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# Using Stochastic Differential Equation for Verification of Noise in Analog/RF Circuits

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**Abstract** Today's analog/RF design and verification face significant challenges due to circuit complexity, process variations and short market windows. In particular, the influence of technology parameters on circuits, and the issues related to noise modeling and verification still remain a priority for many applications. Noise could be due to unwanted interaction between the circuit elements or it could be inherited from the circuit elements. In addition, manufacturing disparity influence the characteristic behavior of the manufactured circuits. In this paper, we propose a methodology for modeling and verification of analog/RF designs in the presence of noise and process variations. Our approach is based on modeling the designs using stochastic differential equations (SDE) that will allow us to incorporate the statistical nature of noise. We also integrate the device variation due to $0.18\mu m$ fabrication process in an SDE based simulation framework for monitoring properties of interest in order to quickly detect errors. Our approach is illustrated on nonlinear Tunnel-Diode and a Colpitts oscillator circuits.

**Keywords** Analog/RF Designs · Noise Modeling · Process Variation · Stochastic Differential Equation · Assertion Based Verification

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## 1 Introduction

In recent years, advanced CMOS fabrication technology has allowed designers to develop smaller, faster, low power analog/RF/digital designs in a single chip, known as systems-on-a-chip (SoCs). Their goal is to address the need for higher performance and functionality in applications such as multimedia, wireless, telecommunications, etc. However, this complex integration among various blocks has brought in additional challenges to the design and verification process due to nonlinear dynamics of analog/RF designs and the influence of process variation on device parameters. For instance, in the case of communication and signal processing designs, high operating frequencies, process variations and environment constraints has made the design susceptible to noise, thereby making the verification unmanageable at the circuit level. At high frequencies, thermal noise is mainly due to the resistance of the channel and the terminal. However, when modeling thermal noise, usually we consider the effect of channel resistance as main dominant source [24]. In general, the sources of noise could be due to unwanted interaction between the circuit elements (e.g., cross-talk noise) or it could be inherited from the circuit elements (e.g., thermal, shot and flicker) [26]. However, by proper layout and shielding techniques, the effect of interference noise can be nullified for a circuit [6]. On the other hand, the inheritance noise can be reduced and cannot be eliminated completely, thereby presenting a practical limit on the performance of electrical circuits and systems [6]. For example, in a RF front-end receiver the noise performance is determined mainly by the interaction between Low Noise Amplifier (LNA), Mixer and Local Oscillator (LO) and also the noise due to each of those individual circuits.

In addition to noise, the fabrication steps such as *Local Oxidation, Photolithography, Ion Implantation,* and *Etching* have created a disparity on the device/circuit parameters across the same die/wafer, thereby influencing the quality and yield of the manufactured circuits [5]. The sources of variations can be classified as *interdie* and *intradie* variations [17]. While, *interdie* variation assumes the device/circuit parameter discrepancies to be the same across *die-to-die* or *lot-to-lot* or *wafer-to-wafer*, it has little influence on the behavior of analog/RF circuits [17]. However, *intradie* variation attributes to the manipulation of device/circuit parameters due to process variation across a single die/wafer [17]. In this case, the devices in the same circuits might have different variations, thereby posing a serious threat on circuit performance and functionality.

Things get even more challenging when moving into deep-submicron process design. For instance, the effect of ultrathin oxide layer (*1.5nm* or less) will make the MOS transistor susceptible to tunneling currents, thereby altering the characteristics of the flicker noise. For thermal noise, due to shrinking technology and manufacturing disparities, carriers can gain enough kinetic energy to move from the silicon substrate to the gate dielectric, thereby altering the device characteristics [31]. The use of deep-submicron processes that give rise to an exponential increase in the number of devices in a design, thereby, creating a need for accurate modeling that could capture the complex noise dynamics of analog/RF/digital interfaces at the component and behavioral levels for a full chip verification.

To fully understand the influence of noise and process variation on the overall performance of the analog/RF design and meet the specification, it is necessary to model and verify all behavior aspects involved in the design. For a given technology, circuit simulators use statistical modeling to study the effect of *intradie* process variation and noise on analog/RF circuit performance [12]. In recent years, many researchers have worked around the problem of expensive simulation run-times by modeling the analog/RF designs at higher level of abstraction. However, with different types of noise sources (thermal, shot and flicker), the challenge faced by the designers is to choose the appropriate type of noise model and

integrate process variations in the verification environment without compromising on simulation run-times and accuracy.

The first step is to find an adequate model for analog/RF designs with noise. Current circuit simulators for statistical analysis of noise involve studying the power spectral density of the circuit. However, for complex circuits, this kind of frequency domain approach can suffer from memory space problem because of increase in the number of higher-order harmonics. Moreover, the usual statistical analysis of stochastic processes does not allow designers to describe the random behavior of a system in time domain. A time-invariant design that operates under small-signal conditions requires a fixed operating point. As a consequence, these kind of models are only applicable for linear systems or a class of nonlinear circuits for which the operating points can be assumed to be stable. However, when the periodic input signal is large, the operating points vary due to nonlinearity, accurate results are only achieved through transient simulation. Due to the statistical behavior of the noise, we are interested in finding a statistical solution rather than a detailed response of the system, therefore we propose to use stochastic differential equations (SDE) [4] as an analog/RF noise model allowing designers to capture the statistical properties of the design in continuous-time. However, the challenge is to incorporate verification techniques that are suited for SDE based modeling.

Verification based on Monte-carlo methods [21] are commonly used to analyze random systems. But, the method is inefficient because it lacks a structure that could characterize the drift and diffusion coefficients in SDEs. Moreover, it inherits the coverage limitation drawbacks from standard simulation methods. Alternatively, in recent years, formal and semi-formal methods have been advocated by many research groups and industries for analog and mixed signal verification [18]. In particular, monitoring techniques based on assertions have been shown to be effective in detecting violation of the design specification thereby avoiding exhaustive checking inherited by traditional circuit simulation and formal methods.

In this paper, we take this verification process a step further, by investigating the usefulness of monitors for analog/RF designs, especially in the presence of noise and process variation. First, we model the analog/RF circuit as an ODE and incorporate stochastic process for the circuit elements in order to get the SDE. We then use the *Euler-Maruyama* method [22] to get the first-order numerical approximation of SDEs in order to study the statistical behavior of noise. We propose an assertion based verification methodology that can handle $0.18\mu m$ process variation and environment constaints for monitoring noise in an MATLAB environment. Our approach is illustrated on a nonlinear Tunnel-Diode oscillator and a Colpitts oscillator circuits in order to study the behavior in the presence of noise and process variation.

The rest of the paper is organized as follows: In Section 2, we review the state-of-the-art in noise modeling and verification of analog/RF designs. In Section 3.2, we discuss about the influence of process variation on passive and active components for $0.18\mu m$ technology. In Section 3, we outline the theory of stochastic differential equations (SDE) and introduce the proposed methodology for monitoring noise in analog/RF designs. Applications with experimental results are illustrated in Section 4, followed by conclusion and future work discussions in Section 5.

## 2 Related Work

In general, noise modeling and simulation are done either using harmonic balance frequency domain techniques [21] or monte-carlo based time domain techniques. The former suffers from memory space problems, while the monte-carlo based full-chip simulation technique is unmanageable at circuit level. But in recent years, several advances have been made in the area of noise modeling and verification of analog/RF circuits based on SDEs. For instance, in [19] the author performs an SDE based phase noise simulation in time domain using the circuit simulator *f*REEDA [9]. Though the phase noise is accurately predicted for a fairly large frequency range, their technique cannot detect undesired behavior or violation. Similar work was conducted in [28], where second-order SDEs are used to simulate the phase noise in a submicron CMOS LC oscillator. In contrast, since we use higher level of abstraction for the SDE models, our proposed methodology can be scaled for larger designs. A behavioral approximation of SDEs based on Euler-Maruyama method for an RL circuit is outlined by the author in [8] and the model is numerically simulated for analysis. A different analysis using model order reduction technique is introduced in [23] for noise modeling of linear time invariant systems (LTI) and simulated using MATLAB [16], but the model proves to be insufficient for time varying systems. A complete simulation based SDE noise analysis of a mixer is performed by the authors in [7] for calculating the optimum value of noise figure and conversion gain. The method provides an effective and accurate simulation result that could be incorporated into the transient analysis of circuit simulators, but suffers from expensive run-times. In summary, the above work emphasize the use of SDEs for noise modeling, but fail to extend them for developing verification methodologies. In contrast, we propose an assertion based verification technique that incorporates $0.18\mu m$ process variations, for monitoring noise in an analog/RF circuit.

Usually, in circuit simulators such as SPICE, process variation can be evaluated using *Worst Case* or *Monte-Carlo* methods [3]. The former provides a fast simulation technique for a single device performance (e.g., speed, power, area). However, the method takes a pessimistic approach for parameter correlations and distribution due to process variation, thus forcing the designers to rely on their experience and intuition in order to achieve accurate results. This may require modification of worst case limits during analysis, thereby increasing the design efforts and costs. On the other hand, MonteCarlo method takes into account a predefined distribution (usually normal distribution) of the device parameter due to process variation. In addition, statistical based simulation for yield analysis and yield optimization for analog/RF circuits have been advocated by many research groups based on worst case files and *e-test* data [14]. The former is appropriate for predicting the variability of a process early in its life cycle, while the latter would better track a maturing process. In summary, all the above methods involve the use of device parameter variation for a particular process at circuit level of abstraction, thereby making the full-chip verification process unmanageable at lower level of abstraction. In contrast, we propose to integrate the process variation device parameters with the verification environment for monitoring noise at higher level of abstraction.

On the verification side, semi-formal methodologies have been presented by many researchers for analog and mixed signal (AMS) designs. The most prominent is the work presented in [20], where the authors proposed a PSL (Property Specification Language [1]) based *offline* methodology for monitoring the simulation of continuous signals. An approach using assertion based verification technique is also introduced in [10]. The authors use systems of recurrence equation (SRE) for modeling and *offline* based monitoring method for verification of analog and mixed signal systems. In contrast to *offline* based verification, the

authors in [11] propose an *online* monitoring technique but, their method cannot support mixed system behavior and any practical property specification language. More recently in [32] the authors have used SREs to express PSL properties for AMS design. They present a tool, named C-SRE, which simulates AMS designs modeled with SREs, reads PSL properties and realizes the online monitoring.

Although there are several papers that target noise modeling and verification separately for analog/RF designs, none of them provides a common platform that could study the effect of noise and process variation for monitoring property of interest. In this paper, we propose, to the best of our knowledge, the first unified methodology to model the noise of an analog/RF circuit based on stochastic differential equation (SDE) and integrate $0.18\mu m$ process variation in an assertion based verification environment.

## 3 Methodology

In this paper, we propose a methodology for modeling and verification of analog/RF designs in the presence of noise and process variations as shown in Figure 1. Thereafter, given an analog/RF design described as a system of *ODEs*, the idea is to include a stochastic process that describes the noise behavior. Due to the statistical behavior of the noise, we propose to use stochastic differential equations (SDE) [4] as an analog/RF noise model in order to capture the statistical properties of the design in continuous-time. Since there are no functions/procedures that can automatically incorporate stochastic processes, we manually generate the *SDEs*.

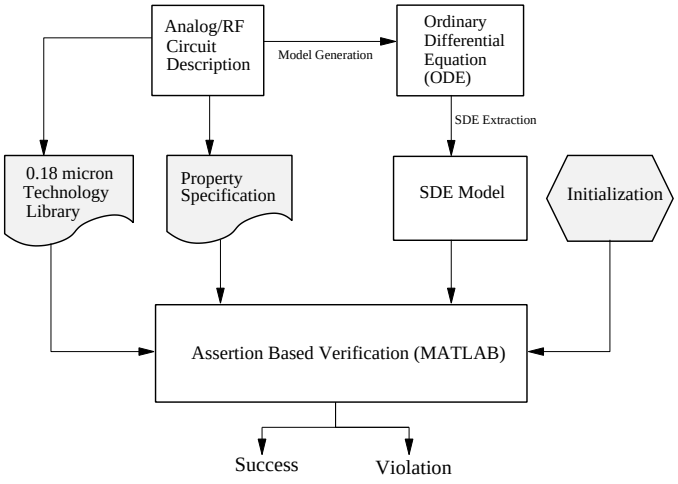


Fig. 1: SDE based Run-Time Verification

Unfortunately, SDEs cannot be solved using traditional mathematics because the Wiener process is non-differentiable, instead we need special techniques such as *Itò* [4] and *Stratonovich* calculus [4]. However, there is not always a closed form solution for SDEs, hence researchers have looked for solving them numerically. The methods based on numerical anal-

ysis are reported in [22], which involve discrete time approximation in a finite time interval over the sample paths. Neglecting the errors due to numerical approximation, the simplest time discretization approach is based on *Euler-Maruyama* approximation [22] which we adopt in this paper.

Based on the process variation, the technology vendors create a library of devices with different process corners such as *slow, nominal* and *fast* [31]. Each process corner characterizes the device in terms of power consumption, speed, area, etc., thereby allowing the designers to choose from a range of devices based on the application and design requirements. Based on the type of process, from the technology library various design parameters in the circuit are calculated for different process corners. These values are passed on as design parameters during simulation.

For environment constraints, this may include the amplitude of the noise, initial conditions of the circuit current and voltages. The environment constraints are passed as a parameter to the design under verification during simulation. The numerical approximation of the design, along with the properties to be monitored, and the environment constraints are coded and simulated in MATLAB [16]. The analog/RF design is simulated within the given environmental constraints and process variation.

An assertion is a piece of code that evaluates the outputs of the simulator and checks whether the property satisfies the design specification. If the property is satisfied, the monitor reports the satisfaction. Otherwise, the monitor can terminate the simulation using *exit* commands at the cycle when the violation occurs. The monitor could be as simple as observing a current or voltage, or could be more complicated, taking several signals, processing and then comparing them against the expected results. The monitors could be constructed so that signals could be observed in an *online* or *offline* fashion. While the online monitoring is more practical when simpler properties are needed to be verified and violations are identified as soon as they occur, offline monitors allow the verification of more complex properties but require the gathering of simulation results which can cost a lot of memory resources. In this paper, we extend the idea of monitoring analog and mixed signal to the next level by developing assertions for monitoring noise in analog/RF designs. In the proposed methodology the monitors are simple finite state machines (FSM) constructed using MATLAB constructs.

### 3.1 Stochastic Differential Equation

An SDE is an ordinary differential equation (ODE) with stochastic process [4]. Given the probability space $\omega$, a stochastic process with state space $E$ is a collection $\{X_t;\ t \in T\}$ of random variables $X_t$ that take values in $E$ for the parameter set $T$. If $T$ is countable, then the stochastic process is *discrete* else *continuous*. Due to statistical properties, a stochastic process can be used to define the randomness in an SDE, thus allowing designers to model the noise behavior of any continuous system. Noise in SDEs is incorporated as an uncorrelated *white gaussian noise* which can be thought of as the derivative of *Brownian motion* (or the *Wiener process*) [4].

**Example.** Consider the RL circuit as shown in Figure 2. The ODE describing the behavior of the RL circuit is given by

$$L\frac{dI}{dt} + RI(t) = V_{in}(t), \quad I(0) = I_0 \tag{1}$$

where the resistance $R$ and the inductance $L$ are design parameters and $V_{in}(t)$ denotes the input source at any time $t$. Assuming white noise process at the input voltage source and at

the resistor, we obtain the following

$$L\frac{dI}{dt} + (R + \alpha\xi_1(t))I(t) = V_{in}(t) + \beta\xi_2(t) \tag{2}$$

where $\xi_1(t)$ and $\xi_2(t)$ are two independent white noise processes, and $\alpha$ and $\beta$ describe the amplitude of the noise. Considering $dW_1(t)$ and $dW_2(t)$ two uncorrelated Wiener processes representing $\xi_1$ and $\xi_2$, respectively, then Equation (2) can be written as:

$$L\frac{dI}{dt} + \big(R + \alpha\frac{dW_2(t)}{dt})I(t\big) = V_{in}(t) + \beta\frac{dW_1(t)}{dt} \tag{3}$$

Rearranging Equation (3), we have the corresponding SDE:

$$dI(t) = \frac{1}{L}\big(V_{in}(t) - RI(t) - \alpha dW_2(t)I(t) + \beta dW_1(t)\big) \tag{4}$$

Consider an *Itò* SDE in differential form

$$dX_t = a(X_t)dt + b(X_t)dW_t \tag{5}$$

where $a$ and $b$ are some functions of time and $W_t$ is a Wiener process. Based on *Euler* approximation, Equation (5) can be written as:

$$X_{n+1} = X_n + a(X_n)\Delta_n + b(X_n)\Delta_n\Delta W_n \tag{6}$$

where for time step $\tau$,

$$\Delta_n = \tau_{n+1} - \tau_n;\ \ \Delta W_{\tau n} = W_{\tau n+1} - W_{\tau n} \tag{7}$$

for *n=0,1,2.....N-1* with initial value $X_0 = x_0$; and for maximum *N* simulation steps.

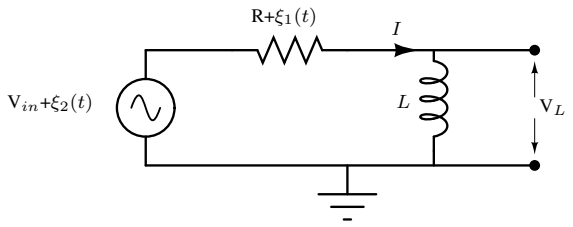


Fig. 2: Series RL Circuit [8].

The recursive method described by Equations (6) and (7) gives only an approximate solution and it is important to note that the solution is close to the *Itò* process [22]. The amount of deviation of the numerical solution is defined by the *absolute error* which satisfies the convergence properties. More accurate numerical methods such as *Milstein, Taylor, Runge-Kutta* that have strong and weak convergence are available in [4] for the numerical simulation of the analog/RF designs.

### 3.2 Process Variation on Device Parameters

Typically, an IC manufacturing process involves a sequence of steps [30]. However, owing to difficulties in controlling the fabrication process at different steps, the variation in device parameter across the die/wafer is unavoidable. For older technologies the influence of process variations on an on-chip device parameter is below 10% [31]. But, in modern CMOS and BiCMOS technologies involving *0.18$\mu$m, 90nm, 65nm, or 45nm*, the on-chip variation is more than 50% [31], mainly caused due to manufacturing uncertainty. Traditionally, the effect of process variation on device parameters are analyzed at lower level of abstraction using circuit simulation. Unfortunately, the occurrence of any bugs late in the design cycle is unacceptable due to short time-to-market window. Hence, there is a growing need to incorporate technology parameters in the verification environment much earlier in the design cycle. However, the challenge would be to calculate and integrate those parameter variation in the verification environment.

In following, we discuss the influence of *0.18$\mu$m* process technology on device parameters that will be adopted in the experiments of the applications part of the paper (Section 4). However, the effect of process variation for other technologies can be extended easily.

**Influence of *0.18$\mu$m* Process Variation on Resistor.** Poly resistor that are built with poly layer deposited over field oxide is used widely to represent resistors in analog/RF designs and its value depends on the sheet resistance ($R_{sh}$) associated with the poly layer. For a given process the variations in poly resistance are mainly due to fluctuation in film thickness, doping concentration, doping profile and annealing conditions [17]. Usually, a *0.18$\mu$m* CMOS process allows 10 to 15% variation in poly thickness which attributes to a similar variation on poly sheet resistance $R_{sh}$. In addition, there is a 10 to 20% variation in $R_{sh}$ due to doping and ion implantation steps. By large, *0.18$\mu$m* CMOS allows 15 to 25% variation in sheet resistance due to the deviation in poly thickness and doping concentration [31]. For instance, the sheet resistance $R_{sh}$ for TSMC *0.18$\mu$m* process is $7.9\Omega/square$ [29]. This means that, for the *slow, nominal* and *fast* process corners, the variation in sheet resistance $R_{sh}$ would be 15%, 20% and 25% respectively. This allows us to use three different values for the resistors in an analog/RF circuit.

**Influence of *0.18$\mu$m* Process Variation on Capacitor.** A typical MOS transistor can be used as a capacitor when operating in the linear region, with the gate representing one plate and drain/source with the channel forming the other plate. Apart from MOS capacitors, current CMOS technology provides *poly-to-poly* capacitors, *metal-to-metal* capacitors and *junction* capacitors. In this paper, we consider the effect of MOS capacitance in *0.18$\mu$m* process, where the variation in MOS capacitance is mainly due to the variation in oxide thickness and the channel doping concentration across the die/wafer. For a *0.18$\mu$m* process, a $\pm$20% variation has to be taken for MOS capacitance which represents a deviation of +20% for *slow* process corner and -20% for *fast* process corner with no changes in capacitance value for *nominal* process corner. However, variation in metal-insulator-metal (MIM) capacitor can be more than 20% [17]. For a given capacitor, a variation of $\pm$20% in the capacitance value is used to represent a *fast* and *slow* process corners.

**Influence of *0.18$\mu$m* Process Variation on MOS Transistor.** A typical MOS transistor can be classified as *enhancement-n* type or *enhancement-p* with positive or negative threshold voltages respectively. For a given technology, the process variation in a MOS transistor may cause a deviation in threshold voltage ($V_t$), length and width of the transistor ($L$ and $W$), oxide thickness ($T_{ox}$) which results in the change in device characteristics across the die/wafer. The deviation in threshold voltage $V_t$ and transconductance parameter $K$ is cal-

culated as [25]:

$$\begin{array}{l} \sigma(\Delta V_t) = \frac{A_{VT}}{\sqrt{WL}} \\ \sigma(\frac{\Delta K}{K}) = \frac{A_K}{\sqrt{WL}} \end{array} \quad (8)$$

In the applications we discuss in this paper, we consider the *0.18$\mu m$* process variation in threshold voltage $V_t$ and transconductance *K*. For instance, given an analog/RF circuit that involve the use of MOS transistor, the variation in threshold voltage is calculated based on equation( 8) and is passed as a *slow, nominal* and *fast* process corner parameter in the verification environment. Table 1 summarizes the technology parameters needed to calculate $V_t$ and *K*.

Table 1: CMOS *0.18$\mu m$* Process Variation [25]

| **Type** | $\mathbf{A}_{VT}$ [$mV\mu m$] | $A_\beta$ [$\%\mu$m] | $\frac{g_m}{I_{DS}}$ [$\frac{S}{A}$] | ($\mathbf{V}_{GS}$ - $\mathbf{V}_T$) [V] |
|---|---|---|---|---|
| nMOS | 5 | 1.04 | 2.08 | 0.96 |
| pMOS | 5.49 | 0.99 | 1.80 | 1.11 |

## 4 Applications

To illustrate the efficiency of the proposed methodology, we have applied it on several benchmark circuits, including a tunnel diode oscillator [27] and a Colpitts oscillator [13].

### 4.1 Tunnel Diode Oscillator

The circuit diagram of a tunnel diode oscillator is shown in Figure 3. The tunnel diode exploits a phenomenon called resonant tunneling due to its negative resistance characteristic at very low forward bias voltages. This means that for some range of voltages, the current decreases with increasing voltage. This characteristic makes the tunnel diode useful as an oscillator. The first step in noise analysis, is to identify and incorporate the sources of noise as a stochastic process in the SDE.

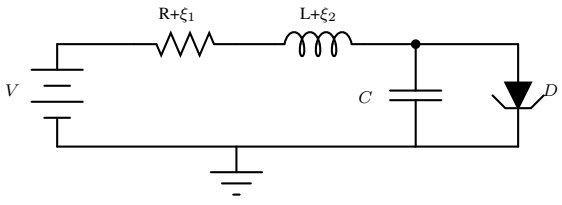


Fig. 3: Tunnel Diode Oscillator

$$\begin{aligned} \dot{V_C} &= \frac{1}{C}(-I_d(V_C) + I_{RL}) \\ \dot{I_{RL}} &= \frac{1}{L}(-V_{C1} - \frac{1}{G}I_{RL} + V) \end{aligned} \tag{9}$$

where $I_d(V_C)$ describes the non-linear tunnel diode behavior given by $I_d(V_c) = V_c^3 - 1.5 * V_c^2 + 0.6 * V_c$. For simplicity, we assume three noise sources, contributed mainly by the input voltage source *V*, the resistor *R* and the inductor *L*. We then derive the SDE model as

$$\begin{aligned} dV_C &= \frac{1}{C}(-I_d(V_C) + I_{RL})dt + (dW_{2t} + dW_{3t}) \\ dI_{RL} &= \frac{1}{L}(-V_C - RI_{RL} + V)dt + \frac{1}{L}dW_{1t} \end{aligned} \tag{10}$$

**Property Observations**
In general, for tunnel diode oscillation, the kind of properties we are interested to verify are: *Is the system behavior the same for the set of initial condition?* or *For which set of parameters values, the circuit oscillates or dies?* The properties that we verify in this paper are the oscillation and no oscillation for different *0.18$\mu$m* process corners shown in Table 2.

Table 2: Tunnel Diode Oscillator Parameters for Property 1

| Parameter | Slow Process Corner | Nominal Process Corner | Fast Process Corner |
|---|---|---|---|
| Sheet Resistance($R_{sh}$)$\Omega/\square$ | 6.715 | 6.32 | 5.925 |
| Resistance ($R$)$\Omega$ | 0.425 | 0.4 | 0.375 |
| Inductor ($L$) H | 1e-6 | 1e-6 | 1e-6 |
| Capacitor ($C$) F | 1200e-12 | 1000e-12 | 800e-12 |
| $V_0$ Volts | 0.131 | 0.131 | 0.131 |
| $I_0$ Amps | 0.04e-3 | 0.04e-3 | 0.04e-3 |

***Property 1:*** We verify that for the set of parameters given in Table 2, there is no oscillatory behavior. The behavior in question is stated as the bounded safety property, meaning for no oscillation property to be satisfied, if for the given simulation time step a certain threshold will not be reached then the property is violated thereby enabling a *violation signal*. The implementation of the assertion as a finite state machine (FSM) for verification of *no oscillation* property is shown in Figure 4.

The FSM has five states namely, *initialization*, *cycling*, *violation* & *cycling, error and stop simulation*. The maximum simulation time, $N_{max}$, and inputs like initial voltage, current and output violation are set in the *initialization* state. As soon as the simulation starts, the FSM goes to the *cycling* state and remains until $T < 3.8 * 10^4$ or $T > 5.5 * 10^4$, where the output voltage $V_c(t)$ is just reported and not observed for any violation. This is because, though the simulation is done from $T = 0$ to $T = N_{max}$, the *no oscillatory* property is verified for the bounded interval $T > 3.8 * 10^4$ to $T \leq 5.5 * 10^4$. As *T* becomes greater than $3.8 * 10^4$, the FSM goes into the *violation* & *cycling* state where the property is verified for any violation, meaning if $V_C(t) < 0.6$, the property is satisfied or else the violation signal is asserted and the FSM enters into the *error* state where it remains there till $T \leq N_{max}$, and then goes to the *stop simulation* state. The results for the verification of Property 1 is

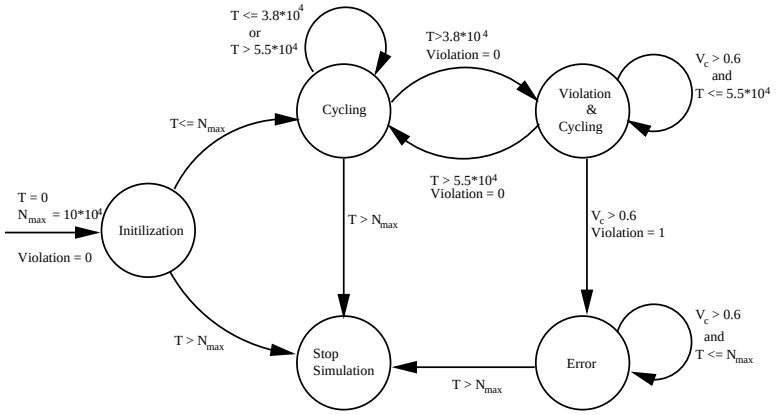


Fig. 4: Property 1 FSM

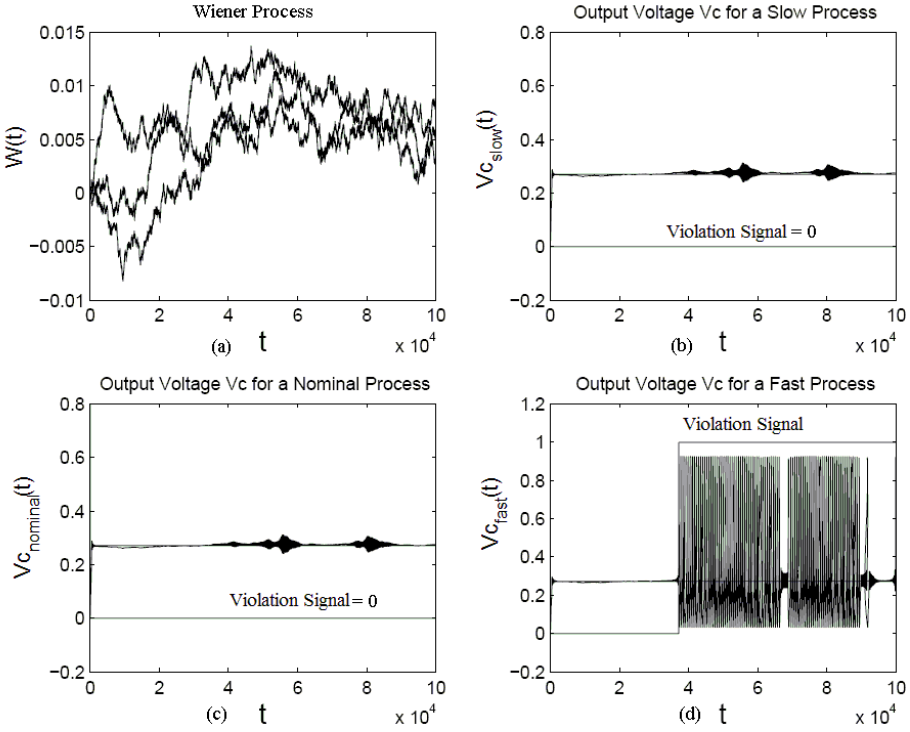


Fig. 5: Property 1 Simulation Result

shown in Figure 5. The results are obtained by simulating the numerical approximation of the SDEs and the assertion using MATLAB. However, the more interesting question that has to be answered is *For the given set of initial conditions and bounded region, how does the influence of noise and process variation affect the oscillatory behavior of the tunnel diode oscillator?* meaning will the tunnel diode oscillator which has been proved to be stable and non oscillating produce the same stable result in the presence of noise?

We simulated the tunnel diode oscillator for three different process corners (*slow, nominal* and *fast*) as shown in Figure 5. The noise is modeled and simulated as a Wiener process as shown in the Figure 5 (a). From the simulation results, Figure 5 (b) and (c), we note that for the given set of parameters, the property is satisfied for *slow* and *nominal* process corners. However, for the *fast* process corner and $T > 3.8 * 10^4$ (Figure 5 (d)) the output has a stable oscillation, thereby detecting a violation. The additive noise $W_2$ and $W_3$ along with the changes in resistor and capacitor due to process variation in the voltage equation $V_c(t)$ causes the tunnel diode oscillator circuit to move to negative resistance region, thereby creating oscillation.

In summary, for the given set of initial conditions and device parameters, though the authors in [27] have verified the *no oscillation* property in the absence of noise and process variation, we demonstrated that the property fail with noise and process variation.

***Property 2:*** We verify that for the set of parameters and initial conditions given in Table 3, the tunnel diode produces a stable oscillation. The oscillation property can be understood as within the time interval [0, *T*] on every computation path, whenever the *Vc* amplitude will reach [0.9v, 1.0v], it will reach this value again until the simulation stops. The proposed monitoring technique based on *if-then-else* makes it difficult to detect oscillation, but can detect failure to oscillate. For oscillation, the values in the current cycle may or may not be the same with the previous cycle, thus making it difficult to detect. We show that within a bounded region, we prove whether the oscillation dies in the presence of noise, meaning, no oscillatory behavior, even though in the noiseless model it was proved to oscillate [27]. The implementation of the assertion as an FSM for verifying the absence of oscillation is shown in Figure 6. The details follow exactly like in Property 1 except that the bounded

Table 3: Tunnel Diode Oscillator Parameters for Property 2

| **Parameter** | **Slow Process Corner** | **Nominal Process Corner** | **Fast Process Corner** |
|---|---|---|---|
| Sheet Resistance($R_{sh}$)$\Omega/\square$ | 6.715 | 6.32 | 5.925 |
| Resistance ($R$)$\Omega$ | 0.17 | 0.16 | 0.15 |
| Inductor ($L$) H | 1e-6 | 1e-6 | 1e-6 |
| Capacitor ($C$) F | 1200e-12 | 1000e-12 | 800e-12 |
| $V_0$ Volts | 0.131 | 0.131 | 0.131 |
| $I_0$ Amps | 0.04e-3 | 0.04e-3 | 0.04e-3 |

region for verification of *no oscillatory* behavior is between $T \geq 4.0 * 10^4$ until $T$=$N_{max}$. The simulation results for the verification of Property 2 are shown in Figure 7. The dotted line represents the output oscillation in the absence of noise, while the bold line represents the output oscillation in the presence of noise and process variation. From the simulation results, we notice that the tunnel diode produces a stable oscillation in the absence of noise. However, in the bounded region from $T \geq 4.0 * 10^4$ until $T = 10.0 * 10^4$, the oscillatory behavior dies out in the presence of noise for all the process corners, thereby detecting a

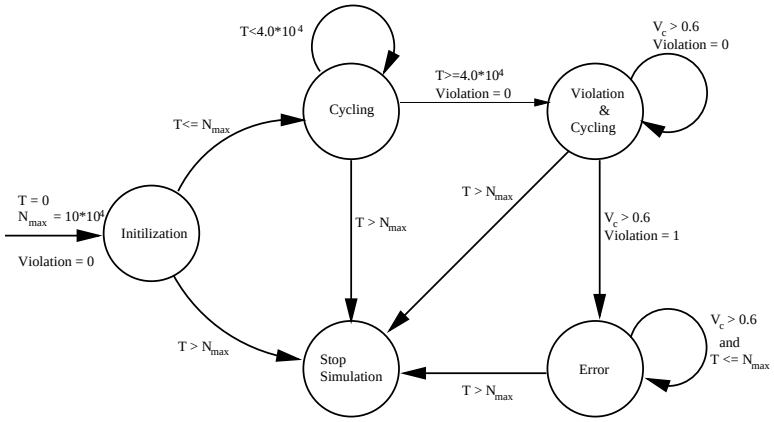


Fig. 6: Property 2 FSM

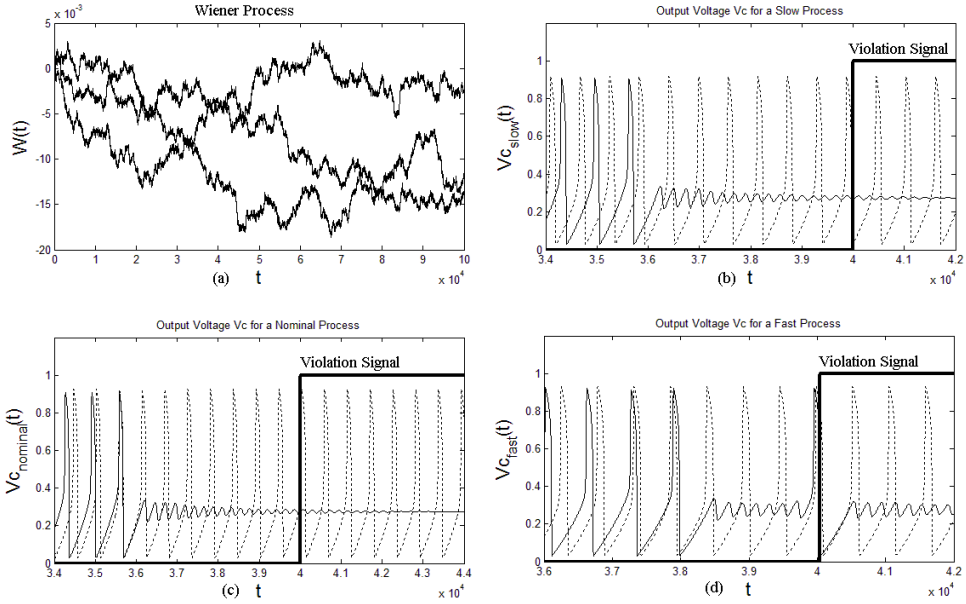


Fig. 7: Property 2 Simulation Result

violation as shown in Figures 7(b), (c) and (d). This shows that the noise and process variation has an adverse effect on the performance of the design under verification. Moreover, we demonstrated that the oscillatory behavior which has been proved in [27] does not hold under noisy and process variation conditions, thereby making our methodology robust in detecting errors.

## 4.2 Colpitts Oscillator

The circuit diagram for a MOS transistor based Colpitts oscillator is shown in Figure 8. For the correct choice of component values the circuit will oscillate. This is due to the bias current and negative resistance of the passive tank.

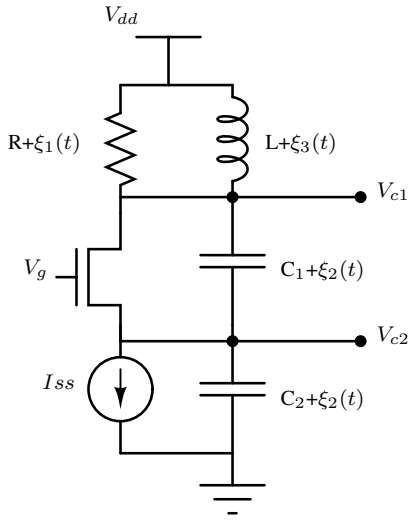


Fig. 8: Colpitts Oscillator

For simplicity, we assume the noise only from the passive elements, while the noise from the MOS transistor is ignored. The first step in noise analysis, is to identify and incorporate the sources of noise as a stochastic process in the SDE. The simplified system of equations that describe the behavior of the Colpitts oscillator is given by:

$$\begin{aligned} \dot{V}_{C1} &= \frac{1.2-(V_{C1}+V_{C2})}{RC} + \frac{I_L}{C} - \frac{I_{ds}}{C} \\ \dot{V}_{C2} &= \frac{1.2-(V_{C1}+V_{C2})}{RC} + \frac{I_L}{C} - \frac{I_{ss}}{C} \\ \dot{I}_L &= \frac{1.2-(V_{C1}+V_{C2})}{L} \end{aligned} \tag{11}$$

where

$$I_{ds} = \begin{cases} 0 \text{ if } V_{C2} > 0.3 \\ K\frac{W}{L}((0.3-V_{C2})(V_{C1}) - 0.5(V_{C1})^2) \text{if } V_{C1}+V_{C2} < 0.3 \\ K\frac{W}{L}(0.3-V_{C2})^2 \text{ if } V_{C1}+V_{C2} \geq 0.3 \end{cases}$$

**Property Observations**

The property that we are interested in analyzing is *whether for the given parameters and initial conditions the circuit will oscillate?* The simulation results in Figure 10 show the variation of output voltages $Vc_1$ and $Vc_2$ with and without noise. The property that we verify in this paper is the no oscillation for different circuit parameters shown in Table 4.

Table 4: Colpitts Oscillator Parameters

| Parameter | Slow Process Corner | Nominal Process Corner | Fast Process Corner |
|---|---|---|---|
| Sheet Resistance($R_{sh}$)$\Omega/\square$ | 6.715 | 6.32 | 5.925 |
| Resistance ($R$)$\Omega$ | 408 | 384 | 360 |
| Inductor ($L$) H | 3e-6 | 3e-6 | 3e-6 |
| Capacitor ($C_1 = C_2 = C$) F | 24e-12 | 20e-12 | 16e-12 |
| Transconductance ($K = 4 * I_{SS}/(V_m^2))$ $Amps/Volt^2$ | 0.0067 | 0.0100 | 0.0133 |
| $V_{dd}$ Volts | 1.2 | 1.2 | 1.2 |
| $I_{SS}$ Amps | 100e-6 | 100e-6 | 100e-6 |

The behavior in question is stated as the bounded safety property, meaning for the given simulation time step oscillation will not occurs if the current cannot exceed a certain threshold. For the no oscillation property to be satisfied, the current through the inductor $I_L$ should

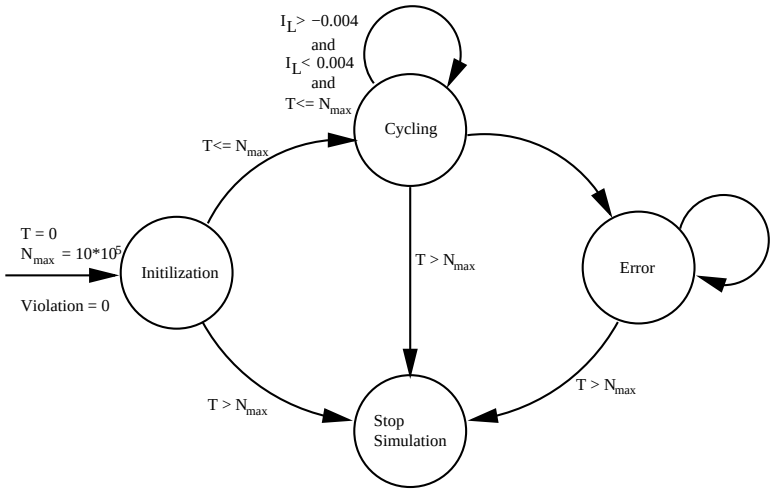


Fig. 9: No Oscillation Property FSM

be bounded within $[-0.004, 0.004]$. If verified to true, the property is satisfied else a violation signal is enabled. The implementation of the assertion as an FSM for verification of no oscillation property is shown in Figure 9.

The FSM has four states namely, *initialization*, *cycling*, *error and stop simulation*. The maximum simulation time, $N_{max}$, and output violation are set in the *initialization* state. As soon as the simulation starts, the FSM goes to the *cycling* state and remains until $T \leq N_{max}$

and there are no violations observed. If the inductor current crosses the bounded threshold, the FSM asserts the *violation* signal and goes into the $error$ state where it remains there till $T \leq N_{max}$ and then goes to the *stop simulation* state.

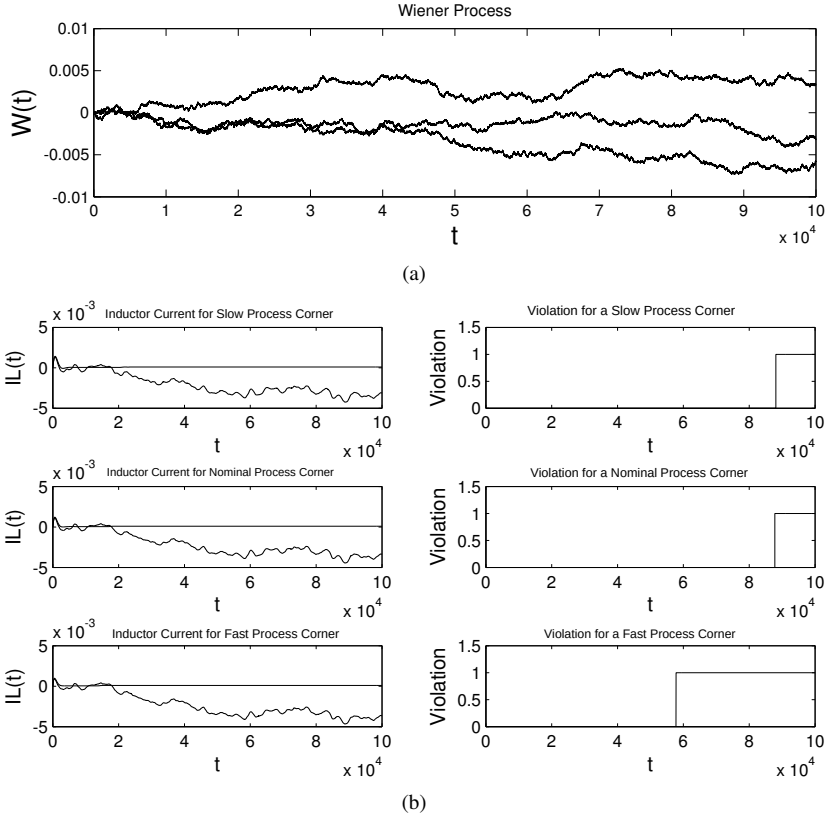


Fig. 10: Simulation Result of Colpitts Oscillator

From the simulation results, we notice that the Colpitts oscillator does not oscillate in the absence of noise. However, for the *slow, nominal* and *fast* process corners in the bounded region from $T$=$5.8 * 10^4$ until $T$=$10.0 * 10^4$, the variation in device parameter and additive noise in the inductive current equation has caused an increase in the inductive current, thereby detecting violation at $T$=$9.0*10^4$, $T$=$8.9*10^4$ and $T$=$5.9*10^4$ as shown in Figure 10 (b), respectively. This shows that the noise and process variation has an adverse effect on the performance of the design under verification.

### 4.3 Discussion

The above simulation results were derived for one particular set of Wiener process and for *0.18$\mu$m* process technology. The FSM for verifying the property of interest is constructed using *if-then-else* MATLAB constructs. The methodology could be easily extended for other

technologies by calculating device parameters based on process variation for *slow, nominal* and *fast* process corners. The values of the Wiener process depends on the random number generator of the system and so we may find different sets of $W_1$, $W_2$ and $W_3$ during each simulation run. Therefore we conclude that, for this particular set of parameter values of $W_1$, $W_2$ and $W_3$ and initial conditions, the properties in the tunnel diode and Colpitts oscillators are violated, but, we can get a different set of values for the Wiener processes for which the property holds. Hence, the verification has to be done for multiple trajectories before concluding the correctness of the design.

## 5 Conclusion

In this paper, we have presented a practical assertion based verification methodology for noise and process variation in analog/RF designs. The approach is based on modeling the noise using SDEs and numerically simulating, in MATLAB, the model with $0.18\mu m$ fabrication process parameter variations, and monitor the property of interest in an online fashion, thereby avoiding large simulation run-times. We have used the methodology to verify the oscillatory behavior of a tunnel diode and Colpitts oscillator circuits. We showed that the properties that are satisfied without noise, have failed in the presence of noise and process variation, thereby proving that the proposed verification environment is efficient in finding bugs. This process is much more reliable than manual (visual or textual) inspection of simulation traces which will cost lots of time.

Due to the statistical property of the noise, we plan to develop probabilistic monitors based on *Markov chains* and incorporate process variations for monitoring noise. In Markov chains, given the *present state*, *future states* are independent of the past states and will be reached based on probabilistic process instead of a deterministic one. This allows us to realize quantitative study of continuous systems. Our proposed approach currently is limited to first-order SDEs and we would like to investigate higher order designs such as $\Delta\Sigma$ modulator and phase locked loops (PLL) that involve the use of second order SDEs with one-dimensional and multi-dimensional noise. We also need to test the feasibility of other numerical models such as Taylor approximation [22] for accuracy, speed and stability and decide on the appropriate ones for practical applications. Therefore, we will be able to achieve a robust verification environment capable of handling probabilistic and deterministic properties of analog/RF designs in the presence of noise and process variation.

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