A Study of New Low-Cost Fabrication Methods of Micro- and Nano-scale Building Blocks for Crystalline Silicon Solar Cells

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ABSTRACT

A Study of New Low-Cost Fabrication Methods of Micro- and Nano-scale Building Blocks for Crystalline Silicon Solar Cells

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Energy is the number one problem facing humanity today. Solar cells can capture and transform clean and abundant solar energy into electricity. However, their efficiency must increase and their material and fabrication costs must decrease in order for them to be considered as a viable alternative to the fossil fuels. This research explores and studies new methods for fabricating silicon micro- and nano-scale structures in an economical way as building blocks for crystalline silicon solar cells to lower their overall manufacturing cost while increasing their overall efficiency.

A novel cost-effective approach was proposed and studied for texturing the crystalline silicon using the gas lift effect (GLE). The new proposed method takes advantage of the generated bubbles to create a gas lift effect that increases the surface wetability and removes undesired gas bubbles during the texturing process. This technique requires 50% less chemicals and 60% shorter etching time to achieve the same reflectivity.

Modeling and simulation techniques were used to investigate and elucidate the fluid flow patterns inside the silicon texturing system operating under the new GLE approach. The simulation tool validated the correlation of the lower fluid velocity with the reduced surface coverage, uniformity and subsequently less optimal surface reflectivity. Various inlet designs were modeled and evaluated using a simulation tool for optimal performance. The best inlet design was fabricated and tested resulting in the validation of

the simulation work and significant improvement in the GLE texturing system performance.

Two solar cell devices, one based on the novel GLE texturing approach, and the other based on the conventional method, were designed, fabricated and characterized. The application of the new GLE texturing approach resulted in considerable improvements in overall power efficiency of silicon solar cells without any additional increase to the production cost.

Micro and nano structures can enhance optical absorption characteristics and help with providing a more direct path for charge transport to the contacts resulting in an increased overall efficiency. An array of silicon micro-rods with nano-tip was fabricated through a novel low cost multistage approach. The transformation of the pyramid-covered silicon surface to the array of free-standing micro-rods with nano-tip as well as their growth mechanism was investigated. At lower than 80% pyramid coverage, the number of nanostructures dropped dramatically and no nano-structures were obtained at low surface coverage values of less than 50%.

Transparent conductive films (TCFs) can be a viable low-cost alternative to the expensive Indium Tin Oxide (ITO) used in solar cells. A novel thermoplastic nanocomposite of copper nanowires and polymethylmethacrylate was developed by solution mixing technique. Thin films of highly conductive nanocomposites were fabricated by solution casting. This investigation demonstrated that the addition of electric conductive nanoscale fibers to a polymer solution at low concentration levels can transform the plastic to highly conductive phase while maintaining an acceptable transparency of about 55%.

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List of Acronyms

AM	Air Mass
C-Si	Crystalline Silicon
CuNWs	Copper Nanowires
DI	Deionized
EDA	Ethylene Diamine
EDX	Energy-dispersive X-ray
EMI	Electromagnetic Impedance
FEM	Finite Element Method
FESEM	Field Emission Scanning Electron Microscopy
FET	Field Effect Transistor
FF	Fill Factor
FTO	Fluorine-doped Tin Oxide
GLE	Gas-Lift Effect
HF	Hydrofluoric Acid
IB	Intermediate Bands
IBSC	Intermediate Bands Solar Cell
IPA	Isopropyl Alcohol
ITO	Indium-doped Tin Oxide
NW	Nanowire
PC	Polycarbonate
PMMA	Poly-methyl Methacrylate
PSI	Porous Silicon
PV	Photovoltaics
RCA	Radio Corporation of America
RHEED	Reflection High-energy Electron Diffraction
RPM	Rounds Per Minute
SEM	Scanning Electron Microscope

SRO	Silicon-rich Oxides
SWR	Solar-weighted Reflectivity
TBA	Tertiary Butyl Alcohol
TCF	Transparent Conductive Film
TF	Thin Film
TGA	Thermal Gravimetry Analysis
TMAH	Tetramethylammonium hydroxide
VLS	Vapor Liquid Solid

List of Symbols

J	Current density	[Acm^{-2}]
ρ	Fluid density	[kg/m^3]
k	Turbulent kinetic energy	[J/kg}
μ_t	Eddy viscosity	[N*s/m^2]
ε	Turbulent dissipation	[J/kg*s}
ϕ_m	Mass content	[%]
ϕ_v	Volume content	[%]
Ω	Resistance	[Ohms]
ρ_s	Surface Resistivity	[Ω/sq]
N_{BC}	Background concentration	[cm^{-3}]
t	Difusion time	[min]
x_j	p-n junction depth	[µm]
η	Efficiency	[%]

1 Introduction

Richard Errett Smalley was a professor of chemistry, physics and astronomy at Rice University. He was awarded the Nobel prize in chemistry for the discovery of a new form of carbon, buckminsterfullerene (“buckyballs”) in 1996. In some of his later presentations, he presented a list entitled “Top Ten Problems of Humanity for Next 50 Years”. The top four problems on his list were: 1) Energy, 2) Water, 3) Food and 4) Environment. According to the US Energy Information Administration report released in 2008, between 1996 and 2006, the world’s total output of primary energy increased at an average annual rate of 2.3 percent. According to the same report, fossil fuels (petroleum, coal and natural gas) accounted for a total of 86% of our energy consumption. Aside from being a finite source of energy and mostly located in politically instable regions of the world such as the Middle East and North Africa, fossil fuels are responsible for an increase in greenhouse gases, acid rain, and the degradation of public health [1]. At the same time that our energy sources are being depleted, the earth population is increasing with an alarming rate resulting in an enormous energy crisis in the very near future. To meet the energy demand of all households worldwide, energy supplies must double by 2050 [2].

One of the largest (almost unlimited) and cleanest sources of energy is sunlight. It provides the Earth with 4.3×10^{20} Joules of energy in one hour while the entire Earth’s consumption of energy is about 4.1×10^{20} Joules per year. As a result, solar electricity is forecasted to become a \$50-\$90 billion industry growing at a rate of 40-50% per year [3]. However, there is still a huge gap between the present use of solar electricity and its enormous unexplored potential. This gap is a direct result of two major challenges facing the scientists working in the photovoltaic area; 1) the efficiency challenge, and 2) the cost challenge. There seems to be always a trade-off between the two. More expensive materials and more complex fabrication techniques can lead to higher efficiency solar cells. The question remains as to how to improve one without sacrificing the other. How can we lower the cost of today's solar cells so they can compete with the traditional sources of energy without losing the battle in the efficiency front?

1.1 Motivation

Making the change to renewable energy such as solar can slow or even eliminate global warming and resolve most of our energy and environmental problems. Harnessing the sun's unlimited energy has put a lot of people to work within the research communities around the world. Scientists are studying and exploring new photovoltaic technologies that can bring down the material and production cost while increasing the efficiency, reliability and durability, to a point where the renewable energies can compete with the fossil fuels. Any new technology needs to be justified in terms of its impact on the environment. However, it would also have to make sense economically. In September of 2011, a solar research and manufacturing company in Northern California, Solyndra inc., filed for bankruptcy. This well-funded company (more than half a billion US dollars) was unable to bring the cost of its solar panels low enough to compete with other traditional sources of energy. In 2012, more than 25 well funded companies had to close as they could not lower their cost to compete. The cost of photovoltaic (PV) electricity today is still not competitive when compared to that of the conventional sources of energy such as fossil fuel or coal, but it is quickly getting there.

Since the very first bulk Si-based solar cell, having an efficiency of only about 5-6%, researchers have been working very hard to come up with new approaches to increase the efficiency while decreasing the material and manufacturing cost of new generation solar cells. Many techniques have been utilized to increase this efficiency to up to about 25% [4], which is very close to the theoretical limit for a single junction under one sun illumination of about 31% [5]. Other techniques such as the use of concentrators or tandem junctions have also been used to narrow the gap between the Shockley-Queisser and the thermodynamic limit. It has been shown and demonstrated experimentally, that a four-junction cell can achieve an efficiency of about 71% under maximum concentration [6]. In general, multi-junction cells have shown promising efficiencies but are rather expensive and complicated to manufacture.

Other semiconductors that support and can possess intermediate bands (IB) between their valence and conduction bands can absorb low-energy photons in a two-photon process that promotes charge carriers to the conduction band. The intermediate band solar cells (IBSC) have the potential for a maximum of about 63% according to the theoretical analysis [7], but on the other hand, they have a rather high fabrication cost.

Texturing is another approach for increasing the light absorption, resulting in an increased overall efficiency. For example, texturing the surface of the silicon can act as an effective coating technique improving the light absorption, leading to the generation of more electricity and therefore, increasing the overall efficiency [8]. Nanostructures such as nanowire arrays have been studied and shown to be effective surface coatings for silicon solar cells [9]. One of the most economically available texturing techniques is the wet anisotropic etching method. However, there are many challenges for this economical silicon texturing process. One major issue is the gas blanketing effect that occurs during the silicon texturing process. The root of the problem comes from the fact that the generated hydrogen bubbles, with typical diameter range of 2-3 mm, stick to the surface long enough to interrupt the chemical reaction between the alkaline solution and the silicon surface. As a result, there is a loss of texturing surface coverage and uniformity. The conventional approach to remedy this gas blanketing effect is to add surfactants such as Isopropyl Alcohol (IPA) to the etching solution [10]. However, as a result of adding IPA, the etching rate decreases and pyramid shape irregularity increases. It also leads to smaller average pyramid size and therefore, not allowing us to have more control over the morphology and the particle average size on the silicon surface. On the other hand, IPA is volatile in a heated etching bath. The boiling point of IPA is around 82° C. Therefore, at the etching temperature of 90° C, it must be constantly added to the solution during the etching process resulting in difficult control and higher consumption of IPA.

The trade off for obtaining higher efficiencies has always been higher cost. The traditional approaches have usually been very costly. The search for large-scale higher efficiency and lower manufacturing and material cost PV technologies remains an ongoing challenge for the scientific community.

1.2 Objectives

This research is primarily concerned with the cost and efficiency challenges facing silicon-based photovoltaic devices today. Reliability and durability issues will not be the focus, and therefore, will not be addressed in this research study. An attempt was made to apply nanotechnology in addressing the efficiency issue by exploiting methods to enhance the capture and conversion of photons into electricity. We also addressed the overall cost as a result of lowering the material, fabrication and manufacturing expenses by applying new silicon texturing methods using the GLE phenomenon. Industrial electrolytic cells that produce gas at one or both electrode surfaces are usually designed to take advantage of this phenomenon to generate gas lift electrolyte circulation by creating a narrow gap between the two electrode surfaces [11]. Good electrolyte circulation provides transport of electro-active species to the electrode surface as well as taking bubbles away from the electrode surface. Internal gas lift circulation in a well-designed electrochemical cell is much more efficient than mechanically pumped circulation [12].

A three-stage low-cost process was used to fabricate a nanostructure as a basis for potentially higher efficiency and lower cost solar cells. New silicon texturing method, proposed in this research study, take advantage of less complicated and more effective natural occurring phenomenon such as GLE to improve the texturing process by providing more control over the morphology as well as the dimensions of these nanostructure building blocks. On the other hand, the cost of texturing is lowered by the reduction of both the required surfactant and the etching time as a direct result of using the GLE system. A modeling of the GLE system was performed based on a proven finite element method (FEM) to optimize this approach for a low-cost viable industrial level (scale up) texturing method for photovoltaic applications.

An attempt was made to fabricate a transparent conductive film as a lower-cost alternative to Indium-doped Tin Oxide (ITO). Further research and study will be needed to optimize the films as a viable solution and a low-cost alternative to ITO.

1.3 Literature review

The search for large-scale higher efficiency and lower material and manufacturing cost solar cells is an ongoing research topic among the scientists in this field. Semiconducting nano- and microstructures can be predictably fabricated in single-crystal, poly-crystal and amorphous forms by controlling all the morphology parameters including doping. They are being utilized as building blocks in photodiodes [13], photovoltaics [14], field effect transistors (FET) [15], and many other electronics devices. In this chapter we present a literature review on the previous works in fabrication and characterization of micro- and nano-scale structures as they apply to photovoltaics.

1.3.1 Nanotechnology

Nanotechnology is a collection of topics in various domains dealing with the structure of materials and devices with a critical length of <100 nm in at least one of the dimensions. Materials and devices at this size scale demonstrate significantly different physical, chemical and biological properties. Nanotechnology is a multi-disciplinary and unifying science with exciting and promising applications in clean and renewable energy field. During the very recent years, there has been a significant increase of interest level in the application of nanotechnology in PV technologies from the research community.

1.3.2 Nano photovoltaic (nano-PV) classifications

Since 1954, when Fuller and Pearson demonstrated solar cells based on a single p-n junction using single-crystal Si with efficiencies of 5-6%, solar technologies have come a long way in terms of their efficiencies and costs. Solar cells can be categorized into three generations:

1. 1st generation PV – Si wafer based solar cells
2. 2nd generation PV – Thin Film (TF) PV systems

3. 3rd generation PV – Multijunction/Tandem/Intermediate Band/Up&Down Conversion Solar cells

In each of the above mentioned generations, the ongoing challenge facing the research community is how to increase efficiency while lowering their material and fabrication costs. The solar cell efficiency (%) is defined as [Power out (W) / (Area (m^2) x 1000 W/m^2)] x 100%, where 1000 W/m^2 is defined as 1 Sun radiation. Regardless of the generation, there is still a big gap between the theoretical efficiencies and the experimental ones.

The use of nanostructures in PV technologies can play an important role with improvements in both the efficiency and cost. Based on their application and dimensionality, these nanostructures can be classified in four major groups [16]:

(1) nanocomposites [3D]
(2) quantum wells [2D]
(3) nanowires and nanotubes [1D]
(4) nanoparticles and quantum dots [0D]

However, in order to achieve better control over the size at nano-scale, one needs to have a good handle on microtechnology, especially if a top-down fabrication is intended for these nano-scale structures.

1.3.3 Texturing silicon solar cells

Silicon is the second abundant element on earth and its raw material cost has been steadily decreasing over the last few years. Just a few years ago, many industry experts believed that getting the cost of silicon-based solar cells below US$1/W would be difficult. At this point, we are already below US$0.50/W with still clearly a significant margin for reduction. The current trend in the cost reduction and the existence of advanced technologies in electronics has created great opportunities for silicon-based solar cells to become the obvious choice of technology among all the existing ones at this point in time.

In the solar cell industry, the surface of the silicon is textured to decrease the reflectivity. One of the most effective and least costly techniques for silicon texturing is the anisotropic wet etching of silicon surface using strong bases such as KOH and TMAH [17]. In aqueous solutions, Tetramethyl Amonium Hydroxide (TMAH) appears in its dissociation form as the hydroxide OH^- and the TMA^+ ions:

$(CH_3)_4NOH \rightarrow (CH_3)_4N^+ + OH^-$

The redox reaction can be written as:

$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2$

To summarize the etching of silicon in the TMAH solution, the overall reaction can be written as follows:

$Si + 2(CH_3)_4NOH + 2H_2O \rightarrow 2(CH_3)_4N^+ + SiO_2(OH)_2^{2-} + 2H_2$

In order to obtain uniform surface texturing using alkaline etchants, one must improve the wet-ability of the surface and facilitate the removal of the generated hydrogen bubbles from the surface. By increasing the uniformity and coverage of the textured silicon surface, more photons are absorbed resulting in decreased reflectivity. In order to achieve high texturing coverage and more uniformity, the conventional approach is to use a surface active agent (surfactant) such as IPA that would increase the wet-ability and facilitate the release of hydrogen bubbles from the silicon surface [10] [18]. However, IPA is volatile in a heated etching bath. The boiling point of IPA is around 82° C. Therefore, at close to or above the boiling point temperatures, it must be constantly added to the solution during the etching process resulting in difficult control and higher consumption of IPA. Also, as IPA concentration increases, the etching rate starts to decrease drastically [19] [20]. In some experiments the IPA was eliminated all together from the etching solution and replaced by dissolved silicon or various ionic surfactants to achieve texture uniformity [21] [22]. Other approaches include the use of other types of additives such as Tertiary Butyl Alcohol (TBA) [23] [24]. Using a metal grid to trap the hydrogen bubbles as a more controlled way to achieve the same favorable outcome has also been reported in the literature [25]. In all the above approaches, in order to obtain reproducible results, the silicon surface is first cleaned using a method called the RCA procedure. This method was developed by Werner Kern while working for Radio Corporation of America (RCA) back in 1965. Unwanted metal particles, such as sodium (Na), aluminum (Al), dust and native oxide, are the most common types of unwanted impurities that a silicon wafer surface may be infected with during storage or fabrication. This cleaning process is performed in 3 steps:

(1) Removal of the organic contaminants (organic clean) using a 1:1:5 solution of NH_4OH (ammonium hydroxide) : H_2O_2 (hydrogen peroxide) : H_2O (DI water) for about 5-10 min. at 80 °C. This step creates ~10Å silicon dioxide layer which will be removed in the next step.

(2) Removal of thin oxide layer (oxide strip) using 1:50 solution of hydrofluoric acid (HF) : DI water for about 1-2 minutes at 25°C (created hydrophobic surface).

(3) Removal of metallic contaminants (ionic clean) using a 1:1:6 solution of HCl (hydrochloric acid) : H_2O_2 : DI water for about 5-10 minutes at 80 °C.

1.3.4 Porous silicon (pSi)

Porous silicon is composed of a silicon skeleton permeated by a network of pores. It can be formed by electrochemical anodization of bulk silicon in an HF electrolyte. Figure 1-1 shows a top view of pSi surface. The electrolyte solution is a combination of aqueous HF and ethanol. Constant current is applied to control the porosity since they are directly related.

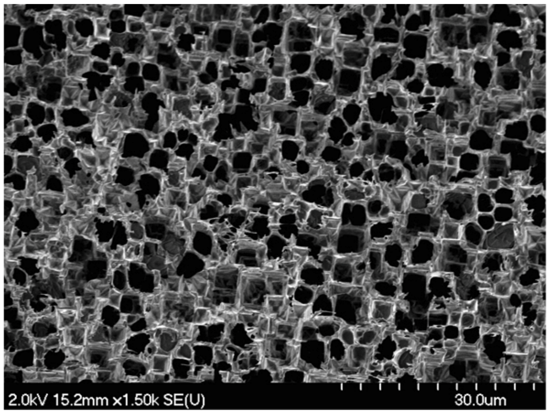


Figure 1-1: The top view of the pSi layer

It is possible to define the characteristics of a particular porous silicon layer in a number of ways. The methods of identification include the layer thickness, average pore width, and porosity. The specific nature of a layer depends on the parameters involved such as HF:Ethanol concentrations, anodization time and current, substrate doping type and the impurity concentration. For example, for the same current density, as the acceptor doping concentration increases, the growth rate of the layer increases and the porosity decreases [26]. For the same doping concentration, as the current density increases, so does the porosity. Figure 1-2 illustrates the correlations between current density and acceptor type doping with porosity. It has been shown that p-type doped silicon results usually in a network of very narrow pores with smaller radius (2 nm) [27]. Heavily n-type silicon produces larger-size pores. It has also been found that porosity is very sensitive to doping. Heavily p-type silicon generates more uniform pore size distribution than the n-type silicon though.

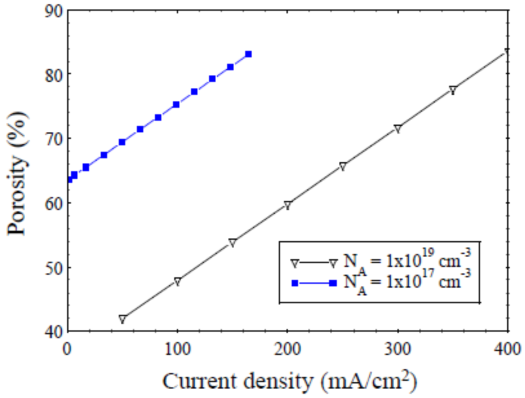


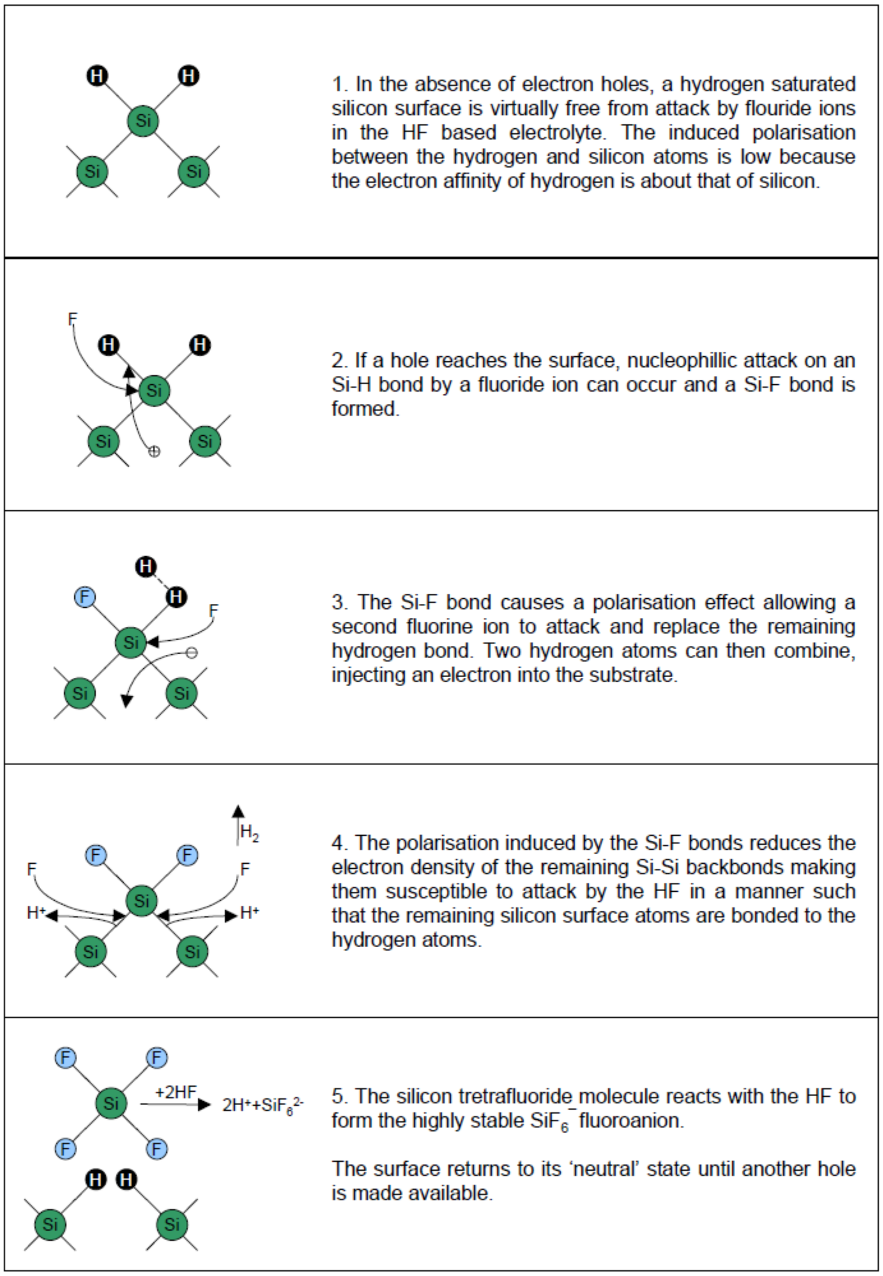
Figure 1-2: Effect of current density and doping on porosity [28]

Because of its small skeletal volume area, pSi layers can be selectively dissolved in dilute NaOH while the crystalline Si substrate remains minimally etched. By careful control of the etching process forming pSi, novel structures can be fabricated [29].

1.3.5 Formation of pSi

The anodization reaction requires the presence of holes [30]. Therefore, the natural choice for substrate doping is low-doped p-type silicon. However, n-type substrates can also be employed for porous silicon fabrication, provided that generation mechanism for excess holes are available. For example through using a constant (35W) white light beam. Dissolution of silicon occurs only under anodic polarization. However, at high anodic currents, the silicon surface goes under electropolishing. On the contrary, at low anodic currents, the surface morphology is covered mostly by a dense array of channels penetrating into the bulk of the silicon with a depth that correlates with the etching time [31]. The longer the time, the deeper will be the pores.

Amongst the various models proposed for the silicon dissolution reaction, the mechanism presented by Lehmann and Gösele is the most accepted in the porous silicon community. The formation of porous silicon involves reactions of Si – Si, Si – H, Si – O, and Si – F bonds at the surface of the silicon crystal. The electronegativity of the elements plays an important role in the formation of pSi. Bonds such as Si-O and Si-F are more polar than others in an aqueous solution and therefore making the silicon atom susceptible to being attacked by molucules or atoms with a free pair of electrons (nucleophilic). Figure 1-3 lists the 5 steps in the process described by Lehmann and Gösele.



1. In the absence of electron holes, a hydrogen saturated silicon surface is virtually free from attack by flouride ions in the HF based electrolyte. The induced polarisation between the hydrogen and silicon atoms is low because the electron affinity of hydrogen is about that of silicon.

2. If a hole reaches the surface, nucleophillic attack on an Si-H bond by a fluoride ion can occur and a Si-F bond is formed.

3. The Si-F bond causes a polarisation effect allowing a second fluorine ion to attack and replace the remaining hydrogen bond. Two hydrogen atoms can then combine, injecting an electron into the substrate.

4. The polarisation induced by the Si-F bonds reduces the electron density of the remaining Si-Si backbonds making them susceptible to attack by the HF in a manner such that the remaining silicon surface atoms are bonded to the hydrogen atoms.

5. The silicon tretrafluoride molecule reacts with the HF to form the highly stable SiF_6^{-} fluoroanion.

The surface returns to its ‘neutral’ state until another hole is made available.

Figure 1-3: The process of pSi formation described by Lehmann and Gösele [32]

1.3.6 Applications of pSi as a sacrificial layer

Nanostructured silicon was first produced by Ingeborg and Arthur Uhlir at Bell Labs in the 1950s [33]. At the time, they were studying electropolishing of silicon surfaces using aqueous solutions of HF. They observed that, at low current densities, it results in a sponge-like structure.

The increased level of interest in pSi resulted primarily from the proposal in 1990 that efficient visible light can be emitted from high porosity structures. Porous silicon has been found to be an excellent anti-reflection coating against incident light when it is compared to other anti-reflection coatings. It also exhibits good light-trapping of a wide wavelength spectrum, making it a good candidate for fabricating high efficiency solar cells [34]. Silicon nanocrystallites or nanoporous silicon are crystalline materials with dimensions measured in nanometers and a nanoparticle with a structure that is mostly crystalline in the interior. They are generally fabricated by the precipitation of excess silicon in silicon-rich oxides (SRO).

The micromachining fabrication method using porous silicon has been utilized to manufacture structures such as cantilevers beams [35], bolometers for thermal measurements, bridges, flow channels and wires [36]. It has been reported that, during the formation of pSi, a homogeneous nanoporous layer (2-3 microns thick) forms first at the surface and then a columnar structure field with nanoporous body (6 microns thick) develops underneath. When using NaOH to etch pSi, nanoporous silicon dissolves first and a macropore structure appears. For a prolonged immersion time, or higher concentration of NaOH, most of or even the entire sacrificial pSi layer is dissolved and the underneath micro or nanostructure appears [37].

1.3.7 Use of micro and nano-scale structures for antireflection coatings

Antireflection coating is used to increase the light absorbance in solar cells. The conventional method for coating is through the use of materials such as Titanium Dioxide

(TiO_2) and Silicon Nitride (Si_3N_4) forming a thin film over the substrate such that for a specific wavelength the incident and reflected wave will interfere and cancel out resulting in no reflection. This can only be achieved with materials with specific refractive index so there are only limited types of material that can be used.

Another approach is through the use of optical nanostrucutres. In these nanostrucutres, the grating period is so small so that the incident light can only be refracted and not diffracted. This is a characteristic of an effective medium. For pillar diffraction grating structures to act like an effective medium, there are conditions that must be met [9]. These conditions are dependent on many parameters such as grating period, refractive index and the mode. For a periodic array of nanorods, approximations are available for the effective refractive index of the mode in the grating area [38]. Such array of nanorod structures can also provide a gradual transition of the refractive index between air and the underlying substrate (like silicon) resulting in a reduction in the reflectance [39].

1.3.8 Applying silicon nanowire array structure to PV

Nanowires are considered 1D nanostructures where carriers are confined in 2 out of three dimensions. Nanowires (NWs) and nanorods are elongated solid nanostructures with a high aspect ratio and may be synthesized by many methods, including laser ablation [40], chemical vapor deposition [41], solution-based chemical synthesis [42], critical point synthesis [43], electrochemical depositio, wet etching [45], and dry etching of nanopatterned features [46].

The nanowires/nanorods provide a more direct path for charge transport to the contacts when utilized as part of a solar cells structure. Based on the research results obtained by Tian, Kempa and Lieber (2008) [47], both axially and radially grown semiconductor nanowires can be fabricated using the vapor-liquid-solid (VLS) method. In their experiment, the authors fabricated a p-i-n type single nanowire using Silicon (n-Si/i-Si/p-Si). In this gold-nanoparticle catalyzed VLS method, depending on the concentration of Au with respect to Si and the temperature, one can control whether to achieve radially grown or axially grown p-i-n type single nanowires.

Nanowire structures also help with achieving enhanced optical absorption characteristics. It was found, by directly comparing the optical properties of solid Si films to nanowire films, that the optical reflectance decreases significantly as expected due to the better index matching of the nanowire array to air [48]. In combination with total transmission measurements it was shown that the optical absorption was enhanced significantly compared to the solid film over all the wavelengths of interest for photovoltaic. NW arrays are potentially more advantages compared to the polycrystalline thin films [14]. This is due to their direct conduction paths for photo-generated carriers resulting in higher carrier collection efficiency. Also, NW arrays have significantly smaller optical reflectance and enhanced light absorption when compared to thin films.

Semiconductor nanowires are attracting intense interest as a promising material for solar energy conversion for the new-generation photovoltaic (PV) technology. In particular, silicon nanowires (SiNWs) are under active investigation for PV applications because they offer novel approaches for solar-to-electric energy conversion leading to high-efficiency devices via simple manufacturing [49].

Silicon is not probably the best material for solar cells due to its indirect band gap. However, Si is the leading material used in the PV industry today since it is the second most abundant element in the earth’s crust, making it a relatively inexpensive semiconductor. There is also a strong technological base for silicon due to the success of the electronics industry. This fact has also contributed to the popularity of Si-based solar cells.

Silicon nanowire-based solar cells have been proposed both by many researches [49] [50] [51]. Tsakalakos et al, and Kayes et al have shown that the Si nanowire-based solar cells can yield efficiencies of up to 18% depending on their length and diameter as well as, of course , quality (carrier life time). The advantage of these solar cells over the Si-bulk based is that the lateral diffusion of minority carriers to the p-n junction is in the order of 50-200 nm rather than a few microns in the Si bulk solar cells.

Tsakalakos et al created the Si nanowire solar cells by first using a p-type (100) substrate. The p-type nanowires were created using an etching technique followed by a deposition of n-type amorphous silicon on the nanowire array. A planar Si cell was fabricated as reference using the same process. It was shown that the efficiency of the NW cell was about 1/10th of the planar cell. The authors then concluded that this drop in efficiency was due to the presence of surface states that could not be fully passivated owing to the high-density of the nanowires which inhibits deposition of the a-Si beyond a few hundred nanometers from the surface of the array. They highlight therefore, the need to trade-off nanowire density with surface passivation in NW cells. However, they also concluded that the superior optical properties of nanowire cells were comparable to the planar cells.

Alivisatos and co-workers in 2002, utilized CdSe nanorods as the electronic conducting layer of a polymer-matrix solar cell. The hybrid structure used inorganic nanorods in an organic matrix resulting in efficiencies of the order of 1.7% for AM1.5 irradiation [52].

The nanowires act as a direct path for transport of charge to the anode without the presence of grain boundaries.

Nanowires and nanorods demonstrate great promise as building blocks for future solar cells devices. However, there are many technological challenges facing the research community such as highly conductive contacts, more efficient surface passivation and shunting approaches.

Towards the end of 2009, Cirlin et all [14], reported a conversion efficiency of 1.65% and the fill factor of 25% based on p-type GaAs NWs grown on the n-type GaAs substrate using the molecular beam epitaxy growth method and getting the best results under substrate temperature of 550^{o} C. One of the most important advantages of using the MBE growth is the ability to control the dimensions and the surface density precisely. One can also monitor the formation and time evolution of NWs in situ by the reflection high-energy electron diffraction (RHEED) technique. The obtained FF of 25% is rather low and further optimization and more research is needed in order to improve the efficiency. This may include the use of heterostructured scheme. One of the disadvantages of this growth method is the high cost of fabrication at high temperature.

2 New Silicon Texturing Process Using the Gas-Lift Effect (GLE)

A new cost-effective and efficient approach is proposed for texturing the crystalline silicon using the gas lift effect (GLE). The advantages of this approach over the conventional ones are that significantly lower amounts of IPA is used and much shorter etching time is required to achieve the same reflectivity. GLE is generated by taking advantage of the hydrogen bubbles evolved between the silicon wafer being etched and a glass plate, placed in parallel, creating a gap of 1-2 mm. This effect then acts as a pumping mechanism detaching more bubbles from the silicon surface, accelerating them to the top and out of the system, as quickly as they are generated. Experiments were carried out with various combinations of TMAH/IPA concentrations for two different GLE conditions to analyze and determine their influence on etching time, etching rate, surface morphology and reflectivity of the textured silicon surface. The use of this new approach in surface texturing, allowed the reduction of the required IPA by 50% and etching time by more than 60% to achieve the same reflectivity. This can ultimately lead to a significant reduction in cost by increasing the efficiency of the texturing process. A combination of 3.5% IPA and 2 mm GLE resulted in a textured silicon surface having a low specular Solar Weighted Reflectivity (SWR) of 0.15%.

2.2 Introduction / Background Information

In the solar cell industry, the surface of the silicon is textured to decrease the reflectivity. One of the most effective and least costly techniques for silicon texturing is the anisotropic wet etching of silicon surface using strong bases such as KOH and TMAH

[17]. In order to obtain uniform surface texturing using these etchants, one must improve the wettability of the surface and facilitate the removal of the generated hydrogen bubbles from the surface. By increasing the uniformity and coverage of the textured silicon surface, more photons are absorbed resulting in the decrease of the reflectivity. In order to achieve this, the conventional approach is to use a surface active agent such as IPA that would increase the wettability and facilitate the release of hydrogen bubbles from the silicon surface [18] [10]. However, IPA is volatile in a heated etching bath. The boiling point of IPA is around 82° C. Therefore, at the etching temperature of 90° C, it must be constantly added to the solution during the etching process resulting in difficult control and higher consumption of IPA. Also, with higher IPA concentrations, the etching rate starts to decrease drastically [20] [21]. In some experiments the IPA was eliminated all together from the etching solution and replaced by dissolved silicon or various iononic surfactants to achieve texture uniformity [22] [23]. Other approaches include the use of other additives such as Tertiary Butyl Alcohol (TBA) [24] [25] or using a metal grid to trap the hydrogen bubbles as a more controlled way to achieve the same favourable outcome [26].

The root of the problem comes from the fact that the generated hydrogen bubbles, with typical diameter range of 2-3 mm, stick to the surface long enough to interrupt the chemical reaction between the alkaline solution and the silicon surface. This gas blanketing effect is a known occurring issue in the electrochemical reactors. Industrial electrolytic cells that produce gas at one or both electrode surfaces are usually designed to take advantage of this phenomenon to generate gas lift electrolyte circulation by creating a narrow gap between the two electrode surfaces [11]. Good electrolyte circulation provides transport of electro-active species to the electrode surface as well as taking bubbles away from the electrode surface. Internal gas lift circulation in a well-designed electrochemical cell is much more efficient than mechanically pumped circulation [12].

In this chapter, the effect of gas-lift circulation on the texturing process of silicon wafers has been studied. Experiments were carried out with different combinations of TMAH/IPA concentrations with two gap sizes between the two flat surfaces facing each other creating the Gas-Lift Effect (GLE) and a reference surface where no GLE exists. More experiments were carried out to determine the effect of etching time as well as etching rate with and without the presence of GLE. Detailed analysis of the surface reflectance and surface morphology was carried out to evaluate the influence of the studied parameters.

2.3 Experimental Procedure

N-type (100) orientation, single side polished, clean room processed and packaged silicon wafers with a thickness of 625+/-25 μm and a resistivity of 1-10 Ω-cm were purchased from Silicon Inc., and used for all experiments. All samples were cleaned using the RCA process before the experiments were carried out. Glass beaker filled with TMAH was used for etching the silicon samples. Teflon basket was used to hold the silicon samples inside the glass beaker. The beaker was placed in an oil bath to maintain temperature uniformity of the etchant solution at 90° C. This operating temperature is below the boiling point of all the etchant solutions used containing various amount of IPA and TMAH. However, precautions were taken to assure that the concentration of all volatile components in the solution remain constant for the duration of etching. Therefore, all experiments were carried out in a closed system consisting of a beaker with a flux cap cooled through an internal circulation of 5-6º C running water resulting in the condensation and return of any evaporated component back to the solution. The TMAH 25 wt.% was purchased from Sachem Inc. and diluted with DI water to reach the desired 1, 2 and 3 wt.% concentrations used in the experiments. 99% IPA was purchased from VWR International and was added to the etching solution to obtain weight concentrations ranging between 0 to 9%. Figure 2-1 shows a schematic view of the apparatus used for the anisotropic etching of silicon.

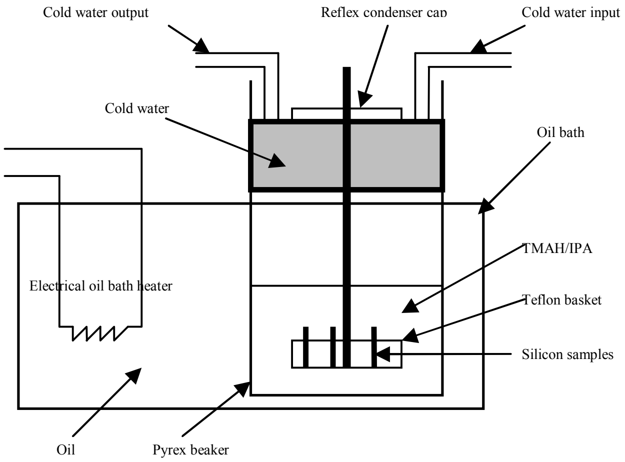


Figure 2-1 : Schematic view of TMAH etching apparatus

For each experiment, three Silicon wafer samples were prepared with equal dimensions of 25(width) x 50(length) x 0.625(thickness) mm. Figure 2-2 illustrates how a piece of glass with the same length and width was used to achieve the GLE in two of the three samples with 1 mm and 2 mm gaps between the glass and the silicon wafers.

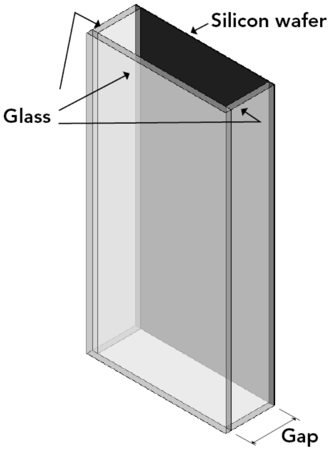


Figure 2-2: Schematic illustration of GLE samples used in each experiment.

Specular reflectivity of the samples was measured using a Varian Cary 5000 spectrophotometer with a baseline correction. The measured reflectivity was converted and presented here as specular Solar-Weighted Reflectance (SWR). We define the solar-weighted average reflectance as the integration of the product of the reflectance and the AM1.5 photon density, divided by the total number of photons between 300 nm and 1100 nm. Etching rates were determined by weighing the samples before and after each experiment. The morphology of the textured surfaces was examined by a Hitachi S-4700 field emission scanning electron microscopy (FE-SEM). The pyramid size distribution, surface coverage and uniformity measurements were obtained by performing image analysis of the SEM photos using the ImageJ image processing program developed by the US National Institute of Health.

2.4 Results and Discussion

Anisotropic etching of silicon was performed using different TMAH (1, 2, and 3 wt.%) and IPA (0, 1 and 9%) concentrations with two GLE configurations (1 and 2 mm gap sizes). The etchant temperature was kept constant at 90° C for the duration of all experiments. The GLE pumping provided agitation to help with the hydrogen bubble detachment from the surface of the silicon and to improve mass transfer of the active species to the silicon surface. The results were compared with the case where no GLE was present. The existence of GLE forced the generated hydrogen bubble to detach from the surface and leave the system as quickly as they are generated. The results in terms of surface reflectivity for three cases of no GLE, 1 mm and 2 mm gap for the previously mentioned TMAH and IPA concentrations and 30 minutes etching time are summarized in table 2-1.

Table 2-1: The Effect of Various IPA and TMAH Concentrations on the Reflectivity with and without the Presence of GLE

	SWR (%)								
	No GLE			1 mm GLE			2 mm GLE		
	TMAH (%)			TMAH (%)			TMAH (%)		
IPA (%)	**1**	**2**	**3**	**1**	**2**	**3**	**1**	**2**	**3**
0	1.92	1.44	12.00	2.59	1.31	15.32	0.72	0.45	5.90
1	0.81	0.62	7.61	0.96	0.45	11.39	0.44	0.39	1.94
9	0.42	0.19	0.23	0.40	0.15	0.22	0.36	0.18	0.22

2.4.1 No GLE present

In order to distinguish and quantify more accurately the effect of gas lift on the texturing process, expressed or measured in terms of surface reflectivity, it was decided to first study the texturing process without the presence of GLE.

As it may be observed from table 2-1, as the concentration of IPA increases, a surface with a lower reflectivity is obtained for all TMAH concentrations as expected and reported in the literature [18]. We can also observe that, regardless of IPA concentration, the optimal concentration of TMAH is around 2% as previously reported [18]. However, one interesting observation from table 1 is that, the effect of IPA in improving the reflectivity is much more significant at 3% TMAH.

It is reported in the literature that the lower texturization performance at higher concentration of TMAH may be attributed to the blocking effect of the TMA+ ions adsorbed on the surface of silicon [21]. This could also explain the higher effect of IPA at 3 % TMAH compared to 2 or 1%.

2.4.2 1mm gap GLE

The same set of experiments with varying concentration of TMAH and IPA was carried out using the experimental setup, as described in section 2.2, to create GLE. The results of the surface reflectance for the 1 mm gap GLE are presented in table 2-1.

Consistently at 9% IPA, the use of 1mm gap GLE improves the performance of texturing the surface resulting in better reflectivity regardless of TMAH concentration compared to the case where no GLE was used. At lower IPA concentrations (0% and 1%), GLE could not be sustained for the entire 30 minutes of etching time resulting in less consistent improvement in reflectivity. This could be related to the very small gap preventing the easy flow of the solution inside the gap between the Si surface and the glass not allowing the liquid to reach the expected velocity.

2.4.3 2mm gap GLE

The results of the 2 mm GLE are also presented in table 2-1. As predicted, the increase in the gap size allowed the sustainment of the GLE throughout the 30 minutes of etching time resulting in a consistent improvement of texturing for all IPA concentrations. In fact, in the presence of 2 mm GLE, the need for the use of IPA as a surface active agent to help minimize the surface reflectivity becomes much less critical. This is also evident from the data presented in figure 2-3.

This figure illustrates that, the use of GLE at 0%IPA, results in 80% reduction of reflectivity compared to where there is no GLE present.

Figure 2-3 also illustrates that, compared with the case where there is no GLE, the 2 mm GLE can result in significant gains in texturing performance at low or even 0% IPA.

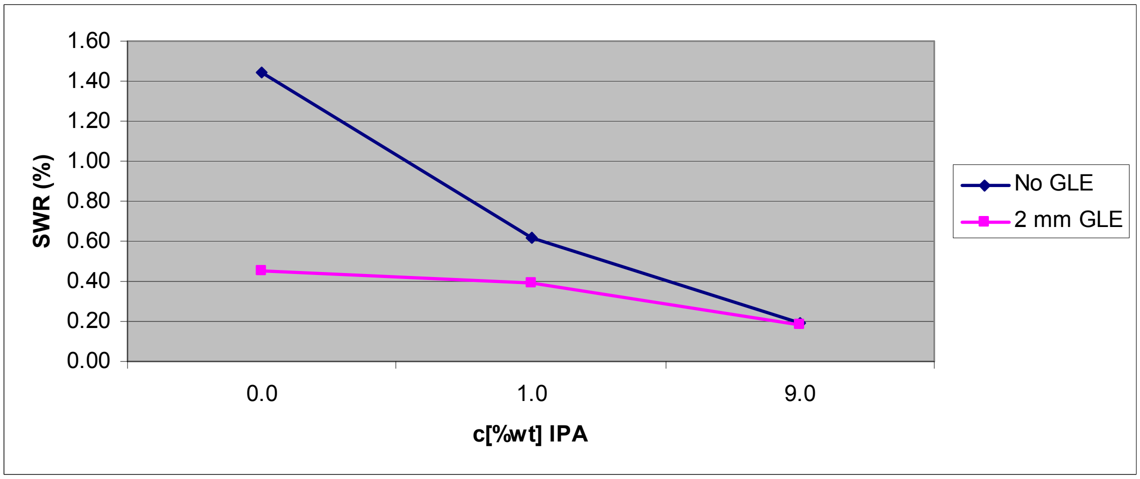


Figure 2-3: The use of IPA as a surface active agent becomes much less critical at the presence of the 2 mm GLE.

2.4.4 Effect of GLE on etching time

Another beneficial effect of GLE is the reduction of the etching time. In this set of experiment, the TMAH and IPA concentrations were set at 2% and 9%, respectively. The temperature was kept at 90º C and the etching times were chosen to be 5, 10, 20 and 30 minutes.

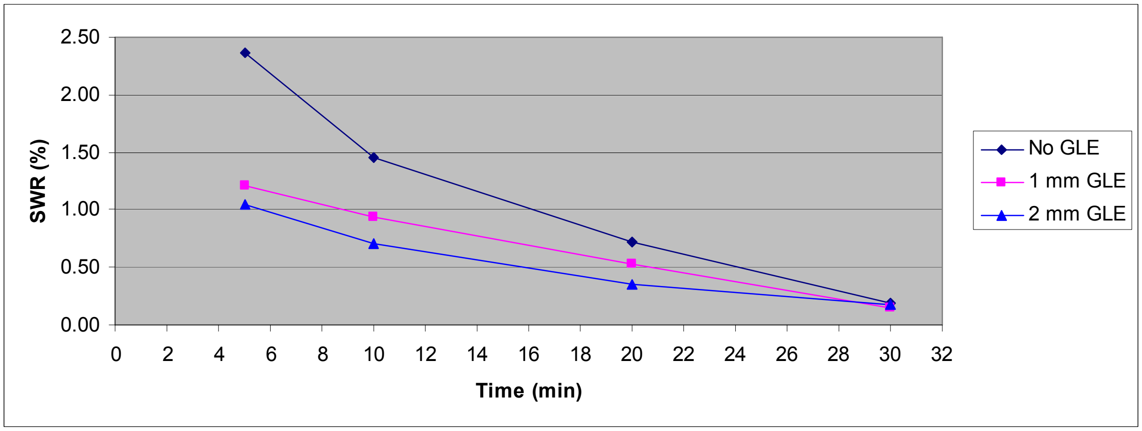


Figure 2-4: GLE and etching time correlation.

It can be observed from figure 2-4 that, at only 5 minutes into the etching time, the reflectivity of both samples with GLE are almost 1/2 of the one without the presence of GLE. With no GLE, around 15 minutes are needed to reach this level of reflectivity. This means that we can achieve the same reflectivity in almost 1/3 the time that is needed without applying GLE.

2.4.5 Optimal % IPA and GLE combination

We can see that the use of GLE would already allow us to obtain very low reflectivity without even using IPA as an active agent for texturing the silicon surface. However, it may also be observed that a combined use of both parameters, IPA and GLE, will result in obtaining even better performance than employing each of these parameters alone.

Although the presence of the IPA is less critical to obtain low reflectance surfaces when GLE is used, it still may be seen that a combination of IPA and GLE results in the optimal outcome.

A performance study was done to determine the optimal IPA concentration in the presence of GLE at 2% TMAH. The 2% TMAH concentration had been found to be the optimal concentration in most of the experiments conducted previously and also supported by the literature [18].

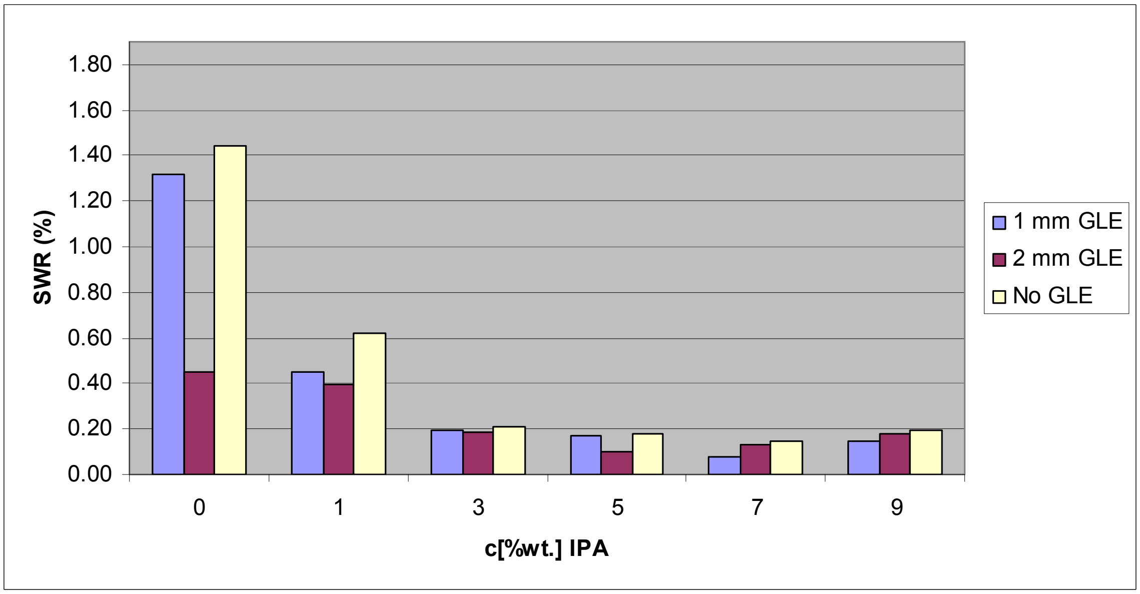


Figure 2-5: Optimal c[%wt.] IPA and GLE Combination.

In our experiments, the lowest reflectivity with no GLE present was found to be at 7% IPA as illustrated in figure 2-5. The goal is to predict a possible optimal combination of IPA concentration and GLE that can achieve the same or better reflectivity as the 7% IPA with no GLE. This combination must also allow the use of the lowest possible amount of IPA concentration leading to the reduction of the texturing cost. An experiment was conducted to confirm this prediction with the following parameter values: 2% TMAH, 30 min, 90° C, 3.5% IPA. The experiment was conducted in the presence of 2-mm gap GLE. The reflectivity of the textured silicon obtained under this condition is compared with others in figure 2-6. The obtained data confirmed our prediction that a combination of 3.5% IPA concentration and the presence of 2-mm gap GLE results in the same reflectivity as the optimal reflectivity with no GLE obtained at 7% IPA.

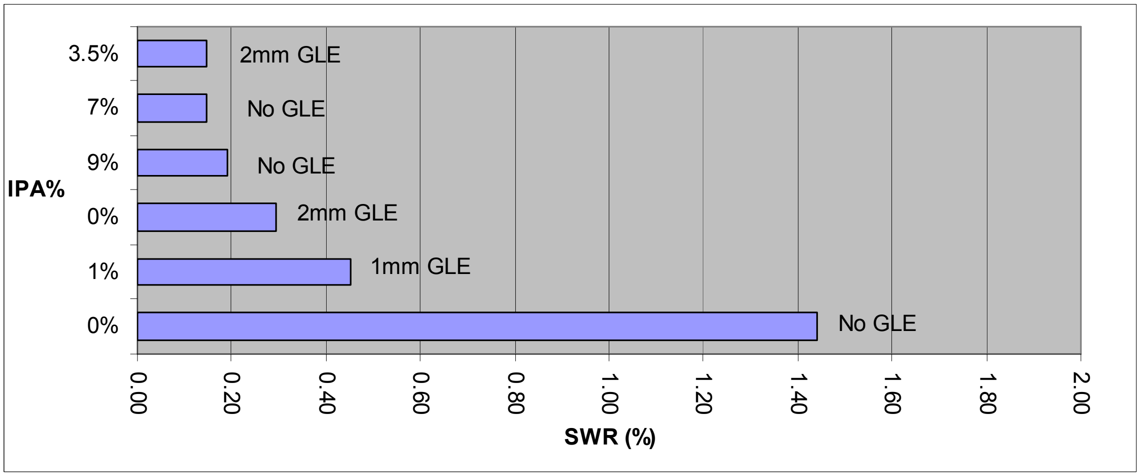


Figure 2-6: Optimal GLE-IPA% combination resulting in 3.86% SWR.

2.4.6 Correlation between reflectivity and etching rate

Figure 2-7 presents the behaviour of both reflectivity and the Etching Rate as the %IPA increases with no GLE present.

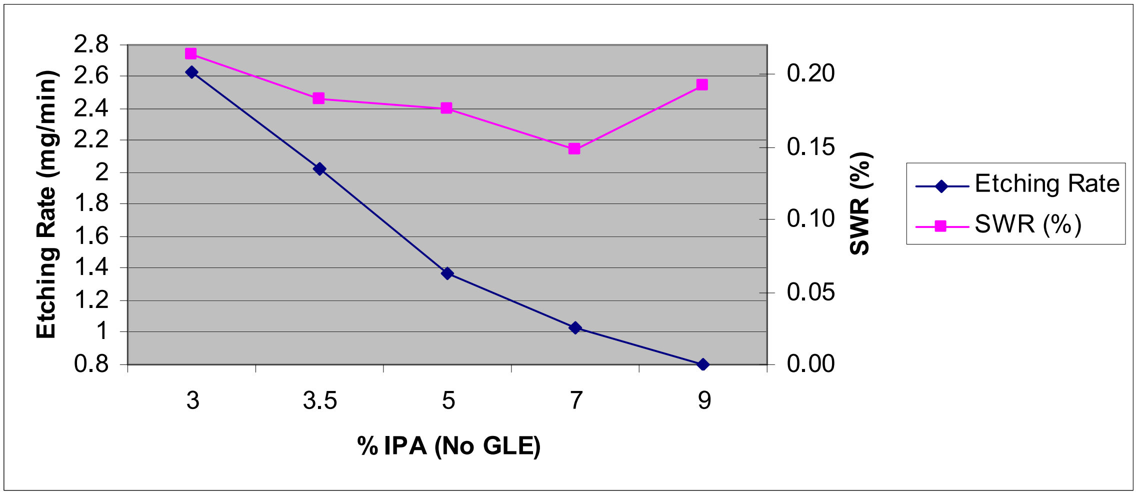


Figure 2-7: The behaviour of reflectivity and etching rate versus increasing %IPA with no GLE present.

As expected, up to a certain point, both reflectivity and etching rate decrease as %IPA increases. However, at around 7% IPA, as the etching rate continues to drop, the reflectivity starts to increase. One possible explanation for this behaviour is that, beyond this optimal IPA concentration, the surface coverage will start to decrease resulting in higher reflectivity. This is also in agreement with our earlier conclusion that reflectivity is dependent on both uniformity and the surface coverage. We believe that, up to 7% IPA, the uniformity and surface coverage are both improving. However, after that point, while the etching rate is still dropping contributing to the uniformity, the increasing IPA concentration starts to have a blocking effect on the etchant to have good surface contact. For the case where there is 2-mm gap GLE, this optimal IPA concentration is shifted to a lower value (around 5%) as shown in figure 2-8. From this point on, the reflectivity starts to increase as the etching rate still continues to drop.

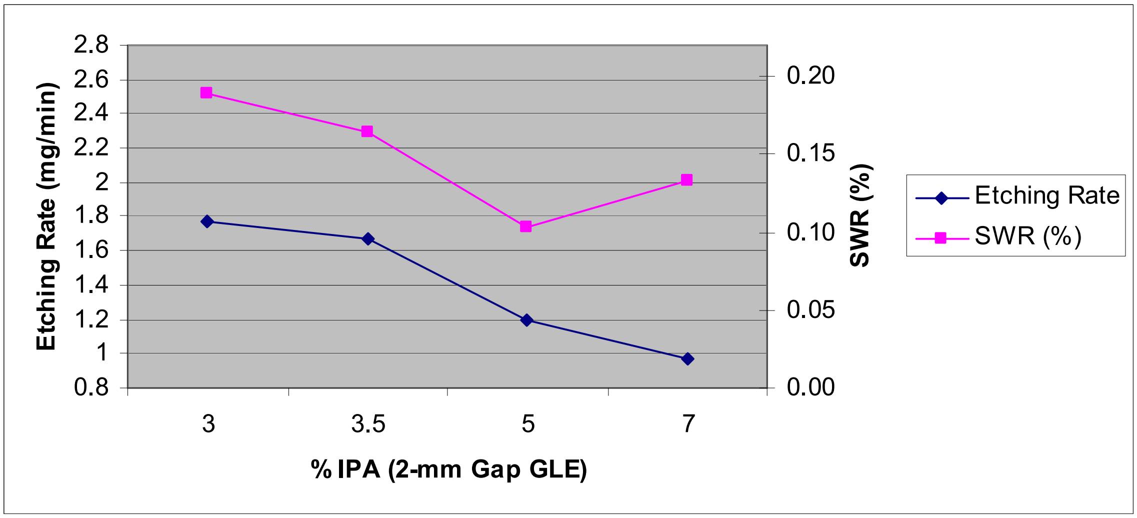


Figure 2-8: The behaviour of reflectivity and etching rate versus increasing %IPA with 2mm GLE present.

2.4.7 Correlation between reflectance and morphology

To evaluate any possible correlation between the measured reflectivity values of the samples and their morphology, an image analysis tool called ImageJ was used to calculate the surface coverage of pyramids and the standard deviation of the their sizes.

The samples listed in table 3 were all etched under the following parameter conditions: 2% TMAH, 30 min and 90º C. The three samples having practically within the same particle size range were selected to evaluate any possible correlation between surface reflectivity and coverage. Table 2-2 clearly shows that as the surface coverage decreases, the reflectivity increases as expected.

Table 2-2 : The correlation between reflectivity and surface coverage.

	2 mm GLE, 3.5% IPA	2 mm GLE, 0% IPA	No GLE, 0% IPA
SWR (%)	0.16	0.45	1.4
Surface Coverage (%)	93.4	92.5	72.3
Mean Particle Size (μ^2)	4	2.7	3

However, as conditions (a) and (b) in table 4 illustrate, the surface coverage is not the only parameter that influences the measured reflectivity. In fact, a significant difference in average particle size results in a considerable difference in surface reflectivity even for the same surface coverage. It may also be noted that the sample with the lower surface reflectivity presents a more uniform surface as it may be confirmed by the values of standard deviation of the particle size in table 2-3. This observation suggests that both surface coverage and particle uniformity influence the reflectivity of the surface. The above point can also be confirmed based on the conditions (c) and (d) in table 2-3. The data show that for slightly lower coverage, smaller particle size and smaller standard deviation result in a lower reflectivity.

Table 2-3: Influence of particle size and uniformity on reflectivity.

Experiment Condition	a*	b*	c*	d*
SWR (%)	0.15	0.45	0.19	0.45
Surface Coverage (%)	87.1	90.9	91.0	92.5
Standard Deviation (μ^2)	0.53	13.6	1.38	3.92
Mean Particle Size (μ^2)	0.52	13.21	0.52	2.7

** (a) No GLE, 7% IPA, (b) 1mm GLE, 1% IPA, (c) No GLE, 9% IPA, (d) 2mm GLE, 0% IPA*

Figures 2-9a and 2-9b illustrate the surface morphology of the two samples listed in table 2-3 as (c) and (d), respectively. As mentioned before, the coverage is slightly higher in the sample presented in figure 2-10b. However, a more uniformity and smaller particle size (figure 2-10a) have resulted in lower reflectivity. One should note that the two SEM pictures have different magnifications and do not have the same scale. The ImageJ tool takes the difference of scale into account when calculating and comparing the surface coverage and particle size uniformity.

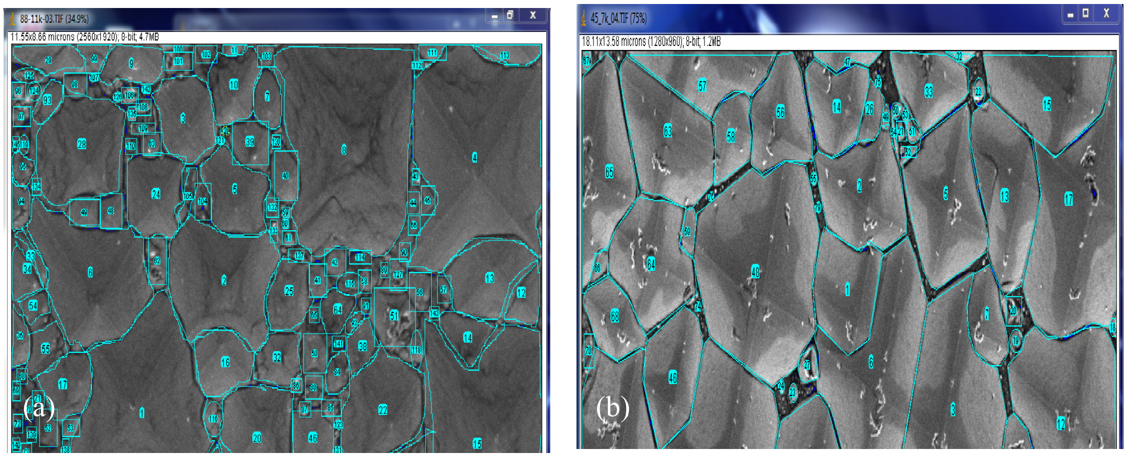


Figure 2-9: Surface image analysis of samples with (a) no GLE and 9% IPA and (b) 2 mm GLE and 0% IPA.

2.4.8 Effect of etching time on morphology

As it was shown earlier in section 3.4, with shorter etching time we can achieve the same reflectivity using GLE. This phenomenon can also be explained by looking at the morphology of the surface of the samples with and without the presence of GLE. The SEM photos in figure 2-10 are taken from samples under the following etching parameters condition: 1% IPA, 2% TMAH and 90º C temperature. This figure compares the surface coverage and uniformity of two samples at 10 minutes into the etching time, one with (figure 2-10a) and one without (figure 2-10b) the presence of GLE. One very clear observation is the surface damages shown in the figure 13b. We speculate that these damages are due to hydrogen bubbles sticking to the surface of silicon in the absence of GLE. Those damaged areas are not observed when GLE is present (figure 2-10a).

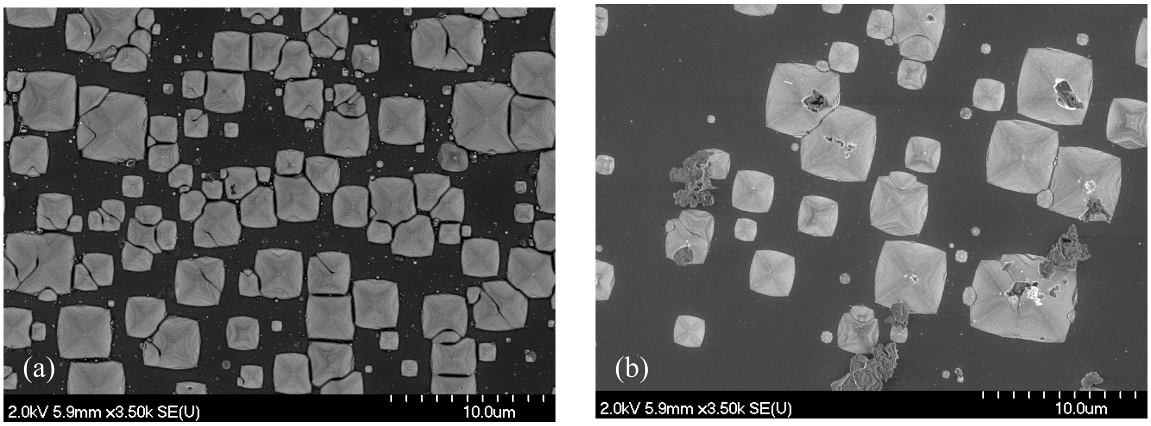


Figure 2-10: SEM photos of textured silicon at 10 minutes into the etching time with 1% IPA and 2% TMAH, (a) presence of 2 mm GLE (b) absence of GLE

The result of performing reflectivity measurements of both samples as well as image analysis of their SEM photos are summarized in table 2-4 in terms of reflectivity, standard deviation, surface coverage and the average particle size.

Table 2-4: Reflectivity, standard deviation, and surface coverage at 10 minutes etching time.

	SWR (%)	Surface Coverage (%)	StDev (μ^2)	Average Particle Size (μ^2)
2 mm GLE	13.9	51.4%	3.53	2.42
No GLE	29.7	28.2%	7.06	4.82

As it may be seen, the use of GLE resulted in a significantly lower reflectivity after 10 minutes into the experiment compared to the sample with no GLE. The analysis of the morphology confirms the previously mentioned observation that the sample with lower reflectivity presents also a higher surface coverage, a lower mean and higher uniformity of the particle size.

2.5 Conclusion

In this study, etching experiments were performed on n-type (100) silicon wafers with and without the presence of Gas Lift Effect (GLE). In the presence of GLE, the need for the use of a surface active agent, such as IPA, to help minimize the surface reflectance becomes much less critical. In fact, GLE can achieve the same reflectivity with 50% the amount of IPA, compared to the case where no GLE is present. It can also reduce the processing time by more than 60% to achieve the same reflectivity. Although the presence of IPA is less critical to obtain low reflectance surfaces when GLE is used, it was concluded that a combination of IPA and GLE achieved the lowest reflectivity. Accordingly, a specular solar-weighted reflectance (SWR) of 0.15% was achieved with a combination of 3.5 %IPA and 2mm GLE. The morphology of the surface was studied by performing image analysis of the SEM photos of the textured surface. The correlation between parameters such as surface coverage, uniformity and particle size with the reflectivity was studied and it was concluded that reflectivity is highly influenced by those parameters. A significant difference in average particle size results in a considerable change in surface reflectivity even at the same surface coverage. Lower reflectivity is a result of a combination of lower mean particle size as well as higher surface coverage and uniformity of the particles. The use of this new approach in surface texturing reduces the IPA and time required to reach the same reflectivity, and therefore, reducing the cost and increasing the efficiency of the texturing process.

3 Modeling and Optimization of the new Texturing System

Modeling and simulation techniques were used to understand the fluid flow patterns inside the silicon texturing system operating under gas-lift effect (GLE) for solar cell applications. Experiments were performed which confirmed the validity of the simulation model and the simulated results. It was determined that due to the original non-optimal inlet, the fluid flow pattern and the non-uniform fluid velocity distribution inside the system resulted in the generation of lower velocity regions on the surface of the textured silicon. The simulation tool validated the correlation of the lower fluid velocity with the reduced surface coverage, uniformity and subsequently less optimal surface reflectivity. Various inlet designs were modeled and evaluated for optimal performance. The best case inlet design was fabricated and tested resulting in the validation of the simulation work and significant improvement in the GLE texturing system performance. With the new inlet design, as the fluid velocity reaches and goes beyond some critical value (in this case 0.047 m/s) in areas that had shown lower velocity in the original inlet design (mainly close to the inlet and side walls), the observed morphology and surface reflectivity improve significantly with values very similar to those of the higher-velocity areas.

3.2 Introduction / Background Information

Lowering the reflectivity of the surface of silicon-based solar cells is an on-going challenge. The anisotropic etching technique is one of the most cost-effective ways for texturing the silicon surface to achieve low reflectivity. However, the hydrogen bubbles generated during the process, lead to the creation of the gas blanketing effect on the surface of the silicon preventing a uniform surface texturing. The traditional methods for removing the bubbles involve adding surface active agents (surfactants) such as Isopropyl alcohol (IPA) [10] to modify the liquid surface tension resulting in the quicker release of the hydrogen bubbles from the silicon surface. However, there are unwanted effects as a result of adding IPA such as less control over the etching rate and the average particle size.

In previous work, we reported a new approach for the removal of the bubbles requiring only half the IPA amount by taking advantage of the gas-lift effect (GLE) [53]. As hydrogen bubbles become large enough, they detach from the silicon surface and rise to the surface of the liquid. The rising velocity of the bubbles reaches a terminal value which is a function of the bubble diameter as well as the liquid viscosity as defined by the Stokes law. As a result of this rising, the bubbles push the liquid upwards, and at the same time, induce a vacuum underneath leading to more liquid suction into the system causing a pumping effect and a natural circulation that stays in effect as long as the bubbles are generated, detach and rise to the surface inside the enclosed GLE texturing system.

Due to a higher liquid velocity inside the GLE system, the hydrogen bubbles attached to the silicon surface are removed much quicker. As a result, the silicon surface is more exposed to the TMAH etching solution leading to higher textured surface area.

However, due to non-uniform velocity distribution inside the GLE system caused by the non-optimal geometry of the inlet, regions with non-uniform reflectivity are formed. We believe that a modification to the GLE structure will be instrumental to achieve uniform texturing of the silicon surface.

The study in this chapter focuses on the use of simulation tools for the optimization of the inlet design and the modification of the flow patterns during the silicon texturing based on the innovative GLE approach. Different inlet geometries were designed, modeled and studied. The best-case inlet design was fabricated and further experiments using the new inlet verified our simulation results confirming a significant reduction of lower velocity regions, and therefore, maximizing surface uniformity.

3.3 Modeling and experimental details

3.3.1 Modeling tool and assumptions

A 3D modeling of the GLE system was performed using COMSOL finite element analysis simulation software version 4.1. The following approximations were considered to simplify the modeling:

- The effect of micro agitation and turbulence created by the silicon surface mesh has been ignored.
- The silicon surface is assumed to be a polished flat surface parallel to the glass surface.
- The Gas-Lift effect due to the hydrogen bubble generation and rising has been modeled as a mechanical pump generating a flow out of the GLE system.

The flow of the liquid inside the GLE system, based on the generation of the hydrogen bubbles and their gas-lift effect, was assumed to be constant in all cases. Then a liquid velocity at the outlet for each case was assumed to be the same and not dependent on the inlet geometry.

3.3.1.1 GLE geometry and dimensions

Table 3-1 lists the geometric parameters and their values for the modeled non-optimal GLE system. Inlets with various geometries were designed and modeled to identify the one with most uniformly distributed resistance resulting in the uniform fluid velocity distribution inside the GLE system.

Table 3-1: Dimensions of the modeled non-optimal GLE system.

Parameter	**Value**	**Unit**
GLE active area width	25	mm
GLE active area height	50	mm
GLE gap	2	mm

3.3.1.2 Turbulent flow model

The flow was considered to be isothermal and in turbulent state. The standard k-ε (k-epsilon) is classified as eddy viscosity model and is the most widely used [54] [55]. This two-equation model includes two extra transport equations to represent the turbulent properties of the flow [56] [57] [58]. Transport equations are solved for two scalar properties of turbulence. The k-equation is a model of the transport equation for the turbulent kinetic energy. The ε-equation is the model for the dissipation rate of turbulent kinetic energy [59].

One of the two main references on this model is described by Launder and Sharma [60]. The Reynolds stresses are modeled as follows:

$\tau_{tij} = 2\mu_t\left(S_{ij} - S_{nn}\delta_{ij}/3\right) - 2\rho k\delta_{ij}/3$, where $\mu_t = c_\mu \rho k^2/\varepsilon$ is the eddy viscosity defined as a function of the turbulent kinetic energy (k) and the turbulent dissipation (ε),

$$S_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\right)$$

is the mean-velocity strain-rate tensor, ρ is the fluid density, k is the turbulent kinetic energy, and δ_{ij} is the Kronenecker delta.

Table 2 contains the turbulence transport equations for the k-ε Launder-Sharma model.

Table 3-2 : Equations used in the modeling of the system by COMSOL.

Equation	**Description**
$\frac{\partial \rho k}{\partial t} + \frac{\partial}{\partial x_j}\left(\rho u_j \frac{\partial k}{\partial x_j} - \left(\mu + \frac{\mu_\tau}{\sigma_k}\right)\frac{\partial k}{\partial x_j}\right) = \tau_{tij}S_{ij} - \rho\varepsilon$	Turbulence energy transport
$\frac{\partial \rho \varepsilon}{\partial t} + \frac{\partial}{\partial x_j}\left(\rho u_j \varepsilon - \left(\mu + \frac{\mu_\tau}{\sigma_\varepsilon}\right)\frac{\partial \varepsilon}{\partial x_j}\right) = c_{\varepsilon 1}\frac{\varepsilon}{k}\tau_{tij}S_{ij} - c_{\varepsilon 2}\rho\frac{\varepsilon^2}{k}$	Energy dissipation transport

The model constants are defined as follows:

$c_\mu = 0.09$, $c_{\varepsilon 1} = 1.45$, $c_2 = 1.92$, $\sigma_k = 1.0$, $\sigma_\varepsilon = 1.3$

Using the turbulence variables, k and ε, it is possible to account for history effect such as convection and diffusion of turbulent energy. Boundary conditions at surfaces (walls) was assumed to be no-slip and were set to k = 0 and ε = 0. Zero-gradient conditions are applied at symmetry boundaries. Inlet boundary condition was set to zero pressure with no viscous stress, and for the outlet, the normal outflow velocity was assumed.

3.3.2 Experimental measurement of the modeling parameters

The fluid viscosity was measured using a Paar Phisica MCR 500 Rheometer. The density of the liquid was measured using a Micromeritics Accupyc II 1340 Pycnometer. The average velocity in the GLE system was calculated by measuring the time it took a red dye to travel the entire length of the GLE system (50 mm). A digital video camera and a digital counter were used to record the entering and exiting times of the red dye into and out of the GLE system. The experiments were repeated 10 times and an average value was obtained to minimize the error. The average velocity was used to calculate the flow rate into the GLE system.

The flow rate at the inlet was calculated by multiplying the inlet area by the measured average fluid velocity inside the system. For an empirically measured average velocity of 0.05 m/s and an inlet cross section area of 0.00005 m^2 the flow at the inlet was calculated to be 0.0025 l/s.

3.3.2.1 Silicon Texturing Experimental Setup

P-type (100) orientation silicon wafers with a thickness of 625+/-25 μm and a resistivity of 10-20 Ω-cm were purchased from Silicon Inc. TMAH 25 Wt. % was purchased from Sachem Inc. and diluted with DI water to reach the desired 2 wt.% concentrations used in the experiments. 99% IPA was purchased from VWR International and was added to the etching solution to obtain weight concentrations of 3.5%. The experimental setup for texturing using the GLE approach as well as the characterization and analysis tools are exactly the same used in our previous work [53]. The specular reflectivity was measured for all samples in our experiments and then converted to specular solar weighted average by integrating the product of the reflectance and the AM1.5 photon density, divided by the total number of photons between 300 nm and 800 nm.

3.4 Results and Discussions

3.4.1 Effect of inlet geometry on flow pattern during the silicon texturing

The accumulation of hydrogen bubbles during the silicon texturing process results in a non-optimal textured surface leading to a non-desirable higher reflectivity values [18] [10]. The conventional approach has been the use of significant amounts of IPA or other surfactants to facilitate the removal of hydrogen bubbles to obtain a textured surface with lowered reflectivity.

In our previous paper [53], we reported the efficacy of the GLE effect on the removal of the hydrogen bubbles which allows obtaining the same desired lower level of reflectivity by using significantly less amounts of IPA. However, due to non-uniform flow pattern inside the used GLE system, regions with lower fluid velocity are formed inside the GLE system resulting in a different reflectivity values for those regions compared to the rest of the textured surface.

Figure 3-1 illustrates the presence of these regions mostly at the inlet and closer to both sidewalls of the system (areas surrounded by the dotted lines). The texturing parameters used for this sample were the same as the ones resulting in the best reflectivity case reported in our previous work [53]. Accordingly, the values of the temperature, GLE gap size as well as the concentrations of TMAH and IPA were, 90 °C, 2mm, 2% and 3.5%, respectively.

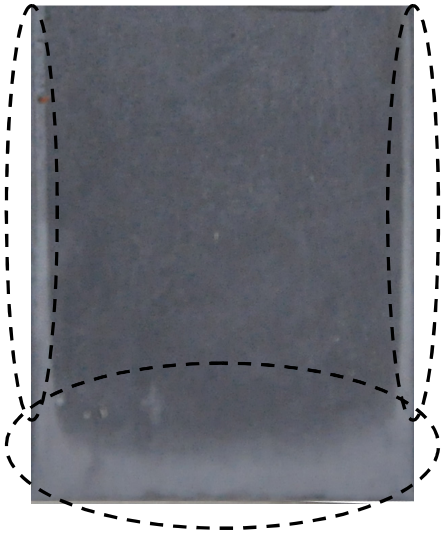


Figure 3-1: Low velocity areas formed by the GLE system.

The morphology and the reflectivity of these lower-velocity areas were compared to those of the rest of the surface using SEM analysis and photo-spectrometry measurements. Figure 3-2 illustrates the morphology of the textured surface of the silicon using the GLE system. As it maybe seen, the areas with higher velocity (figure 3-2a) show significantly higher textured surface coverage compared to the lower-velocity areas (figure 3-2b). Accordingly, the textured surface coverage values determined by SEM image analysis (expressed as the percentage of the surface covered by the formed pyramids with respect to the total surface area) were about 99% and 68% for higher and lower velocity areas, respectively. It may also be noted that the higher fluid velocity results in a more uniform pyramids size distribution.

The specular reflectance spectra of these two distinct areas presented in figure 3-3, also confirm the lower reflectivity of the higher-velocity regions over the entire spectrum (400 to 800 nm).

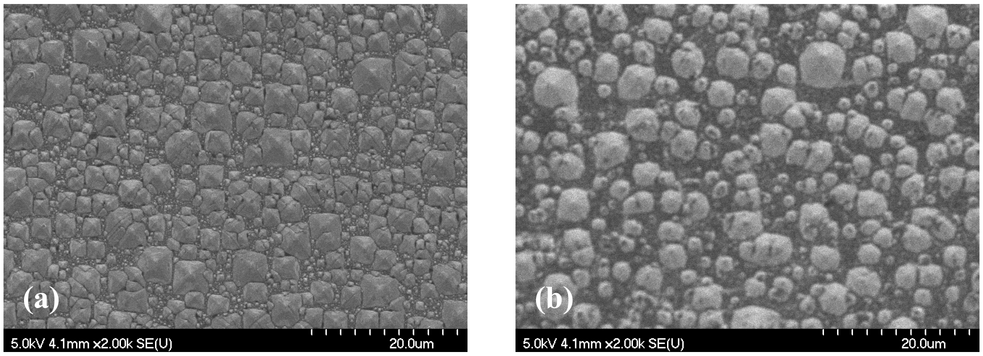


Figure 3-2: Surface of textured silicon in the (a) higher-velocity and (b) lower-velocity areas.

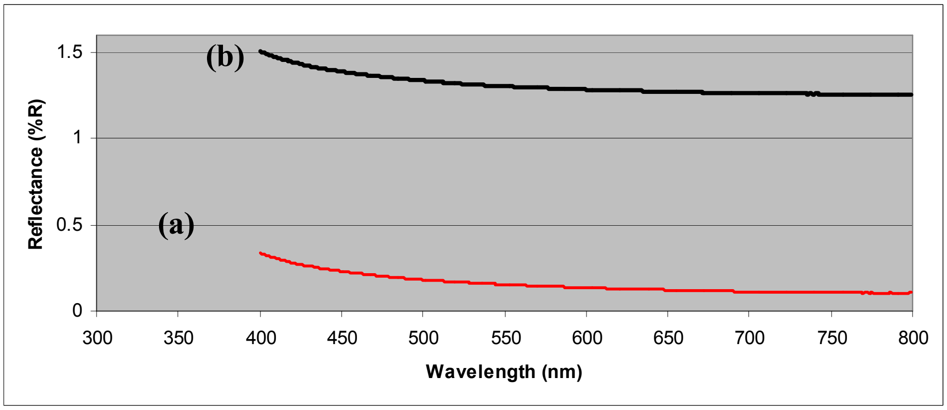


Figure 3-3: The reflectivity of the (a)higher-velocity areas vs (b)lower-velocity areas.

The areas affected by the fluid lower velocity (and consequently, higher reflectivity) represent about 15% of the overall surface, and it is important from an economical point of view, to minimize their surface if the GLE approach is to be used as a viable alternative to the conventional texturing techniques at an industrial scale.

As it was assumed that the formation of these lower-velocity areas was related to the geometry of the GLE system inlet, it was decided to use a simulation tool to model and validate this assumption as well as to improve the design of the inlet.

3.4.2 Modeling of the flow patterns

3.4.2.1 Velocity distribution of non-optimal inlet design

COMSOL software application was used as the simulation tool to obtain a model that can closely represent the formation of the distinctive textured areas observed experimentally in the GLE system using the initial non-optimal inlet design. Table 3-2 summarizes the parameters and their values used for the modeling. The fluid density, viscosity and flow rate were measured under the same experimental conditions as those used for the texturing of the silicon surface sample presented in figure 3-1.

Table 3-3: Parameters and their values used for the modeling.

Name	**Value**	**Description**
ρ	1043 [kg/m^3]	Fluid density
μ	0.6e-3 [N*s/m^2]	Fluid viscosity
Flow Rate	0.0025 [l/s]	Electrolyte flux at the inlet
V_{out}	0.05 [m/s]	Average liquid velocity
G	9.81 [m/s^2]	Gravitational constant

Figure 3-4 illustrates the liquid velocity pattern inside the modelled GLE system.

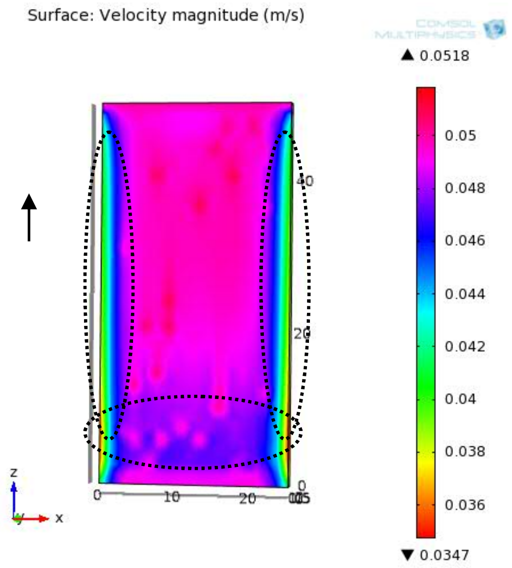


Figure 3-4 : The velocity pattern inside the GLE system.

The surface areas designated by the dotted ovals identify the lower fluid velocity areas. As it may be noted, the model predicts the formation of lower velocity regions close to the inlet and the side walls as observed experimentally (see figure 3-1). The predicted velocity profile across the GLE system width (x direction) for several heights (z direction) on the silicon surface (y=0) are illustrated in figure 3-5. As it maybe seen, lower velocity regions represent up to 25% of the entire width of the GLE system and, in areas close to the sidewalls, the reduction in velocity can reach up to 30% compared to the high velocity regions. The model also predicts lower velocities in areas close to the inlet as it maybe noted from the velocity profile at 4mm height, as also observed in the experimental sample. In addition, the model shows some fluctuations in the velocity value along the width of the GLE system regardless of the height.

Figure 3-5 : Velocity magnitude (m/s) distribution in the GLE system at different heights.

3.4.2.2 Optimization of the GLE inlet design

It was decided to use a design that would result in a higher pressure at the inlet leading to a more uniform fluid flow rate and a better velocity distribution profile. Accordingly, two sets of inlet geometry configurations were designed and tested with the simulation tool to evaluate their influence on the flow pattern and any improvements on the lower-velocity regions. One consisted of an inlet with a slit gap, varying between 0.2 and 1.8 mm (increments of 0.1 mm), all along the width of the GLE system. The other, was an array of small size holes (0.5 mm in diameter) with a number of holes varying between 5 and 15 along the width of the inlet. The best case result was found to be the inlet design with a slit of 1.2 mm gap as illustrated in figure 3-6.

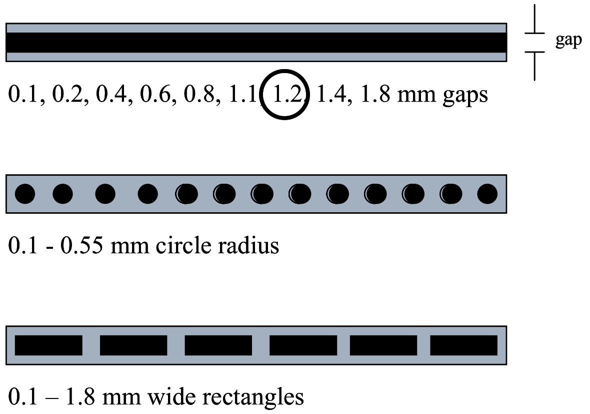


Figure 3-6: Designed and tested inlets using the simulation tool.

Figure 3-7 illustrates the velocity distribution of the electrolyte inside the GLE system with such inlet design. The most noticeable result is the improvements in velocity in the two regions close to the side walls. However, the velocity improvements at the lower heights (closer to the inlet) are less significant and still some velocity fluctuations remain at these lower heights (4 mm height). It was assumed that this effect may be attributed to the edge effect related to sharp corners of the rectangular slit. As a result, an improved version of the same slit was designed and tested with rounded corners.

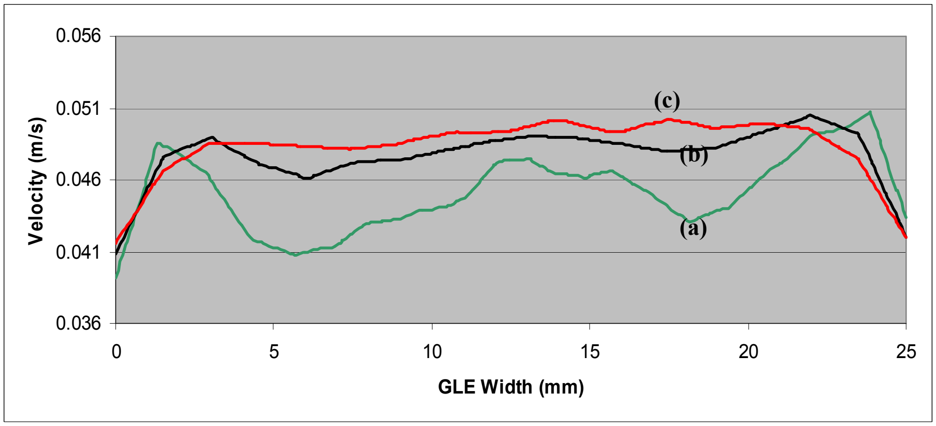


Figure 3-7: Velocity magnitude (m/s) distribution in the GLE system with 1.2 mm slit inlet design at (a) 4 mm, (b) 20 mm, and (c) 40 mm height.

It was assumed that this effect may be attributed to the edge effect related to sharp corners of the rectangular slit. As a result, an improved version of the same slit was designed and tested with rounded corners with a radius of 0.55 mm as illustrated by figure 3-8.

Figure 3-8: The best case inlet design with a 1.2 mm gap and rounded corners of 0.55 mm radius.

The velocity distribution in the GLE system inlet design with the 1.2 mm gap and rounded corners is represented in figure 3-9. It maybe noticed that the latest inlet design addresses the three main issues that had been targeted to be resolved in the non-optimal design. First, the liquid velocities in the two extremities near the side walls have improved significantly. Secondly, the velocity at the very bottom of the GLE system height has also improved significantly. Finally, there are less liquid velocity fluctuations at all heights of the GLE system (4 mm, 20 mm and 40 mm).

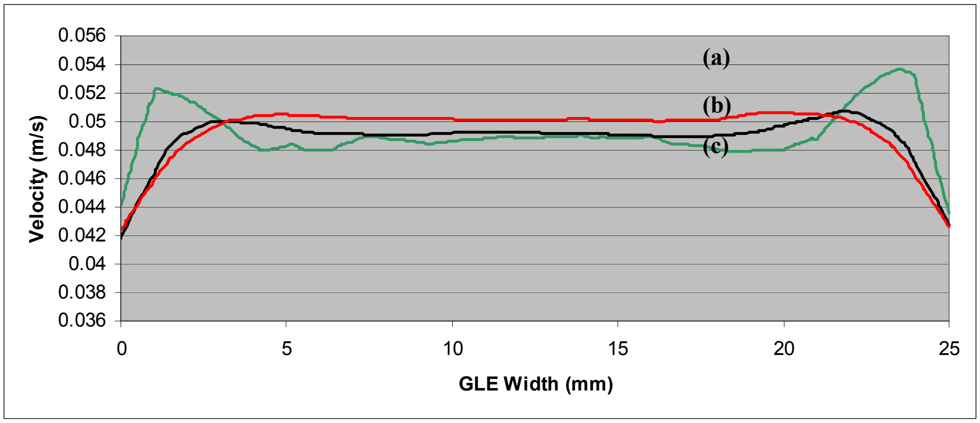


Figure 3-9: Velocity magnitude (m/s) distribution in the GLE system with a 1.2 mm gap slit inlet with rounded corners at (a) 4 mm, (b) 20 mm, and (c) 40 mm height.

The improvements of the flow pattern of the new design can better be appreciated by comparing its velocity profile at low heights with that of the non-improved design as presented in figure 3-10. In fact, as it may be seen, while more than 45% of the width of the GLE system are at velocities below 0.047 m/s in the case of the non-optimal inlet, less than 4% of the total width falls below this velocity for the improved inlet design.

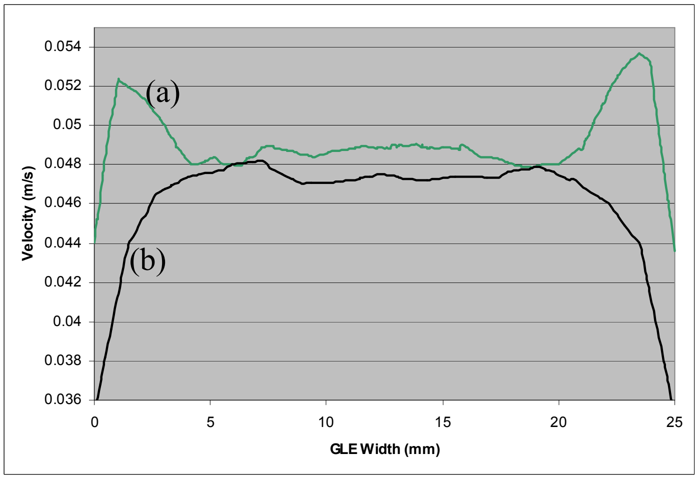


Figure 3-10: The velocity distribution at 4 mm height for the (a) 1.2 mm inlet with round corners versus the (b) 2 mm wide original non-optimal inlet.

3.4.3 Experimental results based on the new inlet design

A new GLE system was fabricated based on the improved 1.2 mm-gap inlet with rounded corners and used to perform silicon surface texturing under the same experimental conditions. Figure 3-11 illustrates the efficacy of the new inlet design in improving the uniformity of the textured sample silicon surface by significantly reducing the low velocity regions.

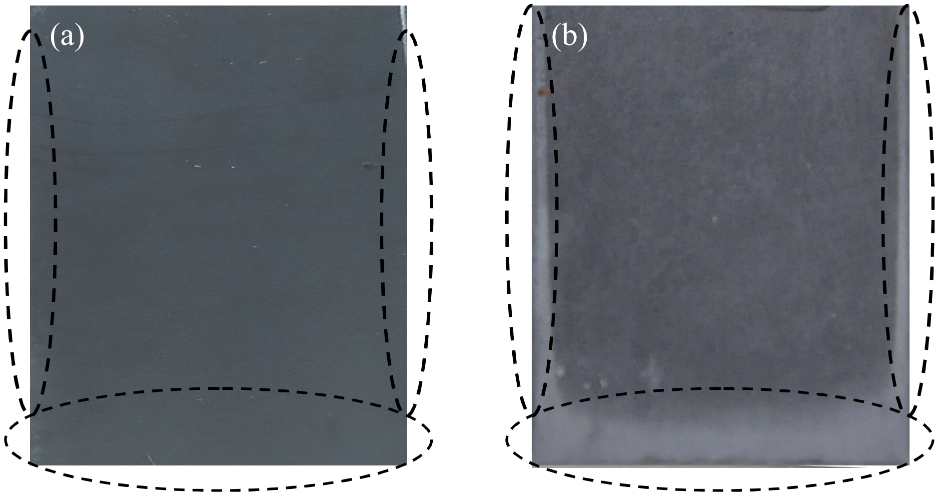


Figure 3-11: Silicon surfaced textured (a) with the optimized GLE system and (b) without.

When the two samples are visually compared, the lower-velocity areas close to the inlet and the side walls of the sample with the optimized inlet have practically disappeared, suggesting the improved velocity flow pattern as a consequence of the improved inlet design. This is also confirmed when the difference in morphology and the reflectance are examined for both inlet designs using SEM and photo spectroscopy respectively. As it may be seen in figure 3-12, the regions close to the side walls and the inlet, present a morphology similar to the higher-velocity areas in the case of the improved inlet design. In fact the value of the surface coverage is practically the same (more than 99%) compared to the non-optimal design (about 68%).

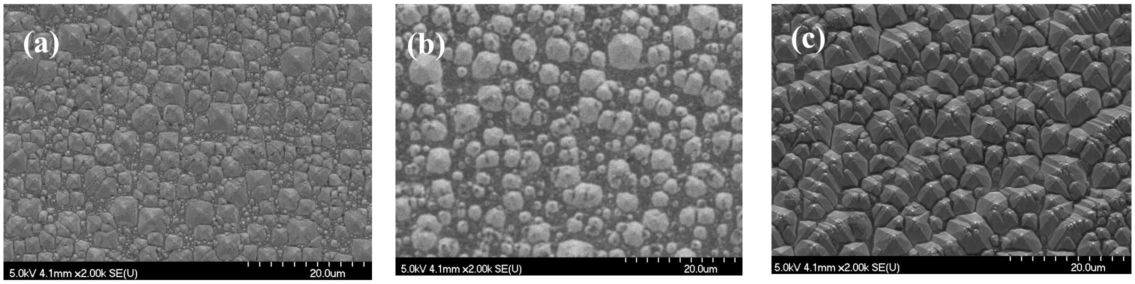


Figure 3-12: The SEM image of the (a) higher-velocity region of the non-optimized, (b) lower-velocity region of the non-optimized and (c) lower-velocity region of the optimized inlet**.**

The efficacy of the new design in improving the reflectance of the lower-velocity regions is illustrated in figure 3-13. As it may be noted, these regions present practically the same low reflectivity as the one observed in the higher-velocity areas (curves (a) and (c)).

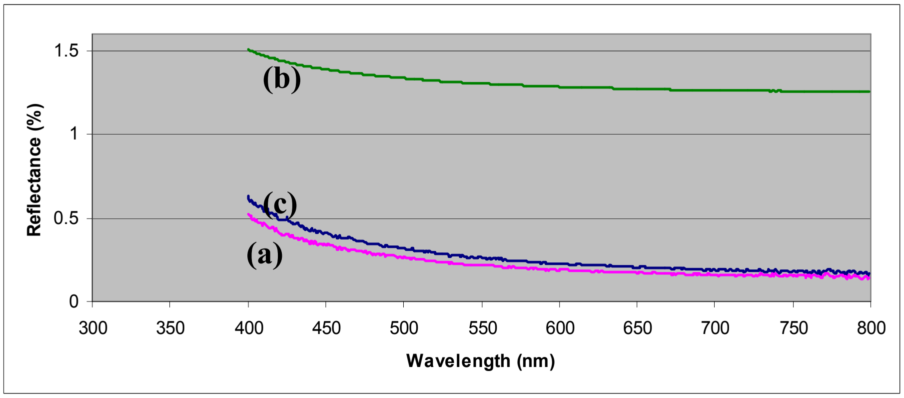


Figure 3-13: The reflectivity spectrum of (a) higher-velocity region of the non-optimized, (b) lower-velocity region of the non-optimized and (c) lower-velocity region of the optimized inlet.

3.5 Conclusion

In this study, COMSOL tool was used to model and simulate the fluid flow patterns inside the GLE silicon texturing system. This allowed a better understanding of the influence of the fluid velocity on the texturing performance and the subsequent characteristics of the textured silicon in terms of morphology and surface reflectivity. The fluid velocity profiles obtained from the simulation tool suggested a good correlation between the location of high-reflectivity (and low surface coverage) areas with that of low fluid velocity regions. These regions are mostly located at the heights close to the inlet and at widths closer to the side walls as observed both experimentally as well as in the case of the simulation.

Based on the fluid velocity distribution predicted by the model and the obtained experimental results in terms of surface coverage and reflectance, it was concluded that the best performance of surface texturing requires some critical fluid velocity that seems to be beyond 0.047 m/s.

Various simulations were performed using different inlet geometry designs and the best case was found to be a slit of 1.2 mm gap all along the entire width of the inlet with rounded corners.

As a result of this new and improved inlet design, the low-velocity regions were drastically reduced resulting in a much more uniform reflectivity on the surface. In fact, with the new inlet design, the areas close to the inlet and the side walls (lower-velocity areas observed in the original inlet design) show morphology and surface reflectivity values very similar to those of the higher-velocity areas as the fluid velocity reaches and goes beyond the critical 0.047 m/s value.

Since the lower-velocity areas represented more than 15% of the total textured area in the case of the non optimal inlet design, the reduction and even elimination of these regions will be more critical in the scaled up process if the GLE approach is to be used as a viable alternative to the conventional texturing techniques at an industrial scale.

4 Improving the efficiency of silicon solar cells using the novel gas-lift effect texturing approach

Texturing the surface of the silicon-based solar cells significantly increases the light absorption contributing to their overall efficiency. Wet anisotropic etching technique utilizing the novel gas-lift effect (GLE) approach is an effective and low-cost approach for texturing commercial silicon solar cells. Two solar cell devices, one based on the novel GLE texturing approach, and the other based on the conventional method, were designed, fabricated and characterized. A significant improvement (more than 100%) was observed in the efficiency of the solar cell based on the GLE texturing approach. This improvement may be contributed to the significant impact of utilizing the GLE approach on increasing the real surface area (resulting in higher electron-hole pair generation) and increased light absorption (decreased reflectivity). The application of the new GLE texturing approach results in considerable improvements in overall power efficiency of silicon solar cells without any additional increase to the production cost.

4.1 Introduction

Lowering the reflectivity of the surface of silicon solar cells can contribute significantly to their overall efficiency. The main approach to lower the reflectivity of silicon-based solar cells is by texturing the silicon surface. The wet anisotropic etching of silicon is the most widely used method to texture silicon surface for improved reflectivity. The accumulation of hydrogen bubbles during the silicon texturing process results in a non-optimal textured surface leading to a non-desirable higher reflectivity values [18]. This method relies on the used of surfactants such as Isopropyl Alcohol (IPA) to improve the wet-ability of the surface as well as facilitating the removal of hydrogen bubbles created during the texturing process [10].

In our previous work, we proposed a cost-effective and efficient approach for texturing the crystalline silicon using the gas-lift effect (GLE) [53]. This effect is generated by carrying out the reaction in a small gap in which the rising hydrogen bubbles create a pumping mechanism resulting in an increased fluid velocity and therefore, detaching more hydrogen bubbles from the silicon surface. This novel approach presents two advantages over the conventional ones. First, significantly lower reflective silicon surface is achieved using the same amount of IPA. Secondly, much shorter etching time is required to achieve the same reflectivity. In our previous studies, the effect of different operating conditions and geometries of various GLE systems were investigated and optimized using both simulation and experimental tourniquets [53] [61].

In this chapter, we report on the use of the optimized GLE texturing system for the fabrication of the solar cell device and its overall efficiency comparison with a device fabricated under the very same conditions but in the absence of GLE.

4.2 *Experimental Details*

Two samples of (100) orientation p-type silicon with the thickness of 625 μm and a resistivity of 10-20 Ω-cm (purchased from Silicon Inc.) were cut and washed using the RCA method [62]. TMAH 25 Wt. % was purchased from Sachem Inc. and diluted with DI water to reach the desired 2 wt.% concentrations used in the experiments. 99% IPA was purchased from VWR International and was added to the etching solution to obtain weight concentrations of 3.5%.

4.2.1 Textured silicon preparation

Samples of silicon were textured under both GLE and non-GLE conditions. The details of the GLE texturing system have been presented in our previously published work. All other texturing parameters were the same for all samples and set to 2%, 90 °C and 30 min for the TMAH concentration, temperature and etching duration, respectively.

Samples were then washed with DI water and etched with diluted HF to remove any native silicon dioxide possibly formed during the TMAH etching step. Energy-dispersive X-ray analysis (EDX) technique was used to assure the absence of any native oxide layer on the silicon surface prior to the device fabrication step. All SEM imaging and the EDX analysis of the samples were performed using a Hitachi S-4700 field emission scanning electron microscopy (FE-SEM).

4.2.2 Design and fabrication of p-n junction

The textured surface of the p-type silicon sample was used for the fabrication of the p-n junction (diode). First, the p-n junction was designed based on the required depth of the junction. Then, pre-deposition diffusion was used to fabricate the junction based on the design parameters values. The textured p-type silicon sample was doped with phosphorous impurities to create the p-n junction. Table 4-1 lists all the design parameter values used based on the desired design criteria.

Table 4-1 : Parameter values used in the design of the p-n junction.

Parameter Description	**Parameter**	**Value**
Background Concentration	N_{BC} (cm^{-3})	1.39×10^{15}
Pre-deposition Temperature	T (C^o)	1100
Junction Depth	x_j (µm)	0.5
Diffusion Time	t (min)	6

As stated in table 4-1, based on the impurity concentration of 1.39 x 10^{15} cm^{-3} and a desired junction depth of 0.5 µm, the temperature and diffusion time were set to 1100 Cº and 6 minutes respectively.

I-V characteristics of the solar cell devices were carried out using the Keithley 4200-SCS semiconductor characterization system. A Laboratory For Science ultra-stable helium-neon laser operating at 633 nm wavelength, a power intensity of 4 mW and a spot size of 1 cm in diameter was used to illuminate the solar cells.

The phosphorosilica gel was applied to the samples using a spin coating machine at 2000 rounds per minute (RPM) for 30 seconds. The samples were then baked in the oven for 1 minute at 110 °C and placed in the diffusion furnace equipment, illustrated in figure 4-1, under 20% O_2 and 80% N_2 atmosphere to prevent the formation of the so-called "brown stain" which causes high contact resistance in the metallization stage.

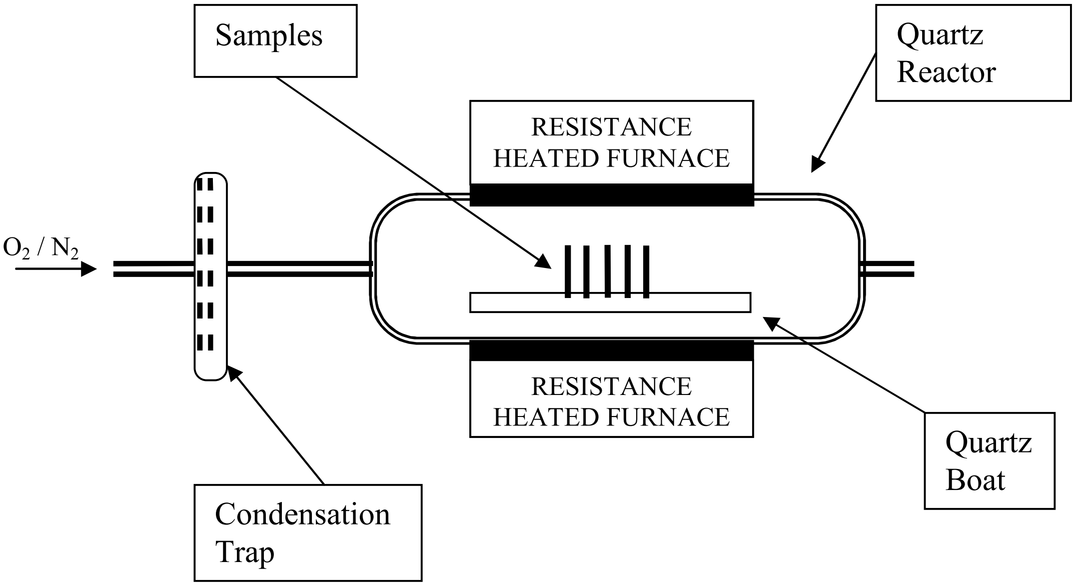


Figure 4-1 : Diffusion furnace equipment setup.

This step was followed by a 30-sec wet oxidation period to create a very thin layer of SiO_2. All excess phosphorosilica gel was removed from the device surface by performing a hydrofluoric acid etching of the oxide layer.

4.2.2.1 Fabricating the electrodes

The metallization is a microelectronic process, by which metal (aluminum) contact is achieved for the back end of the solar cell device. The corners ends and the four sides of the sample were covered with Teflon tapes to prevent any short-circuiting of the back and front of the samples through the sides. The samples were then loaded into the metallization equipment vacuum chamber after being rinsed with DI water and dried by the N_2 gun. At about 10^{-6} Torr, the aluminum was evaporated onto the sample's back surface (p-type silicon). The samples were then removed from the metallization equipment, rinsed with DI water and dried with N_2 gun.

An alloying furnace was used to create an intimate ohmic contact between the deposited aluminum and the silicon on the back end surface of the sample. The alloying was performed at 450 °C for 30 minutes and under equal flow of N_2 and H_2 to prevent silicon oxidation and for passivating the surface of the silicon (treating the surface dangling bonds) respectively. After alloying, the ITO conductive transparent electrode was deposited on the n-type silicon surface using the sputtering technique.

I-V characteristics of the solar cell device was carried out using the Keithley 4200-SCS semiconductor characterization system. A Laboratory For Science ultra-stable helium-neon laser operating at 633 nm wavelength and a power intensity of 4 mW was used to illuminate the solar cells.

4.3 Results and discussions

In order to investigate the influence of the GLE texturing approach on the I-V characteristics of a solar cell device, two sets of devices were textured, designed and fabricated one with and the other without the use of the GLE effect during the texturing stage.

4.3.1 Characterization of the textured silicon

Two crystalline silicon (c-si) samples were prepared and textured using the same wet anisotropic etching conditions but one with GLE effect and the other without. As mentioned in our previous studies, the application of GLE effect during the texturing can influence the characteristics of the surface in terms of morphology and reflectivity. Figure 4-2 shows the SEM images of the samples textured for 30 minutes using 2% TMAH and 3.5% IPA at 90° C.

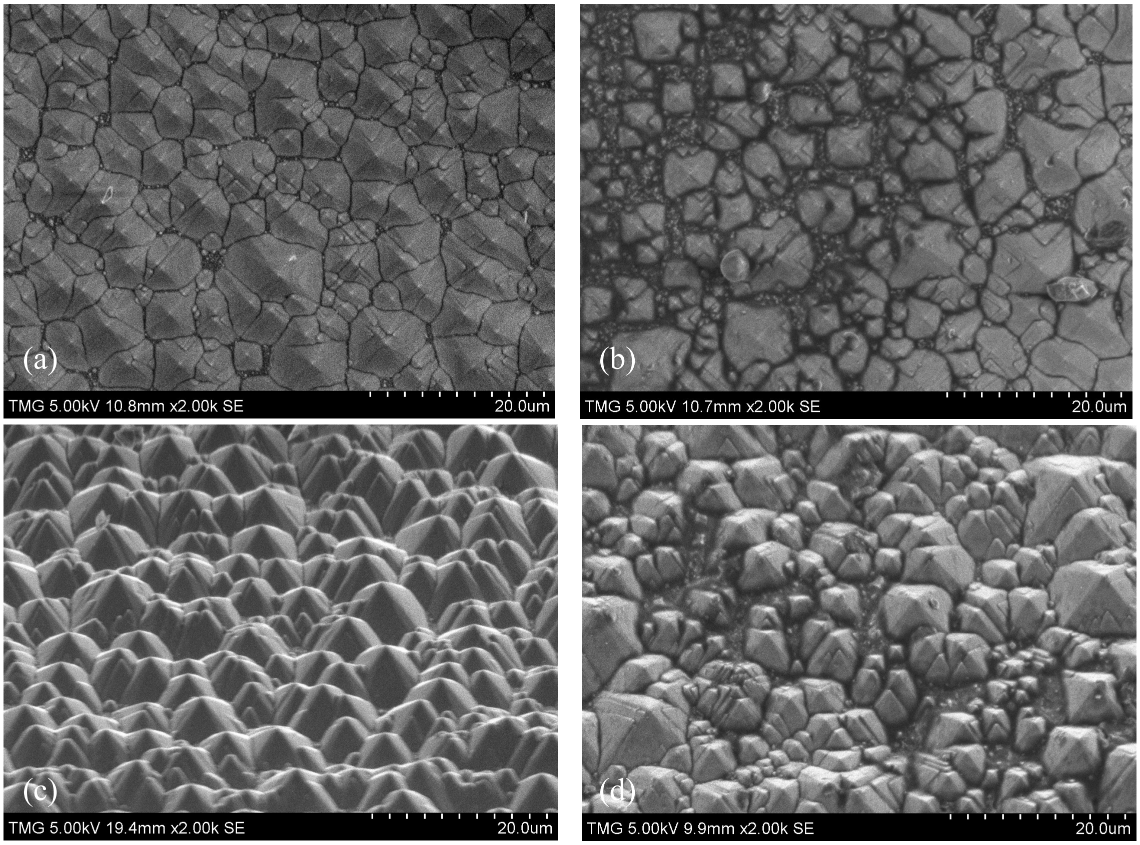


Figure 4-2 : SEM image of the textured sample using a) GLE top view, b) non-GLE top view , c) GLE tilted view and, d) non-GLE tilted view

Figure 4-2a corresponds to the sample with GLE whereas, figure 4-2b corresponds to the one prepared under no GLE effect. Figures 4-2c and 4-2d are the tilted view of the GLE- and non-GLE-textured samples, respectively.

As it may be observed, the use of GLE leads to a higher surface coverage and a more uniform surface texturing characteristics. Some morphological characteristics of the two prepared samples, determined by the image analysis of the SEM images in figure 4-2, are listed in table 4-2.

Table 4-2 : Surface coverage and roughness factor obtained using image analysis.

Parameter	**GLE-Textured Sample**	**Non-GLE-Textured Sample**
Surface coverage (%)	91	70
Real Surface Area (μm^2)	4725	3450
Roughness factor	1.56	1.14

As it may be seen from table 4-2, the sample prepared under the GLE effect shows a 30% higher surface coverage as well as a 37% higher roughness factor. The roughness factor is defined as the ratio of the calculated total real surface area to the geometric surface area.

The specular reflectance of the samples in figure 4-2 was measured over the 400-800 nm wavelength spectrum. The measured specular reflectance versus the wavelength is illustrated in figure 4-3. As it may be noted, the reflectance of the sample textured using GLE (figure 4-3a) is significantly lower than the sample textured in the absence of the GLE effect (figure 4-3b) for the entire spectrum. In order to better quantify this improved reflectivity, the specular Solar-Weighted Reflectance (SWR) was calculated for both samples. Solar-weighted average reflectance is defined as the integration of the product of the reflectance and the AM1.5 photon density, divided by the total number of photons between 400 nm and 800 nm.

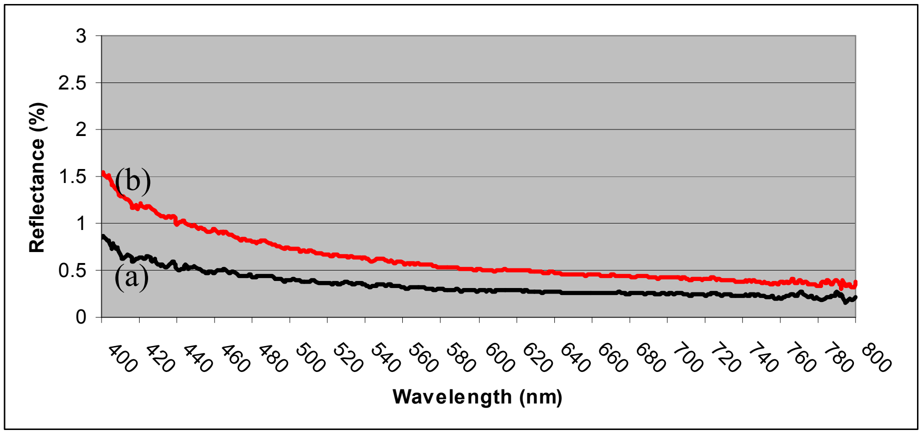


Figure 4-3 : Photo spectroscopy of the a) GLE and b) Non-GLE textured surface.

The Table 4-3 lists the calculated SWR for both samples as well as the measured reflectance at 633 nm wavelength. As it may be noted from table 4-3, an improvement ratio of about 2 is observed for both the calculated Specular SWR and measured reflectance for the sample textured using the GLE method compared to that of non-GLE textured.

Table 4-3 : Calculated SWR for both GLE and non-GLE textured samples.

	GLE Textured Sample (figure 4-3a)	**Non-GLE Textured Sample (figure 4-3b)**	**Improvement Ratio**
Specular SWR (%)	0.29	0.61	2.1
Measured Reflectance at 633 nm (%)	0.26	0.50	1.9

EDX analysis was performed on both samples to validate the absence of any silicon dioxide or any other materials except silicon on the textured silicon. Using a strong base such as TMAH during the texturing stage can cause the creation of a thin layer of native oxide on the surface of the silicon. Figure 4-4 shows the EDX analysis repeated in several spots on the surface of the samples. Silicon was the only element detected in both samples (100%) and the absence of the oxide layer was confirmed.

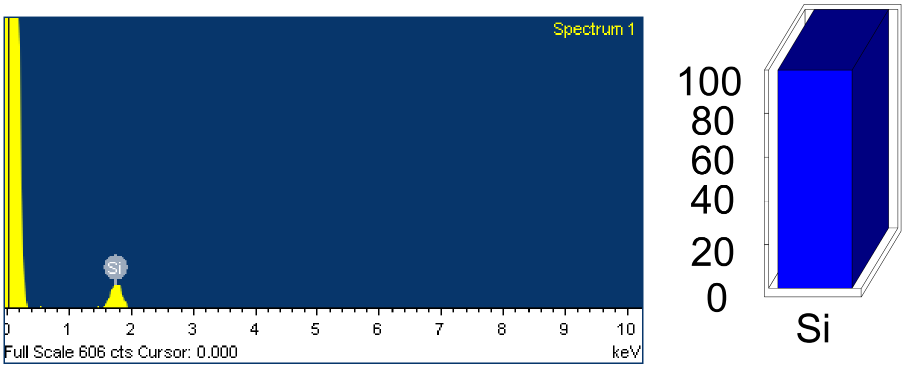


Figure 4-4 : EDX elemental analysis of the samples.

4.3.2 Solar cell device fabrication and characterization

The two types of textured samples (with and without GLE effect) were doped with n-type impurities to create the 0.5 micrometer layer of n-type silicon on top of the p-type silicon substrate as described in detail in section 4.2.2. In order to create the ohmic contacts, the p-type and the n-type side of the created junction were sputtered with aluminum and Indium-doped Tin Oxide (ITO), respectively. The schematic of the fabricated solar cell device is illustrated in figure 4-5.

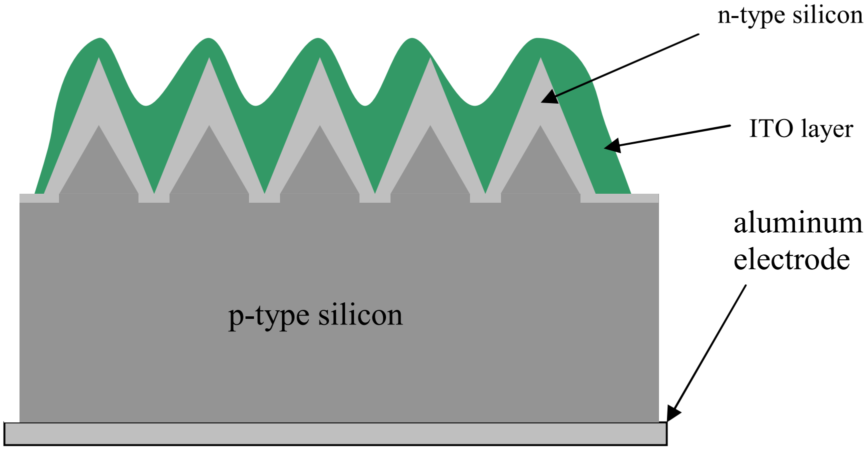


Figure 4-5 : The schematic of the solar cell device.

Figure 4-6 illustrates the SEM images of ITO (figure 4-6a) and aluminum (figure 4-6b) layers deposited as electrodes for the fabricated solar cells. Figure 4-6a confirms the deposition of the intended 350 nm layer of ITO. It shows that after the deposition of the ITO layer, the morphology of the textured layer has been maintained, i.e., the ITO deposition followed the morphology of the textured surface. The intended deposition of about 250 nm layer of aluminum is also evidenced and confirmed by the SEM image in figure 4-6b.

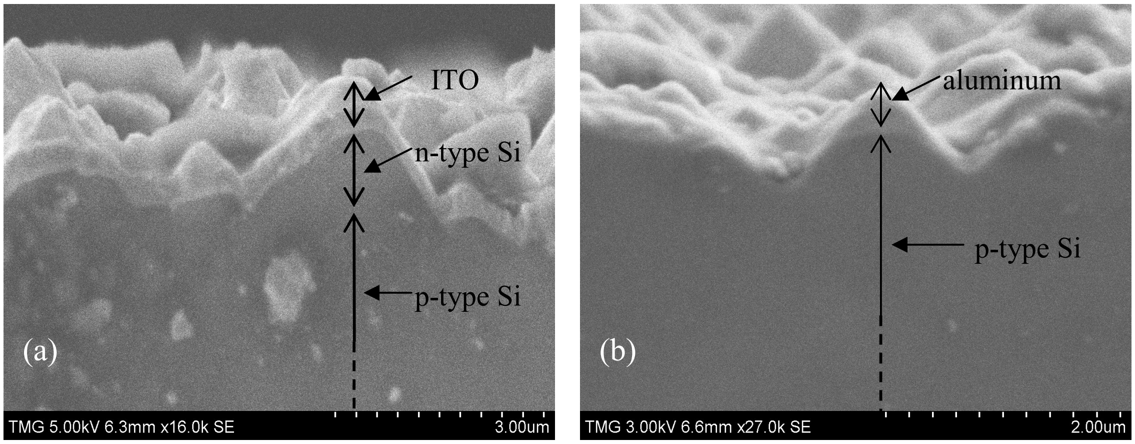


Figure 4-6 : The SEM image of the a) ITO electrode, and b) aluminum electrode layer on silicon.

4.3.2.1 I-V characteristics

A two-probe semiconductor analyzer was used to measure the I-V characteristics of the solar cells fabricated under both GLE and non-GLE texturing conditions. In order to calculate the efficiency based on the measured output power, a light source with stable power and wavelength of 4 mW and 633 nm, respectively, was used. Illuminated and dark I-V characteristics were measured and recorded between -1 and 2 Volts for both solar cells. Figure 4-7 illustrates the output dark and illuminated current of the non-GLE textured device for the -1 to 2 sweeping voltages.

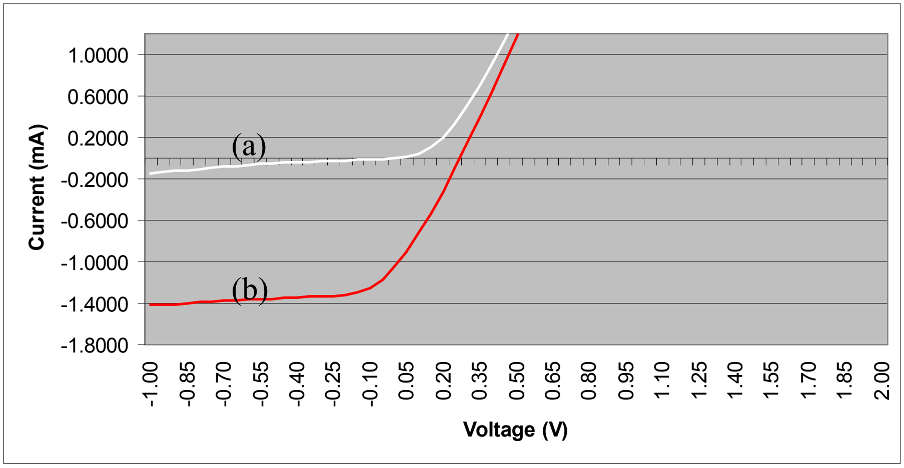


Figure 4-7 : a) Dark and, b) illuminated I-V characteristics of the non-GLE textured solar cell.

The diode behaviour under both dark and illuminated conditions confirms the existence of the p-n junction of the fabricated device. The typical increase in current in the negative voltage bias confirms the generation of the photo current in this solar cell device.

Figure 4-8 shows the I-V characteristics for the GLE-textured solar cell under both dark and illuminated conditions. Again, the typical diode behaviour and the photocurrent existence are observed in this figure for the GLE-textured solar cell.

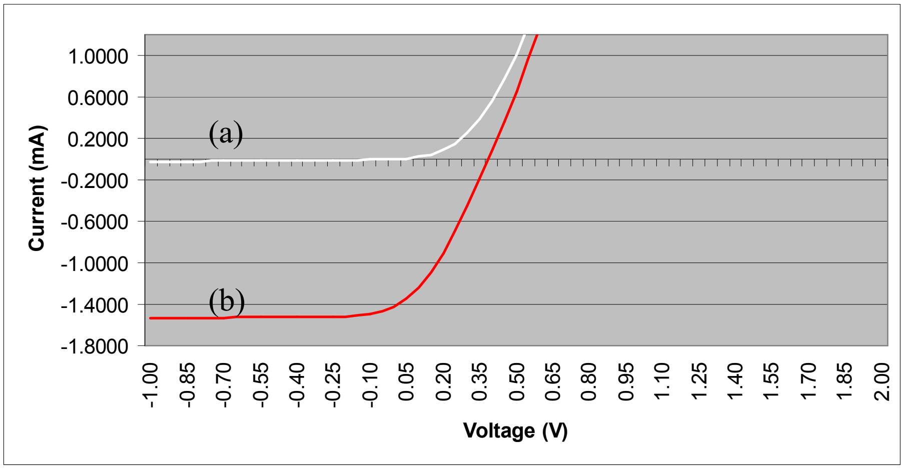


Figure 4-8 : a) Dark and, b) illuminated I-V characteristics of the GLE textured solar cell.

Table 4-4 summarizes the input parameter values as well as the output measurements obtained from the data illustrated in figures 4-7 and 4-8.

Table 4-4 : I-V measured parameters for the fabricated solar cells.

	V_{oc} (V)	J_{sc} (mA/cm^2)	V_{max} (V)	J_{max} (mA/cm^2)	P_{max} (mW)
GLE-Textured Solar Cell	0.42	1.42	0.2	0.91	0.2
Non-GLE-Textured Solar cell	0.3	1.1	0.15	0.53	0.1

The Fill Factor (FF) of a solar cell can be characterized as a fraction involving the maximum output power (V_{max} x J_{max}), open circuit voltage (V_{oc}) and short circuit current density (J_{sc}) according to the following equation [17]:

$$FF = \frac{P_{\max}}{V_{oc} \times J_{sc}} = \frac{V_{\max} \times J_{\max}}{V_{oc} \times J_{sc}}$$

where V_{max} and J_{max} are the voltage and current at the maximum power point.

The estimated efficiency of the solar cell can be calculated by:

$$\eta_{est} = \frac{P_{\max}}{P_{in}}$$

where P_{in} (4 mW) is the incident light power density.

Table 4-5 lists the calculated values for the P_{max}, FF and the estimated efficiencies for both the GLE-textured and non-GLE-textured solar cells.

Table 4-5 : Calculated output values for the fabricated solar cells.

	P_{max} (mW)	FF	η_{est}
GLE-Textured Solar Cell	0.2	0.3	5
Non-GLE-Textured Solar cell	0.1	0.2	2.5

It may be observed that, for a 150% improved FF, the value of the P_{max} for the GLE-Textured solar cell device is more than double of that of the device based on the silicon texturing under the exact same conditions but without the use of the GLE effect. This higher P_{max} also results in a much higher efficiency of the GLE-textured solar cell device

(5% compared to 2.5%). It is important to point out that significant increase in efficiency is achieved without the use of any additional consumables or reagents during the silicon texturing stage and therefore, with practically no impact on the production cost of the manufactured solar cells.

The higher efficiency of the GLE-textured solar cell device may be attributed to its lower surface reflectivity due to a higher surface coverage as well as a higher real surface area resulting in more efficient light trapping. Furthermore, higher real surface area leads to the generation of more electron-hole pairs in the GLE-textured solar cell device under illumination contributing to its higher efficiency. In fact, as observed from the data presented in tables 4-2, 4-3 and 4-5, an increase of more than 37% in the real surface area in the GLE-textured surface results in half the reflectivity and more than 200% increase in power efficiency of the fabricated solar cells.

It should be noted, that although the values of the efficiency presented in this study are lower than typical optimized devices, they are only used to evaluate the impact of using the GLE effect on improving the efficiency of a given solar device. As also mentioned earlier, these lower-than-typical values can be attributed to the higher thickness of the silicon wafer used resulting in higher V_{oc} and J_{sc} due to higher series resistance and higher recombination.

4.4 Conclusion

The use of GLE effect as a novel approach during the wet anisotropic etching of silicon and its effect on the morphology and reflectivity characteristics of the textured surface has been reported in our previous works. In this chapter, the effect of the GLE-texturing approach on the I-V characteristics and the power efficiency of the fabricated were investigated.

The use of GLE effect during the texturing stage resulted in a textured surface presenting a much higher coverage and uniformity as well as a significantly higher surface area. The GLE-textured silicon surface also showed a much lower reflectivity (less than half) compared to the surface texture under the exact wet-etching conditions but with no GLE effect present.

I-V characterization of the solar cell devices fabricated with and without the GLE-textured silicon surfaces showed that the power efficiency of the device can be more than doubled as a result of using the GLE-textured surface. This may be attributed to a higher electron-hole pair generation and a lower reflectivity due to the considerable increase in the real surface area (more than 37%) as a result of the application of the GLE effect during silicon surface texturing.

Considering the fact, that the use of GLE effect does not imply the use of any additional reagents during the texturing process, its application will contribute to significant improvement in the solar cell output power efficiency without increasing the production cost.

5 Further strategies for the optimization of the solar cell device

Two additional strategies were studied to potentially further increase the efficiency and decrease the fabrication cost of such solar devices by integrating an array of micro-rod structures with nano-tip and a low cost conductive-transparent electrode, respectively.

5.1 An array of micro-rod structures with nano-tip

In this study a new multistage approach is introduced for the fabrication of arrays of silicon micro-rods with nano-tip and the growth mechanism of such structure is investigated. In the first stage, the surface of silicon wafers was textured using anisotropic etching method to generate the array of pyramids. Next, the textured surface underwent an electrochemical anodic etching in HF:ethanol solution. The study of the anodic etching showed that the etching initiated at the edge of the pyramids and progressed inward through the faces. The four 111 faces of the pyramids etched forming a pore at each face. At the final fabrication stage, the interconnected walls in the porous silicon layer are etched using diluted NaOH. Results show that the tip of pyramids corresponds to the nano-tips of the micro-rods. A good correlation between the number of pyramids per unit surface area and that of the micro-rods with nano-tip was observed. It was also observed that the micro-rods formed only for high pyramid surface coverage. The effect of anodic electrochemical parameters such as current density and etching time on the fabrication of the silicon micro-rods with nano-tip were investigated. Longer electrochemical etching resulted in thinner interconnect walls, needing shorter NaOH etching time to form and reveal the array of micro-structures with nano-tip.

5.1.1 Introduction / Background Information

Electrochemical etching of silicon in HF solution has attracted a great attention for the fabrication of various micro-structures such as porous silicon [63], trenches [64], and pillars [65] [66]. Recently, fabrication of one-dimensional n-type silicon nanowires from porous silicon has been developed using photo-assisted electrochemical etching [67]. These fabrication methods use oxidation and/or wet etching as post-processing techniques leading to the creation of pillars and nanowires.

In order to pre-determine the location of the fabricated silicon nanowires, in the conventional method, the silicon surface is first patterned using lithography technique followed by wet etching [68] [69]. This technique leads to the creation of inverted pyramids on the silicon surface followed by the formation of porous silicon starting at the pit of these inverted pyramids.

In this work, a new non-lithographical method was used for the fabrication of array of silicon micro-rods with nano-tip. In this approach, the pyramid shape seeding points were first created on the surface of the silicon. Each of these pyramids will become the head with nano-tip of the silicon micro-rods created in the subsequent fabrication stages. This method of synthesizing an array of silicon micro-rods with nano-tip is appealing because the process is non-lithographic and can lead to a low-cost route for fabricating MEMS/NEMS as well as optoelectronic devices. The detail study on growth mechanism of such structure helped develop methods to control the array density and size characteristics of the micro-structures with nano-tip. To the best on our knowledge this is the first report of implementing the electrochemical anodic etching on the textured pyramids surface with no lithography technique aimed at fabrication of arrays of silicon micro-rods with nano-tip.

The influence of NaOH fine-etching time on the morphology and geometry of the structure was investigated in our previous work [70]. Here we report the impact of anodic electrochemical conditions and pyramid surface coverage on the fabrication of the array of silicon micro-rods with nano-tip.

5.1.2 Experimental Procedure

P-type silicon wafers with (100) orientation, and resistivity of 10-20 Ω-cm, were purchased from Silicon Inc. and were used for all experiments. All samples were cleaned prior to experiments using the RCA process. Due to the existence of hole majority carriers in p-type silicon, no illumination of the samples were required.

25wt% tetramethylammonium hydroxide (TMAH) was purchased from Sachem Inc. and diluted with DI water to reach the desired 1.5 wt% concentration used in all experiments. 99% isopropyl alcohol (IPA) was purchased from VWR International and added to the etching solution to obtain 1.5wt.% and 6wt.% weight concentrations. 99.5% ethanol, and 97+% NaOH were purchased from Sigma-Aldrich. 48.8% HF was purchased from ACP Chemicals Inc. Canada.

The anodic electrochemical etching was performed using Allied Research galvanostat potentiometer. The developed nanostructures were characterized using Hitachi S-4700 field emission scanning electron microscopy (FE-SEM). The population density of structures and surface coverage measurements were all obtained by performing image analysis of the SEM photos using ImageJ image processing program developed by the US National Institute of the Health.

This novel approach requires three stages of fabrication to create the desired nano-structure array. Figure 5-1 illustrates the three-stage fabrication transition and the morphology of the created surface structure at the end of each stage. The three fabrication stages are as follows:

1. Anisotropic wet etching of the polished silicon surface using a strong basic solution to create the textured surface consisting of an array of pyramids (figure 5-1a).
2. Anodic electrochemical etching of the textured silicon using a strong acidic solution to create a porous silicon (pSi) layer (figure 5-1b).
3. Fine-etching of porous silicon layer to achieve the desired array of micro-rods with nano-tip (figure 5-1c).

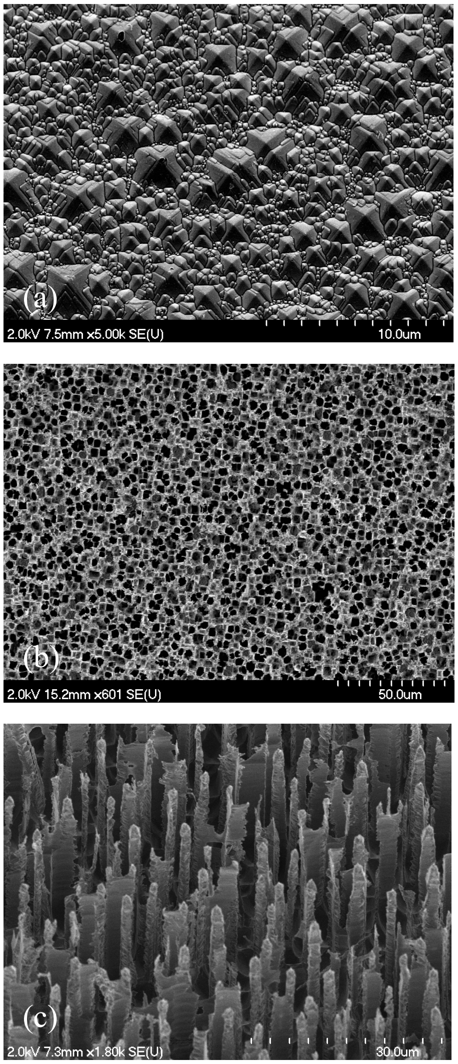


Figure 5-1 : (a)Textured silicon surface after the first fabrication stage (b) the porous silicon layer as a result of the anodization stage (c) the revealing of the array of nano-rods with nano-tip after the final fabrication stage.

5.1.2.1 First fabrication stage (texturing silicon)

Surface of a 1 cm^2 samples of silicon wafer were textured using anisotropic etching process in 1.5 wt% TMAH for 30 minutes. Figure 5-2 illustrates the equipment setup used for the alkaline etching of the samples.

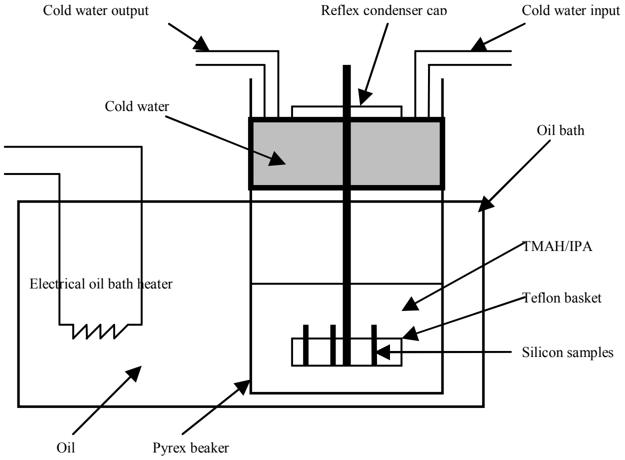


Figure 5-2: Schematic view of TMAH etching apparatus.

Pyramids with various sizes were developed on the surfaces of the samples. During the process IPA was added to TMAH solution in order to remove the hydrogen bubbles from surface of the sample faster to facilitate the etching process. As we have reported in the earlier work, the concentration of the added IPA will influence the size and surface coverage of the pyramids [53]. The novel optimized GLE texturing system developed in our previous work [61] was not used in order to study the effect of various pyramids concentration on the developed final array structure. In this stage we have used samples etched in TMAH with added various IPA concentrations (0, 1.5, & 6 wt%) to create various pyramid concentrations.

5.1.2.2 Second fabrication stage (pSi creation)

An anodic electrochemical etching was performed on the textured silicon surface to create a layer of porous silicon. The etching was done in a two-electrode Teflon cell with metal base plate to form a back ohmic contact. Figure 5-3 illustrates the electrochemical cell equipment used for anodic etching of the textured samples.

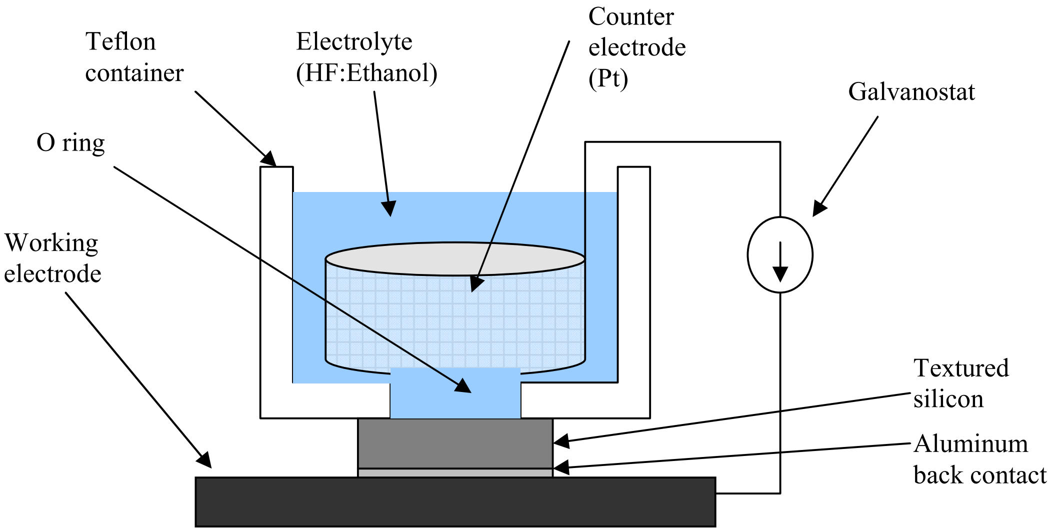


Figure 5-3: Experimental setup for anodic etching of the textured silicon.

A thin layer (~ 1 µm) of aluminum was deposited on the back side of the silicon wafer to obtain an ohmic contact. The silicon wafer is served as working electrode (anode) and the platinum mesh served as counter electrode (cathode). Experiments were performed with various anodic current densities and etching times in such a way that the total charge participating in the reaction, Q, was kept constant at 144 C/cm^2 (e.g. 0.08 C/s-cm^2 x 1800 s or 80 mA/cm^2 x 30 min). The etching solution (electrolyte) consisted of 1:3 (HF:Ethanol) mixture for all experiments. Ethanol was added as a surfactant to facilitate the detachment of the hydrogen bubbles from the surface of the silicon, therefore, resulting in the formation of a more uniform porous layer.

5.1.2.3 Third fabrication stage (array of micro-rods with nano-tip)

Alkaline solution, consisting of a diluted NaOH (0.2 Molar), was used to fine-etch the porous silicon layer in order to achieve the desired nano-structure. In this fabrication stage, the walls connecting the pillars in the porous silicon layer were etched until the desired nano-structure array was achieved. A few drops of IPA were applied to the surface of the sample (porous silicon) to increase its wet-ability before immersing it into the NaOH solution. The temperature was kept constant at 35 ºC, and some agitation was applied using a magnet stirrer.

5.1.3 Results and Discussion

5.1.3.1 Characterization of the textured silicon surface

Samples with different pyramid surface coverage (during the first stage of anisotropic etching) were achieved as a result of various IPA concentrations. Figure 5-4a illustrates the SEM image of a sample textured using 1.5 wt % concentration for IPA (high surface coverage). Figure 5-4b illustrates the use of image analysis of the SEM image to calculate the surface coverage and the number of pyramids per unit area.

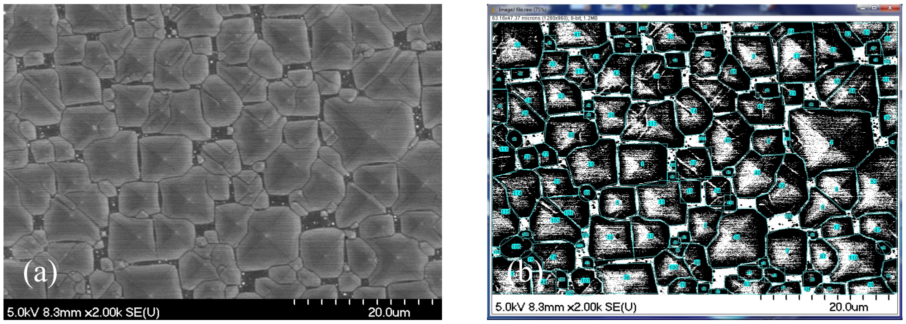


Figure 5-4: (a) Textured silicon surface, (b) image analysis of the textured silicon surface.

Table 5-1 summarizes the influence of various IPA concentrations on the resulting pyramids surface coverage and the number of pyramids per unit area. In order to obtain an average of the measured values, the same experiment was repeated three times. As it may be observed from Table 5-1, as the IPA concentration increases so do the average pyramids surface coverage and the average number of pyramids per unit area.

Table 5-1: Calculated surface coverage and number of pyramids per 1000 μm^2 using image analysis.

	Sample1	**Sample2**	**Sample3**
IPA concentration (wt.%)	0	1.5	6
Average Surface coverage of pyramids (%)	48	82	100
Average No. of pyramids per 1000 μm^2	31	41	51

These results were used to correlate the morphology and density of the fabricated nano-structure array to that of the pyramid-textured surface. The density of the pyramids and how closely packed they were, influenced the creation of the nano-structure array in subsequent fabrication stages.

5.1.3.2 Characterization of the porous silicon layer created at 2nd stage

To investigate the effect of anodic electrochemical etching parameters on the desired nano-structure, experiments were conducted with various anodic current density and anodic etching time but under constant total charge, Q = 144 C/cm^2. The HF:Ethanol concentration ratio was kept constant at 1:3 for all experiments.

5.1.3.2.1 Pores initiation and growth mechanism

Figure 5-5 illustrates the progress of the pore formation during the anodic etching stage. The textured surface illustrated in figure 5-5a was prepared under the texturing condition of sample 2 listed in table 5-1. Figure 5-5b shows the pore formation progress after 1 minute. It was observed, that the pore formation initiated from the edge of the pyramids.

Image 5-5c is the top view of the silicon sample after 3 minutes of anodic etching. The etching had initially started at the edges (figure 5-5b), followed by the etching of the pyramid faces. The tip of the pyramid identified in figure 5-5c by a square, has remained passivated and un-etched. The arrows in figure 5-5c identify the four 111 faces of the pyramid where the etching took place during the porous formation. Figure 5-5d shows the cross sectional view of the same sample where the two arrows illustrate the etched pyramid faces.

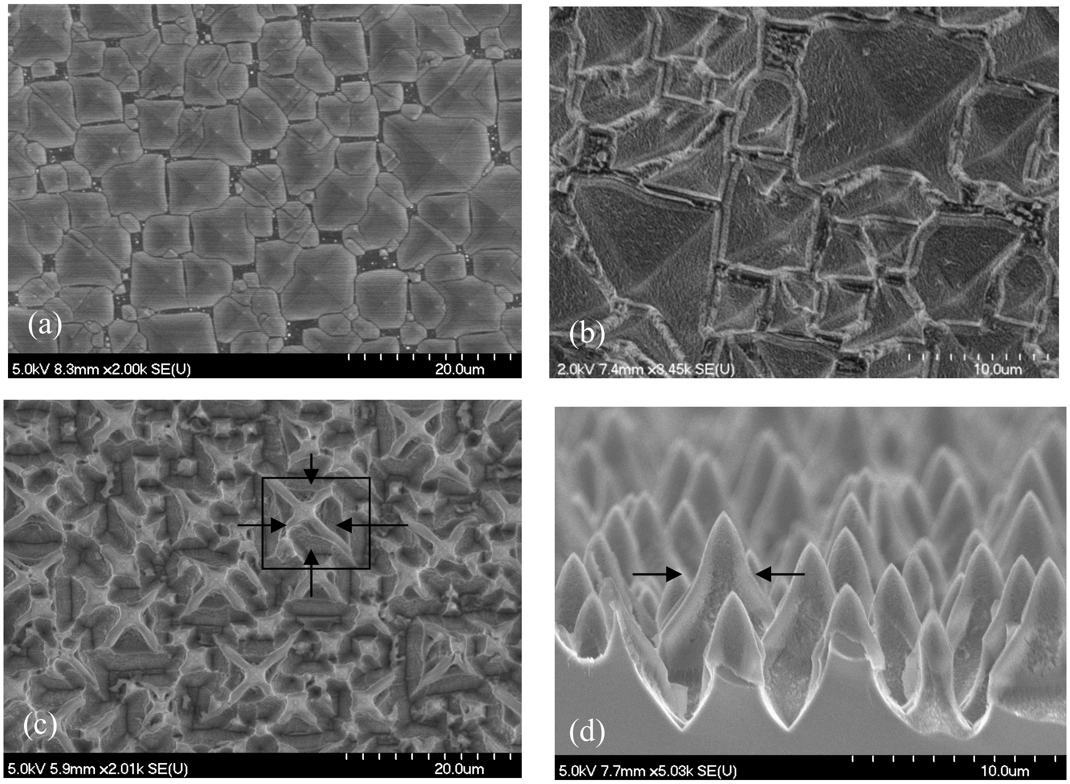


Figure 5-5: The top view of start and progression of the porous layer, (a) textured surface, (b) after 1 minute anodic etching time, (c) after 3 minute anodic etching time, (d) cross section view of the structures in c.

As it has been reported in the literature, in the case of the inverted pyramids textured surface, the pore formation started from the pit of the inverted pyramids due to the higher electric field [71]. Here we report that the pore formation initiation point to be the edges of the pyramids and not the sharp tips. This may be attributed to the roughness that had been created as a result of the anisotropic etching during the first fabrication stage. It has been reported that the roughness of the (111) planes leads to the formation of di-vacancies and tri-vacancies [72] [73]. During anoding etching, the dangling bonds on silicon surface are terminated by hydrogen atoms in the forms of mono, di, and trihydride in HF solution [74]. However, the number of hydride depends on the orientation and roughness of the surface [75]. The dihydride ($Si-H_2$) and trihydride ($Si-H_3$) termination on silicon surface results in a stronger polarization of the back Si-Si bonds. This polarization is considered to be responsible for weakening the back Si-Si bonds and therefore, facilitate their removal. The initiation of the etching at the edges of the pyramids followed by the 111 faces may be attributed to the trihydride termination of the surface atoms which leads to the preferentially attacked 111 faces.

5.1.3.2.2 Porous formation under various anodic etching conditions with constant charge passed

The effect of various anodic current density and anodic etching time (at constant charge passed) on the formation of silicon porous layer were investigated using sample 2 (table 5-1) as the substrate. Furthermore, the impacts of these anodic conditions on the fabrication of the desired silicon nano-structure array in the subsequent stages were studied. The current density and the etching time were altered such a way that Q remained the same for all experiments.

Figure 5-6a illustrates top view of the morphology of the porous silicon layer created on sample 2 using 80 mA/cm^2, and 30 minutes for anodic current density and etching time respectively. The figure shows the porous silicon consisting of pillars and walls connecting them. It also shows the passivated and unetched tip of the pyramids after 30 minutes of etching time. The circled area in figure 5-6a is magnified and illustrated in figure 5-6b identifying the pillars and the wall. Figure 5-6c illustrates the 45-degree tilted view of figure 5-6a.

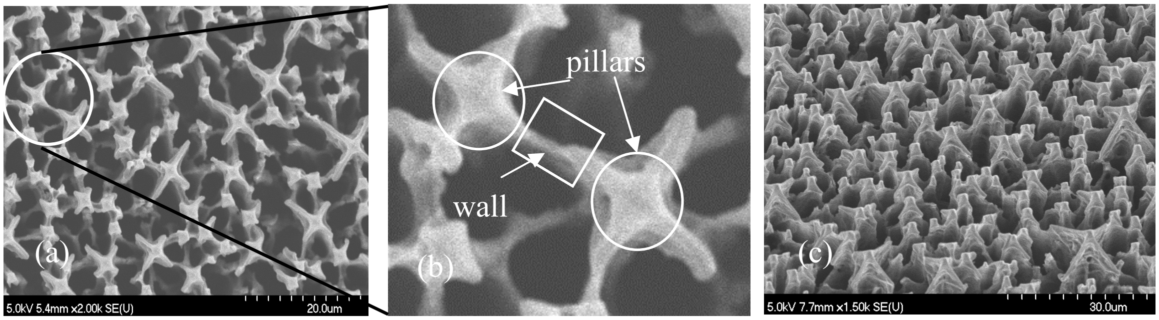


Figure 5-6: (a) The top view of silicon porous layer after 30 min, (b) enlarged image of circled area, and (c) 45 degree tilted view of the image.

This morphology may be attributed to the etching of the edges followed by the faces of the pyramids. Table 5-2 lists the experimental parameter values used for anodic current density and etching time. Image analysis was performed on the SEM images of the anodically etched samples to obtain the average number of pillars per unit area, the average surface coverage of pillars, as well as the porous layer depth also listed in table 5-2.

Table 5-2: Anodic conditions used and the morphological characteristics of the created silicon pillars calculated using the image analysis of the SEM photos.

Anodic Current density (mA/cm^2)	**100**	**80**	**40**	**20**
Etching time (min)	**24**	**30**	**60**	**120**
No. of pillars per 1000 µm^2	0	25	31	39
Surface coverage of pillars (%)	0	10.2	19.6	27.6
Porous layer depth (µm)	0	15	35	47

Experiments showed that, at current densities higher than 80 mA/cm^2, the samples were polished and no porous silicon layer was created. It can also be observed from table 5-2 that, as the current density decreased and etching time increased (under constant charge-passed condition), the average number of pillars per unit area, pillars surface coverage, as well as the porous layer depth increased.

Comparing the results in table 5-1 with those in table 5-2, one may observed that, for the same surface area, the number of created pillars is less than the number of pyramids. This may be due to entirely etching of the smaller pyramids during the anodic etching stage.

5.1.3.3 Characterization and analysis of the nano-rod array with nano-tip

5.1.3.3.1 Effect of anodic etching parameters under constant Q condition

As it was listed earlier in table 5-2, samples with different morphology of porous layer were obtained as a result of various anodic etching conditions. In this stage, the samples were immersed into NaOH solution to dissolve the interconnected walls and reveal the nano-structures. Figure 5-7 illustrates the effect of anodic etching conditions on the number of pillar (pre-NaOH etching) as well as the number of nano-structures (post-NaOH etching) per 1000 μm^2. It can be observed that, under constant charge-passed condition, a combination of lower current density and higher etching time results in higher number of pillars. However, only a specific anodic etching condition (80 mA/cm^2 and 30 min) results in the creation of nano-structure arrays at the end of the final stage of the fabrication. In fact, further away from this optimal condition, almost no nano-structure was achieved. As the anodic current was reduced the pore diameter decreased resulting in the creation of thicker walls. On the other hand, as the etching time increased, the depth of the pores increased as well. A combination of thicker wall (connecting the pillars) and deeper pores created at the 2nd fabrication stage may hinder the formation of the nano-structures in the 3rd stage.

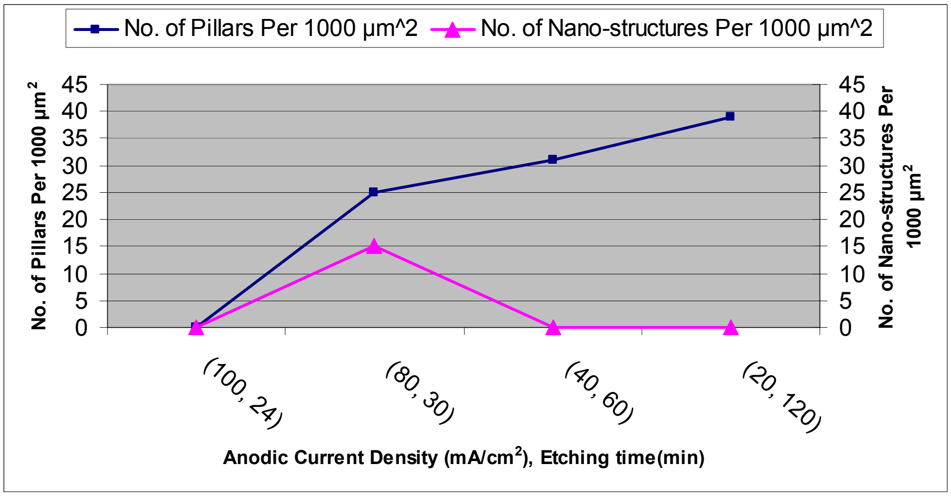


Figure 5-7: Number of pillars per 1000 µm^2 and number of nano-structures per 1000 µm^2 at various anodic etching conditions.

5.1.3.3.2 Effect of anodic etching parameters under various Q values

As it was shown in figure 5-7, the nano-structures were obtained only under certain anodic etching condition (80 mA/cm^2 , 30 min). In order to investigate the effect of anodic etching parameters under various Q values on the creation of nano-structure arrays, the current density was kept constant at 80 mA/cm^2 , while the anodic etching time was changed. Shallower pores with thicker walls were fabricated under 80 mA/cm^2 current density when the samples were anodically etched for 5 and 15 minutes. However, to acheive the nano-strucures, the NaOH fine-etching time needed to be increased in order to compensate for the thicker walls. Figure 5-8 illustrates the nanostructures when the anodic current density was kept at 80 mA/cm^2 for various anodic etching times. The NaOH fine-ecthing time was increased to obtain the desired nano-structure arrays.

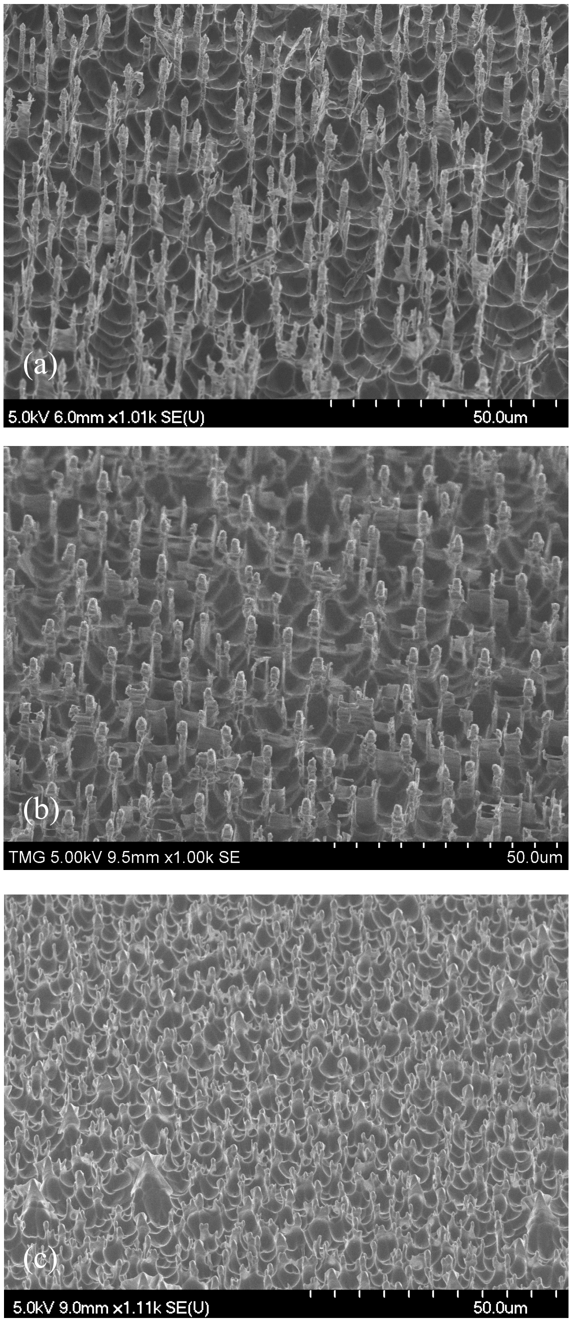


Figure 5-8: The nano-structure array fabricated under constant 80 mA/cm^2 and various etching time, (a) anodic etching time (30 min), NaOH etching time (2.5 min), (b) anodic etching time (15 min), NaOH etching time (4 min), (c) Anodic etching time (5 min), NaOH etching time (5min).

Table 5-3 summarises the influence of the anodic etching time on the geometry and aspect ratio of the fabricated arrays of micro-rods with nano-tip. The longer the anodic etching time, the higher aspect ratio was acheived. It can also be observed from the table 5-3 that as the anodic etching time is increased, the tip diameter of the nano-structure becomes smaller.

Table 5-3: Measured geometric characteristics of nanostructures for samples under different etching times.

	Anodic etching time (min)	Tip diameter (nm)	Length (μm)	Rod diameter (μm)	Aspect ratio
(a)	30	50	15	2	7.5
(b)	15	100	10	3	3.3
(c)	5	500	4	2.5	1.6

5.1.3.3.3 Effect of pyramid surface coverage

In order to investigate the effect of pyramid surface coverage on creation of nano-structure array, samples with various surface coverage were fabricated (as detailed in section 3.1). Then the samples listed in table 5-1 were anodically etched under the best set of anodic etching conditions, 80 mA/cm^2 and 30 minute (as illustrated in figure 4) followed by etching in NaOH solution.

Figure 5-9 shows the relation between the surface concentration of pyramids to the concentration of produced nanostructures. It was observed, that there is a correlation between the pyramid surface coverage and the number of generated nano-structures. As the pyramid surface coverage increases, the number of nano-structures also increases. It may also be noted, that number of nano-structures decreases dramatically as the pyramid surface coverage gets below 80%. This may be attributed to the fact that, as pyramids surface coverage decreases, the spaces between the pyramids increase. This results in random pores creation in the empty space between the pyramids. The creation of random pores with smaller diameters (and therefore thicker walls) hinders the removal of the walls and therefore preventing the generation of the array of micro-rods with nano-tip at the NaOH etching stage. The number of nano-structures is increased as the rate of pyramid surface coverage goes above 80%. However, at much higher rates, the ratio of the pyramid to nano-structure stayed practically the same. This shows that the number of nano-structures per a certain surface area may be increased (higher density) without having an impact on the conversion rate.

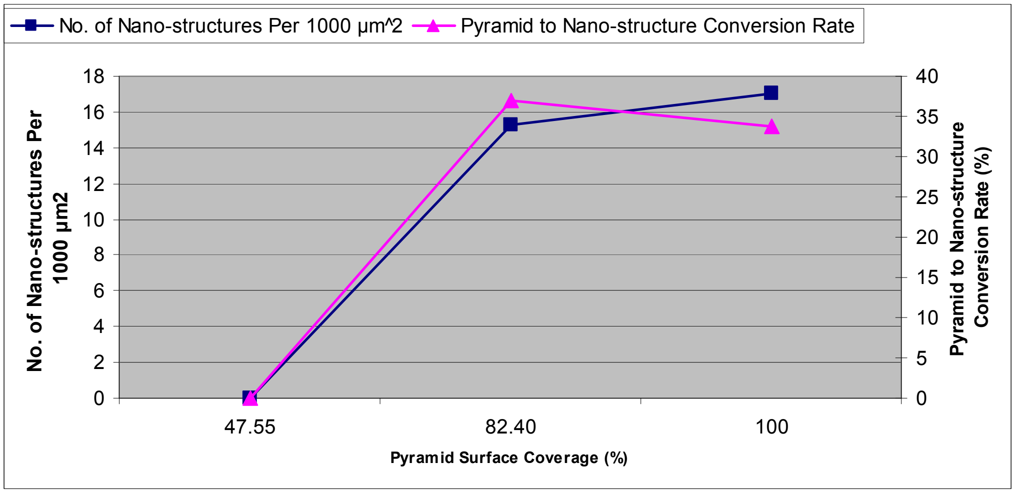


Figure 5-9: Number of nano-structures per 1000 μm^2 and pyramid to nano-structure conversion rate at various pyramid surface coverage.

5.1.4 Conclusion

Array of silicon micro-rods with nano-tip was fabricated through a novel low cost multistage approach. The pyramid structures practically covered the entire silicon surface as a result of anisotropic wet etching technique. This stage was followed by electrochemical anodic etching. The etching initiated at the four edges of the pyramids and progressed inward through 111 faces. The pores were grown vertically along the [100] direction at each face. In the final stage the interconnected porous walls were etched, to form the nano-structure array.

The first fabrication stage is a vital step towards the fabrication of silicon nano-structure arrays. The highly packed pyramids surface coverage is a prerequisite for fabrication of silicon nano-structure array, as the number of nanostructures drops dramatically below 80% and no nano-structures were obtained at low surface coverage values of around 50%. Experiments revealed that, for a constant charge passed, as the current density decreases the pillar density increases. On the other hand, the higher number of pillars per surface area does not necessarily result in higher number of nano-structures. Accordingly, the optimal current density value seems to be around 80 mA/cm^2 as greater values resulted in no nano-structure formation (due to surface polishing) and at lower values, the creation of thick walls prevented the transformation of the created pillars into nano-structures.

The anodic etching time may be used as a practical parameter to control some nano-structure characteristics such as length and thickness.

The fabricated nano-structure array may have wide applications in optoelectronic devices, energy harvesting and storage, MEMS/NEMS, as well as electron emitters in field emission devices.

5.2 A low-cost transparent conductive electrode

Transparent conductive films (TCFs) are optically transparent and electrically conductive. TCFs are increasingly desired for a growing number of applications such as electromagnetic impedance (EMI) shielding in electronic devices as well as optoelectronic devices such as solar cells. TCFs for photovoltaic can be categorized into inorganic and organic. Examples of inorganic materials for the fabrication of such films are indium tin oxide (ITO) and fluorine doped tin oxide (FTO) which are rather expensive. The organic films can be fabricated with much lower cost using a mixture of conductive nano-scale materials, such as copper or silver, and a transparent polymer like poly-methyl methacrylate (PMMA). Metal nanowires have low electric resistivity, high surface areas and high aspect ratios. Therefore, they can be used in combination with commercial transparent plastics for the synthesis of an organic TCF. In this work, we present a method to synthesize thin transparent and moderately to highly conductive TCF of copper nanowires (CuNWs) and low-cost PMMA polymer. Alternative polymers, such as polycarbonate (PC), are more expensive and toxic.

CuNWs of 100-300 nm in diameter and 4-6 μm in length were synthesized from spherical copper seeds in an aqueous solution of NaOH, Cu(NO3)2, ethylene diamine and hydrazine. These large aspect ratio CuNWs (i.e. length/diameter of 30-60) were then processed in the solution state to disperse in a commercial grade PMMA polymer for the production of suspensions by a combination of molecular diffusion and shear. The suspensions of CuNWs/PMMA/solvent were used to fabricate the thin TCFs by solution casting method. Thin TCFs of various thicknesses (i.e. 10 μm to 200 μm), with surface conductivities as high as 1.0 Ω^{-1} and an average transparency of about 55% (300-800 nm), were fabricated by the proposed low-cost method.

5.2.1 Introduction / Background Information

Plastics, by nature, are non-conductive and have high electric surface resistivity (i.e. 10^{14}-10^{20} Ω/sq). They tend to hold electrostatic charges and allow electromagnetic/radio frequency interference (EMI/RFI) to pass through. However, adding an adequate number of conductive high-aspect ratio particles can make plastics partially or highly conductive while still maintaining acceptable transparency. The conductive particles in the plastic phase (above a concentration range referred to as percolation concentration [76]) form a network in contact together and hence start to significantly carry electric current while the cohesion and strength of the particle remains intact. The final product is a conductive polymer composite which can be used for different usages. Figure 5-10 illustrates the different practical applications of conductive plastics in the electronics industry with the range of electric surface resistivity required for each category.

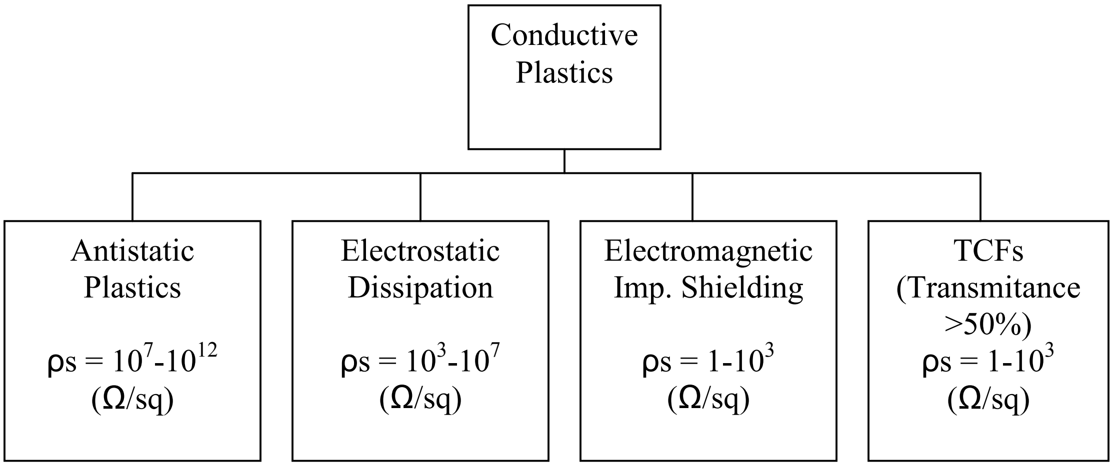


Figure 5-10: Applications of conductive polymers currently used in the electronic industry with the desired surface resistivity range for each application.

In recent years, plastic materials have been used to a greater extent as materials of choice in EMI/RFI shielding applications for internal parts (replacing metal parts) in electronic components such as computers, smart phones, mobile devices and other electronic products. Compared to the conventional metal parts, conductive plastics offer greater design flexibility, lighter weight, and colourability. Additionally, they provide great advantages since the plastic parts can be fabricated by high throughput and cost effective polymer processing machinery to form complex parts. For photovoltaic applications, the challenge is to convert inherently insulating thermoplastic materials to a product that would provide relatively high conductivity while maintaining acceptable transparency. This is also referred to as providing multi-functionality to the plastic part so that it possesses (besides electric conductivity) other properties such as structural, mechanical, or optical. It is the intent of this present investigation to design and fabricate moderately to highly conductive films of nanocomposites of metal fibers (copper nanowires) and transparent plastics (PMMA) for usage as thin TCFs in the photovoltaic applications.

5.2.2 Experimental Procedure

5.2.2.1 Synthesis of copper nanowires (CuNWs)

Chemical reaction for the synthesis of long CuNWs was performed in a 2 litre round bottom flask. The method developed by Zeng and coworkers was used to produce one gram nanowires per each synthesis. In this method CuNWs were grown by reducing copper II ions (i.e. complex with hydrated $Cu(NO_3)_2$) with hydrazine in an aqueous solution of NaOH containing ethylene diamine. Materials: Sodium hydroxide; Copper(II) nitrate $Cu(NO_3)_2$, ethylenediamine, anhydrous hydrazine 35 wt%. In each synthesis, we first prepared 1667 ml 15 M solution of NaOH by adding 1000 g NaOH pellets to DI water. The solution was gently mixed until NaOH pellets were completely dissolved in water and the solution became clear after nearly 30 minutes. This reaction generates a lot of heat and such, the solution was kept in cold water for a couple of hours to cool down. Then 100 ml copper nitrate (0.2 M) prepared in a separate beaker was added to the solution. The solution was then mixed for a few minutes and its color immediately turned to blue by the copper ions. Then 25 ml ethylene diamine (EDA) was added to the solution and mixed. Finally 1.7 ml hydrazine 35%, measured in a plastic syringe, was carefully added to the above solution. The solution was swirled after each addition for two minutes and then heated up to 80° C. The reaction was conducted for 60 minutes and the solution in the reaction flask was carefully stirred during the entire reaction time at ~1500 rpm by an impeller connected to a shaft driven by an electric motor. The blue color of solution due to the copper ions transformed to milky color after the addition of hydrazine. It then and turned to reddish brown as the reaction progressed, confirming the creation of copper nanoparticles and the creation of nanowires by the reduction of Cu^{2+} in the presence of hydrazine. The mechanism of chemical reaction for the synthesis of copper particles from copper nitrate can be summarized as follows [77] [78]:

$$2\,Cu^{2+} + 4\,NO_3^- + N_2H_4 + 4\,Na^+ + 4\,OH^- \xrightarrow[\substack{60\ \mathrm{min} \\ T=80\,^{\circ}C}]{} 2\,Cu + N_2 + 4\,H_2O + 4\,NaNO_3$$

The copper nuclides then started to grow axially in EDA resulting in long and thin nano-size CuNWs.

After the reaction was completed, the copper nanowires were collected from the top of the reactor and washed with a 3% hydrazine solution and then dispersed in a 3 wt% aqueous solution of hydrazine by vortexing. The synthesized CuNWs were then purified by centrifugation at 3000 rpm. After centrifugation, the nanowires were stored in the dilute 3 wt.% solution of hydrazine in water to minimize oxidation. Following synthesis, CuNWs were characterized by the scanning electron microscopy to examine their morphology and sizes. After completion of chemical synthesis, the electric conductivity of the nanowires were checked and short circuit signal for all the synthesized CuNWs confirmed their high conductivity. Figure 5-11 summarizes the synthesis and characterization process flow of the CuNWs.

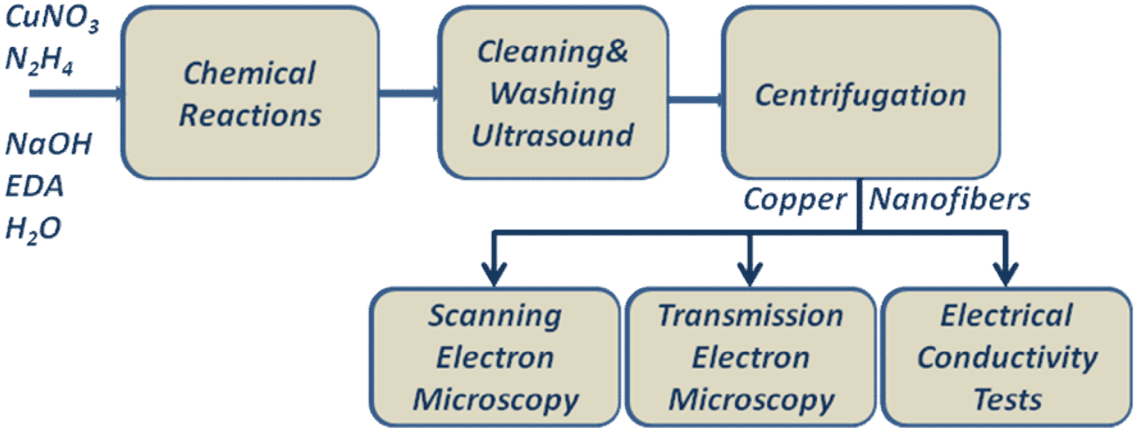


Figure 5-11: Schematic of the different steps of synthesis and characterization of copper nanowires.

5.2.3 Compounding of CuNWs and PMMA polymer

Suspensions of PMMA and CuNWs were prepared in the solution state using ultrasound and mechanical agitation under moderate to high shear. A 10 wt% solution of polymethyl-methacrylate (Rohm&Haas IRD-2) in acetone was first prepared. Then, the

CuNWs were compounded in the polymer solution using the mechanical stirrer at mixing speeds varying between 500 and 1500 rpm until a homogeneous suspension was obtained [79]. To exclude air and oxygen from the system, all preparatory mixing steps were conducted inside a glove box filled with argon gas.

To produce electric conductive films of CuNWs and synthetic polymers, the solution casting method was performed on the suspensions. Following mixing, the suspensions were placed in Petrie dishes to form CuNW/PMMA nanocomposite thin films. The films were allowed to dry for at least 24 h. To complete evaporation of solvent, the Petrie dishes were kept in an oven for 4 h at 50° C. The CuNW/PMMA films were then annealed in an oven for two hours at 100° C. Once the films were removed from the oven, they were gently peeled off the Petri dishes and stored at room temperature. The films had an average thickness of 300 μm.

5.2.4 Characterization Methods

To precisely determine the amount of CuNWs in the nanocomposite films, thermal gravimetry analysis (TGA Instrument model Q50) was performed by heating the sample from room temperature to 500 ^{o}C in a nitrogen environment at a rate of 20° C /min. Thermal decomposition of the polymer phase started at a temperature well above 200° C (~250° C) and completed at 450° C, while the nanowires remained intact during the experiment.

Surface resistivity of the nanocomposite films were measured using a four probe cell model Lucas Labs 302 connected to Keithly Precision current Source model 6220 and Keithly NanoVoltmeter model 2182A.

SEM images were obtained using a Hitachi S-4700 field emission scanning electron microscopy (FE-SEM). Transparency measurements of the films were carried out using a Varian Cary 5000 spectrophotometer with a baseline correction.

5.2.5 Results and Discussion

Figure 5-12 illustrates the scanning electron microscopy image of the copper nanowires.

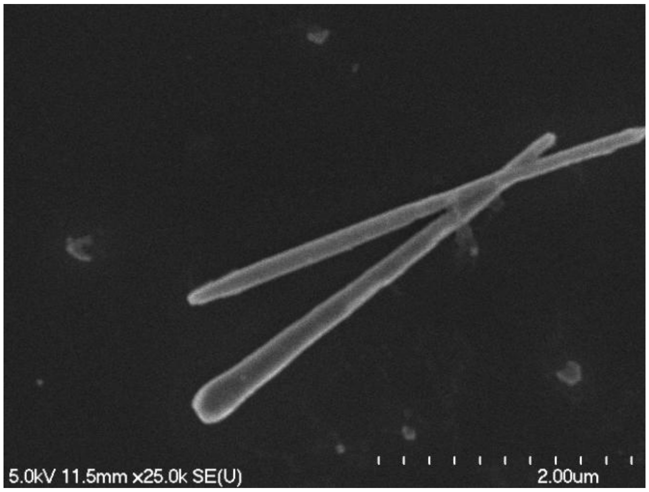


Figure 5-12: SEM image of the copper nanowires.

The diameter of the CuNWs was observed to be between 100 nm and 300 nm with 4-6 μm in length, resulting in aspect ratios of 30-60 (l/d). The more close up of the wires revealed spherical nanoparticles were attached to the nanowires. It appeared the nanowires grew from the spherical nanoparticles that had been generated earlier (initial nucleation stage).

In figure 5-13, we report surface resistivity results for the nanocomposite samples with various CuNWs contents. The PMMA has a very low electrical conductivity which is typical of thermoplastic materials. The PMMA resin used in this study had a surface resistivity of 1014 Ω/sq. With 7 wt% concentration of CuNWs, the measured surface resistivity of the nanocomposite thin film dropped to a low value of 6.6 Ω/sq.

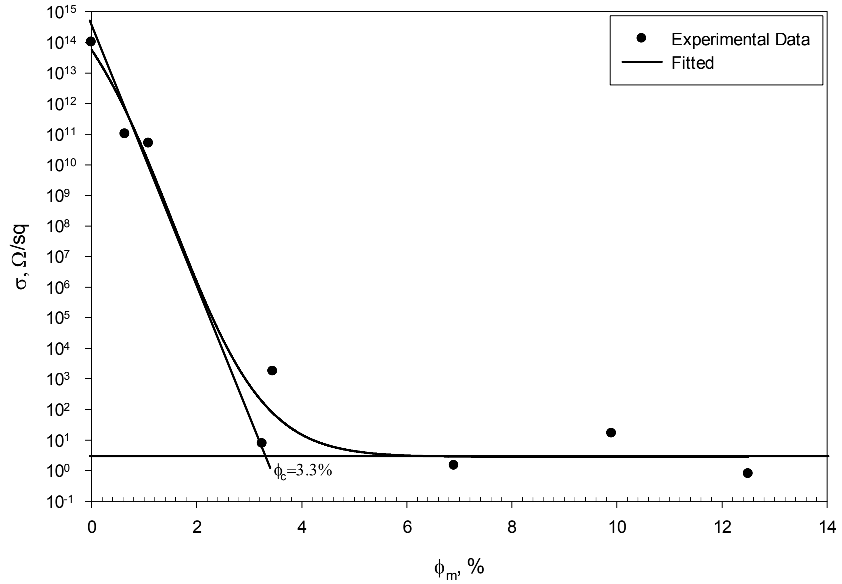


Figure 5-13: Master curve of surface resistivity vs. weight content of CUNWs for the nanocomposites.

Copper is one of the highest conductive materials and its volume conductivity is $5.9\text{x}10^7$ $(\Omega.\text{cm})^{-1}$. The nanocomposites exhibit conductivity somewhere between the polymer and copper metal. The copper nanowires synthesized in this investigation are expected to exhibit lower conductivity due to the crystalline nature of copper nanowires grown from the spheric copper crystals uniaxially [80]. The addition of a small amount of conductive nanowires dropped the measured resistivity values sharply. We note that surface resistivity of the nanocomposite at ϕ_m=1% (mass content of the CuNWs) was measured to be about 10^{11} Ω/sq, i.e. ~1000 times smaller than that of the pure polymer. Further increase of copper nanowire concentration enhanced electric conductivity of the CuNWs/PMMA films dramatically, until a concentration, called percolation, where the maximum conductivity is attained. Further addition of the conductive particles did not enhance the conductivity significantly. At the percolation concentration, the nanowires are believed to have formed a ubiquitous network of connecting wires, thus easily transferring electric charges along and across the sample. The number of conductive nano-sized fibers was sufficient to provide a three dimensional structure of contacting rods at any point. Figure 5-13 demonstrates that, at a copper nanowire content of 3.3 wt%, minimum resistivity was obtained. The resistivity started to level off at ϕ_m=3.3wt%. The corresponding volume content was ϕ_v= 0.44 vol% because of the large difference in the mass densities of the copper nanowires and that of the polymer (i.e. ρ_{copper}=8.96 and ρ_{PMMA}=1.2 g/cc). This confirmed that only half a percent in volume of the large aspect ratio conductive nano-particles was adequate to improve electric conductivity of the polymer required for most applications such as electromagnetic shielding in electronic devices.

Figure 5-14 illustrates the transparency measurement of both the PMMA and the CuNWS/PMMA thin films over the 300 – 800 nm spectrum range.

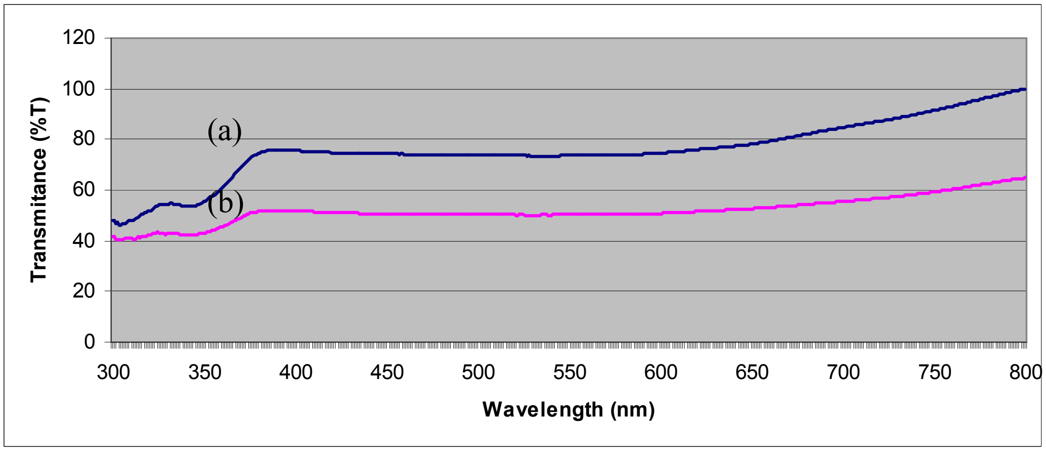


Figure 5-14: Transmittance (%T) of the (a) PMMA and (b) CuNW/PMMA conductive films, over the 300-800 nm spectrum range.

By comparing the PMMA thin film transparency in figure 5-14a with the combined CuNWs/PMMA transparency in figure 5-14b, a drop of about 25% can be observed. As a result, this work resulted in the fabrication of highly conductive film with acceptable transparency of about 55% for the photovoltaic applications.

5.2.6 Conclusion

A novel thermoplastic nanocomposite of CuNWs and PMMA was developed by solution mixing technique. Thin films of highly conductive nanocomposites were fabricated by solution casting. This investigation demonstrated that the addition of electric conductive nanoscale fibers to a polymer solution at low concentration levels of about 3.3 wt% (or 0.4 vol%) can transform the plastic to highly conductive phase while still maintaining a transparency of about 55%. By proper mixing conditions such as speed and time, the two phases are mixed together until a fine microstructure of the nanoparticles dispersed in the polymer is achieved with high conductivity and acceptable transparency.

6 Summary and conclusion

6.1 Overview

The main focus of this work has been to study and establish new fabrication methods for the components comprising the silicon-based solar cells in order to increase their efficiency, and at the same time, to lower their overall material and fabrication costs.

A new cost-effective and efficient approach was proposed for texturing the crystalline silicon using the gas lift effect (GLE). The advantages of this approach over the conventional ones are that significantly lower amounts of IPA are used and much shorter etching time is required to achieve the same reflectivity. The use of this new approach in surface texturing, allowed the reduction of the required IPA by 50% and etching time by more than 60% to achieve the same reflectivity. This can ultimately lead to a significant reduction in cost by increasing the efficiency of the texturing process.

Modeling and simulation techniques were used to understand the fluid flow patterns inside the silicon texturing system operating under GLE for solar cell applications. The simulation tool validated the correlation of the lower fluid velocity with the reduced surface coverage, uniformity and subsequently less optimal surface reflectivity. Various inlet designs were modeled and evaluated for optimal performance. The best case inlet design was fabricated and tested resulting in the validation of the simulation work and significant improvement in the GLE texturing system performance.

Two solar cell devices, one based on the novel GLE texturing approach, and the other based on the conventional method, were designed, fabricated and characterized. A significant improvement (more than 100%) was observed in the efficiency of the solar cell based on the GLE texturing approach. The application of the new GLE texturing approach results in considerable improvements in overall power efficiency of silicon solar cells without any additional increase to the production cost.

Two additional strategies were also studied to potentially further increase the efficiency and decrease the fabrication cost of such solar devices by integrating an array of micro-rod structures with nano-tip and a low cost conductive-transparent electrode, respectively. A new low-cost top-down multistage approach was introduced for the fabrication of arrays of silicon micro-rods with nano-tip and the growth mechanism of such structure was investigated. We also presented a method to synthesize thin and moderately to highly conductive nanocomposite films of copper nanowires (CuNWs) and poly-methyl methacrylate (PMMA) polymer with acceptable transparency to replace the much more expensive ITO. A fine microstructure of the nanoparticles dispersed in the polymer was achieved by appropriate mixing conditions, time and speed. Thin films were then fabricated using the low-cost solution casting.

Below, summaries of each 5 previous chapters are provided. Contributions of each chapter work are provided at the end of each summary.

6.2 Summary and contributions

6.2.1 Introduction (chapter 1)

This chapter established a motivation and an objective for this research work. It also provided a good background and literature review for the research focus area as well as definitions for some basic terms.

6.2.2 New Silicon Texturing Process Using the Gas-Lift Effect (chapter 2)

This chapter addressed the cost and efficiency of the anisotropic silicon texturing technique for the optoelectronic applications by introducing a novel method using the gas-lift effect (GLE) phenomenon. Anisotropic texturing uses a strong base such as KOH or TMAH and a surfactant such as IPA to achieve optimal surface coverage and uniformity. However, there is always a trade-off between the optimal texturing outcome and the etching rate. Adding more IPA will help with the texturing performance in terms of coverage and uniformity but will result in lower etching rates and smaller pyramid size (loss of size control). Experiments were carried out with various combinations of TMAH/IPA concentrations for two different GLE conditions to analyze and determine their influence on etching time, etching rate, surface morphology and reflectivity of the textured silicon surface. The use of this new approach in surface texturing, allowed the reduction of the required IPA by 50% and etching time by more than 60% to achieve the same reflectivity for optoelectronic applications. This can ultimately lead to a significant reduction in cost by increasing the efficiency of the texturing process. This new method also resulted in more control on the pyramid sizes generated as a result of less amount of IPA used during the texturing process. It is important to have as much control as possible on the particle size when it comes to MEMS and NEMS applications.

In the presence of GLE, the need for the use of a surface active agent, such as IPA, to help minimize the surface reflectance becomes much less critical allowing to achieve similar surface reflectivity values using considerably lower amounts of IPA at a much faster pace. The more IPA is used in the solution, the smaller the average size of the pyramids will be on the silicon surface. Therefore, the control over the pyramid size is lost or become very limited when IPA amount increases. Using GLE to compensate for the lack of IPA in the solution will provide us again with the control over the pyramid average size.

Although the presence of IPA is less critical to obtain low reflectance surfaces when GLE is used, it was concluded that a combination of IPA and GLE achieved the lowest reflectivity. Accordingly, a specular solar-weighted reflectance (SWR) of 0.15% was achieved with a combination of 3.5 %IPA and 2 mm GLE. The morphology of the surface was studied by performing image analysis of the SEM photos of the textured surface. The correlation between parameters such as surface coverage, uniformity and particle size with the reflectivity was studied and it was concluded that reflectivity is highly influenced by those parameters. A significant difference in average particle size results in a considerable change in surface reflectivity even at the same surface coverage. Lower reflectivity is a result of a combination of lower mean particle size as well as higher surface coverage and uniformity of the particles. As mentioned previously, the use of this new approach in surface texturing reduces the IPA and time required to reach the same reflectivity, and therefore, reducing the cost and increasing the efficiency of the texturing process both in terms of production cost as well as process productivity.

6.2.3 Modeling and Optimization of the new Texturing System (chapter 3)

This chapter addresses the optimization of the GLE texturing system for large-scale commercial applications. A modeling and simulation approach was used to understand the fluid flow patterns inside the silicon texturing system operating under GLE. Concurrent experimental work confirmed the validity of the simulation model and results.

It was determined that, due to the original non-optimal inlet, the fluid flow pattern and the non-uniform fluid velocity distribution inside the system resulted in the generation of lower velocity regions on the surface of the textured silicon.

The simulation tool validated the correlation of the lower fluid velocity with the reduced surface coverage, uniformity and subsequently less optimal surface reflectivity.

Various inlet designs were modeled and evaluated for optimal performance. The best case inlet design was fabricated and tested resulting in the validation of the simulation work and significant improvement in the GLE texturing system performance. In fact, with the new inlet design, the areas close to the inlet and the side walls (lower-velocity areas observed in the original inlet design) show morphology and surface reflectivity values very similar to those of the higher-velocity areas as the fluid velocity reaches and goes beyond the critical 0.047 m/s value.

Since the lower-velocity areas represented more than 15% of the total textured area in the case of the non optimal inlet design, the reduction and even elimination of these regions will be more critical in the scaled up process if the GLE approach is to be used as a viable alternative to the conventional texturing techniques at an industrial scale.

6.2.4 Improving the efficiency of silicon solar cells using the novel gas-lift effect texturing approach (chapter 4)

This chapter analyzes and validates the impact of applying the GLE texturing approach in the fabrication of solar cells. The efficiency of fabricated solar cell devices are compared with non-GLE textured solar cells fabricated under the same conditions and parameter values. In this study, the effect of the GLE-texturing approach on the I-V characteristics and the power efficiency of the fabricated solar cells were investigated.

The use of GLE effect during the texturing stage resulted in a textured surface presenting a much higher coverage and uniformity as well as a significantly higher surface area. The GLE-textured silicon surface also showed a much lower reflectivity (less than half) compared to the surface textured under the exact wet-etching conditions but with no GLE effect present.

I-V characterization of the solar cell devices fabricated with and without the GLE-textured silicon surfaces showed that the power efficiency of the device can be more than doubled as a result of using the GLE-textured surface. It is important to remember that this considerable improvement in overall power efficiency of silicon solar cells is achieved without the use of any additional reagents in the texturing process. Consequently, the use of GLE effect will contribute to significant improvement in the solar cell output power efficiency without increasing the production cost.

6.2.5 Further strategies for the optimization of the solar cell (chapter 5)

This chapter established two additional strategies, to potentially further increase the efficiency and decrease the fabrication cost of optoelectronic devices, by integrating an array of micro-rods with nano-tip and a low cost conductive-transparent electrode, respectively.

To tackle both the efficiency and cost issue, a new low-cost multistage approach was introduced for the fabrication of arrays of silicon micro-rods with nano-tip and the growth mechanism of such structure was investigated. A non-optimized non-GLE approach was used to investigate the effect of various TMAH/IPA combinations on the density and the morphology of the array.

In order to further address the overall material and fabrication cost of such solar cells, a low-cost fabrication technique was introduced to prepare transparent-conductive films to replace the much more expensive ITO layer. Transparent thin films of various thicknesses (i.e. 10 μm to 200 μm) with low single-digit surface resistivity were fabricated by the proposed low-cost method.

6.3 Future work

Many portions of this work may provide a good background for further efficiency and cost optimization study in the area of optoelectronic devices. The fabrication of the optimized solar cell device will require the integration of all the other optimized components, namely, the use of GLE texturing system, array of micro-rods with nano-tip, as well as the optimized low cost transparent conductive film.

6.3.1 Using the GLE texturing system

To further optimize the fabrication process, GLE texturing approach can be utilized for optimal surface coverage and reflectivity. This GLE-textured surface may then be used in subsequent fabrication stages to create the micro-structures with nano-tip with optimized surface uniformity and reflectivity. An important aspect to be considered in future work for the industrial application of GLE is the evaluation of the scale up process and the validation of the results at large scale. The experimental as well as the simulation model presented in this work have allowed the identification and evaluation of the critical parameters.

6.3.2 Creating the p-n junction inside the micro rods

By design and creation of the p-n junction inside the micro-rods (either axially or radially), one can achieve more carrier collection through less diffusion distance required for the carriers before they are collected. A more defined path is also available for the carriers to travel to the electrodes. This will further improve the efficiency of the solar cell devices.

6.3.3 Optimizing the conductive transparent film

Further optimization of the transparent conductive films fabrication method is needed to improve conductivity and transparency of such films. A few of such optimization techniques and recommendations are listed below:

- Modeling and simulating the random dispersion and orientations of the CuNWs in the polymer solution to better understand and estimate the CuNWs percolation concentration required to form the network of conducting CuNW mesh. This would be the optimal (or minimum) number of nanowires required to form this mesh and therefore achieving the highest transparency.
- Use of higher-grade PMMA to avoid CuNWs oxidation due to contact with impurities
- Take more effective precautions to protect CuNWs against sources of oxidation (oxygen and water) during the synthesis, storage as well as at the mixing stage with the polymer/solvent.

7 References

[1] J. MacKenzie, “Thinking Long Term: Confronting Global Climate Change”, World Resources Institute, http://powerpoints.wri.org/longterm/sld001.htm

[2] Deciding the future: Energy Policy Scenarios to 2050, Executive Summary, World Energy Council, 2007, http://www.worldenergy.org/documents/scenarios_study_es_online.pdf

[3] Nathan S. Lewis, “Report on the Basic Energy Sciences Workshop on Solar Energy Utilization”, Pasadena, CA, California Institute of technology, 2005

[4] J. Zhao, A. Wang, M.A. Green, F. Ferrazza, “19.8% efficient honeycomb textured multicrystalline and 24.4% monocrystalline silicon solar cells”, Appl. Phys. Lett. 73, pp 1991-1993, 1998

[5] W. Shockley, H.J. Queisser, “Detailed Balance Limit of Efficiency of p-n Junction Solar Cell”, J. Appl. Phys. 32, pp 510-519, 1961

[6] A. Marti, G.L. Araujo, “Limiting efficiencies for photovoltaic energy conversion in multigap systems”, Sol. Energy Mater. Sol. Cell 43, pp 203-222, 1996

[7] Luque, A., and Marti, A., “Increasing the efficiency of ideal solar cells by photon induced transitions at intermediate levels”, Phys. Rev. Lett. 78, 5014, 1997

[8] J. W. Leem, Y. M. Song, Y. T. Lee and J. S. Yu, “Effect of etching parameters on antireflection properties on Si subwavelength grating structures for solar cell applications”, Applied Physics B: Lasers and Optics 100, pp 891-896, 2010

[9] Lalanne P., and Hutley M. , “Artificial Media Optical Propertities-Subwavelength Scale”, Optical Engineering, Mercel Dekker, pp 62-71, 2003

[10] Merlos A., Acero M., Bao M. H., Bausells J. and Esteve J., “TMAH/IPA anisotropic etching characteristics”, Sensors and Actuators A 37-38, pp 737-743, 1993

[11] Vogt H, Kreysa G, “Electrochemical Reactors”, Ullmann's Encyclopedia of Industrial Chemistry, 2008

[12] Grotheer M P, “Electrochemical Processing, Inorganic”, Kirk-Othmer Encyclopedia of Chemical Technology 9 618-652, 2000

[13] Clint J. Novotny, Edward T. Yu, and K.L. Yu , “InP Nanowire/Polymer Hybrid Photodiode”, Nano Lett. 8 (3), pp 775-779, 2007

[14] G. E. Cirlin, A. D. Bouravleuv, I. P. Soshnikov, Yu. B. Samsonenko, V. G. Dubrovskii, E. M. Tanklevskaya, P. Werner, “Photovoltaic Properties of p-Doped GaAs

Nanowire Arrays Grown on n-Type GaAs(111)B Substrate” , Nanoscale Res Lett. 5 (2), pp 360-363, 2010

[15] Volker Schmidt, Heike Riel, Stephan Senz, “Realization of Silicon Nanowires Vertical Surround-Gate Field-Effect Transistor”, Small 2 (1), pp 85-88, 2006

[16] Loucas Tsakalakos, “Nanostructures for Photovoltaics” , Materials Science and Engineering R 62, pp175–189, 2008

[17] Green M. A., “Solar Cells: Operating Principles, Technology and System Application”, volume 1, University of New Wales, Kensington, 1982

[18] Papet P, Nichiporuk O, Fave A, Kaminski A, Bazer-Bachi B, Lemiti M, “TMAH texturisation and etching of interdigitated back-contact solar cells”, Materials Science 24, pp 1043-1049, 2006

[19] Zubel I, Barycka I, Kotowska K, Kramkowaska M, “Silicon anisotropic etching in alkaline solutions IV, The effect of organic and inorganic agents on silicon anisotropic etching process” Sensors and actuator A 87 163-171, 2001

[20] Zubel I, Kramkowska M, “The effect of isopropyl alcohol on etching rate and roughness of (100) Si surface etched in KOH and TMAH” solutions Sensors and actuator A 93, pp 138-147, 2001

[21] Ou Weiying, Zhang Yao, Li Hailing, Zhao Lei, Zhou Chunlan, Diao Hongwei , Liu Min, Lu Weiming, Zhang Jun and Wang Wenjing, “Texturization of mono-crtystalline silicon solar cells in TMAH without the addition of surfactant”, Journal of Semiconductors 31 106002, 2010

[22] Chii-Rong Yang, Po-Ying Chen, Cheng-Hao Yang, Yuang-Cherng Chiou, Rong-Tsong Lee “Effects of various ion-typed surfactants on silicon anisotropic etching properties in KOH and TMAH solutions” Sensors and Actuators A 119, pp 271-281, 2005

[23] Soonwoo kwon, Jongheop Yi, Sewang Yoon, Joon Sung Lee, Donghwan Kim, “Effects of textured morphology on the short circuit current of single crystalline silicon solar cells: Evaluation of alkaline wet-texture process” Current Applied Physics 9, pp 1310-1314, 2009

[24] Chii-Rong Yang, Chen-Hao Yang and Po-Ying Chen, “Study on anisotropic silicon etching characteristics in various surfactant-added tetramethyl ammonium hydroxide water solutions”, Journal of Microelectronics and Microengineering 15 2028-2037, 2005

[25] Chu A K, Wang J S, Tsai Z Y, Lee C K, “A simple and cost-effective approach for fabricating pyramids on crystalline silicon wafers”, Solar Energy Materials & Solar Cells 93 1276-1280, 2009

[26] MG Berger, Poröses Silicium für die Mikrooptik: Herstellung, Mikrostruktur und optische Eigenschaften von Einzelschichten und Schichtsystemen, PhD Thesis, Forschungszentrum Jühlich GmbH, 1996

[27] R. Herino, G. Bomchil, K. Barla, C. Bertrand, "Porosity and Pore Size Distributions of Porous Silicon Layers", J. Electrochem. Soc., Volume 134, Issue 8, pp. 1994-2000, 1987

[28] MG Berger, Poröses Silicium für die Mikrooptik: Herstellung, Mikrostruktur und optische Eigenschaften von Einzelschichten und Schichtsystemen, PhD Thesis, Forschungszentrum Jühlich GmbH, 1996

[29] Zhe Chuan Feng, Raphael Tsu, "Porous Silicon", World Scientific, 1994

[30] P. Bettotti, M. Cazzanelli, L. Dal Negro, B. Danese, Z. Gaburro, C. J. Oton, G. Vijaya Prakash and L. Pavesi, "Silicon nanostructures for photonics", J. Phys,: Condens. Matter 14, 8253-8281, 2002

[31] Xifré Pérez E., "Design, fabrication and characterization of porous silicon multilayer optical devices", PhD Thesis, 2007

[32] V Lehmann and U Gösele, "Porous silicon formation: a quantum wire effect", App Phys Lett, Vol 58, No 8, pp 856-858, 1991

[33] A. Uhlir, "Electrolytic Shaping of Germanium and Silicon", Bell Syst. Tech. J 35, pp 333-347, 1956

[34] Wisam J. Aziz, Asmiet Ramizy, K. Ibrahim, Z. Hassan, Khalid Omar , "The effect of anti-reflection coating of porous silicon on solar cells efficiency" , Optik 122, pp 1462– 1465, 2011

[35] R Mlcak, HL Tuller, P Greiff, J Sohn and L Niles, "Photoassisted electrochemical micromachining of silicon in HF electrolytes", Sensors and Actuators A, Vol 40, pp 49-55, 1994

[36] W Lang, P Steiner, U Schaber and A Richter, "A thin film bolometer using porous silicon technology", Sensors and Actuators A, Vol 43, pp 185-187, 1994

[37] Hamm D., Sakka T., Ogata Y. H., "Etching of porous silicon in basic solution", Applied Research, vol. 197 (1), pp 175-179, 2003

[38] Lalanne, P., and D. Lemercier., "On the effective medium theory of subwavelength periodic structures", J. Modern Optics 43, pp 2063-85, 1996

[39] Kanamori, Y., M. Sasaki, et al., "Broadband antireflectiongratings fabricated on Silicon substrate" Optics Lett. 24:1422, 1999

[40] A.M. Morales, C.M. Lieber, “A laser ablation method for the synthesis of crystalline semiconductor nanowires”, Science 279, pp 208-211, 1998

[41] R.S. Wagner, W.C. Ellis, “Vapor-liquid-solid mechanism of single crystal grown”, Appl. Phys. Lett. 4, 89, 1964

[42] B. Liu, H.C. Zeng, “Room temperature solution synthesis of monodispersed single-crystalline ZnO nanorods and derived hierarchical nanostructures”, Langmuir 20, pp 4196-4204, 2004

[43] T. Hanrath, B.A. Korgel, “Supercritical fluid-liquid-solid (SFLS) synthesis of Si and Ge nanowires seeded by colloidal metal nanocrystals”, Adv. Mater. 15, 437-440, 2003

[44] M.E. Toimil Molares, V. Buschmann, D. Dobrev, R. Neumann, R. Scholz, I.U. Schuchert, J. Vetter, “Single-crystalline copper nanowires produced by electrochemical deposition in polymeric ion track membranes”, Adv. Mater. 13, 62-65, 2001

[45] K.Q. Peng, Z.P. Huang, J. Zhu, “Fabrication of large-area silicon nanowire p-n junction diode arrays”, Adv. Mater. 16, 73-76, 2004

[46] N.A. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P.M. Petroff, J.R. Heath, “Ultra high density nanowire lattices and circuits”, Science 300, pp 112-115, 2003

[47] Tian B., Kempa T J, Lieber C M., “Single nanowire photovoltaics”, Chem Soc Rev 38 (1), pp 16-24, 2008

[48] L. Tsakalakos, J. Balch, J. Fronheiser, M.-Y. Shih, S.F. LeBoeuf, M. Pietrzykowski, P.J. Codella, B.A. Korevaar, O. Sulima, J. Rand, A.D. Kumar, U. Rapol, “Strong broadband optical absorption in silicon nanowire films”, J. Nanophoton. 01 013552, 2007

[49] L. Tsakalakos, R.J. Wojnarowski, A. Srivastava, C.S. Korman, J.U. Lee, S.F. LeBoeuf,A. Ebong, O. Sulima, “High efficiency inorganic nanorod enhanced photovoltaic devices”, (140342), US 2006/0207647

[50] B.M. Kayes, N.S. Lewis, H.A. Atwater, “Comparison of the device physics principles of plannar and radial p-n junction nanorod solar cells”, J. Appl. Phys. 97 114302, 2005

[51] K. Peng, Y. Xu, Y. Wu, Y. Yan, S.-T. Lee, J. Zhu, “Aligned single-crystalline Si nanowire arrays for photovoltaic applications”, Small 1, pp 1062-1067, 2005

[52] W.U. Huynh, J.J. Dittmer, A.P. Alivisatos, “Hybrid nanorod-polymer solar cells”, Science 29, 2425-2427, 2002

[53] Amouzgar M, Kahrizi M A new approach for improving the silicon texturing process using gas-lift effect *J. Phys. D: Appl. Phys.* **45** 105102 2012

[54] Comini G, del Giudice S A (k-epsilon) model of turbulent flow, *Numerical Heat Transfer* **8** 133-147 1985

[55] Tanner F X, Zhu G-S and Reitz R D 2001 A turbulence Dissipation Correction to the k-epsilon Model and Its Effect on Turbulence Length Scales in Engine Flows *International Multidimensional Engine Modeling User's Group Meeting at the SAE Congress Detroit*

[56] Harlow F H, Nakayama P I Transport of turbulence energy decay rate *Combust. Flame* **30** 45-319 1968

[57] Jones W P, Launder B E The prediction of laminarization with a two-equation model of turbulence *Int. J. Heat Mass Transfer* **15** 301-314 1972

[58] Launder B E, Spalding D B The numerical computation of turbulent flows *Comp. Methods in Appl. Mech. And Eng.,* **3** 269-89 1974

[59] Bardina J E, Huang P G, Coakley T J Turbulence Modeling Validation, Testing and Development *NASA Technical Memorandum* 110446 1997

[60] Launder B E, Sharma B I Application of energy dissipation model of turbulence to the calculation of flow near a spinning disc *Letters in Heat and Mass Transfer,* **1-2** 131-138 1974

[61] Amouzgar M, Kahrizi M Modeling and optimizing the gas-lift effect system for texturing J. Phys. D: Appl. Phys. 46 135107 2013

[62] W. Kern, Ed., Handbook of Semiconductor Cleaning Technology, Noyes Publishing: Park Ridge, NJ, 1993, Ch 1.

[63] T. Unagami, "Formation Mechanism of Porous Silicon Layer by Anodization in HF Solution," Journal of The Electrochemical Society, vol. 127, no. 2, pp. 476-483, 1980

[64] M. Christophersen, P. Merz, J. Quenzer, J. Carestensen, and H. Foll, "Deep electrocehmical trench etching with organic hydroflouric electrolytes," Sensors and Actuators A, vol. 88, no. 3, pp. 241-246, 2001

[65] H.W. Lau, G.J. Parker, and R. Greef, "High aspect ratio silicon pillars fabricated by electrochemical etching and," Thin Solid Films, vol. 276, no. 1, pp. 29-31, 1996

[66] P. Kleimanna, X. Badel and J. Linnros, "Toward the formation of three-dimensional nanostructures by electrochemical etching of silicon," Applied physics letters, vol. 86, no. 18, p. 183108, 2005

[67] G. Barillaroa, A. Nanninia, and M. Piotto, "Electrochemical etching in HF solution for silicon micromachining," Sensors and Actuators A, vol. 102, no. 1-2, pp. 195-201, 2002

[68] X. Li, H. S. Seo, H. D. Um, S. W. Jee, Y. W. Cho, B. Yoo, and J. H. Lee, "A periodic array of silicon pillars fabricated by photoelectrochemical etching," Electrochimica Acta, vol. 54, no. 27, p. 6978–6982, 2009

[69] J. E. A. M. van den Meerakker, R. J. G. Elfrink, W. M. Weeda, and F. Roozeboom, "Anodic silicon etching; the formation of uniform arrays of macropores or nanowires," physica status solidi (a), vol. 197, no. 1, pp. 57-60, 2003

[70] B. Yaghootkar, M. Amouzgar, and M. Kahrizi, "Fabrication of silicon micro-rod array with controlled density and size distribution using porous silicon," in 38th Annual Conference on IEEE Industrial Electronics Society (IECON), Montreal, 2012

[71] V. Lehmann and S. Rönnebeckb, "The Physics of Macropore Formation in Low-Doped p-Type Silicon," Journal of The Electrochemical Society, vol. 146, no. 8, pp. 2968-2975, 1999

[72] J. Rappich and H. J. Lewerenz, "In situ Fourier transform infrared investigation on the electrolytic hydrogenation of n-silicon (111)," Electrochemical Society, vol. 142, no. 4, pp. 1233-1237, 1995

[73] J. Rappich and H. J. Lewerenz, "In situ FTIR investigation of the electrochemical microstructuring of n-Si(111)," Electrochimica Acta, vol. 41, no. 5, pp. 675-680, 1996

[74] V. A. Burrows, Y. J. Chabal, G. S. Higashi, K. Raghavachari, and S. B. Christman, "Infrared sepectroscopy of Si(111) surface after HF treatment: Hydrogen termination and surface morphology," Applied physics letter, vol. 53, no. 11, p. 998, 1988

[75] H. Ubara, T. Imura, and A. Hiraki, "Formation of Si–H bonds on the surface of microcrystalline silicon," Solid State Communications, vol. 50, no. 7, p. 673, 1984

[76] A Bunde, W Dieterich, "Percolation in Composites", Journal of Electroceramics 5:2, 81-92, 2000

[77] Rathmell, Aaron R. ; Bergin, Stephen M.; Hua, YiLei; Li, Zhi-Yuan; Wiley, Benjamin J., The growth mechanism of copper nanowires and their properties in flexible, transparent conducting films, Advanced Materials, v 22, n 32, p 3558-3563, 2010

[78] L Yang, T Zhang, H Zhou, S Price, B Wiley, W You, “Solution-processed flexible polymer solar cells with silver nanowire electrodes, ACS Applied Materials and Interfaces, v 3, n 10, p 4075-4084, 2011

[79] M Rajabian et al, “Shearing and mixing effects on synthesis and properties of organoclays/poleyter nanocomposites, Rheologica Acta, v 51, n 11, p 1007-1019, 2012

[80] A G Gelves, M H Al-Saleh, U Sundararaj, “Highly conductive and high performance EMI shielding nan-wire/polymer nanocomposites by miscible mixing and precipitation” Journal of Materials Chemistry, v 21, n 3, p 829-836, 2011