A VARIABLE BANDWIDTH, POWER-SCALABLE OPTICAL RECEIVER FRONT-END

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ABSTRACT

A Variable Bandwidth, Power-Scalable Optical Receiver Front-End

Partha Protim Dash

The tremendous growth in internet data traffic and computation power has increased demand for high-speed links in almost all communication systems. Normally, high-speed interconnects in a super computer are implemented using a short distance electrical medium such as a printed circuit board or coaxial cable. However, data transmission through an electrical medium suffers severe bandwidth limitation due to its distributed resistance, inductance and capacitance. To overcome this problem, several equalization techniques are adopted which can make the system more complex and power hungry. An efficient way to enhance the capacity of short-reach link is through the use of an optical channel rather than the band-limited electrical one.

The analog front-end is the most important building block of the optical receiver as it converts the small current generated by the photodiode to a significant voltage level. In this work, we present an inductor-less, variable bandwidth, power-scalable optical receiver front-end in TSMC 65nm and 90nm CMOS with two different topologies. The front-end contains a transimpedance amplifier (TIA) and post amplifiers (PA) in 90 nm CMOS (Design 1) whereas in 65 nm CMOS (Design 2) an offset compensation block and a transconductor is incorporated to improve the robustness of the overall receiver front-end.The transimpedance amplifier in both designs is implemented with the shunt feedback topology and the post amplifiers in 90 nm and 65 nm design use the common source topology loaded with modified active inductors and the Cherry-Hooper inverter

based topology, respectively. In order to make the receiver front-end power and bandwidth scalable, a current controlling PMOS array and a tuneable resistive bank is implemented in both designs. The Design 1 is able to vary the supported data rate from 1.25 Gb/s to 15 Gb/s. The gain at each data rate is ~ 84 dBΩ. The overall power dissipation varies from 0.94 mW to 7.46 mW as the data rate scales, maintaining an energy per bit lower than 800 fJ at all data rates using a 1.2 V power supply. The input referred noise density varies from 4.31 pA/√Hz to 14.27 pA/√Hz. In the Design 2, the receiver front-end can be tuned from 1.25 Gb/s to 20 Gb/s maintaining a fixed gain of ~75 dBΩ. The power dissipation in this case varies from 0.32 mW to 13.5 mW as the data rate scales up, maintaining energy per bit less than 700 fJ using a 1 V power supply. The input referred noise density varies from 8.46 pA/√Hz to 18 pA/√Hz. Simulation shows that Design 1 is not robust enough against the mismatch and global process variations whereas Design 2 is much more robust against these effects.

This type of front-end has applications in links that vary data rate in response to system requirements. Additionally, the lowest data rate can be act as an idle mode which receives data used only to maintain transmitter and receiver synchronization.

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1. List of Tables

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3. List of Acronyms

TIA	Transimpedance Amplifier
PA	Post-Amplifier
LPF	Low Pass Filter
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
XOR	Exclusive OR (logic gate)
UI	Unit Interval
NMOS	N-Channel MOSFET
PMOS	P-Channel MOSFET
CMOS	Complementary MOSFET
CS Amplifier	Common-Source Amplifier
KCL	Kirchhoff's Current Law
PD	Photodetector
PSD	Power Spectral Density
PWL	Piecewise Linear

Chapter 1

1. Preface

1.1 Motivation

Increasing demand for high capacity interconnects makes optical links appropriate not only in long-haul telecom networks but also in short-reach links such as those within data centers, chip-to-chip interconnections etc. The use of optical links instead of electrical links in short-reach applications enables lower latency (less circuit complexity owing to not having any equalization technique or repeaters) and greater scalability in terms of data rate per channel, length of link, and total number of available channels. In order to have higher performance for short-reach links, some additional design goals have to be achieved along with higher data rate. These goals include power efficiency, small footprint for the transmitter and receiver circuits, low-cost implementation and tight integration with optical interconnects [1, 2].

In the majority of computation platforms, limited interconnect capacity is a bottleneck for the system's performance, and hence, increasing per-link data rate is always a design goal. However, even when a compute application's speed is limited by interconnection speed, links are not necessarily all being maximally used. Any link that is not maximally used will still dissipate power, unless it is disabled. Recently, power savings and performance penalties associated with scaling back the speed and power of links within a network have been investigated [3]. The maximum energy savings are

achieved when links can rapidly be configured to operate at the minimum data rate required by the application and with the minimum power dissipation. In order to save energy without incurring a performance penalty, links must be capable of rapidly transitioning back to the higher data rate mode. Figure 1.1 illustrates well the energy savings for data rates change. In Figure 1.1, the green line indicates arbitrary required data rate as a function of time. A receiver designed to operate at a certain data rate will dissipate a fixed power shown by the blue line, resulting in wasted energy if the maximum data rate is not required. An energy efficient design will have the ability to reduce power dissipation when the required data rate is reduced. In this figure, proportional power dissipation with respect to the data rate is shown by the red line. As shown in this thesis in Chapter 4 the receiver front-end of a link operated at 20 Gb/s takes approximately 35 to 40 times more power than 1.25 Gb/s operation. Therefore, when the maximum data rate is not required a variable-rate link can save up to ~ 97.5 % of power by operating the link at 1.25 Gb/s. This savings can be even larger if a high speed (e.g. 40 Gb/s) link is used and data rate can be scaled down below 1.25Gb/s.

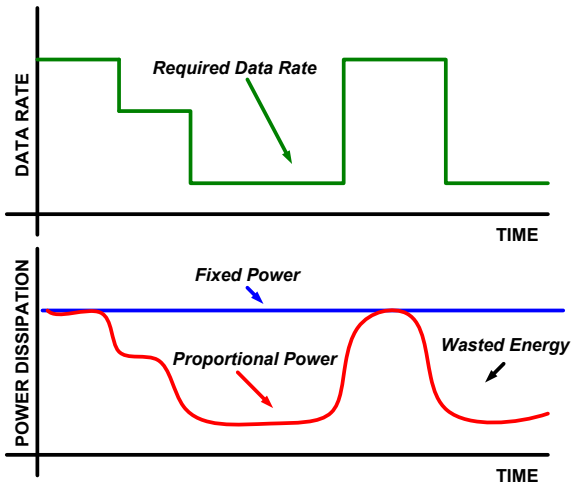

Figure 1.1: Example of an energy efficient short-reach link [4].

1.2 Optical Communication System

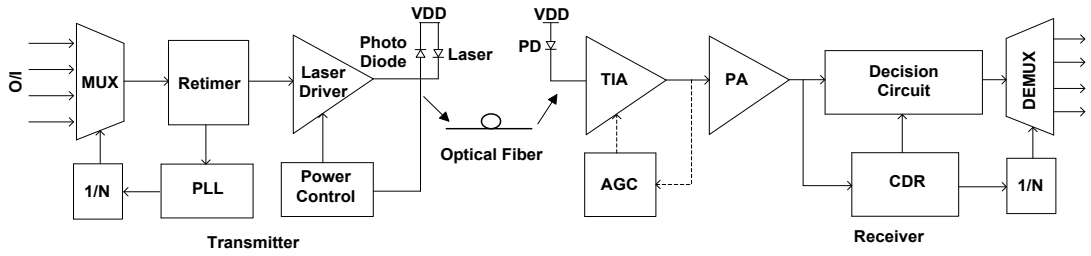

Figure 1.2: Overall optical communication system [5].

Figure 1.2 represents a conventional digital network [5] of an optical communication system. It consists of a transmitter and receiver circuit. In the transmission side, a number of inputs will be multiplexed into a high-speed data stream. This high-speed data stream is then applied to the laser driver via a retimer. In some applications, a power control circuit will adjust the power of the laser driver. A PLL is employed to clock both the retimer and the multiplexer [5].

In the receiver side, the optical light will be converted into a current signal by the photo detector (PD). The TIA then converts this current to a voltage signal. As TIA is the 1st stage of amplification, it should provide high sensitivity. In order to have sufficient bandwidth, the gain of the TIA is usually not high enough to allow direct connection of the TIA to a decision circuit. Therefore, post-amplifiers (PA) usually follow the TIA to amplify its output signal. The post-amplifier's output is finally fed into the de-multiplexer via a decision circuit in order to reproduce the original data stream. A CDR circuit executes amplitude-level decisions on the incoming signal and provides a clock for both the decision circuit and the de-multiplexer, which eventually leads to a time, and amplitude reinforced data stream [5].

1.3 Thesis Objectives

The optical receiver front-end plays a significant role in the design of a receiver chain. The main objective of this thesis is to demonstrate a variable-bandwidth, power-scalable optical receiver front-end in CMOS technology. The following were targeted specifications:

- A range of bandwidth of at least 10x
- A maximum bandwidth ≥15 Gb/s
- Power dissipation that decreases proportionally as data rate is reduced
- Maximum power dissipation of less than 15 mW.

1.4 Thesis Contribution

This work presents a novel tunable optical receiver front-end with power and bandwidth scalability. The main contributions of this thesis are:

- A modified circuit for implementing the tunable TIA and post amplifier.
- Implementation of the architecture in an integrated circuit using TSMC 65nm (Design 2) technology.
- Robustness issue of Design 1 is addressed and solved in Design 2 by employing an offset compensation scheme.
- Design 1 and Design 2 has been presented at *ISCAS 2013* and *MWSCAS 2013* conference, respectively. The paper titles are:

- P. P. Dash, O. Liboiron-Ladouceur, G. Cowan "Inductorless, Power-Proportional, Optical Receiver Front - End in TSMC 90nm "*IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 1127-1130, May 2013.
- P. P. Dash, O. Liboiron-Ladouceur, G. Cowan "A Variable-Bandwidth, Power-scalable, Optical Receiver Front-End in 65nm" *IEEE Midwest Symposium on Circuits and System (MWSCAS),* 2013 (Accepted).

1.5 Thesis Organization

The thesis has a total of five chapters. Chapter 2 is a literature review, where various front-end topologies are discussed. In Chapter 3, the design of the overall receiver chain is discussed, which includes the design and analysis of the TIA, post-amplifiers and the offset-compensation loop. Simulation and parasitic-extracted results are shown in Chapter 4. Finally, conclusions and future works are presented in Chapter 5.

Chapter 2

2. Literature Review & Background

2.1 Literature Review

The two integral parts of an optical receiver front-end are a TIA and a post amplifier. Light traveling through an optical fibre may suffer significant attenuation before reaching the photodetector, therefore the front-end requires a highly sensitive receiver to detect the signal and process it further. A significant amount of research has been conducted in the field of analog front-end design. Only a few will be presented in the next part of this chapter, with primary interest in designs using CMOS technology.

2.1.1 Transimpedance Amplifiers (TIA)

Normally, TIA receives a photocurrent generated by a photodiode at its input and converts that current to voltage with a modest amount of gain. A literature review of the TIA used in several optical receiver front-end designs will be discussed in this section.

2.1.2 Common-Source (CS) Shunt Feedback TIA

Common-source (CS) shunt feedback amplifiers have been widely used in TIA design [5], where the output is fed back to the input via a resistive network shown in Figure 2.1. The significant advantage of this topology is its low noise. With a fixed load resistance (R_L), its noise is inversely proportional to the transconductance (g_m) of CMOS transistor M_1. Therefore, the noise performance can be improved by increasing the g_m.

However, a drawback of this topology is the large input capacitance C_{in} which includes the gate-source capacitance C_{GS}, the miller-amplified gate-drain capacitance C_M and parasitic photodiode capacitance $C_{PD.}$ This input capacitance C_{in} eventually forms a dominant pole at the input node, which limits the bandwidth. In this figure, R_L is the load resistance, R_F is the feedback resistance, C_L is the load capacitance, V_{out} is the output voltage and I_{pd} is the photodiode current.

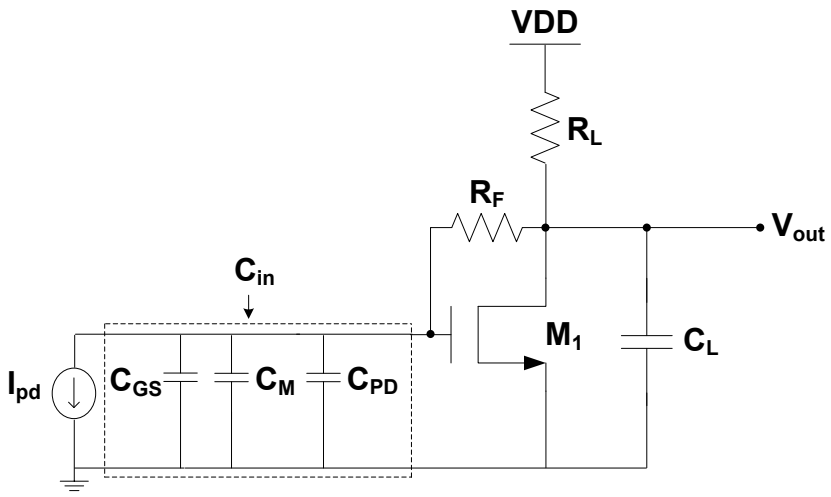

Figure 2.1: Common-source shunt feedback TIA [5].

2.1.3 Common-Gate TIA

The common-gate (CG) TIA is one of the most popular topologies due to its low input impedance as shown in Figure 2.2. But the main drawback of this topology is having a trade-off among noise, bandwidth and the supply voltage. At high frequency, this circuit shows 2 poles which are at the input and output. Because of the photodiode capacitance, the input pole dominates. The magnitude of the input pole can be increased by increasing the transconductance (g_m) of CMOS transistor M_1. This can be achieved by

increasing the bias current or by increasing the width of M_1. However, if the width is increased, the gate-source capacitance (C_{GS}) of M_1 will increase more than the g_m, ultimately limiting the bandwidth. On the other hand, increasing the bias current requires greater supply voltage due to the increased voltage drop across R_D, V_{GS1} (gate-source voltage of M_1) and V_{DS2} (drain-source voltage of M_2). If R_D is decreased to allow greater bias current, the TIA gain goes down which eventually leads to a higher noise current. Therefore, it becomes difficult to design a high gain broadband TIA with lower supply voltage [5].

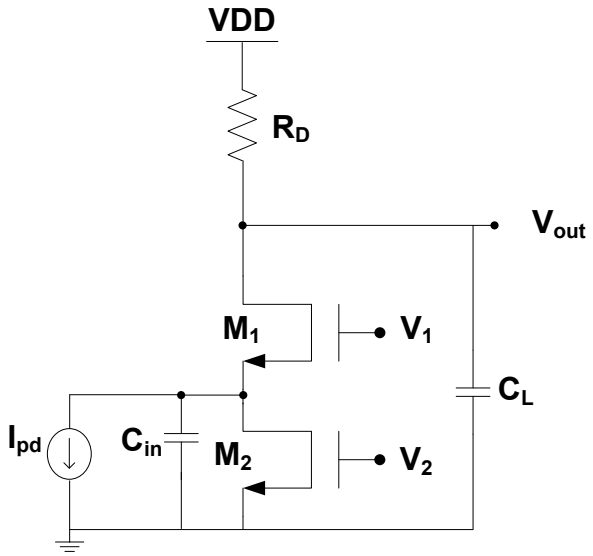

Figure 2.2: Common gate TIA [5].

2.1.4 Regulated Cascode (RGC) TIA

Recently, the regulated cascode (RGC) topology as shown in Figure 2.3 has become more popular. It employs a CG amplifier with local feedback that reduces the

input impedance by the feedback gain [6]. The RGC topology enhances the input transconductance which increases the overall bandwidth.

The two main drawbacks of the conventional RGC topology are as follows:

- The local feedback may introduce peaking in the frequency response, which may distort the output voltage swing in the time domain.
- The conventional RGC suffers from a voltage headroom problem if it is biased from a small power supply, which prevents it from operating at high speed. As an example, from ground to V_y it needs two V_{GS} drop ($V_y = V_{GS3} + V_{GS1}$), which is too high for small supply voltage.

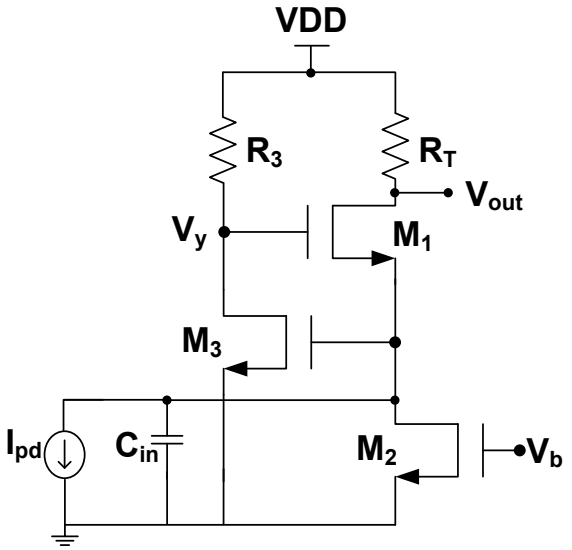

Figure 2.3: Regulated cascode (RGC) TIA [6].

2.1.5 Burst-Mode Receivers

Burst-mode optical receivers (BMR) are mainly used to handle input signals whose amplitude may vary extensively from burst to burst such as in passive optical

networks (PON). These input signals are not dc balanced, thereby requiring a good offset control mechanism. On the other hand, the receiver needs to respond as soon as possible to the incoming asynchronous burst with varying power levels. An adaptive TIA having an automatic gain controller (AGC) circuit with a good offset control mechanism is capable of handling the different bursts of data. Figure 2.4 shows a differential burst-mode TIA with an AGC and adaptive threshold control (ATC) mechanism where the ATC circuit eliminates the output offset voltage on a burst-by-burst basis [7]. Recently, the PON systems are aiming at high speed data transmission efficiency by reducing the receiver response time that is needed for the receiver amplitude recovery in burst-mode. For the 10.3125 Gb/s datarate the necessary response time for the burt mode receiver front-end should be < 800 ns according to the IEEE 802.3av [8]. Although the recent works in this field show the improvement in the response time at higher data rate, but the energy saving is not improved that much. A recently designed burst-mode front-end [9] operated at 10Gb/s consumes ~ 200mW and ~ 430mW power, respectively at 2.5V and 2.2V with 75 ns response time. Another work shows a 10.3 Gb/s burst-mode PIN-TIA [10] design with a small response time ~10ns but the overall power dissipation is ~ 180mV at 3.3 V supply. The proposed front-end designed in this thesis aims to have a lower response time with maximum energy savings.

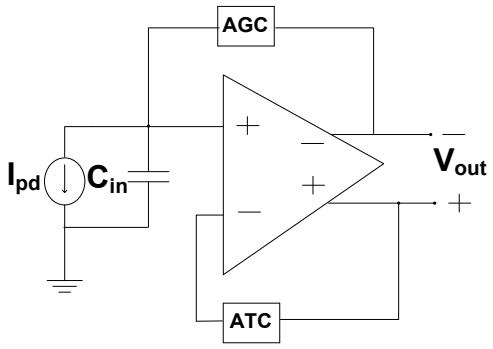

Figure 2.4: Differential burst-mode TIA [7].

2.2 Post-Amplifiers

The design of the post-amplifier typically involves several cascaded gain stages that can produce a large output swing to be applied to the decision circuit. Possible implementation techniques involve cascaded differential pairs, Cherry-Hooper amplifiers, or inverter-based Cherry-Hooper amplifiers.

2.2.1 Cherry-Hooper Amplifier

The Cherry-Hooper (CH) amplifier topology as shown in Figure 2.5 has been widely used for post-amplifier designs. The operation of a CH amplifier is as follows. The amplifier employs local feedback from drain to gate of a CMOS transistor (M_3) to create a high-frequency pole, which results in a bandwidth extension. The major disadvantage of the CH amplifier is that it is power hungry and creates a voltage headroom problem when powered with small supply. Based on the application, a CH amplifier can be single ended or differential [5].

The single ended CH amplifier may suffer from power supply noise and substrate noise. A regulated power supply can reduce this noise. Alternatively, differential pairs can be used to reduce this supply noise. However, the main advantage of using the single-ended amplifier is that it consumes less power than the differential one. The post-amplifier normally employs feedback networks to remove DC offsets due to device mismatch. Figure 2.5 shows the single-ended CH amplifier on the left and the differential CH amplifier to the right.

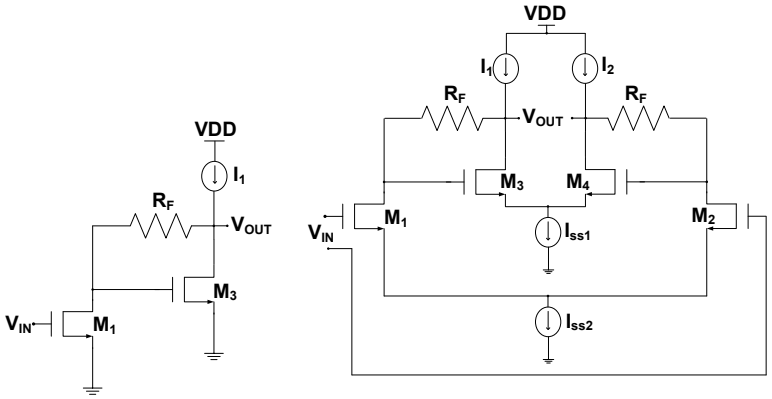

Figure 2.5: Single ended (left) and differential CH amplifier (right) [5].

2.3 Background

In this section a small amount of background information will be presented to help the reader to understand some technical terms that will later be used in the thesis.

2.3.1 Gain-Bandwidth Product

The gain-bandwidth product of an amplifier is defined as the product of a amplifier's low frequency gain (A_{DC}) and its -3dB bandwidth (f_{-3db}). Normally, it is

denoted as GBW. Figure 2.6 shows a typical common source single stage amplifier and its gain bandwidth plot.

$$GBW = f_{-3dB} * A_{DC}$$

$$f_{-3dB} = \frac{1}{2\pi R_L C_{out}}$$

$$GBW = \frac{1}{2\pi R_L C_{out}} * A_{DC}$$

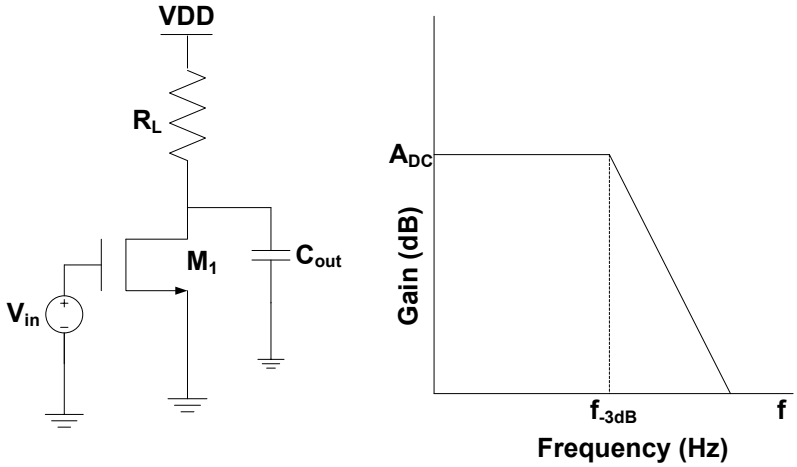

Figure 2.6: CS amplifier with its gain bandwidth plot.

2.3.2 Photodiodes

Photodiodes have p-n junction structures where photons (light) cause the generation of carriers and holes by the internal photoelectric effect. When the photodiodes are reversed biased, these carriers give rise to an electric current due to the presence of an electric field. The generated current is proportional to the incident light. This current is used as input of the optical receiver front end. The photodiode shows a large parasitic capacitance at the input of the receiver front end, which may degrade the

overall performance of the receiver [5]. Therefore, in the design of an optical receiver front-end the photodiode capacitance must be taken into account.

Normally the current generated by a photodiode (I_p) is proportional to the optical power [5]

$$I_p = R_{ph} * P_{op} ,$$

where, R_{ph} is known as "responsivity". For a short-reach optical system the expected optical power signal is ~ -10 dBm and for a PIN diode responsitivity is ~ 0.8 A/Watt. Therefore, the input current generated by the photodiode is ~ 80μA.

2.3.3 Eye Diagram

A data stream can be checked by observing every sequence of bit. However, this will be a tedious job. A common tool for observing any non-ideal phenomena in the data stream is the "eye-diagram". This diagram folds all of the bits into a short interval [5]. Figure 2.7 shows the eye diagram formation from a random binary bit sequence.

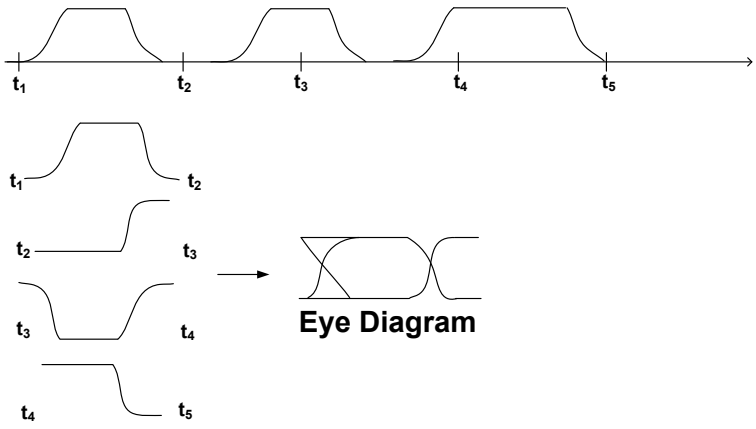

Figure 2.7: Eye diagram formation from random bits [5]

2.4 Conclusion

Different topologies of the optical receiver front-end operated at fixed data rates have been discussed in this Chapter. A small background study is also presented for further understanding. Various design trade-offs have also been considered according to the system requirements. Depending on the configuration used, a design of a low power, high speed and power- scalable CMOS optical receiver front-end can be realized.

Chapter 3

3. Optical Receiver Front-End Design

3.1 Overview of the Optical Receiver

An optical receiver consists of several stages each with their individual functionality [5].

- Transimpedance Amplifier: Its main function is to convert the current to voltage.
- Post-Amplifiers: Amplify the signal for the decision circuits.
- Decision Circuits: Flip-flops for resolving the signal to full-rail logic levels.
- Clock recovery: Recovers clock signal from the input data and helps the decision circuits to sample the data in the middle of each bit.
- De-multiplexer: Reproduces the original parallel data stream from the decision circuit's output.

3.2 Front-End Design Considerations

Generally, input pole of a TIA becomes the dominant pole due to large photodiode capacitance. As a preamplifier, TIA converts the input current to voltage. Normally, the input current of a TIA is small therefore a high gain is required to suppress the noise of the overall receiver. However, high gain can limit the circuit speed due to the gain bandwidth trade-off.

3.2.1 Performance Criteria for a Front-End Design

In order to design an analog front-end, certain design trade-offs should be kept in mind. The design trade-offs are as follows:

- **Noise and Bit Error Rate (BER)**

  Transimpedance amplifiers are typically designed with low noise figures, especially when there is a cascade of gain stages. Normally the TIA noise dominates the overall noise performance as the later stages' noise contribution is cut down by the gain preceding the stages [5].

  Bit error rate is defined as the number of errors divided by the number of received bits. Therefore, if BER is small then the noise of the front-end is small. For an optical system, a BER < 10^{-12} is considered as an error free system. Typically for a receiver design, the ratio of the peak to peak current (I_{p-p}) of a noiseless input and the input referred noise current ($I_{n,\ in}$) should be at least 14 in order to get a BER = 10^{-12} [5].

- **Intersymbol Interference**

  Intersymbol interference (ISI) refers to when the signal of one bit interval affects the signal of a previous or later bit interval. It occurs when the receiver bandwidth is smaller than approximately 70% of the data rate. ISI reduces the output signal swing. Severe ISI can occur when the receiver front-end receives a 1 after a long string of 0s if the bandwidth is not sufficient. Moreover, ISI generated from the offset compensation low pass filter leads to a wandering DC level, which in turn affects the decision threshold of the receiver. ISI also plays an important role in determining the consecutive identical digit (CID) immunity of the receiver.

Consecutive identical digits immunity refers to the number of identical bits that can be received before the DC wandering will cause an error on the next received bit [5].

- **Bandwidth**

  The bandwidth of a TIA is normally chosen between 0.5 - 0.7 of the data rate. This is the typical range of the bandwidth of the optical receiver. A bandwidth chosen to be greater than 0.7 of the data rate causes the integrated noise of the receiver to increase which in turn increases the input referred noise and BER. On the other hand if the bandwidth is less than this range then the receiver output data may suffer large amount of ISI [5].

- **Gain**

  The gain of a TIA cannot be too high or too low. If the gain becomes too high it may affect the circuit bandwidth which prevents the circuit from operating at high speed. On the other hand, a gain which is too low worsens the noise performance of the overall receiver [5].

- **Overload**

  Overload at the input of the TIA may cause the bias point to shift, causing the response time to become slow. The overall performance may get affected if the amount of current fed through to the input becomes large. This problem can be solved if the receiver integrates an automatic gain control circuit, which may increase complexity in the receiver design [5].

- **Baseline Wander:**

  Baseline wander is the variation of the average midpoint of the output NRZ data from a receiver shown in Figure 3.1. This problem may occur if the time constant of the low pass filter incorporated in the offset compensation block is less than the time duration of consecutive identical digits [5].

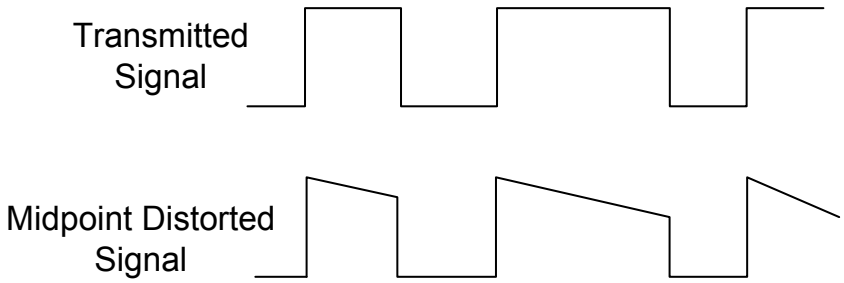

Figure 3.1: Baseline Wander or DC Wander [5].

3.3 Design Goals

Originally, it was decided that the receiver front-end will be taped out at 90 nm CMOS technology, but it was not possible as CMC Microsystems stopped offering 90 nm CMOS design fabrication at the end of 2012. 65 nm CMOS was therefore alternatively chosen for the final design. This thesis consequently characterizes solutions in 2 different technologies.

- Design 1: Only schematic representation of the receiver front-end is given.
- Design 2: Taped out in 65nm CMOS. Simulated and parasitic extracted result of the receiver front-end is presented in the thesis.

Design 1 was the first attempt of designing a variable-bandwidth, power- scalable optical receiver front-end. It had some problems which will be discussed later. Design 2 happened to be in a different technology (65nm CMOS) but more importantly addressed some of the problems of Design 1. According to the state of art, Table 3.1 and 3.2 show the design goals of Design 1 and Design 2, respectively.

Table 3.1: Goals (Design 1)

Supply Voltage	1.2
Target gain	$\geq$ 80 dBΩ
Data rate tuning	1.25 Gb/s to 15 Gb/s
Bandwidth	50 % to 70 % of each data rate
Power Dissipation	$\leq$ 20 mW and scalable with data rates
Response time for reconfiguration	as small as possible (e.g. < 800 ns [8])

Table 3.2: Goals (Design 2)

Supply Voltage	1 V
Target gain	$\geq$ 70 dBΩ
Data rate tuning	1.25 Gb/s to 20 Gb/s
Bandwidth	50 % to 70 % of each data rate
Power Dissipation	$\leq$ 20mW and scalable with data rates
Response time for reconfiguration	as small as possible (with offset compensation enable)

As no bandwidth extension method is applied in the Design 2 and operation of the receiver at high speed (20 Gb/s) is needed, the targeted gain specification has been reduced so that the gain bandwidth trade off does not obstruct the circuit operation.

3.4 Conventional & Proposed Front-End Architectures

Figure 3.2 shows the conventional front-end architecture [5] where TIA, post-amplifiers and offset compensation blocks are presented with an on-chip load (decision circuits). The overall front-end is biased through a fixed supply voltage (VDD).

The proposed front-end architecture in Design 1 and Design 2 are shown in Figure 3.3 and Figure 3.4, respectively. In the proposed Design 1 architecture, the TIA is biased through a digitally controlled resistance, whereas the post amplifiers are biased through an adjustable voltage source. In order to have small response time for data-rate reconfiguration, this design does not incorporate any offset compensation block.

Design 2 incorporates a TIA, post-amplifiers, offset compensation blocks and an input transconductance to bias the TIA with the compensated current. All of the blocks are biased through the digitally controlled resistance. The offset-compensation incorporates an active low pass filter to obtain an improved response time.

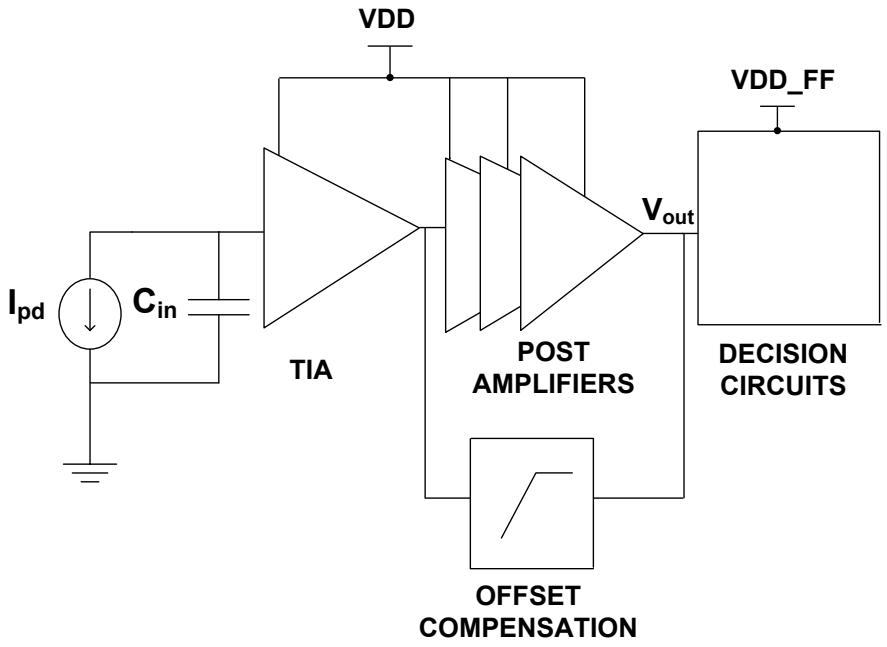

Figure 3.2: Conventional front-end architecture [5].

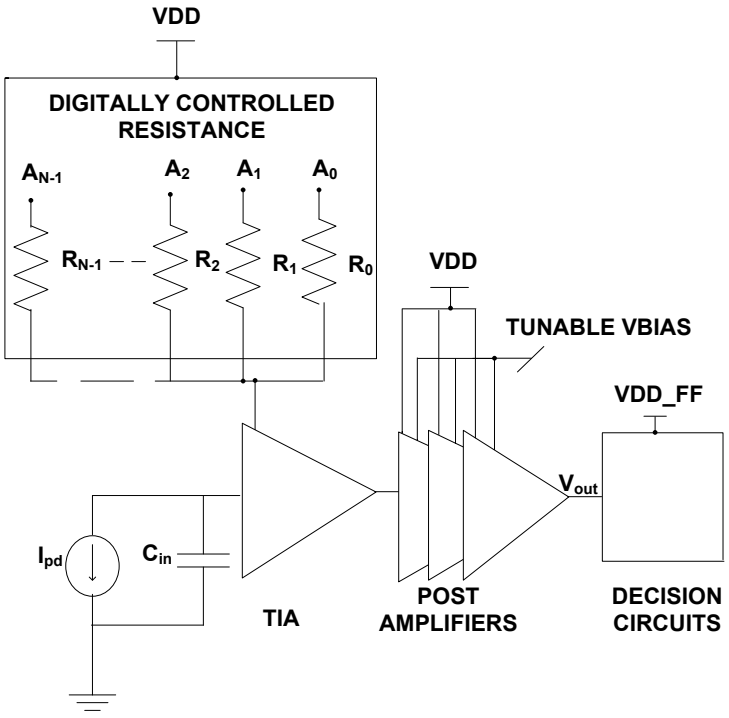

Figure 3.3: Proposed front-end architecture in Design 1.

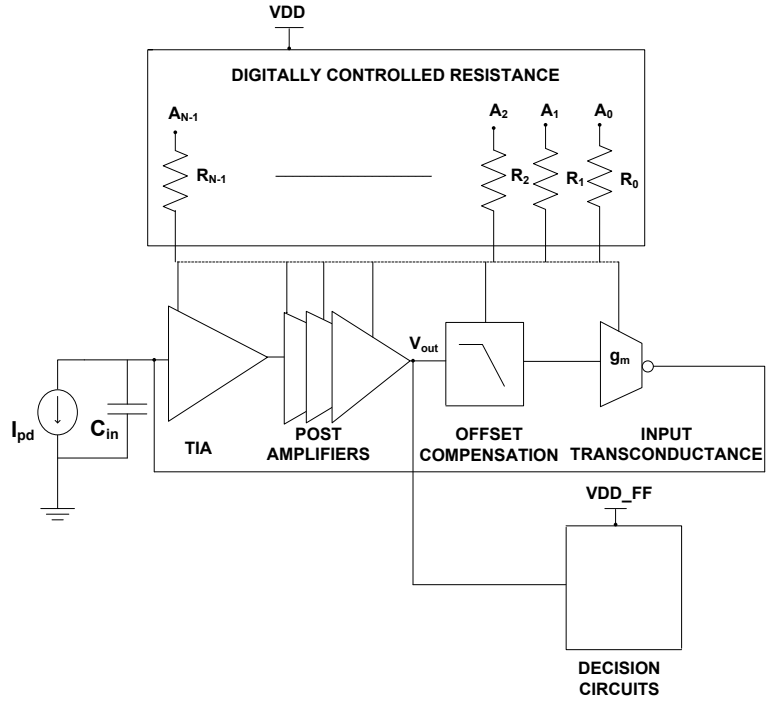

Figure 3.4: Proposed front-end architecture in Design 2.

3.5 Transimpedance Amplifier (TIA) Design

In this work, tunable receiver front-ends are implemented with different topologies and technologies (90nm and 65nm CMOS). In both cases, the transimpedance amplifier uses the inverter-based shunt-feedback topology because the tunability of this configuration can easily be achieved by incorporating a digitally controlled resistance and a tunable resistance than the other topologies and it also provides more transconductance (g_m) with the same power dissipation than a conventional CS resistive-load shunt-feedback TIA. Furthermore, this topology shows low input referred noise which will be discussed later. Before discussing the inverter-based shunt-feedback TIA, the behaviour of a feedback TIA in the frequency domain will be discussed. Figure 3.5 shows a conventional resistive shunt feedback TIA, where R_F is the feedback resistance, A is the amplifier gain, C_{IN} is the input capacitance, I_{IN} is the input current and V_{out} is the output voltage. The detailed analysis of the 1st order and the 2nd order feedback TIA is given below[1].

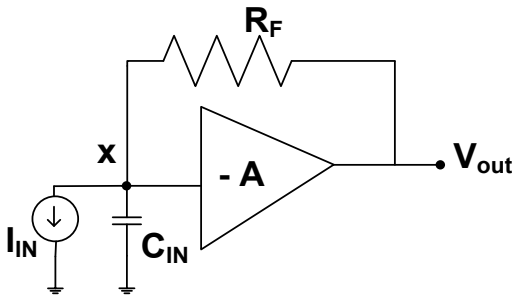

Figure 3.5: Conventional shunt feedback TIA.

[1] G. Cowan, Lecture Slides on Receiver Circuits, Jan. 2013, Concordia University.

Consider the 1st order shunt feedback TIA. Writing KCL at node X,

$$(sC_{IN} + G_F)\, V_X + (-G_F)V_{out} = I_{IN},$$

Where, G_F = feedback conductance (reciprocal of R_F) and V_x = voltage at node X.

Again,

$$V_X + \left(\frac{V_{out}}{-A}\right) = 0$$

Writing this equations in matrix,

$$\begin{bmatrix} sC_{IN} + G_F & -G_F \\ A & 1 \end{bmatrix} \begin{bmatrix} V_X \\ V_{out} \end{bmatrix} = \begin{bmatrix} I_{IN} \\ 0 \end{bmatrix}$$

Using Cramer's rule to solve for input impedance $Z_{IN,}$

$$\frac{V_{out}}{I_{IN}} = \frac{-AR_F}{sR_F C_{IN} + (1+A)} \qquad (3.1)$$

$$\frac{V_X}{I_{IN}} = \frac{1}{sC_{IN} + G_F (1+A)}$$

$$Z_{IN} = \frac{R_F}{sR_F C_{IN} + (1+A)} \qquad (3.2)$$

The -3dB bandwidth of the 1st order system $f_{-3dB\_1^{st}\ order}$ becomes (assuming the input has dominant pole),

$$f_{-3dB\_1^{st}\ order} = \frac{A}{2\pi R_F C_{IN}} \qquad (3.3)$$

Considering now the 2nd order analysis, assuming the feed-forward amplifier has a one-pole transfer function, we obtain

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_0}},$$

where, A_0 denotes the low frequency gain and ω_0 is the 3-dB bandwidth.

Substitution the *A(s)* in (3.1):

$$\frac{V_{out}}{I_{IN}} = - \frac{A_0 \, R_F}{\left(1 + \frac{s}{\omega_0}\right)(sR_F \, C_{IN} + 1) + \, A_0}$$

$$\frac{V_{out}}{I_{IN}} = - \frac{A_0 \, R_F}{\left(\frac{R_F C_{IN}}{\omega_0} s^2\right) + \left(R_F \, C_{IN} + \frac{1}{\omega_0}\right) s + 1 + \, A_0} \qquad (3.4)$$

The above system will have two poles ω_{p1} and ω_{p2}. Assuming the 2nd pole is much higher in magnitude than the 1st pole.

$$\omega_{p2} \gg \, \omega_{p1}, \qquad \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right) \approx \, \frac{1}{\omega_{p1}}$$

From (3.4),

$$\frac{V_{out}}{I_{IN}} = - \frac{A_0 \, R_F/(1 + A_0)}{\left(\frac{R_F C_{IN}}{(1+A_0)\omega_0} s^2\right) + \frac{1}{(1+A_0)}\left(R_F \, C_{IN} + \frac{1}{\omega_0}\right) s + 1}$$

Therefore,

$$\frac{1}{\omega_{p1}} = \, \frac{1}{(1 + A_0)}\left(R_F \, C_{IN} + \frac{1}{\omega_0}\right)$$

$$\omega_{p1} = \frac{(1 + A_0)}{(R_F\, C_{IN} + \frac{1}{\omega_0})} \qquad (3.5)$$

Now, by comparing (3.2) with (3.5) it can be found that, the 1st pole is lower than the 1st order feedback TIA by $(1/\omega_0)$ term.

The 2nd pole can be obtained by,

$$\frac{1}{\omega_{p1}\omega_{p2}} = \frac{R_F\, C_{IN}}{(1 + A_0)\omega_0}$$

$$\omega_{p1}\omega_{p2} = \frac{(1 + A_0)\omega_0}{(R_F\, C_{IN})} \qquad (3.6)$$

Substituting the ω_{p1} to (3.6),

$$\omega_{p2} = \frac{(1 + A_0)\omega_0}{(R_F\, C_{IN})} \cdot \frac{(R_F\, C_D + \frac{1}{\omega_0})}{(1 + A_0)}$$

$$\omega_{p2} = \frac{\omega_0 \left(R_F\, C_{IN} + \frac{1}{\omega_0}\right)}{R_F\, C_{IN}} = \omega_0 + \frac{1}{R_F\, C_{IN}} \qquad (3.7)$$

From (3.7) it can be seen that the 2nd pole is equal to the sum of the open loop poles.

Now assuming that the 2nd pole ω_{p2} is much greater than the 1st pole ω_{p1} then,

$$\omega_{p2} \gg \omega_{p1}$$

From equation (3.5) and (3.7), we get

$$\omega_0 + \frac{1}{R_F\, C_{IN}} \gg \frac{(1 + A_0)}{(R_F\, C_{IN} + \frac{1}{\omega_0})}$$

$$\frac{R_F\, C_{IN}\omega_0 + 1}{R_F\, C_{IN}} \gg \frac{(1 + A_0)}{(R_F\, C_{IN}\omega_0 + 1)}$$

$$(R_F\, C_{IN}\omega_0 + 1)^2 \gg (1 + A_0)R_F\, C_{IN}\omega_0$$

Assuming that the angular frequency is greater than the inverse of the time constant,

Therefore,

$$\omega_0 \gg (R_F\, C_{IN})^{-1}$$

$$(R_F\, C_{IN}\omega_0 + 1) \approx R_F\, C_{IN}\omega_0$$

$$(R_F\, C_{IN}\omega_0)^2 \gg (1 + A_0)R_F\, C_{IN}\omega_0$$

$$R_F\, C_{IN}\omega_0 \gg (1 + A_0)$$

$$\omega_0 \gg \frac{(1 + A_0)}{R_F\, C_{IN}} \qquad (3.8)$$

From (3.8) it is clear that, the open-loop pole of the amplifier should be higher than the close-loop pole resulting from feedback resistance R_F and input capacitance $C_{IN.}$

Now, to ensure a good response in time domain (critically damped behaviour) from a 2nd order system, it requires that $\zeta = \frac{1}{\sqrt{2}}$. Having $\zeta < \frac{1}{\sqrt{2}}$ may create ISI and corrupt the data.

A typical 2nd order transfer function,

$$Z(S) = -\frac{1}{s^2 + 2\zeta\omega_n s + \omega_n{}^2}$$

From (3.4), we obtain

$$\frac{V_{out}}{I_{IN}} = -\frac{A_0 \frac{\omega_0}{C_{IN}}}{s^2 + \frac{R_F C_{IN} + \frac{1}{\omega_0}}{\frac{R_F C_{IN}}{\omega_0}} s + \frac{(A_0+1)\omega_0}{R_F C_{IN}}}$$

Therefore,

$$\omega_n{}^2 = \frac{(A_0 + 1)\omega_0}{R_F C_{IN}} \qquad (3.9)$$

$$\zeta = \frac{1}{2} \frac{R_F C_{IN}\omega_0 + 1}{\sqrt{(A_0 + 1)\omega_0 R_F C_{IN}}} \qquad (3.10)$$

$$\omega_0 = \frac{A_0 \pm \sqrt{A_0{}^2 - 1}}{R_F C_{IN}} \approx \frac{2A_0}{R_F C_{IN}}$$

$$\zeta = \frac{1}{\sqrt{2}}, \quad \omega_0 = \frac{2A_0}{R_F C_{IN}}$$

Substituting ω_0 in (3.9), we get

$$\omega_n{}^2 = \frac{(A_0 + 1)}{R_F C_{IN}} . \frac{2A_0}{R_F C_{IN}}$$

$$\omega_n = \sqrt{2} \frac{A_0}{R_F C_{IN}}$$

$$\omega_{-3dB} = \omega_n = \sqrt{2} \frac{A_0}{R_F C_{IN}} \qquad (3.11)$$

Comparing (3.3) with the (3.11) it can be found that,

$$f_{-3dB\_2^{nd}\ order} = \sqrt{2}\ \frac{A_0}{2\pi R_F\, C_{IN}} = \sqrt{2}\ f_{-3dB\_1^{st}\ order} \qquad (3.12)$$

Therefore, the 2nd order shunt feedback TIA's bandwidth is 41% larger than the 1st order TIA.

Table 3.3: Bandwidth of 1st and 2nd order shunt feedback TIA [5]

TIA	Bandwidth	Improvement
1st order	$\omega_{-3dB} = \frac{A_0}{R_F\, C_{IN}}$	0
2nd order	$\omega_{-3dB} = \sqrt{2}\ \frac{A_0}{R_F\, C_{IN}}$	41%

3.5.1 Small Signal Analysis of Inverter Based Shunt Feedback TIA

The inverter based shunt feedback TIA has more transconductance than a conventional CS resistive feedback TIA as both its PMOS and NMOS contribute in the overall g_m. Figure 3.6 shows the inverter based shunt feedback TIA with its small signal model where, M_1, M_2 is NMOS and PMOS, respectively, R_F is the feedback resistance

and g_m is the total transconductance. The detailed analysis of the inverter based shunt feedback TIA with its low frequency small signal model is given below[1] :

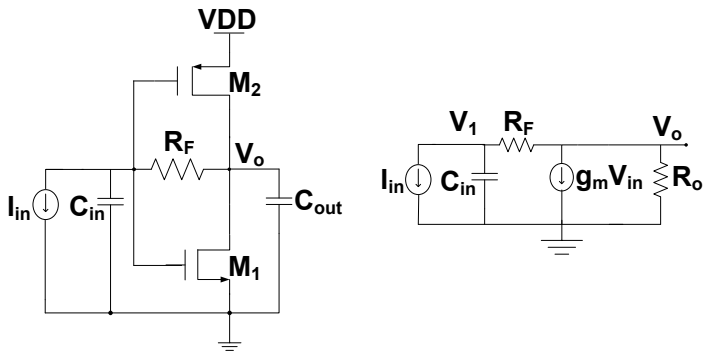

Figure 3.6: The inverter based shunt feedback TIA and its small signal model.

Assumptions: Overall Transconductance, $g_m = g_{m1} + g_{m2}$

Total Output Resistance, $R_0 = r_{01} \,||\, r_{02}$

Total Input Capacitance, $C_{in} = C_{IN} + C_{GS1} + C_{GS2}$

Total Output Capacitance, $C_{out} = C_{DB1} + C_{DB2} + C_{load}$

From low frequency small signal model analysis and applying KCL at node V_1, we obtain

$$\begin{bmatrix} G_F & -G_F \\ g_m - G_F & G_F + G_0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_{out} \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \end{bmatrix},$$

where, G_F and G_0 are the feedback conductance and total output conductance, respectively.

[1] G. Cowan, Lecture Slides on Receiver Circuits, Jan. 2013, Concordia University.

Using Cramer's rule to solve for input resistance R_{in}:

$$det\begin{bmatrix} I_{in} & -G_F \\ 0 & G_F + G_0 \end{bmatrix} = I_{in}(G_F + G_0)$$

The input resistance is

$$R_{in} = \frac{V_1}{I_{in}} = \frac{G_F + G_0}{G_F G_0 + G_F g_m} \approx \frac{1}{g_m} \qquad (3.13)$$

The output resistance is

$$R_{out} = \frac{V_{out}}{I_t} = \frac{G_F}{G_F G_0 + G_F g_m} = \frac{1}{G_0 + g_m} \approx \frac{1}{g_m} \qquad (3.14)$$

The transimpedance is

$$R_T = \frac{V_o}{I_{in}} = \frac{G_F - g_m}{G_F G_0 + G_F g_m} = \frac{1 - g_m R_F}{G_0 + g_m} \qquad (3.15)$$

$$R_T \approx -R_F \ as \ g_m R_F \gg 1$$

The -3dB bandwidth, assuming the input pole becomes dominant, is

$$f_{-3dB} = \frac{1}{2\pi R_{in} C_{in}} \qquad (3.16)$$

From (3.16) it is clear that the TIA bandwidth is determined by the time constant $R_{in}C_{in}$ at the input. If a fixed C_{in} is assumed, the TIA bandwidth can be controlled if R_{in} is controllable. As discussed previously, in order to implement the power and bandwidth

proportional TIA with a fixed gain, a current-controlling PMOS array has been implemented. This current-controlling PMOS array allows the g_m of the TIA to be adjusted which, according to (3.13), will change R_{in}.

3.5.2 Noise Analysis

The noise performance of the inverter based shunt feedback TIA is better than the conventional CS with resistive load TIA. Low frequency noise analysis of the Inverter based shunt feedback TIA is given below:

Assumptions:

- Noise current source due to NMOS (M_1) and PMOS (M_2) = $I_{n,M1\_2}$
- Noise current source due to feedback resistance R_f = $I_{n,Rf}$

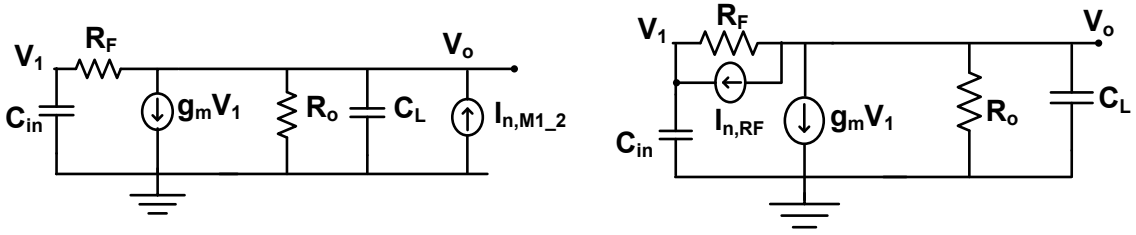

Figure 3.7: Small signal model for low frequency noise analysis with the corresponding noise sources (noise source due to NMOS and PMOS (left) and noise source due to R_f (right)).

Noise transfer function for the PMOS and NMOS, $H_{n,M1\_2}$ becomes:

$$H_{In,M1\_2} = R_{out} = \frac{V_0}{I_{n,M1\_2}} = \frac{G_F}{G_F G_0 + G_F\, g_m} = \frac{1}{G_0 + g_m} \approx \frac{1}{g_m},$$

where, G_F, G_0, g_m, V_0 is the feedback conductance, output conductance, overall transconductance and output voltage, respectively.

Noise transfer function for the feedback resistance, H_{R_F} becomes:

$$H_{R_F} = \frac{V_0}{I_{n,RF}} = \frac{g_m}{G_F G_0 + G_F g_m} = \frac{g_m R_F}{G_0 + g_m} \approx R_F$$

Now, the noise power spectral density (PSD) of R_F and M_{1_2} are $\frac{4kT}{R_F}$ and $4kT\gamma g_m$, respectively. In this case, k indicates the Boltzmann's constant = $1.38 * 10^{-23}\, J/K$ and T is the Absolute temperature in Kelvin.

Therefore, the overall output referred noise $S_{v,n,out}$ will be:

$$S_{v,n,out} = PSD\ of\ R_F * \left(H_{R_F}\right)^2 + PSD\ of\ M_{1_2} * \left(H_{In,M1_2}\right)^2 \qquad (3.17)$$

Substituting the $H_{In,M1\_2}$ and H_{R_F} in (3.17),

$$S_{v,n,out} = \frac{4kT}{R_F}\, {R_F}^2 + 4kT\gamma\, g_m\, \frac{1}{{g_m}^2}$$

Now, the input referred noise will be:

$$S_{IN,in} = \frac{S_{v,n,out}}{{A_v}^2}, \qquad (3.18)$$

where, A_v indicates the low frequency gain of the TIA,

Substituting the $S_{v,n,out}$ in (3.18) the input referred noise becomes:

$$S_{IN,in} = \frac{4kT}{R_F} + 4kT\gamma \frac{1}{g_m {R_F}^2} \qquad (3.19)$$

From (3.19) it is clear that for a fixed feedback resistance, R_F, the second term of the input referred noise is inversely proportional to the transconductance (g_m) of the transistors. The inverter structure has more transconductance (g_m) as it has an extra PMOS transistor with the NMOS.

3.5.3 Design 1

Figure 3.8 shows the proposed TIA that was implemented using the 90nm CMOS technology. There are five PMOS devices in the array from M_3 to M_7 that are switched on and off according to the data rate. For each data rate, only one switch is on. With this mechanism it is possible to control the TIA's dc bias current, which eventually changes the g_m and g_{ds} of M_1 and M_2. The overall g_m of the TIA is further reduced because the output impedance of the PMOS array degenerates M_2, thereby reducing its contribution to the overall g_m of the circuit.

The feedback resistance R_f shown in Figure 3.6 has an important impact in this tuning mechanism. When the data rate scales down from 15 Gb/s to 1.25 Gb/s, the dc bias voltage of the overall receiver chain also goes down. As a result, the post amplifier circuit starts to operate in the weak inversion region as g_m is reduced, which makes the per stage gain of the post amplifier ~ 1. Since it is desired to have a fixed gain throughout all data rates (1.25 Gb/s to 15 Gb/s), the gain of the TIA is boosted up in order to

compensate for the reduced post amplifier gain. This is achieved by tuning M_{15}, an NMOS transistor operating in the triode region, as shown in Figure 3.8.

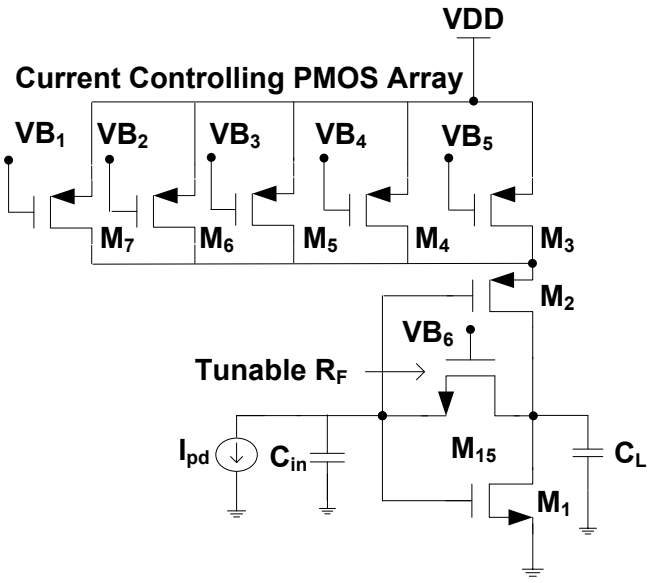

Figure 3.8: Proposed TIA in Design 1.

3.5.4 Design 2

Figure 3.9 shows the proposed TIA designed in 65nm CMOS. The topology used is the same as the one followed for Design 1 but in this case a binary-weighted PMOS array and a resistive bank is incorporated instead of a fixed width PMOS array and a triode-region NMOS. The triode region NMOS suffers from severe global process variations when its overdrive voltage is low while operating at low data rates. To solve this robustness problem, a new resistive bank is implemented in this design. By tuning this proposed resistance bank, a fixed gain can be achieved through the receiver chain when the data rate scales down. The operation of the resistive bank is described in Section 3.9.

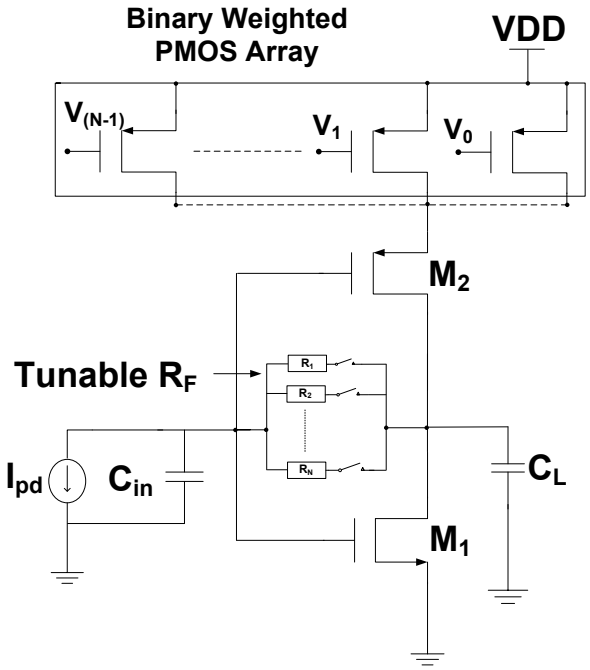

Figure 3.9: Proposed TIA in Design 2 with binary weighted PMOS array and tuneable resistance bank.

3.6 Post-Amplifiers (PA)

In order to amplify the TIA's output to a large enough level to apply to a decision circuit, a post amplifier (PA) is used. Certain requirements have to be fulfilled for designing the post amplifiers [5].

- Output swing: requirements for minimum input signal depend on the decision circuit's sensitivity. As an example, for ~ (10 – 30) μA noise less input current the required output swing for decision circuit is ~ (100 – 300) mV.
- Input capacitance: should not be too high to load the TIA
- Bandwidth: usually should be same as data rate.
- Noise: usually not critical provided the TIA's gain is large enough.

- Gain: should be high enough. Due to the gain bandwidth trade-off, a few stages in the post amplifier are usually needed.
- Output drive: have to drive a 50-ohm output load for standalone testing, or the input capacitance of the decision circuits.
- Offset voltage: an offset voltage is introduced due to device mismatch which may eventually saturate the output swing and change the operating point of the circuit.

3.6.1 Cascaded Gain Stage Design

It is not possible to design a single-stage high-speed, high-gain post-amplifier due to its gain bandwidth trade-off. Therefore, cascaded stages are generally incorporated in order to get a large amount of gain from the post-amplifiers with sufficient bandwidth. To design a cascaded post-amplifier some qualitative analysis is needed. The analysis is shown below:

For a given N identical 1st order stages with a gain of A_0 and a bandwidth of ω_0 , the overall -3dB bandwidth can be derived as follow[1] :

$$H(s) = \left(\frac{A_0}{1 + \frac{s}{\omega_0}} \right)^N$$

Assuming, $s = j\omega_{-3dB}$ and ω_{-3dB} becomes:

[1] G. Cowan, Lecture Slides on Receiver Circuits, Jan. 2013, Concordia University.

$$\left(\frac{A_0}{\sqrt{1+\left(\frac{\omega_{-3dB}}{\omega_0}\right)^2}}\right)^N = \frac{(A_0)^N}{\sqrt{2}}$$

Thus,

$$\left(\frac{\omega_{-3dB}}{\omega_0}\right)^2 = \sqrt[N]{2}-1$$

$$\frac{\omega_{-3dB}}{\omega_0} = \sqrt{\sqrt[N]{2}-1}$$

$$\omega_{-3dB} = \omega_{-overall} = \omega_0\sqrt{\sqrt[N]{2}-1} = \omega_{per\ stage}\sqrt{\sqrt[N]{2}-1} \qquad (3.20)$$

$$\omega_{-3dB} = \omega_0\sqrt{\sqrt[N]{2}-1} \approx \omega_0\frac{0.9}{\sqrt{N}}\ ,if\ N \geq 2$$

However, if we need an overall gain of $A_{tot,}$ each stage only needs to provide $A_0 = \sqrt[N]{A_{tot}}$. As an example, if A_{tot} = 100, then for a 4-stage post-amplifier design per stage gain becomes A_0 = 3.16 and the ω_0 becomes 2.3 times ω_{-3dB} [5].

Now, if B is the gain bandwidth product for an amplifier then,

$$\omega_0 = \frac{B}{\sqrt[N]{A_{tot}}}$$

$$\omega_{-3dB} = \frac{B}{\sqrt[N]{A_{tot}}}\frac{0.9}{\sqrt{N}}$$

Usually, the post-amplifier design is limited to 5 stages because beyond that noise and power dissipation increase more than the bandwidth. Figure 3.10 shows a graph where an incremanetal change in ω_{-3dB}/B is plotted as a function of N for $A_{total}=100$ [5]. From this figure, it is clear that beyond the 5 stages ($N>5$) overall bandwidth improvement goes down. Futhermore, if $N > 5$, the gain per stage becomes smaller and bandwith becomes higher, which results in higher noise current with extra power dissipation [5].

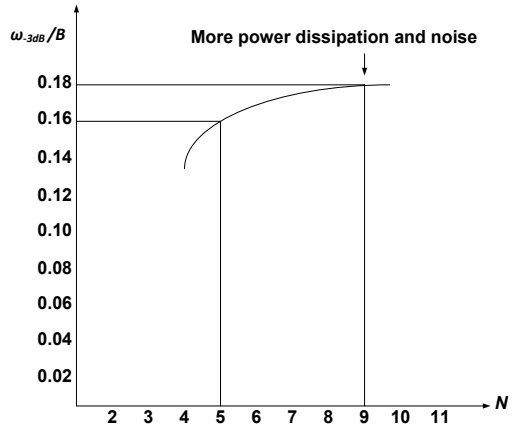

Figure 3.10: Normalized bandwidth as a function of N for $A_{tot}=100$ [5].

3.6.2 Bandwidth Extension

Bandwidth extension is necessary in order to have a wideband receiver. However, one should be careful about peaking in the frequency domain caused by this bandwidth extension as it may distort the amplifier's transient response. Inductive peaking is one of the best ways to extend the bandwidth further . However, passive inductors are big in size compared to the active inductors, therfore it takes a larger chip area than the active one [5]. Theoretical analysis of the shunt inductive peaking with passive inductor and the common source amplifier with resistive load is given below:

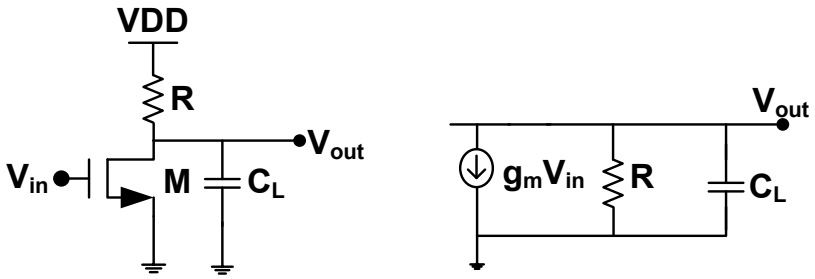

Figure 3.11: Common source amplifier and its small signal model.

Transfer function of the common source amplifier with resistive load is

$$\frac{V_{out}}{V_{in}}(s) = -g_m R \frac{1}{SC_L R+1} \qquad (3.21)$$

The -3dB bandwidth is determined as,

$$\omega_{-3dB} = \frac{1}{RC_L} \qquad (3.22)$$

The above equation (3.21) is a 1st order response and the bandwidth is limited by the output capacitance C_L.

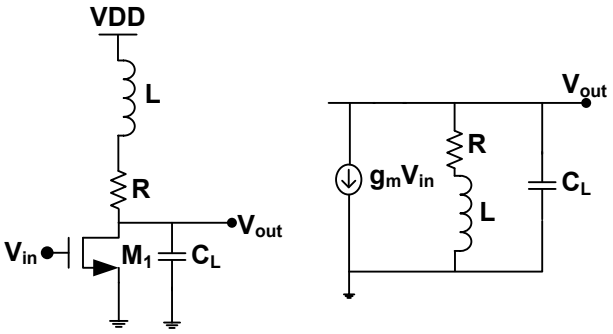

Figure 3.12: Common source amplifier and its small signal analysis with resistive and inductive load.

Transfer function of the common source amplifier with resistive and inductive load:

$$\frac{V_{out}}{V_{in}}(s) = -g_m \frac{R+sL}{sC_L(R+sL)+1}$$

$$\frac{V_{out}}{V_{in}}(s) = -g_m \frac{R+sL}{s^2C_LL+sC_LR+1} \qquad (3.23)$$

From (3.22) the 2nd order parameters are:

$$\omega_n = \sqrt{\frac{1}{C_LL}}, \qquad \zeta = \frac{R}{2}\sqrt{\frac{C_L}{L}}$$

If $\zeta = \frac{1}{2}$ then L becomes:

$$L = \frac{R^2C_L}{2}$$

Therefore neglecting the effect of zero which is $\omega_z = \frac{R}{L}$, the natural frequency or the -3dB bandwidth ($\omega_n = \omega_{-3dB}$) becomes:

$$\omega_n = \omega_{-3dB} = \frac{\sqrt{2}}{RC_L} \qquad (3.24)$$

Now, if (3.22) and (3.24) is compared then it is found that ~ 41 % bandwidth can be extended without zero by the inductive peaking method.

For the more bandwidth extension zero should be considered. Table 3.4 shows the characteristics of the overshoot with zero and without zero and its corresponding bandwidth improvement [5].

Table 3.4: Bandwidth improvement due to inductive peaking with its overshoot characteristics [5]

Overshoot	5%	7.5%	10%
ζ (with zero)	0.73	0.69	0.65
ζ (without zero)	0.69	0.64	0.59
Bandwidth Improvement (with zero)	78%	82%	84%

Although with the help of inductive peaking it is possible to get a large bandwidth extension but implementations of this inductor costs larger chip area. As discussed in earlier chapter, small footprint of the optical transceiver is one of the short-reach link design specifications therefore active inductors [5] are used rather than the passive inductors for bandwidth extension in Design 1(90 nm CMOS). Figure 3.13 shows the active inductor circuit and its small signal model. The impedance transfer function of the active inductor circuit is shown in (3.25).

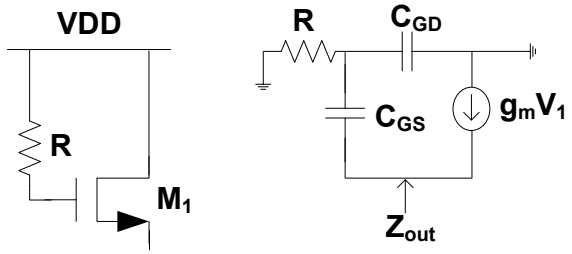

Figure 3.13: NMOS active inductor and its small signal model.

$$Z_{out} = \frac{(1+s(C_{GS}+C_{GD})R)}{(g_{m1}+sC_{GS})(1+sC_{GD}R)}, \qquad (3.25)$$

where, C_{GS},C_{GD} indicates the gate-source capacitance and gate-drain capacitance of the CMOS transistor M_1, respectively.

Frequency response of the impedance transfer function of active inductor circuit is shown in Figure 3.14. The response is plotted with and without gate-drain capacitor (C_{GD}). From the figure, it is clear that without C_{GD}, at low frequency the active inductor circuit behaves like a resistance and at high frequency its response increases like an passive inductor. However, this response at high frequency becomes limited if a gate-drain capacitance (C_{GD}) is considered as shown in Figure 3.14.

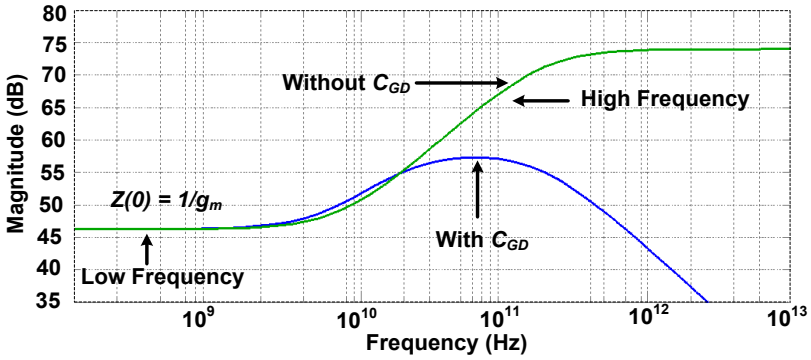

Figure 3.14: Frequency response of the active inductor circuit.

From the simulation it is found that, with the help of inductive peaking it is possible to increase the bandwidth up to ~ 1.8 times whereas using the active inductor bandwidth can be extended up to ~ 1.3 times as its bandwidth extension is limited by a non-zero C_{GD}. Another noticeable problem of the active inductor is the voltage headroom problem if it is biased through a low voltage supply. There are several modifications that have been proposed for these concerns. One solution is to increase the gate voltage of the

active inductor above the V_{DD} in order to reduce the V_{DS} drop as shown in Figure 3.15. The NMOS transistor will operate in the saturation region and its small signal operation will not be hampered. No significant amount of current will be drawn from this extra source. Therefore, the power dissipation will remain unchanged [11].

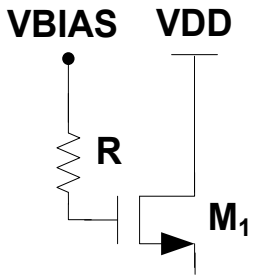

Figure 3.15: Extra voltage applied at the gate to avoid voltage headroom problem.

3.7 Post-Amplifier (PA) Design

Two types of post amplifier having 2 different topologies are implemented in Design 1 and Design 2.

3.7.1 Design 1

In Design 1 post amplifier is based on the conventional common source amplifier with active inductor loads. A common source amplifier with resistive load cannot be used for the highest data rate as its bandwidth is limited by the load capacitance; therefore, the use of a bandwidth extension is necessary. An active inductor is used for the bandwidth extension in this design. The voltage headroom problem of the active inductor is solved using an extra bias to the gate of the MOSFET as shown in Figure 3.15. The 4-stage post amplifier is shown in Figure 3.16.

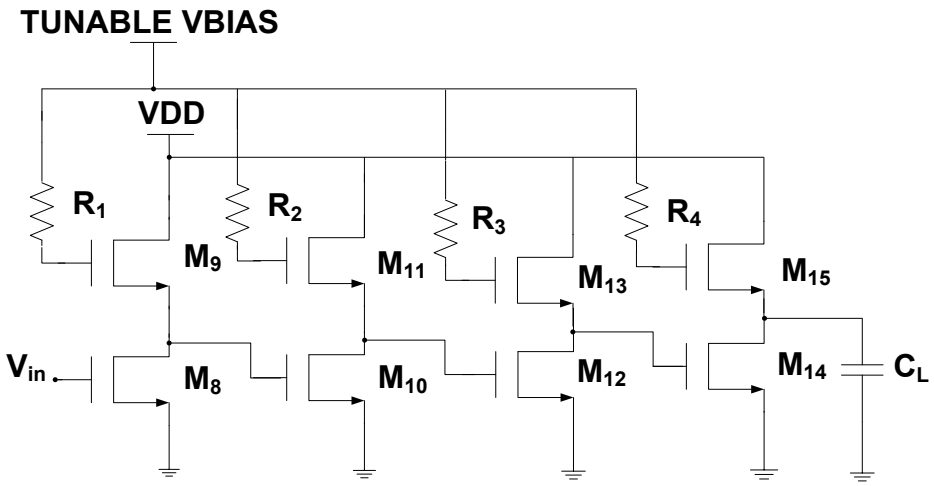

Figure 3.16: 4-stage dc coupled post-amplifiers in Design 1.

Each stage of the post-amplifier is dc-coupled to one another. Therefore, the input of every stage is biased by the output of the previous stage. This voltage is controlled by tuning the VBIAS of the active inductor circuit. VBIAS can be tuned through a DC to DC converter circuit or other mechanisms can be adopted such as storing the bias voltages in capacitors or using resistive dividers.

3.7.2 Design 2

The major drawback of post amplifier tuning in Design 1 is its VBIAS setting. As discussed in the previous section, each stage of the post-amplifier is biased by the output of the previous stage and these voltages are established by tuning the VBIAS, which eventually delays the response time of reconfiguration. On the other hand, implementation of these bias voltages is also difficult. This problem is solved in the Design 2 by incorporating the inverter based structure with binary weighted PMOS array and the resistive bank. The binary weighted PMOS array enables the bias voltage to change rapidly and improves the response time of reconfiguration. In Design 2 the post

amplifiers are based on the single ended Cherry-Hooper inverter-based topology [12]. A 3-stage post-amplifier has been utilized in this design. Each of the three post-amplifier stages is itself a two-stage cascaded amplifier as shown in Figure 3.17. The first stage converts the input voltage V_{in} to a current I_x with a transconductance of $g_{m,a,total}$ ($g_{m,a,total} = g_{m,a,1} + g_{m,a,2}$). The second stage converts the current I_x to a voltage V_{out} with a gain of $\sim -R_f$. The main advantage of this circuit is that it has two poles with low input and output resistance ($\sim 1/g_m$) which results in a much higher pole frequency than any other cascaded common source topology [5].

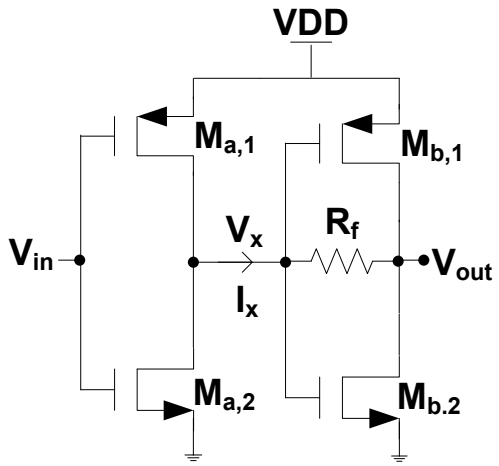

Figure 3.17: Two stage cascaded inverter based post-amplifier.

The low-frequency voltage gain of this circuit is given by:

$$\frac{V_{out}}{V_{in}} = g_{m,a,total}R_f - \frac{g_{m,a,total}}{g_{m,b,total}}, \qquad (3.26)$$

where $g_{m,a,total}$ and $g_{m,b,total}$ indicate the total transconductance of the 1st and 2nd stage of each post amplifier, respectively and R_f is the feedback resistance of the 2nd stage.

Figure 3.18 shows the proposed post amplifiers in Design 2 with the binary weighted PMOS array and the resistive bank.

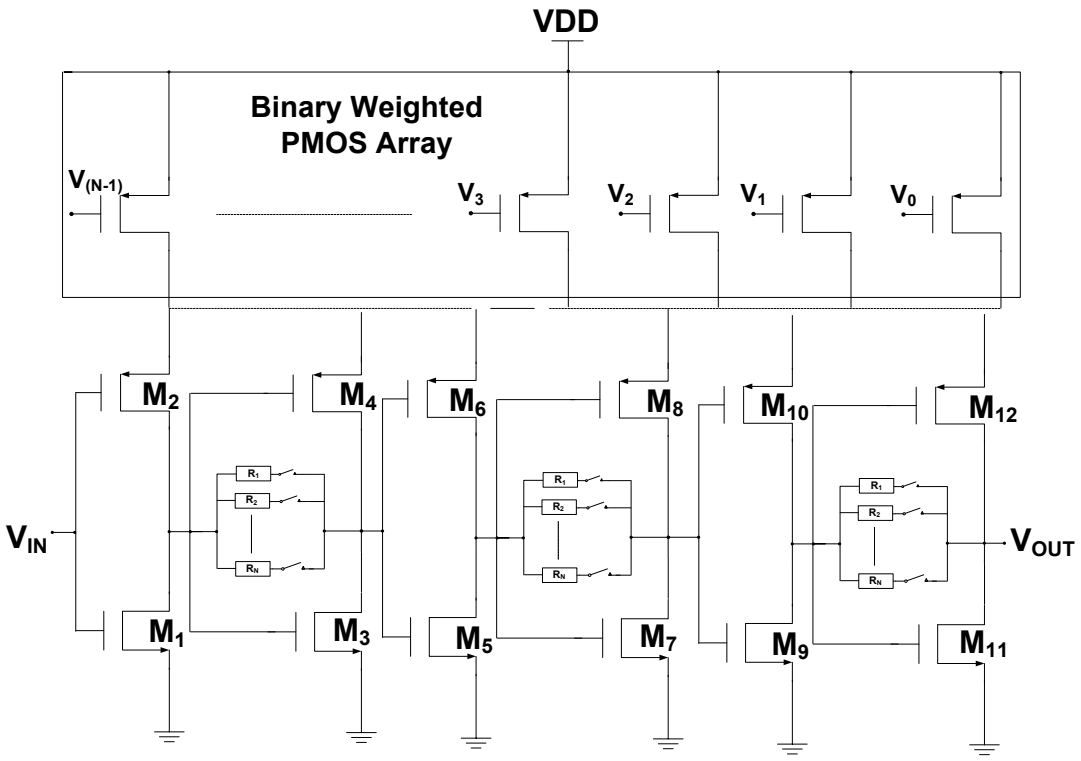

Figure 3.18: 3-stage post amplifier used in Design 2.

3.8 Offset Compensation

The post-amplifier provides a constant gain over a large range of frequencies. However, due to device mismatch and low frequency noise sources, an offset voltage may introduce and saturate the output swing and change the bias voltages. To avoid this problem, an offset compensation loop is necessary. Normally, an offset compensation loop incorporates a feedback loop that reduces the low-frequency gain and obtains a band-pass transfer characteristic of the overall amplifier [13]. Some trade-offs have to be kept in mind while designing an offset compensation block. The trade-offs are:

- The cut off frequency of the low pass filter should be small enough so that it does not create any baseline wander problem while transmitting an longer run of identical bits.
- The cut off frequency needs to be large while changing the data rate so that the overall receiver can shift the bias point as soon as possible.

3.8.1 Design 1

No offset compensation technique is employed, for this reason the circuit suffers severe mismatch and global process variations.

3.8.2 Design 2

In this design, an offset compensation technique is incorporated to cancel out the mismatch effect. The offset compensation employs an active low pass filter [12] with a binary weighted PMOS array shown in Figure 3.19.

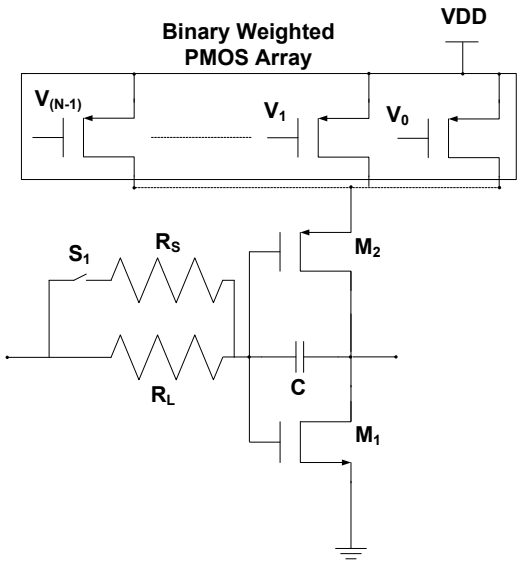

Figure 3.19: Active low pass filter used in Design 2.

In the active low pass filter as shown in Figure 3.19, the effective time constant becomes $\tau = RC\ (1 + g_m r_0)$, where, $g_m = (g_{m1} + g_{m2})$ indicates the total transconductance of the inverter structure, which means that capacitor *C* actually increases due to the miller effect of the inverter. Also, the capacitor is connected in the feedback such that, it does not need to be charged or discharged that much when the bias point is changed at steady-state, compared to the passive low pass filter where the capacitor is connected in between ground and the resistor as shown in Figure 3.20.

A small resistance R_s is also incorporated in the offset compensation block and is connected in parallel with large resistance R_L while the data rate is switching, which helps to make the time constant smaller. To control that small resistance, a pulse generation circuit is implemented, as shown in Figure 3.21. The XOR gate generates the pulse output based on the inputs *IN* and *IN'*. *IN'* is the delayed version of the *IN*. This delay can be controlled by varying the capacitor *C*.

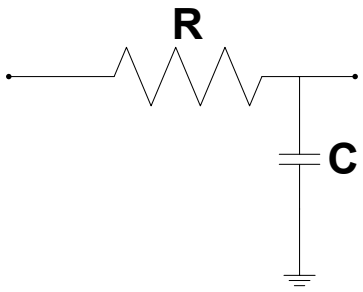

Figure 3.20: Passive low pass filter.

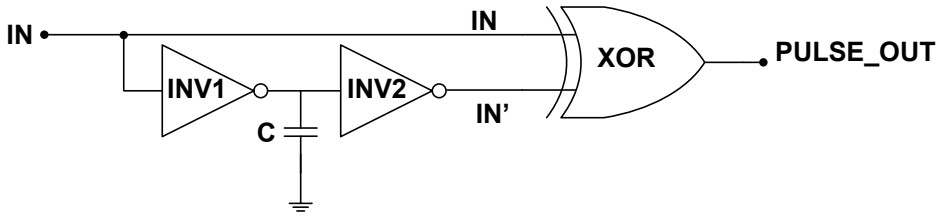

Figure 3.21: Pulse generation circuit for controlling the small R_s.

3.9 PMOS Array and Resistive Bank

Through simulation, the dimension of transistors in both PMOS array (Design1 and Design 2) has been determined. Design 2 PMOS array has more steps than the Design 1 as it incorporates binary weighted PMOS array as shown in Figure 3.22. The weighted range is from 250 nm to 256 μm in steps of 250 nm.

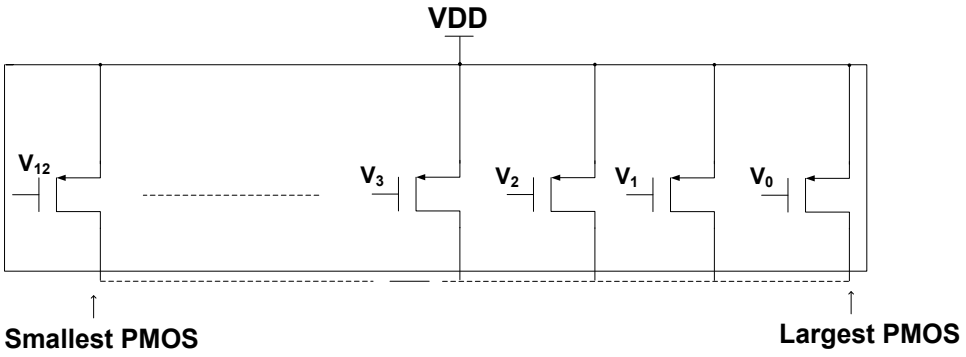

Figure 3.22: Binary weighted PMOS array.

In Design 2 the feedback resistance R_f is implemented by a tunable resistance bank. The resistance bank has 3 different passive resistors with 3 NMOS switches as shown in Figure 3.23. The gate voltage of the different NMOS switches are varied while changing the data rates, keeping the overdrive voltage greater than ~ 400 mV. In order to

get different voltages at different data rates, a voltage divider circuit is implemented as shown in Figure 3.24.

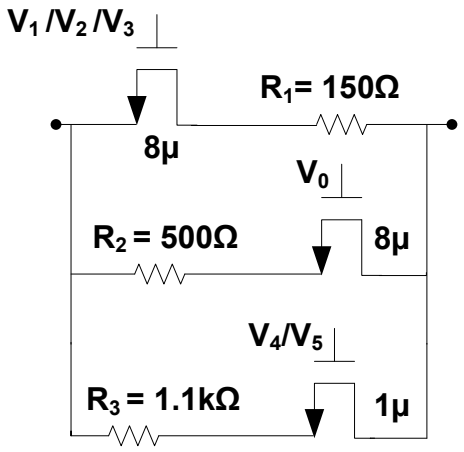

Figure 3.23: Proposed resistive bank used in Design 2.

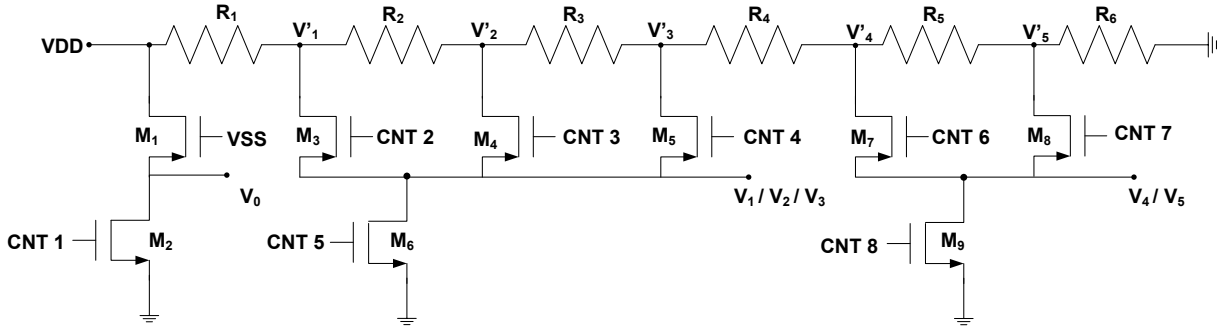

Figure 3.24: Voltage divider with control signals CNT1 to CNT8.

Table 3.5: Combination of control signals and output voltages

Output Voltages							
Control Signals		V_0	V_1	V_2	V_3	V_4	V_5
	Values (V)	1.2	1.1	1	0.85	0.75	0.70
	CNT 1	0	1	1	1	1	1
	CNT 2	1	0	1	1	1	1
	CNT 3	1	1	0	1	1	1
	CNT 4	1	1	1	0	1	1
	CNT 5	1	0	0	0	1	1
	CNT 6	1	1	1	1	0	1
	CNT 7	1	1	1	1	1	0
	CNT 8	1	1	1	1	0	0

Table 3.5 shows the control signals status for a specific output voltages. As an example, in order to get voltage V_1 (1.1 volt) all the control signals should be high except CNT 2 and CNT 5. The connection between the voltage divider and the resistance bank is shown in Figure 3.25.

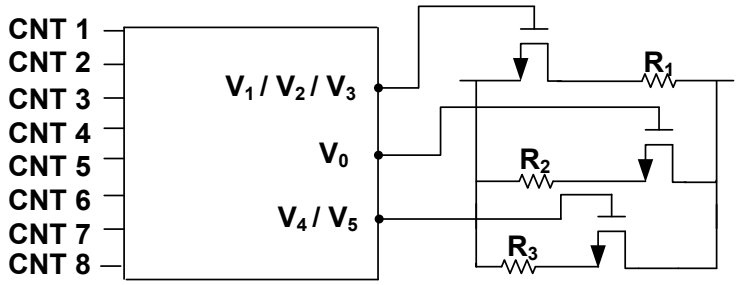

Figure 3.25: Connection between the voltage divider and the resistance bank.

3.10 Robustness

In order to investigate the robustness of both circuits, several simulations are performed in 90nm and 65nm CMOS. In one simulation, it was shown that due to the mismatch of the devices, the standard deviation of the bias voltage at each node of Design 1 becomes ~ 80mV, whereas in Design 2 it is only ~ 1.5 mV. The mismatch effect is more severe in the Design 1 owing to not having any offset compensation technique.

On the other hand, for global process variations which are assumed to equally affect all transistors of a given type in a design, Design 1and Design 2 shows a standard deviation of the bias voltage of ~ 150 mV and ~ 100 mV, respectively. However, for Design 2, this global process variation can be improved by tuning the binary weighted PMOS array and resistive bank. The quantitative analysis which has been done to prove this is shown in chapter 4.

3.11 Baseline Wander Calculation

As discussed, in order to avoid baseline wander caused by long runs of identical bits, the cut off frequency of the low pass filter should be lower. A numerical analysis of calculating the necessary time constant that is needed to avoid baseline wander for a passive low pass filter is given below:

Assumptions, transmitting data rate is = 1.25 G;

Maximum identical bits = 32;

Time for the identical bits length, t = 800 ps/bit * 32 bits = 25.6 ns

The estimation error (acceptable difference between the actual and estimated baseline wander) = ~ 0.001 [14]

For this, (t/τ) should be = 0.045 [14]

Therefore, τ = 568.9 ns

Now, if we assume, C = 1pF then the R = 568.9 ns / 1pF = 568.9 kΩ.

As shown for a fixed C, the required R can be calculated for a certain time constant (τ). In Design 2 due to incorporating a passive low pass filter, the effective time constant becomes $\tau = RC\ (1 + g_m r_0)$. This equation shows that the capacitor value will change if g_m changes. Bias point of the overall receiver changes when data rate changes, and to set the bias point, g_m of the receiver chain will also change which eventually

changes the capacitance value. For this design, the passive capacitance and resistance value that is used in the offset compensation are chosen as $C = 1pF$ and $R = 500k\Omega$.

3.12 Overall Receiver Front-End in Design 1

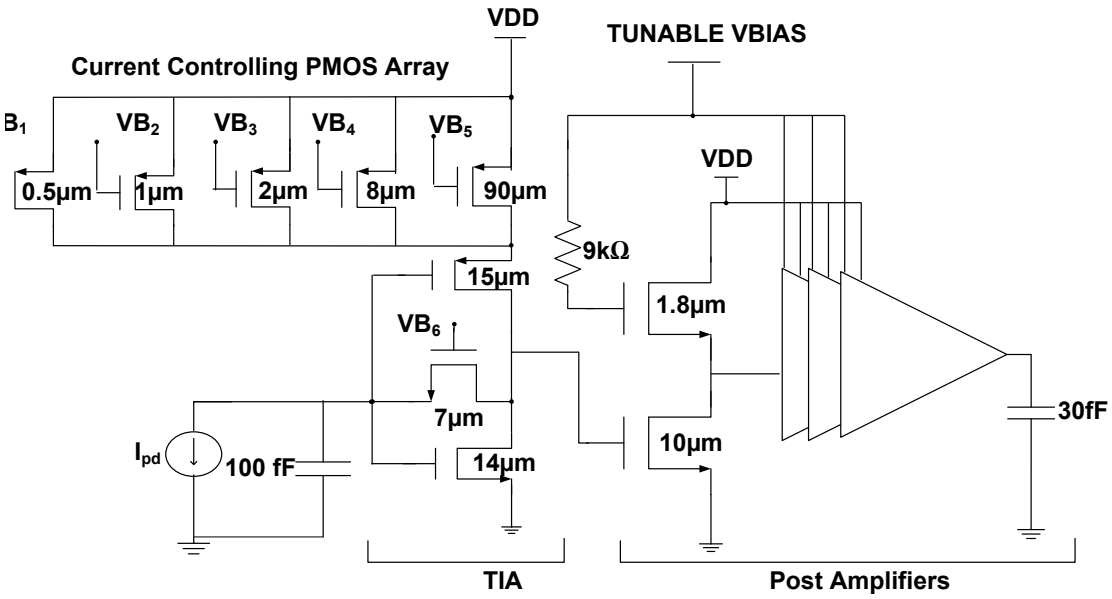

Figure 3.26: The overall receiver front-end receiver chain in Design 1.

Figure 3.26 shows the overall receiver front-end designed in 90nm CMOS.The post amplifiers in Design 1 are dc coupled with the TIA and biased through the dc voltage of the preceding stage. The respective sizes of the active inductors and the overall post amplifiers' transistors are determined from a simulation aiming to maximize the gain bandwidth product.

The input and output capacitances in both designs are assumed as *100fF* and *30fF*. The input capacitance is the sum of the photodiode's capacitance and that of the bond

pad. For the output capacitance, the receiver is assumed to drive a decision circuit, consisting of one or more flip-flops.

3.13 Overall Receiver Front-End in Design 2

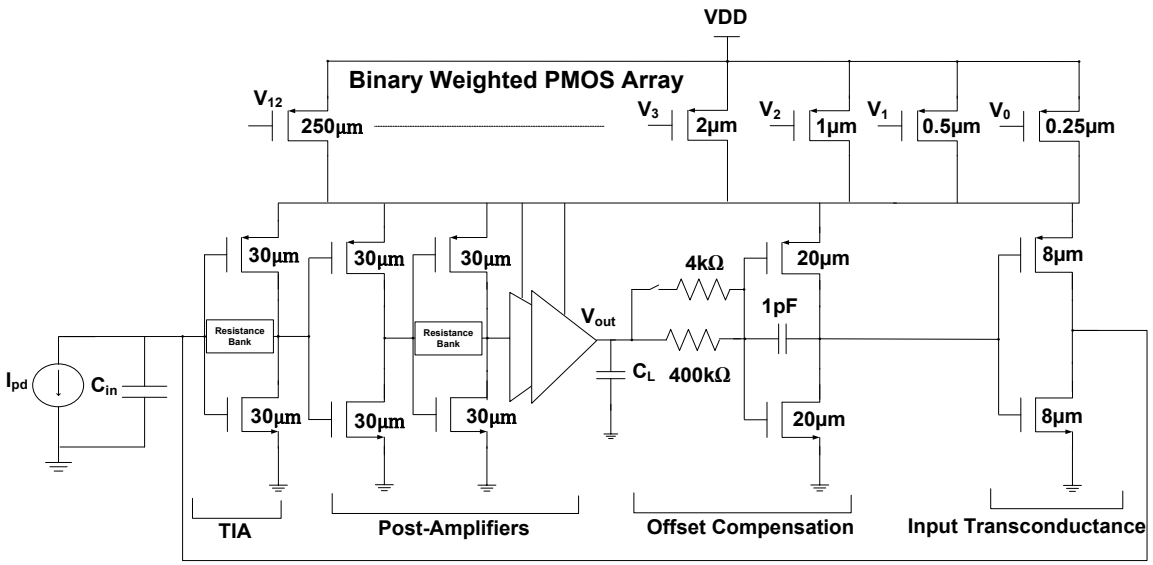

Figure 3.27: The overall receiver front-end receiver chain in Design 2 .

Figure 3.27 shows the overall front-end receiver chain designed in 65nm CMOS. In this design the overall receiver has a single ended inverter based cascaded structure biased through a binary weighted PMOS array. An analytical analysis has been done for determining the optimum dc bias voltage and maximum gain and bandwidth product from a shunt feedback inverter structure. The analysis is shown below[1] :

[1] G. Cowan, Lecture Slides on Receiver Circuits, Jan. 2013, Concordia University.

From Figure 3.6 we can write

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\ \frac{W_n}{L_n}\ (V_{GS1} - V_{tn})^2$$

$$I_{D2} = \frac{1}{2}\mu_p C_{ox}\ \frac{W_p}{L_p}\ (V_{SG2} - |V_{tp}|)^2\ ,$$

where, I_{D1} and I_{D2} = drain current of NMOS (M_1) and PMOS (M_2), μ_n and μ_p= mobility of M_1 and M_2, W_n and W_p = width of M_1 and M_2, L_n and L_p = length of M_1 and M_2, C_{ox} =gate oxide capacitance of CMOS, V_{GS1} = gate-source voltage of M_1. *Vtn* and *Vtp*= threshold voltage of M_1 and M_2, respectively.

Now, for an inverter structure we can write:

$$I_{D1} = I_{D2}$$

$$\frac{1}{2}\mu_n C_{ox}\ \frac{W_n}{L_n}\ (V_{GS1} - V_{tn})^2 = \frac{1}{2}\mu_p C_{ox}\ \frac{W_p}{L_p}\ (V_{SG2} - V_{tp})^2 \qquad (3.27)$$

For an inverter, $V_{GS1} = V_0$ and $V_{SG2} = (V_{DD} - V_0)$, where V_0 indicates the inverter output voltage.

Therefore (3.27) becomes:

$$\frac{1}{2}\mu_n C_{ox}\ \frac{W_n}{L_n}\ (V_0 - V_{tn})^2 = \frac{1}{2}\mu_p C_{ox}\ \frac{W_p}{L_p}\ (V_{DD} - V_0 - V_{tp})^2$$

Solving for V_0 :

$$(V_0 - V_{tn}) = \sqrt{\frac{\mu_p C_{ox} \frac{W_p}{L_p}}{\mu_n C_{ox} \frac{W_n}{L_n}}} (V_{DD} - V_0 - V_{tp})$$

Let $\sqrt{\frac{\mu_p C_{ox} \frac{W_p}{L_p}}{\mu_n C_{ox} \frac{W_n}{L_n}}} = r$;

$$(V_0 - V_{tn}) = r(V_{DD} - V_0 - V_{tp})$$

$$V_0 = \frac{r\left(V_{DD} - V_{tp}\right) + V_{tn}}{1 + r}, \qquad (3.28)$$

The dc output voltage of a given inverter based design can easily be found by using (3.28). For a given design, we can change the performance by increasing the width (W) of both transistors of the inverter structure, which leads to an increase in overall g_m, g_0 , C_F, $C_{GS1/2}$. If a fixed total width is used such as width of PMOS(W_p) + width of NMOS (W_n) = total width (W) then C_F, $C_{GS1/2}$ remains constant.

Now, the ratio W_n / W_p is found to maximize the g_m,

The NMOS and PMOS transcoductance g_{mn} and g_{mp} respectively can be written as

$$g_{mn} = \mu_n C_{ox} \frac{W_n}{L_n}(V_{GS1} - V_{tn}) = \mu_n C_{ox} \frac{W_n}{L_n}(V_0 - V_{tn})$$

$$g_{mp} = \mu_p C_{ox} \frac{W_p}{L_p}\left(V_{SG2} - |V_{tp}|\right) = r^2 \mu_n C_{ox} \frac{W_n}{L_n}(V_{DD} - V_0 - V_{tn}),$$

where, $r = \sqrt{\frac{\mu_p C_{ox} \frac{W_p}{L_p}}{\mu_n C_{ox} \frac{W_n}{L_n}}}$,

For a particular technology L_p and L_n is same therefore r can be written as, $r = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}$,

Total transconductance g_m becomes:

$$g_m = g_{mn} + g_{mp} = \mu_n C_{ox} \frac{W_n}{L_n} \left(V_0 - V_t + r^2 (V_{DD} - V_0 - V_t)\right),$$

$$assuming,\ V_{tn} = V_{tp} = V_t$$

Substituting for V_0 and simplifying,

$$g_m = \mu_n C_{ox} \frac{W_n}{L_n} r (V_{DD} - 2V_t)$$

$$g_m = \frac{\mu_n C_{ox}}{L_n} (V_{DD} - 2V_t)(W_n r)$$

Taking the derivative with respect to W_n,

$$\frac{dg_m}{dW_n} = \frac{\mu_n C_{ox}}{L_n} (V_{DD} - 2V_t)(r + W_n \frac{dr}{dW_n})$$

Assuming, $\left(r + W_n \frac{dr}{dW_n}\right) = 0$,

For the maximum or minimum value derivation is set at 0. Therefore, we can write,

$$\frac{dr}{dW_n} = 0 \qquad (3.29)$$

Substituting, $r = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}$ in (3.29), we get:

$$\frac{dr}{dW_n} = \frac{d}{dW_n}\sqrt{\frac{W_p\mu_p}{W_n\mu_n}} = -\sqrt{\frac{\mu_p}{W_n W_p \mu_n}}, \qquad as \quad \frac{dW_p}{dW_n} = -1$$

Now from $\left(r + W_n \frac{dr}{dW_n}\right) = 0$, we can write:

$$r + W_n \frac{dr}{dW_n} = \sqrt{\frac{W_p\mu_p}{W_n\mu_n}} - W_n\sqrt{\frac{\mu_p}{W_n W_p \mu_n}} = 0$$

$$\sqrt{\frac{W_p\mu_p}{W_n\mu_n}} = \sqrt{\frac{W_n\mu_p}{W_p\mu_n}}$$

$$\frac{W_p\mu_p}{W_n\mu_n} = \frac{W_n\mu_p}{W_p\mu_n}$$

$$W_n = W_p \qquad (3.30)$$

From the analysis and (3.30), it is clear that if the sizes of the PMOS (W_p) and NMOS (W_n) are made equal, the gain bandwidth product of an inverter structure becomes larger with an optimum dc bias voltage. A swept simulation is also done to find out the value of this optimum sizing of the transistors. From simulation, 30um/60nm is found as the optimum size for the both PMOS and NMOS in the receiver front-end chain when the input capacitance is *100 fF* as shown in Figure 3.28. From this figure, if R_F = *150* Ω then the maximum gain bandwidth product is at *60μm,* where *Wp=Wn=30μm.*

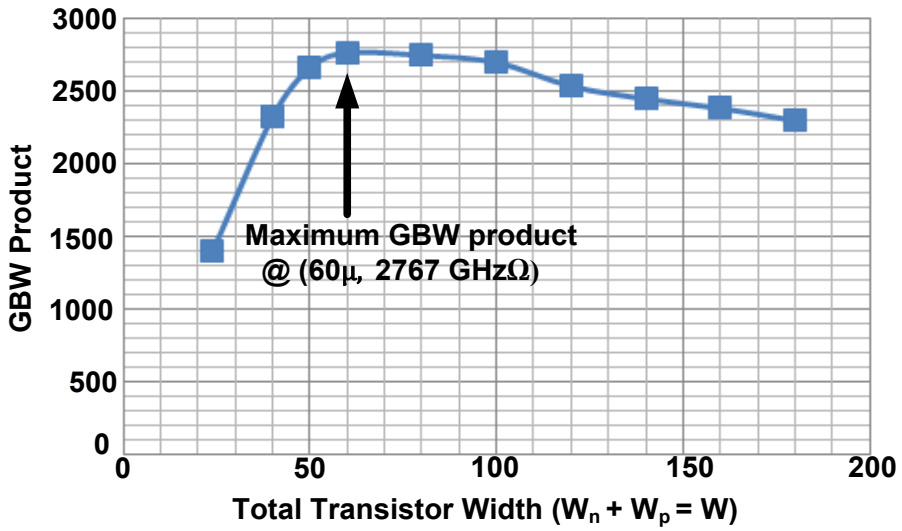

Figure 3.28: Gain Bandwidth product with respect to total transistor width.

At the last stage of the receiver front-end chain, an feedback inverter is included as shown in Figure 3.27, which supplies the compensated current to the TIA, working as an input transconductance. The sizing of this feedback inverter should be kept small so that it does not load significantly the input of the TIA.

In order to observe the changes in the low frequency poles and zeros of this inverter based optical receiver front-end the close loop transfer function is derived and given in below:

Close loop transfer function of a system can be written as,

$$H(s) = \frac{A}{1 + A\beta}\,, \qquad (3.31)$$

where, A is the open loop gain, β is the feedback factor.

A = TIA gain * (Post-Amplifier gain)^3,

$$A = \left(\frac{1 - g_{m1}R_F}{g_{m1} + g_{ds1}}\right)\left(g_{ma}R_F - \frac{g_{ma}}{g_{mb}}\right)^3, \quad (3.32)$$

where, g_{m1} is the overall transcondutance of TIA, g_{ds1} is the overall channel conductance of TIA, g_{ma}, g_{mb} is the overall transconductance of 2-stage cascaded post-amplifier, respectively, R_F is the feedback resistance of both TIA and post-amplifiers.

The passive low pass filter is actually working as a non-ideal integrator.

For the Design 2,

β = Gain of the non- ideal integrator * transcoductance of the feedback inverter ($g_{m,inv}$)

Now, the gain of an integrator A_{int} becomes,

$$A_{int} = -\frac{1}{RCs\left(1 + \frac{1}{g_{m,int}r_{0,int}}\right) + \frac{1}{g_{m,int}r_{0,int}}}, \quad (3.33)$$

where, $g_{m,int}$ and $r_{0,int}$ indicates the overall transcodutance and the channel resistance of this non-ideal integrator, R and C = passive resistance and capacitance used in the offset compensation block.

If the product of $g_{m,int}$ and $r_{0,int}$ $(g_{m,int}r_{0,int})$ goes to ∞, then the A_{int} becomes,

$$A_{int} = -\frac{1}{RCs},$$

which is same as an ideal integrator circuit.

Now,

$$\beta = A_{int} * g_{m,inv}$$

$$\beta = \frac{-g_{m,inv}}{RCs\left(1+\frac{1}{g_{m,int}r_{0,int}}\right)+\frac{1}{g_{m,int}r_{0,int}}} \qquad (3.34)$$

Again ,

$$H(s) = \frac{A}{1+A\beta}$$

$$H(s) = \frac{A}{1-\frac{A\,g_{m,inv}}{RCs\left(1+\frac{1}{g_{m,int}r_{0,int}}\right)+\frac{1}{g_{m,int}r_{0,int}}}} \qquad (3.35)$$

$$H(s) = \frac{A\left(RCs\left(1+\frac{1}{g_{m,int}r_{0,int}}\right)+\frac{1}{g_{m,int}r_{0,int}}\right)}{RCs\left(1+\frac{1}{g_{m,int}r_{0,int}}\right)+\frac{1}{g_{m,int}r_{0,int}}-A\,g_{m,inv}} \qquad (3.36)$$

This equation (3.36) contains one pole (ω_p) and one zero (ω_z),

For an ideal integrator equation (3.36) becomes,

$$H(s) = \frac{A\,RCs}{RCs\ -A\,g_{m,inv}}$$

Now, the Pole location ω_p from the equation (3.36) at low frequency,

$$\omega_p = \frac{\left(A\,g_{m,inv}-\frac{1}{g_{m,int}r_{0,int}}\right)}{RC\left(1+\frac{1}{g_{m,int}r_{0,int}}\right)} \qquad (3.37)$$

From the simulation is found that open loop gain A and $g_{m,int}r_{0,int}$ is approximately fixed at all data rates, therefore, the pole location changes due to the change in $g_{m,inv}$ (feedback inverter transconductance)

Now, the zero ω_z becomes,

$$\omega_z = -\frac{\left(\frac{A}{g_{m,int}r_{0,int}}\right)}{ARC\left(1+\frac{1}{g_{m,int}r_{0,int}}\right)}$$

If open loop gain A and $g_{m,int}r_{0,int}$ is fixed at all the data rates then the low frequency zero location is also fixed.

Table 3.6 shows a list of low frequency pole locations and zeros at different data rates. From the Figure 3.29 changing poles and zeros locations can also be found.

Table 3.6: Low frequency Pole and Zero locations at different data rates

Data Rates (Gb/s)	$g_{m,int}r_{0,int}$	$g_{m,inv}$ (mA/V)	ω_p	ω_z
20	6.00	13.4	$1*10^8$	$2*10^5$
15	6.07	11.3	$0.83*10^8$	$2*10^5$
10	6.05	6.47	$0.48*10^8$	$2*10^5$
5	6.00	2.31	$0.17*10^8$	$2*10^5$
2.5	5.90	0.95	$0.7*10^7$	$2*10^5$
1.25	5.76	0.56	$3.8*10^6$	$1.8*10^5$

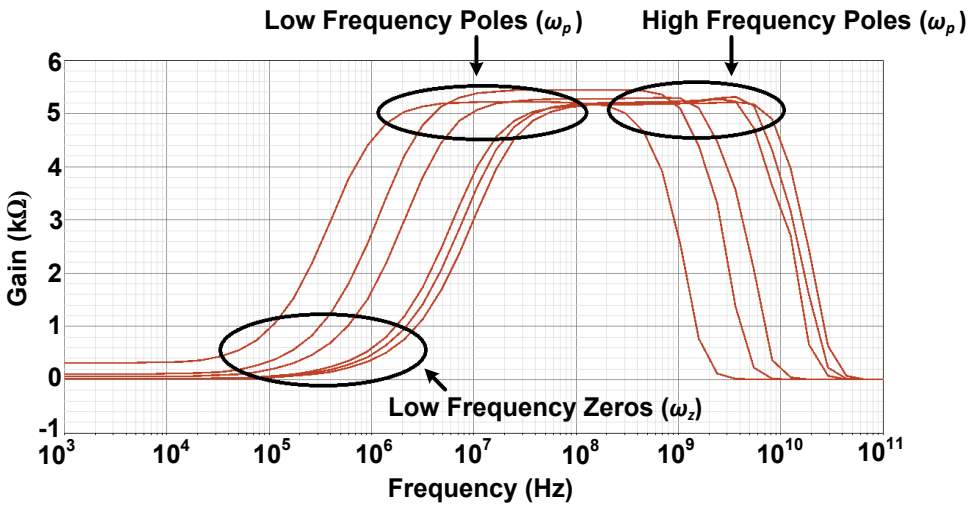

Figure 3.29: Low frequency poles and zeros location

From the simulation, it is also found that the feedback inverter transconductance $(g_{m,inv})$ is scaling when the data rate is scaling. Figure 3.30 shows the scalable transconductance of feedback inverter with respect to data rates.

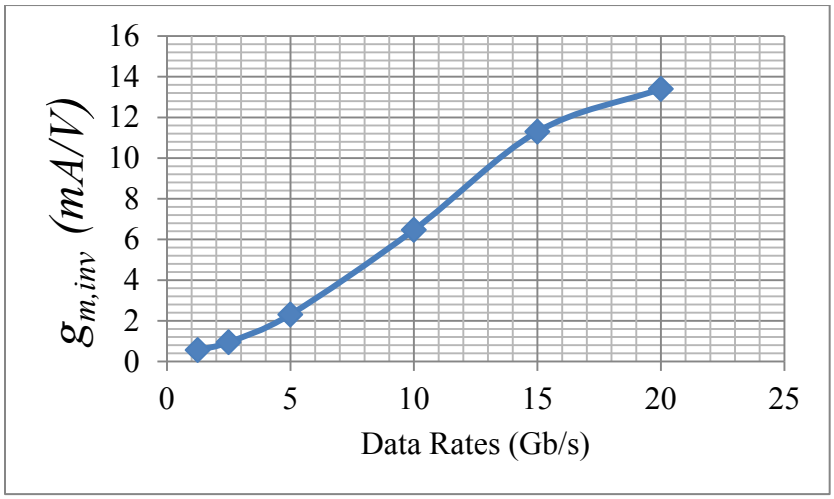

Figure 3.30: Feedback inverter transconductance with respect to data rates

For the further understanding, a chart of effective VDD (due to the binary weighted PMOS array scaling) at each datarate along with the dc bias voltage and maximum allowable input current is presented in Table 3.7. From the table, it is clear that the receiver chain starts operate at weak inversion at lower data rates due to its lower bias voltage. Therefore, the maximum allowable peak to peak input current is reduced at lower data rate to avoid the overaloading problems.

Table 3.7: Effective VDD, Bias Voltage and Maximum Allawable Input Current

Supply Voltage = 1 V						
Data rates (Gb/s)	1.25	2.5	5	10	15	20
Effective VDD (mV)	475	512	617	762	905	980
Bias Voltage (mV)	200	230	273	343	420	480
Maximum Allowable Input Current (μA_{pp})	30	30	35	50	50	50

3.14 Design Methodology

In this section, a design methodology will be discussed which can be helpful for redesigning this topology in a smaller technology (e.g. 45nm, 22nm CMOS technology). Working in smaller technology will enable this design to operate at higher speed with lower supply voltage.

1) The PMOS and NMOS of the inverter structure should be sized equally as derived. For achieving the maximum gain bandwidth product for a small technology some simulations have to be run with a fixed R_F.
2) In this design the input to output capacitance ratio was *~3.33* times. For a small load capacitance the post-amplification stages can be tapered down, which eventually helps to reduce the overall power dissipation.
3) In order to operate the design at high speed, a bandwidth extension method can be applied (e.g. inductive feedback).
4) For this design, the assumed input capacitance was *100 fF*, if the front-end has to load more than *100 fF* at the input then the sizes of the TIA has to be re-investigated because increasing input capacitance effects the circuit bandwidth at high speed.

3.15 Conclusion

The design of a variable-bandwidth, power-scalable optical receiver front-end in 90nm and 65nm CMOS along with in-depth descriptions and analysis of its individual components have been presented. The receiver front-end incorporates an inverter-based shunt feedback TIA and post-amplifiers with a tuning mechanism for variable data rates (1.25 Gb/s to 20 Gb/s). The benefits and drawbacks of both the designs were also presented.

Chapter 4

4. Simulation & Layout

4.1 Simulated Results of Design 1

In this section, the simulated results of Design 1 will be presented.

4.1.1 Frequency Response

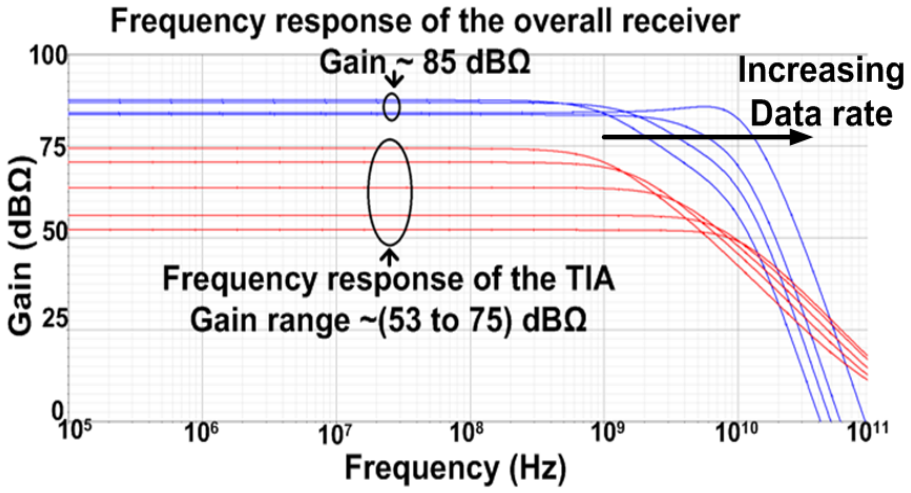

Figure 4.1: Frequency response of the overall receiver front-end.

Figure 4.1 shows the frequency response of the overall receiver front-end designed in 90nm CMOS. The TIA gain varies from 53 dBΩ to 75 dBΩ when the data rate changes from 15 Gb/s to 1.25 Gb/s. The overall gain is fixed at ~85 dBΩ.

4.1.2 Noise Response

The overall noise analysis is shown in Figure 4.2. The input referred noise varies from 4.31pA/√Hz to 14.3 pA/√Hz when the data rate scales up from 1.25 Gb/s to 15 Gb/s.

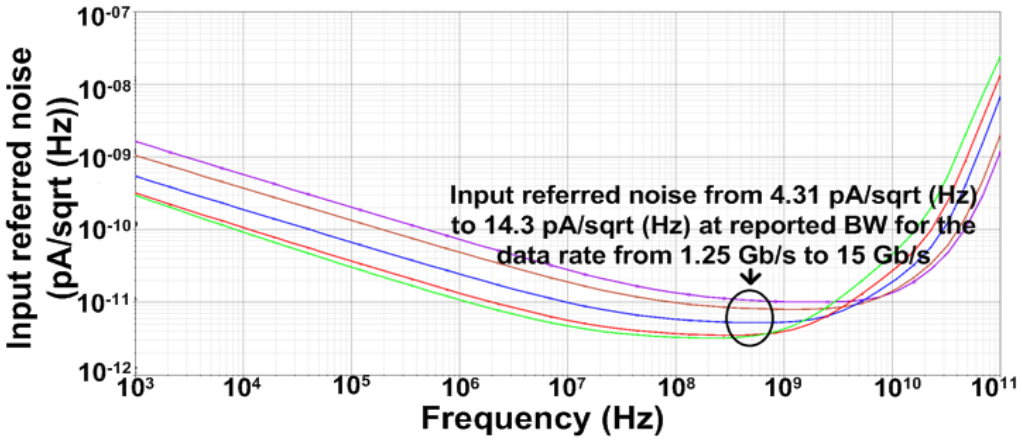

Figure 4.2: Input referred noise of the overall receiver.

4.1.3 Response Time for Reconfiguration

Response time for reconfiguration is one of the most important simulations. As discussed earlier, in order to get a rapidly configurable link, it is important to change the data rate as fast as possible. A test setup circuit for this simulation is shown in Figure 4.3 and Table 4.1 shows the voltages and their respective switching times for different PWL sources, denoted as VPWL1, VPWL2 and VWPL3. Design 1 shows quite a fast response time while changing the data rates from 1.25 Gb/s to 20 Gb/s. Figure 4.4 shows the response time for reconfiguration at steady state. The TIA takes around 125 ps when the data rate changes from 1.25 Gb/s and 15 Gb/s whereas the overall receiver takes 297 ps to reconfigure which is less than 5 unit interval (UI) of the highest data rate.

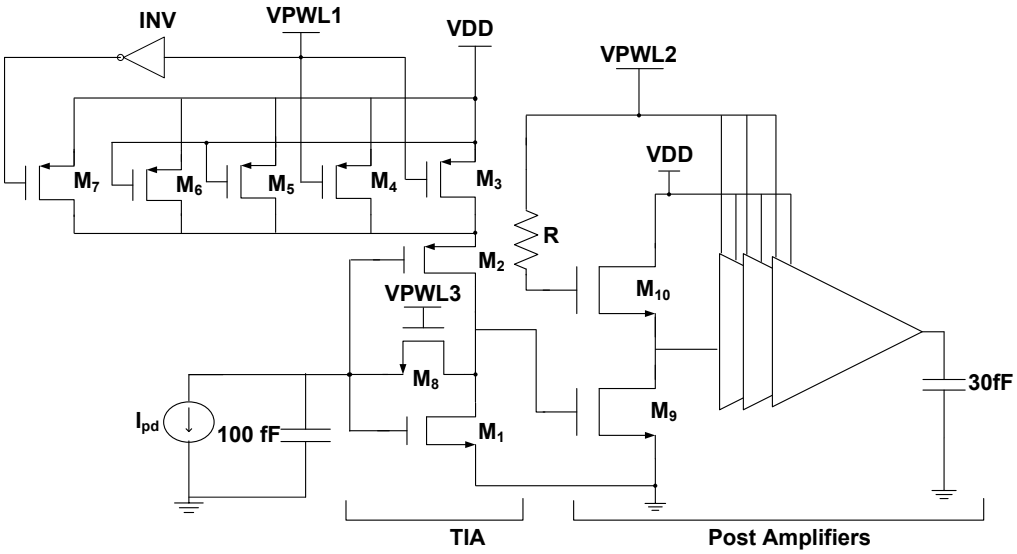

Figure 4.3: Test setup circuit for the response time simulation

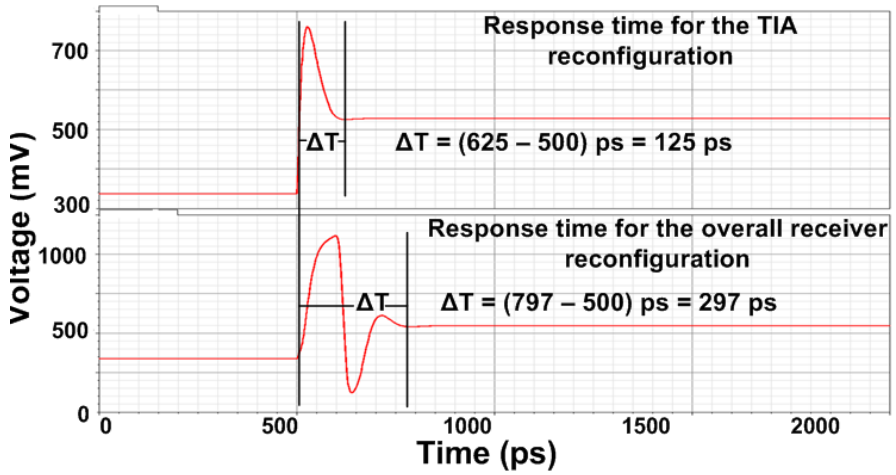

Figure 4.4: Response time for the reconfiguration.

Table 4.1: Voltages and their respective switching time of PWL sources

Sources	VPWL1	VPWL2	VPWL3
Voltage 1 (V)	1.2	1.2	1.6
Volatge 2 (V)	0	0.65	0.55
Switching time (ps)	500	500	500
Note	M_3 & M_4 sets the bias point for 15 Gb/s data where M_7 sets the bias point for 1.25 Gb/s data. The input current magnitude for this simulation is fixed at 0 A		

4.1.4 Power-Scalability

The main goal of this design is to make the receiver front-end power-scalable with respect to the data rate. Figure 4.5 shows the power-scalability with respect to the data rates. This figure shows how power dissipation changes as the data rate varies from 1.25 Gb/s to 15 Gb/s . The energy per bit decreases as the data rate is increased up to 5 Gb/s where it remains approximately constant up to 15 Gb/s.

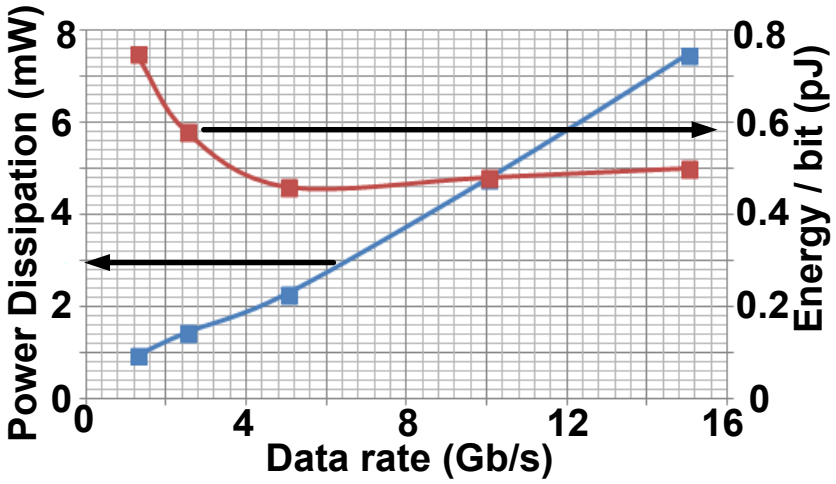

Figure 4.5: Power-scalability and energy / bit with respect to data rate.

4.1.5 TIA and Overall Receiver Performance Summary

Table 4.2: TIA performance summary of Design 1

Data rate (Gb/s)	1.25	2.5	5	10	15
TIA Gain (dBΩ)	74.3	70.5	63.6	56.1	52.2
TIA Bandwidth (GHz)	0.87	1.48	3.08	6.62	9.81
Input Referred Noise (pA/√(Hz))	3.48	3.89	6.04	10.0	12.8
Input Referred RMS Noise (μA_{rms})	0.09	0.14	0.32	0.87	1.06
Power Dissipation (mW)	0.15	0.27	0.50	1.16	1.88

Table 4.3: Overall receiver front-end performance summary of Design 1

Data rate (Gb/s)	1.25	2.5	5	10	15
Gain (dBΩ)	83.6	84.4	83.1	84.3	84.3
Bandwidth (GHz)	0.89	1.56	3.92	8.91	10.8
Input Referred Noise (pA/√(Hz))	4.31	4.88	8.35	12.9	14.3
Input Referred RMS Noise (μA_{rms})	0.12	0.15	0.42	0.98	1.25
Power Dissipation (mW)	0.94	1.44	2.28	4.76	7.46
Energy (pJ/bit)	0.75	0.58	0.46	0.48	0.50

The TIA and overall performance summaries are shown in Table 4.2 and 4.3. From the tables, as data rate is varied from 1.25 Gb/s to 15 Gb/s, the overall gain remains ~ 84 dBΩ. The bandwidth is approximately 70% of the data rates. Power dissipation of the TIA is exactly proportional to the data rates, whereas for the overall front-end there is some non-linearity (not exactly same as the data rate scaling) due to the post-amplifiers' power dissipation.

4.2 Simulated Results of Design 2

The simulated results of Design 2 will be presented here.

4.2.1 Frequency Response

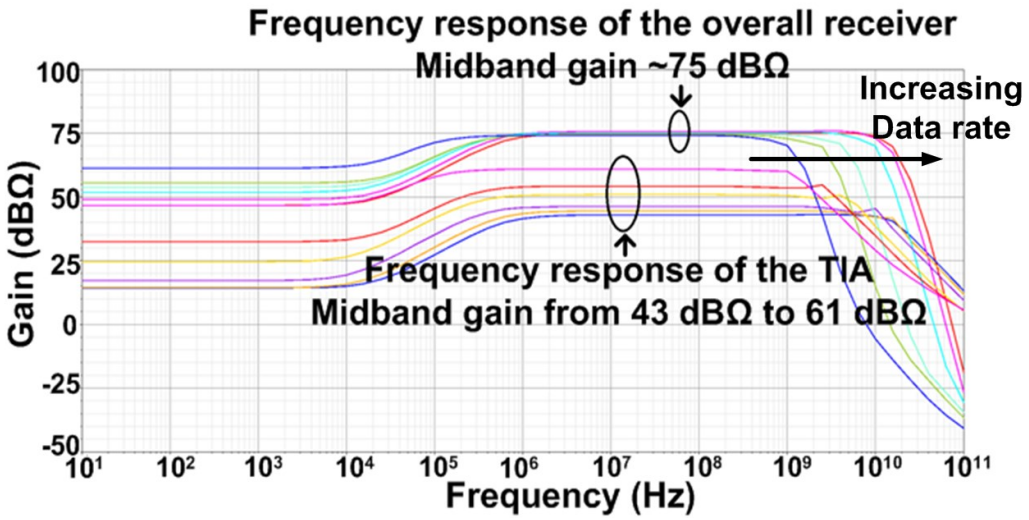

Figure 4.6: Frequency response of the overall receiver designed in 65nm CMOS.

Figure 4.6 shows the frequency response of the receiver front-end designed in 65nm CMOS. TIA gain varies from 43 dBΩ to 61 dBΩ, whereas the overall receiver has fixed gain of ~ 75 dBΩ while the data rate changes from 1.25 Gb/s to 20 Gb/s.

4.2.2 Noise Response

Overall noise response of the receiver front-end is shown in Figure 4.7 The input referred noise varies from 8.46 pA/√ Hz to 18 pA/√ Hz when the data rate ranges from 1.25 Gb/s to 20 Gb/s.

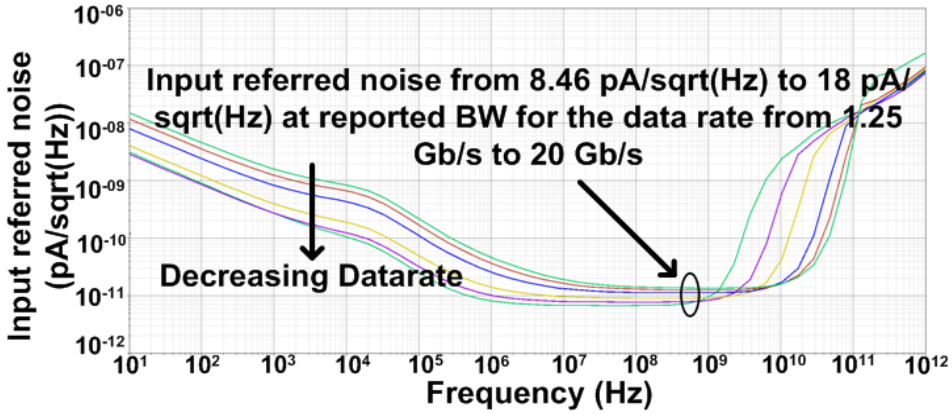

Figure 4.7: Input referred noise of the overall receiver.

4.2.3 Response Time for Reconfiguration

This simulation shows the rapid reconfigurability of the receiver front-end with respect to the changing data rates. The response time for reconfiguration is shown in Figure 4.8. For the TIA it takes 60 ps for the operating point to settle (~ 95% settling time) whereas for the overall receiver takes 500 ps while the data rate scales up from 1.25 Gb/s to 20 Gb/s. For the highest (20 Gb/s) to lowest (1.25 Gb/s) data rate switching the TIA takes 0.55 ns whereas the overall receiver takes 1.5 ns.

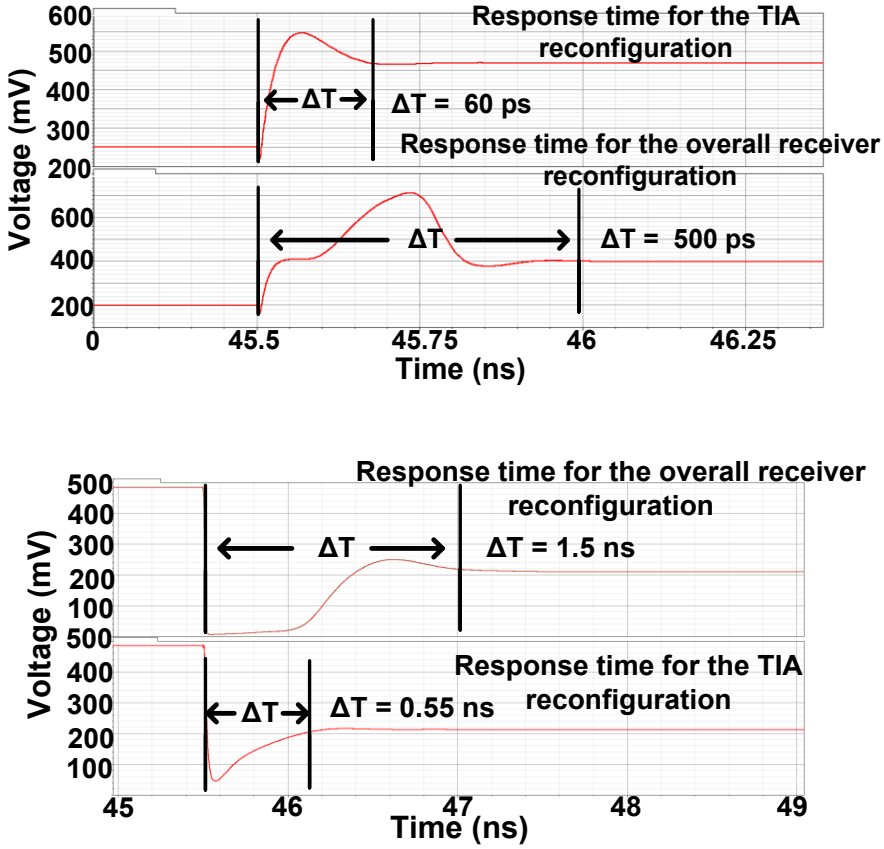

Figure 4.8: Response time for the reconfiguration.

4.2.4 Power-Scalability

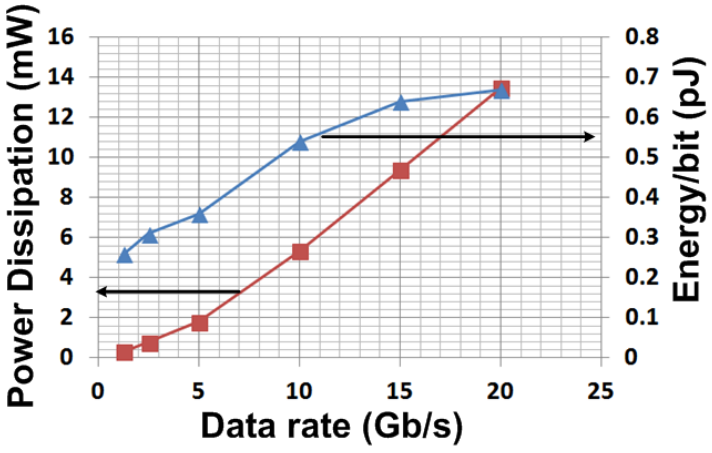

Figure 4.9: Power- scalability and energy/bit with respect to data rate.

Figure 4.9 shows the power-scalability with respect to the data rates. Data rates are varied from 1.25 Gb/s to 20 Gb/s and the corresponding power dissipation is shown in Figure 4.9. The topology of the post-amplifier used in Design 2 helps to make it more power-scalable than the Design 1 with respect to data rate.

4.2.5 Eye Diagram

The eye diagram of the overall receiver was drawn from a random data source. At 20Gb/s data rate the input is fixed at $30\mu A_{pp}$ and the output becomes 175 $mV_{pp.}$ For the input current $80\mu A_{pp}$ the output becomes $465mV_{pp}$ as shown in Figure 4.10. Both the eyes have a little amplitude peaking. It is due to the nearby poles found at high frequency. The eye diagram is also drawn while the data rate is switching as shown in Figure 4.11. In this figure, the first eye diagram was drawn at 1.25 Gb/s, then after immediate switching (at 45.5 ns) and at last after settling down at 20 Gb/s data rate (at 46 ns), respectively. The eye diagam after the immediate switching (45.5 ns) shows severe ISI but after 46 ns the eye is quite open. This means that in the presence of an applied signal, the front-end requires 500 ps to settle.

For the decision circuit sampling, a differential transient output is taken from the feedback and its preceding stage of the PA. An eye diagram is also drawn from this output shown in Figure 4.12. Figure 4.13 shows another eye diagram where the relative time delay (~ 0.03ns) is shown from input to output.

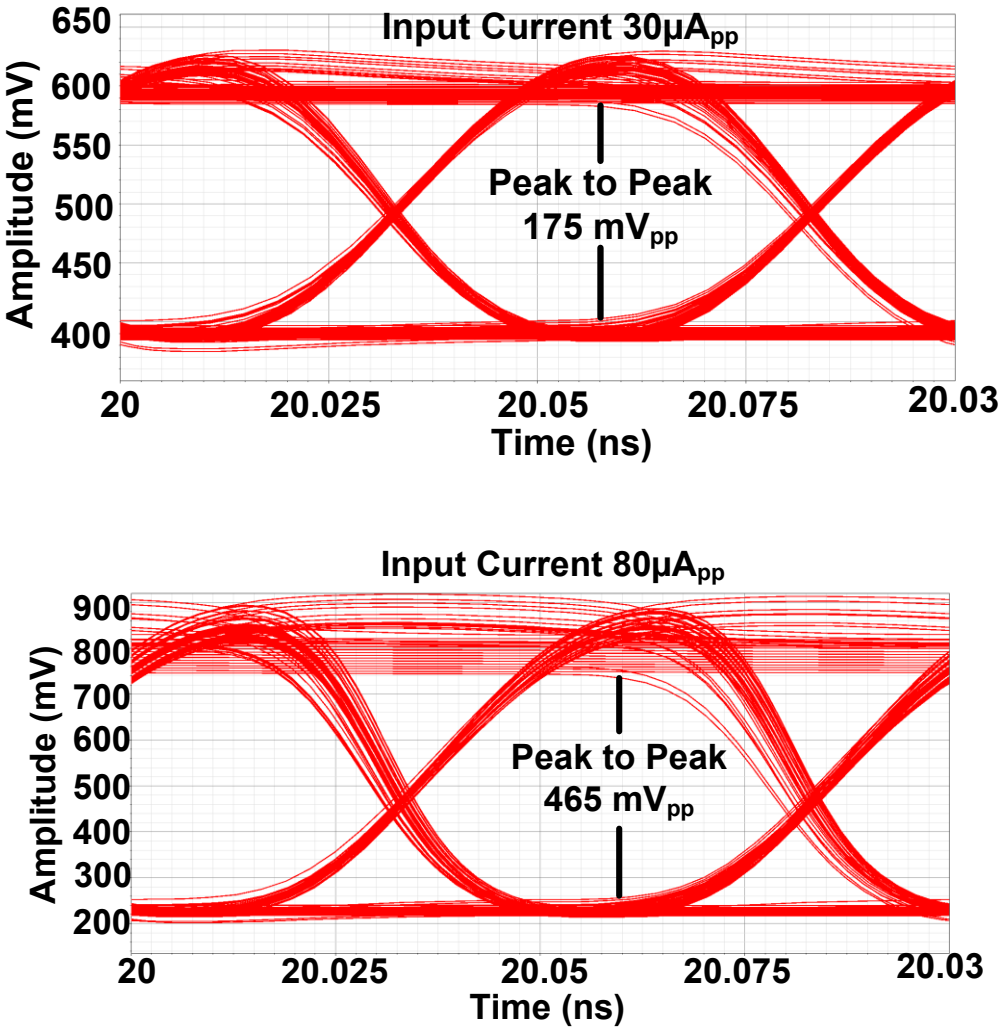

Figure 4.10: Eye diagram of the overall receiver from a random sequence at 20 Gb/s data.

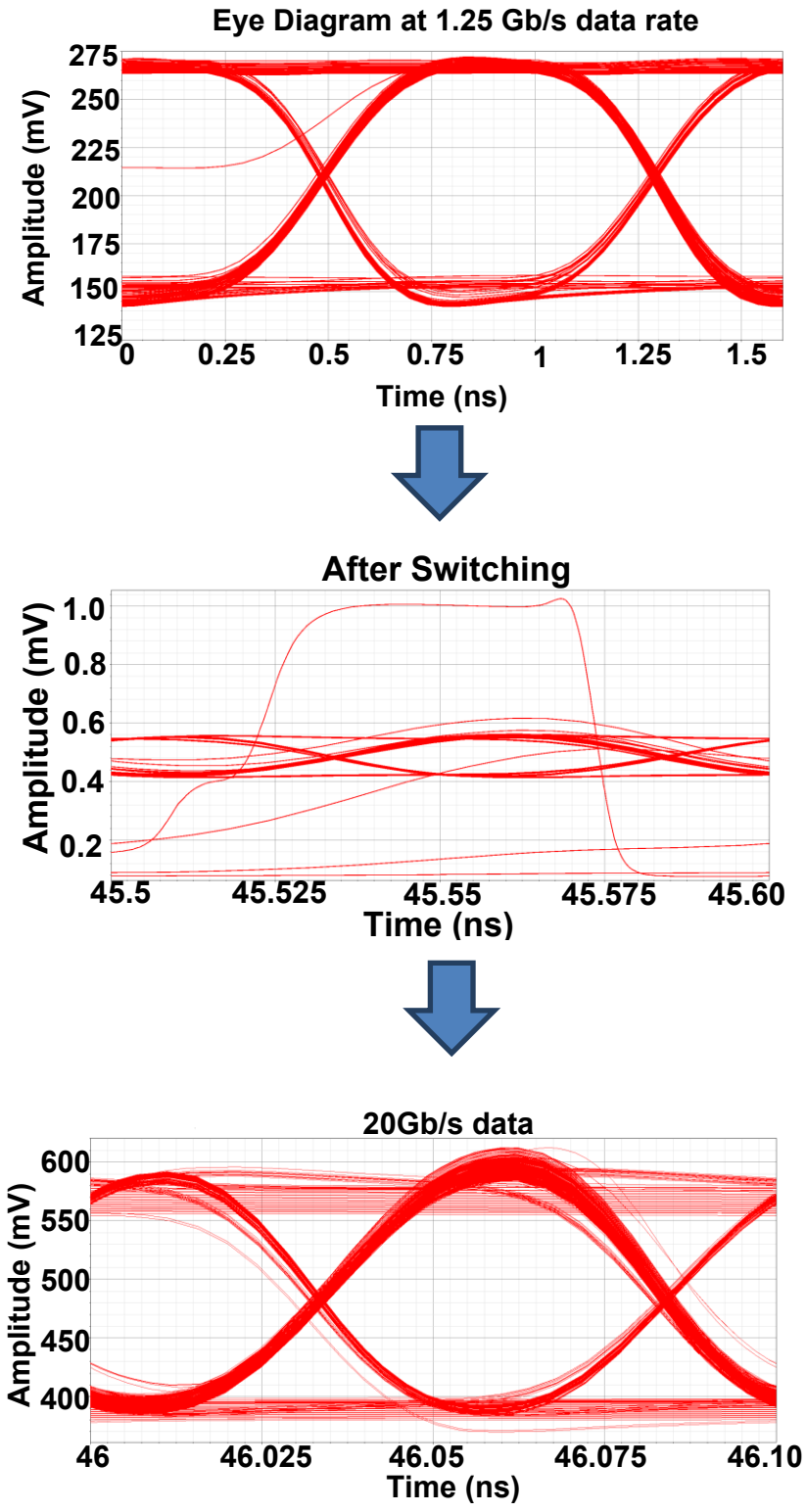

Figure 4.11: Eye diagram while data rate is changing. The data rate changes from 1.25 Gb/s to 20 Gb/s at 45.5 ns

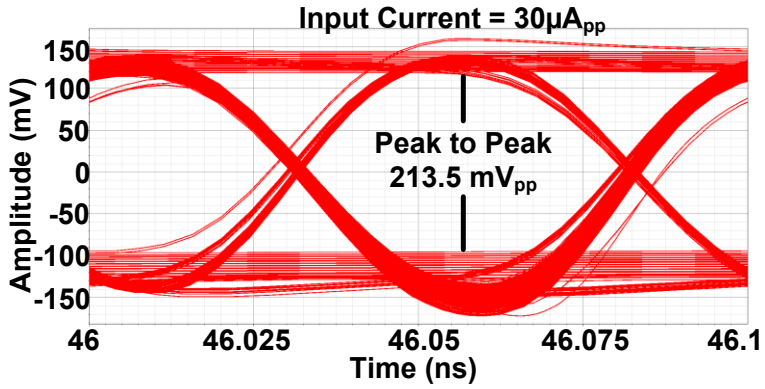

Figure 4.12: Eye diagram from the differential output for the latch

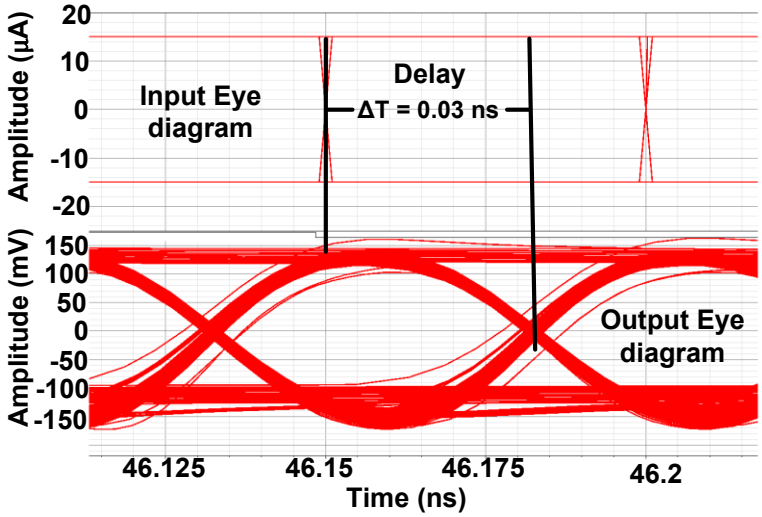

Figure 4.13: Delay from input to output

4.2.6 Robustness

As discussed in chapter 3, Design 1 is not robust because it does not incorporate an offset compensation technique. On the other hand, the current controlling PMOS array does not have wide tunable range and the tuneable resistance, due to low overdrive voltage at lower data rate suffers from severe global process variation.

In order to investigate the robustness of Design 2 against global process variation, a 1000-iteration Monte Carlo simulation was performed. For each set of process parameters, the overall receiver's gain and bandwidth were calculated. From the 1000 iterations, 25 representative data points of the distribution are shown in Figure 4.14 as blue triangle symbols. For this investigation, 65% of the data rate is the target specification for the bandwidth of the receiver [5]. However, a bandwidth of 50% of the data rate is sufficient and was taken as the hard limit for this specification. Performance that did not fall in the targeted specification zone was tuned by reconfiguring the binary weighted PMOS array and the resistance bank. These results are shown as red square symbols in Figure 4.14.

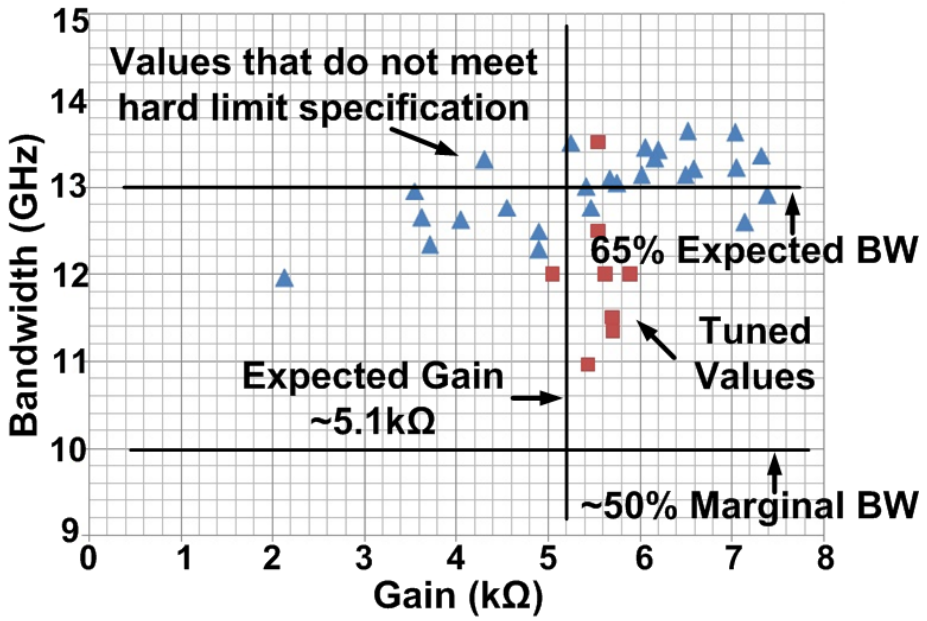

Figure 4.14: Tuning of performance that do not meet hard limit of specifications.

4.2.7 Overall Receiver Performance Summary

Table 4.4: Overall receiver front-end performance summary of Design 2

Data rate (Gb/s)	1.25	2.5	5	10	15	20
Gain (dBΩ)	74.1	74.3	74.8	75.1	74.9	74.5
Bandwidth (GHz)	0.86	1.83	3.78	7.14	10.3	13.1
Input Referred Noise (pA/(Hz))	8.46	10.0	11.6	14.4	15.6	18.0
Input Referred RMS Noise (μA_{rms})	0.26	0.35	0.63	1.21	1.57	1.89
Power Dissipation (mW)	0.32	0.78	1.82	5.35	9.41	13.5
Energy per bit (pJ)	0.26	0.31	0.36	0.54	0.63	0.67

The overall performance summary is shown in Table 4.4. From the table it can be seen that as data rates are varied from 1.25 Gb/s to 20 Gb/s the overall gain remains close to ~75 dBΩ. The bandwidth is around 60% to 70% of each data rate. Power dissipation of the overall receiver is also scaling with data rate.

4.3 Layout

The layout of Design 2 of the receiver front-end is completed in 65nm CMOS. For the standalone chip testing of the receiver front-end, a PMOS source follower buffer

is used. In order to measure the dc bias voltage at each data rate, a passive low pass filter is also incorporated in the design. Figure 4.11 shows the overall schematic diagram that is used for fabrication. The schematic contains TIA, PA, offset compensation, input transconductance, source follower buffer, passive low pass filter, latch, serial shift register pulse generator and voltage divider. The serial shift register which is supplied by the VDD_DIG (1V) is used to provide the control bits for binary weighted PMOS array and voltage divider. The layouts of the different blocks used in the front-end design are shown in Figures 4.12, 4.13 and 4.14. Figure 4.12 shows the layout of the TIA, post-amplifiers, output buffer and the resistance bank. The layout of binary weighted PMOS array (left) with the voltage divider (right) are shown in Figure 4.13. Figure 4.14 shows the pulse generator, passive low pass filter and the offset compensation block as well.

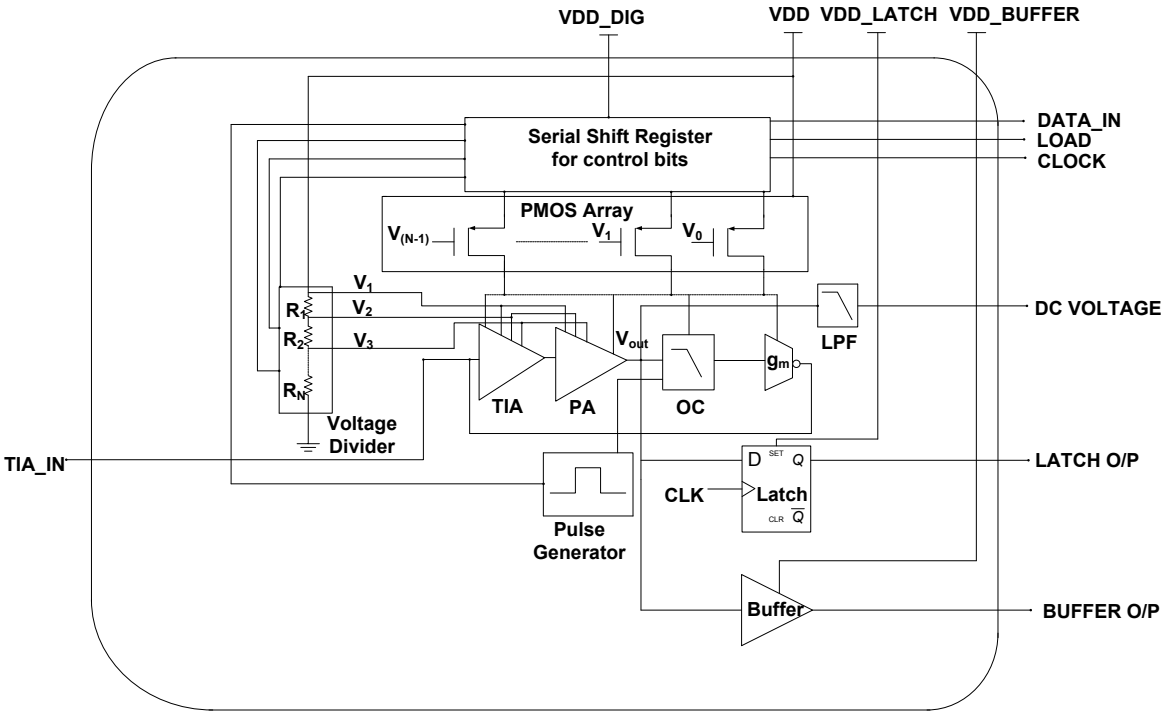

Figure 4.15: Overall schematic used for fabrication.

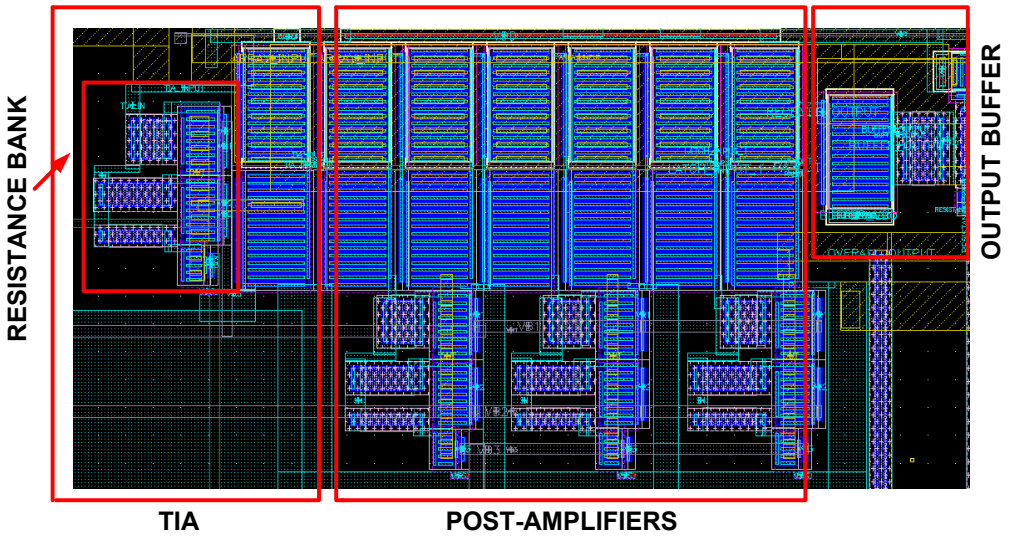

Figure 4.16: Layout of the TIA, Post-Amplifiers, Output buffers and Resistance Bank.

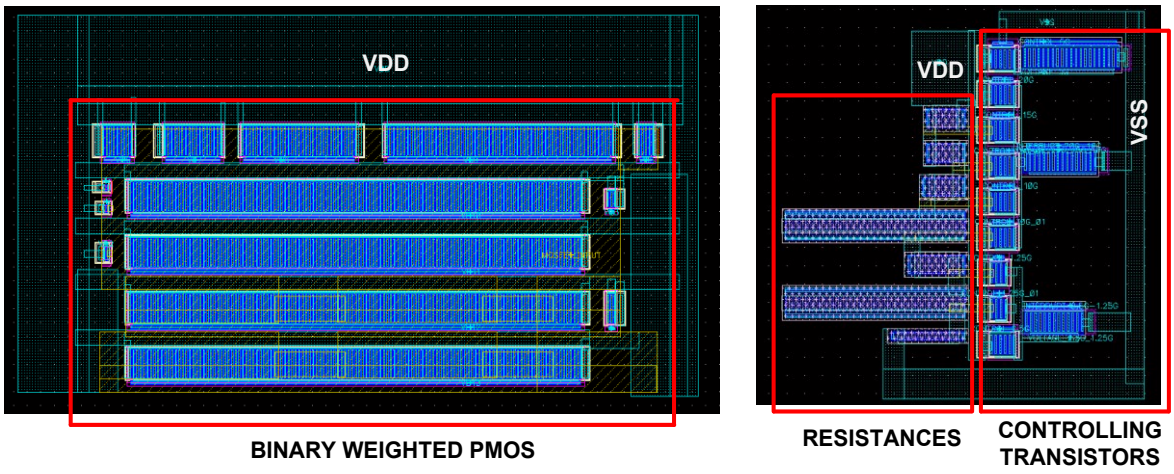

Figure 4.17: Binary weighted PMOS array (left) and the voltage divider (right).

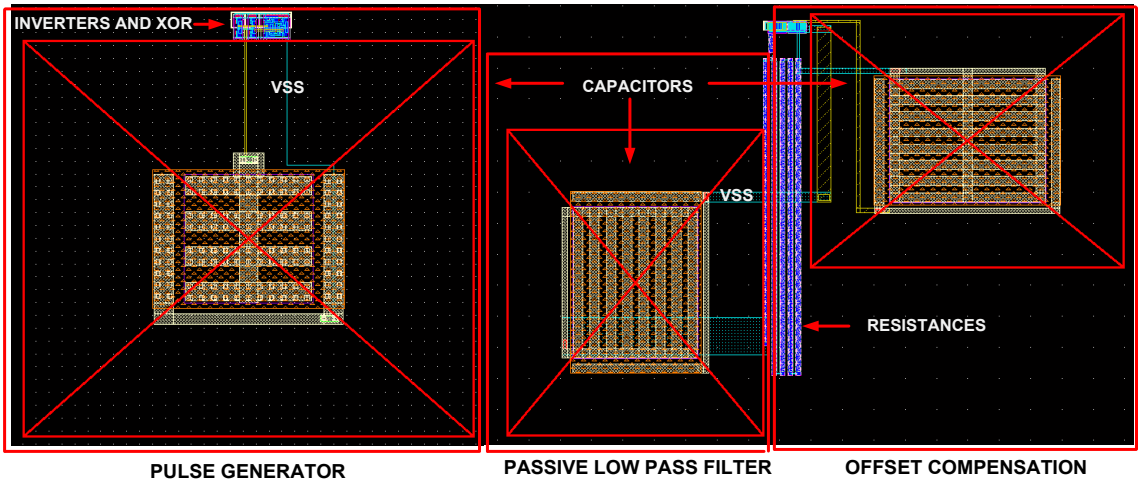

Figure 4.18: Pulse Generator (left), passive low pass filter (middle) & offset compensation (right).

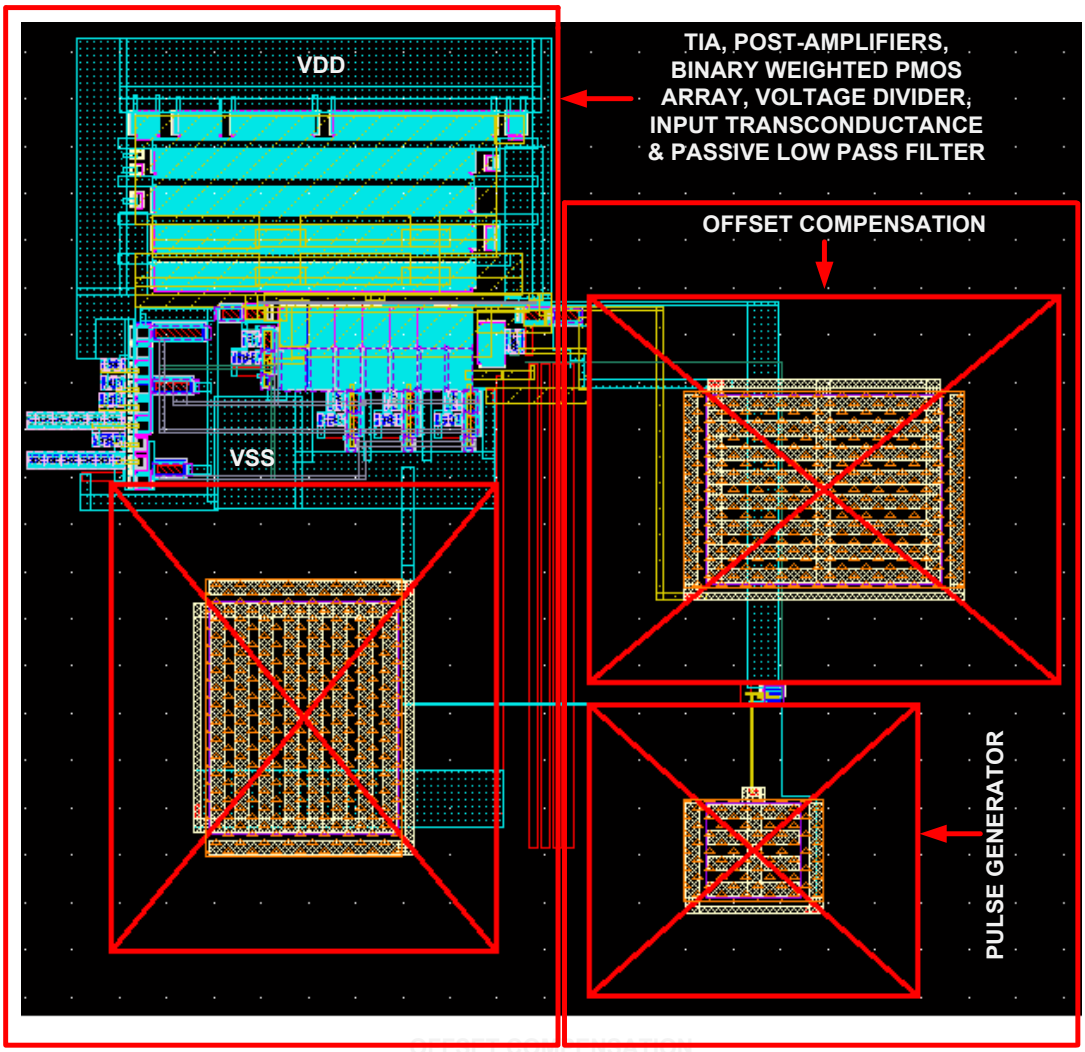

Figure 4.19: Overall receiver front-end chain layout.

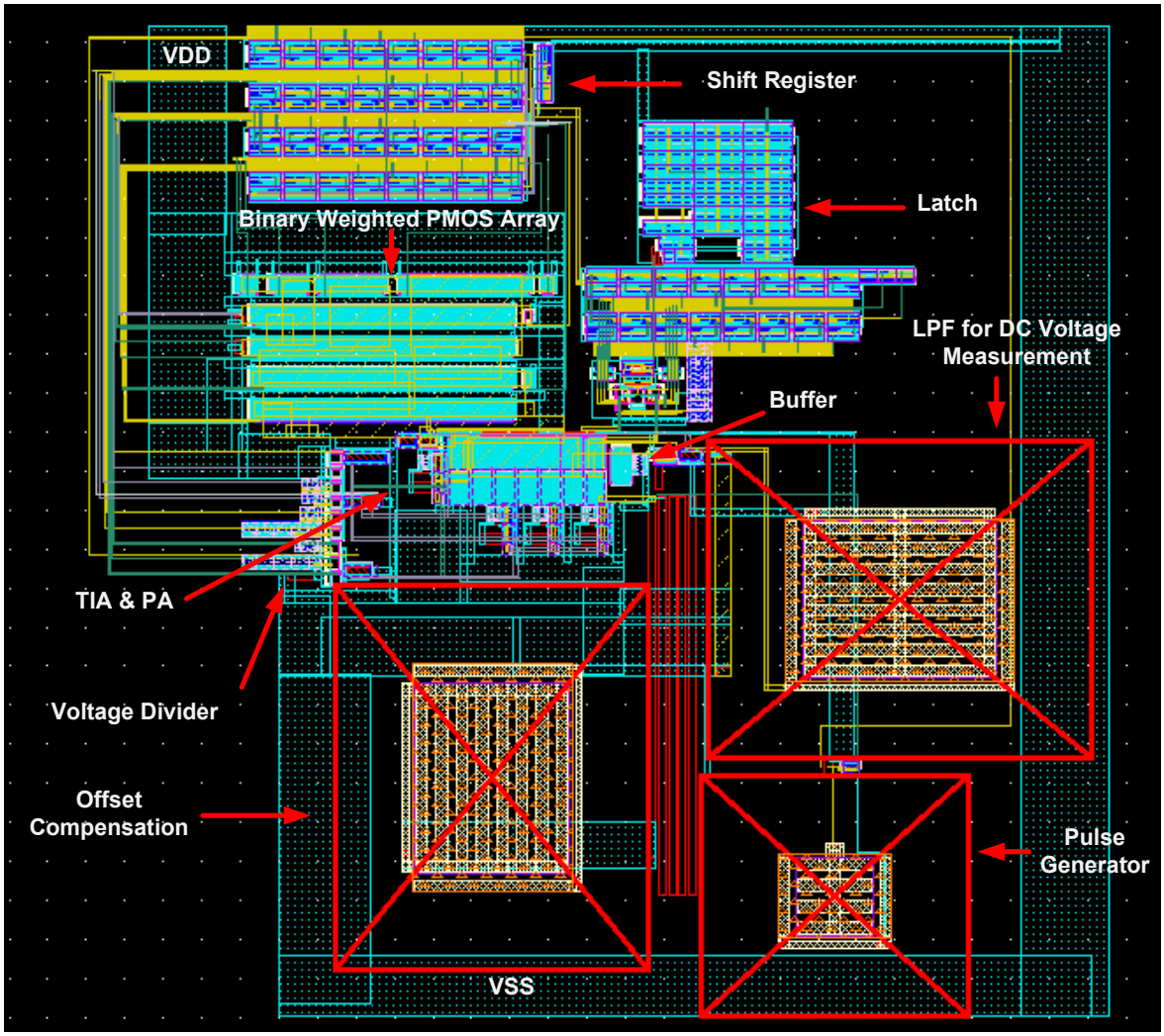

Figure 4.20: Overall receiver front-end with latch and buffer for standalone chip testing.

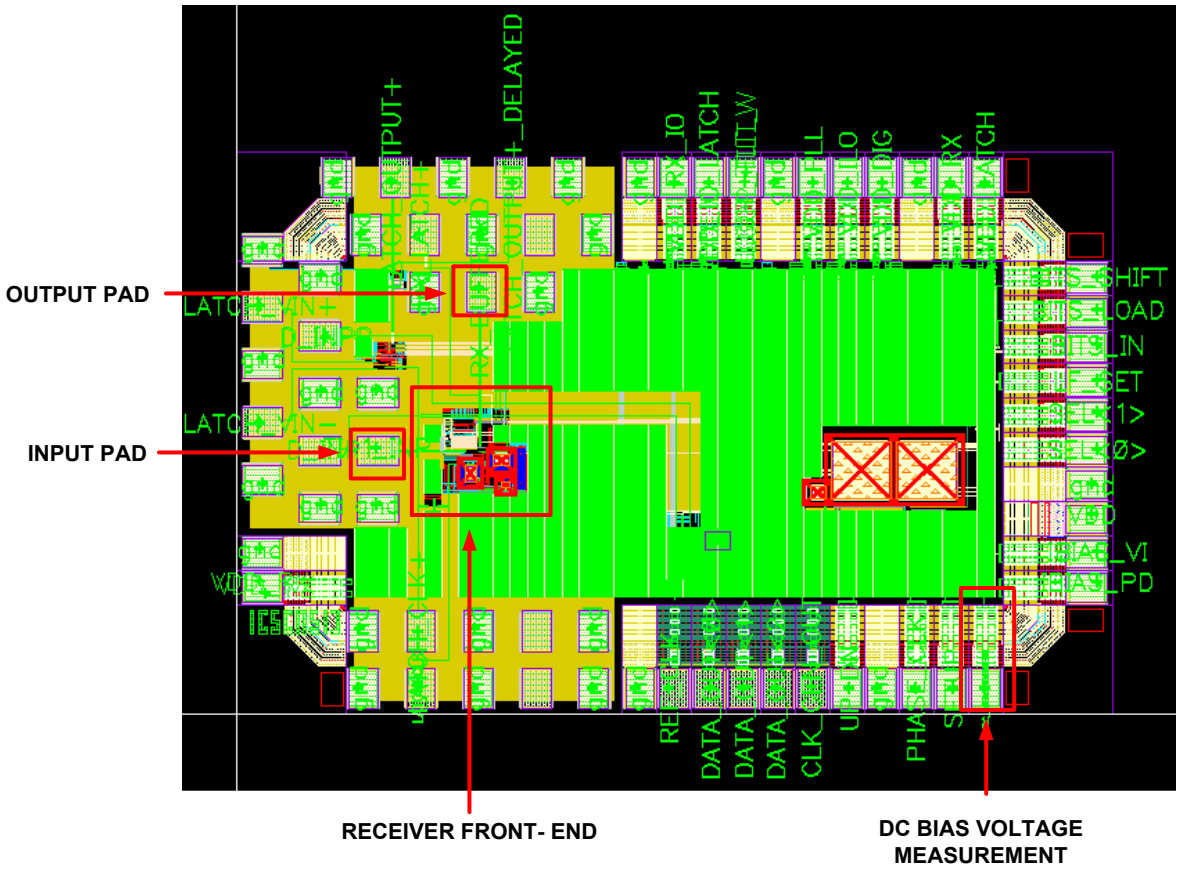

Figure 4.21: Layout of the front- end receiver with the pad ring & power grid.

Figure 4.19 shows the overall layout without the output buffer and latch. As discussed, for standalone chip testing receiver front-end is loaded with a source follower buffer and latch which is shown in Figure 4.20. The latch is designed by a PhD student (Monireh Moayedi) of our group. The dimention of the layout of total receiver front-end with latch and output buffer is ~ 136.40 µm by ~ 127.50 µm. Figure 4.21 shows the overall layout of the chip (pad ring & power grid) including our research group project with the receive front–end, which is illustrated by the red arrows. The serial shift register that is used for the control bits is designed by Michael Sagev. The par ring is designed by

Dr. Glenn Cowan and the power grid is designed by Michel Segev with the help of Dr. Glenn Cowan.

4.3.1 Parasitic Extracted Results

The overall performance of the receiver chain is hampered due to parasitic resistance and capacitance. The input and output capacitances increase due to adding extra ESD protection diodes in the receiver front-end chain. To support the receiver front-end at higher data rate with this extra capacitance, the overall supply voltage is boosted up from 1 V to 1.2 V. To reduce the parasitic resistive drop in VDD and VSS, the local supply and ground grid are made thicker. The connecting wire between different nodes is made moderately wide in order to have less parasitic capacitance and resistance. Some parasitic extracted results are shown in Figures. 4.22, 4.23 and 4.24. Figures 4.22 shows the overall frequency response supplied by 1.2 V, where the TIA gain ranges from 41 dBΩ to 60 dBΩ and overall receiver maintains a fixed gain of ~ 75 dBΩ. Figure 4.23 shows the response time for reconfiguration where TIA and overall receiver take 70 ps and 570 ps, respectively. The parasitic extracted response time is little bit larger than the simulated result because of the delay created by the parasitic capacitances. Power scalability with respect to data rate is also shown in Figure 4.24. The overall power dissipation is increased due to the boosted supply voltage. Table 4.5 shows the overall performance summary where the overall gain is fixed at ~75 dBΩ, bandwidth is slightly reduced due to the parasitic capacitance and resistance. Although power dissipation is increased due to boosted VDD, it still shows scalability with respect to data rates. This work is compared with other inductorless front-end design that are operated at fixed data rate. This comparison is shown in table 4.6. At 10 Gb/s the receiver front-end shows good

performance with less power dissipation where at 20 Gb/s the receiver shows same performance as the reference one with some extra power dissipation.

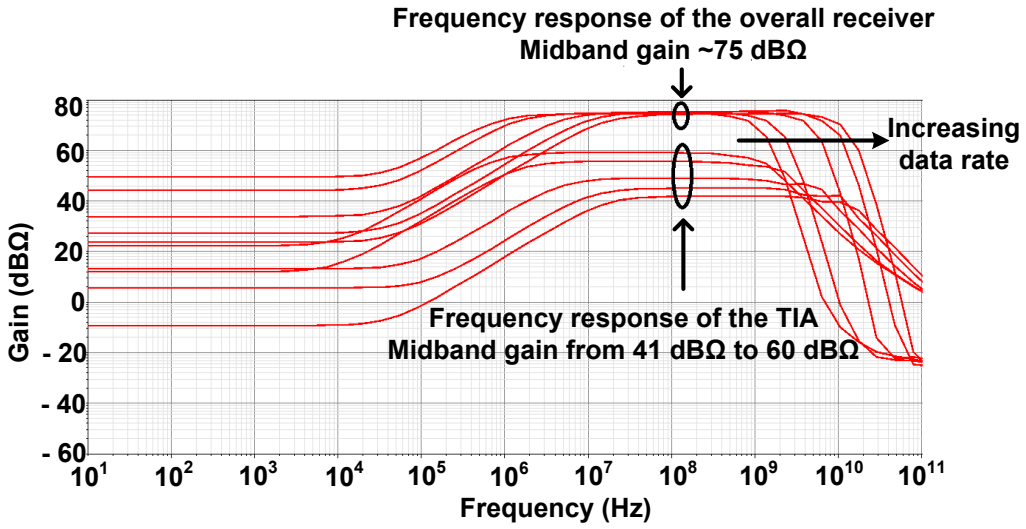

Figure 4.22: Frequency response of the overall receiver front-end in 65nm CMOS (parasitic extracted).

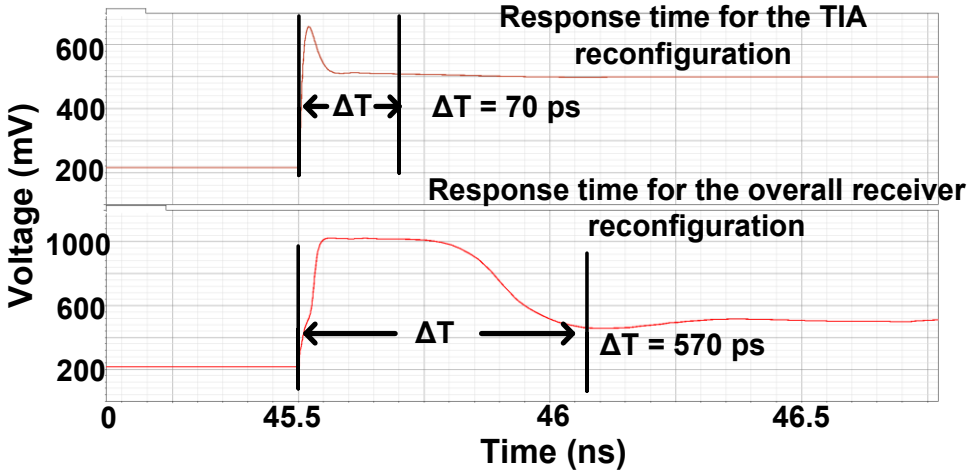

Figure 4.23: Response time for reconfiguration (parasitic extracted).

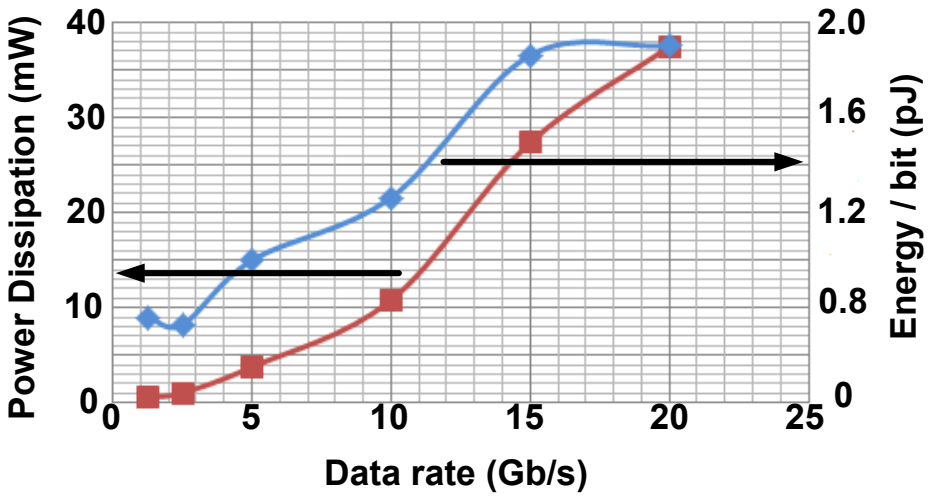

Figure 4.24: Power scalability and energy/bit with respect to data rate (parasitic extracted).

Table 4.5: Overall receiver front-end performance summary (parasitic extracted)

Data rate (Gb/s)	1.25	2.5	5	10	15	20
Gain (dBΩ)	74.4	74.7	75.1	75.3	74.3	74.2
Bandwidth (GHz)	0.86	1.39	3.49	5.51	8.80	10.5
Power Dissipation (mW)	0.56	1.03	3.76	10.8	27.4	37.5
Energy per bit (pJ)	0.45	0.41	0.75	1.08	1.83	1.88

Table 4.6: Comparison with other's work

References	[15]	[16]	[17]	This work	[12]	This work
Data rate (Gb/s)	10	10	10	10	20	20
Gain (dBΩ)	55	62	106	75.1	75.9	74.2
Bandwidth (GHz)	7	6	8.2	7.14	12	10.5
Input Referred Noise (pA/(Hz))	17.5	-	-	14.4	-	18
Input Referred RMS Noise (μA_{rms})	-	-	-	1.21	1.9	1.89
Power Dissipation (mW)	18.6	98	33.4	12	25.2*	37.5
Input Capacitance (pF)	0.2	0.25	1	0.12	0.08	0.12
Technology Used (nm)	180	130	130	65	90	65
Inductor Used	0	0	2	0	0	0
* Includes output buffer @ 1.2 supply voltage						

4.4 Conclusion

A comprehensive discussion in the simulated results based on Design 1 and Design 2 is presented alone with the layout and parasitic extracted result. The parasitic extracted result shows some degradation from the simulated one due to its parasitic capacitance and resistance.

Chapter 5

5. Conclusion & Future Work

Electrical links suffer significant signal attenuation while transmitting data whereas optical links have less attenuation. As short-reach links are not used maximally all the time, a rapidly configurable and tunable optical receiver front–end is a useful design goal.

5.1 Conclusion

We have introduced an optical receiver front-end for operation at variable data rates in two different technologies (90 nm CMOS and 65 nm CMOS) for short-reach applications. A comprehensive literature review of previous front-end topologies that are mainly used for a fixed data rate is given in Chapter 2. In Chapter 3, theoretical background of the receiver front-end is presented with the design topology. The individual components of the receiver front–end, namely, TIA, post-amplifiers, offset compensation, PMOS array, tunable resistance bank etc. designed in both 90nm and 65nm are presented. The performance criteria of these blocks such as noise, bit error rate, gain, bandwidth, eye-diagram, ISI are also described. The design technique of the tuneable inverter based shunt feedback TIA, CH single-ended post-amplifiers, conventional common-source based post-amplifiers, active offset compensation technique etc. designed in 90 nm and 65 nm also have been broadly discussed. The

bandwidth extension method used in 90nm CMOS with the help of active inductor was also presented.

Both of the proposed designs are area efficient owing to not using any spiral inductors. Since power dissipation scales with the data rate, the front-end gives good energy-per-bit performance across all data rates. Response time for reconfiguration is also shown for Design 1 and Design 2. For Design 2 simulations show that the response time of the dc bias conditions when the front-end is reconfigured from lowest to highest data rate is ~ 500 ps, whereas in Design 1 it is ~ 297 ps.

5.2 Future Work

Due to the remarkable growth in internet data traffic communication and technology advancement, high-speed link design is mandatory. Therefore, implementation of a short-reach high speed optical front–end with tunability mechanism is necessary for future communication. This work is based on a conventional front–end receiver topology such as shunt feedback TIA, common source based post-amplifiers etc. In future, further investigation can be done in the following areas:

a) Optimize the core circuitry in terms of lower data rates (e.g. lower input referred noise)
b) The overload condition of the front-end at different data rate needs to be re-investigated.
c) Offset compensation block can be re-investigated where the main goal will be reducing the response time for reconfiguration more compared to this design.

d) Layout is one of the critical parts of designing high-speed links. This design is severely effected by the parasitics. One should be careful about using different types of contacts in the layer, dummy shapes and long wiring. Each element in the layout adds some amount of parasitcs in the circuits. Therefore, layout of the high speed design needs more attention.

e) Some additional work such as an automatic gain controller circuit can be incorporated to fix the overall gain at different data rates rather than the resistive bank. A digitally controlled offset compensation scheme can also be employed instead of the passive one which can reduce the chip area further as the capacitors in this offset compensation scheme take more chip area.

f) A system level modification can also be an another interesting direction for future work where data rate detection and transmitter power scalability will be investigated.

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