

**REDUCTION OF LOW-ORDER HARMONICS AND NEW  
TOPOLOGIES OF CURRENT SOURCE CONVERTERS**

**Maged Fouad Fahmy Naguib Barsom**

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# ABSTRACT

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## REDUCTION OF LOW-ORDER HARMONICS AND NEW TOPOLOGIES OF CURRENT SOURCE CONVERTERS

**Maged Fouad Fahmy Naguib Barsom**

Two CSCs related issues are investigated. The first is the reductions of Low Order Harmonics (LOH) in Low Switching Frequency (LSF) CSCs. High power CSCs operate with LSF. This is not an ideal scenario for Space Vector Modulation (SVM), resulting in non-characteristics LOH, 5<sup>th</sup> and 7<sup>th</sup> (HD<sub>5-7</sub>). Researchers have attempted to reduce these harmonics by creating new sequences of space vectors (states) or different sampling techniques. New approaches based on the fact that HD<sub>5-7</sub> is affected by states ON times calculation process are proposed. Results show that by using a new technique called Record Middle (RM), one can obtain a smaller HD<sub>5-7</sub>. Also, results for calculating states ON times as the reference vector rotates by new SVM equations show that one can get a significant reduction in HD<sub>5-7</sub>. Another alternative effective with large overlap periods is minimizing LOHs in LSF-SVM-CSCs with Minimum Harmonic Tracking (MHT) technique. Fuzzy logic dependent states ON times calculation give fixed states ON times adjustment during steady state and fast response. Those techniques allowed the usage of reduced size ac-side filters with high cut-off frequencies.

The second issue is on new hybrid current source converters (HCSCs). Three SCRs and four IGBTs HCSC has similar characteristics, less capital cost and less power losses compared to the 6-switches CSC. Two types of modulation are proposed. The first is Hard Switching Space Vector Modulation technique (HS-SVM). HS-SVM is

presenting low maximum modulation index ( $m_{a,max}$ ), resulting in LOH distortion and requiring multiple mandatory switching inside a cycle. The second modulation technique achieves line-commutation or soft switching (SS) of the SCRs whenever possible, thus being called Soft Switching Space Vector Modulation technique (SS-SVM). SS-SVM increases the  $m_{a,max}$  while reducing LOH, the switching frequency and switching losses. Comparisons between the 6-switches CSC and the HCSCs are provided. Cost analysis showing the importance of HCSCs is carried out. A case study is presented to show that the HCSC is economically viable in medium and high power ranges. Besides having lower capital cost, the HCSC can operate with lower power losses than 6-switches CSC.

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## LIST OF ACRONYMS

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A (Unit)	Ampere
ac	Alternating Current
ASCI	Auto Sequential Commutated current source Inverter
CF	Correction Factor
CSC	Current Source Converter
CCM	Continuous Conduction Mode
CMOS	Complementary Metal Oxide Semiconductor
CSR	Current Source Rectifier
CSI	Current Source Inverter
db	Decibel
dc	Direct Current
dq	Direct and Quadratic component
DSP	Digital Signal Processor
dSPACE	Digital Signal Processor with real-time hardware, I/O interfaces connected via RTI blocks integrated into MATLAB/Simulink
DS-1103	A type of Digital signal processor with rapid control prototyping
EQ	EQuation
F	Farad (capacitor measuring unit)
f	Frequency
OPAL-RT	A company for Open Scalable Real-Time simulation and control devices
OP-5000	An electronic card use fast processor for rapid control prototyping
GTO	Gate Turns Off

H	Henry (Inductor measurement unit)
HCSC	Hybrid Current Source Converter
HS-SVM	Hard Switching Space Vector Modulation
Hz	Hertz
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
LEM	Type of voltage and current measurement device (transducer)
LOH	Low Order Harmonics
LSF	Low Switching Frequency
MOSFET	Metal Oxide Silicon Field Effect Transistor
MHT	Minimum Harmonics Tracking
pu	Per unit
PCC	Point of Common Coupling
PWM	Pulse Width Modulation
P	Active power
PLL	Phase Locked Loop
PF	Power Factor
Q	Reactive power
RM	Record Middle
RT	Record Transition
RTI	Real Time Interface

SAs	Start SAMpling
SAm	Middle SAMpling
SCR	Silicon Controlled Rectifier
SHE	Selective Harmonics Elimination
SMES	Super Magnetic Energy Storage
SPWM	Sinusoidal Pulse Width Modulation
SQ1	SeQuence one
SQ2	SeQuence two
SQ3	SeQuence three
SS	Soft Switching
SS-SVM	Soft Switching Space Vector Modulation
STATCOM	STATic synchronous COMPensator
SV	Space Vector
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
UPF	Unity Power Factor
V	Voltage
VAR	Variable Reactive Power
VSC	Voltage Source Converter
VSR	Voltage Source Rectifier
VSI	Voltage Source Inverter
t	time (s)
W	Watt (Active power measurement unit)
$\Omega$	Ohm (Resistor measurement unit)

## LIST OF PRINCIPAL SYMBOLS

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$abc/\alpha\beta$	Conversion from three axis stationary frame to two axis stationary frame.
$abc/dq$	Conversion from three axis stationary frame to two axis rotating frame.
A	The distances between $t_i$ calculating and active states transition instants
B	$I_i$ ON time
C	The distance between $t_{i+1}$ calculating and active states transition instants
$C_{ac}$	Ac side Capacitance
C	SVM Cycle number
D	$I_{i+1}$ ON time
$f_{ac}$	Alternating current ac-side cycle frequency
$f_{cycle}$	SVM cycle frequency
$HD_{5-7}$	Index for 5 <sup>th</sup> and 7 <sup>th</sup> non-characteristics harmonics components
$HD_5$	Index for 5 <sup>th</sup> non-characteristics harmonics components
$HD_7$	Index for 7 <sup>th</sup> non-characteristics harmonics components
$I_a$	pulsated current appears in the HCSC terminals for phase A
$I_{as}$	Grid current for phase A at the point of common coupling
$I_{(abc)cap}$	Three phases ac-side capacitor current
$I_{(abc)s}$	Three phases ac-side source currents at PCC
$I_{(abc)}$	Three phases currents in converter ac-side, not include the ac-side filter
$I_{dc}$	Dc-side current
$I_{(dq)}$	Current in HCSC ac-side terminal with two rotating axis frame.
$I_{(dq)s}$	Ac-side currents in PCC with two rotating axis frame.

$\overline{I_{da}}, \overline{I_{qa}}$	dq frame values for the required currents from HCSC in capacitor terminals after changing to adequate SS-SVM concept.
$\overline{I_{db}}, \overline{I_{qb}}$	dq frame values for the required currents from HCSC in capacitor terminals before changing to adequate SS-SVM concept.
$I_{(\alpha\beta)cap}$	Ac-side filter capacitor current in HCSC with two stationary axis frame
$I_{(\alpha\beta)s\_ref}$	The required current from HCSC in the capacitor terminals with two stationary axis frame
$I_{(\alpha\beta)s}$	Ac-side currents in PCC with two stationary axis frame.
$i_a, i_b$ and $i_c$	Instantaneous ac-side currents for phases A, B and C
$I_n$	Reference current vector in SVM
$I_1$ - $I_{10}$	States space vectors in SVM-CSC
$I_i$ and $I_{i+1}$	Active state vectors
$I_z$	Zero state vector
$I_{(1^{st})}$	Fundamental component for the current
$I_{(5^{th})}$	Fifth order harmonics component for the current
$I_{(7^{th})}$	Seventh order harmonics component for the current
$k$	Safety factor required to grantee safe commutation in HCSC
$K_c$	Correction factor required to reduce $HD_{5,7}$ in CF technique
$L_{ac}$	Ac side inductance
$m_a$	Modulation index
$m_{a,max}$	Maximum modulation index
$n$	Number of SVM cycle $n = 1, 2 \dots 3 N_{CS}$ .
$N_C$	SVM cycle Number

$N_{CS}$	Number of cycles per sector
$P_{ref}$	Reference active power
$R_{ac}$	Ac side filter resistance
$Q_{ref}$	Reference reactive power
$Q_a$	Available reactive power in SS-SVM.
$t_{ac}$	Alternating Current ac-side cycle time
$t_{cycle}$	SVM cycle time
$t_i$ and $t_{i+1}$	Active states ON times
$t_{sector}$	SVM sectors time
$t_i(N_C)$	State $I_i$ ON times in SVM cycle $N_C$
$t_{i+1}(N_C)$	State $I_{i+1}$ ON time in SVM cycle $N_C$
$t_z$	Zero state ON time
$t_{z1}$	First half zero state ON time in SQ3
$t_{z2}$	Second half zero state ON time in SQ3
$t_{x(y)}$	State ' $I_y$ ' ON times in SVM cycle ' $x$ '
$t_{x(y)m}$	State ' $I_y$ ' ON time in SVM cycle ' $x$ ' calculated using continuous $t_y$ in the middle of state ' $I_y$ '
$t_{x(y)s}$	State ' $I_y$ ' ON time in SVM cycle ' $x$ ' calculated using continuous $t_y$ in the starting of state ' $I_y$ '
$t_{x(y)f}$	Final state ' $I_y$ ' ON time in SVM cycle ' $x$ ' when CF is used
$t_{z.min}$	Minimum zero state time interval to guarantee the safe commutation of the SCRs in HCSC
$t_q$	Data sheets turn off time for SCRs

$t_{\text{off.min}}$	Minimum turn-off time of an SCR that is actively commutated by diverting its current and without being reverse biased.
$t_{\text{off}}$	Turn-off time of an SCR
$T$	Total pulses cycle in the HCSC feasibility experimental test
$t_{\text{on}}$	SCR gate excitation period in the HCSC feasibility experimental test
$t_x$	Required time to recover SCR in the HCSC feasibility experimental test, during this period SCR and IGBT have no gate signals.
$X_{\text{old}}$	Input of Fuzzy logic effecting LOH
$X_{\text{new}}$	Output of Fuzzy logic required to reduce LOH
$V_a$ or $V_A$	Ac-side capacitor voltage for phase A
$V_{(\text{abc})\text{s}}$	Three phases ac-side source voltages
$V_{(\text{abc})}$	Three phases ac-side capacitor voltage
$V_{\text{dc}}$	direct current in the experimental test circuit
$V_{(\alpha\beta)\text{s}}$	Ac-side source voltages in two stationary axis frame
$V_{(\alpha\beta)}$	Ac-side capacitor voltages in two stationary axis frame
$\varphi_I$	Space vector angle for the SVM reference current
$\varphi_V$	Space vector angle for the ac-side capacitor voltage
$\theta$	The angle of the reference current vector in a given SVM sector
$\omega$	Angular frequency (Space vector rotation speed)
$\theta_{\text{off}}$	Offset angle required to satisfy middle sampling (SAm)
$\theta_{x(y)\text{m}}$	The SVM sector angle at SVM cycle 'x' in the middle of state 'I <sub>y</sub> '
$\theta_{x(y)\text{s}}$	The SVM sector angle at SVM cycle 'x' in the beginning of state 'I <sub>y</sub> '

$\alpha_{\max}$	The biggest firing angle of the SCRs without commutation failure in phase control applications
$\angle \vec{V}$	The capacitor voltage rotating frame angle
$\angle \vec{I}$	The required HCSC rotating current SVM angle
$\delta_{a(n)}$	An array of angles with n length, one of those is required between current and voltages vectors in SS-SVM
$\delta_b$	The angle between $V_a$ and $I_a$ before adjusted to satisfy SS-SVM concept.
$\delta_a$	The angle between $V_a$ and $I_a$ after adjusted to satisfy SS-SVM concept.
$\alpha$	The angle between grid capacitor voltage and grid voltage vectors.



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- [5] M.F. Naguib and L.A.C. Lopes, “The effect of states ON time calculations and states sequence in low order harmonics of space vector modulated current source converter”, in proc. IEEE, EPEC’09, 22 - 23 October 2009.
- [6] M.F. Naguib and L.A.C. Lopes “Soft switching of a hybrid current source converter “, in proc. IEEE, PESC’08, 15 - 19 June 2008, pp. 4177 – 4183.
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- [8] M.F. Naguib and L.A.C. Lopes, “A Hybrid bi-directional current source converter with two force commutated switches and controlled with space vector modulation”; in proc. IEEE, CCECE’08, 4 - 7 May 2008, pp. 173 - 178.
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**PART- 1.**

**REDUCING LOW ORDER HARMONICS IN**

**CURRENT SOURCE CONVERTERS**

---

**CHAPTER 1**

**1. SPACE VECTOR MODULATION FOR CURRENT SOURCE**

**CONVERTER**

---

**1.1. INTRODUCTION**

Controllable Power Electronics switching devices are roughly divided into two types, SCRs and force-commutated switches. SCRs are usually employed in high power applications, above the power ratings of force-commutated switches. An SCR turns on when forward biased with short gating pulses and turns off when its current becomes zero. It cannot be turned off via a gate signal, which limits its operation in PWM techniques. Low and medium power applications can be achieved using MOSFETs and IGBTs, respectively, where around 5 kHz switching frequency is used. For high power levels applications GTOs or IGCTs are used with switching frequency around 2 k Hz, giving long switching times and high power losses [1].

Ac - dc power converter topologies are usually classified into two categories. The first category is Voltage Source Converters (VSC), which is more common and widely used [1] - [5]. Traditional three phase VSC is shown in Fig. 1- 1 when connected as rectifier. In VSC the load is usually connected in parallel with a dc-side capacitor. VSC is used as a rectifier and (or) an inverter in motor drives, reactive power compensation and energy storage systems. VSC with PWM was for long time the traditional way to transfer power between ac-side and dc-side using six forced commutation switches and low harmonic distortion [1] - [5]. VSC based on IGBTs, GTOs or MOSFETs has shown intrinsic weakness for high power applications due to substantial switching losses and high dv/dt of the PWM operation, leading to hazardous over voltages [2]. Many researchers have focused on VSC design, applications, modulation techniques, harmonic spectrum and control [2] - [5].

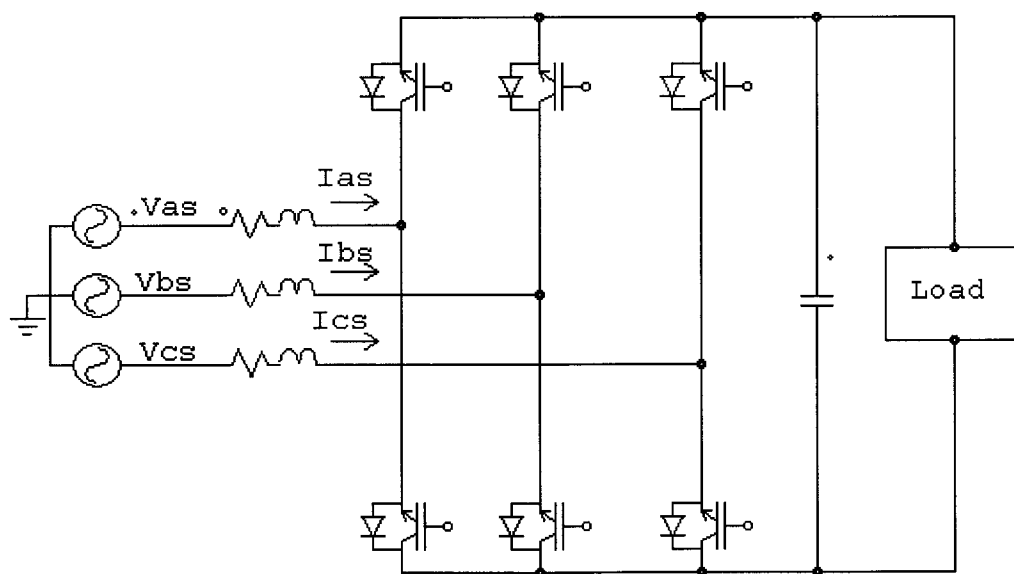


Fig. 1- 1 :- 6-switches IGBT based Voltage Source Converter (VSC).

The second category is current source converters (CSC) [6]. CSC topologies are found in many applications. Such as, superconducting magnet energy storage systems (SMES) [7], reactive power compensation STATCOM [8] - [10], high voltage dc transmissions HVDC [11]. And, in a number of industrial processes like high-power adjustable-speed drives, where four-quadrant operation, near sinusoidal motor terminal voltages, supply voltage variations immunity and inherent short-circuit protection are required [6], [12] - [15].

Traditional GTOs based CSC is shown in Fig. 1- 2 when connected as rectifier. Less research deals with CSC in general [1]. The power circuit of the CSC is simpler and more robust than the VSC due to no freewheeling diodes with unidirectional current flow [6]. In principle, CSC presents a higher reliability than VSC due to the inherent over current protection and the fact that large dc-side capacitors present shorter life spans than large inductors [2]. Non-characteristic harmonics in LSF-CSC are higher than in LSF-VSC [16], [17]. And, both CSC and VSC can be used in both rectifier and inverter modes of operation [1], [3], [5], [6].

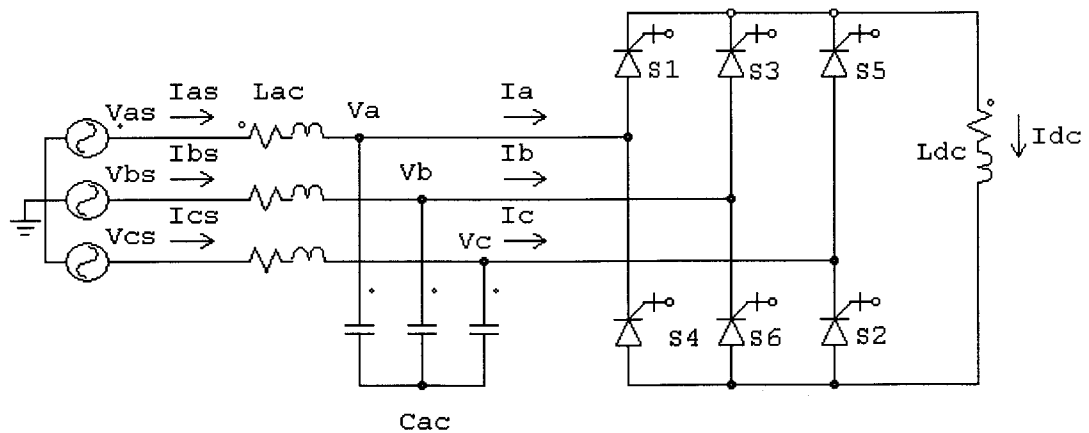


Fig. 1- 2 :- 6-switches GTOs-based current source converter (CSC).

## **1.2. CSC MODULATION TECHNIQUES**

### **1.2.1. COMMON MODULATION TECHNIQUES FOR CSCs**

A number of PWM techniques have been used for generating the gating signals of CSCs [6]. The popular Sinusoidal Pulse width modulation (SPWM) technique results in frequent switching and power losses when applied to CSC, not suitable for high power applications [18], [19].

In high power applications, selective harmonic elimination (SHE) has been used as an off-line technique to eliminate certain harmonics in the ac-side current [20] - [23]. SHE concept can be extended to multilevel CSC [24], [25]. Certain procedures should be used for the ac-side filter design in this case [26]. SHE has been used for CSC with around 500 Hz switching frequency, where a limited number for the SHE chopping angles are calculated off-line [21]. For 1 kHz - 3 kHz, SHE chopping angles are increased which complicating the calculation of those angles.

Space Vector Modulation (SVM) offers an elegant way of generating the gating signals of CSCs on line with reduced switching frequency and increased gain [27] - [33]. Besides, specific gating requirements of CSCs can be readily incorporated in the pattern generation schemes, thus SVM is more suitable for CSC [6]. A comparative study between SPWM and SVM modulation techniques for CSC was presented in [27].

### **1.2.2. FUNDAMENTALS OF SVM- CSCs**

Fig. 1- 2 shows 6-switches (S1- S6) GTO-based CSC. For ideal CSC two GTOs should be ON at any instant, one and only one GTO from upper switches group S1, S3 and S5, and one and only one GTO from lower switches group S2, S4 and S6. That

permits a predefined current path for the dc-side current. In real CSC a commutation (overlap) period is essential to ensure that there is no danger of having no path for the dc link current, to avoid overvoltage [6]. In CSCs both of  $L_{ac}$  and  $C_{ac}$  define the cut-off frequency of the 2<sup>nd</sup> order ac-side filter, which is usually designed for attenuating the characteristic switching current harmonics that appear in the ac-side current. A brief description in CSC ac-side filter effect on harmonic spectrum was presented in [33].

The reference current vector of a three-phase CSC is given by (1- 1).

$$I_n = \frac{2}{3}(i_a + i_b e^{2\pi/3} + i_c e^{-2\pi/3}) = I_\alpha + jI_\beta = |I_n| \angle \varphi_I \quad (1- 1)$$

Where  $i_a, i_b, i_c$  are the instantaneous CSC ac-side currents.

A number of SVM techniques have been proposed to minimize the magnitude of the harmonic distortion caused by 5<sup>th</sup> and 7<sup>th</sup> non-characteristics harmonics components (HD<sub>5-7</sub>) in CSCs operating with LSF [6], [27] - [33]. Those SVM techniques include three main procedures. First, they use the nearest active states in a given sector to synthesize the reference space vector (SV). Second, they select the SVM cycle frequency ( $f_{cycle}$ ) to be a multiple of six of the grid frequency ( $f_{ac}$ ) for synchronized SVM, meaning that each SVM sector is started with one of the SVM cycles. Finally, they choose a certain sequence of states in SVM cycles.

Fig. 1- 3 shows the six sectors complex plane for 6-switches CSC with the reference current vector ( $I_n$ ), six active states ( $I_1$ - $I_6$ ) and three zero states across three CSC legs ( $I_7$ - $I_9$ ). Also it presents CSC switches that are ON in each state. Table 1- 1 presents the switches that are ON in each of the nine states and the direction of the ac currents in each phase.

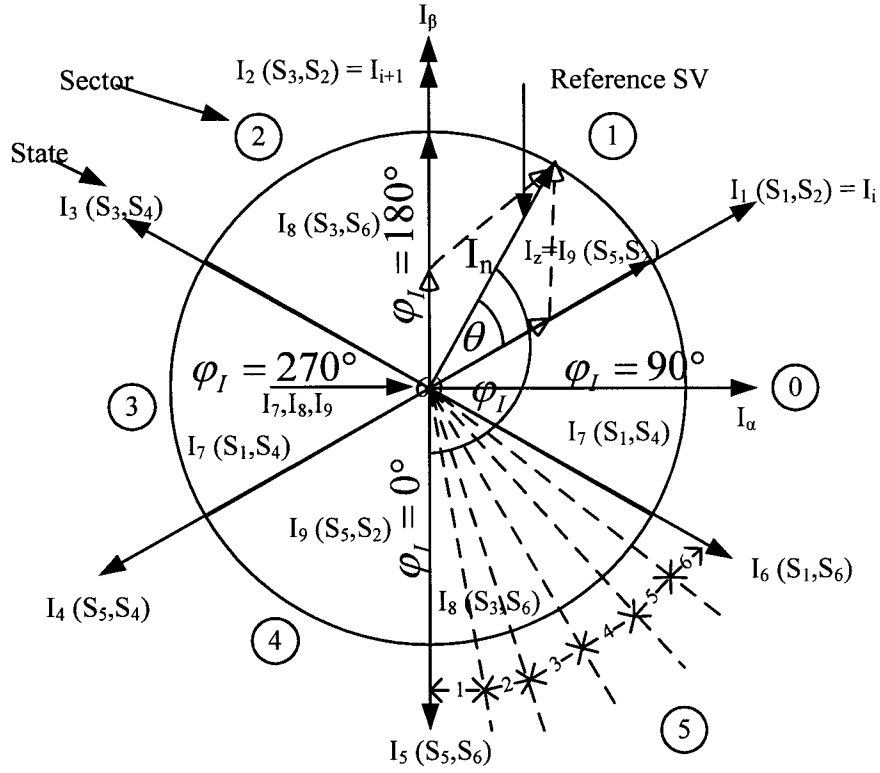


Fig. 1- 3 :- Definition of the sectors (0 - 5), states ( $I_1$ -  $I_9$ ), and the switches which are ON in each state when  $N_{CS} = 6$  in 6-switches SVM-CSC.

The CSC modulated by SVM operates with two active states vectors ( $I_i$  and  $I_{i+1}$ ) and one zero state vector ( $I_z$ ). The angle of the reference vector  $\varphi_I$  defines the sector of operation in the complex plane. The reference current vector is synthesized by using a sequence of two active and one zero states with

$$I_n t_{\text{cycle}} = I_i t_i + I_{i+1} t_{i+1} + I_z t_z \quad (1-2)$$

Where,  $t_{\text{cycle}}$  is the SVM cycle period of a given sequence of states.  $t_{\text{cycle}}$  is the inverse of  $f_{\text{cycle}}$  which depends on the frequency of the fundamental current component at the ac-side ( $f_{\text{ac}}$ ) and on the number of SVM cycles per sector ( $N_{CS}$ ) as given by (1- 3).

$$f_{\text{cycle}} = 6 N_{CS} f_{\text{ac}} \quad (1-3)$$



In synchronized SVM each SVM sector should starts with a new SVM cycle and  $N_{CS}$  should be an integer [6]. In Fig. 1- 3,  $N_{CS} = 6$  was selected, each SVM sector is divided into six SVM cycle. That is applied to SVM sector five in Fig. 1- 3, which give  $f_{cycle}=2160$  Hz, using (1- 3). In this case, the dominant harmonics appears at  $(6 \times N_{CS} \pm 1)$  pu and GTOs switching frequency is  $0.5 \times f_{cycle}=1080$  Hz which is suitable for GTOs and the main advantage of using SVM over SPWM technique.

TABLE 1- 1 :- STATES REALIZATIONS AND SWITCHES SWITCHING FUNCTIONS IN CSC

<i>State</i>	<i>Lower Switch</i>	<i>Upper Switch</i>	$(I_a/i_{dc})$	$(I_b/i_{dc})$	$(I_c/i_{dc})$
1	S2	S1	1	0	-1
2	S2	S3	0	1	-1
3	S4	S3	-1	1	0
4	S4	S5	-1	0	1
5	S6	S5	0	-1	1
6	S6	S1	1	-1	0
7	S4	S1	0	0	0
8	S6	S3	0	0	0
9	S2	S5	0	0	0

### 1.2.3. IMPLEMENTATION OF SVM FOR 6-SWITCHES CSC

SVM had many implementation approaches. SVM for CSC concepts was presented in [6], [27] - [33]. SVM was achieved using different software [34], [35]. There

the procedures to divide the ac-side cycle into SVM sectors, divide SVM sectors to SVM cycles and calculates states ON times implementing SVM cycle were not described. In this thesis SVM for CSC is implemented using MATLAB-SIMULINK and PSIM. SIMULINK is used more often in this thesis while PSIM is used to introduce certain ideas. During research, the results from PSIM and SIMULINK were compared to check results. Thus, SIMULINK blocks used in this thesis to implement the gating signals for SVM-CSC are presented step by step.

The feedback command in closed loop or the desired operating condition in open loop applications of CSCs defines two variables. The first is the modulation index value ( $m_a$ ) and the second is the modulation index angle ( $\phi_I$ ). They are used to implement CSC switches gating pattern. Possible forms for the input variables ( $m_a$  and  $\phi_I$ ) are in (1- 1). If the grid cycle frequency is 60 Hz ( $f_{ac} = 60$  Hz), the ac-side cycle time period is  $t_{ac} = 1/60 = 16.67$ ms, the current SV covers  $360^\circ$  electrical in 16.67ms. There is 6-switches in the CSC topology and 6 active switching schemes in SVM-CSC, so the ac-side current line cycle is divided into six SVM sectors. Each SV sector time is  $t_{sector} = 16.67/6 = 2.78$ ms. That leads each SVM sector to cover  $60^\circ$  electrical. Fig. 1- 3 illustrates one ac-side current line cycle ( $360^\circ$ ) which is divided into six SVM sectors ( $60^\circ$ ). Surrounding the period where phase A current is maximum positive ( $90^\circ$  in ac sinusoidal waveform signal) the upper switch for phase A (S1) of CSC is used. In the first SVM sector (sector 0) S1 is common in  $60^\circ \leq \phi_I \leq 120^\circ$ . Surrounding the period where the phase A current is maximum negative ( $270^\circ$  in ac sinusoidal waveform signal) the lower switch for phase A (S4) of CSC is used. In the fourth SVM sector (sector 3) S4 is common in  $240^\circ \leq \phi_I \leq 300^\circ$ . The same can be said for phases B and C.

Table 1- 2 and Fig. 1- 3 illustrate the divisions of the SVM sectors. Each SVM sector is divided into  $N_{CS} = 6$  cycle. Fig. 1- 4 illustrates how the ac-side line cycle is divided into six SVM sectors, and how a pulse in the beginning of each SVM cycle using SIMULINK Blocks is generated. There the input  $\phi_1$  {[Angle]} is the angle of the required fundamental currents in the converter ac-side. The first output {[A]} represents the number of SVM sector at certain instant varying from zero to six. And, the second output {[B]} is generating a pulse in the beginning of each SVM cycle.

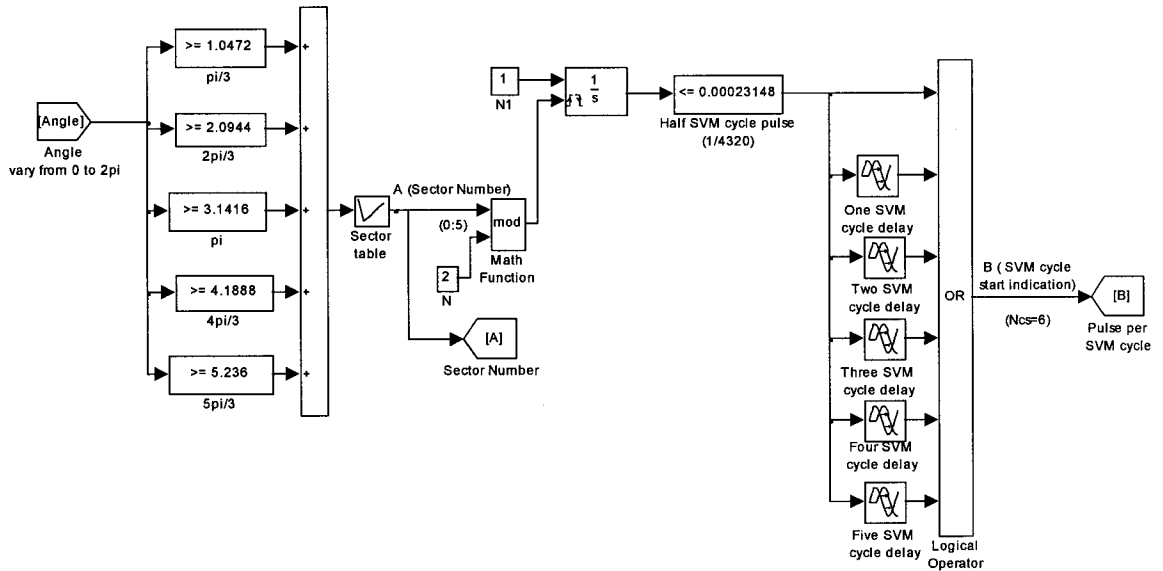


Fig. 1- 4 :-SIMULINK blocks generating SVM sector number and a pulse per SVM cycle

The continuous states ON times for three states ( $t_i$ ,  $t_{i+1}$  and  $t_z$ ) are calculated according to equations (1- 4), (1- 5) and (1- 6), respectively as a function  $m_a = \frac{\|I_n\|}{I_n}$ , such that ( $0 \leq m_a \leq 1$ ), and  $\theta$  is the angle of  $I_n$  in a given sector ( $0^\circ \leq \theta \leq 60^\circ$ ). Fig. 1- 5 illustrates the three continuous states ON times for one SVM sector when  $m_a = 0.5$ . There the SVM sector divided into six SVM cycles when  $N_{CS} = 6$ .

$$t_i = t_{\text{cycle}} m_a \sin\left(\frac{\pi}{3} - \theta\right) \quad (1- 4)$$

$$t_{i+1} = t_{\text{cycle}} m_a \sin(\theta) \quad (1-5)$$

$$t_z = t_{\text{cycle}} - t_i - t_{i+1} \quad (1-6)$$

Fig. 1- 6 represents the SIMULINK blocks used to find the continuous states ON times. There  $\phi_1$  {[Angle]} and sector number {[A]} are used to decide  $\theta$  {[Theta]}, which can be used along with  $m_a$  {[ma]} to decide continuous states ON times {[C]} for  $t_i$ ,  $t_{i+1}$  and  $t_z$  using equations (1- 4), (1- 5) and (1- 6), respectively.

Both active states should be placed one after the other to minimize  $HD_{5-7}$  during sector transitions in SVM-CSC, which generates three sequences of states shown in Fig. 1- 7. States sequences for SVM-CSC were investigated in [33]. In Fig. 1- 7, sequences with good harmonics spectrums are shown.

TABLE 1- 2 :- SECTORS DIVISION IN SVM-CSC

Sector	Common Switch	Non-common Switches	Start angle	Middle angle	End angle
0	S1	S6 - S2	60	90	120
1	S2	S1 - S3	120	150	180
2	S3	S2- S4	180	210	240
3	S4	S3 - S5	240	270	300
4	S5	S4 - S6	300	330	360/0
5	S6	S5 - S1	0	30	60

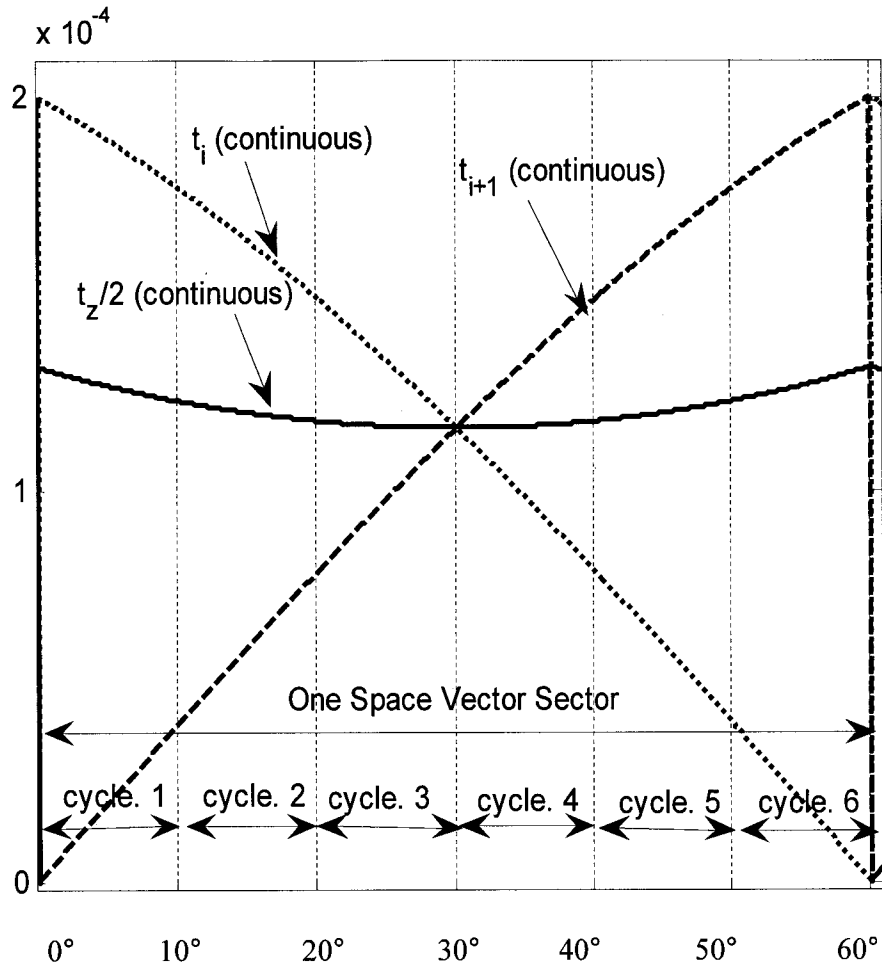


Fig. 1- 5 :-Three continuous states ON times,  $t_i$ ,  $t_{i+1}$  and  $t_z/2$  for one SVM sector when

$$m_a = 0.5 \text{ and } N_{CS} = 6.$$

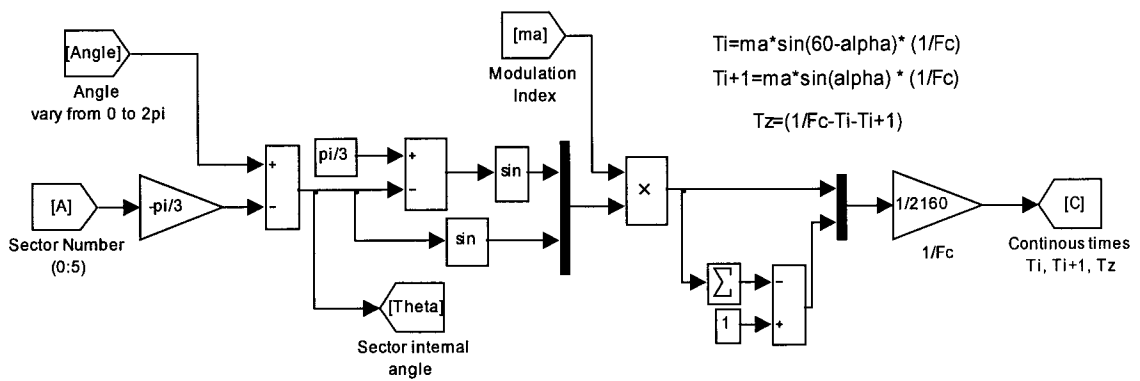


Fig. 1- 6 :-SIMULINK blocks designed to compute continuous states ON times.

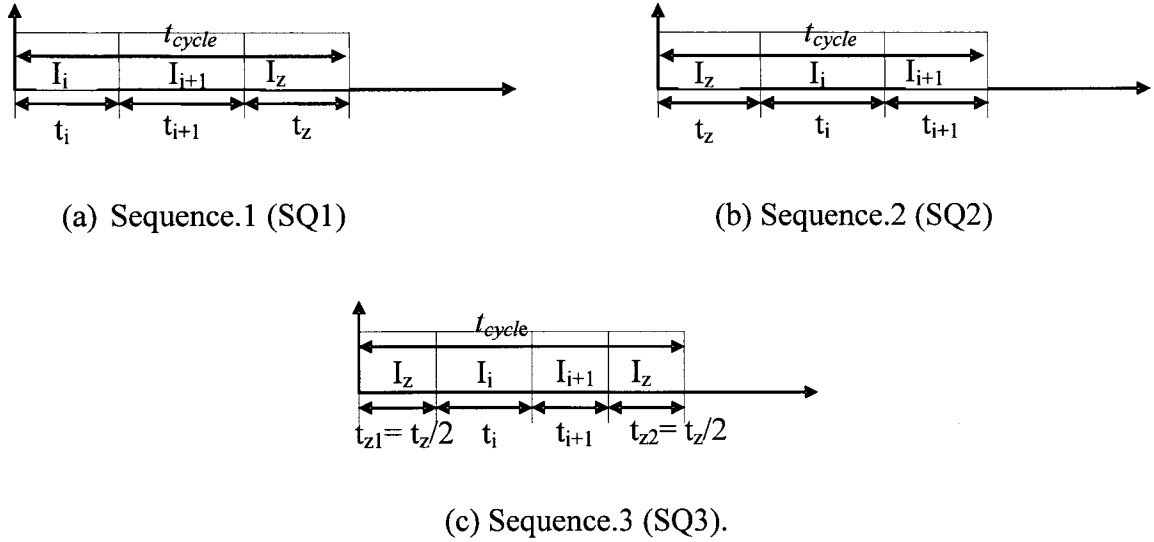


Fig. 1- 7 :-Sequences with the best harmonics spectrum from literature review.

#### 1.2.4. CALCULATIONS OF TRADITIONAL SVM-CSC STATES ON TIME

As an example of SVM-CSC operation from Fig. 1- 3 and Fig. 1- 7, if SQ1 is used for sector one, in the beginning of each SVM cycle  $I_i$  comes first and implemented with  $I_1$  (S1 and S2), the dc-side current flows from phase A to phase C. That is followed  $I_{i+1}$  which is implemented with  $I_2$  (S3 and S2), the dc-side current flows from phase A to phase B. The last state is  $I_z$ , there freewheeling the dc-side current take place, in sector one freewheeling should be across S2, which is common in both active states in sector one using  $I_9$  (S2 and S5), that reduce the switching losses. While if SQ3 is used, each cycle is started by the first half of state  $I_z$  ON time ( $t_{z1} = t_z/2$ ) with  $I_9$ , followed by the first active state  $I_i$  ON time ( $t_i$ ) with  $I_1$ , the second active state  $I_{i+1}$  ON time ( $t_{i+1}$ ) comes next with  $I_2$ , the SVM cycle is ended by the second half of state  $I_z$  ON time ( $t_{z2} = t_z/2$ ) with  $I_9$ . Table 1- 2 is used in selecting switches in SVM-CSC.

SVM with high switching frequency results in low LOH distortion in the CSC ac-side current [35]. However, in high power levels where the switches can only operate at

low switching frequencies (LSF) the magnitude of the non-characteristic 5<sup>th</sup> and 7<sup>th</sup> harmonics ( $HD_{5-7}$ ) presents a serious burden on the design of the low pass input filter of CSCs which typically presents low damping [6]. To reduce LOH in LSF-SVM-CSC an active damping method was proposed to reduce the ac-side line current Total Harmonics Distortion (THD) in [36], [37]. There the reduction of LOH was done with resonance while the source of those harmonics in the SVM-CSC was not introduced. Also, suppression of resonance oscillation resulting from LOH was presented in [37] - [39]. These LOH components propagate through the current control loop and distorting the ac-side current in SVM-CSC. In practice, SVM-CSCs have been implemented with  $f_{\text{cycle}} > 5$  k Hz and a bulky 2<sup>nd</sup> order ac-side filter with 3pu cut off-frequency [40] - [43].

The use of hybrid states sequence scheme where a different sequences are used according to position and value of the reference vector in SVM scheme have been reported with minor reductions in the LOH distortion for VSCs in [44]. The problem of LOH in high power LSF-SVM-CSCs can be mitigated with multi-level topologies by phase shifting the gating signals of CSC levels in an appropriate way [7], [45]. Also, LOH was reduced using Multimodal CSC with modified SVM approach in [11]. To reduce the  $HD_{5-7}$  injected into grid in the PCC large resistors are used in series with ac-side filter capacitors and/or inductors in [37], [46].

The harmonic distortion at the input line current for grid-connected CSC is strictly regulated by guidelines such as the IEEE Standard 519, where smaller than 5% total harmonics distortion (THD) is recommended [47]. Traditional SVM-CSC can barely reach this value with certain types of ac-side filters [33]. Besides, resonance in the CSC ac-side usually amplifies LOH, which was damped in [36] - [39]. The geometric-wall-

model on CSC using duality considerations to VSC to determine the spectra of the pulsed output currents occurring in a CSC was presented in [48].

Another venue for investigation, which was not investigated in previous research, is the way ON times of states are calculated in LSF-SVM-CSC, which is the main focus here. In the conventional SVM techniques, the states ON times are calculated at the same time in the beginning of the SVM cycle and held to be used later in that SVM cycle according to the states sequence [33]. This way is defined as Start Sampling (SAs) in this thesis. This results in an unbalanced use of the states. That is for even  $N_{CS}$ ,

$$t_i(N_c) \neq t_i(N_{cs} - N_c + 1) \quad (1-7)$$

Where  $N_C$  is the cycle number ( $N_C = 1, 2 \dots N_{CS}$ ).

Fig. 1- 8 is presenting the SIMULINK blocks used to convert continuous states ON times  $\{[C]\}$  to a sequence of states  $\{[D]\}$  when SQ1 and SAs are used. There, sampling is done in the beginning of the SVM cycle, that is why it called SQ1-SAs. When states sequence or states ON times calculation technique is changed to be different than SQ1-SAs, then Fig. 1- 8 is changed. The output  $\{[D]\}$  should be one when  $I_i$  is selected, two when  $I_{i+1}$  is selected and three when  $I_z$  is selected. Both of SVM sector number  $\{[A]\}$  and states signal  $\{[D]\}$  are used as an input of a group of look up tables designed to decide the selected switches in 6-switches SVM-CSC according to Table 1- 3.

In the horizontal axis of Fig. 1- 9, SVM sector angles ( $0^\circ \leq \theta \leq 60^\circ$ ) are shown. There are six SVM sectors per ac-side line cycle ( $360^\circ$ ). Since  $\theta = \omega t$ , the horizontal axes in Fig. 1- 9 represents angle ( $\theta$ ) as well as time ( $t$ ), the SVM sector time is divided into six SVM cycles. The vertical axis is the time in seconds used for calculating the states ON times inside SVM cycles. Fig. 1- 9 shows the continuous times for three states  $t_i, t_{i+1}$



and  $t_z$  calculated from (1- 4), (1- 5) and (1- 6), respectively as dotted curves. It also shows  $t_i$ ,  $t_{i+1}$  and  $t_z$  calculated using Start Sampling (SAs) technique as solid curves, those values which changes in the beginning of each SVM cycle are used by SAs to represent states ON times inside SVM cycles independent on SVM sequence of states.

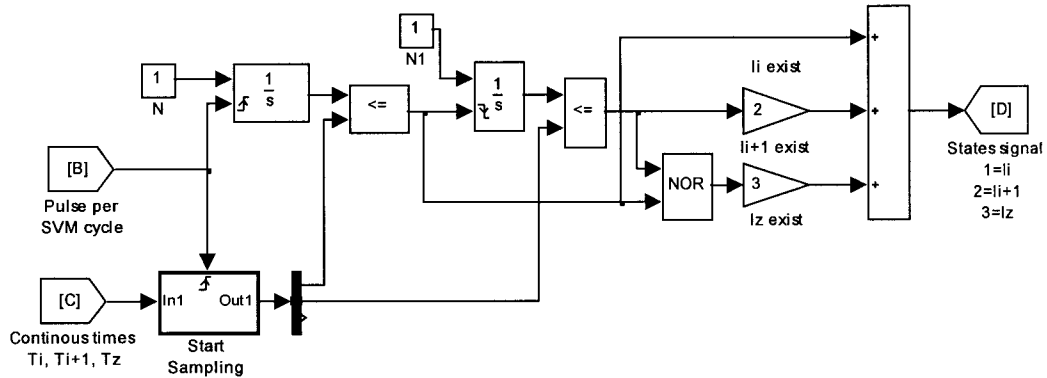


Fig. 1- 8 :- SIMULINK blocks convert generates states signal with SQ1-SAs.

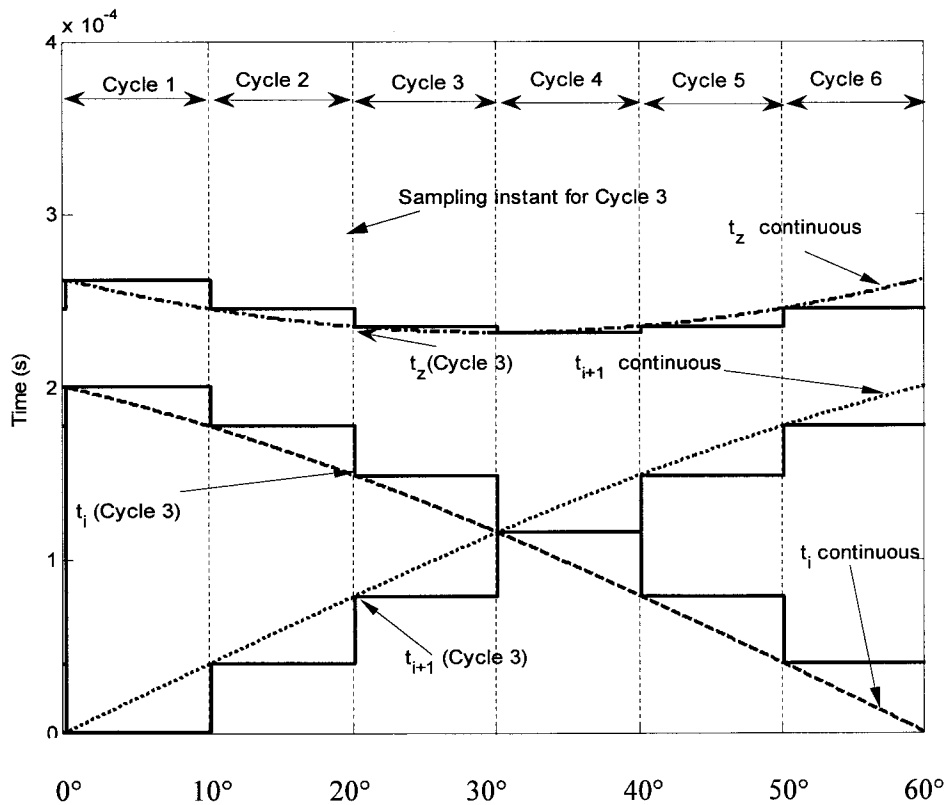


Fig. 1- 9 :-States ON times calculation procedure for  $t_i$ ,  $t_{i+1}$  and  $t_z$  in each SVM cycle in one SVM sector when SAs is used.

TABLE 1- 3 :- ON SWITCHES IN EACH STATE IN SVM-CSC.

Sector Number	State Signal	Upper Switch	Lower Switch
0	$I_i$	S1	S6
	$I_{i+1}$	S1	S2
	$I_z$	S1	S4
1	$I_i$	S1	S2
	$I_{i+1}$	S3	S2
	$I_z$	S5	S2
2	$I_i$	S3	S2
	$I_{i+1}$	S3	S4
	$I_z$	S3	S6
3	$I_i$	S3	S4
	$I_{i+1}$	S5	S4
	$I_z$	S1	S4
4	$I_i$	S5	S4
	$I_{i+1}$	S5	S6
	$I_z$	S5	S2
5	$I_i$	S5	S6
	$I_{i+1}$	S1	S6
	$I_z$	S3	S6

SAs presented in Fig. 1- 9 do not give an ideal SVM in LSF applications. The difference between the dotted curves and SAs solid curves for states is zero in the beginning of SVM cycles and maximum at their ends. With long SVM cycle in LSFs applications, the difference between dotted and solid curves is large. That gives inaccurate calculations for states appearing near the end of SVM cycles. However, with LSF the synthesis of the SVM is concluded several degrees after calculated, leading to an

unbalance in the use of the active states in all sectors, i.e. the first active state  $I_i$  will be used more than the second active state  $I_{i+1}$ . Average times of  $t_i$ 's  $>$   $t_{i+1}$ 's when SAs is used, that is seen in Fig. 1- 10. The state representing  $I_{i+1}$  in the recent sector will represent  $I_i$  in the next sector, which is shown in Fig. 1- 3. Fig. 1- 11 shows the ON times for one (the common) active state in two sectors follows each other when SAs is used, each of the 12 cycles of the 2 sectors ( $120^\circ$ ). There the use of a state is unbalanced for SAs, the ON time is the largest for the cycle 1 and zero for cycle 7, there is no symmetry. Since there are six sectors in the complex plane,  $HD_{5-7}$  should appear in the ac-side current. In SAs technique, independent on  $m_a$  and states sequence, the average error in the SVM sector is positive for  $t_i$  and is negative for  $t_{i+1}$  during an entire SVM sector.

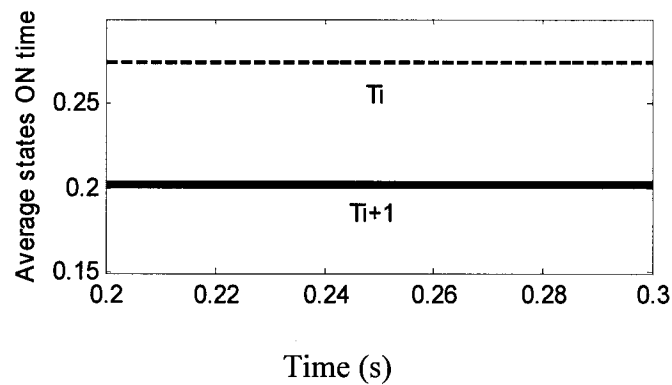


Fig. 1- 10 :- Percentage average active states ON times for SVM sector with SAs  $m_a=0.5$ .

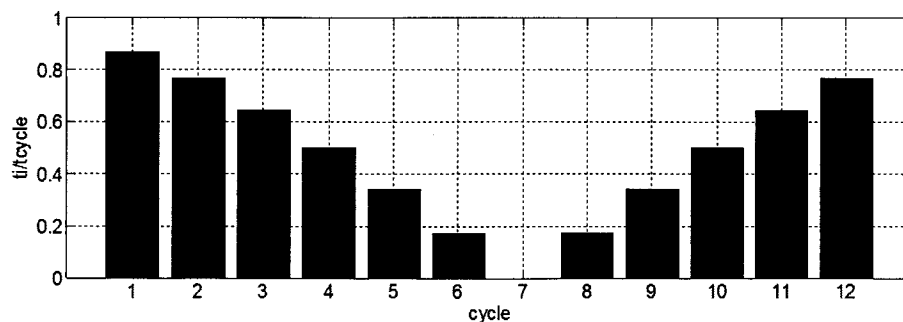


Fig. 1- 11 :- ON times of an active state with SAs when  $N_{CS} = 6$  and  $m_a = 1$ .

The idea behind the SVM technique is to use a sequence of states to synthesize a reference vector ( $I_n$ ), the synthesis is completed at the end of the SVM cycle. Since the reference vector rotates with constant speed, it makes more sense to synthesize the vector when it is located at the midpoint of the region it will travel during the SVM cycle. Recently, the strategy of calculating the states ON times inside SVM cycle to synthesize a reference vector at the midpoint of a given SVM cycle, instead of in the beginning of the SVM cycle, was proposed and presented a moderate reduction in  $HD_{5,7}$ , this process is defined as Middle Sampling (SAM) here. SAM approach was used along with hybrid states sequence scheme yielding to a moderate reduction in  $HD_{5,7}$  [33].

SIMULINK blocks for SAM are implemented by adding an offset angle  $\theta_{off} = 60^\circ/(2 \times N_{CS})$  corresponding to half the duration of SVM cycle time to the angle of the instantaneous reference vector  $\theta$  in (1- 4), (1- 5) and (1- 6). This offset is added by a slight change in SIMULINK blocks designed to decide states ON times presented in Fig. 1- 6 to be as shown in Fig. 1- 12, while other simulation blocks have no change.

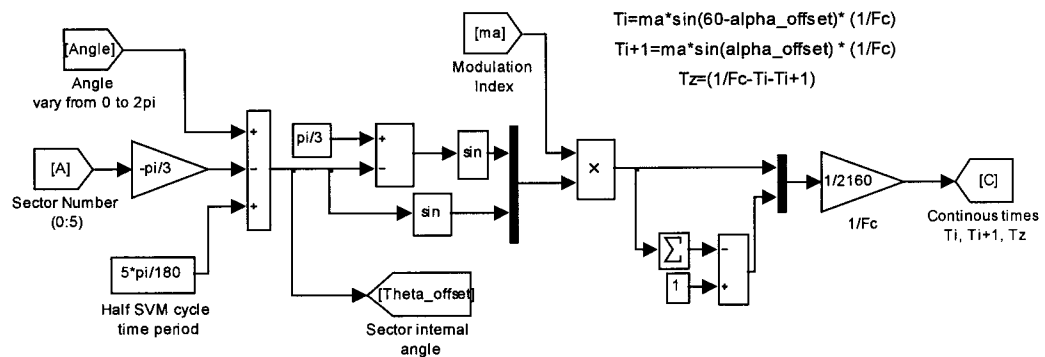


Fig. 1- 12 :- SIMULINK blocks designed to calculate ON times for states if SAM is used.

Fig. 1- 13 shows continuous times of states  $t_i$ ,  $t_{i+1}$  and  $t_z$  as dotted curves. It also shows  $t_i$ ,  $t_{i+1}$  and  $t_z$  calculated with the Middle Sampling (SAM) technique as solid curves.

The difference between dotted and solid curves is small in the beginning of each SVM cycle (positive or negative) and at the end of each SVM cycle (negative or positive) and zero in the middle of SVM cycles. As a result, the average error for  $t_i$  and  $t_{i+1}$  in each SVM sector is almost zero in SAM, and  $t_i$ 's =  $t_{i+1}$ 's in Fig. 1- 14. Fig. 1- 15 shows the ON times for one active state when SAM is used in each of the 12 cycles of the 2 sectors (120°). There the use of the state is balanced when the ON times are calculated with SAM. The sampling instants for cycle 3 in SAM is introduced in Fig. 1- 13 when  $N_{CS} = 6$  and  $m_a = 0.5$ . In CSC, SVM is optimized by SAM to satisfy SVM implementation, which does not generate  $HD_{5-7}$  if the switching frequency is more than 5k Hz. Nonetheless, SAM still produces  $HD_{5-7}$  currents harmonics in LSF as we will see later. SAs and SAM LOH results at different states sequences will be presented in the next chapter.

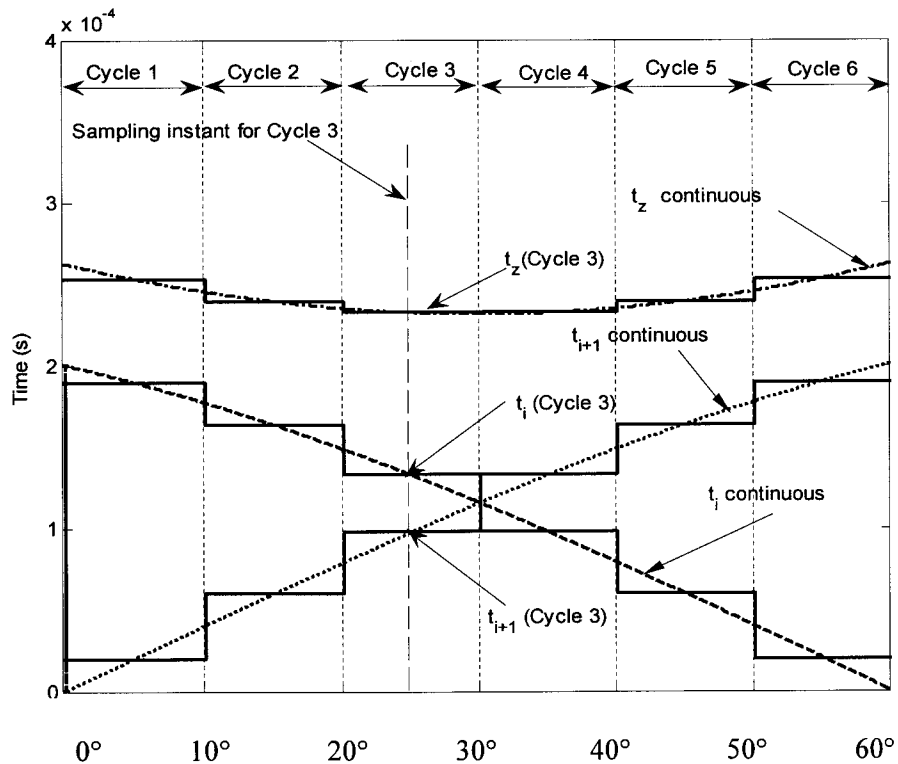


Fig. 1- 13 :- States ON times calculation procedure for  $t_i$ ,  $t_{i+1}$  and  $t_z$  in each SVM cycle in one SVM sector when SAM is used.

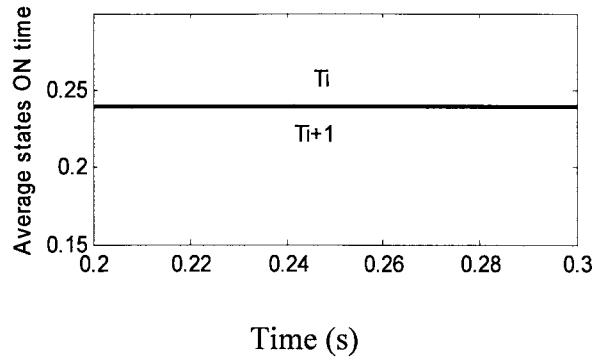


Fig. 1- 14 :- Percentage average active states ON times for SVM sector with SAM  $m_a=0.5$

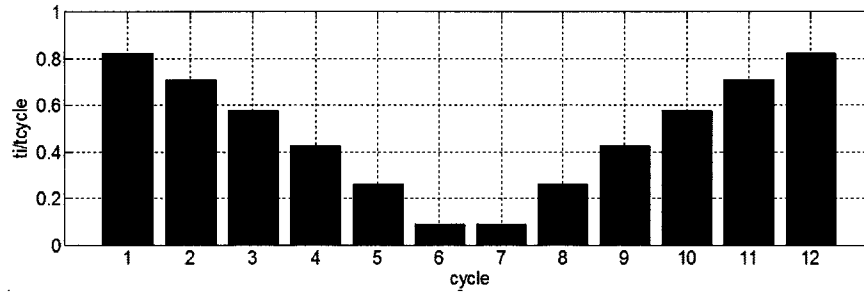


Fig. 1- 15 :- ON time of an active state with SAM when  $N_{CS} = 6$  and  $m_a = 1$ .

### 1.3. THESIS OUTLINE

The contents of this thesis have been organized as follows.

*In chapter two* the magnitude of the 5<sup>th</sup> and 7<sup>th</sup> harmonics ( $HD_{5-7}$ ) is reduced by Record Middle (RM). In RM the states ON times are calculated at different moments, as the states are used in the middle of each state appearing period and with the reference vector placed at different locations during a given cycle. That permits respecting the calculated ON times of only two states, when both active states ON times calculation are respected  $HD_{5-7}$  can be reduced.

*In chapter three*, new SVM equations (EQ) are proposed. The equations procedure varies with the sequence of states to achieve instantaneous calculations, which

results in a reduced  $HD_{5-7}$ . If the calculated ON times are further adjusted to fit in the SVM cycle a new procedure called CF is generated with virtual elimination of  $HD_{5-7}$ .

*In chapter four* minimum harmonics tracking (MHT) technique is presented for a real GTO based CSC with overlap period, input filter and snubber effects. MHT is based on measuring the value of  $HD_{5-7}$  and comes up with a procedure to reduce it using the perturbing and observing principle to reach the least possible  $HD_{5-7}$ .

*In chapter five*, an artificial intelligence technique (Fuzzy logic) is found effective in eliminating  $HD_{5-7}$  with fast response. For the simple Fuzzy logic proposed, no oscillations around best least  $HD_{5-7}$  exist in the steady state as it was the case in tracking techniques. When the operating point is changed, the Fuzzy logic acts fast by varying the value of a parameter (X) to reach the new least  $HD_{5-7}$ .

*In chapter six* a review of existing HCSCs topologies is carried out. Then, two types of HCSCs are proposed. The first is a HCSC with six SCRs and two IGBTs. The second is a HCSC with three SCRs and four IGBTs. An experimental test circuit is implemented to prove the feasibility of the proposed HCSCs topologies.

*In chapter seven*, a Hard Switching SVM (HS-SVM) scheme suitable for the proposed HCSCs is proposed. When HS-SVM is used HCSC is bi-directional with capabilities similar to SVM-CSC. A Three SCRs and four IGBTs HCSC is implemented experimentally and further investigations are done by simulation. A basic closed loop control scheme for the HCSC with HS-SVM that allows it to track  $P_{ref}$  and  $Q_{ref}$  is discussed.

*In chapter eight* an SS-SVM technique for HCSC presents a performance level equivalent to that of conventional 6-switch SVM-CSC in terms of flexibility and

harmonic distortion is proposed. While the HCSC topology reduces the number of force-commutated switches required for the converter, the proposed SS-SVM scheme reduces the number of switch commutations and makes some of them soft-switching.

*In chapter nine* aspects of cost analysis for 6-switches SVM-CSC as well as for the HCSC with HS-SVM and SS-SVM are presented and the economical benefits of the proposed HCSC are demonstrated. That is done to justify replacing the 6-switch topology with HCSC in medium and high power ranges.

## **1.4. CONCLUSION**

In this chapter a review of SVM for CSCs was presented. From previous research, the studies on the fundamentals of SVM for low frequency with higher performance have been centered on the results achieved with different sequences of states. Hybrid schemes where different sequences are used depending on the position and value of the reference vector have been reported with minor reductions in the harmonic distortion. The procedure of implementing the SVM for CSC in SIMULINK is presented. If the vector calculations take place one time in SVM cycle then  $HD_{5-7}$  is generated in LSF-SVM-CSC, even if this vector presentation is in the middle of SVM cycle. In SVM, vector analysis is done at one instant per SVM cycle with a certain SVM vector position, while vector should rotate all the time inside the SVM cycle. This instantaneous movement of SVM vector is manipulated in the following chapters.



## CHAPTER 2

# 2. USING STATES ON-TIMES CALCULATIONS TO REDUCE LOH IN 6-SWITCHES CSC

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### 2.1. INTRODUCTION

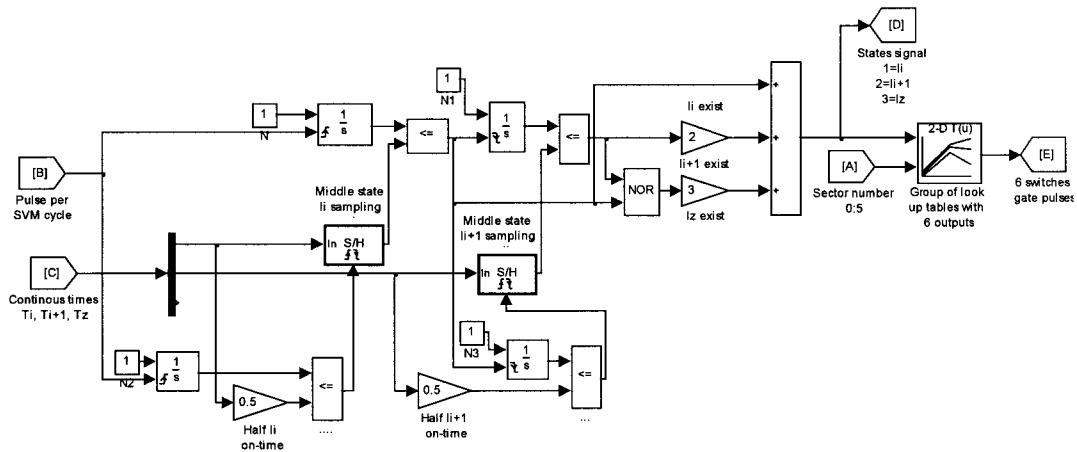
High power CSC is based on GTOs with switching frequency less than 2k Hz. For LSF, as required by GTOs, SVM for CSC results in non-characteristics low order (5<sup>th</sup> and 7<sup>th</sup>) harmonics,  $HD_{5-7}$ . The reduction of  $HD_{5-7}$  has been sought mostly through new sequence of states, which present better performance for different  $m_a$  and PF [33]. Moderate improvement was done by calculating the ON times of states at once in the middle of the SVM cycle [33]. This chapter is proposing a new concept for calculating ON times of states in ideal CSC, which presents minor limitations in practical implementation. The proposed technique of this chapter was presented in [49]. For real CSC, which includes ac-side filter, sunbber circuit, internal switches characteristics and overlap period effects, a more complex procedure should be followed. In this chapter, the effectiveness of the proposed technique for different states sequences is demonstrated by simulations results. The idea presented in this chapter is presented latter on with other procedure in [50], which gives indication of the impotence of the idea presented here.

### 2.2. MIDDLE STATES ON TIMES CALCULATION PROCEDURE

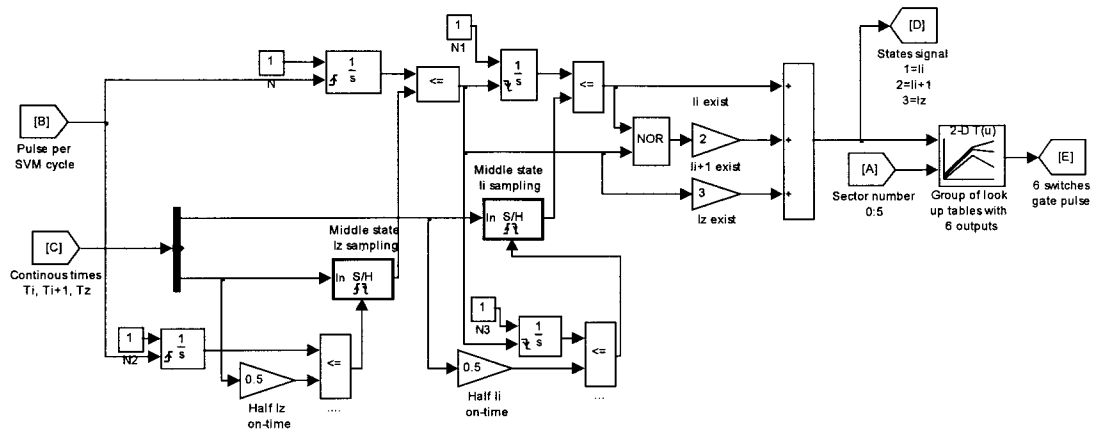
The approach proposed here is to calculate each state ON time when the reference vector is in the middle of this state during rotation, defined as Record Middle (RM).

Unlike sampling techniques, RM technique states ON times calculation instants are not the same for all states representing SVM cycle and varying from one SVM cycle to the other inside the same SVM sector. Also, the states ON times calculations instant vary from one sequence to other, each sequence should be manipulated separately.

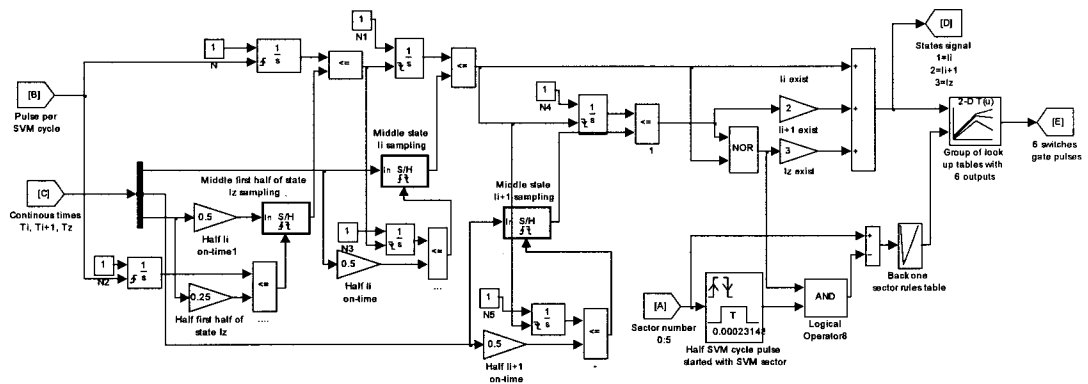
Fig. 2- 1 is presenting RM technique states ON times calculation process using SIMULINK blocks for the three selected sequences. There, the inputs are a pulse in the beginning of each SVM cycle {[B]}, which was in Fig. 1- 4. And, continuous states ON times {[C]}, which was in Fig. 1- 6. Sampling techniques inputs are used as RM inputs, but a different procedure is used to decide states ON time in RM. SIMULINK blocks in Fig. 2- 1 are common. No general sampling procedure exists for signal {[C]}, as it was in sampling. The values of states ON times are selected at different instants, which will be described later on. After states ON times are adjusted, the same procedure used in deciding the ON switches with sampling is used in RM.



(a) SQ1.



(b) SQ2.



(c) SQ3.

Fig. 2- 1 :- RM technique states ON times calculations process.

For states ON times calculation description, one SVM sector was divided into six SVM cycles in Fig. 1- 9 to describe sampling techniques. RM technique requires a deep view inside each SVM cycle. Figures describing RM technique will focus only on one SVM cycle (cycle 3) from the six SVM cycles exist inside the sector, and  $m_a = 0.7$  is selected for description. In all other SVM cycles and  $m_a$  the same can be done. For cycle 3 and  $m_a = 0.7$  states ON times values are near each other, which simplify description.

Fig. 2- 2 illustrates how state  $I_i$  ON time is calculated in SQ1-RM. Since  $\theta = \omega t$ , the horizontal axes as well as the vertical one in Fig. 2- 2 representing time. The

horizontal axis is the cycle 3 time period, which is divided into three states ON times. While the vertical axis is the time used in calculating states ON times when  $m_a = 0.7$ . How to calculate the ON time of  $I_i$  is shown in Fig. 2- 2. There, the continuous ON time for state  $t_i$  in the 3<sup>rd</sup> cycle is shown as a dashed curve. It also shows the continuous ON time  $t_i/2$  as a dotted curve, which is used with an output of unit input resettable integrator shown as dotted curve to calculate the middle of the state  $I_i$ . A pulse starting when  $I_i$  is started and ended in the middle of  $I_i$  is generated and used to calculate  $t_i$ . Sampling is done two times per SVM cycle, one when  $I_i$  is started at  $\theta_{3(i)s}$ . and the second is in the middle of  $I_i$  at  $\theta_{3(i)m}$ , two edges sampling are used. A unit input resettable integrator is used with sampled  $t_i$  presented by heavy lines to calculate state  $I_i$  ON time. The sample in the beginning of the cycle gives estimation for  $t_i$ . The sample in the middle of state  $I_i$  which is  $t_{3(i)}$  in SVM cycle 3 calculates the state  $I_i$  ON time.

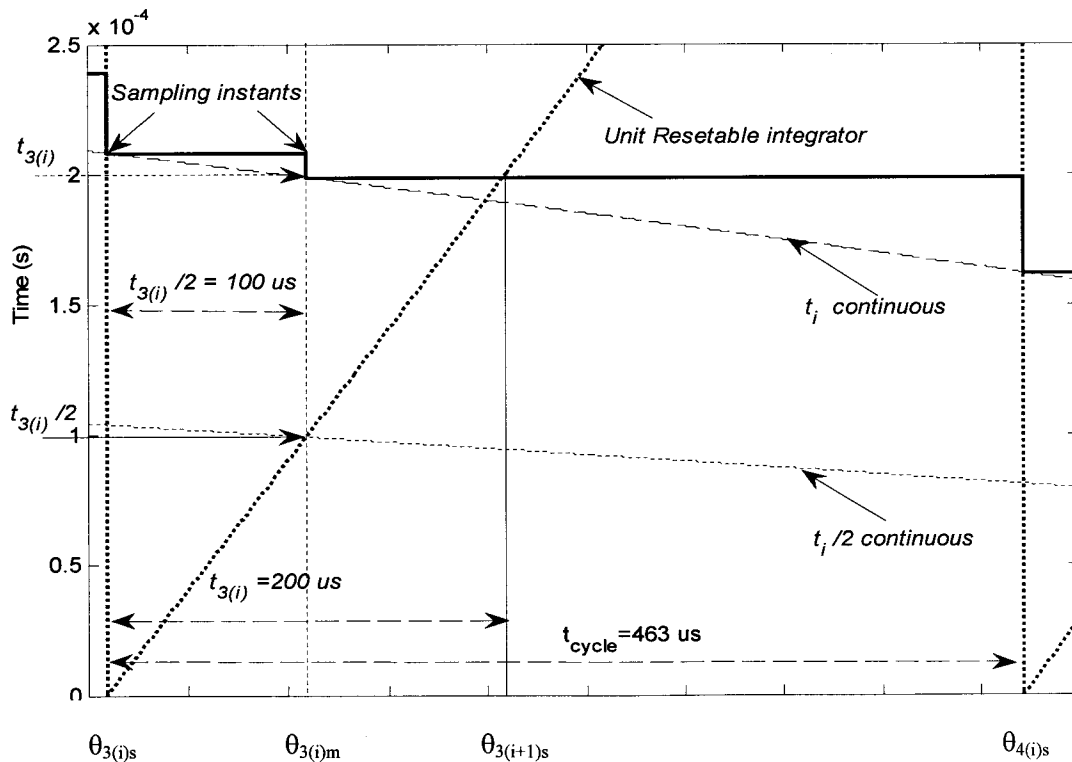


Fig. 2- 2 :- State  $I_i$  ON time calculation when SQ1-RM is used.

Fig. 2- 3 shows how  $t_{i+1}$  and  $t_z$  are calculated for SQ1-RM. The procedure of implementing  $I_{i+1}$  in Fig. 2- 1 (a) is similar to the procedure of calculating  $t_i$ . Thus, continuous half state ON time  $t_{i+1}/2$  dotted curve is used along with an output of resettable integrator, which reset when  $I_i$  is ended, to decide the middle of the state  $I_{i+1}$ . Two edges sampling are used for  $t_{i+1}$ , one when  $I_i$  is ended at  $\theta_{3(i+1)s}$  and the other is in the middle of  $I_{i+1}$  at  $\theta_{3(i+1)m}$ . A Resettable integrator is used with sampled  $t_{i+1}$  presented by heavy lines to calculate state  $I_{i+1}$  ON time. The ON time of zero state  $t_z$  does not need to be calculated, it occupies the remainder of the cycle after  $t_i$  and  $t_{i+1}$  are ended. For SQ1-RM when  $N_{CS} = 6$  and  $m_a = 0.7$  three states ON times for sector three are in Fig. 2- 3. There  $t_{3(i)} = 200\mu s$ ,  $t_{3(i+1)} = 143\mu s$  and  $t_{3(z)} = 121\mu s$ .

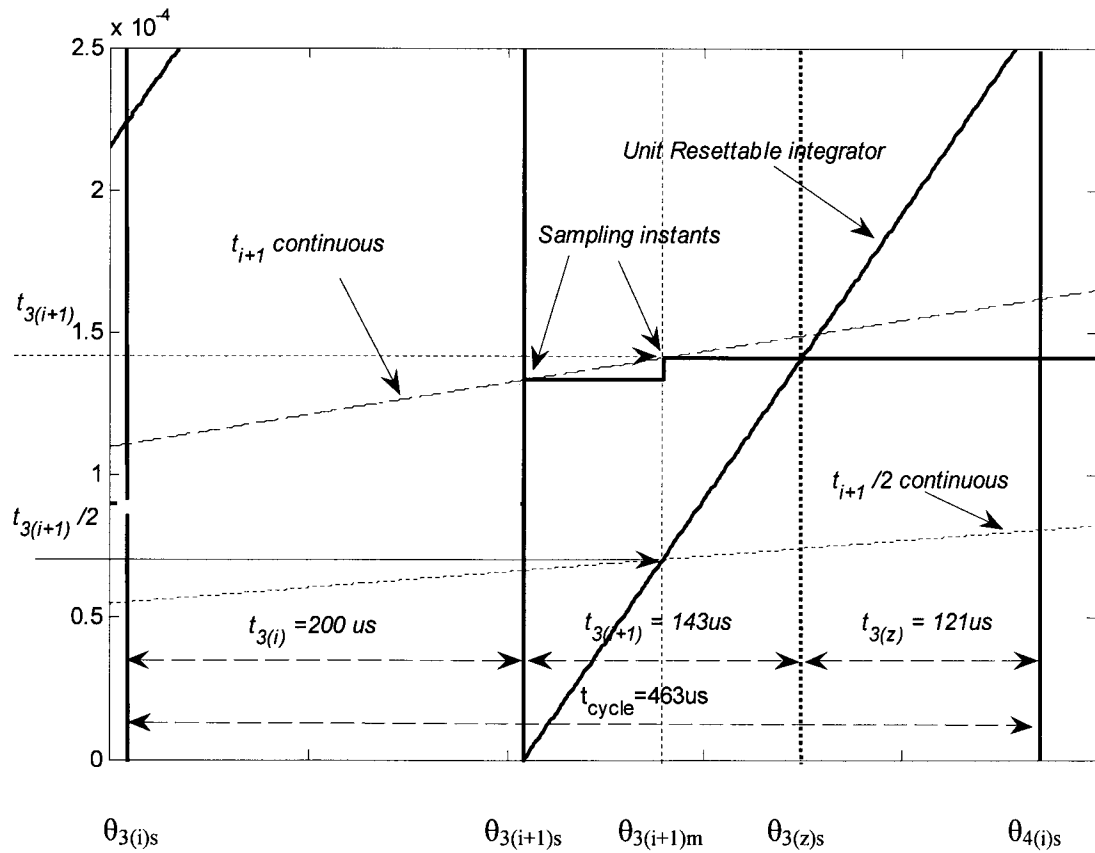


Fig. 2- 3 :- States  $I_{i+1}$  and  $I_z$  ON time calculation when SQ1-RM is used.

Fig. 2- 4 illustrates how state  $I_z$  ON time is calculated when SQ2-RM is used and  $m_a = 0.7$ . There the continuous ON time for state  $I_z$  in the 3<sup>rd</sup> cycle is shown as a dashed curve. It also shows continuous  $t_z/2$  as dotted. Sampling is done two times per SVM cycle for state  $I_z$ , one when  $I_z$  is starting at  $\theta_{3(z)s}$ , and the second is in the middle of  $I_z$ , that is  $\theta_{3(z)m}$  for cycle 3, two edges sampling. A unit input resettable integrator and sampled  $t_z$  presented by heavy lines are used to calculate state  $I_z$  ON time. The sample in the middle of state  $I_z$  which is  $t_{3(z)m}$ , defines the state  $I_z$  ON time in cycle 3.

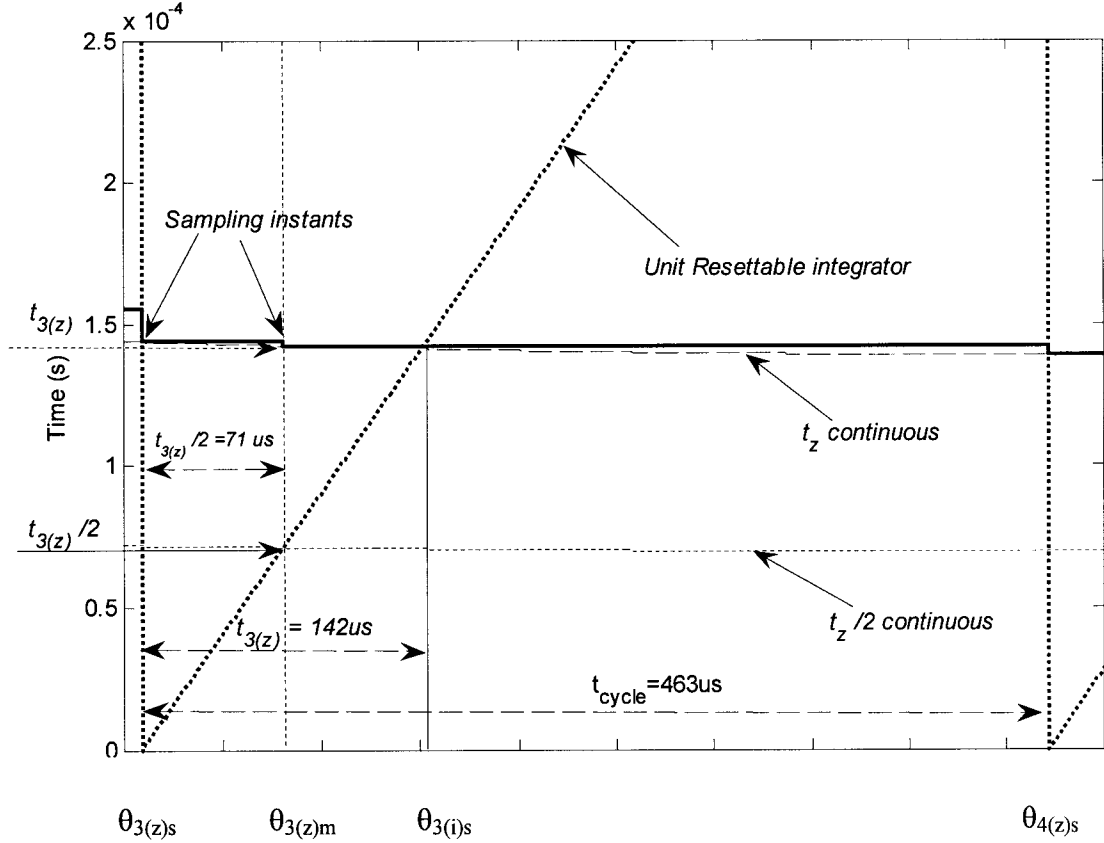


Fig. 2- 4 :- State  $I_z$  ON time calculation when SQ2-RM is used.

Fig. 2-5 shows how  $t_i$  and  $t_{i+1}$  are calculated for SQ2-RM, the procedure of implementing  $t_i$  is similar to the procedure of calculating  $t_z$ . This is done using two edges

sampling one when  $I_z$  is ended at  $\theta_{3(i)s}$  and the other is in the middle of  $I_i$  ON time at  $\theta_{3(i)m}$ . The ON time of second active state  $t_{i+1}$  does not need to be calculated, it occupies the remainder of the cycle after  $t_z$  and  $t_i$  are calculated. For SQ2-RM when  $m_a = 0.7$  three states ON times for cycle three are in Fig. 2- 5,  $t_{3(z)}=142\mu s$ ,  $t_{3(i)}=185\mu s$  and  $t_{3(i+1)}=136\mu s$ .

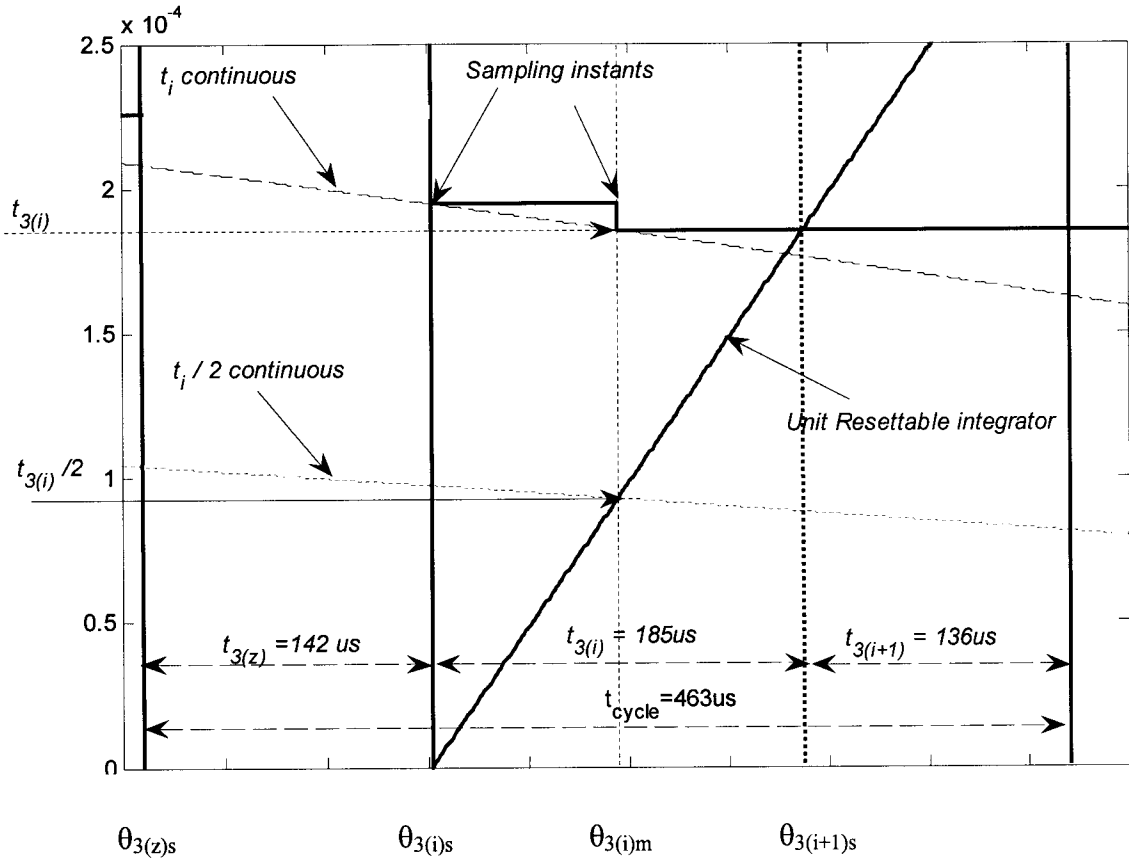


Fig. 2- 5 :- States  $I_i$  and  $I_{i+1}$  ON time calculation when SQ2-RM is used.

One can notice from Fig. 1- 5 in previous chapter that the value of both active states ON times  $t_i$  and  $t_{i+1}$  are varied from  $[0]$  to  $[\frac{\sqrt{3}}{2} t_{cycle} m_a]$  and vice versa inside the SVM sector, which gives large variation for active states inside the SVM cycle. So, not calculating one active state ON time inside SVM cycles should give a large variation in states pulse widths. In SQ1-RM calculated ON times for active states are done, thus

reducing  $HD_{5,7}$ . On the other hand, the value of zero state ON time  $t_z$  is varied from  $[t_{\text{cycle}} (1 - \frac{\sqrt{3}}{2} m_a)]$  to  $[t_{\text{cycle}} (1 - m_a)]$  and vice versa inside the SVM sector, that is a small variation. Also, during  $I_z$  isolation between dc-side and ac-side causes low  $HD_{5,7}$  if the ON time of  $I_z$  is not calculated. In SQ1-RM, when  $t_z$  occupy the remainder of the cycle low  $HD_{5,7}$  is obtained, because the variation of  $t_z$  inside each SVM cycle is small and isolation between dc and ac side current take place.

One can notice that in Fig. 2- 4 the value of continuous  $t_z$  varies between  $138\mu\text{s}$  and  $143\mu\text{s}$  inside cycle 3. While when  $t_z$  occupies the remainder of the cycle after  $t_i$  and  $t_{i+1}$  are passed according to (1- 6) in Fig. 2- 3, then  $t_z = 121\mu\text{s}$ , which is completely different than the value it should be. That mean in SQ1-RM active states ON times are calculated in the middle of their effective periods, which lead  $t_z$  to be completely different than what it should be. Using the same principle in SQ2-RM, there  $t_z$  and  $t_i$  are calculated. On the other hand, in Fig. 2- 3 continuous  $t_{i+1}$  will be around  $160\mu\text{s}$  in the end of cycle three where  $I_{i+1}$  is present, while in Fig. 2- 5  $t_{i+1}$  occupies the remainder of the cycle with  $136\mu\text{s}$ ,  $t_{i+1}$  is completely different than what it should be in SQ2-RM.

Unlike SQ1 and SQ2 with one segment per state, SQ3 has four segments  $t_{z1}$ ,  $t_i$ ,  $t_{i+1}$  and  $t_{z2}$ . Each segment ON time is calculated separately to apply SQ3-RM. The first half zero state ON time  $t_{z1}$  is calculated as a complete state with the same calculation concept as before. When  $m_a = 0.7$  there is  $5\mu\text{s}$  change for  $t_z$  inside entire SVM cycle, half zero state have half of this value,  $2.5\mu\text{s}$ . In the beginning of cycle 3,  $t_z/2$  will be  $71\mu\text{s}$  using RM technique. Fig. 2- 6 illustrates how  $I_i$  ON time is calculated in SQ3-RM technique. This concept is similar to previous techniques, which is using two edges sampling one



when  $I_{z1}$  is ended at  $\theta_{3(i)s}$  and the other is in the middle of  $I_i$  at  $\theta_{3(i)m}$ . A Resettable integrator is used with sampled value of  $t_i$  in the middle of state to calculate  $t_{3(i)}$ .

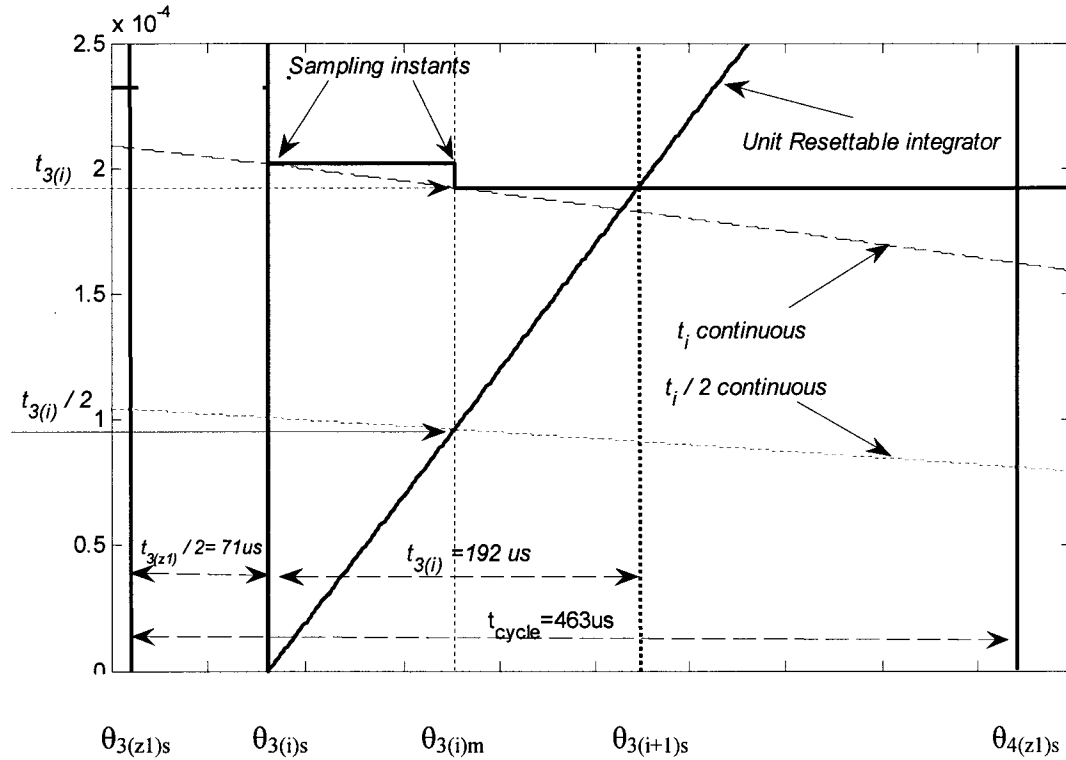


Fig. 2- 6 :- State  $I_i$  ON time calculation when SQ3-RM is used.

Fig. 2- 7 shows how  $t_{i+1}$  and  $t_{z2}$  are calculated for SQ3-RM, the procedure of calculating  $t_{i+1}$  is similar to the one of  $t_i$ . That is done by using two edges sampling one when  $I_i$  is ended at  $\theta_{3(i+1)s}$  and the other is in the middle of  $I_{i+1}$  ON time at  $\theta_{3(i+1)m}$ . A Resettable integrator is used with both sampled  $t_{i+1}$  value to calculate state  $I_{i+1}$  ON time. The ON time of second half of zero state  $t_{z2}$  does not need to be calculated, it occupies the remainder of the cycle after  $t_z$ ,  $t_i$  and  $t_{i+1}$  are calculated. For SQ3-RM when  $m_a = 0.7$ , three states ON times for sector three are seen in Fig. 2- 7. There  $t_{3(z1)} = 71\mu s$ ,  $t_{3(i)} = 192\mu s$ ,  $t_{3(i+1)} = 149\mu s$  and  $t_{3(z2)} = 51\mu s$ .

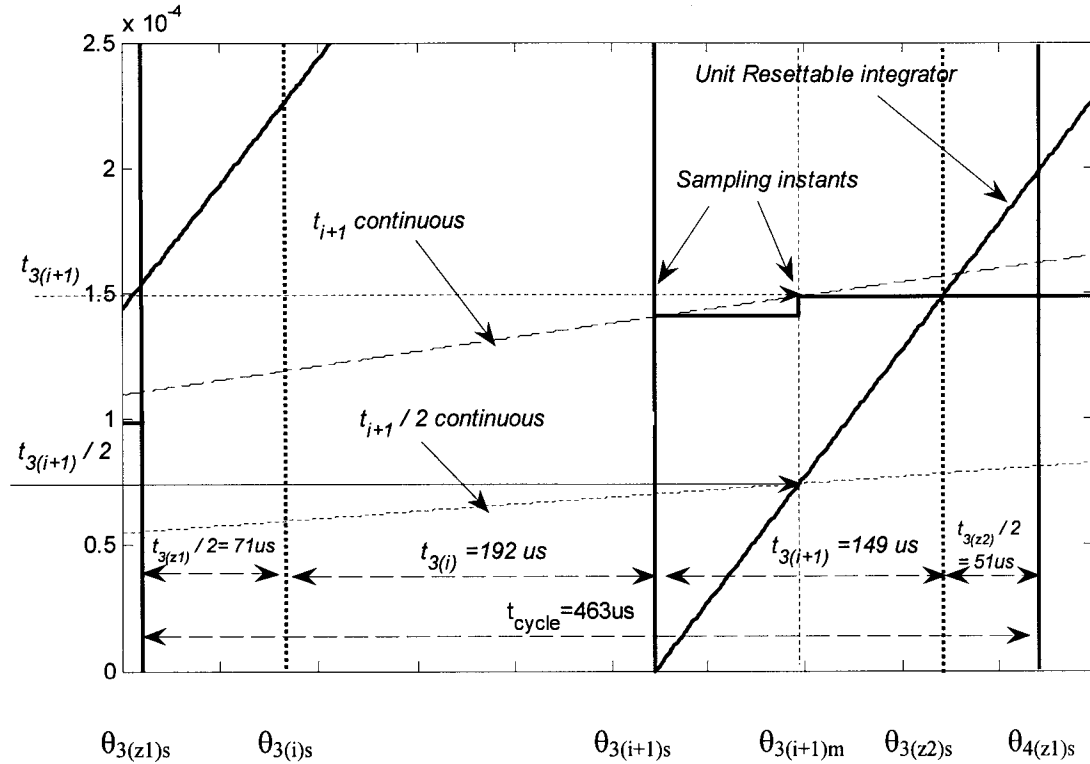


Fig. 2- 7 :- State  $I_{i+1}$  and  $I_z$  ON time calculation when SQ3-RM is used.

### 2.3. PERFORMANCE COMPARISON BETWEEN SAS, SAM AND RM

In this chapter, a modification in SVM for CSC states ON time calculations is proposed. A comparison to measure the improvement in the harmonic spectrum should be done. UPF between CSC ac-side capacitor voltage and reference current ( $m_a$ ) is selected for HD<sub>5-7</sub> performance comparison. The dc-side load is 100mH/5 $\Omega$ , for smooth dc-side current. Overlap period is not included in simulation to measure harmonics generated from SVM weakness in this chapter. To avoid errors in some SIMULINK programs, a simulation step of less than 0.5 $\mu$ s overlap period is used.

The three states ON times calculation techniques presented till now (SAs, SAM and RM) are direct technique; they have a predefined procedure to calculate the states ON times. The index used for HD<sub>5-7</sub> is introduced in (2- 1).

$$HD_{5-7} = \frac{\sqrt{I_{(5th)}^2 + I_{(7th)}^2}}{I_{(1st)}} 100 \quad (2-1)$$

A performance comparison for three states ON times calculation techniques, SAs, SAm and RM for SQ1 (they are SQ1-SAs, SQ1-SAm and SQ1-RM) is introduced in Fig. 2- 8. Those result are obtained with a step change in  $m_a = 0.05$ ,  $HD_{5-7}$  is taken for  $m_a = 0.05, 0.1, \dots, 1$ . Then results are connected together. In Fig. 2- 8 SQ1-RM states ON times calculation is presenting a good performance and much lower  $HD_{5-7}$  than sampling techniques. When  $m_a = 0.7$  all three techniques  $HD_{5-7}$  simulation results are in Fig. 2- 9. There one can conclude that SQ1-RM is presenting 60% reduction in  $HD_{5-7}$  if compared with sampling techniques for SQ1.

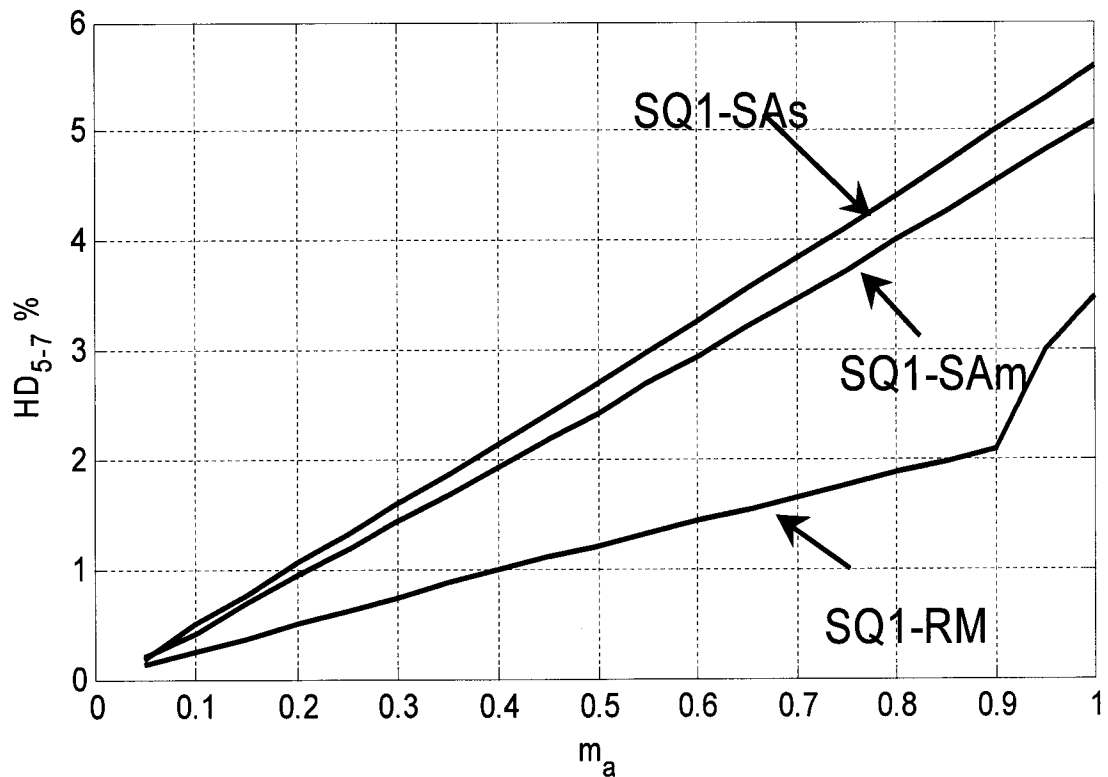
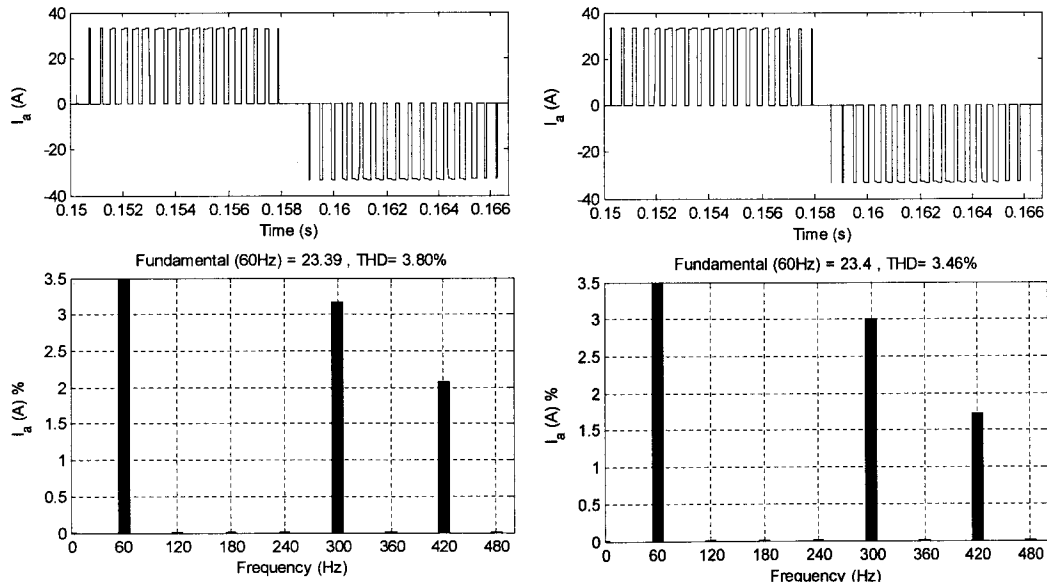


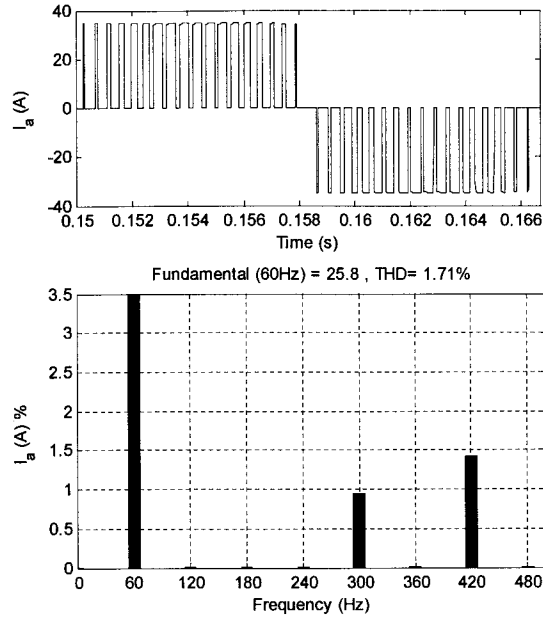
Fig. 2- 8 :- Index  $HD_{5-7}$  measured for sequence one with direct techniques, i.e. SQ1-SAs, SQ1-SAm and SQ1-RM.

In SQ1- RM,  $t_i$  and  $t_{i+1}$  are calculated in the middle of their effective period while  $t_z$  occupies the remainder of the cycle without calculation. In spite of that  $m_a = 0.7$  in all three techniques, there is 2A increment in the fundamental current for SQ1- RM in Fig. 2- 9. That can be deemed to the way of calculating  $t_i$  and  $t_{i+1}$  in SQ1-RM. In SQ1-RM,  $I_i$  is calculated in the beginning of the SVM cycles where  $t_i$  tends to increase in as shown in Fig. 2- 2. And,  $t_{i+1}$  is calculated near the end of the SVM cycles where it tends to increase. Consequently,  $t_z$  tends to decrease in all SVM cycles. With same  $m_a$  SQ1-RM will have more active states ON times and less zero state ON time than SAs and SAM. That leads to an *early* over modulation in SQ1- RM. This is not a critical issue, in closed loop applications  $m_a$  is slightly changed to give the same ac-side fundamental component. The current in SQ1-RM when  $t_i$ 's are calculated near the beginning of the cycle while  $t_{i+1}$ 's are calculated near the end of the cycle tend to increase. Over modulated appears when  $t_z < 0$  in any SVM cycle, that happened in SQ1-RM for  $m_a > 0.9$ . That is why in Fig. 2- 8 there are a sudden increment in  $HD_{5-7}$  for  $0.9 < m_a < 1$ , when SQ1-RM is used.



(a) SQ1-SAs

(b) SQ1-SAM



(c) SQ1-RM

Fig. 2- 9 :- Index  $HD_{5-7}$  in the SVM-CSC ac-side current for different states ON times calculation techniques with SQ1 when  $m_a = 0.7$ .

A performance comparison for three states ON times calculation techniques, SAs, SAm and RM for SQ2 is introduced in Fig. 2- 10, all techniques are presenting high  $HD_{5-7}$ .  $HD_{5-7}$  simulation results with  $m_a = 0.7$  are in Fig. 2- 11. In SQ2-RM,  $t_z$  and  $t_i$  are calculated in the middle of their states ON times, while  $t_{i+1}$  occupy the remainder of the cycle without calculation. Calculate both active states ON times improves  $HD_{5-7}$ , none of them should occupy the remainder of the cycle without calculation, which gives high  $HD_{5-7}$  in SQ2-RM. When  $I_z$  occupies the remainder of the cycle without calculated, that has a smaller impact on  $HD_{5-7}$ . When  $t_z$  is calculated no increment in current appears in SQ2-RM compared with SQ2-SAs and SQ2-SAm. All fundamental current components are nearly the same in Fig. 2- 11, without *early* over modulation.

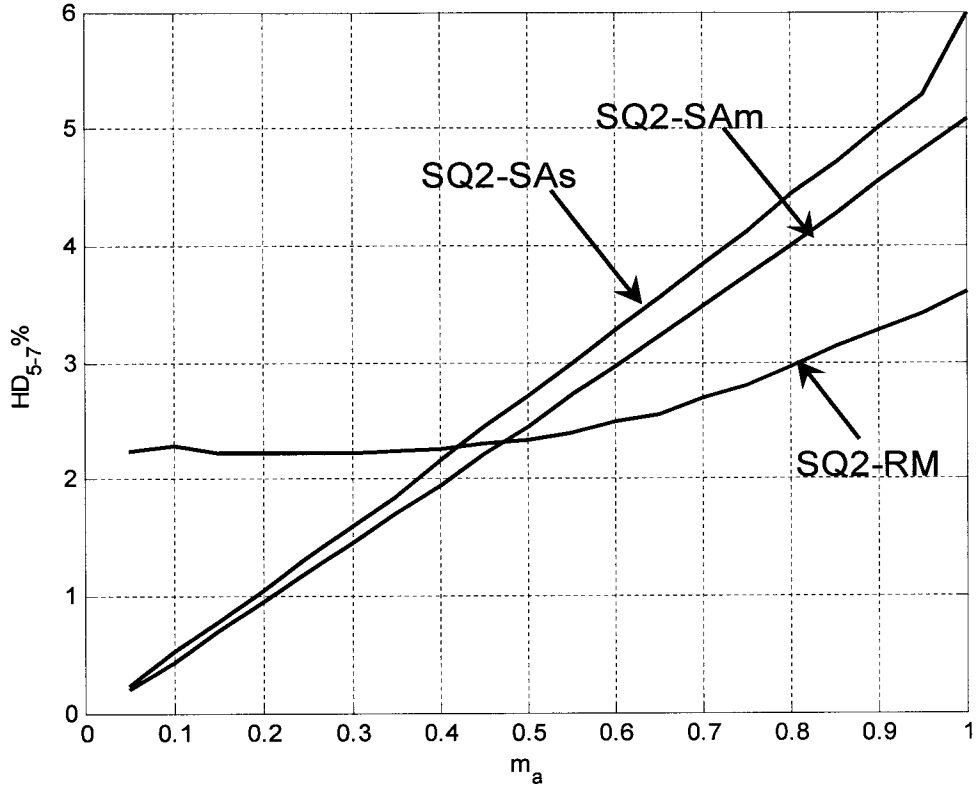
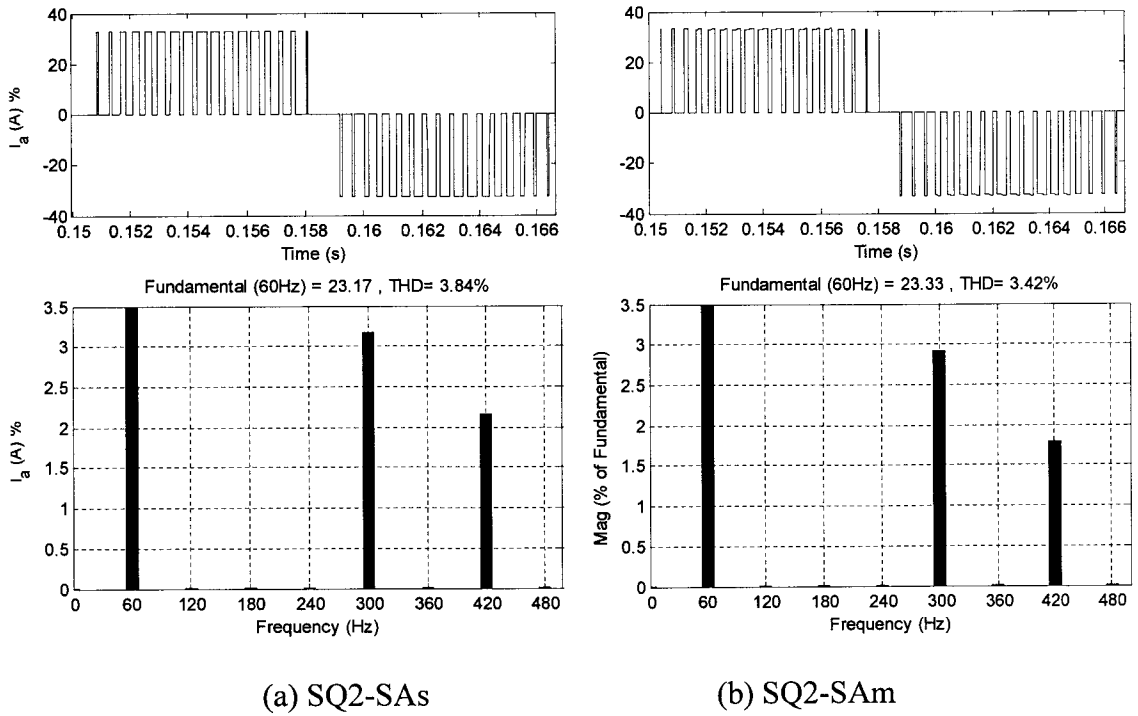
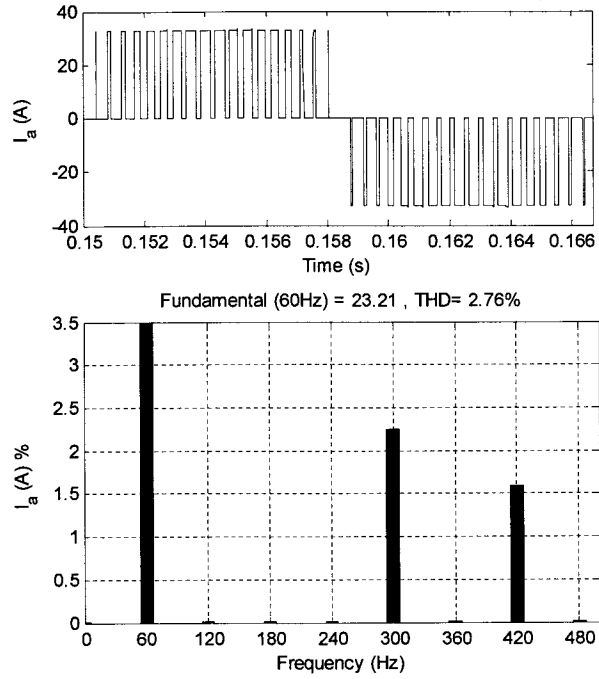


Fig. 2- 10 :- Index HD<sub>5-7</sub> measured for SQ2-SAs, SQ2-SAm and SQ2-RM.





(c) SQ2-RM

Fig. 2- 11 :- Index  $HD_{5-7}$  in the CSC ac-side current for different states ON times calculation techniques with SQ2 when  $m_a = 0.7$ .

A performance comparison for three states ON times calculation techniques, SAs, SAm and RM for SQ3 is introduced in Fig. 2- 12. There SQ3-RM states ON times calculation is presenting lower  $HD_{5-7}$  than sampling techniques. Three techniques  $HD_{5-7}$  simulation results with  $m_a = 0.7$  are in Fig. 2- 13. With SQ3-RM around 90 % reductions in  $HD_{5-7}$  take place. In SQ3-RM  $t_{z1}$ ,  $t_i$  and  $t_{i+1}$  are calculated in the middle of their states ON times while  $t_{z2}$  occupies the remainder of the cycle without calculation. When active states ON times are calculated that yielding reduced  $HD_{5-7}$ .

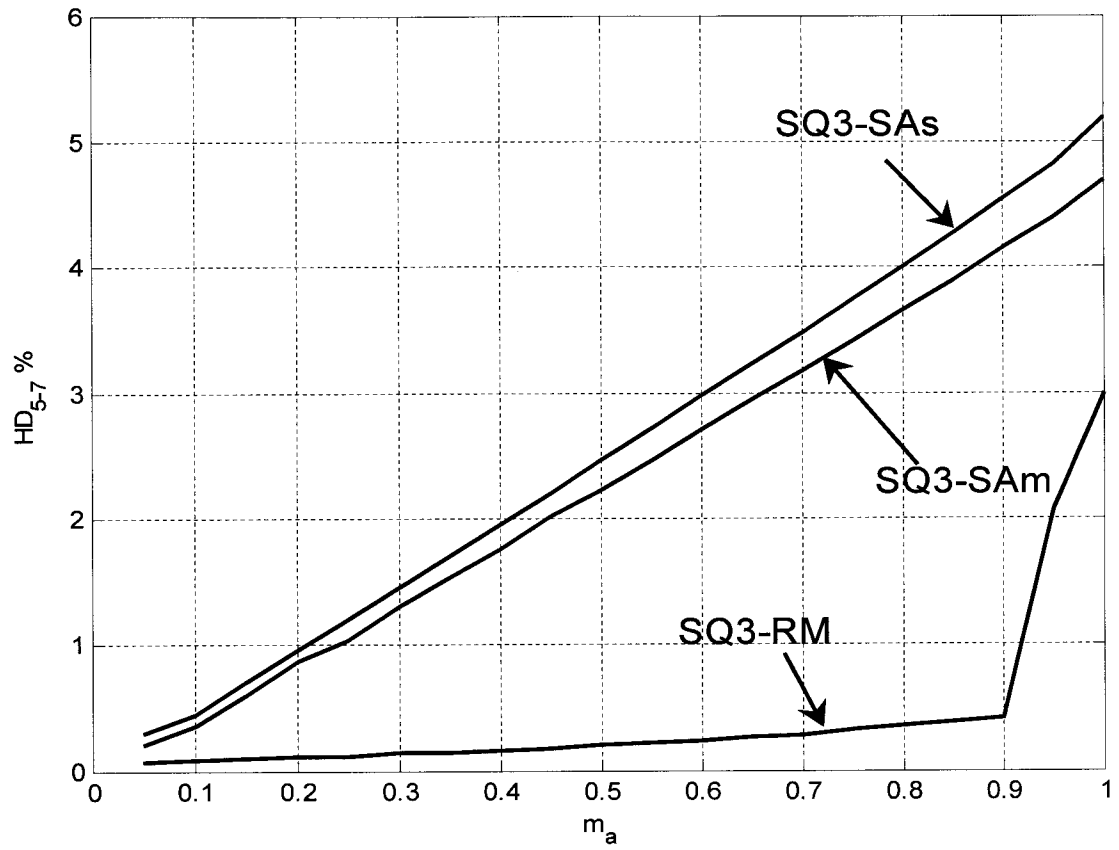
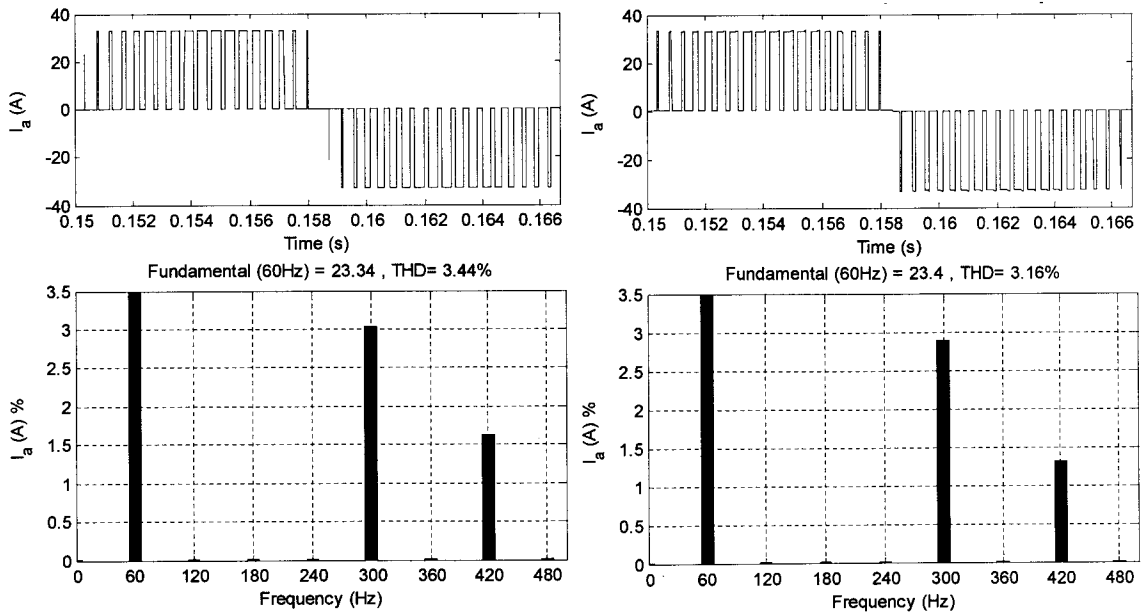


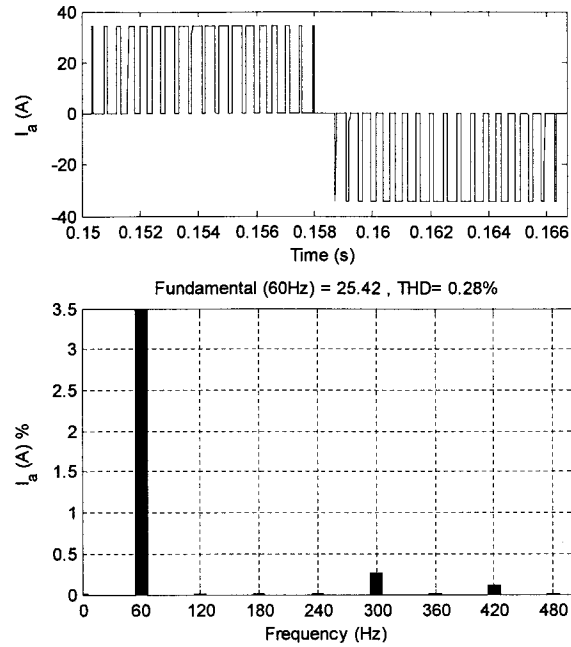
Fig. 2- 12 :- Index  $HD_{5,7}$  measured for SQ3-SAs, SQ3-SAm and SQ3-RM.



(a) SQ3-SAs

(b) SQ3-SAm





(c) SQ3-RM

Fig. 2- 13 :- Index  $HD_{5-7}$  in the CSC ac-side current for different states ON times calculation techniques with SQ3 when  $m_a = 0.7$ .

## 2.4. CONCLUSION

Up to 6%  $HD_{5-7}$  is generated in SVM-CSC when SQ1-SAs is used and  $f_{cycle} = 2160$  Hz, that has been reported in previous research [6], [33]. SQ3, presented in Fig. 1- 7 (c), is the least  $HD_{5-7}$  sequence when SAs is used. SQ3-SAs is presenting 10% reduction in  $HD_{5-7}$  when compared with SQ1-SAs. Besides, 10% reduction in  $HD_{5-7}$  can be achieved if SAm is used along with SQ3 in SQ3-SAm. Those 20% reduction of  $HD_{5-7}$  were not sufficient to satisfy IEEE recommendations for THD. The main reasons of those LOH were usually deemed to snubber circuited, overlap periods, CSC switches tolerance, input ac-side filter and distortion in the capacitor voltage [6] – [36]. These parameters do affect  $HD_{5-7}$  to a certain extent, but the main reason of  $HD_{5-7}$  discovered here is the way

the reference rotating vector has been synthesized. The vector responsible for implementing states in SVM-CSC is rotating all the time, while in sampling the vector is sampled in one instant each SVM cycle.

In LSF the SVM cycle is elapsed  $463\mu\text{s}$  if  $f_{\text{cycle}} = 2160$  Hz. The RM technique is proposed to calculate states ON. In RM, improvement in  $\text{HD}_{5-7}$  can be obtained by calculating the states ON times at different moments, in the middle of each state appearing period. That permits respecting only calculations of two states ON times from three in the sequence, while the third states occupies the remainder of the cycle without calculations. If both active states ON times calculation are respected around 60% reductions in  $\text{HD}_{5-7}$  can be reached in SQ1-RM. The best performance is achieved with SQ3-RM, where active states placed in the middle of the sequence, with around 90% reduction in  $\text{HD}_{5-7}$  compared with standard SVM.

## CHAPTER 3

### 3. NEW SVM EQUATIONS TO REDUCE LOH IN LSF-CSC

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#### 3.1. INTRODUCTION

In the previous chapter,  $HD_{5-7}$  was reduced with a certain procedure based on estimating ON times for the state, and modifying it in the middle of the state existing period. That was not done for all states, the last state is occupied the remainder of the cycle. That led to a search for a sequence adjusting the last state ON time by itself, sequence three. In certain cases, like hybrid CSC topologies in part two of this thesis, the states sequence is not adjusted by our hope but the topology itself adds a restriction on the states sequence.

In this chapter, the calculation of the ON times for states as the reference vector rotates is extended. If the states are used sequentially and each ON time is calculated at the midpoint of the region where it will travel during an estimated ON time, then the sum of ON times for states will not equal to the SVM cycle period, they were not calculated at the same instant. Calculating all states ON times with a set of equations in the beginning of the SVM cycle permits an option for reducing  $HD_{5-7}$ , by recalculate the ON times, so that their sum is equal to the SVM cycle period.

The proposed equations technique is called EQ (Equations), has a concept similar to RM and implemented with a procedure calculates the ON times for states with a set of equations before the SVM cycle is actually started, what cannot be achieved with RM. The ON time of the first state in a given sequence is calculated first, for the reference

vector placed in the midpoint of the region it will cover in an estimated on time. The second state ON time is calculated next, using the same principle but with the estimated time calculated at the moment the previous state is switched off. The ON time of the last state is used for the remainder of the SVM cycle. All those calculations are done in the beginning of the cycle. A correction for EQ (CF) is presented next, in CF all states ON times calculations are done by proposing that the SVM cycle period is not restricted by  $t_{\text{cycle}}$ . After calculating all states ON times, a correction for them depending on the period for SVM cycle  $t_{\text{cycle}}$  is added. This chapter describes how to calculate the ON times of all states for the three states sequences. This chapter material is presented in [51], [52].

## 3.2. SEQUENCE ONE

### 3.2.1. CALCULATION OF STATES ON TIME USING SQ1-EQ

The SVM cycle number  $N_C$  is decided first, where  $N_C = 1, 2 \dots N_{CS}$ . Fig. 3- 1 SIMULINK blocks are using the SVM sector number  $\{[A]\}$  and SVM cycle period (1/2160s) to decide the SVM cycle number  $\{[Nc\_1]\}$ . In SQ1, the first stat is  $I_i$ , its estimated ON time is calculated in the beginning of the SVM cycle at the angle given by (3- 1) in the SVM cycle (C). The estimated ON time of state  $I_i$  in this SVM cycle ( $t_{c(i)s}$ ) is calculated by substituting (3- 1) in (1- 4) and results in (3- 2). The angle at the midpoint of this estimated ON time is calculated in (3- 3). By substituting (3- 3) in (1- 4), the updated value of the ON time of state  $I_i$  is in (3- 4).

$$\theta_{c(i)s} = \frac{60^\circ}{N_{cs}} \times (N_C - 1) \quad (3- 1)$$

For  $N_{CS} = 6$ ,  $N_C$  and  $C = 1, 2 \dots N_{CS}$  then  $\theta_{c(i)s} = 10^\circ \times (N_C - 1)$

$$t_{c(i)s} = t_{\text{cycle}} m_a \sin[60^\circ - 10^\circ \times (N_C - 1)] \quad (3-2)$$

$$\theta_{c(i)m} = \theta_{c(i)s} + \frac{\omega \times t_{c(i)s}}{2}, \quad \text{Where } \omega = 2 \times \pi \times f_{ac} \quad (3-3)$$

$$t_{c(i)m} = t_{\text{cycle}} \times m_a \times \sin \left[ 60^\circ - 10^\circ \times (N_C - 1) - \frac{\omega \times t_{c(i)s}}{2} \right] \quad (3-4)$$

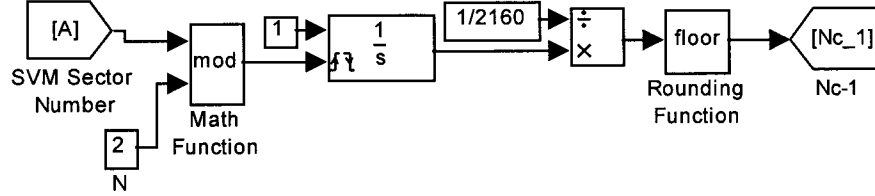


Fig. 3- 1 :- SIMULINK blocks deciding SVM cycle number.

A similar procedure is used for calculating the ON time of the second state ( $I_{i+1}$ ). In such a case, the angle used for calculating the estimated ON time ( $\theta_{c(i+1)s}$ ) is the end angle of the previous state which is given in (3- 5). Thus, the estimated ON time for  $I_{i+1}$  is obtained by substituting (3- 5) in (1- 5) resulting in (3- 6). The angle of the vector in the midpoint of the estimated ON time of  $I_{i+1}$  is calculated as (3- 7), which when substituted in (1- 5) results in (3- 8). Such that  $t_{c(i+1)m}$  is the second state ( $I_{i+1}$ ) calculated ON time.

$$\theta_{c(i+1)s} = 10^\circ \times (N_C - 1) + \omega \times t_{c(i)m} \quad (3-5)$$

$$t_{c(i+1)s} = t_{\text{cycle}} \times m_a \times \sin [10^\circ \times (N_C - 1) + \omega \times t_{c(i)m}] \quad (3-6)$$

$$\theta_{c(i+1)m} = \theta_{c(i+1)s} + \frac{\omega \times t_{c(i+1)s}}{2} \quad (3-7)$$

$$t_{c(i+1)m} = t_{\text{cycle}} \times m_a \times \sin \left[ 10^\circ \times (N_C - 1) + \omega \times t_{c(i)m} + \frac{\omega \times t_{c(i+1)s}}{2} \right] \quad (3-8)$$

The same concept of RM is used in EQ and the ON time of state  $I_z$  occupies the remainder of the SVM cycle. Fig. 3- 2 shows SIMULINK blocks for EQ technique. There,  $m_a$   $\{[ma]\}$ , a pulse in starting of SVM cycle  $\{[B]\}$  and the SVM cycle number

$\{[Nc\_1]\}$  are used to generate  $t_{c(i)m}$   $\{[tcim]\}$  and  $t_{c(i+1)m}$   $\{[tci1m]\}$  with (3- 1) to (3- 8),  $t_{c(i)m}$  and  $t_{c(i+1)m}$  are used to calculate both active states ON times.

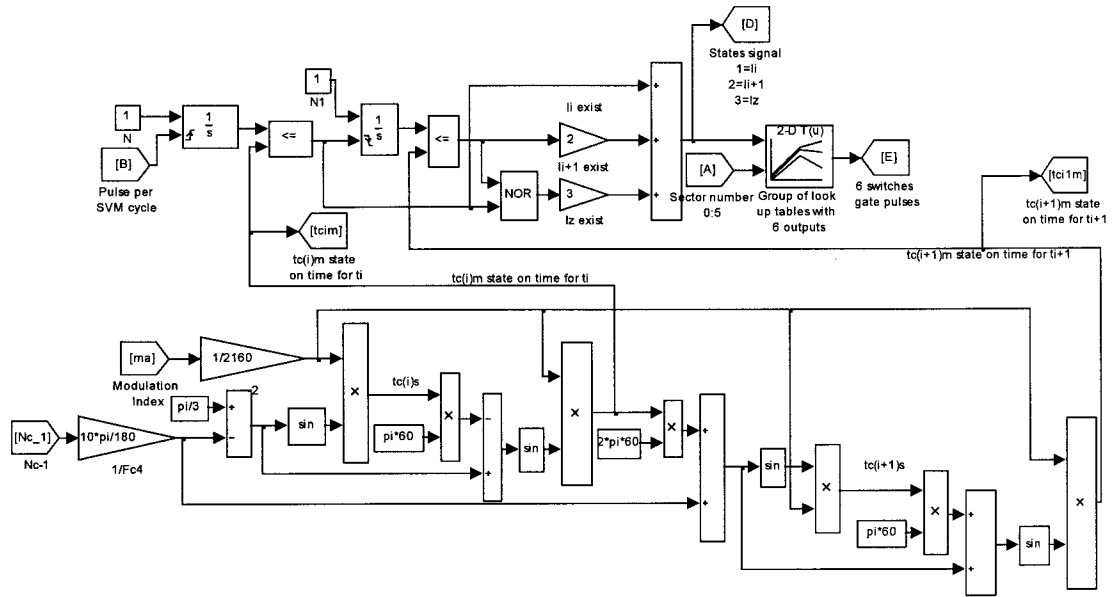


Fig. 3- 2 :- SIMULINK blocks used in calculating states ON times for SQ1-EQ.

A graphical demonstration of the calculation of the ON times for active states  $I_i$  and  $I_{i+1}$  in the 3<sup>rd</sup> cycle with SQ1-EQ is presented in Fig. 3- 3. The curves described by (1- 4) and (1- 5) are not used in EQ. For the 3<sup>rd</sup> cycle starting at  $\theta_{3(i)s}$  the  $t_{3(i)s}$  is obtained using (3- 2). This time is converted to angle by multiplying it with a constant and half of it is added to the  $\theta_{3(i)s}$ . This angle,  $\theta_{3(i)m}$ , generated from (3- 3) is used to obtain the actual ON time for state  $I_i$ , which is  $t_{3(i)m}$  on the vertical axis of Fig. 3- 3 using (3- 4).

The process of calculating  $I_{i+1}$  and  $I_i$  is identical. For the ON time of state  $I_{(i+1)}$  calculations the starting angle is  $\theta_{3(i+1)s}$ . The angle where state  $I_i$  is ended is calculated from (3- 5). Then one obtains the value of  $t_{3(i+1)s}$  from (3- 6) at the vertical axis using  $\theta_{3(i+1)s}$ . This time value is converted to angle by multiplying it with a constant and half of

it is added to  $\theta_{3(i+1)s}$  in the horizontal axis as shown in (3- 7). This angle,  $\theta_{3(i+1)m}$ , is used to obtain the actual ON time for state  $I_{i+1}$  on the vertical axis according to (3- 8) in Fig. 3- 3.

In SQ1-EQ when  $m_a = 0.7$  the values of  $t_{3(i)m}=200\mu s$  and  $t_{3(i+1)m}=143\mu s$ . Active states ON times in SQ1-EQ and SQ1-RM in Fig. 2- 2 are the same. The difference is that in SQ1-EQ all states ON times are known in the beginning of SVM cycle and calculated before the SVM cycle is started. While in SQ1-RM the ON time for each state is available in its middle without opportunity of changing those ON times if they are not achieving the least  $HD_{5-7}$ .

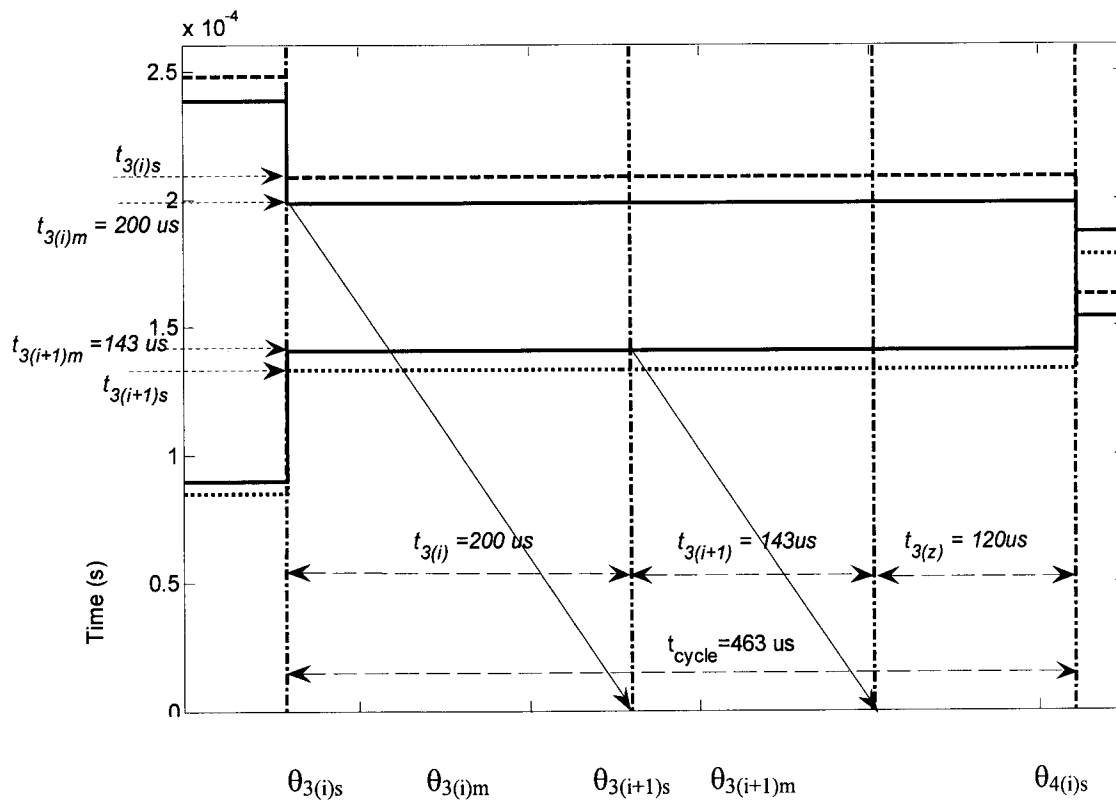


Fig. 3- 3 :- Graphical presentation for SQ1-EQ in the 3<sup>rd</sup> cycle of 6.

### 3.2.2. CALCULATION OF STATES ON TIMES USING SQ1-CF

In SQ1-EQ the zero state is not calculated. This can result in an ON time different from the ON time that would be calculated as for the other active states. To solve this problem a correction factor ( $K_C$ ) is used in a scheme called SQ1-CF. First, the ON times of all states are calculated for the reference vector in the midpoint of the region where each one will travel during estimated ON times. The values of  $t_{c(i)m}$  and  $t_{c(i+1)m}$  are calculated from (3- 4) and (3- 8). The calculation of  $t_{c(z)m}$  is described next. The starting angle for  $t_z$  exists when  $I_{i+1}$  is finished using (3- 9). The estimated ON time of the  $t_z$  is obtained in (3- 10). The angle at the midpoint of this estimated ON time is calculated in (3- 11). Finally, the updated ON time for the zero state is calculated in (3- 12).

$$\theta_{c(z)s} = 10^\circ \times (N_C - 1) + \omega \times t_{c(i)m} + \omega \times t_{c(i+1)m} \quad (3- 9)$$

$$t_{c(z)s} = t_{\text{cycle}} \times [1 - m_a \times \sin(60^\circ - \theta_{c(z)s}) - m_a \times \sin(\theta_{c(z)s})] \quad (3- 10)$$

$$\theta_{c(z)m} = \theta_{c(z)s} + \frac{\omega \times t_{c(z)s}}{2} \quad (3- 11)$$

$$t_{c(z)m} = t_{\text{cycle}} \times [1 - m_a \times \sin(60^\circ - \theta_{c(z)m}) - m_a \times \sin(\theta_{c(z)m})] \quad (3- 12)$$

SIMULINK blocks used for implementing SQ1-CF technique are shown in Fig. 3- 4. There both of  $t_{c(i)m}$   $\{[tcim]\}$  and  $t_{c(i+1)m}$   $\{[tcilm]\}$  are calculated for preliminary estimation of active states ON times using blocks in Fig. 3- 2. Then the preliminary estimation  $t_{c(z)m}$  is calculated in similar procedure in Fig. 3- 4 with (3- 12). Since the sum of those three ON times ( $t_{c(i)m}$ ,  $t_{c(i+1)m}$  and  $t_{c(i+1)m}$ ) is likely different from the SVM cycle ( $t_{\text{cycle}}$ ), those preliminary estimated ON times for states shall be multiplied by a  $K_c$  defined in (3- 13). Then the final ON times for active states  $t_{c(i)f}$  and  $t_{c(i+1)f}$  are calculated using  $K_c$ , they are  $t_{c(i)m}$  and  $t_{c(i+1)m}$  in (3- 14) and (3- 15).



$$K_c = \frac{t_{\text{cycle}}}{t_{c(i)m} + t_{c(i+1)m} + t_{c(z)m}} \quad (3-13)$$

$$t_{c(i)f} = K_c \times t_{c(i)m} \quad (3-14)$$

$$t_{c(i+1)f} = K_c \times t_{c(i+1)m} \quad (3-15)$$

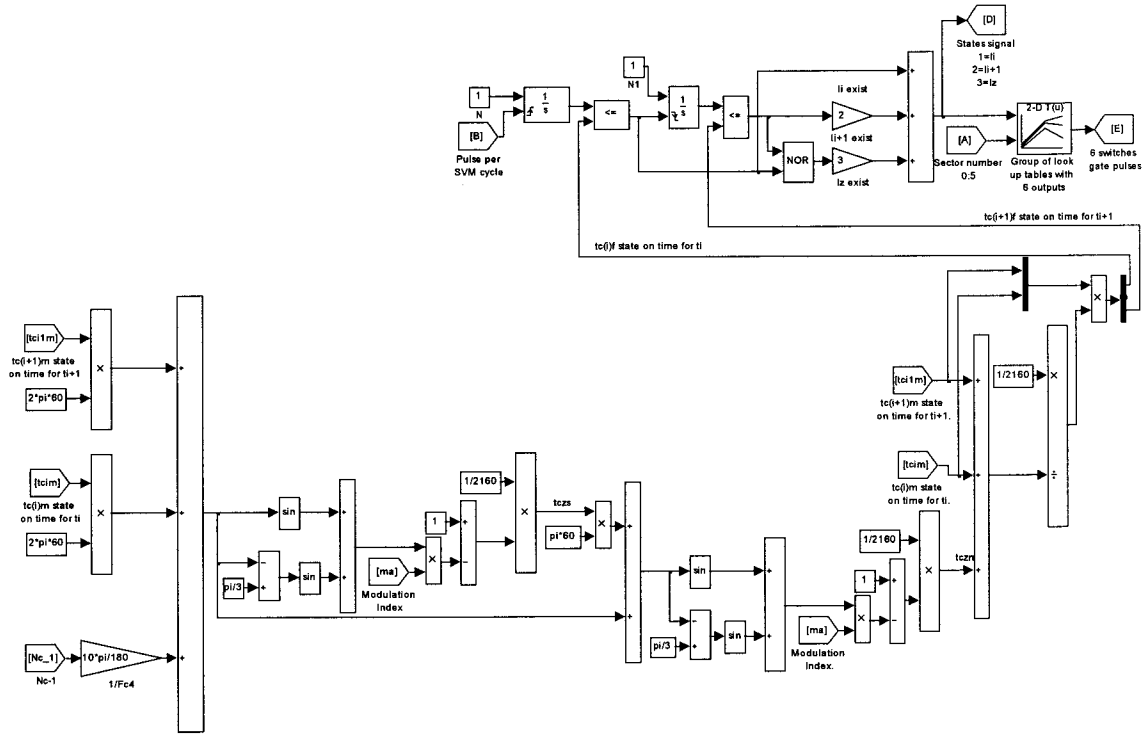


Fig. 3- 4 :- SIMULINK blocks used in calculating states ON times for SQ1-CF.

The correction of active states ON times using (3- 14) and (3- 15) is done in the beginning of a SVM cycle. That is possible because the Preliminary states ON times  $t_{c(i)m}$ ,  $t_{c(i+1)m}$  and  $t_{c(z)m}$  are calculated in the beginning of the SVM cycle. The Preliminary states ON  $t_{c(i)m}$  and  $t_{c(i+1)m}$  are multiplied with  $K_c$  to get the values of  $t_{3(i)f}$  and  $t_{3(i+1)f}$ . Fig. 3- 5 shows  $K_c$  for one SVM sector cycles when  $m_a = 0.7$  in SQ1-CF.  $K_c$  is varying from SVM cycle to the other with maximum of 0.988 and minimum of 0.938.

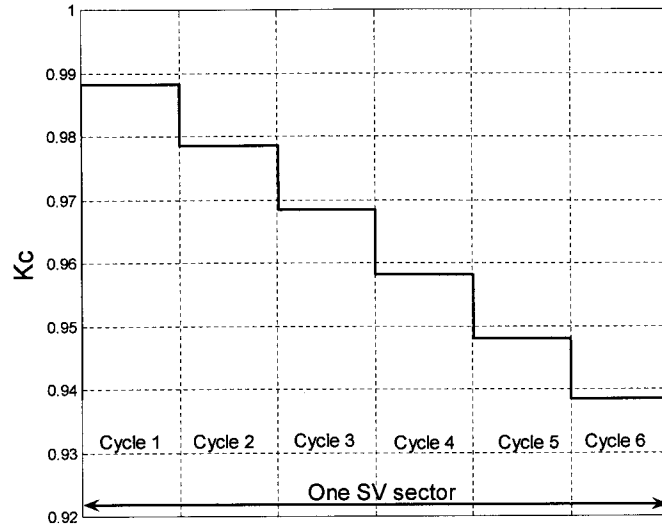


Fig. 3- 5 :-  $K_c$  in one SVM sector cycles with SQ1-CF and  $m_a = 0.7$ .

Vector analysis in sampling is done in the beginning or the middle of the SVM cycle. In EQ, vector analysis is also done but not in the same instant for all states. Here two calculations from the following three calculations are done,  $t_i$  in the middle of the state  $I_i$ ,  $t_{i+1}$  in the middle of the state  $I_{i+1}$  and  $t_z$  in the middle of the state  $I_z$ . That is defined by the author as instantaneous calculations for the two states ON times calculated. The third state is not presented instantaneously. In CF, all three states ON time ( $t_i$ ,  $t_{i+1}$  and  $t_z$ ) are calculated by the same procedure, that is  $t_x$  is calculated in the middle of the state  $I_x$ ,  $x = i, i+1$  and  $z$ . That led the addition of those three states ON times to be different than  $t_{cycle}$ . Thus, they are calculated at different time instant during SVM cycle. The factor  $K_c$  resizes the three states ON times to equal the  $t_{cycle}$ . That is instantaneous calculations for all three states ON times calculated by this procedure.

### 3.2.3. PERFORMANCE OF SQ1-EQ AND SQ1-CF

Fig. 3- 6 illustrates how the index  $HD_{5-7}$  of the input current of the CSC varies with the  $m_a$  for the four schemes. Two when traditional states ON times calculations

SQ1-SAs and SQ1-SAm are used. And, two when the states ON times are calculated with instantaneous calculations of SV, they are SQ1-EQ and SQ1-CF. SQ1-SAs is presenting the worst  $HD_{5-7}$ , followed by the SQ1-SAm then SQ1-EQ schemes. The best result is for SQ1-CF, which presents further reduction in  $HD_{5-7}$  for high values of  $m_a$ .

In SQ1-SAs and SQ1-SAm the SV implementation is depending on the vector analysis in the start and the middle of the SVM cycle, respectively. The SV is rotating all the time. Implementing SVM cycle with states ON times calculated at only one instant each SVM cycle should generate  $HD_{5-7}$ . The instantaneous calculations for active states in SQ1-EQ are reducing  $HD_{5-7}$  to a certain limit. The reduction is increased when states ON times are corrected with SQ1-CF to adjust the zero state ON time, which can be seen in Fig. 3- 6. The  $HD_{5-7}$  for SQ1-CF when  $m_a = 0.6$ ,  $m_a = 0.7$  and  $m_a=0.9$  are shown in Fig. 3- 7.

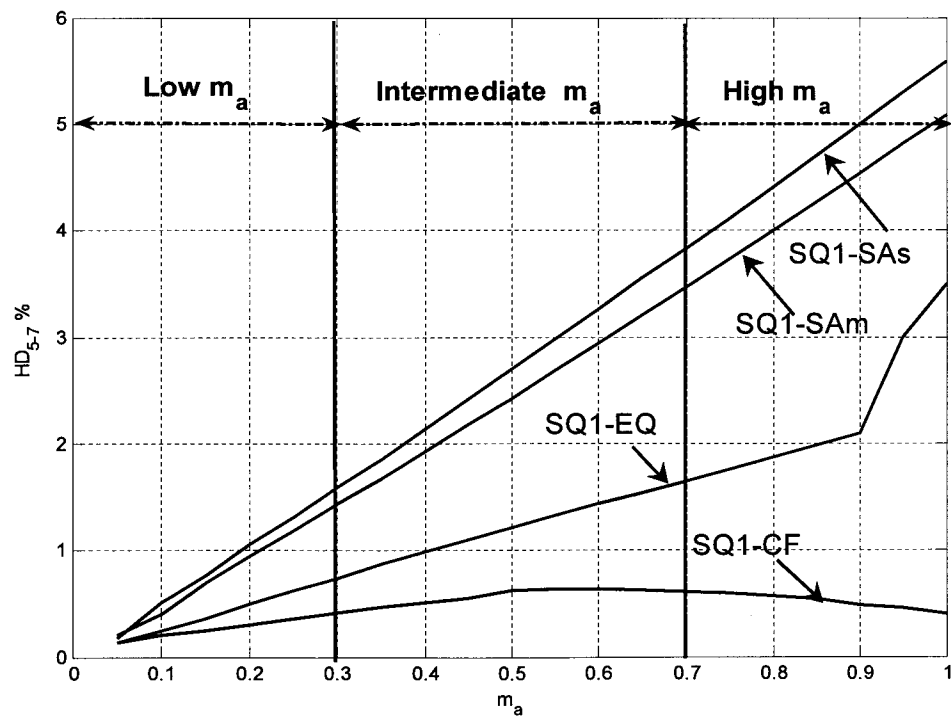
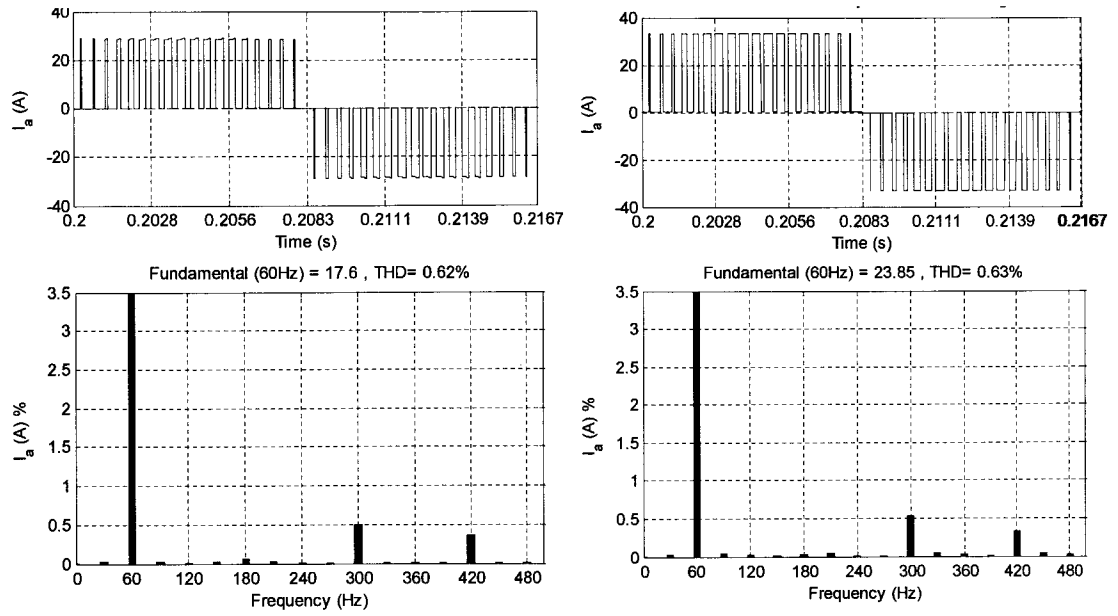
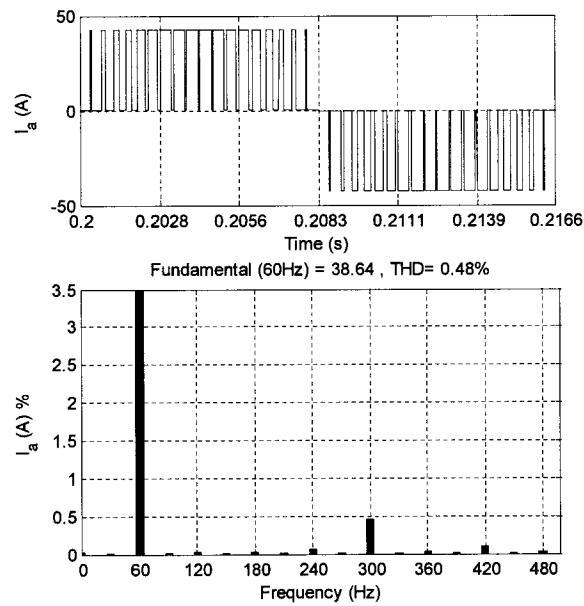


Fig. 3- 6 :- Index  $HD_{5-7}$  for SQ1-SAs, SQ1-SAm, SQ1-EQ and SQ1-CF.



(a)  $m_a = 0.6$ .

(b)  $m_a = 0.7$ .



(c)  $m_a = 0.9$ .

Fig. 3- 7 :- Index  $HD_{5-7}$  in the CSC ac-side current with SQ1-CF at different  $m_a$ 's.

When  $m_a$  increased the weight of active states increase and  $HD_{5-7}$  due to their inaccuracy is increased in SQ1-SAs, SQ1-SAM and SQ1-RM. In Fig. 3- 6 and Fig. 3- 7,  $HD_{5-7}$  is constant for intermediate  $m_a$  (around 0.62%). And,  $HD_{5-7}$  is reduced in high  $m_a$ .

Exact characteristic for  $HD_{5-7}$  in SQ1-EQ and SQ1-CF can be described using one SVM sector cycles states ON times. Resizing active states ON times in SQ1-CF solves the problem of apparent over modulation in SQ1-EQ for  $0.9 < m_a < 1$ . That is noticed from fundamental (60 Hz) current when  $m_a = 0.7$  in Fig. 2- 9 and Fig. 3- 7 (b), it is around 23.5A in SQ1-SAs, SQ1-SAm and SQ1-CF, while it is 25.8A in SQ1-EQ. In SQ1-EQ for the same  $m_a$  the fundamental current is more than other techniques.

$K_c$  resizes the first two states ON times to achieve instantaneous calculations for all states using (3- 13) - (3- 15). For low  $m_a$ , in the range of ( $0 < m_a < 0.3$ ), active states ON times are small when small  $m_a$  value is applied to equations (1- 4) - (1- 6). Both active states have large variation inside SVM cycle while the zero state which is dominant (large) in low  $m_a$  has not. So,  $K_c \approx 1$  in all SVM sector cycles for low  $m_a$  when  $K_c$  is calculated by (3- 13),  $K_c$  impact is minimum. That lead, SQ1-EQ and SQ1-CF results to be similar in low  $m_a$ , where  $HD_{5-7}$  are low in general.

For intermediate  $m_a$ , in the range of ( $0.3 < m_a < 0.7$ ), both active states have large variation inside the same SVM cycle. Fig. 3- 8 (a) shows  $K_c$  for one SVM sector cycles when  $m_a = 0.5$ , it varied from 0.963 to 0.999. In intermediate values of  $m_a$ ,  $K_c$  is reduced and its impact appears. SQ1-EQ where  $K_c$  effect is not taken into consideration results in a sensitive  $HD_{5-7}$ , while SQ1-CF uses  $K_c$  to keep  $HD_{5-7}$  low with intermediate  $m_a$ 's.

For large  $m_a$ , in the range of ( $0.7 < m_a < 1$ ),  $K_c$  variations have high effect in  $HD_{5-7}$ . Fig. 3- 8 (b) shows  $K_c$  for one SVM sector cycles when  $m_a = 0.8$ , it varied from 0.923 to 0.98. As a result of more increment in  $K_c$ , SQ1-EQ with high  $m_a$  results in higher  $HD_{5-7}$  than intermediate  $m_a$ , while SQ1-CF uses  $K_c$  to keep  $HD_{5-7}$  low.  $K_c$  variation with  $m_a$  is proving Fig. 3- 6 results for SQ1-EQ, where  $HD_{5-7}$  increased with  $m_a$  all the time.

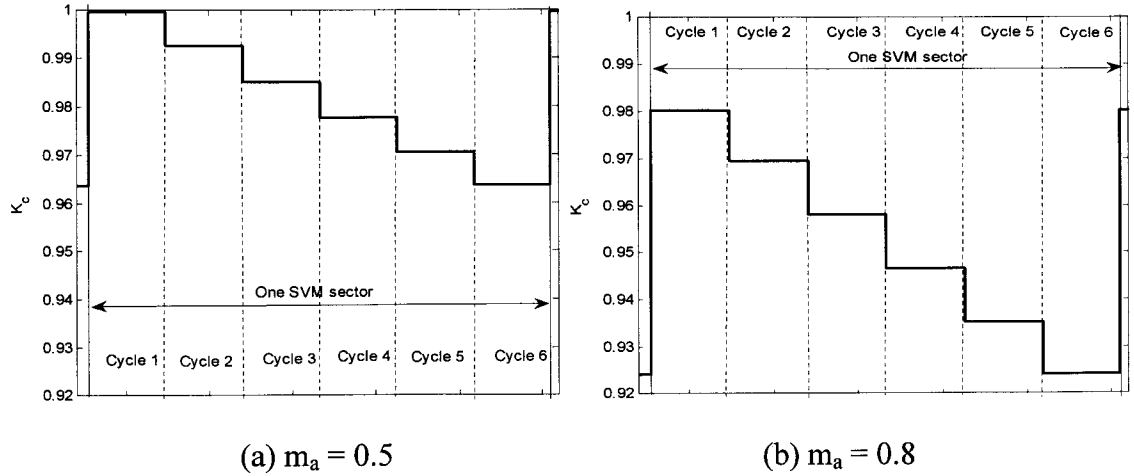


Fig. 3- 8 :-  $K_c$  in one SVM sector cycles when SQ1-CF is used with different  $m_a$ 's.

There are six sectors in the ac-side line cycle. Large differences between summations of states  $t_i$ 's and  $t_{i+1}$ 's in each SVM sector generates  $HD_{5-7}$ . This difference has an impact on  $HD_{5-7}$  for SQ1-CF in Fig. 3- 6. Fig. 3- 9 illustrates states ON times in each SVM cycle for different  $m_a$  when SQ1-CF is used.  $I_i$  and  $I_{i+1}$  states ON times are  $t_{c(i)f}$  and  $t_{c(i+1)f}$ , respectively. The difference between  $t_{3(i)f}$  and  $t_{4(i+1)f}$  gives a direct indication of the difference between  $\sum_{c=1}^{c=6} t_{c(i)f}$  and  $\sum_{c=1}^{c=6} t_{c(i+1)f}$ .  $\sum_{c=1}^{c=6} t_{c(i)f} = \sum_{c=1}^{c=6} t_{c(i+1)f}$  if  $t_{3(i)f} = t_{4(i+1)f}$ . Also, if  $t_{3(i)f} \gg t_{4(i+1)f}$  then  $\sum_{c=1}^{c=6} t_{c(i)f} \gg \sum_{c=1}^{c=6} t_{c(i+1)f}$ . And, if  $t_{3(i)f} \ll t_{4(i+1)f}$  then  $\sum_{c=1}^{c=6} t_{c(i)f} \ll \sum_{c=1}^{c=6} t_{c(i+1)f}$ .

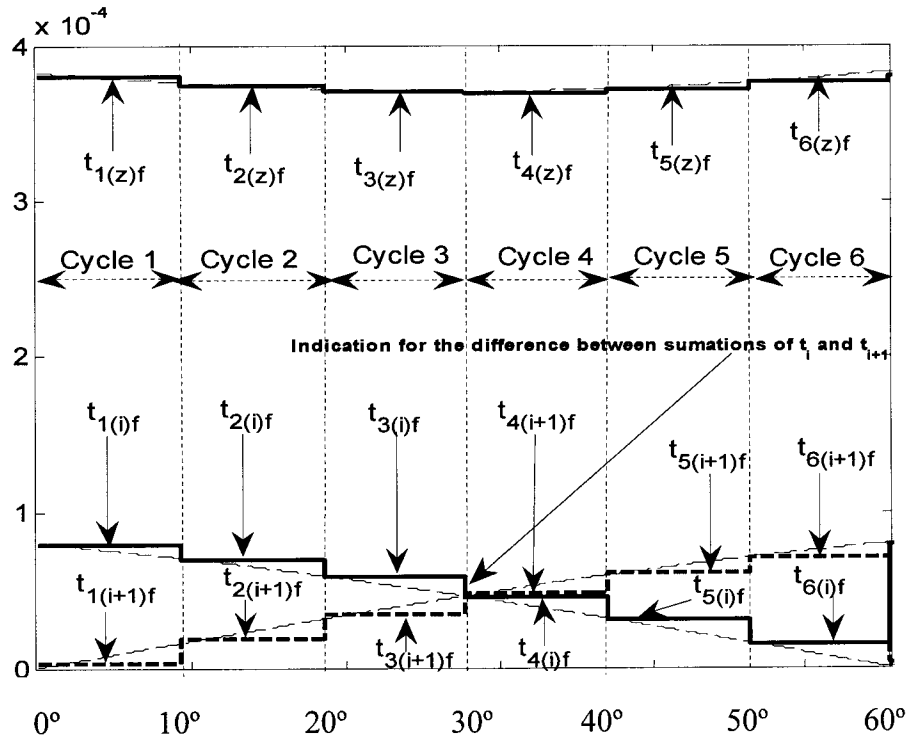
Fig. 3- 9 (a) shows each SVM cycle states ON times for  $m_a = 0.2$  when SQ1-CF is used.  $I_i$ ,  $I_{i+1}$  and  $I_z$  states ON times are  $t_{c(i)f}$ ,  $t_{c(i+1)f}$  and  $t_{c(z)f}$ , respectively. There,  $t_{3(i)f} > t_{4(i+1)f}$ , that lead  $\sum_{c=1}^{c=6} t_{c(i)f} > \sum_{c=1}^{c=6} t_{c(i+1)f}$ , the difference between both summations is not significant because the value of active states ON times are small compared with zero state ON time for low  $m_a$ . This difference generates  $HD_{5-7} = 0.3\%$  when  $m_a = 0.2$  in Fig. 3- 6.

Fig. 3- 9 (b) shows the states ON times for one SVM sector cycles when  $m_a = 0.5$ , there  $t_{3(i)f} \gg \gg t_{4(i+1)f}$ , that lead  $\sum_{c=1}^{c=6} t_{c(i)f} \gg \gg \sum_{c=1}^{c=6} t_{c(i+1)f}$ .  $t_i$ 's and  $t_{i+1}$ 's values are

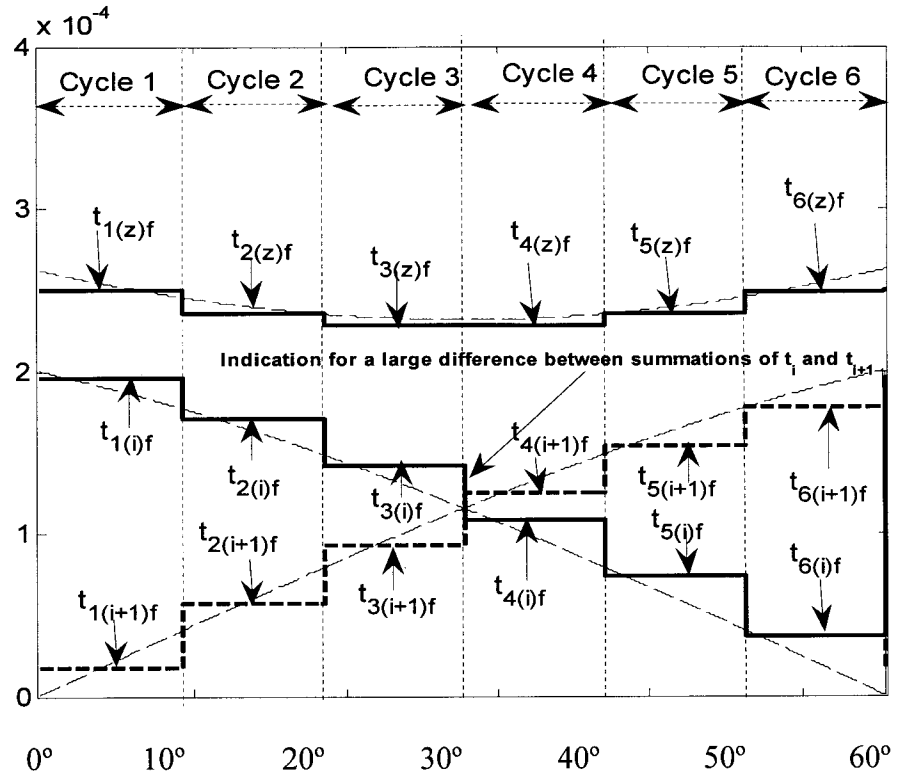
intermediate in this case, but the difference between their summations is big in. So, high  $HD_{5-7}$  exists with intermediate  $m_a$ ,  $HD_{5-7} = 0.64\%$  when  $m_a = 0.5$  as shown in Fig. 3- 6.

Fig. 3- 9 (c) shows the active states ON times for one SVM sector cycles for  $m_a = 0.8$ , there  $t_{3(i)f} > t_{4(i+1)f}$ , that lead  $\sum_{c=1}^{c=6} t_{c(i)f} > \sum_{c=1}^{c=6} t_{c(i+1)f}$ , but the difference between their summations is small and reduced when  $m_a$  increment. So, a reduction of  $HD_{5-7}$  start to appear when  $m_a$  increment,  $HD_{5-7} = 0.57\%$  when  $m_a = 0.8$  as shown in Fig. 3- 6. Also,  $\sum_{c=1}^{c=6} t_{c(i)f} = \sum_{c=1}^{c=6} t_{c(i+1)f}$  at  $m_a = 1$  with more reduction in  $HD_{5-7}$  in Fig. 3- 6.

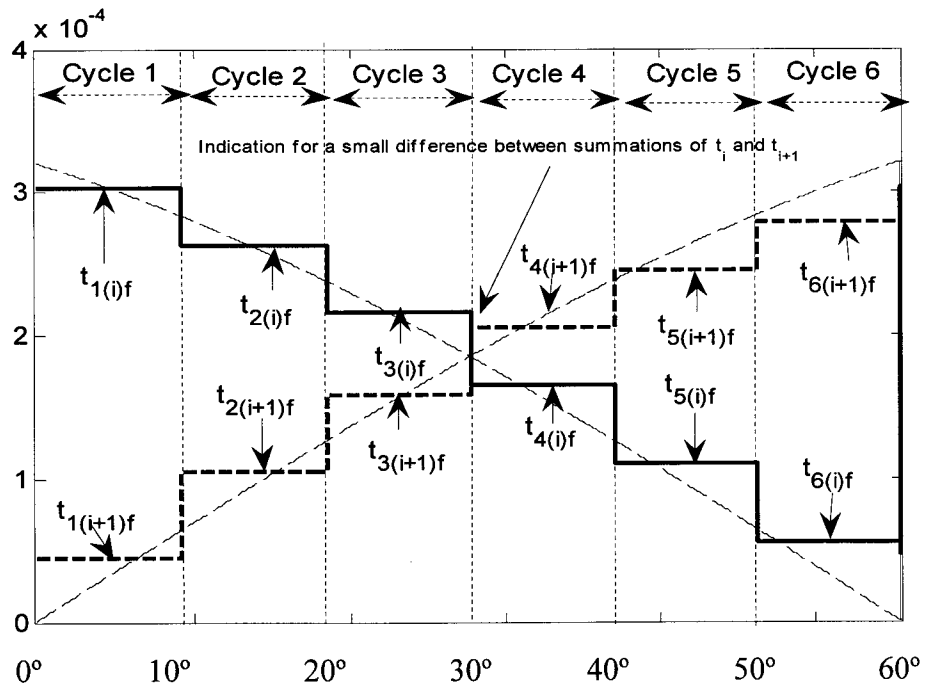
In short, for low  $m_a$  both values of  $t_i$  and  $t_{i+1}$  are small and the difference between active states ON times summations does not affect  $HD_{5-7}$  in SQ1-CF. For Intermediate  $m_a$  this difference is high and  $HD_{5-7}$  increased. In high  $m_a$  this difference started to be reduced until  $m_a = 1$  where it disappeared completely. Thus, for high  $m_a$ ,  $HD_{5-7}$  reduction occurs when  $m_a$  increment take place.



(a)  $m_a = 0.2$



(b)  $m_a = 0.5$



(c)  $m_a = 0.8$

Fig. 3- 9 :- States ON times in one SVM sector cycles for SQ1-CF.



### 3.3. SEQUENCE TWO

#### 3.3.1. CALCULATION OF STATES ON TIME USING SQ2-EQ

Here the zero state comes first. Its estimated ON time is calculated in the beginning of each SVM cycle. There the angle in a given SVM cycle ( $C$ ) is given in (3-16). The zero state estimated ON time is calculated from the estimated ON times of the active states calculated in beginning of the SVM cycle in (3-17). The actual ON time of the zero state is calculated in the middle of the prospected zero state in (3-18). Then, the final value of zero state can be calculated by (3-19). Following the same procedure for the second state, which is  $I_i$  in SQ2, one can find the estimated ON time for  $I_i$  in (3-20) and actual ON time for  $I_i$  in (3-21). The ON time of the second active state, which is  $I_{i+1}$  in SQ2 occupies the remainder of the cycle in SQ2-EQ. SIMULINK blocks achieves SQ2-EQ are shown in Fig. 3-10,  $t_{c(z)m}$  and  $t_{c(i)m}$  are used to calculate the states ON times.

$$\theta_{c(z)s} = 10 \times (N_C - 1) \quad (3-16)$$

$$t_{c(z)s} = t_{\text{cycle}} \times [1 - m_a \times \sin(60^\circ - 10^\circ \times (N_C - 1)) - m_a \times \sin(10^\circ \times (N_C - 1))] \quad (3-17)$$

$$\theta_{c(z)m} = \theta_{c(z)s} + \frac{\omega \times t_{c(z)s}}{2} \quad (3-18)$$

$$t_{c(z)m} = t_{\text{cycle}} \times \left[ 1 - m_a \times \sin\left(60^\circ - 10^\circ \times (N_C - 1) - \frac{\omega \times t_{c(z)s}}{2}\right) - m_a \times \sin\left(10^\circ \times (N_C - 1) + \frac{\omega \times t_{c(z)s}}{2}\right) \right] \quad (3-19)$$

$$t_{c(i)s} = t_{\text{cycle}} \times m_a \times \sin\left(60^\circ - 10^\circ \times (N_C - 1) - \omega \times t_{c(z)m}\right) \quad (3-20)$$

$$t_{c(i)m} = t_{\text{cycle}} \times m_a \times \sin\left(60^\circ - 10^\circ \times (N_C - 1) - \omega \times t_{c(z)m} - \frac{\omega \times t_{c(i)s}}{2}\right) \quad (3-21)$$

A graphical demonstration of the calculation of the ON times for states  $I_z$  and  $I_i$  in the 3<sup>rd</sup> cycle is presented in Fig. 3-11. For a SVM cycle starting at  $\theta_{3(z)}$ ,  $t_{3(z)s}$  is calculated

using (3- 17). This time value is converted to angle, which is used to find  $\theta_{3(z)m}$  from (3- 18). And,  $\theta_{3(z)m}$  is used to obtain the actual ON time for state  $I_z$  on the vertical axis of Fig. 3- 11 using (3- 19). The same calculations are done for state  $I_i$  using (3- 20) and (3- 21).

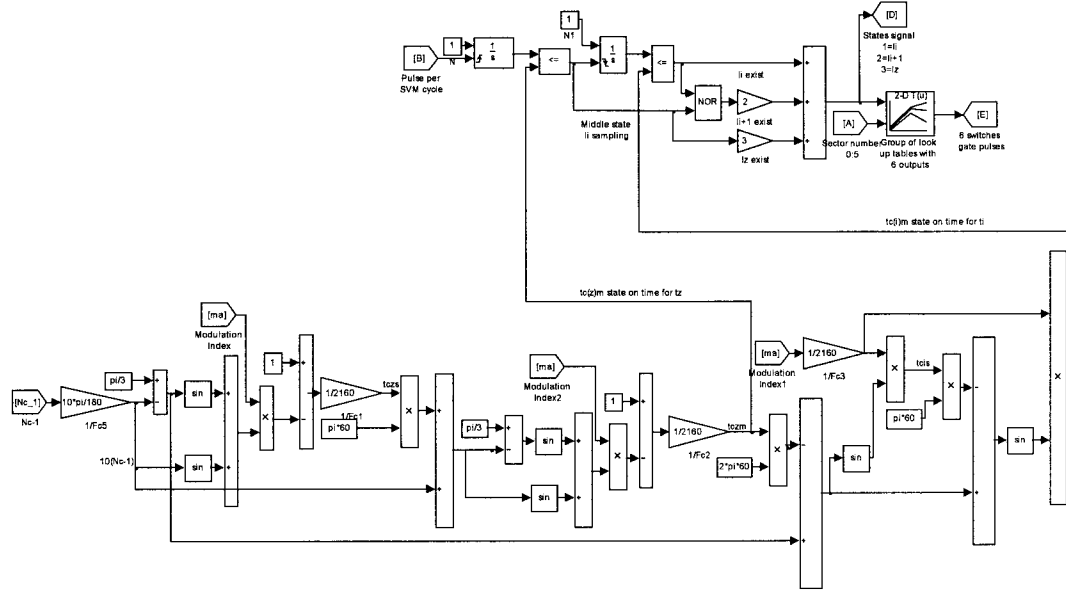


Fig. 3- 10 :- SIMULINK blocks used in deciding states ON times for SQ2-EQ.

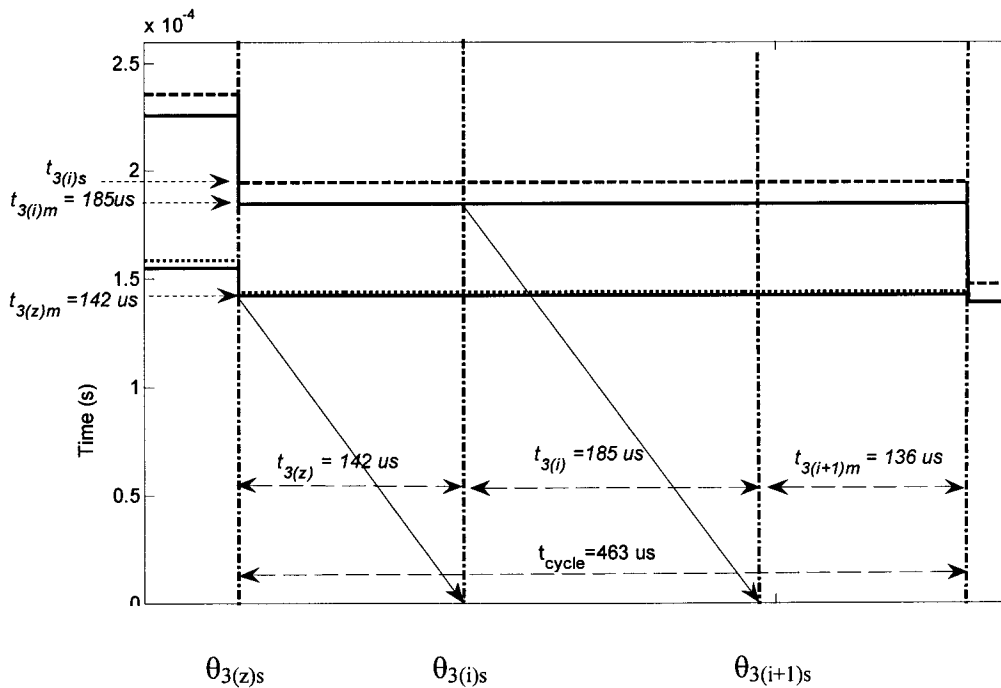


Fig. 3- 11 :- Graphical presentation for SQ2-EQ in the 3<sup>rd</sup> cycle of 6.

In Fig. 3- 11, the values of  $t_{3(z)m}=142\mu\text{s}$  and  $t_{3(i)m}=185\mu\text{s}$  in the third SVM cycle when  $m_a = 0.7$  are calculated in the beginning of SVM cycle. The same states ON times are in Fig. 2- 5 for SQ2-RM, but are calculated during SVM cycle, which giving no opportunity to change those states ON times if they are not yielding suitable  $HD_{5-7}$ , which is the case in this sequence of states.

### 3.3.2. CALCULATION OF STATES ON TIMES USING SQ2-CF

The last state of SQ2 is  $I_{i+1}$ . Its estimated and updated ON times can be calculated using the same approach described in SQ2-EQ for  $I_z$  and  $I_i$  as follows,

$$t_{c(i+1)s} = t_{\text{cycle}} \times m_a \times \sin[10^\circ \times (N_C - 1) + \omega \times t_{c(z)m} + \omega \times t_{c(i)m}] \quad (3- 22)$$

$$t_{c(i+1)m} = t_{\text{cycle}} \times m_a \times \sin \left[ 10^\circ \times (N_C - 1) + \omega \times t_{c(z)m} + \omega \times t_{c(i)m} + \frac{\omega \times t_{c(i+1)s}}{2} \right] \quad (3- 23)$$

The final ON times for states are calculated using  $K_c$  from (3- 13) in,

$$t_{c(z)f} = K_c \times t_{c(z)m} \quad (3- 24)$$

$$t_{c(i)f} = K_c \times t_{c(i)m} \quad (3- 25)$$

SIMULINK blocks achieving SQ2-CF technique are shown in Fig. 3- 12. In this sequence, the zero state comes first. From literature review, this sequence was rarely used and generates high  $HD_{5-7}$ , using zero state in the beginning of the SVM cycle generates  $HD_{5-7}$  [6], [33]. In the second part of this thesis using zero state in the beginning of the SVM sequence is mandatory, there it is recommended to use SQ2-CF where  $HD_{5-7}$  can be kept low.

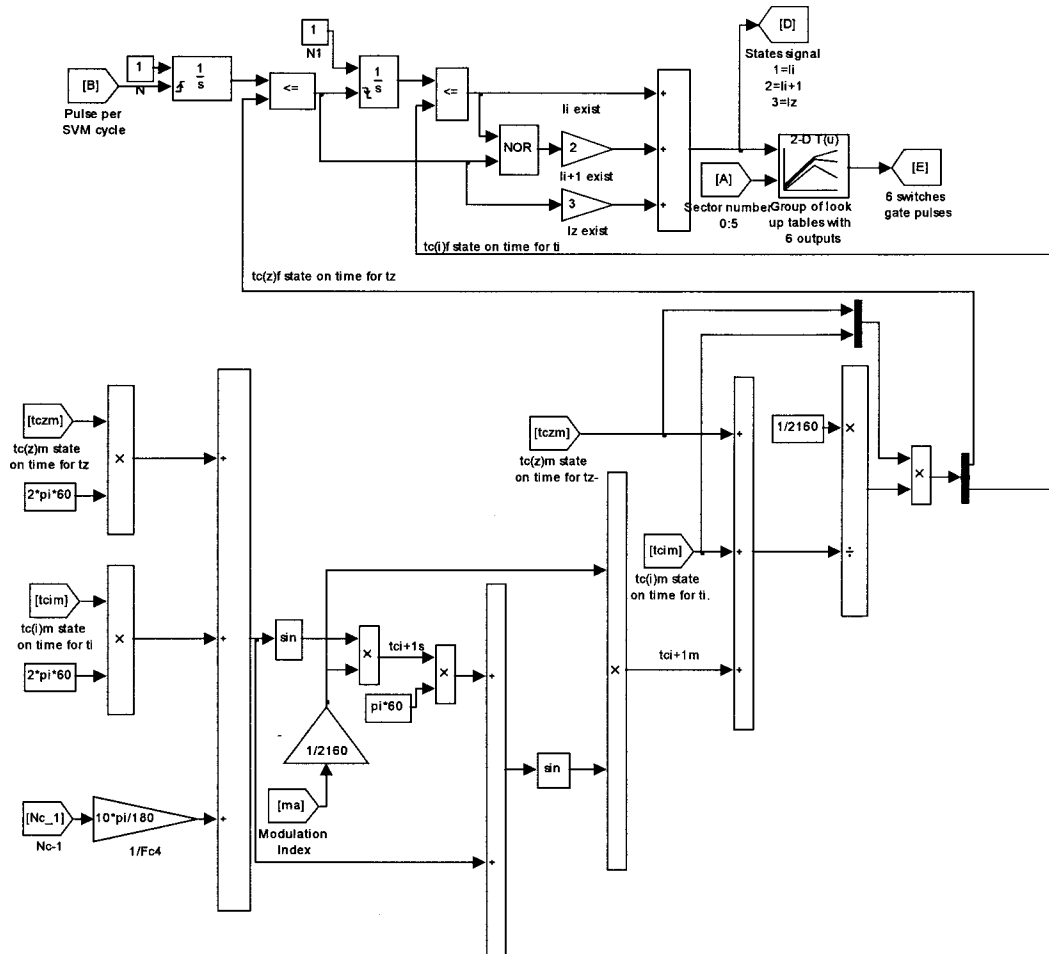


Fig. 3- 12 :- SIMULINK blocks used in calculate states ON times for SQ2-CF.

### 3.3.3. PERFORMANCE OF SQ2-EQ AND SQ2-CF

Fig. 3- 13 illustrates how the index  $HD_{5-7}$  of the CSC input current varies with the  $m_a$  for the four schemes, SQ2-SAs, SQ2-SAm, SQ1-EQ and SQ1-CF. There one sees that SQ2-SAs, SQ2-SAm and SQ1-EQ schemes present high  $HD_{5-7}$ . The best result is for SQ1-CF scheme which presents further reduction in  $HD_{5-7}$  for high values of  $m_a$ . Again, the SV rotates all the time and implementing SVM cycle with states ON times calculated at one instant in each SVM cycle generates  $HD_{5-7}$  in SQ2-SAs and SQ2-SAm. In SQ2-EQ the first two states  $I_z$  and  $I_i$  ON times are calculated, while  $I_{i+1}$  ON time is not. When

the instantaneous calculation of an active state  $I_{i+1}$  is not achieved then  $HD_{5-7}$  is high for the entire range of  $m_a$ . In SQ2-CF, the ON times for all states,  $t_z$ ,  $t_i$  and  $t_{i+1}$ , are corrected in the beginning of the SVM cycle, to achieve the instantaneous calculations  $I_{i+1}$  and  $HD_{5-7}$  is low in SQ2-CF.

Same claims of  $HD_{5-7}$  in SQ1-CF are applied to SQ2-CF with two differences. First, the active states in SQ2 comes after the zero state and calculated late in SVM cycle where  $t_{i+1}$  tends to increase and  $t_i$  tends to decrease. So, a negative difference indication between  $t_i$  and  $t_{i+1}$  summation appears. And,  $t_{3(i)f} \ll t_{4(i+1)f}$  as shown in Fig. 3- 14 when  $m_a = 0.5$ , which leads  $\sum_{c=1}^{c=6} t_{c(i)f} \ll \sum_{c=1}^{c=6} t_{c(i+1)f}$ . Similar difference between summation of  $t_i$  and  $t_{i+1}$  exists for one SVM sector in SQ1-CF and SQ2-CF with different sign. That does not affect  $HD_{5-7}$ .

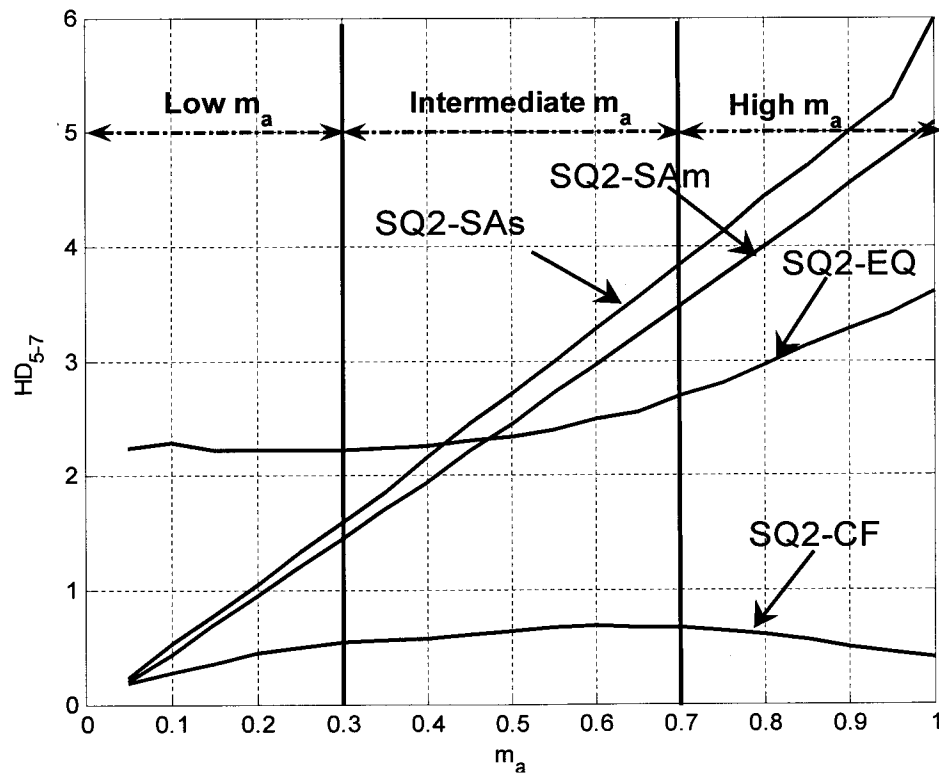


Fig. 3- 13 :- Index  $HD_{5-7}$  for SQ2-SAs, SQ2-SAm, SQ2-EQ and SQ2-CF.

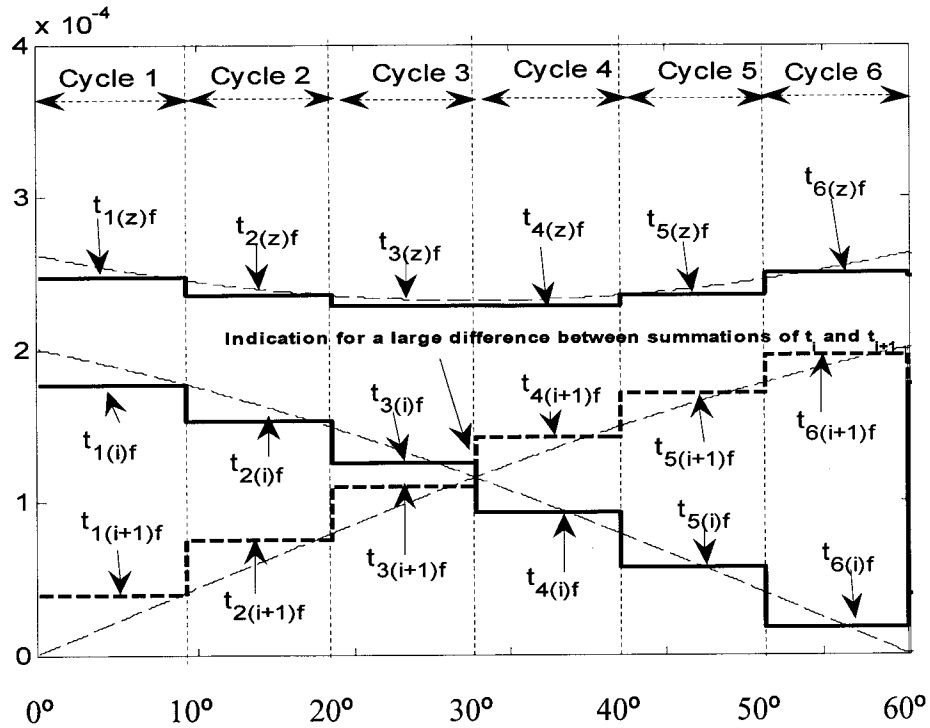


Fig. 3- 14 :- States ON times in one SVM sector cycles for SQ2-CF when  $m_a = 0.5$ .

Second difference is affecting  $H_{5-7}$ , and can be presented as following. When SVM is synthesized instantaneously with states ON times calculated at different times, the SVM cycle time is different than  $t_{cycle}$  which equal  $10^\circ$  electrical when  $N_{CS} = 6$ . That means that  $t_{cycle} \neq t_{c(i)m} + t_{c(i+1)m} + t_{c(z)m}$ . Recall that when CF procedure is used for calculating all states ON times, then  $t_{c(i)m}$ ,  $t_{c(i+1)m}$  and  $t_{c(z)m}$  are calculated in the middle of their  $I_{c(i)}$ ,  $I_{c(i+1)}$   $I_{c(z)}$  states ON times, respectively. Those are states ON time before correction. Resizing all states ON times with  $K_c$  is achieved only after all states ON times are calculated using (3- 13). The difference between the middle of states when EQ concept is used for calculating all states ON times and the middle of states after using CF states ON times is giving lack of accuracy in calculations. For earlier states in the sequence this difference is small. For states coming later in the sequence this difference

increased. And, states ON times come earlier are calculated more accurately than states ON times comes later in the sequence. When active states come later after the zero state in SQ2-CF around 0.05% increment in  $HD_{5-7}$  over SQ1-CF where active states come earlier is introduced. That is seen from SQ1-CF curve in Fig. 3- 6 and SQ2-CF curve in Fig. 3- 13. Also, from the  $H_{5-7}$  results for  $m_a = 0.7$  with SQ1-CF in Fig. 3- 7 (b),  $H_{5-7} = 0.63\%$ . And, results for  $m_a = 0.7$  with SQ2-CF in Fig. 3- 15,  $H_{5-7} = 0.67\%$ .

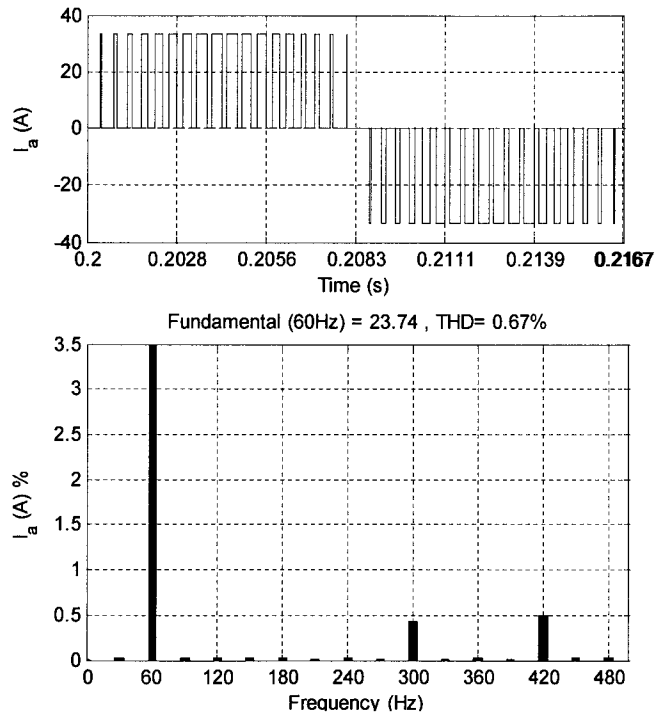


Fig. 3- 15 :- Index  $HD_{5-7}$  in the CSC ac-side current for SQ2-CF when  $m_a = 0.7$ .

### 3.4. SEQUENCE THREE

#### 3.4.1. CALCULATION OF STATES ON TIME USING SQ3-EQ

This sequence is presenting four segments, the first and the last are zero state, what results in only three states transitions per SVM cycle as in the previous sequences

with three segments. The ON time of the zero state is not divided equally between the two segments as in the conventional technique. The duration of the first segment is equal to half of the zero state ON time calculated using the estimate and update approach described for SQ2. The estimated ON time is calculated in (3- 26). Then, it is updated at the midpoint of this segment, resulting in (3- 27).

$$t_{c(z1)s} = \frac{t_{\text{cycle}}}{2} \times [1 - m_a \times \sin(60^\circ - 10^\circ \times (N_C - 1)) - m_a \times \sin(10^\circ \times (N_C - 1))] \quad (3- 26)$$

$$t_{c(z1)m} = \frac{t_{\text{cycle}}}{2} \times \left[ 1 - m_a \times \sin\left(60^\circ - 10^\circ \times (N_C - 1) - \frac{\omega \times t_{c(z1)s}}{2}\right) - m_a \times \sin\left(10^\circ \times (N_C - 1) + \frac{\omega \times t_{c(z1)s}}{2}\right) \right] \quad (3- 27)$$

The second state to be used in this sequence of states is  $I_i$ . Its estimated value is obtained at the end of the first segment of the cycle in (3- 28). The update ON time of state  $I_i$  is calculated in (3- 29). The same approach is used for calculating the estimated and updated ON times of  $I_{i+1}$  in (3- 30) and (3- 31). The second half of zero state occupies the remainder of the cycle.

$$t_{c(i)s} = t_{\text{cycle}} \times m_a \times \sin(60^\circ - 10^\circ \times (N_C - 1) - \omega \times t_{c(z1)m}) \quad (3- 28)$$

$$t_{c(i)m} = t_{\text{cycle}} \times m_a \times \sin\left(60^\circ - 10^\circ \times (N_C - 1) - \omega \times t_{c(z1)m} - \frac{\omega \times t_{c(i)s}}{2}\right) \quad (3- 29)$$

$$t_{c(i+1)s} = t_{\text{cycle}} \times m_a \times \sin[10^\circ \times (N_C - 1) + \omega \times t_{c(z1)m} + \omega \times t_{c(i)m}] \quad (3- 30)$$

$$t_{c(i+1)m} = t_{\text{cycle}} \times m_a \times \sin[10^\circ \times (N_C - 1) + \omega \times t_{c(z1)m} + \omega \times t_{c(i)m} + \frac{\omega \times t_{c(i+1)s}}{2}] \quad (3- 31)$$

SIMULINK blocks for SQ3-EQ are implemented in a similar way of Fig. 3- 2 and Fig. 3- 10, using equations (3- 26) to (3- 31) in sequence. States  $t_{z1}$ ,  $t_i$ ,  $t_{i+1}$  and  $t_{z2}$  ON times are introduced in Fig. 3- 16 when  $m_a = 0.7$ , that is the same values obtained when SQ3-RM is used in Fig. 2- 7.



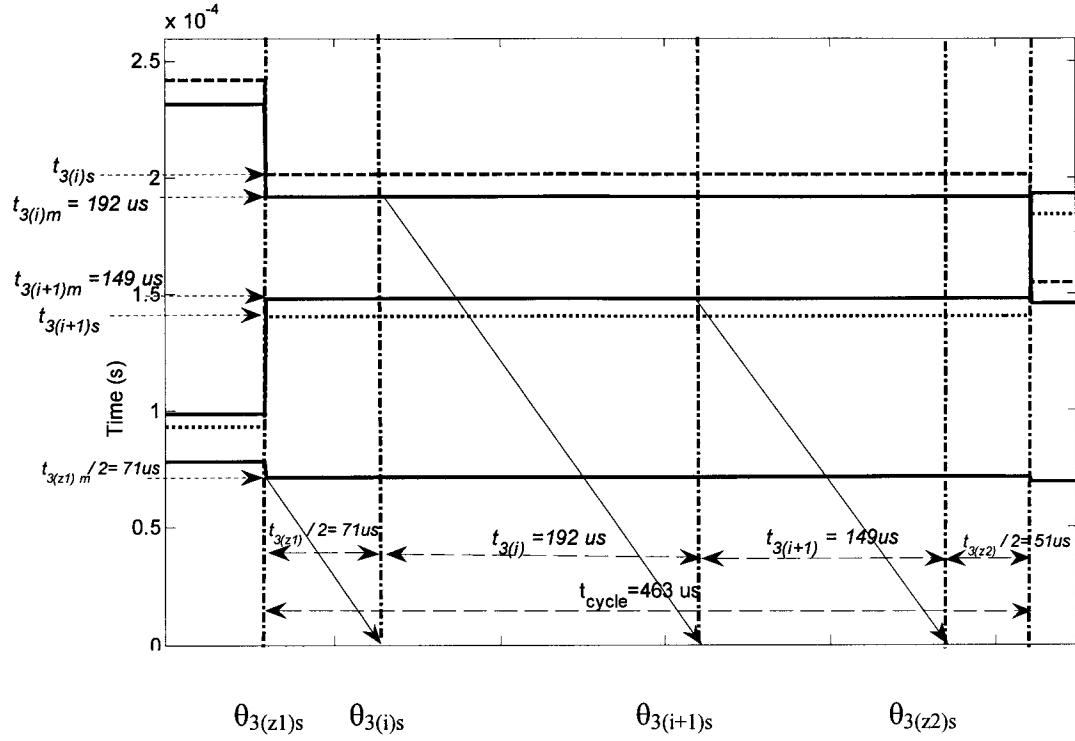


Fig. 3- 16 :- States ON times when SQ3-EQ is used and  $m_a = 0.7$ .

### 3.4.2. CALCULATION OF STATES ON TIMES USING SQ3-CF

The same approach presented in SQ1-CF and SQ2-CF is applied to find states ON times in SQ3-CF. The duration of the last segment is the half of the duration of  $I_z$ , and is called  $t_{z2}$ . The estimated and updated ON times for this segment can be calculated as,

$$t_{c(z2)s} = \frac{t_{\text{cycle}}}{2} \times [1 - m_a \times \sin(60 - \theta_{c(z2)s}) - m_a \times \sin(\theta_{c(z2)s})] \quad (3- 32)$$

$$\text{Where, } \theta_{c(z2)s} = 10^\circ \times (N_c - 1) + \omega \times t_{c(z1)m} + \omega \times t_{c(i)m} + \omega \times t_{c(i+1)m} \quad (3- 33)$$

$$t_{c(z2)m} = \frac{t_{\text{cycle}}}{2} \times [1 - m_a \times \sin(60 - \theta_{c(z2)m}) - m_a \times \sin(\theta_{c(z2)m})] \quad (3- 34)$$

$$\text{And, } \theta_{c(z2)m} = \theta_{c(z2)s} + \frac{\omega \times t_{c(z2)s}}{2} \quad (3- 35)$$

It should be noted that  $t_{C(z)m} = t_{C(z1)m} + t_{C(z2)m}$ . And that, the final ON times of the four segments can be obtained by multiplying the updated values with  $K_c$  from (3- 13) and the final ON times are,

$$t_{c(z1)f} = K_c \times t_{c(z1)m} \quad (3- 36)$$

$$t_{c(i)f} = K_c \times t_{c(i)m} \quad (3- 37)$$

$$t_{c(i+1)f} = K_c \times t_{c(i+1)m} \quad (3- 38)$$

The SIMULINK blocks for SQ3-CF are implemented with a procedure similar to Fig. 3- 4 and Fig. 3- 12 using equations (3- 32) to (3- 38) in sequence.

### 3.4.3. PERFORMANCE OF SQ3-EQ AND SQ3-CF

Fig. 3- 17 illustrates how the index  $HD_{5.7}$  varies with  $m_a$  for the four schemes, SQ3-SAs, SQ3-SAm, SQ3-EQ and SQ3-CF. There SQ3-SAs and SQ2-SAm present high  $HD_{5.7}$ . Perfect  $HD_{5.7}$  results are obtained with SQ3-EQ and SQ3-CF, the improvement offered by the SQ3-EQ and SQ3-CF schemes is substantial for this specific sequence. SQ3-CF still presents an improvement over SQ3-EQ. Also, in high  $m_a$  over modulation effect obstacle presented by SQ3-EQ does not exist anymore in SQ3-CF. The best result overall is accomplished with SQ3-CF with a maximum  $HD_{5.7} = 0.44\%$  for  $m_a = 1$ .

$K_c$  variations in SQ3-CF for  $m_a = 0.5$  and  $m_a = 0.8$  are illustrated in Fig. 3- 18. Unlike SQ1-CF and SQ2-CF, here  $K_c$  does not vary from one SVM cycle to the other inside the same SVM sector, when  $m_a = 0.5$   $K_c \approx 0.981$  and when  $m_a = 0.8$   $K_c \approx 0.952$ . That leads to a balance states ON times error for uncorrected scheme SQ3-EQ. In SQ3 small  $K_c$  variation between SVM cycles and high  $K_c$  value in general for all SVM cycles reduce  $HD_{5.7}$  for SQ3-EQ in Fig. 3- 17.

Since  $K_c$  is nearly fixed inside the SVM sector in SQ3-CF, it varies only with  $m_a$ .  $K_c$  can be achieved by a procedure suitable for on-line operation with look up tables.  $t_{(z)l}$ ,  $t_{(i)l}$  and  $t_{(i+1)l}$  can be multiplied with a value varying with  $m_a$  in a look up table to calculate  $t_{(z)f}$ ,  $t_{(i)f}$  and  $t_{(i+1)f}$ , there  $K_c = 0.981$  when  $m_a = 0.5$  and  $K_c = 0.952$  when  $m_a = 0.8$ . By this procedure, the computation effort in SQ3-CF is similar to SQ3-EQ.

The difference between summations of states  $t_i$  and  $t_{i+1}$  ON times in each SVM sector is almost zero in SQ3-CF independent on the value of  $m_a$ . Fig. 3- 19 illustrates the symmetry assessment for SQ3-CF when  $m_a = 0.5$ , there  $t_{3(i)f} = t_{4(i+1)f}$  and  $\sum_{c=1}^{c=6} t_{c(i)f} = \sum_{c=1}^{c=6} t_{c(i+1)f}$  that lead SQ3-CF to ideally present no  $HD_{5-7}$ ,  $HD_{5-7} = 0.44\%$  when  $m_a = 1$  and less for others in Fig. 3- 17. Also, in SQ3-EQ, large and nearly fixed  $K_c$  and symmetry assessment between active states are keeping  $HD_{5-7}$  low for  $m_a < 0.9$ .

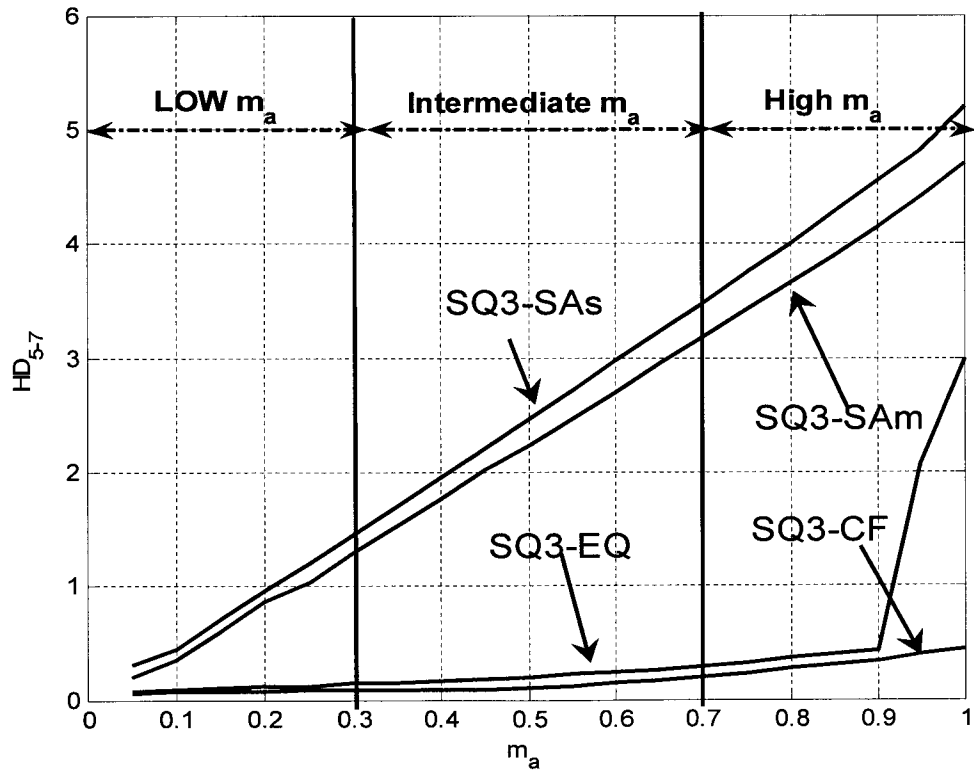


Fig. 3- 17 :- Index  $HD_{5-7}$  calculated for SQ3 using the SAs, SAm, EQ and CF.

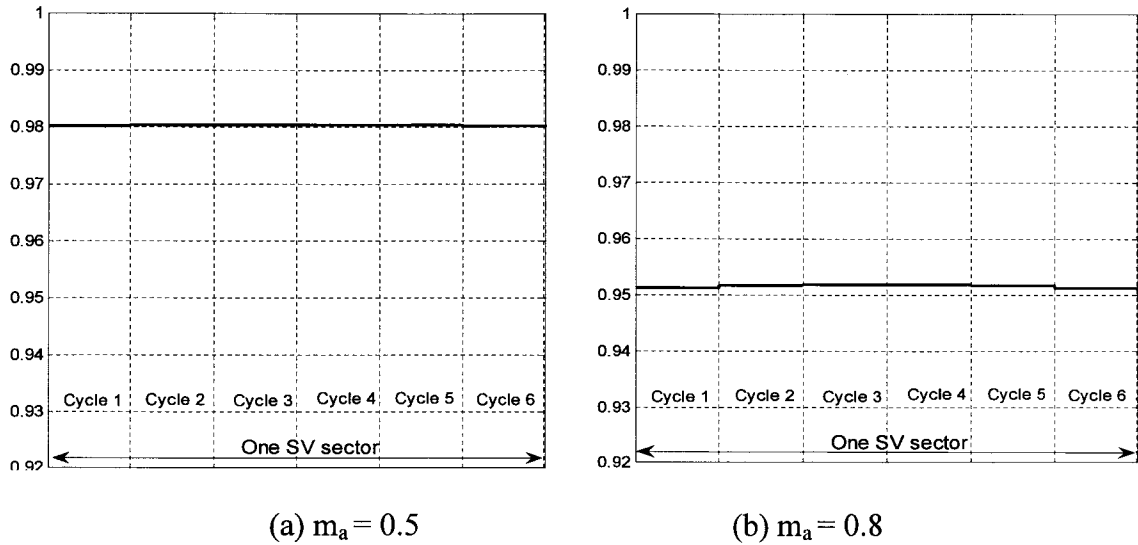


Fig. 3- 18 :-  $K_c$  values in one SVM sector cycles for SQ3-CF.

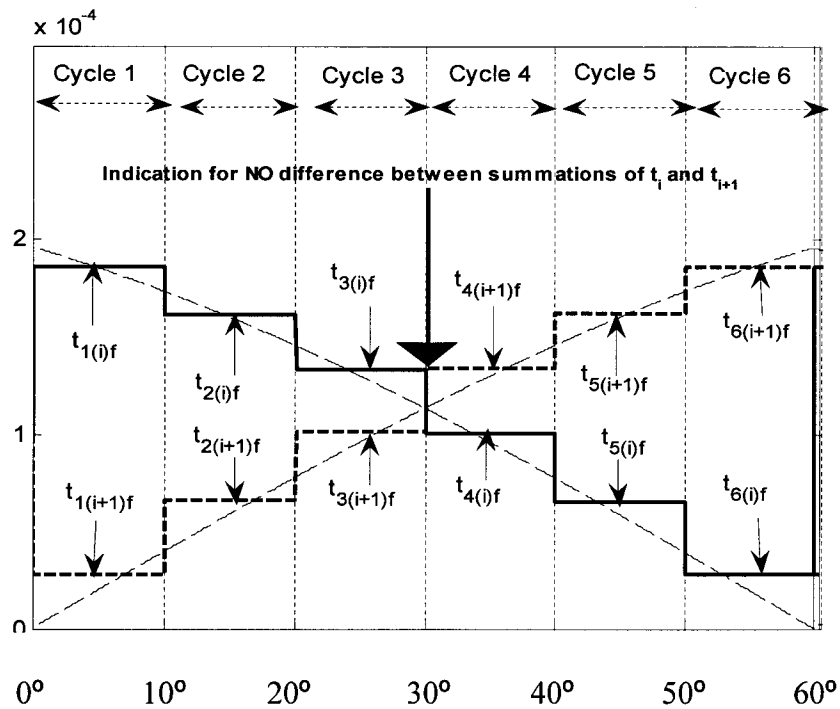


Fig. 3- 19 :- Symmetry assessment in SQ3-CF when  $m_a=0.5$ .

The reason for the remainder  $HD_{5-7} < 0.44\%$  in SQ3-CF is described as follows. Since,  $f_{cycle} \approx 2k$  Hz a small  $HD_{5-7}$  resulted from the sequence of calculation process, correction is achieved after all states ON times are calculated without correction. If each

state ON time is corrected after calculated then its uncorrected value will not affect the following states ON times and  $HD_{5-7} \approx 0\%$ , which was not achieved. Fig. 3- 20 illustrates how low  $HD_{5-7}$  can be when SQ3-CF is used and  $m_a = 0.7$ .

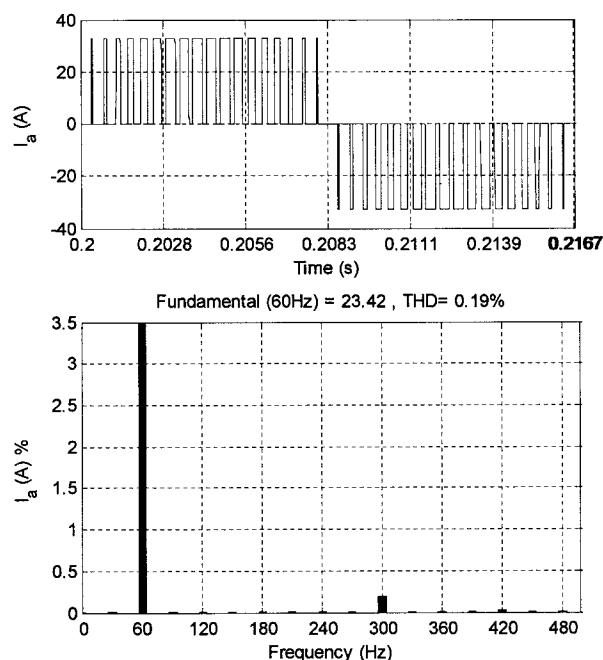


Fig. 3- 20 :- Index  $HD_{5-7}$  in the CSC ac-side current for SQ3-CF when  $m_a = 0.7$ .

### 3.5. EXPERIMENTAL RESULTS

In this chapter the simulation results are obtained with a step time of  $0.5\mu s$ . Also, the snubber circuits and overlap period effects are neglected. Comparing  $HD_{5-7}$  in a real CSC and simulated one will not be effective in this step. Instead, experimental verification is carried out to validate the simulation results presented and to identify any constraints imposed by the proposed techniques for practical hardware implementation.

An experimental set-up based on a digital signal processor (DSP) development kit from dSPACE (DS1103), that operates with a sampling frequency of 18k Hz was built. The SIMULINK files used for the simulations were converted to DSP code by Real Time

Interface (RTI) and downloaded to the DSP. It was found that the minimum step-size (sampling time) that could be successfully used independent on states ON times calculation method, without task over run, was  $25\mu\text{s}$ . The extra steps used by the proposed methods did not add a significant computational burden to the DSP, what could affect the accuracy of the calculated on times more than for the standard methods. On the other hand, if the switching pattern is changed every  $25\mu\text{s}$  that is not fast enough to verify the advantages of the proposed techniques for a CSC operating at a 60 Hz grid. That causes  $\text{HD}_{5-7}$  to be higher than those in simulation for all combinations of sequence of states and ON times calculation schemes.

Thus, the performance verification at the experimental level was carried out for a CSC connected to a fictitious 6Hz ac-side grid. The gating signals of a CSC legs, obtained from the dSPACE interface box, were used to build the ac-side current of one CSC phase. If the top (bottom) switch is on, the ac side current flowing towards the CSC is positive (negative). If they are either on or off, the ac side current in that phase is zero. Assuming that the dc-side current presents low harmonic distortion, this can give a good indication of the ac side current waveform and harmonic spectrum.

Fig. 3- 21 shows the ac-side current waveform and harmonic spectrum when SQ1-SAs is used with  $m_a = 0.7$ . The magnitude of the fundamental component in the harmonic spectrum is 100%. The  $\text{HD}_{5-7}$  is equal 3.65%, very close to that shown in Fig. 2- 9 (a) for SQ1-SAs. Fig. 3- 22 shows the same waveforms but using SQ1-CF. The resulting value for  $\text{HD}_{5-7}$  is equal 0.795 %. Again, it is very close to the value shown in Fig. 3- 7 (b) for SQ1-CF.

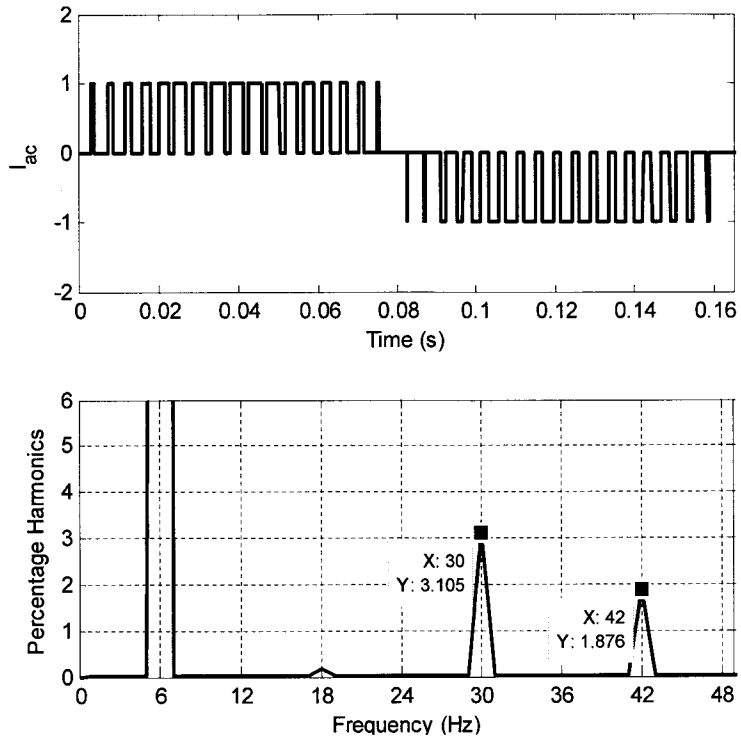


Fig. 3- 21 :- Ac-side CSC current when SQ1-SAs is used with  $m_a = 0.7$  and  $f_{grid} = 6$  Hz.

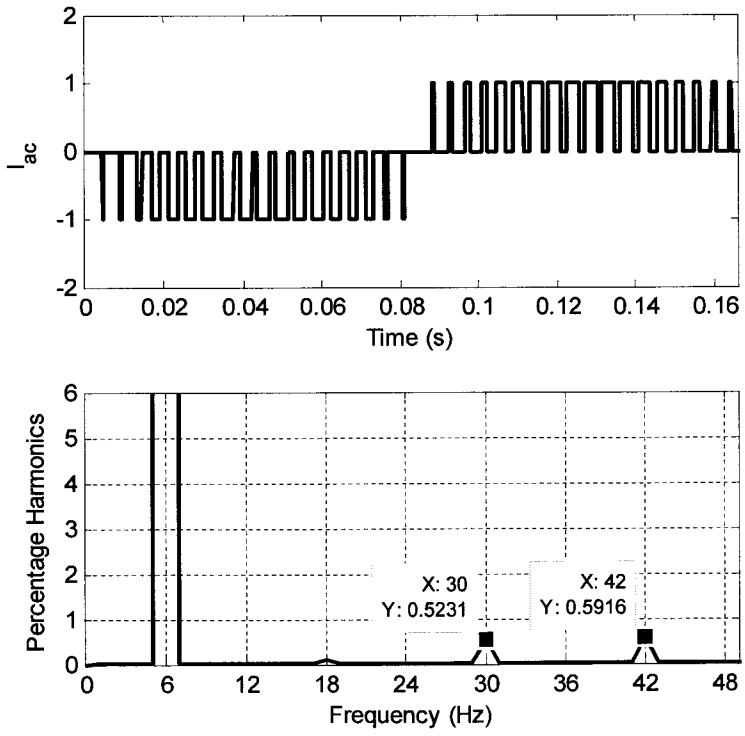


Fig. 3- 22 :- Ac-side CSC current when SQ1- CF is used with  $m_a = 0.7$  and  $f_{grid} = 6$  Hz.

### 3.6. CONCLUSION

The non-characteristic LOH, especially  $HD_{5-7}$ , which appears in LSF-SVM-CSC, has been reduced by a new procedure in this chapter. New equations for the states ON times calculations have been proposed, that is called EQ. Those equations vary with the states sequence to achieve instantaneous calculations for states. An instantaneous calculation means that each state ON time is calculated according to the value of its ON time in the middle of the existing period. Simulation results have shown that this approach results in a reduced LOH. If the calculated ON times are further adjusted to fit in the SVM cycle, the harmonic distortion is significantly reduced compared to previous ON times calculation methods. A states sequence that results in a maximum  $HD_{5-7}$  of 0.44% when used with the proposed scheme has been identified. Also, a procedure suitable for on-line operation with look up tables is proposed. The superior performance of the proposed techniques was also demonstrated with an experimental set-up based on a commercial DSP development kit. A 6 Hz grid was used in this case, because the relatively high minimum sampling time allowed by the dSPACE (DS-1103) system (25 $\mu$ s), significantly increased the harmonic distortion of all SVM schemes making a comparison to the simulated results, carried on with a time step of a few  $\mu$ s, unreasonable.



## CHAPTER 4

# 4. MINIMIZING LOH IN LSF-SVM-CSC WITH MHT TECHNIQUE

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### 4.1. INTRODUCTION

Large reduction in  $HD_{5-7}$  at the CSC ac-side current is achieved by new techniques of calculating states ON times in this chapter. From chapter two, one can conclude that SQ3-RM concept is presenting a good  $HD_{5-7}$  result. This chapter is started by an investigation in SQ3-RM. Then a technique calculating all states ON times when the state changing from one active state to the other in SQ3 is introduced, which are called RT. Both techniques are effective in reducing  $HD_{5-7}$  to a certain limit when overlap period and input ac-side filter design are not taken into consideration. The ac-side filter design basic concepts were presented in [53].

Then, Minimum Harmonics Tracking (MHT) technique for calculating states ON times in LSF-SVM-CSC is proposed. The Tracking technique adjusts states ON times once per four ac-side line current cycles to give the least  $HD_{5-7}$  with feedback concept. MHT is suitable for CSCs with ac side filters that amplify 5<sup>th</sup> or 7<sup>th</sup> harmonics or both with different values.

The ac-side current position during overlap period was investigated in [54]. In the CSC with large overlap period, the power factor (PF) affects  $HD_{5-7}$ . One variable MHT can be used in this case with acceptable  $HD_{5-7}$ . Two variables MHT technique for active

states ON times inside SVM cycle is proposed to give the least possible  $HD_{5-7}$ . Finally, experimental investigation with 6-switches SVM-CSC is introduced. In this chapter major issues of MHT are presented. More details and different operating conditions for the concepts proposed in this chapter can be found in [55].

## 4.2. DIRECT STATES ON TIMES CALCULATIONS WITH LOH

### 4.2.1. MIDDLE STATES ON TIMES CALCULATIONS

One can conclude from chapter two that SQ3-RM reduces  $HD_{5-7}$  to one of the lowest values presented thus far. Improvement over SQ3-RM has the potential for virtually eliminating  $HD_{5-7}$ . Since only SQ3 is used in this chapter, RM will be written instead of SQ3-RM. Although RM technique calculates each state ON time at a certain instant which is different than the other states, but a complete sector view presented in chapter three proves that, the symmetry between both active states ON times inside each SVM sector with respect to its midpoint was a main issue. In other words, RM techniques average time of the first active state  $I_i$  ( $t_i$ ) and average time of the second average state  $I_{i+1}$  ( $t_{i+1}$ ) are equal inside every single SVM sector which satisfy (4- 1).

$$\sum_{N_C=1}^{N_{CS}} t_i(N_C) = \sum_{N_C=1}^{N_{CS}} t_{i+1}(N_C) \quad (4- 1)$$

Such that,  $t_i(N_C)$  and  $t_{i+1}(N_C)$  are states  $I_i$  and  $I_{i+1}$  ON times in cycle  $N_C$ . RM have instantaneous calculations for active states, as shown in Fig. 4- 1 when  $m_a = 0.7$ . But states ON times are not calculated at the same instant inside SVM cycle and (4- 2) is correct if RM concept is used to calculate all states ON times.

$$t_{\text{cycle}} \neq t_{C(z1)m} + t_{C(i)m} + t_{C(i+1)m} + t_{C(z2)m} \quad (4- 2)$$

Where  $t_{C(y)m}$  is the state  $I_y$  ON time for SVM cycle  $C$ , calculated in the middle of state.

To avoid inequality in (4- 2), the same calculation process cannot be used for the last state ON time ( $t_{z2}$ ) calculation. And, a relatively small magnitude of  $HD_{5-7}$  resulted from that  $t_{z1} \neq t_{z2}$  as shown in Fig. 4- 1. On the other hand, SAM technique calculates states ON times at the same instant in the middle of SVM cycles, which give unsuitable ON times for all states and high magnitude of  $HD_{5-7}$ .

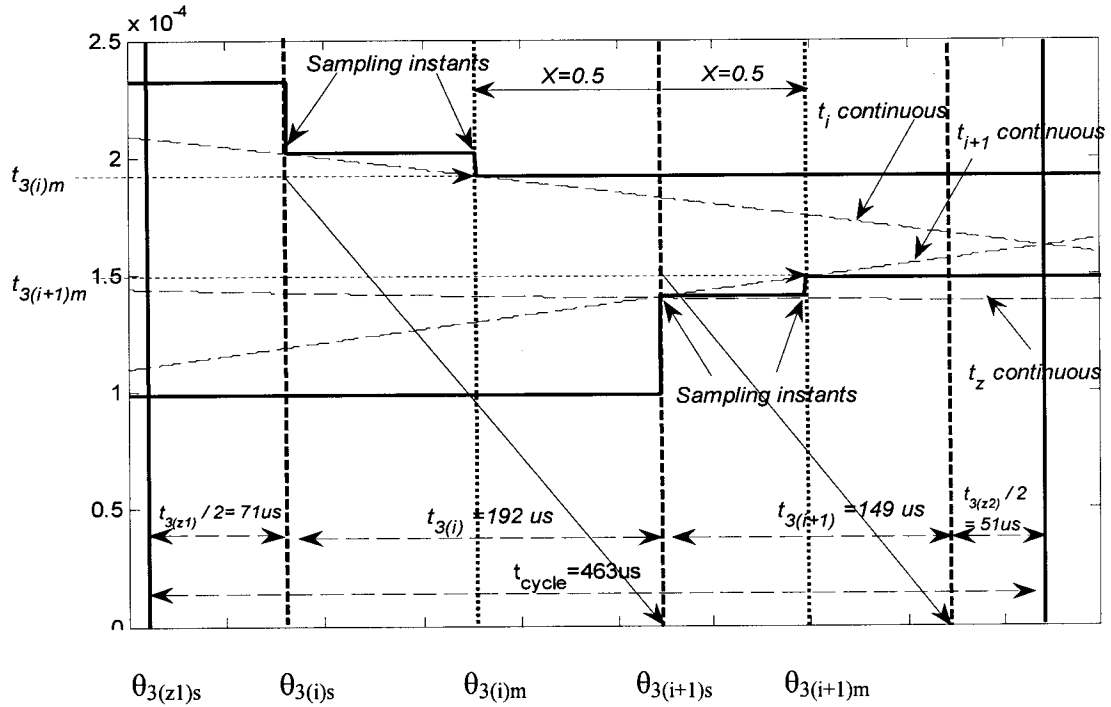


Fig. 4- 1 :- RM technique states ON time calculations in the 3<sup>rd</sup> SVM cycle,  $m_a = 0.7$ .

#### 4.2.2. STATES ON TIMES CALCULATIONS DURING TRANSITION POINT

Calculating active states ON times at the same instant makes  $t_{z1} \approx t_{z2}$ . This technique is called Record Transition (RT), both active states ON times are calculated at active states transition point  $\theta_{(i+1)s}$ , the point where the ON state is changed from  $I_i$  to  $I_{i+1}$  in SQ3. In RT, ON times calculation instant is the same for active states inside each SVM cycle. And, it is varying from one SVM cycle to the other inside the same SVM sector.

Fig. 4- 2 presents the concept behind RT technique in the 3<sup>rd</sup> SVM cycle of 6 SVM cycles when  $m_a = 0.7$ . There, dashed curves are representing  $t_i$ ,  $t_{i+1}$  and  $t_z$  from (1- 4), (1- 5) and (1- 6), respectively. Active states ON times are calculated at the same instant, when the ON state is changed from  $I_i$  to  $I_{i+1}$ , that is  $\theta_{(i+1)s}$  point, at this instant  $t_i = 181.5\mu s$ ,  $t_{i+1} = 140.5\mu s$ . That give  $(t_{z1} = 71\mu s) \approx (t_{z2} = 70\mu s)$ .

RT satisfies the symmetry condition presented in (4- 1). Besides, active states ON times are calculated at the same instant. Also, the point at which active states are calculated leads to partially instantaneous calculations for SV. Instantaneous calculations is achieved only with RM, where  $t_i$  is calculated at  $\theta_{(i)m}$  and  $t_{i+1}$  is calculated at  $\theta_{(i+1)m}$ . RT active states ON times are calculated at  $\theta_{(i+1)s}$  between  $\theta_{(i)m}$  and  $\theta_{(i+1)m}$  where  $t_i$  and  $t_{i+1}$ , respectively, are calculated for RM with instantaneous calculations for SV, that can be called partial instantaneous calculations for SV.

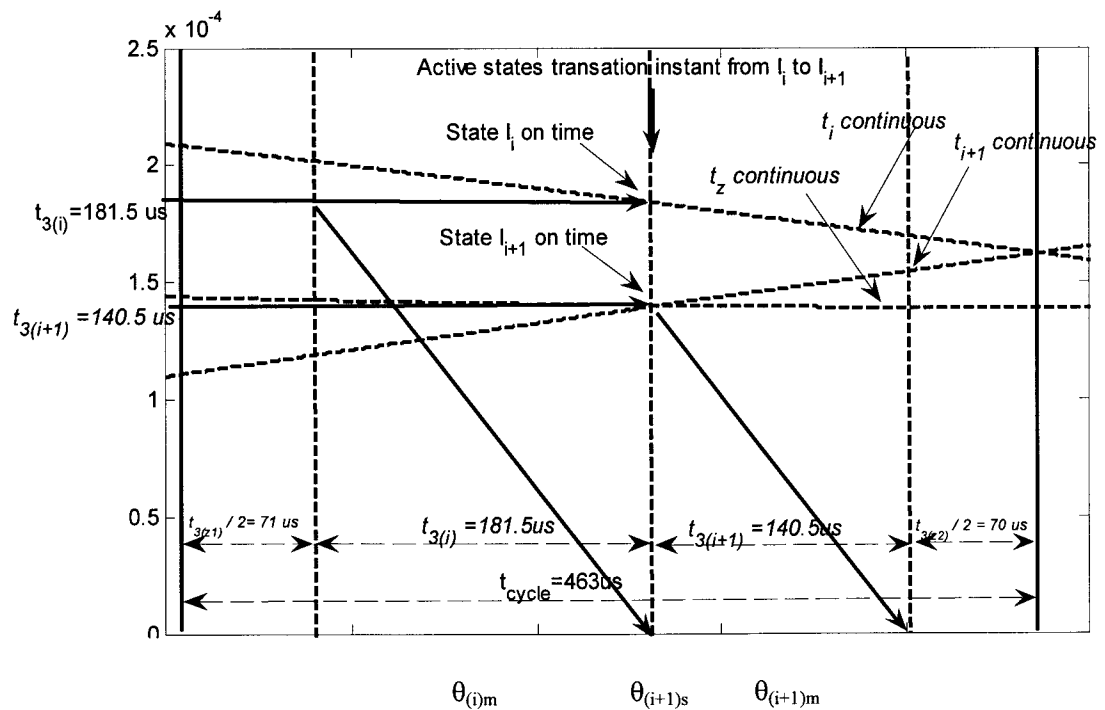


Fig. 4- 2 :- RT for one SVM cycle, 3<sup>rd</sup> cycle of 6 cycles when  $m_a = 0.7$ .

### 4.2.3. PERFORMANCE COMPARISON BETWEEN DIRECT TECHNIQUES

A performance comparison between four states ON times calculation techniques with SQ3, i.e. SAs, SAm, RM and RT, is introduced in Fig. 4- 3. In those techniques, all states ON times calculating instants inside SVM cycles have a predefined procedure. Therefore, they can be called direct techniques. Operating conditions for  $0.1 < m_a < 0.9$  will be taken into consideration. For  $m_a < 0.1$  some inaccurate measurements of  $HD_{5-7}$  are found and for  $m_a > 0.9$  over modulation issue appears in RM, what complicates the procedure to get the least  $HD_{5-7}$ . In general, RM and RT states ON times calculations have low  $HD_{5-7}$  compared to sampling techniques.

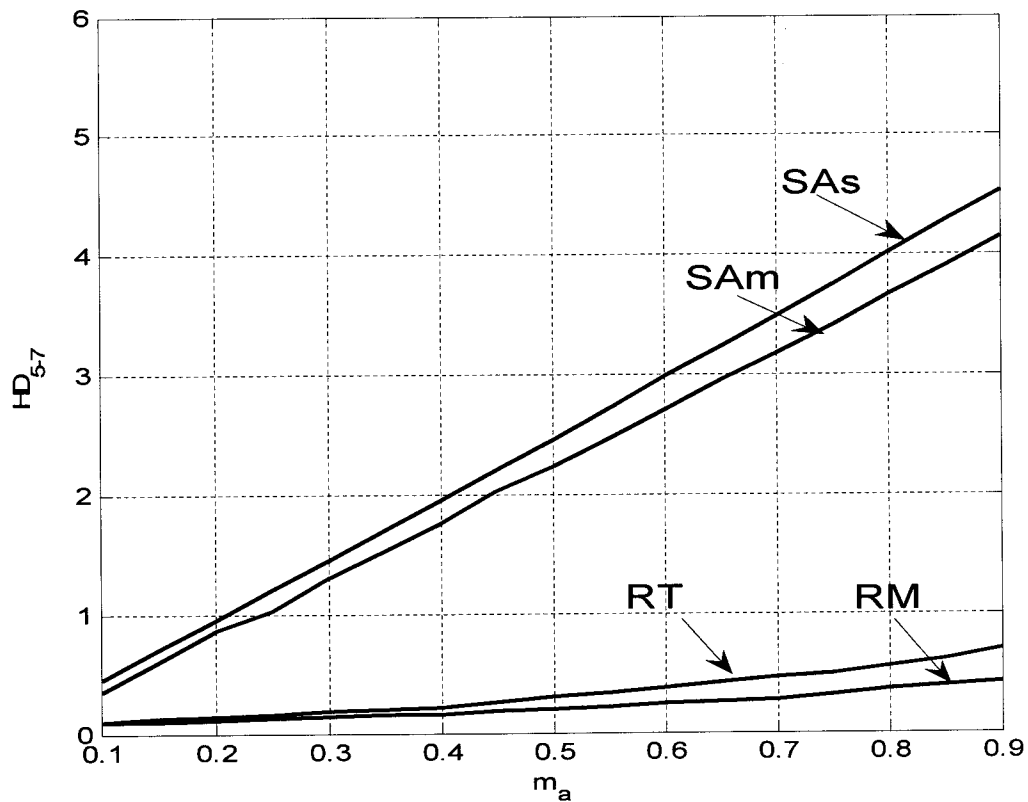


Fig. 4- 3 :- Index  $HD_{5-7}$  for direct techniques of SQ3, i.e. SAs, SAm, RM and RT.

### 4.3. ONE VARIABLE MHT TECHNIQUE

#### 4.3.1. TRACKING TECHNIQUE CONCEPT

From the previous section, one can arrive to the following conclusion. The least  $HD_{5-7}$  can be reached if all states ON times are calculated at the same instant, symmetry between  $t_i$  and  $t_{i+1}$  is achieved with (4- 1) and the SV is calculated instantaneously. RM technique gives low  $HD_{5-7}$  because SV was calculated instantaneously and (4- 1) was satisfied, but least  $HD_{5-7}$  was not reached yet because states ON times were not calculated at the same instant. On the other hand, RT technique also gives low  $HD_{5-7}$  because states ON times were calculated at the same instant and (4- 1) was satisfied, but least  $HD_{5-7}$  did not reach yet because SV was partially calculated instantaneously.

Instants where active states ON times are calculated inside SVM cycle to give the least  $HD_{5-7}$  should be near each other as possible and **almost** presents SV instantaneously while (4- 1) is satisfied. A variable X which can be adjusted to reach the least  $HD_{5-7}$  is presented. X is the distance between active states transition point in SQ3 at  $\theta_{(i+1)s}$  and each active state ON time calculating instant as a percentage of this active state ON time. In (4- 3) X is presented as a function of four times periods A, B, C and D, they are introduced in Fig. 4- 4 when  $m_a = 0.7$  and  $X = 0.3$ , there  $t_i = 188\mu\text{sec}$ ,  $t_{i+1} = 145\mu\text{s}$ ,  $t_{z1} = 71\mu\text{s}$  and  $t_{z2} = 59\mu\text{s}$ .

$$X = \frac{A}{B} = \frac{C}{D} \quad (4- 3)$$

If RM is described with the variable X. then  $X = 0.5$ . While for RT  $X = 0$ . That means,  $HD_{5-7}$  for the case when  $X = 0$  (RT) and for the case when  $X = 0.5$  (RM) are shown in Fig. 4- 3. One value of  $0 < X < 0.5$  for each  $m_a$  may result in less  $HD_{5-7}$ . That

was confirmed by measuring  $HD_{5-7}$  for different values of  $X$ . The target is selecting  $X$  which leads to the least possible value of  $HD_{5-7}$ .

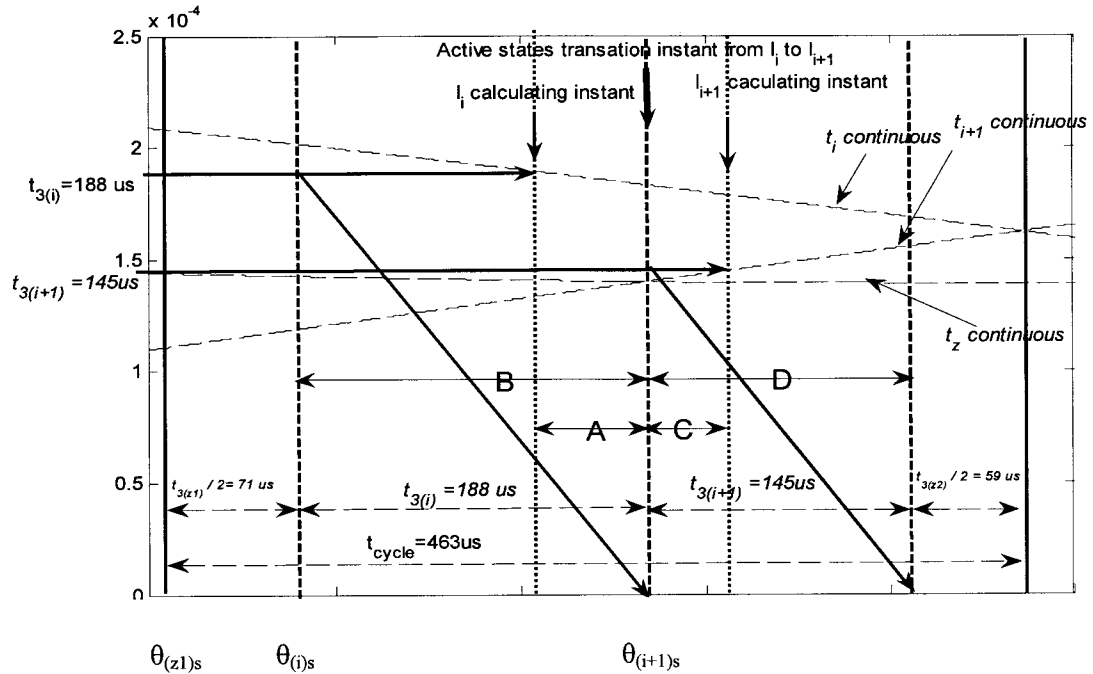


Fig. 4- 4 :- Variable  $X$  definition using  $A$ ,  $B$ ,  $C$  and  $D$  in the 3<sup>rd</sup> SVM cycle when  $m_a = 0.7$  and  $X = 0.3$ .

Fig. 4- 5 describes SIMULINK blocks measuring  $HD_{5-7}$  on-line during operation. After states ON times changes, four ac-side current line cycles are required to measure the correct values of fundamental (1<sup>st</sup>), 5<sup>th</sup> and 7<sup>th</sup> current harmonics by discrete Fourier blocks. Those current harmonics are used to measure  $HD_{5-7}$  with (2- 1).

Fig. 4- 6 presents a typical relation between  $HD_{5-7}$  and  $X$ , when  $X$  was changed manually in a simulation program started from  $X = 0$  and increasing towards  $X = 0.5$ .  $HD_{5-7}$  was reduced until a certain value of  $X$  where  $HD_{5-7}$  started to increase again. There is one value of  $X$  has the least  $HD_{5-7}$  for each operating condition. When  $X$  is gone far from this value, either increased or decreased,  $HD_{5-7}$  is increased.

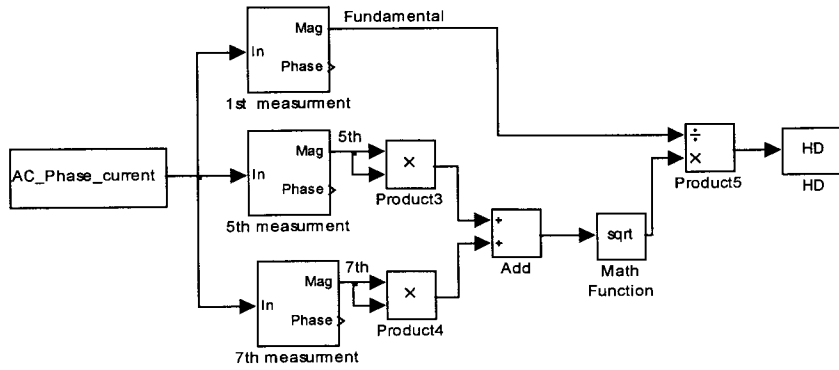


Fig. 4- 5 :- SIMULINK model used to measure  $HD_{5-7}$ .

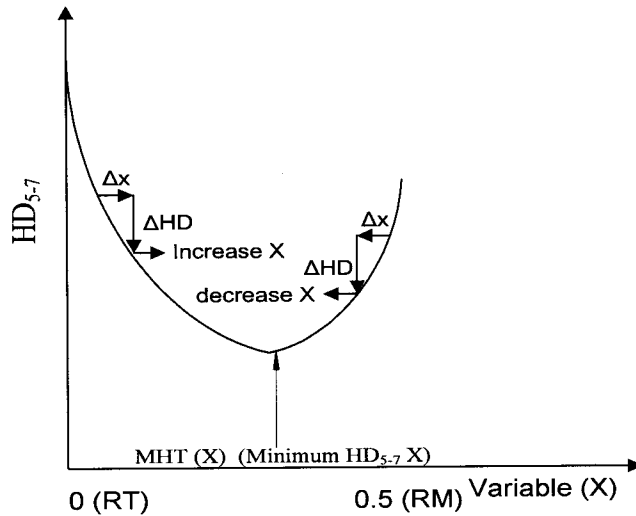


Fig. 4- 6 :- Minimum Harmonics Tracking (MHT) concept.

For simplification, MHT will be used instead of (single variable MHT). MHT technique measures the value of  $HD_{5-7}$  using Fig. 4- 5 blocks and (2- 1). Then, it tries to search for the value of  $X$  with the least  $HD_{5-7}$ . MHT technique perturbs  $X$  (increasing or decreasing by a small value) and measures  $HD_{5-7}$  resulting from the new  $X$  after four ac-side line current cycles. Then MHT either increase or decrease  $X$  to reach the least  $HD_{5-7}$ . MHT concept is described in Fig. 4- 6. There if  $HD_{5-7}$  is decreased when  $X$  is decreased MHT technique continues decreasing  $X$ . If  $HD_{5-7}$  is decreased when  $X$  is increased MHT technique continues increasing  $X$ . In this way, one can reach the least  $HD_{5-7}$ .



MHT logic with SIMULINK is presented in Fig. 4- 7. In MHT model, HD (K), HD (K-1), X (K), and X (K-1) are triggered blocks of sample and hold. When the edge of the pulse generator appears, what happened every four ac-side current line cycles, the present HD (k) subtracts the previous HD (k-1) and the result passes through a sign unit. Similar blocks are applied for the X channel. The results of the two channels are multiplied to determine the perturbation direction. If HD and X increase or decrease simultaneously the product is 1, which means that X should decrease by one step, that can be obtained by multiplying the perturbation step size with the perturbation direction. If they change in opposite way X should increase by one step. Selected perturbation step for X is 0.02, this value can be reduced on the expense of the time required to reach the best value of X.

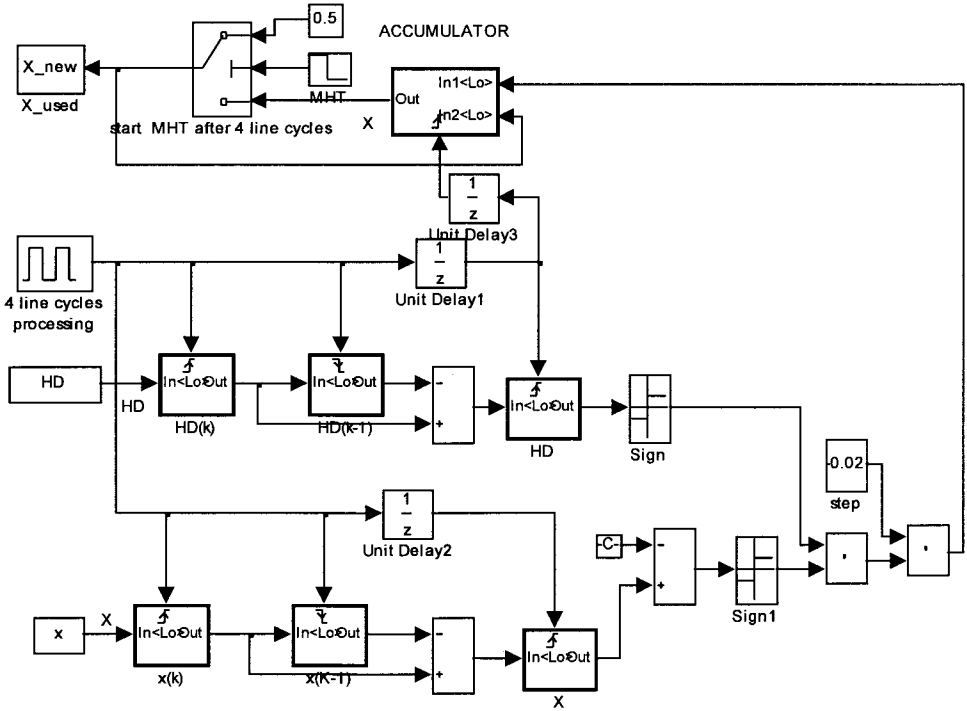


Fig. 4- 7 :- SIMULINK model for MHT technique.

Since RM gives better result than RT in Fig. 4- 3, it is preferable to start MHT with  $X = 0.5$ , that is the  $X$  for RM.  $X_{new}$  is used as a new  $X$  input. And, HD is measured using Fig. 4- 5. Both become ready to change  $X$  after four ac-side line cycles. Fig. 4- 8 illustrates how  $X$  is used to decide states ON times in one and two variables MHT technique. In one variable MHT, proposed in this section,  $X_1 = X_2$  while in two variables MHT, will be presented later on in this chapter, they are different.

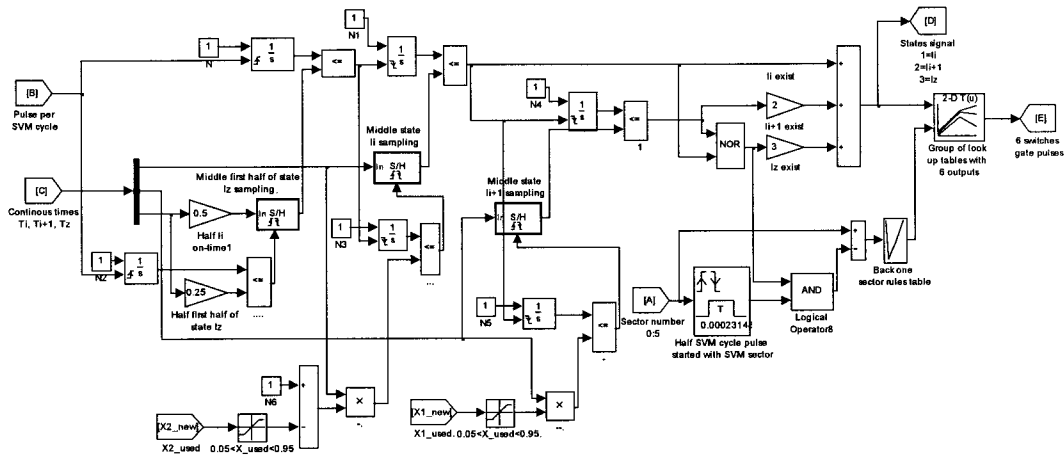


Fig. 4- 8 :- SIMULINK model used to calculate states ON times using  $X_1$  and  $X_2$ .

### 4.3.2. ONE VARIABLE MHT FOR CSC AC-SIDE CURRENT

MHT in this subsection is reducing the CSC ac-side current  $HD_{5-7}$ , not include ac-side filter. Fig. 4- 9 presents a performance of RM, RT and MHT techniques. MHT presents the best performance, MHT results were recorded at different  $X$  for each  $m_a$ . Perturbation of  $X$  does not affect operation during transient because states ON times are slightly changed while states position and sequences are fixed. The accuracy permitted by  $HD_{5-7}$  measurement is 0.01%. In Fig. 4- 10,  $m_a = 0.7$  for 1.5s, then  $m_a = 0.5$  for the following 1s. The value of  $X$  is in the upper window,  $HD_{5-7}$  is in the middle window and both of  $HD_5$  and  $HD_7$  from (4- 4) are in the lower window.

$$HD_5 = \frac{I_{(5^{th})}}{I_{(1^{st})}} 100 \% , \quad HD_7 = \frac{I_{(7^{th})}}{I_{(1^{st})}} 100 \% \quad (4-4)$$

In Fig. 4- 10,  $X = 0.5$  is selected in starting, when  $m_a = 0.7$  that resulting in  $HD_{5-7} = 0.28\%$ . This case can be seen from RM curve in Fig. 4- 9 when  $m_a = 0.7$ . MHT perturbing  $X$  to decrease  $HD_{5-7}$  gradually, which is achieved by decreasing  $X$  until  $X = 0.32$  and  $HD_{5-7} = 0.15\%$ , which can be seen from MHT curve in Fig. 4- 9. If  $X$  is decreased beyond  $0.32$  then  $HD_{5-7}$  increases again. MHT selects  $X = 0.32$  when  $m_a = 0.7$ , what takes around  $0.6s$ . In Fig. 4- 10, after  $1.5s$  from starting  $m_a = 0.5$ . MHT technique selects  $X = 0.3$  with  $HD_{5-7} = 0.1\%$  as least  $HD_{5-7}$  when  $m_a = 0.5$ , which can be seen from MHT curve in Fig. 4- 9 when  $m_a = 0.5$ . Fig. 4- 11 illustrates the importance of deciding the best states ON times when  $m_a = 0.7$ , MHT reduces  $HD_{5-7}$  to  $0.15\%$  from  $3.44\%$  in Fig. 2- 13 (a) for SQ3-SAs, that is  $96\%$  reduction. If MHT is compared with SQ3-RM in Fig. 2- 13 (c) with  $HD_{5-7} = 0.28\%$  it presents  $46\%$  reduction in  $HD_{5-7}$  when  $m_a = 0.7$ .

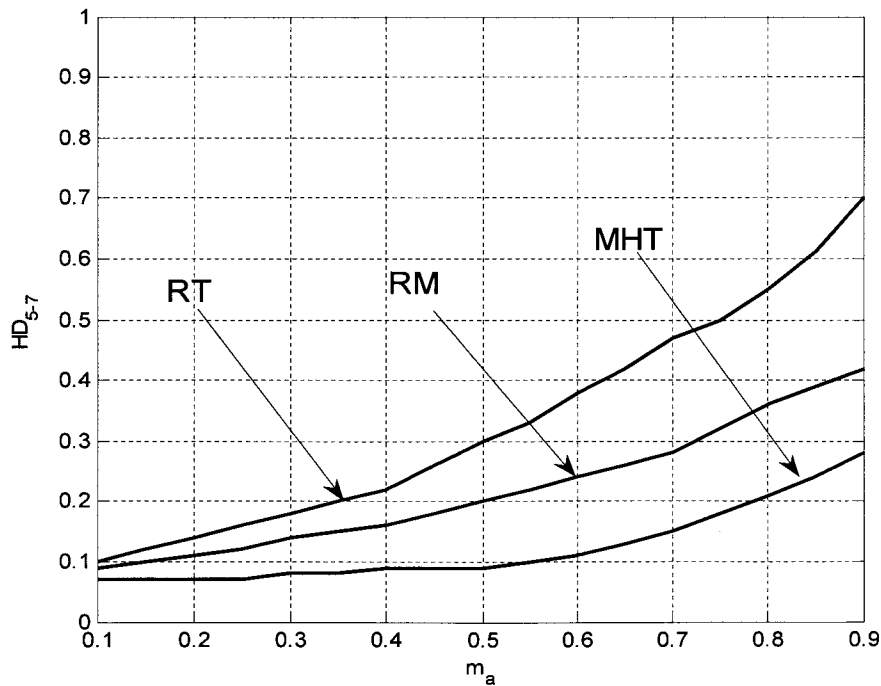


Fig. 4- 9 :- Index  $HD_{5-7}$  for RT, RM and MHT techniques.

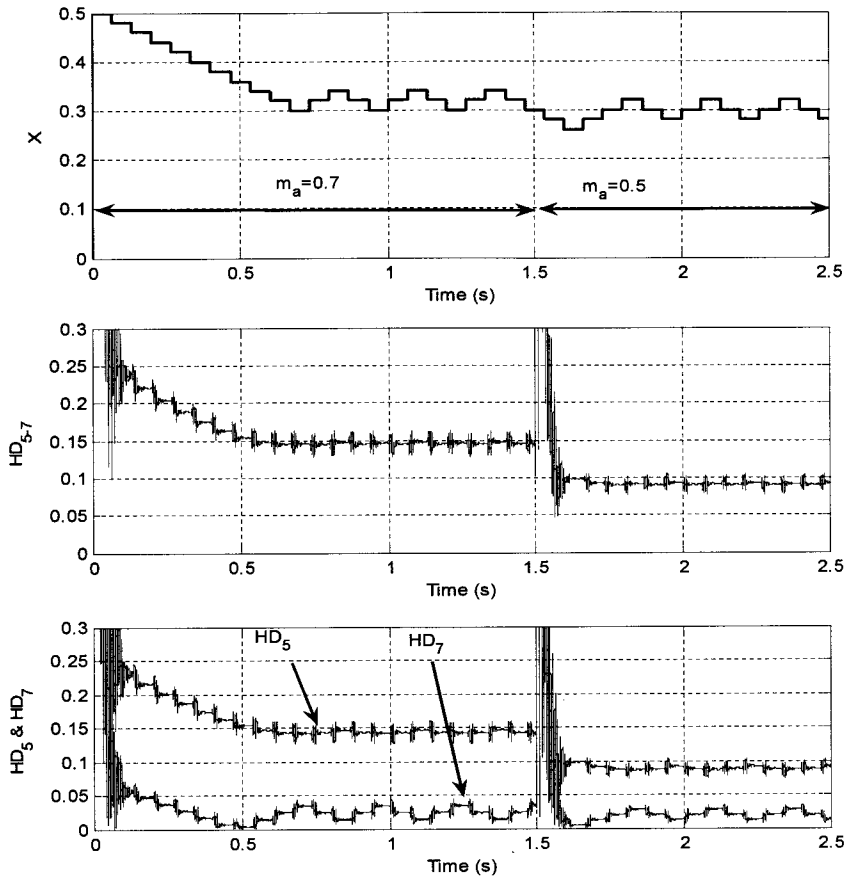


Fig. 4- 10 :- MHT technique reduces  $HD_{5,7}$  in CSC ac-side current when  $m_a = 0.7$  for 1.5s then  $m_a = 0.5$  for 1s.

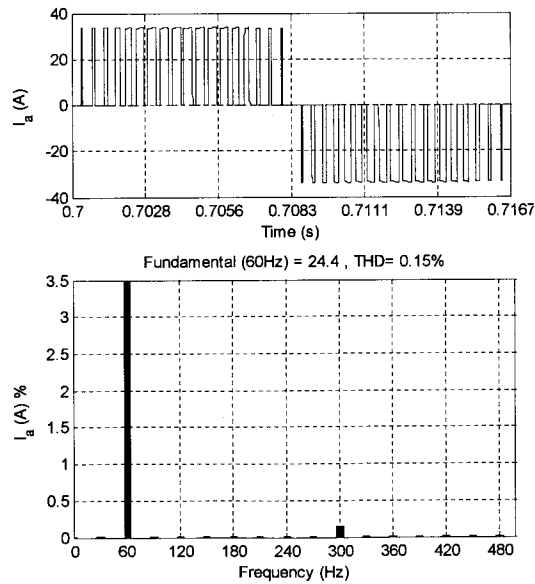


Fig. 4- 11 :- Index  $HD_{5,7}$  in the CSC ac-side current with MHT technique and  $m_a = 0.7$ .

### 4.3.3. ONE VARIABLE MHT FOR FILTERED CSC AC-SIDE CURRENT

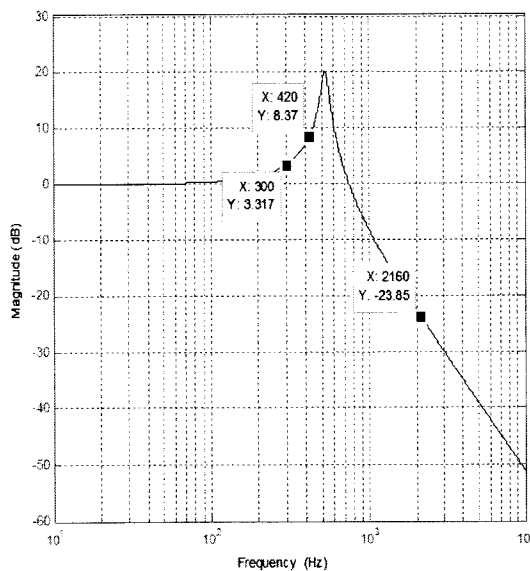
Until now equations in chapter three can be used instead of the complex MHT. The complexity is resulted from a feedback  $HD_{5-7}$  measurement. In the remainder of this chapter, two important aspects will be taken into consideration. They are ac-side filter design and the mandatory overlap period. Both aspects affect  $HD_5$  and  $HD_7$  differently, that supports the usage of MHT more than SQ3-CF. Yet, the straightforward approach presented in SQ3-CF is preferable when the slight reduction in  $HD_{5-7}$  is not necessary.

Let's start by the ac-side filter effect on  $HD_{5-7}$ . UPF between ac-side filter capacitor voltage for phase A ( $V_a$ ) and modulation index for phase A ( $m_a$ ) is assumed in this section. PF variation will be considered later on. In LSF-SVM-CSC the ac-side filter design is a challenge when  $f_{cycle} = 2160$  Hz. The damping resistance will be fixed to  $1\Omega$ . When traditional SQ1-SAs is used, then 9 pu (3mH & 30 $\mu$ F) cut-off frequency 2<sup>nd</sup> order ac-side current filter could not provide enough attenuation around switching frequencies component. Fig. 4- 12 (a) shows attenuation of around -23db for switching frequencies component. Fig. 4- 13 presents the ac-side harmonics spectrum with 9 pu filter when traditional SQ1-SAs is used. There, 5<sup>th</sup>, 7<sup>th</sup>, 11<sup>th</sup>, 13<sup>th</sup> and switching harmonics values are high. That leads to high distortion with THD = 8.9% for ac-side current in the PCC when  $m_a = 0.7$  and UPF. Fig. 4- 12 (a) shows that 5<sup>th</sup> and 7<sup>th</sup> harmonics are amplified by 3.3db and 8.3db when a 9 pu filter is used.

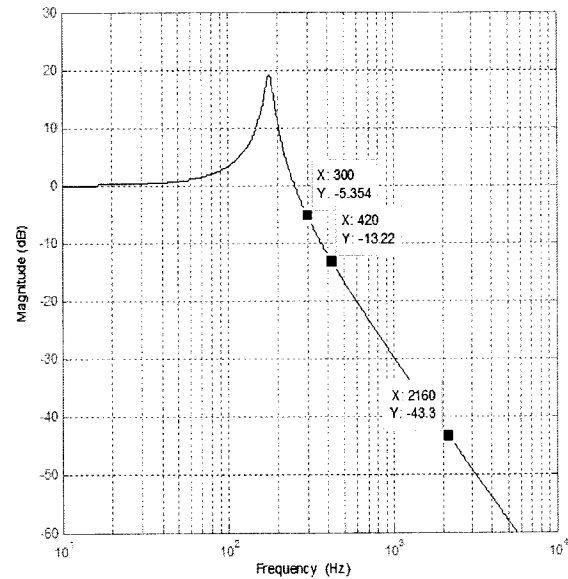
A filter between 5pu and 7pu cannot be used to reduce THD, although they can be able to attenuate switching frequencies harmonics to the permitted level, since it would amplify the 5<sup>th</sup> and 7<sup>th</sup> harmonics due to the resonance phenomenon as shown in Fig. 4- 14 when a 5.93pu (4mH & 50 $\mu$ F) filter is used. In this case THD = 11.6% was recorded.

A 10% tolerance in the values of the power side component is not uncommon. That can change the designed cut-off frequency during operation, where  $4\text{mH} \pm 10\% = 4.4\text{mH}$  or  $3.6\text{mH}$ ,  $50\mu\text{F} \pm 10\% = 55\mu\text{H}$  or  $45\mu\text{H}$ . That will lead 5.93pu filter to vary between around 5pu ( $4.4\text{mH} \& 55\mu\text{H} = 5.3\text{pu}$ ) and around 7pu ( $3.6\text{mH} \& 45\mu\text{H} = 6.6\text{pu}$ ).

The traditional solution for the difficulties of adjusting the exact filter cut-off frequency is using around 3pu bulky filter (2.97pu) with (8mH & 100μF) [6]. Fig. 4- 12 (b) shows that 5<sup>th</sup>, 7<sup>th</sup> and switching frequencies are attenuated by -5.3db, -13.2 db and -43.3db, respectively, when 3pu filter is used. That leads when SQ1-SAs is used to a good harmonic spectrum with THD = 1.8% in Fig. 4- 15. But a large costly  $L_{ac}C_{ac}$  filter is required. Beside, reduction in the reactive power range available in applications likes STATCOM [41].



(a) A 9pu filter.



(b) A 3pu filter.

Fig. 4- 12 :- The effect of ac-side filter on 5<sup>th</sup>, 7<sup>th</sup> and switching frequencies harmonics.

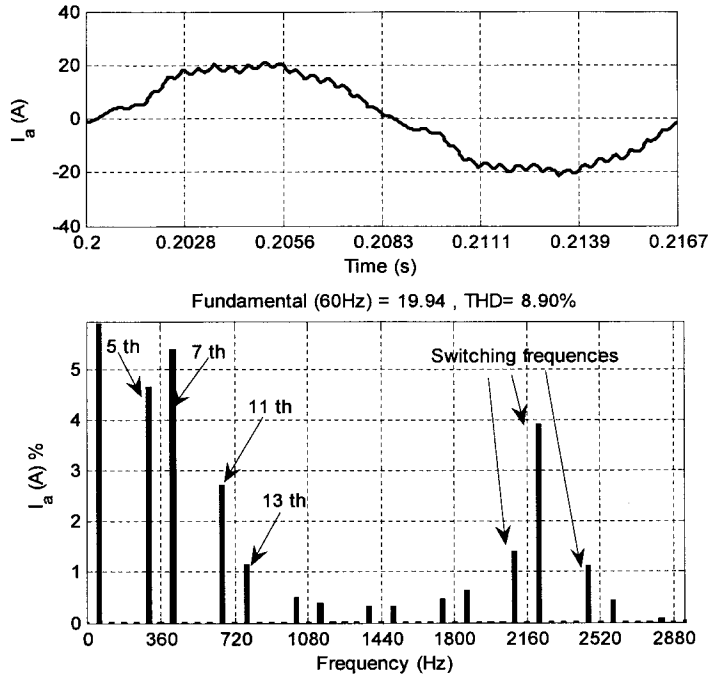


Fig. 4- 13 :- THD in CSC filtered ac-side current with SQ1-SAs, 9 pu filter and  $m_a=0.7$ .

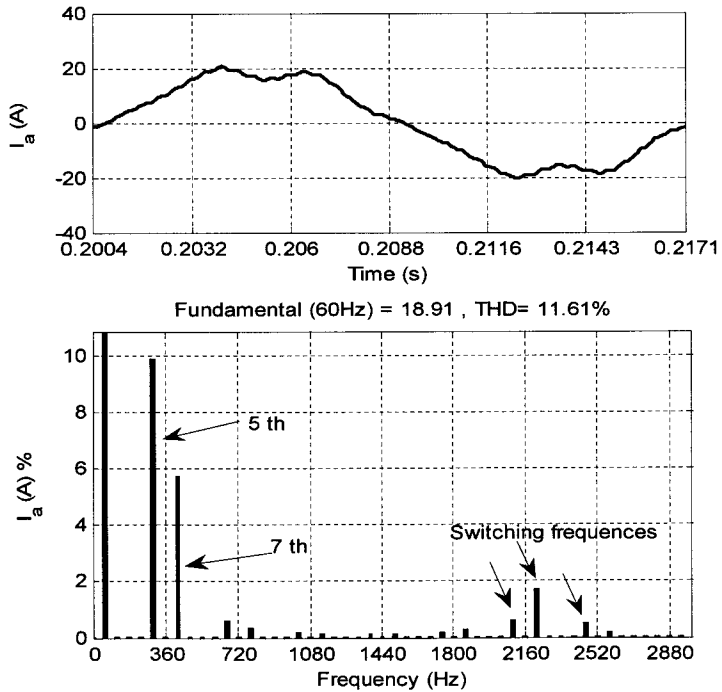


Fig. 4- 14 :- THD in CSC filtered ac-side current with SQ1-SAs, 5.93pu filter and  $m_a=0.7$

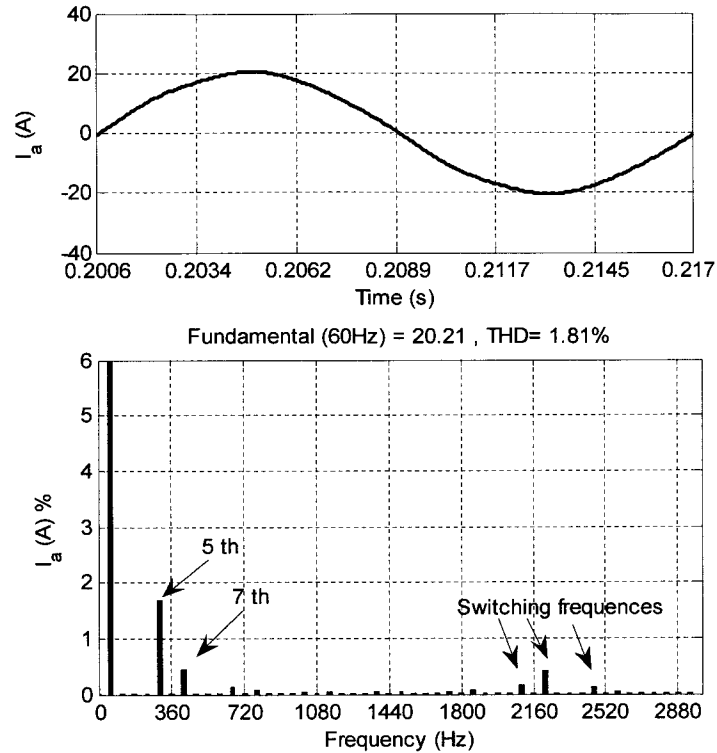


Fig. 4- 15 :- THD in CSC filtered ac-side current with SQ1-SAs, 3 pu filter and  $m_a = 0.7$ .

Small ac-side  $L_{ac}C_{ac}$  filters with cut-off frequencies between 5pu and 7pu are capable of providing enough attenuation to the switching harmonics. They can be used if the  $HD_{5-7}$  in the CSC ac-side current is reduced to virtual elimination point. Both of RM and RT with simple states ON times calculations give  $HD_{5-7} < 1\%$  in CSC ac side current. MHT with feedback process gives less  $HD_{5-7}$ , there  $HD_{5-7}$  is measured and MHT makes a decision, which permits reaching the least  $HD_{5-7}$ . So, MHT should be more effective than RM and RT if one uses a filter amplifying either 5<sup>th</sup> or 7<sup>th</sup> or both by different values, amplify both by the same value using in between cut-off frequency can be proposed theoretically, but in reality it is not possible since  $L_{ac}$  and  $C_{ac}$  filter values are not guaranteed to be fixed with operation. Also, the ac-side filter is connected to the PCC which may lead to vary  $L_{ac}$  and cut-off frequency.



Let's use 5.93pu accurate filter as an example while  $m_a = 0.7$  for 1.5s, then it is varied to  $m_a = 0.5$  for 1s. Fig. 4- 16 shows how MHT technique is able to reduce  $HD_{5-7}$ . Fig. 4- 17 showing that  $THD = 1.86\%$  when  $m_a = 0.7$ , this THD is similar to THD when 3pu filter and SAs-SQ1 are used. That mean a small size  $L_{ac}C_{ac}$  filter with around 6pu can be used along with MHT to reach a good harmonic spectrum. However, it is important to identify the effects of having inaccurate  $L_{ac}C_{ac}$  values on the filter's performance. An investigation of what is the result of using around 7pu filter with MHT in THD value is presented next. The same was done by the author for a 5pu filter in [55] and will not be discussed here.

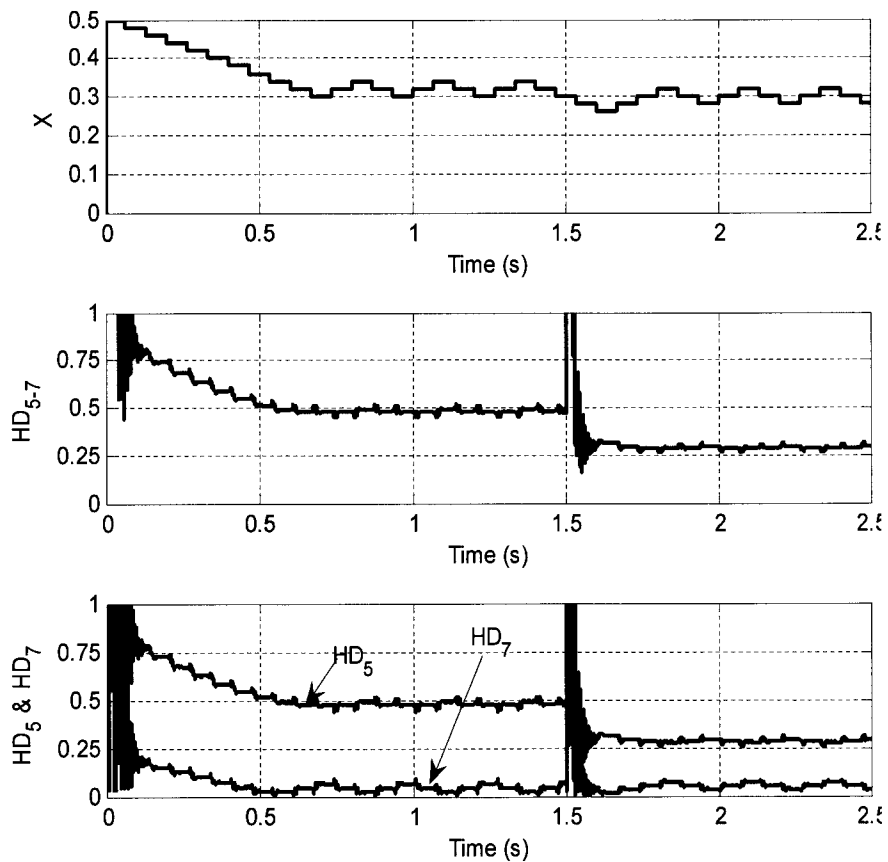


Fig. 4- 16 :- MHT technique reduces index  $HD_{5-7}$  in filtered ac-side current when  $m_a = 0.7$  for 1.5s then  $m_a = 0.5$  for 1s.

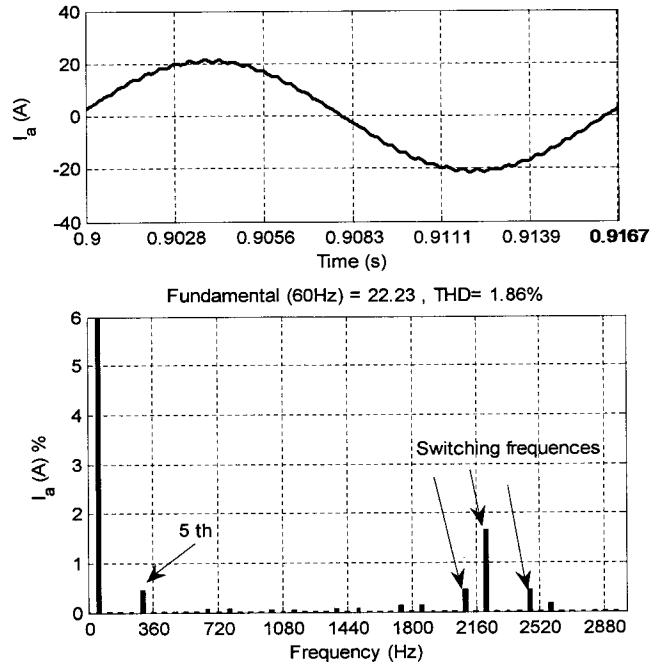


Fig. 4- 17 :- THD in CSC filtered ac-side current with MHT, 5.93pu filter and  $m_a = 0.7$ .

$HD_{5-7}$  for different  $m_a$  values for RM, RT and MHT techniques when 6.8pu (50 $\mu$ f & 3mH) filter is used are shown in Fig. 4- 18. MHT technique gives  $HD_{5-7} < 0.6\%$ . Other techniques have low  $HD_{5-7}$  at CSC ac-side current in Fig. 4- 9, but they are not ideal for LSF-SVM-CSC with 6.8pu filter when  $m_a$  is changing. The best values of X gives the least  $HD_{5-7}$  for MHT are marked by arrows in Fig. 4- 18, where the accuracy is  $\Delta X=0.01$ .

In Fig. 4- 19, when a 6.8pu filter is used and  $m_a = 0.8$  for the first 1.5s, the best value of X which is reached after around 0.5s is  $X = 0.36$  with  $HD_{5-7} = 0.46\%$ . The operating condition is changed after 1.5s to  $m_a = 0.4$ , then the best value of X is 0.22 with  $HD_{5-7} = 0.22\%$ . One can conclude that the larger the variation of  $m_a$  the larger the variation of the best X. Recall that when  $m_a$  was varied from  $m_a = 0.7$  to  $m_a = 0.5$  the variation in X was less. Fig. 4- 20 shows for 6.8pu filter when  $m_a = 0.8$  both of  $HD_{5-7} = 0.46\%$  and  $THD = 1.79\%$  when MHT technique is used, there MHT selects  $X = 0.36$ .

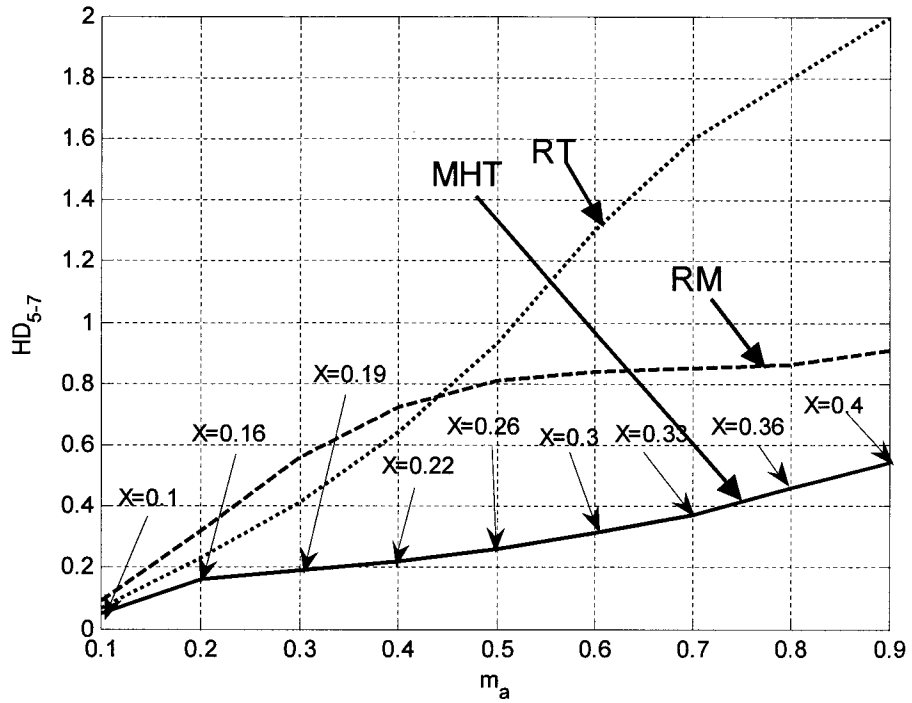


Fig. 4- 18 :- Index  $HD_{5-7}$  for RM, RT and MHT with 6.8pu ac-side filter.

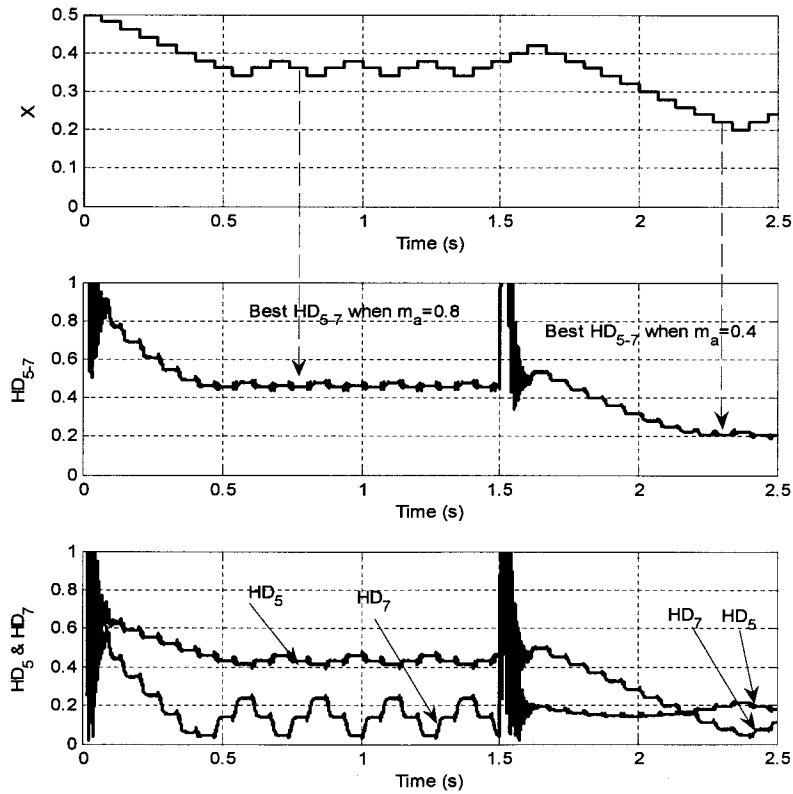


Fig. 4- 19 :- MHT technique reduces  $HD_{5-7}$  in the filtered ac-side current.

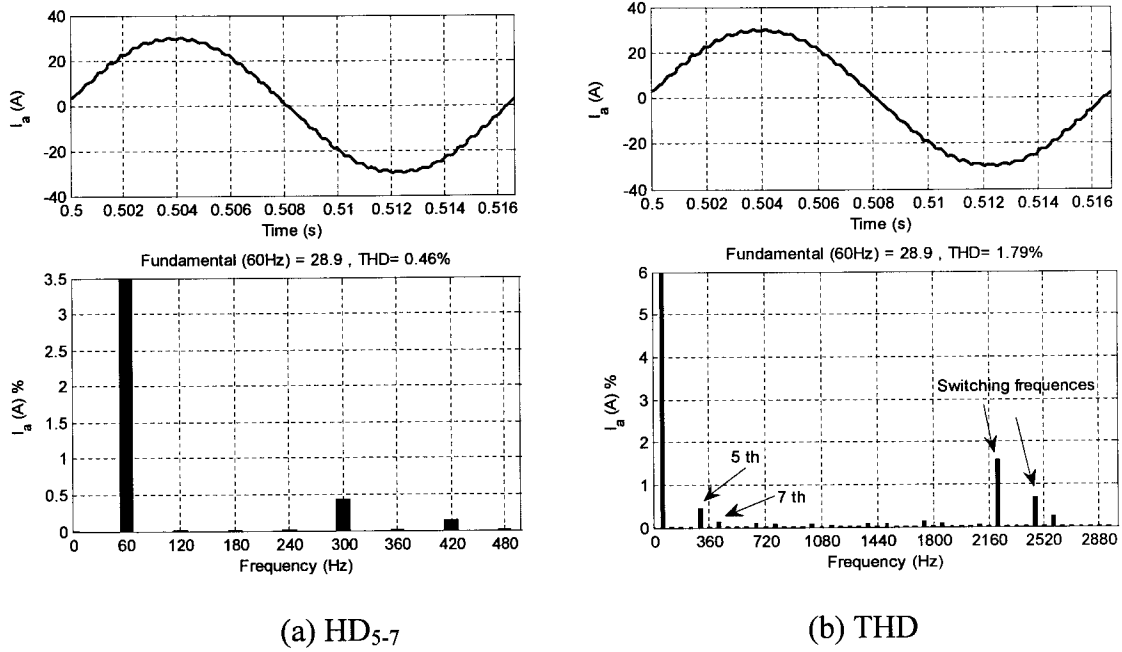


Fig. 4- 20 :- Index HD<sub>5-7</sub> and THD with MHT and 6.8pu ac-side filter at  $m_a = 0.8$ .

#### 4.4. THE OVERLAP PERIOD EFFECT ON HD<sub>5-7</sub>

In the previous section the transition of current between GTOs was proposed to be instantaneously, which is not practical in CSCs. In CSC a commutation (overlap) period is essential to ensure that there is no danger of being no path for the dc link current, to avoid overvoltage [6]. The overlap period should be long enough to turn on the previously off switch before turning off the conducting switch [6]. During the overlap period two GTOs, either of the lower or the upper group, should be ON but the dc-side current is in only one GTO. The current commutation between any two GTOs depends on the polarity of the line voltage between the two phases commutating those GTOs and consequently depends on the PF. The exact commutation instance occurs either at the beginning or at the end of the overlap period [54].

However, ambiguity in the exact commutation instance due to mandatory overlap period implies uncertainty in the switch current, and subsequently the ac-side line current during the overlap periods. Thus for this period, the magnitude of the ac-side line current is not under the direct control of the SVM scheme, but it is controlled by the ac-side line capacitor voltages. That should affect the ac-side line current. The effect of overlap period in the fundamental ac-side current value was covered in [54]. Overlap period was not considered in the SVM concept. So, it affects the current harmonic spectrum and the index  $HD_{5-7}$  as well, that will be considered here. CSCs based on GTOs need from  $5\mu\text{s}$  to  $10\mu\text{s}$  overlap period. RM or RT or MHT techniques should be used to reduce  $HD_{5-7}$ . Although MHT is adapted in this section, but description in MHT is complicated due to X variations. Since RT is easier for description, let's describe the overlap period effect on LSF-SVM-CSC when states ON times are calculated using RT and  $m_a = 0.5$ .

Suppose that the SV, which rotates by constant speed, is in the cycle three of the sector one with  $m_a = 0.5$  and  $10\mu\text{s}$  overlap period. Referring to Fig. 1- 3, states  $I_i$ ,  $I_{i+1}$  and  $I_z$  in sector one are represented by  $I_1$  (S1 and S2),  $I_2$  (S3 and S2),  $I_9$  (S5 and S2), respectively. In Fig. 4- 21, RT concept is presented with and without the overlap period. If the overlap period is not taken into consideration the current pass in CSC switches as recommended by SVM. However, in reality the overlap period is used. And, the switch that conducts during the overlap period is depending on the voltage polarity what can have a detrimental effect on the  $HD_{5-7}$ . For instance in Fig. 4- 21, if the PF angle causes  $V_a > V_c > V_b$  then the overlap period will cause actual  $t_i$  to increase by the overlap period time while actual  $t_{i+1}$  is reduced by the overlap period time. And,  $t_{z1}$  and  $t_{z2}$  have no changes. So, S1 conducts current for longer time and S3 conducts current for less time

than what is described by ideal RT. Also, if the PF angle causes  $V_b > V_a > V_c$  then the overlap period causes actual  $t_{i+1}$  to increase by overlap period time while actual  $t_{z2}$  is reduced by overlap period time. The actual  $t_i$  and  $t_{z1}$  have no change. So, S3 conducts current for longer time and S5 conducts current for less time than what was described by ideal RT. Each voltage polarity results in variations of states ON times with respect to the ideal SVM technique without overlap period.

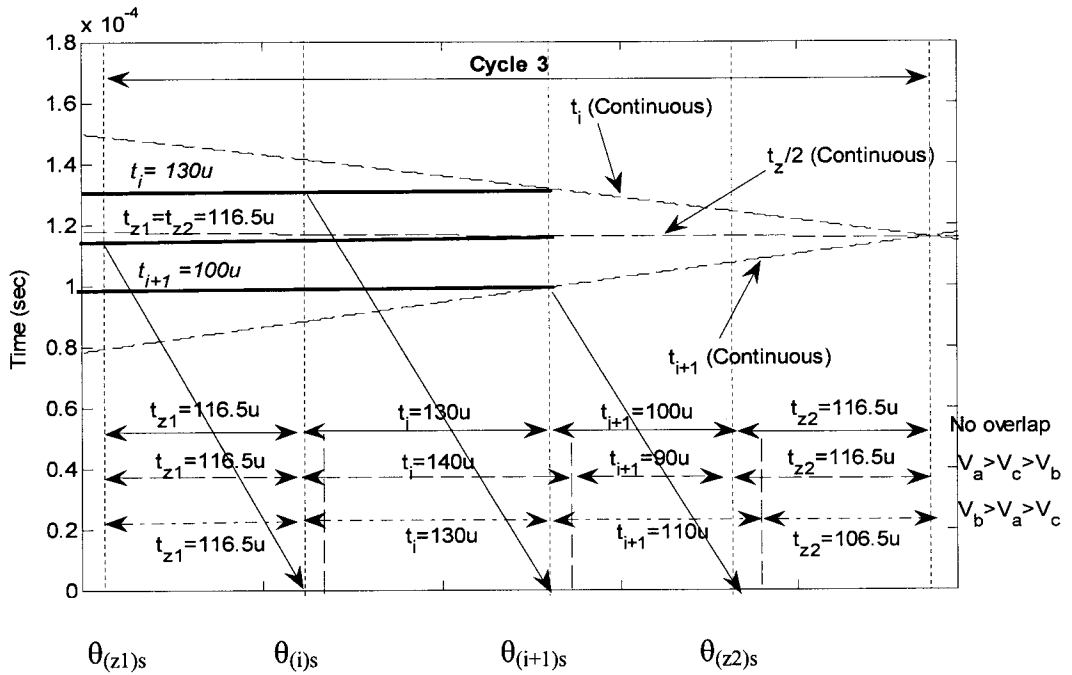


Fig. 4- 21 :- Overlap period effect on RT technique for one SVM cycle (3<sup>rd</sup> cycle) in SVM sector one when  $m_a = 0.5$ .

#### 4.4.1. ONE VARIABLE MHT FOR CSC FILTERED AC-SIDE CURRENT WITH OVERLAP PERIOD

In the ideal CSC, the variations in the PF do not affect that much the value of X where least  $HD_{5-7}$  is found. But if the overlap period effect is taken into consideration,

which is the case in the real CSC, the PF effects on the states ON times appear as described in Fig. 4- 21. In this case, RM and RT are not sufficient to reduce  $HD_{5.7}$  for LSF-SVM-CSC, especially with ac-side filters with cut-off frequency more than 3pu (5pu to 9pu). That is because in those cases the duration of current flow in CSC switches will not depend only on  $m_a$  but also on PF.

Complex analysis should be done to know where the current is during the overlap period. In this case, one may use a very complex technique that varies states ON times with PF after an analysis of the current position depending on the line to line voltage polarity, not used. Or, use a tracking technique in reducing  $HD_{5.7}$ . Thus, the MHT perturb X without knowing where the current is during the overlap period and observe  $HD_{5.7}$  is a suitable procedure. Unlike the previous section where the best X is between 0 and 0.5, when the overlap period is taken into consideration one cannot anticipate the value of X and the SIMULINK model should be slightly modified accordingly.

In this section an ac-side filter with a 6.8pu cut-off frequency, 5 $\mu$ s overlap period and  $m_a = 0.7$  are used. The 6.8pu filter amplifies  $HD_{5.7}$  at the PCC. The 5 $\mu$ s is common in GTOs based CSCs. Fig. 4- 22 illustrates the results when MHT technique is used to reduce  $HD_{5.7}$ . It starts with PF = 0.5 lagging for 1.5s, the  $m_a$  ( $I_{a.ref}$ ) lags the capacitor voltage ( $V_a$ ) by 60°. Then, the PF is changed to 0.866 leading,  $m_a$  leads  $V_a$  by 30°. There, although  $m_a$  is not changed, the PF variation with overlap period effect changes the best value of X. The operation starts with X = 0.5, then MHT searches for the value of X with least  $HD_{5.7}$ . When PF = 0.5 (lagging) the best X = 0.26 with  $HD_{5.7} = 2.23\%$ . When PF changes to 0.866 (leading), then  $HD_{5.7}$  is reduced by a self adjustment from MHT, by increasing X towards X = 1 and settling at X = 0.76 with  $HD_{5.7} = 1.38\%$ , instead of

keeping  $0 < X < 0.5$ , as it is the case when overlap period is not taken into consideration. If large overlap period exist, then states ON times calculation with single variable MHT concept is still reducing  $HD_{5-7}$  to an acceptable limit.

Fig. 4- 23 (a) illustrates the phase shift between  $V_a$  (distorted waveform) and  $m_a=0.7$  ( $I_{a.ref}$ ) for phase A when the PF = 0.5 (lagging). Also, Fig. 4- 23 (b) illustrates  $HD_{5-7}$  for the current waveform. Although ac-side filter amplified the  $HD_{5-7}$ , the MHT technique results in  $HD_{5-7} < 3\%$ . Fig. 4- 23 (b) results for  $HD_5$  and  $HD_7$  can be also seen from Fig. 4- 22 when  $X = 0.26$  and the time is between 1s and 1.5s.

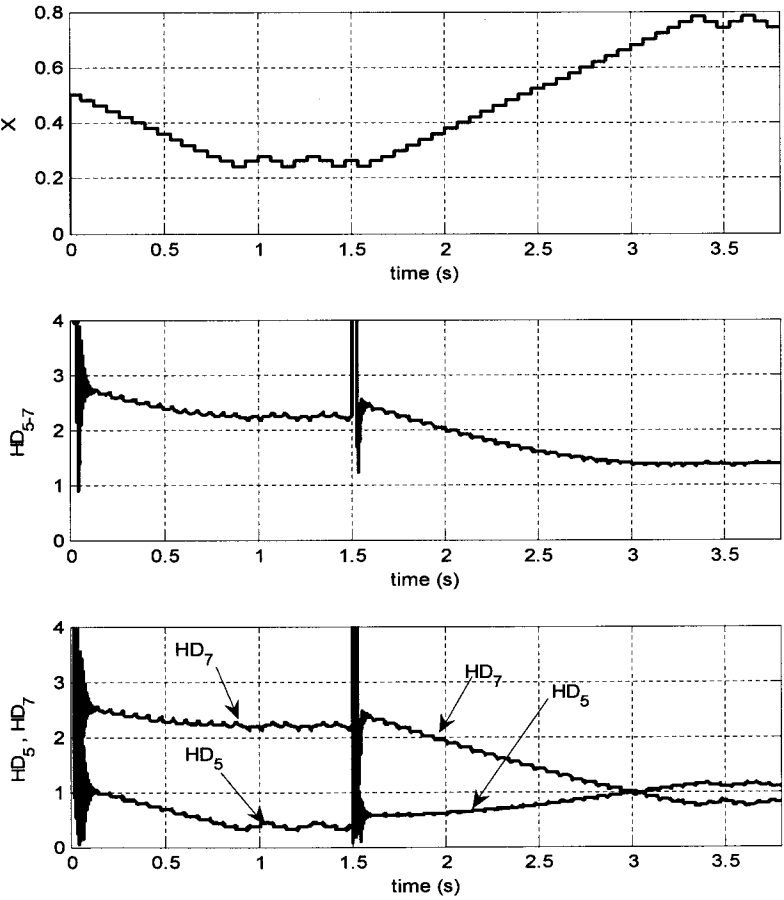


Fig. 4- 22 :- MHT reduces  $HD_{5-7}$  in the filtered ac-side current with 6.8 pu filter,  $5 \mu s$  overlap period and  $m_a = 0.7$ , PF = 0.5 (lagging) for 1.5s then PF = 0.866 (leading).



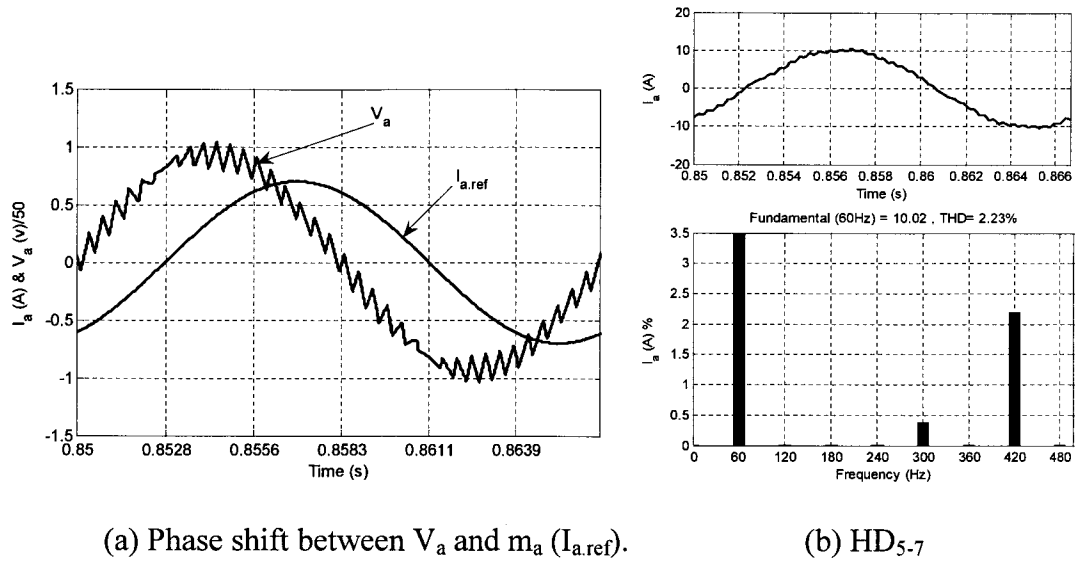


Fig. 4- 23 :- Investigation for single variable MHT when PF = 0.5 (lagging) and  $m_a = 0.7$ .

#### 4.4.2. TWO VARIABLE MHT FOR CSC FILTERED AC-SIDE CURRENT WITH OVERLAP PERIOD

When the overlap period is neglected, there is symmetry between active states ON times for SQ3 when one of SAM, RM, EQ, CF, RT and MHT techniques is used. This means that, the average of  $t_i$  and  $t_{i+1}$  are equal,  $\sum_{c=1}^{c=6} t_{c(i)} \approx \sum_{c=1}^{c=6} t_{c(i+1)}$ . With Overlap period, depending on the PF  $t_i$  and/or  $t_{i+1}$  for each SVM cycle may be changed. Then, SAM, RM, EQ, CF and RT techniques for SQ3 are presenting HD<sub>5-7</sub> due to unsymmetrical between  $t_i$  and  $t_{i+1}$ , when overlap period is taken into consideration.

Single variable MHT ties the pre-overlap  $t_i$  and the pre-overlap  $t_{i+1}$  together with (4- 4) and  $\sum_{c=1}^{c=6} t_{c(i)} \neq \sum_{c=1}^{c=6} t_{c(i+1)}$  after overlap effect appears. That prevents reducing HD<sub>5-7</sub> under a certain limit for certain values of PF, which is clear in Fig. 4- 22 with 6.8pu filter when  $m_a = 0.7$  and PF = 0.5 (lagging) for the first 1.5s, where HD<sub>5-7</sub> is more than 2%. A separation between  $t_i$  and  $t_{i+1}$  calculations is proposed in this subsection. If

symmetry is lost due to the overlap period then there are two variables  $X_1$  and  $X_2$  represented in (4- 5), instead of (4- 4).

$$X_1 = \frac{A}{B}, \quad X_2 = \frac{C}{D} \tag{4- 5}$$

To implement the two variables MHT concept, SIMULINK blocks in Fig. 4- 24 are used. There, Fig. 4- 7 blocks are used in two similar subsystems, one for  $X_{1\text{-new}}$  and the other for  $X_{2\text{-new}}$ , they are used as inputs of Fig. 4- 8 to calculate states ON times.

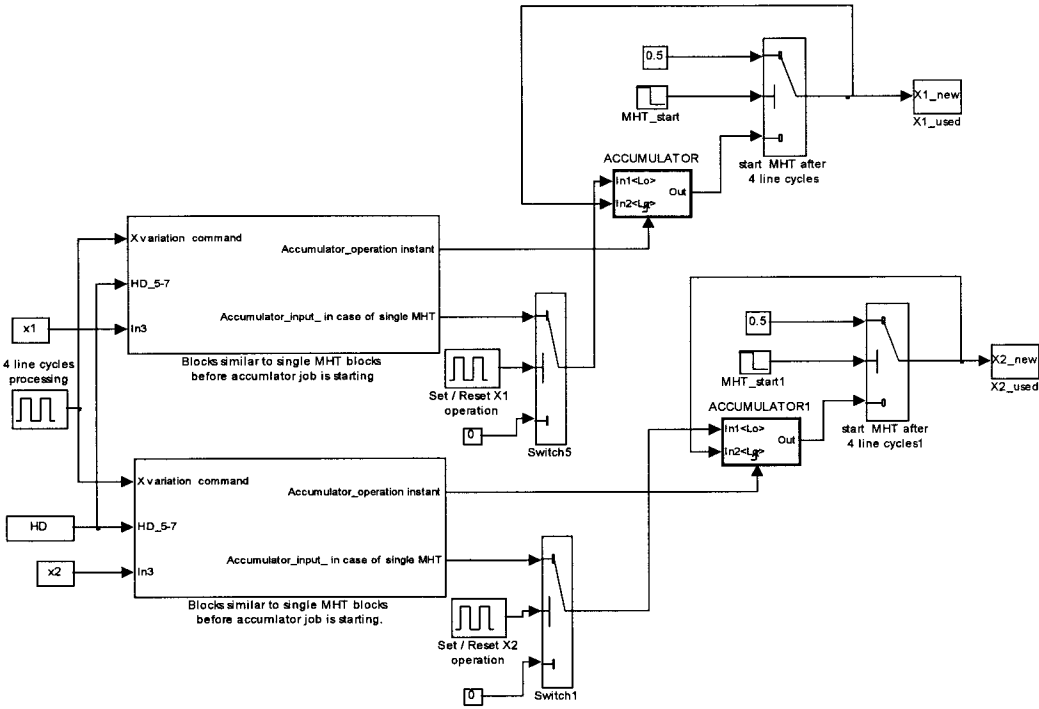


Fig. 4- 24 :- SIMULINK model for two variables MHT.

In the previous subsection, Fig. 4- 22 showed high  $HD_{5-7}$  with  $PF = 0.5$  (lagging) and  $m_a = 0.7$ , more than the other case. So, this case is selected for the two variable MHT investigations. In Fig. 4- 25, two variables MHT is applied for  $PF = 0.5$  (lagging) and  $m_a = 0.7$ . On can note in Fig. 4- 25 that, two variables MHT starts as a single variable MHT for the first 1.33s, that mean  $X_1 = X_2$  and (4- 5) can be simply written as (4- 4). Then  $X_2$

is fixed while  $X_1$  is changed for the second 1.33s, which is enough for the tracking process to reach the required  $X_1$ . After 2.66s from starting instant,  $X_1$  is fixed while  $X_2$  is changed. In this period the adjustment of  $X_2$  is achieved, that does not take long, 0.5s.

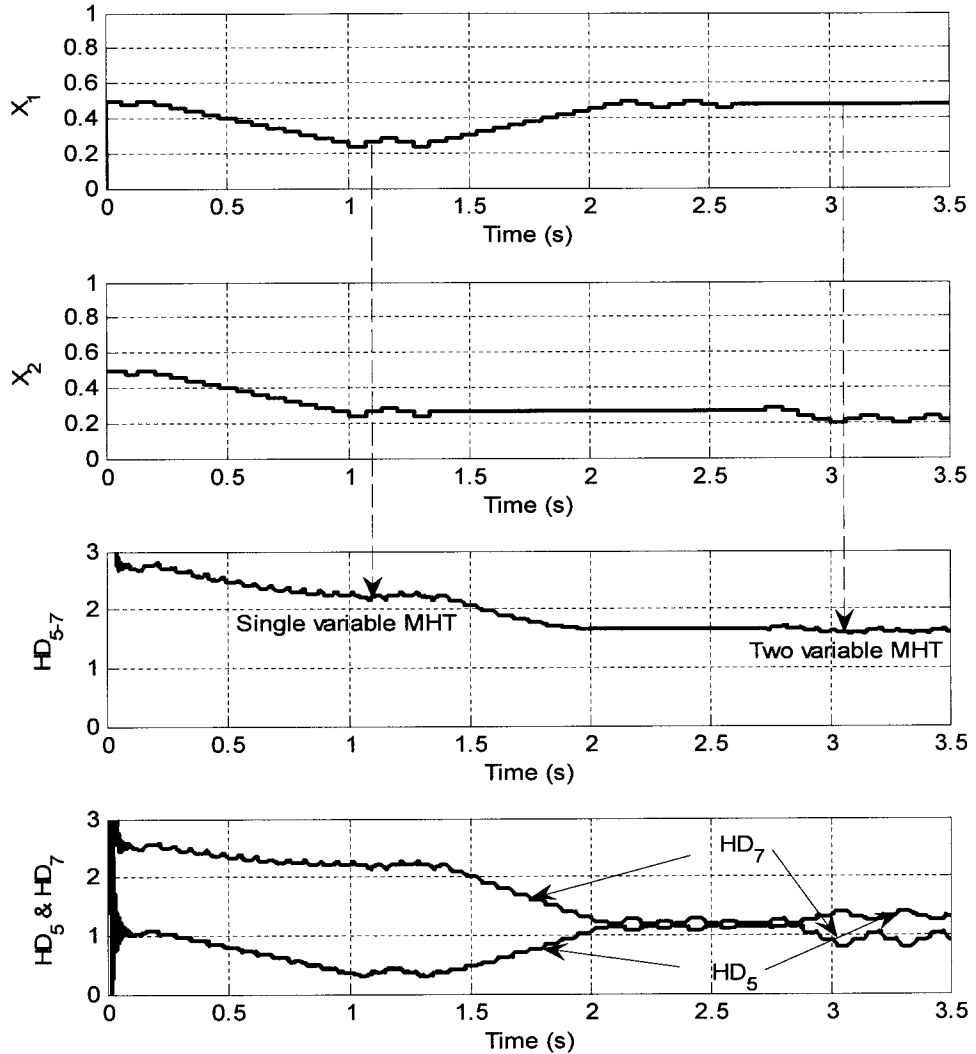
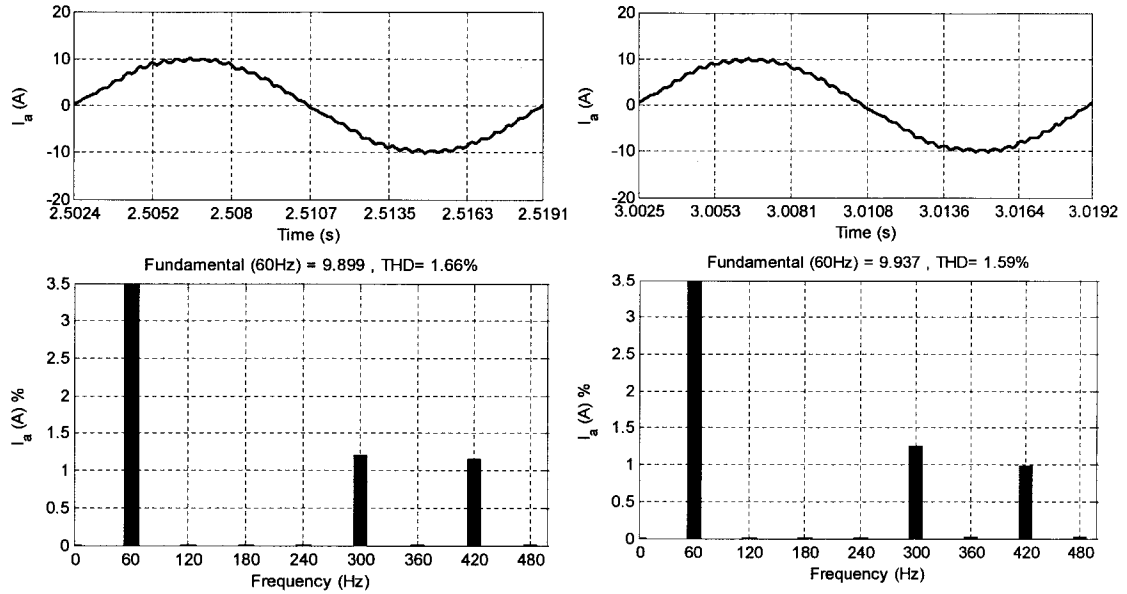


Fig. 4- 25 :- Two variables MHT technique reduces index  $HD_{5-7}$  in the filtered ac-side current with 6.8pu filter and 5 $\mu$ s overlap period,  $m_a = 0.7$  and PF = 0.5 (leading).

Varying  $X_1$  and  $X_2$  followed by varying only  $X_1$  then varying only  $X_2$  should be repeated over and over, to create two variable MHT deals with the operating conditions variations. Fig. 4- 25 is shows  $X_1$  and  $X_2$  variation for 3.5s along with  $HD_{5-7}$ ,  $HD_5$  and

HD<sub>7</sub>. Fig. 4- 26 presents HD<sub>5</sub> and HD<sub>7</sub> with two variables MHT when  $m_a = 0.7$  and PF = 0.5 (lagging) after 2.5s,  $X_1$  is optimized. And after 3s,  $X_1$  and  $X_2$  are optimized. One can notice more reduction in HD<sub>5-7</sub> with two variables MHT which gives HD<sub>5-7</sub> = 1.59 % in Fig. 4- 26 (b), than, single variable MHT, which gives HD<sub>5-7</sub> = 2.32 % in Fig. 4- 23 (b).



(a)  $X_1$  optimized while  $X_2$  not yet, at 2.5s in Fig. 4- 25      (b)  $X_1$  and  $X_2$  are optimized.

Fig. 4- 26 :- Index HD<sub>5-7</sub> in the CSC ac-side current with two variables MHT, 5  $\mu$ s overlap period, 6.8 pu filter cut off frequency,  $m_a = 0.7$  and PF = 0.5 (leading).

## 4.5. EXPERIMENTAL INVESTIGATION AND CHALLENGES

The proposed states ON times calculation techniques described in this chapter, RM, RT and MHT, are instantaneous techniques. To achieve experimentally the theoretical results, one should have 0.5 $\mu$ s to 1 $\mu$ s sampling step. The widely used DSP (DS-1103) presents 20 $\mu$ s to 30 $\mu$ s sampling step. OPAL-RT (OP-5000) can operate with 6 $\mu$ s sampling step with RM or RT. 6-switches MOSFET-based CSC with 6 $\mu$ s sampling step and overlap period investigates the proposed techniques experimentally. A 25V<sub>ph-N</sub>

source voltage with  $10\Omega / 100\text{mH}$  dc side load is used. A certain operating condition tested theoretically, the one presented in Fig. 4- 22 with  $m_a = 0.7$  with  $\text{PF} = 0.866$  (leading), is selected to be tested experimentally. RM technique result is recorded by adjusting  $X = 0.5$ . And, MHT technique result is recorded by adjusting  $X = 0.76$ , the  $X$  presented in Fig. 4- 22. The result of SAs technique is used for comparison. In the PCC,  $\text{HD}_{5-7} = 10\%$  in the current appears in SAs, as in Fig. 4- 27 (a). One can theoretically use  $6.8\text{pu}$  filter with  $\text{HD}_{5-7} < 3\%$  for RM technique and  $\text{HD}_{5-7} < 2\%$  for MHT technique, with  $1\mu\text{s}$  sampling step, that cannot be reached experimentally due to  $6\mu\text{s}$  minimum permitted sampling step. Fig. 4- 27 presents experimental results for RM technique with  $\text{HD}_{5-7} = 5.6\%$  and MHT technique with  $\text{HD}_{5-7} = 4.1\%$ . If  $1\mu\text{s}$  sampling step is exists, experimental results similar to the simulation results presented in the previous section can be found. That should be possible soon, with the advent of faster microprocessors and DSPs.

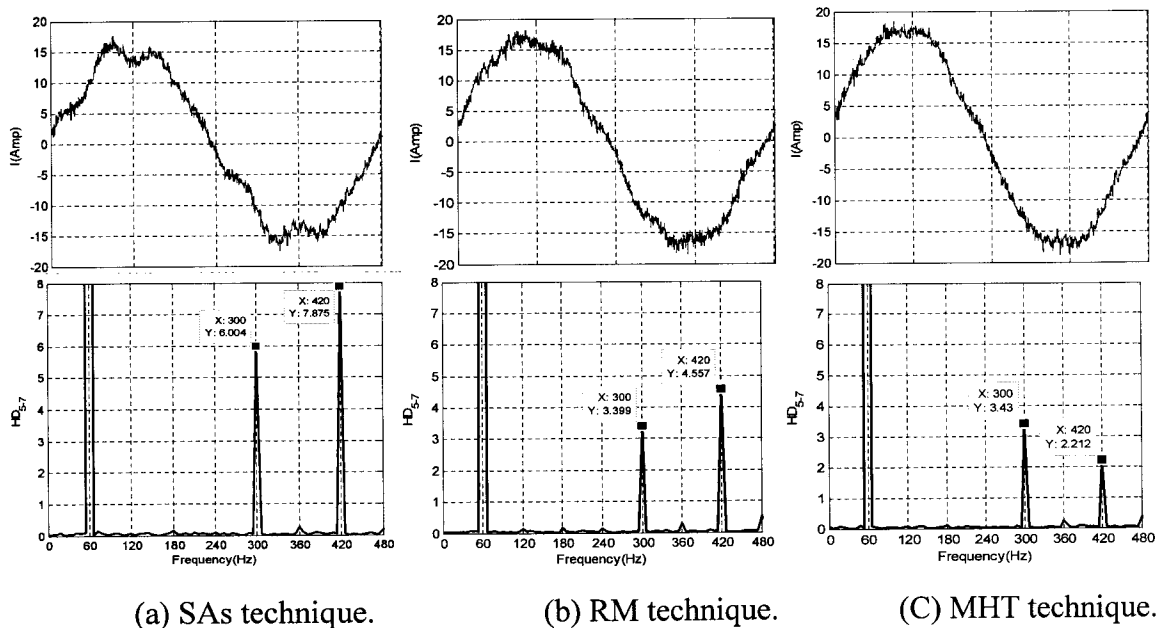


Fig. 4- 27 :- Experimental  $\text{HD}_5$  and  $\text{HD}_7$  in the filtered CSC ac-side current with  $6.8\text{ pu}$  filter when  $m_a = 0.7$  and  $\text{PF} = 0.866$  (leading).

## 4.6. CONCLUSION

In this chapter, the magnitude of  $HD_{5-7}$  resulting from LSF-SVM-CSCs is minimized to the virtual elimination point. When  $f_{\text{cycle}} = 2160$  Hz,  $HD_{5-7}$  is traditionally around 3.5% of the fundamental current magnitude at the CSC ac-side current. SQ3 is selected as a basis of reducing  $HD_{5-7}$ . Two states ON times calculation procedure are presented, RM and RT, which yield  $HD_{5-7} < 1\%$ . Single variable MHT (MHT) technique is proposed to further minimize  $HD_{5-7}$  to around 0.1% and less than 0.25% for all values of  $m_a$  at the CSC ac-side current.

The proposed MHT technique depends on measuring the value of  $HD_{5-7}$  and reducing it with perturbing and observing principle. During MHT operation aspects like keeping symmetry between active states in SVM sector, calculating states ON times nearly in the same instant and achieving nearly an instantaneous calculations for SV, generate a variable X, which can satisfy those conditions as much as possible when varied. During X variation, one aspect takes more or less priority than the others. When  $X = 0$ , states ON times are calculated in the same instant, while when  $X = 0.5$  instantaneous calculations for SV is achieved. For all X values, symmetry assessment between active states is performed. When X is changed from  $X = 0.5$  towards  $X = 0$ , the priority of same instant calculation increases while priority for instantaneous calculations for SV is reduced. In MHT, X and  $HD_{5-7}$  are measured, and the X variation is decided by comparing values of previous and recent  $HD_{5-7}$ . X variations reduce  $HD_{5-7}$  until reaching the virtual elimination point with least  $HD_{5-7}$ .

For GTOs based CSC, a 9pu 2<sup>nd</sup> order low pass filter in the ac-side does not provide the enough attenuation for the dominant switching harmonics. In such a case, a

bulky 3pu cut-off frequency filter should be used, since filters around 6pu would amplify the non-negligible non-characteristic LOH (5<sup>th</sup> and 7<sup>th</sup>) created by conventional SVM-CSCs. There the traditional SVM states ON times calculation procedures result in up to  $HD_{5-7}=15\%$ , which is not acceptable. The proposed MHT technique allowed the use of a small filter with 6.8pu cut off frequency to filter the CSC ac-side current with  $HD_{5-7} < 0.6\%$ , in the same time 6.8pu filter can give the attenuation required for switching frequencies harmonics when  $f_{\text{cycle}} = 2160 \text{ Hz}$ .

Another practical challenge is the ambiguity in the exact commutation instant due to the overlap period in GTOs based CSC, which implies uncertainty of current flow in the switches due to PF variations. Independently of the  $m_a$ , PF, ac-side filter cut-off frequency and overlap period the proposed MHT technique kept the  $HD_{5-7} < 3 \%$ . More reduction in  $HD_{5-7}$  is achieved by modifying the tracking process in MHT technique to deal with large overlap periods, by proposing two variable MHT techniques which gives  $HD_{5-7} < 2\%$ . An experimental investigation demonstrated the effect of correct states ON times calculation on  $HD_{5-7}$ . An issue discussed in [55] and not discussed here is a modification in the proposed MHT technique to operate with better transient.

## CHAPTER 5

### 5. HARMONICS REDUCTION IN CSC USING FUZZY LOGIC

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#### 5.1. INTRODUCTION

In the previous chapter,  $HD_{5.7}$  resulting from LSF-SVM-CSCs was significantly reduced to a point of virtual elimination. However, the results obtained with MHT technique are not ideal. The variation in  $X$  ( $\Delta X = 0.02$  up and down) is present all the time. That resulted from a lack of intelligence in the tracking process.

Among well known artificial intelligence techniques Fuzzy logic with low number of membership functions is suitable in on-line applications. Genetic Algorithm, as example, is not suitable for on-line applications due to large time used in running the programs. That is why, Fuzzy logic has been used to design the main SVM concept on-line in [56], [57]. In this chapter, Fuzzy logic is investigating means for adjusting the parameter  $X$ . Fuzzy logic is tuned to sense reaching the best value of the variable  $X$ . It should be noted that no emphasis is placed on the speed of response, which require a complex Fuzzy logic. The proposed Fuzzy logic can reach the exactly required value of the variable  $X$  with an acceptable flexibility. Materials presented in this chapter are in [58]. Fuzzy logic is used to decide the states ON times for least  $HD_{5.7}$  in LSF-SVM-CSCs. The target of Fuzzy logic is to achieve fast states ON times adjustment with the least  $HD_{5.7}$  in steady state.



## 5.2. PROPOSED FUZZY LOGIC TECHNIQUE

Recall from the previous chapter that,  $X$  is the distance between active states transition point at  $\theta_{(i+1)s}$  and each active state ON time calculating instant as a percentage of this active state ON time. Also, for each  $m_a$ , values of  $X$  between 0 and 0.5 result in lower  $HD_{5-7}$ . There is one value of  $X$  has the least  $HD_{5-7}$  for each operating condition. This accurate value of  $X$  was not reached in previous chapter. There was a  $0.02X$  lack of accuracy due to a constant perturbation.

The proposed Fuzzy logic state ON time calculation technique using SIMULINK blocks is shown in Fig. 5- 1. Those blocks are used to measure the Fuzzy logic inputs,  $HD_{5-7}$  variation ( $\Delta HD_{5-7}$ ) and  $X_{old}$  variation ( $\Delta X_{old}$ ), and to calculate the output,  $X_{new}$  variation ( $\Delta X_{new}$ ).  $HD(K)$ ,  $HD(K-1)$ ,  $X(K)$ , and  $X(K-1)$  are triggered blocks of sample and hold. Every four ac-side current line cycles, the present  $HD(K)$  subtracts the previous  $HD(K-1)$  and the result is  $\Delta HD_{5-7}$  (first input of Fuzzy logic). A similar process is applied for the  $X$  channel to generate input  $\Delta X_{old}$  (second input of Fuzzy logic). Fuzzy logic with block diagram in Fig. 5- 2 was trained to reach  $X_{new}$  with the least  $HD_{5-7}$ . It is preferable to start with  $X = 0.5$ , that leads to less time for Fuzzy logic to get the least  $HD_{5-7}$  variable  $X_{new}$ . Recall that RM with  $X = 0.5$  give better results than RT with  $X = 0$ .

Trained rule base are introduced in Table 5- 1, input variables  $\Delta H_{5-7}$  and  $\Delta X_{old}$  universe of discourses are divided into seven and three Fuzzy sets, respectively. The universe of discourse for the output variable ( $\Delta X_{new}$ ) is divided into seven Fuzzy sets. The input membership functions for Fuzzy model are introduced in Fig. 5- 3. They are  $\Delta H_{5-7}$  and  $\Delta X_{old}$ . Output functions for Fuzzy model  $\Delta X_{new}$  are introduced in Fig. 5- 4. Membership functions are dense at the center to provide greater sensitivity in the region

near minimum  $HD_{5-7}$ . The surface for the Fuzzy logic is introduced in Fig. 5- 5. The output of the Fuzzy logic is a Fuzzy set. However, a crisp output value is required. Hence, the output of the Fuzzy logic should be defuzzified, the centroid method is used for defuzzification [59]. The model was developed on a trial-and-error basis to meet the desired performance criteria.

A suitable tuning gain ( $G$ ) is used for  $\Delta HD_{5-7}$  to match the variations in  $m_a$ ,  $f_{cycle}$  (represented by  $N_{CS}$ ) and input ac-side filter cut-off frequency variations. Tuning gain  $G$  is changed to match the inputs to the respective universes of discourse as illustrated in Fig. 5- 1, providing a larger step variation of  $X$  during the transient phase and an almost zero step variation of  $X$  in the steady-state.

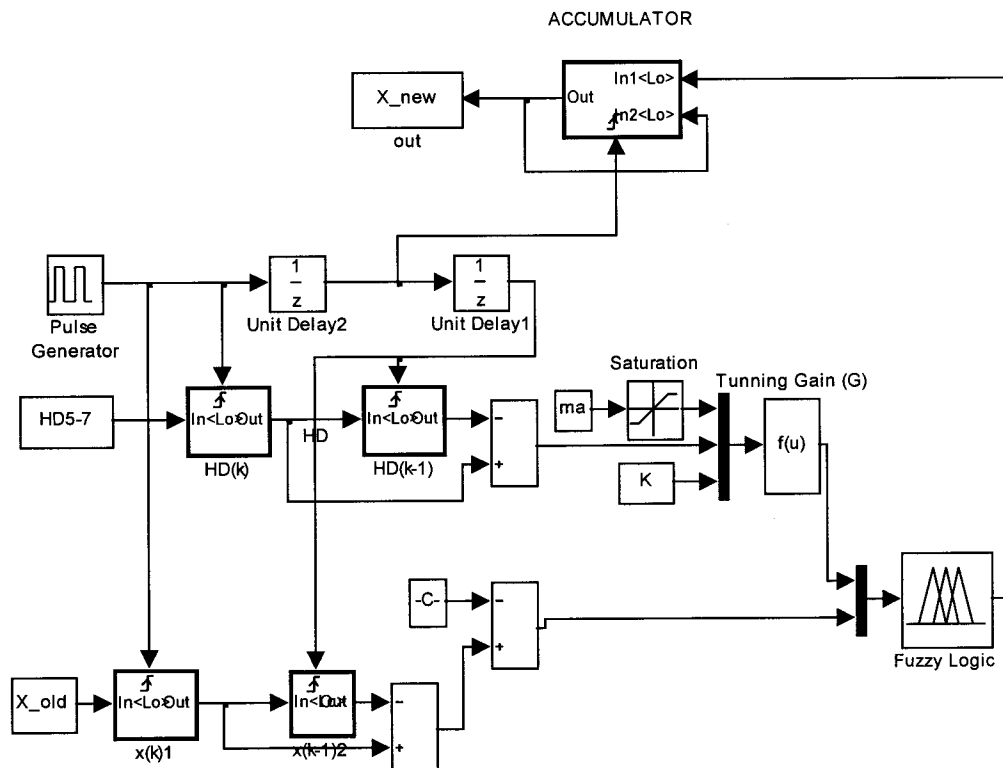


Fig. 5- 1 :- SIMULINK blocks calculate states ON times using Fuzzy logic.

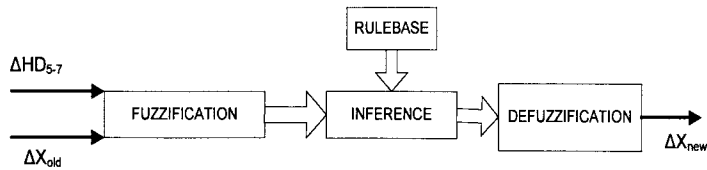
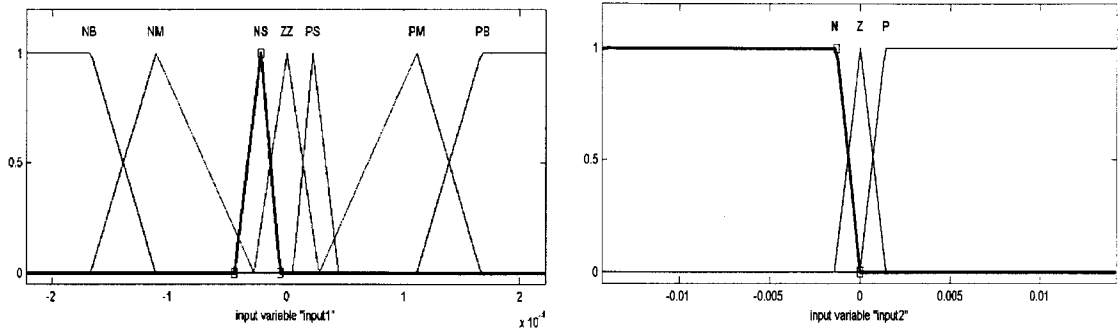


Fig. 5- 2 :- Internal construction of Fuzzy logic.



(a) Input  $\Delta HD_{5-7}$ .

(b) input  $\Delta X_{old}$ .

Fig. 5- 3 :- Input membership functions for the Fuzzy model.

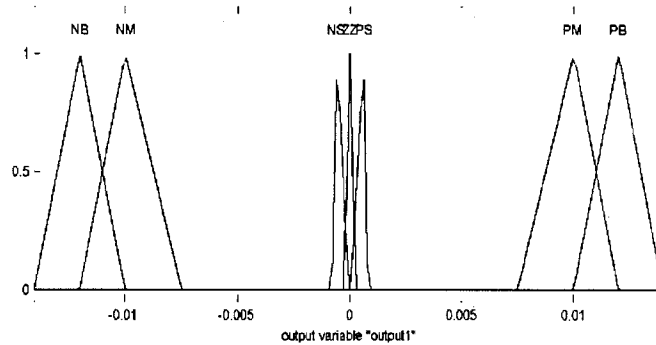


Fig. 5- 4 :- Output  $\Delta X_{new}$  membership functions for the Fuzzy model.

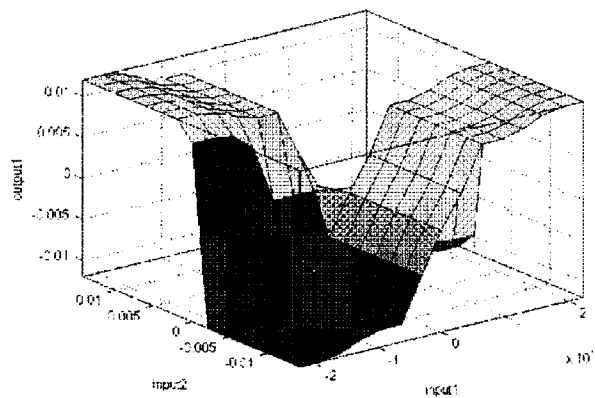


Fig. 5- 5 :- Surface for the Fuzzy logic.

TABLE 5- 1 :- RULE BASE FOR THE FUZZY MODEL

Rule No.	If $\Delta HD_{5-7}$ is	And $\Delta X_{old}$ is	Then $\Delta X_{new}$ is	Rule weights
1	PB (Positive Big)	P (Positive)	NB (Negative Big)	1.0
2	PM (Positive Mid.)	P	NM (Negative Mid.)	1.0
3	PS (Positive Small)	P	NS (Negative Small)	1.0
4	PB	N	PB	1.0
5	PM	N (Negative)	PM	1.0
6	PS	N	PS	1.0
7	NB (Negedive Big)	P	PB (Positive Big)	1.0
8	NM (Negative Mid.)	P	PM (Positive Mid.)	1.0
9	NS (Negative Small)	P	PS (Positive Small)	1.0
10	NB	N	NB	1.0
11	NM	N	NM	1.0
12	NS	N	NS	1.0
13	PB	Z (Zero)	NM	0.5
14	PM	Z	NS	0.5
15	NB	Z	PM	0.5
16	NM	Z	PS	0.5
17	ZZ (Zero)	P	NS	0.5
18	ZZ	N	PS	0.5
19	ZZ	Z	ZZ (Zero)	0.5

One can conclude from previous chapters that,  $m_a$  is affecting the value of  $HD_{5-7}$ . Also,  $\Delta HD_{5-7}$  when  $X$  changing is proportional to  $HD_{5-7}$ . That mean  $\Delta HD_{5-7}$  is depending on  $m_a$ . If tuning gain ( $G$ ) for  $\Delta HD_{5-7}$  channel is designed for a certain  $m_a$  that will optimize Fuzzy logic operation at this  $m_a$ . Besides, the best  $X$  will be reached for a band around that  $m_a$ .  $G$  should be affected by  $m_a$  to permit a good operation of Fuzzy logic. If  $m_a < 0.1$  or  $m_a > 0.9$  Fuzzy logic will not be tuned easily so saturation block is used.

Fuzzy logic tuning gain ( $G$ ) should be changed if either the input ac-side filter cut-off frequency or  $N_{CS}$  is changed. In those cases, a variable defined as  $K$  in Fig. 5- 1, which is the  $HD_{5-7}$  at CSC ac-side when  $N_{CS} = 6$  divided by  $HD_{5-7}$  in the required tuned conditions for RM technique, is used in tuning factor equation adjustment in Fig. 5- 1. Also, both of  $\Delta HD_{5-7}$  and  $\Delta X_{new}$  membership functions are adjusted to avoid Fuzzy logic settling at undesired  $X$  or oscillating around the desired  $X$  for long time.

### **5.3. HARMONICS REDUCTION IN CSC AC-SIDE CURRENT**

Fuzzy logic technique is used to reduce  $HD_{5-7}$  at CSC ac-side current. Fig. 5- 6 shows how Fuzzy logic can reach the best value of  $X$  with an acceptable speed, settling on the best  $X$  and regain its capability to vary  $X$  again when  $m_a$  is changed to resettle on the best  $X$  independent on how small should be the variation of  $X$ . Starting by selecting  $X = 0.5$  when  $m_a = 0.7$  which results in  $HD_{5-7} = 0.28\%$ , Fuzzy logic technique decreases  $X$  to decrease  $HD_{5-7}$  gradually until  $X = 0.305$ , where  $HD_{5-7}$  will equal  $0.15\%$ . If  $X$  is decreased beyond  $0.305$ , then,  $HD_{5-7}$  will increase again. In Fig. 5- 6, after 3s from starting  $m_a$  is changed from  $m_a = 0.7$  to  $m_a = 0.5$ . Fuzzy logic technique selects  $X = 0.29$  with  $HD_{5-7} = 0.09\%$  as least  $HD_{5-7}$  when  $m_a = 0.5$ .

In Fig. 5- 6, states ON time adjustment using Fuzzy logic needs around 1.5s to reach the optimum X during start up. The time required to reach X with least HD<sub>5,7</sub> can be reduced if Fuzzy logic design is complicated with more rules. That is not suitable for on-line applications, fast Fuzzy logic when training cause oscillation around the best X for as if it is an under-damped system. There are no significant differences between HD<sub>5,7</sub> values obtained with MHT and Fuzzy techniques. This can be found by comparing results in Fig. 5- 6 with one which was presented in Fig. 4- 10 and Fig. 4- 11.

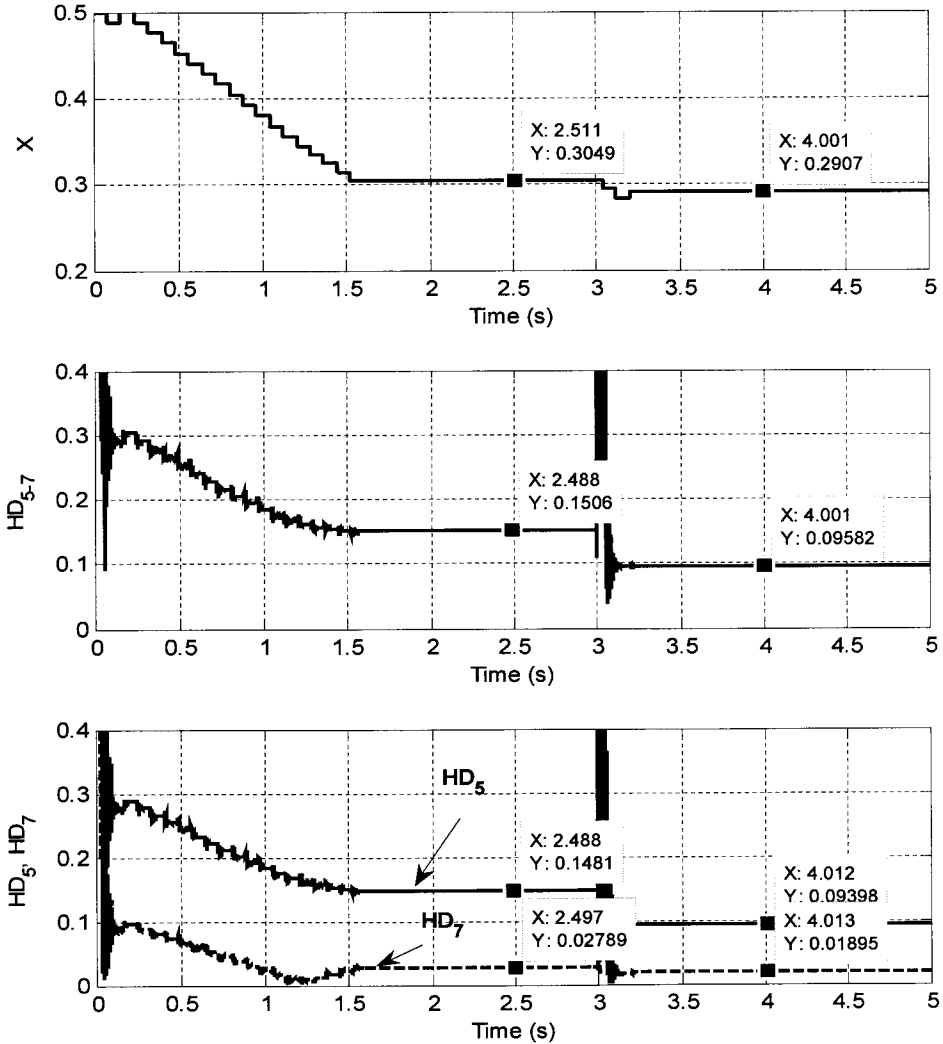


Fig. 5- 6 :- Fuzzy logic reduces HD<sub>5,7</sub> in CSC ac-side current.

## 5.4. HARMONICS REDUCTION IN THE GRID CURRENT

The 6.8pu cut-off frequency filter for the ac-side current is used in this section. Fuzzy logic tuning factor resulting from ac-side filter is adjusted to  $K = 1/3$ . RM, RT and Fuzzy logic techniques  $HD_{5-7}$  with 6.8pu filter are shown in Fig. 5- 7. It should be noted that Fuzzy logic inputs is received from filtered CSC ac-side current at PCC. Fuzzy logic technique gives lower  $HD_{5-7}$  than both of RM and RT techniques. The best values of X selected by Fuzzy logic technique to give the least  $HD_{5-7}$  are shown in Fig. 5- 7. Fuzzy logic adds accuracy in deciding the value of X, which gives a small improvement in  $HD_{5-7}$  if compared with MHT technique. That accuracy of choosing X in Fuzzy logic can be noted by comparing the results shown in Fig. 5- 7 and Fig. 4- 18. Accuracy of deciding X gives around 0.02 % improvement in  $HD_{5-7}$  if compared with previous chapter.

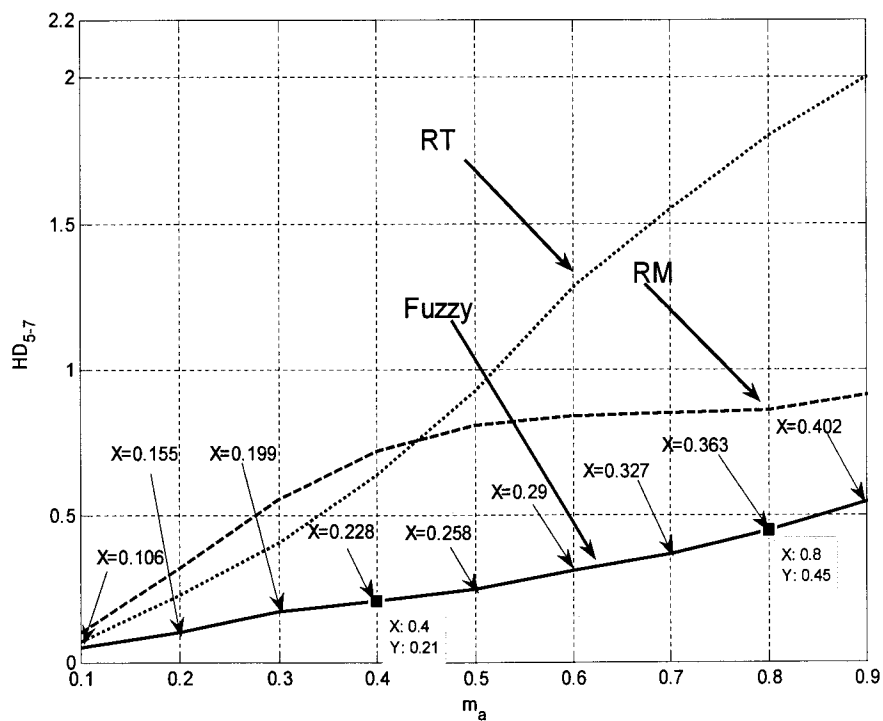


Fig. 5- 7 :-  $HD_{5-7}$  for RM, RT and Fuzzy logic with 6.8pu CSC ac-side filter.

Fig. 5- 8 investigates Fuzzy logic technique with 6.8pu filter cut-off frequency. Operation starts with  $m_a = 0.8$  and  $X = 0.5$  that gives  $HD_{5-7} = 0.86\%$ . Fuzzy logic technique reduces  $HD_{5-7}$  gradually by reducing  $X$  until  $X = 0.363$  where  $HD_{5-7} = 0.45\%$ . After 3s, the operating condition is changed from  $m_a = 0.8$  to  $m_a = 0.4$ . In this case, the best value of  $X$  become  $X = 0.228$  with  $HD_{5-7} = 0.2\%$ .

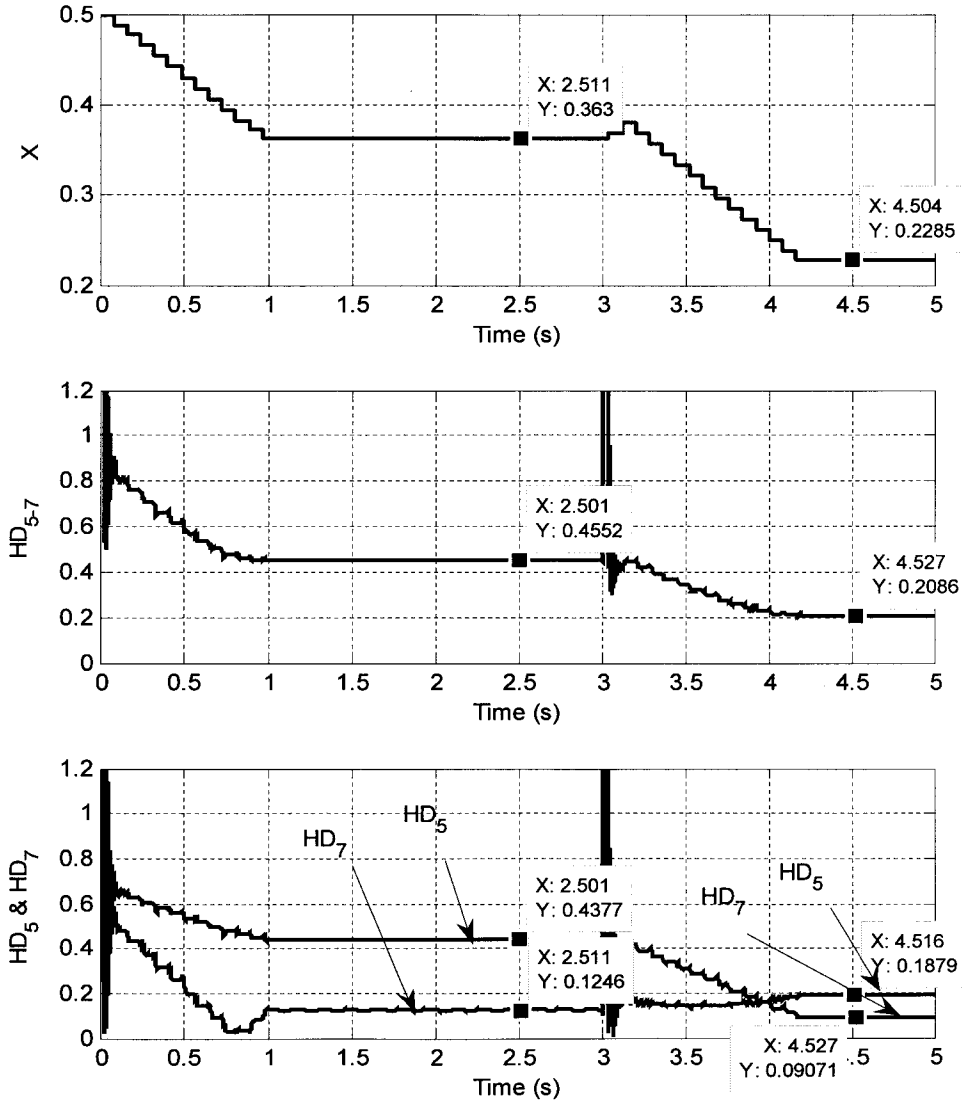


Fig. 5- 8 :- Fuzzy logic technique reduces  $HD_{5-7}$  in the filtered ac-side current with 6.8pu filter when  $m_a = 0.8$  for the first 3s then  $m_a = 0.4$  for the last 2s.



## 5.5. CONCLUSION

In this chapter Fuzzy logic is adopted to reduce the magnitude of the  $HD_{5-7}$  resulting from LSF-SVM-CSCs. Fuzzy logic technique reduces  $HD_{5-7}$ , which permits the use of a small filter with 6.8pu cut-off frequency and  $HD_{5-7} < 0.6\%$  in the PCC. The best operating point is reached with accuracy more than MHT. Reaching the best X can be done fast at the expense of Fuzzy logic simplicity. For the simple Fuzzy logic presented here no oscillations around the best X exist, as it was the case in MHT. When the operating point is changed Fuzzy logic acts by varying the value of X to reach the new least  $HD_{5-7}$ .

## PART- 2.

# SPACE VECTOR MODULATED HYBRID BI-DIRECTIONAL CURRENT SOURCE CONVERTERS

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## CHAPTER 6

### 6. PROPOSAL OF TWO NEW HYBRID CSCs TOPOLOGIES

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#### 6.1. INTRODUCTION

Silicon controlled rectifiers (SCR) based current source converters (CSCs) illustrated in Fig. 6- 1 have been used for many years in high power variable speed drives and HVDC transmission systems [1]. It is usually operated with phase control in the continuous conduction mode (CCM). There are two SCRs on at all times in a three-phase full-bridge topology. One in the top group (three cathode-connected SCRs) and another in the bottom group (three anode-connected SCRs).

SCR commutation is simple for operation in the CCM. A SCR is turned-off by firing a *more* forward biased SCR in the same group. The load current is diverted to the newly fired SCR while the previous one is subject to a reverse voltage for ensuring safe commutation. There is no need for creating overlap of on switches in the same phase to guarantee a path for the dc-side load current during commutations, as in fully controllable CSCs. The firing angle of the SCRs has to be kept smaller than a certain value ( $\alpha_{max}$ ) so

as to keep the SCRs reverse biased for an interval larger than their turn-off time ( $t_q$ ), thus preventing commutation failures. Connecting 6 SCRs based CSR with 6 IGBTs based VSR external circuit to improve the performance of CSR and give acceptable range of PF were proposed in [60] - [62].

Since SCRs cannot be blocked via a gate signal, they are usually limited to operation at line frequency which is 60 Hz in North America. Each SCR is fired once per line cycle, and is blocked by firing a more forward biased SCR. As a result, current LOHs are generated and the active and reactive powers of the converter cannot be controlled independently [63]. Simply put, the six SCRs based CSCs shown in Fig. 6- 1 is rugged and affordable but they create large LOHs and do not allow active power (P) and reactive power (Q) to be controlled independently.

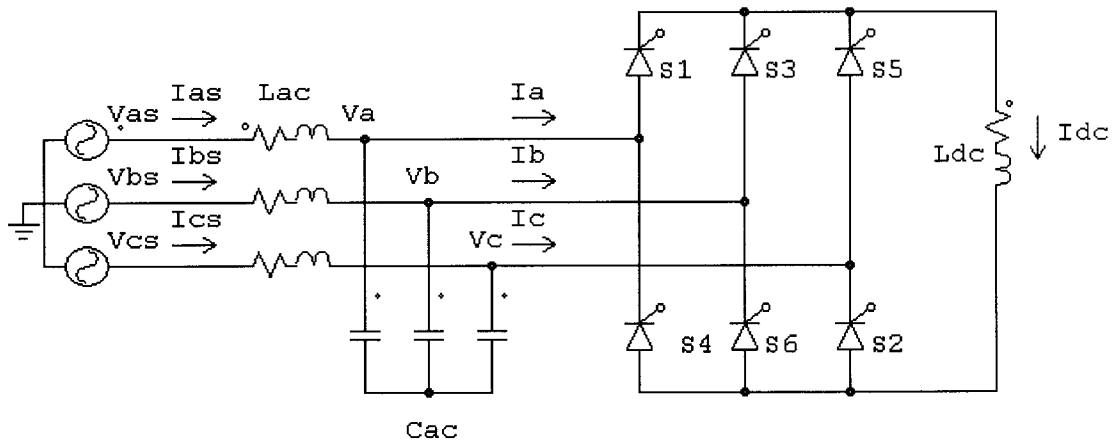


Fig. 6- 1 :- Six SCRs based CSC.

These 6 SCRs based CSC drawbacks can be overcome with topologies based on a more costly force-commutated switches, by replacing the six SCRs with six force-commutated switches, thus allowing the use of PWM techniques presented in chapter one of the thesis: SPWM, SHE and SVM. 6-switches (fully controllable) CSCs require a

more refined circuit than SCRs based ones for generating the gating signals in order to fully benefit from the flexibility offered by these topologies. In these cases, it is possible that the dc-side load current be switched from phase A to B or C or even to a disconnection between the ac-side and dc-side. In such a case all three-phase currents are zero and the dc-side current has to be free-wheeled through one of the legs of the CSC. This is not a major problem for force-commutated topologies where all switches are fully-controllable and can be turned off via a gating signal. As a result, the harmonic spectrum of the ac-side current can be significantly improved.

6-switches GTO based CSC presented in Fig. 1- 2 needs around 1/3 of its forwarded current to be withdrawn from its gate to turn-off [1]. That complicates its gate drive circuits. 6-switches IGCT or SGCT based CSC are more popular but still have some drawbacks presented in [64], [65]. Symmetric GTO based CSC is also presented in [66]. Till now the usual procedure of implementing 6-switches CSC is the one used for implementing CSR in Fig. 6- 2, where six IGBTs plus six diodes are used [6], [67].

Nowadays IGBT is designed only with a parallel diode. Due to IGBTs low reverse voltage blocking capability they cannot be used alone in design a CSC even if the parallel diode does not exist [1]. In LSF applications, conduction power losses dominate switching one. This is partially due to the fact that four semiconductor components are present in the dc-side current path. As a result, 6-switches IGBT based CSCs are characterized by high cost in implementation and conduction power losses. Connecting inexpensive 6 SCRs based CSC with 6- switches based CSC as a multilevel inverter to permit high range of PF was discussed in [68].

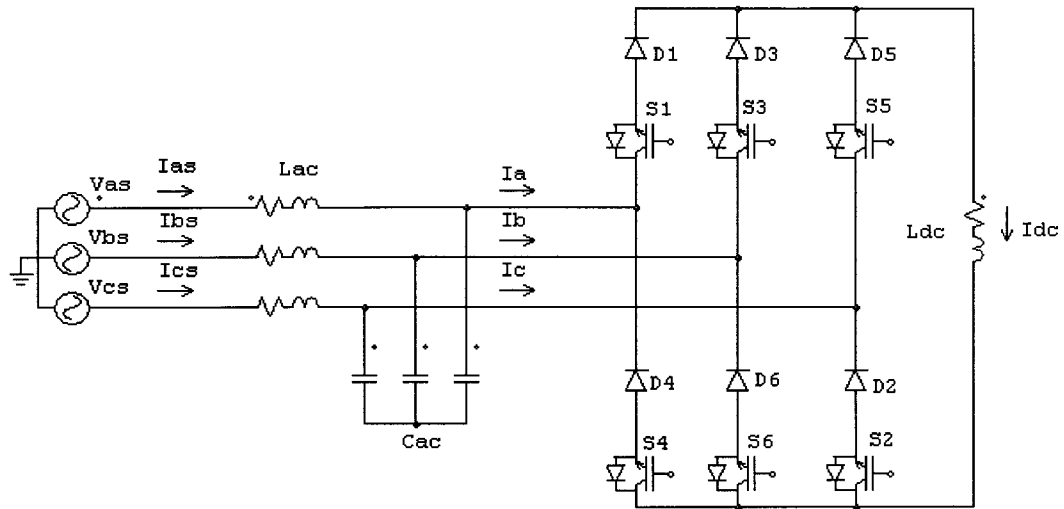


Fig. 6- 2 :- Six IGBTs based CSC.

## 6.2. PREVIOUSLY PROPOSED HCSCs

In order to reduce the cost of the 6-switches IGBT based CSCs with PWM capability, hybrid topologies implemented with SCRs and force-commutated switches have been proposed in the literature. The concept there is to reduce conduction power losses by reducing number of semiconductor devices in current path and to reduce implementation cost by reducing number of costly IGBTs. HCSCs capable of operating with unconstrained power factor have been reported in the literature, but mostly for ac-dc-ac converters used in variable speed drives [69] - [71]. In hybrid ac-dc-ac current source converters active commutation of SCRs is achieved with an energy rebound circuit with two GTOs, one dc capacitor and six diodes connected to the output of the dc-ac converter. Many HCSCs were presented in the [63] with some hints for each. Among those, an interesting SCR-based auto-sequential commutated current source inverter (ASCI) can operate with PWM as shown in [72]. However, connecting capacitors between SCRs causes some difficulties during switching at certain values of PF.

In Fig. 6- 3, the HCSC proposed in [63] is presented. This HCSC can operate as rectifier or inverter, but presents some cost concerns due to the use of six SCRs, four IGBTs and seven diodes. The operation principle for this HCSC is based on the fact that both positive and negative currents in each ac-side phase current pass through the same IGBT with different SCRs and diodes. Unfortunately, only one leg operation was tested in [63], their laboratory facilities were not permit complete topology implementation. It was claimed that the traditional SPWM presented in [6] can drive HCSC in Fig. 6- 3. But, one can observe that to have different PF,  $S_a$  should be turn-off to stop current path in SCR1 for certain time period, Before,  $S_a$  turn ON along with SCR4. That mean, the traditional SPWM require turn-on SCR4 to follow turn-off SCR1 cannot be used. And, another modulation scheme should be proposed. Also, the opinion of the author there is that his topology is attractive in certain cases. But, regarding conduction power loss the current is passed in six semiconductor devices (two IGBTs plus two SCRs plus two diodes) instead of four (two IGBTs plus two diodes) in 6-switches CSC. Also, the rated power for IGBTs was considered equal to 6-switches CSC. But, both positive and negative phase currents are passing through the same IGBT in Fig. 6- 3, whiles half of it path in each IGBT in 6-switches CSC. So, this topology requires IGBTs with high current ratings. And, the capital cost saving presenting by reducing the number of switches by three is absorbed by high conducting losses during operation and high rating of the remaining three IGBTs. Note that, the average current flow in the IGBT in one ac-side current line cycle should be considered to select IGBTs rating.

Since then, other topologies have been proposed. *Active* commutation of a three-phase SCR Bridge can be done with a series connected switch presented in Fig. 6- 4,

resulting in a PWM rectifier [73]. Using the same principle and connecting the switch in shunt with the bridge, a hybrid PWM inverter in Fig. 6- 5 is implemented [74], [75]. The limitation of topologies in Fig. 6- 4 and Fig. 6- 5 is that they are unidirectional topologies, the angle between the ac-side current and voltage is limited within  $\pm 30^\circ$  for proper commutation of the SCRs. For instance, in the case of the inverter, turning on the switch outside this range does not divert the dc-side current from the SCR bridge, failing to actively commutate the SCR, since the line voltage at the ac-side of the bridge with conducting SCRs is negative, lower than the short-circuit offered by the switch.

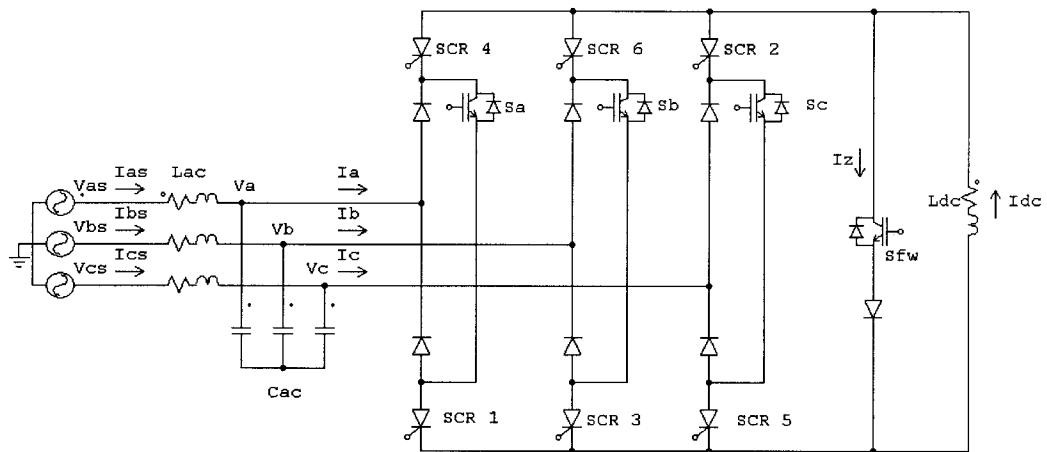


Fig. 6- 3 :- HCSC with six SCRs, four IGBTs and seven diodes.

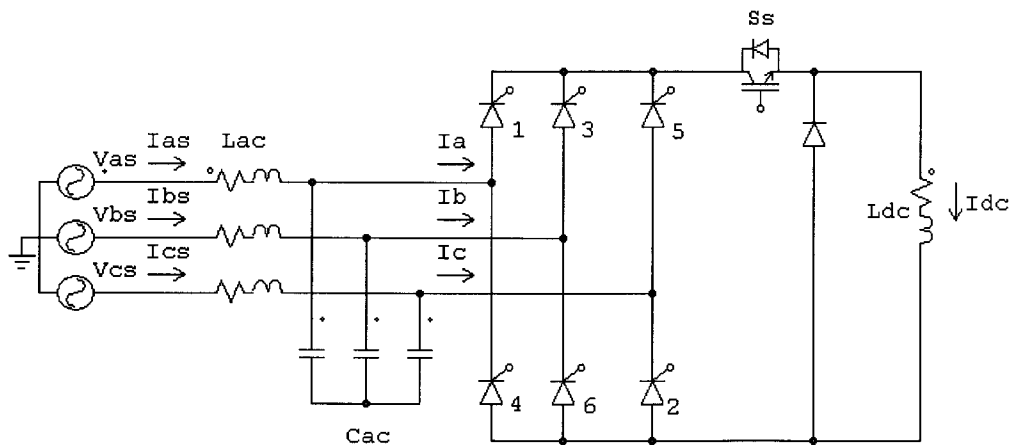


Fig. 6- 4 :- Six SCRs one switch hybrid unidirectional CSR.

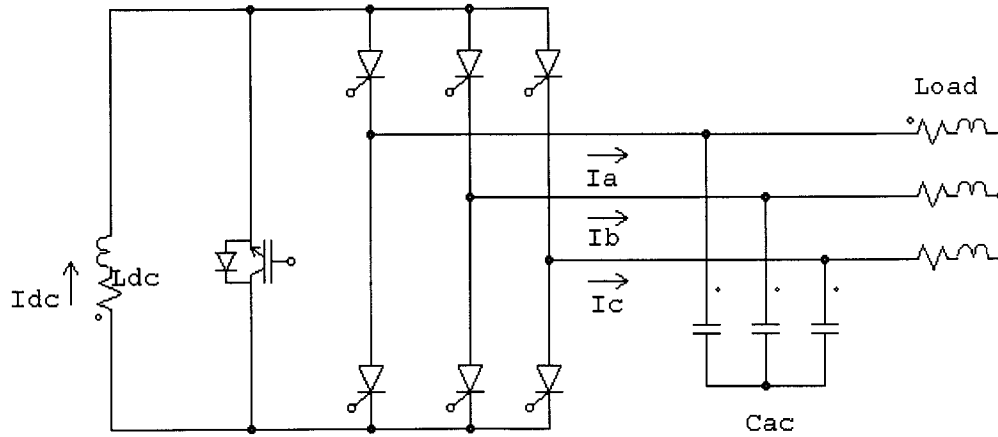


Fig. 6- 5 :- Six SCRs one switch hybrid unidirectional CSI.

### 6.3. PROPOSED HCSC TOPOLOGIES

Two types of hybrid three-phase bi-directional CSCs (HCSC) with features comparable to those of a fully-controlled six IGBTs plus six diodes CSC are presenting in this thesis. They are capable of operating with variable PF when connected to a dc source or load as inverter or rectifier. A potential application for the proposed converter is on STATCOM and super-conducting magnetic energy storage (SMES) systems.

As shown in Fig. 6- 6, the first proposed topology employs an SCR bridge and two switches, and it was presented in [76]. One can consider this topology a combination between Fig. 6- 4 and Fig. 6- 5 topologies which permits multiple PF operation. A diode need to be connected in series with the shunt switch (S7) if the latter does not present reverse voltage blocking capability. The switches operate complementarily and can *actively* commutate the SCR Bridge whatever voltages are present in the ac-side. By opening the series switch (Ss), no current flows through the conducting SCRs which tend to block. During this interval, the shunt switch (S7) free-wheels the dc-side current.



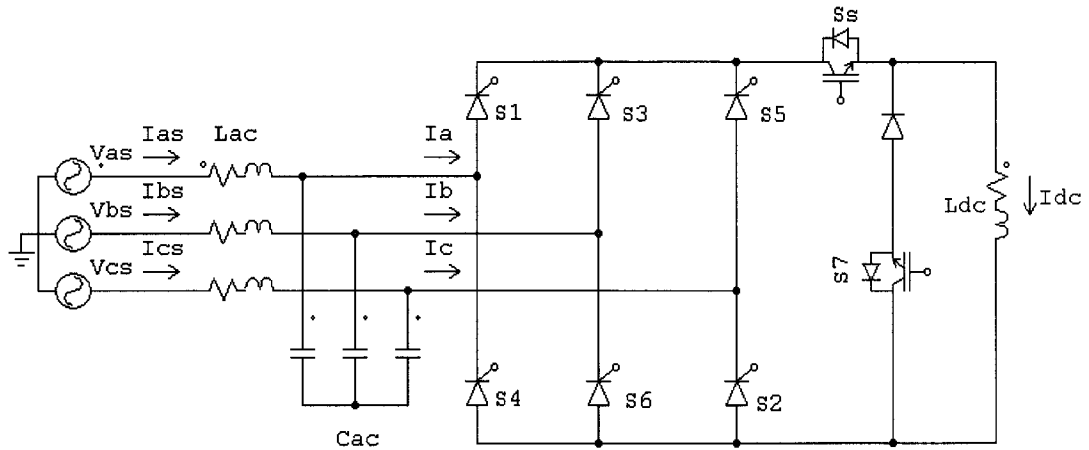


Fig. 6- 6 :- Hybrid bi-directional CSC (HCSC) with an SCR bridge and two IGBTs.

By simple inspection, this topology looks economical. First, there are a lower number of costly IGBTs in addition to SCRs. And, conduction power losses are low due to presence of only three semiconductor devices in the current path (one IGBT and two SCRs). The problem in this topology is that all three phases ac-side current are in one switch which should have high rated current and power loss, what can reduce the actual cost advantage of this topology. Recall that, the relation between the cost and the average current is linear until a certain limit of current where the cost starts to be highly increased with small increment of current [63]. The alternative is connecting in parallel more than one switch with the same rated current of 6-switches topology. Since the current will be tripled, at least three IGBTs are required instead of  $S_s$ . And the topology will have six SCRs and four IGBTs. The procedure for connecting IGBTs in parallel was presented in [77]. Similar problem appears also in topologies of Fig. 6- 3, Fig. 6- 4 and Fig. 6- 5 and nearly all previously proposed HCSCs. Also, as we will see later, freewheeling should appear in  $S_7$  in all sectors, which loads  $S_7$  parallel switch as well and two IGBTs are required in  $S_7$  instead of one, current wise.

The second HCSC, which is found to be a real cost effective solution, is a HCSC that employs three SCRs and four IGBTs in Fig. 6- 7. It also presents features comparable to the fully controllable CSC and was first presented in [78]. It employs a higher number of IGBTs than the previous one, but each conduct only half phase current or less. So, they can in principle have the same current ratings of IGBTs in the six IGBTs based CSC, current pass in each IGBT is less than the current in 6-switches CSC. Also, freewheeling across  $S_7$  in half number of sectors can be achieved by adjusting a suitable SVM technique, described later on. Also, conduction power losses are low due to the existence of three semiconductor devices in the current path. Bridge IGBTs can actively commutate the SCRs whatever voltage polarity is presented in the ac-side of the bridge. If they are turned-off, no current flows through the SCRs which tend to turn-off. The fourth IGBT connected in shunt to the dc-side, is used for free-wheeling the dc-current. Cost issues will be presented in chapter nine in details.

The inherent commutation constraints of the SCRs should be taken into consideration in the selection of a suitable SVM technique, which was not considered in previous research for HCSCs topologies. Usually they mention that, traditional SPWM or SVM can be used [63], [73] - [75], which should be investigated. Comparisons with the fully controllable CSC also should be provided for a fair assessment of the potential of the proposed HCSCs. This comparison should cover both performance and cost aspects, both have not been taken into consideration together in previous researches for other HCSC topologies. Previous HCSC topologies could not compete with 6-switches one in both aspects, while three SCRs four IGBTs has potential to do so. Also, the theoretical

analysis should be verified by means of simulations and experimental verification, not one leg experimental verification as it is usually the case in [63] and earlier researches.

SCRs in the HCSC topologies need time to turn-off. This time may be different than  $t_q$  provided in datasheets. No scenarios that can result in forward biasing the SCRs before it regains its forward blocking capability are allowed. That gives a restriction in switching frequency. And, the high switching frequency in [73], [74] should be questioned. In previous researches it was difficult to implement HCSC topologies for many reasons. It is not a commercial converter like traditional VSC or CSC. A combination of SCRs, diodes and IGBTs should, nonetheless, be viable. A gate drive gives PWM pulse to SCRs is required. Recall that SCRs are usually employed in phase controlled converters and PWM drives for SCRs are not widely available.

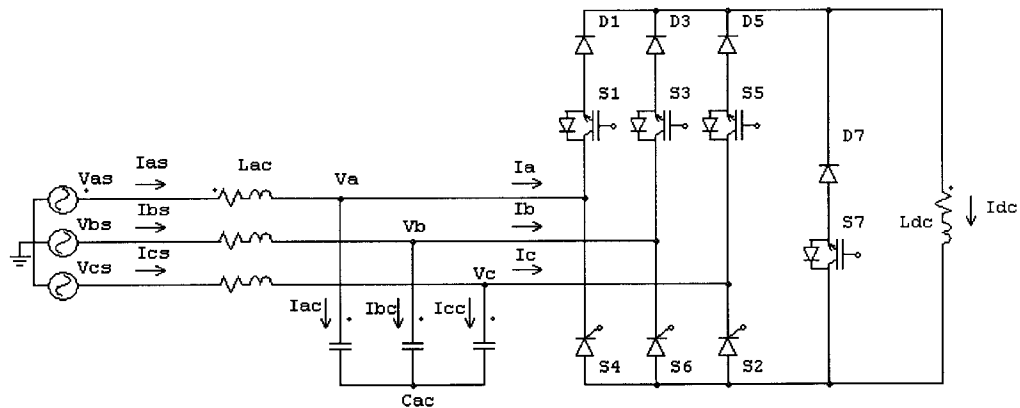


Fig. 6- 7 :- Hybrid bi-directional CSC (HCSC) with three SCRs and four IGBTs.

## 6.4. COMMUTATION IN HCSC TOPOLOGIES

The main challenge in both of the proposed HCSC is the commutation of the SCRs. Although it is an important issue, attention was not given to this issue in the previous HCSCs topologies research. In six SCRs two IGBTs topology the commutation

from one SCR to the other in the same group is complicated (upper or lower). While in three SCRs four IGBTs topology the commutation from one SCR to the other in the lower group is complicated, while it is quite simple for the upper group.

The commutation of the *least* forward biased SCR to another one is straightforward, that can be achieved directly by turning on the more forward biased SCR. However, one also has to consider the transition to a free-wheeling state and the commutation of the *most* forward biased SCR. The first can be accomplished by turning off the IGBT conducting the current along with SCRs and turn on the freewheeling one in both topologies or by turning on the IGBT of the same phase of the conducting SCR and blocking the IGBT that was previously on in three SCR four IGBTs topology. However, for blocking the most forward biased SCR one has to open the conducting IGBT and turn on the free-wheeling IGBT (S7) to provide a path for the dc current, and keep it on until the SCR recovers its direct voltage blocking capability. Then, any new combination of SCRs can be fired along with Ss in the six SCR two IGBTs topology. And, any of the two other SCRs will conduct current, if fired along with any of the IGBTs of the bridge when S7 is turned off in three SCRs four IGBTs topology.

Issues need to be addressed are not only if SCRs will be turned-off when the IGBTs conducted current along with is turned-off, but also the time interval required for an SCR to regain forward voltage blocking capability and its relation with  $t_q$  (SCR turn off time) provided in the datasheets when no reverse voltage is applied across it after its main current goes to zero. Experimental work in [73], [74] was able to prove that SCR will turn-off if an IGBT conducting current along with this SCR is turned-off. That is, if the upper bridge IGBT conducting current is turned-off while S7 is turned-on in Fig. 6- 7.

Then, the lower SCR conducting current will turn-off. Unfortunately, those references did not give the time required for SCR to turn-off. Also, experimental work carried out in [63] showing that the minimum turn-off time ( $t_{off.min}$ ) of an SCR that is actively commutated by diverting its current and without being reverse biased is typically around two times the value of  $t_q$  provided in the datasheet for rated current operation. No more references investigate this issue, because it is a special issue related to connect SCRs in certain HCSC topologies which is rare in general. Those claims should be investigated before going farther in the proposed HCSC topologies issues.

## **6.5. EXPERIMENTAL VERIFICATION OF THE COMMUTATION IN HCSC**

As just mentioned, the operation success of the HCSCs in Fig. 6- 6 and Fig. 6- 7 is based on the principle that an SCR can be actively commutated by opening a switch in the current path, the SCR should regain its forward blocking capabilities before being forward biased again. If the converter is operated with variable PF, one cannot guarantee the reverse bias of the SCRs after their main currents go to zero and the minimum off-times used in the phase-controlled CSCs do not guarantee safe commutation. This is an atypical operating condition for SCRs and there is no data sheets information assist in the definition of a “no reverse biased”,  $t_{off.min}$ . Therefore, an experiment to obtain the critical turn-off time of an SCR in the proposed HCSCs is used.

Fig. 6- 8 is presenting a circuit emulates an active commutation of the SCRs, during HCSC operation. Let’s describe how this circuit emulates three SCRs four IGBTs topology, similar emulation can be done for six SCRs two IGBTs topology. It reproduces

the operating condition when an SCR (from the lower group) and an IGBT (from the upper group) conduct the dc-side current until the IGBT is opened (turned off). The diode free wheels the dc-side current as if it is the free-wheeling IGBT ( $S_7$ ) of Fig. 6- 7.  $V_{dc}$  represents the line to line voltage of the ac system. The worst case for the active commutation is when  $V_{dc}$  is positive with peak line to line voltage.

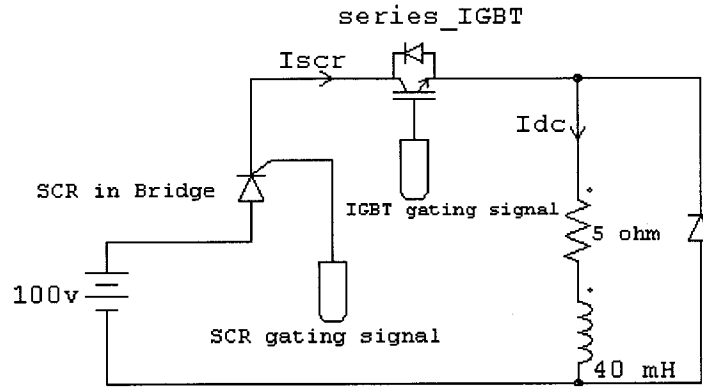


Fig. 6- 8 :- Experimental test verifies the active commutation feasibility.

The gating signals used in the experimental test for the IGBT and SCR are as in Fig. 6- 9. The SCR and the IGBT are kept on for a period of time ( $t_{on}$ ). For given values of  $V_{dc}$  and load one can impose a desired load current by controlling the duty cycle ( $t_{on}/T$ ). Then, the IGBT is turned off and kept off for a period ( $t_x$ ) after which it is turned on again without firing the SCR. A simple logic circuit using CMOS-IC from 4000 series is generating the required electronic gating pulses. Drive circuits will be presented for complete system implementation in the next chapter.

During the test, if  $t_x$  is long enough for the SCR to regain its forward voltage blocking capability, there will be no flow of current from the dc source to the load until both SCR and IGBT are turned on simultaneously. During the test, the segment  $t_x$  is reduced until an SCR commutation failure occurs defining a minimum  $t_{off}$  time for the

SCRs ( $t_{off,min}$ ). The test circuit is implemented with 800V/50A inverter-grade SCR with a datasheet  $t_q=20\mu s$ .  $V_{dc}=100V$  in this test, nearly the line voltage of the HCSC prototype used in the following chapters.

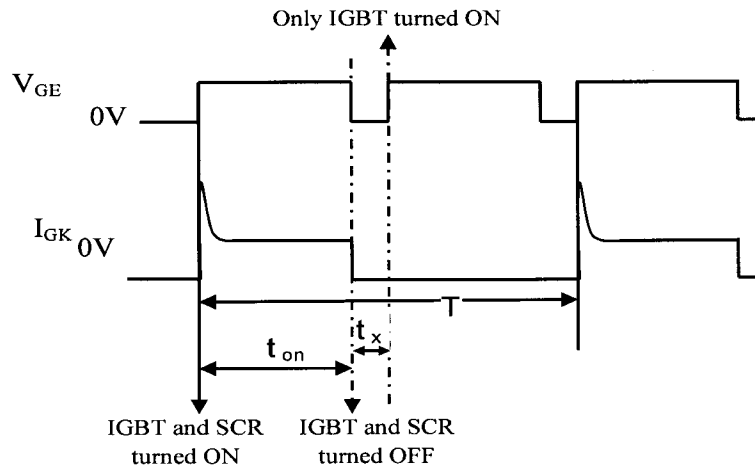


Fig. 6- 9 :- IGBT and SCR gate signals in the active commutation feasibility test.

Fig. 6- 10 presents the waveforms of the current through the SCR (top), SCR gating signal (middle) and IGBT gating signal (bottom) for  $t_x = 10\mu s$ . The duty cycle of the gating signals of the SCR and the IGBT is such that the load current ( $I_{dc}$ ) is adjusted to be 8A, without commutation failure. No current circulates through the SCR if it is not fired, and  $10\mu s$  is enough for SCR to regain forward voltage blocking capability for a current of 8A. On the other hand, Fig. 6- 11 presents the same waveforms for a different current (duty cycle). There one can clearly see that the SCR conducted without being fired when the IGBT is turned on after  $15.5\mu s$  and for a current of 15A. Note, the scales of Fig. 6- 10 and Fig. 6- 11 are different for trace 2.

Table 6- 1 illustrates the recorded values of  $t_x$  for different values of  $I_{dc}$ , up to 25A. There one sees that  $t_x$  increases with  $I_{dc}$ .

For estimating the value of  $t_x$  at the rated current (50A), an empirical formula of  $y$

$\{t_x = (0.85 I_{dc} + 3.2) \mu s\}$  is generated from

Table 6- 1. For  $I_{dc} = 50A$ , the formula gives  $t_x=45.7\mu s = 2.28 t_q$ . Thus, a factor of 2.5 is used to obtain the minimum turn off time for the SCR to commutate safely without reverse voltage at its rated current with respect to its datasheet  $t_q$ , as shown in (6- 1).

$$t_{off.min} = 2.5 t_q \quad (6- 1)$$

Therefore, for an inverter grade SCR with 2.5kV/1kA voltage and current ratings and  $t_q = 20\mu s$ , the dc current should be free-wheeled through S7 for a minimum interval of  $50\mu s$  before any other combination of SCR and IGBT is turned on. This requirement will limit the maximum gain of the CSC and its switching frequency to a few k Hz.

TABLE 6- 1 :- EXPERIMENTAL RELATION BETWEEN THE SCR CURRENT ( $I_{dc}$ ) AND THE MINIMUM TURN OFF TIME ( $t_x$ )

$I_{dc}$ (A)	5	8	10	15	20	25
$t_x$ ( $\mu s$ )	7.7	9.8	11.5	16	20	24.5

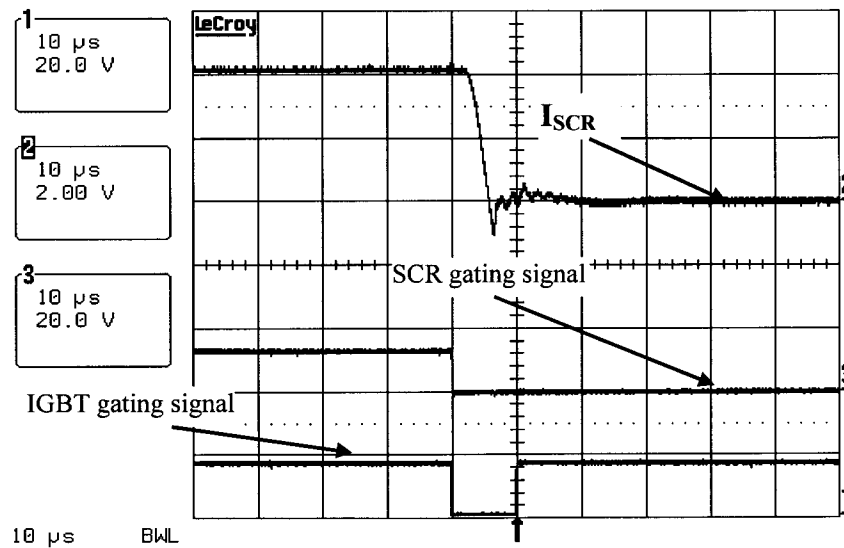


Fig. 6- 10 :- Successful commutation in the active commutation test,  $I_{dc} = 8A$ ,  $t_x = 10\mu s$ .



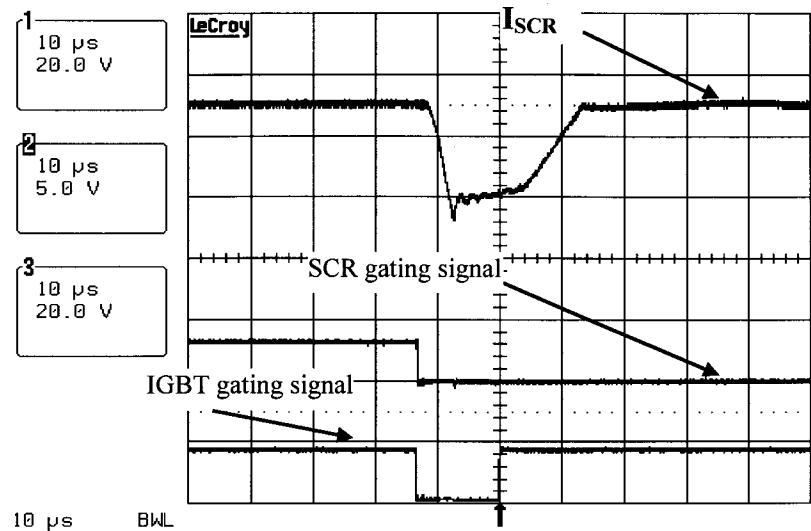


Fig. 6- 11 :- Commutation failure in the active commutation test,  $I_{dc} = 15 \text{ A}$ ,  $t_x = 15.5 \mu s$ .

## 6.6. CONCLUSION

A review in hybrid CSCs (HCSCs) topologies was carried out. Previously one thesis discussed those topologies and come up with one which should be better [63]. Since then other topologies have been presented. Two types of HCSCs are proposed in this thesis. An experimental test circuit was implemented to prove the feasibility of the proposed topologies. Proposed HCSC topologies feasibility, possible modulation techniques, economic analysis, theoretical analysis, simulation results and experimental results aspects will be presented in the remainder of the thesis.

An investigation proves that one of the proposed topologies, with three SCRs and four IGBTs, is presenting a more cost effecting solution than the other, with six SCRs and two IGBTs. That resulted from the current pass in each IGBT per line cycle. Consequentially, three SCRs and four IGBTs topology will be investigated in theoretical, simulation and experimental issues. And, six SCRs and two IGBTs will be investigated theoretically.

## CHAPTER 7

### 7. HARD-SWITCHING SVM FOR HCSC

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#### 7.1. 6-SWITCHES SVM-CSC USED FOR COMPARISON

In chapter one, the SVM scheme was used for fully controllable 6-switches CSC. There a vector rotates counter-clockwise with a constant angular frequency  $\omega$  presents a constant magnitude for a set of balanced sinusoidal currents,  $i_a$ ,  $i_b$  and  $i_c$ . Fig. 1- 3 showed the complex plane with an arbitrary reference SV ( $I_n$ ), six active SVs ( $I_1$  to  $I_6$ ) and three zero SVs ( $I_7$  to  $I_9$ ) and the definition of the 6-sectors of the complex plane.  $m_a = \frac{\|I_n\|}{\|I_1\|}$ , which is ( $0 \leq m_a \leq 1$ ) for 6-switches SVM-CSC, can be replicated with minimum switching frequency by operating the CSC with the nearest active states ( $I_i$  and  $I_{i+1}$ ) and one specific zero state depending on the sector where  $I_n$  is located at a certain sample instant [6]. This approach for choosing the zero state also allows the short circuit (overlap) pulses to be distributed symmetrically through all switches. The continuous states ON times ( $t_i$ ,  $t_{i+1}$  and  $t_z$ ) are usually calculated as a function of the  $m_a$  and  $\theta$ , the angle of  $I_n$  in a given sector ( $0 < \theta < 60$ ). Usually over modulation in CSC is not employed because it generates LOH [79].

The simple SVM sequence in Fig. 7- 1 with SAm is used for comparison.  $N_{CS}$  should be an integer for synchronized SVM. Unlike part one of the thesis where  $N_{CS} = 6$ , here  $N_{CS} = 3$  is selected to simplify description, specify LOH generation reasons in HCSC, give acceptable hardware accuracy in the experimental set-up and give high gain ( $m_{a,max}$ ) in HCSCs. Also, it is suitable for HCSC which require LSF. When,  $f_{ac} = 60$  Hz

and  $N_{CS} = 3$  the dominant harmonics appears at  $6 N_{CS} \pm 1pu$  (17pu and 19pu) with  $f_{cycle} = 1080Hz$ . That mean, Fig. 1- 3 can be redrawn in Fig. 7- 2. There the three SVM cycles representing sectors five are illustrated.

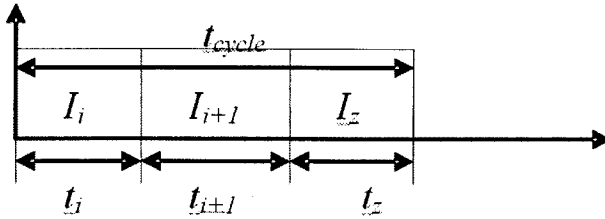


Fig. 7- 1 :- Traditional CSC states sequence used in part two of the thesis.

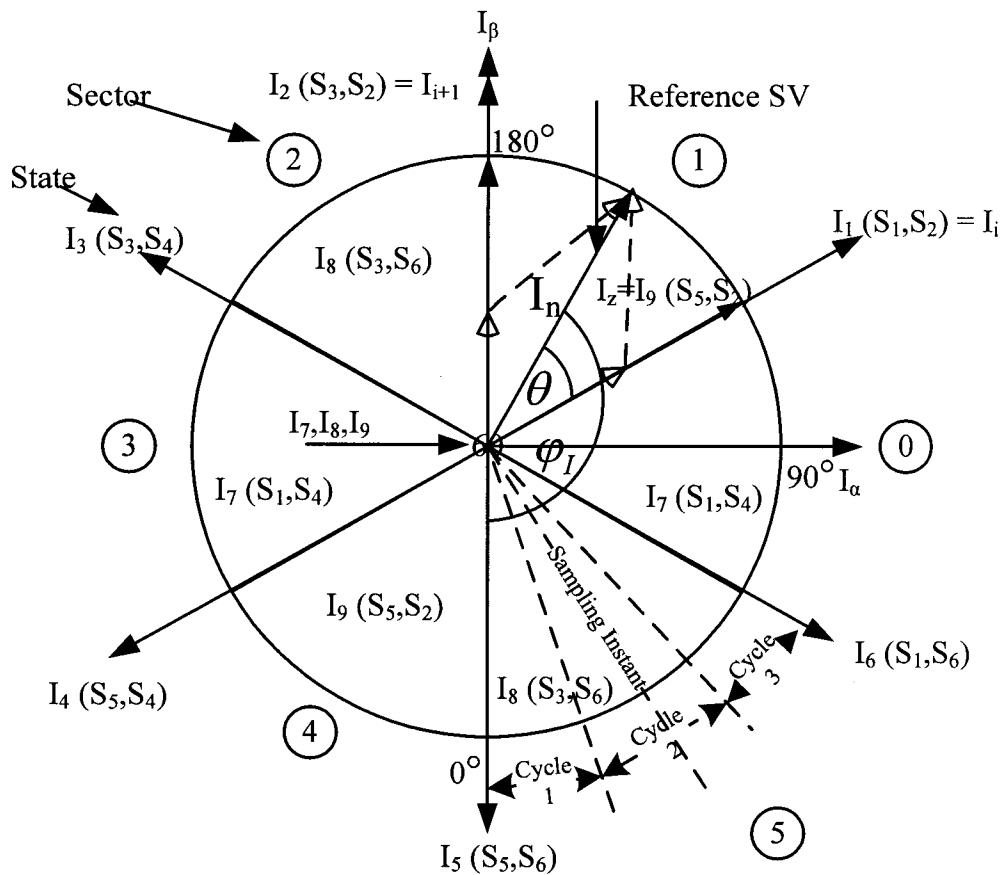


Fig. 7- 2 :- Definition of the sectors (0 to 5), states ( $I_1$  to  $I_9$ ), and the switches which are ON in each state in traditional 6-switches SVM-CSC.

## 7.2. HS-SVM PRINCIPLES FOR THE THREE SCRs AND FOUR IGBTs HCSC

The particular features of the proposed three SCRs four IGBTs HCSC have to be considered when designing a suitable SVM scheme for HCSC. One needs to choose an ideal sequence of states in SVM, define how to implement the zero state and select  $t_{\text{cycle}}$ . This should be done to achieve safe commutation of SCRs, reduce switching frequency and obtain symmetrical pulsed ac-side currents for reducing the magnitudes of LOH.

In this HCSC the bridge bottom switches are replaced by SCRs. The topology is asymmetrical, meaning that all even switches are SCRs while all odd switches are IGBTs with series diode. Therefore, S2, S4, and S6 are hereinafter considered SCRs. There is an additional shunt connected IGBT (S7) which provides means for free-wheeling the dc-side current and realizing an extra zero state ( $I_{10}$ ). Fig. 7- 3 is presenting the definition of sectors, states, ON switches in each state and the reference current vector for this HCSC. The switching functions are presented in Table 7- 1.

If this HCSC is required to operate with variable PF, the commutation of a more forward biased SCR and the firing of a less forward biased SCR is necessary. Since the difficulty in commutating an SCR depends on its forward biasing *degree*, the transitions from one state to another in a given sector and from a sector to other present different challenges for the SVM implementation. An SCR is the common active states switch in odd sectors, while an IGBT is the common active states switch in even sectors as shown in Table 7- 1 and Fig. 7- 3. The transitions from one state to another in odd sectors is relatively simple, requiring the commutation of IGBTs, but is complicated in even sectors, since a *more* forward biased SCR might need to be actively commutated.

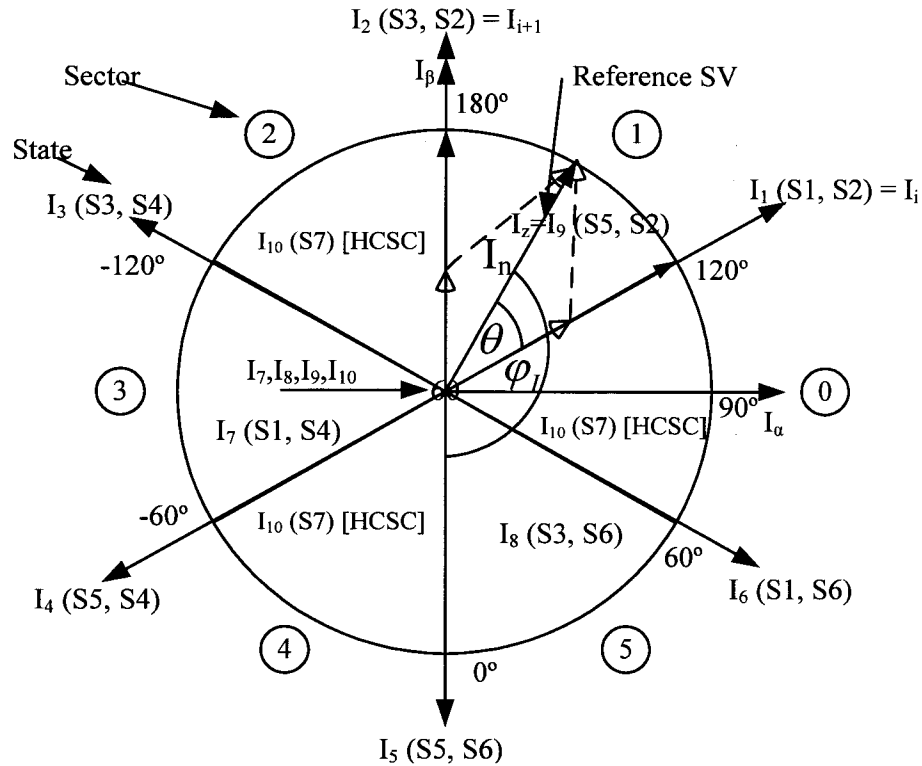


Fig. 7- 3 :- Definition of the sectors (0 to 5), states ( $I_1$  to  $I_{10}$ ), ON switches in each state and the reference current vector for three SCRs and four IGBTs HCSC topology.

The SVM scheme used for fully controllable CSCs, sequence of three segments and zero state implemented in the leg of the switch common to the active states, can be readily used in the odd sectors of HCSC. Where, the zero states  $I_9$ ,  $I_7$  and  $I_8$  are used in sectors 1, 3 and 5, respectively. There, all transitions are accomplished by switching IGBTs. On the other hand, this is not possible for the even sectors where the transition from one active state to another might require the commutation of a more forward biased SCR. This can only be done with an active commutation, by turning off the IGBT common to the two active states. In such a case, the free-wheeling IGBT must be turned on to provide a path for the dc-side current, resulting in the implementation of a mandatory zero state.

TABLE 7- 1 :- STATES REALIZATIONS AND SWITCHING FUNCTIONS OF THREE SCRS FOUR IGBTs HCSC

States	Lower on Device	Upper on Device	$I_a/I_{dc}$	$I_b/I_{dc}$	$I_c/I_{dc}$
1	S2	S1	1	0	-1
2	S2	S3	0	1	-1
3	S4	S3	-1	1	0
4	S4	S5	-1	0	1
5	S6	S5	0	-1	1
6	S6	S1	1	-1	0
7	S4	S1	0	0	0
8	S6	S3	0	0	0
9	S2	S5	0	0	0
10	S7	S7	0	0	0

Active states comprise an SCR and an IGBT on. Transitions from one active state to the next, using the nearest active states to the reference vector, require the commutation of an SCR in even sectors. This might be, or not, the most forward biased one at that moment. To guarantee safe commutation of the SCR, it should be actively commutated. This requires the active states to be separated by a zero state, what implies the use of a sequence of states with four segments shown in Fig. 7- 4.

To avoid commutation failures in even sectors, the zero state is implemented with  $I_{10}$  and separates the active states. In the odd sectors, an SCR is the common switch to the two nearest active states and does not need to be turned-off. So, the zero state is implemented using that SCR with states  $I_7$ - $I_9$  to reduce the switching stress on the S7. For

the sake of symmetry, what reduces the LOHs in the ac-side currents, the four segment sequence of states is used in all sectors. It is worth mentioning that, the SCR in the last zero state of an even sector is the one to be fired next in the following sector and no commutation problems arise with sectors transitions. When this logic is implemented with SVM, it is called by the author hard switching SVM (HS-SVM).

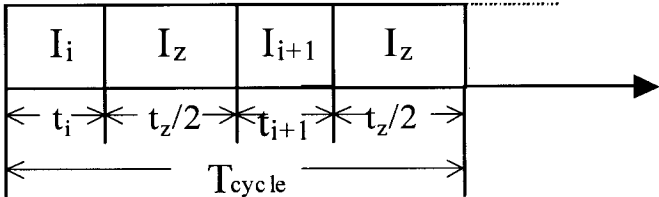


Fig. 7- 4 :- Sequence of states for operation with active commutation (HS-SVM).

**7.3. HS-SVM PRINCIPLES FOR THE SIX SCRS AND TWO IGBTs**

**HCSC**

In six SCRs two IGBTs HCSC, bridge IGBTs are replaced by SCRs. Therefore, bridge SCRs are hereinafter considered SCRs after S<sub>s</sub>. There is no possibility of using the bridge for freewheeling. A new freewheeling state I<sub>7</sub> using S<sub>7</sub> is generated. Fig. 7- 5 presents the definition of the sectors, states, on switches in each state and the reference current vector. The switching functions are presented in Table 7- 2.

Fig. 7- 4 sequence is used here. There is only one way to achieve the zero state using I<sub>7</sub> (S<sub>7</sub>). This zero state separates the active states to give an opportunity to bridge SCRs to turn off. Each zero state should be larger than t<sub>off\_min</sub> for SCRs. This topology is more costly than previous one, because triple rated current appears in S<sub>s</sub> and double appears in S<sub>p</sub>. Independent on the way of implementing states, if the same states sequence is used in both topologies, they ac-side and dc-side current waveforms will be

similar. More specification related to this topology is in [76]. The rest of this thesis will deal with the three SCR's four IGBT's topology which seems more promising.

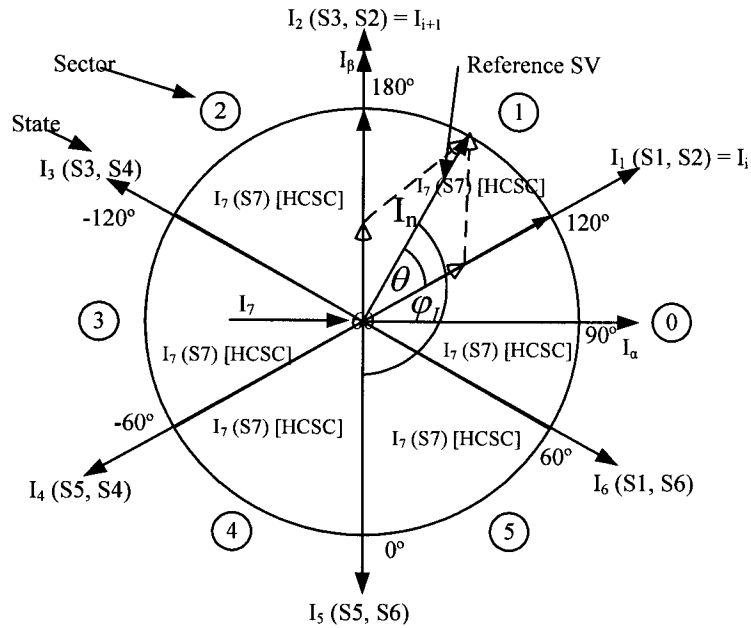


Fig. 7- 5 :- Definition of the sectors (0 to 5), states ( $I_1$  to  $I_7$ ), switches on in each state and the reference current vector for six SCRs and two IGBTs HCSC topology.

TABLE 7- 2 :- STATES, REALIZATIONS AND SWITCHING FUNCTIONS OF SIX SCRs TWO IGBTs HCSC

States	Lower on Device	Upper on Device	$I_a/I_{dc}$	$I_b/I_{dc}$	$I_c/I_{dc}$
1	S2	S1	1	0	-1
2	S2	S3	0	1	-1
3	S4	S3	-1	1	0
4	S4	S5	-1	0	1
5	S6	S5	0	-1	1
6	S6	S1	1	-1	0
7	S7	S7	0	0	0



## 7.4. AVERAGE SWITCHING FREQUENCY OF THE SEMICONDUCTORS

SVM for CSC is not a typical type of PWM. So, a switch might be on for an entire sector, idle in other and switching in others. This section calculates the number of pulses for each switch per line cycle ( $N_p$ ) to obtain an average switching frequency in HCSC with HS-SVM and in 6-switches SVM-CSC. The later is used for comparison.

In the SVM-CSC, a sequence of three segments is used in each SVM cycles. An odd (even) IGBT will be either on or switching when its line current is positive (negative). It will be on for an entire sector when it is common to all states. And, switching in neighboring sectors with  $N_{CS}$  pulses per sector when it belongs to one active state. Besides, it will be switching in another sector when implementing a zero state. Since the first state of the sector follows where a switch is always on includes that switch, the number of pulses per line cycle is  $N_{P-IGBT} = 3N_{CS}$ . Fig. 7- 6 shows the gating signals generated for upper switches in SVM-CSC when  $m_a = 0.7$  and  $N_{CS} = 3$ . There all switches gating signals presenting the same shape with 9 pulses per ac-side current line cycle.

In three SCRs four IGBTs HCSC, the selected sequence contains four segments, two of which correspond to a zero state. These are realized through S7 in the odd sectors and though the bridge SCR that contains the common active states in even sectors. Since SCRs and IGBTs are controlled in different ways, they present different gating patterns.

Starting with SCRs, each will be fired when the current in its phase is positive. Therefore, it will be idle for three sectors. Besides, it will be on all the time during an odd sector when it is the common device to all states. In the two neighboring sectors, this SCR will be fired once per SVM cycle because it belongs to one of the active states. As

for SVM-CSC, the first state of the sector follows where a SCR is always on includes that SCR. The number of pulses per line cycle is  $N_{P\_SCR} = 2 N_{CS}$ , as shown in Fig. 7- 7.

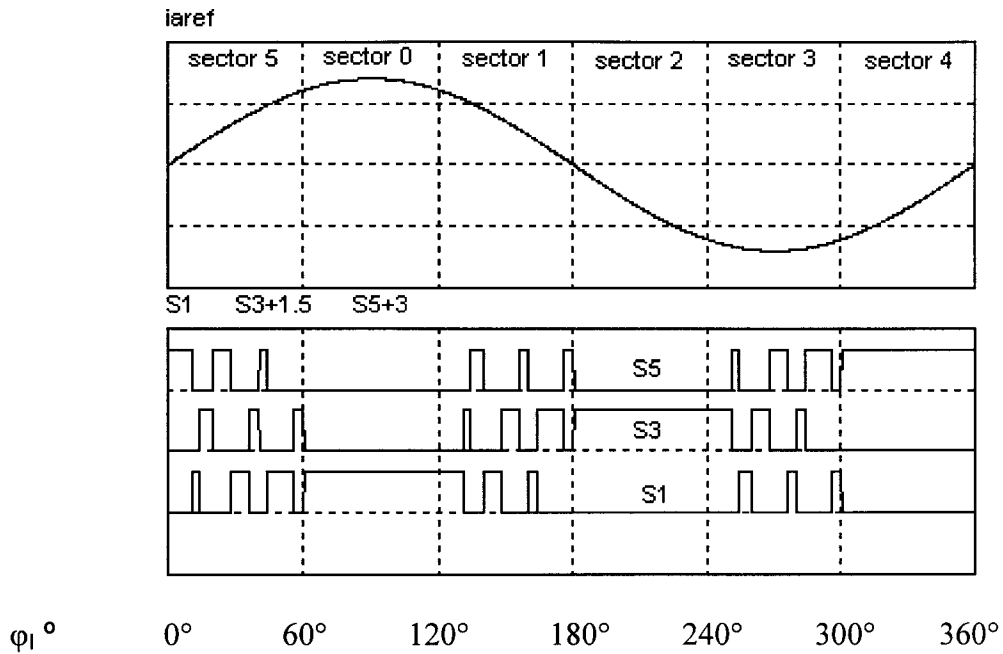


Fig. 7- 6 :- Gating pattern for upper IGBTs in 6-switches SVM-CSC when  $m_a = 0.7$ .

For IGBTs, HS-SVM presents two zero state segments, realized through S7 in even sectors and through the bridge devices in odd sectors. Therefore, S7 remains idle for three sectors and switches with  $2N_{CS}$  pulses in each of three sectors, for a total of  $6N_{CS}$  pulses per line cycle,  $N_{P\_FW\_IGBT} = 6N_{CS}$  as shown in Fig. 7- 8.

Regarding the bridge IGBTs, they switch in four sectors. Three sectors where the desired line currents in their phases present the appropriate direction and in another, an odd sector, to realize a zero state. In the latter case, they are switching with  $2N_{CS}$  pulses because there are two zero states in HS-SVM. They are also switch at this rate, in the even sector where they are the common devices to the two active states because they need to actively commutate an SCR. In two sectors where they belong to one of the two

active states, they switch only  $N_{CS}$  pulses. As a result, each bridge IGBT presents  $6 N_{CS}$  pulses per line cycle,  $N_{P\_bridge\_IGBT} = 6N_{CS}$  as shown in Fig. 7- 8.

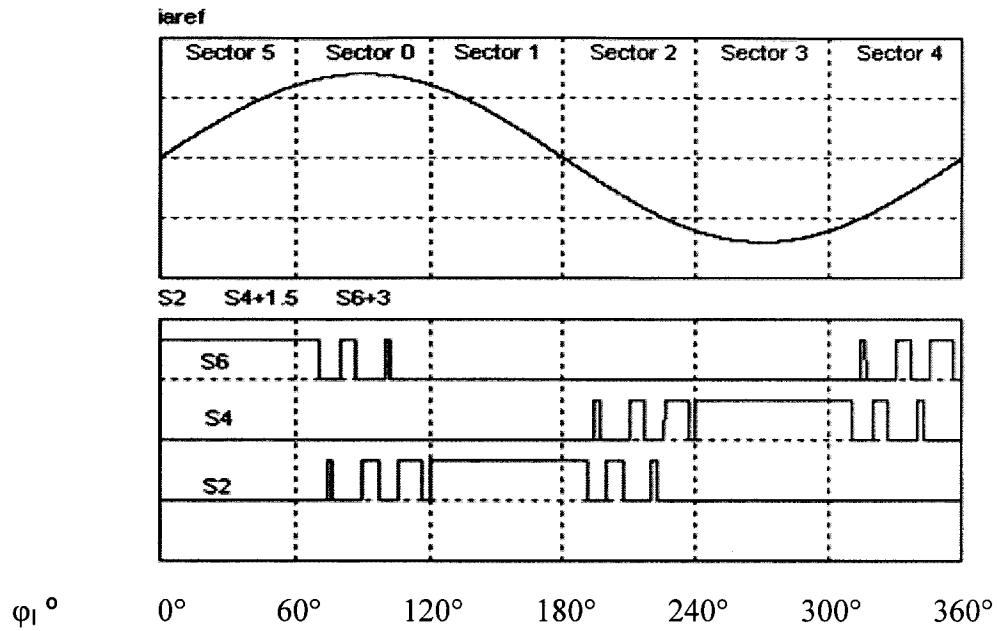


Fig. 7- 7 :- SCRs gating pattern in HCSC with HS-SVM when  $m_a = 0.7$  and  $N_{CS} = 3$ .

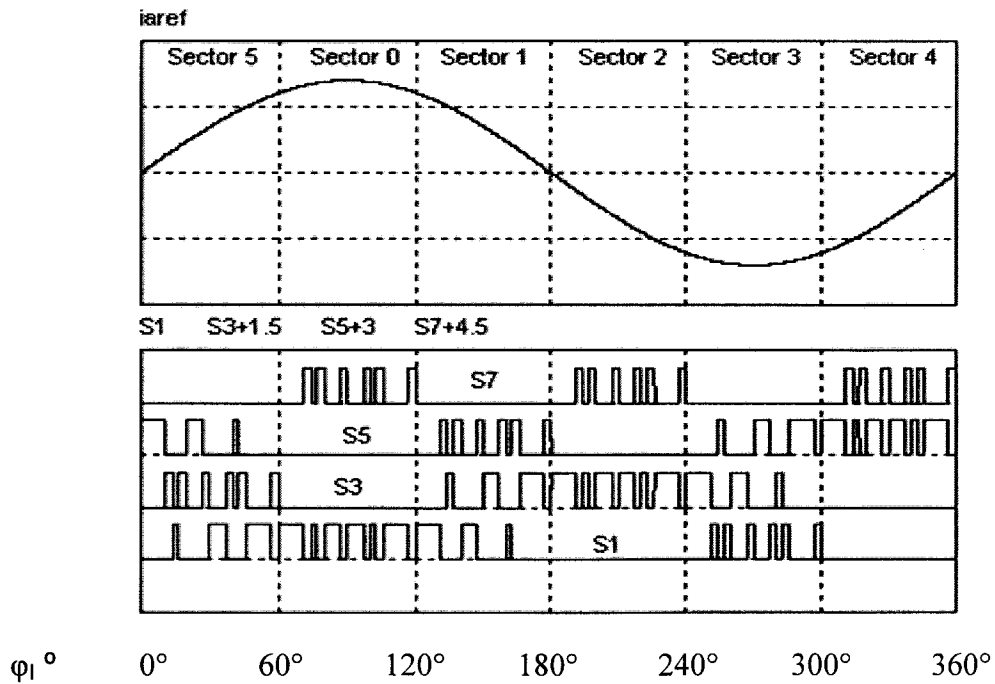


Fig. 7- 8 :- IGBTs gating pattern in HCSC with HS-SVM when  $m_a = 0.7$  and  $N_{CS} = 3$ .

Comparing the total number of pulses in HCSC with HS-SVM to the fully controllable one, in the first case there are  $24N_{CS}$  for IGBTs and  $6N_{CS}$  for SCRs and  $18N_{CS}$  for IGBTs in the second. Besides, the ac-side line cycle switching frequency of the IGBTs in the HCSC is twice as high as that of the IGBTs in SVM-CSC for the same  $N_{CS}$ .

## 7.5. LIMITATIONS ON THE MODULATION INDEX ( $M_A$ )

It was mentioned in the previous sections that a reference vector with  $m_a = \|\mathbf{I}_n\| \leq 1$  can be replicated by a combination of three states ( $I_i$ ,  $I_{i+1}$  and  $I_z$ ) used during given intervals ( $t_i$ ,  $t_{i+1}$  and  $t_z$ ). However, since the zero state has to last a minimum time interval to guarantee the safe commutation of the SCRs ( $t_{z,min}$ ), there will be a maximum possible value for the modulation index ( $m_{a,max}$ ) in HCSC. In HS-SVM the calculated duration of the zero state is split in two segments, and each segment should be long enough to allow the SCRs to recover their forward voltage blocking capability. So, the least zero state time period can be calculated in (7- 1). Substituting (7- 1) in (6- 1) resulted (7- 2). Also, substituting (1- 4), (1- 5) and (7- 2) in (1- 6) resulted in (7- 3). Then, the  $m_a$  restriction is found in (7- 4). And finally, the  $m_{a,max}$  occurs for  $\theta = \pi/6$ , yielding (7- 5).

$$t_z \geq 2 t_{off\_min} \quad (7- 1)$$

$$t_z \geq 5 t_q \quad (7- 2)$$

$$t_{cycle} - t_{cycle} m_a \sin\left(\frac{\pi}{3} - \theta\right) - t_{cycle} m_a \sin(\theta) \geq 5 t_q \quad (7- 3)$$

$$m_a \leq \frac{1 - 5 t_q t_{cycle}}{\sin\left(\frac{\pi}{3} - \theta\right) + \sin(\theta)} \quad (7- 4)$$

$$m_{a,max} = 1 - 5 t_q t_{cycle} \quad (7- 5)$$

Inverter grade power SCRs in the market today present  $t_q$  in the range of  $20\mu\text{s}$  to  $60\mu\text{s}$ , for conventional SCRs  $t_q$  lies in the ranges more than  $500\mu\text{s}$ . Fig. 7- 9 is showing how  $m_{a,\text{max}}$  varies with  $f_{\text{cycle}}$  for typical values of  $t_q$  for inverter grade SCRs. One can see that for a given value of  $t_q$ , the  $m_{a,\text{max}}$  decreases as  $f_{\text{cycle}}$  increases. On the other hand, the frequency of the resulting harmonics in the ac-side current of the HCSC should increase thus reducing the size of the required ac-side filter. Therefore, the design will require a compromise between the  $m_{a,\text{max}}$  and the size of the ac-side filter. The case presented here is for SVM with three cycles per sector ( $f_{\text{cycle}} = 1080 \text{ Hz}$ ) and  $t_{\text{off},\text{min}} = 50\mu\text{s}$  ( $k = 2.5$  and  $t_q = 20\mu\text{s}$ ), that give  $m_{a,\text{max}} = 0.892$ .

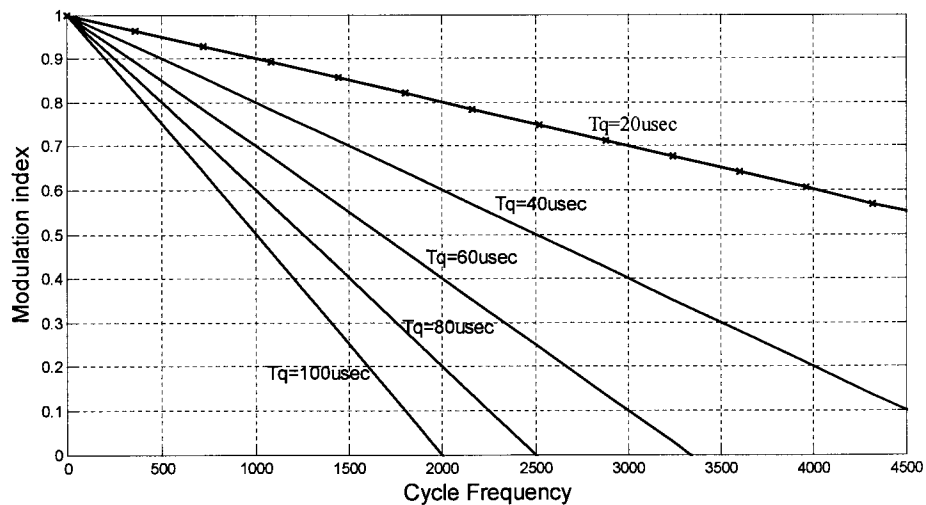


Fig. 7- 9 :-  $m_{a,\text{max}}$  for HCSC as a function of  $f_{\text{cycle}}$  at different SCR turn off time ( $t_q$ ).

## 7.6. EXPERIMENTAL SETUP

A laboratory prototype was built to verify the theoretical analysis and demonstrate the feasibility of the HCSC with three SCRs and four IGBTs. Fig. 7- 10 shows semiconductor devices and their drives in the HCSC. Also, Fig. 7- 11 shows a complete view for the HCSC. The HCSC power circuit was implemented with the Westcode

P0128SH10D SCRs and the Powerex CM100DU-24NFH IGBTs. The SCRs are driven by three (one channel) APS BAP-1106 boards, which allow PWM operation, while the IGBTs were driven by two (two channel) Powerex BG2C boards. The snubbers, which have a significant impact on the commutations, were designed following the approach described in [63].

The modulation techniques were implemented using discrete Z transform blocks in SIMULINK which were then converted to DSP code and used in a dSPACE (DS-1103) development kit.  $N_{CS} = 3$  was selected, which gives good resolution for a sampling step of  $25\mu s$  when UPF is adjusted between  $I_a$  and  $V_a$ , keeping the magnitude of the non-characteristic LOH at acceptable values. The 60 Hz three-phase input voltage was set at 104V, line-to-line (60V-phase). The input filter consists of an  $L = 8mH$  in series with  $R = 0.6 \Omega$  and  $C = 100\mu F$ . The dc-side impedance is composed of  $L = 40mH$  in series with  $R = 10\Omega$ . LEM current sensors (1:18) were used to measure the grid and converter currents while a LEM voltage sensor (1:300) was used to measure the filter capacitor voltage.

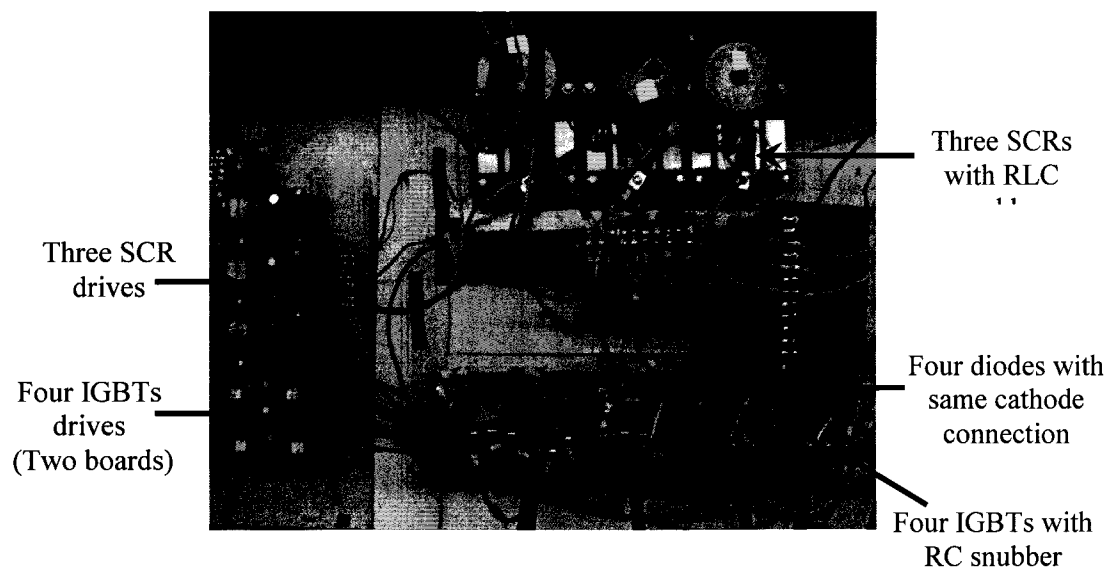


Fig. 7- 10 :- Semiconductors and their drives in Three SCR four IGBTs HCSC.

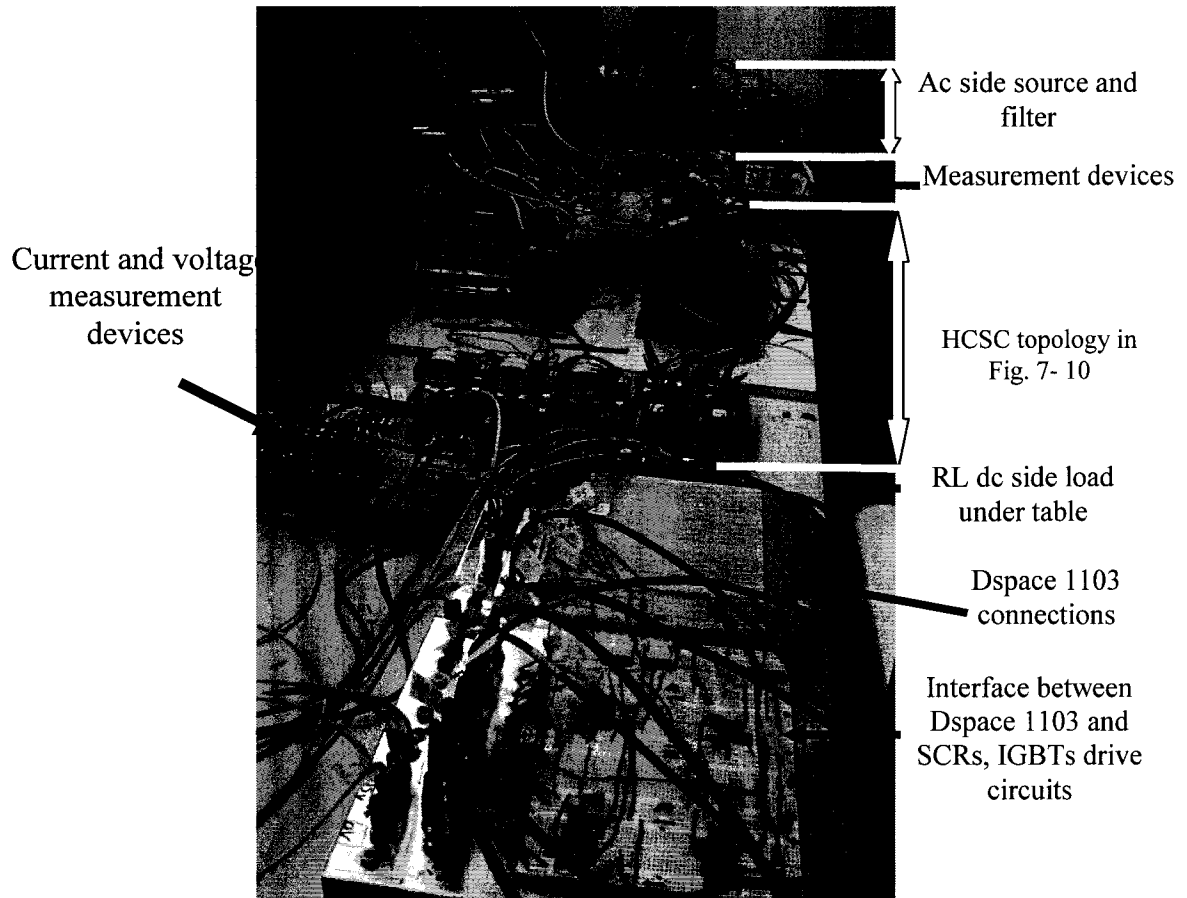
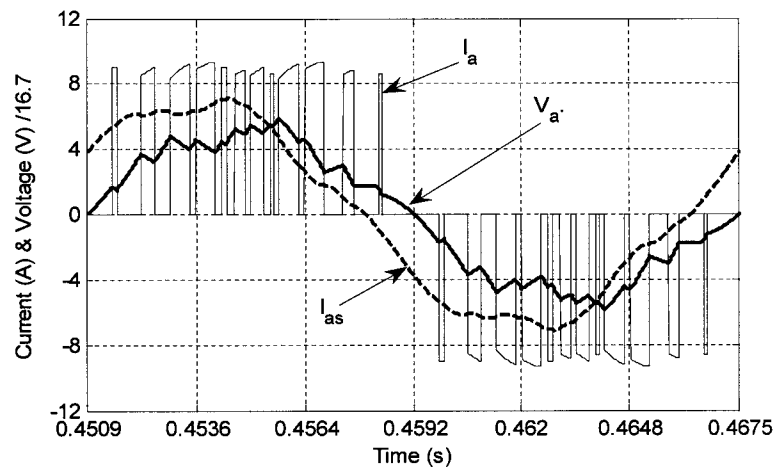


Fig. 7- 11 :- Complete view for Three SCR four IGBTs HCSC.

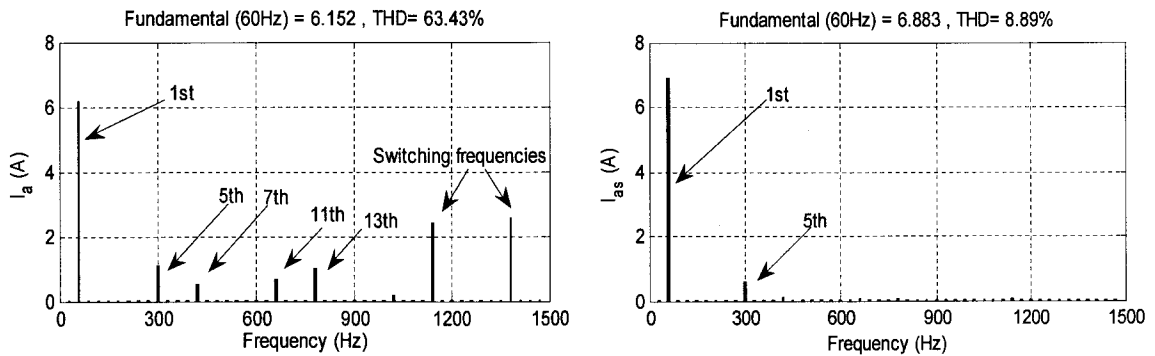
## 7.7. SIMULATION AND EXPERIMENTAL RESULTS

Fig. 7- 12 and Fig. 7- 13 show simulation and experimental results obtained for the HCSC with HS-SVM. There  $m_a = 0.7$  and UPF are adjusted between  $V_a$  and pulsated current in the HCSC terminals for phase A ( $I_a$ ), not include the ac-side filter. The waveforms are  $V_a$ ,  $I_a$  and phase A current at the PCC ( $I_{as}$ ). The harmonic spectra of  $I_a$  and  $I_{as}$  are also presented. The simulation and the experimental results are identical.  $I_a$  presents twice as many pulses in the middle of the positive (negative) semi-cycles because in this sector an IGBT (SCR) of that phase belongs to both active states. Since active states are separated by zero state, there will be two pulses of current per SVM

cycle in that sector. In the neighboring sectors, an IGBT (SCR) of that phase belongs to only one active state, thus generating only one current pulse per SVM cycle. The harmonic spectra show the presence of switching harmonics and non-characteristic LOH commonly found in SVM-CSC with low  $N_{CS}$ . The latter also appear in the 6-switches SVM-CSC with lower magnitudes when SAM is used in Fig. 7- 14. The proposed topology is not restricted to operate as rectifier. Fig. 7- 15 illustrates how UPF operation as inverter is possible as well as UPF rectifier.



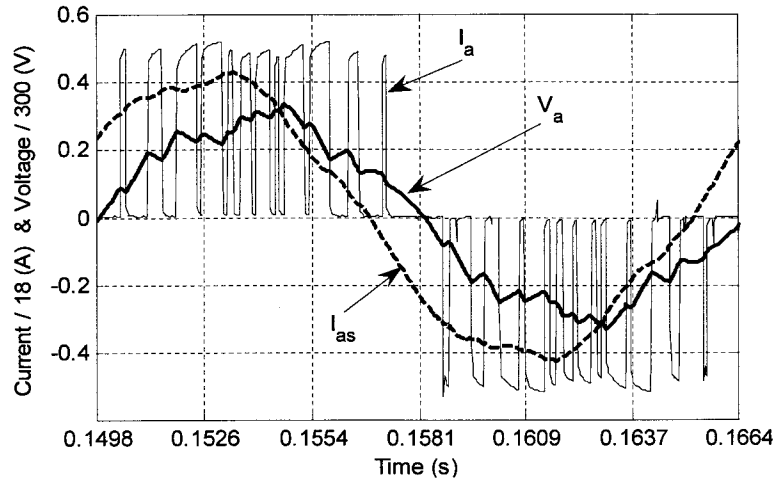
(a) Waveforms



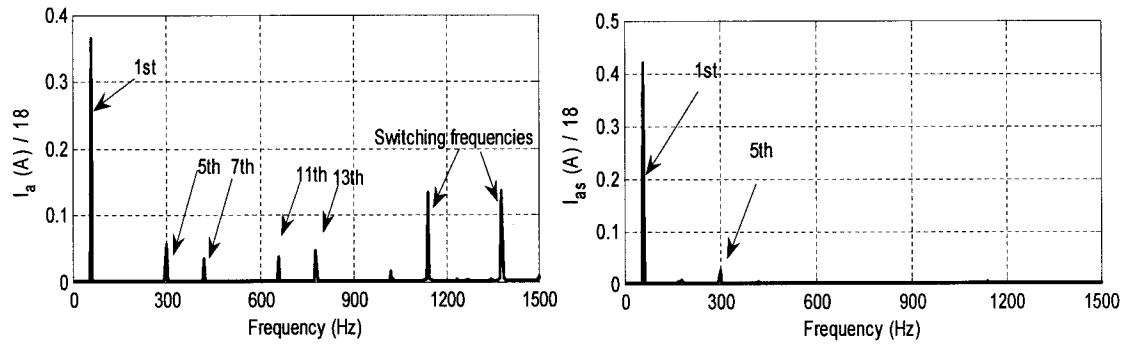
(b) Harmonic spectra.

Fig. 7- 12 :- Simulation results for HCSC with HS-SVM,  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $V_a$ ,  $I_a$  in phase.



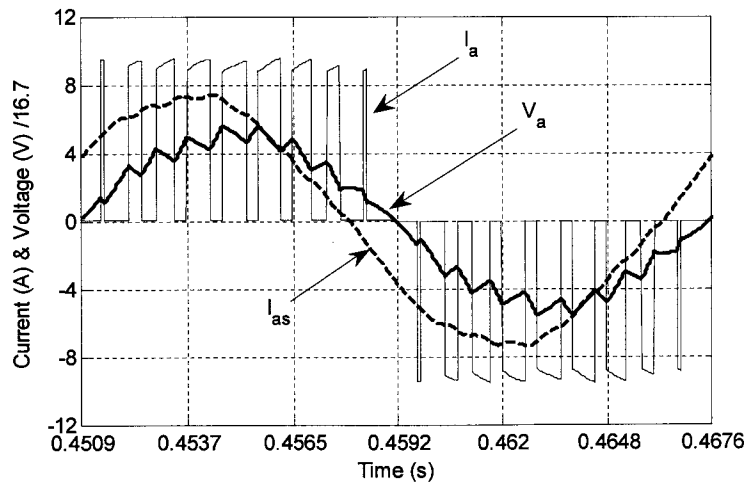


(a) Waveforms.

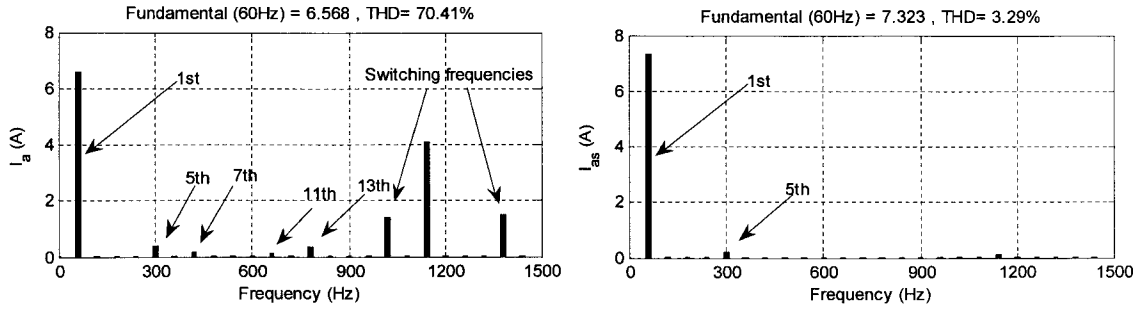


(b) Harmonic spectra.

Fig. 7- 13 :- Experimental results for HCSC with HS-SVM,  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $V_a$ ,  $I_a$  in phase.

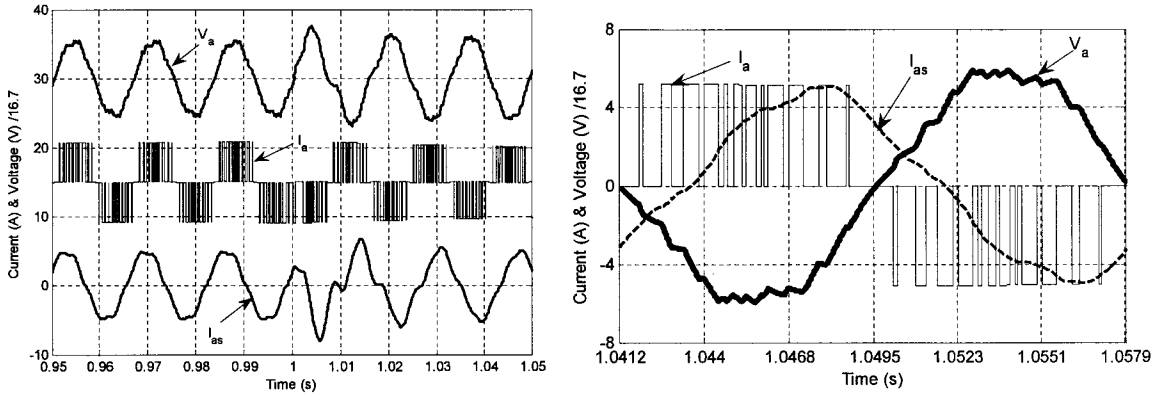


(a) Waveforms.



(b) Harmonic spectra.

Fig. 7- 14 :- Simulation results for SVM-CSC,  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $V_a$ ,  $I_a$  in phase.



(a) Transition from rectifier to inverter

(b) Inverter mode waveforms

Fig. 7- 15 :- Simulation results for HCSC with HS-SVM for  $m_a = 0.7$ ,  $N_{CS} = 3$ .

## 7.8. PF CONTROL FOR HCSC WITH HS-SVM

Closed loop control for 6-switches CSR aims are regulating the dc-side current ( $I_{dc}$ ), tracking reference active power ( $P_{ref}$ ) and reference reactive power ( $Q_{ref}$ ) signals as described in [80] - [84]. A similar control strategy is discussed in this section for the HCSC with HS-SVM. The optimization of the controllers is not the main issues presented in this thesis. Nevertheless, presenting the ability of the proposed HCSC with HS-SVM to operate with variable PF and to follow the required  $P_{ref}$  and  $Q_{ref}$  signals in the PCC is important to validate the proposed HCSC as well as the HS-SVM flexibility.

The study is conducted using the converter shown in Fig. 6- 7, where one can see the current directions and the voltage polarities. The three phase voltages and the three line currents at the PCC,  $(V_{(abc)s})$  and  $(I_{(abc)s})$ , are measured along with the dc-side current  $(I_{dc})$ . The three phase voltages across the capacitors  $(V_{(abc)})$  are calculated instantaneously using measured ac-side variables and the input filter parameters,  $R_{ac}L_{ac}C_{ac}$ , using (7- 6). Abc/ $\alpha\beta$  conversion is used in (7- 6) to simplify the instantaneous calculation process. Also, the capacitor current  $I_{(\alpha\beta)cap}$  ( $I_{(abc)cap}$ ) are calculated using  $V_{(\alpha\beta)}$  ( $V_{(abc)}$ ) and  $C_{ac}$ . From  $P_{ref}$  and  $Q_{ref}$  in the PCC and  $V_{(\alpha\beta)s}$  the required values of  $I_{(\alpha\beta)s\_ref}$  are generated from (7- 7) - (7- 10). By subtracting  $I_{(\alpha\beta)cap}$  from the required  $I_{(\alpha\beta)s\_ref}$ , the current required from the HCSR ( $I_{(\alpha\beta)\_ref}$ ) is found using (7- 11).

$$V_{(\alpha\beta)} = V_{(\alpha\beta)s} - I_{(\alpha\beta)s} \times (R_{ac} + j\omega L_{ac}) \quad (7- 6)$$

$$P_{ref} = V_{as}^{\wedge} I_{as\_ref}^{\wedge} + V_{bs}^{\wedge} I_{bs\_ref}^{\wedge} + V_{cs}^{\wedge} I_{cs\_ref}^{\wedge} = \frac{3}{2} (V_{\alpha s}^{\wedge} I_{\alpha s\_ref}^{\wedge} + V_{\beta s}^{\wedge} I_{\beta s\_ref}^{\wedge}) \quad (7- 7)$$

$$Q_{ref} = jV_{as}^{\wedge} I_{as\_ref}^{\wedge} + jV_{bs}^{\wedge} I_{bs\_ref}^{\wedge} + jV_{cs}^{\wedge} I_{cs\_ref}^{\wedge} = \frac{3}{2} (V_{\beta s}^{\wedge} I_{\alpha s\_ref}^{\wedge} - V_{\alpha s}^{\wedge} I_{\beta s\_ref}^{\wedge}) \quad (7- 8)$$

$$\begin{bmatrix} P_{ref} \\ Q_{ref} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} V_{\alpha s} & V_{\beta s} \\ V_{\beta s} & -V_{\alpha s} \end{bmatrix} \times \begin{bmatrix} I_{\alpha s\_ref} \\ I_{\beta s\_ref} \end{bmatrix} \quad (7- 9)$$

$$\begin{bmatrix} I_{\alpha s\_ref} \\ I_{\beta s\_ref} \end{bmatrix} = \frac{2}{3(V_{\alpha s}^2 + V_{\beta s}^2)} \begin{bmatrix} V_{\alpha s} & V_{\beta s} \\ V_{\beta s} & -V_{\alpha s} \end{bmatrix} \times \begin{bmatrix} P_{ref} \\ Q_{ref} \end{bmatrix} \quad (7- 10)$$

$$I_{(\alpha\beta)\_ref} = I_{(\alpha\beta)s\_ref} - I_{(\alpha\beta)cap} \quad (7- 11)$$

By this procedure, the capacitor voltage is emulated with pure sinusoidal waveform  $(V_{(\alpha\beta)})$  and the required current from HCSC  $I_{(\alpha\beta)\_ref}$  is calculated. So, one can follow the command of  $P_{ref}$  and  $Q_{ref}$  easily, after the input ac-side  $R_{ac}L_{ac}C_{ac}$  filter effect is isolated. That is done by using switching function concept where  $I_{(abc)\_ref}$  is represented in (7- 12). Using abc/dq transformation with capacitor voltage  $V_{(\alpha\beta)}$  ( $V_{(abc)}$ ) angle in the

rotating reference frame, one can follow  $I_{(dq)_{ref}}$ . Then, (7- 13) - (7- 15) are used to calculate the modulation indexes  $m_d$  and  $m_q$  used to generate  $m_{(abc)}$  required to follow  $P_{ref}$  and  $Q_{ref}$ .

$$I_{(abc)_{ref}} = m_{(abc)} \times I_{dc} \quad (7- 12)$$

$$I_{(dq)_{ref}} = m_{(dq)} \times I_{dc} \quad (7- 13)$$

$$m_d = I_{d_{ref}}/I_{dc} \quad (7- 14)$$

$$m_q = I_{q_{ref}}/I_{dc} \quad (7- 15)$$

When  $N_{CS} = 3$ , the minimum sampling step of DS-1103 was  $36\mu s$  when HCSC with HS-SVM was used for  $P_{ref}$  and  $Q_{ref}$  control. The dc-side impedance is increased to 90 mH with a  $10\Omega$  resistance to reduce the dc-side current variation during switching. A step change from  $P_{ref} = 400W$  and  $Q_{ref} = 0VAR$  to  $P_{ref} = 300W$  and  $Q_{ref} = -300VAR$  (leading) and vice versa is created every 0.1s to test the HCSC with HS-SVM. Experimental results are shown in Fig. 7- 16.

In Fig. 7- 16,  $P_{ref}$  and  $Q_{ref}$  variations are in the first window.  $I_{dc}$  gives an acceptable transient response in the second window. The third window is split into two, one for each operating condition (combination of certain  $P_{ref}$  and  $Q_{ref}$ ), where  $m_a$ ,  $V_a$  and  $I_a$  are shown. The fourth window show  $I_{as}$  and  $V_{as}$  in the PCC for a total of 0.3s. Finally,  $I_{as}$  and  $V_{as}$  are shown for one ac-side line cycle for each operating condition.  $I_a$  is rich in LOH due to the variation in the number of pulses, they are dense in the middle of the cycle.  $V_{as}$  and  $I_{as}$  for phase A gives exactly the required  $P_{ref}$  and  $Q_{ref}$  with UPF in the last left hand figure and the required  $P_{ref}$  and  $Q_{ref}$  in the last right hand figure.

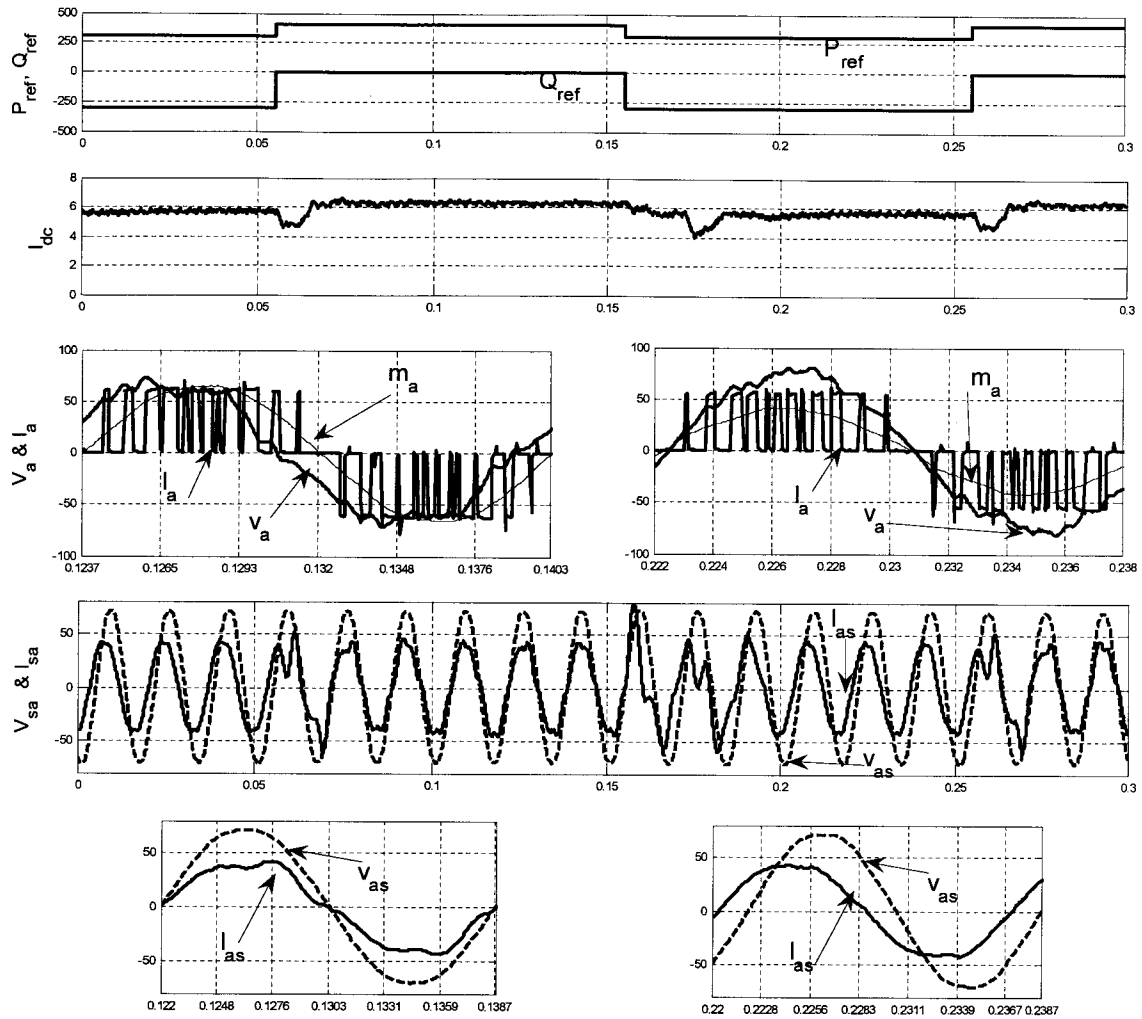


Fig. 7- 16 :- The effect of  $P_{ref}$  and  $Q_{ref}$  variations in HCSC with HS-SVM.

## 7.9. CONCLUSION

This chapter is presenting a hard switching SVM (HS-SVM) scheme suitable for operation with two proposed types of HCSCs, one employs an SCR bridge and two switches for actively commutating the SCRs, while the other employs three SCR and four switches. Unlike previous HCSCs, they are bi-directional and have no PF limitations when HS-SVM is used. These characteristics allow voltage regulation and reactive power

factor compensation. In fact, their capabilities are similar to those of the standard fully-controllable CSCs that require six force-commutated switches.

Typical values of experimentally calculated turn-off times of inverter grade SCRs available in the market today are considered for a realistic analysis of the potential and limitations of the proposed topology. For instance, due to the SCR's commutation issues, the maximum modulation index (gain) for the HCSC is reduced. The gating signals for the semiconductor devices in HCSC with HS-SVM are compared to those of 6-switches SVM-CSC. The switching frequency of the four force-commutated switches is higher than those of a conventional CSC for a given value of  $f_{\text{cycle}}$  used in SVM.

The HCSC with three SCRs and four IGBTs was implemented experimentally and simulation results were obtained. The proposed HCSC has potential to present harmonic spectra similar to those of six-switch CSCs in the ac-side and in the dc-side voltages and currents. A procedure permitting the HCSC with HS-SVM to follow the required  $P_{\text{ref}}$  and  $Q_{\text{ref}}$  using simple closed loop control circuit was discussed. The theoretical analysis was verified by means of simulation results as well as experimental verifications.

## CHAPTER 8

### 8. SOFT-SWITCHING SVM FOR HCSC

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#### 8.1. INTRODUCTION

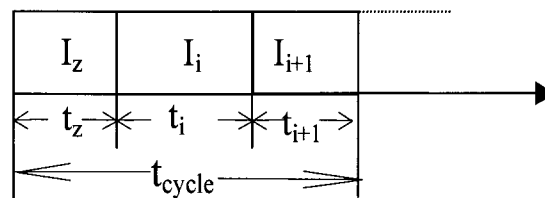
HS-SVM presented in the previous chapter can drive three SCRs four IGBTs HCSC. But, IGBTs are switched with high number of pulses for the same  $f_{\text{cycle}}$  of 6-switches SVM-CSC, which give high switching power losses. Besides, the harmonic spectrum is worse than the one obtained for 6-switches SVM-CSC. And,  $m_{a,\text{max}}$  is limited to a small value, which limits the band of switching frequencies where HCSC compete the traditional 6-switches SVM-CSC.

In this chapter a new SVM technique for HCSC is proposed, named by the author soft switching SVM (SS-SVM). When the angle between current and voltage vectors in the input of the HCSC is known it is possible to identify what transitions between active states can be executed with a more forward biased SCR blocking a less forward biased SCR in the even sectors. This is line-commutation (soft-switching) as occurs for conventional six SCRs phase controlled CSCs and can be implemented using soft switching (SS). There is always one transition can be done by soft switching in each SVM cycle for HCSC while the other require hard-switching. By this way, the number of zero state segments can be reduced to one and sequences with three segments can be used in all sectors to regain good harmonic spectrum, reduce frequent switching of IGBTs for the and  $m_{a,\text{max}}$  can be increased. SS-SVM is presented in this chapter using simulation and experimental results. Parts of this chapter materials were presented in [85], [86].

## 8.2. SS-SVM PRINCIPLES FOR THE THREE SCRs AND FOUR IGBTs HCSC

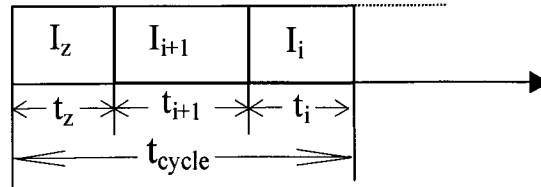
The proposed three segment sequence of states is started with a zero state to give opportunity for the algorithm to decide which active state should be used next (first). If the common device of the active states in a given sector is an SCR the zero state is implemented through this SCR to reduce switching stress on  $S_7$  ( $I_{10}$ ). If not, the zero state is implemented with  $S_7$ . The choice of which zero state should be used in each sector follows the guidelines presented in Table 8- 1, with the exception of the first zero state of odd sectors which require to be implemented using  $S_7$  due to a certain issue, presented later on, appears when both sectors and cycles transactions appears in the same time.

The second state is the active state that will allow natural commutation in the transition to the other active state, when an SCR is fired and the other is blocked. It can be identified based on specific input voltages relationships depicted in Table 8- 1. This can be changed during a sector as the instantaneous values of the phase voltages vary, making one phase voltage change from smaller to larger than the other. In such a case, the sequence of active states should be reversed from the sequence shown in Fig. 8- 1 (a) to the one in Fig. 8- 1 (b) or vice versa to obtain a line-commutation. This procedure is critical in the even sectors to guarantee the safe commutation of SCRs.



(a) Up sequence





(b) Down sequence.

Fig. 8- 1 :- Sequences of states required for line-commutation (soft switching).

TABLE 8- 1 :- AC SIDE VOLTAGE RELATIONS AND REQUIRED STATES SEQUENCES IN SS-SVM.

Sector	Key voltage relation	Irrelevant voltage	Sequence of states
0	$V_C > V_B$	$V_A$	$I_{10}-I_1-I_6$ (Down)
	$V_B > V_C$	$V_A$	$I_{10}-I_6-I_1$ (Up)
1	$V_A > V_B$	$V_C$	$I_9-I_2-I_1$ (Down)
	$V_B > V_A$	$V_C$	$I_9-I_1-I_2$ (Up)
2	$V_A > V_C$	$V_B$	$I_{10}-I_3-I_2$ (Down)
	$V_C > V_A$	$V_B$	$I_{10}-I_2-I_3$ (Up)
3	$V_B > V_C$	$V_A$	$I_7-I_4-I_3$ (Down)
	$V_C > V_B$	$V_A$	$I_7-I_3-I_4$ (Up)
4	$V_B > V_A$	$V_C$	$I_{10}-I_5-I_4$ (Down)
	$V_A > V_B$	$V_C$	$I_{10}-I_4-I_5$ (Up)
5	$V_C > V_A$	$V_B$	$I_8-I_6-I_5$ (Down)
	$V_A > V_C$	$V_B$	$I_8-I_5-I_6$ (Up)

To understand the logic behind SS-SVM, let's take one of the even sectors, sector four as an example, the same can be done for other even sectors. There, the nearest active states are  $I_4$  (S5-S4) and  $I_5$  (S5-S6). Transition from state  $I_4$  to  $I_5$  requires the commutation of S4 what can be done with line commutation by firing S6 if  $V_A > V_B$ . In this case, as shown in Table 8- 1, one should use the “up sequence”  $I_{10}$ - $I_4$ - $I_5$  as depicted in Fig. 8- 1 (a). On the other hand, when  $V_B > V_A$  one should use the “down sequence”  $I_{10}$ - $I_5$ - $I_4$  shown in Fig. 8- 1 (b). The magnitude of  $V_C$  is irrelevant in the process. The voltage relations that need to be considered in each sector for realizing one of the two transitions between active states with SS are shown in Table 8- 1. There one can also see when up and when down sequences should be used and if the transition will result in soft switching of an SCR (mandatory to guarantee safe commutation) or of an IGBT. The latter is not mandatory but should be used for the sake of half wave symmetry of the waveforms, for harmonic spectrum without even harmonics.

It should be noted that as the PF of the HCSC varies, the moment when a phase voltage becomes smaller or larger than another is changed in the SVM sectors. Fig. 8- 2 shows the voltage magnitude relations for the HCSC operating with  $PF = \cos 10^\circ$ , leading. In such a case, the center point of the “voltage disc”  $V_C > V_A > V_B$  leads  $I_5$  by  $10^\circ$ . For lagging power factor, the “voltage disc” should be rotated clockwise with respect to the current vector by an angle equal to  $\cos^{-1}(PF)$ . Thus, for a lagging PF equal to 0.866, ( $\cos 30^\circ$ ), only the up sequence should be used for success soft-switching.

One can note from results in Fig. 7- 12 to Fig. 7- 16 that the capacitor voltage is distorted in SVM-CSC and HCSC with HS-SVM, the same happens in HCSC with SS-SVM. The concept of SS-SVM is depending on the line to line voltage polarity. In CSCs

the current in the converter ac-side before filtering is a pulsating current, the same for HCSC. Thus, the voltage in the ac-side capacitors terminals is distorted. One should check if this distortion has an impact on the safe commutation of SCRs using SS-SVM.

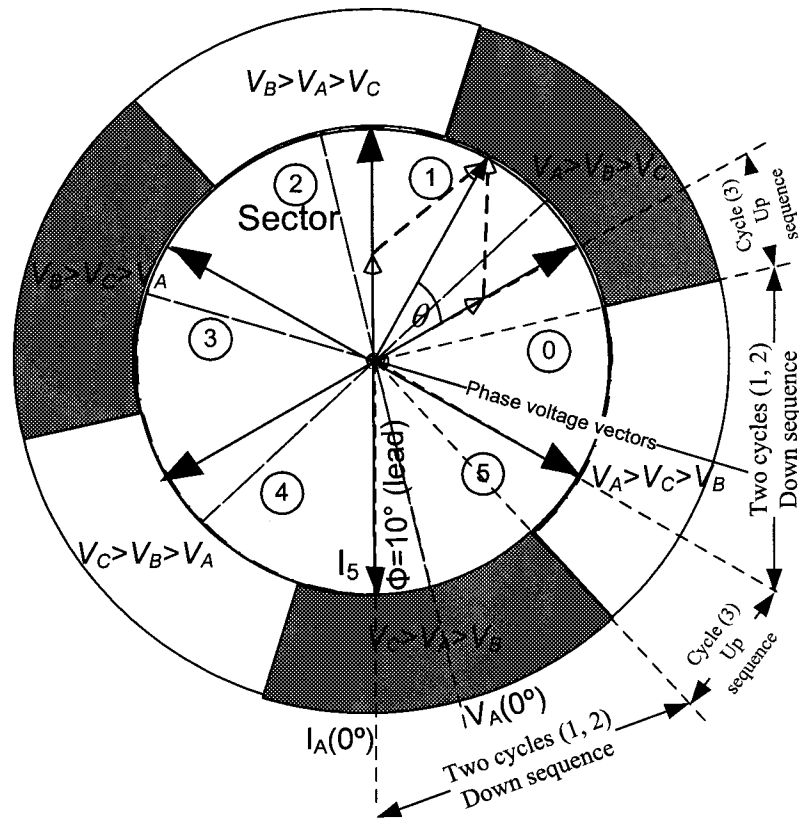


Fig. 8- 2 :- Input voltage relationships and current complex plane for the HCSC with  $PF = \cos 10^\circ$ , leading.

From Table 8- 1, in sector zero when up sequence is used  $V_B > V_C$  is required and exist if there is no voltage distortion. First  $I_{10}$  is used in the beginning of the SVM cycle, where no current drawn from the ac-side. This implies no distortion in capacitor voltages. Then  $I_6$  is used with S1-S6 turned ON and withdraw current from the capacitor voltage  $V_{AB}$ , which leads  $V_{AB}$  to be reduced,  $V_A$  is reduced while  $V_B$  is increased, while  $V_C$  should have no effect. Thus,  $V_B$  becomes higher than what it should be without distortion

which is already higher than  $V_C$ , which enhances state transition from  $I_6$  with S6 to  $I_1$  with S2. Thus, distortion in the capacitor voltage support SS-SVM concept. In SS-SVM the capacitors voltage distortion is an obstacle in deciding the switching instants. PLL (Phase locked loop) is used to generate a pure sine from distorted capacitors voltages, those are used along with the required reference current to generate the gating signals.

The three SCR and four IGBTs HCSC topology itself does not impose any limitations on the PF. In HS-SVM, SCRs are always actively commutated independent on the PF. And, if  $t_{off,min}$  is respected the input voltages have no impact on the safe commutation of the SCRs. On the other hand, when the HCSC is controlled with SS-SVM, there will be a line-commutation of an SCR per SVM cycle, which requires a given voltage relationship to be successful. The decision of using either the up or the down sequence of active states is taken in the beginning of the SVM cycle, based on a given voltage relationship. This cannot be changed during that SVM or commutation failure might occur. Thus, in the proposed SS-SVM scheme, it is necessary that the voltage relationships do not change inside an SVM cycle to guarantee the safe commutation of SCRs. Therefore, the angle between the current and voltage in the input of the CSC, not including the filter, can only be varied in step. This problem can be prevented by limiting the angle between the reference current and capacitor voltage to a set of discrete values given in (8- 1).

$$\angle \vec{I} - \angle \vec{V} = \pm \sum_{n=1}^{n=N_{CS}} \frac{60^\circ}{N_{CS}} n + 30^\circ = \pm \sum_{n=1}^{n=N_{CS}} \delta_{a(n)} \quad (8- 1)$$

Where  $\angle \vec{V}$  is the rotating capacitor voltage vector angle,  $\angle \vec{I}$  is the required rotating current vector angle. The  $30^\circ$  angle is added because of the phase shift between

phase and line voltages, which impact SCR commutation in SS-SVM.  $\delta_{a(n)}$  is an array of angles with length  $n$ , one of those is required between current and voltages vectors for safe commutation. In (8- 1) the number of possible values of PF and also  $\delta_{a(n)}$  array length increases and the different between allowed values decreases as  $N_{CS}$  increases. When  $N_{CS} = 3$  is used, it resulting in multiples of  $20^\circ$  angles with  $10^\circ$  maximum error. This can be reduced by increasing  $N_{CS}$  at the expense of increasing switching frequency. However this would also increase the commutation losses and  $m_{a,max}$  would be reduced.

The magnitude of the pulsated converter current for phase A ( $I_a$ ) can be varied continuously. But the phase angle between the  $I_a$  and  $V_a$  cannot. Thus, one cannot control active and reactive power for HCSC independently and continuously. In such a case, one should create a reference current vector, with the above mentioned angle restrictions, so that  $P_{ref}$  is followed accurately while accepting an error in  $Q_{ref}$ . So, the value of  $\delta_b$  (before changing), which satisfies the exact  $P_{ref}$  and  $Q_{ref}$ , is modified to be  $\delta_a$  which satisfies (8- 1) as one of  $\delta_{a(n)}$  array values, which satisfies  $P_{ref}$  while accepting error in  $Q_{ref}$ . And, the magnitude of the reference current vector is recalculated to give the required value of  $P_{ref}$ .  $Q_{ref}$  will present an error with respect to the reference value,  $Q_a$  is the available reactive power. Then, from the value of  $I_{dc}$  one calculates  $m_a$ , which should be smaller or equal to  $m_{a,max}$ , presented later on. This would be quite acceptable in applications such as SMES and grid-side converter of an adjustable speed drive, where the main task of the HCSCs is to control the active power flow, with reactive power flow control being an added value.

The proposed logic for generating SS-SVM gating signals is as follows. First, the capacitor voltages  $V_{(\alpha\beta)}$  ( $V_{(abc)}$ ) are created using (7- 6). Then, the preliminary values of the current required from the HCSC  $I_{(\alpha\beta)\_ref}$  ( $I_{(abc)\_ref}$ ) are generated from  $P_{ref}$ ,  $Q_{ref}$  and

$V_{(\alpha\beta)}$  ( $V_{(abc)}$ ) using (7- 11). In the following, if the dq frame reference angle is taken from source voltage  $V_{(abc)s}$  the variables will be written with double dash ( $\bar{\bar{I}}$  or  $\bar{\bar{V}}$ ). And, if it is taken from capacitor voltage  $V_{(\alpha\beta)}$  ( $V_{(abc)}$ ) the variables will be written with single dash ( $\bar{I}$  or  $\bar{V}$ ).  $I_{(abc)\_ref}$  is the current required from HCSC. In HS-SVM it is converted to dq frame where the frame reference angle is taken from  $V_{(\alpha\beta)}$  ( $V_{(abc)}$ ). The angle between  $V_a$  and  $I_a$  in this case is  $\delta_b$  (before adjusted).  $\delta_b$  is given in (8- 2) using  $\bar{I}_{db}$  and  $\bar{I}_{qb}$  (dq currents before adjusted).  $\delta_b$  should be changed to the nearest value from  $\delta_{a(n)}$  in (8- 1), that is  $\delta_a$ .

$$\tan(\delta_b) = \frac{\bar{I}_{qb}}{\bar{I}_{db}} \quad (8- 2)$$

To follow the required  $P_{ref}$ ,  $\bar{\bar{I}}_{ds}$  calculated from (8- 3) should be followed.  $\bar{\bar{I}}_{dcap}$  (Capacitor current) are calculated from  $I_{(\alpha\beta)cap}$ . The value of  $\bar{\bar{I}}_d$  required in the terminals of HCSC to follow  $P_{ref}$  is calculated in (8- 4). Since  $V_{(abc)}$ , by definition, lags  $V_{(abc)s}$  by an angle ( $\alpha$ ), then  $\bar{\bar{I}}_d$  with  $V_{(abc)s}$  as dq frame reference angle can be represented with (8- 5) using  $\bar{I}_d$  and  $\bar{I}_q$  with  $V_{(abc)}$  as dq frame reference angle.

$$\bar{\bar{I}}_{ds} = \frac{P_{ref}}{\frac{3}{2} \bar{\bar{V}}_{ds}} \quad (8- 3)$$

$$\bar{\bar{I}}_d = \bar{\bar{I}}_{ds} - \bar{\bar{I}}_{dcap} \quad (8- 4)$$

$$\bar{\bar{I}}_d = \bar{I}_d \cos(\alpha) + \bar{I}_q \sin(\alpha) \quad (8- 5)$$

Both of  $\bar{I}_d$  and  $\bar{I}_q$  should change with a certain profile to reach the required  $\bar{\bar{I}}_d$  and satisfy  $P_{ref}$ . After they change they should satisfy (8- 6) with  $\delta_a$  being the nearest value from array  $\delta_{a(n)}$  calculated from (8- 1). When angle  $\alpha$  supposed to be constant, using (8- 2) and (8- 6) to rewrite (8- 5) one can reach (8- 7) which include  $\bar{I}_{da}$ ,  $\bar{I}_{qa}$ ,  $\bar{I}_{db}$  and  $\bar{I}_{qb}$  (dq frame values for the required currents from HCSC after and before changing to adequate

SS-SVM concept). That is rewritten in (8- 8). From (8- 8) and (8- 6) one can reach (8- 9). That is substituted by (8- 10). Then, the value of  $\overline{I_{da}}$  and selected  $\delta_a$  satisfying (8- 1) are used to calculate  $\overline{I_{qa}}$  from (8- 6).

$$\tan(\delta_a) = \frac{\overline{I_{qa}}}{\overline{I_{da}}} \quad (8- 6)$$

$$\overline{I_d} = \overline{I_{db}} \cos(\alpha) + \overline{I_{qb}} \sin(\alpha) = \overline{I_{da}} \cos(\alpha) + \overline{I_{qa}} \sin(\alpha) \quad (8- 7)$$

$$\tan(\alpha) = \frac{\overline{I_{db}} - \overline{I_{da}}}{\overline{I_{qa}} - \overline{I_{qb}}} \quad (8- 8)$$

$$\tan(\alpha) = \frac{\overline{I_{db}} - \overline{I_{da}}}{\overline{I_{da}} \tan(\delta_a) - \overline{I_{qb}}} \quad (8- 9)$$

$$\overline{I_{da}} = \frac{\overline{I_{db}} + \overline{I_{qb}} \tan(\alpha)}{1 + \tan \alpha \tan(\delta_a)} \quad (8- 10)$$

$\overline{I_{da}}$  and  $\overline{I_{qa}}$  are the dq component with the angle of  $V_{(abc)}$  taken as the frame reference angle for  $I_{dq\_ref}$ . It is used to calculate the modulation index in SS-SVM from (7- 13) - (7- 15). The reactive power available ( $Q_a$ ) is calculated from (8- 12) with  $\overline{I_{qa}}$  calculated from (8- 11). This procedure satisfies (8- 1) and guarantees safe commutation in SS-SVM with the required  $P_{ref}$  and  $Q_a$  instead of  $Q_{ref}$ . This procedure is presented as an example of satisfying SS-SVM restriction, which is used in this thesis. It can be changed depending on the application and which variable is respected,  $P_{ref}$  or  $Q_{ref}$  or  $I_{dc}$ . Another procedure which is not presented here is to follow accurately  $I_{dc}$  when its exact regulation is required while both  $P_{ref}$  and  $Q_{ref}$  can present an error.

$$\overline{I_{qa}} = \overline{I_{qa}} \cos(\alpha) - \overline{I_{da}} \sin(\alpha) \quad (8- 11)$$

$$Q_a = \frac{3}{2} \overline{V_{ds}} \times (\overline{I_{qa}} + \overline{I_{qcap}}) \quad (8- 12)$$

The next step is to identify the sector and respective states, duration of states and the sequence (up or down) that should be used. The sector and active states are identified

directly from  $\varphi_I$ , i.e. the reference vector is in sector five for ( $0^\circ \leq \varphi_I \leq 60^\circ$ ) and the nearest active states are  $I_5$  and  $I_6$ . The selection of the up or the down sequences depends on the voltage relations in the ac-side. For leading PF with  $10^\circ$ , the voltage rings are rotated counterclockwise and the first two SVM cycles of sector five ( $0^\circ \leq \varphi_I \leq 40^\circ$ ) should be implemented with the down sequence while the last SVM cycle ( $40^\circ \leq \varphi_I \leq 60^\circ$ ) with the up sequence, as shown in Fig. 8- 2. There, the center point of the segment “ $V_C > V_A > V_B$ ” leads  $I_5$  by  $10^\circ$ . The first  $40^\circ$  of sector five take place under “ $V_C > V_A > V_B$ ” and the last  $20^\circ$  take place under “ $V_A > V_C > V_B$ ”. In such a case, for  $N_{CS}=3$  and following the directions of Table 8- 1, the down sequence is used in the first two SVM cycles ( $40^\circ$ ) and the up sequence in the last SVM cycle ( $20^\circ$ ). The same applies to the other five sectors. On the other hand, if  $N_{CS} = 4$  with PF =  $10^\circ$  leading, the key voltage ( $V_C > V_A$ ) reverses in the third SVM cycle and a commutation failure might occur.

The impact of the ac-side voltage waveforms on the selection of the type of sequence is shown in Fig. 8- 3, there the gating pattern for the HCSC with SS-SVM when  $m_a = 0.7$ ,  $N_{CS} = 3$  and PF =  $\cos 10^\circ$  leading is shown. The upper window illustrates the  $m_a$  reference current signal ( $I_{a.ref}$ ), the capacitor voltage across phase A ( $V_a$ ) with PLL and line voltages between phases A, B and C ( $V_{ab}$  and  $V_{ac}$ ). The lower window in Fig. 8- 3 (a) illustrates SCRs gating pulses in HCSC with SS-SVM. And, the lower window in Fig. 8- 3 (b) illustrates IGBTs gating pulses in HCSC with SS-SVM.

Let’s investigate what happens in sector two when PF =  $10^\circ$  leading is used as it is shown in Fig. 8- 3.  $V_{AC}$  is required for deciding whether an up or a down sequence should be used in sector two, as mentioned in Table 8- 1. S3 is the common element for states  $I_2$  and  $I_3$  and S7 is used for implementing the zero state ( $I_{10}$ ). For ( $170^\circ \leq \omega t \leq 210^\circ$ )



in Fig. 8- 3,  $V_{AC} > 0$  and the down sequence ( $I_{10}$ - $I_3$ - $I_2$ ) should be used. One can see that S7 is switched first followed by S3 and S4 (state  $I_3$ ) then S3 and S2 (state  $I_2$ ) as described in Table 8- 1. For  $V_{AC} > 0$ , firing of S2 (lower half leg of phase C) will block S4 (lower half leg of phase A). Following the same procedure, for ( $210^\circ \leq \omega t \leq 230^\circ$ ),  $V_{AC} < 0$  and the up sequence ( $I_{10}$ - $I_2$ - $I_3$ ) is used.

Zero state is realized through S7 in even sectors and through the bridge in odd sectors. This approach might fail in even to odd sector transitions, if SVM sector and SVM cycle transitions appear in the same time and down sequences are used in both. As an example, a transition from sector four to sector five would require a transition from active state  $I_4$  (S5-S4) to zero state  $I_8$  (S3-S6), when commutations of both switches and SCRs take place together. The success of the latter is depends on the input voltage relations. To avoid this problem, the first state in all sectors is implemented with state  $I_{10}$  (S7), to which any SCRs commutations is safe.

In Fig. 8- 3 the even sector is ended with an up sequence. In this case, the first zero state of odd sector can be implemented with a bridge leg. But, it is implemented with S7 to avoid changing the freewheeling procedure in the beginning of odd sectors depending on states sequence for the sake of generality and simplicity. If down sequence appears in the last SVM cycle of the SVM sectors, the first zero state of an odd sector should be implemented with S7. Fig. 8- 4 presents the same results of Fig. 8- 3 with  $PF = \cos 30^\circ$  leading, where sectors are ended with down sequence and first state in all sectors should be implemented with S7.

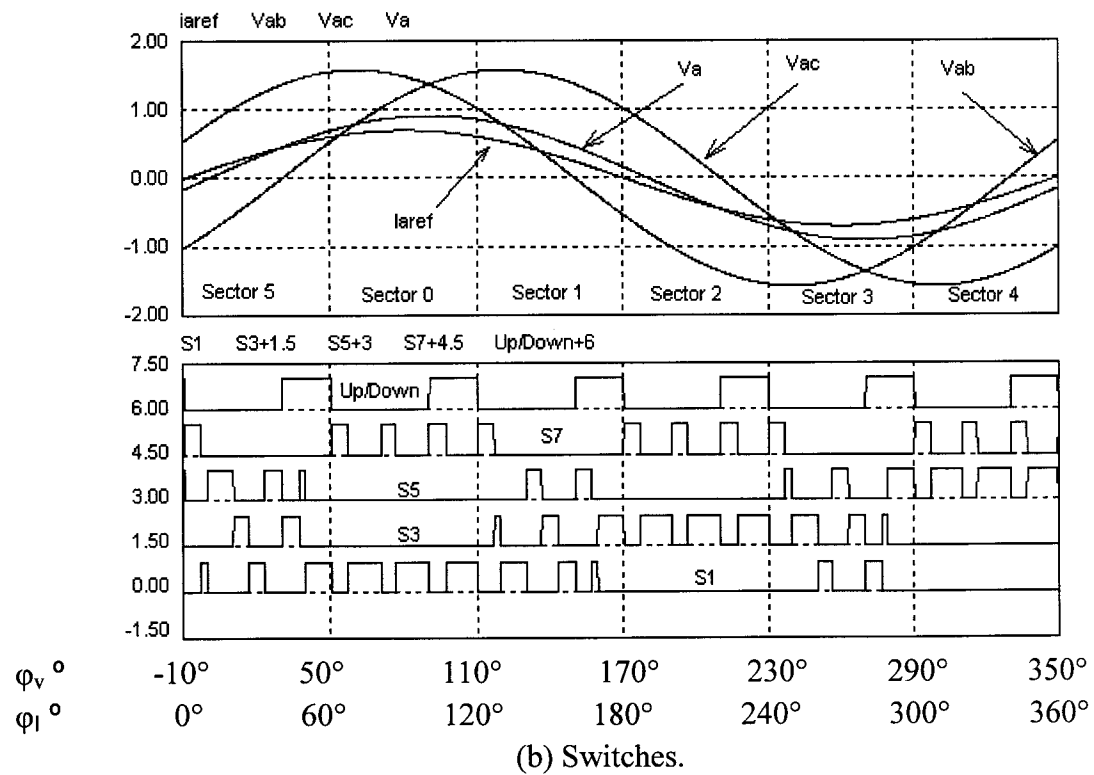
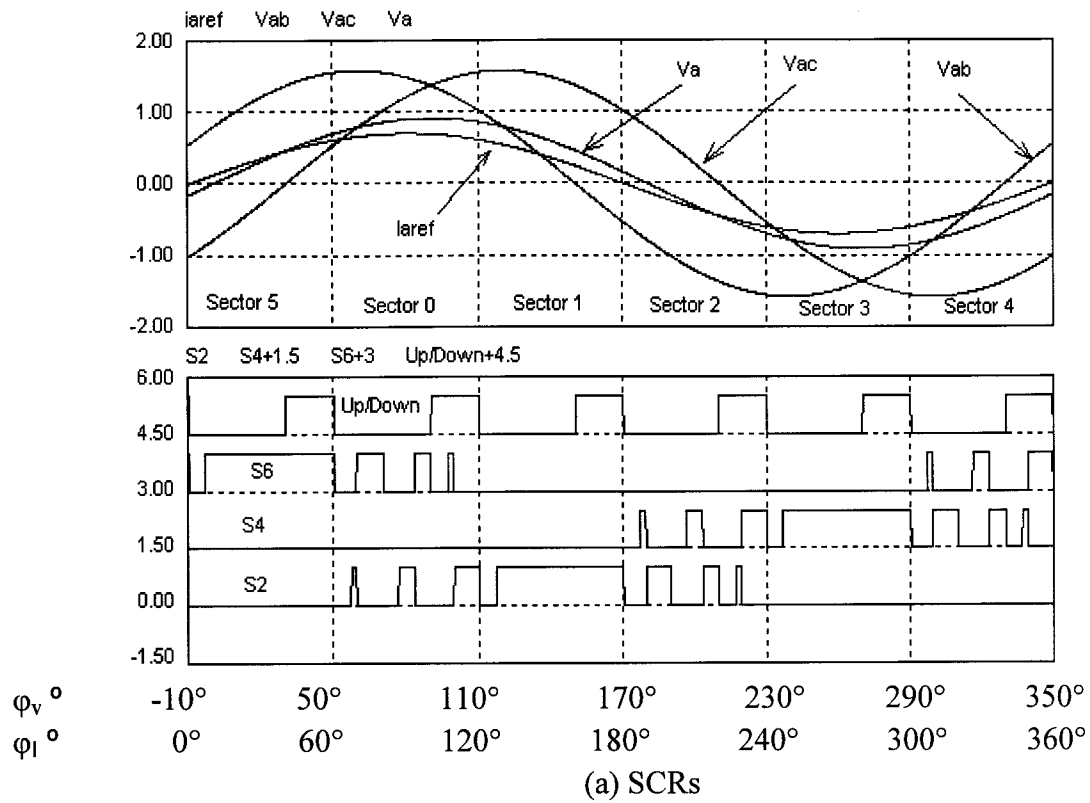


Fig. 8- 3 :- Gating pattern for the HCSC with SS-SVM when  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $PF = \cos 10^\circ$ , leading.

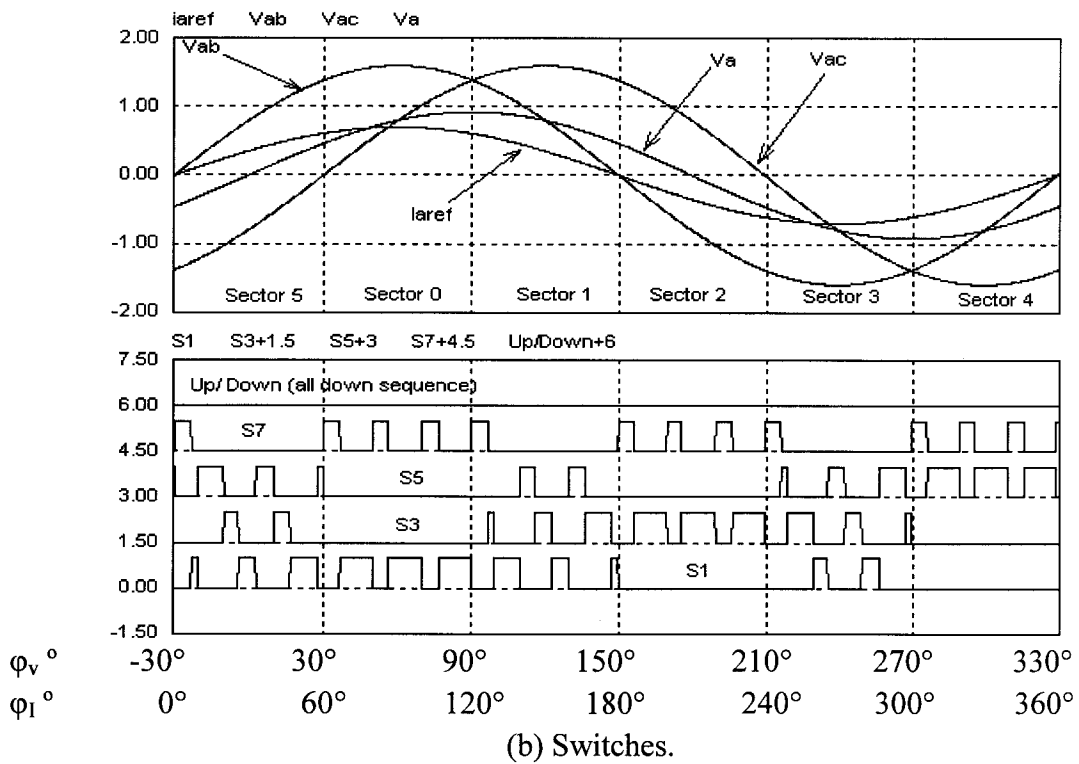
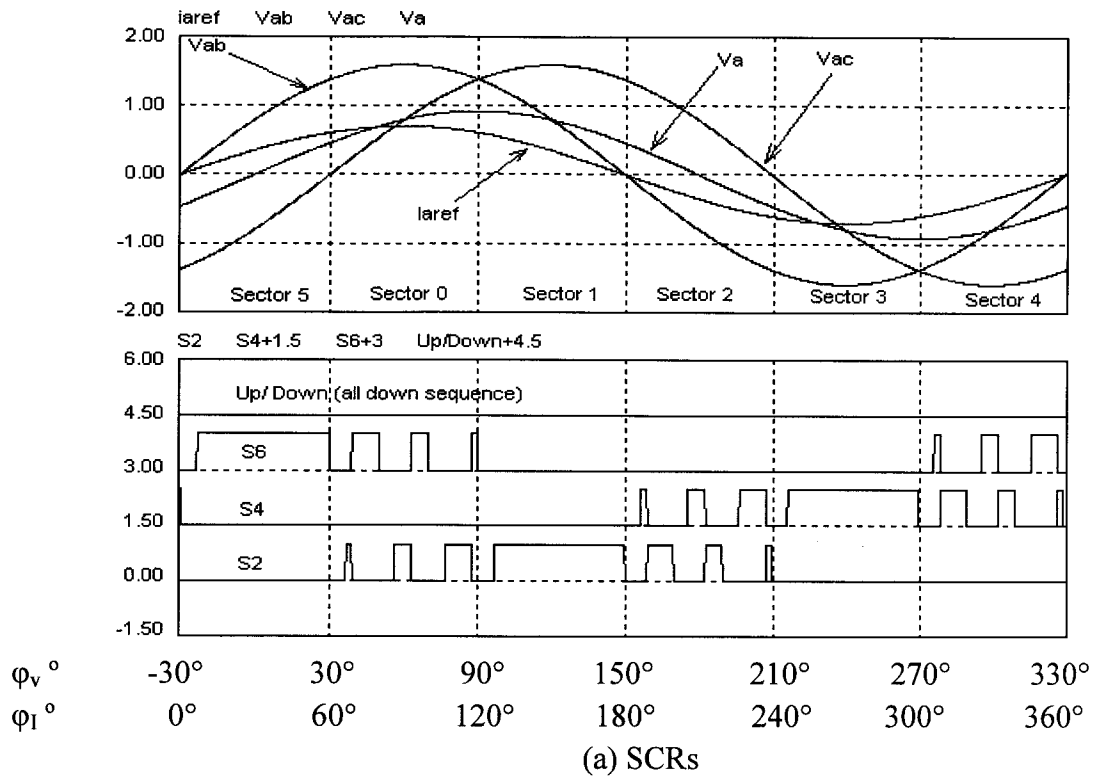


Fig. 8- 4 :- Gating pattern for the HCSC with SS-SVM when  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $PF = \cos 30^\circ$ , leading.

### 8.3. AVERAGE SWITCHING FREQUENCY OF THE SEMICONDUCTORS

In this Section, the total number of pulses per line cycle ( $N_p$ ) imposed on IGBTs and SCRs in HCSC with SS-SVM are calculated. The HCSC presents an asymmetrical topology. The SS-SVM technique employs three segment sequences, with one zero state segment. From Fig. 8- 3 and Fig. 8- 4, the following average switching frequency calculations can be understood.

S7 is presenting  $N_{CS}$  pulses in each of the even sectors, and one in each of odd sector for a total of  $3 N_{CS} + 3$  pulses per line cycle. The bridge IGBTs switch in four sectors. In one, an odd sector, each of them realizes a zero state switching  $N_{CS}$  pulses minus 1, realized by S7 in the beginning of the odd sector. The other three occur when the desired line currents in their phases present the appropriate direction. In two of those, where they belong to one of the two active states, they switch  $N_{CS}$  pulses, in each of sector. In the remaining (even) sector, they are used to implement both active states but unlike in the 6-switch SVM-CSC, they need to be turned off to actively commutate an SCR, thus operating with  $N_{CS}$  pulses in that sector. So, each bridge IGBT presents  $4 N_{CS} - 1$  pulse per line cycle.

Regarding the SCRs, they are used to implement one active state in two even sectors, with  $N_{CS}$  pulses per sector. In one odd sector, between the previous two sectors and where they are common to the two active states, they are used to implement the zero state, with the exception of the first zero state of that sector, realized with S7. In such a case, the SCR will not be common to the last state of previous sector and the first of the actual sector. Besides, since the first state of the following even sector is implemented

through S7, there will be an extra SCR pulse with respect to HS-SVM. Therefore, each SCR will present  $2 N_{CS} + 1$  pulses per line cycle. That can be observed in Fig. 8- 3 and Fig. 8- 4 for the HCSC operating with SS-SVM and  $m_a = 0.7$ ,  $N_{CS} = 3$  for  $PF = \cos 10^\circ$  and  $PF = \cos 30^\circ$  leading, respectively. In the first case, up and down sequences are used while in the second only the down sequence is. The total numbers of “pulses” of the HCSC with SS-SVM is  $15 N_{CS}$  for IGBTs and  $6 N_{CS} + 3$  for SCRs.

#### 8.4. LIMITATIONS ON THE MODULATION INDEX ( $M_A$ )

The maximum modulation index ( $m_{a,max}$ ) is limited by the mandatory time of use of the zero state ( $t_{off,min}$ ). As this increases,  $m_{a,max}$  is reduced. For the HCSC, the value of the smallest possible zero state ON time ( $t_{z,min}$ ) is set based on the time required by an SCR to regain its blocking capability after being actively commutated and how often this occurs in the SVM cycle. There are two zero states in HS-SVM sequence of states, while there is only one in SS-SVM. Thus,  $t_{z,min-HS} = 2t_{z,min-SS} = 2t_{off,min} = 2kt_q$ . Therefore,  $m_{a,max}$  with SS-SVM is higher than  $m_{a,max}$  with HS-SVM. The impact of  $t_{z,min}$  on  $m_{a,max}$  is calculated by substituting (1- 4) and (1- 5) in (1- 6) for  $t_{z,min}$  yielding (8- 13), one obtains (8-14) when solving for  $m_a$ . The  $m_{a,max}$  occurs for  $\theta = \pi/6$  and its value is given in (8- 15).

$$t_{cycle} - t_{cycle} m_a \sin\left(\frac{\pi}{3} - \theta\right) - t_{cycle} m_a \sin(\theta) \geq t_{z,min} \quad (8- 13)$$

$$m_a \leq \frac{1 - t_{z,min} f_{cycle}}{\sin\left(\frac{\pi}{3} - \theta\right) + \sin(\theta)} \quad (8-14)$$

$$m_{a,max} = 1 - t_{z,min} f_{cycle} \quad (8- 15)$$

Fig. 8- 5 shows how  $m_{a,max}$  varies with  $f_{cycle}$  and  $t_{off,min}$  for both HS-SVM and SS-SVM. There one can say that high  $m_{a,max}$  is obtained by using fast SCRs. And, a trade-off solution involving  $m_{a,max}$  and the size of ac-side filter needs to be worked out. As an

example, for SVM with  $N_{CS}=3$ ,  $f_{cycle}=1080\text{Hz}$  and with  $t_{off,min}=50\mu\text{s}$  ( $k=2.5$  and  $t_q=20\mu\text{s}$ ) the  $m_{a,max}$  for HS-SVM is 0.892 while for SS-SVM it is 0.946.

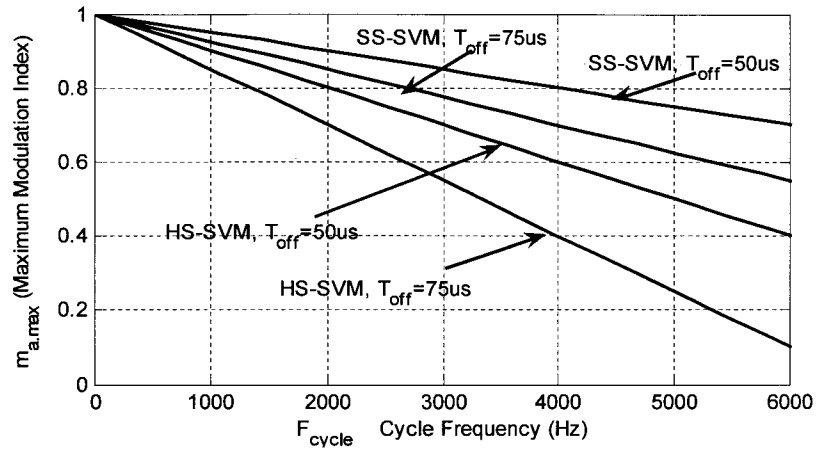
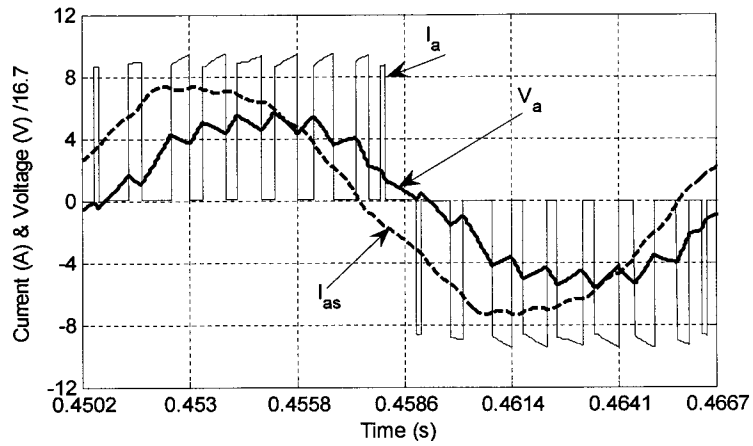


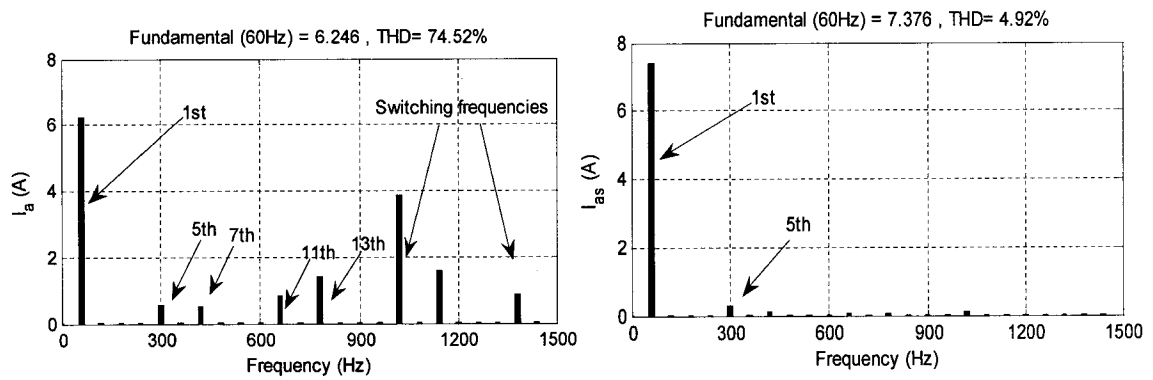
Fig. 8- 5 :-  $m_{a,max}$  VS  $f_{cycle}$  at different  $t_{off,min}$  for HS-SVM and SS-SVM techniques.

## 8.5. SIMULATION AND EXPERIMENTAL RESULTS

A simulation and experimental study was conducted for the HCSC with SS-SVM,  $N_{CS} = 3$  and chapter 7 system specifications. Fig. 8- 6 shows the simulation results for waveforms and harmonic spectra for the HCSC operating with SS-SVM. The  $m_a = 0.7$  and  $\text{PF} = \cos 10^\circ$  leading to avoid the key voltage relations to change inside the SVM cycle thus preventing commutation failure as described previously. There the waveform of  $I_a$  does not present the double switching pulsed in the middle of the positive and negative semi-cycles as it was in HS-SVM, reflecting the potential for reduced switching losses of this technique. The waveforms of the HCSC with SS-SVM are similar to those of the 6-switches SVM-CSC with three segment, regarding shape and harmonics components. With the same operating conditions results were taken in Fig. 8- 7 from the experimental set-up shown in Fig. 7- 11. Both theoretical and experimental results for HCSC with SS-SVM are similar to each other.

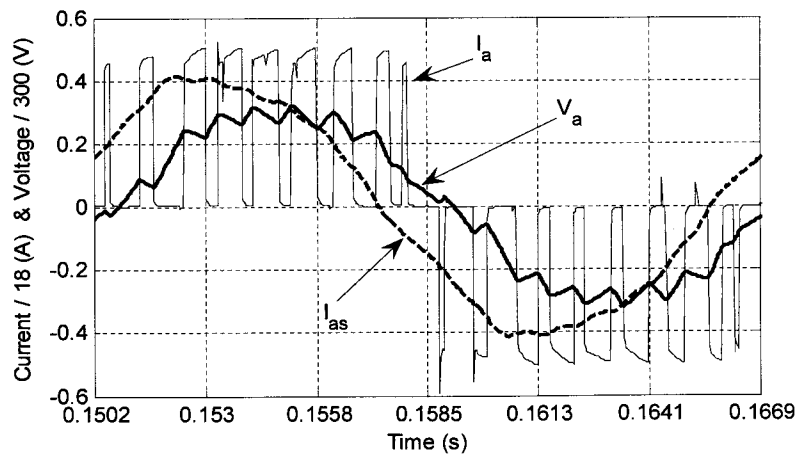


(a) Waveforms.

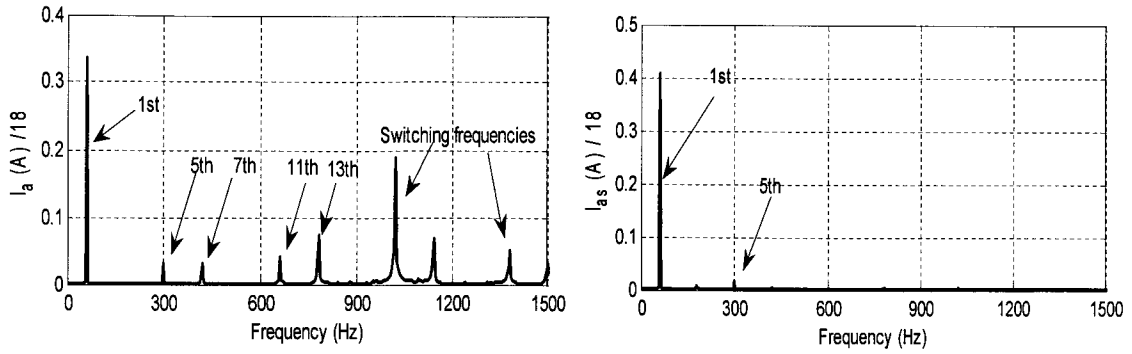


(b) Harmonic spectra.

Fig. 8- 6 :- Simulation results for HCSC with SS-SVM for  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $PF = \cos 10^\circ$ , leading.



(a) Waveforms.

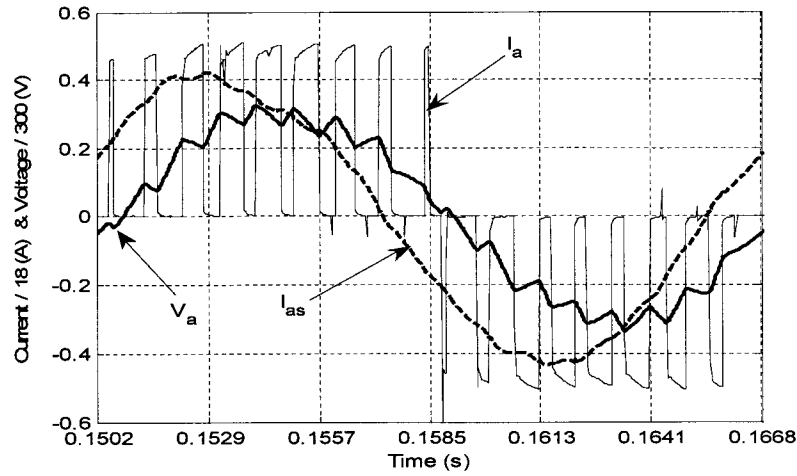


(b) Harmonic spectra.

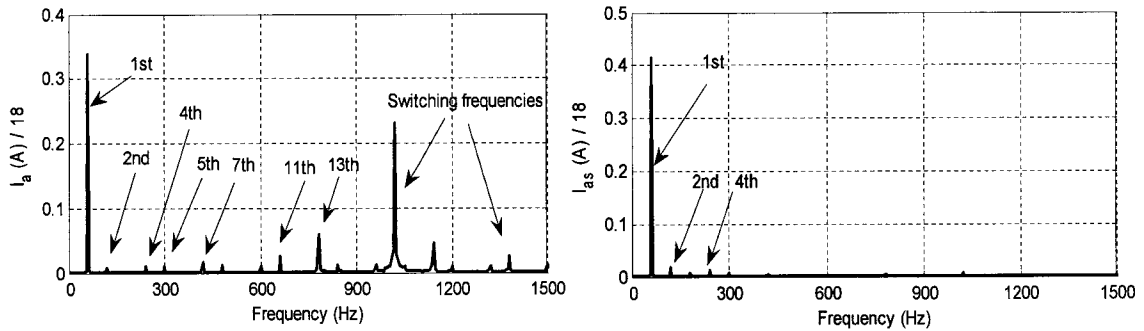
Fig. 8- 7 :- Experimental results for HCSC with SS-SVM for  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $PF = \cos 10^\circ$ , leading.

The impact of changing the sequence (up  $\leftrightarrow$  down) in SS-SVM to prevent commutation failures is verified next. This approach is not necessary in odd sectors, where there are no SCR commutations, but is used for the sake of waveform symmetry. A commutation failure implies that the firing of one SCR will not block another. The dc-side current will not be switched from a phase to another. Thus, a current pulse will be wider than it should (an SCR keeps conducting) in one phase and a pulse will be missed (an SCR is fired but does not latch on) in another phase. Since the SCRs are placed in the bottom part of the bridge, the negative semi-cycle of the currents will be affected. There will be no change in the current waveforms in the positive semi-cycles, since an IGBT will keep conducting as usual. Thus, the current waveforms lose the half-wave symmetry, which generate even harmonics. This is seen in Fig. 8- 8 obtained for  $m_a = 0.7$ ,  $PF = \cos 10^\circ$  leading and SS-SVM using only the down sequence where the last pulse of the negative semi-cycle of the waveforms, which should have been created using the up sequence, is missing.





(a) Waveforms.



(b) Harmonic spectra.

Fig. 8- 8 :- Experimental results for commutation failure with down sequence in all SVM cycles for HCSC with SS-SVM for  $m_a = 0.7$ ,  $N_{CS} = 3$  and  $PF = \cos 10^\circ$ , leading.

In Fig. 8- 8 (a), the third pulse of current in the current negative half cycle becomes wider. If the shape of the pulses in the positive and negative ac-side current half cycles is not the same, half wave symmetry is lost. Regarding the harmonics spectrum in Fig. 8- 8 (b), the even harmonics like 2<sup>nd</sup> and 4<sup>th</sup> are appearing because the half wave symmetry is lost.

The effect of step changes in both  $P_{ref}$  and  $Q_{ref}$  is illustrated in Fig. 8- 9. There the operating conditions are varied from  $P_{ref} = 400$  W and  $Q_{ref} = 0$  VAR to  $P_{ref} = 300$  W and

$Q_{ref} = -300$  VAR (leading) and vice-versa every 0.1s. The first window shows the active power  $P_{ref}$ . The second window shown both of the required reactive power  $Q_{ref}$  and the actual one ( $Q_a$ ). The third window shows  $I_{dc}$ , it has acceptable transient performance. The selected  $\delta_a$ , one angle from the  $\delta_{a(n)}$  array group of angles available in (8- 1) is changing during transient periods and the available reactive power  $Q_a$  is adjusted after the transient periods of  $I_{dc}$  are ended. The difference between  $Q_{ref}$  and  $Q_a$  in steady state operation is affected by the value of  $P_{ref}$ . When  $P_{ref} = 300$  W then  $Q_a \approx -330$  VAR is the actual value of reactive power which is close to  $Q_{ref} = 300$  VAR , while when  $P_{ref} = 400$  W then  $Q_a \approx 20$  VAR is the actual value of the reactive power which is close to  $Q_{ref} = 0$  VAR.

The fourth window is split into two, each one illustrates whether up or down sequence is used in each SVM cycle for both operating conditions during one ac-side current line cycle. When up (down) sequence is used the SIMULINK logic give one (zero). There, the left hand side is for  $Q_{ref} = 0$ VAR and  $P_{ref} = 400$ W case, up sequence is used all the time. While the right hand side is for  $Q_{ref} = -300$ VAR (leading) and  $P_{ref} = 300$ W, this one is the case presented in Fig. 8- 2, the angle between  $V_a$  and  $I_a$  is  $10^\circ$  leading and the down sequence is used for the first two SVM cycles while the up sequence is used for the last SVM cycle.

The fifth window is split into two, there  $V_a$ ,  $m_a$  and  $I_a$  for phase A are shown for each case, one can note the effect of sequence variation in  $I_a$ . Both of  $V_{as}$  (dotted) and  $I_{as}$  (soled) are shown in window six for a complete period (0.3s). In the last window  $V_{as}$  (dotted) and  $I_{as}$  (soled) for each case are presented. There in the left hand side one can note that the exact UPF is not obtained.

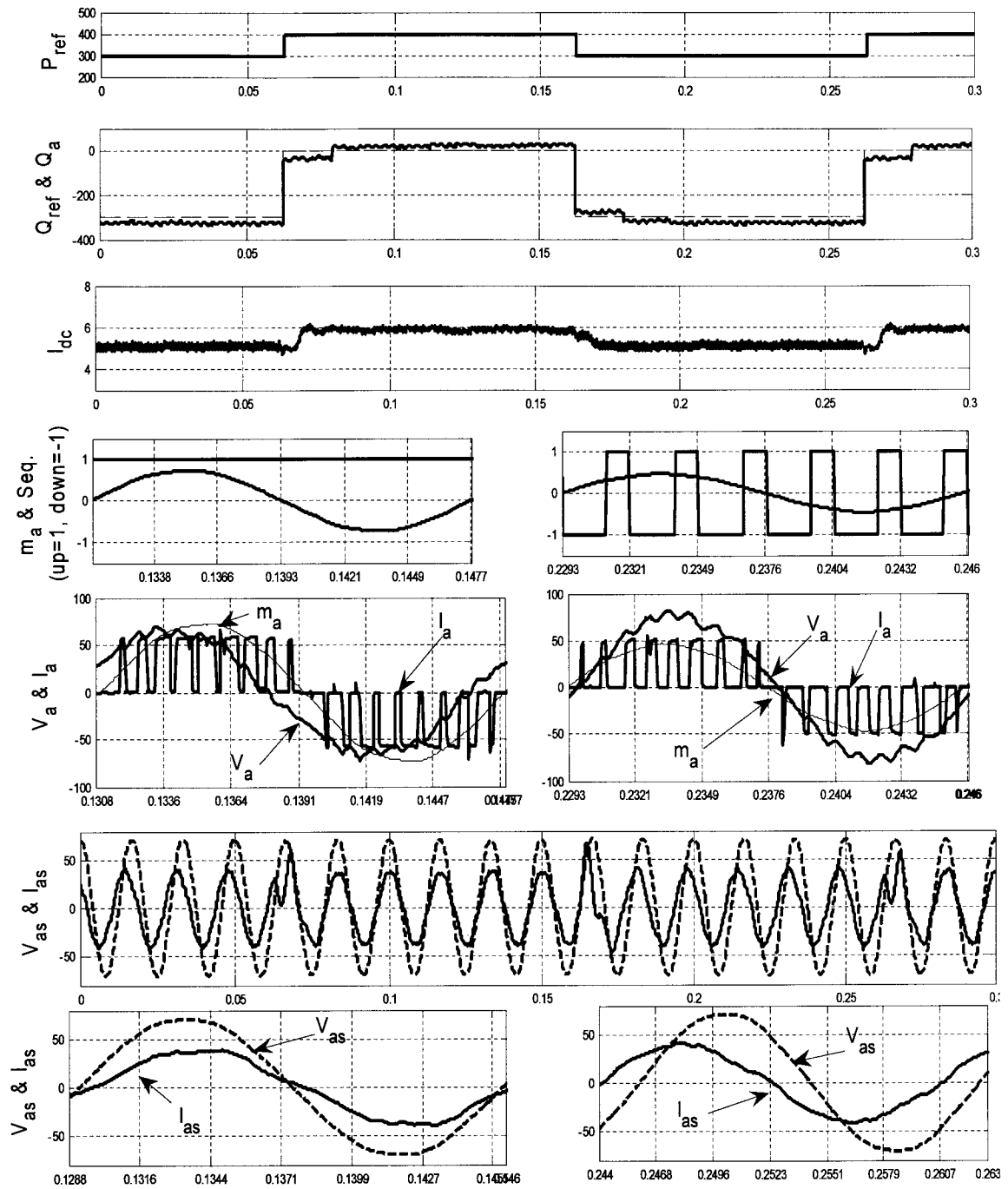


Fig. 8- 9 :- The effect of  $P_{ref}$  and  $Q_{ref}$  variations in HCSC with SS-SVM.

## 8.6. CONCLUSION

A SS-SVM technique suitable for the HCSC employs three SCRs four IGBTs is proposed in this chapter. With SS-SVM, the HCSC presents a performance level equivalent to that of conventional 6-switches SVM-CSC in terms of flexibility and harmonic distortion. While the HCSC topology reduces the number of force-commutated switches required for the converter, the proposed SS-SVM scheme reduces the number of switches commutations and makes some of them soft-switching.

The gating signal generation scheme needs to be more sophisticated for dealing with the commutation issues of SCRs. It considers the instantaneous voltages at the input of the HCSC and the desired PF to determine the order of the active states in a three segment sequence which allows at least one soft-switching commutation in SVM cycle. The proposed SS-SVM increases the maximum gain of the HCSC and reduces the non-characteristic current LOH appears in HCSCs operating with HS-SVM and LSFs.

The drawback of the proposed SS-SVM scheme is that the angle between current and voltage cannot be varied continuously. The step size is defined by the number of cycles per sector used in the SVM and the maximum angle error is equal to  $10^\circ$  for SVM with three cycles per sector. So, active and reactive power cannot be controlled independently. And, one can choose to create a reference current vector with  $P_{ref}$  while accepting an error in  $Q_{ref}$ . Experimental verification support SS-SVM concept, that include commutations success and failure results, beside the possibility of changing the sequence with different PF.

## CHAPTER 9

### 9. COST ANALYSIS

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#### 9.1. INTRODUCTION

The proposed HCSC topology can replace the widely used 6-switches CSC topology if it is less costly in both establishing (capital) and life time losses points of view at a certain power range. The proposed topology concepts and modulation process presented till now are not sufficient. HCSC is less costly than traditional CSC in establishing cost point of view, since one SCR is cheaper than an IGBT plus its series diode with the same power rating [63], [73] - [75]. Nevertheless, that should also be investigated since both topologies semiconductors need drives and heat sinks. But, what needs to be investigated more is the power loss in each device inside the topology and power losses for the whole topology as well, which may affect the power rating of selected devices, the heat sink sizes and the cost for the entire life of the topology.

In the previous chapters, it has been shown that a reduction in the number of switches from 6 to 4 for a flexible bi-directional CSC can be achieved at the expense of an increment in the switching losses of the remaining switches. The increment, per switch, was of 100% for the HS-SVM and roughly 33% for the SS-SVM. This should lead to higher switching power losses on the switches. One should prove that the overall cost saving still exists in the worst operating conditions appearing at certain PF for HCSC. Power losses for each device in HCSCs should be less than the same device in the traditional 6 switches CSC to present lower rating components and smaller heat sinks.

Besides, the complete topology power losses should be lower to compete in the high efficiency class.

Few publications deal with thermal calculations for losses in IGBTs switches, most of those considering VSC [87]. Minimizing the losses in 6-switches CSC was presented in [88]. A preliminary trial to calculate losses in CSCs was presented in [89]. Comparison from a cost point of view between CSI and VSI linked with dc/dc boost converters was presented in [90]. Also, important hints for the difference between VSC and CSC calculation process in both conduction and switching losses was presented in [91], but the modulation technique effect on power losses calculation was not considered.

## 9.2. GENERAL ECONOMICAL FORMULA

Table 9- 1 shows the difference between traditional CSC and HCSC for each device using components count. There negative (positive) sign means that there is a saving (adding) component in HCSC for this device. The heat sink size depends on losses which are represented by heat, not included in Table 9- 1. HCSC is economically effective if (9- 1) is satisfied.

TABLE 9- 1 :- CAPITAL COST COMPARISON BETWEEN 6-SWITCHES CSC AND HCSC.

Comparison Criteria	IGBT (T)	SCR (R)	Diode (D)	IGBT drives (TD)	SCR drives (RD)
6-switches CSC	6	0	6	6	0
HCSC	4	3	4	4	3
Difference	-2	+3	-2	-2	+3

Cost (2T + 2D + 2TD + CSC heat sinks) >> Cost (3SCR + 3RD + HCSC heat sinks) (9- 1)

### 9.3. POWER LOSSES CATEGORIES

The power losses for semiconductor devices are conduction and commutation (switching) losses. The modulation technique has a significant impact on the switching stress and losses on the semiconductor devices. Besides, the modulation technique for HCSC changes the conduction losses as well as switching losses, not the case in 6-switches CSC.

The pulses number per ac-side line cycle and conduction period for each device is used for a preliminary estimation for the switching and conducting stress on the converter. The power losses at a certain power range should be calculated with worst case losses for the selection of the semiconductors and cooling element required to keep the junction temperature below a specified value.

Let's select a high power range where one single IGBT can be used. It is worth mentioning that usually in extra high power applications IGBTs are connected in series/parallel as presented in [77]. For around 1700V/1100A, Table 9- 2 is showing for selected devices datasheet information required in power losses analysis at certain operating conditions [92]. Selected devices are changed with power rating. Even in the same power rating one can select different components with different datasheet information, which resulted from different manufacturer and semiconductor design technology. Here a procedure to calculate conduction and switching power losses for each device in traditional SVM-CSC and HCSC with HS-SVM and SS-SVM is presented.

TABLE 9- 2 :- DATASHEET INFORMATION FOR SCR, DIODE AND IGBT USED IN HCSC.

Rated power	(1700V/1100A)	Proposed Operating conditions $di/dt=100A/\mu s$ and $(1200V_{max}/800A)$
IGBT	CM1200HA-34H	<b>IGBT</b>
Exact rating	1700V/1200A	
$V_{DS,0}$ [V]	1.5 V	The least IGBT drain source forward voltage
$R_{DS}$ [m $\Omega$ ]	1.05 m $\Omega$	The equivalent IGBT series resistance between drain and source
$V_{DS}$ [V]	2.34 V (800A)	The forward IGBT drain source voltage at selected current
$E_{on}$ [mJ]	300 mJ (800A)	Switching ON power losses of IGBT at selected current
$E_{off}$ [mJ]	330 mJ (800A)	Switching OFF power losses of IGBT at selected current
Diode	F1400NC180	<b>Diode</b>
Exact rating	1800V/1093A	
$V_{F,0}$ [V]	1.62 V	The least diode anode to cathode forward voltage drop
$r_F$ [m $\Omega$ ]	0.39 m $\Omega$	The equivalent diode series resistance between anode and cathode
$V_F$ [V]	1.93 V (800A)	The diode anode to cathode forward voltage drop at selected current
$E_{d,rec}$ [mJ]	75 mJ (800A)	The diode reverse recovery energy at selected current, $di/dt=100A/\mu sec$
SCR	R1448NS18H	<b>Thyristor (inverter grade with low conduction power losses)</b>
Exact rating	1800V/1448A	
$V_{AK,0}$ [V]	1.3 V	The least thyristor anode to cathode forward voltage drop, threshold voltage
$r_{AK}$ [m $\Omega$ ]	0.25 m $\Omega$	The equivalent thyristor series resistance between anode and cathode
$V_{AK}$ [V]	1.5 V (800A)	Thyristor anode to cathode forward voltage drop at selected current
$E_{t,rec}$ [mJ]	85 mJ (800A)	The thyristor reverse recovery energy at selected current, $di/dt=100A/\mu sec$
$t_q$	40 $\mu s$	Thyristor turn off time

Different of components for 1700V/1100A power range are investigated, there one can find the following.  $V_{DS,0}$  for IGBT,  $V_{F,0}$  for diode and  $V_{AK,0}$  for SCR are around 1.5V ( $\pm 0.25V$ ). The equivalent series resistance for diodes and SCRs are around 0.3m $\Omega$



( $\pm 0.1\text{m}\Omega$ ). That is one quarter of IGBT's equivalent series resistance which is around  $1.2\text{m}\Omega$  ( $\pm 0.2\text{m}\Omega$ ). Also, turn-on power losses for diodes and SCRs are neglected. Turn-off power losses for SCR are around two times those of a diode, inverter grade SCR have less voltage drop and turn-off power losses than phase controlled SCRs and selected diode showing somehow high switching losses and voltage drop ratings. IGBTs have nearly equal turn-on and turn-off power losses each is from four to five times as much as the turn-off losses for diodes.

#### **9.4. CONDUCTION POWER LOSSES**

CSCs require switches capable of blocking reverse voltage, which are implemented with a diode in series with an IGBT. As a result, the conduction losses in CSCs, where the dc-side current always flow through 4 semiconductors, 2 IGBTs and 2 diodes, is higher than VSCs where current pass through two semiconductors devices [91].

Since the SCR voltage drop is lower than turn-off devices in the medium voltage range due to high forward IGBTs equivalent resistance [93], HCSC should compare favorably with respect to the 6-switches CSC on conduction losses. There dc-side current is passing through IGBT, diode and SCR, while in traditional topology it is passing through 2 IGBTs and 2 diodes.

It is assumed that the dc-side current can be adjusted between 0A and 800A with  $0 < m_a < m_{a,\text{max}}$  in HS-SVM, that is  $0 < m_a < 0.78$  with  $t_q = 40\mu\text{s}$  for the selected SCR. That permits HCSC with HS-SVM to operate properly for  $N_{\text{CS}} = 3$ . In 6-switches CSC each IGBT conduction period do not depend on the modulation technique or  $m_a$ , each conduct current for 1/3 of the line cycle, Fig. 7- 6 illustrates the gating pulses for upper switches group. Conduction power losses for each IGBT plus its series diode is

$$P_{\text{cond-IGBT-D}} = \frac{1}{3} I_{\text{dc}} [(V_{\text{DS},0} + r_{\text{DS}} I_{\text{dc}}) + (V_{\text{F},0} + r_{\text{f}} I_{\text{dc}})] \quad (9-2)$$

In HCSC, freewheeling switch (S7) should be used to implement a zero state at certain cases and the conduction period for IGBTs vary with the SVM strategy and  $m_a$ , this was presented in previous chapters. In power losses analysis zero state duration as an average from (1- 4), (1- 5) and (1- 6) is in (9- 3).

$$t_z = t_{\text{cycle}}(1 - 0.95m_a) \quad (9-3)$$

In HS-SVM each bridge IGBT conducts the dc-side current for 1/3 of the line cycle minus 1/6 of the zero states. While, the free-wheeling switch conducts for 1/2 of the zero states. The conduction power losses for freewheeling and bridge IGBT plus their series diodes are calculated in (9- 4) and (9- 5), respectively. While, for each SCR the conduction power losses is calculated using (9- 6).

$$P_{\text{cond-FW-D}} = \frac{(1-0.95 m_a)}{2} I_{\text{dc}} [(V_{\text{DS},0} + r_{\text{DS}} I_{\text{dc}}) + (V_{\text{F},0} + r_{\text{f}} I_{\text{dc}})] \quad (9-4)$$

$$P_{\text{cond-IGBT-D}} = \frac{(1+0.95 m_a)}{6} I_{\text{dc}} [(V_{\text{CE},0} + r_{\text{CE}} I_{\text{dc}}) + (V_{\text{F},0} + r_{\text{f}} I_{\text{dc}})] \quad (9-5)$$

$$P_{\text{cond-SCR}} = \frac{(1+0.95 m_a)}{6} I_{\text{dc}} [(V_{\text{AK},0} + r_{\text{AK}} I_{\text{dc}})] \quad (9-6)$$

In SS-SVM the conduction losses of the bridge IGBTs and SCRs are slightly decreased while those of the free-wheeling switch are slightly increased due to the use of the free-wheeling switch to implement the first zero state in all sectors. When  $N_{\text{CS}} = 3$ , each bridge IGBT conducts the dc-side current for 1/3 of the line period minus 2/9 of the zero states. While, the free-wheeling switch conducts dc-side current for 2/3 of the zero states. The conduction power losses for freewheeling and bridge IGBT plus their series diodes are calculated in (9- 7) and (9- 8), respectively. While, for each SCR conduction power losses is calculated using (9- 9).

$$P_{\text{cond-FW-D}} = \frac{(2-1.9 m_a)}{3} I_{\text{dc}} [(V_{\text{DS},0} + r_{\text{DS}} I_{\text{dc}}) + (V_{\text{F},0} + r_{\text{f}} I_{\text{dc}})] \quad (9-7)$$

$$P_{\text{cond-IGBT-D}} = \frac{(1+1.9 m_a)}{9} I_{\text{dc}} [(V_{\text{CE},0} + r_{\text{CE}} I_{\text{dc}}) + (V_{\text{F},0} + r_{\text{f}} I_{\text{dc}})] \quad (9-8)$$

$$P_{\text{cond-SCR}} = \frac{(1+1.9 m_a)}{9} I_{\text{dc}} [(V_{\text{AK},0} + r_{\text{AK}} I_{\text{dc}})] \quad (9-9)$$

Table 9- 3 is presenting the conduction losses for SVM-CSC and HCSC with HS-SVM and SS-SVM when IGBTs, diodes and SCRs specified in Table 9- 2 are used. There, the largest power losses for the HCSC topology as well as bridge components appears when  $m_{a,\text{max}} = 0.78$ . The worst conduction losses for the freewheeling IGBT is at another  $m_a$ , when  $\frac{(1-0.95 m_a)}{2} I_{\text{dc}}$  is maximum depending on (9- 4) and (9- 7). Which appears when  $m_a = 0.53$  and  $I_{\text{dc}} = 543.6\text{A}$ , there conduction power losses for freewheeling IGBT plus its series diode is 576.5W in HS-SVM and 768.7W in SS-SVM. From this analysis, one can conclude that the conduction power losses in any IGBT plus its series diode in HCSC are less than those of 6-switches CSC. And, total conduction losses for HCSC are less than those of traditional one SVM-CSC.

TABLE 9- 3 :- CONDUCTION POWER LOSSES FOR EACH SCR, DIODE, IGBT AND FOR THE WHOLE TOPOLOGY.

Topology	Conduction (W)				Total conduction loss (W)
	Bridge switch	Free-wheeling		SCR	
$m_{a,\text{max}} = 0.78$	$m_{a,\text{max}}$	$m_{a,\text{max}}$	Worst	$m_{a,\text{max}}$	$m_{a,\text{max}}$
6-switches CSC	1139.2	-	-	-	6835.2
HS-SVM (HCSC)	991.7	442.6	576.5	348.2	4462.2
SS-SVM (HCSC)	942.5	590.1	768.7	330.9	4410.4

## 9.5. COMMUTATION (SWITCHING) POWER LOSSES

From Table 9- 2, one can conclude that IGBTs switching power losses are dominant if compared to SCRs or diodes. Calculation of the switching power losses of IGBT should be accurate, 90% of switching losses in traditional CSC and HCSC appears in IGBTs. An important issue should be presented to understand how commutation losses are calculated either in 6-switches CSC or in the proposed HCSC. Since in both topologies the upper devices are IGBTs connected in series with diodes, let's present what will happen when SVM is used and the vector position is in sector one for either 6-switches CSC or HCSC (not including the first state in each sector in SS-SVM which implemented with S7). That was presented in Fig. 1- 3 for SVM-CSC and Fig. 7- 3 for HCSC. There, the lower switching device S2 (SCR in HCSC or IGBT in 6-switches) is conducting current in entire sector. While, a switching between two of three upper IGBTs (S1 ( $I_i$ ), S3 ( $I_{i+1}$ ) and S5 ( $I_z$ )) take place when the state is changed.

A mandatory overlap period is required to ensure that there is a dc-side current path during states transition. During this commutation period, there are always two IGBTs involved. Their commutation voltage will always be one of the line voltages. The commutation from one state to the other appears either in the beginning or the end of the overlap period. In the beginning, if the IGBT being turned ON (belonging to the state following the overlap period) is more forward biased than the IGBT being turned OFF (belonging to the state before the overlap period), that leads the turned OFF IGBT to be turned OFF with zero current (softly) without any turn-off switching power losses. And, in the end, if the IGBT being turned ON is less forward biased than the IGBT being

turned OFF. That leads the turned ON IGBT to start conducting current with zero voltage (softly) without any turning ON switching power losses in the end of the overlap period.

In other words, in odd sectors where upper IGBT conducting current is changing each state transition, if the phase voltage of the switch which will be turned ON is more positive than the other one that will be turned OFF, then, losses are generated in the turned ON IGBT and the turning OFF will be softly. While, if the phase voltage of the switch which will be turned OFF is more positive than the other one that will be turned ON, then, losses is generated in the turned OFF IGBT and the turning ON will be softly.

Let's discuss what happens to series diodes. Turn ON losses for diodes are neglected. During turn OFF, when the IGBT in series with the diode turning OFF power losses appears there will be no opportunity to the diode to recover with negative current, since this phase is more forward than the other involved in the commutation. If the phase voltage of the switch that is to be turned OFF is less positive than the one turned ON the switch turn-off softly, while reverse current is injected into its series diode and become forward current in IGBT anti-parallel diode. That leads to recover the series diode with turn OFF power losses. Turn OFF power losses for series diodes appear only when there is no turn OFF power losses in the IGBTs during turning OFF.

Two procedures are available in calculating switching losses in converters, simulation and average calculations. Average calculations were done before in [91] for 6-switches CSC. There is a complexity appears in switching losses average calculations for CSC compared to VSC [90], [91]. That includes the soft switching probability issue and instantaneous line to line voltage effect during switching. Simulations used before for the estimation of switching losses for VSC [94], less research deals with CSCs in general.

The derivation of an accurate expression using average calculation for the switching losses of the HCSC is complicated without solid references or guidelines from 6-switches CSC. Average calculation will be used to prove that the simulation procedure for losses calculations in 6-switches CSC has good accuracy. That simulation concept will be extended to HCSC and compared with average calculations for IGBTs in HCSC to be confident of the results. Since switching losses for IGBTs is dominant, only simulation is used in SCRs. Also, UPF is used for switching power losses. UPF operation (either rectifier or inverter) generates the highest switching power losses in HCSC as we will note later.

### **9.5.1. AVERAGE CALCULATIONS FOR SWITCHING POWER LOSSES**

In 6-switches CSC, average calculations is done by assuming that the turn-on and turn-off energies of the IGBTs vary linearly with the commutation voltages [91]. In average analysis it is proposed that the switching frequency is high, can be used in LSF with error. In 3-segment with 3-transitions SVM-CSC, independent on the PF each of the 3-line voltages affects one of those 3-transitions. Turn-on and turn-off losses are equally weighted for the calculation of the total switching losses, that is available in even  $N_{CS}$  while giving slight error in odd  $N_{CS}$  because  $E_{on} \neq E_{off}$ . Since the difference between  $E_{on}$  and  $E_{off}$  is small, that can be neglected. Thus, 1/3 of the sum of absolute 3-line voltages over one SVM sector ( $60^\circ$ ) is proportional to the average switching losses regardless of the PF at the CSC input, that is  $\left[ \int_0^\pi |V_{AB}| + |V_{BC}| + |V_{CA}| = \frac{6}{\pi} \times \widehat{V}_{line} \right]$ , 1/3 of this value is  $\left[ \frac{2}{\pi} \times \widehat{V}_{line} \right]$ , which is used in calculating the average switching losses for each switch. Each switch in CSC is presenting  $3N_{CS}$  switching pulses. Proposing that half of those is

presenting  $E_{on}$  while other half is presenting  $E_{off}$ . Then, one can calculate the switching energy losses for IGBT and its series diode using (9- 10). Also, an expression for the switching power losses of one IGBT and its series diode is given in (9- 11) using (9- 10) with (1- 3). From (9- 11) with  $f_{cycle}=1080\text{Hz}$  and Table 9- 2 one can find that  $P_{sw-IGBT-D} = 85.54 \text{ W}$ , and  $P_{CSC} = 513.24\text{W}$  for the whole topology.

$$E_{sw-IGBT-D} = \frac{3N_{cs}}{2} \times \frac{2}{\pi} \times (E_{on-IGBT} + E_{off-IGBT} + E_{off-D}) \frac{I_{dc}}{I_{rated}} \frac{\hat{V}_{line}}{V_{rated}} \text{ J/cycle} \quad (9- 10)$$

$$P_{sw-IGBT-D} = \frac{f_{cycle}}{2\pi} (E_{on-IGBT} + E_{off-IGBT} + E_{off-D}) \frac{I_{dc}}{I_{rated}} \frac{\hat{V}_{line}}{V_{rated}} \text{ W} \quad (9- 11)$$

$$P_{sw-IGBT-D} = \frac{1080}{2\pi} (0.3 + 0.33 + 0.075) \frac{1200}{1700} = 85.54 \text{ W} \quad (9- 12)$$

The previous procedure for SVM-CSC is done with help of [91]. In HCSC the calculations procedure is done in a similar way, but it is complex. Average losses calculations will be done for IGBTs and their series diodes, 95% of switching losses. With HS-SVM there are four transitions per SVM cycle. The switching is always between two IGBTs, both from the bridge in odd sectors, and one from the bridge while the other is the freewheeling one in even sectors. When the transition of states is between bridge and freewheeling IGBTs in even sectors, there will be, in addition, a SCR turn-off.

In  $I_1$  to  $I_2$  transition, or vice-versa, there is a line voltage involved. Also, in  $I_{i+1}$  to  $I_2$  transition, or vice-versa, there is another line voltage involved. Unlike the case of SVM-CSC where all three line voltages are involved in commutation, which simplifies the voltages summation, only two line capacitor voltages are involved in the commutation in HS-SVM. The third voltage will not be effective. In sector zero, as an example, both  $|V_{AB}|$  and  $|V_{CA}|$  are involved. The maximum voltage summation for involved line voltages should be considered as the worst case, since the power losses are

dependent on the voltage values. That occurs when  $|V_A|$  maximum, which appears in the middle of sector zero. That takes place when  $\phi_v$  and  $\phi_I$  are in phase. That occurs at UPF, check Fig. 8- 2.

Fourier series is utilized to represent the mean value of the sum of the commutation voltages. Thus, the summations of those two voltages involved in commutation depend on the PF and can be calculated in (9- 13) with the largest value at UPF ( $\theta = 0$ ) calculated in (9- 14). Energy loss is presented in (9- 15), recall that half switching losses are resulted from turn-on while the other half resulted from turn-off, there are  $6N_{CS}$  switching for bridge IGBTs per ac-side line cycle. Maximum switching losses for each IGBT and diode with  $6N_{cs}$  switching can be calculated in (9- 16). With  $f_{cycle}=1080\text{Hz}$  and Table 9- 2, one can find that  $P_{sw-IGBT-D} = 222.4\text{W}$  and for four IGBTs and four diodes in HCSC  $P = 889.6\text{W}$ .

$$|V_{AB}| + |V_{CA}| = \frac{3}{\pi} \times \widehat{V}_{line} \left( \frac{4}{3} - \frac{8}{\pi} \sum_{k=2}^{\infty} \frac{\cos[k(\frac{\pi}{2}+\theta)]}{(k^2-1) \times k} \sin\left(k\frac{\pi}{3}\right) \right) \quad \text{Volt} \quad (9- 13)$$

$$|V_{AB}| + |V_{CA}| = 1.73 \times \frac{3}{\pi} \times \widehat{V}_{line} \quad \text{Volt} \quad (9- 14)$$

$$E_{sw-IGBT-D} = \frac{6N_{cs}}{2} \times 1.73 \times \frac{3}{2\pi} \times (E_{on-IGBT} + E_{off-IGBT} + E_{off-D}) \frac{I_{dc}}{I_{rated}} \frac{\widehat{V}_{line}}{V_{rated}} \quad \text{J/cycle} \quad (9- 15)$$

$$P_{sw-IGBT-D} = \frac{5.2 \times f_{cycle}}{4\pi} (E_{on-IGBT} + E_{off-IGBT} + E_{off-D}) \frac{I_{dc}}{I_{rated}} \frac{\widehat{V}_{line}}{V_{rated}} \quad \text{W} \quad (9- 16)$$

### 9.5.2. SWITCHING POWER LOSSES WITH SIMULATION RESULTS

The proposed simulation procedure is correct if the results achieved there are similar to the results presented for average calculations in (9- 11) SVM-CSC and (9- 16) for IGBTs in HCSC with HS-SVM. Moreover, since simulation results are depending on



the instantaneous voltage value instead of the average one, it will be considered more accurate than average calculation, if both have similar results.

It is important to detect the instants when S1 is switching either ON or OFF to simulate the switching losses for S1. Then, one needs to check the voltage polarity between phase A and the other phase involved in the commutation process. If phase A voltage is higher during switching a power losses proportional to line voltage is added to S1 switching power losses, if not, no switching power losses appears on S1. Fig. 9- 1 illustrates how switching losses in S1 can be simulated when S1 is turned off and S3 is turned on. The same should be done for other switching from or to S1. Then, all losses for S1 are added together in one ac-side line cycle by accumulative procedure. The step time in the simulation should be fixed and less than  $1\mu\text{s}$ . In the beginning of the ac-side current line cycle, not including filter, the integrator is reset to calculate energy losses in each ac-side line cycle. The switching power losses are finally converted from m Jole/ac cycle to Watt.

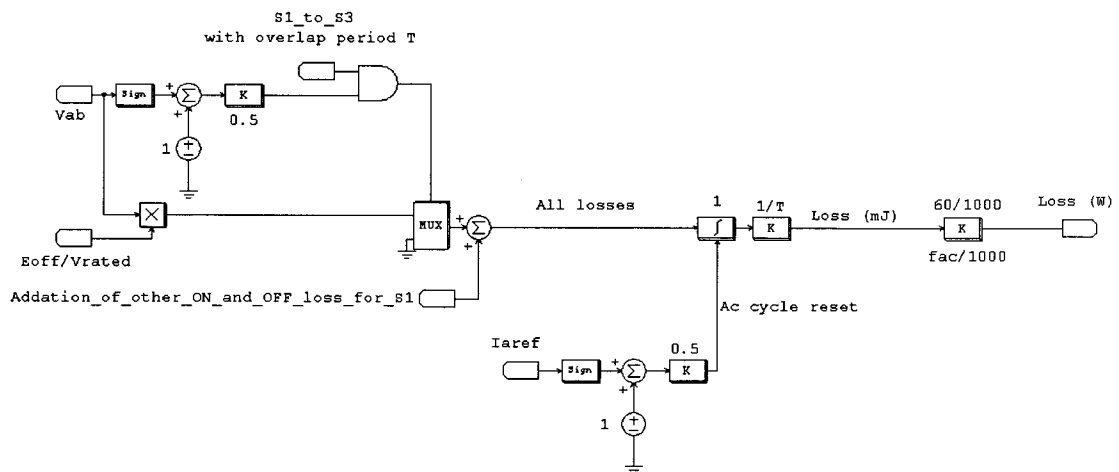


Fig. 9- 1 :-Simulation procedure to calculate S1 switching power loss.

Fig. 9- 2 is presenting the switching losses of S1 (IGBT 1), D1 (diode 1) and the upper half CSC leg for phase A (IGBT 1 plus diode1) in the first window. In the second window, the gating signals of the top switches of the six switches SVM-CSC are shown. The last window shows the ac-side reference current ( $I_{a.ref}$ ), smothered phase A capacitor line to line voltages ( $V_{AB}$  and  $V_{AC}$  waveforms). S1 switch in odd sectors is presenting commutation losses in sector five and sector one, as expected, but not in sector three. This can be explained by taking into consideration the switches and the line voltages involved in the commutations during overlap period with S1. In all sectors, S1 is followed by S3 followed by S5. The turn-on commutation for S1 is from S5 to S1. Therefore, turn-on losses should appear on S1 when  $V_{AC} > 0$ , (sector one and second half of Sector five). And, turn-off losses for S1 occur in transitions from S1 to S3. Therefore, turn-off losses occur when  $V_{AB} > 0$  (sector five and first half of sector one). This is actually seen in Fig. 9- 2. It is interesting to see that S1 switches with no commutation losses in sector 3. That happens because  $V_{AC} < 0$  and  $V_{AB} < 0$  yielding turn-off losses in S5 and turn-on losses in S3 with no commutation losses for S1. IGBT switching losses is 78.14 W in one line cycle. Turn-on power losses For D1 are neglected. And, turn-off power losses appear when  $V_A$  is less than the other voltage involved in the commutation during S1 turn-off. This appears when  $V_{AB} < 0$ , second half of sector one and sector three. Fig. 9- 2 shows that D1 switching OFF losses are 8.86 W in one line cycle.

Finally, the switching losses obtained by simulation at the end of a line cycle for the addition of IGBT plus its series diode are 87W. That is close to what is obtained with the analytical expression in (9- 11), which is 85.54W what validates the simulation procedure. Also, the switching losses, if they appear, are proportional to the instantaneous

line voltage involved in the commutation process. And, around 90% of switching losses appears in IGBT while around 10% appears in series diode.

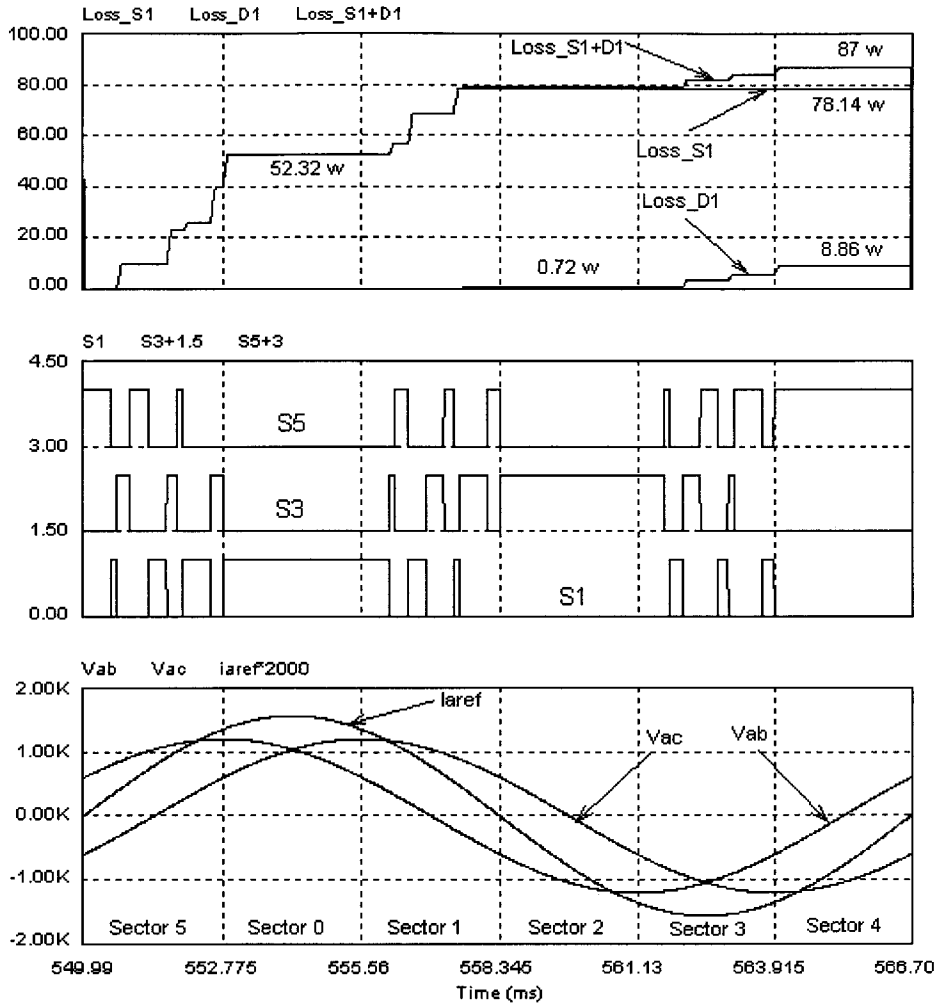


Fig. 9- 2:- Simulation results for the commutation losses for 6-switches SVM-CSC.  
 (a) Power losses in switch S1 and its series diode. (b) Gating signals for upper IGBTs  
 (c) Ac-side reference current and voltages waveforms.

Similar simulation procedure is used for HCSC, Fig. 9- 3 presents simulation results for the switching power losses of S1 (IGBT1), D1 (diode1) and the upper half CSC leg for phase A (IGBT 1 plus diode1) in the first window. In the second window,

the losses for S4 (SCR4), S7 (IGBT7), D7 (diode7) are shown. The third window shows the gating signals of all IGBTs and SCR 4. The last windows shows the ac-side reference current for phase A ( $I_{a,ref}$ ) and phase A lines voltages waveforms for the HCSC operating with HS-SVM and UPF.

To understand the switching losses results in HS-HCSC, it is worth recalling that HS-SVM employs a 4-segment sequence with the active states separated by zero states. Besides, the zero state is implemented by the free-wheeling switch in even sectors, and in the bridge, in odd sectors, as shown in Fig. 7- 7 and Fig. 7- 8. In the odd sectors commutations of switches involve elements of the bridge and are discussed first. The zero state is implemented through S3 in sector five, S1 commutates to and from S3. Thus, only the line voltage  $V_{AB}$  is the key voltage for defining the type of commutations of S1. When UPF is used,  $V_{AB} > 0$  in sector five and S1 is always (turn-on and turn-off) hard-commutated, that may not be the case for other PF. Recall from (9- 13) that UPF is the worst case for switching power losses. Despite presenting virtually the same gating signal with three pulses in sector five as in the 6-switch SVM-CSC, the accumulated commutation losses in S1 at the end of sector five are much larger than those in the 6-switches SVM-CSC presented in Fig. 9- 2. Conversely, in sector three where S1 is used twice per SVM cycle to realizes the zero state there is no losses on it, since  $V_{AB} < 0$  and  $V_{AC} < 0$  in that sector, meaning that the commutation losses will occur on either S3 or S5 and D1 have turn OFF power losses due to availability of a reverse recovery current.

The commutation losses calculation of S1 in sector zero where the free-wheeling switch (S7) implements the zero state is complicated. There, S1 realizes both active states with either S6 or S2. During the transition between an active state and the zero state, if

the involved line voltage ( $V_{AB}$  for S6 and  $V_{AC}$  for S2) is larger than zero, then S1 is hard-commutated while S7 is soft-commutated. With UPF  $V_{AB}$  and  $V_{AC}$  are larger than zero in sector zero and all commutations of S1 will be hard, And, S7 have zero switching power losses although switching pulses appear in sector zero. Based on this concept, zero switching power losses occur for S7 in sectors two and four. Also, S7 is not switching at all in odd sectors. That leads the switching losses for S7 to be zero. With UPF operation when S7 is turned off no power losses appear on it, while power losses appear in D7.

SCRs turn-on power losses are neglected. The commutation losses for SCRs are small compared to IGBTs, 5% of switching losses in HCSC. That is concluded from by fast comparison between  $E_{on}$ ,  $E_{off}$ ,  $E_{d,rec}$  and  $E_{t,rec}$  in Table 9- 2 and by noting that SCRs switching present 1/3 of the IGBTs switching in HS-SVM. Switching losses in HCSC are less than 20% from overall power loss in the considered power range. In short, SCRs present less than 1% from overall power losses. Inaccurate calculation of turn-off power losses for SCRs will not affect that much the overall power losses calculation accuracy.

SCRs safe commutation is depending on turn off the IGBT carry the current along with the SCR and waiting  $2.5t_q$  until charge carriers in PN junctions stop. But, the diode in the upper group is turning off with  $E_{d,rec}$  by injecting reverse current into the diode if its phase voltage is less positive than the one involved with in commutation during turn off. This current passing through the series diode in reverse direction and in the IGBT's ant-parallel diode in forward direction should pass also through SCR in reverse direction during SCRs turn off. The series diode is stopping this current path before SCR completely recover with partial recovery process for SCR. Also, the snubber circuit connected across the SCR discharges with RLC resonance phenomena and partial

recovery process. The worst case of turn off power losses are when SCR have power losses varying with the absolute value of its phase voltage, turn-off losses for SCR is less than that, but even if it is maximized that will not affect, 1% of losses appears from SCRs switching. S4 commutation power losses are presenting small magnitude in Fig. 9- 3

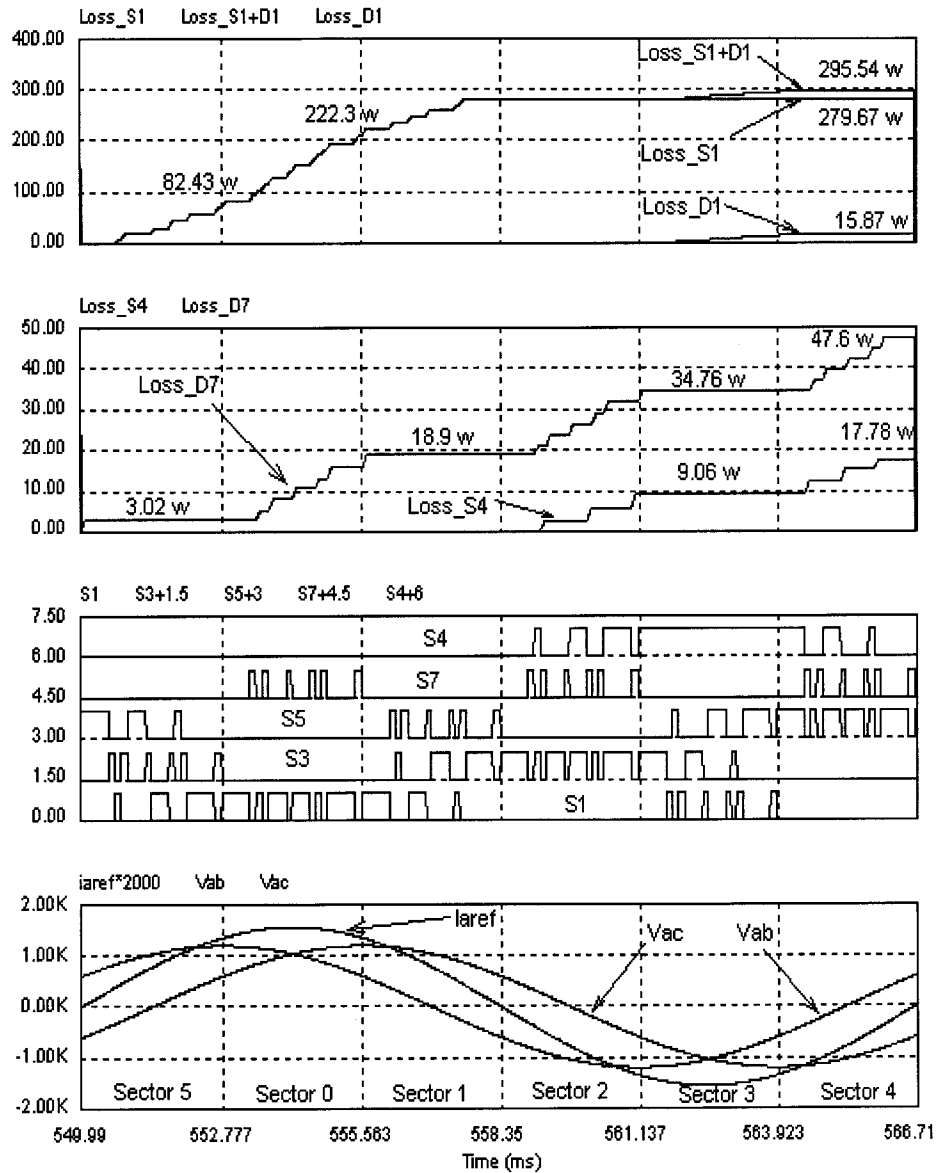


Fig. 9- 3:- Simulation results for commutation losses for HCSC with HS-SVM.  
a) Power losses in switch S1 and its series diode. b) Power losses in S4 and D7.  
c) Gating signals. d) Reference current and ac-side capacitor voltages waveforms.

It should be noted that operation at UPF corresponds to the worst case of commutation losses in the bridge switches and best, virtually zero, for the free-wheeling switch. From Fig. 9- 3, the commutation power losses in the HS-SVM with UPF are for S1 = 279.67W, for D1 = 15.87W, for S1+D1 it is 295.54W, zero for S7, for D7 = 47.6W and S4 = 17.78W. Commutation losses in S1 occur frequently with the final value higher than for the 6-switch SVM-CSC (279.67W), IGBTs losses dominate all other component losses. Simulation results in Fig. 9- 3 and average calculations in (9- 16) gives the same results. The average calculation for four IGBTs plus four diodes gives 889.6W switching power losses with UPF. Fig. 9- 3 losses for four IGBTs plus four diodes with UPF is  $(3 \times 295.54 + 47.6) = 934.2\text{W}$ , less than 5% error. This corresponds to a good agreement since the average calculation is based on the average voltage concept which is not accurate for operation with low  $N_{CS}$  like simulation results.

After become confident of the accuracy presented by simulation, it is used for SS-SVM. Fig. 9- 4 presents simulation results for the HCSC with SS-SVM and  $\text{PF} = \cos 10^\circ$ , leading. Recall that SS-SVM cannot operate with UPF when  $N_{CS}=3$ . Fig. 9- 4 gives results similar to Fig. 9- 3. The average calculation is repeated and it gives similar results to the simulation. The switching power losses of S1 are dominant here again. S1 switches in sectors zero, one and three, similar claims for losses in HS-SVM can be made for SS-SVM with less power losses resulting from less switching events. S1 switching losses appear during switching in sector zero, with relatively high power losses. Switching losses for S7 are zero when  $\text{PF} = \cos 10^\circ$  for the same reasons presented in HS-SVM, the small change in PF did not affect the voltage polarity during switching. In Fig. 9- 4 the number of commutations with losses as well as the total commutation losses in ac-side

current line period for S1 is between those obtained for the 6-switches SVM-CSC and the HCSC with HS-SVM. Switching losses in D1 appear only when its phase voltage is less than the commutated one during turn-off, as presented earlier. Switching losses in D7 appears less frequently due to a lower number of switching.

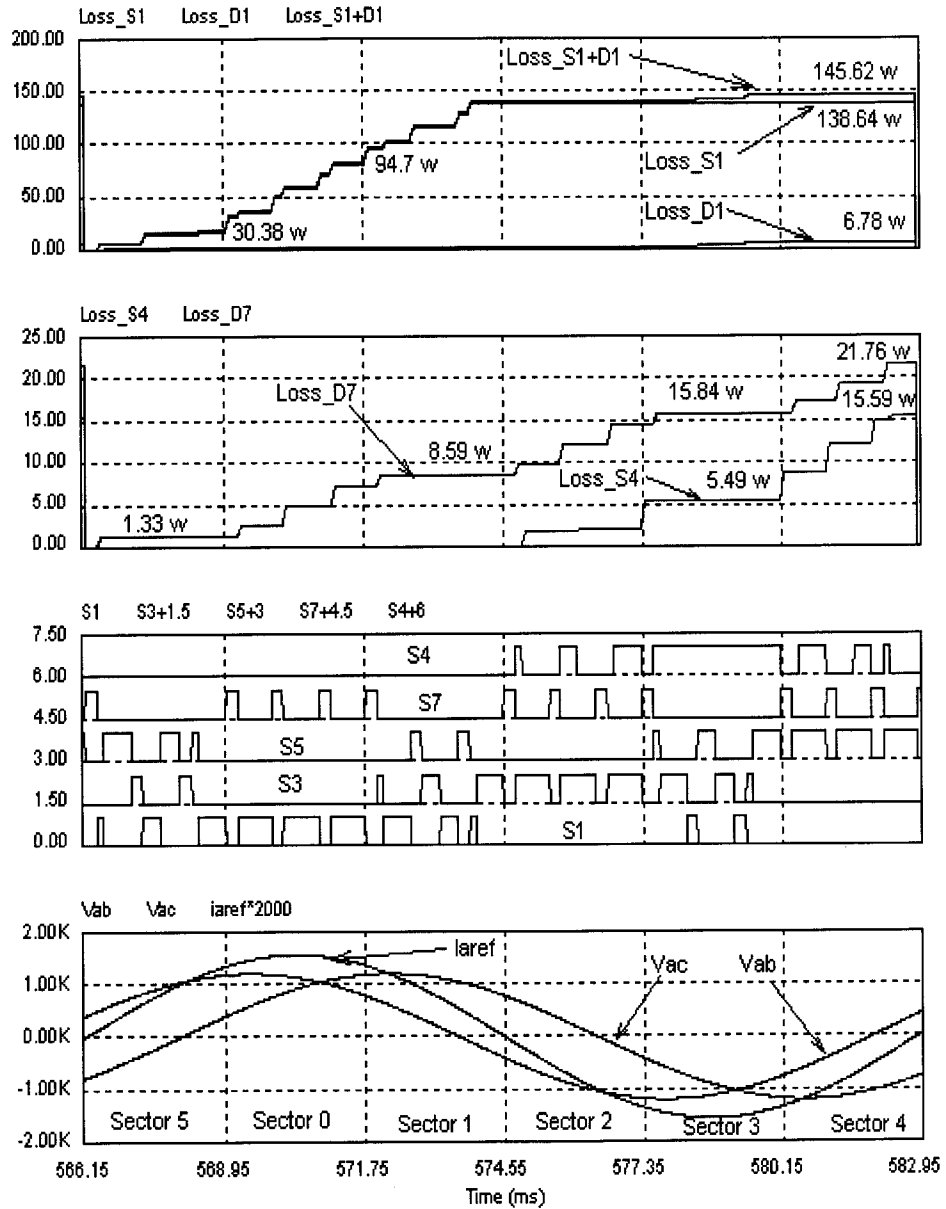


Fig. 9- 4:- Simulation results for the commutation losses for HCSC with SS-SVM.

- a) Power losses in switch S1 and its series diode.
- b) Power losses in S4 and D7.
- c) Gating signals.
- d) Reference current and ac-side line voltages waveforms.



Table 9- 4 shows a summary of the conduction and switching losses for the semiconductors used in the 6-switches SVM-CSC and in the HCSC with HS-SVM and SS-SVM with  $N_{CS} = 3$  and  $m_{a,max} = 0.78$ . The two first converters operate as rectifiers with UPF while the third operates with  $PF = \cos 10^\circ$  leading, where the worst switching power losses for HCSC appears. In such a case, despite the increased in the switching losses of the HCSC, the total power losses at the IGBTs of the HCSCs are smaller than those of the 6-switches CSC. This is the ideal scenario for using the proposed HCSC when the same switch and cooling device of the CSC could be used for the HCSC.

TABLE 9- 4 :- LOSSES FOR SEMICONDUCTORS USED IN THE 6-SWITCH CSC AND HCSC.

	Conduction (W)	Switching (W)					Total power losses (W)
		Bridge switch	Bridge diode	Freewheeling switch	Freewheeling diode	SCR	
SVM-CSC	6835.2	78.14	8.68	-	-	-	7356.12
HS-SVM	4462.2	279.67	15.87	0.0	47.6	17.78	5449.76
SS-SVM	4410.4	138.64	6.78	0.0	21.67	15.59	4915.1

## 9.6. CONCLUSION

Cost analysis for 6-switches SVM-CSC as well as for the HCSC with HS-SVM and SS-SVM are presented and the economical benefits from using HCSC are explained. A preliminary cost equation required to claim cost effectiveness of HCSC is proposed. Capital cost saving in HCSC is investigated. Power losses analysis for the life time cost saving is considered. The number of switching pulses and semiconductor devices in the current path does not give an accurate switching and conduction power losses.

Power losses analysis based on datasheets is presented. The conduction power losses in 6 switches SVM-CSC do not depend on the modulation scheme. But, for HCSC it depends on the modulation scheme. Switching power losses in SVM-CSC and HCSC with both HS-SVM and SS-SVM depend on the sequence of switching and modulation scheme. Switching power losses depend on commutation line to line voltage, while conduction power losses do not depend on commutation voltages. Conduction power losses are dominant in the considered power range with  $f_{\text{cycle}} = 1080$  Hz, around 80% from power losses is conduction while 20% is switching losses. 6-switches SVM-CSC devices and topology present high conduction power losses compared with HCSC. 90% of switching power losses appears in IGBTs.

Issues like, IGBTs can be turned on and off during certain cases without switching losses, diodes and SCRs turn on losses being neglected, and diodes turn off losses being soft in some cases are discussed. That helps to find the switching power losses for semiconductor devices as well as for the whole topologies in the selected case.

The overall power losses in HCSC with HS-SVM or SS-SVM are lower than in 6-switches SVM-CSC topology. So, the heat sink size for HCSC should be smaller than that of 6-switches SVM-CSC. In addition, there is a power saving during lifetime of the HCSC with the same operating condition of 6-switches SVM-CSC topology. Besides, in high power rating IGBTs should be connected in series/parallel to handle high power ratings while one SCR can be used to handle higher power rating, which can justify replacing 6-switches CSC topology with HCSC in medium and high power ranges.

## 10. CONCLUSIONS

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### 10.1. SUMMARY

#### 10.1.1. PART ONE

The first part of the thesis focuses on the reduction of the non-characteristic low order harmonics (LOH) in the ac-side current of low switching frequency space vector modulated current source converter (LSF-SVM-CSC). In chapter one, an analysis of the reasons of those LOH is presented, previous techniques used to calculate the states ON times in SVM-CSC are presented. And, the best sequences of states from low order harmonics point of view are presented.

In chapter two, non-characteristic 5<sup>th</sup> and 7<sup>th</sup> LOH are used to define an index  $HD_{5-7}$ .  $HD_{5-7}$  is reduced in Record Middle (RM) with low software efforts. There an improvement in  $HD_{5-7}$  is obtained by calculating the states ON times at different moments, in the middle of each state appearing period and with the reference vector placed at different locations during a given cycle. That permits respecting the calculated ON times of only two states, from three in the sequence, while the third occupies the remainder of the SVM cycle. When both active states ON times calculation are respected,  $HD_{5-7}$  is reduced to up to 60 % with respect to the standard SVM technique. The best performance is achieved with up to 90 % reduction in  $HD_{5-7}$  using SQ3-RM.

In chapter three, further reductions in  $HD_{5-7}$  are achieved resulting in the virtual elimination of the non-characteristic LOHs. New equations are proposed for a technique

called EQ. The equations procedure varies with the sequence of states to achieve instantaneous calculations. If the calculated ON times are further adjusted to fit in the SVM cycle a new procedure called CF is generated. In CF the harmonic distortion arrives to a virtual elimination point with a certain sequence (SQ3-CF) where  $HD_{5-7} < 0.44\%$  for any  $m_a$ . The superior performance of the proposed techniques was demonstrated with simulation as well as experimental results.

The CSC is considered *ideal* in chapter three and  $HD_{5-7}$  will appear again if the techniques described there are used in a real CSC. For a real GTO based CSC with overlap period and input filter resonance, the elimination of  $HD_{5-7}$  requires a procedure changing the states ON times within a certain limit to reach the least possible  $HD_{5-7}$ . This is done with the minimum harmonics tracking (MHT) technique presented in chapter four. MHT is based on measuring the value of  $HD_{5-7}$  and come up with a procedure to reach the least possible  $HD_{5-7}$  using the perturbing and observing principle. The proposed MHT technique allows the use of a small 6.8pu cut-off frequency filter, that gives the attenuation required for the characteristic harmonics in the ac-side current while keeping  $HD_{5-7} < 0.6\%$ . Ambiguity in the exact commutation instant due to the long overlap period in GTOs based CSC implies uncertainty of current flow in the switches for PF variations. Independently of the  $m_a$ , PF, ac-side filter cut-off frequency and overlap period, the proposed MHT technique kept the  $HD_{5-7} < 3\%$ . More reduction in  $HD_{5-7}$  is achieved by modifying the tracking process to deal with large overlap periods. A two variable MHT technique which gives  $HD_{5-7} < 2\%$  is presented. An experimental investigation demonstrates the effect of correct states ON times calculation on  $HD_{5-7}$ .

In chapter five, Fuzzy logic is found effective in eliminating  $HD_{5-7}$  with fast response. There the least  $HD_{5-7}$  is accurately reached. Reaching the least  $HD_{5-7}$  can be done fast at the expense of the complexity of Fuzzy logic. For the simple Fuzzy logic proposed, no oscillations around the least  $HD_{5-7}$  exist in the steady state. Fuzzy logic is acting fast by to reach the least  $HD_{5-7}$  if the operating point is changed.

### **10.1.2. PART TWO**

The second part of the thesis focuses on reducing the cost of 6-switches CSC. In chapter six, Existing HCSCs topologies are presented. Then, two types of HCSCs are proposed. The first is a HCSC with six SCRs and two IGBTs. This topology presents a problem common in HCSCs, the probability of having a high cost for the two IGBTs. That reduces the cost advantage of the HCSC. The second is a HCSC with three SCRs and four IGBTs, which has the potential for high cost reduction. An experimental test proves the feasibility of the proposed HCSCs topologies.

In chapter seven, a Hard Switching SVM (HS-SVM) scheme suitable for HCSCs is proposed. When HS-SVM is used HCSCs are bi-directional and have no PF limitations with capabilities similar to SVM-CSC. Due to the SCR's commutation issues, the maximum modulation index ( $m_{a,max}$ ) for the HCSC is reduced. The gating signals for semiconductor devices in HCSC with HS-SVM are compared to those of 6-switches SVM-CSC. The increment in the switching losses of the four IGBTs is 100% for the HS-SVM if compared with the 6-switch SVM-CSC. The HCSC with three SCRs and four IGBTs is implemented experimentally and further investigations done by simulation. There is good correlation between the simulations and experimental results. The proposed HCSC has a potential to give characteristics similar to SVM-CSC in ac-side and dc-side

voltages and currents. Closed loop control scheme for the HCSC with HS-SVM allows HCSC to track  $P_{ref}$  and  $Q_{ref}$ .

In chapter eight, SVM technique suitable for three SCRs and four IGBTs HCSC is proposed (SS-SVM). With this technique, the HCSC presents a performance level equivalent to 6-switch SVM-CSC in terms of flexibility and harmonic distortion. While the HCSC topology reduces the number of force-commutated switches required for the converter, SS-SVM scheme reduces the number of switch commutations and makes some of them soft-switching. The gating signal generation scheme considers the instantaneous voltages at the input of the HCSC and the desired PF to determine the order of the active states in a three segment sequence which allows at least one soft-switching commutation in each SVM cycle. The proposed SS-SVM scheme also increases  $m_{a,max}$  and reduces the LOH if compared with HS-SVM. The drawback of the proposed SS-SVM scheme is that the angle between current and voltage cannot be varied continuously. The step size for this angle is defined by the number of cycles per sector used in the SVM. The maximum angle error is equal to  $10^\circ$  for SVM with three cycles per sector. So, active and reactive power cannot be regulated independently. However, one can choose to create a reference current vector, where  $P_{ref}$  is followed accurately while accepting an error in  $Q_{ref}$ . Experimental verification supports the SS-SVM concepts, like commutation success, commutation failure and changing the sequence with different values of PF.

In chapter nine, cost analysis for 6-switches SVM-CSC as well as for the HCSC with HS-SVM and SS-SVM are presented and the economical benefits of the proposed HCSC are demonstrated. Economical benefits are divided into capital and power losses. A datasheet case study is presented for power losses analysis. The modulation scheme

and the line to line voltage effects in conduction and switching power losses in CSC and HCSC are presented. In the considered power range with  $f_{\text{cycle}} = 1080\text{Hz}$ , conduction losses are presenting 80% of the total losses. 6-switches SVM-CSC devices and topology are presenting high conduction power losses compared with HCSC. Switching losses is 20% of the total losses, 90% of the switching losses appear in IGBTs. The overall power losses in HCSC with either HS-SVM or SS-SVM is less than that of the 6-switch SVM-CSC topology. So, the heat sink size for HCSC is smaller than that of 6-switch CSC beside the power saving during lifetime of HCSC with the same operating condition of 6-switch topology. That can justify replacing the 6-switch CSC with HCSC in medium and high power ranges.

## **10.2. FUTURE WORK**

### **10.2.1. PART ONE**

The future work is divided into four points. First, apply the proposed techniques to VSC by changing the SVM to be adequate for 6 switches VSC. A wider comparison base will be available, there are more publications covering VSCs if compared with CSCs. Second, one can use an artificial intelligence technique different than Fuzzy logic, like genetic algorithm which have high computation efforts. Fuzzy logic is the artificial intelligence technique suitable for on-line operation. Due to high computation efforts the selected technique will not be able to drive CSC on-line. Instead, an off-line procedure can be followed. That may lead to another procedure to reduce LOH. The third research point is selecting a faster hardware gives experimentally the theoretical results of  $HD_{5-7}$  with 60 Hz source, like FPGA. Finally, an advance can be in high power multilevel GTO

based CSC. Applying the proposed techniques (RM, CF, MHT and Fuzzy logic) to multilevel CSC with possibility to change the sequence from one layer to the other should be effective if high power without LOHs is required.

### **10.2.1. PART TWO**

Future work in part two is divided into two categories. First, a wider cost analysis can be done by taking into consideration the drive cost as well as the heat-sink shape effect on the cost. Also, the cost analysis can focus on different power ranges. In very high power applications, series-parallel connection requirements in IGBTs can increase the cost of 6 switches SVM-CSC thus making the cost advantage of the HCSC even higher. On the other hand  $t_q$  will increase, what leads  $m_{a,max}$  in HS-SVM to be low. In this case, SS-SVM should be employed. Second, the control scheme for the dc-side and ac-side currents for the HCSC is not fully presented in this thesis. Nonetheless, the author believes that the preliminary control scheme presented in this thesis can be used as the basis for achieving adequate steady state and transient performances.



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