Analytical Modeling of Drain-Current Characteristics of AlGaN/GaN HFETs with Incorporation of the Impacts of Virtual-Gate and Transferred-Electron Effect

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ABSTRACT

Analytical Modeling of Drain-Current Characteristics of AlGaN/GaN HFETs with Incorporation of the Impacts of Virtual-Gate and Transferred-Electron Effect

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GaN-based heterostructure field effect transistors (HFETs) have gained considerable attention in high-power microwave applications. So far, unsurpassed current levels and high output power at microwave frequencies have been achieved. However, the dominant factors limiting the reliability of these devices under high-power operation are still unsettled. Drain current collapse is one of the major encumbrances in the development of reliable high-power devices in this technology. In this thesis, an accurate and versatile analytical model based on the concept of virtual gate formation due to the existence of acceptor type surface states is developed to model the current-collapse phenomenon. The implementation of this simple and at the same time precise analytical model demonstrates superb agreement with the experimental observations of permanent/semi-permanent current collapse in AlGaN/GaN HFETs.

An analytical model, with incorporation of transferred-electron effect, for drain-current characteristics of AlGaN/GaN HFETs is also presented. Oftentimes, the transferred electron effect is neglected in modeling the drain-current characteristics of III-V HFETs. The broader steady-state electron drift-velocity overshoot of GaN in comparison to other direct semiconductors such as GaAs and InP, in addition to the larger difference between the peak and saturation drift-velocity, and the wider bandgap of this

semiconductor predict the importance of the incorporation of transferred-electron effect (i.e. steady-state drift-velocity overshoot) in modeling the drain-current of these devices. Simulation results are compared with the results of the adoption of Ridley's mobility model which does not take into account the transferred-electron effect. Solving the Poisson's equation through a simple iterative method and considering the diffusion component of current are at the core of this model. The iterative nature of this approach has considerably relieved the outcome of the implementation from the choice of fitting parameters.

"Thus, the task is, not so much to see what no one has seen; but to think what nobody has yet thought, about that which everybody sees."

--Edwin Schrodinger

"When we look at how long it took us to get certain ideas, we are impressed with how dumb we were – on how long it took us, and how stupid we were. But we have learned to live with this stupidity, and to find from it what relationships we should have seen in the first place. This recognition that we are not perfect but that persistence pays is a very important factor, in giving one the will to think – you do not need to worry so much about the mistake you make."

--William B. Shockley

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Chapter 1

Introduction

1.1 Advantages of GaN-based devices and research background

Over the past two decades, superb material properties of III-nitride semiconductors have motivated an increasing interest in research and development of novel electronic and optoelectronic devices. GaN along with the other III-nitride binaries and ternaries have found vast range of applications in high-power amplifiers [1], lasers [2], and detectors [3]. In the optoelectronics area, the wide bandgap of III-nitrides have made blue-violet lasers and green through ultraviolet LEDs possible [2]. Depending on the alloy composition, the direct bandgap of III-nitrides varies from about 0.7 eV up to 6.2 eV, covering a wide range of wavelength. Significant progress in the crystal quality and fabrication know-how of devices in this semiconductor family has led to a wide range of commercially viable products.

III-nitride-based power devices have also been the target of much recent progress [1]. Important material superiorities of III-nitride-based devices that make them attractive for high-power/high-frequency applications can be listed as: high electron mobility and saturation velocity, high sheet carrier concentration, good electron confinement, high breakdown electric-field, large thermal stability, and low thermal impedance when grown over thermally conductive substrates (i.e. SiC and Si).

Spontaneous and piezoelectric polarizations in III-nitride material system is at least an order of magnitude larger than those of conventional III-V compound semiconductors such as GaAs and InP [4]. High sheet carrier concentrations exceeding 10^{13} cm^{-2} can be obtained by these high polarization fields at the III-nitride interfaces. The basics and the role of polarization fields in III-nitride devices are briefly discussed later in this chapter.

The drift velocity of electrons in the III-nitride heterointerface has been the subject of much research. The drift-velocity versus electric-field characteristics of III-nitrides, like other III-V semiconductors, is shown to possess an overshoot at moderate values of electric-field and a saturating characteristic at higher electric-fields. This relationship is very essential for comprehending the operation of devices. At low fields, it is the low-field mobility which characterizes the velocity but at higher electric fields, this linear relationship no longer exists. This behaviour, through full incorporation of velocity-field characteristics, must be adopted to obtain a reliable device model.

In order to compare GaN with the two most popular semiconductors (i.e. Si and GaAs) as well as two other major wide bandgap semiconductors (i.e. SiC and diamond), Table 1-1 lists their bandgap energy (E_g), low-field electron mobility (μ_n), saturation velocity (v_{sat}), breakdown field (E_b), and thermal conductivity (Θ_K).

Table 1.1: Comparison of material properties between GaN, Si, GaAs, SiC, and Diamond at 300K [5].

Material	Si	GaAs	4H-SiC	GaN	Diamond
E_g (eV)	1.1	1.42	3.26	3.39	5.45
μ_n (cm^2/Vs)	1350	8500	700	900	1900
E_b (10^6 V/cm)	0.3	0.4	3	3.3	5.6
v_{sat} (10^7 cm/s)	1.0	2.0	2.0	2.5	2.7
Θ_K (W/cmK)	2.5	0.54	4.5	1.3	20

Higher breakdown field and saturation velocity of wide bandgap semiconductors have made them favourable over the conventional semiconductors in fabricating high power microwave transistors. Difficulties in doping and the lack of a suitable large area substrate for diamond as well as higher ability of GaN over SiC to form a heterojunction have made GaN-based device technologies to outstand as the most versatile alternatives for conventional technologies.

GaN-based electronic devices are not fully developed compared to the III-nitride optical devices. So far, different types of electronic devices have been investigated such as Heterojunction Bipolar Transistors (HBTs) [6], Metal Semiconductor Field Effect Transistors (MESFETs) [7], Metal Insulator Semiconductor Heterostructure Field Effect Transistors (MISHFETs) [8], and Heterostructure Field Effect Transistors (HFETs) [9], [10]. Among all these devices, HFETs have been at the center of most of the research. This is since in their operation they are not in need of p-type doping and also they enjoy better carrier transport properties. HFET structure reduces ionized impurity scattering by spatially separating the electrons in the channel from the dopants. A brief description of the operation principles of HFETs is provided later in this chapter.

Considerable effort to fabricate III-nitride microwave power transistors began less than two decades ago when the first AlGaN/GaN transistor was demonstrated by Khan *et al.* in 1993 [9]. They also reported small signal RF performance of AlGaN/GaN HFET

with the current gain cut-off frequency of 11 GHz, for a 0.25 μm-gate-length device [10]. Microwave power density of 1.1 W/mm at 2 GHz for an AlGaN/GaN HFET was reported by Wu *et al.* in 1996 [11]. From then till now, microwave output power densities have been increasing and this performance improvement has been dominantly due to the advancements in growth techniques and enhanced fabrication technology. Among these technological milestones are SiN passivation in 2000 [12] and adoption of field-plate in 2003 [13], [14]. SiN passivation efficiently decreased transconductance dispersions caused by the surface states and field-plate increased the breakdown voltage and also helped with additional reduction of dispersions [15]. Frequency dependent gain reduction of III-nitride transistors (i.e. dispersion) has been an unfortunate companion of transistors fabricated in this technology. These important advancements resulted in a major improvement in output power density up to 40 W/mm at 4 GHz [16]. It is worth noting that this record is partly due to the high thermal conductivity of SiC and is also due to the improved quality of AlGaN/GaN heterostructures grown on SiC. Recently, cut-off frequency of f_T=190 GHz (unity gain cut-off frequency) and f_{max}=241 GHz (maximum oscillation frequency) have been achieved [17].

1.2 Material properties of III-nitrides

The challenging history and the recent achievements in III-nitride devices, both are fed by their unique material properties. Therefore, a complete knowledge of these properties is indispensable for improving material quality, comprehensive device simulations, and obtaining better designs. In the following, important parameters of GaN and AlN have been briefly overviewed and listed in Table 1.2. AlN and GaN are the most important III-

Table 1.2: Basic material parameters of GaN and AlN at 300 K [18].

	GaN (Wurtzite)	GaN (Zinc-blende)	AlN (Wurtzite)
Lattice constant (Å)	a=3.189 c=5.186	4.52	a=3.112 c=4.982
Bandgap energy (eV)	3.39 3.51[19]	3.2 3.3[19]	6.2 6.23[19]
Electron affinity (eV)	4.1	4.1	0.6
Breakdown field (MV/cm)	5	5	1.2~1.8
Optical phonon energy (meV)	91.2 91.8[20]	87.3 91.9[20]	99.2 113[20]
Mass density (g/cm^3)	6.15	6.15	3.23
Static relative dielectric constant	8.9 9.5⊥,10.4∥[21]	9.7	8.5 7.76⊥,9.32∥[22]
RF relative dielectric constant	5.35	5.3	4.6 4.16⊥,4.35∥[22]
Electron diffusion coefficient (low-field) (cm^2s^{-1})	25	25	7
Hole diffusion coefficient (low-field) (cm^2s^{-1})	5	9	0.3
Electron effective mass (in terms of m_0)	0.20	0.13 0.15[19]	0.4 0.48[23]
Hole effective mass (in terms of m_0) $m_{h,h}$ $m_{h,l}$ $m_{h,so}$	 1.4 0.3 0.6	 1.3 0.2 0.3	 (z):3.52, (x):10.42 (z):3.53, (x):0.24 (z):0.25, (x): 3.81
Effective conduction band Density of states (cm^{-3})	2.3×10^{18}	1.2×10^{18}	6.3×10^{18}
Effective valence band Density of states (cm^{-3})	4.6×10^{19}	4.1×10^{19}	4.8×10^{20}
Elastic constants (GPa) [19],[24] C_{11} C_{12} C_{13} C_{33} C_{44}	 390 145 106 398 105	 293 159 N/A N/A 159	 396 137 108 373 116
Piezoelectric constants (cm^{-3}) e_{31} e_{33}	 -0.49 -0.34[25] 0.73 0.67[25]	 N/A	 -0.60 -0.53[25] 1.46 1.5[25]
Coefficients of thermal expansion α_a (10^{-6} K^{-1}) α_c (10^{-6} K^{-1})	 3.1 2.8	 3.8 2.9	 2.9 3.4
Debye temperature (K)	600	600	1150
Thermal conductivity ($Wcm^{-1}K^{-1}$)	2.3	2.3	2.85

nitride binaries for electronic applications. Their ternary compound of $Al_xGa_{1-x}N$ is mostly used as the barriers layer of AlGaN/GaN heterostructures. One of the most important challenges of III-nitride semiconductors has been the lack of a lattice-matched substrate. This challenge has so far been primarily addressed by the adoption of appropriate transition layers grown on lattice mismatched substrates. AlN is often grown as a nucleation layer for growth of AlGaN/GaN heterojunctions on sapphire and SiC substrates.

$Al_xGa_{1-x}N$, $In_xGa_{1-x}N$, and $In_xAl_{1-x}N$ can be grown in form of heterostructures to enable bandgap engineering which has incredible impacts on electronic and optoelectronic applications. For further explanation about calculating material properties of ternary and quaternary materials refer to [26] and [27].

1.3 Piezoelectricity and spontaneous polarization in III-nitride materials

III-Nitrides are traditionally grown by Molecular Beam Epitaxy (MBE) and Metal Organic Vapor Phase Epitaxy (MOVPE) in two crystalline forms: Wurtzite (Wz) and Zinc-blende (Zb). Among which Wurtzite is the thermodynamically stable structure under ambient conditions for all three of III-nitride binaries. For thin films of GaN and InN, the Zinc-blende structure can also be found, while there is no stable Zinc-blende structure for AlN. The Wurtzite crystalline form because of the superiority of polarization charge induction has been the dominant crystalline form used in III-nitride electronics. As it is shown in Figure 1.1, the Wurtzite structure has a hexagonal unit cell. In this structure *a* is the basal lattice constant and *c* is referred to as the height of the hexagonal

prism. The unit cell of this crystal consists of two interpenetrating hexagonal close-packed (hcp) sublattices of one type of atoms of binary each, and they offset along the c-axis by $5/8^{th}$ of the cell height, c.

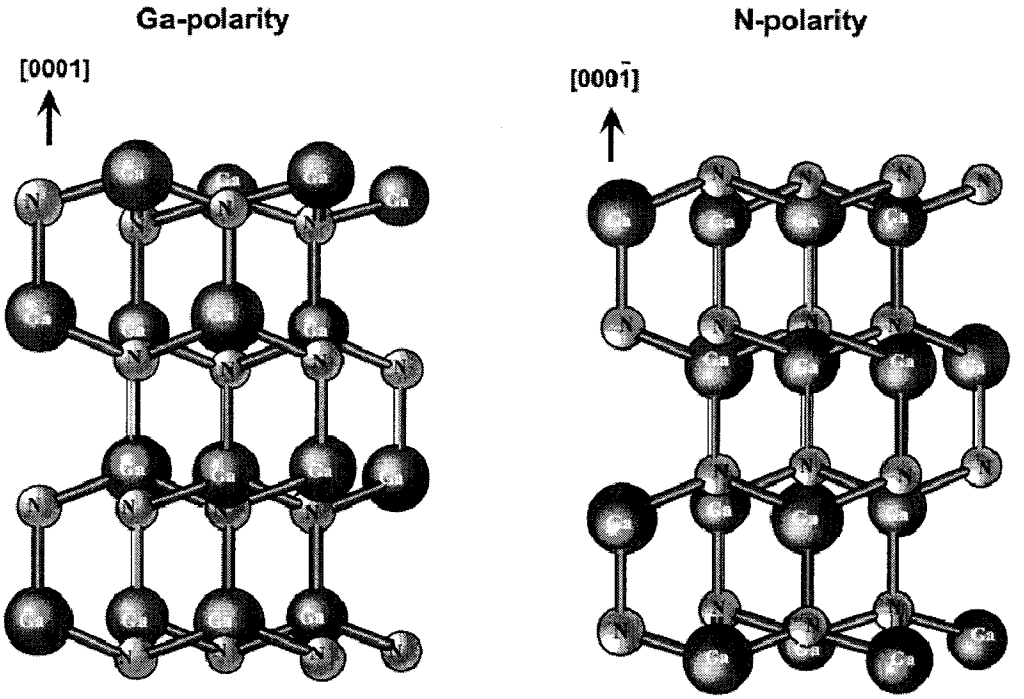


Figure 1.1: A stick-and-ball diagram of a hexagonal structure (the figure is adopted from [27]).

As shown in Figure 1.1, for Wurtzite GaN, the sequence of atomic layers could be either [0 0 0 1] (Ga-polarity) or [0 0 0 $\bar{1}$] (N-polarity). The most commonly used direction for growth is (0 0 0 1). The Wurtzite structure is represented by lattice parameters of a (in the basal plane), c (in the perpendicular direction) and u, internal parameter which is defined as the anion-cation bond length divided by c. In an ideal Wurtzite structure $^{c}/_{a} = \sqrt{^{8}/_{3}} = 1.633$ and $u = {}^{3}/_{8} = 0.375$, respectively. Any deviation from these values causes the formation of a spontaneous polarization.

III-nitride heterostructures present significant polarization effects at the heterointerfaces. Part of this polarization is induced due to the mismatch between the

degree of non-ideality of the layers of the heterostructure (i.e. spontaneous polarization) and the other part is generated due to the strain induced by the coherent growth of two lattice mismatched materials (i.e. piezoelectric effect). For III-nitride devices, control of these polarization effects plays a role as effective as that of barrier doping in inducing a two-dimensional electron gas (2DEG) concentration at the AlGaN/GaN heterointerface [4].

Ambacher *et al.* calculated the polarization induced sheet charge bound at the AlGaN/GaN heterointerfaces and through solving a self-consistent coupled Schrödinger and Poisson equation managed to calculate the induced sheet carrier concentration [28]. They showed that 2DEG formation in undoped and doped AlGaN/GaN structures considerably depends both on piezoelectric and spontaneous polarizations.

In case of an $Al_xGa_{1-x}N$ layer grown over a relaxed GaN layer, forming a single heterojunction, spontaneous and piezoelectric polarizations are parallel to one another and their overall effect is the induction of a sizeable polar 2DEG at the heterointerface.

1.4 AlGaN/GaN HFETs

An HFET is identical to a MOSFET in some ways. Instead of having an oxide layer, a wide-bandgap material (i.e. AlGaN in case of AlGaN/GaN HFET) separates the gate from the channel and a 2DEG forms the channel at the heterointerface. However, unlike the MOSFET in a traditional HFET the 2DEG channel increases the carrier mobility by avoiding the mobility degradation in a nearly ionized impurity scattering-free transport. In traditional HFETs the 2DEG is formed by the transfer of electrons from the doped

barrier to the triangular quantum well of the heterointerface. However, in III-nitride HFETs such a large concentration forms predominantly because of the presence of large polarization fields and not the barrier doping. As a result, this mobility improvement is not as apparent. Due to the presence of large polarization at the heterointerface, AlGaN/GaN HFET operates in the depletion mode. However, researchers are working on the realization of enhancement mode HFETs [29].

In HFETs, the source and drain are directly connected to the 2DEG via Ohmic contacts and the gate electrode modulates the current. A schematic cross-sectional view of a typical lattice-matched AlGaAs/GaAs HFET is shown in Figure 1.2. Electrons from the donor impurities in the barrier layer spill over into the triangular quantum well formed in the smaller bandgap material. Electrons in the quantum well have a two-dimensional degree of freedom. Meaning that they are able to transport in the plane of the device but confined in the growth direction.

This structure presents high carrier density even at very low temperatures. Therefore low temperature transport advantages can be materialized in terms of low-noise and high-gain microwave devices for aerospace applications. Moreover, thin active channel of HFET structure (typically about 20 nm) enables us to exploit very high mobility materials like InAs in the channel. These defect-prone materials are not robust enough to be used in structures like MESFETs.

As it is depicted in Figure 1.2, the AlGaAs barrier is doped and the GaAs channel is undoped. Due to the band bending, the carriers from the doped barrier layer are transferred to the heterointerface apart from doped region and are relieved from ionized impurity scattering. This is called modulation doping and these structures are commonly

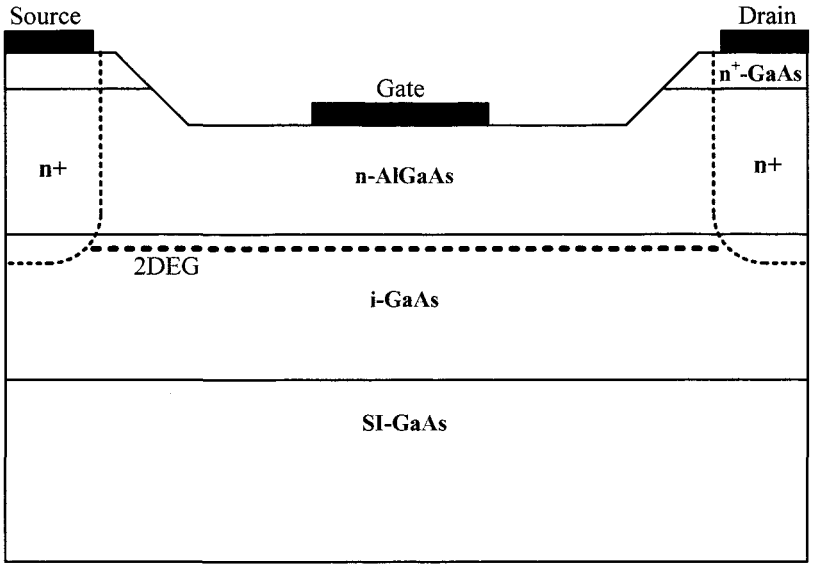


Figure 1.2: Schematic of a GaAs/AlGaAs HFET.

referred to as MODFETs. Figure 1.3 illustrates the conduction band diagram of an AlGaAs/GaAs HFET demonstrating how the band bending leads to the formation of a triangular quantum well at the heterointerface.

Even though GaAs-based HFETs exhibit many advantages over GaN, in this technology high MW-power circuits are only viable by implementation of techniques such as power combining which come at a substantial cost. This is where wide bandgap GaN-based HFETs draw attention.

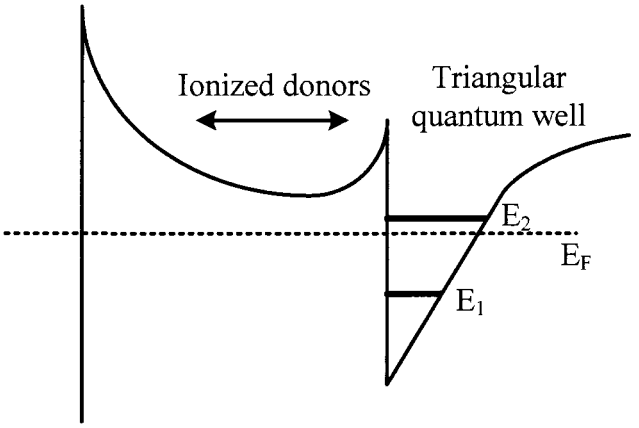


Figure 1.3: Band diagram of an AlGaAs/GaAs HFET showing the band bending leading to a triangular quantum well at the heterointerface.

GaN-based HFETs are different from the conventional GaAs-based HFETs due to the strong polarization terms of III-nitride materials. Figure 1.4 shows a basic AlGaN/GaN HFET structure. The thin AlGaN layer is coherently grown over GaN under tensile strain. This is because of the larger basal lattice constant of GaN. The total polarization charge at the AlGaN side of the heterointerface is calculated according to the sum of the contribution of the piezoelectric and spontaneous polarizations [4].

The net polarization at the heterointerface which is the result of unidirectional spontaneous and piezoelectric polarization terms is positive. This is the cause for the further lowering of the conduction band edge at the heterointerface. This effect can be observed with regard to the variations in the form of band bending in Figure 1.3 and Figure 1.5. This extra band bending results in induction of a much stronger 2DEG in the triangular quantum well. Free electrons are either provided through the surface donors or less probably by the unintentional doping of the heterostructure. Figure 1.5 depicts the conduction band structure of an undoped AlGaN/GaN HFET.

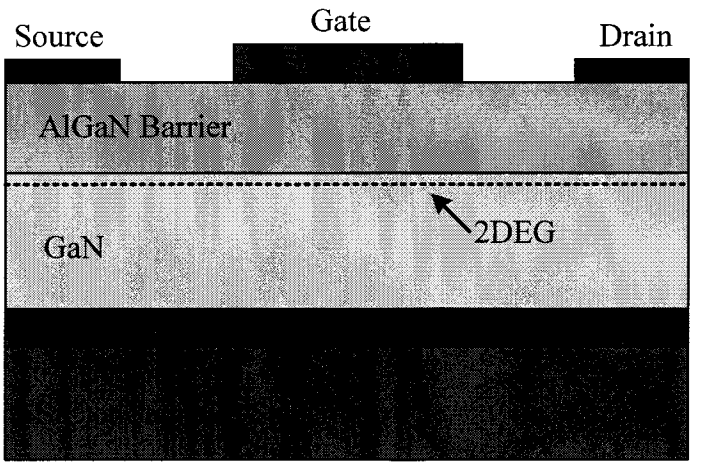


Figure 1.4: Basic AlGaN/GaN HFET structure.

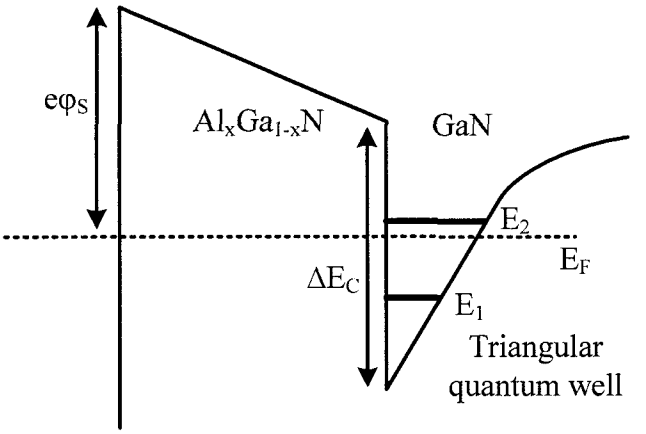


Figure 1.5: Schematic of conduction band structure of an undoped AlGaN/GaN HFET.

An important advantage of polar III-nitride-based HFET over conventional GaAs-based HFET is that in this polar technology it is not necessary to dope the barrier to populate the channel with electrons.

1.5 Anomalous characteristics in AlGaN/GaN HFETs

Despite the advantages, III-nitride materials are suffering from difficulties which must be overcome to make this technology mature and reliable. These challenges are poor crystalline quality, difficulties in growing device layers, presence of native defects, lack of a lattice matched substrate, unavailability of shallow p-type dopants, lack of chemical etchants, and difficulties with achieving a high quality Ohmic contact to GaN. Moreover, among other long-term reliability issues, the main challenges for commercializing GaN HFET technology are current-collapse, gate-lag, gate-leakage, leakage through substrate, and frequency dispersions. Historically, current-collapse is associated with the transient or even permanent reduction of the dynamic DC drain-current which takes place after application of a high frequency power signal. The reduction in maximum drain-current in conjunction with the increase in the knee-voltage, are the reasons for the modesty of the

output power of AlGaN/GaN HFETs in comparison to their DC-predicted values. This degradation phenomenon has been the subject of many recent papers and is generally referred to as "current collapse", "current slump", "current compression", or "dispersion".

Unpassivated surface states can be the cause of the current collapse through reducing the 2DEG charge concentration mostly in the gate-drain spacing. In the performance of III-nitride devices, surface states play a more prominent role compared to GaAs-based devices. This is partly because of the importance of polarization fields in this material system.

1.6 Overview of thesis

Drain-current collapse is one of the major encumbrances in the development of reliable high-power devices in this technology. Other major difficulties include gate-lag, gate-leakage, and leakage through substrate. Although material improvements and advances in fabrication technologies have been considerably helpful in reducing these problems, understanding the physics of these non-ideal effects is still an encumbrance that can be overcome through development of accurate models capable of predicting the variation of reliability metrics with device design. Due to the limiting impact on the microwave output power, the issue of current-collapse is the most important of these device peculiarities. In Chapter 2, an accurate and versatile analytical model based on the concept of virtual gate formation due to the existence of acceptor type surface states is developed to model the current-collapse phenomenon. The implementation of this simple and at the same time precise analytical model demonstrates superb agreement with the

experimental observations of permanent/semi-permanent current collapse in AlGaN/GaN HFETs.

The simulation and modeling of AlGaN/GaN HFETs is an important tool to improve our understanding of these devices and to produce better designs for transistors and circuits. In simulations of AlGaN/GaN HFETs, the adoption of appropriate electron transport model is of paramount importance. The existing models fail to consider the transferred-electron effect in this characteristic. An analytical model, with incorporation of transferred-electron effect, for drain-current characteristics of AlGaN/GaN HFETs is presented in Chapter 3. Oftentimes, the transferred electron effect is neglected in modeling the drain-current characteristics of III-V HFETs. The broader steady-state electron drift-velocity overshoot of GaN in comparison to other direct semiconductors such as GaAs and InP, in addition to the larger difference between the peak and saturation drift-velocity, and the wider bandgap of this semiconductor predict the importance of the incorporation of transferred-electron effect (i.e. steady-state drift-velocity overshoot) in modeling the drain-current of these devices. Simulation results are compared with the results of the adoption of Ridley's mobility model which does not take into account the transferred-electron effect. Solving the Poisson's equation through a simple iterative method and considering the diffusion component of the current are at the core of this model. The iterative nature of this approach has considerably relieved the outcome of the implementation from the choice of fitting parameters. In Chapter 4, conclusions of this work are presented along side with a suggested list of future work in this area.

Chapter 2

Analytical Modeling of Current Collapse in AlGaN/GaN HFETs According to the Virtual Gate Concept*

2.1 Abstract

GaN-based HFETs have gained considerable attention in high power microwave applications. So far, unsurpassed current levels and high output power at microwave frequencies have been achieved. However, the dominant factors limiting the reliability of these devices under high power operation are still unsettled. Drain current-collapse is one of the major encumbrances in the development of reliable high power devices in this technology. In this chapter, an accurate and versatile analytical model based on the concept of virtual gate formation due to the existence of acceptor-type surface states is

* Based on a published manuscript: M. Moradi and P. Valizadeh, "Analytical modeling of current collapse in AlGaN/GaN HFETs according to the virtual gate concept," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 2, June 2010.

developed to model the current-collapse phenomenon. The presented model is considerably simpler and at the same time it is more precise than the other analytical models previously proposed in literature. The implementation of this analytical model demonstrates superb agreement with the experimental observations of permanent/semi-permanent current collapse in AlGaN/GaN HFETs. To demonstrate the versatility, results of this model are also compared with an existing recently-developed analytical model of comparable degree of complexity.

2.2 Introduction

The AlGaN/GaN material system has been proven to be an almost perfect choice for high power microwave applications. Very high breakdown electric-field (>3 MV/cm), polar 2DEG density in excess of 10^{13} cm^{-2} without the need for barrier layer doping, high saturation and overshoot electron velocity (>3×10^{7} cm/s), and good low-field electron mobility (1500-2200 $cm^2/V\cdot s$) are some of the advantages of this material system. So far, excellent microwave device performance has been achieved in this system including: very high output power of 900 W at 2.9 GHz, 81 W at 9.5 GHz and high unity gain cutoff frequency of 181 GHz for gate length of 30 nm [30], [31].

Among other long-term reliability issues, the main challenges for commercializing GaN HFET technology are current-collapse, gate-lag, leakage through the buffer layer, and gate leakage. Despite the fact that the improvements in fabrication technologies and material quality have been noticeably useful in reducing these anomalies, understanding the physics of these non-ideal effects is still a hindrance that can be overcome through development of accurate models capable of predicting the variation of reliability metrics

with device design. Due to the restricting effect of current collapse on the microwave output power, this issue can be considered the most important of these device peculiarities.

Historically, current-collapse is associated with the transient or even permanent reduction of the dynamic DC drain current which takes place after application of a high frequency power signal. The reduction in maximum drain current in conjunction with the increase in the knee-voltage, are the reasons for the modesty of the output power of AlGaN/GaN HFETs in comparison to their DC-predicted values [32]-[36]. In the case of AlGaN/GaN HFETs, the common expectations are that the trapping centers reside either in the GaN buffer layer, in the AlGaN barrier layer, at the heterointerface, or at the surface of the device. There are variety of conflicting explanations for the trapping mechanism and the location of traps responsible for current-collapse in III-nitride HFETs. Following the earlier tracks of current-collapse in FETs, many of the explanations attribute the drain current-collapse to trapping of hot electrons in the gate insulator layer at the drain-access region.

In polar AlGaN/GaN heterostructures existence of large polarization-fields make the consequences of charge-trapping at the surface, dissimilar with the conventional III-V heterostructures. Change in the surface potential has significant effects on the properties of these polar HFETs and it is widely accepted that surface states or surface charges can have a noticeable effect on the microwave performance of GaN HFETs [33]-[36].

According to the virtual gate concept, acceptor-type surface states upon accepting electrons form a negative surface potential which is in effect equivalent to negatively charging an imaginary virtual gate on the surface [33], [37], [38]. These electrons can

originate from the hot electrons of the channel [38], or from the surface component of the gate-leakage current [33], [35]. As it is suggested in Figure 2.1, this negatively biased virtual gate partially depletes the channel of electrons and extends the depletion region. The potential and the length of the virtual gate are dependent on the time, history of the electric-fields applied on the device, and also spatial distribution of traps. In this work, through treatment of the charge-trapped area as a secondary virtual gate, the tandem role of virtual gate and the principal gate in pinching-off the channel has been used to analytically explain the current-collapse phenomenon.

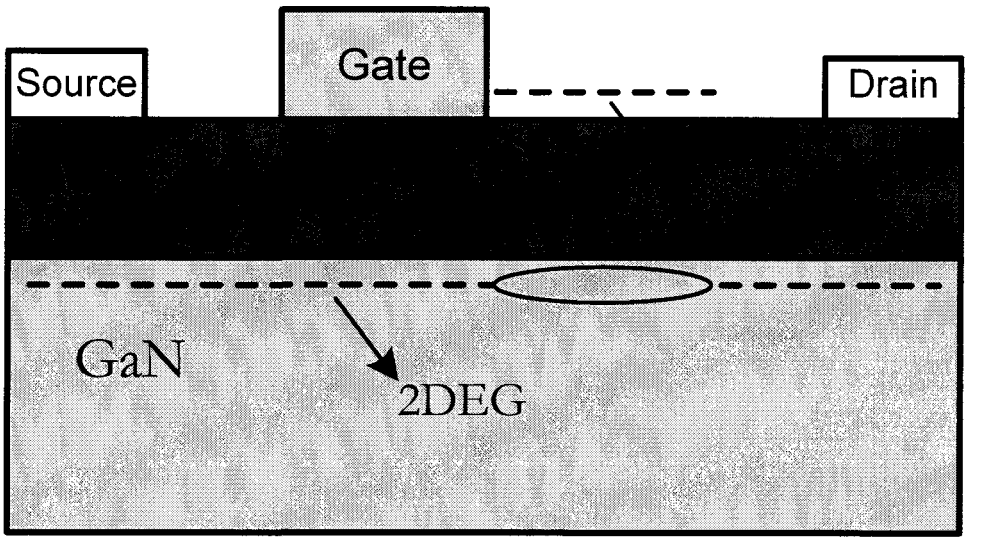


Figure 2.1: Occupied surface states forming a negatively biased virtual gate and depleting 2DEG of electrons. AlGaN is the barrier and 2DEG is formed at the AlGaN/GaN heterointerface. The part of the channel marked by the ellipse is the region in which partial depletion of 2DEG is happening due to electron trapping at the acceptor-type surface states.

After recent developments of high-performance GaN-based devices, development of reliable and versatile analytical models have become imperative to commercializing the technology. While physics-based models based on the self-consistent solution of Schrödinger and Poisson equations require exorbitant computations which are not compatible with the needs of circuit designers, analytical models are being explored. So far,

many analytical models for GaN-based HFETs have been reported [39]-[41]. In this work, due to the ease of implementation and versatility of the model, the modeling strategy of Koudymov *et al.* [41] is followed. In contrast to the other analytical models, this modeling strategy is based on a reasonable set of assumptions and a smaller number of fitting parameters. In spite of that, incorporation of simplifying assumptions as well as the application of a few vague fitting parameters and complicated equations for post-stress characteristics is observed to have created major discrepancy between the best-fit simulation results and the post DC-stress experimental observations of the drain I-V characteristics of the type reported in [38]. In this chapter, a novel analytical model for post-stress I-V characteristics is presented which offers several improvements over the other proposed models. In this more accurate model, complicated numerical calculations are not involved and an excellent agreement with the experimental observations is achieved. The model is shown to be especially superior in predicting the permanent/semi-permanent type of current collapse phenomena in AlGaN/GaN HFETs that was reported by Valizadeh *et al.* [38].

In section 2.3, analytical model for short-channel HFET before and after stress (i.e. in presence of current-collapse) is discussed. In section 2.4, simulation results of the proposed model and its comparison with experimental measurements is presented. Section 2.5 contains the concluding remarks.

2.3 Analytical I-V model of AlGaN/GaN HFET before and after stress

In this section, an analytical model is presented to fully model the permanent degradation of the drain current-voltage characteristics caused by the long-term DC-stress tests of the type

reported by Valizadeh *et al.* in [38]. The analytical model briefly presented in section 2.3.1, follows the model presented in [41]. It is instrumental to revisit this model which has been used as the starting point for the development of the model presented in the next section for the inclusion of post-stress effects. Section 2.3.2 embodies the development of a more accurate model for the post-stress drain current-voltage characteristics, than other analytical models found in literature.

2.3.1 Before stress

Due to the existence of high average electric-field across the channel and significance of velocity-saturation effects in short-channel FETs, adoption of a realistic electron-velocity vs. electric-field (v_d-E) relationship is essential. Despite the existence of more accurate models capable of reproducing the exact v_d-E characteristics of AlGaN/GaN HFETs [42], [43], the two-field approximation of Ridley is deemed sufficient [44]. The main advantage of the adoption of this approximation is that this model easily produces solvable expressions for the current-voltage characteristics as it was observed in [41]. Despite the inherent inaccuracy of this model in predicting the negative differential mobility and peak electron-velocity, it is believed that at the current stage of the development of AlGaN/GaN HFETs the exclusion of these effects will not impact the accuracy of the model [45]. This issue is tested in section 2.4 in conjunction with the matching to the experimental data. According to the two-field approximation:

$$v(F) = v_0 F \frac{F + F_1}{F_1(F + F_0)} \quad F_0 = \frac{v_0}{\mu_0} \quad F_1 = \frac{v_0}{\mu_1} \quad F \leq F_s \tag{2.1}$$
$$v = v_s \quad F > F_s$$

where F_0, F_1, and v_0 are the fitting parameters of the model. Set of parameters matched to

the best fit of the model to the v_d-E relationship produced by the Monte Carlo simulation is adopted from [41]. This model is illustrated on Fig. 2.2(b).

For modeling the I-V characteristics in absence of current-collapse, by using the procedure proposed in [41] the following equation can be obtained for the gate-length (i.e. L_G) before saturation point:

$$L_G = \int_{V_{GT}-V_{SG}}^{V_{GT}-V_{DG}} \frac{JF_1 - c_{CH}v_0F_1V}{2JF_1F_0}dV + \frac{\sqrt{(JF_1 - c_{CH}v_0F_1V)^2 + 4c_{CH}v_0JF_1F_0V}}{2JF_1F_0}dV \tag{2.2}$$

This equation is derived based on the assumption of a drift-only channel under low electric-fields. Charge concentration of 2DEG is modeled through a parallel plate capacitor formed under the gate electrode.

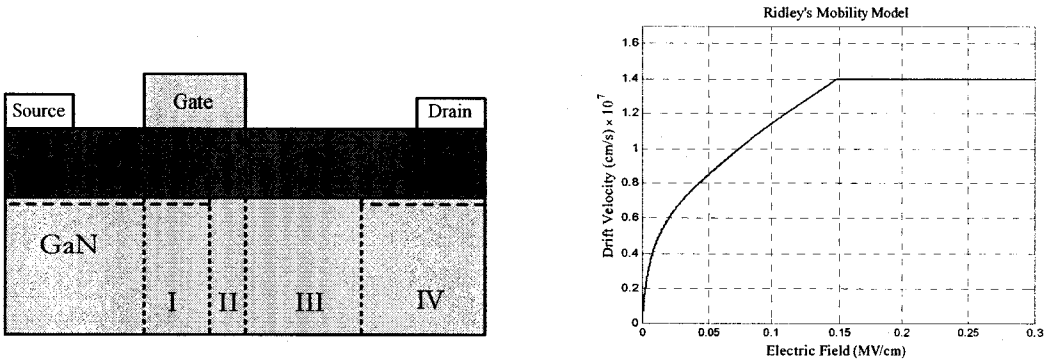
In this equation, V and J are the channel potential and the current density, respectively. V_G is the gate bias, V_T is threshold voltage, L_G is the gate length of the device and C_{CH} is the gate capacitance per unit area. V_{DG} and V_{SG} are representatives of the gate-channel potential at the drain and source side of the gate, respectively. Numerically solving the above equation for any given value of drain-voltage will yield a drain-current value.

According to this model, after the saturation point of drift velocity, the device channel under the gate will be divided into two regions. Boundary of the first region is defined at where the electron velocity is below saturation and the second region is defined by the portion of the channel-length where the velocity is saturated. As it is proposed in [41], the I-V characteristic above saturation point can be modeled by replacing L_G in the left side of (2.2) with the length of the unsaturated channel under the gate terminal and the value of V_{DG} with saturation-voltage. This model also takes into account the extension of the depletion

region into the drain access region. This extension and the voltage distribution in this region are obtained by using the model proposed by Gelmont *et al.* [46], which is represented by:

$$V(x) = \frac{q\left(\sigma_p - {}^{J}/_{qv_s}\right)}{2\pi \in}\left[x\, ln\left(\frac{\sqrt{d_{DEP}^2 - x^2} + d_{DEP}}{d_{DEP} - \sqrt{d_{DEP}^2 - x^2}}\right) + 2d_{DEP}\, sin^{-1}\left(\frac{x}{d_{DEP}}\right)\right] \tag{2.3}$$

Figure 2.2 identifies the different existing regions along the channel. In order to examine the accuracy of the procedure, the analytical relationships have been implemented in MATLAB and as is shown in section 2.4 this simple analytical model is capable of accurately following the experimental I/V characteristics.



(a) (b)

Figure 2.2: Four-region identification of the analytical model presented in [41] (a). Electron drift-velocity versus electric-field characteristics according to Ridley's mobility model [44] (b). For simulation of drain current in saturation regime, regions marked with I and II indicate unsaturated and saturated part of the gate, respectively. Region III marks the extension of the depletion region into the drain-access region and finally region IV represents the linear decay region of the electric-field.

2.3.2 After stress

Following the explanations of the virtual gate concept, electron entrapment in acceptor-type trap sites at the surface of the device will cause a drop in polar 2DEG concentration [33], [38], [41], [47]. In the presently proposed model, contrary to the assumption of Koudymov *et al.* in [41], the impact of this virtual gate has been treated in a fashion

equivalent to negatively biasing a secondary gate on the surface. According to this model, the electron velocity saturation starts from the drain-edge of the virtual gate. By increasing the value of drain voltage, the boundary of the saturation region under the virtual gate moves further towards the main gate until the length of this saturation region will become equal to the length of the virtual gate. This value of drain voltage is the bias necessary for the commencement of saturation of the main gate. Further increase in the drain voltage, further advances the saturation region boundary under the main gate. In this model, the peak of the lateral electric field will happen at the drain edge of the virtual gate and as a result electron drift velocity elsewhere along the channel would be equal to or lower than the electron-velocity at this point. Analysis of the results of the complete implementation of the proposed model and the model of Koudymov *et al.* (i.e. based on incorporation of the charged-trapped region in the form of a fully-saturated gate-less HFET modeled in tandem with the gated HFET) is performed in section 2.4.

In this proposed model, electron trapping only in a very thin surface layer is assumed. This assumption is in agreement with the published observations on the permanent current-collapse in AlGaN/GaN HFETs [38] [47]. In this model, electron trapping in deep surface states is considered only at the exposed surface of the barrier layer and not in the AlGaN barrier. This surface charge accumulation is located at the exposed part of the drain access region. According to this assumption, the thickness of this surface layer is assumed to be much smaller than the barrier thickness. The lateral extent of this region along the channel length is marked by the length of the virtual gate.

In order to derive an analytical model, this virtual gate is treated like a second gate with a different gate voltage (V_{G2}) placed in series with the main gate across the channel

(Figure 2.3). This voltage can be identified by the trap concentration profile at drain side of the gate and its occupation probability.

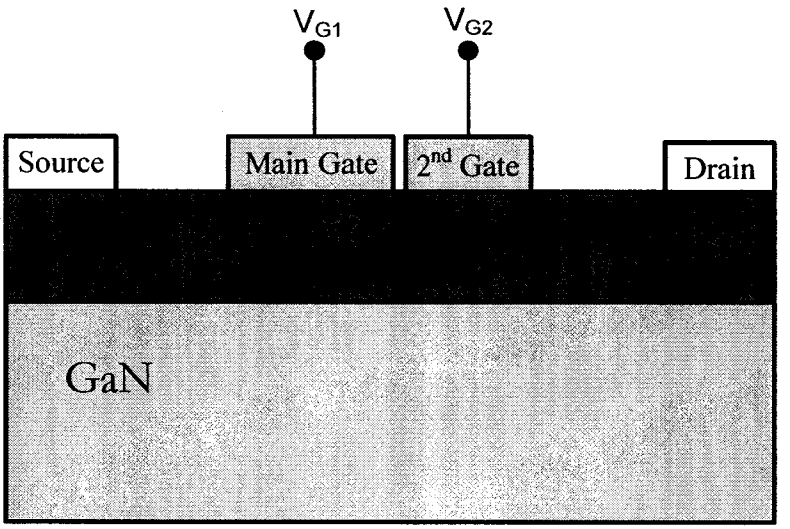


Figure 2.3: Double-gate analogy of the presented analytical model of the effect of virtual gate.

Formation of this virtual gate is assumed to be due to the existence of traps on the surface of the AlGaN. However the source of carriers and the trapping/detrapping time constant by which these traps are occupied or emptied is not of the concern of the current work. For simplicity, the charge trap concentration has been assumed to follow a uniform time-invariable profile. The lateral extent of this profile is also assumed to be bias independent. These assumptions make the current model incapable of shining a light on the dynamics of the transient current-collapse characteristics. However, the current model is fully capable of predicting the permanently-collapsed post DC-stress I/V characteristics of the type reported in [38], [47]. Considering the uniform profile of the trapped-charge concentration, later in section 2.4 the possible impacts of this simplifying assumption will be further elaborated. Since the aim of this work is improvising a very simple analytical model capable of reproducing the experimentally-observed implication of DC-stress, the exact physical properties of the trap-sites (e.g. energy level, emission coefficient, density,

capture cross section,…), and dimensions of the virtual gate are not taken into account.

In this model, for modeling the I-V characteristic of the HFET in presence of the virtual gate, three different regimes have been identified:

1. First regime, occurring at low voltages, where both gates are working below saturation.
2. Second regime, is marked by the commencement of saturation at virtual gate.
3. Third regime surfaces with the full saturation of the virtual gate and the onset of saturation under the main gate.

These three regimes are described further in the following subsections.

2.3.3 Linear regime

For the low values of drain voltages, both gates are working below their saturation point and consequently current-voltage pairs calculated based on the implementation of Koudymov's model under each of the two gates can be easily calculated by adopting (2.2) with appropriate size and potential modifications. In this model, it has been assumed that there is a negligible distance between the two gates and as a result the voltage at the drain side of the main gate is taken equal to the voltage at source side of the virtual gate. By solving the integral in (2.2), the following equations are derived:

$$L_{G1} = -\left\{(aV^2 - 2cV) + (aV + b)\sqrt{V^2 + \frac{2b}{a}V + \left(\frac{c}{a}\right)^2} + \left(\frac{c^2 - b^2}{a}\right) ln\left[d\sqrt{V^2 + \frac{2b}{a}V + \left(\frac{c}{a}\right)^2} + V + \frac{b}{a}\right]\right\}_{V_{G1T}-V_{SG1}}^{V_{G1T}-V_{DG1}} \tag{2.4}$$

$$L_{G2} = -\left\{(aV^2 - 2cV) + (aV + b)\sqrt{V^2 + \frac{2b}{a}V + \left(\frac{c}{a}\right)^2}\right.$$
$$\left. + \left(\frac{c^2 - b^2}{a}\right) ln\left[d\sqrt{V^2 + \frac{2b}{a}V + \left(\frac{c}{a}\right)^2} + V + \frac{b}{a}\right]\right\}_{V_{G1T}-V_{SG1}}^{V_{G1T}-V_{DG1}} \quad (2.5)$$

In which L_{G1} and L_{G2} are the gate length of the main-gate and the virtual gate, respectively. Parameters used in (2.4) and (2.5), based on the v_d-E relationship of (2.1), and other physical parameters of the device are defined as:

$$a = \frac{C_{CH}v_0}{4JF_0}, \quad b = \frac{2F_0 - F_1}{4F_0F_1}, \quad c = \frac{1}{4F_0}, \quad d = 2(C_{CH}v_0F_1)^2, \quad V_{G_xT} = V_{G_x} - V_T$$

The drain I-V characteristic of the device can be developed by performing a simple iterative strategy over (2.4) and (2.5). In this technique, for a definite value of drain-gate voltage (V_{DG1}), it is sufficient to sweep the current density value until (2.4) is satisfied for an assumed length of the virtual gate. The current-voltage pair-values in (2.4) and (2.5) which concurrently satisfy these equations are picked as the desired answers. Considering the current continuity and implementing the simplifying assumption of no gate-current and leakage through substrate, the current density is assumed constant along the channel. As a result, the procedure for solving (2.5) is simplified to sweeping the voltage at drain side of the virtual gate (of pre-assumed length) until the equation is satisfied. This voltage value (i.e. V_{DG2}) is then added to the voltage drop over drain access-region (which is composed of saturated and unsaturated parts) in order to obtain the drain voltage. This procedure is performed for every value of drain-voltage to obtain a complete I-V characteristic. It is worthwhile noting that in this regime, as a check of validity of assumptions, for every value of current and voltage, electron velocity is calculated to ascertain that saturation

velocity is not reached.

2.3.4 Saturation of the second gate

While the voltage on the virtual gate is a pre-assumed value (which is used as a matching parameter to the experimental data), voltage of the main-gate is swept according to the bias topology. Therefore, the I-V characteristics can be divided into three different regimes:

1. Regime of formation of saturation under the virtual gate
2. Regime of full saturation of virtual gate
3. Regime of extension of saturation under the main gate

After the onset of velocity-saturation under the virtual gate, the length of the channel located under this gate will be divided into two regions: saturated and unsaturated. As it was explained earlier in section 2.3.1, under this condition (2.5) needs to be modified as:

$$L_{G2} - \Delta L_2 = -\left\{(aV^2 - 2cV) + (aV + b)\sqrt{V^2 + \frac{2b}{a}V + \left(\frac{c}{a}\right)^2} + \left(\frac{c^2 - b^2}{a}\right) ln\left[d\sqrt{V^2 + \frac{2b}{a}V + \left(\frac{c}{a}\right)^2} + V + \frac{b}{a}\right]\right\}_{V_{G2T}-V_{DG1}}^{V_{G2T}-V_{sat2}} \quad (2.6)$$

where ΔL is the length of the saturated region under the virtual gate and V_{Sat2} is the corresponding saturation voltage.

In agreement with the assumptions of Koudymov *et al.* the voltage drop across the saturated part is calculated by:

$$V_{DG2} - V_{Sat2} = \lambda F_S \sinh\left(\frac{\Delta L_2}{\lambda}\right) \tag{2.7}$$

where λ is the characteristic length of the saturated region and F_S is the saturation field [41].

As the drain voltage increases the length of the depletion region under the virtual gate also increases. Incorporation of this gradual expansion and consequent increase of the voltage drop, as well as the effect of virtual gate on the I-V characteristic before saturation, are the key points of the proposed model.

In the model proposed in [41], the effect of trapped charges has been taken into account through the incorporation of a tandem gate-less HFET of full velocity saturation which is originated in the reduction of charge density in the charge-trapped region. As it is further elaborated in section 2.4, this model has been observed to be incapable of predicting the post DC-stress characteristics especially for the low values of drain-voltage in the observations of the semi-permanently collapsed type. As it will be illustrated later in section 2.4, the full treatment of saturation and expansion of saturation region under the virtual gate in the same fashion as the main-gate, is the fundamental reason for the unsurpassed versatility and accuracy of the presented virtual gate model in matching to the experimental observations.

In this model, depletion region also extends into the gate-drain spacing and as it was explained earlier, the related voltage drop over this region can be incorporated using the model proposed in [46].

2.3.5 Saturation of the main gate

By increasing the drain-voltage, depletion region under the virtual gate will extend until it

is completely saturated while its boundary is arriving at the main gate. This voltage value matches the commencement of saturation under the main-gate. After this point, it is the main-gate which is the dominant gate and the virtual gate acts like a constant voltage drop (i.e. mere parasitic resistance). In this region, (2.6) and (2.7) are applied to the main-gate and after substituting the related parameters, the current and voltage values are calculated. Figure 2.4 shows the flowchart for the implementation of the proposed model.

2.4 Results and discussions

In order to examine the accuracy of the proposed procedure and the model, the analytical relationships are implemented in MATLAB and results are compared with the experimental data. The measurements have been performed on an unpassivated AlGaN/GaN HFET grown by molecular beam epitaxy (MBE) on a SiC substrate. The device has two gate fingers with a gate length of 0.25 μm and a gate finger width of 100 μm. These devices demonstrated permanent (unless UV-illuminated) degradation on the I-V characteristics upon DC-stress, which has been attributed to deep surface trapping [38], [48]. The pre-stress I-V characteristics and post DC-stress I-V characteristics of these devices have been used to validate the results of the proposed model. Further information about the device dimensions and condition of stress has been reported in [38].

Figure 2.5 shows the comparison of measurement and simulation results for the drain I-V characteristics before stress. The demonstrated results are shown for the gate voltages equal to -1.8 V up to -3.4 V with -0.4 V step. A very good agreement between the

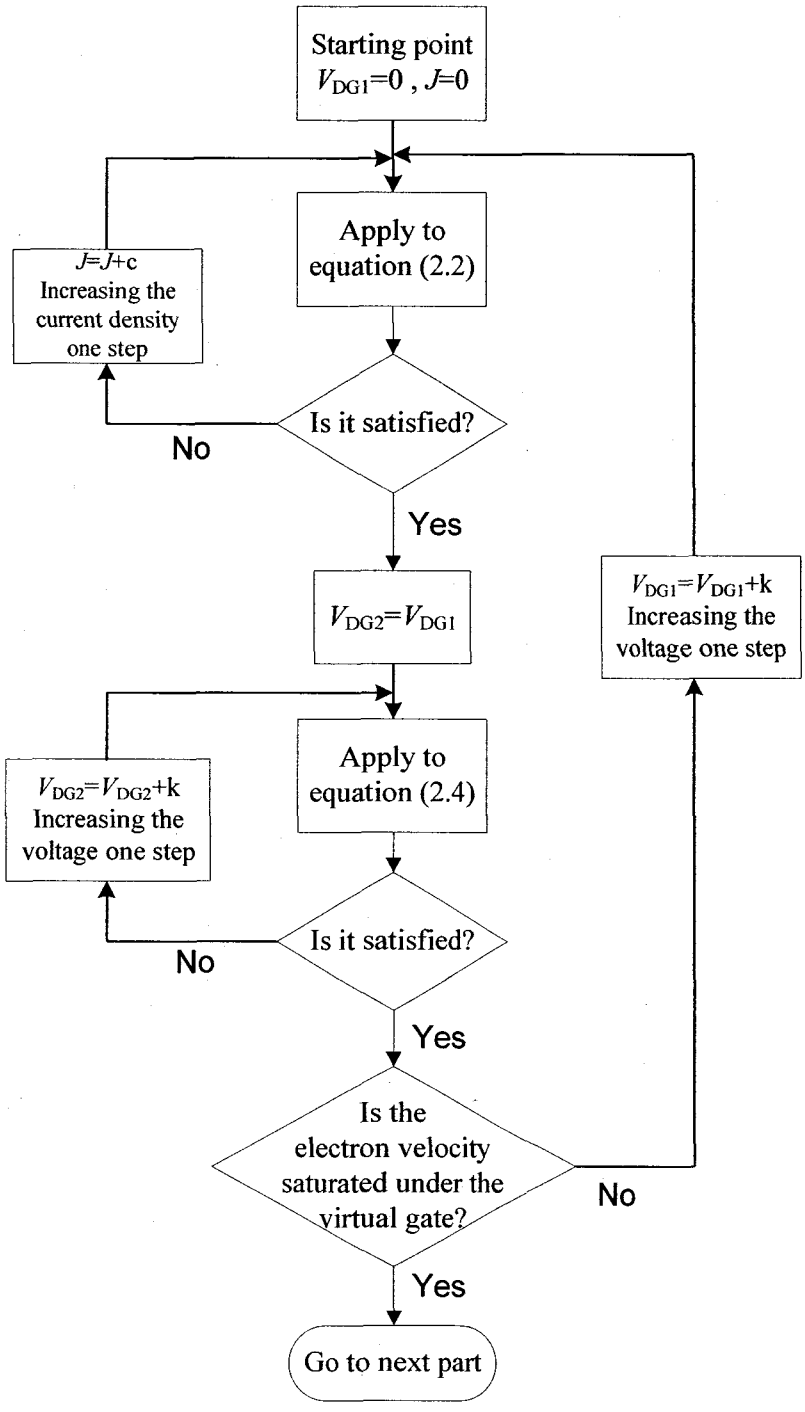


Figure 2.4: Flowchart of the simulation procedure of the proposed model.

experimental data and simulation results is demonstrated which verifies the analytical model of [41] versus our experimental data.

Although this agreement is related to the pre-stress I-V characteristics based on the direct implementation of the model of Koudymov *et al.* [41], it can be concluded that the basics of the post-stress model of this current work and simulation algorithms is accurate. Due to the success of this implementation, the parameters adopted in the simulation of the pre-stress condition are also applied to the model under the post-stress condition. This is crucial since the model proposed for the post-stress behavior of the device is based on this basic model with the major difference of incorporation of two rather than one gates. The complete set of parameters used in these simulations is summarized in Table 2.1.

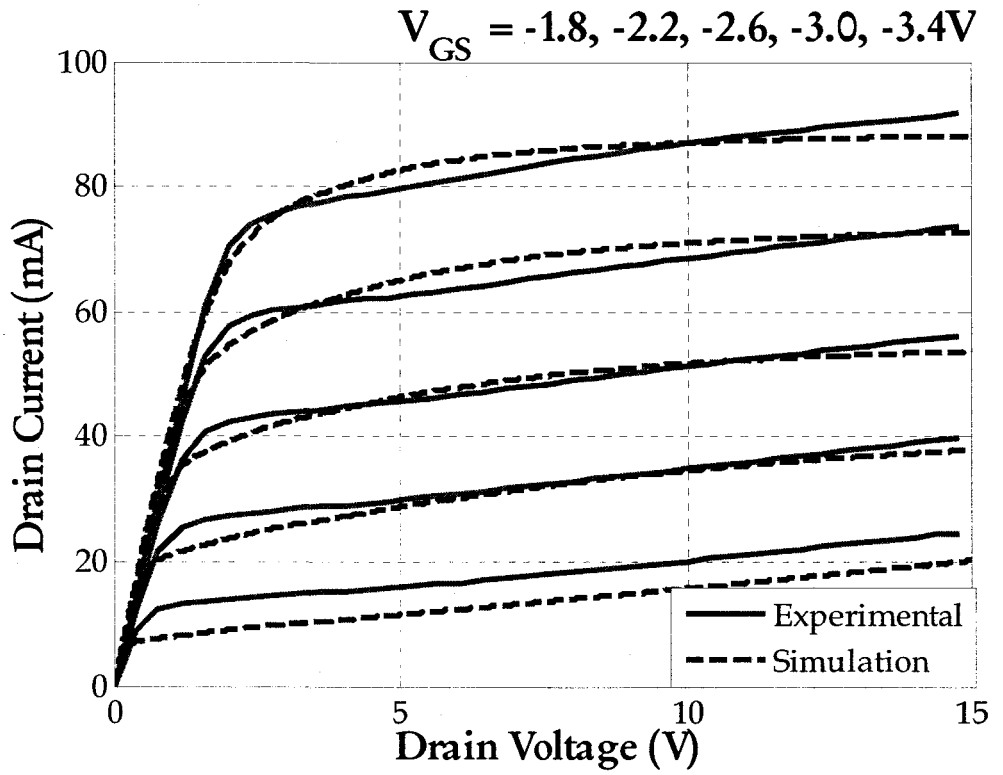


Figure 2.5: Comparison of experimental and simulation results for drain I-V characteristics for V_{GS}=-1.8 V to V_{GS}=-3.4 V in -0.4V steps. Results of simulation are shown in discontinuous representation and continuous graphs are the pre-stress experimental values.

Table 2.1: Parameters used in simulation of pre-stress I-V characteristics.

Symbol	Description	Value
μ_0	Low field mobility	1000 cm^2/V-s
μ_1	High field mobility	50 cm^2/V-s
v_0	Knee velocity	7.2×10^6 cm/s
v_S	Saturation velocity	1.19×10^7 cm/s
d	Barrier thickness	17.5 nm
Δd	2DEG thickness	2 nm
L_{GD}	Gate-drain spacing	1.0 μm
L_G	Gate length	0.25 μm
W	Device width	200 μm
V_T	Threshold voltage	-3.75 V
R_S	Source contact resistance	5Ω
R_D	Drain contact resistance	5Ω
σ_P/q	Donor concentration at the Heterointerface	3×10^{12} cm^{-2}
λ	Characteristic length of saturation region under the gate	45 nm

Figure 2.6 shows the variation of the electric-field along the channel for V_G=-1.8 V at different values of drain voltage before stress. In this figure, the origin is assigned to the source side of the gate and for the special case of V_D=10 V, the region marked from the origin to 0.11 μm defines the unsaturated part of the gate. On this figure, the extension of the saturation region into the drain access-region is marked by arrows. As it is expected, simulation results reveal the extension of the depletion region into the drain-access region while the peak electric-field is increasing. Peaking of the electric field at the drain-edge of the gate has been speculated to be responsible for the instigation of hot-carrier migration to the surface through a number of processes including tunneling or hopping [47], [49].

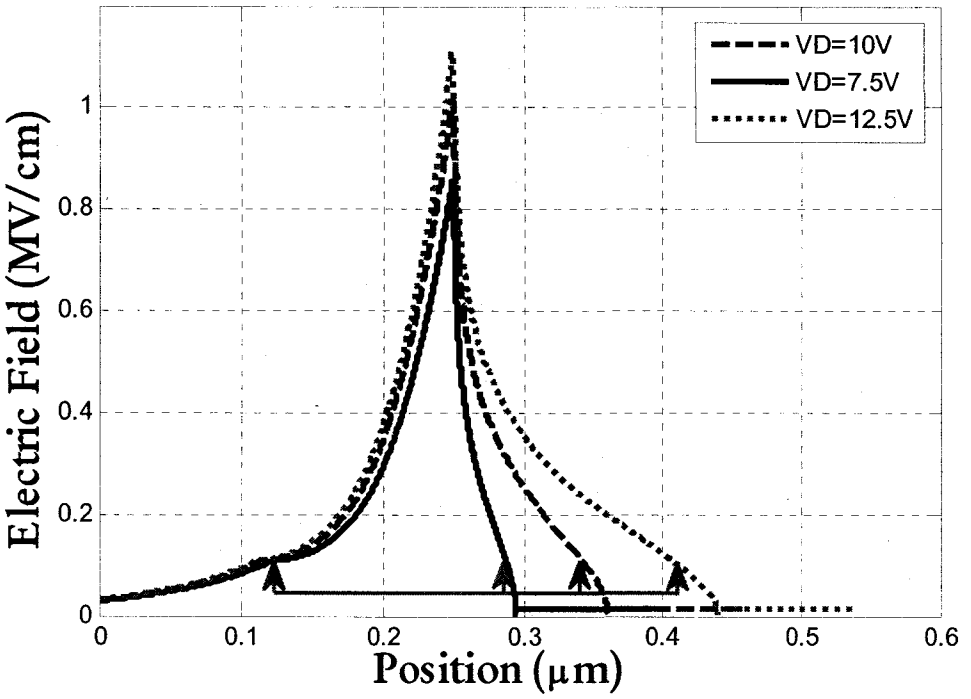


Figure 2.6: Simulated electric-field variations along the channel of a device with no surface trapping for different drain voltages. Arrows show the total depletion length in the channel and its extension by increasing drain voltage.

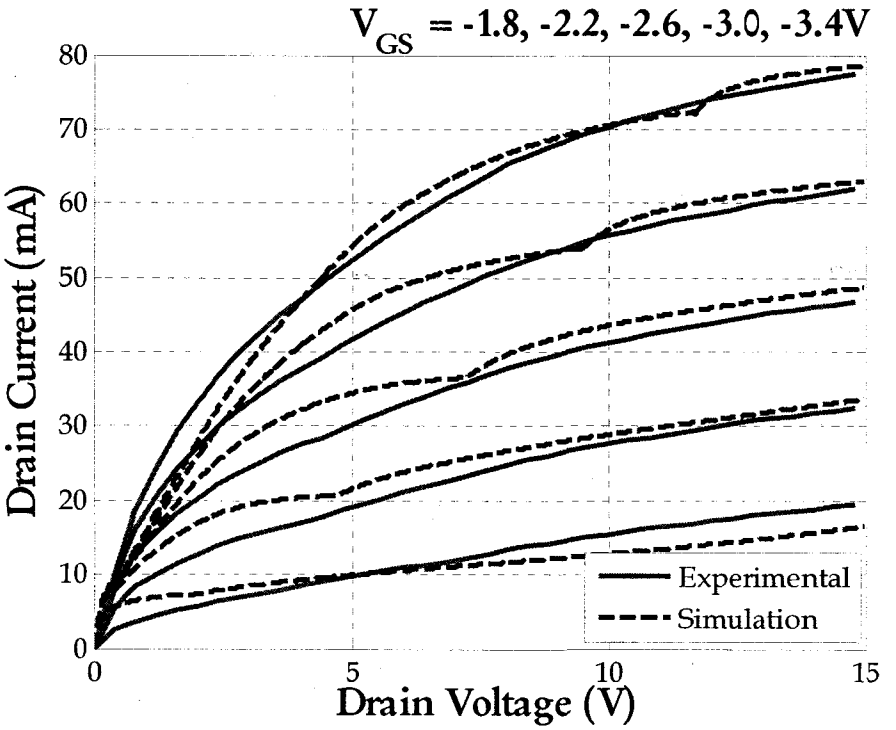


Figure 2.7: A comparison of I-V characteristics for post DC-stress experimental observations (solid lines) and the proposed virtual gate model (dashed lines) for V_{GS}=-1.8 V to V_{GS}=-3.4 V in -0.4 V steps.

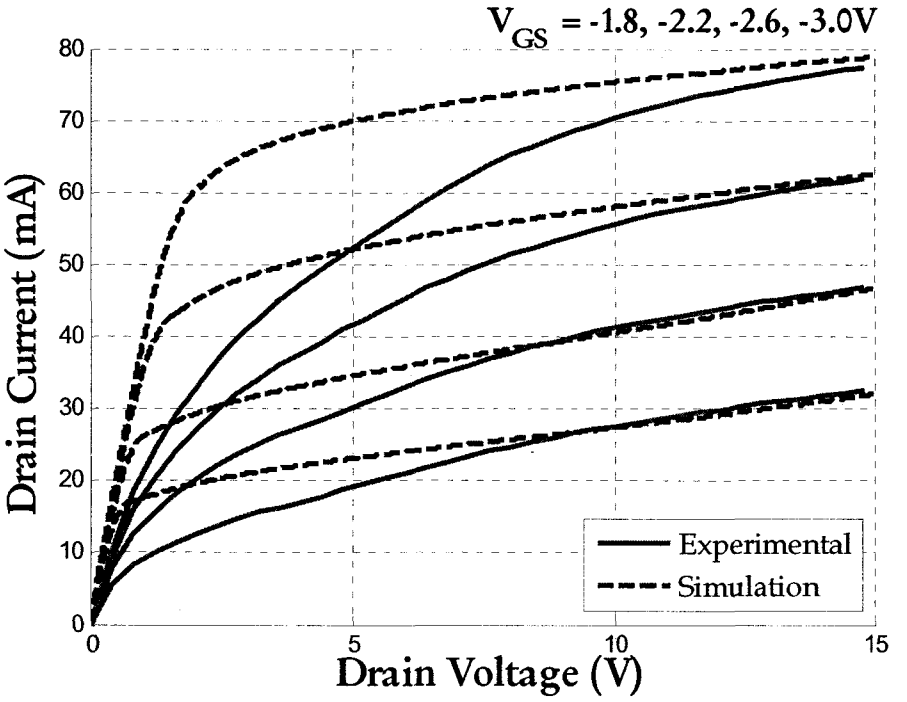


Figure 2.8: A comparison of I-V characteristics for post DC-stress experimental observations (solid lines) and the model of Koudymov *et al.* [41] (dashed lines) for V_{GS}=-1.8 V to V_{GS}=-3.0 V in -0.4 V steps.

Figure 2.7 depicts the simulation results of the proposed model and experimentally observed post DC-stress I-V characteristics. As it is illustrated in this figure, the proposed model closely follows the experimental observations. Figure 2.8, illustrates the best simulation match of the model presented in [41] to this data set. This implementation has been performed with the goal of best matching to drain current at high drain voltage values. Comparison between Figure 2.7 and 2.8 reveals that the complete incorporation of the charge-trapped portion of the drain-access region as a secondary gate with the possibility of partial introduction of velocity saturation along its length can have remarkable impacts on the capability of the model on predicting the drain I-V characteristics, especially for low values of drain-voltage. The results presented for both models are achieved by precise selection of the parameters to realize maximum fitting. The additional parameters used for the simulation of post-stress characteristics are

summarized in Table 2.2. In order to explain the reduction of current levels predicted by the virtual gate modeling at low drain voltages, it should be emphasized that in this model reduction of electron concentration and acceleration of carriers up to the saturation velocity under the short-channel virtual gate is made possible even at low drain voltages.

Table 2.2: Additional parameters used in the simulation of post DC-stress characteristics.

Symbol	Description	Value
L_{G2}	Virtual gate length	35 nm
V_{G2}	Voltage applied to virtual gate	-3.5 V
d_t	Width of trapped region	35 nm
σ_T/q	Trap concentration (used for simulating the model proposed in [41])	2.2×10^{12} cm^{-2}

It should be mentioned that the transition from the regime 2 to 3 (which were explained in the previous section), has introduced negligible kinks in the simulated I-V characteristics of Figure 2.7. It is believed that implementation of a more realistic distribution of trapped surface states in the drain access region would alleviate the kinks currently observed in the simulation results. At higher drain voltages, transition between the dominance of the operation of the virtual gate, defined by the constant distribution profile of surface-trapped charge carriers, and the metal-gate is the cause for this kink in the I-V characteristics. Incorporation of a tapered profile for surface-trapped electron concentration, with its highest value at the maximum-electric-field drain-edge of the gate, is believed to be able to essentially remove the kink. However, this will come at the cost of increasing the complexity of the model and adding to the number of fitting parameters. This approach has been avoided in the implementation of the presented simple analytical model.

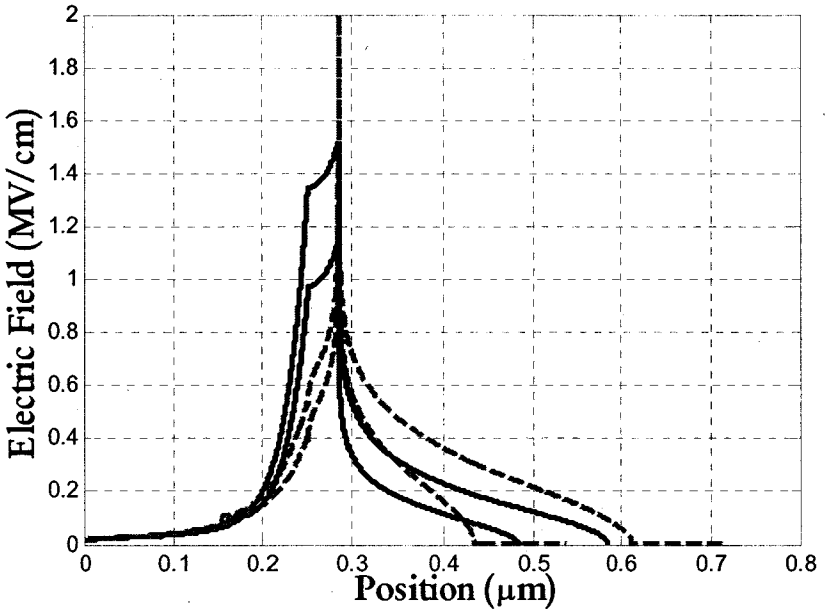


Figure 2.9: Comparison of electric field along the channel after stress using the presented model (solid line) and the model proposed in [41] (dashed line), at V_{DS}=10 V, 15 V and gate voltage of -1.8 V. Further extension in the drain access-region is the result of increasing V_{DS}.

Figure 2.9 compares the variation of the electric-field in the channel of a post-stress device according to the implementation of the virtual gate model of the current work and the model proposed in [41]. Comparison of the outcome of the model of [41] with its pre-stress predictions (i.e. Figure 2.6) reveals the existence of an unphysical singularity in the electric-field characteristics. However, the prediction achieved through the complete implementation of virtual gate, illustrates an electric-field variation of acceptable peak values with no unphysical singularity. While the model of Koudymov *et al.* treats the surface trapping as the addition of a parasitic gate-less HFET in tandem with the device gate, the proposed complete incorporation of the virtual gate is observed to have realistically provided the opportunity of tracking the variation of drain current-voltage characteristics of post DC-stress devices of semi-permanently collapsed type.

Chapter 3

Analytical Modeling of Drain-Current Characteristics of AlGaN/GaN HFETs with Incorporation of Transferred-Electron Effect*

3.1 Abstract

An analytical model, with incorporation of transferred-electron effect, for drain-current characteristics of AlGaN/GaN HFETs is presented. Oftentimes, the transferred electron effect is neglected in modeling the drain-current characteristics of III-V HFETs. This assumption is substantiated based on the quick transfer of electrons through the portion of the channel with electric-field values corresponding to the steady-state peak in the drift-

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velocity. The broader steady-state electron drift-velocity overshoot of GaN in comparison to other direct semiconductors such as GaAs and InP, in addition to the larger difference between the peak and saturation drift-velocity, and the wider bandgap of this semiconductor predict the importance of the incorporation of transferred-electron effect (i.e. steady-state drift-velocity overshoot) in modeling the drain-current of these devices. Although, for the current state of the art of Ohmic contacts in GaN technology, these effects might be masked by the implications of the contact resistance, development of a model capable of predicting the impacts of the transferred-electron effect is worthwhile for understanding the full potentials of this novel semiconductor technology. In order to apply an accurate model, a realistic field-dependent mobility model, which is capable of predicting the negative differential mobility region, is adopted. This closed-form model easily yields an analytically manageable expression for the drain I-V characteristics. Simulation results are compared with the results of the adoption of Ridley's mobility model which does not take into account the transferred-electron effect. Solving the Poisson's equation through a simple iterative method and considering the diffusion component of current are at the core of this model. The iterative nature of this approach has considerably relieved the outcome of the implementation from the choice of fitting parameters.

3.2 Introduction

Over the past two decades the polar III-Nitride family has gained substantial attention from the device and circuit community as an excellent choice for high power microwave applications. This popularity has been mainly caused by the unsurpassed concentration of

polar 2DEG concentration at the III-nitride heterointerfaces and the wide bandgap of AlGaN/GaN heterostructures. Despite the moderate value of low-field electron mobility of GaN in comparison to other compound semiconductors such as GaAs and InP, the larger value of peak electron velocity of this semiconductor makes it suitable for high frequency applications.

In light of the recent developments in further refining the fabrication techniques of AlGaN/GaN HFETs [50], an evermore pronounced need for the development of an accurate model for the prediction of the implications of the particular material characteristics of these heterojunctions on HFETs is being felt. While oftentimes in modeling the drain-current characteristics of long-channel III-V HFETs the steady-state velocity overshoot is overlooked, such an assumption does not seem to be suitable to AlGaN/GaN HFETs which enjoy a much wider steady-state velocity overshoot patterns. In these devices, due to the broadness of this peak, electrons drift under the electric-field values corresponding to the peak drift-velocity in a sizeable proportion of the channel-length. Therefore, in an accurate model the impact of the steady-state velocity overshoot should be carefully represented. In this implementation, electron bunching caused by the evident negative differential mobility necessitates the treatment of the drain-current not only in terms of drift current but also in terms of diffusion current.

So far, a number of approaches based on a variety of numerical and analytical formalisms such as Monte Carlo [51], drift-diffusion and hydrodynamic transport models [52] have been proposed to predict the drain-current characteristics of AlGaN/GaN HFETs. Among these approaches, the analytical charge control models are preferred by engineers due to their lower computational needs and relative ease of intuitive

examination. The degree of complexity of the drift transport model adopted in the drift-diffusion formalism is determinant to the possibility of yielding either an analytical or a numerical model. So far, several electron mobility models have been proposed for AlGaN/GaN heterojunctions. While simpler models such as Ridley's model [44] are preferred in analytical modeling, more elaborate models stand a chance for incorporating further details of the drift transport through the AlGaN/GaN 2DEG (such as steady-state velocity overshoot and inflexion point). These more elaborate analytical models are closely following the trends predicted by the Monte Carlo formalism. With the goal of incorporation of steady-state velocity overshoot in the model, an appropriate mobility model has been adopted which not only provides an accurate representation of electron-transport effect but at the same time yields an analytical solution.

In section 3.3, the adopted drift transport model is described and details of the application of this mobility model to the derivation of an appropriate model for drain-current characteristics of HFETs are presented. In section 3.4, the Einstein's relationship for the diffusion coefficient of a degenerate channel is presented. In section 3.5, results of the application of this model to AlGaN/GaN HFETs are investigated with respect to the variations of drain and source parasitic contact resistances. These results are compared to the outcomes of the application of this formalism if Ridley's mobility model was exploited and also to the experimental current/voltage characteristics.

3.3 Description of the Model

An accurate device design requires an in-depth knowledge of material properties including the electronic transport properties in the given semi-conducting channel. One of

the traditional approaches taken in modeling of electronic devices is the semi-classical approach. In this approach the propagation of wave/particle electron in a semiconductor is seen as the movement of average Newtonian particles over which the Energy-momentum (i.e. E-k) information of an electron-wave is superimposed through the adoption of an appropriate effective mass and series of scattering time constants defined by the Fermi golden rule. The semi-classical framework relieves the device designers from everyday dealing with Schrödinger equation. Such a drift-diffusion transport model is much simpler to implement if the electrons are at the bottom of conduction band. However, as the kinetic energy of electrons increases due to external excitations, electrons will develop a tendency to go through certain variations in scattering rates and they will encounter a larger variety of scattering processes.

Incorporation of scattering mechanisms such as inter-valley scattering and optical-phonon scattering add to the complexity of the implementation of drift-diffusion transport. Specific to the inter-valley scattering from lower-valleys of lower-mass to higher-valleys of higher-mass in conduction band of direct semiconductors such as GaAs, InP, and GaN, in the semi-classical drift transport a steady-state hump prevails in the drift-velocity versus electric-field diagrams (i.e. v_d-E). These behaviours of semiconductors are vigorously studied by physicist by means of Monte Carlo simulations. In the Monte Carlo simulation through incorporation of a random number generator the movement of an ensemble of electrons subjected to scattering processes is studied versus the variation of electric-field.

For different semiconductors there have been a large number of analytical and/or piecewise expressions developed to accurately mimic the predictions of Monte Carol

simulations. However, the adoption of an appropriate transport model to an analytical device model is the result of a compromise between accuracy and the possibility of yielding analytically manageable expressions. In modeling the drain-current characteristics of long-channel III-V HFETs, traditionally the adopted transport models do not take into account the steady-state velocity-overshoot. The adoption of these simplistic models is substantiated by the small width of the hump in the drift-velocity versus electric-field diagrams. Due to this, only in a very small portion of the channel-length electrons traverse under electric-field densities corresponding to the peak velocity. This argument is more prevailing in GaAs than InP in which the steady-state v_d-E possesses a wider hump [53]. The broader v_d-E hump of GaN with respect to InP, and its larger peak velocity signify the importance of the incorporation of a transport model capable of accurately incorporating this steady-state velocity overshoot. Because of the wide bandgap of GaN, HFETs fabricated in this technology are expected to be exposed to electric-field densities larger than those marked by the peak steady-state drift-velocity.

In design of AlGaN/GaN HFET in order to take advantage of the wider bandgap of the semiconductor in extending the breakdown voltage, traditionally the total channel length (i.e. source-drain spacing) amounts to a few microns. As a result, non steady-state velocity overshoot and ballistic transport are not considered in this drift-diffusion treatment of the transport problem. Also, as it is traditionally the case for long-channel FETs in order to keep the model analytically manageable discussions of energy relaxation time constants are avoided [54], [55].

In implementation of the proposed model, the operation is strictly divided between two regions: (1) linear-region for which electron drift-velocity is always lower than the

peak drift-velocity and (2) saturation-region for which the maximum electric-field in the channel has exceeded the value corresponding to the peak drift-velocity. In this model, device is first broken into a series connection of a self-aligned gated HFET and a self-aligned ungated HFET (Figure 3.1) and then in each of these two HFETs the potential drop across the channel for any given value of drain current and gate voltage is calculated according to the two aforementioned regimes. While in sections 3.3.1 and 3.3.2 the model has been presented for the aforementioned regimes in the gated HFET, in section 3.3.3 these models are extended to the ungated channel. The impact of contact resistance is also incorporated in this model through incorporation of contact resistance terms of source and drain (i.e. R_S and R_D, respectively).

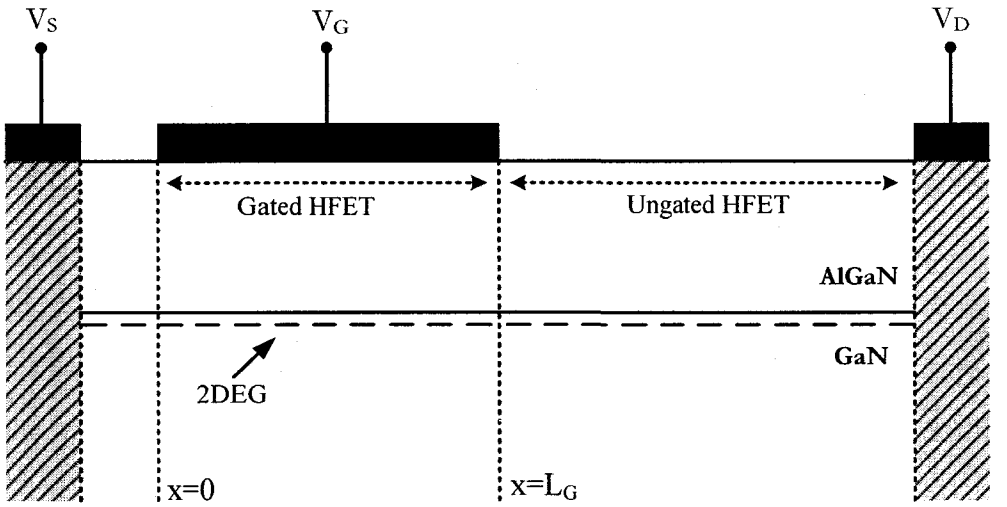

Figure 3.1: Schematic representation of the introduced HFET model.

3.3.1 Linear-region characteristics in the gated channel

Figure 3.1 depicts the device structure of an AlGaN/GaN HFET. In the gated area of an AlGaN/GaN HFET the two-dimensional electron density at the heterointerface, in the presence of a gate bias (i.e. V_G), can be expressed by:

$$qn_s(x) = C_G \times \left(V_G - V_T - V(x)\right)$$

$$\text{where} \quad C_G = \frac{\varepsilon_r \varepsilon_0}{d + \Delta d} \tag{3.1}$$

$V(x)$ is the channel potential and C_G is the gate capacitance per unit area. d is the thickness of the barrier layer (i.e. AlGaN), and Δd is the effective thickness of the 2DEG which is typically about 2-4 nm for AlGaN/GaN 2DEGs [56]. This addition to the barrier thickness is representative of the impact of the series quantum capacitance. V_T is the threshold voltage and ε_r is the relative dielectric constant of AlGaN.

By neglecting the gate-leakage current and diffusion contributions, the current continuity in the device channel under the gate electrode leads to the following expression for the current density per unit width of the device:

$$J_D(^{A}/_{cm}) = qn_s(x)v(x) = v(x)C_G\left(V_G - V_T - V(x)\right) \tag{3.2}$$

In which, $v(x)$ is the electron drift velocity at point x in the channel.

By treating the drift-velocity in the above equation according to Ridley's model [44], which does not include the steady-state velocity overshoot, recently an analytical model for drain-current characteristics of AlGaN/GaN HFETs has been proposed [41]. According to Ridley's drift-transport model of AlGaN/GaN HFETs:

$$v(x) = v_0 E(x)\frac{E(x) + E_1}{E_1(E(x) + E_0)} \quad \left(E_0 = \frac{v_0}{\mu_0},\ E_1 = \frac{v_0}{\mu_1}\right) \quad E(x) \le E_{sat}$$

$$v(x) = v_{sat} \qquad\qquad E(x) > E_{sat} \tag{3.3}$$

While this model with the choice of a few fitting parameters is capable of reproducing the experimental drain-current characteristics of the current state of the art in AlGaN/GaN HFET technology, it fails to accurately incorporate all the features of electronic transport

in an AlGaN/GaN channel. In the present model a more accurate analytical transport model capable of incorporation of transferred-electron effect is adopted from [42]. This model is presented as:

$$v(x) = \frac{\mu_0 E(x) + v_s(\frac{E(x)}{E_1})^5}{1 + (\frac{E(x)}{E_0})^5} \tag{3.4}$$

In order to obtain maximum similarity between the predictions of this model and the Monte Carlo simulation presented in [57], tuning has been carried out on the values of the constants of this model. These values are:

$$\mu_0 = 260 \left(cm^2/_{V.s}\right) , \quad v_s = 2.10 \times 10^7 \ (cm/_s) ,$$

$$E_0 = 15.9 \times 10^4 \ (V/_{cm}) , \quad E_1 = 17.2 \times 10^4 \ (V/_{cm})$$

Figure 3.2 depicts the prediction of this model alongside with those of Ridley's model and the results of Monte Carlo simulations from [57].

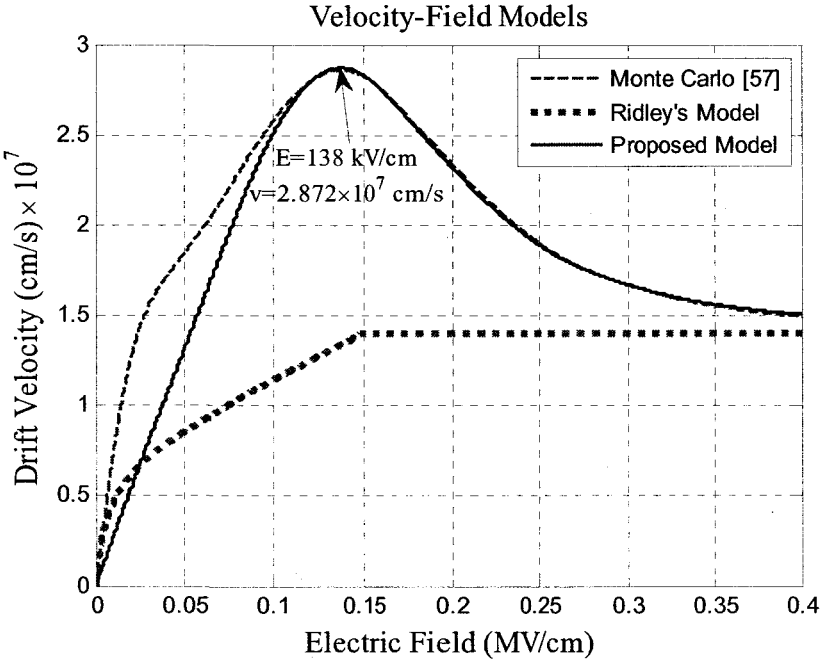

Figure 3.2: v_d-E characteristics of the proposed model presented in (3.4), Ridley's model [44], and Monte Carlo simulation [57].

By plugging this more elaborate transport model in (3.2), the following analytical relationship can be developed for electric-fields smaller than those attributed to negative differential mobility:

$$E(x)^5 + \left(\frac{aV(x)-b}{cV(x)+d}\right)E(x) + \frac{e}{cV(x)+d} = 0 \tag{3.5}$$

where,

$$a = E_1^5\mu_0 C_G, \quad b = E_1^5\mu_0 C_G V_{GT}, \quad c = v_s C_G, \quad d = J_D(\frac{E_1}{E_0})^5 - v_s C_G V_{GT}, \quad e = J_D E_1^5$$

By replacing $E(x)$ with the spatial derivative of channel potential in (3.5) we will have:

$$(\frac{dV(x)}{dx})^5 + \left(\frac{aV(x)-b}{cV(x)+d}\right)\left(\frac{dV(x)}{dx}\right) + \frac{e}{cV(x)+d} = 0 \tag{3.6}$$

The above differential equation is of the form of F(y,y')=0 and it can be rewritten in the form of y=f(y') which can be subsequently solved for the position and channel potential in terms of electric field (i.e. P).

$$y = f(y')$$

$$y' = P \ , \ y = f(P) \ \rightarrow \ dy = f'(P)dP$$

$$dy = Pdx \ \rightarrow \ Pdx = f'(P)dP \ \rightarrow \ dx = \frac{f'(P)}{P}dP \ \rightarrow \ x = \int \frac{f'(P)}{P}dP + c$$

$$\xrightarrow{yields} \begin{cases} y = f(P) \\ x = \int \frac{f'(P)}{P}dP + cte \end{cases} \tag{3.7}$$

In this solution, explicit equation for y(x) might be obtained by possible cancellation of parameter P between the two parametric solutions.

The solution of (3.6) can be obtained as:

$$V = \frac{bP - dP^5 - e}{cP^5 + aP} \tag{3.8}$$

In this solution, the position in the channel under the gate (i.e. x) is related to its corresponding potential value using the parameter P, the value of which denotes the longitudinal electric-field intensity at a given position. By replacing the derivative of (3.8) into (3.7) and integrating, an equation for position in terms of electric-field will be obtained

$$\begin{aligned} x &= \int \frac{-4(ad+bc)P^5 + 5ecP^4 + ae}{P^3(cP^4+a)^2} dP \\ &= \frac{-2(ad+bc)P^5 + ecP^4 - ea}{2aP^2(cP^4+a)} + \frac{ec}{2a\sqrt{ac}} tg^{-1}\left(\sqrt{\frac{c}{a}}P^2\right) \\ &\quad - \frac{\sqrt{2}(ad+bc)}{4ac\sqrt[4]{\frac{a}{c}}}\left(tg^{-1}\left(\frac{\sqrt{2}P}{\sqrt[4]{\frac{a}{c}}}+1\right) + tg^{-1}\left(\frac{\sqrt{2}P}{\sqrt[4]{\frac{a}{c}}}-1\right)\right) \\ &\quad - \frac{\sqrt{2}(ad+bc)}{8ac\sqrt[4]{\frac{a}{c}}} log\left(\frac{P^2 - \sqrt{2}\sqrt[4]{a/c}\,P + \sqrt{a/c}}{P^2 + \sqrt{2}\sqrt[4]{a/c}\,P + \sqrt{a/c}}\right) + cte. \end{aligned} \tag{3.9}$$

The integration constant of (3.9) can be obtained by setting the boundary condition as

$$V(x = 0) = R_S . I_D \tag{3.10}$$

This is based on assuming the role of the source access-region to be presentable through a linear resistive term (i.e. R_S). Due to the low electric-field values and small variation of the electric-field in this region of HFETs, this is an acceptable assumption.

The presented set of formulas are developed for the case that the maximum electric-field intensity in the gated channel (which is occurring at the drain edge of the gate) has not exceeded the corresponding value matched to the maximum steady-state

drift-velocity (marked by $E_{\text{v-max}}$ on Fig 3.2). Equations (3.8) and (3.9) do not provide us with an explicit relationship between the current and voltage at a given location in the channel. Therefore, in order to obtain the dependency of drain-current on drain-source voltage, the drain current density (i.e. J_{D}) is swept to find the suitable value which satisfies the equations. By imposing the condition of not exceeding the peak drift-velocity, this procedure is repeated. The result of this current-sweeping procedure would be a set of corresponding values of V_{DS}^{G} (effective bias boundary of the gate region on the drain side). The procedure is further elaborated as:

1. For a given J_{D}, x is set to L_{G} and P is swept until (3.9) is satisfied (variables d and e must be calculated accordingly).
2. The obtained value for P is substituted into (3.8) to find the related voltage at $x = L_{\text{G}}$ which is V_{DS}^{G}.
3. The constant of integral in (3.9) is found using the boundary condition at $x = 0$.
4. This procedure will continue for the next incremented value of J_{D} until $E(x = L_{\text{G}})$ becomes equal or greater than E_{v-max} which is 138 kV/cm.

For V_{DS}^{G} values for which this electric-field intensity is exceeded at the drain edge of the gate, gated portion of the channel and drain-access region should be divided each into two separate regions: one region in which the maximum electric-field intensity is smaller than E_{v-max} and a region in which electric-fields are larger than this value. In these latter regions, electron bunching caused by negative differential mobility should be investigated. Current continuity and the matching boundary conditions for the electric-field between these regions should be maintained. These cases are treated in sections 3.3.2 and 3.3.3.

Figure 3.3 and Table 3.1 show the simulation flowchart of the linear region of operation and the parameters used in the simulation, respectively.

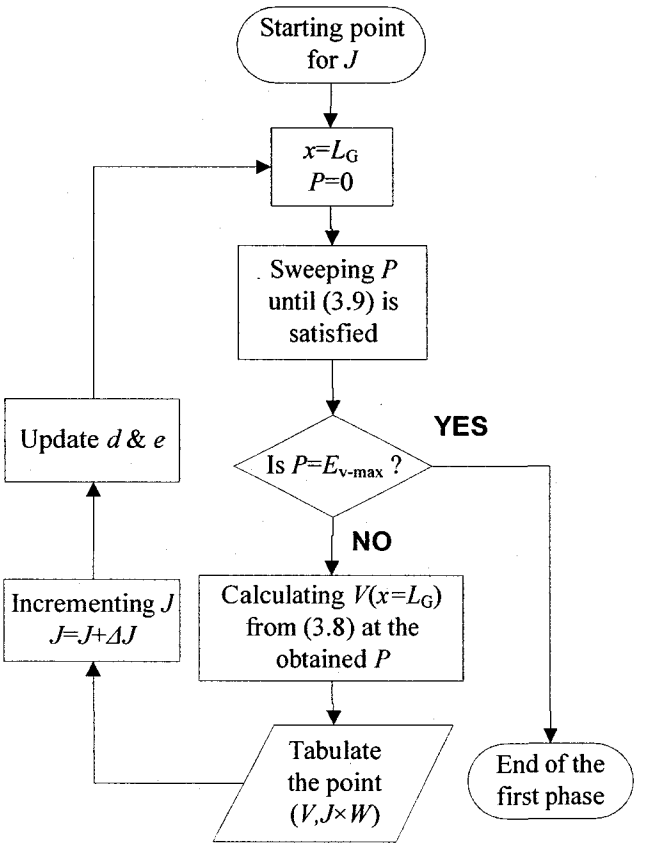

Figure 3.3: Simulation flowchart for the linear region of operation.

Table 3.1: Parameters used in the simulation.

Symbol	Description	Value
d	Barrier thickness	17.5 nm
Δd	2DEG thickness	2 nm
ε_r	AlGaN relative dielectric constant	8.78
R_S	Source contact resistance	5Ω
R_D	Drain contact resistance	5Ω
L_{GD}	Gate-drain spacing	1.0 μm
L_G	Gate length	0.25 μm
W	Device width	200 μm
V_T	Threshold voltage	-3.75 V

3.3.2 Saturation-region characteristics ($v>v_{max}$) in the gated channel

The charge control model presented in section 3.3.1, predicts that the channel at the drain-edge of the gate will be pinched-off as the drain-voltage is increased beyond a threshold voltage. However, such an assumption is in contradiction with current continuity requirements. Nevertheless, for semiconductors that follow a merely saturating v_d-E characteristic such as (3.3), before the inception of the channel pinch-off, the saturation of drift velocity will dictate necessary modification in (3.1) in order to maintain a constant charge concentration in part of the channel with saturated drift velocity. According to these modifications, over the length of the channel with lateral electric-field values greater than or equal to the value corresponding to peak drift velocity, impacts of the lateral and vertical electric-fields should both be incorporated [58]. In the present work, it has been attempted to extend these modifications to a transport characteristic that also incorporates the transferred-electron effect. This is done by applying the Gauss's law to the charge concentration profile in this region of the channel:

$$\oint \vec{E}.d\vec{S} = \frac{Q_{tot}}{\varepsilon_{GaN}} \tag{3.11}$$

In (3.11), Q_{tot} is the total charge enclosed by the surfaces of the Gaussian box, $\vec{E}$ is the electric-field, and $d\vec{S}$ is the surface element. The position of the Gaussian box with respect to the gate electrode and the important electric-field components are marked on Figure 3.4. The bottom of this box is taken well within the GaN layer. Due to the absence of a Z-directed electric-field, the surfaces normal to the Z-coordinate are not taken into account in the integration of (3.11). $\vec{E}_{v-max}$ marks the electric-field at the first point

along the channel for which maximum steady-state drift velocity has been reached. Due to lack of proximity to the gate electrode, vertical electric-field at the bottom surface of Gaussian box is taken to be negligible. This electric-field at the top surface of the box is defined through the parallel plate capacitive field of the gate.

The present model is an extension of the seminal work of Grebene *et al.* [58]. However, due to the presence of transferred-electron effect in the v_d-E characteristics, unlike the assumptions of [58] here the carrier concentration in the Gaussian box cannot be assumed to be constant. Presence of the transferred-electron effect induces carrier bunching and gradient of carrier concentration in the box and as a result the drift-only treatment of the transport problem is not sufficient. With these assumptions, (3.11) can be expanded as:

$$-\left(\int_0^{x'} \frac{Q_n(x")}{\varepsilon_{GaN}} dx" + \frac{qN_{GaN}Y_j}{\varepsilon_{GaN}} x'\right) = E_{v-max}Y_j - E_x(x')Y_j - \frac{\varepsilon_{AlGaN}}{\varepsilon_{GaN}} \int_0^{x'} E_\perp(x")d\,x" \tag{3.12}$$

where the electric-field in AlGaN/GaN heterointerface is

$$E_\perp(x') = \frac{V_{GT} - V(x') + \frac{Q_B}{C_G}}{d + \Delta d} \tag{3.13}$$

Q_B is the total bulk charge in GaN region enclosed by the Gaussian box which can be envisioned in the form of conduction band bending shown in the inset of Figure 3.4. By differentiating (3.12) with respect to x' following relationship is derived

$$\frac{\partial E_x(x')}{\partial x'} + \frac{\varepsilon_{AlGaN}}{\varepsilon_{GaN}Y_j} E_\perp(x') = \frac{Q_n(x')}{Y_j\varepsilon_{GaN}} + \frac{qN_{GaN}}{\varepsilon_{GaN}} \tag{3.14}$$

Q_n is the sheet charge density and it is not assumed to be constant:

$$Q_n(x') \simeq C_G\left(V_{GT}{}' - V(x')\right) \tag{3.15}$$

while in defining the charge carrier density a different definition for effective gate voltage (i.e. $V_{GT}{}'$) has been used instead of V_{GT}. $V_{GT}{}'$ is defined as $V_G - V_T(x)$, in which the threshold voltage unlike V_T in (3.13) is taken as a position dependent quantity. This definition is not foreign to the formalism of Grebene *et al.* [58]. In their model through assuming a fixed carrier concentration in the Gaussian box essentially they have cancelled the position dependency of channel potential by the same type of position dependency implicitly assumed for the threshold voltage. While for saturating transport models such as Ridley's mobility model for GaN, the position variation of channel potential and threshold voltage cancel each other out, in transport models such as (3.4) which is adopted to the present model, presence of transferred-electron effect causes these two profiles to be different than one another. The consequence of this would be electron-bunching inside the Gaussian box which in turn induces a diffusion current component. According to the assumption of current continuity such an element of current should be accounted-for through recalculating the value of drift current at any given point

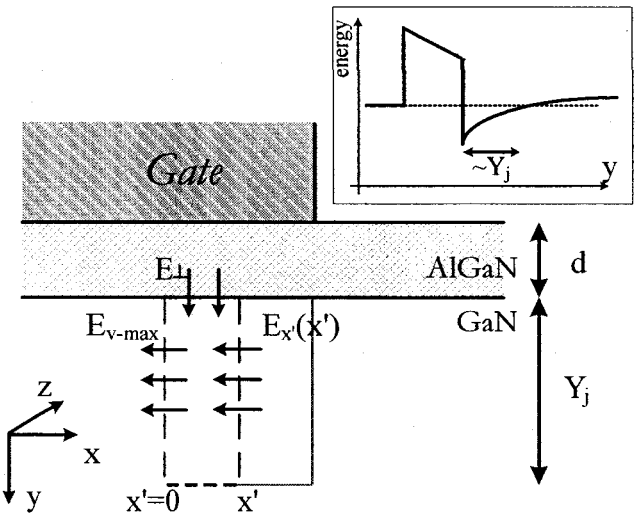

Figure 3.4: Geometry of the Gaussian box in the saturation region of the device. Schematic drawing of the conduction band bending is shown in the inset.

in parts of the channel with electric-field values greater than or equal to $E_{v\text{-}max}$. This procedure is further elaborated in this section.

By substituting (3.15) and (3.13) into (3.14), the following equation is resulted:

$$\frac{\partial E_x(x')}{\partial x'} + \frac{C_G}{\varepsilon_{GaN} Y_j}\left(V_{GT} - V(x') + \frac{Q_B}{C_G}\right) = \frac{C_G}{\varepsilon_{GaN} Y_j}\left(V_{GT} - V(x')\right) + \frac{qN_{GaN}}{\varepsilon_{GaN}} \tag{3.16}$$

which can be simplified as:

$$\frac{\partial E_x(x')}{\partial x'} + \alpha V_T(x') = \beta \qquad \alpha = -\frac{C_G}{\varepsilon_{GaN} Y_j}, \qquad \beta = -\frac{V_T C_G}{\varepsilon_{GaN} Y_j} \tag{3.17}$$

or

$$\frac{\partial E_x(x')}{\partial x'} = \alpha\left(V_T - V_T(x')\right) \tag{3.18}$$

In order to calculate the position dependency of the threshold voltage inside the Gaussian box the form of the variation of channel-potential and lateral electric-field calculated according to the model of Grebene *et al.* are adopted as initial guesses. These initial guesses are represented as [58]:

$$E(x') = E_{v-max} \times cosh\left(\frac{x'}{\lambda}\right) \tag{3.19}$$

$$V(x') = V_{D-v-max} + \lambda E_{v-max} \times sinh\left(\frac{x'}{\lambda}\right) \tag{3.20}$$

$V_{D\text{-}v\text{-}max}$ is the channel potential at the left side boundary of the Gaussian box. In here the parameter λ is taken to be 30 nm. This value is taken within the range of values previously chosen in modeling AlGaN/GaN HFETs without incorporation of transferred-electron effect [41]. As it is explained later in this section, because of the iterative implementation of the present model, final result will be independent of the choice of this parameter.

By taking (3.19) and (3.20) as initial guesses the position variation of drift-velocity can be calculated according to (3.4):

$$v(x') = \frac{\mu_0 E(x') + v_s \left(\frac{E(x')}{E_1}\right)^5}{1 + \left(\frac{E(x')}{E_0}\right)^5} \tag{3.21}$$

The initial guesses for the profiles of threshold voltage and carrier concentration inside the Gaussian box can then be calculated as:

$$V_T(x') = V_G - V(x') - \frac{J_D}{C_G \times v(x')} \tag{3.22}$$

$$Q_n(x') = \frac{J_D}{v(x')} = \frac{J_D\left(1 + \left(\frac{E(x')}{E_0}\right)^5\right)}{\mu_0 E(x') + v_s\left(\frac{E(x')}{E_1}\right)^5} \tag{3.23}$$

The flowchart for implementation of this model is presented in Figure 3.5. According to this flowchart, in the first iteration through incorporation of (3.19) and (3.20) in (3.21), (3.22) and (3.23), initial guesses for profiles of drift velocity, threshold voltage, and carrier concentration are calculated. Due to the position dependency of the carrier concentration it is obvious that the threshold voltage calculated in (3.22) should now be modified through incorporation of the diffusion current. This is done through subtraction of the following diffusion current term from J_D in (3.22):

$$J_{diff}(x') = D_n(x')\frac{dQ_n(x')}{dx'}$$

where (3.24)

$$D_n(x') = \frac{k_B T}{q}\mu(x') \quad and \quad \mu(x') = \frac{v(x')}{E(x')}$$

In calculating the diffusion constant (i.e. D_n) in terms of the linear electron mobility (i.e. μ_n) position dependency is considered through the profile of electric-field

incorporated in $v(x')$. In these equations k_B is the Boltzmann constant, T is the temperature in Kelvin and q is the charge of an electron. In the proposed model, for reducing the math intensity, a simple form of Einstein's relationship has been adopted. However, it should be clarified that this form is not fully applicable to degenerate semiconductors such as the 2DEG channel of an HFET. Nevertheless, later in the next section in the inset of Figure 3.14 the variation of $D_n(x')/\mu(x')$ with respect to k_BT/q for the range of electron energies of interest in these situations is illustrated. This is further elaborated in section 3.4. Without the incorporation of position dependency of this factor, the author has later engaged in comparing the outcome of this simulation versus the outcome of adoption of the maximum deviation of $D_n(x')/\mu(x')$ from k_BT/q throughout the length of the Gaussian box. As shown in section 3.5, results demonstrate that this simplifying assumption minimally impacts the accuracy of the model.

As it is demonstrated in the flowchart of Figure 3.5, after the implementation of the proposed correction on the profile of threshold voltage, $V_T(x')$ is applied to (3.18) to calculate a new profile for electric-field and potential variation in the channel with the use of appropriate boundary condition obtained in section 3.3.1. The aforementioned procedure is then repeated with the corrected profiles of electric-field and channel potential until convergence is obtained. The procedure is then followed by incrementing the current and calculating a value of channel potential at the end of region II. The inner loop of this flowchart is explaining a situation in which the maximum electric-field in the channel has exceeded the onset of saturation in drift velocity. In this portion of the channel as indicated in this loop, (3.19) and (3.20) should be applied to calculate the potential drop across the channel for the given drain-current as proposed in [58].

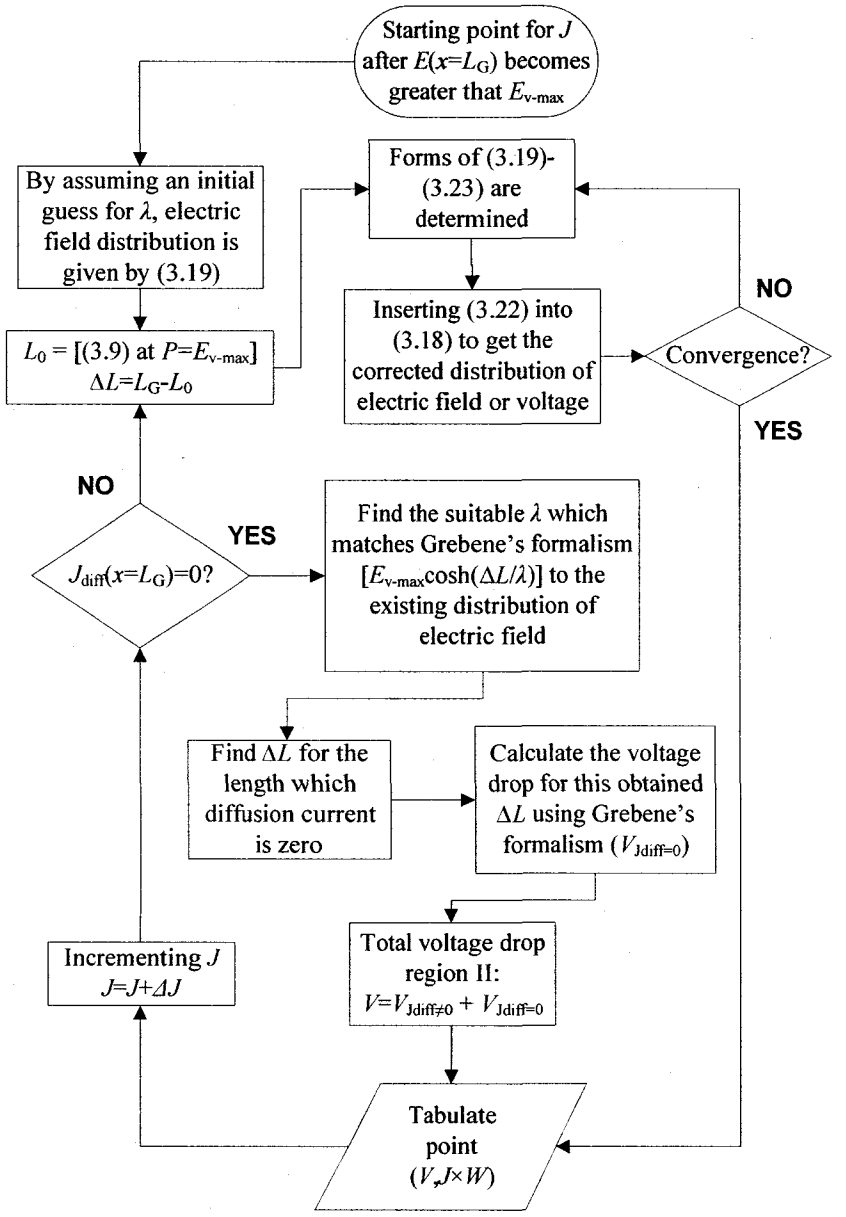

Figure 3.5: Simulation flowchart for the saturation region. Incrementing J will be stopped when reached to the maximum intended current density.

As it is explained in section 3.4, convergence of electric-field and channel-potential profiles is quite insensitive to the initial value taken for parameter λ.

3.3.3 Current-voltage characteristics of the ungated HFET

As it was stated earlier, the present model engages in studying an HFET as a series combination of two self-aligned HFETs: one gated HFET and an ungated HFET. The

channel of each of these two regions can in-turn be divided into regions of operation under linear- and saturation-regimes depending on the maximum lateral electric-field (Figure 3.6). Just for the sake of modeling, the charge carrier of the ungated HFET should be assumed to be of opposite polarity. Such a model assumes that right at the gate edge of the drain there exist an imaginary Ohmic contact which acts as the drain of the two HFETs. Due to this reason, for this plane of negligible width the electric-field variations calculated by the model will not be highly accurate.

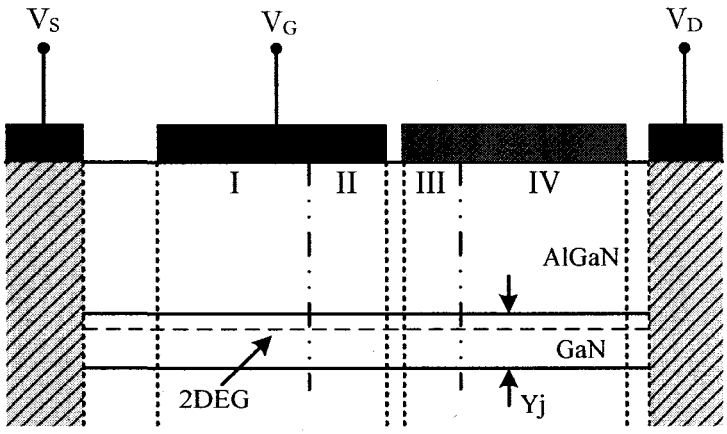

Figure 3.6: Schematic cross section of the four regions in the presented HFET model. Surface of the ungated HFET of the drain access region is shown in lighter shade.

The formalism presented in sections 3.3.1 and 3.3.2 can be easily extended to model the behaviour of the channel of the ungated HFET of drain access-region. The only difference between these two channels is that while in the gated channel the existence of a gate metal with a certain metal work function and a certain value of applied bias create an equipotential surface, over the surface of the drain access-region ideally such an environment is not present. However, it should be emphasized that such an observation is made based on the ideal theory of metal semiconductor junctions. In reality, due to the presence of surface states, the barrier height of a Schottky contact is quite independent of the metal work function. In AlGaN/GaN material system, existence of a large

concentration of surface states is believed to pin the surface potential and make it quite resilient to the choice and even existence of a metal gate [59]. Consequently, in modeling of the drain access-region only the following changes to the models presented in sections 3.3.1 and 3.3.2 are deemed sufficient.

In modeling regions III and IV in Figure 3.6, the assumed surface potential for drain-access region that takes the role of the gate voltage of the gated HFET, is determined by satisfying the electric-field continuity condition at $x=L_G$. Simulation procedure for region III is very similar to region II and also region IV closely follows the model applied to region I. These procedures are applied by the application of appropriate channel-length and also surface potential instead of gate voltage.

In modeling region III, in absence of an actual gate voltage, the role of the apparent spatial variation of the surface potential can be lumped into the variation in threshold voltage that is incorporated in (3.15) in section 3.3.2. This is a practical assumption because in this model it is $V_G(x') - V_T(x')$ that is later used for calculating the current-voltage characteristics. As a result, by taking $V_G(x')$ throughout region III to be equal to the fixed quantity calculated by the electric-field continuity at the drain-edge of the gate, no information will be lost. The flowchart of the model in region IV is shown in Figure 3.7.

3.4 Diffusion constant modification

As it was explained in Chapter 1, HFET structures form a degenerate 2DEG at the heterointerface. Therefore, the commonly used Einstein's relationship of (3.24), which has been developed for non-degenerate semiconductors, needs to be corrected for the use

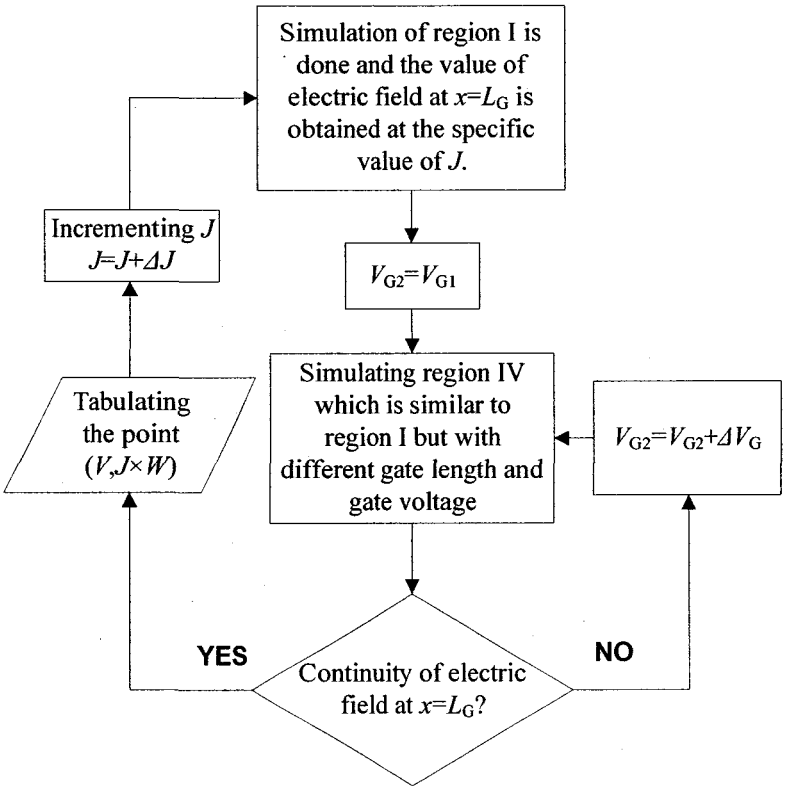

Figure 3.7: Simulation flowchart for region IV.

under such circumstances.

Considering the fact that under equilibrium conditions the total current inside the semiconductor is zero, it can be written that:

$$J_n = nq\mu_n E + qD_n \frac{dn}{dx} = 0 \tag{3.25}$$

$$where\ E = \frac{1}{e}\frac{dE_C}{dx}$$

The presence of degeneracy requires the full consideration of Fermi-Dirac statistics (rather than Maxwell-Boltzmann statistics) in calculation of electron concentration. By considering the Fermi-Dirac statistics, the Fermi-Dirac integral of order j has the following form:

$$F_j(\eta) = \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{\xi^j d\xi}{1+e^{\xi-\eta}} , \qquad \eta = \frac{E_F - E_C}{K_B T} \tag{3.26}$$

where η is the reduced Fermi level and j=1/2 [60]. Therefore

$$\frac{dn}{dx} = -\frac{e}{K_B T}\frac{dn}{d\eta} E \tag{3.27}$$

Substituting (3.27) into (3.25), we obtain

$$\frac{D_n}{\mu_n} = \frac{K_B T}{q} \cdot \frac{n}{dn/d\eta} \tag{3.28}$$

In the non-degenerate limit $\frac{n}{dn/d\eta}$ becomes one. However, in a degenerate semiconductor that is not the case. In this case:

$$n = N_C F_{\frac{1}{2}}(\eta) , \qquad N_C = 2\left(\frac{2\pi m^* K_B T}{h^2}\right)^{3/2} \tag{3.29}$$

$$\frac{d}{d\eta} F_j(\eta) = F_{j-1}(\eta) \tag{3.30}$$

$$\frac{n}{dn/d\eta} = \frac{\Gamma(1/2)}{\Gamma(3/2)} \left[F_{1/2}(\eta)/F_{-1/2}(\eta)\right] \tag{3.31}$$

In [60] correction factor in (3.31) is calculated and plotted for different values of η, the value of which for the case of maximum electric-field of the device studied here is equal to 7.692 and therefore the correction factor for this value will be equal to 5.317.

Later in Figure 3.14 a comparison of the simulation result of I-V characteristics considering the correction factor and the one obtained with application of simple Einstein relationship is shown. As it is depicted there, there is a negligible difference between two

results. Therefore, it has been concluded that employing the simple form of Einstein relationship in the presented calculation has been precise enough.

3.5 Simulation results and discussions

The device structure and material parameters for the AlGaN/GaN HFET used in the simulations, unless identified otherwise, are listed in Table 3.1. Figure 3.8 shows an example of the convergence of the electric-field, channel potential distribution, diffusion current, and threshold voltage in region II of the channel. This figure illustrates that the simulation procedure reaches to an acceptable level of convergence after three steps of iterations (shown in full curve). This level of convergence has been verified for all possible parameters.

In Figure 3.9, comparison is made between the calculated drain-current (i.e. I_D) versus drain-source voltage (i.e. V_{DS}) for gate-source voltages (i.e. V_{GS}) of -1.8, -2.2, -2.6, -3.0, and -3.4 V based on the discussed model (i.e. solid curve) and the simpler implementation of the model according to the saturating mobility model of Ridley [44] (i.e. broken curve). At higher gate voltages a larger difference is observed between the predictions of the two models. At higher V_{GS} values, the observed lower drain-current for low V_{DS} values in the presented model can be explained by smaller electron mobility of the adopted mobility model of the present work in comparison to the predictions of

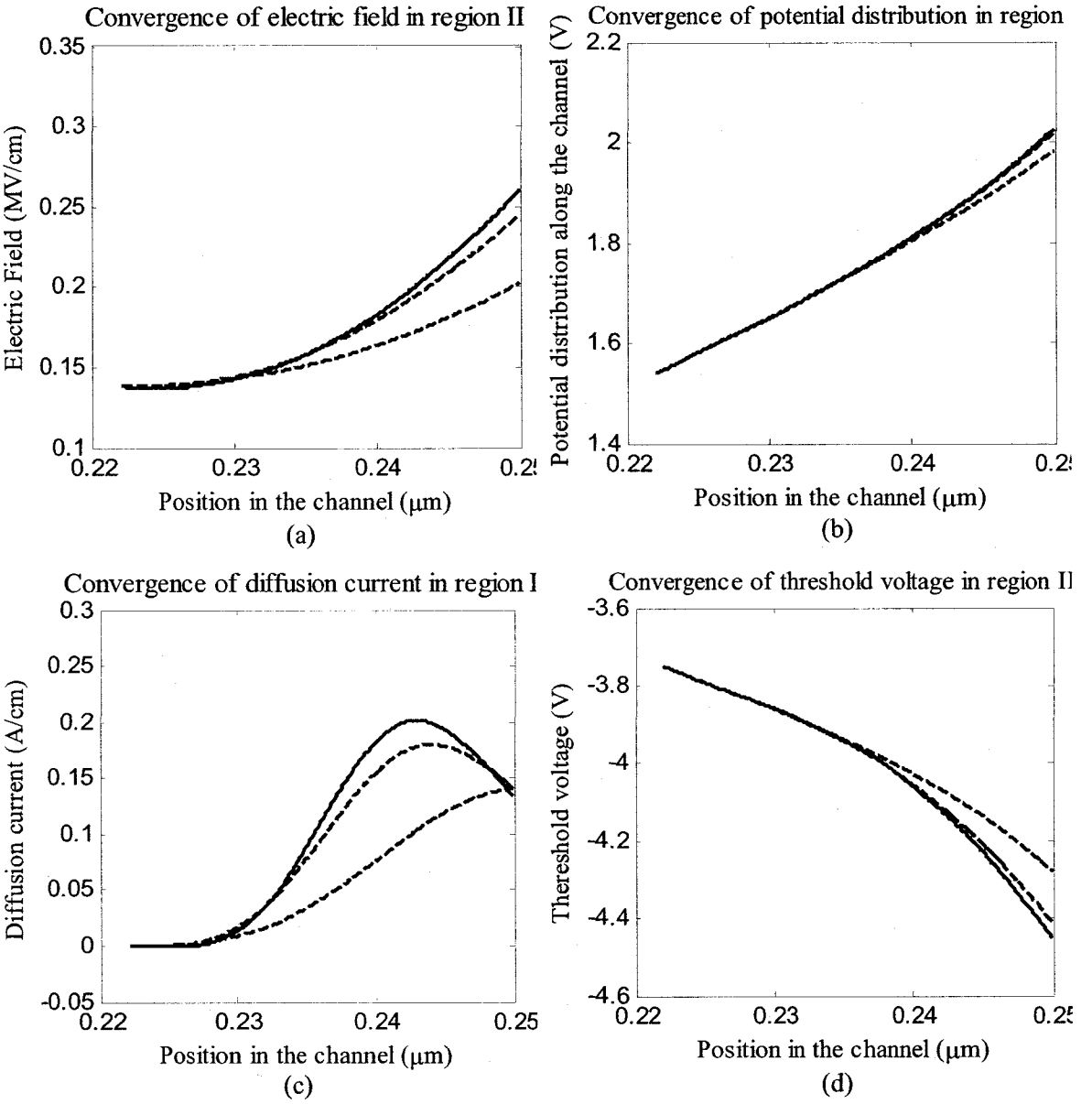

Figure 3.8: Convergence of electric-field (a), channel potential distribution (b), diffusion current (c), and threshold voltage distribution (d) in region II after three steps of iteration for V_{GS}=-1.8 V, I_D=94 mA , R_S= R_D=5 Ω, and L_G=0.25 μm. Convergence is achieved to the curve shown in full line. The curve farther removed from this curve is the initial guess.

Ridley's mobility model. For moderate electric-fields corresponding to larger V_{DS} values such a trend is reversed and as a result the present model is observed to predict higher drain currents. This is most observable farther from the pinch-off condition. According to Figure 3.2, at the electric-field of about 35 kV/cm the drift velocity according to the

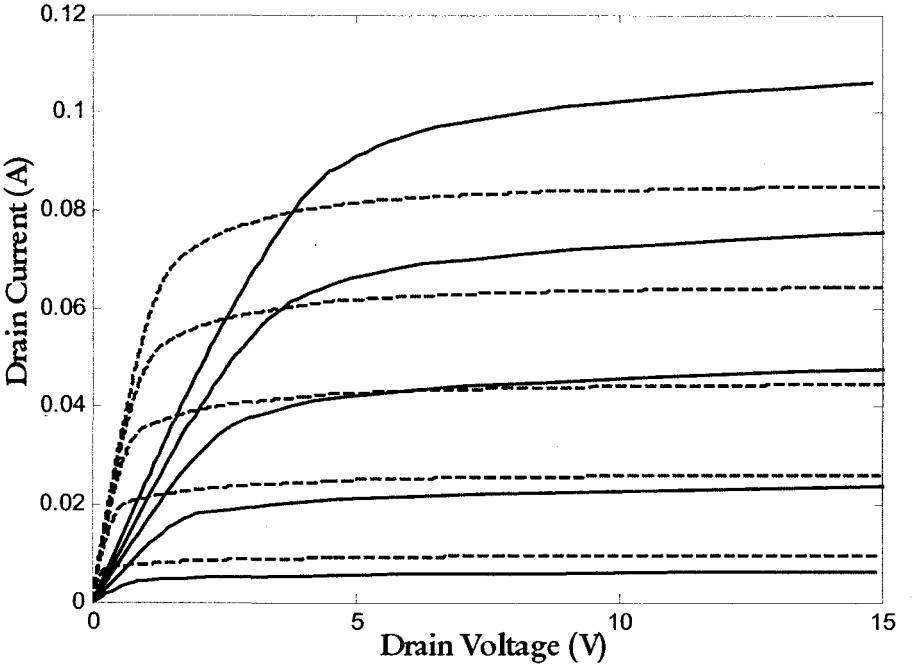

Figure 3.9: I-V characteristics based on the proposed model (solid line) versus the adoption of Ridley's mobility model (dashed line) for V_{GS}=-1.8 V to -3.4 V with the step of -0.4 V.

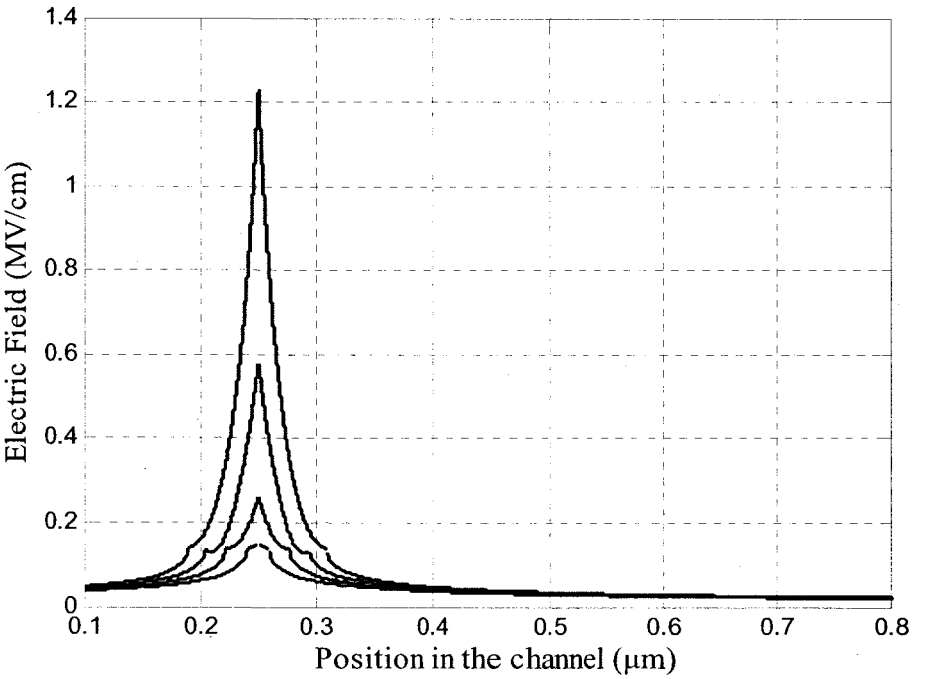

Figure 3.10: Electric-field along the channel for V_{GS}=-1.8 V and I_D= 90, 94, 98 and 102 (mA).

adopted mobility model of (3.4) surpasses the indicated value of Ridley's model. This

point is reached at the exact drain-source voltage for which the aforementioned transition happens. The electric-field along the channel for V_{GS}=-1.8 V for different drain currents is also depicted in Figure 3.10.

The impact of the choice of the mobility model with respect to contact resistance is also investigated. Figures 3.11 and 3.12, illustrate the result of the implementation of the proposed model for the two mobility models expressed in (3.3) and (3.4) for Ohmic contact resistance of 0 and 20 Ω, respectively. As is shown in Figures 3.9, 3.11, and 3.12, the difference between the predictions of the two models increases with the reduction of the contact resistance. As it is illustrated on Figure 3.12, the saturation current levels of the two mobility models are very close for R_S and R_D of 20 Ω. This study shows that the masking effect of parasitic features such as contact resistance can reduce the impact of the transferred-electron effect on the I/V characteristics. With the evermore pronounced goal of improving the contact resistance in III-Nitride technology [50], [61], such features should be emphasized in modeling.

The proposed model with simple adoption of Ridley's mobility model has been matched to an experimental set of I/V characteristics. Measurements have been performed on an AlGaN/GaN HFET grown by molecular beam epitaxy (MBE) on a SiC substrate. The device has two gate fingers with a gate length of 0.25 μm and a gate finger width of 100 μm. As shown in Figure 3.13, a good match is achieved to the experimental values. This is an indication of larger parasitic contact resistance at Ohmic contacts of this device. However, due to the prediction of Figures 3.9, 3.11, and 3.12, with the improvement in the quality of Ohmic contacts, among other technological improvements

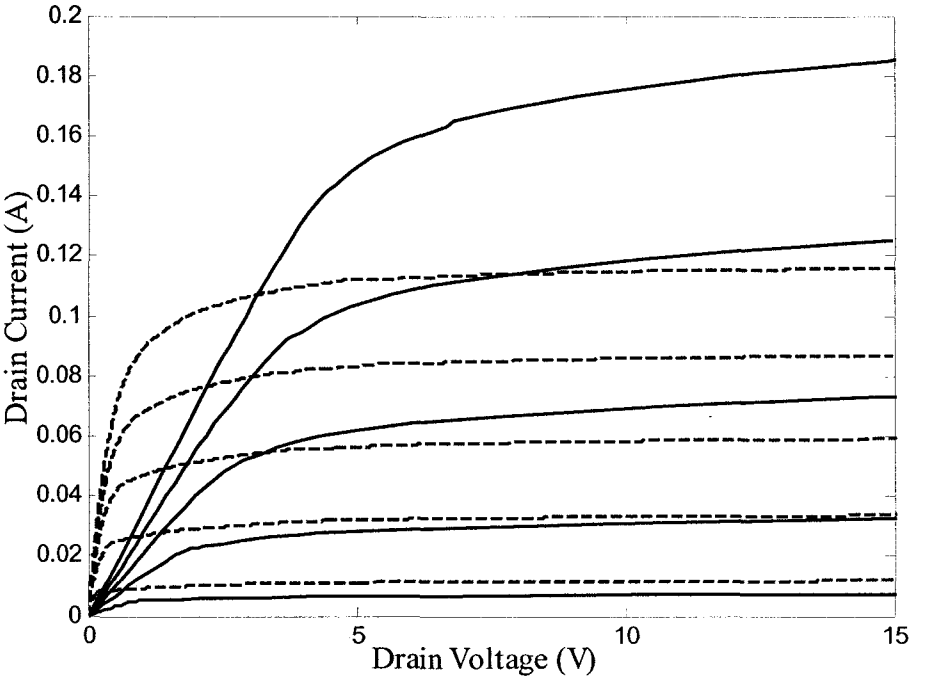

Figure 3.11: I-V characteristics based on the proposed model (solid line) versus the adoption of Ridley's mobility model (dashed line) with the assumption of R_S=R_D=0 Ω for V_{GS}=-1.8 to -3.4 V with the step of -0.4V.

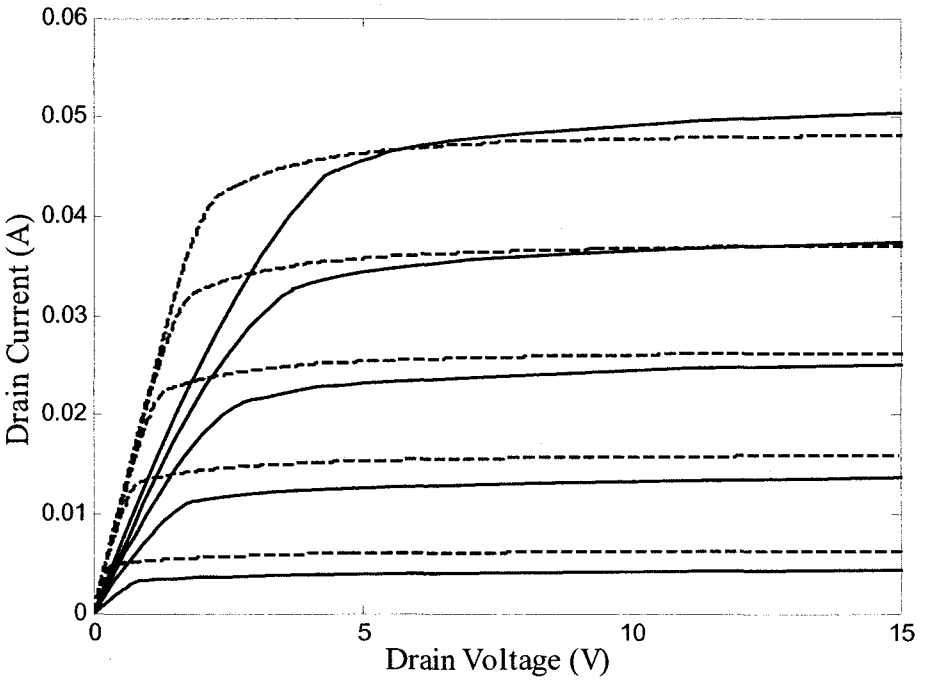

Figure 3.12: I-V characteristics based on the proposed model (solid line) versus the adoption of Ridley's mobility model (dashed line) with the assumption of R_S=R_D=20 Ω for V_{GS}=-1.8 to -3.4 V with the step of -0.4V.

such as improvement in material and interface quality, the implementation of the full model based on adoption of the mobility model presented in (3.4) will be inevitable.

In the presented model, transferred-electron effect was included through calculation of diffusion current in regions II and III. However, the inclusion of diffusion current according to (3.24) does not consider the degeneracy of the 2DEG channel. In order to study the impact of this degeneracy, the correction factor for the full Einstein relationship of a degenerate channel is calculated (section 3.4). Despite the fact that this factor is an energy dependent factor which as a result is evidently position dependent, the adoption of the maximum correction factor throughout regions II and III, as a worst case scenario, as indicated in Figure 3.14 shows that the assumption of (3.24) has been considerably inconsequential.

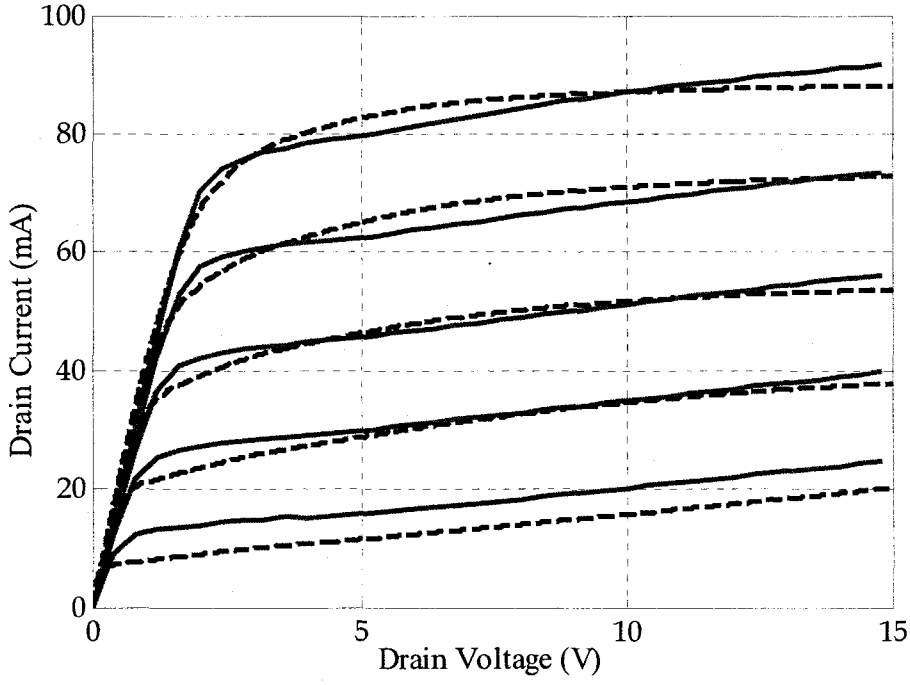

Figure 3.13: Comparison of experimental measurements and simulation results for drain I-V characteristics for V_{GS}=-1.8 V to V_{GS}=-3.4 V in -0.4 V steps. Results of simulation are illustrated in broken lines. Continuous graphs illustrate the experimental values.

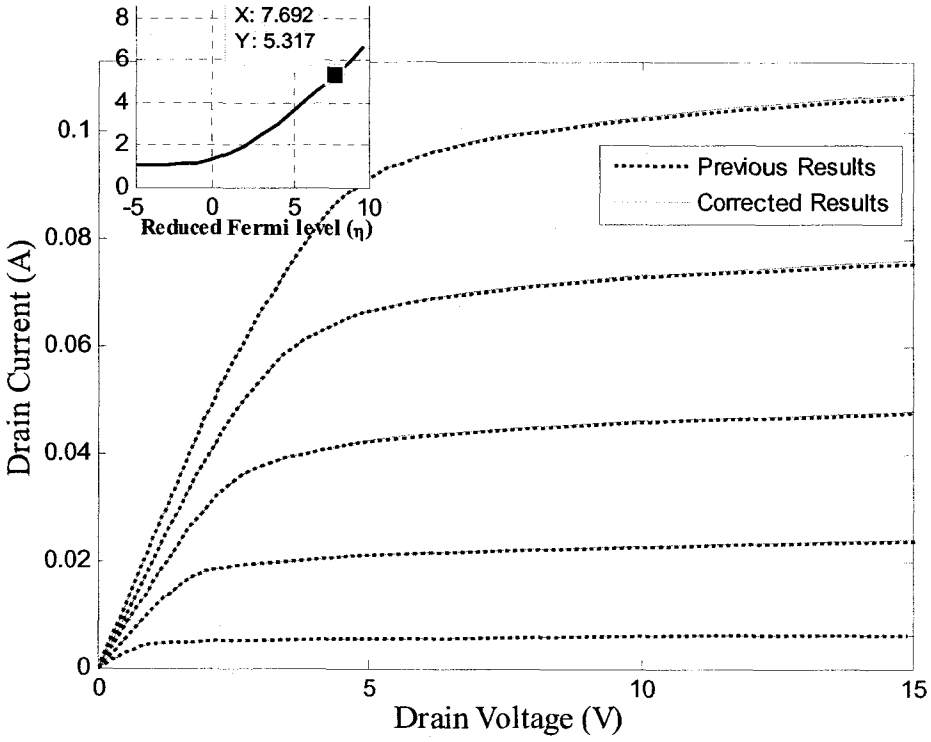

Figure 3.14: I-V characteristics based on the proposed model with and without applying the correction factor in Einstein's relationship. Inset: Calculated values for the correction factor as a function of reduced Fermi level (η). η appears in the Fermi-Dirac integral and is defined as $\frac{E_F - E_C}{k_B T}$.

Chapter 4

Conclusion and Future Works

4.1 Conclusions

This thesis has focused on the modeling of drain current/voltage characteristics of AlGaN/GaN HFETs through incorporation of the impacts of virtual gate and transferred-electron effect. As it has been discussed earlier in the thesis, drain current collapse is an important issue in developing reliable high-power HFET devices. Understanding the physics of this non-ideal effect has been made possible through development of an accurate model. In Chapter 2, an accurate and versatile analytical model based on the concept of virtual gate formation due to the existence of acceptor-type surface states has been presented to model the current-collapse phenomenon.

It is widely accepted that surface states have noticeable effects on the microwave performance of AlGaN/GaN HFETs. These effects have been observed in the form of the modesty of microwave gain and output power of these devices in comparison to their DC

predicted values. The causes for this modesty are the restriction of the load-line due to the permanent/semi-permanent degradation of the DC I-V characteristics due to electron trapping at deep acceptor-type surface states, and also transient degradation of the dynamic load-line due to the electron trapping at shallow acceptor-type trap levels. In this work, a simple analytical model for the incorporation of the permanent/semi-permanent I/V degradations has been proposed. Development of an accurate and yet simple model for prediction of the impact of these states in postponing the saturation characteristics of drain-current has been tackled. In order to derive an accurate analytical model for predicting the current-collapse phenomenon, a model based on the incorporation of the surface-trapped charge as a short-channel secondary virtual gate is proposed. The presented model despite its simplicity in comparison to many other available models has been observed to be capable of remarkably reproducing experimental observations on the post DC-stress characteristics of AlGaN/GaN HFETs.

In Chapter 3, an analytical model with the capability of incorporating the transferred-electron effect for AlGaN/GaN HFETs is proposed. Electron bunching caused by this effect is considered through incorporation of a diffusion current term. It is shown that incorporation of the transferred-electron effect, although inconsequential in devices with large parasitic resistance, is a necessity for understanding the behaviour of AlGaN/GaN transistors of future generations. The wide and large peak of the steady-state electron drift-velocity are important features in adoption of III-Nitride HFETs to microwave applications and as result it is extremely important to validate the consequences of these features on device characteristics through modeling. In this model, the iterative solution of Poisson's equation by far reduces the burden of choosing the fitting parameters.

4.2 Future works

More works can be done in different aspects to improve the proposed models in the future. Selection of more accurate distribution profiles for charge trapping in the drain-access region and also incorporation of dynamic characteristics of electron trapping is expected to not only improve the matching between the experimental values and the simulation results but also to make the model extendable to transient dispersion analyses.

In addition, adopting a more accurate and realistic field-dependent mobility model, which is capable of entirely matching the first inflexion point in the low-field region as well as predicting the negative differential mobility region, can considerably improve the accuracy of the model. These more sophisticated models, however, will not yield to analytical solutions and should be dealt with numerically.

In addition, incorporation of gate leakage and also leakage through the buffer layer are important research endeavors to follow this work.

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