ADVANCED MODULATION TECHNIQUES FOR NEUTRAL-POINT CLAMPED THREE-LEVEL INVERTERS IN AUTOMOTIVE APPLICATIONS

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ABSTRACT

Advanced Modulation Techniques for Neutral-Point Clamped Three-Level Inverters in Automotive Applications

Nazak Soleimanpour

The Neutral-Point Clamped (NPC) three-level inverter is a promising multilevel topology in the application of Electric Vehicle (EV). However, the growing requirements by the EV initiate the thermal unbalance problem for this inverter topology. The present thesis highlights the performance of the NPC three-level inverter supplying a Permanent Magnet Synchronous Motor (PMSM) in the application of EV. The PMSM is considered to operate in the region below the base speed. In this condition, there is an unbalance of conduction power loss among the semiconductors of the inverter. The project deals with the conduction power losses of the semiconductors in a NPC three-level inverter controlled with special Space Vector Modulation (SVM) methods. In order to find an appropriate method for balancing the conduction power loss of devices, three SVM methods, "*Normal*", "*O2*" and "*O3*" are compared. By implementing these three techniques, primarily, the "conduction duty cycle" of the devices is calculated to demonstrate the duration of conducting for each device. Afterwards, the conduction power loss of devices is computed in *MATLAB/Simulink*. In addition, the impact of two parameters, modulation index and power factor, on conduction duty cycle and conduction power loss is investigated. Furthermore, Comparison of the total harmonic distortion of the line-to-line current for different modulation indices is presented for all three modulation techniques. According to the detailed comparisons of methods, O2 Space Vector Modulation technique stands out as a better candidate for thermal redistribution among semiconductors.

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Dedicated to My Beloved Parents,

Mahmood & Fariba

& My lovely brother,

Mohammad Ali

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LIST OF SYMBOLS

R_{th}	Thermal resistance
ΔT	Temperature difference
P_{loss}	Power loss
$Z_{(j\text{-}c)}$	thermal impedance from junction to case
$Z_{(c\text{-}h)}$	thermal impedance from case to heat-sink
$T_{jIGBT\ /\ Diode}$	junction temperature
$P_{IGBT\ /\ Diode}$	total loss in a device (switch and diode)
T_H	heat sink temperature
$R_{th(j-c)}$	thermal resistance of the device from the junction to the case
$R_{th(c-h)}$	thermal resistance from the case to the heat sink
R_d	d-axis resistance
R_q	q-axis resistance
i_d	d-axis current
i_q	q-axis current
$\omega_r\lambda_q$	Induced *EMF*
$\omega_r\lambda_d$	Induced *EMF*
λ_d	flux linkage in d-axis stators
λ_q	flux linkage in q-axis stators
L_d	d-axis inductance
L_q	q-axis inductance

λ_m	permanent magnet flux linkage
p	number of poles
T_e	Field torque
K_t	Torque constant
T_l	Load torque
B	viscous friction
J	moment of inertia
ω_m	mechanical speed
ω_r	electrical speed
V_T	terminal voltage
R	resistance of the PMSM
X_L	inductive reactance of the PMSM
$I_{phase}^{continuous}$	Maximum q-axis current
φ	Load angle
m	Modulation index
V_{dc}	DC source voltage
P_{cond}	average conduction power loss
P_{sw}	average switching power loss
E_{ON}	Switching energy (on state)
E_{OFF}	Switching energy (off state)
$T_j(IGBT)$	junction temperature of switch
$T_j(Diode)$	junction temperature of diode

V_A, V_B, V_C	Three phase desired output voltages
V_α , V_β	Voltages after Clarke transformation
θ	angle of the reference voltage vector
T_S	Sampling time
T_a, T_b , T_0	corresponding durations of the vectors
d_a, d_b , d_0	corresponding duty cycle of the vectors
$P_{cond}(t)$	instantaneous conduction power loss
$v_{ce}(t)$	voltage over the device
$i(t)$	current flowing through the device
$v_{ce\,0}$	DC voltage source in approximate model of semiconductor
r_c	Resistance in approximate model of semiconductor
I_{c-avg}	Average current of semiconductor
I_{c-rms}	RMS value of semiconductor current

CHAPTER1: INTRODUCTION TO THESIS

The present thesis deals with the performance of Neutral-Point Clamped three-level inverter for the application in Permanent Magnet Synchronous Motor drive. As the motor speed increases, the unbalance thermal losses appear among the semiconductors of the inverter. Due to this thermal unbalance in the inverter, the safe power handling capacity of the inverter will be restricted. In order to improve the inverter operation, in the present thesis, a set of Space Vector Modulation techniques is presented. The thesis comprises of 5 chapters. At the end of this chapter, a brief description of all chapters is presented.

1.1. INTRODUCTION TO PERMANENT MAGNET SYNCHRONOUS MOTOR

The development of Permanent Magnet Synchronous Motors (PMSM) makes them more attractive in electric vehicle applications. The PMSM offers the features as the following [1-2]:

- High efficiency, high power density, high power factor, high starting torque and high cruising speed,
- Small size, light weight, small moment of inertia, useful for limited-space electric vehicles,
- It is also suitable for the acceleration of starting due to its large output torque at low speed.

The PMSM is supplied by the converter which has a DC source. The improvement in controlling the semiconductors of the converter has also allowed the converter to generate the waveforms with higher quality.

The diagram of a PMSM and the converter is shown in the Figure 1.1 [3-4]:

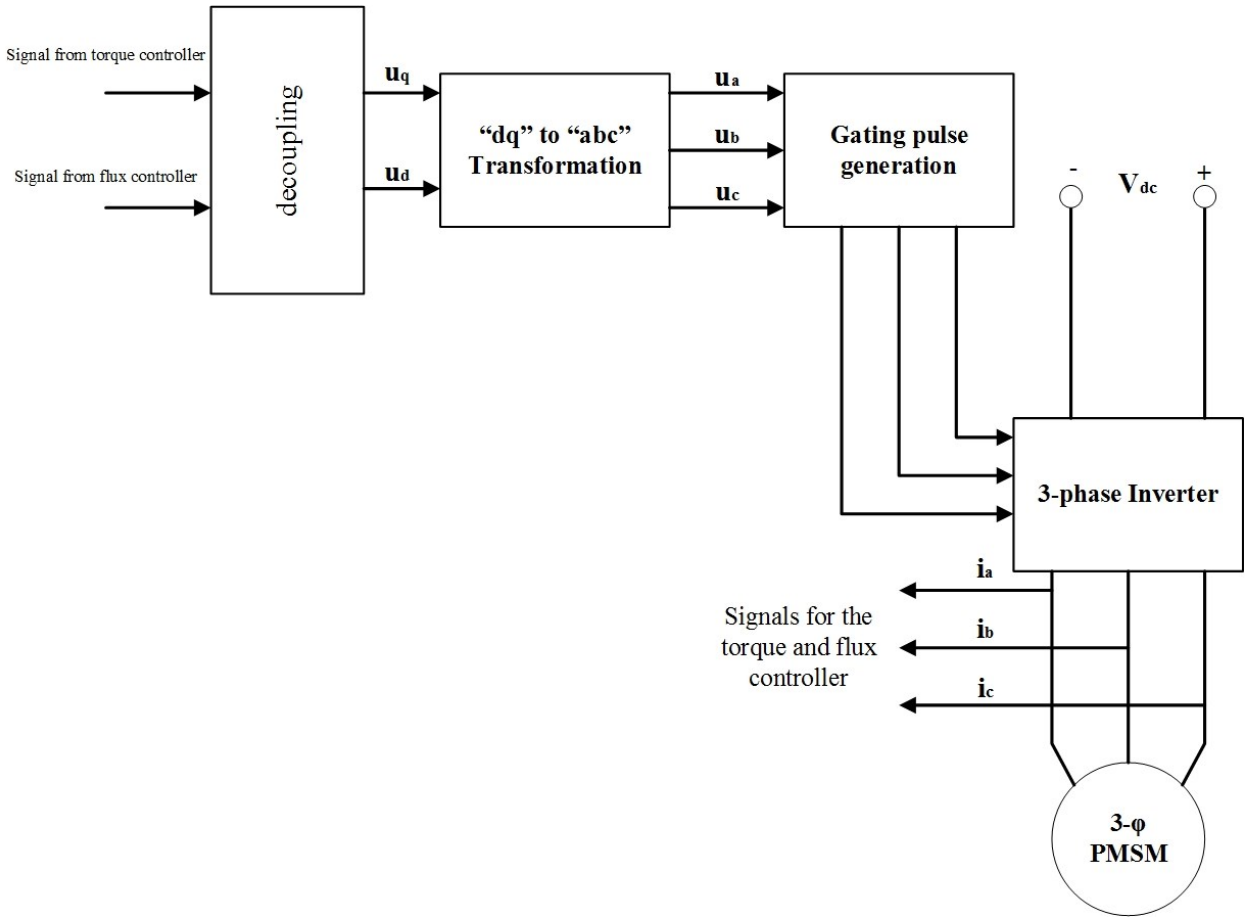


Figure 1. 1: Diagram of converter and PMSM

Considering Figure 1.1, in the present project, the "gating pulse generation" and three-phase inverter is studied.

By applying three controllers, speed and torque are controlled. These controllers are speed controller, torque controller and flux controller. The control strategy accentuates the control of speed and current in "d" and "q" axes.

Considering the speed range of the motor, there are two operating regions for the PMSM; the first region is the Normal range of operation. In this region, the torque is constant at its maximum value and the speed is below the rated value.

The other region is the Field-Weakening region. In this region, the speed is beyond the rated value and the power remains constant. The plot of these regions for the selected PMSM in this study is illustrated in Figure1.2.

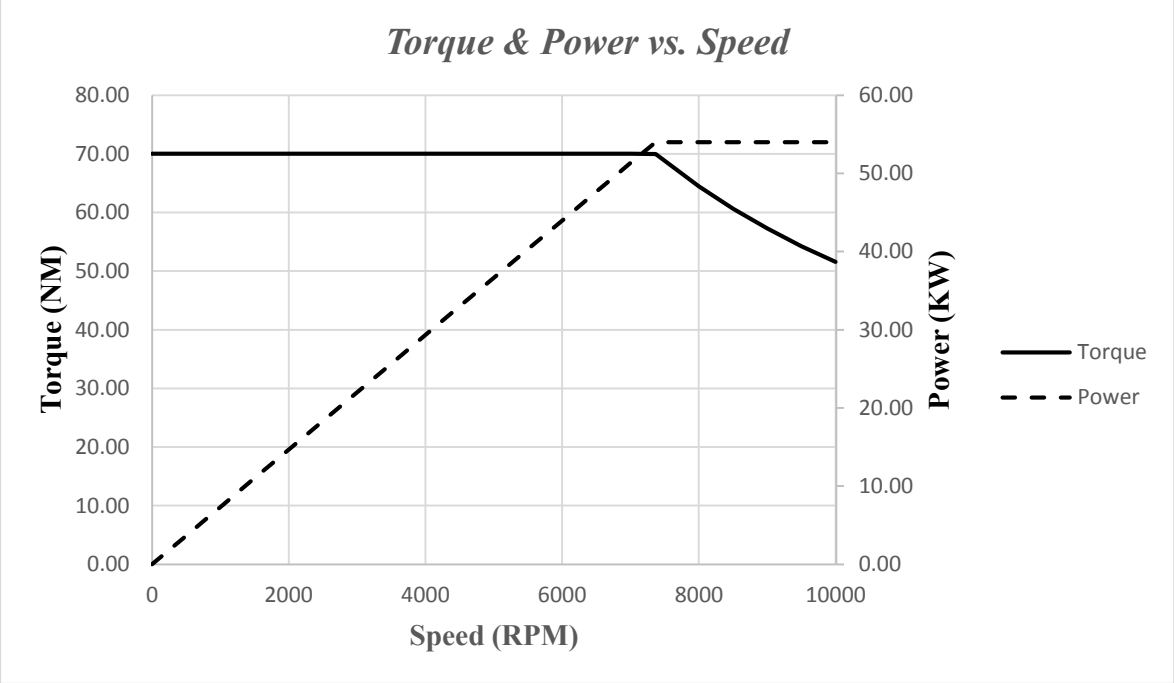


Figure 1. 2: Torque and power vs. speed, PMSM

1.2. INTRODUCTION TO POWER CONVERTERS FOR ELECTRIC VEHICLES

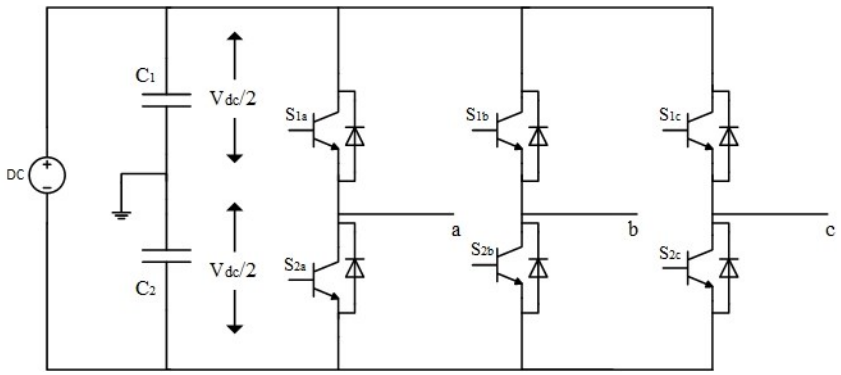
In electric vehicles, it is essential to increase the driving distance. However, the driving distance is limited by the losses in the devices. Therefore, in order to reduce the size of the cooling system for the devices in the converter, the losses should be decreased.

Nowadays, controlled AC Drives are used in the application areas of medium voltage (MV) and high power. Since it is hard to connect a single power semiconductor to the MV network, a series of multi-level converters have got attention in the application of medium voltage and high power. There are two types of inverters; Voltage Source Inverter (VSI) and Current Source Inverter (CSI). In the present study, the VSI has been selected for the application of PMSM drive, because the electric vehicle will be powered by a battery pack. A VSI is applicable to convert a DC voltage to three phase AC voltage.

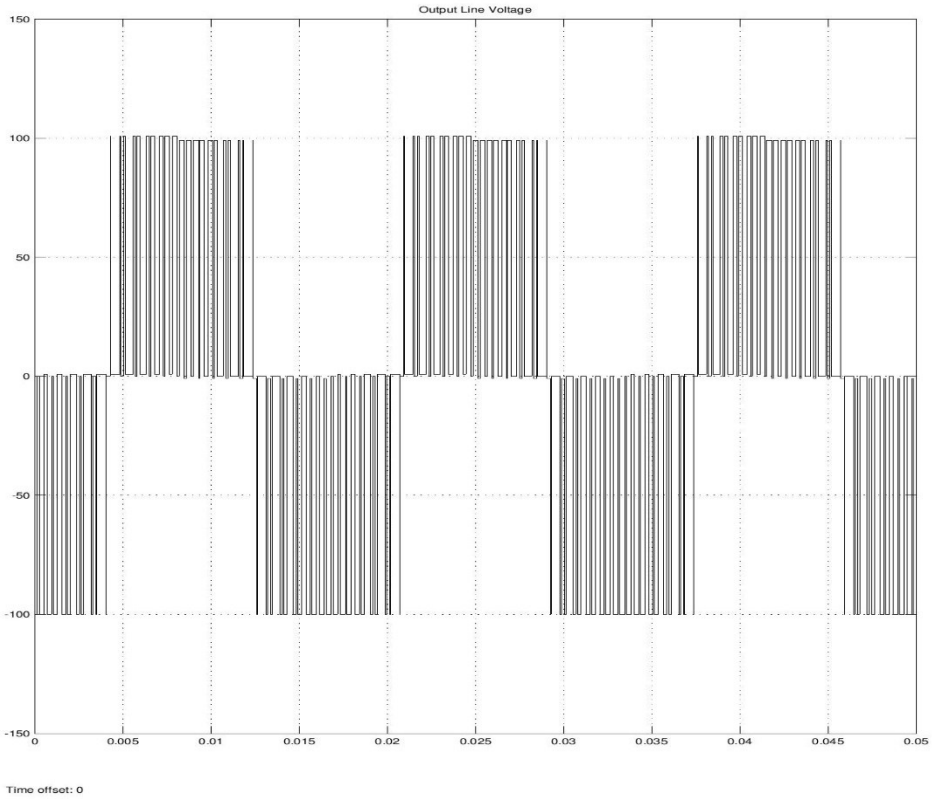
Typically the converters used in EVs are 3-phase 2-level inverters with Pulse-Width Modulation (PWM). However, the inverters that are controlled by PWM, lead to additional switching losses. So they need greater cooling components [5-6].

The main reason for the appearance of the multilevel inverters instead of 2-level inverters is the high value of DC voltage in the source. Therefore, for higher voltage ratings, there is no need to use switches with high voltage ratings. Therefore, it is possible to connect in series the switches with low voltage ratings. Unlike the simple connection of switches in series, multi-level converters naturally limit the voltage stress on the switches to safe values.

The diagram of a two-level inverter and the voltage waveform is shown in Figure 1.3:



(a)



(b)

Figure 1. 3: (a) Two-Level inverter diagram, (b) output line voltage

According to Figure 1.3, the voltage is comprising a fundamental frequency component and several harmonic components. These harmonics cause the losses in switches and lower power quality in the output. In addition, in a two-level inverter, each switch tolerates the voltage value of $+V_{dc}/2$ considering that the DC source is V_{dc}.

A multilevel converter divides the DC source value directly or indirectly, so that the output of each leg can be more than two steps (levels). In addition, the quality of the output waveform gets improved with lower distortion due to the use of both amplitude modulation and pulse width modulation. Multilevel converters are being used in high and medium power applications due to their advantages such as low harmonic contents and low electromagnetic interference (EMI) outputs. Moreover, the switching technique selected to control the converter will have an effective role in harmonic elimination even in two level inverters. The switching technique and the topology of the converter is selected according to power demands of the converters.

Multi-Level converters comprise a series of power semiconductors in each leg and capacitors as voltage sources. Due to this configuration, the power semiconductors withstand the reduced voltages while in the output, there is a high level voltage. This can be done by means of clamping diodes in NPC inverters or by flying capacitors in other configuration of multilevel inverter.

The more increasing the number of levels, the more steps will appear in the output voltage, so the multi-level converter generates a staircase waveform, with lower harmonic distortion.

The number of levels of the multilevel inverter is indeed, the number of steps of phase voltage with respect to the negative terminal of the converter [7]. So, a three-level inverter generates the output voltage with three-levels. In addition, the number of levels of the output line voltage (voltage between two phases), denoted as "*K*" is calculated as the following:

$$K = 2M - 1 \tag{1.1}$$

where M is the number of levels in the multi-level inverter. For example, for a three-level inverter, there are 2×3-1=5 steps in the output line voltage.

Multi-level inverters offer several advantages as the following [7-8];

a) Applicable in networks with high power and medium (high) voltage with low harmonic distortion in the output voltage and current
b) Low common mode voltage, so the stress in the motor bearings is reduced
c) Low voltage stress on power semiconductors
d) High efficiency for fundamental frequency switching
e) The output voltages have lower distortion than a conventional two level inverter
f) They draw input current with very low distortion

There are a number of topologies of multilevel converters that have been proposed since 1975. The most popular multi-level inverter topologies are Flying Capacitor (Clamping Capacitors) [9], Neutral-Point Clamped (NPC) [10] and Cascaded H-Bridge [11]. In this study, the three-level NPC has been selected.

The three-level inverter consists of 12 switches which are divided into three phases. If the DC source has the voltage value of V_{dc}, each switch has to be rated at $+V_{dc}/2$. In the present study, the Neutral-Point Clamped (NPC) three-level inverter has been selected in the application of PMSM drive. In addition, the choice of the switches is IGBT because they are the most common switches for the power range under consideration (600V and 75 kW). The configuration of a three-level NPC VSI and the voltage waveforms are illustrated in Figures 1.4 and 1.5.

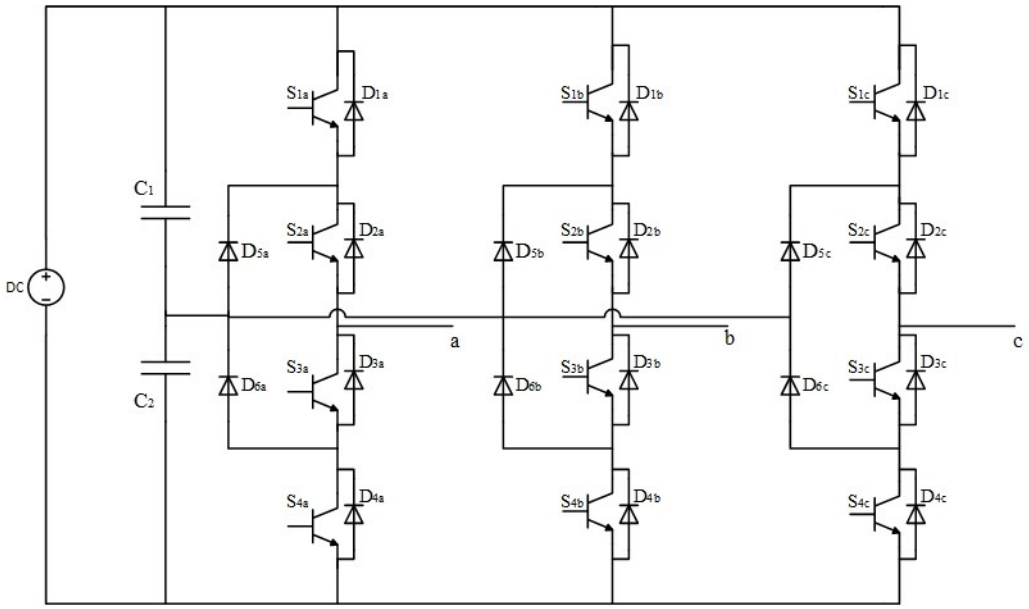


Figure 1. 4: NPC Three-Level inverter

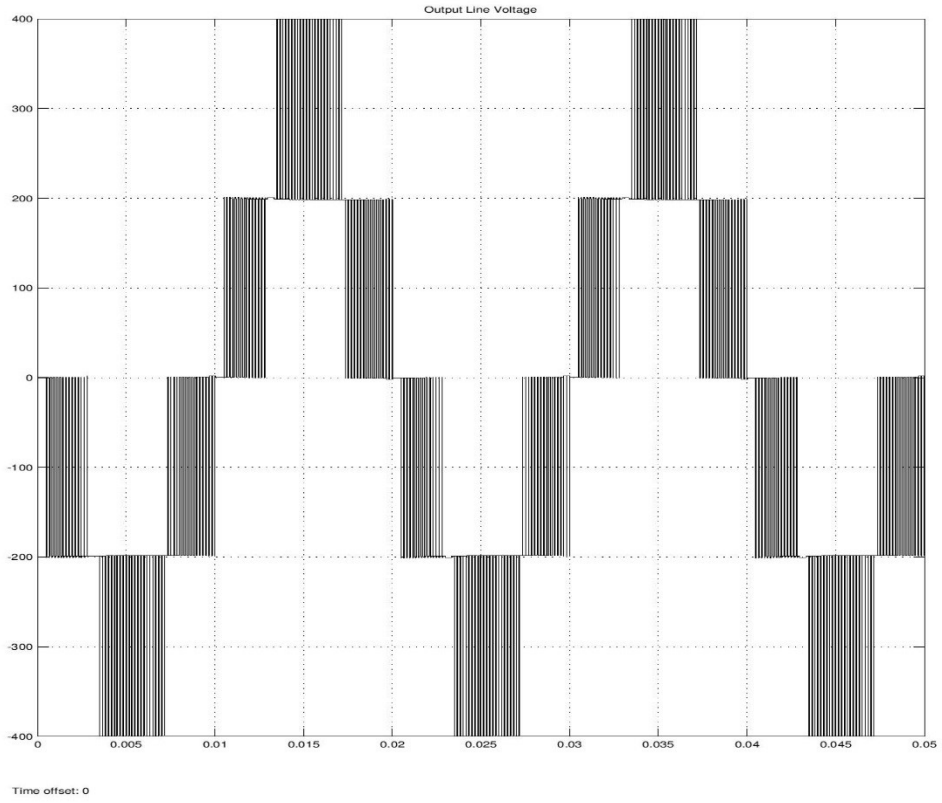


Figure 1. 5: Line voltage of Three-Level inverter with PWM

By comparing Figure 1.3 (b) and Figure 1.5, it can be seen that in a three-level inverter, the voltage has more steps, so it is more similar to a sinusoidal waveform than the output voltage of a two-level inverter.

1.3. GATING SIGNAL GENERATION

There are different modulation techniques to control the switches of multi-level inverters [7]:

a) Sinusoidal Pulse Width Modulation (*SPWM*)

b) Space Vector Modulation (*SVM*)

The basic principle of PWM technique is the comparison of two waveforms: a reference waveform at low frequency (f_r) and a triangle or saw-tooth carrier at high frequency (f_s). If the magnitude of the reference waveform is greater than the magnitude of the carrier waveform, then the switch gets on; otherwise it remains in its off state.

The Sinusoidal Pulse Width Modulation (SPWM), is a kind of PWM technique to control the switching of a converter. The SPWM technique is a popular modulation method in the applications regarding harmonic reduction. In SPWM, to generate the gate signals for the switches of the inverter, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform. The SPWM modulation method is depicted in Figure 1.6.

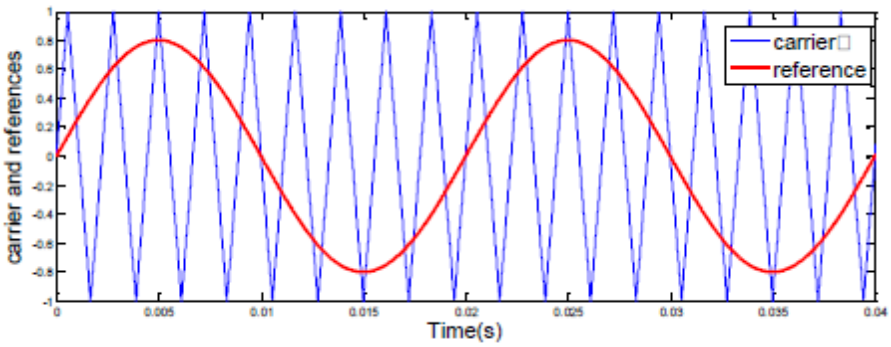


Figure 1. 6: The SPWM modulation method

The sinusoidal reference waveform is compared to a triangular carrier waveform. Therefore, the gating signal is generated for a particular complementary pair of switches in the inverter. Since SPWM separately controls the phases, for a three phase converter, three SPWM controllers are needed. In these three SPWM controllers, the reference waveforms should be 120^o apart from each other.

In Space Vector Modulation (SVM) method, the switching states are determined by the position of the reference voltage vector and the corresponding vector times. In SVM method, the inverter can be controlled by means of switching states. Hence, each switching state is related to a set of three phase voltage. The desired output phase voltages of the inverter are synthesized. The task of the modulator is to decide about two concepts: the switching state the switches should have and then, the duty cycle of the switches for synthesizing the reference voltage vector. The number of switching states in an n-level converter is n^3. The details of the modulation scheme are presented in Chapter 3. The Space Vector diagram for a three-level inverter is illustrated in Figure 1.7.

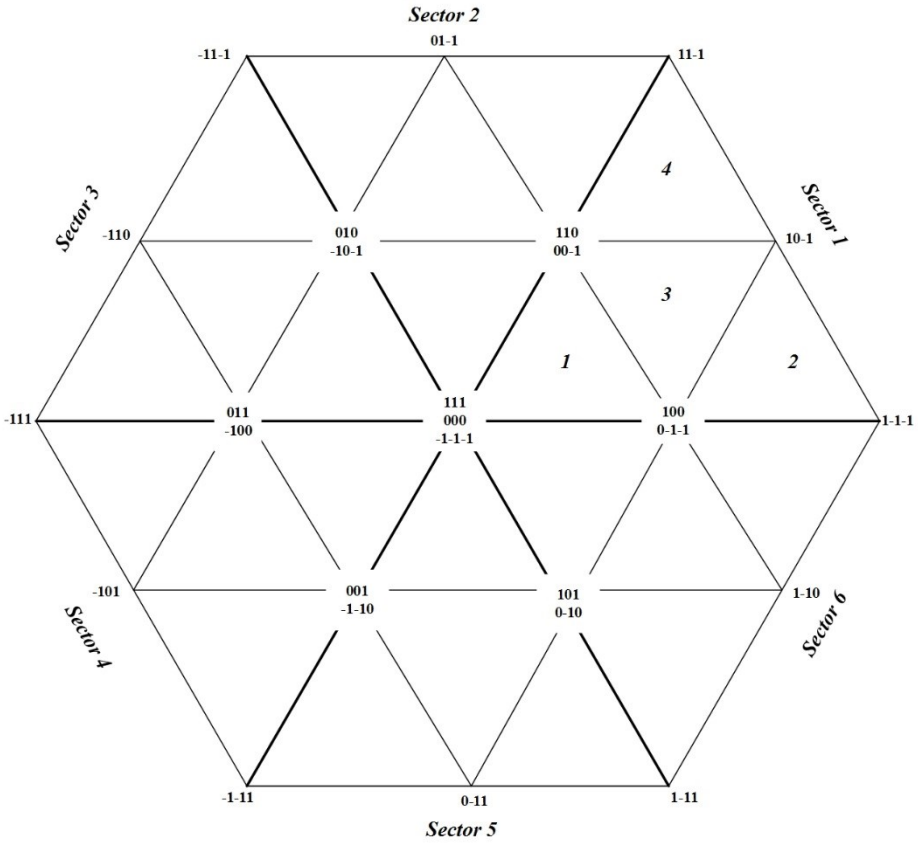


Figure 1. 7: The Space Vector Modulation diagram

According to Figure 1.7, the switching states are ~~a~~ three-bit numbers that will be discussed completely in Chapter 3.

1.4. POWER LOSSES IN THREE-LEVEL INVERTER

Each power device has some features such as limited temperatures. While the inverter is operating, the temperature of the device can be evaluated by calculating the losses. Semiconductor power losses are divided into three groups: Conduction losses (P_{cond}), Switching losses (P_{sw}) and Blocking (Leakage) losses (P_b) [12].

The Blocking losses are normally neglected, so the power losses are comprising the conduction and the switching losses. In the present study, a novel modulation strategy has been proposed by virtue of which the conduction loss of devices has been redistributed. Therefore, the life cycle of devices will be increased and the safe operation region of inverter will be extended.

In order to compute the junction temperature of a switch, that switch is mounted on a multi-layer structure. These layers have different temperatures, therefore there will be an energy flow from the layer with higher temperature toward the layer with lower temperature. Thermal resistance defines the temperature difference between two successive layers for a unit power loss:

$$R_{th} = \frac{\Delta T}{P_{loss}} \tag{1.2}$$

There is a loss model presented in [13] to evaluate the losses of power semiconductor devices. The thermal model of a switch with anti-parallel diode and a clamping diode has been shown in Figure 1.8.

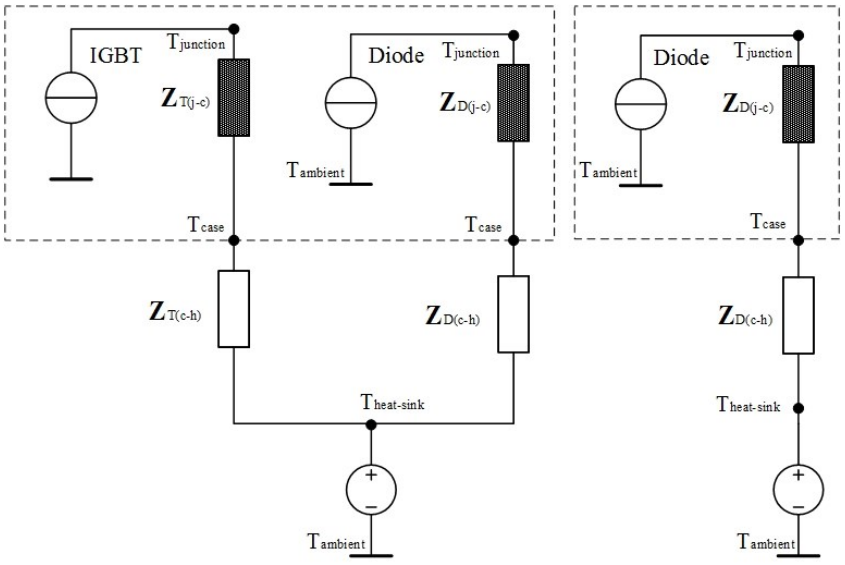


Figure 1. 8: Thermal model of switch, its anti-parallel diode and clamping diode

In this model, $Z_{(j-c)}$ is the thermal impedance from junction to case and $Z_{(c-h)}$ is the thermal impedance from case to heat-sink.

There is a formula from which the steady state mean junction temperature of each device can be evaluated [14-15]:

$$T_{jIGBT\ /\ Diode} = T_H + P_{IGBT\ /\ Diode} .(R_{th(j-c)} + R_{th(c-h)}) \tag{1.3}$$

where $T_{jIGBT\ /\ Diode}$ is the junction temperature, $P_{IGBT\ /\ Diode}$ is the total loss in a device (switch and diode), T_H is the heat sink temperature, $R_{th(j-c)}$ is the thermal resistance of the device from the junction to the case and $R_{th(c-h)}$ is the thermal resistance from the case to the heat sink. The junction temperature of each device of a three-level NPC inverter leg versus motor speed, for an inverter operating with

SPWM has been illustrated in Figure 1.9. There one can observe the unbalance in the junction temperatures.

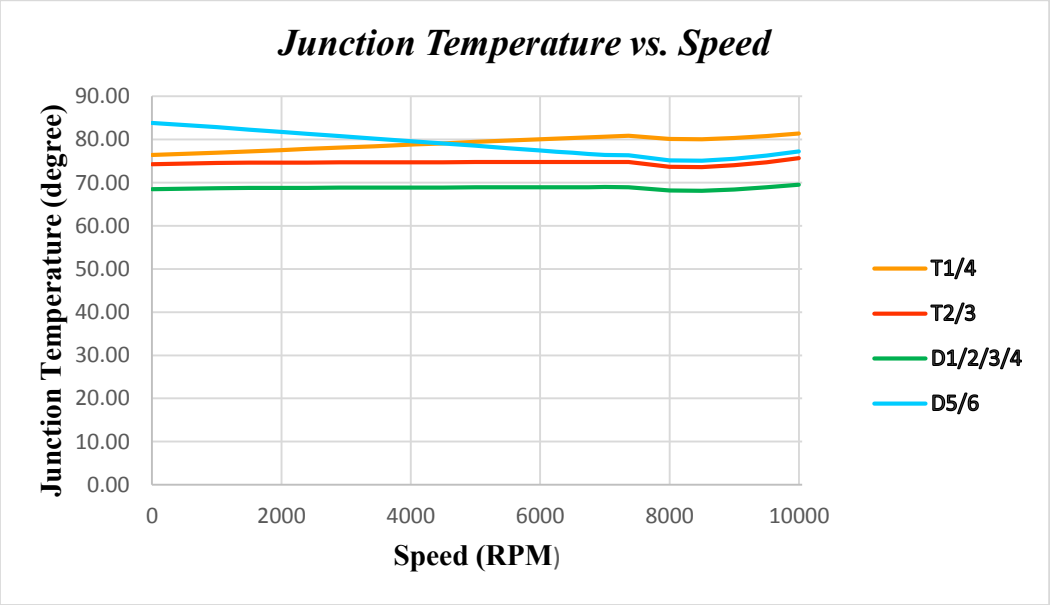


Figure 1. 9: Junction temperature of each device versus speed

1.5. CONTRIBUTION OF THE THESIS

In this project, a NPC three-level inverter is considered in the application of PMSM drive in electric vehicles. The main concern is regarding the thermal losses of the semiconductors in the inverter. Therefore, a series of modulation techniques are investigated for a three phase NPC three-level inverter. These methods are the modified Space Vector Modulation strategies by virtue of which the conduction power loss of devices has been redistributed. The conduction loss has been transferred from the switches with higher loss to those with lower losses. Therefore, the critical switches will tolerate less stress and operate for longer term.

In addition, an index “conduction duty cycle” is introduced in the thesis in order to anticipate the efficiency of the presented methods for balancing the conduction power losses of devices. This is verified by a conventional simulation.

1.6. THESIS OUTLINE

The first chapter has been allocated to introduce the PMSM features for electric vehicles. Then, a brief comparison of two-level and multilevel inverters and their common topologies has been presented. There exist the switching strategies for inverters that have been explained briefly. Moreover, basic principles of thermal model for devices and related equations have been reviewed.

In chapter 2, a model of PMSM in rotor reference frame is presented. According to the PMSM’s plot, the operation range of the PMSM has been determined. In that region, the inverter operation has been evaluated by means of the voltage and motor current. Then, the losses of the devices have been calculated for a three-level inverter with SPWM method.

In chapter 3, the principle of the SVM methods (the conventional and the new ones) is explained. Accordingly, the conduction duty cycle of devices in NPC three-level inverter has been calculated by applying SVM methods.

Chapter 4 has been dedicated to evaluate the impact of two parameters individually on conduction duty cycle of devices in the NPC three-level inverter. These parameters are load angle and modulation index that are explained precisely in Chapter 3. In addition, to determine the proper values for these parameters, the operation region of the PMSM is considered.

In Chapter 5, the conduction power losses of the devices in the NPC three-level inverter are calculated. In this chapter also, the impact of those two parameters on conduction power loss is

investigated individually. In addition, the THD of output current of the inverter is calculated to evaluate the effect the new methods on the current harmonic.

In chapter 6, according to the results presented in chapter 4 and chapter5, some conclusions are obtained. In addition, a few future works are proposed that demands further researches.

CHAPTER 2: MODEL OF THE PERMANENT MAGNET SYNCHRONOUS MOTOR

2.1. INTRODUCTION

In this chapter, the PMSM model in rotor reference frame, the phasor diagram and the single phase equivalent circuit for the PMSM are presented. Furthermore, the rms values of the output voltage and current of the inverter are identified by means of which the PMSM is supplied. The normal range of the PMSM has been considered according to the torque-speed plot. These will be used in the following chapters to calculate the required operating conditions for the power converter.

2.2. THE PMSM IN ROTOR REFERENCE FRAME

The PMSM is an AC synchronous motor. The rotor structure contains permanent magnets without any windings and it provides the constant field excitation. The PMSM is classified into two types depending on the position of the magnets in the rotor: the Surface Mounted (round rotor) PM (SPMSM) and the Interior Mounted PM (IPMSM). In this study, the Surface Mounted Permanent Magnet Motor has been considered. Most of the control methods are based on the PMSM model in the rotor reference frame. Accordingly, this model is presented in the following.

With the help of Clarke transformation, the balanced three phase quantities can be transformed into balanced two phase quadrature quantities to obtain a simpler model for analysis.

By applying the Park transformation, the balanced two phase orthogonal stationary system can be transformed into two phase orthogonal rotating reference frame. Thus, the three phase stationary

"*abc*" frame is transformed into a two phase synchronously rotating "*dq*" frame, where the voltages and currents of the PMSM can be represented by dc quantities, as opposed to ac in the other references frames. The model of PMSM in "*dq*" frame or the rotor reference frame has been shown in Figure 2.1 [16].

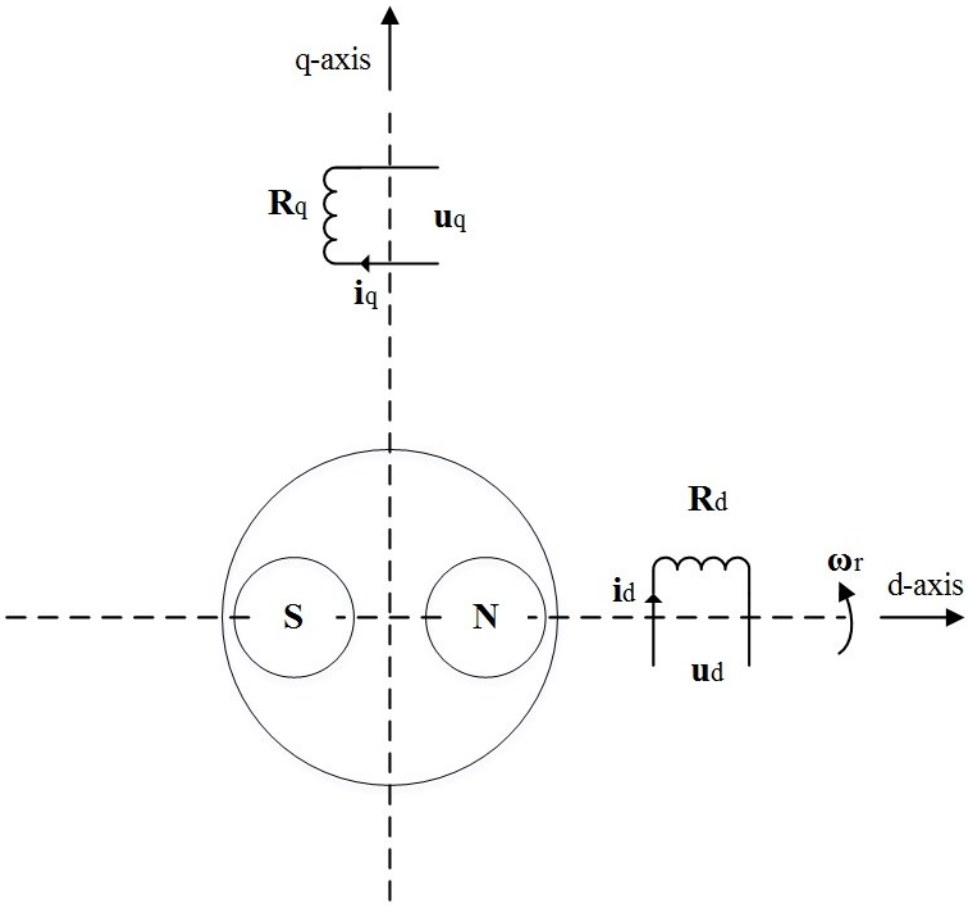


Figure 2. 1: PMSM model in "*dq*" frame

According to Figure 2.1, the induced voltages in d-axis and q-axis windings can be calculated as the following:

$$u_d = R_d i_d + \frac{d\lambda_d}{dt} - \omega_r \lambda_q \tag{2.1}$$

$$u_q = R_q i_q + \frac{d\lambda_q}{dt} + \omega_r \lambda_d \tag{2.2}$$

where "R_d" and "R_q" are d-axis and q-axis resistances and "i_d" and "i_q" are d-axis and q-axis currents. The rotationally induced *EMF* in the stator is due to the rotation of "*dq*" reference frame at synchronous speed, "ω_r". These *EMFs* are denoted as "$\omega_r\lambda_q$" and "$\omega_r\lambda_d$". The terms "λ_d" and "λ_q" are the flux linkages in d-axis and q-axis stators and defined as the following:

$$\lambda_d = L_d i_d + \lambda_m \tag{2.3}$$

$$\lambda_q = L_q i_q \tag{2.4}$$

In a SPMSM, the d-axis and q-axis inductances are equal:

$$L_d = L_q \tag{2.5}$$

The torque equation in a SPMSM is defined by [9]:

$$T_e = \frac{3}{2}\frac{p}{2}\lambda_m i_q \tag{2.6}$$

This torque is essentially the field torque due to the permanent magnet flux linkage, "λ_m" and the torque-producing component, "I_q". In SPMSM, the number of poles "p", and the permanent magnet flux linkage "λ_m" are constant. Therefore, these parameters can be replaced by a constant, "K_t" and the torque can be re-written as:

$$T_e = K_t i_q \tag{2.7}$$

$$K_t = \frac{3}{2}\frac{p}{2}\lambda_m \tag{2.8}$$

The electro-magnetic torque of a motor should be balanced by the load torque "T_l", the viscous friction "B" and the moment of inertia "J" of the motor. So, the electro-magnetic torque is as the following:

$$T_e = T_l + B\omega_m + J\frac{d\omega_m}{dt} \tag{2.9}$$

where "ω_m" is the mechanical speed and it can be defined by means of the electrical speed, "ω_r" and the number of poles, "p":

$$\omega_r = \frac{p}{2}\omega_m \tag{2.10}$$

2.3. SINGLE PHASE EQUIVALENT CIRCUIT OF PMSM

The single phase diagram of a PMSM is illustrated in Figure 2.2 [17]:

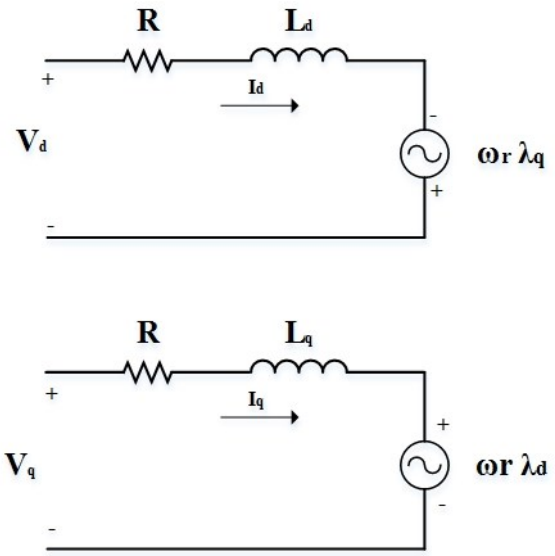


Figure 2. 2: Single phase diagram of a PMSM

The stator current in the PMSM is comprising two components: the flux producing component "I_d" and the torque producing current "I_q". The load angle (power factor angle) is the angle between stator phase current and terminal voltage. Moreover, the torque angle is the angle between the stator phase current and flux vector.

In a PMSM drive, there is a constraint for the voltage; that is the voltage increases with speed but it cannot exceed the nominal value. Therefore, the flux component (or the back *EMF*) must be reduced to allow the nominal voltage to be maintained while the speed is increasing [18]. In order to solve this limitation, it is valuable to introduce the Field-Weakening technique in PMSM. Accordingly, the PMSM has two different phasor diagrams for operating conditions; without Field-Weakening in which the speed is below the base value and with Field-Weakening that is the

speed is beyond the base value. In the present study, the motor has been analyzed for the region below the rated speed. Thus, there is no need to apply the Field-Weakening technique.

The phasor diagram of a PMSM has been illustrated in Figure 2.3 [19]:

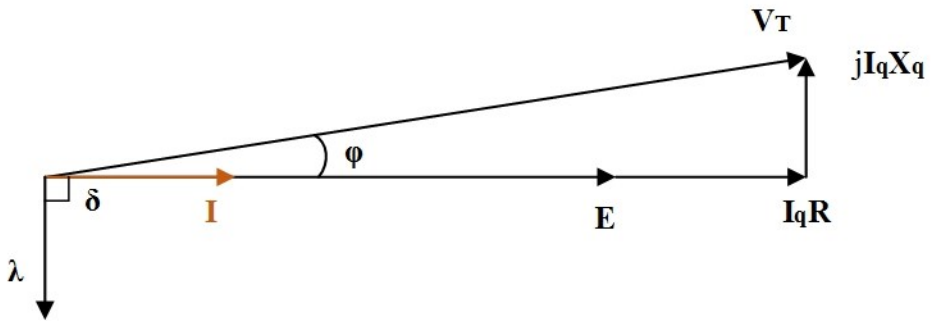


Figure 2. 3: Phasor diagram of a PMSM without field-weakening

According to the phasor diagram, the terminal voltage (V_T) is given by:

$$V_T^2 = (E + RI_q)^2 + (X_q I_q)^2 \tag{2.11}$$

$$V_T^2 = \sqrt{(E + RI_q)^2 + (X_q I_q)^2} \tag{2.12}$$

In the region without Field-Weakening, $\delta = \pi/2$. The speed is defined as below:

$$N = \frac{120\ f}{p} \tag{2.13}$$

where "*p*" is the number of poles and "*f*" is the stator electrical frequency and "*N*" is the electrical speed in "RPM". According to (2.13), the fundamental frequency of output voltage and current of the inverter can be obtained via (2.14):

$$f = \frac{p\ N}{120} \tag{2.14}$$

The power and torque are related by means of the speed as below:

$$P_m = \omega_m . T \tag{2.15}$$

where "ω_m" is the mechanical speed of machine in "rad/sec". Below the base speed, the maximum torque is the rated torque and the maximum power is increasing with speed increment.

In this study, the following parameters are considering for the PMSM, Table 2.1:

Table 2. 1: Rating of the selected PMSM

Parameter	***Value***
R	54 mΩ
L	278 μH
$P_{continuous}$	54 KW
I_{peak}	116 A
J	0.05 kgm^2
B	0.0003035Nm.sec
No. of poles (*p*)	10
Base speed	7367 RPM

Furthermore, the "*Torque-Speed*" plot of the selected PMSM is also shown in Figure 2.4. In this figure, the power versus speed is also illustrated.

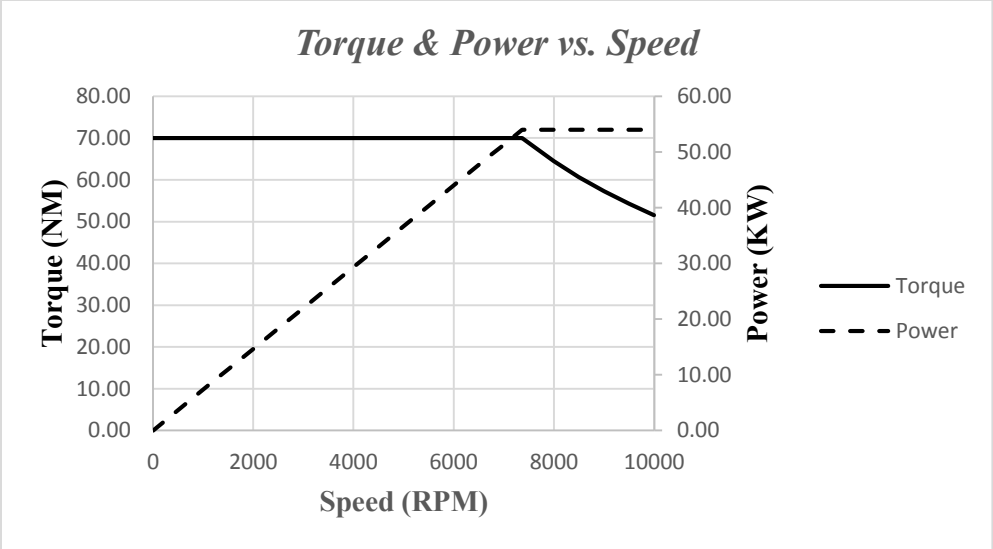


Figure 2. 4: Torque and power vs. speed for the PMSM

2.4. INVERTER VOLTAGE AND ROTOR CURRENT

A three phase Voltage Source Inverter (VSI) has the responsibility to switch the DC-link voltage in the input and generate a sinusoidal fundamental component of voltage to a three phase motor at the output of the inverter. The speed of the motor is controlled by the magnitude and frequency of the sinusoidal output voltage [20]. In this study, a three phase three-level NPC inverter is considered and a PMSM is connected to the output of the inverter.

2.4.1. NEUTRAL-POINT CLAMPED MULTILEVEL INVERTER

The NPC inverter has an important role in the wind turbines and electric vehicle industries. The multi-level NPC inverter offers advantages such as common DC bus for three phases to minimize the number of capacitors, high efficiency in the application of fundamental frequency switching and the ability of pre-charging the DC link capacitors as a group.

The topology of a three-level NPC inverter is shown in Figure 2.5 [7-8]:

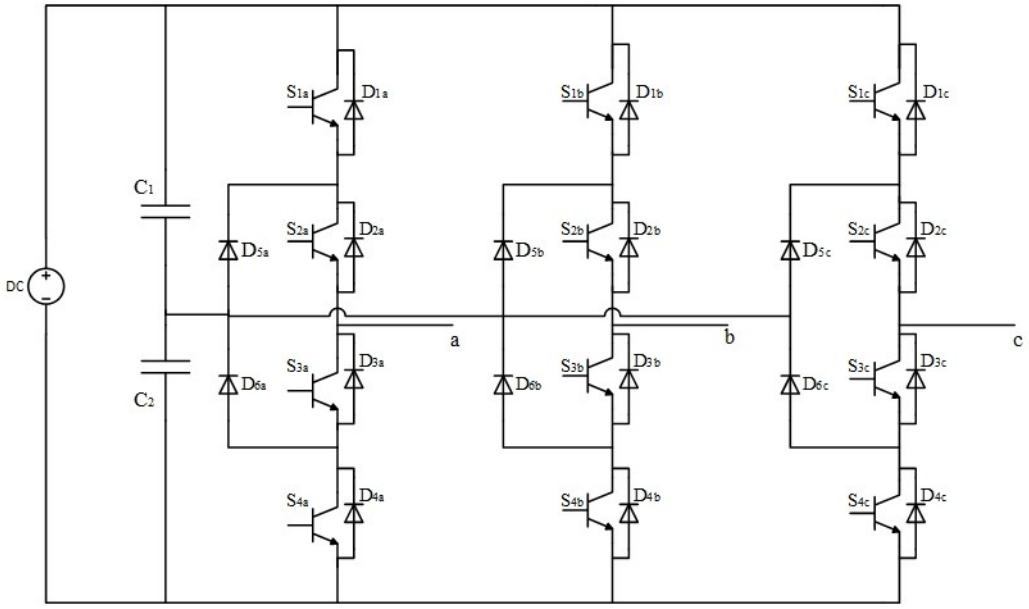


Figure 2. 5: Three-level Neutral-Point Clamped inverter

In the three-level NPC inverter, the three phases of the inverter have a common DC bus and the DC bus voltage is divided into three-levels by means of two series-connected capacitors, C_1 and C_2. These three-levels are $+V_{dc}/2$, 0 and $-V_{dc}/2$. In each leg, there are two pairs of complementary switches (S_1 and S_3) and (S_2 and S_4) and two clamping diodes (D_5 and D_6). The outer switches (S_1 and S_4) are mainly operating for pulse width modulation and the inner switches (S_2 and S_3) are clamping the output terminal to the neutral point, "*n*". Moreover, the two clamping diodes are for clamping the switch voltage to half level of the DC bus voltage, $+V_{dc}/2$.

According to Figure 2.6, the output voltages can be classified into two groups; the AC voltage denoted as v_{an}, which is the voltage across "*a*" and the neutral point "*n*", and the DC voltage, denoted as v_{a0}, which is the voltage across "*a*" and the negative inverter terminal, "*0*". The difference between v_{an} and v_{a0} is the voltage across C_2, $V_{dc}/2$ [7].

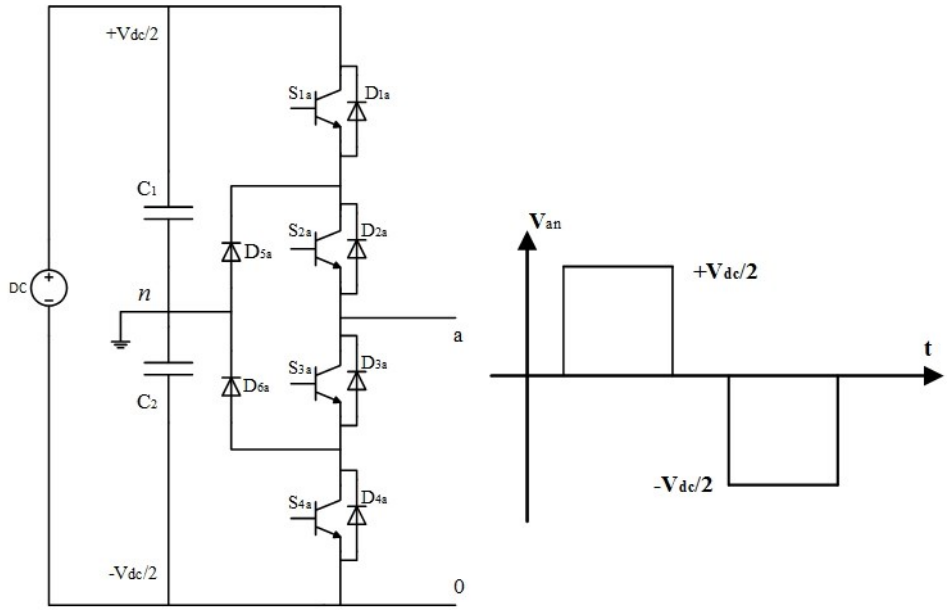


Figure 2. 6: Single Phase Neutral-Point Clamped Three-Level inverter

The neutral point, "*n*", is the middle point of the capacitors, C_1 and C_2. The output phase voltage, v_{an} has three different states: $+V_{dc}/2$, 0 and $-V_{dc}/2$. For the first level, $+V_{dc}/2$, the two upper switches, S_1 and S_2, need to be turned on. For the zero level, two middle switches, S_2 and S_3 and for the third level, $-V_{dc}/2$ the two lower switches, S_3 and S_4 need to be turned on.

When the two upper switches, S_1 and S_2 turn on, $v_{a0} = V_{dc}$, so the lower clamping diode, D_6, balances the voltage sharing between the two lower switches, S_3 and S_4 because S_3 blocks the voltage across C_1 and S_4 blocks the voltage across C_2.

In a three-level inverter, it can be said that each active switching device is required to block a voltage level of $V_{dc}/(3-1) = V_{dc}/2$. If the voltage rating of each clamping diode is assumed to be similar to that of the active device, the number of clamping diodes needed for each phase is $(3-1)\times(3-2) = 2$ [7].

2.4.2. DATA SHEET OF PERMANENT MAGNET SYCHRONOUS MACHINE

As mentioned before, the PMSM has two regions of operation which are below and above the base speed. For the region below the base speed, the Field Weakening is not required. Therefore, the current has only the q-axis component which is the torque-producing current. In this region, the maximum torque is constant and the power is increasing depending on the speed increment as given:

$$P_m = \omega_m \times T \tag{2.16}$$

where "T" is the torque and "ω_m" is the mechanical speed of PMSM. The system frequency is also getting larger with speed increasing:

$$f = \frac{\omega_r \times p}{60} \tag{2.17}$$

where "p" is the number of the pole pairs and "ω_r" is the synchronous speed of PMSM.

The inverter voltage is calculated according to the sinusoidal back EMF and motor currents as the following:

$$V_{inv(LL)} = \sqrt{[EMF + \sqrt{6}(RI_q - X_L I_d)]^2 + [\sqrt{6}(X_L I_q + RI_d)]^2} \tag{2.18}$$

where "R" and "X_L" are the resistance and inductive reactance of the PMSM and "I_q" and "I_d" are q-axis and d-axis currents of the PMSM. In the region below the base speed, the d-axis current is zero because there is no Field-Weakening.

The q-axis current can be calculated from (2.19). Below the base speed, the q-axis current is equal to its maximum value which is the $I_{phase}^{continuous}$.

$$I_{q(rms)} = \begin{cases} I_{phase}^{continuous} & \dfrac{\sqrt{6} \times P_{continous}}{(no.of\ \ phases\ ) \times EMF} \geq I_{phase}^{continuous} \\ \dfrac{\sqrt{6} \times P_{continous}}{(no.of\ \ phases\ ) \times EMF} & otherwise \end{cases} \tag{2.19}$$

In addition, the load angle is calculated as the following:

$$\varphi = \frac{180}{\pi} \times \tanh\left(\frac{X_L I_q + R I_d}{(EMF\ /\sqrt{6}) + R I_q - X_L I_d} \right) \tag{2.20}$$

The data that have been calculated according to the previous formulas are presented in Table 2.2.

Table 2. 2: Data of PMSM current and inverter voltage ratio

Speed *(rpm)*	***Torque*** *(Nm)*	***Power*** *(KW)*	***EMF*** *(V)*	***Frequency (HZ)***	V_{inv} *(V)*	***Iq*** *(A)*	***Modulation index***	***Load Angle*** *(degree)*	***PF***
1	70	0.01	0.08	0	10.85	82.09	0.0181	-0.15	1
500	70	3.67	38.28	42	51.19	82.09	0.0853	-16.61	0.9583
750	70	5.50	57.42	63	71.64	82.09	0.1194	-17.84	0.9519
1000	70	7.33	76.56	83	92.10	82.09	0.1535	-18.53	0.9482
1250	70	9.16	95.70	104	112.58	82.09	0.1876	-18.96	0.9457
1500	70	11	114.83	125	133.06	82.09	0.2218	-19.27	0.9440
2000	70	14.66	153.11	167	174.03	82.09	0.2900	-19.66	0.9417
2520	70	18.47	192.92	210	216.64	82.09	0.3668	-19.91	0.9403
2900	70	21.26	222.01	242	247.78	82.09	0.4130	-20.03	0.9395
3437	70	25.19	263.13	286	291.79	82.09	0.4863	-20.17	0.9387
4064	70	29.79	311.13	339	343.17	82.09	0.5720	-20.28	0.9380
4500	70	32.99	344.50	375	378.91	82.09	0.6315	-20.34	0.9376
5000	70	36.65	382.78	417	419.88	82.09	0.6998	-20.40	0.9373
5500	70	40.32	421.06	458	460.86	82.09	0.7681	-20.44	0.9370
6000	70	43.98	459.34	500	501.84	82.09	0.8364	-20.48	0.9368
6250	70	45.81	478.48	521	522.33	82.09	0.8706	-20.50	0.9367
6500	70	47.65	497.62	542	542.82	82.09	0.9047	-20.52	0.9366
6750	70	49.48	516.76	563	563.31	82.09	0.9389	-20.53	0.9365
7000	70	51.31	535.90	583	580	82.09	0.9667	-20.55	0.9364
7367	70	54	563.99	614	580	82.09	0.9667	-17.19	0.9553

In Table 2.2, the modulation index has been calculated by (2.21):

$$m = \frac{Vinv}{Vdc} \tag{2.21}$$

In the present study, the DC source voltage (V_{dc}) is assumed to be 600V. The data presented in Table 2.2 are for the region below the rated speed and for the selected PMSM, the rated speed is 7367 rpm.

2.4.3. ESTIMATION OF POWER LOSSES

According to [15], to obtain the junction temperature of the devices in the inverter, the average values of conduction losses and the switching losses are required. Conduction loss is the product of the current flowing through the device and the voltage across the device during its conduction. To obtain the average conduction loss, the conducting duration of the device is also needed:

$$P_{cond} = \frac{1}{T}\int_0^{T/2} v(t)\, i(t)\, \tau(t)\, d(\omega t) \tag{2.22}$$

To calculate the average switching power loss, the switching energy and the switching frequency are required. The switching energy can be obtained from the switching energy curve versus the current that is presented in the device datasheet. The switching energy can be plotted via curve fitting as a second-degree polynomial equation of current. The expression for the average switching power loss is as the following:

$$P_{sw} = f_{sw}\, \frac{1}{T}\int_0^{T/2} (E_{ON} + E_{OFF})\, d(\omega t) \tag{2.23}$$

To determine the junction temperature of the devices, the average conduction loss and average switching loss of the devices are required. The junction temperature can be calculated as given below for the IGBT module F3L300R07PE4-INFINEON:

$$\begin{aligned} T_j(IGBT) &= 0.16\,(P_{con} + P_{sw}) + T_{case} \\ T_j(Diode) &= 0.32\,(P_{con} + P_{sw}) + T_{case} \end{aligned} \tag{2.24}$$

where "T_{case}" is dependent on the total average power losses in one leg of the inverter and the heat sink temperature as given in (2.25). The heat sink temperature is also dependent on the total

average power losses in one leg of the inverter. In addition, the liquid temperature is another term of heat sink temperature which is constant. In this study, the liquid temperature is 55^{o} C.

$$T_{case} = (0.0154 \times P_{total\ (1\,leg)}) + T_{heat\ sink}$$
$$T_{heat\ sink} = (0.035 \times P_{total\ (1\,leg)}) + T_{liquid} \quad (2.25)$$

The losses and the junction temperature of the devices in three-level inverter for various speeds in the region below the base speed are presented in Table 2.3. According to this table, by increasing the speed, the junction temperature of all devices are increasing. This statement is valid in the region below the rated speed. Among the devices, the anti-parallel diodes are the coldest devices and the clamping diodes are the hottest devices up to the speed of 4500 RPM.

Table 2. 3: Losses and junction temperature for devices in three-level inverter with SPWM

Speed	*Average Conduction Power Loss*				*Average Switching Power Loss*				*Junction Temperature*			
	S1/4	*S2/3*	*D1-4*	*D5/6*	*S1/4*	*S2/3*	*D1-4*	*D5/6*	*S1/4*	*S2/3*	*D1-4*	*D5/6*
1	0.53	36.23	0.00	33.24	49.15	0.00	0.00	14.75	76.45	74.29	68.50	83.86
500	2.40	36.23	0.00	31.52	48.13	1.03	0.31	14.75	77.66	75.53	69.67	84.38
750	3.33	36.22	0.01	30.65	47.97	1.18	0.35	14.75	78.80	76.58	70.71	85.12
1000	4.27	36.22	0.01	29.78	47.88	1.27	0.38	14.75	79.95	77.60	71.73	85.86
1250	5.20	36.22	0.02	28.92	47.82	1.33	0.40	14.75	81.10	78.62	72.75	86.59
1500	6.14	36.21	0.02	28.05	47.78	1.38	0.41	14.75	82.25	79.64	73.76	87.32
2000	8.01	36.21	0.03	26.31	47.72	1.43	0.43	14.75	83.56	80.67	74.79	87.78
2520	9.96	36.20	0.03	24.51	47.68	1.47	0.44	14.75	84.81	81.68	75.81	88.35
2900	11.39	36.19	0.04	23.19	47.67	1.49	0.45	14.75	85.88	82.69	76.81	89.22
3437	13.40	36.18	0.05	21.32	47.65	1.51	0.45	14.75	87.12	83.70	77.83	89.81
4064	15.75	36.18	0.06	19.15	47.63	1.52	0.46	14.75	88.41	84.72	78.85	90.32
4500	17.38	36.17	0.07	17.64	47.62	1.53	0.46	14.75	89.46	85.72	79.85	91.23
5000	19.25	36.16	0.07	15.90	47.61	1.54	0.46	14.75	90.85	86.74	80.87	91.56
5500	21.13	36.15	0.08	14.16	47.60	1.55	0.46	14.75	92.12	87.76	81.89	92.09
6000	23.00	36.15	0.09	12.43	47.60	1.55	0.47	14.75	93.44	88.77	82.91	92.55
6250	23.94	36.14	0.09	11.56	47.60	1.56	0.47	14.75	94.75	89.79	83.93	93.01
6500	24.87	36.14	0.10	10.69	47.59	1.56	0.47	14.75	96.06	90.80	84.95	93.47
6750	25.81	36.14	0.10	9.83	47.59	1.56	0.47	14.75	97.22	91.81	85.95	94.20
7000	26.57	36.13	0.10	9.12	47.59	1.56	0.47	14.75	98.38	92.81	86.96	94.93
7367	27.15	36.29	0.06	8.74	48.11	1.10	0.33	14.77	99.53	93.82	87.97	95.66

2.5. CONCLUSION

In this chapter, the normal range of the PMSM has been considered according to the torque-speed plot. In addition, for this range, the power losses of devices in the three-level inverter have been calculated. In the following of the thesis, a set of Space Vector Modulation methods are presented in order to balance the heat among the devices.

CHAPTER 3: NEUTRAL-POINT CLAMPED (NPC) THREE-LEVEL INVERTER WITH SPACE VECTOR MODULATION (SVM) TECHNIQUE

3.1. INTRODUCTION

In [14], the three-level NPC converter has been investigated under low voltage ride through condition in the wind power generation system. In this situation, there is an unbalance in the junction temperature of devices in the three-level NPC converter. Therefore, the safe power handling capacity of the power converter will be restricted due to the hottest switches, while the others in principle are operating below full capacity. In order to balance the temperature of devices in a three-level NPC converter, the authors have proposed a series of new SVM methods. In [14], the modulation index, "m" as an important factor in SVM strategy, has been considered as 0.3. This parameter is in fact the ratio between the desired amplitude of the output voltage and the maximum possible amplitude of undistorted sinusoidal voltage that can be generated. Since the modulation index is less than 0.5, the SVM is applicable only in the small hexagon of SVM scheme that has been shown in Figure 1.9. In addition, the phase angle has been considered to be 80^{o} in which the converter operates with a large amount of reactive power.

In the present study, the thermal loss among the power devices in a three-level NPC inverter has been investigated. The inverter is supplying the stator voltages for a SPMSM in an electric vehicle. The PMSM is operating in the region below the base speed. So, there is no need to implement field weakening. In addition, in order to conduct the study in the small hexagon of SVM scheme, the modulation index is considered less than 0.5. Since the hottest switches (inner switches and clamping diodes), in this application are the same as those in [14], the techniques proposed in

[14] are implemented in the present project. In order to decrease the conduction power loss of the hottest switches in the NPC three-level inverter, the dwelling time of zero voltage level should be reduced. Hence, in the present study, the two modified_SVM methods proposed in [14] are investigated for the SPMSM in electric vehicle to see how they performs for this application.

While applying the proposed methods, the conduction power losses of devices in the inverter has been calculated. The product of voltage across the device and current through the device have been computed as instantaneous conduction power of the device. The results illustrate that the new methods can help to redistribute the conduction losses among the devices in order to prolong the life cycle of devices and extend the inverter operation range.

For a specific modulation index, the SVM methods have been applied for two different load angles to indicate the impact of load angle on conduction power loss of the devices. Afterwards, to investigate the influence of modulation index on conduction power of the devices, for a specific load angle, different SVM methods have been implemented for three different modulation indices that are less than 0.5. In the following chapter, for all conditions, the conduction power loss has been computed to evaluate the effectiveness of the methods regarding conduction power balancing among power devices. Finally, the THD of output phase current of the inverter has been calculated for three different modulation indices to evaluate the effect of the proposed methods on the current supplying the motor.

3.2. SPACE VECTOR MODULATION (SVM) TECHNIQUE

There are several types of modulation techniques for two and three-level converters. One of the most common techniques is Space Vector Pulse Width Modulation. This method generates the

gate drive signals for all switches in the converter. The operation of the inverter while producing sinusoidal output voltages can be represented by different switching states (or state vector) and the SVM provides unique switching time calculations for each of these state vectors.

In this method, the desired output phase voltages of the converter are synthesized. The task of the modulator is to decide about the state vector the switches should have and the duty cycle of the switches for synthesizing the reference voltage vector.

The reference rotating space vector voltage representing "V_A", "V_B" and "V_C" (the desired output phase voltages) is computed as the following [21]:

$$V_{ref} = V_{\alpha} + jV_{\beta} = \frac{2}{3}(V_A + V_B e^{j2\pi/3} + V_C e^{-j2\pi/3}) \tag{3.1}$$

So the magnitude and angle of the reference voltage vector is [22]:

$$\left|V_{ref}\right| = \sqrt{(V_{\alpha})^2 + (V_{\beta})^2}$$

$$\angle V_{ref} = \theta = \tan^{-1}(\frac{V_{\beta}}{V_{\alpha}}) \tag{3.2}$$

By expanding (3.1), "V_{α}" and "V_{β}" can be calculated as the following:

$$V_{\alpha} = \frac{2}{3}(V_{A} - \frac{1}{2}V_{B} - \frac{1}{2}V_{C})$$

$$V_{\beta} = \frac{2}{3}(\frac{\sqrt{3}}{2}V_{B} - \frac{\sqrt{3}}{2}V_{C}) \quad (3.3)$$

At every sampling instant, the reference vector is synthesized from the three phase voltages. Therefore, the duration time for each state vector, that will be discussed shortly, is calculated. Considering the following equation, "V_{ref}" is synthesized with three groups of space vectors, (V_a), (V_b) and (V_0).

$$T_S V_{ref} = (T_a V_a + T_b V_b + T_0 V_0) \quad (3.4)$$

where V_a, V_b and V_0 are the vectors defining the triangle in which "V_{ref}" is located and T_a, T_b and T_0 are the corresponding durations of the vectors and "T_S" is the sampling time. So, the sampling time is equal to sum of the duration of each vector:

$$T_S = (T_a + T_b + T_0) \quad (3.5)$$

All the switching states (state vectors) and the reference vector can be represented in a two-dimensional space, which is a hexagon comprising 6 sectors.

3.2.1. SPACE VECTOR MODULATION (SVM) FOR THREE-LEVEL INVERTER

For a three-level inverter, the space vector diagram consists of 6 sectors and each sector is divided into 4 triangles. The space vector diagram for a three-level inverter has been demonstrated in Figure 3.1 and as a sample, the first sector including 4 triangles has been depicted in Figure 3.2. The short vector is in blue, the medium is in green and the large vector is brown.

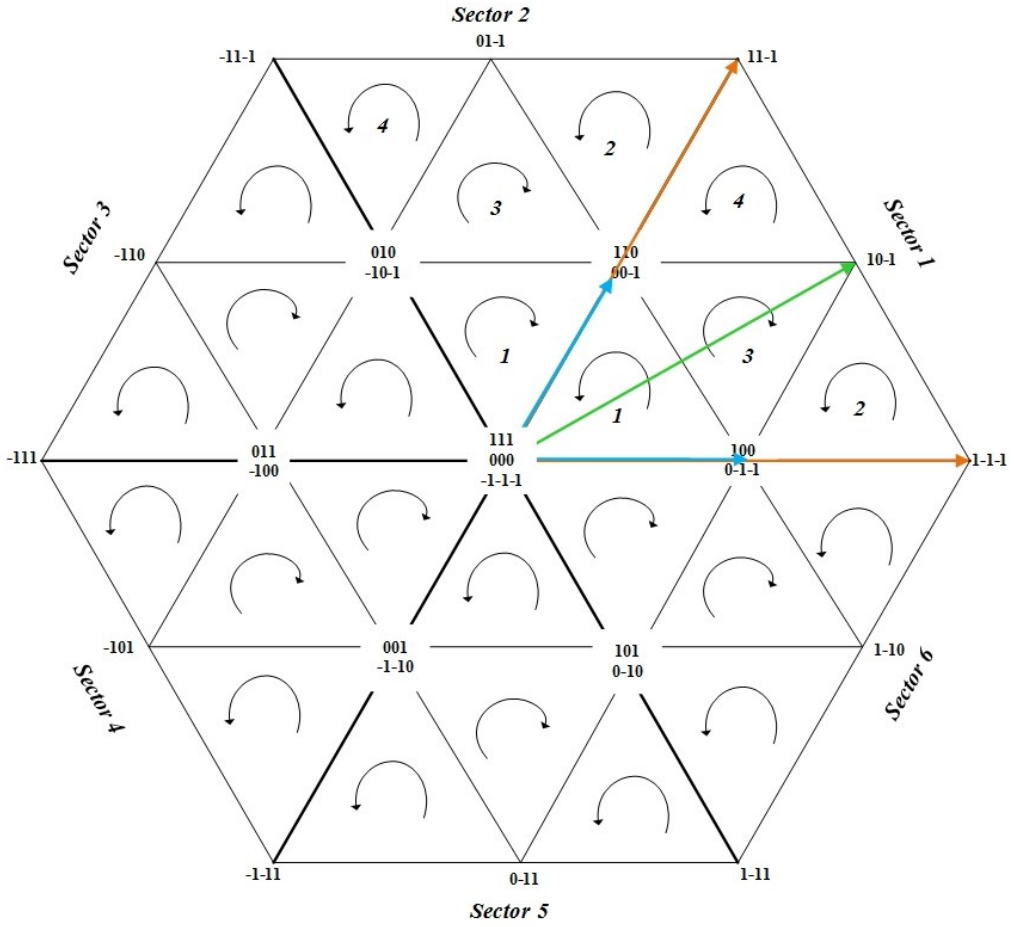


Figure 3. 1: Space vector Diagram for a three-level inverter

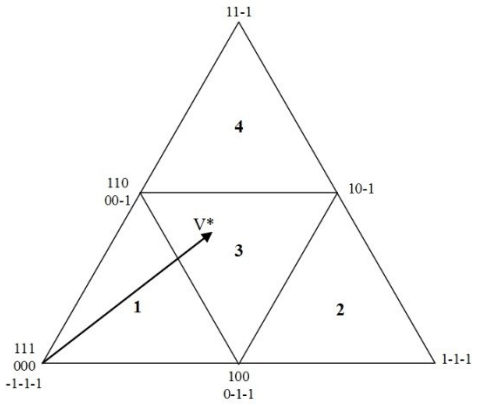


Figure 3. 2: First Sector of the Hexagon

Each state vector has three bits that are pertained to three phases of the three-level inverter. The first bit in the left side is related to phase *A*, the middle bit is for phase *B* and the bit in the right side is related to phase *C*. For example, for the state vector of "*10-1*", in phase *A*, the two upper switches, S_1 and S_2; in phase *B*, the two middle switches, S_2 and S_3 and for phase *C*, the two lower switches, S_3 and S_4 need to be turned on.

Following the pattern for each triangle in the sector results in an On/Off waveform for each phase. The switch has its switching information depending on where the reference vector is located. According to Figure 3.1, the sequence of the state vectors in each triangle is defined in such a way that only one switching transition occurs between two state vectors, otherwise the stress on the devices will be increased if the switching transition occurs at two or three switches simultaneously. Therefore, in all sectors, triangle 2 and triangle 4 have the counter clockwise direction and triangle 3 has the clockwise direction. But for triangle 1, it is a little bit different; in odd sectors, 1, 3 and 5, the direction is counter clockwise and for even sectors, 2, 4 and 6, the direction is clockwise. The sequences should commence with the lowest values to keep the switching transition once per state vector. So, "-1" has higher priority than "0" and "0" has also higher priority than "1". As an example, for two state vectors at the same position, "0-1-1" and

"100", the sequence should commence with "0-1-1". In addition, to determine the start point for a sequence, the value of bits should be considered. For example, in triangle 3 in sector 1, there are three state vectors for the commencement, "0-1-1", "00-1" and "10-1". The best state vector to select is "0-1-1" because the number of lowest values in this state vector is more than other two state vectors.

As an important parameter, the modulation index can be determined according to the side length of the triangles in the sector. As illustrated in Figure 3.3, if the side length of the sector is $2V_{dc}/3$, the modulation index is the ratio of the desired output phase voltage to the maximum sinusoidal phase voltage which is $V_{dc}/\sqrt{3}$.

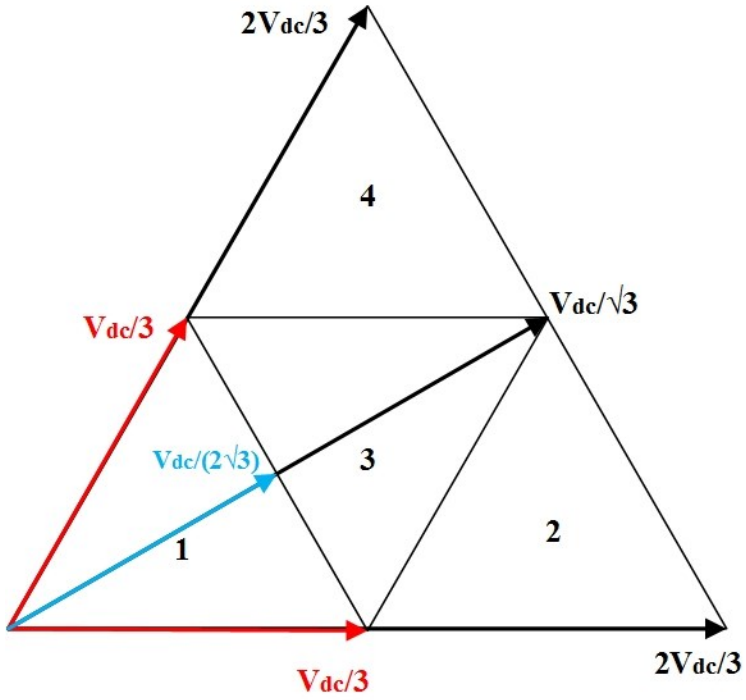


Figure 3. 3: The length of the sectors

For a three-level NPC inverter, there are 288 waveforms for switching sequences; that is $6\ \text{sec}\ tors \times 4\ triangles \times 3\ phases \times 4\ switches$. However, only 144 of these waveforms are needed to calculate because the lower switches in each leg are complementary to the upper switches. The switching signals of Triangle 1 in sector 1 have been shown in Figure 3.4. The sequence is obtained from Figure 3.1.

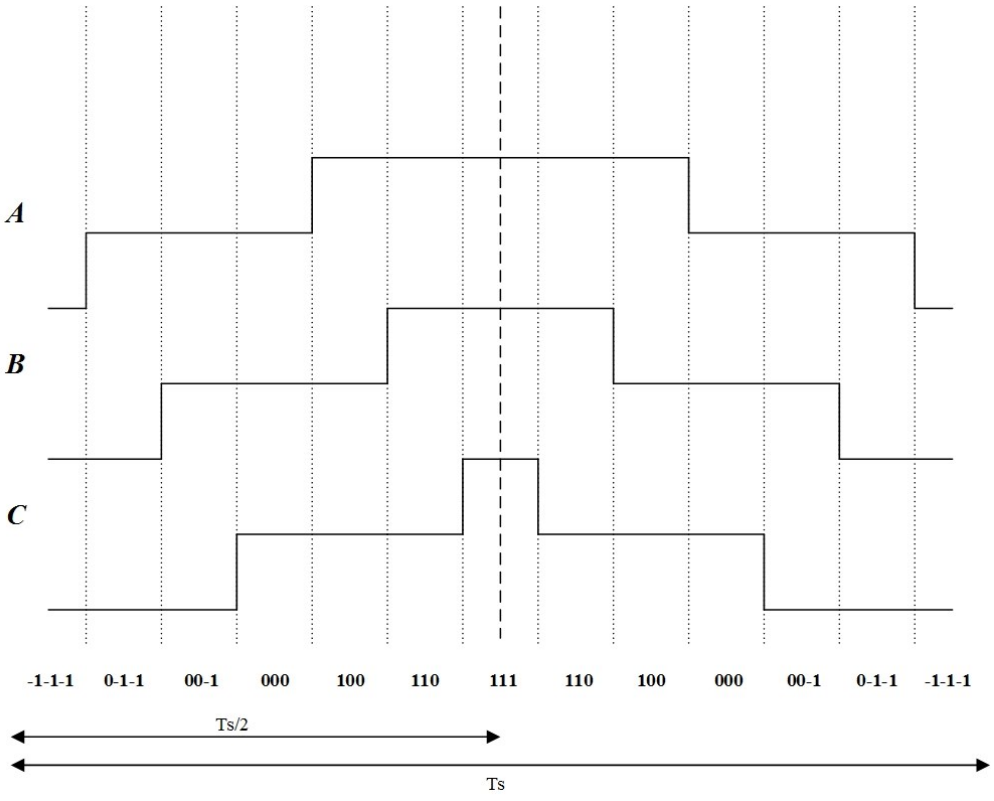


Figure 3. 4: Switching Signals for Triangle 1, Sector 1

In a NPC three-level inverter, the output phase voltage has three different values: $+V_{dc}/2$, 0 and $-V_{dc}/2$; assuming that the dc voltage source is V_{dc}. Depending on the value of the output phase voltage, different switches in one leg need to be turned on.

Conforming to Figure 2.5, for $+V_{dc}/2$ in the output, upper switches S_1 and S_2 need to be turned on. For the zero level, two middle switches, S_2 and S_3 and for the third level, $-V_{dc}/2$ the two lower switches, S_3 and S_4 need to be turned on. The operation of the switches has been summarized in Table 3.1 [23].

Table 3. 1: Switching operation of the NPC three-level inverter

Output Phase Voltage	S_1 (Phases A,B,C)	S_2 (Phases A,B,C)	S_3 (Phases A,B,C)	S_4 (Phases A,B,C)
$+V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

As it is illustrated in Figure 3.5, according to the vector length, the state vectors have been classified into 4 groups [24-25]:

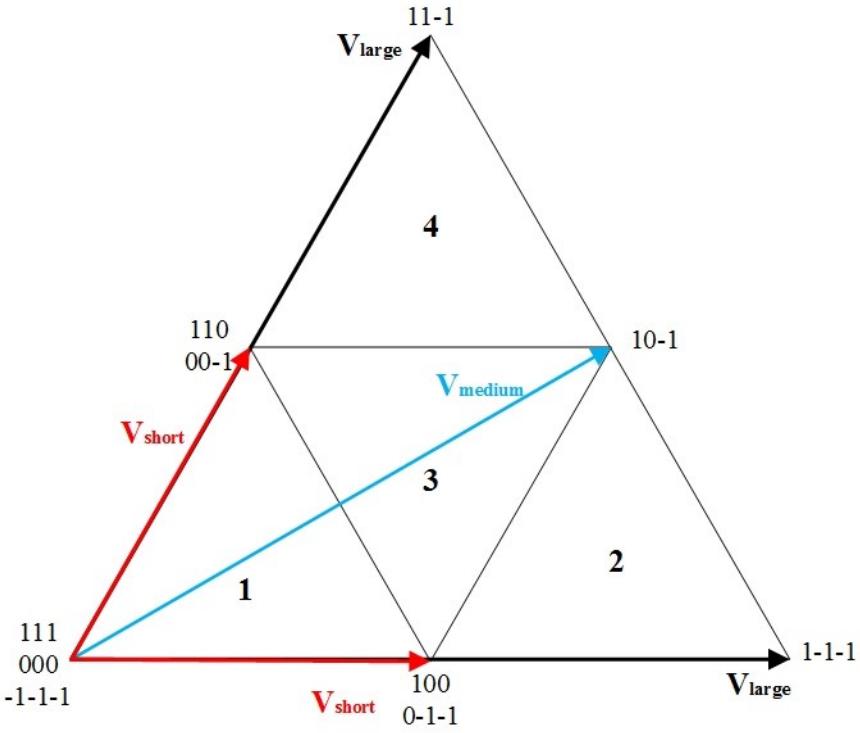


Figure 3. 5: Vectors' Length in Sector 1

a) Zero vectors which are located in the center of the hexagon or at the origin of the sector. These vectors are -1-1-1, 000 and 111.

b) Large vectors whose length is $2V_{dc}/3$. These vectors are 1-1-1, 11-1, -11-1, -111, -1-11 and 1-11.

c) Medium vectors which are the height of each sector and their length is $V_{dc}/\sqrt{3}$. These vectors are 10-1, 01-1, -110, -101, 0-11 and 1-10.

d) Short vectors which are the diagonals of the inner hexagon and their length is $V_{dc}/3$. These vectors are 0-1-1, 100, 00-1, 110,-10-1, 010,-100, 011,-1-10, 001 and 0-10,101.

The SVM for three-level inverters can be implemented by 4 successive steps:

a) Sector determination

b) Triangle determination in one sector

c) Calculation of switching times; T_a, T_b and T_0

d) Determination of the switching states (state vectors)

3.2.1.1. SECTOR DETERMINATION

To determine the sector in which the reference voltage vector is located, the following procedure should be considered. Since the hexagon is comprised of six sectors, each sector is 60°. Due to circular symmetry, if the reference vector is located in sectors other than sector 1, it is possible to relocate the reference vector to the first sector. The equations are in Table 3.2.

Table 3. 2: The Range of Angle in All Sectors

Sectors	*The range of the angle*	*How to get into the 1st sector*
1	$0 \le \theta \le 60^\circ$	$\theta_{new} = \theta_{old} - 0$
2	$60^\circ \le \theta \le 120^\circ$	$\theta_{new} = \theta_{old} - 60^\circ$
3	$120^\circ \le \theta \le 180^\circ$	$\theta_{new} = \theta_{old} - 120^\circ$
4	$180^\circ \le \theta \le 240^\circ$	$\theta_{new} = \theta_{old} - 180^\circ$
5	$240^\circ \le \theta \le 300^\circ$	$\theta_{new} = \theta_{old} - 240^\circ$
6	$300^\circ \le \theta \le 360^\circ$	$\theta_{new} = \theta_{old} - 300^\circ$

3.2.1.2. TRIANGLE DETERMINATION IN ONE SECTOR

To determine the triangle in which the tip of the reference vector lies, there are four comparisons for two parameters, denoted as "m_1" and "m_2" which are calculated according to the angle of the reference vector, θ:

$$m_1 = m\left(\cos\theta - \frac{\sin\theta}{\sqrt{3}}\right)$$
$$m_2 = m\left(\frac{2\sin\theta}{\sqrt{3}}\right) \tag{3.6}$$

If $(m_1+m_2) \leq 1/\sqrt{3}$, then the reference vector is in triangle 1. If $m_1 > 1/\sqrt{3}$, then the reference vector is in triangle 2. If m_1 and $m_2 \leq 1/\sqrt{3}$ and $(m_1+m_2) > 1/\sqrt{3}$, then the reference vector is in triangle 3 and finally, if $m_2 > 1/\sqrt{3}$, then the reference vector is in triangle 4. The following table is the summary of the procedure to find the triangle in which the reference vector lies.

Table 3. 3: The Conditions for Determination of the Triangles

Triangle	Condition
1	$(m_1 + m_2) \leq 1/\sqrt{3}$
2	$m_1 > 1/\sqrt{3}$
3	$m_1 \leq 1/\sqrt{3}$ $m_2 \leq 1/\sqrt{3}$ $(m_1 + m_2) > 1/\sqrt{3}$
4	$m_2 > 1/\sqrt{3}$

3.2.1.3. CALCULATION OF SWITCHING TIMES

Due to the similarity of sectors, it is sufficient to consider the first sector ($0 \leq\theta \leq 60^{o}$) to calculate the times, T_a, T_b and T_0. The definition for times are different for the 4 triangles in sector 1 but they are identical for the corresponding triangle in other sectors. In this study, the PMSM is operating under the base speed. So, the analysis in this work is limited to Triangle 1. Accordingly, the time definition will be presented for Triangle 1 in sector 1 and they can be generalized for other sectors.

For the first triangle, the reference vector is synthesized by two short vectors and one zero vector. Figure 3.6 has shown the scheme and the time calculation is as the following [21]:

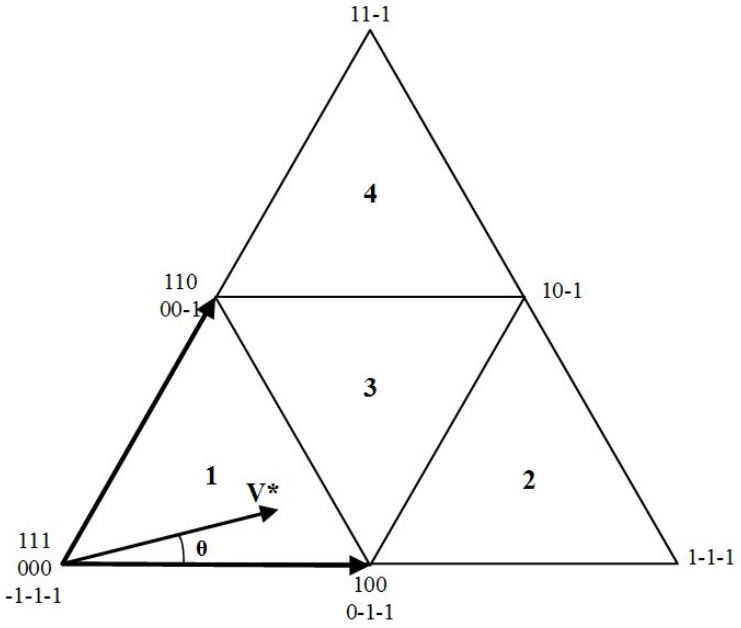


Figure 3. 6: Triangle 1 in Sector 1

T_a is the time regarding the state vectors "0-1-1" and "100" and T_b is the time for "00-1" and "110".

$$T_a = T_s \times (m\sqrt{3}\cos\theta - \sin\theta)$$

$$T_b = T_s \times (2m\sin\theta) \tag{3.7}$$

$$T_0 = T_s \times (1 - m(\sqrt{3}\cos\theta + \sin\theta))$$

3.2.1.4. SWITCHING STATE DETERMINATION

In the present study, the modulation indices have been considered less than 0.5. Hence, the reference voltage vector will be located in Triangle 1 in all sectors (inner hexagon). The state vector sequences of Triangle 1 in all sectors have been presented in Table 3.4. In Triangle 1, there are 7 state vectors in the state sequence that commences with a zero state vector, "-1-1-1". It should be considered that these sequences are for half a space vector cycle and for the second half, the sequence will be reversed. Therefore, it will be terminated with the state vector "-1-1-1" as indicated in Figure 3.4.

Table 3. 4: All switching State Sequences in SVM scheme for three-level inverter in triangle 1, all sectors

Sector	*Triangle*	*Switching States Sequence*
1	***1***	-1-1-1 , 0-1-1 , 00-1 , 000 , 100 , 110 , 111
2	***1***	-1-1-1 , -10-1 , 00-1 , 000 , 010 , 110 , 111
3	***1***	-1-1-1 , -10-1 , -100 , 000 , 010 , 011 , 111
4	***1***	-1-1-1 , -1-10 , -100 , 000 , 001 , 011 , 111
5	***1***	-1-1-1 , -1-10 , 0-10 , 000 , 001 , 101 , 111
6	***1***	-1-1-1 , 0-1-1 , 0-10 , 000 , 100 , 101 , 111

3.2.2. THREE SPACE VECTOR MODULATION (SVM) METHODS

In the present study, three methods based on SVM strategy have been presented; Normal, O2 and O3. All these methods are applied to generate the gating signals for the switches in a three-level inverter.

The "*Normal*" SVM method is the common modulation method in which all state vectors mentioned in Table 3.4 are used in the state sequences. The state sequence starts from zero state vector, "-1-1-1" and returns to the same state vector. Therefore, the state sequence comprises all 7 state vectors.

In order to reduce the zero voltage dwelling time to redistribute the conduction power among switches, two new SVM strategies have been presented; "O2" and "O3" [14]. In O2 SVM, the state vector "000" is eliminated but other state vectors are kept in the state sequence. Therefore, there will be 6 state vectors in a sequence. In this method, the inner switches, S2 and S3 will be relieved more due to the elimination of the state vector "000". In O3 SVM, two zero state vectors "-1-1-1" and "111" are ignored to decrease the stress on the outer switches, S1 and S4. Hence, the state sequence comprises 5 state vectors, it starts from a non-zero state vector and returns to the same state vector.

In the following sections, the duty cycle of the devices obtained via these three modulation methods have been presented to be later used in the analysis of the performance of the methods.

3.2.3. DUTY CYCLE DEFINITION

The term "*Duty Cycle*" is principally the proportion of *ON* time to one switching period, "T_s" (SVM cycle). In other words, the duty cycle describes the *ON-state* of the device as a percentage of the total SVM cycle. Therefore, a low duty cycle for a power device corresponds to low

conduction power losses because the device is in *OFF-state* for most of the time. In the present study, two terms regarding duty cycle have been introduced; "Enabled Duty Cycle" and "Conduction Duty Cycle".

Based on the generated gating signals in SVM scheme, the switches in one leg get enabled to conduct the current. However, either the switch or the anti-parallel diode is going to conduct depending on the direction of the output phase current, in that leg. So, each device conducts for a fraction of the switching period and for the rest of the switching period, it remains open-circuit.

In principal, since only switches need to be enabled to conduct, the term "*Enabled Duty Cycle*" is applicable only for switches. However, this term is also useable for clamping diodes, D_5 and D_6, because they conduct the zero state current simultaneously with S2 and S3. The enabled duty cycle is the duration in which the switch is turned on according to the SVM method, but it does not necessarily mean that the switch is going to conduct.

The term "*Conduction Duty Cycle*" is for both switch and diode. It defines the proportion of conducting time to the switching period. In order to calculate the conduction duty cycle, it is important to determine the direction of the output phase current. Initially, the switch needs to be enabled. Then, if the direction of the output phase current is in accordance with the switch direction, the switch will conduct; otherwise the anti-parallel diode will conduct the current. Therefore, the "conduction duty cycle" is the parameter that should be closely related to the conduction losses of diodes and switches.

3.2.3.1. EFFECT OF POWER FACTOR ON CURRENT POLARITIES

After synthesizing a given reference voltage vector, the current direction should be evaluated. In order to determine the direction of output phase current, "*Power Factor,*" that is, the cosine of the angle between the voltage and the current waveforms in a phase, has an important role.

The power factor along with the knowledge of the angle of the phase voltage can define whether the current is positive or negative. Consequently, the appropriate devices (either switches or diodes) for conducting the current can be determined. Afterwards, the duty cycle of the devices can be calculated according to the conduction time assigned to each device. Hence, to obtain the conduction duty cycle, it is essential to investigate the polarities of the output phase current.

The combination of the polarities for three phase currents is shown in Table 3.5 assuming the balanced sinusoidal currents with 120° phase shift; $i_a(t) = I\ Sin\ (\omega t)$, $i_b(t) = I\ Sin\ (\omega t - 120^\circ)$ and $i_c(t) = I\ Sin\ (\omega t + 120^\circ)$.

The polarities of phase currents are changing every 60°. Since the hexagon is 360°, there are six groups of current polarities.

Table 3. 5: Combination of Current Polarities

Combinations	***Range of ωt***	***Current Polarities***		
0-degree	$0^o < \omega t < 60^o$	Ia > 0	Ib < 0	Ic > 0
60-degree	$60^o < \omega t < 120^o$	Ia > 0	Ib < 0	Ic < 0
120-degree	$120^o < \omega t < 180^o$	Ia > 0	Ib > 0	Ic < 0
180-degree	$180^o < \omega t < 240^o$	Ia < 0	Ib > 0	Ic < 0
240-degree	$240^o < \omega t < 300^o$	Ia < 0	Ib > 0	Ic > 0
300-degree	$300^o < \omega t < 360^o$	Ia < 0	Ib < 0	Ic > 0

The space vector diagram is comprising six sectors but due to the circular symmetry, only the first two sectors have been considered to study. Therefore, for Sectors 1 and 2, the range for reference vector angle is $0^o < \theta < 120^o$.

In addition, three phase waveforms can be divided into three 120^o degrees. Based on the three phase waveforms, it can be observed that there is a similarity between the second and third 120^o segments of each phase and the first 120^o of the other phases. Therefore, one cycle (360^o) of 3 waveforms can be obtained from 120^o of the 3 waveforms. Accordingly, only the calculation of the first 120^o of three phases is required to obtain the whole 360^o of duty cycles for 3 phases. Regardless of the power factor, this strategy for getting the 360^o of duty cycle is applicable for different SVM methods. This homogeneous character of waveforms is summarized in Table 3.6.

Table 3. 6: The summary of Phase Similarities for Current Waveforms

Phase	**Angle**		
	$0^o < \omega t < 120^o$	$120^o < \omega t < 240^o$	$240^o < \omega t < 360^o$
A	A_{120}	C_{120}	B_{120}
B	B_{120}	A_{120}	C_{120}
C	C_{120}	B_{120}	A_{120}

In order to investigate the angle at which the first change in a current polarity occurs for $0^o < \omega t < 120^o$, θ_{max} should be calculated. Hence, for a current waveform lagging the voltage waveform by a certain angle "α", the value of θ_{max} is presented in Table 3.7.

Table 3. 7: Calculation of θ_{max} according to load angle

Load angle (α)	θ_{max}
$-90^\circ < \alpha < -30^\circ$	$\theta_{max} = \alpha + 90^\circ$
$-30^\circ < \alpha < 30^\circ$	$\theta_{max} = \alpha + 30^\circ$
$30^\circ < \alpha < 90^\circ$	$\theta_{max} = \alpha - 30^\circ$

To obtain the current polarities for a specific power factor (or the phase angle between current and voltage waveforms, α) there are two steps as the following:

a) Find the appropriate "combination" that defines the polarities of the three-phase currents at a certain time. This can be done from $\alpha_{new} = 90^\circ - \alpha$:

   The proper combination for beginning can be found according to this new angle, α_{new}. The combination in which α_{new} locates will be the first combination.

b) Determine the angle at which a current polarity changes based on θ_{max}.

   To determine the combination shifting, θ_{max} should be used; The first combination is used in $0^\circ < \theta < \theta_{max}$, the second combination in $\theta_{max} < \theta < \theta_{max} + 60^\circ$ and if it is applicable, the third combination in $\theta_{max} + 60^\circ < \theta < 120^\circ$.

For various ranges of load angle, the procedure to investigate the current polarities is illustrated in Table 3.8.

Table 3. 8: The procedure to find current polarities

Lag load angle (α)	θ_{max}	*Start combination*	*Combination for sectors 1 & 2*	*Current polarities*
0º	30º	Comb_60º	$0^\circ < \theta < 30^\circ$	$Ia > 0\ ,\ Ib < 0\ ,\ Ic < 0$
			$30^\circ < \theta < 90^\circ$	$Ia > 0\ ,\ Ib > 0\ ,\ Ic < 0$
			$90^\circ < \theta < 120^\circ$	$Ia < 0\ ,\ Ib > 0\ ,\ Ic < 0$
$0^\circ < \alpha < 30^\circ$	$\alpha + 30^\circ$	Comb_60º	$0^\circ < \theta < \theta_{max}$	$Ia > 0\ ,\ Ib < 0\ ,\ Ic < 0$
			$\theta_{max} < \theta < 60^\circ$	
			$60^\circ < \theta < \theta_{max} + 60^\circ$	$Ia > 0\ ,\ Ib > 0\ ,\ Ic < 0$
			$\theta_{max} + 60^\circ < \theta < 120^\circ$	$Ia < 0\ ,\ Ib > 0\ ,\ Ic < 0$
$30^\circ < \alpha < 90^\circ$	$\alpha - 30^\circ$	Comb_0º	$0^\circ < \theta < \theta_{max}$	$Ia > 0\ ,\ Ib < 0\ ,\ Ic > 0$
			$\theta_{max} < \theta < 60^\circ$	$Ia > 0\ ,\ Ib < 0\ ,\ Ic < 0$
			$60^\circ < \theta < \theta_{max} + 60^\circ$	
			$\theta_{max} + 60^\circ < \theta < 120^\circ$	$Ia > 0\ ,\ Ib > 0\ ,\ Ic < 0$
90º	60º	Comb_0º	$0^\circ < \theta < 60^\circ$	$Ia > 0\ ,\ Ib < 0\ ,\ Ic > 0$
			$60^\circ < \theta < 120^\circ$	$Ia > 0\ ,\ Ib < 0\ ,\ Ic < 0$

3.2.3.2. CONDUCTION DUTY CYCLE FOR "NORMAL" SPACE VECTOR MODULATION (SVM) TECHNIQUE

For a Normal SVM, there are 7 state vectors in Triangle 1; three of which are zero state vectors and the other four state vectors are the active states. In Normal SVM, all state vectors are used in the sequence in order to synthesize the reference voltage.

As stated in section 3.2.1, the direction of state sequences in Triangle 1, odd sectors differs to even sectors. Therefore, due to the circular symmetry in SVM scheme, only the analysis pertaining to Sector 1 and Sector 2 are presented and this could be generalized for other sectors.

As mentioned previously, the conduction duty cycle is applicable for both switch and diode. Considering the switching states, the switches and diodes that are conducting corresponding to each state vector have been shown in Table 3.9 for Triangle 1, Sector 1. Recall that the switches to be enabled in a given phase, depend on the space vector to be used, which is defined by the SVM method. However, the conducting switches as well as diodes will also depend on the direction of the current. For instance, for space vector -1-1-1, the state of phase A is -1, meaning that S_{A3} and S_{A4} are enabled, but will only conduct when $I_A<0$. Otherwise, with $I_A>0$, D_{A3} and D_{A4} will conduct. Since a space vector with -1 as the first bit is only used in the first of the 7 elements of the state sequence in Triangle 1 Sector 1, the enabled time of, say, S_{A4} is only $(T_0/8)$ in $(Ts/2)$. Its enabled duty cycle would then be $(T_0/8)/(Ts/2)$ while its conduction duty cycle could be the same value or zero, if at that space vector cycle the current in phase A was positive. $(Ts/2)$ is used in this case because in one space vector cycle (T_s) one executes the space vector sequence once in the clockwise and once in the counter clockwise directions, as shown in Figure 3.4 and Figure 3.7.

The duration of T_0, as well as of T_a and T_b, will depend on the magnitude and position of the reference voltage vector at a given time. Conversely, one can see that S_{A3} will be enabled not only

during $(T_0/8)$, but also $(T_a/4)$, $(T_b/4)$ and $(T_0/4)$, which correspond to the first 4 state vectors of the 7-state sequence used in Triangle 1, Sector 1.

$$T_S = T_a + T_b + T_0$$

$$1 = \frac{1}{T_S}(T_a + T_b + T_0) = d_a + d_b + d_0 \tag{3.8}$$

Table 3. 9: State vectors and Related Switches and Diodes in Triangle 1, Sector 1 (Normal SVM)

Triangle 1		*Zero*(T_0/8)	*a* (T_a/4)	*b* (T_b/4)	*2*Zero*(T_0/4)	*a* (T_a/4)	*b* (T_b/4)	*Zero*(T_0/8)
		-1-1-1	0-1-1	00-1	000	100	110	111
Phase a	I>0	D_3 , D_4	D_5 , S_2			S_1 , S_2		
	I<0	S_3 , S_4	D_6 , S_3			D_1 , D_2		
Phase b	I>0	D_3 , D_4		D_5 , S_2			S_1 , S_2	
	I<0	S_3 , S_4		D_6 , S_3			D_1 , D_2	
Phase c	I>0	D_3 , D_4			D_5 , S_2			S_1 , S_2
	I<0	S_3 , S_4			D_6 , S_3			D_1 , D_2

Table 3.10 shows the expressions that should be used for calculating the conduction duty cycle for the switches and diodes of all three phases when the reference voltage vector lies in Triangle 1 Sector 1.

As shown in Table 3.6, one can study a full line cycle (360°) of the three phase voltage waveforms from the first 120° of the three-phases. This corresponds to the reference voltage vector rotating in Sector 1 and Sector 2. Table 3.11 and Table 3.12 bring the same information for Sector 2 that Table 3.9 and Table 3.10 presented for Sector 1.

Table 3. 10: Conduction duty cycle for devices in Triangle 1, Sector 1 (Normal SVM)

Current	***I > 0***		***I < 0***	
Phase	***Switch***	***Conduction duty Cycle***	***Switch***	***Conduction duty Cycle***
Phase a	S_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{8})$	D_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{8})$
	S_{a2}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_0}{8})$	D_{a2}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{8})$
	D_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{8})$	S_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4}+2\times\frac{T_0}{8})$
	D_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{8})$	S_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{8})$
	D_{a5}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+2\times\frac{T_0}{8})$	D_{a6}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+2\times\frac{T_0}{8})$
Phase b	S_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_0}{8})$	D_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_0}{8})$
	S_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+2\times\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{8})$	D_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_0}{8})$
	D_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4})$	S_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4}+2\times\frac{T_0}{8}+\frac{T_a}{4})$
	D_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4})$	S_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4})$
	D_{b5}	$\frac{2}{Ts}\times(\frac{T_b}{4}+2\times\frac{T_0}{8}+\frac{T_a}{4})$	D_{b6}	$\frac{2}{Ts}\times(\frac{T_b}{4}+2\times\frac{T_0}{8}+\frac{T_a}{4})$
Phase c	S_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{8})$	D_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{8})$
	S_{c2}	$\frac{2}{Ts}\times(2\times\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{8})$	D_{c2}	$\frac{2}{Ts}\times(\frac{T_0}{8})$
	D_{c3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4})$	S_{c3}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_0}{8})$
	D_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4})$	S_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4})$
	D_{c5}	$\frac{2}{Ts}\times(2\times\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4})$	D_{c6}	$\frac{2}{Ts}\times(2\times\frac{T_0}{8}+\frac{T_a}{4}+\frac{T_b}{4})$

Table 3. 11: State vectors and Related Switches and Diodes in Triangle 1, Sector 2 (Normal SVM)

Triangle 1		*Zero*(T_0/8)	*b* (T_b/4)	*a* (T_a/4)	*2*Zero*(T_0/4)	*b* (T_b/4)	*a* (T_a/4)	*Zero*(T_0/8)
		-1-1-1	-10-1	00-1	000	010	110	111
Phase a	I>0	D_3 , D_4		D_5 , S_2			S_1 , S_2	
	I<0	S_3 , S_4		D_6 , S_3			D_1 , D_2	
Phase b	I>0	D_3 , D_4	D_5 , S_2			S_1 , S_2		
	I<0	S_3 , S_4	D_6 , S_3			D_1 , D_2		
Phase c	I>0	D_3 , D_4			D_5 , S_2			S_1 , S_2
	I<0	S_3 , S_4			D_6 , S_3			D_1 , D_2

Regarding the calculation of times T_a, T_b and T_0 in Triangle 1 Sector 2, the first step is to relocate the vector to Triangle 1, Sector 1 in order to reach easier analysis. Although the initial state vectors in sectors 1 and 2 are identical, the state sequences are in opposite direction. According to Figure 3.8, the state sequence in Sector 2 is in clockwise direction and it should be shuffled to Sector 1 ($\theta_{new} = \theta_{old} - 60^\circ$). Therefore, T_0, T_b and T_a will be used as the sequence of time as mentioned in Table 3.11. T_a is the time regarding the state vectors "00-1" and "110" and T_b is the time for "-10-1" and "010".

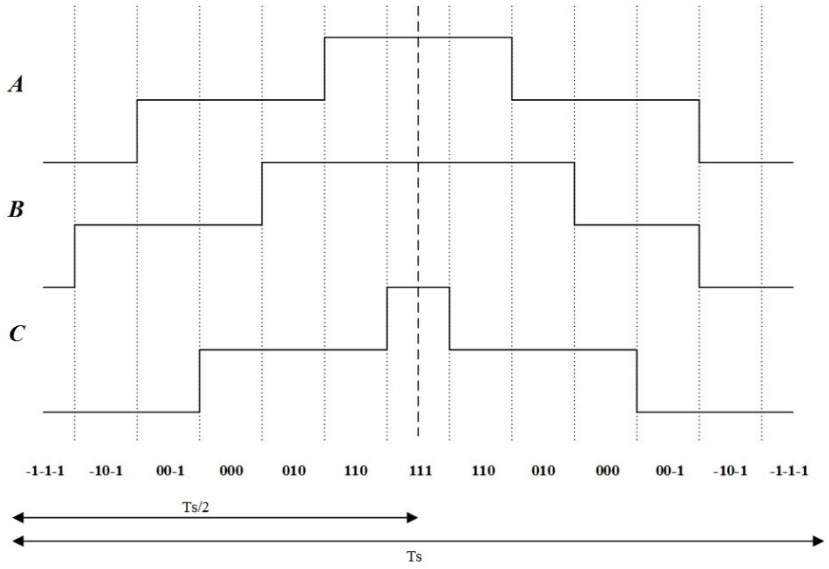


Figure 3. 7: Switching signal and state sequence in Triangle 1, Sector 2 (Normal SVM)

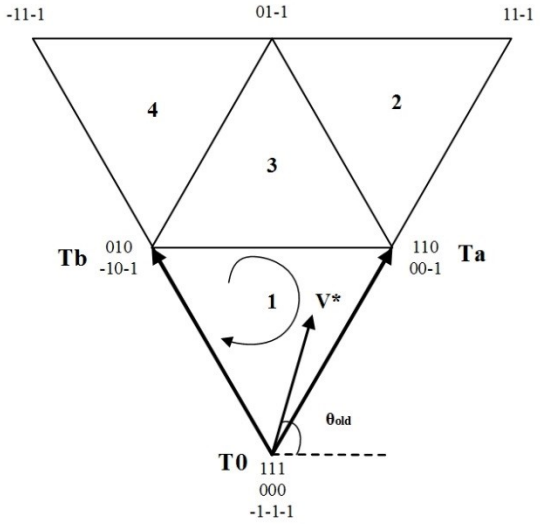


Figure 3. 8: State vectors in Triangle 1, Sector 2

Figure 3.7 depicts the switching signals of three phases in Triangle 1, Sector 2 and Figure 3.9 illustrates Sector 2 shuffled to Sector 1.

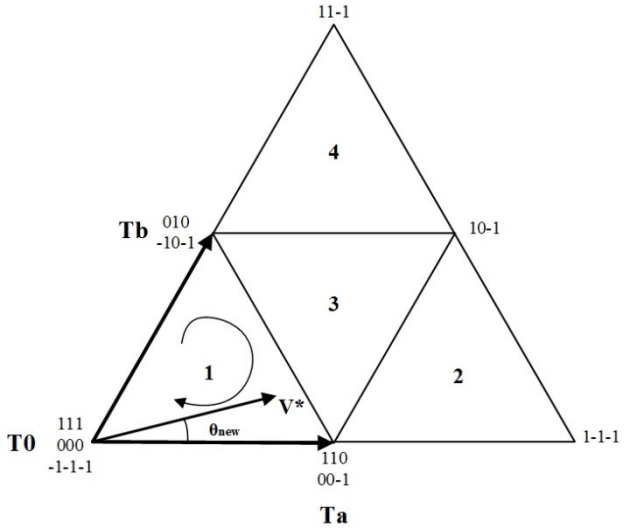


Figure 3. 9: State vectors in Triangle 1, Sector 2 relocated to Sector 1

Table 3. 12: Conduction duty cycle for devices in Triangle 1, Sector 2 (Normal SVM)

Current	***I > 0***		***I < 0***	
Phase	***Switch***	***Conduction duty Cycle***	***Switch***	***Conduction duty Cycle***
Phase a	S_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{8})$	D_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{8})$
	S_{a2}	$\frac{2}{Ts}\times(\frac{T_a}{4}+2\times\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{8})$	D_{a2}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{8})$
	D_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4})$	S_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4}+2\times\frac{T_0}{8}+\frac{T_b}{4})$
	D_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4})$	S_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4})$
	D_{a5}	$\frac{2}{Ts}\times(\frac{T_a}{4}+2\times\frac{T_0}{8}+\frac{T_b}{4})$	D_{a6}	$\frac{2}{Ts}\times(\frac{T_a}{4}+2\times\frac{T_0}{8}+\frac{T_b}{4})$
Phase b	S_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{8})$	D_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{8})$
	S_{b2}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_0}{8})$	D_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{8})$
	D_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{8})$	S_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4}+2\times\frac{T_0}{8})$
	D_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{8})$	S_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{8})$
	D_{b5}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+2\times\frac{T_0}{8})$	D_{b6}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+2\times\frac{T_0}{8})$
Phase c	S_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{8})$	D_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{8})$
	S_{c2}	$\frac{2}{Ts}\times(2\times\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{8})$	D_{c2}	$\frac{2}{Ts}\times(\frac{T_0}{8})$
	D_{c3}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4})$	S_{c3}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_0}{8})$
	D_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4})$	S_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4})$
	D_{c5}	$\frac{2}{Ts}\times(2\times\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4})$	D_{c6}	$\frac{2}{Ts}\times(2\times\frac{T_0}{8}+\frac{T_b}{4}+\frac{T_a}{4})$

3.2.3.3. CONDUCTION DUTY CYCLE FOR "O2" SPACE VECTOR MODULATION (SVM) TECHNIQUE

As mentioned before, in this study, the modulation index is less than 0.5. So in all sectors, the reference voltage vector is located in the first triangle. According to section 3.2.3.2, in Normal SVM, all state vectors are implemented in the switching state sequence. However, in the first modified SVM method (O2), one of the zero state vectors, "000" is eliminated and replaced by the other two equivalent state vectors which are "-1-1-1" and "111". Therefore, the time duration for the zero state vectors will be different from those of Normal SVM method. The state sequences of Triangle 1 in Sectors 1 and 2 for O2 SVM are presented in Table 3.13.

Table 3. 13: State sequences in Triangle 1, Sectors 1 and 2 (O2 SVM)

Sector	Triangle	Switching States Sequence
1	***1***	-1-1-1 , 0-1-1 , 00-1 , 100 , 110 , 111
2	***1***	-1-1-1 , -10-1 , 00-1 , 010 , 110 , 111

The state sequence and time duration assigned to each state vector in Triangle 1, Sector 1 is shown in Table 3.14.

Table 3. 14: State vectors and Related Switches and Diodes in Triangle 1, Sector 1 (O2 SVM)

Triangle 1		*Zero*(T_0/4)	*a* (T_a/4)	*b* (T_b/4)	*a* (T_a/4)	*b* (T_b/4)	*Zero*(T_0/4)
		-1-1-1	0-1-1	00-1	100	110	111
Phase a	I>0	D_3 , D_4	D_5 , S_2		S_1 , S_2		
	I<0	S_3 , S_4	D_6 , S_3		D_1 , D_2		
Phase b	I>0	D_3 , D_4		D_5 , S_2		S_1 , S_2	
	I<0	S_3 , S_4		D_6 , S_3		D_1 , D_2	
Phase c	I>0	D_3 , D_4			D_5 , S_2		S_1 , S_2
	I<0	S_3 , S_4			D_6 , S_3		D_1 , D_2

From Table 3.13, it can be seen that the zero state vector “000” has been eliminated from the state sequences. Therefore the total time duration for zero state vectors is divided between other zero state vectors, “-1-1-1” and “111”.

Since the zero state vectors are common for the first triangle in all sectors, the time division for zero state vectors in other sectors resembles to that of the first sector. Except the state sequence and zero state time division, other properties of this method are similar to those of Normal SVM such as the direction of state sequence of Triangle 1 in all odd sectors and time duration for other state vectors. According to the generated gating signals, the switches in one leg get enabled and considering the direction of output current, either the switch or the anti-parallel diode is going to conduct.

The devices conducting the current regarding each state vector have been presented in Table 3.14. Table 3.15 shows the expressions that should be used for calculating the conduction duty cycle for the switches and diodes of all three phases when the reference voltage vector lies in Triangle 1 Sector 1. In addition, Table 3.16 and Table 3.17 bring the same information for Sector 2 that Table 3.14 and Table 3.15 presented for Sector 1.

Table 3. 15: Conduction duty cycle for devices in Triangle 1, Sector 1 (O2 SVM)

Current	***I > 0***		***I < 0***	
Phase	***Switch***	***Conduction duty Cycle***	***Switch***	***Conduction duty Cycle***
Phase a	S_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{4})$	D_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{4})$
	S_{a2}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_0}{4})$	D_{a2}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{4})$
	D_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{4})$	S_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4}+\frac{T_b}{4})$
	D_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{4})$	S_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{4})$
	D_{a5}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4})$	D_{a6}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4})$
Phase b	S_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_0}{4})$	D_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_0}{4})$
	S_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{4})$	D_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_0}{4})$
	D_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4})$	S_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_a}{4})$
	D_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4})$	S_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4})$
	D_{b5}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$	D_{b6}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$
Phase c	S_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{4})$	D_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{4})$
	S_{c2}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_0}{4})$	D_{c2}	$\frac{2}{Ts}\times(\frac{T_0}{4})$
	D_{c3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4}+\frac{T_b}{4})$	S_{c3}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_0}{4})$
	D_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4}+\frac{T_b}{4})$	S_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_a}{4}+\frac{T_b}{4})$
	D_{c5}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4})$	D_{c6}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4})$

Conforming to Table 3.15, the conduction duty cycle of inner switch, S2, is $\frac{2}{Ts} \times (\frac{Ts}{2} - \frac{T_0}{4})$. Comparing this expression with the corresponding one in Table 3.10 ($\frac{2}{Ts} \times (\frac{Ts}{2} - \frac{T_0}{8})$), it can be deduced that the by implementing O2 SVM technique, the conduction duty cycle of inner switch, S2 is reduced. To mention the same comparison for other inner switch, S3, these expressions are $\frac{2}{Ts} \times (\frac{T_0}{8} + \frac{T_a}{4} + \frac{T_b}{4} + 2 \times \frac{T_0}{8})$ and $\frac{2}{Ts} \times (\frac{T_0}{4} + \frac{T_a}{4} + \frac{T_b}{4})$ for Normal and O2 SVM strategies respectively. Accordingly, O2 SVM technique has reduced the conduction duty cycle of inner switches. Moreover, for the clamping diodes, the conduction duty cycle in Normal SVM is $\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4} + 2 \times \frac{T_0}{8})$ and in O2 SVM is $\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$. It is obvious that the conduction duty cycle of clamping diodes has been reduced by using O2 SVM technique.

Table 3. 16: State vectors and Related Switches and Diodes in Triangle 1, Sector 2 (O2 SVM)

Triangle 1		*Zero*(T_0/4)	*b* (T_b/4)	*a* (T_a/4)	*b* (T_b/4)	*a* (T_a/4)	*Zero*(T_0/4)
		-1-1-1	-10-1	00-1	010	110	111
Phase a	I>0	D_3 , D_4		D_5 , S_2		S_1 , S_2	
	I<0	S_3 , S_4		D_6 , S_3		D_1 , D_2	
Phase b	I>0	D_3 , D_4	D_5 , S_2		S_1 , S_2		
	I<0	S_3 , S_4	D_6 , S_3		D_1 , D_2		
Phase c	I>0	D_3 , D_4			D_5 , S_2		S_1 , S_2
	I<0	S_3 , S_4			D_6 , S_3		D_1 , D_2

Table 3. 17: Conduction duty Cycle for devices in Triangle 1, Sector 2 (O2 SVM)

Current	***I > 0***		***I < 0***	
Phase	***Switch***	***Conduction duty Cycle***	***Switch***	***Conduction duty Cycle***
Phase a	S_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{4})$	D_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{4})$
	S_{a2}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{4})$	D_{a2}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{4})$
	D_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4})$	S_{a3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_b}{4})$
	D_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4})$	S_{a4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4})$
	D_{a5}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4})$	D_{a6}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_b}{4})$
Phase b	S_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{4})$	D_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{4})$
	S_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{4})$	D_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{4})$
	D_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{4})$	S_{b3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4}+\frac{T_a}{4})$
	D_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{4})$	S_{b4}	$\frac{2}{Ts}\times(\frac{T_0}{4})$
	D_{b5}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$	D_{b6}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$
Phase c	S_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{4})$	D_{c1}	$\frac{2}{Ts}\times(\frac{T_0}{4})$
	S_{c2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{4})$	D_{c2}	$\frac{2}{Ts}\times(\frac{T_0}{4})$
	D_{c3}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4}+\frac{T_a}{4})$	S_{c3}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_0}{4})$
	D_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4}+\frac{T_a}{4})$	S_{c4}	$\frac{2}{Ts}\times(\frac{T_0}{4}+\frac{T_b}{4}+\frac{T_a}{4})$
	D_{c5}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$	D_{c6}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$

3.2.3.4. CONDUCTION DUTY CYCLE FOR "O3" SPACE VECTOR MODULATION (SVM) TECHNIQUE

In Normal SVM method, all 7 state vectors in Triangle 1 are used in the state sequence. But in the second modified SVM (O3), two of the zero state vectors, "-1-1-1" and "111" are eliminated and replaced by the zero state vector, "000". Therefore, the time assigned to each state vector will be different from that in Normal SVM method. The state sequences of the Triangle 1 in Sectors 1 and 2 for O3 SVM method is presented in Table 3.18.

Table 3. 18: State sequences in Triangle 1, Sectors 1 and 2 (O3 SVM)

Sector	Triangle	Switching States Sequence
1	***1***	0-1-1 , 00-1 , 000 , 100 , 110
2	***1***	-10-1 , 00-1 , 000 , 010 , 110

The state sequence and time assigned to each state vector in Triangle 1, Sector 1 for O3 SVM method is shown in Table 3.19.

Table 3. 19: State vectors and Related Switches and Diodes in Triangle 1, Sector 1 (O3 SVM)

Triangle 1		*a* ($T_a/4$)	*b* ($T_b/4$)	*Zero*($T_0/2$)	*a* ($T_a/4$)	*b* ($T_b/4$)
		0-1-1	00-1	000	100	110
Phase a	I>0	D_5 , S_2			S_1 , S_2	
	I<0	D_6 , S_3			D_1 , D_2	
Phase b	I>0	D_3 , D_4	D_5 , S_2			S_1 , S_2
	I<0	S_3, S_4	D_6 , S_3			D_1 , D_2
Phase c	I>0	D_3 , D_4		D_5 , S_2		
	I<0	S_3, S_4		D_6 , S_3		

According to Table 3.19, it can be deduced that by eliminating the state vectors "-1-1-1" and "111", the total time for zero state vectors is allocated to the only remained zero state vector, "000". Since the zero state vectors are common for the first triangle in all sectors, the time division for zero state vectors in other sectors is similar to that of Sector 1. All properties of this method are similar to those of Normal SVM except the state sequence and time division.

Table 3.20 shows the expressions that should be used for calculating the conduction duty cycle for the switches and diodes of all three phases when the reference voltage vector lies in Triangle 1 Sector 1.

Table 3. 20: Conduction duty cycle for devices in Triangle 1, Sector 1 (O3 SVM)

Current	***I > 0***		***I < 0***	
Phase	***Switch***	***Conduction duty Cycle***	***Switch***	***Conduction duty Cycle***
Phase a	S_{a1}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$	D_{a1}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$
	S_{a2}	$\frac{2}{Ts} \times (\frac{Ts}{2}) = 1$	D_{a2}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$
	D_{a3}	0	S_{a3}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4} + \frac{T_0}{2})$
	D_{a4}	0	S_{a4}	0
	D_{a5}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4} + \frac{T_0}{2})$	D_{a6}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4} + \frac{T_0}{2})$
Phase b	S_{b1}	$\frac{2}{Ts} \times (\frac{T_b}{4})$	D_{b1}	$\frac{2}{Ts} \times (\frac{T_b}{4})$
	S_{b2}	$\frac{2}{Ts} \times (\frac{Ts}{2} - \frac{T_a}{4})$	D_{b2}	$\frac{2}{Ts} \times (\frac{T_b}{4})$
	D_{b3}	$\frac{2}{Ts} \times (\frac{T_a}{4})$	S_{b3}	$\frac{2}{Ts} \times (\frac{Ts}{2} - \frac{T_b}{4})$
	D_{b4}	$\frac{2}{Ts} \times (\frac{T_a}{4})$	S_{b4}	$\frac{2}{Ts} \times (\frac{T_a}{4})$
	D_{b5}	$\frac{2}{Ts} \times (\frac{T_b}{4} + \frac{T_0}{2} + \frac{T_a}{4})$	D_{b6}	$\frac{2}{Ts} \times (\frac{T_b}{4} + \frac{T_0}{2} + \frac{T_a}{4})$
Phase c	S_{c1}	0	D_{c1}	0
	S_{c2}	$\frac{2}{Ts} \times (\frac{T_0}{2} + \frac{T_a}{4} + \frac{T_b}{4})$	D_{c2}	0
	D_{c3}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$	S_{c3}	$\frac{2}{Ts} \times (\frac{Ts}{2}) = 1$
	D_{c4}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$	S_{c4}	$\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$
	D_{c5}	$\frac{2}{Ts} \times (\frac{T_0}{2} + \frac{T_a}{4} + \frac{T_b}{4})$	D_{c6}	$\frac{2}{Ts} \times (\frac{T_0}{2} + \frac{T_a}{4} + \frac{T_b}{4})$

Along with the expressions in Table 3.10 and Table 3.20, the conduction duty cycle of outer switch, S1 is $\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4} + \frac{T_0}{8})$ and $\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$ for Normal and O2 SVM methods respectively. In addition, for other outer switch, S4, the conduction duty cycle in Normal SVM is $\frac{2}{Ts} \times (\frac{T_0}{8})$ and in O2 SVM is 0 . It indicates that O3 SVM strategy is an appropriate method to reduce the conduction duty cycle of outer switches.

Table 3.21 and Table 3.22 bring the same information for Sector 2 that Table 3.19 and Table 3.20 presented for Sector 1.

Table 3. 21: State vectors and Related Switches and Diodes in Triangle 1, Sector 2 (O3 SVM)

Triangle 1		*b* (T_b/4)	*a* (T_a/4)	*Zero*(T_0/2)	*b* (T_b/4)	*a* (T_a/4)
		-10-1	00-1	000	010	110
Phase a	I>0	D_3 , D_4	D_5 , S_2			S_1 , S_2
	I<0	S_3 , S_4	D_6 , S_3			D_1 , D_2
Phase b	I>0	D_5 , S_2			S_1 , S_2	
	I<0	D_6 , S_3			D_1 , D_2	
Phase c	I>0	D_3 , D_4		D_5 , S_2		
	I<0	S_3 , S_4		D_6 , S_3		

Table 3. 22: Conduction duty cycle for devices in Triangle 1, Sector 2 (O3 SVM)

Current	***I > 0***		***I < 0***	
Phase	***Switch***	***Conduction duty Cycle***	***Switch***	***Conduction duty Cycle***
Phase a	S_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4})$	D_{a1}	$\frac{2}{Ts}\times(\frac{T_a}{4})$
	S_{a2}	$\frac{2}{Ts}\times(\frac{Ts}{2}-\frac{T_b}{4})$	D_{a2}	$\frac{2}{Ts}\times(\frac{T_a}{4})$
	D_{a3}	$\frac{2}{Ts}\times(\frac{T_b}{4})$	S_{a3}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{2}+\frac{T_b}{4})$
	D_{a4}	$\frac{2}{Ts}\times(\frac{T_b}{4})$	S_{a4}	$\frac{2}{Ts}\times(\frac{T_b}{4})$
	D_{a5}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{2}+\frac{T_b}{4})$	D_{a6}	$\frac{2}{Ts}\times(\frac{T_a}{4}+\frac{T_0}{2}+\frac{T_b}{4})$
Phase b	S_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$	D_{b1}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$
	S_{b2}	$\frac{2}{Ts}\times(\frac{Ts}{2})=1$	D_{b2}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$
	D_{b3}	0	S_{b3}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{2})$
	D_{b4}	0	S_{b4}	0
	D_{b5}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{2})$	D_{b6}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4}+\frac{T_0}{2})$
Phase c	S_{c1}	0	D_{c1}	0
	S_{c2}	$\frac{2}{Ts}\times(\frac{T_0}{2}+\frac{T_b}{4}+\frac{T_a}{4})$	D_{c2}	0
	D_{c3}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$	S_{c3}	$\frac{2}{Ts}\times(\frac{Ts}{2})=1$
	D_{c4}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$	S_{c4}	$\frac{2}{Ts}\times(\frac{T_b}{4}+\frac{T_a}{4})$
	D_{c5}	$\frac{2}{Ts}\times(\frac{T_0}{2}+\frac{T_b}{4}+\frac{T_a}{4})$	D_{c6}	$\frac{2}{Ts}\times(\frac{T_0}{2}+\frac{T_b}{4}+\frac{T_a}{4})$

3.3. CONCLUSION

In this Chapter, the expressions regarding the “conduction duty cycle” of switches and diodes have been computed. These expressions present a close relation with the “conduction losses”. Therefore, one should be able to better assess the impact of different modulation techniques on the conduction losses and junction temperatures by observing “conduction duty cycle” index.

CHAPTER 4: CONDUCTION DUTY CYCLE OF SEMICONDUCTORS IN NEUTRAL-POINT CLAMPED (NPC) THREE-LEVEL INVERTER

4.1. INTRODUCTION

This Chapter is focused on the determination of the conduction duty cycle of switches and diodes of a three-level three-phase NPC inverter, with the three SVM methods mentioned in the previous Chapter. The objective is to identify which one is more effective in providing the desired shift of conduction losses, required for reducing the power dissipation and junction temperatures in key components. The impact of the modulation index and also of the power factor will be considered in this study. Since the devices in three phases have similar duty cycles, the plots have been obtained for only phase "A". For the other phases there is a 120^{o} phase shift between the plots.

4.2. ENABLED DUTY CYCLE VERSUS CONDUCTION DUTY CYCLE FOR NORMAL SPACE VECTOR MODULATION (SVM) METHOD

As mentioned in section 3.2.3, the "enabled duty cycle" of all semiconductors of the converter operating with a given SVM method can be calculated from the magnitude of the reference voltage vector. The "conduction duty cycle" requires the knowledge of the power factor. In the following sections, since the inverter is expected to operate in a symmetrical way, instead of presenting the results of all 4 switches and 4 diodes of all phases, only the results concerning S_1 and S_2, outer and inner switches, D_1 and D_2, outer and inner anti-parallel diodes as well as D_5, a clamping diode, of phase A are presented.

The values of the conduction duty cycle will be plotted versus the angle of the reference voltage vector (θ) since this is a common parameter to all SVM methods. The goal is to compare the maximum and the average values of conduction duty cycle of the semiconductors obtained with the three SVM methods.

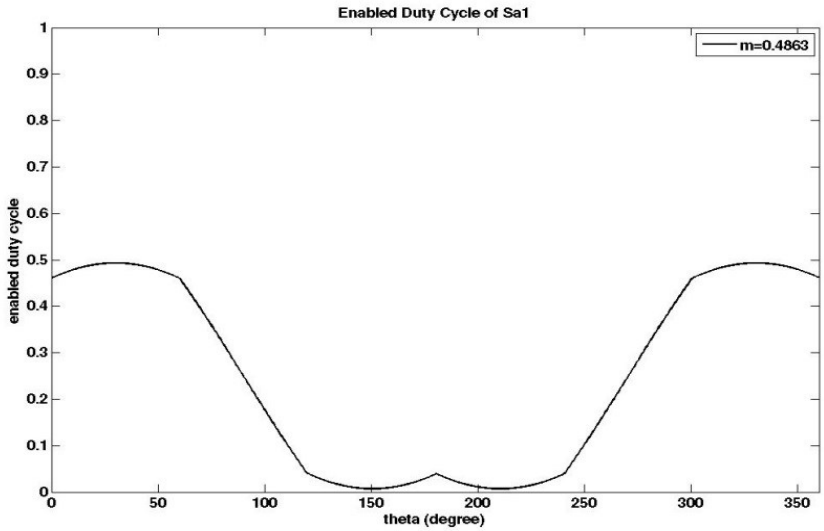
These plots have been drawn by using the expressions in Chapter 3. For instance, according to Table 3.10, the conduction duty cycle of the outer switch, S_{A1} in Normal SVM strategy is $(2/Ts)\times(T_a/4 + T_b/4 + T_0/8)$. This expression is for Sector 1 that is the first 60º. For the second 60º which is Sector 2, the expression for conduction duty cycle is $(2/Ts)\times(T_a/4 + T_0/8)$ considering Table 3.12. The same procedure should be done for corresponding switches in phases *B* and *C*. Afterwards, for the second and third 120º segments of S_1 in the three phases, the rules presented in Table 3.6 should be implemented; that is, the conduction duty cycle of S_{A1} in the second 120º segment is equal to the conduction duty cycle of S_{C1} in the first 120º. To draw the following plots for the conduction duty cycle of the devices, the expressions have been implemented in *MATLAB/M-File* for the three phases.

4.2.1. PLOT ANALYSIS FOR OUTER SWITCH AND ITS ANTI-PARALLEL DIODE

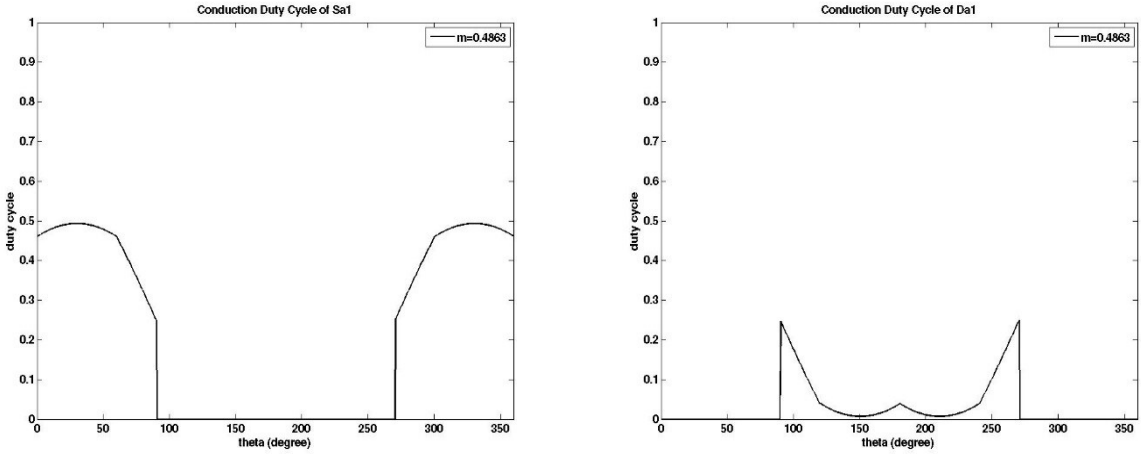
In order to demonstrate the separate parts of the plots clearly, the following plots have been obtained for unity power factor (φ = 0º) and modulation index (m) = 0.4863. The approach of the relation between the plots of the conduction duty cycle and enabled duty cycle can be generalized for other values of power factor and modulation index. In addition, for other devices, the power factor and

modulation index are unity and 0.4863 respectively. The modulation method is Normal SVM method but the principal of the plots are the same for other modulation methods, O2 and O3 SVM.

According to Figure 4.1, the enabled duty cycle of S_{A1}, (Figure 4.1 a) is exactly comprising the conducting duty cycle of S_{A1} (Figure 4.1 b) and its anti-parallel diode, D_1, (Figure 4.1 c). From 0^o to 90^o and 270^o to 360^o, the enabled duty cycle of the switch is equal to the conduction duty cycle of the switch; that is, during this period, the output current is in the direction of the switch. Therefore, the outer switch is conducting the current. From 90^o to 270^o, although the switch is enabled with a varying duty cycle, the anti-parallel diode conducts the current. So, the conduction duty cycle of the anti-parallel diode is identical to the enabled duty cycle of the outer switch.



(a)

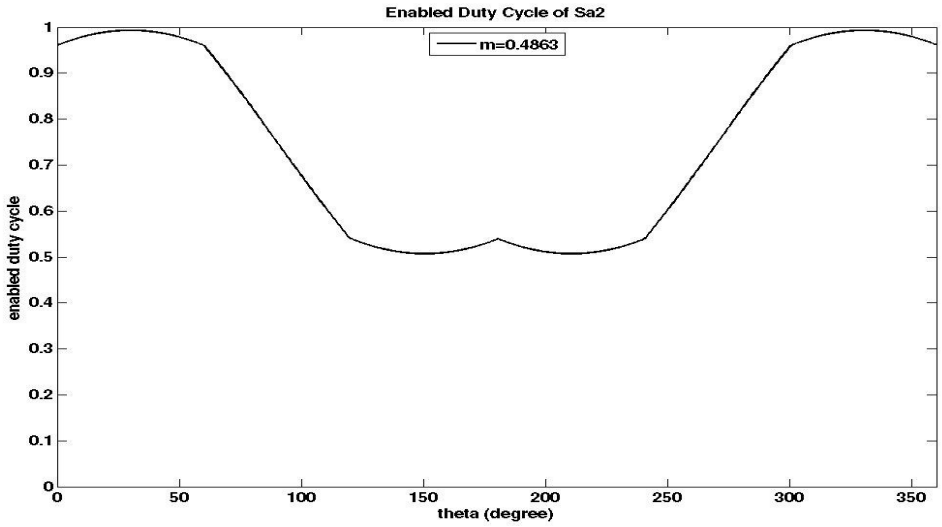


(b) (c)

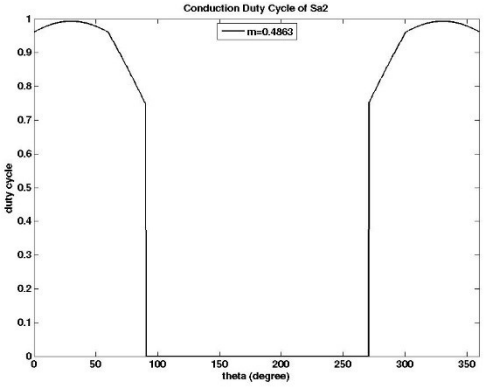
Figure 4. 1: Duty cycle of S1;
(a): enabled duty cycle of S1, (b): conduction duty cycle of S1, (c): conduction duty cycle of D1

4.2.2. PLOT ANALYSIS FOR INNER SWITCH, ITS ANTI-PARALLEL DIODE AND CLAMPING DIODE

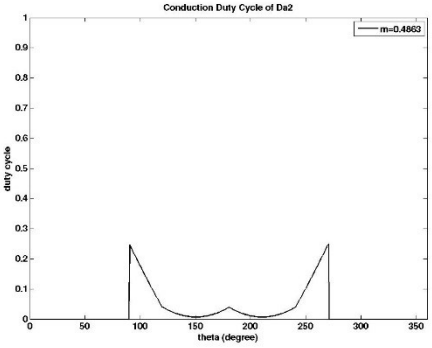
According to Figure 4.2, the enabled duty cycle of S_2, (Figure 4.2 a) consists of two parts; the conducting duty cycle of S_2 (Figure 4.2 b) and the anti-parallel diode, D_2 (Figure 4.2 ac). In two periods of 0^o to 90^o and 270^o to 360^o, the conduction duty cycle of the switch is identical to its enabled duty cycle because the inner switch is conducting the current. From 90^o to 270^o, the anti- parallel and clamping diodes conduct the negative current. When the inner switch is operating for zero state vectors, the clamping diode is also conducting the current. Therefore, the conduction duty cycle of inner switch is the enabled duty cycle for 0^o to 90^o and 270^o to 360^o and conduction duty cycle of the diode is the enabled duty cycle for 90^o to 270^o.



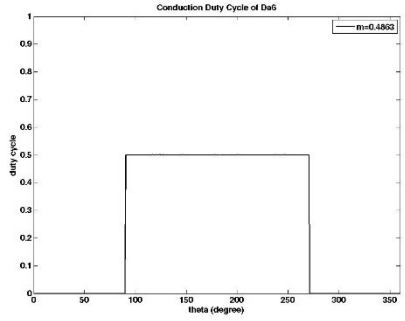
(a)



(b)



(c)

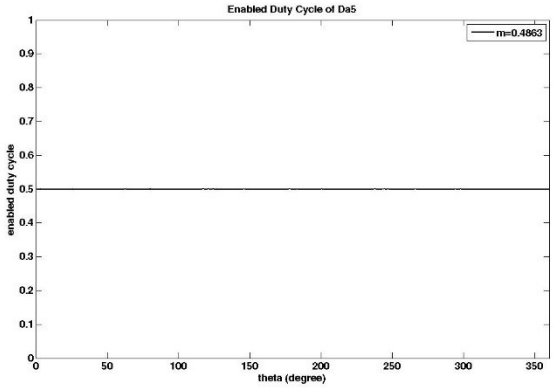


(d)

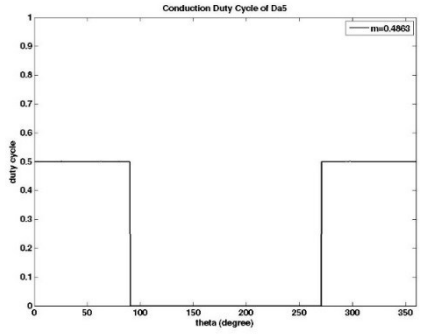
Figure 4. 2: Duty cycle of S2; (a): enabled duty cycle of S2, (b): conduction duty cycle of S2, (c): conduction duty cycle of D2, (d): conduction duty cycle of D6

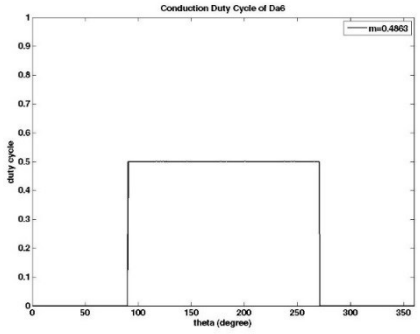
4.2.3. PLOT ANALYSIS FOR CLAMPING DIODES

As stated in Table 3.10, the conduction duty cycle of D_{A5} is equal to that of D_{A6} which is $(2/Ts) \times (T_a/4 + T_b/4 + 2 \times T_0/8)$. Therefore, the conduction duty cycle of clamping diodes is 0.5. However, the clamping diodes do not conduct simultaneously. When the output current is positive, D_{A5} conducts the current, otherwise for negative current, D_{A6} conducts. In addition, according to Figure 4.3, the enabled duty cycle of D_{A5} is comprising the conducting duty cycle of D_{A5} and D_{A6}. It can be deduced that when D_{A5} is enabled, either D_{A5} or D_{A6} conducts depending on the current polarity.



(a)





(b) (c)

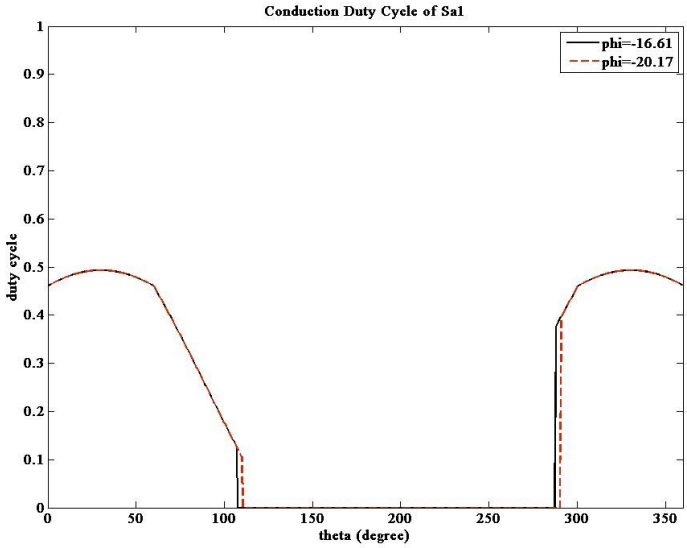
Figure 4. 3: Duty cycle of D_{A5}; (a): enabled duty cycle of D_{A5}, (b): conduction duty cycle of D_{A5}, (c): conduction duty cycle of D_{A6}

4.3. INFLUENCE OF LOAD ANGLE ON CONDUCTION DUTY CYCLE OF DEVICES

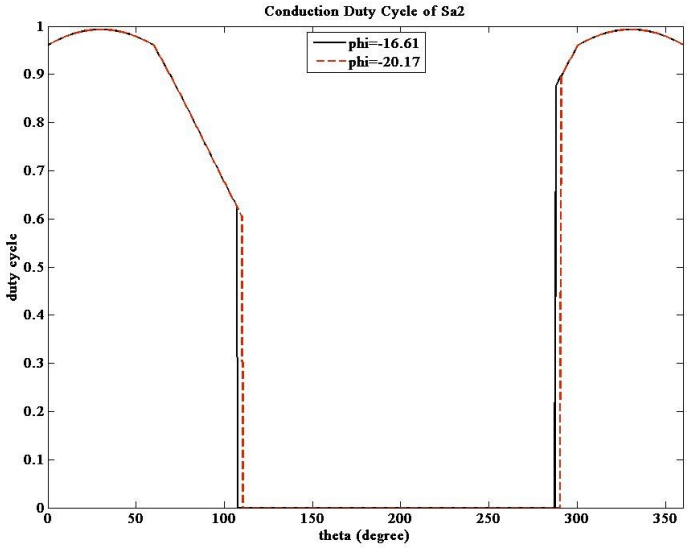
The plots of conduction duty cycle for two different load angles have been obtained from *MATLAB/M-File*. The load angles selected from Table 2.2 are -16.61^{o} and -20.17^{o} and the modulation index is "0.4863". The following plots are regarding upper devices in phase "*A*"; outer switch, inner switch, outer anti-parallel diode, inner anti-parallel diode and clamping diode. The lower devices are complementary with upper devices. Since the mean value is actually calculated by adding all values together and then averaging them, to have better comparison, the average value of conduction duty cycles of upper devices in one leg have been presented.

4.3.1. CONDUCTION DUTY CYCLE FOR "NORMAL" SVM

The plots of conduction duty cycle are shown in Figures 4.4-4.6 for Normal SVM method. Furthermore, the average value of conduction duty cycles of upper devices in one leg (phase *A*) have been calculated and presented in Table 4.1. All the explanations are relevant to upper devices ant it can be generalized for corresponding switches.



(a)



(b)

Figure 4. 4: Duty cycle of switches in phase A (Normal SVM); (a): Conduction duty cycle of outer switch (S_{A1}), (b): Conduction duty cycle of inner switch (S_{A2})

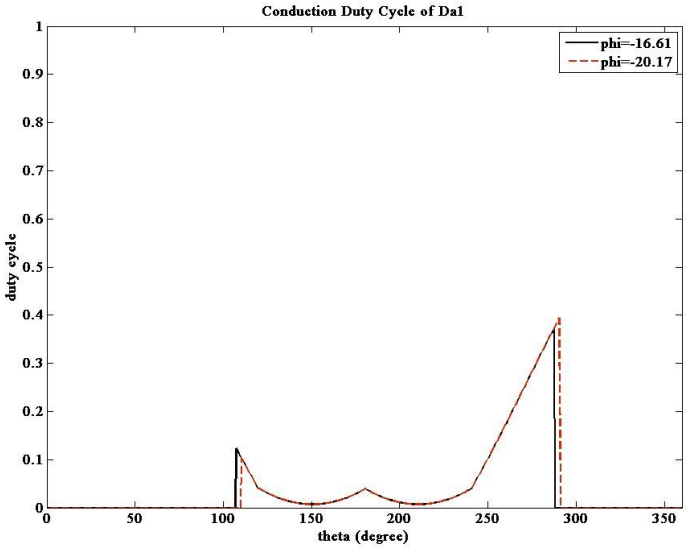
According to Figure 4.4, as the load angle increases, the conduction duty cycle of outer and inner switches is shifting on the horizontal axis and make the plot wider in the first segment, where the magnitude is “lower” and narrower in the second segment, where the magnitude is “higher.” Therefore, the average value of the conduction duty cycle is decreased as the load angle is increased. In addition, the shape of the conduction duty cycle for inner and outer switch is similar but they have different magnitudes. When the state vector is “1” for a phase, both inner and outer switches are conducting and when the state vector is “0”, only the inner switch is conducting. Therefore, when the current is in accordance with the switch direction, the inner switch has higher conduction duty cycle than the outer switch. Accordingly, there is a difference in magnitudes (0.5) in the plot of outer and inner switches. For the lower switches in one leg, the plot of conduction duty cycle will be with a 180^{o} phase shift.

As indicated in Figure 4.5, for the anti-parallel diodes, as the load angle increases, the plot of the conduction duty cycle includes higher values in the right section. Hence, the conduction duty cycle is increased. Furthermore, both inner and outer anti-parallel diodes have similar conduction duty cycle.

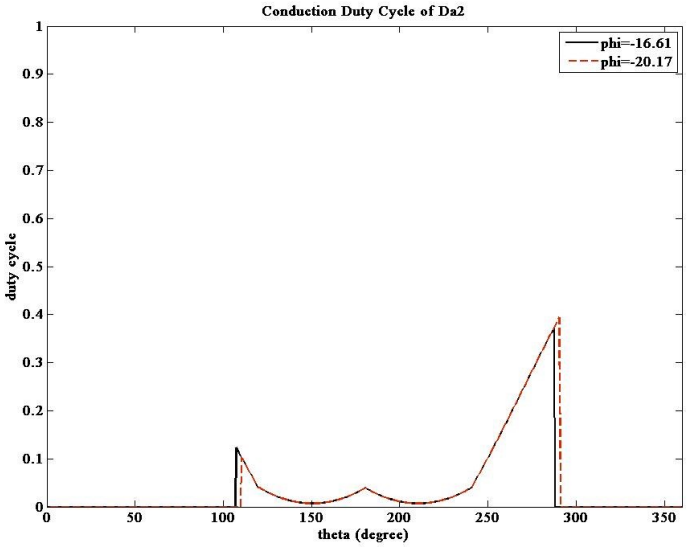
This similarity indicates that the outer and inner switches conduct the output current for the equal period of time. In Tables 3.10 and 3.11 also, the conduction duty cycle for inner and outer anti-parallel diodes is identical. The conduction duty cycle of the upper clamping diode has been shown in Figure 4.6. According to this figure, as the load angle gets larger, the plot relocates on

the horizontal axis but the amount is constant. So, the load angle does not have any impact on the conduction duty cycle of the clamping diode.

In addition, according to Table 3.10, the conduction time for a clamping diode is equal to half of the SVM sampling time, ($T_a/4 + T_b/4 + 2 \times T_0/8 = Ts/2$) and the duty cycle is 0.5 ($\frac{2}{Ts} \times (\frac{Ts}{2}) = \frac{1}{2}$).



(a)



(b)

Figure 4. 5; Duty cycle of anti-parallel diodes in phase A (Normal SVM); (a): Conduction duty cycle of outer diode (D_{A1}), (b): Conduction duty cycle of inner diode (D_{A2})

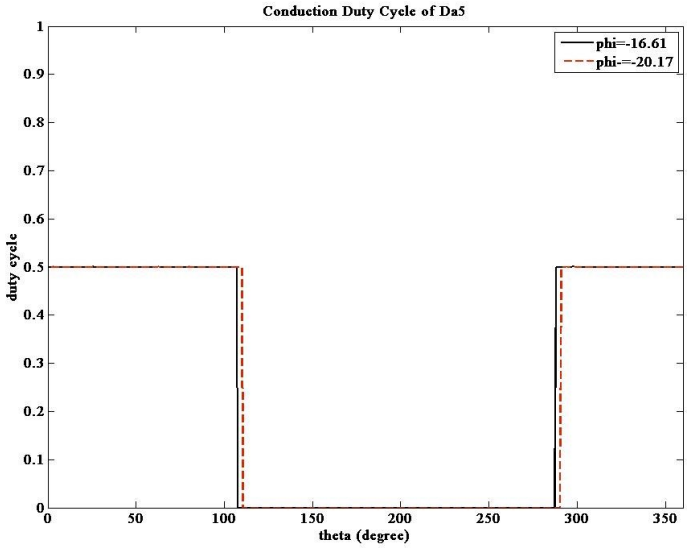


Figure 4. 6: Conduction duty cycle of upper clamping diode (D_{A5}) in phase A (Normal SVM)

Table 4. 1: Average duty cycle of upper devices in phase A for two load angles (Normal SVM)

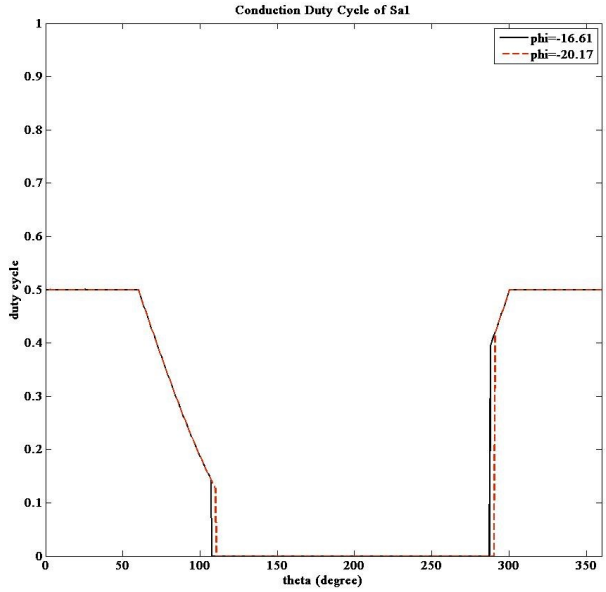
Devices		***Phase A***	
		m=0.4863	
		φ =-16.61º	***φ =-20.17º***
Switches	***S_1***	0.2140	0.2118
	S_2	0.4637	0.4614
Anti-parallel diodes	***D_1***	0.0357	0.0379
	D_2	0.0357	0.0379
Clamping diodes	***D_5***	0.2497	0.2497

According to Table 4.1, the following statements can be deduced:

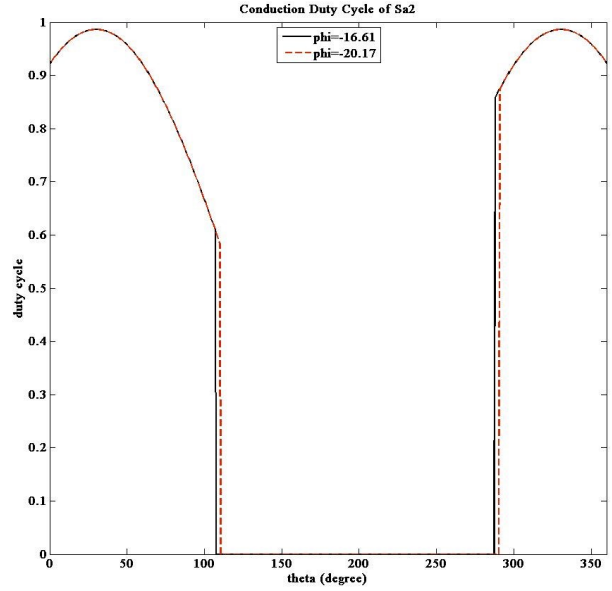
1- As the load angle increases (the power factor decreases), the average conduction duty cycle of switches is decreasing. According to Figure 4.4 with **φ = -20.17°**, the switch will be conducting in a segment with lower conduction duty cycle than that with **φ = -16.61°.** Therefore, the switches will be less stressed in terms of conduction losses.
2- When the power factor is reduced, the average duty cycle of anti-parallel diodes gets larger. So, the conduction duty cycle of diodes will be increasing.
3- The clamping diode has constant average duty cycle. Also, as shown in Figure 4.6, the duty cycle plot is constant. Therefore, as the load angle changes, there will be no change in duty cycle of clamping diode.

4.3.2. CONDUCTION DUTY CYCLE FOR "O2" SVM

The plots of conduction duty cycle are shown in Figures 4.7-4.9 for O2 SVM method. Moreover, the average value of conduction duty cycle of upper devices in one leg (phase *A*) is presented in Table 4.2.



(a)



(b)

Figure 4. 7: Duty cycle of switches in phase A (O2 SVM); (a): Conduction duty cycle of outer switch (S_{A1}), (b): Conduction duty cycle of inner switch (S_{A2})

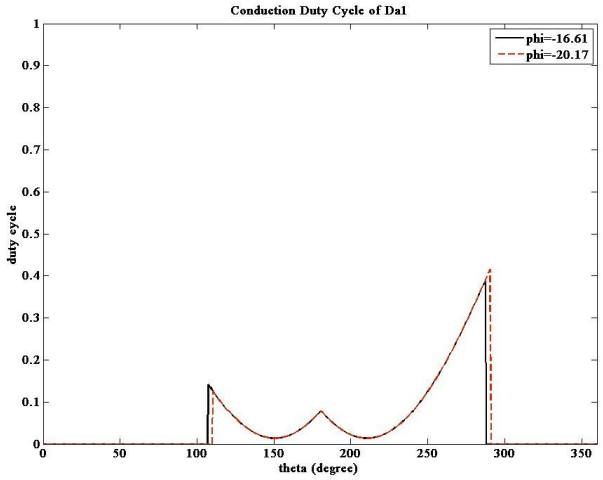
According to Figure 4.7, as the load angle increases, the switches will be operating more in a segment with lower value. So, the conduction duty cycle of switches has reduced. Furthermore, the shape of conduction duty cycle for outer switch is different to the correspondence plot for Normal SVM (Figure 4.4.(a)). As indicated in Table 3.10, the duty cycle of outer switch (S1) in Normal SVM is $2/Ts \times (T_a/4 + T_b/4 + T_0/8)$ and according to Table 3.15, in O2 SVM is $2/Ts \times (T_a/4 + T_b/4 + T_0/4)$. It is obvious that in O2 SVM, the duty cycle of the outer switch is 0.5 which is constant for 0^o to 60^o that is Sector 1, as seen in Figure 4.7.(a). It seems that by using O2 SVM method, the usage of the outer switch is increasing.

For the inner switch, in Figure 4.7. (b), the curve of the plot has a larger slope in O2 SVM than in Normal SVM (Figure 4.4.(b)). Therefore, the inner switch is conducting less in O2 SVM than in Normal SVM due to elimination of the state vector "000".

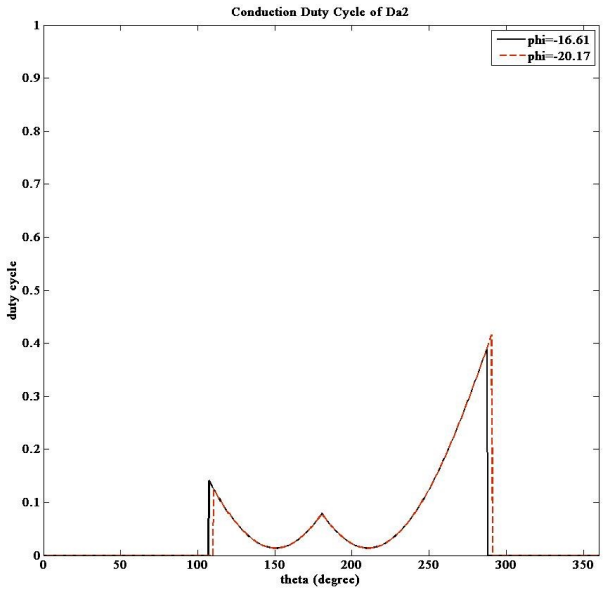
As indicated in Figure 4.8, for the anti-parallel diodes, as the load angle increases, they are operating more in the segment with higher duty cycle. So, the conduction duty cycle gets larger. In addition, the inner and outer anti-parallel diodes have identical conduction duty cycle. This similarity illustrates that the outer and inner switches conduct the output current for the equal period of time. Even in Tables 3.15 and 3.17, the anti-parallel diodes have the same conduction duty cycle.

The conduction duty cycle of the upper clamping diode has been depicted in Figure 4.9. Conforming to this figure, the shape of the plot has some convex curves which have not appeared in plot of Normal SVM. Due to the elimination of the state vector "000" and according to Table

3.15, there is no time regarding this state vector (T_0). So, the duty cycle does not have a constant value and it is smaller than the duty cycle in Normal SVM.



(a)



(b)

Figure 4. 8: Duty cycle of anti-parallel diodes in phase A (O2 SVM); (a): Conduction duty cycle of outer diode (D_{A1}), (b): Conduction duty cycle of inner diode (D_{A2})

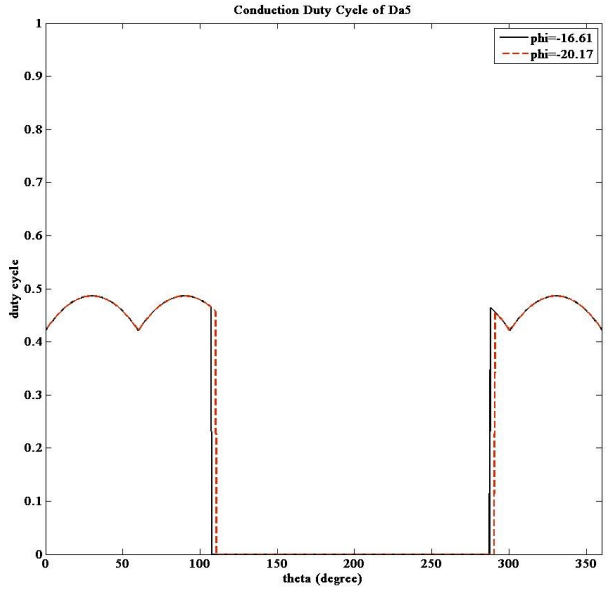


Figure 4. 9: Conduction duty cycle of clamping diode (D_{A5}) in phase A (O2 SVM)

Table 4. 2: Average duty cycle of upper devices in phase A for two load angles (O2 SVM)

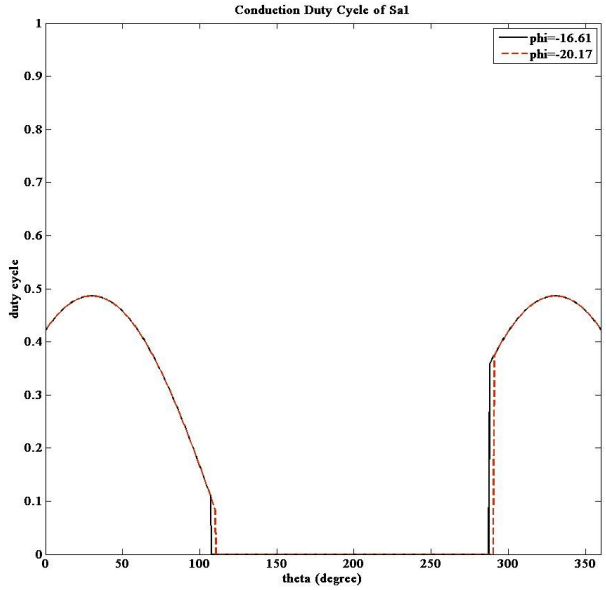
Devices		***Phase A***	
		m=0.4863	
		φ =-16.61º	***φ =-20.17º***
Switches	***S_1***	0.2229	0.2207
	S_2	0.4548	0.4525
Anti-parallel diodes	***D_1***	0.0446	0.0469
	D_2	0.0446	0.0469
Clamping diodes	***D_5***	0.2319	0.2319

As indicated in Table 4.2, the following statements can be deduced:

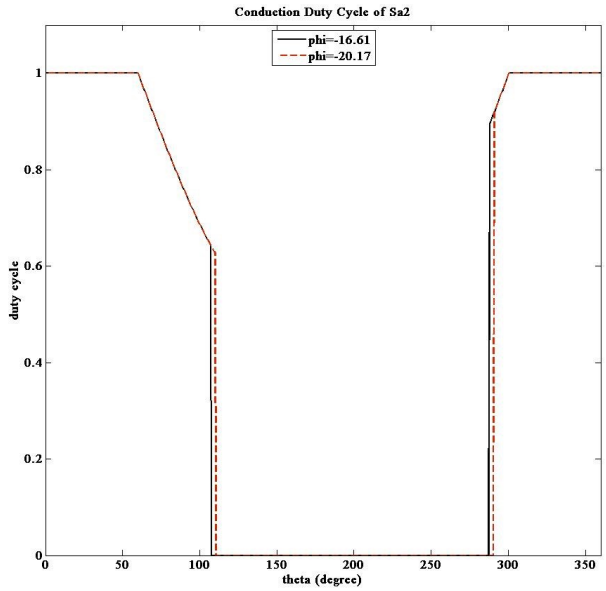
1- As the load angle is increasing, the average duty cycle of switches is decreasing. It can be said that the larger the load angle is, the less the switches are operating.
2- For each load angle, the average duty cycle of anti-parallel diodes are approximately similar. When the power factor is reduced, the average duty cycle of anti-parallel diodes gets larger. So, the conduction duration of the anti-parallel diodes will be increasing.
3- The average duty cycle for the clamping diode is constant. In addition, according to Figure 4.9, although the device conducts more in the first segment, it will be less conducting in the second segment. So, the average of the plot is constant. Hence, by varying the load angle, the average duty cycle of the clamping diodes is not changing.

4.3.3. CONDUCTION DUTY CYCLE FOR "O3" SVM

The plots of conduction duty cycle are depicted in Figures 4.10-4.12 for O3 SVM method. Furthermore, the average conduction duty cycle of upper devices in one leg (phase *A*) has been presented in Table 4.3.



(a)



(b)

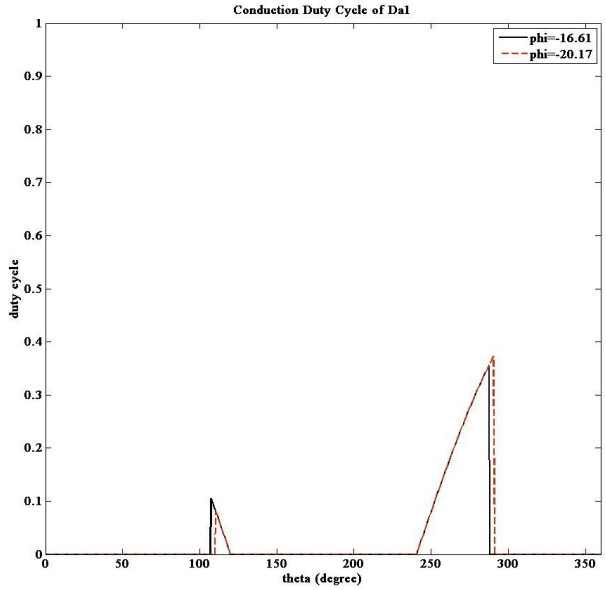
Figure 4. 10: Duty cycle of switches in phase A (O3 SVM); (a): Conduction duty cycle of outer switch (S_{A1}), (b): Conduction duty cycle of inner switch (S_{A2})

According to Figure 4.10, as the load angle increases, the switches will be operating more in a segment with lower value. So, the conduction duty cycle of switches has reduced. Furthermore, for outer switch, the curve of the plot in O3 SVM has larger slope than in Normal SVM (Figure 4.4. (a)). So, the outer switch in O3 SVM is conducting less than in Normal SVM, because in O3 SVM, two zero state vectors, "-1-1-1" and "111" have been eliminated.

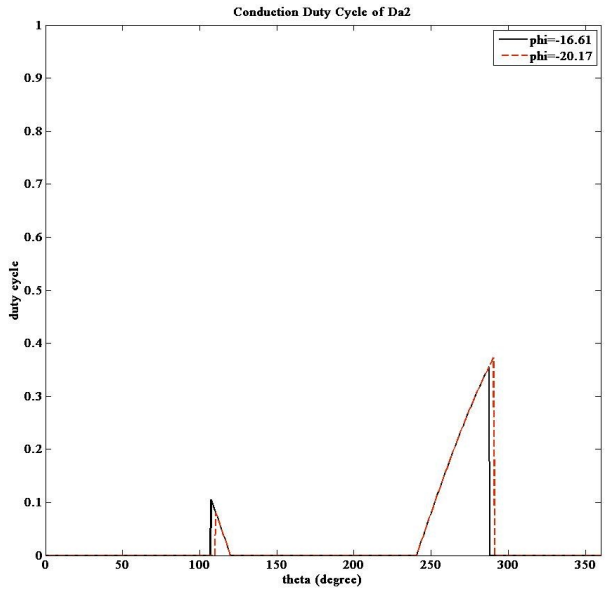
For inner switch, there is a flat part in the plot. As indicated in Table 3.10, the duty cycle of the inner switch (S_2) in Normal SVM is $2/Ts \times (Ts/2 - T_0/8)$ and as shown in Table 3.20, in O3 SVM is "1" for the first 60^o which is Sector 1, as seen in Figure 4.10. (b). Therefore, by using O3 SVM method, the usage of the inner switch is increasing.

As indicated in Figure 4.11, for the anti-parallel diodes, as the load angle increases, they are operating more in the segment with higher value of duty cycle. So, the conduction duty cycle gets larger. In addition, the inner and outer anti-parallel diodes have identical conduction duty cycle. This similarity illustrates that the outer and inner switches conduct the output current for the equal period of time.

Figure 4.12 illustrates the conduction duty cycle of upper clamping diode. Conforming to this figure, the shape of the plot has some concave curves which have not been exposed in plot of Normal SVM. In Normal SVM, the conduction duty cycle is constant at 0.5. In O2 SVM, it has some curves between 0.4 and 0.5 that indicates the decrement in the conduction. But in O3 SVM, the curves are varying between 0.5 and 0.6 that illustrates the increment in the conduction.



(a)



(b)

Figure 4. 11: Duty cycle of anti-parallel diodes in phase A (O3 SVM); (a): Conduction duty cycle of outer diode (D_{A1}), (b): Conduction duty cycle of inner diode (D_{A2})

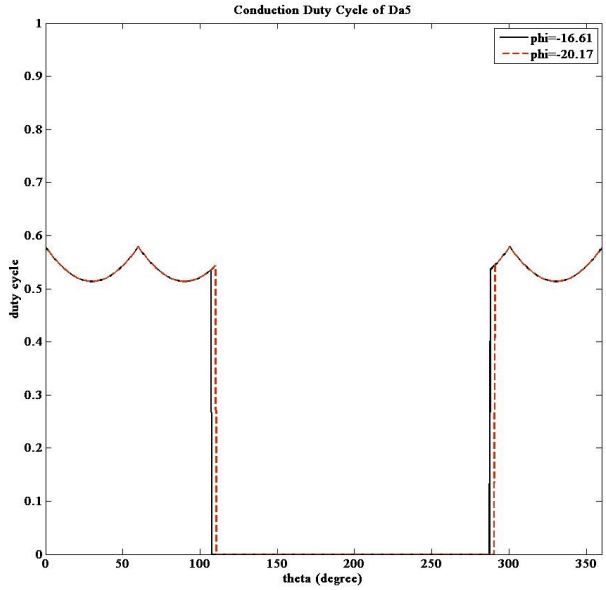


Figure 4. 12: Conduction duty cycle of clamping diode (D_{A5}) in phase A (O3 SVM)

Table 4. 3: Average duty cycle of upper devices in phase A for two load angles (O3 SVM)

Devices		***Phase A***	
		m=0.4863	
		φ =-16.61º	***φ =-20.17º***
Switches	***S_1***	0.2051	0.2029
	S_2	0.4726	0.4703
Anti-parallel diodes	***D_1***	0.0267	0.0290
	D_2	0.0267	0.0290
Clamping diodes	***D_5***	0.2674	0.2674

According to the results in Table 4.3, the following statements can be deduced for modulation index (m) = 0.4863:

1- As the load angle is increasing, the average duty cycle of switches is decreasing. It can be deduced that by increasing the load angle, the average conduction duty cycle of switches is reducing.
2- For each load angle, the average duty cycle of anti-parallel diodes are approximately similar. When the power factor is reduced, the average duty cycle of anti-parallel diodes gets larger. So, the conduction of anti-parallel diodes will be increasing.
3- For the clamping diode, the average duty cycle is constant. According to Figure 4.12, the duty cycle plot has some curves but the average of the plot is constant. Therefore, when the load angle is varying, the average duty cycle of the clamping diode remains constant.

4.3.4. COMPARISON OF THE METHODS

In order to better analyze the SVM methods, all the results concerning the average conduction duty cycles for different power factors are presented in Table 4.4.

Table 4. 4: Comparison of average duty cycle of upper devices obtained from all methods for two different load angles

Modulation index		***m=0.4863***					
Load angle		***φ =-16.61°***			***φ =-20.17°***		
Methods		***Normal***	***O2***	***O3***	***Normal***	***O2***	***O3***
Switches	S_1	0.2140	0.2229	0.2051	0.2118	0.2207	0.2029
	S_2	0.4637	0.4548	0.4726	0.4614	0.4525	0.4703
Anti-parallel diodes	D_1	0.0357	0.0446	0.0267	0.0379	0.0469	0.0290
	D_2	0.0357	0.0446	0.0267	0.0379	0.0469	0.0290
Clamping diodes	D_5	0.2497	0.2319	0.2674	0.2497	0.2319	0.2674

According to Table 4.4, the following statements can be obtained for ***m=0.4863***:

1- In Normal SVM, the inner switch, S2 has larger average conduction duty cycle than the outer switch, S1. By applying O2 SVM, the duty cycle of outer switch, S1 has been increased by about 4.2% and the duty cycle of inner switch, S2 has been decreased by about 1.9% for both load angles. It indicates that by applying O2 SVM, the conduction duty cycle for the inner switch has been reduced and for the outer switch, has been increased. Therefore, O2 SVM is helpful to reduce the conduction duty cycle of the outer switch which has larger duty cycle than inner switch for this particular value of modulation index and specific load angle.

2- By implementing O3 SVM, the conduction duty cycle of outer switch, S1 becomes less than that in Normal SVM and the duty cycle of inner switch, S2 becomes higher than that in Normal SVM. Hence, it can be deduced that for outer switch, S1, the conduction duty cycle can be reduced by 4.2% and for inner switch, S2, there will be an increment of about 1.9%. So, O3

SVM is useful to reduce the conduction duty cycle of outer switch for the modulation index (m) = 0.4863 and a specific load angle (either -16.61° or -20.17°).

3- According to the last two statements, O2 SVM has superiority over O3 SVM because with the help of O2 SVM, the switches that have higher conduction duty cycle in Normal SVM, will be relieved and the conduction duty cycle will be more balanced among the switches for *m=0.4863*.

4- As indicated in previous sections, in each SVM method, the clamping diodes have similar duty cycles for different load angles. So, the clamping diodes have identical behavior during conduction. If O2 SVM method is applied, the duty cycle of the clamping diode is getting smaller by about 7.13% and by using O3 SVM, it has an increment by about 7.09% for both load angles. It indicates that for the clamping diode, O2 SVM method is more efficient than O3 SVM method for *m=0.4863*.

5- For the load angle of *-16.61°*, by applying O2 SVM method, the conduction duty cycle of anti-parallel diodes has been increased by about 24.93% and with the help of O3 SVM method, the conduction duty cycle has been decreased by about 25.21%. Moreover, for the load angle of *-20.17°*, these percentages will be 23.75% of increment by O2 SVM and 23.48% decrement by O3 SVM for diodes. Therefore, for anti-parallel diodes, O3 SVM method is preferable to O2 SVM method because it helps the diodes to have less conduction losses.

The comparison of SVM methods is presented in Table 4.5. These comparisons are valid for two presented load angles.

Table 4. 5: Comparison of methods for duty cycle of upper devices in three-level inverter

Devices		***Comparison of methods***
Switches	S_1	O3 SVM < Normal SVM < O2 SVM
	S_2	O2 SVM < Normal SVM < O3 SVM
Anti-parallel diodes	D_1	O3 SVM < Normal SVM < O2 SVM
	D_2	O3 SVM < Normal SVM < O2 SVM
Clamping diodes	D_5	O2 SVM < Normal SVM < O3 SVM

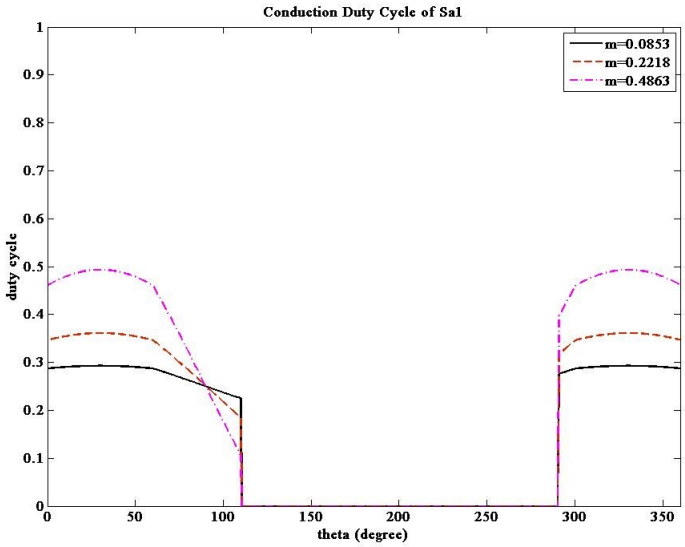
According to Table 4.5, O2 SVM is a favorable method for inner switches (S2 & S3) and clamping diodes because it helps to reduce the conduction duty cycles of these devices. On the other hand, the conduction duty cycle of outer switches (S1 & S4) and anti-parallel diodes is increased. Furthermore, O3 SVM is favorable for outer switches and anti-parallel diodes due to the decrement in their conduction duty cycle.

4.4. INFLUENCE OF MODULATION INDEX ON CONDUCTION DUTY CYCLE

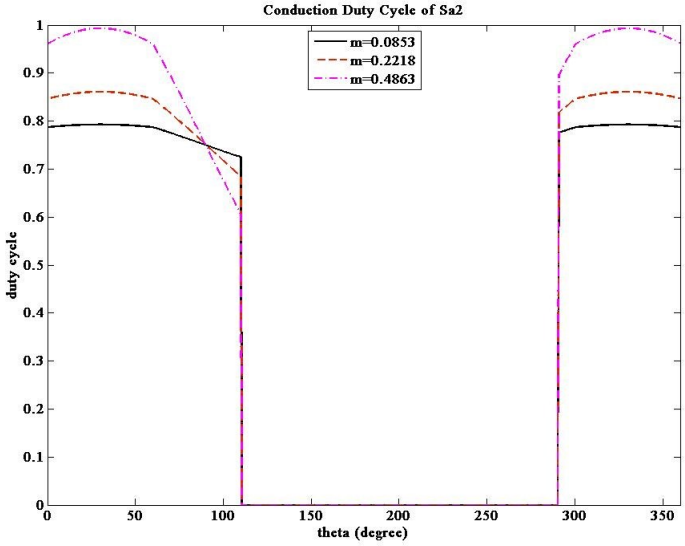
The plots of conduction duty cycle for three different modulation indices have been obtained from *MATLAB/M-File.* The modulation indices selected from Table 2.2 are 0.0853, 0.2218 and 0.4863 and the load angle is "-20.17º". The following plots are related to the upper devices in phase "*A*"; outer switch, inner switch, outer anti-parallel diode, inner anti-parallel diode and clamping diode. The lower devices are identical with upper devices. In addition, to have simply a basis for comparison, the average value of the conduction duty cycles of upper devices in one leg have been presented. Since the devices in the three phases have similar duty cycles, the plots have been obtained for only phase "*A*". For other phases there is a 120º phase shift between the plots.

4.4.1. CONDUCTION DUTY CYCLE FOR "NORMAL" SVM

The plots of conduction duty cycle are shown in Figures 4.13-4.15 for Normal SVM method. Furthermore, the average value of conduction duty cycles of upper devices in one leg (phase *A*) have been calculated and presented in Table 4.6.



(a)



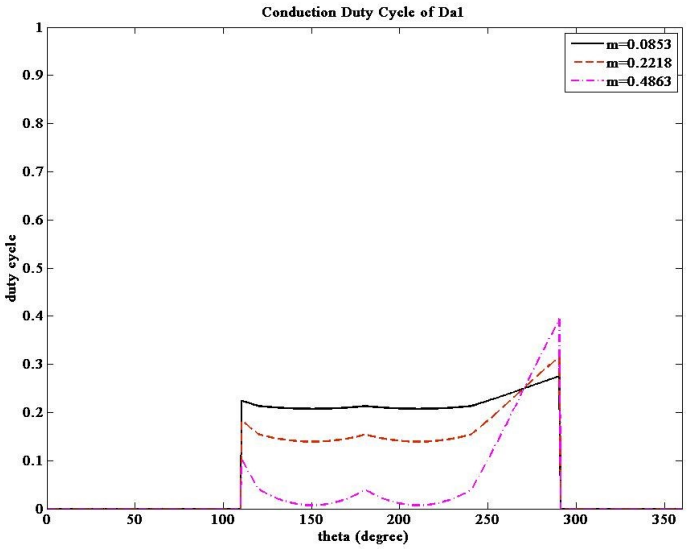
(b)

Figure 4. 13: Duty cycle of switches in phase A (Normal SVM); (a): Conduction duty cycle of outer switch (S_{A1}), (b): Conduction duty cycle of inner switch (S_{A2})

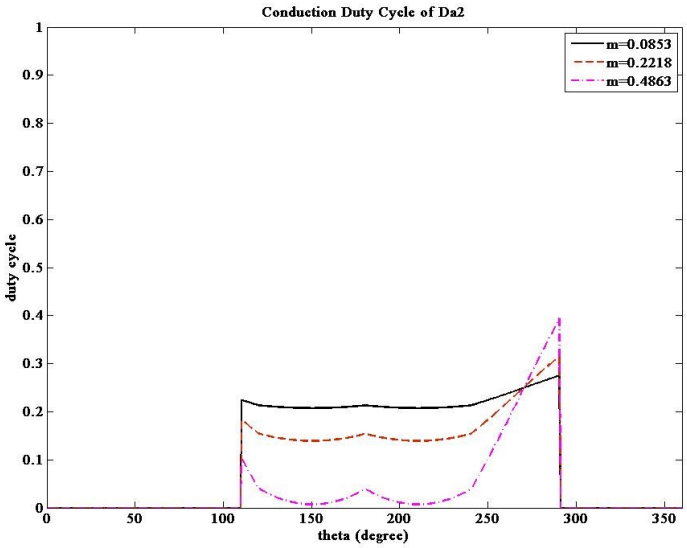
According to Figure 4.13, as the modulation index increases, the switches will be conducting more. So, the conduction duty cycle of outer and inner switches gets larger. In addition, the shape of the conduction duty cycle curves of the inner and of the outer switch for a specific modulation index are similar but there is a different magnitude in the plot of the inner switch which is 0.5. When the state vector is "1" for a phase, both inner and outer switches are conducting and when the state vector is "0", the inner switches are conducting. Therefore, when the current is in accordance with the switch direction, the inner switch has higher conduction duty cycle than the outer switch. Accordingly, there is a reduction in the magnitude in the plot of the inner switch.

According to Figure 4.14, as modulation index increases, the plot of conduction duty cycle will be including less area. Therefore, the conduction duty cycle of the anti-parallel diodes will be decreased. Furthermore, both inner and outer anti-parallel diodes have similar conduction duty cycle. This similarity indicates that the outer and inner switches conduct the output current for an equal period of time.

The conduction duty cycle of the upper clamping diode has been shown in Figure 4.15. According to this figure, the clamping diode has a constant value for conduction duty cycle. According to Table 3.10, the conduction time is equal to half of the SVM sampling time, Ts and the duty cycle is 0.5. In addition, since the load angle is constant, there is no magnitude difference for the plots. So, for different modulation indices, the plot of conduction duty cycle is unique. While the conduction duty cycle for upper clamping diode is zero, the lower clamping diode conducts the output current.



(a)



(b)

Figure 4. 14: Duty cycle of anti-parallel diodes in phase A (Normal SVM); (a): Conduction duty cycle of outer diode (D_{A1}), (b): Conduction duty cycle of inner diode (D_{A2})

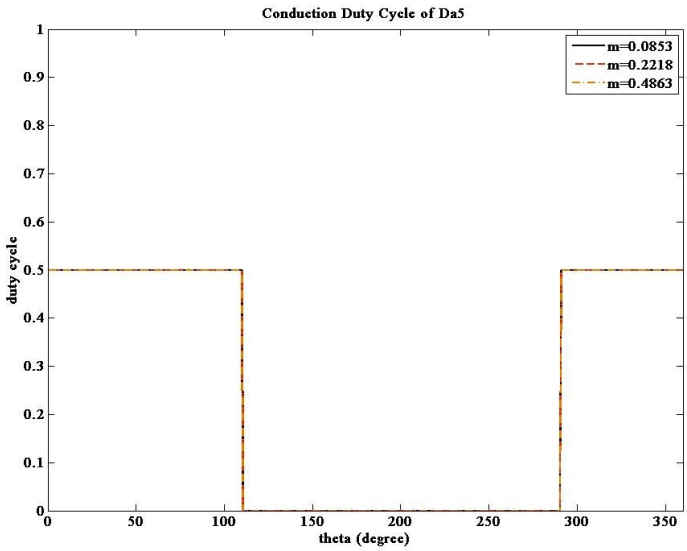


Figure 4. 15: Conduction duty cycle of clamping diode in phase A (Normal SVM)

Table 4. 6: Average duty cycle of upper devices in phase A for three modulation indices (Normal SVM)

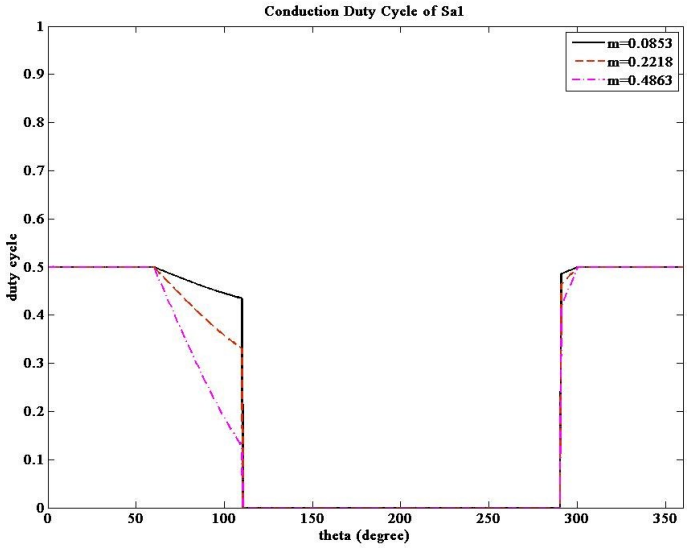
Devices		***Phase A***		
		φ =-20.17°		
		m=0.0853	***m=0.2218***	***m=0.4863***
Switches	S_1	0.1401	0.1645	0.2118
	S_2	0.3897	0.4141	0.4614
Anti-parallel diodes	D_1	0.1099	0.0854	0.0379
	D_2	0.1099	0.0854	0.0379
Clamping diodes	D_5	0.2497	0.2497	0.2497

According to Table 4.6, the following statements can be deduced for *φ =-20.17°*:

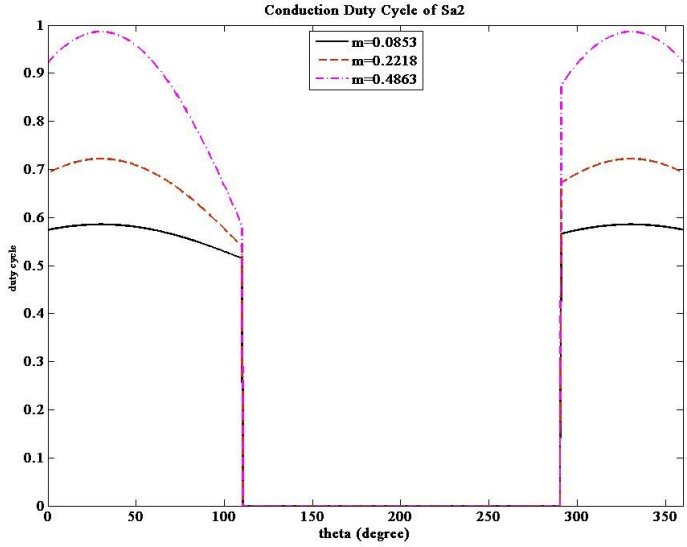
1- There is a correlation between modulation index and conduction duty cycle. For instance, in Sector 1, when the modulation index (m) gets larger from 0 to 0.5, the reference vector gets closer to the state vectors “0-1-1” and “100” in one side and “00-1” and “110” in the other side of Triangle 1. Therefore, the duration of using these state vectors for vector synthesizing augments and the conduction duty cycle of switches is increasing. Hence, the switches will be conducting more.
2- When the modulation index is increased, the average duty cycle of anti-parallel diodes is decreasing. So, the conduction of diodes will be reducing.
3- The clamping diodes have constant average duty cycle. Moreover, Figure 4.15 has shown that the duty cycle plot is constant. Therefore, by varying the modulation index, there will be no change in duty cycle of the clamping diodes.

4.4.2. CONDUCTION DUTY CYCLE FOR “O2” SVM

The plots of conduction duty cycle are shown in Figures 4.16-4.18 for O2 SVM method. In addition, the average value of conduction duty cycles of upper devices in one leg (phase *A*) have been calculated and presented in Table 4.7.



(a)



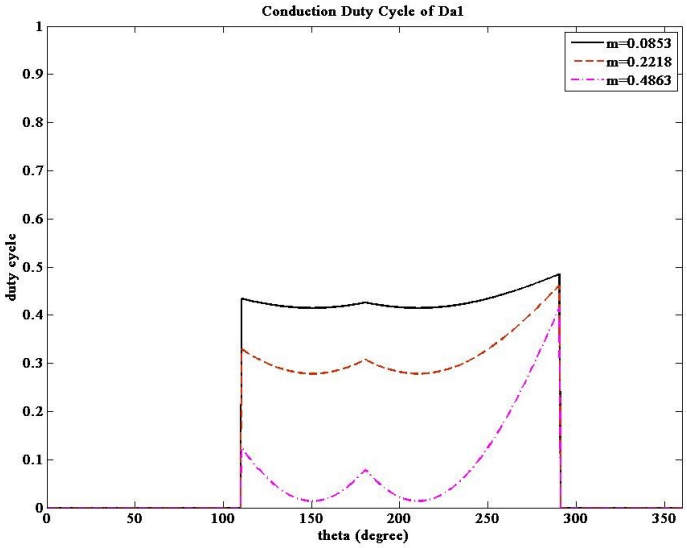
(b)

Figure 4. 16: Duty cycle of switches in phase A (O2 SVM); (a): Conduction duty cycle of outer switch (S_{A1}), (b): Conduction duty cycle of inner switch (S_{A2})

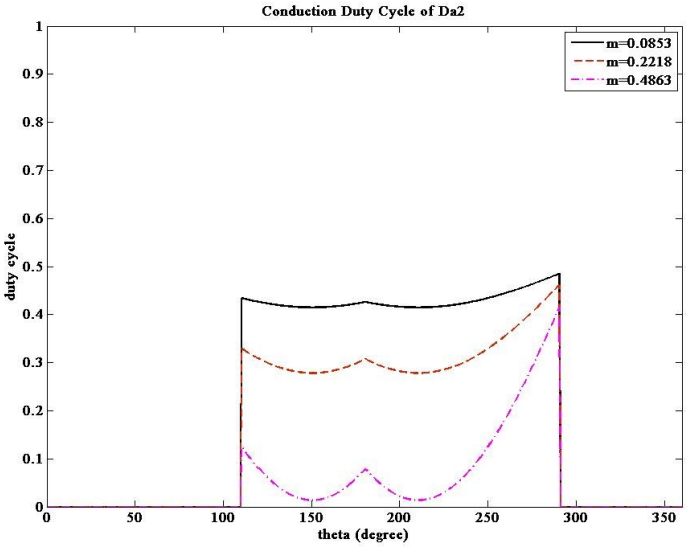
According to Figure 4.16, as the modulation index increases, the conduction duty cycle of the outer switch gets smaller and that of the inner switch gets larger. As mentioned in Table 3.15, the conduction duty cycle of S_{A1} in O2 SVM is $\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4} + \frac{T_0}{4}) = \frac{2}{Ts} \times (\frac{Ts}{4}) = \frac{2}{Ts} \times (\frac{Ts}{2} - \frac{Ts}{4})$ and of S_{A2} is $\frac{2}{Ts} \times (\frac{Ts}{2} - \frac{T_0}{4})$. It is obvious that $\frac{T_0}{4}$ is smaller than $\frac{Ts}{2}$. So, the conduction duty cycle of the inner switch increases while that of the outer switch decreases.

As indicated in Figure 4.17, the inner and outer anti-parallel diodes have identical conduction duty cycle that illustrates the outer and inner anti-parallel diodes conduct the output current for an equal period of time.

The conduction duty cycle of the upper clamping diode has been depicted in Figure 4.18. Conforming to this figure, the shape of the plot has some convex curves which have not appeared in plots of Normal SVM. Due to elimination of the state vector “000” and according to Table 3.15, there is no time (T_0) regarding this state vector ($\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$). So, the duty cycle does not have a constant value.



(a)



(b)

Figure 4. 17: Duty cycle of anti-parallel diodes in phase A (O2 SVM); (a): Conduction duty cycle of outer diode (D_{A1}), (b): Conduction duty cycle of inner diode (D_{A2})

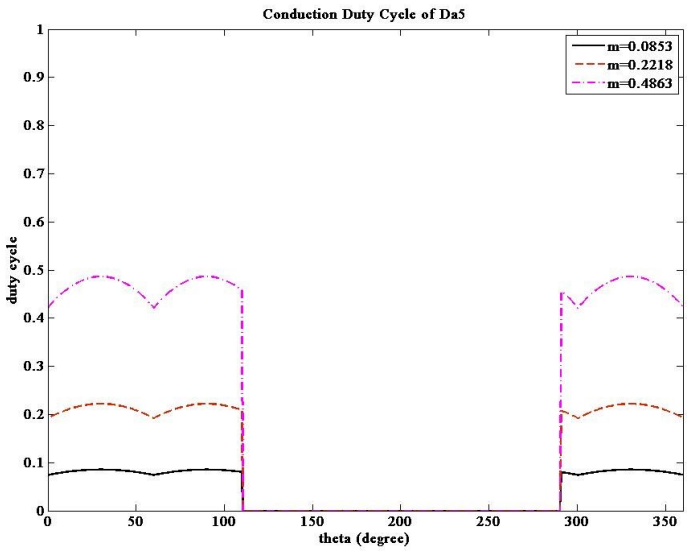


Figure 4. 18: Conduction duty cycle of clamping diode in phase A (O2 SVM)

Table 4. 7: Average duty cycle of upper devices in phase A for three modulation indices (O2 SVM)

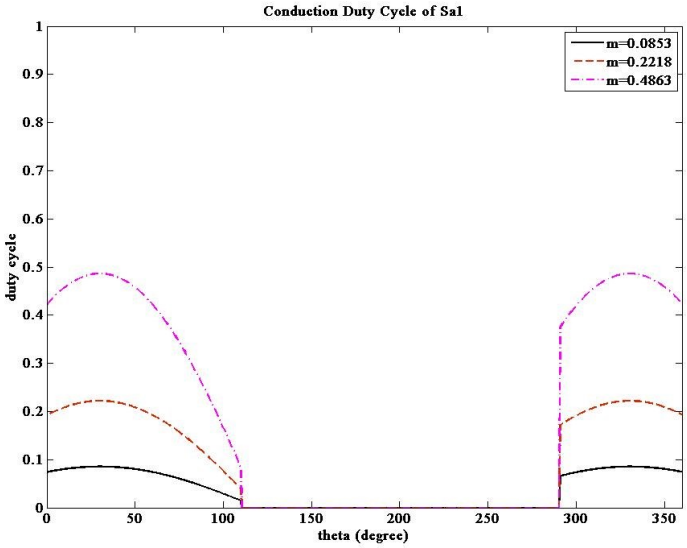
Devices		***Phase A***		
		φ =-20.17º		
		m=0.0853	***m=0.2218***	***m=0.4863***
Switches	S_1	0.2446	0.2364	0.2207
	S_2	0.2852	0.3422	0.4525
Anti-parallel diodes	D_1	0.2147	0.1575	0.0469
	D_2	0.2147	0.1575	0.0469
Clamping diodes	D_5	0.0407	0.1058	0.2319

As indicated in Table 4.7, the following statements can be deduced:

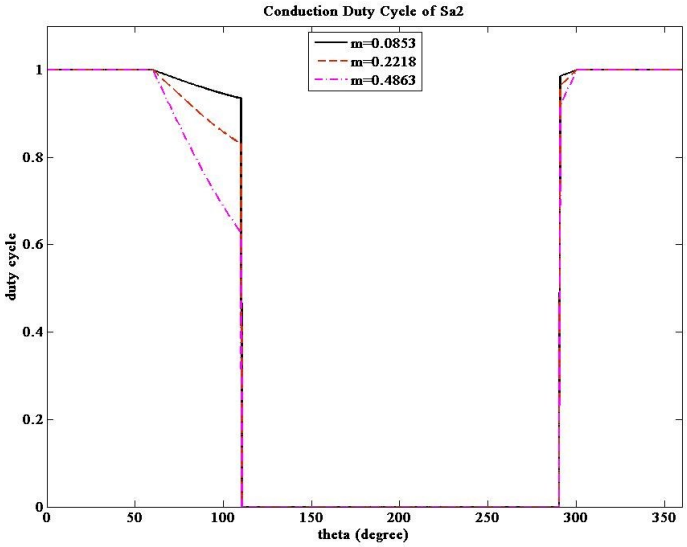
1- As the modulation index is increasing, the usage of zero state vector "111" is decreasing and usage of non-zero state vectors including "0" is increasing; that is, the outer switch will be conducting for smaller duration and inner switch will be conducting for larger duration. Therefore, the average duty cycle of the outer switch, S_1 is decreasing and of the inner switch is increasing. It can also be seen in Figure 4.16 that by increasing the modulation index, the plot for the outer switch gets larger slope and the plot of the inner switch gets higher value of duty cycle.
2- For each modulation index, the average duty cycle of the anti-parallel diodes are approximately similar. When the modulation index gets larger, the average duty cycle of the anti-parallel diodes becomes smaller. So, the conduction of the anti-parallel diodes will be decreasing.
3- According to Figure 4.18 and Table 4.7, as the modulation index is increasing, the average duty cycle for the clamping diode is getting larger.

4.4.3. CONDUCTION DUTY CYCLE FOR "O3" SVM

The plots of the conduction duty cycle are depicted in Figures 4.19-4.21 for O3 SVM method. Furthermore, the average conduction duty cycle of the upper devices in one leg (phase *A*) has been presented in Table 4.8.



(a)



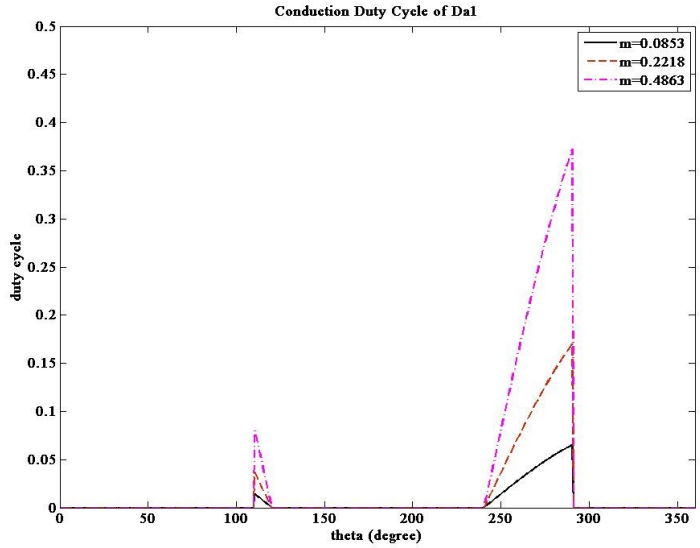
(b)

Figure 4. 19: Duty cycle of switches in phase A (O3 SVM); (a): Conduction duty cycle of outer switch (S_{A1}), (b): Conduction duty cycle of inner switch (S_{A2})

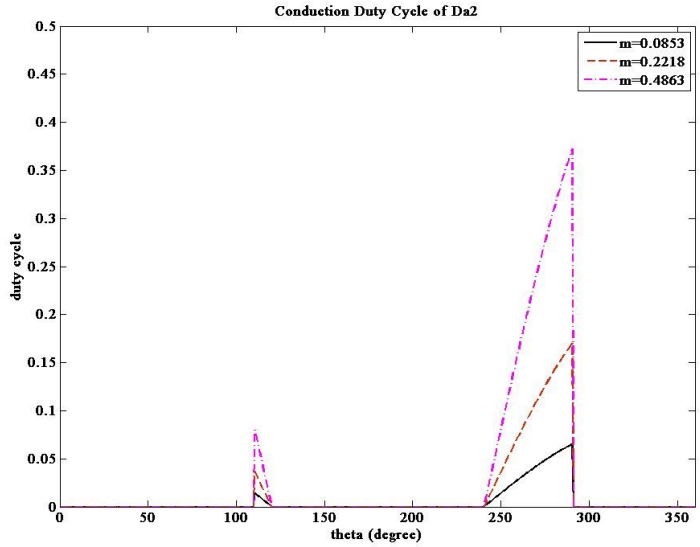
According to Figure 4.19, as the modulation index increases, the conduction duty cycle of the outer switch augments and that of inner switch reduces. When the modulation index increases from 0 to 0.5, the reference vector gets closer to the non-zero state vertices. Therefore, the usage of "1" increases and that of "0" decreases which means that the conduction duty cycle of S_1 gets larger and that of S_2 gets smaller.

As indicated in Figure 4.20, as the modulation index gets larger, the anti-parallel diodes will be conducting more in the segment with higher value of duty cycle. Therefore, the conduction duty cycle of anti-parallel diodes increases. In addition, the inner and outer anti-parallel diodes have identical conduction duty cycle. According to Table 3.20, the conduction duty cycle for upper anti-parallel diode is $\frac{2}{Ts} \times (\frac{T_a}{4} + \frac{T_b}{4})$. Considering the figure and the table, it is reasonable that the outer and inner switches conduct the output current for the equal period of time.

Figure 4.21 illustrates the conduction duty cycle of upper clamping diode. Conforming to this figure, as the modulation index increases, the usage of zero state vectors decreases. Therefore, the conduction duty cycle of the clamping diode gets smaller.



(a)



(b)

Figure 4. 20: Duty cycle of anti-parallel diodes in phase A (O3 SVM); (a): Conduction duty cycle of outer diode (D_{A1}), (b): Conduction duty cycle of inner diode (D_{A2})

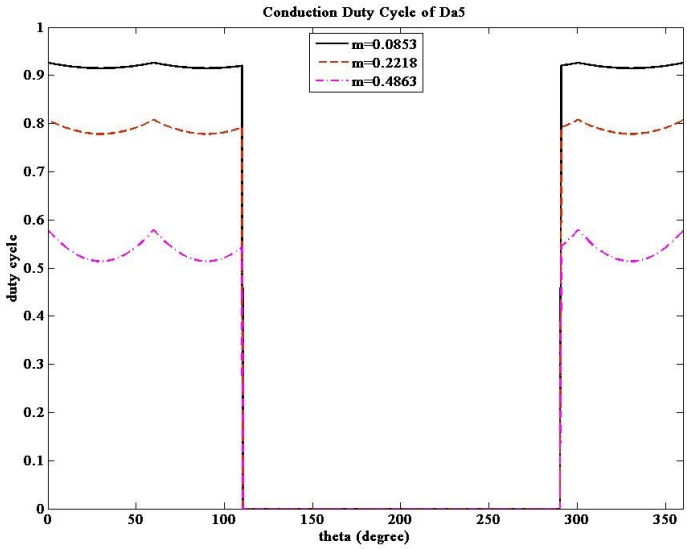


Figure 4. 21: Conduction duty cycle of clamping diode in phase A (O3 SVM)

Table 4. 8: Average duty cycle of upper devices in phase A for three modulation indices (O3 SVM)

Devices		***Phase A***		
		φ =-20.17º		
		m=0.0853	***m=0.2218***	***m=0.4863***
Switches	S_1	0.0356	0.0925	0.2029
	S_2	0.4942	0.4861	0.4703
Anti-parallel diodes	D_1	0.0051	0.0132	0.0290
	D_2	0.0051	0.0132	0.0290
Clamping diodes	D_5	0.4586	0.3936	0.2674

As indicated in Table 4.8, the following statements can be deduced:

1- As the modulation index is increasing, the average conduction duty cycle of the inner switches is decreasing due to the decrement in using zero state vector “000” and the average conduction duty cycle of the outer switches is getting larger due to the increment in using the non-zero state “1”.
2- For each modulation index, the average duty cycle of the anti-parallel diodes are approximately similar. When the modulation index is augmenting, the average duty cycle of the anti-parallel diodes gets larger. So, the conduction of the anti-parallel diodes will be increasing.
3- As the modulation index varies between 0 and 0.5, the average conduction duty cycle of the clamping diode reduces due to the decrement in using the zero state vector “000”.

4.4.4. COMPARISON OF THE METHODS

In order to better analyze the efficiency of the SVM methods in reducing the conduction duty cycle, all the results are presented in Table 4.9.

Table 4. 9: Comparison of average duty cycle of upper devices obtained from all methods for three different modulation indices

Load angle		***φ =-20.17°***								
Modulation index		***m=0.0853***			***m=0.2218***			***m=0.4863***		
Methods		***Normal***	***O2***	***O3***	***Normal***	***O2***	***O3***	***Normal***	***O2***	***O3***
Switches	S_1	0.1401	0.2446	0.0356	0.1645	0.2364	0.0925	0.2118	0.2207	0.2029
	S_2	0.3897	0.2852	0.4942	0.4141	0.3422	0.4861	0.4614	0.4525	0.4703
Anti-parallel diodes	D_1	0.1099	0.2147	0.0051	0.0854	0.1575	0.0132	0.0379	0.0469	0.0290
	D_2	0.1099	0.2147	0.0051	0.0854	0.1575	0.0132	0.0379	0.0469	0.0290
Clamping diodes	D_5	0.2497	0.0407	0.4586	0.2497	0.1058	0.3936	0.2497	0.2319	0.2674

According to Table 4.9, the following statements can be obtained for $\varphi = -20.17^{o}$:

1- By comparing results for 3 different modulation indices, it can be seen that for low value of modulation index, its impact on different methods is significant, while for higher value, the impact is low. Because when the modulation index is low, the zero state vectors are the most used state vectors and as the modulation index increases, the usage of state vectors in vertices of triangles is increasing.

2- In Normal SVM, the duty cycle of outer switch, S1 is less than that of inner switch, S2. For modulation index of *0.0853*, by applying O2 SVM, the duty cycle of the outer switch has been increased by about 74.6% and the duty cycle of the inner switches has been decreased by about 26.82%. For modulation index of *0.2218*, by applying O2 SVM, the duty cycle of S1 has been increased by about 43.71% and the duty cycle of S2 has been decreased by about 17.36%. Finally, for modulation index of *0.4863*, by applying O2 SVM, the duty cycle of the outer switch has been increased by about 4.2% and the duty cycle of the inner switch has been

decreased by about 1.93%. As indicated in this table, by applying O2 SVM, the conduction duty cycle for the inner switches has been reduced and for the outer switches has been increased. Therefore, O2 SVM is an appropriate method to reduce the conduction duty cycle of switches which have larger duty cycle especially for small modulation indices.

3- By using O3 SVM, the duty cycle of the outer switch, S1 is less than that in Normal SVM and the duty cycle of the inner switch, S2 is more than that in Normal SVM. For modulation index of *0.0853*, by applying O3 SVM, the duty cycle of S1 has been decreased by about 74.6% and the duty cycle of S2 has been increased by about 26.8%. For modulation index of *0.2218*, by applying O3 SVM, the duty cycle of S1 has got smaller by about 43.7% and the duty cycle of S2 has been augmented by about 17.4%. Finally, for modulation index of *0.4863*, by applying O3 SVM, the duty cycle of the outer switch has been cut down for about 4.2% and the duty cycle of the inner switch has got larger by about 1.9%. Accordingly, O3 SVM is a useful method to reduce the conduction duty cycle of switches which have lower duty cycle particularly for small modulation indices.

4- According to last two statements, for switches, O2 SVM has superiority over O3 SVM because in O2 SVM, the switches that have higher conduction duty cycle will be relieved and the conduction duty cycle will be more balanced among the switches. In addition, O2 SVM will be more efficient to obtain lower overall conduction losses if it is applied for small modulation indices.

5- In each SVM method, the two clamping diodes have similar duty cycle for different modulation indices. So, the two clamping diodes have identical behavior during conduction. For modulation index of *0.0853*, by applying O2 SVM, the duty cycle of the clamping diodes has been decreased by about 83.7%. For modulation index of *0.2218*, by applying O2 SVM, the

duty cycle of the clamping diodes has got smaller by about 57.6%. Finally, for modulation index of *0.4863*, by applying O2 SVM, the duty cycle of the clamping diodes has been cut down by about 7.1%. Therefore, O2 SVM is an effective method especially for small modulation indices to reduce the conduction duty cycle of the clamping diodes.

6- By using O3 SVM method, the conduction duty cycle of the clamping diodes has got larger. For modulation index of *0.0853*, by applying O3 SVM, the duty cycle of the clamping diodes has been increased by about 83.7%. For modulation index of *0.2218*, the duty cycle of the clamping diodes has been augmented by about 57.7%. Finally, the duty cycle of the clamping diodes has been increased by about 7.1% for modulation index of *0.4863*. So, O3 SVM method is increasing the conduction duty cycle of the clamping diodes especially for small modulation indices.

7- According to the last two statements, for the clamping diodes, O2 SVM has superiority over O3 SVM because in O2 SVM, the clamping diodes will be relieved and the conduction duty cycle will be decreased. In addition, O2 SVM will be more efficient when it is applied for small modulation indices.

The comparison of SVM methods is presented in Table 4.10. These comparisons are valid for three presented modulation indices.

Table 4. 10: Comparison of methods for duty cycle of devices in three-level inverter

Devices		***Comparison of methods***
Switches	S_1	O3 SVM < Normal SVM < O2 SVM
	S_2	O2 SVM < Normal SVM < O3 SVM
Anti-parallel diodes	D_1	O3 SVM < Normal SVM < O2 SVM
	D_2	O3 SVM < Normal SVM < O2 SVM
Clamping diodes	D_5	O2 SVM < Normal SVM < O3 SVM

According to Table 4.10, O2 SVM is a favorable method for inner switches (S2 & S3) and clamping diodes because it helps to reduce the conduction duty cycle of these devices. Nevertheless, the conduction duty cycle of outer switches (S1 & S4) and anti-parallel diodes is increased. O3 SVM is a favorable method for outer switches and anti-parallel diodes due to the decrement in the conduction duty cycle.

4.5. CONCLUSION

According to the results presented in this chapter, it can be deduced that in the first triangle of three-level inverter SVM scheme, as the modulation index or load angle varies independently, the conduction duty cycle of devices will be changing considering the SVM method. In addition, for a specific load angle and modulation index, O2 SVM method is efficient to reduce the conduction duty cycle of the inner switches and clamping diodes. Furthermore, O3 SVM is an efficient method to decrease the conduction duty cycle of the outer switches and anti-parallel diodes.

CHAPTER 5: PERFORMANCE VERIFICATION BY SIMULATION

5.1. INTRODUCTION

In a NPC three-level inverter, there are four switches, four anti-parallel diodes and two clamping diodes in each leg (phase). Considering the generated gating signals and current direction, some specific switches need to be enabled and accordingly, some devices, either switches or diodes, or both, start to conduct. The computation of the conduction duty cycle of semiconductors for three SVM methods has been discussed in Chapter 3.

In the present project, one of the concerns is to balance the conduction power loss among the switches in a NPC three-level inverter. Therefore in this chapter, the conduction power losses of devices in a NPC three-level inverter has been calculated in *MATLAB/Simulink*. The three SVM methods have been compared to investigate the appropriate method for balancing the conduction power loss of the switches.

In addition, since power quality is important in motor drives, the total harmonic distortion (THD) of the output current for three-level NPC inverter using different SVM techniques have been evaluated. The Fast Fourier Transform of the output phase current of the inverter has been presented for three different modulation indices.

5.2. COMPUTATION OF CONDUCTION LOSSES

When the semiconductor is in its *ON*-state, there is a voltage drop across the device and a current flowing through it, thus resulting in conduction power loss that have a major contribution to the total power losses and junction temperature of the semiconductors.

The instantaneous conduction loss is the product of the voltage over the device ($v_{ce}(t)$) and the current flowing through it ($i(t)$):

$$P_{cond}(t) = v_{ce}(t) i(t) \tag{5.1}$$

It is worthy to mention that for a semiconductor conduction loss, there is an approximate model which is a series connection of a DC voltage source (v_{ce0}) and a resistance (r_c):

$$v_{ce}(i_c) = v_{ce0} + r_c i_c \tag{5.2}$$

So, according to (5.1) and (5.2), the instantaneous conduction power loss for a semiconductor is given by:

$$P_{cond}(t) = v_{ce0}.i_c(t) + r_c i_c^2(t) \tag{5.3}$$

In addition, there is an expression for the average conduction power loss over one switching period that is calculated by using the average current (I_{c-avg}) and RMS value of semiconductor current (I_{c-rms}) [15]:

$$P_{cond-avg} = \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{cond}(t)\, dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (v_{ce0}.i_c(t) + r_c i_c^2(t))\, dt = V_{ce0} I_{c-avg} + r_c I_{c-rms}^2 \tag{5.4}$$

where T_{sw} is the inverse of switching frequency ($1/f_{sw}$).

The instantaneous conduction power loss can be computed in *MATLAB/Simulink* by using the voltage across the semiconductor and current flowing through the device in the three-level inverter. The diagram of the blocks for calculating the conduction power loss is shown in Figure 5.1.

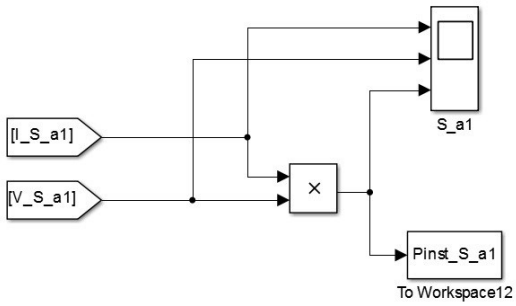


Figure 5. 1: Block diagram for conduction power loss of a switch in NPC three-level inverter in Simulink

The inverter parameters such as the ratings regarding the devices implemented in the *MATLAB/Simulink* and the parameters of the NPC three-level inverter such as switching frequency and output current are indicated in Table 5.1 and Table 5.2 respectively. In addition, the scheme of the NPC three-level inverter implemented in Simulink is shown in Figure 5.2.

Table 5. 1: Parameters of the devices in NPC three-level inverter

Parameter	value
R_{switch}	0.00422 Ω
$V_{f\text{-}switch}$	0.8 v
R_{diode}	0.00293 Ω
$V_{f\text{-}diode}$	0.56 v

Table 5. 2: Parameters relevant to the three-level NPC inverter

Parameter	value
I_{output}	116 A
f_{sw}	12600 HZ
f_{sys}	210 HZ
m	0.4863
V_{DC}	600 V

The system frequency (f_{sys}) is actually the fundamental output voltage frequency and it has been calculated according to the speed and the number of poles of the PMSM presented in Table 2.2.

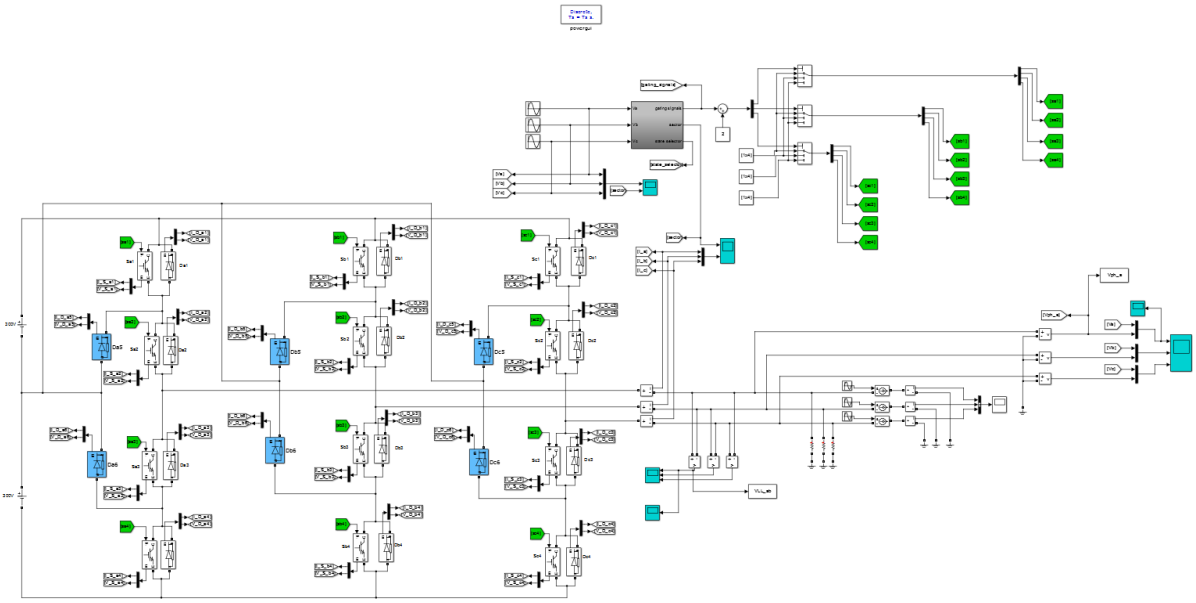


Figure 5. 2: Scheme of NPC three-level inverter and generating gating signals in Simulink

According to Figure 5.2., the simulation includes the 3-level 3-phase NPC inverter, the 3-phase load and the generating gating signal block. This block is including 4 blocks in order to generate gating signals in 4 steps that is explained in the following. This block is shown in Figure 5.3.

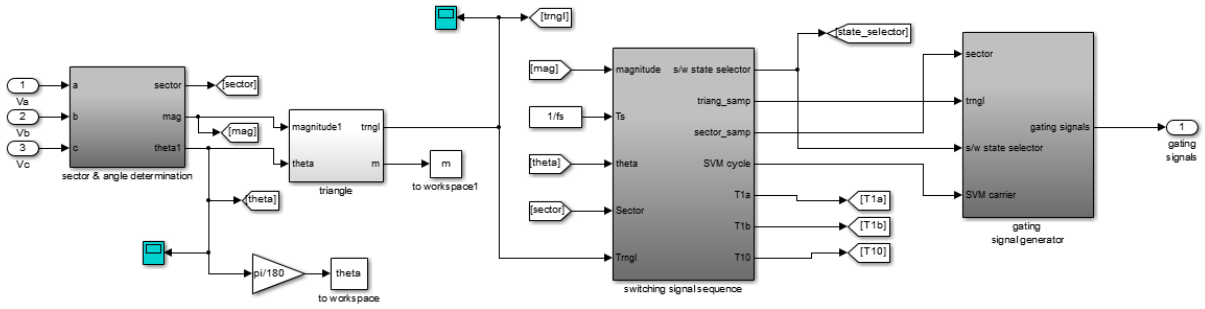


Figure 5. 3: 4-step gating signal generation block diagram

To obtain the instantaneous conduction power loss in *MATLAB/Simulink*, there is a product of the voltage across the device and the current flowing through the device. This calculation has been done for three methods; Normal, O2 and O3 SVM strategies. To generate the gating signals for the switches, 4 blocks have been developed as the following:

1) Determine sector and angle: According to the calculated angle of the reference voltage vector, the sector can be determined. As mentioned before, due to circular symmetry, the angle should be moved to Sector 1. The procedure has been presented in Table 3.2. The block is depicted in Figure 5.4.

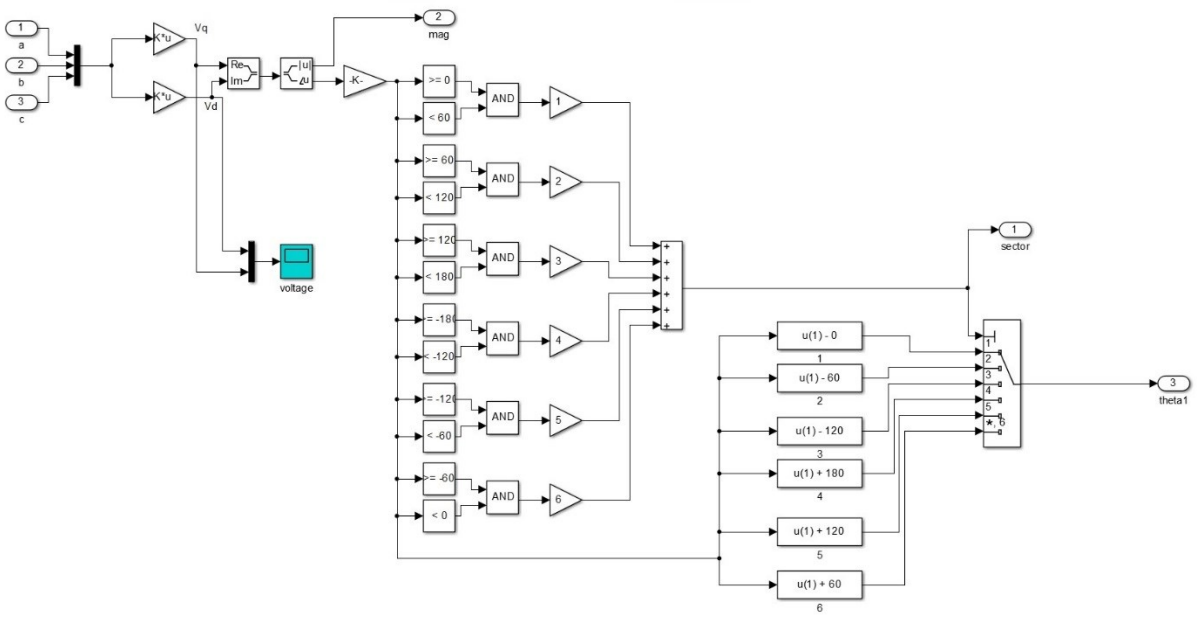


Figure 5. 4: Sector and angle determination in Simulink

2) Determine triangle: As discussed in section 3.2.1.2, according to 4 comparisons for two parameters *m1* and *m2*, the triangle in a sector can be determined. Table 3.3, has presented theses comparisons. The block implemented in Simulink is illustrated in Figure 5.5.

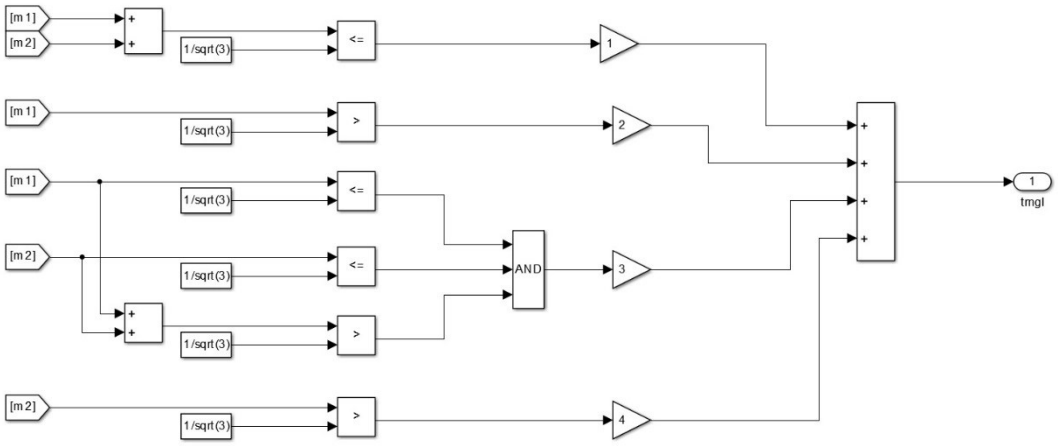


Figure 5. 5: Triangle determination in Simulink

3) Switching signal sequence: In this block, there are two sub-blocks. Primarily, the time (T_a, T_b and T_0) are calculated according to (3.7). Next in order, the number of the state vector is defined. In Triangle 1, there are 7 state vectors in the Normal SVM method, so the number of state vectors is from 1 to 7. The main block consisting of two sub-blocks is depicted in Figure 5.6. The calculation implemented in the second sub-block and the plot of the output signal of this block, regarding the number of state vectors, are shown in Figure 5.7.

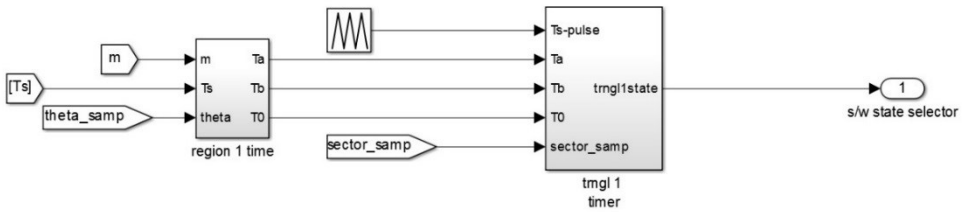
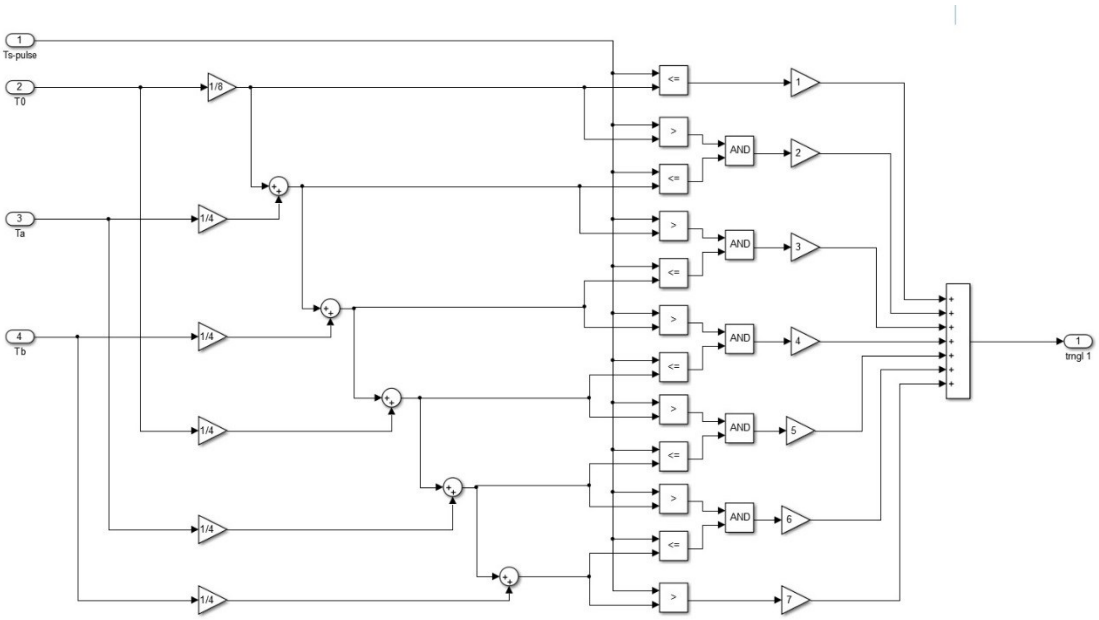
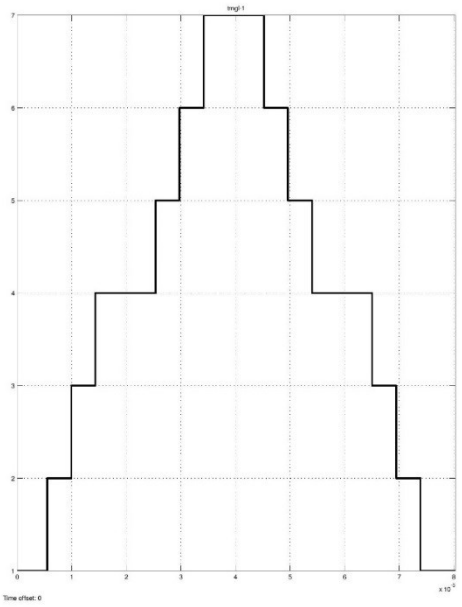


Figure 5. 6: Switching signal sequence block in Simulink



(a)



(b)

Figure 5. 7: State sequence in Simulink; (a): Generating number of state vector; (b): number of state sequences

4) Generate switching signals: According to the number of the state vector obtained from the previous block and the number of the sector, the appropriate states (ON-OFF) are generated for the switches. As illustrated in Figure 5.8, there are 6 sectors in which there are 4 triangles. In the present project, the study is held only in Triangle 1. In Figure 5.9, the state vectors of Triangle 1 in Sector 1 are shown. According to the state vector selector (Figure 5.6), the proper one is generated. For instance, if the signal from the state vector selector brings the number 2, this corresponds to space vector [0 -1 -1], which is implemented by enabling S_2 and S_3 in leg A and S_3 and S_4 in legs B and C.

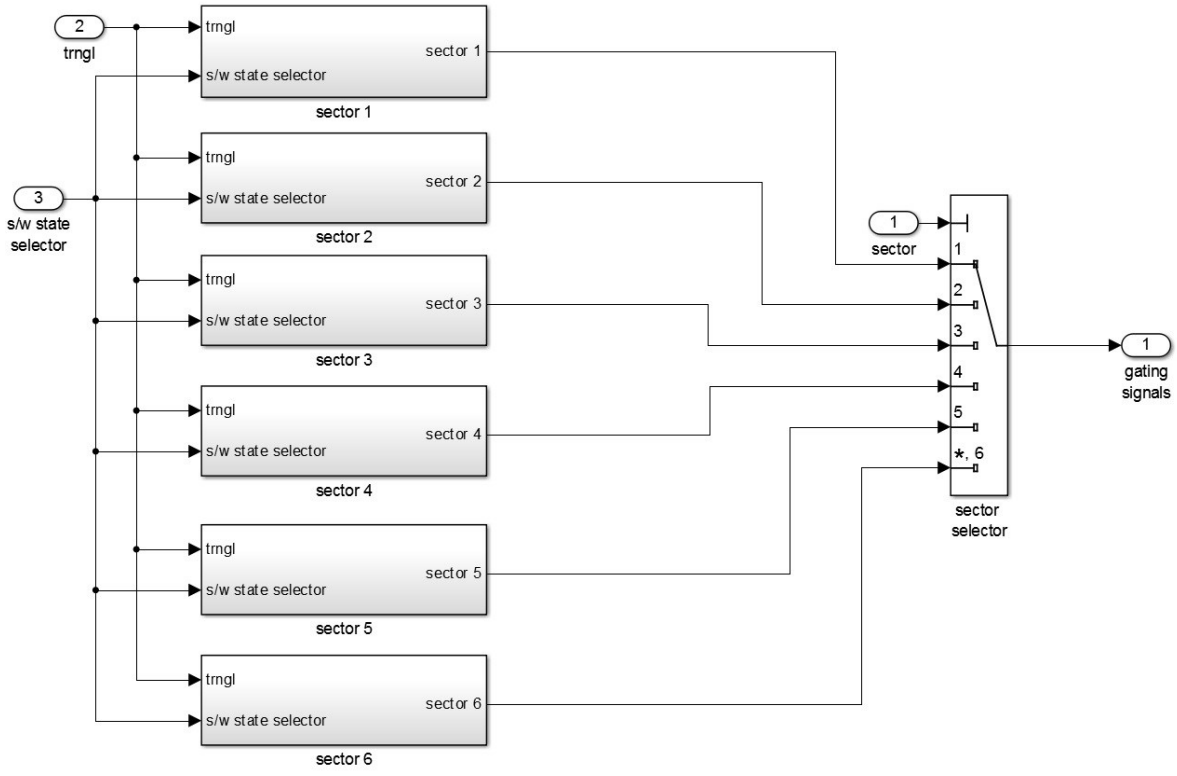


Figure 5. 8: Six sectors in Simulink

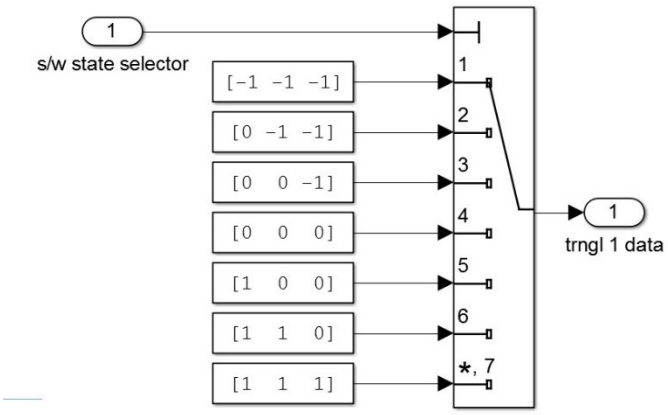


Figure 5. 9: State vectors of Triangle 1, Sector 1 in Simulink

In order to evaluate the methods regarding the average conduction power loss in one line cycle, the DC component in FFT of the instantaneous conduction power has been obtained as an indication of average value for all devices in phase *A*. The trend for the other two phases are similar to that of phase *A*.

As discussed in chapter 3, the results have been obtained in order to indicate the influence of two parameters individually on conduction power loss; the load angle and the modulation index. In the present chapter, these influences have been investigated in *MATLAB/Simulink*. In the following, there are two sections; the impact of load angle on conduction power loss via three methods and the impact of modulation index on conduction power loss via three methods. Furthermore, the effect of these methods on the THD of the output current have been investigated for different modulation indices.

5.3. INFLUENCE OF LOAD ANGLE ON CONDUCTION POWER LOSSES OF DEVICES

The conduction power loss of devices obtained by three methods in *MATLAB /Simulink* are presented in the following sub-sections. The impact of two different load angles on conduction power loss is shown for SVM methods. The load angles belong to the speed range in which there is no field weakening for the PMSM. These values are *-16.61°* and *-20.17°* and have been selected from Table 2.2 for the modulation index of '*0.4863*'. The conduction power losses of semiconductors in the three-level inverter have been obtained for the output phase current (I_{ph}) = 116 A, DC-link voltage (V_{dc}) = 600 V, fundamental output voltage frequency (f) = 210 Hz and switching frequency (f_{sw}) = 12.6 KHz. This condition has been applied for all three methods; Normal, O2 and O3 SVM.

5.3.1. CONDUCTION POWER LOSS FOR "NORMAL" SVM

The average conduction power loss of the devices obtained from *MATLAB /Simulink* are shown in Table 5.2. The first implemented modulation scheme is the Normal SVM method. The waveforms regarding the voltage across the device, the current through the device and the conduction power of the device are shown in Figure 5.10. As an example, these waveforms have been depicted for S_{A1} for two cycles (0.0095 sec). In addition, the conduction power loss for upper devices in phase *A* for Normal SVM method is presented in Table 5.3. The unit of conduction power is watt.

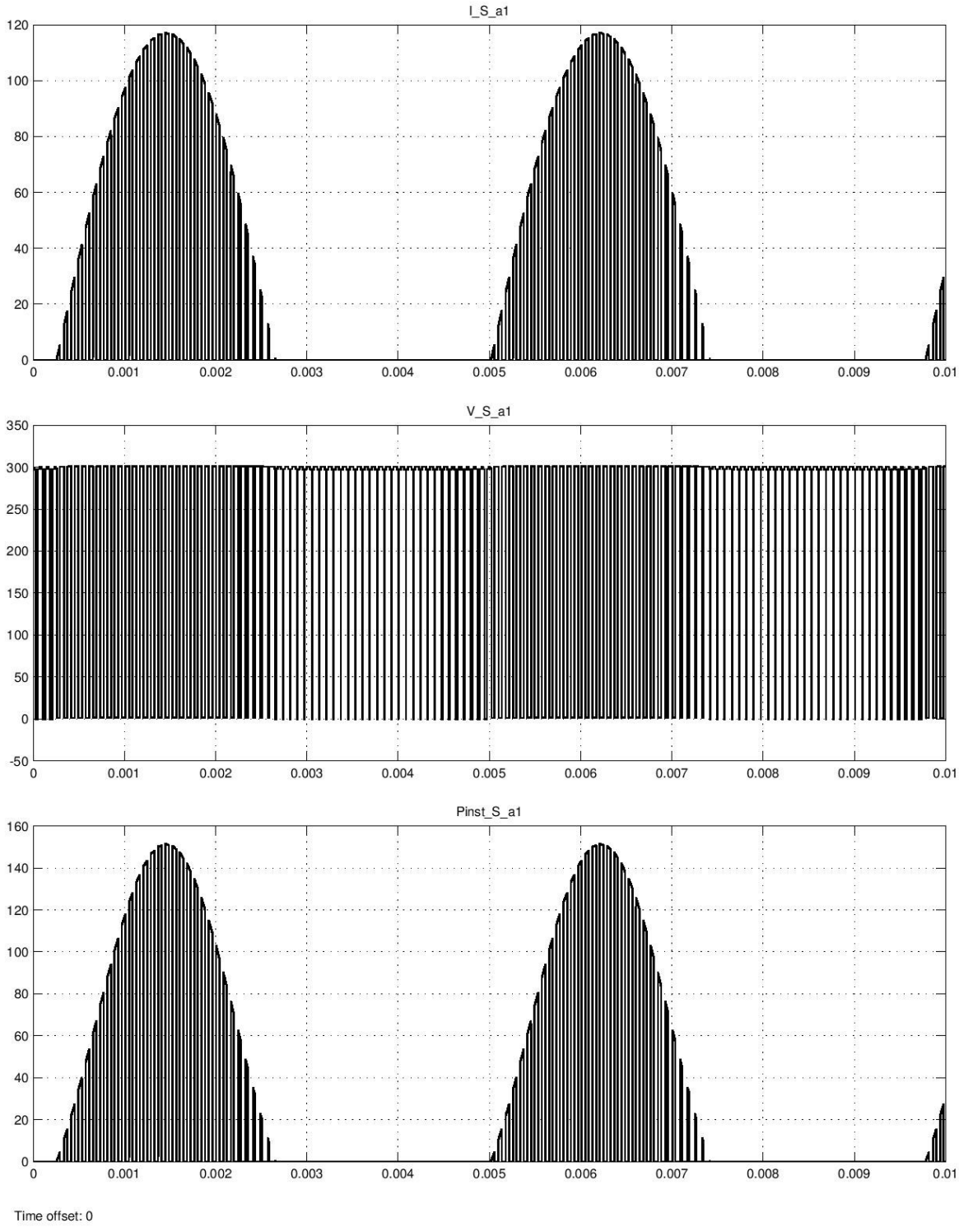


Figure 5. 10: Waveforms of current, voltage and instantaneous power for SA1 (Normal SVM)

Table 5. 3: Conduction power loss for upper devices in phase A (Normal SVM)

Devices		***Phase A***	
		m=0.4863	
		φ =-16.61º	***φ =-20.17º***
Switches	***S_1***	20.84	20.69
	S_2	42.59	42.45
Anti-parallel diodes	***D_1***	0.8971	0.9969
	D_2	0.9178	1.018
Clamping diodes	***D_5***	15.17	15.18

According to Table 5.3, it can be said that when the three-level inverter is operating under Normal SVM strategy, as the load angle increases, the conduction losses of the switches decrease and of the anti-parallel diodes increase. Hence, the conduction of switches is reducing and the conduction of anti-parallel diodes is getting larger. For the clamping diodes, the conduction power is constant. Therefore, for two different load angles, the clamping diodes behave consistently.

As indicated in Table 4.1, for a specific modulation index in Normal SVM method, as the load angle increases, the conduction duty cycle of inner and outer switches decreases, the conduction duty cycle of inner and outer anti-parallel diodes increases and for the clamping diode it remains constant. Therefore, the conduction power loss of a device depends on its conduction duty cycle; the larger the conduction duty cycle is, the more the device is conducting. So, the larger the conduction power loss will be. Besides, there is a good qualitative correlation between the average values of conduction duty cycle shown in Table 4.1 and the actual conduction power losses for the switches shown in Table 5.3.

5.3.2. CONDUCTION POWER LOSS FOR "O2" SVM

The conduction power loss of upper devices under O2 SVM strategy in *MATLAB /Simulink* are shown in Table 5.4. The unit of conduction power is watt.

Table 5. 4: Conduction power loss for upper devices in phase A (O2 SVM)

Devices		***Phase A***	
		m=0.4863	
		φ =-16.61°	***φ =-20.17°***
Switches	S_1	21.53	21.38
	S_2	41.90	41.76
Anti-parallel diodes	D_1	1.374	1.47
	D_2	1.401	1.497
Clamping diodes	D_5	14.2	14.21

According to Table 5.4, it can be inferred that when using O2 SVM strategy for the three-level inverter, as the load angle increases, the conduction losses of the switches decrease and of anti-parallel diodes increase and for clamping diodes, it is constant. Therefore, the switches are conducting less, the anti-parallel diodes are conducting more and there will be no change in conduction of the clamping diodes.

As stated in Table 4.2, for the modulation index (m) = 0.4863 in O2 SVM method, as the load angle increases, the conduction duty cycle of the inner and outer switches decreases, the conduction duty cycle of the inner and outer anti-parallel diodes increases and for the clamping diode it remains constant. Considering the values in Table 5.4, it can be said that the conduction power loss of a device depends on its conduction duty cycle; that is, the device with larger conduction duty cycle will conduct more. Therefore, its conduction power loss will be larger.

5.3.3. CONDUCTION POWER LOSS FOR "O3" SVM

O3 SVM strategy has been applied for the three-level inverter in *MATLAB /Simulink* to obtain the conduction power loss of the devices. These results are shown in Table 5.5. The unit of conduction power is watt.

Table 5. 5: Conduction power loss for upper devices in phase A (O3 SVM)

Devices		***Phase A***	
		m=0.4863	
		φ =-16.61°	***φ =-20.17°***
Switches	***S_1***	20.13	19.99
	S_2	43.28	43.13
Anti-parallel diodes	***D_1***	0.4206	0.5223
	D_2	0.435	0.5373
Clamping diodes	***D_5***	16.15	16.15

According to Table 5.5, by applying O3 SVM strategy for the three-level inverter, as the load angle increases the conduction power of the switches decreases, of the anti-parallel diodes augments and for the clamping diodes, it remains constant. Hence, it can be said that the conduction of switches gets lower, of anti-parallel diodes gets larger and of clamping diodes remains constant.

As presented in Table 4.3, for a specific modulation index in O3 SVM method, as the load angle increases, the conduction duty cycle of the inner and outer switches decreases, the conduction duty cycle of the inner and outer anti-parallel diodes increases and for the clamping diode it remains constant. Therefore, the conduction power loss of a device depends on its

conduction duty cycle; the larger the conduction duty cycle is, the more the device is conducting. So, the conduction power loss will get larger.

To better compare the three SVM methods, all the results are indicated in Table 5.6. The devices can be classified into five categories; outer switch, inner switch, outer anti-parallel diode, inner anti-parallel diode and clamping diode. The results presented in this table are for one device from each category and the analysis can be generalized for the complementary devices.

Considering the results presented in Table 4.4, for a specific load angle and modulation index, by implementing O2 SVM, the conduction duty cycle of the inner switch and clamping diode has been reduced and by using O3 SVM, the conduction duty cycle of these two device categories has been increased. For the outer switches and anti-parallel diodes this approach is reversed; by implementing O2 SVM, the conduction duty cycle of the outer switches and anti-parallel diodes has been reduced and conduction duty cycle of inner switch and clamping diode has been increased. Since the conduction power loss depends on the conduction duty cycle of the device, the results in Table 5.6 should demonstrate similar approach to those in Table 4.4. The unit of conduction power is watt.

Table 5. 6: Comparison of conduction power loss of devices for three SVM methods

Modulation index		***m=0.4863***					
Load angle		***φ =-16.61°***			***φ =-20.17°***		
Methods		***Normal***	***O2***	***O3***	***Normal***	***O2***	***O3***
Switches	S_1	20.84	21.53	20.13	20.69	21.38	19.99
	S_2	42.59	41.90	43.28	42.45	41.76	43.13
Anti-parallel diodes	D_1	0.8971	1.374	0.4206	0.9969	1.47	0.5223
	D_2	0.9178	1.401	0.435	1.018	1.497	0.5373
Clamping diodes	D_5	15.17	14.20	16.15	15.18	14.21	16.15

Based on the results indicated in Table 5.6, in Normal SVM, the conduction power of the inner switch, S2 is larger than the conduction power of the outer switch, S1. In order to balance the conduction power loss among these two switches, the conduction power losses of the inner switch should be reduced and that of the outer switch should be increased. According to Table 5.6, by applying O2 SVM, the conduction power of the inner switch is reduced and the conduction power of the outer switch gets an increment. Because in this method, the state vector "000" is eliminated, so the conduction of the inner switch will be decreasing. Therefore, the conduction power loss among these switches get more balanced. With O2 SVM, the conduction power of outer switch, S1 has an increment about 3.3% and the conduction power of inner switch, S2 has a decrement about 1.6% for both load angles. It indicates that by implementing O2 SVM, the conduction power for the inner switch has been reduced and for the outer switch has been increased. Therefore, this method is helpful to cut down the conduction power of devices which have larger values.

When O3 SVM is used, the conduction power of outer switch, S1 is less than that in Normal SVM and the conduction power of inner switch, S2 is more than that in Normal SVM. Hence, it can be said that for outer switch, S1, the conduction power can be reduced by 3.4% and for inner switch, S2, there will be an increment of about 1.6%. So, O3 SVM method is useful to reduce the conduction power of devices with lower value of conduction power.

According to previous statements, O2 SVM has a better performance than O3 SVM because in O2 SVM, the switches that have higher conduction power will be relieved and the conduction power will be more balanced among the switches.

In order to reduce the conduction power loss of clamping diode (D5/D6), O2 SVM method should be applied. Since the state vector "000" is eliminated in O2 SVM method, the conduction of the clamping diode will be reduced. In each SVM method, the clamping diodes have similar conduction power for different load angles. So, the clamping diodes have identical behavior during conduction. If O2 SVM method is applied, the conduction power of the clamping diode is getting smaller by about 6.39% and by using O3 SVM, it has an increment of 6.4% for both load angles. It indicates that for the clamping diode, O2 SVM method is more efficient than O3 SVM method.

The antiparallel diodes (D1-D4) have similar conduction power loss in each method. By using O2 SVM, the conduction power loss of these diodes is increasing and they will conduct more. Moreover, by applying O3 SVM, the conduction power loss will be reduced and the diodes will be conducting less. For the load angle of -16.61^{o}, by applying O2 SVM method, the conduction power of the anti-parallel diodes has been increased for about 53% and with the help of O3 SVM method, the conduction power has been decreased by about 53%. Moreover, for the load angle of -20.17^{o}, these percentages will be 47.2% of increment by O2 SVM and 47.4% decrement by O3

SVM for diodes. Therefore, for anti-parallel diodes, O3 SVM method is more efficient than O2 SVM method.

Accordingly, it can be said that by implementing O3 SVM method, the conduction power of an outer switch (S1/S4) can be reduced due to the elimination of the state vectors "111" and "-1-1-1". So the dwelling time for the state vector "000" is increasing; that is the usage of inner switches (S2/S3) is increasing. In addition, by implementing O3 SVM strategy, the conduction power of the anti-parallel diodes can be reduced but the clamping diodes will conduct more, so the conduction power loss for the clamping diodes is increasing due to the presence of the zero state vector "000".

The comparison of SVM methods for conduction power loss is presented in Table 5.7. These comparisons are valid for two different load angles: -16.61^{o} and -20.17^{o}.

Table 5. 7: Comparison of methods for conduction power of devices in NPC three-level inverter (different load angles)

Devices		***Comparison of methods***
Switches	S_1	O3 SVM < Normal SVM < O2 SVM
	S_2	O2 SVM < Normal SVM < O3 SVM
Anti-parallel diodes	D_1	O3 SVM < Normal SVM < O2 SVM
	D_2	O3 SVM < Normal SVM < O2 SVM
Clamping diodes	D_5	O2 SVM < Normal SVM < O3 SVM

According to Table 5.7, O2 SVM is a useful method for inner switches (S2 & S3) and clamping diodes (D5 & D6) because it helps these devices to get lower conduction power losses. In this method, the state vector "000" has been eliminated. Therefore, the conduction of the inner switches and clamping diodes has been reduced. Nevertheless, the conduction power loss of outer switches (S1 & S4) and anti-parallel diodes (D1-D4) is increased.

Furthermore, O3 SVM is an efficient method for outer switches (S1 & S4) and anti-parallel diodes (D1 - D4) due to the decrement in the conduction power losses. In this method, both zero state vectors "-1-1-1" and "111" have been eliminated. So, the conduction of outer switches (S1 & S4) has been reduced. However, the inner switches (S2 & S3) and clamping diodes (D5 & D6) get higher conduction power loss.

5.4. INFLUENCE OF MODULATION INDEX ON CONDUCTION POWER LOSS OF DEVICES

The conduction power loss of devices obtained with three methods in *MATLAB/Simulink* are shown in the following sub-sections. The impact of three different modulation indices on conduction power loss is shown for Normal SVM method. These modulation indices are ***0.0853***, ***0.2218*** and ***0.4863*** and have been selected from Table 2.2 for the lagging load angle of '***20.17°***'. Since the devices in the three phases have similar duty cycles, the results have been obtained for phase *A* only. The conduction power losses of semiconductors in the three-level inverter have been obtained for the output phase current (I_{ph}) = 116 A, DC-link voltage (V_{dc}) = 600 V, fundamental output voltage frequency (f) = 210 Hz and switching frequency (f_{sw}) = 12.6 KHz. This condition has been applied for all three methods: Normal, O2 and O3 SVM.

5.4.1. CONDUCTION POWER LOSS FOR "NORMAL" SVM

The conduction power loss of the devices obtained in *MATLAB/Simulink* for Normal SVM method are shown in Table 5.8. The unit of conduction power is watt.

Table 5. 8: Conduction power loss for upper devices in phase A (Normal SVM)

Devices		***Phase A***		
		φ =-20.17°		
		m=0.0853	***m=0.2218***	***m=0.4863***
Switches	S_1	12.81	15.47	20.69
	S_2	34.75	37.35	42.45
Anti-parallel diodes	D_1	6.357	4.552	0.9969
	D_2	6.438	4.615	1.018
Clamping diodes	D_5	15.27	15.23	15.18

According to Table 5.8, it can be said that as the modulation index is increasing, the conduction power of the switches is increasing and of the anti-parallel diodes is decreasing. Therefore, the switches will be conducting more and the anti-parallel diodes less. For the clamping diodes, the conduction power is approximately constant. Therefore, by varying the modulation index, there will not be any noticeable change in conduction power losses of the clamping diodes.

5.4.2. CONDUCTION POWER LOSS FOR "O2" SVM

The conduction power loss of the devices obtained in *MATLAB/Simulink* are presented in Table 5.9. The impact of three different modulation indices on the conduction power loss of the devices is illustrated for the O2 SVM method. The unit of conduction power is watt.

Table 5. 9: Conduction power loss for upper devices in phase A (O2 SVM)

Devices		***Phase A***		
		φ =-20.17°		
		m=0.0853	***m=0.2218***	***m=0.4863***
Switches	S_1	22.03	21.80	21.38
	S_2	25.72	31.17	41.76
Anti-parallel diodes	D_1	12.6	8.813	1.47
	D_2	12.64	8.886	1.497
Clamping diodes	D_5	2.555	6.507	14.21

According to Table 5.9, it can be said that as the modulation index increases, the conduction power of the outer switches (S1 & S4) and anti-parallel diodes (D1-D4) is decreasing and of the inner switches (S2 & S3) and clamping diodes (D5 & D6) is increasing. It seems that by increasing the modulation index, the unbalance of conduction power among switches is increasing; the switches with higher conduction loss will present more conduction power and those with smaller conduction power losses will present less. In addition, the conduction of the anti-parallel diodes is decreasing and the conduction power losses of the clamping diodes is increasing.

5.4.3. CONDUCTION POWER LOSS FOR "O3" SVM

The conduction power loss of the devices obtained in *MATLAB/Simulink* are shown in Table 5.10. The impact of three different modulation indices on conduction power loss of the devices is indicated for the O3 SVM method. The unit of conduction power is watt.

Table 5. 10: Conduction power loss for upper devices in phase A (O3 SVM)

Devices		***Phase A***		
		φ =-20.17°		
		m=0.0853	***m=0.2218***	***m=0.4863***
Switches	S_1	3.62	9.181	19.99
	S_2	43.67	43.49	43.13
Anti-parallel diodes	D_1	0.088	0.2463	0.5223
	D_2	0.091	0.255	0.5373
Clamping diodes	D_5	27.95	23.95	16.15

According to Table 5.10, it can be inferred that as the modulation index increases, the conduction power losses of the outer switches (S1 & S4) and anti-parallel diodes (D1-D4) is increasing and of the inner switches (S2 & S3) and clamping diodes (D5 & D6) is decreasing.

By increasing the modulation index, the unbalance of conduction power losses among switches is decreasing; the switches with higher conduction loss will present lower conduction power losses and the switches with lower conduction power loss will have larger ones. In addition, the conduction of anti-parallel diodes is increasing and the conduction power of the clamping diodes is decreasing.

In order to compare the three SVM methods, all the results are indicated in Table 5.11. In this table, the conduction power loss is presented for one device from each category; outer switch, inner switch, outer anti-parallel diode, inner anti-parallel diode and clamping diode.

Considering the results presented in Table 4.9, for a specific load angle and modulation index, by implementing O2 SVM, the conduction duty cycle of the inner switch and clamping diode has been reduced and by using O3 SVM, the conduction duty cycle of these two device categories has been increased. For the outer switch and anti-parallel diodes this approach is reversed; by implementing O2 SVM, the conduction duty cycle of the outer switch and anti-parallel diodes has been reduced and the conduction duty cycle of the inner switch and clamping diode has been increased. Since the conduction power loss depends on the conduction duty cycle of the device, the results in Table 5.9 should demonstrate similar approach to those in Table 4.9. The unit of conduction power is watt.

Table 5. 11: Comparison of conduction power loss of devices for three SVM methods

Load angle		***φ =-20.17°***								
Modulation index		***m=0.0853***			***m=0.2218***			***m=0.4863***		
Methods		***Normal***	***O2***	***O3***	***Normal***	***O2***	***O3***	***Normal***	***O2***	***O3***
Switches	S_1	12.81	22.03	3.62	15.47	21.80	9.181	20.69	21.38	19.99
	S_2	34.75	25.72	43.67	37.35	31.17	43.49	42.45	41.76	43.13
Anti-parallel diodes	D_1	6.357	12.6	0.088	4.552	8.813	0.2463	0.9969	1.47	0.5223
	D_2	6.438	12.64	0.091	4.615	8.886	0.255	1.018	1.497	0.5373
Clamping diodes	D_5	15.27	2.555	27.95	15.23	6.507	23.95	15.18	14.21	16.15

According to the results in Table 5.11, In Normal SVM, the conduction loss of the outer switch is less than that of the inner switch. To balance the conduction power loss among these two switches, the power of the inner switch should be reduced and that of the outer switch should be increased. For modulation index of *0.0853*, by applying O2 SVM, the conduction power of the outer switch has been increased by about 71.98% and the conduction power of the inner switches has been decreased by about 25.99%. For modulation index of *0.2218*, the duty cycle of S1 has been augmented by about 40.92% and the duty cycle of S2 has been cut down by about 16.55%. Finally, for modulation index of *0.4863*, by using O2 SVM, the conduction power of the outer switch has been increased by about 3.33% and the duty cycle of the inner switch has been decreased by about 1.63%. As it is presented in the table, by applying O2 SVM, the conduction power loss among these switches get more balanced.

By applying O3 SVM, the conduction power of the outer switch, S1 is less than that in Normal SVM and the conduction power loss of the inner switch, S2 is more than that in Normal SVM. For modulation index of *0.0853*, the conduction power of S1 has been decreased by about 71.74% and the conduction power of S2 has been augmented by about 25.67%. For modulation index of *0.2218*, the conduction power of S1 has got smaller by about 40.65% and the conduction power of S2 has been increased by about 16.44%. Finally, for modulation index of *0.4863*, the conduction power of the outer switch has been decreased by about 3.38% and the conduction power of the inner switch has got larger by about 1.6%. Accordingly, O3 SVM is a useful method to reduce the conduction power losses of switches which have lower value, particularly for small modulation indices.

According to the last two statements, for switches, O2 SVM has better performance than O3 SVM because in O2 SVM, the switches that have higher conduction power will be relieved and

the conduction power will be more balanced among the switches. In addition, O2 SVM will be more efficient if it is applied for small modulation indices.

To investigate the impact of modulation index on conduction power loss of the clamping diode in O2 SVM method, it can be said that for modulation index of *0.0853*, by applying this method, the conduction power has been cut down by about 83.27%. For modulation index of *0.2218*, the conduction power of the clamping diode has been decreased by about 57.28%. Finally, for modulation index of *0.4863*, the conduction power of the clamping diode has got smaller by about 6.39%. Therefore, O2 SVM is an effective method especially for small modulation indices to reduce the conduction power of the clamping diode.

In O3 SVM method, the conduction power of the clamping diode, D5 has been increased. For modulation index of *0.0853*, by applying O3 SVM, the conduction power loss of the clamping diode has been increased by about 83.04%. For modulation index of *0.2218*, the conduction power of the clamping diode has got larger by about 57.26%. Finally, for modulation index of *0.4863*, the conduction power of the clamping diode has been augmented by about 6.39%. So, O3 SVM method is increasing the conduction power of the clamping diodes especially for small modulation indices.

Accordingly, in order to reduce the conduction power loss for the clamping diode, D5, it is better to apply O2 SVM than using O3 SVM, because in O2 SVM, the conduction power loss of clamping diode are reducing especially for smaller modulation indices.

The antiparallel diodes (D1, D4) have similar conduction power loss in each method. In O2 SVM, the conduction power loss of these diodes is increasing and they will conduct more. Moreover, by applying O3 SVM, the conduction power loss will be reduced and the diodes will be conducting less. For the modulation index of *0.0853*, by using O2 SVM method, the conduction

power of the anti-parallel diodes has been increased by about 96% and with the help of O3 SVM method, the conduction power losses has been decreased by about 98%. Moreover, for the modulation index of *0.2218*, these percentages will be 92% of increment by O2 SVM and 94% decrement by O3 SVM for diodes. Finally, for the modulation index of *0.4863*, when O2 SVM is applied, the conduction power losses of this device gets larger by about 47% and by using O3 SVM, there is a decrement of about 47%. Therefore, for anti-parallel diodes, O3 SVM method is more efficient than O2 SVM method.

The comparison of SVM methods for conduction power loss is presented in Table 5.12. These comparisons are valid for the three mentioned modulation indices.

Table 5. 12: Comparison of methods for conduction power of devices in NPC three-level inverter (different modulation indices)

Devices		***Comparison of methods***
Switches	S_1	O3 SVM < Normal SVM < O2 SVM
	S_2	O2 SVM < Normal SVM < O3 SVM
Anti-parallel diodes	D_1	O3 SVM < Normal SVM < O2 SVM
	D_2	O3 SVM < Normal SVM < O2 SVM
Clamping diodes	D_5	O2 SVM < Normal SVM < O3 SVM

According to Table 5.12, O2 SVM is a beneficial method for the inner switches (S2 & S3) and clamping diodes (D5 & D6) because it helps these devices to get reduced conduction power loss. In this strategy, the zero state vector “000” has been eliminated. Therefore, the conduction of the

inner switches and clamping diodes has been decreased. Nevertheless, the conduction power loss of the outer switches (S1 & S4) and anti-parallel diodes (D1-D4) is increased.

Furthermore, O3 SVM is an efficient method for the outer switches (S1 & S4) and anti-parallel diodes (D1 - D4) due to the decrement in the conduction power losses. While using O3 SVM, both zero state vectors "-1-1-1" and "111" have been eliminated. So, the conduction of the outer switches (S1 & S4) has been reduced. However, the inner switches (S2 & S3) and clamping diodes (D5 & D6) get higher conduction power loss.

5.5. THD OF INVERTER OUTPUT CURRENTS FOR THREE METHODS

In the present project, in addition to balancing the conduction power loss among the switches, the total harmonic distortion (THD) of output current of the inverter also has been investigated. Therefore, the THD of the output phase current for the NPC three-level inverter using three SVM techniques have been presented.

As discussed before, in the present project, the PMSM is operating below the base speed region in which the modulation indices are less than 0.5. Therefore, the Fast Fourier Transform of the output phase current of the inverter has been presented for three different modulation indices; (m) = 0.15, 0.3 and 0.4. The parameters of the three-level inverter are as the following: DC-link voltage (V_{dc}) = 600 V, fundamental output voltage frequency (f) = 210 Hz, switching frequency (f_{sw}) = 12.6 kHz. The values have been obtained for 10 cycles of the output current for phase *A*. The results are presented in Table 5.13.

Table 5. 13: THD of output current for phase 'A'

Modulation index	*Methods*		
	Normal	***O2***	***O3***
0.15	11.98%	11.72%	11.70%
0.30	23.48%	23.17%	23.17%
0.40	30.97%	30.80%	30.70%

According to Table 5.13, for the modulation index (m) = 0.15, the O2 SVM method has reduced the THD of output current for 2.17% and O3 SVM strategy has decreased it for 2.34% and moreover, for modulation index (m) = 0.30, both methods, O2 and O3 SVM strategies have reduced the THD of output current for 1.32%. Finally, for modulation index (m) = 0.40, the changes in THD of output current are negligible for both methods. Hence, it can be inferred that regarding the THD decrement, both modified SVM methods are helpful to decrease the THD of the current supplying to the PMSM. Furthermore, O3 SVM is even more efficient than O2 SVM, because it can reduce the THD of output current greater than O2 SVM method. Table 5.14 is illustrates the behavior of methods in reducing the THD of output current of the three-level inverter.

Table 5. 14: Comparison of methods for THD of current

Modulation index	***Methods***
0.15	O3 SVM < O2 SVM < Normal SVM
0.30	O3 SVM = O2 SVM < Normal SVM
0.40	O3 SVM < O2 SVM < Normal SVM

5.6. CONCLUSION

According to the results presented in this chapter, it can be said that for a specific load angle and modulation index, O2 SVM method is efficient to reduce the conduction power losses of the inner switches and clamping diodes. Moreover, O3 SVM is an efficient method to decrease the conduction power losses of the outer switches and anti-parallel diodes. In addition, in order to reduce the THD of output current of the inverter, both methods, O2 and O3 SVM are efficient.

It is worthy to mention that there is a potential trade-off between the better balancing of the conduction power losses of the semiconductors and an increment in the total power losses of the inverter. For the first concern, the lifetime of the power devices and the inverter increases because none of the semiconductors is overloaded. On the other hand, if the total power losses in the inverter decreases, the mileage is increasing and one could drive with the available energy in the battery.

CHAPTER 6: CONCLUSION

6.1. SUMMARY

Nowadays, Electric Vehicle (EV) technology is an essential part of development in automotive industry. The drive train of an electric vehicle comprises two main elements; a motor and a power electronics converter. The electric motor provides the power by means of electrical to mechanical energy conversion. In order to control the speed and acceleration of the motor, there is a power controller that operates between the batteries and the motor. The converter transforms DC from the battery into AC for the motors.

In the present project, the conduction power losses of the semiconductors in a Neutral-Point Clamped (NPC) three-level inverter controlled with special Space Vector Modulation (SVM) methods has been studied. The inverter is supplying a PMSM in an electric vehicle. The SPMSM is operating in the region below the base speed. In this region, the modulation index as the most essential parameter in SVM strategy is less than 0.5. Therefore, the analysis has been constrained to the inner hexagon of the three-level SVM space vector plane.

In this condition, there is usually an unbalance of conduction power loss among the semiconductors in the three-level inverter. The inner switches typically present higher value of conduction power loss than the outer switches and for the clamping diodes, the conduction power loss is larger than that of anti-parallel diodes. In order to find an appropriate method for balancing the conduction power of devices, three SVM methods have been compared.

The Normal SVM, as the conventional method, consists of using all 7 state vectors in the state sequence, employed for synthesizing the rotating reference voltage vector that represents the desired three-phase voltages to be applied to the PMSM. In O2 and O3 SVM strategies, the proposed methods, by eliminating one or two zero state vectors, the dwelling time of the zero

voltage level based on either the inner or the outer switches of the inverter leg has been reduced in order to decrease the conduction power losses of devices that present higher conduction power losses. By implementing these three methods, primarily, the conduction duty cycle of the devices has been calculated to demonstrate the duration of conducting for each device. The larger the conduction duty cycle is, the higher the conduction power losses should be. In order to better compare the methods, the impact of modulation index and power factor on the conduction duty cycle of the devices has been investigated individually. This part of study has been conducted by coding in *MATLAB/M-File*.

Furthermore, the conduction power losses of the devices has been calculated in *MATLAB/Simulink*. In order to select the most appropriate method for balancing the conduction power loss of devices, the three presented methods of SVM have been implemented.

In addition, the index "conduction duty cycle" is introduced in order to anticipate the efficiency of the presented methods for balancing the conduction power losses of the devices. An easy approach for determining the "average conduction duty cycle of the semiconductors" is done for multiple cases to assess the conduction losses in the converter. This was verified by a conventional simulation, which is only useful for 1 case at the time. Moreover, the complete scheme for generating the gating signals of a 3-level 3-phase NPC converter for 3 different types of SVM in *MATLAB/Simulink* is implemented. It should be relatively easy to convert it to *Dspace* system for practical experimentation. Finally, the THD of output phase current of the three-level inverter has been calculated to investigate the impact of methods on the quality of the output current.

According to the results presented in Chapter 4, by implementing O2 SVM method, the conduction duty cycle of the inner switches and clamping diodes has been decreased. In addition, O3 SVM method has reduced the conduction duty cycle of the outer switches and anti-parallel

diodes. Nevertheless, in Normal SVM, the inner switches/clamping diodes present larger values of conduction power/duty cycle than the outer switches/anti-parallel diodes. Therefore, the selected method is effective in reducing the conduction power/duty cycle of the inner switches/clamping diodes.

For modulation index (m) equal to 0.0853 and load angle (φ) equal to -20.17°, O2 SVM strategy reduced the conduction duty cycle of the inner switches by *26.82%* and of the clamping diodes by *83.7%*. Conforming to the results presented in Chapter 5, with the help of O2 SVM method, the conduction power losses of the inner switches and clamping diodes has been reduced by *25.99%* and *83.27%* respectively.

In addition, when the modulation index (m) is 0.4863 and the load angle (φ) is -16.61°, O2 SVM method has reduced the conduction duty cycle of the inner switches by *1.93%* and the conduction power losses of this switch by about *1.6%*. To illustrate similar analysis for clamping diodes, O2 SVM has reduced the conduction duty cycle and conduction power by *7.13%* and *6.39%* respectively.

Regarding the decrement in THD of output phase current, both O2 and O3 SVM methods are effective. O2 SVM method has reduced the THD of current by about *0.55%-2.17%* and for O3 SVM, the decrement was about *0.87%-2.34%* for different modulation indices.

It can be deduced that for a NPC three-level inverter that supplies a PMSM in an electric vehicle, the heat balancing among semiconductors is essential in order to prolong the life cycle of the devices. When the PMSM is operating in the region below the base speed, there is an unbalance in conduction power of semiconductors. In order to better balance this inequality, O2 SVM strategy is the most appropriate method among the presented methods. Because this method helps to reduce the conduction power of switches that present higher value of conduction power loss. In

addition, O2 SVM strategy is also effective to decrease the THD of the output current that is supplied to the PMSM. Accordingly, for the operating condition of the PMSM connected to the NPC three-level inverter presented in this project, O2 SVM strategy is the most effective method for balancing the conduction power loss of switches and reducing THD of output current.

6.2. FUTURE WORKS

1- The junction temperature of devices in a three-level inverter is a significant parameter to determine the life cycle of devices and the operating range of the three-level inverter. It will be important to evaluate the junction temperature of devices in a NPC three-level inverter supplying a SPMSM.

2- As mentioned in Chapter 1, for a SPMSM, there are two operating regions: below the base speed and above that. In the present study, the effect of methods on balancing the conduction power of devices has been investigated while the motor is operating below the base speed. It will be valuable to analyze the efficiency of the proposed methods for the second operating region of the SPMSM which is above the base speed.

3- All the studies mentioned before are regarding an EV consuming the energy from the battery. While the EV needs to be charged, there is a regenerative braking process in which the electric motor starts to slow down the vehicle. In this situation, it will be useful to study the performance of the proposed methods for balancing the conduction power and junction temperature of devices in a NPC three-level inverter.

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