A Space Vector Modulation Scheme for Reduction of Dead-Time Effects on Common Mode Voltage of an Open End Winding Induction Machine

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Abstract

A Space Vector Modulation Scheme for Reduction of Dead-Time Effects on Common Mode Voltage of an Open End Winding Induction Machine

Nazli Kalantari

In recent times, the demand for high voltage and high current rating motor drives for electric vehicles applications has increased. These conditions place a great deal of stress on the semiconductor switches, which are usually based on silicon. Multilevel converters provide an alternative that reduces the stress on the switch and also improves the quality of the voltage output. On the other hand, 2-level power converters have proven to be reliable over a number of years. Therefore, they have been used as building blocks to achieve higher voltage and/or currents, by creating a multilevel effect to improve the quality of the voltage waveforms supplied to the motor. In this project, a power configuration with dual 2-level inverters supplying an Open End Winding Machine (OEWM) was studied.

This thesis investigates the Space Vector Modulation (SVM) switching strategy for an open end winding machine, fed by dual 2-level inverters. One DC voltage source is employed to feed the both inverters. In addition, the problem of Common Mode Voltage (CMV) in this configuration was discussed in depth and the cause of this problem was explored.

The existing SVM strategy to eliminate the CMV due to switching states was discussed in depth and it was modified in order to eliminate the effect of dead-time on the common mode voltages. The existing modulation strategy was adjusted to re-align the switching states according to the phase current direction in order to obtain a proper sequence. The proposed scheme is also applicable for n-level inverters.

The performance of the system under the proposed strategy in terms of current and voltage quality was investigated and duly presented. The studies were conducted in MATLAB/Simulink software in the time-domain. Loss calculation using PLECS toolbox is also provided in this thesis.

Acknowledgements

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Chapter 1

Introduction

Voltage source inverters are used in motor drive applications to enable the flow of power from electrical DC source to three phase AC load in the output. The DC source can be provided by a battery source, e.g. for electric vehicles, or having a rectifier to rectify the grid voltage. The magnitude and frequency of the AC output can be adjusted in order to meet the requirement of the machine in terms of the desired torque and speed and power.

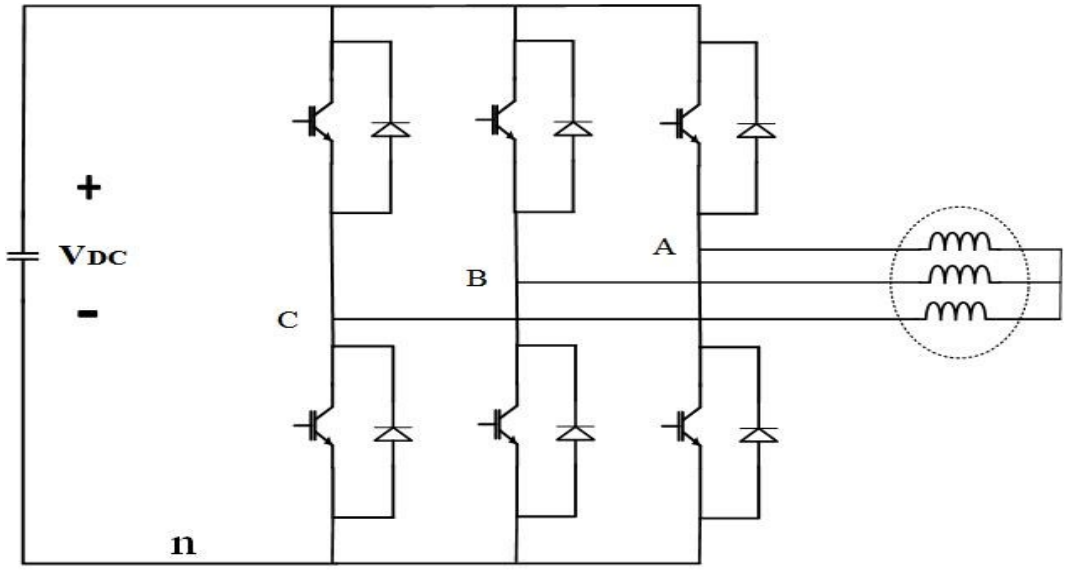


Figure 1.1. 2-level inverter

Fast switching power semiconductor devices such as Insulated Gate Bipolar Transistors (IGBT) are used in modern inverters. Control schemes are employed to control the

switching of the power switch devices in order to improve the performance and the efficiency of the load. The power switches have the advantage of being robust and having relatively low switching losses. However, the voltage rating of the switches are not sufficient to meet the requirements of some higher power applications. To meet high voltage and high power levels, multilevel voltage source configurations are employed. Voltage source inverters can be divided into two main categories based on the number of levels they can produce in the output voltage, 2-level and multilevel inverters.

The 2-level inverter is considered as the simplest drive to feed a three phase load. It consist of 6 power switches, Figure 1.1. A, B and C pole voltages can attain V_{DC} when the upper switch is on, and 0 with respect to the n point when the lower switch is turned on. The upper and lower switch in each leg are complementary to avoid short circuiting the voltage source. The two level inverter can produce overall 8 switching states (2^3).

1.1 Multilevel Inverters

Inverter are developed in such a way that they can create more than 2-levels, therefore the term multilevel is used to refer to these topologies. Multilevel inverters offer many advantages; they divide the dc voltage into the smaller steps in the output voltage. As number of levels in the phase voltage increase, the instantaneous phase voltage is closer to the reference output AC waveform therefore the quality of the AC voltage will be improved [1]-[3].

Multilevel converters allow higher voltage handling capability by utilization of series switching devices and also reduced harmonic distortion in the output waveform [4].

A brief introduction of the main multilevel inverter topologies has been presented in this part. There are three main type of the inverters that are commonly known as multilevel inverter, which are Neutral Point Clamped inverters (NPC), Flying Capacitor inverters and Cascaded H-bridge inverters. Along with these categories, there are number of derivative schemes which can be the combination of these categories [5]. Multilevel inversion is also attainable using two inverters feeding both ends of the machine; in this case machine

structure will be called open ended machine. A brief review of multilevel inverters is presented in this chapter and the main advantages and disadvantages are mentioned.

1.1.1 H-Bridge Inverter

H-bridge cell or full bridge inverter consists of four main semiconductor switches and four anti-parallel diodes. It is possible to obtain a multilevel waveform using series connections of these H-bridge cells which is known as Cascaded H-bridge inverter. In the figure below, general single phase m-level cascaded inverter is shown.

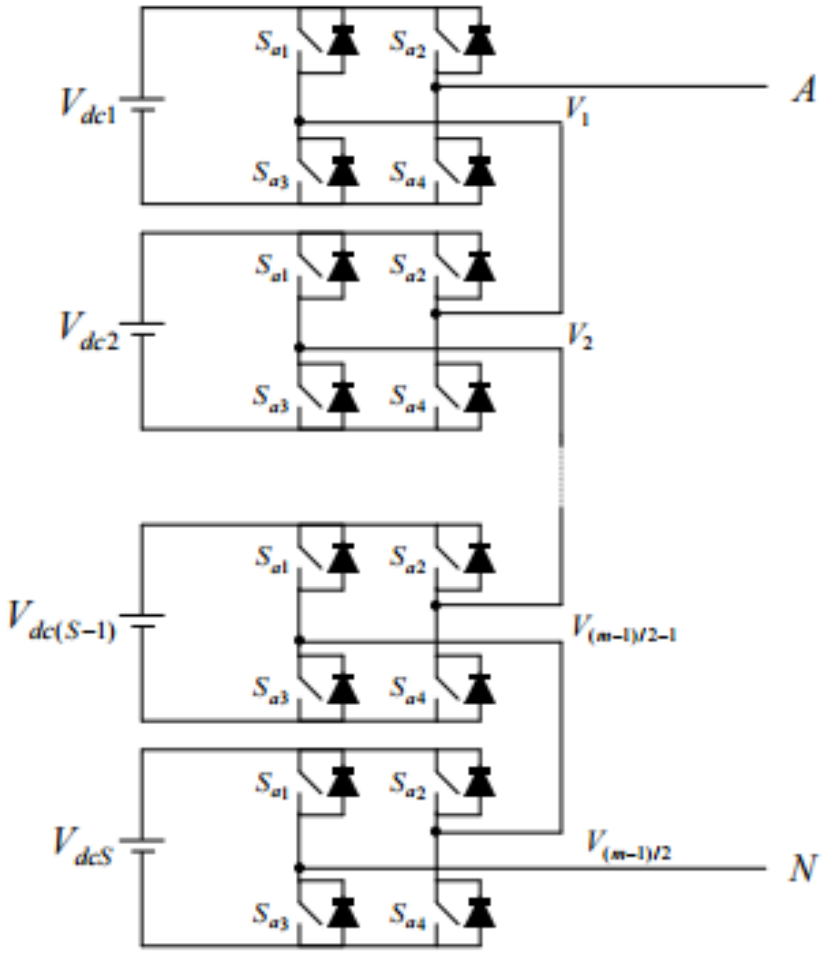


Figure 1.2. Single phase m-level cascaded inverter

Each inverter can produce three different voltage outputs, $+V_{DC}$, 0, and $-V_{DC}$. The overall output voltage is the sum of the individual inverters outputs [6]. The number of the levels of the output, m, can be related to the number of H-bridge cells, s, that are used as follows

$$m=2s+1 \tag{1.1}$$

The output voltage of the inverter is the addition of the output voltages of all units:

$$V_{AN} = V_1 + V_2 + \cdots + V_{(m-1)/2} \tag{1.2}$$

Each H-bridge unit has its own dc source, which is mostly an independent or isolated voltage source provided by transformer or batteries or fuel cells [7]. Each of the H-bridges are switching only at fundamental frequency. Cascade inverters are considered as a viable option for automotive electric motors since it can handle bidirectional real power flow and can operate in the regenerative region as well.

Advantages are

- The number of levels in the output voltage can be twice of the number of DC voltage sources.

Disadvantages are

- Separate dc sources are required for each of the h-bridge units therefore limited to the application where separate dc sources are available.

1.1.2 Flying Capacitor Inverter

The Flying Capacitor multilevel inverter came into existence in 1992 [8]. 3-level flying capacitor is shown in Figure 1.3. For the 3-level scheme two capacitors are needed to split the input dc voltage, and three other capacitors are needed as clamping capacitors [9]. Each leg can produce three voltage levels as + V_{DC}/2, 0, and - V_{DC}/2.

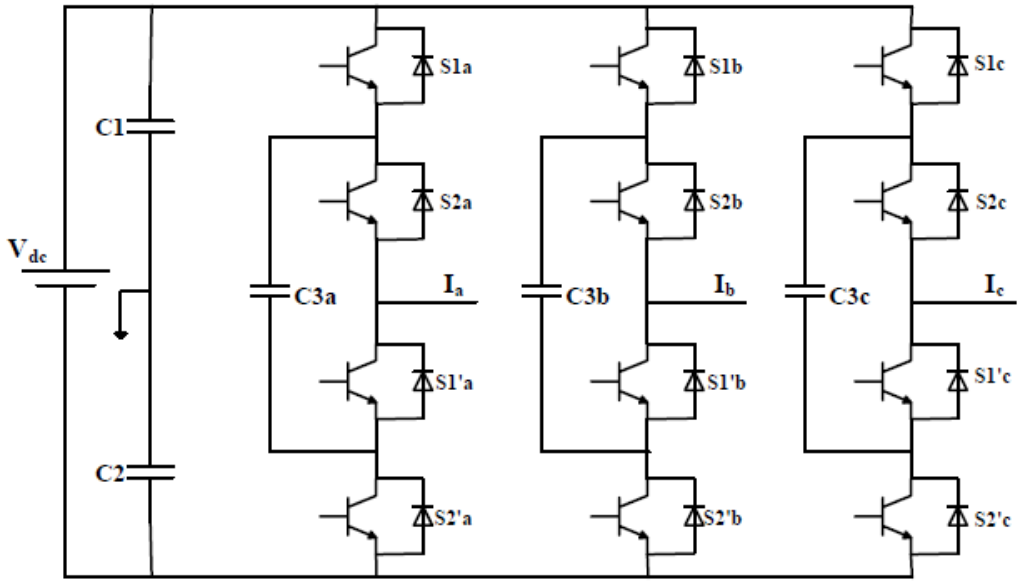


Figure 1.3. Three phase Capacitor-Clamped Multilevel Inverter

Advantages:

- Does not require isolated dc voltage sources.
- There exist switch redundancy for balancing the voltage levels.

Disadvantages:

- Increased number of capacitors needed to obtain higher levels, is costly and makes the system bulky.

1.1.3 N-Level Neutral-Point-Clamped (NPC) Inverter

Diode clamped inverter are commonly known as neutral point clamped inverter. This inverter was introduced near 30 years ago and is the most widely multilevel inverter used in all types of industrial applications [10]. 3-level inverter NPC is shown in Figure 1.4. The circuit consists of two series capacitors to divide the voltage of the dc source into smaller voltages. Switches (S1, S1') and (S2, S2') are complementary pairs in the given leg. Possible pole voltages are $+V_{DC}$, 0, and $-V_{DC}$.

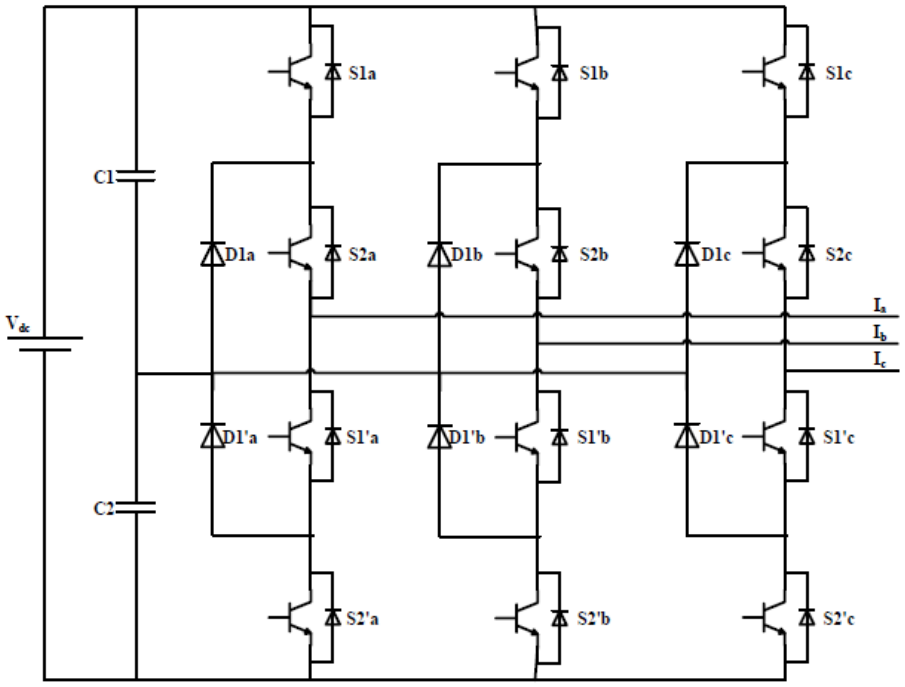


Figure 1.4. Three phase 3-level neutral point clamped inverter

Several techniques are suggested to ensure the equal capacitor voltages such as employing the proper redundant voltage states by [11]-[12].

As the number of level, m, increases, the number of diodes that is required will also increase, (m-1)(m-2) per phase. Each power device should be able to block a voltage level of ($\frac{V_{DC}}{m-1}$) [13].

Advantages:

- Reactive power flow can be controlled
- One dc bus is required
- High efficiency for fundamental switching frequency

Disadvantages:

- Large number of clamping diodes needed for higher levels

- Higher number of levels is possible in NPC structure, but the high losses and uneven distribution of the losses in the switching devices makes it less attractive [7]
- Voltage balancing techniques should be used to ensure equal voltage across the capacitors

1.1.4 Open End Winding Machine

The general idea of the Open Ended Winding Machine (OEWM) is to feed the machine from both terminals with separate inverters as it is shown in Figure 1.5. Feeding the both ends of the stator windings by two inverters were suggested by [14] in 1993. The start terminals of the windings are connected to one inverter, and the three end terminals can be connected to another inverter. Therefore, the phase voltage is formed by the voltages provided by both inverters. The choice of the inverter varies in different research works. Any three phase load can be connected to dual 2-level three phase inverters as shown in Figure 1.5.

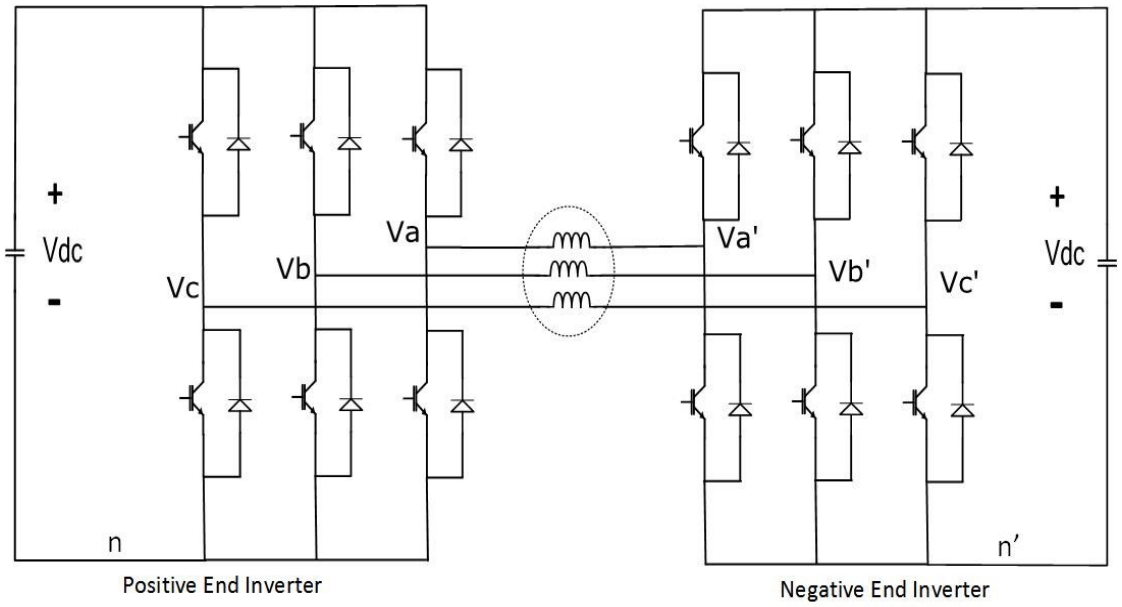


Figure 1.5. Open end winding configuration fed by dual 2-level inverters

The biggest advantage of OEWM, is that in most cases, no electrical or mechanical modification is needed to operate the very same machine which was previously operating in delta or star connection, in open end configuration, since most motors designed for high power applications are provided with all six terminals available externally in the terminal box. This was to facilitate the change in connection between delta and star configuration [15].

The choice of the individual inverters can be a well-known 2-level inverter [16]-[19]. The advantage of the 2-level inverter is that it has been commonly used in the industry and is well tested. Each of the 2-level inverters are capable of attaining 8 switching states independently, which results in overall 64 switching states when dual 2-level inverters are employed. These states provide the same space vector configuration as 3-level inverters, which is to be discussed in more details in the next chapter. Consequently, it is capable of providing more levels in the phase voltage than single 2-level inverter and therefore the quality of the waveform will be improved [20]-[24]. This can be an alternative to NPC and Cascaded multilevel inverters to gain more voltage levels in the output voltage. Several numbers of the space vectors in the space vector diagram of the OEWM are considered as redundant states since they are representing same voltage vector in the space vector configuration. Number of the redundant voltage vectors are increased in this scheme in comparison to that in the 3-level inverter; there exist 27 space vector combinations distributed in the 19 space vector locations, while for the dual 2-level 64 space vector combination located in the same space vector locations which results in more flexibility in selecting the proper switching state. Also in this configuration there is no need to enforce voltage balancing in the neutral point which is the case that should be considered in NPC inverters.

OEWM circuit configuration attracts the interests of many researchers owning to the fact that it is capable to provider higher ac voltage gain for a given dc input in comparison with employing only one inverter. This is because the voltage on the output is the result of the superposition of both inverters [23],[25]. Dual 2-level inverters connected to the OEWM will bring the ability to generate voltage waveforms from dc link source of half the magnitude, comparing to the same in conventional single 2-level inverter.

It is also possible to connect the individual inverters to unequal DC sources. In [26] the OEW load is connected to two unequal, isolated DC voltage sources. In this case the number of the levels on the AC-side of the load can be increased to four levels. As a modification to the open end winding structure is to supply the load by dual 2-level inverters which are fed by two isolated DC buses of different magnitudes [27], which expands the linear modulation range and also is capable to eliminate the 5^{th} and 7^{th} order harmonics throughout the modulation range.

Each of the two inverters can be controlled independently leading to a wide range of choices of control techniques in this inverter configuration. In [28] hybrid PWM control techniques were employed to control the two inverters independently in order to reduce the common mode voltage and therefore the motor shaft voltages.

In most open end schemes, electrically isolated power sources were used to eliminate the flow of zero sequence current from one inverter to the other. In case of only one DC power source, it should be ensured that the zero sequence currents are not circulating between two inverters. This circulating current increases the losses and has high frequency components. The corresponding voltage causes these circulating currents through the switches, can be eliminated using PWM modifications [25], [29]-[31]. Common mode filters, also, can eliminate these undesired currents when the two inverters are fed by the same dc source [32].

Auxiliary switches are added to the dual 2-level fed open end winding load and a proper control PWM switching strategy is proposed in [33] to suppress the zero sequence current without the need of bulky filters.

In [34] a space vector modulation is introduced to eliminate the circulating currents using specific switching states. It is shown that if each of the inverters produce the same common mode voltage, the overall zero sequence voltage will be eliminated thus the circulating current can be forced to zero. This method will cause reduction in the linear modulation region. In [30] it is shown that along with the switching states, there are two more factors that can contribute to the zero sequence currents in the windings, which are voltage drops and the dead-times in the gating signals of the switches. In [35] carrier based PWM is also

suggested to modulate the two inverters, eliminating the common mode voltage due to the switching states.

1.2 Modulation Strategies

Pulse Width Modulation (PWM) is used to control the pulses for the inverter switches to synthesize the ac voltage with the desirable frequency and amplitude [36]. There exist numerous PWM strategies in order to control different inverter topologies. The existing pulse width modulation to operate the voltage source inverters are classified into three major categories (i) selective harmonics elimination techniques, (ii) Carrier based PWM techniques (SPWM), and (iii) Space Vector Modulation techniques (SVM).

AC voltage created by PWM techniques at the machine terminals contain a desired fundamental frequency plus a number of higher frequency harmonics. In selective harmonic elimination method, most significant low order harmonics are eliminated by applying Fourier series analysis, consequently increase the quality of waveform. This modulation strategy provides narrow range of modulation index [37]. The main advantage of this modulation method is the low switching frequency of the switches, reducing the switch losses.

Carrier based PWM is one of the most popular modulation schemes used to control 2-level and multilevel inverters. In this technique modulating signal is a sine wave, which corresponds with the desired frequency and magnitude of the output voltage. This sinusoidal wave is compared with a triangular carrier, which controls the switching frequency of the devices. When the modulating signal is more than the carrier signal the output is 1, which means the switch should be turned on. In the three phase inverters the modulating signals are shifted by 120°. It is common that a sinusoidal third harmonic is injected to the modulating signal to obtain higher output voltage gain. In order to control multilevel inverters using carrier based modulation, several techniques has been developed such as multiple carriers or carrier dispositions to reduce the distortion in the output.

A very common technique to control multilevel inverters is Space Vector Modulation (SVM). SVM technique is an advanced PWM method used widely to realize the reference

phase voltages in three phase converters. Space vector concept is used to compute the value of duty cycle of the switches to synthesize the reference voltage. There are various switching state combinations in space vector modulation for a given scheme. SVPWM can be extended to all multilevel inverters. Each switching state can be depicted as a voltage vector according to the voltage it produces. Voltage vector redundancy in the SVM technique provides numerous advantages depending on the topology, such as flexibility to balance the capacitor voltage, reducing the common mode voltage, balancing the switching losses, etc. In this thesis, SVM technique is used to control the two inverters in order to provide high quality waveform and eliminate undesired voltages at the motor terminals.

1.3 Common Mode Voltage

One of the inherent characteristics of high frequency DC/AC converters is the formation of the common mode voltages at the machine terminals. Decrement of the rise and fall times in the power switches leads to fast switching transients in inverters, which can cause several problems in the machine terminals.

There are many small capacitive couplings exist in the motor drive system which can affect the performance of the machine in high frequencies. Interaction of the high frequency voltages with these capacitive coupling between the rotor and stator winding, also rotor and the frame, can cause undesired circulating currents through the machine. These leakage currents can cause damage to the bearings and shafts of the machine and also creates the problem of the electromagnetic interference [38]-[41]. Common mode voltages are considered as one of the side effects of high frequency PWM. High frequency harmonics at the machine terminals affect the parasitic capacitances and create the path for the current to flow through theses capacitances from the stator windings and rotor and then returns from the stator grounded body [42]-[45].

One of the main drawback of the open end configuration is the circulation of these common mode currents [25], [39]. In [30] three main causes of the common mode voltage in the OEWM has been identified: (i) switching states, (ii) dead-time in the drive circuit and (iii) voltage drop of the switches.

Employing SVM method to control the switching states of the open end winding machine, there exist specific voltage vectors that do not produce zero sequence voltages and hence employing these vectors results in the elimination of unwanted zero sequence currents. However the space voltage vectors situated at the vertices of the hexagon cannot be used, leading to reduced DC bus utilization.

In the ideal case, states of the two switches in an inverter leg change simultaneously in the complementary manner; in practice a short period of time is associated with turn off and turn on in the switch depending on the type of the switch. To avoid the cross conduction of the two switches in the same leg, it is necessary to predetermine a certain blank or dead-time in the control schemes of the power conversion device to turn on the other switch with some delay. This delay is known as the dead-time in the literature. Surprisingly the effect of the dead-time is not negligible and it can cause very high frequency pulses in the common mode voltage. The effect of dead time on the voltage waveform discussed in the literature and several compensation techniques are discussed [46]-[48].

1.4 Thesis Outline

The general motivation for this thesis was provided by the desire to examine the suggested modulation schemes for the open ended winding machines and improve the performance of the pulse width modulations. The main objective of this thesis is to propose a modified modulation scheme to avoid the common mode voltages due to the dead-time. The next 4 chapters of the thesis are organized as follows:

- Chapter 2 investigates open end winding configuration that is operated using dual 2-level inverters. The main problem in this configuration, the common mode voltage, is highlighted and the conventional solutions to eliminate the problem is introduced. It is discussed that the modulation strategy based solution is considered better option, since there is no need for adding extra devices to the system. Conventional space vector modulation schemes for CMV elimination in OEWM is introduced in details. It will be shown that this strategy does not consider the effect of dead time in the common mode voltage.

- Chapter 3 modifies the conventional modulation-based technique to cancel the common mode voltage disturbance. The proposed scheme attempts to eliminate the common mode voltage generated by dead-time in gating signals of the switches by realigning the switching states in the sequence of the space vector modulation.
- Chapter 4 analyzes the effectiveness of the proposed modulation scheme of chapter 3. A comparative study is performed between conventional scheme and the proposed schemes in time domain, using *MATLAB/Simulink*. Loss calculation of the switches is performed in order to study the effect of the modulation scheme on the switch loss balances.
- Chapter 5 concludes the thesis and highlights the contribution.

Chapter 2

Open End Winding Machines

2.1 Topology Description

In the previous Chapter, the open end configuration has been briefly introduced. It was stated that supplying the open end load with two distinct DC voltage sources is not convenient for electric vehicles, which usually employ single battery banks. In this topology, two standard three phase 2-level inverters are connected at both ends of the windings of the machine. This configuration can create phase voltages similar to those of 3-level inverter topologies on machine phase winding. Since 2-level inverters are widely commercialized, this can be an advantage of this topology since it does not require any new configurations. It also provides a better reliability in case of fault in one inverter, the ends connected to the faulty inverter can be shortened and the machine can still be supplied by the other side inverter. Using two inverters in this configuration offers higher degree of utilization of the DC side voltage, which will be explained in more details in Section 2.3.2. In order to better understand the basic principles behind the operation of the Open End Winding Machine (OEWM) fed by dual 2-level inverters, it is important to visualize the modulation schemes for a single 2-level inverter. Consequently, the overall output voltage of the dual 2-level inverter can be obtained by the principle of superposition of both the inverters. The space vector modulation scheme for dual 2-level inverter is investigated in the following sections.

2.2 Space Vector Representation in 2-Level Inverter

Pulse Width Modulation (PWM) is the process of modifying the width of the pulses of the switching devices to attain the desired reference voltages at the power terminals. The width of the pulses are modified to obtain output voltages whose average value is equal to the average of the reference signal during the PWM sampling cycle.

Space Vector Modulation (SVM) technique is an advanced PWM method used widely to realize the reference phase voltages in three phase converters. Space vector concept is used to calculate the duty cycle of the switches. There are various switching sequence combination that can realize the same reference voltage vector in space vector modulation scheme, that can result in reduced total harmonic distortion.

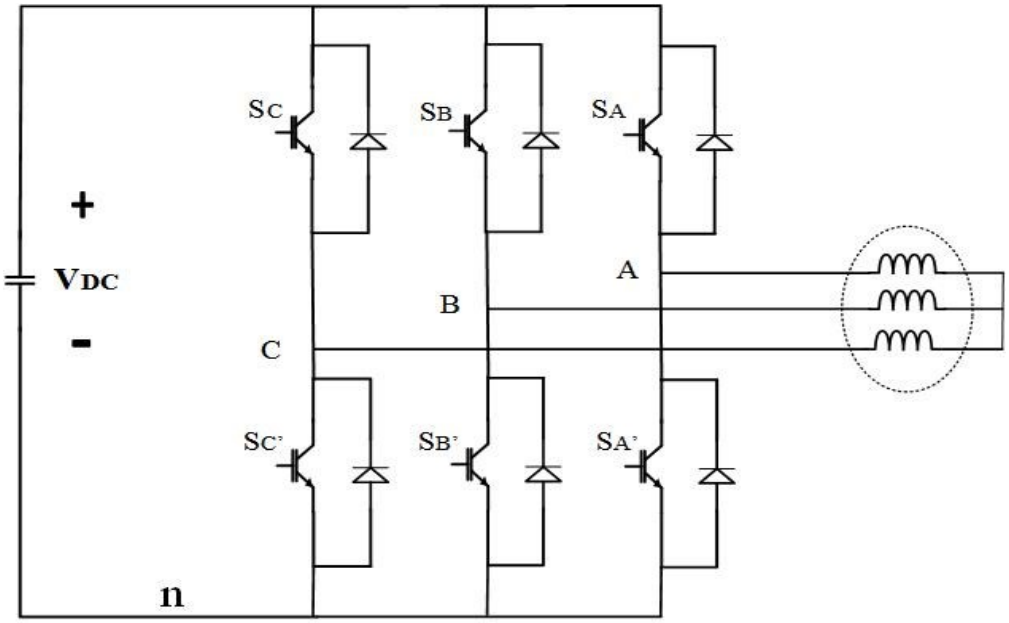


Figure 2.1. Typical 2-level inverter

Consider a typical 2-level inverter feeding a three phase star connected load of Figure 2.1, there are 6 switching devices: S_A, S_B, S_C, $S_{A'}$, $S_{B'}$, $S_{C'}$. In order to prevent short circuiting of the DC voltage source, the switches S_A and $S_{A'}$ are complementary in their gating signals. Similarly (S_B, $S_{B'}$) and (S_C, $S_{C'}$) are complementary pairs. Voltages of V_{An}, V_{Bn} and V_{Cn} are considered as pole voltages of the inverter. The pole voltage can attain 2 values in 2-level inverter; for instance in leg A, V_{An} can attain $+V_{DC}$ when S_A is on ($S_{A'}$ is off) and

0 when $S_{A'}$ is on (S_A is of). Therefore each leg can attain only 2 states, consequently the three legs of the inverter can produce overall 8 (2^3) switching states.

In the SVM technique, the output voltage of the inverter can be represented in a graphical structure, namely voltage Space Vector (SV) diagram. All the switching states of the 2-level inverter can produce a specific voltage output, which can be represented as voltage space vectors in SV diagram. Equation (2.1) represents stator space voltage vector, $\vec{V_s}$.

$$\vec{V_s} = V_{An} + (V_{Bn} \times e^{j\frac{2\pi}{3}}) + (V_{Cn} \times e^{j\frac{4\pi}{3}}) \tag{2.1}$$

where V_{An}, V_{Bn}, and V_{Cn} are the pole voltages of the inverter. This equation transforms the three phase values to a vector $\vec{V_s}$. As it can be noted from equation (2.1), the space vectors are complex numbers. The real part is the component along with the phase A-axis and the imaginary component is orthogonal to the A-axis.

Table 2-1. Switching states of a 2-level inverter and their corresponding space vectors

Switching States of the Inverter	**S_A**	**S_B**	**S_C**	**Space Vector**
0(000)	off	off	off	0
1(100)	on	off	off	$V_{DC}\angle 0$
2(110)	on	on	off	$V_{DC}\angle \frac{\pi}{3}$
3(010)	off	on	off	$V_{DC}\angle \frac{2\pi}{3}$
4(011)	off	on	on	$V_{DC}\angle \pi$
5(001)	off	off	on	$V_{DC}\angle \frac{4\pi}{3}$
6(101)	on	off	on	$V_{DC}\angle \frac{5\pi}{3}$
7(111)	on	on	on	0

Table 2.1 presents all possible switching states of the 2-level inverter and their corresponding voltage space vectors computed by equation (2.1). In this Table, the numbers 0 or 1 is used to show the state of the upper switch of the three legs of the inverter, leg A, leg B or leg C respectively. For instance, switching state (110) means that the upper switch of leg A and B are on, while the upper switch of leg C is off.

For the purpose of simplicity, the switching states are named as numbers between 0-7. Six of these switching states are considered as active vectors, namely 1(100), 2(110), 3(010), 4(011), 5(001), and 6(101). States 0(000) and 7(111) are considered as null or zero vectors. In such a case, there is no power flow between source and load and the load current free-wheels through the inverter. The length of active vectors are equal to V_{DC}, and for the zero vectors it is zero.

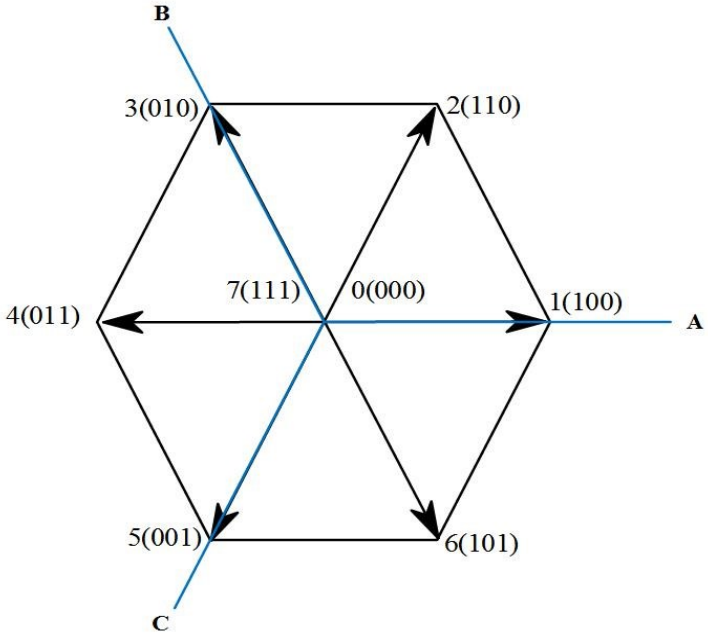


Figure 2.2. Space vector diagram of a 2-level inverter

Figure 2.2 demonstrates the space vector diagram of a 2-level inverter formed by SVs presented in Table 2. 1 along with the three phase axes A, B and C. The voltage vectors form a hexagon at the origin of the plane, and divide the plane into six 60° sectors.

2.3 Space Vector PWM in Open End Winding Scheme

The power circuit of a dual 2-level inverter configuration, supplying a three phase open end winding machine, is shown in Figure 2.3, employing a single DC voltage source to feed power to both inverters. To differentiate the inverters in this thesis, the inverter on the left is called positive end inverter, and the one on right is called negative end inverter.

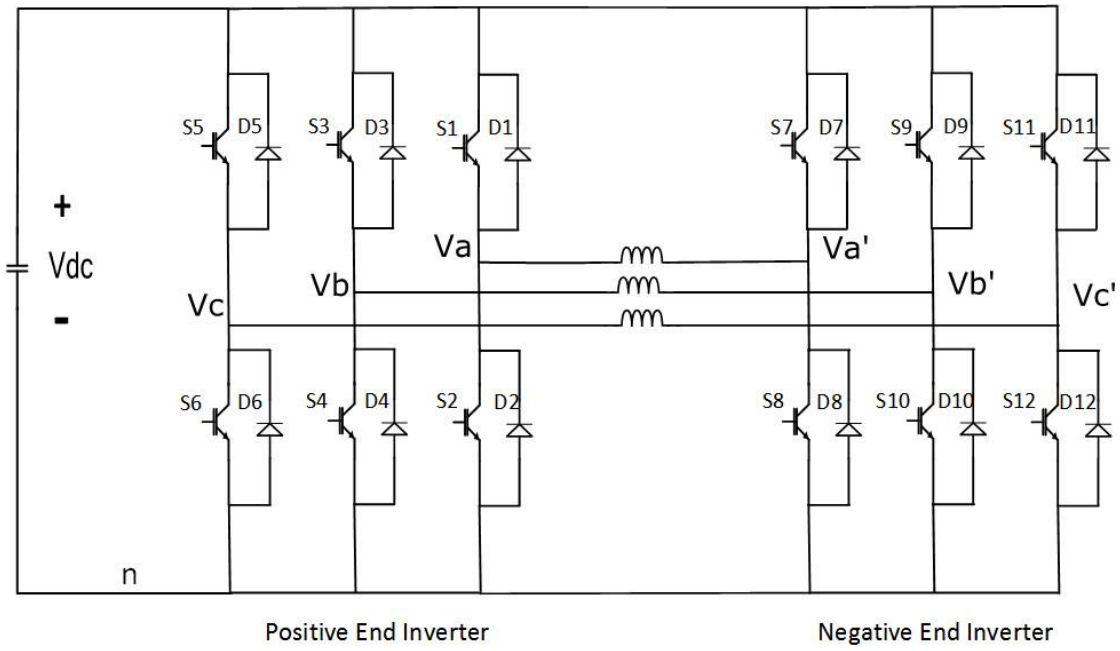


Figure 2.3. Open end winding machine fed by dual 2-level inverters

To obtain proper quality of the output voltage, the inverters should be capable of rapid switching, therefore the inverter requires high-power high-frequency components such as IGBTs. Twelve IGBTs, S1-S12, are employed along with antiparallel diodes, D1-D12. The top and bottom switches are switched complementarily in both inverters, Figure 2.3. In this circuit configuration, all the pole voltages can attain a voltage of V_{DC} with reference to the point n, if the top switch of that leg is on, otherwise it attains 0V.

2.3.1 Space Vector Plane and Voltage Vectors

In the previous sections, the space vector structure for a single 2-level inverter was explained briefly. In this section, the effect of both inverters on the open end winding machine is explained using the principle of superposition.

The 2-level inverters employed in the open end winding load, Figure 2.3, have independent switching states. Each inverter comprises 6 switches arranged in three inverter legs, which works complementarily in pairs, therefore there are 3 independent switching states and eight possible "switching states" in each individual 2-level inverter. Table 2.2 summarizes the switching states for the individual inverters used in open end winding machine.

Table 2-2. Switching states in dual 2-level inverter

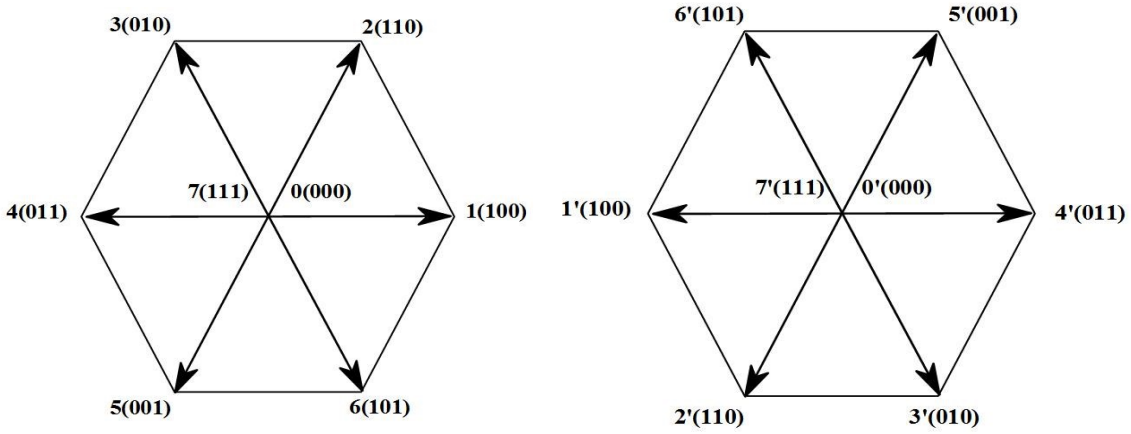
Switching States of Inverter 1	Switches turned on	Switching States of inverter 2	Switches turned on
0(000)	**S2,S4,S6**	**0'(000)**	**S8,S10,S112**
1(100)	**S1,S4,S6**	**1'(100)**	**S7,S10,S12**
2(110)	**S1,S3,S6**	**2'(110)**	**S7,S9,S12**
3(010)	**S2,S3,S6**	**3'(010)**	**S8,S9,S12**
4(011)	**S2,S3,S5**	**4'(011)**	**S8,S9,S11**
5(001)	**S2,S4,S5**	**5'(001)**	**S8,S10,S11**
6(101)	**S1,S4,S5**	**6'(101)**	**S7,S10,S11**
7(111)	**S1,S3,S5**	**7'(111)**	**S7,S9,S11**

Using Kirchhoff's Voltage Law (KVL) in Figure 2.3, one can obtain the three phase voltages as following

$$\begin{aligned} v_{aa'} &= v_{an} - v_{a'n} \\ v_{bb'} &= v_{bn} - v_{b'n} \\ v_{cc'} &= v_{cn} - v_{c'n} \end{aligned} \tag{2.2}$$

where $\upsilon_{an}, \upsilon_{bn}, \upsilon_{cn}$ are the pole voltages of the positive end inverter and $\upsilon_{a'n}, \upsilon_{b'n}, \upsilon_{c'n}$ are the pole voltages of the negative end inverter and $\upsilon_{aa'}, \upsilon_{bb'}, \upsilon_{cc'}$ are the three phase voltages.

As it can be noted from the equation 2.2, the pole voltages of the negative end inverter ($V_{a'n}$, $V_{b'n,}$ and $V_{c'n}$) directly oppose the pole voltages of the positive end inverter. This opposition which is seen by the load, can be represented in the space vector diagram of the negative end inverter. In the interest of simplicity, the space voltage vectors of the negative end inverter are drawn with same magnitude but in the opposite direction, to consider the effect of negative sign of the equation into the space vector structure.



(a) (b)

Figure 2.4. Space vector diagram for (a) positive end inverter and (b) negative end inverter

The resultant space vectors of the dual two level inverter is the sum of the space vector of both inverters seen by the motor.

$$\vec{V_s} = \upsilon_{aa'} e^{j0} + \upsilon_{bb'} e^{j\frac{2\pi}{3}} + \upsilon_{cc'} e^{j\frac{4\pi}{3}} \tag{2.3}$$

The resultant SV locations of the dual 2-level scheme can be obtained by adding the two space vector diagrams of Figure 2.4. As an example, consider the case that the positive end inverter attains the state of 2(110) and the negative end inverter attains the state of 6(101), the resultant vector is presented as 26'. To find the location of the vector 26', the two voltage vectors should be added. Figure 2.5 demonstrates this procedure.

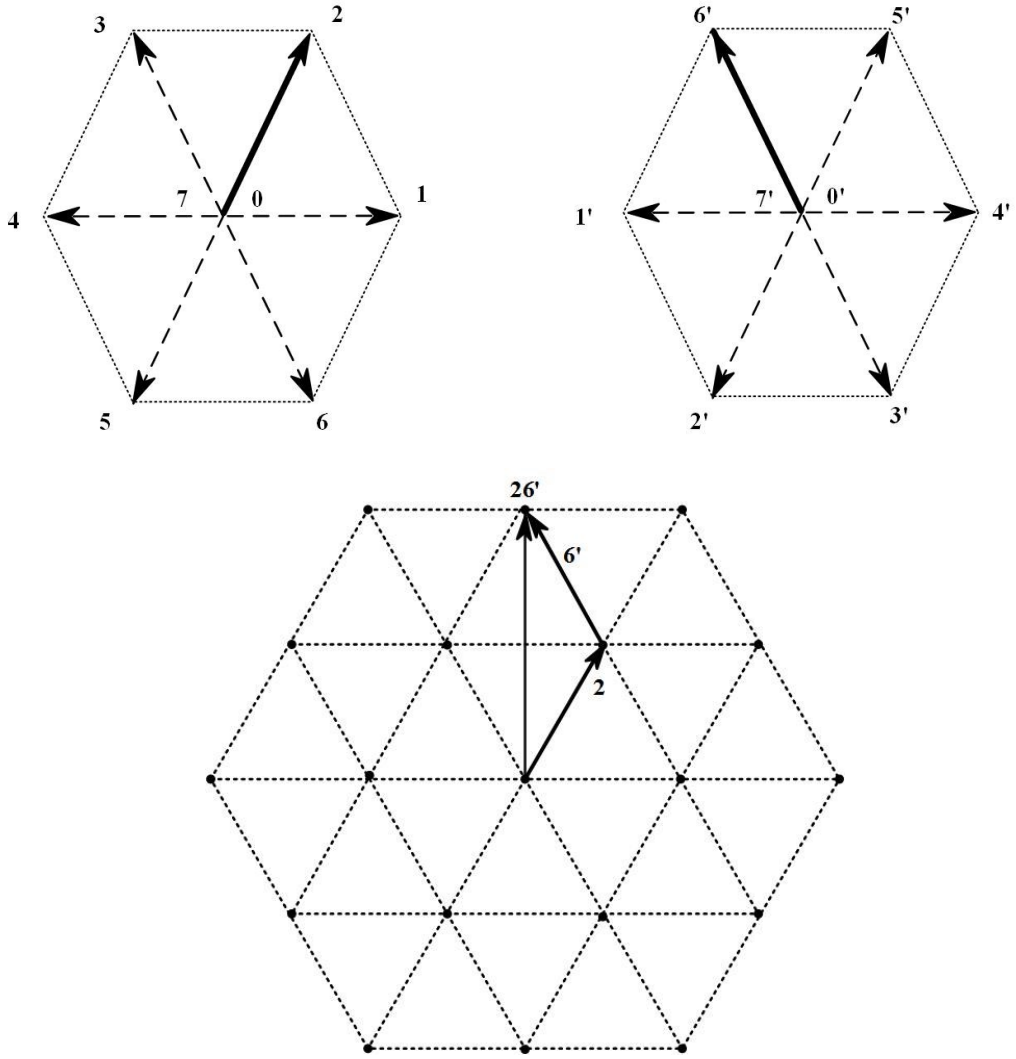


Figure 2.5. SV location when switching states of the positive and negative end inverters are 2 and 6' respectively

All the SV locations can be obtained with the same procedure of adding the individual SVs of both inverters. In Figure 2.6 the SV scheme is presented with all the possible active and zero vectors attainable in the corresponding OEWM.

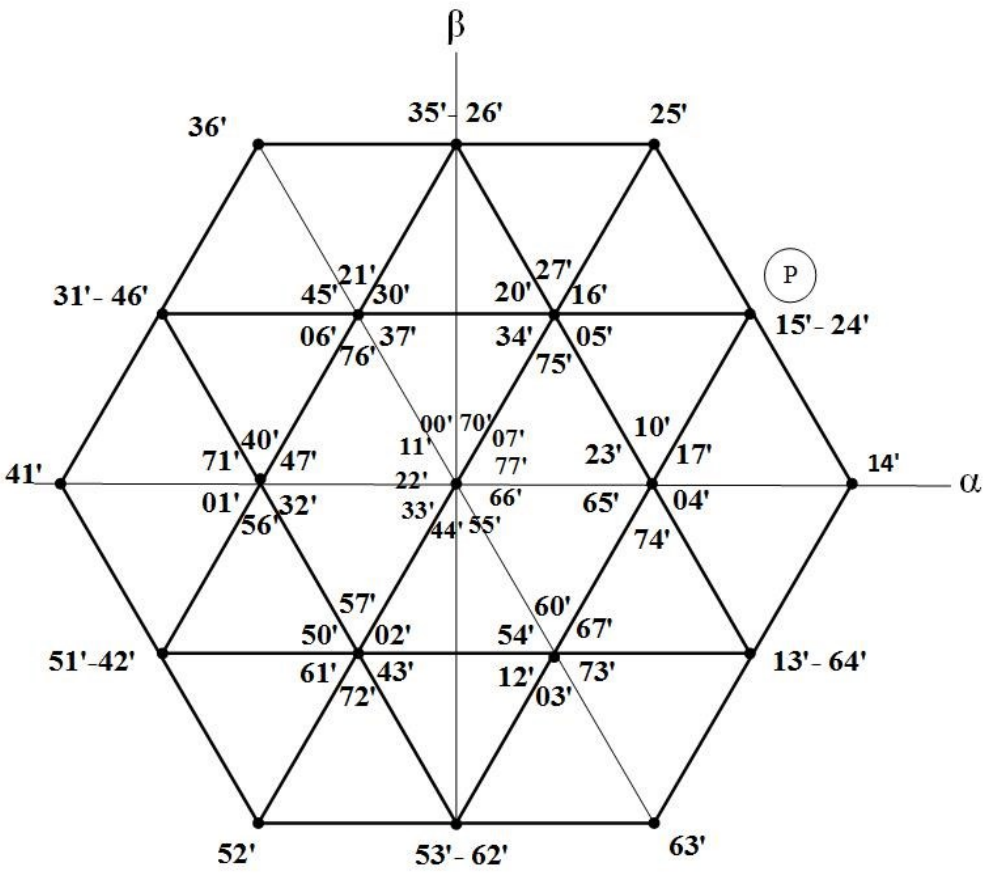


Figure 2.6. Space vector diagram of the dual 2-level scheme with all possible SVs

This space vector diagram consists of 64 space vector combinations distributed over 19 space vector locations. The active vectors divide the plane into 24 sub-triangles.

There exist 10 null or zero vectors located in the origin of the αβ plane and 54 active vectors. Out of the 54 active voltage vectors, 36 are small, which have length of V_{DC}, 12 are medium with the length of $\sqrt{3}V_{DC}$ and 6 are the large voltage vectors with the length of $2V_{DC}$ as shown in Table 2.3.

Table 2-3. Magnitude of the space vectors in dual 2-level inverter

	Switching vector combinations	Voltage level in SV Plane
Zero Vectors	**70'-07'-00'-11'-22'-33'-44'-55'-66'-77'**	**0**
Small Vectors	**17'-10'-23'-04'-74'-65'-16'-27'-20'-34'-75'-05'-30'-21'-45'-06'-76'-37'-47'-40'-71'-01'-56'-32'-02'-57'-50'-61'-72'-43'-67'-60'-54'-12'-03'-73'**	V_{DC}
Medium Vectors	**15'-24'-35'-26'-31'-46'-42'-51'-53'-62'-13'-64'**	$\sqrt{3}V_{DC}$
Large Vectors	**14'-25'-36'-41'-52'-63'**	$2V_{DC}$

Table 2.4 presents all the voltage vectors and the states of the corresponding switches in both inverters.

Table 2-4. All possible switching states and their corresponding SV in the OEWM

n	Switch S1	Switch S3	Switch S5	Switch S7	Switch S9	Switch S11	Magnitude and Position	Name
0	**0**	**0**	**0**	**0**	**0**	**0**	$0\angle 0$	**00'**
1	**1**	**0**	**0**	**0**	**0**	**0**	$V_{DC}\angle 0$	**10'**
2	**1**	**1**	**0**	**0**	**0**	**0**	$V_{DC}\angle \frac{\pi}{3}$	**20'**
3	**0**	**1**	**0**	**0**	**0**	**0**	$V_{DC}\angle \frac{2\pi}{3}$	**30'**
4	**0**	**1**	**1**	**0**	**0**	**0**	$V_{DC}\angle \pi$	**40'**
5	**0**	**0**	**1**	**0**	**0**	**0**	$V_{DC}\angle \frac{4\pi}{3}$	**50'**
6	**1**	**0**	**1**	**0**	**0**	**0**	$V_{DC}\angle \frac{5\pi}{3}$	**60'**

7	**1**	**1**	**1**	**0**	**0**	**0**	$0\angle 0$	**70'**
8	**0**	**0**	**0**	**1**	**0**	**0**	$V_{DC}\angle\pi$	**01'**
9	**1**	**0**	**0**	**1**	**0**	**0**	$0\angle 0$	**11'**
10	**1**	**1**	**0**	**1**	**0**	**0**	$V_{DC}\angle\frac{2\pi}{3}$	**21'**
11	**0**	**1**	**0**	**1**	**0**	**0**	$\sqrt{3}V_{DC}\angle\frac{5\pi}{6}$	**31'**
12	**0**	**1**	**1**	**1**	**0**	**0**	$2V_{DC}\angle\pi$	**41'**
13	**0**	**0**	**1**	**1**	**0**	**0**	$\sqrt{3}V_{DC}\angle\frac{7\pi}{6}$	**51'**
14	**1**	**0**	**1**	**1**	**0**	**0**	$V_{DC}\angle\frac{4\pi}{3}$	**61'**
15	**1**	**1**	**1**	**1**	**0**	**0**	$V_{DC}\angle\pi$	**71'**
16	**0**	**0**	**0**	**1**	**1**	**0**	$V_{DC}\angle\frac{4\pi}{3}$	**02'**
17	**1**	**0**	**0**	**1**	**1**	**0**	$V_{DC}\angle\frac{5\pi}{3}$	**12'**
18	**1**	**1**	**0**	**1**	**1**	**0**	$0\angle 0$	**22'**
19	**0**	**1**	**0**	**1**	**1**	**0**	$V_{DC}\angle\pi$	**32'**
20	**0**	**1**	**1**	**1**	**1**	**0**	$\sqrt{3}V_{DC}\angle\frac{7\pi}{6}$	**42'**
21	**0**	**0**	**1**	**1**	**1**	**0**	$2V_{DC}\angle\frac{4\pi}{3}$	**52'**
22	**1**	**0**	**1**	**1**	**1**	**0**	$\sqrt{3}V_{DC}\angle\frac{3\pi}{2}$	**62'**
23	**1**	**1**	**1**	**1**	**1**	**0**	$V_{DC}\angle\frac{4\pi}{3}$	**72'**
24	**0**	**0**	**0**	**0**	**1**	**0**	$V_{DC}\angle\frac{5\pi}{3}$	**03'**
25	**1**	**0**	**0**	**0**	**1**	**0**	$\sqrt{3}V_{DC}\angle\frac{11\pi}{6}$	**13'**

26	**1**	**1**	**0**	**0**	**1**	**0**	$V_{DC}\angle 0$	**23'**
27	**0**	**1**	**0**	**0**	**1**	**0**	$0\angle 0$	**33'**
28	**0**	**1**	**1**	**0**	**1**	**0**	$V_{DC}\angle \frac{4\pi}{3}$	**43'**
29	**0**	**0**	**1**	**0**	**1**	**0**	$\sqrt{3}V_{DC}\angle \frac{3\pi}{2}$	**53'**
30	**1**	**0**	**1**	**0**	**1**	**0**	$2V_{DC}\angle \frac{5\pi}{3}$	**63'**
31	**1**	**1**	**1**	**0**	**1**	**0**	$V_{DC}\angle \frac{5\pi}{3}$	**73'**
32	**0**	**0**	**0**	**0**	**1**	**1**	$V_{DC}\angle 0$	**04'**
33	**1**	**0**	**0**	**0**	**1**	**1**	$2V_{DC}\angle 0$	**14'**
34	**1**	**1**	**0**	**0**	**1**	**1**	$\sqrt{3}V_{DC}\angle \frac{\pi}{6}$	**24'**
35	**0**	**1**	**0**	**0**	**1**	**1**	$V_{DC}\angle \frac{\pi}{3}$	**34'**
36	**0**	**1**	**1**	**0**	**1**	**1**	$0\angle 0$	**44'**
37	**0**	**0**	**1**	**0**	**1**	**1**	$V_{DC}\angle \frac{5\pi}{3}$	**54'**
38	**1**	**0**	**1**	**0**	**1**	**1**	$\sqrt{3}V_{DC}\angle \frac{11\pi}{6}$	**64'**
39	**1**	**1**	**1**	**0**	**1**	**1**	$V_{DC}\angle 0$	**74'**
40	**0**	**0**	**0**	**0**	**0**	**1**	$V_{DC}\angle \frac{\pi}{3}$	**05'**
41	**1**	**0**	**0**	**0**	**0**	**1**	$\sqrt{3}V_{DC}\angle \frac{\pi}{6}$	**15'**
42	**1**	**1**	**0**	**0**	**0**	**1**	$2V_{DC}\angle \frac{\pi}{3}$	**25'**
43	**0**	**1**	**0**	**0**	**0**	**1**	$\sqrt{3}V_{DC}\angle \frac{\pi}{2}$	**35'**
44	**0**	**1**	**1**	**0**	**0**	**1**	$V_{DC}\angle \frac{2\pi}{3}$	**45'**
45	**0**	**0**	**1**	**0**	**0**	**1**	$0\angle 0$	**55'**

46	**1**	**0**	**1**	**0**	**0**	**1**	$V_{DC}\angle 0$	**65'**
47	**1**	**1**	**1**	**0**	**0**	**1**	$V_{DC}\angle \frac{\pi}{3}$	**75'**
48	**0**	**0**	**0**	**1**	**0**	**1**	$V_{DC}\angle \frac{2\pi}{3}$	**06'**
49	**1**	**0**	**0**	**1**	**0**	**1**	$V_{DC}\angle \frac{\pi}{3}$	**16'**
50	**1**	**1**	**0**	**1**	**0**	**1**	$\sqrt{3}V_{DC}\angle \frac{\pi}{2}$	**26'**
51	**0**	**1**	**0**	**1**	**0**	**1**	$2V_{DC}\angle \frac{2\pi}{3}$	**36'**
52	**0**	**1**	**1**	**1**	**0**	**1**	$\sqrt{3}V_{DC}\angle \frac{5\pi}{6}$	**46'**
53	**0**	**0**	**1**	**1**	**0**	**1**	$V_{DC}\angle \pi$	**56'**
54	**1**	**0**	**1**	**1**	**0**	**1**	$0\angle 0$	**66'**
55	**1**	**1**	**1**	**1**	**0**	**1**	$V_{DC}\angle \frac{2\pi}{3}$	**76'**
56	**0**	**0**	**0**	**1**	**1**	**1**	$0\angle 0$	**07'**
57	**1**	**0**	**0**	**1**	**1**	**1**	$V_{DC}\angle 0$	**17'**
58	**1**	**1**	**0**	**1**	**1**	**1**	$V_{DC}\angle \frac{\pi}{3}$	**27'**
59	**0**	**1**	**0**	**1**	**1**	**1**	$V_{DC}\angle \frac{2\pi}{3}$	**37'**
60	**0**	**1**	**1**	**1**	**1**	**1**	$V_{DC}\angle \pi$	**47'**
61	**0**	**0**	**1**	**1**	**1**	**1**	$V_{DC}\angle \frac{4\pi}{3}$	**57'**
62	**1**	**0**	**1**	**1**	**1**	**1**	$V_{DC}\angle \frac{5\pi}{3}$	**67'**
63	**1**	**1**	**1**	**1**	**1**	**1**	$0\angle 0$	**77'**

2.3.2 Redundant Switching Vectors

Redundant switching states are referred to different switching states which result in the same voltage space vector. The number of states that the dual 2-level inverter can assume is 64. From the SV diagram presented in Figure 2.6, one can note that the redundancy of the space vectors for space vector locations. For example the point 'P' in Figure 2.6 can be obtained by different vector combinations of 24' and 15'.

It can be noted that the space vector scheme shown in Figure 2.6 is similar to that of a 3-level inverter. The SV diagram of the open end scheme consists of 64 voltage vectors while in the 3-level NPC inverter there exists only 27 voltage vectors. Therefore open end winding machine using dual 2-level inverters has more redundant states in comparison to a 3-level NPC and it can provide more flexibility in controlling the phase voltages. Moreover, the magnitude of the large SVs is twice the length of the large active vector in the conventional 3-level NPC. For example the large SV of 14' in Figure 2.6 has the amplitude of $2V_{DC}$, as opposed to the amplitude of V_{DC} in the case of 3-level NPC that demonstrates the higher gain of the dual 2-level inverter configuration.

Since the space vector plane in this configuration assumes higher switching state redundancy, it can provide a higher degree of flexibility to reach a given objective such as providing a better THD or shifting power losses from one switch to another.

2.4 Common Mode Voltage

Pulse width modulated voltage source inverters suffer from common mode voltage issue, which has been reported to cause many problems such as generating voltages on the shaft and bearings and the consequential damage to the motor bearings [44],[49]. Interaction of the common mode voltage and the parasitic capacitances between stator winding and motor frame causes undesired circulating currents. High variation in the common mode voltage causes the parasitic capacitances in the machine to create a path for the current to flow.

Even though high frequency switching results in better harmonic profile and better dynamic performance for the drive system, it also enlarges the common mode voltages

across the machine terminals. Since the voltage source inverter cannot produce pure sinusoidal voltage waveforms, the sharp edged PWM pulses can create unwanted voltages at the machine terminals. Recent developments in power switches technology has led to significant decrement of the rise and fall times during the switching, Figure 2.7. In high-power applications, a change in voltage occurs during this short span of time. The rise/fall time is very short, therefore the high rate of change of voltage, $\frac{dv}{dt}$, generates stress across the machine terminals. In this interval, $\frac{dv}{dt}$ can produce a significant current in interaction with many parasitic capacitive couplings of the machine.

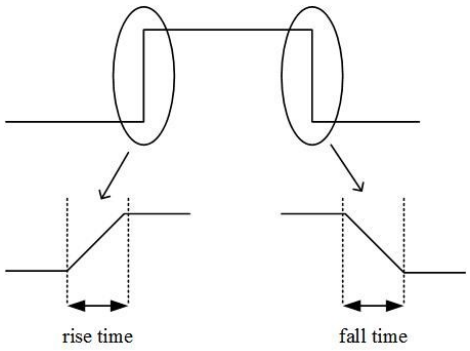


Figure 2.7. Rise and fall time of the switches

In a star-connected machine, common mode voltage is defined as the voltage between the neutral point of the machine and the ground of the system [43]. In open end winding machine configuration, defining the common mode voltage of each side

$$v_{CM-P} = \frac{v_{an} + v_{bn} + v_{cn}}{3}$$
$$v_{CM-N} = \frac{v_{an'} + v_{bn'} + v_{cn'}}{3} \tag{2.4}$$

the common mode in open end winding machine is defined as [30], [34]

$$v_{CM} = v_{CM-P} - v_{CM-N} \tag{2.5}$$

CMV in open end winding configuration can produce a circulating currents through the inverters. This problem does not appear when the dc sources are isolated [52], because the CM current do not have path to circulate, but when the inverters are connected through a

single source, the common mode voltage should be taken care of to avoid the common mode currents. In the case of single DC voltage source, common mode voltages result in the zero sequence currents through the load and switches, which is considered as a serious drawback of this configuration. In this case, the zero sequence current will flow into the load and increase the rms value of the current without any contribution to the delivered power [30]. The meaning of the equation (2.5) is that if the common mode voltage of the both ends are not equal, there will be a zero sequence current circulating through the windings.

The common mode voltage in this configuration can be obtained as

$$v_{CM} = \frac{v_{an} + v_{bn} + v_{cn}}{3} - \frac{v_{a\prime n} + v_{b\prime n} + v_{c\prime n}}{3}$$
$$v_{CM} = \frac{v_{aa\prime} + v_{bb\prime} + v_{cc\prime}}{3} \tag{2.6}$$

There are three major reasons for building the zero sequence current in the open end machine which will be discussed in the next sections. As it was discussed earlier, common mode voltage introduces numerous problems in electrical systems; this voltage can damage the motor insulation and induce destructive bearing currents. Therefore, it is important to study and prevent the effect of the common mode voltage on open end winding machines. In the following sections, the most dominant factors in creating the common mode voltage are discussed.

2.4.1 CMV Associated with the Choice of Switching States

Fluctuation of the common mode voltage is mostly related to the inverter states and the switching frequency. For example if the switching state of the three legs in one inverter changes from 110 to 100, the common mode voltage of this inverter will change from $\frac{2V_{DC}}{3}$ to $\frac{V_{DC}}{3}$. This variation occurs several times in every switching cycle, therefore the frequency of the fluctuation in the common mode voltage is directly dependent on the switching frequency and the magnitude is dependent on the choice of voltage space vectors.

The instantaneous values of the CMV of each inverter for all SVs are obtained by equation (2.6) and shown in Table 2.5. The values of the common mode voltage varies between 0, $\frac{V_{DC}}{3}$, $\frac{2V_{DC}}{3}$ and V_{DC} in this configuration. The maximum peak value is associated with zero vector of 7(111) in which all the upper switches in legs a and b and c are turned on. All the odd vectors will produce common mode voltage of $\frac{V_{DC}}{3}$ and all the even vectors, $\frac{2V_{DC}}{3}$.

The modulation strategy will dictate the sequence of the inverter states. Consequently, it is possible to alter the common mode voltage fluctuation by changing the modulation strategy to reduce or eliminate the common mode current. Peak value minimization can be done by proper vector selection.

Table 2-5. CMV associated with each of SVs

SV	V_{CM}
1(100), 3(010) and 5(001)	$\frac{V_{DC}}{3}$
2(110), 4(011) and 6(101)	$\frac{2V_{DC}}{3}$
0(000)	0
7(111)	V_{DC}

2.4.2 CMV Associated with Non-Ideal Characteristics of the Switching Devices

In practice, inverters employ non-ideal switches which create voltage drop when the switch is in on-state. The voltage drop on the power semiconductor devices can create common mode voltage at the machine terminals [30]. Since the voltage created by this feature is almost negligible in comparison with other factors, in this Thesis, the effect of non-ideal characteristic of the switch is not considered.

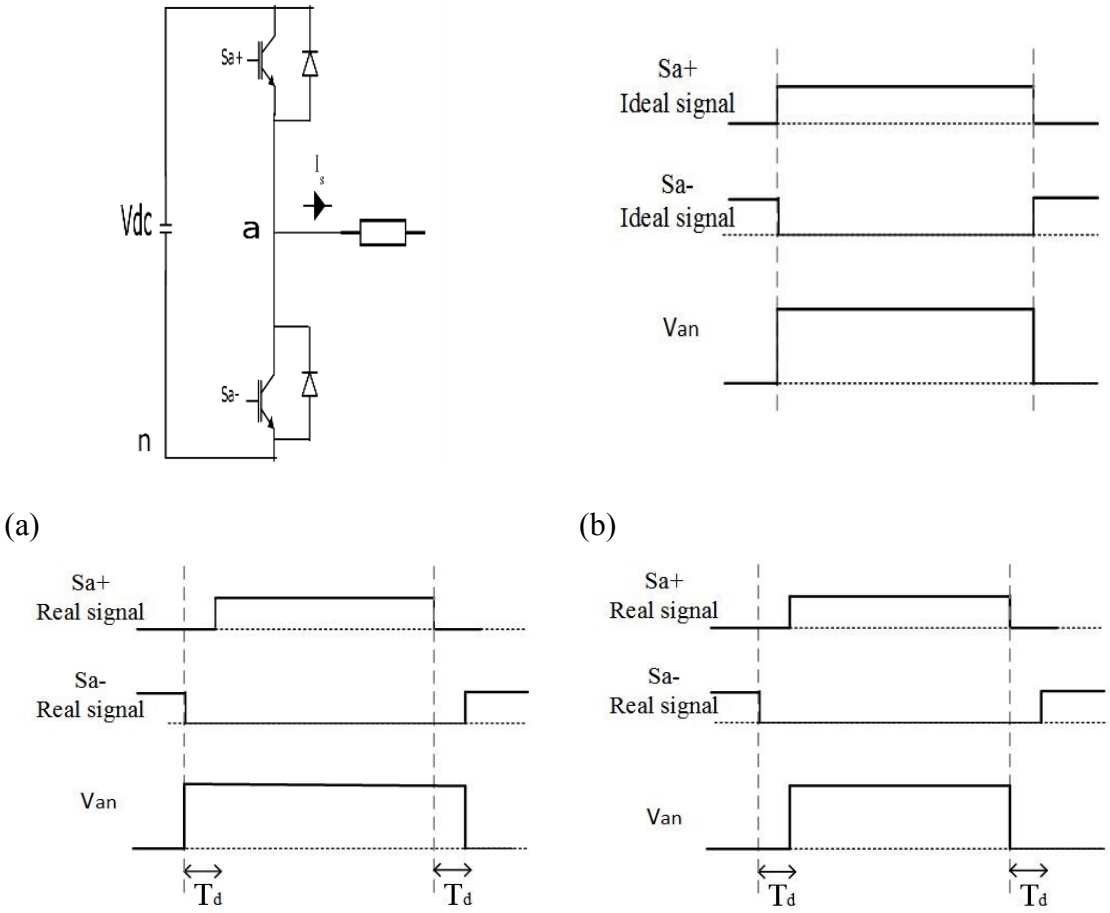


Figure 2.8. Effect of dead-time on the pole voltage depending on the current direction of the load

2.4.3 CMV Associated with the Dead-Time Effect

In all static switching devices there exist turn-on and turn off delay times, with the latter being longer than the former. In order to avoid a shoot through in the DC bus, it is necessary to predetermine a certain blank or dead-time in the control schemes of the power conversion device. During the dead-time, T_d, which is normally realized by delaying the turn-on of a switch, both switches of the leg are off. In this case the current will find its path through the antiparallel diodes. Depending of the current direction, either the upper or the lower diode conducts, therefore the output voltage depends on the current direction in

this dead-time interval. The effect of the current direction on the "pole voltage" is shown in Figure 2.8.

Figure 2.8(b) shows the ideal gating signals for S_{a+} and S_{a-} , which are the gating signals for the upper and lower switches of the given leg, as well as the resulting pole voltage, υ_{an}. In the absence of dead-time, when S_{a+} is enabled, depending on the direction of the pole current, either S_{a+} or its antiparallel diode will conduct producing a pole voltage equal to V_{DC}. Otherwise the pole voltage is zero. On the other hand, when dead-time is used, there will be a time when neither S_{a+} nor S_{a-} are enabled, making one of the antiparallel diodes to conduct the current. When the pole current is positive, or leaving the pole, the lower diode will conduct, leading to a zero pole voltage as shown in Figure 2.8(c). Conversely, when the pole current is negative the upper diode will conduct during the dead-time, leading to a pole voltage of V_{DC} as shown in Figure 2.8(d).

2.5 Eliminating the Common Mode Voltage

Common mode voltage can create several issues for the system such as shaft voltages and ground and bearing currents which leads to premature bearing failures, also it can cause electromagnetic interference (EMI) emissions. In addition, the ground current can lead to false tripping of the ground current relays. It is important to approach a solution to eliminate or reduce the common mode voltage on the terminals in order to prevent the problems in motor and drive applications [50]. Different techniques are used in industry in order to prevent the circulation of undesired current due to the common mode voltage in the machine. In the following part, two most important techniques are introduced.

2.5.1 Common Mode Filters

Common mode filters can be used in order to eliminate the circulating currents in the open end winding machine. The filter consists of common mode choke (inductor), capacitor and resistor. It is designed to eliminate the high-frequency components of the common mode voltage

In [32] common mode passive filter for reducing the shaft voltage, motor bearing current and ground current problem in open end winding machine fed by dual 2-level inverter is proposed. The filter presents a high inductive impedance for the common mode voltage in the phases, therefore provides a high rejection for the common mode noise. The main drawback of adding a filter to the circuit, is its bulky size, which is not applicable in large motor drive systems.

2.5.2 Modulation Strategies

As it was discussed earlier in this chapters, variable speed drive systems suffer from common mode voltages due to the fast switching IGBT-inverters. The amplitude and the number of the common mode voltage is mostly determined by the switching states used in inverter and the dead-time of the switches. Therefore the choice of switching states and the number of the commutations evidently affect the CMV. One option to reduce the common mode voltage is to limit the switching states to those producing lower common mode voltage at the machine terminals. Redundancies of the switching states presented in open end winding configuration can be used to reduce/eliminate the common mode voltage.

Not utilizing specific switching states, might cause some distortion in the quality of the output voltage and current. The problem of current distortion is less severe in inverters with higher number of levels, since the reduction of the switching states does not affect the quality of the waveform [54]-[55].

2.6 Conclusion

The main advantage of the dual 2-level inverter is its DC side/AC-side voltage gain which is a result of the connection of two inverters, one on each end of the open ended load. In this Chapter, the space vector plane of dual 2-level configuration was presented. The SV plane is similar to that of the 3-level NPC inverters, but it presents higher amplitude for voltage vectors which represent higher gains of the open end winding configuration in comparison to the 3-level inverter.

This Chapter also presents the problem of the common mode voltage introducing undesired currents circulations in the open end winding machine, yielding several problems such as more switch losses and bearing damage. The common mode voltage elimination/mitigation can be done by adding a hardware to the system, which is known as common mode filters. Another technique is to adjust the modulation scheme, by selecting proper switching states and their timing in order to obtain zero CMV.

Employing advanced modulation strategy is the most elegant way with lower cost and volume to solve the CMV problem, as compared to the addition of passive filters. Therefore, a modulation-based approach for eliminating/reducing the CMV problem due to dead-time will be discussed in the following Chapter. It will be shown that the reduction of the switching states does not significantly affect the quality of the resulting phase current while successfully eliminates the common mode voltage.

Chapter 3

Common Mode Voltage Elimination in Open End Winding Machines

The space vector plane of the dual 2-level inverter configuration was explained in the previous chapter using all the switching states presented as voltage space vectors. As it was discussed previously, common mode voltages and the circulating currents can cause problems in the machine such as creating higher currents in the phases and also damaging the bearing system of the machine. This chapter presents a modulation scheme to eliminate the common mode voltage on the terminals of the open end winding machine.

It was discussed that the dual 2-level inverter configuration supplying an open end winding machine, provides several redundant voltage space vectors for each space vector location. In this Section the objective is to select the best redundant switching states that can generate the least variation in the common mode voltage to eliminate or minimize the undesired currents in the machine when the load is supplied with a single DC voltage link. In [25] and [51] it was shown that the utilization of the specific voltage vectors and generating the switching pattern accordingly can cancel the common mode voltage at the machine terminals. The existing modulation strategies eliminate the common mode voltage only when the dead-time does not exist in the circuit, and to compensate the dead-time effects another compensation method should be considered. This thesis presents a strategy to improve the work done in [25] and focuses to cancel the dead-time effect on CMV. This method is explained in details in Section 3.2.

3.1 Conventional Modulation Scheme

It has been explained in Section 2.4.1 that each space vector produces a specific common mode voltage and can contribute to the zero-sequence (third harmonic) currents that can circulate in the open end winding machine.

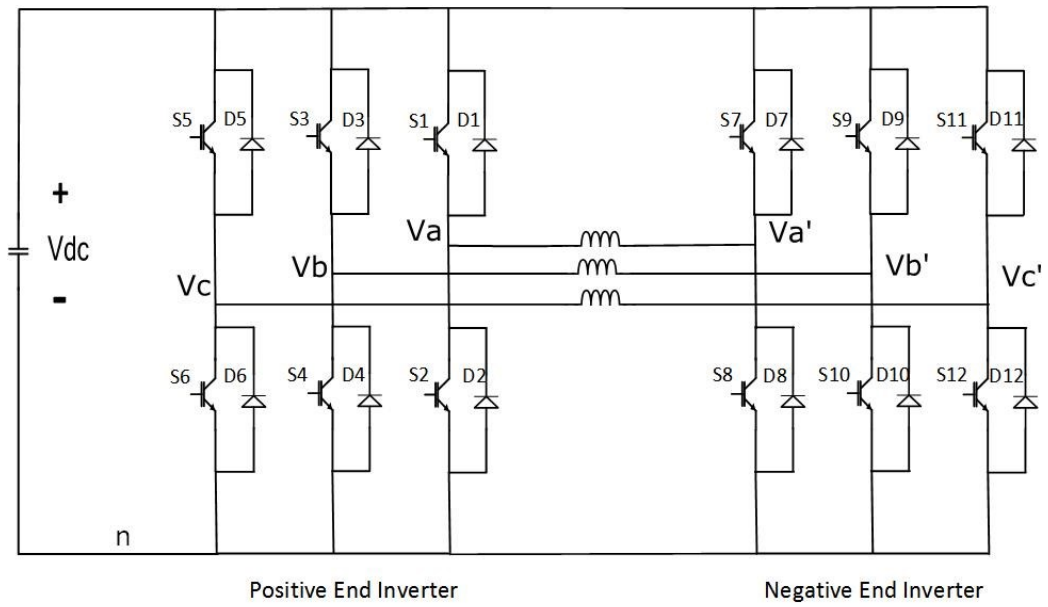


Figure 3.1. Dual 2-level inverter with an open-end winding machine.

Equation (3.1) depicts that the common mode voltage for the open end winding machine can be obtained as

$$v_{CM} = v_{CM-P} - v_{CM-N} \tag{3.1}$$

This equation suggests that the necessary condition to achieve zero common mode voltage is that the common mode voltage produced in both inverters (v_{CM-P} and v_{CM-N}) are equal at any instant. Therefore, the instantaneous overall common mode voltage would be zero. The basic principle in designing a switching strategy capable of reducing the common mode currents is to avoid the variation in common mode voltage. This objective can be achieved by placing a constraint in choosing the voltage vectors to synthesize the reference vector. This only requires the knowledge of the effect of different switching states on the common mode voltage. Thus, it is possible to find a vector combination that presents the

same common mode voltage in both inverters. The Table below shows the voltage space vectors and the common mode voltages they produce in each ends of the load. As it can be noted, the odd SVs, i.e. 1, 3 and 5 have the same CMV as $\frac{V_{DC}}{3}$, and the even SVs, i.e. 2, 4, and 6 cause the same common mode voltage with magnitude of $\frac{2V_{DC}}{3}$.

Table 3-1. CMV generated by switching states

SV	V_{CM}
V_1 (100), V_3 (010) and V_5 (001)	$\frac{V_{DC}}{3}$
V_2 (110), V_4 (011) and V_6 (101)	$\frac{2V_{DC}}{3}$
V_0 (000)	*0*
V_7 (111)	V_{DC}

Therefore the choice of the SV combination of XY', which both X and Y are odd or even numbers will results in the overall zero common mode voltage. In [51] it was proposed that one can achieve zero CMV for the machine by using only odd or even non-zero SVs in both inverters. Therefore this will not contribute to the zero sequence currents between two inverters.

All the space vectors that provide the zero common mode voltage are presented in Table 3.2.

Table 3-2. SVs generating instantaneous zero CMV in open end configuration

Vectors XY' with X and Y are odd vectors	Vectors XY' with X and Y are even vectors
13'-15'-35'-31'-51'-53'-11'-33'-55'	64'-24'-26'-46'-42'-62'-22'-44'-66'

The new space vector diagram having only the voltage vectors presented in Table 3.2 are shown in Figure 3.2.

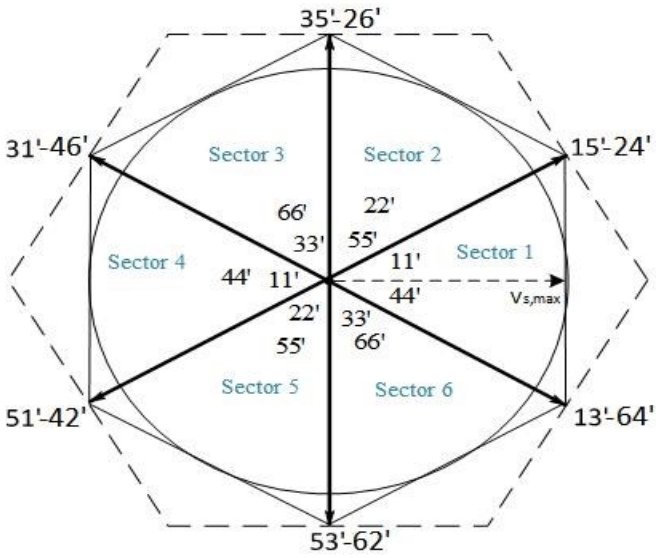


Figure 3.2. Space vector diagram of a dual 2-level scheme with the odd and even SV combinations

The main drawback of using this SV diagram, is the reduction of the linear region for modulating the reference voltage. In the Figure 3.2, the hexagon shaped by the large vectors is drawn in dashed line. There one can see that since the *large* SVs, i.e. 14', cannot be used, the maximum value of the load voltage is limited by the medium voltage vectors, i.e. 15'. Employing the medium vectors, the maximum reference vector is *cos*(30°) times the magnitude of a medium SV. Therefore, the maximum magnitude of the reference load SV ($V_{s,max}$) is $1.5V_{DC}$, 13.4% less than what could be obtained without the constraint for not producing zero-sequence current and generating CMV. It should be noted that the maximum (phase voltage) gain of a 3-level NPC converter is $\frac{V_{DC}}{\sqrt{3}}$, while in this scheme, it is $V_{DC,}$ which it is more than that in 3-level inverters even after limiting the vector combinations to medium vectors.

Consider the case when only odd or even vectors are employed, transitions from one SV to the next will require 2 legs to be switched. Therefore, there is 2 commutations as opposed to 1, which leads to higher switching losses as well as higher harmonic distortion in the output voltages/currents. This is the price to pay for the non-generation of CMV.

In [25] it was suggested to use only the odd vectors in both inverters since having lower common mode voltage (CMV= $\frac{V_{DC}}{3}$) in each side than the case of the even vectors (CMV= $\frac{2V_{DC}}{3}$) which is preferred.

3.1.1 Modulation Index

The modulation index (m) is defined as the ratio of the voltage reference vector to the maximum magnitude of the voltage reference space vector in the linear region.

The maximum amplitude of the reference vector that can be synthesized in this scheme is $\frac{3V_{DC}}{2}$ which corresponds to the radius of the inscribed circle shown in Figure 3.2. It should be noted that in this part, the modulation index is defined for the new SV scheme, and m=1 represents the maximum linear region that it can operate in.

$$|V_{s,max}| = \frac{3\,V_{DC}}{2} \tag{3.2}$$

Therefore the maximum peak amplitude attainable using this scheme is

$$\left|\hat{V}_{phase,max}\right| = \frac{3\,V_{DC}}{2} * \frac{2}{3} = V_{DC} \tag{3.3}$$

The modulation index is described as

$$m_a = \frac{\hat{V}_{phase}}{V_{DC}} \tag{3.4}$$

3.1.2 Placing the SVs in the Sequence

The space vector sequence in a space vector modulation switching pattern, determines the quality of the waveform since it affects the number of transitions of all the switches during the space vector sampling cycle. There are different ways for applying SVM in a dual 2-level inverter scheme [25], [30], [35], [51]. By comparing the SV diagrams of Figure 3.2 and that of the 2-level inverter shown in Figure 2.2, one can see that there are still 6 Sectors for the dual 2-level scheme, but these are phase-shifted with respect to those of the single 2-level inverter schemes. The synthesis of the reference SV for the dual 2-level scheme can

be done by using the nearest active and zero SVs. The choice of SVs 11', 33' and 55'as the zero vectors results in a free-wheeling of the load current, therefore it corresponds to a "zero" SV which should be chosen depending on the sector.

In all the sectors, an appropriate zero vector is chosen to have minimum switching transitions in the space vector modulation sampling cycle. For instance, in Sector 1 of Figure 3.2, two active vectors, 13' and 15', are the nearest active vectors. The options for the zero vector are 11', 33', and 55'. In this sector, the vector 11' is chosen therefore in this sector the active vectors and the zero vector are 13', 15' and 11' respectively. Therefore the positive end inverter is clamped to SV 1(100) while the negative end inverter is switched between SVs 1', 3' and 5'.

Now that the active and zero vectors of each sector have been determined, the proper arrangements of the SVs are required during the sampling cycle to obtain high quality voltage waveforms.

In a single 2-level inverter one can employ the nearest SVs rotating clockwise then counter-clockwise, or vice versa. As an example for Sector 1, one can use sequence 0-1-2-7-2-1-0, where SVs 0 and 7 are "zero" SVs used in the beginning, middle and end of the sequence. One benefit of this strategy is that there will be commutations in only one inverter leg at any transition of SVs.

Extending this approach for the dual 2-level scheme, considering only the odd SVs to avoid CMV at the load, one can use the following sequence of SVs for Sector 1: 11'-13'-15'-11'-15'-13'-11'. In such a case, one keeps the positive end inverter clamped to 1(100), while the negative end inverter switches between SVs 1', 3' and 5'. In this case, there will be simultaneous commutations in 2 legs of the negative end inverter. However, the average switching frequency of the inverters of the dual 2-level configuration will be the same as of a single 2-level inverter since in the following Sector, the negative end inverter will be clamped to SV 5' and the positive end inverter will do the "switching".

In Figure 3.3, the sequence of the vectors suggested in [25] is shown when the tip of the reference vector lie in Sector 1. T_1 and T_2 denote the time for the active vectors of the sector

in which the tip of the reference voltage vector is located, and T_0 is the time for the zero vector of the corresponding sector.

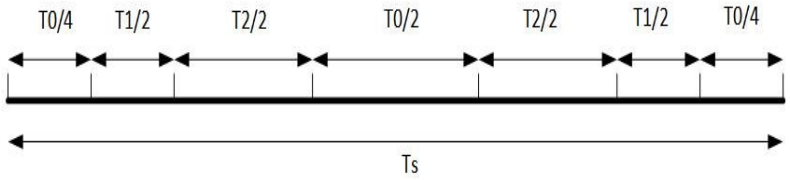


Figure 3.3. Switching sequence when the reference vector is in sector 1

The sequence of the SVs for all the sectors in this modulation scheme is summarized in Table 3.3.

Table 3-3. Sequence of Vectors in the conventional scheme

Sector	Sequence of SVs
Sector 1	**11'-13'-15'-11'-15'-13'-11'**
Sector 2	**55'-35'-15'-55'-15'-35'-55'**
Sector 3	**33'-35'-31'-33'-31'-35'-33'**
Sector 4	**11'-51'-31'-11'-31'-51'-11'**
Sector 5	**55'-51'-53'-55'-53'-51'-55'**
Sector 6	**33'-13'-53'-33'-53'-13'-33'**

As it was discussed in Section 2.4, three factors can affect the common mode voltage, which are (1) switching states, (2) switch voltage drops and (3) dead-time. The strategy presented in this Section can eliminate the common mode voltage on the terminals of the open end winding machine based on the following assumptions:

- The corresponding power switches and diodes are ideal, which means there is no voltage drop on them when they are conducting
- There is no dead-time in the circuit

In this Thesis, the effect of switch voltage drops are neglected since this voltage is negligible in compare to the DC bus voltage. The effect of the dead-time on the common

mode voltage is the main focus of this thesis. The disturbance of the dead-time on the common mode voltage depends on the SV placement and it is discussed in the following sections.

3.2 Effect of Dead-Time on the CMV of an Open End Winding Machine

The strategy for eliminating the CMV described in Section 3.1 is based on the assumption that one can control the pole voltages in the inverters at all times. This solution functions properly only in the ideal case, where power switches commutate instantaneously. Further consideration is needed because of the existence of dead-time in real circuits. As shown in Section 2.4.3, the pole voltage during the dead-time depends on the direction of the pole current. Therefore, there is no control on the voltage for this time interval and it is possible that the inverters operate with a "non-odd" SV during the dead-times interval, which can lead to spikes of different magnitudes in the CMV.

Table 3.4 shows, at the right side, the pole voltages during the dead-time for commutations in those legs for the six possible combinations of current polarities in a 3-wire system. This might look redundant but will help in obtaining the resulting SVs during the dead-time of a transition between the selected (odd) SVs.

Recall that when using only the odd SVs, there will be simultaneous commutations in 2 legs of the inverter while the third remains unchanged. As an example, when there is a change in SVs from 1(100) to 3(010), or vice-versa, in the dead-time interval, the pole voltages in phases a and b will depend on the current polarities in those phases as shown in Table 3.4 while the one at phase c remains zero, (v_{an} v_{bn} 0). Therefore, one can identify the SV of the inverter, during a dead-time, for all possible combinations of current polarities which are shown in the fourth column of Table 3.5. There one can see that there will be some undesired (even or zero) SVs for all SV transitions but that will occur only for certain combinations of current polarities. The SVs of the inverter during a dead-time for a transition 1(100) to 5 (001), or vice-versa, and 3(010) to 5(001), or vice-versa, for various combinations of current polarities are shown in columns 4-6 of Table 3.5.

Table 3-4. Current polarities and pole voltages during dead-time

i_a	i_b	i_c		v_{an}	v_{bn}	v_{cn}
<0	**<0**	**>0**		V_{DC}	V_{DC}	**0**
<0	**>0**	**<0**		V_{DC}	**0**	V_{DC}
<0	**>0**	**>0**	→	V_{DC}	**0**	**0**
>0	**<0**	**<0**		**0**	V_{DC}	V_{DC}
>0	**<0**	**>0**		**0**	V_{DC}	**0**
>0	**>0**	**<0**		**0**	**0**	V_{DC}

Table 3-5. Current polarities and inverter SVs during dead-time of transitions of odd SVs

i_a	i_b	i_c		1(100)↔3(010)	1(100)↔5(001)	3(010)↔ 5(001)
<0	**<0**	**>0**		**2(110)**	**1(100)**	**3(010)**
<0	**>0**	**<0**		**1(100)**	**6(101)**	**5(001)**
<0	**>0**	**>0**	→	**1(100)**	**1(100)**	**0(000)**
>0	**<0**	**<0**		**3(010)**	**5(001)**	**4(011)**
>0	**<0**	**>0**		**3(010)**	**0(000)**	**3(010)**
>0	**>0**	**<0**		**0(000)**	**5(001)**	**5(001)**

It is important to note that the direction of the current is considered as positive when it circulate from positive end inverter to the negative end inverter. Therefore when the current is defined as positive, it leaves positive end inverter, but enters the corresponding leg in the negative end inverter. Table 3.6 shows the leg voltage for both inverters during the dead-time.

Table 3-6. Current direction and the corresponding voltage during dead-time interval for both inverters

Phase Current direction	Voltage of leg in the Negative End Inverter during the dead-time	Voltage of leg in the Positive End Inverter during the dead-time
+	**0**	V_{DC}
-	V_{DC}	**0**

The impact of the dead-times on the CMV at the load terminals when the dual 2-level inverter scheme is controlled with the conventional SVM scheme, which was summarized in Table 3.3, can be illustrated as shown in Figure 3.4. It is assumed that the reference voltage vector is in Sector 2 and that the polarities of the load currents are i_a>0, i_b<0 and i_c<0.

In this figure, pole voltages of the positive end inverter are shown along with the common mode voltage in positive end inverter and the overall common mode voltage for the duration of one sampling cycle, T_s. On the top, all the SVs in the sampling cycle are presented in sequence, which are 55'-35'-15'-55'-15'-35'-55'. Using these odd vectors, one can expect to have constant common mode voltage in both inverters. It should be noted that the negative end inverter is clamped at SV 5'(001), resulting in a constant $V_{CM\text{-}N}=\frac{V_{DC}}{3}$, which is not shown in the figure. Having a dead-time in the power circuit, one can notice the spikes in the common mode voltage of the positive end inverter.

There are positive spikes in CMV during transitions (dead-times) between SV 3(010) and 5(001) resulting the positive end inverter to operate briefly with SV 4(011) leading to $V_{CM\text{-}P}=\frac{2V_{DC}}{3}$.

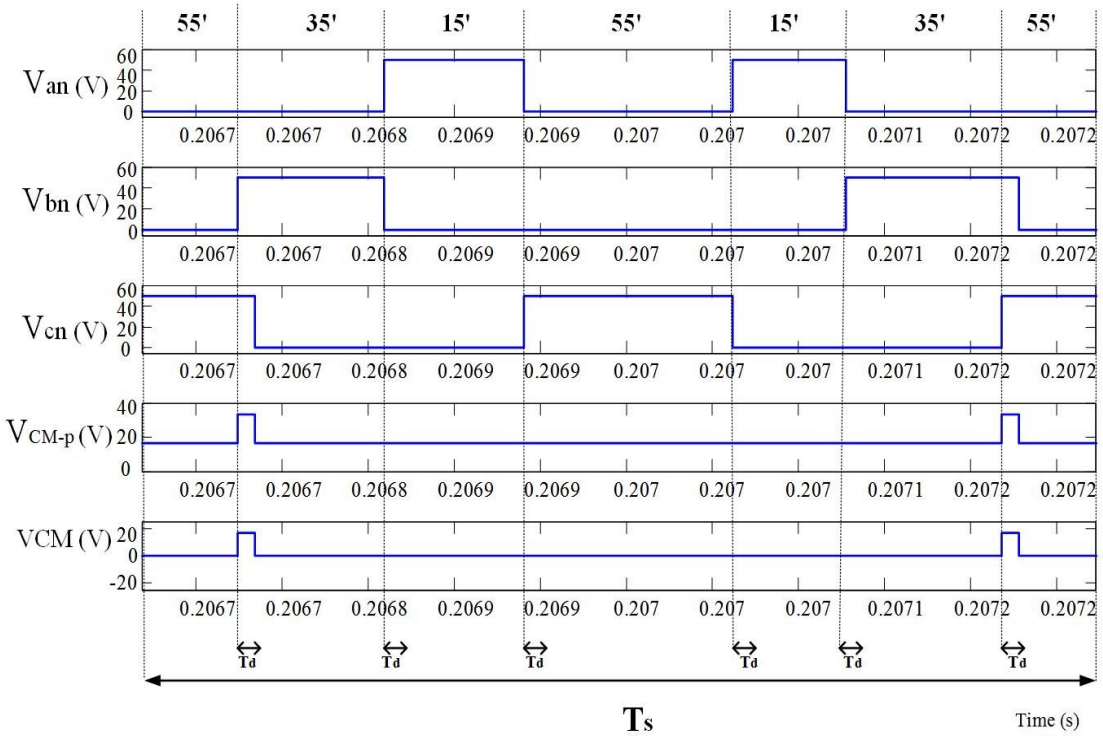


Figure 3.4. Sample case showing the impact of the dead-time on the CMV of an OEWM using the conventional SVM. Td=10 μs

The effect of the dead-time on the CMV can be removed by using a method suggested in [47]. This method [PBDTC] is developed by analyzing the effect of dead-time on a pulse by pulse basis and altering each pulse accordingly.

The pulse time is altered in such a way to cancel the effect of the dead-time in the final pulse. Proper pulse time can be added to or subtracted from the beginning or ending of the pulse duration. The adjusted pulse is processed through the dead-time generator and then applied to the motor terminals.

In Figure 3.5 the pulses are depicted for (1) the ideal case, (2) the ideal pulse after processing through the dead-time generator, (3) the compensated pulse (4) the compensated pulse after processing through the dead-time generator, for two current directions. To compensate the difference, the pulse can be started (or ended depending on the current direction) before the ideal case so that after processing by the dead-time, the

resultant pulse applied to the motor terminals seems like the ideal pulse. This method will compensate dead-time effect on the common mode voltage and also on the phase voltages.

In this method, the correction of the pulse times requires the knowledge of the duration of the dead-time of the device and the current polarity.

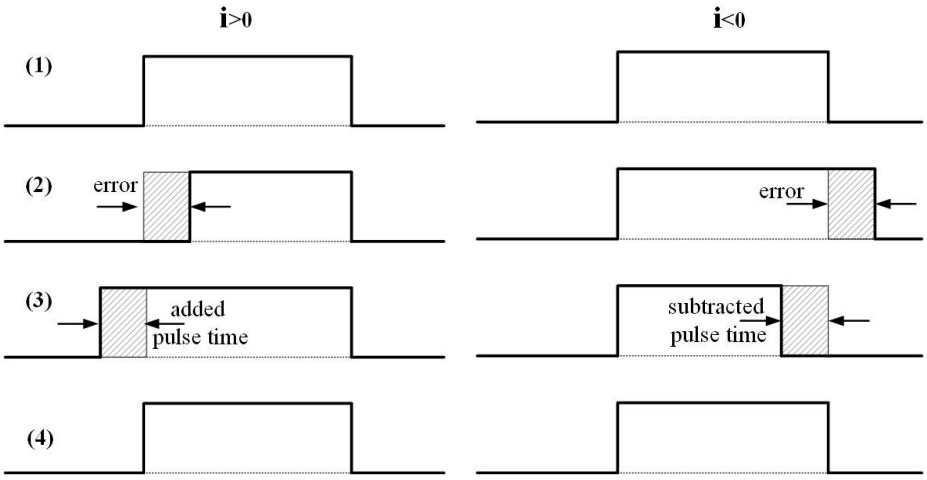


Figure 3.5. Pulse pattern for ideal and using PBDTC method

3.3 Proposed Modulation Scheme to Eliminate the Effect of Dead-Time on the Common Mode Voltage

As shown in the previous Section, the use of the conventional SVM sequence will lead to the occurrence of CMV during the SV transitions for all combinations of current polarities. To prevent this issue, modified SVM that considers the polarity of the load currents is required.

From Table 3.5, column 4, it is observed that transitions between SVs 1(100) and 3(010) will result in non-odd SVs during the dead-times when currents in phases *a* and *b* have the same polarity, in rows 1 and 6. Otherwise, the SV during the dead-time will be either V_1 or V_3. It should be noted that for a transition between SVs 1(100) and 3(010), legs *a* and *b* of the inverter commutate. Therefore one should not use a transition S**V 1(100)↔3(010)** when currents in phases *a* and *b* have the same polarities. The same rule applies to the other SVs:

Transitions between SVs which require commutations in inverter legs with the same current polarity should be avoided.

Table 3-7. Proposed sequence of SVs to avoid CMV during dead-time

	Phase with the different current polarity	**Sequence to eliminate CMV due to the dead-time**
Sector 1	i_c	**11'-15'-13'-15'-11'**
	i_b	**11'-13'-15'-13'-11'**
	i_a	**11'-13'-11'-15'-11'-13'-11'**
Sector 2	i_c	**55'-15'-55'-35'-55'-15'-55'**
	i_b	**55'-35'-15'-35'-55'**
	i_a	**55'-15'-35'-15'-55'**
Sector 3	i_c	**33'-35'-31'-35'-33'**
	i_b	**33'-35'-33'-31'-33'-35'-33'**
	i_a	**33'-31'-35'-31'-33'**
Sector 4	i_c	**11'-51'-31'-51'-11'**
	i_b	**11'-31'-51'-31'-11'**
	i_a	**11'-31'-11'-51'-11'-31'-11'**
Sector 5	i_c	**55'-51'-55'-53'-55'-51'-55'**
	i_b	**55'-53'-51'-53'-55'**
	i_a	**55'-51'-53'-51'-55'**
Sector 6	i_c	**33'-53'-13'-53'-33'**
	i_b	**33'-53'-33'-13'-33'-53'-33'**
	i_a	**33'-13'-53'-13'-33'**

Table 3.7 shows the proposed sequences of SVs to be used in each of the 6 Sectors for different current polarities. There one sees that whenever the current with the different polarity is in a given phase, say *c*, the commutating inverter, say the negative end for Sector

1, has to use the SV particular to phase *c*, 5'(001), between the 2 other SVs, 1'(100) and 3'(010). One can see from Table 3.7 that all sequences of SVs are symmetrical. However, when the current with the different polarity coincides with the phase of the SV to be used as the zero SV, say current *a* in Sector 1, the sequence of SVs is longer than otherwise.

The pulse based dead-time compensation (PBDTC) method is more computationally intensive as the dead-time compensation should be implemented within the dwell time of each space vector location i.e. within T_1, T_2 and T_0. In other words, it means that the computation should be done within this duration which is a fraction of the sampling time Ts. In the proposed method, the decision is taken only once in a sampling time T_s and only the sequence of the space vector location is changed at the beginning of the sampling period. This totally avoids the requirement addition of the compensating pulse duration for each dwell time duration T_1, T_2 and T_0. This is advantageous in terms of computational speed of the controller and the computational requirements for the modulation scheme.

3.4 Conclusion

This Chapter proposes a SVM-based modulation logic to eliminate the effect of dead-time on the common mode voltage in open end winding configuration fed from dual 2-level inverters. Firstly, the previous modulation scheme suggested in [25]-[51] was investigated. The dead-time effect is analyzed in details and the relation of the undesired spikes in common mode voltage and the current direction was studied. The proposed strategy is developed based on the relation of the current and the arrangements of the voltage vectors during the SV sampling cycle. Based on the proposed SV rearrangement, it is possible that the effect of dead-time on the common mode voltage be eliminated. The effectiveness of the proposed strategy will be evaluated in the next Chapter.

Chapter 4

Performance Verification by Simulation

4.1 Introduction

In this project, to operate the open end winding machine, dual 2-level inverters connected to both ends of the windings of the machine, as is shown in Figure 4.1. The problem with the common mode voltage in this scheme has been discussed in Chapter 3. In the present Chapter, the performance of the system is assessed for both the conventional and the proposed SV scheme using *MATLAB/Simulink*.

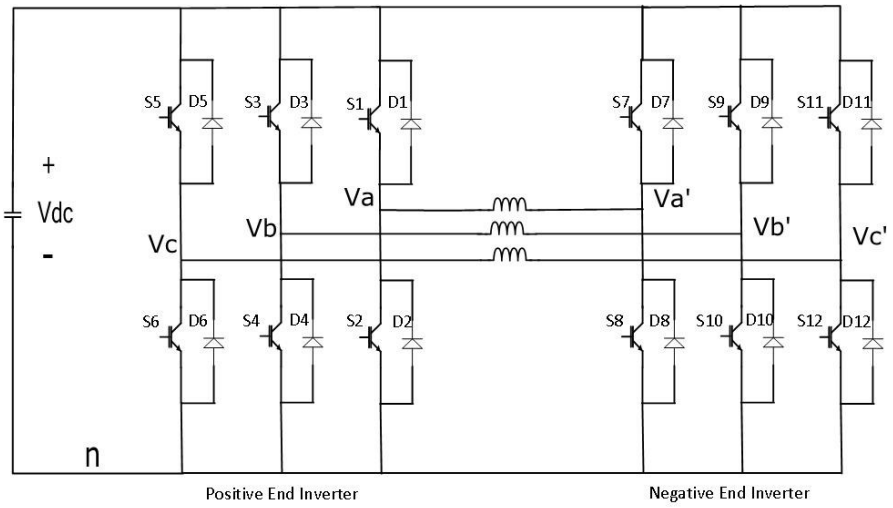


Figure 4.1. Circuit topology of the three phase open end winding machine

The results of the two schemes have been compared to investigate the effectiveness of these schemes on the waveform quality and the power losses of the inverter. The total harmonic

distortion (THD) of the output current for the open end winding with different space vector modulation schemes has been evaluated.

4.2 Principle of Space Vector Modulation in OEWM

As it was mentioned in the previous Chapter, using space vector modulation enables us to present all the switching states as Space Vectors (SV). There are two types of vectors in the space vector diagram, namely active vectors and zero vectors.

Figure 4.2 shows the space vector diagram in order to eliminate the common mode voltage in open end winding machine fed by dual 2-level inverters, using the specific vectors. All the vectors in this scheme results in equal v_{CM-P} and v_{CM-N} as it was shown in section 3.1, therefore the overall common mode voltage in the machine will be zero. One can see that there are six active vectors, namely 15', 35', 31', 51', 53', and 13', which form a hexagon with six sectors. The zero vectors are selected to be 11', 33', and 55' which lie on the center of the hexagon.

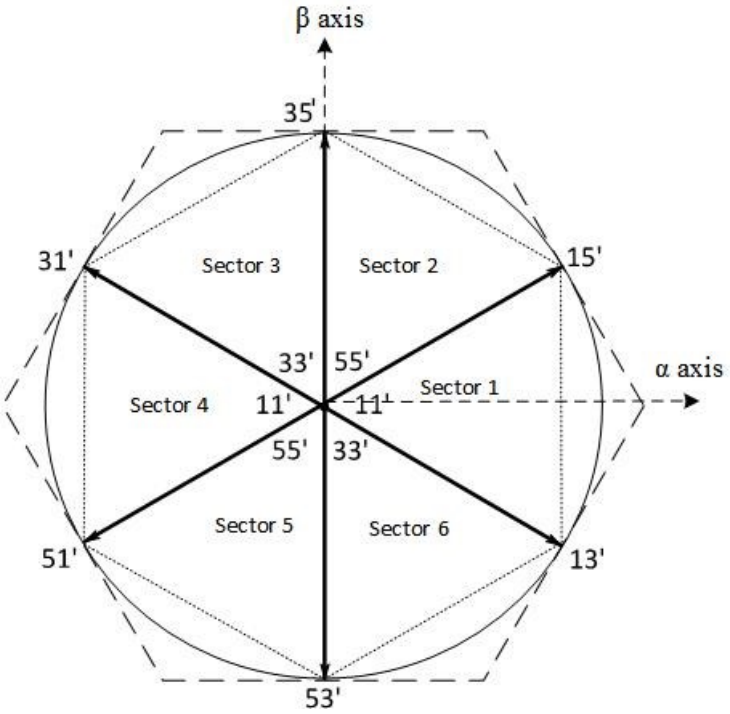


Figure 4.2. Space vector diagram using odd medium vectors

4.2.1 Dwell Time Calculation For Space Vectors

One can deduce the reference space vector in αβ components from the phase voltages in abc frame using the transformation given as (4.1). In this equation, V_α and V_β represent the real and imaginary parts respectively.

$$\overrightarrow{V_s}=\begin{bmatrix}V_\alpha\\V_\beta\end{bmatrix}=\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\begin{bmatrix}\upsilon^*_{aa\prime}\\\upsilon^*_{bb\prime}\\\upsilon^*_{cc\prime}\end{bmatrix} \tag{4.1}$$

where $\upsilon^*_{aa\prime}$, $\upsilon^*_{bb\prime}$, and $\upsilon^*_{cc\prime}$ are instantaneous reference phase voltages. The reference space vector can be expressed in terms of two variables namely V_α and V_β using the following equation

$$\overrightarrow{V_s} = V_\alpha + j\,V_\beta \tag{4.2}$$

The combination of the SVs that can be implemented with the various switch states of the inverter enables the synthesis of the reference vector $\overrightarrow{V_s}$, within every SV sampling duration. In steady state, the reference vector is a rotating vector in the αβ plane with a constant magnitude and rotating with an angular speed related to the fundamental frequency of the reference voltages. The first step to synthesize the reference voltage vector is to find the sector in which the reference vector is located. Sector determination requires the knowledge of the angle of the reference vector. The reference vector calculated in equation (4.2) is represented in rectangular coordinates. Therefore, a *MATLAB* block is used to convert the rectangular to polar coordinates to find the angle of the reference vector with respect to α axis, which is shown in Figure 4.3. This angle (ωt°) is given in the range of (-180, +180] degrees using the complex to polar block in MATLAB/SIMULINK. The relation of the angle (ωt°) and the sector for the space vector scheme of Figure (4.1) is shown in Table 4.1.

Table 4-1. Sector determination of SVM scheme for CMV eliminated SV scheme

Sector	Angle of the reference vector(ωt°)
#1	(-30,30]
# 2	(30,90]
# 3	(90,150]
# 4	(150,180]U(-180,-150]
# 5	(-150,-90]
#6	(-90,-30]

Figure 4.3 shows the Simulink blocks to implement the aforementioned logic for calculating the sectors. The reference phase voltages, $\boldsymbol{\upsilon}_{aa'}$, $\boldsymbol{\upsilon}_{bb'}$ and $\boldsymbol{\upsilon}_{cc'}$, are the inputs to this block, Vα and Vβ are calculated using equation (4.1), then Simulink block "complex to Magnitude-Angle'' converts the variable from the rectangular to polar coordinates. The output angle of that block is in radians, therefore the gain of $\frac{180}{\pi}$ is used to convert the values to degrees. Then, using Table 4.1, the six sectors are identified, and the output 'sector' is a number between 1 and 6.

Based on the volt-second principle, the reference voltage vector can be formed by switching active and zero vectors of each sector. From the angle of the reference vector with respect to the beginning of each sector, dwell times for the two nearest active vectors can be calculated using the volt-second balance principle. Figure 4.4 shows only the sector in which the reference vector is located, the x-y coordinate is defined to ease the calculations. x axis is along the first vector of the sector, and y is the orthogonal to that. In the figure, $\overrightarrow{V_s}$ is the reference vector which is to be synthesized by the two nearest active vectors, $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$, and the zero vector of the sector.

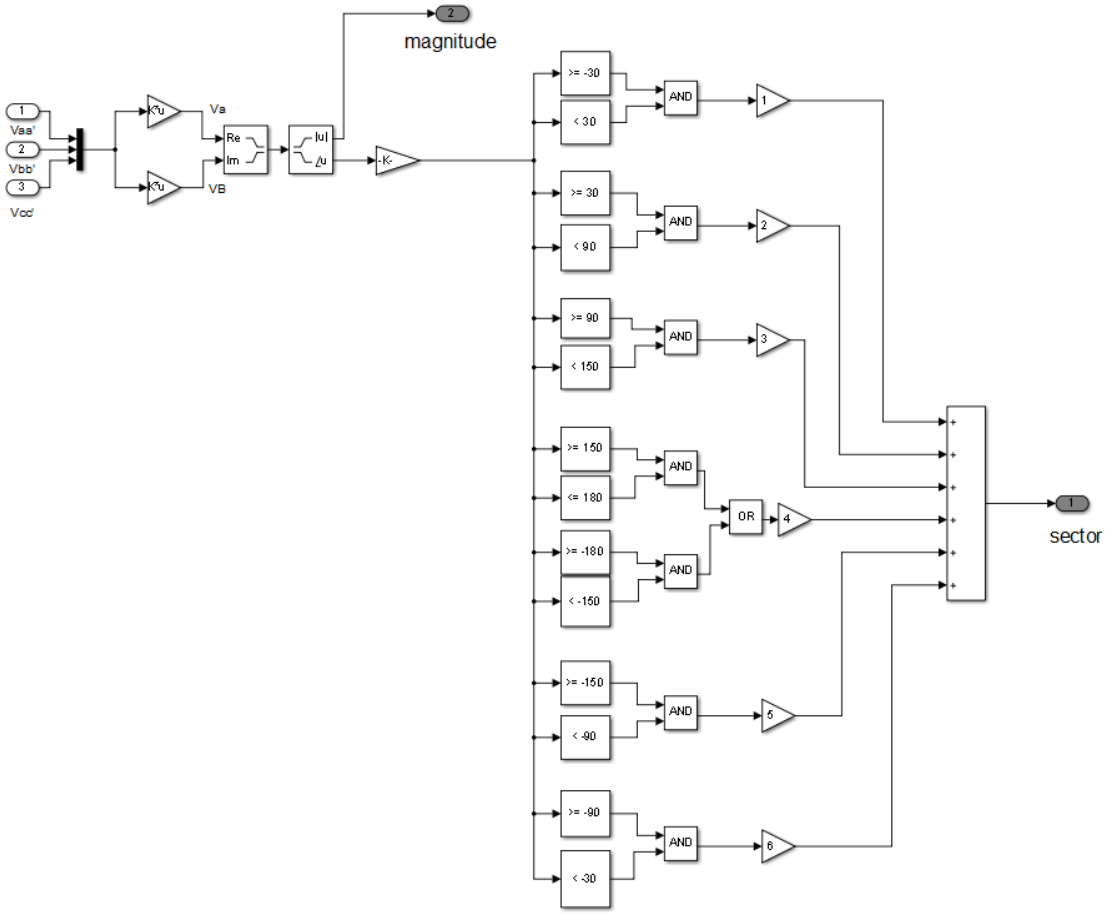


Figure 4.3. Implementation of the sector determination for CMV eliminated SV diagram in Simulink

Based on volt-second balance principle, the product of reference voltage $\overrightarrow{V_s}$ and space vector sampling duration T_s equals the sum of the voltage space vectors multiplied by the time interval (dwell time) of respective space vectors [53]. Equation (4.3) shows the volt-second balance for the vector $\overrightarrow{V_s}$ shown in Figure 4.4. $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ are 60 degrees apart. The angle θ denotes the angle of the reference voltage vector with respect to the beginning of the sector. The objective is to find the dwell times for the two active vectors along with time for zero vector, in order to synthesize the reference vector for the SV sampling duration T_s.

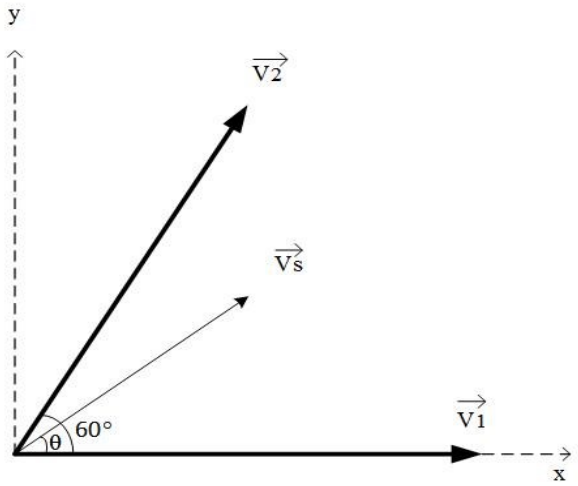


Figure 4.4. Projecting reference vector on two nearby vectors

It is important to note that the reference vector is considered to be constant within the sampling cycle.

$$\overrightarrow{V_1}T_1 + \overrightarrow{V_2}T_2 + \overrightarrow{V_0}T_0 = \overrightarrow{V_s}T_s \tag{4.3}$$

where T_1 and T_2 are the dwell time of vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ respectively, and T_0 is the time for the zero vector.

For the purpose of simplicity, all the vectors in equation (4.3) are presented in real and imaginary parts in equation (4.4)

$$|V_1|T_1[\cos 0° + j \sin 0°] + |V_2|T_2[\cos 60° + j \sin 60°] = |V_s|T_s[\cos\theta + j \sin\theta] \tag{4.4}$$

Equating real and imaginary parts gives two separate equations as shown below.

$$\begin{aligned} T_1|V_1|\cos 0° + T_2|V_2|\cos 60° &= T_s|V_s|\cos\theta \\ T_2|V_2|\sin 60° &= T_s|V_s|\sin\theta \end{aligned} \tag{4.5}$$

$$\begin{aligned} |V_1|T_1 + |V_2|\frac{T_2}{2} &= T_s|V_s|\cos\theta \\ \frac{\sqrt{3}}{2}|V_2|T_2 &= T_s|V_s|\sin\theta \end{aligned} \tag{4.6}$$

Dwell times for the two active vectors of $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ and the time for the zero vector can be derived by solving equation (4.6). Assuming $|V_1| = |V_2|$, we have

$$\begin{aligned} T_1 &= \frac{T_s|V_s|}{\sqrt{3}\,|V_1|}[\sqrt{3}\cos\theta - \sin\theta] \\ T_2 &= \frac{2}{\sqrt{3}}\,\frac{T_s|V_s|}{|V_1|}\,\sin\theta \end{aligned} \tag{4.7}$$

Equation (4.7) shows that the dwell times for both vectors can be obtained as the function of the amplitude of the reference vector, amplitude of the active vectors of $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$, and the angle of the reference vector with respect to $\overrightarrow{V_1}$.

To relate these equations to the space vector scheme of the OEWM, shown in Figure 4.2, the values for the active vectors should be used in the equation. As it was discussed in the previous chapter, the magnitude of all the active vectors of Figure 4.2 are as follows.

$$|V_1| = |V_2| = \sqrt{3}\,V_{dc} \tag{4.8}$$

where V_{dc} is the voltage of the dc bus of the open end winding machine fed by dual 2-level inverter, shown in Figure 4.1, and reference vector is $\overrightarrow{V_s}$ as described in (4.2).

By substituting $\sqrt{3}\,V_{dc}$ for $|V_1|$ and $|V_2|$ into equation (4.7), we obtain the dwell times of the active and zero vectors for the space vector as

$$\begin{aligned} T_1 &= \frac{T_s V_s}{3\,V_{dc}}[\sqrt{3}\cos\theta - \sin\theta\ ] \\ T_2 &= \frac{2}{3}\,\frac{T_s V_s}{V_{dc}}\,\sin\theta \qquad\qquad \text{for } 0 \le \theta < 60° \\ T_0 &= T_s - (T_1 + T_2) \end{aligned} \tag{4.9}$$

Similarly, one can obtain the dwell times for the active vectors when the reference vector is located in any of the other sectors. It requires the knowledge of the angle of the reference vector with respect to the beginning of that given sector.

The angle θ can be obtained for all the sectors depending on the sector in which the reference vector is located using Table 4.2.

Table 4-2. Finding the angle θ for all sectors

Sector	θ (degree)
#1	ωt +30
#2	ωt -30
#3	ωt -90
#4	ωt -150 or ωt +210
#5	ωt +150
#6	ωt +90

After the dwell time calculation for the active and zero vectors, a proper switching pattern should be chosen to obtain the gating pulses for all 12 switches to achieve the desired phase voltages.

The conventional and the proposed switching patterns are discussed in depth in Chapter 3. In the following sections, the performance of the two control strategies are analyzed through simulations.

4.3 The Conventional SV Placement

The procedure to obtain the dwell times of the active vectors along with the time for the zero vector was demonstrated in order to synthesize the phase voltages within the SV sampling cycle using the space vector modulation of Figure 4.2. The distribution of these vectors in the sequence within a sampling cycle should be decided in order to obtain good quality voltage waveforms. The switching algorithm presented in [25] suggests the placements of the SVs during the sampling cycle in such a way that the sequence is symmetrical and the two active vectors are used twice in the SV cycle and the zero vector is used in the start, middle and end of the sampling cycle.

Figure 4.5 demonstrates the SV placements within one sampling cycle, assuming the reference vector is located in sector one.

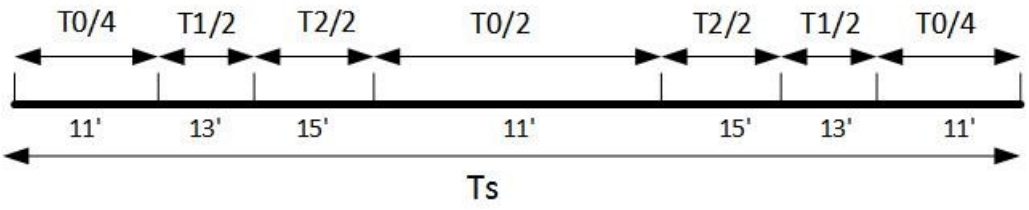


Figure 4.5. SVs placement during one sampling cycle in conventional scheme

Sequences for space vectors alignment are presented in Table 4.3 for all the six sectors.

Table 4-3. Sequence of SVs in the conventional scheme

Sector	Sequence of SVs
#1	**11'-13'-15'-11'-15'-13'-11'**
#2	**55'-35'-15'-55'-15'-35'-55'**
#3	**33'-35'-31'-33'-31'-35'-33'**
#4	**11'-51'-31'-11'-31'-51'-11'**
#5	**55'-51'-53'-55'-53'-51'-55'**
#6	**33'-13'-53'-33'-53'-13'-33'**

The gating signals for all the switches can be obtained by the following procedure. This process is repeated for each sampling duration.

1) Sample the instantanous values of the reference voltages for the three phases.
2) Compute the reference space vector $\overrightarrow{V_s}$, using equation (4.1) and (4.2).
3) Determine the angle of the reference vetor, $\overrightarrow{V_s}$, with respect to the α axis and employ Table 4.1 to find the sector in which the reference vector is located.
4) Calculate the dwell time for the zero and active vectors using equation (4.9).
5) Select the proper SV placement according to Table 4.3.

The implementation procedure of the conventional scheme in order to obtain the gating signals is summerized in Figure 4.6.

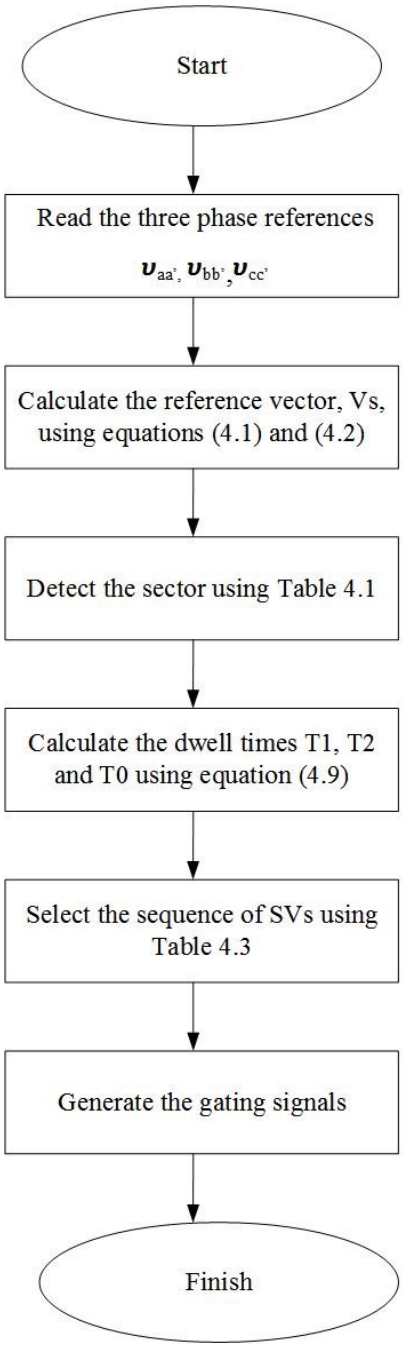


Figure 4.6. Schematic diagram of the conventional space vector modulation in OEWM during one sampling cycle

4.3.1 Average Switching Frequency

The average switching frequency of a switch can be found by knowing the number of full commutations of the switch during each sampling cycle. As it was stated in the previous Chapter, in the space vector scheme employing only odd vectors, in each sector only one of

the inverters is switching and the other is clamped to one switching state. Therefore, each inverter is clamped for 3 sectors, and have switching for the remaining 3 sectors. Therefore, to find the average switching frequency, one should find the number of the switching during the sectors it switches. Investigation of the average switching frequency for the switches in the negative end inverter is done in this part, which it can be easily related to switches in the negative end inverter due to the symmetry of this scheme.

For example in the sector 1, the positive end inverter is clamped to SV 100 and the negative end inverter is switching between SVs 100, 010, and 001. In Figure 4.7, the phase voltages are shown within two SV sampling cycle where the reference SV is located in sector 1. Since the positive end inverter is clamped in this sector, the changes in the phase voltage represent switching in the legs of the negative end inverter. Considering phase voltage $v_{aa'}$ during one sampling period in Figure 4.7, every change in the voltage represents a change in the leg a' of negative end inverter, or namely, switch S7. As it can be noted in this figure, during one sampling period, this switch experiences two "full commutations", since the pole voltage changes from zero to positive twice.

However, when the reference vector is in the next sector, sector 2, the switches of the negative end inverter, including S7, will be clamped without any switching within the sector 2. In the case of sector 3, the switches of the negative end inverter will have 2 full commutations during all the SV cycles, the same as the case in sector 1.

The process is repeated for all the sectors; which means in general each leg has 2 full commutations during sampling periods in 3 of the sectors, and in the remaining 3 sectors it has no switching since it is clamped to one state; therefore in the average sense the switching frequency of each switching device is $\frac{1}{T_s}$ where T_s denotes the SV sampling cycle.

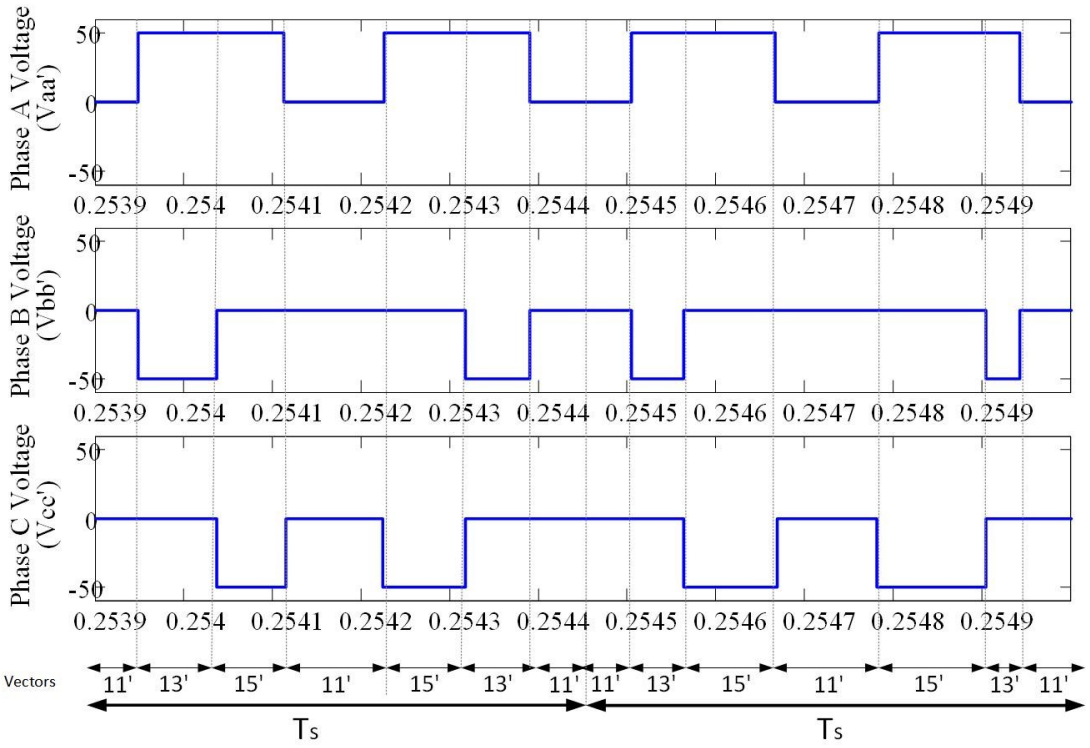


Figure 4.7. Phase voltages during two sampling periods using conventional scheme

In this project, in the implementation of the conventional scheme in Simulink, the SV cycle (T_s) is chosen to be $\frac{1}{1800}$s which results in the average switching frequency of 1800 Hz in all switches.

4.3.2 Simulation Results

Detailed simulation studies were carried out using *MATLAB/Simulink* to observe the dead-time effects on the CMV under "conventional" space vector modulation scheme. Besides, it is important to observe the effect of these modulation schemes on the quality of the load voltage and current and also the power losses in the switches. Table 4.4 summarizes the key parameters that are considered for modeling the system in simulations. The choice of the DC bus voltage will not affect the effectiveness of the method that is proposed.

Table 4-4. Parameters used for simulation studies

Parameters	Value
DC bus voltage (V_{dc})	**50 V**
m_a	**0.6**
Output voltage frequency (f)	**60 Hz**
Resistance	**10 Ω**
Inductance	**32 mH**
Dead-time	**2 µs**

Figure 4.8 shows the load voltage waveforms obtained with the conventional SVM scheme, where all the nearest SVs are used twice in a SVM cycle.

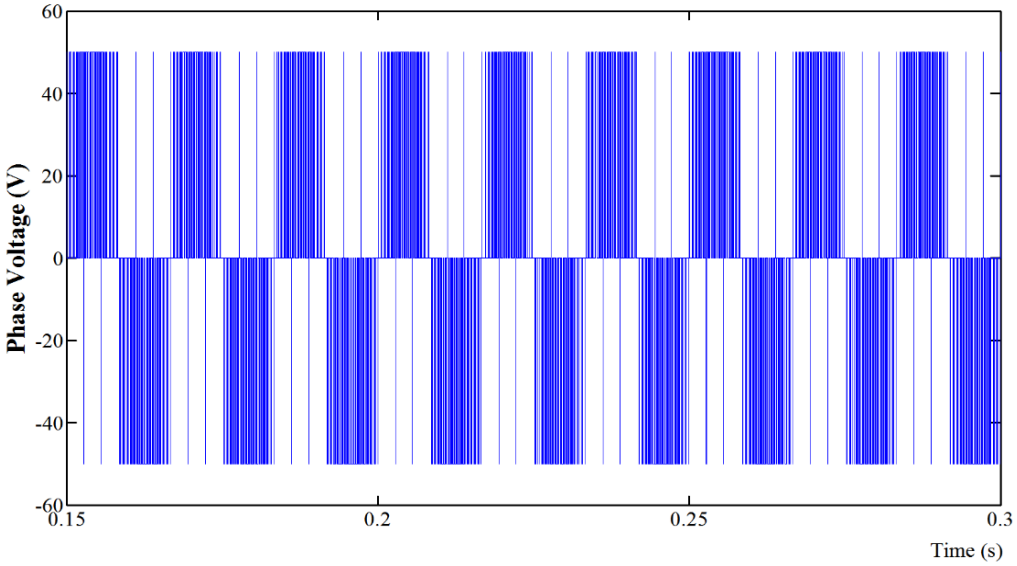


Figure 4.8. Phase voltage waveform across machine terminals, *a* and *a'*

As it can be noted in Figure 4.8, during the negative semi-cycle, there exists some positive spikes and vice versa, which are referred to bipolar spikes in this section. In each power cycle, there are six bipolar spikes in the phase voltage waveform. The bipolar spikes take place during the sector transitions as it is shown in Figure. 4.9. All the sectors start and end with the zero vector of the sector, which are 11' or 33' or 55' depending on the sector. For instance, considering the sector transition between sector 1 and sector 2, the switching state

should change from 11' to 55', which means both positive and negative end inverters will switch from 100 to 001. Therefore switch S2 and S8 in Figure 4.1, which both are connected to the ends of phase a, and S5 and S11, which are connected to the ends of phase c, should turn on. Since the switches do have dead-times in their gating signals, there is no control on the phase voltage $V_{aa'}$ and $V_{cc'}$ for the dead-time duration. Consequently, these two phase voltages depend only on the direction of the current. The currents circulate through the antiparallel diodes during the dead-time.

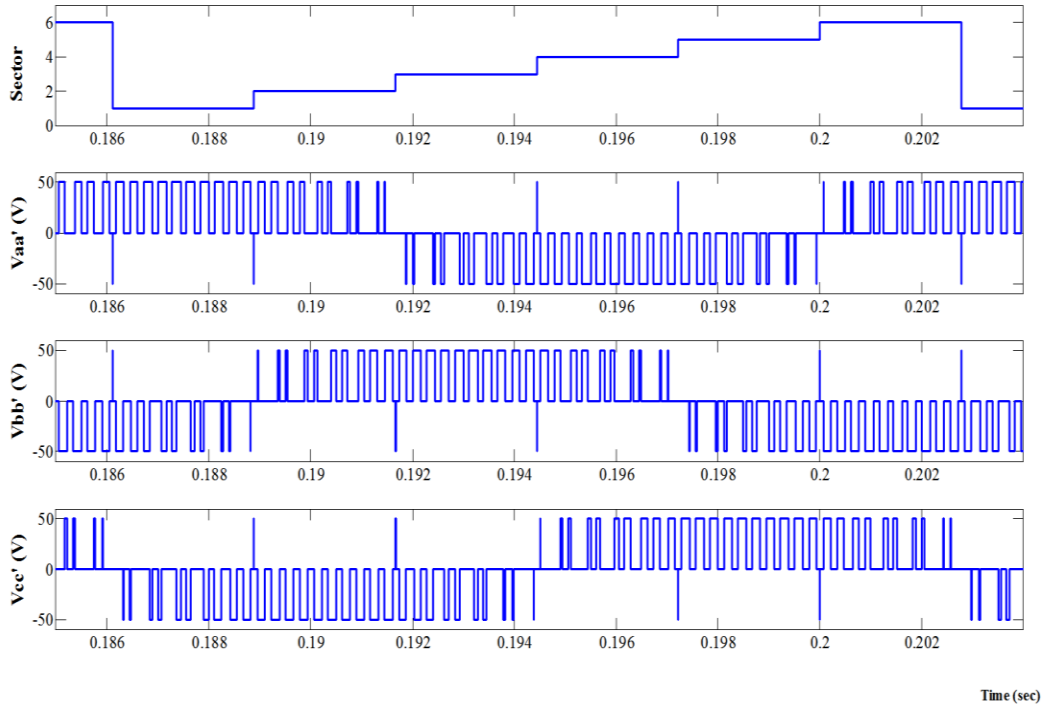
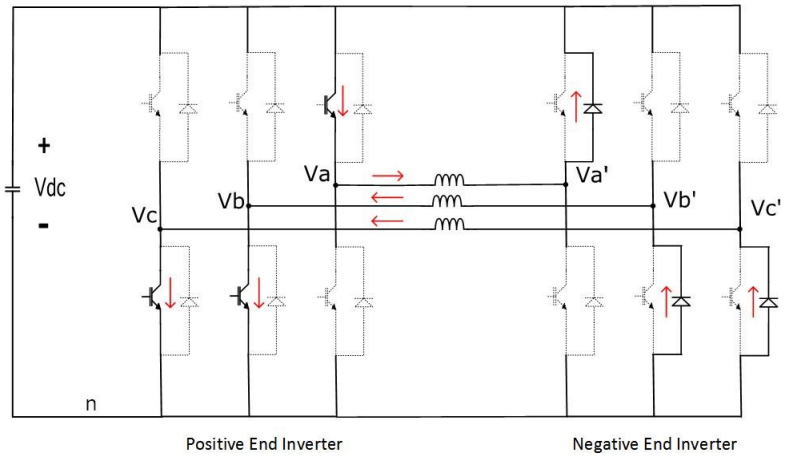
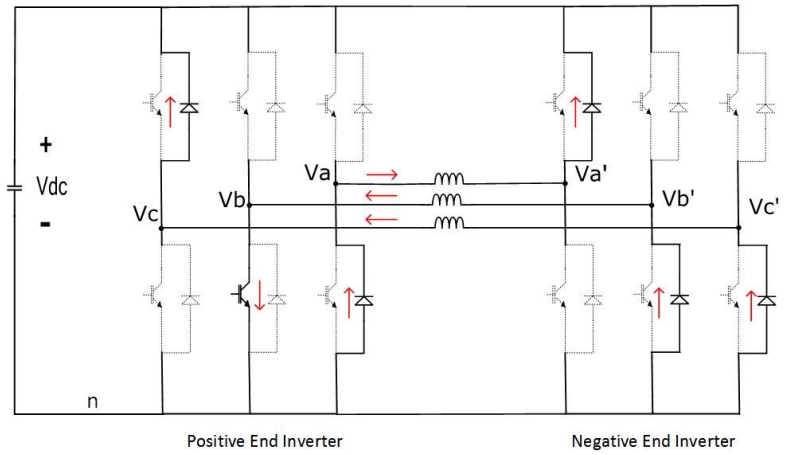


Figure 4.9. Spikes related to sector transitions in the three phase voltages

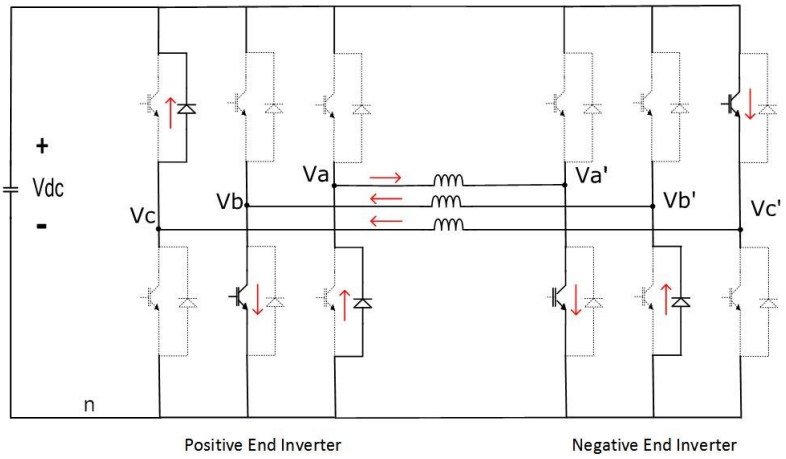
In the Figure 4.10 the inverter is shown for the SV transition 11' to 55' when the current condition is $i_a>0$, $i_b<0$ and $i_c<0$.



(a)



(b)



(c)

Figure 4.10. (a) 11' switch state (b) dead-time interval, only diodes are conducting in leg a and c (c) 55' switching state

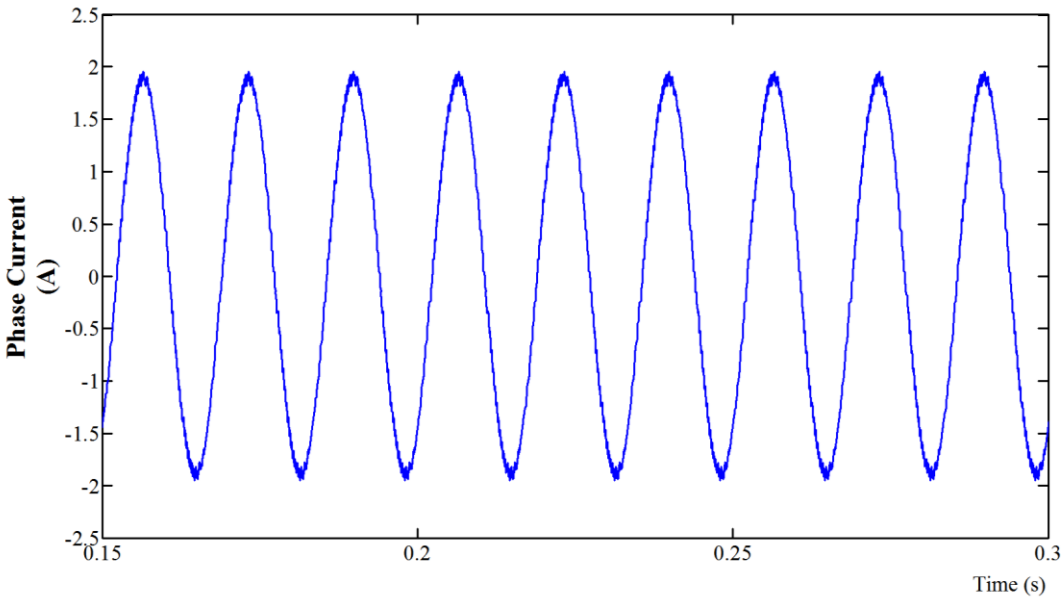


Figure 4.11. Phase *a* current using the conventional scheme

It is important to note that this bipolar spikes exist only during the sector transitions and not in each SV transition within a given sector. This is because in each sector one inverter is always clamped and therefore during the dead-time, one of the endings of the phase can be affected by the dead-time, therefore the change is not bipolar. Figure 4.9 shows the three phase voltages along with the sectors, top waveform. The current waveform using this scheme is presented in Figure 4.11.

The normalized harmonic spectrum of the phase current for operation with this SVM scheme is presented in Figure 4.12. The main harmonics are shown in close-up on the top-right corner. There, one can see that the first group of dominant harmonics components at the ac side are of order 30, which is the switching frequency of the inverter. The dominant harmonics appear around twice the SVM frequency.

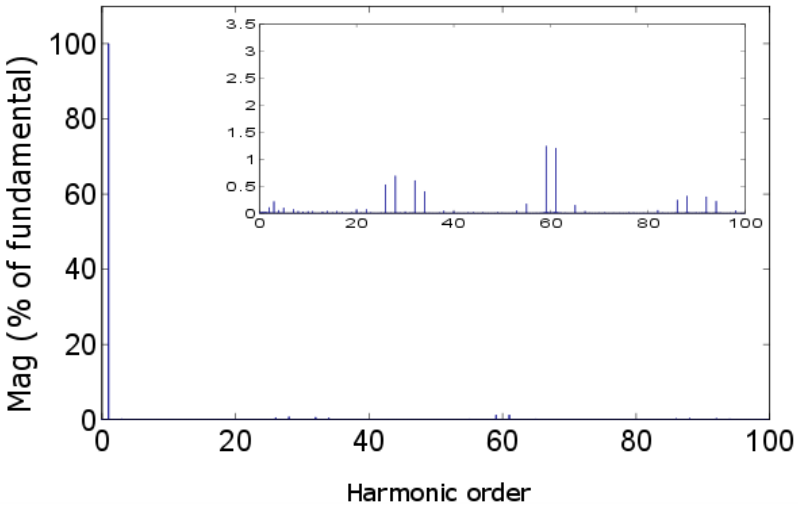
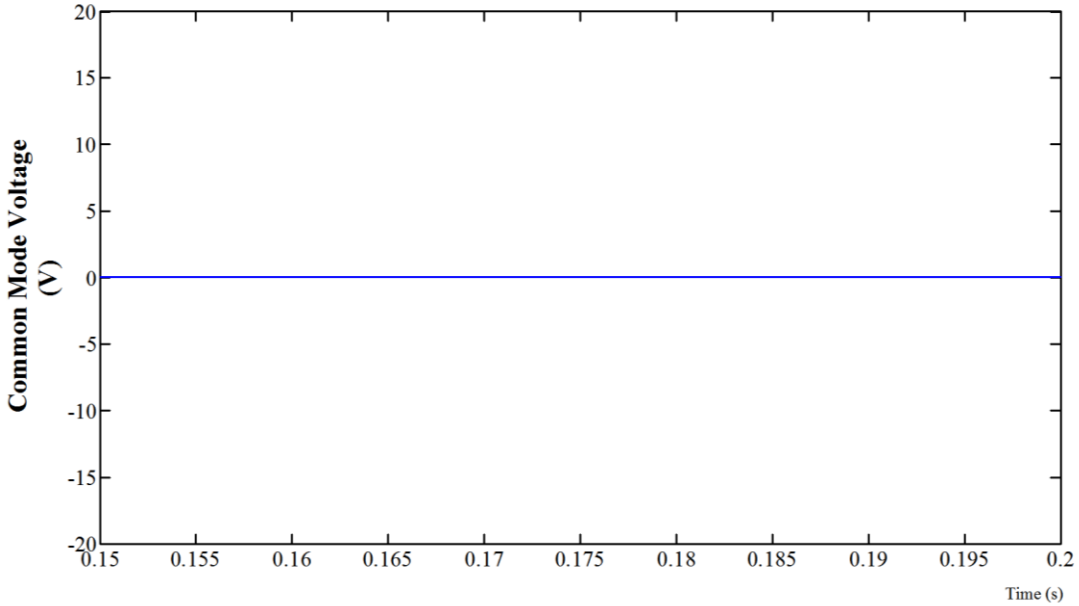
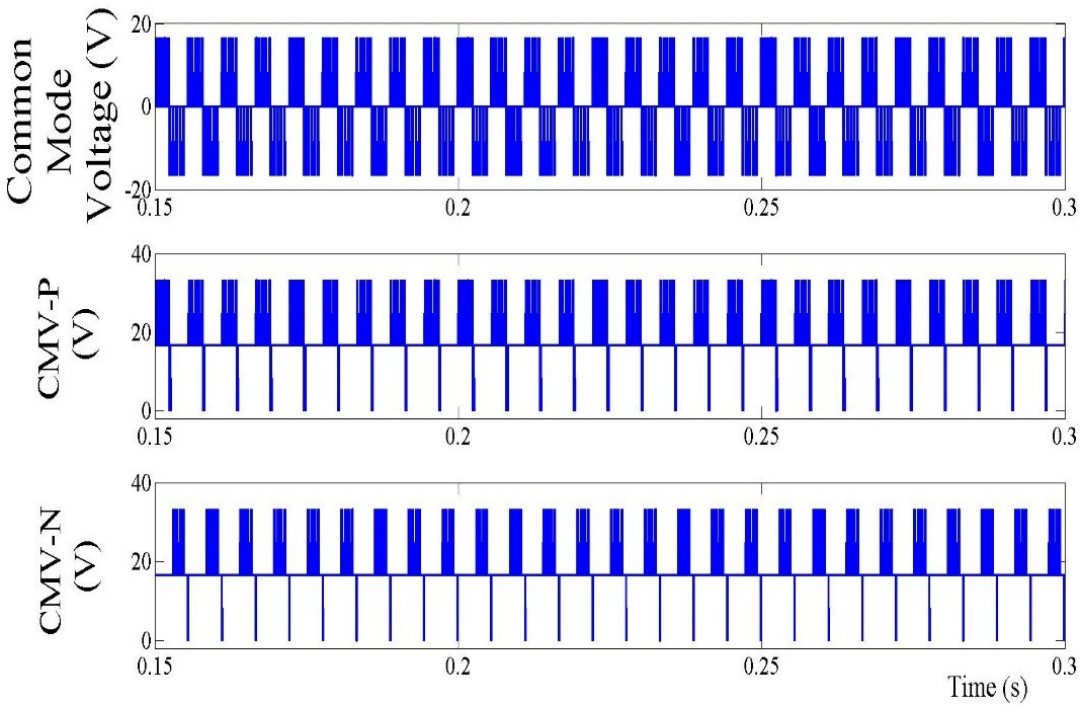


Figure 4.12. Harmonic spectrum of the phase current using the conventional scheme

Figure 4.13(a) shows the CMV for the load using the conventional SVM scheme when there is no dead-time for the gating of the switches. It can be observed that the CMV is cancelled completely in this case by using only the odd vectors as it was discussed in the previous chapter. Figure 4.13(b) shows the CMV when the switches do have dead-time, it is evident that in this case, the common mode voltage is not equal to zero for each instant and that during the dead-time periods, there is a change in the CMV.



(a)



(b)

Figure 4.13. Common mode voltage for the conventional scheme (a) without dead-time and (b) with dead-time of T_d=2 μs.

CMV disturbances due to the dead-time occurs only when the legs with the same direction switch simultaneously. Figure 4.14 demonstrates the appearance of the spikes more in details. As it can be noted in this figure, spikes in CMV are created during specific SV transitions, but not for all transitions. For instance, the first spike on the left in the figure occurs during the transition of SVs 35' to 55'. In this transition, phase b and c of the positive end inverter should switch and there will not be any change in the switching states of phase a. As it can be noted from the figure, current direction in phase b and c are both negative. It was discussed in section 3.2 that when the two legs of the inverter switch simultaneously, the spike can be appeared provided that these phases have the same current direction. Therefore the dead-time can cause a spike in the common mode voltage in this specific SV transition.

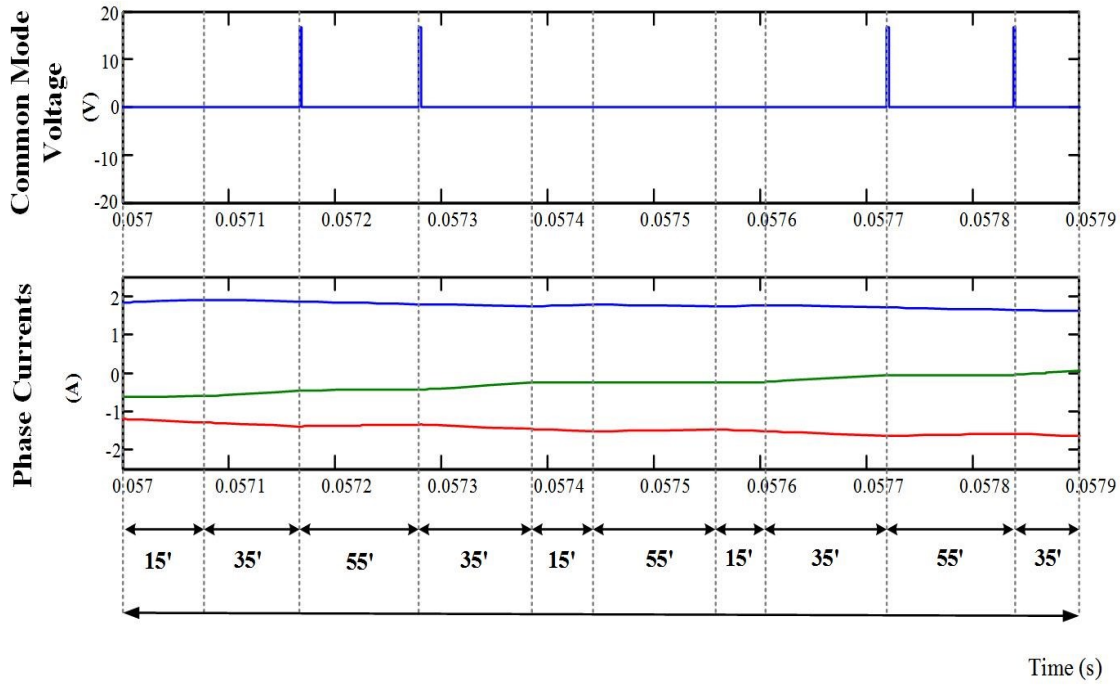


Figure 4.14. Spikes in CMV during the SV transitions and thee phase currents, ia, ib and ic are in blue, green and red colors respectively

4.4 The Proposed SV Sequence

In this proposed scheme, the SV sequence is designed in such a way to suppress the CMV spikes that takes place during the dead-time. As it was discussed in Chapter 3, finding the proper sequence, requires the knowledge of the polarity of the load currents. Therefore, three current sensors are added to the circuit since phase currents should be known, to ensure only phase legs with opposite current directions switch. The proposed sequences of SVs for all sectors are presented in Table 4.5.

Table 4-5. Sequence of Vectors in the proposed scheme

	Phase Current with the different polarity	**Sequence to eliminate CMV due to the dead-time**
Sector 1	i_c	11'-15'-13'-15'-11'
	i_b	11'-13'-15'-13'-11'
	i_a	11'-13'-11'-15'-11'-13'-11'
Sector 2	i_c	55'-15'-55'-35'-55'-15'-55'
	i_b	55'-35'-15'-35'-55'
	i_a	55'-15'-35'-15'-55'
Sector 3	i_c	33'-35'-31'-35'-33'
	i_b	33'-35'-33'-31'-33'-35'-33'
	i_a	33'-31'-35'-31'-33'
Sector 4	i_c	11'-51'-31'-51'-11'
	i_b	11'-31'-51'-31'-11'
	i_a	11'-31'-11'-51'-11'-31'-11'
Sector 5	i_c	55'-51'-55'-53'-55'-51'-55'
	i_b	55'-53'-51'-53'-55'
	i_a	55'-51'-53'-51'-55'
Sector 6	i_c	33'-53'-13'-53'-33'
	i_b	33'-53'-33'-13'-33'-53'-33'
	i_a	33'-13'-53'-13'-33'

To obtain the gating signals for all the switches, the following procedure has been implemented in *MATLAB/Simulink*.

1) Sample the instantanous values of the reference voltages for the three phases
2) Compute the reference space vector $\overrightarrow{V_s}$, using equation (4.1) and (4.2)
3) Determine the angle of the reference vetor, $\overrightarrow{V_s}$, with respect to the α axis and employ Table 4.1 to find the sector in which the reference vector is located

4) Calculate the dwell time for the zero and the active vectors using equation (4.9)
5) Sense the instantanous phase currents
6) Select the proper SV placement according to Table 4.5

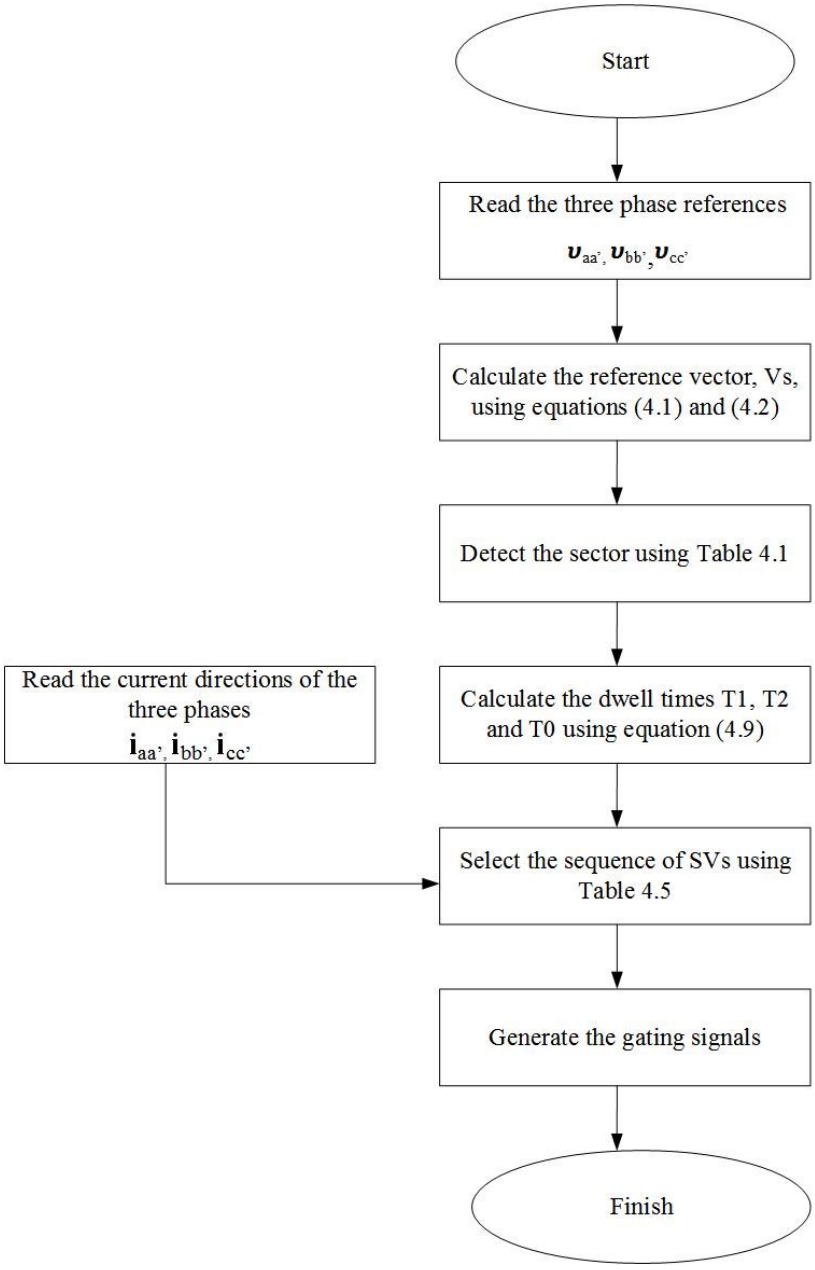


Figure 4.15. Schematic diagram of the proposed space vector modulation in OEWM during one sampling cycle

The flow chart of the algorithm is shown in Figure 4.15 demonstrates the procedure to generate the gating signals in this proposed scheme.

4.4.1 Simulation Blocks

This section details the step-by-step development of the model. The overall circuit of the three phase open ended winding load that is developed in MATLAB/Simulink is shown in Figure 4.16.

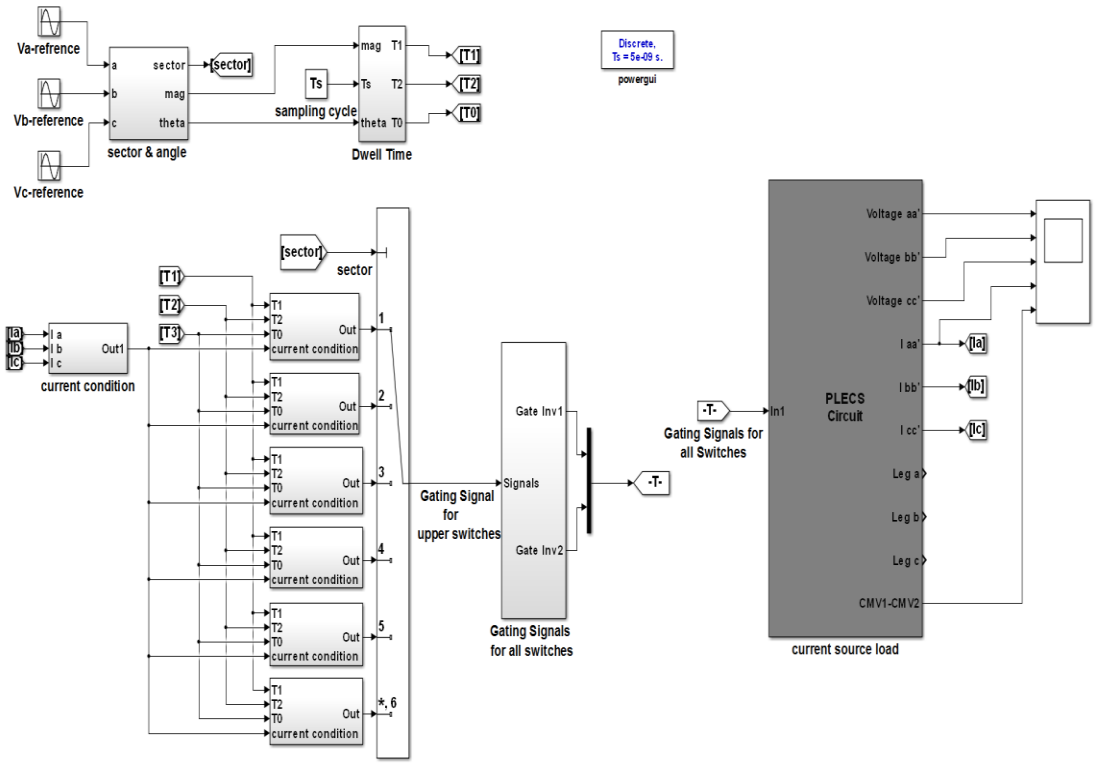


Figure 4.16. Scheme of open end winding machine and generating gating signals in Simulink

This simulation circuit includes two main parts. The function of the first series of blocks is to generate the gating signals using the formulas that are discussed in section 4.2, to generate the gating signals and control the power switches i.e. IGBTs and Diodes. The second part consists of the power circuit and the open ended winding load. Power circuit is developed in PLECS subsystem in MATLAB to enable power loss calculation in the switches. The performance of the blocks are explained briefly in the following.

1) Determine sector and the angle theta of the rotating reference vector in each sampling cycle

Using equation (4.1) and (4.2) the three phase voltages can be represented in αβ plane and the sector in which the reference vector is located can be calculated using Table 4.1. Output of the block in Figure 4.17 is named as 'sector' which is a number between 1 and 6.

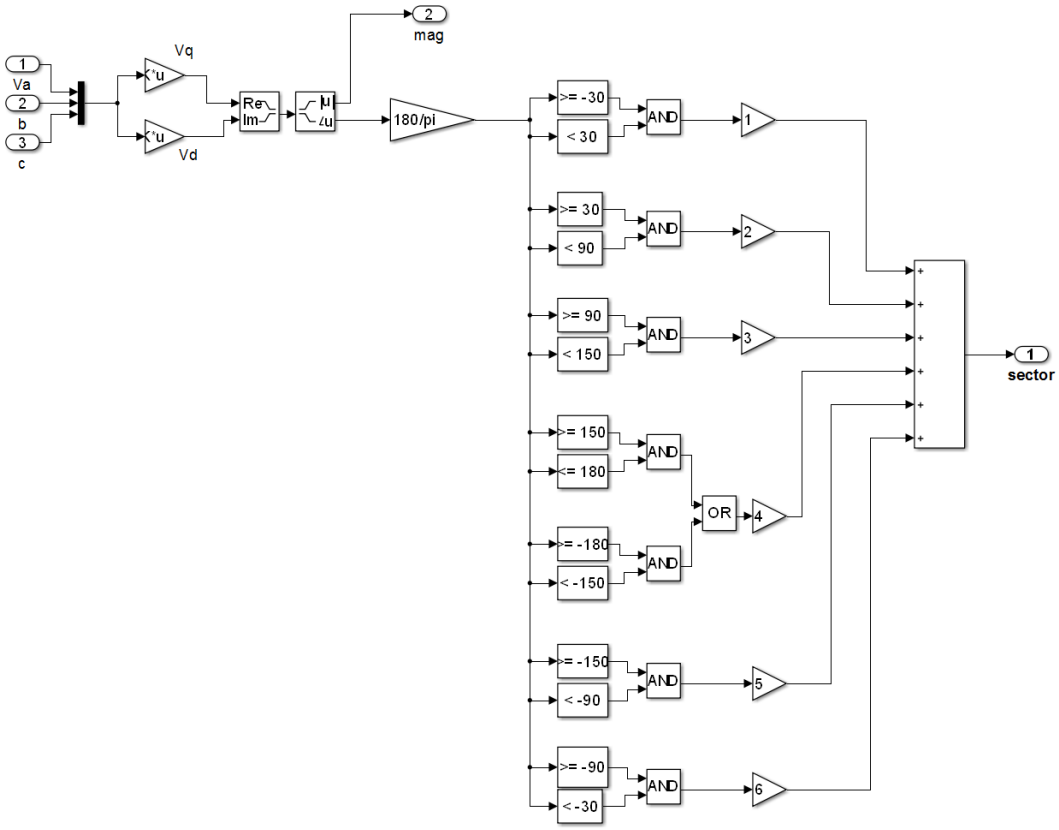


Figure 4.17. Sector determination

The angle **θ** is also calculated in this block using Table 4.2. To avoid the repetition the block set is not shown in this part.

2) Calculate the dwell time for active and zero vectors T_1, T_2 and T_0

Obtaining the dwell times for active and zero vectors of the section requires the knowledge of the angle **θ** and the magnitude of the reference vector. This block represents the calculation of the dwell times as was described in equation (4.9) using the function blocks.

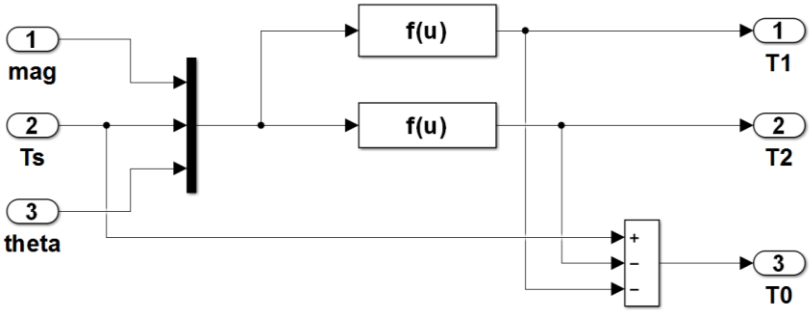


Figure 4.18. Dwell time calculation

3) In the proposed method, finding the proper sequence of the space vectors during the sampling period, requires the knowledge of the current directions and finding the phase current with different polarity. The following block determines the current condition in order to select the proper switching order. The output of this block is a number between 1 and 3 which indicates three different cases for the current. i.e. output 1 of this blocks indicates ic has the different polarity than the two others.

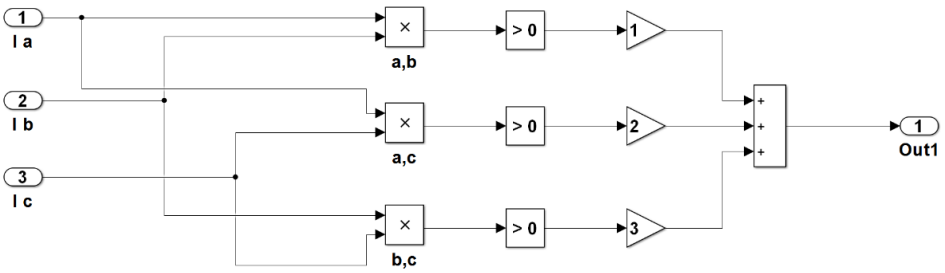


Figure 4.19. Current condition selection in order to find the phase with different polarity

Within each sector there are three blocks representing the three different sequences proposed in Table 4.5. Having the knowledge of the current condition, the proper sequence can be chosen.

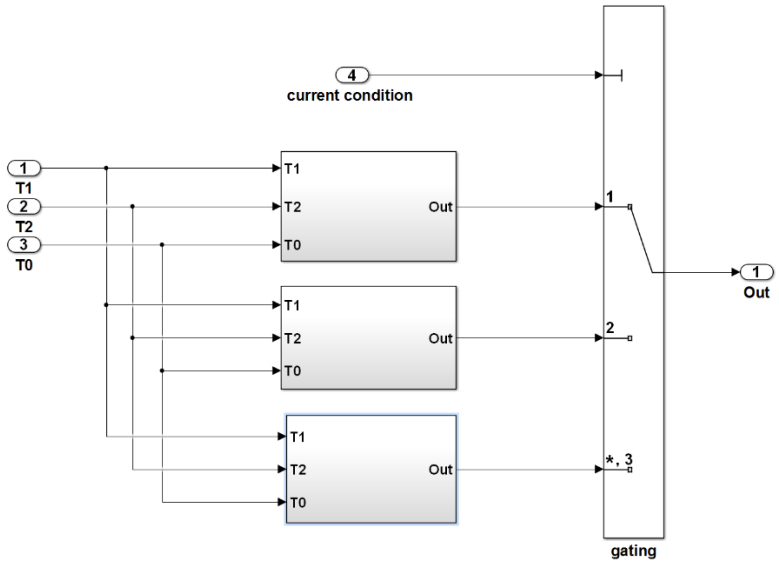


Figure 4.20. Proper sequence should be selected in each sector from the three options according to the current condition

4) Timing to change the switch

Considering the reference vector is located in sector 1 and has the first current condition. Therefore, according to Table 4.5, the space vectors should be placed as: 11'-15'-13'-15'-11' in the SV sampling cycle. The timing associated with each vector (T_1, T_2, T_0) was calculated using the previous blocks. To align the space vectors in this sequence, there are 5 timing steps which is shown in Figure 4.21.

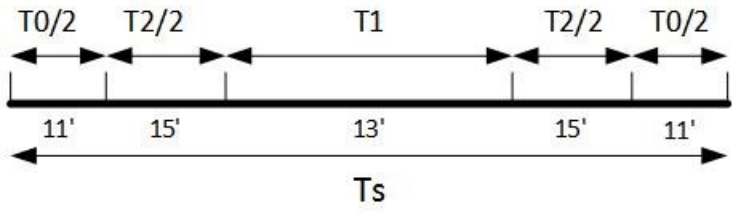


Figure 4.21. aligning the selected space vectors in proper sequence

Because of the symmetry of the sequence, to reduce the calculation in MATLAB/Simulink, only 3 timing step is considered and then by mirroring the steps, one can obtain the full 5 steps. The following block implements this logic to find the proper switch at any instant during the sampling cycle.

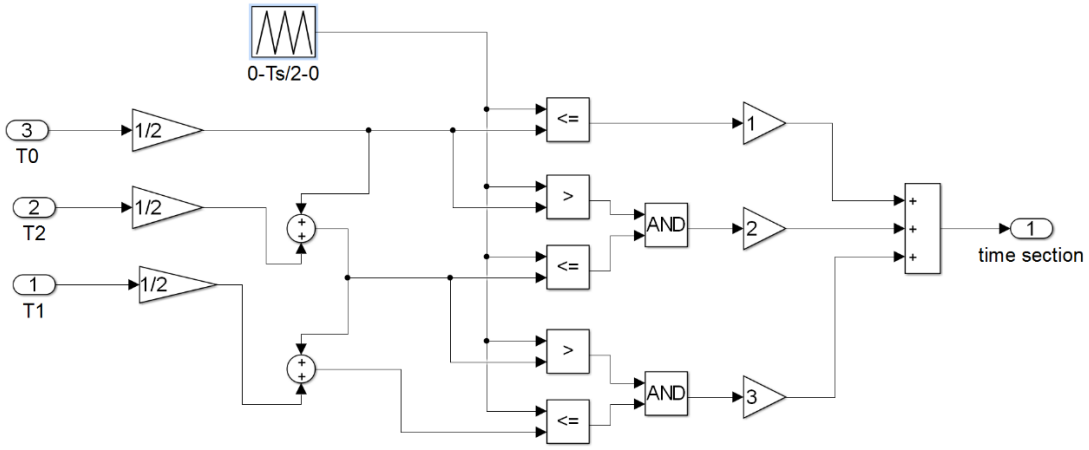


Figure 4.22. Determining the time steps

The output of this block is a number between 1 and 3 which is depicted in Figure 4.23 within one sampling cycle.

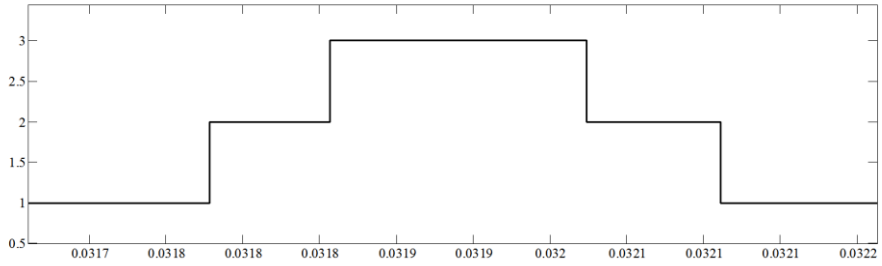


Figure 4.23. Timing steps during sampling cycle with 5 SVs in the sequence and symmetrical SV alignment

This output decides which switching state should take place at any given instant. For instance, when the output of the block in Figure 4.23 is 1, this time step is associated with

first switching state, i.e. 11'. It is notable that the number of the timing steps can vary depending on the number of the SVs placed in a sequence in one sampling cycle.

Figure 4.24 depicts the selection of the proper switching state after determining the timing steps.

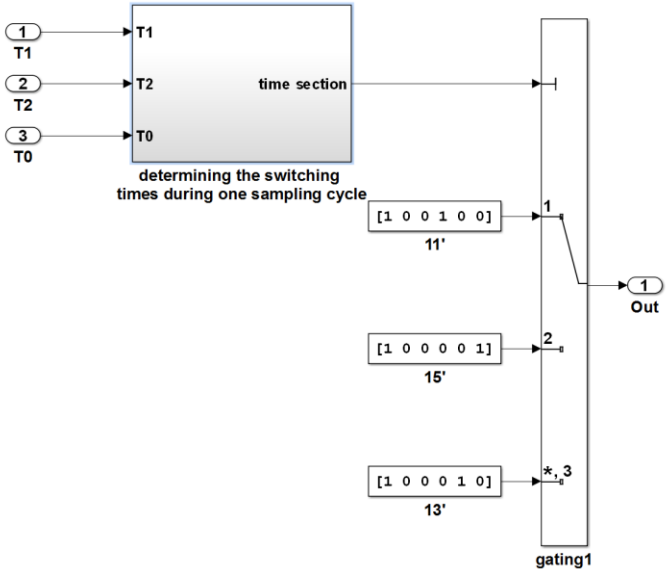


Figure 4.24. Generating the final switching pulses

This output results in the gating signals only for the upper switches in 6 legs. Another block is required to produce the complementary signal for the lower switches.

5) Power circuit in PLECS

Figure 4.25 shows the power circuit. This block consists of the power circuit itself along with additional blocks for calculating the conduction and switching losses in the power switches.

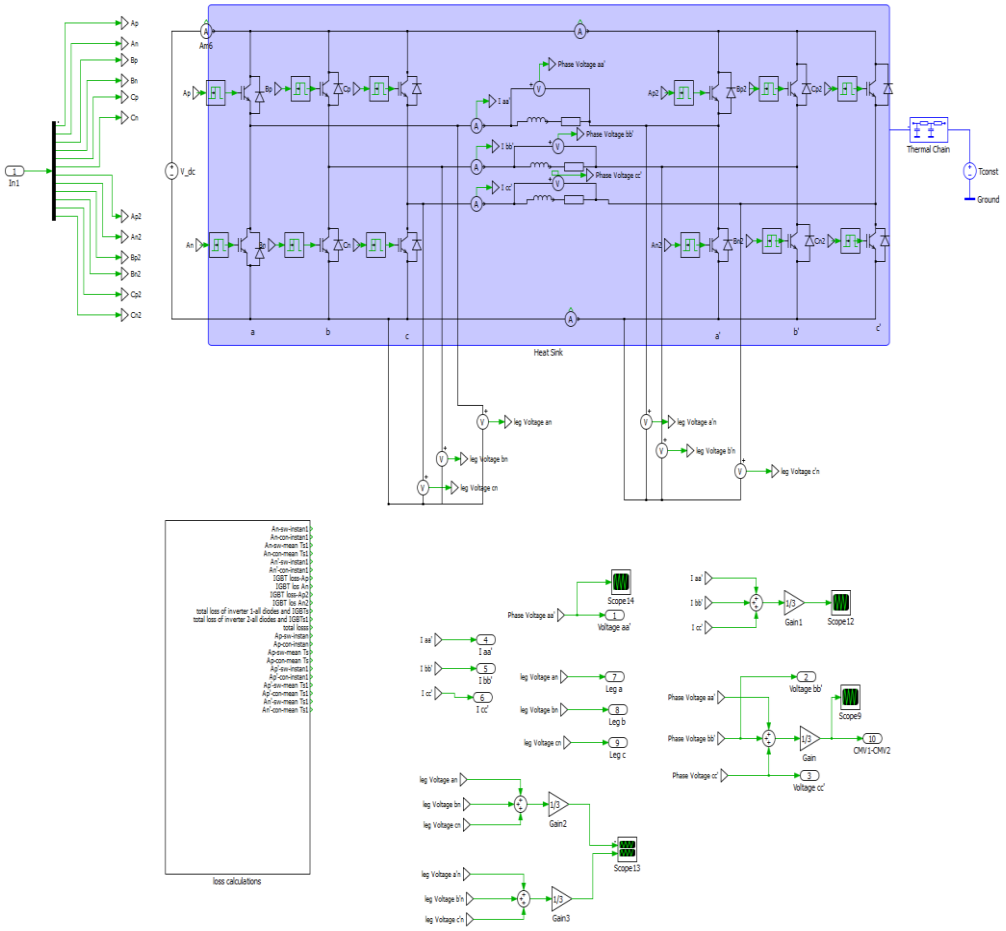


Figure 4.25. Power circuit in PLECS/MATLAB

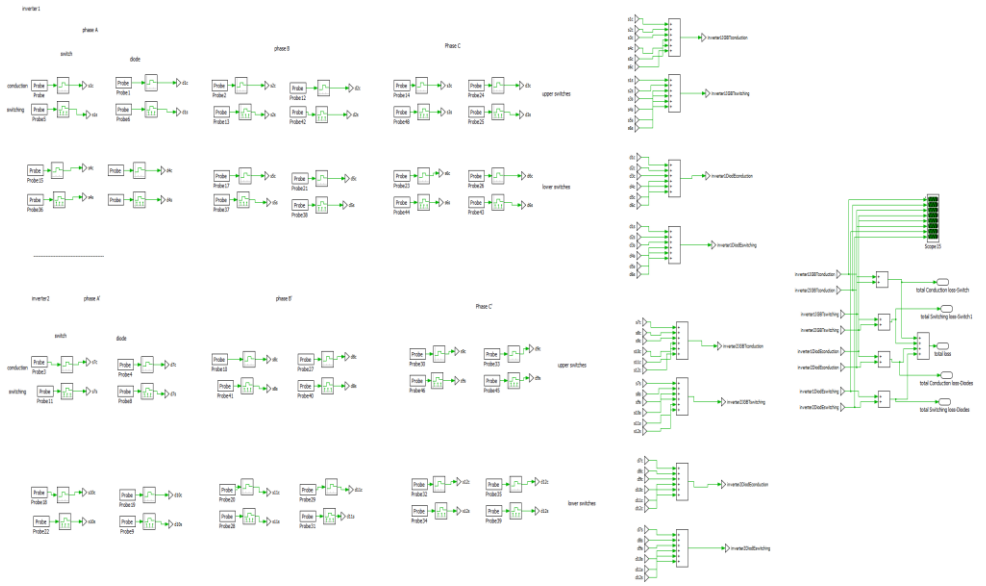


Figure 4.26. Inside the PLECS circuit/ loss calculations

4.4.2 Average Switching Frequency

The procedure to find the average switching frequency in this section is similar to that in section 4.3.1. Figure 4.27 shows the load voltage waveforms during 2 SV sampling cycles when the dual 2-level converter operates in Sector 1, and i_b has a different polarity from the two other currents. The selected sequence, according to Table 4.5, is: 11'-13'-15'-13'-11'. The positive end inverter is clamped at SV 1(100). Therefore the changes in the phase voltage represent the switching in legs of the negative end inverter. There one can see that while leg *b* of the negative end inverter presents two full commutation in this SV sampling cycle, legs *a* and *c* present only one.

In general, in this scheme all the switches will not necessarily have 2 full commutation within one SV sampling cycle and depending on the current condition and the choice of the SV sequence in Table 4.5, the switch can have one, two, three, or zero commutations within each sampling cycle. The average switching frequency should change in this scheme depending on the power factor of the load.

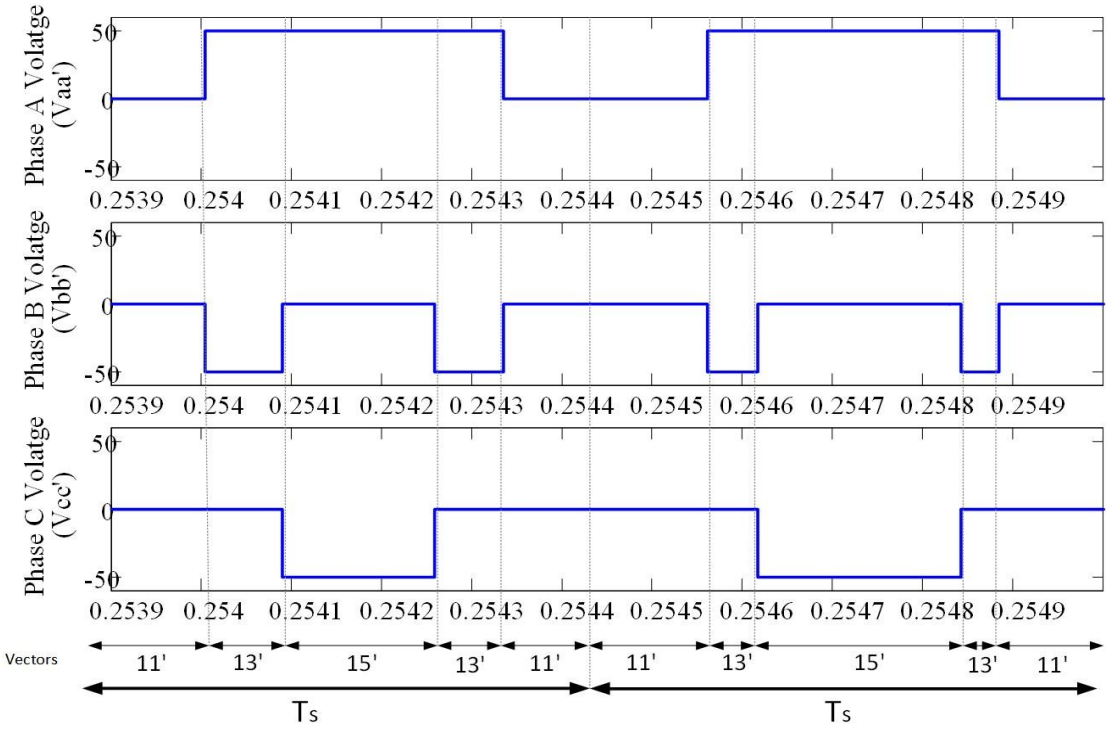


Figure 4.27. Phase voltages during two sampling periods using proposed scheme

Considering the given load of $R = 10\ \Omega$ and $L = 32\ mH$, the average switching frequency is related to the SV cycle as below:

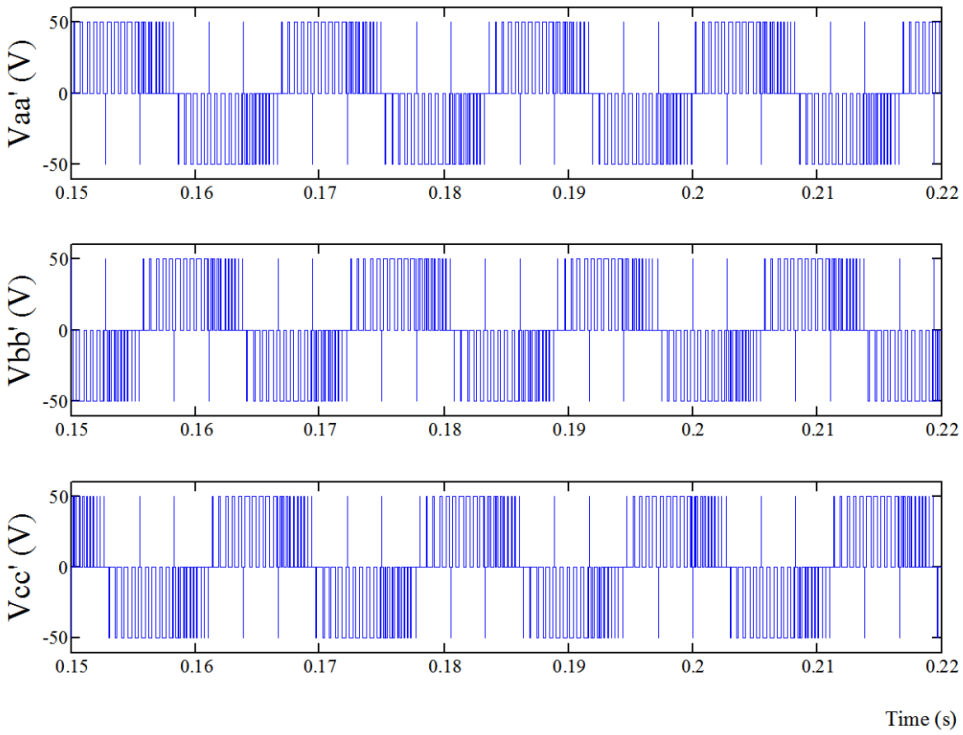
$$f_{sw-averages} = \frac{2}{3}\frac{1}{T_s}$$

4.4.3 Simulation Results

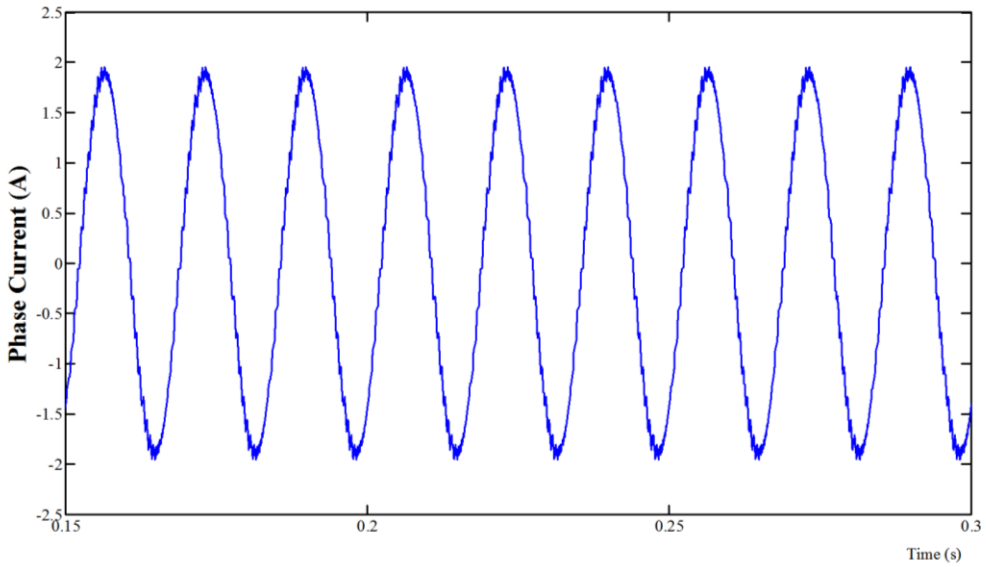
Simulation studies were carried out using *MATLAB/Simulink* to observe the dead-time effects on the CMV under "proposed" space vector modulation scheme. In this study, the main parameter of the system are similar to the previous study, which was presented in Table 4.4.

Voltage waveforms of the three phases and the current waveform are shown in Figure 4.28(a) and 4.28(b) respectively. Bipolar spikes which appear on the output voltage are due to the sector changes and the double commutation of the switches on both ends of the winding, which was discussed in previous sections more in details.

It should be noted that in the load voltage waveform, there are more pulses in one phase voltage than in the other two for the duration of 60 degrees. The more switching in all the phases comes from the fact that in some sectors, some phases/legs have only one full commutation in the SV cycle, but one phase would have two full commutations, as it was discussed in the previous section. The phase with two commutations per SV cycle will experience more switching in that period.



(a)



(b)

Figure 4.28. (a) Three Phase voltages and (b) phase *a* current using the proposed scheme

The normalized harmonic spectrum of a phase current for operation with the proposed SVM scheme is shown in Figure 4.29. In this case, the dominant harmonics appear around the SVM frequency.

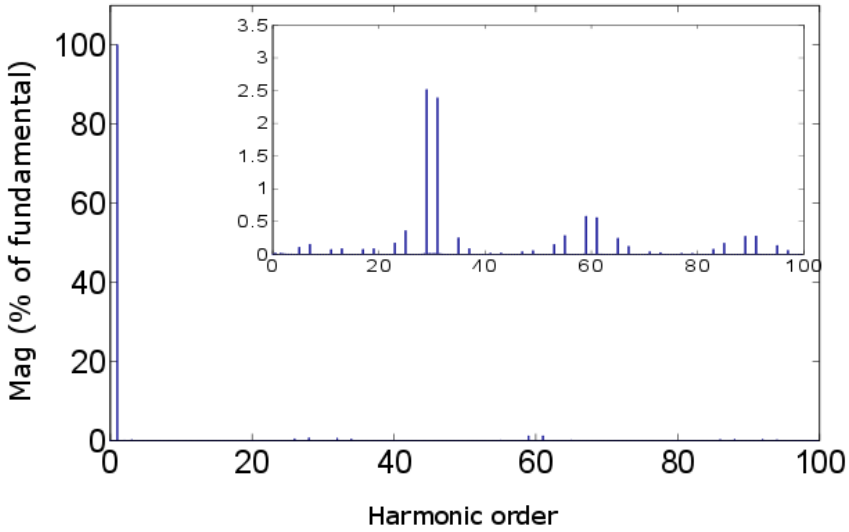


Figure 4.29. Harmonic spectrum of the phase current using the proposed scheme

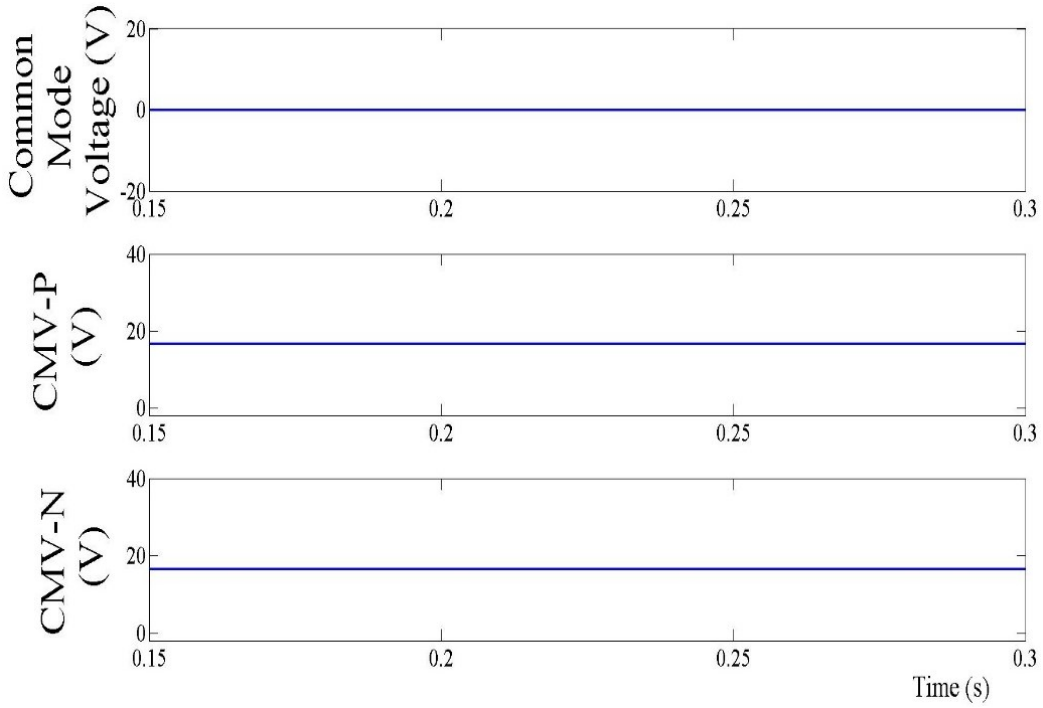


Figure 4.30. Common mode voltage with the proposed SVM scheme (dead-time of T_d=2 μs)

Figure 4.30 demonstrates that the proposed common mode suppression method works as expected. As a result of using the proposed scheme, the common mode voltage at both sides, are kept constant.

Figure 4.31 shows the comparison of the phase voltage %THD of the two control strategies for different modulation indices. The %THD is higher in the proposed scheme since the average frequency is reduced. Note that the SV sampling cycle is equal to $\frac{1}{1800}$ s for both schemes.

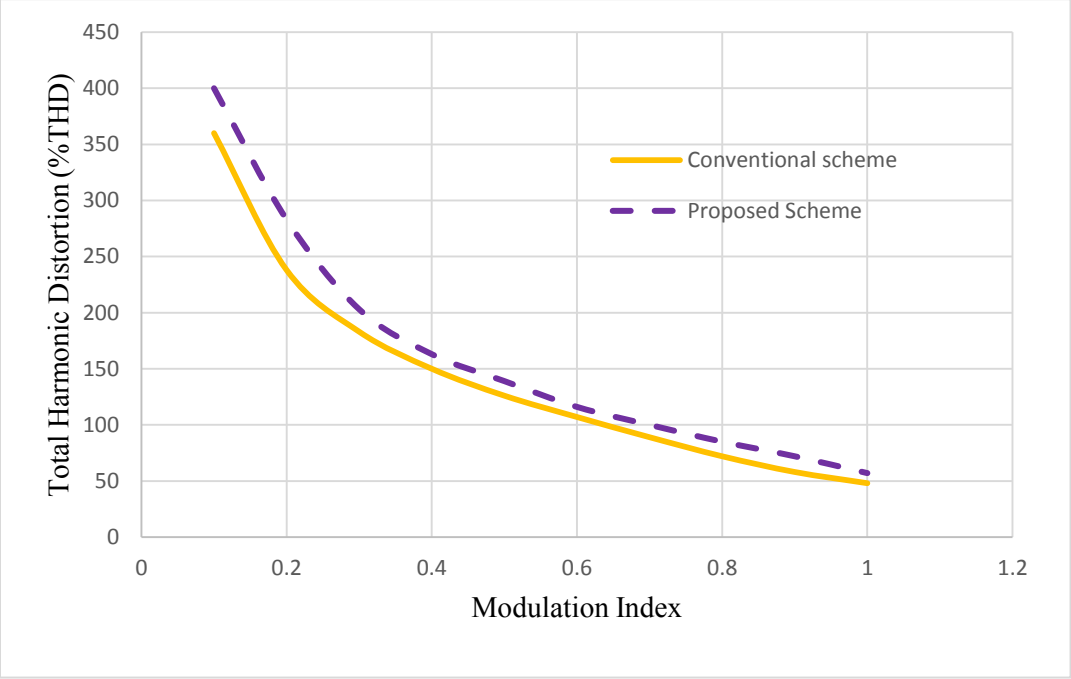
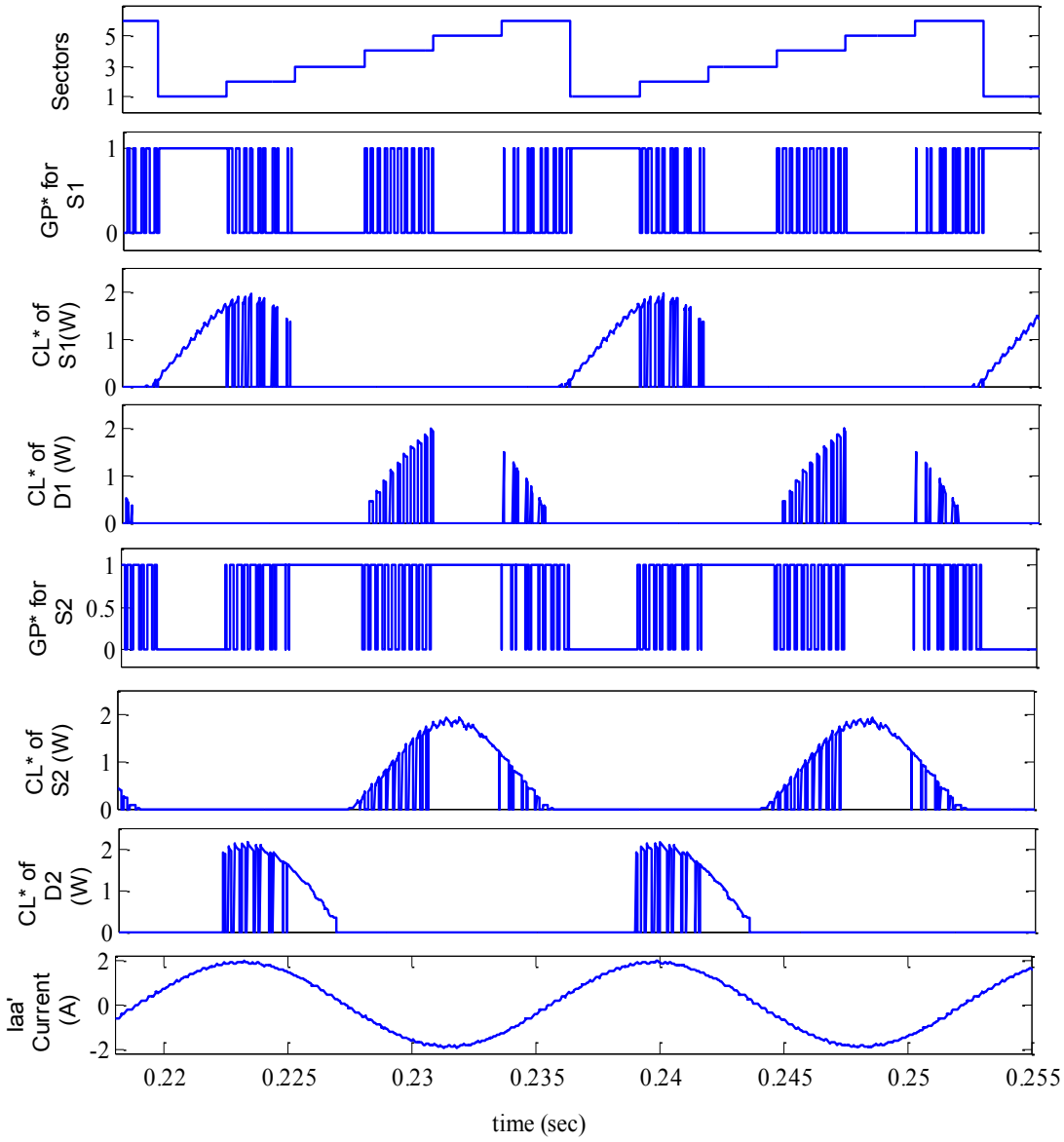


Figure 4.31. Total Harmonic Distortion of the voltage waveform, using the conventional and the proposed scheme, having equal sampling times

4.5 Switching and Conduction Losses in Switches

Switching and conduction losses are functions of the load current and voltage across the power devices. *PLECS* tool in *MATLAB* was used for calculating the power losses in the switches and diodes, and Infineon FS400R12A2T4, 600 V IGBT module is used to model the properties of the switches.

In the scheme using only odd vectors to eliminate the common mode voltage, there is an unbalance in conduction losses of the lower and upper switches in each leg. Figure 4.32 shows the gating signals and the conduction loss of the upper and lower switch and their antiparallel diodes of leg *a* in positive end inverter.



*GP – Gating pulses
*CL-Conduction Losses

Figure 4.32. Waveforms from top to bottom: Sectors of the reference voltage, gating signals for S1, conduction loss of switch S1, conduction loss of diode D1, gating signal for S2, conduction loss of switch S2, conduction loss of diode D2

In Table 4.6 the average conduction and switching losses is presented for upper and lower switches of leg a.

Table 4-6. Average losses in the upper and lower switch of the leg

	Conduction Loss (W)	**Switching Loss (W)**
Upper switches (IGBT plus Diode)	0.344	0.022
Lower switches (IGBT plus Diode)	0.766	0.026

Since the conduction losses for both inverters are similar, in this section conduction losses are evaluated only for one of the inverters, the positive end inverter. Considering the case for the positive end inverter, it is clamped to SV 1(100) in sector 1, SV 3(010) in sector 3, and SV 5(001) in sector 5. It means switch S1 in leg a of the positive end inverter is clamped to the on-state in sector 1, and clamped to the off-state during two sectors of 3 and 5; however the complementary switch S2 will remain off during sector 1, and on for two sectors of 3 and 5. This will result in higher conduction losses for the lower switch in this leg. This is the case for all the lower switches, they are clamped to on-state for two sectors, and to the off-state for only one sector, while the upper switches are on during one sector, and clamped to the off-state during two sectors. Therefore, the conduction losses are higher in the lower switches of each leg compared to the upper switches. To balance the inverter in terms of losses, one can use odd and even vectors every other power cycle.

The overall inverter losses of the conventional and proposed schemes are shown in Table 4.7. The actual values of the losses of the inverter switches in this case study, are not representative of the losses one would find in a practical EV drive system because of the use of the parameters of 600 V switches in a system with a voltage of 50 V dc and high load impedance.

Table 4-7. loss and THD comparison between the conventional and the proposed scheme

	Current %THD	**overall Losses in Inverter (W)**
Conventional Scheme	2.2	6.949
Proposed Scheme	3.67	6.887

4.5.1 Even Vectors Sequence

For eliminating the effect of dead-time on the common mode voltage, the same procedure can be applied when one is only using the odd vectors. Because for the transition between two odd vectors, there are still two switch transitions, one switch turn off and the other should turn on, for instance considering the switching between **2(110)↔4(011)**, leg *a* should turn off, and leg *c* should turn on, an there is no change in phase *b*. the same theory is applicable in this case, which is to cancel the instantaneous error due to dead-time, one should only switch the legs with different polarities in the same inverter at each instant. For example, consider the transition from 110 to 011, if the phase *a* and *c* has different current polarities, the dead-time will not disturb the common mode voltage, otherwise there will be a spike in the common mode voltage. Table 4.8 shows the suggested sequence to eliminate the disturbance of dead-time in common mode voltage using only even vectors.

Table 4-8. Proposed sequence of vectors with even SVs in both inverters

	Phase with the different current polarity	**Sequence to eliminate CMV due to the dead-time**
Sector 1	i_c	**44'-24'-64'-24'-44'**
	i_b	**44'-64'-24'-64'-44'**
	i_a	**44'-64'-44'-24'-44'-64'-44'**
Sector 2	i_c	**22'-24'-22'-26'-22'-24'-22'**
	i_b	**22'-26'-24'-26'-22'**
	i_a	**22'-24'-26'-24'-22'**
Sector 3	i_c	**66'-26'-46'-26'-66'**
	i_b	**66'-26'-66'-46'-66'-26'-66'**
	i_a	**66'-46'-26'-46'-66'**
Sector 4	i_c	**44'-42'-46'-42'-44'**
	i_b	**44'-46'-42'-46'-44'**
	i_a	**44'-46'-44'-42'-44'-46'-44'**
Sector 5	i_c	**22'-42'-22'-62'-22'-42'-22'**
	i_b	**22'-62'-42'-62'-22'**
	i_a	**22'-42'-62'-42'-22'**
Sector 6	i_c	**66'-62'-64'-62'-66'**
	i_b	**66'-62'-66'-64'-66'-62'-66'**
	i_a	**66'-64'-62'-64'-66'**

4.6 Conclusion

Common mode voltage in the open end winding machine can cause problems such as zero sequence current and increased switch losses. It has been shown in the literature that employing specific voltage vectors in the space vector modulation is capable of eliminating the common mode voltage. However, no solution has been proposed to avoid the CMV created by the inherent dead-times. In the chapter 3, a control scheme is proposed based on the direction of the current and realignment of the SVs in the sequence to cancel the effect of dead-time on the common mode voltage.

In this chapter, a comparative study is performed between the conventional scheme and the proposed schemes of chapter 3, using *MATLAB/Simulink*. The simulation results for the conventional scheme is presented with the existence of dead-time in the circuit, which lead to having several spikes on the common mode voltage. Using the proposed control strategy, it was shown that it can eliminates the spikes in the common mode voltage, which were present in the conventional scheme successfully.

It also has been shown that the quality/distortion of the load waveforms as well as the switch losses are fairly comparable between the conventional scheme and the proposed scheme. Switching and conduction losses in power switches were studied using PLEXIM toolbox. It was shown that the total losses of the lower switches are higher with comparison to that in upper switches, which can affect the lifetime of the switches.

Chapter 5

Conclusions

This thesis explores the problem of high frequency common mode voltages in open end winding machines. The purpose of this work is to improve the performance of the open end winding machines connected to dual 2-level inverters supplied by a single DC bus voltage source.

In open end winding structure, one can provide pulse width modulated voltages at both sides of the machine windings. There is parasitic capacitive current path between the parts of the electrical machine and the ground. This capacitance are very small and can be neglected in low frequency range. However, at high frequencies, the current through these parasitic capacitance cannot be neglected. CMV causes such undesired currents to flow through the inverters and the windings of the machine.

In the open end winding configuration where the power is supplied by a single DC voltage source, the circulation of the zero sequence currents between two inverters is considered as the major drawback. This current can increase the switching losses without delivering power to the load. In this thesis a space vector modulation scheme is proposed to reduce the problems caused by common mode voltages during dead-time interval in this configuration.

There are several techniques in the literature that proposes methods to mitigate the detrimental effects of common mode voltages at the machine terminals. Proper PWM strategies can be considered as an elegant common mode voltage reduction technique. It can lead to the elimination of bearing currents and reduction of conducted electromagnetic

interference (EMI). The magnitude of the common mode voltage depends on the switching states and the voltages at the phase terminals. Therefore, using appropriate choice of switching pattern can eliminate the problem. Switching states that generate the maximum common mode voltage can be replaced by other switching states. On the other hand, this technique can lead to reduction of the linear operation range of the drive resulting in current distortion at higher speeds. Higher current ripple will lead to higher ripple in shaft torque of the machine. Dead-time delay, which are used in the gating drives to prevent shoot through of the DC source, is the second important factor in generating the common mode voltages.

In this thesis, the problem of the common mode voltage in three phase open end winding configuration was explored in depth. The study proposed switching patterns to eliminate the dead-time effects on the CMV for open end winding machines. The relation between the current direction and spikes in common mode voltage was studied. Towards obtaining a solution for the high frequency spikes in the common mode voltage in the presence of dead-time, a new space vector modulation technique was also proposed. It was showed that the switching pattern can be altered depending on the current direction in order to cancel the effect of dead-time on common mode voltage. Simulation results are presented to verify the operation of the modulation scheme and the results show that the objective can be satisfied by incorporating the proposed modulation strategy. This project presents a performance comparison of the conventional and the proposed modulation strategies in terms of the quality of the line currents and phase voltages.

Switching losses and conduction losses in IGBT switches and diodes are studied in this thesis. This provides a valuable insight for estimating the life time of the switches. It was shown that there exists an imbalance in conduction losses among upper and lower switches using this modulation scheme which can be investigated in the future. The same method also can be extended to other multilevel topologies. It will be valuable to investigate this issue and propose methods for equalizing power losses. The proposed modulation technique can be experimentally verified. In order to implement the proposed switching pattern, a high resolution hardware PWM module in which the dead-time duration can be controlled should be used. In order to obtain a reasonable accuracy in the outputs, the

modulation resolution of the system should be very high in order to place all the switching states according to their timing. Investigation to explore the possibility of using PMSM machines in open end winding configuration can also be carried out.

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