A Tri-state 4-switch Bi-directional Converter for Interfacing Super-Capacitors to DC Nano-grids

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ABSTRACT

A Tri-state 4-switch Bi-directional Converter for Interfacing Super-Capacitors to DC Nano-grids

Ashutoshkumar Choubey

Supercapacitors are energy storage devices that can contribute with a fast varying current for the regulation of DC grids. However, their power electronics interface should present fast dynamic response as well, what is not exactly the case for the conventional 2-switch buck-boost bi-directional DC-DC converter operating with conventional dual-state modulation scheme. Besides, if the DC grid voltage happens to fall below the supercapacitor voltage, the anti-parallel diodes of the converter conduct and one loses control of the current injected into the DC grid. The alternative considered in this thesis is a 4-switch bi-directional DC-DC converter with an intermediate inductor, which allows the implementation of a tri-state logic that eliminates the RHP zero of the transfer function I_{out}/D, thus allowing the design of a fast acting controller. However it does not provide a solution for the earlier problem of losing control when grid voltage falls below the supercapacitor voltage. One alternative is to use the same 4-switch converter in the buck-boost mode using tri-state logic, which allows the input voltage to be lower or higher than the grid voltage while eliminating the RHP zero at the same time.

This work presents a dynamic model for the 4-switch tri-state converter operating in the boost and buck-boost mode and connected to a droop-controlled DC micro-grid. The tri-state has essentially 3 stages, wherein the Off state length is kept constant. Based on this control approach, there are 2 possible sequences, for which a thorough analysis has been done. Further, the component sizing, selection of various parameters and control loop design for a tri-state system operating with boost mode of operation for higher voltage gain requirement (supercapacitor voltage is significantly lower than DC bus voltage), and with buck-boost mode of operation for low voltage gain requirement (supercapacitor voltage is slightly lower than, equal to or higher than DC bus voltage), is discussed. The simulation result for both modes of operation is presented as well showing an improved performance when compared to the conventional dual-state scheme.

Finally, an experimental implementation of the converter is done and results for the same are provided to verify those described by theoretical analysis as well as simulation results.

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List of Acronyms and Symbols

RHP	Right Hand Pole
T.F.	Transfer Function
w.r.t.	with respect to
DC	Direct Current
SS	Steady State
T_d	Dead-time
IIR	Infinite Impulse Response
EV	Electric Vehicle
ESR	Equivalent Series Resistance
D_{on}	Duty cycle of On state when inductor stores energy from the input
D_{off}	Duty cycle of Off state when inductor transfers energy to the output
D_f	Duty cycle of Freewheeling state when inductor energy stays the same
$D_{d.t.}$	Duty cycle equivalent of the dead time
V_{mid}	The voltage at mid of the of the droop curve voltage axis
V_{dc}	The instantaneous voltage of the DC bus of the nano-grid.
V_o	Voltage across the output capacitor of 4-switch bi-directional DC-DC converter
R_d	The droop resistance of a droop curve
I_{out}	Current injected into the DC bus
C_{out}	Output capacitor of the 4-switch bi-directional DC-DC converter
L_{eq}	The equivalent inductance found by dividing actual inductance by square of Off duty cycle
f_z	Zero frequency
f_{sw}	Switching frequency
V_{meq}	Equivalent voltage source in the DC bus model

R_{eq}	Equivalent series resistance in the DC bus model
I_L	Current through the inductor in between 2 half bridges of the converter
I_{L1}	Average of the ripple component of the inductor
V_L	Voltage across the inductor
V_{in}	Input voltage of the converter
Gain	Voltage gain of the converter
$V_{inMaxBoost}$	The maximum input voltage for which converter operates in boost mode
$V_{inMinBuckBoost}$	The minimum input voltage for which converter operates in buck-boost mode
I_c	Current through the output capacitor
I_{ref}	Reference value for the injected current control loop
$R_{droopConverter}$	Droop resistance parameter of the droop characteristic of the converter
R_L	Load applied across the DC bus of the nano-grid
$V_{midConverter}$	The mid voltage value of the droop characteristic of the converter
$I_{upperLimit}$	The maximum value of the reference provided to injected current control loop
$I_{lowerLimit}$	The minimum value of the reference provided to injected current control loop
$V_{switchover}$	Input voltage at which converter switches from one mode of operation to other

The subscript “SS” denotes steady state value of a symbol

The subscript “Max” denotes maximum value of a symbol

The subscript “Min” denotes maximum value of a symbol

The subscript “RMS” denotes RMS value of a symbol

The subscript “Avg” denotes average value of a symbol

The prefix “Δ” denotes ripple component of a symbol

Chapter 1. Introduction

With the rising adverse effects of fossil fuels on the environment, there has been a shift to renewable energy resources all over the world. There has been a growing trend of using these resources locally, to reduce dependence on the main power grid, and even feeding the surplus production back to it. DC nano-grid systems are used in residences and small buildings that allow the integration of renewable energy sources such as photovoltaic (PV) and fuel cells with the existing grid. However, these sources (renewable) are highly unpredictable in terms of maximum power available at given time, and hence, quite often, various energy storage elements like batteries and supercapacitors are also added to the system to provide backup power when the power available from renewable sources is not enough. In a nano-grid, the load as well as various power sources mentioned before are connected to a common DC bus, providing a very simple system structure. Any extra load is added simply to the bus, whereas any extra source to be added is also interfaced with the same, using applicable power conditioning circuit. Most modern appliances convert the AC supply from grid into DC before driving the load, and hence, it is possible to remove the AC-DC converter stage and associated power factor correction elements and use a direct DC fed configuration utilizing the DC nano-grid. Therefore, the use of a DC distribution system will do away with the part of source and load power conversions which are known to have lower efficiency than DC to DC [5].

One aspect of developing a DC nano-grid is the control and coordination of the power delivered by each energy source, depending on the power availability as well as priority of that particular source. Generally, the methodologies used is the droop control also referred to as DC bus voltage signaling [6], which allows a number of sources to connect directly to the bus and inject a defined value of current in it, depending on their individual droop characteristics, thus not requiring any centralized control unit or extra communication infrastructure. There has also been a lot of work to decide the voltage level of DC bus to be used in such systems. In [8], a dual DC bus system was proposed, with higher voltage bus (~380V) driving high power loads, whereas a lower voltage bus (48V) being used for lighter loads. This thesis aims at developing a power converter operating with the lower DC bus, in a DC nano-grid, though it can be extended to any other voltage level of operation as well.

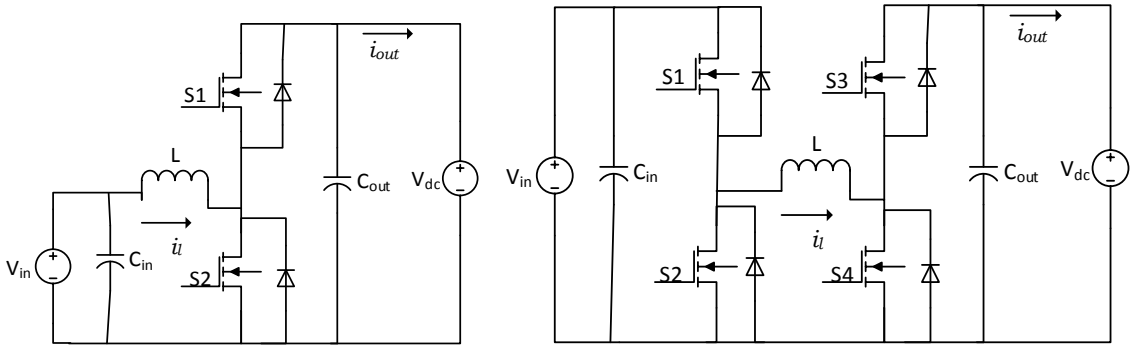
Apart from a stable system, one should be able to get voltage regulation and the grid voltage should not dip on application of high load transient. Supercapacitors can provide relatively high power in a very short time spans and hence are used often in these systems to support large load transients.

Supercapacitors are energy storage device that possess a very high capacitance value in smaller size with a very small Equivalent Series Resistance (ESR). Since they are basically capacitors, they can operate with very high current transients and hence are ideal for providing a high surge of power in a very small time span. This work aims at developing a power converter to interface these devices to an existing DC nano-grid structure. One of the considerations is that the supercapacitor has to be charged, before it can be used for transient support, necessitating a power converter which can allow power flow in both the directions, i.e. from DC bus to the supercapacitor and vice-versa. Moreover, the power converter should be able to control the power flow from supercapacitor to the DC bus, irrespective of the DC bus going below the supercapacitor voltage, a possible situation in case of a high load transient, when grid voltage may dip to a voltage lower than the fully charged supercapacitor. In order to fulfill the 2 constraints mentioned above, a 4-switch bi-directional buck boost converter topology has to be used, which will usually operate in boost mode when supercapacitor voltage is much lower than DC bus and in the buck-boost mode when it is of comparable magnitude. Further, to utilize the capability of supercapacitor in supporting transients, the speed of response of the converter should be quite high as well, something which is not possible with the conventional converter, and is achieved in this work by using a tri-state switching scheme with the same 4-switch bi-directional buck boost topology.

1.1 Problem statement and proposed solution

In order to utilize the full potential of supercapacitors, it is customary to use a power converter which should have a fast transient response as well. The conventional converters used for this purpose are half-bridge buck-boost converter as shown in the Figure 1-1(a)**.** However, this converter loses control when the DC bus voltage goes below that of the supercapacitor. An alternate topology is the 4-switch bi-directional converter (Figure 1-1(b)) operating in boost mode when supercapacitor voltage is smaller than that of the DC bus and buck mode if it is larger. From here on, this is the topology that will be considered in this study.

The transfer function of a conventional (dual-state) boost converter presents a Right Half Plane (RHP) zero in its transfer function, a phenomena which forces the designer to reduce the control loop bandwidth of the system in order to achieve stability. Generally the crossover frequency of the control loop is kept below this zero frequency, which implies lower system bandwidth and hence slower response for the converter. An alternate control scheme is the use of cascaded control, in which an inner current loop is used to control the inductor current while the output voltage/current is controlled by an outer loop. This removes the RHP zero problem, but due to the cascaded structure, the final system bandwidth is that of the outer loop, which by principle, has to be much smaller than the inner loop bandwidth (10-20% of inner loop bandwidth). This again, limits the speed of response and makes the system slower.



(a) (b)

Figure 1-1:The converters used for interfacing supercapacitor with DC nano-grid (a) Half-Bridge buck-boost converter (b) 4 switch bi-directional buck-boost converter

As a solution to this problem, a tri-state uni-directional boost converter was proposed in [2], using 2 switches and 2 diodes with an extra freewheeling state in the switching scheme apart from the conventional on and off state for the inductor. In the freewheeling state, the inductor is short circuited, to ensure that the energy stored neither increases nor decreases and stays constant. This region essentially acts like a buffer between the on time and the off time, and whenever there is a need to increase power transfer, the on-time is increased by sacrificing this region, resulting in a constant off-time and absence of RHP Zero. It allows this converter to be controlled by a single loop control structure with a high bandwidth. In [2], the focus was on driving a resistive load with improved transient response. In this thesis, it is extended to the interfacing of a supercapacitor with a DC bus in a nano-grid and the topology used is a 4-switch bi-directional topology. Moreover, the tri-state operation is extended to the

buck-boost mode as well, this being the operating mode when the supercapacitor voltage is higher than or near the grid voltage. There are 2 possible switching scheme implementations for both the modes, which are studied and a method of selecting one over other to get least switch current for a given output power, is presented as well. The primary goal in this system is to control the output current injected in to the bus, followed by a droop control curve to decide the reference for the output current control loop based on the grid voltage. The control structure is designed in such a way that when the input voltage goes above a certain percentage of the output voltage, the mode of operation changes from boost to buck-boost, and the switching scheme changes accordingly, to ensure that one does not lose the control of the converter.

The objectives of this work in a nutshell, are as follows:

- Interface supercapacitor to a DC nano-grid irrespective of whether its voltage is lower than, equal to or higher than the D.C. bus.
- Ensure bi-directional power flow, so that the supercapacitor can be both charged and discharged.
- Achieve high speed of response showed in terms of rise time/settling time of injected current transient response.
- Implement a droop characteristic curve working as an outer loop, to provide reference for the inner injected current loop. This being customary for interface of any device with a DC bus in a DC Grid structure.

The simulation of this system is done in PSIM (*version 10.0*) and results are presented here. Further, for validation of the simulation results, an experimental prototype is developed as well and the results for the same are also presented.

1.2 Scope and contribution of thesis

This thesis essentially presents the design of a bi-directional DC-DC power converter operating in boost and buck-boost mode with a high control loop bandwidth and consequently a faster transient response.

The main contributions of this thesis are as follows

1. Derivation of a model for the DC bus considering all the sources operating in droop control, with their priorities decided by their droop characteristics itself.

2. Implementation of tri-state boost switching scheme on a 4-switch bi-directional topology, interfaced with a DC nano-grid, allowing bi-directional power flow and a faster speed of response compared to a conventional dual-state boost operation.
3. Extension of the tri-state switching scheme from boost to buck-boost mode of operation, so that one does not lose the control of the converter even if the supercapacitor voltage becomes higher than the grid voltage at any point of time.
4. Analysis of the 2 possible switching schemes for both modes of operation, comparison of both based on the switch currents, and a way of selecting one over the other to minimize power loss.
5. Small signal analysis, and a dual mode control loop design of the converter so that it can operate in both boost and buck-boost mode.
6. Further the simulation results and their validation using experimental implementation.

1.3 Thesis outline

The structure of this thesis is as follows.

In Chapter 2, a DC nano-grid model is presented, which is used later for the derivation of the plant equation, followed by an analysis of different modes of operation which are used conventionally for this application. Generally, a dual-state (ON/OFF) boost mode of operation using a single output voltage controller or a cascaded control structure is used; when the supercapacitor voltage is lower than the grid voltage. Conversely, when it is higher than the grid voltage, a buck or a buck-boost mode must be used. However these control strategies have certain drawbacks which are also outlined.

Then, the detailed analysis of the proposed tri-state converter is given in Chapter 3. The tri-state switching scheme is analyzed for both boost and buck-boost mode of operation, as well as a tri-state buck operation is presented, though it is not used in the system. Further, both modes of operation have 2 possible switching schemes, an analysis for the same is done and how one should select between the 2, based on direction of power flow in order to minimize losses, is also given.

In Chapter 4, a detailed methodology for designing the proposed converter is presented. For that, the sizing of different components for both modes of operation is derived. Further, the component sizing for a case example as well as the design of the control loop is presented as well.

Based on all the analysis, the simulation of the system is done and the same is presented in Chapter 5.

Further, to validate the simulation results, a prototype hardware is implemented and results obtained from the same are presented in Chapter 6.

Chapter 7 summarizes the work presented in this thesis and derives a conclusion based on the results.

Chapter 2 Literature review

2.1 DC bus modeling

Since the application targeted here is the interface of super-capacitors with DC nano-grids, it is essential to find a model for the DC grid before one can derive the plant transfer function of the converter. In a DC nano-grid, there can be a number of power sources and storage units providing or absorbing power and also a number of loads which are only absorbing power from the bus. For this analysis, the loads are considered to be resistive, whereas the power sources and storage units are assumed to be working with a DC voltage signaling strategy. The basic block diagram of a DC nano-grid structure is shown in Figure 2-1(a).

For the power sources operating with droop control, there will be 2 modes of operation. 1st is when it has reached its positive or negative current limit and is simply injecting a particular value of current inside the bus, thus can be modeled as a constant current source, this can be termed as *Saturation mode*. 2nd is when it is injecting a particular amount of current based on the DC bus value and the droop curve, the same can be modeled as a voltage source with a series resistance. This mode of operation can be termed as *Active mode*. This is illustrated further in Figure 2-1(b).

In the active region, the equivalent internal resistance of the source is :

$$R_d = \frac{\Delta v}{\Delta I}, \text{where } \Delta v \text{ and } \Delta I \text{ are the operating voltage and current range of converter.} \quad (1)$$

The output current equation of the converter is given by:

$$I = (V_{mid} - V_{dc})/R_d, \quad (2)$$

V_{dc} is the DC bus voltage & V_{mid} is the 1.000pu voltage in the droop curve.

I is the current injected by the converter in the bus and R_d is the droop resistance

As evident, equation (2) is similar to that of 2 voltage sources connected to each other through a resistor, and hence *Active mode* of operation can be modelled as the same.

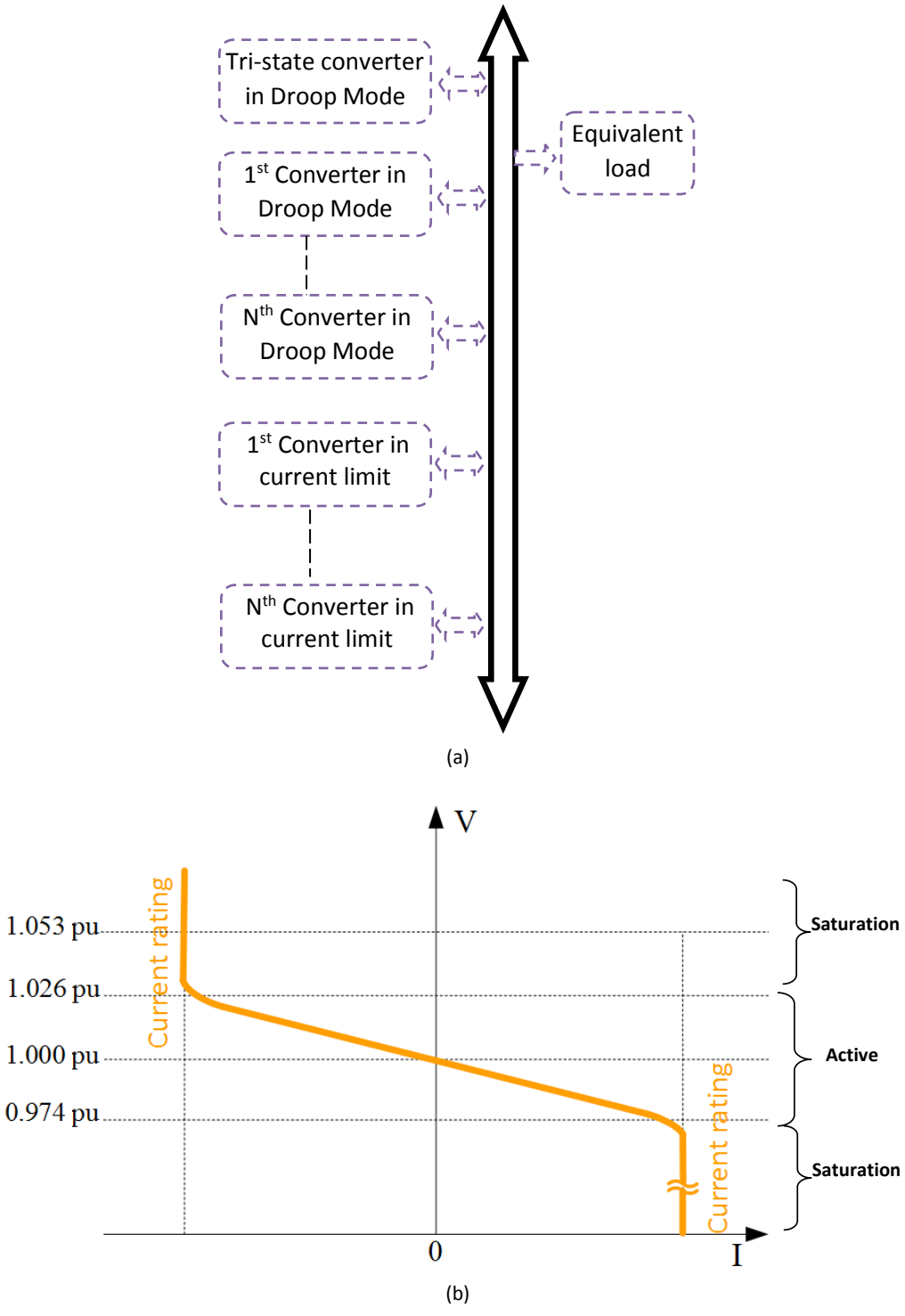


Figure 2-1(a): The DC nano-grid system structure (b) General droop characteristic of a converter

Considering a number of converters operating in parallel, one can model every converter operating in active mode as a voltage source in series with a resistance; their equivalent representation also being of the form of a DC source (V_{mideq}) in series with a droop resistor (R_{deq}). The source transformation steps supporting this theory are shown in Figure 2-2.

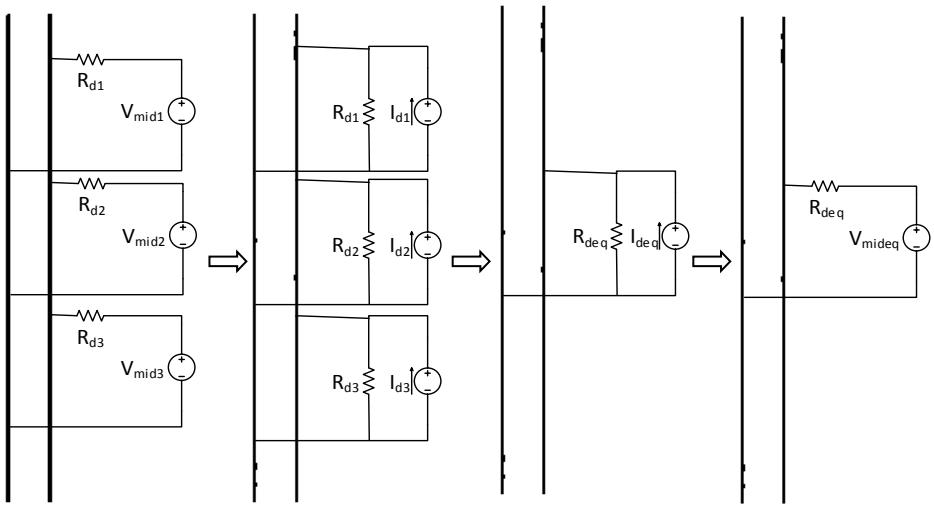
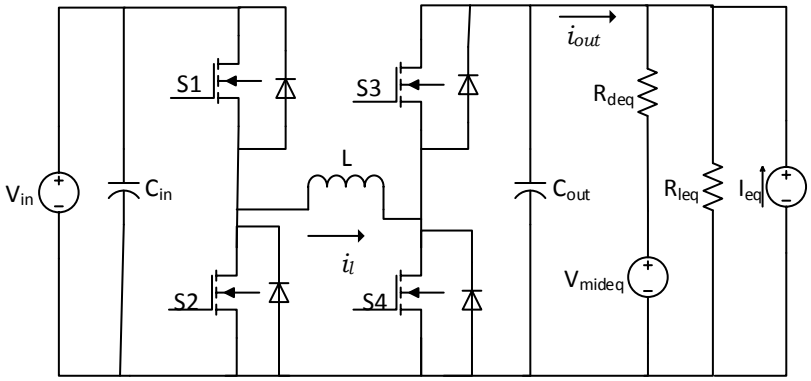


Figure 2-2: Source Transformation steps of DC bus Model Derivation

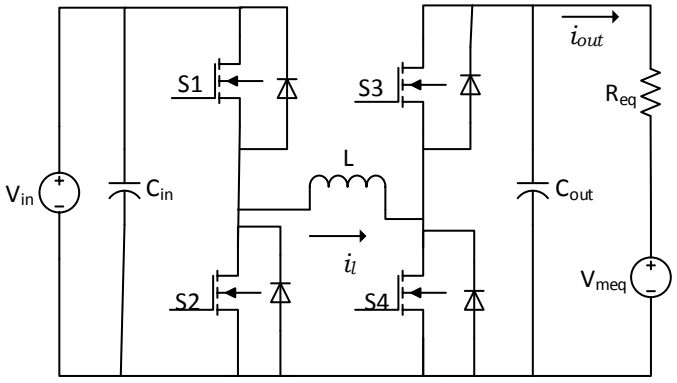
Similarly, the sources operating in their current limit region can be modeled as constant current sources, their equivalent model being a constant DC current source of magnitude equal to sum of all individual sources, whereas all resistive loads can also be modeled by an equivalent load resistance which is equal to their parallel combination. Thus, a DC bus model will consist of (i) an equivalent current source (I_{eq}), which encompasses all current sources as well as constant current loads, (ii) equivalent load resistance (R_{leq}), which is a parallel combination of all individual resistances and (iii) a series combination of equivalent droop resistance(R_{deq}) connected in series with equivalent droop mid-point voltage(V_{mideq}). This is shown in Figure 2-3(a). Further, the series combination of V_{mideq} and R_{deq} can be transformed into a resistance, in parallel with a current source, which is then added with I_{eq} to form an equivalent current source in parallel with equivalent resistance $R_{eq,}$ given by (3). This can be converted back into a voltage source and will give an equivalent source V_{meq} in series with R_{eq} as given by equation (4).

$$R_{eq} = R_{deq} || R_{leq} \; and \; I_{eq1} = I_{eq} + \frac{V_{mideq}}{R_{deq}} \quad (3)$$

$$V_{meq} = I_{eq1} R_{eq} \quad (4)$$



(a)



(b)

Figure 2-3: DC bus model (a) before and (a) after source transformation

To summarize, the model of the plant consists of the proposed converter, providing power to a series combination of a voltage source and an equivalent resistance, the goal being the control of current injected in the same. As mentioned before, the topology used for this work, is a 4-switch topology which allows bi-directional power flow, irrespective of input voltage being greater or lower than the output voltage. The final plant model is shown in Figure 2-3 (b). The value of the load resistance is an important parameter for the design of the control loop and from the above derivation of the DC bus model, the same

can be found. Since the equivalent resistance is derived by parallel combination of all the droop and source resistances, one finds that its value is relatively very small compared to conventional applications.

2.2 Analysis of conventional modes of operation

To present a background for this work, in this section, the conventional modes of operation, generally used for this application are analyzed, their implementation using the 4-switch bi-directional topology is illustrated and their plant transfer function is derived as well. It should be noted that conventional converters have only 2 states of operation, i.e. ON (duty cycle D_{on}) and OFF (duty cycle D_{off}), where voltage across inductor is positive in former and negative in latter.

2.2.1 Boost mode with output current control

The conventional boost converters are extensively used for transferring power from a low voltage bus to a high voltage bus, primarily due to their ease of implementation and low component count. In this application, this mode of operation is used when the supercapacitor voltage is lower than the DC grid bus voltage. There are 2 states in boost mode of operation, ON (duty cycle D_{on}) and OFF (duty cycle D_{off}), both of which will sum up to 1 at all times. The input to output voltage gain is given by:

$$V_o = \frac{V_{in}}{1-D_{on}}, \text{where } D_{on} \text{ is the on time.} \quad (5)$$

The implementation of this mode in the 4-switch bi-directional converter, with the clear illustration of the D_{on} and D_{off} states, for forward transfer of power, is presented in Figure 2-4.

The transfer function of output current with respect to d_{on}, derived by the small signal analysis, is

$$\frac{i_{out}}{d_{on}} = \left[\frac{\frac{V_o}{1-D_{on}} - sL_{eq}I_L}{s^2L_{eq}C_{out}+\frac{sLeq}{R_{eq}}+1}\left(\frac{1}{R_{eq}}\right)\right], \text{where } L_{eq} = \frac{L}{(1-D_{on})^2} \text{ and } V_o \text{ is Voltage across } C_{out}. \quad (6)$$

As evident from (6), the transfer function of the dual-state boost mode of operation has an RHP zero, which is inversely proportional to the output current and leads to a low frequency zero at high output current. The zero frequency is equal to:

$$F_z = \frac{V_o}{2\pi I_{out} L_{eq}} \tag{7}$$

Thus it becomes really difficult to design a controller with a high cut-off frequency. Also the value of L_{eq} changes with D_{off}, making the controller design even more complex.

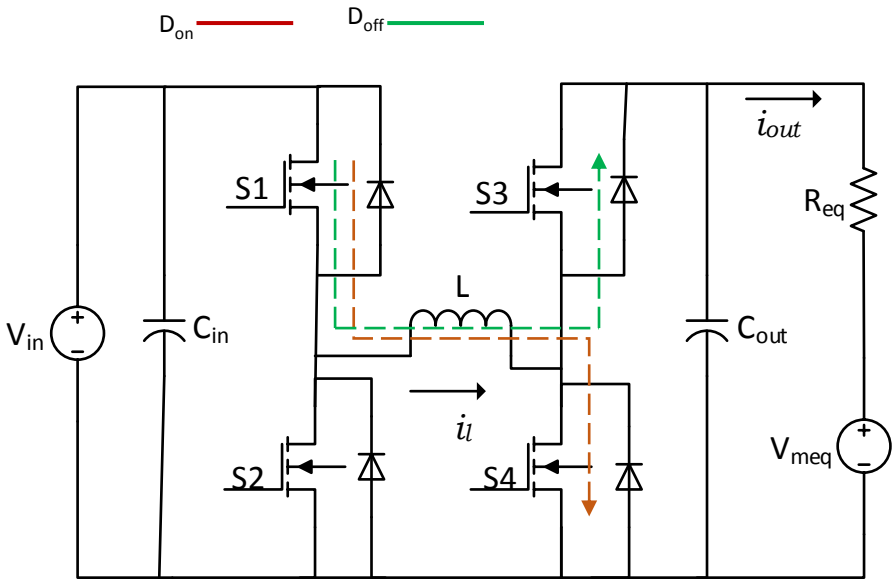


Figure 2-4: Conventional boost switching illustration for 4-switch bi-directional buck-boost topology

2.2.2 Boost mode with cascaded inner current loop control

An alternate option is to use a cascaded loop structure, consisting of an inner current loop controlling the inductor current, and an outer loop controlling the output voltage/current, where the reference for the former (inner loop) is provided by the latter (outer loop).

For inner current loop, the transfer function of inductor current w.r.t. duty cycle is given by [10]:

$$\frac{i_L}{d_{on}} = \frac{C_{out}V_o s + 2(1-D_{on})I_L}{LC_{out}s^2 + \frac{L}{R_{eq}}s + (1-D_{on})^2} \tag{8}$$

This can be further reduced to

$$\frac{i_L}{d_{on}} = \frac{V_o}{L}\left[\frac{s+\frac{2I_{out}}{V_o C_{out}}}{s^2+\frac{s}{R_{eq}C_{out}}+\frac{1}{L_{eq}C_{out}}}\right] \text{ where } L_{eq} = \frac{L}{(1-D_{on})^2} \quad (9)$$

Recall that for boost converter driving a simple resistive load, one can substitute the value of (I_{out}/V_o) by equivalent load resistance, but since in this application, the converter is injecting current in to a voltage source connected in series with a load resistance, I_{out} has to be considered as a DC constant equal to the injected current at the transient instant.

From (9) it can be seen that, for negative initial value of I_{out}, the transfer function has a positive zero again (RHPZ), though the benefit here is that the zero frequency increases with output current value and hence the controller design will not suffer with decrease in the frequency of the RHP zero for higher currents.

As mentioned before, the outer voltage control loop has to be designed as well, which provides the inductor current reference for the inner current loop. By principle of cascaded control, the outer voltage loop bandwidth has to be less than 1/10th of the inner current loop, to allow the duty cycle and the inductor current to be considered as constant DC values.

With I_L considered as constant, the resulting transfer function for the outer loop for controlling the injected current is given by,

$$\frac{i_{out}}{i_L} = \frac{1-D_{on}}{1+sR_{eq}C_{out}} \quad (10)$$

Here, $the\ pole\ frequency = \frac{1}{R_{eq}C_{out}}$, and since RC constant is small, high frequency pole is obtained.

The primary drawback of this control strategy is that the overall bandwidth is equal to that of outer voltage loop, the same being significantly smaller due to the fact that it has to have much lower bandwidth compared to that of inner current loop. This results into lower overall control bandwidth for the system.

2.2.3 Conventional buck mode of operation

The buck mode is used for transfer of power when supercapacitor voltage is higher than that of the DC bus. The implementation of this mode of operation in the current topology with clear illustration of D_{on} and D_{off} for forward transfer of power is shown in Figure 2-5.

The transfer function for this mode is given by:

$$\frac{i_{out}}{d_{on}} = V_{in}\left[\frac{1}{s^2 L_{eq} C_{out} + \frac{sL_{eq}}{R_{eq}} + 1}\right] \quad (11)$$

As evident, this is a simple 2nd order system with 2 poles and due to very low load resistance, the poles will be 2 real poles and not complex conjugates, as normally observed in conventional buck converter systems driving resistive loads.

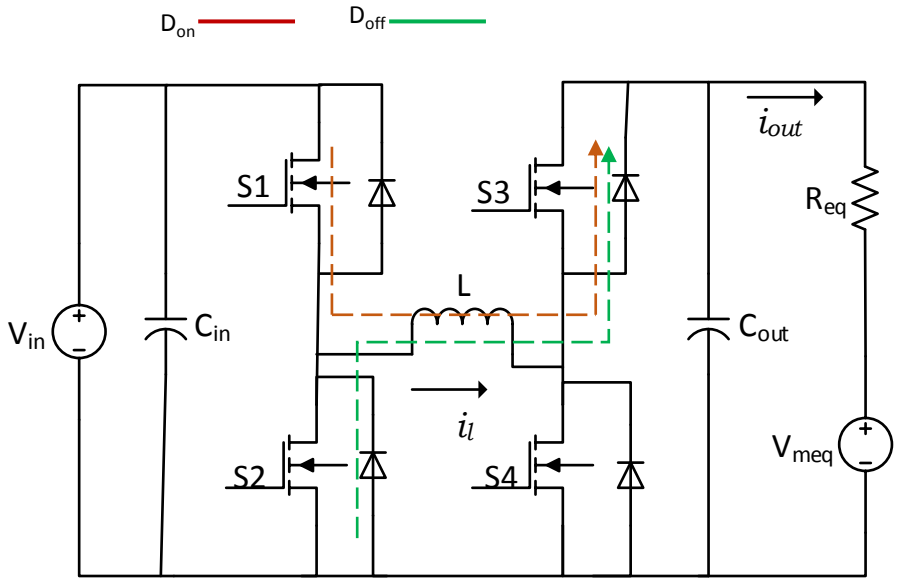


Figure 2-5: Buck mode switching illustration for 4-switch bi-directional buck-boost topology

2.2.4 Conventional buck-boost mode of operation

The buck-boost mode is used when the input power source can be higher or lower than the output power source. The implementation of this mode of operation on 4 switch bi-directional topology is illustrated in Figure 2-6.

After doing a small signal analysis, the TF of this mode is given by (12) and the steady state equation is given by (13).

$$\frac{i_{out}}{d_{on}} = \frac{[(V_{in}+V_o)-(sI_{out}L_{eq})]}{(1-D_{on})R_{eq}}\left[\frac{1}{s^2L_{eq}C_{out}+\frac{sLeq}{Req}+1}\right] \quad (12)$$

$V_o = \frac{V_{in}D_{on}}{1-D_{on}}$, where D_{on} is the on time. (13)

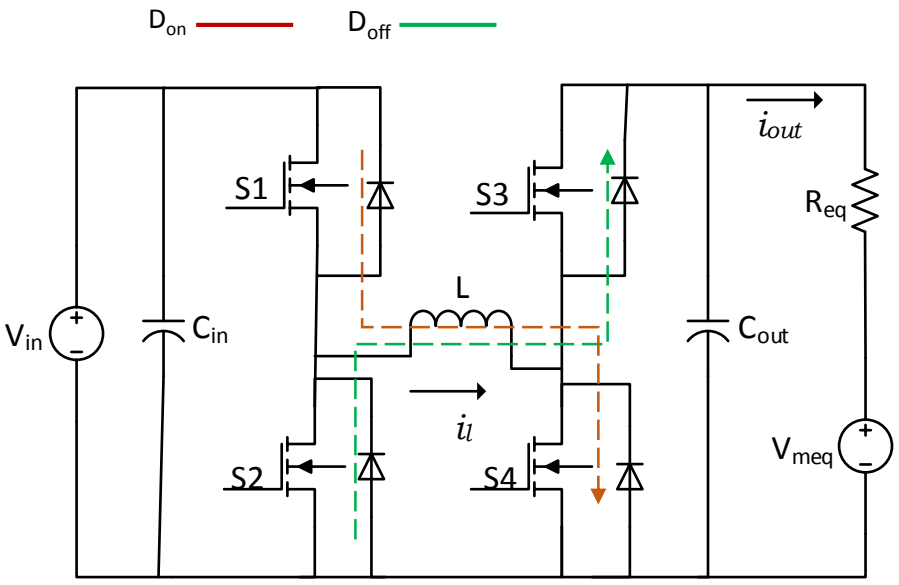


Figure 2-6: Buck-boost mode switching illustration for 4 switch bi-directional buck-boost topology

As evident from (12), an RHP zero is present in this mode, the frequency of which is given by (14). Here also, the initial value of I_{out} decides whether the zero is positive or negative and the zero frequency gets smaller with increasing output current. The value of L_{eq} also varies with D_{off}.

$$F_z = \frac{V_o}{2\pi D_{on} I_{out} L_{eq}} \quad (14)$$

Chapter 3 Proposed converter switching scheme

To overcome the disadvantages of the dual-state modes of operation presented in the previous section, a tri-state switching scheme is proposed where there are 3 states of operation instead of 2. Recall that the goal is to control the current injected in the DC bus, for both cases, supercapacitor voltage being lower as well as higher than the DC grid bus voltage; thus necessitating 2 modes of operation, boost and buck-boost. In this section, an in-depth theoretical analysis of various aspects of the proposed system is presented, which basically consists of, their implementation, small signal characteristics derivation as well as the analysis of 2 possible switching schemes for both modes of operation.

3.1 Basic tri-state converter

A basic tri-state uni-directional converter for boost applications using 2 switches and 2 diodes is shown in Figure 3-1[2].

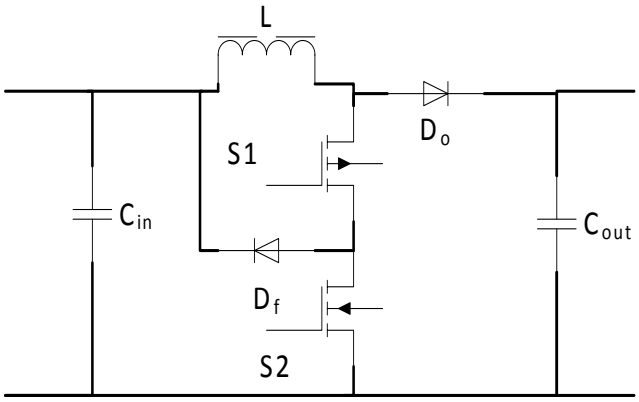


Figure 3-1: Basic Tri-state converter with 3 switches

This topology has 3 states, viz. D_{on} (On time), D_{off} (Off time) and D_f (Freewheeling period). In D_{on}, S1 and S2 are switched on and inductor stores energy supplied by the input power supply. In D_{off}, both switches are turned off, and inductor transfers energy to the output. The additional 3rd stage introduced here is D_f, when S2 is Off and only S1 is conducting, thus short circuiting the inductor, and hence there is no change in the inductor current, which means ideally, the energy stored in it, neither increases nor decreases. This 3rd freewheeling state acts as reservoir of energy. When power requirement increases, the On time is increased on expense of this freewheeling period, while keeping the Off time constant. Due to this, instead

of having 2 control variable (D_{on} and D_{off}), one has to control only the D_{on}, while D_{off} stays constant. This kind of switching methodology is known as "Constant D_{off}" switching and it was introduced in [2], and this is used for all the tri-state modes of operation proposed in this work.

3.2 Tri-state boost mode of operation

In this study, the tri-state logic is implemented on a 4-switch converter (Figure 3-2) where the MOSFETS are used instead of diodes, in form of 2 half-bridge structures, to allow bi-directional power flow i.e. from supercapacitor to DC bus and vice versa. As mentioned before, the tri-state boost mode is used when the supercapacitor has lower voltage than the DC bus, with every switching period consisting of 3 regions viz. D_{on}, D_{off} and D_f. Illustration of this switching scheme implementation for the 4-switch bi-directional topology with forward power flow i.e. I_L >0, is shown in Figure 3-2**.** In D_{on}, the switches S1 and S4 are turned ON. The other 2 switches are complementary, i.e. S2 and S3 are turned OFF, which is essential for half-bridge operation. Then in the 2nd state which is D_{off}, S1 and S3 are turned ON and S2 and S4 are turned OFF, where as in the 3rd state D_f, the lower 2 switches S2 and S4 are turned ON and S1 and S3 are turned OFF.

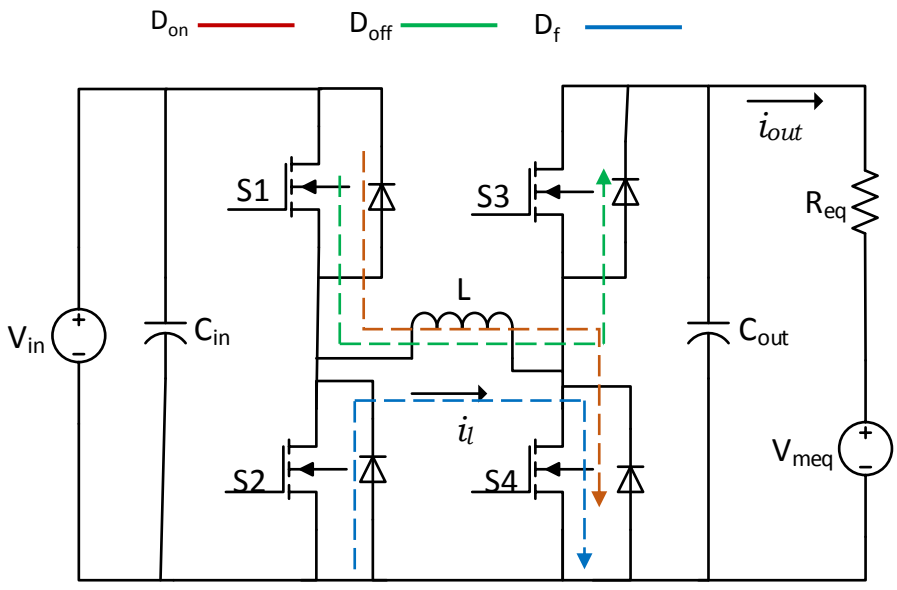


Figure 3-2: Switching scheme illustration of Tri-state boost mode of operation

3.2.1 Tri-state switching schemes

There are 2 possible switching schemes in the operation mentioned above, i.e. **(i)** when D_f is after D_{on} and D_{off} **(ii)** when D_f is in the middle of D_{on} and D_{off}. The waveforms of both switching schemes are shown in Figure 3-3, with V_{in}= 24 V, V_{out} = 48 V, L = 38.8 µH, f_{sw} = 250 kHz, D_{on} = 0.4, D_{off}= 0.4 with I_{out} = 1A.

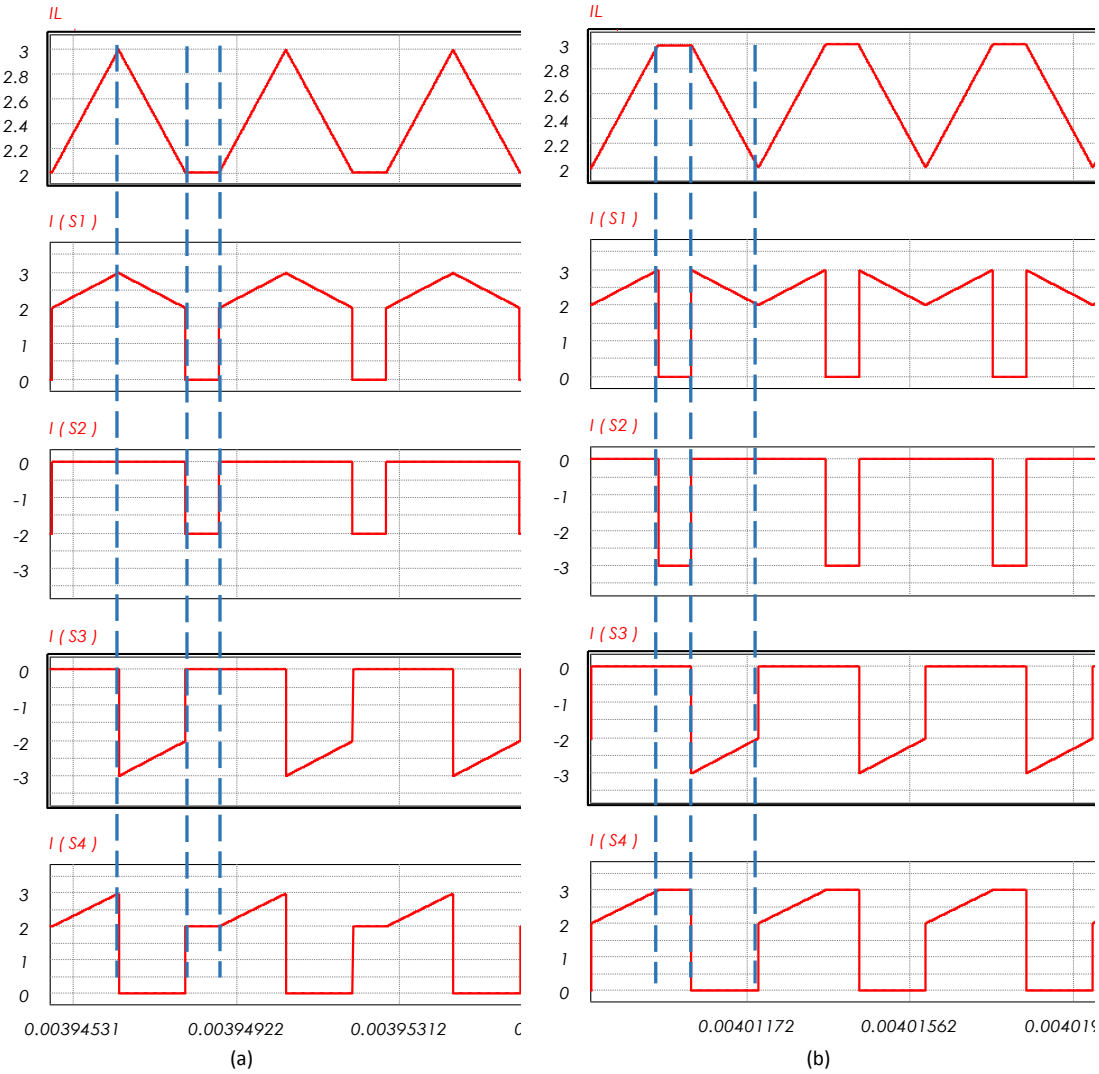


Figure 3-3: Inductor current and switch currents for the Tri-state boost mode, operating with (a) Sequence #1; (b) Sequence #2

For positive values of inductor current, one should ensure that state D_f comes either before or after the completion of both D_{on} and D_{off} states, so that one freewheels the lowest i_L; what should lead to lower losses in the inductor, compared to the case when D_f would come between D_{on} and D_{off} states.

At the same time for negative values of inductor current, i.e. when power flow is from DC bus to the supercapacitor, one should ensure that state D_f comes in between D_{on} and D_{off} states, so that one freewheels the least negative i_L; leading again to lower losses in the inductor.

To support the fact that one switching scheme is better than the other in a given direction of power flow, a mathematical analysis is presented for calculating the individual switch currents for both schemes and the results are compared.

However, first the formulas for some system variables, which will be used in the switch current equations, need to be defined.

In steady-state, the input and output voltages are related by

$$D_{on} = \left(\frac{V_o}{V_{in}} - 1\right) D_{off}, \text{ Where } D_f = 1 - \left(D_{on} + D_{off}\right) \quad (15)$$

The current ripple in the inductor is defined as

$$\Delta I_L = \frac{V_{in} D_{on}}{f_{sw} L} = \frac{V_o}{f_{sw} L}\left(\frac{D_{on} D_{off}}{D_{on} + D_{off}}\right) \quad (16)$$

The average value of the ripple current in the inductor is

$$I_{L1} = \frac{I_{max} + I_{min}}{2} = \frac{I_{out}}{D_{off}} \quad (17)$$

The average value of the current in the inductor (I_L) for sequences 1 and 2 are

$$I_{L\#1} = I_{L1} + \frac{\Delta I_L}{2}\left[\left(D_{on} + D_{off}\right) - 1\right] \quad (18)$$

$$I_{L\#2} = I_{L1} + \frac{\Delta I_L}{2}\left[1 - \left(D_{on} + D_{off}\right)\right] \quad (19)$$

For deriving expressions for the RMS current across the switches, one can see that the current through switch S1 in *Case1*, for example, can be divided into 2 standard waveforms, a pulse wave and a ripple

current which is a triangular wave (Figure 3-4). Hence, by using the standard formulas for calculating the RMS value of triangular and pulse wave, one can get the values of the RMS switch currents as below.

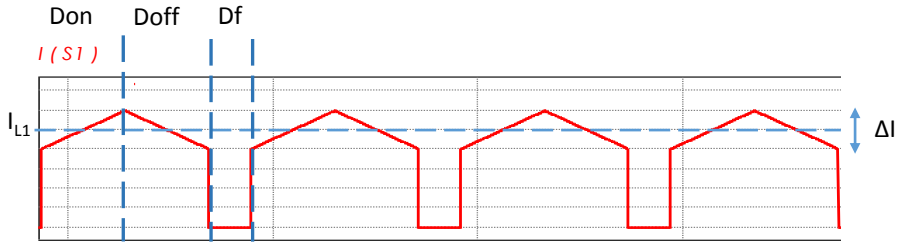


Figure 3-4: Illustration for RMS current derivation for Switch 1

For deriving the current flowing through switch 1 for *Case 1*:

$$I_{pulse\ rms} = \sqrt{{I_{pulse\ peak}}^2 (Duty\ cycle)} \quad \& \ I_{triangular\ rms} = \sqrt{\frac{(I_{peak})^2}{3}(Duty\ cycle)}$$

From Figure 3-4, $I_{s1rms} = \sqrt{{I_{pulse\ rms}}^2 + {I_{triangular\ rms}}^2}$

$$I_{s1rms} = \sqrt{{I_{L1}}^2 (D_{on} + D_{off}) + \left(\frac{\Delta I_L}{2}\right)^2 (D_{on} + D_{off}) \frac{1}{3}} = \sqrt{{I_{L1}}^2 (D_{on} + D_{off}) + \frac{{\Delta I_L}^2}{12}(D_{on} + D_{off})}$$

$$I_{s1rms} = \sqrt{({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12})(D_{on} + D_{off})} \qquad (20)$$

Similarly, the RMS current equations of other switches can be calculated as well.

$$I_{s2rms} = \left(I_{L1} - \frac{\Delta I_L}{2}\right)\sqrt{[1 - (D_{on} + D_{off})]} \qquad (21)$$

$$I_{s3rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{off}} \qquad (22)$$

$$I_{s4rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{on} + \left[\left(I_{L1} - \frac{\Delta I_L}{2}\right)^2 D_f\right]} \qquad (23)$$

For *Case 2*, as seen from Figure 3-3, the current waveforms for switch 3 is the same as that of *Case 1*, whereas the waveform for switch 1, although is not the same, but will have the same RMS and average

current as that of *Case 1*. The switch 2 and switch 4 are the only switches with different current equations, and the same are given below.

$$I_{s2rms} = \left(I_{L1} + \frac{\Delta I_L}{2}\right)\sqrt{\left[1 - \left(D_{on} + D_{off}\right)\right]} \quad (24)$$

$$I_{s4rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{on} + \left[\left(I_{L1} + \frac{\Delta I_L}{2}\right)^2 D_f\right]} \quad (25)$$

To further visualize the impact of the *scheme used*, the RMS currents of switches S2 and S4 are calculated with respect to variations in the input voltage and consequently variation in D_{on}, while considering the output voltage and output current constant. These are plotted in Figure 3-5, as a function of D_{on}. This is the control parameter which varies with variations in the input voltage to get the required voltage gain and also to regulate I_o.

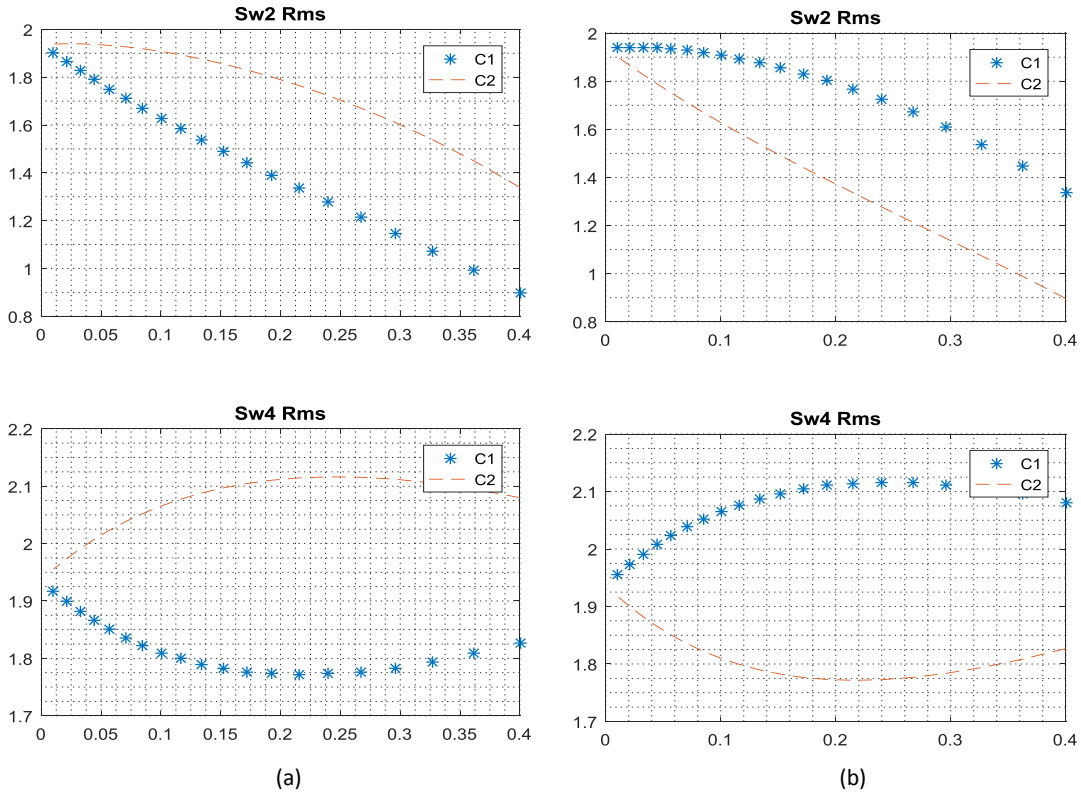


Figure 3-5: RMS values of the currents in S2 and S4 for Cases 1 and 2 of Tri-state boost mode of operation as a function of D_{on} for: (a) Forward power flow (b) Reverse power flow.

Figure 3-5(a) considers the forward (SC to DC grid) and Figure 3-5(b) considers the reverse power flow direction (DC grid to SC). The numerical values are obtained for the same parameters as used in the waveforms shown in Figure 3-3**.** From Figure 3-4(a), power flowing from the supercapacitor to the DC grid, one can see that the value of the RMS currents in S2 and S4 are lower with *Case 1*. The values obtained from the curves in Figure 3-4(a) were compared with those obtained from the simulation results with PSIM shown in Figure 3-2. For Switch S2, the RMS current for *Case 1* was found to be 0.8967, whereas for *Case 2* was found to be 1.3393 A. Likewise, for Switch S4, the values are 1.8267 and 2.0800 respectively. From the simulation, these were found to be 0.8959 and 1.34686 for Switch 2 and 1.8259 and 2.08850 for Switch 4, respectively. Thus, these are in good agreement. In general, the advantage achieved by using *Case 1* instead of *Case 2* for forward power flow increases with D_{on}, evident in terms of lower RMS switch currents for S2 and S4. Conversely, for reverse power flow, the use of *Case 2* leads to lower RMS currents in S2 and S4.

3.2.2 Selection of D_{off} value

In this work, the constant D_{off} scheme is used where the value of D_{off} is always kept constant and D_{on} varies with the variation in the required voltage gain and load conditions. Hence, the constant value of D_{off} is one of the critical parameters of the system.

For tri-state logic, one must always use all three states: D_{on}, D_{off} and D_f. Since D_{off} is made constant, a transient increase in D_{on}, to increase the voltage gain or the inductor current, yields a corresponding transient decrease in D_f. Thus regarding the maximum possible voltage gain, one should also consider a minimum free-wheeling duty cycle (D_{fMin}), and based on its value, the equation of maximum voltage gain is shown in (26). In principle, a lower value of D_{off}, while maintaining a D_{fMin}, will increase the maximum possible voltage gain, allowing the supercapacitor to operate with a lower voltage.

$$Gain_{Max} = 1 + \frac{D_{onMax}}{D_{off}} = 1 + \frac{(1-D_{off}-D_{fMin})}{D_{off}} = \frac{D_{off}+1-D_{off}-D_{fMin}}{D_{off}}$$

$$Gain_{Max} = \frac{(1-D_{fMin})}{D_{off}} \qquad (26)$$

For better visualization, the variation of the maximum possible gain w.r.t. D_{off} is plotted in Figure 3-6**,** while keeping D_{fMin} as 0.05.

Another aspect of this analysis is that the dynamic range of D_{on} for a transient condition is provided by D_f, the worst case being the case of maximum steady state voltage gain requirement, when minimum value of D_f in steady state, D_{fMinSS} (suffix SS denotes steady state) is obtained.

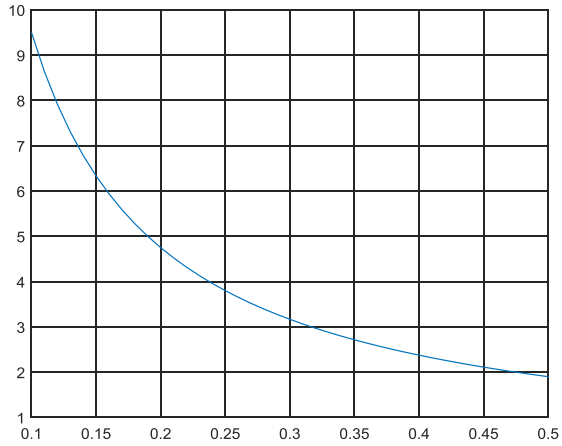


Figure 3-6: Maximum possible gain with respect to D_{off}

Therefore overall, one can have 2 values, D_{fMin} and D_{fMinSS}, where the former is decided by the maximum/ saturation level of the controller and is used to ensure that the converter operates in tri-state mode at all times, while the latter is a constraint to fulfill, based on selection of maximum input voltage of the converter and D_{off} value.

For instance, D_{fMin} can be equal to 0.025, whereas D_{fMinSS} can be decided as 0.1. In this case, the controller output will saturate at a D_{onMax} given by (1- D_{off} - D_{fMinSS}). Considering D_{off} = 0.4, this will be 0.575 (1 - 0.4 - 0.025 = 0.575). Whereas for D_{fMinSS} one finds that $Gain_{MaxSS}$ is 2.25 (26). Hence, the converter specifications will be defined such that minimum input voltage is $0.44V_o$ (1/2.25 = 0.44), implying that the supercapacitor voltage should not be allowed to go below the $0.44V_o$ value.

Viewing this from D_{off} selection point of view, one can restructure the formula in (26) to derive the relation between $Gain_{Max}$, D_{off} and D_{fMin} as in (27). In principle, the D_{fMinSS} has higher value than D_{fMin} and hence, will impose greater restriction on selection of D_{off}, hence this is the value to be considered.

$$D_{fMinSS} = 1 - Gain_{MaxSS} D_{off} \quad (27)$$

Overall, with a lower value of D_{off}, one can increase the maximum possible steady state gain, and at the same time, for a given maximum gain value, the worst case dynamic range for D_{on} (i.e. D_{fMinSS}), will be higher for lower D_{off}.

On the other hand, high value of D_{off} results into a reduction in inductor current for a given output current, the equation for the same is derived with the help of Figure 3-7(a) and presented in (28).

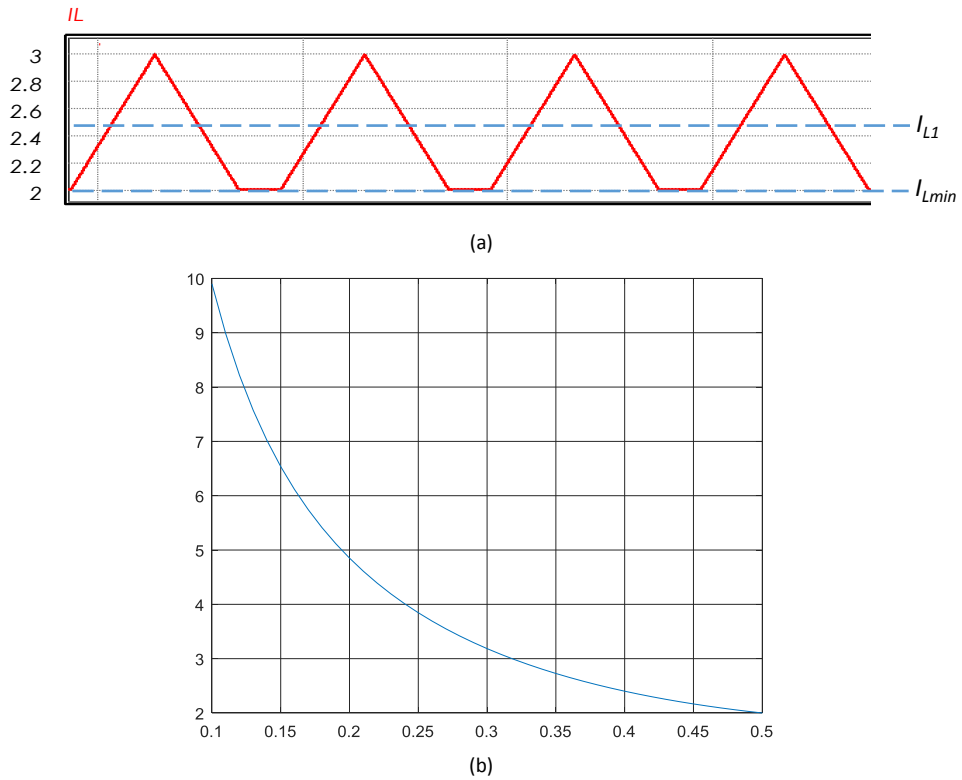


Figure 3-7: (a) Illustration of derivation of inductor current as function of D_{off} (b) Variation in inductor current with respect to variation in D_{off}

$$I_{Lavg} = (D_{on} + D_{off}) I_{L1} + I_{min} D_f \,, \quad (28)$$

$I_{L1} = \frac{I_{out}}{D_{off}}$ which is average of the ripple component in I_L.

To visualize this further, a plot of I_{Lavg} variation w.r.t to D_{off} is also shown in Figure 3-7(b), for unit output current and V_{in} = 24V, V_{out} = 48V and L= 38.8µH.

From all the above arguments, one can deduce that the best way would be to select highest D_{off} value providing the required maximum steady state gain while ensuring a reasonable D_{fMinSS}.

The application considered in this paper concerns the interface of a 48 V supercapacitor, to a DC grid rated at 48 V and as pointed out in [11], by operating a supercapacitor with a minimum voltage of half rated voltage, one can exploit 75% of its rated energy without oversizing the power converter in terms of current, for a given rated output power.

Hence a worst case minimum voltage of 24 V, should be considered for supercapacitor. It is assumed that interface of the supercapacitor (4-switch converter) should be able to generate a maximum output voltage of 52.8 V (10 % margin), to allow the control of current injection into the DC nano-grid. Using the values above with D_{fMinSS} = 0.1 in (27)**,** leads to a $D_{off} \approx$ 0.4. However as mentioned ahead, in *section 3.4*, for operation in both boost and buck-boost mode, this value has to be changed to 0.35.

3.2.3 Small signal analysis

A dynamic model for the 4-switch converter operating with tri-state logic has to be derived to design the controller. For illustration purpose the implementation of tri-state scheme is reshown in Figure 3-8. This converter has 4 but it will operate in 3 states and hence one needs to find the state space equations for these 3 states.

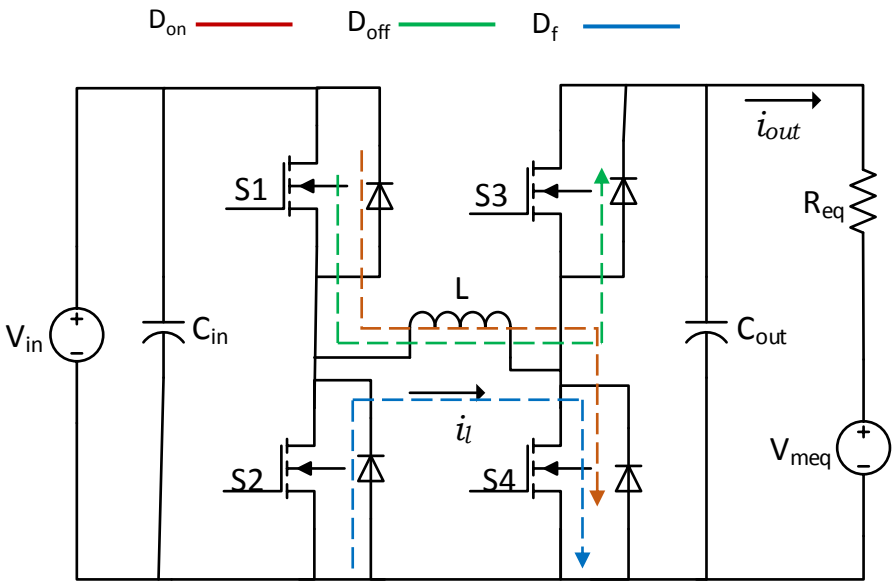


Figure 3-8: Illustration of Tri-state boost mode of operation

1)D_{on}: In this state, the switches S1 and S4 are turned ON. The other 2 switches are complementary, i.e. S2 and S3 are turned OFF, which is essential for half-bridge operation. The inductor current increases and the voltage across the inductor is V_{in}. If one considers the Inductor current (I_L) and the Output capacitor voltage (V_o) as state variables, the state equations for this state is given as:

$$\left[\frac{dI_L}{dt} = \frac{Vin}{L}\right] \quad [V_o = V_{meq} + I_{out}R_{eq}] \quad \left[C_{out}\frac{dV_o}{dt} = -I_{out}\right] \tag{29}$$

2)D_{off}: Here S1 and S3 are turned ON and S2 and S4 are turned OFF. The inductor current decreases and the voltage across the inductor is ($V_{in} - V_o$).The state space equation for this state can be given as

$$\left[\frac{dI_L}{dt} = \frac{V_{in}-V_o}{L}\right] \quad [V_o = V_{meq} + I_{out}R_{eq}\ ] \quad \left[C_{out}\frac{dV_o}{dt} = I_L - I_{out}\right] \tag{30}$$

3)D_f: Finally the 3rd stage is the freewheeling period D_f, for which S2 and S4 are turned ON, so the inductor is short circuited and hence the inductor current remains constant. The state space equation will be,

$$\left[\frac{dI_L}{dt} = 0\ \right] \quad \left[C_{out}\frac{dV_o}{dt} = -I_{out}\right] \quad [V_o = V_{meq} + I_{out}R_{eq}] \tag{31}$$

In tri-state boost mode of operation, there are 2 duty cycles to be controlled. The third one will be calculated directly from the two, due the fact that all three duty cycles will always sum up to 1. However,

the value of D_{off} is constant making D_{on} the only control variable. After applying small perturbations and ignoring the resultant non-linear and DC terms, one can represent this mode of operation with the block diagram shown in Figure 3-9.

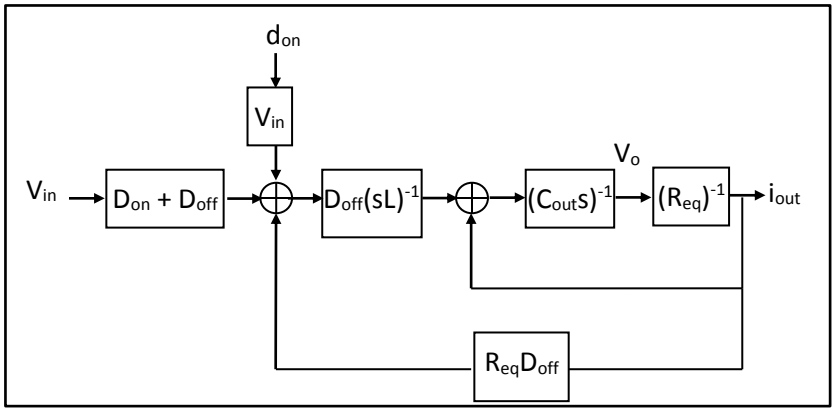


Figure 3-9: Plant Transfer function Block Diagram for Tri-state boost mode of operation

For the design of the control loop the transfer function of i_o with respect to d_{on} is given by:

$$\frac{i_{out}}{d_{on}} = \frac{V_{in}}{(D_{off}R_{eq}L_{eq}C_{out})}\left[\frac{1}{s^2+\frac{s}{R_{eq}C_{out}}+\frac{1}{L_{eq}C_{out}}}\right] \text{where } L_{eq} = \frac{L}{D_{off}^2} \quad (32)$$

The steady state output voltage equation is given by

$$V_o = \left[1+\frac{D_{on}}{D_{off}}\right]V_{in} \quad (33)$$

As evident here, there is no RHP zero present in this equation which was present in the dual-state boost mode of operation derived before (*section 2.2.1*).

3.2.4 Comparison of inductor for dual-state and tri-state mode of operation

For the inductor design, it should be noted that this is a bi-directional current control application and hence, there is no discontinuous mode of operation. If the inductor is too small, the inductor current ripple will be high, however the average value of current, whether positive or negative will still be maintained. Hence, the design of inductor in this application is based on the ripple current required,

making it essential to derive the relation between inductance and the resulting ripple current as well as to find the change in the inductor due to selection of tri-state mode instead of the conventional dual-state boost mode.

For dual-state boost mode of operation

$\frac{\Delta I_L}{2} = \frac{V_{in}D}{2L_c f_{sw}}$, where L_c is used to denote inductor for dual-state boost. (34)

For tri-state boost mode this changes to

$\frac{\Delta I_L}{2} = \frac{V_{in}D_{on}}{2L_t f_{sw}}$, where L_c is used to denote inductor for tri-state boost. (35)

Now for the same input & output conditions, the value of the required voltage gain will be same for both the cases, however the value of D and D_{on} would be different. Equating the 2 gains, one can derive a relation between the duty cycles for dual-state and tri-state modes as shown below.

$Gain = \frac{D_{on}+D_{off}}{D_{off}}$, for tri-state where as $Gain = \frac{1}{1-D}$ for dual-state boost

$$\frac{1}{1-D} = \frac{D_{on}+D_{off}}{D_{off}} \quad => \frac{D}{D_{on}} = \frac{1}{1-D_f} \tag{36}$$

Applying (36) in (35) gives a relation between the inductor needed for tri-state mode and dual-state boost mode for the same input voltage, switching frequency, and inductor ripple (37).

$$L_t = L_c\left(\frac{D_{on}}{D}\right) \quad => L_t = L_c(1 - D_f) \tag{37}$$

Since the value of D_f is always less than 1, hence the required inductor for tri-state mode is lower compared to that of dual-state boost mode, depending on the lowest value possible of freewheeling time D_f. However, in practice the D_{fMin} value is very small; consequently, the inductor values are very close.

3.3 Tri-state buck-boost mode of operation

3.3.1 Boost mode limitation and extension of tri-state to buck boost mode

The tri-state boost mode loses control when the input voltage becomes higher than or equal to the DC bus voltage, as the value of D_{on} becomes really low. The main factors which decides the lowest possible value of D_{on} (D_{onMin}) at all times is the dead time (T_d) used in the 2 half-bridges for avoiding shoot-through. When On time goes below the dead time, the switch turns off permanently and one loses control. Moreover, for proper transient response one needs to maintain some dynamic range of operation over the steady state value. Taking all this into consideration, one can define 2 quantities, the lowest possible value of D_{on} to avoid losing control, denoted as D_{onMin} and the minimum steady state value of D_{on} given as $D_{onMinSS}$. The former will decide the lower saturation limit of the control output whereas latter will be a constraint to fulfill, based on the maximum steady state gain requirement, which in turn depends on selection of maximum input voltage of the converter. Recall that at maximum input voltage one will get lowest value of D_{on} in steady state. Considering a $D_{onMinSS}$ of 0.1, (same as D_{fMinSS} for symmetrical worst case dynamic range on upper and lower limit of input voltage, see *section 3.2.2*), the minimum steady state gain is defined as in (38). Consequently, maximum input voltage can be defined as in (39).

$$Gain_{MinSS} = 1 + \frac{D_{onMinSS}}{D_{off}} \tag{38}$$

$$V_{inMax} = \frac{V_o}{\left(1+\frac{D_{onMinSS}}{D_{off}}\right)} \tag{39}$$

Based on selection of D_{off} = 0.4, the maximum input voltage will be equal to $0.8V_o$.

From above discussion one can conclude that the boost mode of operation can be used only for the input voltage range of $0.5V_o$ to $0.8V_o$ given that D_{off} is 0.4. This situation will be further aggravated when one considers the +/- 10 % worst case margin over the nominal output voltage.

One solution for this is to change the mode of operation from tri-state boost to buck-boost mode for higher input voltage, more details of which will be provide in the following sections.

3.3.2 Implementation and small signal analysis of tri-state buck-boost mode

The switching period of tri-state, as discussed before, is divided into 3 regions viz. D_{on}, D_{off} and D_f. For buck-boost mode, the direction of current flow for 3 time periods for forward power flow is shown in figure below.

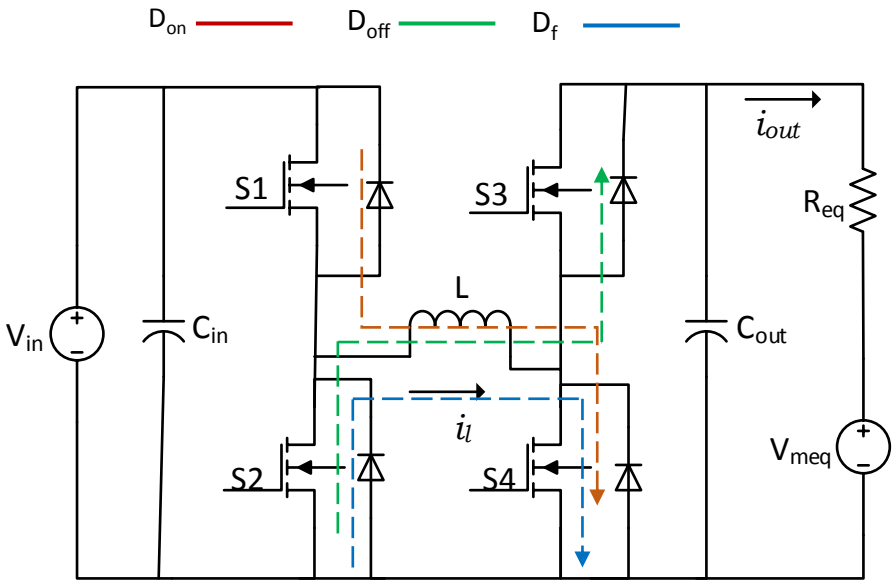


Figure 3-10: Illustration of Tri-state buck-boost mode of operation

1)D_{on}: In this state, the Switches S1 and S4 are turned ON. The other 2 switches are complementary, i.e. S2 and S3 are turned OFF, which is essential for half-bridge operation. The inductor current increases and the voltage across the inductor is V_{in}. If one considers the Inductor current (I_L) and the Output capacitor voltage (V_o) as state variables, the state equations for this state are given as:

$$\left[\frac{dI_L}{dt} = \frac{Vin}{L}\right] \quad \left[V_o = V_{meq} + I_{out}R_{eq}\right] \quad \left[C_{out}\frac{dV_o}{dt} = -I_{out}\right] \tag{40}$$

2)D_{off}: Here S3 and S2 are turned ON. The inductor current decreases and the voltage across the inductor is ($-V_o$). The state space equations for this state can be given as

$$\left[\frac{dI_L}{dt} = \frac{-V_o}{L}\right] \quad \left[V_o = V_{meq} + I_{out}R_{eq}\right] \quad \left[C_{out}\frac{dV_o}{dt} = I_L - I_{out}\right] \tag{41}$$

3)D_f: Finally the 3rd stage is freewheeling period, for which S2 and S4 are turned ON, so the inductor is short circuited and hence the inductor current remains constant. The state space equations will be,

$$\left[\frac{dI_L}{dt} = 0\right] \quad \left[C_{out}\frac{dV_o}{dt} = -I_{out}\right] \quad \left[V_o = V_{meq} + I_{out}R_{eq}\right] \tag{42}$$

So on average:

$$\left[\frac{dI_l}{dt} = \frac{-Vo}{L}D_{off} + \frac{V_{in}}{L}D_{on}\right], \left[V_o = V_{meq} + I_{out}R_{eq}\right] \text{ And } \left[C_{out}\frac{dV_o}{dt} = D_{off}I_L - I_{out}\right] \tag{43}$$

After applying small perturbations and ignoring the resultant non-linear and DC terms, one can represent this mode of operation with the block diagram shown below.

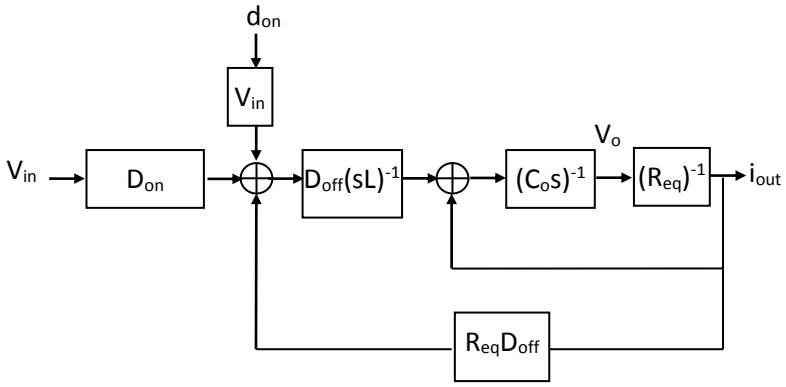


Figure 3-11: Plant transfer function Block Diagram for Tri-state buck-boost mode of operation

This is the same as the tri-state boost mode (Figure 3-9). Only difference is in the transfer function of i_{out} with respect to V_{in}, where the DC gain is D_{on} instead of $D_{on} + D_{off}$ in case of tri-state. But since the actual transfer function to be used is of i_{out} with d_{on}, the plant function for both modes of operation remains the same.

For the design of control loop, the transfer function of i_{out} with respect to d_{on} is given by

$$\frac{i_{out}}{d_{on}} = \frac{V_{in}}{(D_{off}R_{eq}L_{eq}C_{out})}\left[\frac{1}{s^2 + \frac{s}{R_{eq}C} + \frac{1}{L_{eq}C}}\right] where, L_{eq} = \frac{L}{D_{off}^2} \tag{44}$$

3.3.3 Two possible switching sequences

Similar to tri-state boost mode, the tri-state buck-boost mode of operation also has 2 possible switching sequences depending on whether D_f is the 3rd stage or the 2nd stage, and based on the sequence, the waveform of inductor as well as the switch currents would change. In Figure 3-12, the waveforms for the 2 cases is presented, with other system parameters being V_o = 48V, V_{in} = 40 V, I_{out} = 1A, L = 38.8µH, D_{off} = 0.35, f_{sw} = 250 kHz.

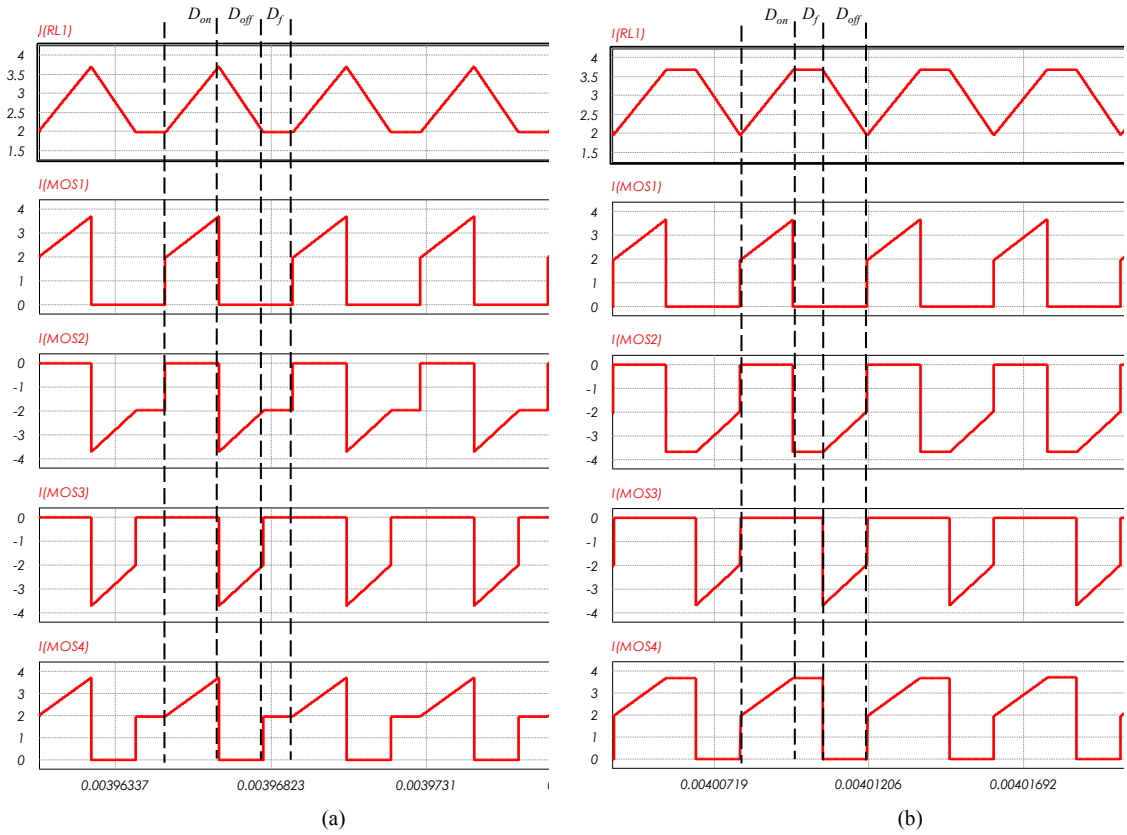


Figure 3-12: Inductor current and switch currents for the tri-state boost mode of operation with (a) Sequence #1 (b) Sequence #2

For positive inductor current, the 1st switching sequence allows the freewheeling of lower $|i_L|$, which implies lower inductor as well as switch currents and consequently lower power loss. Conversely, for negative inductor current, the 2nd switching sequence allows freewheeling of the lowest $|i_L|$ and hence lower losses.

To verify this intuitive speculation, a mathematical analysis is done and expression for RMS currents of all the switches are derived for both the cases.

In the proposed buck-boost tri-state mode of operation, D_{off} is considered as constant, and since the 3 states always sum up to 1, the only control variable is D_{on}, with D_f being calculated from the equation below:

$$D_f = 1 - \left(D_{on} + D_{off}\right) \tag{45}$$

The steady state equation for this mode of operation is given by:

$$D_{on} = \left(\frac{V_o}{V_{in}}\right) D_{off} \tag{46}$$

The ripple in the inductor current is given by

$$\Delta I_L = \frac{(V_o)D_{off}}{L f_{sw}} \tag{47}$$

The average value of the ripple in the inductor current is defined as

$$I_{L1} = \frac{I_{max}+I_{min}}{2} = \frac{I_{out}}{D_{off}} \tag{48}$$

The average value of the current in the inductor (I_L) for cases 1 and 2 are

$$I_{L\#1} = I_{L1} + \frac{\Delta I_L}{2}\left[\left(D_{on} + D_{off}\right) - 1\right] \tag{49}$$

$$I_{L\#2} = I_{L1} + \frac{\Delta I_L}{2}\left[1 - \left(D_{on} + D_{off}\right)\right] \tag{50}$$

For the derivation of switch currents, in switch 1 for instance, one can see that the current waveform can be interpreted as a combination of 2 standard waveforms, a DC pulse wave and a triangular wave due to the ripple. The average value of the pulse waveform is equal to I_{L1} while the triangular component has a peak to peak of ΔI_L. Hence, by using the standard formula for calculating the RMS of these waveforms,

the RMS current for switch 1 can be calculated. Similarly the RMS current equations for all the switches are calculated for both cases.

For *Case 1*:

$$I_{s1rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{on}} \quad (51)$$

$$I_{s2rms} = \sqrt{\left({I_{L1}}^2 + \frac{\Delta I_L^2}{12}\right) D_{off} + \left[\left(I_{L1} - \frac{\Delta I_L}{2}\right)^2 D_f\right]} \quad (52)$$

$$I_{s3rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{off}} \quad (53)$$

$$I_{s4rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{on} + \left[\left(I_{L1} - \frac{\Delta I_L}{2}\right)^2 D_f\right]} \quad (54)$$

For *Case 2*, the waveform of switch 1 and 3 are same as that of *Case 1*, thus there RMS current equation are same as well. For switch 3 and switch 4, the RMS currents are different and are given by the equations below.

$$I_{s2rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{off} + \left[\left(I_{L1} + \frac{\Delta I_L}{2}\right)^2 D_f\right]} \quad (55)$$

$$I_{s4rms} = \sqrt{\left({I_{L1}}^2 + \frac{{\Delta I_L}^2}{12}\right) D_{on} + \left[\left(I_{L1} + \frac{\Delta I_L}{2}\right)^2 D_f\right]} \quad (56)$$

For further visualization, the RMS currents of switch 2 and switch 4 are calculated using these equations and plotted in Figure 3-13, for both the sequences, with respect to variation in the input voltage, and hence D_{on}, while keeping the output voltage constant and output current equal to 1A. This is the parameter which will actually vary in this application, based on the state of charge of supercapacitor as well as to regulate the output current. Figure 3-13(a) shows the RMS currents for forward power flow, whereas Figure 3-13(b) shows for reverse power flow. The switch currents in Figure 3-12, obtained with simulation, are one of the points in the Figure 3-14(a) plots, and the 2 values are compared with each other.

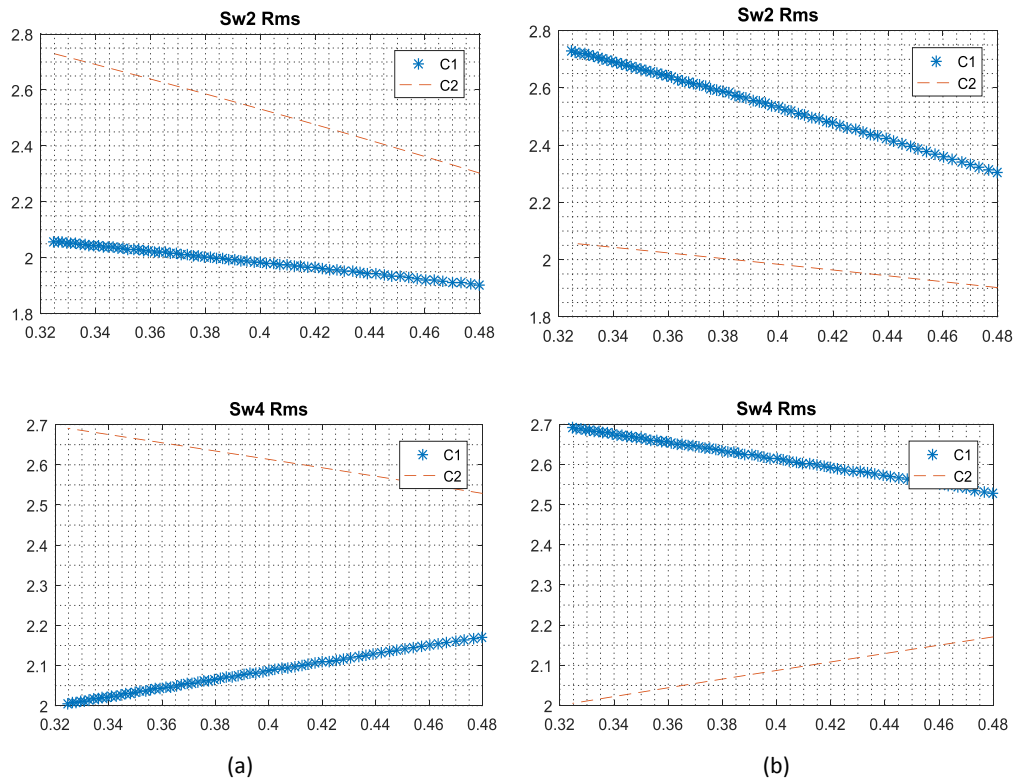


Figure 3-13: RMS values of the currents in S2 and S4 for Cases 1 and 2 for buck-boost mode, as a function of D_{on} for: (a) Forward power flow; (b) Reverse power flow.

From simulation results, the RMS current of switch 2 was found to be 1.955A and 2.48A for *Case 1* and *Case 2* respectively, whereas that of switch 4 was found to be 2.107A and 2.594A. The results of the equation were found to be 1.9638A and 2.4765A for switch 2 and 2.1084A and 2.5926A for switch 4. The values are in close agreement with each other. It is evident that for forward power flow, *Case 1* gives lower switch currents whereas for reverse power flow, same is achieved by *Case 2*. Hence the current for C*ase 1* is about 20% less than *Case 2*, giving significant advantage in terms of power loss. Moreover, the advantage of using one sequence over the other, becomes more significant with decreasing value of D_{on}.

3.3.4 D_{off} selection and selection of boost or buck-boost based on gain requirement

In the tri-state implementation, the D_{off}, D_f and D_{on} are 3 states, wherein D_{off} is kept constant, thus D_{on} is the only control variable. The value of D_{off} is one of the important parameters which has to be selected.

Similar to the boost mode, in the buck-boost mode also, the selection of D_{off} is associated with a tradeoff between maximum possible gain while keeping a D_{fMin}, and the inductor current. The relation between D_{off} and the average inductor current is given by

$$I_{Lavg} = I_{L1} - \frac{\Delta I_L}{2} D_f \Rightarrow I_{L1} - \frac{V_o D_{off}}{2Lf_{sw}} D_f \Rightarrow I_{L1} - \frac{V_o D_{off}}{2Lf_{sw}} (1 - D_{on} - D_{off}) \quad (57)$$

Since, it is not easy to interpret the effect of D_{off} on the average inductor current value, the same is calculated for different values of D_{off} and presented in Figure 3-14 with other parameters being V_o = 48V, V_{in} = 40V, L = 38.8µH, C = 76.8µF and I_{out} = 1 A. It can be seen that the average inductor current decreases with higher D_{off}. Also, the average inductor current in *case 1* of Figure 3-12 in previous section can be compared with that of the corresponding point (D_{off} = 0.35) point in the plot in Figure 3-14, and one can see that the average inductor current from the simulation is equal to 2.643 whereas that calculated in plot is equal to 2.65, both values being in close agreement with each other.

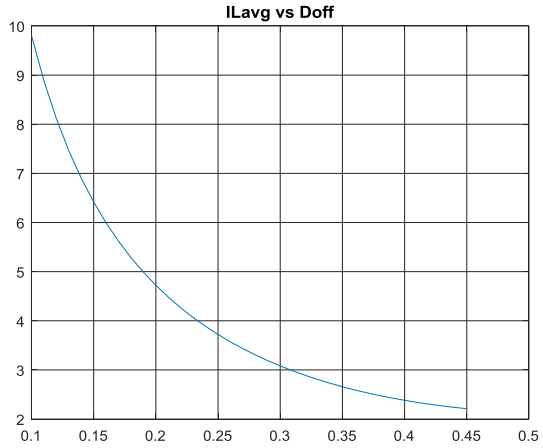


Figure 3-14: Average inductor current variation with respect to D_{off} for tri-state buck-boost mode of operation

For tri-state operation, it is essential to have 3 stages of operation, where an increase in power demand increases D_{on} at the expense of D_f, thus D_f can be seen as dynamic range of D_{on} in case of a transient. Hence, it is imperative to operate with a minimum value of D_f (D_{fMinSS}) in the steady state, obtained at lowest possible input voltage (implying maximum D_{on}) and effectively being the worst case dynamic range for D_{on} in case of a transient. Based on its value, one will have a maximum value of D_{on} ($D_{onMaxSS}$), and

consecutively a maximum value of steady state gain possible, given by (58). As evident, it decreases with higher D_{off}, which effectively limits the range of supercapacitor voltage that can be interfaced with the converter.

From above discussion, one can conclude that the best way to decide the value of D_{off} is to select the highest value so as to ensure lower inductor current, while achieving the required maximum gain and a reasonable value of D_{fMinSS} at the same time.

$$Gain_{MaxSS} = \frac{D_{onMaxSS}}{D_{off}} = \frac{(1-D_{off}-D_{fMinSS})}{D_{off}} = \frac{1-D_{fMinSS}}{D_{off}} - 1 \quad (58)$$

Also,

$$Gain_{MaxSS} = \frac{V_{oMax}}{V_{inMin}} \quad (59)$$

Using the above 2 equations, the value of D_{off} can be calculated as,

$$D_{off} = \frac{1-D_{fMin}SS}{Gain_{MaxSS}+1} \quad (60)$$

Recall that in this application the minimum input voltage range is equal to half of the rated output voltage. If one considers operating with buck-boost mode of operation for whole input range of $V_o/2$ to V_o, maximum output voltage as 110% of the nominal value, and D_{fMinSS} equal to 0.1, the required maximum gain can be calculated using (59), and further the best D_{off} value can be calculated using (60) . The best D_{off} value in this case will be 0.28**.**

3.4 D_{off} selection for dual mode of operation

An alternate approach, as mentioned before in *section 3.1*, would be to operate the converter in tri-state boost mode when the input voltage is low implying higher gain requirement, and switch over to buck-boost mode when the input voltage is high. The potential benefit here would be a reduction in the maximum possible gain requirement of buck-boost and consecutively a higher D_{off} value. Recall that higher D_{off} value reduces the inductor current and hence, would lead to higher efficiency as well as small size of the inductor. This solution becomes a lot more attractive when one considers the fact that the transfer

function of boost as well as buck-boost modes of operation is the same and hence the same controller can be used for both modes of operation.

One needs to decide the input voltage range for which the mode of operation is boost and the point at which it transitions from boost to buck-boost mode, as this point of transition will be the lowest input voltage for buck-boost and will decide the maximum gain requirement for this mode of operation, which in turn will decide the value of D_{off}. In Table 1, the operating voltage range for the 2 modes as well as the resultant hysteresis for various D_{off} values is calculated. Note that the input voltage upper and lower limit are given as a fraction of the output voltage, to make the design scalable to any output voltage value. Further, the hysteresis value for 48 V nominal output voltage condition is given as well. Also, the equations used to get those values are re-mentioned here for ease of reference. These equations are the same as, or can be derived from the equations (38),(39) and (59), mentioned in *section 3.3.1 and 3.3.4* for buck-boost & equations (26) and (27) mentioned in *section 3.2.2* for boost. Note that for this system V_{oMax} = 1.1V_o and V_{oMin} = 0.9V_o, considering a 10 % margin in the DC bus value.

For tri-state boost mode,

$$Gain_{MaxSS} = \frac{(1-D_{fMinSS})}{D_{off}} \qquad V_{inMin} = \frac{V_{oMax}}{Gain_{MaxSS}}, \qquad \text{where} \quad V_{oMax} = 1.1\,V_o \text{ for this system}$$

$$Gain_{MinSS} = 1 + \frac{D_{onMinSS}}{D_{off}} \qquad V_{inMax} = \frac{V_{oMin}}{Gain_{MinSS}}, \quad \text{where} \quad V_{oMin} = 0.9\,V_o \text{ for this system}$$

For tri-state buck-boost,

$$D_{onMaxSS} = 1 - D_{off} - D_{fMinSS}, \qquad Gain_{MaxSS} = \frac{(D_{onMaxSS})}{D_{off}}, \qquad V_{inMin} = \frac{V_{oMax}}{Gain_{MaxSS}}$$

$$Gain_{Min} = \frac{D_{onMinSS}}{D_{off}}, \qquad V_{inMax} = \frac{V_{oMin}}{Gain_{MinSS}}$$

For dual mode of operation,

Hysteresis at switchover is given by ($V_{inMaxBoost} - V_{inMinBuckBoost}$)

Earlier, for the boost mode, the maximum input voltage was found to be $0.8V_o$ (*section 3.3.1*). One approach can be to consider this as the minimum input voltage for the buck-boost, giving a maximum gain requirement for buck-boost mode of operation, and consequently the value of D_{off} using equation (59) and (60).The 1st entry of Table1 shows this condition. This D_{off} value, though being correct for the ideal case, is not a very practical solution. One of the drawbacks is the very small value of voltage range overlap and hence small hysteresis in the switchover from one mode to the other, which makes the system prone to oscillations at the point of transition. Also, due to the effect of the dead time, as shown later in experimental results section, the effective D_{on} value for a steady state gain, changes and is also dependent on the direction of the current. Hence to give more safety margin in switchover by creating an overlap in the input voltage range of 2 modes, a lower D_{off} should be selected.

D_{off} = 0.38, D_{fMinSS} = 0.1, $D_{onMinSS}$ = 0.1			D_{off} = 0.35, D_{fMinSS} = 0.1, $D_{onMinSS}$ = 0.1		D_{off} = 0.35, D_{fMinSS} = 0.125, $D_{onMinSS}$ = 0.125	
Parameter	Boost	Buck boost	Boost	Buck boost	Boost	Buck boost
$Gain_{MaxSS}$	2.368	1.3684	2.57	1.5	2.5	1.5
$Gain_{MinSS}$	1.2632	0.263	1.285	0.2857	1.3571	0.357
V_{inMin}	0.464 V_o	0.658 V_o	0.389 V_o	0.67 V_o	0.44 V_o	0.6632 V_o
V_{inMax}	0.71 V_o	3.8 V_o	0.778 V_o	3.5 V_o	0.733 V_o	2.52 V_o
Hysteresis	0.05 V_o		0.108 V_o		0.07 V_o	
Hysteresis (V_o = *48)*	2.4 V		5.184 V		3.36 V	

Table 1: Illustration of D_{off} selection and resulting values of input range for both modes of operation

In the 2nd entry of Table1**,** a D_{off} value of 0.35 is selected and based on that, the operating voltage range for the 2 modes as well as the resultant hysteresis, is calculated. Further in the 3rd entry, with the same D_{off} value, the values of D_{fMinSS} and $D_{onMinSS}$ is increased from 0.1 to 0.125, to improve the worst case transient response, and all the values are calculated again. This seems the best solution in terms of providing ample gain as well as worst case dynamic range, and hence is used in this work.

3.5 Tri-state buck mode of operation

The buck mode of operation is needed in this application when SC has significantly higher voltage than the DC grid. This section deals with analysis of this mode using tri-state scheme, and presents the implementation as well as small signal analysis of the same. The switching period of tri-state, is again

divided into 3 regions. The direction of current flow for 3 time periods viz. D_{on}, D_{off} and D_f, is shown in Figure 3-15.

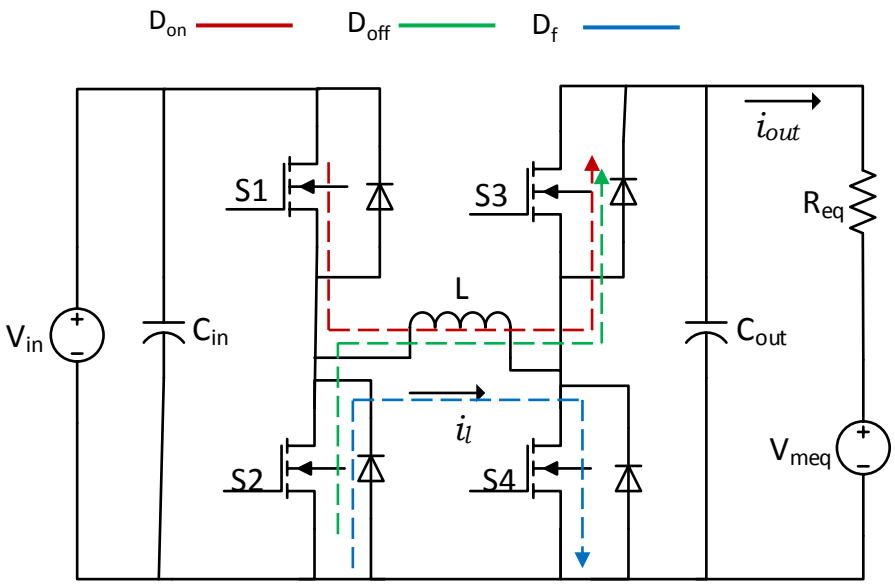


Figure 3-15: Illustration of Tri-state buck mode of operation

3.5.1 Small signal analysis

1)D_{on}: The Switches S1 and S3 are turned ON. The other 2 switches are complementary, i.e. S2 and S4 are turned OFF, which is essential for half-bridge operation. The inductor current increases and the voltage across the inductor is (V_{in} - V_o). If one considers the Inductor current (I_L) and the Output capacitor voltage (V_o) as state variables, the state equation for this state is given as:

$$\left[\frac{dI_L}{dt} = \frac{Vin - V_o}{L}\right]\left[C_{out}\frac{dV_o}{dt} = -I_{out}\right]\left[V_o = V_{meq} + I_{out}R_{eq}\right] \quad (61)$$

2)D_{off}: Here S3 and S2 are turned ON. The inductor current decreases and the voltage across the inductor is ($-$ V_o). The state space equation for this state can be given as

$$\left[\frac{dI_L}{dt} = \frac{-Vo}{L}\right]\left[C_{out}\frac{dV_o}{dt} = I_L - I_{out}\right]\left[V_o = V_{meq} + I_{out}R_{eq}\right] \quad (62)$$

3)D_f: Finally the 3rd stage is freewheeling period D_f, for which S2 and S4 are turned ON, short circuiting the inductor. For this case the state space equation will be,

$$\left[\frac{dI_L}{dt} = 0\right] \left[C_{out}\frac{dV_o}{dt} = -I_{out}\right] \left[V_o = V_{meq} + I_{out}R_{eq}\right] \quad (63)$$

After applying small perturbations and ignoring the resultant non-linear and DC terms, the TF of i_{out} with respect to d_{on} is given by

$$\frac{i_{out}}{d_{on}} = \frac{V_{in}}{(D_{off}+D_{on})^2(R_{eq}L_{eq}C_{out})}\left[\frac{1}{s^2+\frac{s}{R_{eq}C_{out}}+\frac{1}{L_{eq}C_{out}}}\right] where, L_{eq} = \frac{L}{(D_{on}+D_{off})D_{off}} \quad (64)$$

As evident, the value of L_{eq} depends on value of D_{on}, so its value changes with change in the input output voltage, thus changing the location of the 2 real poles obtained due to very low load resistance values.

In this work, the tri-state buck mode is not implemented as it adds unnecessary complexity to the control structure, without any significant advantages compared to conventional buck mode. Also, since the input voltage is not significantly higher than the voltage of the DC bus, the buck-boost mode of operation is enough for the cases when input voltage exceeds output voltage. Therefore, even conventional buck mode is not needed and hence not implemented in this converter design.

Chapter 4 Converter design

In this section, the component sizing for the 2 modes of operation of the converter, as well as their design methodology is presented. Further, an example of the component sizing for these modes of operation is also calculated and verified with the simulation results. The controller design for simulation and experimental prototype is presented as well.

4.1 Boost mode components size derivation

The aim of this work, as mentioned before is to design a fast acting DC-DC converter for interfacing supercapacitors with a DC nano-grid. The worst case is least input voltage which is equal to half of the DC bus. Essentially the variation in the DC bus is very small, whereas that in the supercapacitor is large. Hence, for derivation of various components, the worst case scenarios are decided based on the whole input voltage range, considering the DC bus to be constant. Recall that the value of D_{off} is also constant, and the system is being designed for a given value of output current. For visualization purposes, in many sections, the value of various parameters is calculated with respect to changes in the input voltage, and a plot of the same is given. Unless otherwise specified, the other operating parameters for these plots are V_o = 48V, I_{out} = 1A, L=38.8µH, C = 76.8µF, D_{off} = 0.35.

4.1.1 Input voltage range

As mentioned before, selection of D_{off} decides the maximum possible voltage gain of the converter and based on that one can calculate the minimum possible voltage of supercapacitor, such that one does not loses the control of the converter.

$$D_{onMaxSS} = 1 - D_{fMinSS} - D_{off} \tag{65}$$

Further, the minimum and maximum of the input voltage range can be calculated as in (66), (67). Using these equations, one can decide the input voltage range for a given D_{off} or calculate D_{off} for a given range

$$V_{inMin} = \frac{V_{oMax}}{1+\frac{D_{onMaxSS}}{D_{off}}} \tag{66}$$

$$V_{inMax} = \frac{V_{oMin}}{1+\frac{D_{onMinSS}}{D_{off}}} \quad (67)$$

4.1.2 Inductor selection

For inductor selection, the primary parameters to be calculated are ripple current, average inductor current and peak inductor current.

Ripple Current

For calculation of the ripple current, it is equal to the rise or fall in the inductor current every cycle, in steady state. Considering the change in inductor current due to the voltage across the inductor during D_{off}, which is (V_{in} – V_o), the ripple current can be derived as in (68), and the same can be used to find the ripple current with respect to the variation in V_{in}, keeping V_o, f_{sw} & D_{off} constant. Another approach can be to derive the equation as a function of duty cycle (D_{on}) instead of V_{in} (69), as this is the parameter which changes to account for change in V_{in} as well as I_{out}. Using (69), the value of the ripple current is calculated for different values of D_{on} for a system operating with unit output current and the input voltage varying from 24 to 48V, the same has been plotted in Figure 4-1.

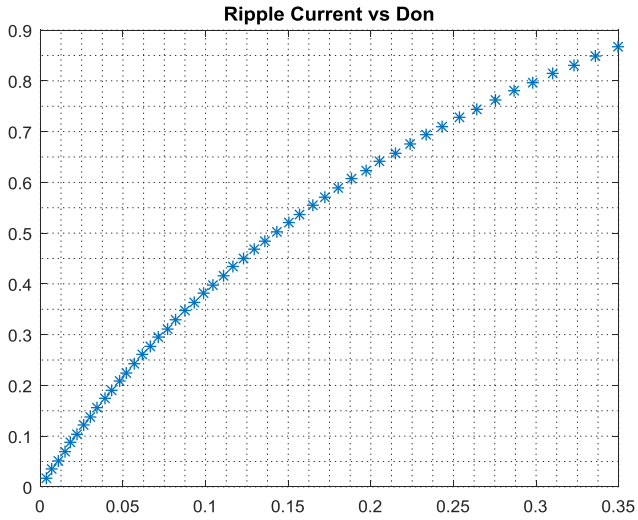


Figure 4-1: Inductor ripple current value with respect to variation in the On time

$$\Delta I_L = \frac{(V_o - V_{in})D_{off}}{Lf_{sw}} \quad (68)$$

$$\Delta I_L = \frac{V_{in} D_{on}}{L f_{sw}} = \left(\frac{V_o}{1+\frac{D_{on}}{D_{off}}} \right) \frac{D_{on}}{L f_{sw}} = \frac{V_o D_{on} D_{off}}{(D_{on}+D_{off}) L f_{sw}} \quad (69)$$

From the plot, one can see that the inductor ripple current increases with increase in D_{on}, which in turn means decrease in the input voltage, worst case being at the lowest possible input voltage.

Inductor average Current

The inductor current was already derived in the *section 3.2.2* and is further simplified here.

$I_{Lavg} = I_{L1}(D_{off} + D_{on}) + I_{min} D_f \Rightarrow I_{L1}(D_{off} + D_{on}) + \left(I_{L1} - \frac{\Delta I_L}{2}\right) D_f$, solving this further

$I_{Lavg} = I_{L1}(D_{off} + D_{on} + D_f) - \frac{\Delta I_L}{2} D_f$, Since $(D_{off} + D_{on} + D_f) = 1$

$$I_{Lavg} = I_{L1} - \frac{\Delta I_L}{2} D_f \quad (70)$$

Similar to the ripple current, one should derive the equation of average inductor current as a function of only D_{on}, by expanding the formula for ripple current (69) in equation (70).

$$I_{Lavg} = I_{L1} - \frac{\Delta I_L}{2} D_f \Rightarrow I_{L1} - \frac{V_o D_{on} D_{off}}{2(D_{on}+D_{off}) L f_{sw}} D_f \Rightarrow I_{L1} - \frac{V_o}{2 L f_{sw}} D_f \frac{D_{on} D_{off}}{(D_{on}+D_{off})}$$

Further replacing D_f,

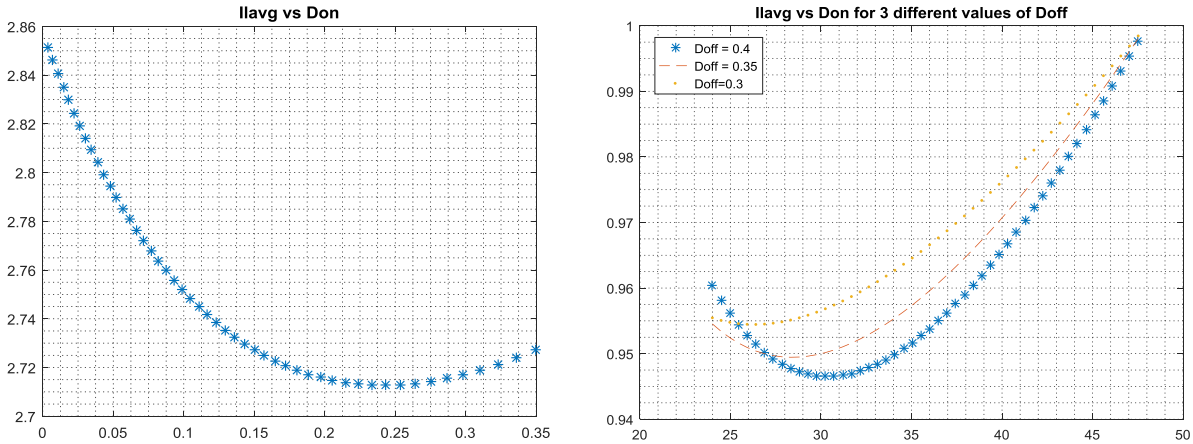
$I_{Lavg} = I_{L1} - \frac{V_o}{2 L f_{sw}} \frac{D_{on} D_{off}}{(D_{on}+D_{off})} (1 - (D_{on} + D_{off}))$, This can be reduce to

$$I_{Lavg} = I_{L1} - \frac{V_o D_{off}}{2 L f_{sw}} \left[\frac{D_{on}}{(D_{on}+D_{off})} - D_{on} \right] \quad (71)$$

Since the determination of the worst-case average inductor current from this equation is not very straight forward, one can calculate its value w.r.t. variation in D_{on}, and the plot of the same is shown in Figure 4-2(a) and it can be seen that there are 2 maxima for the inductor current. It seems that the maximum average inductor current is obtained at lowest D_{on} which implies maximum input voltage. However, one should also consider the fact that the maximum input voltage for boost mode is limited to a predefined value based on D_{off} selection (*section 3.34*), and hence, while comparing the 2 maxima, D_{on} corresponding to that input voltage should be considered. Also, the 2 maxima for the inductor current may vary based

on the type of curve. The parameter which affects the inductor current curve is D_{off}, and to observe its effect, the same plot is given for 3 different values of D_{off} in Figure 4-2(b)**.** Note that the x-Axis is not D_{on} but V_{in}, as the value of D_{on} will vary with respect to D_{off} as well, and hence the only common parameter for comparison here is the input voltage. Also, since one wishes to see only the change in the inductor current curve with respect to D_{off}, each curve is normalized with respect to the corresponding I_{L1}, as this is the parameter which varies with respect to D_{off} selection for a given output current. It can be seen that as D_{off} increases, one gets higher value of lower voltage maxima, and hence the inductor current maxima should be determined depending on the curve generated for the particular value of D_{off} used.

Note that for the worst case, the output voltage considered in the equation should be equal to the minimum output voltage, as that will give minimum value for the negative part of the equation (71).



(a) (b)

Figure 4-2: Analysis of average Inductor current variation with respect to variation in (a) D_{on}; (b) V_{in} and D_{off}

Inductor peak current

The inductor peak current is given by

$$\widehat{I_L} = I_{L1} + \frac{\Delta I_L}{2} => \frac{I_{out}}{D_{off}} + \frac{2V_o D_{on} D_{off}}{(D_{on}+D_{off})Lf_{sw}} \quad (72)$$

Since I_{L1} is constant for a given output current, and the ripple increases with increase in D_{on} (decrease in input voltage), the worst case peak is obtained at the largest D_{on} implying lowest input voltage.

Inductor RMS current

The inductor RMS current equation is given in (73). Since, the worst case average current was obtained at maximum input voltage, the worst case RMS current should also be calculated at the same value.

$$I_{LRMS} = \sqrt{{I_{L1}}^2 + \frac{{\Delta I_L}^2}{4} D_f - I_{L1}\Delta I_L D_f} \qquad (73)$$

4.1.3 Capacitor selection

For the selection of the output capacitor, the important parameters to be calculated are the capacitance and the capacitor RMS current.

Output Capacitor value

The capacitor value will depend on the allowable output ripple current. It is similar to the output capacitor equation of the Boost mode and is given by

$$\frac{\Delta I_{out}}{I_{out}} = \frac{DT_S}{RC} = \frac{1-D_{off}}{RCf_{sw}} \qquad \text{Where R = } R_{eq} \text{ and C = } C_{out} \qquad (74)$$

Output capacitor RMS current

For the calculation of the capacitor current, it can be calculated as the difference of switch S3 current and the output current, and the waveforms of the same is shown in Figure 4-3.

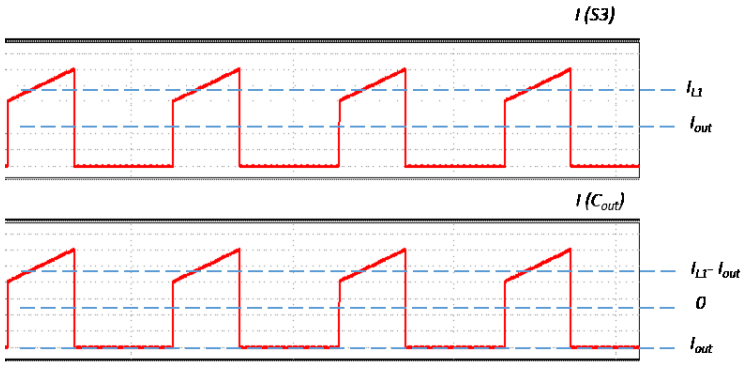


Figure 4-3: Illustration of capacitor RMS current calculation

As seen, the capacitor current can be divided into a sum of a pulse wave of amplitude equal to (I_{L1}-I_o) and a triangular ripple current during D_{off}; and negative of output current during (1-D_{off}). Hence, Capacitor RMS current will be given by

$$I_{CRMS}{}^2 = (I_{L1} - I_{out})^2 D_{off} + \frac{\Delta I_L{}^2}{12} D_{off} + I_{out}{}^2 \left(1 - D_{off}\right) \quad (75)$$

On further simplification, the capacitor current can be found as

$$I_{CRMS} = \sqrt{I_{out}{}^2 \frac{\left(1-D_{off}\right)}{D_{off}} + \frac{\Delta I_L{}^2}{12} D_{off}} \quad (76)$$

As evident, the capacitor current primarily depends on the ripple current, and hence should be calculated for the worst case value of the same.

4.1.4 Diode and switch selection

For Tristate boost mode of operation, the equations for the switch currents were derived in *section 3.2.1* and a plots for the RMS current variation of switch 3 and 4 w.r.t D_{on} were given as well. Here all 4 switch currents are plotted w.r.t. variations in D_{on} for D_{off} = 0.35 and are shown in Figure 4-4.

It can be seen that for switch 1 and switch 3, the maximum current is obtained at maximum D_{on} implying minimum input voltage, whereas for switch 2 and switch 4 it is obtained at lowest D_{on} which implies highest input voltage. For switch 4, a secondary maxima near maximum D_{on} can be seen as well, but this value is still lower than that at D_{onMin} of 0.125 decided earlier. The switches should be sized according to the current obtained for their respective worst case conditions. Moreover, the switches are connected in form of 2 half bridges, hence their worst case voltage should be equal to maximum voltage on the DC bus. The peak current for all the switches is equal to peak inductor current.

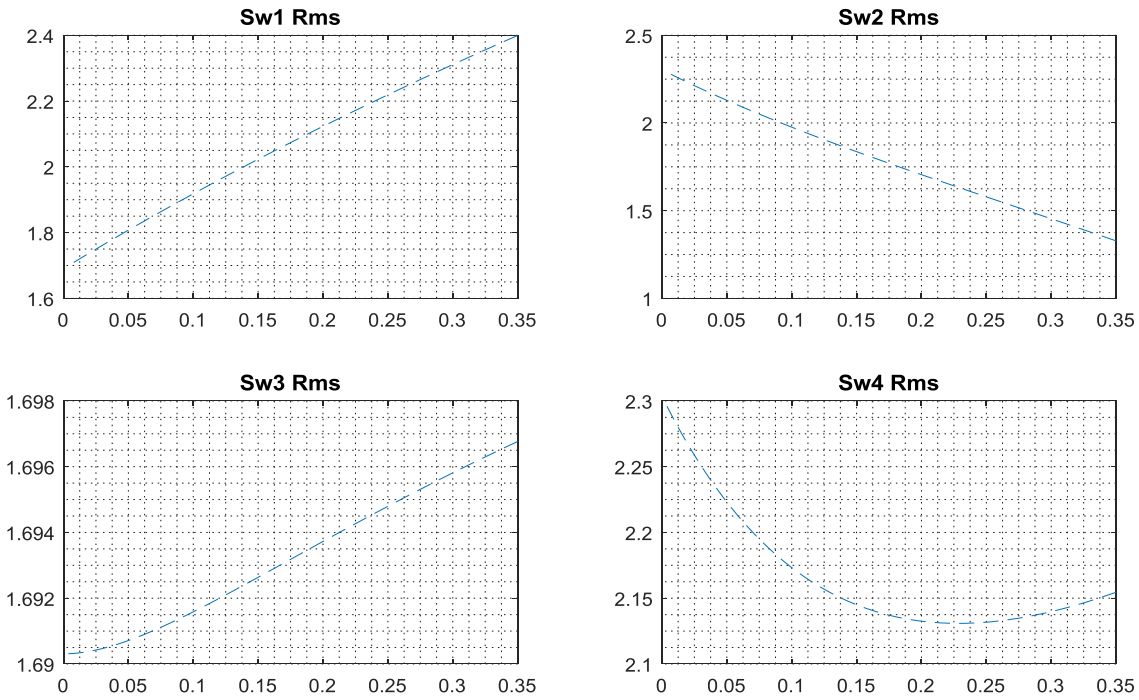


Figure 4-4: RMS current variation of 4 switches with respect to D_{on} for boost mode of operation.

4.1.5 Design summary

After deriving the equations for all the components, here a step by step sequence for designing the system is given. It should be noted that this is considering only the tri-state boost mode of operation.

Key System Specifications:

1. Max output current (I_{out})
2. Maximum output voltage (V_o)
3. Switching frequency (f_{sw})
4. Input voltage range is $V_o/2$ to V_o .
5. Parameters of the DC nano-grid model i.e. R_{eq}.

❖ Decide the value of D_{off} based on the minimum input voltage, or in other words, required maximum voltage gain. Note that, keeping minimum input voltage as half of the output DC bus is advised.

- For inductor sizing, one needs the inductance, worst case ripple and RMS/Average inductor current.
  - Decide the worst case ripple allowed for the system as a percentage of the maximum I_{L1}.
  - Using ripple current calculated in previous step and lowest possible input voltage as V_{in}, calculate the value of L using (69). Note that the value of D_{off} and F_{sw} is already decided.
  - Calculate the maximum inductor current (RMS/Average) at the highest input voltage for a given value of output current using equation (73)/ (71).
- For, selection of the capacitor one needs its capacitance value as well as the worst case ripple current.
  - The capacitor value should be calculated from (74) depending on the allowable output ripple current, as well as the R_{eq}.
  - The capacitor RMS current can be calculated by (76), with the ripple current being the worst case ripple current of the system.
- For, selection of the switches, one needs to calculate their worst case RMS current and drain-source voltage. The currents can be calculated by equations (20) to (23), interpreted for their worst case; and the worst case voltage is equal to maximum output and input voltage for the respective half bridges.

4.2 Buck-boost mode components size derivation

For the buck- boost mode also, one needs to define the component sizing equations.

4.2.1 Input voltage range

In buck-boost mode of operation, the steady state voltage gain is given by ratio of D_{on} and D_{off}. Hence, using this in (66) and (67), similar to boost mode, the equations for V_{inMin} and V_{inMax} can be given by (77) and (78).

$$V_{inMin} = \frac{D_{off} V_{oMax}}{D_{onMaxSS}} \quad (77)$$

$$V_{inMax} = \frac{D_{off} V_{oMin}}{D_{onMinSS}} \quad (78)$$

4.2.2 Inductor selection

For inductor selection, the primary parameters to be calculated are ripple current, average inductor current and peak inductor current. Similar to calculations for the tri-state boost, these values can be calculated for the buck-boost mode as well.

The inductor ripple current can be derived as in (79), and one can see that it is independent of the input voltage. Also, the average current, RMS current and peak current for the inductor are given by (80), (81) and (82) respectively.

$$\Delta I_L = \frac{(V_o)D_{off}}{Lf_{sw}} \tag{79}$$

$$I_{Lavg} = I_{L1} - \frac{\Delta I_L}{2}D_f \Rightarrow I_{L1} - \frac{V_o D_{off}}{2Lf_{sw}}D_f \Rightarrow I_{L1} - \frac{V_o D_{off}}{2Lf_{sw}}(1 - D_{on} - D_{off}) \tag{80}$$

$$\widehat{I_L} = I_{L1} + \frac{\Delta I_L}{2} \Rightarrow \frac{I_o}{D_{off}} + \frac{V_o D_{off}}{2Lf_{sw}} \tag{81}$$

$$I_{LRMS} = \sqrt{{I_{L1}}^2\left(D_{off} + D_{on}\right) + \left(I_{L1} - \frac{\Delta I_L}{2}\right)^2\left(1 - \left[D_{on} + D_{off}\right]\right)} \tag{82}$$

It can be seen from the above equations that, the average/RMS inductor current is maximum for maximum value of D_{on}, which implies lowest input voltage, whereas for a given I_{out} and V_o, I_{L1} and the ripple is always constant, thus the peak inductor current is also constant.

4.2.3 Capacitor selection

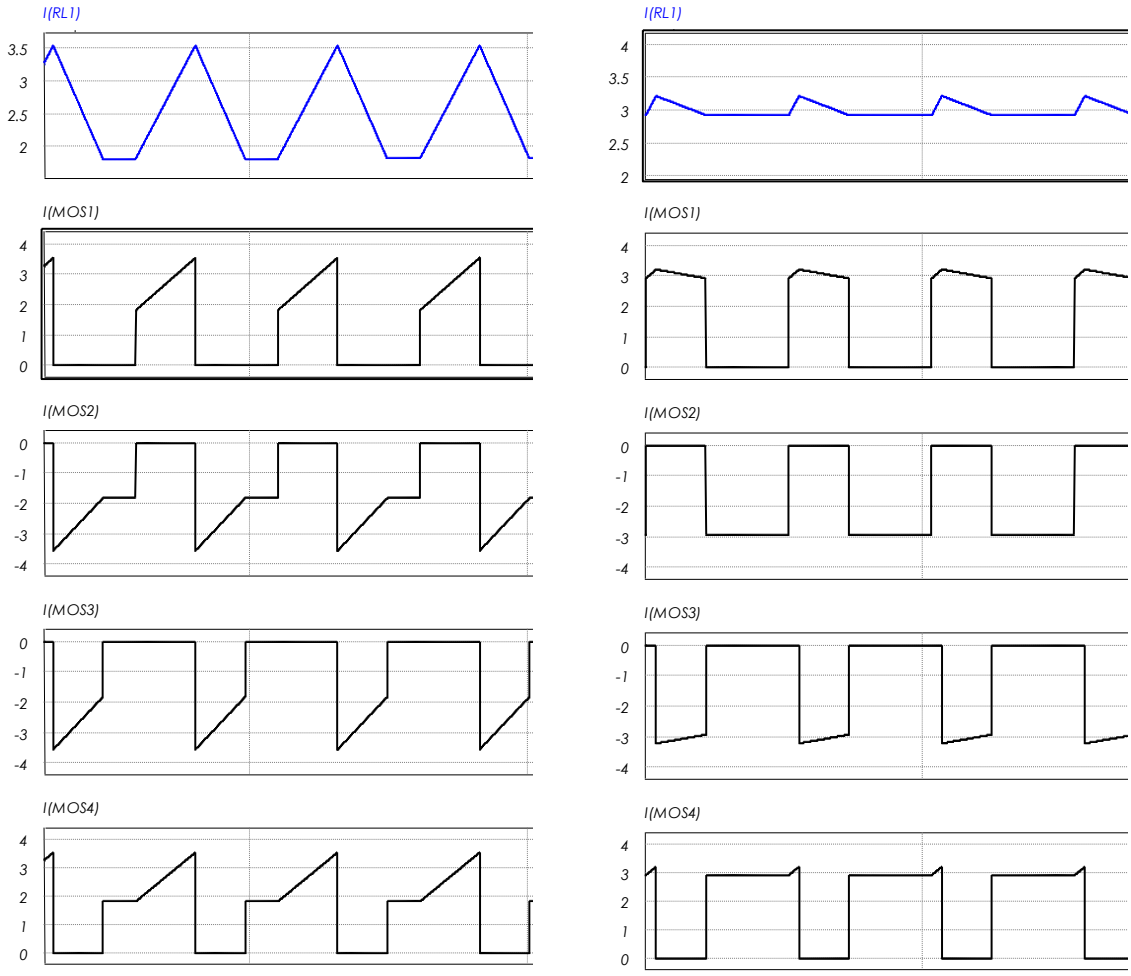
The capacitor current waveform in the buck-boost mode of operation is same as that in boost mode, hence the formula for capacitor RMS current is also the same.

$$I_{cRMS} = \sqrt{{I_{out}}^2\frac{\left(1-D_{off}\right)}{D_{off}} + \frac{{\Delta I_L}^2}{12}D_{off}} \tag{83}$$

As evident from the equation, the capacitor RMS current is the same irrespective of the input voltage, and should be calculated for the maximum output voltage as that would imply maximum ripple current.

4.2.4 Diode and switch selection

To compare the current waveforms of various switches in boost and buck-boost mode, simulation results for both modes of operation are presented in Figure 4-5, where the input voltage is in the overlap region of 2 modes of operation being equal to 40V (0.833 V_o, refer *section 3.4*), the other parameters for these waveforms are, V_o = 48V, D_{off} =0.35 and I_{out} = 1A.



(a) (b)

Figure 4-5: Comparison of inductor current and switch waveforms for (a) Tri-state buck- boost and (b) Tri-state boost mode of operation for same operating conditions.

As evident in Figure 4-5, the basic shape of the waveforms is the same for switch 3 (I(*MOS3*)) and switch 4 (*I(MOS4)*), the only difference is that the buck boost mode has a higher ripple compared to the boost mode due to the fact that the voltage across the inductor in D_{off} state is equal to V_o in the former and V_{in} - V_o in the latter. Consequently, for Switch 3 and Switch 4 the equations of current are the same. For all the switches the equations for calculating their RMS current were mentioned in *section 3.3.3*. Here a plot of their RMS current variation w.r.t. to variation in input voltage and hence in D_{on}, is given in Figure 4-6. The variation in the input voltage is from 35 Volts to 52 Volts to cover both cases, when input is very close to output voltage and also, when it is higher than the output voltage.

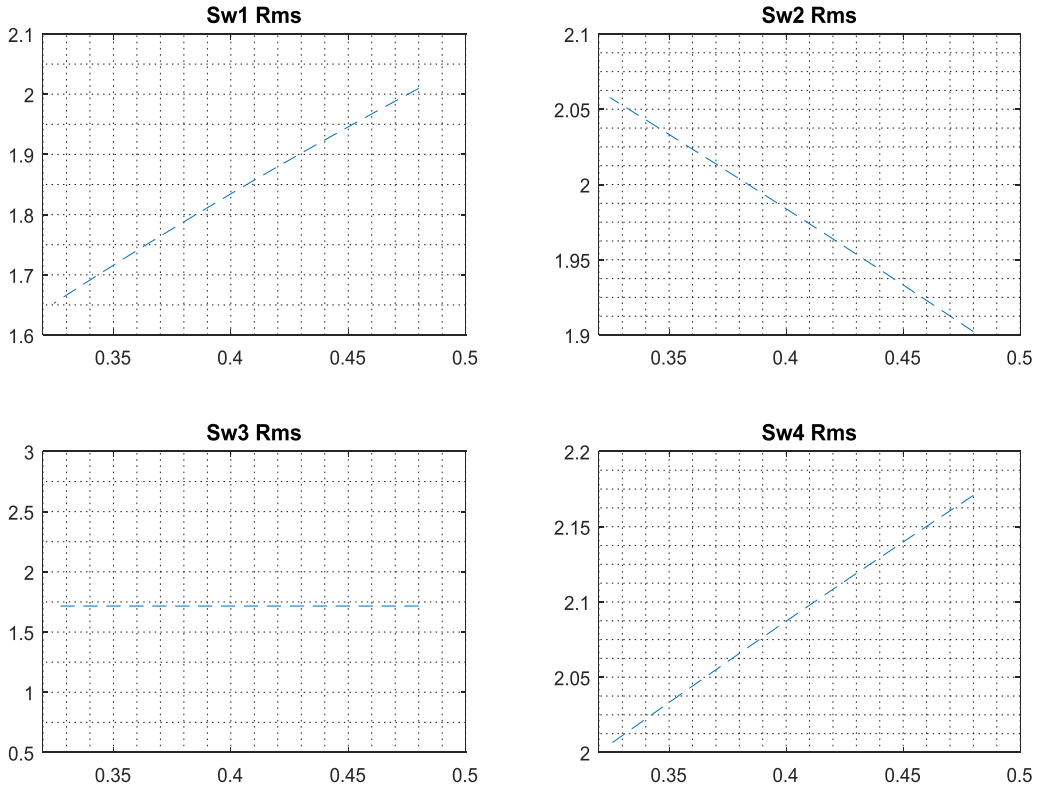


Figure 4-6: RMS current variation for 4 switches in buck-boost mode of operation, w.r.t. variation in D_{on}

For the selection of switches, one needs to compute their worst case RMS current and the condition in which the worst case occurs. From the plots in Figure 4-6, one can see that switch 1 and switch 4 have the maximum current flowing through them when D_{on} is maximum, implying lowest input voltage, whereas

for switch 2, the same occurs at minimum D_{on}, or maximum input voltage. In switch 3 current always stays constant.

The maximum RMS current for each switch has to be calculated at its respective worst case condition and based on that one can select an appropriate device. The worst case of collector-emitter voltage is equal to the maximum possible input and output voltage of the converter, for the switches in the respective input and output side half-bridges. Another important parameter is the peak switch current, which for all the switches, is equal to the peak inductor current calculated in *section 4.2.2*.

4.2.5 Design summary for the buck-boost mode of operation

The worst case values for various components will be different for buck-boost mode of operation compared to that of boost. However, the design steps are similar.

Key system Specifications:

1. Max output current (I_{out})
2. Maximum output voltage (V_o)
3. Switching frequency (f_{sw})
4. Input voltage range is $V_o/2$ to V_o.
5. Parameters of the DC nano-grid model i.e. R_{eq} and V_{meq}.

- Decide the value of D_{off} based on the minimum input voltage, or in other words, required maximum steady state voltage gain. Note that, the minimum input voltage is calculated as in *section 3.4* for dual mode of operation.
- For inductor sizing, one needs the inductance, worst case ripple and RMS/Average inductor current.
  - Decide the worst case ripple allowed for the system as a percentage of the maximum I_{L1}.
  - Using ripple current calculated in previous step, calculate the value of L (79). Note that the value of D_{off} and F_{sw} is already decided.
  - Calculate the maximum inductor current (RMS/Average) at lowest input voltage for a given value of output current using equation (82)/ (80).
- For the selection of the capacitor one need its capacitance value as well as the worst case ripple.

- The capacitor value should be calculated from (74) depending on the allowable output ripple current, as well as the R_{eq}. whereas, the capacitor RMS current can be calculated by (76), with the ripple current being the worst case ripple current of the system.

❖ For, the selection of the switches, one needs to calculate their worst case RMS current and drain-source voltage. The currents can be calculated by equations (51) to (54) for their respective worst case condition, whereas the worst case voltage is equal to the maximum output and input voltages for the respective half bridges.

4.3 Case study to verify the equations of both modes

In this section, the equations for the 2 modes of operation are verified with the simulation results. For this the operating parameters are V_{out} = 48V, L = 38.8 µH, C_{out} = 76.8 µF, I_{out} = 5 A, V_{in} = 24V for boost mode of operation and 40 V for buck-boost mode of operation.

Tri-state boost (V_{in} = 24V, V_o = 48V, L = 38.8µH, C_{out} = 76.8µF , I_{out} = 5A)		
Parameters	Calculated value	Simulation Result
Inductor Ripple current	0.866	0.869
Inductor Average current	14.155	14.118
Inductor RMS current	14.1572	14.1216
Inductor Peak current	14.718	14.685
Capacitor RMS current	6.8154	6.727
Switch 1,2,3 and 4 RMS Current	11.95, 7.59, 8.45, 11.36	11.94, 7.542, 8.34, 11.395

Table 2: Case study for tri-state boost design calculations

Tri-state buck- boost (V_{in} = 40V, V_o = 48V, L = 38.8µH, C_{out} = 76.8µF , I_{out} = 5A)		
Parameters	Calculated value	Simulation Result
Inductor Ripple current	1.732	1.74
Inductor Average current	14.0865	14.086
Inductor RMS current	14.091	14.098
Inductor Peak current	14.718	14.685
Capacitor RMS current	6.82	6.7728
Switch 1,2,3 and 4 RMS Current	9.2638, 10.627, 8.45, 11.28	9.2936, 10.60, 8.46, 11.277

Table 3: Case study for tri-state buck- boost design calculations

From both the tables, one can see that the calculated values are very close to that of the simulation results. The little error seen can be attributed to the fact that, for simulation, the output current has been obtained using a control loop and the actual output current may have minor errors w.r.t. the set point.

4.4 Control loop design

The plant transfer function for the boost and buck-boost modes was discussed in *section 3.2.3* and *section 3.3.2* respectively, and it was found that the transfer function of the output current with respect to d_{on} is the same in both modes of operation. This simplifies the controller design to a great extent as the same controller can be used for both the modes.

Another aspect of the design, as mentioned in the *section 3.4*, is that the converter switches over from one mode to the other based on the desired voltage gain, with tri-state boost being mode of operation for higher voltage gain and buck-boost for lower. At the point of switchover, the ideal condition would be that the controller does not experience any transients at all, or in other words the output of controller should not change irrespective of the mode of operation.

The steady state gain of the buck-boost mode is given by:

$$V_o = \left[\frac{D_{on}}{D_{off}}\right] V_{in} \tag{84}$$

Whereas that of the boost, is given by:

$$V_o = \left[\frac{D_{on}+D_{off}}{D_{off}}\right] V_{in} \tag{85}$$

At the point of transition, the output voltage and input voltage are the same for the 2 equations. As a result, the corresponding D_{on} value for getting the same voltage gain will be different. This causes a transition in the controller at every switch over.

A solution for this can be to treat the controller output as $D_{on} + D_{off}$ in boost and as D_{on} only in buck-boost. Since D_{off} is a constant or a DC value, the plant transfer function for boost mode of operation still stays the same, irrespective of whether the controller output is D_{on} or $D_{on} + D_{off}$.

It should be noted that in the boost mode, to keep D_{off} constant, one must limit the controller output to a lower limit of D_{off}. This is to ensure that one still gets a constant D_{off}, even if in case of a transient, the controller's output tends to go below it. Similarly, the upper limit will be $D_{onMax} + D_{off}$.

As mentioned in Chapter 2, for the conventional dual-state modes of operation, the transfer function concerning the control of the current injected into the DC grid by means of duty cycle (D) control presents a RHP zero. A usual approach for dealing with this is to employ an inner inductor current loop with an outer injected current loop. In this case, PI type controllers were designed to achieve a crossover frequency (bandwidth) of 35 kHz and a phase margin of 54° for the inner loop and a crossover frequency of 2.5 kHz and a phase margin of 80° for the outer loop.

Conversely, using the tri-state logic with constant D_{off}, the transfer function of the current injected into the DC grid by means of duty cycle (D_{on}) control does not present the RHP zero. This allows the use of a single control loop with a relatively high crossover frequency (20 kHz) and a phase margin of 45°. The parameters of the PI type 2 controller calculated for this case are: K_{PI} = 0.7010, τ = 795 µs and T_p = 2.12 µs.

Apart from simulation, an experimental prototype of the proposed converter is developed as well, wherein an Infinite Impulse response (IIR) digital controller generated from a PI Type 2 has been used. One of the important parameters of the digital controllers is the sampling frequency of the feedback sensor, and in principle, one has to limit the bandwidth of the converter to a maximum of $1/20^{th}$ of the sampling frequency for stable operation. In this work, the 250 kHz is not only the PWM but also the sampling frequency of the controller and hence the controller bandwidth has to be below 12.5 kHz. Consequently, the cut off frequency for the experimental prototype is selected as 10 kHz.

Coming to the controller design for the same, a PI Type 2 controller was designed with a phase margin of 68°, K_{PI} = 0.6133, τ = 318 µs and T_p = 1.87 µs.

Chapter 5 Simulation

The performance of the tri-state logic applied to a 4-switch interface of a supercapacitor to a DC nano-grid is verified by means of simulation using PSIM (*version 10.0*). The schematic of the converter as well as the implementation of the 2 modes of operation, each operating with 2 types of switching scheme based on the direction of the power flow, are presented here. Further the response of the converter for both positive and negative transients are provided as well. For comparison purposes, the behavior of the 4-switch converter operating with the conventional dual-state duty cycle control scheme is also presented. In such a case, for the dual-state boost mode of operation, S1 remains on all the time, while S4 operates with PWM in order to control the current injected into the DC nano-grid, whereas for the dual state buck-boost mode of operation, S1 and S3 are switched for the same.

5.1 Simulation schematic

As mentioned before, a 4 switch bi-directional converter is used in this work, the same as implemented in the PSIM simulation, can be seen in the Figure 5-1. The other parameters viz. D_{off} and f_{sw} can also be seen in the figure.

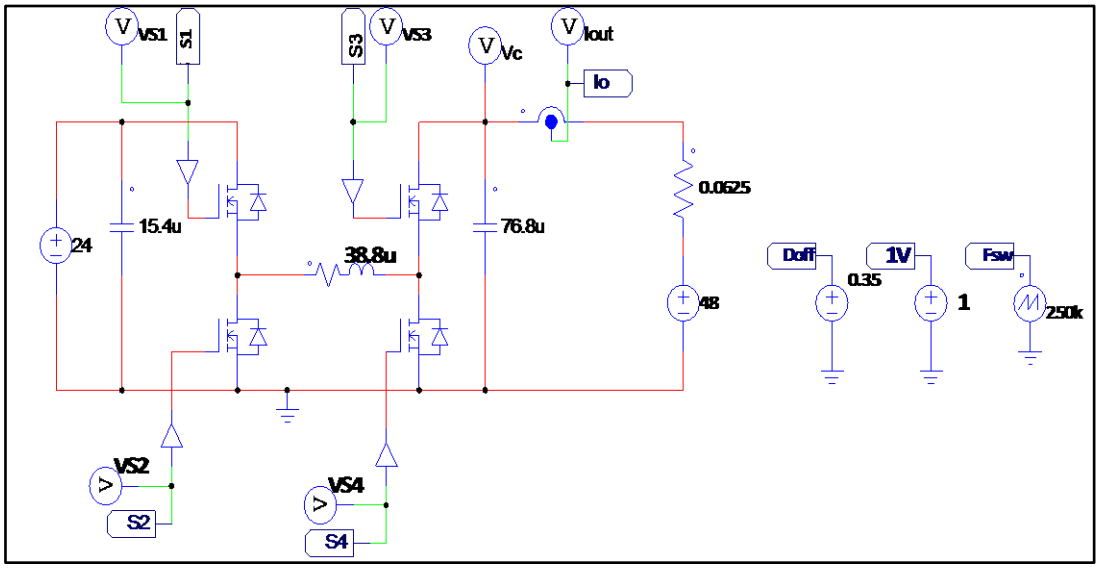


Figure 5-1: The schematic of the converter for simulation in PSIM

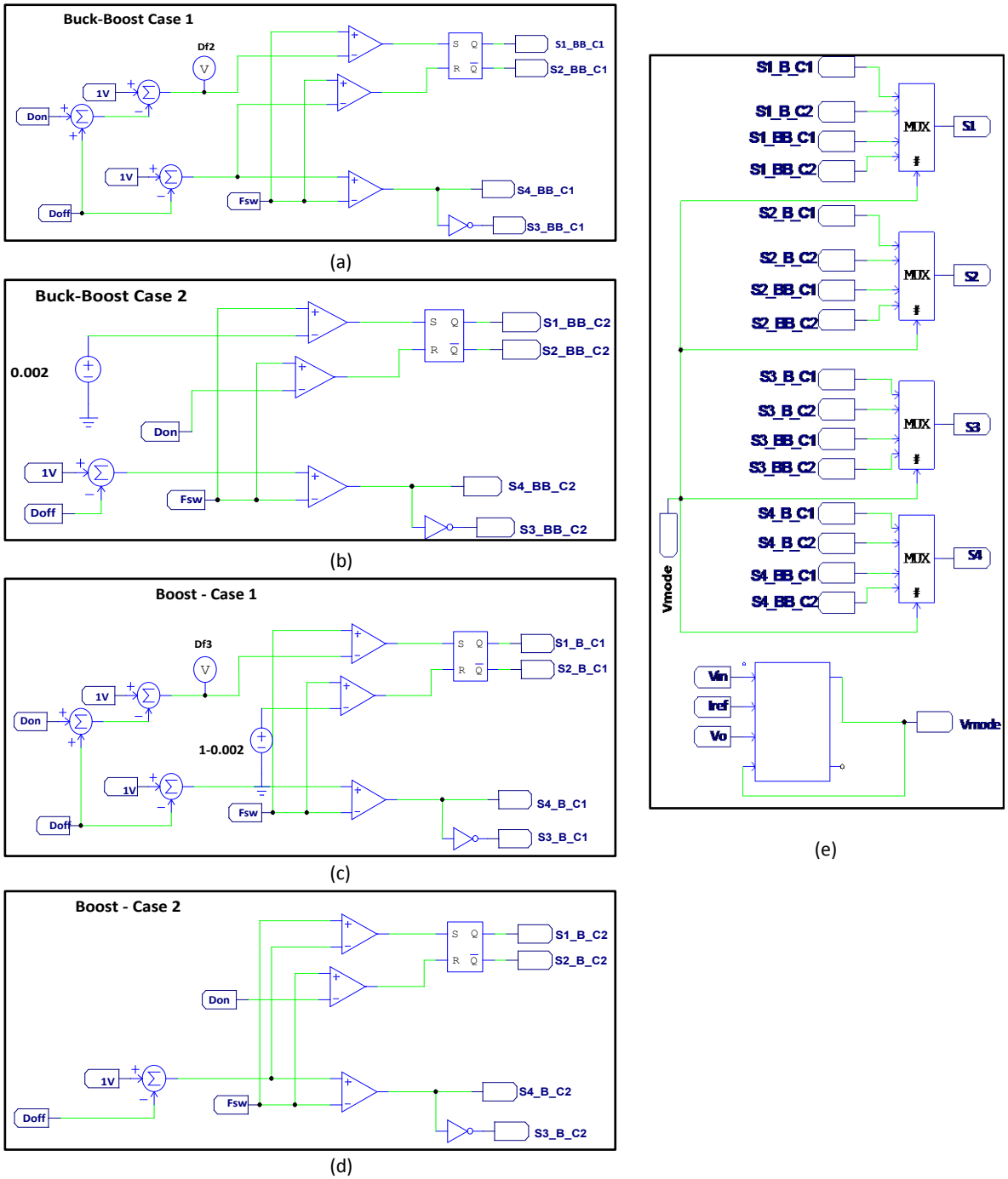


Figure 5-2: Implementation of Gate signal logic for 4 modes of operation. (a) Buck- Boost mode sequence 1 (b) Buck-Boost mode sequence 2 (c) Boost mode sequence 1 (d) Boost mode sequence 2 (e) Selection of 4 cases using Mux

The 4 switches are controlled by the gate signal generation logic shown in Figure 5-2, which again concerns

4 different types depending on the mode of operation, i.e. boost or buck-boost, as well as the type of switching sequence used in a given mode. The selection between these modes is done by a 4 by 1 Mux as in Figure 5-2. For implementing 4 different types of switching sequence, in the first half-bridge, one needs a lot more flexibility than a normal PWM (PWM using a reference and a single comparator), hence it is implemented using 2 comparators for high to low and low to high transition of the PWM, with the SR Flip Flop used to hold the state of ON or OFF until the output of other comparator changes the state. Conversely, for the 2nd Half-Bridge, the D_{off} is always constant and hence that's implemented with a simple comparator and a NOT gate.

The truth-table of all the switches for 3 states of operation depending on the modes of operation, can be found in the Table 4**.**

Tri-state Boost				
State/ Switches	Switch 1	Switch 2	Switch 3	Switch 4
D_{on}	ON	OFF	OFF	ON
D_{off}	ON	OFF	ON	OFF
D_f	OFF	ON	OFF	ON
Tri-state Buck-Boost				
D_{on}	ON	OFF	OFF	ON
D_{off}	OFF	ON	ON	OFF
D_f	OFF	ON	OFF	ON

Table 4: Truth-Table of 4 switches for various modes of operation

5.1.1 Tri-state boost case 1

Tri-state boost *case 1* is used when the converter is operating in boost mode with forward power transfer, i.e. from the supercapacitor to the DC bus. The 1st state is D_f followed by D_{on} and D_{off}, which ensures the freewheeling of minimum inductor current. As evident from Table 4**,** switch 1 has to stay low for D_f**,** followed by high state for D_{on} and D_{Off}. For this SR Flip Flop for switch 1, is turned high by the 1st comparator when the saw-tooth carrier of 250 kHz is equal to D_f, and then turned low again at the end of the cycle.

The amplitude of the carrier is $1V_{pp}$ and the D_f is generated by subtracting D_{off} + D_{on} from the peak value of 1 (Figure 5-2(c)). The gate signal for switch 2 is simply the complement of that of switch 1.

The sequence of states in the 2nd bridge should be the same as that of the 1st bridge, i.e. D_f and D_{on} followed by D_{off}, implying that switch 4 should be high for a time period of 1-D_{off} (D_{on} + D_f =1-D_{off}) and then turn low during D_{off}, the same is implemented using a single comparator. Switch 3 is simply the complement of switch 4 and is generated by a adding a NOT gate (Figure 5-2(c)).

5.1.2 Tri-state boost case 2

Tri-state boost *case 2* is used when the converter is operating in boost mode with reverse power transfer from the DC bus to the supercapacitor. In this mode, D_f has to be between D_{on} and D_{off} resulting in a state sequence of D_{on} and D_f followed by D_{off}. Switch 1 has to be ON for D_{on}, OFF for D_f and then ON again for D_{off} followed by D_{on} of next cycle. One can see that, the high to low transition is after D_{on} and low to high is after D_{on} + D_f, and hence these are the inputs for 2 comparators (Figure 5-2(d)). Recall that D_{on} +D_{off} is equal to 1-D_{off}.

5.1.3 Tri-state buck- boost case 1

Buck-boost *case 1* is used when the converter is operating in buck-boost mode with forward power transfer from the supercapacitor to the DC bus. It is similar to the tri-state Boost *case 1* in terms of sequence of states i.e. D_f followed by D_{on} and D_{off}, however the state of switch 1 for D_{off} is different, the same being turned low instead of staying high, as in tri-state boost. One can see that, the high to low transition is after D_f and low to high is after D_{on} + D_f, and hence these are the inputs for 2 comparators (Figure 5-2(a)).

5.1.4 Tri-state buck- boost case 2

Buck-boost *case 2* is used when the converter is operating in buck-boost mode with reverse power transfer. It is similar to the tri-state boost *case 2* in terms of sequence of states i.e. D_{on} followed by D_f and D_{off}, however the state of switch 1 for D_{off} is different, the same being turned OFF instead of staying ON, as in tri-state boost. One can see that, the high to low transition is after D_f and low to high is at the

beginning of the cycle, and hence these are the inputs for the 2 comparators (Figure 5-2(a)).

5.1.5 Selection of mode of operation

As seen in Figure 5-2(e), the selection of modes is done using a 4 by 1 Mux, with the selection line controlled by a software block. The output of the Mux is used to drive the 4 switches. The code in software block basically takes the direction of reference current as the input and based on its being positive or negative, selects between sequence 1 and sequence 2 for the given mode of operation. At the same time, it also takes in the input and output feedback, and based on the required voltage gain, it selects between the 2 modes of operation. As discussed before in *section 3.4*, there is a hysteresis band for mode selection to ensure noise immunity. The output of the block can be 0, 1, 2 and 3, for selecting boost case 1, boost case 2, buck-boost case1 and buck-boost case 2 respectively.

5.1.6 Controller implementation and anti-windup

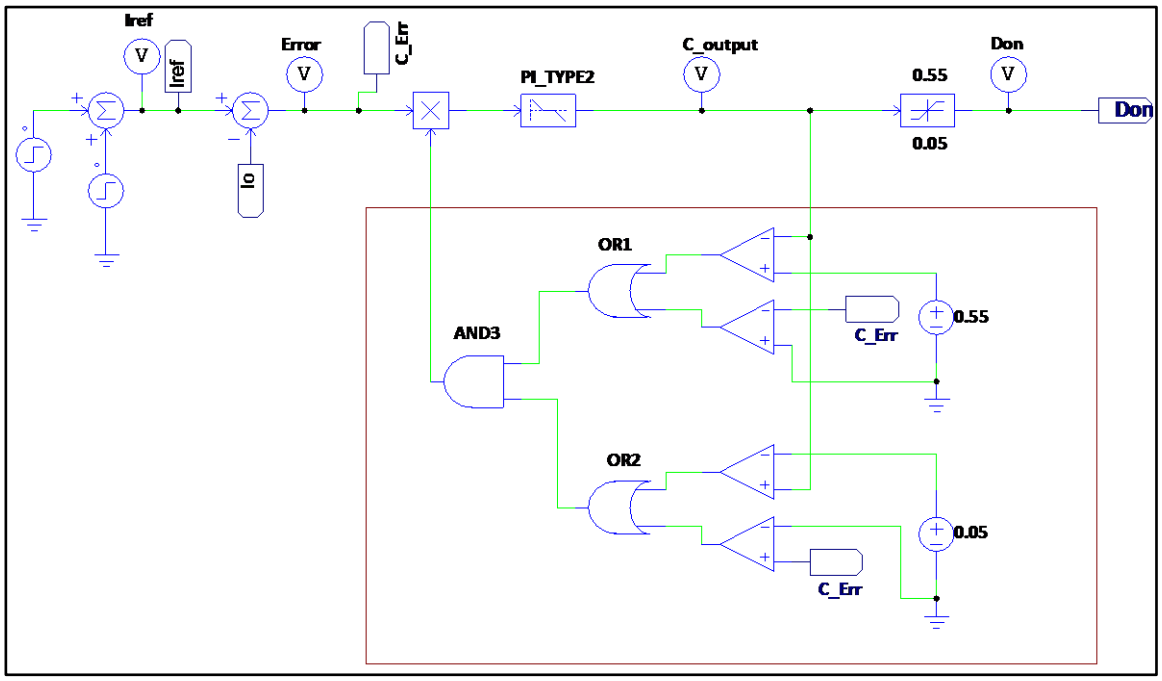
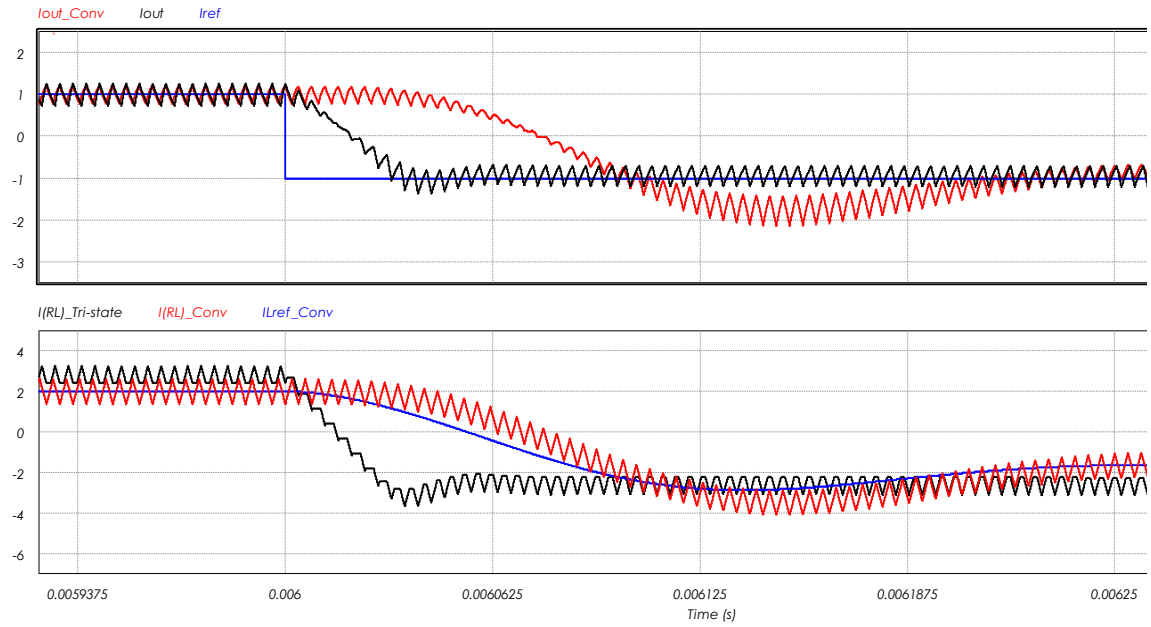


Figure 5-3: Controller Implementation in PSIM and anti-wind up logic

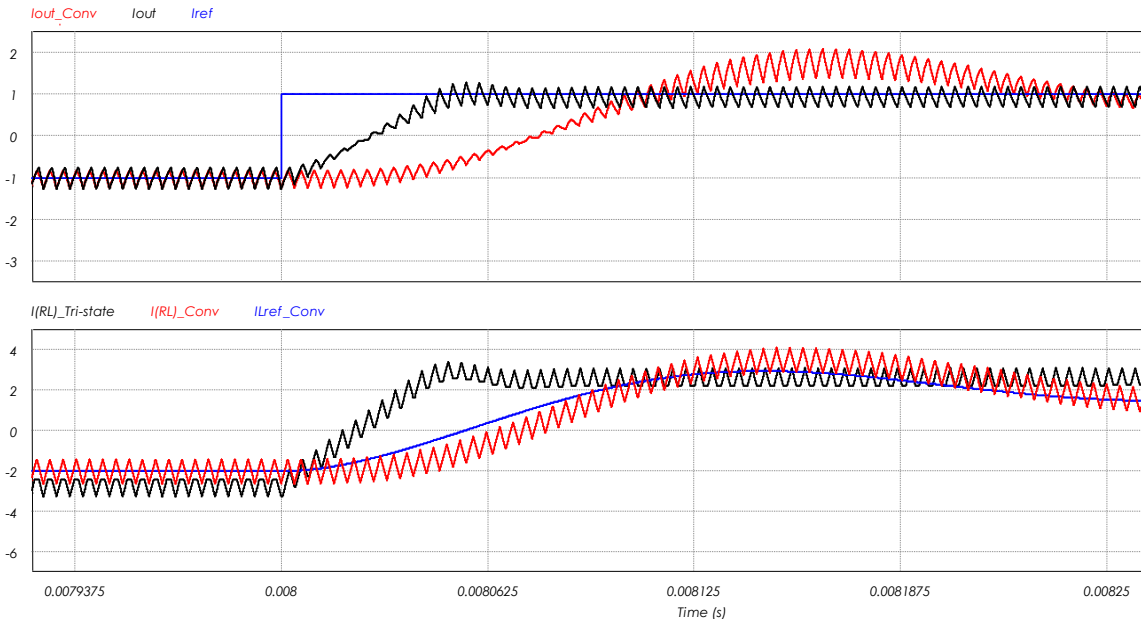
As mentioned in *section 4.4*, a PI type-2 controller is used to control the output current injected into the DC bus. The controller implementation is shown in Figure 5-3. Note than this setup is used to check the transient response of the injected current control loop with the summer near I_{ref} label used for providing the transient in the current reference value. One of the issues with an integrator is accumulation of large error during saturation, what is commonly known as integral wind up. The effect is that the plant has to have an opposite polarity error to unwind the integrator, what would lead to oscillations in the output response and excess overshoot. To prevent this, one of the alternatives is to sense the state of saturation, and make the corresponding error fed into the integrator equal to zero, when it happens. The circuit (with in the rectangle) in Figure 5-3, consisting of 4 comparators, 2 OR gates and an AND gate is included for this very purpose. The 2 comparators sense the positive and negative saturation value of 0.55 and 0.02 for the control output respectively, whereas the other 2 sense the polarity of error. If error is positive and the controller output has reached the saturation level of 0.55, both the outputs of top 2 comparators are 0, making the OR1 gate output zero and consequently, the output of AND 3 is zero. This results into a multiplication of 0 to the error fed to the controller and hence the integrator keeps its output at the saturation level and wind up is prevented. A similar operation is performed by the bottom 2 comparators and OR2 for negative saturation.

5.2 Simulation results

The simulation results for both negative and positive injected current Transients for boost as well as buck-boost mode are presented in this section. The operating parameters are V_{in} = 24V, V_o = 48V, L= 38.8µH, C = 76.8µF, D_{off} = 0.35. The results achieved for a negative step (1 to -1 A) variation of the reference current for tri-state boost mode are shown in Figure 5-4 (a). On the top plot, one sees the reference current (in *blue*) as well as the injected currents, into the DC bus using, the conventional dual-state (in *red*) and the tri-state (in *black*) logic. One can clearly see that the response of the latter (tri-state) is faster than of the former (conventional). The settling time also, for the former is 250 µs, while that of latter is only 62.5 µs. However, the ripple in the current injected into the DC grid with the tri-state logic seems to be higher than with the dual-state scheme. This is due to the higher ripple in the inductor current. This issue can be mitigated with an increase in the output filter capacitor.



(a)



(b)

Figure 5-4: Transient response of the output injected current as well as the inductor current for the Tri-state boost converter (a) Negative transient; (b) Positive transient

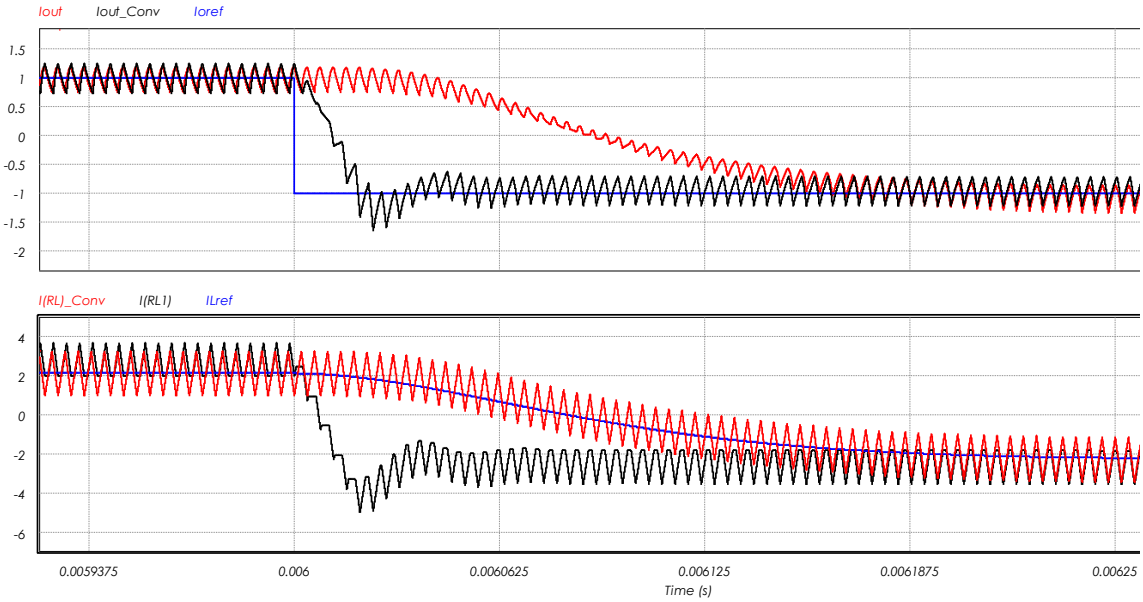
In the bottom plot, one sees the reference signal for the inner (inductor current) loop of the dual-state control scheme as well as the resulting inductor currents with the dual-state and the proposed (tri-state)

schemes. For the dual-state scheme, the inductor current follows very well the reference signal, which is however slower than the inductor current achieved with the single-loop tri-state scheme. One issue with the results obtained with the proposed scheme is that the average and RMS values of the inductor current are larger than with the conventional scheme. To a certain extent, this problem can be dealt with by using a larger value of D_{off}.

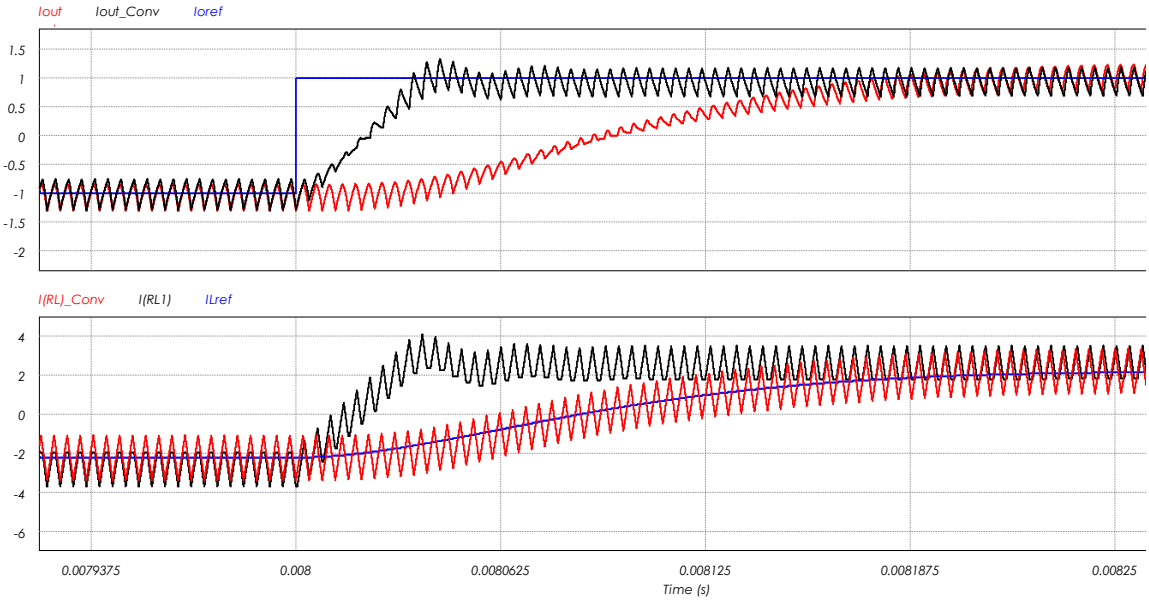
Similar results can be observed for the negative to positive current step shown in Figure 5-4(b). Here again in the top plot, the tri-state converter output reaches the set point much faster than the conventional converter, with the rise time of the former being 62.5 µs where as that of latter is 156.25 µs. In the bottom plot, the inductor current of dual-state converter follows the reference current quite accurately, but due to the presence of a slower outer voltage loop, the reference current itself rises slow, giving a slower response overall, while the tri-state inductor current, as evident, rises much faster.

One discrepancy noted here in the negative and positive transient response is that, the former has a rise time of 62.5 µs, whereas that of latter (negative) is just 32.5 µs. This is due to the fact that in steady state the value of D_{on} is 0.35, thus the dynamic range of D_f for positive transient is lower (0.35 to 0.6) than that of negative transient (0.35 to 0) resulting in relatively early saturation of the control output, and hence one doesn't see the equally fast response for the latter.

To verify the response of the buck-boost mode of operation, the same transient response was observed for it as well and the same is given in Figure 5-5. One can see that the response time of tri-state buck boost is similar to that of the tri-state boost mode of operation. The input voltage in this case is equal to 40 V (V_{in} = 40V) to allow buck-boost mode of operation. The corresponding response for a dual-state buck-boost mode of operations is presented as well for comparison purpose, where one can see that the tri-state buck-boost mode reaches the set point much faster than that of the dual-state converter i.e. in about 62.5µs for both positive and negative transient compared to 187.5µs for the dual-state. Moreover, the inductor current ripple for the tri-state is smaller than that of dual-state.



(a)



(b)

Figure 5-5: Transient response of the output injected current as well as the inductor current for the Tri-state buck-boost converter (a) Negative transient; (b) Positive transient

5.3 Simulation for prototype

Due to the limitation of the sampling frequency for the experimental prototype, it is not possible to get a control loop with a cross over frequency of 20 kHz. Hence for experimental prototype, a control loop with cross over frequency of 10 kHz is used. Moreover, for simulation of a µ-controller based system, PSIM has an inbuilt SIMCODER module as well as models of different peripherals of TMS320F28335, the same controller which is used in the experimental prototype. For illustration purpose, the implementation for boost mode of operation, case 1 is shown below.

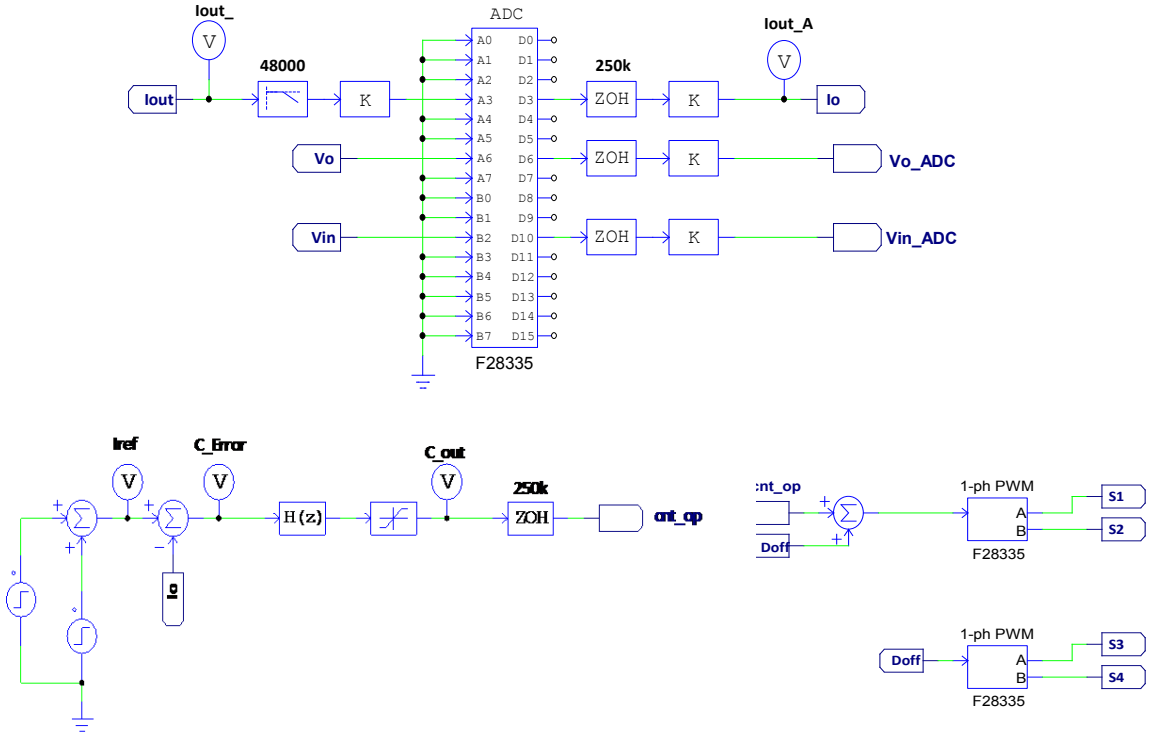
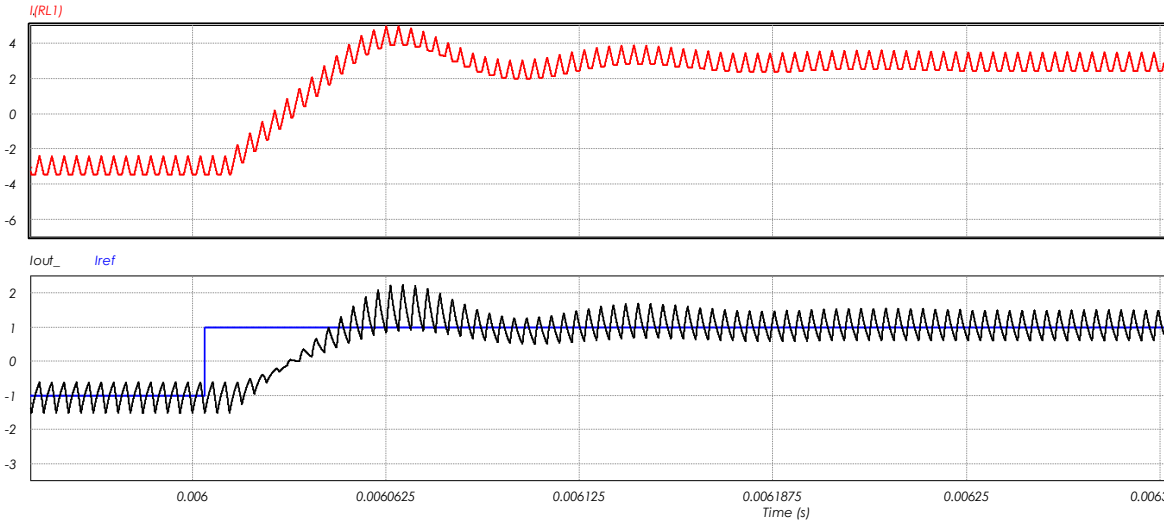


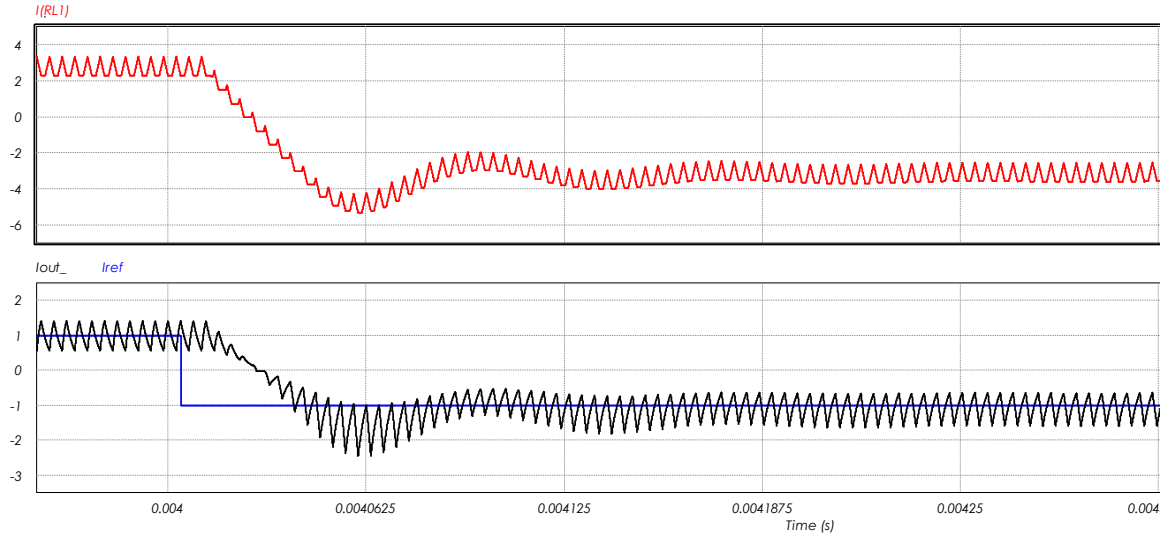
Figure 5-6: Different blocks for simulation using µ-controller: ADC, PWM and Digital control loop implementation

Here, the ADC modules are used to convert analog feedback signals into digital and then they are processed using digital IIR control loops, which is derived by s to z- domain transform of classical analog filters (PI, PI type 2 or PI type 3). The output of the digital filter is then given to the PWM modules, which

drive the switches of the converter. To check the transient response of the current control loop, positive and negative transient of 1 to -1A and vice versa is applied and the response is shown in Figure 5-7.



(a)

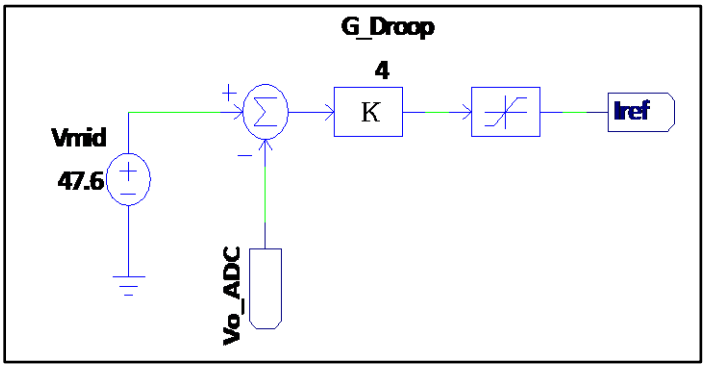


(b)

Figure 5-7: Transient response of output current loop for Experimental setup simulation with (a) Positive (b) Negative transient

The operating parameters are, V_{in} = 25V, V_{out} = 48 V, L = 38.8µH, C = 71.1µF and D_{off} = 0.35. Note that these are the component values for the experimental setup and slightly differ from the values taken for previous

analysis, based on the availability of the components. In Figure 5-7 (a), 2nd plot, the positive transient is applied at 0.006 s, and it can be seen that the output current waveform (*in black*) increases quickly with an overshoot of around 0.5A after 62.5µs, and then settles down to the I_{ref} value (*in blue*) in around 187µs. The 1st plot in Figure 5-7(a) is that of the inductor current response during the transient, which is very similar to that of the output current, with the overshoot of 1A and settling time of 187µs. Similarly, in Figure 5-7(b), a negative transient has been applied at 0.004 s, with all the operating parameters being the same. Here also, the output current (*black waveform*) reduces quickly towards the set point (*blue*) with an overshoot of -0.5A after 62.5µs and settles down to the set point in 187µs.



(a)

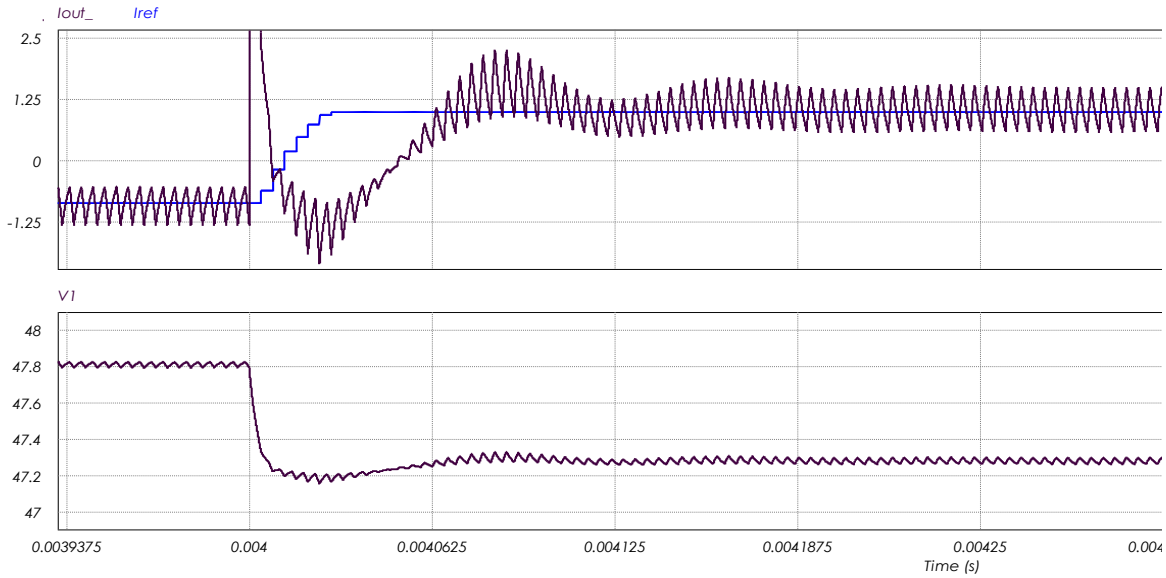


Figure 5-8: (a) Droop control implementation (b) Load transient response of the converter with droop control

Further, a droop control is implemented which measures the input voltage and generates the reference for the current control loop (Figure 5-8(a)). The parameters of the droop control are; bus parameters: R_{droop} = 0.05Ω, V_{meq} = 47.85V, for converter: $R_{droopConverter}$ = 0.25Ω, $V_{midConverter}$ = 47.6 V, $I_{UpperLimit}$ = 1A, $I_{LowerLimit}$ = -1A, the last 2 values being the maximum value of positive or negative current injected by the converter into the DC bus, even if the reference current calculated based on the difference between output voltage and the droop curve mid voltage, goes above these values. In the Figure 5-8(a), the "*G_Droop*" block is actually the inverse of the $R_{droopConverter}$, and hence is multiplied with the difference between the output voltage measured and the $V_{midConverter}$ (V_{mid} – 47.6 V in figure) to generate the reference current. Further the limiting block provides the reference current limit of -1 to 1 A.

For this mode of operation, a load transient is provided to the DC bus at 0.004 s. In Figure 5-8 the waveforms of the output current (*Black – Mid plot)*, inductor current (*Red – Top plot*), the DC bus voltage (*Black – Bottom plot*) and the resultant output current reference (*Blue – Mid plot*) has been shown for the load transient. As expected, on application of load, a high peak of the output current is observed, as it discharges the output capacitor to the lower voltage level. However, it recovers quickly with a second peak of -1.25 A and then settles down to the set point after 187µs. Also, the dip observed in the DC bus voltage (*V1 in Figure 5-8, bottom plot*) is very small and it recovers quickly to the new steady state value as the output current reaches its steady state. Thus, the objective of providing a high speed converter which would inject the required current into the DC bus in case of a transient, has been achieved.

Chapter 6 Experimental implementation

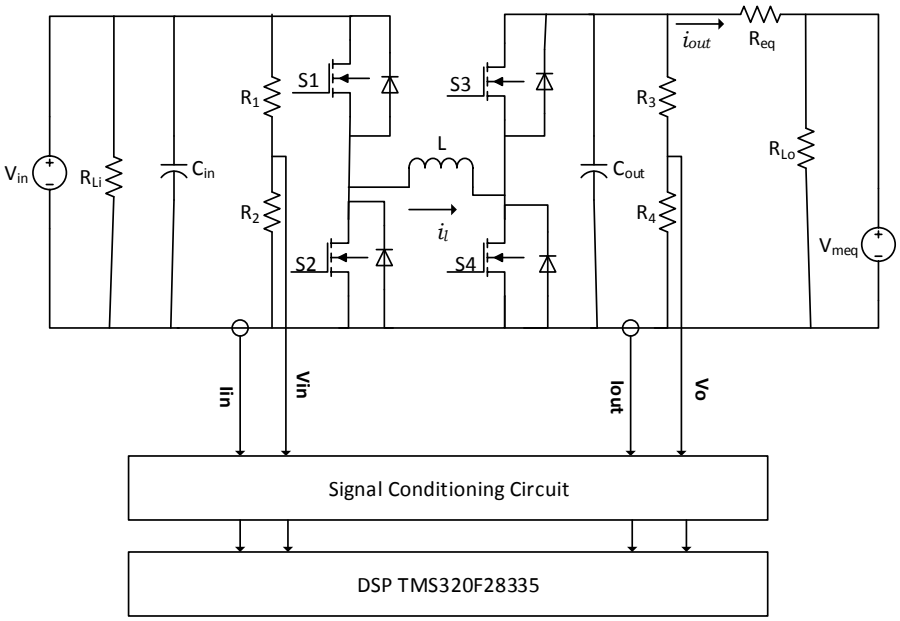
The primary goal in this work is to implement an output current control for a 4 switch bi-directional buck boost converter with a high speed of response. Further a droop control is implemented on top of this current control, similar to what is used in the interface of various sources in a DC nano-grid. In this section, first the experimental setup for obtaining the results is explained, followed by the actual results for the current control loop performance, various modes of operation, switchover condition between 2 modes of operation as well as the droop performance.

6.1 Experimental setup

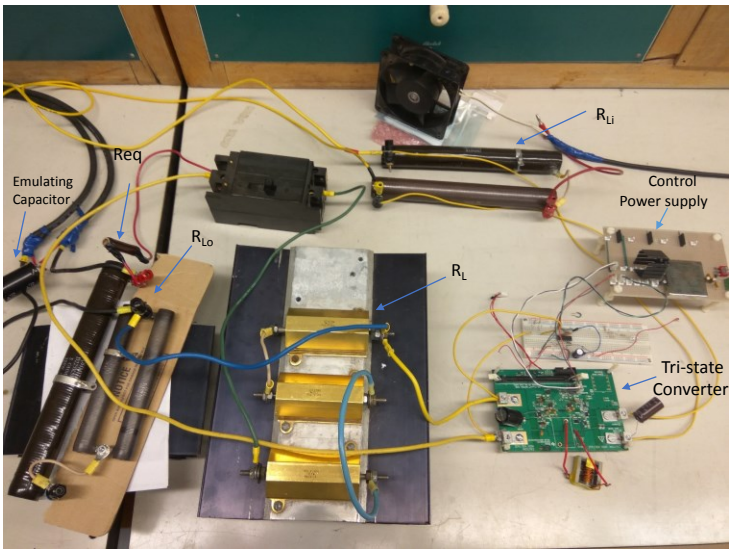
The experimental prototype of the 4 switch bi-directional converter using the tri-state logic is implemented in this work, using a "*Non-Isolated Bi-Directional Buck-Boost prototype board"* from Texas Instruments. The PCB of the board was bought and then filled in the lab. The control card for the used controller, i.e. TMS320F28335 is also from TI, and the code is developed in Code Composer Studio. The results are presented here in form of waveforms taken from a Tektronix Oscilloscope present in the PEER laboratory, Concordia University.

The schematic of the power board by TI consists of the 4-switch bi-directional topology implemented using 4 MOSFETS, the gate driver circuit as well as feedback channels for sensing input and output voltages and currents. There is a filter of 48 kHz in the output current sense channel, so as to smoothen the output current ripple and prevent noisy reading by the ADC in the controller. The output and input voltages are measured using voltage dividers followed by op-amp based voltage followers.

For the emulation of the DC bus, a DC power supply with a series resistance equal to R_{eq} is connected to the output of this board. Similarly, for supercapacitor also, a DC supply is used at the input side. Based on the direction of the output current, one of the power supplies acts as source and other as sink. To ensure that the either of the DC supplies do not have to actually sink current, a high power load (resistive) is added at both input and output, which draws an initial current from these supplies and when the converter is turned ON, the current provided from it will now drive the resistive load and simply reduce the initial current drawn from the supply. The final setup has been shown in Figure 6-1(a).



(a)



(b)

Figure 6-1: (a) The block diagram of the experimental setup (b) The snapshot of the actual experimental setup

Considering an output current reference, the speculated maximum output current to be sank by the supply, will be the sum of average current and the half of the current ripple. The design in *section 6.2*, allowed for an output current ripple of 50%, leading to a peak output current of 1.5 Ampere for a reference current of say 1 A. The initial current drawn by the load resistor in the output side should be higher than

this value to prevent negative current drawn from the supply at all times. Using equation (86) and (87) with I_{out} of 1A and output ripple of 50%, the required R_{Lo} can be calculated as 38.4Ω.

$$\widehat{I_{out}} = I_{outAvg} + \Delta I_{out}/2 \quad (86)$$

$$R_{Lo} < \frac{V_{meq}}{\widehat{I_{out}}} \quad (87)$$

For input power supply, since it is "emulating" a supercapacitor, a large capacitor is added as well at the board input. So the worst case input current will simply be the double of the output current ($V_{inMin} \approx V_o/2$), with the input current ripple being absorbed by the capacitor. Thus, using (88) required R_{Li} can be calculated as 12Ω.

$$R_{Li} < \frac{V_{inMin}}{\widehat{I_{in}}} \quad (88)$$

To ensure a safety margin, a resistance of 10Ω was connected to the output and similarly for input a resistance of 5Ω was selected. For higher input voltages this was increased to 8Ω. Also a very high value capacitor was connected across the output power supply acting as V_{meq} to emulate a very low output resistance power supply.

6.2 Experimental prototype design calculations

The components in the Texas Instruments board have been pre-designed and their values have been provided on their website. However, that is actually for a conventional converter used with PV at the input. For tri-state application, the various component's stress are calculated in this section. It can also be considered as an example of the design method for proposed tri-state system for given specifications.

Specs given

1. Max output current (I_{out}) = 1A, output current ripple = 50 %
2. Maximum output voltage ($1.1V_o$) = 48*1.1 = 52.8V
3. Minimum output voltage (0.9 V_o)= 43.2V
4. Switching frequency (f_{sw}) = 250KHz
5. Input voltage range is $V_o/2$ to V_o = 24 to 48V

6. Parameter of the DC nano-grid model i.e. R_{eq} = 0.05Ω.
7. D_{off} = 0.35, D_{fMinSS} = 0.125, $D_{onMinSS}$ = 0.125 as calculated in *section 3.4*.
8. L = 38.8µH from BOM of the board.

Parameter	Tri-state Boost		Tri-state buck-boost	
	Formula	Value	Formula	Value
V_{inMax}	$\frac{V_{oMax}}{1+\frac{D_{onMin}}{D_{off}}}$	41.76 V	Specs	48 V
V_{inMin}	Specs	24 V	$\frac{V_{oMax}}{\frac{(1-D_{fMin}-D_{off})}{D_{off}}}$	32 V
I_{L1}	$\frac{I_{out}}{D_{off}}$	2.875 A	$\frac{I_{out}}{D_{off}}$	2.875 A
ΔI_{lMax}	$\frac{V_{inMin}D_{onMax}}{Lf_{sw}}$	1.039 A	$\frac{(V_{oMax})D_{off}}{Lf_{sw}}$	1.876 A
$I_{LavgMax}$	$I_{L1}-\frac{V_{oMin}D_{off}}{2Lf_{sw}}\left[\frac{D_{onMin}}{(D_{onMin}+D_{off})}-D_{onMin}\right]$	2.725 A	$I_{L1}-\frac{V_{oMin}D_{off}}{2Lf_{sw}}(1-D_{onMin}-D_{off})$	2.466 A
$\widehat{I_L}$	$I_{L1}+\frac{\Delta I_{LMax}}{2}$	3.4 A	$I_{L1}+\frac{\Delta I_{LMax}}{2}$	3.813 A
$I_{LRMSMax}$	$\sqrt{{I_{L1}}^2+\frac{{\Delta I_{LMax}}^2}{4}D_f-I_{L1}\Delta I_{LMax}D_f}$	2.81 A	$\sqrt{{I_{L1}}^2(1-D_{fMax})+\left(I_{L1}-\frac{\Delta I_L}{2}\right)^2 D_{fmax}}$	2.428 A
C_{out}	$\frac{1-D_{off}}{Rf_{sw}}\frac{I_{out}}{\Delta I_{out}}$	83.2 µF	$\frac{1-D_{off}}{Rf_{sw}}\frac{I_{out}}{\Delta I_{out}}$	83.2µF
I_{CRMS}	$\sqrt{{I_{out}}^2\frac{(1-D_{off})}{D_{off}}+\frac{{\Delta I_{LMax}}^2}{12}D_{off}}$	1.89 A	$\sqrt{{I_{out}}^2\frac{(1-D_{off})}{D_{off}}+\frac{{\Delta I_{LMax}}^2}{12}D_{off}}$	2.15 A
V_{Cout}	1.1 V_o	52 V	1.1 V_o	52 V
I_{s1rms}[1]	$\sqrt{({I_{L1}}^2+\frac{{\Delta I_L}^2}{12})(D_{onMax}+D_{off})}$	2.704 A	$\sqrt{\left({I_{L1}}^2+\frac{{\Delta I_L}^2}{12}\right)D_{onMax}}$	2.09 A
${I_{s2rms}}^1$	$\left(I_{L1}-\frac{\Delta I_L}{2}\right)\sqrt{[1-(D_{onMin}+D_{off})]}$	1.86 A	$\sqrt{\left({I_{L1}}^2+\frac{{\Delta I_L}^2}{12}\right)D_{off}+\left[\left(I_{L1}-\frac{\Delta I_L}{2}\right)^2 D_{fMax}\right.}$	2.227 A
${I_{s3rms}}^1$	$\sqrt{\left({I_{L1}}^2+\frac{{\Delta I_{LMax}}^2}{12}\right)D_{off}}$	1.71 A	$\sqrt{\left({I_{L1}}^2+\frac{{\Delta I_{LMax}}^2}{12}\right)D_{off}}$	1.73 A
${I_{s4rms}}^1$	$\sqrt{\left({I_{L1}}^2+\frac{{\Delta I_L}^2}{12}\right)D_{onMin}+\left[\left(I_{L1}-\frac{\Delta I_L}{2}\right)^2 D_f\right]}$	2.143 A	$\sqrt{\left({I_{L1}}^2+\frac{{\Delta I_L}^2}{12}\right)D_{onMAx}+\left[\left(I_{L1}-\frac{\Delta I_L}{2}\right)^2 D_f\right]}$	2.13 A
$\widehat{I_{sw}}$	$\widehat{I_L}$	3.4 A	$\widehat{I_L}$	3.4 A
$\widehat{V_{sw}}$	1.1 V_o	52 V	1.1 V_o	52 V

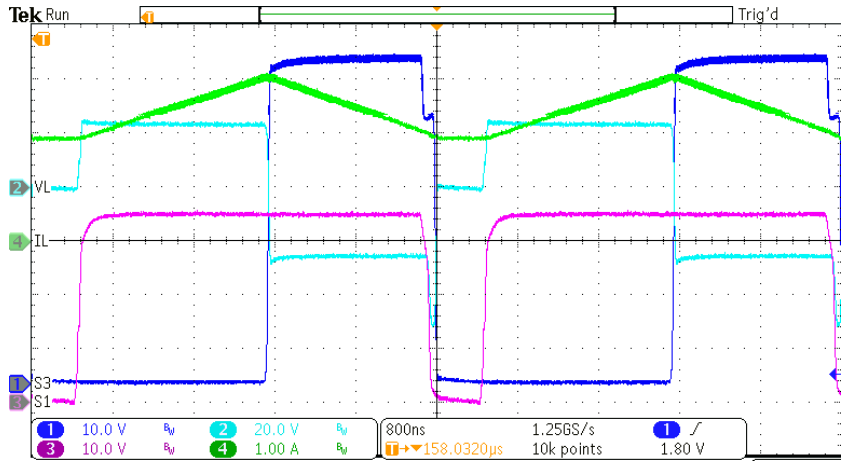
[1] The values of all other parameters are at respective D_{onMax}/ D_{onMin}

Table 5: Calculation of various parameters for both mode of operation

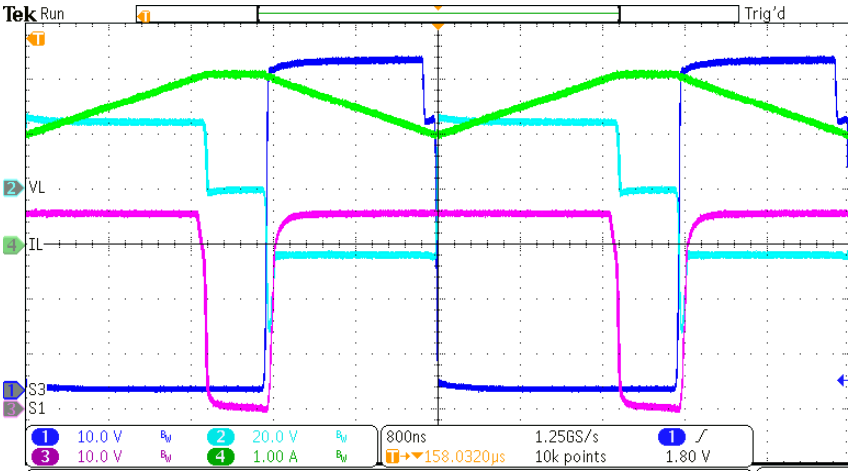
In Table 5, the worst case parameters for both modes of operation are given, and the final device selection should be based on the value which is higher of the 2 modes. For instance the inductor ripple current for the buck-boost mode is higher than that in boost mode, hence worst case ripple considered should be that of the buck-boost mode whereas, the worst average inductor current is higher in boost mode and hence the same should be considered for inductor design.

6.3 Experimental results

6.3.1 Tri-state boost mode of operation and 2 switching schemes



(a)



(b)

Figure 6-2: Inductor current and voltage waveforms for Tri-state boost mode of operation for positive injected current of 1A with: (a) switching sequence #1 (b) switching sequence #2.
Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): inductor voltage, *Ch1* (*Royal-Blue*): Gate of S3 w.r.t DC bus Gnd and *Ch3* (*pink*): Gate of S1 w.r.t DC bus Gnd

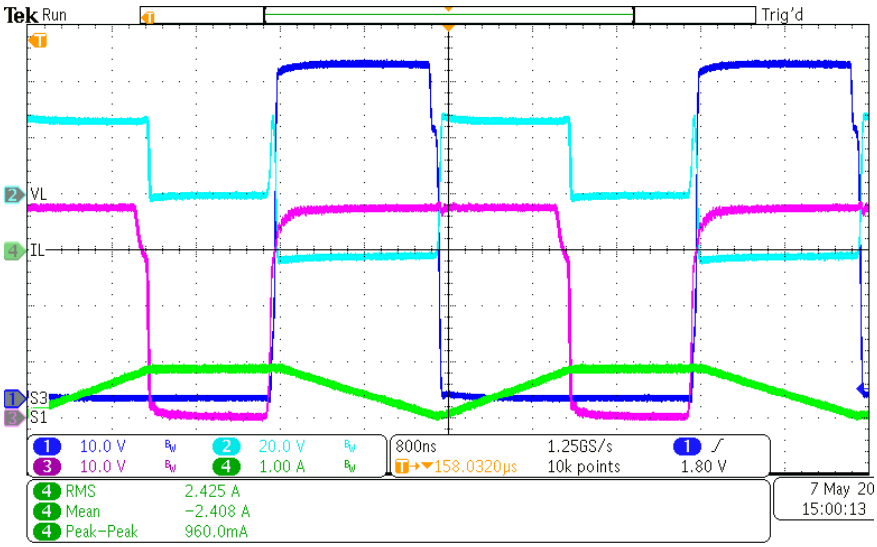
It should be noted that, the Gate waveforms of Switch 1 and Switch 3 are measured here with respect to DC bus ground and hence the corresponding waveforms are a summation of the Emitter voltage of the upper switch in the respective half bridge w.r.t. DC bus ground and the gate voltage at any instant.

In *section 3.2.1*, the 2 switching schemes of the tri-state boost mode of operation have been analyzed and it was proved that one switching scheme is better than the other in terms of lower RMS currents for different switches as well as inductor current. In the setup shown above, it can be seen that it is not possible to measure the current in the switches as they have been soldered on the PCB itself. However, it is possible to observe the inductor current and measure its average and RMS value. In Figure 6-2**,** the inductor current and inductor voltage waveforms for the 2 switching schemes of the tri-state boost mode of operation are presented for positive injected current. It can be seen that in both waveforms, the ripple current as well as the peak current of the inductor is the same, however the RMS and average current of sequence 1 is lower than that of sequence 2. Also, the operating parameters of these waveforms are the same as that of the simulation results presented in Figure 3-3, in *section 3.2.1 i.e.* V_o = 48V, Vin = 24 V, L= 38.8µH, D_{off} = 0.4., and it can be seen that the inductor current waveforms for the simulation results match those of the experimental (Table 6), thus verifying the analysis.

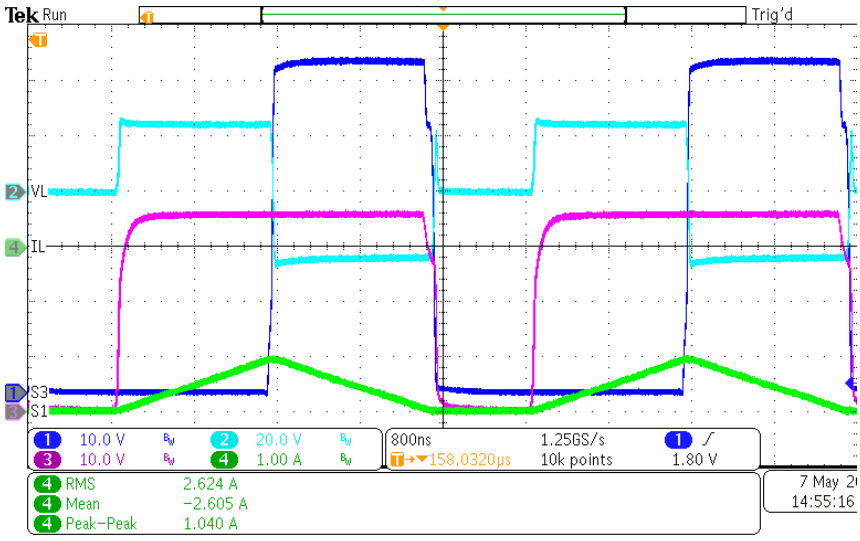
Sequence	Type of result	I_{LAvg} (A)	I_{LRMS} (A)	Δ I_L (A)	I_{Lpeak} (A)
Case 1	Simulation	2.428	2.42	1	3
	Experimental	2.419	2.446	1.2	3
Case 2	Simulation	2.618	2.638	1	3
	Experimental	2.62	2.64	1	3

Table 6: Comparison of simulation and experimental results for 2 cases of operation in tri-state boost mode.

Further, for negative injected current, the 2 sequences are presented in Figure 6-3.



(a)



(b)

Figure 6-3: Inductor current and voltage waveforms for Tri-state boost mode of operation for negative injected current of 1A with: (a) switching sequence #1 (b) switching sequence #2

Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): inductor voltage, *Ch1* (*Royal-Blue*): Gate of S1 w.r.t DC bus Gnd and *Ch3* (*pink*): Gate of S3 w.r.t DC bus Gnd

The average and RMS current values for sequence 1 were measured to be -2.6 A and 2.624 A respectively, whereas that of sequence 2 was measured to be -2.41 A and 2.425 A. Thus the average and RMS inductor current value for sequence 2 is smaller than those of sequence 1.

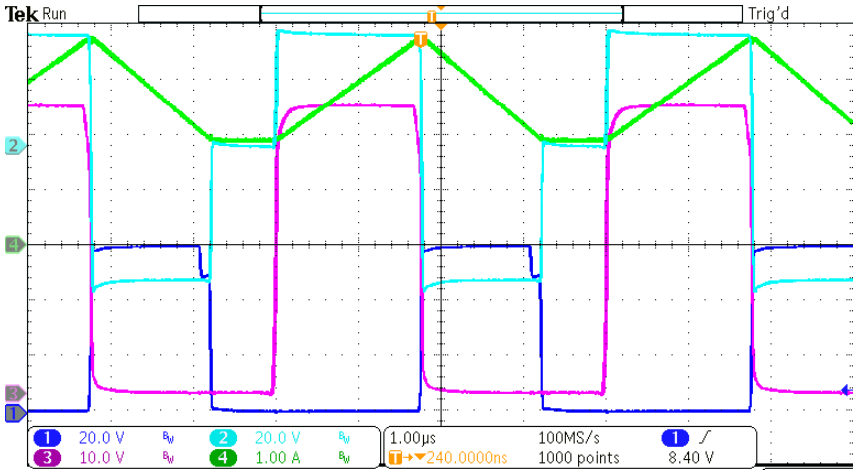
From the analysis above, it can be seen that the experimental results also verify the fact that sequence 1 is better than 2 for positive power flow and vice-versa.

6.3.2 Tri-state buck - boost mode of operation and the 2 switching schemes

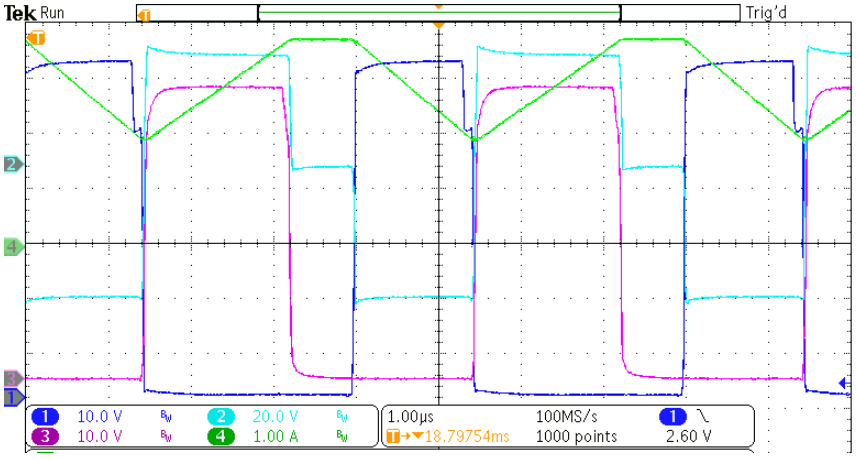
Similar to the tri-state boost, in *section 3.3.2*, the 2 switching schemes of the tri-state buck-boost mode of operation are also analyzed and it can be seen that one switching scheme is better than the other in terms of lower RMS currents for different switches as well as inductor current. In Figure 6-4, the inductor current and inductor voltage waveform for 2 switching schemes of tri-state buck-boost mode of operation are presented. It can be seen that in both waveforms, the ripple current as well as the peak current of the inductor are the same. However the RMS and average current of *Case 1* is lower than that of *Case 2*. Also, the operating parameters of these waveforms are the same as that of the simulation results presented in Figure 3-12, in *section 3.2.1 i.e.* V_o = 48V, V_{in} = 40 V, L= 38.8µH, D_{off} = 0.35., and it can be seen that the inductor current waveforms for the simulation results match with those of the experimental, thus verifying the analysis. The inductor current ripple, peak, RMS and average values measured from simulation (Figure 3-12) and experimental are compared in Table 7, and it can be seen that they are in good agreement with each other.

Sequence	Type of result	I_{LAvg} (A)	I_{LRMS} (A)	Δ I_L (A)	I_{Lpeak} (A)
Case 1	Simulation	2.644	2.70	1.73	3.7
	Experimental	2.74	2.8	1.86	3.72
Case 2	Simulation	3.034	3.08	1.73	3.7
	Experimental	2.948	3.01	1.87	3.65

Table 7: Comparison of simulation and Experimental results for 2 cases of operation in tri-state buck-boost mode.



(a)



(b)

Figure 6-4: Inductor current and voltage waveforms for Tri-state buck-boost mode of operation for positive injected current of 1A with: (a) switching sequence #1 (b) switching sequence #2.

Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): inductor voltage, *Ch1* (*Royal-Blue*): Gate of S3 w.r.t. DC bus Gnd and *Ch3* (*pink*): Gate of S1 w.r.t. DC bus Gnd

Further, for negative injected current the 2 sequences are presented in Figure 6-5.

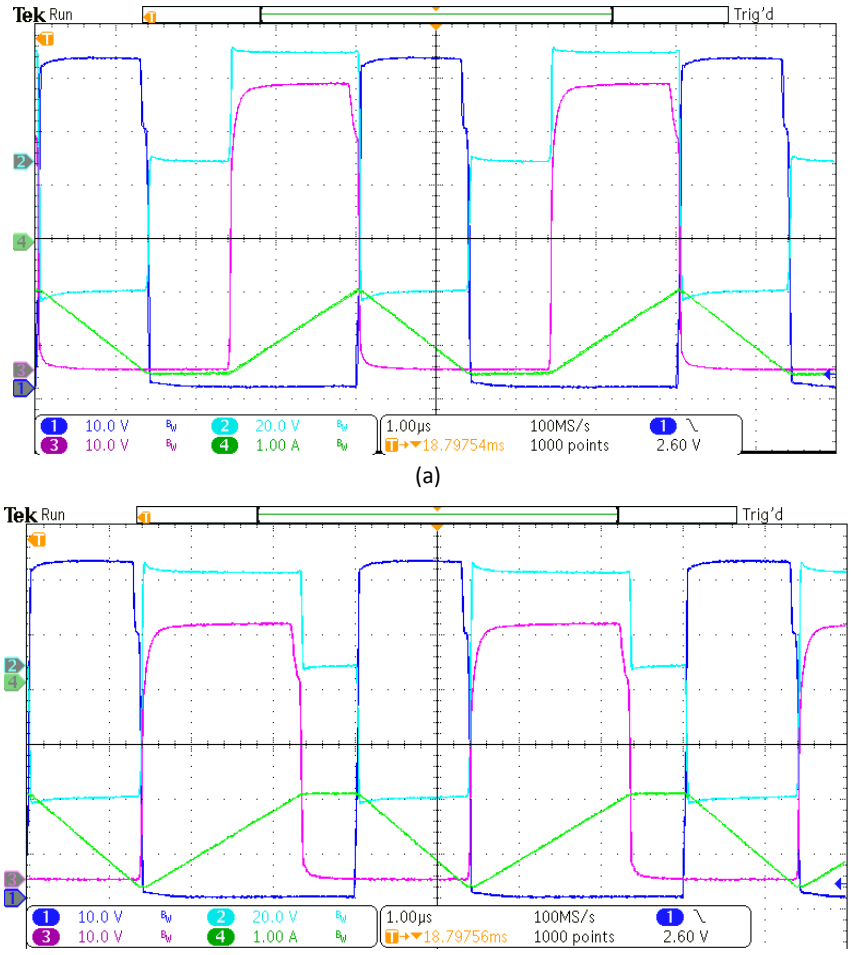


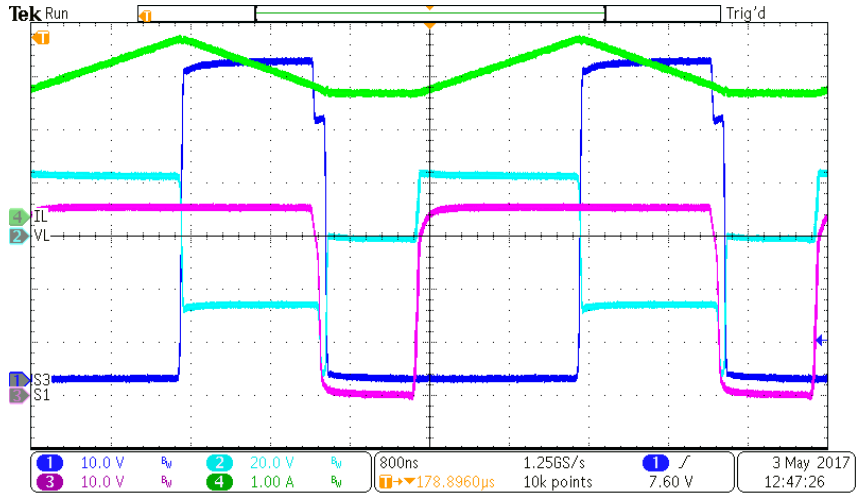
Figure 6-5: Inductor current and voltage waveforms for Tri-state buck-boost mode of operation for negative injected current of 1A with: (a) switching sequence #1 (b) switching sequence #2.

Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): inductor voltage, *Ch1* (*Royal-Blue*): Gate of S3 w.r.t DC bus Gnd and *Ch3* (*pink*): Gate of S1 w.r.t DC bus Gnd

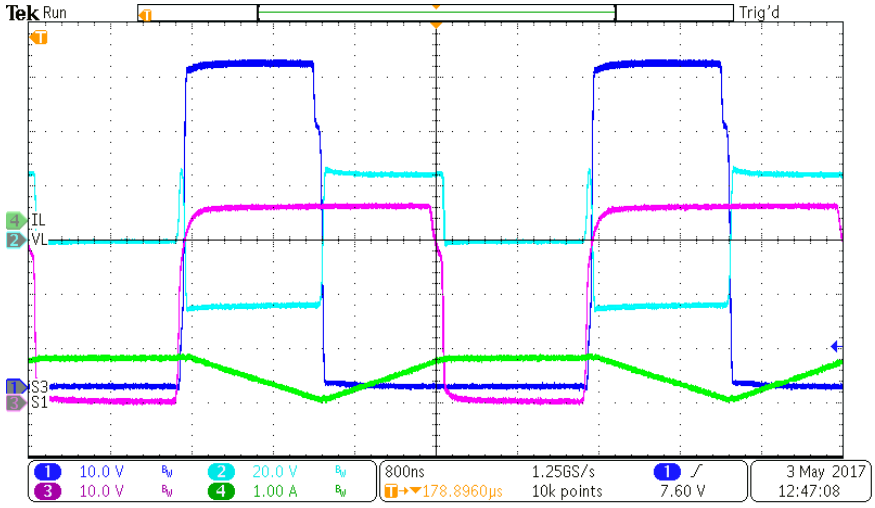
The average and RMS currents for sequence 1 were measured to be -3.015 A and 3.02 A respectively, whereas that of sequence 2 was measured to be -2.816 A and 2.873 A. Thus the average and RMS inductor current for sequence 2 is smaller than that of sequence 1. From the analysis above, it can be seen that the experimental results also verify the fact that sequence 1 is better than 2 for positive power flow and vice-versa.

6.3.3 Various modes of operation

In this section, the results for various mode of operation are presented in terms of waveforms of gate signals, inductor current and inductor voltage.



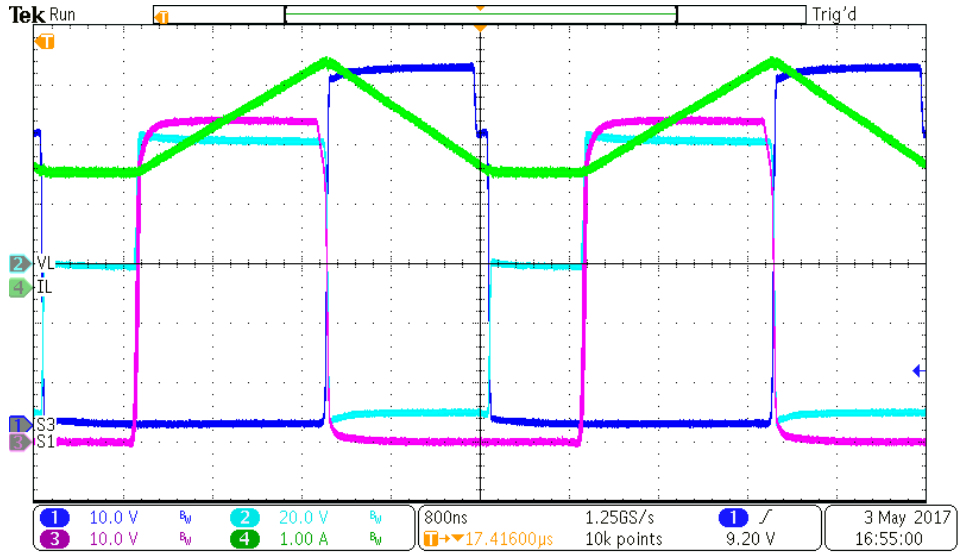
(a)



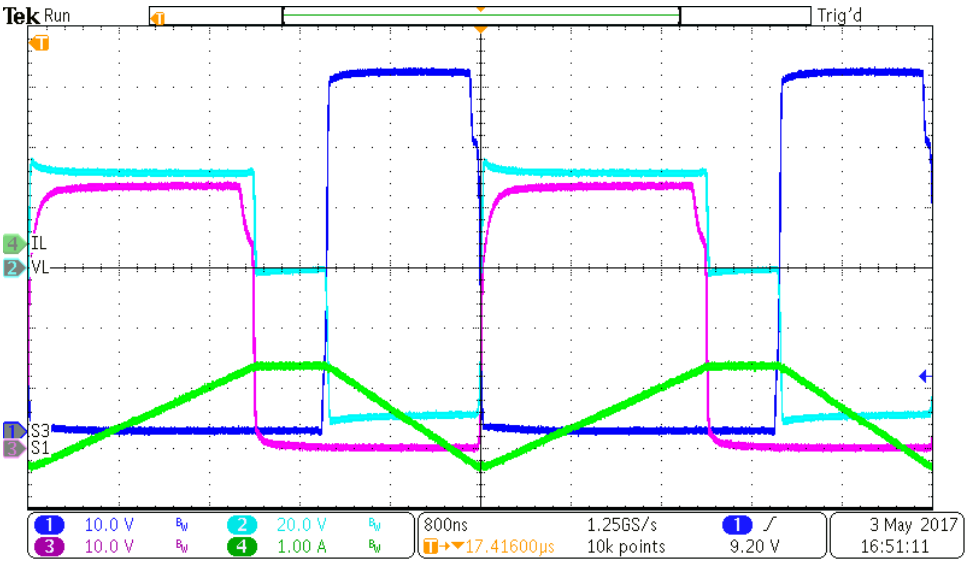
(b)

Figure 6-6: Tri-state boost mode of operation (a) Waveforms for injected current of 1A (b) Waveforms for injected current of -1A

Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): inductor voltage, *Ch1* (*Royal-Blue*): Gate of S3 w.r.t DC bus Gnd and *Ch3* (*pink*): Gate of S1 w.r.t DC bus Gnd



(a)



(b)

Figure 6-7: Tri-state buck-boost mode of operation (a) Waveforms for injected current of 1A, V_{in} = 40V (b) Waveforms for injected current of -1A, V_{in} = 32V. The channels represent same quantities as in Figure 6-5.

The results for operation with tri-state boost mode for the 2 cases are presented in Figure 6-6. For tri-state boost mode, the inductor voltage is equal to the input voltage i.e. 24 V for D_{on}, difference between the input and output voltages i.e. -24 V (24-48 =-24), for D_{off}, and zero for D_f.

Similarly, the 2 sequences of operation for the buck-boost mode of operation are shown in Figure 6-7. The buck-boost mode of operation is selected when input voltage is "high", hence in Figure 6-7, for positive injected current and negative injected current waveforms the input voltage is 32 V and 40 V respectively. Please note that the D_{off} value is 0.35 V for both modes of operation. In Figure 6-7(a), as expected for buck-boost mode of operation, the inductor voltage is equal to the input voltage i.e. 32 V for D_{on}, output voltages i.e. -48 V, for D_{off}, and zero for D_f. The sequence changes from D_f, D_{on} and D_{off} to D_{on}, D_f and D_{off} for positive and negative output current respectively. Also, as expected the ripple in the inductor current is higher in the buck-boost mode compared to that of the boost mode.

One of the dissimilarities observed in the experimental results and simulation results is, the presence of a spike in the inductor voltage at either ends of the D_f based on the direction of the current in Figure 6-6, i.e. in the tri-state buck boost mode of operation. This is result of the dead time implemented in the PWM waveforms for the 2 half-bridges and is explained in the next section.

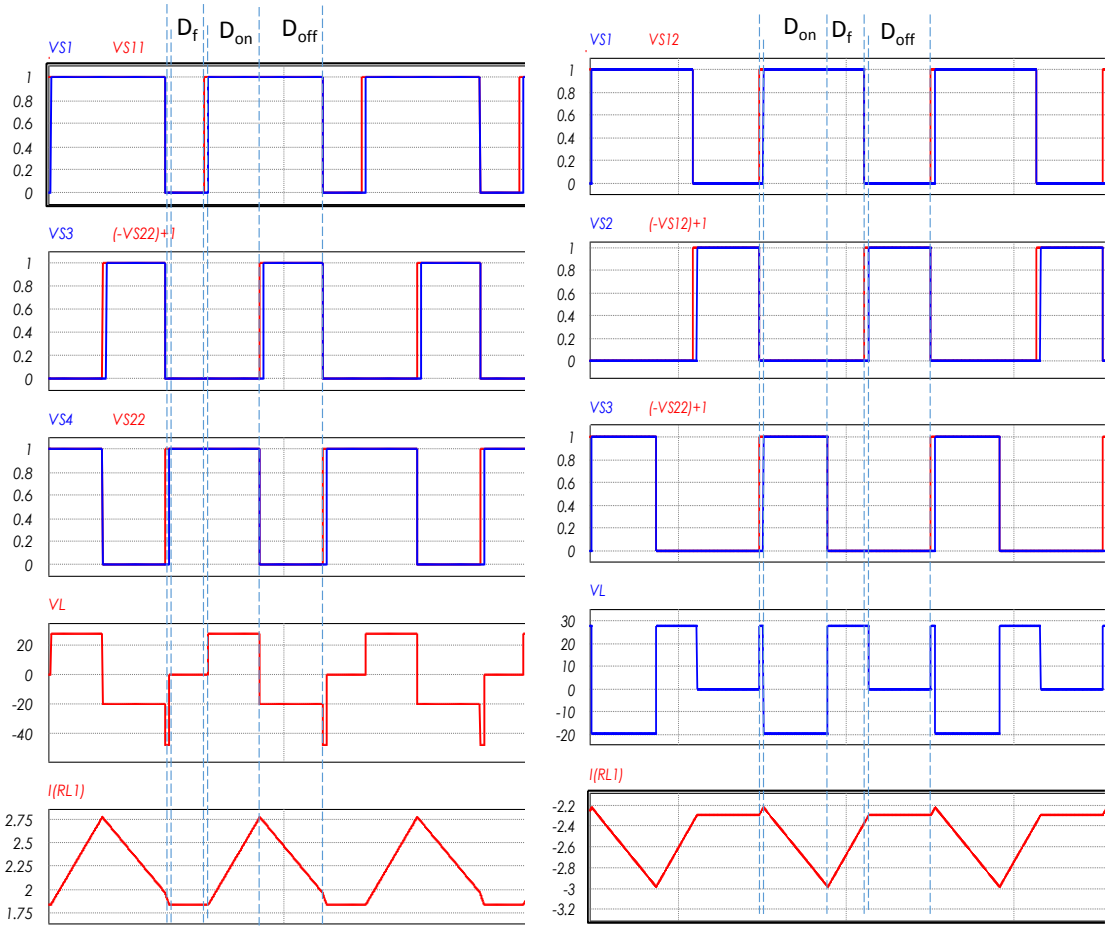
6.3.4 Effect of dead time on the switching waveforms and gain of the converter

The 4-switch bi-directional converter topology basically consists of 2 half- bridges, connected to the input and output buses. The switches in every bridge operate by complementing each other to prevent the short-circuit of the corresponding bus and resulting damage to the switches. To ensure that this shoot through condition never occurs, a dead time is added in the switching waveforms, which is essentially the delay between Switch ON of next switch after switch OFF of the 1st one.

The aim here is to observe the way in which the steady state value of D_{on} for given input & output conditions differs from its ideal value after considering the effect of dead time on the inductor voltage waveforms. As far as transient response is concerned, the dead time is a constant value, so its addition or subtraction should not change the transfer function. Also, since this is not an A.C. waveform, there is no issue of waveform distortion and, the main concern here is that the converter should be able to get the required voltage gain, and consequently achieve the injected current set point.

For analysis purpose, the waveforms for the converter operation in the tri-state boost mode are presented in Figure 6-8**.** The top plot is that of the Gate signal applied to S1 (Red – without dead time, Blue- with

dead time),the 2nd plot is that of S3, the 3rdplot is that of S4, the 4th plot shows voltage across inductor and 5th is the inductor current. Other Parameters are,V_{in} = 28V, V_o = 48V, I_{out} = 1A for (a) and -1A for (b), dead-time = 0.1µs.



(a) (b)

Figure 6-8: Dead time illustration for Tri-state boost mode of operation (a) Positive Current (b) Negative Current

For positive currents, it is evident that, due to the effect of the dead time, the effective value of D_{on} reduces, as the point of transition of inductor voltage from 0 to V_{in} takes place at the 2nd dotted line instead of the 1st. The D_{off} period stays as it is, whereas the D_f period shifts while retaining its length. Between D_{off} and D_f, during the dead time associated with S4 of 2nd Bridge, the inductor voltage is observed to have a spike equal to $-V_o$. This is because, during this region, S1 is off & S2/D2 is ON in the 1st bridge, whereas S3

and S4 are both OFF in the 2nd, forcing D3 to turn on and provide path to positive inductor current, making the inductor voltage equal to V_o. Recall that this segment was not present in the ideal waveforms, instead it has appeared due to the effect of dead time, and needs to be accounted for, while calculating the practical steady state D_{on} value for a given input output conditions.

For calculating the converter steady state gain equation for this switching scheme, recall that the average inductor voltage is zero in steady state. The dead time is represented here in form of a duty cycle for mathematical analysis.

$$V_{Lavg} = 0 \quad => (D_{on} - D_{d.t.})V_{in} + D_{off}(V_{in} - V_o) + D_{d.t.}(-V_o) + D_f(0) = 0$$

$$(D_{on} - D_{d.t.})V_{in} + D_{off}(V_{in}) = D_{off}(V_o) + D_{d.t.}(V_o)$$

$$\left(D_{on} - D_{d.t.} + D_{off}\right)V_{in} = \left(D_{off} + D_{d.t.}\right)(V_o)$$

$$Gain = \frac{V_o}{V_{in}} = \frac{(D_{on} - D_{d.t.} + D_{off})}{(D_{off} + D_{d.t.})} = \left[1 + \frac{(D_{on} - 2D_{d.t.})}{(D_{off} + D_{d.t.})}\right] \quad (88)$$

Also, for a given voltage Gain, D_{on} can be calculated as,

$$D_{on} = \left[(Gain - 1)\left(D_{off} + D_{d.t.}\right)\right] + 2D_{d.t.} \quad (89)$$

Recall that for ideal conditions, the formula of D_{on}, for a given voltage gain is given by,

$$D_{on} = (Gain - 1)D_{off} \quad (90)$$

From these 2 equations one can see that the required D_{on} value to achieve the same voltage gain increases due the effect of the dead time. This implies that for a given D_{on} max value, the achievable gain reduces, which in turn would result into a higher "minimum allowable voltage for supercapacitor" compared to the ideal case when dead time was not considered.

Similarly for the negative output current scenario different waveforms are given in the Figure 6-8(b).

Recall that for negative current, the 2nd switching sequence has to be used, to ensure that one freewheels current with minimum absolute value. From Figure6-8(b), one can see that, the effective D_{on} increases

whereas the values of D_f and D_{off} reduce. Further, the spike is observed during the dead time of 1st half bridge and is equal to V_{in}, a phenomenon similar to the one for the positive current analysis, the difference being that the negative inductor current will find a path through D1 and D4 diodes in this case, resulting in the inductor voltage being equal to input voltage.

For calculating the converter steady state gain equation for this switching waveform, the average inductor voltage can again be considered zero.

$$V_{Lavg} = 0 \quad => (D_{on} + D_{d.t.})V_{in} + \left(D_{off} - D_{d.t.}\right)(V_{in} - V_o) + D_{d.t.}(V_{in}) = 0$$

$$(D_{on} + 2D_{d.t.})V_{in} + \left(D_{off} - D_{d.t.}\right)(V_{in}) = \left(D_{off} - D_{d.t.}\right)(V_o)$$

$$\left(D_{on} + 2D_{d.t.} + D_{off} - D_{d.t.}\right)V_{in} = \left(D_{off} - D_{d.t.}\right)(V_o)$$

$$Gain = \frac{V_o}{V_{in}} = \frac{\left(D_{on}+2D_{d.t.}+D_{off}-D_{d.t.}\right)}{\left(D_{off}-D_{d.t.}\right)} = \left[1 + \frac{\left(D_{on}+2D_{d.t.}\right)}{\left(D_{off}-D_{d.t.}\right)}\right] \quad (91)$$

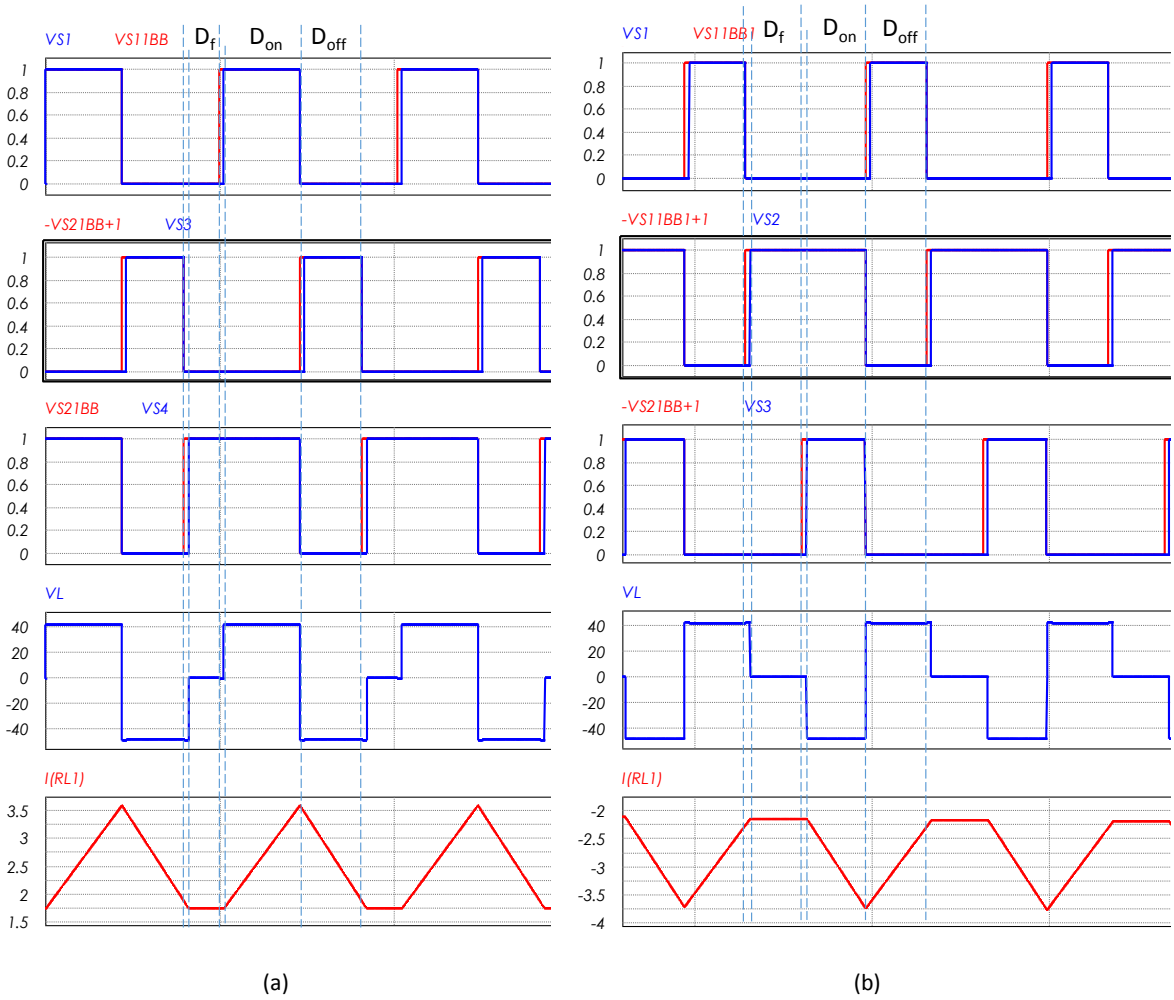
Also, for a given voltage gain, D_{on} can be calculated as,

$$D_{on} = (Gain - 1)\left(D_{off} - D_{d.t.}\right) - 2D_{d.t.} \quad (92)$$

From the equations, one can see that the required D_{on} value to achieve the same voltage gain decreases due the effect of the dead time. This implies that for a given D_{on} max value, the minimum achievable gain increases, which in turn would mean that now the maximum possible voltage of the supercapacitor which can be interfaced without losing control, has decreased from the previous ideal definition.

So to summarize, due to the effect of the dead time the actual operating voltage range of the supercapacitor voltage, reduces from both the maximum and minimum sides.

For buck-boost mode of operation also, a similar analysis regarding the effect of dead time has to be considered. For this purpose, the waveforms at the steady state for an output current of 1A and -1A are showcased in the Figure 6-9. Here again the gate signal applied with deadtime is in *Blue* and without deadtime (ideal) is in *Red*. Other Parameters are, V_{in} = 42V, V_o = 48V, I_{out} = 1A/ -1A, dead-time = 0.1µs.



(a) (b)

Figure 6-9: Dead time illustration for tri-state buck-boost mode of operation (a) Positive Current (b) Negative Current

From the figure one can see that, the value of D_{on} reduces by a time period equal to the dead time, while the value of D_{off} increases by the same amount. The freewheeling period D_f simply shifts while retaining its actual length. To decide the steady state D_{on} for this waveform, recall that the average value of inductor voltage is zero in steady state.

$$V_{Lavg} = 0 \quad => (D_{on} - D_{d.t.})V_{in} + (D_{off} + D_{d.t.})(-V_o) = 0$$

On simplifying this equation,

$$Gain = \frac{V_o}{V_{in}} = \frac{(D_{on} - D_{d.t.})}{(D_{off} + D_{d.t.})} \quad (93)$$

Also, for a given voltage gain, D_{on} can be calculated as,

$$D_{on} = Gain(D_{off} + D_{d.t.}) + D_{d.t.} \quad (94)$$

Recall that for ideal case, the similar formula for D_{on} would be,

$$D_{on} = Gain\ D_{off} \quad (95)$$

As seen from the 2 equations, similar to the boost case, in buck-boost also, the required D_{on} for a given value of gain while maintaining positive output current, is found to be higher than the ideal value, which in turn would increase the minimum allowable voltage of supercapacitor which can be interfaced.

Similar analysis for negative current would yield the derivation given below.

$$V_{Lavg} = 0 \quad => (D_{on} + D_{d.t.})V_{in} + (D_{off} - D_{d.t.})(-V_o) = 0$$

$$Gain = \frac{V_o}{V_{in}} = \frac{(D_{on} + D_{d.t.})}{(D_{off} - D_{d.t.})} \quad (96)$$

Also, for a given voltage gain, D_{on} can be calculated as,

$$D_{on} = Gain(D_{off} - D_{d.t.}) - D_{d.t.} \quad (97)$$

Here again one can see that, the required D_{on} value required to achieve the same voltage gain decreases due the effect of the dead time, which in turn would mean that now the maximum possible voltage of supercapacitor which can be interfaced without losing control, has decreased from the previous ideal definition. So to summarize, due to effect of the dead time the actual operating voltage range of the supercapacitor voltage, reduces from both the maximum and minimum side in buck-boost mode as well.

To further support this theoretical analysis, experimental results are presented here, where the value of D_{on} for both modes of operation as well as both power flow directions, are recorded. The dead time in both waveforms can be seen to be around 80 ns which is the same as what has been defined in the PWM module of the µ-controller. This is used to calculate the value of 'D_{on} with dead time considered' in the Table 8 & 9, using equation (89) & (94) for positive currents and equation (92) & (97) for negative currents. The 'Ideal D_{on}' is calculated using the equations for D_{on} before considering the dead time, equation (90) for boost and equation (95) for buck-boost. The 'D_{on} measured from experiment' are the average D_{on} values obtained from the µ-controller in real time, for given input and output conditions.

From Table 8 and 9, one can see that the values of D_{on} calculated with dead time using equations derived in this section, and those obtained from the experimental results are very close to each other, thus validating the theoretical analysis. As expected, both these values are always higher than the ideal ones for positive current and lower for negative current. Consequently, for positive output current operation (Table 8), at input voltage of 40 V, the value of D_{on} has reached 0.1, which is too low, and one needs to switchover to buck-boost mode of operation. The values of the buck-boost mode of operation around this input voltage are given as well, and it can be seen that there is an overlap in the 2 and this can be used to implement hysteresis.

Output current = 1 A					
V_{in}	V_{out}	Ideal D_{on}	D_{on} with dead time considered	D_{on} measured from experiment	Mode of operation
24	48	0.35	0.41	0.4056	Boost
24	52	0.408	0.472	0.46817	Boost
38	48	0.092	0.1374	0.1311	Boost
39	48	0.0801	0.1254	0.1186	Boost
40	48	0.07	0.114	0.1072	Boost
38	48	0.4421	0.487368	0.478	Buck- Boost
39	48	0.431	0.475385	0.467	Buck- Boost
40	48	0.42	0.464	0.4563	Buck- Boost
41	48	0.409	0.453171	0.445	Buck- Boost
47	48	0.357	0.397872	0.3909	Buck- Boost
47	43.2	0.322	0.36	0.347	Buck- Boost
47	52	0.387234	0.429362	0.4148	Buck- Boost

Table 8: Comparison of theoretical and experimental steady state values of D_{on} for variation in input voltages for positive output current

Output current = -1 A					
V_{in}	V_{out}	Ideal D_{on}	D_{on} with Dead time considered	D_{on} measured from experiment	Mode of operation
24	48	0.35	0.29	0.302	Boost
24	52	0.408	0.345	0.35868	Boost
30	48	0.21	0.158	0.1711	Boost
31	48	0.1442	0.140967742	0.1533	Boost
32	48	0.092	0.125	0.134	Boost
33	48	0.0801	0.11	0.102	Boost
31	48	0.431	0.490967742	0.5110	Buck- Boost
32	48	0.42	0.475	0.4988	Buck- Boost
33	48	0.409	0.46	0.477	Buck- Boost
34	48	0.494	0.446	0.4655	Buck- Boost
47	48	0.357	0.397872	0.3909	Buck- Boost
47	43.2	0.321702	0.283	0.3068	Buck- Boost
47	52	0.387234	0.345106383	0.368	Buck- Boost

Table 9: Comparison of theoretical and experimental steady state values of D_{on} for variation in input voltages with negative output current

Similarly in Table 9**,** the experimental values are always higher than the ideal one, for negative values of the output current. At input voltage of 33 V, the D_{on} has reached 0.102, which is too low, and one needs to switchover to buck-boost mode of operation. The values of the buck-boost mode of operation around this input voltage are given as well, and it can be seen that there is an overlap in 2 and this can be used to implement hysteresis.

6.3.5 Switch over of controller between 2 modes of operation

In the last section, it was shown that the converter has to switch from boost to buck-boost mode of operation when the required gain reduces, and due to the effect of the dead time, the point of switchover is different for different directions of power flow. Another aspect of this is the transition of the controller form one mode to the other during the switchover. In *section 4.4*, a switchover strategy for the control loop was discussed, where in it was proposed that, in the boost mode the output of the controller will be treated as D_{on} + D_{off}, whereas in buck-boost mode it would be treated as just D_{on}; what would lead to the same steady state output for both modes for a given input-output condition, and hence smoother transition.

To validate this further, an experimental analysis was done wherein, in the 1st case, the control loop output was treated as D_{on}, and the switch over response was recorded, and in the 2nd case, the results for switchover for the proposed strategy were recorded. The results are presented in Figure 6-10 and Figure 6-11 for both types of transition, i.e. boost to buck-boost and buck-boost to boost.

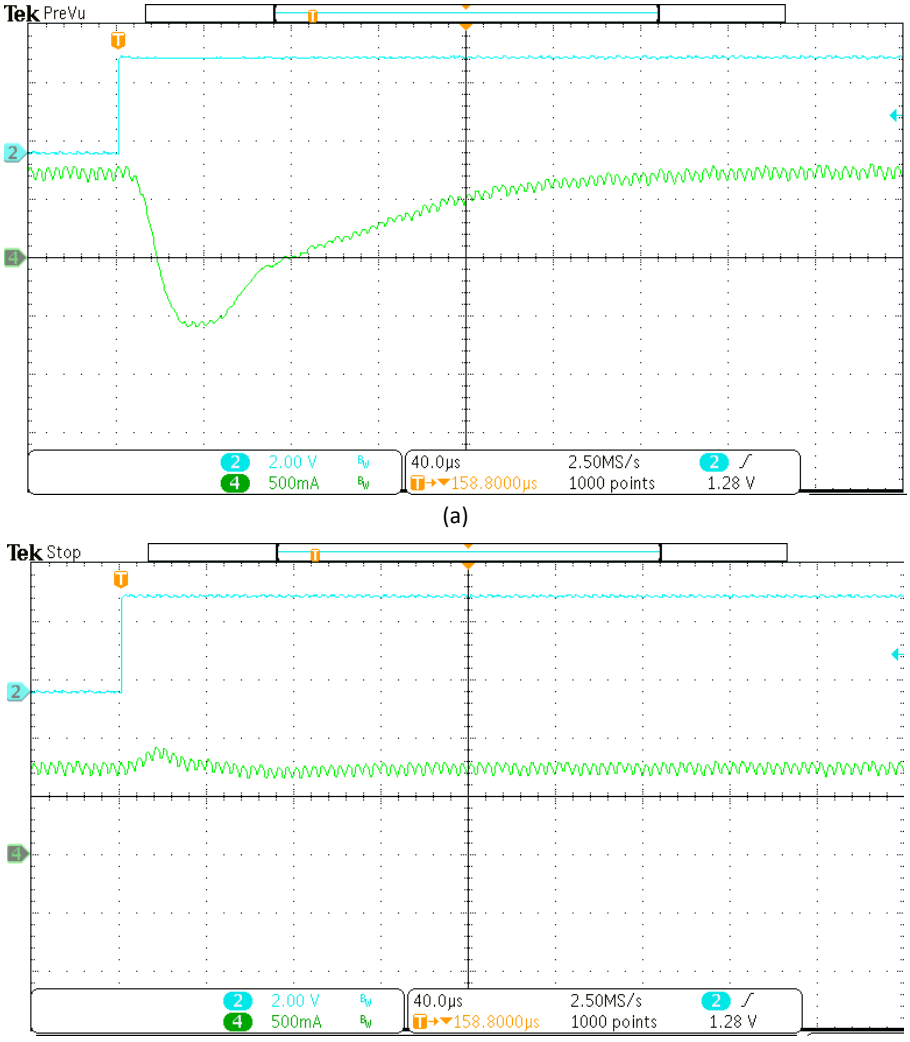


Figure 6-10: Illustration of switch over response of boost to buck- boost (a) General control strategy (b) Proposed control strategy

Ch4 (*green*): Output current, *Ch2* (*Sky-Blue*): Mode of operation 1: buck-boost and 0: boost

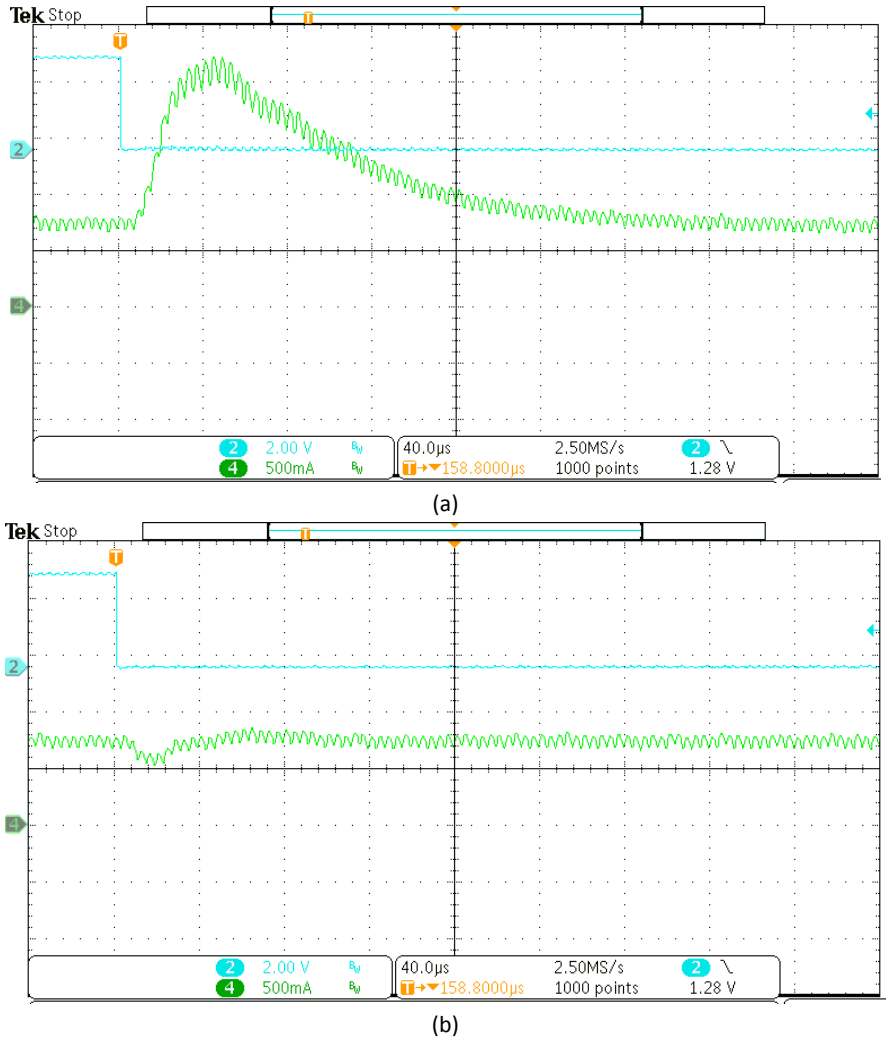
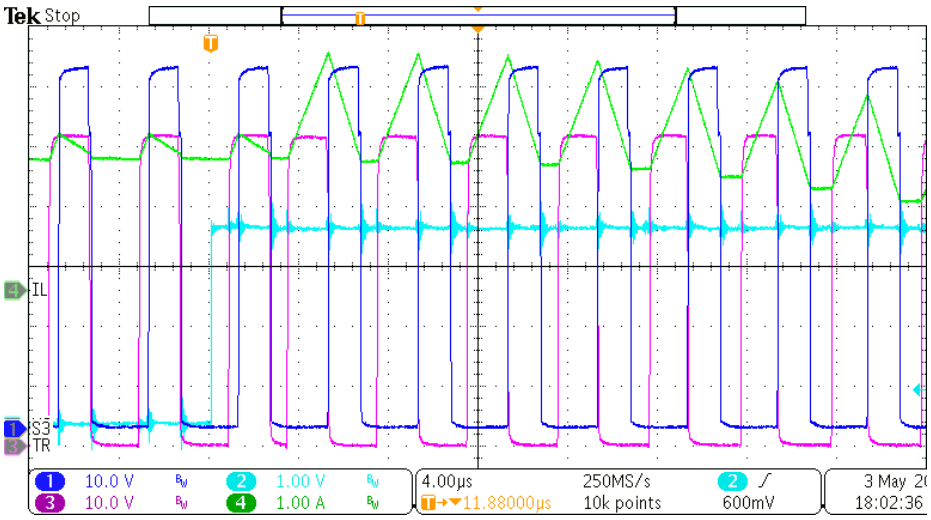


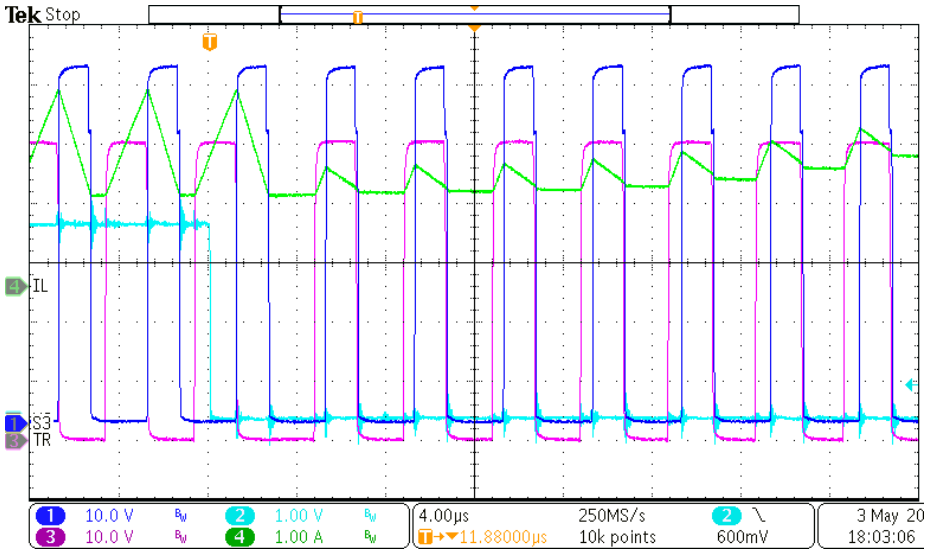
Figure 6-11: Illustration of switch over response of boost to buck- boost (a) General control strategy (b) Proposed control strategy

Ch4 (*green*): Output current, *Ch2* (*Sky-Blue*): Mode of operation 1: buck-boost and 0: boost

One can see from the waveforms that the proposed strategy has a much smoother switch over response with very low output current peak/dip compared to the 1st case. Please note that these 2 experiments were done at lower input voltages and lower set points of the output current, and are just for the illustration of the 2 types of control loop transition response.



(a)



(b)

Figure 6-12: The inductor current and gate signal waveforms for switch over from boost to buck-boost (a) Magnified view of the point of switchover (b) Zoomed out waveform for observing the output current during transition
Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): Mode of operation 1: buck-boost and 0: boost, *Ch1* (*Royal-Blue*): Gate of S1 w.r.t DC bus Gnd and *Ch3* (*pink*): Gate of S3 w.r.t DC bus Gnd

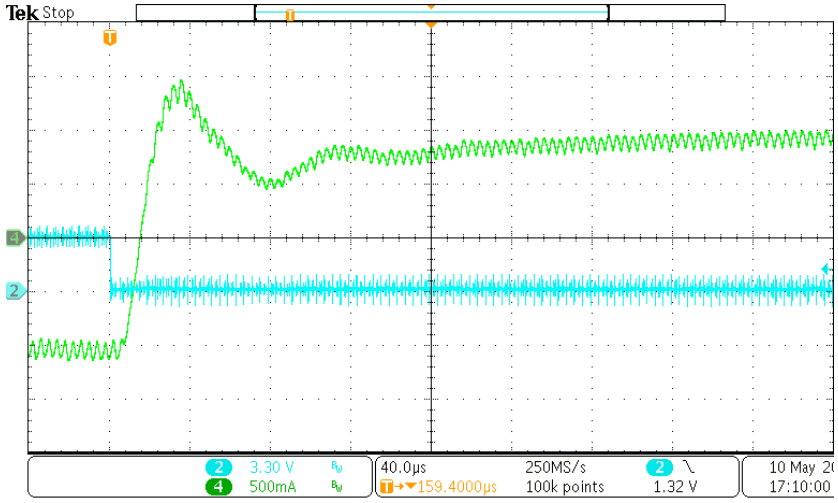
Finally, the waveforms for switchover at a lower scale, showing the variation in the inductor current at the point of transition for both buck-boost to boost and vice-versa, for a negative current set point is

presented in Figure 6-12. One can see that, as the mode changes, the waveform of switch 1 and switch 2 change as well, and consequently the inductor current waveform changes.

In Figure 6-12(a), it can be seen that**,** before the transition, the S1 is overlapping on S3 as in the boost mode S1 is On for D_{on} as well as D_{off} (S3 is equivalent to D_{off}). After the transition, it shifts and the overlap is removed which is in accordance with the buck-boost mode of operation. Recall that in the buck-boost mode, switch S1 is On for only D_{on} and stays Off for D_{off}. Also, the ON time of S1 stays the same, which is in accordance with the control loop switch over strategy, because the same controller output is now equal to D_{on}, where as in boost mode it was equal to sum of D_{on} and D_{off}, and the S1 period is also equal to sum of D_{on} + D_{off} before and is equal to D_{on} after transition. Similarly, in Figure 6-12(b), the transition is from buck-boost to boost and one can see that the On period of S1 shifts and an overlap with S3 is created after transition, which is in accordance with the boost mode of operation. The waveform of the inductor current changes as well and the ripple is much lower in the tri-state boost mode as expected. Thus in this section, the switchover operation as well as the output response for both boost to buck-boost as well as buck-boost to boost transition is analyzed with the experimental results.

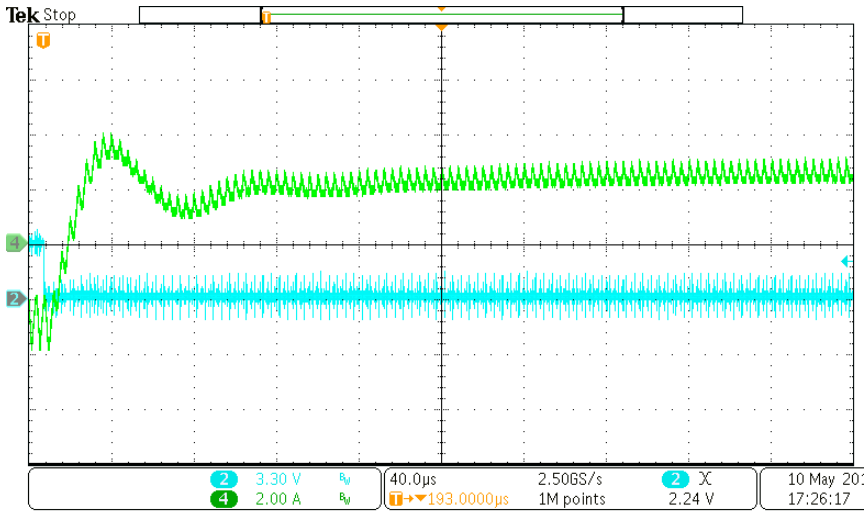
6.3.6 Transient response of the output current control

To verify the transient response of the current controller, both negative and positive transient in the output reference current is applied to the converter and the results is presented in Figure 6-13 and Figure 6-14. The other parameters are V_o = 48V, L = 38.8µH, C = 71.2µF, R_{eq} = 0.05Ω.



(a)

Ch4 (*green*): output current, *Ch2* (*Sky-Blue*): Polarity of I_{ref}: 0 is positive 1 is negative.

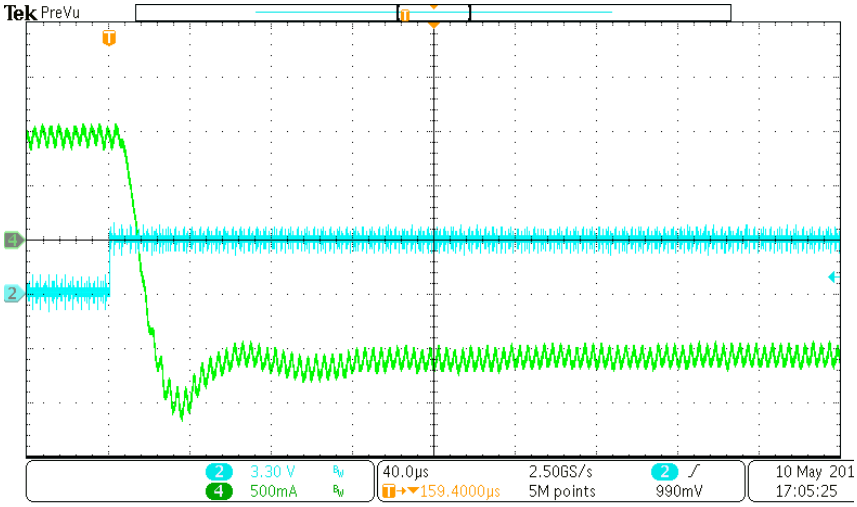


(b)

Figure 6-13: The transient response of the (a) Output Current (b) Inductor current; for V_{in} = 33 V for output current reference negative transient of: -1 to 1 A

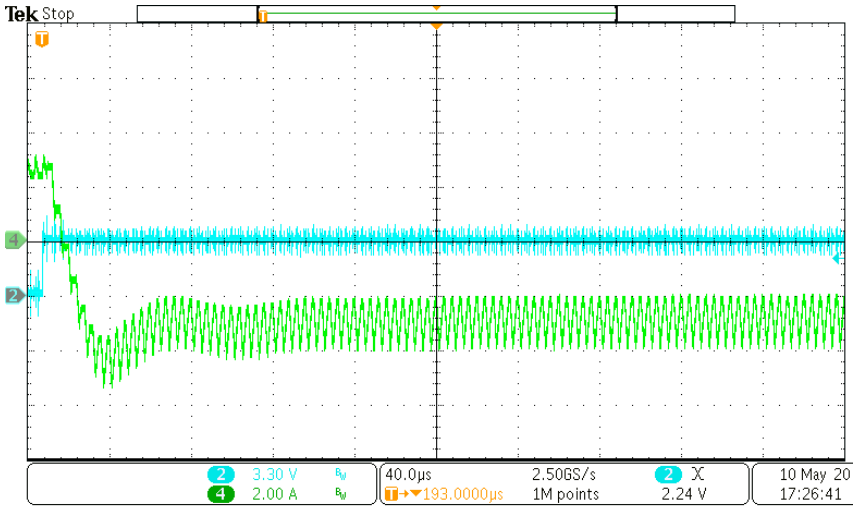
Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): Polarity of I_{ref}: 0 is positive 1 is negative.

In Figure 6-13(a), the negative to positive transient in the output current for V_{in} = 33 V is shown, where the reference current is changed from -1 to 1 A at the point of trigger shown by the step transition in (*Ch2 sky-blue)*, and it can be seen that the converter has an overshoot of 0.5 A after 32µs, and the output current (*Ch4 sky-blue)*, settles down after around 200 µs.



(a)

Ch4 (*green*): output current, *Ch2* (*Sky-Blue*): Polarity of I_{ref}: 0 is positive 1 is negative.



(b)

Figure 6-14: The transient response of the (a) Output Current (b) Inductor current for V_{in} = 33 V for output current reference positive transient of: 1 to -1 A

Ch4 (*green*): inductor current, *Ch2* (*Sky-Blue*): Polarity of I_{ref}: 0 is positive 1 is negative.

In Figure 6-13(b), the corresponding waveform of inductor current during the transient is shown as well and it can be seen that the curve of 2 waveforms mirror each other and inductor current also has an overshoot of around 1A after 40µs and a settling time of 200 µs. For the same parameters, the output and inductor currents for a negative transient of 1 to -1A is also shown in Figure 6-14**,** where one finds that a similar response to that of the positive transient is obtained, with the overshoot being of -0.5 A after 32µs and settling time of around 120µs . Note that, the mode of operation changes from tri-state boost to tri-state buck-boost and vice-versa for negative and positive transient respectively which is in accordance with the analysis done in *section 6.3.4*. This is evident from the fact that, the inductor current ripple is lower for tri-state boost and increases considerably, after negative transient, when the output current goes negative, as in the buck-boost mode the current ripple is higher.

On comparing experimental results with that obtained from simulation using PSIM (*section 5.3*), one finds that the former does not totally agree with that of latter. The rise time in former is much smaller than that in latter, however, the settling time of both is very close, i.e. 187µs in simulation whereas 200 µs in the experimental. The difference in the rise time can be attributed to the fact that, the DC bus has been emulated using a resistor in series with a Laboratory power supply, which is not an ideal voltage source as assumed. Taking the experimental results with an actual DC nano-grid would be valuable, as mentioned in *section 7.2*.

6.3.7 Transient response of the droop mode control

For testing the response of the converter while operating in droop mode, a load transient of 4.5Ω is applied to the DC nano-grid bus, consequently the bus voltage reduces, and according the droop characteristic, the converter, initially charging the supercapacitor, will now start providing power to the DC bus to support the load transient. The parameters of this setup are, bus parameters: R_d = 0.05Ω, V_{meq} = 47.85V, converter parameters: $R_{droopConverter}$ = 0.25Ω, $V_{midConverter}$ = 47.6 V. So initially, the output current reference will be equal to -0.8A, as calculated by the equation (98).

$$I_{outInitial} = \frac{(V_{meq} - V_{midConverter})}{R_d + R_{droopConverter}} \quad (98)$$

After applying a transient of 4.5Ω, one can find the new R_{eq} and V_{meq} for the bus using the source transformation discussed while deriving the model of the DC bus (*section 2.1*). V_{meqNew} and R_{eqNew} are equal to 47.324V and 0.0417Ω, given by the formula (99) and (100). Consequently, the output current I_{out} in the balance state after transient will be 0.9, as obtained by new value of V_{meq} and R_{eq} (equation 98).

$$R_{eqNew} = \frac{(R_{eq}R_L)}{R_{eq}+R_L} \quad (99)$$

$$V_{meqNew} = \frac{(V_{meq}R_L)}{R_{eq}+R_L} \quad (100)$$

The waveforms for this transient response can be seen in Figure 6-15. The operating parameters are V_{in} = 33V, V_{meq} = 47.85V, R_{eq} = 0.05Ω, applied load R_L = 4.5Ω**.**

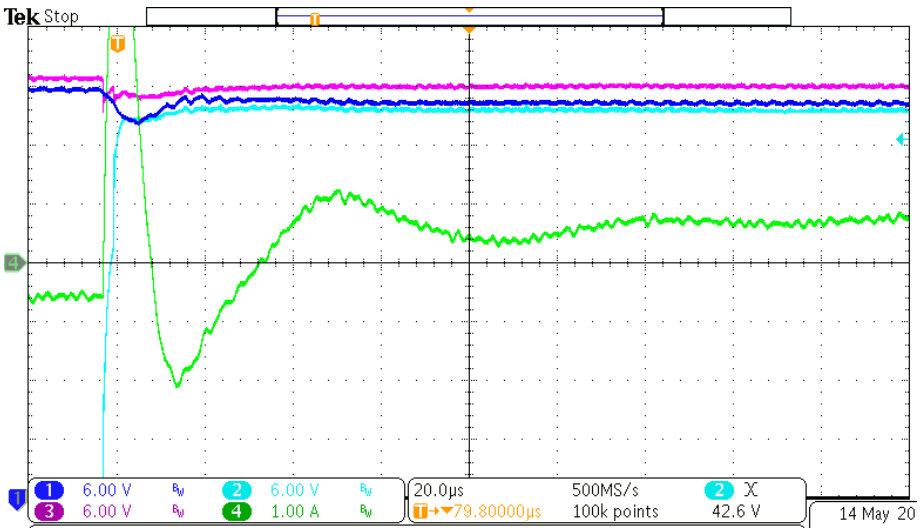


Figure 6-15: Experimental results for droop control transient response of the converter
Ch4 (*green*): output current, *Ch2* (*Sky-Blue*): voltage across R_L, *Ch1* (*Royal-Blue*): DC bus voltage and *Ch3* (*pink*): V_{meq}

The waveform of Ch2 (*Sky-blue*) is the voltage across the load, which increases to the DC bus voltage at the point of transient. Note that, the output current (*Ch4-Green*) will have a high peak at the point of transition, as the output capacitor discharges on application of load. However, it recovers quickly and settles down to the set point in around 140µs. Also, the DC bus voltage (*Ch1-Royal Blue*) dips slightly at the point of transition due to discharge of capacitor, but settles down to the new value as the output

current reaches its set point. Its value is lower than anticipated, which can be explained from the fact that, the V_{mideq}, not being an ideal power supply, dips slightly due to load application, thus reducing the overall DC bus value.

Chapter 7 Conclusion

7.1 Summary

The work presented in this thesis demonstrates the advantages of a tri-state control strategy over a conventional dual-state one, for boost and buck-boost modes of operation using a 4-switch bi-directional DC-DC converter for interfacing a supercapacitor with a DC nano-grid, in terms of speed of response and control loop design simplicity. The simulation results as well as the experimental results to support the same, are presented. The converter essentially operates in the boost mode of operation when the supercapacitor voltage is significantly lower than that of the DC bus. Conversely, it switches to the buck-boost mode of operation when the latter (supercapacitor voltage) is comparable to or greater than the former (DC bus voltage), to ensure that one does not loses the control of the converter. The primary goal of this application is to control the current injected into the DC nano-grid, and thus the amount of power supplied or absorbed from the DC bus of the nano-grid into the supercapacitor. Further, the amount of current injected is decided by a droop curve, this being the control strategy generally used to interface storage units to a DC bus.

In Chapter 2 and 3, the dynamic model of the conventional dual-state and the tri-state schemes have been presented respectively, for both modes of operation, where one can see that the former (dual-state) has an RHP zero which is absent in the latter (tri-state). This results in a simple controller design consisting of just a single loop for the tri-state mode of operation, compared to the two cascaded loops control for the conventional dual-state. Moreover, an added advantage of the tri-state logic is that the plant transfer function of both modes of operation (boost and buck-boost) is the same for given operating conditions, what would lead to the same controller being used in either mode.

In Chapter 4, the controller design for the tri-state converter has been discussed, where an improved control strategy for switchover from one mode to the other has been presented as well, and it can be seen from the hardware results presented in Chapter 6 that the new strategy leads to a significantly smoother transition between the 2 modes, observed in form of 80 % lower dip/overshoot in the injected current at the point of transition.

Another aspect of the dual mode of operation is the selection of the point of transition at which the converter switches from one mode to the other. A detailed analysis regarding the same is presented in Chapter 4, where the point of transition is derived, considering the worst case dynamic range of the control loop output variable as well as ensuring minimum value for the inductor current. It is deduced that the transition should be done when V_{in} ≈ 70% of V_o and the value of D_{off} for the same is found to be 0.35, what would ensure a reasonable hysteresis band (3.36V for V_o = 48V) and thus avoid oscillations at the point of transition. Further, for the experimental implementation presented in Chapter 6, it is found that due to the high switching frequency, the role of dead-time becomes significant in deciding the point of transition. This is because, due to the effect of the dead-time the steady state value of controller output increases or decreases, depending on the direction of current, for a given operating condition. The expressions for the new steady state value of the controller output are derived and validated with the results obtained from the experimental results. Based on this analysis one has to select a new point of transition based on the direction of current, which is $V_{switchover}$≈ 80% of V_o for positive injected current and $V_{switchover}$ ≈65% for negative injected current.

The simulation results comparing the response of the 2 control strategies (tri-state and dual-state) for positive and negative transients in the injected current control loop, is given in Chapter 5, and one finds that the proposed tri-state logic has a speed of response about 4 times faster than that of the conventional dual-state for the boost mode of operation and 3 times faster for buck-boost mode of operation, with the same converter topology and component values.

The experimental results for the tri-state modes of operation is presented in Chapter 6. Due to the lower sampling frequency of the system in the experimental setup, the crossover frequency of the control loop is limited to 10 kHz. For comparison purposes, the simulation results of a similar system, showing the transient response of the injected current control loop as well as droop mode of operation, is presented in Chapter 5, where one can see that for both, the experimental results are very similar to those of the simulation.

For developing a comprehensive system design methodology for the two tri-state modes of operation, the expressions for the operating parameters of all major components are derived in Chapter 4, and

further compared with the results obtained with simulation, where one can see that they are in close agreement with each other. The experimental results for supporting the equations of inductor parameters as well as its waveforms for various modes of operation are also presented in Chapter 6, and one finds that the experimental results closely match that of the simulation. The inductor is the only component accessible and all other components like switches and capacitors are soldered on the Printed Circuit Board, hence inaccessible for measurements.

One drawback of the tri-state scheme is the increase in the RMS and average currents of the inductor as well as switches, the equations for which have been presented. This can be reduced to some extent by proper selection of the value of D_{off}. Moreover, there are 2 schemes for implementation of the tri-state logic, which should be selected depending on the direction of power flow to further reduce the inductor and switch currents by 10% and 20% respectively, and thus result into lower power losses.

7.2 Future work

In this work, the droop control implemented does not considers the state of charge of the supercapacitor. One of the potential future developments can be to design the droop curve parameters as a function of supercapacitor's state of charge, what would prevent the further discharging of an already discharged supercapacitor in heavy load conditions and similarly, further charging of a fully charged supercapacitor in light load conditions for the DC nano-grid.

In this work, the DC bus of a nano-grid was modelled after some simplifications. The experimental results presented here were also taken on a setup which "emulates" a DC bus. Obtaining the experimental results for an actual DC nano-grid system can be a valuable future work.

The converter presented in this thesis considers only the application of interface of a supercapacitor with a DC nano-grid. However, it can be used for any application which requires a fast acting converter for the interface of a supercapacitor with an existing DC bus. One of the potential applications is a battery support system, in an electric vehicle (EV). The battery pack is interfaced with the DC bus of the EV using a DC-DC converter. The supercapacitor can be connected at the input side of this DC-DC converter, via the tri-state converter proposed in this thesis, and would essentially provide the high frequency ripple current required

by the DC-DC converter while the average DC current can be provided by the battery, what would lead to an increased battery life. Design of the output capacitor as well as the experimental results for such an application can be also be a potential future work.

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