Dielectric Filled Printed Gap Waveguide for Millimeter Wave Applications

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A Thesis

In the Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy (Electrical and Computer Engineering) at

Concordia University

Montreal, Quebec, Canada

September 2017

CONCORDIA UNIVERSITY
SCHOOL OF GRADUATE STUDIES

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By: Jing Zhang

Entitled: Dielectric Filled Printed Gap Waveguide for Millimeter Wave Applications

and submitted in partial fulfillment of the requirements for the degree of

Doctor Of Philosophy (Electrical and Computer Engineering)

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ABSTRACT

Dielectric Filled Printed Gap Waveguide for Millimeter Wave Applications

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Concordia University, 2017

As the communication system goes up to millimeter-wave frequencies for high data rate demands, the conventional microstrip line no longer meets the requirements due to its excessive radiation and harmful surface waves, causing unacceptable insertion loss and interference issues. The radiation and surface waves are absent in the stripline. However, its conductor loss becomes worse due to the narrower strip causing by the implemented two ground planes. In addition, any vertical asymmetry in the stripline can generate unwanted higher order waveguide modes that will be able to propagate wherever the ground planes exist. The standard waveguide technology is not suitable for millimeter-wave bands because of the small dimension of the hole, which causes fabrication challenging and high cost.

The new technology of gap waveguide (GW) offers a solution to the above problems in current guiding structures. Considerable effort is being made to miniaturize it using the printed circuit technology for low-cost and low-profile applications. The microstrip-ridge GW and the inverted microstrip GW are the two candidates reported previously. However, they come with their own drawbacks. The tiny air gap makes it very sensitive to the outside pressure or the environmental factors. The plated vias in the copper strip and the electroless nickel immersion gold (ENIG) coating on the strip cause substantial attenuation and a frequency shift. In addition, it is challenging to connect to other transmission lines or conventional rectangular waveguides for the integration and measurements. Therefore, one major part of this thesis is to develop innovative GW structures without the formerly mentioned issues to be suitable for millimeter-wave frequencies and easier implementation. Another major part is developing passive components, such as antenna arrays, using the proposed new GW structures. The third part is studying the GW-based PMC packaging for the irregular ground/PEC plane. This will help extend this new packaging technology from the microstrip line circuits to the substrate integrated waveguide (SIW)- or grounded coplanar waveguide (GCPW)-based circuits.

ACKNOWLEDGEMENTS

I sincerely thank my supervisors, Prof. John Xiupu Zhang and Prof. Ahmed Kishk, for all their guidance and support.

I am grateful to my parents and my wife, Xin Yue Wang, for their love and encouragement.

Furthermore, I would like to thank the committee members for their review of my thesis and their numerous constructive comments and feedback.

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List of Acronyms

DGS	Defect Ground Structure
EBG	Electromagnetic Bandgap
ENIG	Electroless Nickel Immersion Gold
GCPW	Grounded Coplanar Waveguide
GW	Gap Waveguide
HFSS	High Frequency Structural Simulator
LTCC	Low Temperature Co-Fired Ceramic
MEMS	Micro-Electro-Mechanical System
mm-wave	Millimeter-Wave
PCB	Printed Circuit Board
PEC	Perfect Electric Conductor
PMC	Perfect Magnetic Conductor
SIGW	Substrate Integrated Gap Waveguide
SIW	Substrate Integrated Waveguide
SMA	SubMiniature Version A
TEM	Transverse Electromagnetic
TRL	Thru-Reflect-Line
VNA	Vector Network Analyzer
3D	3 Dimensional

Chapter 1 Introduction

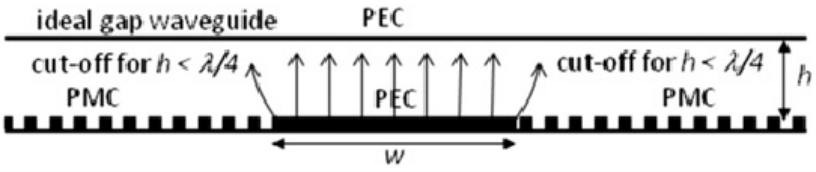
1.1 Challenge in Guiding Structures at High Frequencies

As the communication system is going up to millimeter-wave frequencies for the growing demand for utilizing high data rates, the most common guiding structures all have inevitable problems at high-frequency bands. The microstrip line, for example, suffers from much radiation and surface waves and thus has unacceptable insertion loss and interference with the adjacent components at millimeter-wave bands. The radiation and surface waves are absent in the stripline. However, the implemented two ground planes make strip narrower, which is only half of the microstrip line width for a given frequency. The narrow strip not only considerably increases conduction losses due to the higher current density and conductor roughness but also causes challenges in the fabrication at high frequencies for the required high precision. Moreover, any vertical asymmetry in the stripline can create unwanted higher order waveguide modes that will be able to propagate wherever the two ground planes exist. Considering hollow waveguides, they have excellent performance at mm-wave bands. However, the large size and weight prevent them from many implementations. In addition, due to the small size of the hole at high frequencies, hollow waveguides have to be fabricated in separate parts and then connected. This requires an excellent electrical contact and precision in aligning. As the planarization of hollow waveguides, the substrate integrated waveguide (SIW) has significantly reduced the size and weight. However, its fundamental TE_{10} mode causes mode conversion losses when combing with other transverse electromagnetic (TEM)/quasi-TEM transmission lines. Besides the increased insertion loss, the additional transition part, such as a tapered microstrip, is also necessary which is not preferred in the circuit compactness.

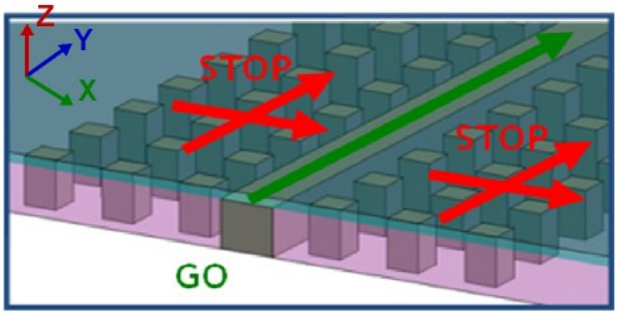
1.2 Gap Waveguide Technology

Recently, a new metamaterial-based guiding structure, gap waveguide (GW) technology, has been introduced for microwave and millimeter-wave applications [1]-[3]. As illustrated in Figure 1-1, the gap waveguide is formed in the narrow gap between the central metal ridge and

the top metal plate. When the gap height is smaller than a quarter wavelength, there will be only a propagating quasi-TEM mode guided by the metal ridge, which is surrounded by the perfect magnetic conductor (PMC) surface, as indicated by the green line in Figure 1-1 (b). As explained by the red lines in Figure 1-1 (b), the propagation of all kinds of global parallel-plate modes are prohibited by a bed of periodic metal pins on both sides of the ridge, which creates a high impedance surface (ideally a PMC). A larger gap can be used in the GW to minimize the conduction losses, without radiation losses or surface waves that exist in microstrip lines. The GW is compatible with other planar circuits and easily fabricated at mm-wave frequencies since no electrical contacts are required between the PEC and PMC plates. The GW has been implemented to realize high-performance components, such as filters, power dividers, and antennas [4]-[7].



(a)



(b)

Figure 1-1 Illustration of a ridge gap waveguide (GW). (a) Front view [3]. (b) Overview [6].

A GW unit cell of a bed of periodic metal pins is illustrated in Figure 1-2 (a). The dispersion diagram for this cell, calculated from the high frequency structural simulator (HFSS) eigenmode solver, is shown in Figure 1-2 (b). As indicated by the dashed green curve, the basic parallel-plate mode starts at zero frequency as a TEM mode and then goes into cutoff at 9.23 GHz. It appears again at 22.17 GHz together with another mode, indicated by the dotted-dashed blue and dotted-dotted-dashed orange curves, respectively [1], [3]. This cell with a guiding ridge in the bed of periodic pins is presented in Figure 1-3 (a). Different from the dispersion diagram

in Figure 1-2 (b), Figure 1-3 (b) shows that a quasi-TEM mode following the ridge is generated in the band gap without any other propagating modes. It is termed as a quasi-TEM mode because it follows the light line (i.e., representing a TEM mode) very closely but not exactly. Several modes appear below 10.65 GHz due to the interaction of the ridge with the pins as well as due to the truncation of the periodicity in the transverse direction and thus possible standing waves that are introduced due to the metal walls used to support the upper metal cover. A higher order gap waveguide mode comes in at 21.54 GHz, which is the end of this band gap.

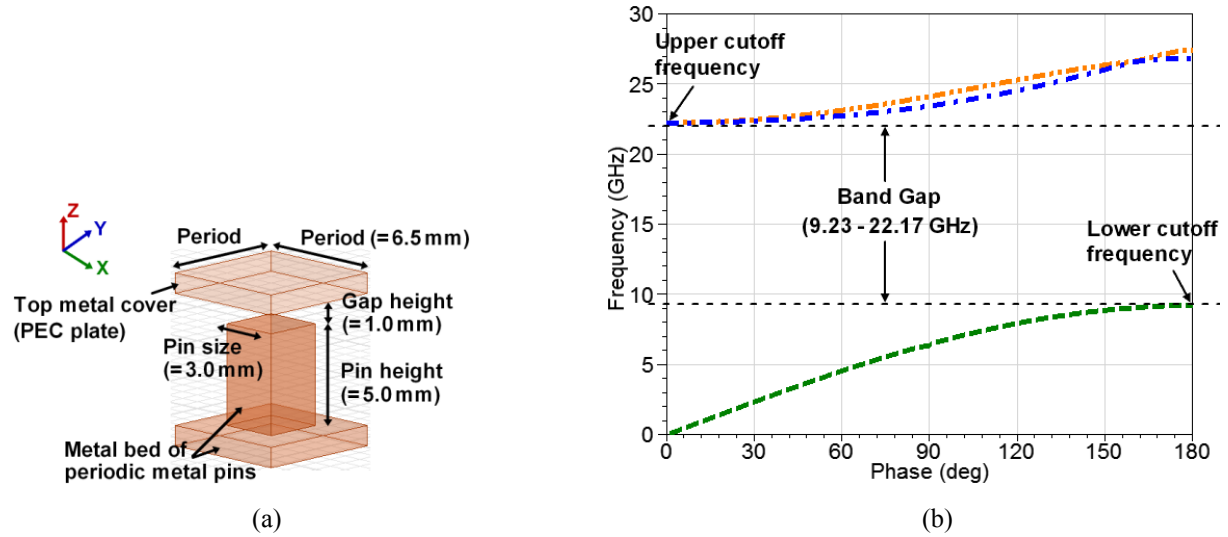


Figure 1-2 (a) A GW unit cell of a bed of periodic metal pins. (b) Calculated dispersion diagram.

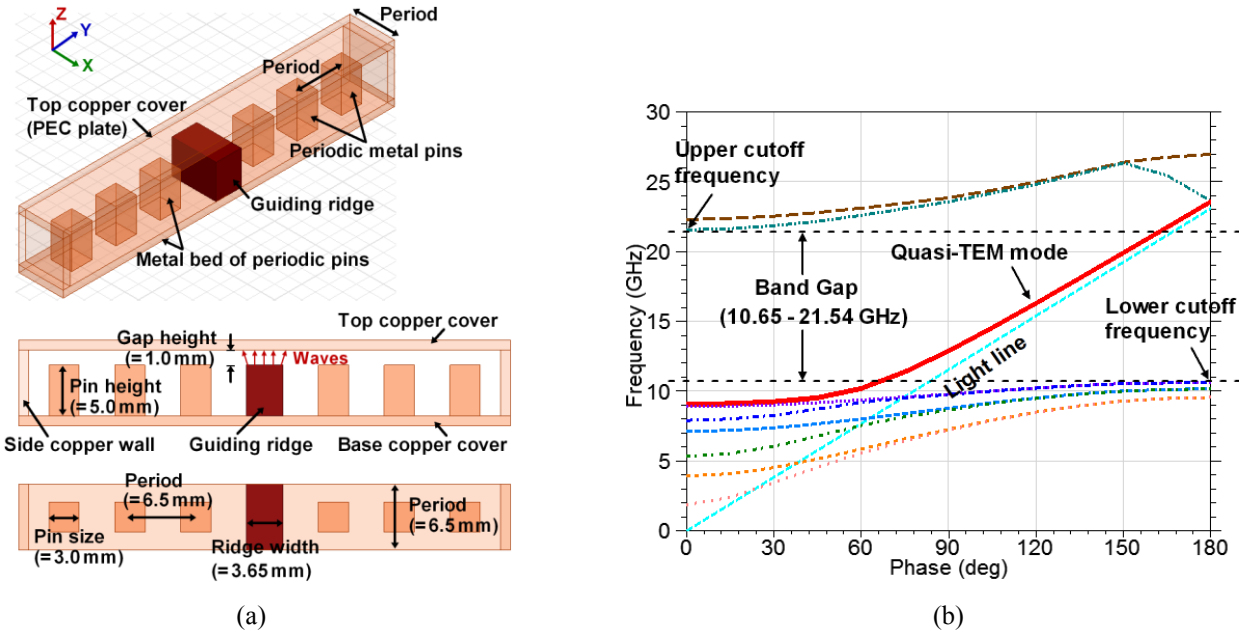


Figure 1-3 (a) A GW unit cell of a bed of periodic pins with a guiding ridge. (b) Calculated dispersion diagram.

1.3 Gap Waveguide PMC Packaging Technology

As indicated above, when the separation between PEC and PMC surfaces is smaller than a quarter wavelength, a propagating quasi-TEM mode is also available if a narrow metal strip over the PMC surface without having any other unwanted modes. So, the other application of the GW technology is to employ it as a packaging technology for planar microstrip circuits, such as microstrip filters [8], [9], microstrip power dividers [10], and active component [11], [12]. This packaging technology is illustrated in Figure 1-4. Figure 1-5 (b) indicates that the band gap still exists even when a dielectric substrate is inserted between the PMC and PEC plates as presented in Figure 1-5 (a). And similar to Figure 1-2 (b), the basic TEM mode starting at zero frequency goes into cutoff at 9.40 GHz and appears again at 19.34 GHz together with another mode.

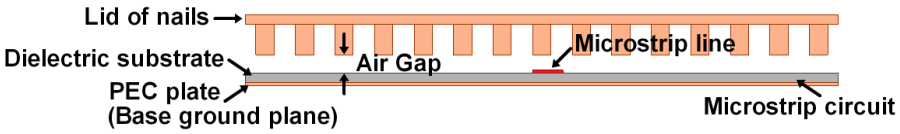
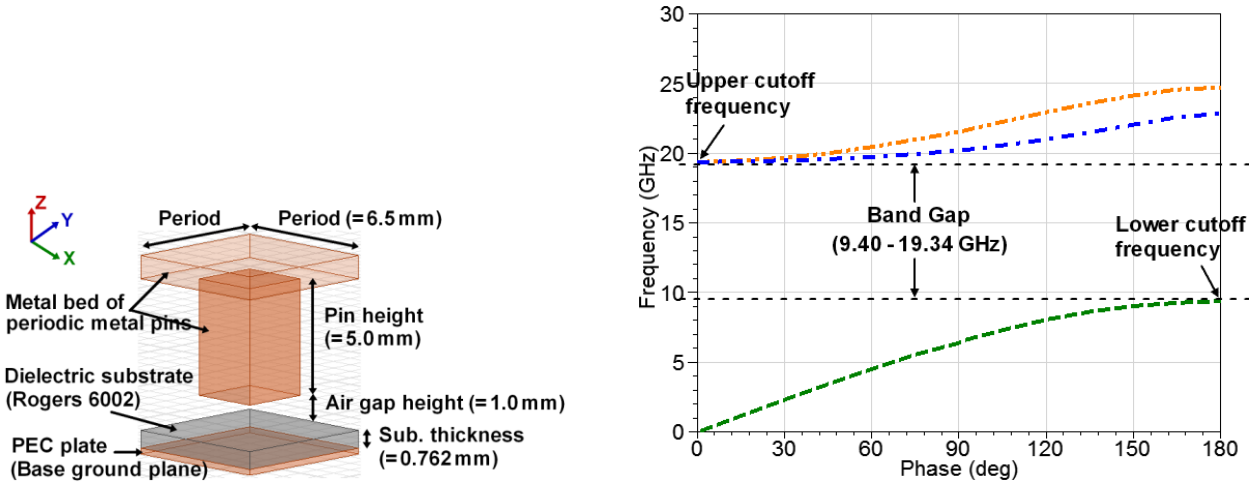


Figure 1-4 Illustration of GW-based PMC packaging technology for a microstrip line circuit.



(a) (b)

Figure 1-5 (a) A GW unit cell of a bed of periodic pins containing a dielectric substrate. (b) Calculated dispersion diagram.

The advance of such a GW-based PMC packaging technology is evident if compared with the current packaging solutions as presented in Figure 1-6. As seen, a sealed metal box is used to enclose a circuit to suppress radiation and shield it against the environmental effects. Metal septa and lossy absorbers are added to prevent cavity resonances and coupling over the air. Of course,

grounded vias are also needed to stop such a coupling between the adjacent components through the surface waves in the substrate. It is seen that the absorbers and grounded vias are all unneeded in the PMC packaging (Figure 1-4), while both unwanted cavity modes and surface waves can be suppressed within the band of interests and better isolation performance can be achieved.

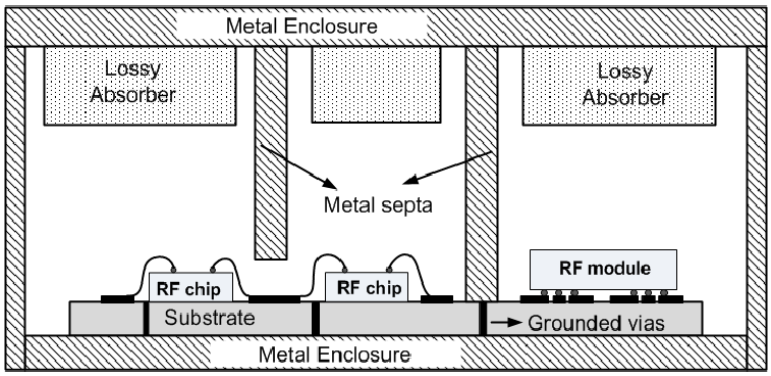


Figure 1-6 Conventional packaging enclosure with metal septa, lossy absorbers, and grounded vias [11].

1.4 Motivation and Contributions

Being free from radiation and surface waves and easier manufacturing at high frequencies, the GW technology is promising for microwave/mm-wave applications. However, the size and weight still prevent it from the low-profile and low-cost applications. We may have to resort to the high-cost micro-electro-mechanical system (MEMS) process to realize the desired small-size periodic pins [13], [14]. Besides, the transition between the GW and other planar circuits is still complex and limits its compatibility [15]-[17]. Efforts have been made to miniaturize the original GW, such as the microstrip-ridge GW [18] and the inverted microstrip GW [19], replacing the conventional periodic metal pins with the plated vias that can be easily realized by the low-cost PCB process. Unfortunately, these reported variants of the GW come with their own problems [18]-[24]. The implemented air gap is so tiny that makes it very sensitive to the outside pressure or environmental effects. The plated vias in the copper strip and the electroless nickel immersion gold (ENIG) coating on the strip cause substantial attenuation and a frequency shift. In addition, it is challenging to connect them to other planar lines or conventional rectangular waveguides for the integration and measurements.

Therefore, a major part of this thesis is devoted to address the above defects in current GW technologies. Two innovated GW variants have been developed based on the low-cost PCB technology. The first one shown in Chapter 2 is named as a substrate integrated gap waveguide (SIGW). It is constructed by two-layer substrates and uses two contacted printed strips to build the required conducting ridge. In the SIGW, the wave will no longer interact with the plated vias in the strip and the high-loss ENIG coating. The other one presented in Chapter 4 is named as a packaged microstrip line, which not only avoids using plated vias in the printed strip but also avoids the possible alignment issue in the SIGW between the two strips. Moreover, the strip can have an arbitrary width, no longer limited to the available diameter of the plated via in the PCB technology. Of course, in both the proposed GW variants, a stable gap is guaranteed with the use of a gap-layer substrate, which also helps resist the environmental impact. A constant gap height between PMC and PEC surfaces is critical in ensuring the desired performance. The design of slot antennas based on the SIGW and the packaged microstrip line are presented for the first time in Chapter 3 and Chapter 4, respectively. Without radiation and surface waves, it can be expected that enhanced gain, efficiency, and radiation characteristics can be achieved in these antennas.

The other concentration of this thesis is, of course, the GW PMC packaging technology. This packaging solution has been studied previously for microstrip filters [8], [9] and microstrip power dividers [10]. All those reported works are on the basis of a smooth PEC/ground plane and concentrated more on the construction of the PMC surface for different frequency bands, such as inverted pyramid-shaped pins [25], a lid of springs [26], and a lid of printed zigzag wires [27]. However, the ground plane under the PMC could be irregular. For example, in the grounded coplanar waveguide (GCPW), a number of ground vias are implemented along with the slots to reduce the radiation losses and suppress the parasitic parallel-plate modes. Another example is the SIW combining with microstrip lines. The upper PMC shielding will face two different gap heights – one is from the PMC to the SIW top metal cover, and the other is between the PMC and the ground plane of the microstrip line. Because the generation and characteristics of the band gap are critically dependent on the gap between the PMC and PEC, the effectiveness of this packaging technology for such an irregular PEC/ground plane should be proven additionally and investigated. This study, presented in Chapter 5, will make the GW PMC packaging technology available for more different planar transmission lines, no longer only limited to the microstrip line circuits.

1.5 Thesis Outline

This thesis is organized into six chapters with abstract and references as follows:

Chapter 2 introduces the proposed SIGW. The dimensions (gap height, strip width, and via diameter) and the substrate property (permittivity, ε_r, and loss tan δ) are taken into account to study the characteristic impedance and the loss performance. The study has also considered the gap- and via-layers of the SIGW using different substrates, which will make the SIGW more flexible in a design for the desired performance. A guideline will be offered for implementing the SIGW after investigations. The bend discontinuities of the SIGW strip-ridge are studied further. This is of great help to realize future feeding networks for SIGW antenna arrays or other types of cost-effective SIGW passive components, in which many discontinuities are naturally present. A simple solution will be presented to minimize the discontinuities and suppress the possible cavity resonances. Three fabricated prototypes will be used to present the experimental verification for the proposed SIGW and the bend solution.

In Chapter 3, slot antennas constructed on the SIGW are presented for the first time. In particular, a bandwidth-enhancement method is proposed for the SIGW-based slot antenna. The plated vias next to the strip feed line are utilized to fine tune the impedance of the cavity under the slot, which will be able to offer a very broadband impedance transition between the feed line and the slot. It has been proven that the achievable antenna bandwidth can be greater than 20 GHz centered at 60 GHz. A single-slot antenna and a 4-slot linear antenna array, both at 60 GHz, have been fabricated to verify the SIGW antenna and the proposed bandwidth-enhancement method.

Chapter 4 is the study of the other proposed GW variant, packaged microstrip line, which further addresses the possible alignment issue in the SIGW between the two printed strips. The stopband, dielectric/conduction losses, and characteristic impedance of the packaged microstrip line have been carefully investigated to offer a general design guideline for this new planar line. The transition from the packaged microstrip line to the standard microstrip line is also included in the study. It has been proven that the external transition part, such as a tapered microstrip line, is unneeded for such a connection, which is helpful for the circuit design and compactness. Two fabricated prototypes with different PMC-layer substrates are used to provide the experimental

verification. Also, a 60 GHz antenna has been realized for the first time based on the packaged microstrip line.

In Chapter 5, the characteristics of the band gap are studied for the PMC shielding with an irregular PEC/ground plane. In the case of the ground plane containing grounded vias, the study considers the relative size of the solid rectangular pin and the cylinder plated via and their relative positions in the vertical. The effectiveness is verified by a fabricated GCPW with a PMC shielding lid of metal pins. In the study of the SIW integrated with the microstrip line using the PMC lid of metal pins, the pin size, air gap, and substrate height and ε_r have been taken into account. A simplified PMC lid is proposed further by removing the metal pins directly over the SIW. It will show how many columns of the pins should remain and the required position of the pins relative to the SIW. Moreover, the effect of the side air gap between the SIW and side metal walls to the PMC shielding will be presented, with a corresponding solution. A fabricated SIW Chebychev bandpass filter is used to give the experimental verification.

Chapter 6 concludes the thesis.

Chapter 2 Substrate Integrated Gap Waveguide

2.1 Introduction

As introduced in Chapter 1, gap waveguide (GW) technology is promising for microwave and mm-wave applications over the currently used planar lines – microstrip line, stripline, and SIW. The current research interests on GW is to miniaturize it for low-profile implementations using the low-cost PCB technology. The two reported candidates are the microstrip-ridge GW [18] and inverted microstrip GW [19]. Considering the microstrip-ridge GW, however, lots of grounded vias in the copper strip heavily perturb the current flowing on it and cause substantial losses. The attenuation can also be of the high-loss ENIG coating on the strip top, which is standard in the PCB technology [18]. A frequency shift of S_{11} can even be caused additionally by the ENIG coating. This is because that the waves in the microstrip-ridge GW propagate in the air gap on the strip top, i.e., the ENIG-plated side of the copper. As a result, the copper strips have to be plated with silver to offset the ENIG effects. The effects of the ENIG coating and grounded vias in the strip are avoided in the inverted microstrip GW, by implementing the PMC surface under the substrate [19]. Unfortunately, it is challenging to connect such an inverted microstrip GW to other planar lines or conventional hollow waveguides for integration and measurements [19], [23], [24]. Moreover, considering the tiny air gap between the PMC and PEC/ground planes, in practice it is really challenging to keep a constant air gap height all over the circuit – for example, the feeding network for a big antenna array. The degraded performance due to the deformation of the air gap is unpredictable, which could be due to the outside pressure or other environmental factors. However, the band gap, conduction losses, and characteristic impedance of the GW are all critically determined by the air gap.

In this chapter, a developed GW is proposed using the PCB technology, based on the fact the claimed lower losses of the GW (compared to microstrip circuits) actually mainly owe to the thicker gap which is able to significantly reduce the conduction losses, rather than the removal of dielectric which offers only about 25% of the total losses [29]. The construction of this novel GW, named as a substrate integrated gap waveguide (SIGW), will be described firstly. It will be seen that the wave in the SIGW will no longer interact with the plated holes in the strip and high-

loss ENIG coating, by using the built conducting ridge. Moreover, the integration between the SIGW and microstrip line is much easier, because they can share with the same substrate. This improves the transition continuity and decreases the structure and design complexity. It will be proven further that the additional transition part, such as a tapered microstrip line, is unnecessary between them. Two SIGW prototypes are fabricated to offer the experimental verification. The ridge-bend discontinuities in the SIGW have been studied additionally. This is the basis to realize future feeding networks for SIGW antenna arrays or other cost-effective SIGW passive components, in which many discontinuities are naturally present. A simpler solution to the bend discontinuities is proposed, compared with the one in [18] for the microstrip-ridge GW. This solution is verified as well with a fabricated SIGW with two 90º bends.

2.2 Construction of Substrate Integrated Gap Waveguide (SIGW)

A unit cell of the SIGW is illustrated in Figure 2-1. As seen, the SIGW is constructed by two-layer substrates: a gap-layer to guarantee a constant gap height, resisting the environmental impact, and a PMC-layer built by periodic plated vias to suppress all the unwanted modes. The conducting ridge is realized by two contacted metal strips – on the top of the via-layer and at the base of the gap-layer, as shown in Figure 2-1 (c). Different from the microstrip-ridge GW, the plated vias are only in the lower strip. Therefore, the wave on the upper strip top will no longer interact with these vias. Moreover, the inner surface of the copper strip is without the ENIG coating. Therefore, the SIGW has better loss performance than the microstrip-ridge GW. And the frequency shift due to the plated vias in the strip can be removed.

Figure 2-2 is the dispersion diagram for one SIGW unit cell calculated from the HFSS eigenmode solver, with the dimensions and materials indicated in Figure 2-1. It is seen that a quasi-TEM mode, presented by the solid red line, is generated within the band from around 43 to 76 GHz without any other modes. The light line, presented by the dashed blue line, is used to represent the pure TEM mode in the substrate.

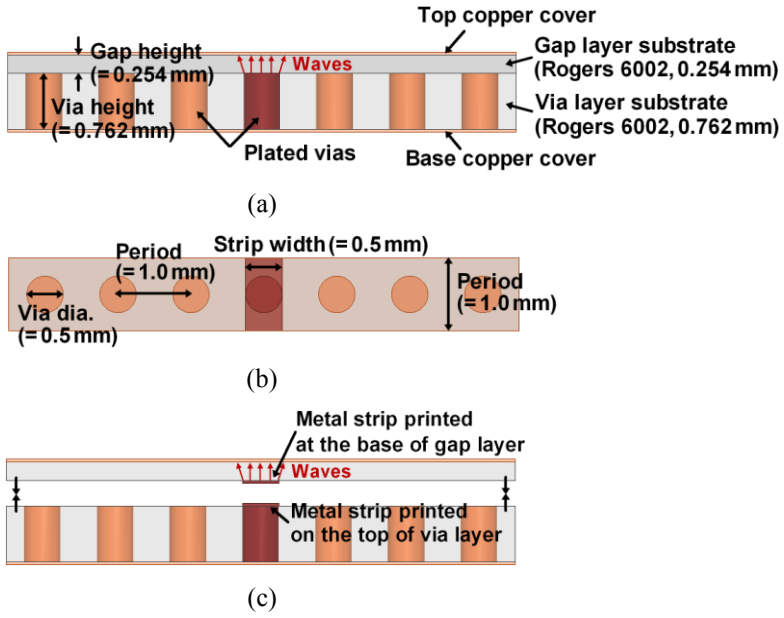


Figure 2-1 Illustration of a SIGW unit cell. (a) Front view. (b) Top view. (c) Distributed view.

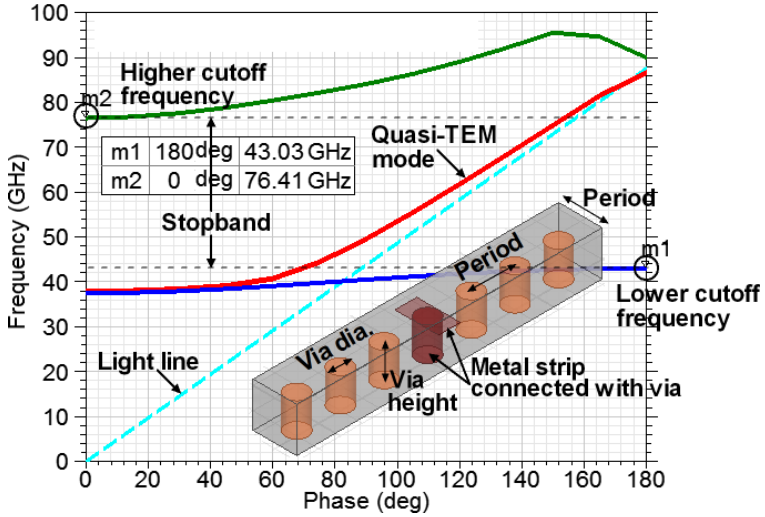


Figure 2-2 Dispersion diagram of a SIGW unit cell.

Considering the via- and gap-layers with different ε_r, the characteristics of the quasi-TEM mode presented in Figure 2-3 show that it is mainly determined by the gap-layer. For example, as demonstrated by the solid red curve in Figure 2-3 (b), the quasi-TEM mode in the case of via-layer ε_r = 5 and the gap-layer ε_r = 3 is almost the same in the case of via-layer ε_r = 3 and the gap-layer ε_r = 3 shown by the dashed green curve. This is because the wave is mainly concentrated in the gap-layer. However, the divergence between the above two indicated curves also reveals the via-layer effect, which can be stronger if this layer ε_r is much larger than the gap-layer ε_r, as presented in Figure 2-3 (c) considering the via-layer ε_r =10 and the gap-layer ε_r = 3 or 5. The

quasi-TEM mode indicated by the solid red curve (via-layer ε_r = 10 and gap-layer ε_r = 3) is not closed anymore to the dashed green curve for via-layer ε_r = 3 and gap-layer ε_r = 3. The reason is that part of the power is leaked from the gap into the via-layer substrate. Obviously, the via-layer of a high ε_r will hold more power and impose a stronger effect on the propagating mode. Therefore, in the following study of the SIGW characteristic impedance and loss performance, this case for the gap- and via-layers using different substrates will be considered.

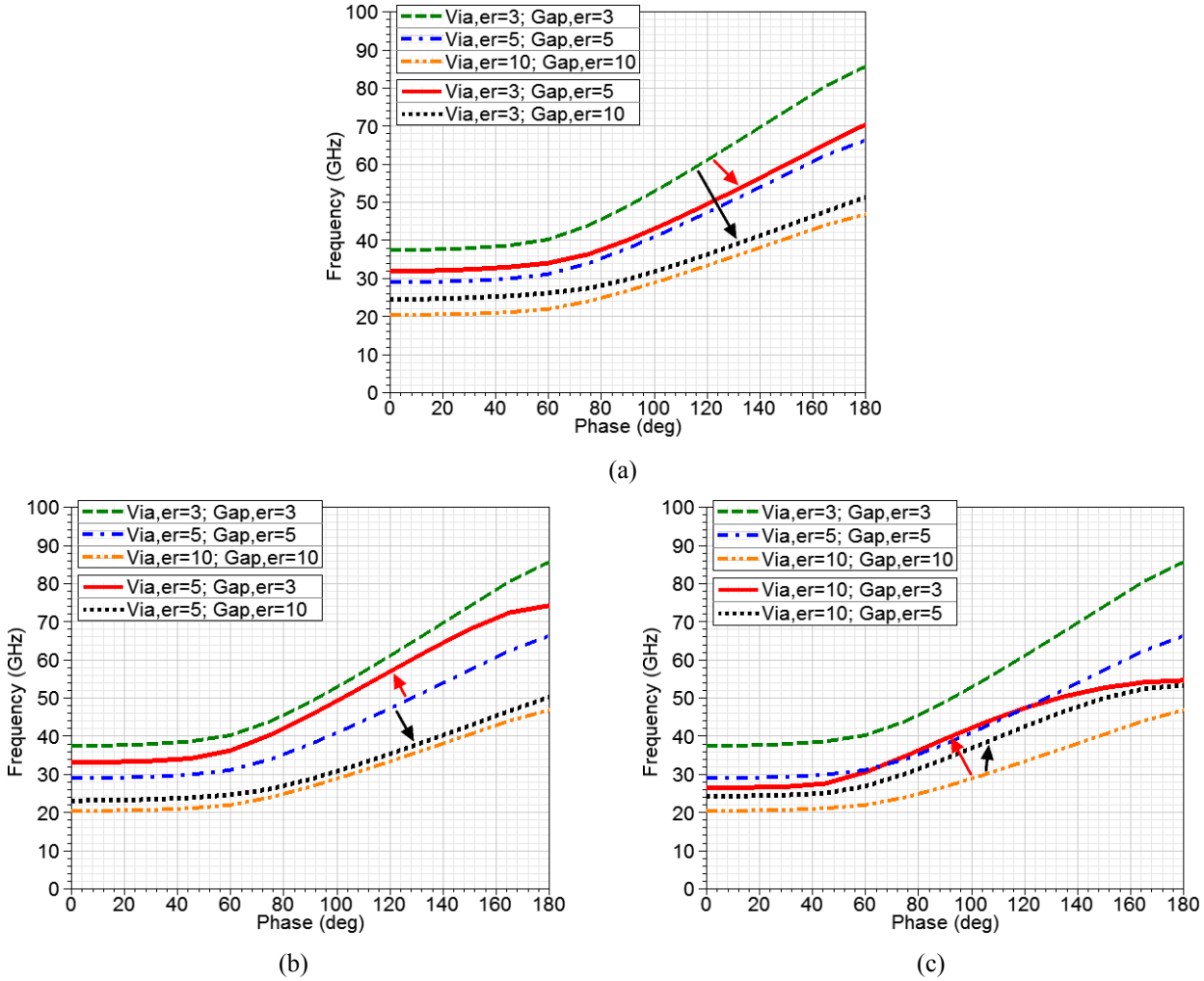
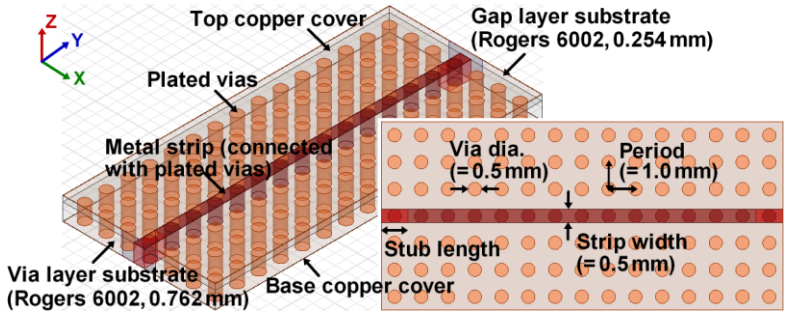


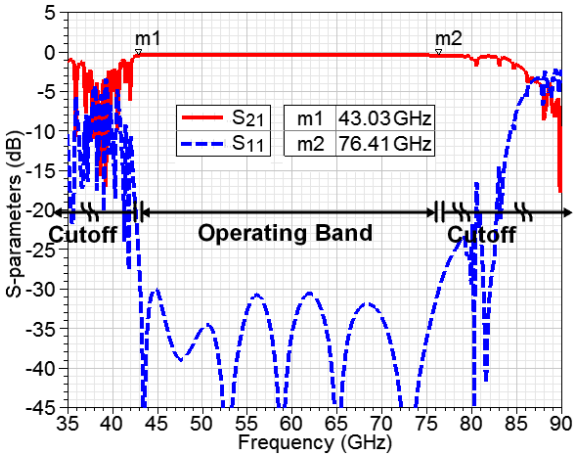
Figure 2-3 Characteristics of SIGW quasi-TEM mode with different substrates for the via- and gap-layers. (a) Via-layer ε_r = 3, and gap-layer ε_r = 5 or 10. (b) Via-layer ε_r = 5, and gap-layer ε_r = 3 or 10. (c) Via-layer ε_r = 10, and gap-layer ε_r = 3 or 5. For comparison, the via- and gap-layers of the same substrate is also shown, i.e., ε_r =3, 5, or 10.

2.3 Study of Characteristic Impedance

The SIGW, which is used to examine the characteristic impedance and losses, is shown in Figure 2-4, with the same dimensions and materials given in Figure 2-1. The metal stubs at the input and output are to offer impedance matching for the wave port in HFSS. The simulated S-parameters are shown in Figure 2-4 (b). Initially considering the gap- and via-layers with the same substrate of Rogers RT/Duroid 6002, a passband from 43.03 to 76.41 GHz is generated.



(a)

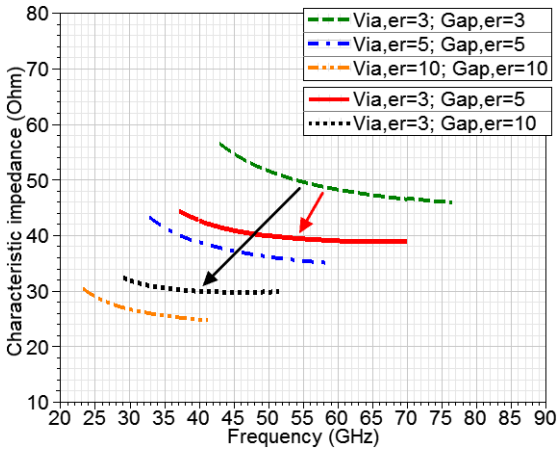


(b)

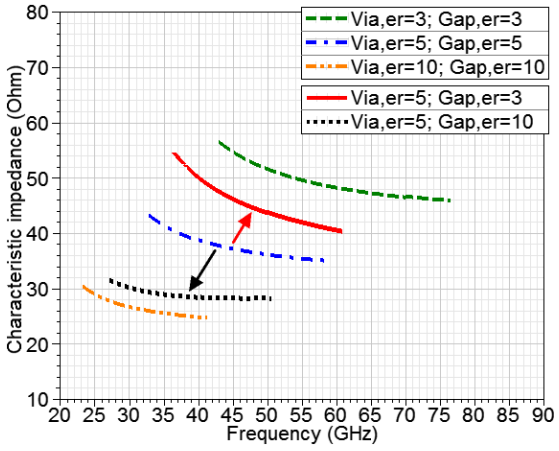
Figure 2-4 SIGW entire structure in simulations. (a) Overview and top view. (b) Simulated S-parameters with the same dimensions defined in Figure 2-1.

According to [18], the characteristic impedance of a GW can be calculated using the wave port in HFSS, and it is very precise as far as the reflection coefficients, S_{11}, are lower than -30 dB. Given the gap height of 0.254 mm, Figure 2-5 presents the change in the SIGW characteristic impedance with its gap- and via-layers of the same or different ε_r. Only the performance within the created passband is presented (curves outside the passband are truncated). The length of the metal stubs is optimized to make the reflection lower than -25 dB at least to

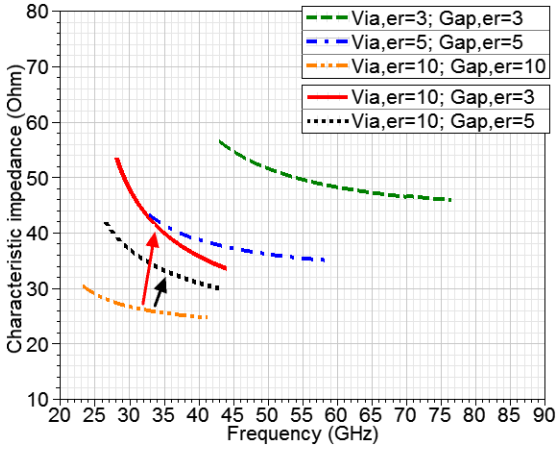
achieve a sufficient accuracy. In general, if the two layers hold the same ε_r, the characteristic impedance drops with an increased ε_r. Corresponding to Figure 2-3, the impedance is dependent on the gap-layer ε_r rather than the via-layer. Taking the solid red curve (via-layer $\varepsilon_r = 3$ and gap-layer $\varepsilon_r = 5$) in Figure 2-5 (a) for instance, which gets closer to the dotted-dashed blue curve (via-layer $\varepsilon_r = 5$ and gap-layer $\varepsilon_r = 5$), instead of keeping with the dashed green curve (via-layer $\varepsilon_r = 3$ and gap-layer $\varepsilon_r = 3$). It means that the via-layer of $\varepsilon_r = 3$ has a limited effect on the characteristic impedance. A similar behavior can be found in Figure 2-5 (b), in which the dotted black curve (via-layer $\varepsilon_r = 5$ and gap-layer $\varepsilon_r = 10$) is very close to the dotted-dotted-dashed yellow curve for via-layer $\varepsilon_r = 10$ and gap-layer $\varepsilon_r = 10$.



(a)



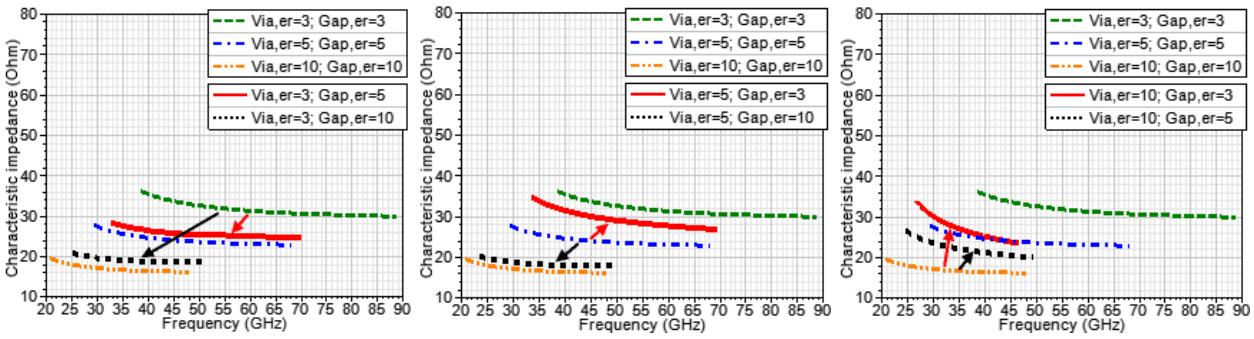
(b)



(c)

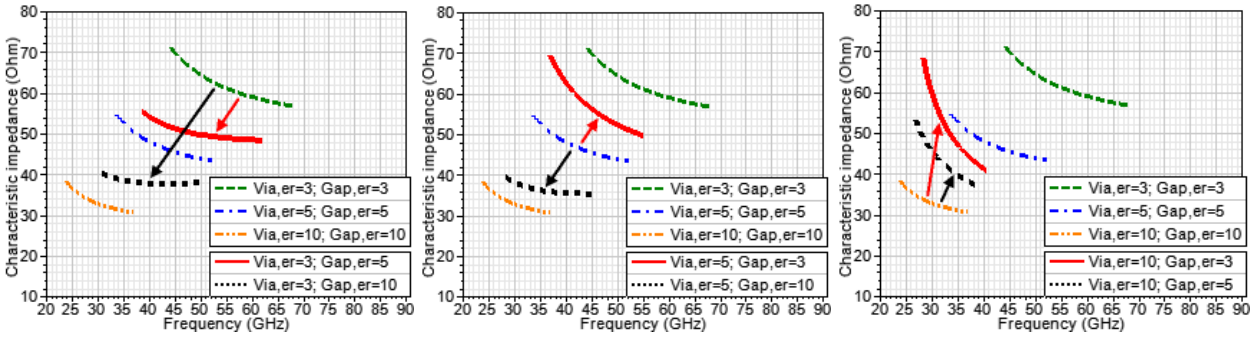
Figure 2-5 Change in SIGW characteristic impedance with a 0.254 mm gap height, but different substrates for the via- and gap-layers. (a) Via-layer $\varepsilon_r = 3$, and gap-layer $\varepsilon_r = 5$ or 10. (b) Via-layer $\varepsilon_r = 5$, and gap-layer $\varepsilon_r = 3$ or 10. (c) Via-layer $\varepsilon_r = 10$, and gap-layer $\varepsilon_r = 3$ or 5. In addition, the same substrate used for both via- and gap-layers also shown, i.e., $\varepsilon_r = 3$, 5, or 10.

However, as explained above, as part of the power is leaked into the via-layer substrate, the impact of the via-layer on the characteristic impedance cannot be ignored, especially when it is of higher ε_r. This is evident as presented by the solid red curve in Figure 2-5 (b) for the case of via-layer ε_r = 5 and gap-layer ε_r = 3, which is far away from the dashed green curve (via-layer ε_r = 3 and gap-layer ε_r = 3). This via-layer effect could be stronger if its ε_r is enlarged further, such as 10 indicated by the solid red curve in Figure 2-5 (c). As a result, the impedance flatness over frequencies is significantly degraded. Or in other words, in order to improve the flatness of the SIGW characteristic impedance over the band, the via-layer substrate ε_r cannot be much higher than the gap-layer ε_r, and the gap-layer with a relatively higher ε_r is useful to keep that flatness.



(a) (b) (c)

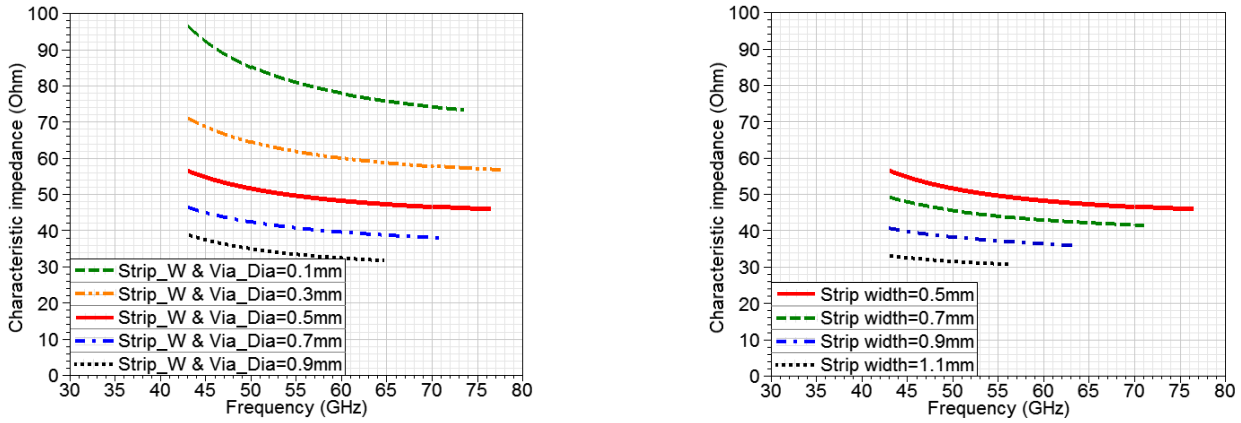
Figure 2-6 Change in SIGW characteristic impedance with a 0.127 mm gap height, but different substrates for the via- and gap-layers. (a) Via-layer ε_r = 3, and gap-layer ε_r = 5 or 10. (b) Via-layer ε_r = 5, and gap-layer ε_r = 3 or 10. (c) Via-layer ε_r = 10, and gap-layer ε_r = 3 or 5. In addition, the same substrate used for both via- and gap-layers also shown, i.e., ε_r = 3, 5, or 10.



(a) (b) (c)

Figure 2-7 Change in SIGW characteristic impedance with a 0.381 mm gap height, but different substrates for the via- and gap-layers. (a) Via-layer ε_r = 3, and gap-layer ε_r = 5 or 10. (b) Via-layer ε_r = 5, and gap-layer ε_r = 3 or 10. (c) Via-layer ε_r = 10, and gap-layer ε_r = 3 or 5. In addition, the same substrate used for both via- and gap-layers also shown, i.e., ε_r = 3, 5, or 10.

Another critical parameter in the SIGW characteristic impedance is the gap height, i.e., the gap-layer substrate thickness. So, two more gap heights of 0.127 and 0.381 mm are included in the study and presented in Figure 2-6 and Figure 2-7, respectively. Comparison of Figure 2-5, Figure 2-6, and Figure 2-7 reveals that a gap-layer with a smaller thickness is greatly helpful to keep a good impedance flatness over the band, as observed in Figure 2-6. It is valid even when the via-layer ε_r is much larger than the gap-layer ε_r. For example, the flatness over frequencies presented by the solid red curve in Figure 2-6 (c) for 0.127 mm gap is much better than the same ones in Figure 2-5 (c) and Figure 2-7 (c) for 0.254 and 0.381 mm gap, respectively. This implies that a thinner gap makes the power much more concentrated in the gap-layer and thus less power is leaked into the via-layer. It helps alleviate the via-layer effect. In addition, as indicated by the dashed green curves in Figure 2-6, an operation bandwidth of 50 GHz (from 38 to 88 GHz) is achieved, which is 12 GHz larger than the available bandwidth of the SIW in theory with the same low cutoff frequency of 38 GHz. Generally, to achieve a good flatness of the characteristic impedance for wideband implementations, a thinner gap-layer substrate with a relatively high ε_r is preferred.



(a) (b)

Figure 2-8 Change in SIGW characteristic impedance with metal strip width. (a) Diameter of the plated via connected to the strip keeps equal to the strip width. (b) Diameter of the plated via connected to the strip = 0.5 mm.

Figure 2-8 presents the effect of the strip width on the SIGW characteristic impedance, with a gap height of 0.254 mm and substrate ε_r of 3. This is necessary since it is different from the previous study in the microstrip line or stripline, in which no plated vias are connected to the metal strip. Two different cases are considered for the diameter of the plated vias keep equal to the strip width or be smaller than the width. As observed in both cases, a wider strip lowers the

characteristic impedances. The only found difference is that the falling range of impedance due to the increased strip width is shrunk if the diameter of the plated vias connected with the strip is fixed at 0.5 mm as shown in Figure 2-8 (b). In contrast, the impedance flatness over frequencies is not improved or degraded with the changed strip width, no matter if the diameter of the plated vias changes with the strip width or not. Of course, it is apparent that a strip width can be chosen for the desired SIGW characteristic impedance.

2.4 Study of Conductor and Dielectric Losses

2.4.1 Losses with Gap Height and Metal Strip Width

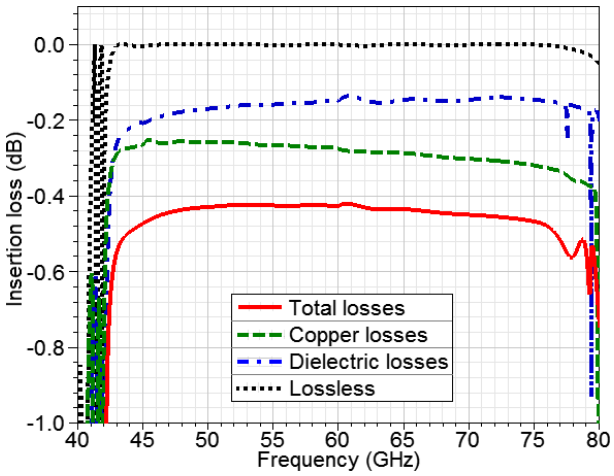


Figure 2-9 Comparison of different types of SIGW insertion loss.

The side power leakage from the gap between the PEC and PMC can be ignored when at least two rows of periodic pins are set [30]. The study for the conductor and dielectric losses in this section is also based on the SIGW in Figure 2-4, with the same dimensions and materials. Figure 2-9 is a general view of each contribution of conductor and dielectric losses to the total insertion loss of the SIGW. In the case considering copper losses only, the substrate loss tan δ is kept as 0. In the case of considering the dielectric losses with loss tan δ of 0.0012, the conductor is kept PEC. The case of lossless means no conductor and dielectric losses (i.e., loss tan δ = 0 and conductor = PEC). As observed, the insertion loss is primarily from the conductor losses, which even increase with frequencies. However, as presented in Figure 2-10, the conduction losses can be reduced by using a larger gap (i.e., thicker gap-layer substrate), for the lower

current density flowing in the conductor surface. The dielectric losses may keep constant with the varied gap heights as it is independent of the substrate thickness.

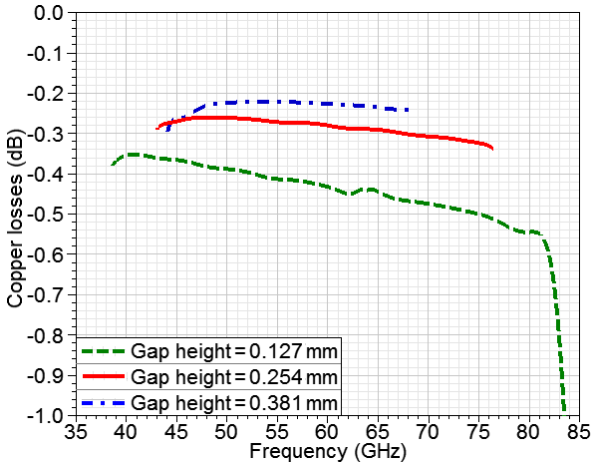
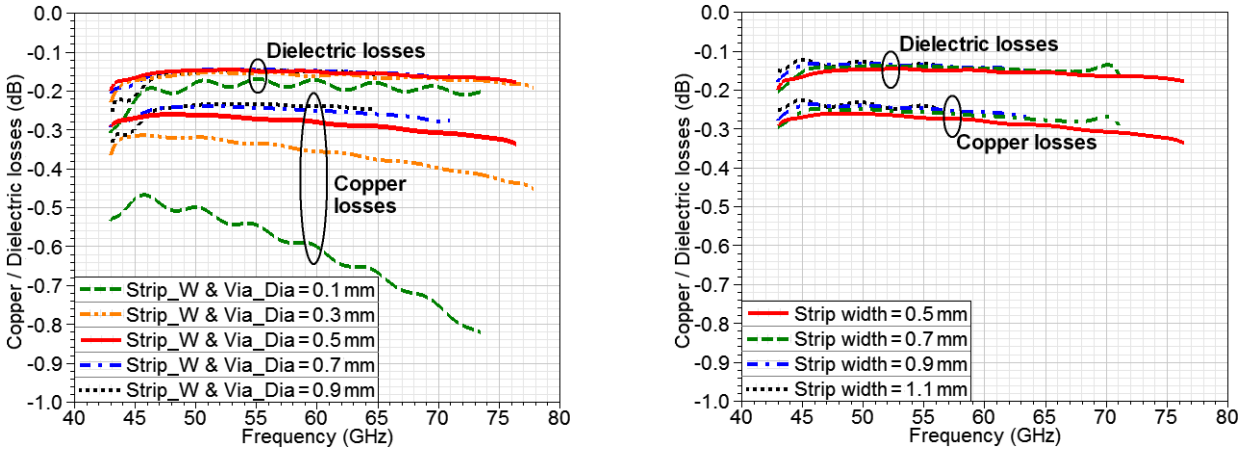


Figure 2-10 Change in the SIGW copper losses with gap height, i.e., thickness of gap-layer substrate.



(a) (b)

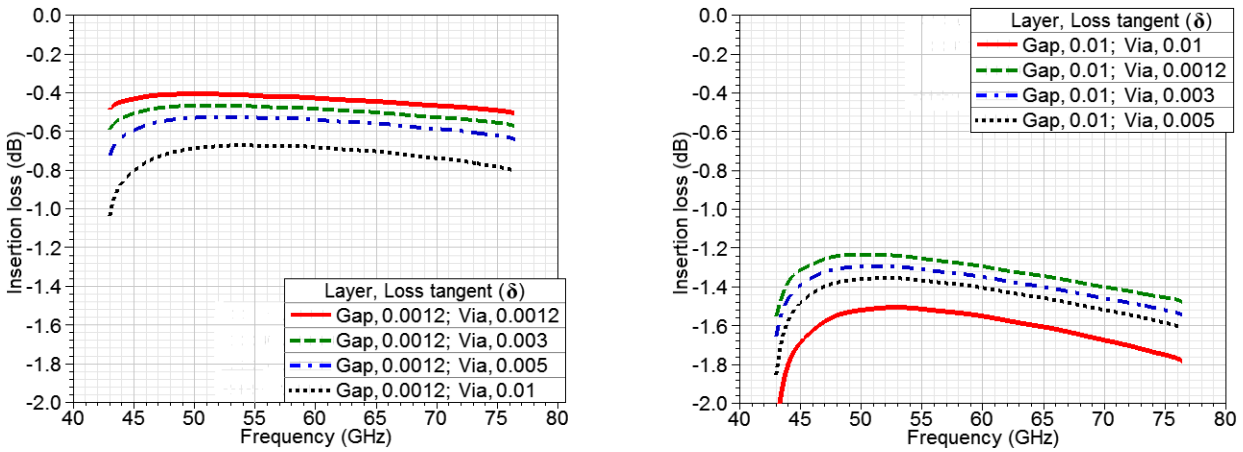
Figure 2-11 Change in the SIGW copper and dielectric losses with strip width. (a) Diameter of the plated vias connected to the strip keeps equal to the strip width. (b) Diameter of the plated vias connected to the strip = 0.5 mm.

Different from the microstrip line, lots of plated vias are connected to the metal strip. Their effects on the conductor and dielectric losses are presented in Figure 2-11. Initially, if the diameter of the plated vias connected to the strip keeps equal to the strip width, Figure 2-11 (a) shows that a narrower strip significantly increases the conduction losses. However, Figure 2-11 (b) shows the conduction losses have no evident dependence on the strip width if the diameter of the connected plated vias is fixed as 0.5 mm, smaller than the strip width. The fact is that the higher edge current of the strip is able to flow strongly to those plated vias connected to the

metal strip when the strip and vias have the same dimension. This results in the increased conduction losses. The length of the SIGW was also under study and found that the conduction and dielectric losses are both increased by around two times over the values in Figure 2-10 and Figure 2-11 if the length is two times longer than that in Figure 2-4. Therefore, to minimize the insertion loss of the SIGW, a larger gap, a wider strip, and a shorter length are preferred.

2.4.2 Losses with Substrate Dielectric Loss Tan δ

Since two-layer substrates are used, and part of the power may leak into the via-layer, it is necessary to study the loss of the SIGW when the gap- and via-layers are of different dielectric loss tan δ. The study is presented in Figure 2-12, considering four tan δ for the via-layer: 0.0012, 0.003, 0.005 or 0.01. The tan δ of the gap-layer is fixed at 0.0012 or 0.01. The copper losses are counted in the simulated results for a more real situation, but they are constant due to the fixed dimensions and materials. Figure 2-12 (a) shows that, although the losses are dominated by the gap-layer in which the wave is concentrated, the dielectric losses due to the via-layer can be high if it has a high loss tan δ, such as 0.01 indicated by the dotted black curve. Or on the other hand, the loss due to a high tan δ of the gap-layer can be alleviated by using a lower tan δ in the via-layer.



(a) (b)

Figure 2-12 Change in the SIGW insertion loss for the via- and gap-layers with different dielectric loss tan δ. (a) Gap-layer loss tan δ = 0.0012, and via-layer loss tan δ = 0.003, 0.005, or 0.01. (b) Gap-layer loss tan δ = 0.01, and via-layer loss tan δ = 0.0012, 0.003, or 0.005.

The above study in Sections 2.3 and 2.4 gives a general design guideline for the SIGW. Primarily, ε_r, loss tan δ, and thickness of the gap-layer substrate should be first selected for the desired characteristic impedance, loss performance, and operation bandwidth of the SIGW. For wideband applications, a thinner gap-layer is preferred for the larger band gap size and better impedance flatness over frequencies. However, a thinner gap-layer leads to increased conduction losses. This is a tradeoff, and a compromise should be made in the design. Also, a wider strip is able to reduce the conductor losses. However, it lowers the characteristic impedance of the SIGW which could not be the desired value. Besides, more attention should be paid to the via-layer if it is of high ε_r or tan δ. As proven above, if the via-layer ε_r is higher than the gap-layer ε_r, the SIGW characteristic impedance set up by the gap-layer can be badly changed, and the impedance flatness over frequencies is degraded. And, more dielectric losses may be caused if the via-layer of a high tan δ, since part of the power is able to leak into this layer. Currently, a theoretical analysis of a GW structure is very complicated [31]-[34], so the parametric study method based on the commercial software, such as HFSS or CST, is employed to make the desired design.

2.5 Connection between SIGW and Microstrip Line

The connection of the SIGW to the microstrip line is necessary for the measurement and integration to microstrip circuits. The conventional tapered microstrip transition is considered first in this study. But it will further verify that such an additional transition part is unnecessary for the SIGW, which will be significant in the circuit design and compactness.

2.5.1 Conventional Tapered Microstrip Transition

Based on the previous design presented in Figure 2-4, an SIGW with tapered microstrip transitions at the input and output is shown in Figure 2-13. Since it will be fabricated by the PCB process, a circular metal pad is attached to the plated via end due to its metalized process. The diameter of all the vias is 0.5 mm. The pad diameter is 1.008 mm for the process requirement of 0.254 mm spacing between the hole edge and copper edge. Thus, the period of the plated vias is increased to 1.262 mm to separate the adjacent pads sufficiently. Also, the strip width is enlarged to 1.008 mm, due to 0.5 mm diameter of the plated vias connected to the strip and the required spacing of 0.254 mm. The lower gap-layer substrate is Rogers RT/Duroid 6002 of 0.254 mm thickness, and it is 5 mm longer than the upper via-layer at the input and output, respectively, to

place the microstrip feed line and transition. The via-layer is to build the PMC surface, including two cases: Rogers RT/Duroid 6002 of 0.762 mm thickness and RT/Duroid 6006 of 0.635 mm thickness (ε_r = 6.15 and loss tan δ = 0.0027). Those two SIGWs are corresponding to the above study of the gap- and via-layers using the same or different substrates. The spacing of the plated vias connected to strip is increased to move the start and end vias closer to the strip edge in the upper substrate, which is able to improve the transition performance further.

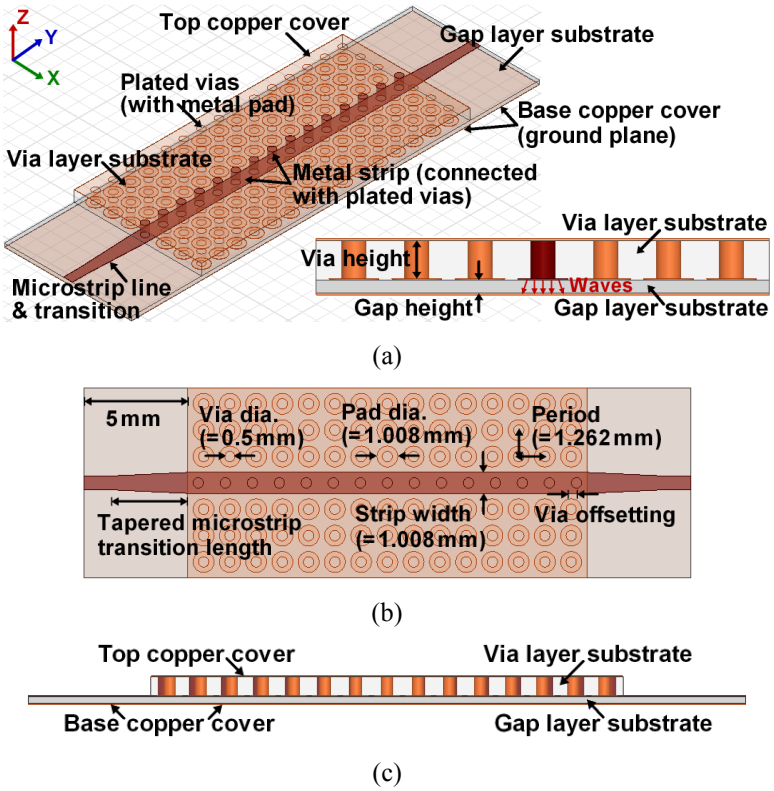
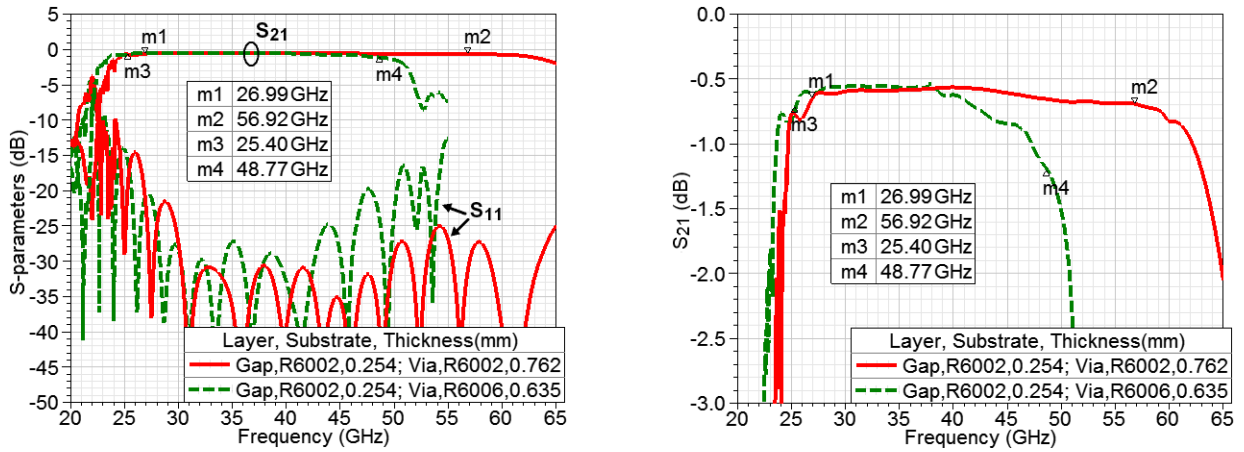


Figure 2-13 SIGW with transitions to microstrip lines. (a) Overview and front/back view. (b) Top view. (c) Side view.

The passband for the SIGW using Rogers RT/Duroid 6002 for both via- and gap-layers is from 26.99 to 56.92 GHz. The input-output microstrip line width is then fixed at 0.64 mm for 50 Ω at about the passband center frequency. The optimal length of the tapered microstrip transition is 4.05 mm for the best transmission performance over the band, which is shown as the solid red curve in Figure 2-14. The reflection within the passband is below -25 dB, and even lower in the middle of the band, which means a proper impedance matching achieved between the SIGW and microstrip lines. The second SIGW, using Rogers RT/Duroid 6002 and 6006 for the gap- and via-layers, respectively, has a passband from 25.40 to 48.77 GHz. The microstrip feed line width

is 0.638 mm for 50 Ω at around the passband center frequency. The simulated performance is presented by the dashed green curve in Figure 2-14, with an optimized transition length of 3.9 mm. It is seen that within the passband the return loss, S_{11}, is mostly below -25 dB and better at the middle passband. Compared to the shown solid red curve for the first SIGW, however, it can also be found that the reflection performance of the second SIGW is degraded in the overall passband. It can be explained by the previous study – the via-layer substrate $\varepsilon_r = 6.15$ higher than the gap-layer $\varepsilon_r = 2.94$ degrades the SIGW characteristic impedance flatness over the frequencies, as indicated by the solid red curve in Figure 2-5 (b). As a result, the tapered microstrip transition cannot offer such a wideband impedance matching.



(a) (b)

Figure 2-14 Simulated performance of the tapered microstrip transitions for the SIGW with the same or different substrates for the gap- and via-layers. (a) S_{11} and S_{21}. (b) Zoom-in S_{21}.

2.5.2 Connection without Additional External Transition

The above constructed transition utilizes the tapered microstrip line and the plated via at the input and output for the desired performance. The reason for such a complicated transition is because of the SIGW small characteristic impedance. The enlarged strip width from 0.5 to 1.008 mm for the required spacing of 0.254 mm makes the characteristic impedance lower than 40 Ω over the most of the passband. Therefore, if the SIGW is properly designed with a characteristic impedance closer to 50 Ω, the additional external tapered microstrip transition can be minimized or removed totally. One example is presented in Figure 2-15 (a), in which no transition structure is added at the input and output. The via-layer substrate is Rogers RT/Duroid 6002 of 0.508 mm thickness, and the gap-layer substrate is Rogers RT/Duroid 5880 of 0.254 mm thickness. The

diameter of the plated vias and metal pads is 0.254 and 0.762 mm, respectively, with a period of 1.016 mm. The obtained passband is from 35.2 to 76.2 GHz under the above given conditions.

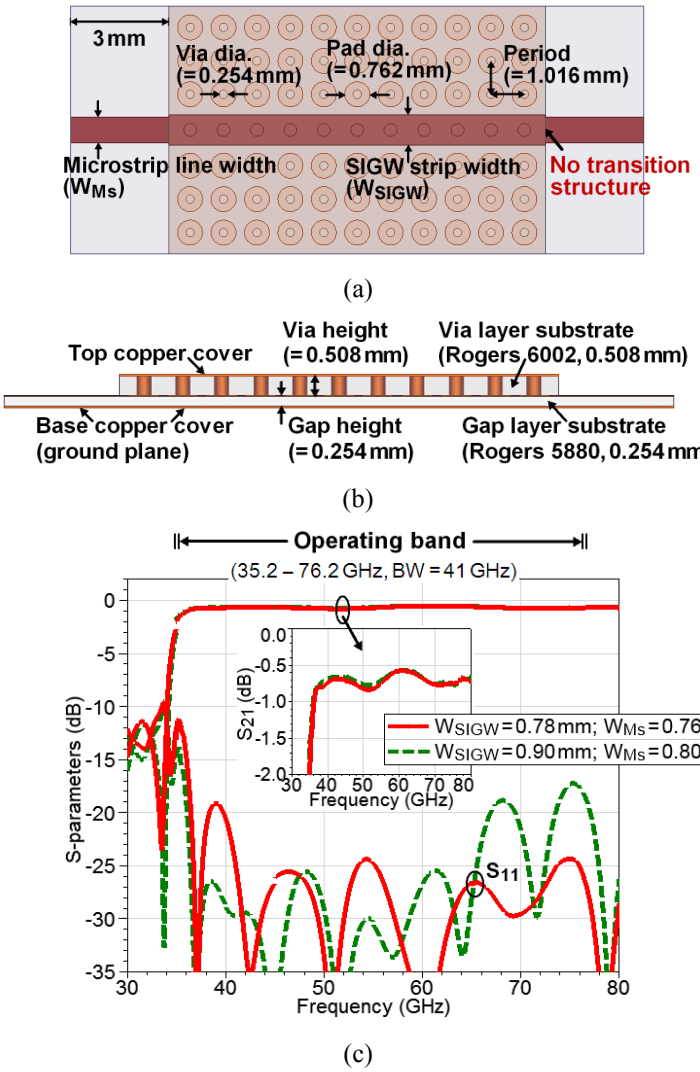
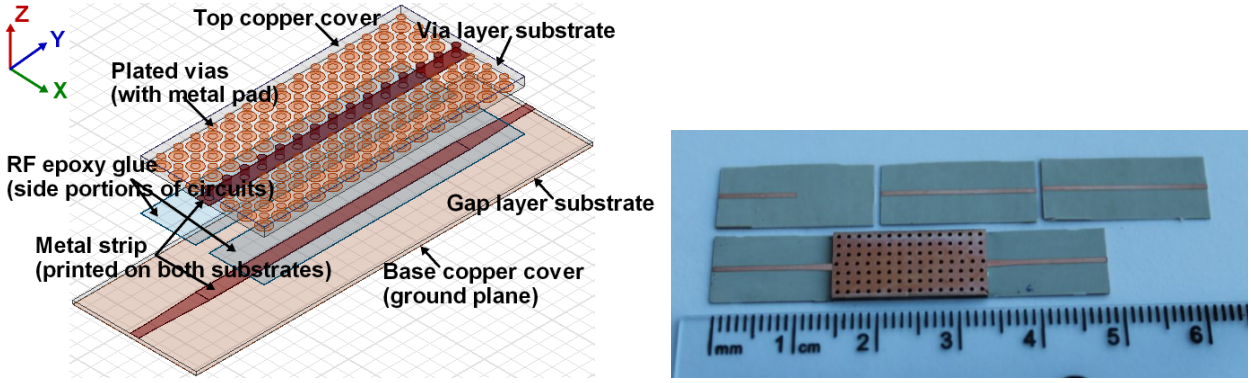


Figure 2-15 SIGW without additional external transitions to the microstrip lines. (a) Top view of the circuit. (b) Side view of the circuit. (c) Simulated S_{11} and S_{21}.

The simulated results are presented in Figure 2-15 (c), including two designs. One SIGW has a strip width of 0.9 mm, offering a characteristic impedance of 50 Ω at the above passband center frequency of 55.7 GHz. The other has a strip width of 0.78 mm, giving a characteristic impedance of 55 Ω at 55.7 GHz. It is seen that combined with a proper width of the microstrip feed line; it is available to obtain the desired impedance matching over broadband. The SIGW of 0.9 mm strip width has a lower reflection at the lower band as shown by the dashed green curve; while the one of 0.78 mm strip width is presented better at the higher frequencies. The microstrip

line of 50 Ω at 55.7 GHz has a 0.765 mm width. The achieved broadband impedance matching between the SIGW and microstrip lines without additional transition structures is because the wave of both guiding structures is all concentrated in the lower gap-layer substrate. As a result, the strip widths of the SIGW and the microstrip line are almost equal to a given characteristic impedance. This is significant in the circuit design and compactness over the stripline or SIW.

2.6 Prototypes and Measurement



(a) (b)

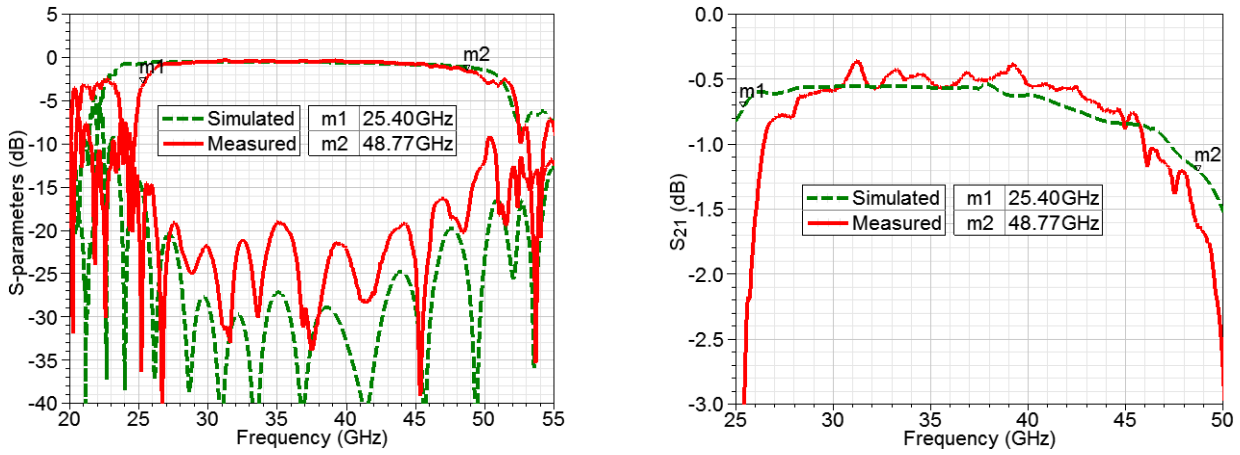
(c)

Figure 2-16 Prototype and measurement setup. (a) Distributed 3-D view of the fabrication for the designed SIGW. (b) Photo of the fabricated SIGW with the tapered microstrip transitions, including TRL calibration kits. (c) Photo of the measurement set-up.

The SIGW presented in Figure 2-13 with an additional tapered microstrip transition has been fabricated and shown in Figure 2-16 (b). The used substrates for the gap- and via-layers are

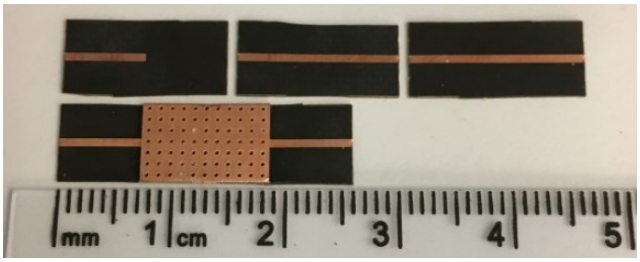
Rogers RT/Duroid 6002 and 6006, respectively. The process is fully based on the low-cost multi-layer PCB technology, as illustrated in Figure 2-16 (a). The plated via in the top-layer substrate and the metal strips on both layers are first processed, and then the two substrates are stuck together using a thin layer RF glue with high temperature and pressure. The metal strip is printed on both the substrates – on the top of the lower layer and at the base of the upper layer. In the fabrication, the glue is located only in the side portions of the circuits to guarantee the electrical contact between the metal strips. The glue thickness is 5 um, much thinner than the copper foil thickness of 18 um, and thus a tight contact between the strips can be guaranteed. With this built strip-ridge, the wave in the SIGW will no longer interact with the plated vias in the strip and the high-loss ENIG coating. This is advanced over the reported microstrip-ridge GW. Moreover, as seen, stable gap performance is also guaranteed in the SIGW with the gap-layer substrate, rather than the unstable air gap in the microstrip-ridge GW or other GW structures. This is significant for a large circuit, such as a feeding network for a big antenna array. The length of the bottom substrate of the fabricated SIGW in Figure 2-16 (b) is 20 mm longer than the original design in Figure 2-13, which is for the Thru-Reflect-Line (TRL) calibration to remove the effects of the test fixture in measurements. The fabricated microstrip calibration kit is shown in Figure 2-16 (b). It includes: 1) a thru of 20 mm length; 2) an open circuit with a microstrip of 10 mm length, i.e., half-length of the thru; and 3) a line which is 1.297 mm longer than the thru, corresponding to a quarter wavelength at 37 GHz. The substrate of all the kit circuits is Rogers RT/Duroid 6002 of 0.254 mm thickness, the same as the bottom substrate of this fabricated SIGW. The measured S-parameters from a vector network analyzer (VNA) are shown in Figure 2-17, which agree well with the simulated results, in both bandwidth and inband performance.

The SIGW in Figure 2-15 (a) without the external transition has also been fabricated and shown in Figure 2-18 (a), in which W_{SIGW} = 0.78 mm and W_{MS} = 0.76 mm. The TRL calibration kit contains 1) a thru of 15 mm length; 2) an open circuit with a microstrip of 7.5 mm length, i.e., half-length of the thru; and 3) a line that is 1.115 mm longer than the thru, corresponding to a quarter wavelength at 48.5 GHz. These microstrip kit circuits use the same substrate as the base substrate of this SIGW, i.e., Rogers RT/Duroid 5880 of 0.254 mm thickness. The measured S-parameters are given in Figure 2-17 (b). The measured results are only up to 67 GHz, due to the test frequency of the available test fixture and VNA. While the measured and simulation results also present quite good agreement over broadband.

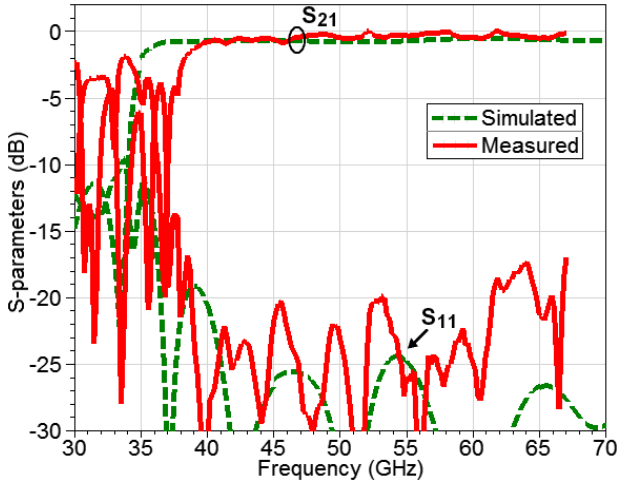


(a) (b)

Figure 2-17 Measured S-parameters of the fabricated SIGW, compared with the simulated. (a) S_{11} and S_{21}. (b) Zoom-in S_{21}.



(a)



(b)

Figure 2-18 Fabrication and measurement. (a) Photo of the fabricated SIGW without additional external transition to microstrip lines (W_{SIGW} = 0.78 mm and W_{MS} = 0.76 mm), including TRL calibration kits. (b) Measured and simulated S_{11} and S_{21}.

The differences between the measured and simulated results observed in Figure 2-17 and Figure 2-18 (b) could be possible from the used glue that is difficult to accurately model in the simulation. Another possible factor is the base-layer substrate of 0.254 mm thickness, which is too soft and its deformation could cause errors in measurements. Besides, fabrication tolerance, metal surface roughness, and substrate frequency-dependent ε_r and tan δ could also possibly cause the presented differences between the measured and simulated results.

2.7 Study of Bend Discontinuities in SIGW

A straight-through SIGW without bends has been previously presented above. However, many discontinuities are naturally present in any actual microwave circuits, such as power dividers and a feeding network for antenna arrays. Therefore, it is of great interest and necessary to study the discontinuity of the strip-ridge bend, thus offering guidelines for design. This study is different from the discontinuity in the classic microstrip line, in which no plated vias are connected to the metal strip. A solution is proposed additionally to improve the bend discontinuity. This solution is much simpler than the one shown in [18] for the microstrip-ridge GW, which has to fine tune up to three sets of vias at the bend and even each set contains at least three vias. Moreover, much better return loss, S_{11}, over a wider band is obtained with the proposed method.

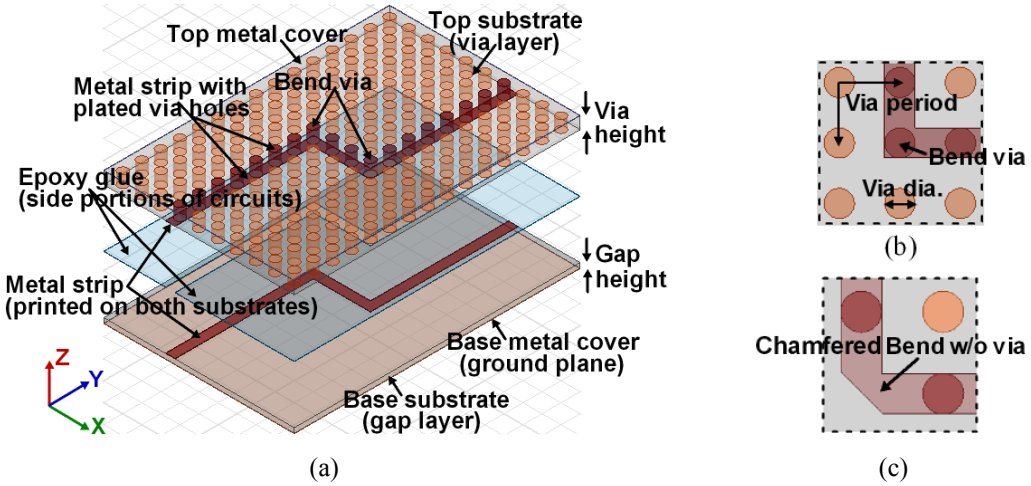


Figure 2-19 SIGW with a double 90º bend. (a) Distributed 3D view. (b) Zoomed unmodified bend. (c) Zoomed chamfered bend without via. All the via holes are copper plated.

An SIGW with two 90º bends is shown in Figure 2-19. The PMC is realized by periodic plated vias, which are about 0.762 mm height, 0.5 mm diameter, 1.0 mm period, and 0.127 mm gap to the base ground plane. The copper strip-ridge has a width of 0.5 mm and is connected to the plated vias on it. The substrate is Rogers RT/ Duroid 6002 with ε_r of 2.94 and tan δ of 0.0012. Figure 2-20 presents that the bends discontinuities badly degrade the transmission performance within the generated passband from around 39 to 87 GHz. It is also evident that chamfering the bend is no more helpful, if the bend via is removed. Instead, a resonant mode (around 73 GHz) is formed inside the via-removed cavity at the bend, as shown by the dotted-dashed blue curves in Figure 2-20. The chamfered right-angle bend without bend via is illustrated in Figure 2-19 (c).

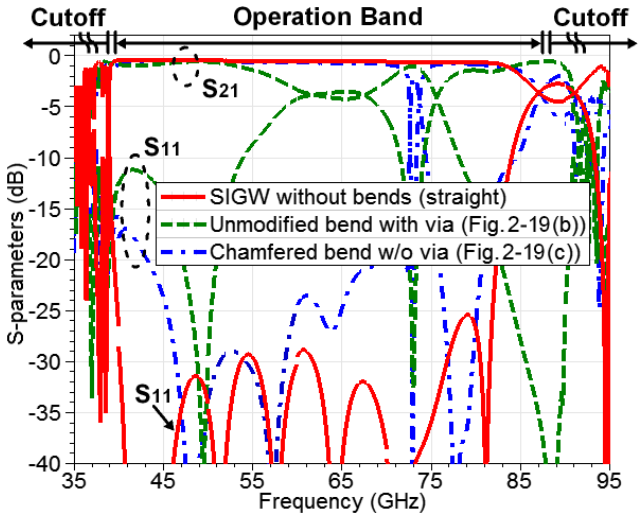


Figure 2-20 Simulated S-parameters of an SIGW with a double 90º bend: with or without the bend vias indicated in Figure 2-19.

2.7.1 Chamfered Right-Angle Bend

To address the issues shown in Figure 2-20, a plated via is added to the chamfered strip bend, as illustrated in Figure 2-21. It is seen that the cavity resonance is suppressed. And, with $D_{\text{bend-via}}$ = 0.335 mm and L_{bend} = 0.525 mm, the achieved performance shown by the solid red curves in Figure 2-21 agrees well with the straight case without bends indicated by the dotted black curves. Moreover, no additional insertion loss, S_{21}, is caused. In addition, Figure 2-21 reveals the effects of the diameter of the bend via, $D_{\text{bend-via}}$, and indicates that $D_{\text{bend-via}}$ should be kept large enough to ensure a good electrical contact between the strip bend and base ground

plane. Otherwise, the cavity resonance could not be effectively inhibited. Note that, a proper ratio of L_{bend} and $D_{bend\text{-}via}$ is the critical factor in minimizing the bend discontinuities.

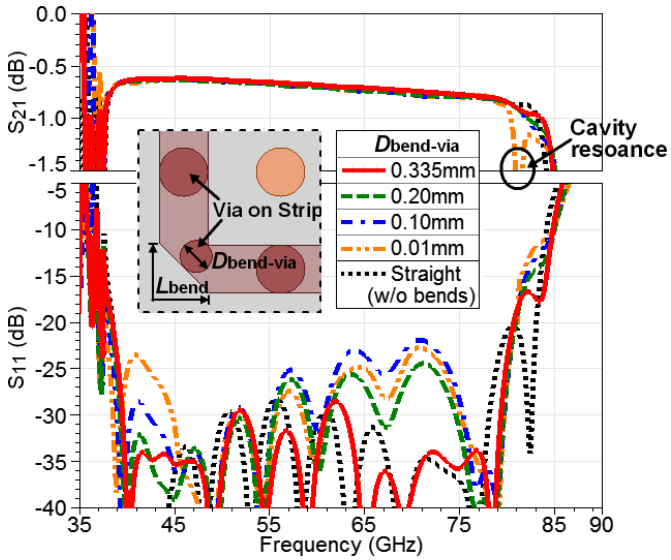
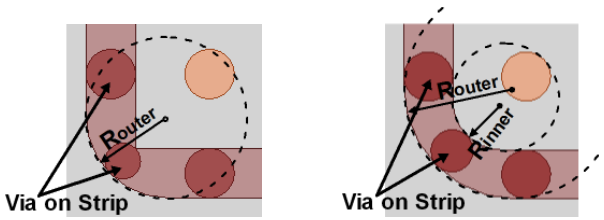


Figure 2-21 Simulated S-parameters of an SIGW with double chamfered right-angle bends: diameter of the bend via is varied, compared to the straight case.

2.7.2 Curved Right-Angle Bend

In addition to the chamfered right-angle bend, another configuration of the curved right-angle bend is also included in the study, considering two different types shown in Figure 2-22: curved outer edge, and both curved inner and outer edges. The performance of these two curved-bend types is compared in Figure 2-23, with two different cases for the second type in Figure 2-22 (b). The optimized dimensions of the bends (curve radius and bend via diameter) are given in Table 2-1, in which $D_{bend\text{-}via}$ is set as large as touching the bends curved edges to guarantee electrical contact as explained previously.



(a) (b)

Figure 2-22 Two different types of curved right-angle bend configuration. (a) Curved outer edge. (b) Both curved inner and outer edges.

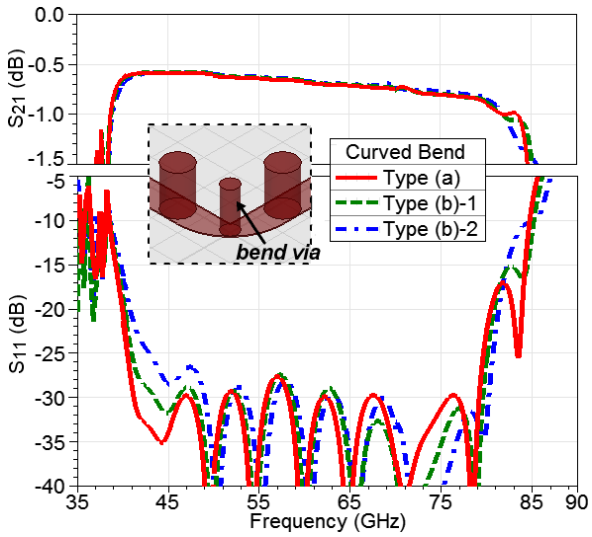


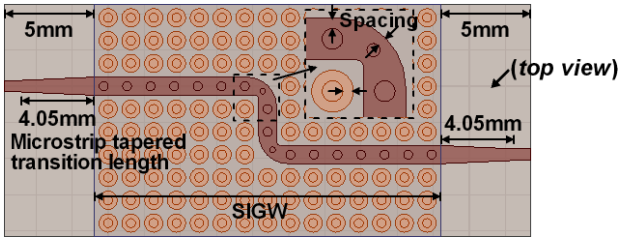
Figure 2-23 Simulated S-parameters of an SIGW with two curved right-angle bends shown in Figure 2-22, and with dimensions given in Table 2-1.

Table 2-1 Dimensions of curved right-angle bends and bend via.

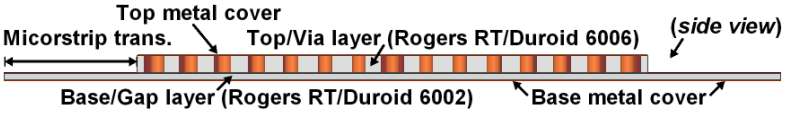
Type	R_{outer} (mm)	R_{inner} (mm)	$D_{bend\text{-}via}$ (mm)
(a)	0.83	---	0.18
(b)-1	0.92	0.20	0.20
(b)-2	1.15	0.50	0.215

Except the ones indicated in Table 2-1, the other dimensions for this SIGW with curved right-angle bends are kept the same as defined previously. Figure 2-23 presents that almost the same performance in insertion loss and return loss is achieved for the three curved configurations. Comparing to the chamfered bend in Figure 2-21, no distinct advantages of the curved types is observed. Therefore, for design simplicity, a chamfered right-angle bend with a proper plated via is effectively enough to minimize the bend discontinuities and achieve the desired performance. However, for a given $D_{bend\text{-}via}$, if a larger R_{outer} (or L_{bend}) is required to improve the performance, the curved bend type shown in Figure 2-22 (b) could be the only choice, since the bend inner curved edge allows the bend via to have a larger diameter.

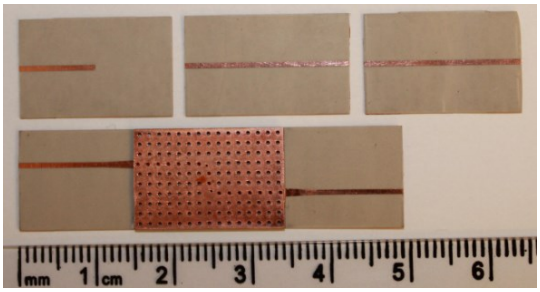
2.7.3 Experimental Verification and Analysis



(a)



(b)



(c)

Figure 2-24 SIGW with two curved right-angle bends and transition to microstrip lines. (a) Top view. (b) Side view. (c) Photo of the fabricated SIGW with TRL calibration circuits. The circuit bottom is fully covered by the copper.

To experimentally demonstrate the presented solution to the SIGW strip-bend, an SIGW with a double 90º bend has been fabricated by PCB technology. The adopted bend configuration is the one shown in Figure 2-22 (b) to allow a larger R_{outer}. This is due to the PCB two fabrication limitations: 1) the minimum diameter of plated via is half of the substrate thickness, and 2) the minimum spacing between the hole edge and copper edge is 0.254 mm. Thus, the initial structure in Figure 2-19 is modified as shown in Figure 2-24 (a): a period of 1.262 mm and a strip width of 1.008 mm. Additional circular metal pads of 1.008 mm diameter are attached to the plated vias. The dimensions of the bend edges and vias are re-optimized as: R_{outer} = 1.65 mm, R_{inner} = 0.205 mm, $D_{\text{bend-via}}$ = 0.319 mm. The tapered microstrip transitions from the SIGW to microstrip lines are designed for later measurements. Also, the thickness of the gap-layer (i.e., Rogers RT/Duroid 6002) is increased to 0.254 mm to enhance its mechanical strength in practice. The top substrate is replaced by Rogers RT/Duroid 6006 of 0.635 mm thickness (ε_r = 6.15; tan δ = 0.0027). The purpose is to provide verification for a more general case of the gap- and via-layers of the SIGW

using different substrates. Due to the implemented via pads, a thicker gap-layer, a smaller via height, and higher ε_r of the via-layer, the generated passband is now from around 25 to 50 GHz.

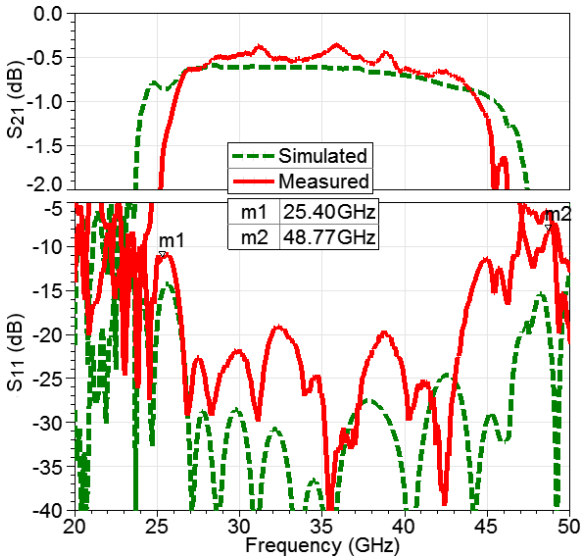


Figure 2-25 Measured results of the fabricated SIGW with double curved right-angle bends, compared with the simulated.

The metal strip is printed on both of the substrates – on the top of the gap-layer and at the lower part of the via-layer, as illustrated in Figure 2-19 (a). Then, the two substrates are stuck together using a thin layer RF glue, which is located only on the side portions of the circuit to ensure the electrical contact between the metal strips. The photo of the fabricated SIGW circuit is shown in Figure 2-24 (c). The length of the bottom substrate is 20 mm longer than the design in Figure 2-24 (a) for the TRL calibration to remove the effects of the test fixture in measurements. The measured results presented in Figure 2-25 are in good agreement with the simulated results. The transmission and reflection coefficients are at the same level of the measured performance of the SIGW without bends presented in Figure 2-17. The differences observed between the measured and simulated results could be possible due to the RF glue, fabrication tolerances, measurement uncertainty, and substrate frequency-dependent ε_r and tan δ, which were not considered in the simulations.

2.8 Conclusion

In this chapter, a novel miniaturized gap waveguide, named as a substrate integrated gap waveguide (SIGW), is presented and realized. It is fully based on the low-cost PCB technology and totally avoids the defects inherent in the microstrip-ridge GW or inverted microstrip GW, such as the high-loss ENIG coating, plated vias in the strip, unstable air gap, or integration issue. The SIGW is also advanced over the microstrip line and stripline for its lower conduction losses and without the undesired radiation, surface waves, or higher order modes. Moreover, no external transition is required for the SIGW when integrating with microstrip feed lines, which makes the SIGW more compatible and compacted in the circuit than the SIW. The fundamental TE_{10} mode of the SIW causes mode conversion losses when connecting with other TEM/quasi-TEM lines. It has also been proven that a wider operation bandwidth is available with the SIGW than the SIW. A design guideline has been offered after the careful study of the characteristic impedance and conductor and dielectric losses of the SIGW, considering both structure dimensions and substrate property. The SIGW has been demonstrated with two fabricated prototypes, considering with or without an external transition part to microstrip feed lines. Further, the discontinuity of the strip-ridge bend in SIGW has also been studied, which is necessary to realize future feeding networks for SIGW antenna arrays or other types of cost-effective SIGW passive components, in which many discontinuities are naturally present. Two different configurations – chamfered and curved right-angle bends – are included in the study. It has been proven that with a proper ratio of the chamfered length and the bend via diameter, the bend caused discontinuities can be minimized and achieve the desired transmission performance. The experimental verification for this solution has also been presented with a fabricated SIGW of two 90º bends.

Chapter 3 Broadband 60 GHz Antennas Fed by SIGW

3.1 Introduction

The GW technology has been used to excite antenna arrays at mm-wave frequencies with excellent radiation characteristics, such as wide- and narrow-slot antennas [7], [35]-[38], a patch antenna [39], and a leaky wave antenna [40]. However, the size and weight prevent the original GW from low-cost and low-profile implementations. As introduced previously, the PCB-based microstrip-ridge GW and inverted microstrip GW have significantly reduced the size and weight. However, the inherent defects of plated vias in the strip, high-loss ENIG coating, unstable air gap, and difficult integration apparently will limit the antenna performance and compatibility. Also, because of the wave propagating in the air and the low ε_r, the width of the feeding strip-ridge is large. This could make the spacing between the feeding ends to the array elements greater than a wavelength, causing the problem of grating lobes [19], [41]. Considering microstrip lines, the radiation and surface waves will badly degrade the antenna efficiency and radiation patterns [42]-[46]. The high attenuation of the stripline due to its narrower strip as well as the unwanted high order waveguide modes due to any vertical asymmetry will also limit the stripline in the implementation of antenna arrays. Therefore, the SIGW introduced in Chapter 2 is promising in the antenna design at microwave/mm-wave bands.

The first antenna constructed on the SIGW will be presented in this chapter. In addition, a bandwidth enhancement method is proposed by tuning the cavity exciting the slot antenna. It will offer a broadband impedance transition between the low characteristic impedance of the feed line and the high radiation impedance. The achieved bandwidth can be more than 21 GHz centered at 60 GHz (35%). This method is entirely different from the conventional ones previously used in the GW-based antennas, such as the T-shaped metal ridge [7], [19], [40], [41], ellipse-shaped slots [47], rotated rectangle slots [40], offset feeding [48], or dielectric superstrates placed above the slot [49], [50], which are originated from the microstrip antennas. The SIGW slot antenna and the bandwidth enhancement method are introduced first. Further, an improved configuration is presented with better bandwidth performance. A single-slot antenna and a 4-slot linear antenna array at 60 GHz have been fabricated and measured to verify the simulated results.

3.2 SIGW Slot Antenna and Bandwidth Enhancement Method

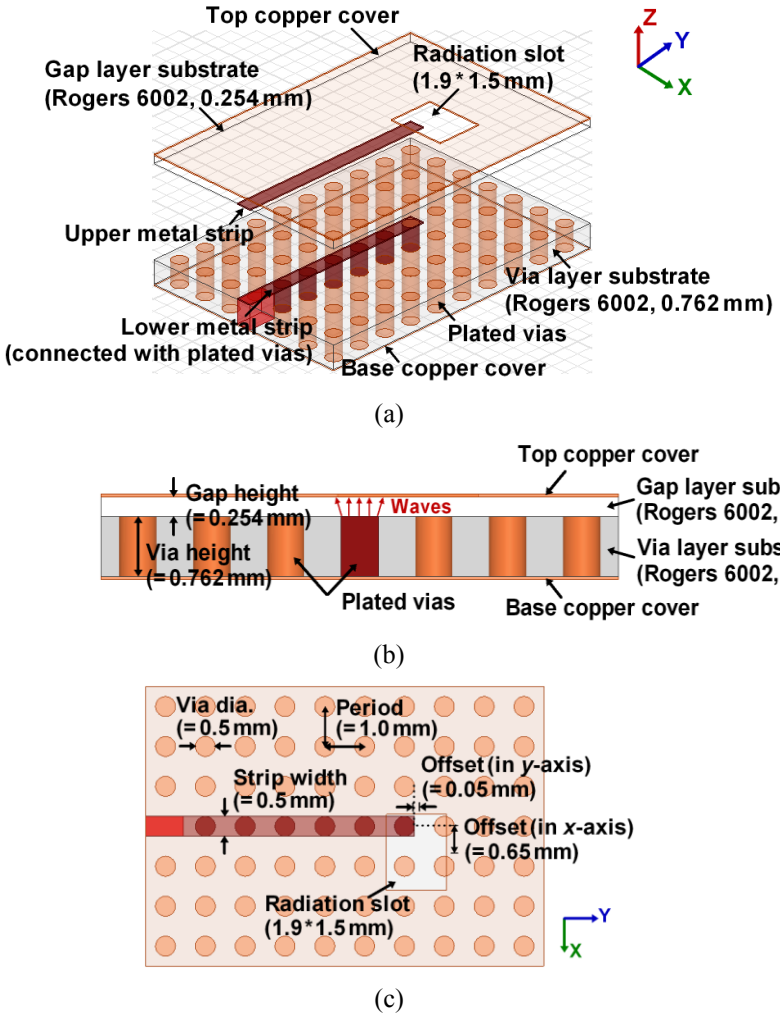


Figure 3-1 Slot antenna fed by SIGW, composed of periodic plated vias, a conducting strip-ridge, and two substrates. The top of the upper substrate (gap-layer) and the base of the lower substrate (via-layer) are fully covered with copper. (a) Distributed overview. (b) Front view. (c) Top view.

A single-slot antenna based on the SIGW is presented in Figure 3-1. The gap- and PMC-layers of the SIGW use Rogers RT/Duroid 6002 (ε_r = 2.94; tan δ = 0.0012). The radiating slot in the top metal cover is over the copper feed strip, which is connected to the base ground by the plated vias. The computed dispersion diagram of Figure 3-2 shows that the operation band of the SIGW is from 43.0 to 76.4 GHz, with the dimensions given in Figure 3-1. As seen, a quasi-TEM mode, shown by the solid red line, is generated between the lower and upper cutoff frequencies. The light line indicating a pure TEM mode in the substrate is illustrated by the dashed black line in Figure 3-2.

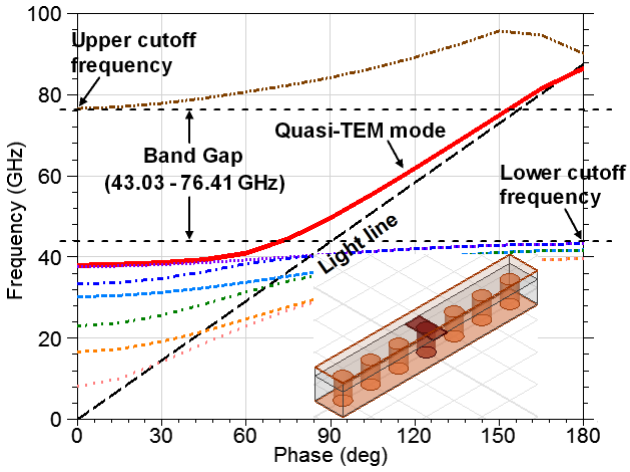


Figure 3-2 Dispersion diagram of the SIGW row cell with a metal strip connected to the base ground and the plated via under it. Periodic plated vias of 0.5 mm diameter, 1.0 mm period, 0.762 mm height, and 0.254 mm gap to the top copper cover. The dielectric substrate is Rogers RT/Duroid 6002.

Initially, to improve the bandwidth of the SIGW antenna, the offset feeding as commonly used in conventional microstrip antennas is employed, as presented in Figure 3-1. However, the maximum achieved bandwidth is only 6.08 GHz for 10 dB return loss, with 0.65 and 0.05 mm offset in the *x*- and *y*-direction, respectively, as observed from Figure 3-3.

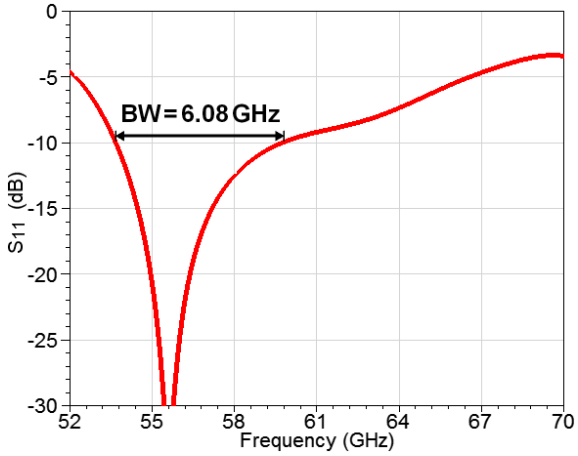


Figure 3-3 Simulated reflection coefficients, S11, of the slot antenna in Figure 3-1 with 0.65 and 0.05 mm in the *x*- and *y*-axis, respectively.

To overcome this limitation for a wider bandwidth, a unique method is proposed as presented in Figure 3-4 (a). The four sets of the plated vias next to the end of the strip feed line, i.e., "U_1", "T_1", "L_1", and "L_2", are exploited and moved to activate and tune the cavity under the slot. As a result, the cavity with the slot becomes the radiating mechanism of the antenna.

Thereby, besides the slot resonance itself, there is the second resonance effect introduced by the cavity. The resonances from the slot and the cavity appear to be close to each other that benefits the bandwidth.

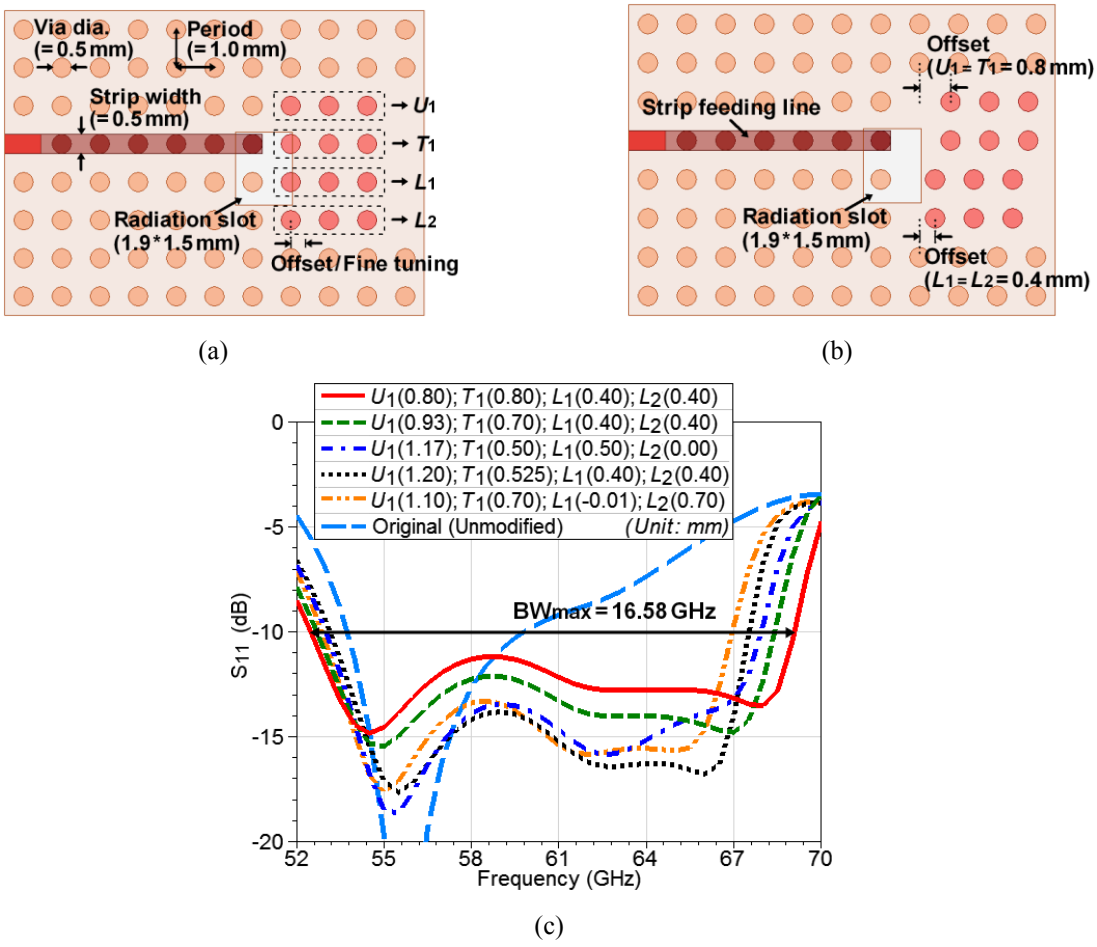


Figure 3-4 Slot antenna excited by SIGW for bandwidth enhancement by fine tuning the plated vias next to the strip feeding line end. (a) Top view. (b) Top view of U_1 = 0.8 mm, T_1 = 0.8 mm, L_1 = 0.4 mm, and L_2 = 0.4 mm. (c) Simulated reflection coefficient, S_{11}, with different fine-tuning offsets. For comparison, the antenna without fine-tuning of the plated vias is also shown.

Each set of the plated vias can be moved independently or with others synchronously, creating various fine-tuning schemes achieving different bandwidth performance. For example, the maximum bandwidth of 16.58 GHz for 10 dB return loss, presented by the solid red curve in Figure 3-4 (c), is achieved under the condition of U_1 = 0.80 mm, T_1 = 0.80 mm, L_1 = 0.40 mm, and L_2 = 0.40 mm as shown in Figure 3-4 (b). The other performance with different fine-tuning configurations in Figure 3-4 (b) further shows that lower in-band return loss is generally got with

a decreased bandwidth. This implies a tradeoff between these two kinds of performance. But, an optimal scheme could be found, as indicated by the dotted black curve in Figure 3-4 (c), which reaches a good compromise between the bandwidth and in-band return loss. The realized gain for all the configurations in Figure 3-4 (c) is shown in Figure 3-5, in which an obvious improvement in the gain is found from 61 to 67 GHz, corresponding to the bandwidth improvement shown in Figure 3-4 (c).

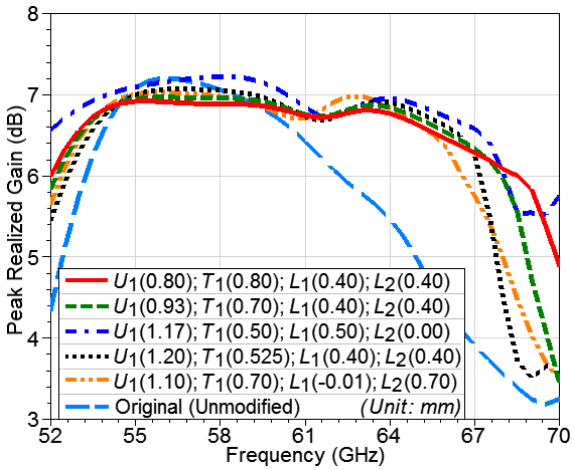


Figure 3-5 Simulated realized peak gain of the slot antenna with different fine-tuning offsets of the plated vias, corresponding to the ones in Figure 3-4 (b). For comparison, the antenna without fine-tuning of the plated vias is also shown.

3.3 Improved Bandwidth-Enhancement Configuration

3.3.1 SIGW Gap- and Via-Layers of The Same Substrate

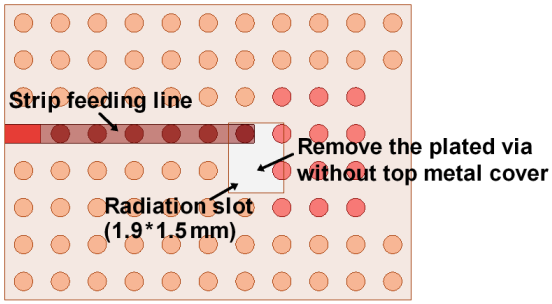
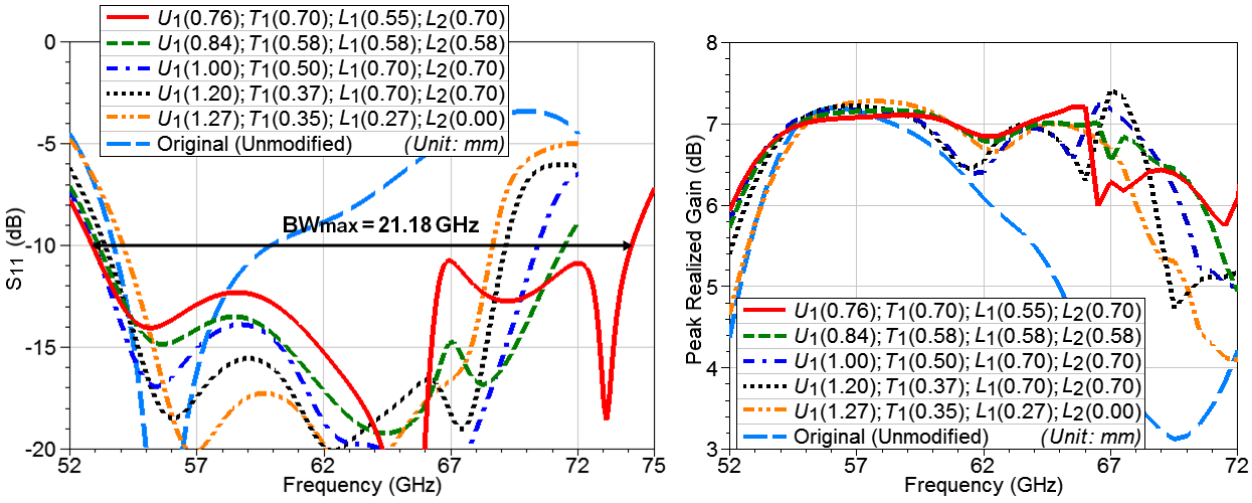


Figure 3-6 A single-slot SIGW antenna of the modified bandwidth-improvement fine-tuning configuration, i.e., removing the plated via just under the radiation slot (i.e., without upper metal cover).

In the last section, a unique method for improving the bandwidth of the slot antenna excited by SIGW was presented. However, it is seen from Figure 3-1 and Figure 3-4 that a plated via is just under the slot, i.e., without a metal cover over it. Thus, it is not a part of the GW or SIGW structure. This particular plated via is therefore removed from the above structure giving a modified bandwidth improvement configuration as shown in Figure 3-6. The simulated reflection coefficient, S_{11}, and gain performance with this modified configuration are presented in Figure 3-7 using the same dimensions and materials of Figure 3-1. As indicated by the solid red curve in Figure 3-7 (a), the maximum achieved bandwidth is 21.18 GHz for 10 dB return loss (35.3% at 60 GHz) that is around 5 GHz wider than the maximum one of 16.58 GHz got in the previous configuration shown in Figure 3-4. Removing the plated via without the top metal cover enlarges the cavity under the slot. Therefore, the cavity has more freedoms in adjusting to offer a wider-band impedance transition between the feed line and radiation impedances. The tradeoff found in Figure 3-4 (c) between the bandwidth and in-band return loss is also observed in Figure 3-7 (a) – lower reflection coefficients generally results in a decreased bandwidth. But, an optimal scheme for a good compromise between them is still existent, as presented by the dotted black curve in Figure 3-7 (a). The realized gains corresponding to the configurations in Figure 3-7 (a) is shown in Figure 3-7 (b), in which an improvement is found in all cases compared with the original one without tuning.

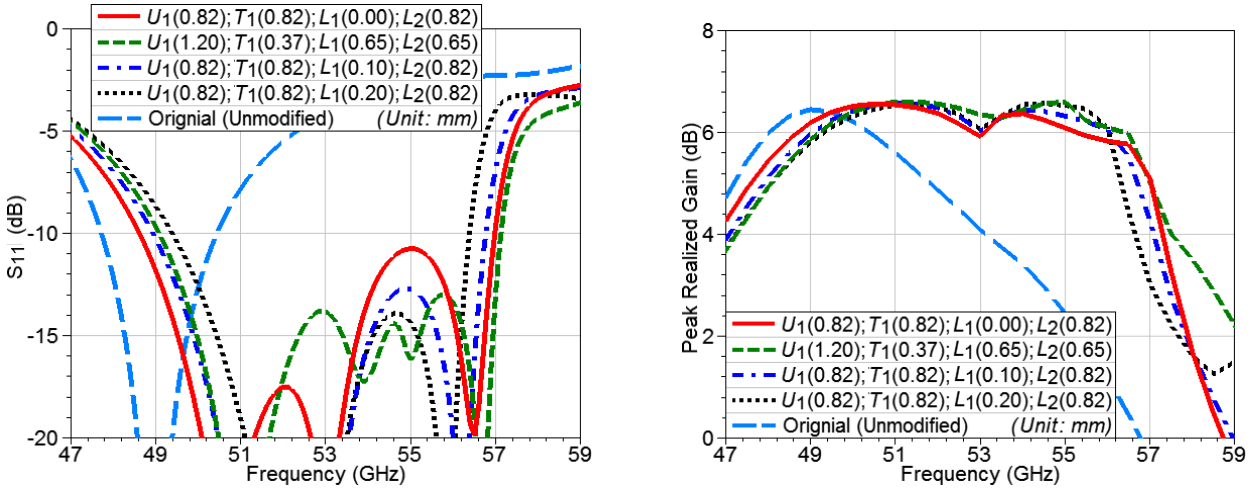


(a) (b)

Figure 3-7 Slot antenna of the modified bandwidth enhancement configuration. (a) Simulated reflection coefficient, S_{11}, with different fine-tuning offsets of the plated vias. (b) Simulated peak realized gain corresponding to the used offsets in Figure 3-7 (a). For comparison, the antenna without modification is also shown.

3.3.2 SIGW Gap- and Via-Layers of Different Substrates

The above study assumes that the gap-layer and via-layer of the SIGW are made on the same substrate, i.e., Rogers RT/Duroid 6002. However, the substrates of the gap- and via-layers can be different in a real implementation for the desired performance. For example, as indicated in [51] and [52], the SIGW operating frequency can be decreased by using a via-layer of higher ε_r. We do not have to care much about its loss tan δ because the dielectric losses are dominated by the gap-layer in which the signal propagates that should have lower tan δ. So, the proposed bandwidth-enhanced method is examined further in the case of using the gap- and via-layers with different substrates.



(a) (b)

Figure 3-8 A single-slot SIGW antenna of the modified bandwidth-improvement configuration. Gap-layer of ε_r = 2.94 and loss tan δ = 0.0012; via-layer of ε_r = 5.0 and loss tan δ = 0.0012. (a) Simulated return loss, S_{11}, with different fine-tuning offsets of the plated vias. (b) Simulated peak realized gain is corresponding to the used offsets in Figure 3-8 (a). For comparison, the antenna without modification is also shown.

The simulated performance presented in Figure 3-8 considers ε_r of the gap- and via-layers with 2.94 and 5.0, respectively (tan δ of those two layers is kept at 0.0012). The offsets of the slot relative to the center of the strip feed line end are adjusted to 0.85 and 0.05 mm in the x- and y-axis, respectively. The other dimensions are kept the same as in the previous design. It is clear from Figure 3-8 (a) that, even if the gap- and via-layers are of different ε_r, the presented method for improving the antenna bandwidth is still valid and very efficient. The improved realized gain due to the lowered inband return loss is presented in Figure 3-8 (b).

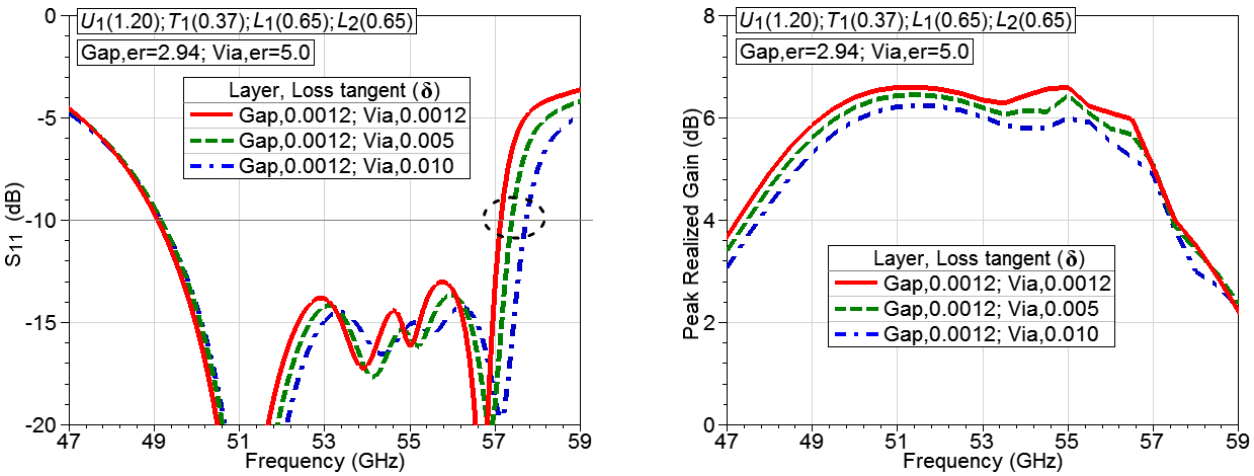


Figure 3-9 Slot antenna of the modified bandwidth enhancement configuration. Gap-layer of ε_r = 2.94 and tan δ = 0.0012; via-layer of ε_r = 5.0 and tan δ = 0.0012, 0.005, or 0.01. (a) Simulated reflection coefficient, S_{11}, with different fine-tuning offsets of the plated vias. (b) Simulated peak realized gain corresponding to the used offsets in Figure 3-9 (a).

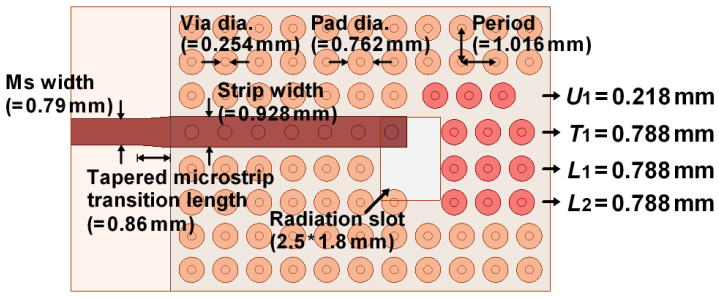
The other substrate parameter included in the study is tan δ. Since moving the plated vias away from the feed line end may cause more power leakage from the gap-layer to the via-layer, more dielectric losses will affect the antenna efficiency. This could be worse if the via-layer with a higher ε_r that will hold more power in and impose more effect on the propagating signal. The effect of the via-layer tan δ is presented in Figure 3-9 based on the configuration indicated by the dashed green curve in Figure 3-8 (a) for U_1 = 1.20 mm, T_1 = 0.37 mm, L_1 = 0.65 mm, and L_2 = 0.65 mm. Three different tan δ for the via-layer of 0.0012, 0.005, and 0.01 are considered. The gap-layer tan δ is kept at 0.0012. The gap- and via-layers ε_r are 2.94 and 5.0, respectively. The other structure dimensions are kept the same as in Figure 3-8. As observed in Figure 3-9 (b), even if the via-layer tan δ is increased to 0.01, which is around 10 times higher than its original value of 0.0012, the degradation in the gain is insignificant, as proven by the dotted-dashed blue curve. The corresponding bandwidth is given in Figure 3-9 (a), which shows that the increase in tan δ of the via-layer has a limited effect on the bandwidth, which just slightly lifts the upper end of the operation band.

Further to the above, the investigation of different tuning configurations of the plated vias offers a valuable guideline to improve the bandwidth. In general, the overall fine-tuning process can be started with two adjacent sets of vias (U_1-T_1, T_1-L_1, or L_1-L_2) or three adjacent sets of vias

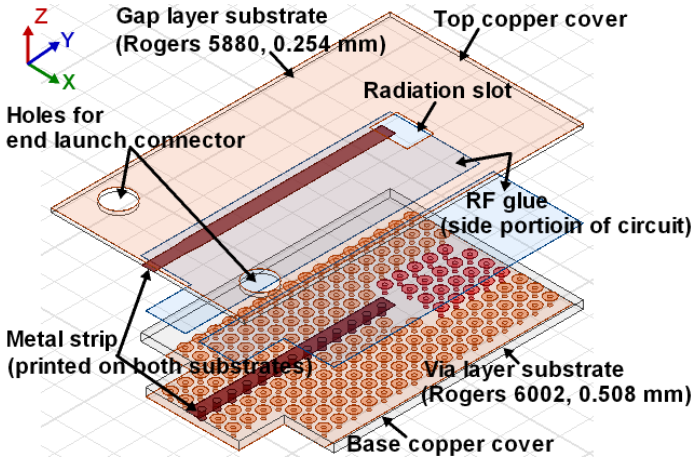
(U_1-T_1-L_1, or T_1-L_1-L_2). The next step is to fine-tune the one/two sets of vias that are not used in the last step. The objective in each fine-tuning step is achieving an optimal tradeoff between the bandwidth and in-band return loss (S_{11}). For example, the first step of the optimal configuration indicated by the dotted black curve in Figure 3-7 (a) is $L_1 = L_2 = 0.70$ mm. The second step is $U_1 = 1.20$ mm; and the final step is $T_1 = 0.37$ mm. In addition, if the slots separation of the antenna array is limited, the performance with tuning only two sets of the plated vias is acceptable. The simulation results show that the maximum bandwidth of the designed antenna shown in Figure 3-6 (without the plated via under the slot) can be up to 15.88 GHz (26.47%) with the configuration of $U_1 = 0.84$ mm, $T_1 = 0.84$ mm, $L_1 = 0.0$ mm, and $L_2 = 0.0$ mm, which is 9.8 GHz larger than the original one of 6.08 GHz shown in Figure 3-3. We should further take a note that, although the above demonstration is based on the SIGW, this presented bandwidth enhancement method is valid if used in the air-gap-based GW, such as the metal-ridge GW and the microstrip-ridge GW.

3.4 Experimental Verification and Analysis

The experimental verification of the presented bandwidth-enhancement method include two fabricated prototypes of a single-slot antenna and a 4-slot linear antenna array operating at 60 GHz. Since the fabrication is fully based on the low-cost PCB process, a metal pad has to be added to the plated via, as seen in Figure 3-10 (a). A spacing of 0.254 mm is required between the hole edge and the copper edge due to the metallization of the plated via, so the pad diameter is 0.762 mm for the plated vias of 0.254 mm diameter. The period of the plated vias is then 1.016 mm. The width of the SIGW strip-ridge is 0.928 mm for about 50 Ω characteristic impedance at 60 GHz. Thus, the diameter of the plated vias connecting the strip to the base metal cover is 0.42 mm due to the required 0.254 mm spacing. A tapered microstrip transition is built between the SIGW strip-ridge and the standard microstrip line for the measurement purpose. The width of the microstrip line is 0.79 mm for around 50 Ω characteristic impedance at 60 GHz. The width and length of the slot are 1.8 × 2.5 mm, respectively. The offsets of the slot relative to the center of the feed line end are 0.8 and 0.106 mm in the x- and y-direction, respectively.



(a)



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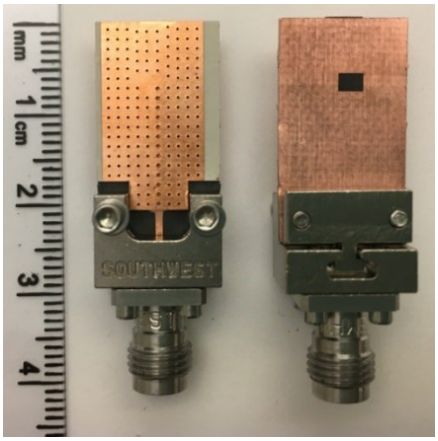


(c)

Figure 3-10 Slot antenna with transition to the standard microstrip line and the modified bandwidth enhancement configuration: U_1 = 0.218 mm, T_1 = 0.788 mm, L_1 = 0.788 mm, and L_2 = 0.788 mm. (a) Top view. (b) Distributed 3-D view of the fabrication. (c) Photo of the fabricated antenna with end launch connector for measurement (top view and back view).

3.4.1 Prototype of Single-Slot SIGW Antenna

The fabricated slot antenna in Figure 3-10 has an optimal tapered microstrip transition length of 0.86 mm for the low return loss over the operation band. The optimal fine-tuning configuration with U_1 = 0.218 mm, T_1 = 0.788 mm, L_1 = 0.788 mm, and L_2 = 0.788 mm is implemented. The distributed 3-D view of the fabrication is shown in Figure 3-10 (b). In the process, the plated vias in the base-layer substrate and the metal strips on both layers are first made, and then these two substrates are stacked together using a thin layer RF glue, with high temperature and pressure. The glue is located only on the side portions of the circuits to ensure the electrical contact between the metal strips – on the top of the lower layer and at the base of the upper layer. The available glue thickness is 5 um, much thinner than the copper foil thickness of 18 um, so a tight contact between the strips can be guaranteed. It is evident that since the propagating wave of the SIGW is concentrated in the gap-layer substrate, the effects of the high-attenuation ENIG coating only on the copper strip outer surface and the plated vias in the copper strip that usually perturbs the current are entirely avoided. The photo of the fabricated slot antenna is shown in Figure 3-10 (c) with an end launch connector for measurements. The measured S_{11} parameters of the slot antenna (including the transition to the microstrip line and the end launch connector) from a VNA are presented in Figure 3-11 (a), which shows a bandwidth of 14.4 GHz (24.1%) for the S_{11} lower than -10 dB (from 52.6 to 67 GHz) and have good agreement with the simulation. The measured and simulated realized gain are compared in Figure 3-11 (b) and they are presented in good agreement. The difference between the simulated directivity and realized gain is due to the mismatch loss and the losses in the feeding network. As the realized gain has taken the return loss into account, the increased S_{11} after 64 GHz can still cause the drop in the gain even if S_{11} is lower than -10 dB. The additional mismatch loss and insertion loss caused by the end launch connector used in measurements are the possible main reasons for the degraded measured S_{11} and realized gain. The connector was not considered in the simulations, in which a numerical wave port was used. The other possible factor for the degraded measured performance could be the used RF glue that was also not taken into account in simulations. The glue with ε_r of 3.5 (different from that of the used substrates) and tan δ of 0.03 (larger than that of the substrates) may also introduce additional mismatch loss and dielectric losses. Figure 3-11 (c) shows that the calculated radiation efficiency of the single-slot

SIGW antenna is around 93% over the achieved band. The mismatch loss has been taken into account in the total antenna efficiency, indicated by the dashed green curve.

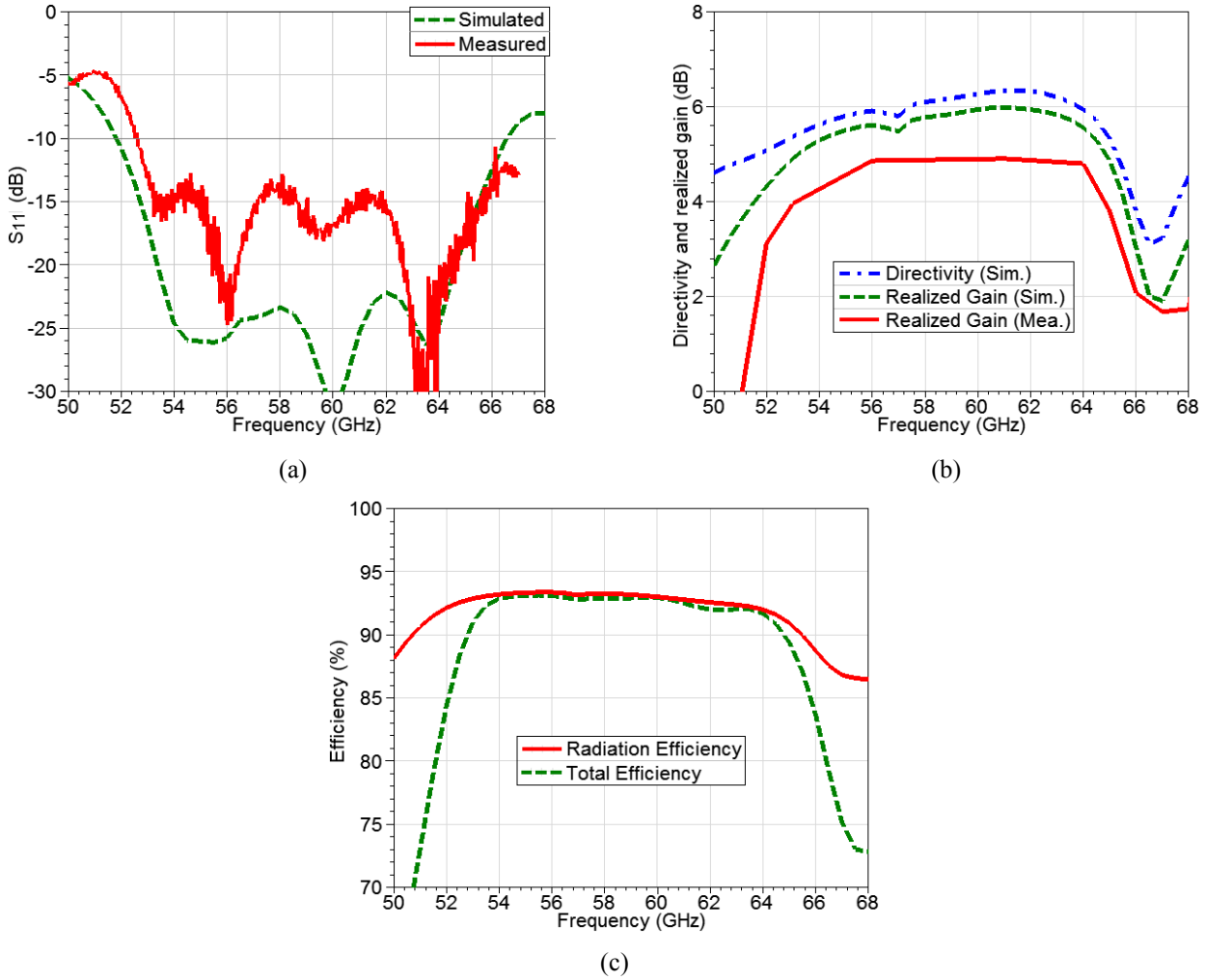


Figure 3-11 (a) Measured and simulated S_{11} of the single-slot SIGW antenna. (b) Measured and simulated realized gain of the single-slot SIGW antenna, with a comparison with simulated directivity. (c) Simulated radiation efficiency and total efficiency of the single-slot SIGW antenna.

Note that the selected fine-tuning configuration of the plated vias in fabrication is due to the frequency limit of 67 GHz of the coaxial connector. However, a broader bandwidth is available with other proper tuning schemes, as indicated in Figure 3-12. A bandwidth of 20.6 GHz (33%) can be obtained with S_{11} less than -10 dB (from 50.79 to 70.85 GHz) using the configuration of U_1 = 0.618 mm, T_1 = 0.288 mm, L_1 = 0.288 mm, and L_2 = 0.288 mm.

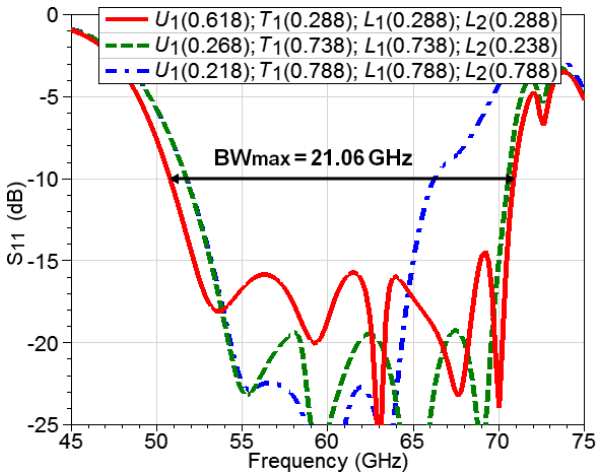
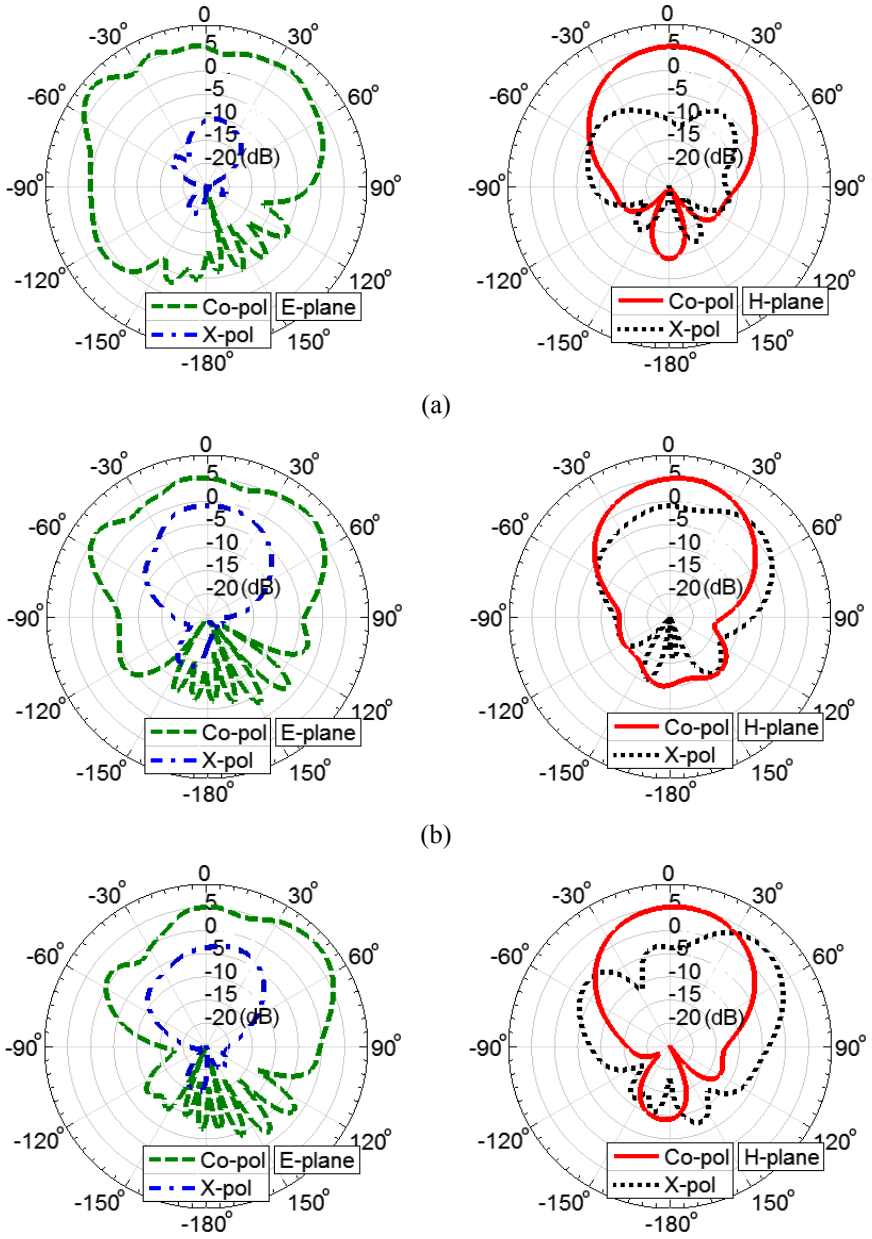


Figure 3-12 Simulated return loss, S_{11}, of the fabricated single-slot SIGW antenna with different fine-tuning schemes of the plated vias, excluding the microstrip line and transition.

The simulated co-polar and cross-polar radiation patterns of the single-slot SIGW antenna in E- and H-plane are given in Figure 3-13 at three frequencies of 54, 60, and 64 GHz. The E-plane beamwidth is wider than the H-plane beamwidth. The measured and simulated far-field radiation patterns of the antenna in the E- and H-planes at 54, 60, and 64 GHz are compared in Figure 3-14 showing good agreement. As the slot is excited by the feed line together with the cavity, the shifting of the slot in both x- and y-axis and the asymmetry of the cavity around the slot (due to the shifting of the selected plated vias), as observed in Figure 3-10 (a), cause the asymmetry presented in E- and H-planes. This effect will appear more evident at higher frequencies due to the decreased wavelength. Also, because the E-plane cut provides the contribution of the used connector, the simulated radiation patterns without the connector will have some differences from the measured ones. The observed differences in all the above measured and simulated performance (S_{11}, realized gain and radiation patterns) could also be possible due to fabrication tolerances, measurement uncertainties, copper surface roughness, and substrate frequency-dependent ε_r and tan δ.

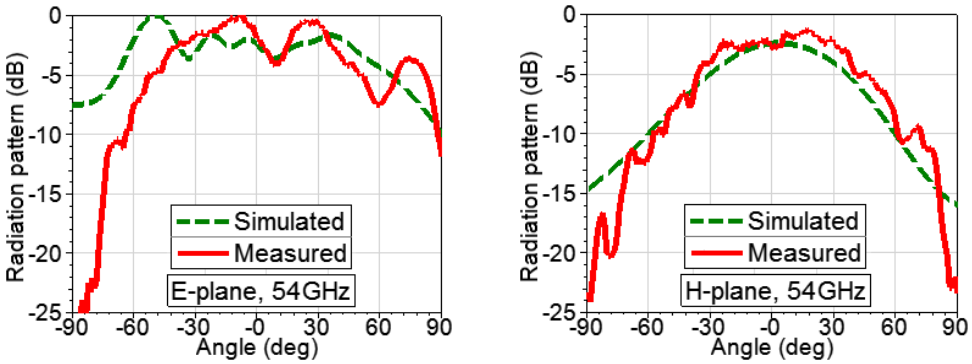


(a)

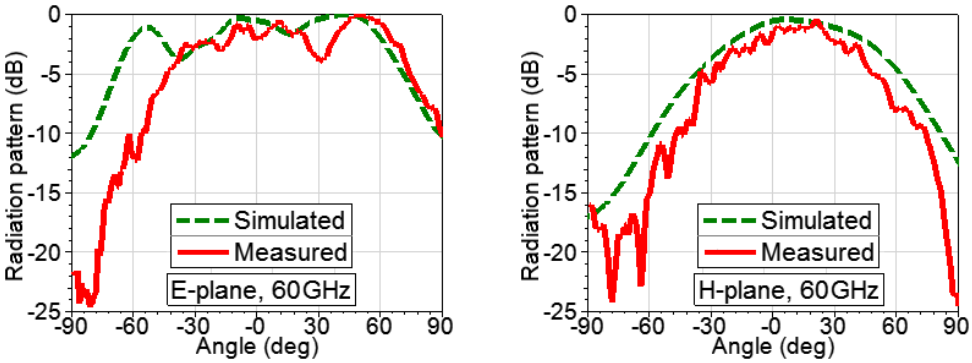
(b)

(c)

Figure 3-13 Simulated co-polar and cross-polar radiation patterns of the single-slot SIGW antenna in E- and H-planes. (a) 54 GHz. (b) 60 GHz. (c) 64 GHz.



(a)



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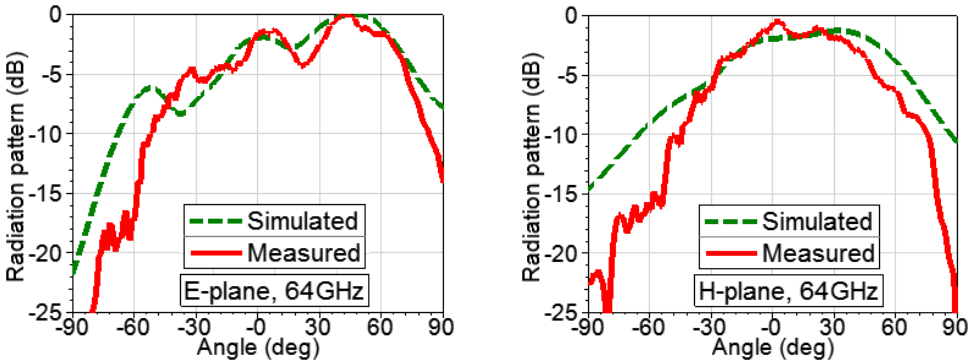
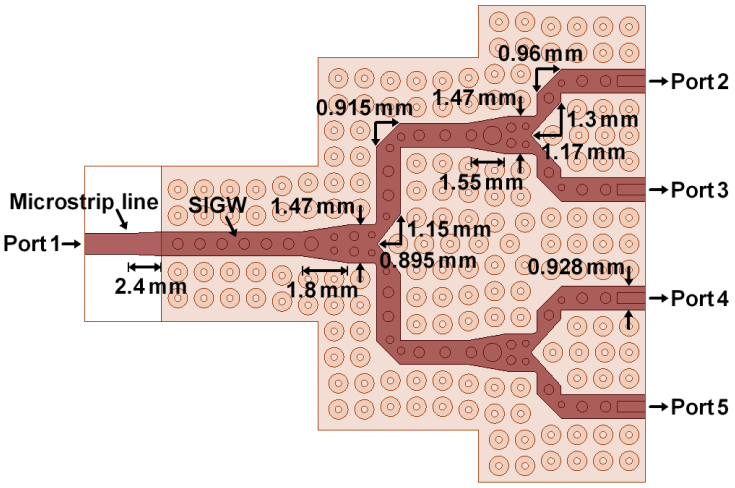


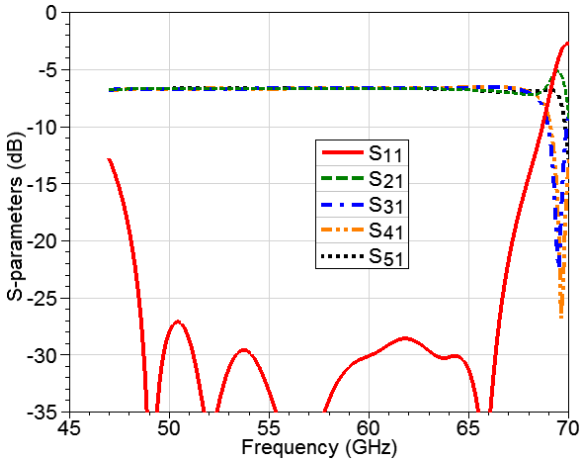
(c)

Figure 3-14 Measured and simulated normalized far-field radiation patterns of the single-slot SIGW antenna in E- and H-planes. (a) 54 GHz. (b) 60 GHz. (c) 64 GHz.

3.4.2 Prototype of 4-Slot SIGW Linear Antenna Array



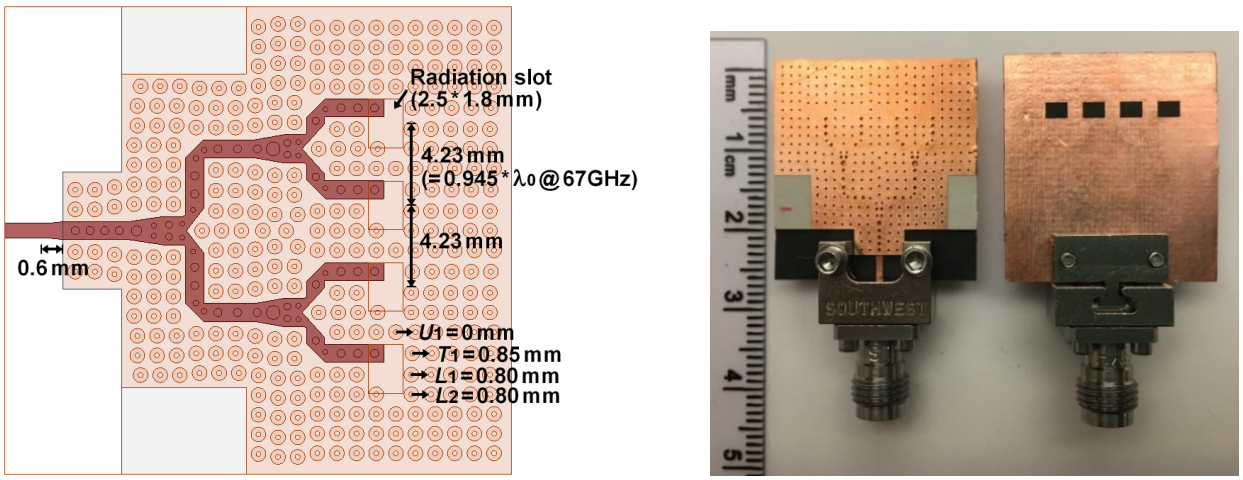
(a)



(b)

Figure 3-15 Power distribution network for the 4-slot SIGW linear antenna array, with the transition to the standard microstrip line. (a) Top view. (b) Simulated S-parameters.

To further investigate the proposed bandwidth enhancement method in the antenna array, a prototype of 4-slot SIGW linear antenna array is built. The power distribution network shown in Figure 3-15 (a) is based on T-shaped power dividers and quarter wavelength impedance transformers. The simulated performance is shown in Figure 3-15 (b) indicating a uniform power distribution. The insertion loss is 0.7 dB (including the losses of the microstrip line) and the input return loss, S_{11}, is lower than -20 dB from 48 to 67 GHz.



(a) (b)

Figure 3-16 A 4-slot SIGW linear antenna array with transition to the standard microstrip line and the modified bandwidth enhancement configuration: U_1 = 0 mm, T_1 = 0.85 mm, L_1 = 0.80 mm, and L_2 = 0.80 mm. (a) Top view. (c) Photo of the fabricated antenna with end launch connector for measurement (top view and back view).

The 4-slot linear array is excited with equal amplitude and phase by the feeding network. The element spacing is chosen to be 4.23 mm, which is about 0.945 wavelengths at 67 GHz – smaller than a wavelength – to avoid the grating lobe issue. The used fine-tuning configuration of the plated vias is: U_1 = 0 mm, T_1 = 0.85 mm, L_1 = 0.80 mm, and L_2 = 0.80 mm. The offset U_1 of 0 mm (i.e., only three sets of the plated vias are utilized) is to ensure keeping at least one pin row between these neighboring cavities under the slots to avoid their mutual coupling. The fabricated 4-slot SIGW linear antenna array with the modified fine-tuning of the plated vias and the transition to the microstrip line is shown in Figure 3-16. The length of the tapered microstrip line is changed to 0.60 mm. The measured S_{11} of the antenna array including the microstrip line and the end launch connector is given in Figure 3-17 (a). It is found that a measured bandwidth of 12.07 GHz (20.34%) is achieved for S_{11} lower than -10 dB (from 53.31 to 65.38 GHz) and the measured and simulated S_{11} are in good agreement. The measured realized gain is compared with the simulated one in Figure 3-17 (b), and they are in good agreement with the frequency band. The difference between the simulated directivity and realized gain is mainly due to the mismatch loss and the losses in the feeding network. Compared with the simulated, the degradation in the measured in-band S_{11} and the realized gain observed in Figures 3-17 (a) and (b) is still possible due to the connector and RF glue that was not considered in simulations, as explained previously in Figure 3-11 for the single-slot SIGW antenna. Figure 3-17 (c) presents the calculated radiation

efficiency of the 4-slot SIGW linear antenna array, which is around 90% over the achieved bandwidth. The total antenna efficiency, presented by the dashed green curve, has considered the mismatch loss.

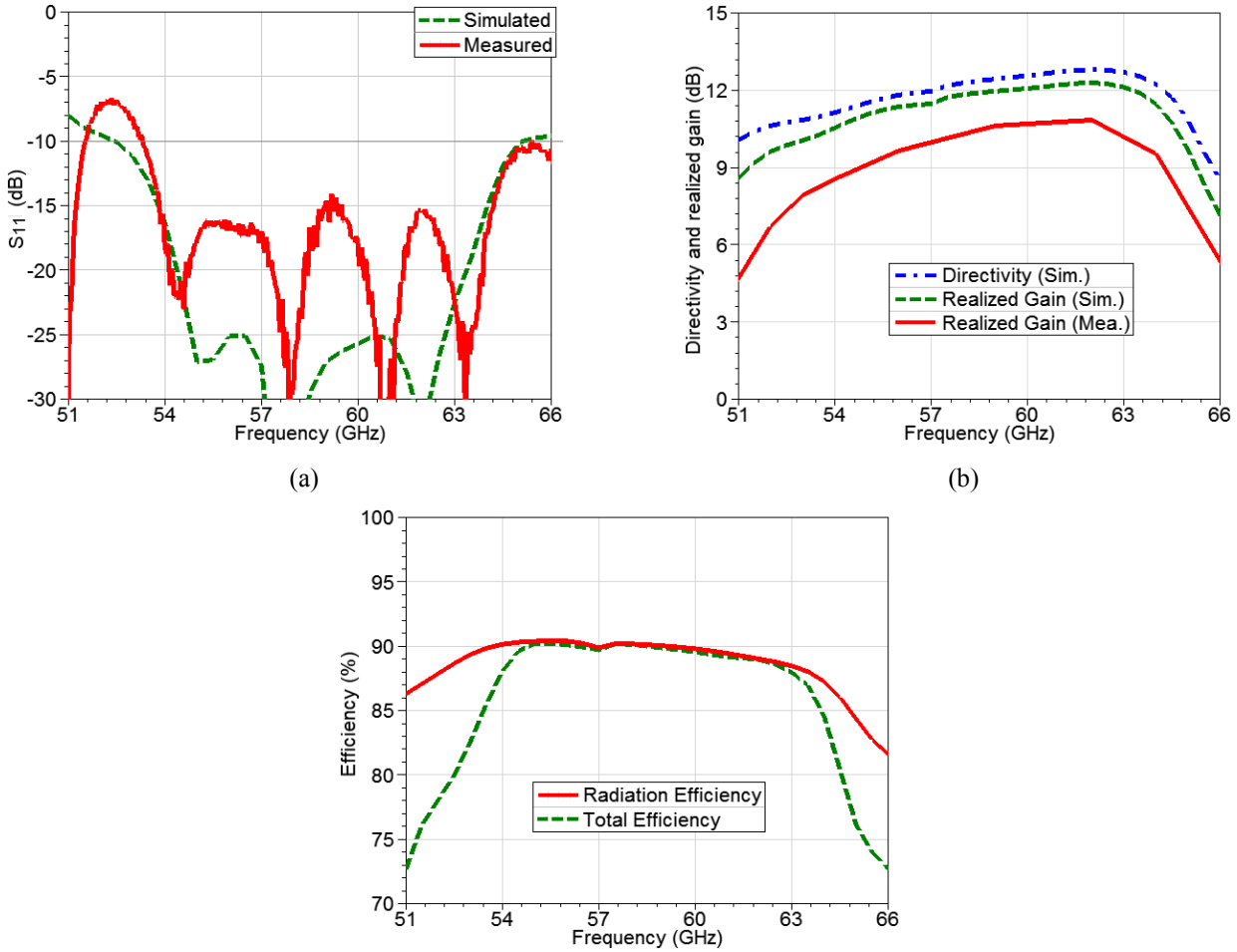
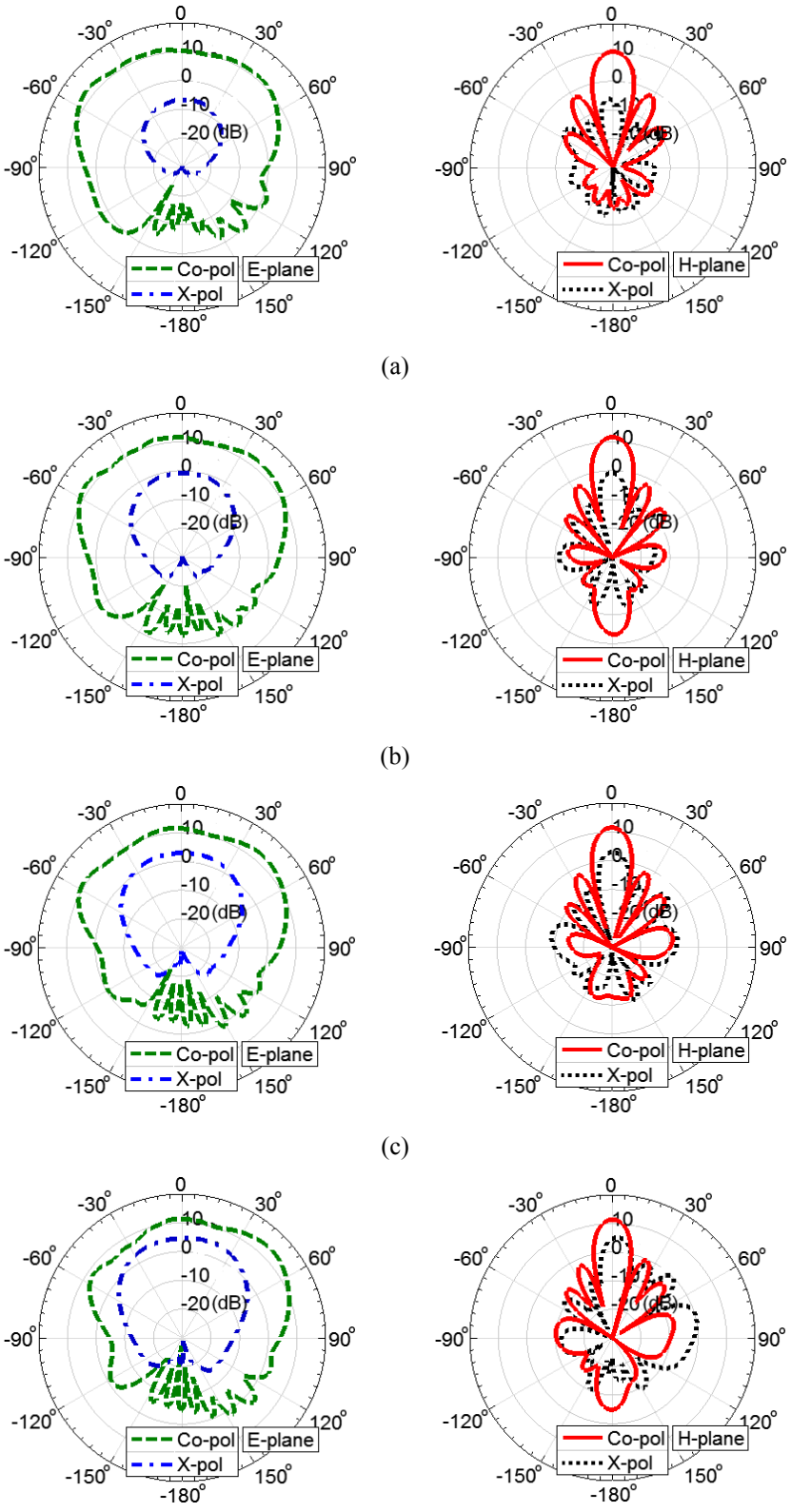


Figure 3-17 (a) Measured and simulated S_{11} of the 4-slot SIGW linear antenna array. (b) Measured and simulated realized gain of the 4-slot SIGW linear antenna array, with a comparison with simulated directivity. (c) Simulated radiation efficiency and total efficiency of the 4-slot SIGW linear antenna array.



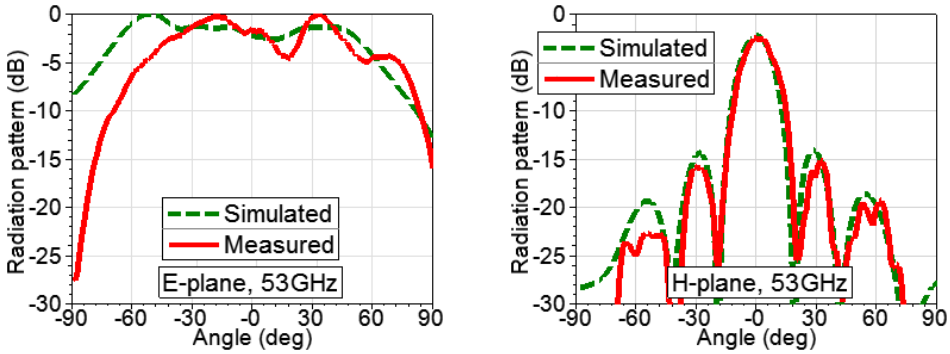
(a)

(b)

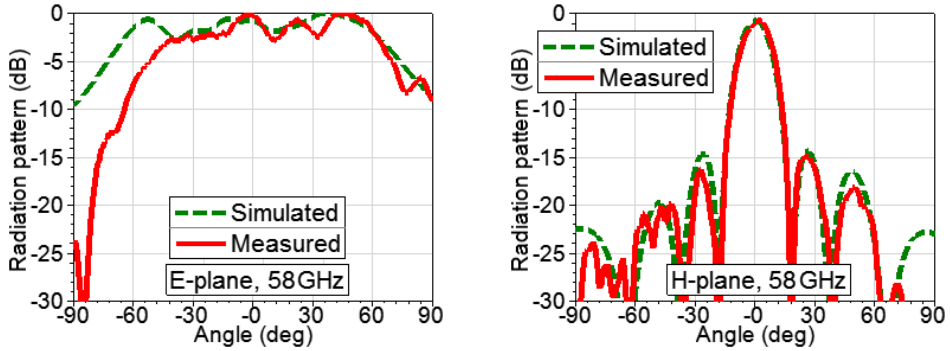
(c)

(d)

Figure 3-18 Simulated co-polar and cross-polar radiation patterns of the 4-slot SIGW linear antenna array in E- and H-planes. (a) 53 GHz. (b) 58 GHz. (c) 60 GHz. (d) 63 GHz.



(a)



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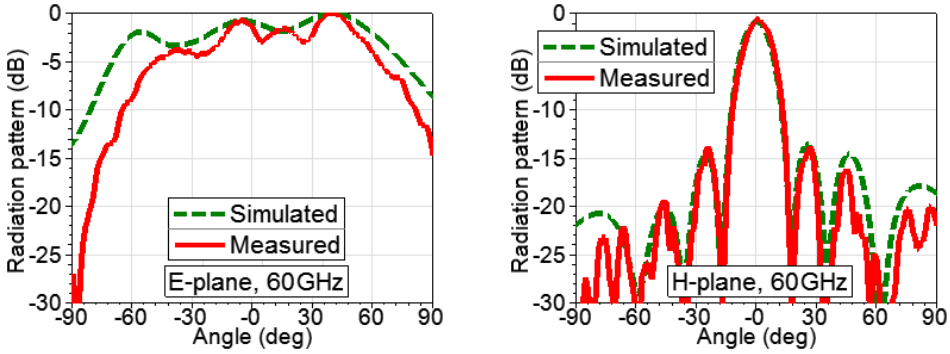
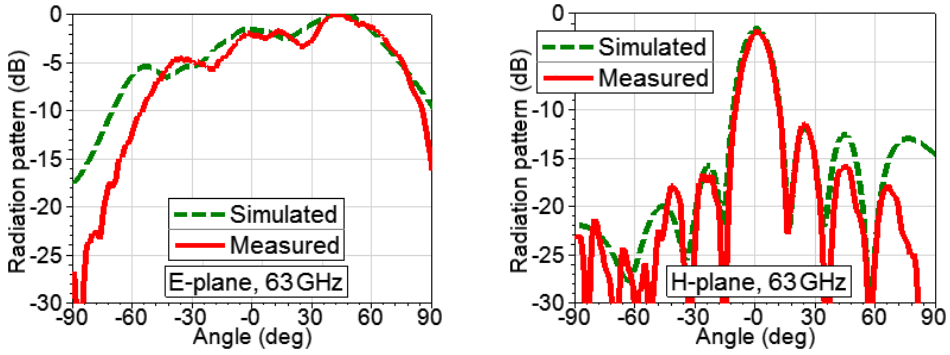


(c)



(d)

Figure 3-19 Measured and simulated normalized far-field radiation patterns of the 4-slot SIGW linear antenna array in E- and H-planes. (a) 53 GHz. (b) 58 GHz. (c) 60 GHz. (d) 63 GHz.

The simulated co-polar and cross-polar radiation patterns of the 4-slot SIGW linear antenna array in E- and H-plane are given in Figure 3-18 at four frequencies of 53, 58, 60, and 63 GHz. The E-plane beamwidth is wider than the H-plane beamwidth. The measured and simulated far-field radiation patterns of the antenna array in the E- and H-plane at 53, 58, 60, and 63 GHz are compared in Figure 3-19 showing good agreement. The measured first sidelobe level at 53, 58 and 60 GHz is below -12 dB in H-plane, but increases to -10 dB at 63 GHz as the element spacing is closer to a wavelength at the higher frequency. As explained previously in Figure 3-14 for the single-slot SIGW antenna, the asymmetry observed in E- and H-plane for the 4-slot linear antenna array is still attributed to the shifting of the slot, the asymmetry of the cavity around the slot, as well as the used connector. Of course, the differences seen in Figure 3-17 and Figure 3-19 between the measured and simulated results are also possible due to fabrication tolerances, measurement uncertainties, copper surface roughness, and substrate frequency-dependent ε_r and tan δ.

3.5 Conclusion

A unique and more powerful method has been presented and studied in this chapter to enhance the bandwidth performance of the SIGW slot antenna. By shifting the plated vias next to the end of the strip feeding line, the cavity under the slot is activated and tuned. This makes the cavity with the slot become the radiation mechanism of the antenna. Therefore, besides the slot resonance itself, there is a second resonance introduced by the cavity. The resonances from the slot and the cavity appear to be close to each other that benefits the bandwidth. A modified configuration of this method has been presented further, which has been proven to be even better, by removing the plated via without the top metal cover. The demonstration has considered the gap- and via-layers of the SIGW with the same or different ε_r and tan δ and shown that a bandwidth over 21 GHz (35%) centering at 60 GHz is achieved. Two fabricated 60 GHz SIGW antennas (a single-slot antenna and a 4-slot linear antenna array) with this bandwidth enhancement method have offered the required experimental verification. Quite good agreement between the measured and simulated results have been achieved even with the presence of the connector in the measurement, fabrication tolerances, measurement uncertainties, and substrate frequency-dependent ε_r and tan δ. Moreover, this work is also the first component designed in

the novel SIGW, which deals with the bulky original metal GW and the deficiencies inherent in the microstrip-ridge GW and inverted microstrip GW.

Chapter 4 Packaged Microstrip Line

4.1 Introduction

The SIGW has been introduced and implemented on antenna arrays at mm-wave bands in Chapter 3 and Chapter 4. However, the precise alignment required in the SIGW between the two printed metal strips may still be challenged in the fabrication. In this chapter, a new GW variant is developed from the SIGW and named as a packaged microstrip line. Different from the SIGW with two strips and two layers, this packaged microstrip line is comprised of only one metal strip and three-layer substrates. A bottom layer is to place the metal strip. A top layer builds the PMC shielding with the periodic plated vias. And a middle layer separates the PMC layer from the metal strip and base ground plane. The propagating wave, a quasi-TEM mode, is guided by the metal strip and concentrated in the base-layer substrate [2], [8], [53]-[56]. No other undesired modes exist within the band of interest, with the top-layer PMC shielding as a proper gap height is implemented. Note that, the ground plane works as an ideal PEC creating a PEC-PMC structure, and thus the gap between the PEC and PMC contains both the base and middle layers. Due to the absence of radiation and surface waves, the conduction losses due to the high current density can be significantly reduced with a thicker base-layer substrate, without interference or crosstalk between the adjacent components [57]-[59]. Besides, it is seen that no plated vias are required in the printed strip. This makes the strip width more flexible in the design with the packaged microstrip line than the SIGW since the minimum via diameter in the PCB technology cannot exceed the half of the substrate thickness. And there is an additional required spacing of 0.254 mm between the via edge and copper edge, which further limits the available minimum strip width in the SIGW. Therefore, the packaged microstrip line is promising at microwave and mm-wave bands in circuits' performance and fabrication [60]-[63].

Indeed, the suppression of the surface waves in the substrate can also be realized by the electromagnetic bandgap (EBG) or defect ground structure (DGS) with their high-impedance surface [64]-[66]. However, an additional metal shielding that surrounds a microstrip-EBG/DGS circuit is still required to stop the space radiation. Otherwise, significant radiation will increase the insertion loss and additionally cause the unwanted RF interference among the adjacent circuit elements. Moreover, the implementation of such packaging is very complicated, since a recessed

region is required in the metal bearing carrier under the defected ground slots, and the resonance frequency of the DGS depends on the dimensions of this region [67], [68]. So, it is seen that the packaged microstrip line merges both the virtues of suppressing the space radiation and surface waves in the substrate, which makes it very attractive for the cost-effective circuit design in both performance improvement and size reduction.

The stopband, dielectric/conductor losses, and characteristic impedance of the packaged microstrip line are carefully investigated in this chapter. Both the cases are considered for the plated vias are directly over the metal strip or not because more power could be coupled to the vias causing more conductor/dielectric losses in the PMC layer if the plated vias are directly over the strip. The study will offer a guideline on how to adopt a proper substrate for each layer of the packaged microstrip line, considering both the desired stopband and in-band performance, as well as on how to design the line width for a given impedance at an operating frequency. The study also includes the transition from the packaged microstrip line to the standard microstrip line. It will prove that such transition part external to the packaged microstrip line is unnecessary. The performance of the packaged microstrip line is further going to be compared with the standard microstrip line (with or without a conventional metal shielding box). Two fabricated prototypes with different substrates for the PMC layer provide the required experimental verification. In addition, the first antenna realized with this new packaged microstrip line is presented.

4.2 Study of Stopband Characteristics

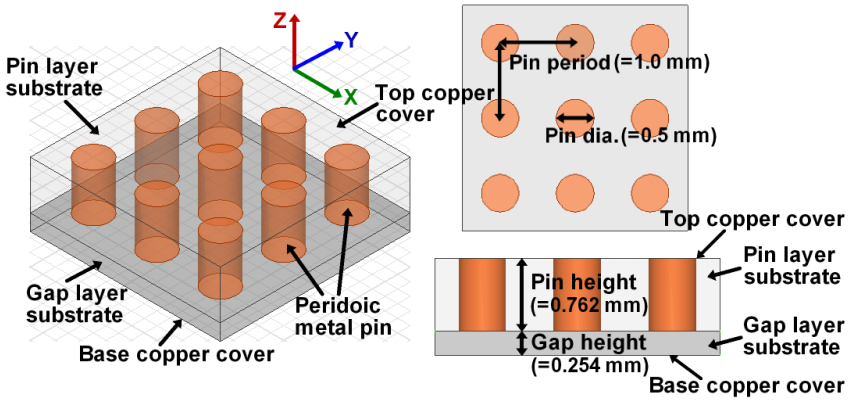


Figure 4-1 GW composed of nine cells of periodic metal pins and containing two substrates for the pin- and gap-layers: overview, side view, and top view. The top of the upper substrate and the bottom of the lower substrate are fully covered with copper.

The structure used to study the stopband characteristics of the packaged microstrip line is shown in Figure 4-1 containing nine unit cells. The effects of the pin- and gap-layer substrates ε_r on the stopband characteristics are going to be investigated in this section, together with the geometric parameters. This will help find out which layer substrate is dominant in the stopband characteristics, and give us a guideline to achieve the desired operation band.

4.2.1 Pin- and Gap-Layers of Different Substrates

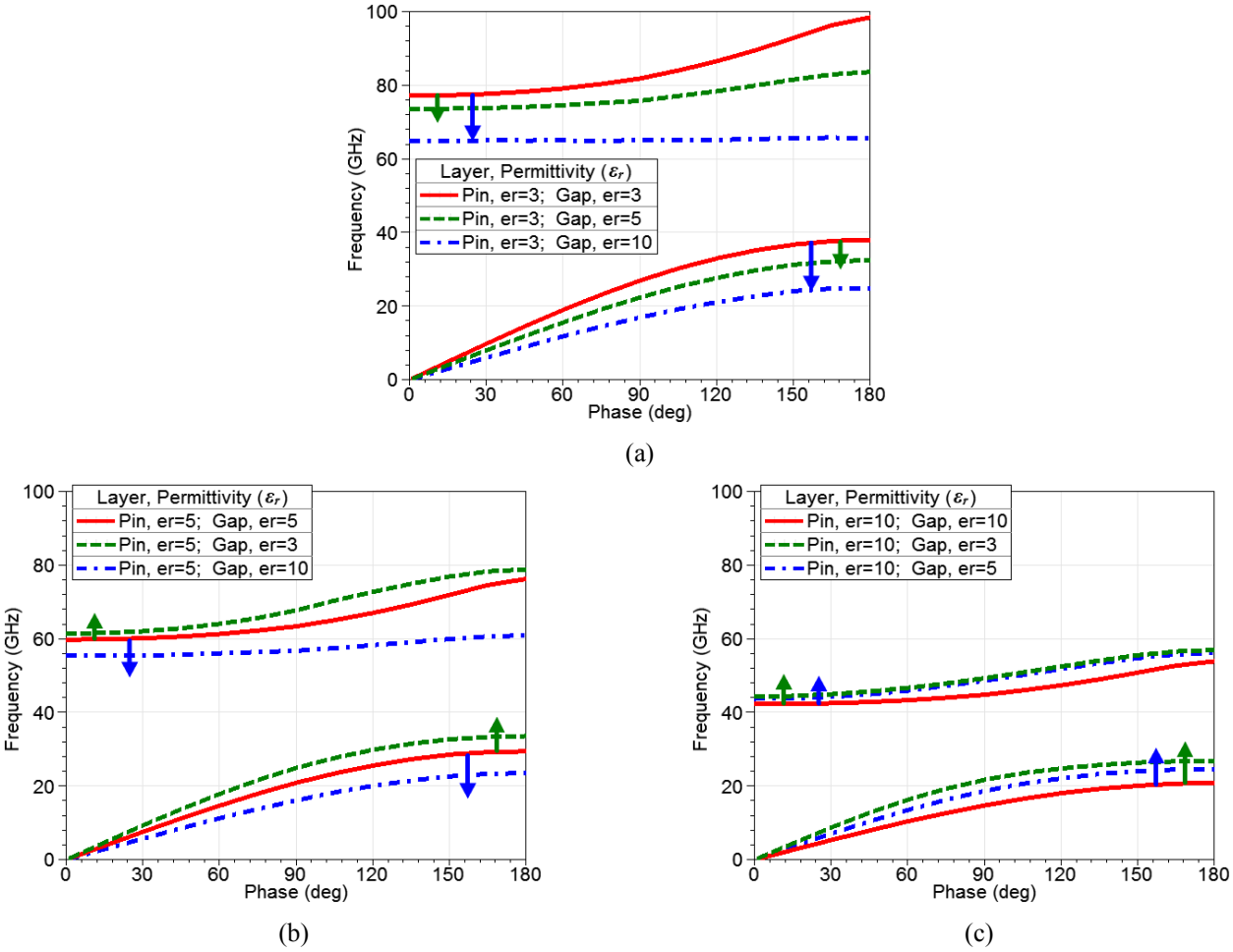


Figure 4-2 Dispersion diagram for a unit cell shown in Figure 4-1, with pins of 0.5 mm diameter, 1.0 mm period, 0.762 mm height, and 0.254 mm gap to the cell base, but with two different substrates for the pin- and gap-layers. (a) Pin-layer ε_r = 3 and gap-layer ε_r = 5 or 10. (b) Pin-layer ε_r = 5 and gap-layer ε_r = 3 or 10. (c) Pin-layer ε_r = 10 and gap-layer ε_r = 3 or 5. For comparison, the dispersion diagrams of the cell using the same substrate for both the pin- and gap-layers are also shown for ε_r = 3, 5, and 10.

The contributions of both the pin- and gap-layer substrates to the stopband characteristics can be clearly observed from Figure 4-2, which are three dispersion diagrams of the unit cell in

Figure 4-1, computed from the HFSS Eigenmode solver. The periodic metal pin has a diameter of 0.5 mm, a period of 1.0 mm, a height of 0.762 mm, and a gap of 0.254 mm to the cell base. In each diagram, the pin-layer ε_r is fixed, while the gap-layer ε_r is changed. For comparison, the dispersion curves for the unit cell using the same substrate for both the pin- and gap-layers are also added in Figure 4-2. From Figure 4-2 (a), it is seen that if the pin-layer ε_r is fixed at 3, but the gap-layer ε_r = 3 (solid red curve) is increased to ε_r = 5 (dashed green curve), both the lower and upper cutoff frequencies drop down, compared with the case of the same substrate of ε_r = 3 used in both the two layers. Such behavior is enhanced further when the gap-layer ε_r is increased further to 10 (dotted-dashed blue curve). This phenomenon is very different from that happening to the varied gap height, which makes the lower and upper cutoff frequencies of the stopband move in the opposite direction in the frequency [69], [70]. So, the only possible explanation for the shown effect of the gap-layer substrate is that its increased ε_r enlarges the effective electrical length of the pin and this causes the drop in both the lower and upper cutoff frequencies.

As the above, similar variations can be seen in Figure 4-2 (b) and Figure 4-2 (c), in which the pin-layer ε_r is fixed at 5 and 10, respectively. When the gap-layer ε_r is higher than the pin-layer ε_r, the lower and the upper cutoff frequencies drop to lower values, while both the cutoff frequencies are uplifted when the gap-layer holds a lower ε_r. Relative to the results in Figure 4-2 (a), it is found that the variation ranges due to the gap-layer ε_r are apparently limited, particularly when the pin-layer ε_r is 10, as seen in Figure 4-2 (c). It is evident that the possible effect that the gap-layer substrate imposes on the effective electrical length of the metal pin is reduced for the pin-layer with a larger ε_r. In fact, Figure 4-2 has indicated that, rather than the gap-layer, the stopband characteristics are determined mostly by the pin-layer substrate, in particular for the latter of a higher ε_r. It is also seen that more sensitivities are presented in the lower cutoff frequencies to the gap-layer ε_r, compared with the upper counterparts.

4.2.2 Substrate Permittivity Versus Gap Height

The gap height between the PMC and PEC is the decisive factor in the GW stopband, so, in particular, this geometrical parameter is studied together with the pin- and gap-layers substrate ε_r. As shown by the solid red curve in Figure 4-3 (a) for using the same substrate of ε_r = 3 for the pin- and gap-layers, the enlarged gap height drops the upper cutoff frequency, while the caused increase in the lower cutoff frequency happens only at a small gap. Because of the increased

effective electrical length of the metal pin due to the increased gap-layer ε_r, the lower and upper cutoffs of the stopband are both decreased. However, it is noted that the effect of the gap-layer ε_r is insignificant for a small gap height. Similar variations due to the gap-layer height and ε_r can also be found in Figures 4-3 (b) and (c), when the pin-layer ε_r is fixed at 5 and 10, respectively. And corresponding to Figure 4-2, the effect of the gap-layer ε_r to the cutoff frequencies is clearly limited if the pin-layer with a high ε_r. So, in general, a smaller gap height and a higher pin-layer ε_r are preferred to limit the gap-layer ε_r effect. Or, in other words, the gap-layer ε_r can be utilized to fine-tune the stopband to get the desired performance if the dimensions are given.

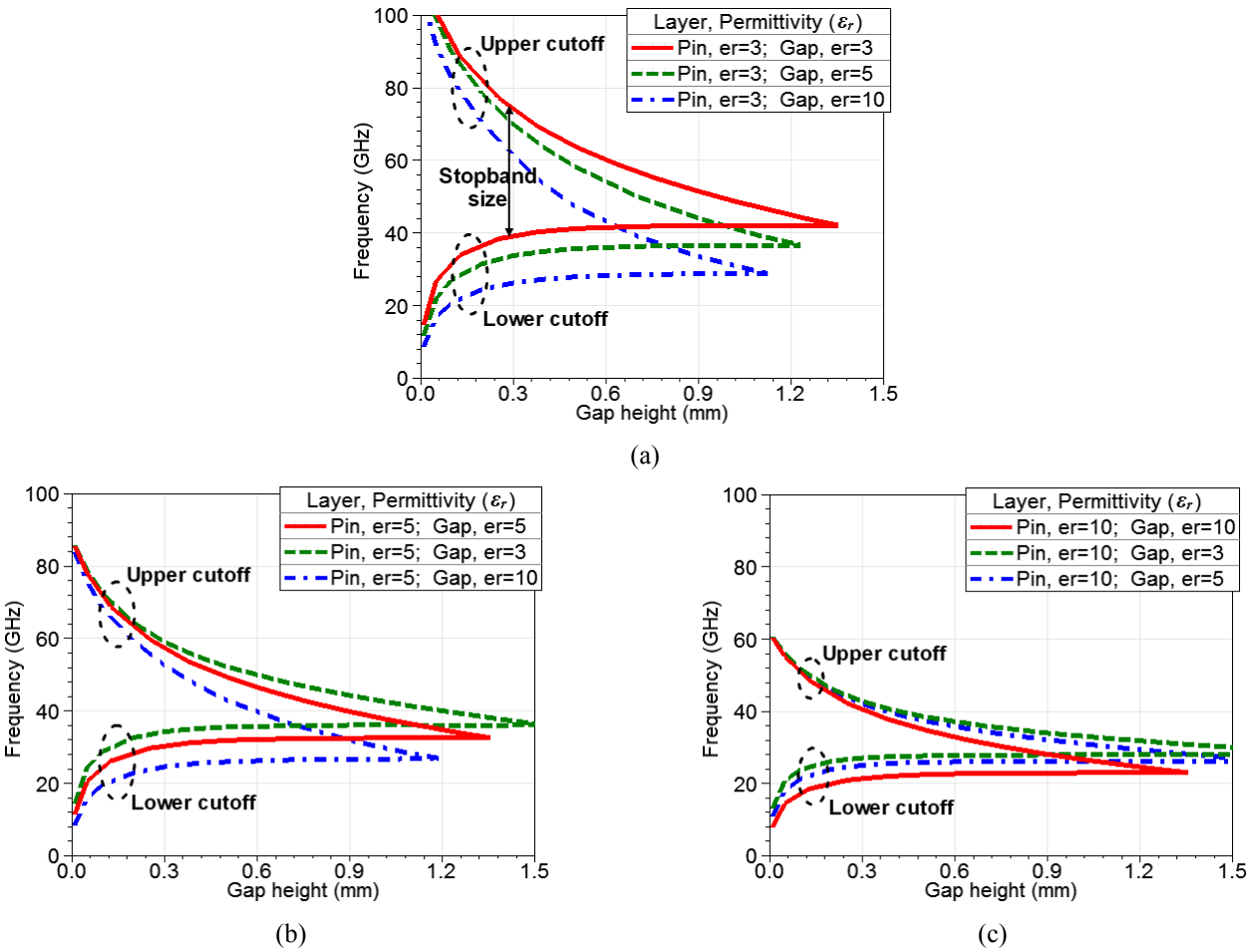


Figure 4-3 Change in lower and upper cutoff frequencies with gap height for one unit cell shown in Figure 4-1, using two different substrates for the pin- and gap-layers. (a) Pin-layer ε_r = 3 and gap-layer ε_r = 5 or 10. (b) Pin-layer ε_r = 5 and gap-layer ε_r = 3 or 10. (c) Pin-layer ε_r = 10 and gap-layer ε_r = 3 or 5.

The other finding from Figure 4-3 is that the changed gap-layer ε_r makes the stopband end at different gap heights. In particular, it occurs at a smaller gap height as the gap-layer ε_r is

higher than the pin-layer ε_r. This is clearer as observed in Figure 4-4, which is the stopband size calculated from the difference between the lower and the upper cutoff frequencies in Figure 4-3. However, it is seen that the bandwidth with the gap height is almost entirely decided by the pin-layer ε_r, although the lower and the upper cutoffs of the stopband may change due to the varied gap-layer ε_r. The explanation is that the increment or decrement of the lower and the upper cutoff frequencies due to the changed effective electrical length of the metal pin, from the varied gap-layer ε_r, is almost the same. Note that, for the pin- and gap-layers with the same ε_r, the stopband comes to an end at the same gap height of 1.35 mm, as shown by the solid red curves in Figure 4-3 and Figure 4-4.

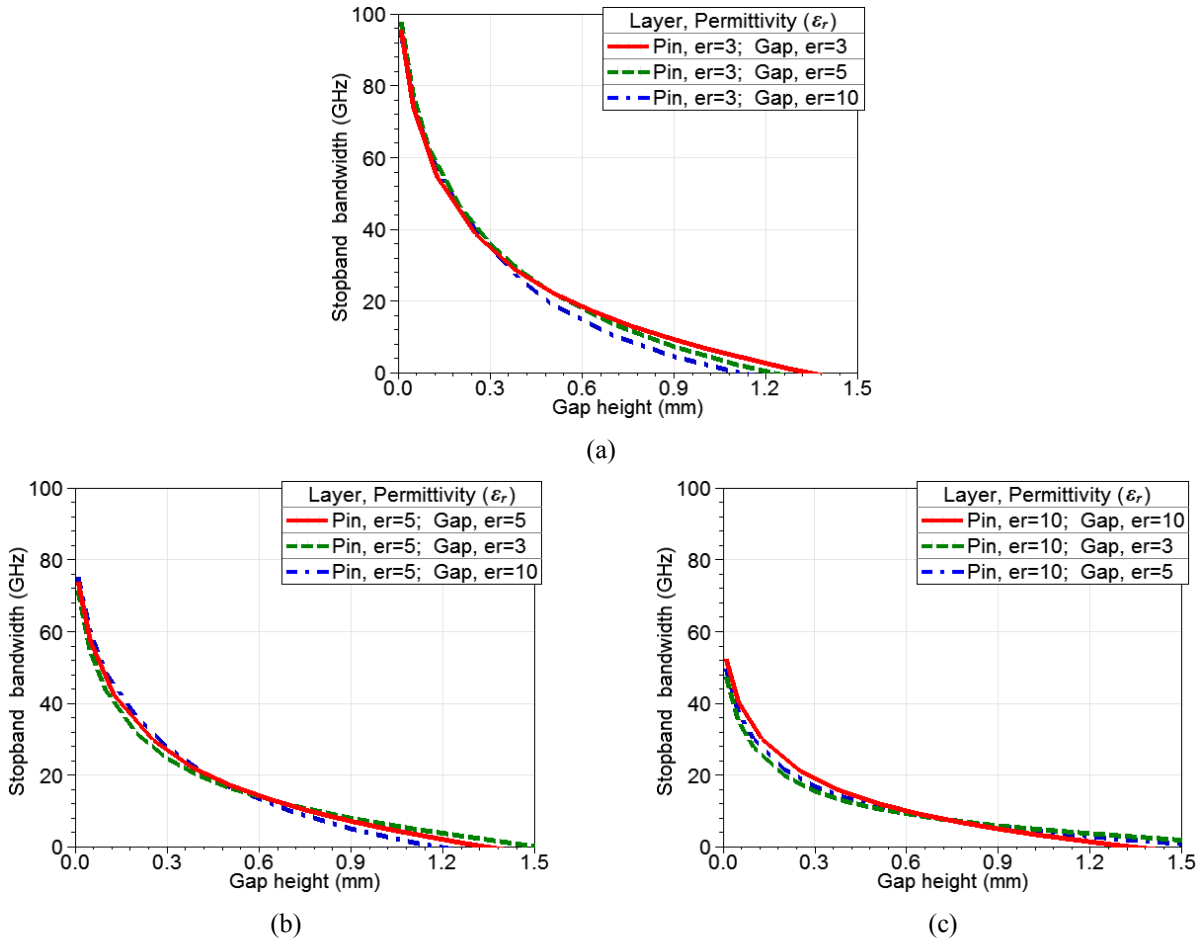


Figure 4-4 Change in stopband size with gap height for one unit cell shown in Figure 4-1, using two different substrates for the pin- and gap-layers. (a) Pin-layer ε_r = 3 and gap-layer ε_r = 5 or 10. (b) Pin-layer ε_r = 5 and gap-layer ε_r = 3 or 10. (c) Pin-layer ε_r = 10 and gap-layer ε_r = 3 or 5.

4.2.3 Substrate Permittivity Versus Other Dimensions

To build a complete analysis and to offer a guideline for the design of the packaged microstrip line, the effects of the layer substrate ε_r on the stopband characteristics are studied together with the other three geometric parameters: cell period, pin diameter, and pin height, which are presented in Figure 4-5, Figure 4-6, and Figure 4-7, respectively.

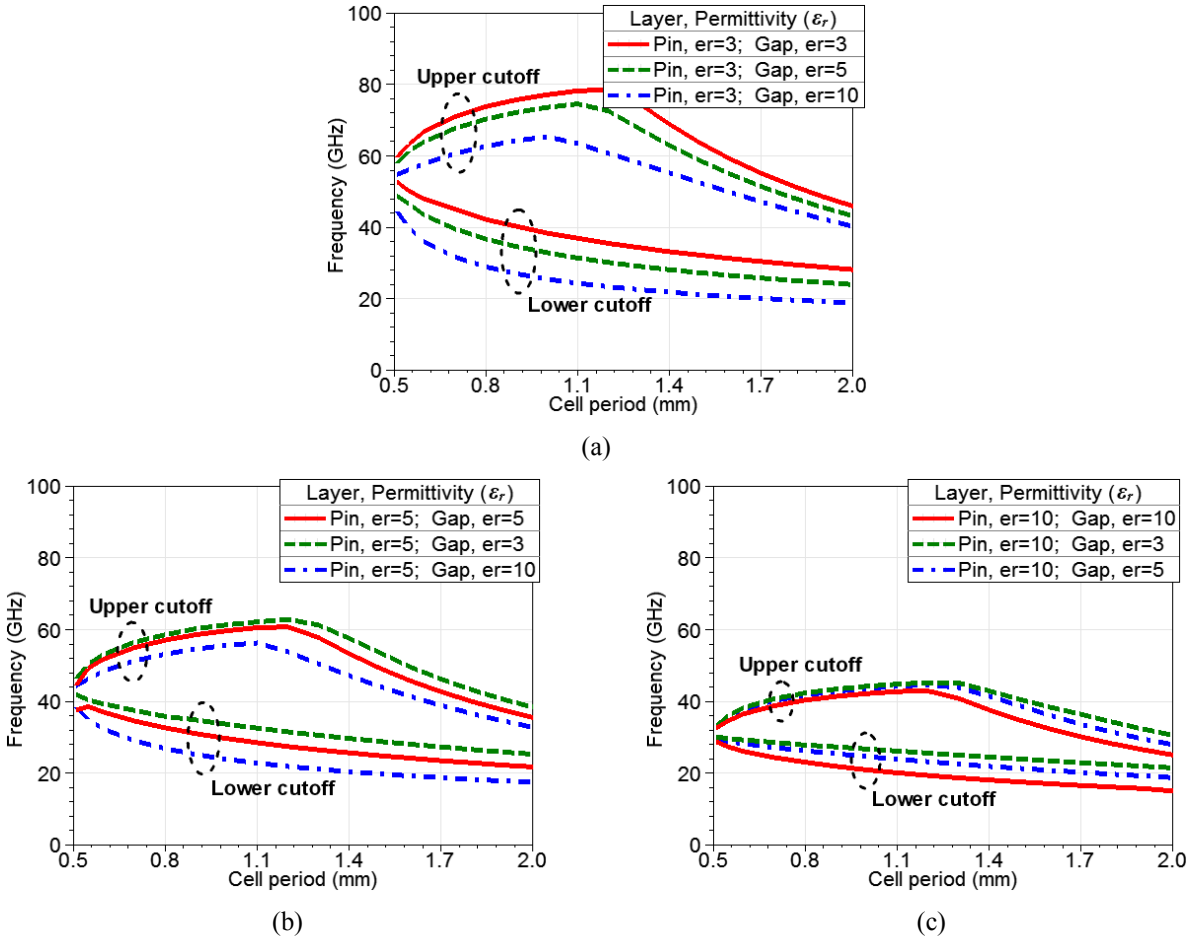


Figure 4-5 Change in the lower and upper cutoff frequencies with cell period for one unit cell shown in Figure 4-1, using two different substrates for the pin- and gap-layers. (a) Pin-layer ε_r = 3 and gap-layer ε_r = 5 or 10. (b) Pin-layer ε_r = 5 and gap-layer ε_r = 3 or 10. (c) Pin-layer ε_r = 10 and gap-layer ε_r = 3 or 5.

Similar variations as those described above for the gap height in Figure 4-3 can also be found in Figure 4-5 and Figure 4-6 for the cell period and pin diameter: the gap-layer of higher ε_r forces the lower and the upper cutoffs of the stopband to drop in the frequency, which, however, is limited if the pin-layer with a high ε_r or with small dimensions (i.e., small cell period/pin diameter). However, Figure 4-7 for the pin height shows that the gap-layer ε_r loses its effect in

the stopband for a pin height of over about 0.6 mm. This means that the increment or decrement imposed on the pin effective electrical length from the changed gap-layer ε_r is negligible, for the metal pin with a relatively large physical length. Such a behavior appears more distinct in the upper cutoff frequencies than the lower ones. The total stopband bandwidth, corresponding to the lower and the upper cutoff frequencies in Figure 4-5, Figure 4-6, and Figure 4-7, was also computed, which is also almost entirely dependent on the pin-layer ε_r and the dimensions (cell period, pin diameter, pin height), as seen in Figure 4-4 for the gap height. Thus, in the design of using different substrates for the pin- and gap-layers, the band size can be easily predicted by the case for the two layers using the same substrate as the one in the pin-layer.

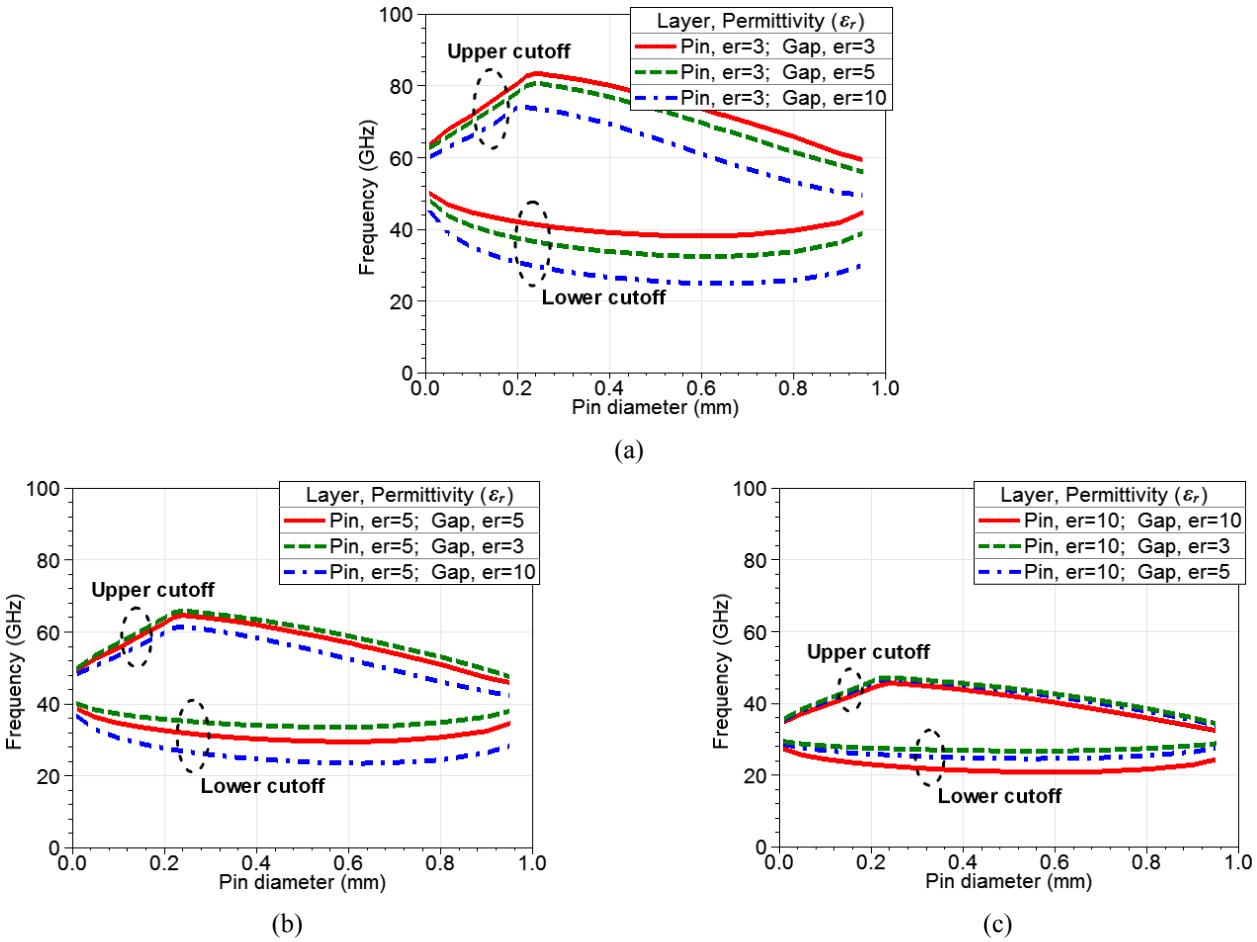
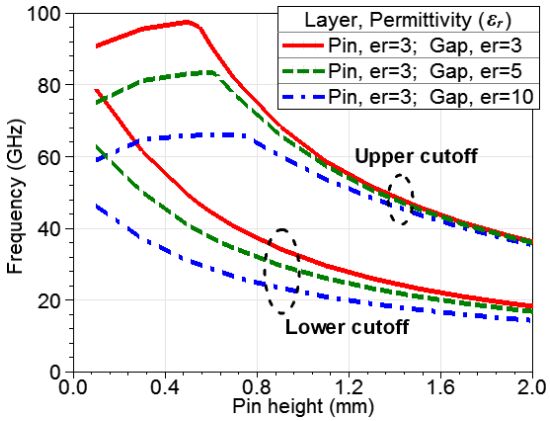
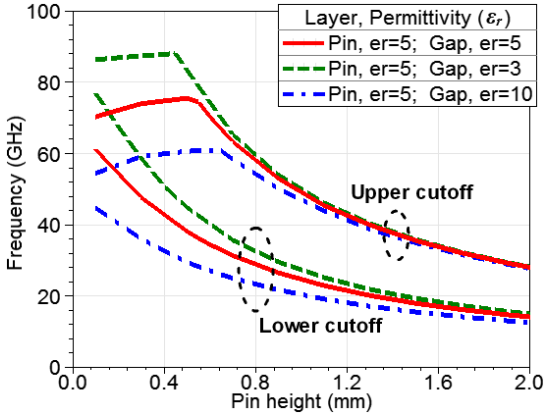


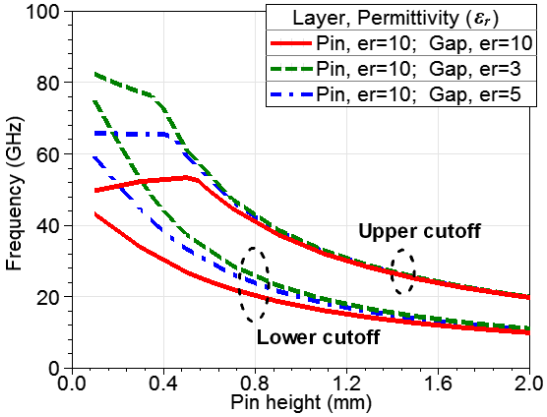
Figure 4-6 Change in the lower and upper cutoff frequencies with pin diameter for one unit cell shown in Figure 4-1, using two different substrates for the pin- and gap-layers. (a) Pin-layer ε_r = 3 and gap-layer ε_r = 5 or 10. (b) Pin-layer ε_r = 5 and gap-layer ε_r = 3 or 10. (c) Pin-layer ε_r = 10 and gap-layer ε_r = 3 or 5.



(a)



(b)



(c)

Figure 4-7 Change in the lower and upper cutoff frequencies with pin height for one unit cell shown in Figure 4-1, using two different substrates for the pin- and gap-layers. (a) Pin-layer $\varepsilon_r = 3$ and gap-layer $\varepsilon_r = 5$ or 10. (b) Pin-layer $\varepsilon_r = 5$ and gap-layer $\varepsilon_r = 3$ or 10. (c) Pin-layer $\varepsilon_r = 10$ and gap-layer $\varepsilon_r = 3$ or 5.

4.3 Transition between Packaged Microstrip Line and Standard Microstrip Line

This section is to design the transitions between the proposed packaged microstrip line and the standard microstrip line, which is needed for further investigations of this new line in-band transmission performance and for future measurements. Two different transition structures are presented in Figure 4-8 and Figure 4-9. The only difference between them is whether the middle-layer substrate covers the input-output tapered microstrip transitions. It is seen that the gap-layer shown in Figure 4-1 is comprised of the middle- and base-layer substrates. Since the printed strip on the base-layer substrate is very narrow, its effect on the generated stopband characteristics is negligible.

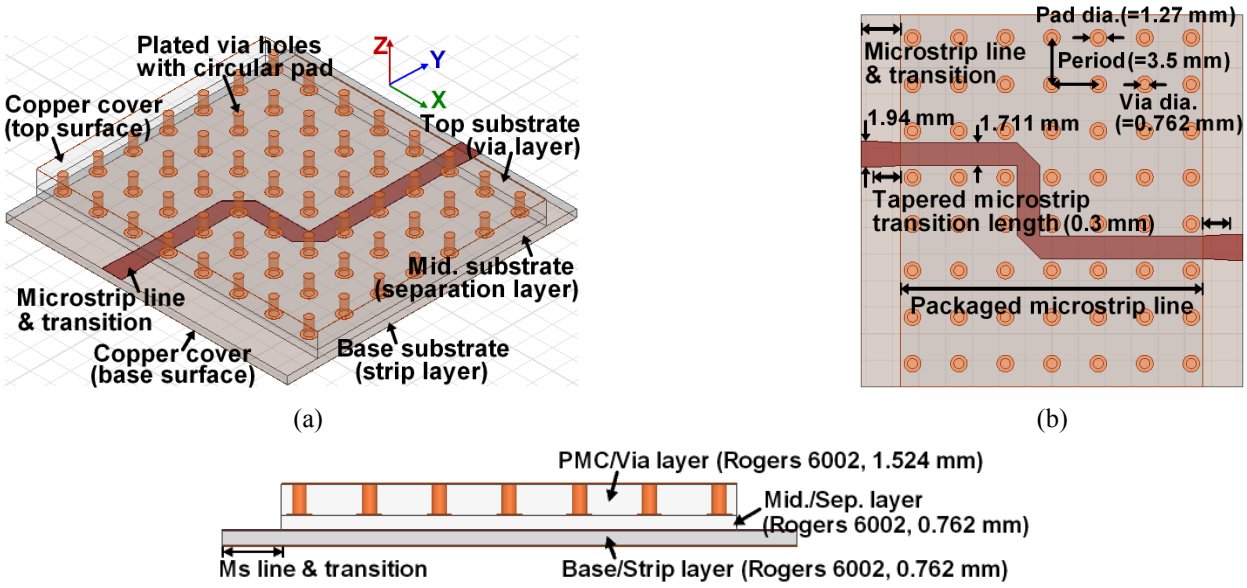


Figure 4-8 Packaged microstrip line with double 90° bends and with transitions to standard microstrip lines (middle layer does not cover the tapered microstrip transitions on base layer). (a) Overview. (b) Top view. (c) Side view.

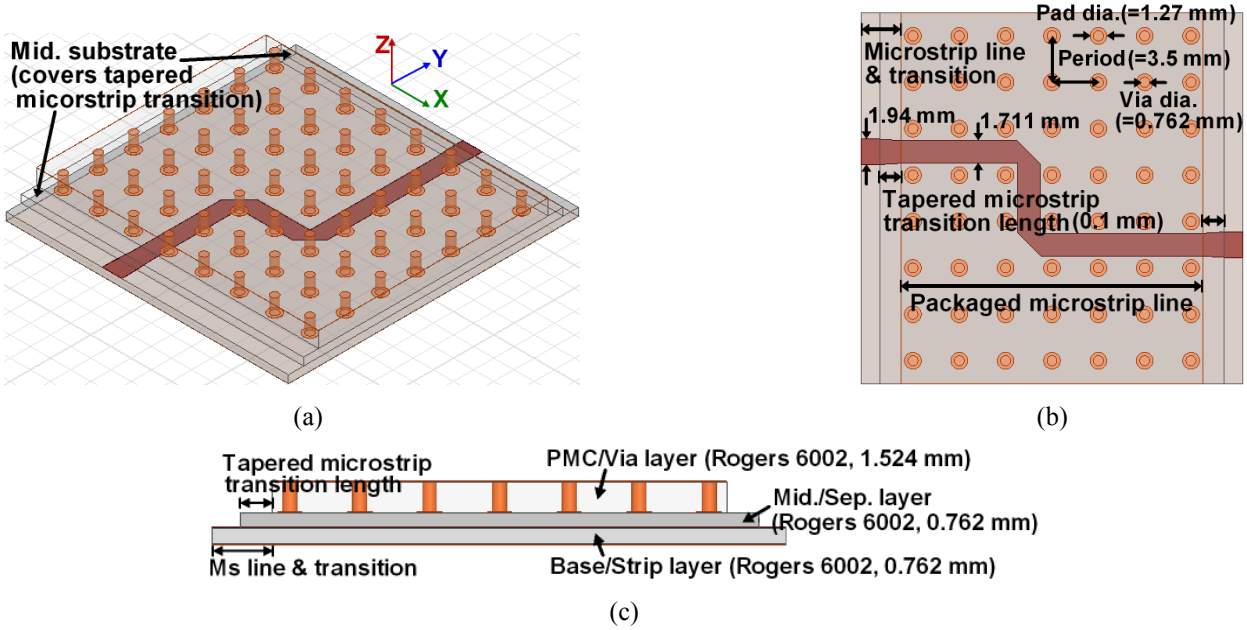


Figure 4-9 Packaged microstrip line with double 90° bends and with transitions to standard microstrip lines (middle layer covers tapered microstrip transitions on base layer). (a) Overview. (b) Top view. (c) Side view.

In both the designs shown in Figure 4-8 and Figure 4-9, the base-layer substrate thickness is 0.762 mm, Rogers RT/Duroid 6002, with ε_r of 2.94 and tan δ of 0.0012. The metal strip with two 90° bends has a width of 1.711 mm for 50 Ω at the desired center operating frequency of

20.5 GHz. The width is calculated when the strip is covered only by the middle substrate (i.e., without the top PMC-layer) as an embedded microstrip line [71], [72]. The chamfered strip bends are optimized with the PMC shielding to minimize the possible discontinuities. The width of the input-output standard microstrip line is 1.94 mm for 50 Ω at 20.5 GHz. The length of the tapered microstrip transitions is fine-tuned to offer the best impedance matching in the overall band. For the transition configuration in Figure 4-8, the optimized tapered length is 0.3 mm, while it is 0.1 mm for that in Figure 4-9 in which the middle layer covers the tapered microstrip. The middle substrate thickness of both the designs is 0.762 mm, Rogers RT/Duroid 6002.

The top-layer substrate is applied to build the PMC shielding, which is realized by a periodic plated via with a period of 3.5 mm and a diameter of 0.762 mm. Owing to the platting process, a circular metal pad of 1.27 mm diameter must be attached to the via hole. The substrate adopted for this layer is also Rogers RT/Duroid 6002 but is of 1.524 mm thickness. The above conditions generate an operating bandwidth from 16 to 25 GHz, as presented in Figure 4-10. In addition, it shows that the in-band transmission performance of the above two built transitions is almost identical. The one without covering the tapered microstrip (Figure 4-8) is selected in the following study for simplicity.

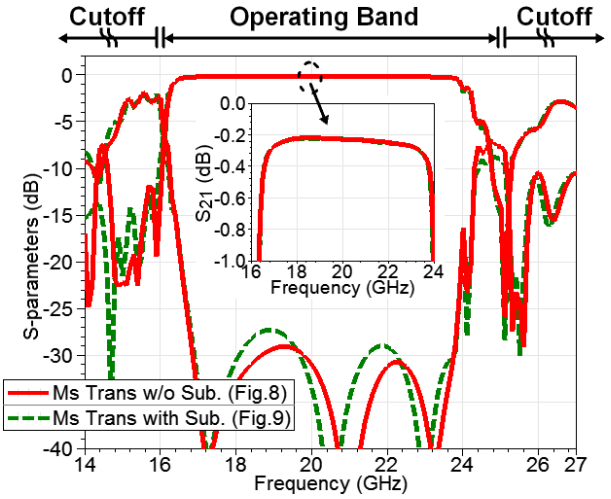


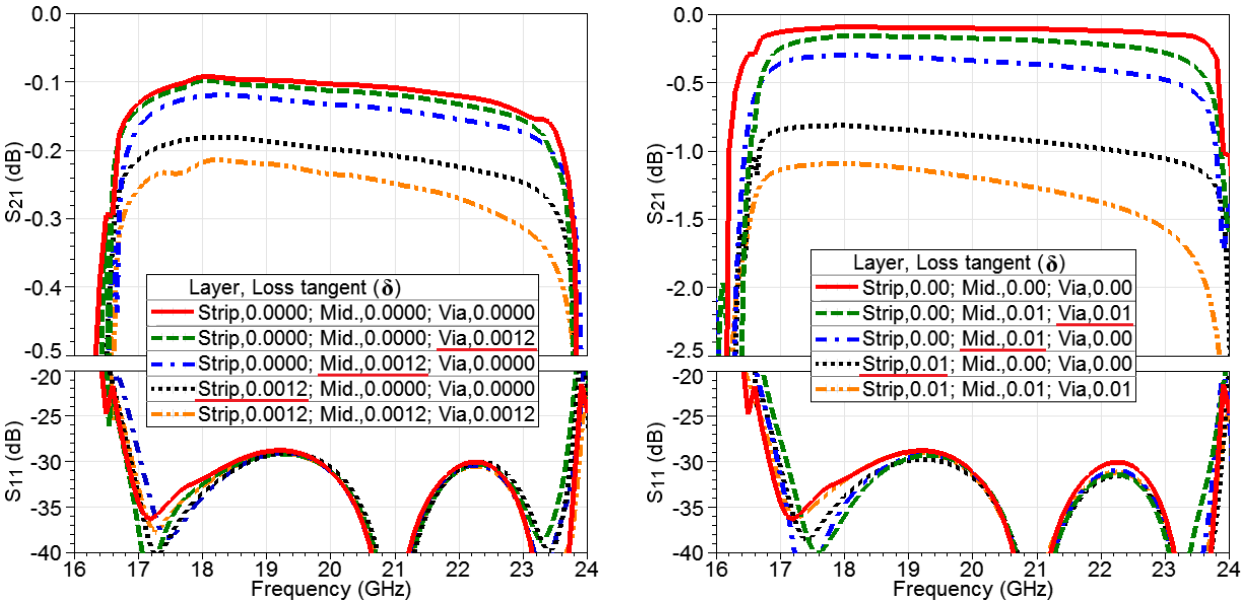
Figure 4-10 Simulated performance of two transition configurations presented in Figure 4-8 and Figure 4-9 for whether the middle layer covers the tapered microstrip.

4.4 Study of In-Band Transmission Performance

This section focuses on the effects of the top PMC/via-layer in the dielectric/conductor losses and the characteristic impedance of the packaged microstrip line. The investigations are based on the structure built in Figure 4-8 and will be helpful in the choice of a proper substrate for each layer of this proposed new line in the transmission performance, beyond the stopband characteristics considered previously.

4.4.1 Study of Dielectric and Conductor Losses

In order to observe the contribution from each layer substrate to the line dielectric losses, each case study presented in Figure 4-11 considers only one layer tan δ (i.e., the other two layers tan δ is fixed at "0"). For comparison, the cases of all the three layers with tan δ = 0 (no dielectric losses), 0.0012, and 0.01 are also provided in Figure 4-11. As the substrates ε_r is kept at 2.94, no significant change is presented in the in-band return loss.



(a) (b)

Figure 4-11 Simulated S-parameters of the packaged microstrip line with two 90° bends for each layer dielectric losses. (a) tan δ = 0.0012. (b) tan δ = 0.01.

As seen by the dashed green curve in Figure 4-11 (a), the dielectric losses due to the lossy top PMC-layer substrate are so small that they can be neglected compared with the lossless case shown by the solid red curve in Figure 4-11 (a). This proves that the wave is almost suppressed

under the PMC-layer and the power leakage in this layer is insignificant. Consequently, it is also indicated that the power consumed by the plated vias in the top PMC-layer and the top copper cover is very small. Thus, the line total conduction losses will not be increased. Besides, Figure 4-11 (a) reveals that the dielectric losses due to the middle-layer are also very small, and the base strip-layer is the primary source of the dielectric losses. This is because that the wave is mainly concentrated between the metal strip and the ground plane. As shown above, similar variations due to each layer dielectric losses are observed in Figure 4-11 (b), even if the tan δ under test is enlarged to 0.01, around 10 times over that in Figure 4-11 (a).

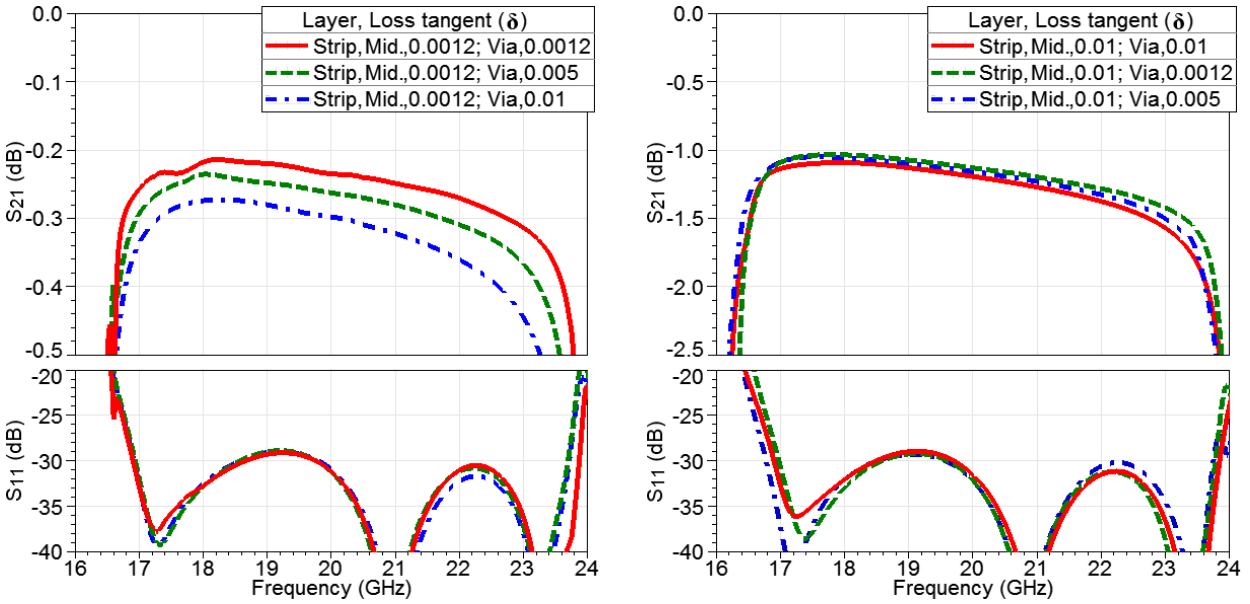
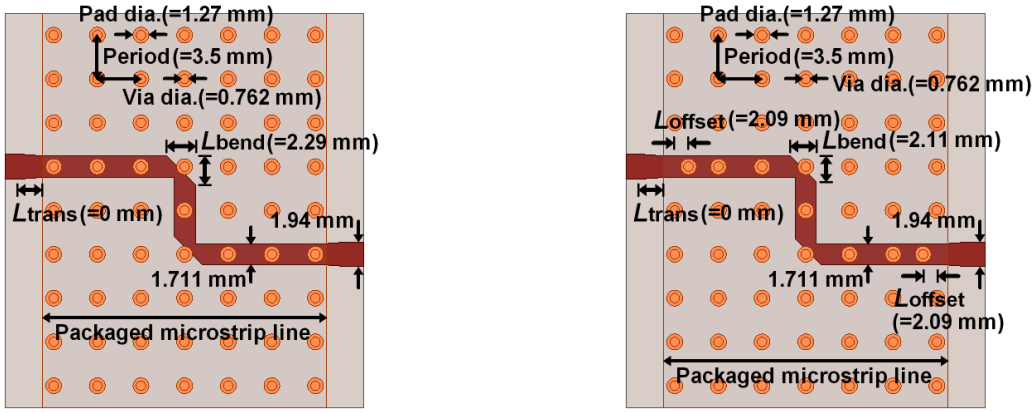


Figure 4-12 Simulated S-parameters of the packaged microstrip line with double 90° bends for dielectric losses from the PMC/via-layer. (a) Strip- and middle-layers tan δ = 0.0012, but via-layer tan δ = 0.0012, 0.005, or 0.01. (b) Strip- and middle-layers tan δ = 0.01, but via-layer tan δ = 0.0012, 0.005, or 0.01.

To further demonstrate the above statements for the effect of the PMC/via-layer substrate on the line loss, Figure 4-12 shows two more real situations, in which each layer substrate of the packaged microstrip line is lossy. The strip- and middle-layers tan δ are fixed at 0.0012 and 0.01, and only the pin-layer tan δ is varied. Still, as seen in Figure 4-12, the line dielectric losses are mostly determined by the layers under the PMC, while the PMC-layer substrate does not play a significant role.



(a) (b)

Figure 4-13 Overview of a packaged microstrip line with double 90° bends and with transitions to standard microstrip lines (plated vias directly over the metal strip). (a) General type. (b) Modified type (i.e., the input-output vias over the strip are offset for impedance matching transition).

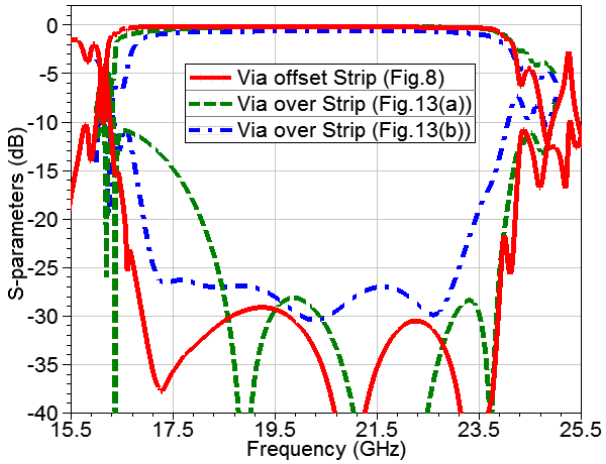
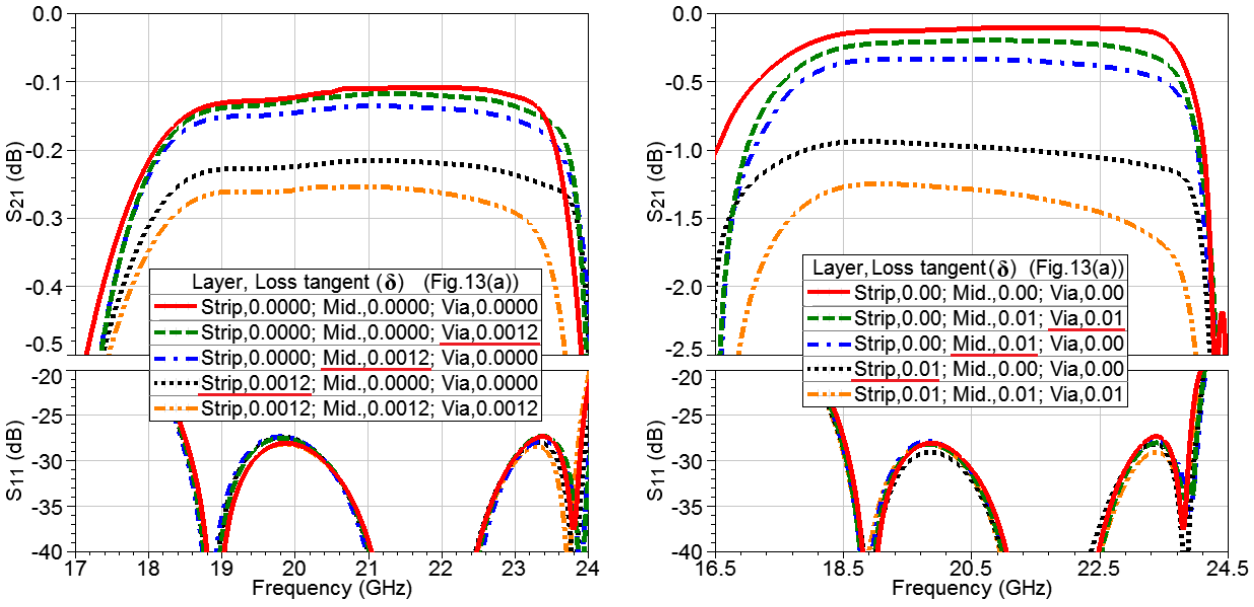


Figure 4-14 Simulated performance comparisons of the packaged microstrip line presented in Figure 4-8 and Figure 4-13 (a) and (b).

Figure 4-13 (a) is another case study of the line loss, in which the plated vias are directly over the metal strip. This should be taken into consideration since more power could be coupled from the strip to the metallic vias and pads causing more losses in the PMC layer compared to the case in Figure 4-8, in which the metal strip and plated vias are offset. The two 90° bends and transition length are reoptimized (L_{bend} = 2.29 mm, L_{trans} = 0 mm) for the in-band performance. The dashed green curve shown in Figure 4-14 indicates that the performance of the configuration in Figure 4-13 (a) agrees well with the case of Figure 4-8 (the solid red curve in Figure 4-14), except for the reflection coefficients at the passband lower end. To deal with this problem, one more parameter is proposed and applied in this design, which is the offset distance (L_{offset}) of the

input-output plated vias over the metal strip, as indicated in Figure 4-13 (b). By fine-tuning L_{offset} with proper L_{bend} and L_{trans}, better impedance matching transition at lower frequencies is achieved and improved return loss, as proven by the dotted-dashed blue curve in Figure 4-14. The selected optimal dimensions are L_{offset} = 2.09 mm, L_{bend} = 2.11 mm, and L_{trans} = 0 mm. The design tradeoff of this modification is only a slight shift and reduction in the passband, compared to the solid red curve in Figure 4-14 of offsetting the strip and vias. The loss analysis for this case of the plated vias directly over the metal strip is shown in Figure 4-15, considering without tuning the plated vias as that in Figure 4-13 (a). However, it shows that even if the plated vias are directly over the metal strip, the losses caused by the PMC-layer are still much smaller than that of the strip-layer substrate. Moreover, no additional increment is found in the total loss (see the dotted-dotted-dashed yellow line in Figure 4-15) compared to its counterpart shown in Figure 4-11, even when the substrate tan δ is increased to 0.01, as seen in Figure 4-15 (b).



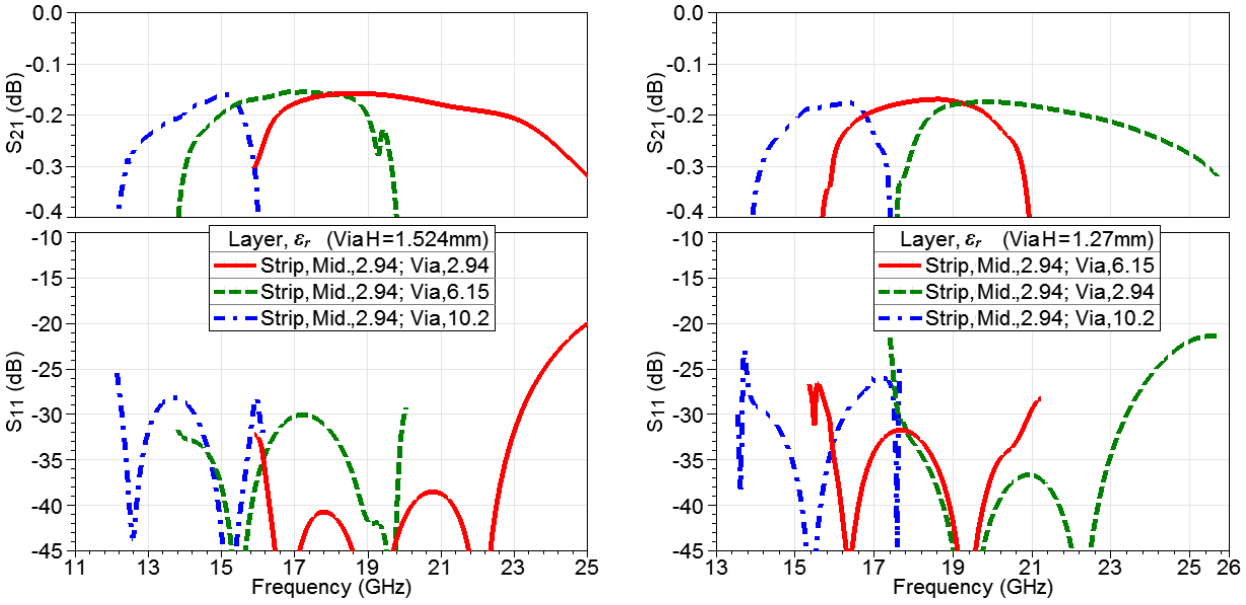
(a) (b)

Figure 4-15 Simulated S-parameters of the packaged microstrip line with two 90° bends for each layer dielectric losses. (a) tan δ = 0.0012. (b) tan δ = 0.01.

In general, to minimize the losses of the packaged microstrip line, significant efforts should be devoted to select a proper base-layer substrate of a low tan δ and a proper thickness. The absence of radiation and surface waves makes a thicker strip-layer substrate available in the packaged microstrip line to reduce the conduction losses.

4.4.2 Line Impedance Affected by PMC Layer

Further to the above study of line losses, this part explores the effect of the PMC-layer ε_r on the characteristic impedance of the packaged microstrip line and gives a guideline to design the line width for a given characteristic impedance at the operating frequency. To avoid the possible interference of the strip bend, a straight through packaged microstrip line, i.e., without bends, is adopted in the following impedance analyses.



(a) (b)

Figure 4-16 Simulated S-parameters of a straight through packaged microstrip line for the strip- and middle-layers ε_r = 2.94, but via-layer ε_r = 2.94, 6.15, or 10.2. (a) Via-layer 1.524 mm thick. (b) Via-layer 1.27 mm thick.

The simulated results are given in Figure 4-16 (a) to present the performance only within the passband, based on the structure in Figure 4-8 with the same substrates, dimensions, and transitions. It is shown that the increase in ε_r of the PMC-layer from 2.94 to 6.15 or 10.2 not only changes the passband but also degrades the in-band reflection coefficients. This reveals that the increased PMC-layer ε_r makes the characteristic impedance of the packaged microstrip line change, and therefore degrades the impedance matching transition that is designed under the case of the PMC-layer ε_r = 2.94. However, Figure 4-16 (a) also shows that, even if ε_r is enlarged to 10.2 (around 3.5 times over 2.94), the return loss within the passband is still below -28 dB. This indicates that the line characteristic impedance variation due to the increased ε_r of the PMC-layer is not significant – i.e., at an acceptable level.

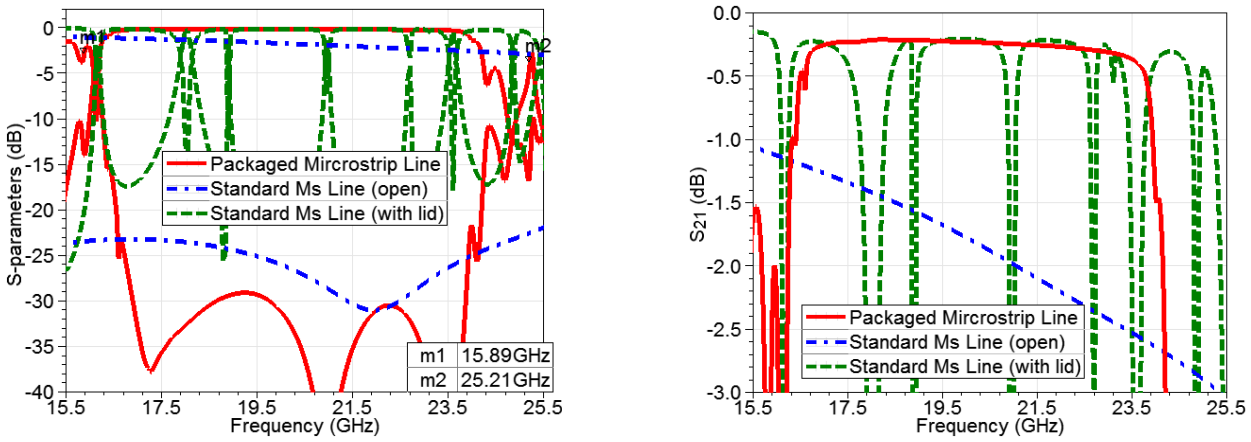
In addition, Figure 4-16 (b) presents the simulated results for another prototype of the packaged microstrip line. Other than the design in Figure 4-8, the top PMC-layer is replaced by another substrate, i.e., Rogers RT/Duroid 6006 with a thickness of 1.27 mm, ε_r of 6.15, and tan δ of 0.0027, which generates a passband from 15.36 to 21.23 GHz. The input-output microstrip line width and the optimal transition length are modified as 1.93 and 0.2 mm, respectively, for 50 Ω at the above modified passband center frequency. The other substrates and dimensions are kept the same as before. The performance of this modified prototype is presented as the solid red curve in Figure 4-16 (b). Similar to Figure 4-16 (a), under the built transition for the case of the PMC-layer ε_r = 6.15, the change in this layer ε_r from 6.15 to 2.94 or 10.2 does not cause too much variation in the line characteristic impedance, and thus the changed inband return loss is also in an acceptable range.

Thereby, in the design, the width of the packaged microstrip line of 50 Ω at the operating frequency can be simply calculated by the embedded microstrip line model without considering the PMC-layer ε_r, as presented in Section 4.3. However, to obtain a more accurate line width, optimization/fine tuning with the PMC-layer is needed, especially when the ε_r difference between the PMC-layer and the layers under it is too large.

4.4.3 Comparisons with Standard Microstrip Line

The final part of this section is to verify the performance of the packaged microstrip line over the standard microstrip line and the conventional shielding solution with a smooth metal lid. The packaged microstrip line is that given in Figure 4-8 with the same dimensions and substrates. So the standard microstrip line used for comparison has a width of 1.94 mm, on the substrate of 0.762-mm-thick Rogers RT/Duroid 6002, the same substrate as used in the bottom layer of this packaged microstrip line. The microstrip line is also with two 90° bends that are optimized under the unpackaged condition for the best performance. The smooth shielding lid for the microstrip line is located at 4.34 mm, i.e., 5.7 times of the used substrate thickness, above the line to avoid affecting its characteristics. The simulated results of this novel packaged microstrip line, and the standard microstrip line (without and with the shielding lid) are compared in Figure 4-17. The observed much larger insertion loss in the case of the standard microstrip line without shielding is due to the significant radiation caused by the heavy discontinuities of the metal strip from the two 90° bends. The radiation losses and interference grow even more severe with the frequency,

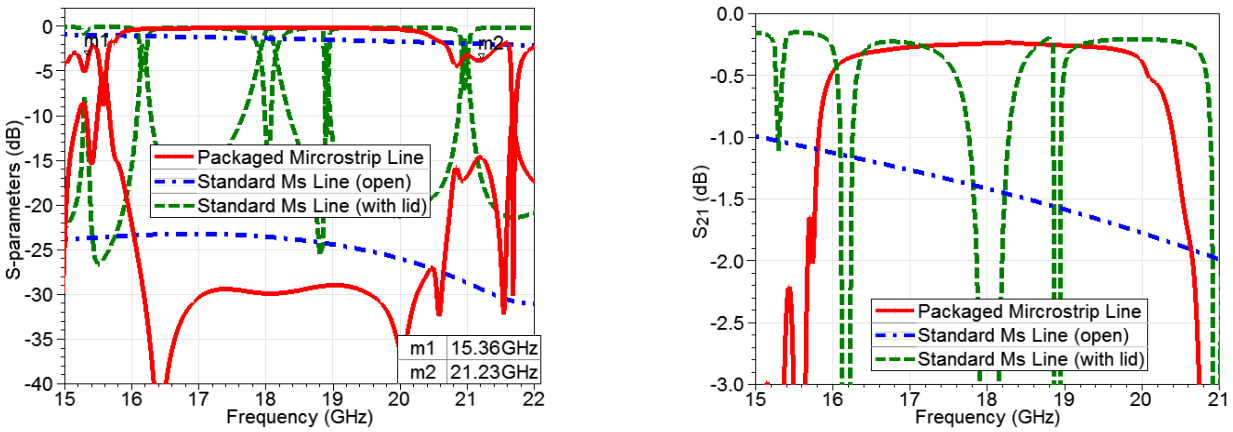
which suggests why the classical microstrip line is not suitable at high frequencies. Although the radiation is suppressed by the bulky shielding box, the resonances inside the cavity limit its use in a broadband application, as shown by the dashed green curves in Figure 4-17. In addition, due to the strip discontinuities, the substrate surface waves will be launched causing additional losses and interference issues. However, Figure 4-17 proves that the proposed packaged microstrip line effectively suppresses the radiation losses and eliminates the possible cavity resonances. And, as explained in Section 4.1, the surface waves in the substrate are prevented within the operating band in the packaged microstrip line with the top-layer PMC shielding. Besides, Figure 4-17 (b) shows that the losses due to the middle- and top-layer substrates are ignorable since the insertion loss of the packaged microstrip line (solid red curve) is at the same level as the standard microstrip line using the shielding box (dashed green curve).



(a) (b)

Figure 4-17 Simulated S-parameters of the packaged microstrip line with two 90° bends (via-layer of 1.524-mm-thick Rogers 6002 substrates), compared to a similar standard microstrip line without/with the shielding using a smooth metal lid. (a) S_{11} and S_{21}. (b) Zoomed-in S_{21}.

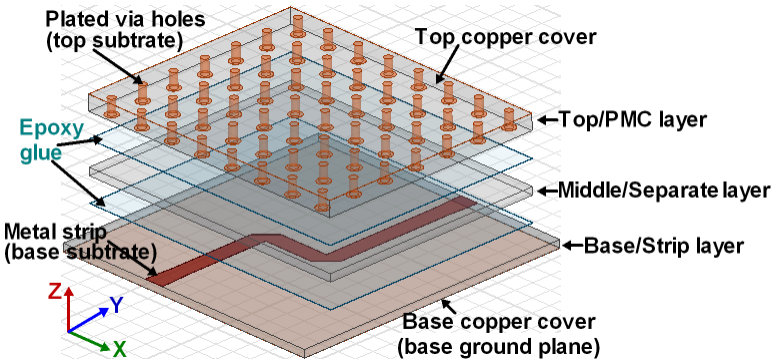
The second prototype of the packaged microstrip line described in the last part of using Rogers RT/Duroid 6006 with 1.27 mm thickness for the top PMC-layer is studied as well with a comparison to the standard microstrip line. The simulated results are given in Figure 4-18, and similar improvements in insertion loss and cavity resonances are observed within the operating band.



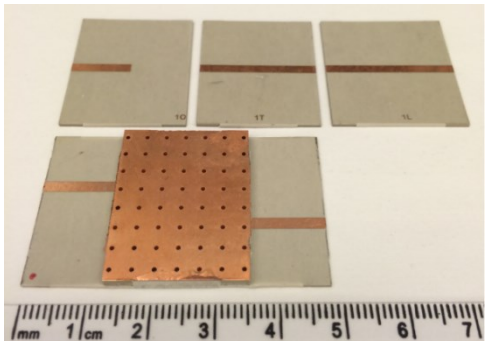
(a) (b)

Figure 4-18 Simulated S-parameters of the packaged microstrip line with two 90° bends (via-layer of 1.27-mm-thick Rogers 6006 substrate), compared to a similar standard microstrip line without/with the shielding using a smooth metal lid. (a) S_{11} and S_{21}. (b) zoom-in S_{21}.

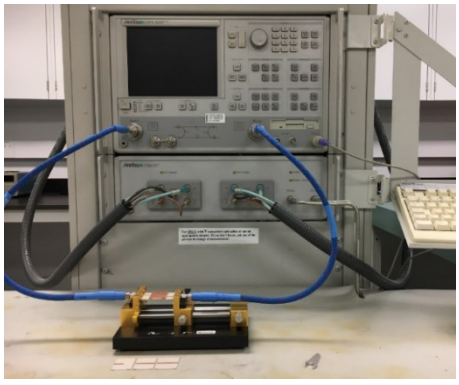
4.5 Experimental Verification and Analysis



(a)

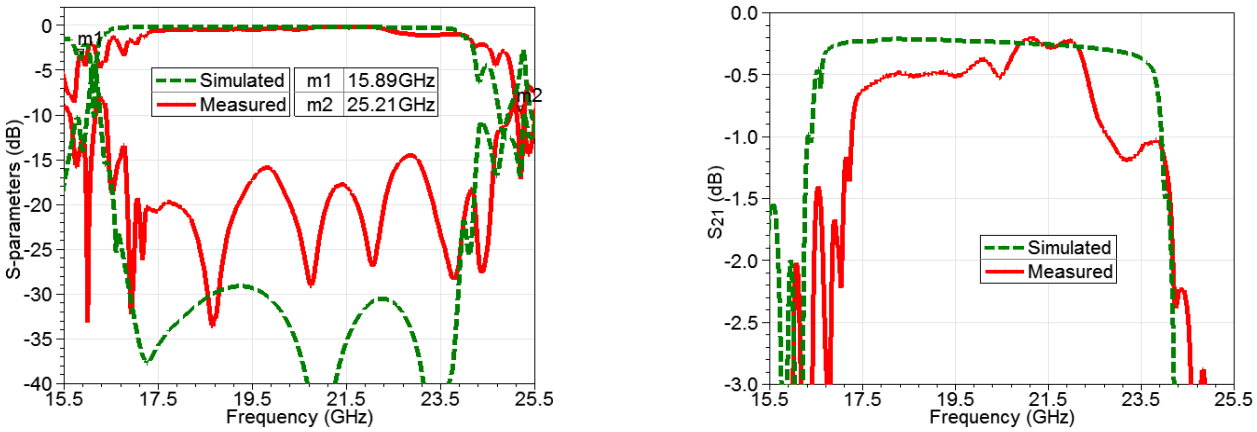


(b)



(c)

Figure 4-19 (a) Distributed 3D view of the fabrication for a packaged microstrip line. (b) Fabricated packaged microstrip line with double 90° bends (via-layer of 1.524-mm-thick Rogers 6002 substrates) and TRL calibration kits. (c) Photograph of the measurement setup.



(a) (b)

Figure 4-20 Measured S-parameters of the packaged microstrip line with double 90° bends (via-layer of 1.524-mm-thick Rogers 6002 substrates). (a) S_{11} and S_{21}. (b) Zoomed-in S_{21}.

The distributed 3D view of a packaged microstrip line is presented in Figure 4-19 (a). The two different prototypes of the packaged microstrip line presented in Section 4.4 have been fabricated. The one of using 1.524-mm-thick Rogers RT/Duroid 6002 for the top PMC/via-layer is shown in Figure 4-19 (b), with the measured and simulated results given in Figure 4-20. The circuit and measured performance of the other prototype with 1.27 mm thick, Rogers RT/Duroid 6006, for the PMC/via-layer are presented in Figure 4-21 and Figure 4-22, respectively. In the fabrication, the plated vias in the top substrate and the metal strip on the base substrate are first made, and then the three substrate layers are stuck together using a thin layer of RF epoxy glue, at high temperature and pressure. The length of the base substrate is 24 mm longer than the above original design only for TRL calibration to remove the test fixture effects in measurements [73]. The fabricated microstrip calibration kit is also shown in Figure 4-19 (b). It has a line width of 1.94 mm and includes the following. 1) A thru of 24-mm length, around two wavelengths at its lowest working frequency of 16 GHz to avoid the input and output coupling of the test fixture causing errors in measurements. 2) An open circuit with a microstrip of 12 mm length, i.e., half-length of the thru. 3) A line that is 2.30 mm longer than the thru, corresponding to a quarter wavelength at its center operating frequency of 20.5 GHz.

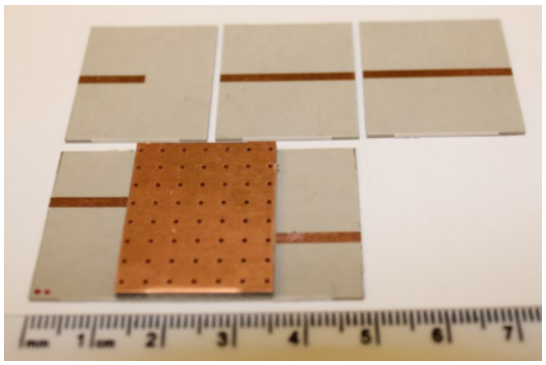
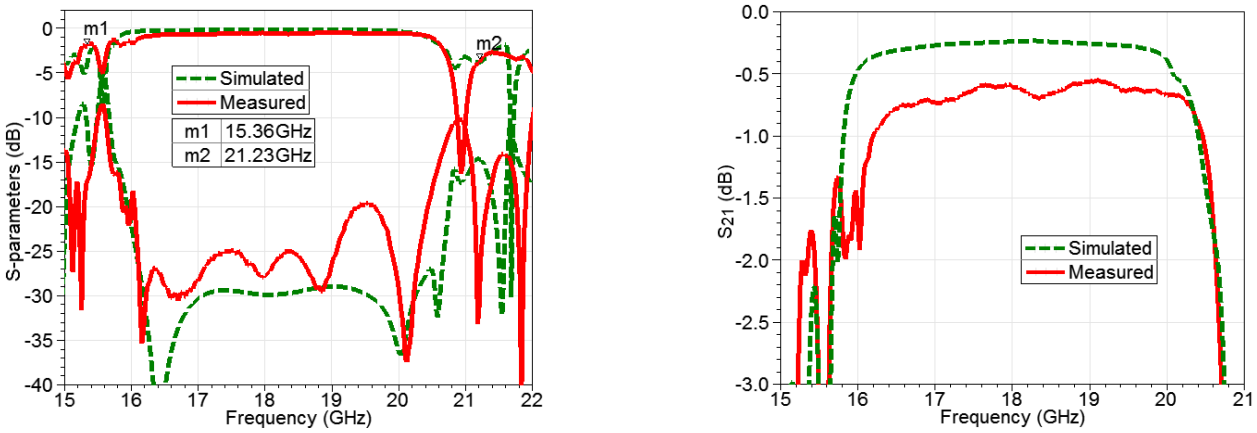


Figure 4-21 Fabricated packaged microstrip line with double 90° bends (via-layer of 1.27-mm-thick Rogers 6006 substrate) and TRL calibration kits.



(a) (b)

Figure 4-22 Measured S-parameters of the packaged microstrip line with double 90° bends (via-layer of 1.27-mm-thick Rogers 6006 substrate). (a) S_{11} and S_{21}. (b) Zoomed-in S_{21}.

Similar to the above, the microstrip calibration kit shown in Figure 4-21 for the second fabricated prototype has a strip width of 1.93 mm, including: 1) a thru of 24 mm length; 2) an open circuit with a microstrip of 12 mm length; and 3) a line that is 2.56 mm longer than the thru, corresponding to a quarter wavelength at its center operating frequency of 18.3 GHz. All the fabricated microstrip calibration kits use 0.762-mm-thick Rogers RT/Duroid 6002, i.e., the same substrate as used in the bottom layer of the above fabricated packaged microstrip lines.

The measured results observed in Figure 4-20 and Figure 4-22 from a VNA present good agreement with the simulated results in both the passband and in-band performance. The shown differences between both the results could be possibly attributed to the glue used in fabrication that was not considered in the simulations. This glue tan δ is 0.03, higher than that of the Rogers RT/Duroid 6002/6006 utilized in the packaged microstrip line, which could increase the

dielectric losses. The glue ε_r is 3.5, different from that of the above two used substrates, which could slightly degrade the designed bend performance and impedance matching transition, as explained in Section 4.4, for the substrate overlying on the base strip-layer top. The differences could also be from the via model used in the simulations, which is simply set as a solid copper cylinder, instead of the real one in practice, which is a via hole with the copper plating [74]-[77]. The measured results could also be possibly affected by other factors, such as fabrication tolerances as well as the substrate frequency-dependent ε_r and tan δ. Nevertheless, the presented results and comparisons have sufficiently demonstrated the concept of this proposed packaged microstrip line, which is promising for cost-effective circuits/components design in both performance and compactness at microwave/mm-wave bands.

4.6 60 GHz Antenna Fed by Packaged Microstrip Line

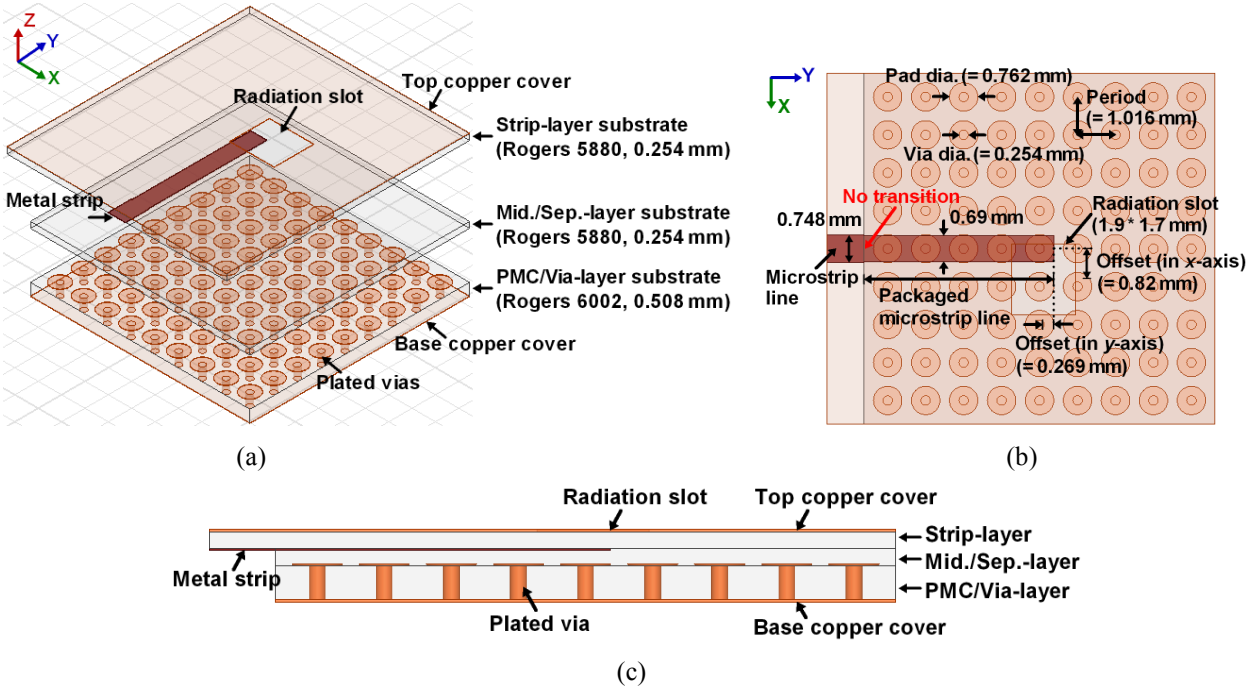
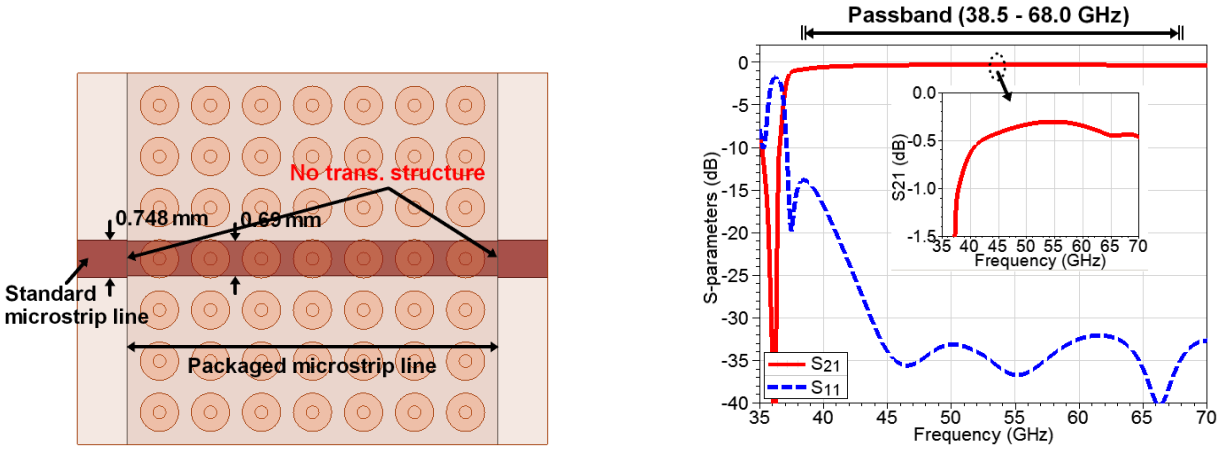


Figure 4-23 Slot antenna fed by a packaged microstrip line, composed of periodic plated vias, a conducting strip-ridge, and three substrates. The top of the upper substrate and the base of the lower substrate are fully covered with copper. (a) Distributed overview. (b) Top view. (c) Side view.

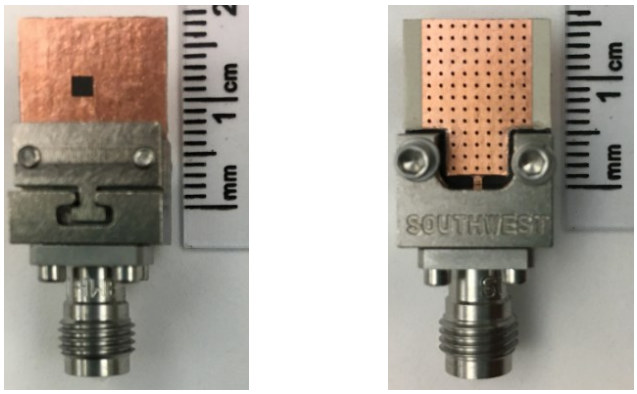
The first antenna constructed on the packaged microwave line is presented in this section, as shown in Figure 4-23. The generated passband is from 38.5 to 68.0 GHz, given the materials and dimensions. No additional transition, such as the tapered microstrip line (shown in Figure 4-

9), is implemented between the packaged microstrip line and the standard microstrip line. The performance of such a connection without transition is provided in Figure 4-24 (b). The photo of the fabricated antenna is presented in Figure 4-25.



(a) (b)

Figure 4-24 Fabricated packaged microstrip line with double 90° bends (via-layer of 1.27-mm-thick Rogers 6006 substrate) and TRL calibration kits.



(a) (b)

Figure 4-25 Photo of the fabricated antenna with end launch connector. (a) Top view. (b) Back view.

In the fabrication, the plated vias in the base substrate and the slot and metal strip on the top substrate are first made, and then the three substrate layers are stuck together using a thin layer of RF epoxy glue, at high temperature and pressure. The measured S_{11} parameters of the slot antenna (including the microstrip line and the end launch connector) from a VNA are given in Figure 4-26 (a), which show good agreement with the simulation. The measured realized gain is presented in Figure 4-26 (b), with a comparison to the simulated realized gain and directivity. The difference between the simulated directivity and realized gain is mainly due to the mismatch

loss and the losses in the feeding network. As the realized gain has taken the return loss into account, the increased S_{11} after 60 GHz can still cause the drop in the gain even if S_{11} is lower than -10 dB. The degraded measured performance presented in Figure 4-26 is possible due to the end launch connector, which was not considered in the simulation and then introduces additional insertion loss and mismatch loss in measurements. A numerical wave port is used in simulations. The other possible factor for the degraded measured performance could be the used RF glue that was also not taken into account in simulations. The glue with ε_r of 3.5 (different from that of the used substrates) and tan δ of 0.03 (larger than that of the substrates) can also cause additional mismatch loss and dielectric losses. Figure 4-26 (c) shows that the calculated radiation efficiency of the single-slot antenna in Figure 4-23 is around 96.5% over the achieved band. The total antenna efficiency, indicated by the dashed green curve, has considered the mismatch loss.

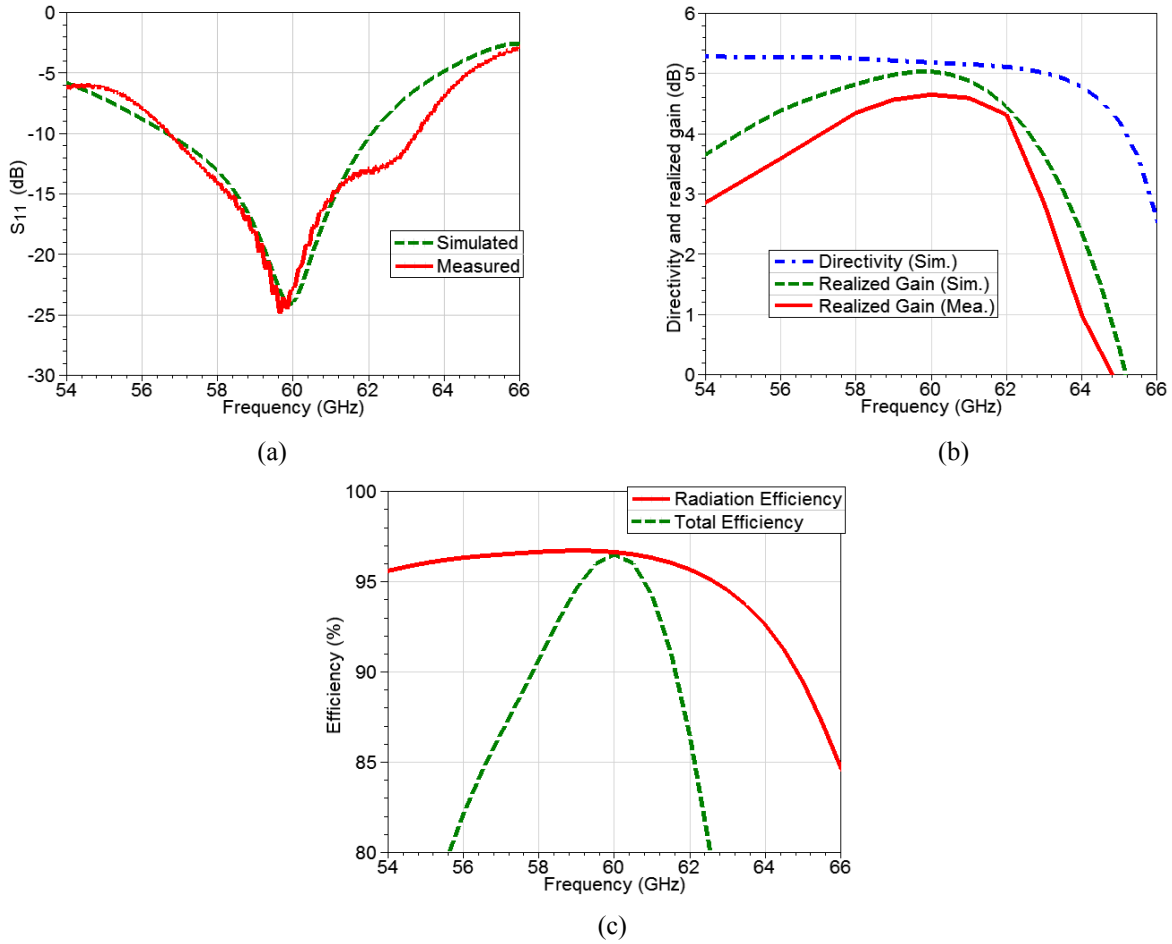


Figure 4-26 (a) Measured and simulated S_{11} of the single-slot antenna fed by a packaged microstrip line. (b) Measured and simulated realized gain of the single-slot antenna, with a comparison with simulated directivity. (c) Simulated radiation efficiency and total efficiency of the single-slot antenna.

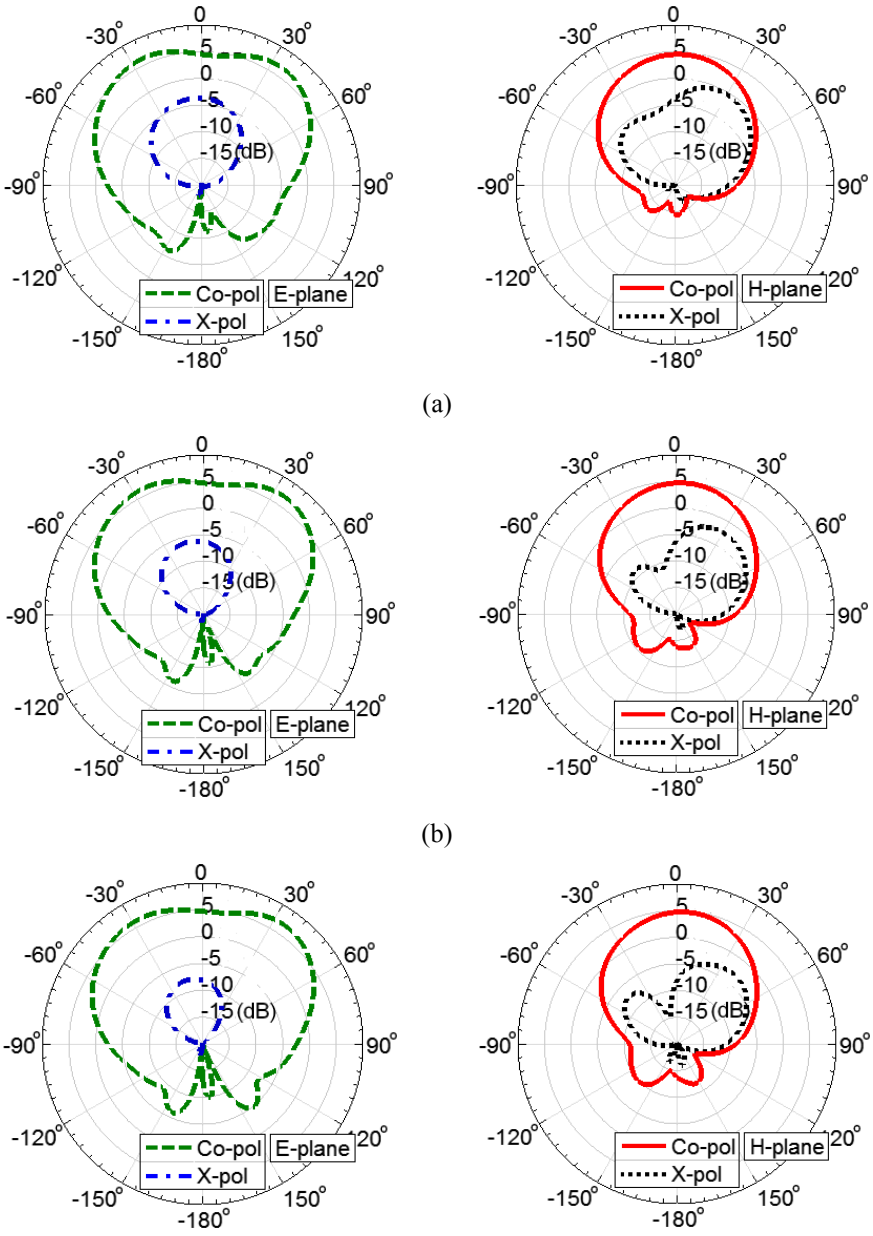
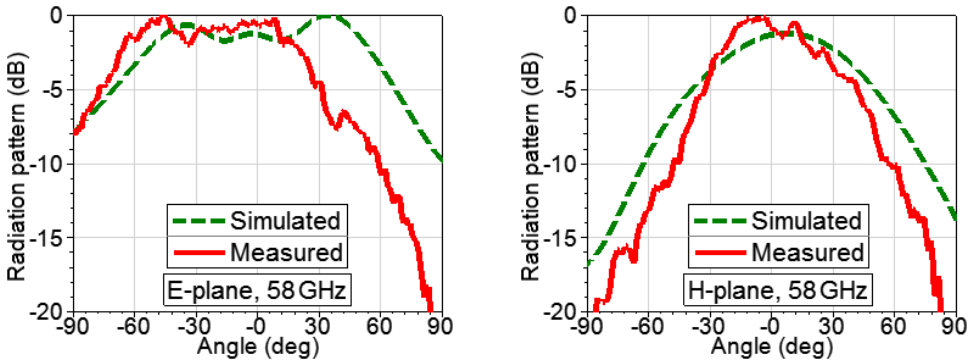


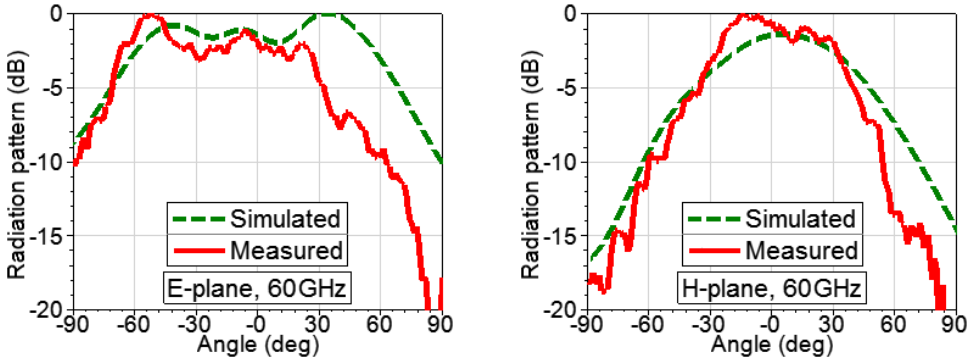
Figure 4-27 Simulated co-polar and cross-polar radiation patterns of the single-slot antenna in E- and H-planes. (a) 58 GHz. (b) 60 GHz. (c) 62 GHz.

The simulated co-polar and cross-polar radiation patterns of the single-slot antenna in E- and H-plane are given in Figure 4-27 at three frequencies of 58, 60, and 62 GHz. The measured and simulated far-field radiation patterns of the antenna in the E- and H-planes at 58, 60, and 62 GHz are compared in Figure 4-28 and provide good agreement. The asymmetry in E- and H-plane is mainly due to the shifting of the slot in both x- and y-axis. Also, the E-plane cut provides the contribution of the used connector. Therefore, the simulated radiation patterns

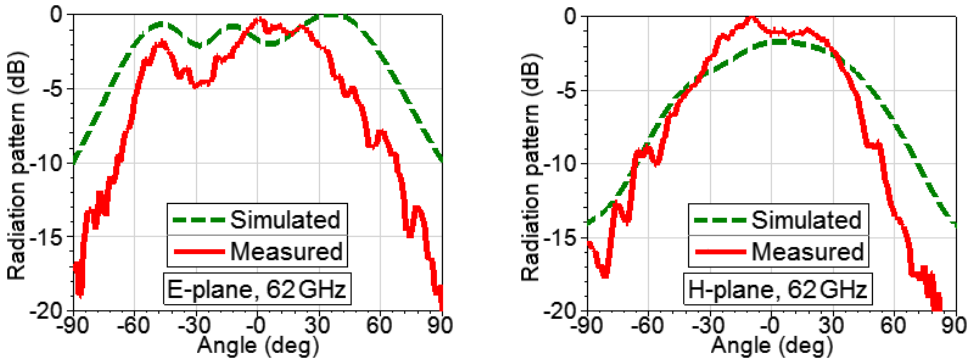
without the connector will have some differences from the measured ones. The observed differences in all the above measured and simulated performance (S_{11}, realized gain, and radiation patterns) could also be possible due to fabrication tolerances, measurement uncertainties, copper surface roughness, and substrate frequency-dependent ε_r and tan δ.



(a)



(b)



(c)

Figure 4-28 Measured and simulated normalized far-field radiation patterns of the single-slot antenna in E- and H-planes. (a) 58 GHz. (b) 60 GHz. (c) 62 GHz.

4.7 Conclusion

A new transmission line called a packaged microstrip line has been presented and studied in this chapter. Without radiation and surface waves, the packaged microstrip line further solves the fabrication issue in the SIGW that requires a strict alignment between the two printed metal strips. The study of stopband, dielectric/conductive losses, and characteristic impedance gives a guide in the choice of a proper substrate for each layer of the packaged microstrip line. In general, the top PMC-layer ε_r has a limited effect on the line loss and impedance, which are mostly determined by the base-layer substrate in which the line fields are concentrated. In contrast, the stopband characteristics are significantly controlled by the PMC layer ε_r. The ε_r of the substrates under the PMC-layer has a negligible impact on the stopband bandwidth. However, it can affect the lower and upper limits of the stopband by altering the pin effective electrical length, typically when the ε_r of other layers is larger than the PMC-layer ε_r. This effect of the substrate between the PMC and PEC can be minimized by adopting proper geometrical dimensions (i.e., small gap height, cell period, and pin diameter; or large pin height), or it can be utilized as a new design freedom to achieve the desired operating band. The transition between the packaged microstrip line and the standard microstrip line has also been studied. It has been proven that the additional transition structure, such as the tapered microstrip, is unnecessary for the packaged microstrip line, which is significant in circuit compactness and design. Two fabricated prototypes offer the required experimental verification. Further, the first antenna prototype realized in this proposed packaged microstrip has also been presented with measurement results.

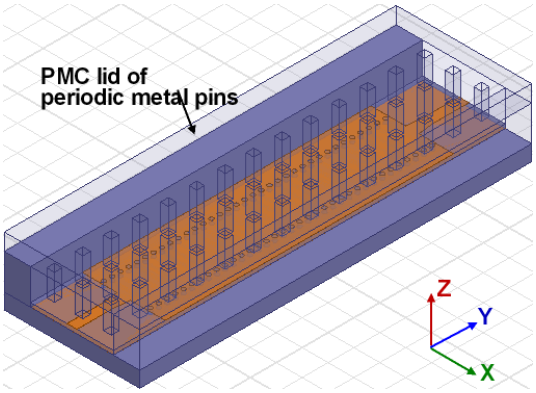
Chapter 5 Gap Waveguide PMC Packaging Technology

5.1 Introduction

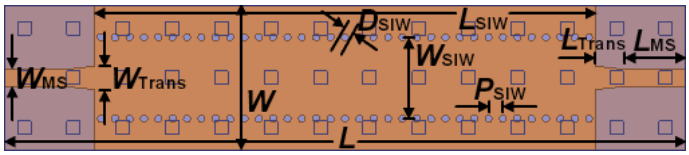
As indicated above, when the separation between the PEC and PMC plates smaller than a quarter wavelength, a propagating quasi-TEM mode is also available if a narrow metal strip over the PMC surface without having any other unwanted modes. Therefore, the other important use of the GW technology is to employ it as an effective packaging technology for planar microstrip circuits, such as microstrip filters [8], [9], microstrip power dividers [10], and active component [11], [12]. In contrast, metal septa and lossy absorbers must be implemented in the conventional shielding solution, as presented in Figure 1-6, to suppress cavity resonances and electromagnetic coupling over the air. Additional ground vias are also required to prevent the adjacent coupling through surface waves in the substrate.

However, all the reported works assumed a smooth PEC/ground plane and concentrated more on the construction of the PMC surface for different applications, such as inverted pyramid -shaped pins [25], the lid of springs [26], and the lid of printed zigzag wires [27]. In reality, the ground plane under the PMC could be non-smooth. Taking the grounded coplanar waveguide (GCPW) for example, many ground vias are implemented along with the slots to reduce the radiation losses and suppress the parasitic parallel-plate modes. Another example is about the SIW connecting with the semi-open microstrip lines. The microstrip line could be the SIW feeding line or used to realize other desired functions [78]-[82]. As a result, the upper PMC lid will have to face two different gap heights – one is from the PMC to the SIW top plate, and the other is the separation between it and the base ground plane. In addition, a dielectric substrate is existent in the air gap. Both the gap height and the substrate ε_r will greatly affect the generated gap-band characteristics. Therefore, the validity and efficiency of this GW-based PMC packaging technology for such an irregular PEC/ground plane should be proven and investigated further, which has been included in this chapter.

5.2 Packaging for SIW Connecting with Microstrip Line



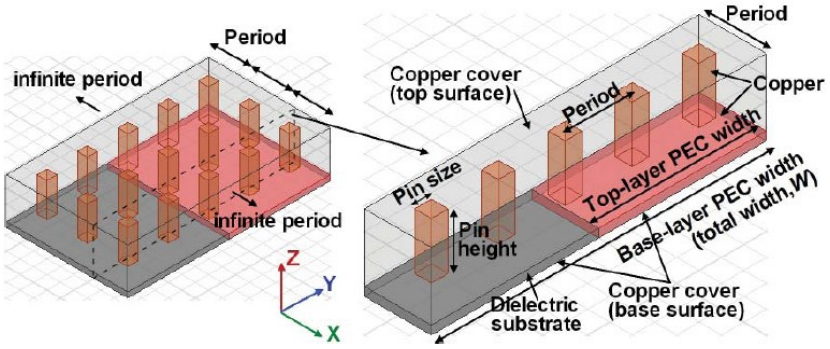
(a)



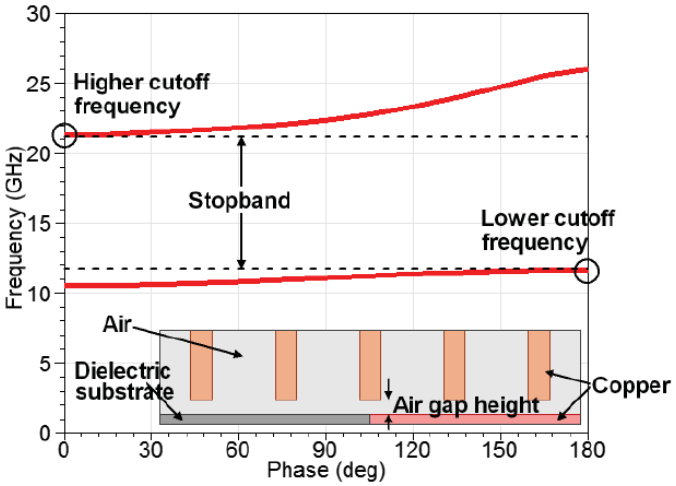
(b)

Figure 5-1 GW PMC packaging for an SIW with transitions to microstrip lines. (a) Overview. (b) Top view.

The GW-based PMC packaging for an SIW with transitions to microstrip feeding lines is shown in Figure 5-1, from which the two different gap heights from the PMC to the base ground plane and the SIW top metal cover are clearly observed. To study such a synthesis gap effect with an inserted substrate, an analysis model is built as illustrated in Figure 5-2 (a). The PMC lid contains infinite periodic metal pins in the longitudinal plane, but limited five-column pins in the transverse extent. The used substrate is Rogers RT/Duroid 6002 with ε_r of 2.94 and thickness of 0.762 mm. The PEC block next to the substrate is used to represent the SIW top metal cover. Considering the dimensions – pin size of 1.5 mm, pin height of 5.0 mm, air gap height of 1.0 mm, cell period of 6.0 mm, and total width (W) of 30 mm, the calculated dispersion diagram from the HFSS Eigenmode solver is shown in Figure 5-2 (b). The generated stopband, i.e., gap band, is from around 12 to 21 GHz.



(a)



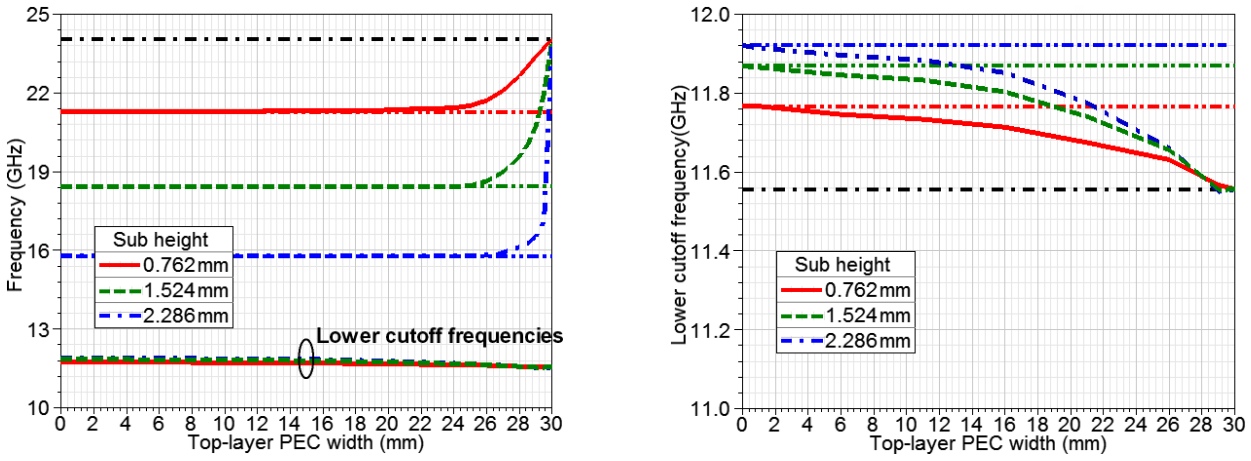
(b)

Figure 5-2 (a) GW unit cell with two-layer PEC surfaces: infinite periodic metal pins in the longitudinal plane, but limited five-column pins in the transverse extent. (b) Dispersion diagram of the unit cell: pin size of 1.5 mm, pin height of 5.0 mm, air gap height of 1.0 mm, cell period of 6.0 mm, and a substrate thickness of 0.762 mm (Rogers RT/Duroid 6002 with ε_r of 2.94).

5.2.1 Unit Cell-Based Study

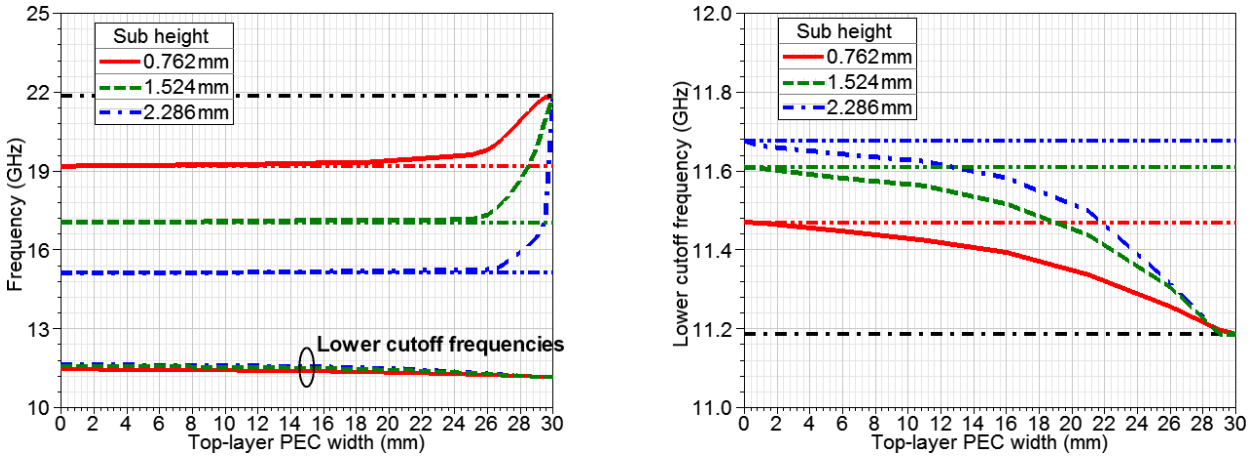
As presented by the solid red curves in Figure 5-3 (a) for the substrate thickness of 0.762 mm, the higher cutoff frequency remains unchanged with the increased width of the PEC/copper block until the width increases to around 24 mm. This also happens to the substrate thickness of 1.524 or 2.286 mm as presented by the dashed green or dotted-dashed blue curves in Figure 5-3 (a), respectively. The air gap height is fixed at 1.0 mm for each case. In contrast, no obvious variations occur in the lower cutoff frequencies with the PEC width for those three substrates' thickness as seen in Figure 5-3 (b). It indicates that the stopband is mostly determined by the gap with a larger height. The smaller gap height between the PMC and the upper metal cover becomes significant only when the upper metal cover is so large that makes the substrate face

only one pin-cell period. The above observation is still valid even when the size of the square metal pin increases from 1.5 to 3.0 mm, as presented in Figure 5-4.



(a) (b)

Figure 5-3 Change in stopband with top-layer PEC width at three different substrate heights. (a) Lower and higher cutoff frequencies. (b) Zoomed-in view of lower cutoff frequencies. A square-shaped pin with a size of 1.5 mm is used.

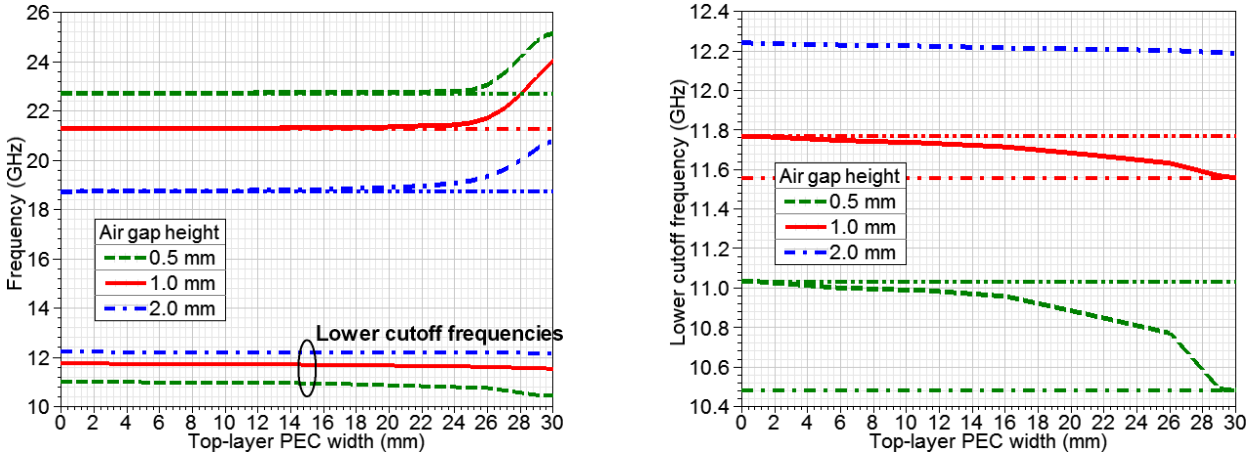


(a) (b)

Figure 5-4 Change in stopband with top-layer PEC width at three different substrate heights. (a) Lower and higher cutoff frequencies. (b) Zoomed-in view of lower cutoff frequencies. A square-shaped pin with a size of 3.0 mm is used.

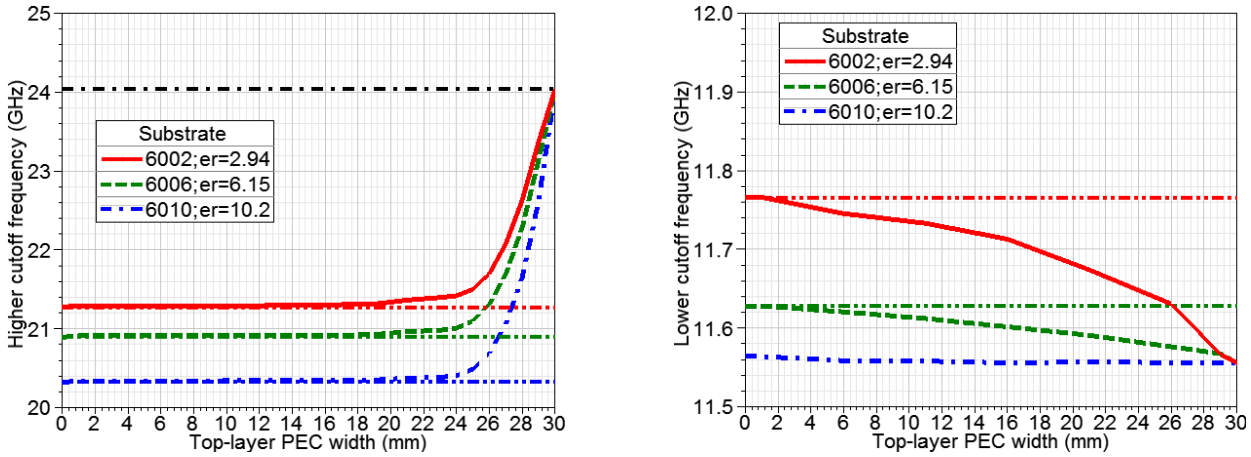
The effect of the air gap height with two layers PEC surfaces is also studied considering different air gap heights and shown in Figure 5-5. It is found that with a larger air gap height the higher cutoff frequency shows more sensitive to the increased width of the PEC block. However, it is found that the apparent variation in the higher cutoff frequencies still happens at the PEC

block width of 24 mm, which makes the substrate face only one pin-cell period. Similar behavior can be found in Figure 5-6 which studies the effect of the substrate ε_r with two layers PEC planes since the substrate is exposed to the upper PMC shielding. The differences shown in Figure 5-6 (a) with the three ε_r show that a higher ε_r may slightly delay the effect of the smaller gap due to the enlarged PEC block width, as shown by the dotted-dashed blue curve for ε_r = 10.2. However, the caused variations are still so small that can be ignored. Therefore, for the GW PMC shielding with two different gap heights, we should take more care of the gap with a larger height, except for the substrate facing only one pin-cell period.



(a) (b)

Figure 5-5 Change in stopband with top-layer PEC width at three different air gap heights. (a) Lower and higher cutoff frequencies. (b) Zoomed-in view of lower cutoff frequencies.



(a) (b)

Figure 5-6 Change in stopband with top-layer PEC width and three different substrates. (a) Higher cutoff frequencies. (b) Lower cutoff frequencies.

5.2.2 GW PMC Packaging for SIW with Microstrip Lines

The simulated performance for the designed GW PMC packaging in Figure 5-1 is shown in Figure 5-7 (a), with the same materials and dimensions except for the cell period of 5.5 mm. To meet with the generated stopband from around 11 to 23 GHz, the SIW dimensions are chosen as summarized in Table 5-1 with the dimensions of the microstrip lines and tapered transitions. The performance of a shorter SIW (i.e., L_{SIW} = 30.11 mm) using the above built PMC shielding is also presented in Figure 5-7 (a). The length of the microstrip line, L_{MS}, for this shorter SIW is increased to 19.8 mm due to the fixed circuit length L = 75.71 mm. As presented by the dashed green curves, the higher cutoff frequency drops in the case of the shorter SIW (i.e., decreased the width of the top-layer PEC plane) and the change in the lower cutoff frequency is very small, corresponding to the previous cell-based study shown in Figure 5-3. Besides, as presented in Figure 5-7 (b), the packaging is still effective even if the PMC shielding lid with only two-row pins. The different in-band performance is because of the characteristic impedance of the microstrip line, which is affected by the upper PMC lid.

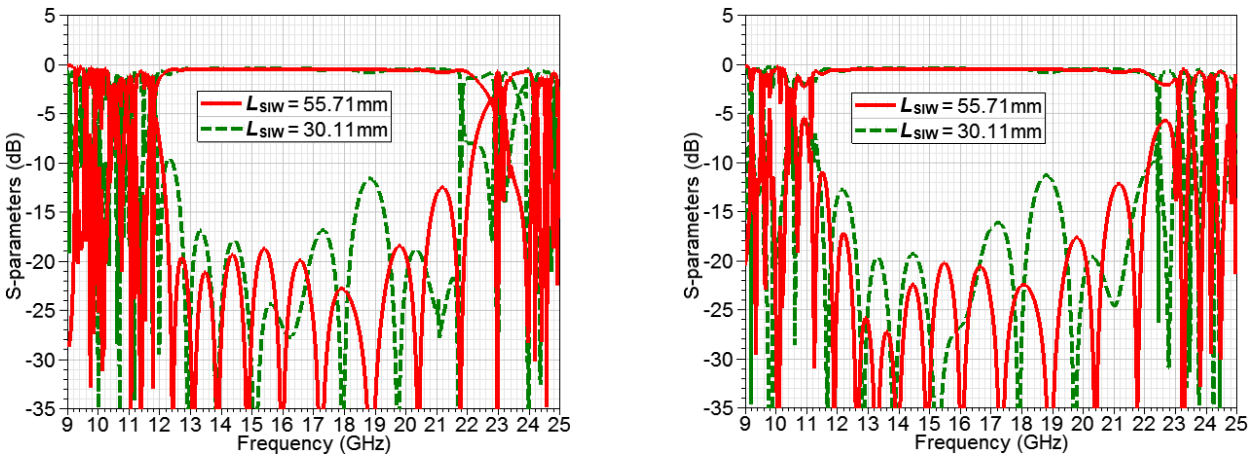


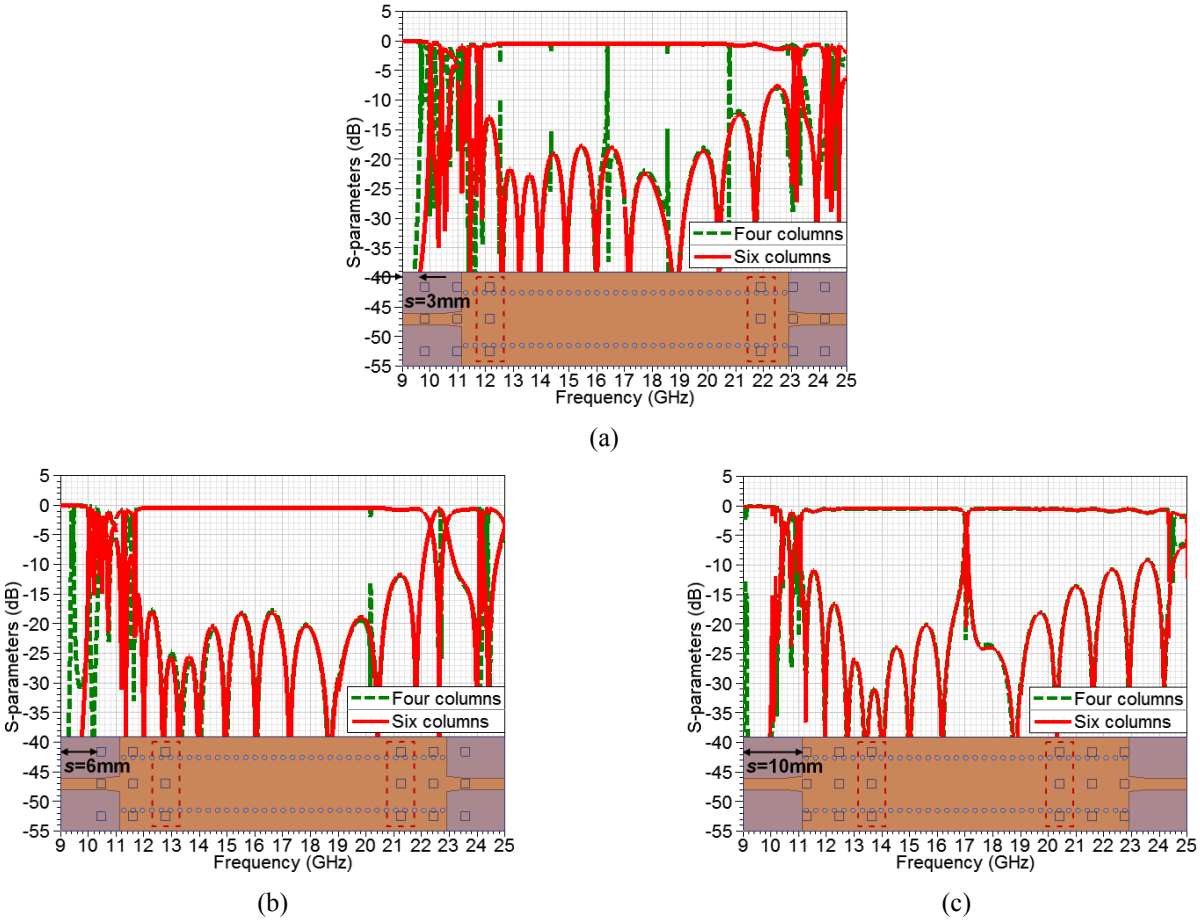
Figure 5-7 Simulated S-parameters of GW package using a lid of fourteen-column pins for an SIW with transitions to microstrip lines and SIW lengths of 55.71 and 30.11 mm. (a) Three-row pins. (b) Two-row pins.

However, as observed from Figure 5-1, a number of metal pins are directly over the SIW that are redundant actually due to the SIW self-enclosed feature. Therefore, such redundant pins are removed creating a simplified PMC shielding as presented in Figure 5-8. This revision makes the PMC shielding easier be fabricated and implemented. Besides, the design flexibility can be

improved by the introduced variable separation, *s*, between the pins and front/back metal walls. The following study will investigate how many columns of the pins at the input/output should be kept to guarantee the desired packaging performance and the required *s*.

Table 5-1 Dimensions of the circuit based on SIW and microstrip lines.

Symbol	D_{SIW}	P_{SIW}	W_{SIW}	L_{SIW}	W_{MS}	L_{MS}
(mm)	0.8	1.6	9	55.71	1.93	7.0
Symbol	W_{Trans}	L_{Trans}	W	L		
(mm)	2.6	3.0	16	75.71		



(a) (b) (c)

Figure 5-8 Simulated S-parameters of GW package using a lid of three-row and four-/six-column pins with a separation from the front/back wall. (a) 3 mm. (b) 6 mm. (c) 10 mm.

As indicated by the dashed green curves in Figures 5-8 (a) and (b), a lid with four-column pins is not sufficient to suppress the cavity resonances within the operating band from around 11

to 23 GHz, no matter if the input/output pins arrays just approach (s = 3 mm) or cross (s = 6 mm) the SIW borderline. These cavity modes are created in the pins-removed airspace over the SIW, due to the insufficient attenuation of the propagating wave. Thus, by adding one more column of the pins at the input and output, respectively, denoted by the dashed boxes in Figures 5-8, the resonances are completely suppressed with s = 6 mm as shown by the solid red curves in Figure 5-8 (b). However, Figure 5-8 (c) then indicates that if the separation, s, is too large (s = 10 mm), the resonance may occur in the airspace enclosed by the pins and front/back metal wall. Similar observations happen in Figure 5-9 for the lid of pins with four/six columns but two rows.

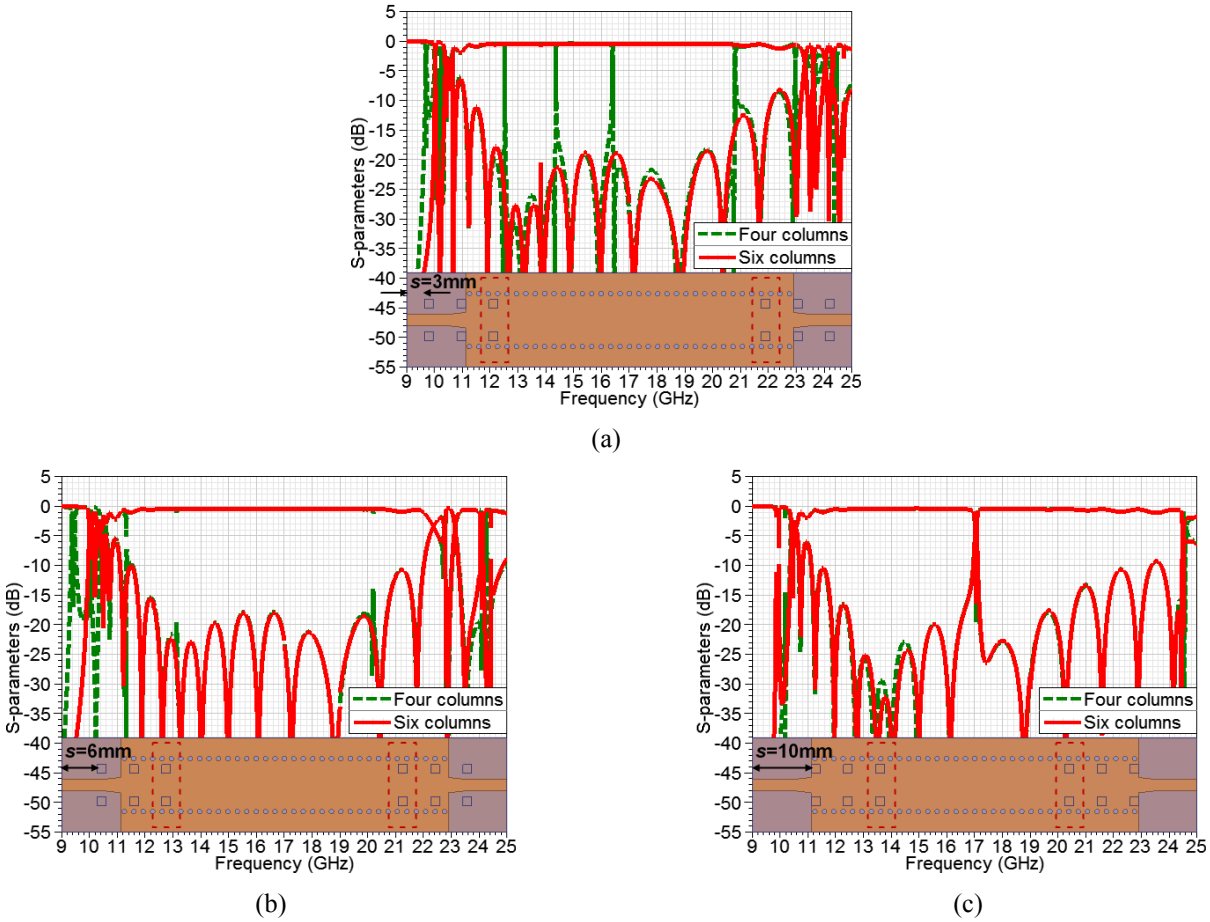


Figure 5-9 Simulated S-parameters of GW package using a lid of two-row and four-/six-column pins with a separation from the front/back wall. (a) 3 mm. (b) 6 mm. (c) 10 mm.

5.2.3 GW PMC Packaging for SIW-Based Filter

A 5-order Chebychev bandpass filter is built on the SIW-microstrip structure in Figure 5-1. This SIW-microstrip filter with GW PMC packaging will prevent the input-output coupling

and the interference from the environment. The filter has 0.1-dB ripple and 500-MHz bandwidth centered at 14.25 GHz. This center frequency allows the microstrip transition designed previously. The filter is illustrated in Figure 5-10 (a). Six additional plated vias in the SIW are to realize the filter function [83]. Their diameters are D_F = 1.546 mm. The distance between them are: L_0 = 5.837 mm, L_1 = 8.270 mm, L_2 = 9.136 mm, and L_3 = 9.222 mm. Two offsets off_1 = 1.935 mm and off_2 = 0.629 mm are used to control the filter's external quality factors and internal coupling coefficients, respectively. Except for these additional plated vias, the substrate and dimensions are kept the same as in Figure 5-1.

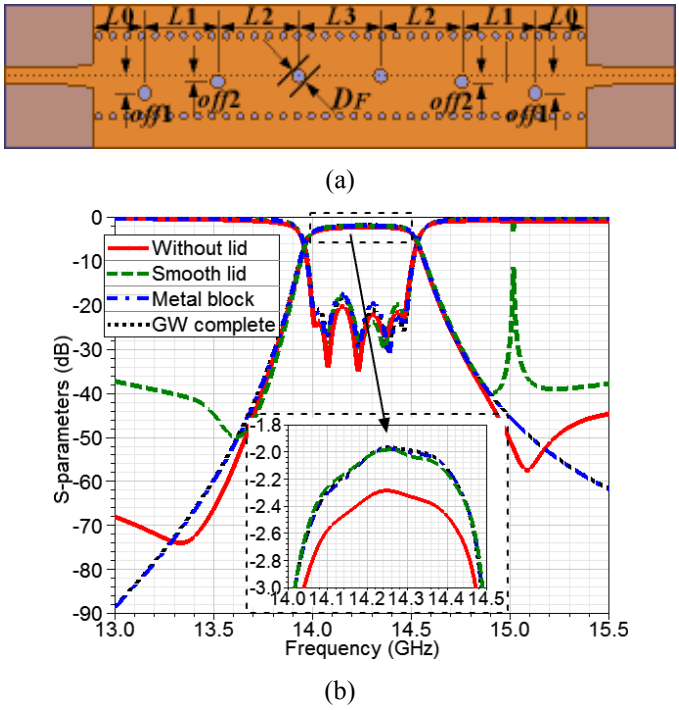
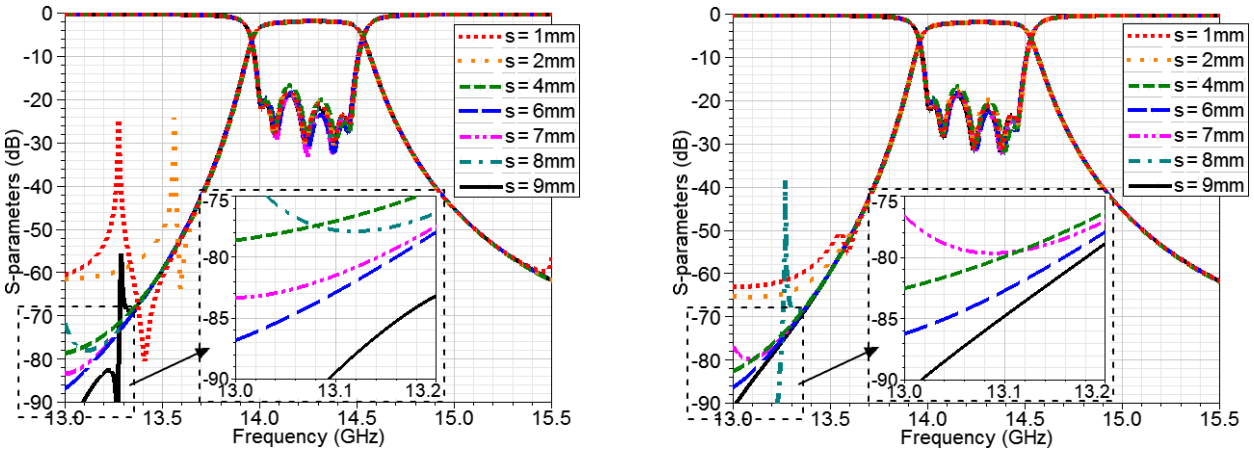


Figure 5-10 (a) Filter based on SIW and microstrip line. (b) Simulated results for the filter before and after using the three different lids indicated in the figure.

The simulated filter performance with different shielding lids is compared in Figure 5-10 (b). The complete GW packaging uses two-row and fourteen-column pins with 1.5 mm size and 5.5 mm period. Two conventional packaging methods are considered: a smooth metal lid and a modified smooth lid with a metal block exactly covering and touching the SIW top metal plate. It is found that the filter outband rejection becomes worse when shielded by the smooth metal lid, which results from the input and output coupling and the generated resonance. The best outband rejection is achieved by the other two methods. But, besides being cumbersome, the lid with the

metal block is also not suitable for some advanced SIW circuits that are not allowed to touch the top [80], [81]. The electrical contact is, however, not required in the GW PMC packaging, and it is valid even if the circuit containing two-layer PEC surfaces.

The simplified GW PMC packaging indicated in Figure 5-9 with two-row and six-column pins is also investigated for this designed filter. Figure 5-11 (a) shows that different separations, *s*, are corresponding to different outband rejection performance, and a separation larger than 3 mm is necessary to suppress the possible resonances. The best rejection performance is achieved for s = 4 mm. However, the rejection cannot always be enhanced for further larger separations. Instead, a resonance re-emerges for s = 9 mm, which is formed in the cavity enclosed by the metal pins and front/back wall as explained in Figure 5-9 (c). The situation could be better if the period of the pins increases from 5.5 to 6.0 mm as seen in Figure 5-11 (b), in which a separation of 2 mm is sufficient to suppress the possible resonances. The insignificant variations presented in the filter inband reflection coefficients are caused by the lid of pins, which imposes different influence on the characteristic impedance of the microstrip line due to the different separations.

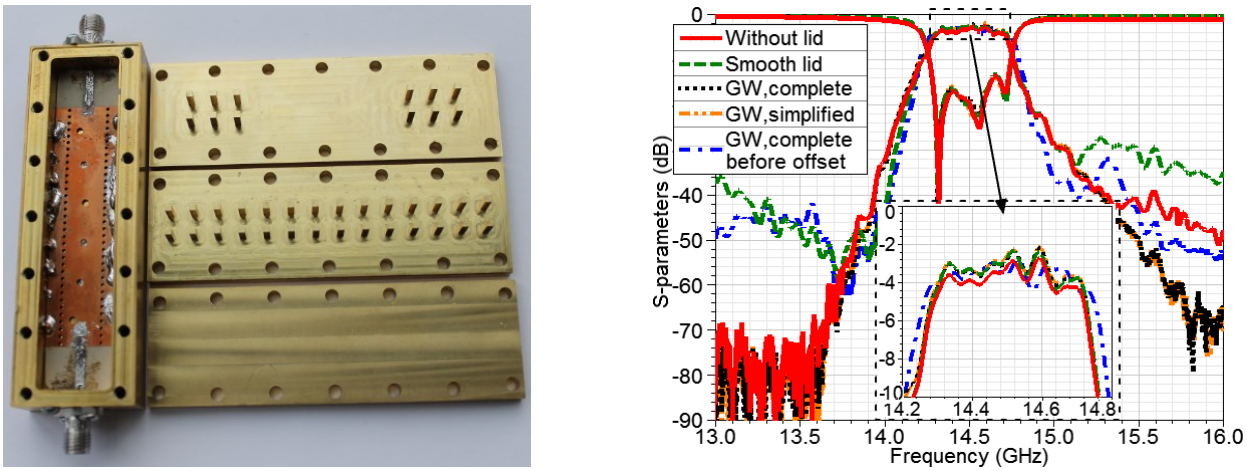


(a) (b)

Figure 5-11 Simulated S-parameters of GW package using a lid of two-row and six-column pins for the filter with separations from the front/back wall. (a) Pins of 1.5-mm size and 5.5-mm period. (b) Pins of 1.5-mm size and 6.0-mm period.

The designed SIW filter is fabricated and fitted in a brass box as illustrated in Figure 5-12 (a) with the fabricated packaging lids. The fabricated PMC shielding lids contain the original one of using two-row and fourteen-column pins of 1.5-mm size and 5.5-mm period, and its simplified counterpart of six-column pins and a separation of 6 mm. Because of long and thin metal pins,

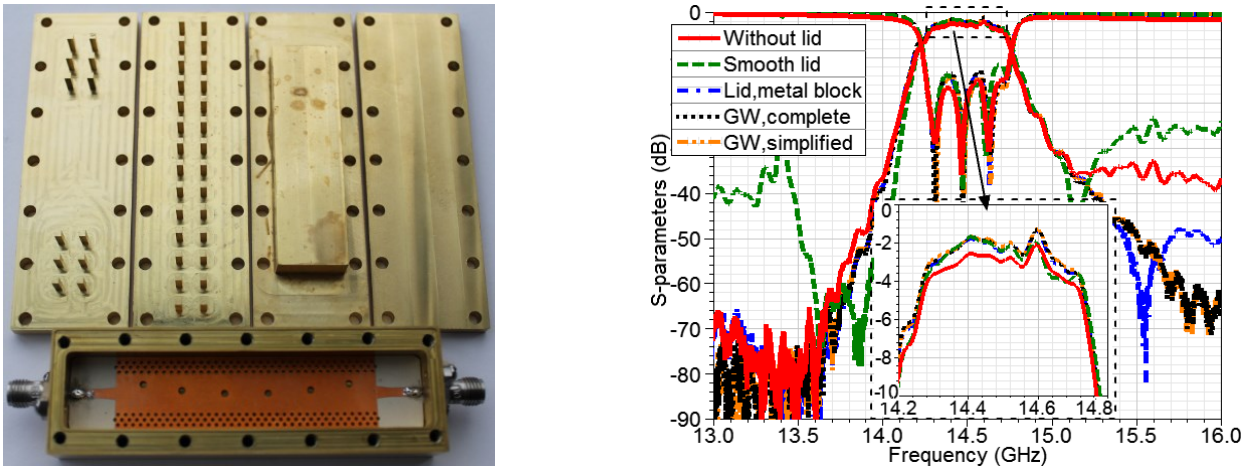
the lid thickness is set as 3.81 mm, large enough to avoid its warping. The lids can be screwed to the box, and the complete device was measured with a VNA. The measured results are shown in Figure 5-12 (b). First of all, we must pay special attention to the air gap between the PCB circuit and the box side walls due to the fabrication tolerances. As indicated by the dotted-dashed blue curves in Figure 5-12 (b), this side air gap badly degrades the PMC packaging performance, compared to its corresponding simulated performance in Figure 5-10 (b). This can be explained as follows. Far away from the plated vias, this side air gap makes the electric conductors on both sides of the substrate resemble a conventional dielectric-filled parallel plate waveguide. This waveguide supports the coupling between the input and output. As a result, even though the coupling through the airspace above the circuit is prevented by the lid of pins, it still happens in the substrate and lowers the filter outband rejection. Note that this problem is dedicated to such a hybrid circuit containing two-layer PEC surfaces and using the GW PMC packaging. This issue of the side air gap can be resolved by soldering box side walls and SIW top metal plate together to destroy the two-conductor structure, as shown in Figure 5-12 (a). The number of the additional soldering points should be enough to ensure their electrical contacts. After this offset, the filter is measured again with the three fabricated lids. As shown by the dotted-dotted black and dotted-dotted-dashed yellow curves in Figure 5-12, the outband rejection has been improved with the PMC packaging, and the same performance is obtained with the complete and simplified forms.



(a) (b)

Figure 5-12 (a) Fabricated filter with three different packaging lids: smooth lid, complete GW PMC lid, and simplified GW PMC lid. (b) Measured results before and after shielding by the three lids.

The soldering, however, may not be feasible when more rows of metal pins are required, as the case with three-row pins in the previous description. This is due to the really small air gap between the pins and substrate. Figure 5-13 (a) presents another solution to the side air gap by implementing two more rows of the plated vias on each ground side of the SIW. The principle is to reduce the area of the SIW base and top metal plates that may form a parallel plate waveguide. Such additional vias have the same diameter and period as the ones used to construct the SIW. Besides, by their zigzag arrangement, the SIW side energy leakage between the adjacent vias can be prevented further thus reducing the possible insertion loss. The validity of this solution is verified by the measured results in Figure 5-13 (b), as presented by the dotted-dotted black and dotted-dotted-dashed yellow curves. Considering inband insertion loss, about 1-dB improvement is achieved with the four different lids due to the suppression of the radiation losses of microstrip lines. This improvement can be more evident when the filter operates at a higher frequency. The observed degraded measured filter inband return loss in Figure 5-12 (b) and Figure 5-13 (b) is possible due to the impedance mismatch between the SubMiniature version A (SMA) connectors and the microstrip feed lines.



(a) (b)

Figure 5-13 (a) Modified fabricated filter with four different packaging lids: smooth lid, modified smooth lid, complete GW PMC lid, and simplified GW PMC lid. (b) Measured results before and after shielding by the four lids.

5.3 Packaging for Ground with Plated Vias

As explained in Chapter 1, ground vias are required in the circuit to stop energy coupling via the substrate leaky waves [84]-[86]. However, it creates a non-smooth PEC/ground plane for

the upper PMC shielding, which is different from the above case of two-layer PEC surfaces. One typical example is the grounded coplanar waveguide (GCPW), in which a significant number of grounded vias are implemented along with the slots to reduce the radiation losses and suppress the parasitic parallel-plate modes. Hence, the validity and characteristics of the PMC packaging technology for such an irregular ground surface containing plated vias should be verified and investigated further.

5.3.1 Unit Cell of Packaging Containing Via Hole

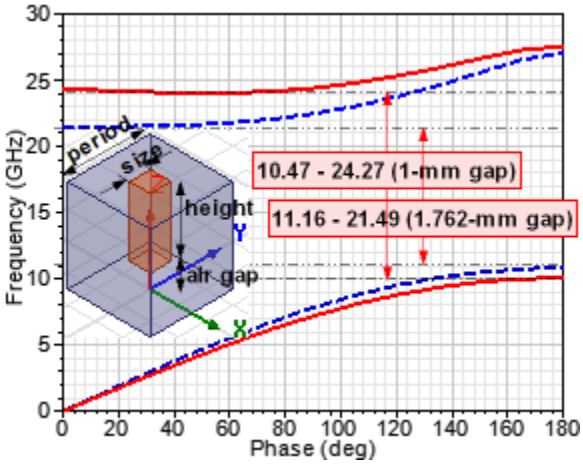
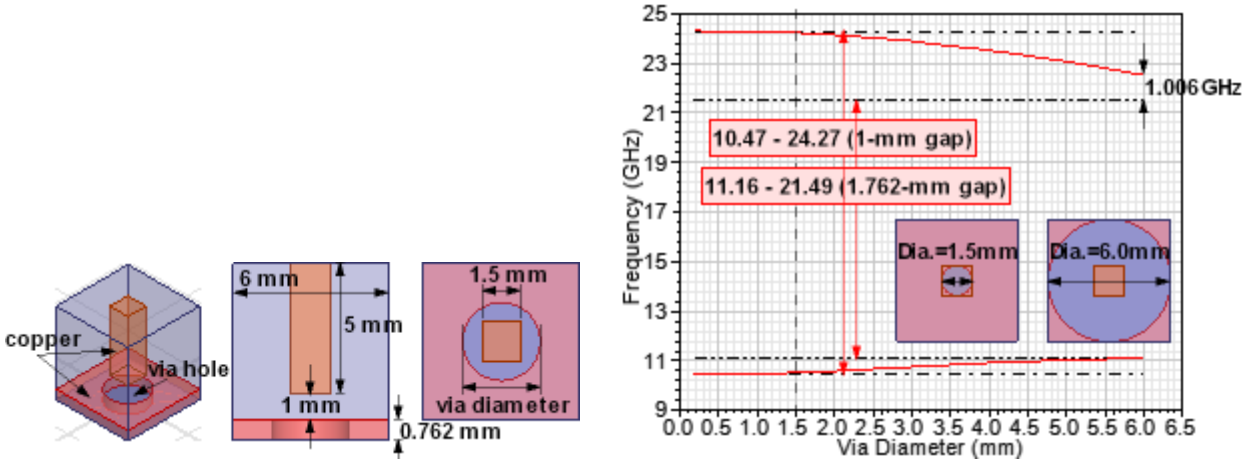


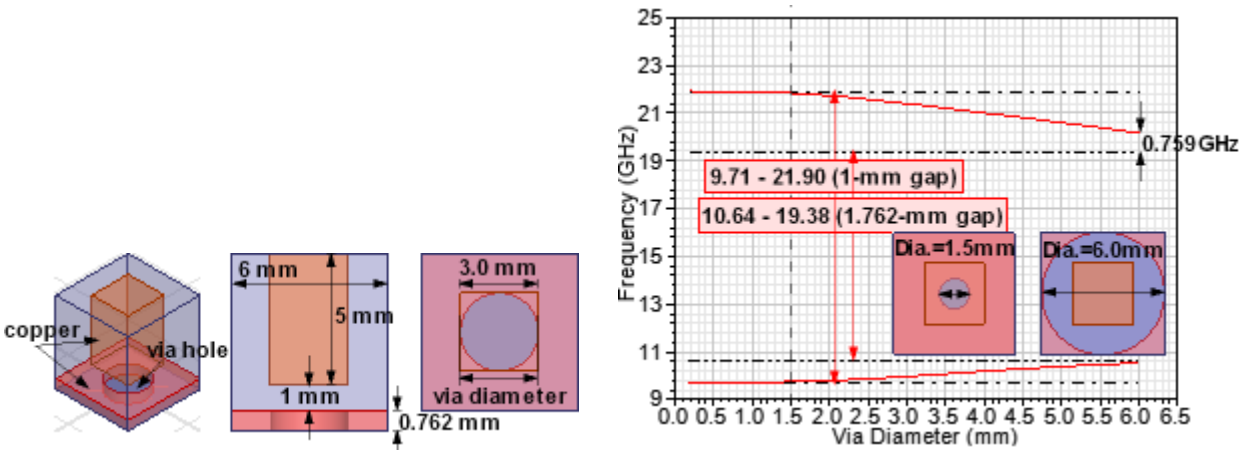
Figure 5-14 Dispersion diagram for a unit cell of periodic pins of 5 mm height as well as 1.5 mm size and 6 mm period but with two different heights of the air gap between the pin and the base: 1.0 and 1.762 mm.



(a) (b)

Figure 5-15 One unit cell containing one via hole and one pin of 1.5 mm size. (a) Overview, side view, and top view of the whole structure. (b) Change in the lower and higher cutoff frequencies with the via diameter.

A unit cell of the GW PMC packaging can be found in Figure 5-14, considering two air gap heights of 1.0 and 1.762 mm which generate two different band gaps. To represent the plated via in such a unit cell, a copper block is laid on the cell base with a hole directly under the metal pin, as illustrated in Figure 5-15 (a). The size and thickness of the square copper block are 6.0 and 0.762 mm, respectively. The air gap between the bottom of the pin and the upper surface of the copper block is 1.0 mm. The simulated lower and upper cutoff frequencies with the enlarged via diameter is presented in Figure 5-15 (b), which shows that the two cutoff frequencies move toward the performance of 1.762 mm air gap. It is also found that the distinct variation in both the lower and upper cutoff frequencies occurs at the via diameter of 1.5 mm. However, different from the lower counterpart, the upper cutoff frequency does not fall to the level of the 1.762 mm air gap (indicated by the dotted-dotted-dashed black line) for the maximum via diameter of 6.0 mm. The difference between them is 1.006 GHz. It is believed that this difference is due to the remaining part of the copper block around the via hole, which is still effective even when the via hole the pin facing is larger than the pin size. Similar observations can be found in Figure 5-16 when the pin size is increased to 3.0 mm. It shows that the distinct variation occurring in the lower and upper cutoff frequencies is still at the via diameter of 1.5 mm, independent of the pin size.



(a) (b)

Figure 5-16 One unit cell containing one via hole and one pin of 3 mm size. (a) Overview, side view, and top view of the whole structure. (b) Change of the lower and higher cutoff frequencies with the via diameter.

Another parameter taken into account is the substrate thickness, i.e., the height of the plated via. In the study, the substrate thickness is represented by the height of the copper block,

as illustrated in Figure 5-17 (a). As presented by the dotted-dotted blue curves in Figure 5-17 (b), even if the height and diameter of the via hole are increased to 2.286 and 6.0 mm, respectively, the higher cutoff frequency is far away from the one for an air gap of 3.286 mm height indicated by the dotted-dotted-dashed blue line. The difference between them is up to 3.489 GHz. Instead, it is much closer to the higher cutoff frequency for an air gap of 1.762 mm shown by the dotted-dotted-dashed red line. This implies that the effect of the via hole is not significantly enhanced by the depth of the hole.

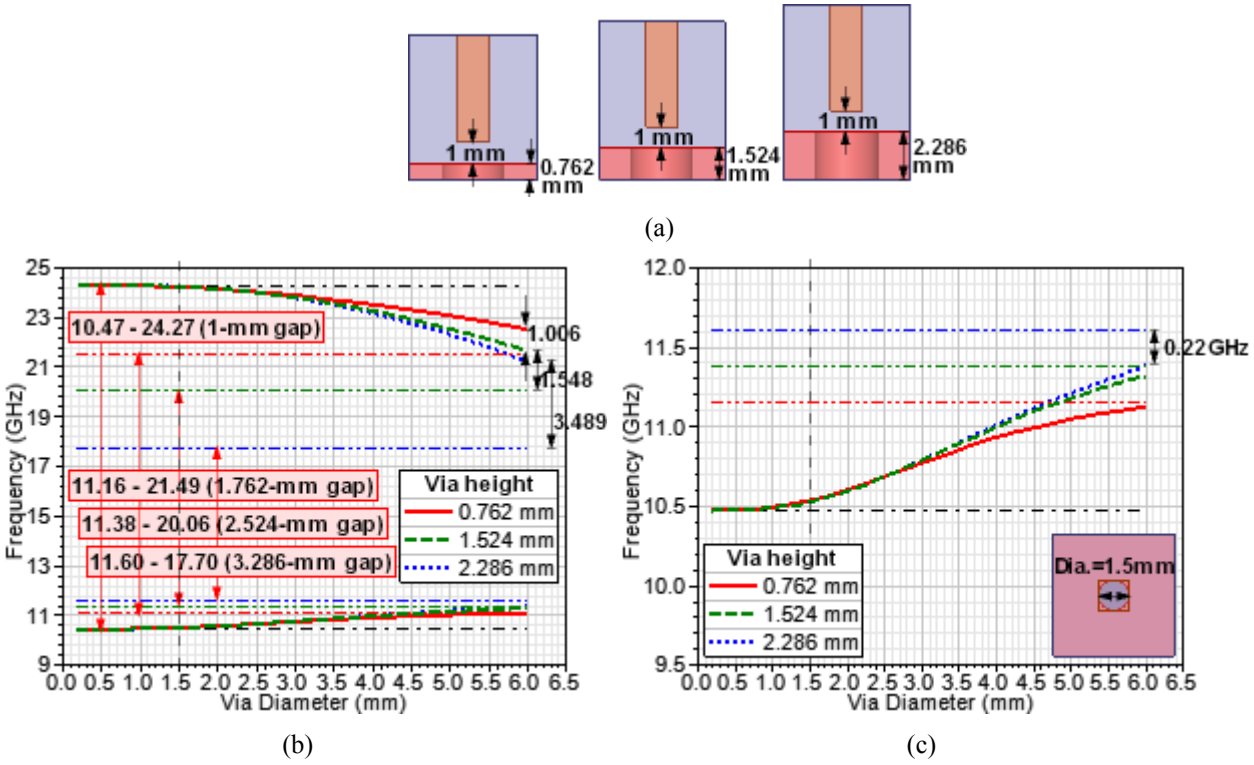
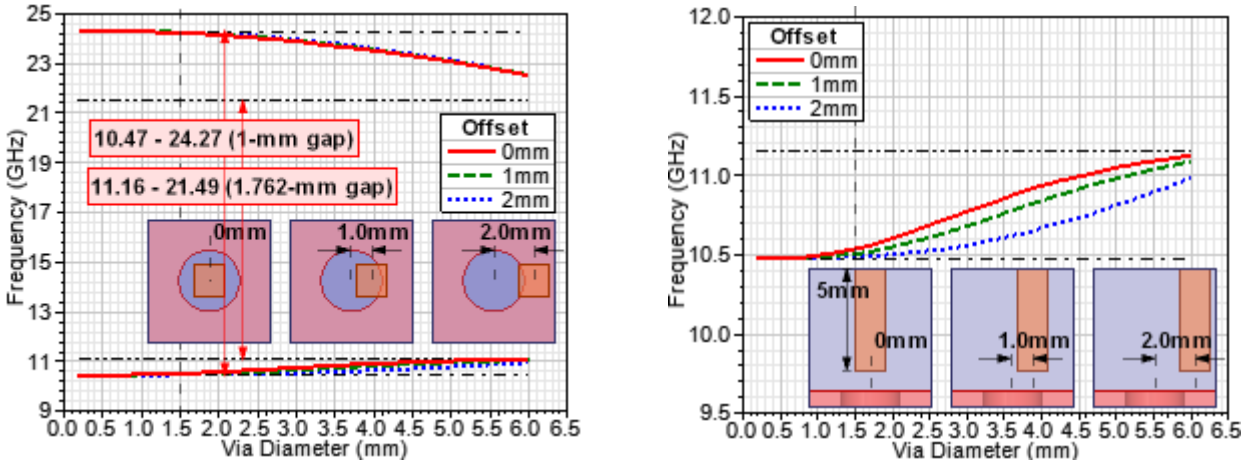


Figure 5-17 One unit cell containing one via hole and one pin of 1.5 mm size, with three different via heights. (a) Side view of the structures. (b) Change in the lower and higher cutoff frequencies with the via diameter. (c) Change in the lower cutoff frequencies with the via diameter.

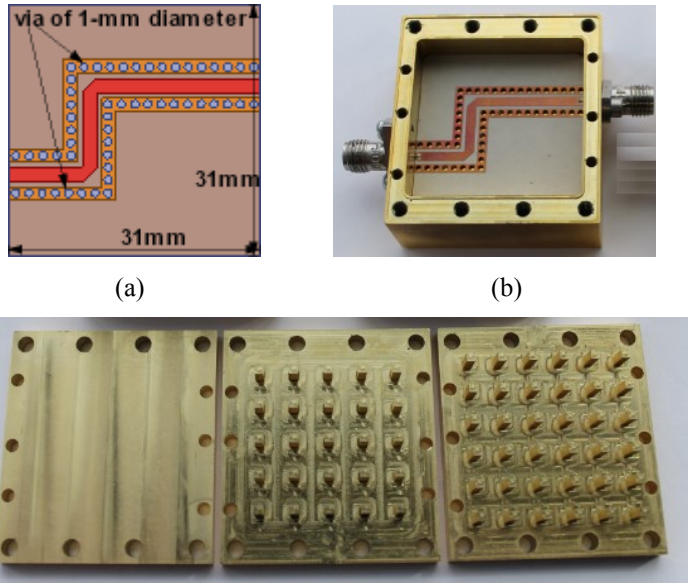
As in practice the via hole is mostly not aligned with the metal pin, the relative position between the pin and the via hole is investigated additionally. However, as presented in Figure 5-18, the variations due to the different offset positions are insignificant in the lower and higher cutoff frequencies. In general, all the above investigations reveal the effect of the upper ground plane on the stopband characteristics, even if the via hole under the metal pin is larger than the pin size. The pin size as well as the via diameter and height should be taken into account for the desired stopband when implementing the GW PMC packaging for the ground with plated vias.



(a) (b)

Figure 5-18 One unit cell containing one via hole of 0.762 mm height and one pin of 1.5 mm size and 5 mm length with three different offsets. (a) Lower and higher cutoff frequencies. (b) Change in its lower cutoff frequencies.

5.3.2 Experimental Verification for GW PMC Packaging for GCPW



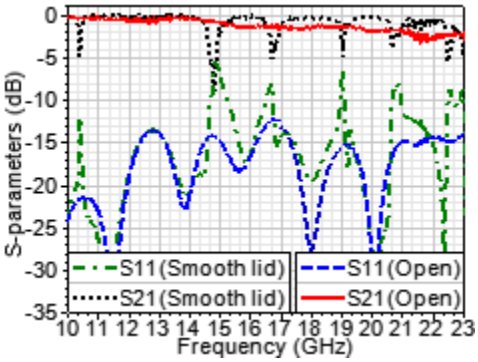
(a) (b)

(c)

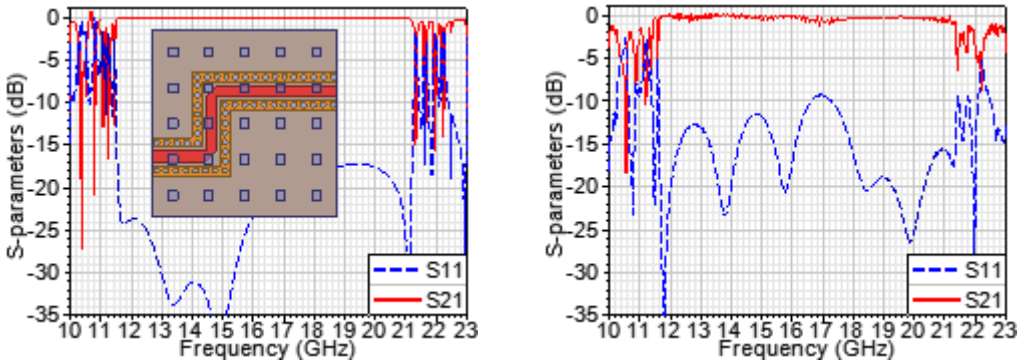
Figure 5-19 (a) Top view of a GCPW with two 90º bends. (b) Photo of fabricated GCPW. (c) Photo of fabricated packaging lids.

The signal line width and the ground gap of the fabricated GCPW for verifications are 1.766 and 0.668 mm, respectively, according to 50 Ω at 14.25 GHz. The diameter of the ground vias along the signal line is 1.0 mm. The spacing between the hole edge and copper edge is 0.254 mm, due to the process requirement. The used substrate is Rogers RT/Duroid 6002 with 0.762

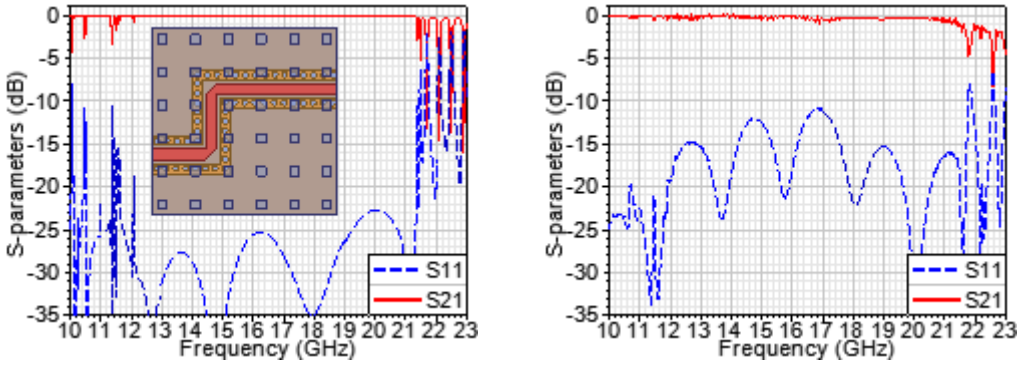
mm thickness and 18 um copper foil. Two PMC shielding lids are fabricated as shown in Figure 5-19 (c). One is comprised of five-row and five-column pins with 1.5 mm size and 6 mm period. The other is of six-row and six-column pins with 1.5 mm size and 5.5 mm period. The fabricated circuit is fitted in a brass box. The lids can be screwed to the box, and the complete device is measured with a VNA.



(a)



(b)



(c)

Figure 5-20 (a) Measured results of the GCPW before and after shielded by a smooth metal lid. (b) Simulated and measured results of the GCPW using the lid with five-row and five-column pins with 1.5 mm size and 6 mm period. (c) Simulated and measured results of the GCPW using the lid with six-row and six-column pins with 1.5 mm size and 5.5 mm period.

As presented in Figure 5-20 (a), although the smooth metal lid is able to prevent the radiation losses, it causes the severe cavity resonances. While the PMC shielding lid presents its effectiveness in suppressing the radiation losses and cavity resonances, no matter if the metal pins are directly over the plated vias (Figure 5-20 (c)) or they are offset (Figure 5-20 (b)). The degraded measured inband performance is possible due to the impedance mismatch caused by the SMA connector that was not considered in the simulations.

5.4 Conclusion

In this chapter, the GW-based PMC packaging for the irregular ground/PEC surface has been studied and verified, considering two-layer ground planes and with grounded vias. It helps extend the application of this packaging technology from the microstrip line circuits to the SIW combining with microstrip lines and the GCPW-based circuits. The effect of the SIW length, the metal pin size, the ground via diameter, the substrate thickness, and ε_r, and the relative position between the pins and SIW or via hole on the stopband characteristics have been investigated. This will help achieve the desired stopband. The experimental verifications include a 5th-order Chebyshev bandpass filter based on the SIW-microstrip line and a GCPW with two 90º bends. It has been proven that the GW-based PMC packaging is able to suppress both radiation losses and possible cavity resonances, compared with the open case or with a conventional smooth metal lid. In particular, an effective solution is proposed to deal with the issue of the side air gap existing in the SIW-based circuits when using this GW-based PMC packaging technology.

Chapter 6 Conclusion and Future Works

6.1 Conclusion

Different from conventional hollow waveguides, the metamaterial-based gap waveguides do not require any electrical contact between various layers and parts, which makes their assembly easier and suitable for higher frequencies. Different variants of the GW based on the PCB technology had been reported previously to offer a low-cost and low-profile application of this technology, such as the microstrip-ridge GW and inverted microstrip GW. However, these two developed gap waveguides come with their own drawbacks. The unstable air gap makes them very sensitive to the outside pressure or the environmental factors. The plated vias in the copper strip and the high-loss ENIG coating on the strip may cause substantial attenuation and a frequency shift. In addition, it is challenged to connect them to other planar lines or conventional hollow waveguides for the integration and measurements. In this thesis, two innovative GW variants have been proposed to deal with the above problems. The substrate integrated gap waveguide, i.e., SIGW, ensures a constant gap height with a gap-layer substrate. And the wave no longer interacts with the plated vias and ENIG coating with the constructed strip-ridge. The other is named as a packaged microstrip line, comprised of three-layer substrates, which further solves the alignment issue in the SIGW between the two strip-ridges. The packaged microstrip line is therefore much easier in fabrication and implementation at mm-wave bands. Several 60 GHz antenna arrays have been realized for the first time using the SIGW and the packaged microstrip line. In particular, a bandwidth-improvement method has been proposed for the SIGW -based antenna through fine-tuning the plated vias next to the strip feeding line. The achievable bandwidth can be larger than 21 GHz (35%) centered at 60 GHz. Another major part of this thesis is about the GW-based PMC packaging for the irregular ground/PEC plane, including two special cases of including two gap heights and the ground plane with plated via holes. This study makes this packaging technology no longer only limited to microstrip line circuits with a smooth ground plane, but also available for the SIW combining with microstrip lines and the GCPW-based circuits.

The introduction of the SIGW has been presented in Chapter 2. The structure dimensions (i.e., gap height, strip width, and via diameter) and the substrate property (i.e., ε_r and loss tan δ)

have been taken into account to study SIGW characteristic impedance and loss performance. The study also includes the bend discontinuities. A simple solution has been presented additionally to minimize the discontinuity effects and suppress the possible cavity resonance. This is of great help to realize future feeding networks for SIGW antenna arrays or other types of cost-effective SIGW passive components, in which many discontinuities are naturally present. Three fabricated prototypes have offered the experimental verification for the proposed SIGW and bend solution.

The antenna array realized on the SIGW has been presented for the first time in Chapter 3, with the proposed bandwidth-improvement method. By tuning the plated vias next to the strip feeding line, the impedance of the cavity under the slot is changed which is able to offer a very broadband impedance transition between the feeding line and the slot. The achievable bandwidth can be larger than 21 GHz (35%) centered at 60 GHz. The presented study on this bandwidth-enhancement method has also considered the gap- and via-layers of the SIGW with different substrates, which could be required for the desired bandwidth. A single-slot antenna and a 4-slot linear antenna array have been fabricated to offer the experimental verification with measured reflection coefficients, realized gain, and radiation patterns. Quite good agreement between the measured and simulated results have been achieved.

The packaged microstrip line has been introduced in Chapter 4. The study of stopband, dielectric/conduction losses, and characteristic impedance has offered a design guideline for the implementation of this transmission line. It has been further proven that no additional external transition, such as the tapered microstrip line, is required for the packaged microstrip line when integrating with the standard microstrip lines. Two fabricated prototypes with different top-layer PMC substrates have offered the required experimental verification. In addition, a 60 GHz slot antenna has been realized for the first time using this proposed packaged microstrip line.

The GW-based PMC packaging for the irregular ground/PEC plane has been presented in Chapter 5. The case of the PMC shielding containing two different gap heights has been studied. This case happens when the PMC shielding is used to package an SIW with microstrip lines. One gap height is from the PMC to the SIW top metal cover; the other is between the PMC and the base ground plane. A simplified PMC shielding lid of metal pins has been presented, which removes the pins directly over the self-enclosed SIW. The needed columns of the metal pins and

the relative positions of these remained pins and the SIW have been investigated, when considering this simplified PMC lid. Also, a bad effect of the side air gap between the circuit and the side metal walls to the PMC shielding performance has been found. The corresponding solution is implementing more ground vias on each ground side of the SIW. The experimental verification is with a fabricated 5-order Chebychev bandpass SIW filter. The case of the ground plane with plated via holes happens for a GCPW using the PMC shielding. The study of this case has considered the relative size of the solid rectangular pin and the cylinder plated via as well as their relative positions in the vertical. The effectiveness is verified by a fabricated GCPW with two 90º bends. The above investigations have helped expand the application range of this GW-based PMC packaging technology, which is no longer only limited to the microstrip line circuits with a smooth ground plane.

6.2 Future Works

Several other components, such as filters and diplexers, can be developed in the SIGW or packaged microstrip line technology. Benefitting from the low-cost fabrication and the absence of unwanted modes, these components will present compacted size and high performance at mm-wave bands for high data rate communications. Also, a general design equation can be developed to offer an easier or a more accurate implementation of the above two innovative planar lines. Besides, they can also be realized by the low temperature co-fired ceramic (LTCC) technology to avoid the additional circuit area occupied by the metal pads attached to the plated vias, which are required by the PCB technology for the via-hole plating process. This will also further makes the design more flexible with better accuracy in fabrication.

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