Validation and Enhancement of Two-Level Inverter Models for Very Low Time-Step Real-Time Applications

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ABSTRACT

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Ahmed Kotb Abdalla

Very low time-step real-time simulations are highly needed when simulating power converters to capture the fast transients caused by the switching devices of the converter. With very low time-steps, it is possible to represent fast transitions precisely and enhance simulation accuracy. FPGA-based solutions are mandatory to carry out very low time-step simulations. However, the complexity of FPGA programming makes such simulations undesirable for many users who might lack the required programming skills. A solver called eHS developed by OPAL RT establishes itself as a solution for this problem. It is designed to shadow the complexity of FPGA programming by automatically generating the code of the converter for the user.

FPGA-based low time-step real-time simulations, however, impose restrictions on the switch model that can be used to represent the converter. The switch model should be as simple as possible yet provides a good representation of a switch. It should inherit minimum computational efforts such that the requirements of low time-step simulations are satisfied. Several switch models offered in the literature are reviewed and discussed. Afterwards, a criterion to compare between these models is set and followed to select the most suitable one among the considered alternatives.

The main objective of this research work is to validate the converter models used in real-time simulations. This includes the converter, composed of the chosen switch model, programmed on the FPGA using the eHS solver. This entire model will be validated in offline and in real-time against a physical setup. More specifically, a new test plan to validate the converter model against an experimental setup is proposed and tested. The results of the converter simulated at a very low time-step on an FPGA through the eHS solver are compared to results from a real converter. Furthermore, the performance of the converter is tested in various operating conditions including unbalanced load and faulty situations. Based on the results of the offline and real-time validation, several recommendations on system improvement are proposed in the last chapter.

I dedicate this work to my parents and my sister, Sarah…

ACKNOWLEDGEMENT

In the name of God Almighty, the Most Compassionate, the Most Merciful, all praises and thanks be to HIM. This is by the grace of my God.

Then, I would like to take this opportunity to express my gratitude to my advisor, Prof. Akshay Kumar Rathore, for giving me this chance to indulge in a collaborative project with the industry in the field of power electronics. He was always motivating me to move forward with the project, and he was always ready to answer me when I faced problems. I would also like to thank him for including me in the financial grant of the NSERC CRD project sponsored by OPAL RT.

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I would also like to express my deep thanks to my colleague Amit Kumar, who generously spared some of his own time to guide me in using the OPAL RT system. He put me on track at the beginning of the project, and he was always happy to clear my numerous doubts. Also, I would thank my friend Ahmed Assad for generously spending some of his free time in reading the thesis and suggesting content and grammatical modifications. I would like to thank my lab mates and my friends for standing beside me and supporting me in my program. Last but not least, I express my gratitude to OPAL RT and NSERC for their financial support.

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CPU	Central Processing Unit
DFT	Discrete Fourier Transform
FPGA	Field Programmable Gate Array
HIL	Hardware-in-Loop
LCA	Loss Compensation Algorithm
PMSM	Permanent Magnet Synchronous motor
PWM	Pulse Width Modulation
RCP	Rapid Control Prototyping
RMS	Root Mean Square
RTE	Real-Time Events
SIL	Software-in-Loop
SPS	SimPowerSystems
THD	Total Harmonic Distortion

1. INTRODUCTION TO REAL-TIME SIMULATION AND OPAL RT SYSTEM

1.1 Introduction to Real-Time Simulation

Real-time simulations are quite different from the well-known offline simulations in many aspects including execution time, constraints etc. In this Chapter, real-time simulations are discussed thoroughly addressing several points such as the constraints for a valid real-time simulation, the different modes of a real-time simulation and the available hardware to implement the real-time simulation. The application of real-time simulations in the field of power electronics will be the core of this thesis.

1.1.1 What is a Real-Time Simulation?

Software packages such as Matlab and Simulink are widely adopted to validate the performance of mathematical and theoretical models and modern designs of systems. Nevertheless, these packages run in non-real-time (or offline), which means that the computation time of the model can be much longer than the response time of the real system. This prevents the interface of external hardware, which restricts the use of these packages to only offline verification with no hardware involved in the process [1].

To be able to interface external hardware, the simulator must receive information from the external system and use it to compute the model outputs within the time-step of the simulation. In other words, the computation time of the model must be less than the simulation time-step. This is basically the definition of a real-time simulation. In simple words, the real-time simulator must produce the internal variables and outputs within the same length of time as its physical counterpart would, as illustrated in Figure 1.1 [2]. With this condition satisfied ($T_c < T_S$), a sound real-time simulation is achieved and the integration of external equipment with real-time simulators is possible. If the computations are not performed within the simulation time-step, the simulation is considered erroneous. In this case, one time-step is omitted and the simulator uses the following time-step to perform the next computation. This is referred to as an overrun.

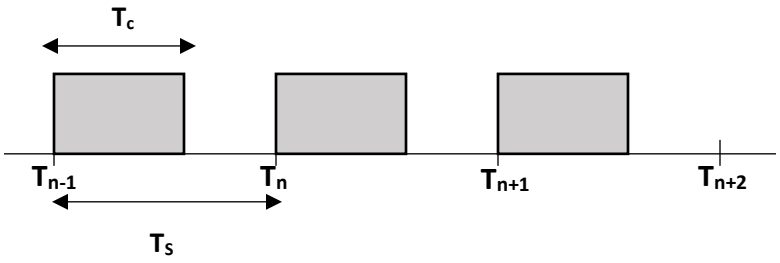

Figure 1.1 Accurate implementation of a real-time simulation

1.1.2 Modes of Real-Time Simulation

Real-time simulators are used in three different modes: Rapid Control Prototyping (RCP), Hardware-in-the-loop (HIL), and Software-in-the-loop (SIL) [2]. Rapid control prototyping is where a digital controller is implemented in the real-time simulator and connected to a physical plant. Conversely, in HIL applications, a physical controller is tested against a virtual plant modelled on the real-time simulator. Finally, SIL is the combination of RCP and HIL simulations, where both the controller and the plant are running on the simulator.

HIL simulations are typically employed when testing a physical controller or a protection scheme, but the actual plant is either unavailable or not permissible for testing. Therefore, a virtual plant, which emulates the performance of the real system, is implemented on the real-time simulator allowing for safe and early testing of the controller/protection device. Moreover, many possible scenarios that could happen in a real system can be tested quickly, securely and without physical modifications. In power systems, utilities prohibit testing with the actual system. Therefore, a virtual plant which captures all attributes of the real system is developed on a real-time simulator, and the protection device is then incorporated with the simulator. Faults can be applied safely to the virtual plant to verify the functionality of the protection device. Another application of HIL simulations is in motor drives. In some cases, the power converter and the motor are not available at the time when the physical controller is developed. Therefore, a virtual plant consisting of the power converter and the motor is developed on the real-time simulator to save time and perform early testing of the drive. Furthermore, extreme conditions that would, in practice, damage a real motor can be investigated.

The focus of this thesis is to investigate the performance of power converters in HIL simulations. Power converters are the heart of many applications including renewable energy,

energy storage, automotive applications such as electric cars and buses, and power generation applications. Therefore, it is of immense importance to make sure that the virtual model of the power converter is as accurate as possible as it is an essential building block of many systems.

1.2 CPU vs FPGA-Based HIL Simulations of Power Converters

HIL simulations of power converters can be performed on CPU cores or on an FPGA. Despite that CPUs can execute complex algorithms and support complex solvers, the nature of their structure limits the minimum allowable time-step to 5-10us [3]. In fact, CPU-based HIL simulators such as RT-Lab, dSpace and RTDS can hardly achieve a time-step less than 25us [4]. This constraint on the time-step can become critical in many applications involving very fast transients, such as high frequency converters.

There are plenty of benefits that can be realized by employing high frequency converters in various applications such as motor drives. High motor efficiency, smoother currents, low motor torque ripple, and smaller filter size are among the numerous advantages of high frequency PWM in motor drive applications [5]. In automotive industries, PWM frequencies are increased beyond 20 kHz to reduce weight, space, and noise. When such converters are HIL simulated, there are two main requirements that need to be fulfilled: low latency between controller and plant, and high PWM sampling resolution [6].

Latency is the time delay that arises between the controller sending its command and a change happening on the plant's output. The latency in modern control and protection systems is required to be maintained below few microseconds [6]. The high frequency PWM signals require a high sampling frequency so that they are precisely sampled. Jitter in the PWM signals can occur if the time-step is not sufficiently small. This can cause uncharacteristic harmonics in the output waveforms [2]. For instance, when a time-step of 10μs was used in [4] to simulate the PMSM drive, non-physical spikes were induced in the motor currents. These spikes were minimized when the time-step was reduced to 1 and 0.25μs. Therefore, the use of CPU-based HIL simulations with time-steps as low as 25μs will fail to meet the requirements of low latencies and high sampling resolutions.

Because of these deficiencies, FPGA-based HIL simulators manifest themselves as a solution to reducing latencies and increasing accuracy. FPGAs allow simulations to be carried out at time steps as low as 5-10ns due to their parallel-computing nature. In [7], the authors were able to accurately simulate different power converters with time-steps in the range of hundreds of nanoseconds. These include a three-level NPC inverter feeding an inductive load at 500ns, a three-phase diode rectifier with an LC filter at 170ns and a boost converter with a fixed resistive load at 170ns. In [8], the authors were able to simulate a three-level NPC inverter at 12.5ns allowing them to capture the switching transients of the IGBTs. The authors in [9] used a dual simulation time-step method to simulate a test network. The non-switching part of the network was simulated at 50µs on a traditional processor, while the switching converter was simulated at 5µs on an FPGA. The 50µs time-step is sufficient to accurately represent 50 or 60Hz power systems, but it is inadequate for the high switching converter. Therefore, a combination of both time-steps seems to be a potential solution for this problem.

Nevertheless, there are several drawbacks associated with FPGA-based simulations. First, the structure of the FPGA prevents the use of complex solvers. This means that the compilation time of an FPGA can be in hours. On the contrary, CPUs support complex solvers and therefore, the compilation time can be in minutes. Consequently, a combination of FPGA and CPU technologies is employed to enhance the performance of real-time simulators.

Programming an FPGA to simulate a power converter requires very high-level programming skills, which many power systems and control engineers might lack. This pushed the motive to develop ways to circumvent the programming stage of an FPGA. One solution has been proposed by OPAL RT Technologies, a company specialized in designing real-time simulators. OPAL RT developed the “eHS solver”, which made FPGA-based simulations of power converters readily available to engineers with even minimum programming skills.

1.3 The OPAL RT system

The OPAL RT system consists of two parts, the host computer and the real-time simulator. The host computer contains the software architecture in the form of RT-Lab. RT-Lab allows the user to import Simulink models, edit and then transform them to a real-time application via

automatic code generation. The real-time simulator forms the hardware architecture of the system, which is responsible of the real-time execution of the Simulink model. Communication between the host and the real-time simulator happens via TCP/IP protocols. Each of the software and hardware architectures will be discussed further in the following subsections.

1.3.1 Software Architecture: RT-Lab

RT-Lab is a user interface that facilitates working with the OPAL RT system to the users. It helps the user navigate smoothly through the process to run a real-time simulation. RT-Lab V11.0.8.13 was used in this project. The window view is shown in Figure 1.2.

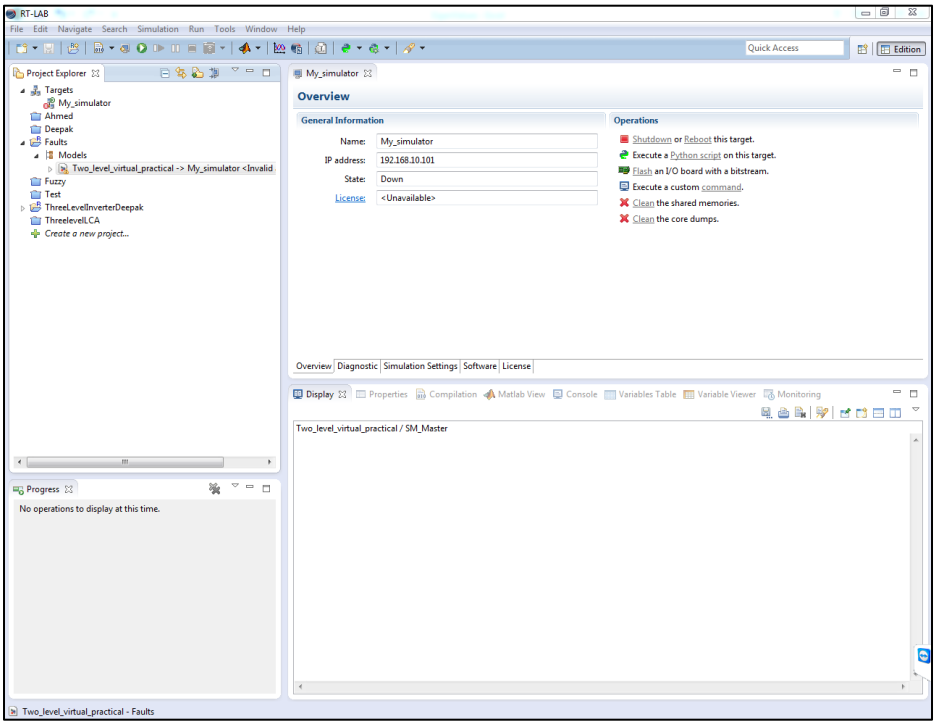

Figure 1.2 RT-Lab window view

There are various functions that RT-Lab offers to the users. On the left panel shown in Figure 1.3, the following icons allow the user to:

- **Targets:** Discover real-time simulators (targets) connected to the host computer.

- **Projects:** Create projects in which the user can import a ready Simulink model or build one from scratch.

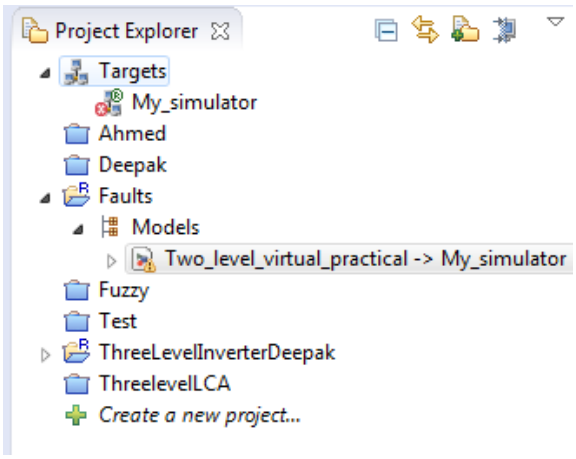

Figure 1.3 Left panel options

When a model is selected from a project, the panel on the right, shown in Figure 1.4, appears to the user. The following icons allow the user to:

- **Edit:** Modify the Simulink model through RT-Lab
- **Build:** Compile the model and generate the C-code using the Real-time Workshop toolbox in Matlab. The code is sent to the real-time simulator, which then creates real-time executable files and sends them back to the host computer.
- **Load:** The real-time executable files are loaded onto the real-time simulator. The simulator is now ready to carry out the simulation
- **Execute:** Starts the real-time simulation
- **Reset:** Terminates the real-time simulation

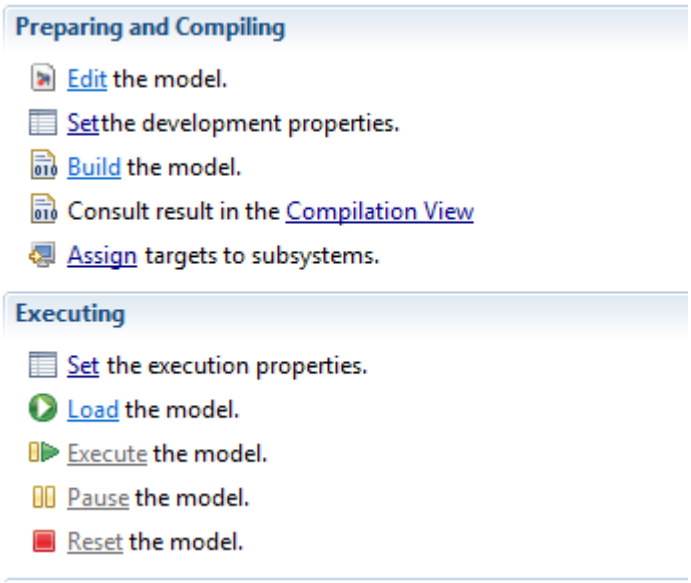

Figure 1.4 Right panel options

1.3.2 Hardware architecture: OP4510

OP4510 simulator, shown in Figure 1.5, was used in this project. The OP4510 simulator is equipped with the latest generation of Intel Xeon four-core processors and a powerful Xilinx Kintex 7 FPGA. Co-simulation between FPGA and CPU is also possible, thanks to a fast PCIexpress link exchanging data and signals between devices [10]. Simulation time-step of the FPGA can go to as low as 160ns making it possible to simulate high frequency converters accurately. OP4510 contains 16 Analog I/O channels and 32 Digital I/O. The architecture of the simulator is shown in Figure 1.6.

Figure 1.5 OP4510 Simulator

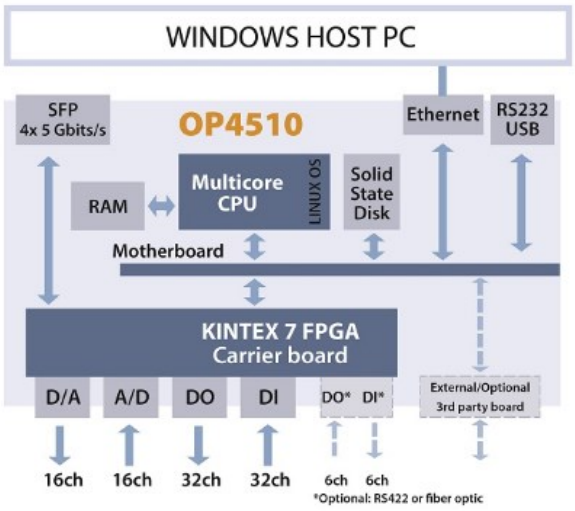

Figure 1.6 OP4510 System Architecture [13]

1.3.3 Transforming a Simulink Model to a Real-Time Simulation

Once the Simulink model has been validated in offline, the next step is to import the model file into RT-Lab. Once imported, any further modifications to the model should only happen through RT-Lab. Alternatively, the user can build the entire model from scratch in RT-Lab environment.

1.3.3.1 Grouping the model

Simulink models in RT-Lab must be grouped into subsystems. Each subsystem is implemented at a certain target in the OPAL RT system. The three types of subsystems are: Console, Master and Slave. In any model, one console and one master subsystem should exist. Addition of a slave subsystem is optional. The console subsystem runs in the host computer, while the master and slave subsystems run in the real-time simulator in assigned computation nodes. Figure 1.7 illustrates the master and console subsystems. The three subsystems are discussed below.

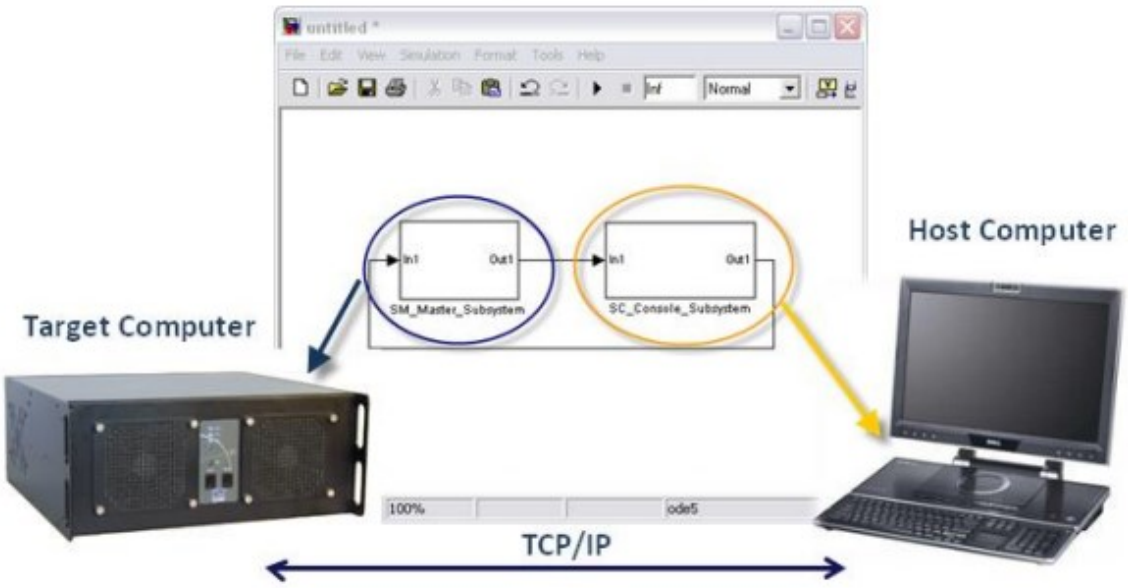

Figure 1.7 Master and console subsystem [14]

- **Console Subsystem:** The console is the only subsystem that can be altered during the real-time simulation. Typically, it contains the parameters that the user wishes to change on the fly such as reference speed, input voltage, switching frequency etc. Time-varying signals cannot be placed in the console. Any outputs or readings, such as a voltage waveform or the RMS value of a current, that need to be observed during the simulation are also displayed in the console. Figure 1.8 shows a console subsystem with variable parameters. It contains parameters that the user can modify on the fly including modulation index, modulating frequency, carrier frequency in addition to a manual switch to control the delivery of the gating signals.

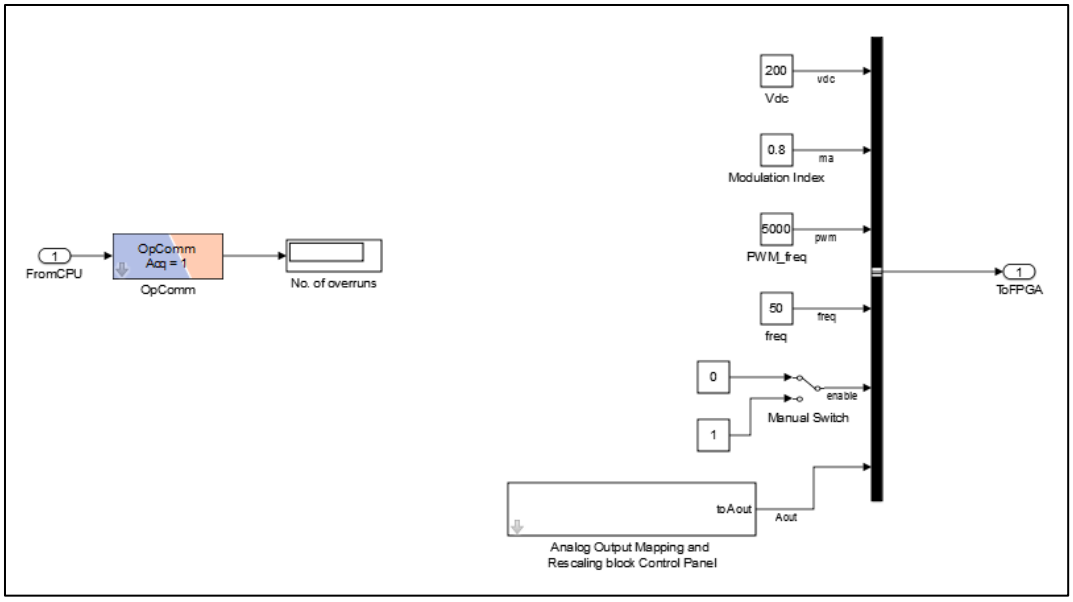

Figure 1.8 Console Subsystem: Includes variable parameters such as Input Voltage and Modulation index

- **Master Subsystem:** The master subsystem contains the computational blocks of the model, mathematical operations, comparative elements, varying signals, I/O blocks etc. However, none of these elements can be adjusted while the simulation is running. Therefore, the user has to know which elements are to be varied on the fly and place them in the console. For example, if the user wishes to change the modulating frequency on the fly, then the frequency must be entered in the console and the modulating signal shall be generated manually in the master. If the signal generator block is used, then it will not be possible to adjust the frequency during the simulation. The master subsystem is executed on a CPU core in the real-time simulator.

- **Slave Subsystem:** Slave subsystems are usually added when simulating large systems and when the user wishes to distribute the model rather than having it entirely in the master subsystem. Nevertheless, the real-time simulation can still be implemented with no slave subsystems.

1.3.3.2 Communication between Subsystems

In RT-Lab, signals cannot be exchanged between subsystems as in a normal Simulink model. When a signal is sent from one subsystem to the other, it should first pass through OpComm block, shown in Figure 1.9, before being able to process this signal in the subsystem. The communication between the console and master/slave is asynchronous while the communication between master and slave is synchronous. Therefore, signals sent through synchronous or asynchronous communication cannot share the same OpComm block. For example, if a master subsystem is to receive signals from the console and slave, there should be two distinct OpComm blocks: one for the asynchronous signal from the console, and one for the synchronous signal from the slave.

Figure 1.9 OpComm block

1.3.4 The eHS solver

OPAL RT developed a solver called eHS which allows the user to skip the programming step by using a block in their eFPGASIM Library. The user has only to build the circuit of the power converter in any circuit editor such as Simulink or PSIM and then introduce the eHS block to transfer the power converter onto the FPGA. This is illustrated in Figure 1.10.

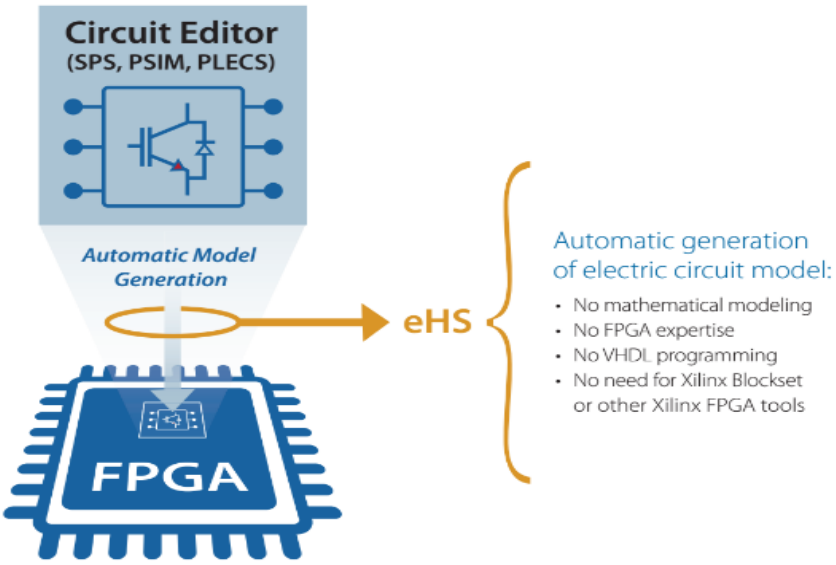

Figure 1.10 The eHS solver [15]

The eHS solver runs at the time-step of the FPGA, which varies depending on the size and complexity of the model being implemented on the FPGA. The circuit of the power converter is built in a different Simulink file. This file is never run, but is used as a reference to generate the equivalent converter on the FPGA.

Data exchange between the CPU and the FPGA happens at the time-step of the CPU as shown in Figure 1.11. This can be problematic if the gating signals are generated on the CPU for high frequency converters. The CPU time-step might not be short enough to accurately sample the gating signals. Therefore, in such cases, it is recommended to avoid using the conventional sine-triangle wave comparison blocks available from Simulink library. Instead, one might use blocks from RT-Events library as the RTE signals are of a higher time resolution which allows them to be sampled at eHS time-step.

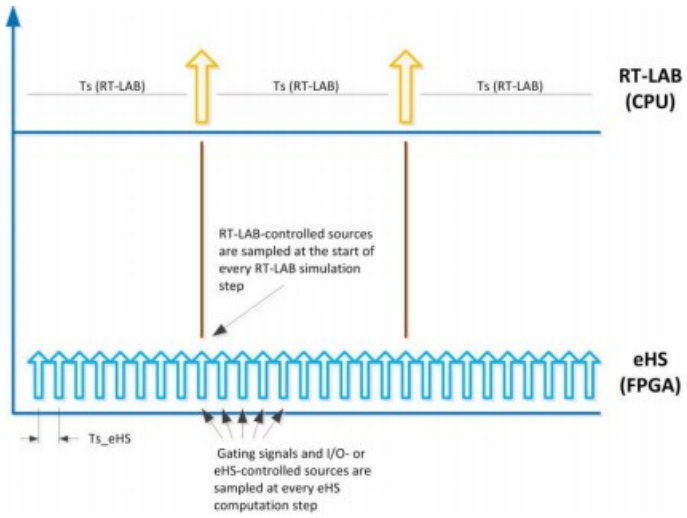

Figure 1.11 CPU time-step vs FPGA time-step [16]

1.3.5 The eHS Gen3 block

Figure 1.12 shows the eHS Gen3 block which is responsible for transferring the power converter from Simulink to the FPGA. “Inputs” port can accept a vector of voltages and currents specified by the user. Usually, these inputs come from the console so that the user has the freedom to alter the inputs on the fly. “GATES RTE” is the port where the gating signals of the switches are applied. The gating signals can be generated on the CPU model or it can be captured from an external source through digital input cards of the OP4510. “Outputs” port is from where the user can obtain the outputs of the converter. The outputs can be sent to the console for display during the simulation, or it can be written to a Matlab file for post-simulation analysis. The outputs from the converter are acquired at the CPU time-step. In the case of high frequency converters, it is thus recommended to output the data directly from the FPGA to the real world through analog output cards. The waveforms can then be displayed on an oscilloscope to enjoy a greater accuracy in the waveforms.

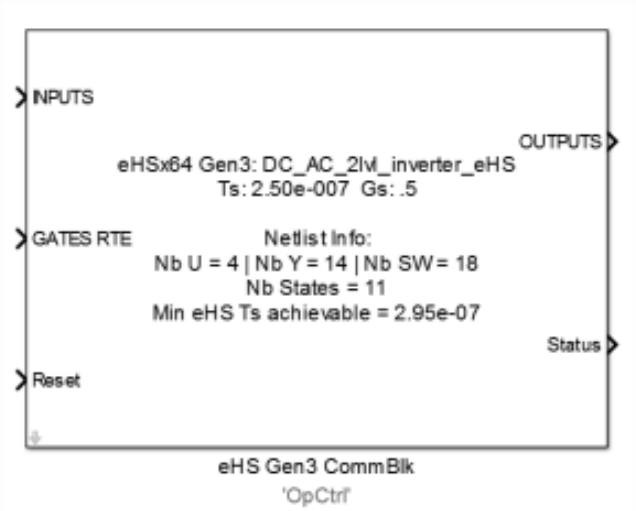

Figure 1.12 The eHS Gen3 Solver block [16]

Figure 1.13 shows the eHS Gen3 block parameters. In the circuit tab, the first field is the circuit filename. It was mentioned earlier that the power converter should be built on a separate Simulink file. The name of this file should be provided in this field. The next field is the sample time for eHS solver. This value is dictated by the Min eHS Ts achievable provided by the eHS block. It is provided on the outer view of the block as shown in Figure 1.12. The value Ts for the solver should be selected such that it is a factor of the CPU model time-step to eliminate errors that can arise due to poor synchronization between the CPU and FPGA time-steps. The last field is the switch conductance. This parameter will be discussed in more details in the next section.

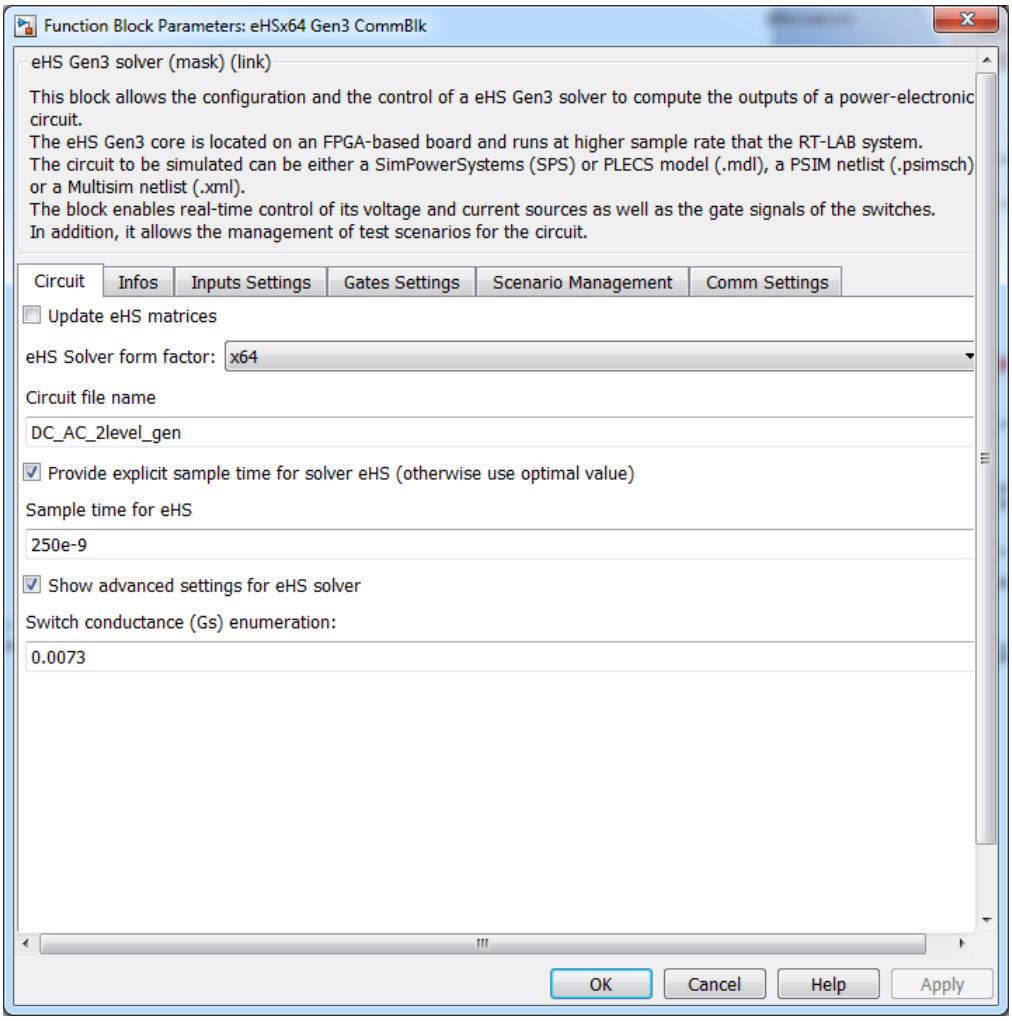

Figure 1.13 eHS Block parameters: Circuit Tab

Figure 1.14 shows that Gates Settings tab details. In this tab, the user specifies the source of gating signals. If the gating signals are coming from an external source, the "Independent setting for each element" option should be selected. Then, the user specifies that the signals are coming from Digital In. The switch polarity field allows the user to specify whether the switches will be active, high, or low.

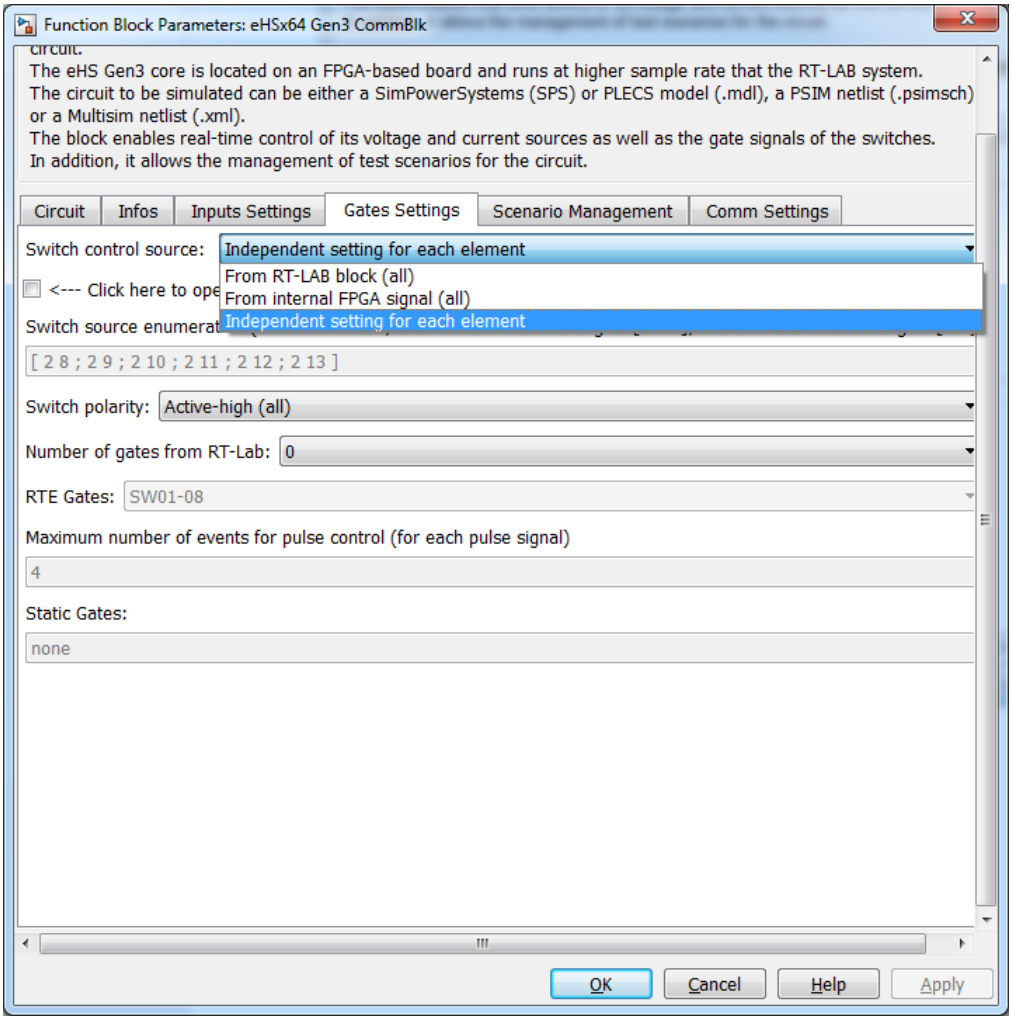

Figure 1.14 eHS Block Parameters: Gates Settings Tab

1.4 Switch Models for Real-Time Simulations

As previously stated, it must be ensured that the computation time of a system is less than the simulation time-step for the implementation of an accurate real-time simulation. In the case of power converters, this implies that a simplified switch model should be employed. Detailed switch models that characterize the switching transients impose computational burdens making them unsuitable for low time-step real-time applications. In fact, such detailed models are only required when investigating certain phenomena such as switching losses, arcing times and electromagnetic transients associated with switching-arc extinction [17]. In many other applications such as motor drives, a simple switch model is sufficient to study the performance of the system. This can be

justified since the switching transitions are generally much shorter than the switching period, and therefore, the errors induced by ignoring these details are negligible.

1.4.1 Switch Representations

The simplest approach is to represent a switch by a resistor. While a large value of resistance is used to represent the "off" state, a small value of resistance is used to represent the "on" state [18]. However, this approach mandates the update and inversion of the system's admittance matrix after every state change. The matrix inversion is a time-consuming operation, which adds extra computational efforts to the system. Such representation is, therefore, not suitable for very low time-step real-time applications.

Another approach is to use ideal switch models. An ideal switch is represented by an open circuit when "off" and a short circuit when "on". The differential equations describing each topology of the converter are derived. In [19], the Chebyshev series is used to compute the matrix exponential that results from the solution of the differential equations. There are several drawbacks associated with this model. Firstly, deriving the differential equations for each converter topology can be very challenging. Secondly, the number of switches in the converter is limited due to having to compute differential equations for 2^n possible configurations of the converter. Thirdly, pre-knowledge of how the converter functions is required to set conditions for network transitions. Despite the fact that this can be a very fast algorithm to simulate converters, there are many difficulties associated with it.

Thereafter, several efforts took place to suggest simple discrete circuit models for switches. In [20], the transmission-line modelling technique was used to represent switches. This model guaranteed a constant admittance matrix, but the errors introduced were not clearly identified. Pejovic and Maksimovic proposed in [21] a switch model that maintains a constant admittance matrix. The model is basically based on representing the "on" switch with a small inductance and the "off" switch with a small capacitance. The discrete-time equivalent of such a representation is a conductance (Gs) in parallel with a controlled current source. During a change in switch state, the value of Gs remains constant and the change is reflected in the value of the current source. Current sources are not accounted for in the admittance matrix which means that the admittance

matrix does not change when the switch turns from “on” to “off” and vice versa. This representation is known as the Fixed Admittance Matrix Nodal Method (FAMNM).

This switch representation fits the requirements of a low-step real-time simulation. First, it is a very simple representation which does not require an extensive computational effort to be solved. Second, this representation results in a fixed admittance matrix which means that the admittance matrix can be inverted a priori to the real-time simulation eliminating any complexities presented by matrix inversion. Additionally, prior knowledge of the converter operation is not required to run the simulation. This switch model will be referred to as the Pejovic switch from now on.

1.4.2 The Pejovic Switch Model

The equations for the conductance (Gs) and the parallel current source can be derived by applying numerical integration to the equations of an inductor and a capacitor. In [21], the authors picked the Backward Euler method. With this technique, the following equation for the switch conductance is obtained.

$$Gs = \frac{Cs}{Ts} = \frac{Ts}{Ls} \tag{1.1}$$

where Ls and Cs are the “on” inductance and “off” capacitance

The value of the parallel current source is given by:

$$j(n+1) = \begin{cases} -isw(n) & for\ the\ \text{"on"}\ state \\ GsVsw(n) & for\ the\ \text{"off"}\ state \end{cases}$$

Figure 1.15 summarizes the Pejovic approximation of a switch. It is clear that the value of the current source depends on the past values of switch current and voltage.

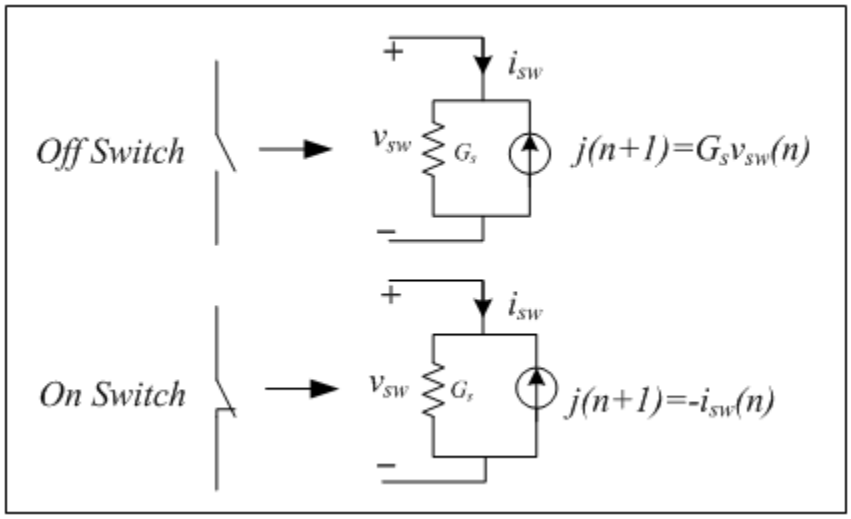

Figure 1.15 Pejovic Switch Approximation

The choice of other numerical integration methods to derive different switch models is possible. However, certain problems arise when some of these techniques are used. For example, Pejovic and Maksimovic derived another switch model using the trapezoidal algorithm. When the switch model was used in a buck converter, it resulted in oscillatory switch voltage. In fact, the switch model obtained by the trapezoidal algorithm is equivalent to the transmission-line switch model presented in [20].

In [22], the authors presented the trapezoidal with numerical stabilizer integration technique to derive a switch model. The model is very similar to the Pejovic switch except for additional terms containing the parameter "α" in the current source expression. In the ON model, the extra term is $-Gs\frac{1-\propto}{1+\propto}Vsw(n)$, and in the OFF model, it is $\frac{1-\propto}{1+\propto}Isw(n)$. In fact, when α=1, the model reduces to the Pejovic switch. When α=0, the model reduces to the model returned by the trapezoidal technique. This concludes that increasing alpha increases the damping effect of the resulting switch model. Increasing alpha beyond one will damp the numerical oscillations further, but it will come at the expense of increased errors. Therefore, the preferred value is α=1, which ends up at the Pejovic switch.

1.4.2.1 Drawbacks of the Pejovic Switch Model

Despite the simplicity of this switch model, selecting the optimal value of the conductance (Gs) that will result in accurate results is a challenge. It is desirable to keep the values of the on-state inductance and off-state capacitance as small as possible. However, this need is restricted by the relationship expressed below derived from equation (1.1). Reducing the value of one parasite comes at the cost of increasing the value of the other parasite. Therefore, a compromise needs to be made between the sizes of the two parasites.

$$Cs \propto \frac{1}{Ls} \tag{1.2}$$

When a very high value of Gs is selected, the off-state capacitance will be a large value($Gs \propto Cs$). This means that the capacitor will take longer time to get charged and block current flow. On the other hand, selecting a too low value of Gs will result in a very large on-state inductance($Gs \propto \frac{1}{Ls}$). This means that the inductor will take longer time to get charged and act as a short circuit. Both of these extreme conditions can affect the overall performance of the converter and result in considerable inaccuracies. Therefore, the value of Gs should be selected such that both switch parasites charge quickly and have negligible effect on the overall performance.

Another drawback of the Pejovic approximation is the switching losses. Losses occur every time the switch turns on/off. Let's consider a switch that has been open for a long time. The switch would be acting as a charged capacitor with a certain voltage across it. The energy stored in a capacitor is given by: $E = \frac{1}{2}CV^2$.

When this switch is turned on, it will be represented by an inductor. The initial current of the inductor is zero since no current was flowing prior to turning on the switch. In other words, the fully charged capacitor was replaced by an uncharged inductor when the switch was turned from off-to-on. In such case, the energy lost during turning on is equal to the energy stored in the capacitor. The same logic can be applied when turning off the switch. A fully charged inductor is replaced by an uncharged capacitor. Therefore, the total energy lost in one switching cycle is given by:

$$E_{total} = E_C + E_L = \frac{1}{2}CV^2 + \frac{1}{2}LI^2 \tag{1.3}$$

1.4.2.2 Optimum Value of Switch Conductance (Gs)

Equation (1.3) gives a good starting point to pick the right value of Gs. The value of Gs can be optimized to give the minimum losses during switching. Substituting equation (1.1) into equation (1.3) yields:

$$E_{total} = \frac{1}{2} TsGsV^2 + \frac{1}{2}\frac{Ts}{Gs} I^2 \tag{1.4}$$

In order to determine the value of Gs that will result in minimum losses, one needs to set the derivative of equation (1.4) to zero, and solve for Gs. In other words:

$$\frac{dE_{total}}{dGs} = 0 \tag{1.5}$$

$$\frac{dE_{total}}{dGs} = \frac{1}{2} TsV^2 - \frac{1}{2}\frac{Ts}{Gs^2} I^2 = 0 \tag{1.6}$$

$$\frac{1}{2} TsV^2 = \frac{1}{2}\frac{Ts}{Gs^2} I^2 \tag{1.7}$$

$$Gs^2V^2 = I^2 \tag{1.8}$$

$$Gs = \frac{I}{V} \tag{1.9}$$

"V" is the voltage seen across the switch. For example, the voltage seen across any switch in a two-level inverter is equal to the DC bus voltage. The value of "I" is the effective current flowing through a switch. In AC systems, the value of "I" is the RMS value of the load current. In DC systems, "I" is chosen to be the average current of the load. When Gs is selected according to equation (1.9), minimum energy loss is achieved and acceptable simulation results are realized.

1.5 Objectives and Related Work

The objectives of this study are shown below:

- To validate the performance of the eHS solver. In [7], [10]-[12], the real-time models of the power converters were always validated by comparing the results to those obtained with offline simulations in SPS. In this work, a new test procedure to validate eHS is proposed which involves comparing results with real inverters. Additionally, in the offline verification, results from PSIM and values obtained from mathematical expressions describing the waveforms of the power converter are included. The converter that will be considered is the two-level inverter feeding passive loads in open-loop.
- To identify cases where the results given by the eHS solver do not converge to the expected values. Then, it will be studied whether this case could be solved by re-tuning Gs. This will then pave the way to develop systematic methods to re-tune Gs in such cases of operation.
- To suggest a simple expression to select Gs that does not need any mathematical effort or knowledge of the converter outcomes. There are various proposed methods to select optimal Gs. The simplest one is the trial and error process, which can be very time-consuming. Others, such as the one described in this Chapter, depends on optimizing Gs by obtaining a value that minimizes the switching losses. Another algorithm is based on minimizing the error between eHS and SPS results, which is the method adopted by OPAL RT combined with the LCA algorithm. In [17], the proposed method depends on reducing the Euclidean distance between the eigenvalues of the admittance matrices of the power converter that result from using Pejovic and ideal switches.

1.6 Conclusion

In this Chapter, it was discussed that an FPGA-based HIL simulation of a power converter composed of Pejovic switches is the most suitable way to meet the requirements of a valid implementation of a power converter. The difficulties associated with programming a power converter on an FPGA are overcome by utilizing the eHS solver. In the next Chapter, the soundness of the eHS solver will be investigated through offline simulations.

2. OFFLINE VERIFICATION OF TWO-LEVEL INVERTERS WITH PEJOVIC SWITCH

2.1 Introduction

In this Chapter, the switch model used in low time-step real-time applications with the value of Gs selected according to equation (1.9), which was derived in Chapter 1, is examined. Real-time simulation will be avoided at this stage and the model will only be tested offline. This is to guarantee that there are no external factors affecting the accuracy of the simulation and the outputs are a mere result of the Pejovic switch approximation. The study is a comparison between eHS offline, which is a block from OPAL RT that simulates power converters according to the Pejovic approximation, and the conventional converters from SimPowerSystems (SPS). The RMS values of eHS must be within 2% difference from SPS, otherwise, the results are considered inaccurate.

2.2 Model for Offline Verification

Figure 2.1 depicts the entire model of the test circuit. The inverters from SPS and eHS are run simultaneously in the same model to assure a fair comparison. The model consists of three subsystems, namely PWM_Generation, SPScircuit, and eHS offline simulation block. SPScircuit and eHS offline block receive exactly the same gating signals, which are generated in the PWM_Generation subsystem. Each subsystem is discussed in more details next.

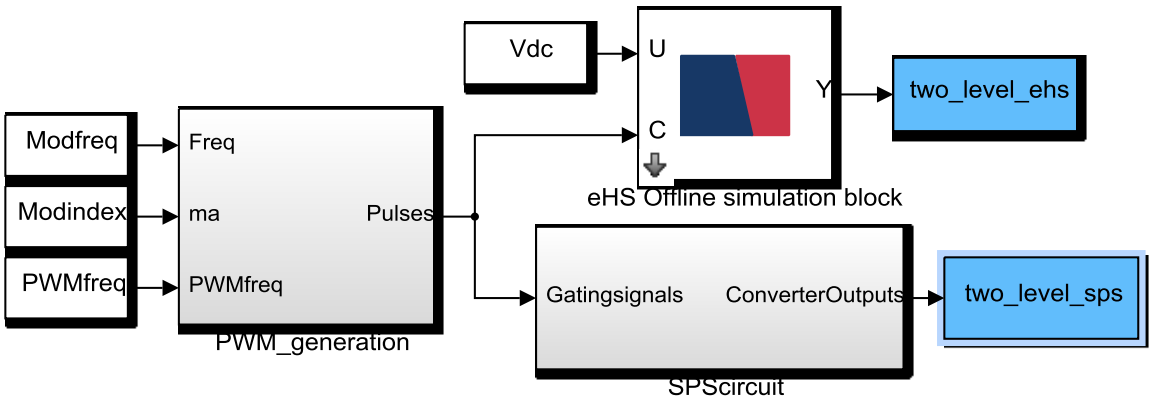

Figure 2.1 Offline verification model

2.2.1 PWM_Generation

Figure 2.2 shows the PWM_Generation subsystem. The block diagram can be divided into four stages as shown in the figure: Modulating Signal Generation, Sizing, Gating Signal Generation, and Regrouping.

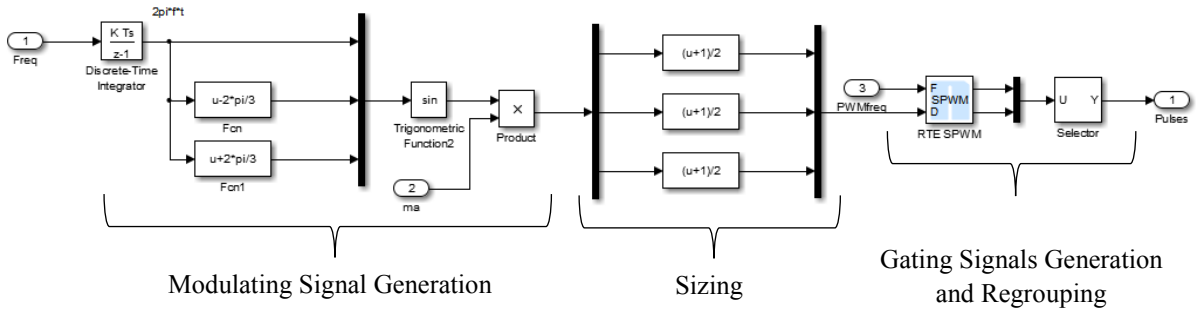

Figure 2.2 PWM generation subsystem

2.2.1.1 Modulating Signal Generation

In this stage, the three sine waves that are compared against the carrier wave are generated. The modulating frequency, provided by the user, is integrated with respect to time to generate the ωt term. The angle is shifted by 120 and 240 degrees to generate the angles of the other two modulating signals. The three angles are fed to a sine block to produce three continuous sine waves phase shifted by 120 degrees. The modulating signals are multiplied by the modulation index to set their amplitudes.

2.2.1.2 Sizing

The RTE SPWM block from OPAL RT generates the gating signals by comparing the modulating signals with a carrier wave running between 0 and 1. Therefore, the sine waves have to be shifted up by a value of unity and then divided by two so that it is in the same range of the carrier wave.

2.2.1.3 Gating Signals Generation and Regrouping

The RTE SPWM block has the option of generating the gating signals and their complements besides allowing the user to specify the desired dead time. The gating signals are delivered as two vectors where the first vector contains the result of the comparison of the sine waves with the carrier wave, and the second vector contains the complement of the first one. Then,

a selector is added to arrange the gating signals such that they comply with the switch arrangement in the inverter.

2.2.2 SPScircuit

Figure 2.3 illustrates the SPScircuit subsystem. This subsystem contains the circuit of the two-level inverter to be simulated by the conventional method. The outputs of this inverter will serve as the reference platform to which the eHS offline results are compared. The vector of gating signals from the PWM_Generation block is demuxed and each switch is provided with the relevant gating signal. The outputs of the inverter are stored in a matlab file for post-simulation analysis.

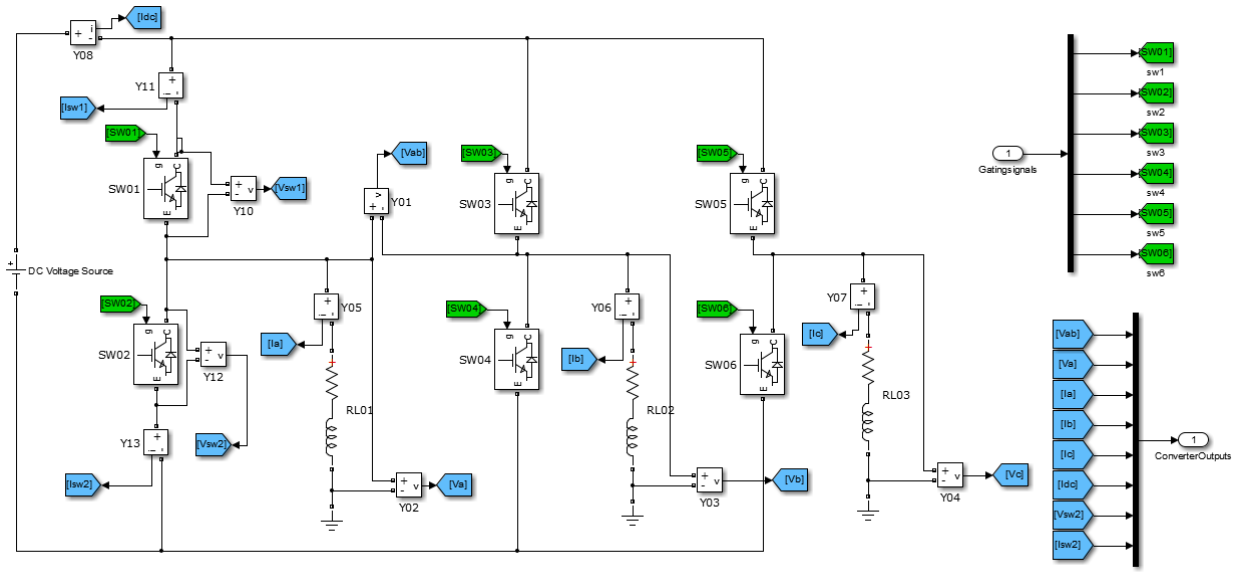

Figure 2.3 SPScircuit subsystem

2.2.3 eHS Offline Simulation Block

Figure 2.4 shows the eHS offline simulation block. This block allows the user to simulate the converter with the eHS solver used in FPGA-based simulations and with the same time-step but in an offline environment. This block is very handy since it gives an initial indication of the performance of the converter before engaging in a real-time simulation. If the eHS offline block yields acceptable results and still problems arise in the real-time simulation, the user shall know that the problem is not related to the eHS solver nor the Pejovic switch.

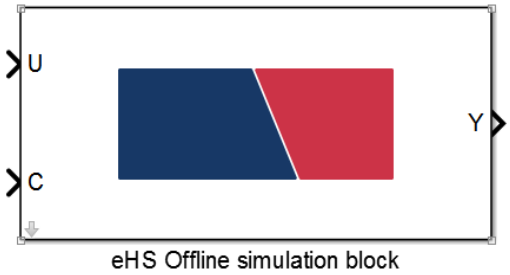

Figure 2.4 eHS offline simulation block

2.3 Loss Compensation Algorithm (LCA)

It was explained in the Chapter 1 that the Pejovic switch introduces switching losses, and these switching losses will be minimized by selecting Gs value according to equation (1.9). OPAL RT has developed the Loss Compensation Algorithm (LCA) aiming to eliminate even the minimum of these losses. In this work, two inverters from eHS are simulated: one with LCA disabled, and one with LCA activated. The impact of LCA on the inverter efficiency and its outputs is investigated. Thereon, the inverter without LCA is labeled as eHS, and the other one is named eHS LCA.

2.4 Test Conditions

Table 2-1 shows the test parameters used to validate the performance of the eHS inverters. Three sets of load are considered:

- R=25Ω, L=32mH (P.F. = 0.85)
- R=3Ω, L=500µH (P.F. = 0.97)
- R=100Ω (unity power factor)

Table 2-1 Test parameters

Parameter	Value
DC Bus Voltage	200V
Modulation Index	0.8
Modulating Frequency	50Hz
PWM Frequency	5kHz
On-state Resistance	1mΩ
Dead time	4µs
Time Step	250ns

2.5 Test Results

In the following subsections, the optimal value of Gs is given with each load condition. Waveforms and RMS values from SPS, eHS and eHS LCA are presented in each case, and a comparison is drawn between the results.

2.5.1 First Case: R=25Ω, L=32mH, Gs=0.00986

Figure 2.5 shows the line voltages from each inverter. The line voltages from SPS and eHS LCA are very similar, but there is a significant difference in the eHS line voltage. Therefore, there is a need to look at the spectral analysis of the line voltage to have a sounder evaluation of the waveform. Figure 2.6 shows the spectral analysis of the line voltages from SPS and eHS superimposed.

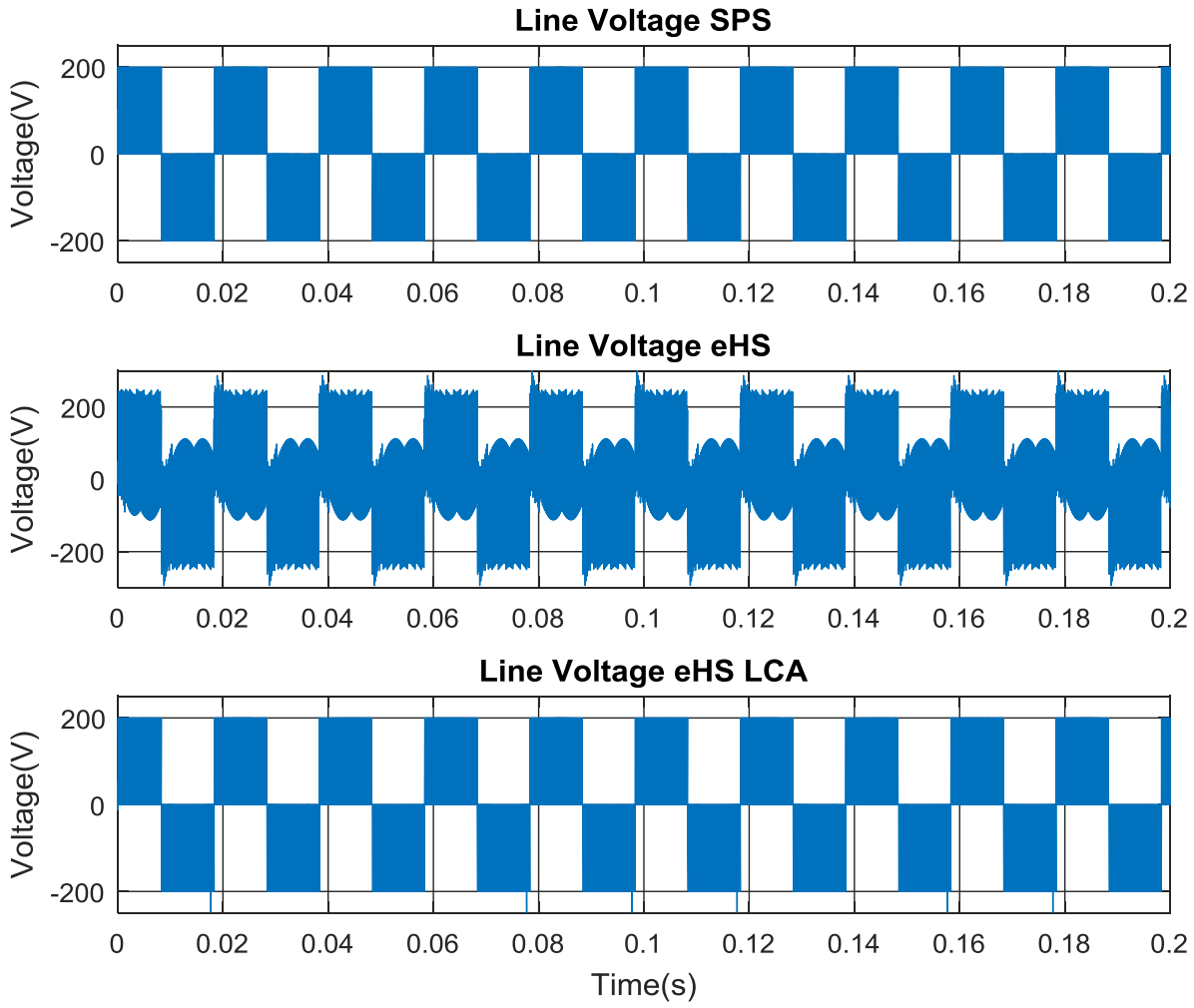

Figure 2.5 Line voltages from SPS, eHS, and eHS LCA (R=25Ω, L=32mH)

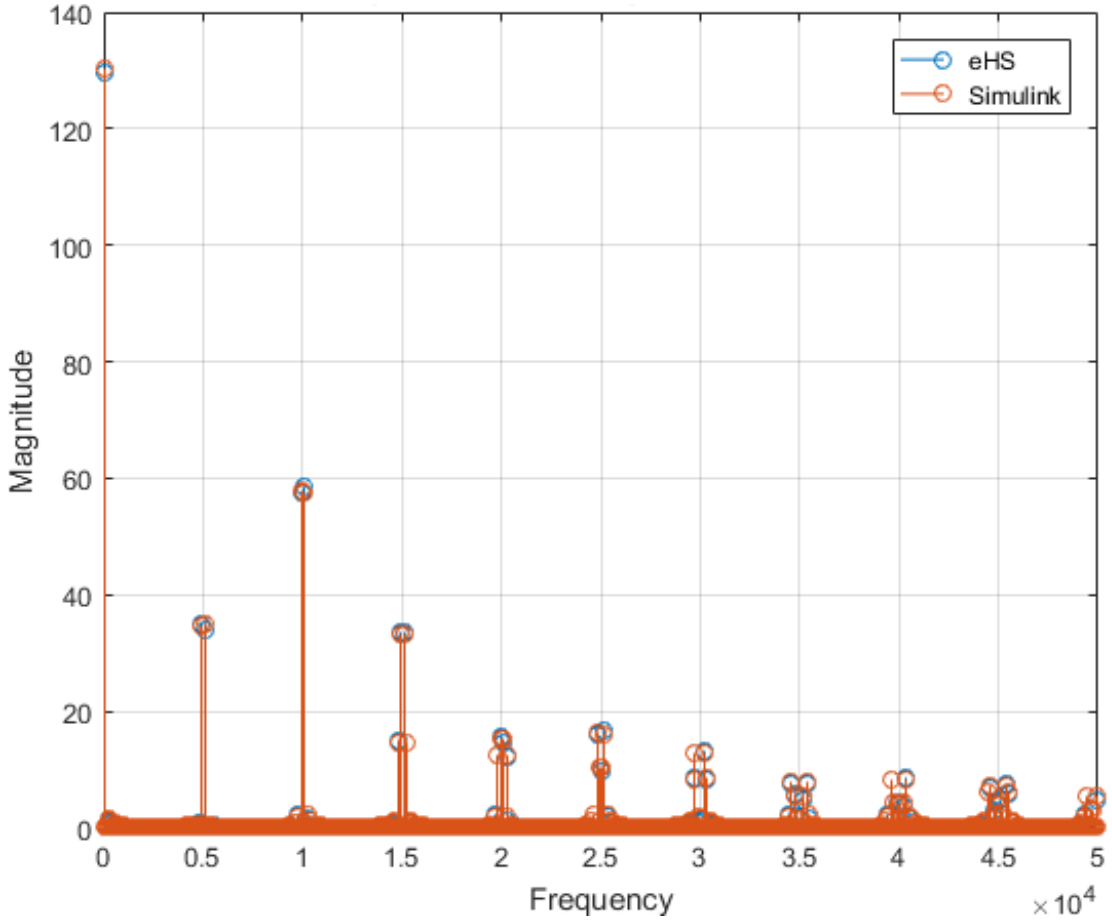

Figure 2.6 Spectral analysis of SPS and eHS line voltages (R=25Ω, L=32mH)

From the spectral analysis, it is observed that the spectral content of the two waveforms is very similar. When zooming into the line voltage from eHS, it is clear that the original shape of the voltage waveform is preserved despite suffering from large oscillations, as shown in Figure 2.7. This is why the waveform has a different look compared to the waveform from SPS. However, these oscillations have negligible effect on the overall performance. This can be seen from the load current waveforms in Figure 2.8 , where the currents from all three inverters are closely tracking each other. Table 2-2 shows a comparison of other voltage and current values from each inverter.

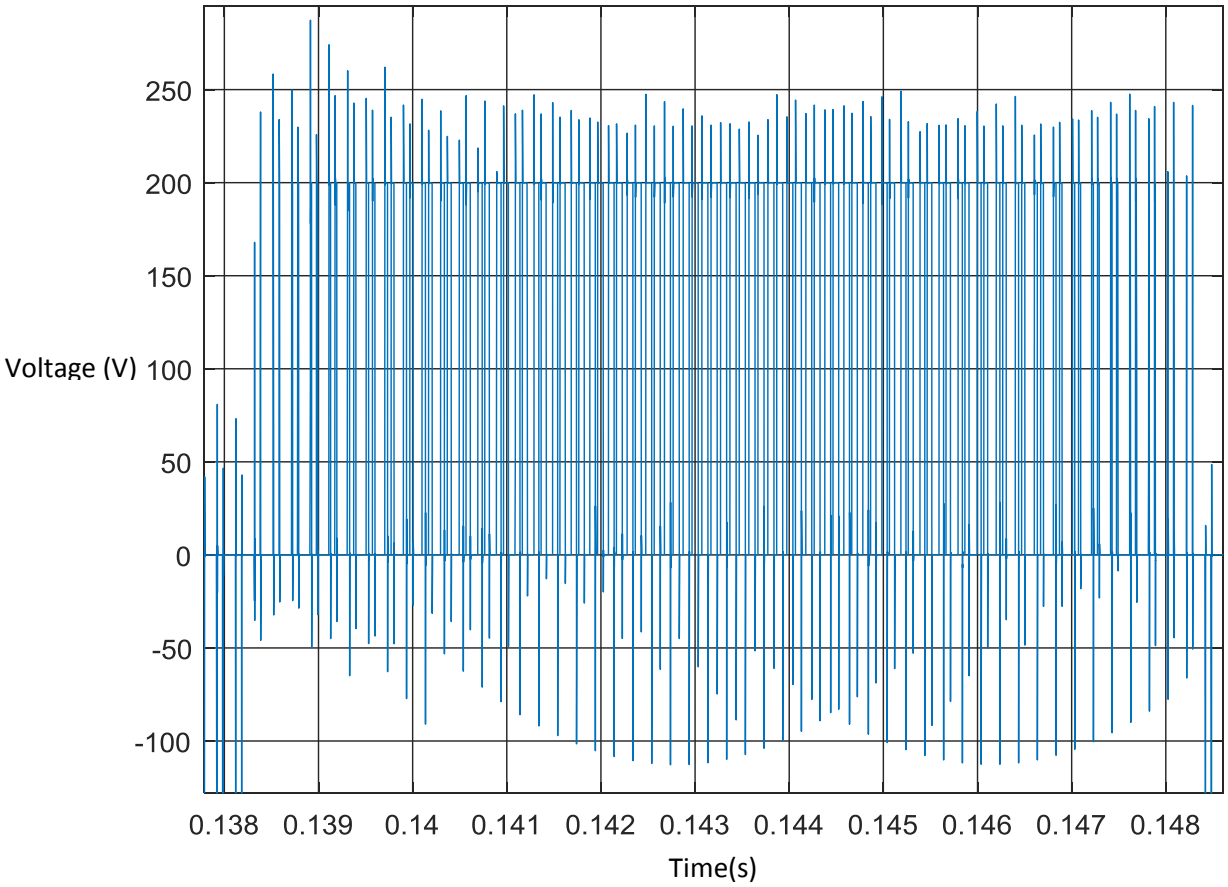

Figure 2.7 Closer view of eHS line voltage

The values returned by eHS LCA are almost identical to those of the SPS values. On the other hand, the values returned by the eHS inverter (without LCA) are slightly lower than those provided by SPS, still within a 2% difference. The efficiency of the eHS inverter is 98.7% whereas the eHS LCA inverter is 99.87%, close to full efficiency. The optimal value of Gs tries to minimize the power loss of the inverter. However, the LCA activated approach tries to achieve ideal results.

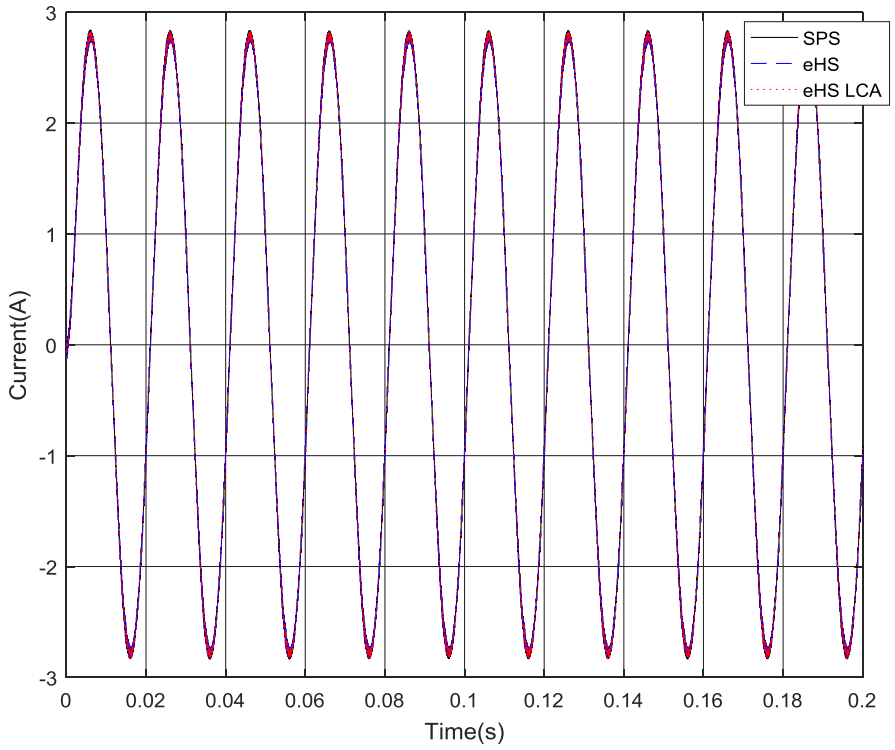

Figure 2.8 Load currents from SPS, eHS, and eHS LCA (R=25Ω, L=32mH)

Table 2-2 Comparison between SPS, eHS, and eHS LCA values for R=25Ω, L=32mH

	SPS	**eHS**	**eHS LCA**
V_{LL} fund.(V)	92.072	91.614	92.065
V_{phase} fund.(V)	53.169	52.897	53.167
I_a fund.(A)	1.973	1.963	1.973
V_{LL}(V)	128.702	128.412	128.661
V_{phase}(V)	74.327	74.148	74.301
I_a(A)	1.974	1.964	1.974
I_{dc}(A)	1.463	1.465	1.463
THD(V_{LL})	97.671	98.217	97.623
THD(V_{phase})	97.685	98.229	97.621
THD(I_a)	2.251	2.257	2.356
Input Power (W)	292.598	293.069	292.55
Output Power (W)	292.192	289.207	292.17
Efficiency (%)	99.86	98.7	99.87

2.5.2 Second Case: R=3Ω, L=500µH, Gs=0.088605

In the second case, the performance of the inverters is tested for higher load condition. Figure 2.9 shows the line voltages from each inverter. Again, the spectral analysis of the eHS line voltage is needed to assess its accuracy. Figure 2.10 shows the spectral content of the SPS and eHS line voltages in the same window. As in the previous case, the spectral content of the two signals are very similar despite their different forms in time domain. The load currents from eHS and eHS LCA are tracking closely the reference current from SPS (Figure 2.11). Table 2-3 summarizes the results of the three inverters. The same conclusions made for the small inductive load apply to larger loads as well.

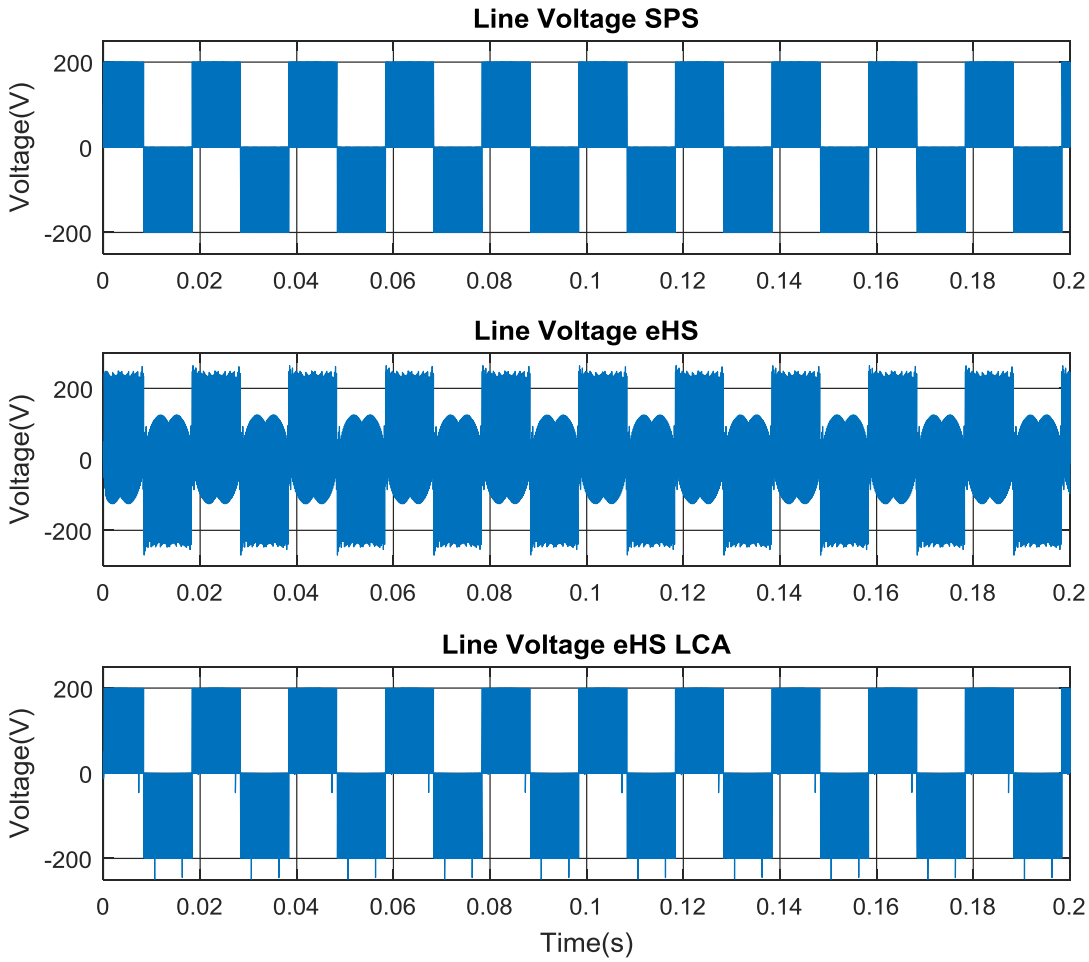

Figure 2.9 Line voltages from SPS, eHS, and eHS LCA (R=3Ω, L=500µH)

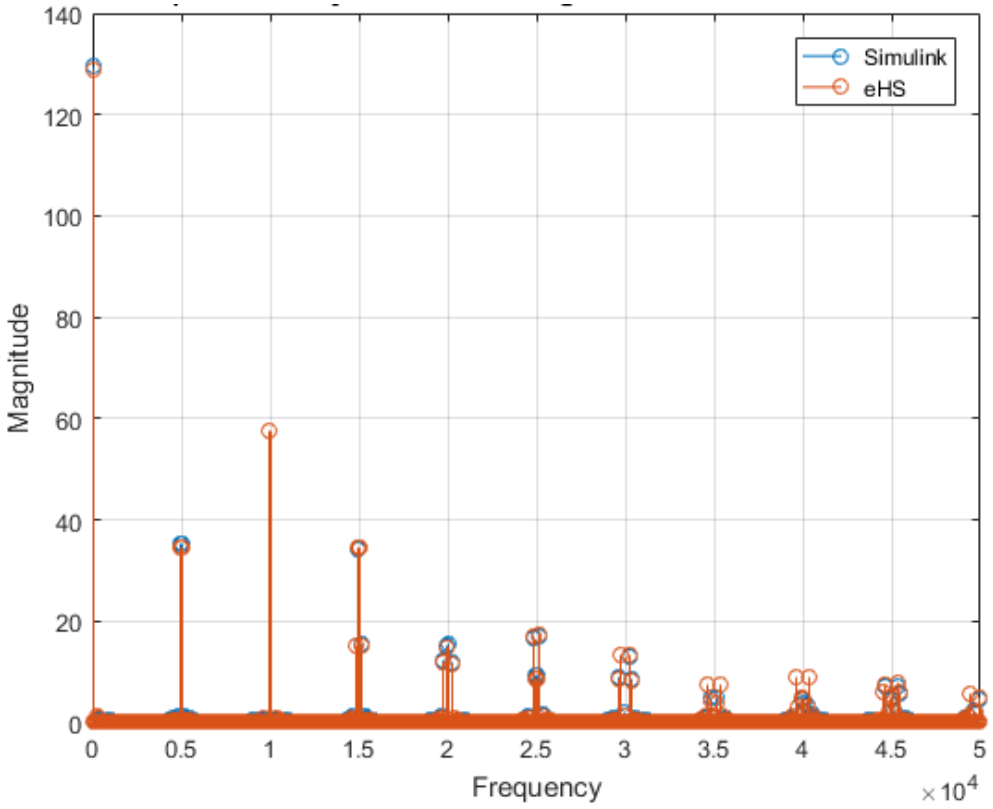

Figure 2.10 Spectral analysis of SPS and eHS line voltages (R=3Ω, L=500µH)

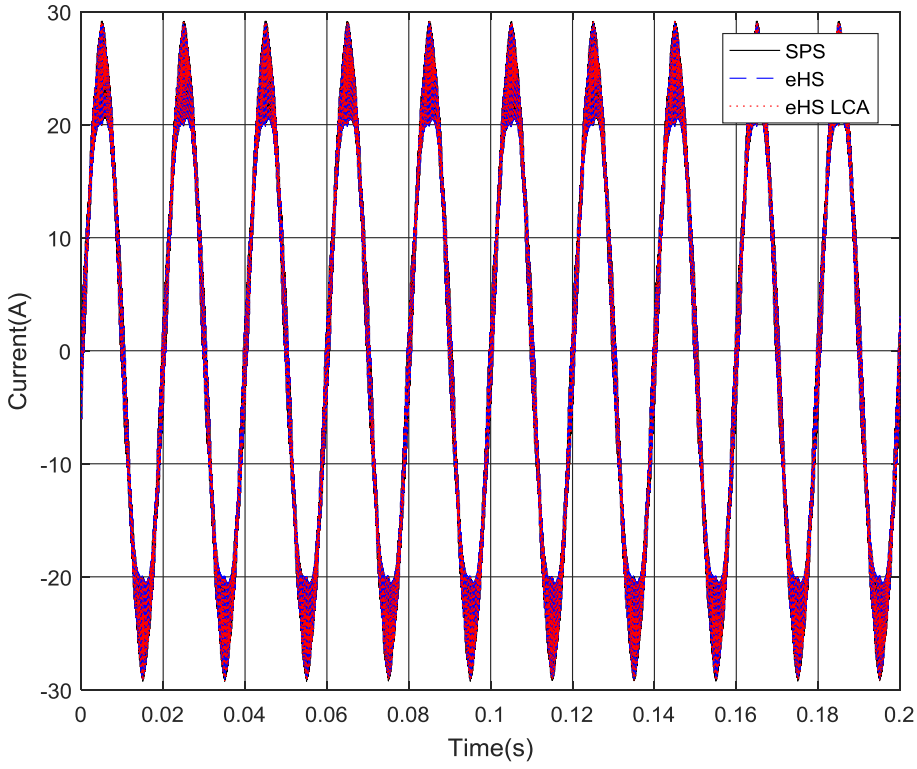

Figure 2.11 Load currents from SPS, eHS, and eHS LCA (R=3Ω, L=500µH)

Table 2-3 Comparison between SPS, eHS, and eHS LCA values for R=3Ω, L=500μH

	SPS	eHS	eHS LCA
V_{LL} fund.(V)	91.753	91.123	91.765
V_{phase} fund.(V)	52.976	52.611	52.968
I_a fund.(A)	17.634	17.513	17.632
V_{LL}(V)	128.690	128.086	128.367
V_{phase}(V)	74.306	73.957	74.107
I_a(A)	17.721	17.598	17.718
I_{dc}(A)	14.135	14.114	14.143
THD(V_{LL})	98.346	98.783	97.819
THD(V_{phase})	98.358	98.796	97.847
THD(I_a)	9.918	9.885	9.863
Input Power (W)	2826.93	2822.83	2828.66
Output Power (W)	2826.28	2787.31	2825.20
Efficiency (%)	99.98	98.74	99.88

2.5.3 Third Case: R=100Ω, Gs=0.004006

In the previous two cases, the load was inductive which filtered out the harmonics in the voltage and resulted in a sinusoidal load current. Now, it is desired to test the performance of the inverters when the waveform of the current is not sinusoidal anymore. OPAL RT provides a support script with its product that assists the user in selecting the optimal value of Gs. In the case of resistive loads, the user has to enter the base power, DC bus voltage, and nominal duty cycle so that the script returns the value of Gs. Next, the results of the inverters are examined while supplying a resistive load with switch conductance (Gs) determined by the script. Figure 2.12 shows the line voltages from SPS, eHS, and eHS LCA.

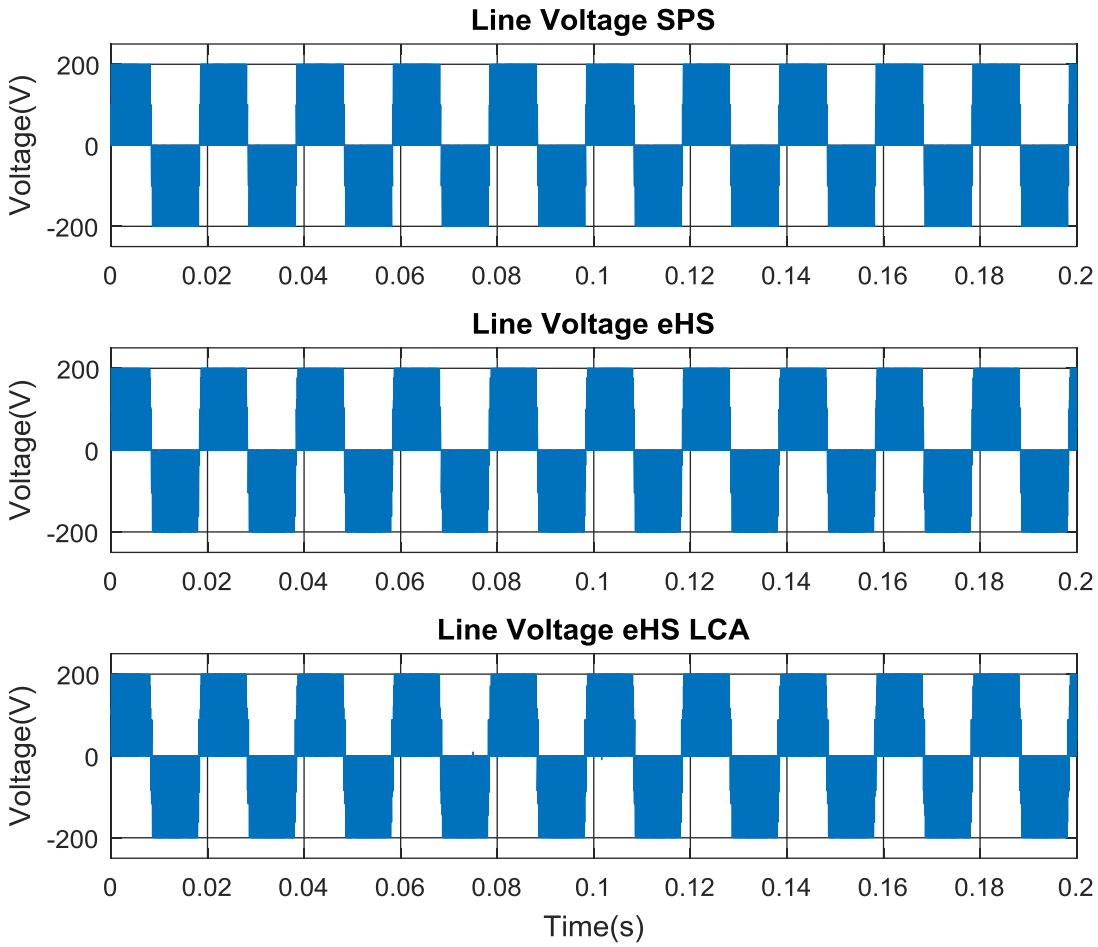

Figure 2.12 Line voltages from SPS, eHS, and eHS LCA (R=100Ω)

In this condition, the line voltage waveforms from all three inverters are very similar. The oscillations in the eHS line voltage, that were previously apparent with inductive loads, have now considerably diminished with the resistive load. The current waveforms, shown in Figure 2.13, are scaled replica of the phase voltage. Therefore, superimposing them will not yield a beneficial implication on their proximity. In this case, the RMS values of the load currents and their fundamental components gives a better insight on their proximity. These values in addition to other parameters are given in Table 2-4.

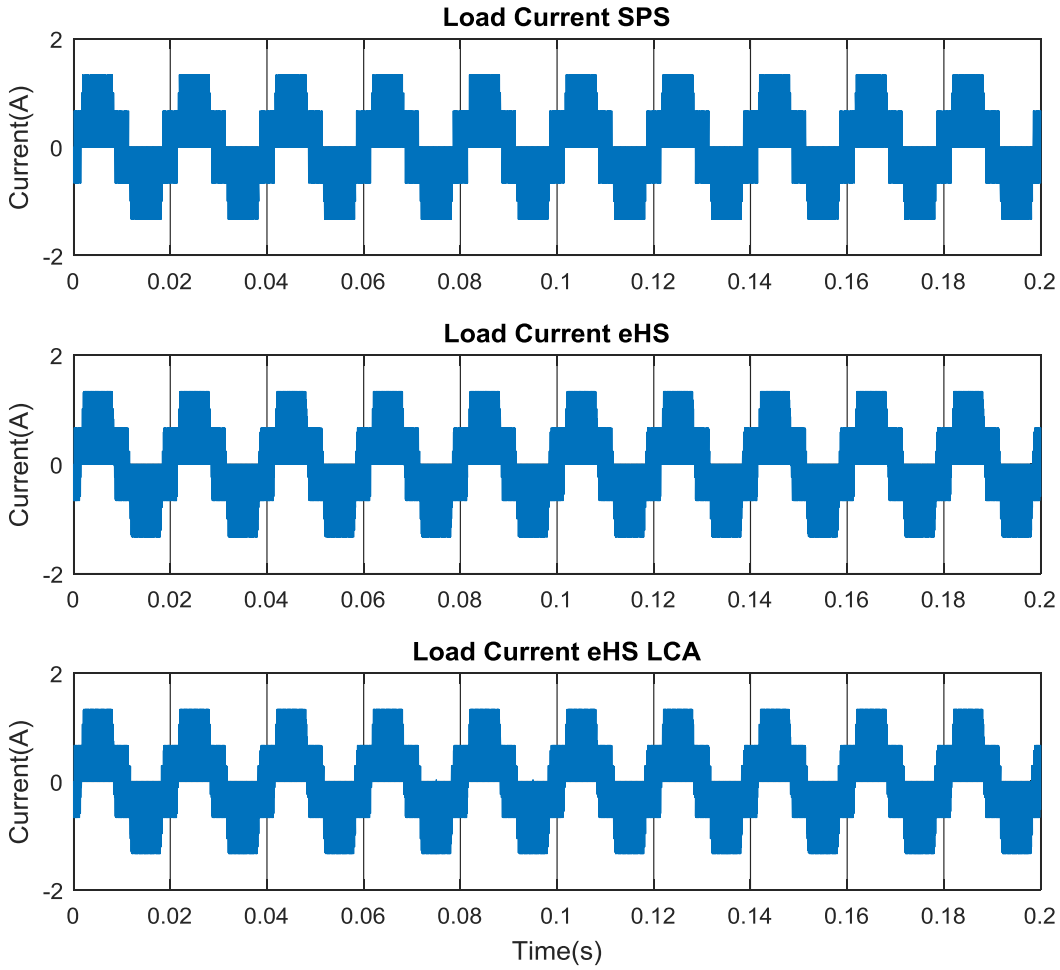

Figure 2.13 Load currents from SPS, eHS and eHS LCA (R=100Ω)

In Table 2-4 , the values returned by eHS and eHS LCA have almost the same percentage difference from SPS. In fact, the values returned by eHS were slightly better than those returned by eHS LCA in some cases. For instance, the percentage difference in the line voltage is 0.32% in eHS and 0.50% in eHS LCA. Moreover, the efficiency of the eHS LCA inverter is slightly lower than the SPS inverter, unlike with the inductive load cases where the eHS LCA inverter efficiency was almost identical to SPS.

Table 2-4 Comparison between SPS, eHS and eHS LCA values for R=100Ω

	SPS	eHS	eHS LCA
V_{LL} fund.(V)	92.469	92.172	92.930
V_{phase} fund.(V)	53.389	53.216	53.656
I_a fund.(A)	0.534	0.532	0.537
V_{LL}(V)	127.740	126.734	126.837
V_{phase}(V)	73.756	73.175	73.235
I_a(A)	0.738	0.732	0.732
I_{dc}(A)	0.822	0.817	0.814
THD(V_{LL})	95.308	94.370	92.890
THD(V_{phase})	95.316	94.379	92.893
THD(I_a)	95.316	94.379	92.893
Input Power (W)	164.34	163.32	162.81
Output Power (W)	163.20	160.64	160.90
Efficiency (%)	99.30	98.36	98.83

2.6 Verification against theoretical expressions and other software

The offline results are further verified by comparing them against the inverter results obtained through the proven mathematical expressions of the two-level inverter. PSIM, which is another reliable software for power electronics simulations, is also used to validate the accuracy of the results. Equation (2.1) describes the line-to-neutral voltage of a two-level inverter. Using this expression, theoretical values of RMS voltages and currents are computed via Matlab. This expression does not include the effect of dead-time. Therefore, in this section, the dead-time is assumed to be zero.

$$Vaz(t) = VdcMcos(\omega_o t) + \frac{4Vdc}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin\left([m+n]\frac{\pi}{2}\right)\cos(m\omega_c t + n\omega_o t) \quad (2.1)$$

Where *M* is the modulation index, *m* is the multiple of the switching frequency, *n* is the multiple of the modulating frequency, *Jn(x)* is the Bessel function of the first kind, ω_c is the switching angular frequency and ω_o is the modulating angular frequency.

Table 2-5, Table 2-6 and Table 2-7 show the results returned by SPS and eHS LCA in addition to the two other references, PSIM and theoretical values. In the three load cases, a very close agreement can be observed between the results from all four sources. This gives further credibility to the eHS LCA results, since they are also matching with other references.

Table 2-5 Comparison between theoretical, PSIM, SPS and eHS LCA values for R=25Ω, L=32mH

	Theoretical	**PSIM**	**SPS**	**eHS LCA**
V_{LL} fund.(V)	97.920	97.922	97.980	97.970
V_{phase} fund.(V)	56.534	56.533	56.569	56.564
I_a fund.(A)	2.098	2.099	2.099	2.099
V_{LL}(V)	132.712	132.781	132.839	132.785
V_{phase}(V)	76.621	76.659	76.700	76.669
I_a(A)	2.099	2.100	2.100	2.100
I_{dc}(A)	1.652	1.654	1.655	1.655
THD(V_{LL})	91.480	91.588	91.550	91.489
THD(V_{phase})	91.480	91.589	91.561	91.500
THD(I_a)	2.271	2.274	2.377	2.378
Input Power (W)	330.40	330.80	331.04	331.00
Output Power (W)	330.20	330.75	330.75	330.67
Efficiency (%)	99.94	99.98	99.91	99.90

Table 2-6 Comparison between theoretical, PSIM, SPS and eHS LCA values for R=3Ω, L=500µH

	Theoretical	**PSIM**	**SPS**	**eHS LCA**
V_{LL} fund.(V)	97.932	97.889	97.951	97.949
V_{phase} fund.(V)	56.540	56.514	56.553	56.552
I_a fund.(A)	18.822	18.824	18.825	18.825
V_{LL}(V)	132.780	132.759	132.818	132.502
V_{phase}(V)	76.661	76.646	76.687	76.505
I_a(A)	18.906	18.908	18.909	18.908
I_{dc}(A)	16.080	16.078	16.094	16.102
THD(V_{LL})	91.560	91.616	91.577	91.101
THD(V_{phase})	91.560	91.616	91.588	91.112
THD(I_a)	9.446	9.449	9.454	9.399
Input Power (W)	3216.00	3215.60	3218.76	3220.31
Output Power (W)	3215.91	3217.61	3217.96	3217.53
Efficiency (%)	99.99	99.94	99.98	99.91

Table 2-7 Comparison between theoretical, PSIM, SPS and eHS LCA values for R=100Ω

	Theoretical	PSIM	SPS	eHS LCA
V_{LL} fund.(V)	97.920	97.921	97.983	97.982
V_{phase} fund.(V)	56.534	56.532	56.571	56.571
I_a fund.(A)	0.565	0.565	0.566	0.566
V_{LL}(V)	132.724	132.782	132.841	132.302
V_{phase}(V)	76.672	76.659	76.701	76.390
I_a(A)	0.766	0.767	0.767	0.764
I_{dc}(A)	0.885	0.882	0.888	0.883
THD(V_{LL})	91.580	91.585	91.547	90.731
THD(V_{phase})	91.580	91.586	91.558	90.742
THD(I_a)	91.580	91.586	91.558	90.742
Input Power (W)	177.00	176.34	177.64	176.65
Output Power (W)	176.03	176.30	176.49	175.06
Efficiency (%)	99.45	99.98	99.35	99.10

2.7 Conclusion

Small and large inductive loads in addition to a small resistive load were used to evaluate the performance of the eHS solver in offline (with and without LCA) and the Pejovic switch with Gs selected as discussed in Chapter 1.

In the case of inductive loads, the line voltages from eHS were observed to have large oscillations which, at the first glance, gave an impression that the waveforms were erroneous. However, after careful inspection and with the aid of the Fourier transform, it is concluded that the voltage waveforms from eHS were technically very similar to their counterpart from SPS, and that the oscillations had negligible effect on the overall performance. These oscillations vanish when the LCA is activated. Values returned by eHS LCA are almost identical to SPS. While the eHS inverter returned slightly lower values, they are still within a 2% difference. Another feature that was investigated is the inverter efficiency. With proper selection of Gs value selected and the LCA activated, the switching losses introduced by the Pejovic approximation are almost nullified.

In the case of resistive loads, the eHS line voltage waveform has the expected form with no oscillations. The LCA with resistive loads is not as effective as with inductive loads. The degree of accuracy in the results of the eHS and eHS LCA inverter were very comparable, while with inductive loads, eHS LCA yielded more precise results.

At the end of this Chapter, a list of questions that need to be addressed in the following Chapters was sought. It shall be explained why oscillations appear in the voltage waveforms when the LCA is not activated, and why are they damped when the load is resistive. A simplified method to determine Gs value without prior knowledge of the inverter outcomes is proposed for resistive load cases. Also, it will be shown the change in the value of Gs to get a closer value of load current to the reference value without degrading the overall efficiency (in case of no LCA). Finally, in the past three tests, the inverters were operating at the point which Gs was calculated for. It is, then, desirable to assess the robustness of Gs to deviations in the operating point.

In the next Chapter, the test plan to validate the eHS solver against an experimental setup is proposed. The same test conditions and load cases are considered in the practical verification.

3. VERIFICATION OF TWO-LEVEL INVERTER WITH PEJOVIC SWITCH IN REAL-TIME

3.1 Introduction

The eHS implementation of the two-level inverter in offline was just an initial verification on the performance of the converter. In practice, the offline implementation is not of substantial use since the existing software packages, such as Simulink and PSIM, are sufficient to study the performance of the converters offline. The significant value of the eHS implementation arises when it is used in very low time-step real-time applications, where the Pejovic switch allows very fast execution of the converter. Therefore, it is of a great importance to ensure that the converter implementation in eHS yields acceptable results in real-time. The performance of eHS in real-time is assessed against an experimental setup. As in Chapter 2, the difference between eHS and real inverter results must be less than 2%.

3.2 Experimental Setup

Figure 3.1 shows the block diagram of the test setup. The OP4510 is responsible for generating the gating signals as well as emulating the two-level inverter. The gating signals generation happens on the CPU, while the inverter is implemented by the FPGA.

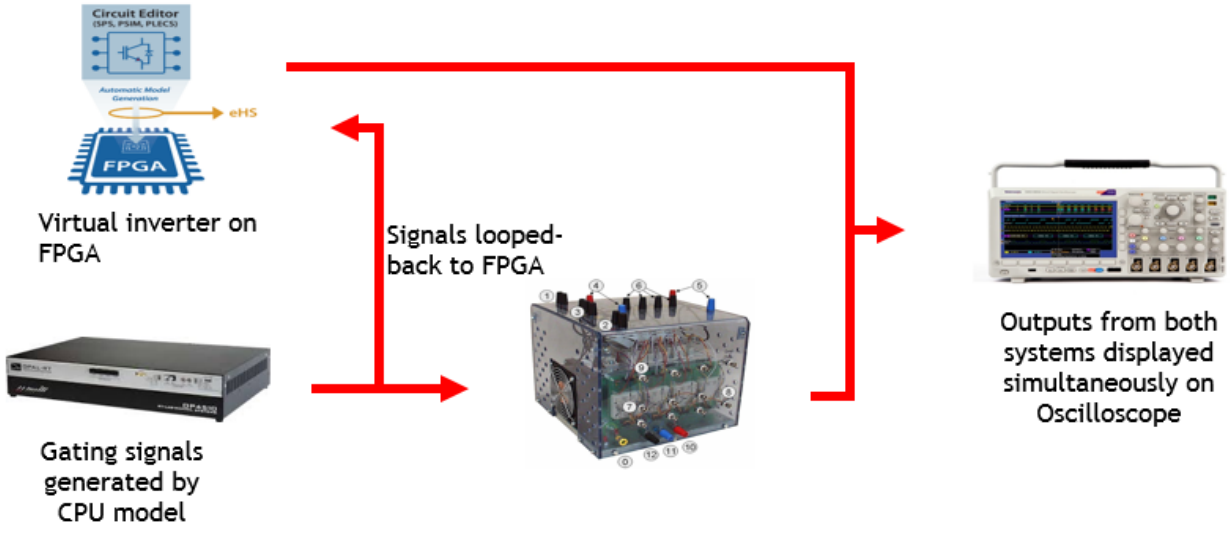

Figure 3.1 Block diagram of test setup

The gating signals generated by the CPU model are provided to a physical inverter and a virtual inverter on the FPGA simultaneously. With such arrangement, it is confirmed that both inverters receive exactly the same signals. Figure 3.2 illustrates the experimental setup.

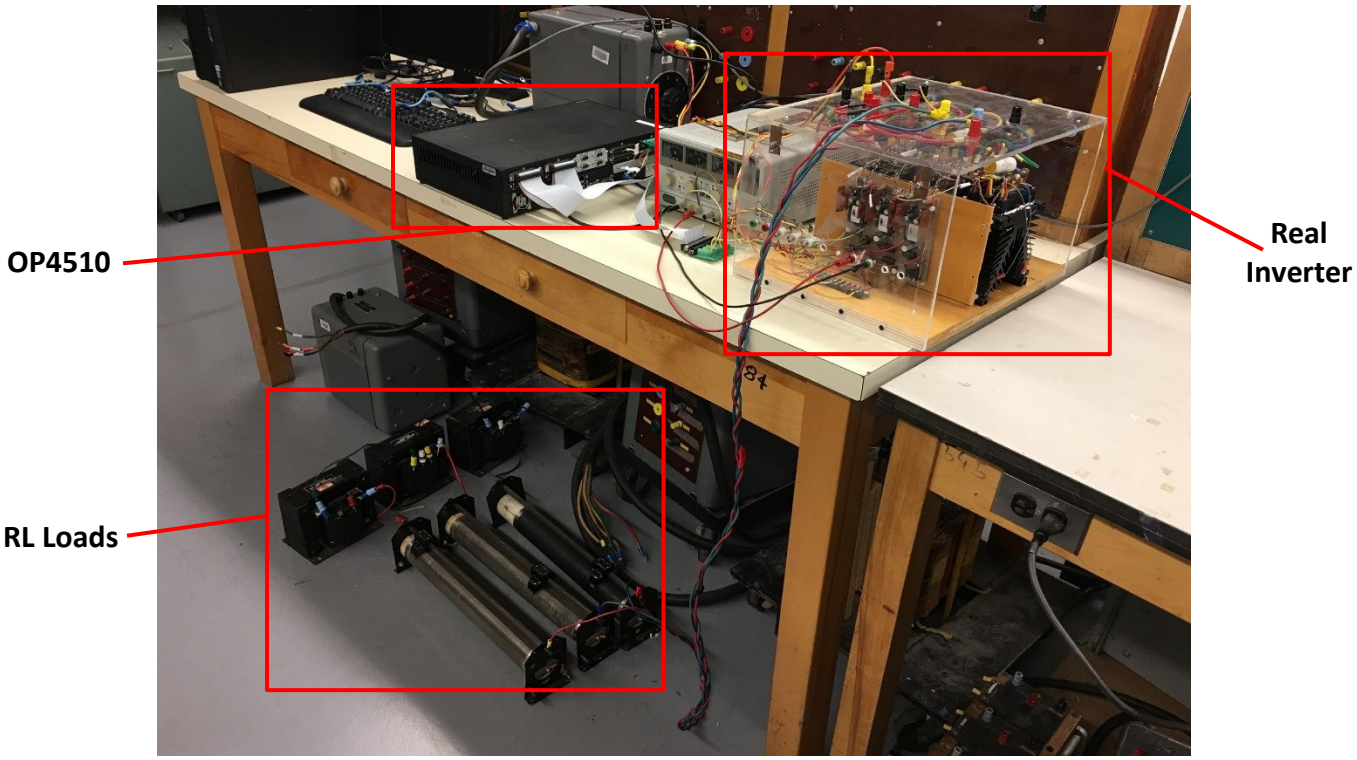

Figure 3.2 Experimental setup

Figure 3.3 shows how the gating signals are distributed. The numbering on the figure is explained next, but before that, the arrangement of the I/O channels in the OP4510 must be addressed. The labelling of the I/O slots on the OP4510 are classified according to the following code:

- 1 for Digital
- 2 for Analog
- A for Input
- B for Output

Therefore, the Analog In slot, for example, is labelled as 2A. Digital Out is labelled as 1B. These labels are clear on the OP4510.

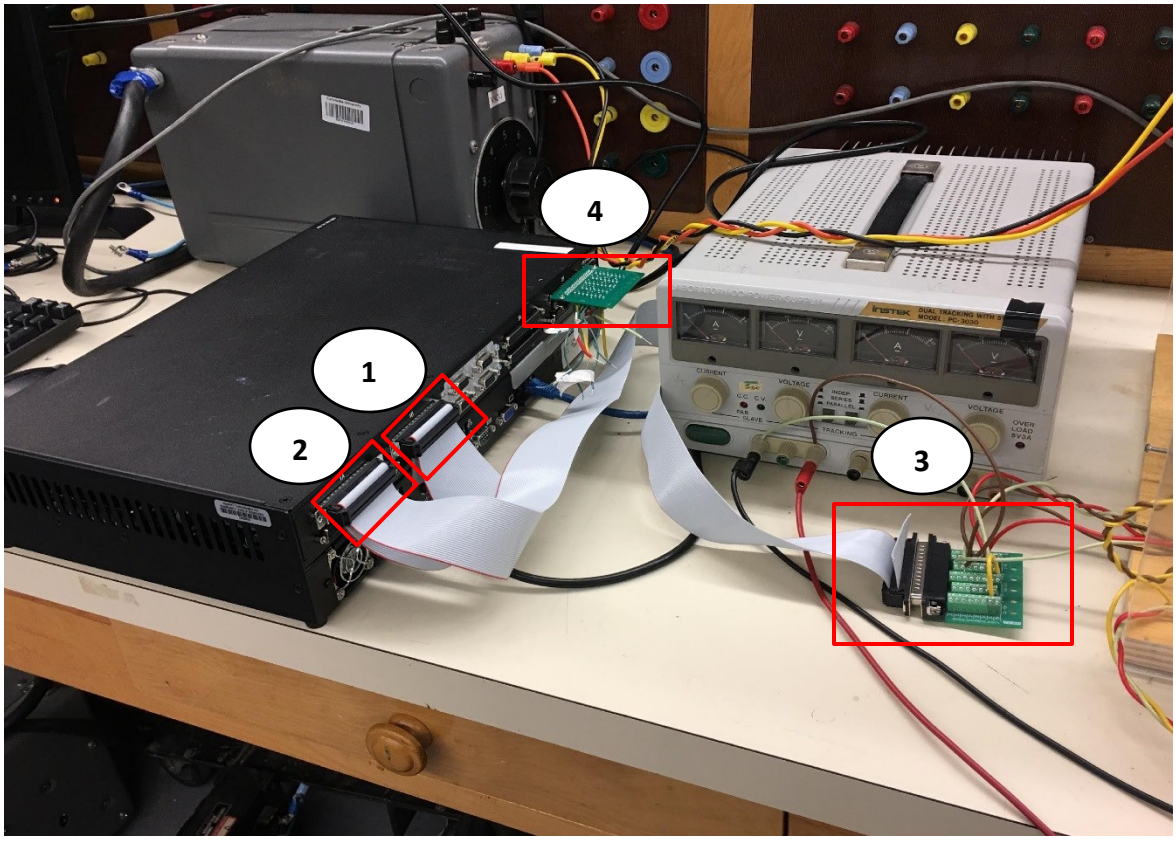

Figure 3.3 Gating signals distribution

- Label 1: This slot is ‘1B’, which corresponds to Digital Output on the OP4510. The gating signals generated on the CPU are delivered through this slot.
- Label 2: This slot is ‘1A’, which corresponds to Digital Input. The gating signals to the virtual inverter are captured by the FPGA through this slot. It can be clearly seen that the gating signals are returned back to the OP4510 through the loop-back cable.
- Label 3: The remaining part of the cable is connected to a DB37 connector to send the gating signals to the physical inverter.
- Label 4: This slot is ‘2B’ corresponding to Analog Output. The outputs of the virtual inverter, such as line voltages and load currents, can be acquired through this slot. It is more accurate to display outputs on the oscilloscope from this slot than observing them on a scope in the software model.

3.3 Test Conditions

The same conditions used in the offline simulations are used for the real-time simulations. However, only two load cases are considered, namely the 25Ω, 32mH case and the resistive load case. Table 3-1 shows the test conditions.

Table 3-1 Test conditions

Parameter	Value
DC Bus Voltage	200V
Modulation Index	0.8
Modulating Frequency	50Hz
PWM Frequency	5kHz
On-state Resistance	1mΩ
Dead time	4μs
Time Step	250ns

3.4 Test Results

The voltage and current waveforms for each load case is presented in the following subsections. The RMS values of voltages and currents recorded in the tables were measured directly from the experimental setup using the Fluke Digital Multimeter. The fundamental components were extracted using a DFT script in Matlab.

3.4.1 First Case: R=25Ω, L=32mH, Gs=0.00986

Figure 3.4 shows the line voltages from eHS, eHS LCA and the practical inverter. The oscillations that were observed in the eHS line voltage in offline simulation are still visible in the real-time simulation, but they are less intensive due to the sampling rate of the DAC in the OP4510. The FPGA outputs are sent to the oscilloscope every 2.5μs, while the FPGA computes outputs every 250ns. In other words, from every 10 FPGA outputs, only one is displayed on the oscilloscope. Therefore, several details in the oscillations are omitted and hence, the effect of the oscillations on the shape of the voltage waveform is less severe.

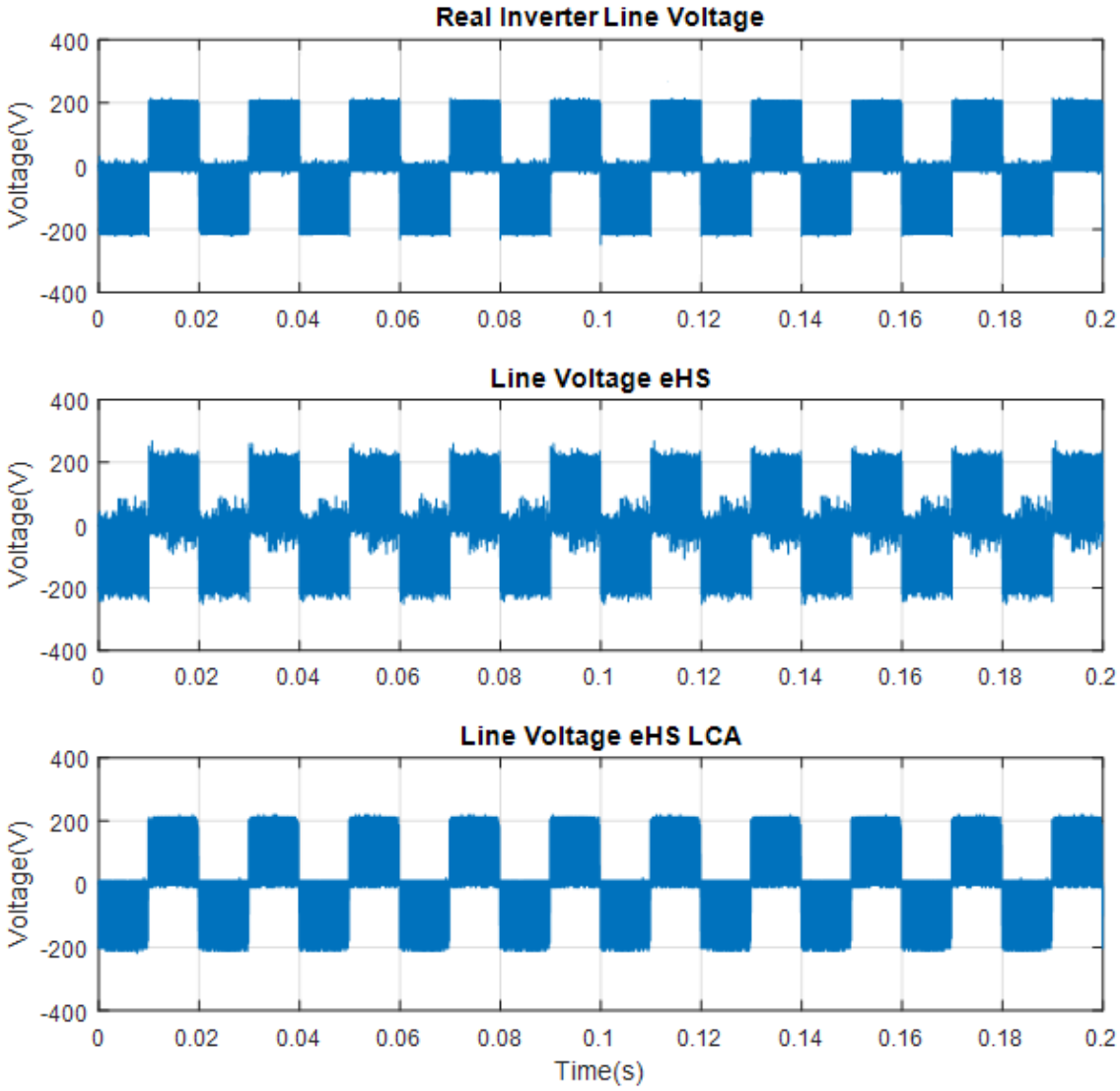

Figure 3.4 Line voltages from real inverter, eHS and eHS LCA (R=25Ω, L=32mH)

Figure 3.5 shows the current waveforms from the two inverters laid on top of each other. Again, it can be seen that there is good agreement between the two current waveforms. The currents from eHS and eHS LCA are closely tracking the current from the real inverter.

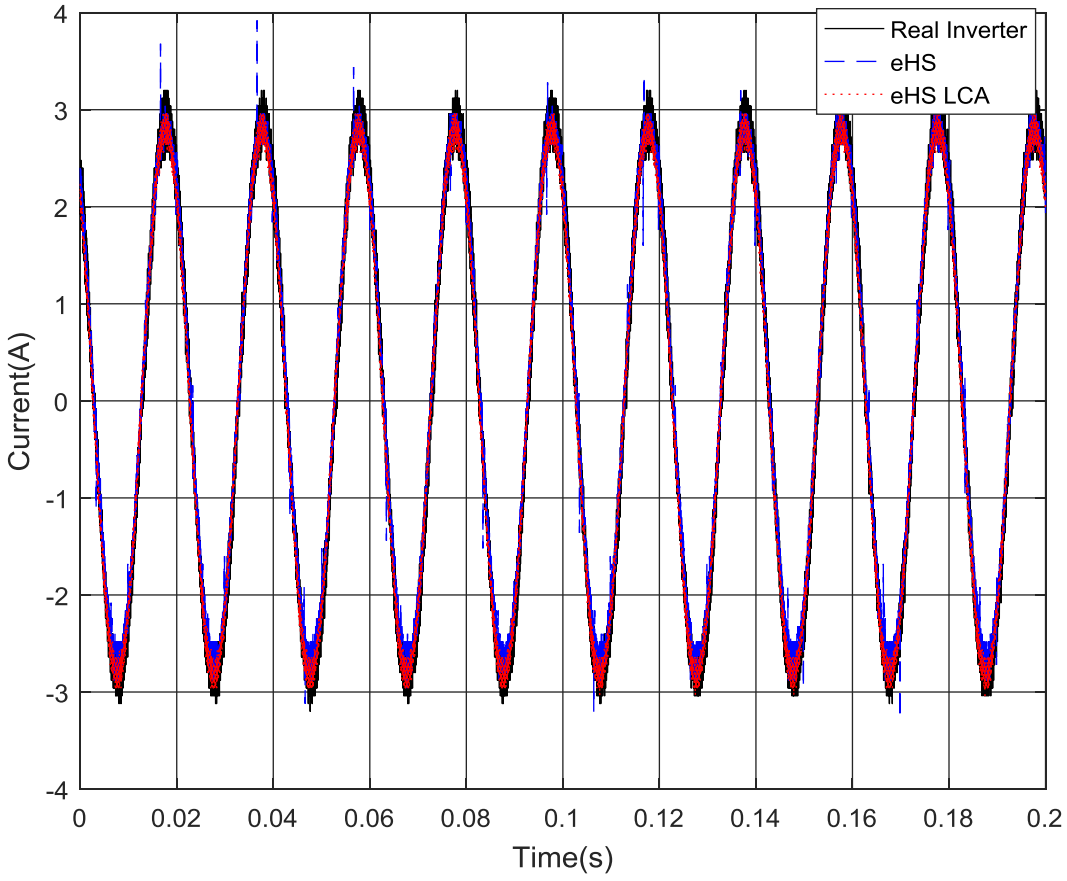

Figure 3.5 Load currents from real inverter, eHS and eHS LCA

Table 3-2 shows a comparison between the RMS values of line voltage and load current from the real and virtual inverters. The values are very close to each other and moreover, they are very close to the values obtained in offline simulation.

Table 3-2 Comparison of RMS values of line voltages and load currents (R=25Ω, L=32mH)

	V_{LL} (V)	V_{LL} fund. (V)	I_a (A)
eHS	128.24	91.92	1.965
eHS LCA	127.47	92.36	1.974
Real Inverter	129.27	92.77	1.973

3.4.2 Second Case: R=100Ω, Gs=0.004006

Figure 3.6 depicts the line voltage waveforms from real and virtual inverters. Figure 3.7 shows the load currents. It can be observed once again that the oscillations in the line voltage of the eHS inverter have dramatically diminished when the load is resistive.

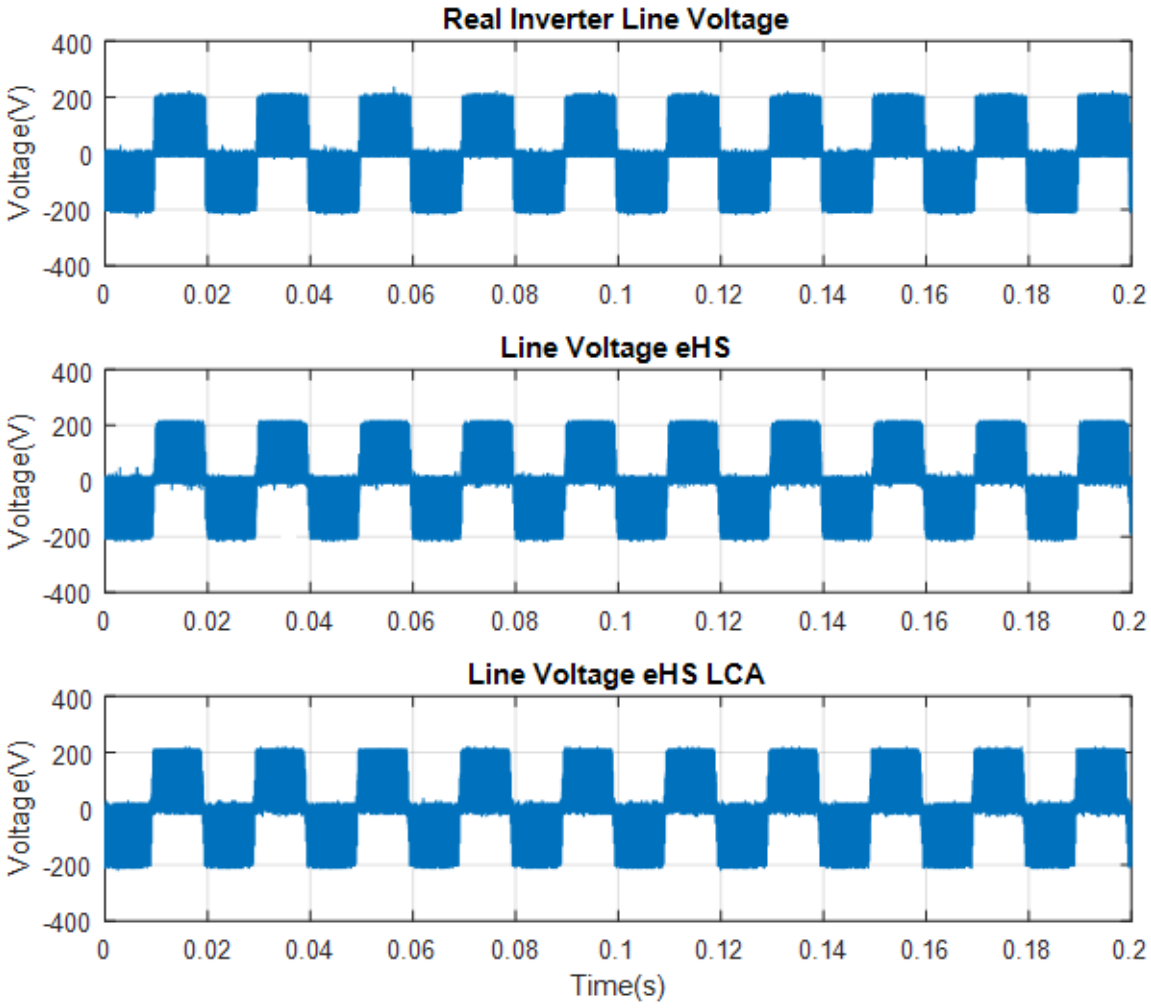

Figure 3.6 Line voltage from real inverter, eHS and eHS LCA (R=100Ω)

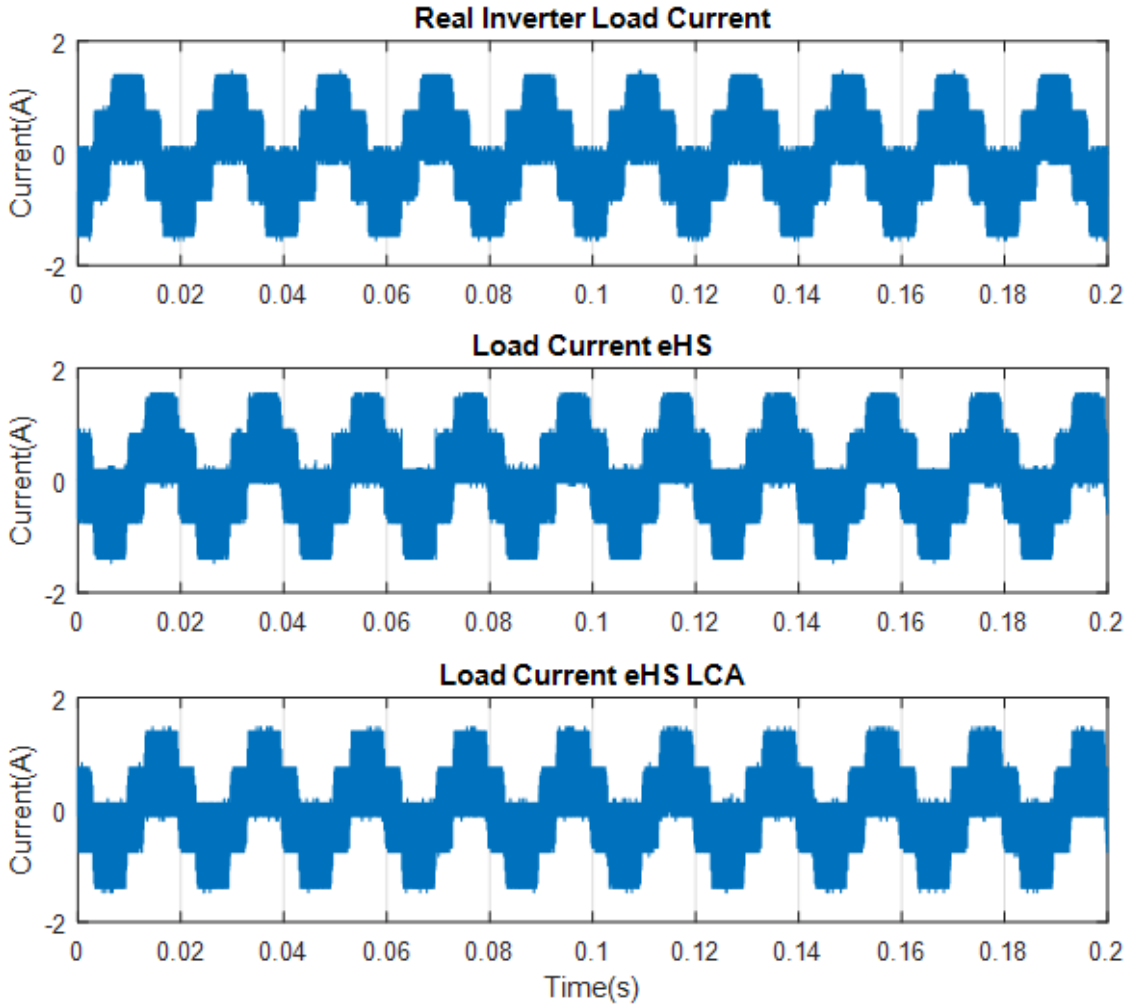

Figure 3.7 Load currents from real inverter, eHS and eHS LCA (R=100Ω)

Table 3-3 shows the RMS values of the line voltage and load current. Since the load currents are not sinusoidal, the RMS values of the load current and its fundamental component are given in the table. The line voltages and the load currents from the real and virtual inverters show very close proximity.

Table 3-3 Comparison of RMS values of line voltages and load currents (R=100Ω)

	V_{LL} (V)	I_a (A)	I_a fund. (A)
eHS	126.23	0.731	0.533
eHS LCA	126.18	0.728	0.529
Real Inverter	126.75	0.742	0.540

3.5 Conclusion

In this Chapter, an FPGA-based real-time simulation of a two-level inverter with a time-step of 250ns was carried out successfully. The results of the eHS and eHS LCA inverters were very close to the results of the practical inverter. Additionally, the results from the real-time simulation were very close to those obtained in offline. There are several conclusions that can be made at the end of this task. First, the eHS offline simulation block renders results that are almost identical to the real-time implementation, which means that this block is reliable for initial validation. Second, the outputs of the practical inverter, with all its non-ideal characteristics such as switching transients and on-state voltage drop, were very close to the SPS results. This means that SPS results can serve as a reliable platform to compare eHS results with. Finally, it has been verified that a two-level inverter with a very low time-step can be simulated with acceptable accuracy in real-time, and that external hardware can be integrated with the virtual inverter.

In Chapter 2 and this Chapter, the eHS inverters were operated at the optimal value of Gs. However, in the next Chapter, the performance of the inverters with a value of Gs slightly different from the optimal value is investigated.

4. ROBUSTNESS OF THE SWITCH CONDUCTANCE (Gs) TO CHANGES IN OPERATING POINT AND FAULTS

4.1 Introduction

When the switch conductance (Gs) is determined for the inverter, it is done only for a single operating point. In other words, it was determined for a known set of values of voltage and current. This is one of the drawbacks of the Pejovic switch model, that the conductance is selected for one operating point. If the load condition changes during the simulation, it is not possible to alter the value of Gs. Otherwise, its feature of maintaining a fixed admittance matrix will be lost if Gs is changed every time the load changes. Therefore, there is a need to study the performance of the inverter while operating at a point different than what Gs was initially calculated for. This is done by applying unbalanced loads, operating the inverter away from its rated conditions and by applying faults to the inverter.

4.2 Unbalanced loads

The value of Gs under study is fixed for the condition when all three phases of the inverter are connected to a 25Ω, 32mH load. The resistive part is changed to create more than 40% deviation in current from its original value. The new load resistance values are 10, 20 and 30Ω respectively. When the loads are balanced, the value of Gs is 0.00986. This value will now be used in the unbalanced case and the results are compared to the true values in offline and in real-time.

4.2.1 Offline Simulation: R_1=10Ω, R_2=20Ω, R_3=30Ω, L=32mH, Gs=0.00986

Figure 4.1 shows the currents for the three phases from SPS, eHS and eHS LCA.

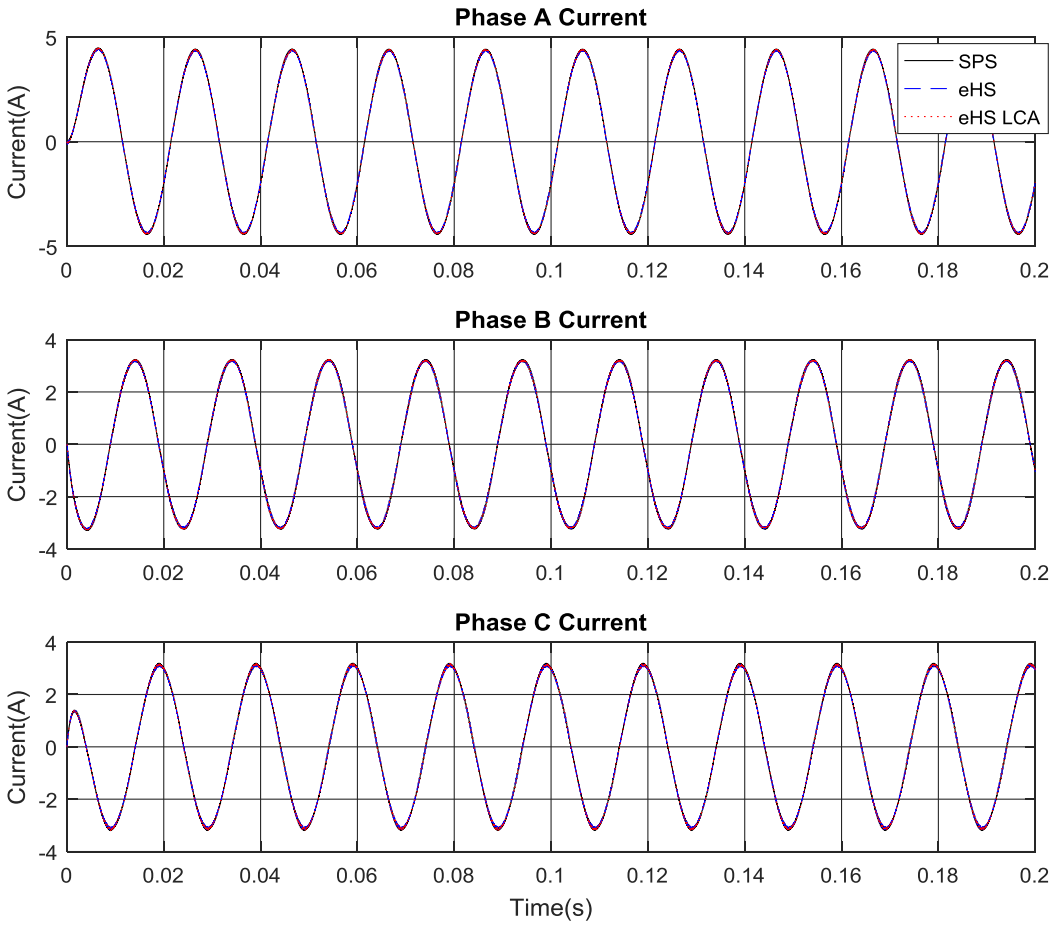

Figure 4.1 Phase currents for three phases from SPS, eHS, and eHS LCA

Figure 4.1 depicts a strong proximity between the currents from SPS, eHS and eHS LCA. Table 4-1 shows the RMS values of the currents in the three phases. In the balanced load case, the current is 1.9738A. Now, the current in phase A is 3.101A, which is a 57% increase on the initial operating point. The RMS values from eHS LCA as well as the total efficiency are identical to the ones given by Simulink. The values returned by eHS are slightly lower but are within the 2% difference range. Total efficiency has dropped from 98.7% to 98.2%, which means that the efficiency will drop further if the load unbalance increases.

Therefore, in unbalanced load conditions, the same value of Gs used in balanced load conditions can still yield acceptable results. Furthermore, if the LCA is activated, the differences occurring due to the load unbalance are compensated, and accurate results are obtained at the output.

Table 4-1 RMS values of voltage and current in unbalanced load conditions (offline)

	V_{LL} (V)	I_a (A)	I_b (A)	I_c (A)	Efficiency
SPS	129.107	3.101	2.282	2.186	99.5%
eHS	128.831	3.071	2.267	2.169	98.2%
eHS LCA	129.038	3.100	2.281	2.186	99.5%

4.2.2 Real-time Simulation: R_1=10Ω, R_2=20Ω, R_3=30Ω, L=32mH, Gs=0.00986

It is now desired to check whether the results obtained in real-time are similar to those from offline. The same loading conditions and the same switch conductance are used.

Table 4-2 shows a comparison between the values of line voltage and phase A current obtained from eHS, eHS LCA and real inverter. For a second time, there is a good agreement between the values from the three inverters, which supports the conclusion reached in the previous subsection.

Table 4-2 RMS values of voltage and current in unbalanced load conditions (real-time)

	V_{LL} (V)	I_a (A)
eHS	128.09	3.0997
eHS LCA	127.91	3.097
Real Inverter	128.31	3.053

4.3 Operating away from rated conditions

Loading conditions of a converter may vary during operation. For example, an induction motor fed by a two-level inverter can be running at a rated load. Later, the load can be removed, and the motor operates at no load condition. Likewise, a two-level inverter can be supplying a house from a solar panel. The loading conditions of the inverter will always vary depending on the consumption in the house. When attempting to simulate these cases in real-time, the optimum

value of Gs has to be changed each time the load changes. However, as was previously mentioned, this is not possible as it contradicts the purpose of using the Pejovic switch model in the first place. Therefore, in this section, the value of Gs for the inverter is picked according to its rated values. The inverter is then run at only 20% of the rated condition and the accuracy of the results is observed. In this section, the performance of the inverter is studied using offline simulation only.

4.3.1 Case 1: 20% of Rated Current

The first assumption is that each switch of the inverter is rated at 200V, 10A RMS. Therefore, the optimum value of Gs is 0.05 according to equation (1.9). In this subsection, it is assumed that the inverter will only supply 20% of its rated current, which is equal to 2A. The optimum value of Gs for this condition is 0.01, but the value of 0.05 corresponding to rated condition is used in the simulation.

Table 4-3 shows a summary of the results obtained when the inverters are operated at 20% load current. The first column under eHS and eHS LCA shows the values returned have the optimal Gs been used. The next column is the results obtained when Gs for rated conditions is used.

Considering the results obtained from the eHS inverter first, one can notice that by increasing Gs beyond the optimum value, the RMS values of voltages and currents also increase. In this case, they even increased beyond the real values given by SPS. Nonetheless, this gives an indication that it might be possible to find a value of Gs that can render results closer to the values given by SPS.

The percentage error is 1.5% in the fundamental component of line voltage and 1.6% in fundamental component of the load current. In terms of RMS values, the error in line voltage is 0.5% and 1.6% in load current. The THD in the line and phase voltages dropped down because the increase in the fundamental component outweighed the increase in the total RMS value. The error in the THD is 2.4%. In terms of efficiency, the expected drop in efficiency is noticed. The optimum value of Gs is selected to result in minimum power loss, so by deviating away from this point, the power losses will inevitably increase. Yet, the drop in efficiency in this case is not very severe. All in all, since most percentage errors are less than 2%, the converter performance can be considered acceptable when it is operated below rated current.

The values returned by the eHS LCA inverter are almost identical whether the optimal or rated Gs is used. They were also very close to the SPS values. Additionally, there was no drop in efficiency when rated Gs was used as in the case of eHS inverter.

Table 4-3 Comparison between SPS, eHS and eHS LCA at 20% of rated inverter current

	SPS	eHS		eHS LCA	
		(Gs_{opt}=0.01)	(Gs_{rated}=0.05)	(Gs_{opt}=0.01)	(Gs_{rated}=0.05)
V_{LL} fund.(V)	92.072	91.614	93.593	92.065	92.075
V_{phase} fund.(V)	53.169	52.897	54.036	53.167	53.174
I_a fund.(A)	1.973	1.963	2.0054	1.973	1.973
V_{LL}(V)	128.702	128.412	129.294	128.661	128.715
V_{phase}(V)	74.327	74.148	74.651	74.301	74.332
I_a(A)	1.974	1.964	2.0059	1.974	1.974
I_{dc}(A)	1.463	1.465	1.551	1.463	1.463
THD(V_{LL})	97.671	98.217	95.309	97.623	97.685
THD(V_{phase})	97.685	98.229	95.319	97.621	97.678
THD(I_a)	2.251	2.257	2.272	2.356	2.356
Input Power (W)	292.598	293.069	301.78	292.55	292.61
Output Power (W)	292.192	289.207	310.18	292.17	292.25
Efficiency (%)	99.86	98.70	97.29	99.87	99.88

4.3.2 Case 2: 20% of Rated Voltage

In this subsection, the inverter is assumed to be provided with only 20% of the rated voltage and supplies rated current. In other words, the DC bus voltage will be only 40V. The optimum value of Gs based on these conditions is 0.25, which is five times larger than the value at rated conditions. In simulation, the value of 0.05 used for Gs is fifth the corresponding optimum value.

Table 4-4 shows a summary of the results obtained when the inverters are operating with 20% of its rated voltage. The first observation that can be noticed in the eHS inverter results is that the load current with Gs at rated value is quite low compared to the actual current (SPS). There is a 4% difference between the currents, while in the previous scenario, there was a 1.6% difference in current. This was clearly reflected on the output power from eHS, where it was 8% less than the actual output power. This makes sense since the output power is proportional to the square of the load current, hence the error in power will be double the error in current. The second major issue

is the THD in the line and phase voltages. In the previous section, the difference was 2.4%, while in this case, the difference reaches up to 10%. All of the aforementioned shortcomings were rectified with the LCA activated. Almost full efficiency was achieved.

Table 4-4 Comparison between SPS, eHS and eHS LCA at 20% of rated inverter voltage

	SPS	eHS		eHS LCA	
		(Gs_{opt}=0.25)	(Gs_{rated}=0.05)	(Gs_{opt}=0.25)	(Gs_{rated}=0.05)
V_{LL} fund.(V)	18.367	18.271	17.628	18.365	18.359
V_{phase} fund.(V)	10.605	10.549	10.178	10.605	10.601
I_a fund.(A)	10.118	10.065	9.7104	10.117	10.114
V_{LL}(V)	25.729	25.662	25.970	25.715	25.660
V_{phase}(V)	14.857	14.818	14.997	14.849	14.818
I_a(A)	10.120	10.067	9.7128	10.120	10.116
I_{dc}(A)	7.675	7.681	7.250	7.675	7.669
THD(V_{LL})	98.095	98.626	108.188	98.010	97.651
THD(V_{phase})	98.111	98.638	108.220	98.021	97.666
THD(I_a)	2.287	2.195	2.260	2.288	2.286
Input Power (W)	307.01	307.23	289.99	307.01	307.03
Output Power (W)	306.98	304.03	283.02	306.98	307.01
Efficiency (%)	99.9	99.0	97.6	99.9	99.9

Based on the results shown in Table 4-3 and Table 4-4, when the LCA is not activated, selecting a value of Gs that is slightly higher than the optimum value will yield acceptable results at the output. However, when Gs is lower than the optimum value, results at the output will carry significant errors. The load current will be low resulting in low output power and the THD in the line and phase voltages will significantly increase.

From the above study, it can be stated that if:

Gs for a two-level inverter is selected according to the rated values, then

- Operating the inverter at a lower current will not have significant adverse effects on the accuracy of the results
- Operating the inverter at a lower voltage will have significant adverse effects on the accuracy of the results, and the user should be careful when simulating such cases.
- Activating LCA will result in acceptable results in both cases.

4.4 Converter Operation under Faults

One purpose of a HIL simulation is to validate the performance of protection systems. Before judging whether the protection system is working correctly, the soundness of the outputs provided from the converter need to be checked such that the protective device will react accordingly. In this section, faults are introduced by blocking some of the switches in the inverter and checks on whether the outputs would match the actual values will take place. The comparison is done in offline and real-time.

Figure 4.2 illustrates the switches that are blocked in the scenario. Two load cases are used and the optimum value of Gs under the respective normal conditions is selected. It is of great importance to learn whether the optimum switch conductance under normal conditions will still perform appropriately in faulty conditions. If that is not the case, the user needs to be conscious when selecting Gs, and shall have prior knowledge of whether the converter will be operated in sound or faulty conditions.

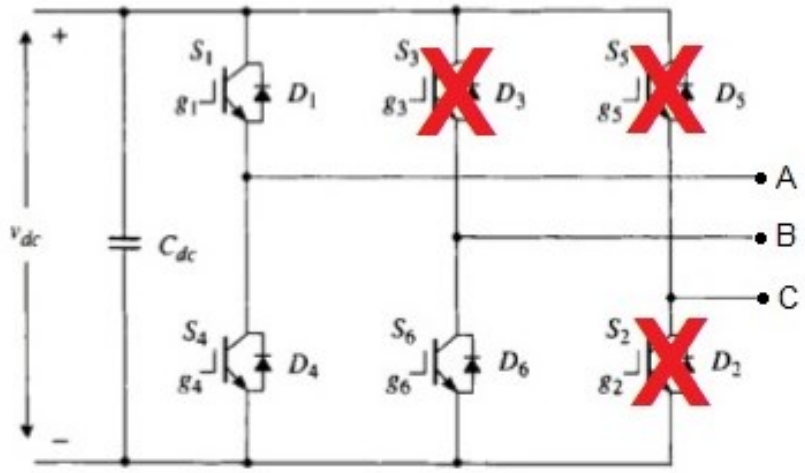

Figure 4.2 Blocked switches in the converter

4.4.1 Offline Simulation with Fault Introduction

The two load conditions and the respective Gs are: 25Ω, 32mH, Gs=0.00986 and 3Ω, 500µH, Gs=0.0886. In this part of the study, eHS LCA will only be used as the virtual inverter. It is only when discussing faulty situations that eHS LCA will be referred to simply as eHS.

4.4.1.1 First Case: 25Ω, 32mH, Gs=0.00986

Figure 4.3 shows the line voltages from SPS and eHS. The positive cycles are almost similar, but there is a noticeable difference in the negative cycles. In terms of load current in phase A, shown in Figure 4.4, the currents are closely tracking each other except for some small oscillations about the zero level in the current from eHS. Inspecting the waveforms, especially for the line voltage, is not sufficient to deduce that the eHS results are acceptable. Table 4-5 shows a comparison of the RMS values of the line voltage and the load currents. The values of the load current in each phase are very close to each other. However, there is a considerable difference in the line voltages. The percentage error in the line voltage from eHS is 21.7%, which is completely out of range and can cause erroneous performance of voltage-oriented protection systems. Next, another load case is presented to investigate the reoccurrence of the same problem.

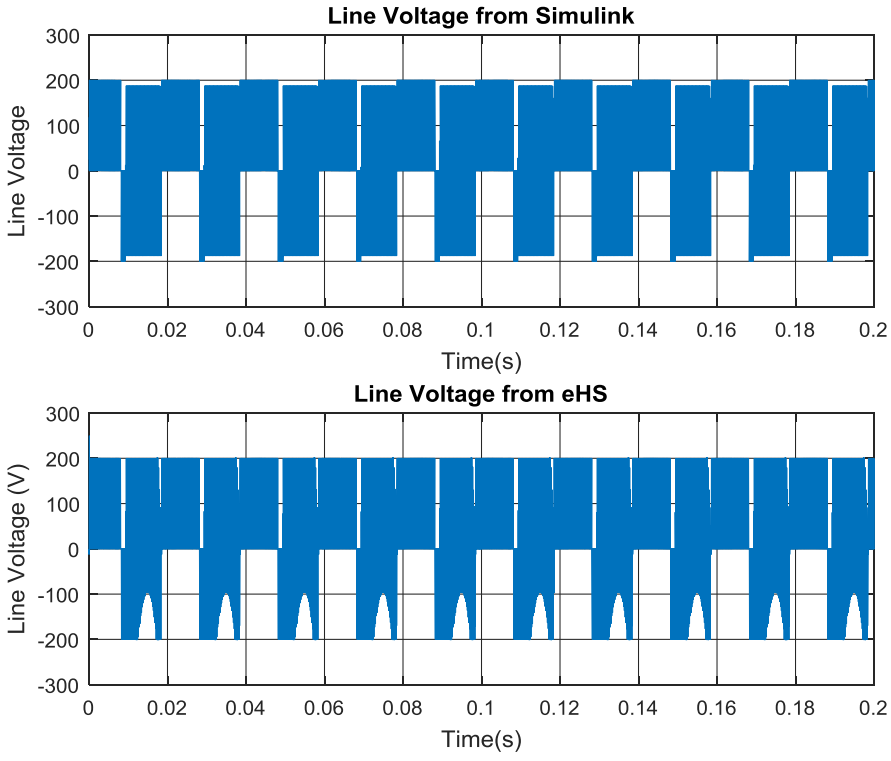

Figure 4.3 Line voltages from SPS and eHS in faulty condition (R=25Ω, L=32mH)

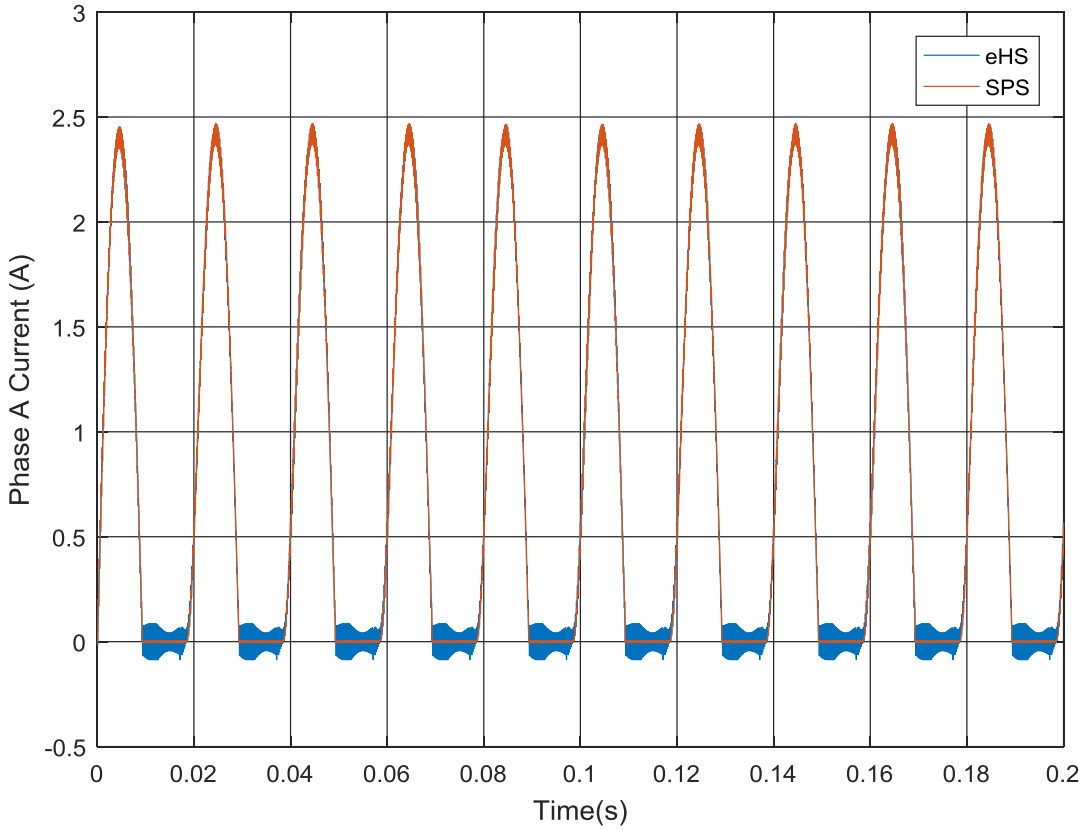

Figure 4.4 Load currents from SPS and eHS in faulty condition (R=25Ω, L=32mH)

Table 4-5 Comparison of RMS voltages and currents from SPS and eHS under faults (R=25Ω, L=32mH)

	V_{LL} (V)	I_a (A)	I_b (A)	I_c (A)	Efficiency
SPS	92.176	1.2026	1.2024	0.0017	98.4%
eHS	112.212	1.2052	1.2021	0.0366	98.25%

4.4.1.2 Second Case: 3Ω, 500µH, Gs=0.0886

Figure 4.5 shows the line voltages from SPS and eHS. In this case, it is quite difficult to say that the waveforms are similar. Actually, by inspection one can simply say they are completely different. Nevertheless, the RMS values in Table 4-6 show that the difference is smaller than the one that was obtained in the earlier case. The percentage error is now 11%, and the waveforms of the load currents are very similar as shown in Figure 4.6. Yet again, there are oscillations about the zero level in the eHS current that are now more noticeable when the load was increased. Next, the first load case is repeated in real-time to make sure that the results are consistent with the offline simulation results.

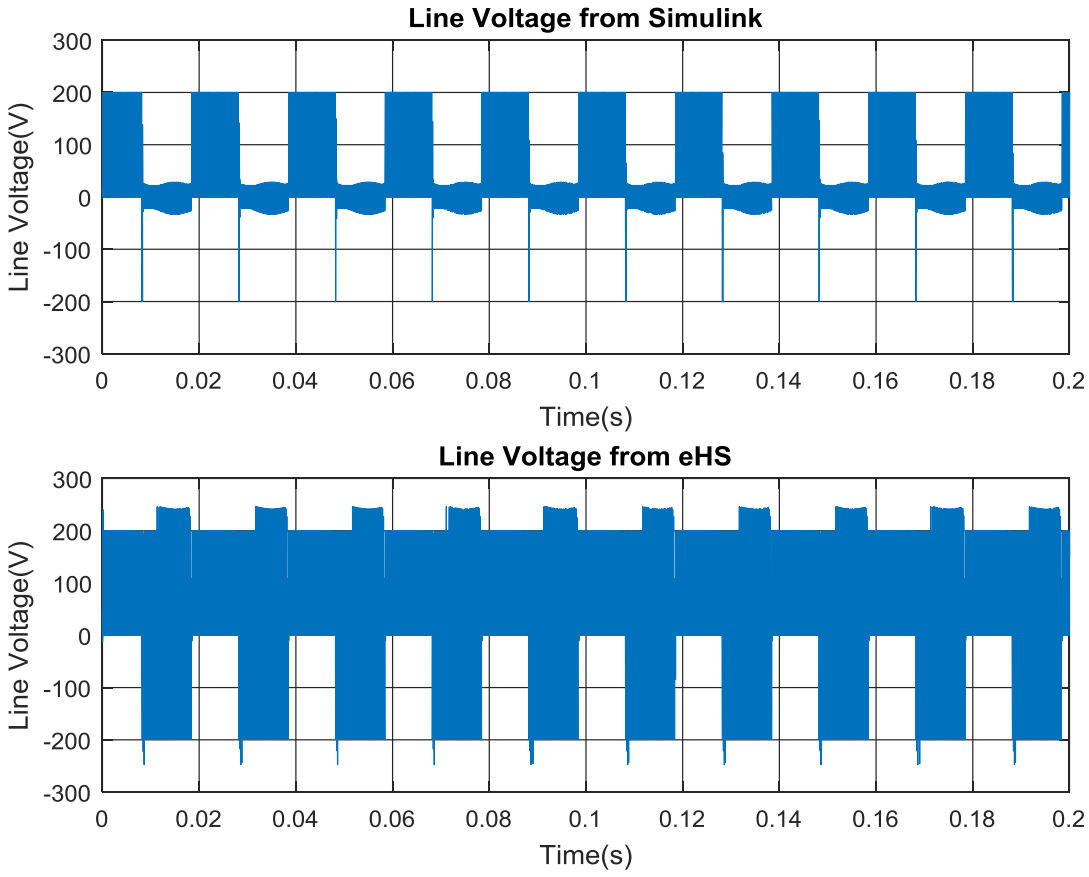

Figure 4.5 Line voltages from SPS and eHS in faulty condition (R=3Ω, L=500µH)

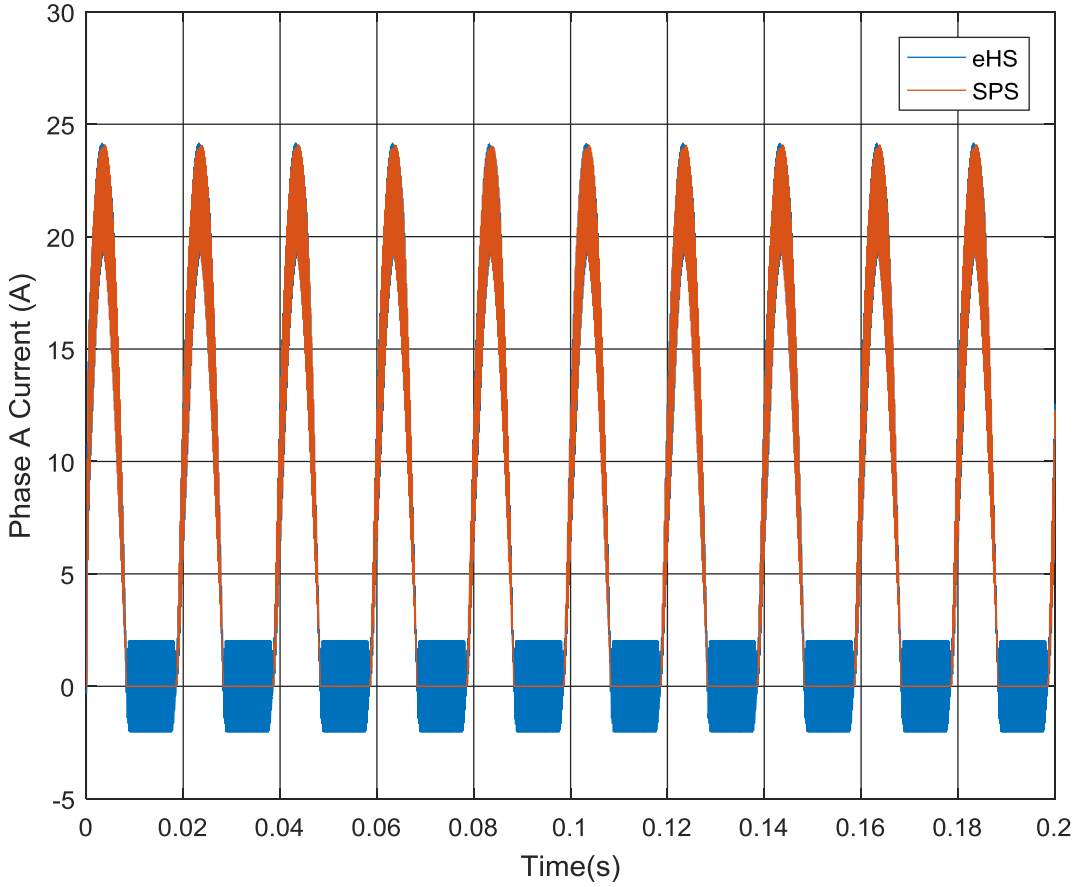

Figure 4.6 Load current from SPS and eHS in faulty condition (R=3Ω, L=500μH)

Table 4-6 Comparison of RMS voltages and currents from SPS and eHS under faults (R=3Ω, L=500μH)

	V_{LL} (V)	I_a (A)	I_b (A)	I_c (A)	Efficiency
SPS	89.664	10.727	10.727	0.0023	99.8%
eHS	100.802	10.778	10.742	0.703	99.3%

4.4.2 Real-time Simulation with Fault Introduction

In this section, the first load case (25Ω, 32mH) is considered due to the unavailability of the other load in the laboratory. Figure 4.7 and Figure 4.8 show the line voltages and load currents respectively. The shape of the waveforms is very similar to the waveforms obtain from offline simulations. Table 4-7 shows that the conclusions derived in the previous section stand valid. While there is a large difference in the line voltages, the load currents are very similar. This consistency between offline and real-time results permits further investigation of the results in either environment. From now on, the offline results are considered to explore the problem in the line voltages. In the following subsection, the DFT of the line voltages is computed to understand the cause of the large difference in line voltages while load currents are similar.

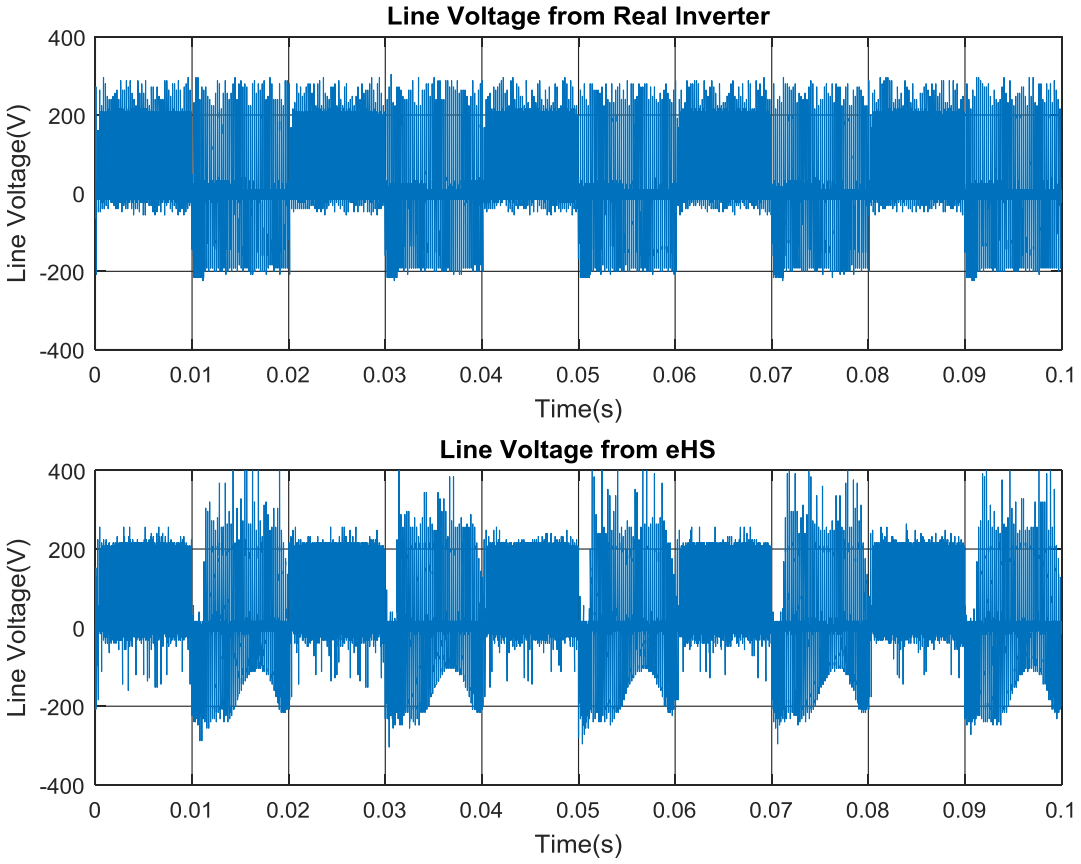

Figure 4.7 Line voltages from real and eHS inverters in faulty condition

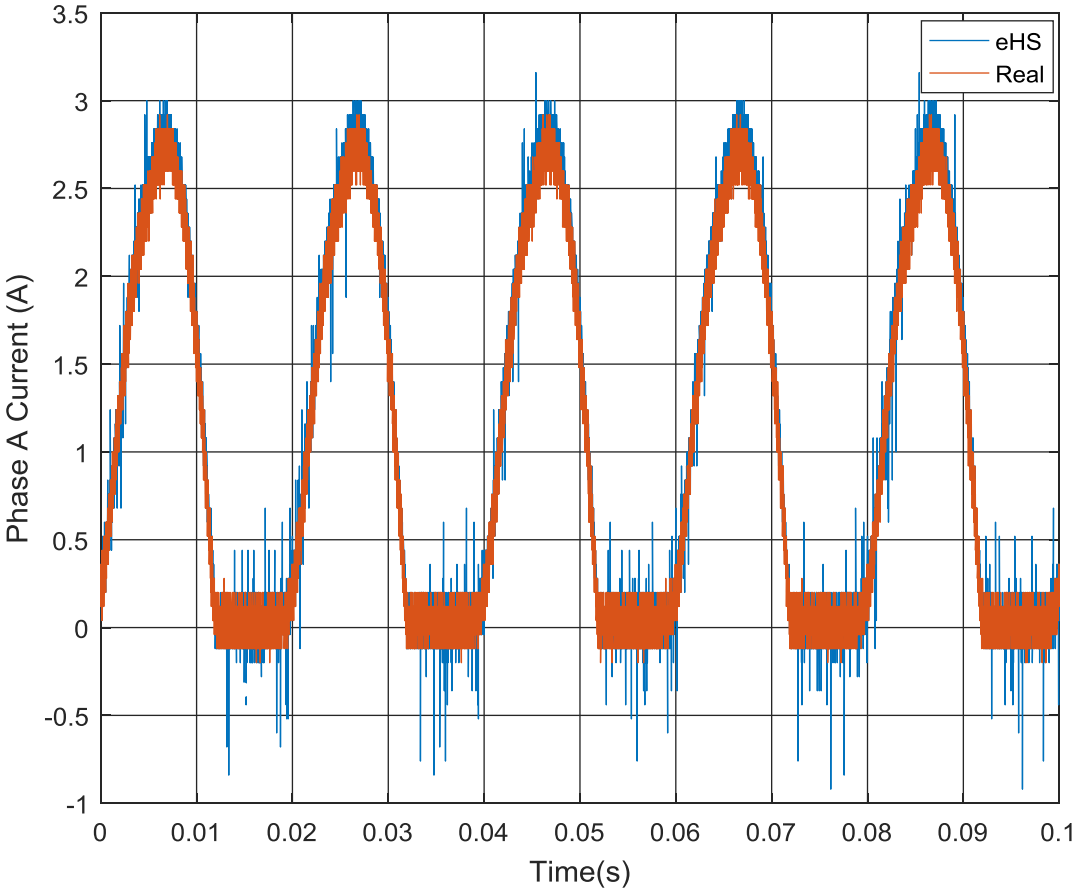

Figure 4.8 Load currents from real and eHS inverters in faulty condition

Table 4-7 Comparison of RMS voltages and currents from real and eHS inverters

	V_{LL} (V)	I_a (A)
eHS	112.21	1.215
Real Inverter	95.21	1.214

4.4.3 DFT of Line Voltages in Faulty Conditions

The DFT of the line voltages provides a deeper understanding of the content of the signals to understand where the problem occurs. The harmonic content of the signals will be presented for the following frequencies: fundamental frequency, switching frequency, two times switching frequency and three times switching frequency. Figure 4.9 to Figure 4.12 show the spectral content of the line voltages in the aforementioned order.

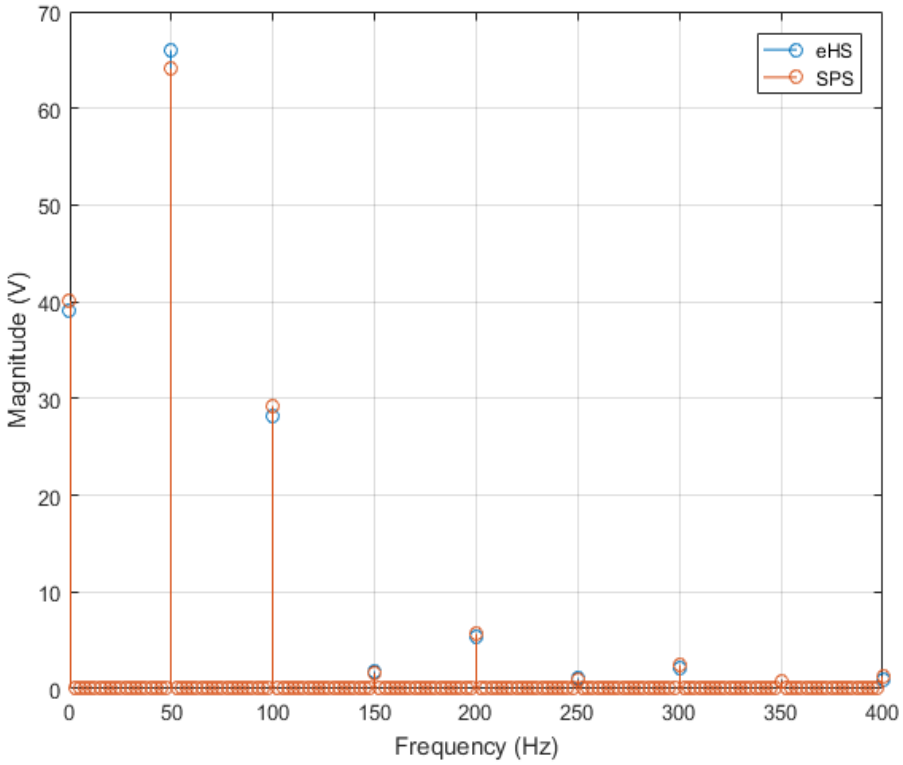

Figure 4.9 Spectral content at fundamental and low order frequencies

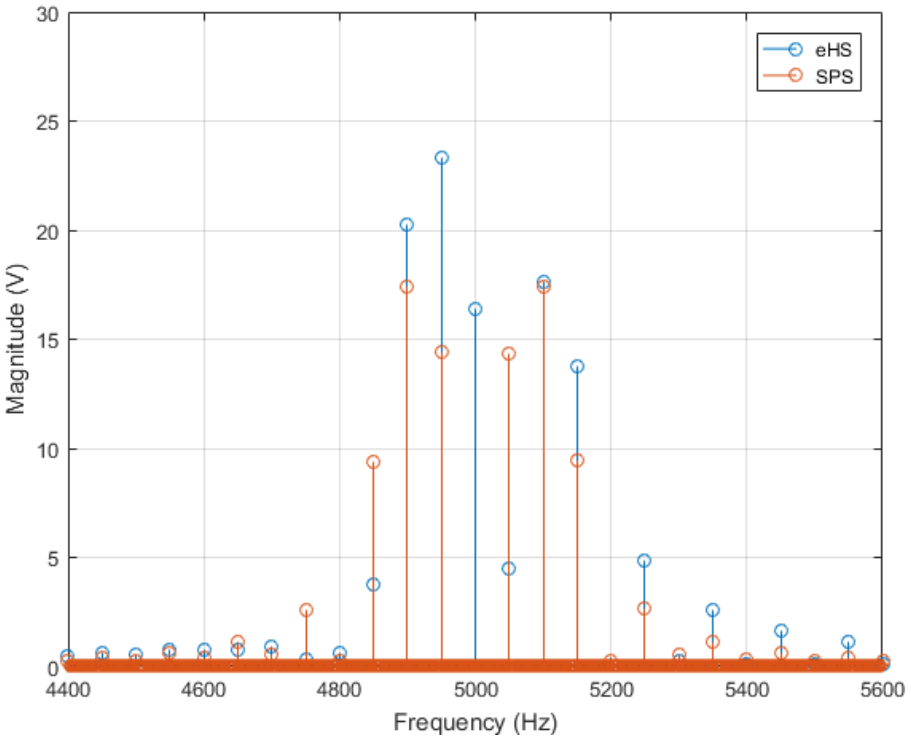

Figure 4.10 Spectral content at and around switching frequency

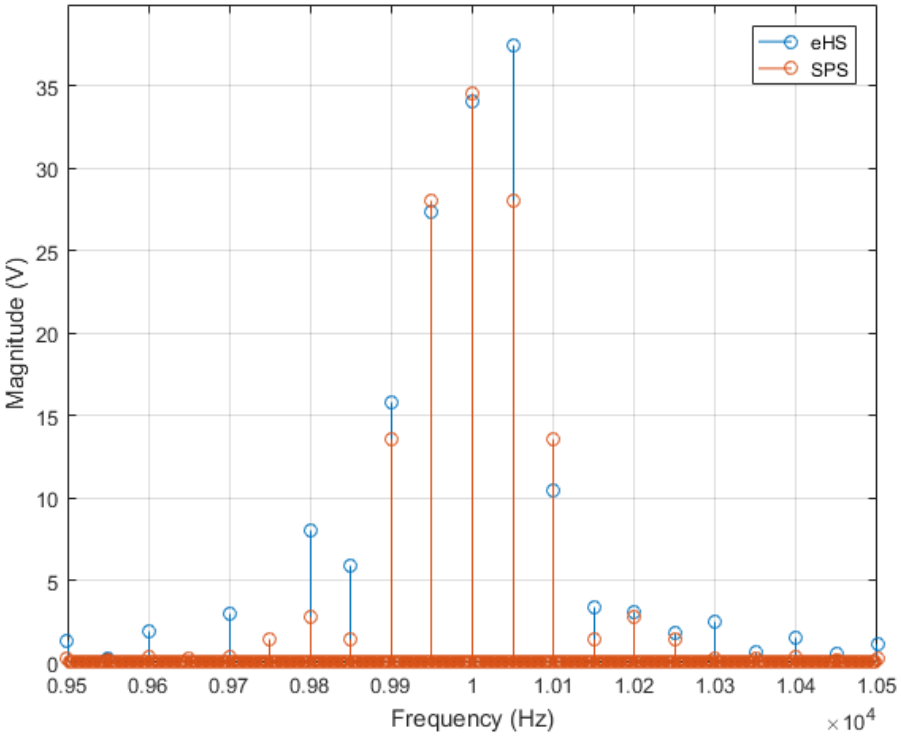

Figure 4.11 Spectral content at and around 2x switching frequency

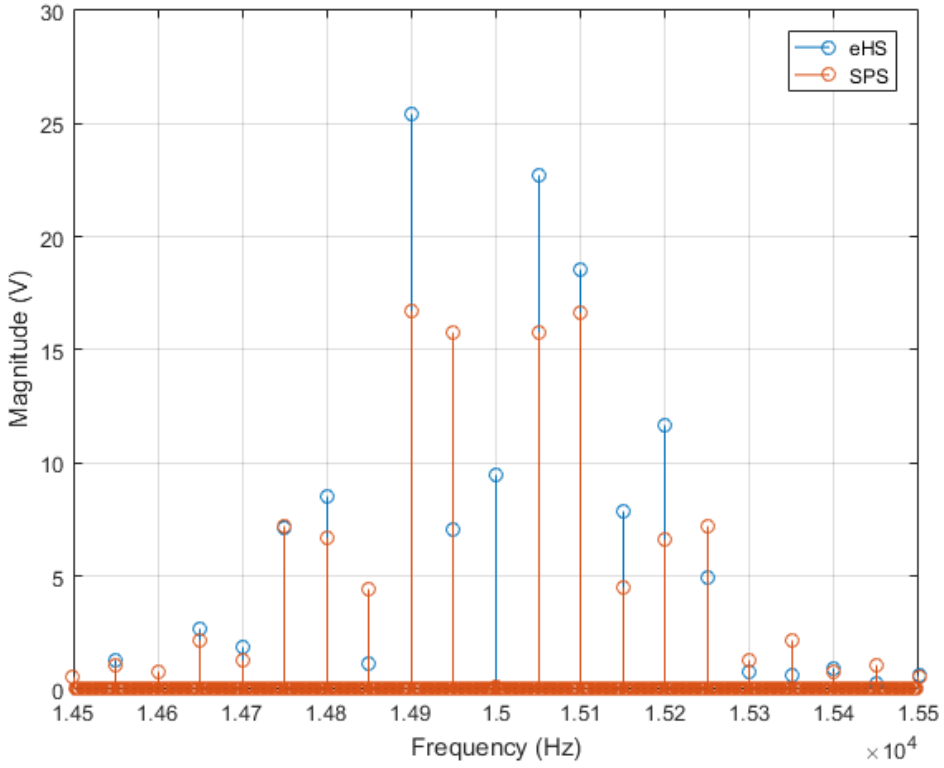

Figure 4.12 Spectral content at and around 3x switching frequency

The following observations can be noted from Figure 4.9 to Figure 4.12:

- The magnitudes of the fundamental and low order components are very close to each other
- There is an added component at odd multiples of the switching frequency in the eHS line voltage that does not exist in the SPS line voltage
- Away from the low order frequency range, considerable differences can be observed in the voltage magnitude between eHS and SPS, and in most cases, the eHS magnitude is higher.

These observations help to further understand the results obtained in the previous subsection. The load currents are very similar because the low order components of the line voltages are similar and the higher order components, that are quite different, are filtered out

by the inductive load. Had the load been resistive, considerable differences would have been seen in the load currents. There is a large difference in the line voltages due to the artificial component introduced by eHS at odd multiples of the switching frequency, and additionally because of the high order components of eHS being mostly larger than SPS.

Following these observations, it can be concluded that the optimum value of Gs at normal operating conditions will perform poorly in faulty conditions. Therefore, a method to tune Gs for the faulty switches that will eventually yield acceptable results has to be suggested. This will be discussed thoroughly in the next Chapter.

4.5 Conclusion

The main objective of this Chapter was to assess the performance of the eHS inverters when operated with unbalanced loads, below rated conditions and with faults introduced to the inverters. Results from offline and real-time simulations showed that, with LCA activated, the inverters performed as expected when operated at below rated conditions and with unbalanced loads. However, in faulty situations, there were considerable inaccuracies in the results even when LCA was activated.

In the following Chapter, the values of Gs are re-tuned to observe whether the results will improve with faults provoked. Also, a mathematical approach is followed to analyze the performance of the inverter in inductive and resistive load cases. Moreover, several enhancements, related to selecting Gs, are proposed.

5. PERFORMANCE ANALYSIS AND ENHANCEMENT OF POWER CONVERTERS WITH PEJOVIC SWITCH MODEL

5.1 Introduction

In this Chapter, the several remarks that were raised previously at the end of the Chapter 2 will be revisited and addressed. The Pejovic Switch Model is analyzed mathematically to understand the presence of overshoots in the line voltages. Also, the effect of adding a dead-time with the Pejovic Switch Model is studied. Finally, a set of recommendations on the below issues are proposed to assist the users of such application to obtain better results:

- A modified switch model to damp oscillations in case LCA is not activated
- A simple way to select Gs for resistive loads
- Improved value of Gs with minor effects on efficiency
- Selecting Gs for faulty switches to obtain acceptable results

5.2 Mathematical Analysis of Pejovic Switch Model

The behavior of the commutation of ideal switches in one arm of a two-level inverter is considered in this section. The load is assumed highly inductive such that the load current does not change much during one commutation. Therefore, it can be replaced by a constant current source. This situation is illustrated in Figure 5.1 in which the DC voltage is assumed to be 10V, and the load current is 2A.

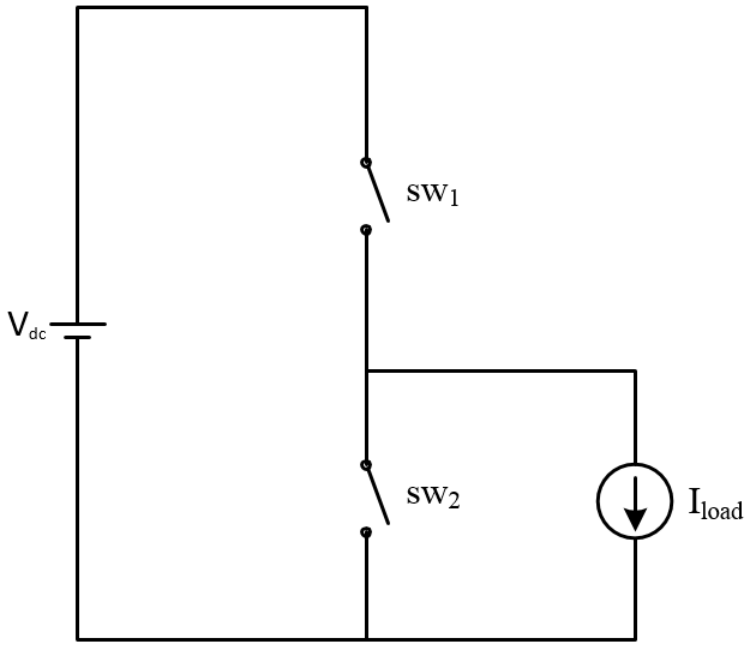

Figure 5.1 One arm of two level inverter

5.2.1 sw1 ON, sw2 OFF

It is assumed that sw1 has been OFF for a long time, and sw2 has been ON for a long time such that the switch voltages and currents have reached their steady-state values. The change takes place at the next interval such that sw1 turns ON and sw2 turns OFF. At this stage, the effect of dead-time is neglected. Figure 5.2 shows the converter circuit with the Pejovic Switch Model. In all cases, the circuit configuration will not change. It is just the expression for the parallel current source that will change depending on the state of the switch.

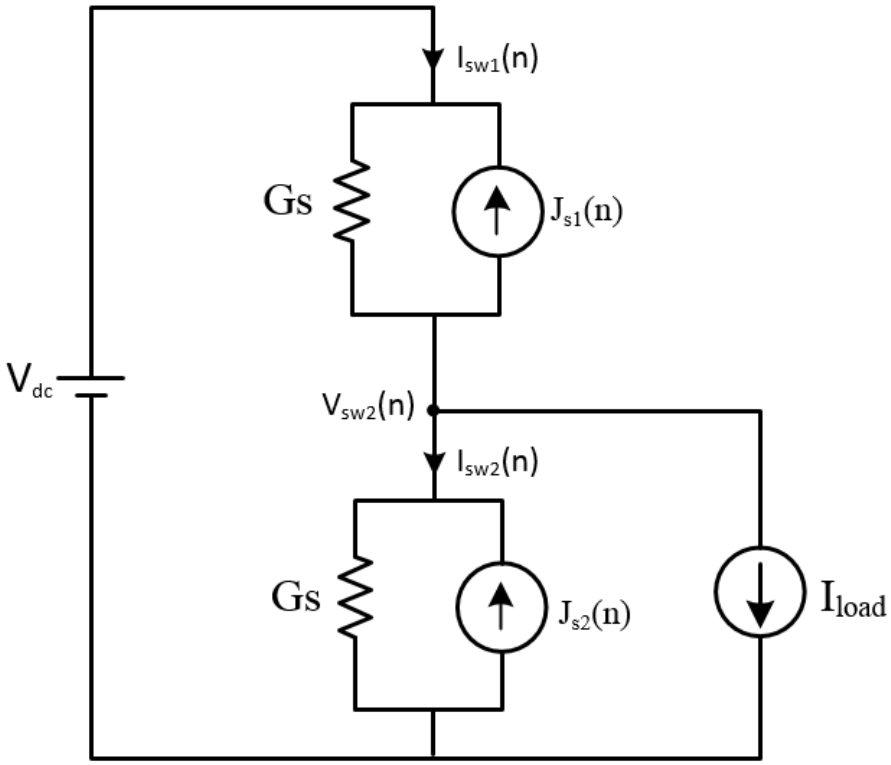

Figure 5.2 Converter circuit with Pejovic Switch Model

Since sw_1 is ON and sw_2 is OFF, the expressions for J_{s1} and J_{s2} are as follows:

- $Js1(n) = -Isw1(n-1)$ (5.1)
- $Js2(n) = GsVsw2(n-1)$ (5.2)

Performing the nodal analysis at V_{sw2}:

$$GsVsw2(n) - GsVsw2(n-1) + Gs(Vsw2(n) - Vdc) - Isw1(n-1) + Iload = 0 \quad (5.3)$$

$$2GsVsw2(n) = GsVsw2(n-1) + GsVdc + Isw1(n-1) - Iload \quad (5.4)$$

The expression for the voltage of the bottom switch is:

$$Vsw2(n) = \frac{1}{2}Vsw2(n-1) + \frac{1}{2Gs}Isw1(n-1) + \frac{1}{2}(Vdc - \frac{Iload}{Gs}) \quad (5.5)$$

The top switch voltage can now be easily expressed as:

$$Vsw1(n) = Vdc - Vsw2(n) \quad (5.6)$$

For the switch currents, either one of the switches can be considered to derive an expression. If the top switch is considered, the switch current can then be expressed as:

$$Isw1(n) = GsVsw1(n) + Isw1(n-1) \quad (5.7)$$

Thereafter, the bottom switch current can be expressed as:

$$Isw2(n) = Isw1(n) - Iload \quad (5.8)$$

The solutions to the difference equations (5.5) to (5.8) can be easily obtained by computing these expressions directly in Matlab. The initial conditions and the switch conductance (Gs) need to be specified to start the iterations. Figure 5.3 shows the switch voltages and Figure 5.4 shows the switch currents after the changes to the switch states happen. Gs is selected as 0.2 and the solution is plotted for 30 iterations.

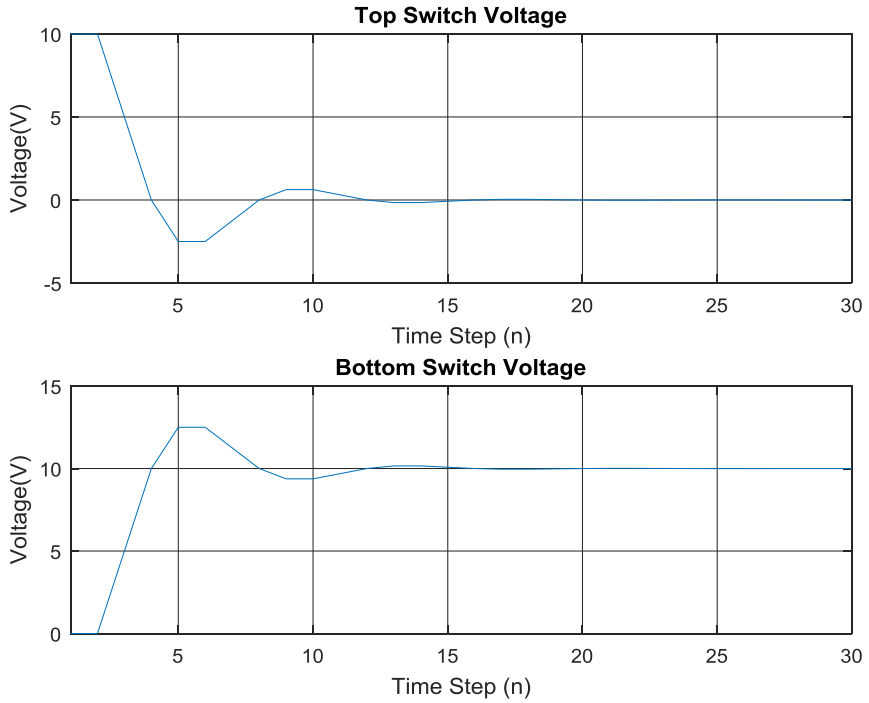

Figure 5.3 Graphical solution of switch voltages

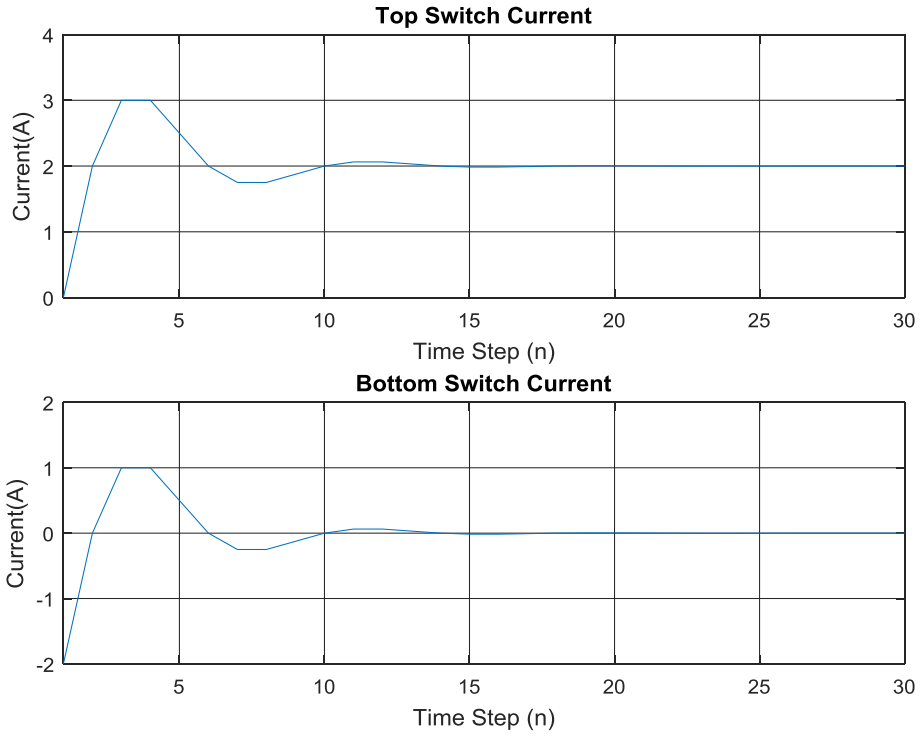

Figure 5.4 Graphical solution of switch currents

5.2.2 sw_1 ON, sw_2 OFF (Resistive Load)

In this subsection, the behavior of the switch voltages and currents when the inductive load is replaced by a purely resistive load is investigated. The expressions for J_{s1} and J_{s2} will not change, and the load is assumed to be 5Ω.

Performing the nodal analysis at V_{sw2}:

$$GsVsw2(n) - GsVsw2(n-1) + Gs(Vsw2(n) - Vdc) - Isw1(n-1) + \frac{1}{R}Vsw2(n) = 0 \tag{5.9}$$

$$(2Gs + \frac{1}{R})Vsw2(n) = GsVsw2(n-1) + GsVdc + Isw1(n-1) \tag{5.10}$$

The expression for the voltage of the bottom switch is:

$$Vsw2(n) = \frac{1}{2Gs + \frac{1}{R}}(GsVsw2(n-1) + Isw1(n-1) + GsVdc) \tag{5.11}$$

The bottom switch current can be expressed as:

$$Isw2(n) = Isw1(n) - \frac{1}{R}Vsw2(n) \tag{5.12}$$

The voltage and current equations for the top switch are the same as (5.6) and (5.7). Figure 5.5 and Figure 5.6 illustrate the solutions when the load is resistive.

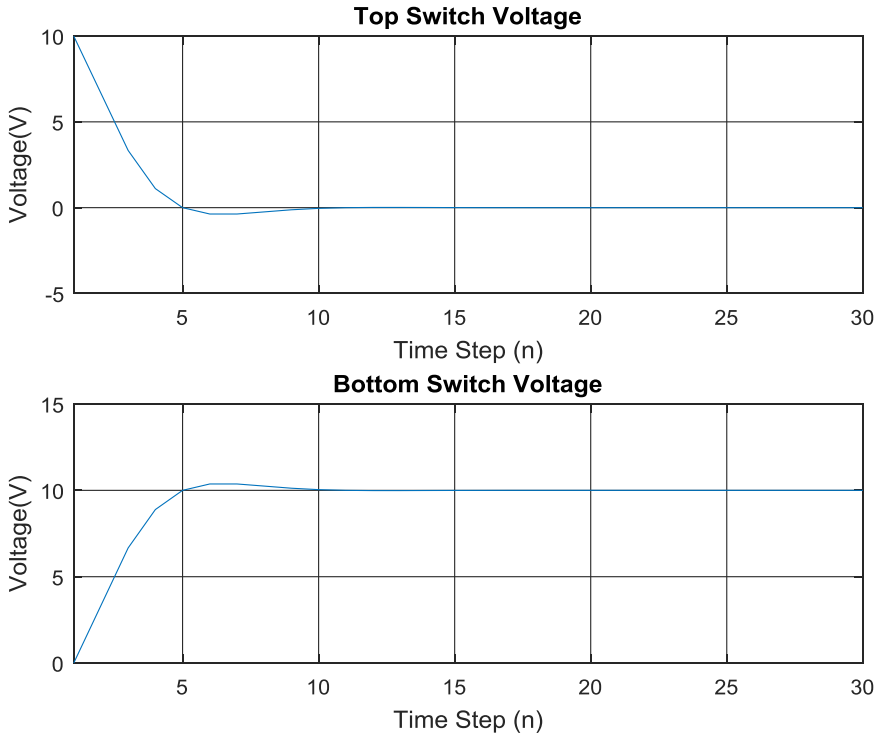

Figure 5.5 Graphical solution of switch voltages with resistive load

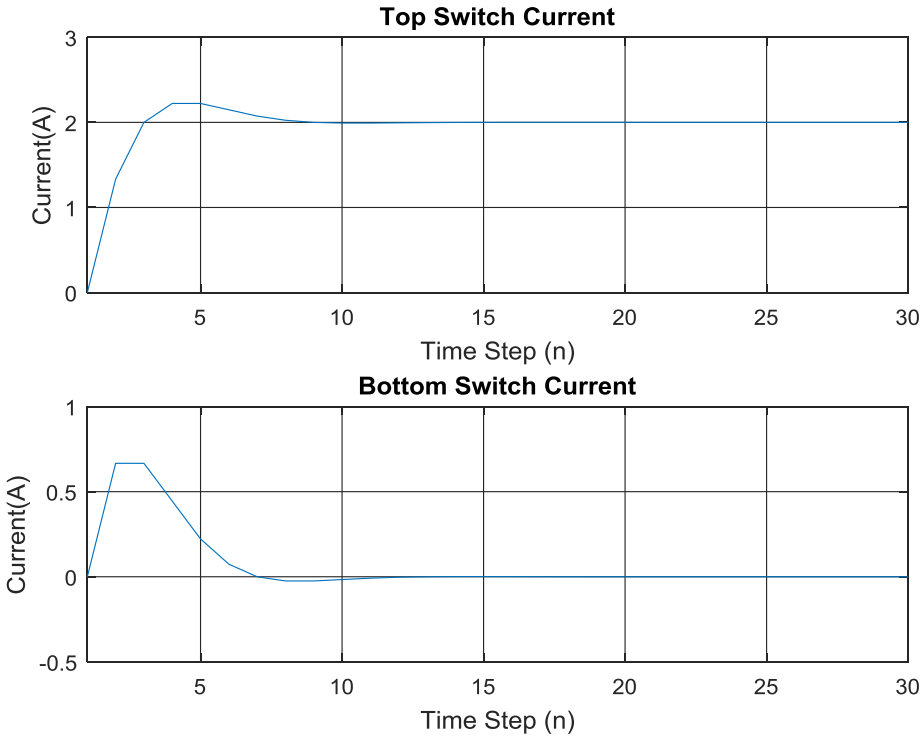

Figure 5.6 Graphical solution of switch currents with resistive load

5.2.3 Discussion of results

The results obtained in the previous two subsections coincide well with the observations from the validation stage outlined in Chapters 2 and 3. The observations include large overshoots in the line voltages with inductive loads which drastically diminished with resistive loads. The same exact behavior can be observed when looking at Figure 5.3 and Figure 5.5. In Figure 5.3, a large overshoot can be seen in the switch voltages, which are directly reflected on the output. In Figure 5.5, where the load is resistive, the overshoot is too small and the switch voltages almost have a critically damped response.

To understand the reasons causing these overshoots in the inductive load case, the analytical solution of the bottom switch voltage is required. By taking the Z-transform of equations (5.5) to (5.7) and re-arranging to make the bottom switch voltage the subject, equation (5.13) is attained:

$$Vsw2(z) = \frac{5z}{(z-1)(z^2 - z + \frac{1}{2})} \tag{5.13}$$

By using the partial fraction expansion and then the inverse Z-transform, the solution to the bottom switch voltage can be expressed as:

$$vsw2(n+1) = 10 - 10\left(\frac{\sqrt{2}}{2}\right)^n \cos(\frac{\pi}{4}n) \tag{5.14}$$

The solution is composed of two parts: the DC bus voltage plus an oscillatory, erroneous term. The presence of the cosine function is what causes the overshoots and oscillations in the switch voltage. The Cosine function is multiplied by a damping function, otherwise the switch voltage would have kept oscillating infinitely. However, the damping factor is not large enough to suppress these oscillations and diminish their presence in the output voltage.

Conversely, the oscillations were barely visible in the resistive load case. The solution of the bottom switch voltage is required again to understand the reason. Taking the Z-transform and rearranging equation (5.11) results in the following expression for the bottom switch voltage:

$$Vsw2(z) = \frac{\frac{10}{3}z^2}{(z-1)(z^2 - z + \frac{1}{3})} \tag{5.15}$$

The solution of the bottom switch voltage is therefore:

$$vsw2(n+1) = 10 - \frac{20}{3}\left(\frac{\sqrt{3}}{3}\right)^n \cos(\frac{\pi}{6}n) \tag{5.16}$$

If equations (5.14) and (5.16) are compared, the first thing that can be observed is that the damping functions of the switch voltages are different. The damping effect in the resistive load is greater than in the inductive load case. Figure 5.7 shows the plots of the two damping functions. It can be clearly seen that the second damping function, corresponding to the resistive load, decays towards zero faster than the other one. In addition to the greater damping effect, the amplitude of the cosine function with the resistive load (6.67V) is smaller than in the inductive load expression (10V). These two factors combined are the causes of having minimal oscillations in the switch voltage in the resistive load case.

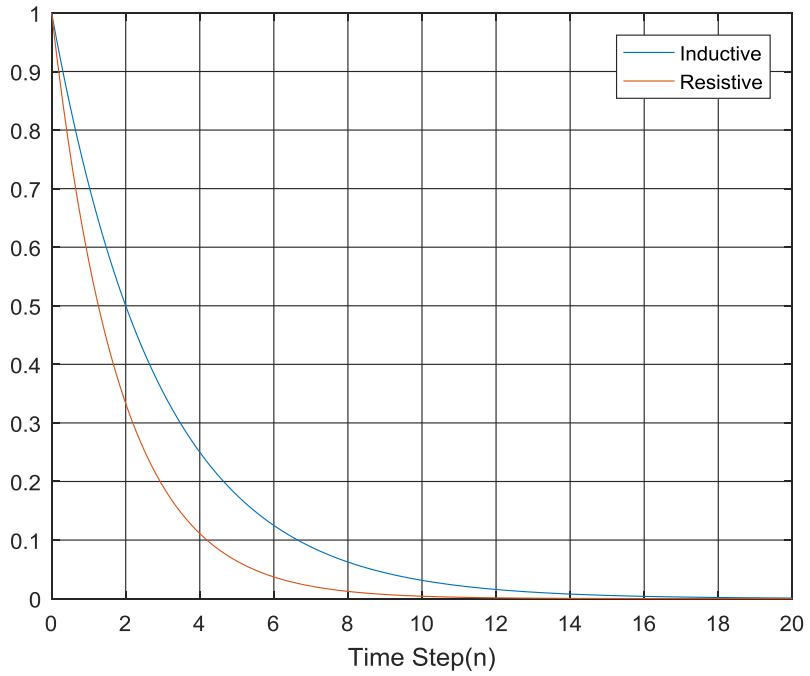

Figure 5.7 Damping functions

The frequency of the Cosine functions is another remark to consider. The frequency of the Cosine function in the inductive load expression $(\frac{\pi}{4})$ is higher than that in the resistive load expression $(\frac{\pi}{6})$. Both the rise and peak time are inversely proportional to the natural frequency of the system and directly proportional to the damping factor. Accordingly, this results in a low rise and peak time in the switch voltage response with the inductive load as the frequency is higher and the damping factor is lower compared to the resistive load case. This can be clearly seen by referring to the switch voltage response in Figure 5.3 and Figure 5.5, where the switch voltage response at the beginning is faster in Figure 5.3, the inductive load case.

5.3 Effect of dead-time on Pejovic Switch Model

In this Section, the effect of adding dead-time to the switch commutation is studied with the Pejovic Switch Model. The assumption now is that sw_1 changes from ON-OFF, and sw_2 changes from OFF-ON. When sw_1 is turned OFF, sw_2 stays OFF for the period of the dead-time. Therefore, the expressions for J_{s1} and J_{s2} are as follows:

- $Js1(n) = GsVsw1(n-1)$ (5.17)
- $Js2(n) = GsVsw2(n-1)$ (5.18)

Following the procedure in the previous Section, one can get the following expression at V_{sw2}:

$$-GsVsw1(n) + GsVsw2(n) + GsVsw1(n-1) - GsVsw2(n-1) + Iload = 0 \quad (5.19)$$

$$Vsw2(n) = Vsw1(n) - Vsw1(n-1) + Vsw2(n-1) - \frac{Iload}{Gs} \quad (5.20)$$

The top switch voltage can be simply expressed as:

$$Vsw1(n) = Vdc - Vsw2(n) \quad (5.21)$$

Substituting (5.21) into (5.20), V_{sw2} can be re-written as:

$$Vsw2(n) = Vdc - Vsw2(n) - \big(Vdc - Vsw2(n-1)\big) + Vsw2(n-1) - \frac{Iload}{Gs} \quad (5.22)$$

This substitution finally yields:

$$Vsw2(n) = Vsw2(n-1) - \frac{Iload}{2Gs} \quad (5.23)$$

Expression (5.21) can be re-written as:

$$Vsw2(n) = Vdc - Vsw1(n) \quad (5.24)$$

Substituting (5.24) into (5.23) yields:

$$Vsw1(n) = Vsw1(n-1) + \frac{Iload}{2Gs} \tag{5.25}$$

The top switch current can be expressed as:

$$Isw1(n) = Gs(Vsw1(n) - Vsw1(n-1)) \tag{5.26}$$

Substituting (5.25) into (5.26) returns:

$$Isw1(n) = Gs(Vsw1(n-1) + \frac{Iload}{2Gs} - Vsw1(n-1)) \tag{5.27}$$

Then, I_{sw1} can be expressed as:

$$Isw1(n) = \frac{Iload}{2} \tag{5.28}$$

Thereafter, I_{sw2} is simply:

$$Isw2(n) = -\frac{Iload}{2} \tag{5.29}$$

Equations (5.23), (5.25), (5.28) (5.29) describe the behavior of the switches during dead-time. There is a major problem in the expressions of the switch voltages. Instead of each switch having a constant, equal share of the DC bus voltage, the top switch voltage is increasing by $Iload/2Gs$ and the bottom switch voltage is decreasing by the same value every step. This results in distortions in the switch voltages and can affect the results of the converter. However, from Chapters 1 and 2, this problem was not encountered in the line voltages. This is because OPAL RT have designed a solution for this problem and the linear change in the switch voltages is avoided. The inverter outputs with the Pejovic Switch were computed manually by the modified nodal approach using Matlab. In this method, the effect of dead-time was not handled as in eHS. Figure 5.8 shows the line voltage from eHS, SPS and the manual computation of the inverter

outputs. The linear decrease in the voltage from the manual computation during the dead-time is clearly visible in Figure 5.8, whereas the voltage from eHS follows the voltage from SPS. Also, RMS values of voltages and currents with the untreated dead-time effect are significantly erroneous, as shown in Table 5-1. This is one benefit of using OPAL RT system that the user need not to concern about obtaining wrong outputs when adding dead-time.

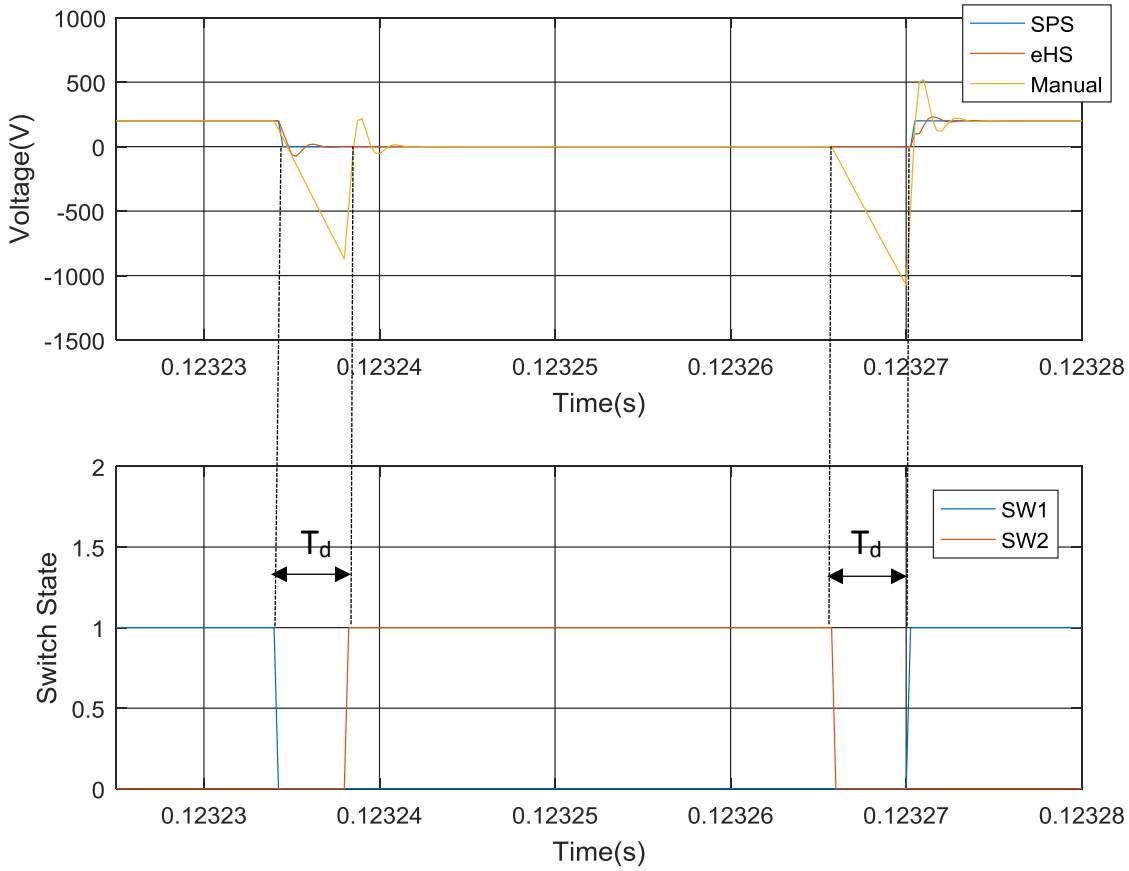

Figure 5.8 Effect of dead-time on line voltage with Pejovic Switch Model

Table 5-1 RMS voltages and currents with dead-time effect

	V_{LL} (V)	I_a (A)
SPS	128.70	1.974
eHS	128.41	1.964
Manual Computation	212.74	1.294

5.4 Damping the numerical oscillations by modifying the Pejovic Switch

The numerical oscillations in the switch voltages can be damped by applying the trapezoidal with numerical stabilizer integration method to the inductor and capacitor equations [19]. "Alpha" is a unitless parameter that controls the degree of damping.

ON Switch:

The ON switch is represented by an inductor, so the discrete-time expression of the inductor current is given by:

$$i_L(n) = i_L(n-1) + \frac{T}{2}\left[(1+\propto)\frac{1}{L}v_L(n) + (1-\propto)\frac{1}{L}v_L(n-1)\right] \tag{5.30}$$

By letting $G_L = \frac{T(1+\propto)}{2L}$, equation (5.30) can be re-written as:

$$i_L(n) = G_L V_L(n) - j_L(n) \tag{5.31}$$

Where $j_L(n)$ is the current source expression, and is given by:

$$j_L(n) = -\frac{T}{2L}(1-\propto)V_L(n-1) - i(n-1) \tag{5.32}$$

Since $\frac{T}{2L} = \frac{G_L}{1+\propto}$, the current source expression can be written as:

$$j_L(n) = -G_L\frac{(1-\propto)}{(1+\propto)}V_L(n-1) - i(n-1) \tag{5.33}$$

OFF Switch:

The exact same procedure can be applied to the capacitor voltage to obtain the current source expression for the OFF switch. This expression is given by:

$$jc(n) = GcVc(n-1) + \frac{1-\propto}{1+\propto}i(n-1) \tag{5.34}$$

To maintain a fixed admittance matrix, G_L and Gc must be equal. Therefore, both can be expressed as Gs. Gs can still be selected according to equation (1.9). The value of "alpha" can be varied to control the damping effect. If equation (5.32) and equation (5.34) are examined carefully,

substituting a value of 1 for “alpha” will result in the Pejovic switch. A value of 0 will result in entirely oscillating switch voltages. Therefore, “alpha” is increased beyond 1 to damp the oscillations. Figure 5.9 shows the switch voltage with the following “alpha” values: 1,3,5. It can be clearly seen that by increasing alpha, a less oscillatory switch voltage is obtained. However, the settling time of the switch voltage will increase, and this can be critical in high frequency applications where the change in switch voltage from one value to another must be instant.

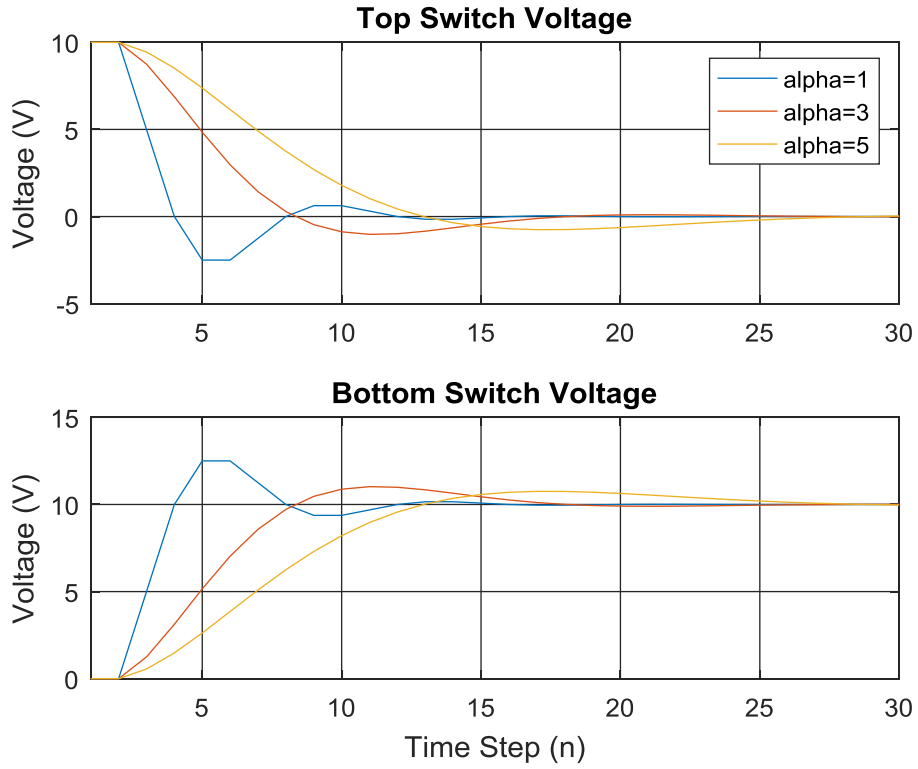

Figure 5.9 Switch voltages with modified switch model

5.5 Selection of Gs for Resistive loads

The OPAL RT script that returns the value of Gs for resistive loads requires the user to enter the base power, DC bus voltage and the nominal duty cycle. However, the user can obtain acceptable results without prior knowledge of the converter outputs by choosing Gs according to equation (5.35).

$$Gs = \frac{1}{R} \tag{5.35}$$

Different cases of load resistance, modulation index, switching frequency and dead-time with Gs selected according to equation (5.35) were simulated and the results are shown in the following Table 5-2 and Table 5-3. Table 5-2 shows the detailed results of the simulation. Table 5-3 shows summarized results of one more load case. With this selection of Gs, there is a close agreement between results from eHS and SPS. The RMS values are almost the same, but the fundamental components are slightly higher with eHS. There is a 0.9% difference in fundamental line voltage and 0.98% in load current, which are clearly very small.

Table 5-2 Results of first load case with Gs=1/R

Vdc=200, ma=0.6, td=2µs, Fpwm=5kHz, R=50Ω, Gs=0.02		
	SPS	**eHS**
V_{LL} fund.(V)	70.699	71.335
V_{phase} fund.(V)	40.813	41.181
I_a fund.(A)	0.816	0.824
V_{LL}(V)	112.059	112.057
V_{phase}(V)	64.692	64.691
I_a(A)	1.294	1.294
I_{dc}(A)	1.262	1.279
THD(V_{LL})	122.974	121.144
THD(V_{phase})	122.983	121.149
THD(I_a)	122.983	121.149
Input Power (W)	252.38	255.81
Output Power (W)	251.10	251.10
Efficiency (%)	99.49	98.16

Table 5-3 Summary of results of second load case with Gs=1/R

Vdc=100, ma=0.8, td=4µs, F_{pwm}=8kHz, R=10Ω, Gs=0.1		
	SPS	**eHS**
V_{LL} (V)	62.94	62.307
I_a (A)	3.597	3.597
Efficiency (%)	99.92	98.23

5.6 Improved value of Gs with minor effects on efficiency

In Chapter 1, it has been explained that selecting a very low value of Gs will result in a low load current, while on the other hand, selecting a very large value of Gs will allow more current to flow. This remark was further reinforced in Section 4.3 when a value of Gs lower than the optimum value was selected, the load current was low compared to the actual current. Conversely, when Gs was higher than the optimum value, the load current was higher than the actual current. Therefore, in this Section, a graphical method is used to show how much Gs can be increased to approach the actual load current while minimally degrading the efficiency.

The converter shown in Figure 5.1 will be revisited to carry out the analysis. In equation (5.5), which describes the behavior of the switch voltage, the only adjustable element is Gs. In other words, the characteristics of the response of the switch voltage is entirely governed by the value of Gs. These characteristics include the percentage overshoot, rise time and settling time. The rise time of the switch voltage gives an indication of the slope of the change in switch voltage. By inspecting the effect of changing Gs on the rise time, a good indication on the change in load current can be implied. There is some kind of correlation between all these parameters since they are all controlled by one variable. Gs will be changed from 0.2 to 1 in incremental steps of 0.1 (50% increase on the original value of Gs) and the switch voltage will be plotted.

Figure 5.10 shows the result of plotting the switch voltage with the various values of Gs. By increasing Gs, it can be seen that the response of the switch voltage becomes faster. It needs 4 time steps for the switch voltage to reach 10V when Gs=0.2, but it needs around 3.3 time steps to reach the same value when Gs=1. Also, it can be noticed that minor changes occur on the time response when Gs is increased beyond 0.5. The considerable changes happen when Gs is increased from 0.2 to 0.5. This observation can be reflected on the load current meaning that the effective increase in current will be observed when Gs is increased by 2.5 times. Increasing Gs beyond that will not result in noticeable changes in the current. The effect of increasing Gs on the efficiency will be investigated next to determine the extent to which Gs can be increased without degrading the overall efficiency.

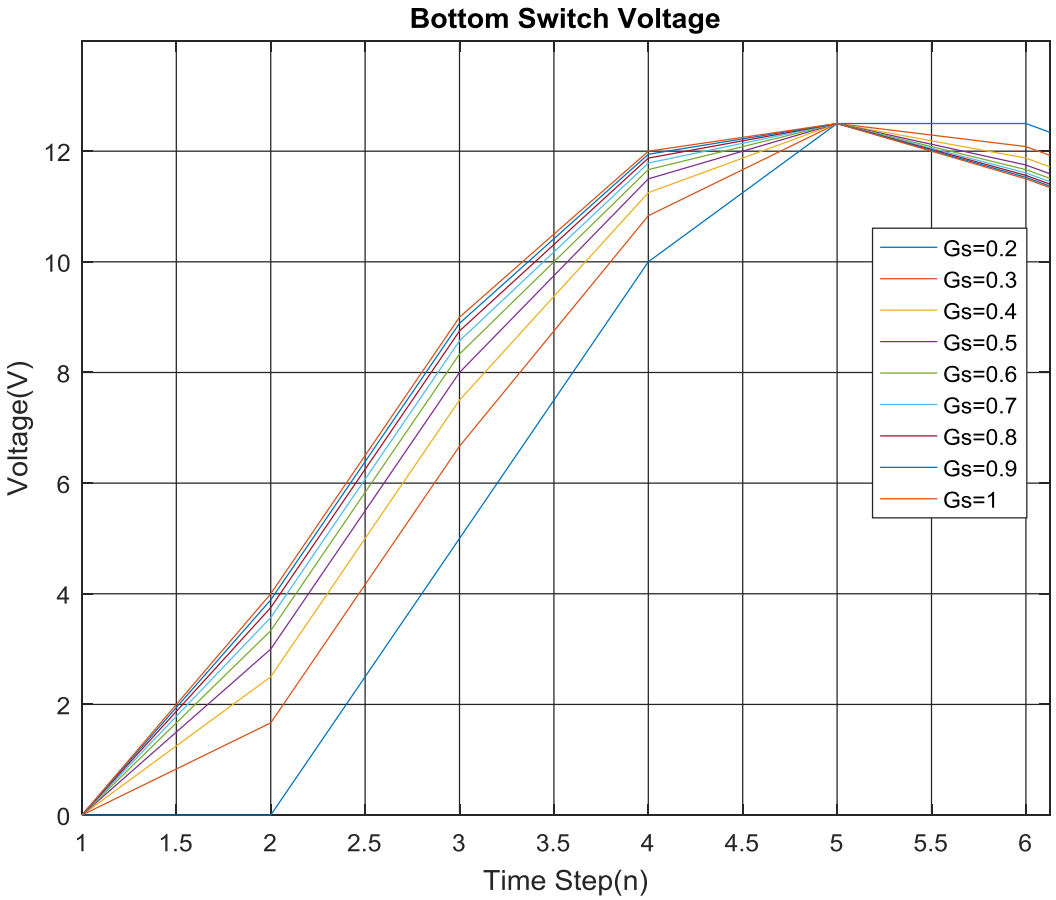

Figure 5.10 Switch voltage with different values of Gs

The expression for the total loss of energy by one switch was stated in the Chapter 1 as:

$$E_{total} = \frac{1}{2} TsGsV^2 + \frac{1}{2}\frac{Ts}{Gs} I^2 \tag{5.36}$$

This expression is used to plot the total energy loss as a function of Gs and then graphically determine the effect of increasing Gs on the efficiency. Assuming that that DC bus voltage is 10V, current is 2A, Gs is 0.2 and the time-step Ts is 250ns, the energy loss curve is as shown in Figure 5.11.

First, it can be realized that the minimum energy loss occurs at Gs=0.2, which corresponds to the value returned by Gs=I/V. If Gs deviates away from this point, the energy loss increases.

The energy loss increases more rapidly if Gs is decreased beyond the optimum value than if increased. At this point, it must be specified how much Gs can be increased without resulting in excessive energy losses. From the graph, by increasing Gs by 50% from 0.2 to 0.3, the energy lost rises by 10% (from 5 to 5.5uJ). Increasing Gs by 100% will result in almost 22% rise in energy loss. A 150% increase in Gs will result in 50% increase in energy loss. Therefore, from this graphical approach, it is recommended to increase Gs by 50% since this will not result in a significant impact on the efficiency. Moreover, increasing Gs by 100% might not be a bad option in some cases, but when doing so, the user has to check the efficiency of the system. To sum up, if the user is to increase Gs, a 50% increase can be a very good choice.

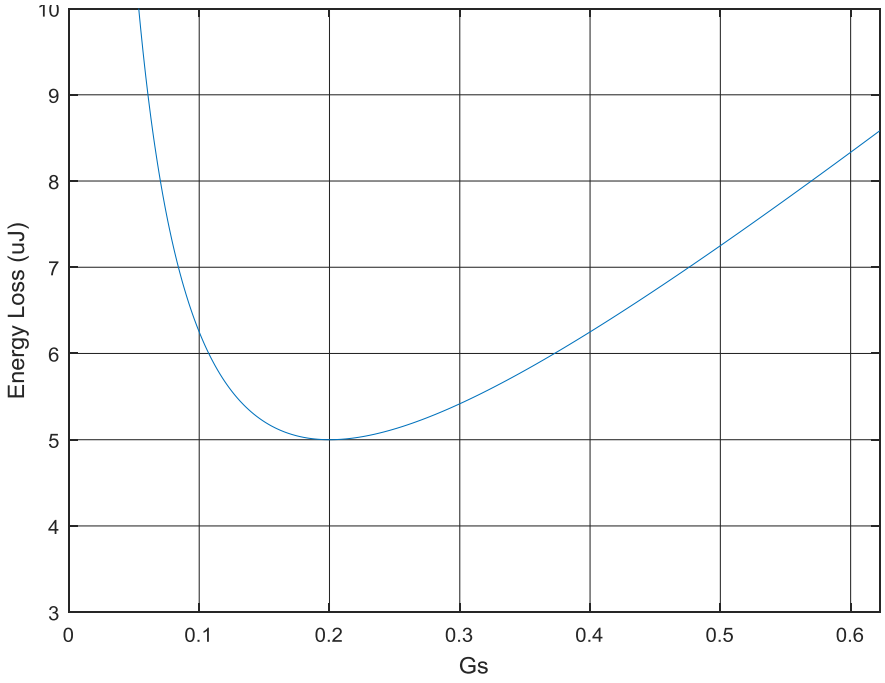

Figure 5.11 Energy loss of one switch as a function of Gs

Table 5-5 summarizes the results of a two-level inverter with Gs increased from its optimum value in steps of 50%. The test conditions are shown in Table 5-4. The actual load current is 2.100A and thus Gs is 0.0105. As Gs is increased, the load current gradually approaches the reference value. The trend in the values of current and efficiency follow the same profile that was discussed earlier via the graphical approach. After increasing Gs by 150%, the percentage increase

in load current due to incrementing Gs by 50% becomes very minor. For example, increasing Gs from 50 to 100% results in a 0.13% increase, while increasing from 300 to 350% results only in a 0.03% rise. As for efficiency, when Gs was increased by 50% from optimum value, a very small drop of 0.16% happened. The percentage drop in efficiency was less than 1% up to 150% increase on optimal Gs. Beyond that, the drop in the efficiency of the inverter becomes considerable. Therefore, as was mentioned earlier, 50% increase on the optimal Gs yielded acceptable results with a sound increase in load current and a minimal drop in efficiency. Additionally, the 100% increase yielded acceptable results with even a better value of load current but with a slightly bigger drop in efficiency. Nevertheless, a 0.47% drop in efficiency can be tolerated in many cases. The line voltage maintained almost a constant value for all cases of Gs.

Table 5-4 Test Conditions

Parameter	Value
DC Bus Voltage	200V
Modulation Index	0.8
Modulating Frequency	50Hz
PWM Frequency	5kHz
On-state Resistance	0Ω
Dead time	0μs
Time Step	250ns
Load	R=25Ω, L=32mH

Table 5-5 Results of two level inverter with Gs increased in steps of 50%

Gs	**% rise in Gs**	**V_{LL}(V)**	**I_a(A)**	**% rise in I_a**	**Efficiency (%)**	**% drop in Efficiency**
0.0105	-	132.998	2.0827	-	98.38	-
0.0158	50	132.948	2.0885	0.28	98.22	0.16
0.0210	100	132.960	2.0913	0.41	97.92	0.47
0.0263	150	132.978	2.0931	0.50	97.55	0.84
0.0315	200	132.995	2.0942	0.55	97.16	1.24
0.0368	250	133.010	2.0951	0.60	96.76	1.65
0.0420	300	133.023	2.0957	0.62	96.34	2.07
0.0473	350	133.033	2.0962	0.65	95.93	2.49
0.0525	400	133.042	2.0966	0.66	95.511	2.92

5.7 Improvement of Performance under Faults

It was shown in Chapter 4 that the eHS solver fails to perform properly with the introduction of faults to the inverter. The fundamental and low order components were acceptable but major problems were faced in the higher order components. This means that when the user wishes to introduce faults to the inverter, it is not possible to use the same value of Gs that is entered in normal operating conditions. Therefore, the next step was to determine a value of Gs, by trial and error, that can render acceptable values in faulty situations. The load used was 3Ω, 500μH which draws 17.72A of current in normal conditions when it is supplied by a 200V DC bus. The optimum value of Gs under normal operating conditions is 0.0886.

Table 5-6 shows how the values of Gs were changed until acceptable results were achieved. The switches were categorized into normal and faulty switches. Switches in one category were given the same value of Gs. The value of Gs for each category was tuned until desired voltage and current values were obtained.

First, when both categories were given the optimal Gs, a large error can be noticed in the line voltage. Next, Gs for the normal switches was kept constant at the optimal value and Gs for the faulty switches was varied. Increasing Gs by almost 10 times to 1 worsened the line voltage. Then Gs was decreased by almost 10 times to 0.01 which slightly reduced the line voltage from 100.802 to 97.228. Decreasing Gs to 0.006 reduced the voltage to 97.0318, but halving this value of Gs made the line voltage increase back again. Therefore, at this point, Gs for the faulty switches was maintained constant at 0.006 and Gs for the normal switches was varied. Reducing Gs to almost half of its value (0.0537) resulted in a drop in voltage from 97.038 to 95.212. Halving Gs again resulted in a further drop in line voltage to 92.984. Finally, Gs was reduced to 0.01 causing the line voltage and load current to approach the reference values provided by SPS.

Table 5-6 Trial and error process to tune Gs in faulty conditions

Gs Normal	Gs Faulty	V_{LL} RMS (V)		I_a RMS (A)	
		SPS	eHS	SPS	eHS
0.0886	0.0886	89.66	100.802	10.73	10.78
0.0886	1	89.66	110.913	10.73	10.988
0.0886	0.01	89.66	97.228	10.73	10.792
0.0886	0.006	89.66	97.0318	10.73	10.83
0.0886	0.003	89.66	97.138	10.73	10.92
0.0537	0.006	89.66	95.212	10.73	10.818
0.027	0.006	89.66	92.984	10.73	10.801
0.010	0.006	89.66	89.71	10.73	10.76

It is a good practice to check that the other phases are also giving acceptable results in faulty situations. Table 5-7 shows the results of the other two phases. There are some problems in the line voltage from phase C in addition to a small current of 0.1A that is flowing in that phase. Since the problem arises in phase C, the switch parameters of that phase can be tuned further to correct the values.

Table 5-7 Results for three phases of the inverter

	V_{LL} RMS (V)			I_a RMS (A)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
SPS	89.66	44.83	44.87	10.73	10.73	0.002
eHS	89.71	46.62	50.10	10.76	10.76	0.10

Table 5-8 shows how the switch conductance of the two faulty switches in phase C were altered until acceptable results were achieved. Gs for the switches of the other two phases were maintained at the values obtained in table 6. Increasing Gs worsens the results as illustrated in the first row. However, by decreasing Gs, the results gradually approach the correct values. By setting Gs to 0.0005 for the switches in the third arm, very close values to the actual ones are obtained for all three phases.

Table 5-8 Tuning Gs for the switches of phase C

Gs (sw_5, sw_2)	V_{LL} RMS (V)			I_a RMS (A)		
	Phase A	**Phase B**	**Phase C**	**Phase A**	**Phase B**	**Phase C**
0.06	91.048	59.09	67.16	10.78	10.77	0.623
0.003	89.51	45.80	48.45	10.76	10.76	0.0623
0.001	89.44	45.27	46.30	10.76	10.76	0.038
0.0005	89.42	45.02	45.40	10.76	10.76	0.018

Figure 5.12 to Figure 5.16 depict the spectral content of the line voltage from SPS against the line voltage of eHS with the tuned values in addition to the line voltage with optimal Gs at the fundamental frequency and at multiples of the switching frequency. It can be noticed that the spectral content of eHS with the tuned Gs (red) is very close to SPS (blue), minimizing the large differences between SPS and eHS with optimal Gs (yellow). Also, the artificial components at odd multiples of the switching frequency have been substantially suppressed. The last point to verify is whether these tuned values of Gs will still render acceptable results in normal operating conditions.

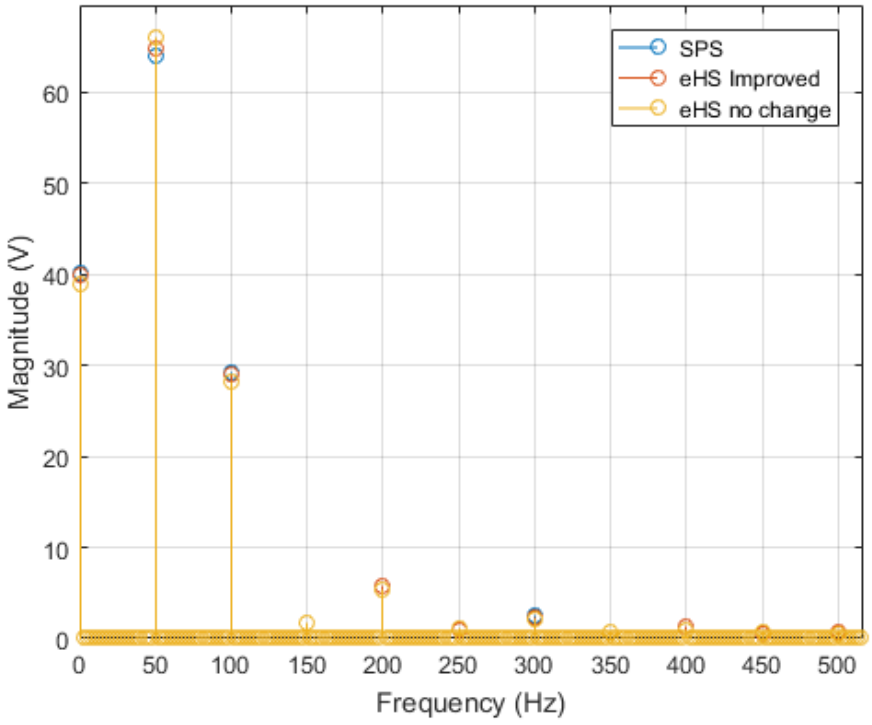

Figure 5.12 Spectral content at fundamental and low order frequencies

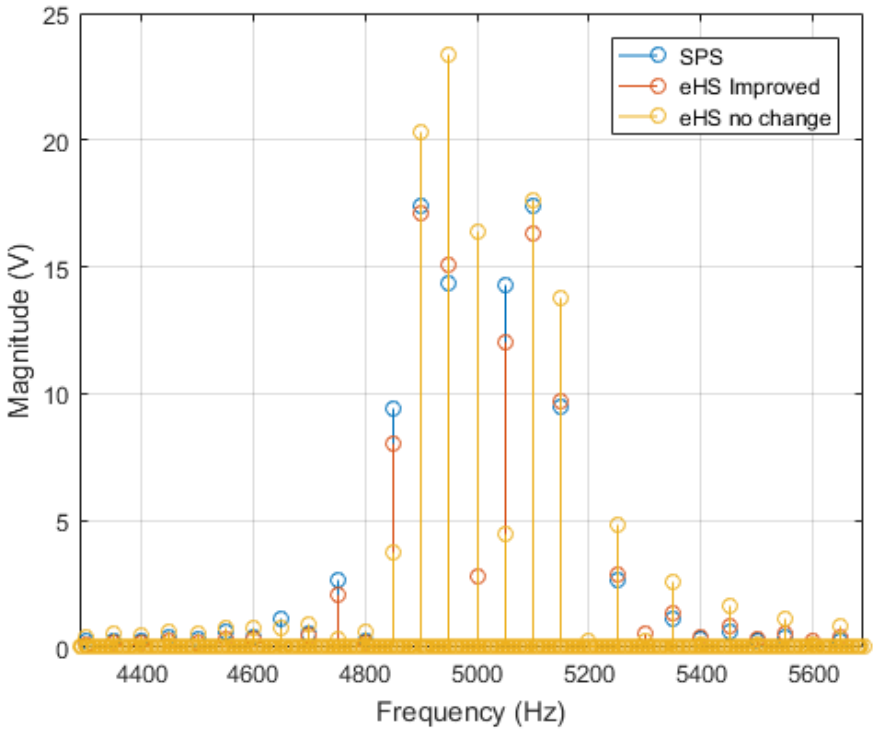

Figure 5.13 Spectral content at and around switching frequency

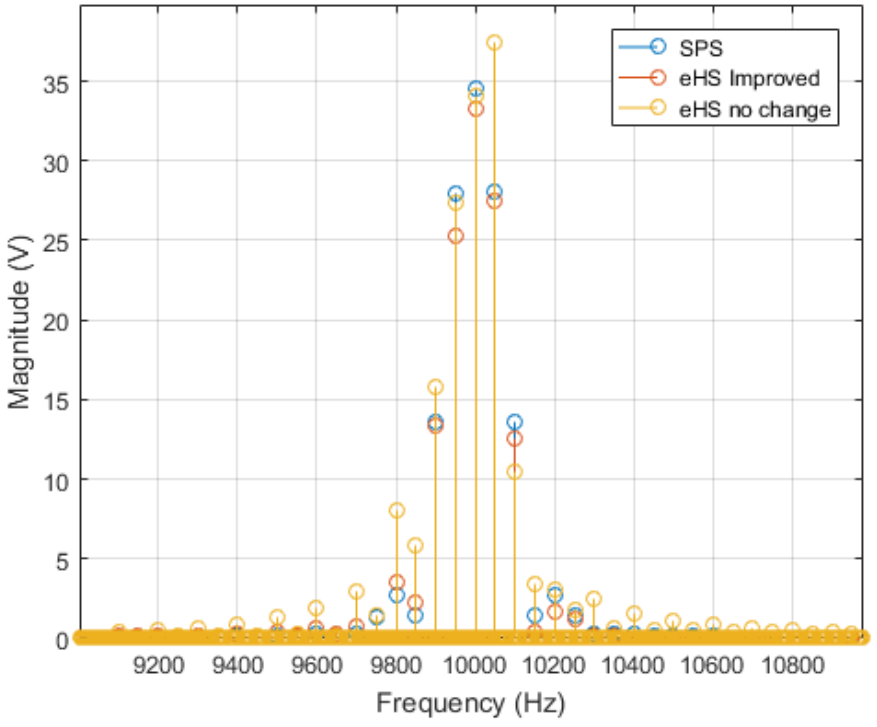

Figure 5.14 Spectral content at and around 2x switching frequency

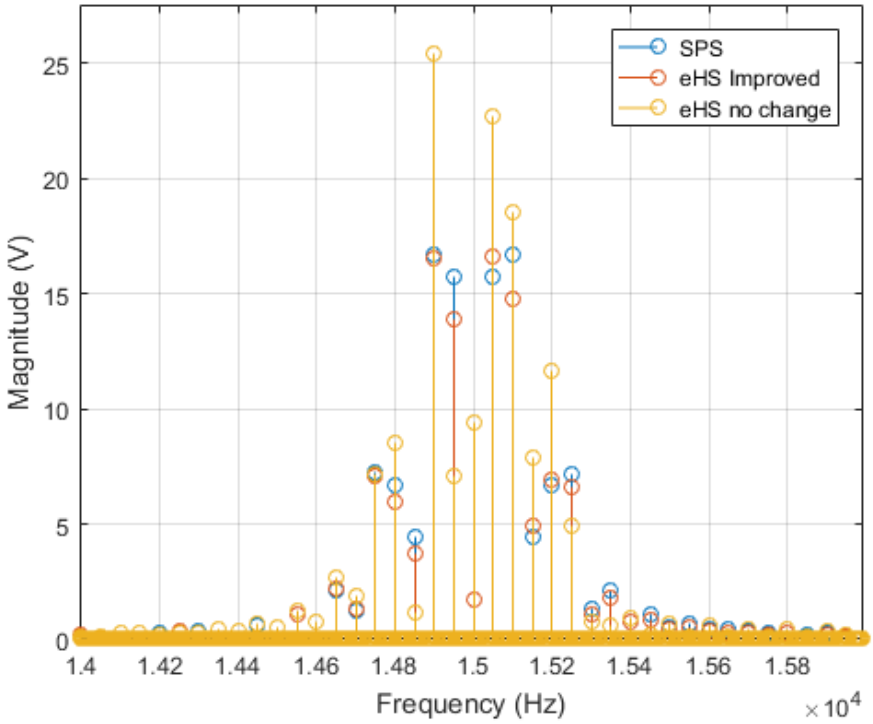

Figure 5.15 Spectral content at and around 3x switching frequency

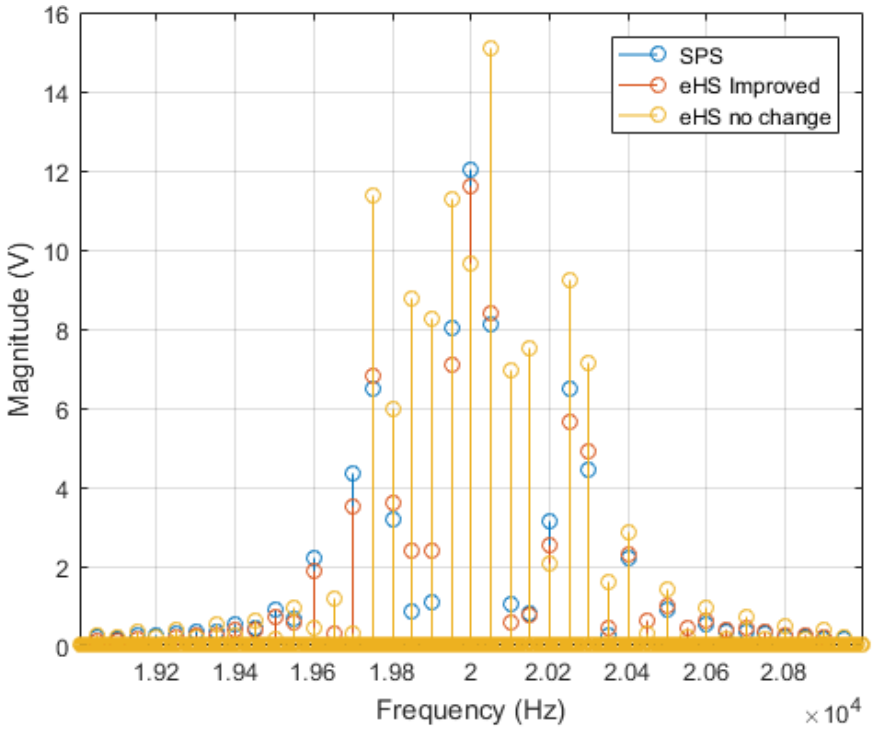

Figure 5.16 Spectral content at and around 4x switching frequency

Table 5-9 shows the results of the simulation when the value of Gs in faulty situations is used for normal operating conditions. The RMS values of the line and phase voltage are lower than the actual values: there is a 2.6% difference in line voltage and 6.8% difference in phase voltage. However, the fundamental components of these voltages are close to the actual values. The defect is, therefore, in the harmonic components of the line and phase voltages. The harmonics are lower than in the actual waveforms, and this was clearly reflected in the corresponding THD. As these harmonic components were naturally filtered out by the inductive load, the fundamental and RMS values of load currents were both close to the reference. Therefore, if the user is to worry only about fundamental components (for example, by adding a filter to extract fundamental quantities), it is acceptable to use the tuned values of Gs for faulty cases whether the faults are introduced or not. Otherwise, it is recommended to use the designated values for each operating condition. The future challenge is to determine a scientific way to obtain these tuned values and without going through trial and error process.

Table 5-9 Inverter results with tuned values of Gs operated in normal conditions

	SPS	**eHS**
V_{LL} fund.(V)	91.753	91.764
V_{phase} fund.(V)	52.976	52.206
I_a fund.(A)	17.634	17.378
V_{LL}(V)	128.690	125.363
V_{phase}(V)	74.306	69.279
I_a(A)	17.721	17.446
I_{dc}(A)	14.135	14.044
THD(V_{LL})	98.346	93.078
THD(V_{phase})	98.358	87.235
THD(I_a)	9.918	8.839
Input Power (W)	2826.93	2808.80
Output Power (W)	2826.28	2739.27
Efficiency (%)	99.98	97.52

5.8 Conclusion

In this chapter, a mathematical approach was followed to analyze the performance of inverters with Pejovic switches. The cause of the oscillation in the line voltages with inductive loads was clearly outline. Moreover, the errors induced by the addition of dead-time with Pejovic switches were pointed out. Selecting Gs as 1/R in case of purely resistive loads was

proven to yield acceptable results. Furthermore, in case of inductive loads, it was shown that increasing by 50% yields improved results with negligible drop in efficiency. This is in case the LCA is not activated. Finally, a set of Gs values for the switches of the two-level inverter, which resulted in acceptable output in faulty cases, was determined.

6. CONCLUSION AND FUTURE WORK

6.1 Summary of the work

In this thesis, the results of an FPGA-based HIL simulation of a two-level inverter using OPAL RT's eHS solver with a time-step of 250ns was validated against a real setup. A new test plan was proposed to ensure a fair comparison between the virtual and real inverter. Previous work involved validating the HIL inverters in offline, but in this work, this step was taken further to validation against a real system.

The results presented in Chapter 3 demonstrate a close proximity between the eHS and real results. This verifies the performance of the eHS solver and the selection of the optimal value of switch conductance (Gs). Moreover, the significance of the loss compensation algorithm was clearly shown. The activation of the LCA eliminated the numerical oscillations and the switching losses introduced by the Pejovic switch. Furthermore, inaccuracies resulting from operating away from the optimal value of Gs (either below or above) were compensated by the LCA. This gives the user the flexibility to simulate the inverter accurately in cases where the load is varying.

The very low time-step that the inverter was simulated at has several benefits. The main one is that the simulation accuracy can be increased, and the PWM signals are sampled with a much higher resolution. With such low time-steps, even the dead-time can be accurately represented. When the dead-time is 4us and the time-step is 10us, the dead-time duration will not be precisely represented because the time-step is much longer than the dead-time. However, at 250ns, the dead-time duration will be sampled accurately since the time-step is shorter than the dead-time.

Several tips were given to the user of this system when selecting Gs. In resistive load cases, a very simple expression was suggested that facilitates to the user the selection of Gs. This selection was tested in various conditions and the results were acceptable. Also, it was explained that increasing Gs by 50% from the optimal value improves the accuracy of the results with minor effects on efficiency in inductive load cases.

The HIL inverters were tested further in faulty situations by blocking some of the switches. The inverter failed to work properly with the optimal value of Gs. Therefore, new values of Gs

were tuned for the working and faulty switches through trial and error. The inverter returned acceptable results with the new values. When these values were used in normal conditions, the results were acceptable but not as satisfying as with the optimal Gs. Nevertheless, it was possible to arrive at a set of values of Gs that can produce acceptable results in each situation.

6.2 Contributions of this work

1. The proposal of a test procedure to validate the real-time model of a two-level inverter against a real inverter. The novelty of this contribution is the involvement of real hardware in the validation process given that all previous validation work was done in offline using reliable software such Simulink.
2. The identification of a scenario in which optimized Gs in combination with the LCA do not achieve expected results. Previous work was always focused on enhancing the accuracy of the real-time models in case of normal operation. A further step was taken in this work to identify the scenario which results in considerable inaccuracies, namely invoking faults on the inverter. Furthermore, the fault case presented in this work is one which truly results in large differences between actual and expected results. Other fault conditions might not have such a severe effect.
3. The attainment of a set of values of Gs capable of producing acceptable results in presence and absence of faults. The procedure to obtain these values was described in the thesis.
4. The proposal of a simple expression to select optimal Gs in case of resistive loads. Since it only depends on the per phase load resistance, the user does not need to know the inverter outcomes to select Gs. Moreover, this expression is independent of any factor such as DC bus voltage, modulation index, switching frequency, dead-time etc. This means that the value of Gs selected accordingly is robust to any changes in the test parameters. Several methods are provided to tune Gs to achieve acceptable results, but this expression is stated for the first time.

6.3 Future Work

1. In this work, the real-time two-level inverter models were validated in open-loop. A potential expansion is to verify the proximity of these models to a real system in closed-loop. An interesting application is the active rectifier, where the two-level converter is controlled to draw sinusoidal currents from the grid in addition to regulating the DC bus voltage.
2. The proposed test plan was implemented for a two-level inverter only. This test plan can now be extended to other advanced power converters such as the three-level NPC inverters.
3. Despite that the procedure followed to tune Gs in case of faults is clear and simple, it can be time-consuming especially if the number of switches in the converter is large. Therefore, the finding in this work is a good starting point that can be extended to determine a systematic method to tune Gs in faulty situations.
4. Due to the asynchronous communication between the real-time simulator and the PC, observing fast-changing signals accurately on the scope of the Console subsystem is not possible. This dictates the need of a real oscilloscope to observe the results accurately. Therefore, a further enhancement can be the implementation of a virtual oscilloscope that can emulate a real oscilloscope and thus, eliminate the need of the real, expensive one.

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