Validation and Enhancement of a Three-level Inverter for Applications in Real-time Simulations

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ABSTRACT

The motivation of this thesis is to perform a hardware validation of a three-level inverter in real-time simulation. Real-time simulators enable faster design and prototyping of controllers without the need of building hardware based test benches. But, it is also essential that the virtual models behave the way they were supposed to, and produce equivalent output as the physical setups. Power electronic systems often have very fast switching devices, which are an inhibiting factor for real-time simulation, as the simulator must have the capability to produce high resolution samples of the gate pulses of these fast acting devices. A virtual model for the three-level inverter is available already for real-time simulation. This model had been tested with the outcome of other non-real-time solvers such as the one from Simscape Power System's Simulink, but not alongside with a physical inverter. Hence, a physical inverter was operated along with its virtual model in a real-time simulator to verify the model.

Real-time simulators use different approaches to model power electronic systems and also make them suitable for such simulations. One such approach is to solve for the nodal voltages and currents using fixed admittance matrices derived from the network. This fixed matrix contains a switch conductance parameter derived from a discrete time model of an ideal switch. The choice of this parameter is very crucial in determining the accuracy of the real-time simulations. A number of ways are used to optimize this parameter, but optimizing a proper value is always a challenge.

This work is dedicated to my father…

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LIST OF ACRONYMS

KVL	Kirchhoff's Voltage Law
KCL	Kirchhoff's Current Law
AC	Alternating Current
DC	Direct Current
PF	Power Factor
RMS	Root mean square
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse width modulation
MNA	Modified Nodal Analysis
FAMNM	Fixed Admittance Modified Nodal Analysis Method
RTS	Real-time Simulation
CPU	Central Processing Unit
FPGA	Field-Programmable Gate Array
DAC	Digital to Analogue Converter
I/O	Input/output
RCP	Rapid Control Prototyping
HIL	Hardware in the Loop
SIL	Software in the Loop
PHIL	Power Hardware in the Loop

DSP	Digital Signal Processor
SPS	Simscape Power Systems
eHS	Electric Hardware Solver
MLI	Multilevel Inverter
RTE	Real-time Events
NPC	Neutral Point Clamped
3 L NPC	Three-level Neutral Point Clamped
IGBT	Insulated Gate Bipolar Transistor
HMI	Human Machine Interface

INTRODUCTION

The real-time simulation of power electronic systems provides a lot of flexibility in the design and testing process. It also does not require a physical test bench to finalize the design; this can lead to a great reduction in the designing and testing costs. Moreover, the same real-time simulator can be used for the realization of converters with multiple topologies; the tests are repeatable without loss of credibility in the results, as the behavior of the simulator does not change with repetition. The real-time simulations of power electronic converters have some challenges and the primary one being the high switching frequency of the devices. The high switching frequency requires the use of very low sampling times (in the order of nanoseconds) to provide high resolution samples of the switching pulses.

The discrete switch model and the usage of a fixed admittance matrix proposed by Pejovic and Maksimovic in 1994, allows the solution of the system equations within the small time step. The switch conductance parameter, G_s used in the discrete switch model remains constant during a simulation but, it is critical to obtain an optimized value before the start of the simulation. An improper G_s would lead to inaccurate simulation results, moreover, this parameter can be dependent upon other factors such as the topology of the converter, connected load etc. which makes the synthesis of an optimized G_s even more difficult. And although optimization tools such as GsGui2 are available for selecting G_s some scenarios may still need the manual tuning of this parameter. GsGui2 is tool that provides a good-enough value of G_s based on converter's ratings and topology. It is available in the eFPGAsim installer. A two-level inverter had been validated successfully against a physical setup in an earlier work. However, in the presence of faults the G_s values from GsGui2 along with the Loss Compensation Algorithm (LCA) did not work properly, which prompted the use of trial and error methodology to find proper G_s values. In this thesis, interpretations from the two-level inverter shall be generalized to a three-level inverter and an optimization technique using eigenvalues shall also be explored. This thesis has been divided into six chapters, the first chapter carries out a literature review about trends in real-time simulation, and it also provides an insight to the related work done and provides a glimpse of the work that shall be done in this thesis. The second chapter introduces the switch model that will be used in this work along with the benefits and drawbacks. The third chapter describes the

validation of a three-level inverter in real-time simulation with a physical converter. Chapter four describes methodologies to optimize the critical switch conductance parameter and to enable real-time simulation of circuits with faulty conditions. Chapter five analyses the three-level inverter using the offline simulation block of eHS. Chapter six is the conclusion of the thesis and states the future work that may be done in its continuation.

Chapter 1. Literature Review

1.1 Simulation of power electronic circuits

To simulate a power electronic circuit or any electrical circuit, there are a few procedures that are required to be followed. At first, a mathematical model of the circuit under test is built, and then solvers are chosen to solve those equations [1]. After a proper model is chosen, the mathematical equations for the model can be developed by using either Maxwell's cyclic current, widely known as Kirchhoff's Voltage Law (KVL), nodal analysis or Kirchhoff's Current Law (KCL) or the relatively newer approach called Modified Nodal Analysis (MNA) [2]. Nodal analysis had some advantages over mesh analysis, one being reduced number of equations compared to mesh analysis. But there were difficulties in the use of the classical nodal analysis, particularly in computer simulation; certain elements such as voltage sources, dependent sources, transformers etc. could not be included in the analysis unless some conversion was done to some extent, but on conversion, there was always loss of information about the model [3]. MNA was proposed by Chung-Wen Ho in 1975, to resolve the limitations of the classical nodal analysis. MNA can considerably reduce computation time for solving the network matrices and is easier to implement on a computer, thus making it more suitable for simulation of electrical circuits. Real-time Simulation (RTS) of power electronic circuits demand even faster computation and a slightly different version of MNA called the Fixed Admittance Modified Nodal Analysis Method (FAMNM) [4]-[6] came into use. This method allowed the system equations to be solved in very small time steps as required by RTS of fast switching power electronic converters.

1.2 Real-time Simulation

A real-time simulation is a type of computer simulation, where a computer model runs at the same pace and produces similar output as the physical system it represents. The virtual representation of physical system i.e. a virtual model runs at the same speed, and for the same time as the physical system. They may share common input variables and come out with comparable output. One good example for a RTS can be operation of the Fuel Injection System of a modern day computer controlled car engine, the onboard computer (Engine Control Unit) calculates the duration of operation and the interval between each operation based upon the

throttle input, camshaft position, dwell time, inputs from Oxygen Sensors, inputs from NOx sensors etc. all of which are measured in real-time.

A computer does all the computations using an operating system which eventually does all of its calculations in the form of 0's and 1's. All the differential equations, state equations or any mathematical functions representing a physical system will converted to a discrete system of 0's and 1's; these will be solved by the computer simulation software using their own solvers. The solvers use different numerical methods to do the computations and each may take different amount of time and produce results with different accuracy.

To work with RTS, the simulation associated would be for discrete time with a constant step size. Variable time-step simulation is not suitable for RTS and hence the time is incremented in equal step sizes called *Simulation Time Steps* and the simulation itself is often called *Fixed Time Simulation.*

As mentioned earlier, the differential equations and the mathematical functions representing the model are solved to perform the input/output (I/O) operations and to obtain the output of the model. However during a 'discrete non real-time simulation' the actual time required to solve the aforementioned equations and functions may be more or less than the simulation time step. But in case of real-time simulation it is necessary that (apart from the precise modeling of the physical system) all the computations are done within the simulation time step, only then the model under test can accurately represent the functioning and perform all the I/O operations as its equivalent real or physical system.

If the computations are not complete within the simulation time step the real-time simulation results are not accurate, which is also referred to as an '*overrun*' and the simulation ceases to be real-time. If the computations are done before the simulation time step is complete, then the remaining time, called the *'idle-time'* [7] is simply lost in case of RTS. This in contrast to the accelerated simulations where the remaining time would be utilized to perform the computations of the subsequent time step. Figure 1.1 to Figure 1.3 distinguishes between the characteristics of a real-time and non-real-time simulations.

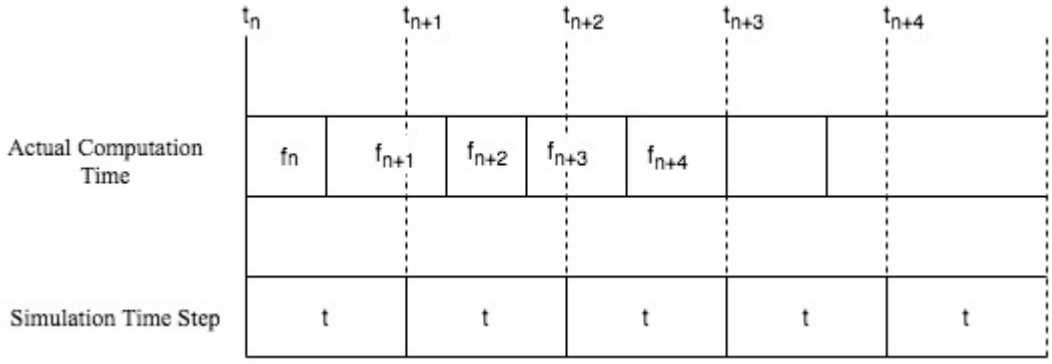


Figure 1.1. Timing Diagram when Computation Time is less than Simulation Time Step (non-real-time)

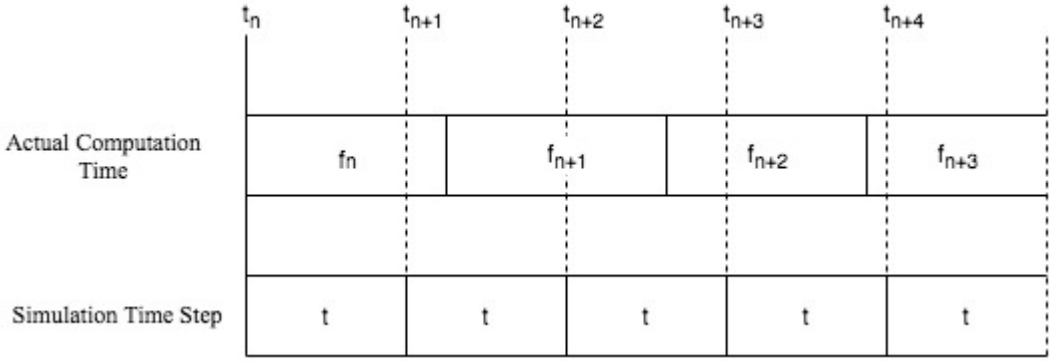


Figure 1.2. Timing Diagram when Computation Time is greater than Simulation Time Step (non-real-time)

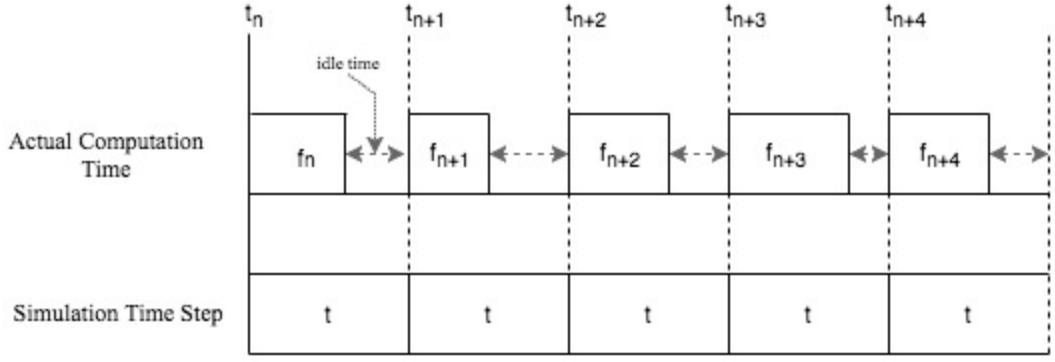


Figure 1.3. Timing Diagram during Real-time Simulation

1.3 Selection of the real-time simulator

As suggested in [7]-[11] selection of real-time simulators can be done based upon the applications to which they are intended for and can be categorized as:

Rapid Control Prototyping (RCP):

In a Rapid Control Prototyping a physical setup is always used and the controller is implemented in a real-time simulator. The presence of a virtual controller enables it to be configured with more flexibility and be debugged easily. Since the modelling and testing of the controller becomes easy and fast, the prototype model of the controller can be developed sooner to a final robust product.

Hardware in the Loop (HIL):

In Hardware in the Loop a virtual model is run on a real-time simulator, this virtual model emulates and behaves like a physical test bench; the virtual model is then controlled by a physical controller. In a variation of HIL, another real-time simulator can function as a physical controller and feed the virtual model in a separate simulator. This configuration is very beneficial because the controller can be tested even without a physical setup, the tests are very repeatable and can be done without any fear of damage, in contrast to a real hardware based setup. The work in this literature uses Hardware in the Loop (HIL) simulation.

Software in the Loop (SIL):

Software in the Loop is possible as the simulators grow more and more powerful. This allows the controller and the virtual plant model to be implemented in the same real-time simulator. Here, no physical input/outputs are used and that ensures that the fidelity of the signals is maintained. Moreover, the simulations can now run only in the virtual mode and there are no constraints in following the time clock of the real world. Simulation can now take their own time and if resources are available simulations can run faster than the real world time while maintaining the integrity of the results.

1.4 CPU and FPGA Based Simulation

The computer architecture has changed a lot in the last two decades, the advent of multiple cores, increase in parallel processing capabilities, decrease in the I/O latencies, faster working memories and improved hardware interfaces have made the modern computer quite suitable for real-time simulations. Figure 1.4 shows an Intel chipset architecture widely used until 2011 [12], Figure 1.5 shows an architecture used currently in most modern computers [13].

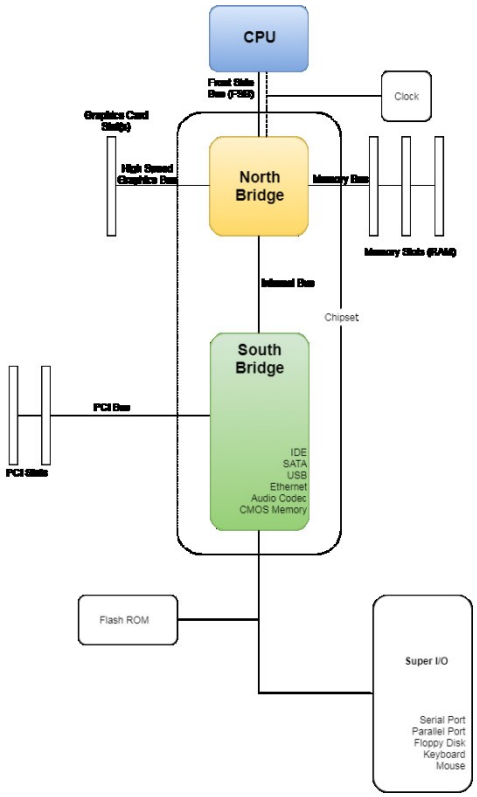


Figure 1.4. Computer chipset architecture prevalent before Sandy Bridge microarchitecture introduced in 2011

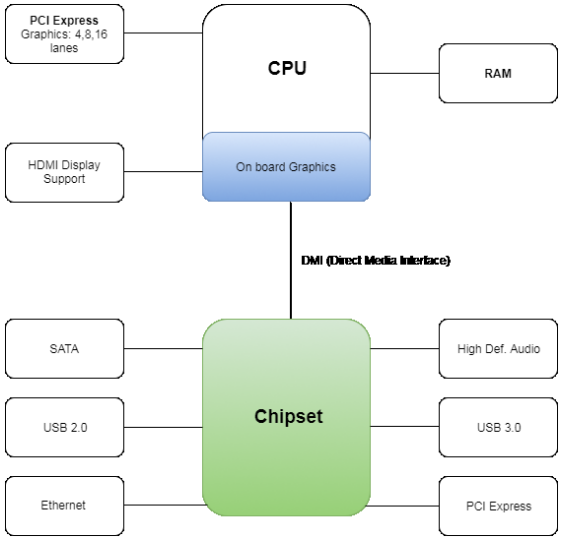


Figure 1.5. Modern computer chipset using Nehalem microarchitecture

However, even though the CPU of a modern computer has a very high clock frequency, the sequential nature of the operating system and the latencies still present at the I/O communications, allows it to have a minimal sampling time of about 5-10µs. This sampling time

is often enough for the real-time simulation of systems with slower dynamics such as a motor, but for fast systems like the high frequency switches in the power electronic systems, this sampling rate is inadequate. So, a methodology was developed wherein the models requiring very low sampling times are simulated in Field Programmable Gate Arrays (FPGAs) [14] – [16], the highly parallel structure of the FPGA allowed very high sampling rates with simulation time steps as low as 250ns. Figure 1.6 shows a CPU based simulation and Figure 1.7 shows a FPGA based simulation.

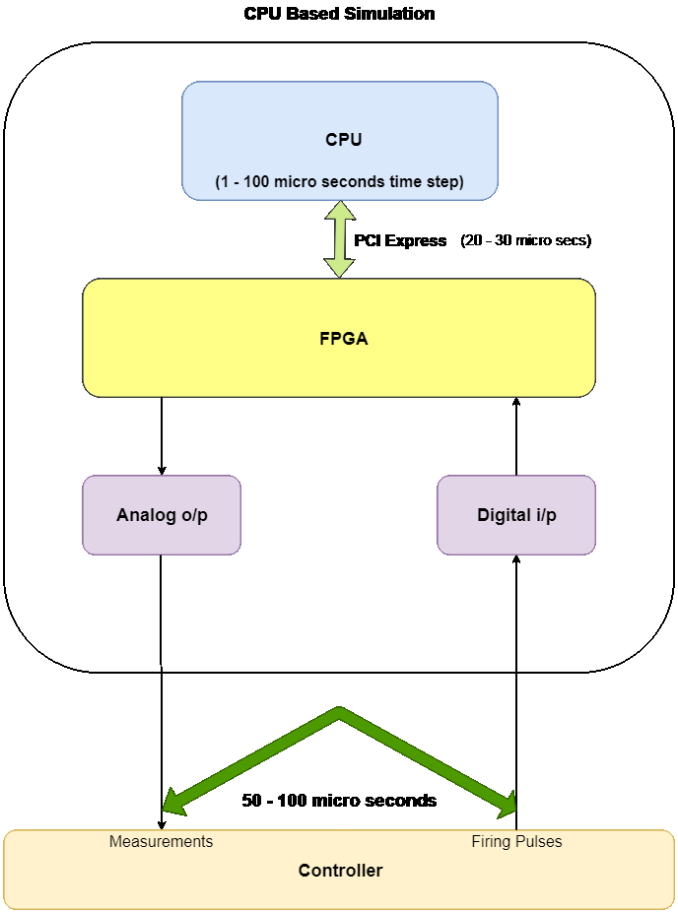


Figure 1.6. CPU Based Simulation

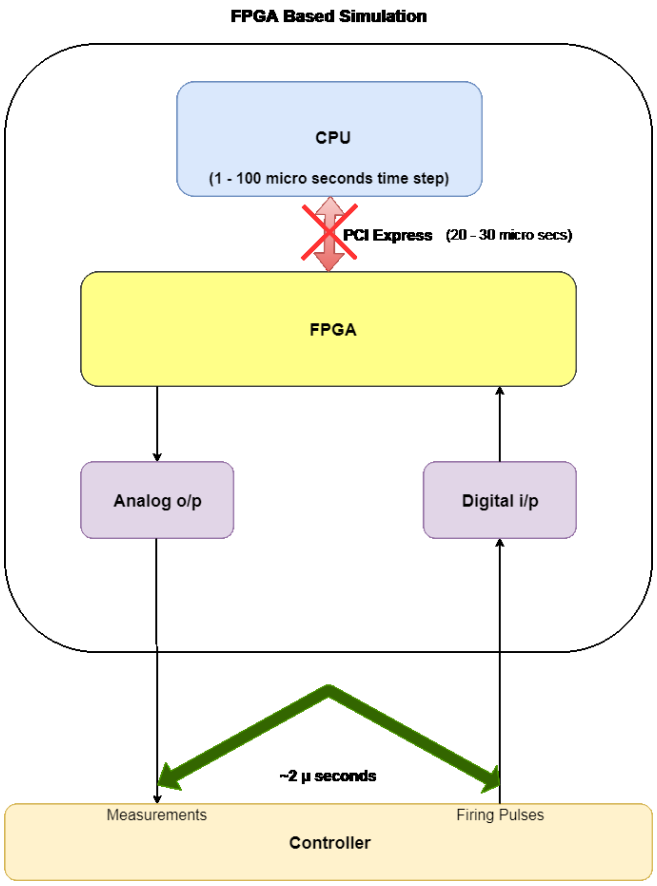


Figure 1.7. FPGA Based Simulation

1.5 Discrete Time Switch Model in Real-time Simulation

There are a number of models for representing a switch in order to make it suitable for computer simulations. Some simulators model the switch as a small resistance when it is ON and a large resistance when it is OFF [5], the value of the ON and OFF resistances are updated at every step of the iteration in the numerical method used for the simulation [5]. The trouble with this approach is that for a large network with a number of switches, huge amount of computational resources may be consumed for updating the resistance parameters at every step of the simulation. To cope with that, some real-time solvers achieve a precomputation of these matrices and store them in memory. Then, at every time-step, the corresponding matrix is used to solve the circuit. That is the case with ARTEMIS and Simscape Power Systems (SPS) SPS/SSM solvers. Due to memory limitations the number of switches will be limited consequently. In [17] a model with a RC circuit is proposed for an open circuit and an inductor for a short circuit, this representation removes the need of a system matrix inversion when the switch state changes

from ON to OFF or OFF to ON. Another model proposed in [18], represents the switch as a resistance across a capacitance, when the switch turns ON this resistance goes low and goes high when it is turned OFF.

In the switch model mentioned in [5] an ideal switch is modelled as a conductance in parallel with a current source. This conductance will not change with the iteration steps and the current source shall provide details of the state of the switch. The work in this thesis shall consider this model for real-time simulation.

1.6 Validation of Power Electronic Circuits

Validation of power electronic systems is necessary to ensure that a virtual model behaves like a real physical system to the extent possible. Real-time simulation of fast switching power electronic converters using a FPGA based Electric Hardware Solver (eHS) [8] is discussed in [16]. The design flow for the solver as well as validation results of the RTS of a number of power electronic converters are also covered. The results were validated by comparing the output of the eHS with those from the variable step Ode 23tb (stiff) solver in Simulink. This thesis will also utilize this Simulink solver as the benchmark. Some of the shortcomings of this method of simulating fast switching devices have also been discussed. Notwithstanding the shortcomings, the technique of performing real-time simulation of power electronic systems in FPGAs has a lot of potential. [7]

1.7 Multilevel Inverters

An introduction to the different topologies and working principles of multilevel converters are covered in [19], [20]. A more detailed overview about Neutral Point Converter (NPC) based inverters along with the modulation techniques is provided in [21]. Different modulation schemes for a three-level inverter are introduced in [22]. A comprehensive working of the three-level NPC inverter is discussed in [23] and [24], this will also be covered in detail in the Chapter 3 along with a step by step procedure in the hardware validation of the same. The results obtained from the simulation of a three-phase three-level inverter in SimScape Power Systems (SPS), a FPGA based eHS and the physical converter shall be compared. Furthermore, few

techniques for optimizing the switch conductance for the Pejovic discrete time switch model shall be discussed in more details in Chapter 4.

1.8 Conclusion

A brief introduction to circuit simulation and real-time simulation of power electronic converters is provided in this chapter. The chapter introduces some of the current trends in real-time simulation and also familiarizes the reader with the basics of RTS. The chapter also introduces some switch models which are often used in the RTS of electrical systems. Certain constraints in the RTS of power electronic systems are also discussed, this chapter also reckons with related work done by other researchers and gives a glimpse of the work that shall be done to complete this thesis.

Chapter 2. Switch Model in Real-Time Simulation

2.1 Switch Model in Real-time Simulation:

An ideal switch has been shown in Figure 2.1, it is a single pole switch with a single throw. The switch offers just two states either ON or OFF, the truth table is provided in Table 1.

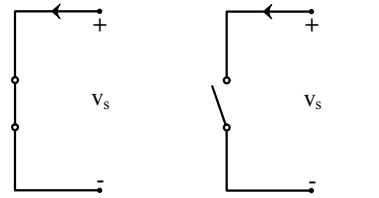


Figure 2.1. Ideal Switch

Table 1. Table of the Switch State and Boolean Value

Switch State	Boolean Value
ON	1
OFF	0

In an ideal switch, the change of state happens without any delay, moreover for controlled switches, which depend upon an external signal for the change of state to happen, a function can also be assigned that would govern the operation of the switch. This function is referred to as a switching function [5]. However, this function is not relevant to uncontrolled switches such as diodes, as their operation would not be dependent upon any control element outside the switch. In addition to this, the switch state can also be a function of the switch voltage or current.

To enable computer simulation of an ideal switch, an approximate discrete time switch model was developed. The model contains a conductance parameter, also known as Switch Conductance (G_s) in parallel to a current source as shown in Figure 2. 2. This representation of the discrete switch does resemble the equivalent circuit of a voltage controlled nonlinear resistor. When modified nodal analysis of the network containing the switches is done, the resultant system matrix will contain this G_s parameter. In a given simulation step the solution of the nodal equations would provide the output of the network and the G_s is updated after the iteration is over, inversion of the system matrix is done at every simulation step with an updated G_s value.

But this requires a lot of computational resource and time. To hasten the speed and increase efficiency of the simulation the switch conductance parameter (G_s) is kept constant, this implies that the system matrix would also contain the constant G_s value, which shall not be updated in the subsequent iterations. And since G_s is no longer updated in every simulation step, the system matrix inversion required for solving the network need not be done for every iteration and thus, can be done away with by just doing it once at the initialization of the simulation. This step is crucial considering that during RTS, the simulator must arrive with the solutions of the network within a given time step and failing to do so would result in an "overrun" or produce unreliable results.

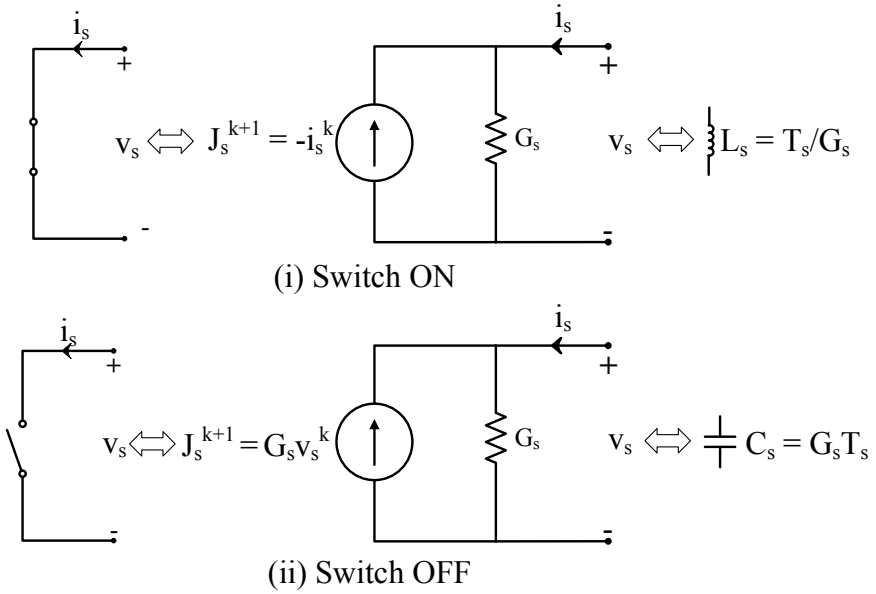


Figure 2.2. Discrete Switch Model of an (i) ON Ideal Switch and (ii) OFF Ideal Switch

As the G_s would remain constant and bear no burden in identifying the switch state, it is the current source, j_s^{k+1}, that indicates the state of the switch. It is to be reckoned that this j_s^{k+1}, is not a part of the system matrix that was discussed a little while earlier. In contrast to the model of the ideal switch, the current source, j_s^{k+1} in the discrete switch model is dependent upon the current and voltage parameters obtained in the previous iteration. If the present simulation step is $k+1$ and previous step is k, the state of the current source is given by (2.1):

$$j_s^{k+1} = \begin{cases} -i_s^{k+1}, \text{when switch is ON} \\ G_s v_s^{k+1}, \text{when switch is OFF} \end{cases} \quad (2.1)$$

But for the computation of j_s^{k+1}, it is necessary that it should be dependent upon known parameters or signals and in this case, the values of current and voltage from the previous simulation step are known. If a simulation step ($T_s = t^{k+1} - t^k$) is chosen such that current and voltage in the present simulation step is approximately the same as that of the previous step, i.e. $i_s^{k+1} \cong i_s^k$ and $v_s^{k+1} \cong v_s$, then the state of the current source can be re-written as:

$$j_s^{k+1} = \begin{cases} -i_s^k, \text{when switch is ON} \\ G_s v_s^k, \text{when switch is OFF} \end{cases} \quad (2.2)$$

Now, the computation of j_s^{k+1} is possible since it is dependent upon known values of current and voltages obtained from an earlier simulation step. This however, leads to an approximation in the discrete switch model representation of an ideal switch.

Moreover, the discrete switch model is also similar to the discrete time model of an inductor or a capacitor, but the switch conductance G_s, shall be replaced by G_L (in case of inductor) and G_c (in case of capacitor). The equivalent current sources shall be represented by j_L and j_c respectively. Comparing all the discrete time models (switch, inductor and capacitor) it can be inferred that switch state can be indicated by a small inductance when turned ON and a small capacitance when turned OFF. Since the switch conductance has to be kept constant throughout the simulation the following equality is achieved:

$$G_s = G_L = G_c = \frac{C_s}{T_s} = \frac{T_s}{L_s} \quad (2.3)$$

2.2 Real-time Simulation of Power Electronic Converters:

In case of Power Hardware in the Loop (PHIL) with power electronic converters, it becomes necessary to use fixed-step non iterative solvers. This is because the power converter may comprise of many switches and whose switching frequencies can be high in comparison to the sampling frequency of a real-time simulator. Moreover, the differential equations that represent the power electronic system are often very large and thereby difficult to simulate within a small time step. [25] Mentions a suitable time step in the range of 25-30µs for a 1 KHz PWM frequency, i.e. the simulations have to be completed within the 25-30µs range.

The typical sampling time available from Central Processing Units (CPUs) is in the range of 5-10μs and 5-10ns when FPGA is used. The CPU however, allows the computation of complex algorithms and solvers, whose compilation can be done in minutes in contrast to FPGAs, which only allows the implementation of much simpler ones. The compilation time taken by the FPGAs to get one 'bit stream' which configures the I/O ports can be in hours. Thus a combination of both CPU and FPGA technologies are used to achieve the real-time simulation of a power electronic system, high resolution samples of gate switching of a power electronic converter can be captured by the fast sampling FPGA and the averaged information can be provided to the CPU side for interpretation and make the results available to the user. [16], [25].

The minimum time step possible in a CPU without any I/O or external dependencies can be in the range of 1-100μs (7μs in case of OPAL-RT OP4510). Because of sequential operations involved in the processing in a CPU, sampling time is still high despite of the CPU's very high clock frequencies (>3 GHz for modern CPU's), improved parallel processing capabilities and lower I/O latencies. In contrast to the CPU, a FPGA has a clock frequency in the range of a few hundreds of MHz, but by means of parallel processing with logic blocks, very low sampling time can be achieved (5 - 400ns) which again can provide very high resolution samples of the gating pulses (50 - 100KHz). The total latency including I/Os in case of FPGA can also be as low as 2.5μs. This high speed capability allows the user to simulate on board switching device protections, such as V_{ce} short circuit protections. Very high sampling frequencies can also be achieved in FPGAs because the I/O ports are placed very close to the FPGA and the latencies are very low, moreover, the ADC/DAC's can be modelled on the FPGA itself. [16], [25], [26]

2.3 The need of Fixed Admittance Matrix Nodal Method:

As discussed in the earlier sections, an approximate discrete time model is used to represent an ideal switch for the purpose of simulation. A small inductance indicates the ON-State and a small capacitance indicates the OFF-State of the switch. The discrete switch model can be further represented by an equivalent conductance (G_s) in parallel to a current source (j_s^{k+1}). Some simulators use this model to represent an ideal switch, however the parameter G_s is updated in each iteration which is again burdensome to the computational resources and cannot be used in RTS of switches, meant for fast switching power electronic converters. Thus, another approach

was formulated which enables the parameter, G_s to be kept fixed and the value of the current source (j_s^{k+1}), also referred to a 'history term', is changed in accordance to the state of the switch. Modified nodal analysis can be used to formulate the circuit elements. The current source is not a part of the system admittance matrix, and is contained in the vector of the unknown independent sources. The fixed admittance matrix obtained from MNA, with a constant G_s is the basis of the FAMNM. This approach with the fixed admittance matrix, inverts the system matrix, say '*A'* only once at the start of the simulation. This inverted matrix 'A^{-1}' is then multiplied with the vector '*y*' containing the known sources which also includes the current sources or the memory elements of the discrete switch model [5]. If *'x'* is the vector containing the nodal voltages and currents then during a current simulation step *'k+1'* the network or the circuit can be solved as (2.4):

$$x^{k+1} = A^{-1}y^{k+1} \tag{2.4}$$

2.4 Limitations of Pejovic Switch Model

There are a few limitations of the Pejovic switch model which can cause simulation inaccuracies, they are:

Artificial losses during switch commutation: In the discrete time switch model an ideal switch can be modelled as an inductor when it is ON, and a capacitor when it is OFF. If there is a change of state of the switch in between the simulation steps *k* and *k+1* from ON to OFF, the inductor is replaced by a capacitor. The energy stored in the inductor when the switch was ON is $0.5L_s(i_s^{k-1})^2$, where L_s is the inductance when the switch is modelled as an inductor, and i_s^{k-1} is the current flowing through the switch in an earlier simulation step. But, when the switch turns OFF, say at $k+1^{th}$ simulation step the switch is now modelled as a capacitor and the state of the memory element is $j_s^{k+1} = G_sV_s^k$, where V_s^k is the switch voltage in the k^{th} simulation step i.e. when the switch was still ON, hence $V_s^k = 0$. The energy now stored in the capacitor is $0.5C_s(V_s^k),^2$ which is equal to zero, so during the state change from ON to OFF an energized inductor was replaced by a capacitor without any charge and hence, the energy that was stored in the inductor is lost; this is also true when the reverse happens when the switch state changes from OFF to ON. These artificial losses during the state changes can cause errors in the simulation results [26].

Need of proper optimization: It is important to properly optimize the value of G_s, a small value would mean that for a given time step (T_s) equivalent inductance $(L_s = T_s/G_s)$ is large and capacitance $(C_s = T_sG_s)$ is small. A large L_s will act as a high reactance when a high switching frequency is applied and so will a low C_s; this high reactance will allow lesser power to flow through the switch. Similarly when a high G_s value is used, more power can flow through the switch. Thus, G_s can influence the power flow in the circuit and an improper selection can produce an erroneous output, moreover, when a circuit is more complex with a greater number of switches, predicting a proper G_s becomes more difficult. [26]

2.5 Conclusion

A discrete time switch model is introduced in this chapter. This model shall be used in the real-time simulation of power electronic converters throughout this thesis. There are other approaches and different switch models as well; however, this model is one of the most widely used. The chapter also discusses about the FAMNM approach and its need in RTS. Finally some limitations of the discrete switch model are elaborated.

Chapter 3. Real-Time Simulation of a Three-Level NPC Inverter

3.1 Introduction to Multilevel Inverters

Multilevel Inverter (MLI) topologies can be broadly classified into three categories [19], [20], [23]:

1. Diode Clamped Multilevel Inverter
2. Flying Capacitor Multilevel Inverter
3. Cascaded Inverter with Separate DC Sources

Diode Clamped Multilevel Inverter:

The diode clamped inverter was first proposed by Nabae Et Al in 1981, this topology consists of a DC bus whose voltage levels are subdivided into smaller ones by means of capacitors. The maximum number of voltage levels so obtained are *n+1,* where *n* is the number of capacitors. The point where the capacitors meet is clamped by diodes and hence the name diode clamped multilevel inverter. The point where the first two top switches connect, is joined by the cathode of the first clamping diode and the anode of the diode is connected to the meeting point of the first two capacitors; this is done for the remaining clamping diodes of the higher side (i.e. for all the switches connected above the DC bus midpoint). The first clamping diode of the lower side (i.e. for all the switches connected below the DC bus midpoint) is arranged in a similar fashion but now the anode is connected in between the first two switches just below the DC bus midpoint and the cathode is connected between the first two capacitors, the remaining clamping diodes of the lower side are connected to the corresponding elements. The output pole voltage levels so obtained are: 0, $+/-V_{dc}/n$, $+/-2V_{dc}/n$, $+/-3V_{dc}/n$….. $(n - 1)V_{dc}/n$

As the number of levels increase the output waveform would have lesser harmonic distortion in the output voltage and current. Figure 3.1 shows a three-level diode clamped inverter.

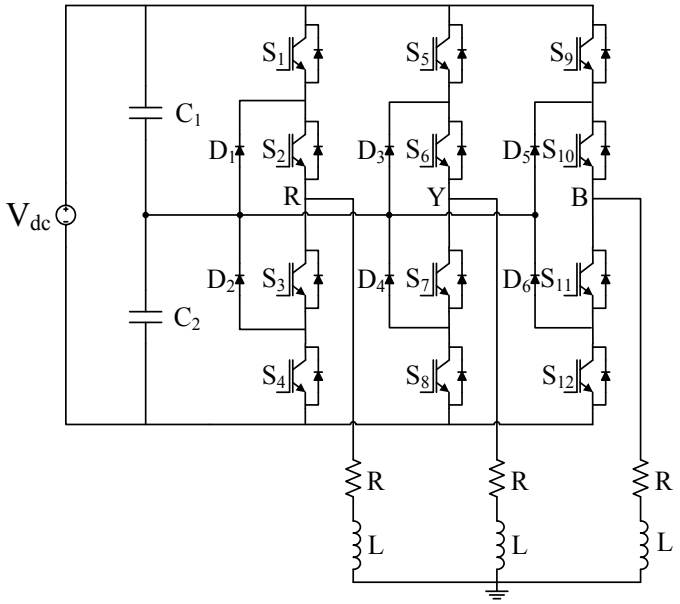


Figure 3.1. Circuit Diagram of a Three-phase Three-level NPC Inverter

Flying Capacitor Multilevel Inverter:

The flying capacitor or the capacitor clamped inverter is quite similar to the diode clamped inverter but the clamping diodes are replaced by capacitors. The capacitor voltages can be regulated to control the output voltages. The switches can be controlled to charge or discharge the clamping capacitors and thereby the output voltage can be balanced. The switching states available in this topology is higher when compared to diode clamped inverter, the capacitors can also have different ratings depending upon their position in the legs. The inverter also allows control of active and reactive power flow but the requirement of large number of capacitors can make the inverter very bulky and expensive. The control of the inverter is more complex compared to NPC, the switch utilization and efficiency is poorer. [20]

Cascaded Inverter with Separate DC Sources:

In a cascaded multilevel inverter, cells of single phase full bridge inverter are arranged in a cascaded manner to obtain a multilevel phase leg to produce the desired staircase AC voltage waveform. A single phase full bridge inverter produces a three-level voltage output i.e. if the source voltage is V_{dc} the output from one cell would be $+V_{dc}$, 0 & $-V_{dc}$. More levels are obtained by stacking these cells together in series, this uniformity makes this topology easy to design and

fabricate. This topology also uses the least number of power components among other MLI's but the need of isolated and separate DC power sources is a major shortcoming. [20]

3.2 Working of the Three-level NPC Inverter

The three-level inverter is the lowest number of voltage levels achieved amongst multilevel inverters. A three-level inverter produces three voltage levels by connecting the AC output either to +0.5 V_{dc}, -0.5V_{dc} or 0 V_{dc}. This is in contrast to a two-level inverter where the output voltage is produced by connecting the AC side just to the +0.5V_{dc} and -0.5V_{dc} of the DC link. Owing to the availability of a third voltage level, the output voltage waveform so obtained is closer to the sinusoidal waveform desired [24], [28]. This results in a significant reduction in the Total Harmonic Distortion (THD) levels of current and lesser filtering requirements as well as lower losses in the filter. For the same THD specifications the switches can be operated at lower frequency thus resulting in lower switching losses.

The diode clamped multilevel inverter can be again classified into two sub-categories:

1. Three-Level NPC (also NPC 1), see Figure 3.9
2. Three-Level TNPC (also NPC 2), see Figure 3.8

In a two-level inverter the DC bus midpoint '0 V' may or may not be available physically, this midpoint is available halfway between the DC buses usually formed by a voltage divider with two capacitors connected in series. The operation in a leg of a two-level inverter can be realized with the functioning of a single pole switch with two throws. The switch can connect to the positive DC bus or the negative DC bus and there is no intermediate state in between. The voltage between the pole and the midpoint is half of that of the DC voltage, i.e. for a DC bus voltage of V_{dc} then the pole voltage would be V_{dc} / 2. So, when a pole say 'R', can have either V_{RO} = +V_{dc} / 2 when it is connected to the top positive bus or V_{RO} = - V_{dc} / 2, when connected to the bottom DC bus. This availability of the two voltages with opposite polarity at the pole of the switch gives it the name of two-level inverter.

For a three-level inverter however, the DC neutral or the DC bus midpoint is available for connection. This can be evaluated by considering one leg of the three-level inverter and applying a similar analogy to that of a two-level inverter, but with a single pole three throw switch instead of two throws in between a DC bus. Understanding the switch realization of the three-level

inverter as discussed in [28] can be very useful in the real-time simulation work that will be done in the coming sections. The three throw switch can now connect to the top DC bus, the DC midpoint and the bottom DC bus. The voltage between the pole and the DC bus would again be half the DC bus voltage. For a DC bus voltage V_{dc}, the pole voltage with respect to the DC bus midpoint would be V_{dc} / 2. So when a pole 'R' is connected to the top DC bus the pole voltage V_{RO} = + V_{dc} / 2, when it is connected to DC bus midpoint, the pole voltage V_{RO} = 0 and finally when the pole is connected to the bottom DC bus the pole voltage V_{RO} = - V_{dc} / 2. The availability of these three voltage levels at the pole gives it the name three-level inverter. [24], [28]

There are some additional requirements that the switches have to meet and enable the three-level inverter to function properly. The switches should be able to let the current flow both ways and all the while should also be able to maintain the load voltage, notwithstanding the direction of current [28]-[30]. Moreover, for a three-phase inverter three such legs shall be required and each leg shall produce output voltages which are electrically apart by 120^{o}.

To get the switch realization in a single leg of a three-level inverter, a single pole switch with three throws is chosen with a pole 'R' and throws 'T_1', 'T_2' and 'T_3' and the following three states are possible:

State 1: When the pole is connected to the top bus i.e. 'R' connected to T_1

The current should be able to flow from 'R' to T_1 and vice versa, the pole is not connected to the other throws and the switches which establish this must allow the aforementioned flow of current and block the voltages between the open throws. Table 2 below provides the details of state of the switches between the pole and the throws, and the blocking voltages to be endured.

Table 2. Voltage Blocked by the Top Throw Switch

Switch (between pole and throw)	State	Voltage to be blocked
R - T_1	Closed	0
R - T_2	Open	0.5 V_{dc}
R - T_3	Open	V_{dc}

State 2: When the pole is connected to the DC bus midpoint i.e. 'R' connected to T_2

The current should be able to flow from 'R' to T_2 and vice versa, the pole is yet again not connected to the remaining two poles. Table 3 below provides the details of the state of the switches between the pole and the throws and the blocking voltages to be endured in State 2.

Table 3. Voltage Blocked by the Middle Throw Switch

Switch (between pole and throw)	State	Voltage to be blocked
R - T_1	Open	0.5 V_{dc}
R - T_2	Closed	0
R - T_3	Open	0.5V_{dc}

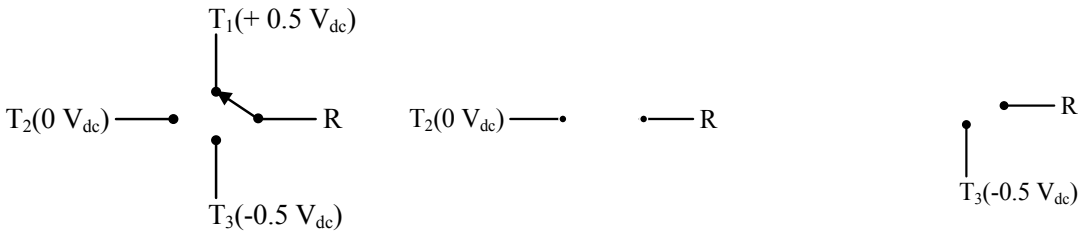
State 3: When the pole is connected to the bottom DC bus i.e. 'R' connected to T_3

The current should be able to flow from 'R' to T_3 and vice versa, the remaining two poles are not connected. Table 4 below provides the details of the state of the switches between the pole and the throws and the blocking voltages to be endured in State 3.

Table 4. Voltage Blocked by the Bottom Throw Switch

Switch (between pole and throw)	State	Voltage to be blocked
R - T_1	Open	V_{dc}
R - T_2	Open	0.5 V_{dc}
R - T_3	Closed	0

Combining all the three states obtained earlier and obtaining the equivalent electronic switches for State 1 as shown in Figure 3.2.



(a). Throw 1 ON in State 1 (b). Throw 2 OFF in State 1 (c). Throw 3 OFF in State 1

Figure 3.2. State of the Switch with Pole Connected to the Top DC Bus

So the equivalent electronic switch for throw T_1 must allow bidirectional current flow through it and must block a maximum voltage of V_{dc}. The switch that can be established shall be a transistor with an antiparallel diode rated at V_{dc} as shown in Figure 3.3.

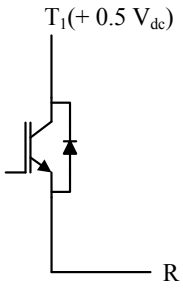
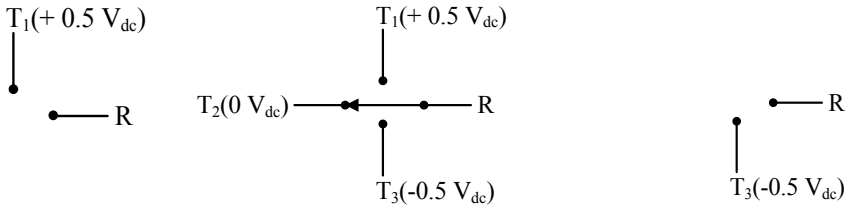


Figure 3.3. Equivalent Electronic Switch for Throw T_1

Combining all the three states obtained earlier and obtaining the equivalent electronic switches for State 2 as shown in Figure 3.4.



(a). Throw T_1 OFF in State 2 (b). Throw T_2 ON in State 2 (c). Throw T_3 OFF in State 2

Figure 3.4. State of the Switch with Pole Connected to the Midpoint of the DC Bus

The equivalent electronic switch for throw T_2 must allow bidirectional current flow through it and must block a maximum voltage of $0.5V_{dc}$. The switch that can be established shall be a four quadrant switch comprising of two antiparallel transistors with series diodes rated at $0.5V_{dc}$ as shown in Figure 3.5.

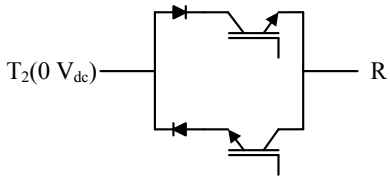
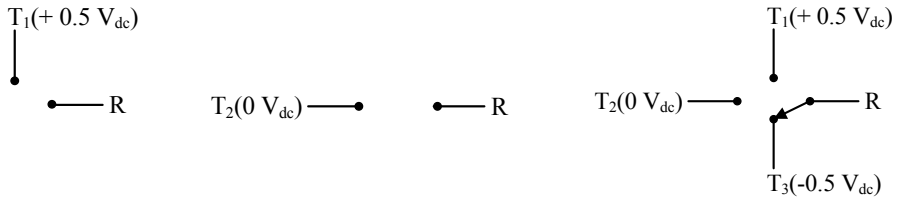


Figure 3.5. Equivalent Electronic Switch for Throw T_2

Combining all the three states obtained earlier and obtaining the equivalent electronic switches for State 3 as shown in Figure 3.6.



(a). Throw 1 OFF in State 3 (b). Throw 2 OFF in State 3 (c). Throw 3 ON in State 3

Figure 3.6. State of the Switch with Pole Connected to the Top DC Bus

The equivalent electronic switch for throw T_3 must allow bidirectional current flow through it and must block a maximum voltage of V_{dc}. The switch that can be established shall be a transistor with an antiparallel diode rated at V_{dc} as shown in Figure 3.7.

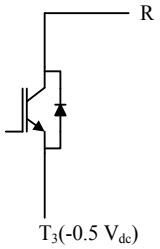
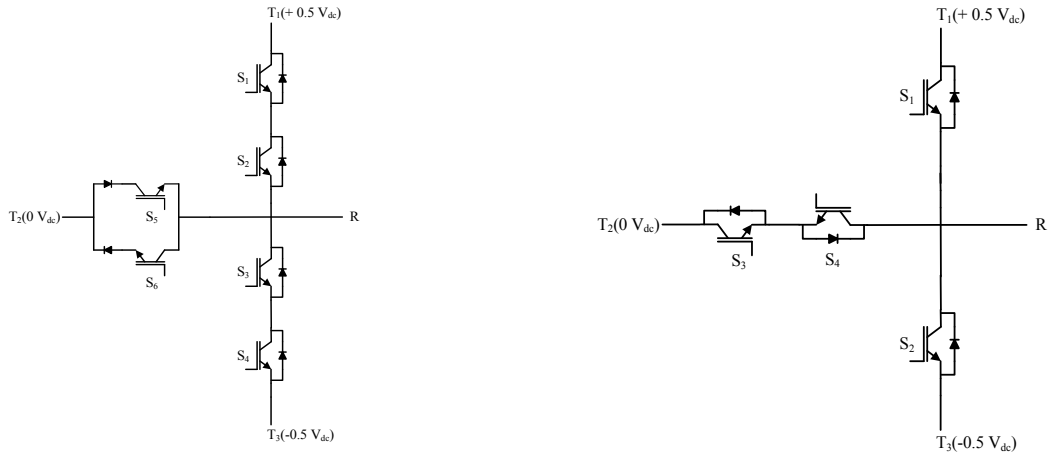


Figure 3.7. Electronic Switch for Throw T_3

The derived configuration combining all the equivalent switches is close to the three-level TNPC topology, this configuration however, has switches with different blocking voltages, and this can be further modified to have a topology where the switches have similar blocking voltages as shown in Figure 3.8 (i), the 3L TNPC topology is shown in Figure 3.8 (i). The basis for this derivation is that, when the pole 'R' is connected to the throw 'T_1' the two switches S_1 & S_2 have to be turned ON together, but when the throw has to be disconnected either S_1 or S_2 can be turned OFF. At this state, the switches between 'R' and throw 'T_2' has to block a voltage of $0.5V_{dc}$, similarly the switches S_3 and S_4 block the DC bus voltage V_{dc} together. The blocking voltage for each switch in this configuration is 0.5 V_{dc}.



(i) (ii)

Figure 3.8. (i) Derived configuration and (ii) 3L TNPC topology

Another redundancy would remain in the circuit, which can be seen when S_1 & S_2 are ON (i.e when Pole 'R' is connected to throw 'T_1'), the voltage between pole 'R' and throw 'T_2' is blocked by the diode in series of S_5. This scenario can be repeated if the pole 'R' is connected to the throw 'T_3', where again only the diode in series with S_5 will block the voltage. Moreover, to isolate throw T_1 from the pole, S_2 can be opened instead of both S_1 and S_2, similarly T_2 can be isolated just by opening S_3. Thus the circuit can be reduced further, and S_5, S_6 can be removed. The following circuit in Figure 3.9 achieves the final reduction in the redundancy and works the same as the earlier circuit.

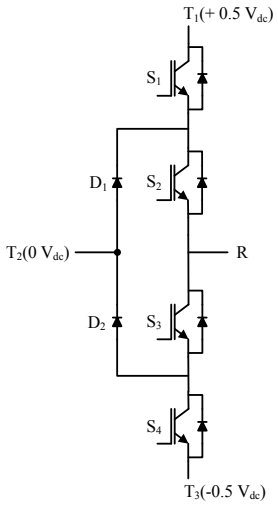


Figure 3.9. Single Leg of a NPC Inverter

From the switch status given in Table 5, it can be seen that the switches S_1 & S_3 are never ON together, again S_2 & S_4 are never ON together so the combinations S_1 & S_2, S_3 & S_4 are always complementary. It is also observed that for every pole and throws connection S_2 and S_3 switches are involved, meaning that they are ON for a longer duration than S_1 and S_4, which would also imply that there are more losses in S_2 and S_3. [28]

Table 5. Complementary Behavior of the Switches

Connection (Pole and Throw)	Switch Status (ON)	Switch Status (OFF)
Pole 'R' to 'T1'	S_1 & S_2 ON	S_3 & S_4 OFF
Pole 'R' to 'T2'	S_2 & S_3 ON	S_1 & S_4 OFF
Pole 'R' to 'T3'	S_3 & S_4 ON	S_1 & S_2 OFF

Table 6. Switch States and Instantaneous Switch Voltages

S_1	S_2	S_3	S_4	Pole Voltage (V_{RO})
1	1	0	0	+0.5 V_{dc}
0	1	1	0	0 V_{dc}
0	0	1	1	-0.5V_{dc}
0	0	0	0	0 V_{dc} (unloaded)

3.2.1 Allowed Switching States

In case of a three-level NPC inverter, there are certain switching states which are to be avoided in-order to prevent damage or occurrence of faults [30]. Any state that involves the switching ON of three adjacent switches would cause short circuiting of the DC bus and hence must be prevented, if $S_1/S_2/S_3$ are switched on simultaneously then the top half of the DC bus is shorted and if $S_2/S_3/S_4$ are switched ON simultaneously then the lower half of the DC bus is shorted. If $S_1/S_2/S_4$ are switched together then the entire DC bus voltage is upon S_3 and if the applied voltage is greater than the blocking voltage of S_3, it would fail and would cause a potential short circuit of the DC link, this is also applicable to when $S_1/S_3/S_4$ are switched together.

Care must be taken during the switching ON and OFF operation of the inverter legs, the inner switches must be completely switched ON before the outer switches, else the DC link voltage will have to be borne by the inner switches which can be damaged, if the voltage exceeds its blocking capability. A reverse order has to be followed during the turning off process, i.e. the inner switches must be entirely turned OFF before the outer switches. Allowable switching states are given in Table 7.

Table 7. Allowed Switching States

Switches	**Allowed States**				
S_1	0	0	0	1	0
S_2	0	1	0	1	0
S_3	0	0	1	0	1
S_4	0	0	0	0	1

Switching States that can potentially cause harm and should be avoided are given in Table 8.

Table 8. Switching States to be avoided

Switches	**Switching States that will cause faults**				
S_1	1	1	1	0	1
S_2	1	1	0	1	1
S_3	1	0	1	1	1
S_4	0	1	1	1	1
Switches	**Switching States that may cause harm to the switches**				
S_1	1	1	0	1	0
S_2	0	0	0	0	1
S_3	0	0	0	1	0
S_4	0	1	1	0	1

3.2.2 Classification of Modulation Techniques Available For 3 Level Inverters

There are three broad classifications of Modulation Techniques for Multilevel Inverters [21], [22]

1. Carrier-Based PWM
    a. Based on types of modulating Signal
        i. Sinusoidal PWM (SPWM)
        ii. Third Harmonic Injected PWM (THPWM)
        iii. 60^{o} Sinusoidal Modulated PWM (SDPWM)
        iv. Trapezoidal PWM (TRPWM)
    b. Based on type of carrier signal
        1. Level Shifted PWM
            1. Phase Disposition (PD-PWM)
            2. Phase Opposition Disposition (POD-PWM)
            3. Alternate Phase Opposition Disposition (APOD-PWM)
            4. Carrier Overlapping (CO-PWM)
        2. Phase Shifted PWM
2. Space-Vector Modulation (SVM)
3. Selective Harmonic Elimination (SHE)

3.2.3 Sinusoidal PWM (SPWM) for a Three-level Inverter:

In a Sinusoidal PWM generating technique the carrier or switching frequency is compared to a sinusoidal modulating signal. The gating signals are generated when the carrier and modulating signals intersect. For a three-phase inverter, three modulating signals are used. Moreover, for multilevel inverters multiple carrier waveforms are used and there are several SPWM techniques that can be used in multilevel converters.

In a two-level inverter, a comparison is made between one sine wave and a triangular carrier wave, the gating pulses so generated could be used to operate one pair of complementary switches. A three-level inverter leg has two such pairs of complementary switches and hence would need a combination of one sine and two carriers or two sines and one carrier. In a Phase Disposition SPWM [20], [22], the carrier signals used are similar in terms of frequency and amplitude, there is no phase difference between the carriers but the signals are given a DC offset, for example in a three-level inverter a carrier signal with a positive DC offset can be used to compare the upper half of the sinusoidal modulating signal and an another carrier with a negative DC offset can be used to compare the lower half as shown in the Figure 3.10. Figure 3.11 shows the switching of the top two switches of the first leg of the inverter. The upper carrier will produce gate pulses for the outer switch and the lower carrier shall produce gate pulses for the inner switch.

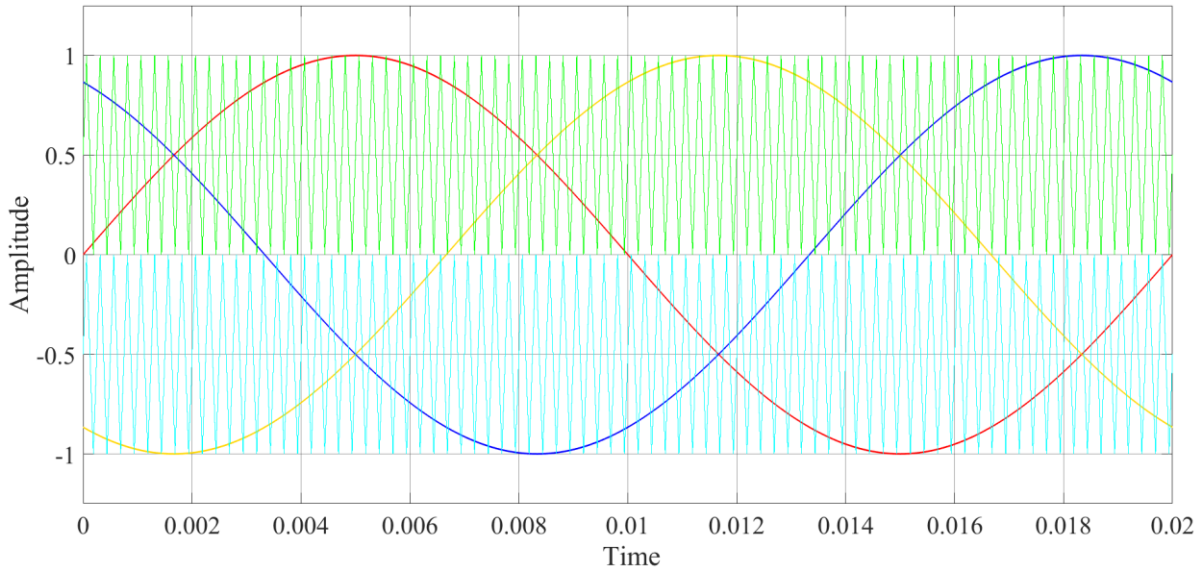


Figure 3.10. Two Carrier Sinusoidal Modulation

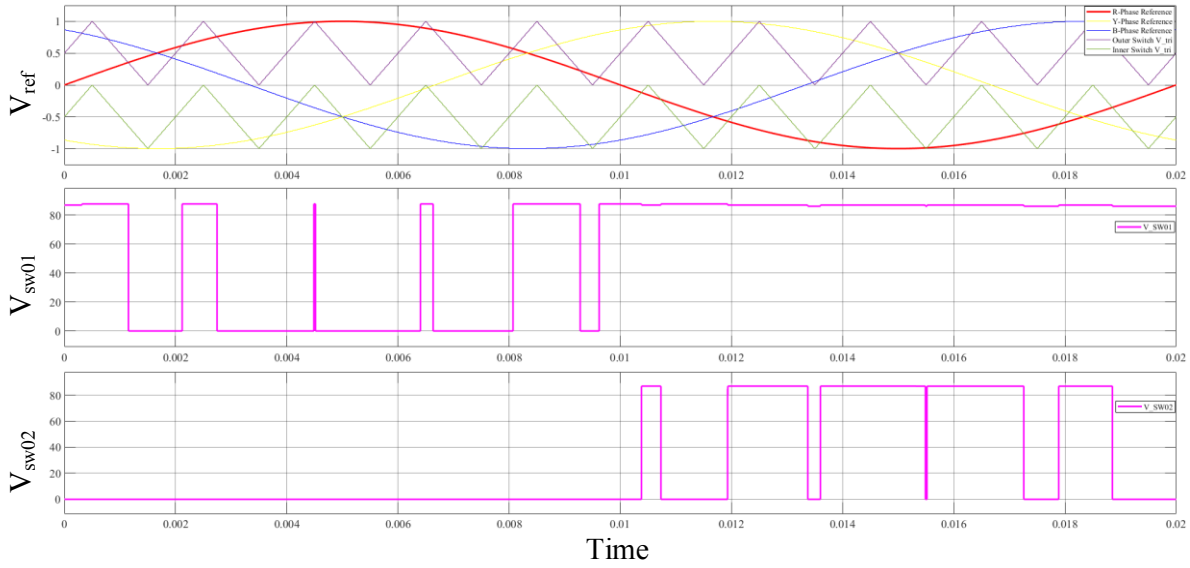


Figure 3.11. Switching of the Top Outer and the Inner Switches of the First Leg of the Inverter

For a real-time simulation of the three-level inverter the RTE-SPWM block in RT-Lab operates with a single carrier with level between 0 and 1. Hence, there is no level shifted carrier for the inner switch; instead, the modulating sine wave with levels between -1 and 1 is replicated and given a DC bias of 1 so the bottom half of the sine wave, which was earlier in the levels of 0 and -1 is lifted to 0 and 1. Thus, instead of having two different carriers for the two complementary switch pairs, there are now two sine-waves compared to a single carrier, each producing the gate pulses for either complementary switch pair in a leg of a three-level inverter.

A list of other existing SPWM techniques used for multilevel inverters [22]:

1. Phase Opposition Disposition (POD-PWM)
2. Alternative Phase Opposition Disposition PWM
3. Phase Shift PWM
4. Carrier Overlapping
5. Multi-Carrier Sinusoidal Pulse Width Modulation with Variable Frequency PWM

3.2.4 Advantages and Applications of Three-level Inverter

There are several advantages of a three-level inverter compared to a two-level [29]. Amongst the foremost ones is that, with higher switching frequencies the losses in the filters are lesser than in case of a two-level inverter. Moreover, for the same switching frequency the total THD in a three-level inverter is also less. Since the DC link voltage is shared amongst four switches, the voltage stress per switch is also reduced and hence higher voltage blocking capability is achieved for a given device rating. The reduction in the THD levels of current also means that the filter requirement shall be less too, which would lessen down copper costs. Figure 3.12 shows the line voltage of a two-level inverter; Figure 3.13 shows the THD of the two-level, Figure 3.14 and Figure 3.15 shows the line voltage and THD of a three-level inverter respectively. The voltage THD was reduced from 80.76 % in a two-level inverter to 38.27 % in a three-level using the same switching frequency, input DC voltage and load. Current THD was also reduced from 9.47 % to 4.45 %.

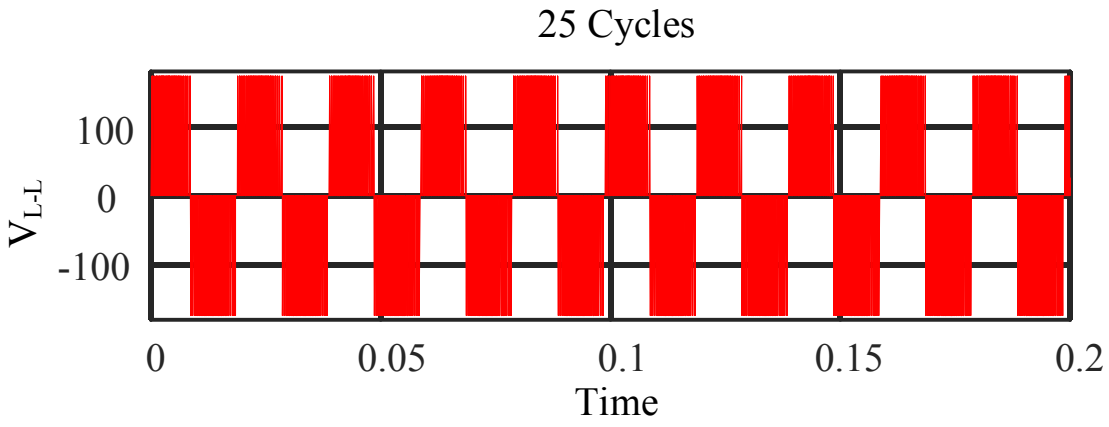


Figure 3.12. Line Voltage of a Two-level Inverter

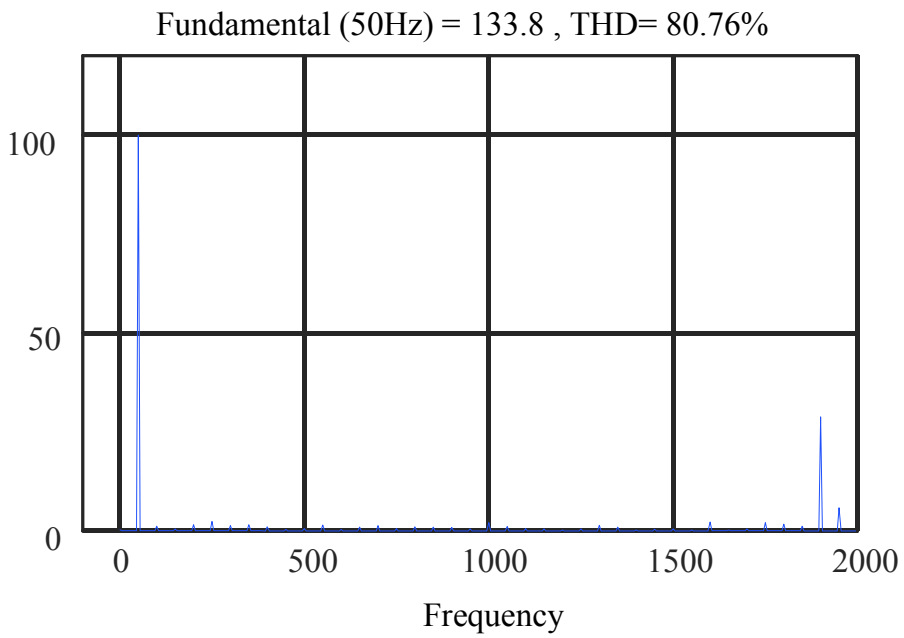


Figure 3.13. THD of a Two-level Inverter

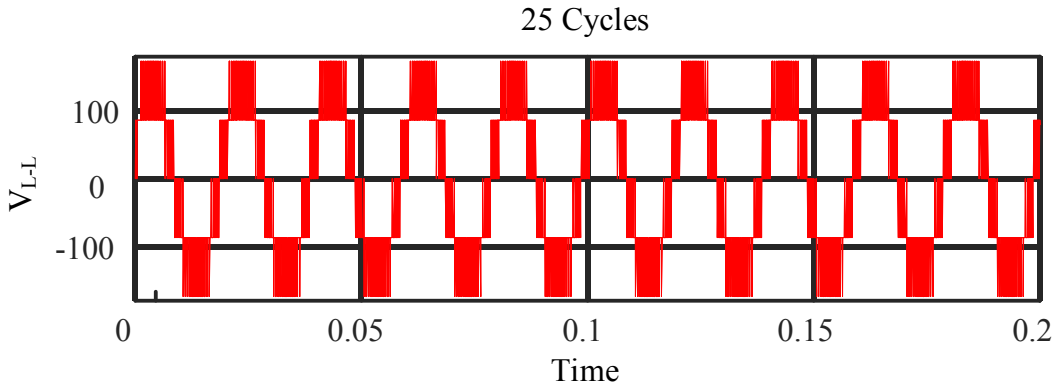


Figure 3.14. Line to Line Voltage of a Three-level Inverter

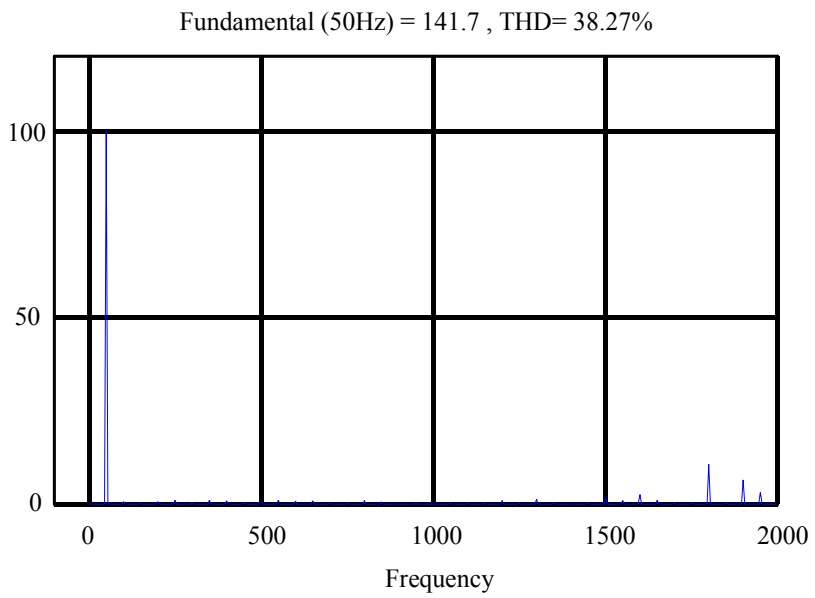


Figure 3.15. THD of a Three-level Inverter

Applications:

Multilevel Inverters (MLI's) can remove the need of the phase shift transformer often used to reduce harmonics. [20], [29]

Multilevel inverter such as a three-level NPC inverter is finding a lot of usage in medium voltage (2 to 6 KV) motor drives.

MLIs have also found applications in power systems especially the cascaded bridge topology owing to its uniform structure that can be stacked up and obtain large power handling capabilities.

3.3 Modelling of a Three-level Inverter in Real-time Simulation

Real-time simulation has changed a lot from the large, expensive and inflexible analogue simulators to the microprocessor and Digital Signal Processor (DSP) based simulators seen today. With the advent of multi-core processors at lower cost and high performances, RTS could be performed with smaller workstations in contrast to the supercomputers that were needed a decade ago. RTS simulators can now run in standard operating systems such as Windows or Linux and are also compatible with multi-domain analysis tools such as Simulink, PSim etc. The ability to run the real-time simulators under multi-domain environment enables the interfacing with different systems such as electrical, power electronics and mechanical systems etc. A

relatively new way of simulating the models on FPGA, facilitates the real-time simulation of fast switching power electronic devices. The FPGA provides the low sampling times required for high resolution sampling of the gating pulses, but there can be many complications in the implementation. Some of the complications can be due to the long time required for compiling the FPGA and complexity in the coding of the same. The real-time simulation covered in this literature employs this distributed structure where the fast switching gate pulses are sampled by FPGA and the systems with slower dynamics can be sampled by a fast multi-core microprocessor on board of the real-time simulator. [16], [25]

3.3.1 The RT Lab Environment

The preliminary modelling, compilation, control initialization and the HMI are handled by a host computer. The software used for the real-time simulation is RT-Lab from OPAL-RT which has been integrated with MATLAB/Simulink. To start off with a real-time simulation in RT-Lab, a new *project* has to be created and then a *new model* built, the model has to be assigned to a *target* or a simulator after proper configuration. All of these, can be accomplished from the *Project Explorer* menu in the RT-Lab window as shown in Figure 3.16. Even though a model can be created or edited without a connection to a simulator, a real-time simulation won't take place without one. The RTS for a three-phase three-level inverter was done with an OPAL-RT OP4510 simulator [31], the required model can be prepared in Simulink environment accessible within RT-Lab. The model should be run in the Simulink environment before it is *built* or *loaded* onto the simulator; any model that produces errors in Simulink environment should not be loaded to the simulator. The elements in the model can be distributed into subsystems, there can be three such subsystems: A) Master Subsystem B) Console Subsystem and C) Slave Subsystem.

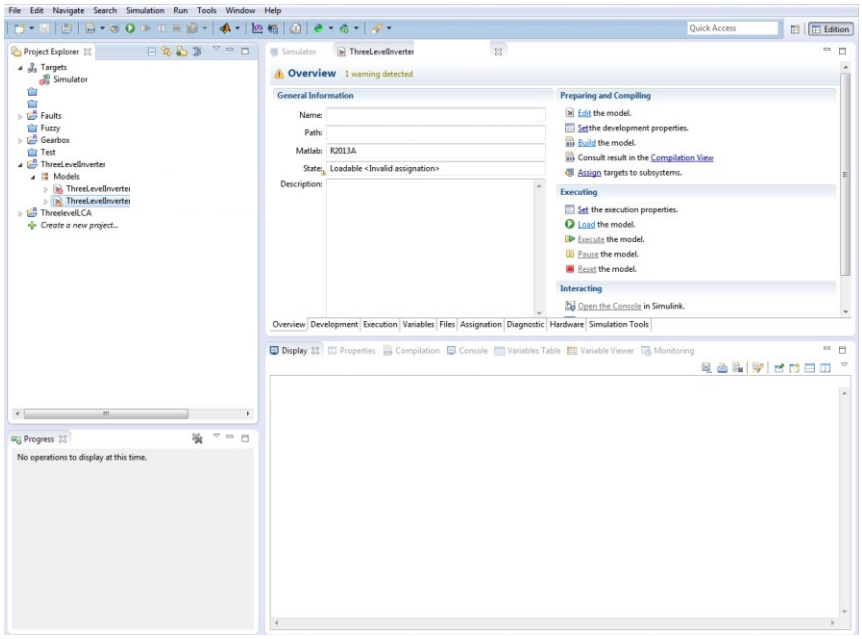


Figure 3.16. The RT Lab Window

A. Master Subsystem (SM): Any model intended for a real-time simulation can have only one Master Subsystem. This subsystem would contain all the signal generators, input output operations, data logging, mathematical operations etc. The naming of the subsystem starts with 'SM' to enable RT-Lab to know that the ascribed subsystem is a master. The master subsystem shall no longer remain accessible when the simulation is running.

B. Console Subsystem (SC): The console subsystem's name start with 'SC' and the elements contained inside this subsystem shall remain accessible to the user during the course of the simulation. Any parameter that has to be changed during the simulation must be placed here. For the three-level inverter, there may be a need to change the modulation index or the switching frequency or the DC link voltage, which can be changed at will if configured in the console.

C. Slave Subsystem (SS): The use of the slave subsystem is necessary while simulating large systems where the computation is not possible within one master and has to be distributed among different computer nodes.

For the real-time simulation of the three-level NPC inverter only the Master and the Console Subsystems shown in Figure 3.17 shall be used. The Console and the Master Subsystems have to be connected in a loop. It is necessary that all the signals coming in or going out of the

subsystems pass through the communication blocks known as *'Op Comm'* block, shown in Figure 3.18 before any operation is performed on the signal. The purpose of the block is to read the synchronized signals from other subsystems. Moreover, since a physical converter shall run in parallel along with the virtual model, the simulator must be set to *'hardware synchronized'* mode rather than *'software synchronized'* during the initialization of the simulator. The console contains the parameters that may be changed during the simulation, these parameters are DC link voltage (V_{dc}), PWM frequency (f_s), modulating frequency (f_m), enable switch etc.

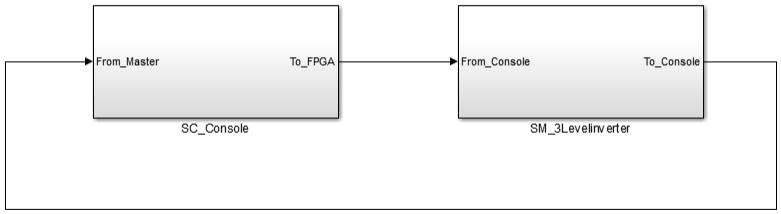


Figure 3.17. The Master and Console Subsystems in RT Lab

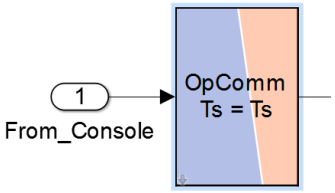


Figure 3.18. The OpComm Block in RT Lab

When the simulation is ON, these values from the console are sent to the master, and as mentioned earlier, the signals pass through the communication blocks. The gating signals are generated based upon the inputs received from the console. The gating signals are routed to the physical inverter through the digital output port(s) of the simulator, the same signals will be given to the eHS solver. The virtual model will run on the FPGA and uses a Simulink model (.mdl) file of only the converter bridge as a reference. This is a separate file and must be kept in the same directory containing the main model; this directory should also contain the *bit-stream* and other relevant files for the project. The name of the model must be fed to the eHS and then it will detect and obtain the required 'netlist' details from the model. The gating signals can be routed through a digital input port or internally from the block that generates the gating signals. To ensure that the same gating pulses are received by the physical and virtual converter, the

gating signals are routed back from the physical converter to a digital input port from which eHS would receive the gating inputs. Figure 3.19 shows the 'eHS Gen3' solver block as it appears in RT-Lab.

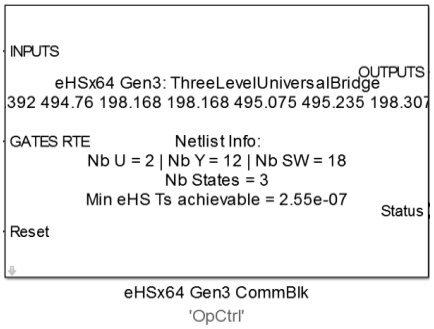


Figure 3.19. The eHS Solver Block

Additionally, an analogue output port has to be configured so that the output of the virtual model evaluated by the eHS can be read. The configuration of the input and output port would depend upon the selection of a *bit-stream* that would determine the port assignments, size of the ports and their subsections. The simulation time shall be set to infinity and when the model is built, loaded and executed, only the console subsystem window shall be accessible at the host computer or workstation. The console will appear as shown in Figure 3.20 when the simulation is ongoing. An enable switch is provided in the console to turn the gating pulses ON or OFF while the simulation is running. To end the simulation the model should be *reset* from the RT-Lab window, stopping the simulation from the console window will only stop the console but the overall model would still be running.

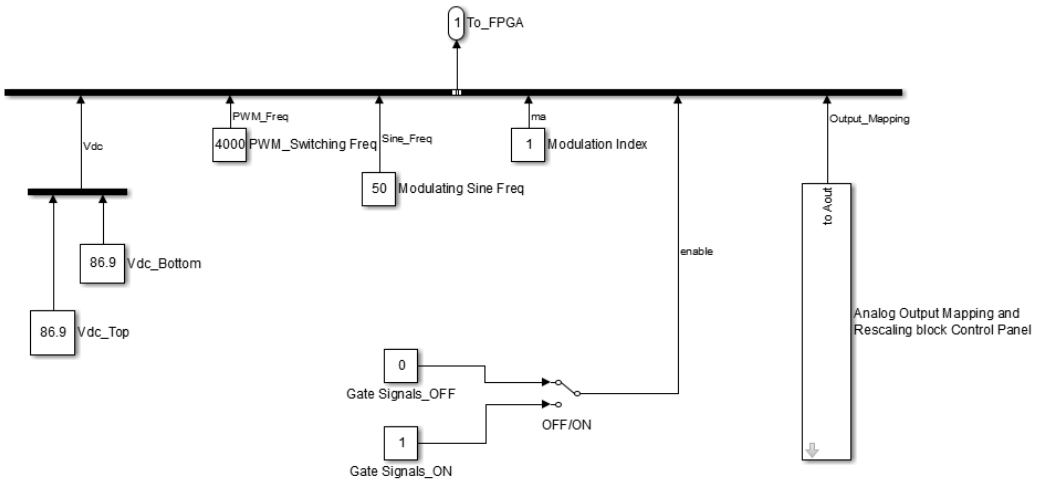


Figure 3.20. The Console Window Available during Real-time Simulation

A specific naming convention must be followed [32] for the sources, switches and the measurements in the model provided to eHS so that it can read them properly, Table 9 provides some details of the naming convention used. Table 10 shows that names of the elements in the reference model. The parameter settings window of the eHS solver as shown in Figure 3.21 and Figure 3.22 gives details as how the solver shall be configured prior to the loading of the model to the simulator. It is yet again very important that the reference model is contained in the same directory as the other model files, else the eHS shall not be able to detect the file and the simulation would not proceed.

Table 9. Naming Convention of the Elements in the Reference Model

Element	Naming Convention
Sources (Dependent)	U01, U02, U03…..etc
Switches	SW01, SW02, SW03…..etc
Measurements	Y01,Y02,Y03…..etc

The output of the virtual converter shall be obtained in the same order as the assigned measurements. If a phase voltage V_{ab} measurement is assigned as ‘Y01’ then the first pin of the configured analogue output port would produce this output. It is also necessary that the ‘0’ in the naming of the elements is not ignored. As discussed earlier, the gating pulses will be looped back from the real inverter, Figure 3.23 shows the switch details in the virtual inverter and the indices of the digital input port of the simulator to which the gate pulses shall be fed to.

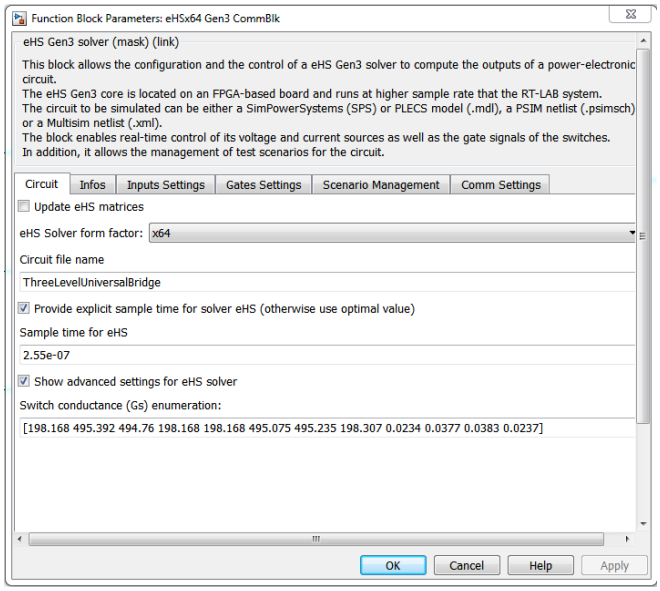


Figure 3.21. The Parameter Setting Window of the eHS Solver Block

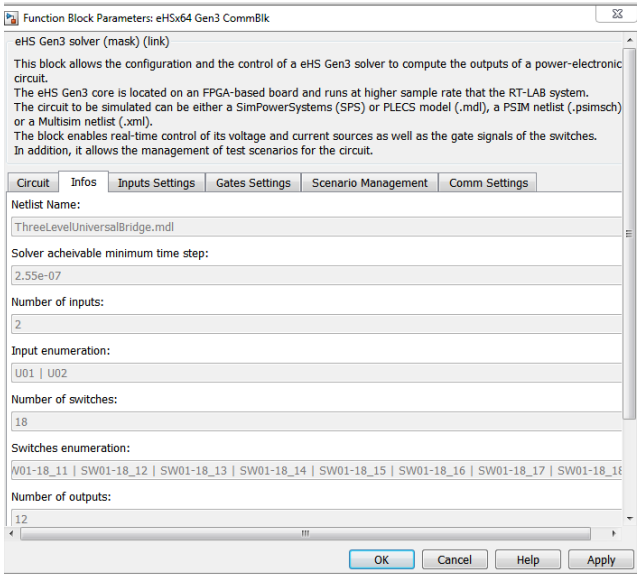


Figure 3.22. Parameter Window of the eHS Solver Block Showing the Netlist Details Extracted by the Solver

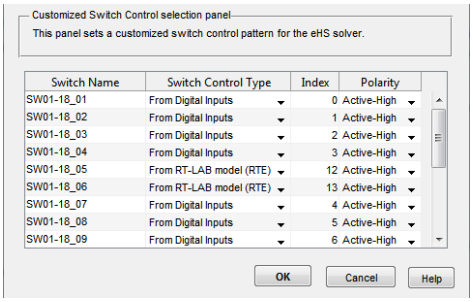


Figure 3.23. Window Showing the Gate Settings for the eHS Solver

Table 10. Naming Convention of the IGBT's in the Reference Model

Nomenclature of the IGBTs/Anti-Parallel Diodes					
Leg 1		Leg 2		Leg 3	
IGBT/ *Anti-parallel Diodes		IGBT/ *Anti-parallel Diodes		IGBT/ *Anti-parallel Diodes	
SW01	D_{a1}	SW07	D_{b1}	SW13	D_{c1}
SW02	D_{a2}	SW08	D_{b2}	SW14	D_{c2}
SW03	D_{a3}	SW09	D_{b3}	SW15	D_{c3}
SW04	D_{a4}	SW10	D_{b4}	SW16	D_{c4}
Clamping Diodes for Leg 1		Clamping Diodes for Leg 2		Clamping Diodes for Leg 3	
SW05(D_1)	SW06 (D_2)	SW11 (D_3)	SW12 (D_4)	SW17 (D_5)	SW18 (D_6)

**The naming convention does not apply to antiparallel diodes; the naming shown is just for identification purposes*

3.3.2 Gating Pulse Generation in RT Lab

The gate pulse generation for the three-level inverter has been discussed in Section 3.2.3. Figure 3.24 shows the model used for generation of the reference sinusoidal waves. These reference sine waves are then compared with the triangular carrier and gate pulses are obtained. These gating pulses have to be routed to the digital output ports of the simulator. The gate pulses are first conditioned using a RTE converter and forwarded to output control boards via a RTE event detector as shown in Figure 3.25.

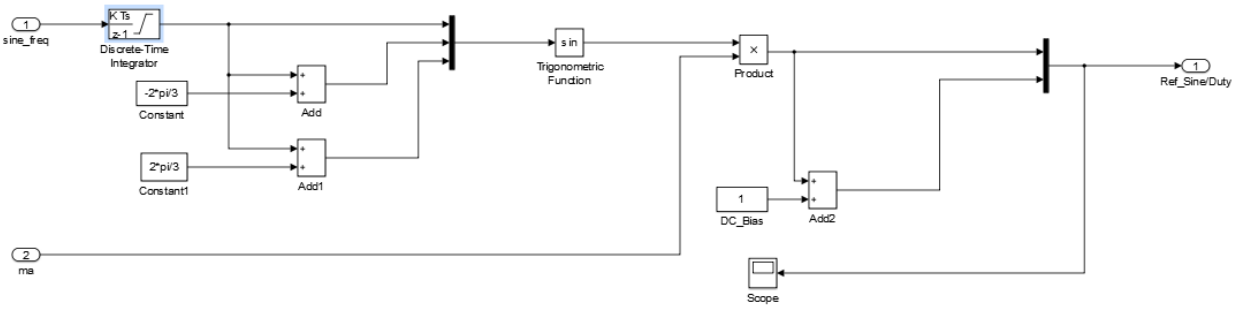


Figure 3.24. Reference Sine Generation in RT Lab

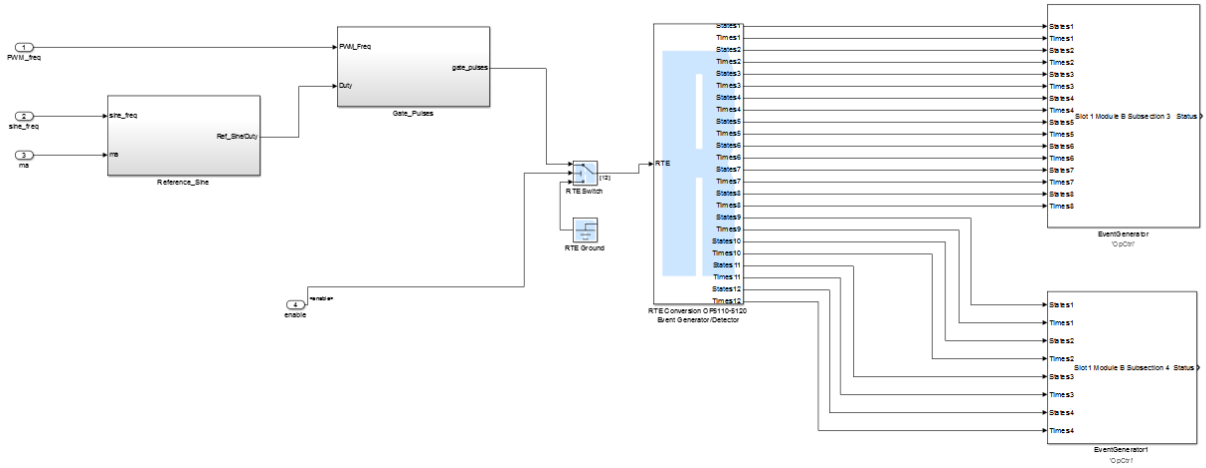


Figure 3.25. Routing of the Gate Pulses to the Digital Output Boards

3.3.3 Experimental Setup

Block diagram of the model built for the real-time simulation of the three-level inverter is given in Figure 3.26.

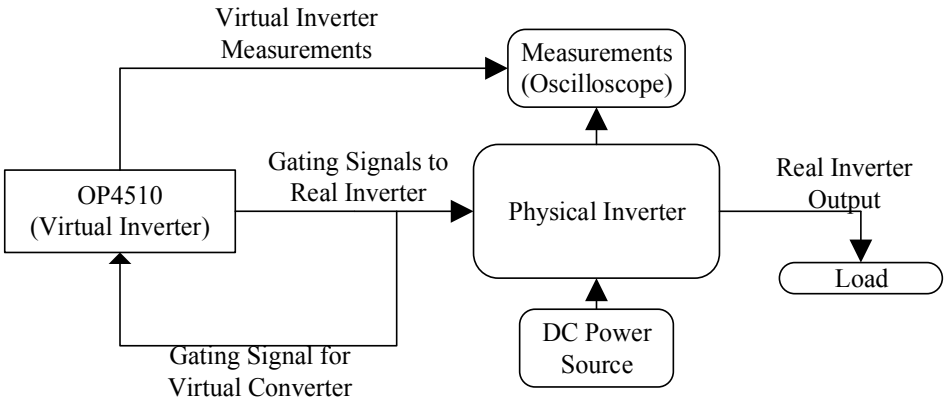


Figure 3.26. Block Diagram of the Setup for the RTS of a Three-level Inverter

A physical test setup of a three-level NPC inverter was prepared for the validation work. The inverter was assembled using three-level NPC-1 modules of Infineon make with a maximum DC blocking capacity of 650 V. A DB37 port is used to interface the inverter with the OPAL-RT OP4510 real-time simulator. Figure 3.27 to Figure 3. 31 shows some details of the setup, a few parameters of various components are tabulated in Table 11.

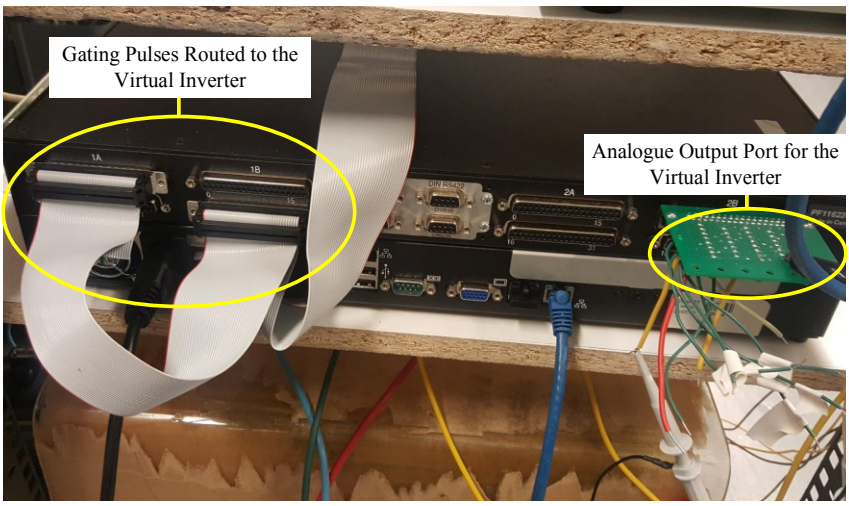


Figure 3.27. Rear Side of the OPAL-RT OP4510 Simulator Showing the Digital Input/output Ports and the Analogue Port

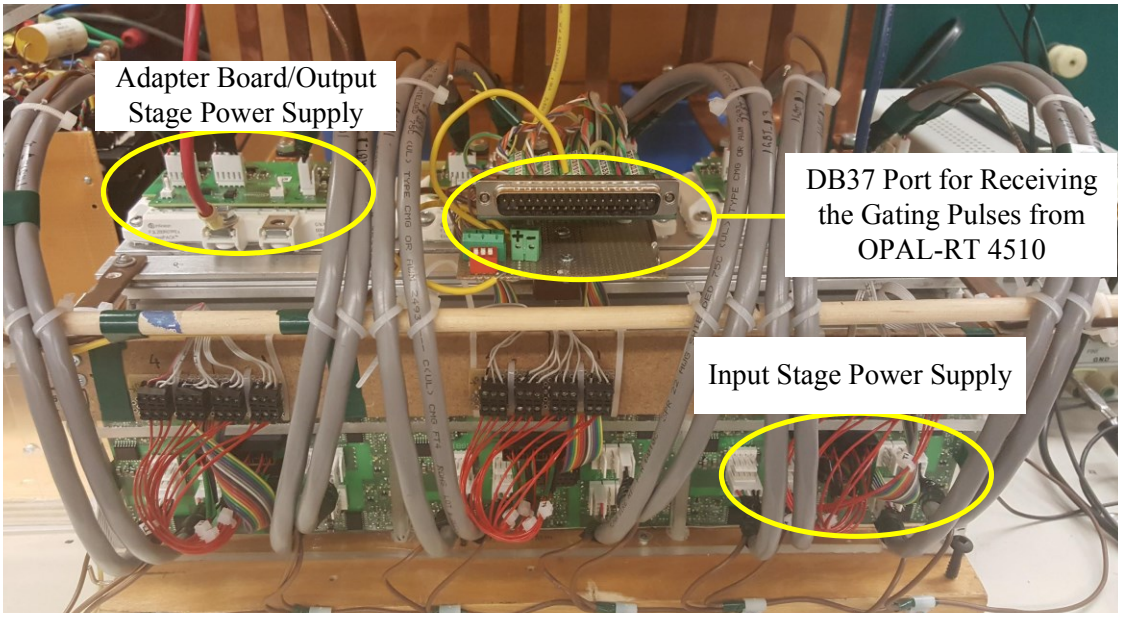


Figure 3.28. Front Side of the Three-level Inverter

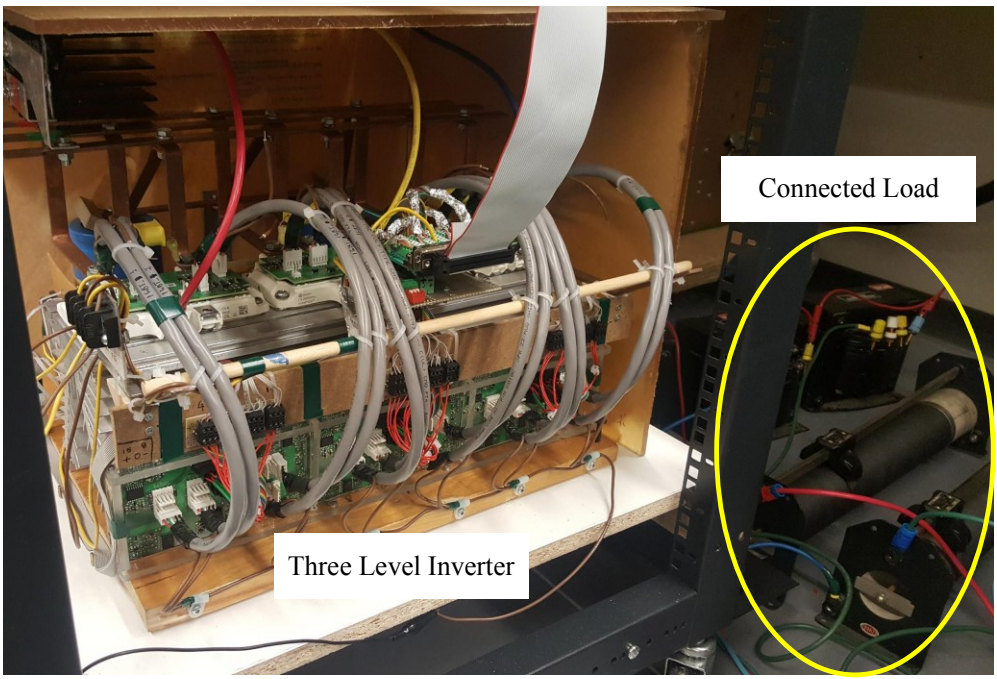


Figure 3.29. The Connected RL Load to the Inverter

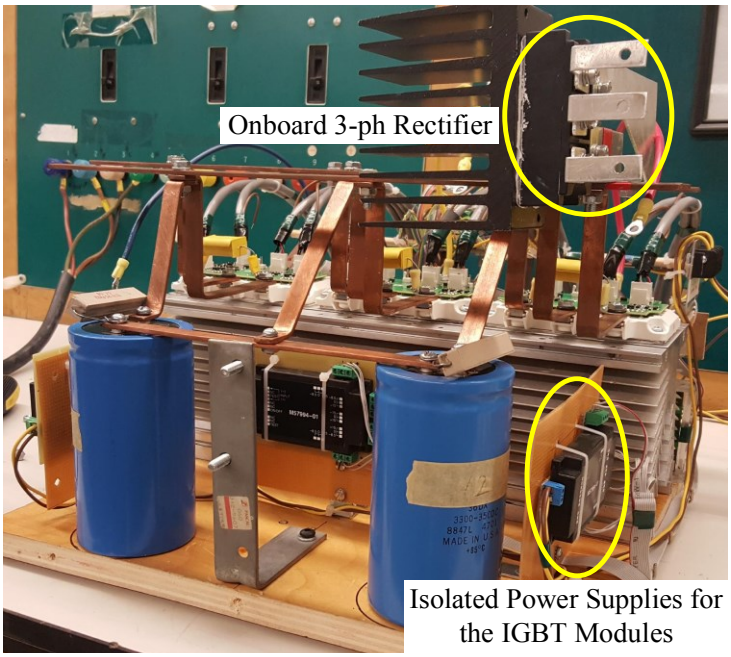


Figure 3.30. Rear Side of the Three-level Inverter

Table 11. Details of Some of the Components in the 3 L NPC Inverter

Item Name	Make	Parameter	Value		
IGBT Module (NPC 1)	Infineon (F3L200R07PEF)	Collector Emitter Voltage, (V_{CES})	650 V		
		Continuous DC Collector Current, (I_C)	200 A		
		Total Power Dissipation	680 W		
		Gate Threshold Voltage	Min 5.0 V	Typ. 5.8 V	Max 6.8 V
Evaluation Driver Board	Infineon (F3L020E07_F-P_Eval)	Input Supply	15V, 0V, -8V		
Adapter Board	Infineon (MA3L080E07_Eval)	Max DC Supply Voltage (V_{DC})	+/- 20V		
		Continuous Output Current (I_a)	8 A		
		Max PWM Frequency	60 KHz		
Isolated Power Supply	Powerex (M57994-01)	Input Voltage	10-32 V		
		No of Isolated Output	5 4x(+15, 0, -8.5 V, 100mA) 1x(+15/-15 V, 200mA)		

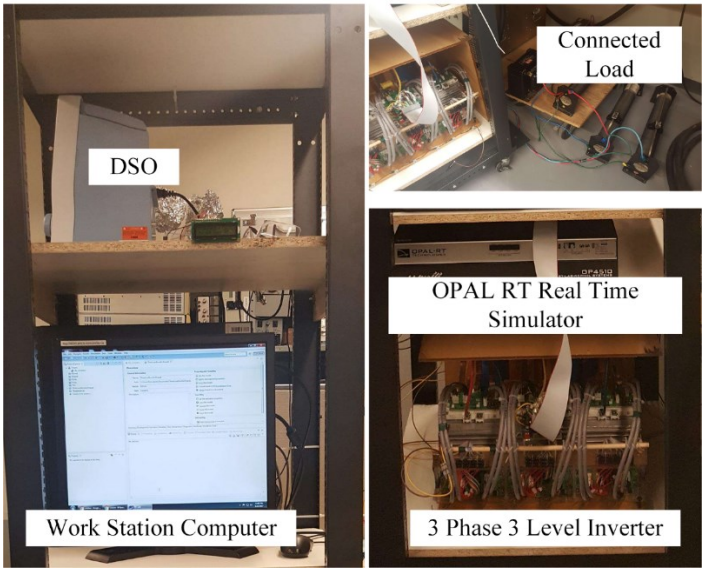


Figure 3.31. Setup for the Validation of Three-level Inverter

3.4 Expressions for Instantaneous Voltages

Instantaneous Pole Voltages, Line to Line Voltages and Line to Neutral Load Voltages: The instantaneous pole voltages are given in Table 12.

Table 12. Instantaneous Pole Voltages

Pole Voltage	Available Voltages		
V_{RO}	+0.5 V_{dc}	0 V_{dc}	-0.5 V_{dc}
V_{YO}	+0.5 V_{dc}	0 V_{dc}	-0.5 V_{dc}
V_{BO}	+0.5 V_{dc}	0 V_{dc}	-0.5 V_{dc}

Line to Line voltage

The expressions for the modulating sine waves are shown in equations (3.1) to (3.3).

$$m_R = (V_m/V_p)\ sin\ (\omega t) = m_a\ sin\ (\omega t) \quad (3.1)$$

$$m_Y = (V_m/V_p)\ sin\ (\omega t - 120°) = m_a\ sin\ (\omega t - 120°) \quad (3.2)$$

$$m_B = (V_m/V_p)\ sin\ (\omega t - 240°) = m_a\ sin\ (\omega t - 240°) \quad (3.3)$$

The average voltages of the pole voltages can be obtained as in (3.4) to (3.6) and the instantaneous average line voltages can be found using expressions from (3.7) to (3.9).

$$V_{RO} = m_a\ (V_{dc}/2)\ sin\ (\omega t) \quad (3.4)$$

$$V_{YO} = m_a\ (V_{dc}/2)\ sin\ (\omega t - 120°) \quad (3.5)$$

$$V_{BO} = m_a\ (V_{dc}/2)\ sin\ (\omega t - 240°) \quad (3.6)$$

$$V_{RY} = V_{RO} - V_{YO} \quad (3.7)$$

$$V_{YB} = V_{YO} - V_{BO} \quad (3.8)$$

$$V_{BR} = V_{BO} - V_{RO} \quad (3.9)$$

The RMS value of the line voltage can be obtained as shown in expressions (3.10) to (3.13).

$$V_{RY} = m_a\left(\frac{V_{dc}}{2}\right)\sin\omega t - m_a\left(\frac{V_{dc}}{2}\right)\sin(\omega t - 120°) \quad (3.10)$$

$$V_{RY} = m_a\left(\frac{V_{dc}}{2}\right)\left[\frac{3}{2}\sin\omega t + \frac{\sqrt{3}}{2}\cos\omega t\right] \quad (3.11)$$

$$V_{RY_{rms}} = m_a\left(\frac{V_{dc}}{2}\right)\frac{\left[\int_0^{\pi}\left(\frac{3}{2}\sin\omega t + \frac{\sqrt{3}}{2}\cos\omega t\right)^2 d(\omega t)\right]^{0.5}}{\pi^{0.5}} \quad (3.12)$$

$$V_{RY_{rms}} = V_{YB_{rms}} = V_{BR_{rms}} = m_a \frac{\sqrt{3}}{\sqrt{2}} \frac{V_{dc}}{2} = m_a 0.6124 V_{dc} \quad (3.13)$$

3.5 Validation of a Virtual Inverter with a Physical Three-level NPC Inverter

Validation of the three-level three-phase inverter was done by comparing the results obtained from the FPGA based electrical hardware solver (eHS), Ode 23tb (stiff) solver in SimScape Power Systems (SPS) and a physical setup. Tests were done with 1.0 PF, 0.95 PF and 0.9 PF, the load parameters are provided in Table 13; Table 14 provides the parameters of the circuit which was shown in Figure 3.1. The measurements of the real inverter were taken using a digital storage oscilloscope and a Fluke Digital Multimeter, the output of the virtual inverter is available in a configured analogue output port discussed earlier. This port is essentially a Digital to Analogue Converter (DAC) that converts the digital output from the FPGA simulating the virtual inverter to analogue output, these output can be measured by a means of an external oscilloscope as the simulator does not have a built in facility to display the simulation output directly. A Fluke make clamp meter was also used to measure the line currents of the real inverter.

Section 2.4 discussed some limitations of the Pejovic switch model, among which were the losses occurring in the model during commutation. The optimization of G_s parameters achieved by GsGui2 is based on the minimization of the error between eHS results and SPS benchmark results. In addition to this; a Loss Compensation Algorithm (LCA) [33] has also been implemented by OPAL-RT to minimize artificial losses and, consequently, reduce the effect of numerical oscillations. The effect of LCA has already been analyzed in [27], and keeping in view of the advantages that LCA can bring in, all the validation work with RTS in this thesis, have LCA enabled in them.

Table 13. Details of the Load Connected for Different Power Factors

Unity PF		**PF = 0.95**		**PF = 0.9**	
R (Ω)	X_L (Ω)	R (Ω)	L (H)	R (Ω)	L (H)
30.5	--	30.5	32e-03	20.75	32e-03

Table 14. Parameters Set for the Virtual and the Physical Inverter

Parameter	Label	Value
Switching Frequency	PWM_Freq	2 kHz
DC Link Voltage	Vdc_Source	173.8 V
IGBT ON Resistance	R_{on} (S01,…S12)	1e-3 Ω
IGBT Snubber Resistance	R_s (S01,…S12)	1e5 Ω
IGBT Snubber Capacitance	C_s (S01,…S12)	inf
Modulating Frequency	f_{ref}	50 Hz

3.5.1 Inverter Operation at Unity Power Factor

Figure 3.32 shows the results from RTS of the three-level NPC inverter supplying a load with unity power factor. The switch conductance parameters obtained from GsGui2 were G_{s1} (outer switch) = 0.024166 and G_{s2} (inner switch) = 0.012083. A close up snap shot of the output of the physical inverter is shown in Figure 3.33.

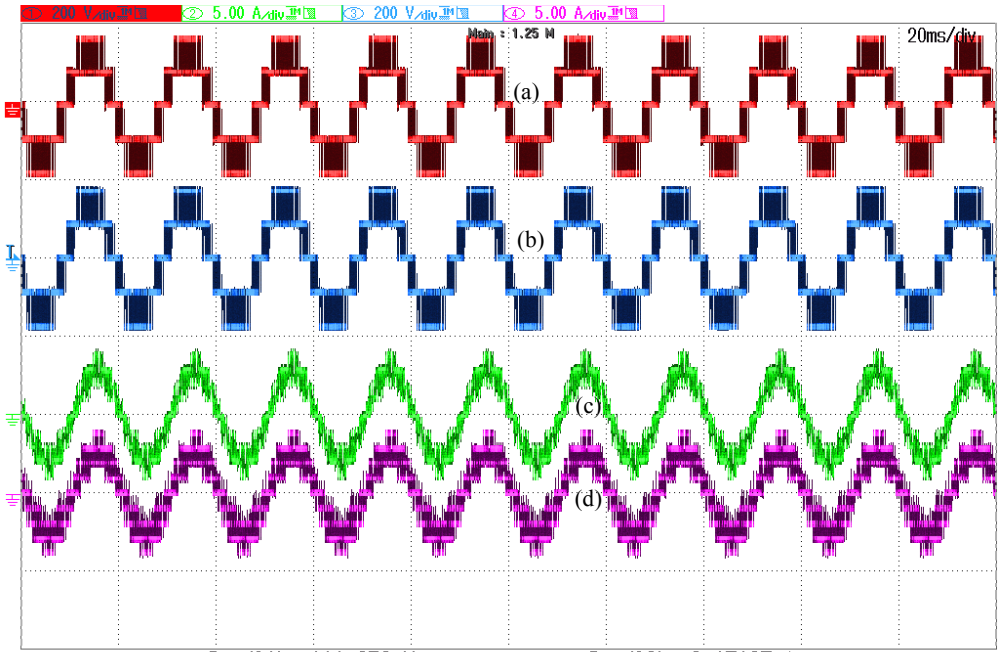


Figure 3.32. Test Results from RTS of 3 L NPC Inverter with Unity Power Factor Load; (a) Line Voltage (V_{RY}) of the Physical Inverter; (b) Line Voltage (V_{RY}) of the Virtual Inverter; (c) Line Current (I_R) of the Physical Inverter; (d) Line Current (I_R) of Virtual Inverter

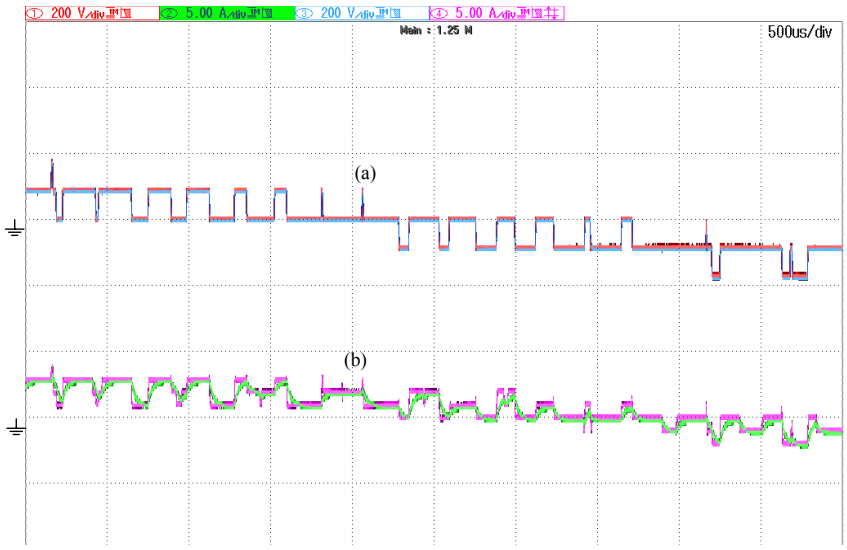


Figure 3.33. Close Up View of Superimposed Results from RTS of 3 L NPC Inverter with Unity Power Factor Load; (a) Line Voltage (V_{RY}) of the Physical and Virtual Inverter; (b) Line Current (I_R) of the Physical and Virtual Inverter

3.5.2 Inverter Operation at 0.95 Power Factor

Figure 3.34 shows the results from the RTS of the three-level NPC inverter supplying a 0.95 power factor load. The switch conductance parameters obtained from GsGui2 were G_{s1} (outer switch) = 0.021864 and G_{s2} (inner switch) = 0.010932. The line voltage and currents of the real inverter and the virtual one are very similar to each other. The readings of the measuring instruments are placed in Table 15.

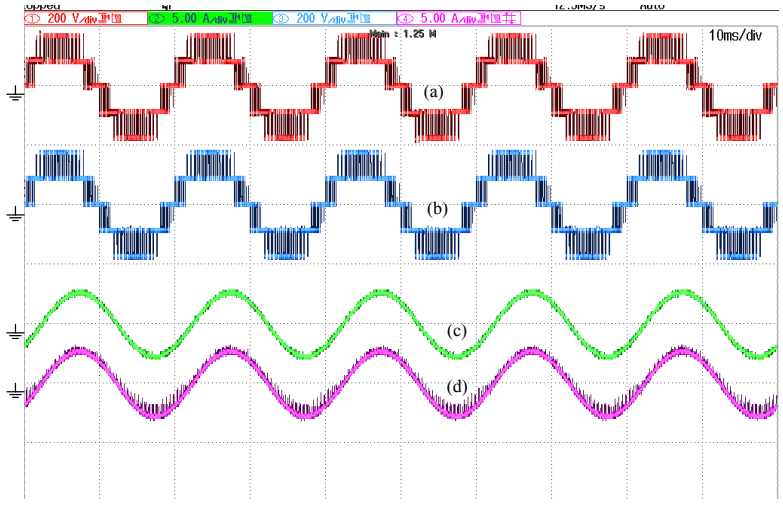


Figure 3.34. Test Results from RTS of 3 L NPC Inverter with 0.95 Power Factor Load; (a) Line Voltage (V_{RY}) of the Physical Inverter; (b) Line Voltage (V_{RY}) of the Virtual Inverter; (c) Line Current (I_R) of the Physical Inverter; (d) Line Current (I_R) of Virtual Inverter

3.5.3 Inverter Operation at 0.9 Power Factor

Figure 3.35 shows the results from RTS of the three-level NPC inverter supplying a load with 0.9 power factor. The switch conductance parameters obtained from GsGui2 were G_{s1} (outer switch) = 0.030495 and G_{s2} (inner switch) = 0.015247. A close up snap shot of the output of the physical inverter is shown in Figure 3.36. Yet again the results from the real inverter and the virtual model are quite similar. The results are tabulated in the measurements Section 3.5.4.

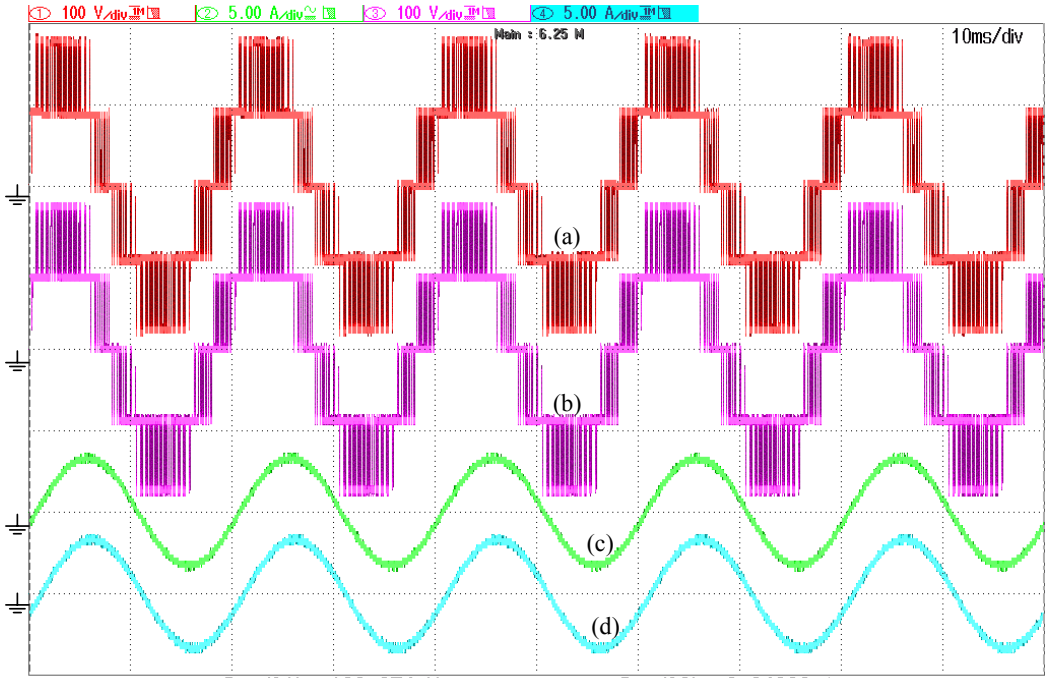


Figure 3.35. Test Results from RTS of 3 L NPC Inverter with 0.9 Power Factor Load; (a) Line Voltage (V_{RY}) of the Physical Inverter; (b) Line Voltage (V_{RY}) of the Virtual Inverter; (c) Line Current (I_R) of the Physical Inverter; (d) Line Current (I_R) of Virtual Inverter

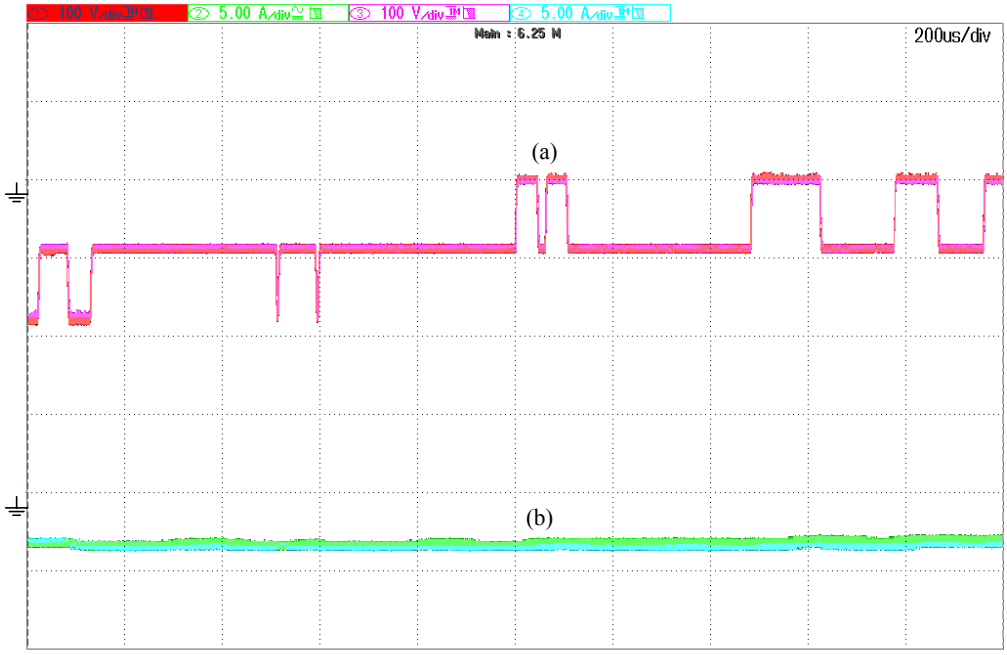


Figure 3.36. Close-up Superimposed View of Results from RTS of 3 L NPC Inverter with 0.9 Power Factor Load; (a) Line Voltage (V_{RY}) of the Physical and Virtual Inverter; (b) Line Current (I_R) of the Physical and Virtual Inverter

3.5.4 Measurements:

During the real-time simulation of the three-level inverter, the same gating pulses were shared by the virtual and the real inverter. The output of both the real and the virtual inverter were measured by an oscilloscope. The output of the real inverter was also measured using a multimeter and the results are provided in Table 15.

Table 15. Output of the Real Inverter Measured Using a Voltmeter and a Clamp-meter

Output RMS Voltage of Real Inverter (Voltmeter)			
$V_{(RY)}$	$V_{(YB)}$	$V_{(BR)}$	PF
110.00 V	109.78 V	110.35 V	1
111.39 V	111.20 V	110.82 V	0.95
102.65 V	103.11 V	102.85 V	0.9
Output RMS Current of Real Inverter (Clamp-meter)			
I_R	I_Y	I_B	PF
2.17 A	2.0 A	2.1 A	1
1.9 A	1.9 A	1.8 A	0.95
2.38 A	2.36 A	2.40 A	0.9

Table 16 states the output of the virtual inverter running on the FPGA of the real-time simulator, Table 17 compares the output of both the real and virtual inverter. The details of the oscilloscope is given in Table 18, and the details of the real-time simulator are given in Table 19.

Table 16. Output of the Virtual Inverter Measured Using a Digital Storage Oscilloscope

Output RMS Voltage (Virtual Inverter)		**Output RMS Current (Virtual Inverter)**	
V_{RY}	PF	I_R	PF
110.32 V	1	2.1 A	1
112.33 V	0.95	1.9 A	0.95
102.39 V	0.9	2.37 A	0.9

Table 17. Results of the Real-time Simulation Compared with Different Solvers

Comparison between RMS values of Real Inverter and Virtual Inverter								
	SPS Inverter		Real Inverter		Virtual Inverter (eHS)		PSIM Inverter	
PF	Voltage (V_r)	Current (I_r)	Voltage (V_r)	Current (I_r)	Voltage (V_r)	Current (I_r)	Voltage (V_r)	Current (I_r)
1	111.80 V	2.131 A	110 V	2.17 A	110.32 V	2.15 A	112.26 V	2.132 A
0.95	111.89 V	1.903 A	111.39 V	1.9 A	112.33 V	1.91 A	112.32 V	1.911 A
0.9	101.87 V	2.368 A	102.65 V	2.38 A	102.39 V	2.37 A	101.86 V	2.369 A

Table 18. Oscilloscope Settings

Oscilloscope Settings		
Make: Yokogawa		
Model: DLM2024		
Bandwidth: 200MHz		
Probe Settings		
Channel	Measuring	Attenuation
CH1	Voltage (real-inverter)	1000:1
CH2	Current (real-inverter)	100:1
CH3	Voltage (virtual-inverter)	1000:1
CH4	Current (virtual-inverter)	100:1
Isolated Voltage Probe Attenuation: 100:1		

Table 19. Details of the Real-time Simulator

Name of Real-time Simulator	OPAL-RT/OP4510
Digital Output port Used (For Gating Signals):	1 B (Group 1/Section B)
Digital Input Port Used:	1 A (Group 1/Section A)
Analogue Output Port Used:	2 B (Group 2/Section B)
Gain for CH0 of Analogue Outport 1A	1/100
Gain for CH1 of Analogue Outport 1A	1/10

3.6 Inverter Operation with Unbalanced Load

The inverter was tested with the parameters given in Table 20, it can be seen that the load is now unbalanced but the G_s used shall be for a balanced circuit obtained from the eHS

optimization tool *GsGui2*. The line currents shall be limited to below 3.5 A, so as not to exceed the maximum current rating of the load used in the real inverter.

Table 20. Inverter Parameters for Inverter Operation with Unbalanced Load

Parameter		**Value**
PWM_Freq		4 kHz
Vdc_Source		173.8 V
R_{on} (S01,…S12)		1e-3 Ω
R_s (S01,…S12)		1e5 Ω
C_s (S01,…S12)		inf
f_{ref} (sine frequency)		50 Hz
R-Phase	R	15 Ω
	L	32mH
Y-Phase	R	15 Ω
	L	32mH
B-Phase	R	70 Ω
	L	32mH

The results from the RTS of the three-level NPC inverter supplying the unbalanced load as mentioned earlier are provided in Table 21. The optimization tool needs two inputs for evaluating the G_s parameter and they are the input DC voltage and line current respectively. Since during the unbalanced conditions, line currents will not be similar, providing different line current values to the tool will result in different G_s values. Choosing the higher values of current resulted in switch conductance parameters with which, the eHS produced very close results with those of SPS's, but choosing the lower values of line current, produced a deviation between the results of the solvers.

The results from validation of a two-level inverter done in [27], suggests that when the inverter is connected to an unbalanced load, the SPS, eHS and the real inverter currents do not match using G_s values meant for rated conditions. The unbalance in the load introduced here, is more than what was done for the two-level inverter in [27], the resistive load in the B-phase is almost 5 times smaller than the other two phases. This was done to create as much unbalance as possible and to study the behavior of G_s which were optimized for rated conditions. Figure 3.37 to Figure 3.39 shows the waveforms of the line voltages and currents from the validation test.

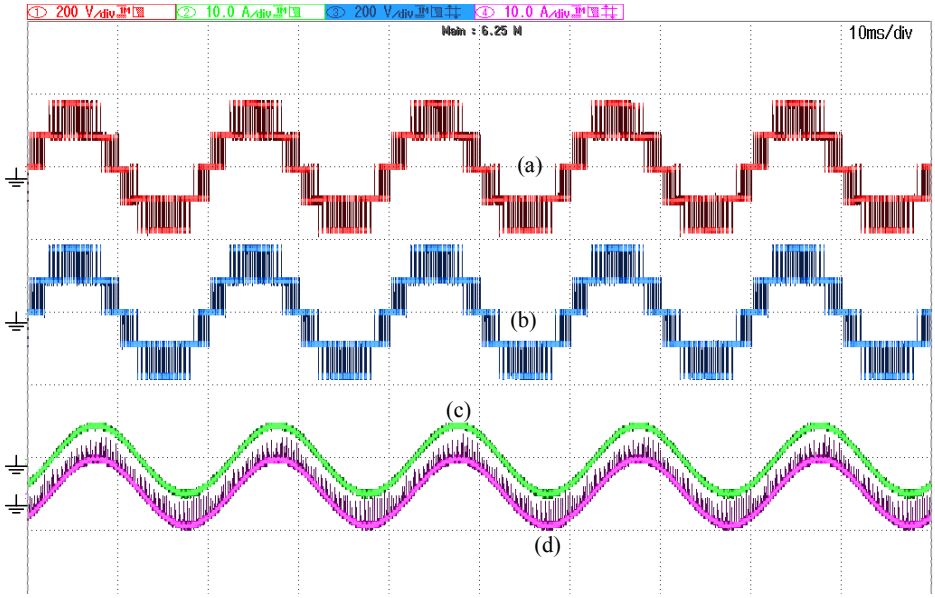


Figure 3.37. Test Results from RTS of 3 L NPC Inverter with an Unbalanced Load; (a) Line Voltage (V_{RB}) of the Physical Inverter; (b) Line Voltage (V_{RB}) of the Virtual Inverter; (c) Line Current (I_R) of the Physical Inverter; (d) Line Current (I_R) of Virtual Inverter

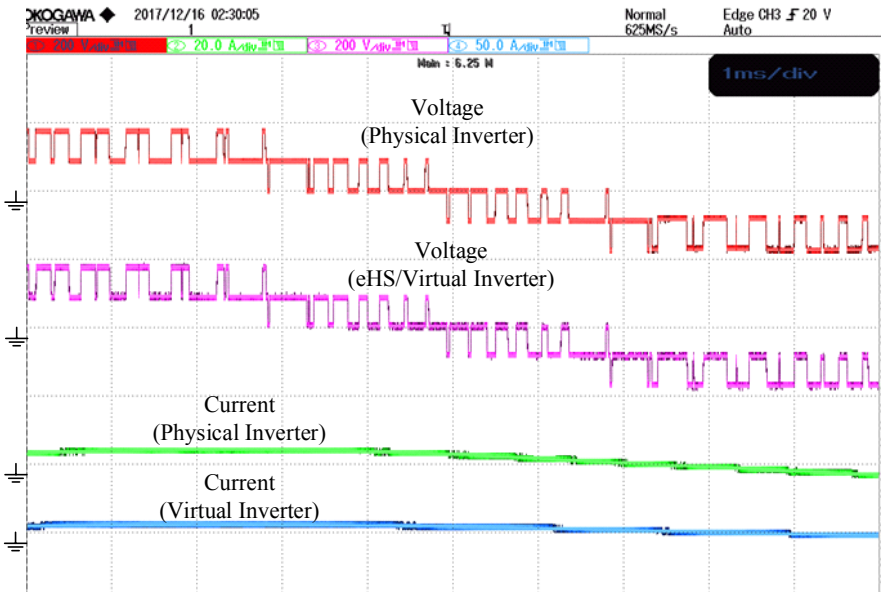


Figure 3.38. Zoomed Waveforms of the Line Voltages and Currents (R-Phase)

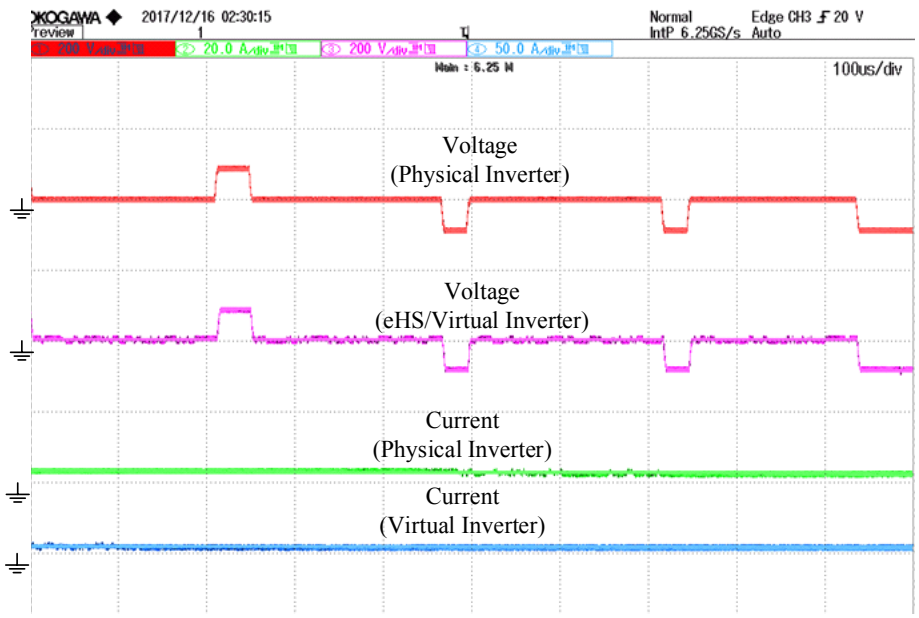


Figure 3.39. Greater Zoomed Waveforms of the Line Voltages and Currents

Table 21. Comparison of the Results (RMS output) of RTS of the 3 L NPC Inverter with Unbalanced Load

Measurements using G_s by taking larger value of Line Current (G_{s1} = 0.036571 G_{s2} = 0.018285)					
Measurement	**SPS**	**Virtual Inverter (eHS)**	**Real Inverter**	**% difference SPS vs eHS**	**% difference SPS vs Real**
V_{R-Y} (RMS)	111.8 V	111.92 V	111.04 V	0.11 %	0.68 %
V_{Y-B} (RMS)	112.3 V	112.30 V	112.50 V	0.18 %	0.18 %
V_{B-R} (RMS)	111.7 V	112.06 V	111.60 V	0.32 %	0.09 %
I_R (RMS)	3.178 A	3.19 A	3.20 A	0.38 %	0.69 %
I_Y (RMS)	2.744 A	2.75 A	2.70 A	0.22 %	1.60 %
I_B (RMS)	1.156 A	1.164 A	1.17 A	0.69 %	1.21 %
Measurements using G_s by taking smaller value of Line Current (G_{s1} = 0.013303 G_{s2} = 0.0066513)					
Measurement	**SPS**	**Virtual Inverter (eHS)**	**Real Inverter**	**% difference SPS vs eHS**	**% difference SPS vs Real**
V_{R-Y} (RMS)	111.8 V	112.80 V	111.35 V	0.89 %	0.40 %
V_{Y-B} (RMS)	112.3 V	111.96 V	111.90 V	0.30 %	0.36 %
V_{B-R} (RMS)	111.7 V	111.93 V	112.50 V	0.21 %	0.72 %
I_R (RMS)	3.178 A	3.186 A	3.2 A	0.25 %	0.69 %
I_Y (RMS)	2.744 A	2.754 A	2.8 A	0.36 %	2.04 %
I_B (RMS)	1.156 A	1.164 A	1.17 A	0.69 %	1.21 %
Measurements using G_s by taking rated value of Line Current (G_{s1} = 0.023015 G_{s2} = 0.011507)					
Measurement	**SPS**	**Virtual Inverter (eHS)**	**Real Inverter**	**% difference SPS vs eHS**	**% difference SPS vs Real**
V_{R-Y} (RMS)	111.8 V	112.14 V	110.15 V	0.30 %	1.48 %
V_{Y-B} (RMS)	112.3 V	112.06 V	110.52 V	0.21 %	1.59 %
V_{B-R} (RMS)	111.7 V	111.94 V	113.60 V	0.21 %	1.70 %
I_R (RMS)	3.178 A	3.192 A	3.2 A	0.44 %	0.69 %
I_Y (RMS)	2.744 A	2.76 A	2.7 A	0.58 %	1.60 %
I_B (RMS)	1.156 A	1.182 A	1.17 A	2.25 %	1.21 %

3.7 Inverter Operation with an Unbalanced Load and Reduced DC link voltage

The DC link voltage was lowered to 114.3 V and the same unbalanced load was maintained as in the previous section, the parameters are provided in the Table 22. This was done to study the effects of alteration of the DC link voltage in eHS and also reduce the current stress on the equipment which were subjected to near maximum continuous rating in the previous test. The outcome of the test are tabulated in Table 23, it is seen that the virtual inverter's line currents were a little different from those of SPS. Figure 3.40 shows the output of the real and virtual inverter. Figure 3.41 compares the real and virtual inverter output using G_s values obtained by using the smaller line current. Zoomed in waveforms of the line voltages and line currents of the real and the virtual inverter are shown in Figure 3.42 and Figure 3.43, the output of the Y-phase of both the inverters is shown in Figure 3.44.

Table 22. Inverter Parameter for Inverter Operation with Unbalanced Load and Reduced DC Link Voltage

Parameter		**Value**
PWM_Freq		4 kHz
Vdc_Source		114.3 V
R_{on} (S01,…S12)		1e-3 Ω
R_s (S01,…S12)		1e5 Ω
C_s (S01,…S12)		inf
f_{ref} (sine frequency)		50 Hz
R-Phase	R	15 Ω
	L	32mH
Y-Phase	R	15 Ω
	L	32mH
B-Phase	R	70 Ω
	L	32mH

Table 23. Comparison of the Results (RMS output) of RTS of the 3 L NPC Inverter with Unbalanced Load

Measurements using G_s by taking larger value of Line Current (G_{s1} = 0.013303, G_{s2} = 0.0066513)					
Measurement	SPS	Virtual Inverter (eHS Online)	Real Inverter	% difference SPS vs eHS	% difference SPS vs Real
V_{R-Y} (RMS)	72.80 V	73.87 V	72.13V	1.47 %	0.92 %
V_{Y-B} (RMS)	73.43 V	73.78 V	72.69 V	0.48 %	1.01 %
V_{B-R} (RMS)	72.78 V	73.43 V	71.65 V	0.89 %	1.55 %
I_R (RMS)	2.07 A	2.03 A	2.1 A	1.93 %	1.45 %
I_Y (RMS)	1.79 A	1.824 A	1.8 A	1.90 %	0.56 %
I_B (RMS)	0.752 A	0.78 A	0.76 A	3.72 %	1.06 %
Measurements using G_s by taking smaller value of Line Current (G_{s1} = 0.0086536 G_{s2} = 0.0043268)					
Measurement	SPS	Virtual Inverter (eHS Online)	Real Inverter	% difference SPS vs eHS	% difference SPS vs Real
V_{R-Y} (RMS)	72.80 V	73.72 V	72.15 V	1.26 %	0.89 %
V_{Y-B} (RMS)	73.43 V	73.87 V	72.50 V	0.60 %	1.27 %
V_{B-R} (RMS)	72.78 V	73.81 V	72.55 V	1.42 %	0.32 %
I_R (RMS)	2.07 A	2.11 A	2.1 A	1.93 %	1.45 %
I_Y (RMS)	1.79 A	1.825 A	1.8 A	1.96 %	0.56 %
I_B (RMS)	0.752 A	0.778 A	0.76 A	3.46 %	1.06 %

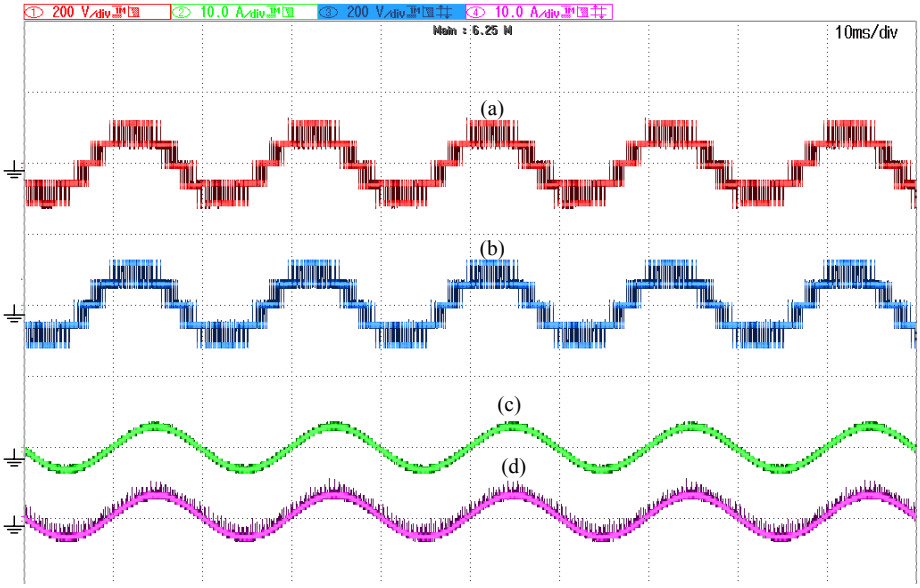


Figure 3.40. Test Results from RTS of 3 L NPC Inverter Feeding an Unbalanced Load; (a) Line Voltage (V_{RY}) of the Physical Inverter; (b) Line Voltage (V_{RY}) of the Virtual Inverter; (c) Line Current (I_R) of the Physical Inverter; (d) Line Current (I_R) of Virtual Inverter

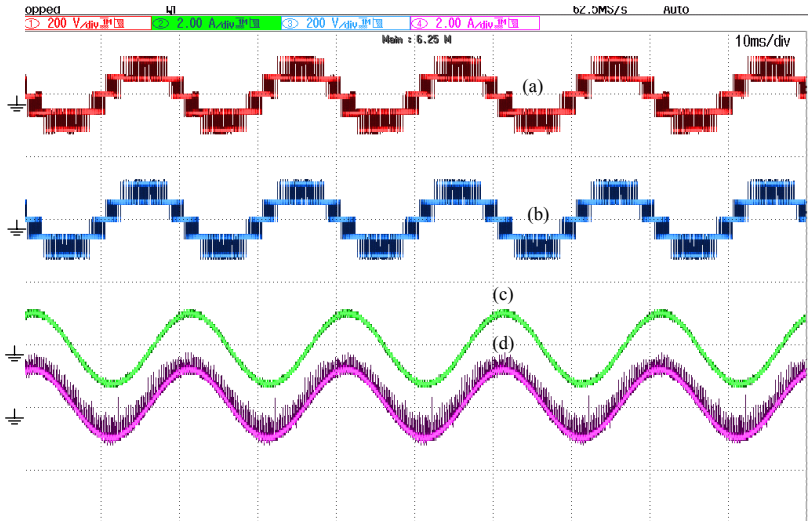


Figure 3.41. Test Results from RTS of 3 L NPC Inverter Feeding an Unbalanced Load; (a) Line Voltage (V_{RY}) of the Physical Inverter; (b) Line Voltage (V_{RY}) of the Virtual Inverter; (c) Line Current (I_B) of the Physical Inverter; (d) Line Current (I_B) of Virtual Inverter for G_{s1} = 0.0086536 and G_{s2} = 0.0043268

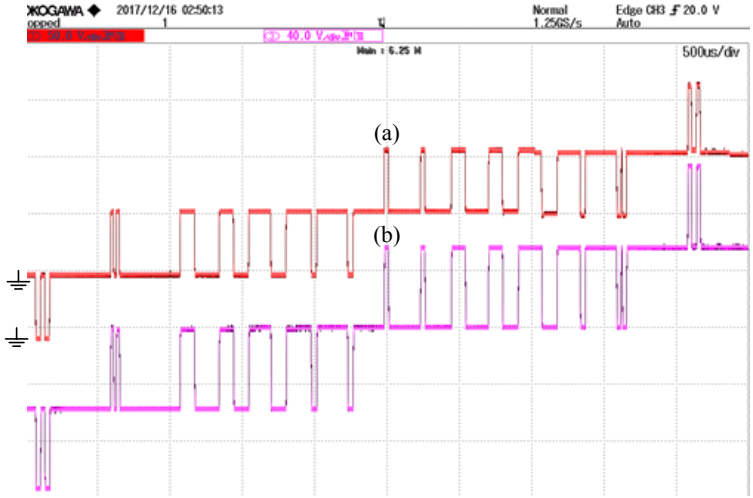


Figure 3.42. Zoomed in Waveform of the Line Voltage, V_{RY} (a) Physical Inverter and (b) Virtual Inverter

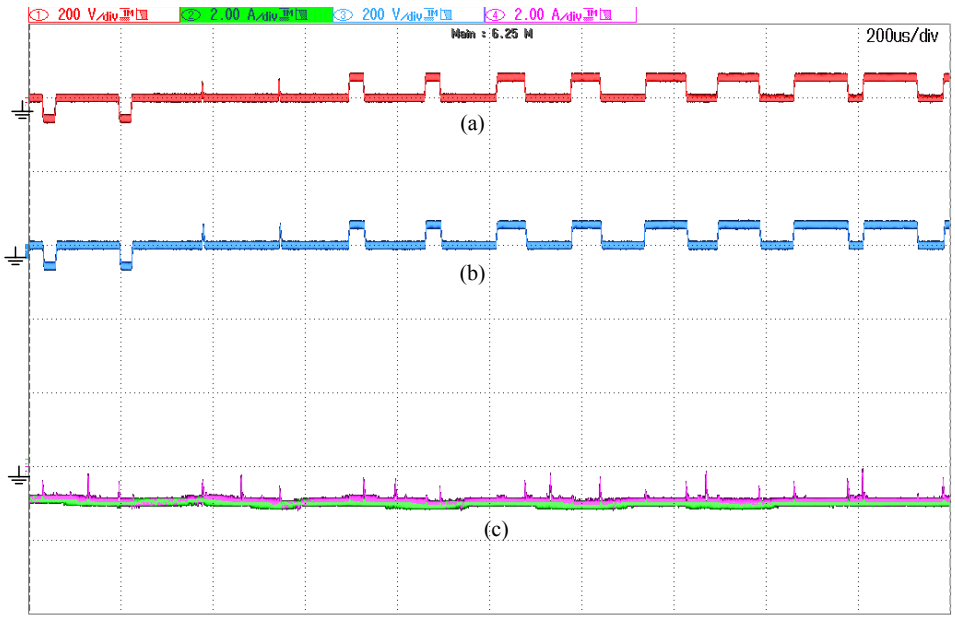


Figure 3.43. Zoomed in Waveforms of Line Voltages (V_{RY}) of (a) Physical Inverter, (b) Virtual Inverter (c) Line Current (I_R) of the both the Inverters

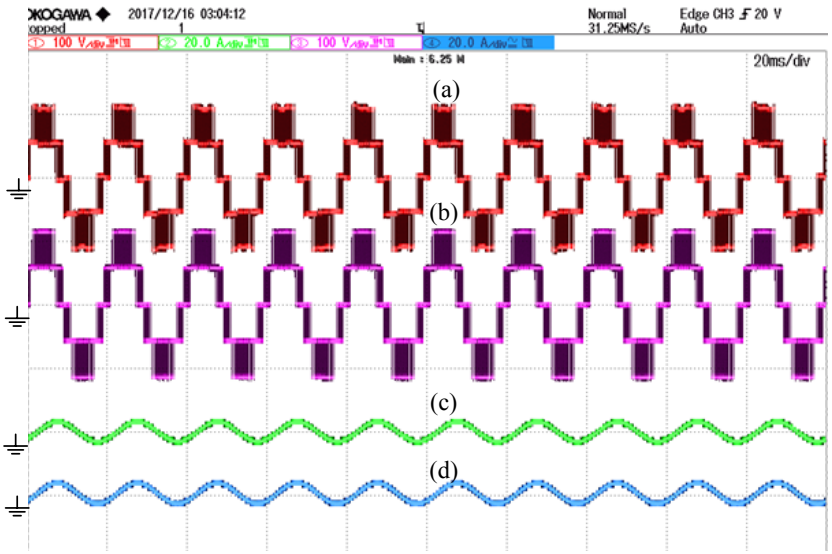


Figure 3.44. Line Voltage (V_{YB}): (a) Physical Inverter and (b) Virtual Inverter; Line Current (I_Y): (c) Physical Inverter and (d) Virtual Inverter

Figure 3.45 shows the SPS output of the three-level inverter when connected to different loads, it can be seen that the voltage and current waveforms are quite similar to the ones obtained in Sections 3.5.1 to 3.5.3.

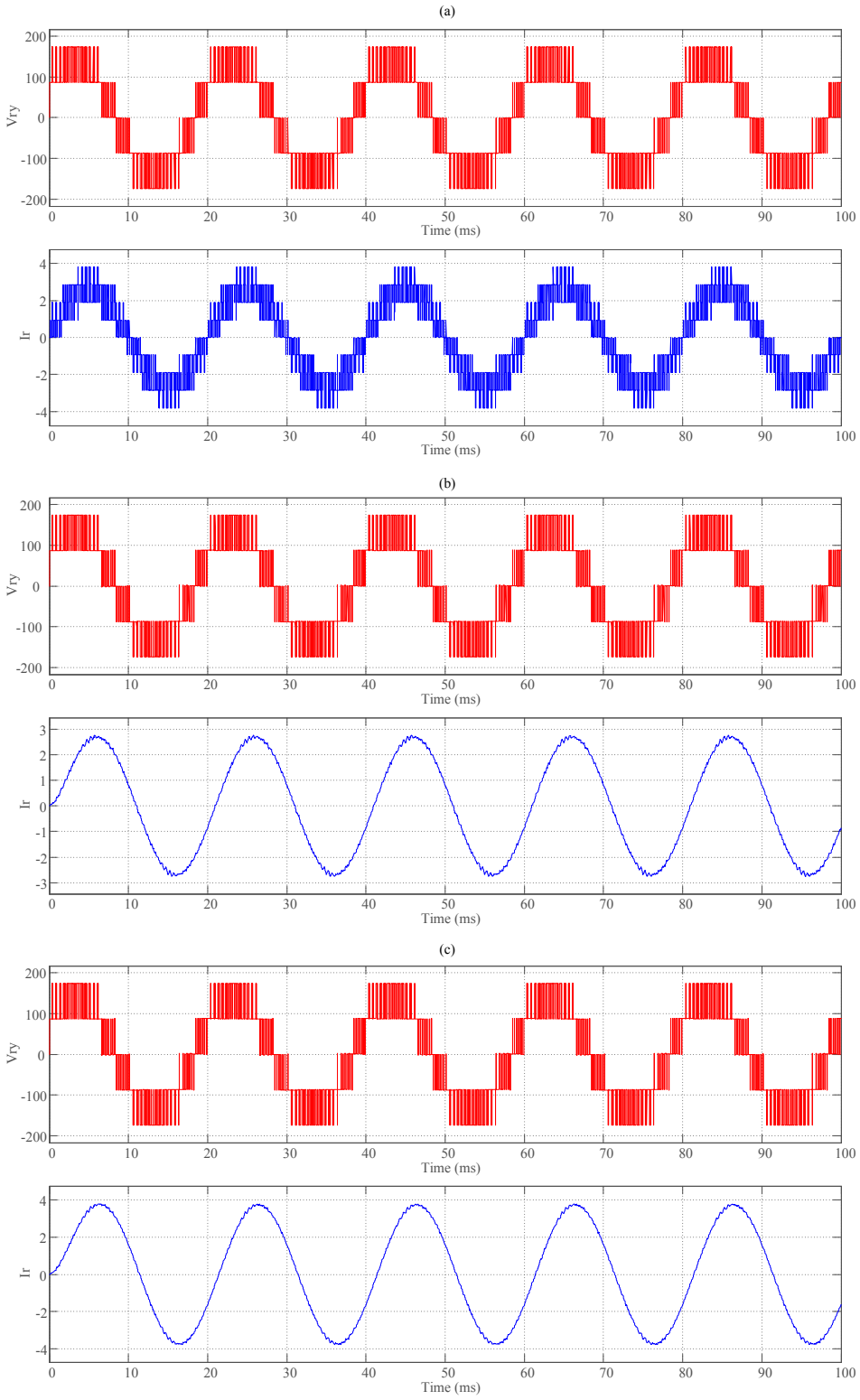


Figure 3.45. SPS output of Line-Line Voltages (V_{RY}) and Line Current (I_R) (a) At Unity Power Factor, (b) At 0.95 Power Factor and (c) At 0.9 Power Factor

3.8 Conclusion

A validation of a three-phase three-level inverter was done in real-time simulation. The chapter also gives a brief introduction to the concept of multilevel inverters, basic topologies and operation. The modulation technique for the three-level NPC inverter is also discussed along with an introduction to various other modulation schemes available. The chapter also provides the methodology for the real-time simulation of a three-level inverter in RT-Lab. With an optimized switch conductance parameter for rated conditions the validations of the eHS solvers were successful. The validation was also done for unbalanced load, the eHS and SPS output was mostly within a 2 % error margin.

Chapter 4. Optimization of G_S Parameter used in FAMNM for RTS

4.1 Need of G_s Optimization

The switch conductance parameter can dictate the power flow through a circuit. As already discussed in Chapter 2, the choice of a proper G_s shall influence how much power can be delivered to the load through a switch. But in RTS, choice of this G_s value becomes very critical, after the simulation starts, this value is no longer accessible; once it is set during the initialization it remains fixed until the end of the simulation. So, in order to get accurate results from a real-time simulation, an optimized switch conductance parameter will be necessary. [26] and [27] discusses some means to find G_s for a two-level inverter, but as [26] mentions this switch parameter can be influenced by the circuit conditions such as input voltage, load, duty cycles of the switches etc.

A three-level inverter leg is shown in Figure 4.1, and the conduction path when the top switches (SW1 and SW2) are ON and the bottom switches (SW3 and SW4) are off is shown in Figure 4.2.

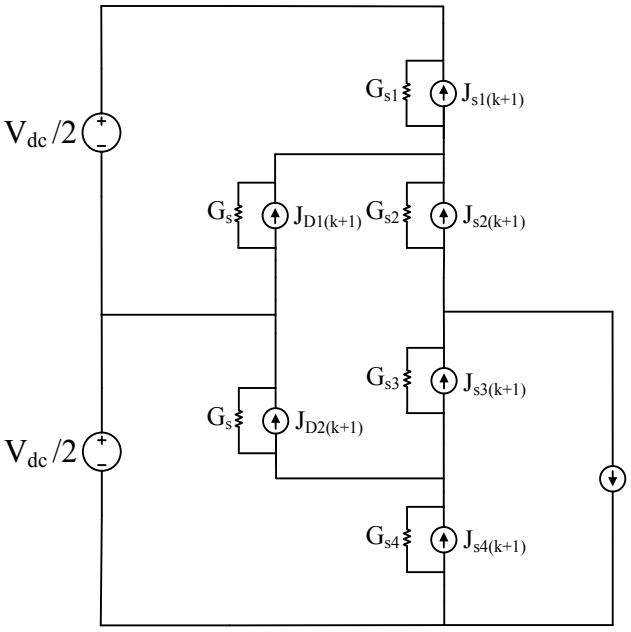


Figure 4.1. Three-level Inverter Leg with Discrete Switches

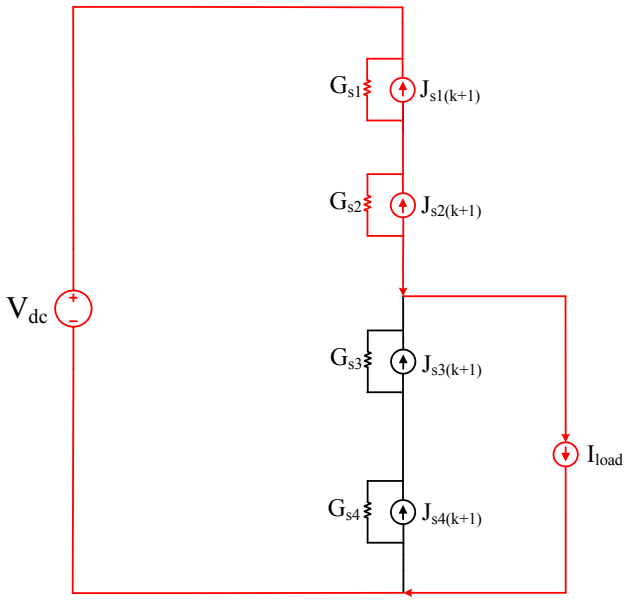


Figure 4.2. Power Flow in the Inverter Leg with S_1 and S_2 ON

The currents in each of the switches in one leg of the three-level inverter can be derived as shown in equations (4.1) to (4.4).

$$I_{SW1}(k+1) = i_{Gs1}(k+1) - j_{s1}(k+1) \tag{4.1}$$

$$I_{SW2}(k+1) = i_{Gs2}(k+1) - j_{s2}(k+1) \tag{4.2}$$

$$I_{SW3}(k+1) = i_{Gs3}(k+1) - j_{s3}(k+1) \tag{4.3}$$

$$I_{SW4}(k+1) = i_{Gs4}(k+1) - j_{s4}(k+1) \tag{4.4}$$

The switch conductance parameters can be replaced by their reciprocals to simplify the expressions as shown in (4.5).

$$r_{s1} = \frac{1}{G_{s1}}; r_{s2} = \frac{1}{G_{s2}}; r_{s3} = \frac{1}{G_{s3}}; r_{s4} = \frac{1}{G_{s4}} \tag{4.5}$$

Applying KVL in the circuit shown in Figure 4.2 expression (4.6) can be obtained.

$$V_{dc} = r_{s1}I_{Gs1}(k+1) + r_{s2}I_{Gs2}(k+1) + r_{s3}I_{Gs3}(k+1) + r_{s4}I_{Gs4}(k+1) \tag{4.6}$$

Again applying KCL at the node where the load is connected in the same circuit, expressions (4.7) to (4.9) can be obtained.

$$-i_{Gs2}(k+1) + j_{s2}(k+1) + i_{load} + i_{Gs3}(k+1) - j_{s3}(k+1) = 0 \tag{4.7}$$

$$i_{Gs2}(k+1) = j_{s2}(k+1) - j_{s3}(k+1) + i_{Gs3}(k+1) + i_{load} \tag{4.8}$$

$$i_{Gs3}(k+1) = j_{s3}(k+1) - j_{s2}(k+1) + i_{Gs2}(k+1) - i_{load} \tag{4.9}$$

Substituting (4.9) in (4.6) expressions (4.10) and (4.11) can be derived:

$$\begin{aligned} V_{dc} = {} & r_{s1} i_{Gs1}(k+1) + r_{s2} i_{Gs2}(k+1) \\ & + r_{s3}\{i_{Gs2}(k+1) - j_{s2}(k+1) - i_{load} + j_{s3}(k+1)\} + r_{s4} i_{Gs4}(k+1) \end{aligned} \tag{4.10}$$

$$\begin{aligned} & i_{Gs2}(k+1) \\ & = \frac{[V_{dc} - r_{s1} i_{Gs1}(k+1) - r_{s3}\{j_{s3}(k+1) - j_{s2}(k+1) - i_{load}\} - r_{s4} i_{Gs4}(k+1)]}{r_{s1} + r_{s3}} \end{aligned} \tag{4.11}$$

Substituting (4.11) in (4.2), expression (4.12) and (4.13) can be derived which is the final expression is for the current in the top inner switch of the inverter leg.

$$\begin{aligned} & I_{SW2}(k+1) \\ & = \frac{[V_{dc} - r_{Gs1} i_{rs1}(k+1) - r_{s3}\{j_{s3}(k+1) - j_{s2}(k+1) - i_{load}\} - r_{s4} i_{Gs4}(k+1) - r_{s2} j_{s2}(k+1) - r_{s3} j_{s2}(k+1)]}{r_{s2} + r_{s3}} \end{aligned} \tag{4.12}$$

$$\begin{aligned} & I_{SW2}(k+1) \\ & = \frac{\{V_{dc} - r_{s1} i_{Gs1}(k+1) - r_{s3} j_{s3}(k+1) + r_{s3} i_{load} - r_{s4} i_{Gs4}(k+1) - r_{s2} j_{s2}(k+1)\}}{r_{s2} + r_{s3}} \end{aligned} \tag{4.13}$$

If an assumption in (4.14) is made, then the current in the second switch can be expressed as (4.15).

$$r_{s4} = r_{s1}, r_{s3} = r_{s2} \tag{4.14}$$

$$\begin{aligned} & I_{SW2}(k+1) \\ & = \frac{[V_{dc} - r_{s1}\{i_{Gs1}(k+1) + i_{Gs4}(k+1)\} - r_{s2}\{j_{s2}(k+1) + j_{s3}(k+1)\} + r_{s2} i_{load}]}{2 r_{s2}} \end{aligned} \tag{4.15}$$

Similarly, the current expression *(I_{sw3})* for the lower side inner switch can be found from the expressions (4.16) to (4.21).

$$\begin{aligned} V_{dc} = {} & r_{s1} i_{Gs1}(k+1) + r_{s2}\{j_{s2}(k+1) - j_{s3}(k+1) + i_{Gs3}(k+1) + i_{load}\} \\ & + r_{s3} i_{Gs3}(k+1) + r_{s4} i_{Gs4}(k+1) \end{aligned} \tag{4.16}$$

$$\begin{aligned} V_{dc} = {} & r_{s1} i_{Gs1}(k+1) + r_{rs2}\{j_{s2}(k+1) - j_{s3}(k+1)\} + i_{Gs3}(k+1)\{r_{s2} + r_{s3}\} \\ & + r_{s2} i_{load} + r_{s4} i_{Gs4}(k+1) \end{aligned} \tag{4.17}$$

$$i_{Gs3}(k+1) = \frac{[V_{dc} - r_{s1}i_{Gs1}(k+1) - r_{s2}\{j_{s2}(k+1) - j_{s3}(k+1)\} - r_{s4}i_{Gs4}(k+1) - r_{s2}i_{load}]}{r_{s2} + r_{s3}} \quad (4.18)$$

$$I_{SW3}(k+1) = i_{Gs3}(k+1) - j_{s3}(k+1) \quad (4.19)$$

$$I_{SW3}(k+1) = \frac{[V_{dc} - r_{s1}i_{Gs1}(k+1) - r_{s2}j_{s2}(k+1) - r_{s4}i_{Gs4}(k+1) - r_{s2}i_{load} - r_{s3}j_{s3}(k+1)]}{r_{s2} + r_{s3}} \quad (4.20)$$

$$I_{SW3}(k+1) = \frac{[V_{dc} - r_{s4}\{i_{Gs1}(k+1) + i_{Gs4}(k+1)\} - r_{s3}\{j_{s2}(k+1) + j_{s3}(k+1)\} - r_{s3}i_{load}]}{2r_{s3}} \quad (4.21)$$

Using the expressions (4.14), (4.15) and (4.21), the expression for the load current can be obtained.

$$I_{SW2}(k+1) - I_{SW3}(K+1) = i_{load} \quad (4.22)$$

Expression (4.22) indicates that the assumptions made in (4.14) are correct, thus the switch conductance values for the both the inner switches and the two outer switches shall be similar. Since the top two switches are ON and the bottom two switches are OFF, expressions (4.1) to (4.4) can be re-written as (4.23) to (4.26) using the expression for the current source in (2.1). These expressions indicate that the switch currents in the current simulation step, *k+1* is dependent upon the currents or voltages of a previous simulation step *k*.

$$I_{SW1}(k+1) = i_{Gs1}(k+1) + I_{SW1}(k) \quad (4.23)$$

$$I_{SW2}(k+1) = i_{Gs2}(k+1) + I_{SW2}(k) \quad (4.24)$$

$$I_{SW3}(k+1) = i_{Gs3}(k+1) - G_{s3}V_{SW3}(k) \quad (4.25)$$

$$I_{SW4}(k+1) = i_{Gs4}(k+1) - G_{s4}V_{SW4}(k) \quad (4.26)$$

From the analysis above, it can be seen that the switch conductance parameter can determine the current flowing through a switch which again, dictates the flow of load current. Hence it is very important that this parameter is properly optimized to produce accurate simulation results. Figure 4.3 and Figure 4.4 shows the current in the outer and the inner switch respectively.

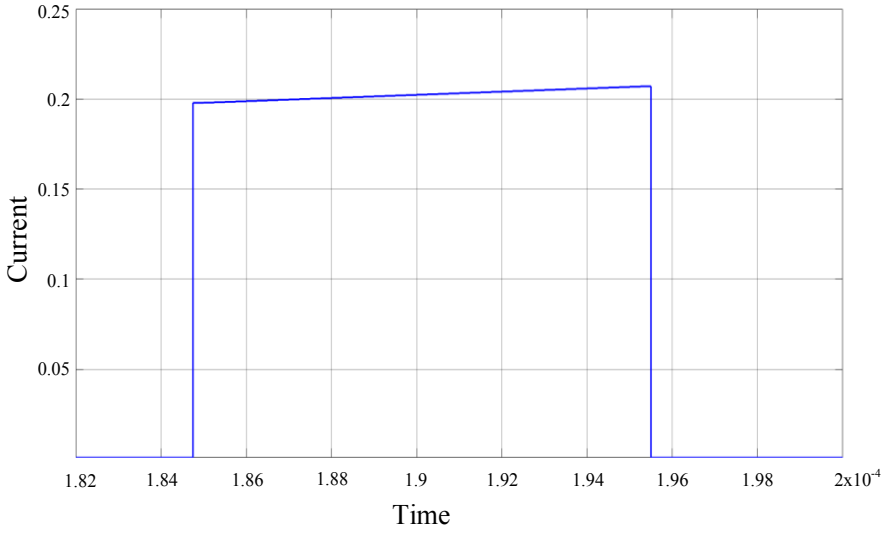


Figure 4.3. Current in Switch 1 (top outer switch)

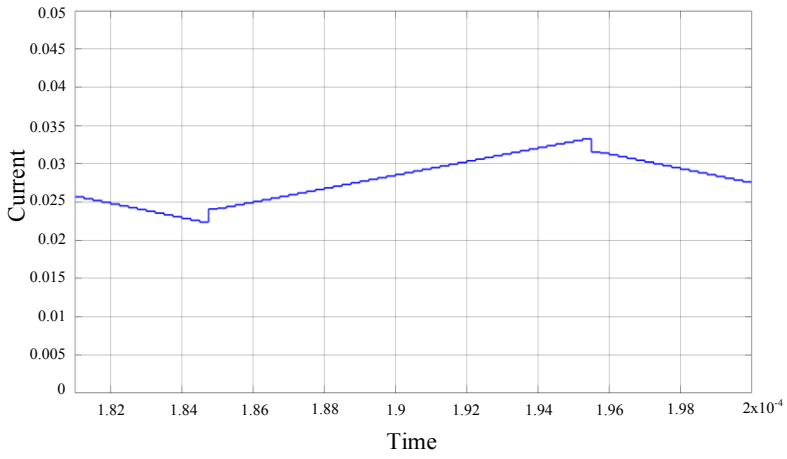


Figure 4.4. Current in Switch 2 (top inner switch)

4.2 Getting G_s as a Ratio of Switches' Currents and Voltages

As discussed earlier in Section 2.4, one of the biggest drawbacks of the Pejovic switch model is the inclusion of artificial losses, which is prominent during commutation of the switch. The discrete switch is modelled as an inductor when it is ON and a capacitor when it is OFF. When there is a change of state from ON to OFF an energized inductor is replaced by a capacitor with no energy, similarly in a transition from OFF to ON an energized capacitor is replaced by a de-energized inductor [26].

If a switch was ON in k^{th} simulation step and turned OFF in the subsequent $k+1^{th}$ step and the energy from inductor in the k^{th} step is propagated to the $k+1^{th}$ step then the equality in (4.27) is

observed. L_{sON} and C_{sOFF} are the small inductances and capacitances when the switch is modelled ON and OFF respectively.

$$0.5\left(L_{s_{ON}}\right)(i_s^k)^2 = 0.5\left(C_{S_{OFF}}\right)(v_s^{k+1})^2 \tag{4.27}$$

The equality in (4.27) is important when a switch has been conducting a large amount of current or blocking a large voltage and the energy stored in either of the ON or OFF models may not be neglected. Substituting the values of $L_{sON} = T_s/G_s$ and $C_{sOFF} = T_sG_s$ (4.27) can be re-written as shown in (4.28) and (4.29):

$$G_S = \frac{i_s^k}{v_s^{k+1}} \tag{4.28}$$

$$G_S \cong \frac{(\sum i_s^k)}{\left(\sum v_s^{k+1}\right)} \tag{4.29}$$

The expression in (4.28) and (4.29) can also be derived by minimizing the losses during switch commutations [26], [27]. The total losses during a switch commutation can be described as in (4.30) and (4.31).

$$E_{loss} = \ 0.5\left(L_{s_{ON}}\right)(i_s^k)^2 + \ 0.5\left(C_{S_{OFF}}\right)(v_s^{k+1})^2 \tag{4.30}$$

$$E_{loss} = \ 0.5\left(\frac{T_s}{G_s}\right)(i_s^k)^2 + \ 0.5\,(T_SG_s)(v_s^{k+1})^2 \tag{4.31}$$

Minimizing the error in (4.31) with the derivative:

$$\frac{dE_{loss}}{dG_s} = 0 \tag{4.32}$$

The derivative in (4.32) can be simplified to as:

$$G_s = \frac{i_s^k}{v_s^{k+1}} = \frac{I_{RMS}}{V_{RMS}} \tag{4.33}$$

An evaluation of the G_s parameter derived on the basis of the switch current and voltage shall be done on a number of converters. An attempt shall be made to obtain a mechanism to optimize the switch conductance parameter irrespective of the circuit topologies. Usage of (4.33) to obtain the currents and voltages for each sample and then averaging them to calculate G_s will be referred to as the 'Sample Method' and when RMS values of switch current and voltage are

used, it will be referred to as the 'RMS Method'. The G_s parameter(s) shall be computed using either or both methods and put to test on the following circuits:

a) A Buck Converter with an Open Circuited Freewheeling Diode.

b) A Boost Converter with a Short Circuited Freewheeling Diode.

c) A Three-phase Three-level Inverter with Unbalanced Load.

4.2.1 A Buck Converter with an Open Circuited Freewheeling Diode

A buck converter was chosen for the purpose of testing the derived G_s parameter because of its simplicity. The results obtained, may be extended to more sophisticated and complex circuits. In order to test the robustness of this method to calculate G_s, the buck converter is subjected to some abnormal working conditions such as an open freewheeling diode. The parameters of the converter are provided in Table 24. The buck converter with an open freewheeling diode is shown in Figure 4.5. To emulate the open freewheeling diode, it is replaced by a very high resistance. The switch current is shown in Figure 4.6. Due to the open circuited freewheeling diode it is expected that the voltage across the switch would be very high during an ON to OFF switch transition as shown in Figure 4.7 and Figure 4.8. The simulation result confirms the presence of this transient voltage, this voltage decays to a steady state value. For the circuit under study, the time required for the voltage to get to its steady state value was 2μs, and with a time-step of 250ns, 8 samples can be collected in between this interval. So by collecting 8 samples of current just before the switch is turned OFF, and 8 samples of voltage just after the switch is turned OFF and substituting the values in (4.28) the G_s obtained is 2.1279e-04. Another way of evaluating the switch conductance parameter is by substituting the RMS values of current and voltage in (4.28), the G_s parameter calculated by this means is 2.9524e-04. Table 25 gives a comparison between the output of the different solvers using the aforementioned switch conductance values and Figure 4.9 shows the eHS and SPS output of the buck converter.

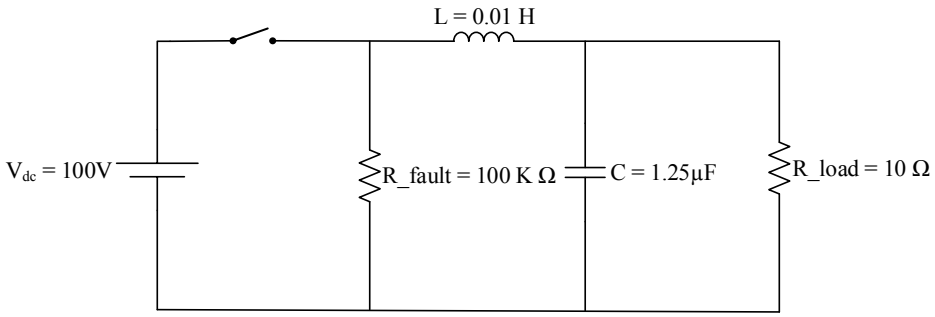


Figure 4.5. Buck Converter Circuit with an Open Circuited Diode

Table 24. Circuit Parameters of the Buck Converter

Parameter	**Label**	**Value**
PWM Frequency	PWM_Freq	10 KHz
DC Source	Vdc_Source	100 V
Diode ON Resistance	Diode_Ron	1e-3 Ω
Diode Snubber Resistance	Diode_Rs	1e5 Ω
Diode Snubber Capacitance	Diode_Cs	Inf
IGBT ON Resistance	IGBT_Ron	1e-3 Ω
IGBT Snubber Resistance	IGBT_Rs	1e5 Ω
IGBT Snubber Capacitance	IGBT_Cs	Inf
Resistive Load	R_Load	10 Ω
Buck Inductor	L	1e-2 H
Output Ripple Capacitor	C	1.25µF

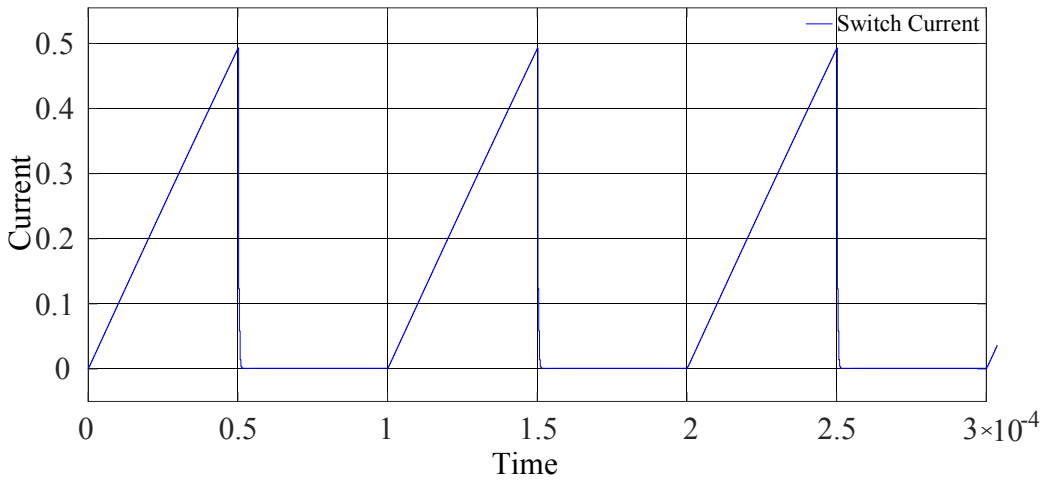


Figure 4.6. Switch Current in the Buck Converter

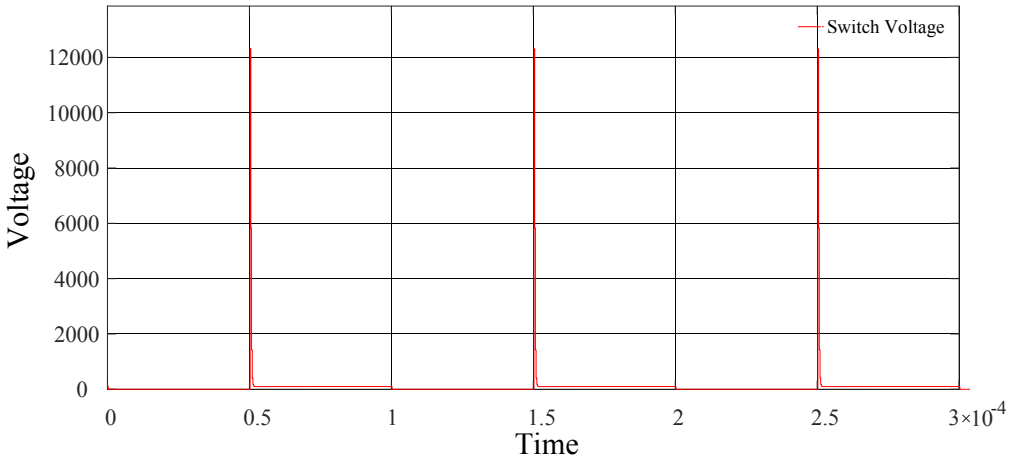


Figure 4.7. Switch Voltage in the Buck Converter

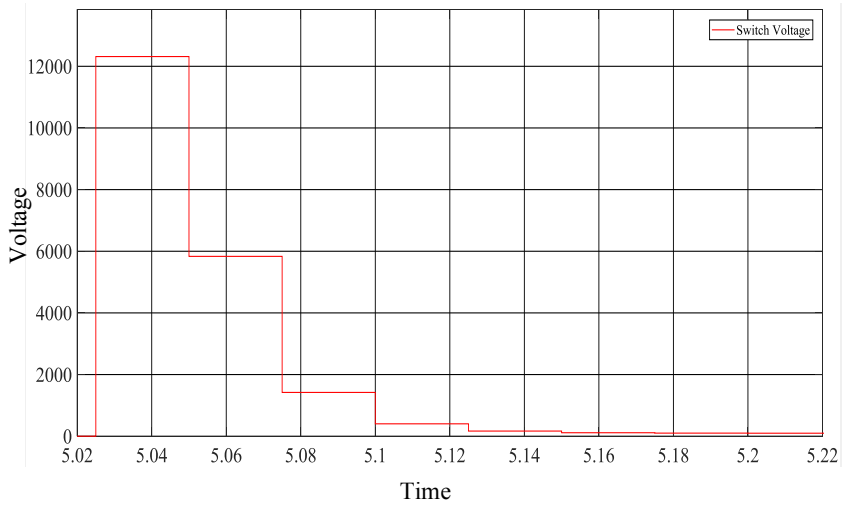


Figure 4.8. Zoomed Switch Voltage in the Buck Converter

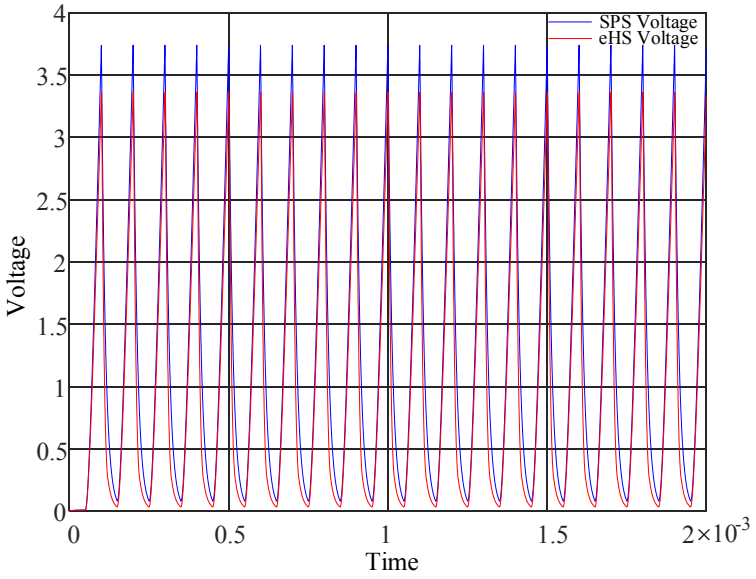


Figure 4.9. Output of the Buck Converter from the SPS and eHS Solvers

Table 25. Output of the Buck Converter with Open Diode

G_s = 2.1279e-4 (From sample method)					
SPS Voltage (Avg)	eHS Voltage (Avg)	error	SPS Voltage (RMS)	eHS Voltage (RMS)	error
1.2398 V	0.9884 V	20.26 %	1.6623 V	1.4282 V	14.08 %
G_s = 2.9524e-4 (From RMS method)					
SPS Voltage (Avg)	eHS Voltage (Avg)	error	SPS Voltage (RMS)	eHS Voltage (RMS)	error
1.2398 V	0.9508 V	23.31 %	1.6623 V	1.4607 V	12.13%

This method for optimizing G_s extended to a normal buck converter as well, the buck converter had no faulty components in it and was just supplying a nominal load. Figure 4.10 shows a normal buck converter circuit. The switch current is shown in Figure 4.11. During a switching cycle, the switch current varied from 4.817A to 5.086A, however the switch voltage remained constant at around 100V. With a time step of 250ns again, it can be ascertained that there are 400 samples collected in a switching cycle, 200 each for the ON and OFF periods respectively. Collecting all of these samples, summing the values and substituting them in (4.28), the switch conductance calculated is 0.0472, moreover, if the RMS values of the current and voltages are used the G_s value returned is 0.0414. On the other hand, the switch conductance optimized by GsGui2 is 0.05, the switch conductance parameters returned by either of these three techniques are now closer than they were when there was a faulty diode in the circuit. The comparison in Table 26 shows that the output of the buck converter from SPS and eHS are very

close to each other for any of the three optimized G_s values. Figure 4.12 and Figure 4.13 shows the output of the buck converter from the eHS and SPS solvers.

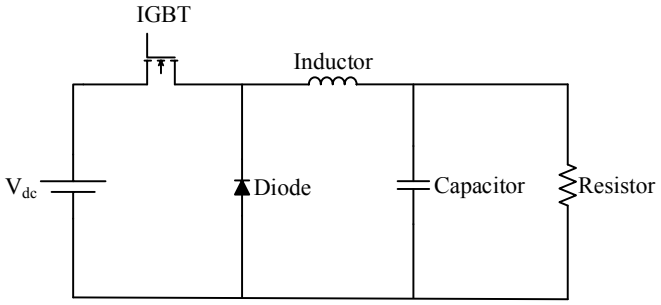


Figure 4.10. A Buck Converter

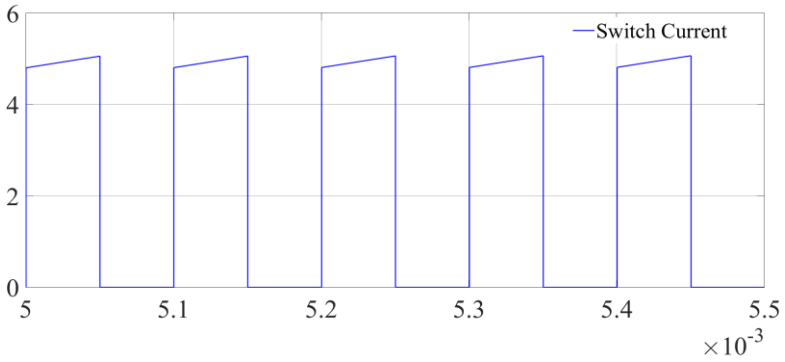


Figure 4.11. Switch Current of a Normal Buck Converter

Table 256. Output Parameters of the Normal Buck Converter

G_s = 0.0472 (From sample method)					
SPS Voltage (Avg)	eHS Voltage (Avg)	error	SPS Voltage (RMS)	eHS Voltage (RMS)	Error
48.97 V	48.98 V	0.02%	49.23 V	49.24 V	0.02%
G_s = 0.0414 (From RMS method)					
SPS Voltage (Avg)	eHS Voltage (Avg)	Error	SPS Voltage (RMS)	eHS Voltage (RMS)	Error
48.97 V	48.98 V	0.02%	49.23 V	49.24 V	0.02%
G_s = 0.05 (From GsGui2)					
SPS Voltage (Avg)	eHS Voltage (Avg)	Error	SPS Voltage (RMS)	eHS Voltage (RMS)	Error
48.97	48.98 V	0.02%	49.23 V	49.24 V	0.02%

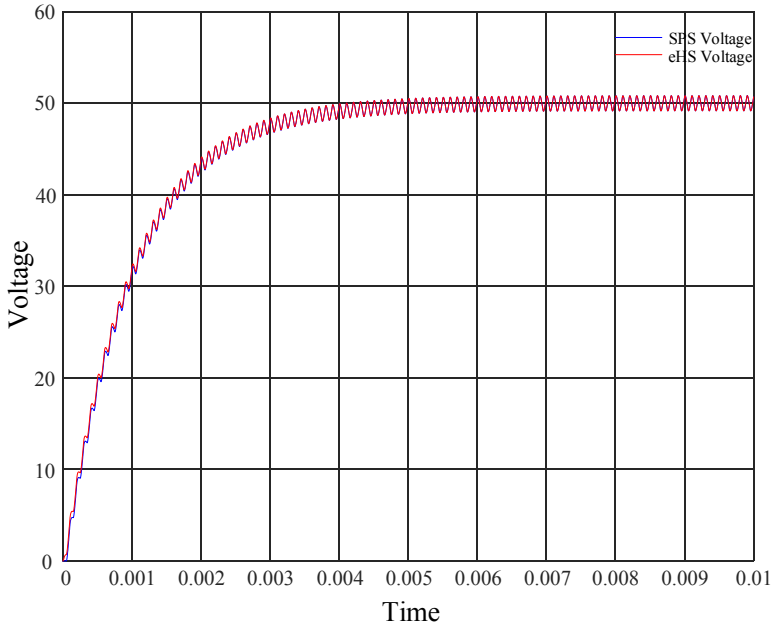


Figure 4.12. Output of the Normal Buck Converter with G_s = 0.0414

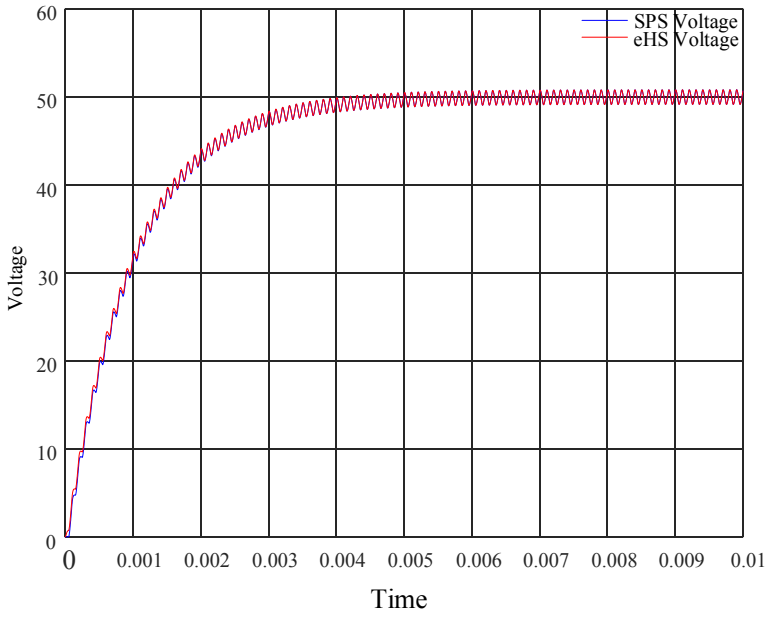


Figure 4.13. Output of the Normal Buck Converter with $G_s = 0.05$ (Returned by eHS Optimized Tool)

4.2.2 A Boost Converter with a Short Circuited Freewheeling Diode

To ensure that the method established earlier for the G_s optimization of the buck converter circuit is generic and would be applicable to other topologies as well, it was tested on a boost converter. The component parameters in the boost converter are same as of those of the buck converter provided in Table 24. The diode in the boost converter is shorted for the analysis, the circuit is as shown in Figure 4.14. Upon simulation of the circuit in MATLAB and substituting the currents and voltage values in (4.28), a $G_s = 0.1601$ is obtained. Furthermore by taking into account the RMS values of current and voltages, placing them in (4.28) produced a $G_s = 0.458$. The GsGui2 produces a $G_s = 0.2$ for the boost converter operating without any abnormality. Table 27 shows the output of the boost converter from the two solvers for with the G_s parameters evaluated, the output of the boost converter is shown in Figure 4.15.

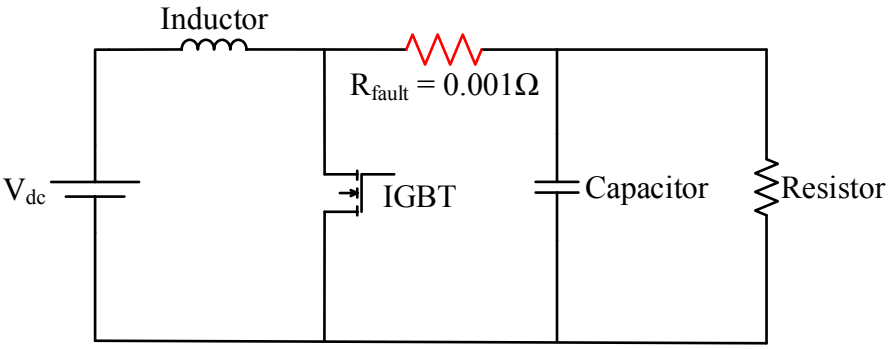


Figure 4.14. Boost Converter with a Shorted Diode

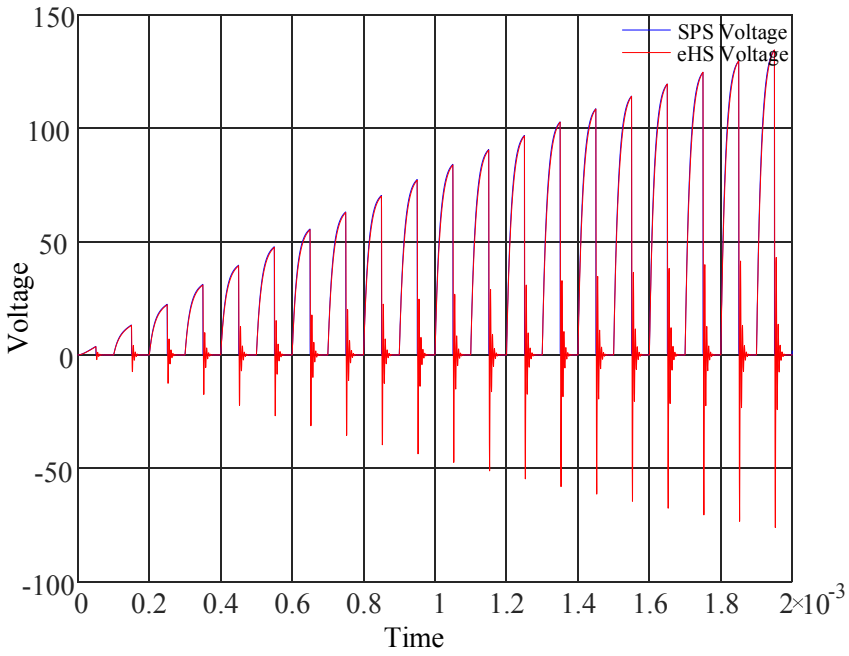


Figure 4.15. Output of the Boost Converter Using G_s = 0.458

Table 267. Output Comparison of the Boost Converter with Different G_s values

G_s = 0.1601 (From sample method)					
SPS Voltage (Avg)	eHS Voltage (Avg)	Error	SPS Voltage (RMS)	eHS Voltage (RMS)	Error
94.67 V	94.63 V	0.0423 %	142.92 V	147.73 V	3.37 %
G_s = 0.458 (From RMS method)					
SPS Voltage (Avg)	eHS Voltage (Avg)	Error	SPS Voltage (RMS)	eHS Voltage (RMS)	Error
94.67 V	94.53 V	0.148 %	142.92 V	145.49 V	1.8 %
G_s = 0.2 (From GsGui2)					
SPS Voltage (Avg)	eHS Voltage (Avg)	Error	SPS Voltage (RMS)	eHS Voltage (RMS)	Error
94.67 V	94.63 V	0.0423 %	142.92 V	147.06 V	2.897 %

4.2.3 A Three-phase Three-level Inverter with Unbalanced Load

When the inverter was connected to an unbalanced load in Section 3.6, it was found that the error between the line currents from eHS and SPS differed marginally based upon the values of line currents taken. The circuit parameters are mentioned again in Table 28, this is the same circuit used in Section 3.6. The switch conductance measurement using the RMS values of the switch currents and voltages have proven viable earlier, it will be tested again in a circuit with an unbalanced load. The evaluation of the G_s parameter is again shown in Table 29 and Table 30, using these switch conductance values and simulating the circuit in eHS online, the results shown in Table 31 can be obtained. It is also observed that the error in between the values returned by eHS and SPS solvers have been reduced compared to the results in Section 3.6.

Table28. Parameters of the Three-level Inverter for the Unbalanced Conditions

Parameter		**Value**
PWM_Frequency		4 kHz
Vdc_Source		173.8 V
R_{on} (S01,…S12)		1e-3 Ω
R_s (S01,…S12)		1e5 Ω
C_s (S01,…S12)		inf
f_{ref} (sine frequency)		50 Hz
R-Phase	R	15 Ω
	L	32mH
Y-Phase	R	15 Ω
	L	32mH
B-Phase	R	70 Ω
	L	32mH

Table 29. G_s Calculation Table for the three-level Inverter Connected to an Unbalanced Load

Switch	Vsw (RMS)	Isw (RMS)	Gs	Switch	Vsw (RMS)	Isw (RMS)	Gs	Switch	Vsw (RMS)	Isw (RMS)	Gs
SW01	72.12	2.1	0.0291	SW05	71.94	1.527	0.0212	SW09	72.11	0.8247	0.0114
SW02	48.5	2.225	0.0459	SW06	48.76	1.922	0.0394	SW10	48.44	0.807	0.0167
SW03	48.47	2.224	0.0459	SW07	48.76	1.923	0.0394	SW11	48.47	0.8119	0.0168
SW04	72.09	2.099	0.0291	SW08	71.92	1.528	0.0212	SW12	72.14	0.8284	0.0115

Table 270. G_s Matrix for the Inverter with a 0.001 Ω Line to Line Fault

$$\begin{bmatrix} 0.0291 & 0.0212 & 0.0114 \\ 0.0459 & 0.0394 & 0.0167 \\ 0.0453 & 0.0313 & 0.0171 \\ 0.0291 & 0.0212 & 0.0115 \end{bmatrix}$$

Table 281. Output of the Inverter from eHS and SPS

Measurement	eHS	SPS	Error
V_{R-Y} (RMS)	110.995 V	111.8 V	0.72 %
V_{Y-B} (RMS)	111.808 V	112.3 V	0.44 %
V_{B-R} (RMS)	111.221 V	111.7 V	0.43 %
I_R (RMS)	3.183 A	3.178 A	0.16 %
I_Y (RMS)	2.752 A	2.744 A	0.29 %
I_B (RMS)	1.153 A	1.156 A	0.26 %

4.3 Getting G_s by Reducing the Distance between Eigenvalues of Ideal Switches and Pejovic Switches.

As discussed in Sections 2.4 and 4.2.1, the discrete time switch model introduced some artificial error into the simulation of an ideal switch. These losses are incurred during the change of switching states from ON to OFF, and vice versa. A technique was devised in [34] wherein these losses were sought to be reduced by minimizing the Euclidian distances between the eigenvalues of the FAMNM matrix of a network and those pertaining to matrices containing ideal switches for the same network.

Yet again the buck converter shall be used owing to the ease of detailed analysis with it. At first, all the components in the buck converter shall be replaced by their discrete equivalent models and all the nodal equations will be derived by using MNA on it. Figure 4.16 shows the buck converter and Figure 4.17 shows the circuit with the equivalent discrete models of the components. Based on these equations the admittance matrix is evaluated which shall bear the switch conductance G_s in it, however, contrary to the FAMNM approach, the G_s in the matrix shall be varied in order to get an optimized value. Then, matrices were derived by using MNA

onto the network with ideal switches and are known as *Reference Matrices*. Only the discrete models of the switches are replaced with ideal switches however, the ON resistance and snubber resistances are preserved as mentioned in Table 24. As the admittance matrix in this case contains a variable G_s, the eigenvalues for the matrix will also change as the G_s parameter is updated, the eigenvalues would be functions of the switch conductance parameter. The FAMNM matrix is shown in Figure 4.18 and the plot of the eigenvalues [35], [36] are given in Figure 4.19.

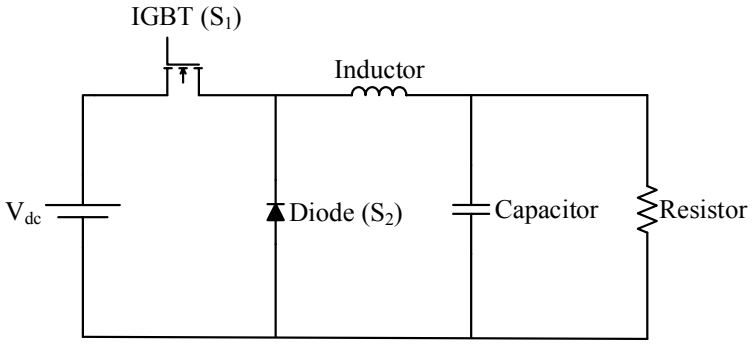


Figure 4.16. The Buck Converter

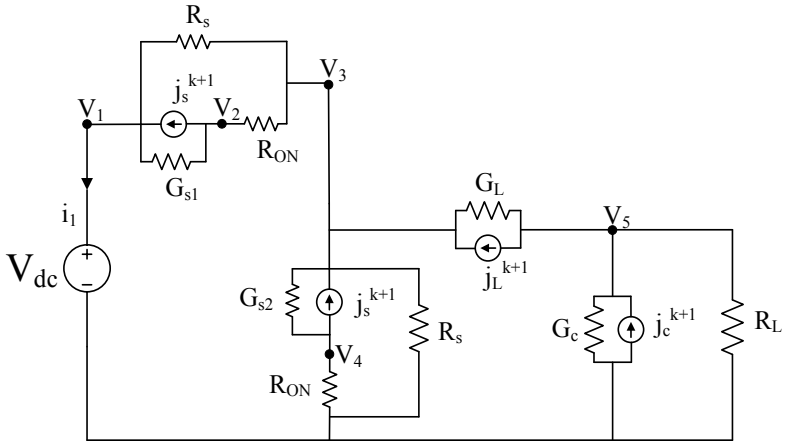


Figure 4.17. The Buck Converter with Discrete Switches

The equations (4.34) to (4.39) can be obtained using MNA on the circuit shown in Figure 4.17. The approximate expressions for the eigenvalues are given in (4.40) to (4.45) and their plots are provided in Figure 4.19.

Node 1:

$$V_1\left(\frac{1}{R_s}+G_{S1}\right)-V_2\,G_{s1}-V_3\frac{1}{R_s}+i_1=J_{s1}^{k+1} \tag{4.34}$$

Node 2:

$$-V_1 G_{s1} + V_2 \left(G_{s1} + \frac{1}{R_{on}} \right) - V_3 \frac{1}{R_{on}} = -J_{s1}^{k+1} \tag{4.35}$$

Node 3:

$$-V_1 \frac{1}{R_s} - V_2 \frac{1}{R_{on}} + V_3 \left(\frac{2}{R_s} + \frac{1}{R_{on}} + G_{s2} + G_L \right) - V_4 G_{s2} - V_5 G_L = J_{s2}^{k+1} - J_L^{k+1} \tag{4.36}$$

Node 4:

$$-V_3 G_{s2} + V_4 \left(G_{s2} + \frac{1}{R_{on}} \right) = -J_{s2}^{k+1} \tag{4.37}$$

Node 5:

$$-V_3 G_L + V_5 \left(G_c + \frac{1}{R} + G_L \right) = J_c^{k+1} + J_L^{k+1} \tag{4.38}$$

$$V_1 = E \tag{4.39}$$

$$\begin{bmatrix} G_{s1} + \frac{1}{R_s} & -G_{s1} & -\frac{1}{\mathrm{R_s}} & 0 & 0 & 1 \\ -\mathrm{G_{s1}} & G_{s1} + \frac{1}{R_{on}} & -\frac{1}{R_{on}} & 0 & 0 & 0 \\ -\frac{1}{R_s} & -\frac{1}{R_{on}} & G_L + \frac{2}{\mathrm{R_s}} + G_{s2} + \frac{1}{R_{on}} & -G_{s2} & -G_L & 0 \\ 0 & 0 & -G_{s2} & G_{s2} + \frac{1}{R_{on}} & 0 & 0 \\ 0 & 0 & -G_L & 0 & G_L + \mathrm{G_c} + \frac{1}{\mathrm{R}} & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Figure 4.18. The FAMNM Matrix Obtained from the MNA equations

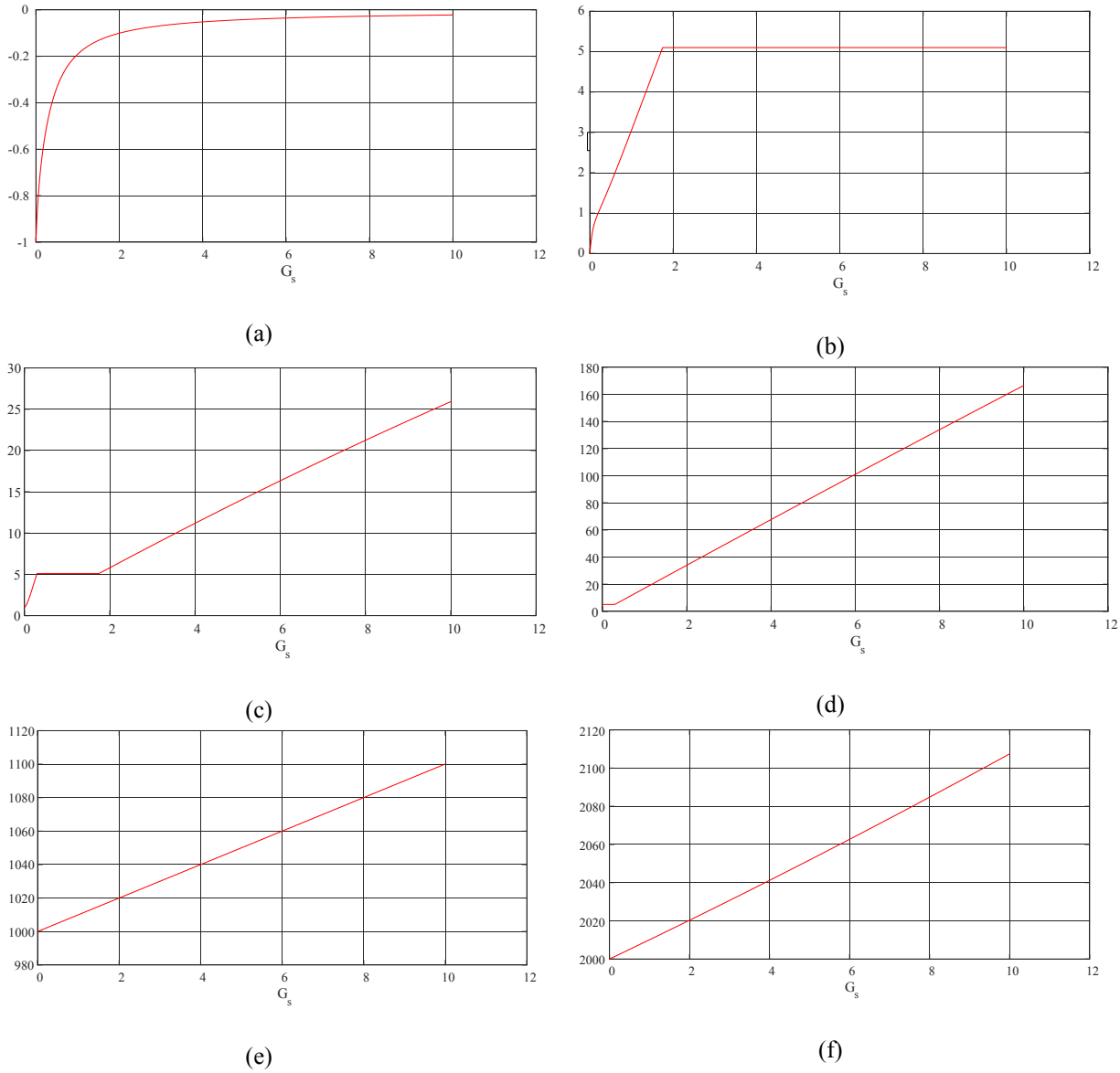


Figure 4.19. Plot of the Eigenvalues Obtained by Varying G_s in the FAMNM Matrix

$$-(1e-07)G_s^2 + 0.0004G_s - 0.9847 \quad (4.40)$$

$$-(5e-07)G_s^2 + 0.001G_s - 0.0168 \quad (4.41)$$

$$(2e-06)G_s^2 - 0.0008G_s + 1.2005 \quad (4.42)$$

$$-(2e-06)G_s^2 + 0.0014G_s + 4.8675 \quad (4.43)$$

$$0.001G_s + 999.999 \quad (4.44)$$

$$0.001008G_s + 1999.9875 \quad (4.45)$$

After the matrix for the network with the discrete switches are obtained, the buck converter with ideal components was evaluated for the following conditions:

a. Ideal Switch S_1 ON and S_2 (Diode) OFF

b. Ideal Switch S_1 OFF and S_2 (Diode) ON

c. Both S_1 and S_2 ON Simultaneously

d. Both S_1 and S_2 OFF Simultaneously

4.3.1 Buck Converter with Ideal Switch S_1 ON and S_2 OFF

The discrete switch model of the IGBT and the freewheeling diode in the buck converter shown in Figure 4.16 are replaced by ideal switches, the discrete models of the remaining components however, are not changed. The resultant circuit is shown in Figure 4.20 using MNA, six nodal equations, from (4.46) to (4.51) can be extracted. The admittance matrix from the set of nodal equations provided earlier is shown in Figure 4.21 the matrix also returns a set of six eigenvalues, since there are no variables in the matrix, this set of eigenvalues would remain constant as stated in Table 32.

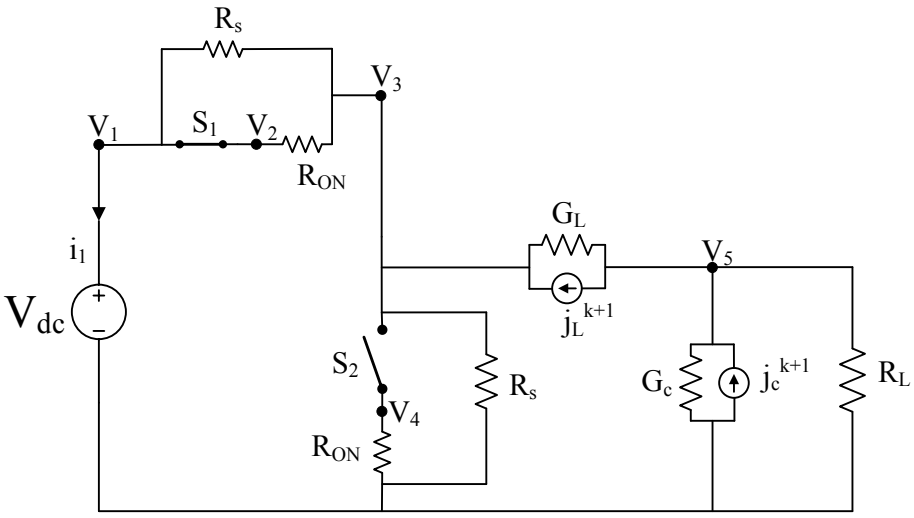


Figure 4.20. Buck Converter with S_1 ON and S_2 OFF

Node 1:

$$V_1\left(\frac{1}{R_s}+\frac{1}{R_{on}}\right)-V_3\left(\frac{1}{R_s}+\frac{1}{R_{on}}\right)+i_1=0 \tag{4.46}$$

Node 2:

$$V_2-V_1=0 \tag{4.47}$$

Node 3:

$$-V_1\left(\frac{1}{R_s}+\frac{1}{R_{on}}\right)+V_3\left(\frac{2}{R_s}+\frac{1}{R_{on}}+G_L\right)-V_5\,G_L=-J_L^{k+1} \tag{4.48}$$

Node 4:

$$V_4 = 0 \tag{4.49}$$

Node 5:

$$-V_3 G_L + V_5 \left(G_L + G_c + \frac{1}{R} \right) = J_L^{k+1} + J_c^{k+1} \tag{4.50}$$

$$V_1 = E \tag{4.51}$$

$$\begin{bmatrix} 1000 & 0 & -1000 & 0 & 0 & 1 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ -1000 & 0 & 1000 & 0 & -2.5e-5 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -2.5e-5 & 0 & 5.1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Figure 4.21. Admittance Matrix of the Buck Converter with S_1 ON and S_2 OFF

Table 292. Eigenvalues of the Buck Converter with S_1 ON and S_2 OFF

Sl. No	Eigenvalues
1	1
2	2000
3	-0.707
4	0.707
5	5.10
6	1

4.3.2 Buck Converter with Ideal Switch S_1 OFF and S_2 ON

Figure 4.22 shows the buck converter with the IGBT ON and the freewheeling diode OFF. The MNA equations are yet again extracted from the network and provided from (4.52) to (4.57). The reference admittance matrix derived from the circuit is shown in Figure 4.23 and the eigenvalues for the network are tabulated in Table 33.

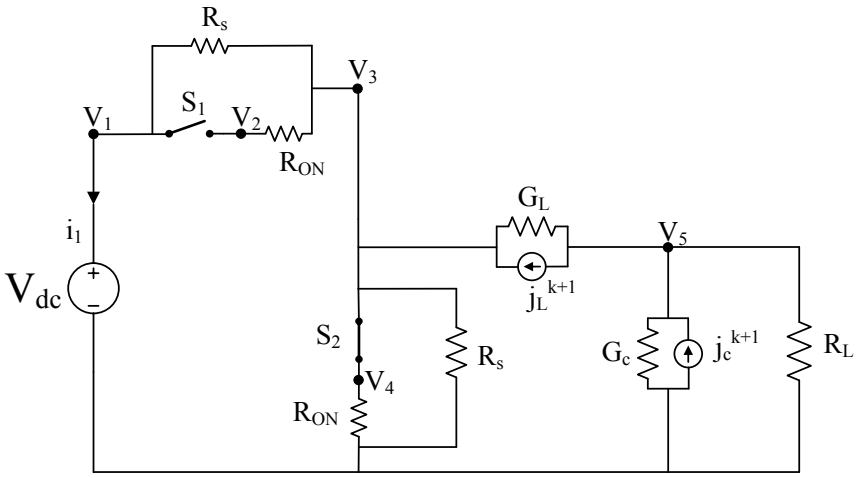


Figure 4.22. Buck Converter with S_1 OFF and S_2 ON

Node 1:

$$V_1\left(\frac{1}{R_s}+\frac{1}{R_{on}}\right)-V_3\left(\frac{1}{R_s}+\frac{1}{R_{on}}\right)+i_1=0 \tag{4.52}$$

Node 2:

$$V_2-V_1=0 \tag{4.53}$$

Node 3:

$$-V_1(\frac{1}{R_s}+\frac{1}{R_{on}})+V_3\left(\frac{2}{R_s}+\frac{1}{R_{on}}+G_L\right)-V_5\,G_L=\ -J_L^{k+1} \tag{4.54}$$

Node 4:

$$V_4=0 \tag{4.55}$$

Node 5:

$$-V_3G_L+V_5\left(G_L+G_c+\frac{1}{R}\right)=J_L^{k+1}+J_c^{k+1} \tag{4.56}$$

$$V_1=E \tag{4.57}$$

$$\begin{bmatrix} 1000 & 0 & -1000 & 0 & 0 & 1 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ -1000 & 0 & 1000 & 0 & -2.5e-5 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -2.5e-5 & 0 & 5.1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Figure 4.23. Admittance Matrix of the Buck Converter for S_1 OFF and S_2 ON

Table 303. Eigenvalues of the Buck Converter with S_1 OFF and S_2 ON

Sl. No	Eigenvalues
1	1
2	2000
3	-0.707
4	0.707
5	5.10
6	1

4.3.3 Buck Converter with Ideal Switch S_1 and S_2 ON

The buck converter with both the switches S_1 and S_2 ON is shown in Figure 4.24 and the MNA equations are tabulated from (4.58) to (4.63) and the derived admittance matrix and eigenvalues are provided in Figure 4.25 and Table 34 respectively. This circuit condition would correspond to a buck converter operating with a shorted diode.

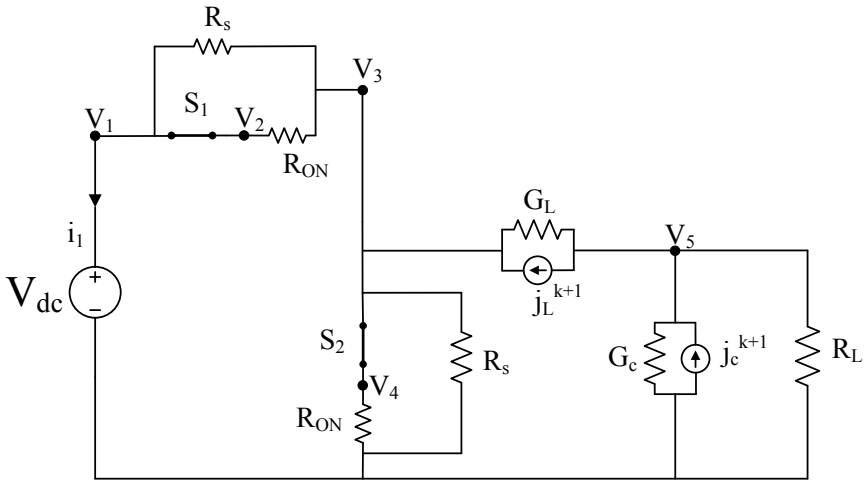


Figure 4.24. Buck Converter with S_1 and S_2 ON

Node 1:

$$V_1 \frac{1}{R_s} - V_3 \frac{1}{R_s} + i_1 = 0 \tag{4.58}$$

Node 2:

$$V_2 - V_3 = 0 \tag{4.59}$$

Node 3:

$$-V_1 \frac{1}{R_s} + V_3 \left(\frac{2}{R_s} + G_L + \frac{1}{R_{on}}\right) - V_5 G_L = -J_L^{k+1} \tag{4.60}$$

Node 4:

$$V_4 - V_3 = 0 \tag{4.61}$$

Node 5:

$$-V_3 G_L + V_5 \left(G_L + \frac{1}{R} + G_c\right) = J_L^{k+1} + J_c^{k+1} \tag{4.62}$$

$$V_1 = E \tag{4.63}$$

$$\begin{bmatrix} 1\text{e}-5 & 0 & -1\text{e}-5 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ -1e-5 & 0 & 1000 & 0 & -2.5-5 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & -2.5e-5 & 0 & 5.1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Figure 4.25. Admittance Matrix of the Buck Converter for S_1 and S_2 ON

Table 314. Eigenvalues of the Buck Converter with S_1 OFF and S_2 ON

Sl. No	Eigenvalues
1	1
2	1
3	1000
4	5.10
5	-1
6	1

4.3.4 Buck Converter with Ideal Switch S_1 and S_2 OFF

When both the switches S_1 and S_2 are open simultaneously, the buck converter would correspond to the operation of the converter with an open diode. Figure 4.26 shows the buck converter circuit with both the ideal switches S_1 and S_2 OFF. The nodal equations are provided

from (4.64) to (4.69), Figure 4.27 shows the reference admittance matrix for the buck converter and Table 35 contains the eigenvalues of the matrix.

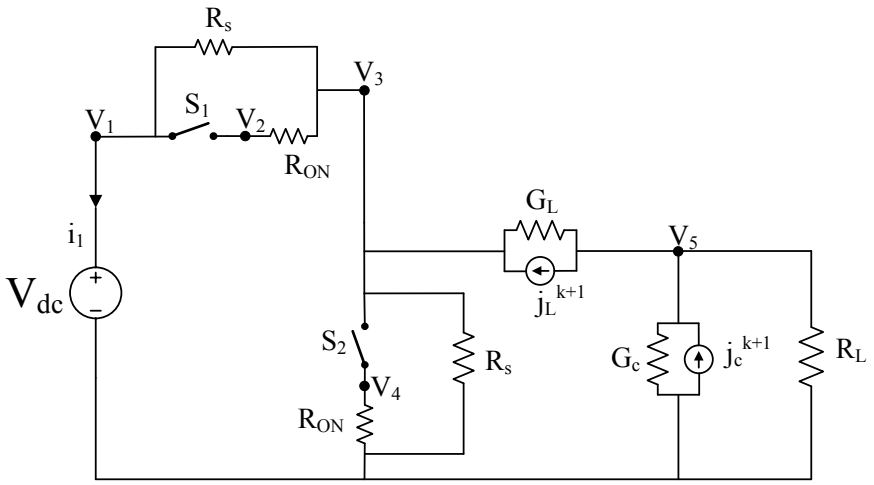


Figure 4.26. Buck Converter with S_1 and S_2 OFF

Node 1:

$$V_1\frac{1}{R_s} - V_3\frac{1}{R_s} + i_1 = 0 \tag{4.64}$$

Node 2:

$$V_2 - V_3 = 0 \tag{4.65}$$

Node 3:

$$-V_1\frac{1}{R_s} + V_3\left(\frac{2}{R_s} + G_L\right) - V_5\,G_L = -J_L^{k+1} \tag{4.66}$$

Node 4:

$$V_4 = 0 \tag{4.67}$$

Node 5:

$$-V_3\,G_L + V_5\left(G_L + G_c + \frac{1}{R}\right) = J_L^{k+1} + J_c^{k+1} \tag{4.68}$$

$$V_1 = E \tag{4.69}$$

$$\begin{bmatrix} 1e-5 & 0 & -1e-5 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ -1e-5 & 0 & 4.5e-5 & 0 & -2.5e-5 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -2.5e-5 & 0 & 5.1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Figure 4.27. Admittance Matrix of the Buck Converter for S_1 and S_2 OFF

Table 325. Eigenvalues of the Buck Converter with S_1 OFF and S_2 ON

Sl. No	Eigenvalues
1	1
2	-1
3	1
4	4.4-05
5	5.10
6	1

4.3.5 Algorithm for Implementing the Proposed G_s Optimization Method

Some of the eigenvalues from the FAMNM matrix shall remain constant. These eigenvalues correspond to the part of the circuit that is not connected directly to a switch. Predicting those eigenvalues would allow the reduction of the size of the matrix for which the eigenvalues as functions of G_s are to be evaluated [34]. The matrices obtained from the buck converter model with ideal switches shall act as reference matrices, the eigenvalues derived from these matrices shall remain constant. However, the eigenvalues from the FAMNM model of the buck converter will be a function of G_s. By finding the total Euclidian distances between the eigenvalues of the FAMNM matrix and those of the reference matrices, and minimizing the sum of the normalized distances as mentioned in [34]; a G_s parameter optimized for all the switch combinations should be obtained. The Euclidian distances can be found by using equation (4.70), where the subscript *'i'* corresponds to the step of the iteration and *'n'* corresponds to the rank of the matrix.

$$EuD_{in} = \left\{Eig_{in}(FAMNM) - Eig_n\left(S_{1_{ON}} \,\&\, S_{2_{OFF}}\right)\right\}^2 + \left\{Eig_{in}(FAMNM) - Eig_n\left(S_{1_{OFF}} \,\&\, S_{2_{ON}}\right)\right\}^2 + \left\{Eig_{in}(FAMNM) - Eig_n\left(S_{1_{ON}} \,\&\, S_{2_{ON}}\right)\right\}^2 + \left\{Eig_{in}(FAMNM) - Eig_n\left(S_{1_{OFF}} \,\&\, S_{2_{OFF}}\right)\right\}^2 \quad (4.70)$$

Eigenvalues of the FAMNM network were obtained by varying G_s in an iterative method. The sum of all the squared Euclidian distances were obtained in each iteration and stored in an array.

The ratio of the sum of all the total squared Euclidian distances and the maximum value contained in the matrix would give the value of the objective function. This value obtained in each iteration was yet again stored in an array and the index of the array where the minimum value is contained, would correspond to the optimized G_s value [34]. Figure 4.28 shows the flow chart of the algorithm and Figure 4.29 shows a plot of the objective function. Table 36 tabulates all the eigenvalues for all the combinations discussed.

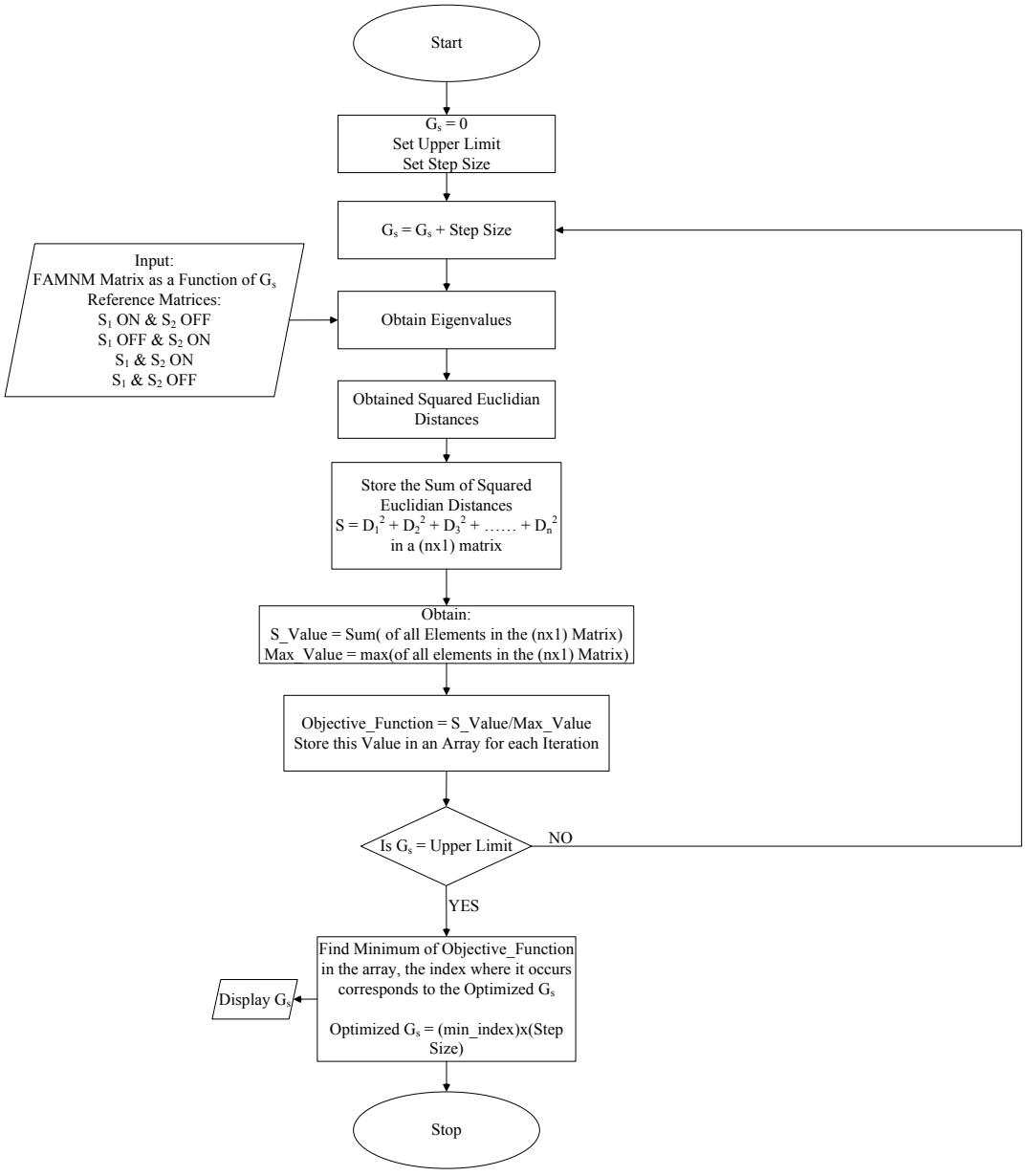


Figure 4.28. Flow Chart of the Algorithm for Optimizing G_s

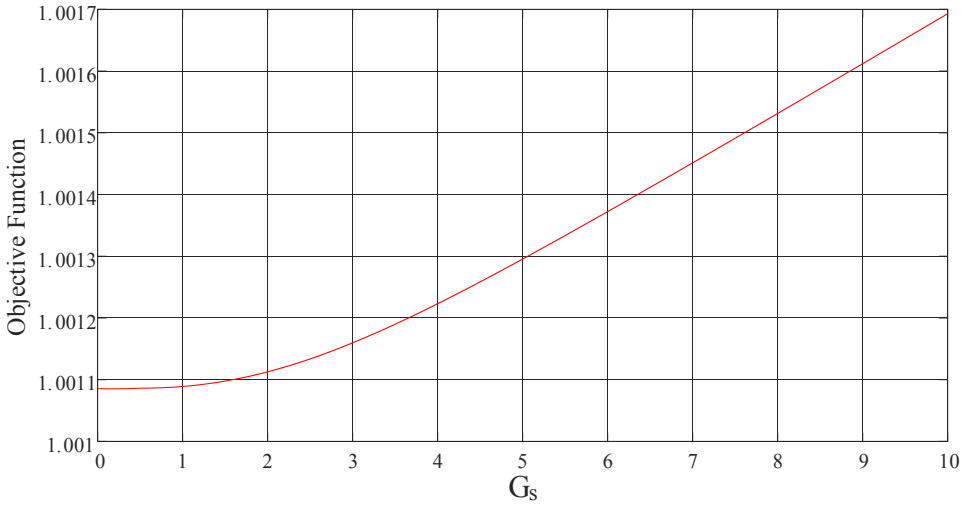


Figure 4.29. Plot of the Objective Function

Table 336. Eigenvalues for all the Switch Combinations

Sl. No	FAMNM	S_1 ON & S2 OFF	S1 OFF & S2 ON	S1 ON & S2 ON	S1 OFF & S2 OFF
1	$0.0004G_s - 0.985$	1	1	1	1
2	$0.001G_s - 0.0168$	2000	1	1	-1
3	$0.0008G_s + 1.2$	-0.707	1000	2618.03	1
4	$0.0014G_s + 4.868$	0.707	5.10	381.97	4.4-05
5	$0.001G_s + 999.999$	5.10	-1	-0.002	5.10
6	$0.0010G_s + 1999.99$	1	1	5.10	1

4.3.6 Validation of the Buck Converter

The optimized G_s parameter shall be tested in the eHS offline solver of OPAL-RT. The results will be compared with those returned by SPS and the difference between the results when the switch conductance returned by the available eHS optimization tool, GsGui2. Since the parameter was optimized for different combinations of the switches in the buck converter, it is to be seen if this single G_s value would provide comparable results between the eHS and SPS solvers for different circuit conditions. The parameter shall be tested for the following circuits:

a. Normal buck Converter
b. Buck Converter with a shorted freewheeling diode
c. Buck converter with an open freewheeling diode

A. Normal Buck Converter

GsGui2 returned a G_s value of 0.05 for a nominal circuit and the algorithm produced a G_s of 0.237. Substituting both these values in the eHS offline solver produces the results shown in

Table 37. Figure 4.30 shows the comparison between the eHS and SPS output voltage for the G_s returned by the algorithm and Figure 4.31 shows the comparison with the switch conductance optimized using GsGui2. The combination of the switch states of (i) S_1 ON & S_2 OFF and (ii) S_1 OFF and S_2 ON corresponds to the normal operation of the buck converter.

Table 347. Output of the Buck Converter from SPS and eHS

G_s = 0.05 (From GsGui2)		
SPS Voltage (Avg)	eHS Voltage (Avg)	Error
49.94 V	49.94 V	0.0423 %
G_s = 0.237 (From Algorithm)		
SPS Voltage (Avg)	eHS Voltage (Avg)	Error
49.943 V	49.945 V	0.0423 %

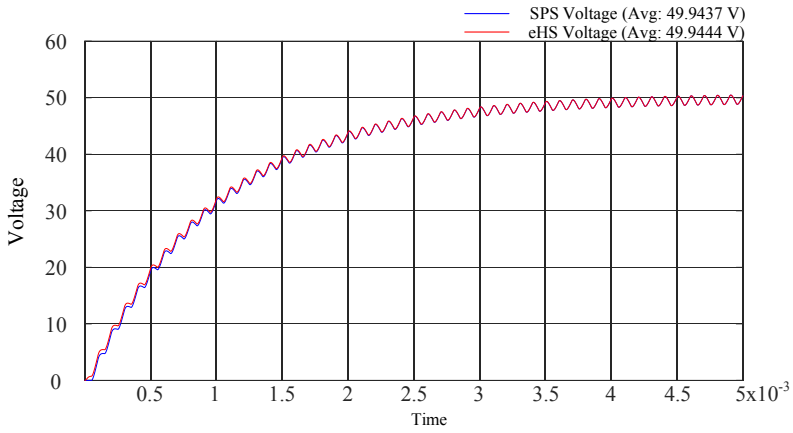


Figure 4.30. SPS and eHS Output for Gs = 0.05 (from GsGui2) in the Normal Buck Converter

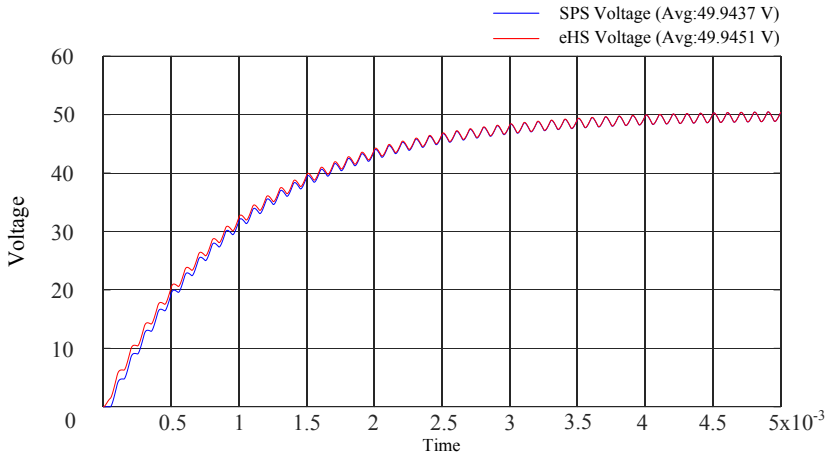


Figure 4.31. SPS and eHS Output for Gs = 0.237 (from the algorithm) in the Normal Buck Converter

B. Buck Converter with a Shorted Diode

As discussed in Section 4.3.3, when both switches are ON in the buck converter it resembles a buck converter with a shorted freewheeling diode. Table 38 shows output from the eHS and SPS solvers using the G_s parameter from the algorithm and GsGui2. Figure 4.32 and Figure 4.33 shows the output voltage of the two solvers with the two switch conductance values.

Table 358. Output of the Buck Converter With Shorted Diode

G_s = 0.05 (From GsGui2)		
SPS Voltage (Avg)	eHS Voltage (Avg)	error
24.973 V	0.2493 V	99 %
G_s = 0.237 (From Algorithm)		
SPS Voltage (Avg)	eHS Voltage (Avg)	error
24.973 V	1.1525 V	95.38 %

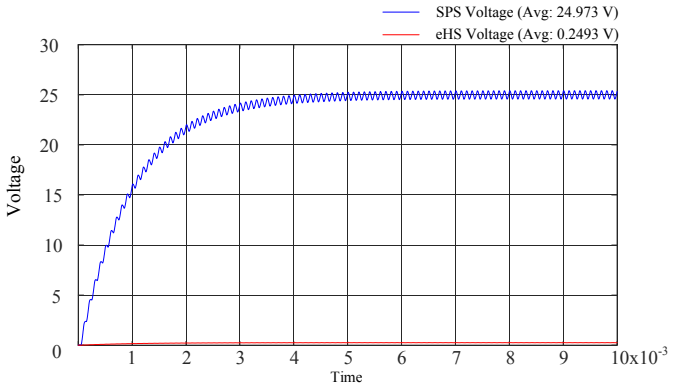


Figure 4.32. SPS and eHS Output for G_s = 0.05 (from GsGui2) in the Buck Converter with Shorted Diode

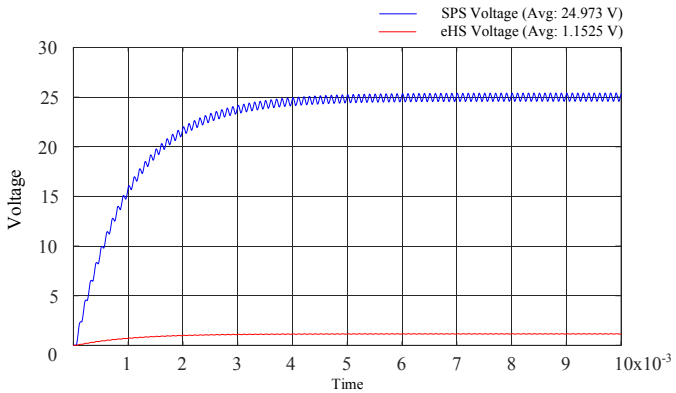


Figure 4.33. SPS and eHS Output for G_s = 0.237 (from Algorithm)

Table 38 indicates that the errors between the SPS and eHS solvers are very high in the buck converter with the shorted freewheeling diode for the chosen G_s parameter. Hence it can be concluded that the G_s parameter returned by the algorithm is not suitable for this circuit.

C. Buck Converter with an Open Diode

The circuit in Section 4.3.4, corresponds to the operation of a buck converter with an open freewheeling diode. The switch conductance from the algorithm and the optimization tool are again tested in the circuit, the output is presented in Table 39, Figure 4.34 and Figure 4.35 shows the output of the buck converter with these two switch conductance parameters.

Table 39. Output of the Buck Converter with Open Diode

G_s = 0.05 (From GsGui2)		
SPS Voltage (Avg)	eHS Voltage (Avg)	error
1.2652 V	0.119 V	90.59 %
G_s = 0.237 (From Algorithm)		
SPS Voltage (Avg)	eHS Voltage (Avg)	error
1.265 V	3.03 V	139.49 %

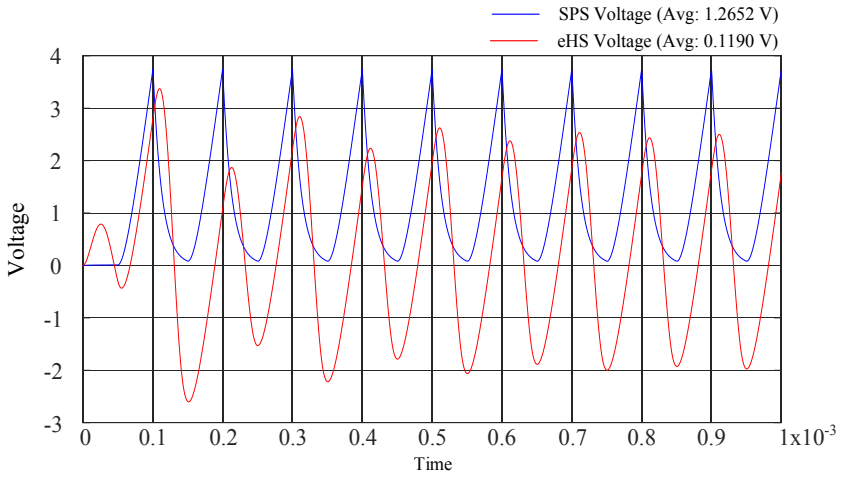


Figure 4.34. SPS and eHS Output for Gs = 0.05 (from GsGui2) in the Buck Converter with Open Diode

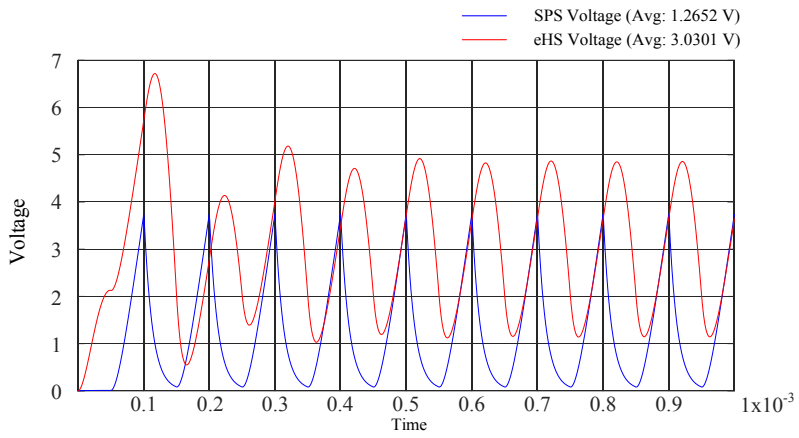


Figure 4.35. SPS and eHS Output for Gs = 0.237 (from Algorithm) in the Buck Converter with Open Diode

Section 4.2.2 had optimized a G_s parameter for the buck converter with an open freewheeling diode. The error between eHS and SPS solvers was significantly less compared to the error when the G_s from the present implemented algorithm is used.

4.4 Conclusion

This chapter discusses two techniques for optimization of the switch conductance parameter. The results from each technique were tested and validated using different circuits operating under normal and faulty conditions.

Operating under normal conditions, with LCA activated, it was found that both methods worked well. However, optimization technique using the RMS values of switches currents and voltages performed better. The optimization technique using eigenvalues did not take into account the converter's ratings while computing the G_s parameter(s).

While operating under faulty conditions the optimization technique using eigenvalues did not produce good results. The RMS method on the other hand did reduce the errors between SPS and eHS but not within acceptable limits (2%), it was also not able to optimize the conductance parameter accurately for open circuit conditions with high transient voltages across the switch during switch turn OFF. In this case the switch conductance value is on the lower side and the output voltage of the eHS didn't match very well with those of SPS's.

Chapter 5. Evaluation of Efficiency of the Three-Level Inverter using Offline Simulation

5.1 Introduction

In this chapter the G_s parameters returned by GsGui2 and by using the RMS method shall be examined using the eHS offline simulation block. This block from Opal-RT enables the simulation of power electronic converters using the Pejovic switch model. The three-level inverter shall be simulated using both eHS offline block and SPS, the results from them shall be compared. This would allow the evaluation of the artificial losses incorporated into the system because of the Pejovic switch model and also provide insight to the application of the G_s using the RMS method into the virtual model of eHS. The offline simulation enables the maintenance of the fidelity of the signals and provides more accurate comparisons. The difference between the output of eHS and SPS are expected to be within 2 % in-order to be deemed reliable.

5.2 Verification Model for Offline eHS Simulation

Figure 5.1 shows the model of the eHS Offline test circuit. The circuit has four main blocks namely the reference wave generation, gate pulse generation, SPS block with the universal bridge and the eHS offline block.

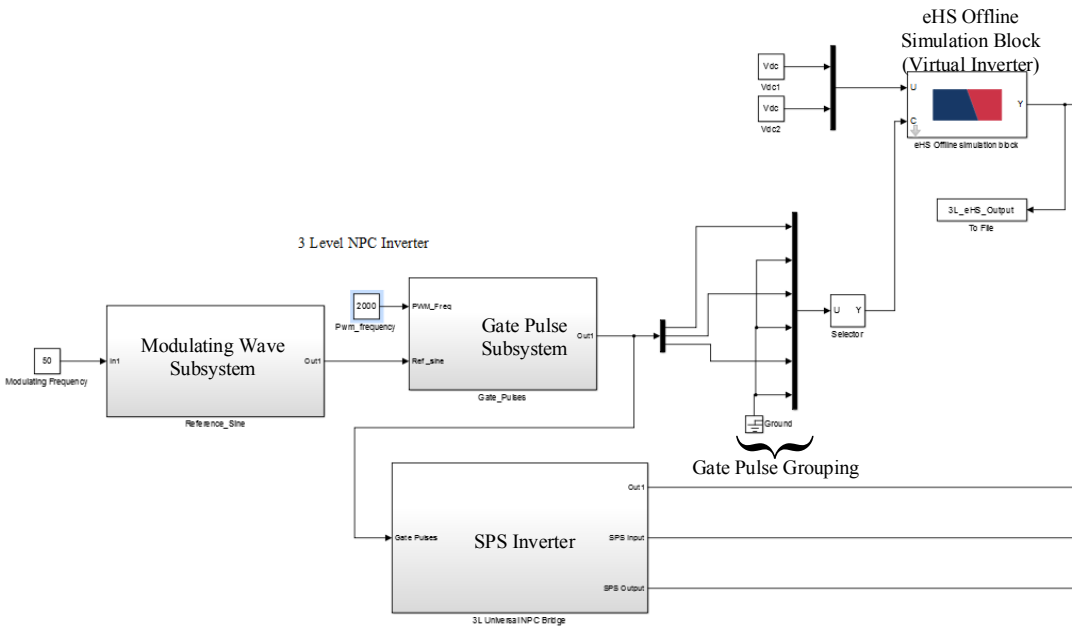


Figure 5.1. The eHS Offline Circuit for the Three-Level Inverter

The operation of the gate generation block is similar to the one used for eHS online, its main function is the generation of modulating signals, sizing of those modulating signals and gating pulse generation.

The gate pulses are generated by the gate pulse generation block, this block compares the modulating sines with a carrier wave with amplitude between 0 and 1. The gating pulses are grouped together in four vectors, the first one being for the upper level outer switch, the second for the complimentary lower inner switch along with the required ON delay. The third and the fourth vectors are meant for the upper inner switch and the lower outer switch respectively.

5.3 SPS Circuit with the Universal Bridge

The reference SPS Bridge of the three-level inverter is shown in Figure 5.2, the purpose of this bridge is similar to the one used in online simulation. It is from this bridge that the eHS solver extracts all the *netlist* details to be used in the simulation.

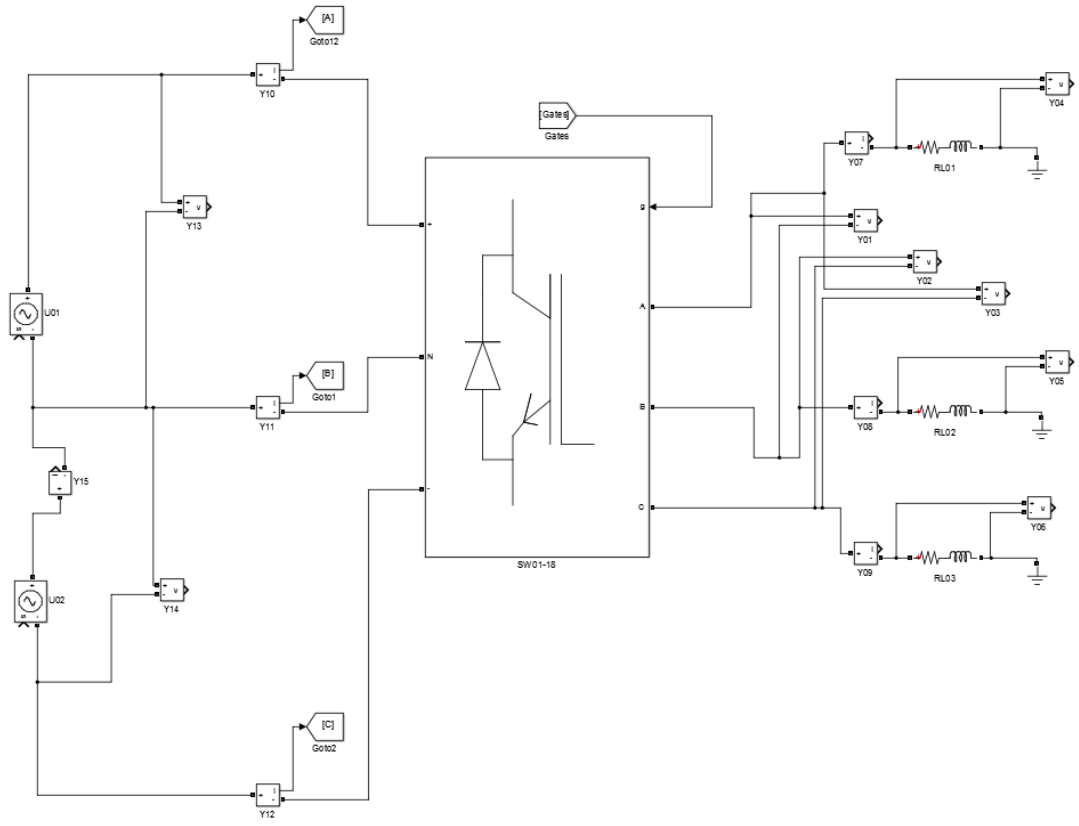


Figure 5.2. The SPS Bridge of the Three-Level Inverter

5.4 eHS Offline Block

The eHS Offline block enables the simulation of power electronic converters with the eHS solver with very low time steps, but FPGA is not used in this simulation. This offline simulation happens in non-real time but the output would be equivalent to those of a real-time simulation. The Loss Compensation Algorithm (LCA) will always be engaged during the offline simulation, this would compensate for the artificial losses in the Pejovic switch model. Two conditions in the three-level inverter shall be analyzed in eHS offline simulation

A. Three-level inverter connected to a 0.9 power factor load
B. Three-level inverter connected to an unbalanced load

These two cases can be used to evaluate the impact of the artificial losses in the eHS model and the ideal inverter simulated in SPS.

A. Three-level inverter connected to a 0.9 power factor load

Figure 5.3 shows the output of the eHS and SPS inverter when the inverter supplies to a 0.9 power factor load as in Section 3.5.3, the G_s parameters used are G_{s1} (outer switch) = 0.029459 and G_{s2} (inner switch) = 0.01473 which were provided by GsGui2, the eHS optimization tool. Some oscillations are seen in the lower half of the eHS voltage waveform, which means that the G_s parameters may have not been fully optimized. It is to be reckoned that, when GsGui2 provides the G_s parameters for the three-level inverter, the G_s for the upper switch contains values for both the switch and the freewheeling diodes. Furthermore, it can be seen that in most cases, G_s from GsGui2 for the outer switch and the freewheeling diodes is about twice of that for the inner switch. Therefore, the G_s from the RMS components is modified to include the clamping diodes as well, the oscillations further decrease as shown in Figure 5.4. It is seen that the oscillations present in the first case using G_s from GsGui2 has reduced after the switch conductance values calculated from RMS values were used. The results for the modified value of G_s are tabulated in Table. 41.

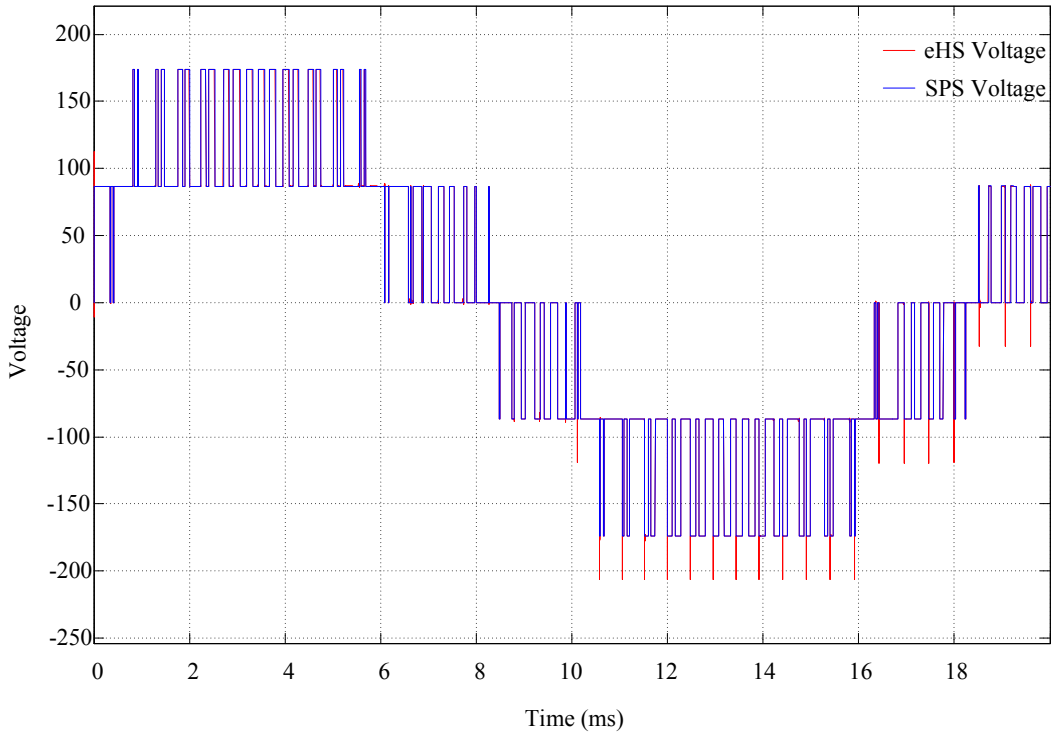


Figure 5.3. The eHS and SPS Inverter Line Voltage Output Using G_s from GsGui2

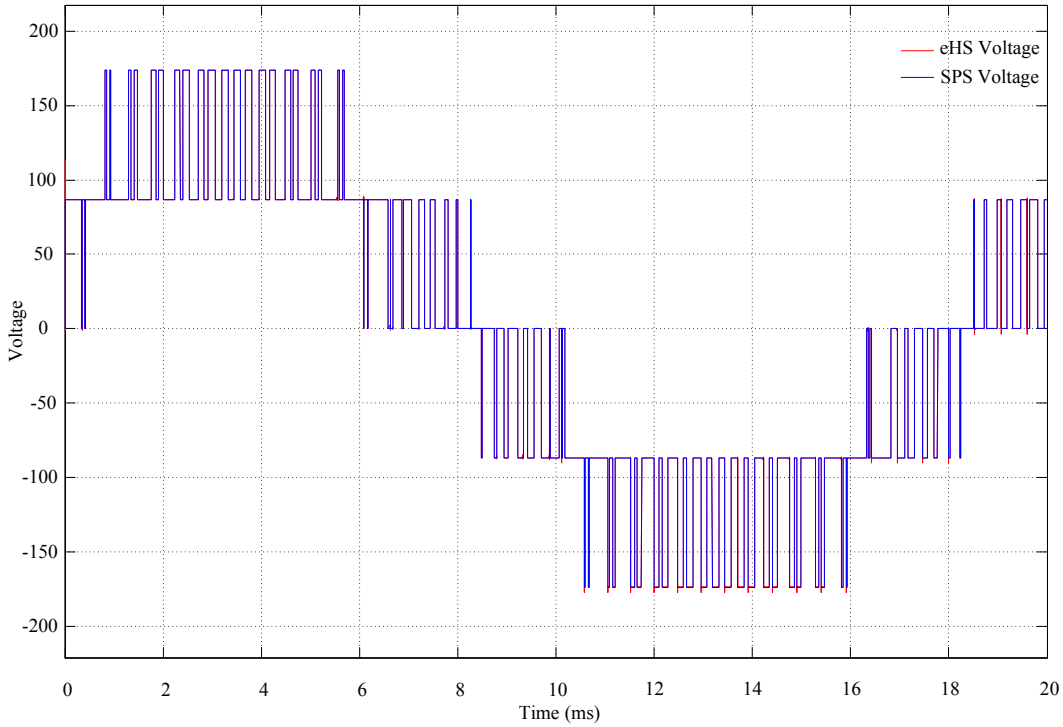


Figure 5.4. The eHS and SPS Inverter Line-Line Voltage Output Using Modified G_s Calculated from RMS Components

Table 360. Output of the SPS and eHS Inverter at 0.9 PF Load

G_{s1}: 0.0407 G_{s2}: 0.0376 (obtained from RMS parameters)		
Parameters	SPS Inverter	eHS Inverter
V_{L-L}	101.868	101.882
I_L	2.368	2.37
PWM Freq (kHz)	2	2
V_{dc}	173.8	173.8
THD(V_{L-L}) %	39.54	39.53
THD (I_L) %	7.16	7.17
Input Power (W)	365.723	365.945
Output Power (W)	365.130	365.330
Efficiency (%)	99.84	99.83

B. Three-level inverter connected to an unbalanced load

Figure 5.5 shows the output of the eHS and SPS inverter when it is connected to an unbalanced load using the G_s parameters from RMS components of current and voltage. The resistive load is 15 Ω, 15 Ω and 70 Ω in the R, Y and B phase respectively, the inductive load is 32mH for all the phases. The results and comparisons are made in Table 42. In this case too, the G_s values calculated using RMS voltage and current components of the switches were conditioned to include the clamping diodes.

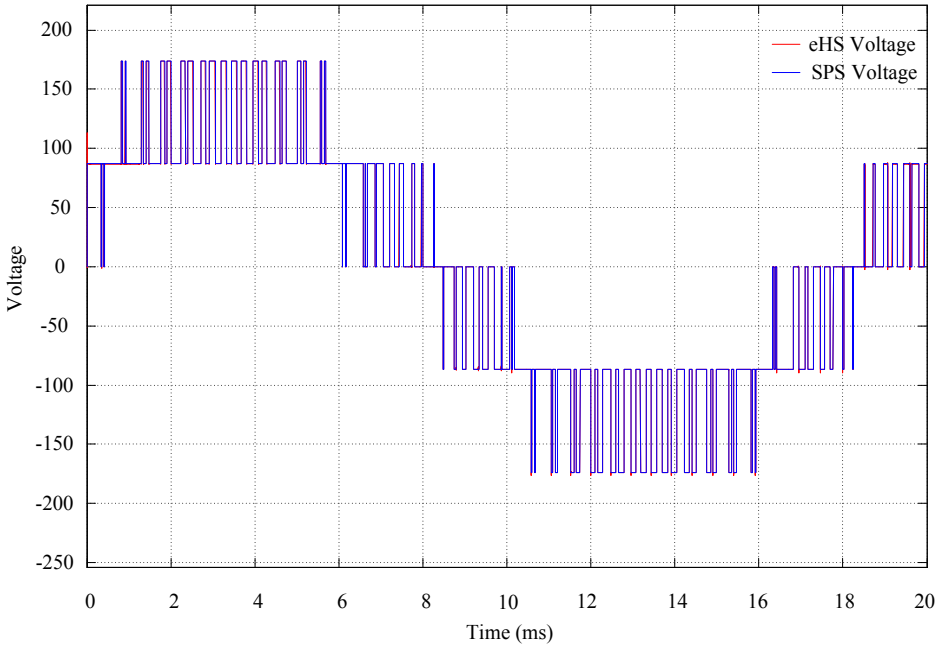


Figure 5.5. The eHS and SPS Inverter Line-Line Voltage Output, when connected to an Unbalanced Load

Table 371. Comparison of the SPS and eHS Inverters connected to an Unbalanced Load

G_{s1}: 0.0475 G_{s2}: 0.0448 (obtained from RMS parameters)		
Parameters	SPS Inverter	eHS Inverter
V_{L-L}	101.761	101.842
I_L	3.055	3.055
L (mH)	32	32
PWM Freq (kHz)	2	2
V_{dc}	173.8	173.8
THD(V_{L-L}) %	39.54	39.50
THD (I_L) %	3.16	3.17
Input Power (W)	333.902	334.337
Output Power (W)	333.353	333.758
Efficiency (%)	99.84	99.83

5.4 Conclusion

This chapter does an offline simulation of the three-level inverter using the eHS offline simulation block. The G_s found by using the RMS values of the switch currents and voltages or any other may have to be conditioned and formatted properly for the eHS solver to be able to use them. It was observed that the three-level model in eHS takes in the G_s parameter of the top switch and the freewheeling diodes clubbed together. The eHS optimization tool GsGui2 is designed to produce the switch conductance parameters in a format required by the eHS solver. But when other methods are used, formatting or grouping of the switch conductance parameters may be necessary depending upon the circuit being simulated.

Chapter 6. Conclusion and Future Work

Conclusion

A real-time simulation of a three-level inverter was done in this thesis. The simulation was done with a relatively new technique based on simulating fast switching power electronic converters on FPGA's. An OPAL-RT OP4150 simulator was used for the real-time simulation with a very low time step, the minimum time step available for the model in the eHS solver was 255ns. The results of a virtual model were compared and validated against a physical test bench. The HIL testing of a three-level inverter against a real setup has not been done earlier, this test enables a complete validation including results from different solvers such as SPS and ensures that the virtual model is indeed running in real-time. This work would also help researchers working in the field of real-time simulation of power converters.

The process of validating the three-level inverter and a summary of the results are discussed in Chapter 3. The test was done by subjecting both the real and virtual inverters to different loads, the output for each situation was tabulated and compared. It was found that the results obtained from both inverters (virtual and real) were very close even when they were supplying unbalanced loads.

In an earlier work while validating a two-level inverter [27], it was found that the eHS solver simulating the virtual model did not produce good results, when operating under faulty conditions. This pushed for the need of a more methodical and generic way of optimizing the switch conductance parameter (G_s). This was particularly significant for more complex circuits where the prediction of the G_s parameter(s) by hit and trial means would be very difficult. Two techniques were chosen to be tested for obtaining suitable switch conductance parameters. One of them was based upon minimizing the Euclidian distances between the eigenvalues of the matrices formed by the FAMNM network, and those formed by replacing the discrete switch models with ideal switches. This was done to reduce the effect of artificial losses in the discrete switch model. Another, more generic approach for optimizing the switch conductance parameter was also tested. This method utilized the current and voltage information of each switch of a circuit to obtain the G_s parameters. Thus, the power flow through each switch in a circuit can be tuned. The switch currents and voltages can be easily determined by simulating the circuit in a

non-real-time environment or by manual calculations as well. A number of circuits were tested successfully using the G_s values evaluated from this method. The test results were however, not satisfactory in the presence of transients in the circuit.

Contributions of the Thesis

A detailed procedure for real-time simulation of a multilevel inverter with a hardware test bench has been proposed. The work shall also be helpful to users who intend to interface real-time simulators with physical three-level inverter test benches.

The validations of the earlier real-time models were restricted only to the outcomes of the benchmark solvers, such as SPS, PSIM etc. This thesis established a validation work involving a three-level inverter physical test bench and its equivalent virtual model running together.

This thesis was able to propose a more generic way of finding the switch conductance parameter, G_s, that can be used with different topologies and when operating under faulty conditions. One advantage of the proposed technique is that, there is no hit and trial involved in tuning the G_s parameter. In certain cases the switch conductance parameters calculated through this technique did perform better than the ones returned by the available GsGui2. It was also found that it is necessary to understand how the eHS solver interprets the G_s parameters; care must be taken to condition the parameters properly depending upon the circuit model before they are used in a simulation.

Another approach for optimization the G_s parameter was tested and the results were put to trial. This approach was based upon minimization of Euclidean distances between the eigenvalues of the admittance matrices of a circuit with ideal switch and the same circuit containing Pejovic switch. An attempt was made to obtain G_s values that can be used for normal and faulty conditions in a circuit. And even though a G_s parameter was obtained, which happened to be very different than the one optimized from the available optimization tool, GsGui2; it produced good results with normal circuit conditions. However, once faults were introduced, this approach did not perform very well.

Future Work

The attempt to optimize a G_s parameter that can be used both for a normal and a faulty circuit was not successful. However, the ‘Scenario Management’ option that comes along with the eHS

online solver, it is possible to make changes in the RLC components of a given circuit which is being simulated in real-time. This option can be used to introduce faults into the circuit during the course of a real-time simulation and the changes in the behavior of the circuit can be seen in real-time. More work is hence recommended using the Scenario Management option to explore the possibility of having G_s values performing well in both normal and faulty conditions.

BIBLIOGRAPHY

[1] Najm, F. (2010). Circuit simulation. Hoboken: J. Wiley & Sons.

[2] Chung-Wn Ho, Albert E Ruehli, Pierce A. Brennan, “The modified Nodal Approach to Network Analysis”. IEEE Transactions on Circuits and Systems, Vol. Cas-22 no 6, pp. 505-509, June 1975

[3] L.M. Wedepohl and L. Jackson, "Modified nodal analysis: an essential addition to electrical circuit theory and analysis", Engineering Science and Education Journal (Volume: 11, Issue: 3, June 2002)

[4] R. Razzaghi, M. Paolone and F. Rachidi, "A general purpose FPGA-based real-time simulator for power systems applications", ISGT EUROPE, 2013 4th IEEE/PES

[5] P. Pejovic and D. Maksimovic, "A method for fast time-domain simulation of networks with switches," in IEEE Transactions on Power Electronics, vol. 9, no. 4, pp. 449-456, Jul 1994

[6] S. Y. R. Hui and C. Christopoulos, "A discrete approach to the modelling of power electronic switching networks," 20th Annual IEEE Power Electronics Specialists Conference, Milwaukee, WI, 1989, pp. 130-137 vol.1.

[7] S. Abourida, S. Cense, C. Dufour and J. Bélanger, "Hardware-in-the-loop simulation of electric systems and power electronics on FPGA using physical modeling," 4th International Conference on Power Engineering, Energy and Electrical Drives, Istanbul, 2013, pp. 775-780.

[8] https://www.opal-rt.com/solver-ehs/

[9] https://www.slideshare.net/OPALRTTECHNOLOGIES/opalrt-real-time-simulation-using-rtlab

[10] https://www.slideshare.net/OPALRTTECHNOLOGIES/opalrt-and-ansys?qid=541fc399-6e6d-4152-aa3f-d76387d22778&v=&b=&from_search=11

[11] https://www.slideshare.net/OPALRTTECHNOLOGIES/opal-rt-hypersim-seminar-in-india-2013

[12] http://www.ni.com/white-paper/11266/en/

[13] https://www.intel.com/content/www/us/en/products/chipsets/desktop-chipsets/x99.html

[14] Aung Myaing and Venkata Dinavahi "FPGA-Based Real-Time Emulation of Power Electronic Systems with Detailed Representation of Device Characteristics", IEEE Transactions on Industrial Electronics, Volume: 58, Issue: 1, Jan. 2011

[15] Morteza Rezaei Larijani, Mohammad-Reza Zolghadri and Mahmoud Shahbazi "Design and implementation of an FPGA-based Real-time simulator for H-Bridge converter", 7th PEDSTC, 2016

[16] Jean Belanger, Amine Yamane, Andy Yen, Sebastien Cense, Pierre-Yves Robert, "Validation of eHS FPGA reconfigurable low-latency electric and power electronic circuit solver" Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE

[17] K. Ou et al., "Research and application of small time-step simulation for MMC VSC-HVDC in RTDS," 2014 International Conference on Power System Technology, Chengdu, 2014, pp. 877-882.

[18] Handy Fortin Blanchette, Tarek Ould-Bachir and Jean Pierre David, "A State-Space Modeling Approach for the FPGA-Based Real-Time Simulation of High Switching Frequency Power Converters", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 59, NO. 12, DECEMBER 2012

[19] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel converters-a new breed of power converters," Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE, Orlando, FL, 1995, pp. 2348-2356 vol.3.

[20] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Transactions on Industrial Electronics (Volume: 49, Issue: 4, Aug 2002)

[21] Sandro Calligaro, Federico Pasut, Roberto Petrella and Alessandro Pevere, “Modulation Techniques for Three-Phase Three-level NPC Inverters: A Review and a Novel Solution for Switching Losses Reduction and Optimal Neutral-Point Balancing in Photovoltaic Applications”, APEC, Long Beach, CA, USA, 2013

[22] Rekha Agrawal, Jitendra Kumar Tandekar and Shailendra Jain. (2016). Multi-Carrier Pulse Width Modulation Schemes for Multilevel Converters. Presented at 2016 IEEE Students' Conference on Electrical, Electronics and Computer Science.

[23] J. Rodriguez, S. Bernet, Peter K. Steimer and Ignacio E. Lizama, “A survey on Neutral-Point-Clamped Inverters,” IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Dec. 2010.

[24] K. S. Amitkumar and G. Narayanan, "Simplified implementation of space vector PWM strategies for a three-level inverter," 2012 IEEE 7th International Conference on Industrial and Information Systems (ICIIS), Chennai, 2012, pp. 1-6

[25] https://www.opal-rt.com/wp-content/themes/enfold-opal/pdf/L00161_0436.pdf

[26] Nicolas Kamel, "Optimization of Very Low Time Step FPGA-Based Simulations Using a Fixed Admittance Matrix Approach," M.Sc Thesis, ETS, UDEM, Montreal,Quebec, 2014.

[27] Ahmed Kotb Abdalla, "Validation and Enhancement of Two-Level Inverter Models for Very Low Time-Step Real-Time Applications," M.A.Sc Thesis, Concordia University, Montreal, Quebec, 2017.

[28] http://nptel.ac.in/courses/108108035/4

[29] Hans-Peter Krug, Tsuneo Kume and Mahesh Swamy.(2004) Neutral-Point Clamped Three-Level General Purpose Inverter - Features, Benefits and Applications. Presented at 351h Annual IEEE Power Electronics Specialists Conference, Aachen, Germany.

[30] Application Note, AN-11001 3L NPC & TNPC Topology, Rev 05, Semikron, Nurnberg, 2015-10-12

[31] https://www.opal-rt.com/wp-content/themes/enfold-opal/pdf/L00161_0124.pdf

[32] https://www.opal-rt.com/wp-content/themes/enfold-opal/pdf/L00161_0407.pdf

[33] Christian Dufour, “Method and system for reducing power losses and state-overshoots in simulators for switched power electronic circuit ”, US Patent 9,665,672 B2, May 30, 2017

[34] R. Razzaghi, C. Foti, M. Paolone and F. Rachidi, “A Method for the Assessment of the Optimal Parameter of Discrete-Time Switch Model”, Electric Power Systems Research, 16 March 2014

[35] M. Matar and R. Iravani, "FPGA Implementation of the Power Electronic Converter Model for Real-Time Simulation of Electromagnetic Transients," in IEEE Transactions on Power Delivery, vol. 25, no. 2, pp. 852-860, April 2010.

[36] T. Feng and H. Liu, "The Computer Realization of the QR Decomposition on Matrices with Full Column Rank," 2009 International Conference on Computational Intelligence and Security, Beijing, 2009, pp. 76-79.