Fault Protection Scheme for DC Nanogrids Based on the Coordination of Fault-Insensitive Power Electronic Interfaces and Contactors

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Abstract

Fault Protection Scheme for DC Nanogrids Based on the Coordination of Fault-Insensitive Power Electronic Interfaces and Contactors

Saroosh Saeed

DC power distribution systems (especially DC nanogrids) are becoming a great area of interest for researchers, that can lead to a better integration of DERs and supplying local loads in a more efficient way compared to AC systems. DC nanogrids for Net-Zero Energy Homes (NZEHs) are expected to include a number of Distributed Energy Resources (DERs) in relatively close proximity. The control structure can be based on a hierarchical approach with DC bus signaling (DBS). Power electronics interfaces (uni-directional Boost for sources and bi-directional Class-C for storage units) are usually employed as the interface of DERs in DC nano and microgrids. However, these power interfaces are fault-sensitive, meaning that in case of a fault in the DC bus, with a DC bus voltage lower than the source voltage, the upper anti-parallel diode conducts. Thus, one loses control of the current injected into the DC nanogrid. In conventional systems, this current is typically high enough to open the DC Circuit Breakers (CBs). One issue in DC nanogrids is the difficulty in making only the DC CBs close to the fault to open. Various control schemes have been developed for power balance and energy management, but fault protection still remains an issue.

This Thesis discusses the realization of a fault detection and isolation scheme which is based on the coordination of fault-insensitive power electronics interfaces and low cost contactors. A bi-directional 4-switch DC-DC converter is employed in this work which allows the control of the injected current regardless the source voltage to be lower or higher than the DC bus voltage. Fault current limiting and blocking capabilities of the fault-insensitive converter allows the use of low cost and lower rated contactors. The identification of which segment(s) of the DC nanogrid is(are) faulted and which contactor(s) should open is based on peer-to-peer communication between DERs. Following the detection of a fault, the DERs decrease the injected current to a value low enough for safe action of the contactors.

Finally, the proposed concepts are verified with hardware experiments. Experimental results with power electronics interfaces operating with DC Bus Signaling (DBS) with VI curves including droop, current limiting and a CAN communication system are presented. It is shown that the DC grid can be protected against faults by coordinating the action of power interfaces and contactors, and only the faulted segment is isolated keeping the healthy part of the DC nanogrid energized.

I dedicate this work to my father, who has passed away during my studies…

Acknowledgements

In the name of ALLAH (God) Almighty, the Most Compassionate, the Most Merciful, all praises and thanks be to HIM. This is by the grace of God.

Then, I would like to take this opportunity to express my deep gratitude to my advisor, Professor Luiz A. C. Lopes for his invaluable guidance and continuous support throughout this work. Although highly passionate about power electronics, his very broad knowledge and passion has greatly influenced my perception of engineering in general. In the same time, his sense of humor, intelligence, positive attitude and character changed my perception of life, which will be beneficial for my career.

In particular, I am thankful to the members of my research committee, for their time and guidance through the review of the thesis. It is my pleasure to acknowledge my colleagues in the Power Electronics and Energy Research (PEER) group of Concordia University; your friendship and encouragements helped me to overcome the obstacles. Special thanks to Mathews Boby, Ahmad Malkawi, Sivanagaraju and Tamanwe Payarou who were always willing to help and share their valuable experiences. I am highly thankful for my friends, Khaled Elamari and Zaid Zaid for their encouragement during the program journey.

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Nomenclature

AC: Alternating Current

ADC: Analog-to-Digital Converter

CAN: Controller Area Network

CB: Circuit Breaker

CS: Current Sensor

DBS: DC Bus Signaling

DC: Direct Current

DERs: Distributed Energy Resources

ESSs: Energy Storage Systems

LTF: Loop Transfer Function

LV: Low Voltage

NZEHs: Net-Zero Energy Homes

PCB: Printed Circuit Board

PV: Photovoltaic

PWM: Pulse Width Modulation

RES: Renewable Energy Source.

T.F: Transfer Function

Chapter 1 Introduction

With the increasing demand of energy and the climate concerns over burning fossil fuels, the use of renewable energy sources (RESs) is gaining popularity all over the world. The research and development in the evolution of power network at the distribution level facilitates the integration of these resources that open new possibilities. An isolated power system can be formed with power sources and loads or combined with other local generators —a microgrid or nanogrid [1]. A nanogrid is similar to the microgrid, but smaller in size, with a capacity of up to 10's of kW [2]. Nanogrids are used typically in residences and small buildings with renewable energy sources such as photovoltaics (PV) and wind energy and can be connected or not with the existing utility grid. However, these sources (renewable) are stochastic and fluctuating in nature. In order to provide backup power, when the available power of renewable sources is not sufficient to meet the load demand, various energy storage units like batteries and ultra-capacitors need to be added to the system. In fact, the future smart residences/homes would offer high controllability and smart optimization of the system sources and loads to achieve net-zero energy homes (NZEHs), a concept that has been gaining popularity in recent years. The concept of NZEHs is that, by incorporating distributed energy resources (DERs), the buildings/homes will be able to produce the amount of energy they consume in a given period of time: Day, month or year [3]. Nanogrid systems can be based on AC or DC distribution [4] and [7]. However, DC distribution systems have various advantages over traditional AC systems. Most of the modern appliances employ AC-DC converters in their internal circuitry before "driving the load". It is possible to eliminate this conversion stage's associated losses and the intermediate stage of the appliance can be directly fed by the DC nanogrid. Also, most RESs and storage units such as PVs, fuel cells and batteries are inherently DC supplies suitable for NZEHs. What is more, DC-DC interfaces tend to present a higher efficiency than their DC-AC counterparts. Therefore, DC systems seem to be a more promising, straight forward and cost effective solution with higher efficiency and fewer conversion stages as compared with AC-based integration [5].

Power electronic interfaces are used to connect RESs, storage units and plug-in hybrid electric vehicles to the DC Nanogrid. Uni-directional Boost converters are normally employed for sources to convert the voltage to the voltage level of the DC bus. Bi-directional Class-C converters are key power converters used for the interface of storage units to the DC bus. A bi-directional AC-DC

converter is required to interface the AC power grid to the DC Nanogrid. The nanogrid can be operated either connected to the utility grid or in stand-alone/islanded mode. For operation in islanded mode, the converter must have enough power generation and storage capacity to supply the maximum load. In the grid-connected mode, it can be less and depending on the load demand and amount of power generated, power flow can be from the nanogrid to the utility or vice-versa [6]. Figure 1. 1 [7] shows a basic configuration of a DC nanogrid for a future home with generation units (photovoltaic solar cells, wind generators), local storage, plug-in hybrid electric vehicle (PHEV) and loads together with the utility grid connection. It is a dual DC bus system with a 380V higher bus voltage, used to drive high power loads, whereas for lighter loads, a 48V lower voltage bus is used. A lot of research has to be done to decide the voltage levels of DC bus to be utilized in such systems. In this thesis, the aim is to consider power interface operating with the lower voltage DC bus (48V) in a DC nanogrid. However, it can be further extended to any other potential voltage level of operation as well.

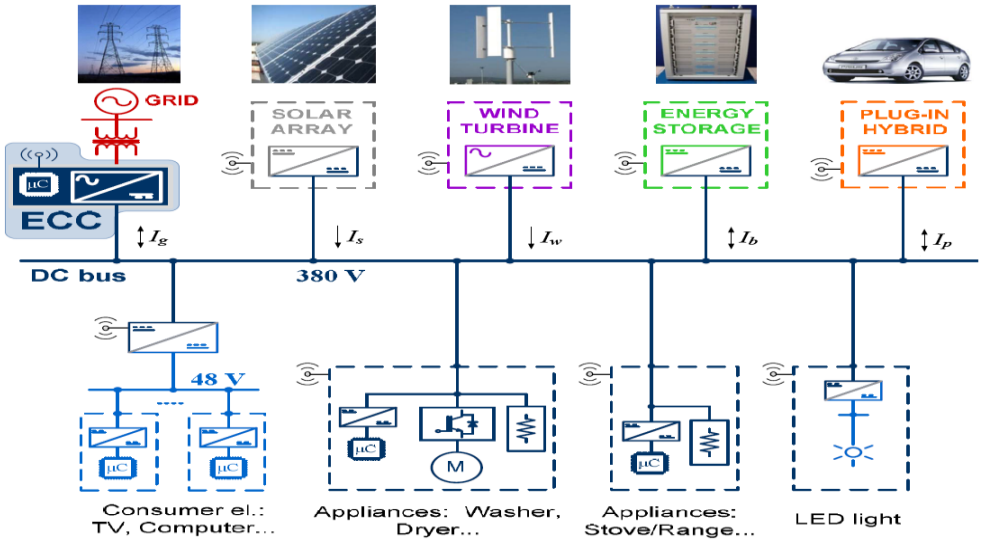


Figure 1.1 Configuration of a DC nanogrid [7].

Another main aspect of the DC nanogrid development is to control and coordinate the power delivered by each DER, based on the availability of power and also the priority of that particular DER. Generally, the method used is the distributed control strategy with DC bus signaling (DBS), which includes droop control that allows various sources to connect directly to the bus [8]. The DERs inject a defined value of current based on their individual VI curve as discussed below. The VI curves typically present a droop and a current limit region. The parameters used to define the

VI curve are mainly the droop slope ($\Delta V/\Delta I$) and the no-load voltage (V_{nl}). The injected current (I_{dc}) is determined based on the DC bus voltage (V_{dc}). As the load demand increases, the bus voltage decreases, increasing the current injected by the DER into the DC bus while operating in the droop region, until the current limit value is reached. The droop region can be described by:

$$V_{dc} = V_{nl} - I_{dc}R_d, \tag{1.1}$$

Where R_d is the droop slope factor given as:

$$R_d = \frac{\Delta V}{\Delta I}, \tag{1.2}$$

Since the advantages of DC distribution systems are significant, various control schemes have been developed for power balance and energy management of a DC nanogrid, but fault protection still remains an issue [9] - [11]. The faults of DC systems are much more difficult to interrupt, locate and isolate than AC. The technology for AC distribution systems is very mature and the protection standards are well defined, but the same cannot be directly applied to a DC nanogrid. AC circuit breakers that are very common and rely on natural zero crossings of AC current are normally employed to interrupt the fault in AC systems. Unlike AC, the DC current has no natural zero crossing points resulting in aggressive DC arcs. This leads to a requirement of larger size and higher rating equipment. Due to the lack of natural zero crossing point in DC current, the existing AC breakers cannot be directly used for DC systems. These breakers can be further modified but this would lead to a more complicated design with higher cost [12]. Some manufacturers like EATON and ABB launched DC circuit breakers but still the devices needs to open high DC currents and they are bulky in size and much expensive [13]- [14]. Another issue in the DC nanogrid is that impedances between nodes are very small, and the line reactance is almost negligible. This could lead to a rapid propagation of faults across wider areas and locating of DC faults will be more challenging [9]. Several protection solutions are available for DC distribution systems. The solution that has been commonly implemented in DC applications such as solar, marine and traction systems is overcurrent (O/C) DC protection [15]. In [16], this protection scheme has been used in a real Low Voltage DC (LVDC) research site. The circuit breaker is normally employed to open after a certain time, depending on the value of current. However, in order to withstand high fault current during fault conditions, the use of overrated power electronics is required. Some other techniques have also been introduced for fault

protection, which includes rate of current rise (ROCR) protection [17], distance protection [18] and signal processing based protection [19]. Voltage resonance based protection [20] has also been proposed for DC distribution system which estimates the fault distance and location by extracting fault characteristics. These methods are typically applicable for large systems. However, in compact systems (DC nanogrid) the impedances between the nodes are typically very small and it would be difficult to achieve the desired levels of discrimination. Besides, large protection equipments are required to break high fault currents where space and weight are the major constraints of the design. In DC nanogrid, the faults are likely to develop very fast and can also be very severe in nature as compared to larger systems. Since high fault currents and larger equipment are not inherently desirable, this Thesis presents the realization of a fault detection and isolation scheme which is based on the coordination of fault-insensitive power electronics interfaces and low cost contactors.

1.1 Problem statement and proposed solution

The bi-directional Class-C DC-DC converter as shown in Figure 1.2, is frequently employed as the interface of Energy Storage Systems (ESSs) in DC nano and microgrids [21]. It is a simple and effective topology but it is expected to operate with an input (storage medium) voltage lower than the output (DC bus) voltage, what is fine for normal operating conditions. However, it is a fault-sensitive converter, meaning that in case of a fault in the DC bus, with an output voltage lower than the input voltage, the upper anti-parallel diode conducts. Thus, one loses control of the current injected into the DC nanogrid. In conventional systems, this current is typically high enough to open the DC Circuit Breakers (CBs). One issue in DC nanogrids is the difficulty in making only the DC CBs close to the fault to open [20] - [21].

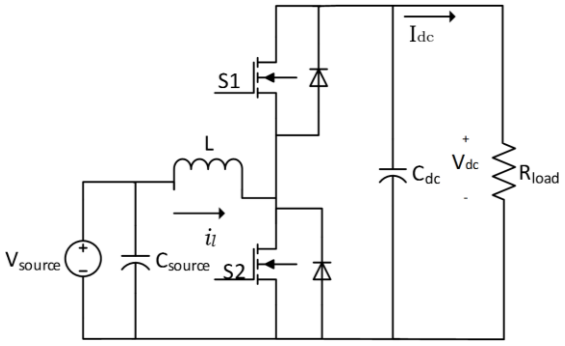


Figure 1.2 Bi-directional Class-C DC-DC converter.

As a solution to this problem, a concept was proposed in [22]. It replaces the DC CBs with lower cost, but lower rated current, contactors and employ a logic to determine which contactors should be opened, to clear the faulted DC nanogrid segment(s). For this, one also needs to be able to control the current injected by the source/storage unit so that the contactors can open with acceptable current levels. In order for the contactors to open with a low current, the power electronics interfaces of all DERs should be fault-insensitive, that is, capable of operating with an input (storage medium) voltage higher than the output (faulted DC bus) voltage. This can be done with a bi-directional 4-switch DC-DC converter [23]. It can operate in Class-C mode when the input voltage is smaller than that of the DC bus and in Buck mode if the input voltage is higher. From now on, this is the topology that will be considered in this Thesis. This fault-insensitive converter would allow a reduction of the injected current to a pre-defined value, following "fault detection," compatible with the rated current of the contactors. The principle of using this fault current limitation and interruption approach with the coordination of fault-insensitive power interfaces and contactors as well as the traditional (tripping by overcurrent) breakers is presented in Figure 1.3 [24]. In the beginning, the current is flowing under normal operating conditions, then a fault occurs. In case of traditional breakers, the current goes very high for a large period of time, until the breaker trips. However, this requires high equipments rating and could also lead to a damage to the power converter. On the hand, with the coordination scheme, when a fault occurs, currents can be actively controlled and limited by the fault-insensitive converters, which can drive the fault current to a predefined value so that the contactors can open with low current and less risk to isolate the faulted section of the bus.

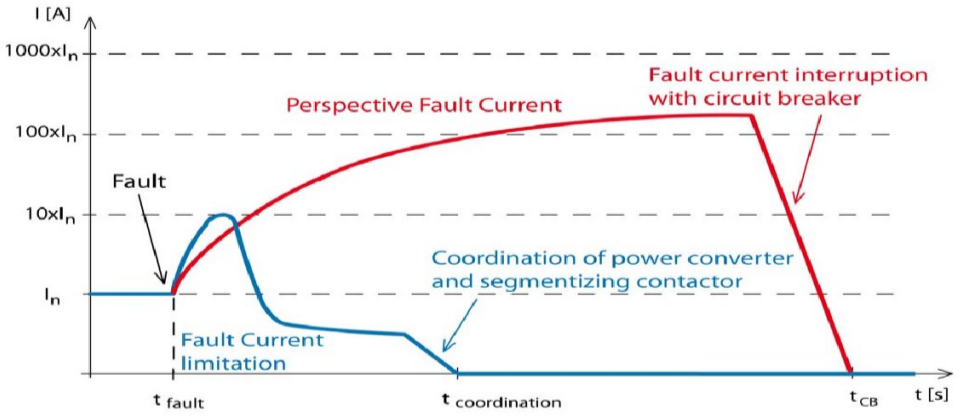


Figure 1.3 Traditional breakers tripping vs fault current limitation and interruption with the coordination of fault-insensitive power interfaces and contactors [24].

Although the fault currents are actively limited by the fault-insensitive converters, this would make more difficult to identify the fault and its location because the amplitude of the fault and gradient might not be much different than the amplitude of normal expected current values. A concept that was proposed in [20] is employed in this work which is based on peer-to-peer communication to identify which segment(s) of the DC nanogrid is(are) faulted and which contactor(s) should open. This can be determined based on the direction of the currents in a given branch, seen from the side of each DER. Whenever the directions of the currents in a branch, as seen by the DERs, are the opposite, that branch is likely faulted and the contactors in their ends should open. Otherwise, they should remain ON. A fast, robust and reliable communication network is required for a nanogrid network. Controller Area Network (CAN), due to its various features like robust error handling, collision free arbitration, high frame rate, acknowledgement capability and differential signal transfer, is employed in this work [25].

1.2 Contributions of the research work

This Thesis focuses on a fault protection scheme for a DC nanogrid with distributed energy resources based on the coordination of fault-insensitive power electronic interfaces and contactors.

The main contributions of this work are as follows:

1) The control of the bi-directional 4-switch DC-DC converter as a conventional Class-C converter until one risks losing control of the inductor current and change to the Buck mode in fault conditions, so that one does not lose the control of current even if the source voltage becomes greater than the DC bus voltage.
2) The logic for communication between neighboring units of the “interface node”, which contains the current sensors and contactors, and between the “interface nodes” and the interface converter of the source/storage units. The description of the interface node is presented in Chapter 3.
3) Experimental verification of the proposed technique.

1.3 Outline of the Thesis

The next Chapters of this Thesis are structured as follows:

In Chapter 2, a bi-directional 4-switch DC-DC converter with a suitable control logic is discussed. The control scheme operates in two modes: Class-C, under normal conditions with DBS, and Buck mode with low current injection when the grid is faulted. The performance of the controller in both modes is also verified by simulation.

Chapter 3 presents a fault protection scheme for DC nanogrids based on the coordination of power electronic interfaces and contactors. The operation of the protection method and fault detection logic is also described in this Chapter. Furthermore, the protection logic for fault location and isolation is developed under various fault scenarios. The Chapter also includes the details of the implementation of peer-to-peer communication between interface nodes using CAN.

In Chapter 4, a prototype hardware is implemented and theoretical calculations are performed for faults at different locations of the system. Finally, the performance of the proposed fault protection scheme is verified through experimental results, which are also presented and discussed in this Chapter.

Chapter 5 concludes the Thesis, highlights its outcomes and suggests topics for further work related to this project.

Chapter 2 Bi-directional 4-Switch DC-DC Converter

To overcome the limitations of fault-sensitivity of the conventional Class-C and Boost converters used in most DER interfaces, a 4-switch topology is employed in this work. The goal is to control the injected current during normal conditions (Class-C) and also when the grid is faulted (low voltage), thus necessitating 2 modes of operation, Class-C and Buck. In this Chapter, the control scheme for the 4-switch converter in normal and fault conditions is presented. The performance of the controller in both modes (Class-C and Buck) is also visualized by simulation.

2.1 Bi-directional 4-switch DC-DC converter

Figure 2.1 shows the bi-directional 4-switch DC-DC converter to be used in this work. The converter is able to control the injected current as the conventional Class-C under normal DC bus voltage condition. As opposed to the conventional Class-C converters, this 4-switch converter will also be able to control the current in fault conditions, what requires the converter to operate in Buck mode. The 4-switch DC-DC converter used in the experiments is a new realization of an existing Class-C (2-switches) Texas Instruments (TI) converter "LM5170EVM-BIDIR Evaluation Module*"* that was designed for a similar application. The TI converter is modified to a 4-switch converter by adding another leg (S1-S2) as shown in Figure 2.1. The specifications of the 4-switch converter was chosen as similar values as the TI converter, with $C_{source} = C_{dc} = 1000\text{uF}$, $L = 200\text{uF}$. The converter will be switching at 30kHz.

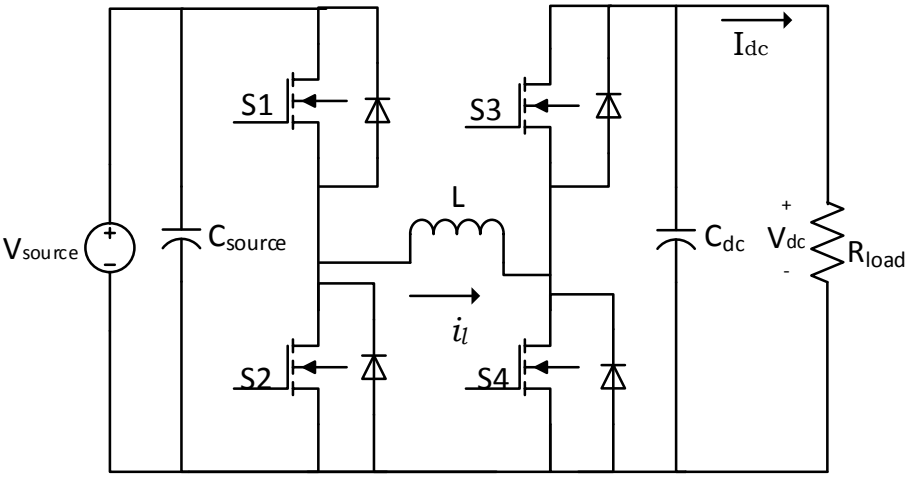


Figure 2.1 Bi-directional 4-switch DC-DC converter.

2.2 Bi-directional 4-switch converter Class-C mode of operation

In this Section, the 4-switch DC-DC converter is demonstrated in Class-C mode. For this mode, the voltage level at the DERs must be lower than that at the common DC bus voltage (V_{dc}). Under normal conditions, the converter operates in the Class-C mode, with S1 ON while S3 and S4 PWMing to regulate the inductor current (I_L).

2.2.1 Switching scheme

The illustration of this switching scheme implementation for the 4-switch converter Class-C mode with forward power flow i.e. $I_L > 0$, is shown in Figure 2.2**.**

1) D_{ON}: The switches S1 and S4 are turned ON while the other 2 switches are complementary, i.e. S2 and S3 are turned OFF.

2) D_{OFF}: S1 and S3 are turned ON and S2 and S4 are turned OFF.

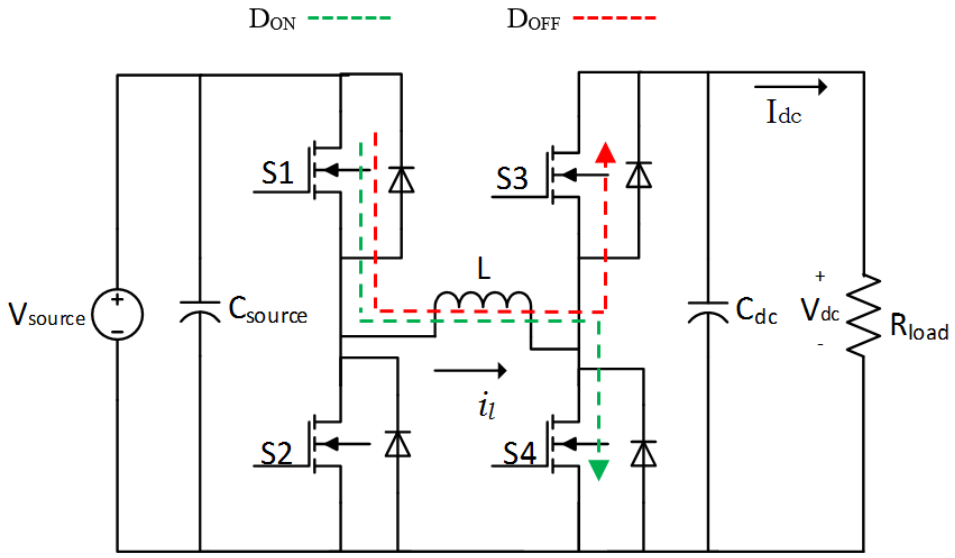


Figure 2.2 Switching scheme of 4-switch converter in Class-C mode.

2.2.2 Controller design

In order to design the inductor current loop controller for the Class-C mode of the 4-switch DC-DC converter, a transfer function is required. The transfer function of the inductor current $i_L(s)$ to the duty cycle $d(s)$ for the Class-C converter has been presented in the literature [26], is given by:

$$\frac{i_L(s)}{d(s)} = \frac{V_{dc}C_{dc}s + \frac{2V_{dc}}{R_{load}}}{LC_{dc}s^2 + \frac{L}{R}s + (1-D)^2}, \quad (2.1)$$

Where C_{dc} is the output capacitor, L is the inductance, R_{load} is the equivalent load resistance and D is the average duty cycle. The operating parameters for the converter are taken as: V_{dc} = 48V, I_L = 10A, R_{load} = 9.6Ω, L = 200μH, C_{dc} = 1000μF, D = 0.5 and V_{source} = 24V. The Bode plot of the plant transfer function is shown in Figure 2.3.

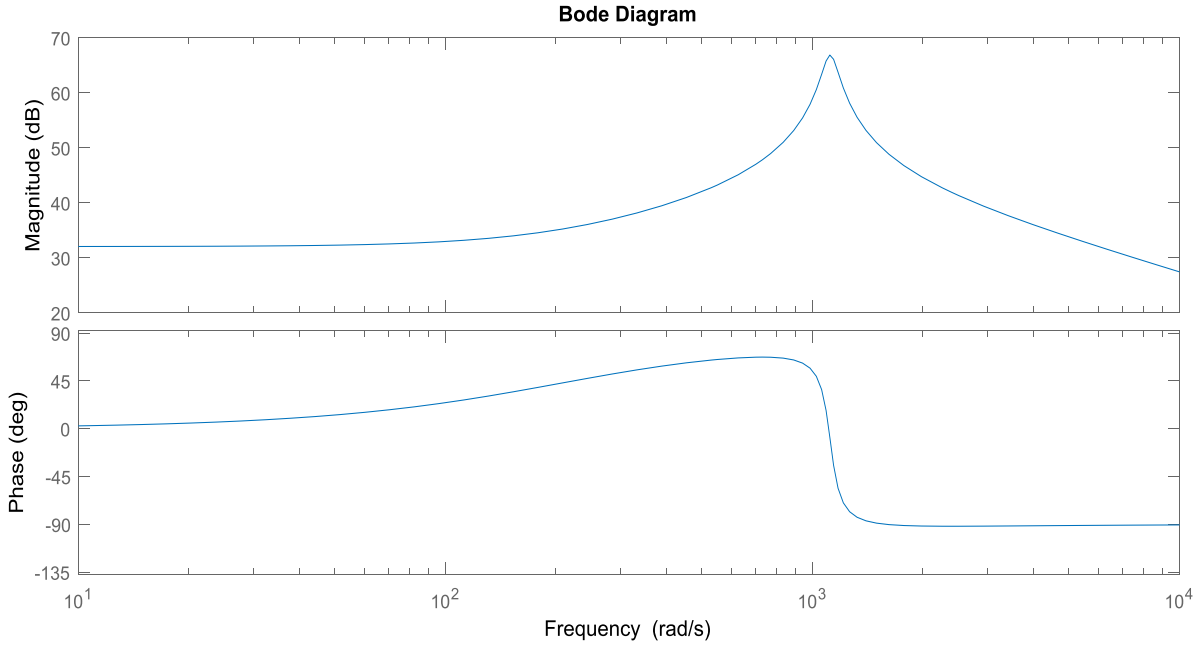


Figure 2.3 Bode plot of the Class-C mode plant.

For the steady state error to be zero, an integrator is required in the controller. The current control loop of the converter employs a PI type-I controller/compensator, with a crossover frequency of $f_x = 0.1f_{sw}$ = 3kHz and a phase margin (PM) of 60^0. The transfer function of the PI type-I controller is:

$$PI(s) = K_P + \frac{K_I}{s} \quad (2.2)$$

The resulting parameters of the PI controller are K_P = 0.07, K_I = 754.06 and τ = 93μs.

2.3 Bi-directional 4-switch converter Buck mode

In this section, the 4-switch DC-DC converter is demonstrated in Buck mode. The Buck mode of operation is required in this application when the voltage at DC bus (V_{dc}) becomes smaller than the input voltage of the converter (V_{source}). Under faulted conditions, the converter will operate in this mode, with S1 PWMing to regulate $I_L = I_{dc}$ at a low value (I_{dc_lcl}) while S3 is ON and S4 is OFF.

2.3.1 Switching scheme

The illustration of this switching scheme implementation for the 4-switch converter Buck mode is shown in Figure 2.4**.** In D_{ON}, the switches S1 and S3 are turned ON while the other 2 switches are complementary, i.e. S2 and S4 are turned OFF. In D_{OFF}, The switch S3 is turned ON while S1, S2 and S4 are turned OFF.

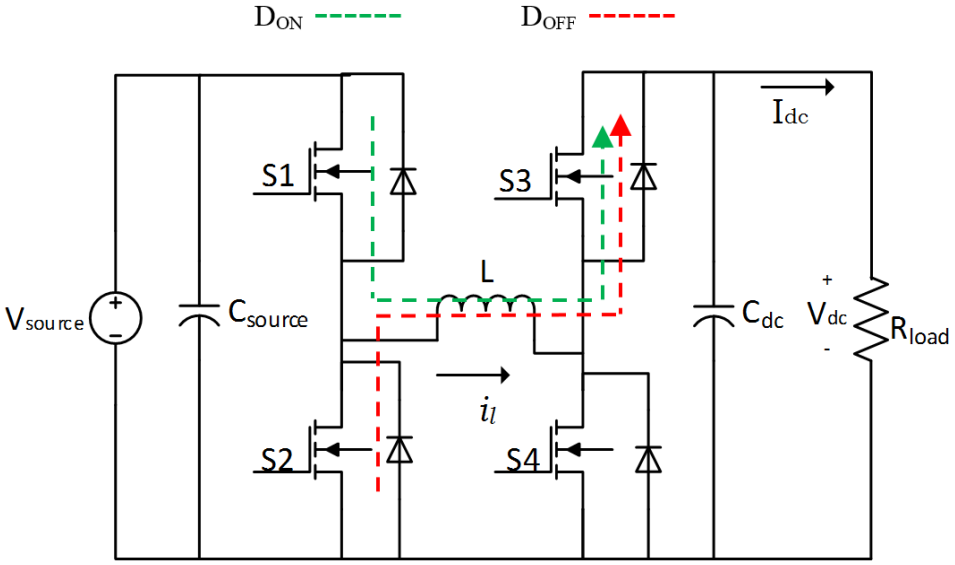


Figure 2.4 Switching scheme of 4-swich converter in Buck mode.

The transfer function of the inductor current $i_L(s)$ to the duty cycle $d(s)$ for the Buck converter has been presented [27], is given by:

$$\frac{i_L(s)}{d(s)} = \frac{V_{source}(1+R_{load}C_{dc}S)}{S^2LC_{dc}R_{load}+SL+R_{load}}, \quad (2.3)$$

The operating parameters of the converter are taken as same as in Class-C mode, however the load impedance (R_{load}) is chosen as 0.5Ω in this case. The Bode plot the plant transfer function is shown in Figure 2.5.

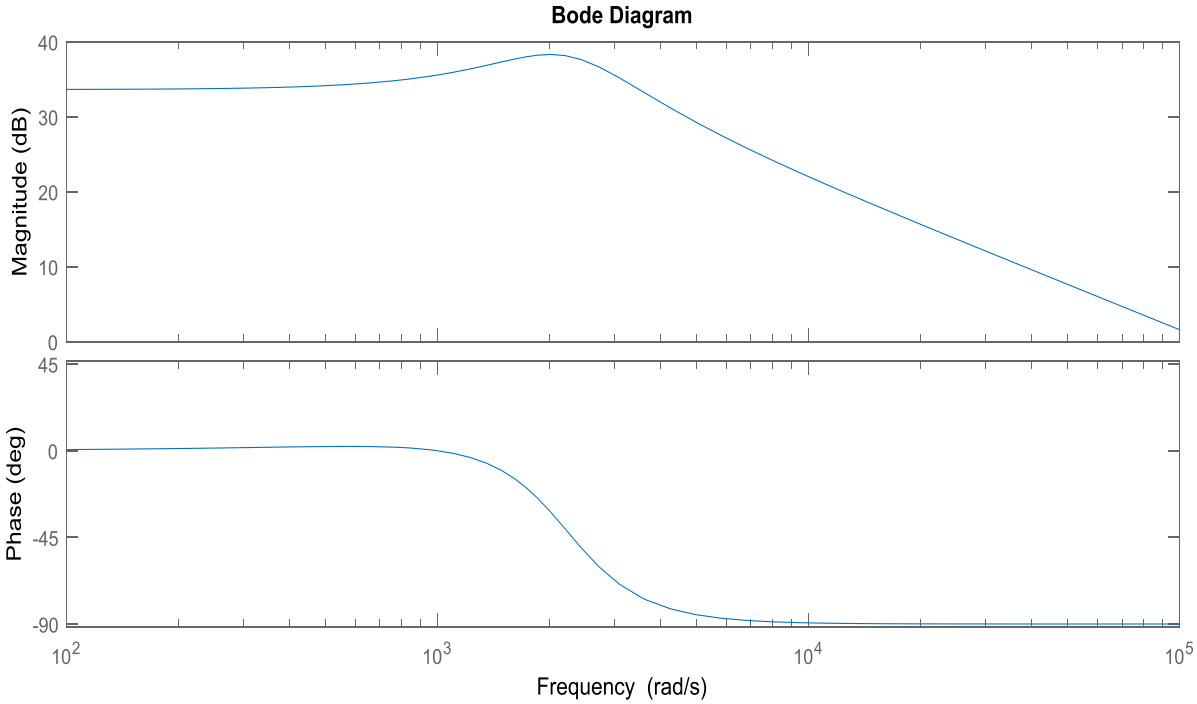


Figure 2.5 Bode plot of the Buck mode plant.

2.3.2 Performance of normal case controller in fault condition

The same PI controller designed for regulating the inductor current in Class-C mode (normal condition) is employed for regulating the inductor/injected current in the Buck mode (fault condition). The performance of the normal mode controller in fault condition is demonstrated by deriving the loop transfer function which is given as:

$$LTF = PI(s)\ 1/V_{ST}\ i_L(s)/d(s), \tag{2.4}$$

Where $PI(s)$ is the current loop controller of the Class-C mode, V_{ST} is the peak value of the sawtooth carrier and $i_L(s)/d(s)$ is the transfer function of plant in Buck mode. The Bode plot of the loop transfer function is shown in Figure 2.6, it can be noticed that the system is stable with a phase margin of 48.1^0 at a crossover frequency of 1.9kHz.

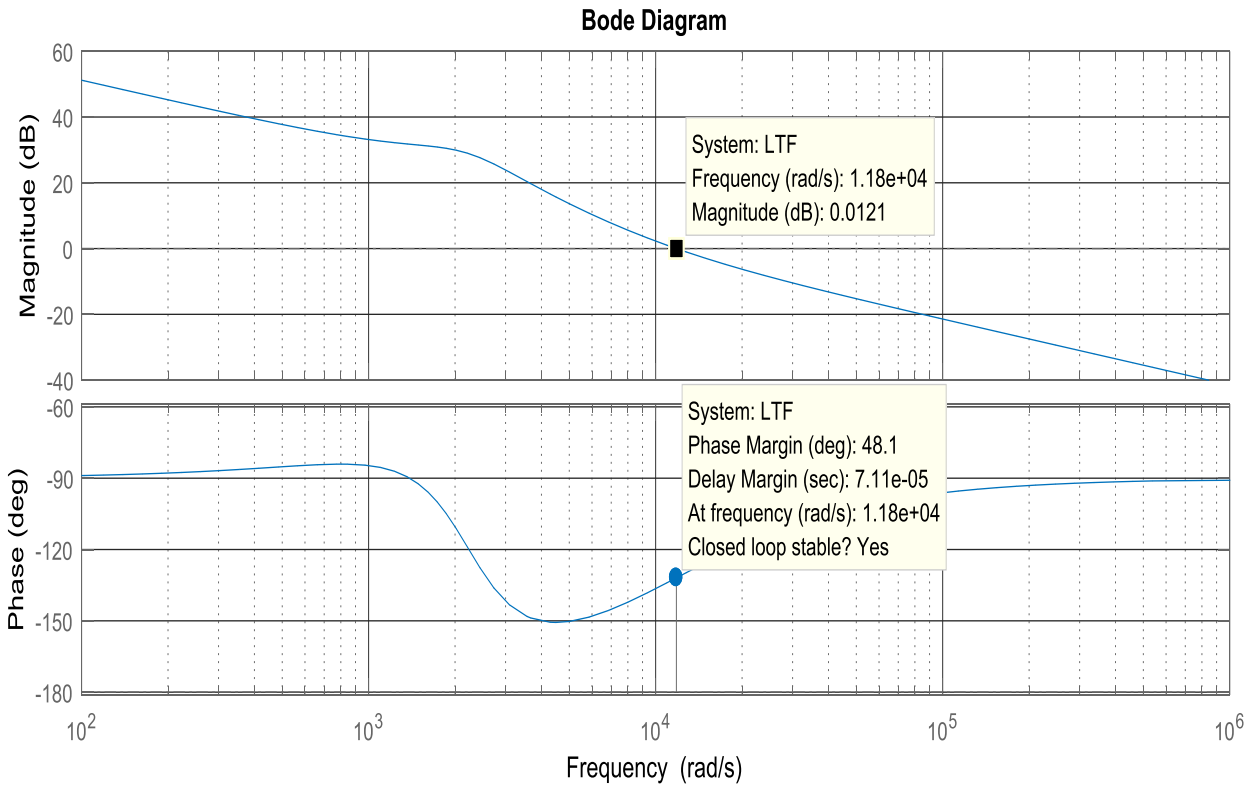


Figure 2.6 Bode plot of the loop transfer function.

2.4 Transition from Class-C (Boost) to Buck mode

A PI type controller is used for regulating the inductor current regardless of the mode of operation. The 4 switches are controlled depending on the mode of operation, i.e. Class-C (Boost) or Buck. In Class-C (Boost) mode, the Pulse Width Modulation (PWM) output goes to S4 with S3 complimentary while S1 is always ON and S2 is always OFF. Following a fault, the DC bus voltage will decrease, what requires the 4-switch converter to operate in Buck mode. The same output of the PWM used for S4 in the Class-C Boost mode is then used for S1 in Buck mode, while S3 is always ON and S2 and S4 are always OFF. A Mux is used to swap gating signals during transitions from one mode of operation to the other, as shown in Figure 2.7. In Class-C mode the top input of Mux will be its output, whereas in Buck mode the bottom input will be the output of the Mux.

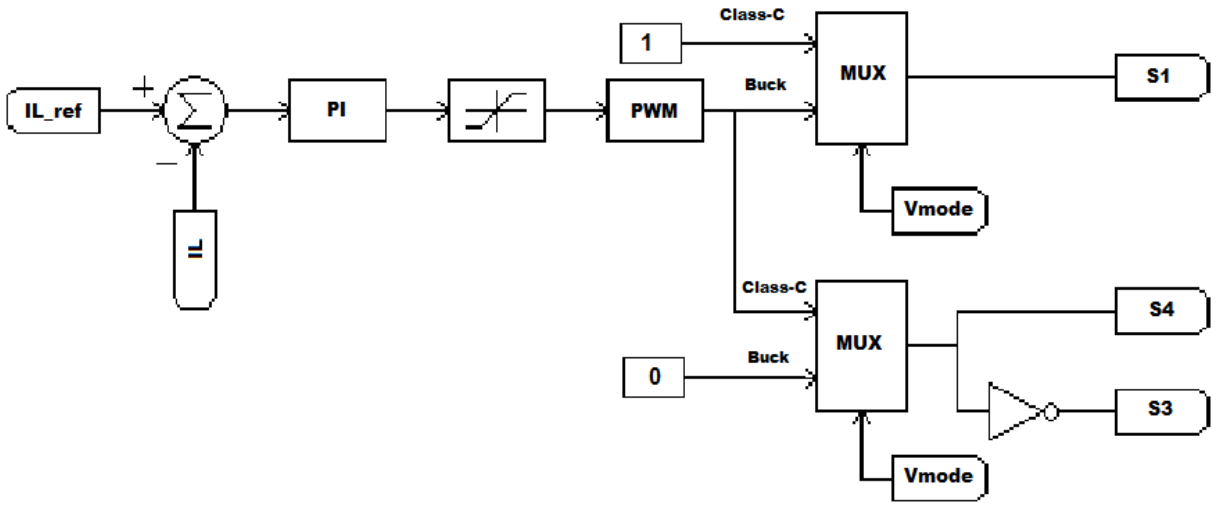


Figure 2.7 Transition from Class-C (Boost) to Buck mode.

The truth-table of all the switches depending on the modes of operation, i.e. Class-C (Boost) and Buck mode is presented in the Table 2.1**.**

Table 2.1 Truth-Table of 4-switches for both modes of operation.

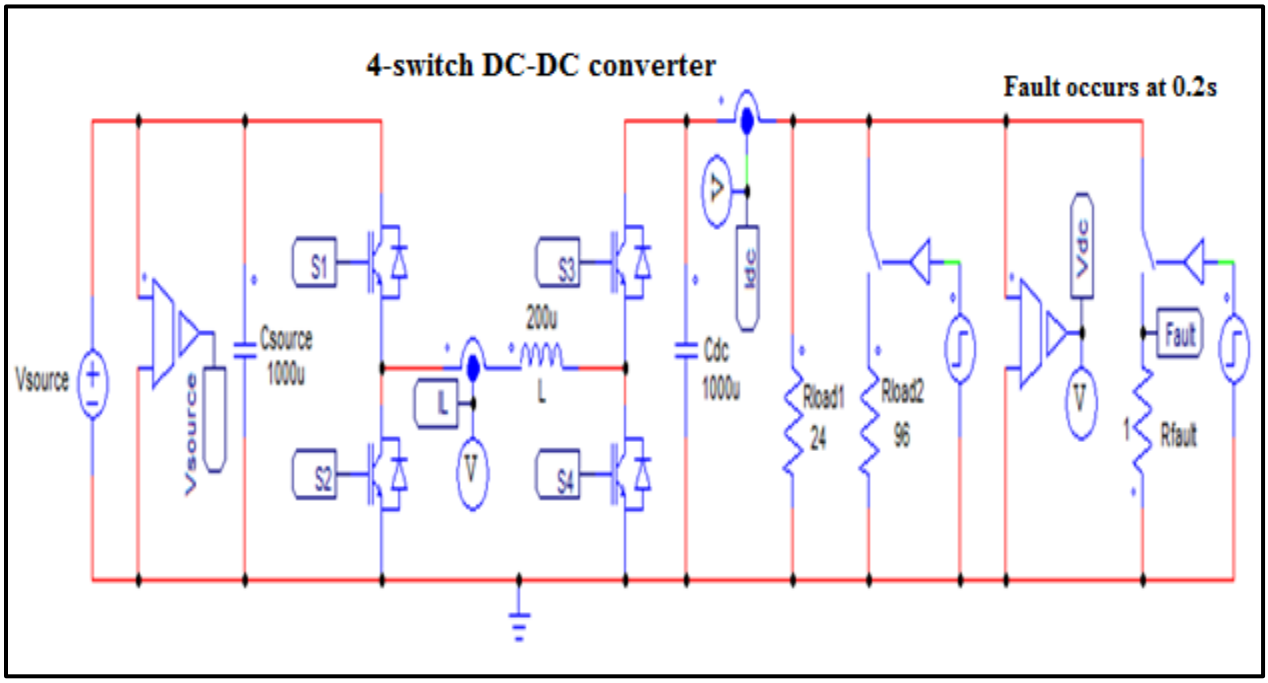
Mode	State/Switches	Switch 1	Switch 2	Switch 3	Switch 4
Class-C (Boost)	D_{ON}	ON	OFF	OFF	ON
	D_{OFF}	ON	OFF	ON	OFF
Buck	D_{ON}	ON	OFF	ON	OFF
	D_{OFF}	OFF	OFF	ON	OFF

2.5 Simulation

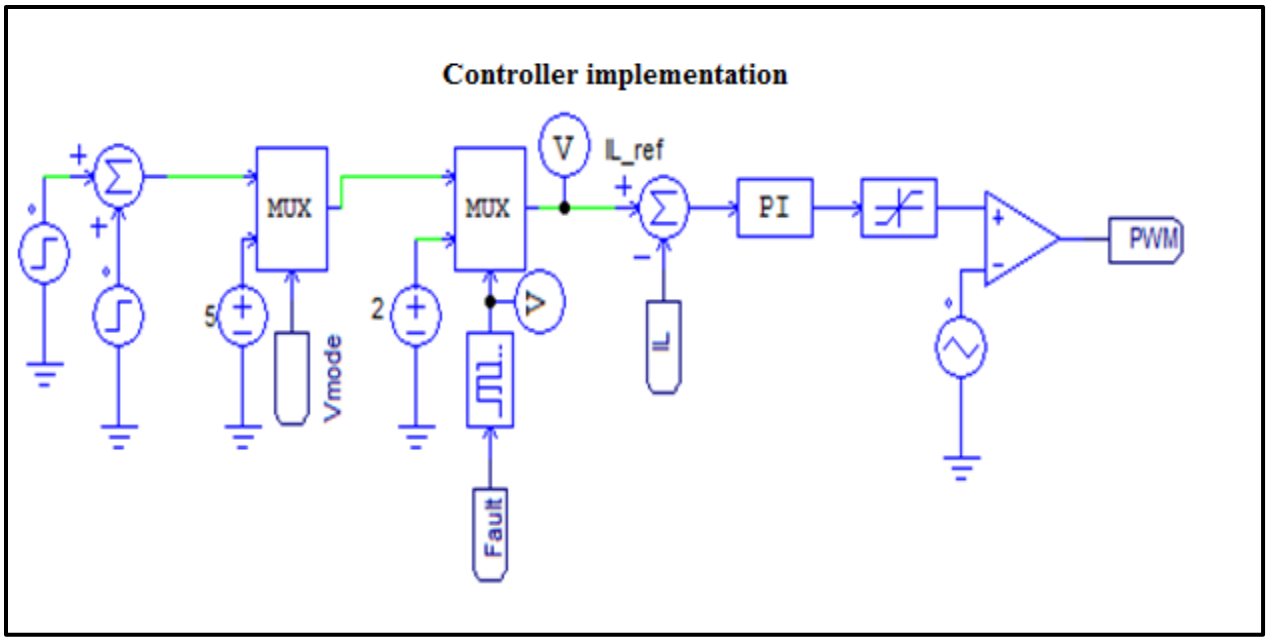
The schematic of the converter as well as the implementation of both modes of operation, Class-C (Boost) and Buck mode are presented here. The performance of the controller in both modes and the transition of mode from Class-C to Buck is also visualized by means of simulation using PSIM.

2.6 Simulation schematic

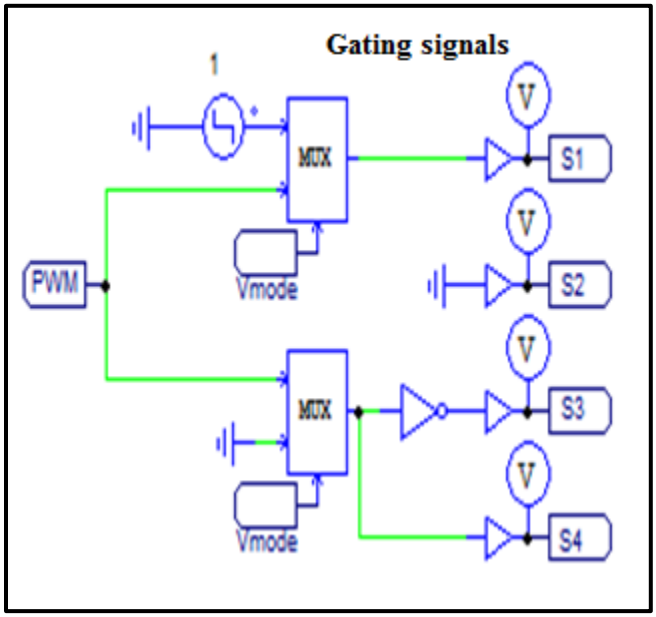
As mentioned before, a 4-switch bi-directional DC-DC converter is used in this work, the same as implemented in the PSIM simulation, can be seen in the Figure 2.8.a). Note that this setup is used to visualize the performance of controller in both modes of operation. The implementation of the PI controller used to control the inductor current is shown in Figure 2.8.b). Following the connection of a low impedance at a load bus, the current supplied by the DERs will increase but will be limited to the maximum current (5A) for 100ms, then the reference current is set to a lower current limit (2A) by using 2 by 1 Muxs. The selection between the modes is also done by a 2 by 1 Mux as shown in Figure 2.8.c). In the beginning, the system will operate in Class-C (Boost) mode. At t = 0.2s, fault is created by connecting a 1Ω fault resistance (R_{fault}) at 0.2s to the original load. Following a fault, the output voltage will decrease and the converter will start operating in Buck mode. The operating parameters of the converter, switching scheme, step load change values and the inductor current reference values will be demonstrated in the Section of Simulation results.



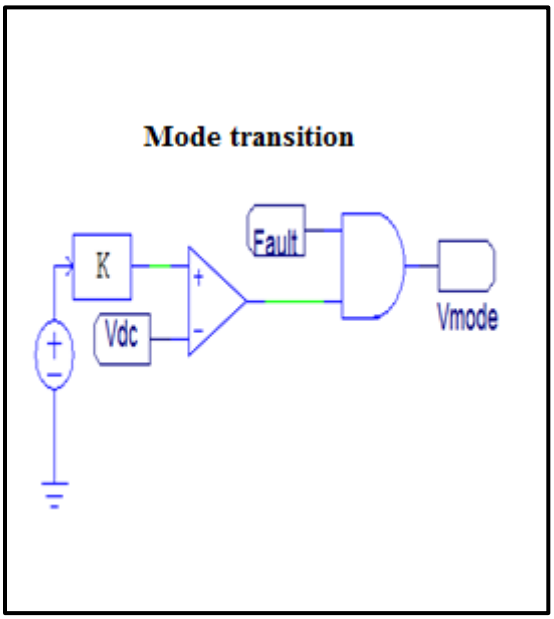
(a)



(b)



(c)



(d)

Figure 2.8 Power electronics interface: a) 4-switch DC-DC converter. b) Controller implementation. c) Implementation of gating signals for Class-C Boost and Buck mode. d) Mode transition.

2.7 Simulation results

The simulation results for both Class-C (Boost) and Buck modes are presented. The operating parameters are V_{source} = 24V, V_{dc} = 48, L = 200uH, C_{source} = C_{dc} = 1000uH. Figure 2.9 shows the performance of the converter in both modes. The waveforms of the output voltage (Graph A), inductor current and reference inductor current (Graph B), Gating signals of switch1 (Graph C) and the gating signals of switch 4 (Graph D) has been shown. In the beginning, the converter is operating in Class-C (Boost) mode with S1 ON while S3 and S4 PWMing to regulate the inductor current (I_L). The inductor current reference is set to 4A and a 24Ω load resistance (R_{load1}) is connected. At t = 0.1s, the inductor current reference is set to 5A and another load resistance (R_{load2}) of 96Ω is connected in parallel with the load, so the total load resistance (R_{load}) is equal to 24||96 = 19.2Ω. At 0.2s, a fault resistance (R_{fault}) of 1Ω is connected to the original load, (19.2Ω). The output voltage decreases and the converter starts operating in Buck mode with S1 PWMing to regulate the current $I_L = I_{dc}$, while S3 is ON and S4 is OFF. A 5A maximum current is injected for 100ms and the output voltage decreases to 4.8V. Then at t = 0.3s, the injected current $I_L = I_{dc}$ is limited at a low value (I_{dc_lcl}), 2A and the output voltage reduces further to 1.9V. To visualize the transition of converter from Classical Class-C (Boost) to Buck mode, the PWM signals of the two main switches (S1 and S4) are also shown in Graph C and Graph D. During normal operation (Boost mode), switch4 (S4) is operating with PWM while the switch1 (S1) is ON. When fault occurs, the output voltage decreases and the converter starts operating in Buck mode. Then S1 starts operating with PWM to control the inductor / injected current and S4 is OFF.

From the results, it can be observed that the 4-switch DC-DC converter is able to control the current when the output voltage is higher than the source voltage in Class-C mode under normal conditions. When faults occurs, the converter is not able to operate in Class-C, since the output voltage becomes smaller than the source voltage but it is able to control the current in Buck mode. It is also observed that the controller provides good performance in both modes of operation and the currents are regulated at their respected values.

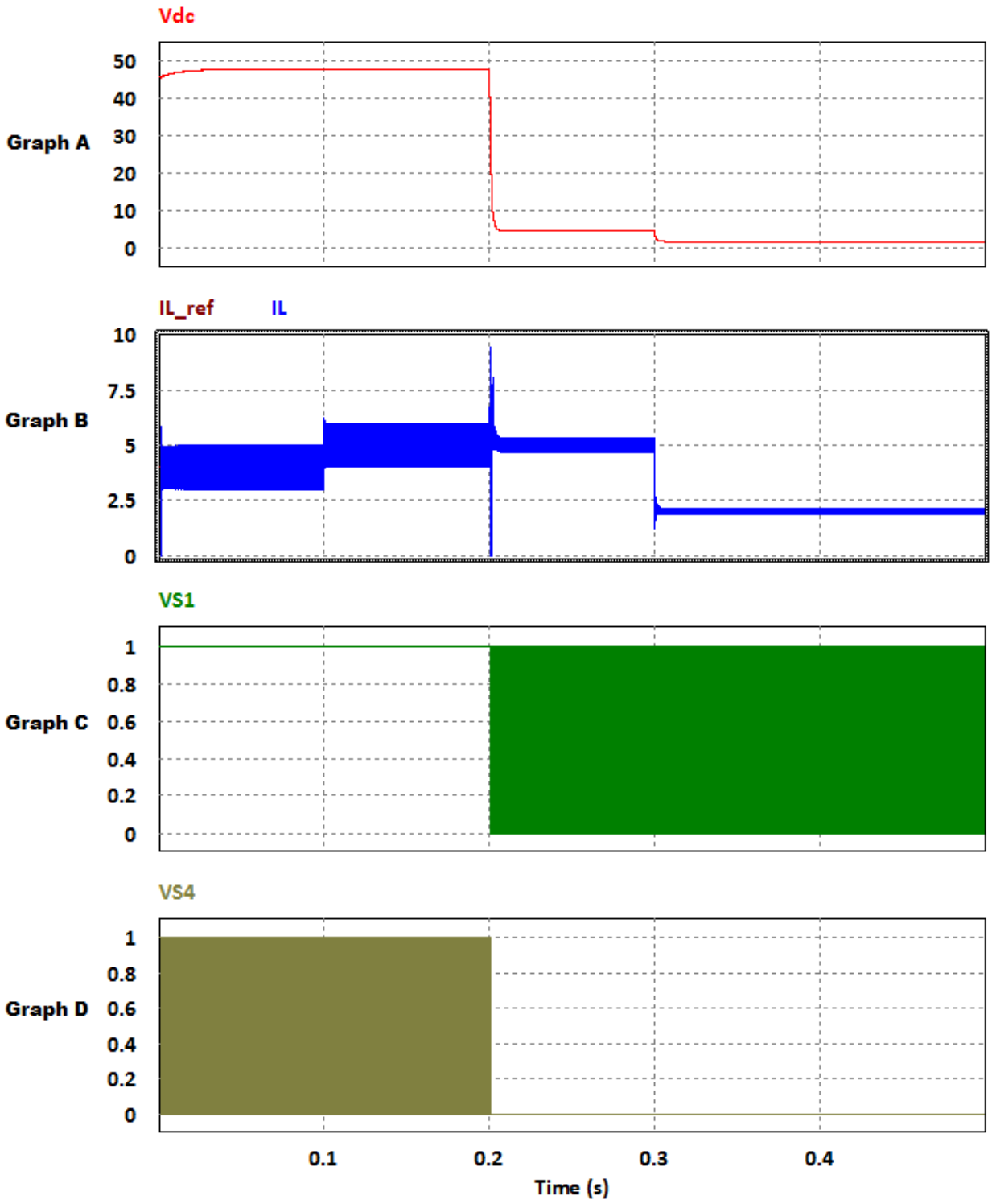


Figure 2.9 Simulation results. Graph A: Output voltage (Vdc). Graph B: Inductor current (IL) and reference inductor current (IL_ref). Graph C: Gating signals of switch1 (VS1). Graph D: Gating signals of switch4 (VS4).

2.8 Summary

A 4-switch fault-insensitive DC-DC converter is demonstrated in this Chapter. Unlike conventional Class-C and Boost converters, this 4-switch converter is used to control the current in both modes, Class-C (Boost) and Buck. The current-controlled converter is capable of switching automatically from the Class-C mode (normal operation) to the Buck mode (faulted system). A PI controller is used for regulating the inductor current regardless of the mode of operation with appropriate current control scheme. The controller provides good performance in both modes, and the expected results are obtained as shown by simulation results. The current limiting capability of the power electronics converter allows the use of low current protection devices (contactors), as will be discussed in Chapter 3. The converter is also implemented and the experimental implementation and results are presented in Chapter 4.

Chapter 3 Fault Protection Scheme

In this Chapter, a fault protection scheme is proposed to detect, locate and isolate the faulted segments of the DC bus without de-energizing the whole system. For identifying the faulted segment of a DC bus, CAN communication is used. The current limiting feature of the power interface along with a coordinated action eliminates the need for expensive and larger circuit breakers and allows the use of simpler and less expensive contactors, which can then open with low current and less risk.

3.1 System layout

Figure 3.1 shows DERs connected to the DC bus through interface nodes and supplying load groups (A, B and C). The power electronic interface of the DERs is the current controlled 4-switch converter, discussed in Chapter 2, and that operates as a conventional Class-C converter under normal conditions and as a Buck converter, during fault conditions. The current control loop and associated circuitry is realized with a digital controller. The interface nodes present two current sensors and two contactors, one of each to the right and the other to the left of the point of connection of the DERs. The current sensors are installed to continuously monitor the magnitude and the direction of currents in both branches connected to a DER. The contactors are used to connect / disconnect the segments of the DC nanogrid. It is assumed that the direction of current is positive, if current is entering the dot of the current sensor, and negative, if it is leaving the dot. During fault conditions, the DC bus voltage tends to collapse to a very low value due to small fault impedances despite large fault currents. The operation of the fault protection scheme, the logic for fault detection and the fault location method are discussed in the next Sections.

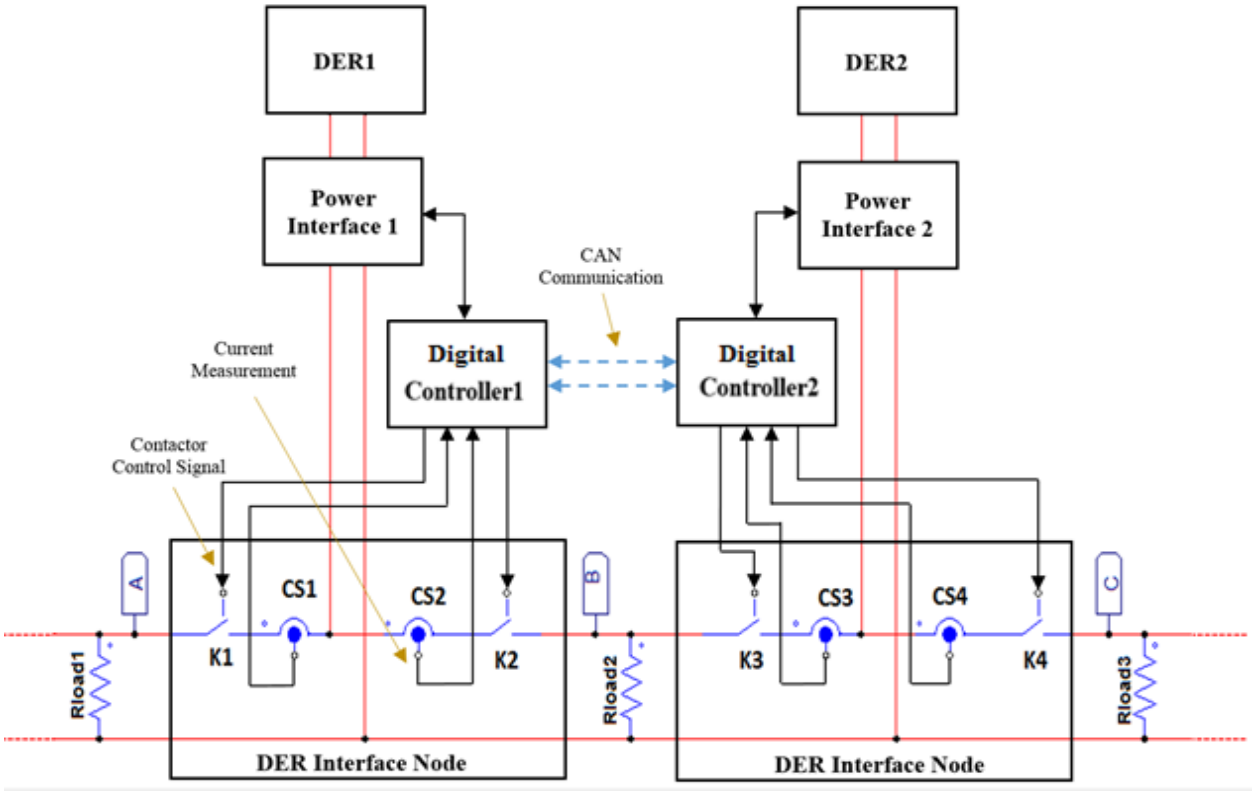


Figure 3.1 System with power electronic interfaces, interfacing nodes and load groups.

3.2 Operation of the protection method

When a fault occurs, the power interfaces reference currents and the potential activation signals for the contactors follow a sequence of operation as mentioned below:

1) Current limiting at maximum value: Following the connection of a low impedance at a load bus, the current supplied by the DERs will increase but will be limited to the maximum current as per the VI curve of the DERs. The DC bus voltage should decrease and the 4-switch converter should change from the Class-C to the Buck mode of operation.
2) Fault current reduction: If the current provided by the power interfaces remain at the maximum value for a given period of time, say 30 ms, and the voltage at the DC bus is "low" ($<0.5V_{fl}$), then it is assumed that a fault has occurred and the reference current is set to a lower current limit to allow the contactor(s) to open with a low current and less risk.
3) Faulty segment identification and isolation: Upon the realization that a fault has occurred, digital controllers will exchange information by means of a peer-to-peer communication scheme implemented via CAN, regarding the direction of the fault currents in their respective

interface nodes. This will allow digital controllers to determine which, if any, contactors should open to clear the fault. The logic for determining this action is discussed in a following Section.

4) Post fault operation: After opening the contactors of the faulted segment, the current references for the power interfaces will be determined by the VI curve of the DER, and the system will return to normal operation.

3.3 Fault detection logic

As the current drawn from a DER at a certain moment reaches the maximum current level, as defined by its VI curve, the voltage at its terminals will decrease as a function of the load impedance. As can be seen in Figure 3.2, for a small but "normal" load impedance, the decrease in the voltage level is relatively small and the system should remain in operation as is. However, if the load impedance is really small, such as of a fault impedance, then the voltage decreases significantly, what indicates that a fault has occurred.

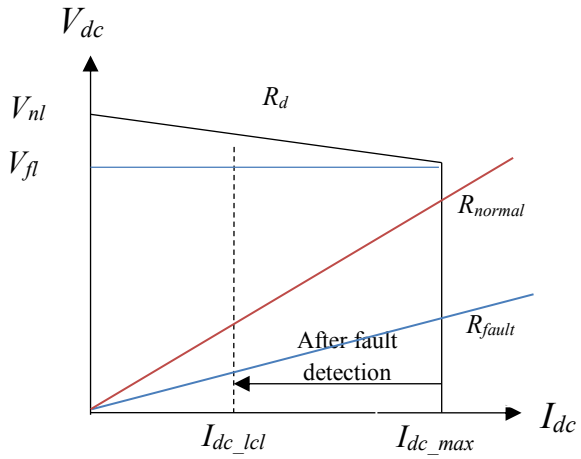


Figure 3.2 VI curve with a small normal load impedance (orange curve) and a small fault impedance (blue curve).

For the case study considered in this work, a "critical" current $I_{CSX} > 4.5$A passing through a current sensor along with a DC bus voltage level $V_{DCX} < 22.8$V, that is half of the typical full-load voltage of the DER (V_{fl}), for 30 ms, indicates the occurrence of a fault. It should be noted that the value of I_{CSX} was selected to be about 90% of the maximum current of the VI curve of the DER since it can provide power/current to loads placed to the right and to the left sides of the interface node.

3.4 Fault location and isolation

The directions of the DC nanogrid currents are measured at multiple locations as shown in Figure 3.1. It is assumed that the direction of current is indicated by means of a bit flag (B_{CSX}). If the potential fault current (I_{CSX}) in a given current sensor enters the dot and is positive i.e. B_{CSX} = 1. Conversely, if the current leaves the dot and is negative, B_{CSX} = 0.

3.4.1 With CAN communication between neighboring interfacing nodes

The interface nodes sense the magnitude and direction of the currents, at both of its branches, and send this info to the digital controller of the DER. Considering the system shown in Figure 3.1, by definition, the sensor and contactor to the left branch have an odd number and those to the right branch have an even number. By peer-to-peer communication in case of fault detection, a DER, say DER2, sends to its neighbor to the left, (DER1) the status/direction of its current in its left branch, i.e. B_{CS3} = 1 if the current flows from left to right and B_{CS3} = 0 if the current flows from right to left. From the neighbor to the left, it receives the information regarding the neighbor's current in his right side, that is, of current sensor 2 (CS2). If there is a fault in the branch between these two DERs, B_{CS2} = 1 and B_{CS3} = 0, what should lead to the opening of K2 and K3. If the data communicated between the two DERs are identical, say B_{CS2} = B_{CS3} = 1, then the fault is not in their common branch and those contactors should remain ON. Recall that digital controller1 does not share with digital controller2 the information regarding B_{CS1}, which does not share with digital controller1 the information regarding B_{CS4}. The fault might be in the immediate branch to the right side of DER2, what should be detectable by comparing the status of "his" B_{CS4} to the right-side neighbor's B_{CS5}, not shown in Figure 3.1. If they are identical, there are no faults in any branches connected to DER2. The logic discussed above considers when the digital controller of an interface node should open the contactor of its "right side", K2 of interface node 1 and when it should open the contactor of its "left side", which is K3 by digital controller2 of interface node 2. This logic is valid for all "intermediate" interface nodes of a DC nanogrid. As per the contactor at the left side of an interface node without a neighbor in its left side, say K1 of interface node 1, if B_{CS1} = 0, then digital controller1 should open K1. Likewise, for a contactor at the right side of an interface node without a neighbor in its right side, say K4 of interface node 2, if B_{CS4} = 1, then digital controller2 should open K4.

The following Sections discuss which contactors should open for given fault conditions, based on the flags of the four current sensors of the two interface nodes and the information exchanged with peer-to-peer communication.

When a fault occurs at bus 'A':

During a fault at bus 'A' as shown in Figure 3.1 , CS2 and CS3 will notice the fault current with negative current direction ($B_{CS2} = 0$, $B_{CS3} = 0$). CS4 will not notice the fault current in this case. CS1 will notice the fault current with negative current direction ($B_{CS1} = 0$). Since there is no neighbor for CS1 on the left, the logic proposed is that digital controller1 assumes that the bit flag it receives from its fictitious neighbor is $B_{CS0} = 1$. Thus, the fault at bus 'A' will be identified and the contactor K1 should open, however the contactors K2, K3 and K4 should remain ON as shown in Table 3.1.

Table 3.1 Direction of current sensors and contactors open signal during fault at bus 'A'.

DERs	Power interface 1		Power interface 2	
Current Sensors (CS)	CS1	CS2	C3	CS4
Current directions (B_{CS})	0	0	0	1
Contactors	K1	K2	K3	K4
Contactors open signal	✓	-	-	-

When a fault occurs at bus 'B':

During a fault at bus 'B' as shown in Figure 3.1, CS1 and CS4 will not notice a fault current. CS2 will notice the fault in the positive direction ($B_{CS2} = 1$) and CS3 will notice the fault in the negative current direction ($B_{CS3} = 0$). So, the fault at bus 'B' will be identified and the contactor K2 and K3 should open, while contactors K1 and K4 should remain ON as shown in Table 3.2.

Table 3.2 Direction of current sensors and contactors open signal during fault at bus ‘B’.

DERs	Power interface 1		Power interface 2	
Current Sensors	CS1	CS2	C3	CS4
Current directions	0	1	0	0
Contactors	K1	K2	K3	K4
Contactors open signal	-	✓	✓	-

When a fault occurs at bus ‘C’:

During a fault at bus ‘C’ as shown in Figure 3.1 , CS2 and CS3 will notice the fault current with positive current directions ($B_{CS2} = 0$, $B_{CS3} = 0$). CS1 will not notice the fault current in this case. CS4 will notice the fault current with positive current direction ($B_{CS4} = 1$). Since there is no neighbor for CS4 on the right, the logic proposed is that digital controller2 assumes that the bit flag it receives from its fictitious neighbor to the right is $B_{CS5} = 0$. Thus, the fault at bus ‘C’ will be identified and contactor K4 should open, while contactors K1, K2 and K3 should remain ON as shown in Table 3.3.

Table 3.3 Direction of current sensors and contactors open signal during fault at bus ‘C’.

DERs	Power interface 1		Power interface 2	
Current Sensors	CS1	CS2	CS3	CS4
Current directions	0	1	1	1
Contactors	K1	K2	K3	K4
Contactors open signal	-	-	-	✓

3.4.2 Without communication/communication failure between neighboring interfacing units

In case of no communication or communication failure, accurate fault location on the DC nanogrid cannot be determined. However some protection actions are performed based on the

direction of current and the possibility of the fault location to clear the fault. From Figure 3.1, contactor K1 should open, if the left most current sensor CS1 senses a fault current with negative direction ($B_{CS1} = 0$). Contactor K2 should open, if CS2 senses a fault current with positive direction ($B_{CS2} = 1$), which could be due to a fault in either bus 'B' or bus 'C'. In such a case, at least load group A can be supplied safely. Contactor K3 should open, if CS3 senses a fault current with negative direction ($B_{CS3} = 0$), which could be due to a fault in either bus 'A' or bus 'B'. Also, contactor K4 should open, if CS4 senses a fault current with positive direction ($B_{CS4} = 1$).

When a fault occurs at bus 'A':

During a fault at bus 'A' as shown in Figure 3.1, CS1, CS2 and CS3 will notice the fault current with negative direction ($B_{CS1} = 0$, $B_{CS2} = 0$, $B_{CS3} = 0$). CS4 will not notice the fault current in this case. Considering the logic for the case of failure of communication between interface nodes 1 and 2, contactors K1 and K3 should open, while contactors K2 and K4 should remain ON as shown in Table 3.4. It is important to notice that in this case with no communication, the fault at bus 'A' will be cleared and load groups B and C will not be dropped. Power interface 1 will supply bus 'B' and power interface 2 will supply bus 'C' in this case. A limitation in this case is that if power interface 1 does not have enough capacity to meet load demand B while there is surplus of power in power interface 2, the system will operate under non-ideal conditions, with a lower voltage level at bus 'B' then it could be if contactor K3 was still on.

Table 3.4 Direction of current sensors and contactors open signal during fault at 'A'.

DERs	Power interface 1		Power interface 2	
Current Sensors	CS1	CS2	C3	CS4
Current directions	0	0	0	1
Contactors	K1	K2	K3	K4
Contactors open signal	✓	-	✓	-

When a fault occurs at bus ‘B’:

During a fault at bus ‘B’ as shown in Figure 3.1, CS2 will notice the fault current with positive direction ($B_{CS2} = 1$) and CS3 will notice the fault current with negative direction ($B_{CS3} = 0$). CS1 and CS4 will not notice a fault current in this case. Considering the logic for the case of failure of communication between interface nodes 1 and 2, contactors K2 and K3 should open, while contactors K1 and K4 should remain ON as shown in Table 3.5. It is important to notice that even if there is no communication, the fault at bus ‘B’ will be cleared and load groups A and C will not be dropped. Power interface 1 will supply bus ‘A’ and power interface 2 will supply bus ‘C’ in this case.

Table 3.5 Direction of current sensors and contactors open signal during fault at ‘B’.

DERs	Power interface 1		Power interface 2	
Current Sensors	CS1	CS2	C3	CS4
Current directions	0	1	0	0
Contactors	K1	K2	K3	K4
Contactors open signal	-	✓	✓	-

When a fault occurs at bus ‘C’:

During a fault at bus ‘C’ as shown in Figure 3.1, CS2, CS3 and CS4 will notice a fault current with positive direction ($B_{CS2} = 1$, $B_{CS3} = 1$, $B_{CS4} = 1$). CS1 will not notice the fault current in this case. Considering the logic for the case of failure of communication between interface nodes 1 and 2, contactors K1 and K3 should remain ON as shown in Table 3.6. It is important to notice that even if there is no communication, the fault at bus ‘C’ will be cleared and load groups A and B will not be dropped. Power interface 1 will supply bus ‘A’ and power interface 2 will supply bus ‘B’ in this case.

Table 3.6 Direction of current sensors and contactors open signal during fault at ‘C’.

DERs	Power interface 1		Power interface 2	
Current Sensors	CS1	CS2	CS3	CS4
Current directions	0	1	1	1
Contactors	K1	K2	K3	K4
Contactors open signal	-	✓	-	✓

3.5 Implementation of the peer-to-peer communication between interface nodes

In this Section, the description of the interface node with current sensors and contactors and their link to the digital controller is presented. Furthermore, the implementation of peer-to-peer communication between digital controllers with CAN using transceiver is also explained in this Section.

3.5.1 Interface node

The DERs of the DC nanogrid are connected to the DC bus by means of an interface node as shown in Figure 3.1. The interface node consists essentially of two sets of a current sensor in series with the contactor, one to left and one to the right of the DERs.

The LA 55-P (LEM) Hall-effect current sensors are used for implementing the interface nodes. These sensors are capable of sensing both the magnitude and direction of currents in their respective branches, and this information is sent to the digital controller of the DER. Figure 3.3 shows the basic diagram of the current sensor configuration and its link to the digital controller. The same power supply which is used to supply the power interfaces sensors is used to supply the sensors of the interface node. To apply measured current to ADC channel of the digital controller, the gain and offset circuit is employed that makes the signal level within digital controller input range, 0~3V.

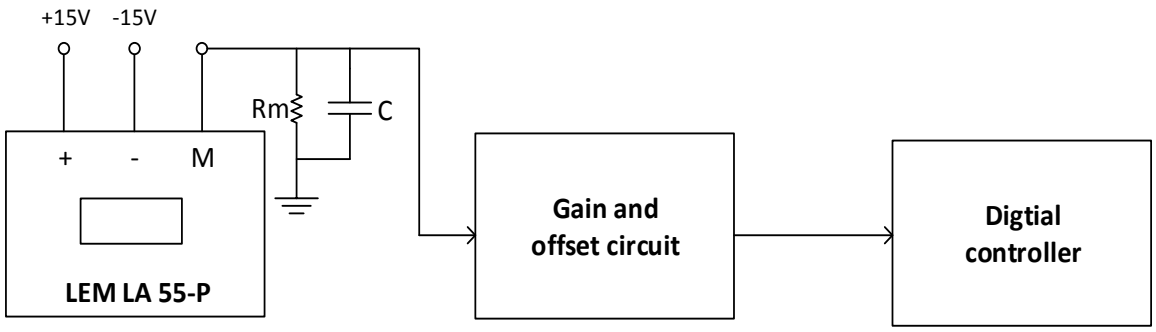


Figure 3.3 Configuration of current sensor measurement and its link to the digital controller.

Figure 3.4 shows the current sensor measurement with its external circuitry. LA 55-P sensors are utilized for current measurements up to ±25A and converting it into -3~3V by using measurement resistance R_m. A simple gain and offset circuit using op-amp and voltage divider circuit is then used to convert the resulting signal into a 0~3V signal to be used by the ADC of the digital controller.

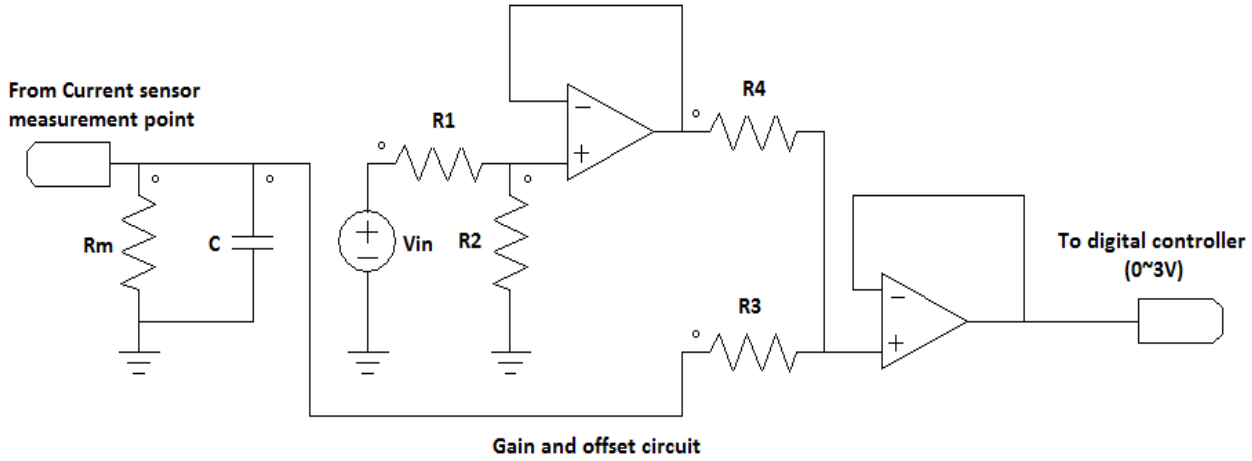


Figure 3.4 Current sensor measurement with gain and offset circuit.

The parameters used for the above circuit are presented in Table 3.7.

Table 3.7 Parameters for current sensor measurement with gain and offset circuit.

R_m (Ω)	C (uF)	V_{in} (V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)
120	0.1	15	10k	2.5k	10k	10k

The EV200 (TE Connectivity) DC contactors are employed for implementing the interface nodes. These contactors are used to connect / disconnect the segments of the DC nanogrid. Figure

3.5 shows the basic diagram of contactor configuration and its link to the digital controller. In case of a fault in the DC nanogrid, the digital controller of the power electronics interface might decide to open one or none of its interface node contactors, based on the direction of the current in its current sensors as well as on the current sensors of neighboring units, in the same branches. The contactor drive circuit controls the contactor according to the digital controllers control signal. A power supply is used to power the contactor coil.

Figure 3.5 Configuration of contactor and its link to the digital controller.

Figure 3.6 shows the circuit used to drive a high current rating contactor from a 3.3V low current digital signal. The contactor needs typically 9~36V/2A supply to energize its coil. A gate drive opto-coupler "HCPL-3120" is used which can provide up to 2.5A/15~30V output. In order to meet the opto-coupler input current requirement (25mA), a transistor (Q1) "2N2222A" is used which can provide up to 800mA continuous collector current.

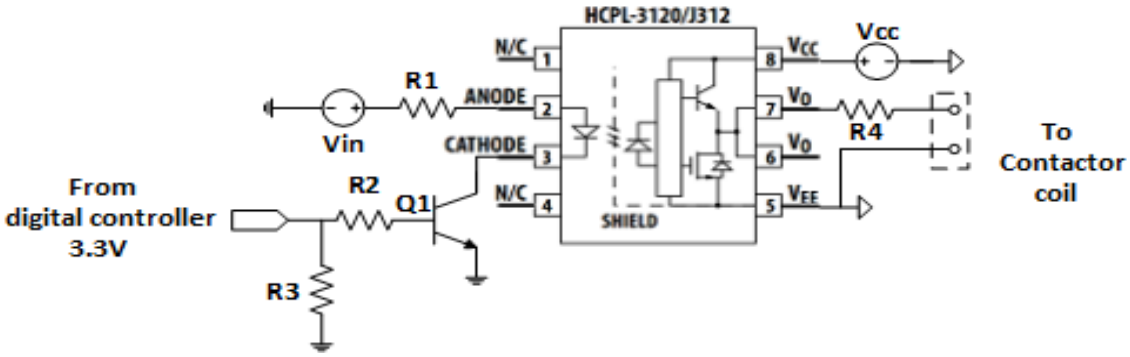


Figure 3.6 Contactor drive circuit.

The parameters used for the above circuit are presented in Table 3.8.

Table 3.8 Parameters for contactor drive circuit.

V_{in} (V)	V_{cc} (V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)
15	15	1.2k	2.7k	10k	1.2

3.5.2 Implementation of CAN communication between digital controllers

As mentioned in *Section 3.4*, the digital controllers of neighboring DERs communicate with each other on a peer-to-peer fashion, the information regarding the currents in the common branches to determine the fault location and to identify the appropriate contactors that should be open. In this work, this is implemented with Controller Area Network (CAN) communication.

CAN data format

Figure 3.7 [25] shows the standard data format defined for CAN communication. The data is send across the CAN network on packets called frames. A typical CAN frame consists of:

- Start bit: Start of frame
- Arbitration field: It contains the identifier and the type of message being sent. The identifier establishes the priority of the message. The lower the binary value, the higher its priority.
- Control bits: Control field indicating the number of bytes being transmitted.
- Data field: Up to 8 bytes of data may be transmitted
- CRC bits: Cyclic redundancy check (CRC)
- Acknowledge: Each node acknowledges (ACK) its data integrity
- End: End-of-frame bits

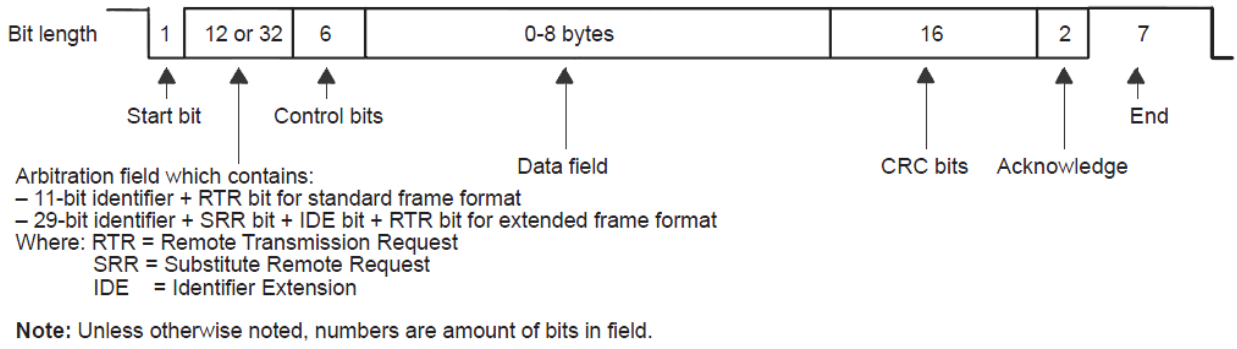


Figure 3.7 CAN data format [25].

Figure 3.8 shows the typical data frame that would be sent in this particular work. An 11-bit identifier standard frame format arbitration field is selected. In this simple case, control bit is equal to 1, since only one byte is used for transmitting the data. The data field contains the actual data being transmitted. Only two bits are used, where “bit0” is used for fault bit signal and “bit1” is used for the direction of current.

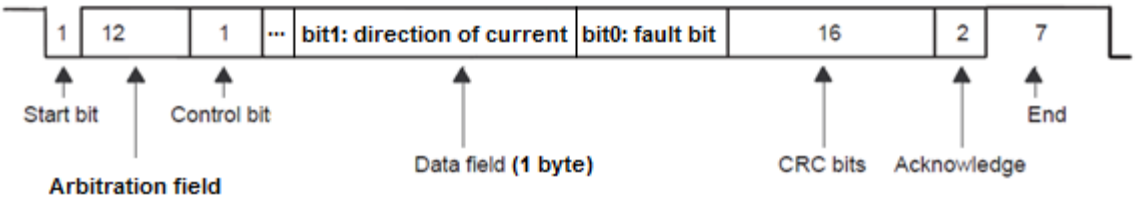


Figure 3.8 Typical CAN data transmitted in this work.

CAN implementation

The digital controller TMS320F28335 implemented in this work is integrated with CAN controller. The connection to the physical medium is then implemented with Texas Instruments SN65HVD230 3.3V CAN transceivers. The transceivers are powered with their respective digital controllers. Figure 3.9 shows the configuration of the CAN implementation with transceivers. CAN communication enables the digital controllers to talk by linking the nodes connected to a bus. The use of a CAN transceiver allows the CAN controller to adapt the CAN bus levels to levels compatibles with the CAN controller to access the CANH and CANL lines of the network. The CAN controller output 'CANTX' is connected to the transceivers driver input pin 'D' and the input of the CAN controller 'CANRX' is connected to the transceivers receiver output pin 'R'. As specified by the ISO11898 standard, termination resistance 'R_{TERM}' of 120Ω is connected at both ends of the cable to prevent signal reflections [28].

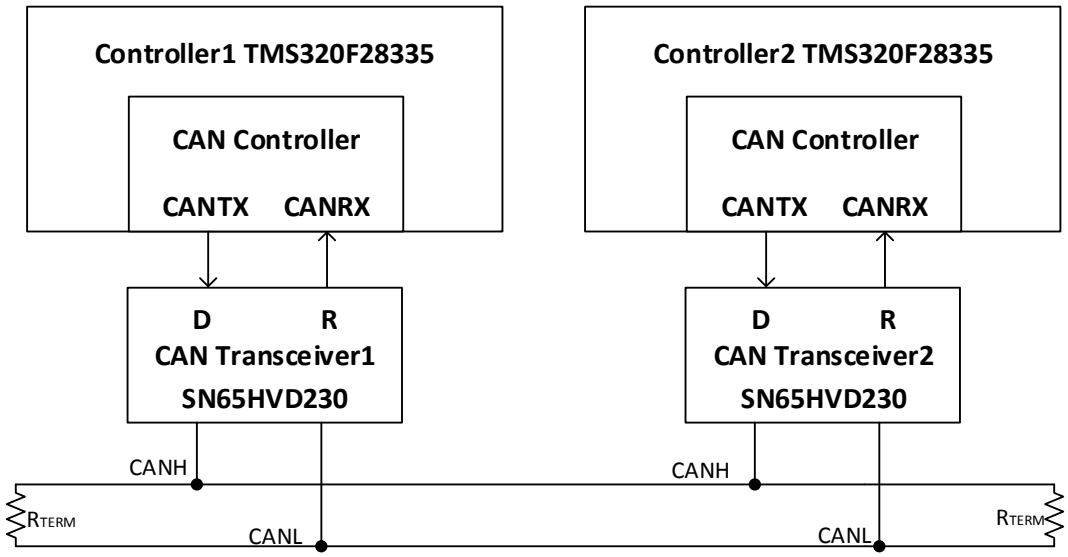


Figure 3.9 CAN implementation using transceivers.

3.6 Summary

A fault protection scheme for DC nanogrid based on the coordination of fault-insensitive converters and contactors for the DC nanogrid has been presented in this Chapter. The scheme based on peer-to-peer communication to identify the faulted segment(s) of the DC nanogrid and which contactors should open. The communication is implemented with Controller Area Neatwork (CAN). Finally, a backup protection strategy was also presented for the case of communication failure, so that the fault can still be cleared. The effectiveness of the proposed scheme is demonstrated with experimental results in the next Chapter.

Chapter 4 Experimental Implementation

The primary goal in this work is to implement the proposed fault protection scheme for a DC nanogrid with distributed energy resources (DERs). The experimental setup for obtaining the results is described in this Chapter. Then, theoretical calculations are performed for the experimental tests with different cases. Finally, the experimental results are presented and discussed for all the cases.

4.1 Experimental setup

The experimental prototype of the bi-directional 4-switch DC-DC converter is implemented in this work, which is a new realization of an existing Class-C (2-switches) Texas Instruments (TI) converter "LM5170EVM-BIDIR Evaluation Module*"* that was designed for a similar application. The specifications of the converter are already mentioned in Chapter 2. The 4-switch DC-DC converter is able to control the injected current as the conventional Class-C, under droop control and current limit under normal DC bus voltage condition, and also when the grid is faulted, what is the focus of this work. It consists of four MOSFETS with the respective gate driver circuits. Also, voltage and current sensors are installed for sensing the input and output voltages as well as the inductor current. A digital controller is equipped with the converter that is capable of measuring the sensed values. The layout of the printed circuit board (PCB) was designed using "EASYEDA" software. The PCB was ordered and then populated in the lab.

A single unit of the 4-switch DC-DC converter was built. For tests with multiple distributed energy resources, a standard laboratory power supply operating as a regulated lab voltage source with a limited current is employed. By inserting a properly selected output resistor in series with the power supply, one can emulate a uni-directional DER operating with droop control and current limit. The voltage drop across the output resistance realizes the droop control function of the emulated converter. As the DC bus voltage decreases, the voltage across the output resistance increases, increasing the current injected by the power supply into the DC bus. This occurs, until the current limit value of the power supply is reached.

In order to implement the proposed fault protection scheme in a DC nanogrid, the DERs are connected to the distribution system by means of special interface nodes. As shown in Figure 4.1, both the converter and power supply interface nodes contain two contactors and two current

sensors. The output voltage sensor of the converter is used to sense the voltage at the converter interface node, however an additional voltage sensor is installed at the power supply interface node to sense its node voltage. The digital controller used in the converter for basic current control function is also used to realize the functions of the converter interface node. However, since the power supply is not equipped with such a controller, an external digital controller is installed to realize the functions of power supply interface node. These interfaces also present a peer-to-peer communication scheme, implemented in this work with Controller Area Network (CAN).

The digital controller used in the power electronics interface and interface node is the TMS320F28335 from Texas Instruments. The codes for both the digital controllers are generated in Code Composer Studio using PSIM. The results are presented here in the form of waveforms taken from a Tektronix Oscilloscope available in the PEER laboratory, Concordia University.

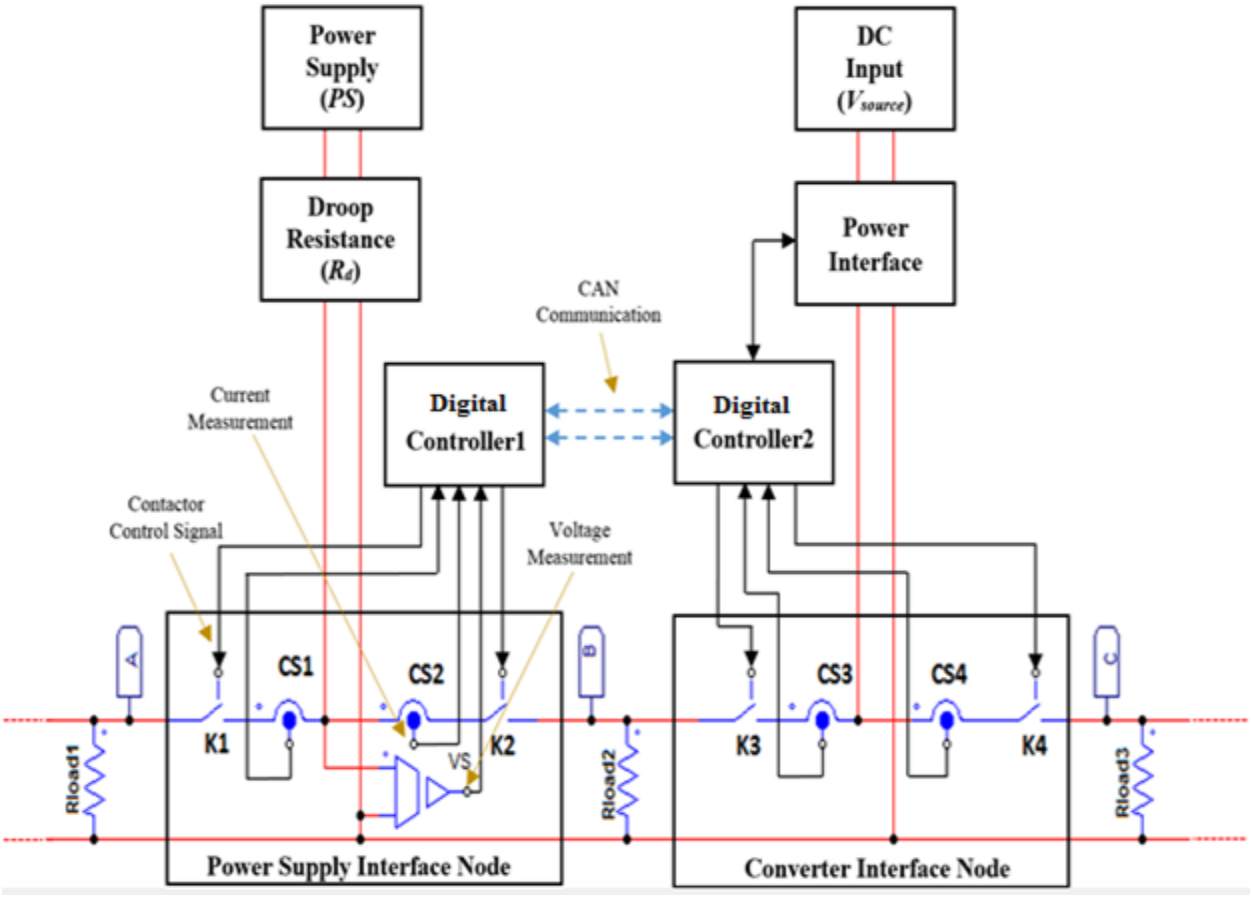


Figure 4.1 Complete system layout.

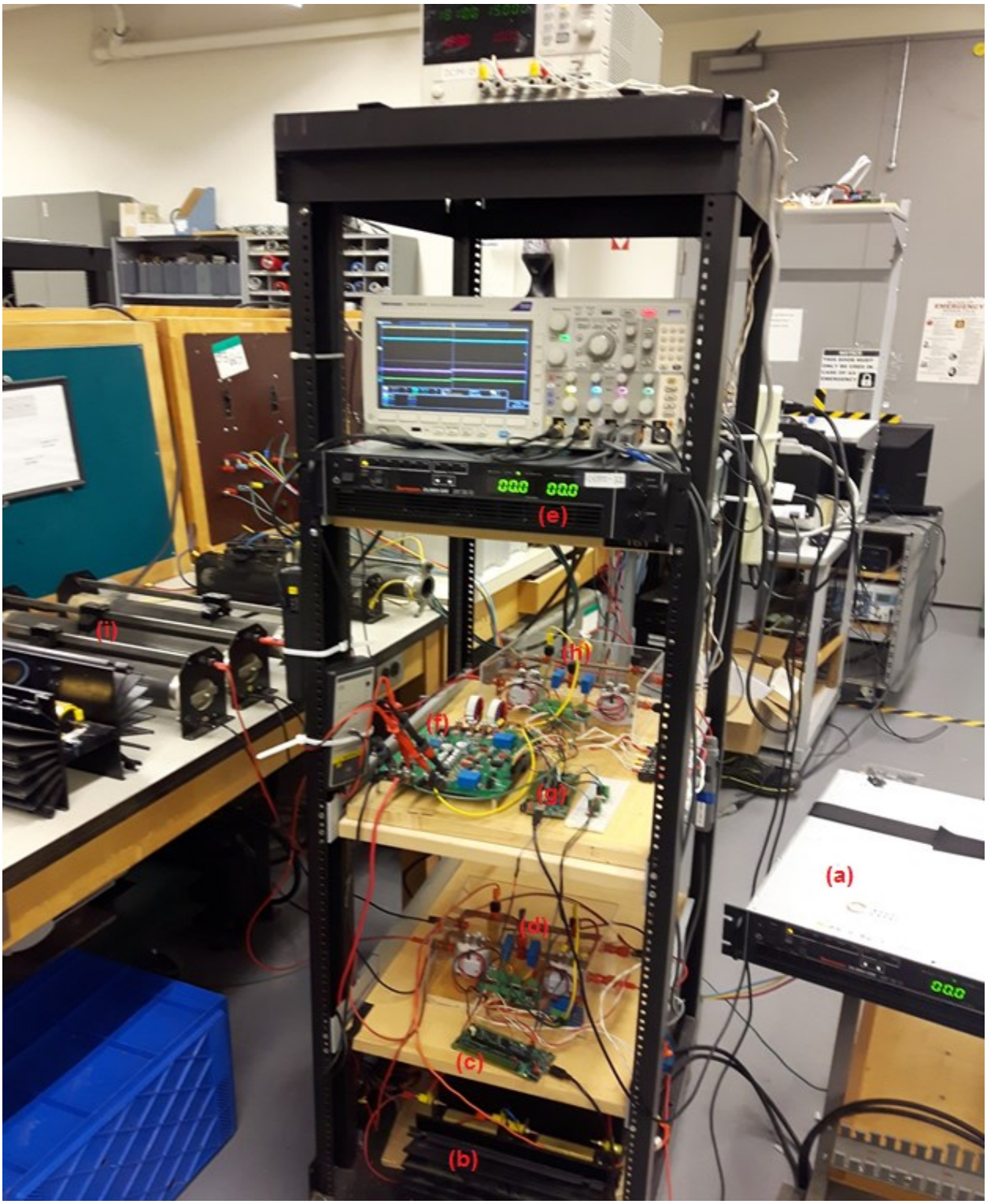


Figure 4.2 Snapshot of the actual experimental setup. (a) Power supply. (b) Droop resistance. (c) Digital Controller1. (d) Power supply interface node. (e) DC input. (f) Power converter. (g) Digital Controller2. (h) Converter interface node. (i) Loads.

4.2 Experimental tests theoretical calculations

In this Section, first the performance of the DERs are studied without interface nodes and communication, in different cases. These tests are performed to explore the behavior of DERs in different modes of operation. This includes tests with a single DER in droop, current limit (normal condition) and current limit with low load impedance (fault condition). Finally the complete system is implemented as shown in Figure 4.1, to verify the proposed fault location method, so as to open only the faulted segment. The operation of the DERs (converter and power supply) is essentially the same for "normal conditions". In droop mode, the DER will follow the VI curve as shown in Figure 4.3, and during the current limit, the DERs will operate in maximum current limit. However, following a low load impedance condition, the converter and power supply will operate in maximum current limit during fault detection and once the fault is detected, the converter will switch to a low current limit(I_{dc_lcl}). But since the power supply is not fully controllable, a low current limit reference for the power supply could not be set and it will operate in maximum current limit. This is set by the current limit of the laboratory power supply, even after the fault detection. For illustration purposes, the contactor near the power supply would open at the same (high) current in this experiment. This is not desirable and does not match the specifications defined by the proposed fault protection scheme to be employed with power converters, but it will not damage the contactor.

4.2.1 Tests with a single DER without interface nodes

In this Section, the experimental tests with a single DER (converter and power supply) in droop mode, current limit and low load impedance (fault) condition are performed individually to understand the operation of each element independently in different cases. The basic specifications of the VI curve for the DER interfaces are as follows:

Key system specifications:

1. No-load voltage (V_{nl}) = 48V
2. Full-load voltage (V_{fl}) = 45.5V
3. Droop resistance (R_d) = 0.5Ω
4. Maximum current limit (I_{dc_max}) = 5A
5. Converter lower current limit at fault condition (I_{dc_lcl}) = 2A

6. Converter input voltage (V_{source}) = 24V
7. Power supply voltage (V_{ps}) = 48V
8. Switching frequency (f_{sw}) = 30kHz

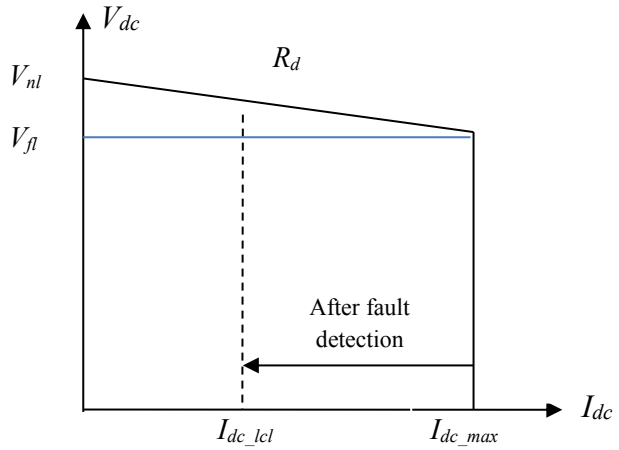


Figure 4.3 VI curve.

Although the VI curve of the DER is defined for the DC bus voltage and the injected current, the current that is actually controlled is the average current of the inductor. The reference value of the injected current is generated from the VI curve and then converted to the reference current of the inductor (I_L) by using the power balance equation as:

$$I_L V_{source} \eta = I_{dc} V_{dc} , \tag{4.1}$$

Assuming that the system is loss-less, i.e. efficiency (η) is 100%. So the equation (4.2) can be re-written as:

$$I_L = \frac{I_{dc} V_{dc}}{V_{source}} , \tag{4.2}$$

a) Droop mode

To visualize the operation of droop control with a single DER, a step change in the load resistance is applied. At the beginning, a load resistance (R_{load}) of 40Ω is connected. Then another load resistance of 40Ω is connected in parallel with 40Ω (i.e. 40||40=20Ω).

The current injected by the DER interface in the droop mode is given by:

$$I_{dc} = \frac{V_{nl} - V_{dc}}{R_d}, \quad (4.3)$$

Where I_{dc} and V_{dc} are the injected current and DC bus voltage respectively. V_{nl} is the no-load voltage of the droop control scheme and is set by the operator. The following relation is also valid:

$$V_{nl} = V_{dc} + V_d, \quad (4.4)$$

Where V_d is the droop voltage. For a single DER and single load (R_{load}) system, it can be computed as a function of the droop resistance as:

$$V_d = \frac{V_{nl}R_d}{R_d + R_{load}}, \quad (4.5)$$

The resulting DC bus voltage can be computed as

$$V_{dc} = \frac{V_{nl}R_{load}}{R_{load} + R_d}, \quad (4.6)$$

Based on the values previously presented, the theoretical values obtained for this tests case are presented in Table 4.1

Table 4.1 Theoretical values with single DER operating under droop control.

Theoretical values			
R_{load} (Ω)	V_{dc} (V)	I_{dc} (A)	V_d V)
40	47.41	1.19	0.59
20	46.83	2.34	1.17

b) Current limit (normal) condition

The converter and power supply operating under current limit (normal) condition is demonstrated by applying a step load change, which is achieved by connecting a 7Ω resistance to the original load, (20Ω). The DERs will operate in maximum current limit during this condition. So, the equivalent load resistance (R_{load}') and DC bus voltage (V_{dc}') after the step change and in the current limit mode are:

$$R_{load}' = R_{load} \,||\, R_{7\Omega}\,, \tag{4.7}$$

$$V_{dc}' = I_{dc\_max}\, R_{load}', \tag{4.8}$$

The theoretical values for this case are presented in Table 4.2.

Table 4.2 Theoretical values with a single DER operating under maximum current limit.

Theoretical values		
R_{load}' (Ω)	I_{dc} (A)	V_{dc}' (V)
5.19	5	25.92

c) Low load impedance (fault) condition

The converter and power supply operating under low load impedance (fault) condition is demonstrated, which is achieved by connecting a fault resistance (R_{fault}) of 2Ω to the original load, (20Ω). This test is performed with single DER and simple system without the interface nodes to first explore the operation of DERs in low load impedance condition. Thus, the fault would not be isolated in this case. The DERs will operate in maximum current limit during the fault detection i.e. 30ms, as mentioned in Chapter 3. Once the fault is detected the converter will switch to low current limit (I_{dc_lcl}). So, the equivalent load resistance (R_{load}'') and DC bus voltage during fault detection (V_{dc}'') in the low load impedance condition are:

$$R_{load}'' = R_{load} || \, R_{fault}, \tag{4.9}$$

$$V_{dc}'' = I_{dc\_max}\, R_{load}'', \tag{4.10}$$

The theoretical values for this case are presented in Table 4.3.

Table 4.3 Theoretical values with single DER during fault detection.

Theoretical values		
R_{load}'' (Ω)	During fault detection	
	I_{dc} (A)	V_{dc}'' (V)
1.82	5.0	9.1

4.2.2 Tests with both DERs, interface nodes and communication

In this Section, the complete system is implemented as shown in Figure 4.1, with both DERs, interface nodes and communication to verify the proposed fault protection scheme, so as to open only the faulted segment. The experimental tests with both DERs in current limit (normal) and low load impedance (fault) conditions are performed in this Section.

The equivalent circuit of the new configuration with both DERs operating in the droop mode is shown in Figure 4.4.

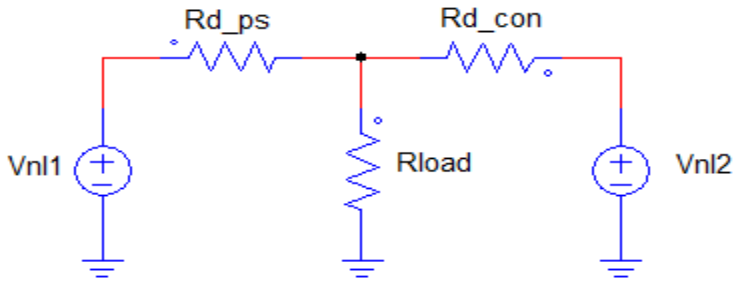


Figure 4.4 Eq. circuit with both DERs and load resistance.

Where,

V_{nl1} is the lab voltage source value, which corresponds to the no-load output voltage of this DER

V_{nl2} is the converter output voltage at no-load, set in its VI curve

R_{d_con} is the converter droop resistance factor

R_{d_ps} is the droop resistance connected in series with lab power supply

R_{load} is equivalent load resistance as given by:

$$R_{load} = R_{load1} \,||\, R_{load2} \,||\, R_{load3}\ , \tag{4.11}$$

Here $V_{nl1} = V_{nl2}$, which means the two sources start to regulate the DC bus from the same voltage,

By applying the Thevenin's theorem we get,

Since, $R_{d\_con} = R_{d\_ps} = R_d$,

Neglecting the cable resistance, the equivalent droop resistance (R_{d_eq}) is given by,

$$R_{d\_eq} = R_{d\_con} || R_{d\_ps} \tag{4.12}$$

$$R_{d\_eq} = \frac{R_d}{2} \tag{4.13}$$

The Thevenin's equivalent circuit of Figure 4.4 is shown in Figure 4.5

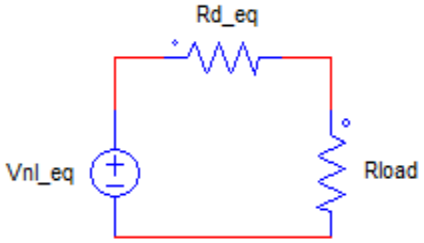


Figure 4.5 Thevenin's equivalent circuit of Figure 4.4.

Since two sources are now connected in parallel, the maximum grid current limit now is the sum of both sources.

$$I_{dc\_max} = I_{dc\_conmax} + I_{dc\_psmax} \tag{4.14}$$

Where,

I_{dc_max} is the maximum grid current,

I_{dc_conmax} is the converter's maximum output current

I_{dc_psmax} is the maximum/limit current of the lab power supply

Key system specifications:

1. Converter no-load voltage (V_{nl1}) = 48V
2. Power supply set voltage, identical to the no-load voltage (V_{nl2}) = 48V
3. Equivalent no-load grid voltage (V_{nl_eq}) = 48V
4. Full-load voltage (V_{fl}) = 45.5
5. Converter maximum current limit (I_{dc_conmax}) = 5A
6. Power supply maximum current limit (I_{dc_psmax}) = 5A
7. Maximum current limit (I_{dc_max}) = 10A
8. Converter droop resistance factor ($R_{d_{con}}$) = 0.5Ω

9. Power supply series droop resistance ($R_{d_{ps}}$) = 0.5Ω
10. Equivalent droop resistance (R_{d_eq}) = 0.25Ω
11. DC-DC converter input voltage (V_{source}) = 24V
12. Switching frequency (f_{sw}) = 30kHz
13. Individual load resistances ($R_{load1} = R_{load2} = R_{load3}$) = 60Ω
14. Equivalent load resistance (R_{load}) = 20Ω

The total current injected by both DERs interface in the droop mode is given by:

$$I_{dc} = \frac{V_{nl\_eq} - V_{dc}}{R_{d\_eq}}, \tag{4.15}$$

Where I_{dc} and V_{dc} are the total injected current and DC bus voltage respectively. V_{nl} is the no-load voltage of the droop control scheme and is set by the operator. The following relation is also valid:

$$V_{nl\_} = V_{dc} + V_{d\_eq}, \tag{4.16}$$

Where V_{d_eq} is the equivalent droop voltage. With multiple DERs and single load (R_{load}) system it can be computed as a function of the equivalent droop resistance as:

$$V_{d\_eq} = \frac{V_{nl\_eq} R_{d\_eq}}{R_{d\_eq} + R_{load}} \tag{4.17}$$

The resulting DC bus voltage can be computed as:

$$V_{dc} = \frac{V_{nl\_eq} R_{load}}{R_{load} + R_{d\_eq}} \tag{4.18}$$

a) Current limit (normal) condition

The performance of both DERs together under current limit (normal) condition is demonstrated, which is achieved by connecting a 3.5Ω resistance at point 'B' to ground in Figure 4.1. During the current limit (normal) condition, both the DERs will operate in maximum current limit. The equivalent load resistance (R_{load}') and DC bus voltage (V_{dc}') after connecting 3.5Ω resistance and in the current limit mode are:

$$R_{load}' = R_{load} \parallel R_{3.5\Omega}, \tag{4.19}$$

$$V_{dc}' = I_{dc\_max}\, R_{load}', \tag{4.20}$$

The current flowing through individual load resistances (I_{loadn}) is:

$$I_{loadn} = \frac{V_{dc}'}{R_{loadn}}, \tag{4.21}$$

Where n (= 1, 2, 3) is the number of load resistance.

The current passes through each current sensor in Figure 4.1, can be calculated in this case as:

$$I_{cs1} = -I_{load1} \tag{4.22}$$

$$I_{cs2} = 5 + I_{cs1} \tag{4.23}$$

$$I_{cs3} = -5 + I_{cs4} \tag{4.24}$$

$$I_{cs4} = I_{load3} \tag{4.25}$$

The theoretical values for this case are presented in Table 4.4.

Table 4.4 Theoretical values with both DERs in current limit (normal) condition.

Theoretical values					
R_{load}' (Ω)	I_{cs1} (A)	I_{cs2} (A)	I_{cs3} (A)	I_{cs4} (A)	V_{dc}' (V)
2.98	-0.5	4.5	-4.5	0.5	29.8

Although each DER is in maximum current limit mode i.e. 5A, but not all the current will flow to the connected 3.5Ω resistance at bus 'B', because there is some current also going to the real loads.

c) Low load impedance (fault) condition

The performance of both DERs operating under low load impedance condition is demonstrated, which is achieved by connecting a fault resistance (R_{fault}) of 1.1Ω at either bus A or B or C to ground in Figure 4.1. The DERs will operate in maximum current limit mode during the fault

detection. Once the fault is detected the converter will switch to low current limit (I_{dc_lcl}). The equivalent load resistance (R_{load}'') in low load impedance condition is:

$$R_{load}'' = R_{load} \parallel R_{fault}\ , \tag{4.26}$$

During fault detection:

During fault detection, The DC bus voltage (V_{dc}''), individual load resistances current (I_{loadn}) and the current flowing through the fault resistance (I_{fault}) are:

$$V_{dc}'' = I_{dc\_max}\, R_{load}'', \tag{4.27}$$

$$I_{loadn} = \frac{V_{dc}''}{R_{loadn}}\ , \tag{4.28}$$

Where n (= 1, 2, 3) is the number of load resistance.

$$I_{fault} = \frac{V_{dc}''}{R_{fault}}\ , \tag{4.29}$$

When fault is at bus A:

The fault at "bus A" is created by connecting a fault resistance of 1.1Ω at bus A to ground in Figure 4.1.

During fault detection:

$$I_{cs1} = -(I_{load1} + I_{fault}) \tag{4.30}$$

$$I_{cs2} = 5 + I_{cs1} \tag{4.31}$$

$$I_{cs3} = 5 - I_{cs4} \tag{4.32}$$

$$I_{cs4} = I_{load3} \tag{4.33}$$

The theoretical values for this case are presented in Table 4.5.

Table 4.5 Theoretical values during fault detection when fault is at bus A.

Theoretical values during fault detection					
R_{load}'' (Ω)	I_{cs1} (A)	I_{cs2} (A)	I_{cs3} (A)	I_{cs4} (A)	V_{dc}'' (V)
1.04	-9.6	-4.6	-4.8	0.2	10.4

Although each DER is in maximum current limit mode i.e. 5A, but not all the current is flowing to the connected fault resistance (R_{fault}) of 1.1Ω at bus 'A', because there is some current also going to the real loads.

When fault is at bus B:

The fault at "bus B" is created by connecting a fault resistance of 1.1Ω at bus B to ground in Figure 4.1.

$$I_{cs1} = -I_{load1} \tag{4.34}$$

$$I_{cs2} = 5 + I_{cs1} \tag{4.35}$$

$$I_{cs3} = -5 + I_{cs4} \tag{4.36}$$

$$I_{cs4} = I_{load3} \tag{4.37}$$

The theoretical values for this case are presented in Table 4.6.

Table 4.6 Theoretical values during fault detection when fault is at bus B.

Theoretical values during fault detection					
R_{load}'' (Ω)	I_{cs1} (A)	I_{cs2} (A)	I_{cs3} (A)	I_{cs4} (A)	V_{dc}'' (V)
1.04	-0.2	4.8	-4.8	0.2	10.4

Although each DER is in maximum current limit mode i.e. 5A, but not all the current is flowing to the connected fault resistance (R_{fault}) of 1.1Ω at bus 'B', because there is some current also going to the real loads.

When fault is at bus C:

The fault at "bus C" is created by connecting a fault resistance of 1.1Ω at bus C to ground in Figure 4.1.

$$I_{cs1} = -I_{load1} \tag{4.38}$$

$$I_{cs2} = 5 + I_{cs1} \tag{4.39}$$

$$I_{cs3} = -5 + I_{cs4} \tag{4.40}$$

$$I_{cs4} = I_{load3} + I_{fault} \tag{4.41}$$

The theoretical values for this case are presented in Table 4.7.

Table 4.7 Theoretical values during fault detection when fault is at bus C.

Theoretical values during fault detection					
R_{load}'' (Ω)	I_{cs1} (A)	I_{cs2} (A)	I_{cs3} (A)	I_{cs4} (A)	V_{dc}'' (V)
1.04	-0.2	4.8	4.6	9.6	10.4

Although each DER is in maximum current limit mode i.e. 5A, but not all the current is flowing to the connected fault resistance (R_{fault}) of 1.1Ω at bus 'C', because there is some current also going to the real loads.

4.3 Experimental results

4.3.1 Results with a single DER without interface nodes

a) Droop mode

Converter in droop mode

The operation of DC-DC converter in droop control is shown in Figure 4.6. In the beginning, a 40Ω load is connected, the DC bus voltage (V_{dc}), sky blue curve, is 47.4V and the injected current (I_{dc}), green curve is 1.2A. Then, a step load change is applied, changing the load impedance from

40Ω to 20Ω, the DC bus voltage decreases to 46.8V and the injected current increases to 2.4A, so the inductor current, pink curve, also increased according to equation (4.2).

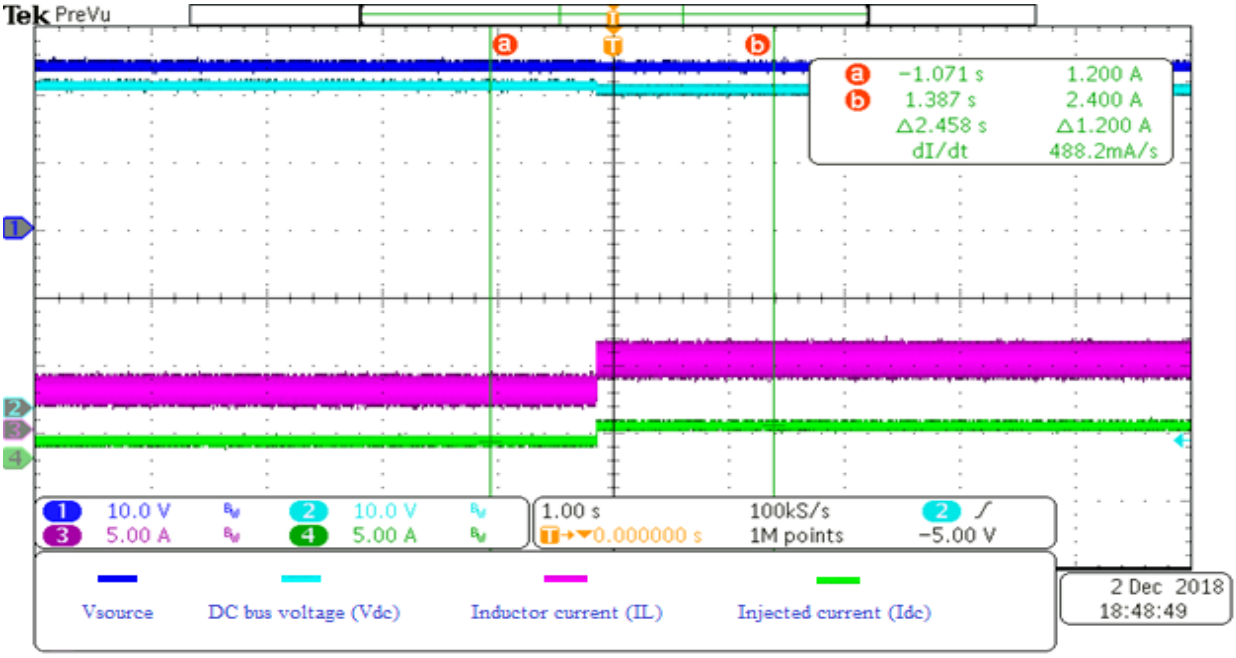


Figure 4.6 Converter in droop control.

Ch1 (*dark blue*): Vsource, Ch2 (*sky blue*): DC bus voltage (Vdc), Ch3 (*pink*): Inductor current (IL) Ch4 (*green*): injected current (Idc)

In *Section 4.2.1*(*a*), the operation of the DER under droop control is analyzed and also the theoretical values are presented, and the comparison of theoretical values and experimental values are presented in Table 4.8. It can be seen that the theoretical values match with those of the experimental.

Table 4.8 Comparison of theoretical values and experimental values for the operation of converter in droop control.

$R_{load}(\Omega)$	Type of result	I_{dc} (A)	V_{dc} (V)
40	Theoretical	1.20	47.41
	Experimental	1.20	47.40
20	Theoretical	2.34	46.83
	Experimental	2.40	46.82

Power supply in droop mode

The operation of power supply in droop control is shown in Figure 4.7. In the beginning a 40Ω load is connected and the DC bus voltage (V_{dc}), sky blue curve, is 47.4V and the injected current (I_{dc}), green curve, is 1.2A. Then, a step load change is applied from 40Ω to 20Ω, the DC bus voltage decreases to 46.8V and the injected current increases to 2.32A.

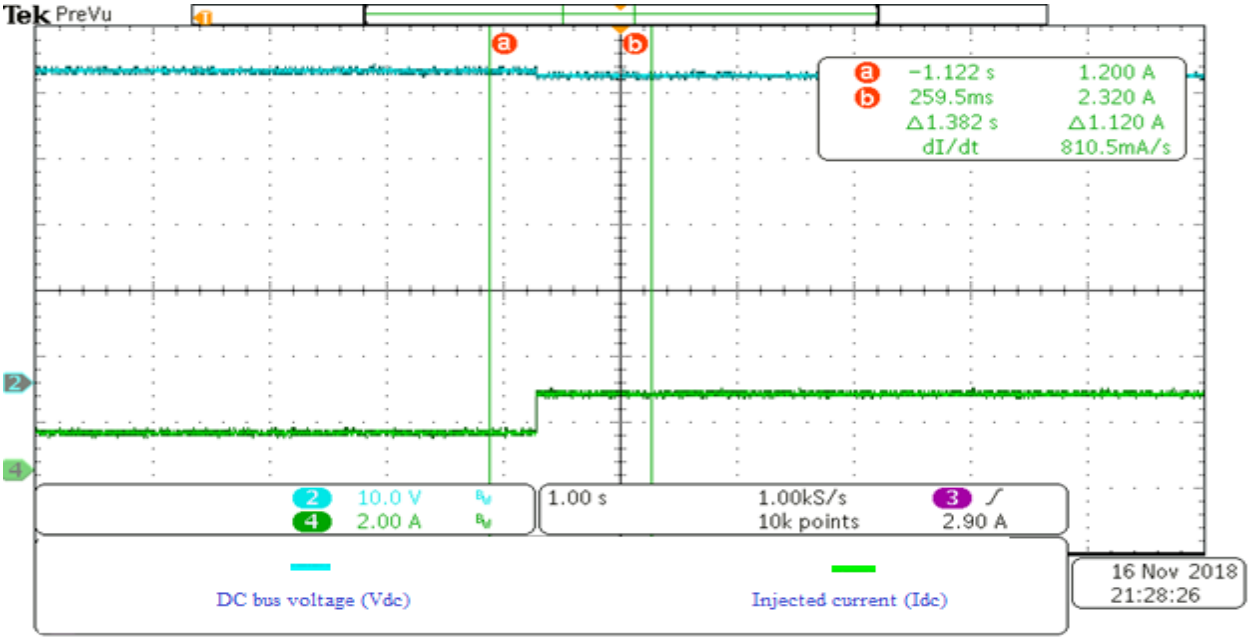


Figure 4.7 Power supply in droop control.

Ch2 (*sky blue*): DC bus voltage (Vdc), Ch4 (*green*): injected current (Idc)

In *Section 4.2.1(a),* the operation of DER under droop control is analyzed and also the theoretical values are presented, and the comparison of theoretical values and experimental values are presented in Table 4.9. It can be seen that the theoretical values match very well with those of the experimental.

Table 4.9 Comparison of theoretical and experimental values for the operation of power supply in droop control.

R_{load} (Ω)	Type of result	I_{dc} (A)	V_{dc} (V)
40	Theoretical	1.2	47.41
	Experimental	1.2	47.40
20	Theoretical	2.34	46.83
	Experimental	2.32	46.82

b) Current limit (normal) condition

Converter in current limit (normal) condition

The operation of DC-DC converter in current limit (normal) condition is shown in Figure 4.8. In the beginning, a 20Ω load is connected and the DC bus voltage (V_{dc}), sky blue curve, is 46.8V and the injected current (I_{dc}), green curve, is 2.4A. Then, a step load change is applied by connecting a 7Ω resistance to the original load, 20Ω, the DC bus voltage (V_{dc}) decreases to 26.4V and the injected current increases to maximum current limit i.e. 5A. The current that is controlled is the average current in the inductor, and from this current the injected current reference is generated, so the transient current observed is due to the energy stored in the converter's output capacitor, that the capacitor releases when the voltage decreases due to a higher load drawing more power. Although the current goes high in the transient, the steady state current is limited at the expected value.

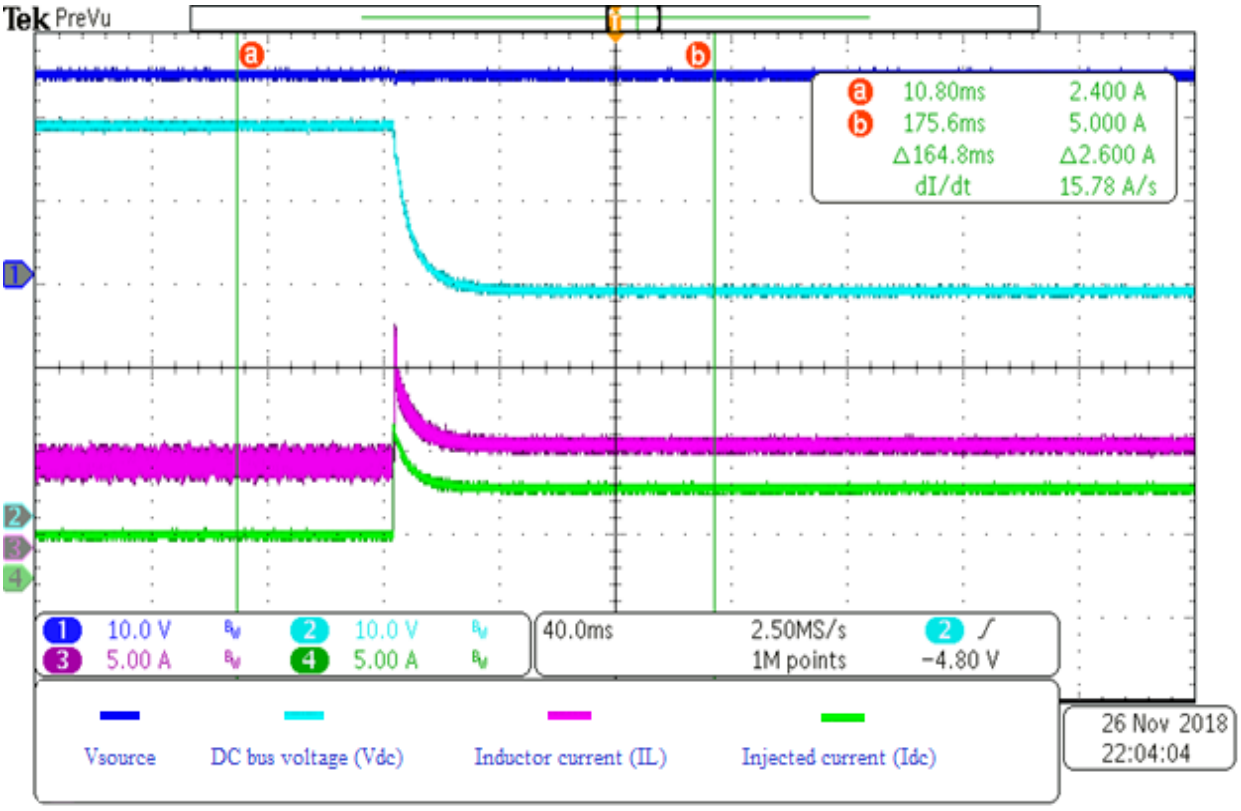


Figure 4.8 Converter in current limit (normal) condition.

Ch1 (*dark blue*): Vsource, Ch2 (*sky blue*): DC bus voltage (Vdc), Ch3 (*pink*): Inductor current (IL) Ch4 (*green*): injected current (Idc)

In *Section 4.2.1*(*b*), the operation of DER under maximum/normal current limit is analyzed and also the theoretical values are presented, and the comparison of the theoretical values and steady state experimental values are presented in Table 4.10. It can be seen that they match very well with each other.

Table 4.10 Comparison of theoretical values and experimental steady state values for the operation of converter in current limit (normal) condition.

R_{load}' (Ω)	Type of result	I_{dc_max} (A)	V_{dc}' (V)
5.2	Theoretical	5	26.00
	Experimental	5	26.20

Power supply in current limit (normal) condition

The operation of power supply in the maximum/normal current limit mode is shown in Figure 4.9. In the beginning, a 20Ω load is connected and DC bus voltage (V_{dc}), pink curve, is 46.8V and the injected current (I_{dc}), green curve, is 2.4A. Then, a step load change is applied by connecting a 7Ω resistance to the original load, 20Ω, the DC bus voltage (V_{dc}) decreases to 26.4V and I_{dc} increases to maximum current limit i.e. 5A. It is observed that the power supply is able to maintain its maximum current limit (5A), but it does not limit it directly. First it goes to a high transient current and then it limits the steady state current at the expected value. This is due to the intrinsic characteristics of the lab power supply used in this test.

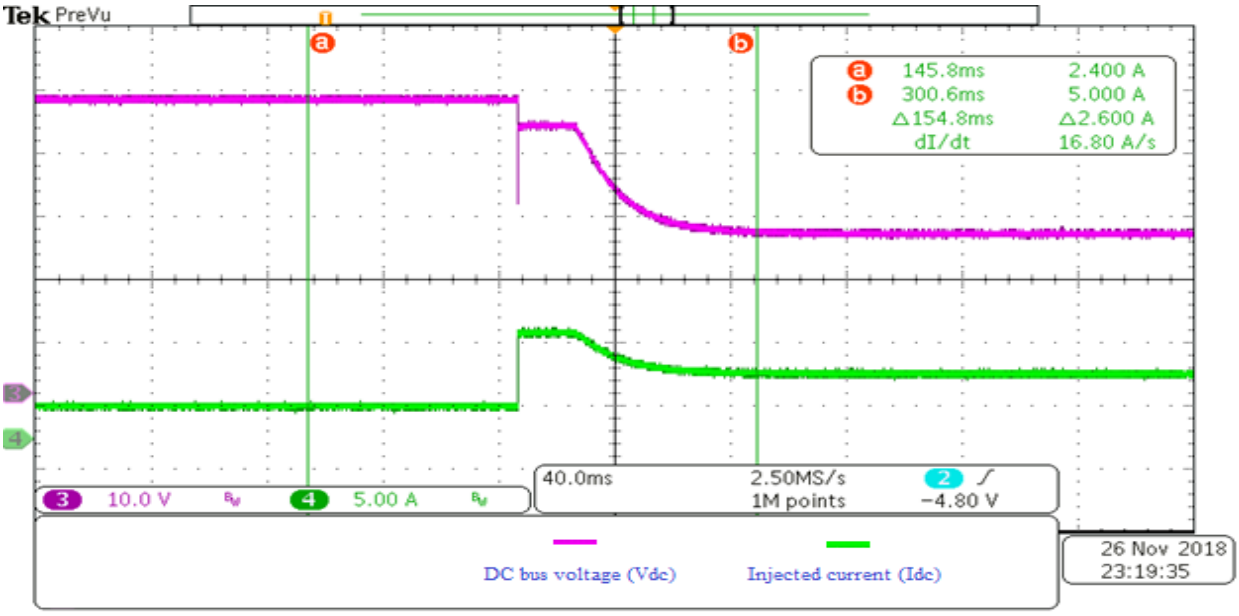


Figure 4.9 Power supply in current limit (normal) condition.

Ch3 (*pink*): DC bus voltage (Vdc), Ch4 (*green*): injected current (Idc)

In *Section 4.2.1*(*b*), the operation of DER under maximum current limit is analyzed and also the theoretical values are presented, and the comparison of the theoretical values and steady state experimental values are presented in Table 4.11. It can be seen that they match very well with each other.

Table 4.11 Comparison of theoretical values and experimental steady state values for the operation of power supply in current limit (normal) condition.

R_{load}' (Ω)	Type of result	I_{dc_max} (A)	V_{dc}' (V)
5.2	Theoretical	5	26.0
	Experimental	5	26.2

c) Low load impedance (fault) condition

Converter in low load impedance (fault) condition

The operation of the DC-DC converter in low load impedance condition is shown in Figure 4.10. Recall that these results are with a single DER and simple system without the interface nodes to first explore the operation of DERs in low load impedance condition so the fault would not be isolated in this case. In the beginning a 20Ω load is connected and DC bus voltage (V_{dc}), pink

curve, is 46.8V and injected current (I_{dc}), green curve, is 2.4A. Then a fault resistance (R_{fault}) of 2Ω is connected to the original load, (20Ω). During fault detection, when the grid current is set to maximum current i.e. 5A the DC bus voltage decreases to 9.2V, then after 30ms the fault is detected, and the injected current reference is decreased to 2A and DC bus voltage reduces further to 3.6V. Also, the operation of the two main switches are shown to visualize the transition of converter from classical Class-C to Buck mode, can be observed by the dark blue (V_{gs1}) and sky blue (V_{gs4}) waveforms. During normal operation (Boost mode), switch4 (S4) is operating with PWM while the switch1 (S1) is ON. When the DC bus voltage decreases to a lower value ($<0.5V_{fl}$) i.e. Buck mode, the S1 starts operating with PWM to control the current and S4 is OFF. The current loop is controlling the average current in the inductor, and from this current the injected current reference is generated. When a low load impedance is connected, a high current peak is observed in the transient, which is due to the energy stored in the converter's output capacitor that the capacitor releases when the voltage decreases due to a higher load drawing more power. Although the current goes high in the transient, the aim is to control the steady state current, which is limited at the expected values as shown in the Figure below.

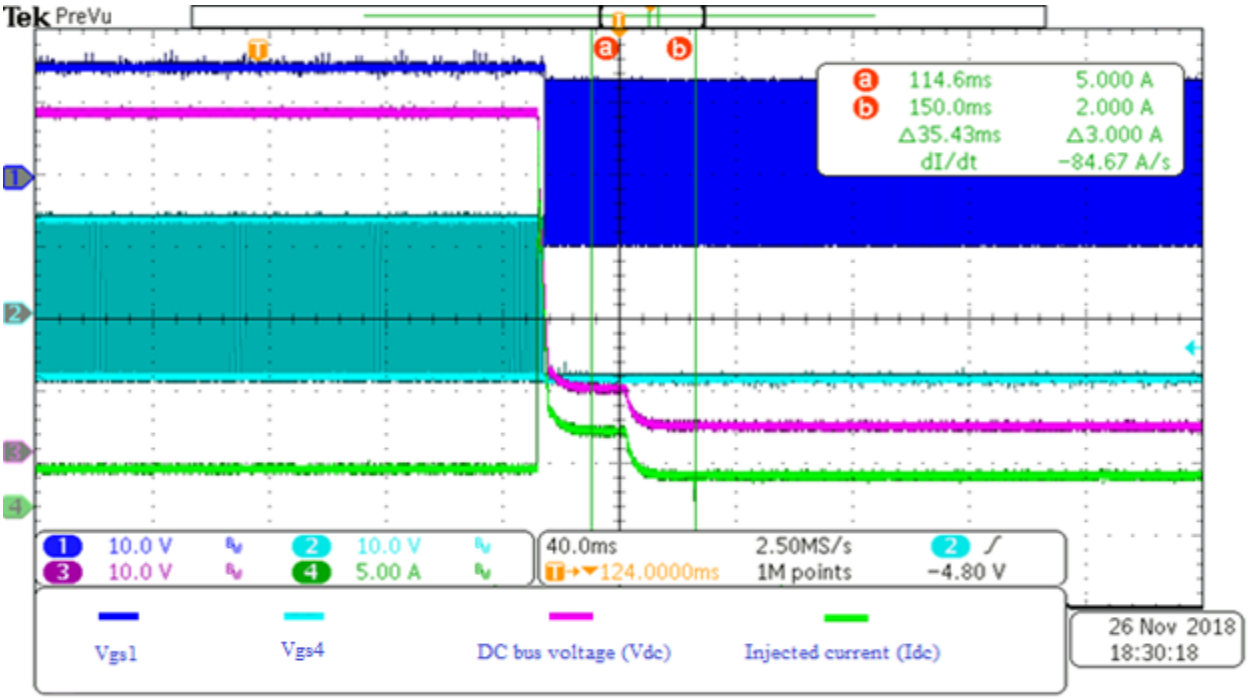


Figure 4.10 Converter in low load impedance condition.

Ch1 (*dark blue*): Vgs1, Ch2 (*sky blue*): Vgs4, Ch3 (*pink*): DC bus voltage (Vdc), Ch4 (*green*): injected current (Idc)

In *Section 4.2.1*(*c*), the operation of the DER under low load impedance condition is analyzed and also the theoretical values are presented. The comparison of the theoretical values and steady state experimental values are presented in Table 4.12. It can be seen that the theoretical values match with those of the experimental tests.

Table 4.12 Comparison of theoretical values and experimental steady state values for the operation of converter during fault detection.

R_{load}'' (Ω)	Type of result	During Fault detection	
		I_{dc} (A)	V_{dc}''
1.82	Theoretical	5	9.1
	Experimental	5	9.2

Power supply in low load impedance (fault) condition

The operation of the power supply in low load impedance condition is shown in Figure 4.11. In the beginning, a 20Ω load is connected and (V_{dc}), pink curve, is 46.8V and injected current (I_{dc}), green curve, is 2.4A. Then, a fault resistance (R_{fault}) of 2Ω is connected to the original load, (20Ω). Once the fault resistance is connected, a high peak current is observed which is due to behavior of power supply in transient, however it limits the steady state current to 5A as adjusted and the DC bus voltage decreases to 9V as shown in the Figure below.

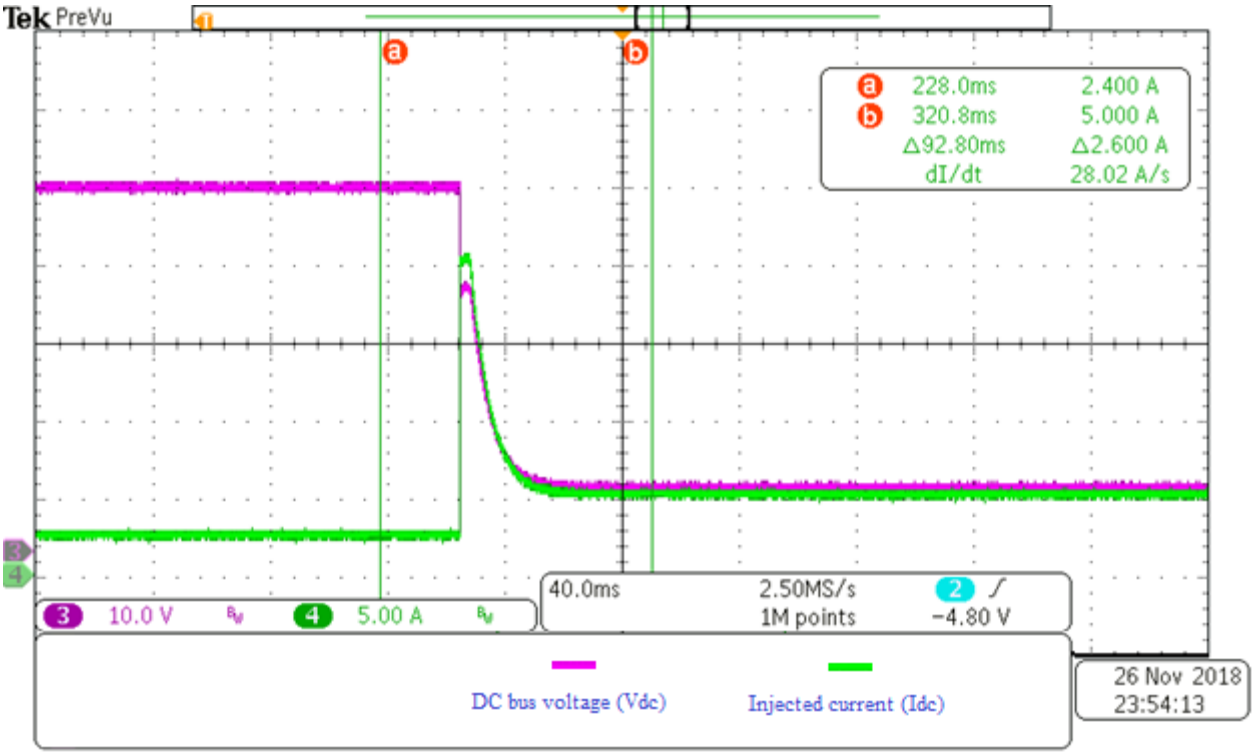


Figure 4.11 Power supply in low load impedance condition.

Ch3 (*pink*): DC bus voltage (Vdc), Ch4 (*green*): injected current (Idc)

Figure 4.11 shows the operation of the power supply in low load impedance condition. In *Section 4.2.1*(*c*), the operation of DER under low load impedance condition is analyzed and also the theoretical values are presented. The comparison of the theoretical values and steady state experimental values are presented in Table 4.13. It can be seen that the theoretical values match with those of the experimental tests.

Table 4.13 Comparison of theoretical values and experimental steady state values for the operation of power supply in low load impedance condition.

R_{load}'' (Ω)	Type of result	During Fault detection	
		I_{dc} (A)	V_{dc}''
1.82	Theoretical	5	9.1
	Experimental	5	9.0

4.3.2 Results with both DERs, interface nodes and communication

In this Section, the results are shown when complete system is implemented as shown in Figure 4.1, with both DERs, interface nodes and communication to verify the proposed fault protection scheme. In such a case, the protection scheme should open only the faulted segment. The experimental results with both DERs in current limit (normal) and low load impedance (fault) conditions are shown in this Section.

a) Current limit (normal) condition

The operation of converter and power supply operating together in current limit (normal) condition is shown in Figure 4.12, which is tested by connecting a 3.5Ω resistance at point 'B' to ground in Figure 4.1. In the beginning, the system is operating in droop region, the DC bus voltage at converter (V_{dc}), sky blue curve, is 47.4V, current I_{cs2}, green curve, is 400mA and I_{cs3}, pink curve, is -400mA. Then, a 3.5 Ω resistance is connected at point 'B' to ground in Figure 4.1, V_{dc} decreases to 30.2V, both the DERs start operating at maximum current limit (5A), I_{cs2} rises to 4.5A and I_{cs3} falls to -4.5A. A high current peak is observed in transient, which is due to the energy stored in the converter's output capacitor that the capacitor releases when the voltage decreases due to a higher load drawing more power and also due to the transient behavior of power supply, that first goes to a high transient current and then it limits the steady state current at the expected value. However, both the DERs operate as expected in steady state.

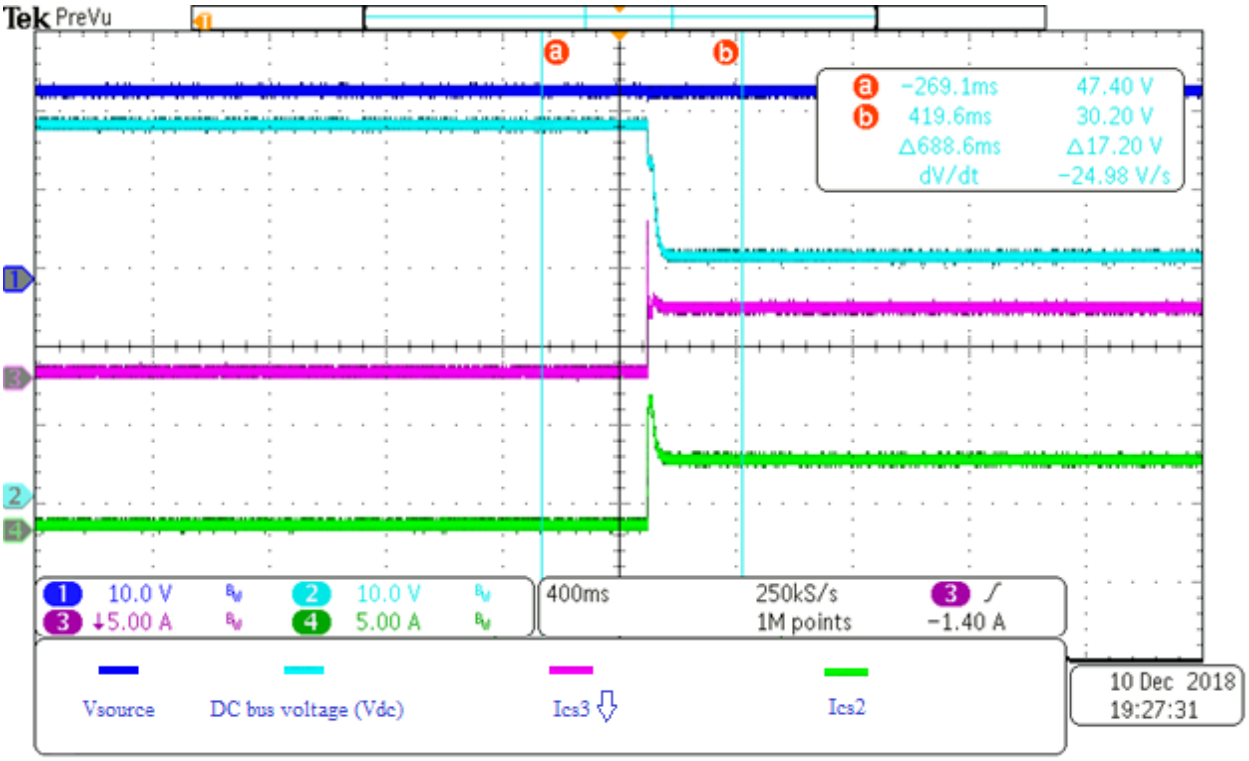


Figure 4.12 DERs in current limit (normal) condition.

Ch1 (*dark blue*): Vsource, Ch2 (*sky blue*): DC bus voltage at converter (Vdc), Ch3 (*pink*): Ics3 (inverted) Ch4 (*green*): Ics2

In *Section 4.2.2*(*a*), the operation of both DERs together in current limit (normal) condition is analyzed and also the theoretical values are presented. The comparison of the theoretical values and steady state experimental values are presented in Table 4.14. It can be seen that they match very well with each other.

Table 4.14 Comparison of theoretical values and experimental steady state values with both DERs in current limit (normal) condition.

R_{load}' (Ω)	Type of result	I_{cs2} (A)	I_{cs3} (A)	V_{dc}' (V)
2.98	Theoretical	4.5	-4.5	29.8
	Experimental	4.5	-4.5	30.2

b) Low load impedance (fault) condition

For this case, it is important to consider the transient characteristic of the power supply and converter, in case of a variation in the load. When a low impedance is connected, the power supply current flow with no control for a short transient time before limiting the current to steady state. Also, the converter produces a high transient peak current. For the converter, the current that is controlled is the average current in the inductor, and from this current the injected current reference is generated. This high transient peak of converter is due to the energy stored in the converter's output capacitor that the capacitor releases when the voltage decreases due to a higher load drawing more power. For testing the proposed logic experimentally, once the fault occurs, a 50ms delay is introduced before implementing the fault detection logic, so anything happens in the transients can be disregarded. As the time for fault detection is 30ms, due to this delay, the total time will be the sum of 50ms (transient delay) delay and 30ms (fault detection time), which will be 80ms.

Results with communication

When a fault occurs at bus 'A':

The operation of the system when a fault occurs at bus 'A' is shown in Figure 4.13. In the beginning, the system is operating under droop control and the DC bus voltage at converter (V_{dc}), sky blue curve, is 47.4V, current I_{cs1}, pink curve, is 800mA and I_{cs2}, green curve, is 400mA. At t = 80ms, the fault occurs, the DC bus voltage decreases to 10.6V, both the DERs start operating at maximum current limit (5A), I_{cs1} falls to -9.6A and I_{cs2} falls to -4.6A. At t = 160ms, the fault condition is detected, indicated by a fault flag (F) = 1, dark blue curve. The converter starts operating at lower current limit (2A), the contactor K1 is then opened and the faulted segment is isolated. After fault isolation, the system returns to normal operation (droop control), (V_{dc}) increases to 47.6V, $I_{cs1} = 0A$, $I_{cs2} = 800mA$ and the loads 2 and 3 are still fed by the DERs. At 80ms, when the fault occurs, unexpected currents flow for some transient time, which is due to the inherent behavior of the lab power supply in transient. However, the logic is working as expected and anything happening during the transition delay can be disregarded.

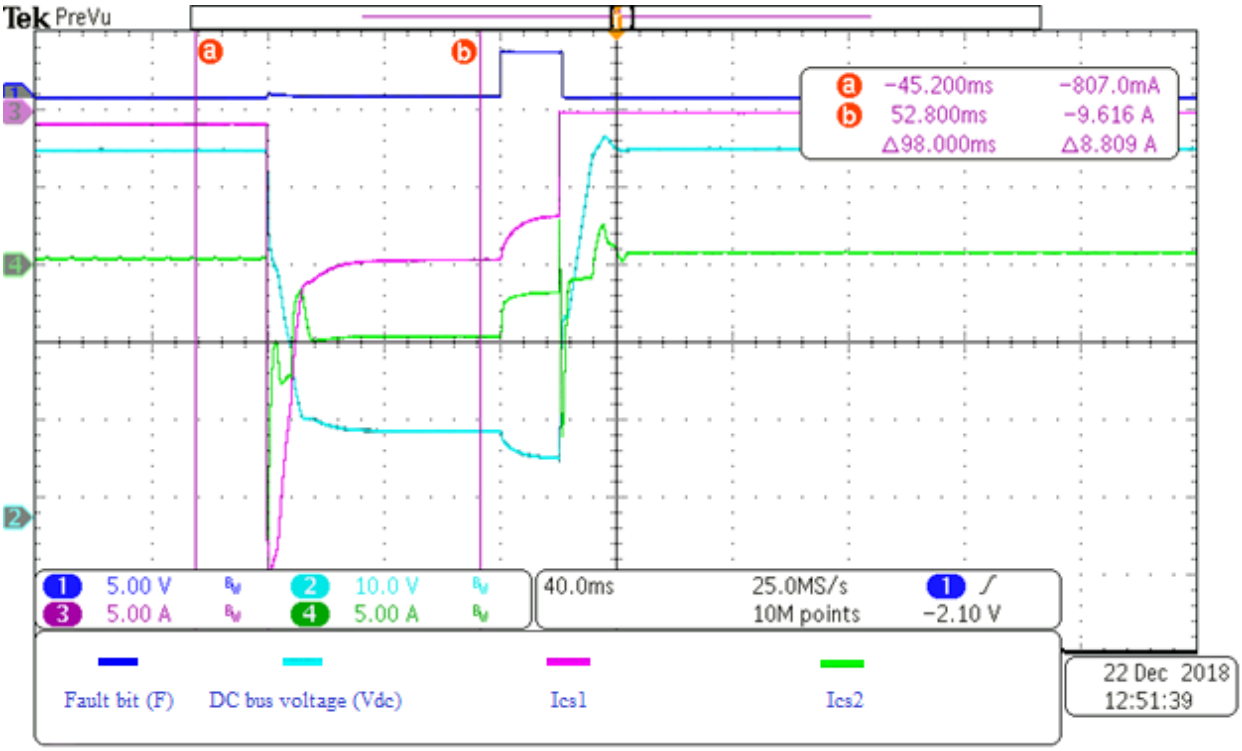


Figure 4.13 Fault is at bus 'A' with communication.

Ch1 (*dark blue*): Fault bit (F), Ch2 (*sky blue*): DC bus voltage at converter (Vdc), Ch3 (*pink*): Ics1, Ch4 (*green*): Ics2

In *Section 4.2.2*(*b*), the operation of both DERs together when a fault is occurs at bus 'A' is analyzed and also the theoretical values are presented. The comparison of the theoretical values and steady state experimental values are presented in Table 4.15. It can be seen that the theoretical values match with those of the experimental tests.

Table 4.15 Comparison of theoretical values and experimental steady state values when fault is at bus A with communication.

R_{load}'' (Ω)	Type of result	During fault detection		
		I_{cs1} (A)	I_{cs2} (A)	V_{dc}'' (V)
1.04	Theoretical	-9.6	-4.6	10.4
	Experimental	-9.6	-4.6	10.6

When a fault occurs at bus ‘B’:

The operation of the system when a fault occurs at bus ‘B’ is shown in Figure 4.14. In the beginning, the system is operating under droop control and the DC bus voltage at converter(V_{dc}), sky blue curve, is 47.4V, current I_{cs2}, pink curve, is 409mA and I_{cs3}, green curve, is –400mA. At t = 80ms, a fault occurs, V_{dc} decreases to 10.5V, both the DERs start operating at maximum current limit (5A), I_{cs2} rises to 4.8A and I_{cs3} falls to -4.8A. At t = 160ms, the fault condition is detected, indicated by a fault flag (F) = 1, dark blue curve. The converter starts operating at lower current limit (2A), the contactors K2 and K3 are then opened and the faulted segment is isolated. After fault isolation, the system returns to normal operation (droop control), V_{dc} increases to 47.6V, $I_{cs2} = 0A$ and $I_{cs3} = 0A$ and the load 1 is fed by the power supply and load 3 is fed by the converter. At 80ms, when the fault occurs, unexpected currents flow for some transient time, which is due to the inherent behavior of the power supply in transient. However, the logic is working as expected and anything happening during the transition delay can be disregarded.

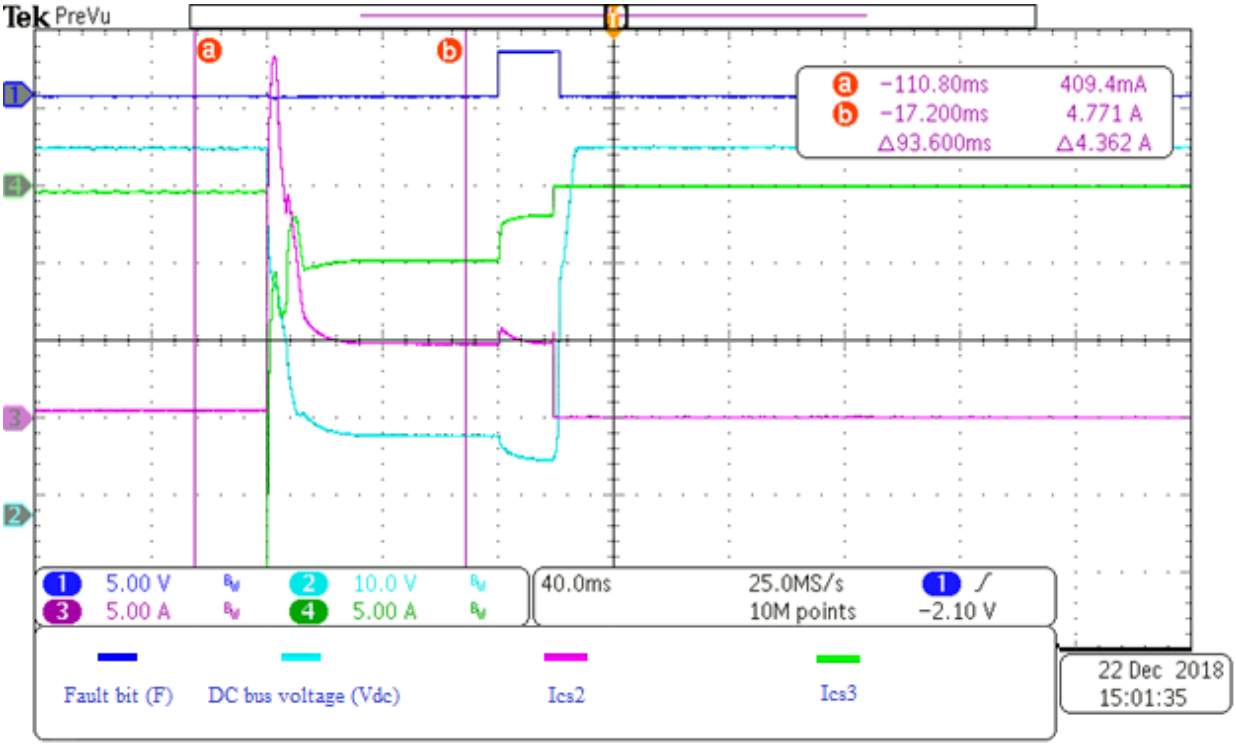


Figure 4.14 Fault is at bus ‘B’ with communication.

Ch1 (*dark blue*): Fault bit (F), Ch2 (*sky blue*): DC bus voltage at converter (Vdc), Ch3 (*pink*): Ics2, Ch4 (*green*): Ics3

In *Section 4.2.2*(*b*), the operation of both DERs together when a fault occurs at bus 'B' is analyzed and also the theoretical values are presented. The comparison of the theoretical values and steady state experimental values are presented in Table 4.16. It can be seen that the theoretical values match with those of the experimental tests.

Table 4.16 Comparison of theoretical values and experimental steady state values when fault is at bus B with communication.

R_{load}'' (Ω)	Type of result	During fault detection		
		I_{cs2} (A)	I_{cs3} (A)	V_{dc}'' (V)
1.04	Theoretical	4.8	-4.8	10.4
	Experimental	4.8	-4.8	10.5

When a fault occurs at bus 'C':

The operation of the system when a fault occurs at bus 'C' is shown in Figure 4.15. In the beginning, the system is operating under droop control and the DC bus voltage at converter (V_{dc}), sky blue curve, is 47.4, current I_{cs3}, pink curve, is -400mA and I_{cs4}, green curve, is 794mA. At t = 80ms, a fault occurs, V_{dc} decreases to 10.5V, both the DERs start operating at maximum current limit (5A), I_{cs3} increases to 4.6A and I_{cs4} increases to 9.6A. At t = 160ms, the fault condition is detected, indicated by a fault flag (F) = 1, dark blue curve. The converter starts operating at lower current limit (2A), the contactor K4 is then opened and the faulted segment is isolated. After fault isolation, the system returns to normal operation (droop control), V_{dc} increases to 47.6V, $I_{cs3} = -800mA$ and $I_{cs4} = 0A$ and the loads 1 and 2 are still fed by the DERs. At 80ms when the fault occurs, unexpected currents flow for some transient time, which is due to the behavior of the power supply in transient. However, the logic is working as expected and anything happening during the transition delay can be disregarded.

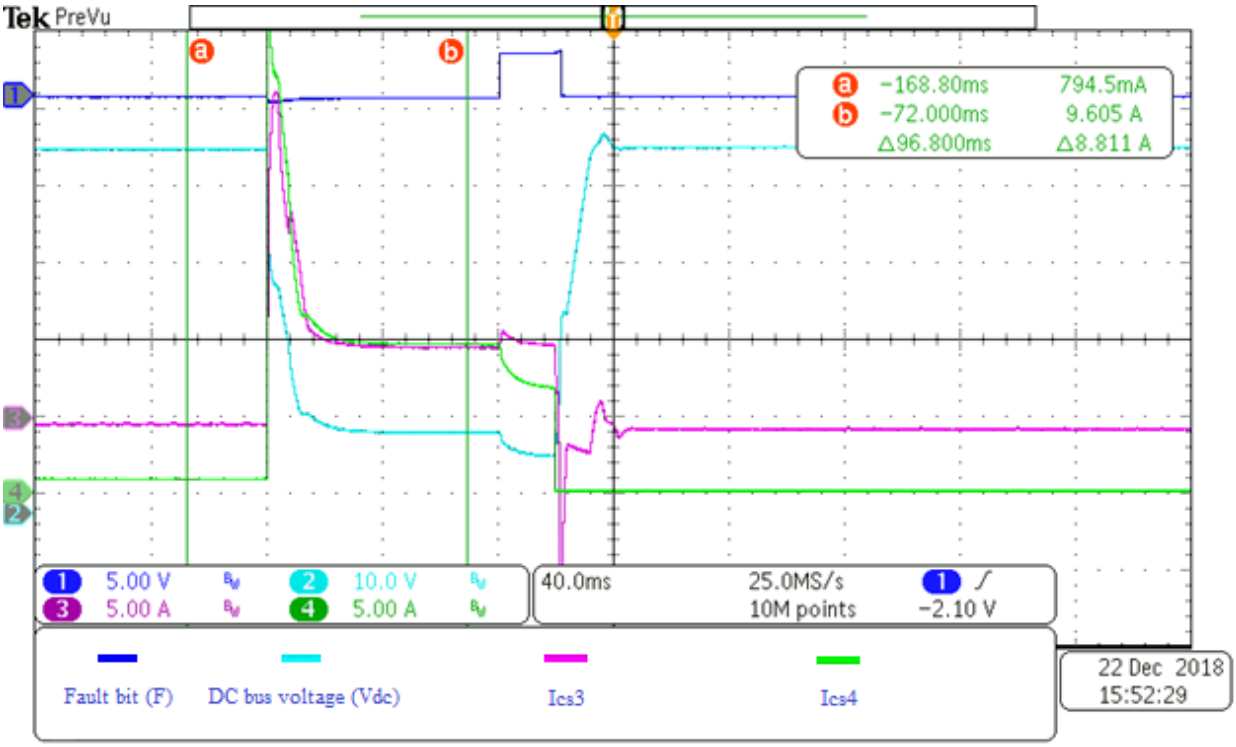


Figure 4.15 Fault is at bus 'C' with communication.

Ch1 (*dark blue*): Fault bit (F), Ch2 (*sky blue*): DC bus voltage at converter (Vdc), Ch3 (*pink*): Ics3, Ch4 (*green*): Ics4

In *Section 4.2.2*(*b*), the operation of both DERs together when a fault occurs at bus 'C' is analyzed and also the theoretical values are presented. The comparison of the theoretical values and steady state experimental values are presented in Table 4.17. It can be seen that the theoretical values match with those of the experimental tests.

Table 4.17 Comparison of theoretical values and experimental steady state values when fault is at bus C with communication.

R_{load}'' (Ω)	Type of result	During fault detection		
		I_{cs3} (A)	I_{cs4} (A)	V_{dc}'' (V)
1.04	Theoretical	4.6	9.6	10.4
	Experimental	4.6	9.6	10.5

Results without communication / communication failure

As mentioned in Chapter 3, even in case of communication failure, some protection actions are performed, so that the fault can be cleared and at least part of the system survives.

When a fault occurs at bus 'A':

The operation of the system without communication when a fault occurs at bus 'A' is shown in Figure 4.16. In the beginning, the system is operating under droop control and the DC bus voltage at converter (V_{dc}), sky blue curve, is 47.4V, current I_{cs1}, pink curve, is -796mA and I_{cs3}, green curve, is -400mA. At t = 80ms fault occurs, V_{dc} decreases to 10.6V, both the DERs start operating at maximum current limit (5A), I_{cs1} falls to -9.6A and I_{cs3} falls to -4.8A. At t = 160ms, the fault condition is detected, indicated by a fault flag (F) = 1, dark blue curve. The converter starts operating at lower current limit (2A), the contactors K1 and K3 are then opened and the faulted segment is isolated. After fault isolation, the system returns to normal operation (droop control), V_{dc} increases to 47.6V, $I_{cs1} = 0A$ and $I_{cs3} = 0A$. It is important to notice that even if there is no communication, the fault at bus 'A' is still cleared and the other loads are still fed, as the power supply is supplying bus 'B' and the converter supplying bus 'C', in this case. At 80ms, when the fault occurs, unexpected currents flow for some transient time, which is due to the behavior of the power supply in transient. However, the logic is working as expected and anything happening during the transition delay can be disregarded.

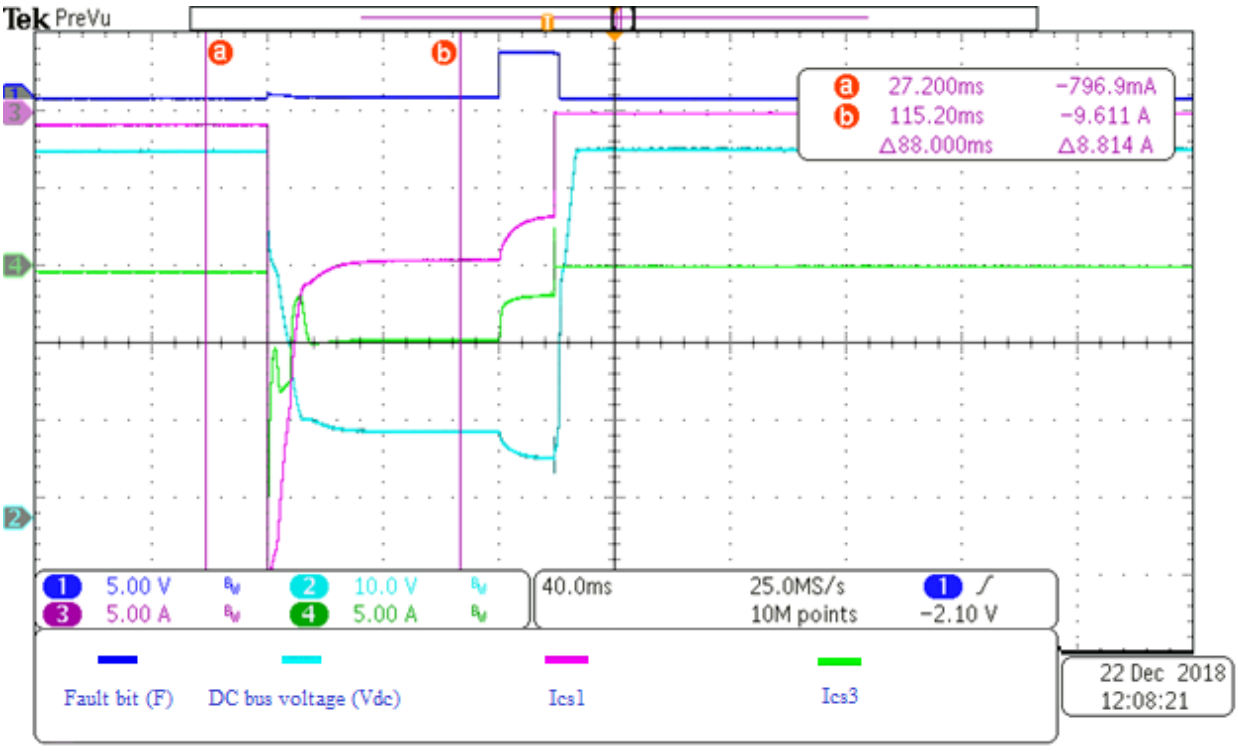


Figure 4.16 Fault is at bus 'A' without communication.

Ch1 (*dark blue*): Fault bit (F), Ch2 (*sky blue*): DC bus voltage at converter (Vdc), Ch3 (*pink*): Ics1, Ch4 (*green*): Ics3

In *Section 4.2.2*(*b*), the operation of both DERs together when a fault occurs at bus 'A' is analyzed and also the theoretical values are presented. The comparison of the theoretical values and steady state experimental values are presented in Table 4.18. It can be seen that the theoretical values match with those of the experimental tests.

Table 4.18 Comparison of theoretical values and experimental steady state values when fault is at bus A without communication.

R_{load}'' (Ω)	Type of result	During fault detection		
		I_{cs1} (A)	I_{cs3} (A)	V_{dc}'' (V)
1.04	Theoretical	-9.6	-4.8	10.4
	Experimental	-9.6	-4.8	10.6

When a fault occurs at bus ‘B’:

The results when a fault occurs at bus ‘B’ without communication are the same as when a fault occurs at ‘B’ with communication and are not shown again, since the same contactors K2 and K3 need to be open in both cases.

When a fault occurs at bus ‘C’:

The operation of the system without communication when a fault occurs at bus ‘C’ is shown in Figure 4.17. In the beginning, the system is operating under droop control and the DC bus voltage at converter(V_{dc}), sky blue curve, is 47.4, current I_{cs2}, pink curve, is 400mA and I_{cs4}, green curve, is 796mA. At t = 80ms, a fault occurs, V_{dc} decreases to 10.5V, both the DERs start operating at maximum current limit (5A), I_{cs2} increases to 4.8A and I_{cs4} increases to 9.6A. At t = 160ms, the fault condition is detected, indicated by a fault flag (F) = 1, dark blue curve. The converter starts operating at lower current limit (2A), the contactors K2 and K4 are then opened and the faulted segment is isolated. After fault isolation, the system returns to normal operation (droop control), V_{dc} increases to 47.6V, $I_{cs2} = 0A$ and $I_{cs4} = 0A$. It is important to notice that even if there is no communication, the fault at bus ‘C’ is still cleared and some loads are still fed, as the power supply is supplying bus ‘A’ and the converter is supplying bus ‘C’, in this case. At 80ms, when the fault occurs, unexpected current flow for some transient time, which is due to the behavior of the power supply in transient, however the logic is working as expected and anything happening during the transition delay can be disregarded.

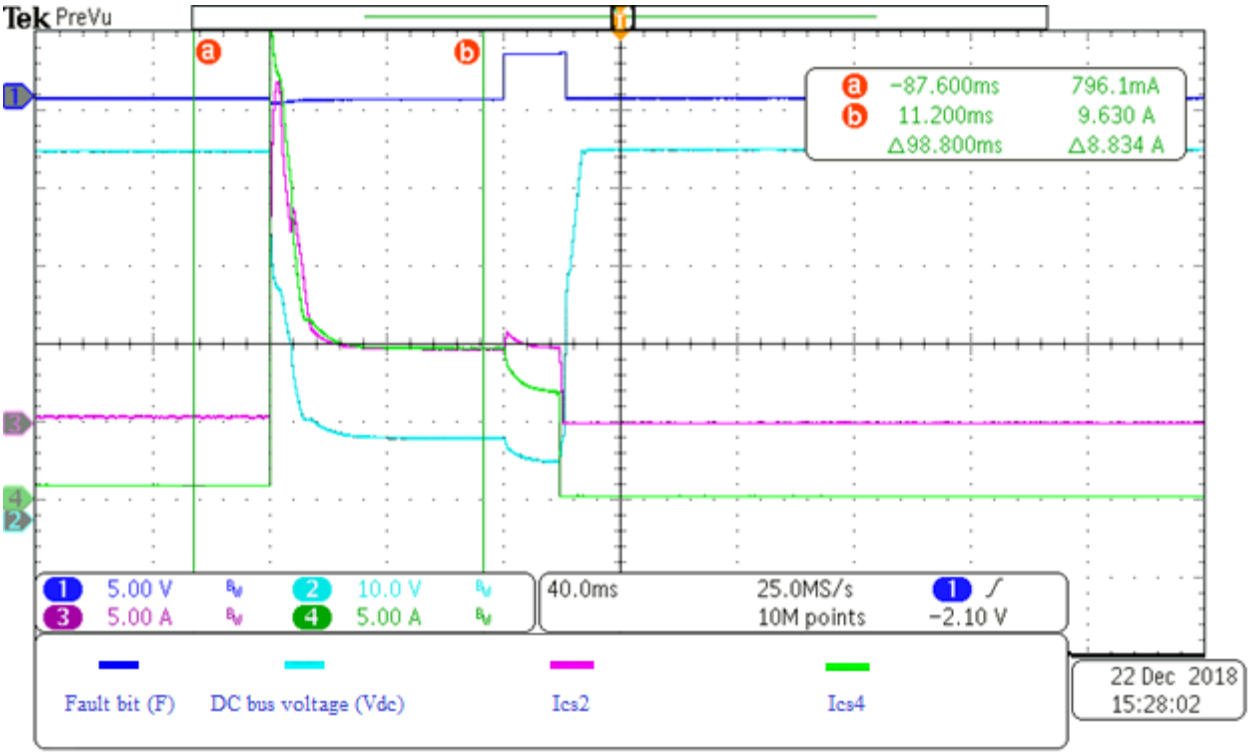


Figure 4.17 Fault is at bus 'C' without communication.

Ch1 (*dark blue*): Fault bit (F), Ch2 (*sky blue*): DC bus voltage at converter (Vdc), Ch3 (*pink*): Ics2, Ch4 (*green*): Ics4

In *Section 4.2.2*(*b*), the operation of both DERs together when a fault occurs at bus 'C' is analyzed and also the theoretical values are presented. The comparison of theoretical values and steady state experimental values are presented in Table 4.19. It can be seen that the theoretical values match with those of the experimental tests.

Table 4.19: Comparison of theoretical values and experimental steady state values when fault is at bus C without communication.

R_{load}'' (Ω)	Type of result	During fault detection		
		I_{cs2} (A)	I_{cs4} (A)	V_{dc}'' (V)
1.04	Theoretical	4.8	9.6	10.4
	Experimental	4.8	9.6	10.5

4.4 Summary

The proposed fault protection scheme for the DC nanogrid is implemented and its performance is reported in this Chapter. The interface nodes are used to detect the fault current and to isolate the faulted segments of the DC bus. Based on the proposed fault location method, the fault location is determined and only the faulted segment is isolated, to avoid entire system shutdown. The performance of the fault protection scheme is also verified by showing the theoretical calculations and experimental results. However the transient response of an "emulated DER" is not identical to that of a real current controlled 4-switch converter, mostly during the transient following a low impedance fault load. Besides, this emulated DER is not able to reduce the injected current to I_{dc_lcl} following a fault detection. In the next Chapter, the conclusions of this work and the guidelines for future work are presented.

Chapter 5 Conclusions

5.1 Summary

This Thesis presented a fault protection scheme for a DC nanogrid with distributed energy resources (DERs) based on the coordination of a fault-insensitive converter, i.e. a bi-directional 4-switch DC-DC converter, with appropriate current control scheme, and low-cost contactors. The location of the faulted segment(s) is identified by means of peer-to-peer communication between neighboring DERs. This allows only the faulted segment(s) to be opened keeping the healthy part of the DC nanogrid energized.

In Chapter 2, a bi-directional 4-switch DC-DC fault-insensitive converter was presented as the required alternative to the conventional Class-C. The primary goal of this topology is to control the current injected into the DC nanogrid, in normal as well as faulted conditions. The converter normally operates in the Class-C mode of operation under normal conditions when the source interface voltage is significantly lower than that of the DC bus. Further, the amount of current injected is decided by a VI droop curve, the hierarchical control scheme with a primary control level based on DC bus signaling (DBS) generally used to interface DER units to a DC bus. Conversely, the converter switches to the Buck mode of operation in fault conditions when the DC bus voltage decreases to a low value, to ensure that one does not loses the control of the current injected by the power converter. A PI type controller was designed for regulating the inductor current regardless of the mode of operation. A strategy for the transition between modes has been presented as well. From the simulation results presented in Chapter 2, it is observed that the controller provides good performance in both modes, and the expected results were obtained. It was also shown that the 4-switch current-controlled converter is capable of switching automatically from the Class-C mode (normal operation) to the Buck mode (faulted system).

Secondly, a fault protection scheme for a DC nanogrid was developed and presented in Chapter 3. This scheme employed a valid substitute for high rating, bulky size and costly circuit breakers (CBs) with low-cost, smaller size and low-current contactors. Firstly, the operation of the protection scheme was described showing how the combination of current-controlled power interfaces and contactors can protect and reconfigure a DC nanogrid, in response to a fault in the DC bus. This method utilizes the current limiting feature of the power interfaces to limit and reduce

the fault current to a low value, so that the contactors can open with less risk. A fault detection technique was presented which is based on a maximum current and low DC bus voltage set point. Moreover, a fault location and isolation logic was developed based on peer-to-peer communication between neighboring units of the "interface node," with current sensors and contactors, to identify which segment(s) of the DC nanogrid is(are) faulted and which contactor(s) should open. In this work, this was implemented with Controller Area Network (CAN) communication. Finally, a backup protection strategy was also presented for the case of communication failure, so that the fault can still be cleared.

In Chapter 4, a laboratory-scale hardware based DC power system was developed to experimentally verify the effectiveness of the developed protection scheme for a DC nanogrid with distributed energy resources (DERs). Complete details of the circuits and systems used in the experimental set-up were shown and described in this Chapter. Theoretical calculations were performed for the experimental tests of DERs in different cases. Finally, experimental results were presented for all the cases. The results shown that the developed protection scheme was accurate, satisfactorily identifying a fault and its location and isolating only the faulted segment, protecting the entire system from a shutdown. The comparison of the theoretical values with experimental results was also presented, where one can see that the experimental results are very similar to those of the theoretical calculations.

A fault protection scheme capable to detect, locate and isolate the faults for a DC nanogrid was the main goal of this work. As shown in this Thesis, a fault protection scheme with this criteria was successfully designed and accomplished.

5.2 Future work

A lot of research needs to be done in this field especially for the implementation of DC nanogrids. Some of the suggestions for future work related to this study are as follows:

- In this work, a single unit of the 4-switch DC-DC converter was built. For tests with multiple distributed energy resources, a standard laboratory power supply operating as a regulated lab voltage source with a limited current was employed. It is evident that the behavior of the power supply was not identical to that of a real current controlled 4-switch

DC-DC converter. One of the potential future works is to get the results with two power converters.

- Develop an approach for reconnecting the faulted segment to the remainder of the DC nanogrid after fault clearance.
- The fault protection method has been verified experimentally at the low voltage, low power level. These results give confidence that the protection scheme can also be tested for a higher voltage and power level in the further research work.

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