Analysis and Design of Discontinuous Conduction Mode AC-DC Power Factor Correction Converters

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ABSTRACT

Analysis and Design of Discontinuous Conduction Mode AC-DC Power Factor Correction Converters

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In more electric aircrafts (MEAs), the synchronous generators are connected directly to the turbo-engine to develop constant voltage variable frequency (CVVF) AC supply bus. In addition, the MEA has adopted high voltage DC bus in its power system to cater the various categories of load used by aircraft. Therefore, the MEA requires AC-DC power converters to convert CVVF AC to constant DC. Existing diode-bridge based passive multi-pulse AC-DC converters are suffering from heavy and bulky low frequency 350 Hz transformers, poor input power quality, low efficiency and unregulated output voltage. To overcome these drawbacks, this thesis work proposes and studies several new active switched-mode AC-DC converters (isolated and non-isolated) strictly satisfying the enhanced requirements of the aircraft application. The vital constituent in active AC-DC power conversion is the power factor correction (PFC). Understanding the certain limitations of the continuous conduction mode (CCM) operation for CVVF AC supply, the proposed converters are designed to operate in discontinuous conduction mode (DCM) to make use of its obvious benefits such as inherent PFC, reduced number of sensors, simple control, inherent zero current turn-on of the switches, and inherent zero diode reverse recovery losses. A single sensor based simple voltage control loop is only used to obtain the tightly regulated output voltage, which makes it economical, and improves the system reliability and robustness to high-frequency noise.

At first, a three-phase modular single-stage-isolated Cuk converter is proposed on considering Cuk converter merits such as inrush current limitation, no input filter requirement, and easy implementation of high frequency transformer isolation. The phase-modular converters are easy to implement, can be paralleled easily for high power design, operational with two-phase loss, and provide quick repair and maintenance. However, they employ more number of components and

suffering from higher conduction losses. To overcome these issues, a new direct three-phase non-isolated Cuk-derived PFC converter with reduced number of components and conduction losses is proposed. With this new topology, the conduction losses are significantly reduced, and efficiency is improved by 4 % compared to the previously analyzed phase-modular converter. However, this converter needs two DC-link capacitors for its operation at DC output that added extra capacitive losses. Further to reduce the capacitive losses, a new direct three-phase non-isolated buck-boost-derived PFC converter with one DC-link capacitor and reduced capacitive losses, along with retention of all the benefits of Cuk-derived PFC converter is proposed. For high power operations, interleaved topology of the three-phase buck-boost-derived PFC converter with reduced filter size, reduced losses, and improved efficiency is proposed. Finally, an isolated topology of the three-phase buck-boost-derived PFC converter with a novel clamping circuit to capture and utilize the transformers leakage inductance energy in order to improve the converter efficiency is proposed. The converters steady-state operation, DCM condition, and design equations are reported in detail. The small-signal models for all the proposed topologies using average current injected equivalent circuit approach are developed, and a detailed closed-loop controller design is illustrated. The simulation results from PSIM 11.1 software and the experimental results from proof-of-concept laboratory hardware prototypes are provided in order to validate the report analysis, design, and performance.

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List of Abbreviations

AC	Alternating Current – represents alternating quantities
ACARE	Advisory Council for Aeronautics Research in Europe
AP	Area Product
APU	Auxiliary Power Unit
ATRU	Auto Transformer Rectifier Unit
ATU	Auto Transformer Unit
CCM	Continuous Conduction Mode
CIECA	Current Injected Equivalent Circuit Approach
CVVF	Constant Voltage Variable Frequency
DAB	Dual Active Bridge
DCM	Discontinuous Conduction Mode
DCVM	Discontinuous Capacitor Voltage Mode
DICM	Discontinuous Inductor Current Mode
DIICM	Discontinuous Input Inductor Current Mode
DOICM	Discontinuous Output Inductor Current Mode
GM	Gain Margin
HF	High Frequency
IDG	Integrated Drive Generator
LC	Inductor-Capacitor
LCD	Inductor-Capacitor-Diode
MEA	More Electric Aircraft
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NASA	National Aeronautics and Space Administration
PF	Power Factor

PFC	Power Factor Correction (or Corrected)
PLL	Phase-Locked-Loop
PM	Phase Margin
PWM	Pulse Width Modulation
RCD	Resistor-Capacitor-Diode
RMS	Root mean square
SEPIC	Single-Ended Primary-Inductor Converter
SSPC	solid-state power controllers
UPF	Unity Power Factor
THD	Total Harmonic Distortion
TRU	Transformer Rectifier Unit
ZCS	Zero-Current Switching

List of Symbols

$C_{1a,b,c}$	Input side energy transfer Cuk capacitors
$C_{2a,b,c}$	Output side energy transfer Cuk capacitors
$C_{ia,b,c}$	Intermediate energy transfer capacitors
C_k	Clamping capacitor
C_f	Input filter capacitor
C_o	Output filter capacitor
d , D	Duty cycle of the switch
f	Line frequency
f_s	Switching frequency
$i_a,\ i_b,\ i_c$	Input phase currents
$i_{Lia},\ i_{Lib},\ i_{Lic}$	Input inductor currents
$i_{Loa},\ i_{Lob},\ i_{Loc}$	Output inductor currents
$i_{fwa,b,c}$	Freewheeling currents
$i_{Tpa,b,c}$	Transformer primary currents
$i_{Tsa,b,c}$	Transformer secondary currents
$i_{da,b,c}$	Output diode currents
i_{do}	Output current before capacitor filter
i_o	Load current
i_c , i_{co}	Output filter capacitor current
$i_{o,avg}$	Switching cycle average output current
$I_{o,avg}$	Line period average output current
I_{o_n}	Normalized average output current
$i_{ab},\ i_{bc},\ i_{ca}$	Flyback transformer primary currents

$i'_{ab},\ i'_{bc},\ i'_{ca}$	Flyback transformer secondary currents
$i_{sw,a,b,c}$	Currents through the power switches
$i_{af},\ i_{bf},\ i_{cf}$	Unfiltered input currents
k_a	Conduction parameter
$k_{a,crit}$	Critical conduction parameter
$L_{1a,b,c},\ L_{ia,b,c}$	Input inductances
$L_{2a,b,c}$, $L_{oa,b,c}$	Output inductances
$L_{ma,b,c}$	Transformers magnetizing inductances
$L_{la,b,c}$	Transformers leakage inductances
L_f	Input filter inductance
M	Voltage conversion ratio
M_{cr}	Critical voltage conversion ratio
n	Transformer turns ratio
P_{in}	Converter input power
P_o	Converter output power
$P_{Ll,avg}$	Average power transferred from transformer leakage inductances
t_{on}	On time period of the switch
T_s	One switching cycle time period
$t_{dkon,k=a,b,c}$	On time period of the output diodes
$T_a,\ T_b,\ T_c$	Flyback transformers
$v_{a,b,c}$	Input phase voltages
v_o	Converter output voltage
$v_{o,ref}$	Reference output voltage
V_m, I_m	Peak value of phase input voltage and phase input current

$V_{m,min}$	Minimum value of phase input peak voltage
$V_{m,max}$	Maximum value of phase input peak voltage
$v_{c1a,b,c}$	Voltage across input Cuk capacitor
$v_{c2a,b,c}$	Voltage across output Cuk capacitor
$V_{Tpa,b,c}$	Voltages across transformer primary
$V_{Tsa,b,c}$	Voltages across transformer secondary
$V_{swa,b,c}$	Voltages across power switches
V_{ck}	Clamping capacitor average voltage
ΔV_{ck}	Clamping capacitor voltage ripple
Δi_a , Δi_{Li}	Input current ripple

Chapter 1 : Introduction

1.1 Introduction

At present, the worldwide air traffic has significantly increased compared to the twentieth century and has been estimated to increase at a rate of 5-7% in the foreseeable future. This is mainly due to the technological advancements in the aircraft systems that lead to the improved aircraft efficiency and the reduced operating costs. As of today, the air transport is responsible for 2% of the total man-made carbon emissions and is estimated to increase further by 3% in the next twenty years [1]. Thus, if proper measures are not taken for limiting the carbon emissions from a single empty aircraft then the aviation industry is expected to contribute to the global climatic change. Therefore, in this regard, the Advisory Council for Aeronautics Research in Europe (ACARE) has set the goals for 2020 (short-term) and for 2050 (long-term) on carbon and NO_X emissions released by a single aircraft and are given in Table 1.1. This includes 50% reduction of CO_2 emissions, 80% reduction of NO_X emissions by 2020, and a further 25% reduction of CO_2 emissions, 10% reduction of NO_X emissions by 2050 [2], [3]. Thus, a substantial improvement in the aircraft system efficiency is required in order to reduce the single aircraft fuel consumption, and thereby, the carbon emissions. A study from National Aeronautics and Space Administration (NASA) reported that by replacing the less efficient hydraulic, pneumatic and mechanical systems with a single highly efficient electrical system in a medium range conventional civil aircraft such as Boeing 767 would result in 10% weight reduction of an empty aircraft, 9% increase in the fuel efficiency, and 13% reduction in the thrust required from the engine [4]. The main reason for this weight reduction is the use of single electrical system allows the load sharing for the entire flight profile resulting in a compact and lighter power system. Therefore, in view of this, the more electric aircrafts (MEAs) such as Airbus A380, and Boeing 787 are commercially evolved by incorporating more electrical systems.

Table 1.1: ACARE goals for 2020 and 2050

Goals	**2020**	**2050**
CO_2 emissions reduction	50 %	75 %
NO_X emissions reduction	80 %	90 %
External noise reduction	50 %	65 %
Fuel consumption reduction	50 %	-----

1.2 Literature review

In this section, a detailed review of conventional and more electric power system architectures is provided. Further, a detailed study of the AC-DC converters suitable for more electric aircraft system is provided, and their merits and demerits are discussed.

1.2.1 Conventional aircraft power system architecture

Fig. 1.1, shows the architecture of conventional aircraft power system, which is adopted in Airbus A320, and Boeing 767 [5]-[7]. It contains two synchronous generators located on each wing of the aircraft, are driven by the turbo engines and function as main source of power during fly. The power system also contains one auxiliary synchronous generator located on aft of the aircraft and is driven by the auxiliary power unit to power the aircraft on ground, and also serves as back-up power during fly. The power system consists of two AC buses of voltage levels 115 V, 400 Hz, and one 28 V DC bus. The constant voltage 115 V AC is obtained by using the voltage control unit for each synchronous generator, and the constant frequency 400 Hz is obtained by connecting a heavy variable-gear-ratio mechanical gearbox between the engine and the generator,

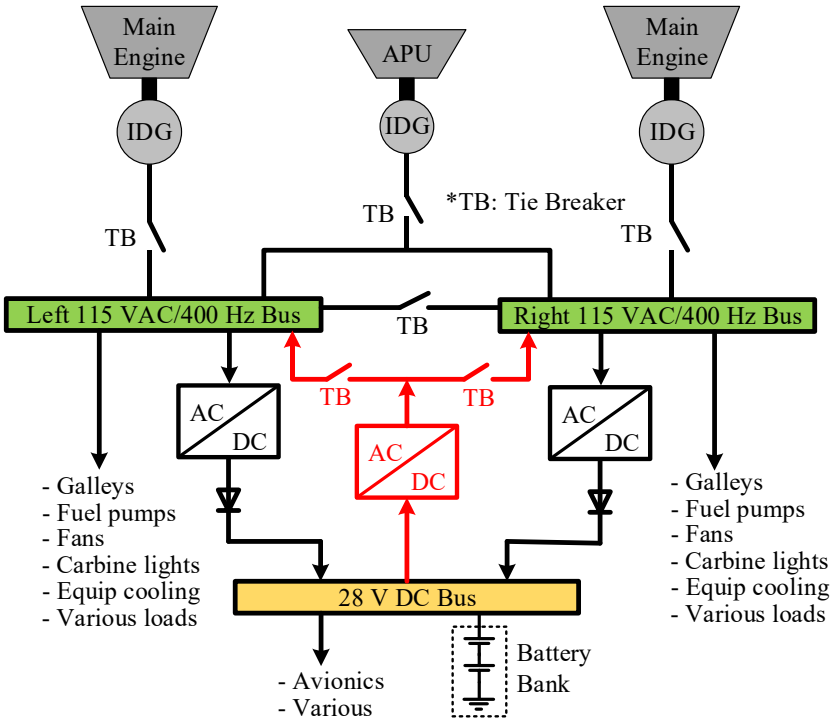


Fig. 1.1. Architecture of conventional aircraft power system.

which is generally integrated into the synchronous generator termed as integrated drive generator (IDG). To maintain the redundancy of the power system, each of these generators and the AC buses are connected through tie breakers, and the power can be circulated in either way. The transformer rectifier units (TRUs) are generally employed to obtain the isolated 28V DC from the AC due to their simple and reliable operation [8]. This power system used the battery as an emergency source of power.

1.2.2 More electric aircraft power system architecture

Fig. 1.2 shows the typical power system architecture of an MEA, which is adopted in Airbus A380 and Boeing 787 [6], [7], [9]-[11]. It comprises of AC (115/230 V), high voltage DC (270/540 V), and low voltage DC (28 V) buses coupled with several solid-state power controllers (SSPC) to accommodate the redundancies required for emergency. The constant speed IDG is removed in MEA architecture and the synchronous generators are directly connected to the turbo engine that resulted in variable frequency AC bus system, the frequency typically varies from 360 Hz to 800 Hz. The elimination of IDG is resulted in significant benefits including reduced weight, reduced

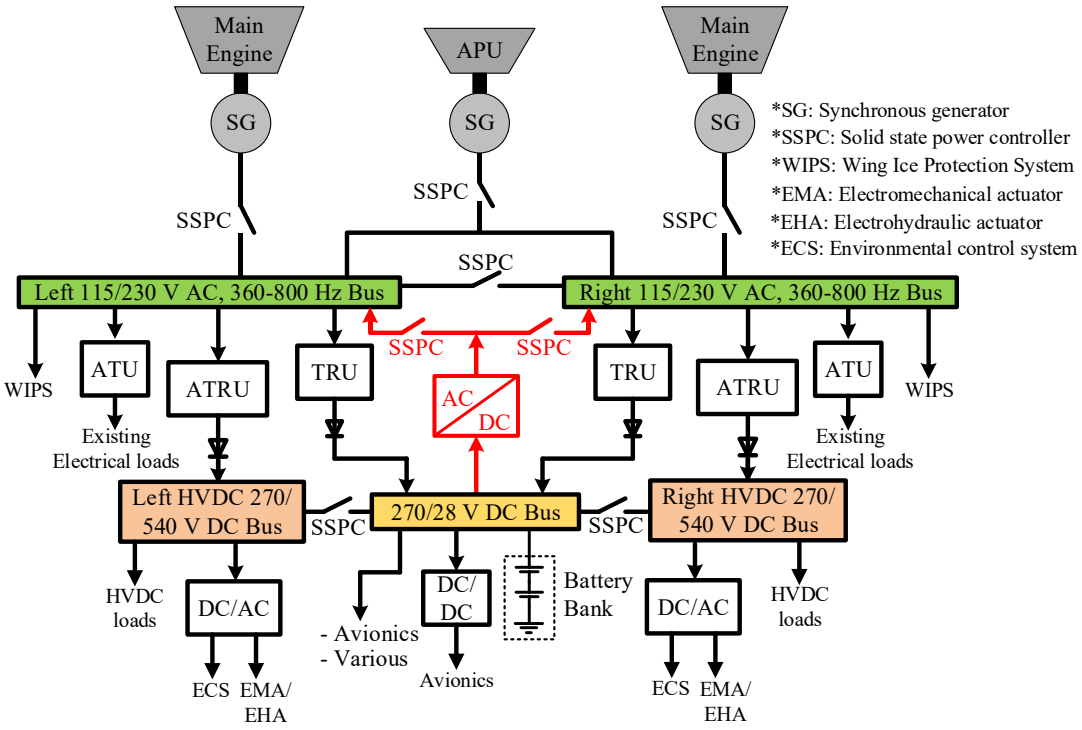


Fig. 1.2. Architecture of MEA power system.

maintenance cost, and improved reliability [12]. Fig. 1.3 shows the benefits of MEA Boeing 787 when compared to the conventional aircraft Boeing 767. The Boeing 787 has 20% better fuel economy which resulted in reduced CO_2 and NO_X emissions, as well as huge reduction in noise footprint owing to the elimination of engine bleed air system in MEA.

The Airbus A380 employs 115 V AC variable frequency bus whereas the Boeing 787 employs 230 V AC variable frequency bus. In accordance, high voltage 270 V DC bus and 540 V DC bus systems are adopted, respectively to reduce the weight of the cables. Therefore, the employment of variable frequency AC bus necessitated several power converters including AC-DC, AC-AC, DC-AC, and DC-DC converters to supply the generated power to various electrical loads, as shown in Fig. 1.2. The power conversion should possess high power quality, reliability, efficiency and power density (less number of components and sensors). In addition, the converters should also provide a degraded but continuous operation in case of a single-phase open failure.

1.2.3 Power electronic converters in MEA

The MEA requires several power electronic converters such as AC-DC, AC-AC, DC-AC, and DC-DC to supply different electrical loads, as shown in Fig. 1.2. The auto-transformer rectifier

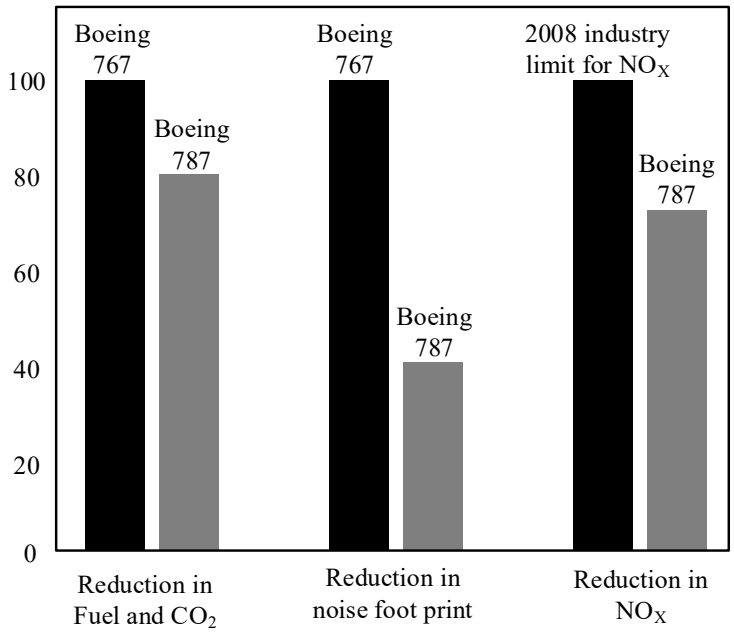


Fig. 1.3. Benefits of MEA Boeing-787 compared to conventional aircraft Boeing-767 [12].

unit (ATRU) is a non-isolated three-phase AC-DC converter that converts the constant voltage variable frequency (CVVF) AC into constant DC voltage. The transformer rectifier unit (TRU) is an isolated three-phase AC-DC converter, which combines the functions of transformer and rectifier in one unit to convert the CVVF AC into a low voltage DC with electrical isolation. The auto-transformer unit (ATU) is typically an AC-AC converter that converts the CVVF AC voltage into constant voltage constant frequency AC. This thesis mainly focuses on the AC-DC converters i.e., both ATRU and TRU. Since the MEA power system does not offer any energy storage element at AC mains, the power flow from AC-DC converters should be maintained always unidirectional from AC mains to the loads [13].

1.2.4 AC-DC converters (rectifiers) for MEA

Fig. 1.4 gives an overview of the unidirectional AC-DC converters according to [13]. Basically, two types of AC-DC power conversions are reported in literature; 1) passive power conversion, 2) active power conversion. The passive power converters employ huge passive components along with diode rectifiers to obtain the DC supply, whereas the active power converters employ semiconductor switching devices generally operating at higher switching frequency in order to reduce the size of passive components.

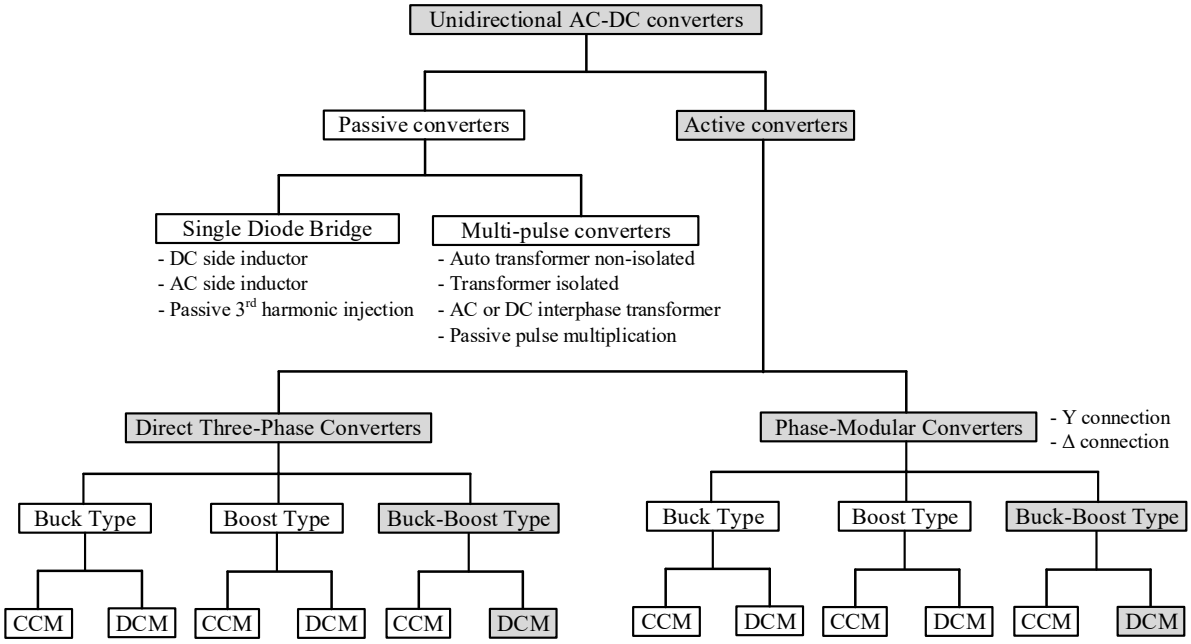


Fig. 1.4. Overview of the unidirectional AC-DC converters according to [13].

1.1.1.1 Passive AC-DC converters

The passive AC-DC power converters are presently used in MEAs due to their simple and reliable operation. In order to meet the harmonic limits set by the airborne standard DO-160G [14], and the military standard MILSTD704F [15], the 12- pulse diode based passive ATRUs and TRUs have been chosen to generate the non-isolated DC supply and the isolated DC supply, respectively from the CVVF AC supply. The schematic of the conventional 12-pulse ATRU [16], [17] and TRUs [18], which are employed in MEAs are shown in Fig. 1.5, and Fig. 1.6, respectively. The operation of both the rectification is similar except the type of transformer employed at AC supply for generating the two partial current systems phase shifted by 30^0. The ATRU employs a non-

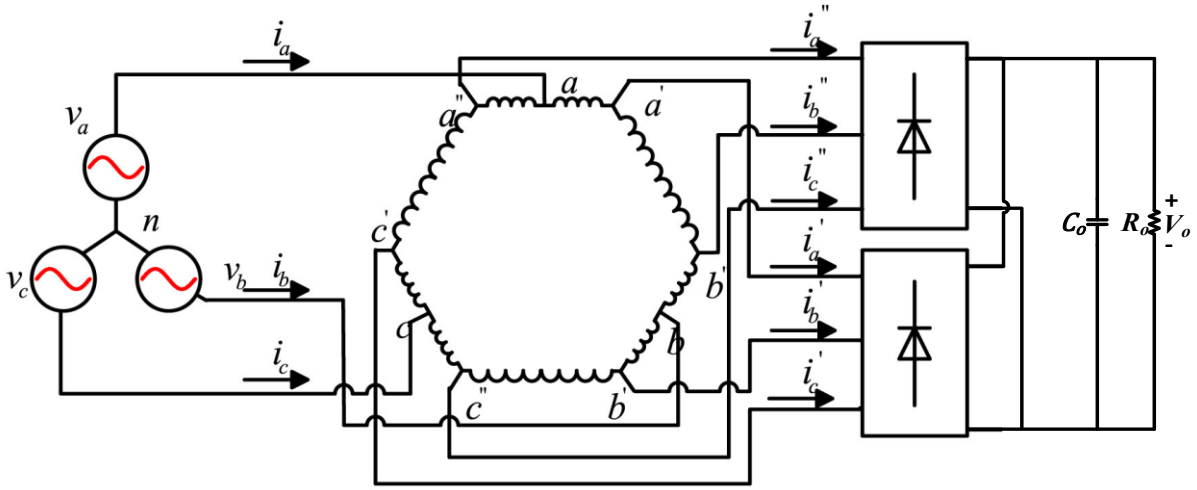


Fig. 1.5. The schematic of conventional 12-pulse ATRU.

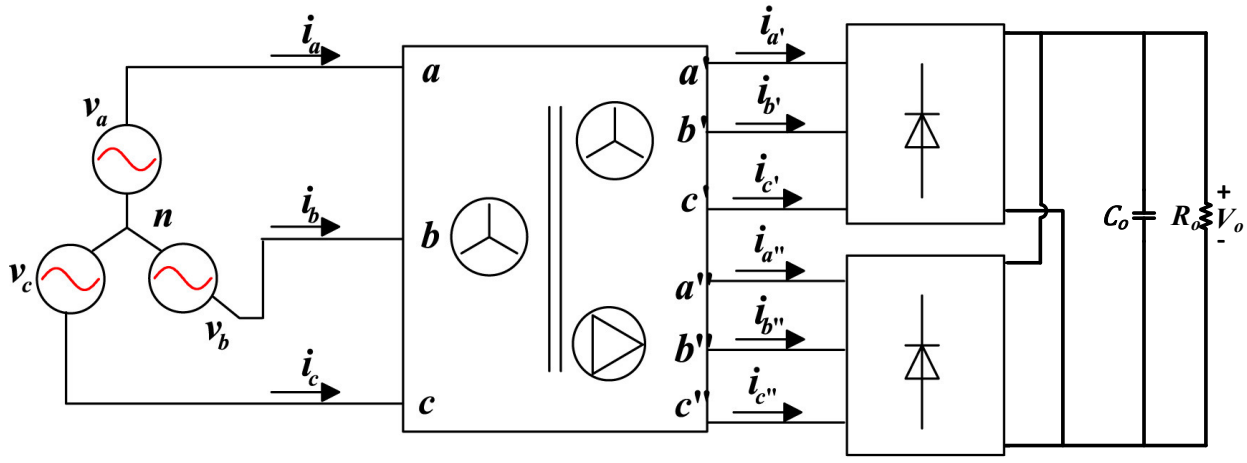


Fig. 1.6. The schematic of conventional 12-pulse TRU.

isolated phase-shifting interphase auto-transformer whereas the TRU employs the isolated three-winding transformer at AC mains with secondary and tertiary windings are connected in wye and delta configuration, respectively. The phase shifting through the transformer arrangement suppresses the 5th and 7th harmonics in the input current, which are generally present in 6-pulse diode rectifiers. As a result, the input current appears almost like sinusoidal; however, it still contains the lower order 11th, 13th, 23rd, 25th harmonics of high amplitudes [19].

The drawback of passive ATRU and TRUs is that they are heavy and bulky, occupy larger space due to the employment of supply frequency 350 Hz transformers. In addition, the output DC bus voltage is not regulated and varies with the load and supply voltage as illustrated in Fig. 1.7 [20]. The output voltage is high at no load and it is low for supply frequency 800 Hz at full load. Therefore, this voltage variation must be accommodated in the design of supplied pulse-width-modulated (PWM) converter or electric machines. At present, the diode rectifiers are just meeting the harmonic levels imposed by the standards DO-160G, and MILSTD704F. In future, more stringent harmonic limits are expected to be into force [13]. In that case, 12-pulse ATRU or TRUs cannot meet the future total harmonic distortion (THD) stringent limits and so either 18-pulse [21], [22] or 24-pulse [23] passive ATRU or TRUs should be employed. Though, the higher pulse passive rectifiers are feasible, it is worth to mention that they are still using the supply frequency 350 Hz transformers in addition to a complicated transformer winding structure comprising weight and density. Therefore, the alternative feasible solution is the active power conversion.

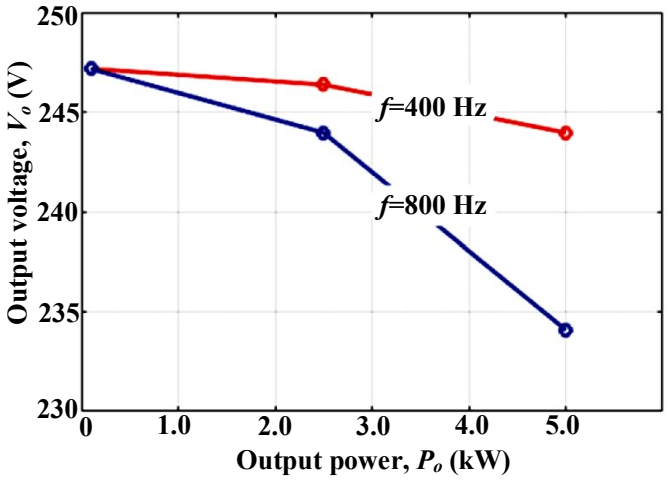


Fig. 1.7. Output voltage versus output power of 12-pulse ATRU for supply frequencies 400 Hz, 800 Hz for input rms voltage 115 V.

1.1.1.2 Active AC-DC converters

Table 1.2 provides the comparison of the active rectification with the passive rectification in MEA. The active power converters employ semiconductor switching devices generally operating at higher switching frequency in order to reduce the size of passive components, subsequently it reduces the total weight of the system. The active control rectification gives stiff regulated DC output voltage with superior input power quality. Hence, the active power converters are the good alternatives to the passive power converters. A comparative study of the passive converters and the active converters [20], [24] also revealed that the active converters show the great potential for the future aircrafts due to their higher power density, better input power quality and stiff regulated DC bus voltage. This is mainly due to the rapid progress in the semiconductor materials such as wide-band-gap semiconductors SiC and GaN. The high operating frequency capability of wide-band-gap semiconductors will significantly reduce the volume and weight of the passive components and subsequently increases the system power density. Therefore, the present focus is on active PWM converters.

The vital constituent in active AC-DC power conversion is the power factor correction (PFC). In literature, several active AC-DC PFC converters are reported for improving the power quality. Their detailed review is presented in [25]-[29]. According to Fig. 1.4, the active PFC converters are either phase-modular converters or direct three-phase converters, and each of them can be configured as buck-type, boost-type, and buck-boost type topology. Each topology can either be operated in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), which

Table 1.2: The comparison of active rectification and passive rectification.

Active rectification	**Passive rectification**
Uses semiconductor switching devices and require control circuitry.	Uses diode-based rectifiers. Simple and reliable.
Power density is high due to the reduced size of passive components.	Power density is less due to the heavy and bulky supply frequency 350 Hz transformers.
High frequency transformer isolation.	Low frequency transformer isolation.
Provides controllable power factor.	No control over power factor.
Low input current THD because of switching scheme.	High input current THD, require multi-pulse auto transformer to meet THD requirements.
Active damping	No active damping

is mainly discriminated by the inductor current continuity in the converter. In MEA, since the DC-link voltage is greater than the peak input AC voltage, either boost or buck-boost type converters are the suitable choice for the AC-DC rectification. Therefore, in literature survey, only the boost and buck-boost type AC-DC converters are considered.

The three-phase two-level six-switch boost converter, and the three-level six-switch Vienna boost converter are the traditional topologies and has been widely discussed in literature [30]-[33]. In [34], a three-phase delta-switch boost converter with an optimal current control modulation concept for MEA is presented. In [35]-[38], the three-phase buck-boost type converters with high input current quality are reported. The converters proposed and studied in [30]-[38] are operated in CCM, and either DQ-domain-vector control or direct-linear-phase control technique has been employed for fulfilling the PFC control objectives. The PFC control objectives are as follows

1) sinusoidal input current in-phase with input voltage for all supply frequencies
2) stiff regulated DC output voltage.

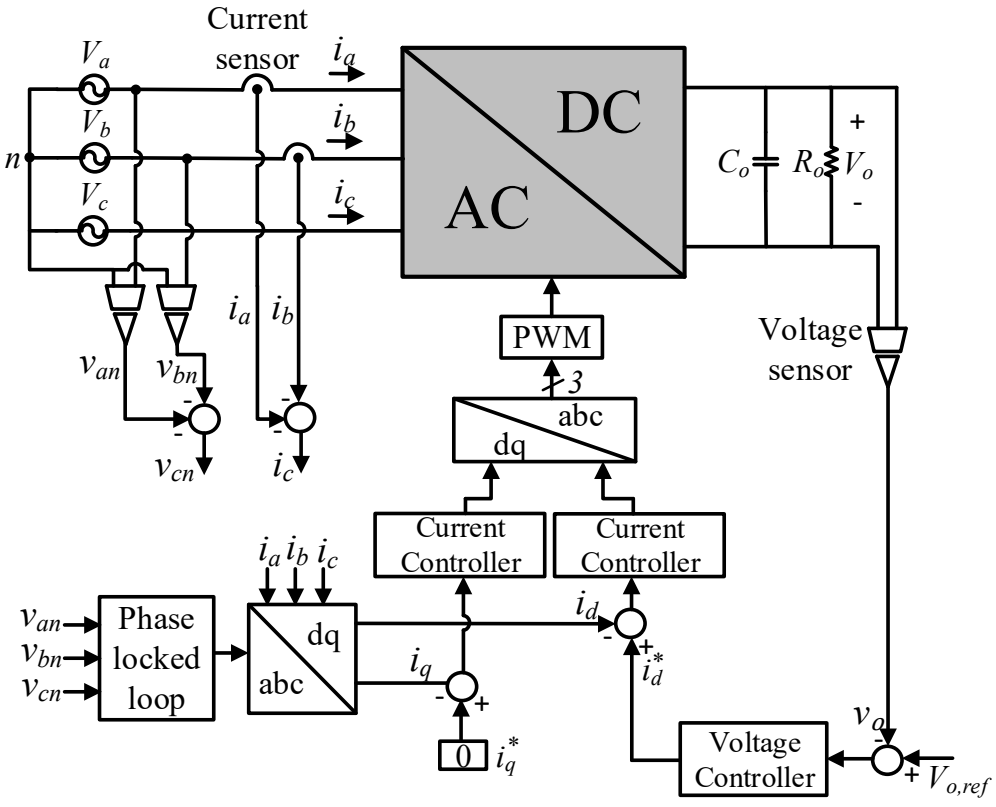


Fig. 1.8. DQ-domain-vector control block diagram for three-phase CCM converters.

The control block diagrams of DQ-domain-vector control and the direct-linear-phase control are shown in Fig. 1.8 and Fig. 1.9, respectively. Both the control techniques require two control loops; the outer loop is to regulate the output voltage and the inner loop is to shape the input current by maintaining the unity power factor (UPF) operation. The DQ-domain-vector control requires phase-locked-loop (PLL) to generate the phase angle required for abc-to-dq transformation. The MEA variable frequency operation makes the design of PLL complex, and also the inner current loop controllers must be designed for a higher bandwidth. On the other hand, the direct-linear-phase control further require very high bandwidth for the inner current controllers than the DQ-domain-vector control to track the sinusoidal reference currents, which in turn require a high switching frequency operation to ensure a stable operation.

According to Fig. 1.8 and Fig. 1.9, both the DQ-domain-vector control and the direct-linear-phase control require at least five sensors (two input voltages, two input currents, one output voltage) for the PFC control implementation. Reducing the sensors count, adds several benefits [39], [40] such as

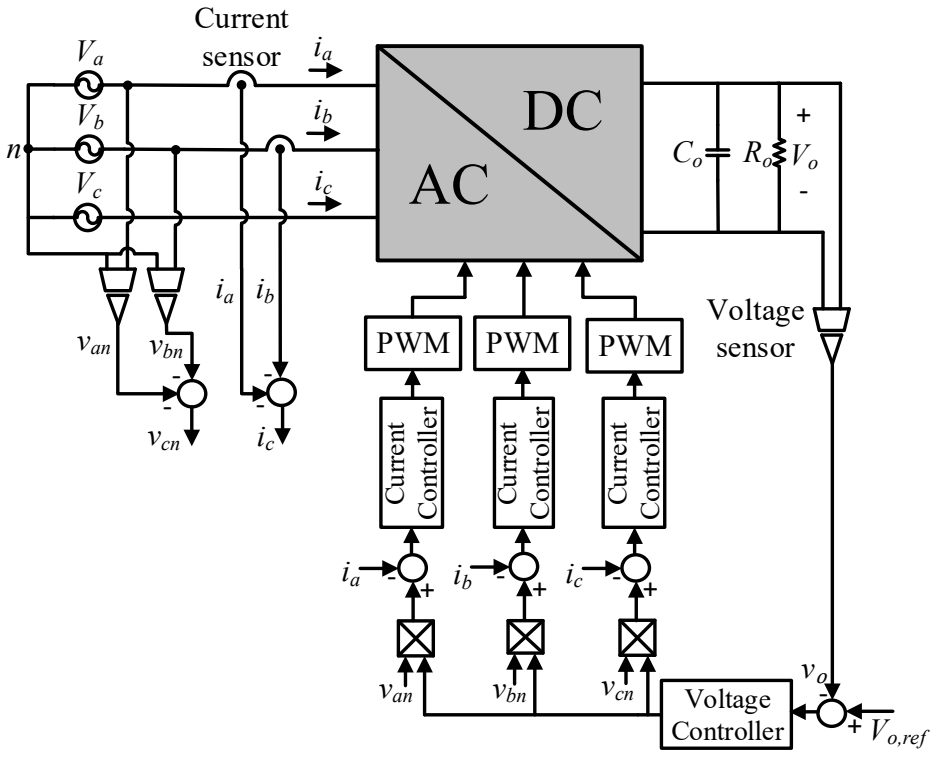


Fig. 1.9. Direct-linear-phase control block diagram for three-phase CCM converters.

1) Reduction in cost
2) Robustness to high frequency noise
3) Improvement in system reliability
4) Reduction of system weight
5) Slight improvement in efficiency by eliminating the sensor losses
6) Reduction in control complexity and simplicity of control implementation.

For reducing the number of sensors, several different algorithms [41]-[46] are reported in the literature for estimating the input currents and voltages from the DC-link current or the DC-link voltages, and by using the information of PWM switching states in the current sample and the phase duty cycles from the previous current samples. The reconstructed phase currents involve one cycle delay in the control loop that leads to system instability at the digital control platform during transient operations. Further, these control algorithms are too complex and involve lot of mathematical equations, which increase the control complexity and makes them difficult for practical implementation. Also, these algorithms work only for the balanced systems.

In a converter, the number of sensors by default can be reduced by operating it in DCM. In DCM, the average value of the input current in a switching cycle is determined by the input voltage at that instant, therefore the average input current naturally follows the input voltage, which means the DCM operation inherently fulfills the PFC, the first control objective. The second objective of PFC control can be achieved by using a single voltage control loop depicted in Fig. 1.10. To

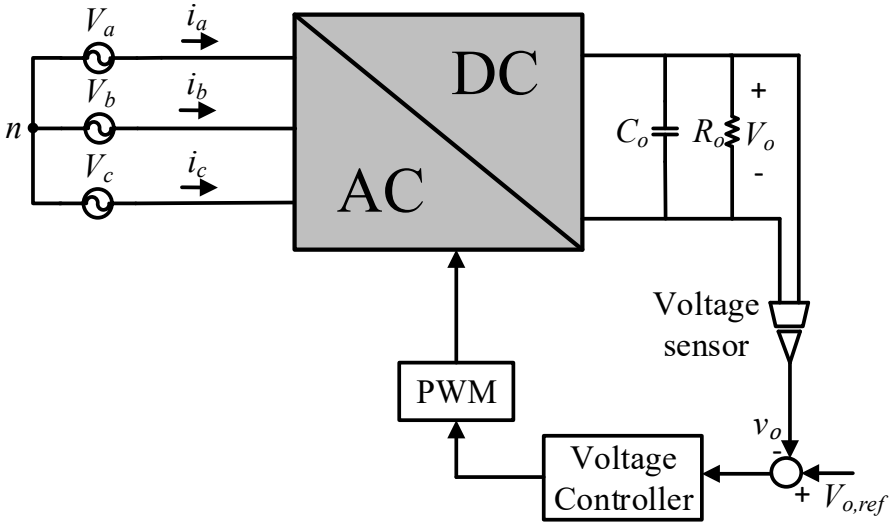


Fig. 1.10. Control block diagram of a converter operating in DCM.

conclude, the DCM operation by default eliminates requirement of the input voltage and input current sensing and therefore, only one output voltage sensor is required. Further the DCM operation inherently realizes the zero-current switching (ZCS) of the converter switches and the zero reverse recovery losses in the converter diodes [47]. Since a small inductor is required for converter DCM operation, it reduces the converter total weight and improves power density. But, the drawback of DCM operation is the high current stress of the semiconductor devices, however the higher current rating semiconductor devices are commercially available at reasonable price. Therefore, by considering all the benefits of DCM, the DCM operated converters are considered in this research work.

In [48]-[50], a three-phase DCM boost converter with single-switch formed by combining a three-phase six-pulse diode-bridge rectifier and the DC boost chopper circuit is proposed and is shown in Fig. 1.11. The three-phase boost converters with two-switch [51]-[53] and three-switch [54]-[56] topologies operated in DCM are shown in Fig. 1.12 and Fig. 1.13, respectively. These are simple circuits, but due to the boost nature, these converters [48]-[56] exhibit a relatively higher fifth order harmonic in the input current for lower voltage gains [57], [58]. Fig. 1.14(a) depicts the simulated input current of DCM boost PFC converter and Fig. 1.14(b) depicts its frequency spectrum. A converter voltage gain of 3X is considered for the simulation. The simulated input current is not pure sinusoidal and is having a flat dip at sinusoidal peak, which is mainly due to the presence of higher amplitude fifth and seventh harmonic in input current. As a consequence, the DCM boost converters require a large filter at the input side to filter out this lower order harmonics, which in turn reduces the power density of the system. Several methodologies are proposed for improving the input current quality in DCM boost converter [59]-[61] by reducing the lower order harmonic content. However, these approaches require extra sensing [62], and the reduction in total harmonic content is not very significant. Therefore, the DCM boost topologies are not the feasible option for MEA application.

On the other hand, the buck-boost type (flyback, SEPIC, Cuk) circuits [63]-[68] operating in DCM are the perfect PFC regulators, and do not contain any lower order harmonics in the input current. Fig. 1.15(a) depicts the simulated input current of DCM buck-boost PFC converter for voltage gain of 3X and Fig. 1.15(b) depicts its frequency spectrum. The input current is perfectly sinusoidal and no lower order harmonics are present. The input current contains only higher

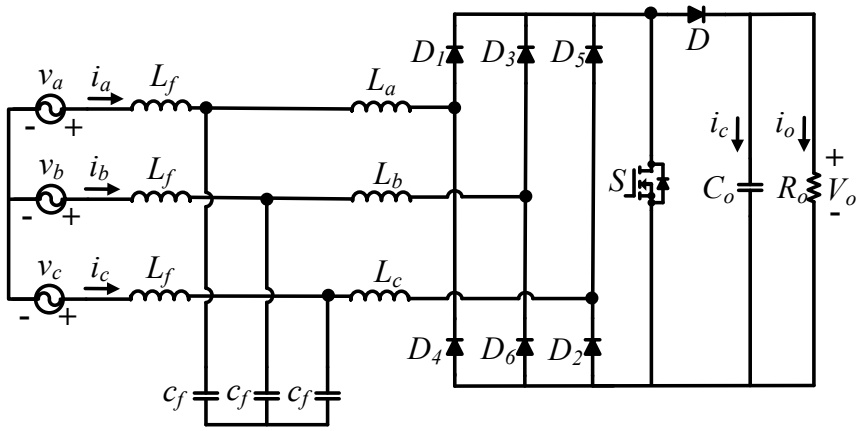


Fig. 1.11. Single-switch DCM boost PFC converter.

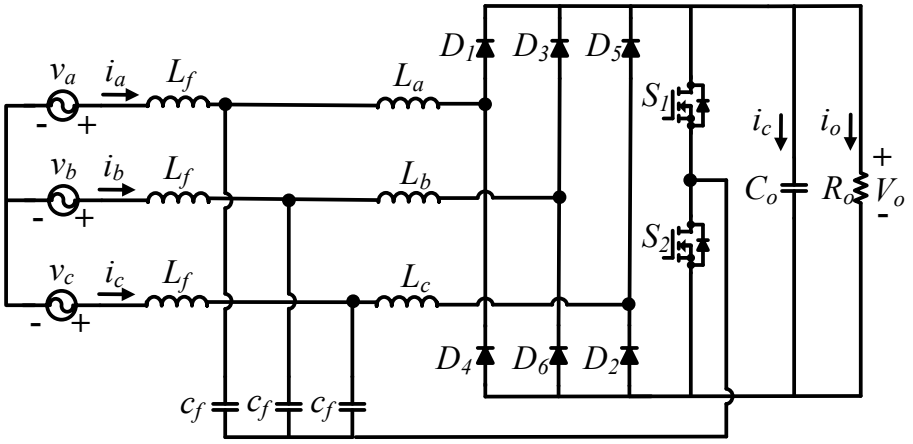


Fig. 1.12. Two-switch DCM boost PFC converter.

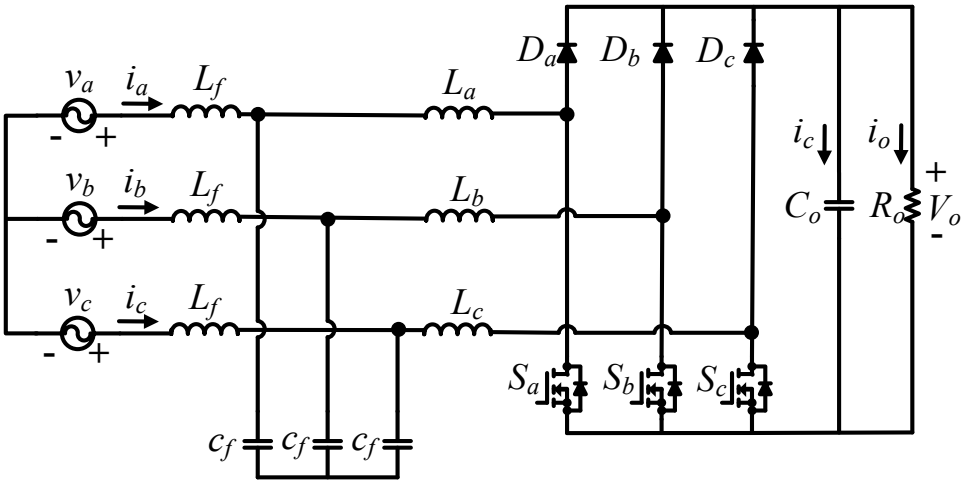


Fig. 1.13. Three-switch semi-controlled DCM boost PFC converter.

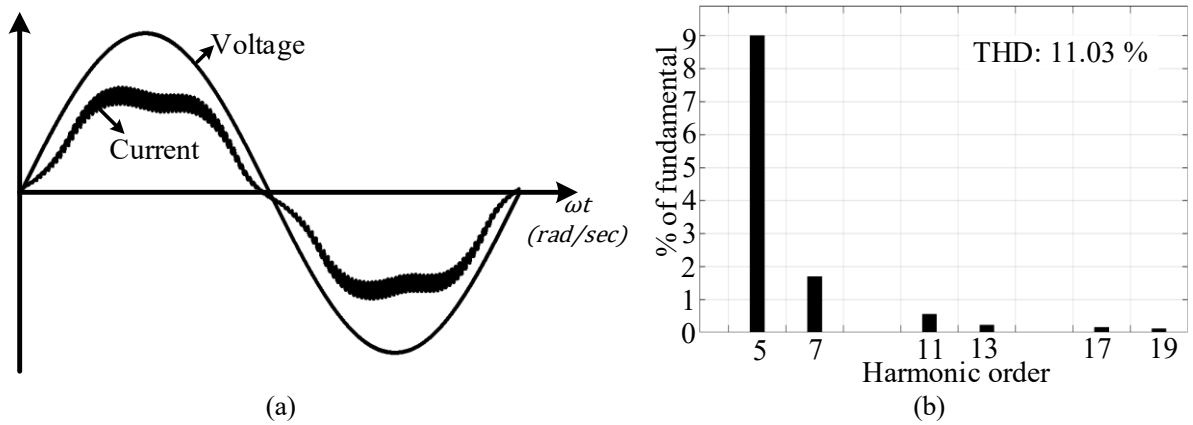


Fig. 1.14. Three-phase DCM boost converter (a) simulated input voltage and current; (b) current frequency spectrum.

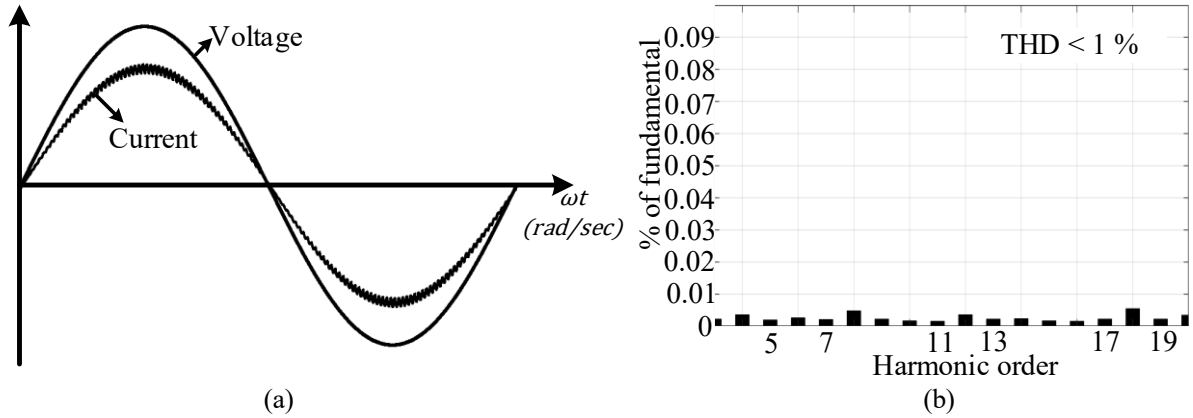


Fig. 1.15. Three-phase DCM buck-boost converter (a) simulated input voltage and current; (b) current frequency spectrum.

switching order harmonics, hence a small input filter is sufficient to filter out these higher order switching harmonics. Therefore, considering the advantages of the DCM operation and the buck-boost type converters, this thesis explores some three-phase buck-boost type PFC topologies (both isolated and non-isolated) operating in DCM.

1.1.1.3 Requirements for AC-DC converters

The AC-DC converters connected to the MEA mains should satisfy the following requirements according to the airborne standards [14], [15].

- The converter power flow should be unidirectional from AC-mains to the DC bus due to the absence of energy storage elements at AC side in MEA.

- The converter should be able to handle an input voltage unbalance upto 10%.
- The converter should be able to operate safely and should provide degraded power operation in case of one or more phases loss.
- The converter input current harmonics must fulfill the upper bounds defined in Table 1.3. In addition, the converter must comply with the high frequency conducted emissions defined in the airborne standards.
- The converter power factor must be maintained between 0.85 lagging and unity for power levels greater than 50% of the rated output power.
- The converter should provide regulated DC either 270 V (Airbus A380) or 540 V (Boeing 787).

Table 1.3: Input current harmonic limits according to airborne standard DO-160G [14].

Harmonic order	**Limits**
3rd, 5th, 7th	0.02 I_1
Odd triplen harmonics (h= 9th, 15th, 21st, 27th, ---39th)	0.1 I_1/h
Odd non-triplen harmonics 11th, 13th, 23rd, 25th	0.03 I_1
Odd non-triplen harmonics 17th, 19th	0.04 I_1
Odd non-triplen harmonics 29th, 31st, 35th, 37th	0.3 I_1/h
Even harmonics 2nd, 4th	0.01 I_1/h
Even harmonics > 4; 6th, 8th, 10th------40th	0.0025 I_1

where I_1 is the magnitude of fundamental component

Table 1.4: The requirements of AC-DC converters connected to the AC mains of MEA.

Description	**Value**
Input line voltage	110 V $\pm$ 10 %
Output voltage	270 V
Input supply frequency	360 to 800 Hz
Power factor	> 0.95 lagging
Input current quality	THD < 5 %; Individual harmonic according to Table 1.3
Efficiency	> 90% at rated output power
Output power with single-phase loss	$\geq$ 50 % of rated output power

The airborne standards defined the upper bounds on current harmonics considering the passive 12-pulse rectifier systems, so that the characteristic harmonics at (h.12 ± 1) can be applied, where h is the harmonic order number. In general, every aircraft company creates their own standard with partly more stringent limits than the specified in Table 1.3, e.g., the Boeing defined more stringent harmonic limits for the 11^{th} and 13^{th} harmonics [13]. Therefore, with a consideration of future stringent harmonic limits for the next generation MEA's, the active AC-DC PFC converters proposed and studied in this work are designed with an objective of strictly satisfying the requirements specified in Table 1.4.

1.3 Research objectives and proposal

The fundamental objective of this thesis is to propose new active AC-DC PFC solutions (both non-isolated and isolated) to replace the currently used passive multi-pulse ATRU and TRUs with fulfilling all the electrical requirements of MEA listed in Table 1.4. In particular, the active AC-DC buck-boost type PFC converters are studied and analyzed with a focus on minimizing the total number of components, improving power quality, and improving the overall operating efficiency and density. The proposed converters are designed for the DCM operation in order to simplify the control circuit and to reduce the number of sensors which consequently increases the converter reliability, and robustness. Further, the converters design and performance are tested for supply frequency change, load perturbations, and single-phase loss operation.

The objectives of this thesis are:

1) Proposal of AC-DC converters with simplified control and easy implementation
2) Operation with reduced number of sensors
3) Higher reliability
4) Improved power quality (THD < 5%)
5) Improved efficiency (> 90 %)
6) UPF operation for wide range of supply frequency (360 to 800 Hz)
7) Simplified operation and practical implementation.

To accomplish these objectives, and to replace the conventional diode-based rectifier with active PFC rectification, the thesis proposes a number of active PFC converter topologies described briefly in thesis outline next section 1.4, and in detail in various Chapters 2 to 6.

1.4 Thesis outline

The contents of the thesis in various Chapters are organized as follow:

In Chapter 2, a three-phase modular single-stage isolated Cuk-based PFC converter with output inductors operating in DCM is reported. The steady-state operation, design, DCM condition, small-signal model, and the closed-loop controller design have been reported. The effect of transformer leakage inductance on the converter operation has been studied. A passive resistor-capacitor-diode (RCD) clamping circuit design to clamp the surge voltage caused by the transformer leakage inductance has been provided in detail. The analysis and design are validated with the simulation results from PSIM 11.1 software, and further verified with the experimental results from a 2.0 kW hardware prototype developed in the lab.

In Chapter 3, a new direct three-phase non-isolated Cuk-derived PFC converter operating with reduced number of components is studied. The converter is operated in DCM to achieve the unity power factor (UPF) operation for wide range of supply frequency. The steady-state operation, design, DCM condition, small-signal model, and closed-loop controller design have been presented in detail. The analytical voltage and current stress expressions for each component are derived and verified with simulation. The performance and the analysis have been validated with the simulation results from PSIM 11.1 software, and further verified with the experimental results from a 2.0 kW hardware prototype developed in the lab.

In Chapter 4, an improved direct three-phase non-isolated PFC converter derived from buck-boost topology has been proposed and analyzed. The output inductors are designed for DCM operation in order to achieve UPF operation at AC mains for wide range of frequency. The steady-state operation, design, DCM condition, small-signal model, and closed-loop controller design have been presented in detail. The operation and performance of the converter are demonstrated with the simulation results from PSIM 11.1 software, and the experimental results from a 2.0 kW laboratory prototype.

In Chapter 5, an interleaved topology of the three-phase buck-boost derived PFC converter is studied and analyzed. The input filter size is reduced by half with the proposed interleaved topology and the control. The advantages of the interleaved converter when compared with the

single-cell converter in terms of power density, efficiency, and reliability are demonstrated analytically and confirmed with both the simulation and experimental results.

In Chapter 6, an isolated topology of the three-phase buck-boost derived PFC converter with a novel clamping circuit to capture and utilize the transformers' leakage inductance energy in order to improve the overall efficiency is proposed and analyzed. The steady-state design equations, and the small-signal model along with closed-loop controller design have been presented in detail. The simulation results, and the experimental results from a 1.0 kW laboratory are presented in order to validate the converter analysis and the design and demonstrated the performance.

In Chapter 7, the contributions of the thesis are summarized, and guidelines for the future work are presented.

1.5 Conclusion

This Chapter discussed the short-term and long-term goals of the future aircrafts and presented the power system architectures of conventional and more electric aircrafts. In MEA, the constant speed heavy mechanical gearbox IDG is eliminated and the generator is coupled directly to the main engine, which resulted in variable frequency mains of 360 to 800 Hz. The MEA adopted 270 V DC bus system in order to reduce the size and weight of the cables that created a requirement for the power electronic AC-DC converters to convert the variable frequency AC supply to constant DC voltage.

The comprehensive review of the currently used diode-based AC-DC converters and their limitations to meet the power density requirements of the next generation MEAs have been discussed. The advantages of active rectification system over the diode-based rectification has been explained. The literature study of active AC-DC PFC converters revealed that the CCM operated converters require at least five sensors and two control loops whereas the DCM operated converters require only one sensor and one control loop to fulfill the PFC control objectives. The reduction in number of sensors has several merits such as reduction in converter cost, reduction in control complexity and implementation, increased reliability, increased robustness to high frequency noise, and improved system power density. In view of the benefits of the DCM operation, and considering the advantages of DCM buck-boost converters over the DCM boost converters, the fundamental objective of this thesis is to study, analyze and develop a number of

three-phase DCM buck-boost type PFC topologies (isolated and non-isolated), and to contribute the power electronic AC-DC solutions.

Chapter 2 : Three-Phase Modular Single-Stage Isolated Cuk-based PFC Converter

2.1 Introduction

Typically, in three-phase converters, the PFC with isolation is implemented using a two-stage conversion. In two-stage conversion, a three-phase ac-dc non-isolated active PFC converter is employed at first stage followed by an isolated dc-dc converter at second stage [69]-[72]. The front-end active PFC converter provides sinusoidal input currents with unity power factor and low THD. The second stage DC-DC converter provides isolation and regulated output voltage according to the load requirements. This is the simplest approach, but the total power has to be processed two times, which leads to higher losses and low efficiency. In addition, the two-stage conversion requires more number of semiconductors and a bulky DC-link electrolytic capacitor, which increases the system weight and compromises the system reliability [56]. Therefore, it is not a viable option for aircraft application. The alternate option is the single stage approach, where the power is processed only one time. The PFC and isolation stages are combined to have direct power conversion. As a single-conversion stage, it is expected to have less number of components, higher power density and reliability. But the single stage approach requires three transformers in contradictory to one transformer in two stage approach. Further, the power transferred over each transformer pulsates at twice the main frequency which leads to poor utilization of core and windings and increases the converter overall volume. This disadvantage of single stage approach can be lessened by some with design of individual transformers on a single three-phase transformer core. The single-stage high-frequency (HF) transformer isolation can be implemented easily with buck-boost type converters such as Cuk converter. The Cuk topology comprises the boost structure at input, and the buck structure at output. Thus, it has the benefits of both the boost and the buck topologies such as inherent inrush current limitation during start-up and overload conditions, no additional input filter, and a small output capacitor filter. Hence, the Cuk isolated topology is selected to implement the single-stage AC-DC PFC rectification.

The three-phase AC-DC PFC rectifier systems are either phase-modular systems or direct-three-phase rectifier systems. The phase-modular systems comprise three autonomous single-phase rectifiers, and each of them is connected to individual phase and neutral of the three-phase system

to form either wye (Y) or delta (Δ) configuration to deliver the required amount of power. In phase-modular systems, each phase-operation is independent, and the system can deliver the power even if two-phases are failed. Further, the system repair and maintenance are easy in case of a single-module failure, and can bring the system into full operation by just replacing the faulty module. Therefore, considering the merits of the phase-modular system, and the Cuk topology, a three-phase modular single-stage isolated PFC converter Cuk rectifier is studied and analyzed in this Chapter.

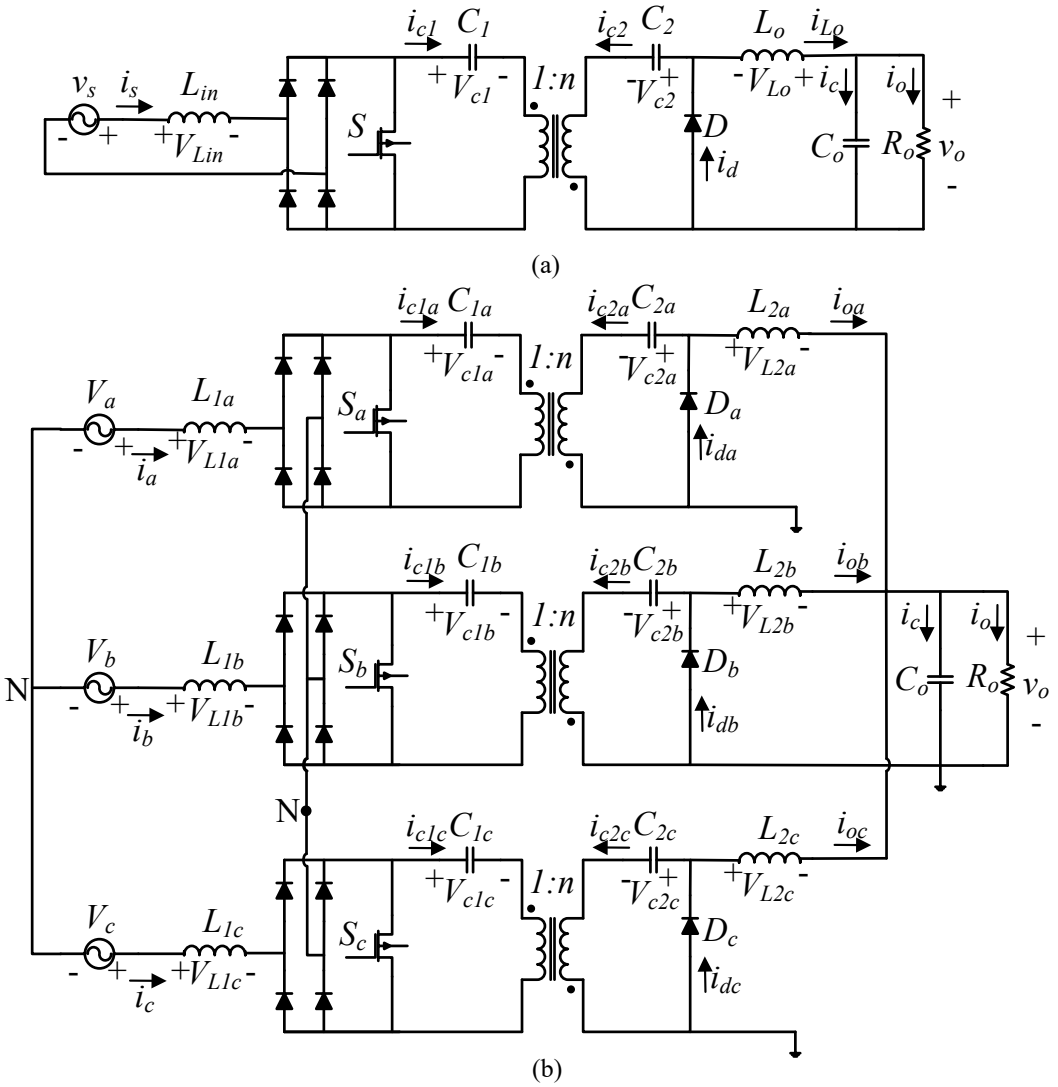


Fig. 2.1. a) Single-phase isolated Cuk PFC converter; (b) proposed structure of the three-phase modular single-stage isolated Cuk converter.

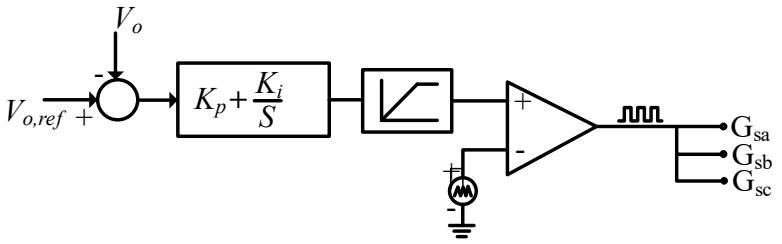


Fig. 2.2. Gate drive control circuit.

2.2 Proposed converter

The single-phase isolated Cuk converter is shown in Fig. 2.1(a). The proposed converter Fig. 2.1(b) is derived by combining three single-phase circuits into a three-phase three-wire system with output ports connected in parallel. The second leg midpoints of the single-phase diode bridge rectifiers are connected together to form neutral. The proposed converter is operated in DCM to achieve PFC. In Cuk converter, the DCM operation is broadly classified as a) discontinuous inductor current mode (DICM) b) discontinuous capacitor voltage mode (DCVM). The DICM is more suitable for high-voltage-low-current applications whereas the DCVM is a dual form of DCIM suitable for low-voltage-high-current applications. The DICM operation can further be classified into discontinuous input inductor current mode (DIICM) and discontinuous output inductor current mode (DOICM). In DIICM, the input inductor current is discontinuous, so it requires an additional input filter to filter out the HF components of input current. In DOICM, the output inductor current is discontinuous, and the input inductor itself acts as input filter, hence DOICM operation does not require an additional input filter. By considering these merits of DOICM, the proposed converter is studied and analyzed in DOICM operation.

The discontinuous current in the output inductor is defined by the current discontinuity in the output diode. Therefore, to achieve the DCM in all three-phases, it is required to ensure current discontinuity in all the three output diodes. Once this is ensured, the converter emulates a resistor behavior at AC mains and provides a sinusoidal input current in-phase with the input voltage. Subsequently, it eliminates the inner current loop and requires only one simple voltage control loop to regulate the system output voltage. Also, all the three power switches S_a, S_b, and S_c of the proposed converter are driven by the common gating signal as shown in Fig. 2.2. From Fig. 2.2, it is clear that the on-time of the switch depends only on the error between the reference output

voltage and measured output voltage. Thus, the duty cycle of the converter is constant, and it does not vary with sinusoidal change in the input voltage. However, duty cycle adjusts only if there is a change in the output voltage reference or in case of any disturbances viz. load change or variation in source voltage amplitude, etc.

2.3 Steady state operation of the converter for one switching cycle

The following assumptions are made to analyze the converter:

a. In order to ensure DCM in the output inductor, the output inductor should be smaller than the input inductor as given in (2.1).
b. The voltage across each input Cuk capacitor is constant during a HF switching cycle and equal to the respective rectified input phase voltage as expressed in (2.2).
c. The voltage across each output Cuk capacitor is constant and equal to the output voltage as expressed in (2.3).
d. As defined in (2.4), all the parameter values are same to maintain the circuit symmetry.

$$L_{2a} \ll L_{1a};\ L_{2b} \ll L_{1b};\ L_{2c} \ll L_{1c} \tag{2.1}$$

$$v_{c1a} = |v_a|;\ v_{c1b} = |v_b|;\ v_{c1c} = |v_c| \tag{2.2}$$

$$v_{c2a} = v_{c2b} = v_{c2c} = v_o \tag{2.3}$$

$$\begin{cases} L_{1a} = L_{1b} = L_{1c} = L_1 \\ L_{2a} = L_{2b} = L_{2c} = L_2 \\ C_{1a} = C_{1b} = C_{1c} = C_1 \\ C_{2a} = C_{2b} = C_{2c} = C_2. \end{cases} \tag{2.4}$$

In order to simplify the mathematical analysis, the output stage is referred to the primary side of the transformer and the resulting topology is shown in Fig. 2.5(a). The transformer magnetizing inductance is considered very large since the transformer action is instantaneous, i.e., it does not store any energy. The capacitances C_1 and C_2 are replaced by its equivalent capacitance C_{int}, which

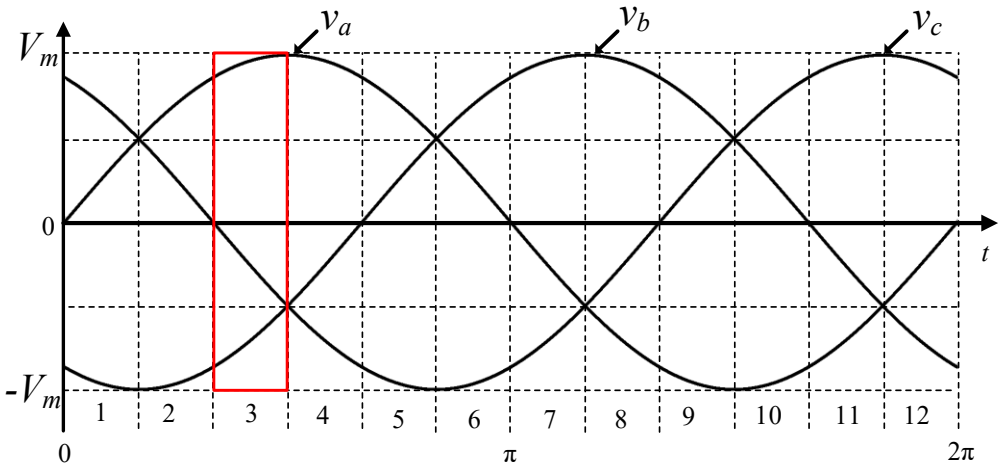


Fig. 2.3. The three-phase input voltages.

is given by (2.5) with a voltage $|v_k| + {}^{v_o}/_{n}$ across it, where k = a, b, c. To further simplify, the output connections are removed which is valid as long as the relation (2.6) is maintained.

$$C_{int} = \frac{C_1 C_2'}{C_1 + C_2'} \tag{2.5}$$

$$i_{oa}' + i_{ob}' + i_{oc}' = n i_o. \tag{2.6}$$

where, the parameters with ‘’ represents the quantities referred to primary side viz. $C_2' = n^2 c_2$.

The three-phase sinusoidal signals are divided into 12 sectors of each 30^0 as shown in Fig. 2.3. In each sector, the converter behavior is similar because of the symmetric structure of the circuit and thus, analysis has been presented only for sector-3. For instance, in sector-3, the three-phase voltages are expressed as follows:

$$\begin{cases} v_a > 0, v_b < 0, v_c < 0 \\ |v_a| > |v_b| > |v_c|. \end{cases} \tag{2.7}$$

The current wave forms of input, output inductors and output diode in one-line cycle are shown in Fig. 2.4(a). To proceed with the analysis, the same current waveforms for four switching cycles in sector-3 are shown in Fig. 2.4(b). It should be noted that the converter has five modes of operation in a switching cycle.

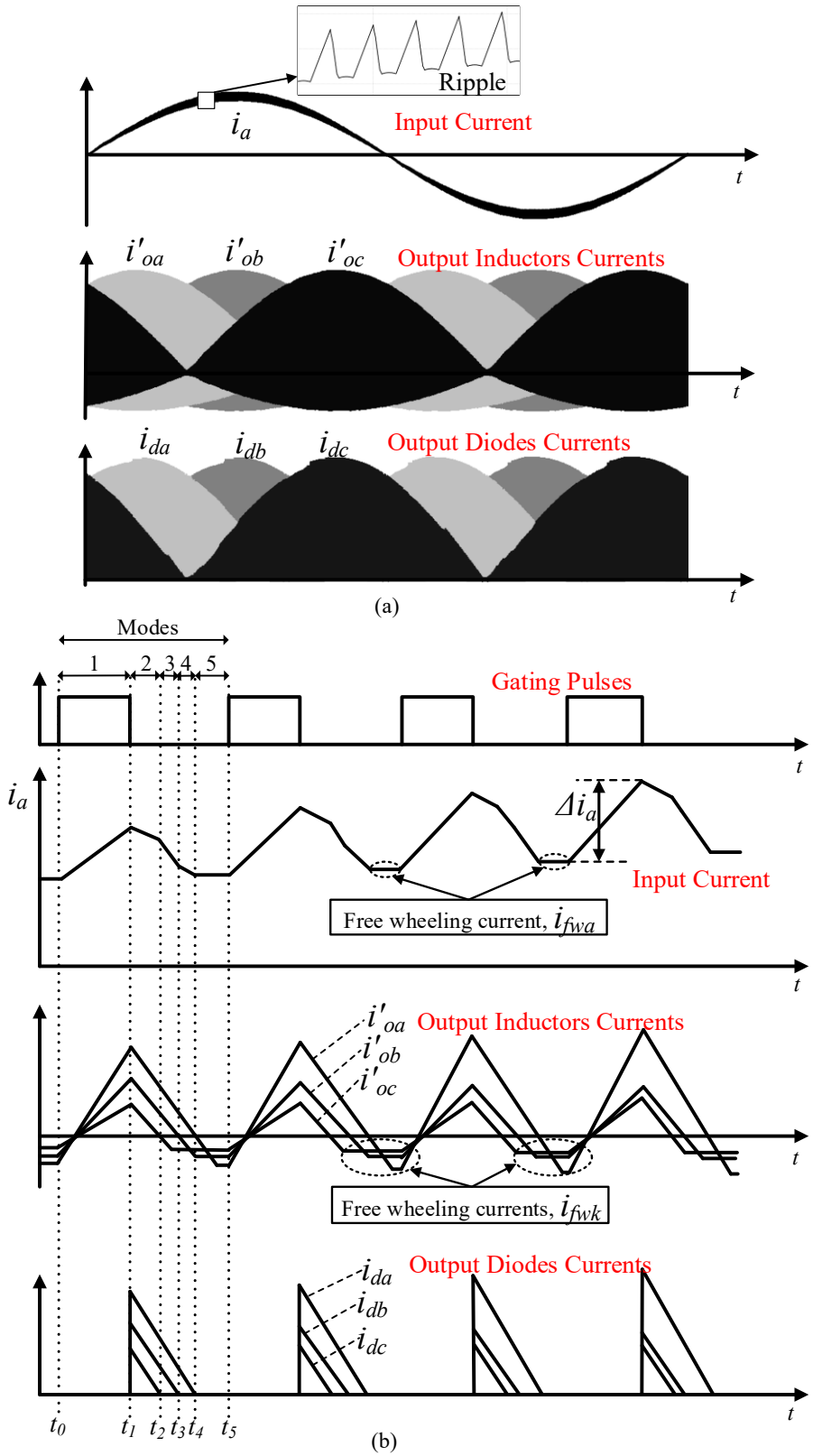


Fig. 2.4. Input current of one phase, output inductors and output diodes current waveforms, (a) for one cycle; (b) for four switching cycles in sector-3.

Mode-1 (t_0 - t_1): This mode starts when all the three power switches are conducting, the equivalent circuit is shown in Fig. 2.5(b). Prior to this mode, the input currents are freewheeling in the converter and represented as i_{fwk} in Fig. 2.4(b). Its sign is positive for the input currents because freewheeling currents are in the same direction of input currents whereas its sign is negative for output currents because they flow in the opposite direction of output currents. When all the switches are conducting, the input and output inductors store energy at a rate proportional to the instantaneous values of their respective phase voltages. The output filter capacitor supplies the power to the output. The inductor currents are expressed as

$$i_k = i_{fwk} + \frac{v_k}{L_1} t \tag{2.8}$$

$$i'_{ok} = -i_{fwk} + \frac{|v_k|}{L'_2} t \tag{2.9}$$

where, $L'_2 = \frac{L_2}{n^2}$.

Mode-2 (t_1 - t_2): This mode starts when the gate signals are zero. In this mode, all the three power switches are turned-off and all the three output diodes start conducting. The equivalent circuit is shown in Fig. 2.5(c). The input inductor and the source are in series to charge the intermediate capacitors and the output inductors supply the power to the output. The inductor currents are expressed as

$$i_k = i_{fwk} + \frac{v_k}{L_1} dT_s - \frac{v_o}{nL_1} t \tag{2.10}$$

$$i'_{ok} = -i_{fwk} + \frac{|v_k|}{L'_2} dT_s - \frac{v_o}{nL'_2} t. \tag{2.11}$$

From (2.9), it should be observed that the energy stored in the output inductors depends on the magnitude of input phase voltages. In sector-3, the phase-C voltage magnitude is less compared with other two phases. Hence, the energy stored in phase-C output inductor is less and it goes into DCM first. This mode ends when the phase-C output diode current is zero, i.e.

$$i_c = -i'_{oc} = n i_{oc} \tag{2.12}$$

On substituting (2.10), (2.11) in (2.12),

$$t_{dc,on} = d_1 T_s = \frac{|v_c|}{v_o} n d T_s \tag{2.13}$$

Mode-3 (t_2 - t_3): This mode starts once the phase-C output diode current is zero and the equivalent circuit is shown in Fig. 2.5(d). In this mode, (2.10) and (2.11) hold true till phase-B output diode current is zero. This implies

$$i_b = -i'_{ob} = n i_{ob}. \tag{2.14}$$

By solving (2.14)

$$t_{db,on} = d_2 T_s = \frac{|v_b|}{v_o} n d T_s. \tag{2.15}$$

Mode-4 (t_3 - t_4): This mode starts once the phase-B output diode current is zero and the equivalent circuit is shown in Fig. 2.5(e). In this mode, (2.10) and (2.11) hold true till phase-A output diode current is zero. This implies

$$i_a = -i'_{oa} = n i_{oa}. \tag{2.16}$$

By solving (2.16)

$$t_{da,on} = d_3 T_s = \frac{|v_a|}{v_o} n d T_s. \tag{2.17}$$

From (2.13), (2.15) and (2.17), a generalized expression can be derived as follows:

$$t_{dk,on} = \frac{|v_k|}{v_o} n d T_s \tag{2.18}$$

where, *k=a, b, c*.

Mode-5 (t_4 - t_5): This mode starts after the phase-A output diode current is zero and the equivalent circuit is shown in Fig. 2.5(f). In this mode, neither the switches nor the output diodes are in conduction but in blocking mode. Due to the large size of input inductors, the input currents

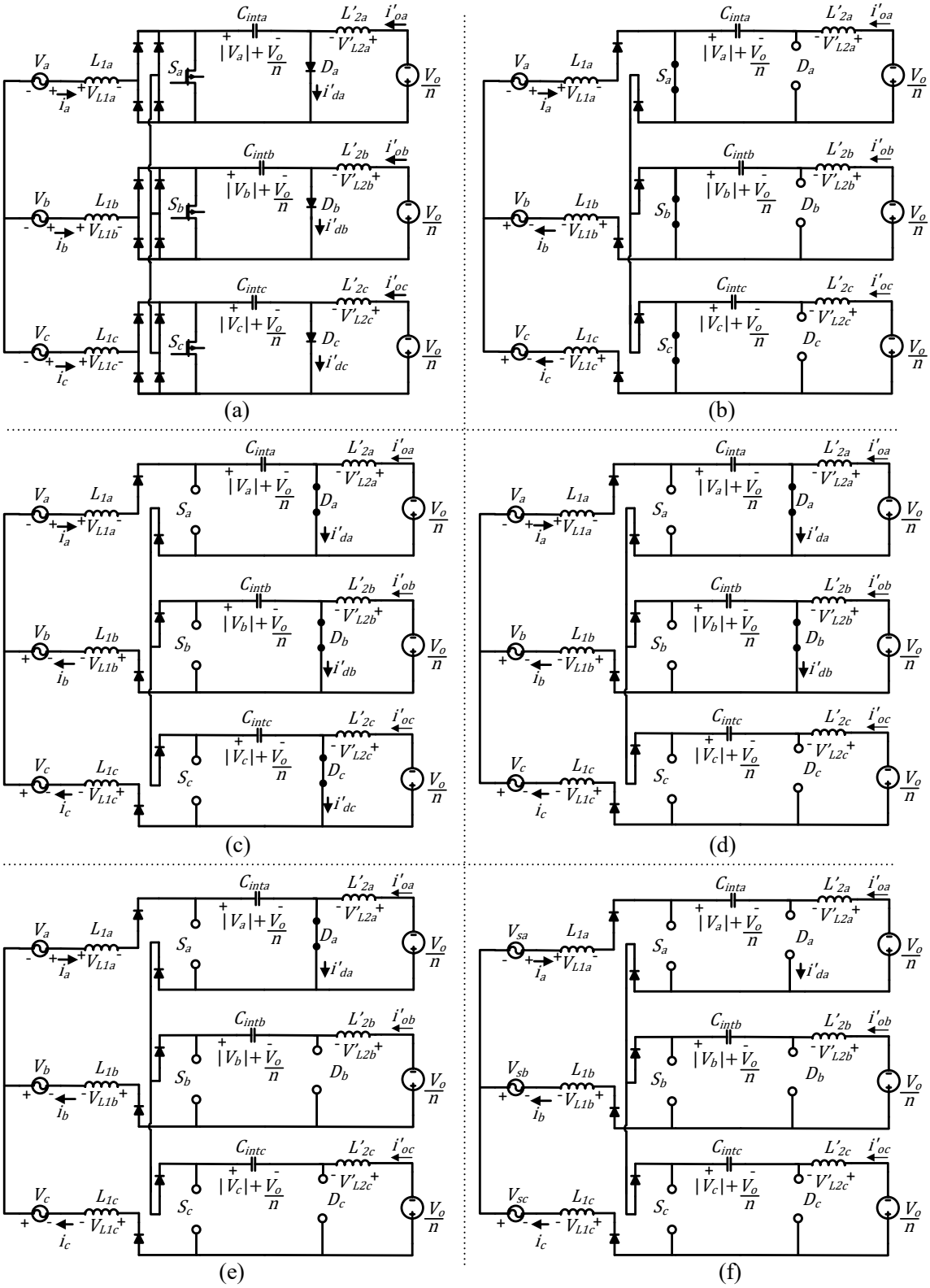


Fig. 2.5. Equivalent circuit of the proposed circuit: (a) referred to primary; (b) mode-1; (c) mode-2; (d) mode-3; (e) mode-4; (f) mode-5.

freewheels as shown in Fig. 2.5(f). These are called freewheeling currents represented as "i_{fwk}" and freewheels till the next gating pulse applied to the switches.

2.4 Converter Design

In this section, the expressions for converter average output current and input current, and the DCM condition are derived. Further, the design equations for each passive component of converter are developed.

2.4.1 Average output current

The average output current of each module is equal to the average output diode current of the corresponding phase i.e.

$$i'_{oa,avg} = i'_{da,avg};\ i'_{ob,avg} = i'_{db,avg};\ i'_{oc,avg} = i'_{dc,avg}. \tag{2.19}$$

The peak value of diode current is given by

$$i'_{dk,pk} = \frac{v_k}{L_{eq}} dT_s \tag{2.20}$$

where

$$L_{eq} = \frac{L_1 L'_2}{L_1 + L'_2}. \tag{2.21}$$

The average value of diode current in a switching period is given by

$$i'_{ok,avg} = i'_{dk,avg} = \frac{i'_{dk,pk}\, t_{dk,on}}{2T_s}. \tag{2.22}$$

On substituting $i'_{ok,avg} = n i_{ok,avg}$ and $i'_{dk,avg} = n i_{dk,avg}$ in (2.22)

$$i_{ok,avg} = i_{dk,avg} = \frac{i'_{dk,pk}\, t_{dk,on}}{2nT_s}. \tag{2.23}$$

From (2.18), (2.20) and (2.23), the following expression is obtained:

$$i_{ok,avg} = i_{dk,avg} = \frac{{v_k}^2 d^2 T_s}{2L_{eq} v_o}. \tag{2.24}$$

Since the average current through the output filter capacitor is zero, the average output current of the converter is the sum of the average output currents of three modules and is given by

$$i_{o,avg} = \frac{d^2 T_s}{2L_{eq} v_o} \sum_{k=a,b,c} {v_k}^2. \tag{2.25}$$

Let $v_a = V_m \sin \omega t$, $v_b = V_m \sin(\omega t - \frac{2\pi}{3})$, $v_c = V_m \sin(\omega t + \frac{2\pi}{3})$ then ${v_a}^2 + {v_b}^2 + {v_c}^2 = \frac{3}{2}$. On substituting in (2.25), the converter average output current in a switching cycle is given as

$$i_{o,avg} = \frac{3{V_m}^2 d^2 T_s}{4L_{eq} v_o}. \tag{2.26}$$

The average output current over a line period is calculated by integration of the switching cycle average output current over sector-3 period

$$I_{o,avg} = \frac{6}{\pi} \int_{\pi/3}^{\pi/2} i_{o,avg} \; d(\omega t) = \frac{3{V_m}^2 d^2 T_s}{4L_{eq} v_o}. \tag{2.27}$$

2.4.2 Input current

In the proposed converter, the three modules can be considered independently for a three-phase balanced system. Assuming the lossless circuit, i.e., 100% efficiency, the input power of each module is equal to the output power of each module. For phase-A module

$$v_a i_a = v_o i_{oa,avg}. \tag{2.28}$$

By using (2.24) in (2.28)

$$v_a i_a = \frac{{v_a}^2 d^2 T_s}{2L_{eq}} \tag{2.29}$$

$$i_a = \frac{v_a d^2 T_s}{2L_{eq}} = \frac{V_m d^2 T_s}{2L_{eq}} \sin \omega t \tag{2.30}$$

$$i_a = I_m \sin \omega t \tag{2.31}$$

where

$$I_m = \frac{V_m d^2 T_s}{2L_{eq}}. \tag{2.32}$$

Since the duty cycle of the converter is constant in DCM (Fig. 2.2), the relation given by (2.31) indicates the UPF operation of the converter and phase-A input current is sinusoidal with peak current given by (2.32). Similarly, this can be shown for the other two-phase input currents. The higher switching order harmonics present in the input currents will be filtered out by the input inductors and result in low input current THD.

2.4.3 DCM condition

For the sector under analysis, if phase-A operates in DCM, the other phases will also operate in DCM as well. The condition to operate phase-A in DCM is

$$t_{on} + t_{da,on} < T_s \tag{2.33}$$

$$d\left(1 + \frac{n}{M} \sin \omega t\right) < 1 \tag{2.34}$$

where $M = \frac{V_o}{V_m}$ and $v_a = V_m \sin \omega t$.

The worst situation occurs when $\omega t = 90^0$. Therefore, to operate in DCM

$$d < \frac{M}{n + M}. \tag{2.35}$$

The average output current is given by

$$I_{o,avg} = \frac{v_o}{R_o}. \tag{2.36}$$

From (2.26) and (2.36)

$$d = \sqrt{\frac{2}{3}}\, M\sqrt{k_a} \tag{2.37}$$

where k_a is the conduction parameter of the converter

$$k_a = \frac{2L_{eq}}{R_o T_s}. \tag{2.38}$$

From (2.35) and (2.37), the critical value of k_a ($k_{a,crit}$) to operate at DCM is found as

$$k_{a,crit} = \frac{3}{2}\,\frac{1}{(n+M)^2}. \tag{2.39}$$

2.4.4 Design of input and output inductor

The design of input inductor L_1 depends on the desired input current ripple. Considering the input current shown in Fig. 2.4, the input current peak-peak ripple (Δi_a) is given by

$$\Delta i_a = \frac{v_a}{L_1} dT_s. \tag{2.40}$$

The current ripple is maximum when the input voltage is at its maximum and is given by

$$\Delta I_a = \frac{V_m}{L_1} dT_s \tag{2.41}$$

$$L_1 = \frac{V_m}{\Delta I_a} dT_s. \tag{2.42}$$

The output inductor L_2' is calculated from (2.21)

$$L_2' = \frac{L_1 L_{eq}}{L_1 - L_{eq}} \tag{2.43}$$

where the value of L_{eq} is obtained from (2.38)

$$L_{eq} = \frac{R_o T_s k_a}{2}. \tag{2.44}$$

2.4.5 Design of Cuk capacitor

The design of the intermediate energy transfer capacitor is critical because its value greatly influence the quality of input current. Its value shall not cause low frequency oscillations with the input and output inductors [73]. The resonant frequency f_{r1} caused by the energy transfer capacitor during DCM stage shall be higher than line frequency f_l and lower than switching frequency f_s. Thus

$$f_l < f_{r1} < f_s \tag{2.45}$$

where

$$f_{r1} = \frac{1}{2\pi\sqrt{C_{int}(L_1 + L_2')}}. \tag{2.46}$$

Let C_1 and C_2' to be equal, and their values are calculated as follows:

$$C_1 = C_2' = 2 \times C_{int} \tag{2.47}$$

On the other hand, there is an additional resonance caused by the energy transfer capacitor C_1 and transformer magnetizing inductance L_M that might cause a problem. As mentioned earlier, the energy transfer capacitor shall not cause low frequency oscillations in the input current. Therefore, the resonant frequency f_{r2} caused by the energy transfer capacitor C_1 and magnetizing inductance L_M during DCM stage shall be higher than the resonant frequency f_{r1} and lower than switching frequency f_s. Thus

$$f_l < f_{r1} < f_{r2} < f_s \tag{2.48}$$

where

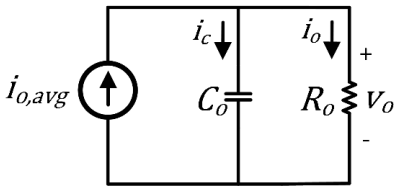


Fig. 2.6. Equivalent circuit of the converter for small-signal modeling.

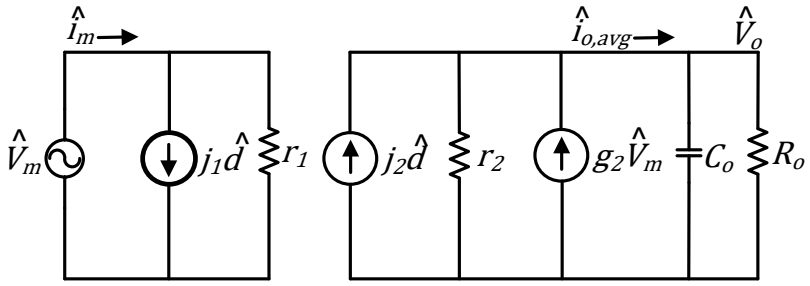


Fig. 2.7. Small-signal model equivalent circuit.

$$f_{r2} = \frac{1}{2\pi\sqrt{C_1 L_M}}. \tag{2.49}$$

2.5 Converter small-signal model

A small-signal model of the converter operating in DCM can easily be obtained by using average current-injected equivalent circuit approach (CIECA) [74], [75]. This approach linearizes the non-linear part of the circuit by injecting the average output current produced by the non-linear part in a switching cycle ($i_{o,avg}$) into the linear part as shown in Fig. 2.6. Since, the average output current is a function of the input voltage, duty cycle and the output voltage, CIECA approach defines the control-to-output transfer properties as well as input and output properties of the converter.

On applying the small signal perturbations (ˆ) to the equations (2.26) and (2.32) around the steady state operating point and making the small signal approximation give

$$\hat{\imath}_{o,avg} = j_2\hat{d} + g_2\hat{v}_m - \frac{1}{r_2}\hat{v}_o \tag{2.50}$$

$$\hat{\imath}_m = j_1\hat{d} + \frac{1}{r_1}\hat{v}_m \tag{2.51}$$

where $j_2 = \frac{3V_m^2}{v_o}\frac{dT_s}{2L_{eq}}$; $g_2 = \frac{3V_m}{v_o}\frac{d^2T_s}{2L_{eq}}$; $r_2 = \frac{v_o}{I_{0,avg}}$; $j_1 = \frac{dV_mT_s}{L_{eq}}$; $r_1 = \frac{2L_{eq}}{d^2T_s}$.

The equivalent small-signal model described by (2.50) and (2.51) is shown in Fig. 2.7. Using Fig. 2.7, the desired transfer function can be obtained. Considering the load as resistive, the transfer functions for the output voltage to input voltage and the output voltage to duty cycle are expressed as

$$\frac{\hat{v}_o}{\hat{d}} = \frac{2K_1V_m}{1 + \frac{K_1V_md}{v_o} + sR_oC_o} \tag{2.52}$$

$$\frac{\hat{v}_o}{\hat{v}_p} = \frac{2K_1d}{1 + \frac{K_1V_md}{v_o} + sR_oC_o} \tag{2.53}$$

where

$$K_1 = \frac{3V_mR_odT_s}{4v_oL_{eq}}. \tag{2.54}$$

2.6 Effect of transformer leakage inductance

To study the effect of transformer leakage inductance, one section of the converter along with clamping circuit is shown in Fig. 2.8(a) and the key waveforms are shown in Fig. 2.8(b). When the switch is on, the current flowing through the transformer leakage inductance (i_{Tpa}) is the sum of the magnetizing current and the primary side reflected load current. Since the magnetizing current is too small, it can be neglected. Therefore, the peak value of current through leakage inductance is given by

$$i_{T,pk} = ni_{oa,pk} = n\frac{v_a}{L_2}dT_s. \tag{2.55}$$

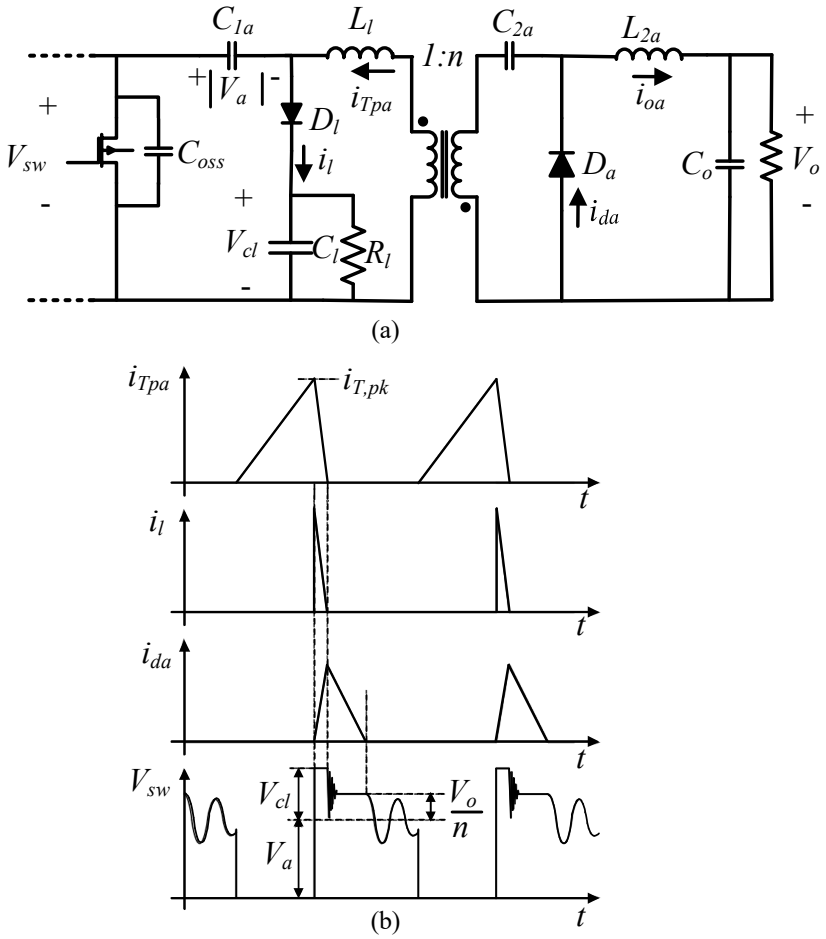


Fig. 2.8. (a) One section of the converter with clamping circuit; (b) key waveforms of the RCD clamping circuit.

When the switch is off, the current flowing through the leakage inductance (L_l) is interrupted, which induces a large voltage spike across the switch. This large voltage can cause the switch failure. To suppress the voltage spike, a resistor-capacitor-diode (RCD) passive clamping circuit is generally used across the transformer and is shown in Fig. 2.8(a). The clamping circuit absorbs the current in the leakage inductor through the clamping diode (D_l). The energy stored in the leakage inductor is transferred to clamping capacitor (C_l) and then is dissipated by the clamping resistor (R_l). The clamping circuit parameters are calculated by using the formulae proposed in [76]. According to [76] the clamping circuit parameters are given by

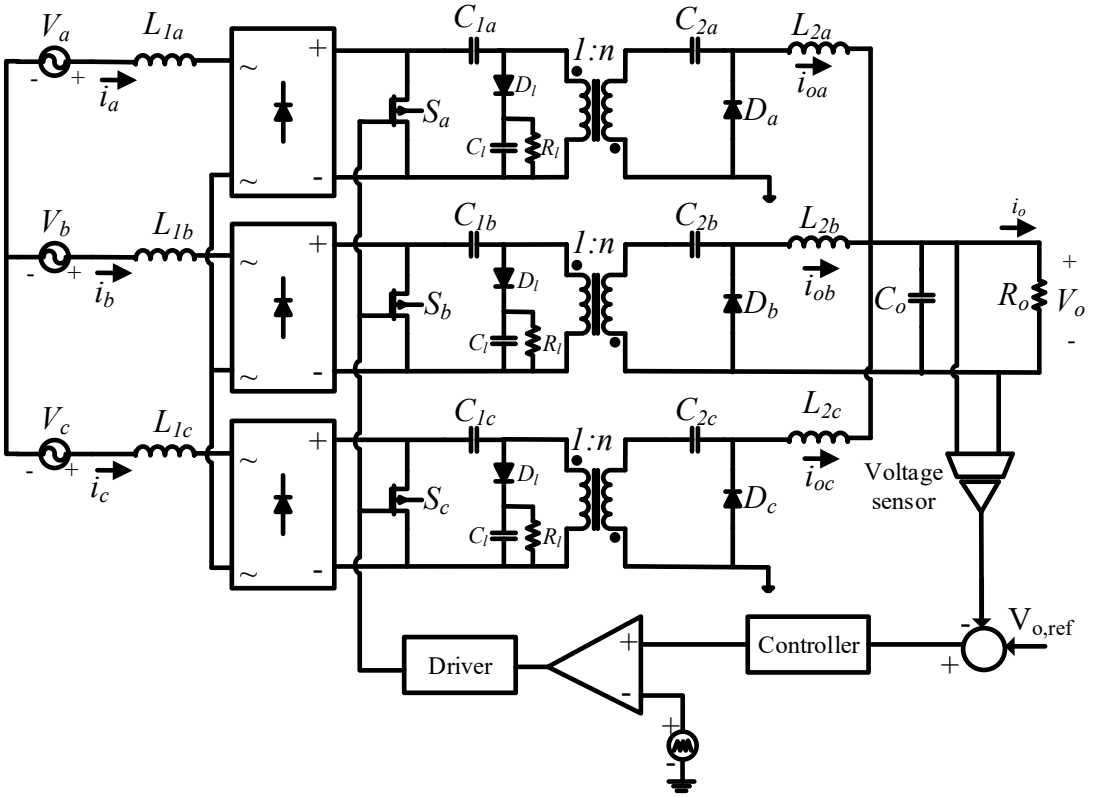


Fig. 2.9. The schematic of the proposed converter used for simulation and experimentation.

$$R_l = \frac{V_{cl}(V_{cl} - \frac{v_o}{n})T_s}{\frac{1}{2}L_l i_{T,pk}^2} \tag{2.56}$$

$$C_l > \frac{V_{cl}T_s}{R_l \Delta V_{cl}} \tag{2.57}$$

where V_{cl} = voltage across clamping capacitance, and ΔV_{cl} = maximum ripple of the clamping capacitor voltage.

2.7 Simulation results

The converter circuit under the simulation is shown in Fig. 2.9. It comprises of a RCD snubber circuit in each module, and is connected across each isolation transformer to clamp the voltage spikes caused by the transformer leakage inductance. The converter specifications are shown in Table 2.1, and the design values of the circuit components are given in Table 2.2. From (2.43),

Table 2.1: Input specifications

Rated Power (P_o)	2.0 kW
Output voltage (V_o)	270 V
Switching frequency (f_s)	100 kHz
Input line voltage	110 V $\pm$ 10 %
Supply frequency (f_l)	360-800 Hz
Input current ripple (Δi_a)	15% of peak input current

Table 2.2: Design parameters

Parameter	**Value**
Critical conduction parameter ($k_{a,crit}$)	0.09375
Maximum Duty cycle (d_{max})	0.75
Designed duty cycle (d)	0.7
Input inductance (L_1)	280 µH
output inductance (L_2)	16 µH
Energy transfer capacitors (C_1, C_2)	1 µF
Output capacitance (C_o)	750 µF
Clamper capacitance (C_l)	200 nF
Clamper resistance (R_l)	7.5 kΩ
Transformer turns ratio	1:1

(2.44), the converter output inductance is calculated, and its value is L_2 = 18 µH. In view of the system losses, the output inductance L_2 = 16 µH is considered for simulation. The transformer turns ratio of 1:1 is considered to get good magnetic coupling, and thereby the transformer leakage inductance is reduced. The transformer leakage inductance is considered as 1% of transformer magnetizing inductance. The clamping parameters are calculated at peak input voltage, the maximum voltage across the switch is clamped at 1000 V and a maximum clamping capacitor voltage ripple ΔV_{cl} = 10% of V_{cl} is assumed.

From (2.52), the control-to-output transfer function G(s) is obtained and is given by (2.58). A proportional-integral controller described by (2.59) is designed for allowing the voltage loop cut-off frequency of 667 rad/sec with a phase margin 75^0 and infinity gain margin. The open loop

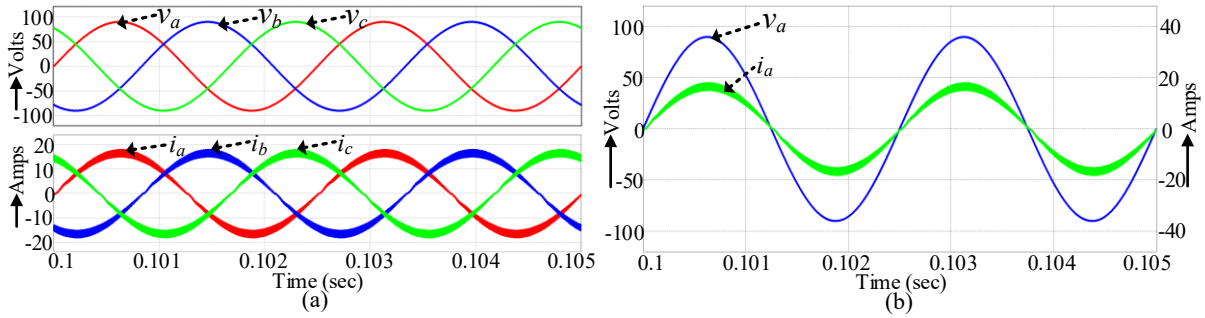


Fig. 2.10. Simulation results at rated output power (a) input voltages (v_a, v_b, v_c) and input currents (i_a, i_b, i_c); (b) input voltage (v_a) and input current (i_a) of phase-A.

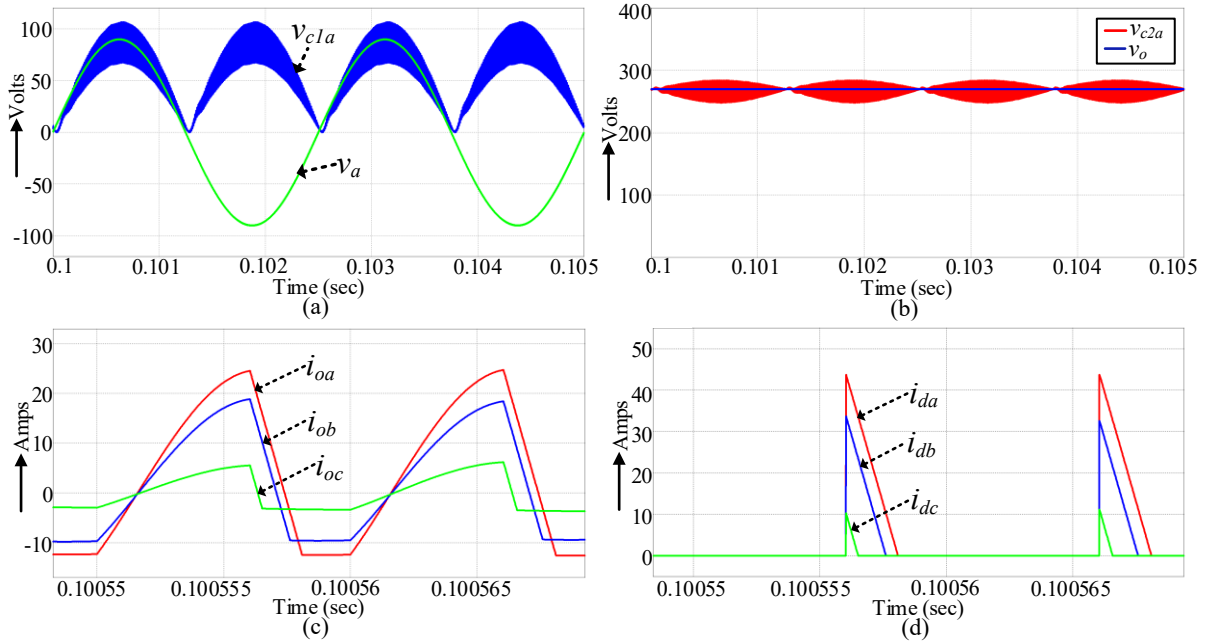


Fig. 2.11. (a) The voltage across capacitor C_{1a}; (b) the voltage across capacitor C_{2a}; (c) output currents of the three phases; (d) diode currents of the three phases.

transfer function described by (2.60) has -20 db slope at zero cross over frequency for all the loads below rated load, which indicates the system stability for all the load conditions.

$$G(s) = \frac{v_o(s)}{d(s)} = \frac{40.83}{0.0273\,S + 1.053} \tag{2.58}$$

$$H(s) = 0.42127 + \frac{93.617}{S} \tag{2.59}$$

$$G(s)H(s) = \frac{17.2(S + 222.27)}{S(0.0273S + 1.053)} \tag{2.60}$$

The output of the controller is compared with a triangular waveform of frequency 100 kHz to generate the gate signal common to all the power switches, as shown in Fig. 2.9. The simulated input voltages and the input currents are shown in Fig. 2.10(a). The input currents are sinusoidal and are in phase with the input voltages. The input current and voltage waveforms of phase-A are shown in Fig. 2.10(b). The input current is in-phase with the input voltage, which confirms the unity power factor (UPF) operation of converter.

The voltage across the capacitor C_{1a} along with its phase input voltage v_a are shown in Fig. 2.11(a). The capacitor voltage C_{1a} is rectified form of the phase input voltage, which validates the assumption (2.2). The voltage across the capacitor C_{2a} along with output voltage V_o are shown in Fig. 2.11(b). The average voltage across capacitor C_{2a} is following the output voltage V_o and thus validating the assumption (2.3). The output inductor currents, and the output diode currents are shown in Fig. 2.11(c), and Fig. 2.11(d), respectively. The output diode currents are discontinuous, and thus validating the converter analysis and the design.

The output voltage and input currents of the converter for input frequency change from 400 Hz to 800 Hz is shown in Fig. 2.12(a). The output voltage is constant at 270 V, and the input current is closely following the input voltage both in-phase and shape, which shows the robustness of the converter and accuracy of the design. The output voltage and input currents of the converter when it is subjected to a load step change from 50% to 100% of the rated output power are shown in Fig. 2.12(b). The output voltage is closely tracking the reference voltage with a small dip during load variation and is settled within the designed settling time of 10 ms, which proves the robustness of the designed controller. Due to the modular nature of the converter, each phase shares the equal amount of output power. Therefore, the converter can provide 66.66% of the rated power with one-phase loss, Fig. 2.13(a), and 33.33% of the rated power with two-phase loss, Fig. 2.13(b), without changing the controller structure and the design, which is the key merit of the modular converters.

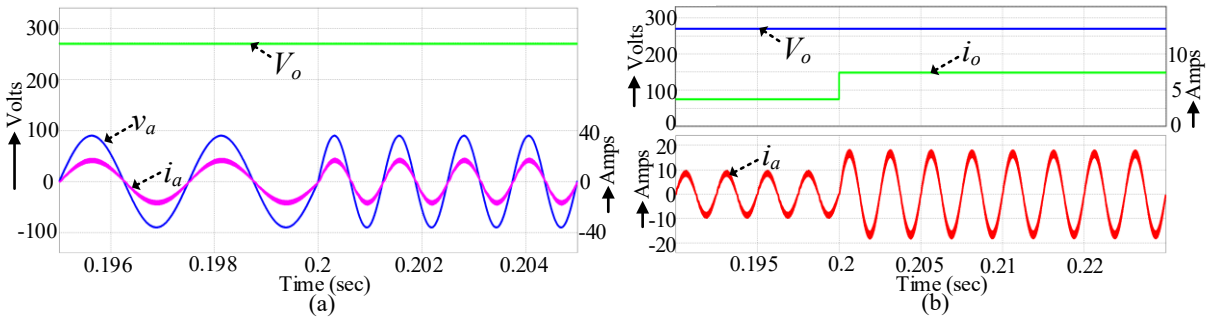


Fig. 2.12. The converter output voltage and input current of the converter (a) supply frequency variation from 400 Hz to 800 Hz; (b) load variation from 50% to 100% of the rated output power.

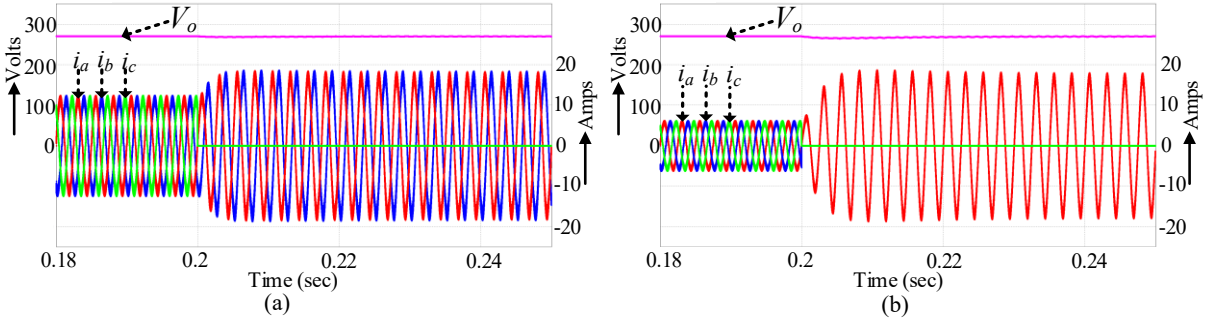


Fig. 2.13. The converter response (a) with single-phase loss; (b) with two-phase loss.

2.8 Experimental results

A 2.0 kW proof-of-concept hardware prototype is developed with the same parameters of simulation to validate the converter analysis, and to verify the simulation results. The inductors and transformers are developed with ferrite EE core, and litz wire of 14AWG to minimize the magnetic losses. The components used to develop the prototype are listed in Table 2.3. The complete experimental prototype developed in the lab is shown in Fig. 2.14. At first, the converter has been tested for grid frequency 60 Hz and the corresponding results have been presented from Fig. 2.15 to Fig. 2.18. Then, the converter PFC performance has been tested for varying supply frequency 300 to 500 Hz and the corresponding results have been presented in Fig. 2.19 and Fig. 2.20.

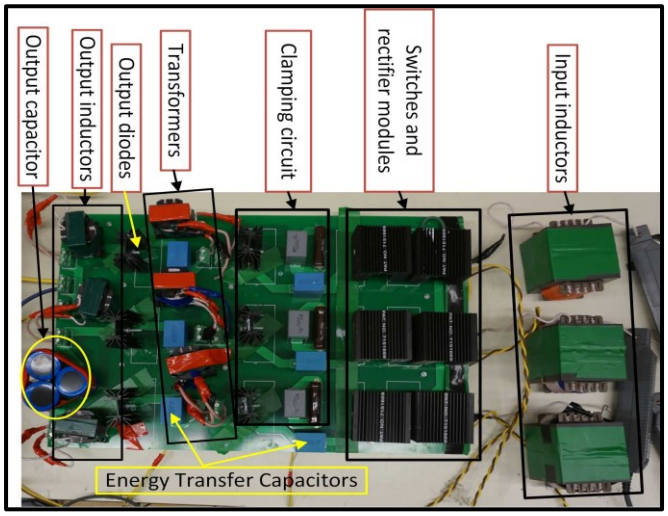


Fig. 2.14. Experimental prototype of the proposed converter.

Table 2.3: Experimental setup component specifications

Component	Specifications
Power switches, S_a, S_b, S_c	SCT3040KLGC11, 1200V, SIC Mosfet
Output diodes, D_a, D_b, D_c	RURG80100, 1000 V
Rectifier modules	FBO16-12N, 1200 V
Energy transfer capacitors (C_1, C_2)	B32674D8105K, 1 µF
Clamping diodes	FFPF10F150STU, 1500 V
Clamping capacitors, C_l	R76UR32004030J, 220 nF
Clamper resistors (R_l)	B20J15KE, 15 kΩ/2, 20 W
Output capacitor, C_o	MAL215929271E3, 3 x 270 µF
Input inductors	55 x 28 x 21, EE Ferrite cores
Output inductors, Transformers	42 x 21 x 20, EE Ferrite cores
Input source	California-MX30, 110 V, 300-500 Hz
Voltage sensor	Hall-effect LV-25P
Gate driver	Semikron- SKHI 61 R
Control platform	DSP TMS320F28335

Fig. 2.15(a) shows the measured input voltages, and Fig. 2.15(b) shows the measured three-phase input currents and output voltage. The input currents are sinusoidal, and the output voltage is settled at 270V as in simulation. Fig. 2.15(c) shows the converter input voltage and current waveforms for one phase. The input current is sinusoidal and in phase with the input voltage which

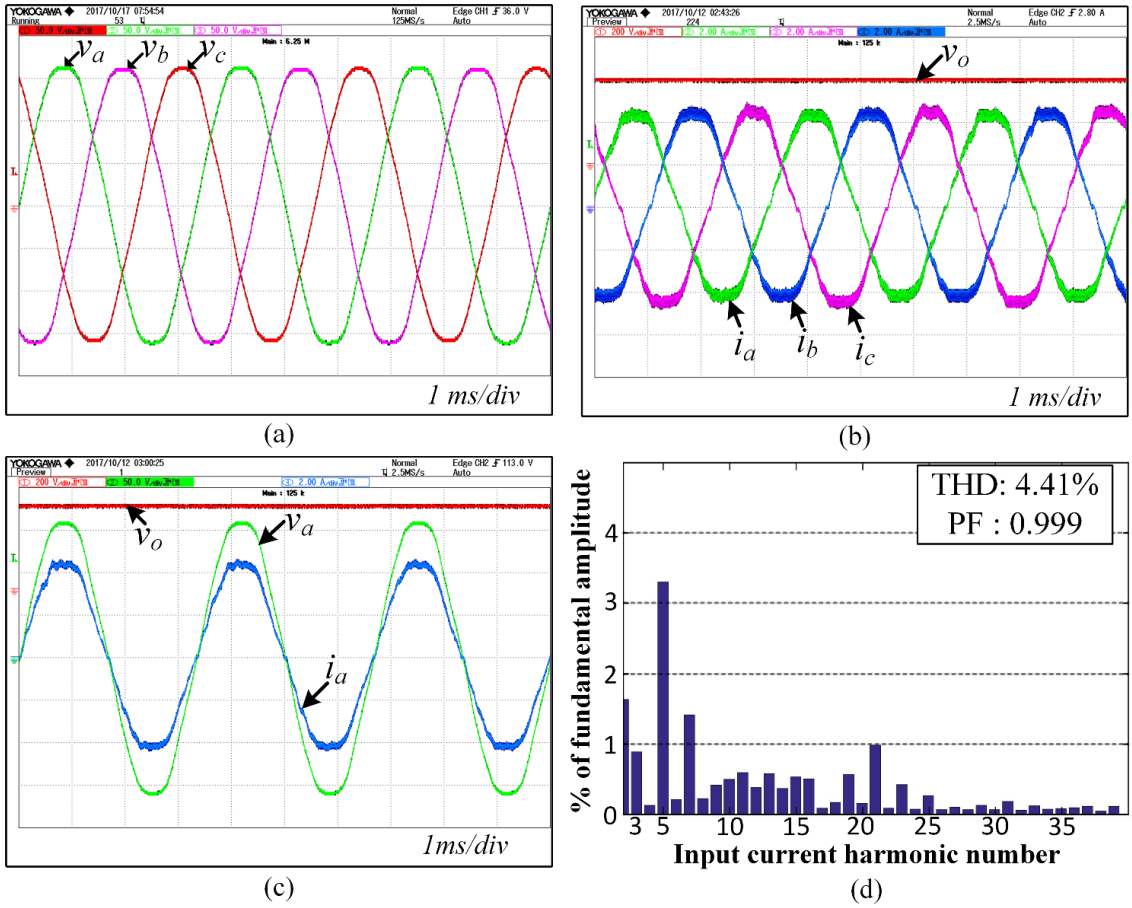


Fig. 2.15. Experimental waveforms: (a) input voltages of each phase (50V/div); (b) input currents of each phase and output voltage (2.0A/div, 200V/div); (c) input voltage (50V/div) and input current (2.0A/div) of each phase; (d) input current harmonic spectrum.

is in good agreement with the analysis. Fig. 2.15(d) shows the input current harmonic spectrum. The measured input PF is 0.999 and the THD is 4.41 %.

Fig. 2.16(a) shows the voltage across the capacitor C_{1a} which is rectified form of the input voltage v_a. Fig. 2.16(b) shows the voltage across capacitor C_{2a}, its average is equal to the output voltage V_o. Thus, Fig. 2.16(a) and Fig. 2.16(b) are confirming the simulation results and validating the converter analysis. Fig. 2.16(c) shows the measured one phase transformer primary current and secondary currents which proves that transformer action is instantaneous. Because of magnetizing current, the primary current is slightly more than secondary current. Fig. 2.16(d) shows the output current waveforms which are discontinuous and agree with the analysis. Fig. 2.16(e) and Fig. 2.16(f), show the voltage across each transformer primary and the voltage across each

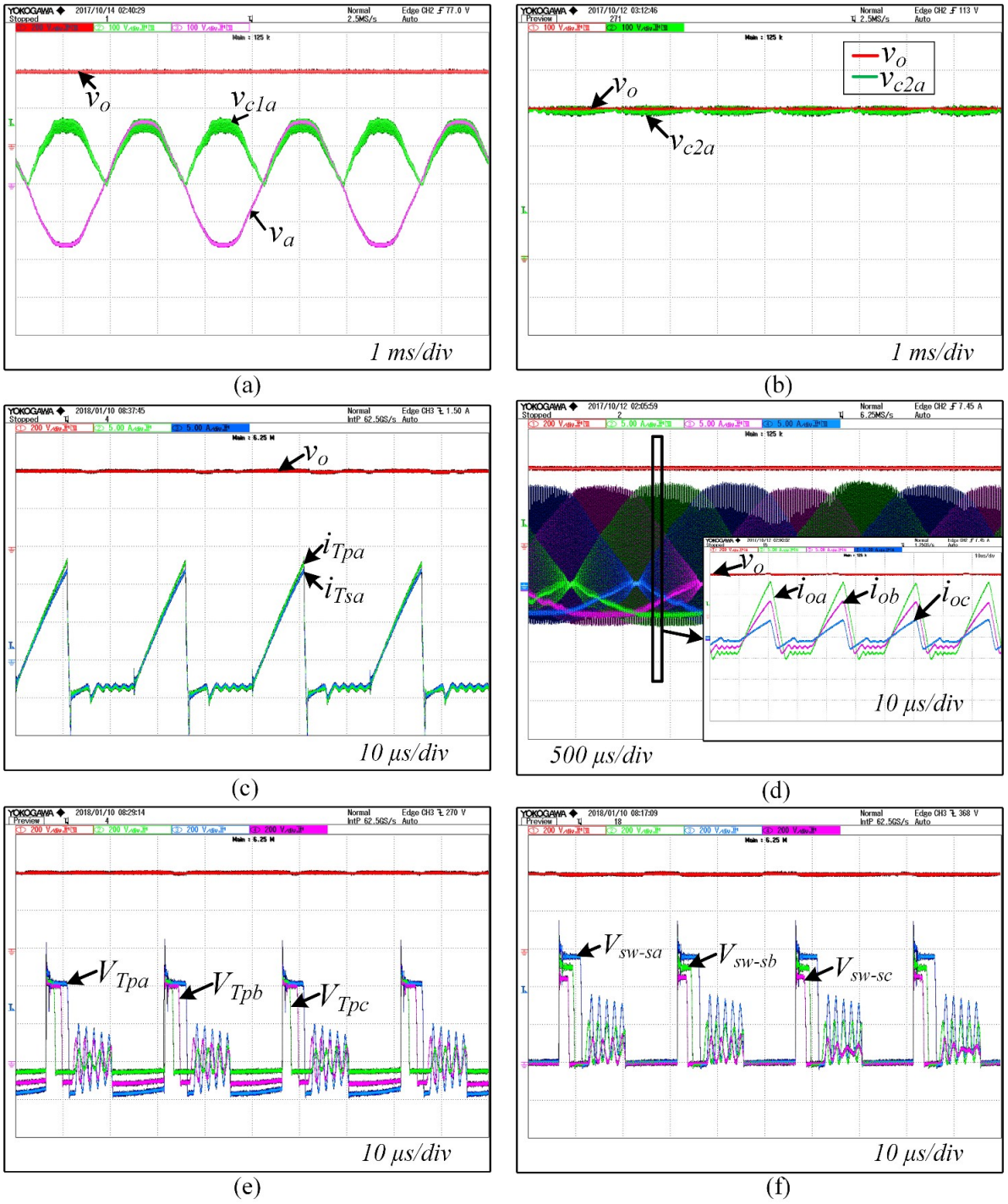


Fig. 2.16. Experimental waveforms: (a) input voltage (100 V/div) and voltage across capacitor C_{1a} (100 V/div); (b) output voltage (100V/div) and voltage across capacitor C_{2a} (100 V/div); (c) one phase transformer primary and secondary currents (5.0 A/div each); (d) output currents of each module (5.0 A/div); (e) transformer primary voltages of each phase (200 V/div); (f) voltage across each switch (200 V/div).

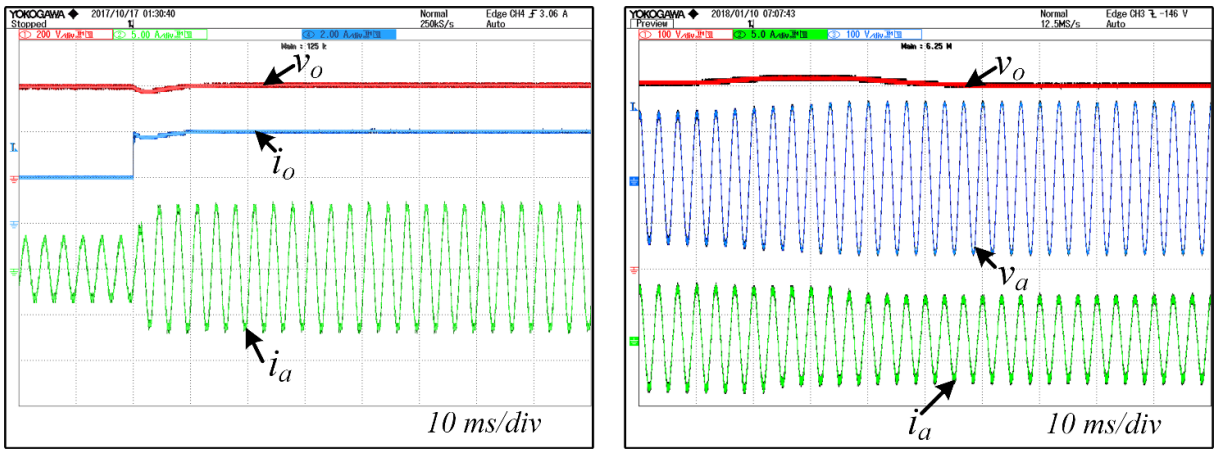


Fig. 2.17. (a) The experimental output voltage (200 V/div), output current (2.0 A/div) and input current (5.0 A/div) for load power disturbance from 0.8 kW to 1.6 kW; (b) experimental output voltage (100 V/div), input voltage (100 V/div) and input current (5.0 A/div) for phase input voltage disturbance from 100 V to 115 V.

Table 2.4: Input current THD (%) and power factor of the proposed converter at different power levels.

Output Power (P_o), kW	**THD (%)**	**PF**
0.5	4.31	0.999
0.67	4.39	0.999
0.8	4.40	0.999
1.0	4.41	0.999
1.33	4.46	0.999
1.6	4.57	0.998
2.0	4.87	0.998

power switch, respectively. It is observed that, at an instant, the voltage across each power switch is the sum of output voltage and the line to neutral input voltage of the corresponding phase.

To verify the robustness of controller, two disturbances are introduced to the converter. The first one is a load step change from 0.8 kW to 1.6 kW, and the second one is a change in phase input voltage from 100 V to 115 V. In both the cases, the output voltage is closely tracking the reference voltage, and are shown in Fig. 2.17(a) and Fig. 2.17(b), respectively. The input current THD (%) and the power factor (PF) of the converter for different output powers are listed in Table

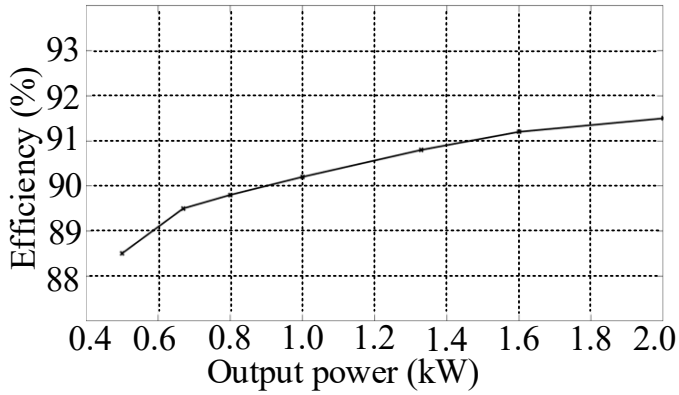


Fig. 2.18. Measured efficiency curve at different power outputs.

2.4. It shows that the converter power factor is 0.999 almost unity and the THD is less than 5 %. The measured efficiency curve of the converter (designed and built only for proof-of-concept purpose) for different power outputs is shown in Fig. 2.18. The maximum efficiency obtained is 91.5 % at rated power. The converter efficiency can further improve by at least 2 % by employing either regenerative or active-clamping circuit.

Fig. 2.19(a) shows the converter measured input currents and output voltage at rated output power for supply frequency 400 Hz. The converter input currents are sinusoidal and balanced, and the output voltage is constant and stable at reference value 270 V. Fig. 2.19(b) shows the converter UPF operation where the converter input current is closely following the input voltage both in phase and shape. Fig. 2.19(c) shows the converter for supply frequency variation 350 to 500 Hz. The converter output voltage is not disturbed and stable at 270 V, and the input currents are following the input voltage during input frequency change as well which proves the converter PFC operation. Fig. 2.19(d) shows the converter measured output inductor current which are discontinuous and validating the design. Fig. 2.20(a) shows the converter response for load perturbation from 1.0 kW to 2.0 kW. The converter output voltage is closely tracking the reference 270 V and is settled within designed time 10 ms. Fig. 2.20(b) shows the converter operation with single-phase loss. The input currents are sinusoidal, and they are in phase with input voltages which is another advantage of proposed modular converter.

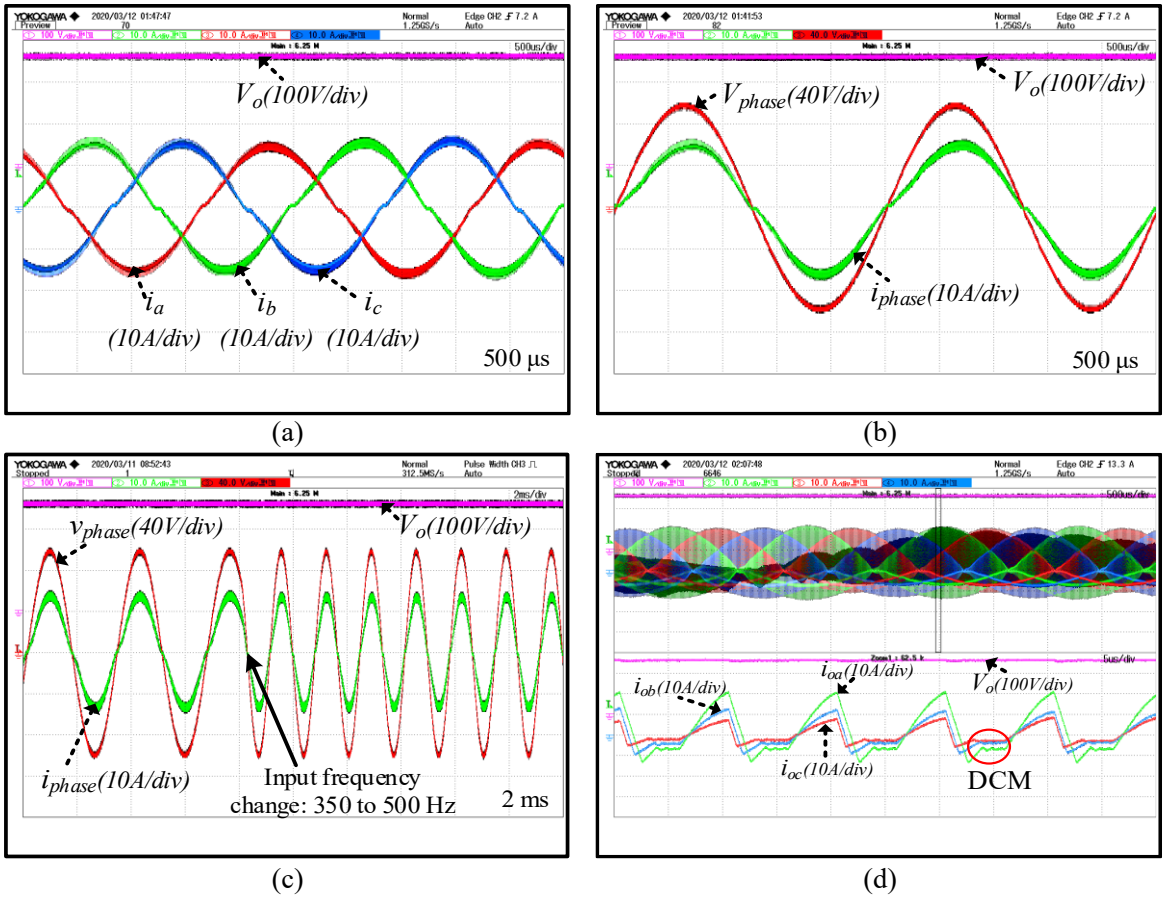


Fig. 2.19. (a) converter input currents and output voltage at rated output power for supply frequency 400 Hz; (b) converter one phase input voltage and input current at rated output power for supply frequency 400 Hz; (c) converter response for supply frequency change 350 to 500 Hz; (d) converter output inductor currents.

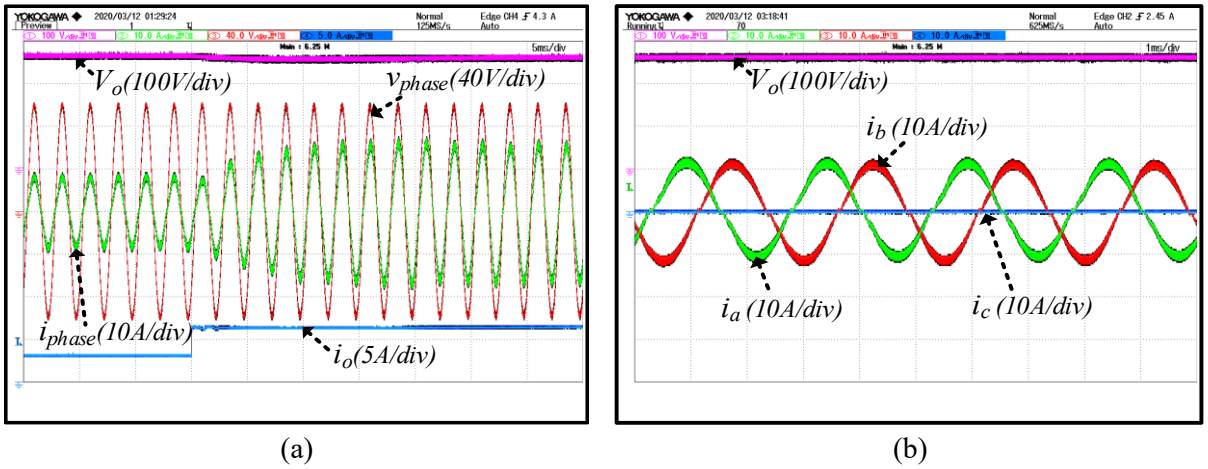


Fig. 2.20. (a) Converter response for load perturbation 1.0 to 2.0 kW; (b) converter operation with single-phase loss.

2.9 Conclusion

In this Chapter, a three-phase modular single-stage isolated Cuk PFC converter is proposed on considering the merits of Cuk converter such as inrush current limitation, no input filter requirement, and easy implementation of high frequency transformer isolation. It is operated in DOICM to obtain the PFC at AC mains for wide range of frequency. The steady-state operation, and design have been presented in detail. A simple voltage control loop with single output voltage sensor is used to regulate the output voltage, which makes the control simple, increases the reliability and robustness. The converter realized zero current turn-on of the switches, and zero diode reverse recovery losses. The converter detailed small-signal model using CIECA approach is presented to aid the controller design. The design equations for RCD snubber circuit to clamp the surge voltage caused by the transformer leakage inductance are provided in detail.

The converter analysis and design are confirmed with the simulation results from PSIM 11.1 software. It is shown that the input currents are sinusoidal and in-phase with the corresponding input voltages. An experimental laboratory prototype of 2.0 kW is designed and built to further validate the simulation results. The experimental results are in good agreement with the simulation results and validating the converter analysis and design. A high efficiency of 91.5 % (> 90 %) and an input current THD of 4.87 % (< 5 %) are recorded at rated output power with the developed laboratory prototype. Due to the modular nature of the converter, the converter can provide 66.66 % of the rated output power with one-phase loss, and 33.33 % of the rated power with two-phase loss, which is key merit of the proposed converter.

Chapter 3 : Three-Phase Non-Isolated Cuk-derived PFC Converter

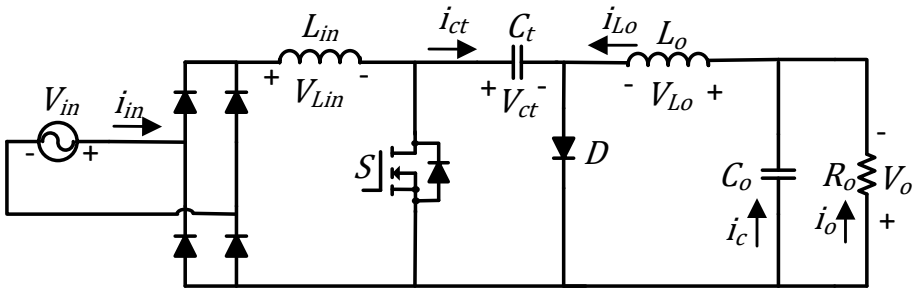
3.1 Introduction

The converter studied in Chapter 2 is a phase-modular converter, which is easy to develop, and the system repair and maintenance is easy in case of a failure. However, the three-phase modular converters in general require three single-phase full-bridge rectifiers, and three-switches, one for each phase for their operation. At a given instant, three semiconductor devices (two diodes, one switch) in each phase are in the current conduction path, which increases the converter conduction losses, and reduces the system power conversion efficiency leading to the higher thermal requirement i.e., heat sink size, and consequently reduces the system power density. Therefore, with a focus on reducing the total number of semiconductor devices and reducing the number of semiconductors per phase in the current conduction path, a three-phase Cuk-derived PFC converter is proposed and analyzed in this Chapter.

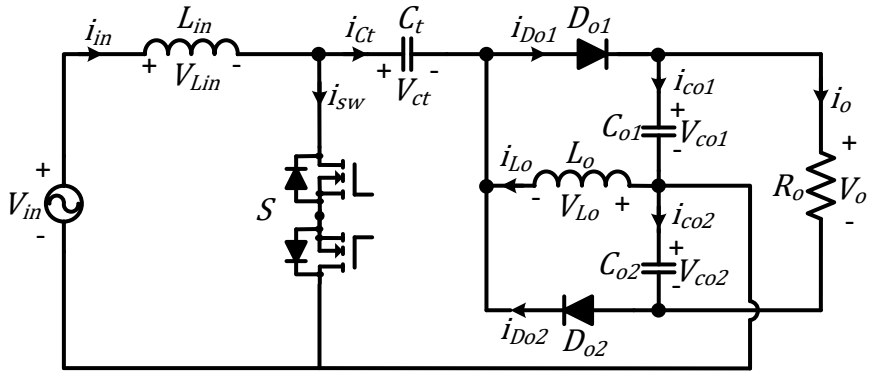
3.2 Proposed converter and control scheme

Fig. 3.1(a) shows the single-phase non-isolated Cuk PFC converter with all components placed after the full-diode bridge rectifier. Moving all the components except the DC-link capacitor on AC supply side and eliminating the full-diode bridge rectifier, the single-phase bridgeless Cuk-derived PFC converter shown in Fig. 3.1(b) is derived, where a four-quadrant switch is placed to provide the bidirectional blocking. The proposed converter shown in Fig. 3.1(c) is formed by combining the three single-phase circuits of Fig. 3.1(b) into a three-phase three-wire system, where the four-quadrant switches are no more required when the three-switches are operated synchronously with the common gate signal.

The proposed converter comprises of three input inductors, three power switches, three intermediate transfer capacitors, three output inductors, two output capacitors, and one three-phase diode-bridge rectifier. The output inductors are connected in wye configuration, and the wye junction is connected to the mid-point of the output capacitors. The three power switches are also connected in wye configuration and are controlled with the common control signal. The output inductors are designed for DCM operation to realize the inherent PFC at AC power source. In



(a)



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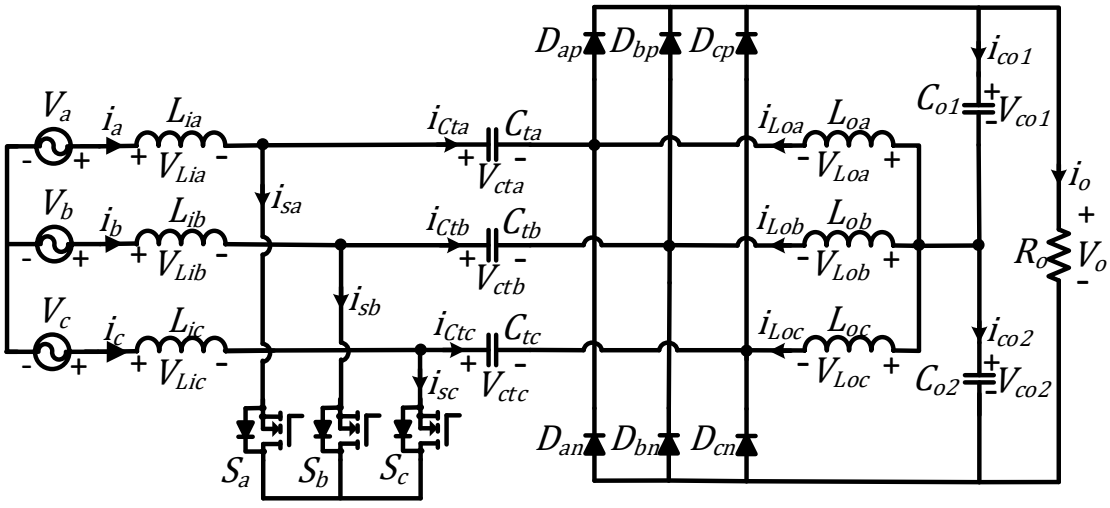


(c)

Fig. 3.1. (a) Single-phase non-isolated Cuk PFC converter; (b) single-phase non-isolated bridgeless Cuk-derived PFC converter; (c) proposed three-phase Cuk-derived non-isolated PFC converter.

Table 3.1: Comparison of the proposed Cuk-derived converter with the state-of-the art Cuk converters.

Description	Number of semiconductors			Number of passive components	Number of semiconductors per phase in the current conduction path	
	Switches	Diodes	Total		Switch ON	Switch OFF
Converter [77]	3	15	18	17	4	3
Converter [78]	1	7	8	10	2	2
Converter [79]	1	12	13	10	3	2
Converter [80]	1	7	8	12	2	2
Converter [81]	6	9	15	10	2	3
Converter [82]	2	22	24	11	3	3
Converter [83]	3	15	18	10	3	3
Proposed Converter	3	6	9	11	1	1

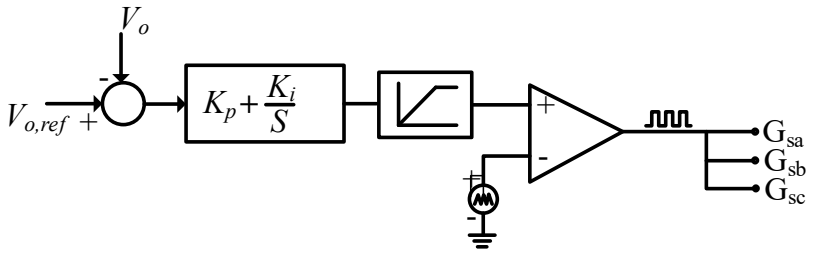


Fig. 3.2. The control circuit for the proposed converter.

DCM operation, the energy stored in the output inductor in a switching cycle depends on the value of input voltage at that instant. Therefore, the average input current naturally follows the input voltage. The converter output voltage is controlled with a simple voltage control loop shown in Fig. 3.2. Since the controlled variable is the DC output voltage, the converter duty cycle is constant for a given output power and input voltage.

The merits of the proposed converter configuration is the reduced number of components compared to the three-phase modular converters and only one semiconductor device conducts current at a time that substantially reduces the conduction losses leading to high system power conversion efficiency and power density. To demonstrate the novelty of the proposed converter, a comparison with the state-of-the art three-phase Cuk converters is provided in Table 3.1. It should

be observed that in state-of-the art converters, at a given instant, more than one semiconductor device is in the current conduction path.

The other benefit of the proposed converter is that it still operates with single-phase loss and delivers 50% of the rated output power without changing the controller structure. With a single-phase loss, the converter resembles a single-phase converter with line-to-line voltage as supply source. The limitation in delivered power is due to the duty cycle limit, which is defined in converter control system to ensure the DCM operation during overloads. The expression for the maximum duty cycle is presented in the converter design session.

3.3 Converter steady state analysis over one switching cycle

In the analysis, the phase voltages and output voltage are considered constant in one switching cycle. The following assumptions are considered to maintain the converter symmetry

$$L_{ia} = L_{ib} = L_{ic} = L_i \tag{3.1}$$

$$C_{ta} = C_{tb} = C_{tc} = C_t \tag{3.2}$$

$$L_{oa} = L_{ob} = L_{oc} = L_o \tag{3.3}$$

$$C_{o1} = C_{o2} = C_o. \tag{3.4}$$

It is also considered that the average voltage across each phase intermediate transfer capacitor is equal to the corresponding phase input voltage, and the output capacitors share the output voltage equally i.e.

$$V_{cta} = v_a; V_{ctb} = v_b; V_{ctc} = v_c \tag{3.5}$$

$$V_{co1} = V_{co2} = \frac{V_o}{2}. \tag{3.6}$$

In the proposed converter, the discontinuous current operation in output inductors is confirmed by the current discontinuity in the bridge rectifier diodes. Due to the symmetric nature of the converter, the steady-state analysis is presented only for supply period $\omega t = 0$ to $^{\pi}/_{6}$. The waveforms of current through phase–A, output inductors, and bridge rectifier diodes for one input supply period are shown in Fig. 3.3(a). The currents through the output inductors and the bridge rectifier diodes operating in discontinuous current mode for one switching cycle for supply period

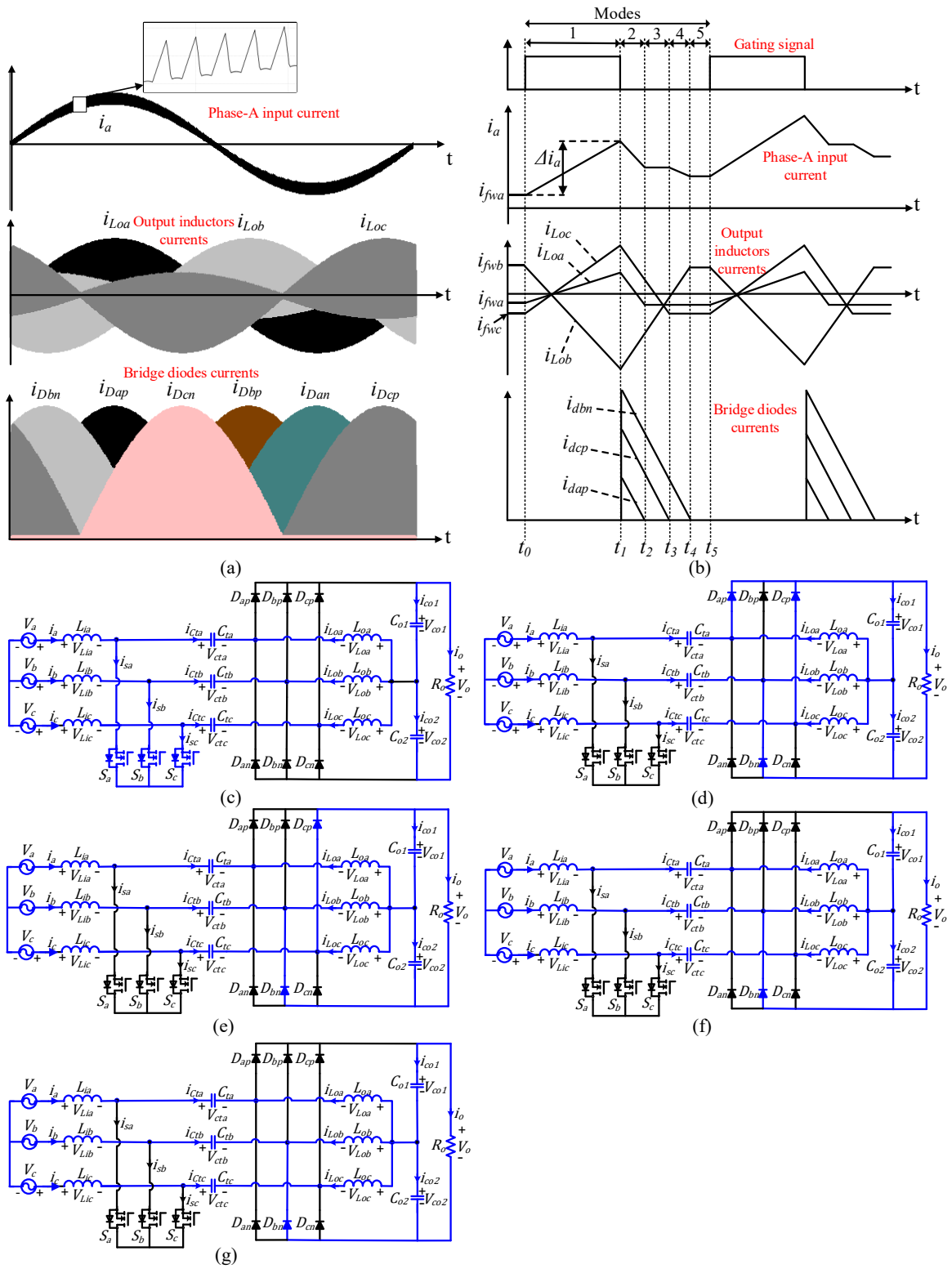


Fig. 3.3. (a) Converter phase-A input current, output inductors, and bridge rectifier diodes currents for one supply period; (b) output inductors currents, and bridge rectifier diodes currents for one switching time period; (c) to (g) the converter equivalent circuits for different operating modes.

$\omega t = 0$ to $^{\pi}/_{6}$ are shown in Fig. 3.3(b). The converter exhibits a total of five operating modes in one switching cycle, and the corresponding converter equivalent circuits are shown in Fig. 3.3(c) to Fig. 3.3(g). Since $v_c > v_a > 0$, and $v_b < 0$, the bridge rectifier diodes D_{ap}, D_{cp}, D_{bn} are in operation for supply period $\omega t = 0$ to $^{\pi}/_{6}$.

Mode-1: In this mode, all the switches are in ON state, and the bridge rectifiers are in OFF state. The converter equivalent circuit for this mode is shown in Fig. 3.3(c). The input phase voltages appear across the input inductors, and the voltages across intermediate transfer capacitors appear across output inductors. So, the input and output inductors store the magnetic energy in proportion to the voltages applied across them, while the load is supplied by the output capacitors.

Mode-2: In this mode, the gate signals to the power switches are removed, and the switches are in OFF state. The converter equivalent circuit for this mode is shown in Fig. 3.3(d). All the input inductors, and the output inductors demagnetize by delivering the stored energy to the load via the bridge rectifier diodes D_{ap}, D_{cp}, D_{bn}, while the output capacitors C_{o1}, C_{o2} and the intermediate transfer capacitors $C_{ta,b,c}$ get charged. This mode continues until the current through the bridge rectifier diode D_{ap} becomes zero.

Mode-3: In this mode, the phase-A input current is in freewheeling state, and the input inductors L_{ib}, L_{ic} and the output inductors L_{ob}, L_{oc} are still demagnetizing. The converter equivalent circuit for this mode is shown in Fig. 3.3(e). This mode continues until the current through the bridge rectifier diode D_{cp} becomes zero.

Mode-4: In this mode, the phase-A and phase-C input currents are in freewheeling state, and the input inductor L_{ib}, and the output inductor L_{ob}, are still demagnetizing. The converter equivalent circuit for this mode is shown in Fig. 3.3(f). This mode continues until the current through the bridge rectifier diode D_{bn} reaches zero.

Mode-5: In this mode, all the input currents are in freewheeling state, and all the semiconductors are non-conducting, while the load is supplied by the output capacitors. The converter equivalent circuit for this mode is shown in Fig. 3.3(g).

The expressions for current through the input inductors and output inductors for each mode of operation are derived and given in Table 3.2.

Table 3.2: Converter input and output inductors currents expressions for different modes of operation.

	Mode – 1	Mode – 2	Mode – 3	Mode – 4	Mode – 5
$i_{Lia}(t)$	$i_{fwa} + \frac{v_a}{L_i}t$	$i_{Lia}(t) = I_{Liap} - \frac{V_0}{3L_i}t$ $I_{Liap} = i_{fwa} + \frac{v_a t_{on}}{L_i}$	$i_{Lia}(t) = I_{Liar}$ $I_{Liar} = I_{Liap} - \frac{2v_a(L_i + L_o)t_{on}}{L_i(3L_i + 2L_o)}$	$i_{Lia}(t) = I_{Lias} - \frac{V_0}{6L_i}t$ $I_{Lias} = I_{Liar}$	$i_{Lia}(t)$ $= I_{Lias} - \frac{V_0}{6L_i}t_t$
$i_{Lib}(t)$	$-i_{fwb}$ $+\frac{v_b}{L_i}t$	$i_{Lib}(t) = I_{Libp} + \frac{2V_0}{3L_i}t$ $I_{Libp} = -i_{fwb} + \frac{v_b t_{on}}{L_i}$	$i_{Lib}(t) = I_{Libr} + \frac{V_0}{2L_i}t$ $I_{Libr} = I_{Libp} + \frac{4v_a(L_i + L_o)t_{on}}{L_i(3L_i + 2L_o)}$	$i_{Lib}(t) = I_{Libs} + \frac{V_0}{3L_i}t$ $I_{Libs} = I_{Libr} + \frac{v_{ca} t_{on}}{L_i}$	$i_{Lib}(t)$ $= I_{Libs} + \frac{V_0}{3L_i}t_t$
$i_{Lic}(t)$	$i_{fwc} + \frac{v_c}{L_i}t$	$i_{Lic}(t) = I_{Licp} - \frac{V_0}{3L_i}t$ $I_{Licp} = i_{fwc} + \frac{v_c t_{on}}{L_i}$	$i_{Lic}(t) = I_{Licr} - \frac{V_0}{2L_i}t$ $I_{Licr} = I_{Licp} - \frac{2v_a(L_i + L_o)t_{on}}{L_i(3L_i + 2L_o)}$	$i_{Lic}(t) = I_{Lics} - \frac{V_0}{6L_i}t$ $I_{Lics} = I_{Licr} - \frac{v_{ca} t_{on}}{L_i}$	$i_{Lic}(t)$ $= I_{Lics} - \frac{V_0}{6L_i}t_t$
$i_{Loa}(t)$	$-i_{fwa}$ $+\frac{v_a}{L_o}t$	$i_{Loa}(t) = I_{Loap} - \frac{V_o}{2L_o}t$ $I_{Loap} = -i_{fwa} + \frac{v_a t_{on}}{L_o}$	$i_{Loa}(t) = -i_{Lia}(t)$	$i_{Loa}(t) = -i_{Lia}(t)$	$i_{Loa}(t)$ $= -i_{Lia}(t)$
$i_{Lob}(t)$	$i_{fwb} + \frac{v_b}{L_o}t$	$i_{Lob}(t) = I_{Lobp} + \frac{V_o}{2L_o}t$ $I_{Lobp} = i_{fwb} + \frac{v_b t_{on}}{L_o}$	$i_{Lob}(t) = I_{Lobr} + \frac{V_o}{2L_o}t$ $I_{Lobr} = I_{Lobp} + \frac{3v_a(L_i + L_o)t_{on}}{L_o(3L_i + 2L_o)}$	$i_{Lob}(t) = I_{Lobs} + \frac{V_o}{2L_o}t$ $I_{Lobs} = I_{Lobr} + \frac{v_{ca} t_{on}}{L_o}$	$i_{Lob}(t)$ $= -i_{Lib}(t)$
$i_{Loc}(t)$	$-i_{fwc} + \frac{v_c}{L_o}t$	$i_{Loc}(t) = I_{Locp} - \frac{V_o}{2L_o}t$ $I_{Locp} = -i_{fwc} + \frac{v_c t_{on}}{L_o}$	$i_{Loc}(t) = I_{Locr} - \frac{V_o}{2L_o}t$ $I_{Lobr} = I_{Locp} - \frac{3v_a(L_i + L_o)t_{on}}{L_o(3L_i + 2L_o)}$	$i_{Loc}(t) = -i_{Lic}(t)$	$i_{Loc}(t)$ $= -i_{Lic}(t)$
Time period	$t_{on} = dT_s$	$t_r = \frac{6v_a(L_i + L_o)}{V_o(3L_i + 2L_o)}t_{on}$	$t_s = \frac{2v_{ca}}{V_o}t_{on}$	$t_t = \frac{18v_a L_i(L_i + L_o)}{V_o(3L_i + 2L_o)^2}t_{on}$	$T_s - t_{on} - t_r$ $- t_s - t_t$

3.4 Converter design

This section presents the expressions for converter average output current and input current and derives the DCM condition and the design equations for each passive component.

3.4.1 Condition for discontinuous current operation

The converter discontinuous current operation is ensured, when the sum of the time durations of converter modes 1 to 4 is less than the switching period T_s,

$$t_{on} + t_r + t_s \leq T_s. \tag{3.7}$$

On substituting t_{on}, t_r, t_s, t_t expressions from Table 3.2 in (3.7), and after simplifying gives,

$$d\left(1-\frac{2v_b}{V_o}-\frac{4v_a}{V_o}\left(\frac{L_o}{3L_i+2L_o}\right)^2\right)\leq 1. \tag{3.8}$$

Since $L_o \ll L_i$, the term containing $\left(\frac{L_o}{3L_i+2L_o}\right)^2$ in equation (3.8) can be neglected. On substituting, $-v_b = V_m \sin(\omega t + 60^0)$ gives,

$$d \leq \frac{M}{M+2\sin(\omega t+60^0)}. \tag{3.9}$$

In (3.9), the converter minimum duty cycle occurs when $\sin(\omega t + 60^0) = 1$, on simplifying it gives $\omega t = 30^0$. Therefore, the condition for converter discontinuous current operation is

$$d \leq \frac{M}{M+2}. \tag{3.10}$$

The converter critical voltage conversion ratio for a given duty cycle can be defined from (3.10), and is given as,

$$M_{cr} \geq \frac{2d}{1-d}. \tag{3.11}$$

From the converter configuration, it is evident that the converter output voltage must be greater than two times of the peak input voltage to reverse bias the bridge rectifier diodes. Therefore, to operate the converter as intended, the converter voltage gain must be,

$$M \geq M_{cr} \geq 2. \tag{3.12}$$

3.4.2 Converter average output current

It is known that in steady state, in a switching cycle, the average current through the capacitor is zero. Therefore, the average output current of the converter for one switching cycle is given by,

$$i_{o,avg} = \frac{1}{2}\left(\langle i_{dap}\rangle + \langle i_{dbn}\rangle + \langle i_{dcp}\rangle\right). \tag{3.13}$$

The expressions for each diode currents in above equation is given as,

$$i_{dap}(t) = i_{Lia}(t) + i_{Loa}(t) \tag{3.14}$$

$$i_{dbn}(t) = i_{Lib}(t) + i_{Lob}(t) \tag{3.15}$$

$$i_{dcp}(t) = i_{Lic}(t) + i_{Loc}(t). \tag{3.16}$$

Substituting the input inductor and output inductor current expressions from Table 3.2 in (3.14), (3.15), (3.16), and calculating the average for one switching cycle, and further substituting in (3.13), and simplifying gives the converter average output current for one switching cycle.

$$i_{o,avg} = \frac{3V_m^2 d^2 T_s}{4L_{eq}V_o} \tag{3.17}$$

where

$$L_{eq} = \frac{L_i L_o}{L_i + L_o}. \tag{3.18}$$

The average output current of the converter for one input supply period is calculated as

$$I_{o,avg} = \frac{6}{\pi}\int_0^{\pi/6} i_{o,avg}\ d(wt) = \frac{3V_m^2 d^2 T_s}{4L_{eq}V_o}. \tag{3.19}$$

The converter normalized output current from (3.19) is given as

$$I_{o\_n} = \frac{d^2 V_m}{V_o} = \frac{d^2}{M}. \tag{3.20}$$

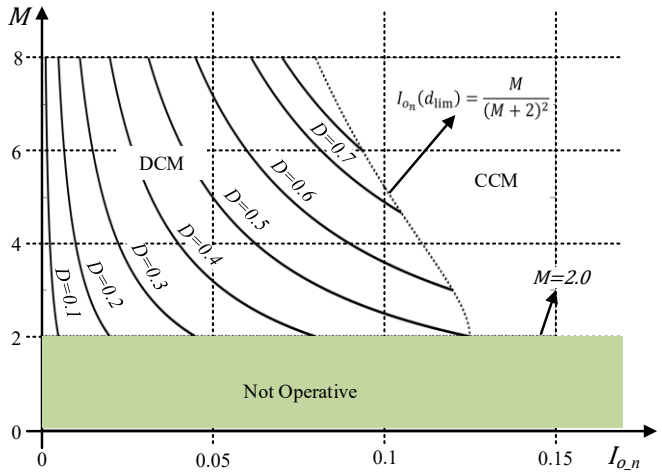


Fig. 3.4. Load characteristics of converter: voltage gain versus the normalized average output current.

Using (3.20), the converter load characteristics are drawn and are shown in Fig. 3.4. The converter is moving towards CCM with the increase in load, and it is evaded by limiting the duty cycle defined in (3.10).

3.4.3 Converter input current

With a consideration that the converter operation is loss free, then

$$P_{in} = P_o \tag{3.21}$$

$$\frac{V_m I_m}{2} = V_o I_{o,avg}. \tag{3.22}$$

On substituting $I_{o,avg}$ expression from (3.19) in (3.22), and then simplifying gives,

$$I_m = \frac{V_m d^2 T_s}{2L_{eq}}. \tag{3.23}$$

3.4.4 Design of input and output inductors

The input inductor is designed by choosing the maximum allowable current ripple through it over a switching cycle. If Δi_{Li} is the maximum allowable current ripple over one switching cycle, then

$$\Delta i_{Li} = \frac{V_m}{L_i} dT_s \tag{3.24}$$

$$L_i = \frac{V_m}{\Delta i_{Li}} dT_s \tag{3.25}$$

If L_i is known, then output inductor L_o can be calculated from (3.18), and is given as

$$L_o = \frac{L_i L_{eq}}{L_i - L_{eq}}. \tag{3.26}$$

The value of L_{eq} is obtained from (3.10), (3.19), and is given as

$$L_{eq} \leq \frac{3{V_m}^2 {V_o}^2 T_s}{4P_o(V_o + 2V_m)^2}. \tag{3.27}$$

3.4.5 Design of intermediate transfer capacitor

The transfer capacitor 'C_t' design is very vital as its value has substantial impact on input current quality. The transfer capacitance value should be selected in such a way that it should not produce low frequency oscillations with the input inductor and as well as the output inductor. Therefore, the resonant frequency f_r caused by the intermediate transfer capacitor C_t must be in between the switching frequency and the supply frequency,

$$f \ll f_r \ll f_s \tag{3.28}$$

where $f_r = \frac{1}{2\pi\sqrt{C_t(L_i+L_o)}}$.

3.4.6 Design of output capacitor

In aerospace applications, the output capacitor design depends on the power holdup time required after the AC source interruption. If t_h is the holdup time required to bring the output capacitor voltage to 90%, then each output capacitance value required in the proposed converter is given by

$$C_{o1} = C_{o2} = \frac{4P_o t_h}{(0.19V_o^2)}. \tag{3.29}$$

3.5 Component stresses

This section presents the voltage and current stress expressions for each converter component and validates with simulated values.

3.5.1 Voltage stress

3.5.1.1 Switches S_a, S_b, S_c

Fig. 3.5(a) shows the voltage profile of the switch S_a for one supply period. Each switch body diode is forward biased for two-third of the supply period during its phase negative half-cycle around its negative peak, and in the meanwhile the two anti-parallel body diodes of the other switches experience a maximum voltage stress of

$$V_{sw,max} = V_o + \sqrt{3}V_m. \tag{3.30}$$

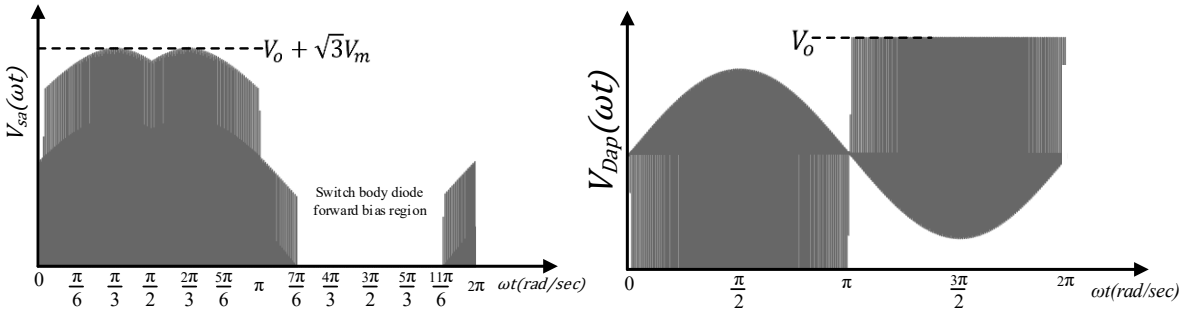


Fig. 3.5. (a) The voltage profile of switch mosfet 'S_a' for one input line period; (b) the voltage profile of power bridge rectifier diode 'D_{ap}' for one input line period.

3.5.1.2 Bridge rectifier diodes

Fig. 3.5(b) shows the voltage profile of the bridge rectifier diode D_{ap} for one supply period. Each bridge diode experiences a maximum voltage stress of V_o when the other diode in its leg is in conduction.

3.5.2 Current stress

3.5.2.1 Switches S_a, S_b, S_c

The current expression flowing through the switch for one switching period is given as

$$i_{sw,a,b,c}(t) = \begin{cases} \frac{v_{a,b,c}}{L_{eq}} t & 0 < t \leq t_{on} \\ 0 & t_{on} < t \leq T_s \, . \end{cases} \tag{3.31}$$

Using (3.31), the expressions for the switch average and root mean square (RMS) currents are derived and are given in (3.32), and (3.33), respectively

$$I_{sw,avg} = \frac{V_m d^2 T_s}{\pi L_{eq}} \tag{3.32}$$

$$I_{sw,rms} = \frac{V_m d T_s}{L_{eq}} \sqrt{\frac{d}{6}} . \tag{3.33}$$

3.5.2.2 Bridge rectifier diodes

The expressions to determine the bridge rectifier diode average and RMS currents are as follows

$$I_{D,avg} = \frac{V_m^2 d^2 T_s}{4 L_{eq} V_o} \tag{3.34}$$

$$I_{D,rms} = \frac{2 V_m d T_s}{3 L_{eq}} \sqrt{\frac{d V_m}{\pi V_o}} \, . \tag{3.35}$$

3.5.2.3 Output filter capacitors, C_{o1}, C_{o2}

The expression to determine the output capacitors RMS current is

$$I_{Co,rms} = \sqrt{I_{do,rms}^2 - I_{do,avg}^2} \tag{3.36}$$

where

$$I_{do,rms} = \frac{V_m d T_s}{L_{eq}} \sqrt{\frac{2 d V_m}{\pi V_o} \left(\sqrt{3} - 1\right)} \tag{3.37}$$

$$I_{do,avg} = \frac{3 V_m^2 d^2 T_s}{4 L_{eq} V_o} . \tag{3.38}$$

3.5.2.4 Intermediate transfer capacitors, $C_{ta,b,c}$

The expression to determine the intermediate transfer capacitors RMS current is

$$I_{ct,rms} = \frac{V_m d T_s}{2 L_{eq}} \sqrt{\frac{2d}{3} - \frac{d^2}{2}} . \tag{3.39}$$

3.5.2.5 Input inductors, $L_{ia,b,c}$

The expression to determine the input inductors RMS current is

$$I_{Li,rms} = \frac{V_m d^2 T_s}{2\sqrt{2} L_{eq}} . \tag{3.40}$$

3.5.2.6 Output inductors, $L_{oa,b,c}$

The expression to determine the output inductors RMS current is

Table 3.3: Numerical values of theoretically calculated and simuated average and RMS currents for P_o = 2.0 kW, V_{L-L} = 110 V_{rms}, V_o = 270 V, f_s = 100 kHz, L_{eq}= 10.907 μH, d = 0.6005.

Quantity	Calculated	Simulated
$\boldsymbol{I_{sw,avg}}$	9.45	9.40
$\boldsymbol{I_{sw,rms}}$	15.64	15.79
$\boldsymbol{I_{D,avg}}$	2.47	2.51
$\boldsymbol{I_{D,rms}}$	8.32	8.38
$\boldsymbol{I_{Co,rms}}$	13.14	13.24
$\boldsymbol{I_{Ct,rms}}$	11.60	11.61
$\boldsymbol{I_{Li,rms}}$	10.50	10.55
$\boldsymbol{I_{Lo,rms}}$	12.36	12.13

$$I_{Lo,rms} = \frac{V_m d T_s}{3L_{eq}} \sqrt{\left(\frac{8V_m}{\pi V_o} + \frac{3}{2}\right)(d - d^2)}\,. \tag{3.41}$$

The analytical expressions derived from (3.32) to (3.41) are verified with the simulation results. Table 3.3 lists the numerical values of theoretically calculated and the simulated average and RMS currents at 2.0 kW output power. The calculated values are almost equal to the simulated values, which shows the accuracy of the derived formulae.

3.6 Converter small-signal model

The converter control-to-output transfer function is obtained using CIECA approach [74], [75]. This approach linearizes the converter non-linear part by replacing it with the switching cycle average current produced by it, as shown in Fig. 3.6. The converter small-signal model defined by (3.42) and (3.43) represented in Fig. 3.7 is obtained by applying small-signal perturbations to (3.17) and (3.23), and after neglecting the second order terms.

$$\hat{\imath}_{o,avg} = j_2 \hat{d} + g_2 \hat{v}_m - \frac{1}{r_2}\hat{v}_o \tag{3.42}$$

$$\hat{\imath}_m = j_1 \hat{d} + \frac{1}{r_1}\hat{v}_m \tag{3.43}$$

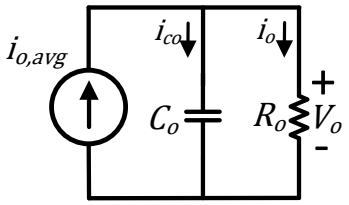


Fig. 3.6. Converter equivalent circuit as per CIECA approach.

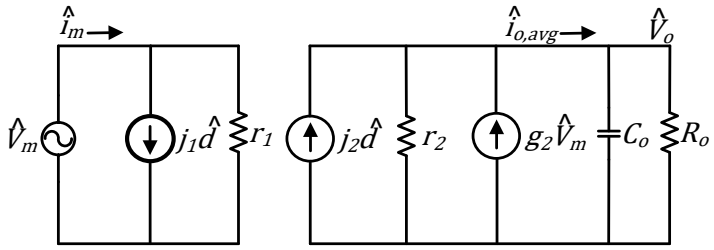


Fig. 3.7. Small-signal model of the proposed converter.

where $j_2 = \frac{3V_m^2}{v_o}\frac{dT_s}{2L_{eq}}$; $g_2 = \frac{3V_m}{v_o}\frac{d^2T_s}{2L_{eq}}$; $r_2 = \frac{V_o}{i_{0,avg}}$; $j_1 = \frac{dV_mT_s}{L_{eq}}$; $r_1 = \frac{2L_{eq}}{d^2T_s}$.

The desired control-to-output transfer function described in (3.44) is obtained from Fig. 3.7 by considering the resistive load.

$$\frac{\hat{v}_o}{\hat{d}} = \frac{2K}{1 + \frac{Kd}{V_o} + sR_oC_o} \tag{3.44}$$

where

$$K = \frac{3{V_m}^2R_odT_s}{4V_oL_{eq}}. \tag{3.45}$$

3.7 Results and discussion

This section presents the simulation and experimental results of the proposed converter to validate the converter analysis and design, and presents a discussion on converter efficiency.

3.7.1 Simulation results

The proposed converter shown is simulated in PSIM 11.1 software to confirm the converter analysis and the design. The converter specifications are given in Table 3.4. The results of the

Table 3.4: Converter input specifications.

Parameter	Value
Line voltage	110 V ± 10 %
Input frequency, $\boldsymbol{f}$	360-800 Hz
Output power, $\boldsymbol{P_o}$	2.0 kW
Output voltage, $\boldsymbol{V_o}$	270 V
Switching frequency, $\boldsymbol{f_s}$	100 kHz

Table 3.5: Converter designed parameters.

Parameter	Value
Maximum Duty cycle, $\boldsymbol{d_{max}}$	0.6005
Input inductance, $\boldsymbol{L_i}$	240 μH
Output inductance, $\boldsymbol{L_o}$	11 μH
Intermediate transfer capacitance, $\boldsymbol{C_t}$	2 μF
Output capacitances, $\boldsymbol{C_{o1}}$, $\boldsymbol{C_{o2}}$	1.44 mF

converter design is given in Table 3.5. The input inductance value is calculated from the allowable maximum input current ripple which is 15% of the peak value. The output inductance value is calculated from (3.26). The output filter capacitances values are calculated from the holdup time required which is considered at 2.5 ms. Using the designed parameters, the converter control-to-output transfer function is obtained from (3.44) and is given in (3.46). A PI-controller transfer function described in (3.47) is designed for a phase margin of 75^0 and gain cross-over frequency 625 rad/sec.

$$G(s) = \frac{v_o(s)}{d(s)} = \frac{939.5}{0.02624\,S + 2.053} \tag{3.46}$$

$$H(s) = 0.0162 + \frac{4.143}{S} \tag{3.47}$$

With the designed parameters and the designed controller, the circuit is simulated, and the results have been presented for input frequency f = 400 Hz. Fig. 3.8(a) depicts the converter input phase currents, which are sinusoidal, and balanced. Fig. 3.8(b) depicts the converter input phase voltage and input phase current of phase-A. The phase current is in-phase with the corresponding phase voltage and confirming the converter UPF operation. Fig. 3.8(c) depicts the output voltage across each output capacitor, and the combined total output voltage. Each output capacitor is sharing the half- of the output voltage as anticipated and validating the assumption (3.6). Fig. 3.8(d) depicts the phase-A intermediate transfer capacitor voltage along with phase-A input voltage; both are in phase, and the average values are equal, validating the assumption (3.5). Fig. 3.8(e) depicts the converter response for input frequency variation from 400 Hz to 800 Hz; the output voltage is constant during input frequency variation, and the input current is in phase with

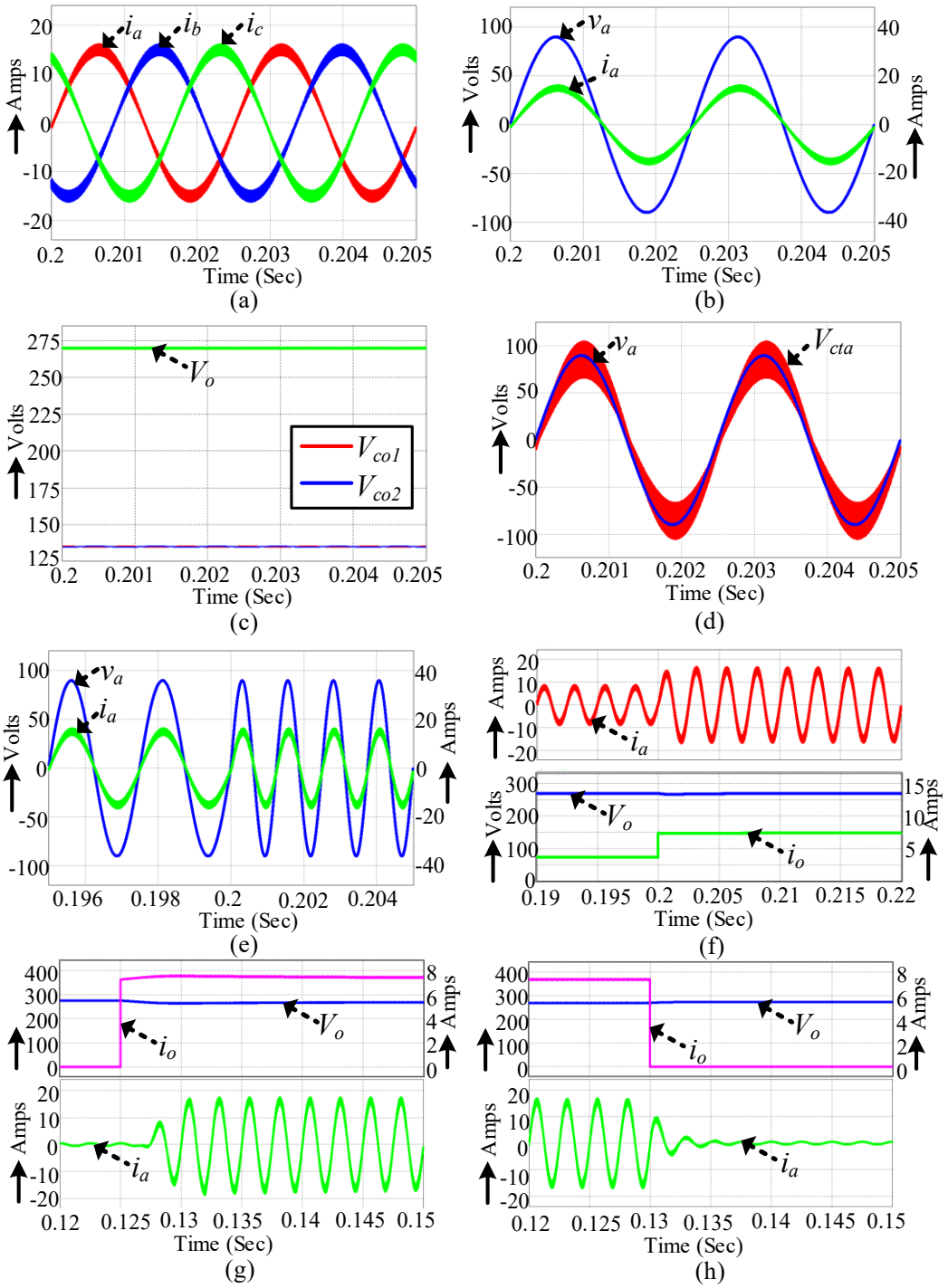


Fig. 3.8. Simulation results at rated output power (a) input phase currents; (b) phase-A voltage and current; (c) output capacitors voltages and total output voltage; (d) phase-A intermediate transfer capacitor voltage along with phase-A input voltage; (e) converter response for input frequency variation 400 to 800 Hz; (f) converter response for load change 50 % to 100 % of rated output power; (g) converter response for rated constant power load applied; (h) converter response for rated constant power load removed.

the input voltage. Fig. 3.8(f) depicts the converter response for load variation from 50% to 100%; the controller responds immediately to the load change, and the output voltage is settled at reference value 270 V within the designed settling time of 10 msec. Fig. 3.8 (g) and Fig. 3.8 (h) show the converter response when rated constant power applied and removed, respectively. In both cases, the converter response is smooth and instantaneous, and the output voltage is closely tracking the reference which validates the robustness of the converter and the designed controller.

3.7.2 Experimental results

To validate the analysis of the proposed converter and to verify the simulation results, a 2.0 kW proof-of-concept laboratory hardware prototype has been built with the same parameters used in simulation and is shown in Fig. 3.9. The hardware details are given in Table 3.6. The DSP TMS20F28335 is employed as digital control platform to generate the gate signals for the

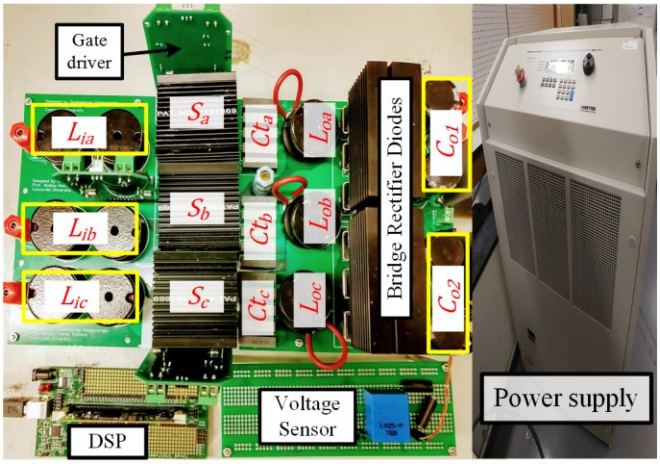


Fig. 3.9. The hardware prototype of the proposed converter.

Table 3.6: Prototype component specifications.

Component	**Specifications**
Switches, $\boldsymbol{S_a, S_b, S_c}$	UJ3C065030K3S, 650 V, 62 A, 35 mΩ
Bridge rectifier Diodes	VS-65EPF06LHM3, 600 V, 65 A
Output capacitors, $\boldsymbol{C_{o1}}$, $\boldsymbol{C_{o2}}$	ESMQ401VSN471MQ50W, 3*470 µF
Transfer capacitors, $\boldsymbol{C_t}$	R71PI34704030M, 5 x 0.47 µF
Input inductors	1140-101K-RC, 2*100 μH
Output inductors	1140-100K-RC, 10 μH
Snubber capacitor	R75QD0470DQ30J, 470 pF
Snubber resistor	EP5WS100RJ, 100 Ω
Gate drivers	HCNW3120 IC
Power source	California-MX30 (300 – 500 Hz)

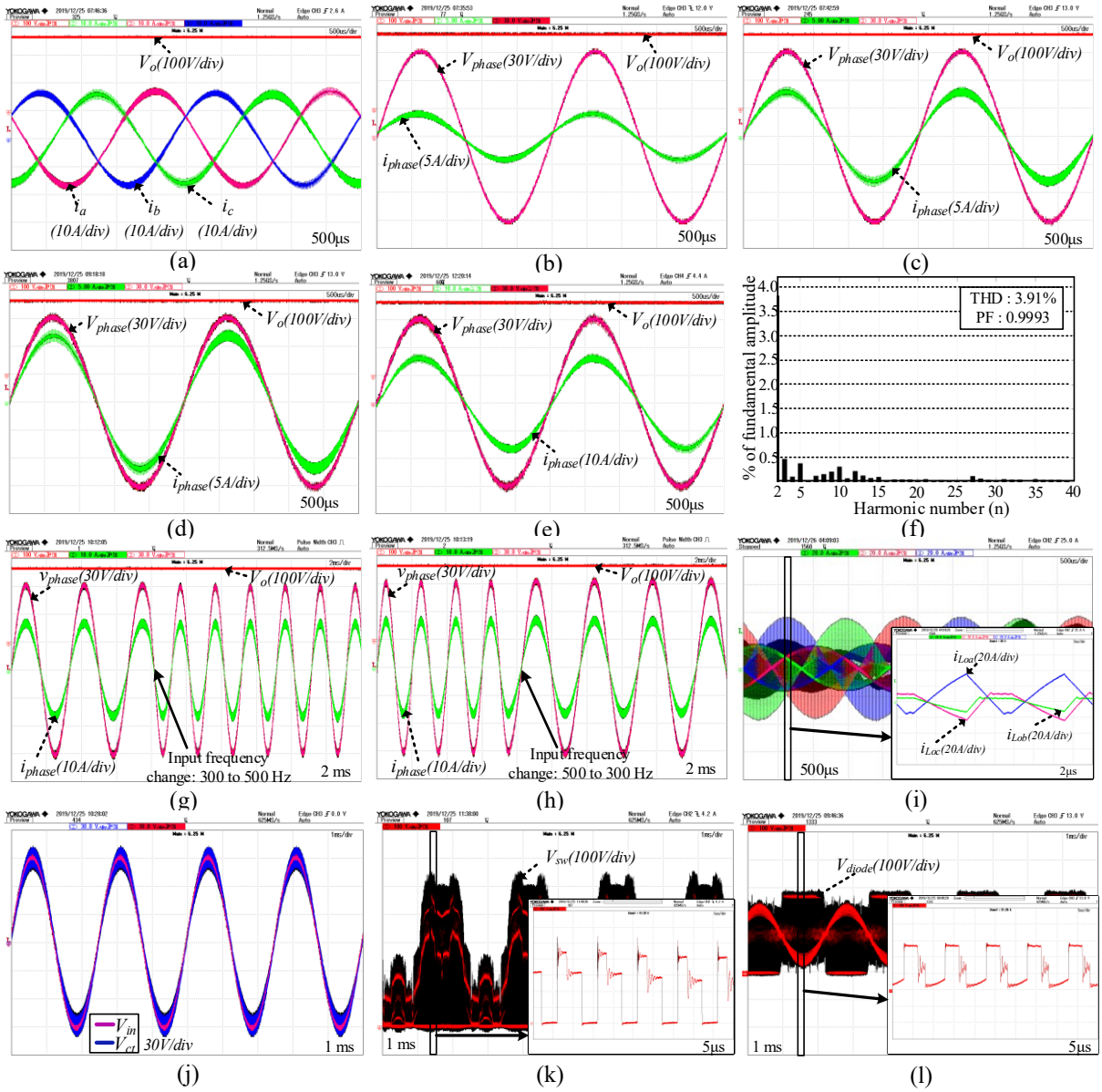


Fig. 3.10. Experimental results (a) input phase currents for rated output power; (b), (c), (d), (e) one phase input voltage and input current for converter output powers of 0.5 kW, 1.0 kW, 1.5 kW, 2.0 kW; (f) harmonic spectrum of input current at rated output power; (g), (h) converter response for supply frequency variation 300 Hz to 500 Hz, and 500 Hz to 300 Hz; (i) output inductors currents; (j) intermediate transfer capacitor voltage and its phase input voltage; (k) voltage waveform across one of the power switches; (l) voltage waveform across one of the bridge rectifier diodes.

Table 3.7: Converter measured input current THD (%) and power factor at different output powers.

P_o, kW	THD (%)	PF
0.5	6.99	0.9976
0.75	6.19	0.9981
1.0	5.49	0.9985
1.25	4.99	0.9988
1.5	4.52	0.9990
1.75	4.10	0.9992
2.0	3.91	0.9993

converter. The hall-effect sensor LV-25P is employed to sense the converter output voltage. The converter steady-state results for converter input frequency of 400 Hz are shown in Fig. 3.10.

Fig. 3.10(a) depicts the measured input phase current waveforms at rated output power for supply frequency 400 Hz, which are sinusoidal, and balanced. Fig. 3.10(b), Fig. 3.10(c), Fig. 3.10(d), and Fig. 3.10(e) depict the waveforms of one phase input voltage and input current for output power of 0.5 kW, 1.0 kW, 1.5 kW, and 2.0 kW, respectively. In all the cases, the input current is following the input voltage both in phase and shape, confirming the converter UPF operation, and verifying the simulation results. Fig. 3.10(f) depicts the harmonic spectrum of input current at rated output power; the measured THD is 3.91%, and the power factor is 0.9993 almost unity. The converter measured input current THD (%), and power factor (PF) at different output powers are listed in Table 3.7. Fig. 3.10(g), and Fig. 3.10(h) depict the waveforms of output voltage, one phase input voltage, and input current for supply frequency variation from 300 Hz to 500 Hz, and from 500 Hz to 300 Hz, respectively. In both cases, the output voltage is constant, and the input current is following the input voltage. Fig. 3.10(i) depicts the waveforms of output inductor currents which are discontinuous, validating the analysis and the design. Fig. 3.10(j) depicts the intermediate transfer capacitor voltage along with its phase input voltage. As anticipated, the intermediate transfer capacitor voltage is in phase with the input voltage, and its average value is equal to the input voltage validating the assumption (3.5) and the simulation. Fig. 3.10(k) depicts the measured voltage waveform across one of the power switches. The peak voltage is around 430 V, it is equal to the sum of output voltage and peak line-to-line voltage. Fig. 3.10(l) depicts the measured voltage waveform across one of the bridge rectifier diodes. The maximum voltage stress is 270 V which is in good agreement with the analysis.

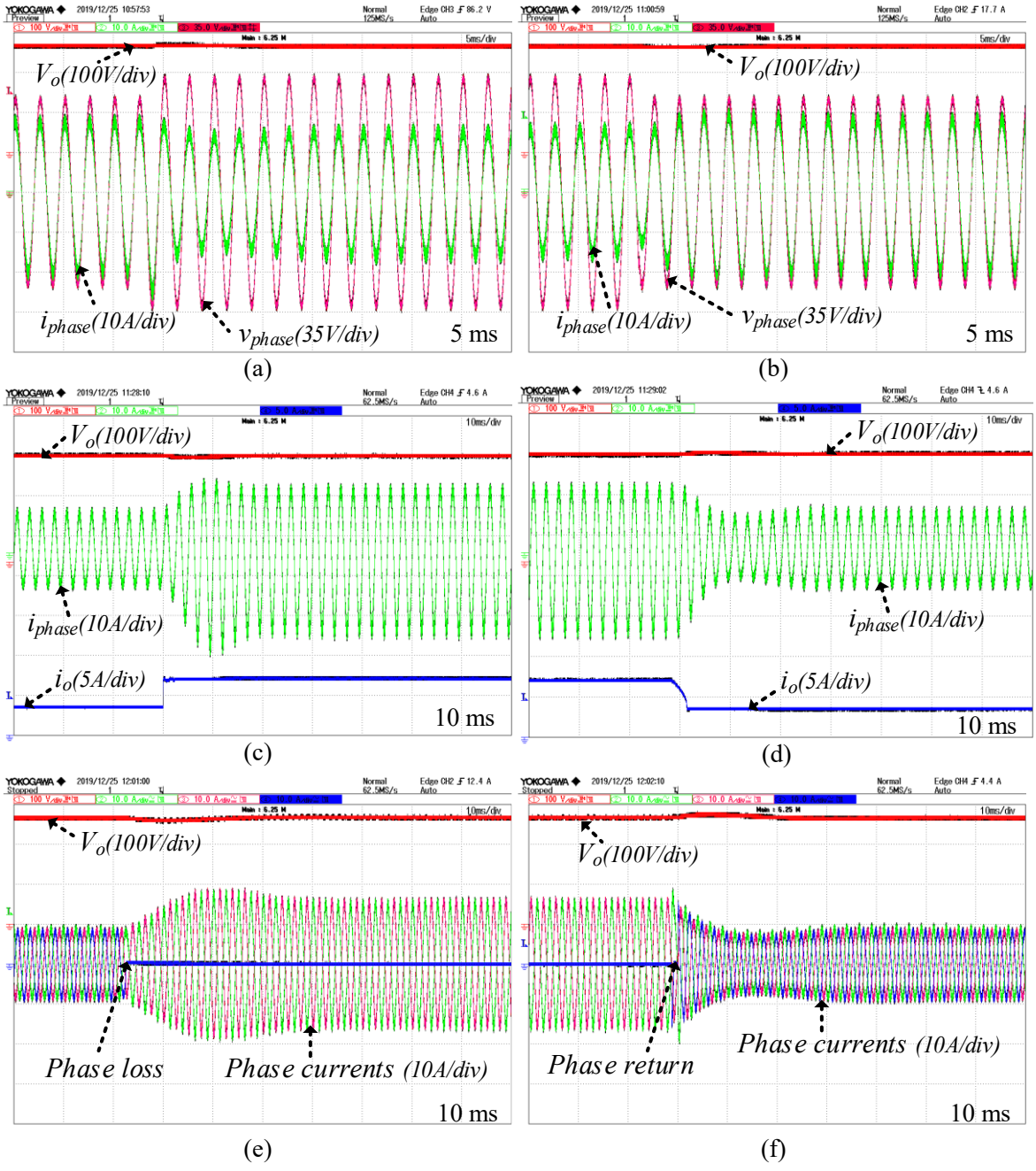


Fig. 3.11. (a), (b) Converter response for ±20 % input voltage perturbation; (c), (d) converter response for output load perturbation from 1.0 kW to 2.0 kW, and from 2.0 kW to 1.0 kW; (e), (f) converter response with single-phase loss, and return at 1.0 kW output power.

Fig. 3.11(a) and Fig. 3.11(b) depict the converter response for 20% input voltage incremental, and decremental change, respectively. The converter input current is reduced in case of input voltage incremental change whereas it is increased in case of decremental change for maintaining the input and output power balance. Fig. 3.11(c) and Fig. 3.11(d) depict the converter response for load perturbation from 1.0 kW to 2.0 kW, and from 2.0 kW to 1.0 kW, respectively. In both the cases, a small voltage dip is observed in output voltage, and it is getting settled at reference value 270 V within the designed settling time of 10 ms, which proves the robustness of the converter, and the designed controller. Fig. 3.11(e) and Fig. 3.11(f) depict the converter response with single-phase loss, and return at 1.0 kW output power, respectively. With single-phase loss, the output voltage is having second order supply frequency oscillations as in single-phase converter and is well-tracking the reference voltage.

3.7.3 Converter efficiency

Using the analytical expressions derived in section 3.5 and from the datasheet specifications of the components, the converter losses for rated and half-rated output power are calculated and listed in Table 3.8. The loss equations defined in appendix are used to calculate the losses. The converter measured efficiency curve from the developed prototype for different output power is shown in Fig. 3.12. The measured efficiency is very close to, and slightly lesser than the calculated

Table 3.8: Proposed converter itemized losses for rated and half-rated output power.

Output power	1000	2000	W
Input voltage (line-to-line rms)	110	110	V
Input current (rms)	5.586	11.156	A
Duty cycle (*d*)	0.4246	0.6005	
Losses			
Power switch losses	22.35	42.48	W
Full bridge diode losses	6.37	13.73	W
Total semiconductor losses	28.72	56.21	W
Input inductors	4.51	18.22	W
Output inductors	1.25	2.29	W
Output filter capacitors	8.29	19.78	W
Intermediate transfer capacitors	4.68	9.61	W
Auxiliary losses (core losses, skin effect,…)	15	15	W
Total power losses	62.45	121.11	W
Efficiency	94.12	94.29	%

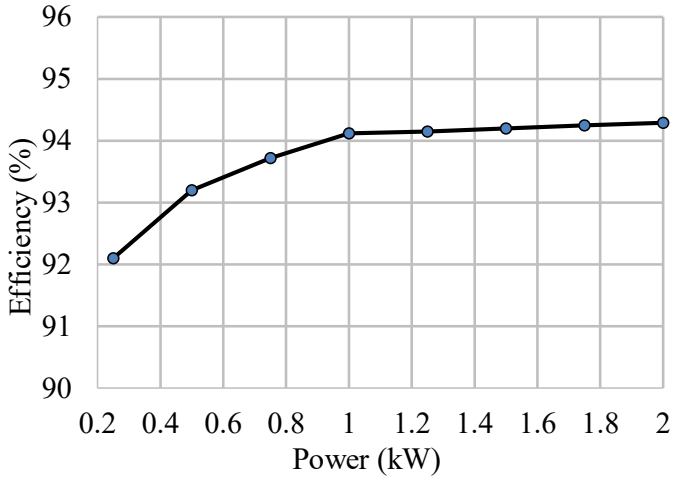


Fig. 3.12. Converter measured efficiency curve.

efficiency. It is due to some hidden losses such as core losses, and losses due to skin effect, etc., which are considered as auxiliary losses in calculation to match the measured efficiency.

3.8 Conclusion

A new three-phase Cuk-derived PFC converter with three switches connected in wye configuration is proposed. The proposed converter offers benefits of limited components for its operation and only one semiconductor from each phase is in current conduction path throughout the converter operation, which reduced the converter conduction losses, and increased the converter efficiency. The reduction in conduction losses minimizes the converter thermal management, and consequently increases the system power density. In addition, the control effort required for converter operation is very less because all the switches are driven by one common gate signal. The output inductors of the converter are designed for DCM operation for the entire power range to realize natural PFC at AC mains for wide range of frequency. Therefore, the converter control requires only one output voltage sensor which makes the system more economical, robust, simple and reliable. The converter steady-state operation and the design are presented in detail. The average and RMS currents expressions for each component are derived, and verified with the simulation. The feasibility of the proposed scheme and the design are validated with the simulation results, and further verified with the experimental results from a 2.0 kW laboratory prototype. It is shown that the results are in good agreement with the analysis and the design. An input current THD of 3.91 % (< 5 %), and a high efficiency of 94.29 % (> 90 %)

are recorded at rated output power from the developed laboratory prototype. The converter experimental results for single-phase loss fault-tolerant operation at 50 % of the rated output power has been presented. It is observed that during single-phase loss the converter losses are increased due to the high currents through the converter which caused the converter efficiency drop by 4 % when compared to the normal operation.

Chapter 4 : Three-Phase Non-Isolated Buck-Boost-derived PFC Converter

4.1 Introduction

The three-phase Cuk-derived PFC converter presented in Chapter 3 was an optimal topology in terms of semiconductors count and conduction losses. However, the converter employs two DC-link capacitors at the output, which creates extra capacitive losses. Further, the value of the intermediate energy transfer capacitor required in each phase is high to keep its voltage ripple low, and it has to handle the both input RMS current, and the output inductor current ripple which also adds to the extra capacitive losses. Therefore, with a focus on reducing the capacitive losses and also retaining the merits of Cuk-derived PFC converter, a three-phase buck-boost derived PFC converter is proposed and analyzed in this Chapter.

4.2 Proposed converter and control scheme

This section presents the derivation methodology of the proposed converter, and its merits. Further, it also presents the control scheme employed for the proposed converter.

4.2.1 The proposed converter

Fig. 4.1(a) shows the single-phase buck-boost PFC converter with inductor on AC-side for energy transfer, and a four-quadrant switch is used for PFC operation. The proposed converter shown in Fig. 4.1(b), is derived by combining the three single-phase structures of Fig. 4.1(a) into three-phase three-wire system, where a three-phase diode bridge rectifier is used in place of three single-phase diode bridge rectifiers. For a balanced three-phase system, the four-quadrant switches are no more required and just three switches (one in each phase) are sufficient and are operated synchronously, as shown in Fig. 4.1(b). The input filter capacitors, and the inductors are connected in delta-configuration, as it results in lower peak currents when compared to the wye-configuration. Moreover, in case of a single-phase failure or open-switch fault, all the inductors participate in power transfer. The proposed converter uses only one DC-link capacitor and can view it as a derived form of the three-phase Cuk-derived PFC converter with a swapping of the converter switches and the intermediate energy transfer capacitors.

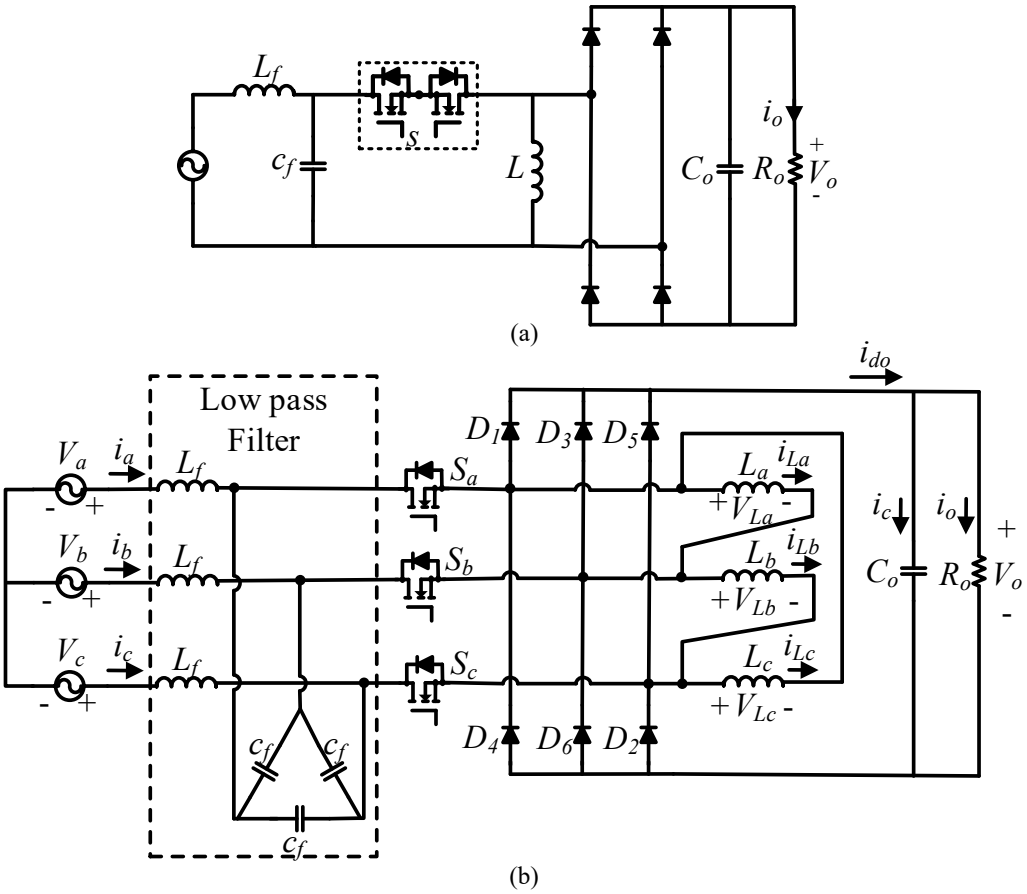


Fig. 4.1. (a) Single-phase buck-boost PFC converter with AC inductor for energy transfer; (b) the proposed three-phase buck-boost-derived PFC converter with AC inductors connected in delta-configuration.

Table 4.1: Comparison of the proposed buck-boost-derived converter with the state-of-the art buck-boost converters.

Description	**Number of semiconductors**			**Number of passive components**	**Number of semiconductors per phase in the current conduction path**		**Number of sensors**
	Switches	**Diodes**	**Total**		**Switch ON**	**Switch OFF**	
Converter [35]	3	13	14	8	3	1	5
Converter [36]	6	7	13	8	2	1	5
Converter [37]	4	6	10	10	2	2	5
Converter [38]	6	24	30	10	4	4	5
Converter [84]	4	6	10	10	1	2	1
Converter [85]	4	13	17	10	4	3	1
Converter [86]	6	24	15	12	4	4	1
Proposed Converter	3	6	9	10	1	1	1

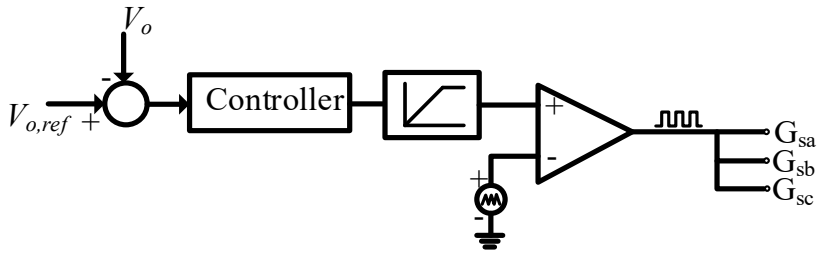


Fig. 4.2. Control circuit for the proposed converter.

To demonstrate the novelty of the proposed converter it has been compared with state-of-the art buck-boost converters and is given in Table 4.1. The comparison criteria comprise the number of switches, number of diodes, number of sensors, total number of semiconductors, total number path during both conduction and commutated states. In state-of-the art converters, at a given instant, more than one semiconductor device is in the current conduction path.

4.2.2 Control scheme

The objectives of a PFC converter are; 1) the sinusoidal input current in-phase with input voltage, 2) regulated DC output voltage. The first objective is achieved by operating the converter in DCM operation. The second objective is achieved by using a simple voltage control loop, as shown in Fig. 4.2. It is considered that all the switches are operated synchronously and the value of input inductance in each phase is the same. From the control loop, it can be seen that the duty cycle of the switches depends only on the error between the reference voltage and the output voltage means for a given output power and input voltage, the converter duty cycle is constant and it does not change with input voltage sinusoidal variation. The duty cycle changes only if there is change in output voltage reference or any disturbances viz. load change or variation in source voltage amplitude, etc.

When all the switches are on, three inductors L_a, L_b, L_c come across the line voltages v_{ab}, v_{bc}, v_{ca} respectively. Consequently, the inductor currents i_{La}, i_{Lb}, i_{Lc} begin simultaneously to rise from zero at a rate proportional to the instantaneous values of their respective line voltages. The specific inductor peak current values during each ON interval are proportional to the average values of their input line voltages during the same ON interval. Since average value of each of these line voltages varies sinusoidally, the inductor current peak and average values also vary sinusoidally. Subsequently, the line currents i_a, i_b, i_c also vary sinusoidally. The low-pass filter placed at input

side filters out the HF switching components of the line currents and presents only the fundamental average component of line currents at mains supply, which are sinusoidal and in-phase with the phase voltages.

4.3 Steady state analysis and design

In the analysis, the following assumptions are made

1. All the switches, inductors and capacitors are ideal.
2. The output filter is large enough to maintain the output voltage constant.
3. As switching frequency is much higher than line frequency, the phase voltages and output voltage are constant in a switching cycle.
4. As defined in (4.1), the input inductances in each phase are the same.

$$L_a = L_b = L_c = L\,. \tag{4.1}$$

The three-phase sinusoidal signals are divided into 12 sectors each of 30^0 as shown in Fig. 4.3. Due to the symmetric nature of the converter, its behavior is same in each sector. Hence, the analysis is presented only for sector-1 i.e. $\omega t = 0$ to $^{\pi}/_{6}$. The inductor current waveforms for one switching cycle operating in DCM in sector-1 are shown in Fig. 4.4. It should be observed that the converter has four operating modes in a switching cycle.

Mode-1: This mode starts when all the three power semiconductor switches S_a, S_b, S_c are turned-on. Prior to this mode, the input inductors L_a, L_b, L_c are in fully demagnetized state. Therefore, the switches turn-on with zero current. The equivalent circuit of the converter in this mode is shown in Fig. 4.5(a). In this mode, the input inductors store the energy owing to the line voltages appearing across the inductors, while the output capacitor supplies the load. At the end of this mode, the inductor currents reach their peak values as shown in Fig. 4.4.

Mode-2: This mode starts when the gating signals for the switches are withdrawn. The equivalent circuit of the converter in this mode is shown in Fig. 4.5(b). In this mode, the inductors L_a, L_b start to reset by delivering the stored energy to the load through diodes D_2, D_3, D_4 at a rate of $^{V_o}/_{L}$ and the inductor L_c retains its peak current value. This mode ends when the inductor L_a current i_{La} equals to the inductor L_c peak current I_{Lcp} as shown in Fig. 4.4.

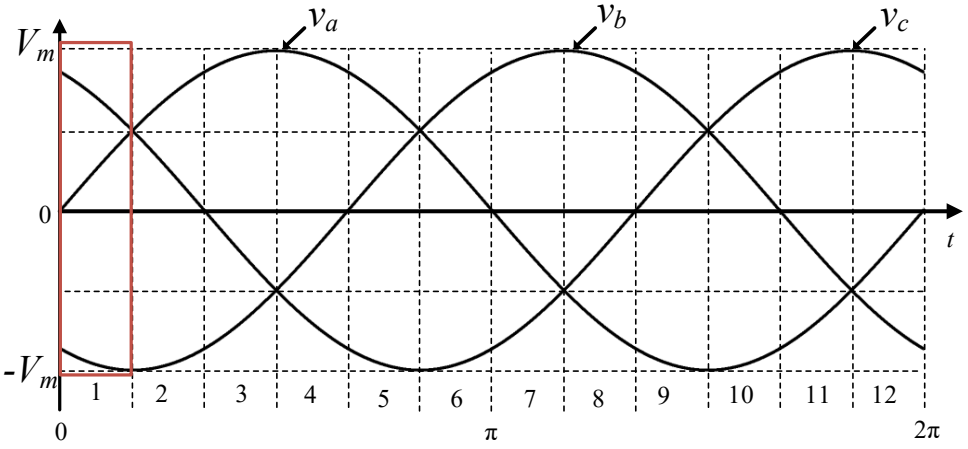


Fig. 4.3. The three-phase input voltages.

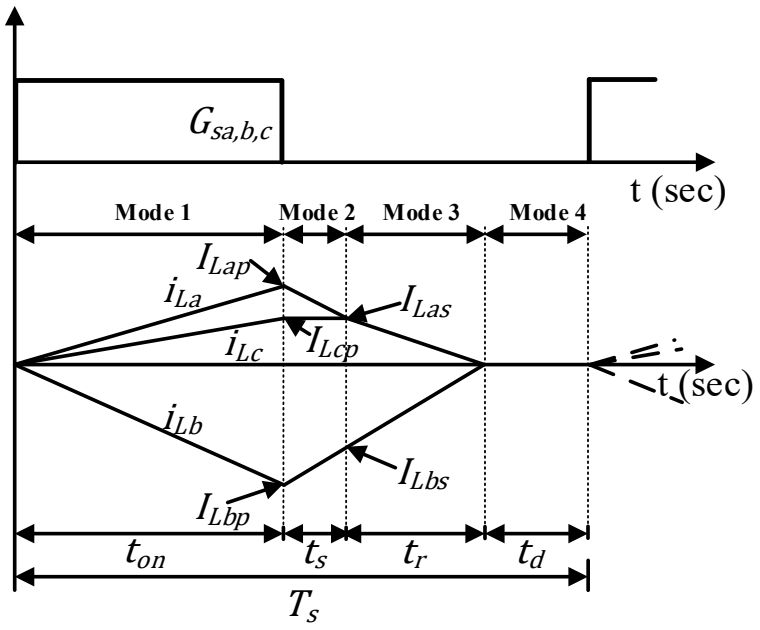


Fig. 4.4. The input inductors current waveforms in sector-1.

Mode-3: The equivalent circuit of the converter in this mode is shown in Fig. 4.5(c). In this mode, all three inductors L_a, L_b, L_c start to reset by transferring the stored energy to the load through diodes D_2, D_3 at a rate of $^{V_o}/_{2L}$, $^{V_o}/_{L}$, $^{V_o}/_{2L}$ respectively. This mode ends when all the inductors currents reach zero as shown in Fig. 4.4.

Mode-4: The equivalent circuit of the converter in this mode is shown in Fig. 4.5(d). In this mode, all the input inductors are in fully demagnetized condition and all the switches, diodes are

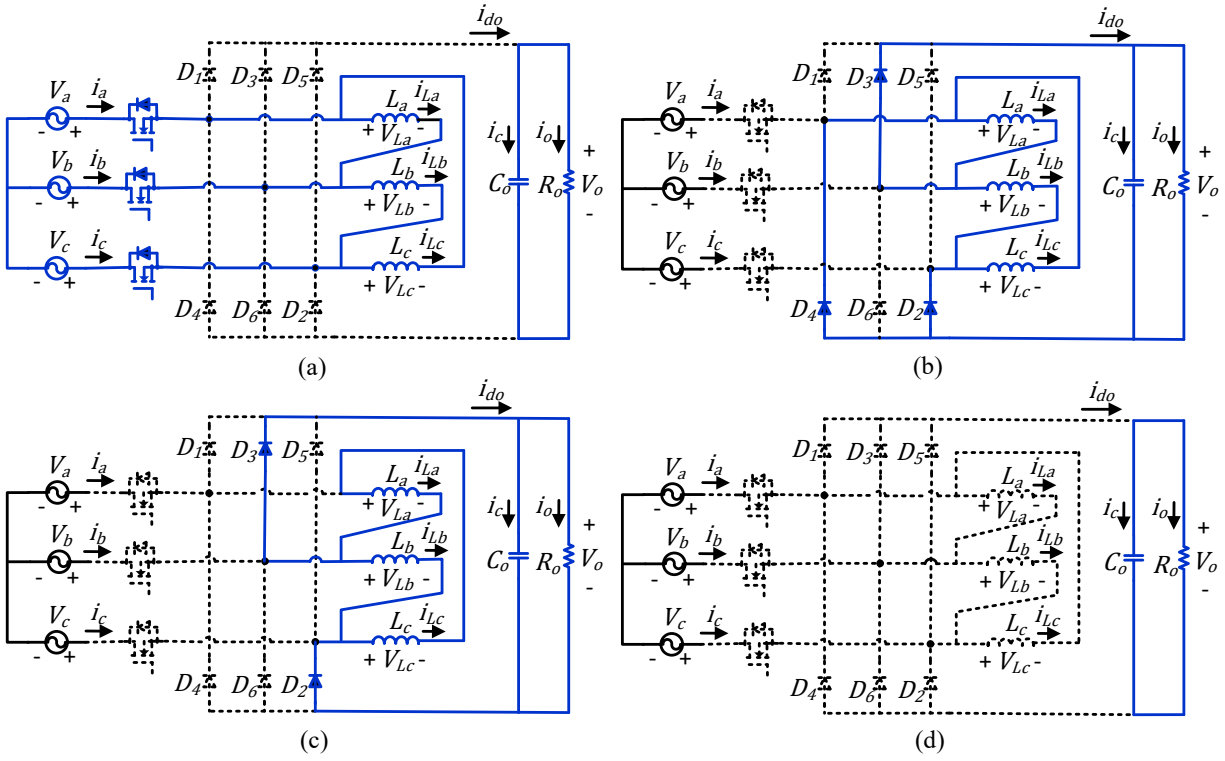


Fig. 4.5. The equivalent circuit of the proposed converter in different modes of operation (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

Table 4.2: Mathematical representation of inductor currents for different modes of operation in sector-1.

Description	**Mode-1**	**Mode-2**	**Mode-3**	**Mode-4**
$i_{La}(t)$	$i_{La}(t) = \frac{v_{ab}}{L}t$	$i_{La}(t) = I_{Lap} - \frac{V_o}{L}t$ $I_{Lap} = \frac{v_{ab}}{L}t_{on}$	$i_{La}(t) = I_{Las} - \frac{V_o}{2L}t$ $I_{Las} = \frac{v_{ca}}{L}t_{on}$	$i_{La}(t) = 0$
$i_{Lb}(t)$	$i_{Lb}(t) = \frac{v_{bc}}{L}t$	$i_{Lb}(t) = I_{Lbp} + \frac{V_o}{L}t$ $I_{Lbp} = \frac{v_{bc}}{L}t_{on}$	$i_{Lb}(t) = I_{Lbs} + \frac{V_o}{L}t$ $I_{Lbs} = -\frac{2v_{ca}}{L}t_{on}$	$i_{Lb}(t) = 0$
$i_{Lc}(t)$	$i_{Lc} = \frac{v_{ca}}{L}t$	$i_{Lc}(t) = I_{Lcp}$ $I_{Lcp} = \frac{v_{ca}}{L}t_{on}$	$i_{Lc}(t) = I_{Lcs} - \frac{V_o}{2L}t$ $I_{Lcs} = \frac{v_{ca}}{L}t_{on}$	$i_{Lc}(t) = 0$
Time period	$t_{on} = dT_s$	$t_s = \frac{3v_a}{V_o}dT_s$	$t_r = \frac{2v_{ca}}{V_o}dT_s$	$t_d = (T_s - t_{on} - t_s - t_r)$

in off state. The output filter capacitor supplies the load. This mode continues till the next switching period starts.

Following to the converter modes of operation, the converter inductor currents expressions are defined and tabulated in Table 4.2.

4.3.1 DCM operating condition

To ensure the converter DCM operation

$$t_{on} + t_s + t_r \leq T_S \,. \tag{4.2}$$

Substituting t_{on}, t_s, and t_r expressions from Table 4.2 in (4.2)

$$d \leq \frac{M}{M + \sqrt{3}\sin\left(\omega t + \frac{\pi}{2}\right)}. \tag{4.3}$$

The worst situation occurs when $\sin\left(\omega t + \frac{\pi}{2}\right) = 1$, which gives $\omega t = 0$. Therefore, to operate in DCM

$$d \leq \frac{M}{M + \sqrt{3}}. \tag{4.4}$$

From (4.4), the critical value of conversion ratio, which defines the boundary between continuous and discontinuous modes can be determined and is given by (4.5)

$$M_{cr} = \frac{\sqrt{3}\,d}{1 - d}. \tag{4.5}$$

The converter output voltage should be higher than the peak line-to-line voltage to ensure the reverse bias of bridge diodes D_1 to D_6. Hence, for a given duty cycle d, the converter is said to operate in DCM when $M > M_{cr} > \sqrt{3}$.

4.3.2 Average output current

In a switching cycle, the average current of the output filter capacitor is zero. Therefore, for the sector under the analysis, the average output current of the converter is given by

$$i_{o,avg} = \langle i_o \rangle = \langle i_{d3} \rangle . \tag{4.6}$$

The equation of i_{d3} in mode-2 is given by

$$i_{d3}(t) = i_{La}(t) - i_{Lb}(t) \tag{4.7}$$

$$i_{d3}(t) = -\frac{3v_b}{L} dT_s - \frac{2V_o}{L} t . \tag{4.8}$$

Similarly, the equation of i_{d3} in mode-3 is given by

$$i_{d3}(t) = \frac{3v_{ca}}{L} dT_s - \frac{3V_o}{2L} t . \tag{4.9}$$

From (4.8) and (4.9), the average value of output current in a switching cycle can be calculated as

$$i_{o,avg} = \langle i_{d3} \rangle = \frac{9d^2 T_s V_m^2}{4LV_o} . \tag{4.10}$$

The average output current over a line period equals to

$$I_{o,avg} = \frac{6}{\pi} \int_0^{\pi/6} i_{o,avg} \; d(wt) = \frac{9d^2 T_s V_m^2}{4LV_o} . \tag{4.11}$$

From (4.11), the normalized average output current is defined and is given as,

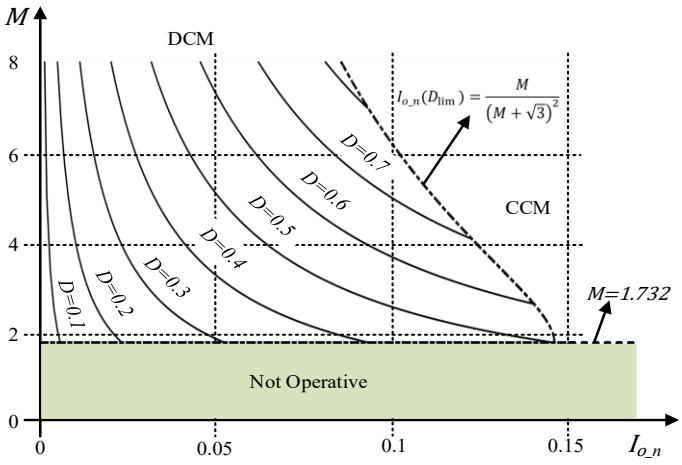


Fig. 4.6. The converter load characteristics: converter gain as a function of the normalized average output current.

$$I_{o\_n} = \frac{d^2 V_m}{V_o} = \frac{d^2}{M}. \tag{4.12}$$

Fig. 4.6 shows the converter load characteristics, is a function of converter gain and normalized average output current, is drawn by using (4.12). It is observed that the converter is tending towards CCM with the increase in the load current. For a given conversion ratio and the output power, the converter CCM operation can be avoided by setting a limit on the duty cycle, defined by (4.4).

4.3.3 Input current

The expression for phase-A input current before filtering is,

$$i_a(t) = \begin{cases} \frac{3v_a}{L} t & 0 < t \leq t_{on} \\ 0 & t_{on} < t \leq T_s \end{cases}. \tag{4.13}$$

where $v_a = V_m \sin(\omega t)$ is the instantaneous value of phase-A voltage. The Fourier series of the input current for one switching period is,

$$i_a(t) = \frac{a_0}{2} + \sum_{h=1}^{\infty} (a_h \cos(h\omega_s t) + b_h \sin(h\omega_s t)) \tag{4.14}$$

where $a_0 = \frac{3v_a}{L} d^2 T_s$, $a_h = \frac{6v_a}{h\omega_s L}\left(d \sin(2h\pi d) + \frac{1}{2h\pi}\cos(2h\pi d) - \frac{1}{2h\pi}\right)$, $b_h = \frac{6v_a}{h\omega_s L}\left(\frac{1}{2h\pi}\sin(2h\pi d) - D\cos(2h\pi d)\right)$.

On combining the harmonic current components a_h and b_h, and substituting $v_a = V_m \sin(\omega t)$,

$$i_a(\omega t) = \frac{3V_m}{2L} d^2 T_s \sin(\omega t) + \sum_{h=1}^{\infty} \frac{6V_m d}{h\omega_s L} \sin(\omega t) \sin(h\omega_s t + \delta_h) \tag{4.15}$$

where $\delta_h = \tan^{-1}\frac{b_h}{a_h}$.

The first term in (4.15) represents the fundamental current component and the second term represents the total harmonic current of input current 'i_a'. By designing a low-pass LC filter with a cut-off frequency much lower than the switching frequency, the harmonic currents can be filtered

out. Therefore, the resulting input current contains only the fundamental current component, and is given as

$$i_a(\omega t) = \frac{3V_m}{2L} d^2 T_s \sin(\omega t) = I_m \sin(\omega t) \tag{4.16}$$

where

$$I_m = \frac{3V_m}{2L} d^2 T_s \,. \tag{4.17}$$

Equation (4.16) shows that the filtered phase-A input current is sinusoidal and is in phase with the input voltage, which proves the unity power factor operation of the converter.

4.3.4 Inductor design

The inductor design should be such that it has to maintain the DCM for minimum input voltage and maximum output power (rated power) condition. Because at this condition, the converter input current is maximum, and consequently the inductor current peak also will be maximum. If the inductor can demagnetize within a switching period at this condition, then the DCM would be ensured for all the input voltages above the minimum input voltage and for all the load values below rated power. Therefore, using (4.4), the maximum duty cycle to ensure the DCM operation for minimum input voltage is given as

$$d_{max} \leq \frac{V_o}{V_o + \sqrt{3} V_{m,min}} \,. \tag{4.18}$$

The average output current for the given rated power and the rated output voltage is expressed as

$$I_o = \frac{P_o}{V_o} \,. \tag{4.19}$$

Using (4.11), (4.18) and (4.19), the value of the inductor to operate the converter always in DCM is given as

$$L \leq \frac{9}{4} \frac{d_{max}^2 V_{m,min}^2 T_s}{P_o} \,. \tag{4.20}$$

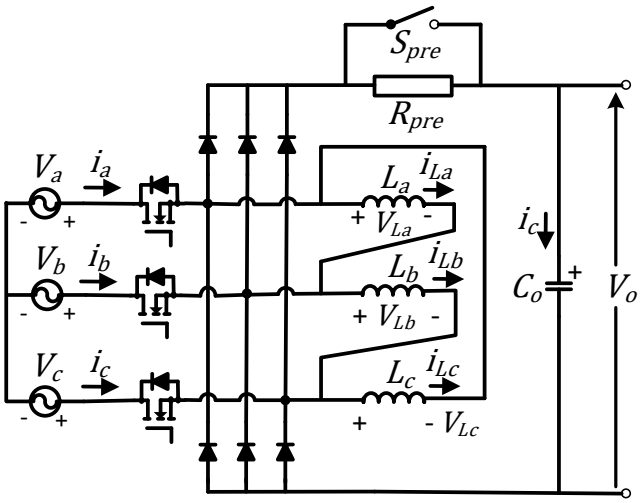


Fig. 4.7. Proposed converter with pre-charging circuit.

4.3.5 Output capacitor design

In aerospace applications, the output capacitor design depends on the power holdup time required after the AC source interruption. If t_h is the holdup time required to bring the output capacitor voltage to 90%, then the value of the output capacitance is given by

$$C_o = \frac{2P_o t_h}{(0.19V_o^2)}. \tag{4.21}$$

4.4 Converter start-up

The proposed converter requires a pre-charging circuit to limit the inrush current at start-up of the converter. A standard pre-charging circuit comprises of a pre-charge resistor, R_{pre}, and a switch, S_{pre}, is used, as shown in Fig. 4.7. During start-up, the switch, S_{pre}, is off and the pre-charge resistor, R_{pre} limits the inrush current. The switch, S_{pre}, is made ON, when the output capacitor voltage is greater than the maximum peak line-to-line voltage ($\sqrt{3}V_{m,max}$).

4.5 Component stress

4.5.1 Voltage stress

Fig. 4.8(a) shows the voltage across one of the power-mosfets for a line cycle. In each phase, the body diode of the power switch, which is in series with that phase, is forward biased for two

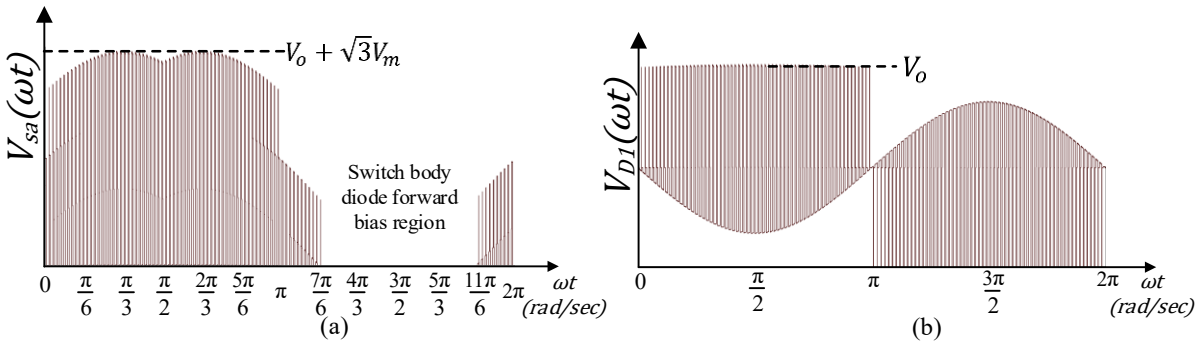


Fig. 4.8. (a) Voltage across one of power mosfet for a line cycle; (b) voltage across one of the diodes of full-bridge rectifier for a line cycle.

third of its negative cycle, when the phase negative amplitude is high. For example, the body diode of power switch S_a is forward biased from $\omega t = \frac{7\pi}{6}$ to $\frac{11\pi}{6}$ as shown in Fig. 4.8(a). During this period, the body diodes of the other two switches are reverse biased and experience a maximum voltage stress of peak line-to-line voltage plus the output voltage. Hence, the maximum voltage across the power switch is given by

$$V_{sw,max} = \sqrt{3}V_{m,max} + V_o \,. \tag{4.22}$$

Fig. 4.8(b) shows the voltage across one of the diodes of full-bridge rectifier for a line cycle. Each diode of the full bridge rectifier experiences a maximum voltage stress of output voltage V_o, when the other diode in its phase leg is ON.

4.5.2 Current stress

In this section, the analytical expressions for the average and rms currents through the power switches, diodes, inductor, and the output filter capacitor are determined.

4.5.2.1 Power switches S_a, S_b, S_c

From the converter operation, the expression for switch current in a switching cycle is given as

$$i_{sw,a,b,c}(t) = \begin{cases} \frac{3v_{a,b,c}}{L}t & 0 < t \le t_{on} \\ 0 & t_{on} < t \le T_s \,. \end{cases} \tag{4.23}$$

Using (4.23), the expressions for the average and rms currents through the power switches are determined and given as

$$I_{sw,avg} = \frac{3V_m d^2 T_s}{\pi L} \tag{4.24}$$

$$I_{sw,rms} = \frac{\sqrt{3}V_m d T_s}{L}\sqrt{\frac{d}{2}}. \tag{4.25}$$

4.5.2.2 Diodes $D_{1\ to\ 6}$

The average and rms currents through the full-bridge rectifier diodes are

$$I_{D,avg} = \frac{3d^2 T_s V_m^2}{4LV_o} \tag{4.26}$$

$$I_{D,rms} = \frac{\sqrt{3}V_m d T_s}{L}\sqrt{\frac{V_m d(3-\sqrt{3})}{\pi V_o}}. \tag{4.27}$$

4.5.2.3 Output filter capacitor, C_o

The rms current through the output filter capacitor can be calculated using

$$I_{Co,rms} = \sqrt{I_{do,rms}^2 - I_{do,avg}^2} \tag{4.28}$$

where

$$I_{do,rms} = \frac{3V_m d T_s}{L}\sqrt{\frac{2V_m d(\sqrt{3}-1)}{\pi V_o}} \tag{4.29}$$

$$I_{do,avg} = \frac{9d^2 T_s V_m^2}{4LV_o}. \tag{4.30}$$

4.5.2.4 Inductor, *L*

The expression for input inductor rms current is derived by using the input inductor equations and is given as

Table 4.3: Analytically calculated and simulated average and rms current values of active and passive devices for an output power of 2.0 kW, input line-to-line voltage of 110 V_{rms}, d = 0.6, f_s = 50 kHz, L = 65 μH.

Quantity	Calculated	Simulated
$\boldsymbol{I_{sw,avg}}$	9.50	9.38
$\boldsymbol{I_{sw,rms}}$	15.73	15.59
$\boldsymbol{I_{D,avg}}$	2.48	2.51
$\boldsymbol{I_{D,rms}}$	8.16	8.22
$\boldsymbol{I_{Co,rms}}$	13.22	13.33
$\boldsymbol{I_{L,rms}}$	11.26	11.23
$\boldsymbol{I_{cf,rms}}$	7.30	7.38

$$I_{L,rms} = \frac{V_m d T_s}{L} \sqrt{\frac{V_m d}{2\pi V_o}\left(\frac{\pi V_o}{V_m} + 4(3-\sqrt{3})\right)} \tag{4.31}$$

4.5.2.5 Filter capacitor, C_f

The rms current through the output filter capacitor can be calculated using

$$I_{cf,rms} = \frac{\sqrt{3} V_m d T_s}{2 L_{eq}} \sqrt{\frac{2d}{3} - \frac{d^2}{2}}. \tag{4.32}$$

The derived formulae from (4.24) to (4.32) are verified with the simulation. The calculated and simulated average and rms current values for an output power of 2.0 kW and input line-to-line voltage of 110 V_{rms} are listed in Table 4.3. It is observed that the calculated values are very close to the simulated values and shows high accuracy of the derived formulae.

4.6 Converter small-signal model

The small-signal model of the proposed converter is obtained by using current injected equivalent circuit approach (CIECA) [74], [75]. In this approach, the non-linear part of the circuit is linearized by injecting the average output current in a switching cycle ($i_{o,avg}$) produced by the non-linear part into the linear part as shown in Fig. 4.9.

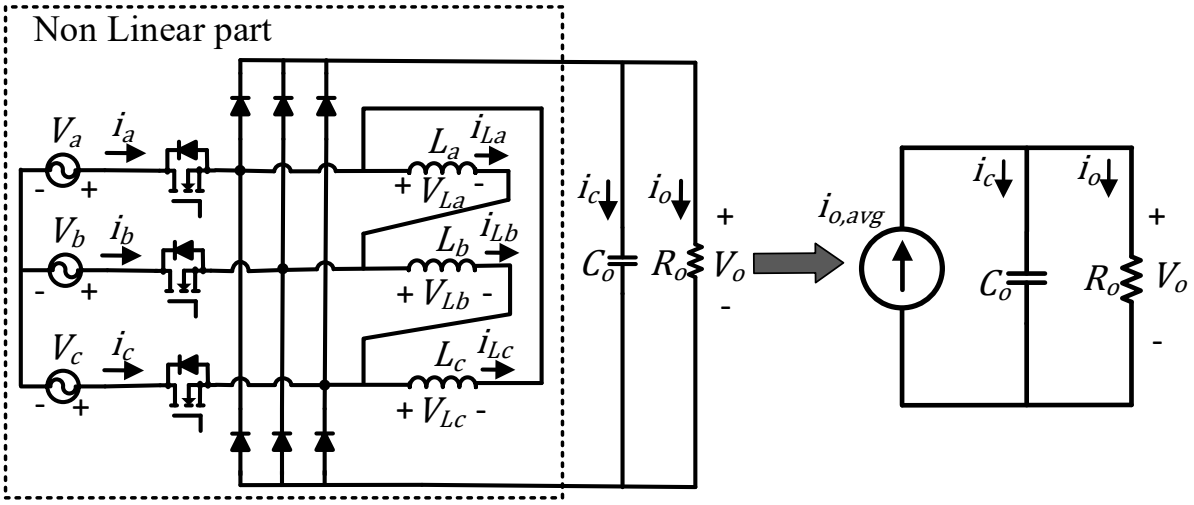


Fig. 4.9. Equivalent circuit of the converter for small-signal modeling.

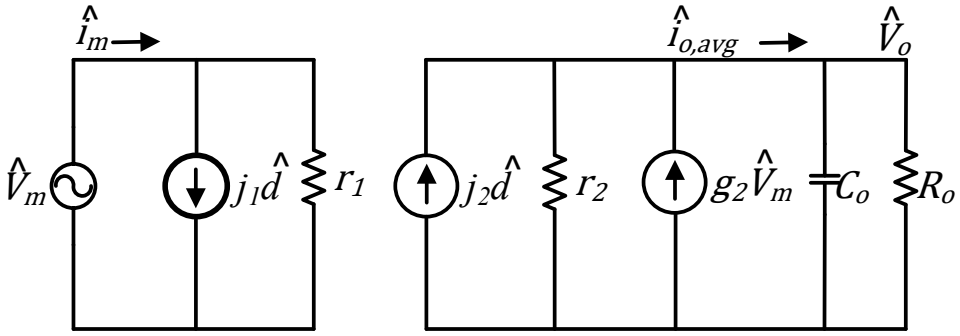


Fig. 4.10. Small signal model equivalent circuit.

Applying perturbations to (4.10), (4.17), around the steady state operating point and making the small signal approximation gives

$$\hat{\imath}_{o,avg} = j_2\hat{d} + g_2\hat{v}_m - \frac{1}{r_2}\hat{v}_o \tag{4.33}$$

$$\hat{\imath}_m = j_1\hat{d} + \frac{1}{r_1}\hat{v}_m \tag{4.34}$$

where $j_2 = \frac{9V_m^2}{v_o}\frac{dT_s}{2L}$; $g_2 = \frac{9V_m}{v_o}\frac{d^2T_s}{2L}$; $r_2 = \frac{V_o}{i_{0,avg}}$; $j_1 = \frac{3dV_mT_s}{L}$; $r_1 = \frac{2L}{3d^2T_s}$.

The equivalent small signal model described by (4.33) and (4.34) is shown in Fig. 4.10. Using Fig. 4.10, the desired transfer function can be obtained. By considering the load as resistive load,

the transfer functions for the output voltage to input voltage and the output voltage to duty cycle are expressed as

$$\frac{\hat{v}_o}{\hat{d}} = \frac{2KV_m}{1 + \frac{KV_m d}{V_o} + sR_o C_o} \tag{4.35}$$

$$\frac{\hat{v}_o}{\hat{v}_m} = \frac{2Kd}{1 + \frac{KV_m d}{V_o} + sR_o C_o} \tag{4.36}$$

where

$$K = \frac{9V_m R_o d T_s}{4V_o L}. \tag{4.37}$$

4.7 Input filter design

The criteria for the low-pass filter design are:

1) selection of cut-off frequency, f_c

$$f_c = \frac{1}{2\pi}\sqrt{\frac{3}{L_f C_f}} \tag{4.38}$$

2) minimization of filter reactive power consumption for the supply frequencies at rated output power. This is possible when the filter characteristic impedance is equal to the converter input impedance i.e.,

$$Z_c = \sqrt{\frac{3L_f}{C_f}} = Z_{in} \tag{4.39}$$

where Z_c is characteristic impedance = $\sqrt{\frac{3L_f}{C_f}}$, and Z_{in} is converter input impedance at rated output power = $\frac{2L}{3d^2 T_s}$.

Using (4.38), and (4.39), the expressions for the low-pass filter parameters are obtained as

Table 4.4: Input specifications.

Parameter	Value
Input line voltage	110 V ± 15%
Input frequency, $\boldsymbol{f}$	360-800 Hz
Output power, $\boldsymbol{P_o}$	2.0 kW
Output voltage, $\boldsymbol{V_o}$	270 V
Switching frequency, $\boldsymbol{f_s}$	50 kHz

Table 4.5: Designed parameters.

Parameter	Value
Maximum Duty cycle, $\boldsymbol{D_{max}}$	0.685
Input inductance, $\boldsymbol{L}$	60 μH
Output capacitance, $\boldsymbol{C_o}$	1.44 mF
Filter inductance, $\boldsymbol{L_f}$	120 μH
Filter capacitance, $\boldsymbol{C_f}$	1.1 μF

$$L_f = \frac{Z_c}{2\pi f_c} \tag{4.40}$$

$$C_f = \frac{1}{6\pi f_c Z_c}. \tag{4.41}$$

4.8 Results and discussion

This section presents the simulation and experimental results of the proposed converter along with a discussion on converter efficiency.

4.8.1 Simulation results

The proposed converter shown in Fig. 4.1(b) is simulated in PSIM 11.1 software to confirm the converter analysis and the design. The converter specifications are given in Table 4.4. Substituting given specifications in (4.20), the input inductor value L is calculated. It should be less than 62 μH to operate the converter in DCM. In view of converter losses, the converter is simulated with input inductor value of $L = 60$ μH. The output capacitance value is calculated from the holdup time required which is considered at 2.5 ms. The input filter is designed for a cut-off frequency 8 kHz. The results of the design are given in Table 4.5. From (4.35) and by using the designed parameters, the converter transfer function G(s) is obtained and is given by (4.42). A proportional-integral controller described by (4.43) is designed for a gain cross-over frequency of 625 rad/sec with a phase margin 75^0 and infinity gain margin. The open loop transfer function described by (4.44) has -20 db slope at zero cross-over frequency for all the loads below rated load. This indicates the system stability for all the load conditions below rated load

$$G(s) = \frac{v_o(s)}{d(s)} = \frac{1062}{0.05249\,S + 2.278} \tag{4.42}$$

$$H(s) = 0.0296 + \frac{6.293}{S} \tag{4.43}$$

$$G(s)H(s) = \frac{598.78(S + 212.57)}{S(S + 43.39)}. \tag{4.44}$$

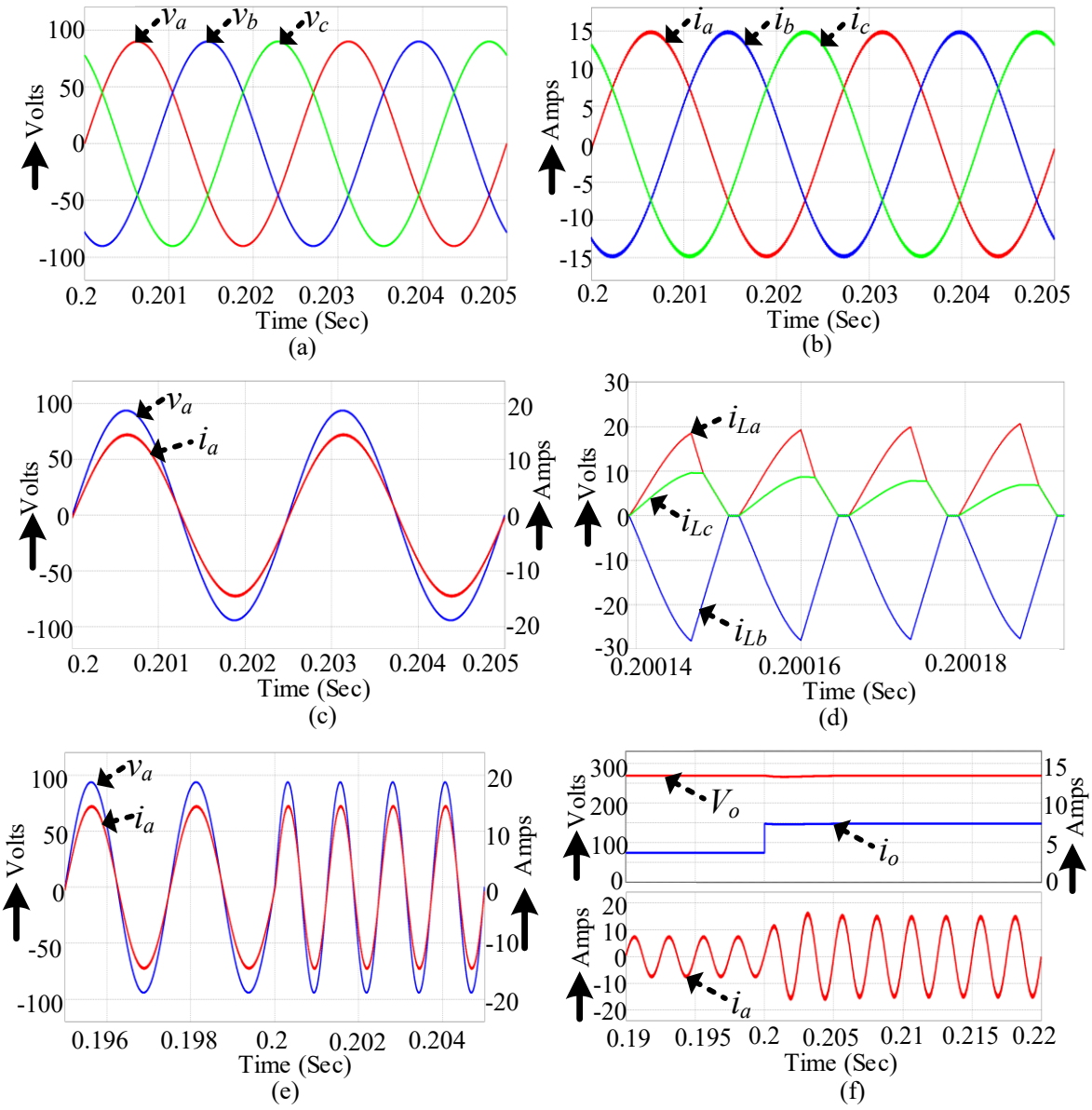


Fig. 4.11. Simulation results (a) input phase voltages; (b) input phase currents; (c) phase-A voltage and current; (d) input inductor currents; (e) output voltage and phase-A input current for load disturbance from 50% to 100% of rated power; (f) phase-A voltage and current for input frequency variation 400 Hz to 800 Hz.

With the designed parameters and the designed controller, the circuit is simulated, and the results are presented for input frequency f = 400 Hz. The simulated three-phase input voltage and current waveforms are shown in Fig. 4.11(a) and Fig. 4.11(b), respectively. The currents are sinusoidal and balanced. The phase-A voltage and current waveforms are shown in Fig. 4.11(c). The input current is in-phase with the input voltage, confirming the UPF operation of converter. The input inductor current waveforms are shown in Fig. 4.11(d). The inductor currents are discontinuous and following the analysis. The input voltage and input current of the converter for supply frequency variation from 400 Hz to 800 Hz are shown in Fig. 4.11(e). The input current is following the input voltage during supply frequency variation. The output voltage and input current of the converter when subjected to a load step change from 50% to 100% of the rated power are shown in Fig. 4.11(f). It is observed that the output voltage is closely tracking the reference voltage and settled within the settling time of 10ms, which confirms the robustness of the converter and the controller design.

4.8.2 Experimental results

To validate the reported analysis, and control, and to verify the simulation results a 2.0 kW proof-of-concept laboratory hardware prototype is developed and is shown in Fig. 4.12. The hardware prototype details are provided in Table 4.6. The designed controller is implemented in DSP TMS320F28335 and the output DC voltage is sensed by using hall-effect voltage sensor LV 25-P. The reference voltage is compared with the measured voltage, and the error signal is fed to

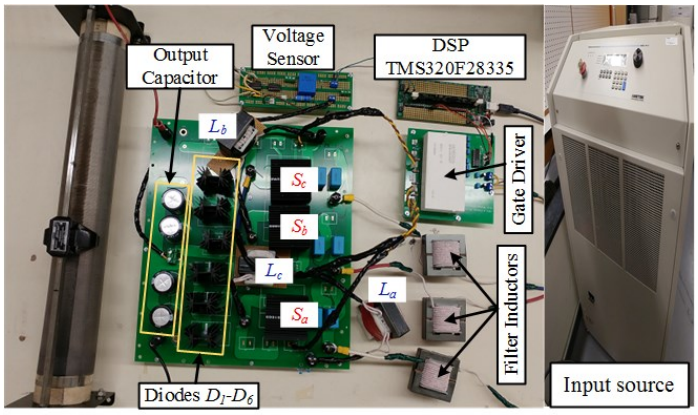


Fig. 4.12. Experimental prototype of the proposed converter.

Table 4.6: Experimental setup component specifications.

Component	Specifications
Input source	California–MX30 (300-500 Hz)
Switches,	UJ3C065030K3S, 650 V, 62 A, 35 mΩ
Diodes	VS-65EPF06LHM3, 600 V, 65 A
Output capacitor	ESMQ451VSN471MR45S, 4 x 470 μF
Filter capacitors	PHE845VY6220MR06L2, 5 x 0.22 μF
Filter and input inductors	55 x 28 x 21, EE Ferrite cores
Snubber capacitor	R75QD0470DQ30J, 470 pF
Snubber Resistor	SQP500JB-1K6, 1.6 $k\Omega$
Gate driver	Semicron SKHI 61(R)

the designed controller to generate the control signal. The control signal is basically the duty cycle fed to the saturation block, where the upper limit is set to the value defined by (4.18). The duty cycle reaches its upper limit during overloads and it is capped to this limit to protect the converter against overloads and to avoid the converter CCM operation. As a result, the output voltage will drop accordingly. The output of the saturation block is compared with a sawtooth waveform of frequency 50 kHz to generate the gate signal and it is fed to all three power switches. The experimental results are presented for input frequency f = 400 Hz.

The measured three-phase input voltage waveforms for input frequency f = 400 Hz are shown in Fig. 4.13(a). The measured phase input currents and output voltage waveforms at 1.0 kW output power are shown in Fig. 4.13(b). The input currents are sinusoidal, and the output voltage is settled at 270 V. The measured input voltage and input current waveforms for one phase at 0.5, 1.0, 1.5, and 2.0 kW output power are shown in Fig. 4.13(c), Fig 4.13(d), 4.13(e) and Fig 4.13(f), respectively. It should be observed that the phase input current is sinusoidal and is in phase with input voltage for varying output power, which confirms the UPF operation of the converter. The output voltage and the phase input current of the converter for frequency change from 350 to 500 Hz at 1.0 kW output power are shown in Fig. 4.13(g). The output voltage is constant at 270 V, and the input current is in-phase with the input voltage during input frequency change, same as in the simulation. The input inductor current waveforms are shown in Fig. 4.13(h) and they are discontinuous, which validates the reported analysis and the design. The measured switch voltage and switch current waveforms for a switch are shown in Fig. 4.13(i) and Fig. 4.13(j), respectively,

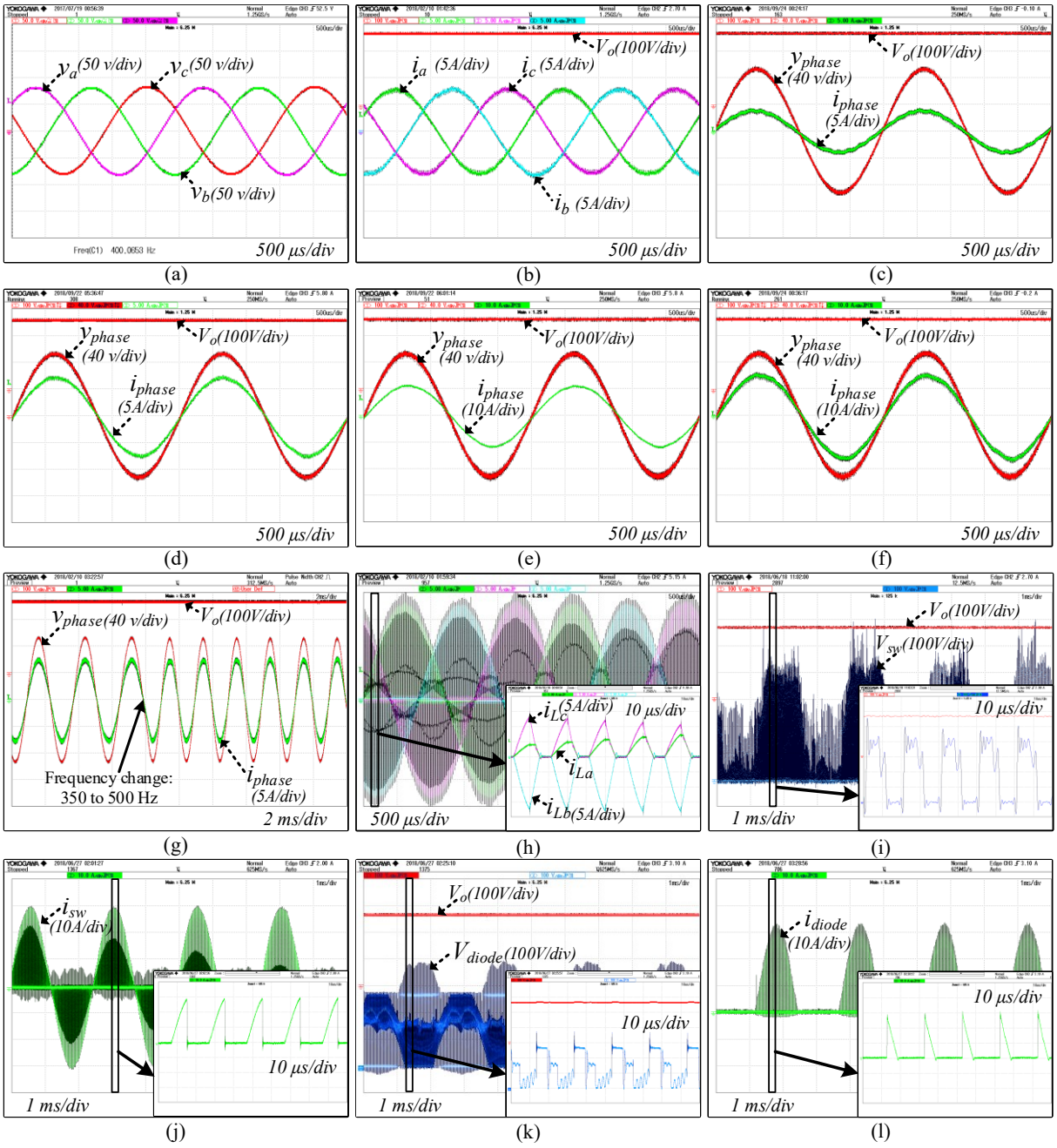


Fig. 4.13. Experimental results: (a) phase input voltages, 400 Hz; (b) phase input currents, and output voltage, at 1.0 kW output power; (c) phase input voltage, phase input current at 0.5 kW output power; (d) phase input voltage, phase input current at 1.0 kW output power; (e) phase input voltage, phase input current at 1.5 kW output power; (f) phase input voltage, phase input current at 2.0 kW output power; (g) the converter output voltage, and input current for supply frequency change 350 to 500 Hz; (h) input inductor currents; (i) voltage across one of the power switches; (j) current through one of the power switches; (k) voltage across one of the of the full-bridge rectifier diodes; (l) current through one of the full-bridge rectifier diodes.

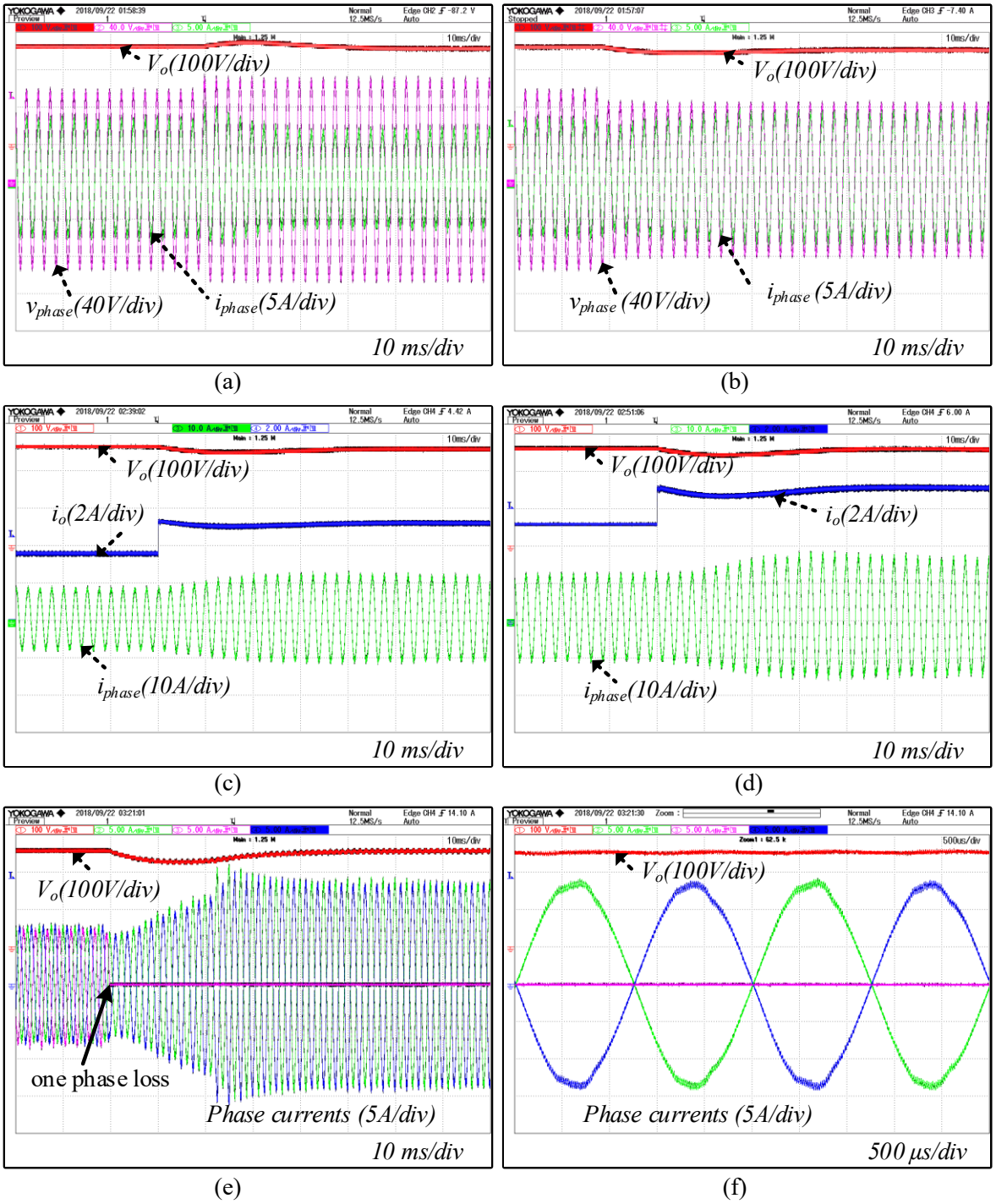


Fig. 4.14. (a), (b) The converter output voltage, input voltage, and input current for 15% increase, and for 15% reduction in nominal phase input voltage; (c), (d) the converter output voltage, output current, and input current for load step change from 1.0 kW to 1.5 kW and from 1.5 kW to 2.0 kW; (e) the converter output voltage, and input currents for one phase loss at 1.0 kW output power; (f) the zoomed version of converter response during single-phase loss.

and the measured diode voltage and diode current waveforms for a diode of the full-bridge rectifier are shown in Fig. 4.13(k) and 4.13(l), respectively, and they are in close agreement with the analysis.

To verify the robustness of the controller, the proposed converter is subjected to two disturbances. The first one is the change in the input-phase voltage and the second one is a load-step change. Fig. 4.14(a) and Fig 4.14(b) show the converter response for 15% increase and for 15% reduction in the phase input voltage, respectively. Fig. 4.14(c), and Fig. 4.14(d) show the converter response for load step change from 1.0 kW to 1.5 kW and 1.5 kW to 2.0 kW, respectively. In all the cases, it is observed that the output voltage is closely following the reference voltage and getting settled within the designed settling time.

Moreover, the proposed converter configuration allows it to operate in case of a single-phase failure or open-switch fault, which is required for MEA application. With a phase loss, the converter can be considered as a single-phase converter with a line-to-line voltage applied at input, and the converter can deliver 50% of the rated power. The reduction in deliverable power is due to the maximum duty cycle limit. The converter response with a phase loss at 1.0 kW output power is shown in Fig. 4.14(e). It is observed that the output voltage is settled at 270 V and is having the second order harmonic oscillations like a single-phase PFC converter. Since the converter is still operating in DCM during single phase loss, the input current contains the fundamental component and higher switching order harmonics. Therefore, the filtered input currents contain only the fundamental components, which are sinusoidal and are in-phase, opposite polarity to each other to ensure the zero sum as shown in Fig. 4.14(f).

4.8.3 Converter efficiency

Table 4.7 lists the calculated loss breakdown for each component of the proposed converter for rated and half-rated output power. The losses are calculated using the analytical expressions derived in section 4.5 and based on the components datasheet parameters. The measured efficiency curve of the proposed converter for different output power is shown in Fig. 4.15. It is observed that the calculated efficiencies are in good agreement with the measured efficiencies. The measured efficiencies are little bit low when compared to the calculated efficiencies due to some hidden losses such as ferrite core losses, and losses due to skin effect etc, and the same has been considered as constant auxiliary losses in the calculation.

Table 4.7: Calculated loss breakdown of the proposed converter for rated and half-rated output powers.

Output power	1000	2000	W
Input voltage (line-to-line rms)	110	110	V
Input current (rms)	5.468	11.03	A
Duty cycle (*d*)	0.423	0.6	
Losses			
Power switch losses	17.01	35.13	W
Full bridge diode losses	6.24	13.64	W
Total semiconductor losses	23.25	48.77	W
DCM inductor	2.694	7.22	W
Output filter capacitors	4.035	10.01	W
Input Filter capacitors	1.582	3.70	W
Filter inductors	2.242	9.18	W
Auxiliary losses (snubber, skin effect,…)	15	15	W
Total power losses	48.8	93.88	W
Efficiency	95.34	95.52	%

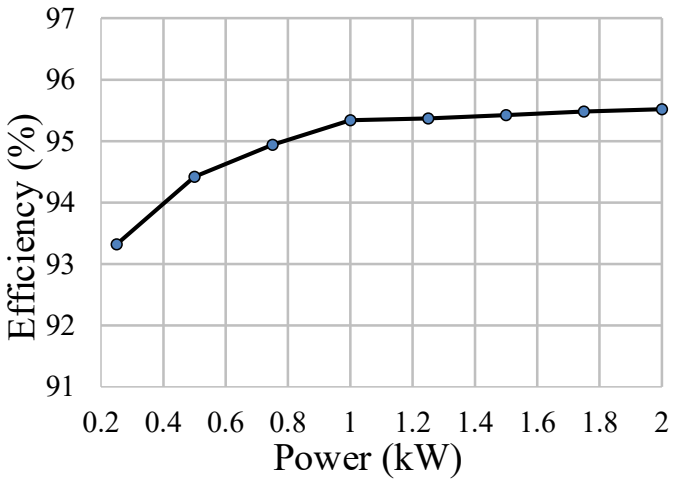


Fig. 4.15. Measured efficiency curve for different output powers.

The harmonic spectrum of input current at 1.0 kW output power for input frequency of f = 400 Hz is shown in Fig. 4.16. The input current THD is 3.43 % and measured input PF is 0.9994. The input current THD (%) and the power factor (PF) of the converter for different output power levels for input frequency f = 400 Hz are listed in Table 4.8. It is observed that the converter power factor is 0.999 (almost unity) and input current THD is less than 4%.

Table 4.8: Input current THD (%) and power factor of the proposed converter for different output powers.

P_o, kW	THD (%)	PF
0.5	3.56	0.9993
0.75	3.49	0.9993
1.0	3.43	0.9994
1.25	3.30	0.9995
1.5	3.05	0.9995
1.75	2.87	0.9996
2.0	2.76	0.9996

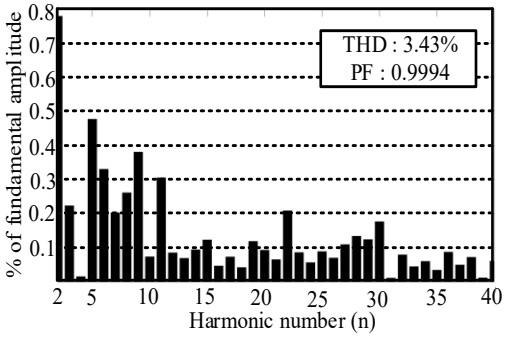


Fig. 4.16. Input current harmonic spectrum at 1.0 kW output power.

4.9 Conclusion

A new three-phase buck-boost derived PFC converter with inductors connected in delta-configuration is proposed in this Chapter. The proposed converter employs only three power switches and all the switches are driven by the same gate signal. The converter is operated in DCM to achieve PFC at the ac input for wide range of frequency. The converter requires only one output voltage sensor, which makes the system cost-effective, reliable and robust. The steady-state operation of the converter, detailed design calculations are presented. The analytical expressions for each component stress are derived to simplify the converter design. The small-signal model of the converter is derived by using CIECA approach to aid the controller design.

The simulation results from PSIM 11.1 software, and the experimental results from a 2.0 kW laboratory prototype are presented to confirm the operation of the proposed converter. The results demonstrate that the input currents are sinusoidal, and the converter achieved UPF operation for wide range of output power and input supply frequency. The converter is subjected to the input voltage disturbance and load step change. In both the cases, the output voltage is closely tracking the reference voltage and getting settled within the designed time. It is also shown that the proposed converter will be in operation in case of a single phase open fault and provides 50% rated power during fault condition without changing the controller structure. From the developed hardware prototype, an input current THD of 2.76 % (< 5 %) and a high efficiency of 95.52 % (> 90 %) are recorded at rated output power.

Chapter 5 : Three-Phase Interleaved Non-Isolated Buck-Boost Derived PFC Converter

5.1 Introduction

In general, the DCM operation bounds the converter operating range due to its low inductance generates high current peaks through switches and diodes, which consequently necessitates high-current rated semiconductor components, and also large filters size. However, these limitations can be overcome by adopting interleaved technique [87]-[90]. Interleaving is a popular approach in power electronics connecting two or more identical converter cells in parallel at input and output sharing the total power equally. Thus, the power processed by each converter cell will be reduced, which further reduces the current peaks through the semiconductor components. To reduce the filter size, the gate signals for each interleaved cell are phase-shifted by $^{360^o}/_{n}$, where *n* is the number of interleaved converter cells [91]. The phase-shifting of the gate signals also phase-shifts the input currents in each switching cycle connected to the same phase. Therefore, the effective line input current in a switching cycle, which basically is the sum of the currents drawn by the phase-shifted interleaved cells connected to the same line, will present a lower input current ripple due to ripple cancellation. Further, the dominant high frequency harmonic of the effective line input current is no more around f_s, it is around nf_s, where f_s is the switching frequency. As a result of the reduced input current ripple and incremental increase in the effective ripple frequency, the filter requirement gets reduced and is designed for a higher cut-off frequency to realize the same power quality, which improves the system power density. Therefore, considering the merits of the interleaved technique, an interleaved version of the three-phase buck-boost derived PFC converter is studied and analyzed in this Chapter. Further, the benefits of the proposed interleaved converter are demonstrated by comparing it with the single-cell three-phase buck-boost derived converter reported in Chapter 4 for the same operating conditions.

5.2 Proposed converter and control scheme

The proposed three-phase interleaved buck-boost derived PFC converter is shown in Fig. 5.1, which is formed by connecting two cells of three-phase buck-boost derived PFC converter presented in Chapter 4 in parallel at both the input and the output. Two extra output switches S_{1o}, S_{2o} are added at the output of each full-diode bridge rectifier to make the cells operate

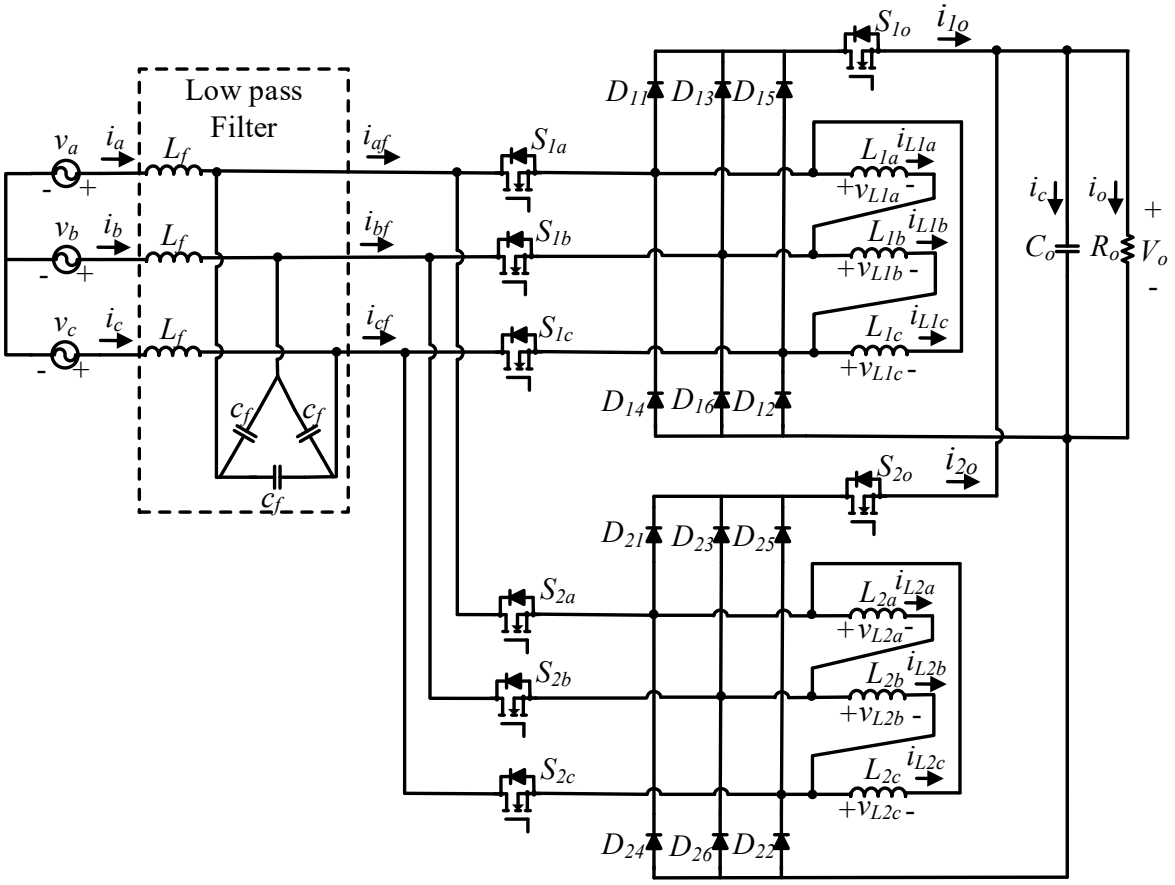


Fig. 5.1. The proposed three-phase interleaved buck-boost derived PFC converter.

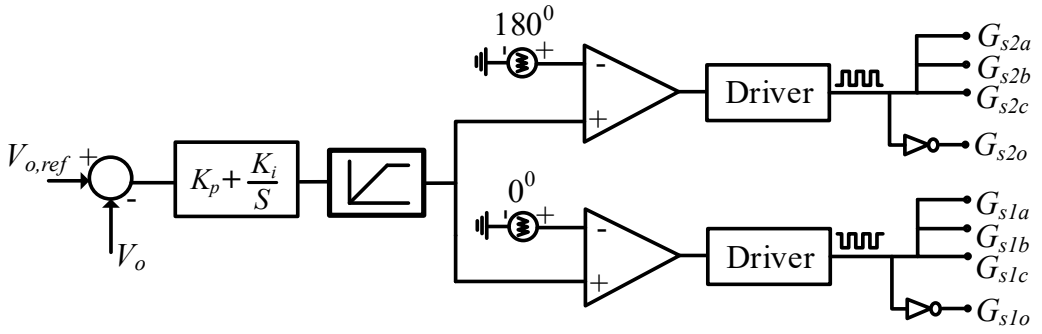


Fig. 5.2. The control circuit to generate the gate signals for all the switches of interleaved converter.

independently. The output switches are operated complementary to the corresponding converter cell input switches so that it avoids the interaction between two converter cells. Each interleaved unit is operated in DCM to realize the natural PFC at AC mains. Fig. 5.2, depicts the control strategy for the proposed converter. It is just a single voltage loop control for output voltage

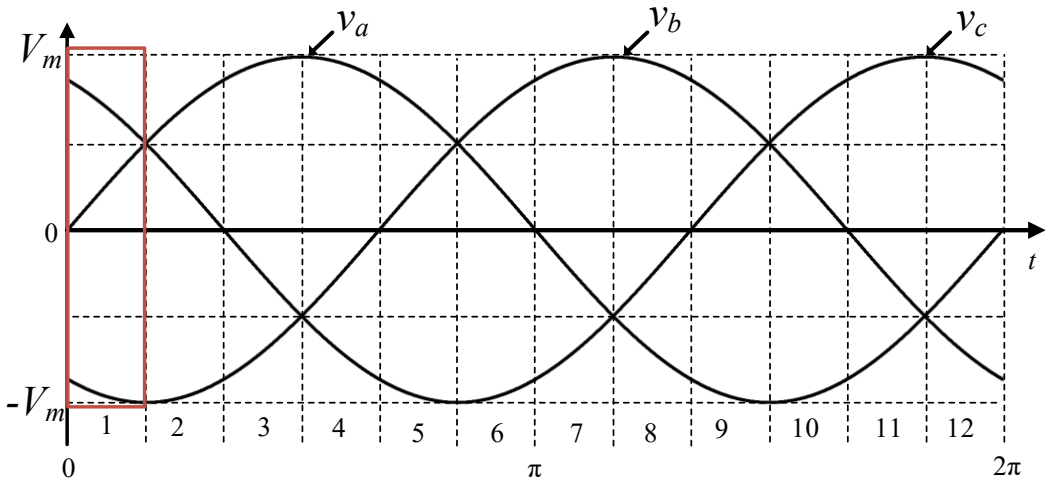


Fig. 5.3. Twelve sectors of one supply time period.

regulation, therefore it requires only one voltage sensor. All the input switches of both the cells are operated with the same duty ratios but the operation of one cell with respect to the other cell is phase-delayed by 180^0. This way, the resultant input current ripple amplitude is reduced, and the effective ripple frequency is doubled, which further helps in reducing the input and output filter requirements.

5.3 Converter steady state analysis and design

In the analysis, it is assumed that all the components are ideal and lossless. The output capacitor is large enough to keep the output voltage ripple within the defined limits in a switching cycle. It is also assumed that the input voltages and output voltage are constant within a switching cycle. To maintain the converter symmetricity, it is considered that all the input inductance values of both the cells are same as defined in (5.1).

$$L_{1a,b,c} = L_{2a,b,c} = L \tag{5.1}$$

The supply time period is divided into twelve sectors as shown in Fig. 5.3. Since the converter is symmetric, the analysis is presented only for sector-1. The same analysis is valid for remaining supply period as well. The input inductors current waveforms of both the interleaved cells for duty cycle $d \leq 0.5$ and $d > 0.5$ are shown in Fig. 5.4, and Fig. 5.5, respectively. It is observed that in both the cases, the two interleaved cells are working independently, and there is no interaction

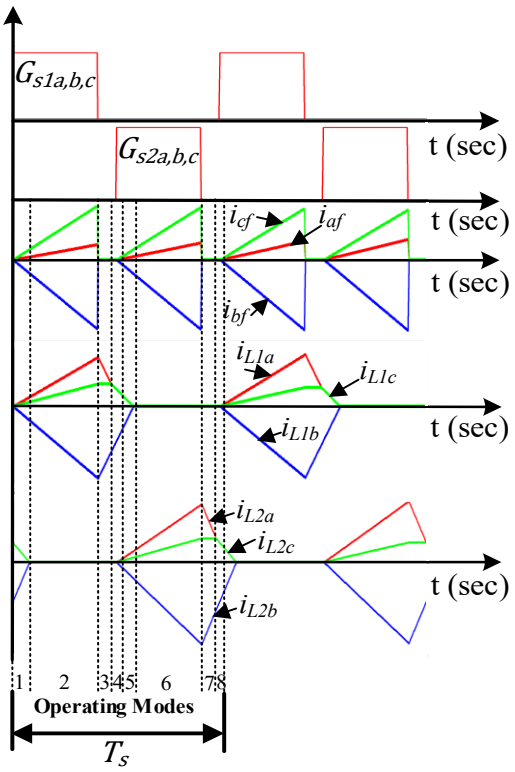


Fig. 5.4. The converter current waveforms for duty cycle $d \leq 0.5$.

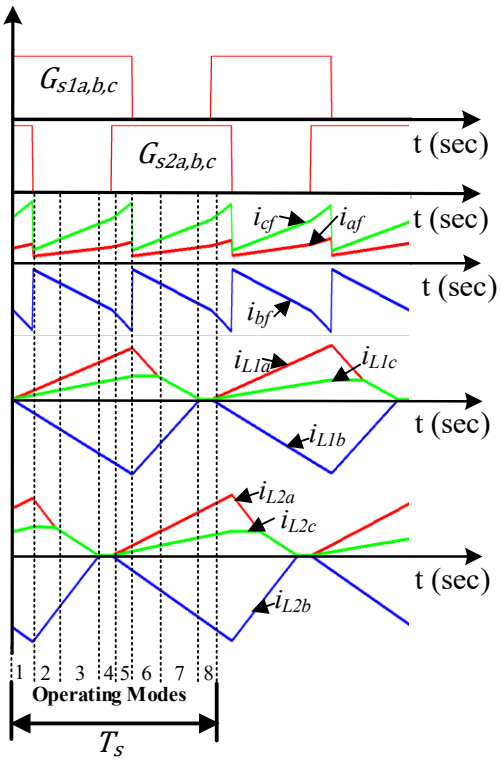


Fig. 5.5. The converter current waveforms for duty cycle $d > 0.5$.

between them. It is also observed that in both the cases the converter exhibits total eight modes of operation and the input current ripple frequency is twice of the switching frequency. Since the converter operation is same for $d \leq 0.5$ and $d > 0.5$, the converter steady state operation is explained only for $d > 0.5$.

1st Mode: This mode triggers when gate signals to input switches of the first cell are supplied. Before starting this mode, the input inductors of first cell are in fully demagnetized state, whereas the input inductors of the second cell are storing energy according to the input voltages at that instant because the input switches of the second cell are already in closed position. Since the input switches of the first cell are closed, the input inductors start storing the energy according to the input voltages appeared across them. As the output switches of both the cells are in open position, the load is supplied by the output capacitor. The equivalent circuit of the converter operating in this mode is shown in Fig. 5.6(a). This mode ends when the gate signals to the input switches of the second cell are withdrawn.

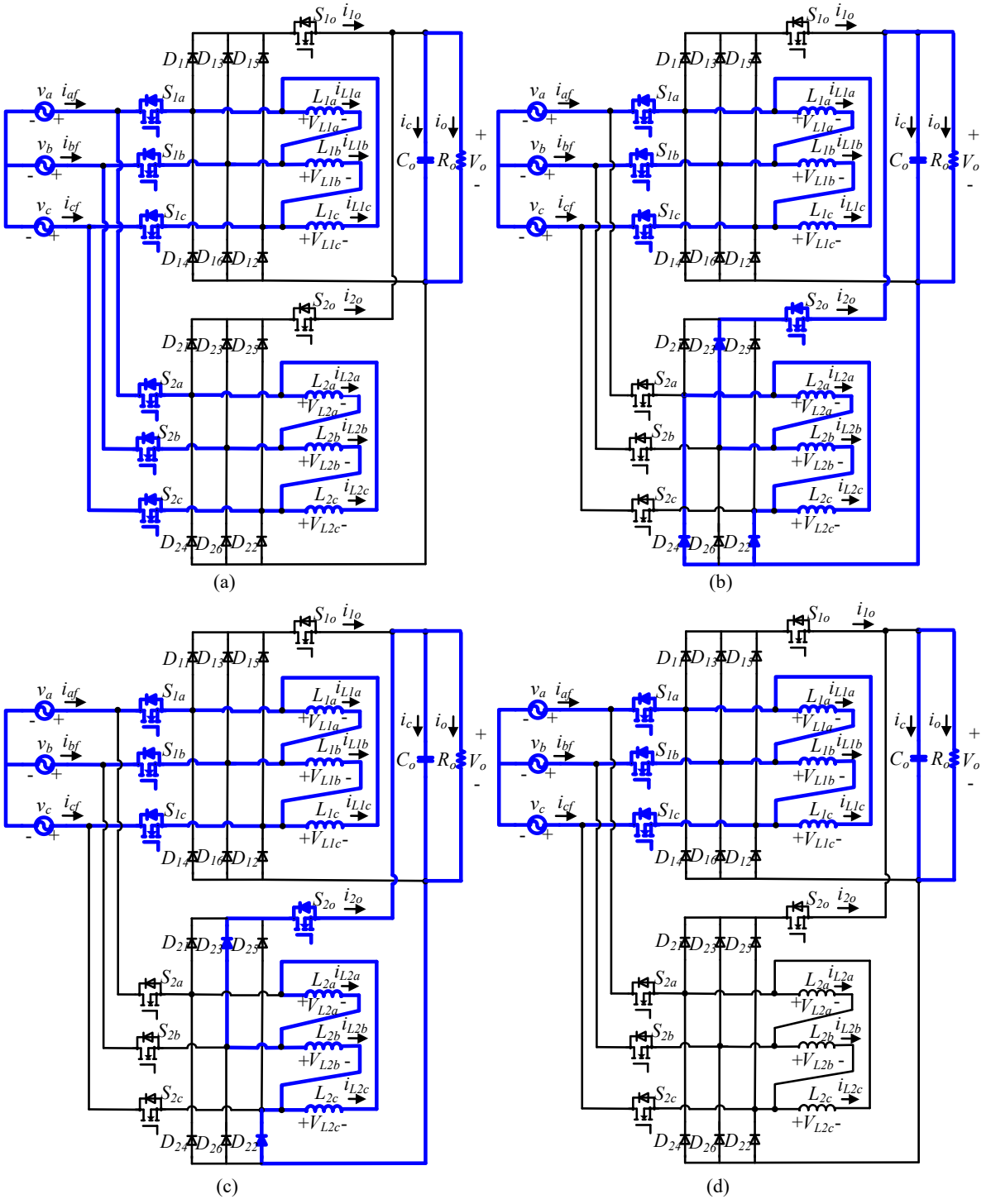


Fig. 5.6. Converter equivalent circuits (a) 1st mode; (b) 2nd mode; (c) 3rd mode; (d) 4th mode.

2nd Mode: In this mode, the second cell input switches are opened, and its output switch is closed. Therefore, the second cell inductors start demagnetizing by delivering the stored energy to the load via diodes D_{22}, D_{23}, D_{24}, whereas the input inductors of the first cell are in the same state as in 1st mode. The equivalent circuit of the converter operating in this mode is shown in Fig. 5.6(b). This mode ends when the inductor L_{2a} current equals to the inductor L_{2c} current.

3rd Mode: In this mode, the switching states are the same as in 2nd mode except the diode D_{24} that goes to OFF state from ON state. The inductors of the first cell are storing energy and the inductors of the second cell are demagnetizing by giving the stored energy to the load only via diodes D_{22}, D_{23}, as shown in Fig. 5.6(c). This mode ends when all the inductors of the second cell are fully demagnetized.

4th Mode: In this mode, all the inductors of second cell are in demagnetized state, and the inductors of the first cell are still storing energy as the input switches of first cell are in ON state. Since, there is no power transfer from input to output from either of the cell, the load is supplied by the output capacitor. The equivalent circuit of the converter operating in this mode is shown in Fig. 5.6(d).

5th Mode: This mode starts when gate signals to input switches of the second cell are supplied. Since the second cell inductor currents are starting from zero, the input switches are turning-on with zero current. Therefore, the second cell switches turn-on losses are zero, and the same is true for the first cell as well. In this mode, the input inductors of the first cell are in the same state as in the previous mode i.e. storing energy whereas the second cell input inductors start to store energy according to the input voltages appeared across them. As the output switches of both cells are in open position, the load is supplied by the output capacitor. The equivalent circuit of the converter operating in this mode is shown in Fig. 5.7(a). This mode ends when the gate signals to the input switches of the first cell are withdrawn.

6th Mode: In this mode, the first cell input switches are opened, and its output switch is closed. Therefore, the first cell inductors start demagnetizing by giving the stored energy to the load via diodes D_{12}, D_{13}, D_{14}, as shown in Fig. 5.7(b), while the input inductors of the second cell are in the same state as in 5th mode i.e. storing the energy. This mode ends when the inductor L_{1a} current equals to the inductor L_{1c} current.

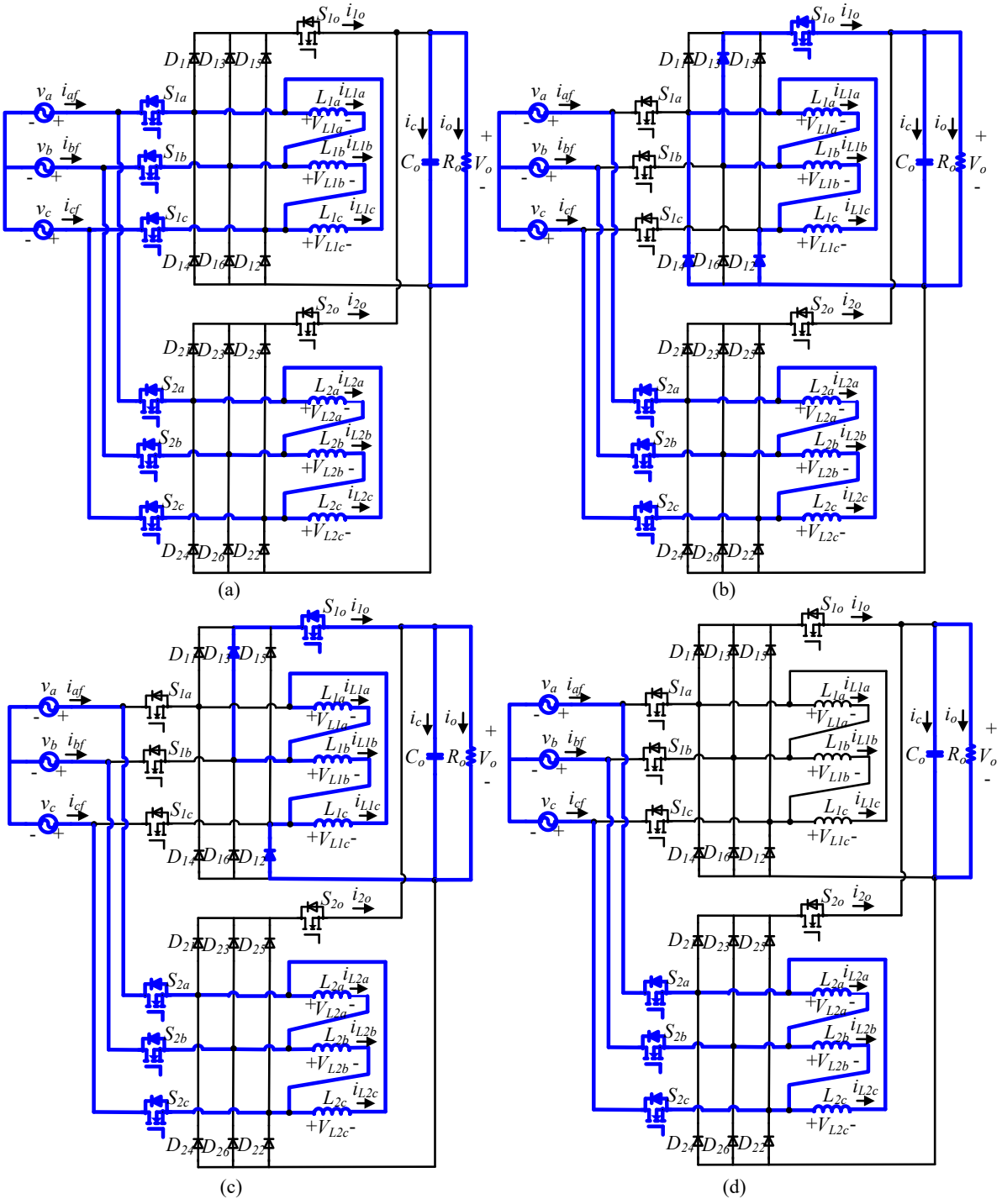


Fig. 5.7. Converter equivalent circuits (a) 5th mode; (b) 6th mode; (c) 7th mode; (d) 8th mode.

7th Mode: In this mode, the switching states of the switches are the same as in the 6th mode except the diode D_{14} that goes to OFF state from ON state. The inductors of the second cell are storing energy and the inductors of the first cell are demagnetizing by delivering energy to the load through diodes D_{12}, D_{13}, as shown in Fig. 5.7(c). This mode ends when all the inductors of the first cell are fully demagnetized.

8th Mode: In this mode, all the inductors of the first cell are in demagnetized state, and the inductors of the second cell are still storing energy as the input switches of first cell are in ON state. Since, there is no power transfer from input to output from either of the cell, the load is supplied by the output filter capacitor. The equivalent circuit of the converter operating in this mode is shown in Fig. 5.7(d).

With reference to the operating modes of the converter, the expressions for input inductor currents of both the cells are defined and given in Table 5.1.

Table 5.1: Input inductors currents equations for different modes of operation in sector-1 for duty cycle $d > 0.5$.

	1st mode	2nd mode	3rd mode	4th mode	5th mode	6th mode	7th mode	8th mode
$i_{L1a}(t)$	$\frac{v_{ab}}{L}t$					$I_{Lap} - \frac{V_o}{L}t;$ $I_{Lap} = \frac{v_{ab}}{L}t_{on}$	$I_{Las} - \frac{V_o}{2L}t;$ $I_{Las} = \frac{v_{ca}}{L}t_{on}$	$i_{L1a}(t) = 0$
$i_{L1b}(t)$	$\frac{v_{bc}}{L}t$					$I_{Lbp} + \frac{V_o}{L}t;$ $I_{Lbp} = \frac{v_{bc}}{L}t_{on}$	$I_{Lbs} + \frac{V_o}{L}t;$ $I_{Lbs} = -\frac{2v_{ca}}{L}t_{on}$	$i_{L1b}(t) = 0$
$i_{L1c}(t)$	$\frac{v_{ca}}{L}t$					$I_{Lcp};$ $I_{Lcp} = \frac{v_{ca}}{L}t_{on}$	$I_{Lcs} - \frac{V_o}{2L}t;$ $I_{Lcs} = \frac{v_{ca}}{L}t_{on}$	$i_{L1c}(t) = 0$
$i_{L2a}(t)$	$\frac{v_{ab}}{L}t$	$I_{Lap} - \frac{V_o}{L}t;$ $I_{Lap} = \frac{v_{ab}}{L}t_{on}$	$I_{Las} - \frac{V_o}{2L}t;$ $I_{Las} = \frac{v_{ca}}{L}t_{on}$	$i_{L2a}(t) = 0$	$\frac{v_{ab}}{L}t$			
$i_{L2b}(t)$	$\frac{v_{bc}}{L}t$	$I_{Lbp} + \frac{V_o}{L}t;$ $I_{Lbp} = \frac{v_{bc}}{L}t_{on}$	$I_{Lbs} + \frac{V_o}{L}t;$ $I_{Lbs} = -\frac{2v_{ca}}{L}t_{on}$	$i_{L2b}(t) = 0$	$\frac{v_{bc}}{L}t$			
$i_{L2c}(t)$	$\frac{v_{ca}}{L}t$	$I_{Lcp};$ $I_{Lcp} = \frac{v_{ca}}{L}t_{on}$	$I_{Lcs} - \frac{V_o}{2L}t;$ $I_{Lcs} = \frac{v_{ca}}{L}t_{on}$	$i_{L2c}(t) = 0$	$\frac{v_{ca}}{L}t$			
Time	$t_{on} - \frac{T_s}{2}$	$t_2 = \frac{3v_a}{V_o}t_{on}$	$t_3 = \frac{2v_{ca}}{V_o}t_{on}$	$(t_{off} - t_2 - t_3)$	$t_{on} - \frac{T_s}{2}$	$t_6 = \frac{3v_a}{V_o}t_{on}$	$t_7 = \frac{2v_{ca}}{V_o}t_{on}$	$(t_{off} - t_2 - t_3)$

5.3.1 DCM operation condition

For the converter DCM operation

$$t_{on} + t_6 + t_7 \leq T_S. \tag{5.2}$$

Substitute t_{on}, t_6 and t_7 from Table 5.1 in (5.2)

$$d \leq \frac{M}{M + \sqrt{3}\sin\left(\omega t + \frac{\pi}{2}\right)} \tag{5.3}$$

where $M = {V_o}/{V_m}$, is voltage gain of the converter; V_m is peak value of phase input voltage. In (5.3), the minimum duty cycle occurs when the denominator is maximum, i.e. $\sin\left(\omega t + \frac{\pi}{2}\right) = 1$. Therefore, for the desired converter gain, the duty cycle limit for converter DCM operation is

$$d \leq \frac{M}{M + \sqrt{3}}. \tag{5.4}$$

From (5.4), the converter critical voltage conversion ratio for a given duty cycle is defined and is given as

$$M_{cr} \geq \frac{\sqrt{3}d}{1 - d}. \tag{5.5}$$

5.3.2 Converter average output current

From the converter operation, the converter average output current is equal to the sum of the average output currents of the individual cells as defined in (5.6)

$$i_{o,avg} = i_{1o,avg} + i_{2o,avg}\,. \tag{5.6}$$

For the sector under the analysis, the average output current of first cell in a switching cycle is given as

$$i_{1o,avg} = \langle i_{L1a} - i_{L1b} \rangle\,. \tag{5.7}$$

Using the expressions from Table 5.1, the expression for the first cell average output current is determined as

$$i_{1o,avg} = \frac{9V_m^2 d^2 T_s}{4LV_o}. \tag{5.8}$$

Equation (5.8) holds true for the second cell as well. Therefore, the average output current of the interleaved converter is twice of the average output current of single cell, and its expression is given as

$$i_{o,avg} = \frac{9V_m^2 d^2 T_s}{2LV_o}. \tag{5.9}$$

5.3.3 Converter input current

Considering lossless operation of the converter,

$$\frac{3}{2} V_m I_m = V_o i_{o,avg} \tag{5.10}$$

$$I_m = \frac{3V_m d^2 T_s}{L} \tag{5.11}$$

where I_m is peak input current.

5.3.4 Inductor design

The inductor design is explained with an example. The converter is designed with the following input specifications;

Input line voltage = 110 V $\pm$ 15%

Supply frequency, f_{in} = 360-800 Hz

Converter rated power, P_o = 2.0 kW

Rated output voltage, V_o = 270 V

Switching frequency, f_s = 50 kHz.

For the above specifications, the converter gain *M* is

$$M = \frac{V_o}{V_{m,min}} = \frac{270}{80.82} = 3.341. \tag{5.12}$$

From (5.4), the maximum value of the duty cycle allowed is

$$d \leq \frac{3.341}{3.341 + \sqrt{3}} \leq 0.6585. \tag{5.13}$$

From (5.9), the converter average output current for $d = 0.6585$, and $V_{m,min}$ = 80.82 V is

$$i_{o,avg} = \frac{9.4412 \times 10^{-4}}{L}\ A. \tag{5.14}$$

From the converter input specifications, the converter output current is

$$I_o = \frac{P_o}{V_o} = \frac{2000}{270} = 7.4074\ A. \tag{5.15}$$

By equating equations (5.14) and (5.15), the value of the input inductor to maintain the converter operation in DCM is 127.45 µH. In view of converter losses, the inductance value $L = 120$ µH is chosen for simulation and experimentation.

5.3.5 Output capacitor design

The output capacitor is designed based on the power holdup time required. If 't_h' is the holdup time required to bring the output capacitor voltage to 90%, then the output capacitance value required is given as

$$C_o = \frac{2P_o t_h}{(0.19V_o^2)}. \tag{5.16}$$

For a holdup time of 5 *ms*, the output capacitance required is C_o = 1440 µF.

5.4 Components voltage stress

From the converter operation, it is observed that the anti-parallel diode of each input switch (mosfet) gets forward biased for the $^2/_3$ period of its corresponding phase negative half-cycle, while the other two switches see a maximum voltage stress of

$$V_{sw,max} = \sqrt{3}V_m + V_o \,. \tag{5.17}$$

From converter mode-2 operation, it can be understood that each output switch (mosfet) experience a maximum voltage stress of peak line-to-line voltage ($\sqrt{3}V_m$). The upper diodes of the bridge rectifier see a maximum voltage stress of output voltage (V_o), whereas the lower diodes of power bridge rectifier see a maximum voltage stress of output voltage plus peak line-to-line voltage ($V_o + \sqrt{3}V_m$).

5.5 Converter Output Voltage to Duty Cycle Transfer Function

The average current injected equivalent circuit approach (CIECA) [74], [75] is used to derive the control-to-output transfer function. In this approach, the converter non-linear part is substituted with the switching cycle average value of current generated by it, as shown in Fig. 5.8. Introducing the perturbations to (5.9), and ignoring the second order terms

$$\hat{\imath}_{o,avg} = \frac{9V_m^2 dT_s}{V_o L}\hat{d} + \frac{9V_m d^2 T_s}{V_o L}\hat{v}_m - \frac{i_{o,avg}}{V_o}\hat{v}_o \tag{5.18}$$

From Fig. 5.8

$$\hat{\imath}_{o,avg} = \left(sC_o + \frac{1}{R_o}\right)\hat{v}_o \,. \tag{5.19}$$

Equating (5.18), (5.19), and substituting $\hat{v}_m = 0$,

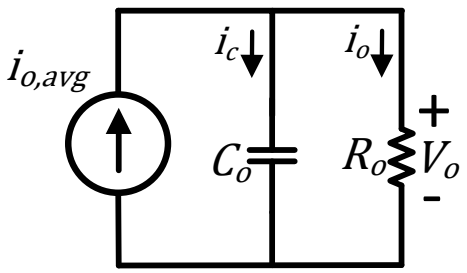


Fig. 5.8. Converter equivalent circuit to derive the control-to-output transfer function as per CIECA approach.

$$\frac{v_o(s)}{d(s)} = \frac{2K}{1 + \frac{Kd}{V_o} + sR_oC_o} \tag{5.20}$$

where $K = \frac{9V_m^2 R_o dT_s}{2V_o L}$, and R_o= load resistance in ohms.

5.6 Input Filter Design

The criteria for the low-pass filter design are:

1. selection of cut-off frequency, f_c

$$f_c = \frac{1}{2\pi}\sqrt{\frac{3}{L_f C_f}} \tag{5.21}$$

2. minimization of filter reactive power consumption for the supply frequencies at rated output power. This is possible when the filter characteristic impedance is equal to the converter input impedance i.e.,

$$Z_c = \sqrt{\frac{3L_f}{C_f}} = Z_{in} \tag{5.22}$$

where Z_c is characteristic impedance = $\sqrt{\frac{L_f}{C_f}}$, and Z_{in} is converter input impedance at rated output power = $\frac{L}{3d^2T_s}$.

By using (5.21), and (5.22), the expressions for low-pass filter parameters are obtained as

$$L_f = \frac{Z_c}{2\pi f_c} \tag{5.23}$$

$$C_f = \frac{1}{6\pi f_c Z_c}. \tag{5.24}$$

5.7 Results and discussion

This section presents the converter simulation results as well as experimental results in order to validate the reported analysis and design. Further, it presents a discussion on comparison of the

interleaved converter, and single-cell converter in terms of power density, efficiency, and reliability.

5.7.1 Simulation results

The proposed three-phase interleaved buck-boost derived converter shown is simulated in PSIM 11.1 software with input filter parameters of L_f = 40 µH and C_f = 0.37 µF, where filter cut-off frequency is chosen at 24 kHz. The converter control-to-output transfer function is obtained by using the designed parameters in (5.20) and is given by (5.25). Since the plant is a single-pole system, a simple PI controller $(k_p + \frac{k_i}{s})$ is sufficient to get the desired converter response. The controller transfer function described by (5.26) is designed for the control design specifications considered at phase margin 75^0 and gain cross-over frequency 100 Hz. Fig. 5.9 shows the frequency response of plant transfer function G(s), controller transfer function H(s), and the open loop transfer function G(s)*H(s). The open loop transfer function has an infinity dc gain which indicates the system reference tracking with zero steady state error, and the system robustness for the input and load disturbances. The open loop phase margin 75^0 indicates enough damping of the

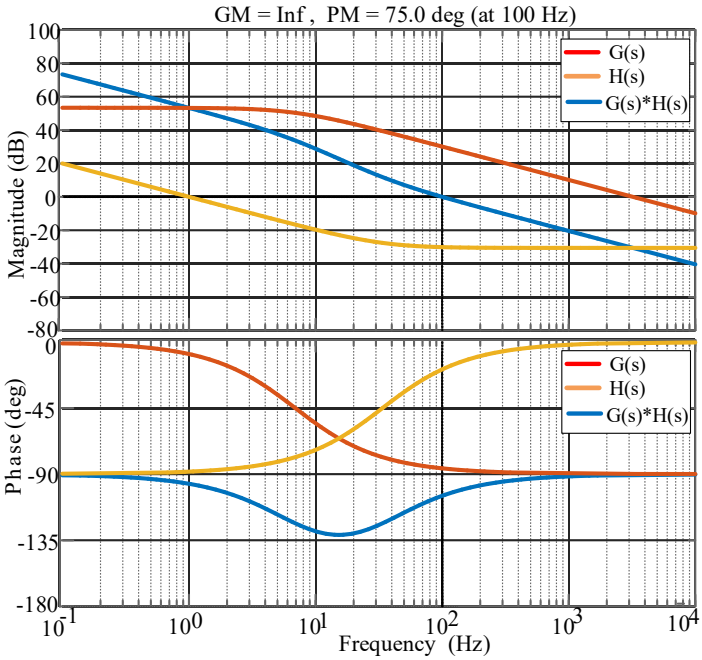


Fig. 5.9. Frequency response of plant G(s), controller H(s), and open-loop G(s)*H(s).

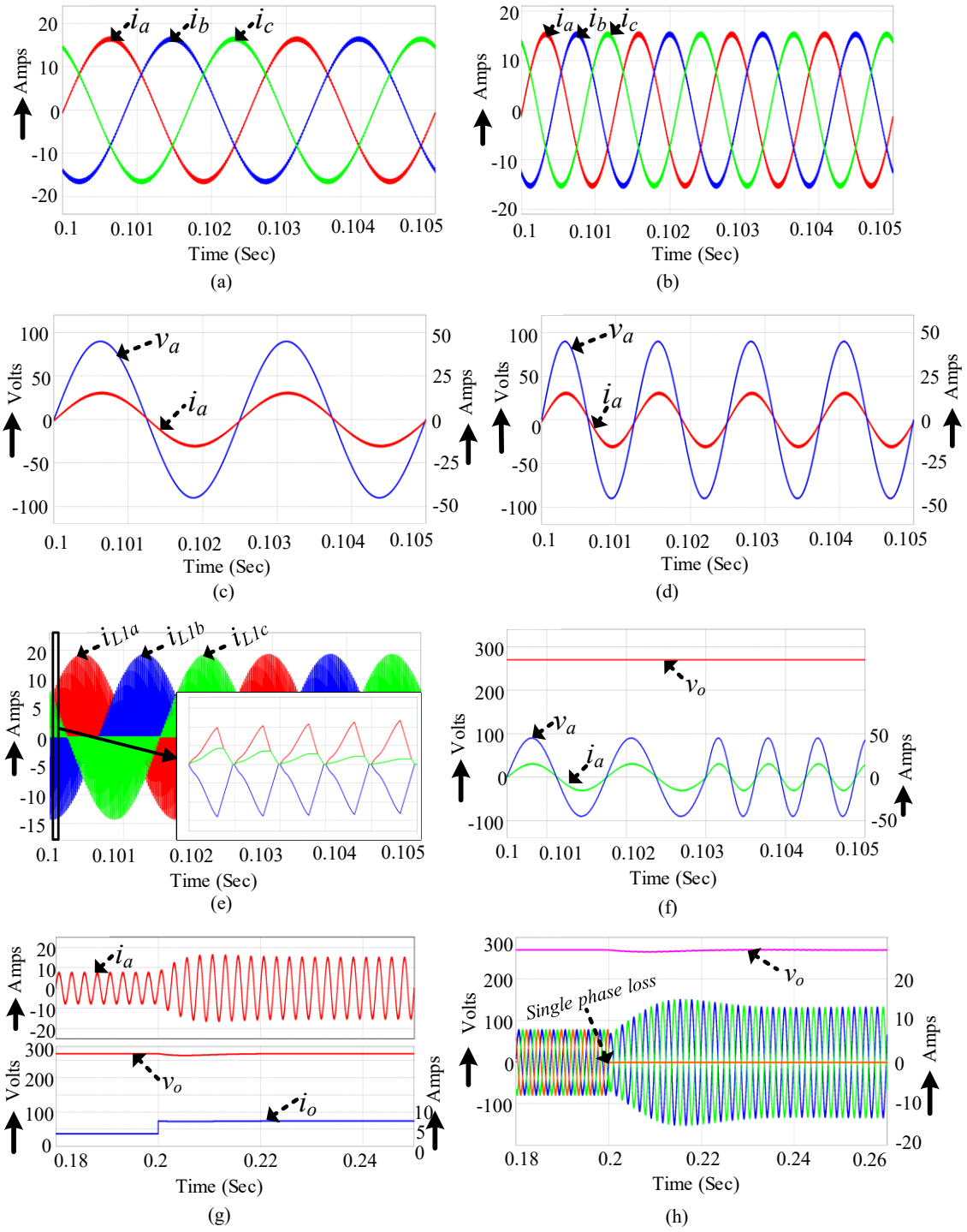


Fig. 5.10. Simulation results of three-phase interleaved buck-boost derived converter (a) phase input currents 400 Hz; (b) phase input currents 800 Hz; (c) phase-A input voltage and input current for supply frequency 400 Hz; (d) phase-A input voltage and input current for supply frequency 800 Hz; (e) inductor currents of one interleaved cell; (f) converter response for input frequency change from 400 Hz to 800 Hz; (g) converter response for 50% load perturbation from 1.0 kW to 2.0 kW; (h) converter response for a single-phase loss.

system, and the -20 dB slope at zero gain cross over frequency indicates the system robustness towards the high frequency noise rejection in the control loop.

$$G(s) = \frac{v_o(s)}{d(s)} = \frac{1062}{0.0525\,S + 2.278} \tag{5.25}$$

$$H(s) = 0.0296 + \frac{6.2937}{S} \tag{5.26}$$

With the designed controller, a closed-loop simulation for the proposed converter is performed in PSIM 11.1 software, and the results are depicted in Fig. 5.10. Fig. 5.10(a) and Fig. 5.10(b) show the converter input currents for supply frequencies 400 Hz and 800 Hz, respectively. Fig. 5.10(c) and Fig. 5.10(d) show the waveforms of phase-A input voltage and input current for supply frequencies 400 Hz and 800 Hz, respectively. The input currents are sinusoidal and following the input voltages both in phase and shape, confirming the UPF operation of the converter. Fig. 5.10(e) shows the input inductor current waveforms of one interleaved cell at rated output power, the inductor currents are discontinuous and validating the design. Fig. 5.10(f) shows the converter response for supply frequency change from 400 Hz to 800 Hz. The output voltage is not disturbed, and the input current is closely tracking the input voltage both in phase and shape during input frequency change, which proves the robustness of the converter and the control. Fig. 5.10(g) shows the converter response for 50% load perturbation from 1.0 kW to 2.0 kW. The output voltage is stable and tracking the reference voltage with a settling time of 10 ms, which confirms the robustness of the designed controller. Further, the proposed converter provides the fault tolerant operation for a single-phase loss and gives 50% of the rated output power without altering the controller structure. The reduction in power is due to the duty cycle limit derived in (5.4). With a single-phase loss, the converter resembles a single-phase converter with line-to-line voltage as input source. Therefore, the output voltage is having second order supply frequency oscillations like a single-phase PFC rectifier as shown in Fig. 5.10(h).

5.7.2 Experimental results

To validate the converter analysis and to further verify simulation results, a 2.0 kW proof-of-concept hardware prototype is developed, and the details are mentioned in Table 5.2. The hardware is not optimized, it is just developed for to prove the developed concept and analysis. Fig. 5.11

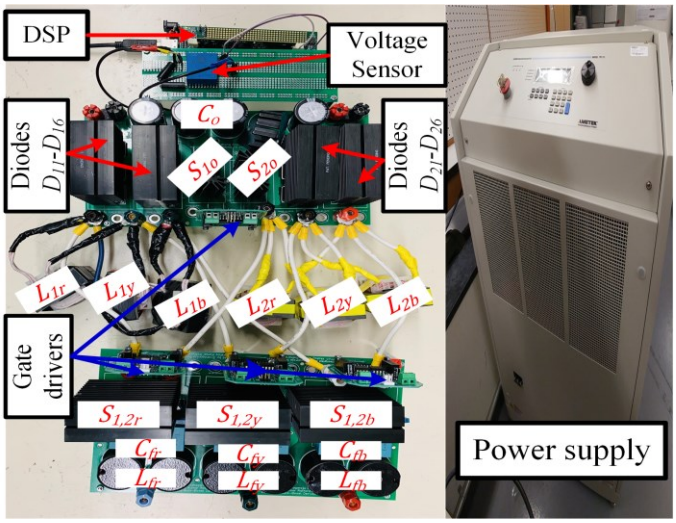


Fig. 5.11. A 2.0 kW experimental prototype of proposed converter.

Table 5.2: Hardware components specifications.

Component	**Specifications**
Switches	UJ3C065030K3S, SIC, 650V, 30 *m*ohm
Diodes	RHRG5060-F085, 600 V
Output capacitor, C_o	ESMQ401VSN471MQ50W, 4 x 470 µF
Filter capacitors, C_f	F873DU104M760Z, 4 x 0.1 μF
Filter inductors, L_f	1140-101K-RC, 100/2 μH
Snubber capacitor	R75QD0470DQ30J, 470 pF
Snubber resistor	EP5WS100RJ, 100 Ω
Inductors, $L_{1r,y,b}$, $L_{2r,y,b}$	55 x 28 x 21, EE Ferrite cores
Gate drivers	HCNW3120 IC
Power source	California-MX30 (300 – 500 Hz)

depicts the hardware prototype developed in lab where DSP TMS320F28335 is used to program the designed controller, and LEM voltage sensor LV-25P is used to measure the converter output voltage.

Fig. 5.12(a) and Fig. 5.12(b) depict the measured input currents at rated output power for the supply frequency of 300 Hz and 500 Hz, respectively. Fig. 5.12(c) and Fig. 5.12(d) depict the measured converter input voltage and input current of one phase at rated output power for supply

Table 5.3: Converter input power factor and current THD (%) for different output powers for supply frequencies 350 Hz and 500 Hz.

Power (kW)	350 Hz		500 Hz	
	PF	THD (%)	PF	THD (%)
0.25	0.9969	6.39	0.9956	6.35
0.5	0.9983	5.20	0.9978	5.19
0.75	0.9990	4.20	0.9989	4.19
1.0	0.9994	3.33	0.9994	3.33
1.5	0.9995	3.05	0.9995	3.04
2.0	0.9996	2.70	0.9996	2.52

frequency of 300 Hz and 500 Hz, respectively. The input currents are sinusoidal and are tracking the input voltages both in phase and shape endorsing the simulation results. Fig. 5.12(e) and Fig. 5.12(f) depict the harmonic spectrum of input current at rated output power for supply frequency of 300 Hz and 500 Hz, respectively. The current THD is less than 3% in both the cases, and the input power factor is very close to unity. The converter measured input power factor and current THD for different output power for supply frequency of 350 Hz, and 500 Hz are listed in Table 5.3. The converter power factor is 0.99 (almost unity) and input current THD is less than 6.5%. Fig. 5.12(g) depicts the input inductor current waveforms of one interleaved cell at rated output power, the inductor currents are discontinuous and confirming the design and simulation. Fig. 5.12(h) depicts the measured voltage across one of the input switches; the switch sees a maximum voltage stress equal to the output voltage plus the peak line-to-line voltage. Fig. 5.12(i) depicts the converter response for supply frequency change from 300 Hz to 500 Hz. The output voltage is not disturbed, and the input current is closely tracking the input voltage, as observed in simulation. Fig. 5.12(j), depicts the converter response for 20% input voltage reduction; the converter input current is increased accordingly for given load. Fig. 5.12(k), depicts the converter response for 50% load perturbation from 1.0 kW to 2.0 kW. The converter response is fast, and the output voltage is stable, validating the simulation results. Fig. 5.12(l) depicts the converter response at 1.0 kW output power with a single-phase loss. The output voltage is stable and having the second order supply frequency oscillations as observed in simulation.

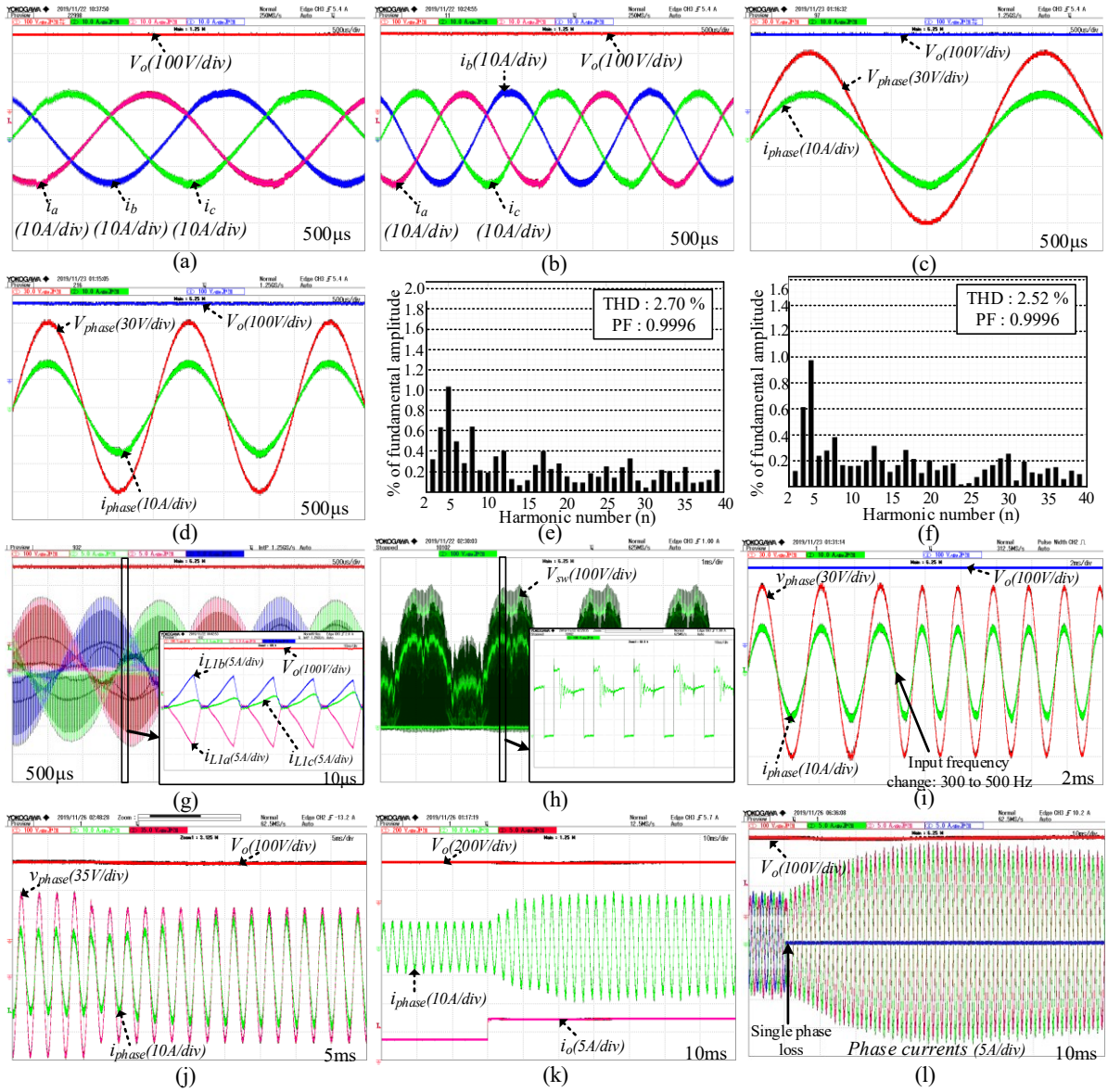


Fig. 5.12. Experimental results of three-phase interleaved buck-boost derived converter at rated output power (a) phase input currents 300 Hz; (b) phase input currents 500 Hz; (c) input voltage and input current of one phase for supply frequency 300 Hz; (d) input voltage and input current of one phase for supply frequency 500 Hz; (e) input current harmonic spectrum for supply frequency 300 Hz; (f) input current harmonic spectrum for supply frequency 500 Hz; (g) inductor currents of one cell; (h) measured voltage across one of input side switch; (i) converter response for input frequency change from 300 Hz to 500 Hz; (j) converter response for 20% input voltage perturbation; (k) converter response for 50% load perturbation from 1.0 kW to 2.0 kW; (l) converter response for a single-phase loss.

5.7.3 Comparison of the proposed interleaved converter with the single-cell converter

To demonstrate the merits of the proposed interleaved converter, it is compared with the single-cell converter for the same specifications and operating conditions. The comparison criteria include the power density, efficiency, and reliability. In general, the magnetic components (inductors and transformers), and the heat sinks occupy most of the converter volume and decide the power density, while the electrolytic capacitors decide the converter reliability.

5.7.3.1 Inductors

The inductors size basically depends on the inductance value and the amount of energy to be stored, which is best described by the area product (AP) formulae given below [92]. The AP described by (5.27) best suits for the filter inductors where the core loss is not severe and the flux swing is limited by core saturation. The AP described by (5.28) best suits for DCM operated inductors where the flux swing is limited by its core loss.

$$AP = A_e A_w = \left(\frac{10^4 L_f i_{Lfsc} i_{Lf,rms}}{B_m J_m K_p}\right)^{4/3} \text{ cm}^4 \tag{5.27}$$

$$AP = A_e A_w = \left(\frac{10^4 L\, \Delta i_L\, i_{L,rms}}{\Delta B_m J_m K_p}\right)^{4/3} \text{ cm}^4 \tag{5.28}$$

where

L_f = filter inductance value, H

i_{Lfsc} = maximum short circuit peak current through filter inductance, A

$i_{Lf,rms}$ = filter inductance maximum RMS current, A

B_m = core saturation flux density, T

L = DCM inductance value, H

Table 5.4: Analytical comparison of the inductor sizes of the single-cell and the proposed interleaved converters.

Description		Value (µH)	$i_{Lf,rms}$ or $i_{L,rms}$ (A)	i_{Lfsc} or Δi_L (A)	AP (cm^4)	Core	Core volume V_e (cm^3)	Core weight (g)	Turns	wire size (mm^2)	Total weight (g)
Filter inductor	**Single-cell**	120	10.5	18.4	5.79	EE 4220	45.4	112	26	2.5	162
	Interleaved	40	10.5	18.4	1.33	EE 3512	24.32	62	16	2.5	92
DCM inductor	**Single-cell**	60	16.6	29.8	13.7	EE 5525	104	260	13	4.0	310
	Interleaved	120	8.16	14.9	5.33	EE 4220	45.4	112	22	2.5	153

Δi_L = maximum current swing, A

ΔB_m = maximum flux density swing, T

$i_{L,rms}$ = DCM inductance maximum RMS current, A

J_m = maximum current density; 450 A/cm^2 for filter inductor, 297 A/cm^2 for DCM inductor

K_p = 0.4, window area utilization factor.

Table 5.4 compares the inductances values, RMS, peak currents through them, the calculated area product, the selected core size, and its calculated weight. In both converters, the input filter inductance values are selected with a consideration of the same input current ripple attenuation after filtering. The core size is chosen based on minimizing the core loss where the ferrite core EE-3C92 type material has been selected because of its low core loss and high saturation flux density. From Table 5.4, it is observed that the volume and weight of the interleaved DCM inductor is more than half when compared to the single-cell DCM inductor. To prove the analytical calculations, the DCM inductors has been prepared at lab with the cores specified in Table 5.4. Fig. 5.13, shows the pictures of the DCM inductors made in the lab along with their dimensions; left side is the interleaved DCM inductor with volume 64.32 cm^3, weight 165 g; the right side is single-cell DCM inductor with volume 140.36 cm^3, weight 350 g. It confirms that the actual measures are in line

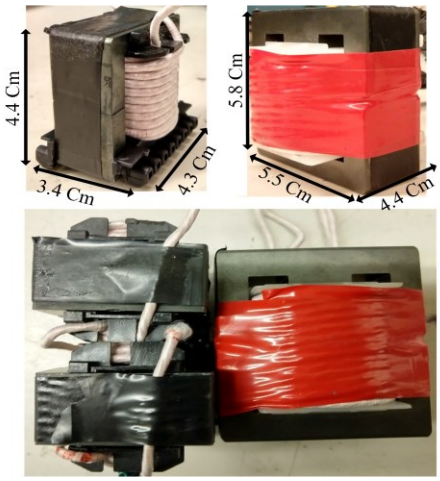


Fig. 5.13. The pictures of the DCM inductors made in lab; left side is for interleaved, right side is for single-cell.

with the calculated values. To get the actual physical interpretation, the two inductors of interleaved cell DCM inductors are placed beside to the single-cell DCM inductor, and is depicted in Fig. 5.13, which clearly show that two interleaved DCM inductors can be easily accommodated in place of one single-cell DCM inductor. Since the interleaved converter employs DCM inductors twice the quantity as compared to the single-cell topology, the half-reduction in volume and weight compensates the extra DCM inductors count in interleaved converter. On the other hand, both converters employ the same number of filter inductors. The reduction in weight and volume of interleaved filter inductor clearly enhances the interleaved converter power density, and reduces the converter total weight.

5.7.3.2 Heat sink

The power processing in a converter through switching of the semiconductor devices generates power losses inside the devices, which in turn generates the heat and increases the devices junction temperature. In order to keep the device junction temperature within the defined safety level, the heat sinks are generally fixed to the semiconductors devices to dissipate the generated heat. The amount of heat transfer from the devices to the ambient is proportional to the surface area of the heat sink. If only one heat sink is employed for all the semiconductors, then the heat sink size is directly determined by the total amount of semiconductor power losses incurred.

Table 5.5 shows the semiconductors loss breakdown of both the converters for the rated output power. It is assumed that both the converters employed identical switches (UJ3C065030K3S, SIC,

Table 5.5: The semiconductors loss breakdown for the single-cell converter, and the interleaved converter at 2.0 kW output power.

Description	Single-cell	Interleaved	
Input switch rms current	16.41	8.20	A
Input switch turn-off average current	34.30	17.15	A
Output switch rms current	-----	7.80	A
Output switch turn-on average current	-----	25.73	A
Bridge diode rms current	8.286	4.19	A
Bridge diode average current	2.47	1.254	A
Switches switching losses	9.16	9.16	W
Switches conduction losses	24.23	15.75	W
Bridge diode conduction losses	13.71	12.24	W
Total semiconductor losses	47.10	37.15	W

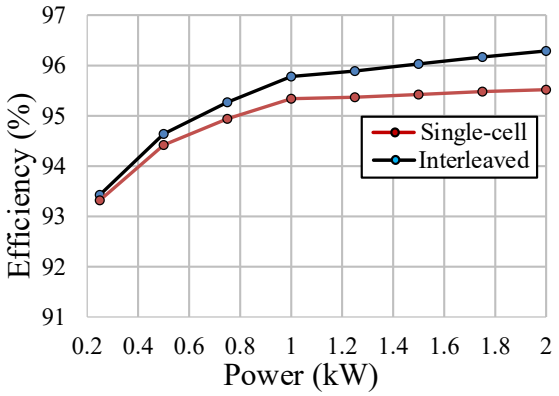


Fig. 5.14. The calculated efficiency curves of single-cell and interleaved converters.

650V, 30 *m*ohm), and the diodes (RHRG5060-F085, 600 V) for their operation. From Table 5.5, it should be observed that the total semiconductor losses in the interleaved converter are less than the single-cell converter, which indicates that the heat sink volume requirement for the interleaved converter is less than the single-cell converter when both the converters are designed for the same specifications and operating conditions. Therefore, the reduction in heat sink volume enhances the interleaved converter power density and reduces the total weight. Fig. 5.14 depicts the measured efficiency curves of both the converters for different output power. It shows clearly that the efficiency in interleaved converter is high when compared to the single-cell converter which is due to the reduction in semiconductor losses and filter losses.

5.7.3.3 Capacitors

In a converter, the electrolytic capacitors are the most fragile components and decides the lifespan or reliability of the system. Considering the operating temperature of both the converters same, then the expected life of a capacitor with respect to its ripple current at the given operating condition [93], [94] is given as

$$Life_{exp} = Life_{base} * 2^{\left(K_t i_{a,ripple}^2 R_{ESR}\left(1-\left(\frac{i_{a,ripple}}{i_{r,ripple}}\right)^2\right)\right)} \quad (5.29)$$

where

$Life_{base}$: Capacitor life specified in datasheets at the rated operating condition

$i_{a,ripple}$: Actual ripple current through the capacitor

$i_{r,ripple}$: Rated ripple current of the capacitor

R_{ESR}: Equivalent series resistance of the capacitor

K_t: $55/S^{0.8}$, 'S' is capacitor surface area in cm^2.

From (5.29), it is clear that when the actual ripple current approaching the rated ripple current, the factor $\left(1-\left(\frac{i_{a,ripple}}{i_{r,ripple}}\right)^2\right)$ is moving towards zero, and the expected life of capacitor is getting reduced and approaching the '$Life_{base}$'. That means, if the ripple current through the capacitor is

Table 5.6: Numerical values of capacitors ripple currents in single-cell and interleaved converters.

Description		Value (µF)	Maximum ripple current (A)	Ripple frequency (kHz)
Input Filter capacitor	**Single-cell**	1.1	30.16	50
	Interleaved	0.4	14.7	100
Output filter capacitor	**Single-cell**	1440	51.4	50
	Interleaved	1440	25.8	100

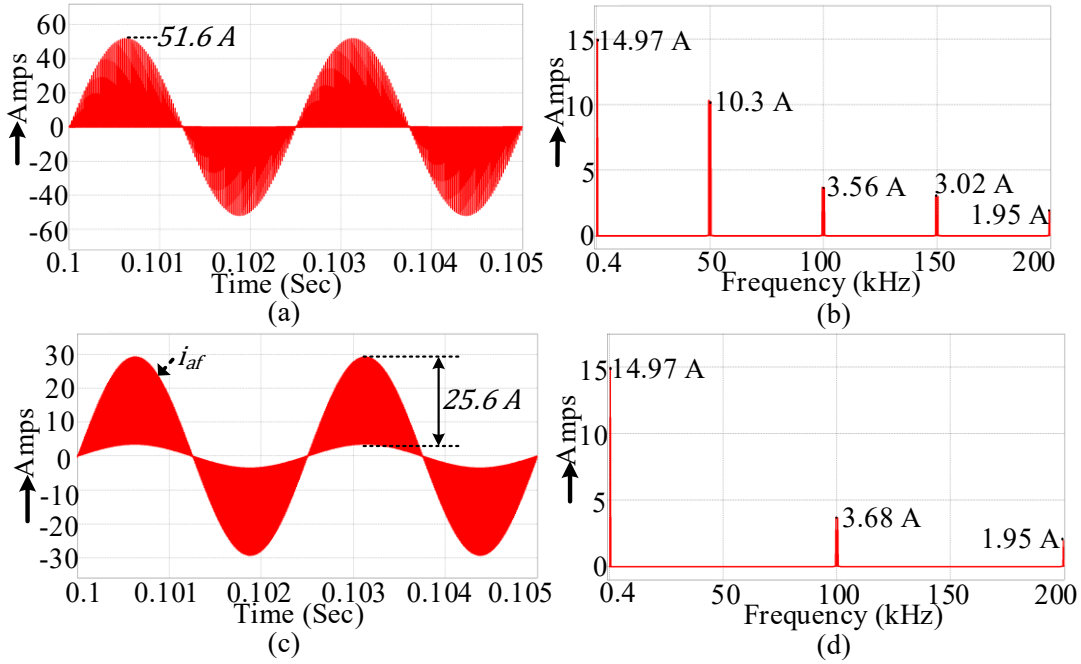


Fig. 5.15. Simulated unfiltered input current, and its FFT (a), (b) single-cell converter; (c), (d) interleaved converter.

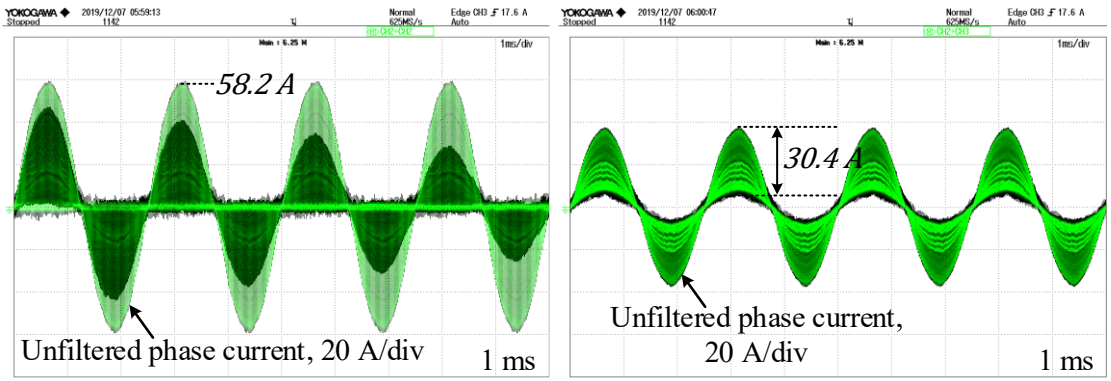


Fig. 5.16. Unfiltered input current at 2.0 kW output power from experimentation (a) interleaved converter; (b) single-cell converter.

minimized, then the lifespan of the capacitor will be enhanced, and thereby it increases the converter reliability. Table 5.6 shows the numerical values of the capacitors ripple currents for both the single-cell and the interleaved converters, at rated output power. The input filter capacitors ripple current with interleaved operation is reduced to half and its effective frequency is doubled, which is evident from the simulation and experimental results of unfiltered input currents shown

in Fig. 5.15 and Fig. 5.16. Similarly, the unfiltered DC current ripple is also reduced by half and contains a very low amplitude of 6^{th}, 12^{th}, and 18^{th} order supply frequency components and high amplitude of high frequency switching components in addition to the DC component. The 50 % reduction in the ripple current in interleaved converter helped in enhancing the lifespan of output electrolytic capacitors by 2.71 times when compared to the single-cell converter. This is calculated from (5.29) considering both the converters employing the capacitors (ESMQ401VSN471MQ50W) and the capacitors in the single-cell converters are operating at the rated ripple current. The increase in the ripple frequency in the interleaved converter increases the ripple current handling capability of the electrolytic capacitors further, which further enhances the capacitors lifespan and the system reliability.

5.8 Conclusion

A three-phase interleaved buck-boost derived PFC converter operating in DCM for MEA is proposed, analyzed, and designed. With the wide supply frequency variation, the converter UPF operation at varying supply frequency is obtained through inherent PFC characteristic of DCM without any current control loop, and with reduced number of sensors. A simple output voltage control loop with a single sensor is implemented to accomplish the tight output voltage regulation. A 2.0 kW laboratory hardware prototype is developed to verify the reported analysis and design. It is shown that the converter maintains UPF operation for different load and for varying supply frequency. An input current THD of 2.7% (< 5%) and a maximum efficiency of 96.3% (>90%) are recorded from the developed prototype at rated output power.

The DCM inductor size and weight in interleaved converter is 50% less compared to the single-cell converter which has been validated analytically, and with physical inductors made in the lab. This 50% reduction compensates the extra usage of the DCM inductors in interleaved converter. However, the filter inductors size and the heat sink requirement in interleaved converter is substantially less compared with single-cell converter, which shows the higher power density of the interleaved converter, and the same has been validated analytically. It is also shown that in the interleaved converter the ripple currents through the filter capacitors are reduced 50 %, and their effective frequency is doubled. The reduction in ripple current facilitated in enhancing the lifespan of output electrolytic capacitors by more than two times compared to the single-cell converter, which shows the higher reliability of the interleaved converter.

Chapter 6 : Three-Phase Single-Stage Isolated Flyback-based PFC Converter

6.1 Introduction

The flyback topology is an isolated form of buck-boost converter and is derived by replacing the buck-boost inductor with flyback transformer. The main drawback of the flyback converter is low efficiency, which is mainly due to the leakage inductance of the flyback transformer. In flyback converter topology, the transformer leakage inductance is in series with the power switch and produces a large voltage spike when the switch is turned-off. It is due to the absence of the current conduction path for the leakage inductance energy when the switch is turned-off, then interacts with the switch output capacitance and appears as large voltage surge across the switch. This voltage surge is usually high and may go beyond the switch rated voltage and can cause the switch failure. The traditional way of limiting this voltage surge is introducing a snubber circuit across the flyback transformer which is referred as clamping circuit.

The clamping circuits are broadly classified into two categories; 1) passive-clamping circuit and 2) active-clamping circuit. The passive-clamping circuit consists of a large capacitor where the transformer leakage inductance energy is stored when the switch is turned-off and contain some additional components to discharge the capacitor [95]-[98]. The clamping circuits namely resistor-capacitor-diode (RCD), inductor-capacitor-diode (LCD), and energy regenerated snubber circuits come under the category of passive-clamping circuit. The active-clamping circuit employs at least one switch along with large capacitor to recover the leakage inductance energy [99]-[101]. In literature, the methods of active-clamping is defined only for single-phase flyback converters [99]-[101], and the same can be extended only for three-phase modular flyback converters [63], [102], [103] on the cost of increasing the complexity both in control and circuit configuration by adding footprints.

In [63], [89], [102]-[106], the three-phase isolated single-stage flyback based converters operating in DCM are reported. The three-phase modular flyback converters with three single-phase flyback circuits connected in wye-configuration with passive RCD clamping circuit across each transformer to cap the voltage surge are reported in [63], [102], [103]. The main concern with the modular structure is higher semiconductors count, low efficiency, and the higher effort for

clamping the switch over voltages. In view of reducing the semiconductors count, a three-phase flyback topology with a single-switch is reported in [104]. A two-switch version of the single-switch converter for the use with higher input voltages is reported in [105]. However, both the converters require nine diodes and three center-tapped three-winding transformers for its operation, with poor transformer utilization compared to the converter reported in [106]. The interleaved version of the converter [106] is reported in [89] with a main focus on the transformer design to reduce the transformer leakage inductance. The stated converters in [63], [89], [102]-[106] employed the conventional passive RCD dissipative-clamping circuit across each transformer for limiting the voltage surge. In RCD clamping circuit, the transformer leakage inductance energy is transferred to the capacitor when the switch is turned-off and is simply dissipated in the resistor as heat, hence, these converters suffer from lower efficiency.

Therefore, with a focus on utilizing the transformers leakage inductance energy, and thereby to improve the converter overall efficiency, a three-phase single-stage isolated flyback-based converter with a novel clamping circuit is proposed and studied in this Chapter. With the proposed clamping circuit, all the flyback transformers leakage inductance energy is successfully captured in a single clamping capacitor and is fed back to the DC-link to enhance the overall converter efficiency.

6.2 Proposed converter and control scheme

The proposed three-phase single-stage isolated flyback-based converter along with the proposed clamping circuit is shown in Fig. 6.1. The proposed converter is an isolated version of the converter analyzed in Chapter 4, and is obtained by replacing the input inductors L_a, L_b, L_c with flyback transformers T_a, T_b, T_c. The power circuit comprises of three flyback transformers, three power switches, and one three-phase diode-bridge rectifier. The PFC at the AC source is obtained by designing the flyback transformers for DCM i.e., the transformers are designed such that their magnetizing inductance will be fully demagnetized at the end of every switching cycle. The converter switches are driven synchronously and fed with a common gating signal. Fig. 6.2 shows block diagram of the output voltage control scheme for the proposed converter. The voltage controller generates the duty cycle required for the switches to regulate the output voltage and it

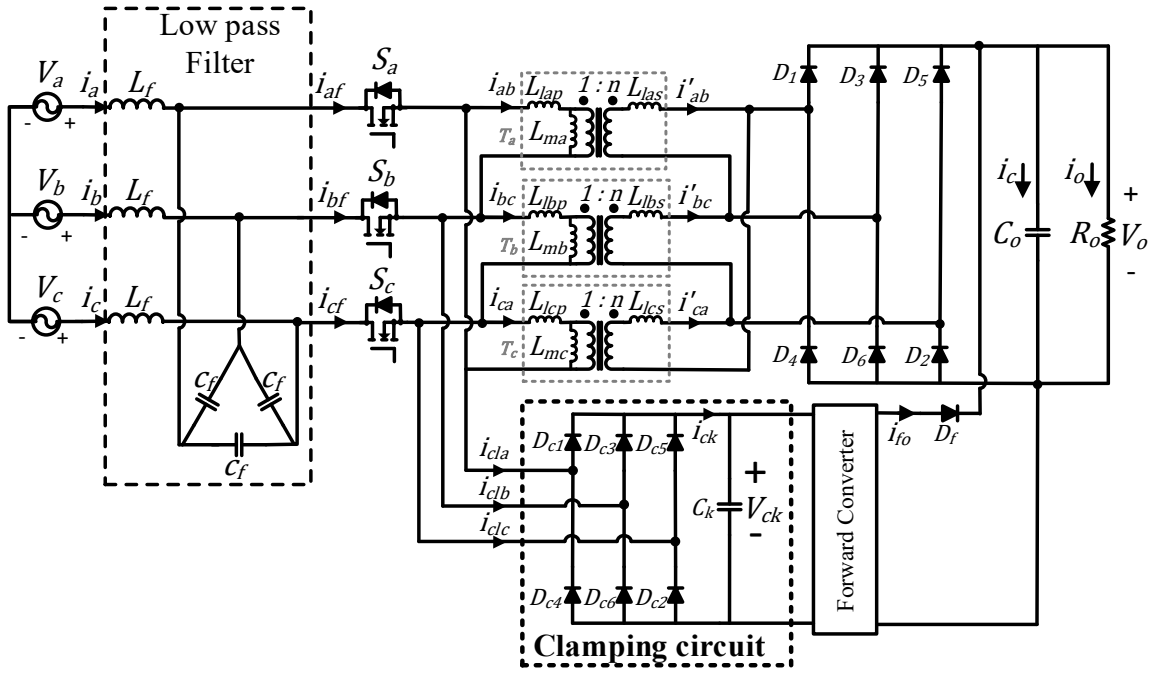


Fig. 6.1. Proposed three-phase single-stage isolated flyback-based converter with clamping circuit to recover the transformers leakage energy.

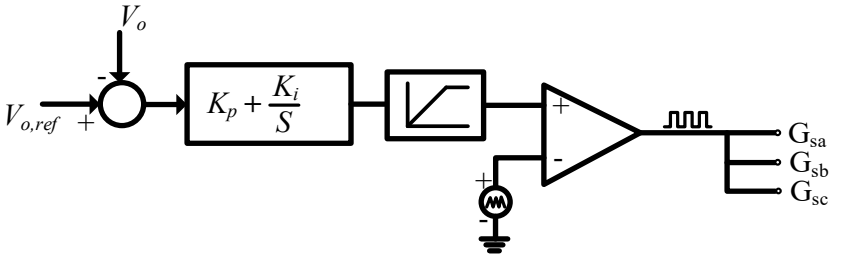


Fig. 6.2. The converter output voltage control block diagram.

is fed to the saturation block where it gets capped to the upper limit during overloads to protect the converter by limiting the converter currents within the rated values.

Since the flyback transformers in the proposed converter are connected at AC side, it is allowed to use a single clamping circuit comprising of one three-phase diode-bridge rectifier and a single capacitor, which is not the case with the state-of-the-art converters. The state-of-the-art converters used an individual RCD clamping circuit across each flyabck transformer. Therefore, the individual flyback transformer leakage inductance energy is captured in individual clamping capacitor, and it is dissipated in clamping resistors. While, in the proposed clamping circuit, all

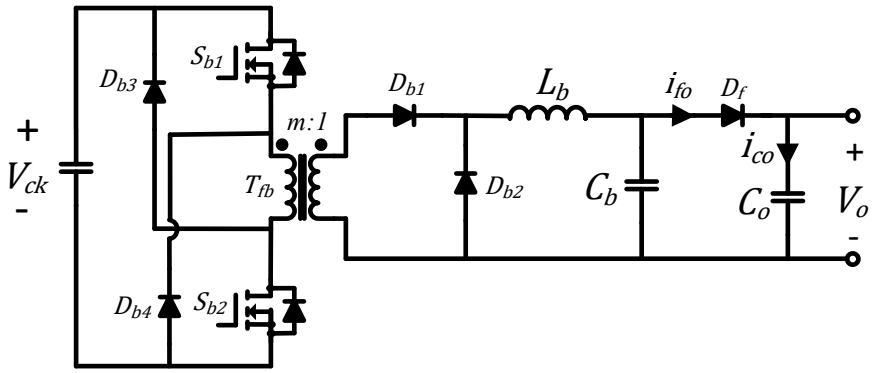


Fig. 6.3. A two-switch forward converter to transfer the captured transformers leakage energy to the DC-link.

three flyback transformers leakage inductance energy is captured in a single clamping capacitor by connecting a three-phase diode-bridge rectifier module called clamping rectifier at the primary side of the transformers, as shown in Fig. 6.1. The captured energy is fed to the DC-link by using an auxiliary two-switch forward converter shown in Fig. 6.3 across the clamping capacitor, which improves the overall converter efficiency. The auxiliary two-switch forward converter is also designed to operate in DCM. The switches of auxiliary forward converter are provided with the same duty cycle, and it should be selected to be less than 0.5 so that it evades the saturation of forward transformer. The diode 'D_f' placed between the forward converter and the DC-link ensures the unidirectional power flow from forward converter to the DC-link.

6.3 Converter steady state analysis

Since the switching time period is very small when compared to the supply time period, it is considered that the variation in input voltage and output voltage are negligible and considered them constant in one switching period. It is also considered that all the transformers are identical i.e., their magnetizing and leakage inductance values are same

$$\begin{aligned} L_{ma} &= L_{mb} = L_{mc} = L_m \\ L_{lap} &= L_{lbp} = L_{lcp} = L_{lp} \\ L_{las} &= L_{lbs} = L_{lcs} = L_{ls}\,. \end{aligned} \tag{6.1}$$

In the analysis, the transformer secondary leakage inductance values are referred to the primary side. Therefore,

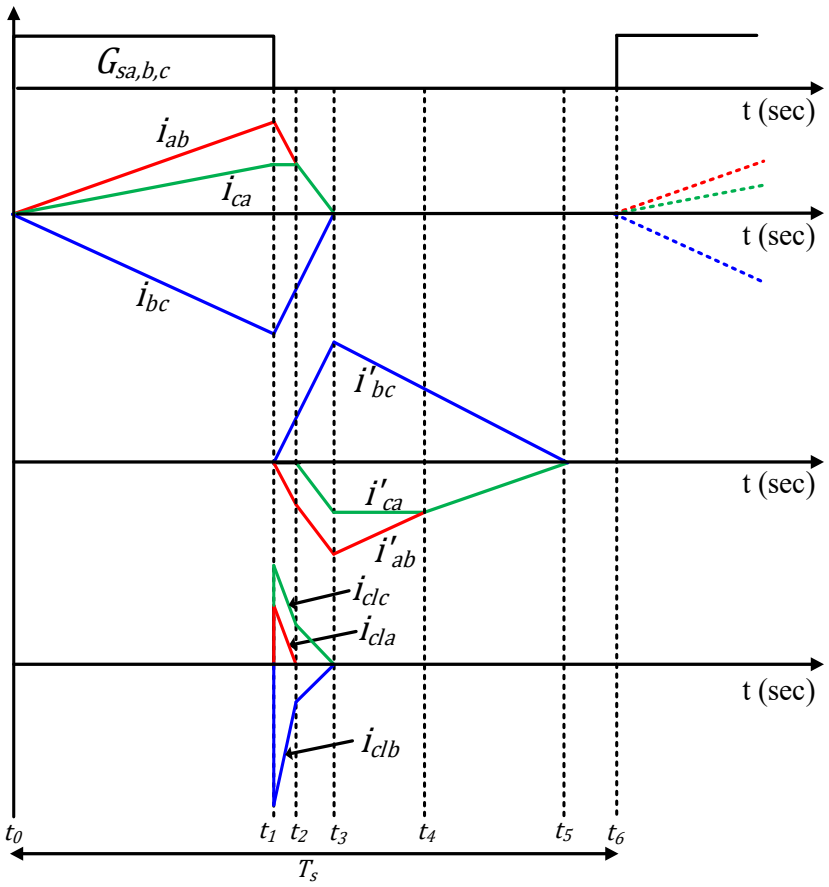


Fig. 6.4. The converter key current waveforms for one switching cycle.

$$L_{lp} = L'_{ls} = L_l \tag{6.2}$$

where L'_{ls} is the transformer secondary leakage inductance referred to primary side.

Since the forward converter operation is independent of the main converter operation, only the main converter with clamping circuit is considered for the analysis. The steady state current waveforms of transformers primary, secondary, and the clamping circuit in one switching cycle for supply time period $\omega t = 0$ to $\frac{\pi}{6}$ are shown in Fig. 6.4. It should be observed that the converter has six operating modes in a given switching cycle, and the converter equivalent circuits for the different modes of operation are shown in Fig. 6.5.

1st mode $(t_0 - t_1)$: Prior to this mode, all the flyback transformers are in fully demagnetized state. In this mode, all the three power switches are turned-on, and all the rectifier diodes are reverse biased. The bridge rectifier diodes D_{1-6} are reverse biased by the output voltage, and the

clamping rectifier diodes D_{c1-c6} are reverse biased by the clamping capacitor voltage. The converter equivalent circuit operating in this mode is shown in Fig. 6.5(a). When the switches start conducting, the flyback transformers store energy in both the magnetizing and the leakage inductance according to the voltage appearing across them. Hence, the total energy can be divided into two components; 1) magnetizing inductance energy, 2) leakage inductance energy. In this mode, the load is supplied by the output filter capacitor.

2nd mode $(t_1 - t_2)$: This mode starts when all three switches are turned-off. The converter equivalent circuit operating in this mode is shown in Fig. 6.5(b). When the switches are OFF, the transformers primary currents will not go to zero instantly due to the transformer's primary leakage inductance. The energy stored in the transformers leakage inductances forward biases the clamping rectifier diodes D_{c2}, D_{c3}, D_{c4}, and is transformed to the clamping capacitor. Therefore, the clamping capacitor voltage appears across the transformers, and clamps the voltage across the switch at the desired value. At the same time, the rectifier diodes D_2, D_3, D_4 are forward biased by the energy stored in the magnetizing inductances. The transformers secondary currents also do not raise abruptly to their peak value because of the transformers secondary leakage inductance. In this mode, the transformer T_c primary current retains its peak value because of zero voltage appearing across its both primary and secondary windings. This mode ends when the transformer T_a primary current is equal to the transformer T_c primary peak current.

3rd mode $(t_2 - t_3)$: The converter equivalent circuit operating in this mode is shown in Fig. 6.5(c). The status of the switches and diodes are in the same state as 2nd mode except D_{c4} which goes to OFF state. At the end of this mode, all the transformers primary currents reach zero, and the secondary currents reach their peak values, as shown in Fig. 6.4.

4th mode $(t_3 - t_4)$: The converter equivalent circuit operating in this mode is shown in Fig. 6.5(d). In this mode, all the clamping rectifier diodes are in OFF state, and the rectifier diodes are in the same state as the 2nd mode. The transformer T_c secondary current retains its peak value, and the transformers T_a, T_b secondary currents flow through the load. This mode ends when the transformer T_a secondary current is equal to the transformer T_c secondary peak current.

5th mode $(t_4 - t_5)$: The converter equivalent circuit operating in this mode is shown in Fig. 6.5(e). The status of the switches and diodes are in the same state as the 4th mode except D_4 which

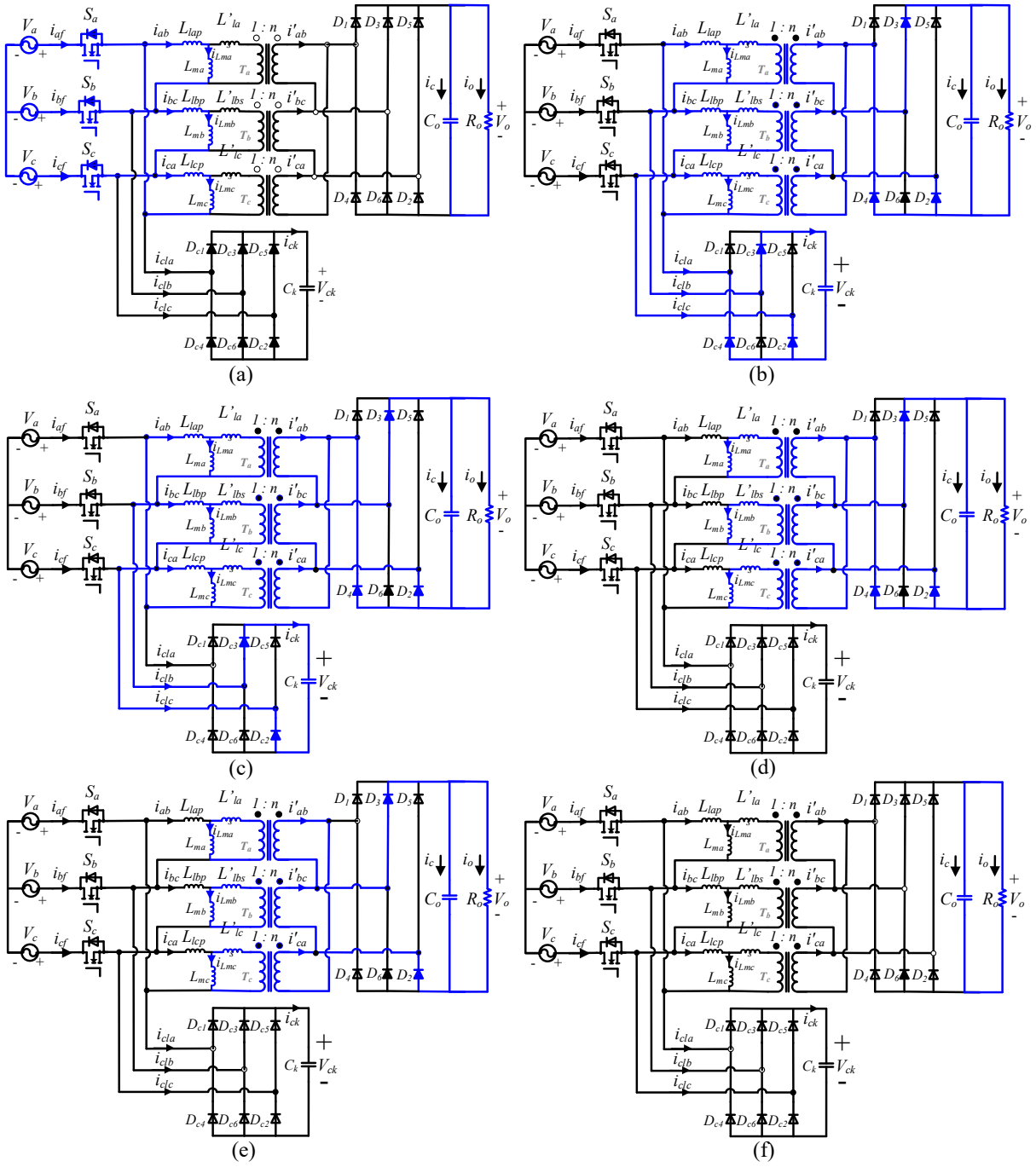


Fig. 6.5. Converter equivalent circuits; (a) 1st mode; (b) 2nd mode; (c) 3rd mode; (d) 4th mode; (e) 5th mode; (f) 6th mode.

Table 6.1: Flyback transformers primary and secondary currents expressions for different modes of operation.

	1st mode	2nd mode	3rd mode	4th mode	5th mode	6th mode
$i_{ab}(t)$	$\frac{v_{ab}}{L_m+L_l}t$	$I_{abp}-\frac{(nV_{ck}-V_o)}{2nL_l}t;$ $I_{abp}=\frac{v_{ab}}{L_m+L_l}t_{on}$	$I_{abs}-\frac{(nV_{ck}-V_o)}{4nL_l}t;$ $I_{abs}=\frac{v_{ca}}{L_m+L_l}t_{on}$	0	0	0
$i_{bc}(t)$	$\frac{v_{bc}}{L_m+L_l}t$	$I_{bcp}+\frac{(nV_{ck}-V_o)}{2nL_l}t;$ $I_{bcp}=\frac{v_{bc}}{L_m+L_l}t_{on}$	$I_{bcs}+\frac{(nV_{ck}-V_o)}{2nL_l}t;$ $I_{bcs}=-\frac{2v_{ca}}{L_m+L_l}t_{on}$	0	0	0
$i_{ca}(t)$	$\frac{v_{ca}}{L_m+L_l}t$	$I_{cap};$ $I_{cap}=\frac{v_{ca}}{L_m+L_l}t_{on}$	$I_{cas}-\frac{(nV_{ck}-V_o)}{4nL_l}t;$ $I_{cas}=\frac{v_{ca}}{L_m+L_l}t_{on}$	0	0	0
$i'_{ab}(t)$	0	$\frac{-(nV_{ck}-V_o)}{2n^2L_l}t$	$I'_{abs}-\frac{(nV_{ck}-V_o)}{4n^2L_l}t;$ $I'_{abs}=\frac{-3v_a}{n(L_m+L_l)}t_{on}$	$I'_{abr}+\frac{V_o}{n^2(L_m+L_l)}t;$ $I'_{abr}=\frac{-v_{ab}}{n(L_m+L_l)}t_{on}$	$I'_{abq}+\frac{V_o}{2n^2(L_m+L_l)}t;$ $I'_{abq}=I'_{car}$	0
$i'_{bc}(t)$	0	$\frac{(nV_{ck}-V_o)}{2n^2L_l}t$	$I'_{bcs}+\frac{(nV_{ck}-V_o)}{2n^2L_l}t;$ $I'_{bcs}=\frac{3v_a}{n(L_m+L_l)}t_{on}$	$I'_{bcr}-\frac{V_o}{n^2(L_m+L_l)}t;$ $I'_{bcr}=\frac{-v_{bc}}{n(L_m+L_l)}t_{on}$	$I'_{bcq}-\frac{V_o}{n^2(L_m+L_l)}t;$ $I'_{bcq}=-2I'_{car}$	0
$i'_{ca}(t)$	0	0	$\frac{-(nV_{ck}-V_o)}{4n^2L_l}t$	$I'_{car};$ $I'_{car}=\frac{-v_{ca}}{n(L_m+L_l)}t_{on}$	$I'_{caq}+\frac{V_o}{2n^2(L_m+L_l)}t;$ $I'_{caq}=I'_{car}$	0
Time period	$t_{on}=dT_s$	$\frac{6nv_aL_lt_{on}}{(nV_{ck}-V_o)(L_m+L_l)}$	$\frac{4nv_{ca}L_lt_{on}}{(nV_{ck}-V_o)(L_m+L_l)}$	$\frac{3nv_a}{V_o}t_{on}$	$\frac{2nv_{ca}}{V_o}t_{on}$	T_s- (Modes 1 to 5 Time periods sum)

goes to OFF state. In this mode, the transformers T_a, T_b, T_c secondary currents decreases through the load through diodes D_2, D_3, and reach zero at the end of this mode.

6th mode $(t_5 - t_6)$: The converter equivalent circuit operating in this mode is shown in Fig. 6.5(f). In this mode, all the switches and diodes are in OFF state, and the output filter capacitor delivers power the load.

Since the proposed converter is symmetric, the above analysis can be extended for remaining supply time period. For each mode, the transformers primary currents, secondary currents are defined and given in Table 6.1.

6.4 Converter design

This section presents the DCM condition, and the expressions for converter average output current and input current and derives the design equations for each component of converter.

6.4.1 DCM operation condition

To ensure the converter DCM operation, the sum of the time intervals of modes 1 to 5 should be less than or equal to the switching period. Since, the time intervals of mode-2 and mode-3 are very small compared to the time intervals of other modes, they are neglected for the simplicity of mathematical analysis. Therefore,

$$t_{on} + \frac{3nv_a}{V_o} t_{on} + \frac{2nv_{ca}}{V_o} t_{on} \leq T_s. \tag{6.3}$$

Simplifying, and substituting $t_{on} = dT_s$ and, $v_{ca} = \sqrt{3}V_m \sin\left(\omega t + \frac{\pi}{2}\right)$ in (6.3)

$$d \leq \frac{M}{M + \sqrt{3}n \sin\left(\omega t + \frac{\pi}{2}\right)} \tag{6.4}$$

where $M = {V_o}/{V_m}$.

In equation (6.4), the switch duty cycle is minimum it the denominator is maximum i.e., when $\sin\left(\omega t + \frac{\pi}{2}\right) = 1$. Therefore, for a given converter gain, the maximum value of the duty cycle to operate the converter in DCM is

$$d \leq \frac{M}{M + n\sqrt{3}}. \tag{6.5}$$

From (6.5), the converter critical voltage conversion ratio, which decides the converter DCM operation is defined, and is given as

$$M > M_{cr} = \frac{n\sqrt{3}\, d}{1 - d}. \tag{6.6}$$

In the proposed converter to ensure the reverse bias of the rectifier diodes, the output voltage should be higher than the turns ratio (n) times of the peak value of line-to-line input voltage. Hence, for a given duty cycle, the converter is said to be operated in DCM when $M \geq M_{cr} > n\sqrt{3}$.

6.4.2 Average output current

From the converter operation, the average output current in a switching cycle is defined as

$$i_{o,avg} = \langle i_{d3} \rangle = \langle i'_{bc}(t) - i'_{ab}(t) \rangle \,. \tag{6.7}$$

On substituting $i'_{ab}(t)$, $i'_{bc}(t)$ expressions from Table 6.1 in (6.7), and on averaging for a switching cycle

$$i_{o,avg} = \frac{9d^2 T_s V_m^2 \big(L_m(nV_{ck} - V_o) - L_l(nV_{ck} + V_o)\big)}{4(L_m + L_l)^2 (nV_{ck} - V_o) V_o} \,. \tag{6.8}$$

Since the duty cycle of the converter is constant, (6.8) implies the average output current in a switching cycle is constant. Using the same analysis described above, the clamping circuit average output current is calculated as

$$i_{ck,avg} = \frac{9nL_l d^2 T_s V_m^2}{2(L_m + L_l)^2 (nV_{ck} - V_o)} \,. \tag{6.9}$$

Considering the two-switch forward converter is loss less, the total converter average output current is the sum of the power circuit average output current, and the clamping circuit average output current. Before doing sum, the clamping circuit current should be multiplied by $\frac{V_{ck}}{V_o}$ to make forward converter power balance. Therefore

$$i_{oT,avg} = i_{o,avg} + \left(\frac{V_{ck}}{V_o} * i_{ck,avg}\right) \tag{6.10}$$

$$i_{oT,avg} = \frac{9d^2 T_s V_m^2}{4(L_m + L_l) V_o} \,. \tag{6.11}$$

6.4.3 Input current

Considering the loss less operation of the converter, the total input power is equal to the output power, i.e.

$$\frac{3}{2}V_m I_m = V_o i_{oT,avg} \tag{6.12}$$

$$I_m = \frac{3V_m d^2 T_s}{2(L_m + L_l)} \tag{6.13}$$

where I_m is peak value of input phase current.

6.4.4 Transformer magnetizing inductor

The converter average value of output current for a given output power, P_o, and output voltage, V_o, is

$$I_{o,avg} = \frac{P_o}{V_o}. \tag{6.14}$$

Using equations (6.11), and (6.14), the value of the inductance required to operate the converter in DCM is calculated as,

$$(L_m + L_l) \leq \frac{9}{4}\frac{d^2 V_m^2 T_s}{P_o}. \tag{6.15}$$

To ensure the converter DCM operation always, the duty cycle in (6.15) should be calculated for minimum input voltage, and maximum output (rated) power condition.

6.4.5 Clamping capacitor

The voltage surge caused by the transformer leakage inductance is clamped at V_{ck} by using the proposed clamping circuit. The clamping capacitor voltage stabilizes when the average power transferred from the transformers leakage inductances is equal to the power transferred to the load by the two-switch forward converter. Therefore, in steady-state at rated power, considering constant voltage V_{ck} across the clamping capacitor, the average power transferred from transformers leakage inductances can be expressed as

$$P_{Ll,avg} = \frac{9L_l d^2 T_s V_m^2}{2(L_m + L_l)^2}\left(\frac{nV_{ck}}{nV_{ck} - V_o}\right). \tag{6.16}$$

Considering a maximum voltage ripple ΔV_{ck} of clamping capacitor, the value of the clamping capacitor is given as

$$C_k = \frac{P_{Ll,avg} T_S}{V_{ck} \Delta V_{ck}}. \tag{6.17}$$

6.4.6 Forward converter inductor

It is considered that the forward converter is operated in DCM, and its duty cycle is constant at d_f =0.4 throughout the converter operation. By considering the forward converter is loss-less, the forward converter inductance required to operate the forward converter in DCM is

$$L_b \leq \frac{(1-d_f) {d_f}^2 m^2 {V_{ck}}^2 T_S}{2P_{Ll,avg}} \leq \frac{0.048 m^2 {V_{ck}}^2 T_S}{P_{Ll,avg}} \tag{6.18}$$

where m = forward converter transformer turns ratio. In above equation, the average power transferred from transformers leakage inductances should be calculated at converter rated power condition.

6.4.7 Components voltage stresses

The voltage profile of switch mosfet 'S_a' for one input line period is shown in Fig. 6.6. It should be observed that the anti-parallel diode of each mosfet gets forward biased for the $^2/_3$ period of its corresponding phase negative half-cycle under its negative peak, while the other two switch anti-parallel diodes see a maximum stress, which is given as

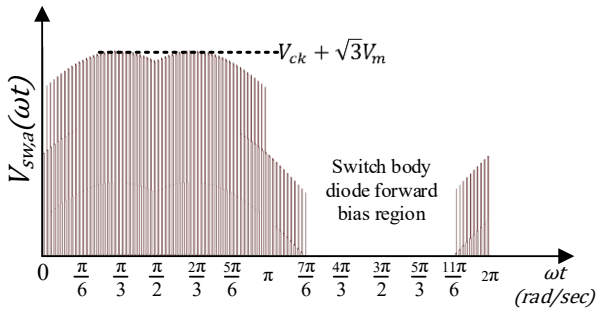


Fig. 6.6. The voltage profile of power switch S_a.

$$V_{sw,max} = \sqrt{3}V_m + V_{ck}\,. \tag{6.19}$$

The power circuit bridge rectifier diodes see a maximum stress of V_o. Similarly, the clamping rectifier diodes see a maximum stress of V_{ck}.

6.4.8 Converter small-signal model

The average current injected equivalent circuit approach (CIECA) [74], [75] is used to derive the small-signal model of the converter. In this approach, the non-linear part of the converter is linearized by injecting the switching cycle average output current ($i_{oT,avg}$) produced by it into the linear part. Introducing the perturbations around the steady-state operating point to (6.11) and (6.13), and neglecting the second order terms gives

$$\hat{\imath}_{oT,avg} = j_2\hat{d} + g_2\hat{v}_m - \frac{1}{r_2}\hat{v}_o \tag{6.20}$$

$$\hat{\imath}_m = j_1\hat{d} + \frac{1}{r_1}\hat{v}_m \tag{6.21}$$

where $j_2 = \frac{9V_m^2 dT_s}{2V_o(L_m+L_l)}$; $g_2 = \frac{9V_m d^2 T_s}{2V_o(L_m+L_l)}$; $r_2 = \frac{V_o}{i_{oT,avg}}$; $j_1 = \frac{3dV_m T_s}{L_m+L_l}$; $r_1 = \frac{2(L_m+L_l)}{3d^2T_s}$.

Fig. 6.7, shows the converter small-signal model defined by equations (6.20) and (6.21). Considering the load as resistive, the converter control-to-output transfer function is derived from Fig. 6.7 and is given as,

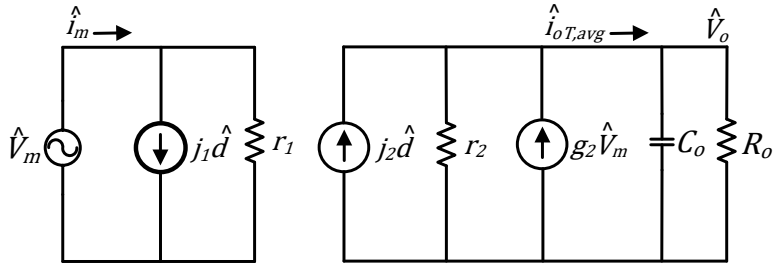


Fig. 6.7. The converter small-signal model equivalent circuit.

$$\frac{\hat{v}_o}{\hat{d}} = \frac{2KV_m}{1 + \frac{KV_m d}{V_o} + SR_o C_o} \tag{6.22}$$

where $K = \frac{9V_m R_o d T_s}{4V_o(L_m + L_l)}$, and R_o= load resistance in Ω.

6.4.9 Input filter design

The criteria for the low-pass filter design are:

1) selection of cut-off frequency, f_c

$$f_c = \frac{1}{2\pi}\sqrt{\frac{3}{L_f C_f}} \tag{6.23}$$

2) minimization of filter reactive power consumption for the supply frequencies at rated output power. This is possible when the filter characteristic impedance is equal to the converter input impedance i.e.,

$$Z_c = \sqrt{\frac{3L_f}{C_f}} = Z_{in} \tag{6.24}$$

where Z_c is characteristic impedance = $\sqrt{\frac{L_f}{C_f}}$, and Z_{in} is converter input impedance at rated output power = $\frac{2(L_m + L_l)}{3d^2 T_s}$.

Using (6.23), and (6.24), the expressions for low-pass filter parameters are obtained as

$$L_f = \frac{Z_c}{2\pi f_c} \tag{6.25}$$

$$C_f = \frac{1}{6\pi f_c Z_c}. \tag{6.26}$$

6.5 Results and discussion

This section presents the simulation results as well as experimental results of the proposed converter along with a discussion on converter efficiency. Further, it also presents detailed explanation of the converter operation with single-phase loss and related results.

6.5.1 Simulation results

This sub-section presents the simulation results of the proposed converter on PSIM 11.1 software. The converter is designed with the specifications mentioned in Table 6.2, and the designed parameters are given in Table 6.3. The input LC low-pass filter is designed for a cut-off frequency of 8 kHz. The flyback transformer turns ratio of 1:1 is selected to get the better magnetic coupling and to reduce the transformer leakage inductance. The transformer magnetizing inductance required for the converter DCM operation is calculated using (6.15), and its value should be less than 62 μH. In view of converter losses, the converter is simulated with transformer magnetizing inductance L_m = 60 μH. The transformer leakage inductance is considered at 2.5% of

Table 6.2: Converter design input specifications.

Rated Power (P_o)	2.0 kW
Output voltage (V_o)	270 V
Switching frequency (f_s)	50 kHz
Input line voltage	110 V_{rms} ±10%
Line frequency (f)	360-800 Hz

Table 6.3: Converter designed parameters.

Flyback Transformer Turns ratio, *1:n*	1:1
Maximum Duty cycle, d	0.65
Filter inductance, L_f	120 μH
Filter capacitance, C_f	1.1 μF
Transformer magnetizing inductance, L_m	60 μH
Transformer leakage inductance, L_l	1.5 μH
Output filter capacitance, C_o	1440 μF
Clamping capacitance, C_k	0.68 μF
Forward transformer turns ratio, *1:m*	1:1.5
Forward converter inductance, L_b	0.8 mH

magnetizing inductance. The output filter capacitor designed for a hold-up time of 5 ms, and its values is C_o = 1440 μF. The clamping circuit is designed to maintain the clamping capacitor voltage at 400 V. With an assumption of 10% voltage ripple across clamping capacitor, the clamping capacitance is calculated using (6.17), and its value is 0.47 μF, the standard value of 0.68 μF is chosen. The forward converter switches are provided with the common gating signal of constant duty cycle value of 0.4 for all the load conditions. The forward converter inductance is calculated using (6.18), its value should be less than 0.92 mH; L_b= 0.8 mH is chosen for simulation.

Using the designed parameters in (6.22), the converter control-to-output transfer function G(s) is obtained and is given in (6.27). A proportional-integral (PI) controller H(s) described by (6.28) is designed for system open-loop cut-off frequency 100 Hz, and phase margin of 75^0. Fig. 6.8 shows the frequency response of plant transfer function G(s) and the open loop transfer function G(s)*H(s). The phase margin and gain margins are positive with enough margins and the open loop transfer function has -20 db slope at zero cross-over frequency for below rated load, which indicates the system stability for below rated load.

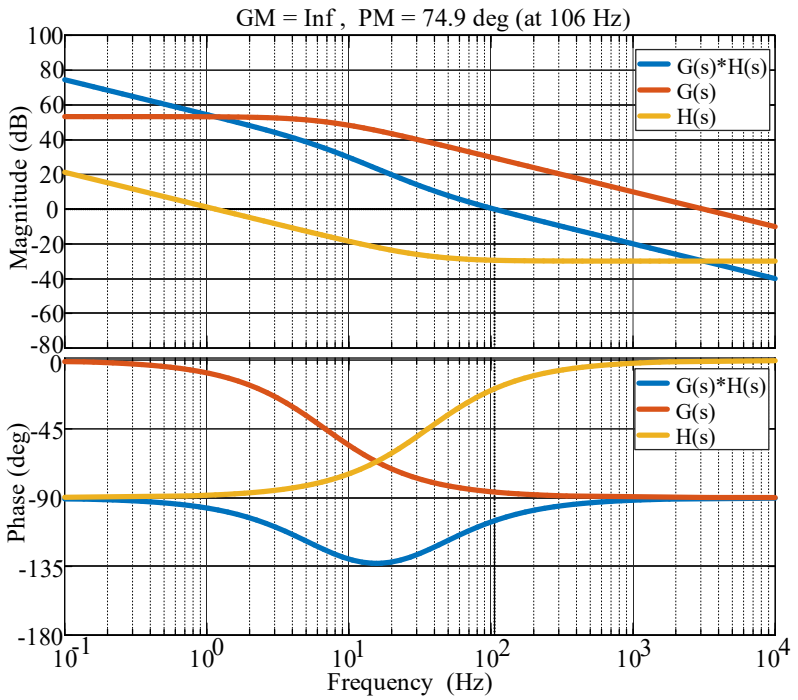


Fig. 6.8. Frequency response of plant transfer function G(s), and open loop transfer function G(s)*H(s).

$$G(s) = \frac{v_o(s)}{d(s)} = \frac{1036}{0.05249\,S + 2.247} \tag{6.27}$$

$$H(s) = 0.032 + \frac{7.226}{S} \tag{6.28}$$

With the designed controller, the proposed converter is simulated in PSIM 11.1 by setting the converter maximum duty cycle at a value defined by (6.5) to avoid the converter CCM operation during overloads. Fig. 6.9 shows the converter simulation results for input frequency 400 Hz at rated output power. Fig. 6.9(a) shows the converter simulated input currents. The converter input

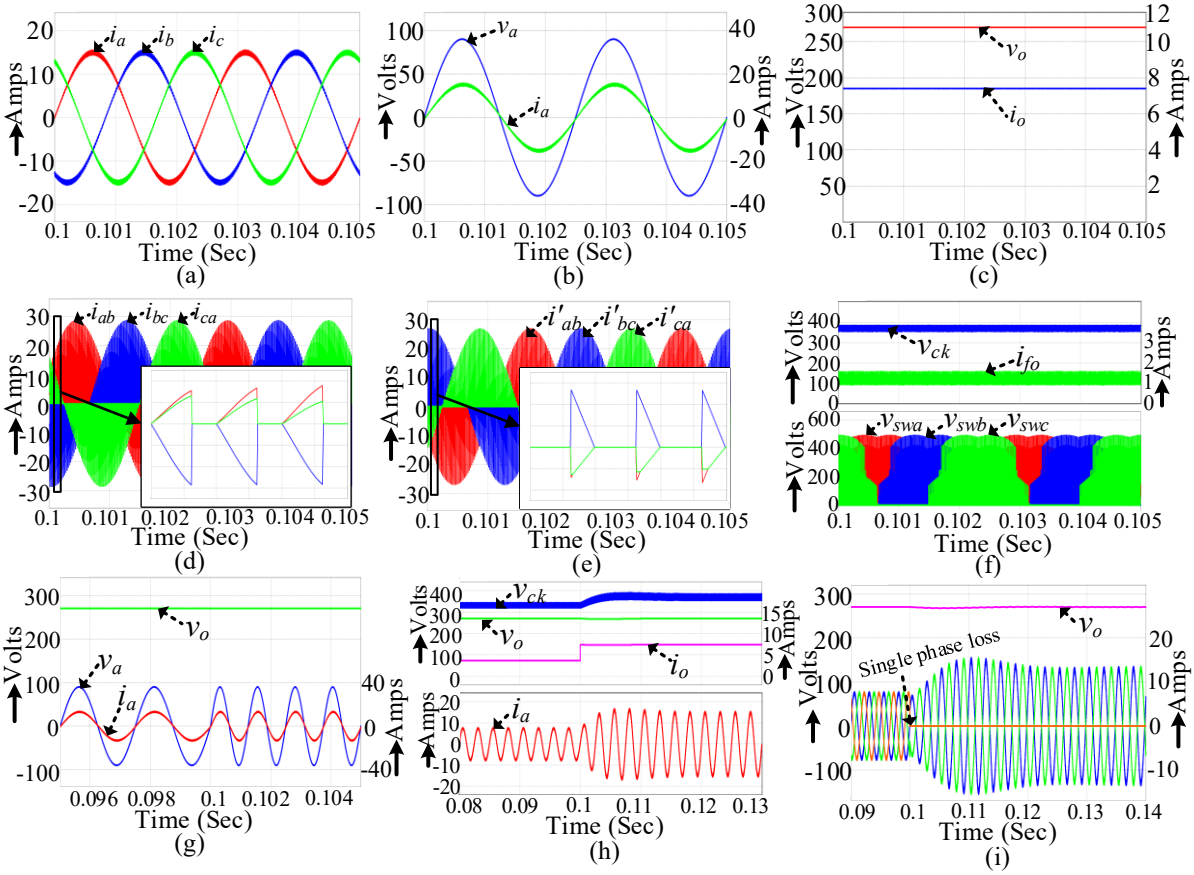


Fig. 6.9. Simulation results at rated output power, (a) converter input currents; (b) phase-A voltage and current; (c) converter output current and voltage; (d) flyback transformers primary currents; (e) flyback transformers secondary currents; (f) clamping capacitor voltage, forward converter output current and voltages across power switches; (g) converter input voltage and input current for input frequency change form 400 Hz to 800 Hz; (h) clamping capacitor voltage, output voltage and input current for load disturbance from 50% to 100% of rated power; (i) converter response for single-phase loss at half rated output power.

currents are sinusoidal and are closely tracking the input voltages as shown in Fig. 6.9(b), confirming the UPF operation. Fig. 6.9(c) shows the converter output voltage waveform, which is constant and settled at a designed value 270 V. Fig. 6.9(d) and Fig. 6.9(e) show the flyback transformers primary and secondary currents respectively. The transformers secondary currents are discontinuous, and are in good agreement with the analysis. Fig. 6.9(f) shows the clamping capacitor voltage, the forward converter output current, and the power switches voltages. As designed, the clamping capacitor average voltage is almost 400V, which validates the converter analysis and design. Fig. 6.9(g) shows the converter response for the input frequency change from 400 Hz to 800 Hz; the input current is closely tracking the input voltage, and the output voltage is steady without any oscillations. Fig. 6.9(h) shows the converter response for load change from 50% to 100%. The output voltage is closely tracking the reference voltage and is getting settled within the designed settling time of 10 ms, which proves the robustness of designed controller. Further, the proposed converter provides the fault tolerant operation for a single-phase loss and gives 50% of the rated output power without altering the controller. The reduction in output power is due to the duty cycle limit derived in (6.5). With a single-phase loss, the converter resembles a single-phase converter with line-to-line voltage as input source. Therefore, the output voltage is having second order supply frequency oscillations like a single phase PFC rectifier as shown in Fig. 6.9(i).

6.5.2 Experimental results

In this sub-section, the experimental results of the proposed converter from a scaled down 1.0 kW proof-of-concept laboratory prototype are presented. The ferrite core material is selected for flyback transformer and is designed for a magnetizing inductance of 120 μH. Fig. 6.10 shows the developed hardware prototype in the lab, where DSP TMS320F28335 is used as digital control platform, and IC HCNW3120 is used as gate driver. The hall- effect sensor LV-25P has been used for sensing the output voltage. Table 6.4 lists the components employed to develop the hardware prototype. The California-MX30 is used as source to generate 110 V variable frequency AC supply.

Fig. 6.11(a) shows the measured three-phase input voltages at 400 Hz. Fig. 6.11(b) shows the converter measured input currents and, output voltage at 1.0 kW output power. The input currents are balanced and sinusoidal, and the output voltage is steady at refence value 270 V. Fig. 6.11(c),

Table 6.4: Hardware setup component specifications

Component	**Specifications**
Switches	UJ3C065030K3S, 650 V, 62 A, 35 mΩ
Diodes	VS-65EPF06LHM3, 600 V, 65 A
Output capacitor, C	ESMQ401VSN471MQ50W, 4x470 µF
Filter capacitors, C_f	PHE845VR6680MR06L2, 0.68 μF
Filter inductors, L_f	1140-331K-RC, 330/2 μH
Clamping capacitor, C_k	PHE845VY6220MR06L2, 0.22 μF
Snubber capacitor	R75QD0470DQ30J, 470 pF
Snubber Resistor	EP5WS100RJ, 100 Ω
Transformers, T_a, T_b, T_c	55 x 28 x 21, EE Ferrite cores
Forward converter transformer	42 x 21 x 20, EE Ferrite core
Forward converter inductance, L_b	1140-102K-RC, 1.8 mH

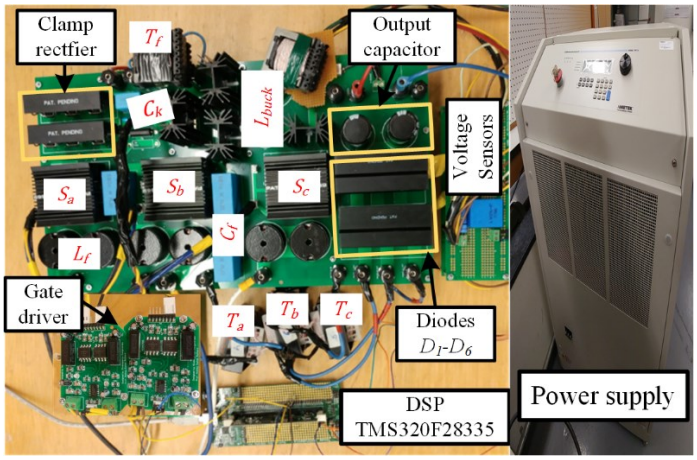


Fig. 6.10. The hardware laboratory prototype of the flyback-based converter.

Table 6.5: Converter measured input current THD (%), clamping capacitor average voltage, forward converter average output current for different output powers.

P_o, watts	**THD (%)**	**Average 'V_{ck}'**	**Average 'i_{fo}'**
250 W	2.67 %	305 V	0.15 A
500 W	3.26 %	327 V	0.24 A
750 W	3.85 %	350 V	0.30 A
1000 W	4.45 %	360 V	0.36 A

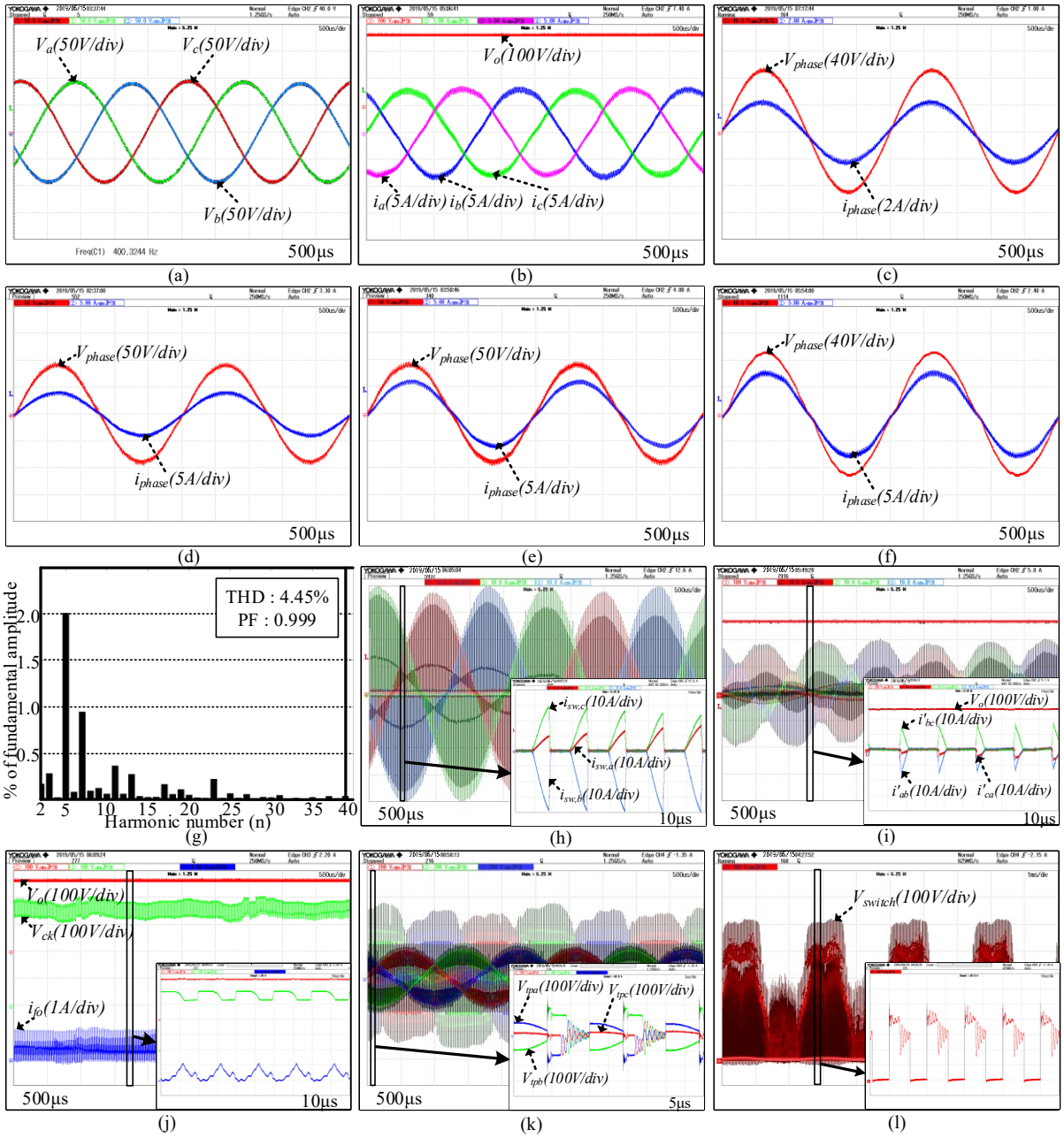
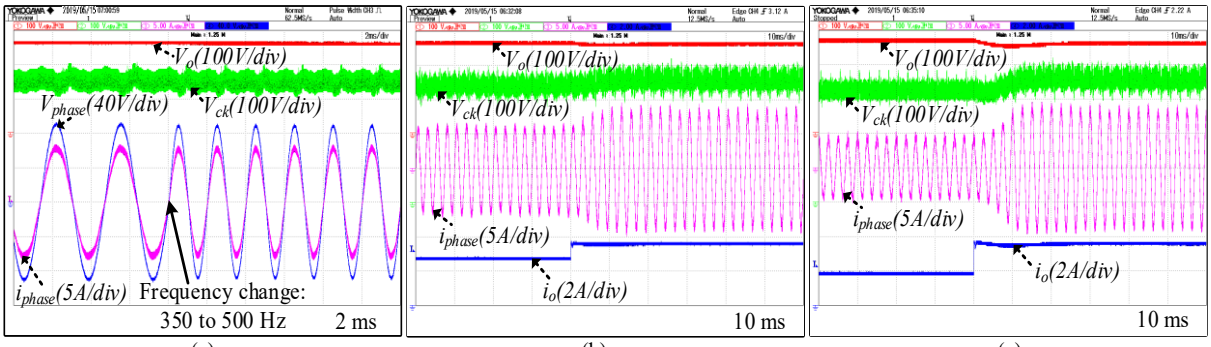


Fig. 6.11. Experimental results: (a) phase input voltages, 400 Hz; (b) phase input currents, and output voltage, at 1.0 kW output power; (c) phase input voltage, phase input current, at 0.25 kW output power; (d) phase input voltage, phase input current, at 0.5 kW output power; (e) phase input voltage, phase input current, at 0.75 kW output power; (f) phase input voltage, phase input current, at 1.0 kW output power; (g) input current harmonic spectrum at 1.0 kW output power; (h) switch currents; (i) flyback transformers secondary currents; (j) output voltage, clamping capacitor voltage, and forward converter output current; (k) flyback transformers primary voltages; (l) measured voltage across one of the power switches.

Fig. 6.11(d), Fig. 6.11(e), and Fig. 6.11(f) show the converter input voltage and input current waveforms of one phase at 250 W, 500 W, 750 W, and 1000 W output power, respectively. It should be observed that the input current is following the input voltage both in phase and shape at varying output power, confirming the converter UPF operation. Fig. 6.11(g) shows the input current harmonic spectrum at 1.0 kW output power, the measured input current THD is 4.45%. Fig. 6.11(h) shows the switch currents, which are $\sqrt{3}$ times of the transformers primary currents, and following the same shape of transformers primary currents. Fig. 6.11(i) shows the transformer secondary currents, which are discontinuous and validating the design. Fig. 6.11(j) shows the clamping capacitor voltage and forward converter output current at 1.0 kW output power. The measured clamping capacitor average voltage is 360 V confirming the analysis and design. Fig. 6.11(k) and Fig. 6.11(l) show the transformer primary voltages and switch voltages and their peak values are clamped at the designed value. Table 6.5 lists the measured input current THD, the clamping capacitor average voltage, and the forward converter average output current for different values of output power. The maximum measured THD is 4.45%, and the maximum clamping capacitor average voltage is 360 V.

Fig. 6.12(a) shows the converter response for the input frequency change from 350 Hz to 500 Hz. The converter input current is following the input voltage during frequency change as depicted in simulation. Fig. 6.12(b) and Fig. 6.12(c) show the converter dynamic response for the load change from 750 W to 1000 W, and from 500 W to 1000 W, respectively. In both the cases, the



(a) (b) (c)

Fig. 6.12. (a) converter output voltage, clamping capacitor voltage, input voltage, and input current for input frequency change; (b), (c) output voltage, clamping capacitor voltage, input current, and output current for load change from 0.75 kW to 1.0 kW, and from 0.5 kW to 1.0 kW.

output voltage is following the reference, and the clamping voltage transition is smooth, which proves the robustness of controller and the proposed clamping circuit.

6.5.3 Converter efficiency

The proposed converter itemized losses for the rated output power are listed in Table 6.6. The converter losses are calculated using the loss equations defined in appendix, and from the datasheet values of selected components. The converter measured efficiency curve for different loading is depicted in Fig. 6.13, where converter peak efficiency of 94.02% is recorded at rated load. The proposed converter efficiency is compared with state-of-the-art flyback converters and listed in Table 6.7. It is observed that the proposed converter and its clamping technique has high

Table 6.6: Calculated loss breakdown of the proposed converter for rated output power.

Description	**Value**	**Unit**
Output voltage, $\boldsymbol{V_o}$	270	V
Output power, $\boldsymbol{P_o}$	1000	W
Input voltage	110	V
Switching frequency, $\boldsymbol{f_s}$	50	kHz
Duty cycle, $\boldsymbol{d}$	0.645	
Clamping capacitor voltage, $\boldsymbol{V_{ck}}$	350	V
Forward converter duty cycle, $\boldsymbol{d_f}$	0.4	
Losses		
Power switches conduction losses	6.27	W
Power switches switching losses	6.38	W
Power diodes	5.34	W
Flyback Transformers	9.96	W
Output filter capacitors	2.07	W
Input filter inductors	9.07	W
Input filter capacitors	3.95	W
Total power converter losses	43.04	W
Clamping diodes	0.91	W
Clamping capacitor	0.14	W
Forward switches	0.33	W
Forward diodes	0.63	W
Forward inductor	1.66	W
Forward transformer	1.69	W
Total clamping converter losses	5.36	W
Switches gating losses	0.17	W
Auxiliary losses	15.0	W
Total losses	63.57	W
Efficiency	94.02	%

Table 6.7: Comparison of proposed converter efficiency with state-of-the-art converters.

Description	Rated Power (kW)	Efficiency (%)
Modular flyback converter [63]	0.5	85.0
Single-switch flyback converter [104]	0.5	86.2
Two-switch flyback converter [105]	1.2	87.0
Interleaved flyback converter [89]	6.5	87.1
Proposed converter	1.0	94.02

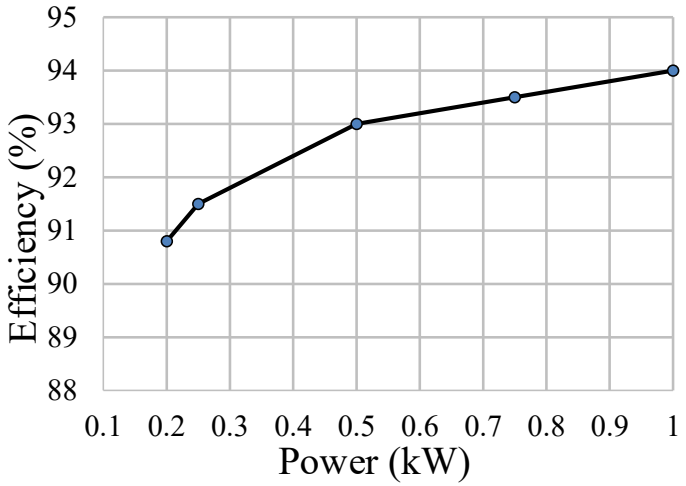


Fig. 6.13. Measured efficiency curve for different output powers.

efficiency, it is due to the utilization of captured transformer leakage inductance energy which is not the case in state-of-the-art converters where the captured energy is dissipated in clamping resistor as heat.

6.5.4 Converter operation with single-phase loss

The proposed converter continues to operate in case of single-phase loss, which is one of the desired features in aircraft application. With single-phase loss, the proposed converter resembles a single-phase converter with line-to-line voltage applied at input, as shown in Fig. 6.14(a). As stated in previous sections, the converter operation has duty-cycle limiter to avoid the converter CCM operation. Therefore, with a limit on duty cycle defined by (6.5), the converter delivers 50% of the rated output power with single-phase loss without change in control system. Since the converter duty cycle is limited, the currents flowing through the switches and diodes are also

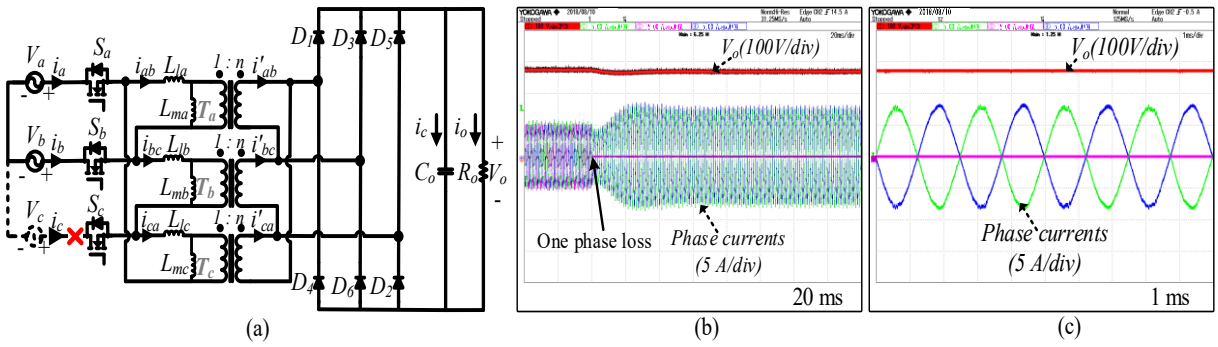


Fig. 6.14. (a) Converter structure with single-phase loss; (b) converter operation during single-phase loss; (c) converter input currents and output voltage with single-phase loss.

limited. Therefore, the proposed converter works without oversizing the semiconductor components with single-phase loss for 50% of rated output power. Fig. 6.14(b) shows the converter operation during single-phase loss at 50% of rated output power. It is observed that the converter input current peaks are raised by 73.2% to maintain the power balance. Since the converter operation is still in DCM, the input currents are still sinusoidal and of opposite polarity to each other to make the total sum zero and is shown in Fig. 6.14(c). It should be noted that the converter output voltage is constant and closely tracking the reference voltage without change in control circuit.

6.6 Conclusion

A three-phase single-stage isolated flyback-based PFC converter with a novel clamping technique to capture and utilize the transformers leakage energy is proposed and studied. The converter UPF operation for all supply frequency variation is obtained by using the inherent resistance property of DCM. The converter control circuit requires only one sensor, which reduced the system cost and control complexity as well as increased the system robustness to HF noise. By using the proposed clamping circuit, the transformers leakage inductance energy is successfully captured in a single clamping capacitor, and fed to the DC-link using two-switch forward converter. Thus, the overall efficiency of the converter is improved. The converter steady-state analysis and the design equations are presented in detail. The converter small-signal model is also presented for closed-loop controller design.

The converter analysis and the design are first verified with the simulation results, and later with the experimental results from a 1.0 kW laboratory prototype. It is demonstrated that the input currents are following the input voltages both in phase and shape for different supply frequency, and it is a desired feature for MEA application. Using the proposed clamping circuit, the surge voltage across switch due to the transformers leakage inductance during switch state transition are successfully clamped at the designed value. The designed controller robustness is confirmed for both the input frequency and load perturbations. The converter detailed loss breakdown at rated output power is provided, and the proposed converter efficiency is compared with the state-of-the-art converters. The proposed converter and its clamping technique has high efficiency due to the utilization of the transformers leakage inductances energy. It is also demonstrated that the converter provides the fault-tolerant operation for single-phase loss. An input current THD of 4.45 % (< 5 %), and a high efficiency of 94.02 % (> 90 %) are recorded from the developed laboratory prototype.

Chapter 7 : Conclusions and Future Research

This Chapter discusses the contributions of this research and the thesis in section 7.1 and provides the guidelines for future scope of this research based on the findings in Section 7.2.

7.1 Contributions of the thesis

In MEA, three-phase AC-DC PFC converters of several kilowatts are required. This thesis focuses on active AC-DC PFC isolated and non-isolated topologies as a solution to replace the currently employed passive multi-pulse ATRU and TRUs with an objective of strictly fulfilling the requirements of the next generation MEA's.

In another words, this thesis contributes to the analysis and design of buck-boost type AC-DC PFC converters with a focus on minimizing the total number of components, and improving the overall system efficiency. The proposed converters are studied, analyzed, and designed for DCM operation in order to simplify the control circuit and to reduce the number of sensors, which consequently increases the converter reliability, and robustness. Simple control, high input power quality, improved efficiency, and improved reliability are the major highlights of the proposed DCM converter topologies.

1. At first, a three-phase modular single-stage isolated Cuk PFC converter, derived by combining three single-phase isolated Cuk structures with output ports connected in parallel, is proposed and analyzed in Chapter 2. The highlights of the proposed converter are inrush current limitation, no input filter requirement, can be paralleled easily for high power design, and operational even with two-phase loss. A high efficiency of 91.5 % (> 90 %) and input current THD of 4.87 % (< 5 %) are recorded from the developed prototype at rated output power. Though the phase-modular converters are easy to implement, and provide quick repair and maintenance but they need high number of components for their operation and also three semiconductor devices from each phase are in the current conduction path which increases the converter conduction losses and reduces the converter efficiency.

2. A new direct three-phase non-isolated Cuk-derived PFC converter with reduced number of components and conduction losses is proposed and analyzed in Chapter 3. The novelty of the proposed converter is demonstrated by comparing it with the state-of-the-art converters. The key contribution of the proposed converter is that only one semiconductor device from each phase is in the current conduction path throughout the converter operation which reduced the converter conduction losses, and increased the converter efficiency. A low input current THD 3.91 % (< 5 %) and high efficiency 94.29 % (> 90 %) are recorded at 2.0 kW rated output power from the developed hardware prototype. Though the proposed converter is optimized in terms of semiconductor count and conduction losses but needs two DC-link capacitors at the output that added extra capacitive losses.

3. A new direct three-phase non-isolated buck-boost-derived PFC converter with reduced capacitive losses is proposed and analyzed in Chapter 4. It has been compared with the state-of-the-art converters and demonstrated its novelty. The key contribution is the less number of components for its operation, and only one semiconductor device from each phase conducts at a time. A high efficiency of 95.52 % (> 90 %) and low input current THD of 2.76 % (< 5 %) are recorded at 2.0 kW rated output power from the developed hardware prototype.

4. An interleaved topology of the three-phase non-isolated buck-boost-derived PFC converter for high power design with reduced filter losses and size is studied and analyzed in Chapter 5. This contributes to 50% reduction in the unfiltered ripple current magnitude, and to reduce the input filter requirement substantially by doubling the effective ripple frequency. The size of the filter inductors, and the heat sink requirements are estimated analytically for both the two-cell interleaved and single-cell converters. It is demonstrated that the proposed topology contributes to 50 % reduction in filter inductors size and reduced the heat sink requirement as compared to the single-cell converter. It is also demonstrated that the lifespan of output electrolytic capacitors enhanced by more than two times in interleaved converter when compared to the single-cell converter, which shows the higher reliability of proposed interleaved topology. An input current THD as low as 2.7% (< 5 %)

and a maximum efficiency of 96.3 % (> 90 %) are recorded from the developed prototype at 2.0 kW rated output power.

5. An isolated topology of the three-phase non-isolated buck-boost-derived PFC converter with a novel clamping circuit to capture and utilize the transformers leakage inductances energy for improved efficiency is proposed and analyzed in Chapter 6. The novel clamping circuit comprises of one three-phase full-bridge rectifier and single clamping capacitor contributes to capturing leakage inductances energy. The captured energy is fed to the DC-link by using an auxiliary two-switch forward converter, which enhanced the converter efficiency. A high efficiency of 94.02 % (> 90 %) and an input current THD of 4.45 % (< 5 %) are recorded at rated output power.

In addition to the above contributions, the following conclusions which are common to all the proposed topologies are summarized as follow:

- The converters are designed for DCM operation, and obtained UPF at AC mains with less input current distortion for different loads and for wide range of supply frequencies 360 to 800 Hz.
- All the switches are operated with zero current switching turn-on, and the diodes are with zero reverse recovery losses which are inherent to the DCM operation.
- All the converters require high current rated semiconductor components due to the high current peak offered by the DCM operation.
- The converters output voltage is regulated with a simple voltage control loop, and all the power switches are driven with the common gate signal, which simplified the control effort substantially.
- Only single sensor is required for PFC control implementation, which makes the converter more economical, increases the reliability, improves the robustness to high frequency noise, and increases the system power density.
- The steady state operation, DCM condition, design equations, and the components stress expressions are reported in detail.
- The small-signal models for all the converters using CIECA approach are developed, and a detailed discussion for the closed-loop controller design is provided.

- Detailed simulation results as well as experimental results are provided to validate the analysis, design, and their feasibility.
- Through simulation it is observed that proposed converters power quality and their operation are very sensitive to the DCM inductance values, and not much sensitive to the filter capacitance values.
- Converters operation is smooth when rated constant power load is applied and removed, and the output voltage is well following the reference voltage.
- An input current THD less than 5 %, and efficiency greater than 90 % are recorded at rated output power from the developed prototypes.
- The hardware's developed are of concept-proof-prototypes to verify the proposed concepts and are not optimized in terms of efficiency and switching frequency.
- The converters operation for single-phase loss for 50 % rated power operation has been discussed, and the relevant results have been presented.

7.2 Future scope of research

The recommendations for future research based on the findings from this research work are as follow

7.2.1 Three-phase modular Cuk converter with active clamping circuit

The three-phase modular isolated Cuk converter presented in Chapter 2 suffers from low efficiency due to the employment of passive RCD dissipative clamping circuit across each transformer. If active-clamping circuits are employed across each transformer as shown in Fig. 7.1, better converter efficiency can be obtained. In the control, it should be ensured that the active-clamping circuit switching operation should not interrupt the main circuit operation, and also the modifications to the control circuit should be minimum so that the merits of the existing converter can be retained. One of the possible option is to operate the active-clamping switches with constant duty cycle, and the gating signal should be provided during the DCM period (when all the converter semiconductor devices are in OFF state) of the converter for very short time compared to the switching period e.g. 4 % of the switching period.

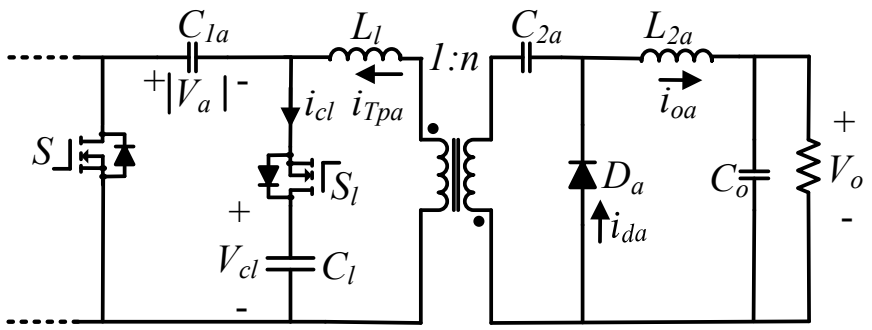


Fig. 7.1. Single-section of the three-phase modular isolated Cuk converter with proposed active clamping circuit.

7.2.2 Three-phase Cuk-derived PFC converter with less capacitive losses

A modification to the three-phase Cuk-derived PFC converter proposed in Chapter 3 in order to reduce the capacitive losses by eliminating the two DC-link capacitors, is shown in Fig. 7.2. In the modified circuit, the output inductors are connected in delta-configuration and the DC-link capacitors midpoint is eliminated. The operation, analysis, design, and feasibility analysis of this topology can be considered as the extension of this research work.

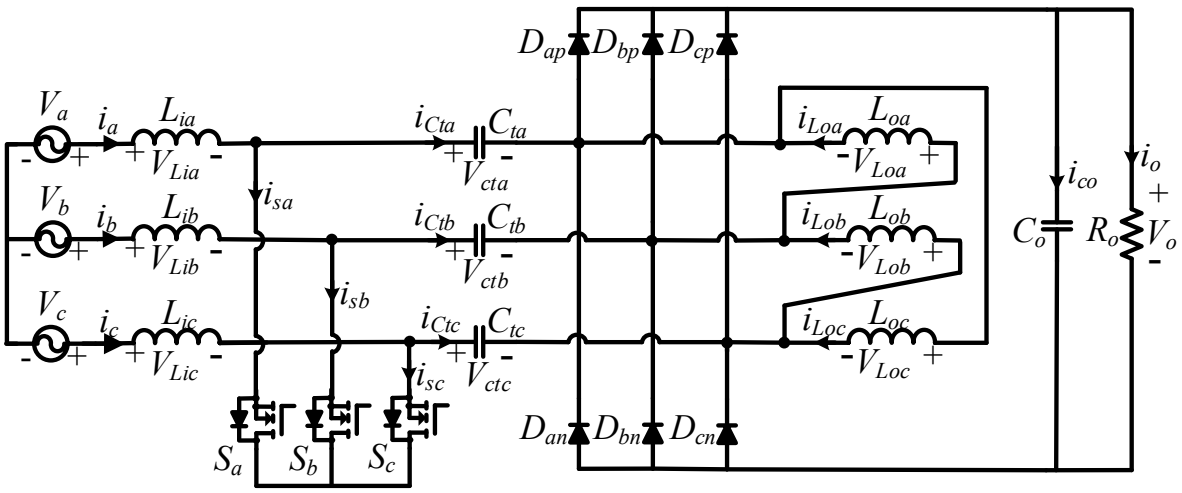


Fig. 7.2. Proposed modified three-phase Cuk-derived PFC converter with one DC-link capacitor.

7.2.3 Design and development of EMI/EMC filter

The design and development of EMI/EMC filters for the proposed converters and investigating their high frequency conducted emissions to meet the levels mentioned in airborne standards [14], [15].

7.2.4 Current-fed Bidirectional DC-DC converters

The adaptation of 270 V DC bus system in MEA created a requirement for DC-DC converters to provide 28 V DC power used by some equipment such as long-term and short-term storage (battery and supercapacitors), and the aircraft conventional electronic loads. The desirable characteristics for the DC-DC converter are high power density, high efficiency, and bidirectional power flow control along with galvanic isolation [107]. In literature, the voltage-fed dual active bridge (DAB) bidirectional DC-DC converter solutions have been reported for MEA application [108], [109]. There have been limited literature reported for studying the feasibility of current-fed bidirectional converters for MEA application. When compared to the voltage-fed DAB converter, the current-fed DAB converter has several advantages such as lower peak and circulating current, reduced rms current, lower transformer kVA ratings, and better efficiency [110]. Further, the current-fed DAB converter provide better battery utilization compared to the voltage-fed DAB converter. Thus, the study of the current-fed bidirectional DAB DC-DC converters, and reviewing their feasibility for MEA application can be considered as one of the future scope of research.

7.2.5 Bidirectional AC-DC converters

In future aircraft, feedback of energy into the mains might be allowed. Therefore, another possible scope of research could be the modification of the proposed unidirectional AC-DC converters for allowing the bidirectional power flow with minor changes in control circuit.

7.2.6 CCM operation of proposed converters

The modification of the proposed converters for CCM operation by replacing the unidirectional voltage blocking switches with the bidirectional voltage blocking switches and modifying the PFC control accordingly could be a possible scope of future research. The comparison of the modified CCM operated converters with the proposed DCM operation in terms of cost, control effort, efficiency, and power density could also be considered as another possible scope of research.

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Appendix

Table A.1: Loss equations used to calculate the converter losses.

Description	Equation
Switch conduction loss	$i_{sw,rms}^2 R_{DS,on}$
Switch turn-off loss	$\frac{v_{sw,avg} i_{sw,avg} t_f f_s}{2}$
Switch output capacitance loss	$\frac{C_{oss}\, f_s}{2\pi} \int_0^{2\pi} v_{sw}^2(\omega t)\ d(\omega t)$
Switch gate drive loss	$C_{iss} V_g^2 f_s$
Diode conduction loss	$i_{D,rms}^2 R_D + i_{D,avg} V_{df}$
Diode output capacitance loss	$\frac{C_{odd}\, f_s}{2\pi} \int_0^{2\pi} v_{diode}^2(\omega t)\ d(\omega t)$
Inductor power loss	$i_{L,rms}^2 R_L$
Inductor core loss	$P_{c,limit} V_e$
Capacitor loss	$i_{C,rms}^2 R_{ESR}$

where

$i_{sw,rms}$ = Switch rms current, A

$R_{DS,on}$ = Switch drain-to-source on resistance, Ω

$v_{sw,avg}$ = Switch average voltage during turn-off, V

$i_{sw,avg}$ = Switch average current during turn-off, A

t_f = Switch fall-time, s

f_s = Switching frequency, Hz

C_{oss} = Switch output capacitance, F

C_{iss} = Switch input capacitance, F

V_g = Switch driving voltage, V

$i_{D,rms}$ = Diode rms current, A

R_D = Diode turn-on resistance, Ω

$i_{D,avg}$ = Diode average current, A

V_{df} = Diode forward voltage, V

C_{odd} = Diode output capacitance, F

$i_{L,rms}$ = Inductor rms current, A

R_L = Inductor DC resistance, **Ω**

$P_{c,limit}$ = Inductor core loss limit, mW/cm^3

V_e = Effective core volume, cm^3

$i_{C,rms}$ = Capacitor ripple rms current, A

R_{ESR} = Capacitor equivalent series resistance, **Ω**.

List of Publications

Journal papers

1. **S. Gangavarapu,** A. K. Rathore and D. M. Fulwani, "Three-Phase Single-Stage-Isolated Cuk-Based PFC Converter," in ***IEEE Transactions on Power Electronics***, vol. 34, no. 2, pp. 1798-1808, Feb. 2019.
2. **S. Gangavarapu** and A. K. Rathore, "Three-Phase Buck–Boost Derived PFC Converter for More Electric Aircraft," in ***IEEE Transactions on Power Electronics***, vol. 34, no. 7, pp. 6264-6275, July 2019.
3. **S. Gangavarapu**, A. K. Rathore and V. Khadkikar, "High-Efficiency Three-Phase Single-Stage Isolated Flyback-Based PFC Converter With a Novel Clamping Circuit," in ***IEEE Transactions on Industry Applications***, vol. 56, no. 1, pp. 718-729, Jan.-Feb. 2020.
4. **S. Gangavarapu** and A. K. Rathore, "A Three-Phase Single-Stage Isolated Flyback-Based PFC Converter With Leakage Energy Recovery Clamping Circuit," in ***IEEE Transactions on Transportation Electrification***, vol. 5, no. 4, pp. 1155-1168, Dec. 2019.
5. **S. Gangavarapu,** and A. K. Rathore, "A Three-Phase Single-Sensor based Cuk-derived PFC Converter with Reduced Number of Components for More Electric Aircraft" **accepted** for ***IEEE Transactions on Transportation and Electrification*****,** 2020.
6. **S. Gangavarapu,** and A. K. Rathore, "Analysis and Design of a Single-Sensor based Three-Phase Interleaved DCM Buck-Boost Derived PFC Converter" under review for ***IEEE Transactions on Industry Applications*****,** 2020.

Conference papers

1. **S. Gangavarapu**, A. K. Rathore, "Analysis and Design of a Three-Phase Cuk-derived PFC Converter," accepted for *IEEE APEC*-2020**.**
2. **S. Gangavarapu,** and A. K. Rathore, "Analysis and Design of Three-Phase Interleaved Buck-Boost Derived PFC Converter," *2019 IEEE Industry Applications Society Annual Meeting*, pp. 1-8, Baltimore, MD, USA, 2019.

3. **S. Gangavarapu,** and A. K. Rathore, "Analysis and Design of Three-Phase Single-Stage Isolated Flyback Based PFC Converter with a Novel Clamping Circuit," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1910-1917, Anaheim, CA, USA, 2019.

4. **S. Gangavarapu**, A. K. Rathore and V. Khadkikar, "A Three-Phase Isolated Buck-boost Derived PFC Converter with a Novel Clamping Circuit," *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1-5, Chennai, India, 2018.

5. **S. Gangavarapu**, A. K. Rathore and D. M. Fulwani, "Discontinuous conduction mode three-phase buck-boost derived PFC converter for more electric aircraft with reduced switching, sensing and control requirements," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1467-1472, San Antonio, TX, 2018.

6. **S. Gangavarapu,** and A. K. Rathore, "Analysis and design of three-phase single-stage isolated Cuk-based PFC converter," *2017 IEEE Industry Applications Society Annual Meeting*, Cincinnati, pp. 1-8, OH, USA, 2017.

7. **S. Gangavarapu,** and A. K. Rathore, "Three-phase interleaved semi-controlled PFC converter for aircraft application," ***IECON 2017*** *- 43rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 6652-6657, Beijing, 2017.