Small Signal Analysis and Control of Snubberless Naturally-Clamped Soft-Switching Current-Fed PWM DC/DC Converters

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ABSTRACT

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Koyelia Khatun

Power electronic is the prominent enabling technologies for the uninterruptible power supply (UPS), renewable energy sources, fuel cells, energy storage, electric transportation, electrical appliances and industrial processes. Owing to the challenges to safety, high step-up ratio, galvanic isolation, high-frequency (HF) transformer isolated topologies are introduced. Current-fed topologies offer the merits of high voltage gain, stiff input current and reduced peak currents. The major limitations of current-fed converters is the requirement of snubber circuit to clamp the turn-off voltage spike across the semiconductor devices. Passive snubbers leads to low efficiency as the energy absorbed by the clamping capacitor is dissipated in the resistor. Active-clamping results in better efficiency and simultaneously achieves zero voltage switching (ZVS) of the semiconductor devices. However, it needs floating active device(s) and high value of HF clamp capacitor for the effective voltage clamping. In addition, it suffers from the demerits of high current peak, high circulating current at light load, and reduced voltage gain. A new modulation technique was proposed to modulate secondary side controlled devices to clamp this voltage spike across the primary side devices eliminating the requirement of external snubber circuit. Steady-state analysis, power circuit design and steady-state performance have been reported for such class of snubberless naturally clamped current-fed converters. However, small signal analysis, control design, implementation, and transient/dynamic performance have not been studied yet.

The objectives of this thesis are to present small signal analysis, closed loop control design, and demonstrate the transient performance through simulation and experimentation of the snubberless naturally clamped current-fed half-bridge and push-pull dc-dc converter topologies. Small signal model has been derived using state space averaging. Closed loop control design is done employing two-loop average current control. Simulation results using PSIM 11.1.64 are reported to verify the converter performance with the designed controller. Experimental results from a 250W proof-of-concept hardware prototype are demonstrated to show the transient performance of current-fed half-bridge and push-pull dc-dc converter topologies.

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Chapter 1

Introduction

1.1 Background and Overview

Power electronics is an enabling and essential technology that deals with the conversion and control of electrical power through switch-mode electronic devices for a wide range of applications with high efficiency. These include dc and ac power supplies for various applications such as electrochemical processes, heating and lighting control, electronic welding, power line volt–ampere reactive (VAR) and harmonic compensators, high-voltage dc (HVDC) systems, flexible ac transmission systems (FACTs), alternative energy (solar, wind, fuel cells) power conversion, high-frequency (HF) heating, and motor drives. Power electronics for alternative energy sources, distributed generation, microgrid, and transportation electrification are major topics of research.

Solar power is known as the one of the most well-known energy sources. Now a days, it has been used extensively commercially. This system is noise free and work almost all the time. There is also low maintenance cost associated with it.

Solar and wind power are intermittent and very much subjected to weather conditions, so these sources produce discontinuous output. However, fuel cells are potential candidates for distributed generation. They can provide clean, efficient and environmentally friendly electric power. Fuel cells can provide the continuous power in all seasons as long as the continuity of the fuel is maintained [1-2]. Fuel cells can convert the chemical energy in the fuel into electrical energy. Fuel cells have lower emissions than combustion engines. Hydrogen fuel cells emit only water, so there are no carbon emissions.

Fuel cells are ideal for power generation, either connected to the power grid to provide supplemental power or installed as a standalone inverter as a back-up assurance for critical areas, which are inaccessible by power lines [1-2]. Fuel cell is non-polluting renewable energy and it has no moving parts during operation, they are more reliable than heat engines and have less noise pollution. As a result of promising power generation with high efficiency and low environmental impact due to no combustion of gas. The heat from a fuel cell can be used to provide hot water or

space heating for a home [3] or for co-generation [1-2]. They offer high efficiency than the conventional power plants [1-2] and the efficiency can be enhanced by utilizing the generated heat [1-2]. The fuel cells can be used in a wide range of applications of electrical power ranging from watts to megawatts [1-2].

In this thesis, the control of converter is developed under the scenario of fuel cell applications. However, the proposed novel soft-switching current-fed topologies and modulation techniques [4-5] are suitable for any general low voltage high current applications such as solar/fuel cell-based utility interactive inverters, UPS, micro grid, V2G, and energy storage.

1.2. Introduction of Fuel Cell Characteristics and Properties

A fuel cell is an electrochemical device that converts chemical energy of a fuel into electrical energy and generates heat as byproduct. It requires continuous flow of fuel for the consistent operation. Fuel cell stack is needed to boost the low voltage of the fuel cell. At a given fuel flow rate, fuel cell has an optimum current to supply maximum output power [1-2, 6-7].

Fig. 1.1 shows the variation of fuel cell voltage with current drawn from the fuel cell [6-7]. There are three regions for the whole characteristics curve and those are R-1, R-2 and R-3.

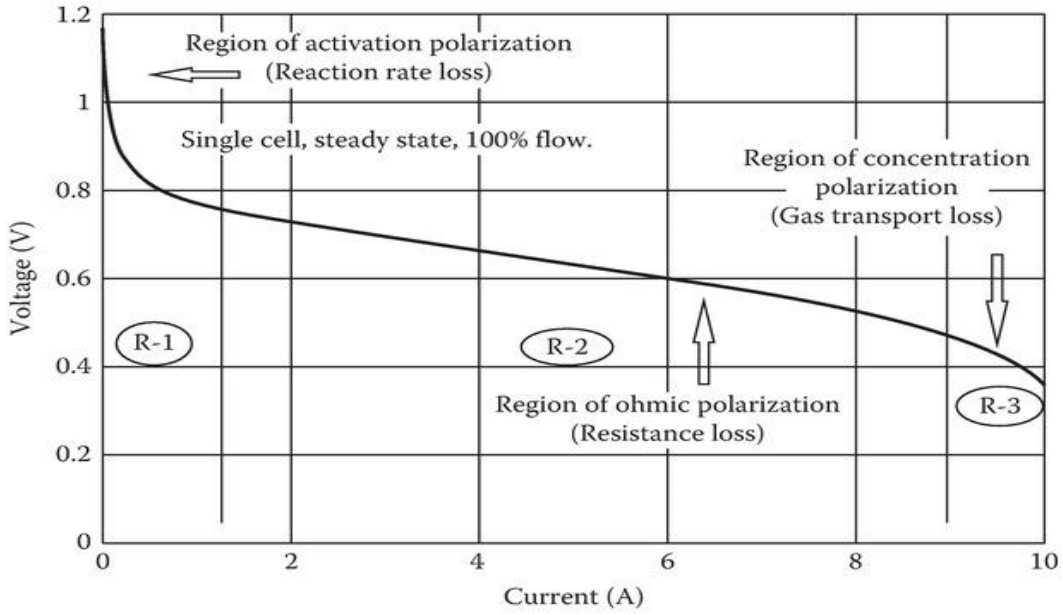


Fig. 1.1 Fuel cell voltage-current characteristic [1-2]

Fig. 1.1 shows that when current is drawn from the fuel cell, its actual operating voltage decreases from open circuit voltage [1-2]. The point at the boundary of regions R-2 and R-3 is regarded as the optimum/knee point or the point of maximum power density [1-2, 6-7]. An attempt to draw additional current (more than the optimum current) will shift the operating point, right to the knee/optimum point (region R-3), that will collapse the fuel cell voltage to zero sharply [1-2, 6-7], resulting in no power being supplied to the load. Prolonged operation in this region may damage the fuel cell [5]. Therefore, it is safe to operate the fuel cell to the left in region R-2 [1-2, 6-7]. Reverse current flow can damage the Fuel cell and so current feedback technique is avoided while designing the Fuel cell system.

1.3 Fuel Cell Applications

Fuel cells are seen as a secured output potential source for electric transportation due to zero-emission and back-up inverter power supplies due to continuous power flow in all seasons.

1.3.1 Fuel Cell Inverter

Solar power is intermittent and very much subjected to weather conditions so these sources produce discontinuous output. However, Fuel cells are ideal for power generation due to continuous power flow as long as fuel is provided. Fuel cell inverters provide continuous and secured output in all seasons. Low voltage energy storage system (ESS) in microgrid, electric vehicles (EVs), uninterruptible power supply (UPS), and DC microgrid are also within the scope of low voltage high current applications. The advantage of using a fuel cell to provide the chemical to-electrical energy conversion is high. This conversion ratio can be boosted by using the heat by product from home water and space heating.

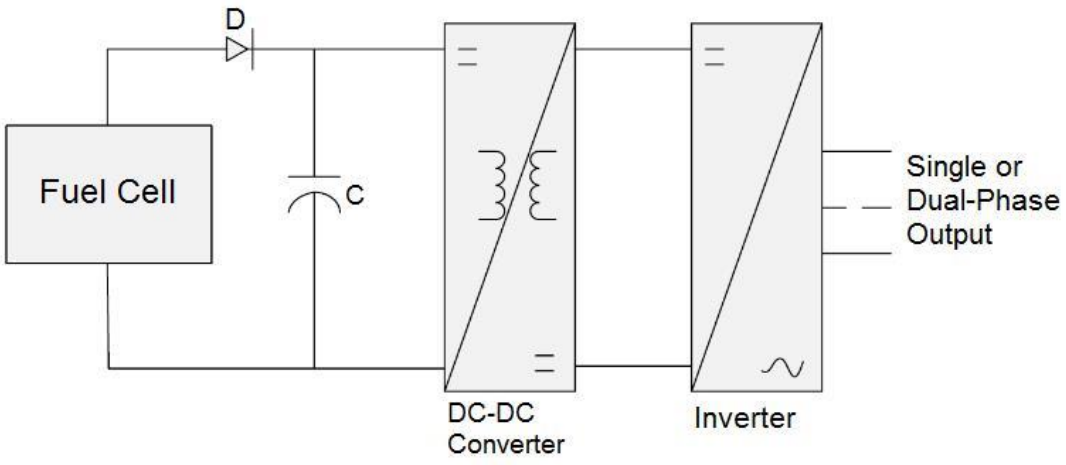


Fig 1.2 Block diagram of a fuel cell inverter system.

Fig. 1.2 shows typical fuel cell inverter system in which fuel cell DC power is converted into utility interactive AC power. DC-DC converter is a part of this system, required to step-up the low fuel cell stack voltage to peak of the utility line voltage at the intermediate DC link. Power flow control strategy is very important to manage the power distribution in between fuel cell (FC), Energy storage (ES) and motor drive. The design of power flow strategy will affect the size and lifetime of ES, efficiency of system, dynamic performance and fuel cell. The inverter deals with high voltage low current application. However, fuel cell is low voltage source therefore, DC-DC converter is applicable to boost up fell cell stake voltage to the to peak of the utility line voltage at the intermediate DC link. So, the efficiency of the whole system depends mainly on the efficiency of the front-end DC-DC converter. Therefore, a suitable front-end DC-DC converter topology must be selected and designed to realize a highly efficient system.

1.3.2 Transportation

Recently, transportation electrification has been an emerging topic of research owing to its merits of zero emission, positive impact on health, and its contribution towards clean atmosphere. With the developing concepts of smart grid and micro-grid, smart meters, smart homes, smart buildings etc. EVs have also recently emerged as a mean of mobile energy storage for addressing energy fluctuations in the power network. Battery based Electric Vehicles (EVs) and Fuel cell vehicles (FCVs) are emerging as viable solutions for transportation electrification with lower emission, better vehicle performance and higher fuel economy [4]. EVs and FCVs are emerging means of

transportation using 3-phase electric motor for propulsion. They propel much more quietly, smoothly, and efficiently needing less maintenance than internal combustion-based vehicle with zero emission resulting in nature and environment friendly mobility [8]. Fuel cell vehicles (FCVs) are part of the continuum of electric drive technologies, which are projected to capture an increasingly large share of the global passenger car and transit bus markets [8]. A diagram of a typical FCV propulsion system is shown in Fig. 1.3

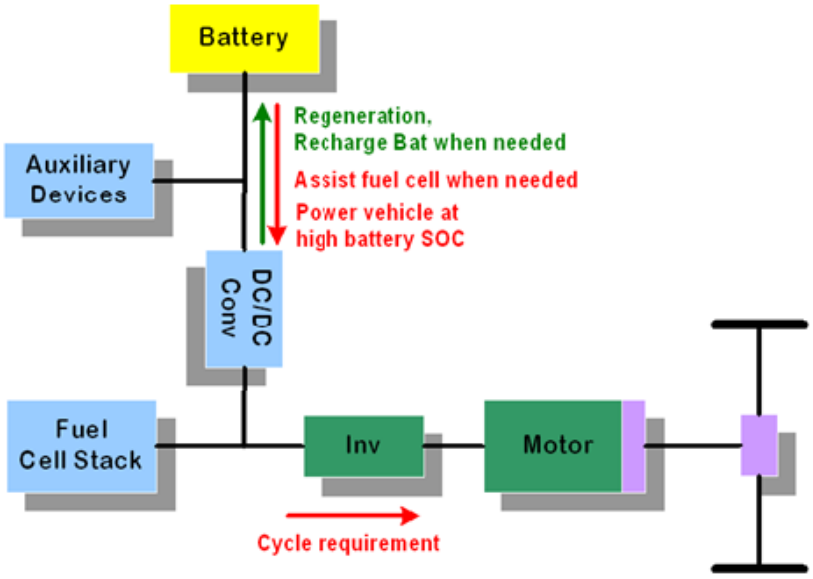


Fig. 1.3. Diagram of a FCV propulsion system.

For the passenger car market, fuel cells offer the benefits of zero emissions operation without the range and charging limitations of pure battery electric vehicles (EVs). In Chicago (USA), Vancouver, BC (Canada) And Germany, not only FCVs cars but also local bus transportation system have been tested on road. Automotive industries like Honda, Toyota, GM, Ford and Kia Ria are designing their fuel cell vehicles [9]. Ballard designed fully integrated fuel cell modules delivering 75 kW and 150 kW for local bus transportation in London which operates up to 19 hours without refueling [10]. As one of the essential enabling technologies of FCVs, power converters play a vital role in the commercialization of FCVs. FCVs offer zero emission, satisfied driving range, and short refueling time, and therefore FCVs exhibit significant potential for transportation.

1.4 Role of energy storage in FCVs

In FCVs, basically fuel cell stack oxidizes hydrogen gas and generates electrical energy in DC form. Power converters are responsible for conditioning the generated electrical energy to propel the vehicle smoothly and efficiently.

Operating point of fuel cell varies with electrical load demands. As this operating point is function of fuel cell, so it must be adjusted for efficient operation of fuel cell. There should have good balance between reactant supply, heat and water management and pressure drop. So, the flow rates of both fuel and oxidant are adjusted to ensure this balance. One well-known problem of fuel cell system is that it has low dynamic response time due to its low internal electrochemical and dynamic characteristics. The low-reactant condition caused by the load transient is harmful to fuel cell as it shortens the life of fuel cell. The difference between the time constants of the fuel cell and electrical load calls for an energy storage unit that would supplement the peak power demand from the fuel cell during transients. This slow response time should be compensated under quick load variation condition by adding a separate energy storage device, such as battery, ultra-capacitor which can be used to supply power to the load during all transient periods.

The advantages of using the secondary sources are [11-12]:

1. Compensates for the slow fuel cell dynamics
2. Responds to the fast-changing electrical load during transients
3. Provides the power to the load until the fuel cell output is adjusted to match the new steady-state demand.

Two possible solutions for separate energy storage devices are:

1. Batteries
2. Ultracapacitors

Between the two mentioned solutions, ultracapacitors offer better power density [11-12], more charging and discharging cycles during their life time [11-12], very good charge/discharge efficiency and can be constructed in modular or stackable format power density [11-12]. Ultracapacitors can also provide large transient power instantly to support the increased load demand [11-12]. On the other hand, batteries offer high energy density. Ultracapacitors aren’t

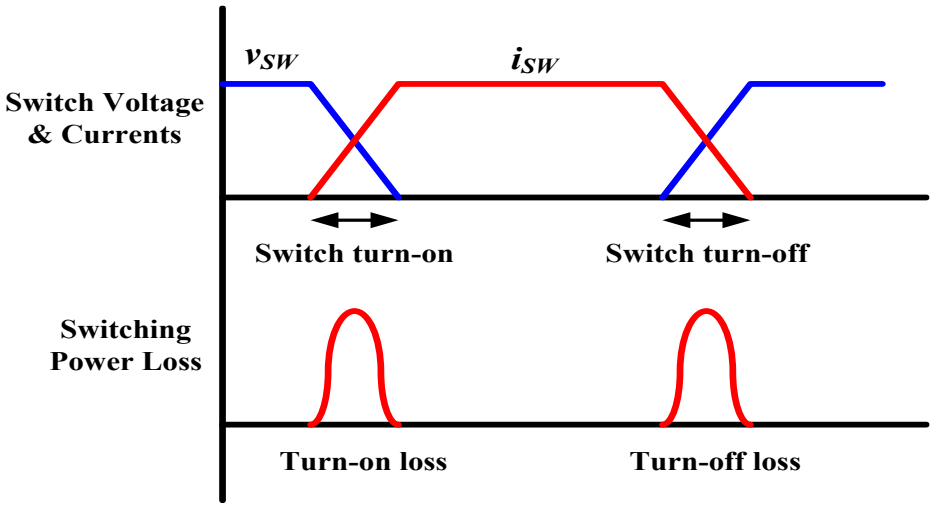
well-suited for long-term energy storage. The discharge rate of ultracapacitors is significantly higher than lithium-ion batteries; they can lose as much as 10-20% of their charge per day due to self-discharge. While batteries provide a near-constant voltage output until spent, the voltage output of capacitors declines linearly with their charge. Therefore, for vehicle application, where transients are frequent due to speed variation, braking, etc., battery is preferred.

1.5 High frequency DC-DC converter

Fuel-cell stack is characterized by low and unregulated DC output voltage. Fuel cell is large variation of low output voltage under various load conditions. The voltage conversion ratio must be very high to meet the requirement of load voltage as shown in Fig. 1.2 and 1.3. Therefore, transformer is necessary to boost-up the voltage. It also offers isolation and ensure the safety of operation. High frequency (HF) transformer is to realize a compact, low-cost, light weight system [13]. A suitable front-end DC-DC converter topology must be selected and designed to realize a highly efficient system as it deals with the higher current from the fuel cell stack.

1.6 Soft switching in DC-DC converter

DC-DC converters are classified into hard-switching and soft-switching converters. The concept of hard-switching manifests the overlap of device voltage and device current during switching transition, results into switching losses that is proportional to device switching frequency as shown in Fig. 1.4. This overlap causes energy losses which can be minimized by increasing *di/dt* and *dv/dt*. However, high switching frequency introduced fast changing of *di/dt* and *dv/dt* that causes electromagnetic interference (EMI) [14-15]. Hard switching has numerous well-known drawbacks including switching losses. Switching losses increase with increasing of switching frequency, therefore efficiency of converter reduces requiring increased cooling requirements.



1.4 Switching losses in hard switching circuit.

Hard-switching limits the maximum switching frequency operation of the semiconductor devices. Lower switching frequency increases the size of the magnetic components and filters –which adds to the cost, size and weight [15]. An effective approach to deal with these issues is that the use of soft-switching techniques, which can shape the rising and falling of current through and voltage across the semiconductor devices and eliminate/limit the switching losses in the semiconductor devices. This circuit, then, can operate at higher switching frequency to reduce the size, weight, and cost of the converter as well as to achieve higher efficiency [16-17]. Soft switching introduces any of electrical parameter (current and voltage) to zero before turning on or off the switch, which reduces the switching losses of converter and minimize EMI. Soft-switching can be classified into zero voltage switching (ZVS) and zero current switching (ZCS) as shown in Fig. 1.5.

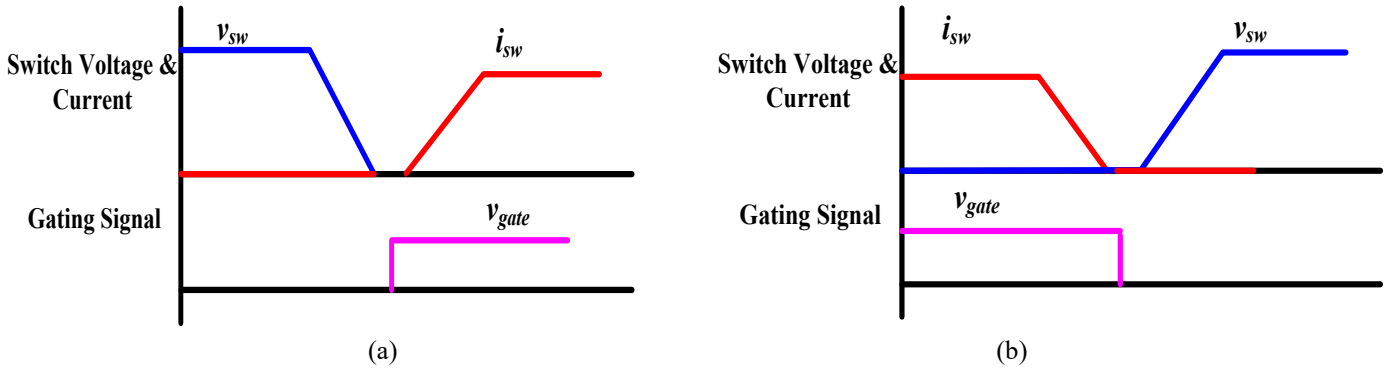


Fig. 1.5. Soft-switching of the semiconductor devices (a) zero voltage switching (ZVS) and (b) zero current switching (ZCS)

A. Zero voltage switching (ZVS):

If the voltage across a switch is reduced to zero before applying the gating signal to the switch to turn-it on, called as zero voltage switching (ZVS). Fig 1.5(a) shows the ZVS waveform across the switch. Turn-off losses can be reduced by placing a capacitor across the switch. Since, the snubber capacitor is never discharged through the switch; snubber discharge resistor is not required, resulting in lossless snubber [16-17].

B. Zero current switching (ZCS):

If the gating signal to a switch is removed after the current through a switch reaches naturally zero, called zero current switching (ZCS). Fig 1.5(b) demonstrates the ZCS waveform where current reaches to zero naturally. There is no turn-off losses in the switch. The switch is subjected to turn-on losses. Snubber capacitor is discharged through the switch when it is turned on, resulting in a large current peak through the switch. Therefore, a resistor is connected in series with each snubber capacitor across the switch to limit this peak current through the switch. Losses in these snubber resistors increase with increase in switching frequency and supply voltage [18].

1.7 HF Transformer Isolated DC/DC Converter Topologies

DC-DC converters can be categorized into two types: Voltage-fed converter and Current-fed converter. Each type can further be classified into pulse width modulation (PWM) and resonant converters. Voltage- fed converter has a large capacitor across the input as shown in Fig. 1.6, however current- fed converter employs large inductor in series with input as shown in Fig. 1.7.

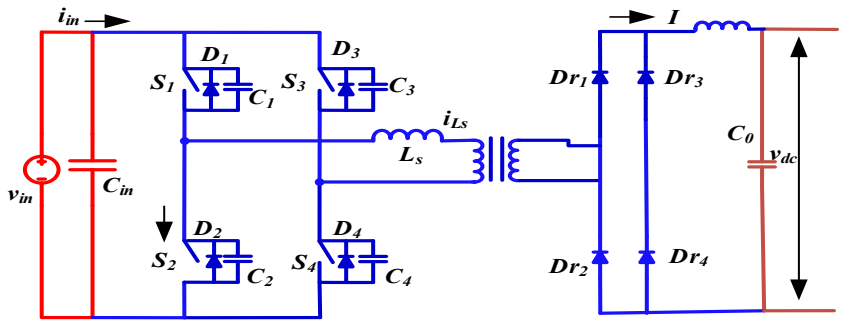


Fig 1.6 Voltage-fed full-bridge converter.

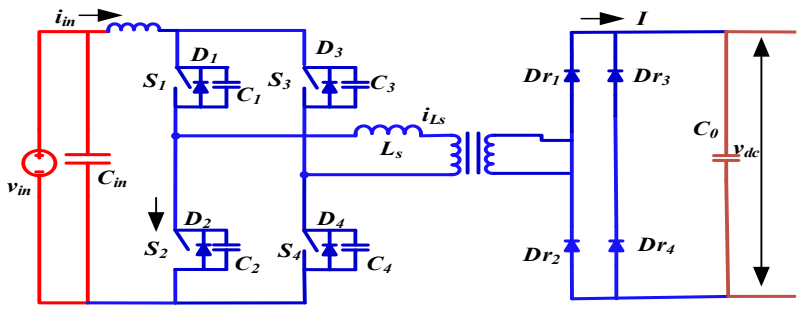


Fig 1.7 Current-fed full-bridge converter.

1.7.1 Voltage-fed PWM DC/DC converter

Voltage-fed isolated PWM converters can be divided into the two-types:

1. Single-ended topology (flyback and forward) (low power applications, < 500 W)
2. Doubled-ended topology (half-bridge, full-bridge, and push-pull) (usually up to 5 kW)

The transformer core utilization of the double-ended topologies is better, which affects the size and weight of the converter crucially. Besides, the transformer of double-ended topologies can be further operated and optimized over full duty cycle range [14]. Also, double ended topologies are modular, scalable and are preferred for higher power applications. Therefore, the double-ended topologies are suitable for FCVs where high power density and high-power transferring ability are desired. However, the voltage fed converter suffers from limited soft-switching range, voltage ringing across rectifier diodes, high circulating current through devices, duty cycle loss (inductive output filter) and it provides low partial load efficiency for low voltage high power specifications with wide input voltage variation [19].

1.7.2 Current-fed PWM DC/DC converter

Voltage-fed topologies employ considerably large electrolytic capacitor to suppress the large input current ripple, resulting in large size, high cost and shortened lifetime. Compared with voltage-fed converters, current-fed converters exhibit the following merits:

1) Smaller input current ripple is beneficial to extract and maintain stable maximum power point from fuel cell system and extend its lifespan.

2) Lower transformer turns-ratio: Current-fed converters are boost-derived converters and have built-in boost function. Therefore, current-fed converters have lower transformer turns ratio, which can simplify the design.

3) Negligible diode ringing and free from duty cycle loss due to capacitive output filter.

4) Easier current control ability. The input current can be directly and precisely controlled. Besides, the fuel cell stack output current is proportional to hydrogen flow rate. Therefore, if the fuel cell stack current is directly and precisely controlled, the amount of hydrogen utilized in a direct hydrogen system could be better-controlled [20].

Owing to these merits, current-fed converter is suitable for low voltage high current applications, in particular for high voltage gain applications with wide input voltage variation. Different topologies of PWM current-fed converters are illustrated in Fig 1.8, i.e., full-bridge, half-bridge, and push-pull. For the high voltage side rectifier stage, some popular topologies like full-bridge diode rectifier, half-bridge voltage doubler, and center-tapped rectifier are shown. However, the major drawback of using current-fed converter is device voltage spike/overshoot at device commutation (turn-off) due to energy stored in leakage inductance of the transformer [21].

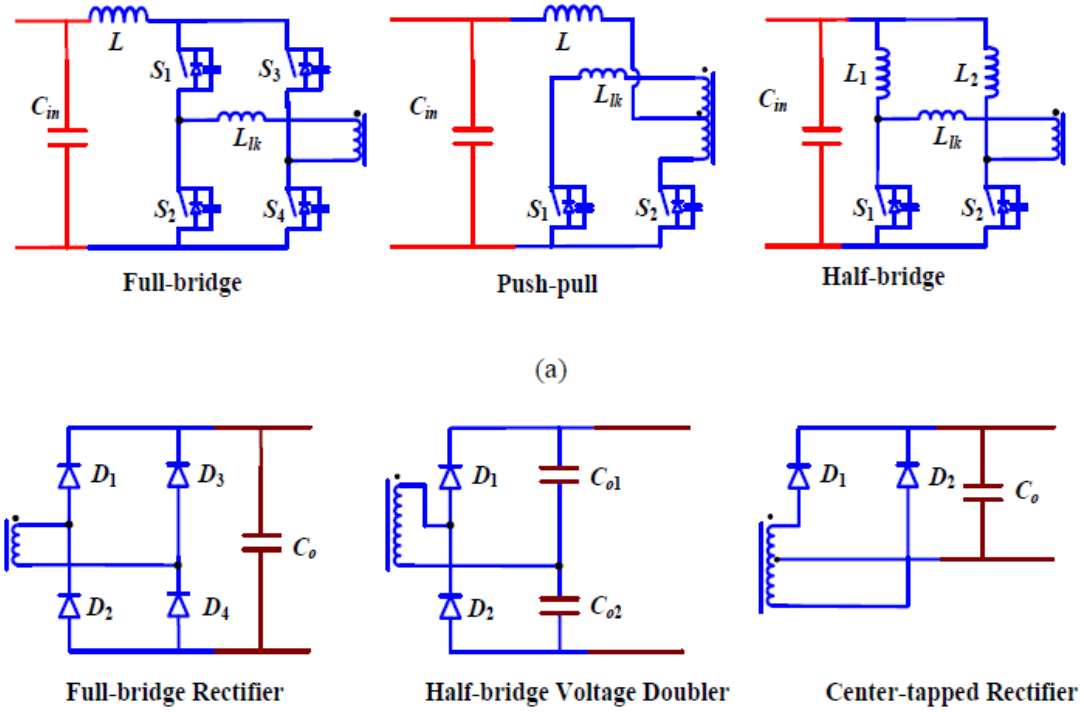


Fig. 1.8. Conventional current-fed PWM DC/DC converter topologies. (a) Three typical topologies for the low voltage inverter stage. (b) Three typical topologies for the high voltage side rectifier stage.

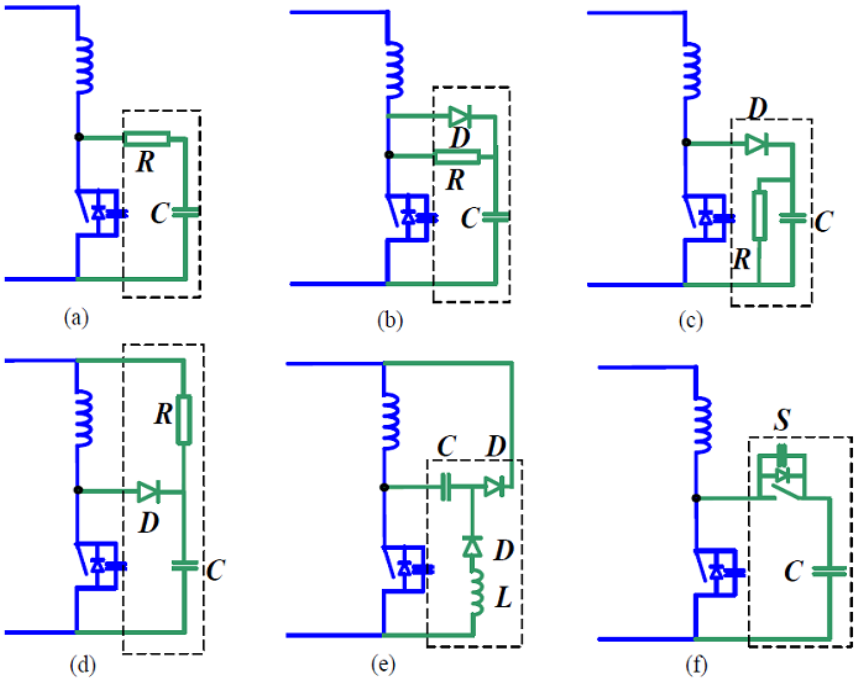


Fig.1.9. Snubbers for suppressing the voltage spike: (a) Dissipative RC snubber, (b)(c)(d) Dissipative RCD snubber,(e) Non-dissipative energy recovery LC snubber, and (f) active-clamping snubber.

Snubber circuit is required to suppress the device voltage spike and to prevent damage to the switches. There are different types of snubber circuits such as dissipative, regenerative, and active snubbers have been shown in Fig 1.9 [22]. These snubbers compromise on the boost capacity and modularity of the converter and add to the cost and volume of the converter. Hardware complexity is another disadvantage.

Dissipative snubbers lead to low efficiency owing to the energy dissipated in the snubber resistor. To improve the efficiency, energy recovery LC snubbers have been proposed as shown in Fig. 1.9(e) [23-26]. The LC snubber stores the surge energy in the capacitor during device turn-off. Once the switch is turned on, the capacitor is reset, and energy stored in the inductor is fed back to the input instead of being dissipated. However, the conventional LC snubber has complex structure, difficult optimal design, and do not assist in soft switching. The most popular snubber circuit is active-clamp circuit as shown in Fig. 1.9(f). In this circuit, HF transformer leakage inductance energy is dissipated into the capacitor and returned to the load. With a proper design, ZVS of primary switches can be achieved. Several examples of typical current-fed full-bridge topologies employing active-clamping techniques are displayed in Fig. 1.10 [25].

The active-clamp circuit archives ZVS at turn-on. The active-clamping snubber circuits need floating active device(s) and high value of HF clamp capacitor for accurate and effective clamping [24]. From the Fig 1.10 it is clear that the circuits are very complex and not modular as well as compromise on the boost capacity along with introducing hardware complexity. In addition, the auxiliary circuits still contribute to substantial amount of loss.

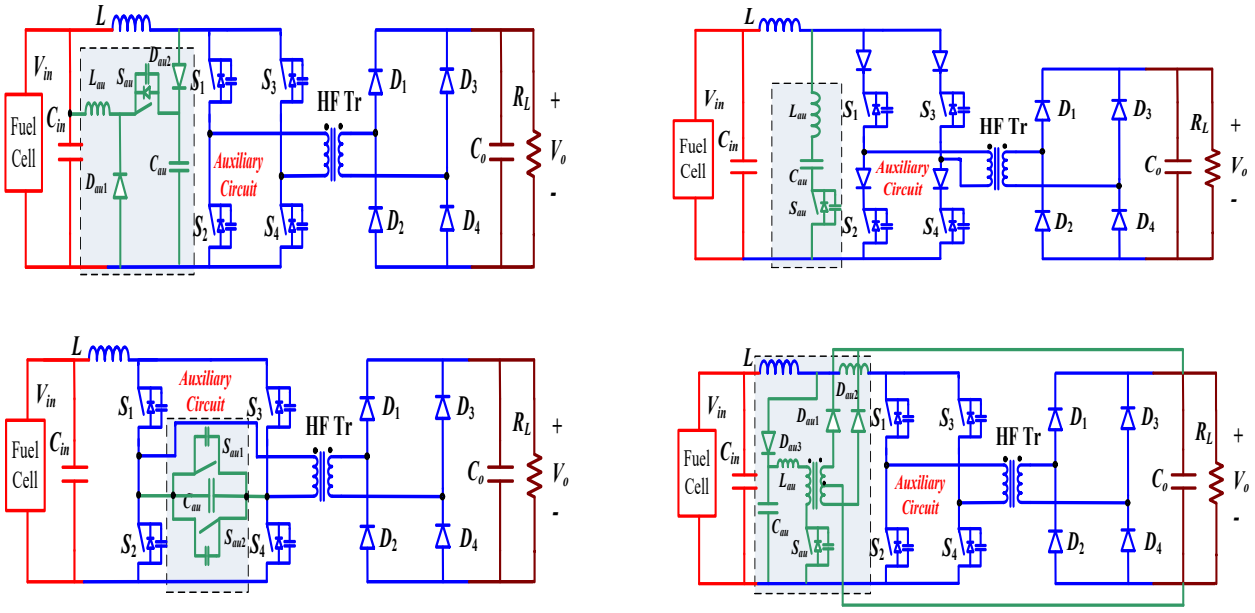


Fig. 1.10. Different types of converter with active-clamped snubber.

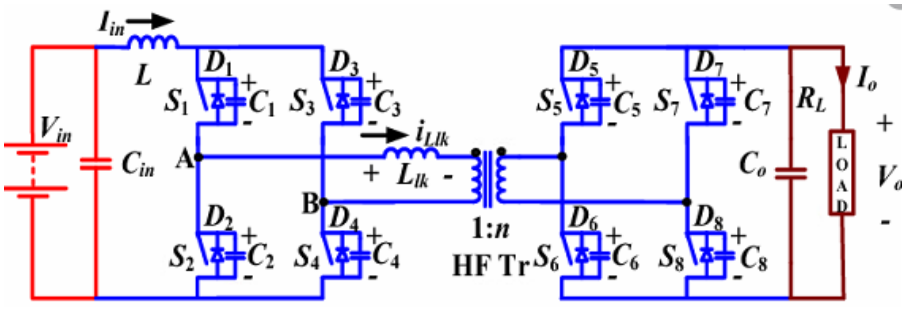
1.7.3 Resonant-type DC/DC Converter

Since 1980's, the resonant converters have arisen as a hot research topic and significant amount of research efforts were diverted to this area. The resonant concept, basically, is to incorporate resonant tanks (consisting of capacitor(s) and inductor(s)) to create oscillatory voltage and/or current waveforms so that ZVS or ZCS soft-switching of semiconductor devices can be achieved. For the conventional resonant converters, three most popular topologies including Series Resonant Converter (SRC) [27-28], Parallel Resonant Converter (PRC) [29-30], and Series Parallel Resonant Converter (SPRC) [31] have been intensively investigated. The main problems with these resonating techniques are high circulating energy for low voltage high current specifications, high turn-off current at high input voltage conditions [32]. Thus, conduction loss and switching

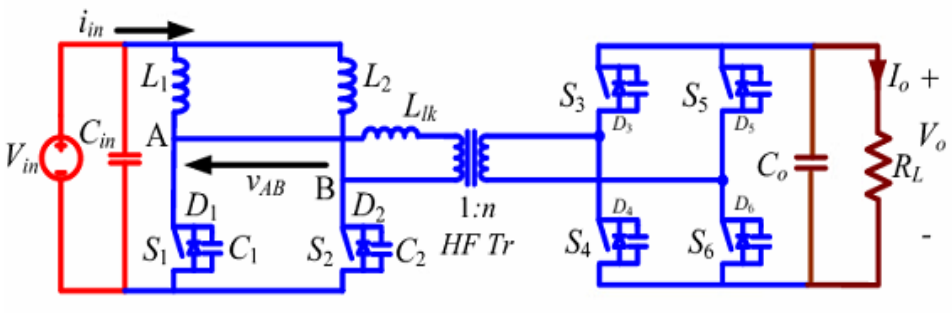
loss will increase at high input voltage condition making these techniques not suitable for wide voltage and power range application like fuel cells, solar, energy storage, etc.

1.7.4 Snubberless Naturally Clamped Current-fed DC-DC Converters

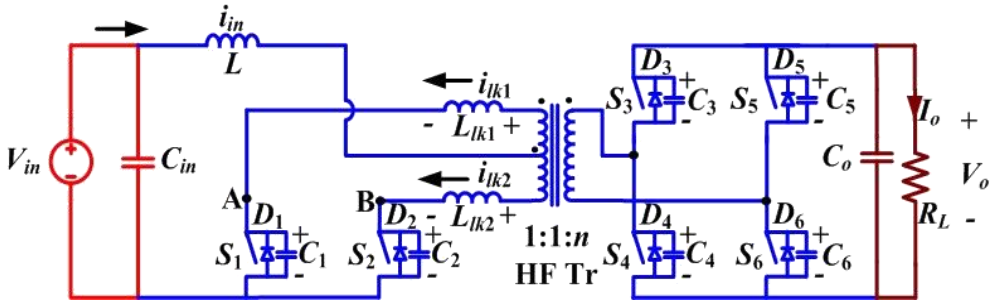
To avoid the historical complexity of snubber circuit, novel secondary-modulation-based naturally clamped soft-switching bidirectional current-fed dc/dc converters [33-35] as shown in Fig. 1.11.



(a) Full-bridge topology



(b) Half-bridge topology



(C) Push-pull topology

Fig. 1.11 Snubberless naturally clamped soft-switching current-fed dc/dc converter

Natural commutation or voltage clamping with zero-current switching (ZCS) of devices is achieved by fixed-frequency duty cycle modulation without any external snubber circuit, thus

reducing the hardware complexity as well preserving the originality/modularity of the circuit and the voltage gain capability. Switching losses are reduced significantly owing to soft switching of primary and secondary devices. It permits a high-switching-frequency operation making a compact and low-cost system [33]. Detailed steady-state analysis, design, and results have been reported for these snubberless naturally-clamped topologies with soft-switching [33-35].

1.8 Steady State and Small Signal Analysis

Steady state operation and analysis of a converter is needed to contunue its small signal analysis, and closed loop design. As fuel stack voltage varies with fuel flow based on the load requirement and that causes the variation of output voltage of DC-DC converter under different load condition. Therefore, DC-DC converter should be controlled to produce a constant voltage at all the fuel flow values, i.e. load voltage regulation. A control circuit, therefore, should be designed for the closed loop control of the converter so that by adjusting the duty cycle of the semiconductor devices, output voltage of the converter can be regulated at a specific constant value. Close loop control design requires the mathematical transfer function of the converter and that requires the small signal analysis of the converter for the given modulation technique.

The following systematic step-by-step procedure is adopted for the small signal analysis [36-37]:

1. Develop steady-state operating equivalent circuits of the converter during different intervals of operation for given modulation.
2. Define state variables
3. Write state space equation for each interval of operation.
4. Averaging of state equation over a switching cycle.
5. Introduce perturbation round the steady state (DC) operating point.
6. Isolate ac and dc quantities neglecting second order and higher order ac terms.
7. Introduce Laplace transformation to ac equations.
8. Develop transfer function or matrix

1.9 Research Objective

The objective of this thesis is to drive small signal model, design closed loop control system and experimentally demonstrate the transient performance of the snubberless current-fed dc-dc converter topologies. Detailed steady-state analysis and design of snubberless current-fed half-

bridge and push-pull topologies using a novel fixed-frequency duty cycle modulation technique have been reported in [34-35]. However, their small signal analysis, closed loop control, and transient results have not been reported yet. The outline of this thesis is mentioned in the next Section.

1.10 Thesis Outline

The set objectives of this thesis are achieved and organized in the various Chapters of the thesis.

Chapter 1 contributed to general understanding of fuel cells, its characteristic, and the requirement of secondary source (buffer) of energy. The introductory information on the high-frequency power conversion, various types of dc-dc converters and the need of the steady-state analysis and small-signal analysis have been reported. The research objectives of this thesis are highlighted.

In Chapter 2, snubberless current-fed half-bridge PWM dc-dc converter and its fixed-frequency duty cycle modulation are discussed. Systematic small signal modeling using state-space averaging and closed loop control system design using two-loop average current control of this converter are presented. The control-to-output function is derived. A complete design procedure for the controller design is presented. Bode plots obtained from the theoretical analysis and the simulations are presented to verify the design. The simulations results using PSIM 11.1.64 for step change in the load are illustrated to verify the controller performance and closed loop design. The controller was built in the laboratory using TI DSP for the 250 W proof-of-concept hardware prototype of the converter to demonstrate the experimental performance of the converter during transients with designed controller. Detailed steady-state analysis and design of this converter are presented in [34].

In Chapter 3, snubberless current-fed push-pull PWM dc-dc converter and its fixed-frequency duty cycle modulation are discussed. Detailed small signal modeling using state-space averaging and closed loop control system design using two-loop average current control for the transient performance evaluation of this converter are presented. Simulation results using PSIM 11.1.64 with the designed controller are shown to validate the system stability. The controller was built in the laboratory using TI DSP for the 250 W proof-of-concept hardware prototype of the converter to demonstrate the experimental performance of the converter during transients with designed controller. Experimental results demonstrated satisfactory transient performance at step change in

the load and validated the derived model and the controller design. Detailed steady-state analysis and design of this converter are presented in [35].

In Chapter 4, partial resonance impulse commutated current-fed half bridge and its variable frequency and duty cycle modulations are discussed. Detailed small signal modeling using state-space averaging and closed loop control system design using two-loop average current control for the transient performance evaluation of this converter are presented. Simulation results using PSIM 11.1.64 with the designed controller of variable frequency control and fixed frequency control of this converter are shown to validate the system stability.

In Chapter 5, main contributions and summary of the results of this thesis along with recommendations for the future work are reported.

Chapter 2

Small Signal Analysis and Control of Snubberless Naturally Clamped Soft-Switching Current-Fed Half-Bridge DC/DC Converter

2.1 Introduction

In this Chapter, small signal analysis of snubberless naturally-clamped soft-switching current-fed half-bridge (CFHB) isolated dc/dc converter, shown in Fig. 2.1, is presented and small signal model of the converter is derived. A fixed-frequency duty cycle modulation technique is proposed [34] to solve the traditional voltage spike across the semiconductor devices at their turn-off associated with current-fed converters. This modulation technique eliminates the device turn-off voltage overshoot without requiring any external active-clamping circuit or passive snubbers. Detailed steady-state analysis, converter design, and steady-state open loop experimental results for the CFHB dc-dc converter are presented [34]. Steady-state operating waveforms of the converter modulated with proposed modulation technique is shown in Fig. 2.2. However, to regulate the load (output) voltage and power flow control, closed loop control is compulsory. In practice, the power electronic products in market includes closed loop control system. For the design and development of closed loop control, small-signal model of the converter is required. Small signal modeling (SSM) is a widely adopted to analyze the performance of nonlinear systems such as PWM converters [37] and is important to design a closed-loop controller to obtain a good transient performance of the converter [38]. Small signal analysis, closed loop control design, and transient results of the CFHB converter are not yet reported. The objectives of this Chapter is to present systematic small signal analysis, derive the small signal model in matrix form, step-by-step closed loop controller design, and demonstrate the transient performance using simulation and experimental results. Small signal model of the converter has been derived using state space averaging in Section 2.2. Closed loop controller design employing two-loop average current control approach is given in Section 2.3. Simulation results using PSIM 11.1.64 are reported to verify the converter performance with the designed controller in Section 2.4. Experimental results

from a 250W converter proof-of-concept hardware prototype are demonstrated to show the transient performance of the converter for step changes in load.

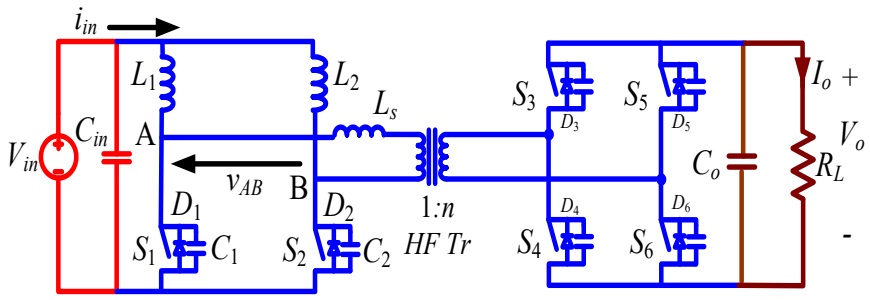


Fig. 2.1. ZCS naturally-clamped current-fed half-bridge isolated dc/dc converter [34].

2.2 Small Signal Analysis

In this Section, state-space equations for each interval of operation are written followed by the derivation of small signal ac model using state-space averaging. For the analysis, the following assumptions are made:

a) All the components are assumed ideal and lossless.
b) Input inductors $L_1$and L_2 are assumed large so that current through them can be considered constant.
c) Series inductor L_s includes the leakage inductance of the HF transformer's primary winding.
d) Magnetizing inductance is infinitely large.

Steady-state operating waveforms are shown in Fig. 2.2 [34]. The primary side devices S_1 and S_2 are operated with identical gating signals phase-shifted with each other by 180°. The duty cycle of primary switches is always kept above 50%.The operation during different intervals in a one half switching cycle is explained with equivalent circuits shown in Fig. 2.3 [34].
Here, n is secondary-to-primary transformer turns ratio, C_0 is output capacitance, R_L is load resistance, T_s is switching period.

State variables defined for the small signal modeling of the converter are: 1) Current through the transformer leakage inductor i_{ls}. 2) Input inductor currents $i_{L1,}$,i_{L2}. 3) Output voltage v_o. 4) Input voltage v_{in}.

Interval 1 (Fig. 2.2a; $t_0<t<t_1$): During this interval, primary side switch S_1 and anti-parallel body diodes D_4 and D_5 of secondary switches are conducting. Power is transferred to the load through HF transformer. Transformer leakage inductance is negative and constant. Switch S_1 is carrying the entire input current. State equations of this interval are:

$$L_1 \frac{di_{L1}}{dt} = v_{in} \tag{2.1}$$

$$L_2 \frac{di_{L2}}{dt} = (v_{in} - \frac{v_o}{n}) \tag{2.2}$$

$$C_o \frac{dv_o}{dt} = \frac{i_{Ls}}{n} - \frac{v_o}{R_L} \tag{2.3}$$

$$L_s \frac{di_{Ls}}{dt} = 0 \tag{2.4}$$

Interval 2 (Fig. 2.2b; $t_1<t<t_2$): Primary side switch S_2 starts conducting. The transformer leakage inductance starts transferring the current to switch S_2 with a slope limited by L_s. State equations of this interval are:

$$L_2 \frac{di_{L2}}{dt} = v_{in} \tag{2.5}$$

$$L_s \frac{di_{Ls}}{dt} = \frac{v_o}{n} \tag{2.6}$$

Interval 3 (Fig. 2.2c; $t_3<t<t_4$): Secondary side devices S_4 and S_5 are turned-on with ZVS. State equations of interval 2 still hold good.

Interval 4 (Fig. 2.2d; $t_4<t<t_5$): Primary side device S_1 turns-off with ZCS and its anti-parallel body diode starts conducting. State equations of interval 2 still hold good.

Interval 5 (Fig. 2.2e; $t_5<t<t_6$): Secondary side devices S_4 and S_5 are forced commutated and anti-parallel body diodes D_3 and D_6 of secondary switches takes over the current.

$$L_s \frac{di_{Ls}}{dt} = -\frac{V_o}{n} \tag{2.7}$$

Equations (2.1), (2.3) and (2.5) hold good for inductor currents i_{L1}, i_{L2}, and output capacitorc_o

Identically, state equations for the other half cycle can also be derived. State equations are averaged over a HF cycle. The average value for the rate of change of i_{Ls} over one complete HF cycle is zero and the averaged state equation is

$$L_s \left\langle \frac{di_{Ls}}{dt} \right\rangle = 0 \tag{2.8}$$

So, the state variable i_{Ls} is omitted for the following analysis. Define: $d_1T_s = t_2\text{-}t_1$, $d_2T_s = t_3\text{-}t_2$, $d_3T_s = t_4\text{-}t_3$, $d_4T_s = t_5\text{-}t_4$, $d_5T_s = t_6\text{-}t_5$, $d_6T_s = t_7\text{-}t_6$, $d_7T_s = t_8\text{-}t_7$, $d_8T_s = = t_9\text{-}t_8$, $d_9T_s = t_{10}\text{-}t_9$, $d_{10}T_s = t_1\text{-}t_{10}$.

The averaged state equations of defined state variables over a HF cycle are given:

$$L_1 \left\langle \frac{di_{L1}}{dt} \right\rangle = v_{in} - d_6 \frac{v_o}{n} \tag{2.9}$$

$$L_2 \left\langle \frac{di_{L2}}{dt} \right\rangle = v_{in} - d_1 \frac{v_o}{n} \tag{2.10}$$

$$C_o \left\langle \frac{dv_o}{dt} \right\rangle = i_{average} - \frac{v_o}{R_L} \tag{2.11}$$

where $i_{average}$ is the average current feeding the output capacitor and load from secondary side H-bridge switches and is given by,

$$i_{average} = \frac{i_{L2}}{n}(d_1) + \frac{i_{L1}}{n}(d_6) \tag{2.12}$$

Substituting (2.12) in (2.11),

$$C_o \left\langle \frac{dv_o}{dt} \right\rangle = \frac{i_{L2}}{n}(d_1) + \frac{i_{L1}}{n}(d_6) - \frac{v_o}{R_L} \tag{2.13}$$

The duty ratio of the main switches including conduction of the reverse anti-parallel diodes are defined as:

$$d=d_{S1} = d_1+d_2+d_3+d_4+d_5+d_7+d_8+d_9+d_{10} \tag{2.14}$$

$$d=d_{S2} = d_2+d_3+d_4+ d_5+d_6+d_7+d_8+d_9 +d_{10} \tag{2.15}$$

Introducing perturbation around the steady state values of the state variables and input voltage such that , $i_{L1} = I_L + \hat{\imath}_{L1}$,$i_{L2} = I_L + \hat{\imath}_{L2}$ $v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$,$d_{s1} = D + \hat{d}_{s1}$ and $d_{s2} = D + \hat{d}_{s2}$. And the state equations are modified to the following:

$$L_1 \frac{d(I_{L1}+\hat{\imath}_{L1})}{dt} = (V_{in} + \hat{v}_{in}) - \left(1 - D - \hat{d}_{s1}\right)\frac{(V_o+\hat{v}_o)}{n} \tag{2.16}$$

$$L_2 \frac{d(I_{L2}+\hat{\imath}_{L2})}{dt} = (V_{in} + \hat{v}_{in}) - \left(1 - D - \hat{d}_{s2}\right)\frac{(V_o+\hat{v}_o)}{n} \tag{2.17}$$

$$C_o \frac{d(V_o+\hat{v}_o)}{dt} = \left(\frac{I_{L1}+\hat{\imath}_{L1}}{n}\right)\left(1 - D - \hat{d}_{s1}\right) + \left(\frac{I_{L2}+\hat{\imath}_{L2}}{n}\right)\left(1 - D - \hat{d}_{s2}\right) - \left(\frac{V_o+\hat{v}_o}{R_L}\right) \tag{2.18}$$

Neglecting the second order terms and steady state or dc terms, results in the following equations.

$$L_1 \frac{d\hat{\imath}_{L1}}{dt} = \hat{v}_{in} - (1 - D)\frac{\hat{v}_0}{n} + \hat{d}_{s1}\frac{V_o}{n} \tag{2.19}$$

$$L_2 \frac{d\hat{\imath}_{L2}}{dt} = \hat{v}_{in} - (1 - D)\frac{\hat{v}_o}{n} + \hat{d}_{s2}\frac{V_o}{n} \tag{2.20}$$

$$C_o \frac{d\hat{v}_o}{dt} = (1 - D)\frac{\hat{\imath}_{L1}}{n} + (1 - D)\frac{\hat{\imath}_{L2}}{n} - \frac{I_{L1}}{n}\hat{d}_{s1} - \frac{I_{L2}}{n}\hat{d}_{s2} - \frac{\hat{v}_o}{R_L} \tag{2.21}$$

Taking Laplace transform, and then solving results in-

$$sL_1\hat{\imath}_{L1}(s) + \frac{(1-D)\hat{v}_o(s)}{n} = \frac{V_o}{n}\hat{d}_{s1}(s) + \hat{v}_{in}(s) \tag{2.22}$$

$$sL_2\hat{\imath}_{L2}(s) + \frac{(1-D)\hat{v}_o(s)}{n} = \frac{V_o}{n}\hat{d}_{s2}(s) + \hat{v}_{in}(s) \tag{2.23}$$

$$\frac{(1-D)}{n}\hat{\imath}_{L1}(s) + \frac{(1-D)}{n}\hat{\imath}_{L2}(s) - \left(sC_o + \frac{1}{R_L}\right)\hat{v}_o(s) = \frac{I_{L1}}{n}\hat{d}_{s1}(s) + \frac{I_{L2}}{n}\hat{d}_{s2}(s) \tag{2.24}$$

Writing in matrix form

$$\begin{bmatrix}\hat{\imath}_{L1}(s)\\ \hat{\imath}_{L2}(s)\\ \hat{v}_o(s)\end{bmatrix} = [A(s)].\begin{bmatrix}\frac{V_o}{n}\\ 0\\ \frac{I_{L1}}{n}\end{bmatrix}.\hat{d}_{s1}(s) + [A(s)].\begin{bmatrix}0\\ \frac{V_o}{n}\\ \frac{I_{L2}}{n}\end{bmatrix}\hat{d}_{s2}(s) + [A(s)].\begin{bmatrix}1\\ 1\\ 0\end{bmatrix}\hat{v}_{in}(s) \tag{2.25}$$

Where,

$$A(s) = \begin{matrix} sL_1 & 0 & \frac{(1-D)}{n} \\ 0 & sL_2 & \frac{(1-D)}{n} \\ \frac{(1-D)}{n} & \frac{(1-D)}{n} & -\left(sC_o + \frac{1}{R_L}\right) \end{matrix}^{-1} \tag{2.26}$$

$$sL\left(\hat{\imath}_{L1}(s) + \hat{\imath}_{L2}(s)\right) + \frac{2(1-D)\hat{v}_o(s)}{n} = \frac{V_o}{n}\left(\hat{d}_{s1}(s) + \hat{d}_{s2}(s)\right) + 2\,\hat{v}_{in}(s) \tag{2.27}$$

Writing in matrix form

$$\begin{bmatrix} \hat{\imath}_{L1}(s) + \hat{\imath}_{L2}(s) \\ \hat{v}_o(s) \end{bmatrix} = [A(s)].\begin{bmatrix} \frac{v_o}{n} \\ \frac{I_L}{n} \end{bmatrix}.\left(\hat{d}_{s1}(s) + \hat{d}_{s2}(s)\right) + [A(s)].\begin{bmatrix} 2 \\ 0 \end{bmatrix}\hat{v}_{in}(s) \tag{2.28}$$

Where,

$$A(s) = \begin{bmatrix} sL & \frac{2(1-D)}{n} \\ \frac{(1-D)}{n} & -\left(sC_o + \frac{1}{R_L}\right) \end{bmatrix}^{-1} \tag{2.29}$$

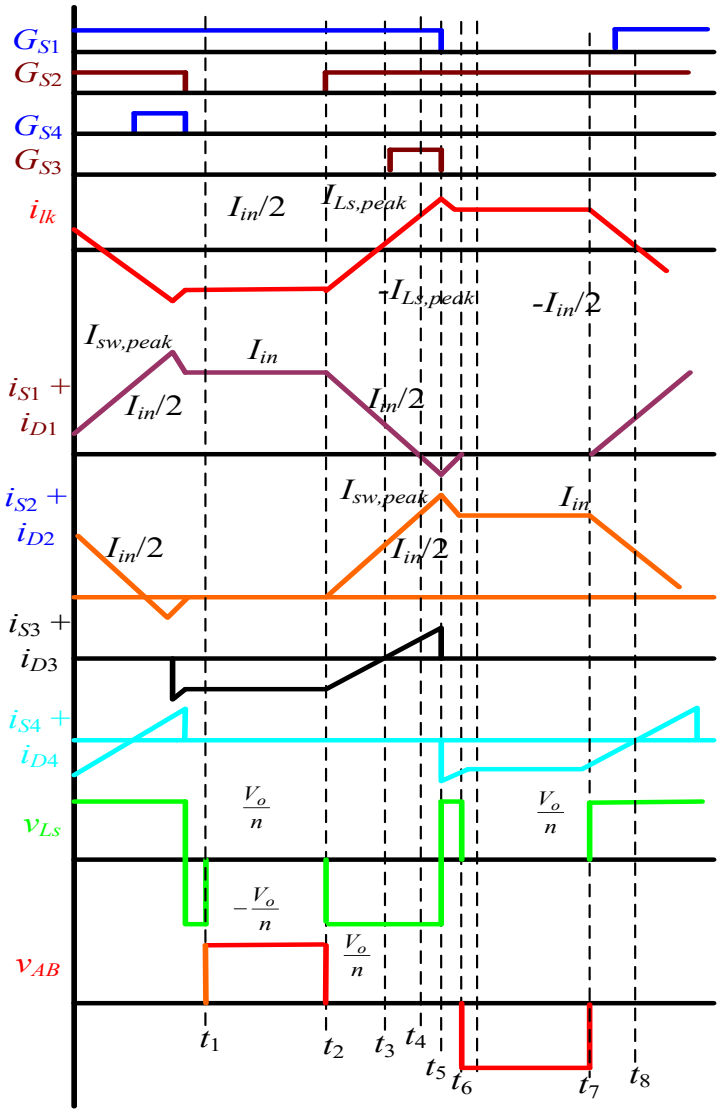
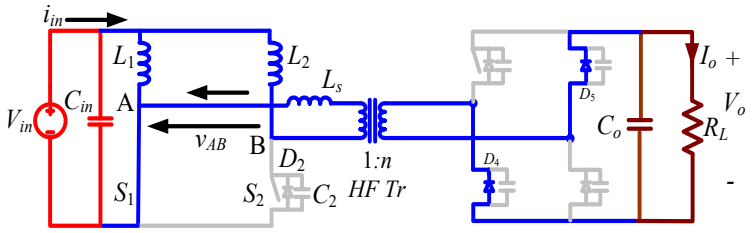


Fig. 2.2. Operating waveforms of ZCS current-fed converter [34]

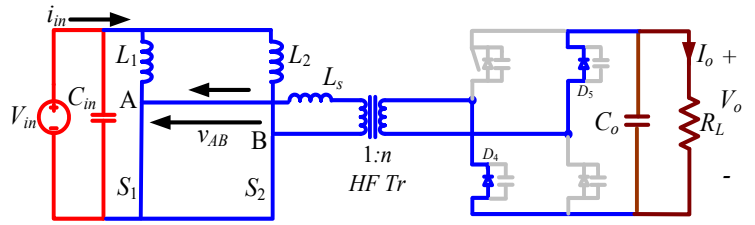
Control-to-output Transfer Function

From equation (2.28), the control-to-output transfer function is obtained by setting $\hat{v}_{in} = 0$. It results in the following equation

$$\frac{\hat{v}_o(s)}{\hat{d}_{s1}(s)+\hat{d}_{s2}(s)} = \frac{\frac{(1-D)V_O}{n^2} - s\frac{L.I_L}{n}}{(LC_o)s^2+\frac{L}{R_L}s+\frac{2(1-D)^2}{n^2}} \tag{2.30}$$



(a)



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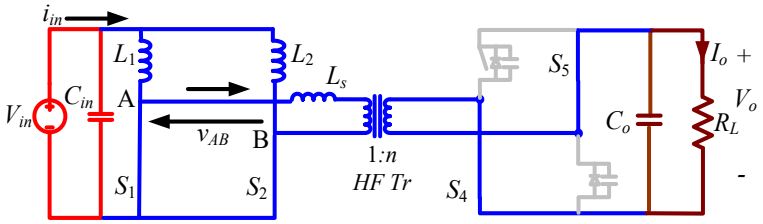

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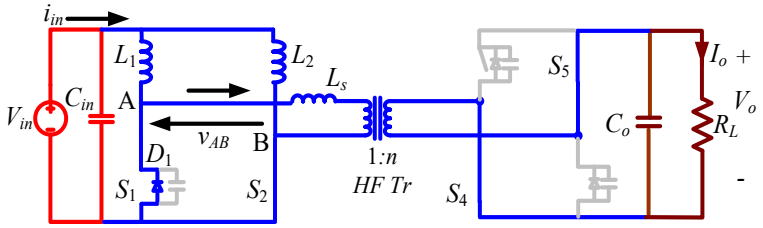

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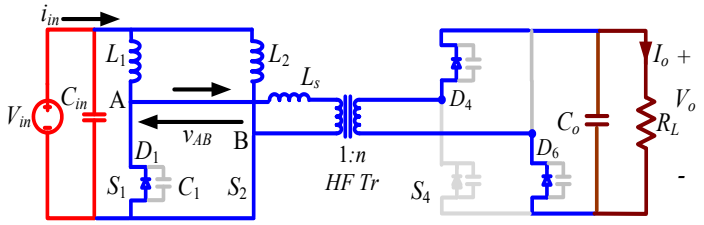

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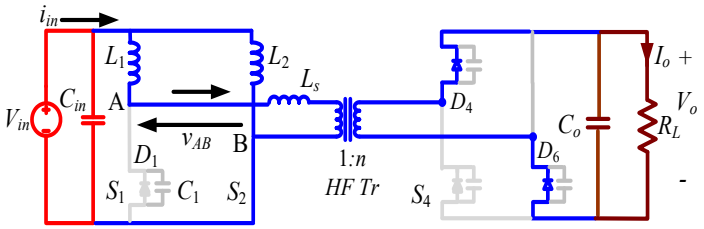


(f)

Fig. 2.3. Equivalent circuits during different intervals of the operation [34].

2.3 Designing of Two-Loop Average Current Control

In this Section, two-loop average current control design procedure is illustrated systematically. The specifications of the converter: input voltage V_{in} = 12 V, output voltage V_o = 288V, output power P_o = 250W, switching frequency f_s = 100 kHz, leakage inductor or series inductor L_s = 4.1µH, boost inductor L=$L_1 = L_2 = 200$µH, transformer turns ratio n = 8.4, output capacitor C_o = 270 µF, full-load resistance R_L = 332 Ω.

Fig. 2.4 shows the complete two-loop feedback control system using 2 PI controllers and 2 modulators having the same values of frequency and amplitude but phase shifted by 180°. Active current ripple is the major issue for designing of fuel cell converter. The key to ripple reduction is to control the average inductor current i_L to be dc, which requires that bandwidths of voltage and current loops are separated far apart with a slow voltage loop and a fast current loop [39] .Two-loop control consists of outer voltage control loop and inner current control loop. These two loops are designed separately. Outer voltage loop bandwidth (BW) is set much lower than the inner current loop, which simplifies the design [40-41].Therefore the inner current loop with higher BW has faster dynamics than outer voltage loop. The inductor current is able to change more quickly than the output voltage. Voltage control loop regulates the output voltage by generating reference

for the input inductor current, $i_{L1,ref}$ and $i_{L2,ref}$ reference. Inductor currents i_{L1} and i_{L2} are tuned to this reference value by adjusting the duty ratio of the switches.

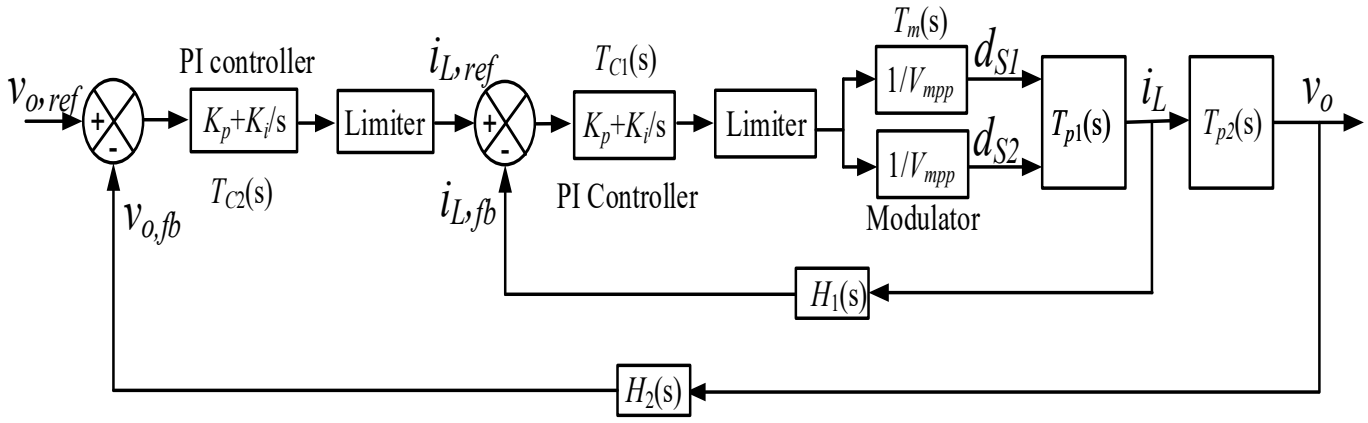


Fig. 2.4. Complete two-loop average current control system schematic diagram.

Bode plot of the control-to-output voltage transfer function given by (2.30) in Fig. 2.5. The phase margin is negative. This makes the system sensitive to small disturbances in input or source voltage and load current. From Fig. 2.6, it is clearly visible that this transfer faction has right half plane zero, which adds negative phase to the system. Instead phase increasing from 0 to 90 degrees, its phase increases from 0 to -
90 degrees. This causes delay in system response which can lead to instability if not taken care.

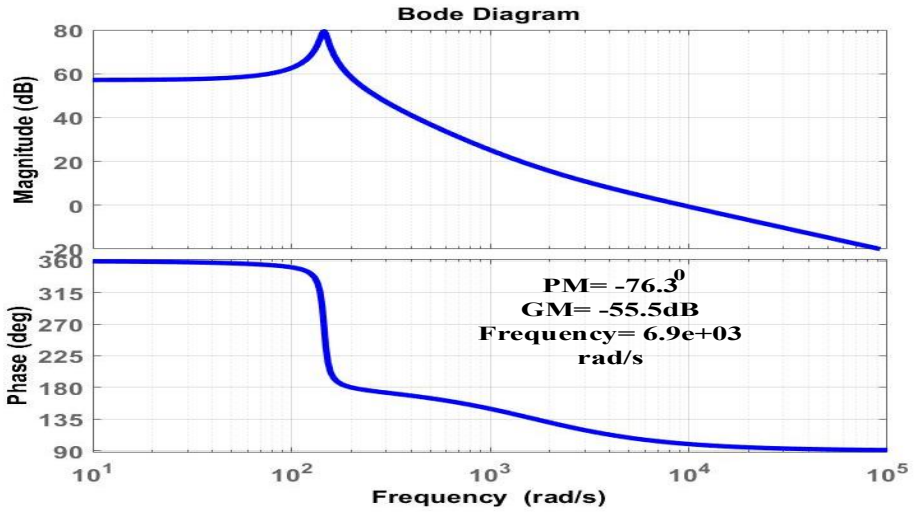


Fig. 2.5. Control to output voltage transfer function of the system without controller

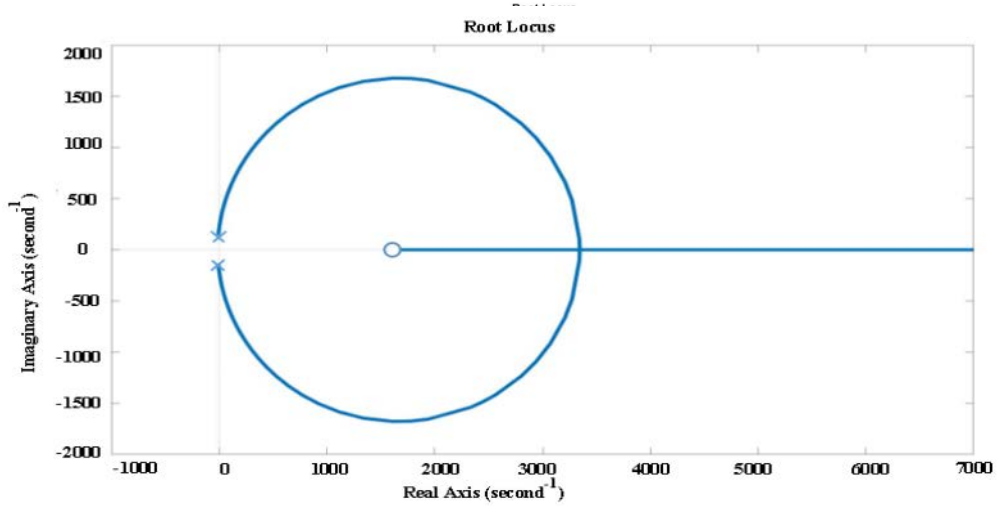


Fig. 2.6. Pole-zero map of Control to output voltage transfer function of the system without controller

2.3.1 Designing of Current Control Loop:

The schematic diagram of the inner current control loop is shown in Fig. 2.7. Input inductor current is fed back to the error amplifier with the gain of $H_1(s)$. Output of the PI controller is sent to the modulator to generate the gating signals. Then inductor current i_{L1} is regulated by adjusting the duty ratio of the switches.

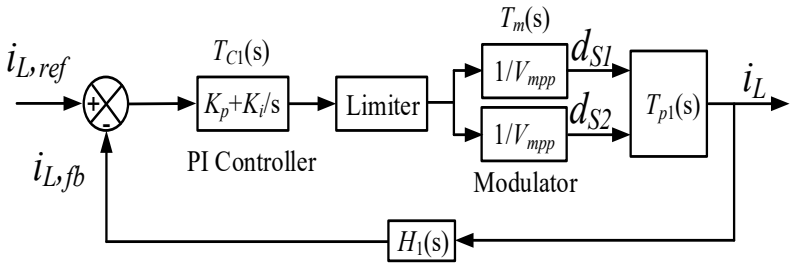


Fig. 2.7. Inner current control loop schematic diagram.

Duty ratio to the inductor current transfer function is,

$$\frac{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)}{\hat{d}_{s1}(s)+\hat{d}_{s2}(s)} = \frac{\left(\frac{C_O V_O}{n}\right)s+\frac{V_O}{nR_L}+\frac{2(1-D)I_L}{n \quad n}}{(LC_O)s^2+\frac{L}{R_L}s+\frac{2(1-D)^2}{n^2}} \tag{2.31}$$

For the given specifications, duty ratio to inductor current transfer function is given by,

$$T_{p1}(s) = \frac{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s}{\hat{d}_{s1}(s)+\hat{d}_{s2}(s)} = \frac{0.004542s+0.331514}{4.26*10^{-8}s^2+5.847*10^{-7}s+3.472*10^{-3}} \quad (2.32)$$

The gain margin and phase margin of current control loop without controller is plotted Fig 2.8, which shows of PM= 90^0 at 177 krad/s. A PI controller is designed to increase the low frequency gain, to reduce the steady-state error between the desired and actual inductor current and to achieve stability over a certain range.

Transfer function of a PI controller is given by,

$$T_{C1}(s) = K_p + \frac{K_i}{s} = \frac{K_p(s + K_i / K_p)}{s} \quad (2.33)$$

Open loop transfer function of the current loop is given by,

$$T_{OL1}(s) = T_{C1}(s) \cdot T_m(s) \cdot T_{p1}(s) \cdot H_1(s) \quad (2.34)$$

LEM sensor LA25-NP is used to sense the inductor current and to provide the isolation between power circuit and controller. Here current feedback gain is chosen as $H_1(s)$ =1. The voltage signal at the output of the current controller (limited to the range of 0 to 3.3V) is converted from analog to digital and used to control duty ratio of PWM blocks. They work together serving as the modulator. The duty ratio of the primary switches is restricted to the range or 0.55 to 0.8. Considering the gain of ADC (the modulator phase lag introduced by conversion delay of ADC has been neglected) and subsequent digital process, overall gain of the modulator is given as,

$$T_m(s) = \frac{1}{10} \quad (2.35)$$

For the given specifications, open loop transfer function of the current loop is given by,

$$\angle T_{OL1}(jw_c) = PM - 180^o \quad (2.36)$$

$$T_{OLI}(jw_c) = \frac{106572K_p\left(jw_c+\frac{K_i}{K_p}\right)(jw_c+73.02)}{jw_c({jw_c}^2+13.72jw_c+81502.34jw_c)} \quad (2.37)$$

$${k_p}^2\left(1.5625 * 10^{10} + {\frac{k_i}{k_p}}^2\right) = 4.875 * 10^{11} \quad (2.38)$$

PI controller parameters are designed to obtain PM of 60º [42] at the gain crossover frequency of 31.5 krad/s (5 kHz). It results in the gain K_p and integrator time constant K_i as 0.16 and 7269.58

respectively. Fig. 2.9 shows the Bode plot of the compensated transfer function showing improved low frequency gain and the expected PM at desired crossover frequency.

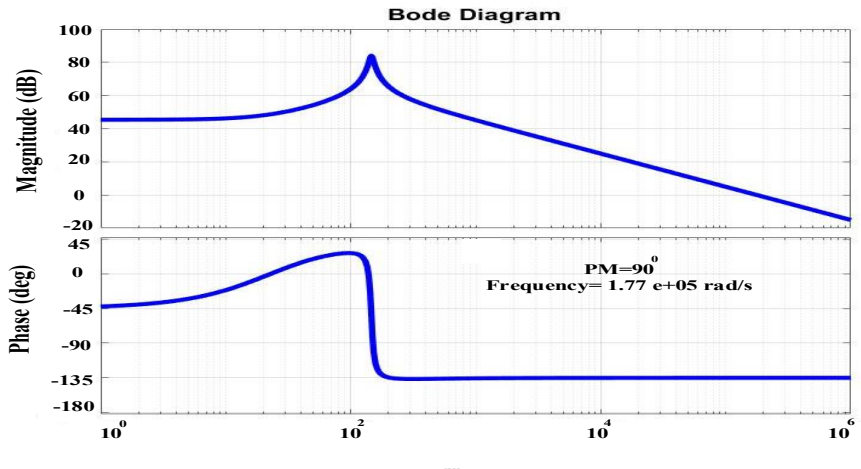


Fig. 2.8. Bode plot of uncompensated control to input current transfer function: PM = 90^0at 177 krad/s

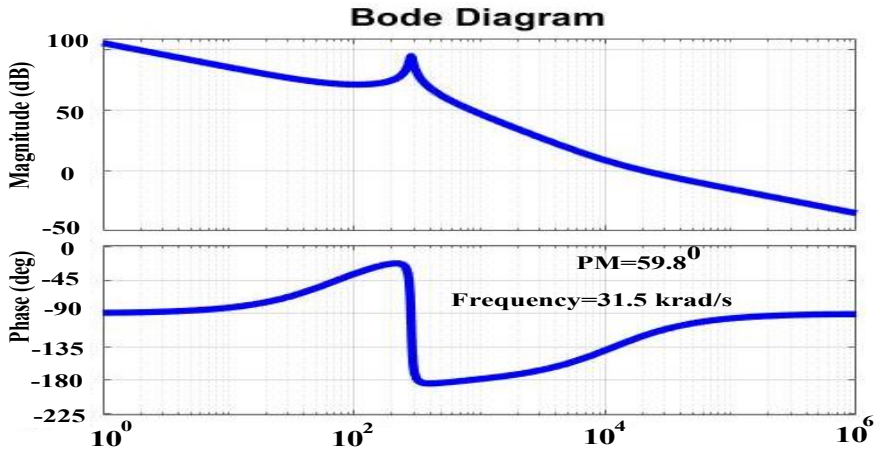


Fig. 2.9. Bode plot of compensated control to input current transfer function: PM = 59.8^0at 31.5 krad/s(5000 Hz)

2.3.2 Designing of Voltage Control Loop:

Outer voltage control loop regulates the output voltage at the reference value by setting reference for the current through the input inductors as shown in Fig. 2.10. Inner current control loop has faster dynamics compared to outer voltage loop. Hence, the current loop dynamics are neglected during the design of voltage controller [43]. Its transfer function is not included and the

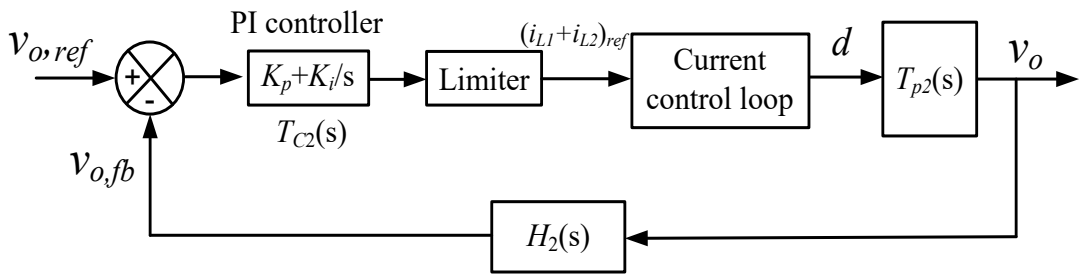


Fig. 2.10. Outer voltage control loop schematic diagram.

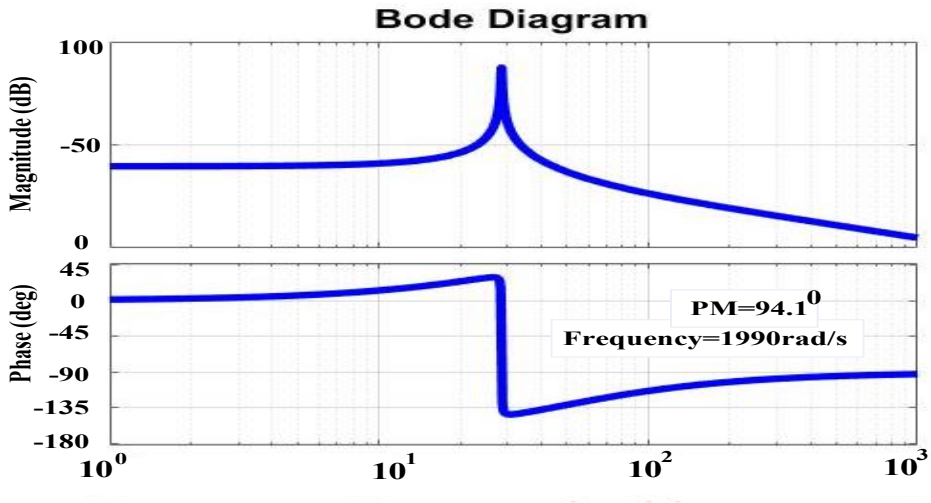


Fig. 2.11. Bode plot of uncompensated plant in voltage control loop: PM = 94.1^0 at 1990 rad/s

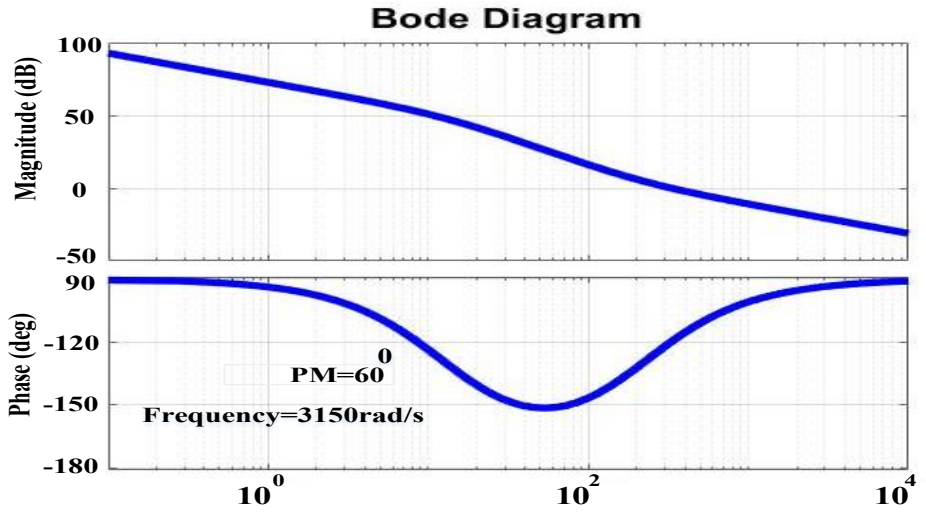


Fig. 2.12. Bode plot of compensated system in voltage control loop: PM = 60^0 at 3150 rad/s(500 Hz)

perturbation in duty cycle can be neglected. Therefore, inductor current to output voltage transfer function T_{p2}(s) is obtained as (2.39)

$$T_{p2}(s) = \frac{v_o(s)}{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)} = \frac{(1-D)}{nC_o(s+\frac{1}{R_L C_o})} \tag{2.39}$$

$$T_{P2}(s) = \frac{0.35}{.001848s+0.025} \tag{2.40}$$

LEM sensor LV20-P is used to sense output voltage and also to provide the necessary isolation. Here voltage feedback gain is chosen as,

$$H_2(s) = 24 \tag{2.41}$$

PI controller transfer function T_{C2}(s) is given by (2.33). Overall open loop transfer function of the voltage loop is given by,

$$T_{OL2}(s) = T_{C2}(s) \cdot T_{p2}(s) \cdot H_2(s) \tag{2.42}$$

$$T_{OL2}(s) = \frac{0.35K_p\left(s+\frac{K_i}{K_p}\right)}{.001848s^2+0.025s} \tag{2.43}$$

Gain crossover frequency for voltage controller is selected 10 times slower than that of inner current loop. Hence the phase margin should be 60º at the gain crossover frequency of 3150 rad/s It results in the gain K_p and integrator time constant K_i as 16.83 and 9767.84, respectively. Taking into account dynamics of current control loop,

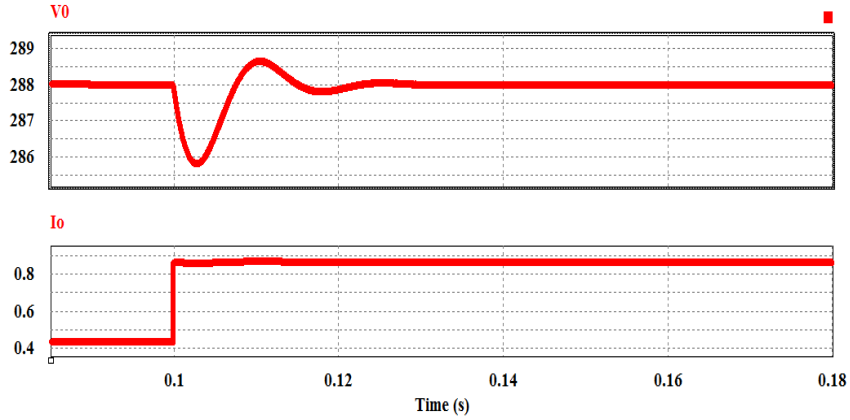
Overall transfer function of the system can be written as given in

$$T_{OL}(s) = \left[\frac{T_{C1}(s)\cdot T_{p1}(s)\cdot T_m(s)\cdot H_1(s)}{1+T_{C1}(s)\cdot T_{p1}(s)\cdot T_m(s)\cdot H_1(s)}\right]\cdot T_{C2}(s)\cdot T_{p2}(s)\cdot H_2(s)\cdot\frac{1}{H_1(s)} \tag{2.44}$$

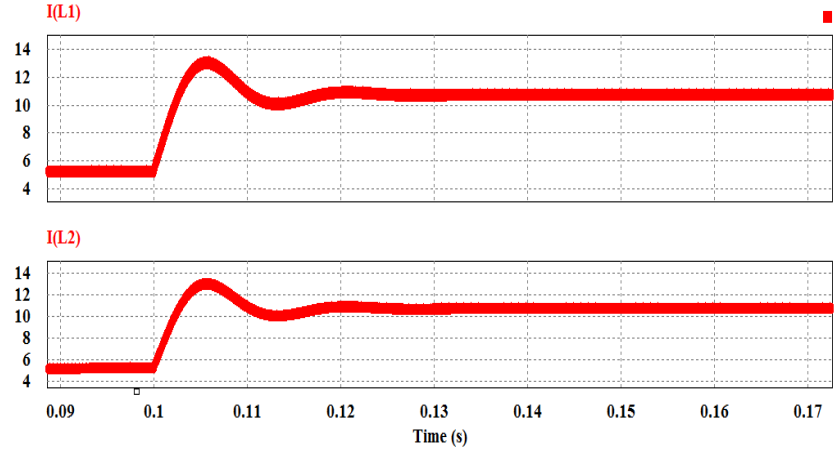
Gain at lower frequency is high indicating zero steady state error. Positive PM has been achieved resulting in a stable system with better control against disturbances for wide range in source voltage and load current variations.

2.4 Simulation and Experimental Results

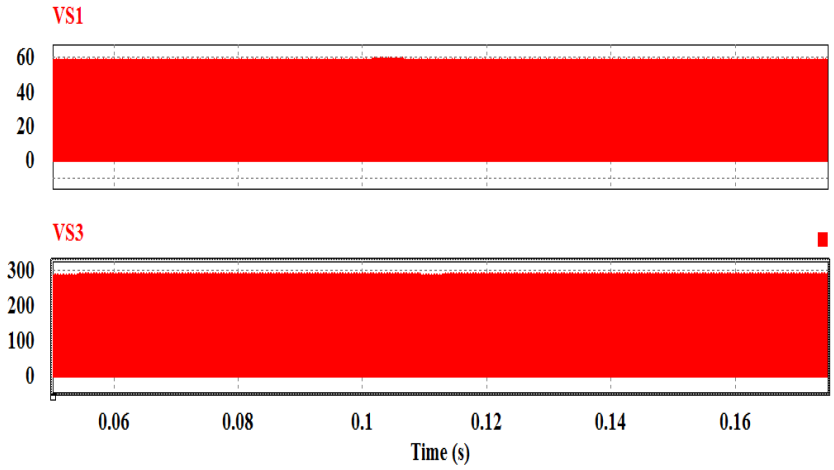
Simulation model of circuit topology and two-loop control was developed on software package PSIM 11.1.64 and was run to capture waveforms and observe transient performance of the converter under load current variations. Simulation results are illustrated in Fig. 2.13 and Fig. 2.14 for step change in the load from half-load to rated load and rated-load to half-load, respectively. It should be observed that the overshoot or undershoot in output voltage is around 3V (1%) for both the sudden jump in the load and then regulated to the desired value. Load current, two input inductors' current, and the voltage across the switches are adjusting smoothly and reaching to the next steady-state without overshoot. The settling time of booth input boost inductor current and output voltage is around 20 ms.



(a)

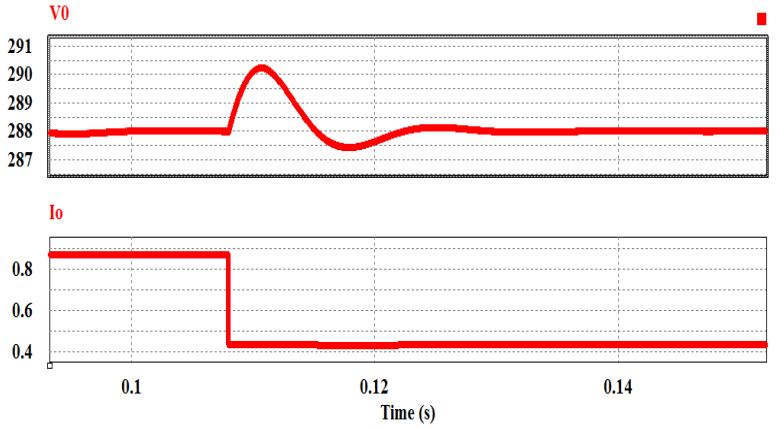


(b)

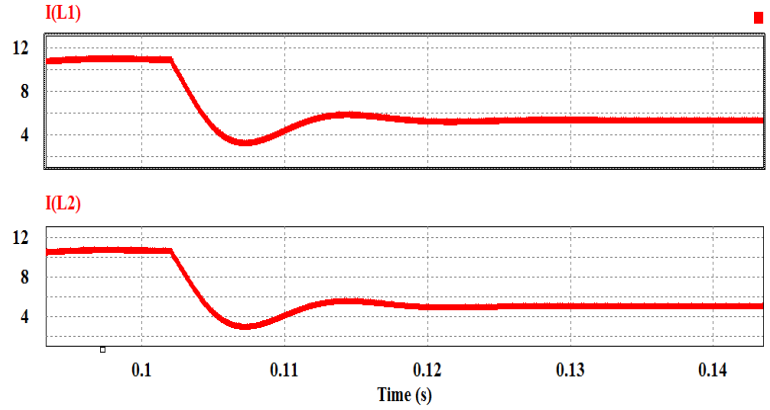


(c)

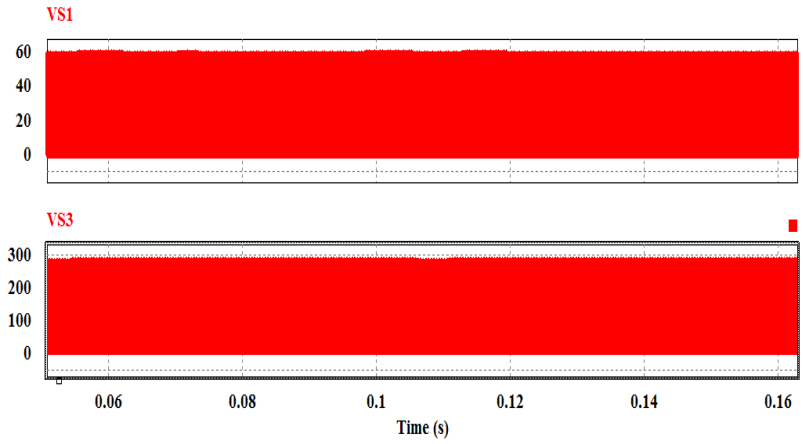
Fig. 2.13. Simulation waveforms for V_{in}=12V with step change in load from 50% load to rated full-load; V_0 is output voltage,I_0 is output current, I_{L1} and $I_{L2}$are input inductor currents, $V_{s1}$and $V_{s3}$are voltage across the switches S_1 and S_3, respectively.



(a)



(b)



(c)

Fig. 2.14. Simulation waveforms for V_{in}=12V with step change in load from rated load to half-load with identical nomenclature.

Table I: Components' Parameters of the Hardware Prototype:

Components	Parameters
Primary switches (S_1, S_2)	IRFB4127PbF 200V, 76A, $R_{ds,on}$ =17mΩ
Secondary switches (S_3, S_4)	IPP60R125CP 650V, 11A, $R_{ds,on}$ =0.125Ω
Series Inductor	TDK5901PC40Z core, 3.9 µH
HF transformer	3C95ETD49 ferrite core; N_1=5, N_2=45
Boost Inductors	3C95ETD49 ferrite core, $N = 42$, $L = 200$µH
Output CapacitorC_O	220µF, 450 V electrolytic capacitor 0.68 µF, 450V high frequency film capacitor

Fig. 2.15 shows the experimental hardware laboratory prototype of the CFHB dc-dc converter. The hardware prototype details are given in Table I. Gating signals for the devices are generated using DSP TMS320F28335. The designed controller has been tested in the laboratory for step changes in load from half-load to full load and vice-versa for fixed input voltage of 12 V. Fig. 2.16 shows the variations of inductor current i_L, transformer primary voltage V_{AB}, output voltage V_o, with respect to time for step change from half-load to full-load. Similar waveforms for the step change from full-load to half-load are recorded as shown in Fig. 2.17. Output voltage is regulated at constant value of 288 V with negligible overshoot and undershoot. The variation in

inductor current i_L and the transformer primary voltage V_{AB} are also within range from one steady-state to another during transient. Therefore, the switches do not experience any voltage spike during this transition, which ensure normal and safe operation of the converter. It demonstrates stability of performance over load variation. An undershoot (Fig. 2.16) and overshoot (Fig. 2.17) in output voltage up to 12 V is observed during sudden change in load. The settling time is nearly 20 ms. Fig. 2.18 and Fig. 2.19 show zoomed steady state switch currents, gate-to-source voltage of primary and secondary devices, secondary drain-to-source voltage and V_{AB} under and half-load and full-load, respectively.

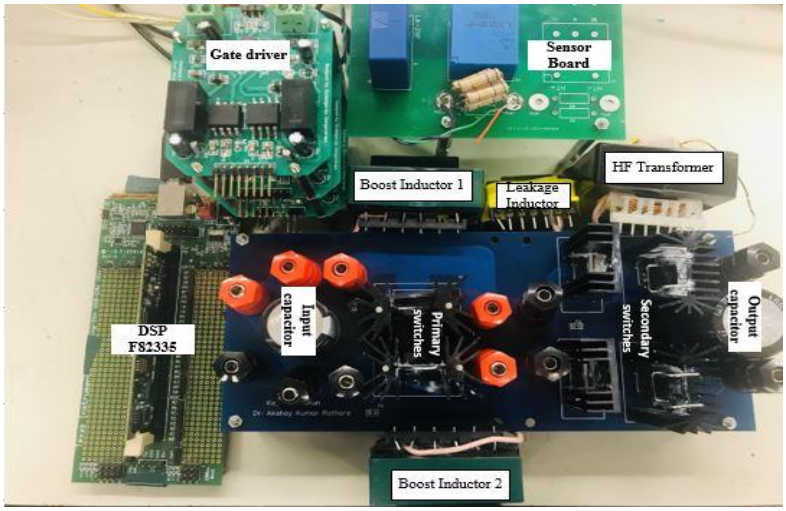


Fig. 2.15 Laboratory prototype of snubberless current-fed half-bridge dc-dc converter

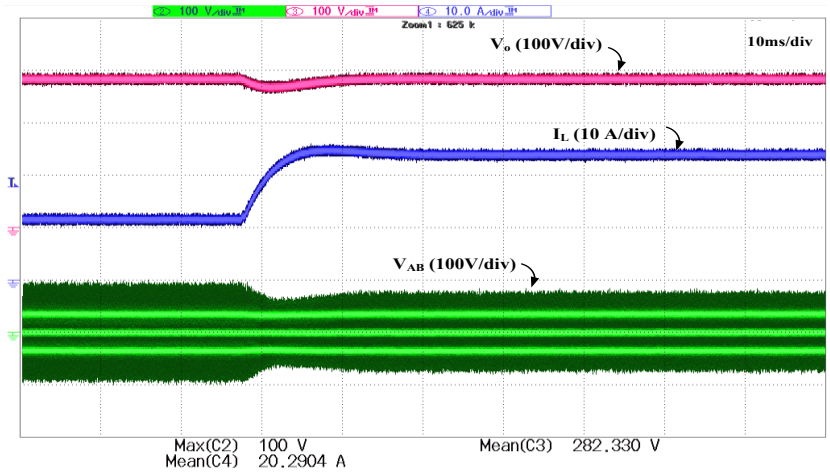


Fig. 2.16 Hardware result for step change in load from half-load to full-load :(1) voltage V_{AB} (100 V/div), (2) inductor current i_L (10 A/div) and (3) output voltage V_O (100 V/div)

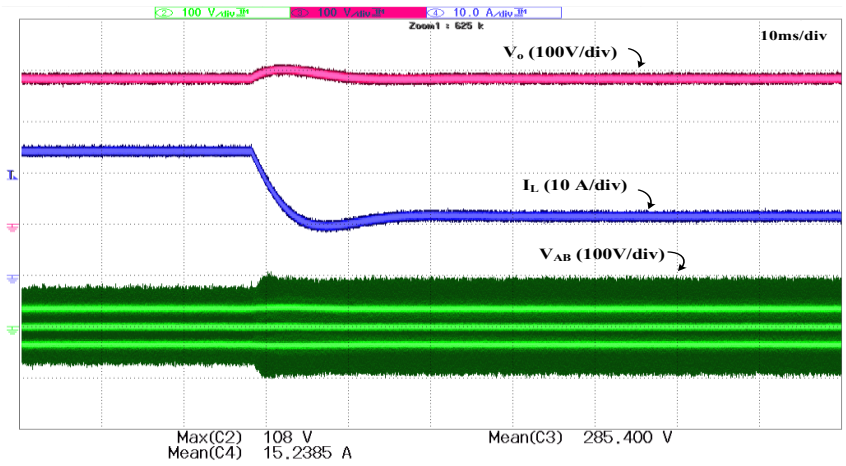
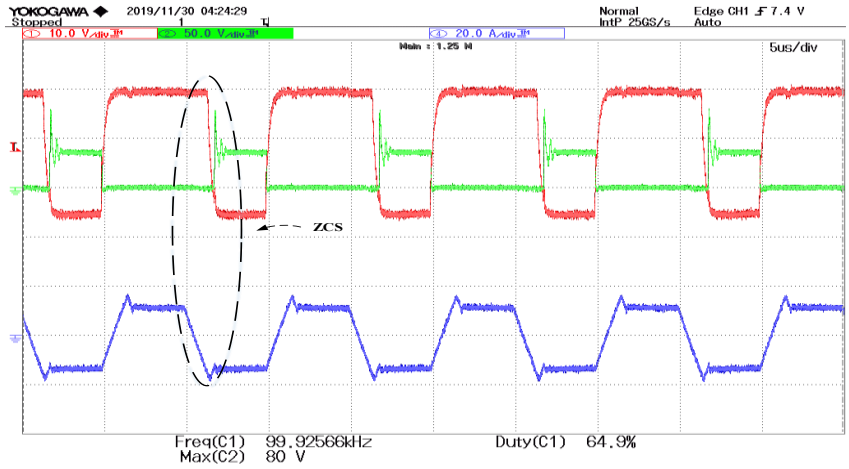
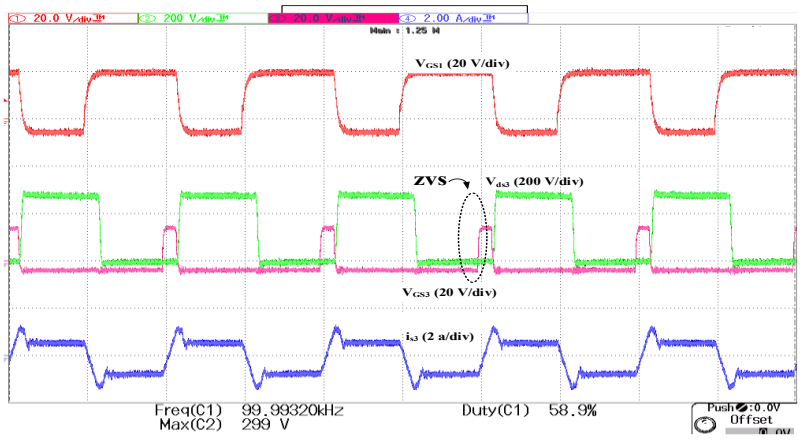


Fig 2.17.Hardware results for step change in load from full-load to half-load :(1) voltage V_{AB} (100 V/div), (2) inductor current i_L (10 A/div) and (3) output voltage V_O (100 V/div)

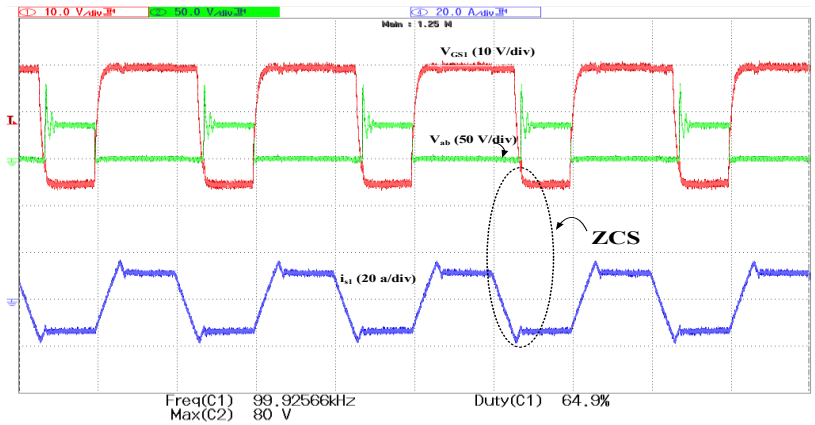


2.18(a)

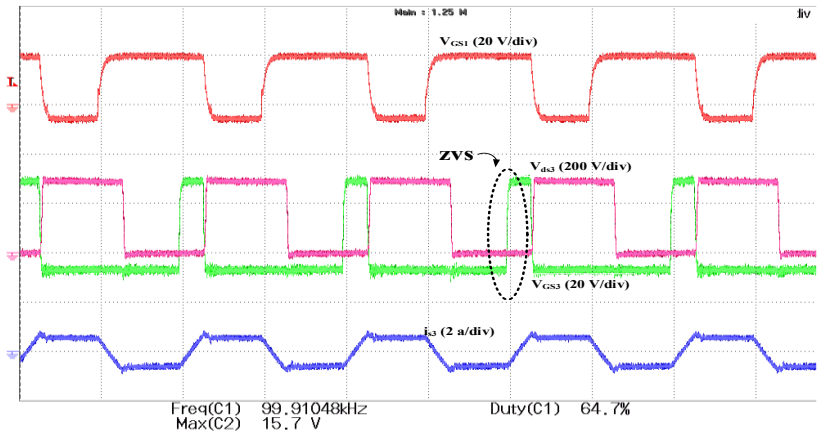


2.18(b)

Fig.2.18. Experimental results for v_{in}=12V at half-load (a) Gate-to-source voltage V_{GS1} (20 V/div), current through transformer i_p(20 A/div), and voltage V_{AB}=50V/div (b) Gate- to-source voltage V_{GS3}(20 V/div),drain-to-source voltage V_{ds3}(200 V/div), transformer secondary current i_{s1}(2 A/div).



2.19(a)



2.19(b)

Fig.2.19. Experimental results for v_{in}=12V at full-load (a) Gate-to-source voltage V_{GS1} (20 V/div), transformer primary current i_p (20 A/div), and voltage V_{AB}=50V/div (b) Gate- to-source voltage V_{GS3}(20 V/div),drain-to-source voltage V_{ds3}(200 V/div), transformer secondary current i_{s1}(2 A/div).

Figs. 2.18(a) and 2.19(a) show the gate-to-source V_{GS}, and transformer primary current i_s waveforms across primary-side MOSFET under half-load and full-load condition respectively. It clearly demonstrates that the current through the switch naturally goes to zero followed by antiparallel body diode conduction before turning-off the gating signals, ensuring ZCS turn-off at primary side.

Corresponding, the gate-to-source V_{GS} and drain-to-source voltages V_{ds} of secondary waveforms are shown in Fig 2.18(b) and Fig. 2.19(b) for half-load and full-load, respectively. The gate-to-source voltage (V_{GS}) is applied when the voltage across secondary device is already zero that ensures ZVS operation in secondary devices. Therefore, it verifies the soft-switching of the primary and secondary side devices.

It should be noticed that settling time is higher than the simulation results due to the circuit experiences power loss, voltage drop, stray inductance/capacitance, system delay and parasitic in real experiment which cause the aberration from the ideal model. Better dynamic performance may be achieved by proper tuning of the controller parameters.

2.5 Conclusion

In this chapter, detailed small signal analysis to obtain the small signal model of the snubberless naturally-clamped soft-switching current-fed half-bridge dc-dc converter is reported. State variables are defined and state space averaging technique is followed to systematically derive the small signal model of the converter. Placing the values of power circuit components' from the steady-state design, the small signal model is presented in numerical form. Two-loop average current control approach is followed to design a closed loop control system using 2 PI controllers to meet the frequency response requirements and obtain stability during load disturbances and transients. A detailed and systematic procedure to design the inner current control loop and outer voltage loop is illustrated. Simulation results, obtained through PSIM 11.1.64 are presented to verify the controller design and investigate the initial transient performance of the converter. Experimental results on a proof-of-concept hardware laboratory prototype are shown to demonstrate the satisfactory transient performance of the converter and effectiveness of the implemented controller

Chapter 3

Small Signal Analysis and Control of Snubberless Naturally-Clamped Soft-Switching Current-Fed Push-Pull DC/DC Converter

3.1 Introduction

In this Chapter, small signal analysis and a closed loop control design of snubberless naturally-clamped soft-switching current-fed push-pull (CFPP) isolated dc/dc converter, shown in Fig 3.1, is presented. Mathematical small signal model of the converter operated with a given modulation technique is derived. A fixed-frequency duty cycle modulation technique is proposed [35] to solve the traditional voltage spike across the semiconductor devices at their turn-off associated with current-fed converters. This modulation technique eliminates the device turn-off voltage overshoot without requiring any external active-clamping circuit or passive snubbers. Detailed steady-state analysis, converter design, and steady-state open loop experimental results for the push-pull dc-dc converter is presented [35].This topology has one input inductor and two devices with common ground with the supply reducing the gate driver requirement. Source side devices achieve zero current switching (ZCS) and load side devices achieve zero voltage switching (ZVS). It clamps the voltage across the devices naturally and attains soft-switching of all the devices for the wide operating range. The voltage across primary-side devices is independent of the duty cycle with varying input voltage and output power clamped at reflected output voltage, enabling the use of low voltage semiconductor devices. Steady-state operating waveforms of the converter modulated with proposed modulation technique is shown in Fig. 3.2. However, to regulate the load (output) voltage and power flow, closed loop control is compulsory. In practice, the power electronic products in the market include closed loop control system. For the design of the closed loop control, small-signal model of the converter is required. Small signal modeling (SSM) is a widely adopted to analyze the performance of nonlinear systems such as PWM converters [37] and is important to design a closed-loop controller to obtain a good transient performance of the converter [38]. Detailed steady-state analysis and design of this converter have

been presented [35]. Steady-state analysis is useful for the power circuit design and evaluate the steady-state performance of the converter. Small signal analysis, closed loop control design, and transient results of the CFPP converter are not yet reported.

The objective of this Chapter is to simulate and experimentally demonstrate the transient performance of the converter. Systematic small signal model of the converter has been derived using state space averaging in Section 3.2. Step-by-step closed loop controller design employing two-loop average current control approach is presented in Section 3.3. Simulation results using PSIM 11.1.64 are illustrated to verify the controller design and converter performance in Section 3.4. Experimental results from a 250W converter proof-of-concept hardware prototype are demonstrated to show the transient performance of the converter for step changes in load. The dynamic performance of the converter is tested for load changes by designed the close loop controller.

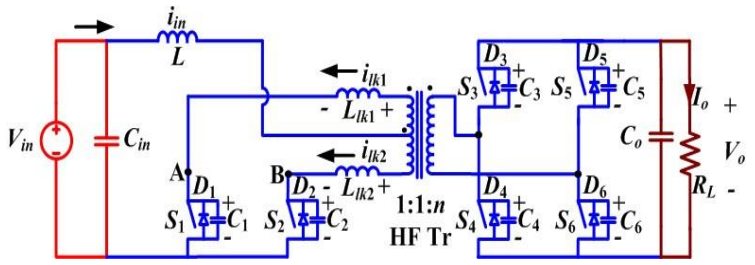


Fig. 3.1. Snubber-less naturally-clamped current-fed push-pull dc/dc converter [35].

3.2 Small Signal Modeling Using State-space Averaging

In this section, the state-space equations for each interval of operation are given. Based on state space averaging technique the small signal AC model of the converter has been presented systematically. The following assumptions are made for the analysis:

a) All the components are ideal and lossless.
b) Input inductor L is large enough to maintain constant current.
c) Series inductors L_{lk1} and L_{lk2} include the leakage inductance of the two transformer's primary winding.
d) Magnetizing inductance is infinitely large.

e) The snubber capacitors' charging and discharging time are very small as compared to HF cycle and neglected.

The primary side devices S_1 and S_2 are operated with identical gating signals phase-shifted by 180^0. The duty cycle of primary side switches is always kept above 50%. The operation in a half switching cycle is explained with equivalent circuits shown in Fig. 3.3. Here, n is secondary-to-primary transformer turns ratio, C_0 is output capacitance, R_L is load resistance, T_s is switching period, and I_{in} is input current.

State variables defined for the small signal analysis are: 1) Leakage inductors current i_{lk1} and i_{lk2}, 2) current through input inductor i_l, 3) Output voltage v_o and control variables for regulation are 1) Input voltage v_{in} 2) duty ratio d.

Interval 1 (Fig. 3.3a; $t_0<t<t_1$): In this interval, primary side switch S_2 and antiparallel body diodes D_3 and D_6 of the secondary-side H-bridge switches are conducting. Switch S_2 carries entire input current. State equations of this interval are:

$$i_{lk2} = i_{in} \tag{3.1}$$

$$(L + L_{lk1})\frac{di_{in}}{dt} = \left(v_{in} - \frac{v_o}{n}\right) \tag{3.2}$$

$$L_1 \frac{di_{lk1}}{dt} = 0 \tag{3.3}$$

$$C_o \frac{dv_o}{dt} = \frac{i_{in}}{n} - \frac{v_o}{R_L} \tag{3.4}$$

Interval 2 (Fig. 3.3b; $t_1<t<t_2$): Switch S_1 is turned on and all Primary side switches conduct simultaneously during this interval. The current through L_{lk2} and hence through S_2 decreases similarly, current through S_1 increases linearly. Here, $L_{lkT} = L_{lk1} + L_{lk2}$. State equations of this interval are:

$$L_{lk_T} \frac{di_{lk1}}{dt} = \frac{2v_0}{n} \tag{3.5}$$

$$L_{lk_T} \frac{di_{lk2}}{dt} = -\frac{2v_0}{n} \tag{3.6}$$

$$L\frac{di_L}{dt} = v_{in} + \frac{v_o}{n}\left[1 - \frac{2L_{lk1}}{L_{lk_T}}\right] \tag{3.7}$$

$$C_o \frac{dv_o}{dt} = \frac{i_{lk2} - i_{lk1}}{n} - \frac{v_o}{R_L} \tag{3.8}$$

Interval 3 (Fig. 3.3d; $t_3<t<t_4$): In this interval, secondary H-bridge devices S_3 and S_6 are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 2. At the end of this interval, the primary device S_2 commutates naturally with zero current commutation and the respective current I_{S2} reaches zero obtaining ZCS. The full current, i.e., input current is taken over by other device S_1. Final values are: $I_{lk1} = I_{S1} = I_L$, $I_{lk2}=I_{S2}=0$, $I_{S3} = I_{S6} = I_L/n$. State equations of interval 2 still hold good.

Interval 4 (Fig. 3.3d; $t_4<t<t_5$): In this interval, the leakage inductance current i_{Lk1} increases further with the same slope and antiparallel body diode D_2 of switch S_2 starts conducting causing extended zero voltage to appear across commutated switch S_2 to ensure ZCS turn-off. Now, the secondary devices S_3 and S_6 are turned off. State equations of interval 4 are:

$$L_{lk\_T}\frac{di_{lk1}}{dt} = -\frac{2v_0}{n} \tag{3.9}$$

$$L_{lk_T}\frac{di_{lk2}}{dt} = \frac{2v_0}{n} \tag{3.10}$$

$$C_o\frac{dv_o}{dt} = \frac{i_{lk2}-i_{lk1}}{n} - \frac{v_o}{R_L} \tag{3.11}$$

Interval 5 (Fig. 3.3e; $t_5<t<t_6$): During this interval, secondary switches $S_3$and $S_6$are turned-off. Antiparallel body diodes of switches S_4 and S_5take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch and S_1 body diodes D_2 also start decreasing. Equation (3.7) hold good for inductor currentI_L.

Identically, state equations for the other half cycle can also be derived. State equations are averaged over a HF cycle. Assuming $L_{lk1}=L_{lk2}=L_{lk}$, The average value for the rate of change of i_{LIK} over one complete HF cycle is zero, and the averaged state equation is:

$$L_{lk}\left\langle\frac{di_{LIk}}{dt}\right\rangle = 0 \tag{3.12}$$

Average current components of L_{lk} are nullified out over a HF switching cycle, state variables I_{lk1} and I_{lk2} can be neglected in the small signal relation between V_{in}, d and V_o. Define: $d_1T_s = t_2-t_1$, $d_2T_s = t_3-t_2$, $d_3T_s = t_4-t_3$, $d_4T_s = t_5-t_4$, $d_5T_s = t_6-t_5$, $d_6T_s = t_7-t_6$, $d_7T_s = t_8-t_7$, $d_8T_s = = t_9-t_8$, $d_9T_s = t_{10}-t_9$, $d_{10}T_s = t_1-t_{10}$

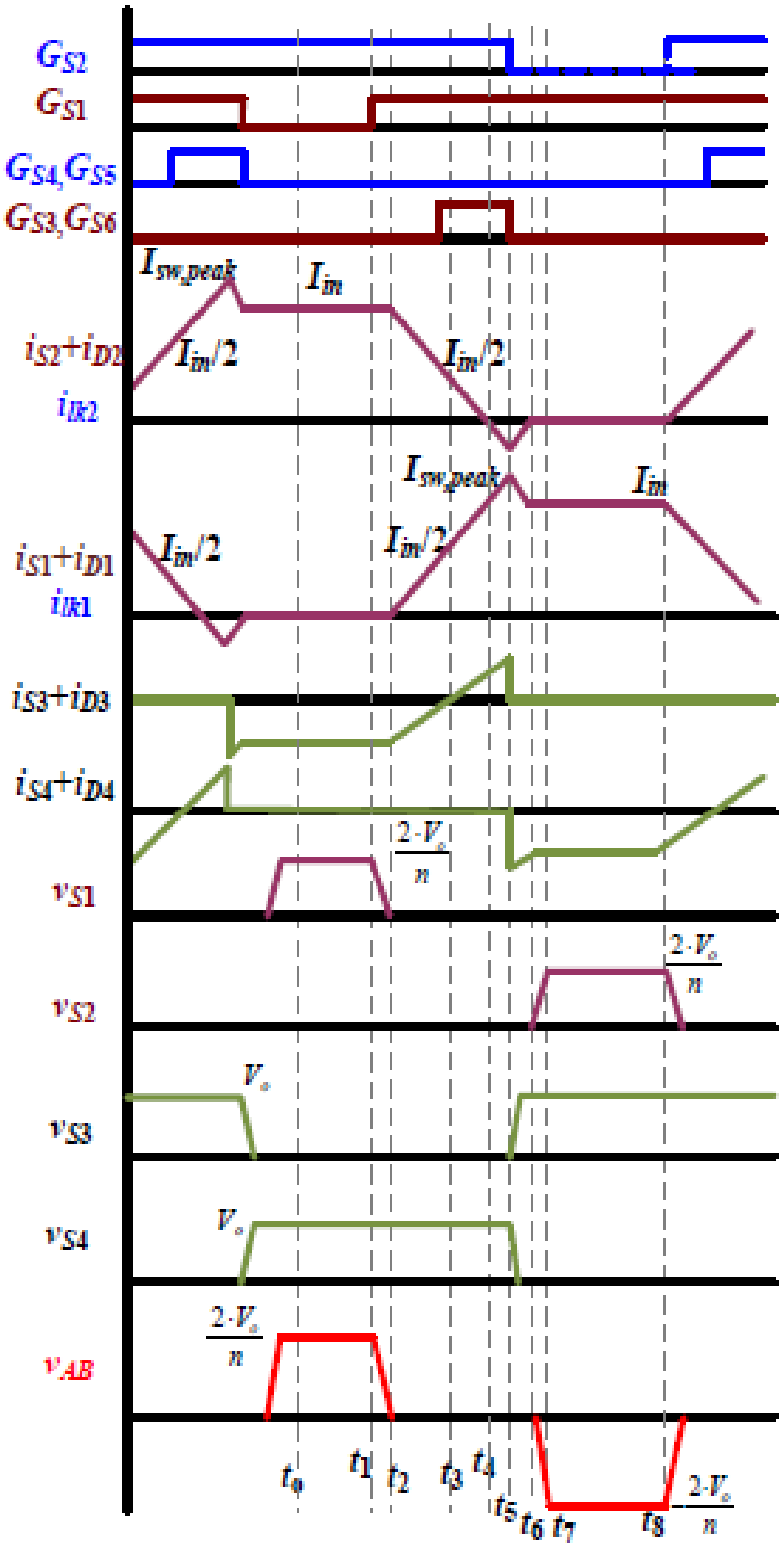
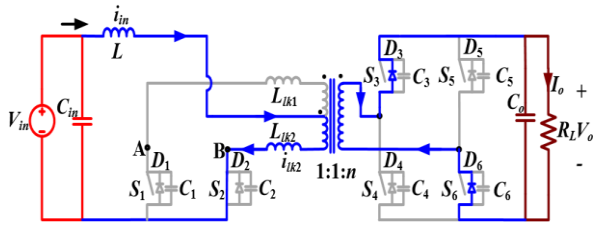
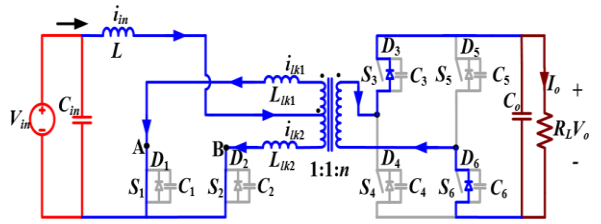


Fig. 3.2 steady-state operating waveform of converter [35].



(a)



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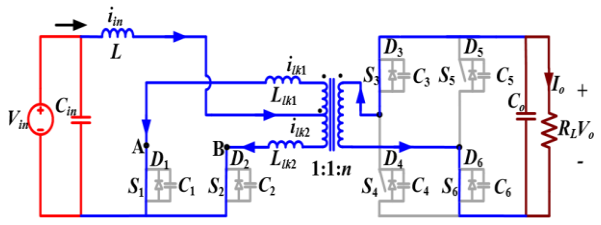
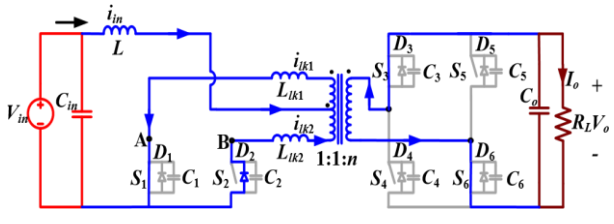
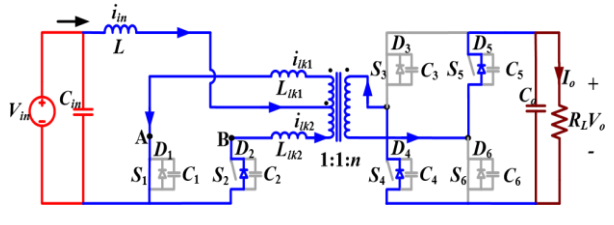


(c)



(d)



(e)

Fig. 3.3. Equivalent circuits during various intervals.[35]

The averaged state equations of defined state variables over a HF cycle are given:

$$(L + L_{lk})\left\langle \frac{di_L}{dt} \right\rangle = v_{in} - (d_1 + d_8)\frac{v_o}{n} \tag{3.13}$$

$$C_o\left\langle \frac{dv_o}{dt} \right\rangle = i_{average} - \frac{v_o}{R_L} \tag{3.14}$$

Where, $i_{average}$ is the average current feeding the output capacitor and load from secondary side H-bridge switches and is given by:

$$i_{average} = \frac{i_{L2}}{n}(d_1) + \frac{i_{L1}}{n}(d_6) \tag{3.15}$$

Substituting equations (3.15) in (3.14),

$$C_o \langle \frac{dv_o}{dt} \rangle = \frac{i_{L2}}{n}(d_1) + \frac{i_{L1}}{n}(d_6) - \frac{v_o}{R_L} \tag{3.16}$$

The duty ratio of the main switches including conduction of the reverse anti-parallel diodes are defined as:

$$d = d_{S1} = d_3 + d_4 + d_5 + d_6 + d_8 + d_{10} + d_{11} + d_{12} \tag{3.17}$$

$$d = d_{S2} = d_1 + d_3 + d_4 + d_5 + d_{10} + d_{11} + d_{12} + d_{13} \tag{3.18}$$

Introducing perturbation around the steady state values of the state variables and input voltage such that, $i_{L1} = I_L + \hat{\imath}_{L1}$,$i_{L2} = I_L + \hat{\imath}_{L2}$, $v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$,$d_{s1} = D + \hat{d}_{s1}$ and $d_{s2} = D + \hat{d}_{s2}$. And the state equations are modified to the following:

$$(L + L_{lk})\frac{d(I_L + \hat{\imath}_L)}{dt} = V_{in} + \hat{v}_{in} - \frac{2}{n}(V_o + \hat{v}_o)(1 - D - \hat{d}) \tag{3.19}$$

$$C_o \frac{d(V_o + \hat{v}_o)}{dt} = \frac{2}{n}(I_{in} + \hat{\imath}_{in})\left(1 - D - \hat{d}\right) - \frac{(V + o\hat{v}_o)}{R} \tag{3.20}$$

Neglecting the second order terms and steady state or dc terms, results in the following equations.

$$(L + L_{ik})\frac{d\hat{\imath}_L}{dt} = \hat{v}_{in} + \frac{2}{n}V_o\hat{d} - \frac{2}{n}(1 - D)\hat{v}o \tag{3.21}$$

$$C_o \frac{d\hat{v}_o}{dt} = -\left(\frac{2}{n}\mathrm{I}_{in}\right)\hat{d} + \frac{2}{n}(1 - D)\hat{\imath}_{in} - \frac{\hat{v}_o}{R} \tag{3.22}$$

Taking Laplace transform, and then solving results in-

$$S(L + L_{ik})\hat{\imath}_{in}(s) = 2\frac{V_o}{n}\hat{d}(s) - \hat{v}_{in}(s) - \frac{2(1-D)\hat{v}_o(s)}{n} \tag{3.23}$$

$$SC_o\hat{v}_o(s) = \frac{-2I_{in}}{n}\hat{d}_s + \frac{2(1-D)}{n}\hat{\imath}_{in} - \frac{1}{R}\hat{v}_o(s) \tag{3.24}$$

Writing in matrix form

$$\begin{bmatrix}\hat{\imath}_L(s)\\ \hat{v}_o(s)\end{bmatrix} = [A(s)].\begin{bmatrix}\frac{2v_o}{n}\\ \frac{2I_{in}}{n}\end{bmatrix}.\hat{d}(s) + [A(s)].\begin{bmatrix}1\\0\end{bmatrix}\hat{v}_{in}(s) \tag{3.25}$$

Where,

$$A(s) = \begin{bmatrix} sL & \frac{2(1-D)}{n} \\ \frac{2(1-D)}{n} & -\left(sC_o + \frac{1}{R}\right)\end{bmatrix}^{-1} \tag{3.26}$$

Control-to-output Transfer Function

From (3.25), the control-to-output transfer function is obtained by setting $\hat{v}_{in} = 0$. It results in the following equation

$$\frac{\hat{v}_o(s)}{\hat{d}_s(s)} = \frac{\frac{4(1-D)V_O}{n^2} - s\frac{L.I_L}{n}}{(LC_O)s^2 + \frac{L}{R_L}s + \frac{4(1-D)^2}{n^2}} \tag{3.27}$$

3.3 Closed loop controller design

Table 1: Specifications to design the control system of following converter:

Input voltageV_{in}	12V
Output VoltageV_o	300V
Peak output powerP_o	250W
Switching frequency of converterf_s	100kHz
Leakage inductors L_{ls}	4.09µH,
Input Boost Inductor L	22.5µH,
Output CapacitorC_O	220µF
Full-loadR_L	360Ω.

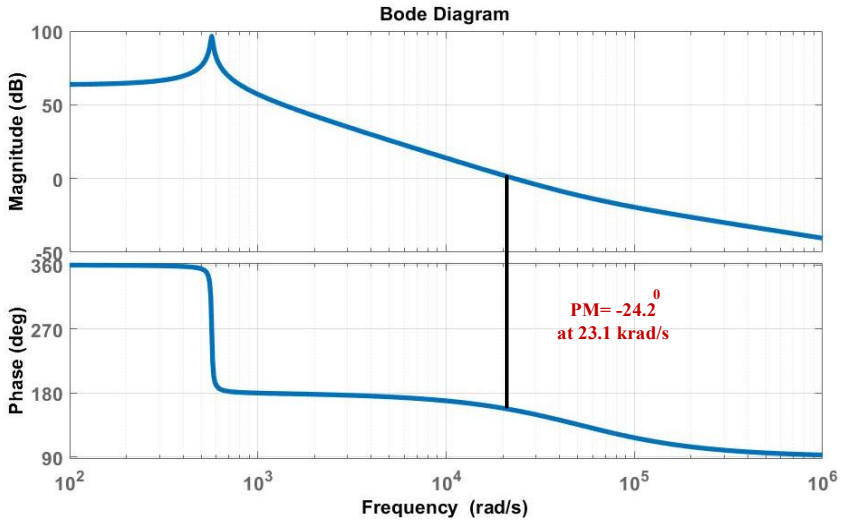


Fig 3.4 control-to-output transfer function

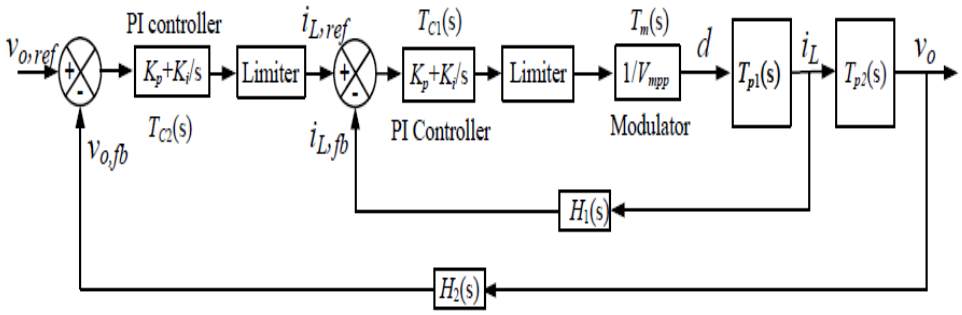


Fig. 3.5. Complete two-loop average current control system schematic diagram.

Specifications and the components' values of the converter are shown in Table I and are determined from the steady-state analysis and are similar to the [35]. 288-300 V output is for fuel cell vehicle application. Switching frequency of 100 kHz is chosen to make a balance between the switching losses and the conduction losses. It is also the same as reported in [35]. The converter does not eliminate the turn-off losses of the secondary (load) side devices and turn-on losses of the primary side (source) devices. Therefore, too high switching frequency may compromise the efficiency. The purpose of this paper is to design and test the performance of the controller. Converter power of 250W is chosen just to develop a proof-of-concept hardware prototype in research lab and test the controller performance. The controller, once satisfactory, can be used for higher power level and does not need any scaling.

Fig 3.4 Bode plot of the control-to-output voltage transfer function given by (3.27) is plotted. The gain cross-over frequency and the phase margin (PM) is shown in Fig. 3.4 of the system without controller are negative. This makes the system sensitive to small disturbances in input or source voltage and load current.

Fig. 3.5 shows the complete two-loop feedback control system using 2 PI controllers and 1 modulator having the same values of frequency and amplitude, but phase shifted by 180°. Two-loop control consists of outer voltage control loop and inner current control loop. These two loops are designed separately. Outer voltage loop bandwidth (BW) is set much lower than the inner current loop, which simplifies the design [40-41]. Therefore, the inner current loop with higher BW has fast dynamics than outer voltage loop. Voltage control loop regulates the output voltage by generating reference for the input inductor current, i_{Lref}. Inductor current i_L is tuned to this reference value by adjusting the duty ratio of the switches.

3.3.1 Designing of Current Control Loop:

The schematic diagram of the inner current control loop is shown in Fig. 3.6 Input inductor current is fed back to the error amplifier with the gain of $H_1(s)$. Output of the PI controller is sent to the modulator to generate the gating signals. Then inductor current i_L is regulated by adjusting the duty ratio of the switches.

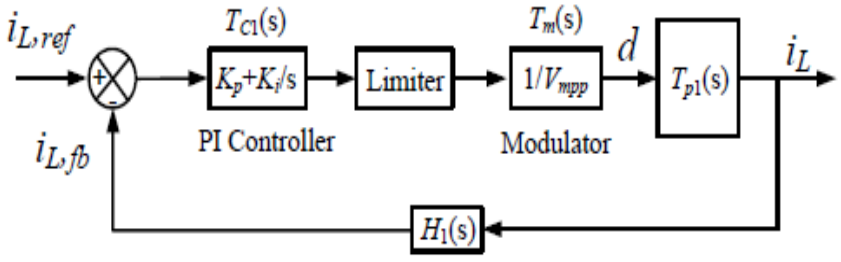


Fig. 3.6. Inner current control loop schematic diagram.

Duty ratio to the inductor current transfer function is derived from (3.28) and given by (3.29). The Bode plot of current control loop transaction function $T_{p1}(s)$ without controller is plotted Fig 3.7, which shows of PM= 90^0 at 2790 krad/s.

$$T_{p1}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}_s(s)} = \frac{\left(\frac{2c_oV_o}{n}\right)s + \frac{2V_o}{nR_L} + \frac{4(1-D)I_L}{n \quad n}}{(LC_o)s^2 + \frac{L}{R_L}s + \frac{4(1-D)^2}{n^2}} \tag{3.28}$$

$$T_{p1}(s) = \frac{0.0165s+0.4166}{(5.849*10^{-9})s^2+(73.6*10^{-9})s+0.0009} \tag{3.29}$$

A PI controller is introduced and designed to increase the low frequency gain, to reduce the steady-state error between the generated and actual inductor current and to achieve stability over a certain range.

Transfer function of $T_{c1}(s)$ of a PI controller is given by,

$$T_{C1}(s) = K_p + \frac{K_i}{s} = \frac{K_p(s + K_i / K_p)}{s} \tag{3.30}$$

Open loop transfer function $T_{oL1}(s)$ of the current loop is given by,

$$T_{OL1}(s) = T_{C1}(s) \cdot T_m(s) \cdot T_{p1}(s) \cdot H_1(s) \tag{3.31}$$

LEM sensor LA25-NP is used to sense the inductor current and to provide the isolation between power circuit and controller. Here current feedback gain is chosen as $H_1(s)$ =1. The voltage signal at the output of the current controller (limited to the range of 0 to 3.3V) is converted from analog to digital and used to control duty ratio of PWM blocks. They work together serving as the modulator. The duty ratio of the primary switches is restricted to the range or 0.55 to 0.8. Considering the gain of ADC (the modulator phase lag introduced by conversion delay of ADC has been neglected) and subsequent digital process, overall gain of the modulator is given as,

$$T_m(s) = \frac{1}{10} \tag{3.32}$$

For the given specifications, open loop transfer function of the current loop is given by,

$$T_{OLI}(s) = \frac{(8.9*10^6)K_p\left(s+\frac{K_i}{Kp}\right)(3.96*10^{-2}s+1)}{(s^3+12.5s^2+15.38*10^4 s)} \ . \tag{3.33}$$

PI controller parameters are designed to obtain PM of 60º (3.34) [42] at the gain crossover frequency (unity gain, (3.35), (3.36)) of 12.6 krad/s (2 kHz). It results in the gain $K_p$and $K_i$as 1.1261 and 11547.34 respectively.

$$\angle T_{OL1}(jw_c) = PM - 180^o \tag{3.34}$$

$$T_{OL1}(jw_c) = \frac{8.9*10^6\, k_p\left(jw_c+\frac{k_i}{k_p}\right)(0.0396jw_c+1)}{jw_c({jw_c}^2+12.5jw_c+15.38*10^4)} \tag{3.35}$$

$$k_p{}^2\left(1.5625 * 10^{10} + \frac{k_i{}^2}{k_p}\right) = 1.9814 * 10^{15} \tag{3.36}$$

The bode plot for compensated current loop is shown in Fig 3.8 with PM=60^0at12.6 krad/s (2 kHz). Also low-frequency gain is improved. Fig. 3.8 shows the Bode plot of the compensated transfer function showing improved low frequency gain and the expected PM at desired crossover frequency.

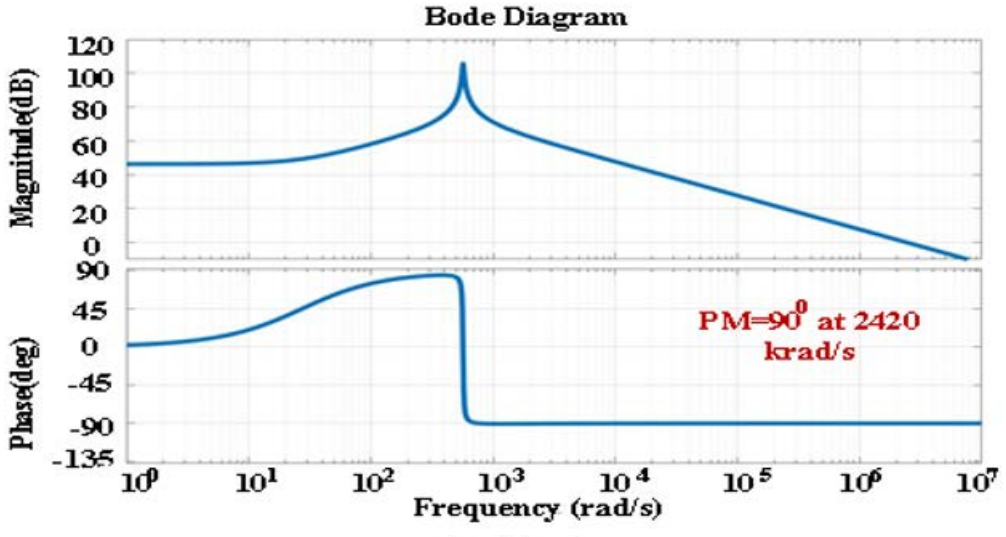


Fig. 3.7. Bode plot of uncompensated control to input current transfer function: PM = 90^0at 2420 krad/s

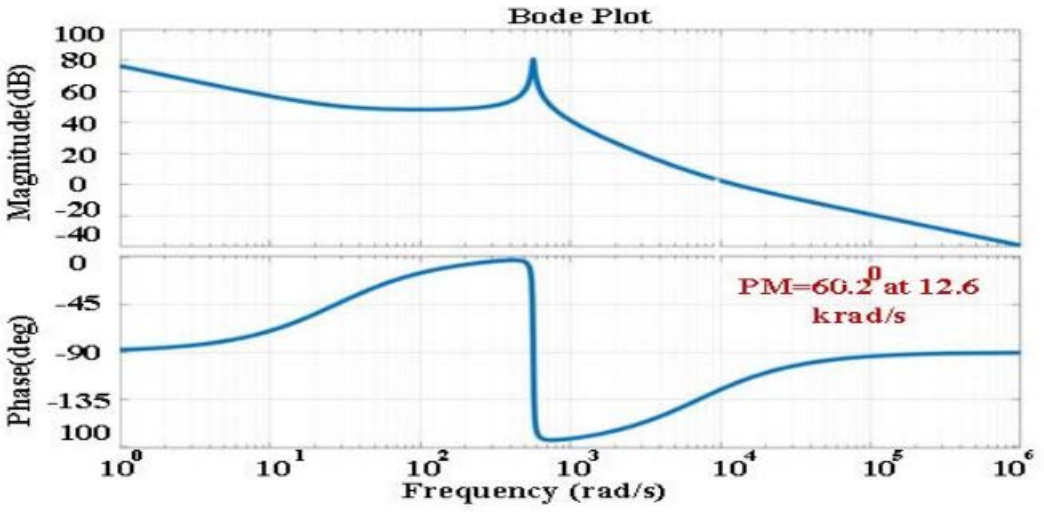


Fig. 3.8. Bode plot of compensated current loop transfer function: PM = 60^0 at 12.6 krad/s

3.3.2 Designing of Voltage Control Loop:

Outer voltage control loop regulates the output voltage at the reference value by setting reference for the current through the input inductors as shown in Fig. 3.9. Inner current control loop has faster dynamics in compare to outer voltage loop. So, the current loop dynamics are neglected during the design of voltage controller [43]. Its transfer function is not included and the perturbation in duty cycle can be neglected. Therefore, inductor current to output voltage transfer function T_{p2} (s) is obtained as (3.37). Fig. 3.10 shows corresponding bode plot with 90 rad/s gain crossover frequency. Open loop transfer function $T_{oL2}(s)$ is given by (3.38) with feedback gain $H_2(s)$ of 24, and PI type as controller.

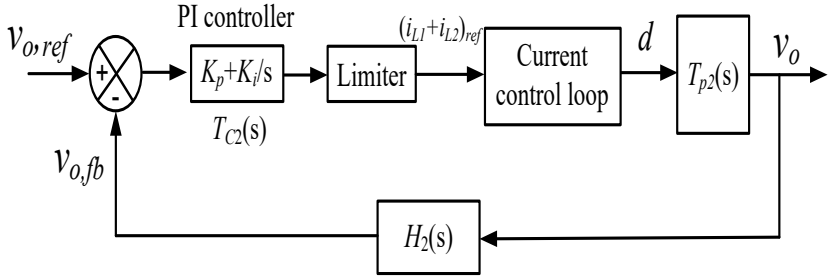


Fig. 3.9. Outer voltage control loop schematic diagram.

$$T_{p2}(s) = \frac{v_o(s)}{i_L(s)} = \frac{2(1-D)}{nC_o(s+\frac{1}{R_L C_o})} \tag{3.37}$$

$$T_{OL2}(s) = T_{C2}(s)T_{p2}(s)H_2(s) = \frac{3.636K_p\left(s+\frac{K_i}{K_p}\right)}{s^2+12.59s} \tag{3.38}$$

PI controller parameters are designed to obtain PM of 60º at the gain crossover frequency of 12.6 krad/s. It results in the gain K_p and integrator time constant K_i as 5 and 9523.8, respectively. Required PM is achieved from this design of PI parameters, which can be observed from the frequency response of the voltage control loop in Fig. 3.11, which is 10 times slower than the current gain cross over frequency.

Overall transfer function $T_{oL}(s)$ of the system is derived given in (3.39)

$$T_{OL}(s) = \left[\frac{T_{C1}(s)\cdot T_{p1}(s)\cdot T_m(s)\cdot H_1(s)}{1+T_{C1}(s)\cdot T_{p1}(s)\cdot T_m(s)\cdot H_1(s)}\right]\cdot T_{C2}(s)\cdot T_{p2}(s)\cdot H_2(s)\cdot\frac{1}{H_1(s)} \tag{3.39}$$

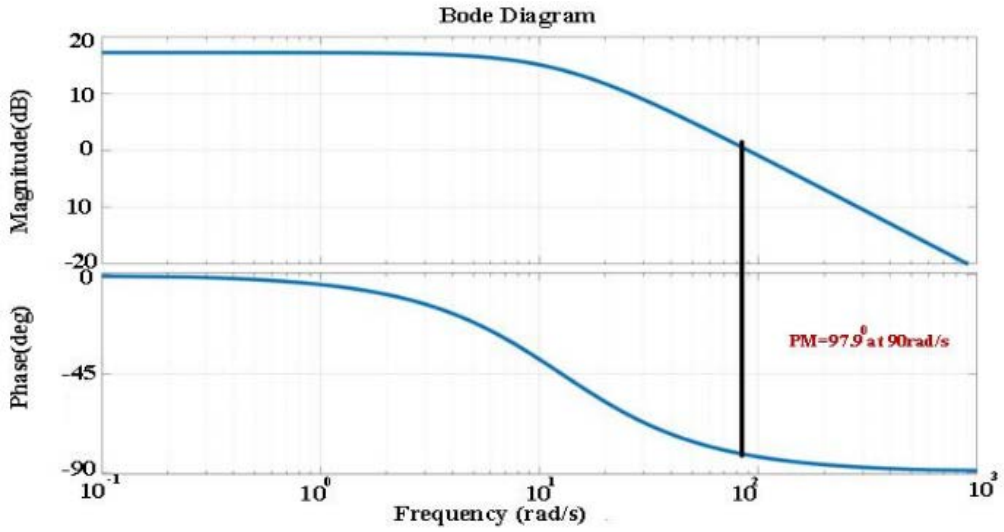


Fig 3.10. Bode plot of uncompensated plant in voltage control loop: PM = 98^0 at 90 rad/s.

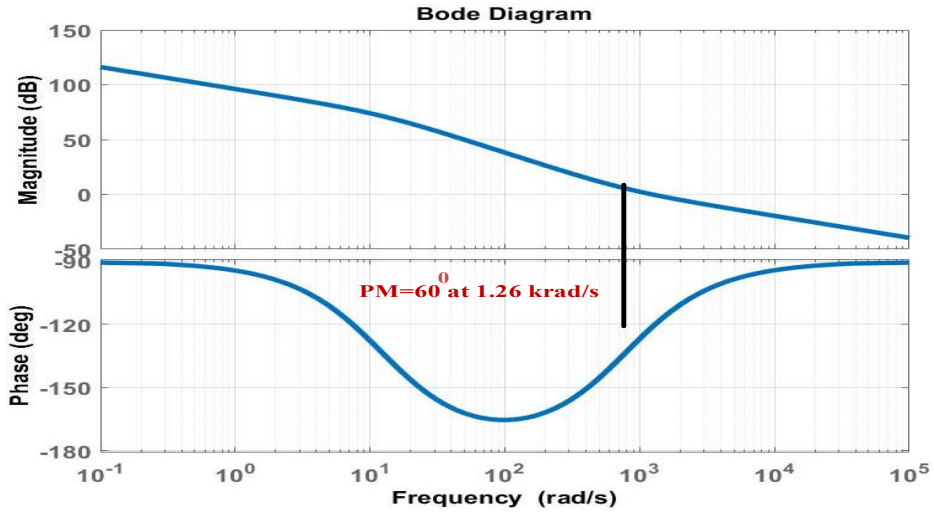


Fig 3.11. Bode plot of compensated system in voltage control loop: PM = 60^0 at 1.26 krad/s.

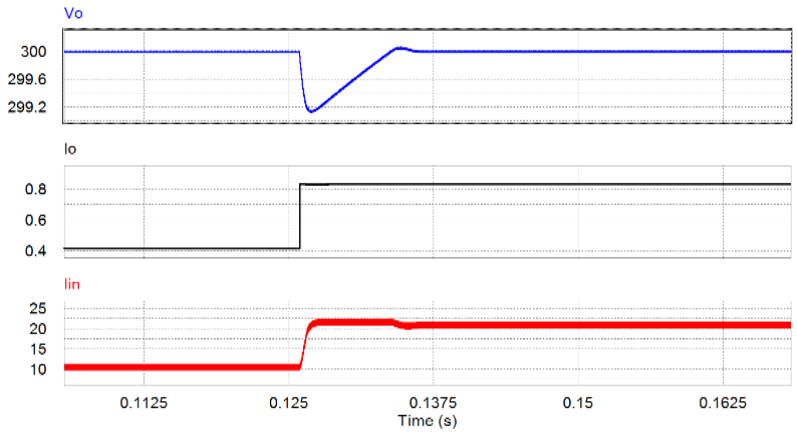
Gain at lower frequency is high indicating zero steady state error. Positive PM has been achieved resulting in a stable system with better control against disturbances for wide range in source voltage and load current variations.

3.4. Simulation and Experimental Results

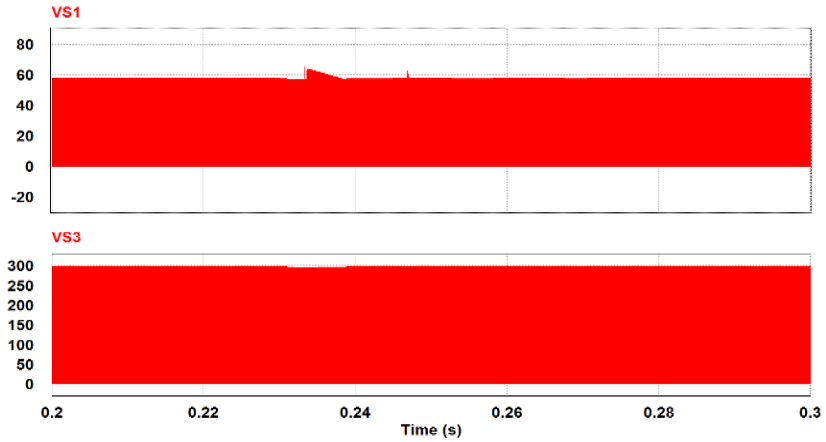
Simulation model of the circuit topology with designed two-loop control was developed on software package PSIM 11.1.64 and simulated to capture waveforms during transients under load

disturbances. Corresponding simulation outcomes are illustrated in Fig. 3.12 and Fig. 3.13. The load change from half-load to rated load and from rated load to half-load, respectively.

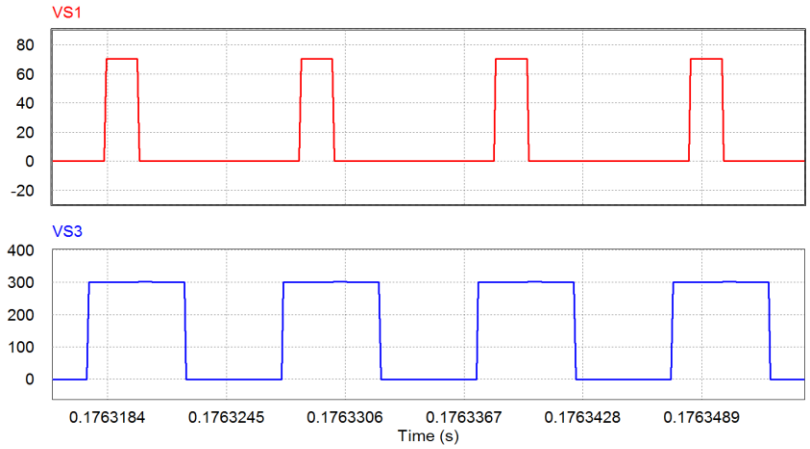
It should be noted that the overshoot or undershoot in output voltage is approximately 6V (2%) for both step changes. Further, it can be observed that the load current and input inductor current adjust very smoothly to the next steady-state value without overshoot. The setting time of both input boost inductor current and output voltage is nearly 8ms. These results demonstrate that the converter operates continuously and safely during sudden transients. Fig. 3.12(a) illustrates that the output voltage remains constant with a 3V dip during transient period. Fig. 3.12(c), zoomed portion of Fig. 3.12(b) during transient period, shows nearly 2% overshoot in the voltage across primary side devices while voltage across the secondary side devices is naturally clamped at output voltage. Fig. 3.12(e) shows steady-state (zoomed) waveforms of primary (i_{s1}) and secondary device switch current (i_{s3}) and inductor current (i_L) at rated load. It is clearly observed that the primary side devices maintain ZCS and secondary side devices maintain ZVS despite of the load fluctuations. Similar performance is observed for step change in load from rated load to half-load as demonstrated in Fig 3.13. Current through the load, switches, inductor, and transformer are smoothly reaching to the next steady state without significant overshoot. Output voltage is quickly regulated with 3V jump. Fig 3.13(c), which is zoomed version of Fig 3.13(b) during transient period, shows small overshoot in voltage across Voltage across the secondary side devices is always clamped at output voltage. Fig. 3.13(e) shows steady-state waveforms at full-load.



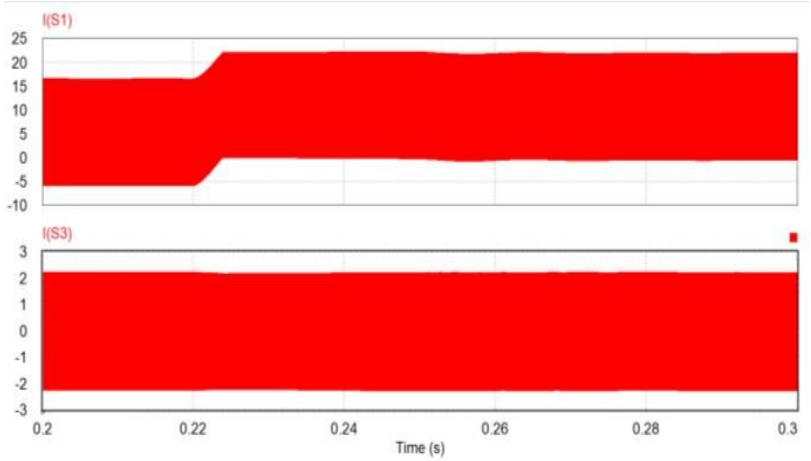
(a)


VS1
80
60
40
20
0
-20
VS3
300
250
200
150
100
50
0
0.2
0.22
0.24
0.26
0.28
0.3
Time (s)

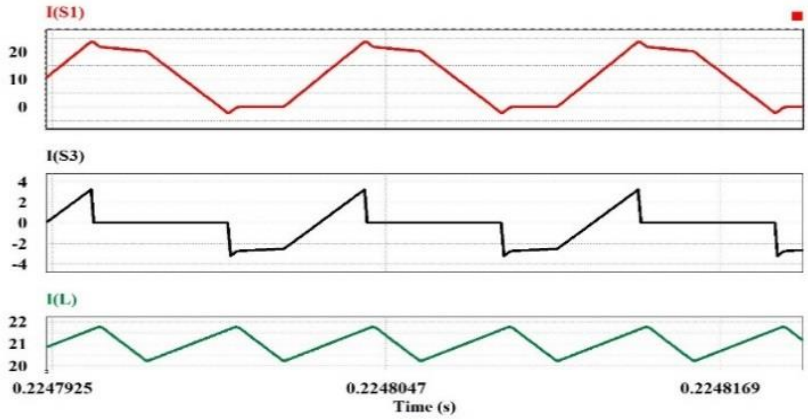
(b)


VS1
80
60
40
20
0
-20
VS3
400
300
200
100
0
0.1763184
0.1763245
0.1763306
0.1763367
0.1763428
0.1763489
Time (s)

(c)

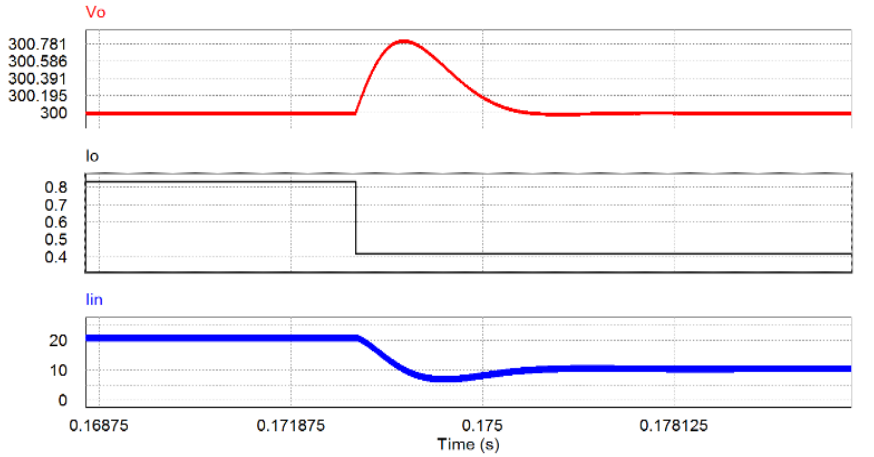

I(S1)
25
20
15
10
5
0
-5
-10
I(S3)
3
2
1
0
-1
-2
-3
0.2
0.22
0.24
0.26
0.28
0.3
Time (s)

(d)

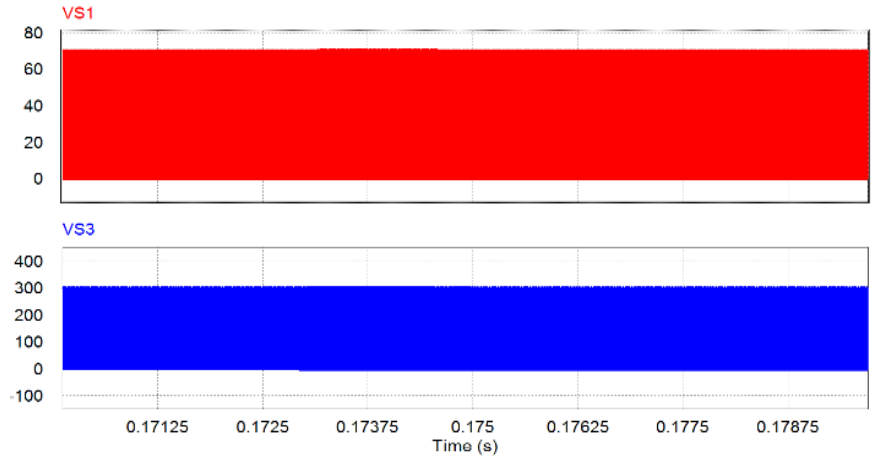


(e)

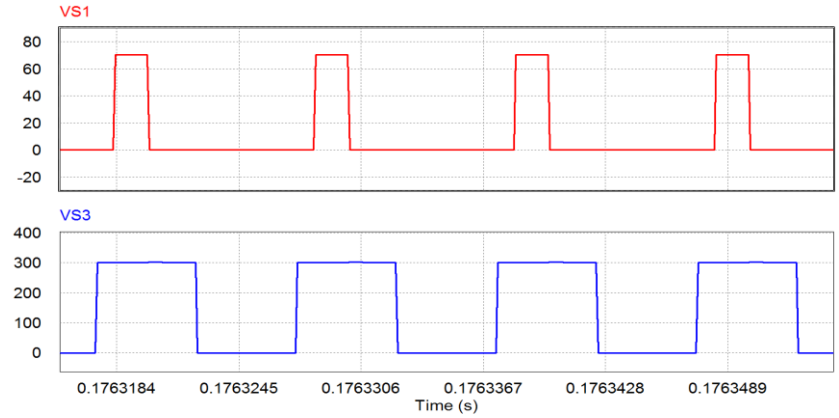
Fig. 3.12. Simulation waveforms for V_{in}=12V with step change in load from half load to rated load; V_o is output voltage, I_o is output current, I_L is input inductor current, i_{S1} and i_{S2} are current through the switches S_1 and S_3, respectively, V_{S1} and V_{S3} are voltage across the switches S_1 and S_3, respectively.



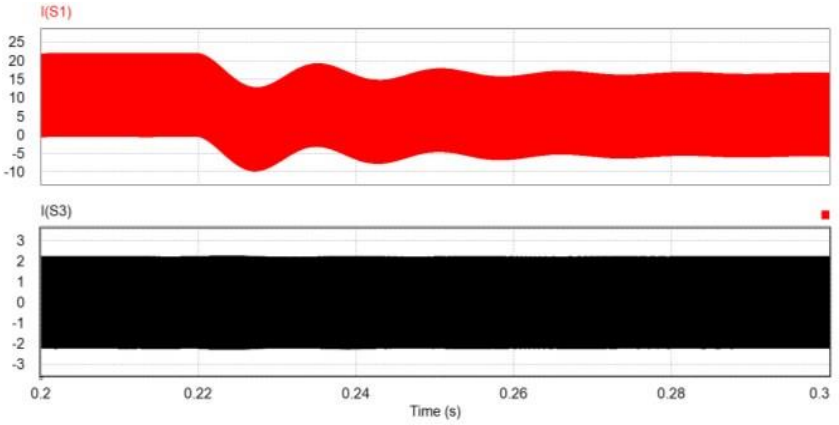
(a)



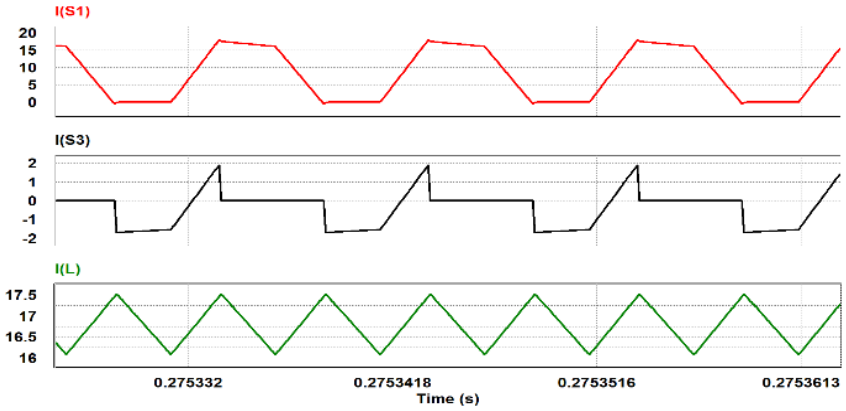
(b)



(c)



(d)



(e)

Fig. 3.13. Simulation waveforms for V_{in}=12V with step change in load from rated load to full load; V_o is output voltage, I_o is output current, I_L is input inductor current,i_{S1} and i_{S2} are current through the switches S_1 and S_3, respectively, V_{S1} and V_{S3} are voltage across the switches S_1 and S_3, respectively.

Table II: Components' Parameters of the Hardware Prototype:

Components	Parameters
Primary Switch (S_1, S_2)	IRFB4127PbF 200V, 76A, $R_{ds,on}$ =17mΩ
Secondary Switch(S_3, S_4)	IPP60R125CP 650V, 11A, $R_{ds,on}$ =0.125Ω
Series Inductors	TDK5901PC40Z core, 3.7 µH and 3.9 µH
HF transformer	3C95ETD49 ferrite core; N_1=5, N_2=45
Boost Inductor	3C95ETD49 ferrite core, $N = 12$, $L = 22.5$µH
Output CapacitorC_O	220µF, 450 V electrolytic capacitor 0.68 µF, 450V high frequency film capacitor

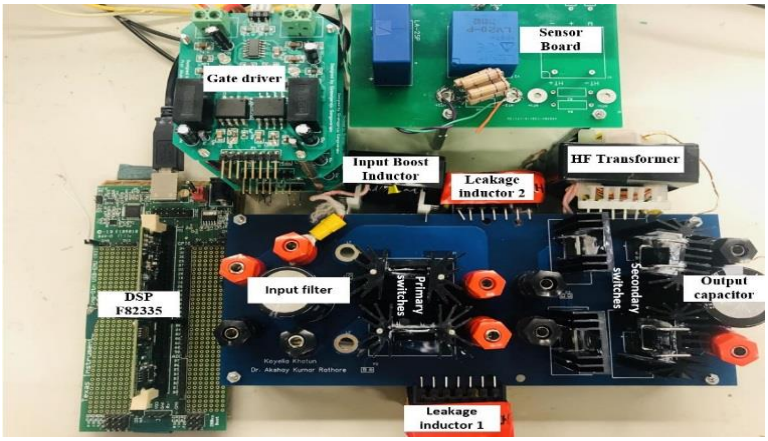


Fig. 3.14. Laboratory prototype of push-pull converter

It shown that the primary side devices maintain ZCS and secondary side devices maintain ZVS under all conditions. The transient results are satisfactory, and steady-state results are as expected.

The designed controller has been implemented tested in lab for step changes in load from 25% to 75% load and vice-versa for fixed 12-V input voltage Fig. 3.14 shows the experimental hardware laboratory prototype of the CFPP dc-dc converter. The hardware prototype details are given in Table II. DSP TMS320F28335 is used to generate the pulses for the power electronic switches according to command from the controller.

Fig. 3.15 show the variations of inductor current i_L, voltage V_{AB}, output voltage V_o with respect to time for step change in load from 25% to 75% load. The same waveforms for step change in load

from 75% load to 25% load are shown in Fig. 3.16. Output voltage is regulated at a constant value with negligible overshoot and undershoot. During the transient period, it should be seen from Fig. 3.15 and Fig. 3.16 that the transformer voltage V_{AB} is unaffected. Therefore, the switches do not experience any voltage spike during transition which ensures safe and continuous operation of the switches. It confirms the voltage clamping across the devices. Inductor current i_L waveform is adjusted to their new steady-state value smoothly. Further, output voltage V_o is maintained constant. It demonstrates stable performance over wide load range. Inductor current i_L variation remain within the limiting values. The settling time is nearly 30 ms. The sudden change in load causes a jump in switch voltage and current during transient period but these values are within safe limiting values as desired which maintains converters safe operation. Also. Converter maintains soft-switching during transient period. The transient results are satisfactory and it matches with the simulation results.

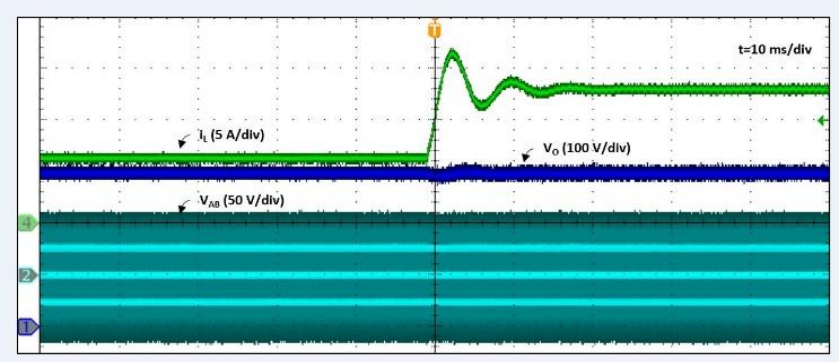


Fig. 3.15 Hardware result for step change in load from 25% load to 75% load (10 ms/div): (1) voltage V_{AB} (50 V/div), (2) inductor current i_L (5 A/div) and (3) output voltage V_O (100 V/div).

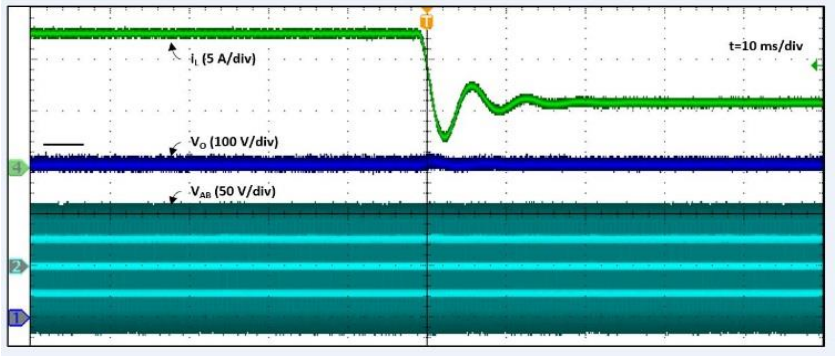


Fig. 3.16.Hardware results for step change in load from 75% load to 25% load (10 ms/div): (1) voltage V_{AB} (50 V/div), (2) inductor current i_L (5 A/div) and (3) output voltage V_O (100 V/div).

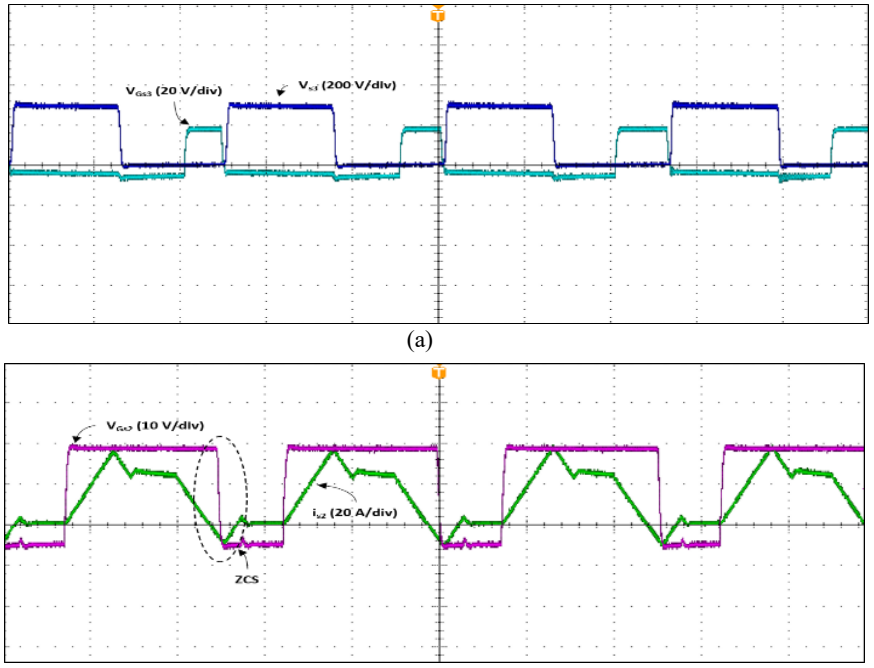


Fig. 3.17.Experimental results for V_{in}=12V at 75% load (a) Gate- to-source voltage V_{GS3}(10 V/div) and drain-to-source voltage V_{ds}(100 V/div) ,(b) Gate-to-source voltage V_{GS2}(10 V/div) and current across primary-side MOSFET.

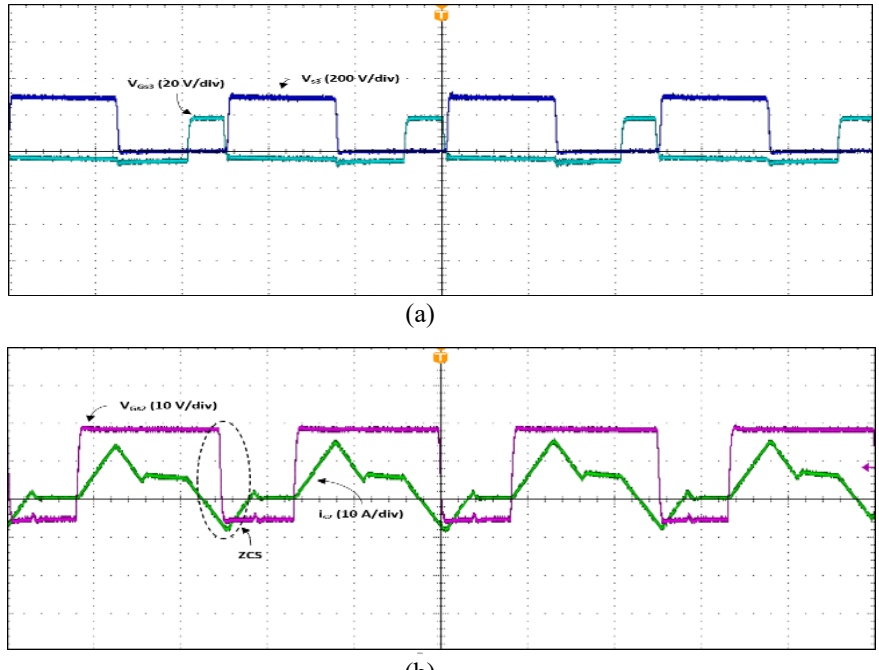


Fig. 3.18.Experimental results for v_{in}=12V at 25% load (a) Gate- to-source voltage V_{GS3}(10 V/div) and drain-to-source voltage V_{ds}(100 V/div), (b) Gate-to-source voltage V_{Gs2} $(10\ V/\mathrm{div})$ and current across primary-side MOSFET.

Figs 3.17-3.18 show the steady-state waveforms of gate-to-source voltage (V_{GS}) of primary and secondary devices, drain-to-source V_{ds} voltage waveform across secondary devices, and current waveform across primary devices under 75% and 25% load, respectively. Waveforms of Fig. 3.17(b), 3.18(b) clearly confirms the ZCS of primary devices. The current through the switch naturally reaches zero followed by the antiparallel body diode conduction (negative current) prior to turning-off the gating signal. Also, from the Fig. 3.17(a) and 3.18(a), ZVS turn-on of the secondary switches should be observed. In the secondary device, gate-to-source voltage (V_{GS3}) is applied when the voltage across secondary device is zero already that ensures ZVS operation in secondary devices.

It should be noticed that the overshoot and undershoot of inductor current I_L are higher than the simulation results as wel as the response/settling time. In the real experimentation, the circuit experiences power loss, voltage drop, stray inductance/capacitance, and parasitic causing the aberration from the ideal model. Better dynamic performance may be achieved by proper tuning of the controller parameters, which is a usual practice.

It should be noticed that with the sudden load change, the inductor current should settle within a reasonable time; however, it does not due to the collapse of the magnetic energy within the input inductor and it takes certain time to reach the next steady state value. This input inductor current transfer from one primary winding to the other primary winding of the transformer cannot be instantaneous due to the fundamental property of opposing the change in current. This time lag is generally decided by the LCR parameters of the circuits.

This converter is promising for fuel cell application. The controller is intentionally designed for slow response below 50 ms and it gives satisfactory result. However, if the converter application is designed for battery charging application, then the settling time should be lower and can be reduced by increasing the outer loop bandwidth of the controller.

3.5 Conclusion

In this Chapter, detailed small signal analysis of the snubberless naturally-clamped soft-switching current-fed push-pull dc-dc converter is reported. State variables are defined and state space averaging technique is followed to systematically derive the small signal model of the converter. Placing the power circuit components' values from the steady-state design, the small signal model is presented in numerical form. Two-loop average current control methodology is

followed to design a closed loop control system using 2 PI controllers to meet the frequency response requirements and obtain stability during load disturbances and transients. A detailed and systematic procedure to design the inner current control loop and outer voltage loop are illustrated. Simulation results obtained through PSIM 11.1.64 are presented to verify the controller design and investigate the initial transient performance of the converter. Experimental results on a proof-of-concept hardware laboratory prototype are shown to demonstrate the satisfactory transient performance of the converter and effectiveness of the implemented controller.

Chapter 4

Small Signal Analysis and Control of partial resonance impulse commutated CFHB dc/dc converter

4.1 Introduction

This chapter presents the small signal analysis, derives the transfer functions, and reports a controller design for the closed loop operation of partial resonance impulse commutated CFHB dc/dc converter. A complete design procedure is presented. Simulation results using PSIM 11 with the designed controller of variable frequency control and fixed frequency control of partial resonance impulse commutated current-fed half-bridge topology are shown to validate the stability of the control system. It has been discussed that snubberless current-fed converters with all controlled semiconductor devices have been proposed, studied and analyzed for the device voltage clamping at their turn-off. Several applications such as solar and fuel cells, prefer unidirectional converters in order to reduce the hardware, control, and footprint requirements along with operational complexity. The device voltage-clamping problem has been addressed through partial-resonance-pulse, thus introducing another class of impulse-commutated current-fed converters. It is done by a parallel tank that achieves zero current switching (ZCS) of semiconductor devices. A non-isolated impulse-commutated current-fed half-bridge topology is shown in Fig. 4.1. Detailed steady-state analysis, converter design, and steady-state performance of this converter are presented in [44]. Steady-state operating waveforms are shown in Fig. 4.2 [44]. However, its small signal analysis, mathematical transfer functions, closed loop control design, and transient results are not yet reported.

The objective of this Chapter is to simulate the transient performance of the converter using variable frequency and duty cycle control. Systematic small signal model of the converter has been derived using variable frequency control in Section 4.2.1. Step-by-step closed loop controller design employing two-loop average current control using variable frequency control approach is presented in Section 4.2.2. Simulation results using variable frequency control are illustrated to

verify the controller design and converter performance in Section 4.3. Similarly, Systematic small signal model of the converter has been derived using variable duty control in Section 4.4.1. Step-by-step closed loop controller design employing two-loop average current control using duty cycle control approach is presented in Section 4.4.2. Simulation results using variable duty control are illustrated to verify the controller design and converter performance in Section 4.5.

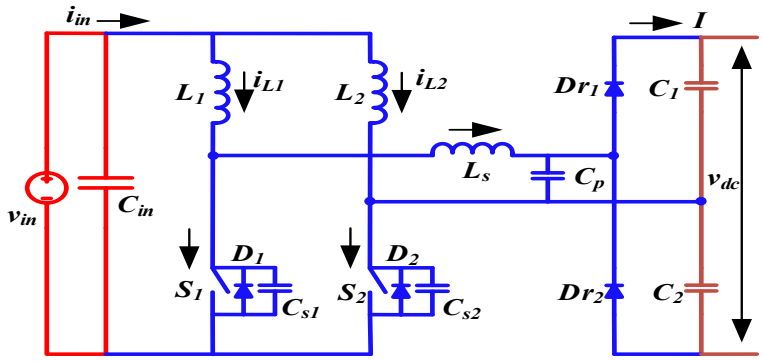


Fig. 4.1. Parallel-LC resonant current dc-dc converter topology [44].

4.2 Variable frequency control of partial resonance impulse commutated CFHB dc/dc converter

Controlling resonant type power converters are complicated, since it requires frequency modulation, instead of the simpler fixed-frequency duty cycle modulation. In this section, the small signal model, the transfer functions derivation and controller design using variable frequency control for closed loop operation are reported for voltage regulation and power flow control.

4.2.1 Small Signal Analysis

In this section, state-space equations for each interval of operation are listed and followed by derivation of small ac model using state-space averaging, small signal model is derived. State phase equation of each interval of operation are mentioned. Primary switches have identical gating signals with 180º shifted from one another. The duty cycle of primary switches is always kept above 50%. The operation during different intervals in a one-half switching cycle is explained with equivalent circuits shown in Fig. 4.3.

For the analysis, the following assumptions are made: 1) all the components are assumed ideal and lossless; 2) Inductors L_1 and L_2 are assumed large so that current through them can be considered

constant; 3) Series inductor L_s indicate the leakage inductance of resonant tank; and 4) Magnetizing inductance is very large.

Interval (Fig 4(a); (t_0-t_1):

During this interval, Primary switch S_1 and rectifier diode D_2 is conducting Power is transferred through load to source. Switch S_2 is blocking the voltage $V_{dc}/2$. Switch S_1 is carrying the entire input current I_{in} while $-I_{in}/2$ flows through series inductor. State equations of this interval are:

$$L_1 \frac{d_{il1}}{d_t} = v_{in} \tag{4.1}$$

$$(L_2 + L_{ls}) \frac{di_{l2}}{dt} = \left(v_{in} - \frac{v_{dc}}{2}\right) \tag{4.2}$$

$$C_o \frac{dv_0}{dt} = \left(I_{in} - \frac{v_o}{R_l}\right) \tag{4.3}$$

Interval (Fig 4(b);(t_2-t_3): Both primary switches conduct in this interval. Reflected output voltage $V_{dc}/2$ appears across the series inductor and i_{ls} starts increasing. It causes current through S_2 start increasing while the current S_1 start decreasing. State equations of interval 1 still hold good.

Interval (Fig 4(c); (t_3-t_4): Capacitors C_1 and C_2 constituting the voltage doubler feed the load. The resonance between L_s and C_p commences. The energy stored in the tank increases. The switch currentsi_{s1} and i_{s2} start decreasing and increasing, respectively in a resonant fashion. State equations of this interval:

$$(L_1 + L_{ls}) \frac{di_{l2}}{dt} = (v_{in}) \tag{4.4}$$

$$L_2 \frac{d_{il1}}{d_t} = v_{in} \tag{4.5}$$

$$C_o \frac{dc_p}{dt} = (I_{ls}) \tag{4.6}$$

Interval (Fig 4(d); (t_4-t_5): Due to resonance, current i_{ls}rises above $I_{in}/2$. This additional current flows through the body- diode of S_1leading to ZCS turn-off of switch S_1. State equations of interval 3 still hold good.

Interval (Fig 4(e); (t_5-t_6): During this interval constant current $I_n/2$ flows through L_s and charges the parallel capacitor C_p. Input current flows through the switch S_2. State equations of interval 3 still hold good.

Identically, state equations for the other half cycle can also be derived. State equations are averaged over a HF cycle. State variable $\boldsymbol{I_{ls}}$ can be neglected in the small signal relation between V_{in}, d and V_o.

The averaged state equations of defined state variables over a HF cycle are given:

$$L_1 \frac{di_{l1}}{d_t} = 2v_{in} - \frac{v_o}{2}(d_{s1} + d_{s2}) \tag{4.7}$$

$$L_2 \frac{di_{l1}}{d_t} = 2v_{in} - \frac{v_o}{2}(d_{s1} + d_{s2}) \tag{4.8}$$

$$C_o \frac{dc_o}{dt} = i_{average} - \frac{2v_0}{R_L} \tag{4.9}$$

where $i_{average}$ is the average current feeding the output capacitor and load from secondary side H-bridge switches and is given by (4.10),

$$i_{average} = \frac{I_{in}}{2}(d_{s1} + d_{s2}) \tag{4.10}$$

On Substituting (4.10) in (4.9),

$$C_o \frac{dc_0}{dt} = \frac{I_{in}}{2}(d_{s1} + d_{s2}) - \frac{2v_0}{R_L} \tag{4.11}$$

The duty ratio of the main switches including conduction of the reverse anti-parallel diodes are defined as,

$$d_{s1} = 0.5 + \left(f_{s1} * \frac{i_{in}}{v_o} * k\right) \tag{4.12}$$

$$d_{s2} = 0.5 + \left(f_{s2} * \frac{i_{in}}{v_o} * k\right) \tag{4.13}$$

$$k = \frac{Z_r}{8 * pi * {f_r}^2} \tag{4.14}$$

Introducing perturbation in state variables such that $i_{L1} = I_{L1} + \hat{i}_{L1}$,$i_{L2} = I_{L2} + \hat{i}_{L2,} v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$, $f_{s1} = F + \hat{s}_1$, $f_{s2} = F + \hat{f}_{s2}$

For achieving dynamic model of the converter, perturbations are introduced in state variables,

$$L_1 \frac{(I_{L1} + \hat{i}_{L1})}{d_t} = 2(V_{in} + \hat{v}_{in}) - \frac{(V_o + \hat{v}_o)}{2}\left[1 + \left(\left(f_{s1} + \hat{f}_{s1}\right) + \left(f_{s1} + \hat{f}_{s1}\right)\right) * (I_{L1} + \hat{\imath}_{l1})k\right] \tag{4.15}$$

$$L_2 \frac{(I_{L2} + \hat{i}_{L2})}{d_t} = 2(V_{in} + \hat{v}_{in}) - \frac{(V_o + \hat{v}_o)}{2}\left[1 + \left(\left(f_{s1} + \hat{f}_{s1}\right) + \left(f_{s1} + \hat{f}_{s1}\right)\right)(I_{L2} + \hat{\imath}_{l2}) * k\right] \tag{4.16}$$

$$C_o \frac{d(V_o + \hat{v}_o)}{dt} = \left(\frac{I_L + \hat{\imath}_L}{2}\right)\left[1 + \left(\left(f_{s1} + \hat{f}_{s1}\right) + \left(f_{s1} + \hat{f}_{s1}\right)\right) * k\right] - \frac{2(V_o + \hat{v}_o)}{R_L} \tag{4.17}$$

In Laplace domain, the results in-

$$(sL_1 + kf_1)\hat{\imath}_L(s) + \frac{\hat{v}_o(s)}{2} = 2\hat{v}_{in}(s) - \frac{(I_{l_2} * k)}{2}\left(\hat{f}_{s1} + \hat{f}_{s2}\right) \tag{4.18}$$

$$(sL_2 + kf_1)\hat{\imath}_L(s) + \frac{\hat{v}_o(s)}{2} = 2\hat{v}_{in}(s) - \frac{(I_{l_2} * k)}{2}\left(\hat{f}_{s1} + \hat{f}_{s2}\right) \tag{4.19}$$

$$\left(2I_L kF + \frac{v_o}{2}\right)\hat{\imath}_L(s) - \hat{v}_o(s)\left(v_o c_o S + \frac{4v_o}{R_l} - \frac{I_L}{2}\right) = -\frac{{I_L}^2 k}{2}\left(\hat{f}_{s1} + \hat{f}_{s2}\right) \tag{4.20}$$

$$\begin{bmatrix}\hat{\imath}_{L1}(s)\\ \hat{\imath}_{L2}(s)\\ \hat{v}_o(s)\end{bmatrix} = [B(s)].\begin{bmatrix}-\frac{I_{L1}k}{2}\\ 0\\ -\frac{{I_L}^2 K}{2}\end{bmatrix}.\hat{f}_{s1}(s) + [B(s)].\begin{bmatrix}0\\ -\frac{I_{L1}k}{2}\\ -\frac{{I_L}^2 k}{2}\end{bmatrix}.\hat{f}_{s2}(s) + [B(s)].\begin{bmatrix}2\\ 2\\ 0\end{bmatrix}.\hat{v}_{in}(s) \tag{4.21}$$

Where,

$$B(s) = \begin{bmatrix}(SL_1 + kf_1) & 0 & 0.5\\ 0 & (SL_2 + kf_2) & 0.5\\ \left(2kf_1 I_{L1} + \frac{V_O}{2}\right) & \left(2kf_2 I_{L2} + \frac{V_O}{2}\right) & -\left(V_o C_o S + \frac{4V_O}{R_L} - \frac{I_L}{R_L}\right)\end{bmatrix}^{-1} \tag{4.22}$$

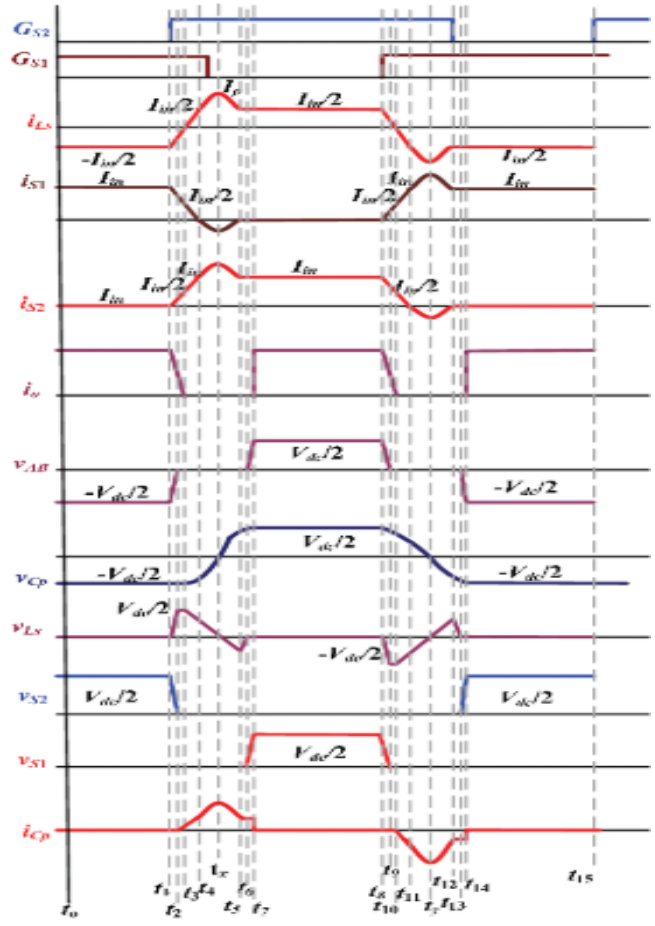


Fig. 4.2. Steady state operating waveforms of the converter [44].

$$sL\left(\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)\right)+\hat{v}_O(s)=-\frac{I_L K}{2}\left(\hat{f}_{s1}(s)+\hat{f}_{s2}(s)\right)+4\hat{v}_{in}(s) \tag{4.23}$$

Writing in matrix form,

$$\begin{bmatrix}\hat{\imath}_{L1}(s)+\hat{\imath}_{L1}(s)\\ \hat{v}_o(s)\end{bmatrix}=[B(s)].\begin{bmatrix}-\frac{I_{L1}K}{2}\\ 0\\ -\frac{I_L{}^2K}{2}\end{bmatrix}.\left(\hat{f}_{s1}(s)+\hat{f}_{s2}(s)\right)+[B(s)].\begin{bmatrix}4\\ 0\end{bmatrix}\hat{v}_{in}(s)$$

(4.24)

Where,

$$B(s)=\begin{bmatrix}(SL+kF) & 1\\ \left(2I_L kF+\frac{V_O}{2}\right) & -\left(V_O C_O S+\frac{4V_O}{R_L}-\frac{I_L}{R_L}\right)\end{bmatrix}^{-1} \tag{4.25}$$

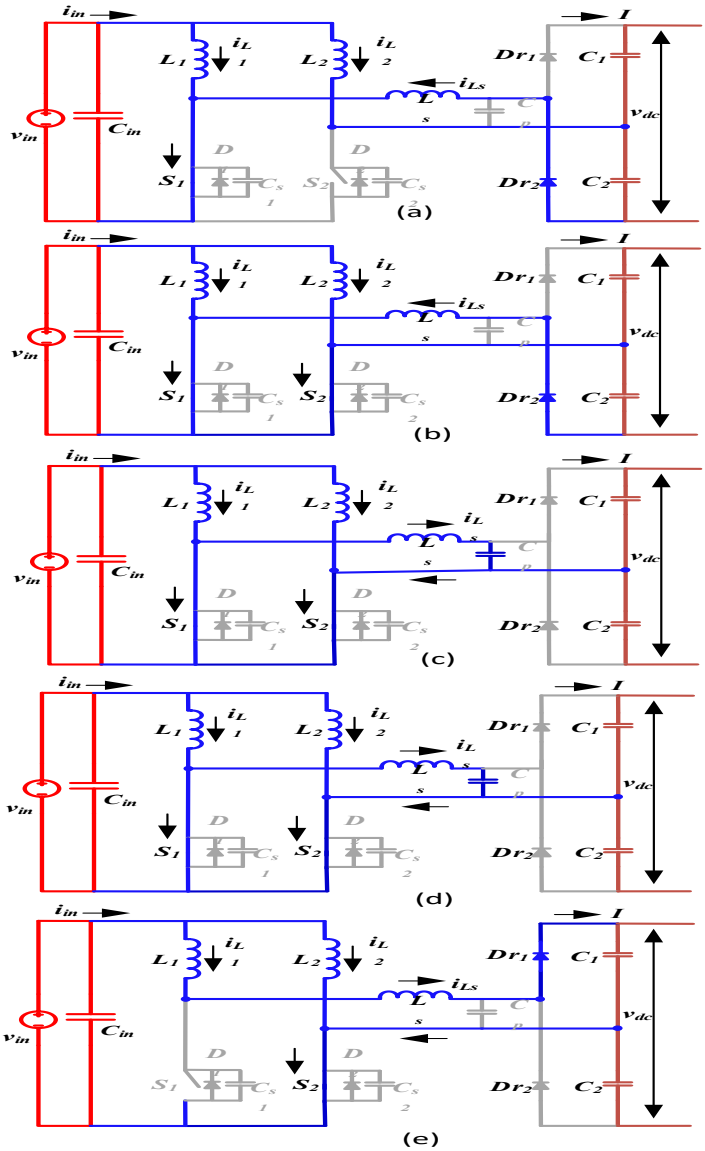


Fig. 4.3. Equivalent circuits during different intervals in half switching cycle [44].

Control-to-output transfer function is given by setting $\hat{v}_{in} = 0$ in (4.24)

$$\frac{\hat{v}_o(s)}{\hat{f}_{s1}(s)+\hat{f}_{s2}(s)} = \frac{I_L KF*0.25\left(I_L{}^2+V_O I_L-2K\right)-s(0.5V_o I_L K)}{(LC_O V_O)s^2-\left(\left(\frac{4I_L V_O+I_L L}{R_L}\right)+C_O V_O kF\right)s-\left(\frac{4kFV_O-I_L kF}{R_L}\right)} \quad (4.26)$$

4.2.2 Closed Loop Controller Design

Table 4.1: Specifications to design the control system of following converter

Input voltageV_{in}	42V
Output VoltageV_o	200V
Peak output powerP_o	500W
Switching frequency of converter f_s	40 kHz- 175 kHz
Leakage inductorL_{ls}	1.96µH,
Input Boost Inductor L	400µH,
Output CapacitorC_O	100µF
Full-loadR_L	80Ω.

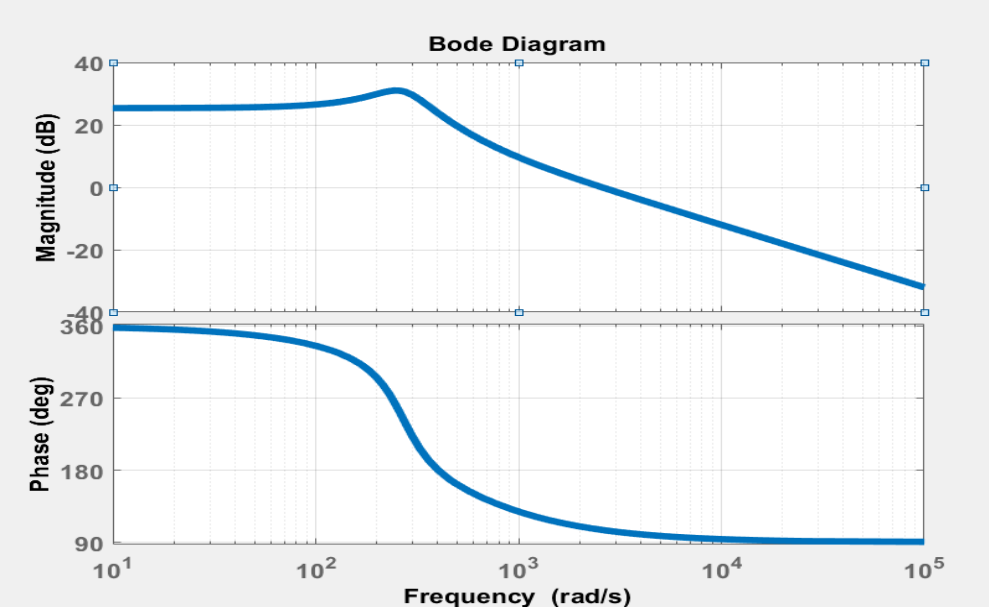


Fig. 4.4. Bode Plot of plant Transfer function

Specifications and the components' values of the converter are shown in Table 4.1 and are determined from the steady-state analysis and are similar to the [44]

Fig. 4.4 shows the bode plot of plant transfer function. It can be easily found that phase margin (PM) is negative that demonstrates the whole system is unstable.

Fig. 4.5. Illustrates two-loop average current control design, using 2 PI controller having fixed duty cycle but variable frequency modulation control with phase shift of 180^0[45].Outer loop regulates the load voltage by producing the reference values for the input inductor currents, Inductor currents are controlled by controlling the frequency of the devices.

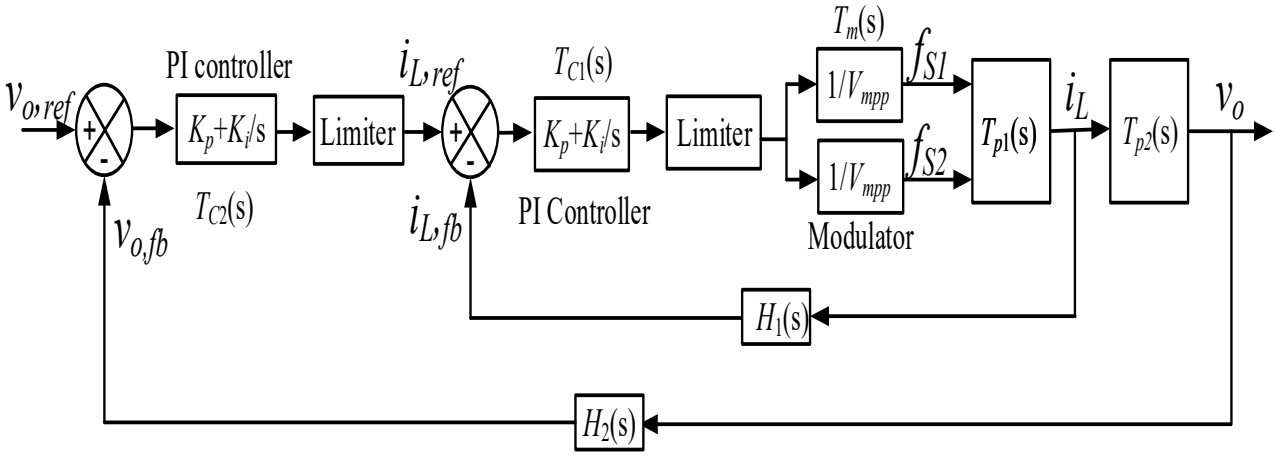


Fig. 4.5. Two-loop control system.

4.2.2.1 Designing of Current Control Loop:

Fig. 4.6 shows the schematic diagram of the inner current control loop. For generating the gating signals, output of the PI controller is sent to the modulator

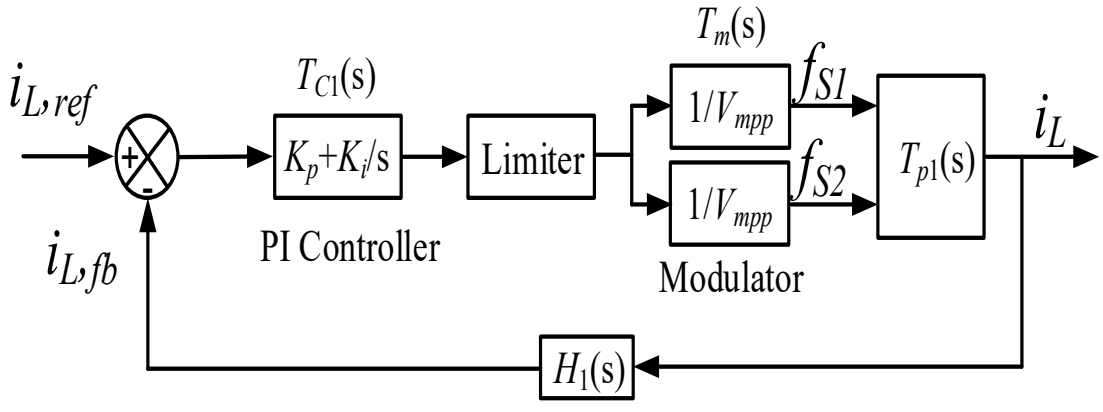


Fig. 4.6. Inner current control loop schematic diagram.

Frequency to the inductor current transfer function is given by,

$$T_{p1} = \frac{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)}{\hat{f}_{s1}(s)+\hat{f}_{s2}(s)} = \frac{\frac{(4V_O-I_L)+R_L}{R_L} - sV_oC_o}{(LC_OV_O)s^2-\left(\left(\frac{4I_LV_O+I_LL}{R_L}\right)+C_OV_OkF\right)s-\left(\frac{4kFV_O-I_LkF}{R_L}\right)} \quad (4.27)$$

For the given specifications, the frequency-to-inductor current transfer function is given by,

$$T_{p1} = \frac{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)}{\hat{f}_{s1}(s)+\hat{f}_{s2}(s)} = \frac{-0.02s+10.85}{8*10^{-6}s^2+1.62*10^{-3}s+4788.64} \quad (4.28)$$

The gain margin and phase margin of current control loop without controller shows of PM= 87^0at $2.7 * 10^4$rad /s. Thus, a PI controller is designed to increase the low frequency gain, to reduce the steady-state error between the desired and actual inductor current and to achieve stability over a certain range. Transfer function of a PI controller $T_{c1}(s)$ is given by (4.29).Transfer function of the current loop $T_{OL1}(s)$ is given by, where $H_1(s)$ is the current feedback gain and $T_m(s)$ is the overall gain of the modulator. Here current feedback gain is selected as $H_1(s)$ =1.

$$T_{c1}(s) = K_p + \frac{K_i}{s} = \frac{K_p(s+K_i/K_p)}{s} \quad (4.29)$$

Open loop transfer function of the current loop is given by,

$$T_{OL1}(s) = T_{C1}(s).T_m(s)T_{p1}(s)H_1(s) \quad (4.30)$$

So, current loop transfer function is given by,

$$T_{OL1}(s) = \frac{0.02s+0.10K_p(s+K_i/K_p)}{8*10^{-6}s^3+1.62*10^{-3}s^2+4788.64s} \quad (4.31)$$

For the given specifications, To obtain PM of 60º at 2.07k rad/s gain crossover frequency, Based on the above procedure, to obtain the calculated parameter values of PI controller are: k_p = 57.3 and the time constant of the integrator, $K_p/K_i = 3 * 10^{-5}$ respectively.

4.2.2.2 Designing of Voltage Control Loop:

Fig. 4.7 shows outer voltage control loop that regulates the load voltage at the desired value by generating reference current. value for the input inductors. As outer voltage loop has slower dynamics than the inner current control loop, during the design of voltage controller current loops dynamics are neglected [43].

For the given specification, inductor current to output voltage transfer function T_{p2}(s) is given by,

$$T_{p2} = \frac{\hat{v}_0(s)}{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)} = \frac{I_L KF*0.25\left({I_L}^2+V_O I_L-2K\right)-s(0.5V_O I_L K)}{\frac{(4V_O-I_L)+R_L}{R_L}-sV_O C_o} \quad (4.32)$$

$$T_{p2} = \frac{\hat{v}_0(s)}{\hat{\imath}_L\,(s)} = \frac{-3.53*10^{-3}s+41.85}{-0.02s+10.85} \quad (4.33)$$

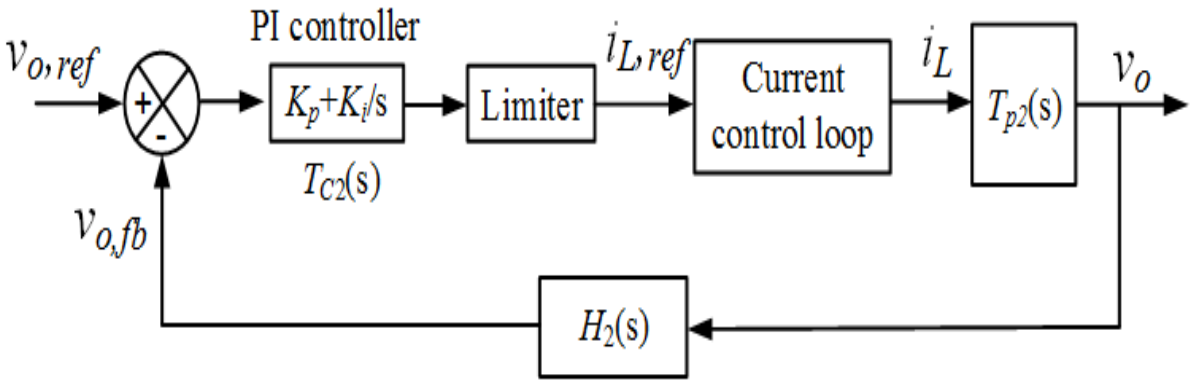


Fig. 4.7. Outer voltage control loop schematic diagram

Voltage loop transfer function is given by,

$$T_{OL2}(s) = T_{C2}(s).T_m(s)T_{p2}(s)H_2(s) \quad (4.34)$$

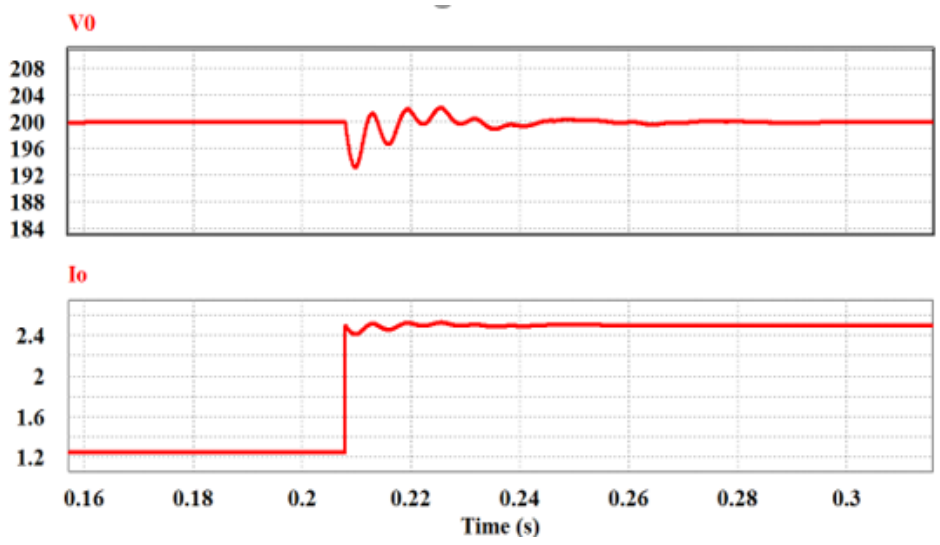
Voltage feedback gain $H_2(s)$ is selected to be 1

$$T_{OL2}(s) = \frac{-3.53*10^{-3}s+41.85K_p(s+K_i/K_p)}{-0.02s+10.85} \quad (4.35)$$

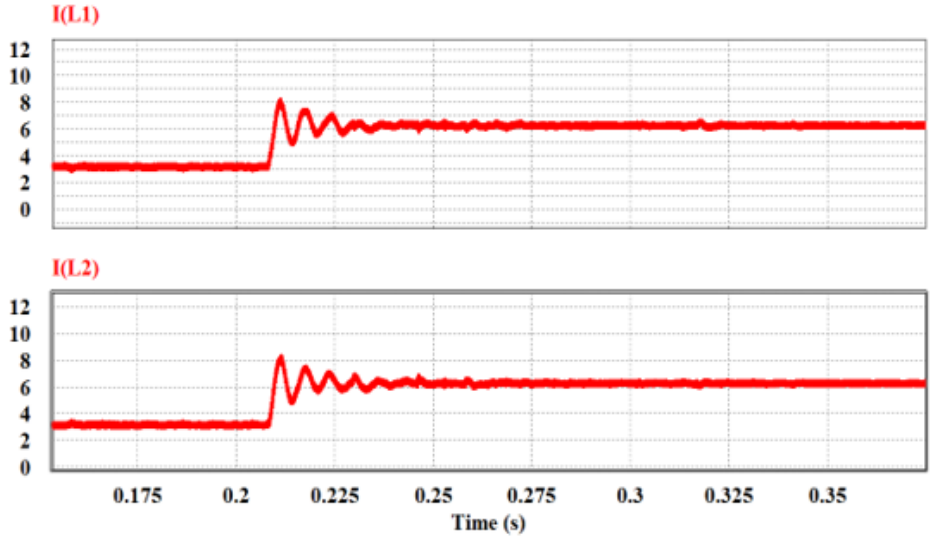
Voltage loop transfer function is given by, (4.35). Where, voltage feedback gain $H_2(s)$ is selected to be 1 and PI controller transfer function T_{C2}(s) is given by (4.29). Inner current loop is 10 times faster than gain cross over frequency of the voltage controller. Hence the phase margin should be 60º at the gain crossover frequency of 2.790 krad/s. It results in the gain k_p and integrator time constant K_p/K_i as 0.05 and $1.2 * 10^{-3}$respectively. Taking into account dynamics of current control loop. Stable system offers positive PM. As a result, it provides better control against disturbances for wide range in source voltage and load current variations. Stable system offers positive PM. As a result, it provides better control.

4.3 Simulation Results

Simulation results of two-loop control was developed on software PSIM 11.1.64. Transient performance of various load conditions of output voltage and current are illustrated in Fig. 4.8(a) and 4.9(a). The load is changed from half to rated load and vice-versa. Overshoot or undershoot in output voltage is less than 6V (0.02%) for both step changes in load. It can be noted that primary switch maintained ZCS for both full load to half load and vice-versa condition. Inductor currents are oscillated after load disturbance and then it settled down very smoothly to the next steady-State value (Fig 4.8(b), 4.9(b). Settling time can be adjusted by tuning of controller parameters. The frequency variation is between 149KHz- 162KHz (Fig 4.8(g) and 4.9(g) which is less sensitive at load variation from full load to half load and vice versa where duty is fixed at 0.56. Similar performance is observed for step change in load from rated load to half-load as demonstrated in Fig. 4.9. Current through the load, switches, inductor, and transformer are smoothly reaching to the next steady state without significant overshoot. Output voltage is quickly regulated with 5V jump. Fig. 4.8(e), which is zoomed version of Fig. 4.8(c) and Fig. 4.9(e), which is zoomed version of Fig. 4.9(c) shows steady-state (zoomed) waveforms at rated load and half-load, respectively. The transient results are satisfactory, and the steady-state results are as expected.



(a)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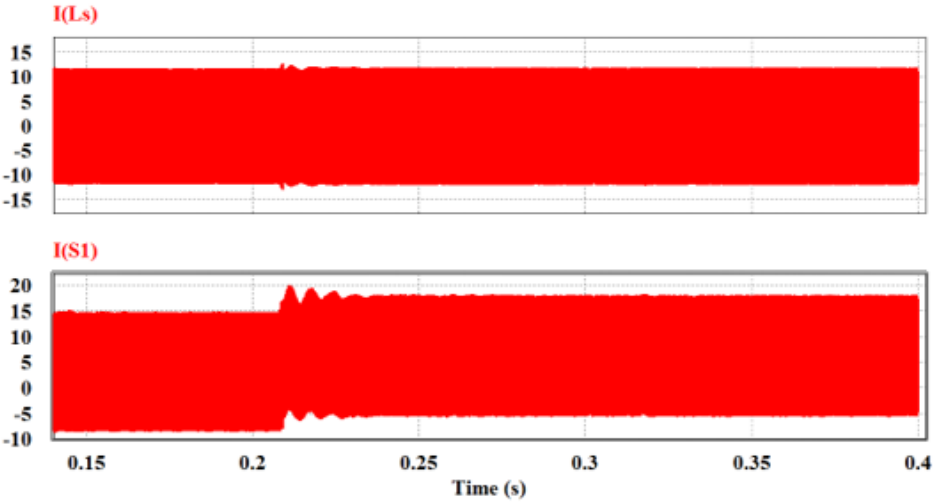
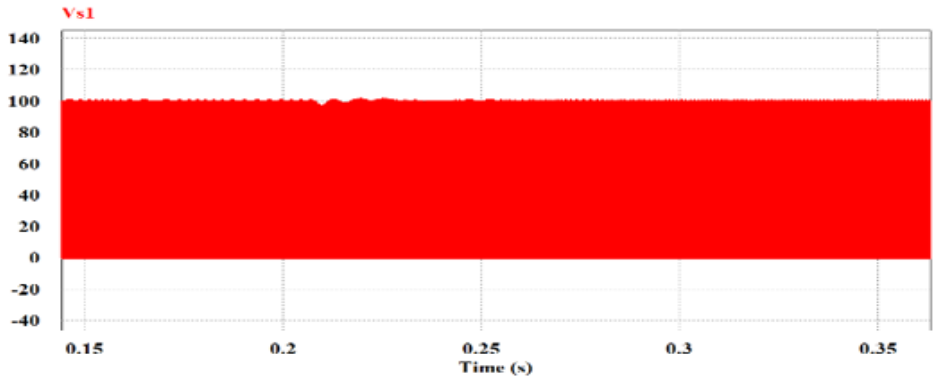
12
10
8
6
4
2
0
I(L2)
12
10
8
6
4
2
0
0.175
0.2
0.225
0.25
0.275
0.3
0.325
0.35
Time (s)

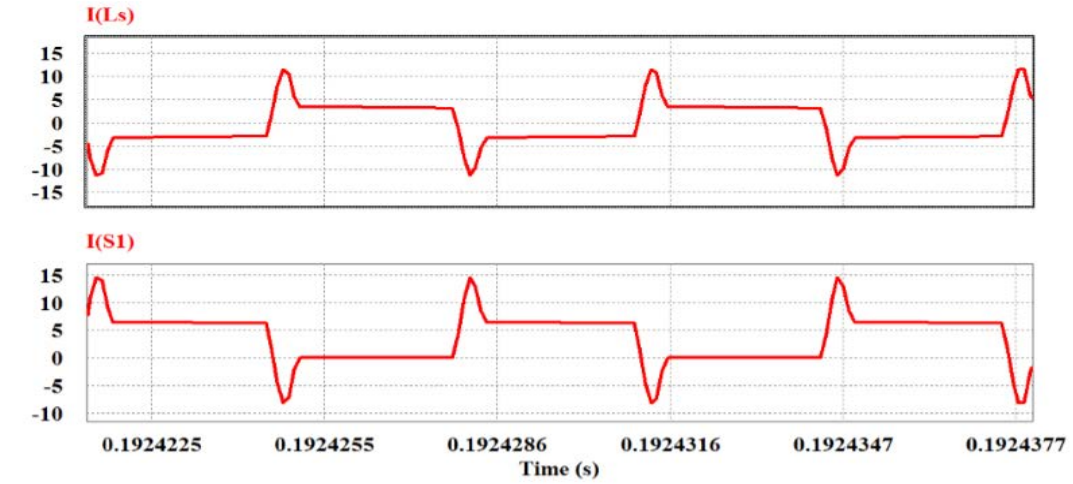
(b)


I(Ls)
15
10
5
0
-5
-10
-15
I(S1)
20
15
10
5
0
-5
-10
0.15
0.2
0.25
0.3
0.35
0.4
Time (s)

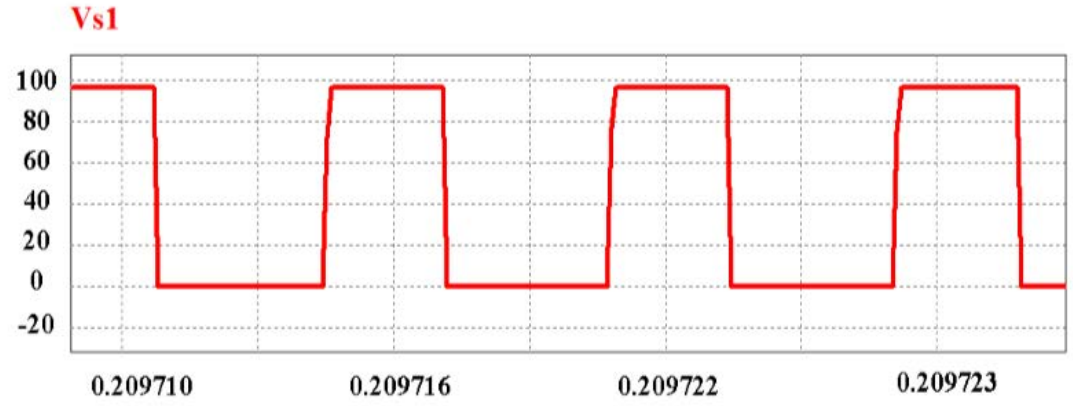
(C)


Vs1
140
120
100
80
60
40
20
0
-20
-40
0.15
0.2
0.25
0.3
0.35
Time (s)

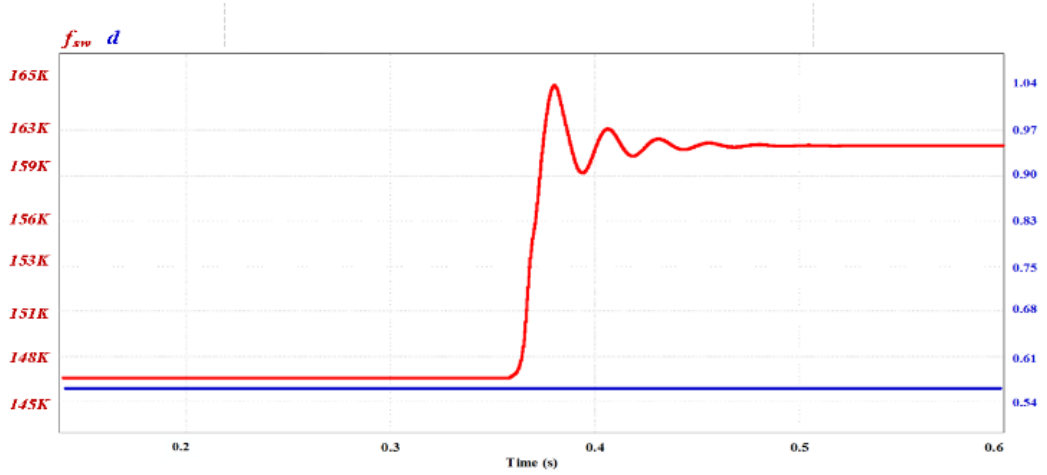
(d)



(e)

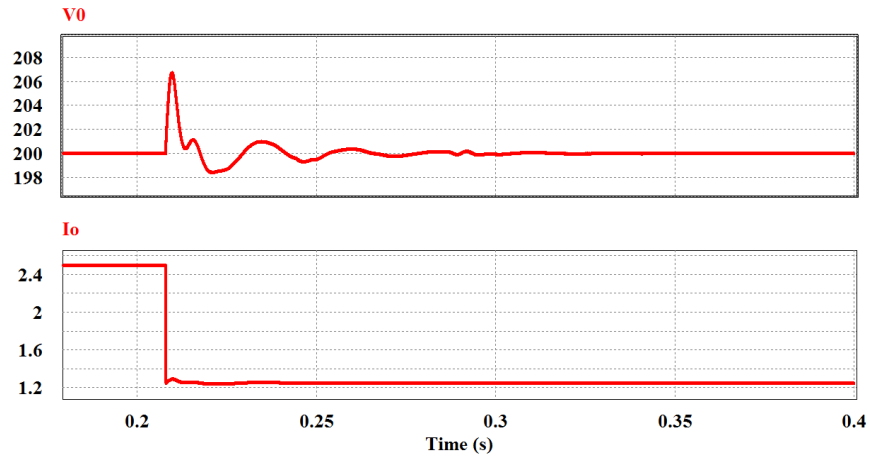


(f)

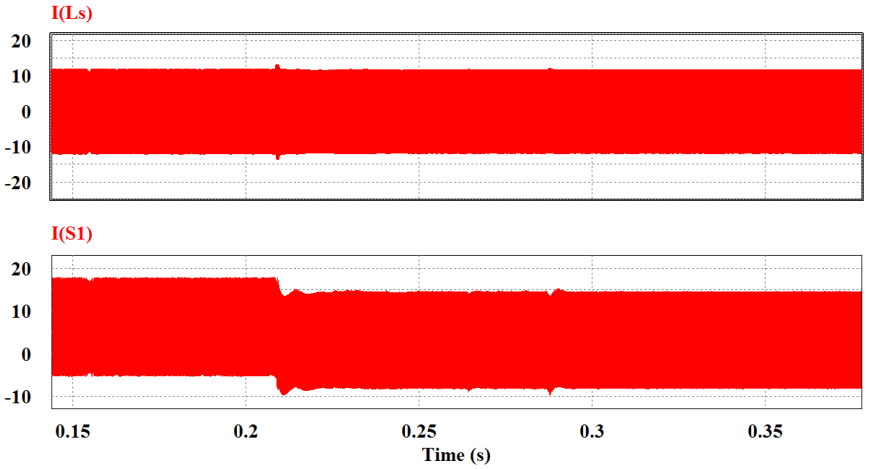


(g)

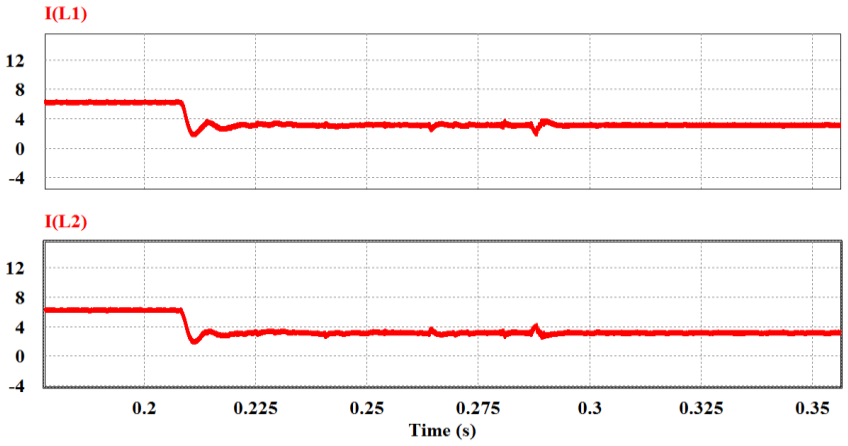
Fig. 4.8. Simulation waveforms for Vin =42V with step change in load from half to full load. v_0 is output, $I_{L1.}$ $I_{L2.}$are boost inductor currents, V_{s1} is switch across voltage,f_{sw} is switching frequency and d is duty cycle.


V0
208
206
204
202
200
198
Io
2.4
2
1.6
1.2
0.2
0.25
0.3
0.35
0.4
Time (s)

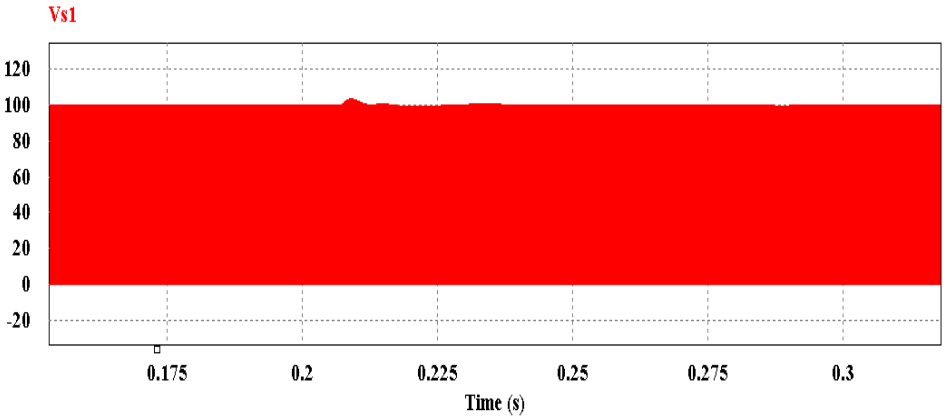
(a)


I(Ls)
20
10
0
-10
-20
I(S1)
20
10
0
-10
0.15
0.2
0.25
0.3
0.35
Time (s)

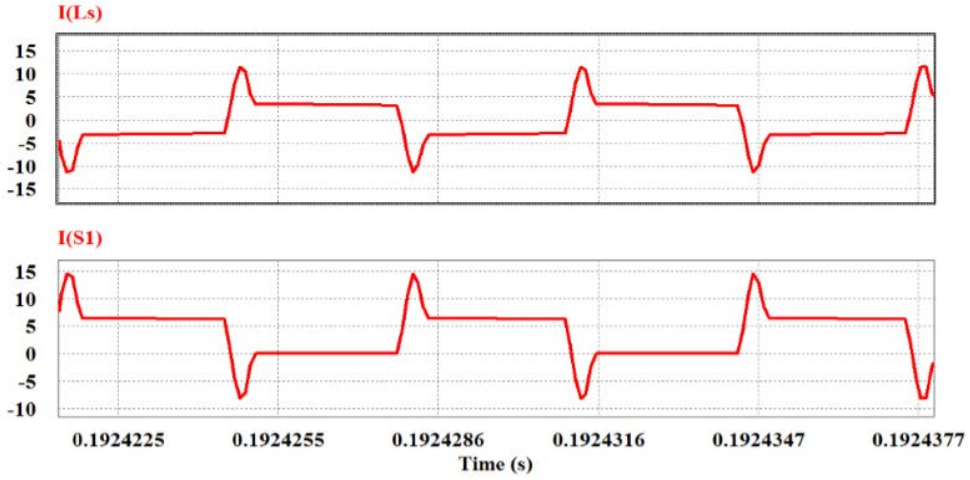
(b)


I(L1)
12
8
4
0
-4
I(L2)
12
8
4
0
-4
0.2
0.225
0.25
0.275
0.3
0.325
0.35
Time (s)

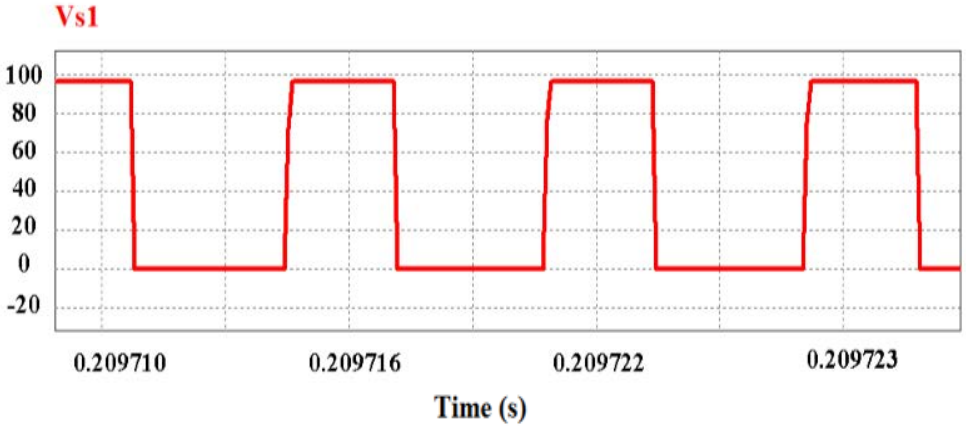
(c).


Vs1
120
100
80
60
40
20
0
-20
0.175
0.2
0.225
0.25
0.275
0.3
Time (s)

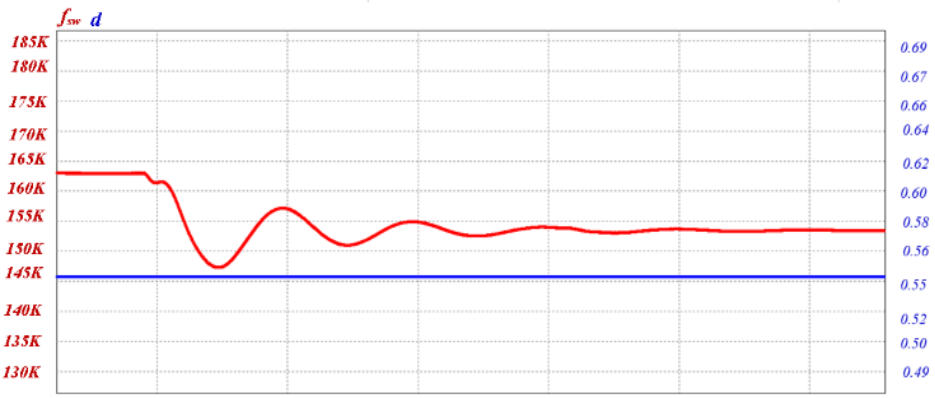
(d)


I(Ls)
15
10
5
0
-5
-10
-15
I(S1)
15
10
5
0
-5
-10
0.1924225
0.1924255
0.1924286
0.1924316
0.1924347
0.1924377
Time (s)

(e)


Vs1
100
80
60
40
20
0
-20
0.209710
0.209716
0.209722
0.209723
Time (s)

(f)



(g)

Fig. 4.9. Simulation waveforms for Vin = 42V with step change in load from rated load to half-load with identical nomenclature.

4.4 Fixed frequency control of partial resonance impulse commutated CFHB dc/dc converter

This section presents detailed small signal modelling, closed loop control of non-isolated impulse commutated parallel LC resonance based half-bridge current-fed dc/dc converter achieving zero current switching (ZCS) of the semiconductor devices by varying duty cycle control for renewable energy conversion applications. The topology attains natural commutation of semiconductors devices. Using state-space averaging, derivation of small signal model of this converter is illustrated. Transfer functions are derived. Two-loop average current controller is designed and implemented on digital signal processor to evaluate and demonstrate the transient performance of the converters. Simulation results using PSIM 11 with the designed controller are shown to validate the stability of the control system. In order to overcome the drawback of a wide range of switching frequency in this parallel resonant converters, fixed frequency pulse-width modulation is introduced to regulate the output voltage at different load conditions. Current-fed voltage doubler can offer 10× voltage gain [46] being transformer less and similarly a non-isolated current-fed voltage quadrupler can offer 20× voltage gain and it offers low source current ripple [47], reducing input filter requirement. Despite of merit, the major fundamental issue with current-fed topologies turn-off voltage spike/overshoot at device commutation and thus requirement of traditional snubber [48-49]. The converter with snubber is complex and not modular. To avoid the historical complexity of snubber, naturally commutated topology is proposed which clamp the device

voltage by creating resonance impulse using an inductance and capacitance circuit achieves zero current switching (ZCS) of semiconductor devices, Fig 4.1. Soft switching techniques, such as asymmetric pulse-width modulation (PWM) techniques [50]-[51], active-clamping converters [52]-[54] and phase-shift PWM converters [55], have been proposed for the past twenty years to reduce switching losses of MOSFETs and improve efficiency of converter. However, maintaining soft switching of these approaches is limited to specific input voltage ranges or load conditions. Thus, it is difficult to attain zero voltage switching (ZVS) and zero current switching (ZCS) with wide load ranges. Resonant converters in [56]-[60] with variable switching frequency to regulate the output voltage have been proposed with the advantages of zero voltage switching (ZVS) or zero current switching (ZCS) for wide range of input voltage and load current. However resonant converter has wide range of switching frequency at different load conditions. So, at optimal point, designing magnetic components of resonant converters are not easy. It is better that converter attains soft-switching and operates at a duty cycle control instead of varying frequency control. In addition, these circuit also contains low switching losses at high switching frequencies. Switching losses can be minimized by operating these circuits under soft-switching conditions. Detailed steady-state analysis, converter design, and steady-state waveforms of this converter are presented in [50]. However, its small signal analysis, closed loop control design, and transient results are not yet reported. This section presents the small signal modeling, derives the transfer functions and reports a controller design for closed loop operation, voltage regulation and power flow control.

4.4.1 Small Signal Model

In this section, state-space equations for each interval of operation are listed and followed by derivation of small ac model using state-space averaging is derived. Primary switches have identical gating signals with 180º shifted from one another. The duty cycle of primary switches is always kept above 50%. The operation during different intervals in a one-half switching cycle is explained with equivalent circuits shown in Fig. 4.3.

For the analysis, the following assumptions are made: 1) all the components are assumed ideal and lossless; 2) Inductors $L_1$and $L_2$are assumed large so that current through them can be considered constant; 3) Series inductor L_s indicates the leakage inductance of resonant tank; and 4) Magnetizing inductance is very large.

Interval (Fig 4(a); (t_0-t_1): During this interval, Primary switch $S_1$and rectifier diode D_2 is conducting Power is transferred through load to source. Switch $S_1$is blocking the voltage $V_{dc}/2$. Switch S_1 is carrying the entire input current I_{in} while $-I_{in}/2$ flows through series inductor. State equations of this interval are:

$$L_1 \frac{d_{il1}}{d_t} = v_{in} \tag{4.36}$$

$$(L_2 + L_{ls}) \frac{di_{l2}}{dt} = \left(v_{in} - \frac{v_{dc}}{2}\right) \tag{4.37}$$

$$C_o \frac{dv_0}{dt} = \left(I_{in} - \frac{v_o}{R_l}\right) \tag{4.38}$$

Interval (Fig 4(b); (t_2-t_3): Both primary switches conduct in this interval. Reflected output voltage $V_{dc}/2$ appears across the series inductor and i_{ls} starts increasing. It causes current through S_2 start increasing while the current S_1 start decreasing. State equations of interval 1 still hold good.

Interval (Fig 4(c); (t_3-t_4): Capacitors C_1 and C_2 constituting the voltage doubler feed the load. The resonance between L_s and C_p commences. The energy stored in the tank increases. The switch currents i_{s1} and i_{s2} start decreasing and increasing, respectively in a resonant fashion. State equations of this interval:

$$(L_1 + L_{ls}) \frac{di_{l2}}{dt} = (v_{in}) \tag{4.39}$$

$$L_2 \frac{d_{il1}}{d_t} = v_{in} \tag{4.40}$$

$$C_o \frac{dc_p}{dt} = (I_{ls}) \tag{4.41}$$

Interval (Fig 4(d); (t_4-t_5): Due to resonance, current i_{ls}rises above $I_{in}/2$. This additional current flows through the body- diode of S_1 leading to ZCS turn-off of switch S_1.State equations of interval 3 still hold good.

Interval (Fig 4(e); (t_5-t_6): During this interval constant current $I_n/2$ flows through L_s and charges the parallel capacitor C_p. Input current flows through the switch S_2. State equations of interval 3 still hold good.

Identically, state equations for the other half cycle can also be derived. State equations are averaged over a HF cycle, state variable $\boldsymbol{I_{ls}}$ can be neglected in the small signal relation between V_{in}, d and V_o.

So, the state variable i_{Ls} is omitted for the following analysis.

Define: $d_1T_s = t_2\text{-}t_1$, $d_2T_s = t_3\text{-}t_2$, $d_3T_s = t_4\text{-}t_3$, $d_4T_s = t_5\text{-}t_4$, $d_5T_s = t_6\text{-}t_5$, $d_6T_s = t_7\text{-}t_6$, $d_7T_s = t_8\text{-}t_7$, $d_8T_s = = t_9\text{-}t_8$, $d_9T_s = t_{10}\text{-}t_9$, $d_{10}T_s = t_1\text{-}t_{10}$.

The averaged state equations of defined state variables over a HF cycle are given:

$$L_1 \frac{di_{l1}}{d_t} = 2v_{in} - \frac{v_o}{2}(d_{s1} + d_{s2}) \tag{4.42}$$

$$L_2 \frac{di_{l1}}{d_t} = 2v_{in} - \frac{v_o}{2}(d_{s1} + d_{s2}) \tag{4.43}$$

$$C_o \frac{dc_o}{dt} = i_{average} - \frac{2v_0}{R_L} \tag{4.44}$$

Where $i_{average}$ is the average current feeding the output capacitor and load from secondary side H-bridge switches and is given by (4.45),

$$i_{average} = \frac{I_{in}}{2}(d_{s1} + d_{s2}) \tag{4.45}$$

On Substituting (4.45) in (4.44),

$$C_o \frac{dc_0}{dt} = \frac{I_{in}}{2}(d_{s1} + d_{s2}) - \frac{2v_0}{R_L} \tag{4.46}$$

The duty ratio of the main switches including conduction of the reverse anti-parallel diodes are defined as,

$$d = d_{s1} = d_1 + d_2 + d_3 + d_4 + d_5 + d_{11} \tag{4.47}$$

$$d = d_{s2} = d_2 + d_3 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 + d_{10} \tag{4.48}$$

Introducing perturbation in state variables such that $i_{L1} = I_{L1} + \hat{\imath}_{L1}$,$i_{L2} = I_{L2} + \hat{\imath}_{L2,} v_{in} = V_{in} + \hat{v}_{in}$,$v_o = V_o + \hat{v}_o$, $f_{s1} = F + \hat{s}_1$, $f_{s2} = F + \hat{f}_{s2}$

For achieving dynamic model of the converter, perturbations are introduced in state variables,

$$L_1 \frac{(I_{L1} + \hat{\imath}_{L1})}{d_t} = (V_{in} + \hat{v}_{in}) - (1 - D - \hat{d}_{s1}) \left(\frac{V_o + \hat{v}_o}{2}\right) \tag{4.49}$$

$$L_2 \frac{(I_{L2} + \hat{\imath}_{L2})}{d_t} = (V_{in} + \hat{v}_{in}) - (1 - D - \hat{d}_{s2}) \left(\frac{V_o + \hat{v}_o}{2}\right) \tag{4.50}$$

$$C_o \frac{d(V_o + \hat{v}_o)}{dt} = \hat{\imath}_{L1}(1 - D - \hat{d}_{s1}) + \hat{\imath}_{L2}(1 - D - \hat{d}_{s2}) - \left(\frac{V_o + \hat{v}_o}{R_L}\right) \tag{4.51}$$

Neglecting the second order terms and steady state or dc terms, results in the following equations.

$$L_1 \frac{d\hat{\imath}_{L1}}{dt} = \hat{v}_{in} - (1 - D)\frac{\hat{v}_o}{2} + \hat{d}_{s1}\frac{V_o}{2} \tag{4.52}$$

$$L_2 \frac{d\hat{\imath}_{L1}}{dt} = \hat{v}_{in} - (1-D)\frac{\hat{v}_o}{2} + \hat{d}_{s2}\frac{V_o}{2} \tag{4.53}$$

$$C_o \frac{d\hat{v}_o}{dt} = (1-D)\hat{\imath}_{L1} + (1-D)\hat{\imath}_{L2} - I_{L1}\hat{d}_{s1} - I_{L2}\hat{d}_{s2} - \frac{\hat{v}_o}{R_L} \tag{4.54}$$

In Laplace domain, the results in-

$$sL_1\hat{\imath}_{L1}(s) + \frac{(1-D)\hat{v}_o(s)}{2} = \frac{V_o}{2}\hat{d}_{s1} + \hat{v}_{in}(s) \tag{4.55}$$

$$sL_2\hat{\imath}_{L2}(s) + \frac{(1-D)\hat{v}_o(s)}{2} = \frac{V_o}{2}\hat{d}_{s2} + \hat{v}_{in}(s) \tag{4.56}$$

$$(1-D)\hat{\imath}_{L1}(s) + (1-D)\hat{\imath}_{L2}(s) - \left(SC_o + \frac{1}{R_L}\right)\hat{v}_o(s) = I_{L1}\hat{d}_{s1} - I_{L1}\hat{d}_{s1} \tag{4.57}$$

Writing in matrix,

$$\begin{bmatrix}\hat{\imath}_{L1}(s)\\ \hat{\imath}_{L2}(s)\\ \hat{v}_o(s)\end{bmatrix} = [K(s)].\begin{bmatrix}\frac{V_o}{2}\\ 0\\ I_{L1}\end{bmatrix}.\hat{d}_{s1}(s) + [K(s)].\begin{bmatrix}0\\ \frac{V_o}{2}\\ \frac{V_o}{2}\end{bmatrix}.\hat{d}_{s2}(s) + [K(s)].\begin{bmatrix}1\\ 1\\ 0\end{bmatrix}.\hat{v}_{in}(s) \tag{4.58}$$

Where,

$$K(s) = \begin{matrix} SL_1 & 0 & \frac{(1-D)}{2} \\ 0 & SL_2 & \frac{(1-D)}{2} \\ \frac{(1-D)}{2} & \frac{(1-D)}{2} & -\left(sC_o + \frac{1}{R}\right)\end{matrix}^{-1} \tag{4.59}$$

$$sL\left(\hat{\imath}_{L1}(s) + \hat{\imath}_{L2}(s)\right) + \left(\hat{v}_O(s)(1-D)\right) = \frac{V_o}{2}\left(\hat{d}_{s1}(s) + \hat{d}_{s2}(s)\right) + 2\hat{v}_{in}(s) \tag{4.60}$$

Writing in matrix,

$$\begin{bmatrix}\hat{\imath}_{L1}(s) + \hat{\imath}_{L2}(s)\\ \hat{v}_o(s)\end{bmatrix} = [K(s)].\begin{bmatrix}\frac{v_o}{2}\\ I_L\end{bmatrix}\left(\hat{d}_{s1}(s) + \hat{d}_{s2}(s)\right) + [K(s)].\begin{bmatrix}2\\ 0\end{bmatrix}\hat{v}_{in}(s) \tag{4.71}$$

Where,

$$K(s) = \begin{bmatrix} SL & (1-D) \\ (1-D) & -\left(sC_o + \frac{1}{R}\right)\end{bmatrix}^{-1} \tag{4.72}$$

Control-to-output transfer function is given by setting $\hat{v}_{in} = 0$ in (4.71)

$$\frac{\hat{v}_o(s)}{\hat{d}_{s1}(s)+\hat{d}_{s2}(s)} = \frac{(1-D)V_o - (SLI_L)}{(LC_o)s^2 + \frac{L}{R_L}s + ((1-D)^2)} \tag{4.73}$$

4.4.2 Two-Loop Average Current Control Design

Table 4.2: Specifications to design the control system of following converter

Input voltageV_{in}	42V
Output VoltageV_o	200V
Peak output powerP_o	500W
Switching frequency of converter f_s	100 kHz
Leakage inductorL_{ls}	1.96µH,
Input Boost Inductor L	400µH,
Output CapacitorC_O	100µF
Full-loadR_L	80Ω.

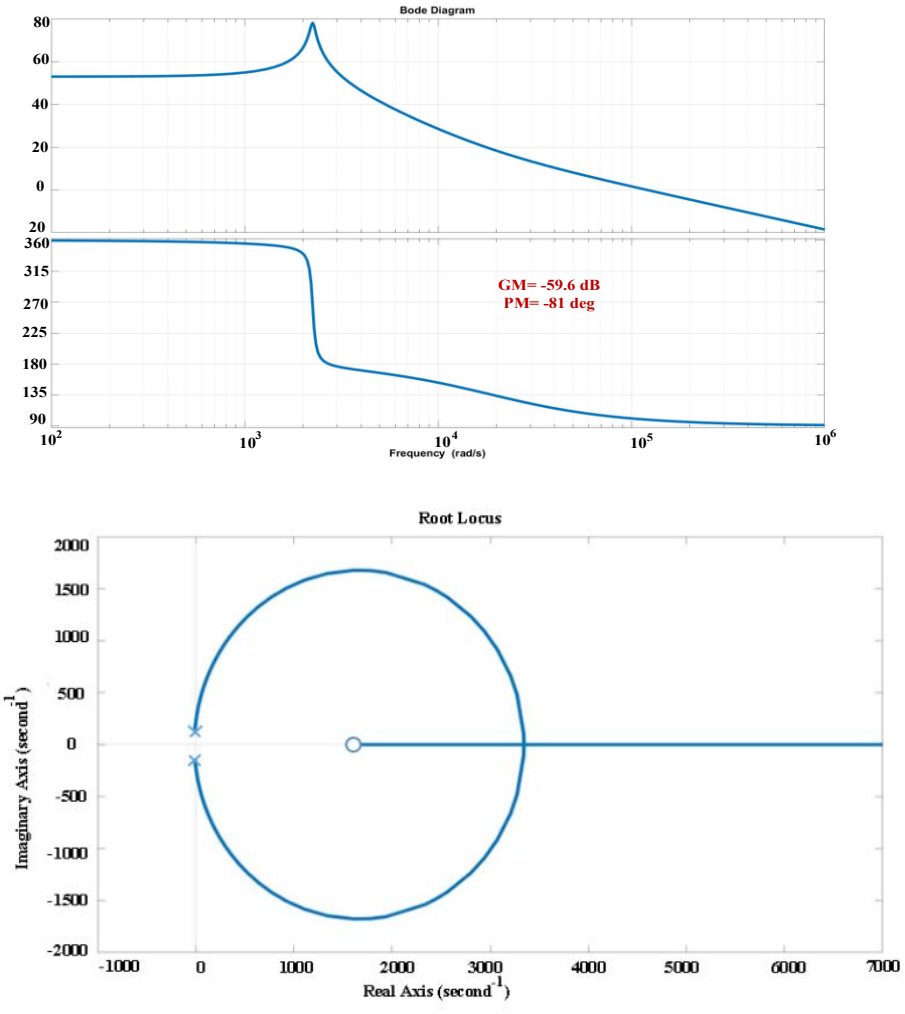


Fig. 4.11. Pole-zero map of Control to output voltage transfer function of the system without controller.

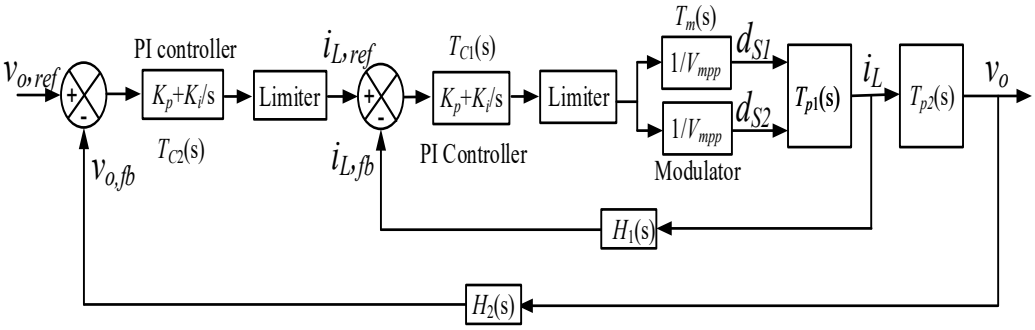


Fig 4.12. Two-loop control system

Fig. 4.10 shows the bode plot of plant transfer function. It can be easily found that phase margin (PM) is -81 degree and gain margin is -59.6 dB which demonstrates the whole is system is not stable.

Fig. 4.11 clearly shows that, this transfer faction has right half plane zero which adds negative phase to the system. Instead phase increasing from 0 to 90 degrees, its phase increases from 0 to -90 degrees. This causes delay in system response which can lead to instability if not taken care.

Fig. 4.12 illustrates two-loop average current control design, using 2 PI controller having fixed duty cycle but variable frequency modulation control with phase shift of 180^0 [40-41]. Outer loop regulates the load voltage by producing the reference values for the input inductor currents, Inductor currents are controlled by controlling the frequency of the devices.

4.4.2.1 Designing of Current Control Loop:

Fig. 4.13 shows the schematic diagram of the inner current control loop. For generating the gating signals, output of the PI controller is sent to the modulator. Then by adjusting the duty ratio of switches, inductor currents I_L is controlled.

Duty to the inductor current transfer function is given by,

$$T_{p1} = \frac{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)}{\hat{d}_{s1}(s)+\hat{d}_{s2}(s)} = \frac{\left(\frac{C_O V_O}{2}\right)s+\frac{V_O}{2R_L}+2(1-D)I_L}{(LC_O)s^2+\frac{L}{R_L}s+(1-D)^2} \quad (4.74)$$

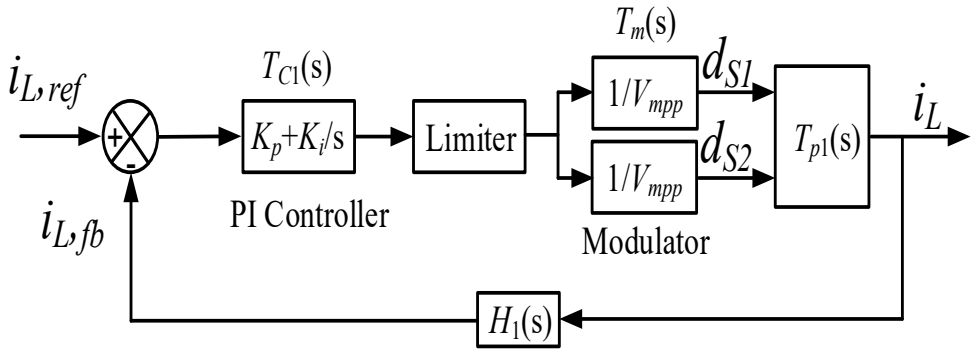


Fig. 4.13. Inner current control loop schematic diagram

For the given specifications, the duty-to-inductor current transfer function is given by,

$$T_{p1} = \frac{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)}{\hat{d}_{s1}(s)+\hat{d}_{s2}(s)} = \frac{0.005s+11.96}{2.38*10^{-8}s^2+5.95*10^{-6}s+0.2025} \quad (4.75)$$

The gain margin and phase margin of current control loop without controller shows of PM= 89.4^0at $2.1 * 10^5$rad /s. The controller is designed to achieve PM of 60^0[20-21]at selected cross over frequency f_c=15.92 kHz or $\omega_c = 100$krad/sec.Thus a PI controller is designed to increase the low frequency gain, to reduce the steady-state error between the desired and actual inductor current and to achieve stability over a certain range. Transfer function of a PI controller $T_{c1}(s)$ is given by, (4.76). Transfer function of the current loop is given by (4.77), where $H_1(s)$ is the current feedback gain and $T_m(s)$ is the overall gain of the modulator. Here current feedback gain is selected as $H_1(s)$ =1.

$$T_{c1}(s) = K_p + \frac{K_i}{s} = \frac{K_p(s+K_i/K_p)}{s} \quad (4.76)$$

Open loop transfer function of the current loop is given by,

$$T_{OL1}(s) = T_{C1}(s).T_m(s)T_{p1}(s)H_1(s) \quad (4.77)$$

So, current loop transfer function is given by,

$$T_{OL1}(s) = \frac{0.005s+11.96K_p\left(s+\frac{K_i}{K_p}\right)}{2.38*10^{-8}s^2+5.95*10^{-6}s+0.2025} \quad (4.78)$$

For the given specifications, To obtain PM of 60º at 15.92 kHz (100krad/s) at gain crossover frequency, based on the above procedure, to obtain the calculated parameter values of PI controller are: K_P and K_i as 27.3 and 91000 respectively.

4.4.2.2 Designing of Voltage Control Loop:

Fig. 4.14 shows voltage control loop regulates the load voltage at the desired value by generating reference current value for the input inductors. Voltage loop transfer function is given by (4.82),

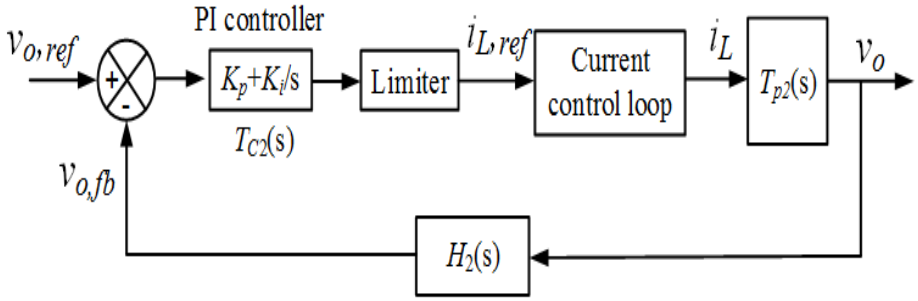


Fig. 4.14. Outer voltage control loop schematic diagram

Where, voltage feedback gain $H_2(s)$ is selected to be 1. Inner current loop is 10 times faster than gain cross over frequency of the voltage controller.

For the given specification, inductor current to output voltage transfer function T_{p2}(s) is given by,

$$T_{p2} = \frac{\hat{v}_o(s)}{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)} = T_{p2}(s) = \frac{v_o(s)}{\hat{\imath}_L(s)} = \frac{(1-D)}{C_o(s+\frac{1}{R_L C_o})} \quad (4.79)$$

The plant transfer function T_{p2} (s) of this loop is obtained as,

$$T_{p2} = \frac{\hat{v}_o(s)}{\hat{\imath}_{L1}(s)+\hat{\imath}_{L2}(s)} = \frac{0.45}{50*10^{-6}s+0.0125} \quad (4.80)$$

Voltage loop transfer function is given by,

$$T_{OL2}(s) = T_{C2}(s).T_m(s)T_{p2}(s)H_2(s) \quad (4.81)$$

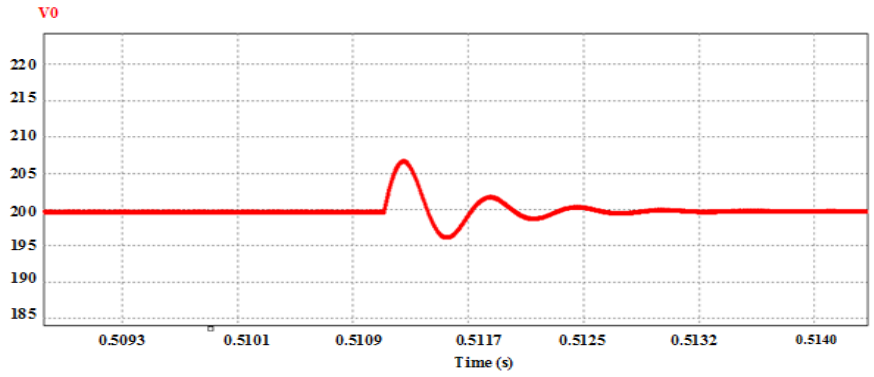
$$T_{OL2}(s) = \frac{0.45K_p(s+K_i/K_p)}{50*10^{-6}s+0.0125} \quad (4.82)$$

where, voltage feedback gain $H_2(s)$is selected to be 1 and PI controller transfer function T_{C2}(s) is given by (4.76).Hence the phase margin should be 60º at the gain crossover frequency of 1.59 kHz (10 krad/s). It results in the gain $K_p$and K_i as 2 and 1666.67, respectively. Considering dynamics of current control loop. Stable system offers positive PM which demonstrates better

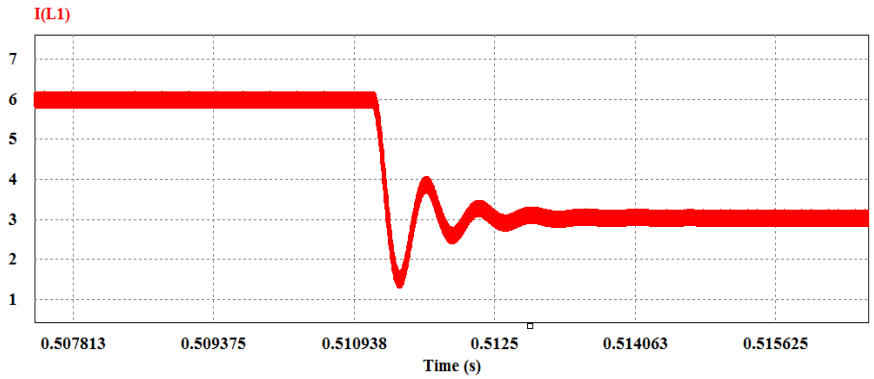
control against disturbances for wide range in source voltage and load current variations. Hence system provides better control and stability over certain range.

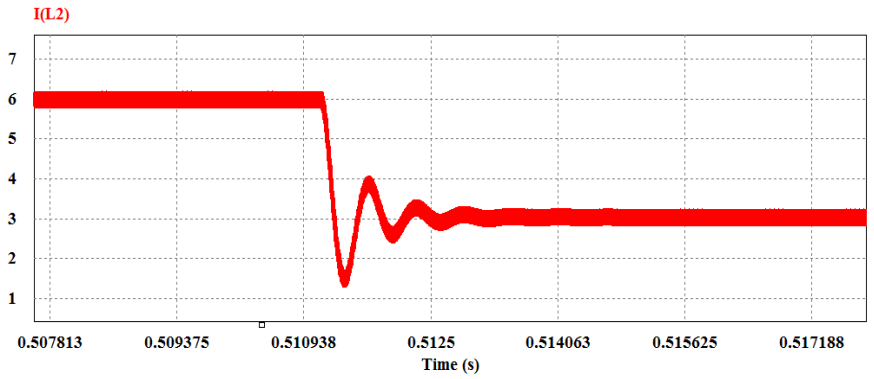
4.5 Simulation Results

Simulation model of this circuit topology and two-loop control was developed on software package PSIM 11.1.65 and was run to capture waveforms and observe transient performance of the converter under load current variations in Fig. 4.15 and Fig. 4.16 for full load to half load and vice-versa, respectively. Transient performance of various load conditions of output voltage is illustrated in Fig 4.15(a) and Fig. 4.15(b), respectively. Negligible overshoot or undershoot in output voltage are observed in transient period. By changing the control parameters, better results can be expected for both step changes in load. Fig 4.15(b) and Fig 4.16(b) illustrate two input inductor currents are adjusted smoothly to next steady state value. Fig 4.15(c) and 4.16(c) shows that transient results of primary switch voltages for step load change where 5V (25%) overshoot is observed in primary switch voltage devices which demonstrate good stability in control. Fig 4.15(e) and 4.15(f) shows steady-state waveforms of leakage inductor current and switch current respectively at full load. Fig 4.16(e) and 4.16(f) show the same waveform but at half load condition. It should be noted ZCS is maintain by the primary devices for both the full load and the half load condition. During transient period inductor currents are oscillated but it settled down very smoothly to the next steady-state value. Settling time is around 6 ms. Settling time can be adjusted by tuning of controller parameters. Similar performance is obtained for step change in load from half load to rated-load as demonstrated in Fig. 4.16. Current through the load, switches, inductors, and transformer are smoothly reaching to the next steady-state without overshoot. Output voltage is quickly regulated with 5V jump. The transient results are satisfactory and the steady state results are as expected. It should be noted that primary side devices maintain ZCS under both conditions.

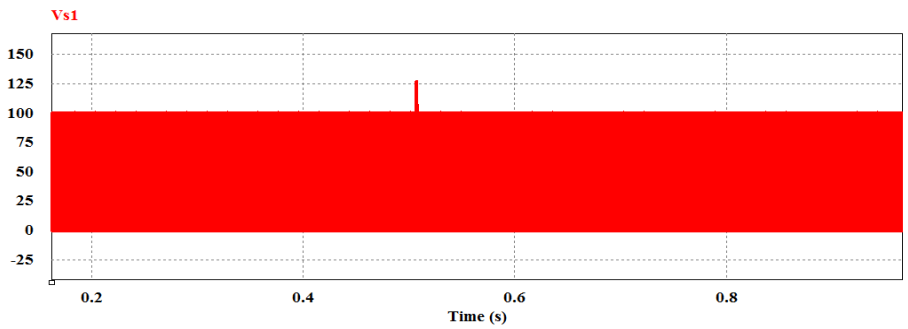

V0
220
215
210
205
200
195
190
185
0.5093
0.5101
0.5109
0.5117
0.5125
0.5132
0.5140
Time (s)

(a)

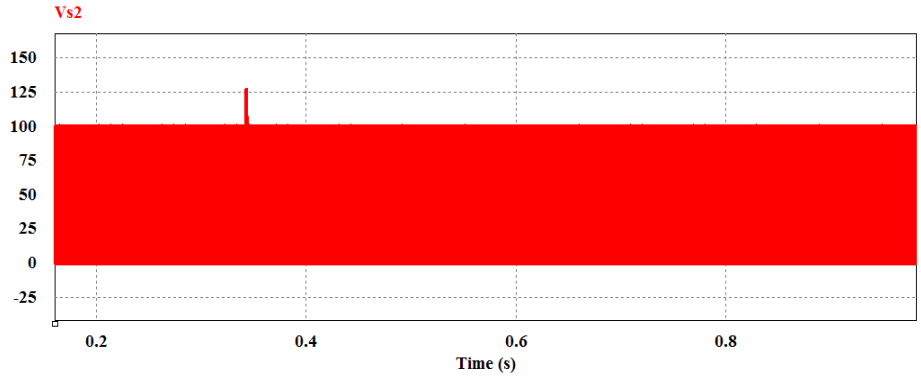

I(L1)
7
6
5
4
3
2
1
0.507813
0.509375
0.510938
0.5125
0.514063
0.515625
Time (s)


I(L2)
7
6
5
4
3
2
1
0.507813
0.509375
0.510938
0.5125
0.514063
0.515625
0.517188
Time (s)

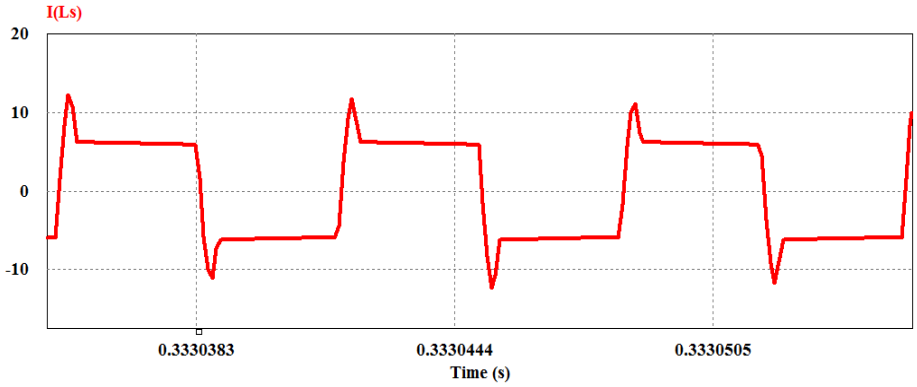
(b)


Vs1
150
125
100
75
50
25
0
-25
0.2
0.4
0.6
0.8
Time (s)

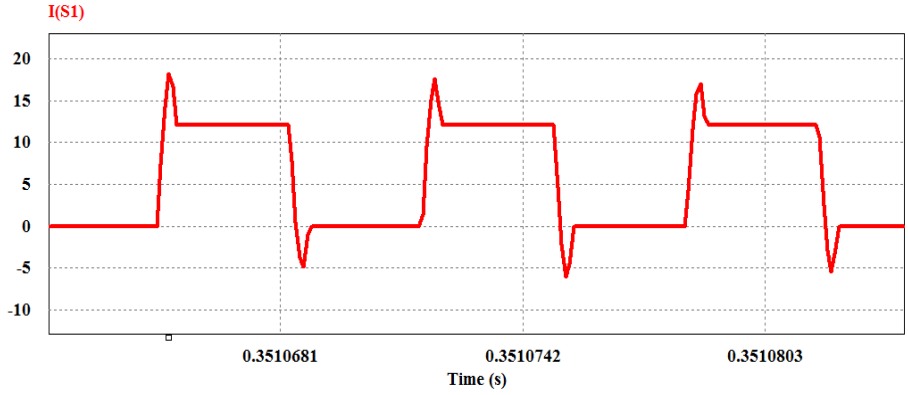
(c)


Vs2
150
125
100
75
50
25
0
-25
0.2
0.4
0.6
0.8
Time (s)

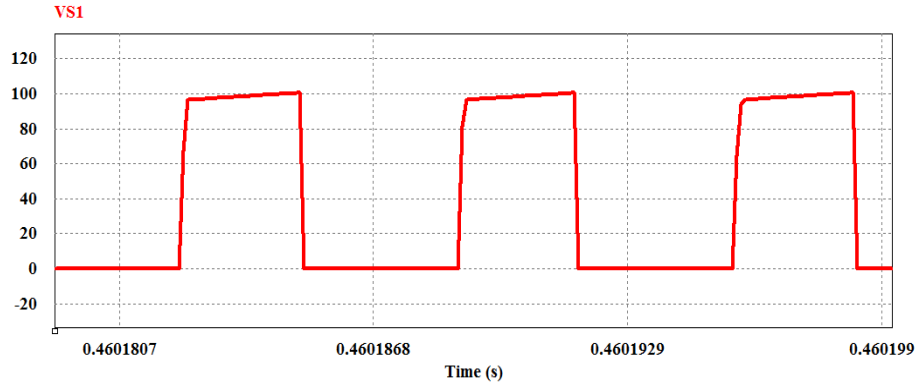
(d)


I(Ls)
20
10
0
-10
0.3330383
0.3330444
0.3330505
Time (s)

(e)

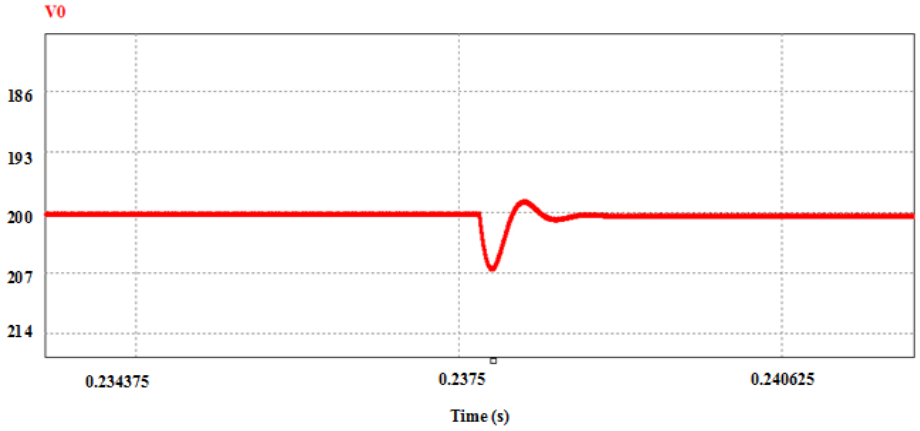

I(S1)
20
15
10
5
0
-5
-10
0.3510681
0.3510742
0.3510803
Time (s)

(f)

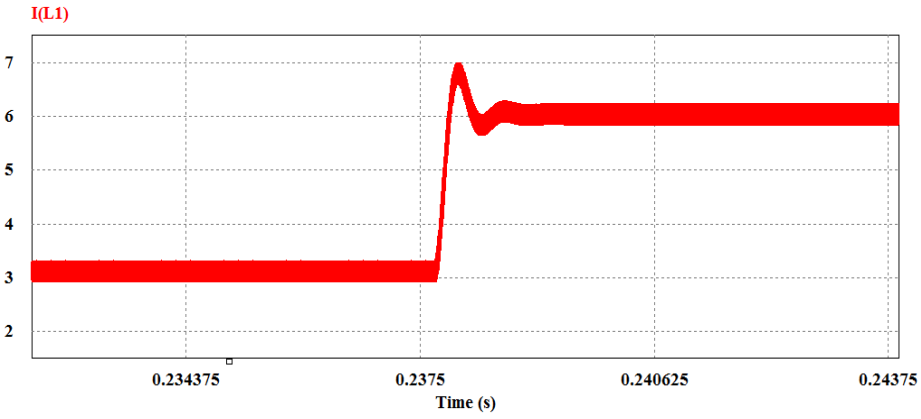


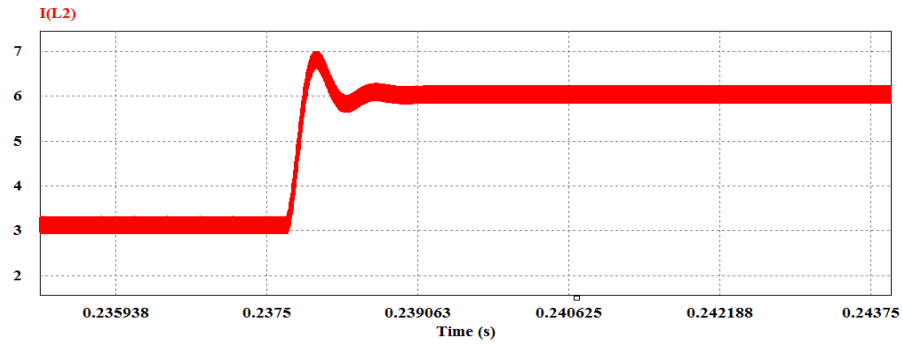
(g)

Fig. 4.15. Simulation waveforms for Vin =42V with step change in load from full to half load. v_0 is output , $I_{L1.}$ $I_{L2.}$ is boost inductor currents, , V_{s1}, V_{s2} are switch across voltages, I_{s1} is Primary switch current

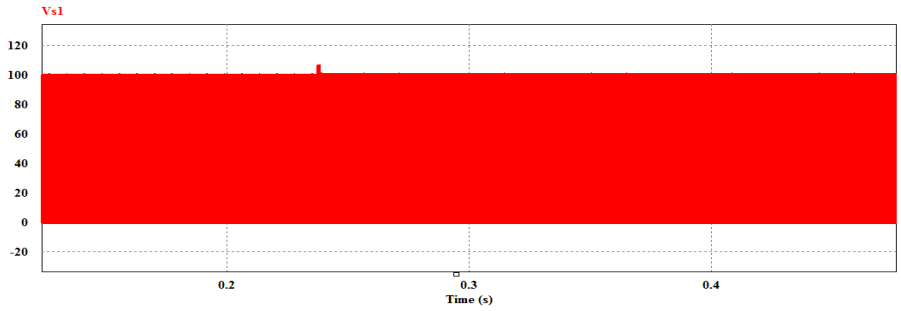


(a)

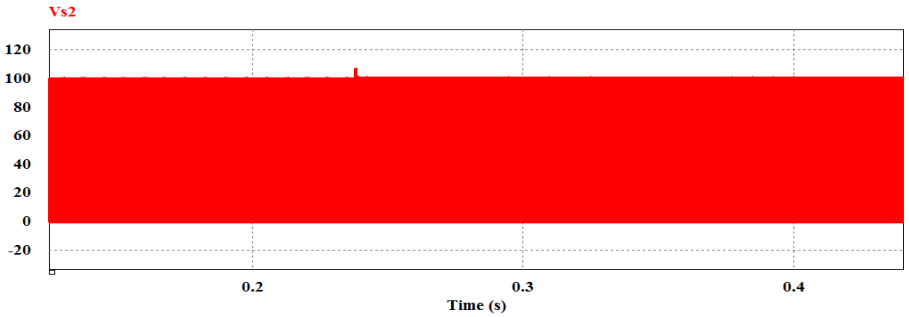



I(L2)
7
6
5
4
3
2
0.235938
0.2375
0.239063
0.240625
0.242188
0.24375
Time (s)

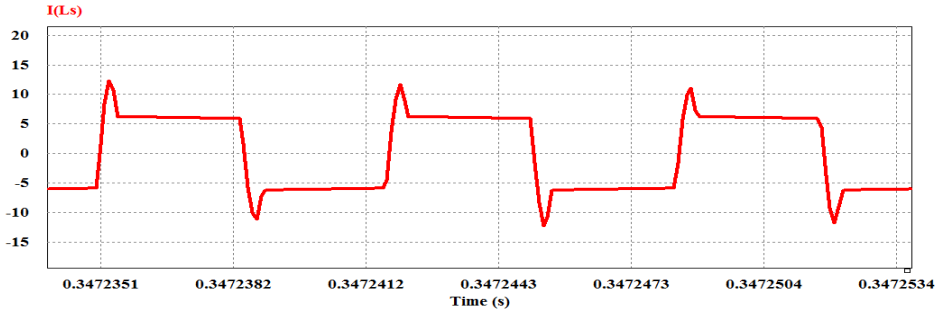
(b)


Vs1
120
100
80
60
40
20
0
-20
0.2
0.3
0.4
Time (s)

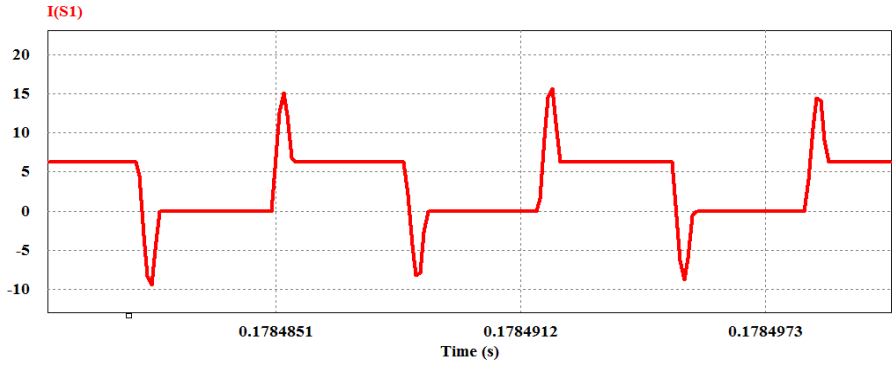
(c)


Vs2
120
100
80
60
40
20
0
-20
0.2
0.3
0.4
Time (s)

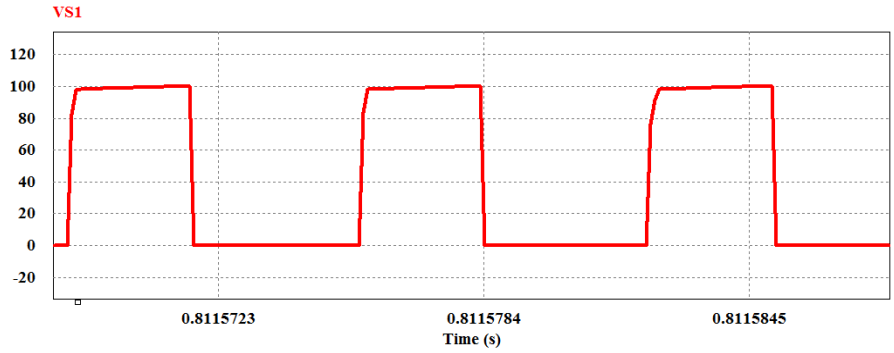
(d)


I(Ls)
20
15
10
5
0
-5
-10
-15
0.3472351
0.3472382
0.3472412
0.3472443
0.3472473
0.3472504
0.3472534
Time (s)

(e)



(f)



(g)

Fig. 4.16. Simulation waveforms for Vin =42V with step change in load from half to full load. v_0 is output, $I_{L1.}$ $I_{L2.}$ is boost inductor currents, , V_{s1}, V_{s2} are switch across voltages, I_{s1} is Primary switch current.

4.6 Conclusion

In this Chapter, detailed small signal analysis of the partial resonant CFHB dc/dc converter is reported for variable frequency control and fixed frequency control. State space averaging technique is followed to systematically derive the small signal model of the converter. Two-loop average current control methodology is followed using variable frequency modulation and duty cycle modulation at fixed frequency to design a closed loop control system using 2 PI controllers to meet the frequency response requirements and obtain stable response during load disturbances and transients. Simulation results have been presented for both the cases to verify the controller design and investigate the initial transient performance of the converter.

Chapter 5

Conclusions and Scope for Future Work

5.1 Introduction

This Chapter summarizes the main contributions and summary of the results of this thesis along with recommendations for the future work. The contributions are outlined in Section 5.2. The recommendation for the future work is reported in Section 5.3.

5.2 Major Contributions

This thesis is focused on the closed loop performance and the transient results of the snubberless naturally commutated soft-switching current-fed half-bridge and push-pull dc-dc converter topologies. This class of current-fed topologies utilizes a unique modulation to clamp the voltage across the semiconductor devices at their turn-off without requiring any additional snubber circuit. The thesis contributes to the following:

1. Detailed small signal analysis and control of the snubberless current-fed half-bridge dc/dc converter has been presented in Chapter 2 using state-space averaging technique. Small signal model and the transfer functions have been derived. A two-loop average current control is designed, and the dynamic performance of the converter has been demonstrated through simulation and hardware experimentation.
2. Detailed small signal analysis and control of the snubberless current-fed push-pull dc/dc converter has been presented in Chapter 3 using state-space averaging technique. Small signal model and the transfer functions have been derived. A two-loop average current control is designed, and the dynamic performance of the converter has been demonstrated through simulation and hardware experimentation.
3. Detailed small signal analysis and control of the partial resonance current-fed half bridge dc/dc converter has been presented in Chapter 4 using state-space averaging technique. The two loop average current control is designed. Simulation results using PSIM 11 with the designed controller of variable frequency control and fixed frequency control of this converter are shown to validate the stability of the control system and demonstrate the dynamic performance of converter.

5.3 Future work

In Chapter 4, small signal analysis and the transfer functions, for the closed loop operation for voltage regulation and power flow control of this converter are reported. A complete design procedure is presented. Simulation results using PSIM 11 with for the variable frequency control and the fixed frequency control of partial resonance impulse commutated current-fed half-bridge topology are shown to validate the stability of the control system. Experimental results are not demonstrated in this chapter. Hardware prototype development along with variable and fixed frequency control implementation are the potential future work to verify the control and transient performance of this converter and other similarly for the full-bridge and push-pull isolated topologies.

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List of Publications

Journals

1. K. Khatun, V. R. Vakacharla, A. R. Kizhakkan and A. K. Rathore, "Small Signal Analysis and Control of Snubberless Naturally-Clamped Soft-Switching Current-Fed Push-Pull DC/DC Converter," in IEEE Transactions on Industry Applications, doi: 10.1109/TIA.2020.2995561.

2. Koyelia Khatun, Venkata R Vakacharla, Akshay K Rathore “Small Signal Modeling, Closed Loop Design, and Transient Results of Snubberless Naturally-Clamped Soft-Switching Current-Fed Half-bridge DC/DC Converter.” (submitted)

Conferences

1. Koyelia Khatun and Akshay Kumar Rathore, “Small Signal Modeling, Closed Loop Design, and Transient Results of Snubberless Naturally-Clamped Soft-Switching Current-Fed Half-bridge DC/DC Converter,” in I*EEE International Symposium on Industrial Electronics (ISIE) 2019*, 12-14 June 2019, Vancouver, BC, Canada, pp 2571-2576. DOI: 10.1109/ISIE.2019.8781406.
2. Koyelia Khatun, Akhil Raj Khizakkan, Venkata Ratnam Vakacharla, and Akshay Kumar Rathore, “Small Signal Analysis and Closed Loop Fixed-Frequency Control of Snubberless Naturally-Clamped Soft-Switching Current-Fed Push-Pull DC/DC Converter,” in *IEEE Industry Applications Society (IAS) Annual Meeting 2019*, 29 Sept-3 Oct, Baltimore, MD, USA. DOI: 10.1109/IAS.2019.8911986.

3. V. R. Vakacharla, K. Khatun and A. K. Rathore, "Mixed Domain Model to Mimic Current-fed LCC-T Resonant Converter," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, Cochin, India, 2020, pp. 1-3, doi: 10.1109/PESGRE45664.2020.9070511.

4. Koyelia Khatun, Venkata Ratnam and Akshay Kumar Rathore “Small Signal Analysis of Variable Frequency Modulated Non-isolated Current-fed Parallel LC Resonance Impulse Commutated DC-DC Converter” to 2020 IEEE Transportation Electrification Conference (Accepted).

Book Chapter

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