Single-Sensor DCM PFC Based Onboard Chargers for Low Voltage Electric Vehicles

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ABSTRACT

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Karan Pande

Grid-connected plug-in electric vehicles (PEVs) are considered as one of the most sustainable solutions to substantially reduce both the oil consumption and greenhouse gas emissions. Electric vehicles (EVs) are broadly categorized into low power EVs (48/72 V battery) and high power EVs (450/650 V battery). Low power EVs comprise two-wheelers, three-wheelers (rickshaws), golf carts, intra-logistics equipment and short-range EVs whereas high power EVs consist of passenger cars, trucks and electric buses. Charger, which is a power electronic converter, is an important component of EV infrastructures. These chargers consist of power converters to convert AC voltage (grid) to constant DC voltage (battery). The existing chargers are bulky, have high components' count, complex control system and poor input power quality. Henceforth, to overcome these drawbacks, this thesis focuses on the onboard charging solutions (two-stage isolated and single-stage non-isolated) for the low voltage battery EVs. Power factor correction (PFC) is the fundamental component in the EV charger. Considering the specific boundaries of the continuous conduction mode (CCM) operation for AC-DC power conversion and their complexity, the proposed chargers are designed to operate in discontinuous conduction mode (DCM) and benefiting from the characteristics like built-in PFC, single sensor, simple control, easy implementation, inherent zero-current turn-on of the switches, and inherent zero diode reverse recovery losses. Proposed converters can operate for the wide input voltage range and the output voltage is controlled by a single sensor-based single voltage control loop making the control simple and easy to implement, and improves the system reliability and robustness.

This thesis studies and designs both single-stage non-isolated and two-stage isolated onboard battery chargers to charge a 48 V lead-acid battery pack. At first, a non-isolated single-stage single-cell buck-boost PFC AC-DC converter is studied and analyzed that offers reduced components' count and is cost-effective, compact in size and illustrates high efficiency. While the DCM operation ensures unity power factor (UPF) operation at AC mains

without the use of input voltage and current sensors. However, they employ high current rated semiconductor devices and the use of diode bridge rectifier suffers from higher conduction losses. To overcome these issues, a new front-end bridgeless AC-DC PFC topology is proposed and analyzed. With this new bridgeless front-end topology, the conduction losses are significantly reduced resulting in improved efficiency. The low voltage stress on the semiconductor devices are observed because of the voltage doubler configuration. Later, an isolated two-stage topology is proposed. The previously proposed bridgeless buck-boost derived PFC converter is employed followed by an isolated half-bridge LLC resonant converter. Loss analysis is done to determine optimal DC-link voltage for the efficient operation of the proposed conversion. The converters' steady-state operation, DCM condition, and design equations are reported in detail. The small-signal models for all the proposed topologies using the average current injected equivalent circuit approach are developed, and detailed closed-loop controller design is illustrated. The simulation results from PSIM 11.1 software and the experimental results from proof-of-concept laboratory hardware prototypes are provided in order to validate the reported analysis, design, and performance.

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List of Abbreviations

EVs	Electric Vehicles
PHEV	Plug-in Hybrid Electric Vehicle
OBCs	On-board Battery Charger
BMS	Battery Management System
PFC	Power Factor Correction (or Corrected)
THD	Total Harmonic Distortion
EMI	Electromagnetic Interference
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
AC	Alternating Current
DC	Direct Current
LLC	Inductor-Inductor-Capacitor
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
UPF	Unity Power Factor
kW	Kilo-Watt
CC	Constant Current
CV	Constant Voltage
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
CIECA	Current Injected Equivalent Circuit Approach
RMS	Root Mean Square
ms	Millisecond
PF	Power Factor
FFT	Fast Fourier Transform
G2V	Grid to Vehicle
V2G	Vehicle to Grid

List of Symbols

V_{in}	Input Voltage
V_o	Output Voltage
V_{1r}	Rectified Input Voltage
L	Buck-Boost Inductor
DT_s	Switch On-Time
D	Duty Cycle
$I_{O,Avg}$	Output Average Current
$I_{in}\ and\ I_1$	Input Current
M	Buck-Boost Converter Gain
K_{cond}	Conduction Parameter of Converter
K_{cric}	Critical Conduction Parameter
$V_{o,ripple}$	Output Voltage Ripple
C_o, C_{o1}, C_{o2}	Output Capacitors
L_f	Input Filter Inductor
C_f	Input Filter Capacitor
f_s	Switching Frequency
$i_{o,avg}$	Switching cycle average output current
$R_L\ and\ R$	Load Resistance
P_o	Converter Output Power
V_{pk}	Peak Input Voltage
$i_{L,pk}$	Peak Inductor Current
I_{pk}	Peak Input Current
f_c	Cut-Off Frequency
Z_{in}	Input Impedance
f_o	Resonant Frequency
$V_{dc,link}$	DC-link voltage
$1:n:n$	Transformer turns ratio

$I_{sw,rms}$	Switch rms current
$R_{DS,on,FE}$	Switch drain-to-source on resistance (front end)
$P_{c,limit}$	Inductor core loss limit, mW/cm^3
V_e	Effective core volume, cm^3
V_f	Buck-boost diode forward voltage
R_d	Buck-boost diode resistance
$I_{C_{dc,link},rms}$	DC-link capacitor rms current
$R_{C_{dc,link}ESR}$	DC-link capacitor ESR
R_L	Load resistance
L_m	Transformer magnetizing inductance
V_g	Applied gate voltage
T_{dead}	Dead-time for back-end switches
L_r	Resonant inductor
L_{lk}	Transformer leakage inductance
$C_{r_1} = C_{r_2}$	Resonant capacitor
$V_{in,pk}\sin(\omega t)$	Line input voltage
C_{oss}	Switch output capacitance
$I_{o,BB}$	Buck-boost average output current
$I_{sw_k,rms;k=BE,SR}$	Back-end switch current
$T_{sw_{kB,k=BE}}$	Switching time period of buck-boost or half-bridge converter

CHAPTER 1: INTRODUCTION

1.1 Introduction

The automotive industry globally is witnessing a major transformation due to research and development on transportation electrification. Growing concerns for the environment and energy security clubbed with rapid advancements in technologies for the powertrain electrification are transforming the automotive business. One of the key facets of such a change is the rapid development in the field of electric mobility which might transform the automotive industry like never before. Electric vehicles (EVs) for the road transport enhances the energy efficiency, require no direct fuel combustion and rely on electricity – the most diversified energy carrier, thereby contributing to a wide range of transport policy goals. Global EV sales figures have been growing rapidly and according to an analysts, the global feet of EV sales could rise to 120 million in 2030 [1]. At the end of 2019, the global fleet of plug-ins was 7.5 million counting the light vehicles [2]. Medium and heavy commercial vehicles add another 700,000 units to the global stock of plug-in vehicles [3]. EVs comprise a broad spectrum of vehicles right from two-wheelers, three-wheelers (rickshaws), golf carts, intra-logistics equipment, passenger cars, trucks and electric buses. Fig. 1.1 illustrates the classification of EVs depending upon their battery capacity whereas, Table 1. 1 shows EV charging type

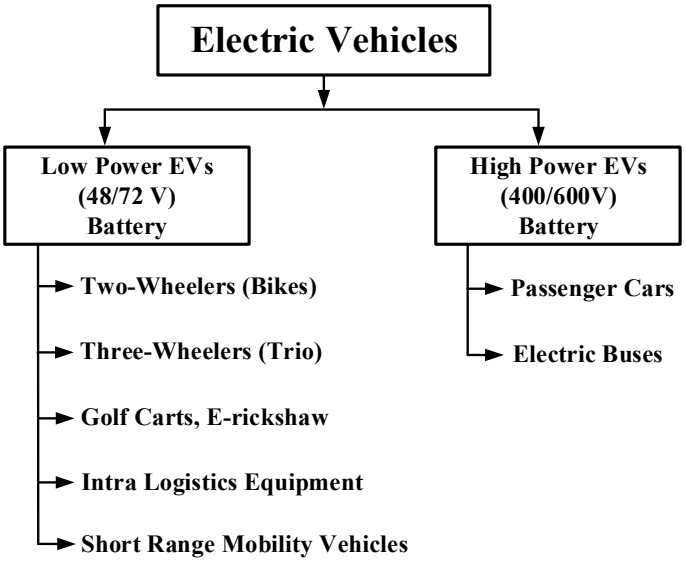


Fig. 1. 1. Classification of EVs

Table 1.1: Types of EVs and Charging Time

EV	Battery Type	Charger Power	Charging Time
Two Wheeler/ E-rikshaw/ Intra Logistics Equipment	SLI – 48V	0.5 – 1 kW	6-8 Hrs
Trio/Golf Carts	Li-Ion / AGM 48V	1 -3 kW	3-4 Hrs
Short Range Mobility Vehicle	Li-Ion 120V	3.3 – 7 kW	4 Hrs
Passenger cars/ Buses	Li-Ion 400-600V	62 - 500 kW	30 mins

Three-wheelers are the intrinsic part of the local transportation in the south East Asian countries. E-rickshaw has gained popularity in the Asian market post-2010 as a result of their symbolic resemblance with traditional auto-rickshaw, they are also exhausting as they don't require all-day peddling unlike cycle rickshaws resulting into more rides in a day proving more profitability. E-rickshaw is hauled by an electric motor ranging from 850W-1400W, which is supplied from the lead-acid battery pack of 100-120 Ah [4]. An article published by Bloomberg claims that the south Asian countries combined have 1.5 million electric three-wheeled rickshaws, which are more than the total number of electric passenger cars sold in China since 2011 [5]. India and China are the two biggest manufacturers of E-Rickshaw [5]. According to an analyst it is estimated that about 60 million Indians hop on an e-rickshaw every day [6]. Research and Markets, a market research company in Ireland claims that the Asia Pacific e-rickshaw market is estimated to hit $11,935.1 million by 2023 [7]. The fast growth of the market is principally pushed by the low ownership cost of electric three-wheelers, falling battery prices, and favorable government policies and support [8]. P&S Intelligence another market research company claims that the Indian and Chinese market to reach double the current scenario by 2024 [9]. An OBC is used to transfer power from the grid to charge the battery pack of the e-rickshaw. The OBC has to be compact and light since it is housed inside the vehicle. In addition, the OBC is also required to limit the input current harmonics to meet regulatory standards, such as IEC 61000-3-2 [10].

1.2 Literature Review

In this section, a detailed review of conventional OBCs along with their architectures is provided.

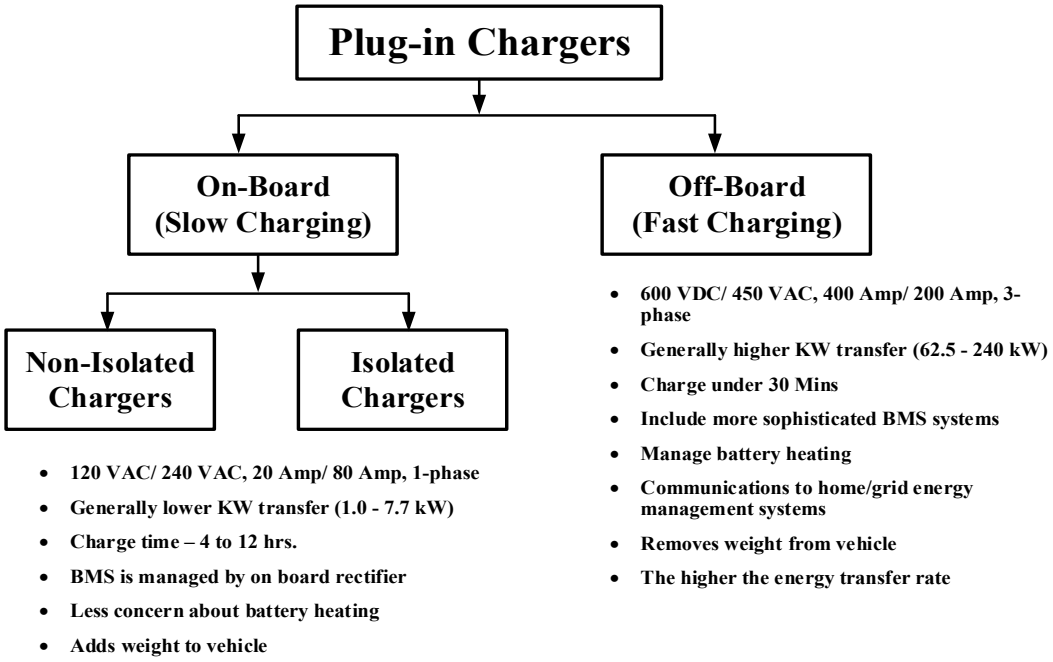


Fig. 1. 2. Classification of plug-in chargers

1.2.1 Classification of Plug-in Chargers

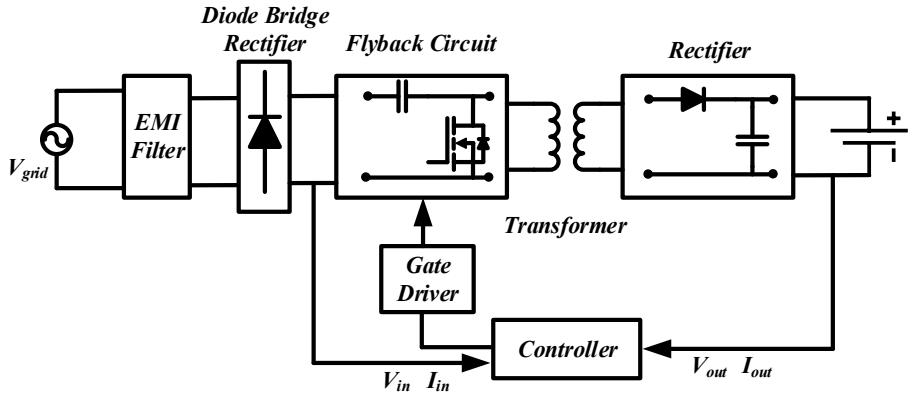
Fig. 1.2 shows the classification of plug-in battery chargers. The plug-in chargers for the EVs are classified into two type's namely on-board chargers and off-board chargers. An off-board charger is generally designed to transfer higher kilowatts of power and requires a more sophisticated battery management system (BMS) on the plug-in hybrid electric vehicles (PHEV) and EVs. A high power off-board charger (>100 kW) can charge the EV battery within 30 minutes. In addition, it removes significant weight from the PHEVs and EVs, which can increase the vehicle's overall efficiency. The demerits of the fast off-board charger are high current is injected in the battery, resulting in the rise of temperature and frequent maintenance and replacement of the batteries. On the contrary, an onboard charger is generally designed for lower kilowatts of power transfer usually 3.3 kW, and is further classified into isolated and non-isolated chargers. The non-isolated topologies do not implement galvanic isolation as the output voltage is low. Therefore, the non-isolated topologies are more compact in weight and have high efficiency [11]. On the other hand, the isolated topologies end up bulky in overall weight since it uses galvanic isolation (usually achieved using an isolation transformer) and possess a complex control structure which reduces overall reliability of OBC [13]. The isolated topologies are again further classified into two types namely single-stage

and two-stage topologies. Based on the on-board charger power level, they charge the battery in 4 to 7 hours [12]. Due to low current charging, it supports the specified lifetime of the battery and demands for reduced maintenance. Most common E-Rickshaw battery is the lead-acid, SLI type as it is cheap to manufacture. Also, It can provide high currents (400-400 A) for turning the starter motor for short periods..

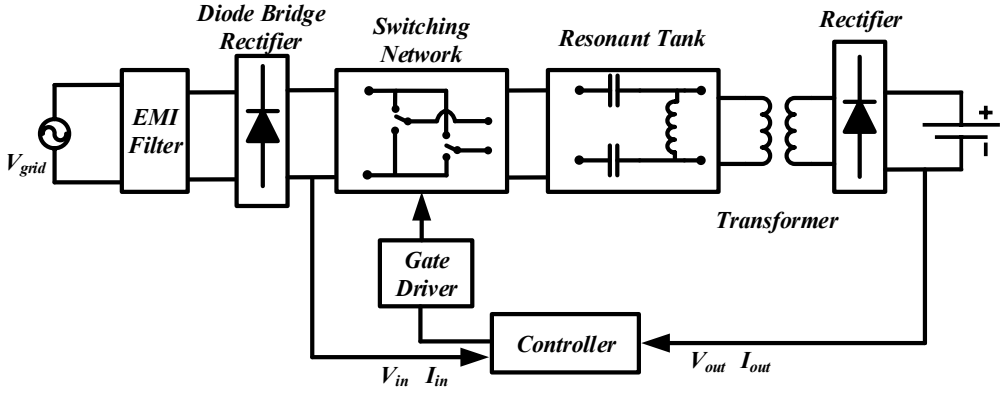
1.3 Conventional OBC Architecture

1.3.1 Single Stage Isolated Topologies

Fig. 1.3 (a) and (b) show the block diagram of the conventional isolated single-stage converter topologies. These isolated topologies consist of a diode bridge rectifier followed by an isolated flyback converter [14] or a half-bridge isolated DC/DC resonant converter [15]. The isolated flyback converter is a very simple and effective solution for battery charging



(a)



(b)

Fig. 1. 3. Single Stage (a) Isolated flyback converter; (b) half bridge isolated DC/DC resonate converter

applications. It has a low components count making it an inexpensive solution to provide a DC voltage from an AC source. This converter also does not require a complex control. The isolated flyback converter topologies suffer from the effect of leakage inductance resulting into high stress on switch voltage [15]. It is observed that when the switch is turn-off the leakage inductance of the transformer is discharged and a huge voltage spike across the switch appears. To clamp this voltage spike across the switch external RCD snubbers are connected [16]. In addition hard-switching operation of the switch also leads to high power losses in the converter.

Single-stage AC-DC converters based on the resonant half-bridge converter provide ZVS operation of the PWM switches and does not face the voltage spike across the switch due to the presence of series resonant tank [15]. However, the majority of these developments have been focused only on reducing the switching power losses. But this configuration also poses losses because of the presence of diode bridge rectifier at the output side. Especially for low voltage battery charging application, the full-bridge diode rectifier causes high conduction and turn-on losses, resulting in additional thermal management requirements [17].

The converters in Fig. 1.3(a) and (b) employ an uncontrolled diode bridge rectifier to converter the AC grid voltage into DC voltage. This uncontrolled diode rectification draws a peaky input current. In both the single-stage isolated converter configurations there is no dedicated PFC converter in the front end resulting into the injection of odd harmonics in the grid leading to poor power quality and higher input current THD [18]. Both the configurations require a bulky passive filter in order to filter out these harmonics consequently leading to increased weight and size of the battery chargers. As per IEC-6000-3-2, the input current THD limit should be less 5% for automobile battery chargers but these chargers fail to meet the standards.

1.3.2 Two-Stage Isolated Topologies

Fig. 1.4 illustrates a simplified block diagram of a universal input two-stage PFC technique. The first stage AC/DC PFC converter typically consists of an EMI filter, rectifier, PFC converter, as well as a DC link capacitor. The PFC stage rectifies the input AC voltage and transfers it into a regulated intermediate DC link bus. The converter is controlled by a

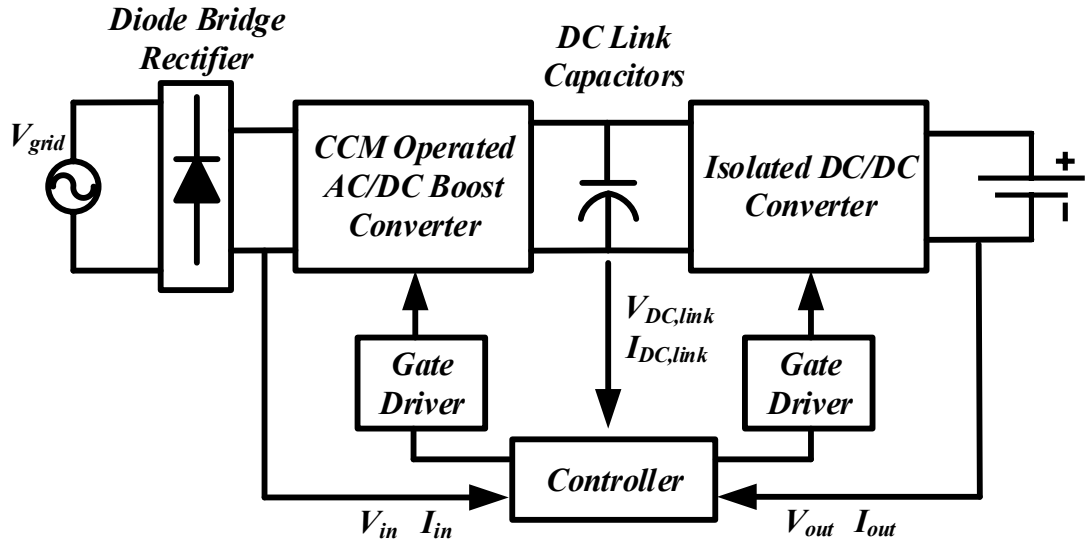


Fig. 1. 4. Block diagram of two-stage PFC technique

high-frequency signal to shape the input current to follow the AC line voltage for near-unity power factor operation. Such converters are operated in continuous conduction mode (CCM) and typically require three sensors in order to achieve PFC [19], [20]. Such systems require high sampling frequency in order to shape input current. A typical second stage of an isolated DC/DC converter consists of a switching network, high-frequency transformer, rectifier, and a low pass filter. This DC-DC stage converts the intermediate DC link voltage into a regulated output voltage, which is required to meet the battery charging specifications. For achieving high efficiency and reduced switching losses, an additional resonant tank between switching network and high-frequency transformer is required. Two of the most common DC-DC converter topologies are phase-shifted full-bridge (PSFB) [19] and LLC resonant converter [20]. The phase-shifted full-bridge converters are able to achieve ZVS turn-on of primary switches by controlling the gating signals. Such converters fails to achieve soft-switching at light load, thus reducing the efficiency of the overall system [21]-[24]. On the other hand, LLC converters achieve ZVS over entire load range, thus overcoming the limitations posed for PSFB. But such converters use complex frequency modulation to control the output voltage and current thus reducing the reliability of the LLC converter [25]-[28].

Although a two-stage topology with galvanic isolation has been a common topology with an additional safety margin, isolation is not an essential requirement for the OBCs, according

to standards such as SAE J1772 [29], [30]. Hence, researchers have studied the applicability of non-isolated chargers for PEVs. Non-isolated topologies have upper hand as compared to the single-stage and two-stage isolated topologies. High-frequency transformer is absent in non-isolated topologies thus, eliminating the problems introduced by the leakage inductance on switch voltage and improve efficiency. In addition a non-isolated OBC possesses less volume and losses. Yet again, these non-isolated topologies deal with the problem of an increased number of semiconductor count and sensors, which increases the cost [11].

1.4 Research Objectives

The objective of this thesis is to investigate on the high-performance single-phase solutions for the AC-DC PFC converter for low voltage EV battery chargers. The thesis investigates both isolated and non-isolated PFC battery charging topologies offering simple and practical solution to achieve high efficiency and PFC with low THD standards defined by IEEE. The active AC-DC PFC converters are studied and analyzed with a focus on minimizing the total number of components, improving power quality, and improving the overall operating efficiency and power density along with reduced cost. The proposed converters are designed for DCM operation in order to simplify the control circuit and to reduce the number of sensors, which consequently increases the converter reliability and robustness. Further, the design and performance of the converter are tested for a supply voltage change, load perturbations, and single-phase operation.

The objectives of this thesis are listed below:

1. High switching frequency operation to reduce the volume, cost, and weight.
2. Sinusoidal input current with low THD (<5%) and UPF operation over a range of input voltage.
3. Stiff and regulated DC output voltage.
4. High efficiency with load current and source voltage variation.
5. Simple and easy control.

To accomplish these objectives, and to replace the conventional diode-based rectifier with active PFC rectification, the thesis proposes three active PFC converter topologies described briefly in the next section, and in detail in various Chapters 2 to 4.

1.5 Thesis Outline

The major research contributions of this thesis are as follows:

In Chapter 2, a non-isolated single-stage single-cell buck-boost AC-DC converter based battery charger configuration with the inductor operating in DCM has been reported. DCM operation is used in order to achieve UPF operation at AC mains without the use of input voltage and current sensors. The converter output is controlled by only one control loop and a single sensor. The proposed topology is cost-effective, compact size and illustrates high efficiency. The steady-state operation, design, DCM condition, small-signal model, and closed-loop controller design have been presented in detail. The operation and performance of the converter are demonstrated using the simulation results obtained from PSIM 11.1 software and the experimental results from a 1.0 kW laboratory hardware prototype testing.

In Chapter 3, to reduce the diode bridge losses, a new front-end bridgeless AC-DC PFC topology is proposed and studied. The proposed converter shows low conduction loss due to bridgeless operation and low voltage stress on the semiconductor devices because of voltage doubler configuration. Low switching losses are achieved due to ZCS turn-on of the MOSFETs. The converter output is controlled by only one control loop and a single sensor. The steady-state operation, design, DCM condition, small-signal model, and closed-loop controller design have been analyzed in detail. The operation and performance of the front end converter are demonstrated with the simulation results using PSIM 11.1 software, and the experimental results from a 1.0 kW laboratory hardware prototype testing.

In Chapter 4, an isolated two-stage onboard battery charger is proposed. Bridgeless DCM topology studied in Chapter 3 is adopted as the first stage for PFC and THD reduction while reducing the number of semiconductors, sensors and the magnetic components. In the second stage, a half-bridge LLC resonant converter is employed to achieve high conversion efficiency over the wide voltage range. The loss analysis is done to determine optimal DC-link voltage for the efficient operation of the converter. The suitability and advantages of the proposed charger are discussed and design guidelines are provided. The analysis and design are validated with simulation results from PSIM11.1 software and further verified with the experimental results from a 1.0 kW laboratory hardware prototype testing.

1.6 Conclusion

This Chapter discusses the progress and ongoing developments in EVs and its promises for the world's shift to sustainable energy and particularly towards reduced emission. EVs provide low-cost ownership, low maintenance, higher efficiency, higher fuel economy and high reliability leading to a rapid increase in the EV annual sales. Emerging innovations in the smart charging for high voltage EVs such as passenger cars and buses have seen an astronomical growth whereas low voltage vehicles (e-rickshaws for local e-mobility) are still less explored in terms of battery charging.

The Chapter investigates and provides a comprehensive overview of the presently used AC-DC converters for EV charging applications. The literature survey provides the advantages and disadvantages along with their limitations to meet power quality standards. The Chapter provides a through overview of both the isolated and non-isolated topologies along with single-stage and two-stage PFC circuits. The limitations of the flyback and half-bridge resonant topologies are shown including high voltage stress and larger transformer size along with increased conduction losses. Also, these topologies suffer from poor efficiency and increased components' count. The disadvantages of the front end diode-bridge rectifier were explained, showing the desirability of PFC operation. Finally, an investigation on the existing two-stage isolated AC-DC PFC configuration was presented. The CCM operated converter requires at least three sensors and two control loops, which increase the burden on microcontrollers. Henceforth, a DCM based battery charger configurations (isolated, non-isolated and front end-bridgeless) are studied in order to reduce cost, volume and achieve high efficiency.

The next chapter deals with a non-isolated single-stage single-cell buck-boost AC-DC converter, operating in DCM is presented for low power EVs (e-rickshaw) battery charging application.

CHAPTER 2: DCM CONCEPT STUDY AND ANALYSIS OF BUCK-BOOST PFC RECTIFIER FOR AC CHARGING

2.1 Introduction

Owing to the research on enabling technologies for transportation electrification worldwide, a tremendous increase in the use of electric vehicles (EVs) has been witnessed due to the increased awareness of environmental issues and fossil fuel depletion threat. Road EVs comprise a broad spectrum of vehicles right from two-wheelers, three-wheelers (rickshaws/Auto/Trio), cars, trucks and electric buses. Three-wheeler has signaled a new era in the field of transport consequently becoming an intrinsic part of local transportation in South East Asian countries. E-Rickshaw has gained popularity in the Asian market post-2010 because of its symbolic resemblance with traditional auto-rickshaw. E-Rickshaw is hauled by electric motor ranging from 850W-1400W power, which is supplied from the lead-acid battery pack of 100-120 Ah [31]. Due to the safety limitations and the lack of charging infrastructure, most E-Rickshaws are equipped with an on-board charger (OBC) that allows us to charge battery packs from standard single-phase power supply sockets.

It has been observed that most of the plug-in battery chargers are based on the two stages power conversion. These chargers have increased semiconductor devices leading to increased system weight and reduced reliability. On the other hand, single stage chargers have reduced number of components thus utilizing minimum number active and passive components [11]. Conventional single-stage isolated AC-DC e-rickshaw chargers available in market utilizes diode-bridge along with a flyback converter topology to control the charging process. These e-rickshaw chargers use a simple charging method by just pushing current equal to the maximum current limit of the lead-acid battery. As the battery voltage increases gradually this current decreases and charging is turned off. Even though such topology is simple to implement, these chargers fail to achieve unity power factor and draw non-sinusoidal current which increases input current THD. Moreover, the present grid-tied e-rickshaw battery chargers do not implement CC-CV mode of charging in order to reduce cost and complexity [32], [33]. On the other hand, single stage PFC chargers have high sensor count, leading to

increase cost and converter complexity [11]. DCM based single-stage chargers reported in [12]-[14] utilizes increased semiconductor count and have bulky transformer leading to poor low load efficiency.

Although a two-stage and single-stage structure with galvanic isolation has been a common topology with an additional safety margin, isolation is not a requirement for OBCs, according to standards such as SAE J1772 [34]. Moreover, the battery ground is always in floating with the vehicle body ground, hence it is not mandatory to have an isolation feature from AC input. EVs are inherently equipped with relays and isolation breakers, which can deactivate auxiliary modules during charging or in any malfunctioning conditions. Therefore, the researchers have studied the applicability of non-isolated chargers for low voltage EV battery charging applications.

2.2 Review of Non-Isolated PEV Charger Topologies

In order to select optimum non-isolated topology for battery charging, two-stage interleaved buck topology, non-inverting buck-boost PFC topology, Sepic PFC topology, as well as Cúk PFC topology are reviewed for low voltage EV charging application.

2.2.1 A Two-Stage Interleaved Buck Topology

Fig. 2.1. illustrates the schematic of a two-stage interleaved buck converter topology. An AC-DC boost PFC converter is used to convert the universal grid input to a fixed dc-link voltage, which is higher than the maximum battery voltage. An interleaved buck converter is employed to step down the dc-link voltage to the required battery voltage. With this interleaving configuration, output current ripples are mostly compensated as they cancel each other out. In addition, the current stress on each leg is reduced to half so that a higher power level can be achieved. While this is one of the simplest topologies for battery charging application, it exhibits higher component count, high power loss, and complex control. The topology also suffers from high voltage stress, PFCs have high switching and conduction losses [35].

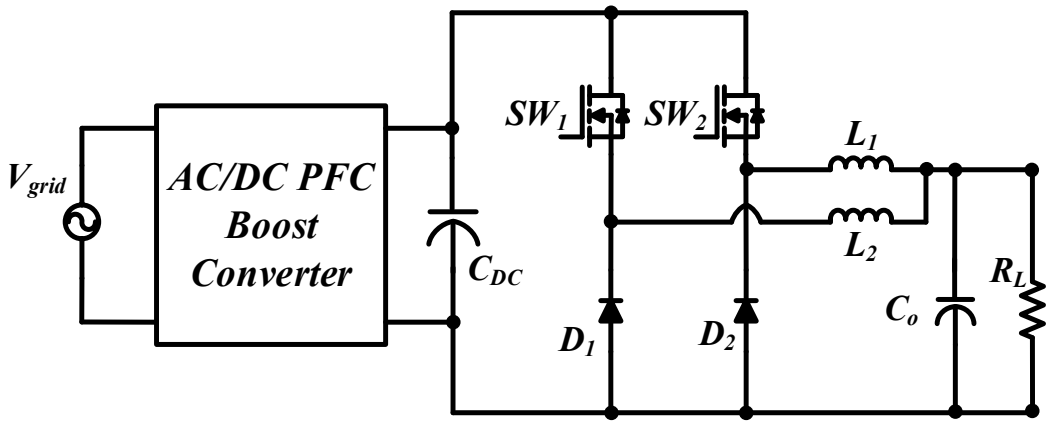


Fig. 2. 1. Two-stage interleaved buck converter

2.2.2 Non-Inverting Buck-Boost Topology

Fig. 2.2 shows the schematic of the non-inverting buck-boost converter. Non-inverting buck-boost topologies are appropriate solutions for the battery-powered power supplies, fuel-cell systems, telecommunication systems, and PFC applications due to their ability to provide wide operating range of input and output voltage [36]. These applications require both buck and boost operation depending on the input and output voltage magnitudes. When the input voltage is greater than the output voltage, a buck operation is used. Boost operation is performed when the input voltage is less than the output voltage. This topology benefits from low voltage stresses across MOSFET and the input ground polarity is the same as that of the output side [35]. One of the key difficulties in non-inverting buck-boost topology is the smooth transition from buck to boost operation or boost to buck operation that requires fast

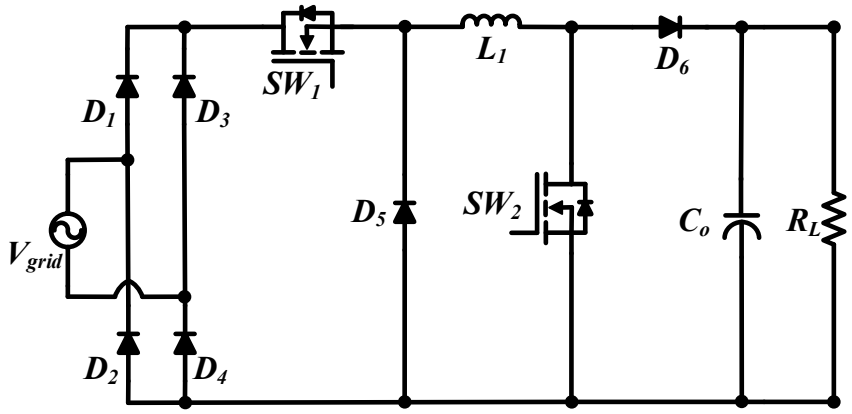


Fig. 2. 2. Non-inverting buck-boost converter

and precise voltage sensors for the input and output voltages. The sensor delay, coupled with the unaccounted voltage drops in the converter components, leads to a discontinuity in the input current during the transition between the modes. Additionally, hard-switching between the two modes leads to high and unstable output voltage transients. Hence, this topology requires a complex control and a large EMI filter resulting in a bulky converter and complex system operation [37], [38].

2.2.3 Sepic Converter

A typical Sepic converter with PFC stage is shown in Fig. 2.3. The converter is gaining popularity in the field of battery charging because of the reduction in input current ripple along with non- inverting buck-boost characteristics. It also provides a high power factor despite the output voltage because of the step-up and step-down functions [35]. Though there are these added advantages, still it does not overcome the traditional problem of buck-boost derived converter of higher voltage stress i.e. (V_{in}+V_{out}). It also increases the number of passive components (L and C) and requires a more robust and bulky LC filter to overcome the input current ripple [39].

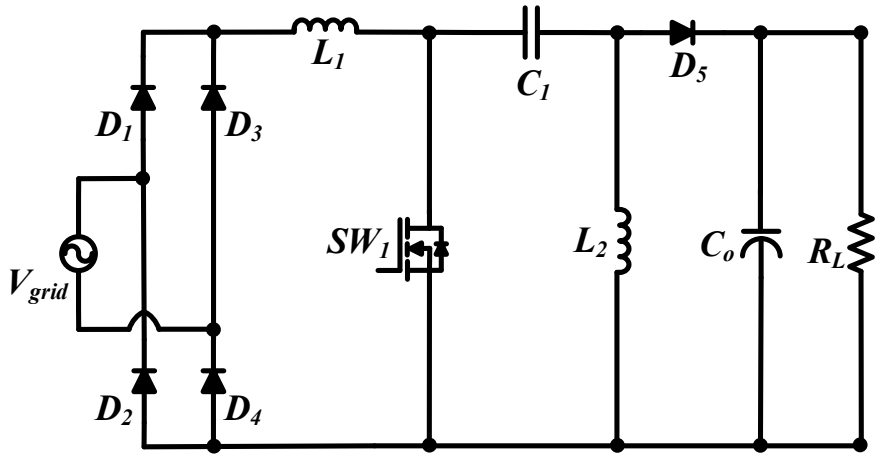


Fig. 2. 3. Sepic converter

2.2.4 Ćuk Converter

Fig. 2.4 shows the schematic of Ćuk converter. The primary advantage of the converter is that it has continuous input as well as the output current. Moreover, the output voltage can be either higher or lower than the input voltage depending upon the requirement. In addition, the

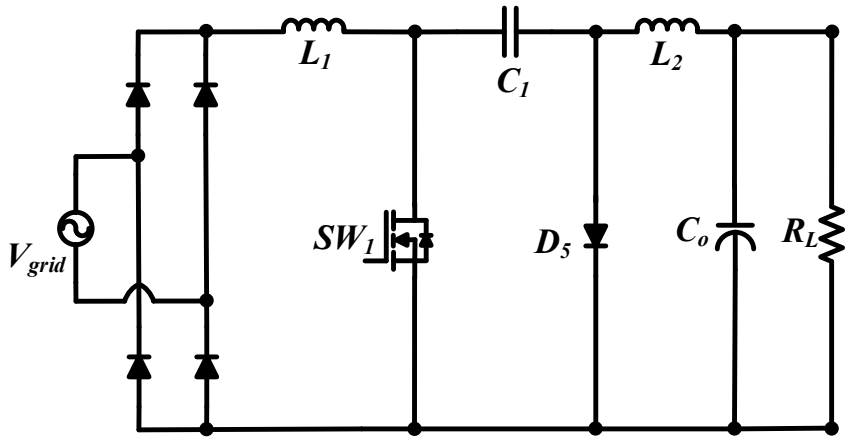


Fig. 2.4. Cuk converter

input and output filter size is considerably smaller than buck-boost derived converters. However, on the other hand, the converter has both high voltage and current stress across the switching devices resulting in a high number of passive components and large inductors [40]. Phenomena similar to the buck-boost converter of reversed ground polarity between the input side and the output side can also be observed [35].

Therefore, from the above review, it is clear that the present non-isolated power converter topologies also struggle with a higher component counts', higher losses along with the control complexity henceforth, ending up using more additional sensors along with the implementation of PLL. Table 2.1. describes the present operating conditions of an e-rickshaw. Hence the topology should satisfy the following requirements for the OBC system.

1. The output voltage should be stably controlled for a wide input-voltage range.
2. The input current should comply with the standards of the UPF.

Table 2.1: Specification of E-Rickshaw

Parameter	Specifications
Speed	0-25 km/hr in Power Mode
Range	120 km/Charge
Loading Capacity	Up to 4-5 Passengers
Battery Rating	4*12V (48V) of 100-120Ah Capacity
Motor Rating	48V, 850-1400 W BLDCM
Charger output voltage	63-65V
Output charging current	10-12A

3. High-frequency switching control for compact and lightweight charger.
4. Simple, reliable and stable control.

Considering the limitations of the above-mentioned topologies and the present operating conditions of an e-rickshaw, a traditional non-isolated single-cell buck-boost converter for e-rickshaw battery charging operated in discontinuous conduction mode (DCM) in order to reduce sensor count and control complexity has been studied and analyzed. The topology is not only cost-effective but also reduces the number of semiconductor devices as compared to [11]. Due to the DCM operation, as inductor current is zero in every switching cycle, semiconductor switches realize zero current switching (ZCS) turn-on and the diodes have zero reverse-recovery losses. A DCM buck-boost becomes meritorious as the inductor is either connected to the input or to the output, thus harmonics from the output are not transferred to the input side thus achieving a good THD and UPF operation. Moreover, it has less passive component count as compared to the conventional Sepic or Ćuk converter making it a cost-effective option for this application. The additional advantage of the converter is the reduced input filter size thus diminishing the overall weight of the system.

2.3 Studied converter and control scheme

Fig. 2.5 shows the DCM operated non-isolated single-cell buck-boost converter. The studied converter is derived from the classical buck-boost converter. The converter is a combination of a full-bridge diode rectifier and a single switch buck-boost converter. When

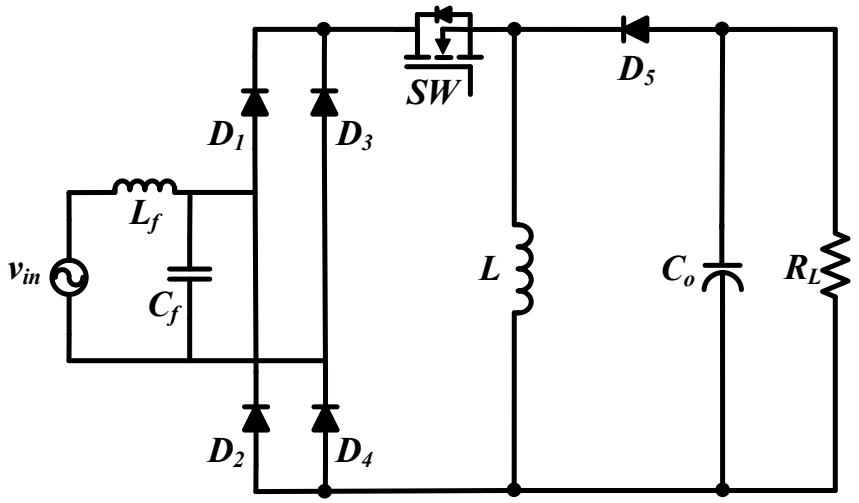


Fig. 2. 5. Non-isolated single-cell buck-boost converter

switch is closed, the inductor current increases and stores energy while the capacitor supplies the load. The inductor supplies the current to the load through the diode when the switch is opened. The control objectives of the PFC converters are to achieve the sinusoidal input current in-phase with the input voltage and to have uniform output voltage regardless of the variation to the input voltage and load. The converter operates in DCM thereby achieving the first control objective. It is acclaimed that in the DCM mode, the buck-boost converter acts as a resistor which is the unique property of the converter [39]. The duty cycle of the converter is always fixed for a given power and input voltage. The duty cycle of the single switch PFC buck-boost converter operating in DCM does not change with sinusoidal change in input voltage, unlike traditional PFC converters. However, the duty cycle changes only if there is a change in output voltage reference or any disturbances. This feature is mathematically derived in [39] for a single buck-boost converter operating in DCM.

The discontinuous current in the output inductor is defined by the current discontinuity in the output diode. Therefore, once the current discontinuity in the output diode is ensured, the converter emulates a resistor behavior at AC mains and provides a sinusoidal input current in-phase with the input voltage. Subsequently, it eliminates the inner current loop and requires only one simple voltage control loop to regulate the system output voltage. Fig. 2.6 illustrates the control circuit for the studied converter. The converter output is controlled by only one control loop and a single sensor. Thus achieving the second objective of the converter.

A comparative evaluation with the state-of-the-art non-isolated topologies is provided in Table 2.2. In all the above state-of-the art converters, it is observed that at all the converters have a higher components' count, complex control system which makes the system bulky and costly.

The studied converter is also meritorious over the other non-isolated topologies as it has less volume, cost, and losses. Moreover, it possesses the capability of maintaining high power quality for a wide input voltage range and a fixed output voltage and achieves zero current switching (ZCS) as inductor energy is zero reset to every switching cycle. The studied buck-boost OBCs draw power from the input grid supply and fulfill the output requirements

Table 2.2: Comparison of the studied converter with the state-of-the art converters

Parameters	Two-Stage Interleaved Buck	Non-inverting buck-boost	Sepic Converter	Cuk Converter	Studied Converter
No. of Semiconductor Devices	6	4	2	2	2
No. of Passive Components	5	2	4	4	2
Control Technique	Complex	Complex	Moderate	Moderate	Simple
Cost	High	Medium	Medium	Medium	Low
Size	Bulky	Moderate	Moderate	Moderate	Small

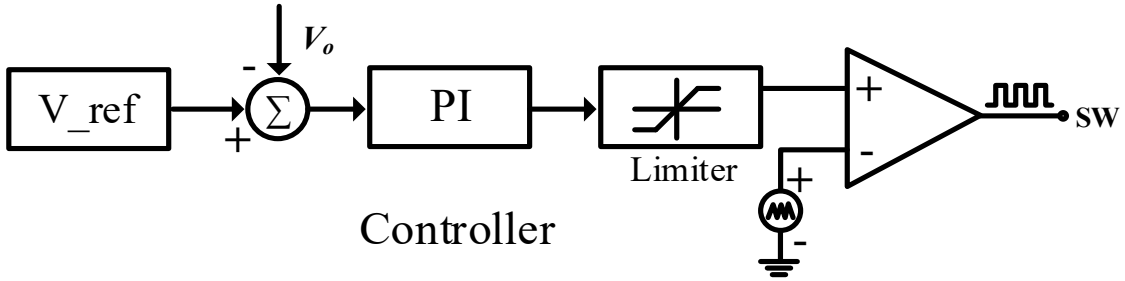


Fig. 2.6. The control circuit for the studied converter.

maintaining, the harmonics of the input current drawn from the grid as per the IEC and EN 6100-3-2 class D standard [41]. The converter achieves a high input PF and low harmonic distortion, PFC. The studied converter achieves PFC over a range of input voltage while maintaining a low THD of less than 5%. It also maintains a stiff regulated DC output voltage. Due to the DCM operation, the sensor requirement is reduced to one voltage sensor and avoids the sensing of the input current, input voltage sensing and output current. It allows simple and effective control.

2.4 Converter Steady-State Analysis Over One Switching Cycle

The converter has unidirectional operation and operates in buck mode. The converter is designed to be operated in DCM to achieve natural PFC at AC input.

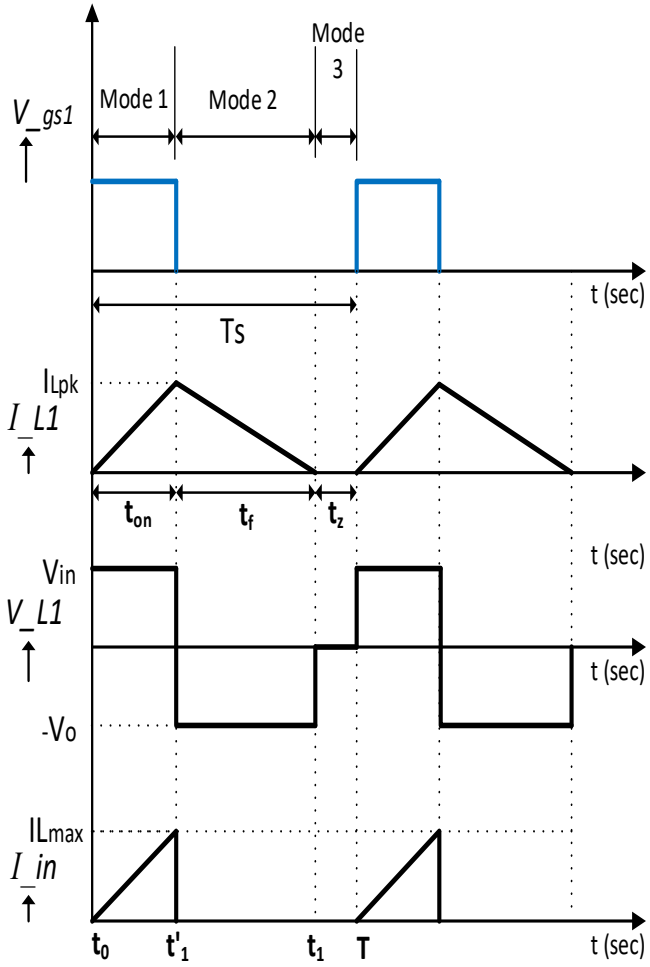


Fig. 2. 7. Waveforms for one switching cycle

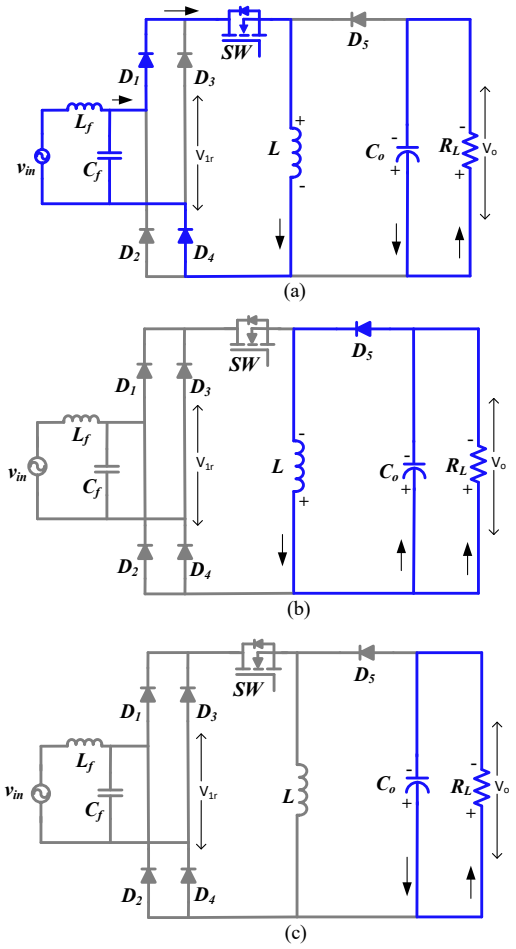


Fig. 2. 8. Equivalent circuits during positive half-cycle; (a) Mode-1; (b) Mode-2; (c) Mode-3.

The steady-state waveform of the studied converter for one switching cycle are shown in Fig. 2.7 with the following assumptions whereas Fig. 2.8 shows equivalent circuits during the positive half cycle:

a) All components are ideal.
b) Within one switching cycle, input and output voltages are constant
c) The output capacitor is large enough to maintain the output voltage constant.
d) The duty cycle is fixed for one power level.

1) Mode I:- ($t_0 < t < t_1^{'}$)

This stage is shown in Fig. 2.8(a) and is defined as ON state of the switch. In this stage, the inductor charges, capacitor supplies the load and the inductor current is given as,

$$i_L(t) = \frac{V_{1r}}{L} t_1' \tag{2.1}$$

2) Mode II:- $(t_1' < t < t_1)$

The switch is turned off and inductor current freewheels through the diode as shown in Fig 2.8(b) and current $i_l(t)$ is defined as,

$$i_L(t) = i_{Lpk} - \frac{V_o}{L}(t_1) \tag{2.2}$$

where $i_{L,pk}$ is the peak inductor current given by

$$i_{Lpk} = \frac{V_{1r} D T_s}{L} \tag{2.3}$$

Where, DT_s=switch on-time, L= DCM inductor and V_{1r} = rectified AC voltage

3) Mode III:- $(t_1 < t < T)$

In this stage where the capacitor supplies the load as shown in Fig. 2.8(c). This stage lasts until the new switching cycle ends. The zero time of switch and diode is given by

$$t_{z=} T_s - t_{on} - t_f \tag{2.4}$$

Where, t_z= zero time period, t_{on}= on-time of switch t_f= fall time of inductor current

2.5 Studied Converter Design

This section presents the expressions for converter average output current, input current, and derives the DCM condition and the design equations for each passive component.

2.5.1 Average Output Current

The average output current $I_{O\,,Avg}$ is indeed the average diode current that is the area under the i_l curve (Fig 2.7). From (2.2) and (2.3) and substituting t=t_f, in (2), we get

$$I_{O\,,Avg} = \frac{1}{2} * t_f * i_{Lpeak} \tag{2.5}$$

$$I_{O\,,Avg} = \frac{V_{1r}^2 D^2 T_s}{2 V_o L} \tag{2.6}$$

$$i_{o,avg} = \frac{V_1^2 D^2 T_s \sin^2(\omega t)}{2 V_o L} \tag{2.7}$$

And thus the average current for half of the line period is given by

$$I_{O\ Avg} = \frac{1}{\pi}\int_0^{\pi} i_{o,avg} d\omega t \tag{2.8}$$

$$I_{O\ Avg} = \frac{V_{1r}^2 * D^2 * T_s}{4LV_o} \tag{2.9}$$

2.5.2 Input Current

Assuming 100% efficiency, the input current expression of the studied converter for one switching cycle can be defined as

$$V_o I_{O\ Avg} = v_1 i_1 \tag{2.10}$$

Using Equation (2.7) and (2.10) and noting that$v_1^2 = (V_{1r}^2)$, from equation (2.11) sinusoidal current is drawn at all times

$$i_1 = \frac{V_1 D^2 T_s sin(\omega t)}{2L} = I_1 sin(\omega t) \tag{2.11}$$

$$I_1 = \frac{V_1 D^2 T_s}{2L} \tag{2.12}$$

Equation (2.12) shows that the filtered input current is sinusoidal and is in phase with the input voltage, which proves the UPF operation of the converter.

2.5.3 DCM Operation and Critical Conduction Parameters

Following inequalities must hold for DCM operation which is given as

$$t_{on} + t_f < T_s$$

$$d\left(1 + \frac{1}{M} sin\{\omega t\}\right) < 1 \tag{2.13}$$

At ωt = 90^0, is the worst-case to operate in DCM

$$D < \frac{M}{1+M} \tag{2.14}$$

Where, $M = \frac{V_o}{V_1}$

The average output current is given by,

$$I_{O\ Avg} = \frac{Vo}{R} \tag{2.15}$$

From (2.9) and (2.15),

$$D = \sqrt{2K}M \tag{2.16}$$

Where K=conduction parameter of the converter

$$K_{cond} = \frac{2L}{RT_s} \tag{2.17}$$

From (2.14) and (2.16) critical conduction parameter K_{cric} can be calculated as

$$K_{critical} = \frac{1}{2M^2} \tag{2.18}$$

2.5.4 Design of Inductor

To maintain PFC under all conditions, the inductor current needs to be in DCM for worst-case input voltage. Value of inductor is calculated as,

$$L < \frac{V_{1r} * D^2 * T_s}{2I_{in}} \tag{2.19}$$

2.5.5 Design of Output Capacitor

In the PFC rectifier, the output capacitor is designed to filter the harmonic components occurring at twice the line frequency. Thus, the variation in the power (input and output) is supported through the output filter capacitor and is expressed as

$$P_c(t) = P_{ac}(t) - P_o(t) \tag{2.20}$$

$$V_o i_c = V_s I_s cos2\omega t - V_o I_o \tag{2.21}$$

Considering efficiency equal to 100%,

$$i_c(t) = \frac{V_s I_s}{V_o} cos2\omega t = I_o cos2\omega t \tag{2.22}$$

The output voltage ripple equation is given by,

$$V_{o,ripple}(t) \approx \frac{1}{C}\int i_c(t)dt \tag{2.23}$$

By substituting (2.22) into (2.23),

$$V_{o,ripple}(t) = -\frac{I_o sin2\omega t}{2\omega C} \tag{2.24}$$

$$C_o = \frac{I_o}{2\omega V_{o,ripple}} \tag{2.25}$$

2.5.6 Design of Input Filter

The criteria to design a low-pass LC filter is as follows:

1. Selection of cut-off frequency f_c given by

$$f_c = \frac{1}{2\pi}\sqrt{\frac{1}{L_f C_f}} \tag{2.26}$$

2. Minimization of filter reactive power consumption for 60 Hz at 1.0 kW. The reactive power is minimum when filter characteristic impedance Z_{ch} is equal to the converter impedance Z_{in} i.e.

$$Z_{ch} = \sqrt{\frac{L_f}{C_f}} = Z_{in} \tag{2.27}$$

where Z_{in} is given by

$$Z_{in} = \frac{2L}{D^2 T_s} \tag{2.28}$$

Using (2.26) and (2.27), low-pass filter parameters L_f and C_f can be obtained as

$$L_f = \frac{Z_{ch}}{2\pi f_c} \tag{2.29}$$

$$C_f = \frac{1}{2\pi Z_{ch} f_c} \tag{2.30}$$

2.6 Studied Converter Small-Signal Model

The average current injected equivalent circuit approach (CIECA) [42], [43] is used to derive the control-to-output transfer function. In this approach, the converter non-linear part is substituted with the switching cycle average value of current generated by it as shown in Fig. 2.9. Introducing the perturbations to (5.9) and ignoring the second-order terms.

$$\hat{\imath}_{o,avg} = \left(sC + \frac{1}{R_L}\right)\hat{v}_o \tag{2.31}$$

On applying perturbations to (12) we get

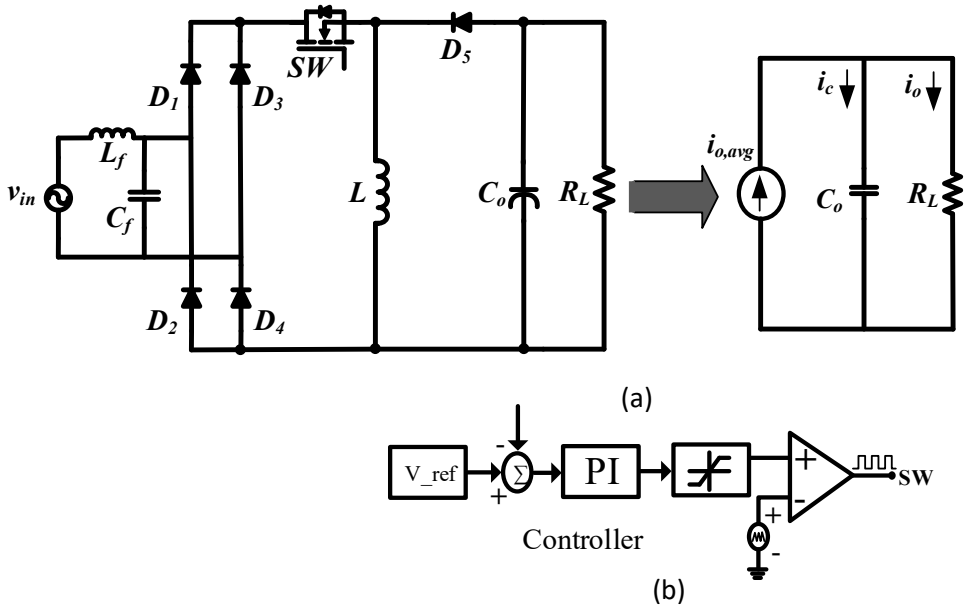


Fig. 2. 9. (a) Equivalent circuit for small signal modelling. (b) Control Diagram.

$$\hat{\imath}_{o,avg} = \frac{V_{1r}^2 DT_s}{4LV_o}\hat{d} + \frac{V_{1r}D^2T_S}{4LV_o}\hat{v}_{1r} - \frac{i_{o,avg}}{V_o}\hat{v}_o \tag{2.32}$$

On equating (2.31) and (2.32), and substituting $\hat{v}_{1r} = 0$

$$\frac{v_o(s)}{d_o(s)} = \frac{V_{pk}D}{K_{cond}M(sR_LC + 2)} \tag{2.33}$$

Where,$C = C_o$ $M = \frac{V_o}{V_{1r}}$ and R_L =load resistance.

The converter control to output transfer function is obtained by substituting the design parameters in (2.33). As the transfer function is a single-pole system, a simple PI controller $\left(K_p + \frac{K_i}{s}\right)$ is used to control the output voltage as shown in Fig. 2.9(b). The output voltage is sensed using a hall-effect based LV-25P sensor. The sensed voltage is compared with the reference voltage and the error is fed into the PI controller. The PI controller generates the duty cycle to control the switch SW. A limiter is connected in order to limit the duty cycle during start-up and overload conditions.

Table 2.3: Converter design specifications.

Parameter	Value
Line voltage, $\boldsymbol{V_{in}\ RMS}$	110 $V_{RMS\ nominal}$
Input frequency, $\boldsymbol{f}$	60 Hz
Output power, $\boldsymbol{P_o}$	1.0 kW
Output voltage, $\boldsymbol{V_o}$	65 V
Switching frequency, $\boldsymbol{f_{sw}}$	50 kHz
Duty cycle, $\boldsymbol{D}$	0.213
Buck-Boost Inductance, $\boldsymbol{L}$	10 µH
Output capacitance, $\boldsymbol{C_o}$	1800 µF
Output voltage ripple, $\boldsymbol{V_{o,ripple}}$	5% of output voltage (V_o)

2.7 Result and Discussion

This section presents the simulation and experimental results of the studied converter to validate the converter analysis and design and presents a discussion on converter efficiency.

2.7.1 Simulation Results

The studied converter is simulated in PSIM 11.1 software to confirm the converter analysis and design. The converter design specifications are given in Table 2.3. The buck-boost inductance value is calculated from (2.19). The output filter capacitance value is calculated from (2.25). Using the designed parameters, the converter control-to-output transfer function is obtained from (2.33) and is given in (2.34). A PI controller transfer is designed for phase margin of 60^0 a bandwidth of 314.159 rad/sec. By taking $k_p = 0.003$ and time constant $\tau = 0.012$ controller is designed and implemented.

$$\frac{v_o(s)}{d(s)} = \frac{1282.584}{1 + 0.032s} \tag{2.34}$$

With the designed parameters and the designed controller, the circuit is simulated, and the results have been presented for input frequency f = 60 Hz. The simulated input voltage and input current waveforms for half load (500W) and full load (1.0 kW) are shown in Fig. 2.10(a) Fig. 2.10(b) respectively. It is observed that input current is in phase with input voltage, thus validating UPF operation of the converter. The output voltage and output current are shown in Fig. 2.10(c). It is seen that output voltage has second order line frequency ripple, thus

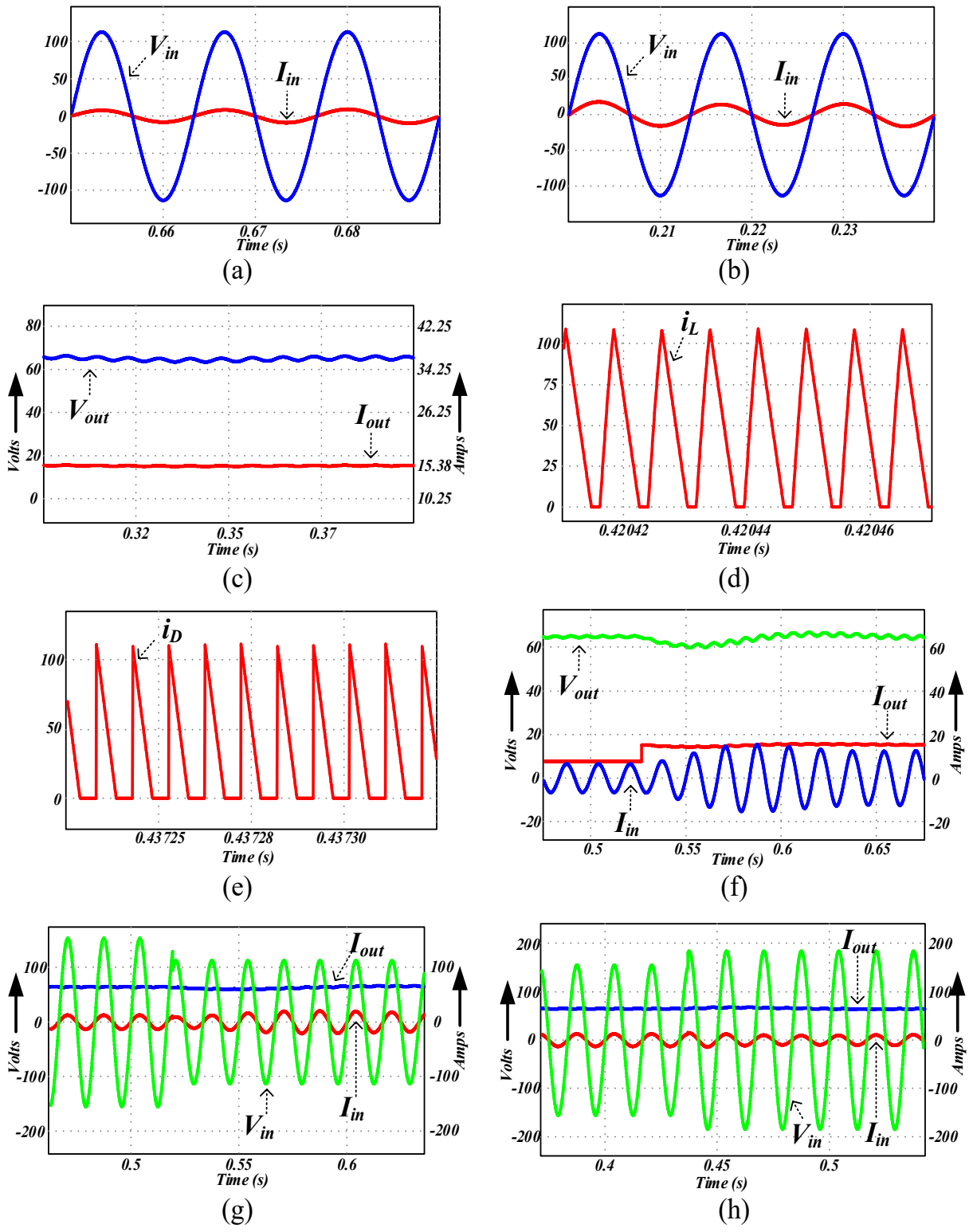


Fig. 2. 10. Simulation results (a) input voltage and input current at 250W; (b) input voltage and input current at 1kW (c) output voltage and output current; (d) inductor current; (e) output diode current; (f) load change from 100% to 10%; (g) input voltage change from 110 V to 80 V. (h) input voltage change from 110 V to 130 V.

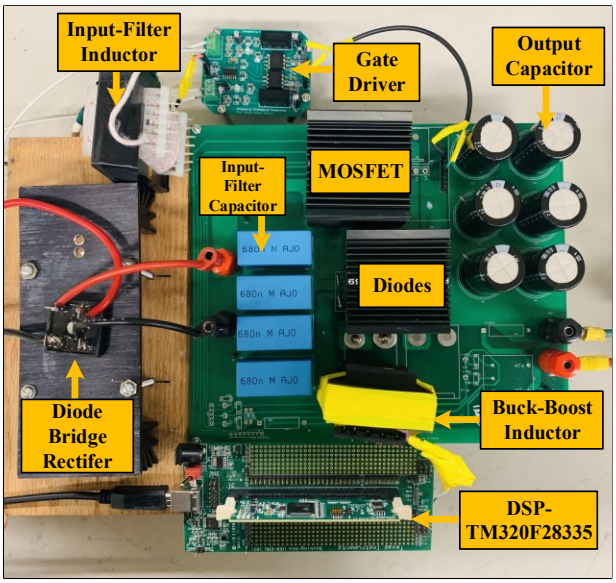
Table 2.4: Converter hardware specifications.

Components	Specifications
MOSFET	IPW60R018CFD7XKSA1, SiC 600V, 18mohm
Diode	60EPF12,1200V, 60A
Input filter capacitor C_f	0.68 μF*4, 480 VAC, R76QR32204030J
Input filter inductor L_f	371μH, 42 x 21 x 20, EE Ferrite Cores
Output filter Cap	1800 μF*6, 100 VDC, LGU2A182MELA
Buck-Boost Inductor	10 μH, EE Ferrite Cores
DSP	DSP-TMS320F28335
Gate Driver	Gate Driver IC, IXYS-IXDN609SI

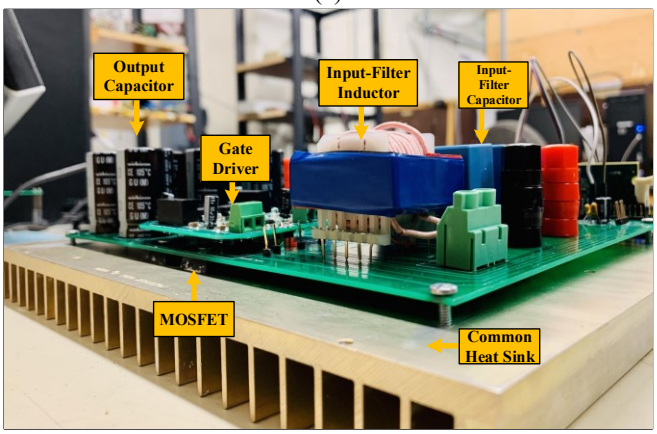
validating the output capacitor selection criteria. Fig. 2.10(d) and Fig. 2.10(e) shows the inductor current and diode current respectively, thus confirming DCM operation of inductor and zero reverse recovery losses of buck-boost diode. The output voltage, output current and input current waveforms during a load change from 50% to 100% is shown in Fig. 2.10(f). The controller responds immediately to the load change, and the output voltage is settled at reference value 65 V within the designed settling time of 10 ms. Fig. 2.10(g) and Fig. 2.10(h) shows the converter response during input voltage perturbations from 110 V to 80 V and 110 V to 130 V respectively. Output voltage is maintained at constant value of 65 V and the input current is closely tracking the input voltage both being in phase and shape. The output current is stable and tracking the reference current with a settling time of 10ms, which confirms the robustness of the design controller.

2.7.2 Experimental Results

To validate the analysis of the converter and to verify the simulation results, a 1.0 kW proof-of-concept laboratory hardware prototype has been built for the same specifications used in the simulation. The hardware details are given in Table 2.4. The DSP TMS20F28335 is employed as a digital control platform to generate the gate signals for the converter. The hall- effect sensor LV-25P is employed to sense the converter output voltage. Fig. 2.11(a) and Fig. 2.11(b) show the top and side views of the experimental set-up respectively. The converter nominal input voltage of 110 V RMS is been selected as per voltage-levels available in the lab. The input filter parameters L_f and C_f are calculated for a corner frequency of 5 kHz. Fig. 2.12(a) shows that the input current is purely sinusoidal and inphase with the input



(a)



(b)

Fig. 2. 11. Experimental prototype of single stage single cell converter (a) top view. (b) Side view.

voltage, thus achieving PFC at 1.0 kW. Fig. 2.12(b) shows the input voltage and current waveforms, output voltage and current waveforms, which indicate that the input current is sinusoidal and in phase with the input voltage result in UPF operation. Fig. 2.12(c) shows the diode and switch stresses for the studied converter. The zoomed version of both is shown in Fig. 2.12(d) when switch SW is turned on inductor L charges and diode D blocks with a voltage equal to Vo+Vm. Fig. 2.12(e) and Fig, 2.12(f) shows the switch voltage and inductor current profile at 1.0 kW. It is observed that switch switches turn on with zero current, thus validating ZCS turn-on operation of the converter. The inductor current profile is illustrated in Fig. 2.12(g) and Fig. 2.12(h) respectively. It is observed that inductor current reaches zero in every switching cycle, thus confirming DCM operation of inductor.

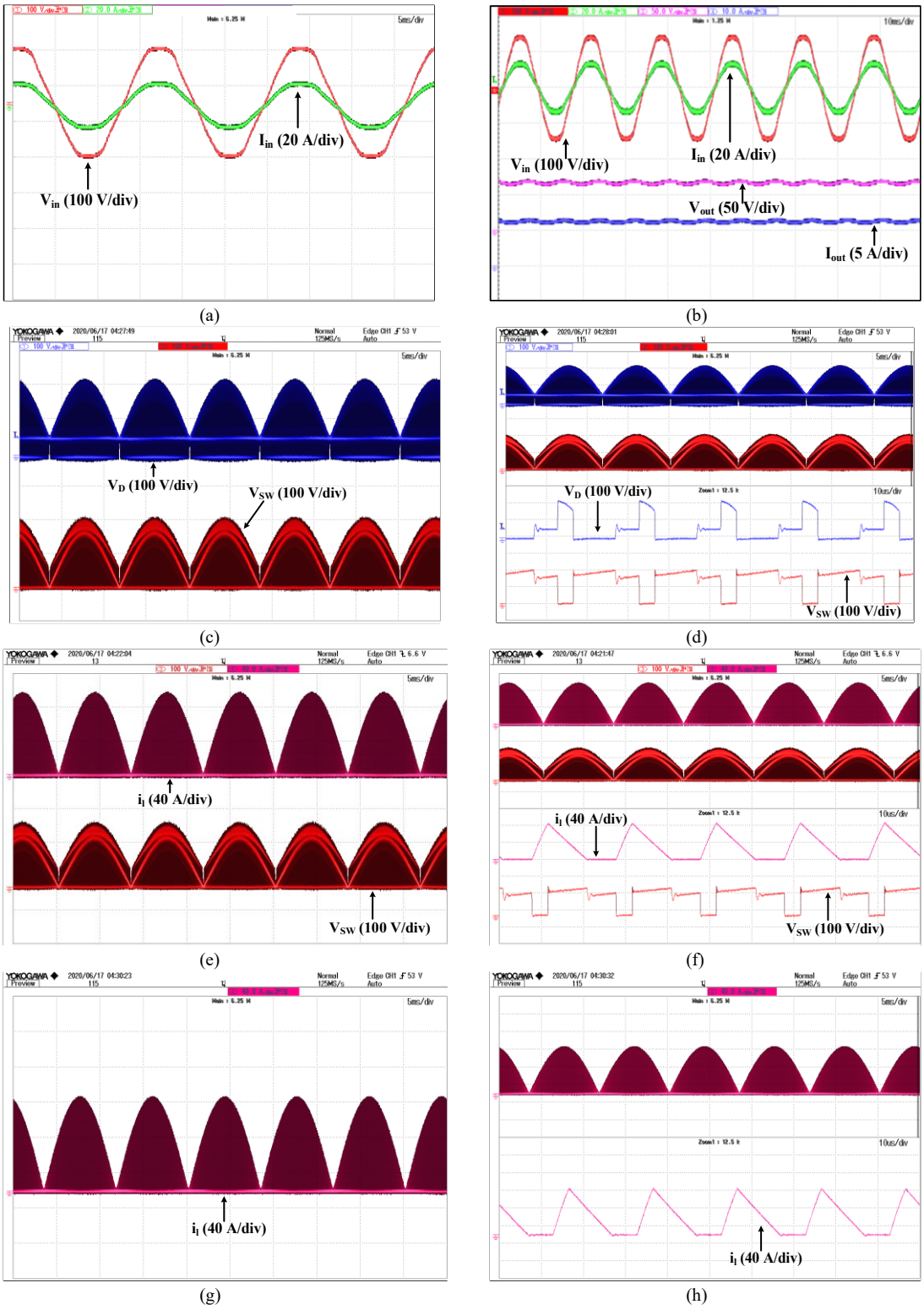
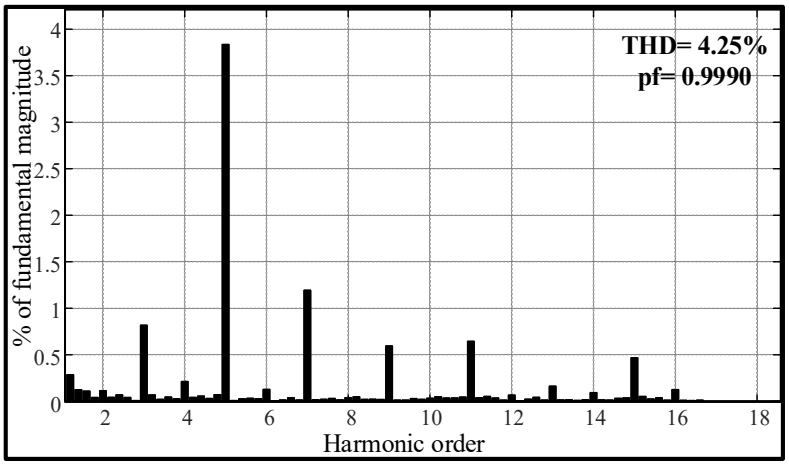
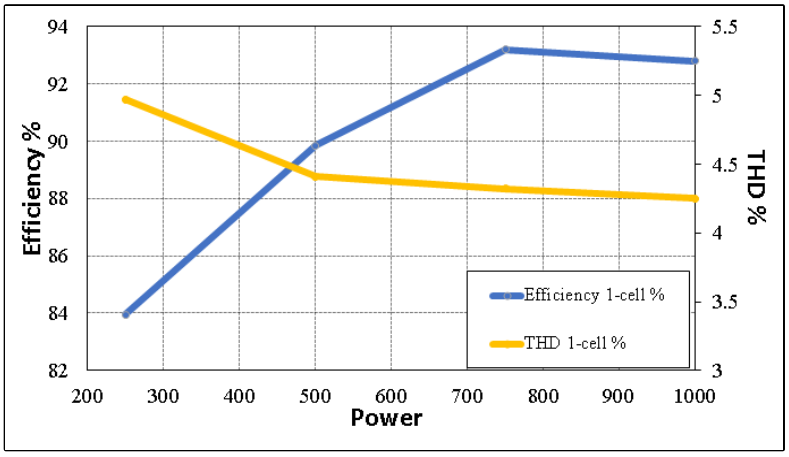


Fig. 2. 12. Experimental results (a) PFC operation at 1.0 kW. (b) Efficiency of single-cell converter (c) Single-cell diode and switch voltage stresses (d) Zoomed in version for single-cell voltage stresses on diode and switch. (e) Switch voltage and inductor current waveform. (f) Zoomed in version for switch voltage and inductor current waveform. (g) Inductor current waveform. (h) Zoomed in inductor current waveform at 1.0 kW.



(a)



(b)

Fig. 2. 13. (a) FFT analysis of input current for single-cell converter, (b) THD and Efficiency of converter

Fig. 2.13(a) shows the input current harmonic spectrum. The measured input PF is 0.999 and the THD is 4.25 % which is as per IEC-61000-3-2. Fig. 2.13(b) shows the variation of THD and efficiency of the studied single-cell converter for various power levels. It is seen that the converter maitains a THD of below 5% and an efficiency of above 82% for all power power levels.

In order to validate the robustness of the controller, two load disturbances are applied. Fig. 2.14(a) and Fig. 2.14(b) show load disturbances from 500W to 1.0 kW and from 1.0kW to 500W respectively. In both cases, it is observed that the output voltage tracks closely the reference voltage and is settling in the design time of 30ms. To confirm converter UPF operation for line voltage variation, it is subjected to 25% line voltage dip and swell conditions. Fig. 2.14(c) shows the converter response for the input voltage variation from

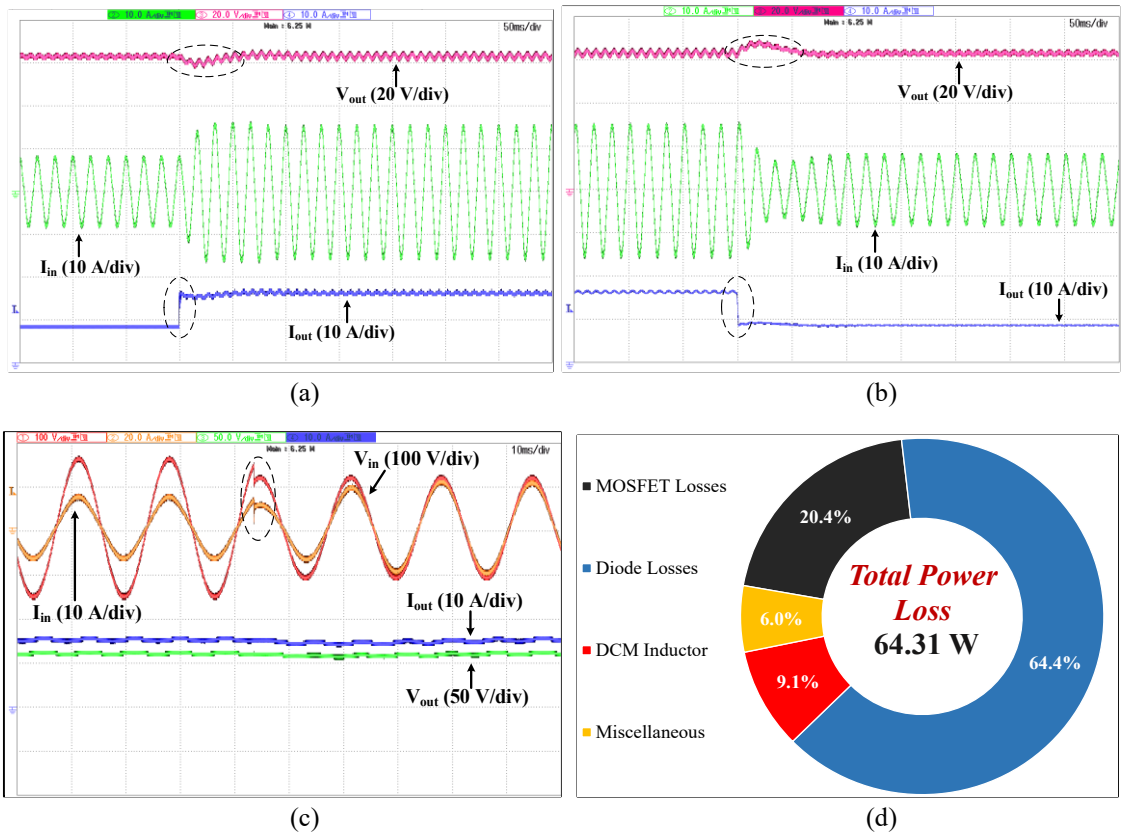


Fig. 2. 14. Converter response (a) load change from 500W to 1.0 kW, (b) load change from 1.0 kW to 500 W, (c) input voltage swell, (d) Power loss distribution of converter at 1.0 kW.

110V to 80V RMS. It is observed that during the voltage dip condition, the input current is increased for maintaining the same power. In these conditions, input current remains sinusoidal which confirms UPF operation thus validating the design. Fig. 2.14(d) shows the power loss distribution chart at 1.0 kW. The semiconductor losses contribute to a significant amount of total losses with diode losses contributing up to 64.4 % of the total losses.

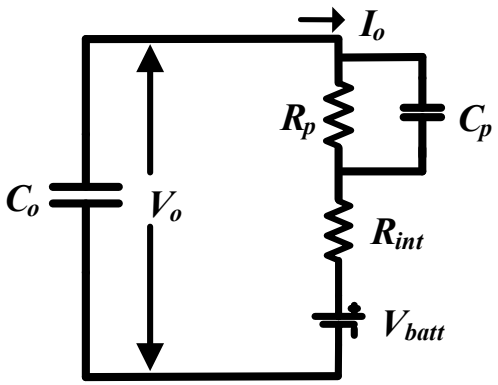


Fig. 2.15 Battery Equivalent circuit when connected to battery charger.

Battery equivalent circuit is shown in Fig. 2.15. It consists of a series internal resistance and parallel capacitor C_p, along with resistor Rp, which defines the battery capacity given by 2.34. During the charging process, charger pushes in current equal to the maximum battery current limit in order to charge it. During this period, battery acts as a current sink and absorbs charge in order charge completely. Thus the charging of a battery can be emulated by a resistive load, which acts as a current sink, and has been implemented as a load instead of practical battery for experimental verification.

$$C_p = \frac{kWh * 3600 * 1000}{0.5(V_{batt,max}^2 - V_{batt,min}^2)} \tag{2.34}$$

2.8 Conclusion

In this Chapter, a single-phase single-cell non-isolated buck-boost PFC converter is studied for e-Rickshaw battery charging application. The battery charger is analyzed and designed to reduce overall size, to bolster up overall efficiency and to offer simpler control. It is operated in DCM to obtain the PFC at AC mains for a wide range of input voltage. The steady-state operation and design have been presented in detail in this chapter. A simple voltage control loop with a single output voltage sensor is used to regulate the output voltage, making the control simple, reliability and robust. The converter realized zero-current turn-on of the switches, and zero diode reverse recovery losses due to its DCM operation. The converter detailed small-signal model using the CIECA approach is presented to support the controller design.

The converter analysis and design are confirmed with the simulation results using PSIM 11.1 software. It is shown that the input currents are sinusoidal and in-phase with the corresponding input voltage specification. An experimental laboratory prototype of 1.0 kW is designed and built to further validate the simulation results. The experimental results are in good agreement with the simulation results and validating the converter analysis and design. High efficiency of 93.5 % (> 90 %) and an input current THD of 4.25 % (< 5 %) are documented at rated output power with the developed laboratory prototype. The converter has a high power factor of 0.9990 which makes it suitable for battery charging applications.

The next chapter proposes a new bridgeless AC-DC front-end converter for EV charging application for achieving high efficiency.

CHAPTER 3: SINGLE-PHASE SWITCHED MODE BRIDGELESS AC-DC BUCK-BOOST DERIVED CONVERTER

3.1 Introduction

The converter configuration discussed in Chapter 2 is a single-stage configuration which is easy to develop, and requires minimum number of active and passive devices, However, such converters require high current rated semiconductor devices, leading to increased thermal requirement. Moreover, as the application demands high current at the output, output capacitors are bulky due to second order current ripple leading to increased weight and reduced reliability. Two-stage converters are highly advantageous in low voltage charging applications as output current of the first stage is low thus requiring low value dc-link capacitors. Even though number of active and passive components are more, lower circulating currents reduce the thermal management issues leading to overall reduction in size. The conventional front-end converter employs a diode-bridge rectifier along with a boost converter for PFC. This front-end converter is the most complex and lossy part because of its high semiconductor count. Reference [44] identifies that the bridge rectifiers are accountable for a sizable part of conduction losses in any frontend PFC converters. Therefore, to eliminate the diode bridge rectifiers for improved efficiency and reduced losses, bridgeless topologies are implemented [45]-[47]. The bridgeless topologies eliminate the use of input diode bridge and mostly comprises of boost or boost derived topologies to achieve the desired high voltage output and considered for battery charging applications. In this Chapter, an elaborative discussion on the limitations of state-of-the-art available bridgeless boost topologies in EV charging application is reported. Established on this understanding, a new single-phase switched-mode bridgeless AC-DC buck-boost derived converter topology as a front end converter is proposed, analyzed, and designed in detail.

3.2 Review of Front End Bridgeless AC-DC PFC Topologies

Bridgeless boost topology, semi-bridgeless, bridgeless interleaved boost PFC topology, bridgeless buck-boost PFC topology as well as bridgeless Sepic and Cuk PFC topologies are reviewed for application in ac-dc PFC stage for EV battery charging applications.

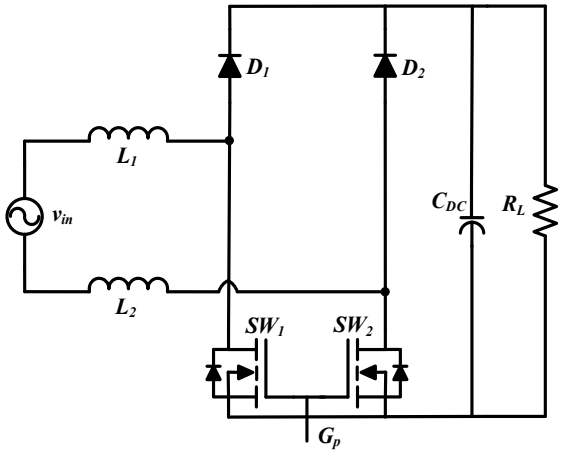


Fig. 3. 1. Bridgeless boost PFC converter

3.2.1 Bridgeless Boost PFC Converter

Fig. 3.1 shows the schematic of the bridgeless boost PFC converter. The bridgeless boost PFC topology eliminates the requirement of the diode rectifier at the input side however upholds the traditional boost topology features. Consequently, the loss associated with the diode rectifier bridge is reduced, making it suitable up to kW where the need for high power density and efficiency is a major concern. The converter resolves the issues of heat management at the input side but raises the concern of high EMI [48]. The floating input line makes it impossible to sense the input voltage without a low-frequency transformer or an optical coupler. In order to sense the input current, a complex circuit is necessary to sense the current through the MOSFET and diode separately [49], [50]. The topology also generates high common-mode noise than other bridgeless topologies.

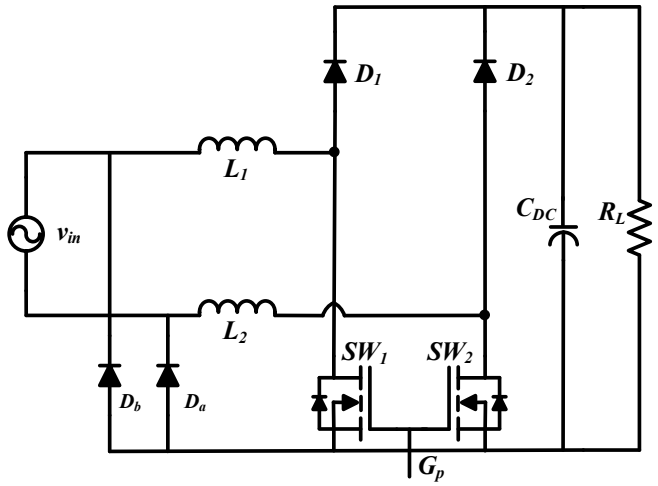


Fig. 3. 2. Semi-bridgeless boost PFC converter

3.2.2 Semi-Bridgeless Boost PFC Converter

Fig. 3.2 shows the schematic of the Semi-bridgeless boost PFC converter. The topology contains two slow diodes namely D_a and D_b. These diodes address the EMI issue at the input side as the current does not always return on this path and it also resolves the issue of floating ground. The conduction losses are very low in the converter. However, the converter control and current sensing are complex and expensive as it requires either three current transformers or the use of Hall Effect sensors and can also be measured by a differential amplifier. The efficiency is significantly improved at light load as compared to traditional bridgeless boost PFC topology. However, this topology does not achieve high full-load efficiency since there is high power loss in the MOSFETs due to high intrinsic body diode losses [51], [52].

3.2.3 Bridgeless Interleaved Boost PFC Converter

Fig. 3.3 illustrates the schematic of a bridgeless interleaved boost PFC topology. In comparison to the bridged interleaved boost PFC topology, it introduces two additional switches and trades bridge diodes with two fast diodes. The gating signals are 180^0 out of phase, similar to the interleaved boost PFC topology. The converter demonstrates a high input power factor, high efficiency, and low input current harmonics. The topology requires a small EMI filter at the input side and exhibits a low capacitor ripple. Converter consisting of four diodes, four switches, and four inductors and is used for power level above 3.3kW.Hence, the topology has the highest number of the components' count than any other bridgeless PFC

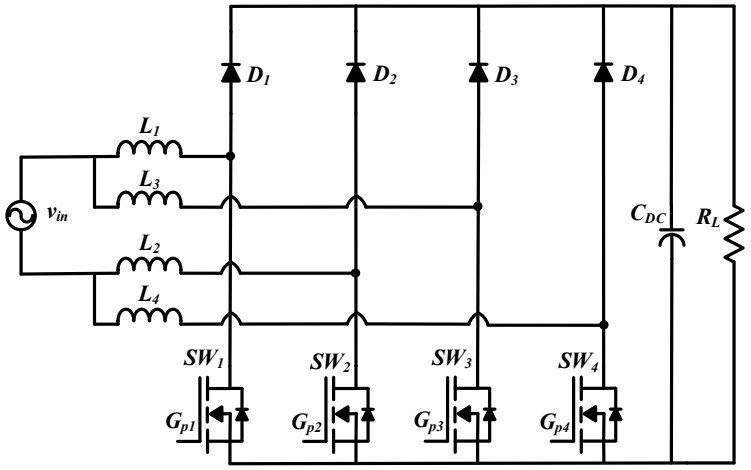


Fig. 3. 3. Bridgeless Interleaved Boost PFC converter

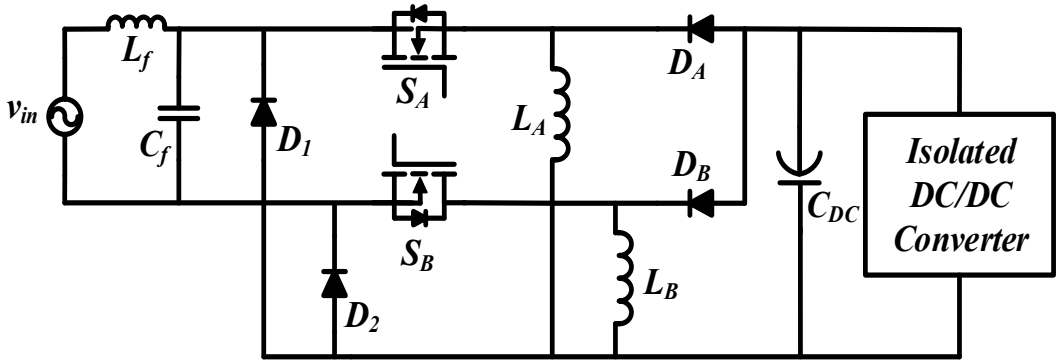


Fig. 3. 4. Single phase bridgeless buck-boost PFC converter

topology making it costly and bulky in size for practical usage with complex control strategies [53], [54].

3.2.4 Bridgeless Buck-Boost PFC Converter

Fig. 3.4. illustrates the schematic of a single-phase bridgeless buck-boost PFC topology serving as a front end for a two stage EV battery charger. The front end converter uses two series connected buck-boost converter operating in positive and negative half line cycle to maintain constant intermediate DC link voltage using the voltage follower mode control. The converter utilizes discontinuous operation of inductors L_A and L_B with voltage follower mode control to afford a wide variation in line voltage over one complete switching period. However, the converter consist of two line diodes, two high frequency diodes, two switches, and two inductors for its operation. This increases the conduction losses, moreover the converter provides negative voltage at the output. The voltage stress on the switches is $V_{in} + n * V_o$. During one switching cycle, one switch and two diodes are in the current flowing path. This increases the conduction loss substantially thus raising thermal management issues [55].

3.2.5 Bridgeless Sepic and Cuk PFC Converter

Fig. 3.5 (a) and (b) show the schematic of the bridgeless PFC circuits derived from the Sepic and Cuk topologies respectively. The topologies are formed by connecting two dc–dc Sepic or Cuk converters, one for each half-line cycle of the input voltage. The input ac line voltage is always connected to the output ground through the slow-recovery diodes D_p and

D_n. Thus, the topologies do not suffer from the high common-mode EMI noise emission problem. Each topology utilizes two power switches (Q_1 and Q_2), two low-recovery diodes (D_p and D_n), and a fast diode (D_o). Passive components' count increases due to the presence of the intermediate capacitor which leads to reduced power density. Also, there is one switch and two diodes in the current conduction path; hence, the conduction losses as well as the thermal stress on the semiconductor devices are further increased. Moreover, the structure of the proposed topologies utilizes one additional inductor compared to the conventional topologies which consequently increases the size and cost of the converter. The converter operation is limited to low-power applications (< 300 W). The bridgeless sepic converter demonstrates high output and input ripple current. The voltage stress on the switches of both the converter are $V_{in} + V_o$ [56].

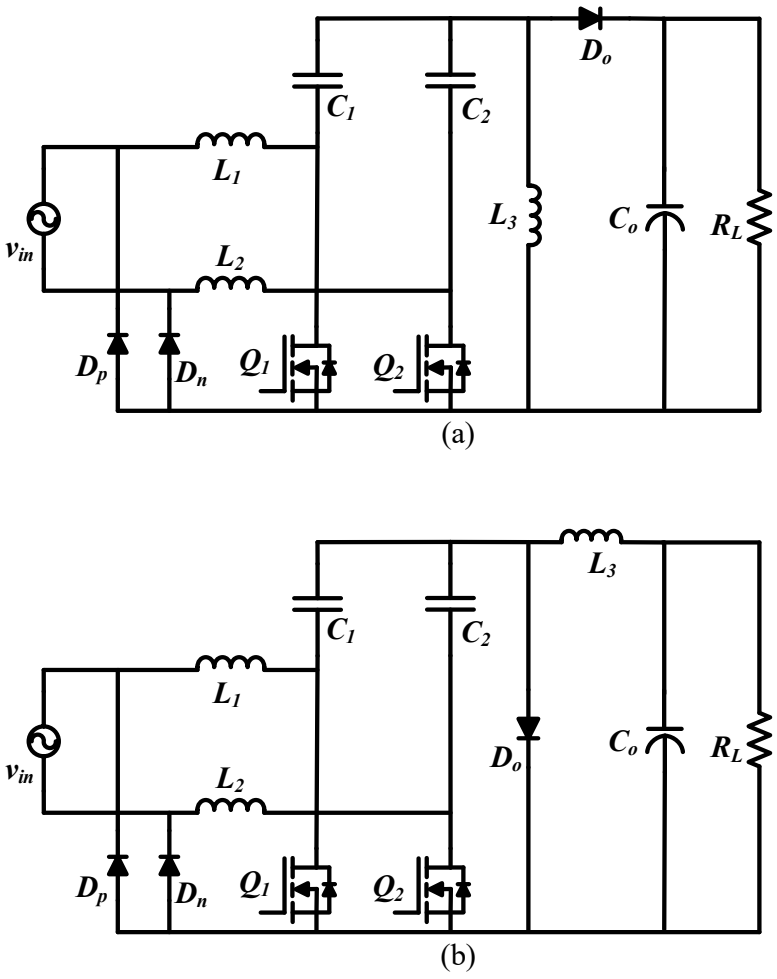


Fig. 3. 5. Converter configuration (a) Bridgeless Sepic, (b) Bridgeless Cuk

As the present bridgeless topologies are operated in CCM, input voltage and current sensing are required in order to implement PFC. Moreover, the same topologies can be extended to DCM, which don't require input sensing, but have control complications due to the boost structure. The input current expression $i_{in}(t)$ for a bridgeless boost can be given as

$$i_{in}(t) = \begin{cases} \dfrac{V_{in}}{L}t, & 0 < t \leq t_{on} \\ \dfrac{(V_{in} - V_o)}{L}t, & t_{on} < t < T_s \end{cases} \tag{3.1}$$

Where, V_{in} and V_o are the input voltage and output voltage. On performing fast Fourier transform (FFT) analysis of input current for one switching cycle using (3.2), we get

$$i_{in}(t) = \frac{a_0}{2} + \sum_{h=1}^{\infty} (a_h \cos(h\omega_{sw}t) + b_h \sin(h\omega_{sw}t)) \tag{3.2}$$

$$a_h = \frac{V_0}{2\pi h}\left(\frac{Dsin(2\pi hD)}{L} + \frac{cos(2\pi hD)}{2\pi h}\right) + \frac{(V_{in} - V_o)}{h\omega_{sw}t}\left(\frac{\cos(2\pi h)}{(2\pi h)^2}\right) \tag{3.3}$$

$$b_h = \frac{V_0}{2\pi h}\left(\frac{-Dsin(2\pi hD)}{L} + \frac{cos(2\pi hD)}{2\pi h}\right) - \frac{(V_{in} - V_o)}{L}\left(\frac{\cos(2\pi h)}{(2\pi h)^2}\right) \tag{3.4}$$

Where D is the duty cycle and L is the converter boost inductance. It is observed that lower-order odd harmonics are present which leads to high input current THD evident from (3.3) and (3.4). Therefore, these converters require complex control and a large input filter, which leads to heavy and low power density converter.

Considering the limitations of the above-mentioned topologies, a new single-phase switched-mode bridgeless AC-DC buck-boost derived PFC converter topology for a front end AC-DC conversion of EV charger has been proposed next. The proposed converter doesn't exhibit traditional THD issues as the inductor is connected to the supply during the switch turn-on period and to the load side during the switch turn-off. Thus, any non-linearity of the output is not transferred to the input, hence a small input filter is enough, which increases the converter power density. The proposed converter is designed to work in the DCM to achieve natural PFC for the variable AC input. This operation expels the sensing of input current, making the converter reliable and cost-effective. The converter control is absolutely simple with the requirement of only one control loop, and a single sensor.

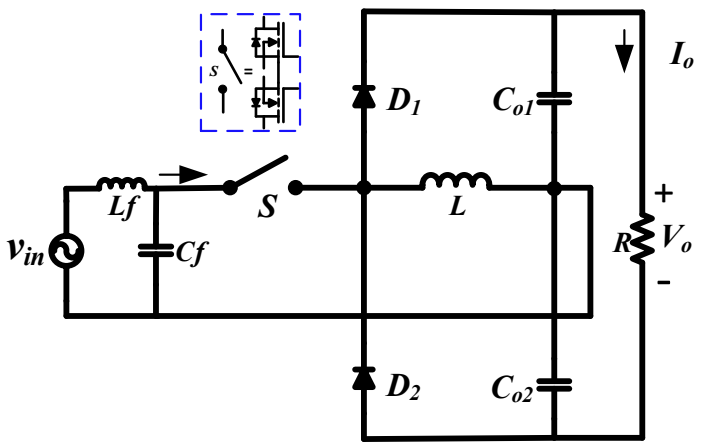


Fig. 3. 6. Proposed single-phase switched-mode bridgeless AC-DC buck-boost derived PFC converter

3.3 Proposed converter and control scheme

Fig. 3.6 shows the proposed single-phase switched-mode bridgeless AC-DC buck-boost derived PFC converter. The proposed converter is derived from the classical buck-boost converter. The diode rectifier is removed from the front end and integrated on the load side in the form of a voltage doubler configuration. The converter embodies two back-to-back connected MOSFETs, two diodes, one inductor, and two electrolytic capacitors. The voltage across the devices is reduced by the DC-split output configuration in the proposed converter, which reduces the switching losses. The back-to-back connected MOSFETs are connected in common source configuration and as they are controlled by the same gate signal, it is considered as a single switch S in the analysis. The buck-boost inductor is designed for DCM operation to realize the inherent PFC at the AC power source. In the DCM operation of the converter, the value of the input voltage determines the amount of energy stored in the buck-boost inductor. Therefore, the average input current inherently trails the input voltage. Fig. 3.7 illustrates the control circuit for the proposed converter. The converter output is controlled by only one control loop and a single sensor. As the controlled variable is DC output voltage, the proposed converter duty cycle is constant for rated output power and input voltage.

The proposed converter demonstrates several advantages likes the reduced number of components as compared to the conventional boost and bridgeless boost converters. Moreover, only one semiconductor device conducts current at a time that significantly reduces the conduction losses benefiting high power conversion efficiency and power density. To validate the performance of the proposed converter, a comparative evaluation with the state-

Table 3.1: Comparison of the proposed converter with the state-of-the art converters

Attributes	Bridgeless Boost	Semi-Bridgeless	Bridgeless Buck-Boost	Bridgeless Sepic	Bridgeless Cuk	Proposed
Output voltage	-ve	+ve	-ve	+ve	+ve	+ve
Line diodes requirement	-	2	2	2	2	-
Switching Devices in operation over one switching cycle	2sw+2D	1sw+2D	1sw+2D	1SW+1D	1SW+1D	2SW or 1D
HF inductors	2	2	2	3	3	1
HF Diode	2	2	2	2	2	2
Intermediate capacitor	No	No	No	Yes	Yes	No
Conduction Loss	High	Low	Medium	High	Low	Low
Switch Voltage Stress	High	Medium	High	High	High	Low

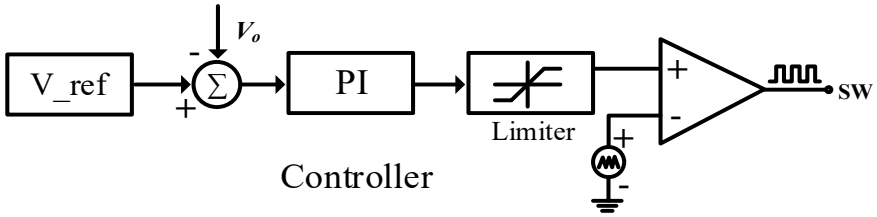


Fig. 3. 7. The control circuit for the proposed converter.

of-the-art front end AC-DC PFC topologies converters is provided in Table 3.1. In all the above state-of-the art converters it is observed that at a given point of time, more than one semiconductor are in the path of current conduction.

The proposed converter also illustrates some additional benefits such as reduced voltage stress of $V_{pk} + \frac{V_o}{2}$ across all semiconductor devices as comparison to a traditional buck-boost converter. The proposed converter achieves PFC over the range of input voltage while maintaining a low THD below 5%. It also maintains a stiff regulated DC voltage. Due to DCM operation, the sensor requirement is reduced to one voltage sensor and avoids the sensing of input current, input voltage and output current sensing.

3.4 Steady-State Analysis of Proposed Converter

The proposed converter only operates in the boost mode in order to reverse bias the output diodes when the switch S is conducting. The equivalent circuit S of operation during positive

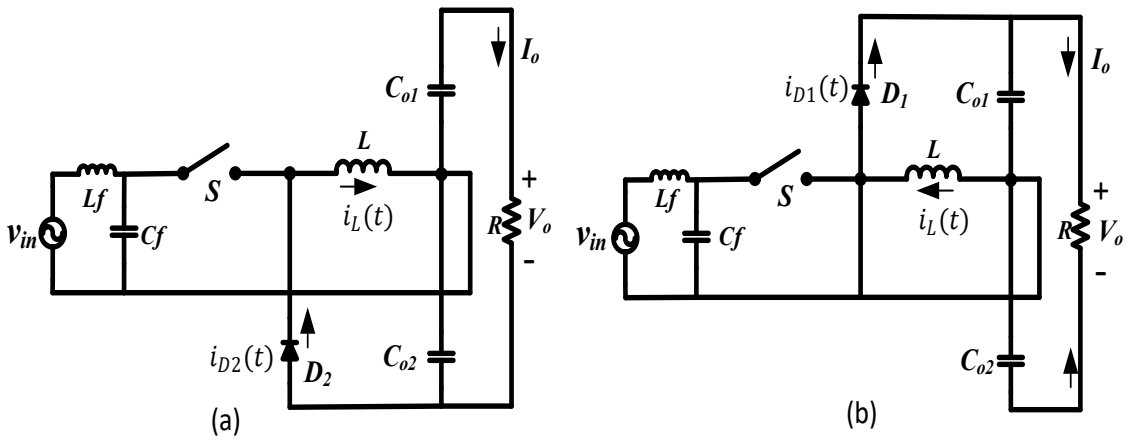


Fig. 3. 8. Proposed converter configurations during (a) positive half cycle, (b) negative half cycle

and negative half-line cycles are shown in Fig. 3.8 (a) and Fig. 3.8 (b), respectively. It must also be taken into account that either the switch S or only one diode (D_1 or D_2) is in the current flowing path, which consequently reduces the conduction losses. The converter is designed to be operated in DCM to achieve natural PFC at AC input. Fig 3.10 shows equivalent circuits of operation during a positive half cycle of input voltage.

The steady-state waveform of the proposed converter for one switching cycle are shown in Fig. 3.9 with the following assumptions.

e) All components are ideal and the input voltage and the output voltage are considered constant within one switching cycle.

f) The output side filter capacitor is large enough to maintain the output voltage constant in one switching cycle.

g) The output capacitors 'C_{01}'and 'C_{O2}' share half-of the output voltage.

1) Mode I:- $(\mathbf{0 < t < t_1'})$

In mode I, switch S is turned on with the gate signalV_g. Inductor L stores the energy and capacitors $C_{01}$and C_{O2} supply power to the load. The expression for the inductor current $i_L(t)$ is given as

$$i_L(t) = \frac{V_{in}}{L} * (\Delta t) \tag{3.5}$$

where, V_{in} = input voltage.

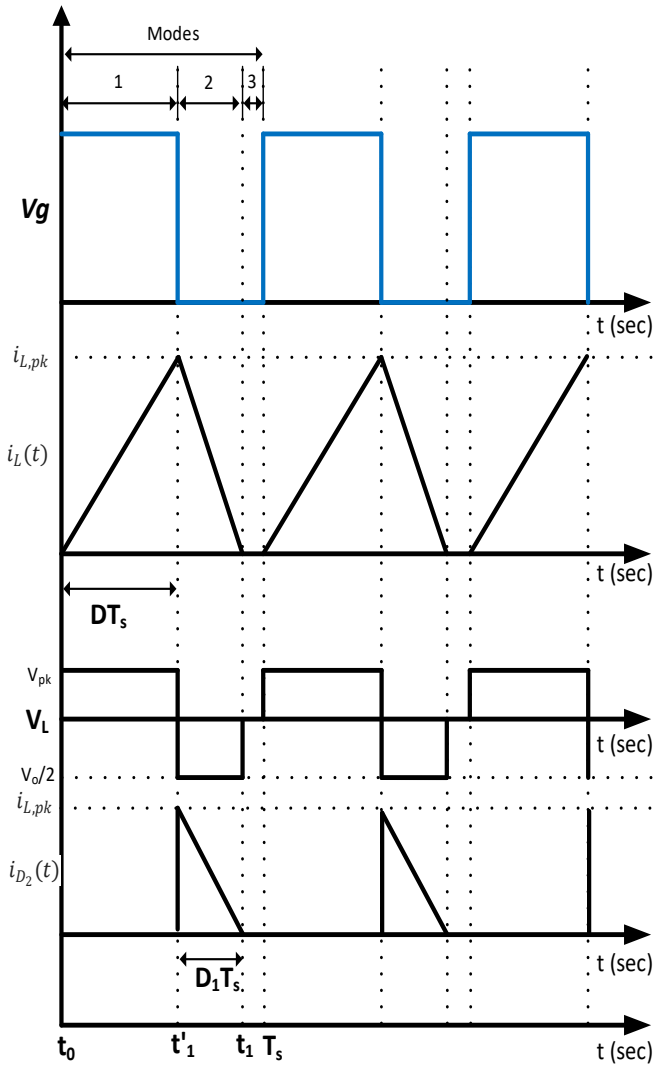


Fig. 3. 9. Waveforms for one switching cycle

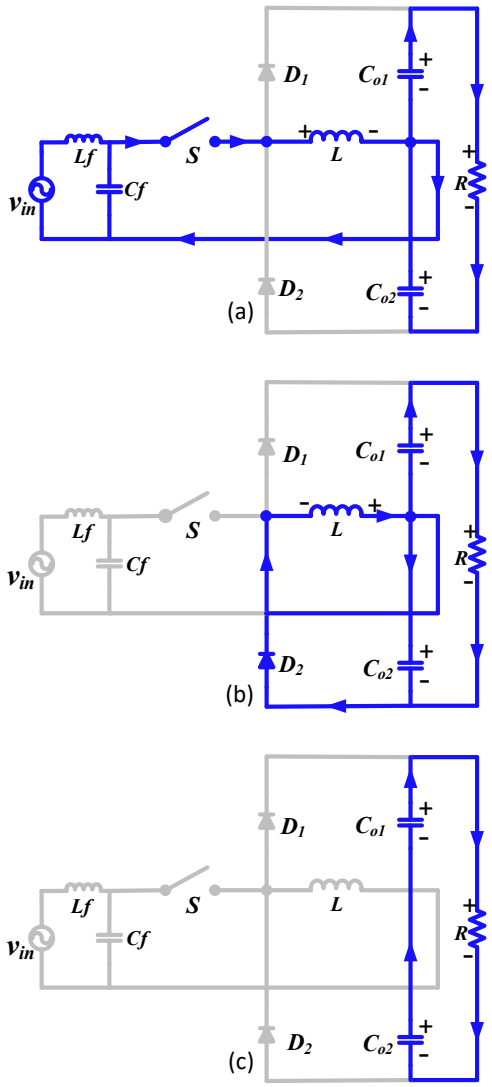


Fig. 3. 10. Equivalent circuits during positive half-cycle; (a) Mode-a; (b) Mode-b; (c) Mode-c.

2) *Mode II:-* $(t_1' < t < t_1)$

In this mode, the gate signal is removed and switch S is turned off. The inductor L starts demagnetizing by delivering the stored energy to the load while the capacitor C_{O2} gets charged. The expression for the inductor current $i_L(t)$ is given as

$$i_L(t) = i_{L,pk} - \frac{V_o}{2L} * (\Delta t) \tag{3.6}$$

where $i_{L,pk}$ is the peak inductor current given by

$$i_{L,pk} = \frac{V_{in}}{L}(DT_s) \tag{3.7}$$

where, DT_s=switch on-time.

This mode ends when the current through the diode D_2 is zero, that implies

$$D_1 T_s = \frac{2V_{in}}{V_o} DT_s \tag{3.8}$$

where, $D_1 T_s$=diode conduction time.

3) Mode III:- $(t_1 < t < T_s)$

In this mode, all semiconductor devices are in off state and capacitors C_{o1} and C_{o2} supply power to the load.

3.5 Proposed Converter Design

This section presents the expressions for converter average output current and input current and derives the DCM condition and the design equations for each passive component.

3.5.1 Average Output Current

The current supplied to the load is nothing but the average diode D_1current $i_{D_2,avg}$ in the positive half-line cycle. Since the current is triangular in shape, its average can be given as

$$i_{D_2,avg} = \frac{i_{L,pk} D_1 T_s}{2T_s} \tag{3.9}$$

Substituting (3.7) and (3.8) in (3.9), the average output current for one switching cycle can be given as

$$i_{o,avg} = \frac{i_{D_2,avg}}{2} = \frac{V_{in}^2 D^2 T_s}{2LV_o} \tag{3.10}$$

Where D=duty cycle and V_o= output voltage.

Thus the average diode current $I_{D_2,avg}$ for half-line period can be defined as

$$I_{o,avg} = \frac{1}{2\pi} \int_0^{\pi} i_{D_2,avg} d\omega t \tag{3.11}$$

$$I_{o,avg} = \frac{V_{pk}^2 D^2 T_s}{4LV_o} \tag{3.12}$$

3.5.2 Input Current

The input current expression of the proposed converter for one switching cycle can be defined as

$$I_{in}(t) = \begin{cases} \frac{V_{in}}{L} t, & 0 < t \leq t_{on} \\ 0, & t_{on} < t \leq T_s \end{cases} \tag{3.13}$$

On performing FFT of (3.16) using (3.2)

$$a_0 = \frac{V_{in}}{L} D^2 T_s \tag{3.14}$$

$$a_h = \frac{V_{in}}{L}\left(Dsin(2\pi hD) + \frac{1}{2h\pi}\cos(2\pi hD) - \frac{1}{2h\pi}\right) \tag{3.15}$$

$$b_h = \frac{V_{in}}{2\pi h f_{sw} L}\left(\frac{sin(2\pi hD)}{2h\pi} - Dcos(2\pi hD)\right) \tag{3.16}$$

On substituting $V_{in} = V_{pk}\sin(\omega t)$ in (3.14) the fundamental component of the input current is obtained (3.15) and (3.16) shows the switching order harmonics, which needs to be filtered out. Respective comparison of (3.3) and (3.4) with (3.15) and (3.16), it is noted that unlike conventional boost converter the proposed converter does not inject harmonics in the input and thus requires a relatively small filter. By designing a low-pass LC filter with a cut-off frequency much lower than the switching frequency, the harmonic currents can be filtered out. Therefore, the resulting input current contains only the fundamental current component, and it can be obtained by applying power balance expression (3.13). The input current can be found by,

$$V_{in} I_{in} = V_o i_{o,avg} \tag{3.17}$$

Substituting (3.10) in (3.13)

$$V_{in} I_{in} = \frac{V_{in}^2 D^2 T_s}{2L} \tag{3.18}$$

$$I_{in} = \frac{V_{in} D^2 T_s}{2L} = \frac{V_{pk} D^2 T_s}{2L}\sin(\omega t) = I_{pk}\sin(\omega t) \tag{3.19}$$

Where, $I_{pk} = \frac{V_{pk} D^2 T_s}{2L}$ peak input current.

Equation (3.19) shows that the filtered input current is sinusoidal and is in phase with the input voltage, which proves the UPF operation of the converter.

3.5.3 DCM Operation and Critical Conduction Parameters

Following inequalities must hold for DCM operation which is given as

$$DT_s + D_1T_s < T_s \tag{3.20}$$

On substituting (3.8) in (3.20)

$$D < \frac{M}{(M + 2\sin(\omega t))} \tag{3.21}$$

Where, $V_{in} = V_{pk}\sin(\omega t)$, $M = V_o/V_{pk}$.

In (3.21), the worst case occurs at $\omega t = 1$, thus by substituting $\omega t = \frac{\pi}{2}$ in (3.21) the condition to operate the converter in DCM is given as,

$$D < \frac{M}{(M + 2)} \tag{3.22}$$

From (3.22), the critical value of voltage conversion ratio M_{cric} for a given duty cycle can be defined and is given as,

$$M_{cric} < \frac{2D}{(1 - D)} \tag{3.23}$$

Output current is given as

$$I_o = \frac{V_o}{R} \tag{3.24}$$

Substituting (3.12) in (3.24),

$$D = M\sqrt{2K_{cond}} \tag{3.25}$$

where K_{cond}=conduction parameter of the converter

$$K_{cond} = \frac{2L}{RT_s} \tag{3.26}$$

From (3.22) and (3.25), critical conduction parameter K_{cric} can be calculated as

$$K_{cric} = \frac{1}{2(M + 2)^2} \tag{3.27}$$

3.5.4 Inductor Design

To maintain PFC under all conditions, the inductor current needs to be in DCM for the worst-case input voltage. The DCM inductor can be computed by using (3.12) and (3.22) and is given by

$$L < \frac{{V_{pk}}^2 {V_o}^2 T_s}{4P_o\left(V_o + 2V_{pk}\right)^2} \tag{3.28}$$

3.5.5 Design of Output Capacitor

In a single-phase PFC rectifier, the output capacitors are designed to filter out the second order supply frequency oscillations present in the output voltage. The output ripple is caused by the unbalanced instantaneous power between input and output. Therefore, capacitors are designed to buffer this unbalanced power and filter out oscillations. Thus, by considering $C_{o1} = C_{o2} = C_o$, the low-frequency output voltage ripple $V_{o,ripple}$ is given as

$$\Delta V_{o,ripple} = \frac{1}{C_o}\left(\int i_{co1}dt + \int i_{co2}dt\right) \tag{3.29}$$

$$= \frac{1}{C_o}\int (i_{D1} - 2i_o)dt = \frac{2i_o}{\omega C_o} \tag{3.30}$$

$$C_o = \frac{2I_o}{\omega V_{o,ripple}} \tag{3.31}$$

3.5.6 Input Filter Design

The criteria to design a low-pass LC filter is as follows:

3. Selection of cut-off frequency f_c given by

$$f_c = \frac{1}{2\pi}\sqrt{\frac{1}{L_f C_f}} \tag{3.32}$$

4. Minimization of filter reactive power consumption for 60 Hz at 1.0 kW. The reactive power is minimum when filter characteristic impedance is equal to the converter impedance i.e.

$$Z_{ch} = \sqrt{\frac{L_f}{C_f}} = Z_{in} \tag{3.33}$$

where, Z_{ch} is the characteristic impedance and Z_{in} is the input impedance at rated load and is given by

$$Z_{in} = \frac{2L}{D^2 T_s} \tag{3.34}$$

Using (2.32) and (2.33), low-pass filter parameters L_f and C_f can be obtained as

$$L_f = \frac{Z_{ch}}{2\pi f_c} \tag{3.35}$$

$$C_f = \frac{1}{2\pi Z_{ch} f_c} \tag{3.36}$$

3.6 Proposed Converter Small-Signal Model

Traditional front-end converters of battery chargers use complex control which requires input voltage and current sensing along with PLL. Such systems pose a higher burden on microcontroller as more computation speed is required. The proposed converter mitigates these problems by eliminating the input sensing and just use one sensor to control the output as shown in Fig. 3.7 (b). The small signal model of the proposed converter is obtained by using the current injected equivalent circuit approach (CIECA) [42], [43]. This approach is better than the conventional state-space averaging approach as it becomes cumbersome and

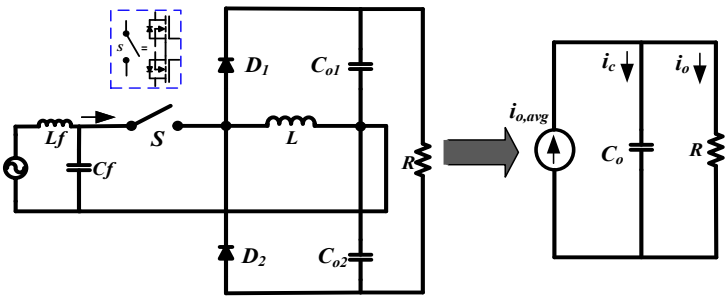


Fig. 3. 11. Equivalent circuit for small signal modelling

complex in DCM. Such complex models are tough to derive even for simple DC-DC based DCM converters [57]. On the other hand, the CIECA approach is much easier as it only models the transfer properties of the converter [42]. In CIECA, the entire circuit can be scaled down as shown in Fig. 3.11. The non-linear parameters of the circuit are linearized by injecting the average output current produced by the non- linear part. From Fig. 3.11(a)

$$\hat{\imath}_{o,avg} = \left(sC + \frac{1}{R}\right)\hat{v}_o \tag{3.37}$$

On applying perturbations in (3.12) we get

$$\hat{\imath}_{o,avg} = \frac{V_{pk}^2 D T_s}{2LV_o}\hat{d} + \frac{V_{pk} D^2 T_S}{2LV_o}\hat{v}_{pk} - \frac{i_{o,avg}}{V_o}\hat{v}_o \tag{3.38}$$

On equating (3.37), (3.38) and substituting $\hat{v}_{pk} = 0$

$$\frac{v_o(s)}{d_o(s)} = \frac{V_{pk} D}{K_{cond} M(sRC + 2)} \tag{3.39}$$

Where, $C = \frac{C_{o1}C_{o2}}{C_{o1}+C_{o2}}$, $M = \frac{V_o}{V_{pk}}$, and R =load resistance.

The converter control to output transfer function is obtained by substituting the design parameters in (3.39). As the transfer function is a single-pole system, a simple PI controller $\left(K_p + \frac{K_i}{s}\right)$ is used to control the output voltage as shown in Fig. 3.7 (b). As the output capacitor sees a voltage ripple of twice the line frequency, a PI controller with bandwidth lower than the 120Hz is selected with a Phase Margin (PM) of 60^0. The controller is tuned using sisotool in Matlab and the controller parameters are computed as $K_p = 0.00252$ and $K_i = 0.21$. The output voltage is sensed using a hall-effect based LV-25P sensor. The sensed voltage is compared with the reference voltage and error is fed into the PI controller. The PI controller generates the duty cycle to control switch S. A limiter is connected in order to limit the duty during start-up and overload conditions.

3.7 Result and Discussion

This section presents the simulation and experimental results of the proposed converter to validate the converter analysis and design and demonstrates its performance.

3.7.1 Simulation Results

The proposed converter is simulated in PSIM 11.1 software to confirm the converter analysis and the design. The converter design specifications are given in Table 3.2. The buck-boost inductance value is calculated from (3.28). The output filter capacitances values are calculated from (3.31). Using the designed parameters, the converter control-to-output transfer function is obtained from (3.39) and is given in (3.40). A PI-controller transfer function is designed for Phase Margin of 60^0 a bandwidth of 628.31 rad/sec. It determines $k_p = 0.00252$ and time constant $\tau = 0.012$ controller is designed and implemented.

$$\frac{v_o(s)}{d(s)} = \frac{1282.584}{1 + 0.032s} \tag{3.40}$$

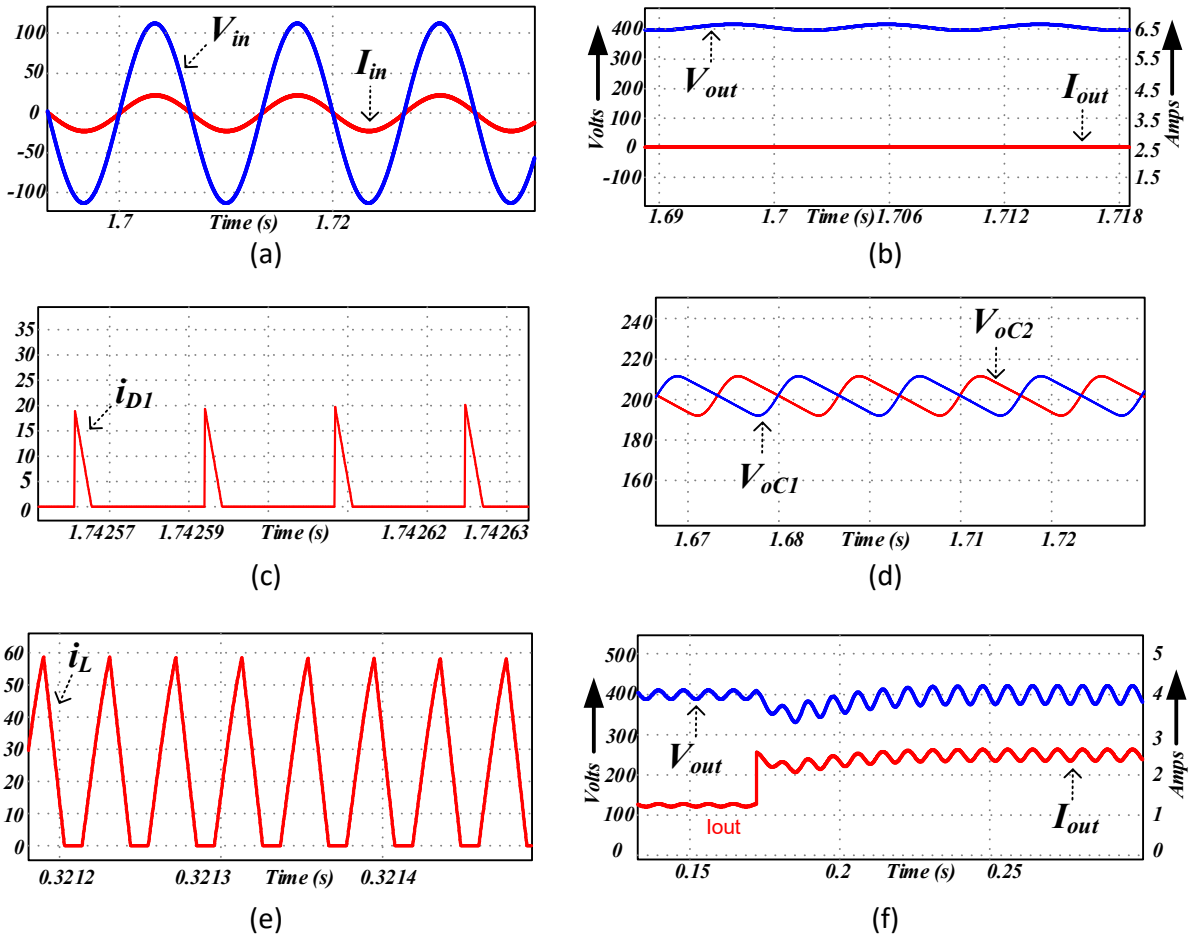


Fig. 3. 12. Simulation results (a) input voltage and input current; (b) output voltage and output current; (c) output diode $Do1$ current; (d) output capacitors voltages; (e) inductor current; (f) converter response for load change 50 % to 100 %.

Table 3.2: Converter design specifications.

Parameter	Value
Line voltage, $\boldsymbol{V_{in}}$ $\boldsymbol{RMS}$	110 $V_{RMS\ nominal}$
Input frequency, $\boldsymbol{f}$	60 Hz
Output power, $\boldsymbol{P_o}$	1.0 kW
Output voltage, $\boldsymbol{V_o}$	400 V
Switching frequency, $\boldsymbol{f_{sw}}$	50 kHz
Duty cycle, $\boldsymbol{D}$	0.638
Buck-Boost Inductance, $\boldsymbol{L}$	24.45 µH
Output capacitance, $\boldsymbol{C_{o1}, C_{o2}}$	82.4 µF
Output voltage ripple, $\boldsymbol{V_{o,ripple}}$	5% of output voltage (V_o)

With the designed parameters and the designed controller, the circuit is simulated, and the results have been presented for input frequency f = 60 Hz. The simulated input voltage and input current waveforms are shown in Fig. 3.11(a). The output voltage and output current are shown in Fig. 3.11(b). The output diode 'D1' current waveform is shown in Fig. 3.11(c), which is discontinuous, and validates the converter design. The voltages across output capacitors are shown in Fig. 3.11(d). Each output voltage capacitor is sharing half-of the output voltage, which is in good agreement with the analysis. The inductor current waveform is shown in Fig. 3.11(e). The output voltage and input current waveforms when the converter subjected to a load disturbance from 50% to 100% of the rated power are shown in Fig. 3.11(f). The controller responds immediately to the load change, and the output voltage is settled at reference value 400 V.

Table 3.3: Converter hardware specifications.

Components	Specifications
MOSFET	UF3C120040K4S, SIC 1200V, 45mohm
Diode	RURG80100,1000V, 80A
Input filter capacitor $\boldsymbol{C_f}$	0.22 µF*10, 480 VAC, R76QR32204030J
Input filter inductor $\boldsymbol{L_f}$	371µH, 42 x 21 x 20, EE Ferrite Cores
Output filter Cap	82.4 µF*10*2, 450 VDC, UPZ2W820MHD
Buck-Boost Inductor	24.45µH, 42 x 21 x 20, EE Ferrite Cores
DSP	DSP-TMS320F28335
Gate Driver	Gate Driver IC, IXYS-IXDN609SI

3.7.2 Experimental Results

To validate the analysis of the proposed converter and to verify the simulation results, a 1.0 kW proof-of-concept laboratory hardware prototype has been built for the same specification and design parameters used in the simulation. The hardware details are given in Table 3.3. The DSP TMS20F28335 is employed as a digital control platform to generate the gate signals for the converter. The hall-effect sensor LV-25P is employed to sense the converter output voltage. Fig. 3.13(a) and Fig. 3.13(b) show the top and side views of the experimental set-up respectively. The converter nominal input voltage of 110 V RMS is been selected as per voltage-levels available in the lab. An approximate variation of 25% in input voltage has been considered to validate the converter PFC operation. The output voltage of 400 V is selected by considering the voltage

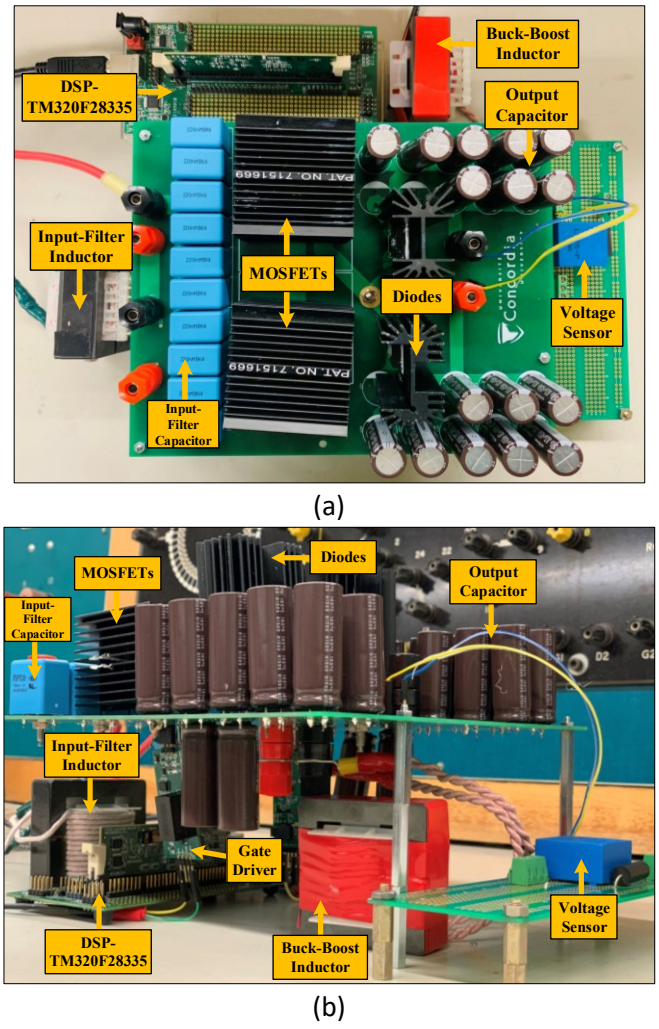


Fig. 3. 13. Experimental prototype of bridgeless converter (a) top view. (b) side view.

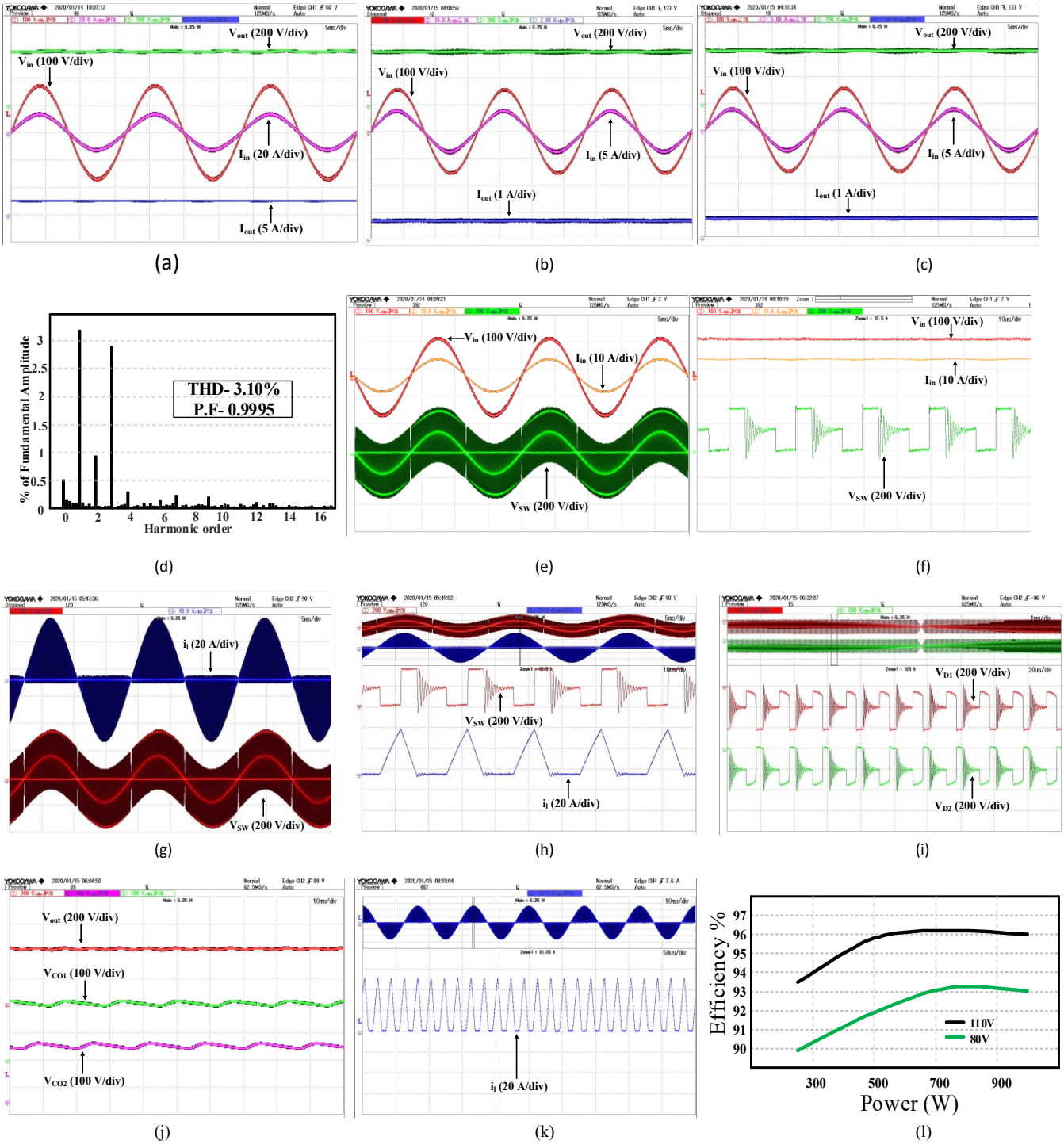


Fig. 3. 14. Experimental results (a) PFC operation at 1.0 kW. (b) PFC operation at 500W. (c) PFC operation at 250W. (d) Input current THD at 1.0 kW. (d) THD and power factor at various power levels. (e) Switch voltage waveform along with PFC. (f) zoomed in version for switch voltage waveform. (g) Switch voltage and inductor current (g) ZCS turn-on of switch. (h) Diode voltage waveform. (j) Output capacitor voltage. (k) Zoomed in Inductor waveform at 1.0 kW. (l) Efficiency curve for various power levels.

margins for output capacitors [12]. The input filter parameters L_f and C_f are calculated for a cut-off frequency of 6 kHz. Fig. 3.14(a), Fig. 3.14(b) and Fig. 3.14(c) show that the input current is purely sinusoidal and in-phase with the input voltage, thus achieving PFC at 1.0 kW, 500W and 250W, respectively. Fig. 3.14(d) shows the input current FFT analysis where the input current THD of 3.10% (<5%) at 1.0 kW with a power factor of 0.9995. Fig. 3.14(e) shows the input voltage and input current along with the voltage across back to back connected switches. Fig. 3.14(f) shows the zoomed version of Fig. 3.14(e) where the maximum switch voltage stresses are 360V which is approximately equal to $V_{pk} + \frac{V_o}{2}$ thus shows a good agreement with the analysis. Inductor charging and switch blocking state are shown in Fig. 3.14(g). Fig. 3.14(h) shows the zoomed version of Fig. 3.14(g), the inductor current and switch waveform at 500W output power where inductor current is zero before turn-on confirming ZCS turn-on of switch S. Fig. 3.14 (i) shows the diode voltage waveform with maximum voltage stress of 380V. It is seen that during one-half cycle only one diode conducts whereas another the diode is completely in the blocking state. Fig. 3.14(j) shows capacitor voltages $V_{C_{01}}$ and $V_{C_{02}}$. It is observed that both capacitors are sharing voltage equally. Fig. 3.14(k) shows

Table 3.4: Converter measured input current THD (%) and power factor at different output powers.

Power	THD (%)	Power Factor (PF)
250 W	4.13	0.9991
500 W	3.72	0.9993
750 W	3.45	0.9994
1000 W	3.10	0.9995

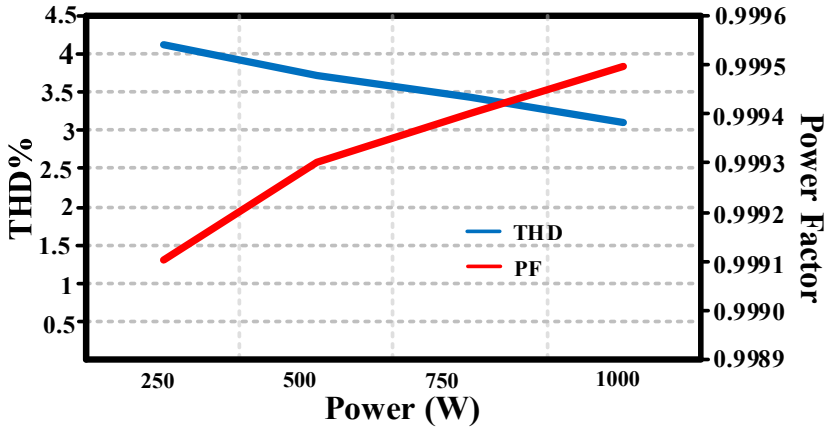


Fig. 3. 15. THD and power factor at various power levels

the inductor current waveform at 1.0 kW where the inductor current is discontinuous confirming the converter DCM operation of the inductor. The measure efficiency curve of the proposed converter for different output powers is shown in Fig. 3.14(l).

The input current THD (%) and PF for different output power levels at 60 Hz input frequency is plotted and is shown in Fig. 3.15. It is observed that input PF is almost unity (0.999) with a THD less than 5% for output powers variation. Table 3.4 describes the converter measured input current THD (%), and PF at different output power. Fig. 3.16(a) and Fig. 3.16(b) show two load disturbances from 500W to 1.0 kW and from 1.0kW to 500W respectively. In both cases, it is observed that the output voltage closely tracks the reference voltage and is getting settled in the design time of 20 ms. To confirm the UPF operation for line voltage variation, it is subjected to 25% line voltage dip and swell conditions. Fig. 3.16(c) and Fig. 3.16(d) show the converter response for input voltage variation from 80V to 110V and 110V to 80V RMS, respectively. It is observed that during the voltage swell condition,

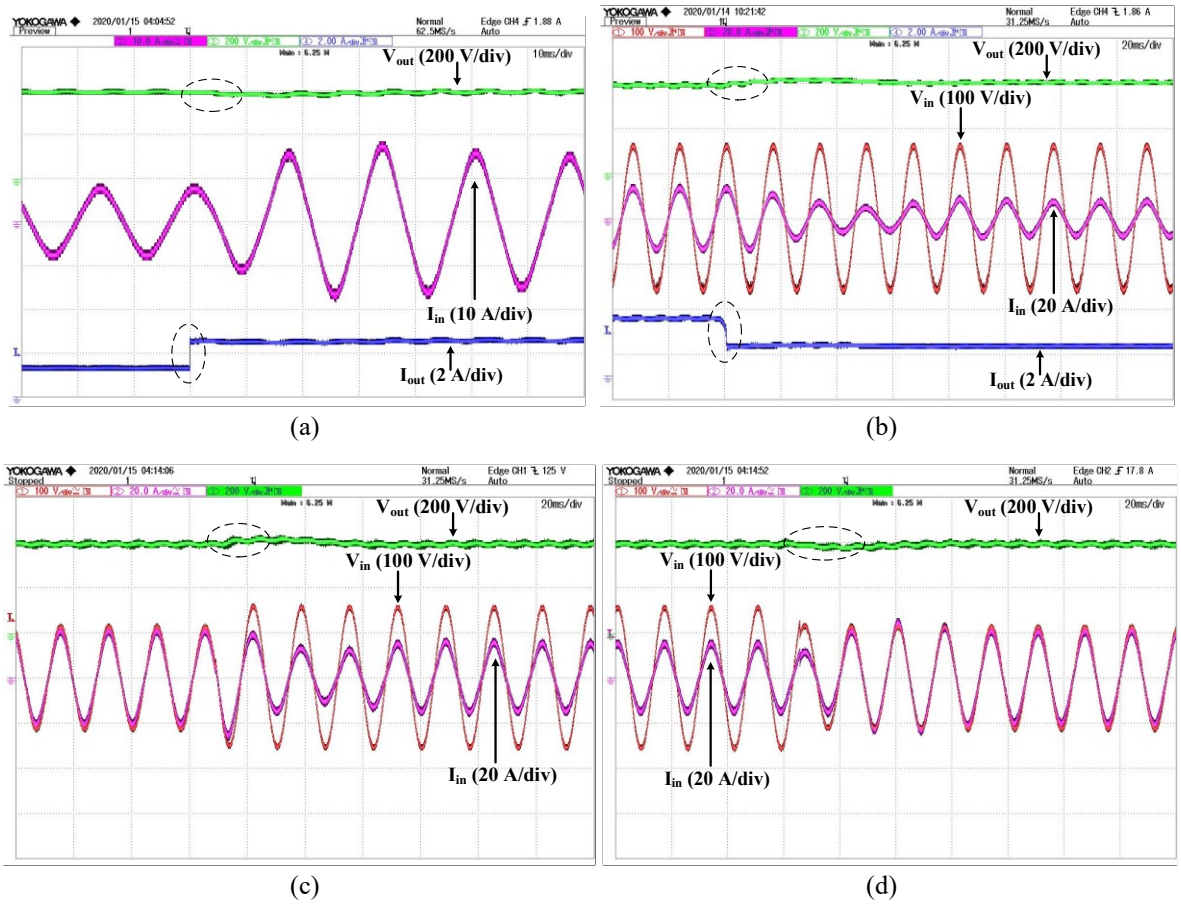


Fig. 3. 16. Converter response (a) load change from 500W to 1.0 kW; (b) load change from 1.0 kW to 500 W; (c) input voltage swell. (d) Input voltage dip

the input current is decreased for maintaining the same power. Conversely, the input current is increased for the voltage dip condition at constant power. For both the conditions, input current remains sinusoidal that confirms UPF operation thus validating the inductor design.

3.8 Conclusion

A new single-phase switched-mode bridgeless AC-DC buck-boost derived converter is proposed. The proposed converter serves as a feasible front-end converter for the on-board EV chargers. The proposed converter benefits from a reduced number of components sensors, which further helps in minimizing the charger cost and volume. The converter is operated in the DCM in order to achieve PFC for wide input voltage variation. The PFC control requires one simple voltage control loop to regulate load voltage and a single sensor, which makes the system cost-effective, reliable, and robust. The steady-state operation of the converter and detailed design calculations are presented. The small-signal model of the converter is derived using the CIECA approach. Due to the DCM operation, the converter requires high rated current switches. However, the merits of the proposed converter such as low voltage stress, single sensors, soft turn-on of the switches and control simplicity significantly prevail the disadvantage of high current rated switches. An input current THD of 3.13 % (< 5 %), and a high efficiency of 96 % are recorded at rated output power from the developed laboratory prototype. The experimental results from a 1.0 kW hardware prototype have been presented which validates the converter analysis and design.

The next chapter deals with a two-stage onboard battery charger, including a new bridgeless buck-boost based converter with a lower number of components and with simple control. The second stage consist of an unregulated half-bridge series LLC DC-DC resonant converter which provides isolation as well as soft-switching for primary switches. Synchronous Rectification (SR) is implimented on transformer secondary to improve overall efficiency.

CHAPTER 4: AN ON-BOARD EV CHARGER USING BRIDGELESS PFC AND LLC RESONANT CONVERTER

4.1 Introduction

In previous Chapter, a bridgeless buck-boost derived topology is proposed that can act as a front-end PFC converter for a two-stage battery charger. Isolated DC-DC converters can serve as back-end for controlling charging voltage and current. Even though such configurations are simple to implement, such chargers increases control burden on the microcontroller leading to reduced overall system reliability [17],[19] [20]. Moreover, incorporation of in total of two sensors (dc-link voltage and output voltage) can lead to reduced reliability of the system. Henceforth, a two stage topology should satisfy the following requirements:

1. Simple and reliable control in front-end PFC converter.
2. Good voltage regulation at light load condition
3. Maintain soft-switching over wide load range.
4. Less diode reverse recovery losses and low voltage stress on the diodes.
5. Single sensors should be used in order to implement the control.
6. Modelling of the converter and control should be less complex.
7. Low input current THD should be maintained at different power levels.

By considering the aforementioned points of a two stage isolated on-board battery charger, a new two-stage isolated EV Charger integrating a bridgeless PFC and half-bridge LLC resonant converter has been proposed. In this Chapter, an elaborative discussion on the limitations of state-of-the-art available isolated dc/dc topologies in EV charging application is reported in order to select a suitable back-end for the proposed charger configuration.

4.2 Review of Second Stage Isolated DC-DC Topologies

In the sub-section, four different types of isolated full-bridge dc/dc topologies namely full bridge PWM buck topology, full bridge phase-shift PWM topology, full bridge series resonant topology and full bridge LLC resonant topology are reviewed, analyzed, and compared for EV charging application.

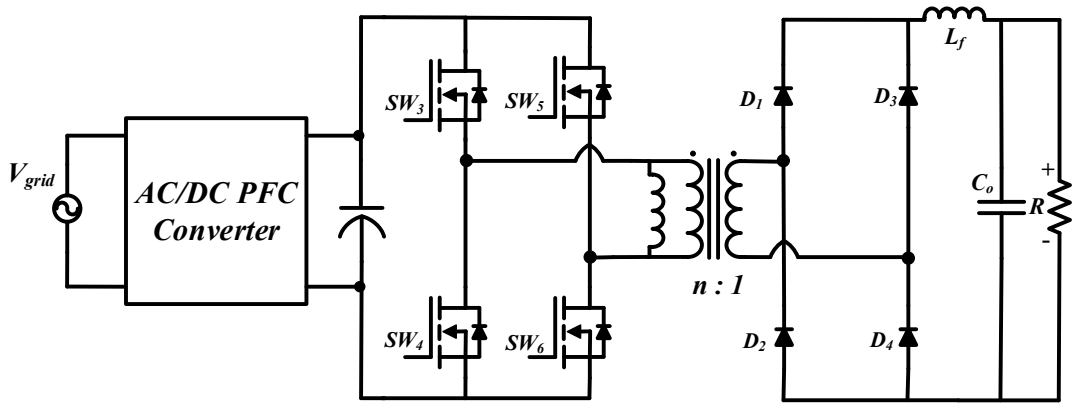


Fig. 4.1. Full-bridge isolated buck converter

4.2.1 Full-Bridge Isolated PWM Buck Converter

Fig. 4.1 shows the schematic of the of full-bridge isolated buck converter. The input and output voltages relation in CCM operation is given by

$$V_{bat} = nDV_{dc} \tag{4.1}$$

Conferring to (4.1), it is easy to control the output voltage by regulating the duty cycle. The voltage gain required by the battery charger is achieved by selecting a proper transformer turns' ratio. While this is an easy topology to implement it has limited ZVS range with duty cycle modulation at fixed frequency. This causes considerable switching losses below rated load that critically constrain the switching frequency. Furthermore, there is also duty cycle loss, diode rectifier ringing along with secondary snubber requirement are key issues with this topology [35].

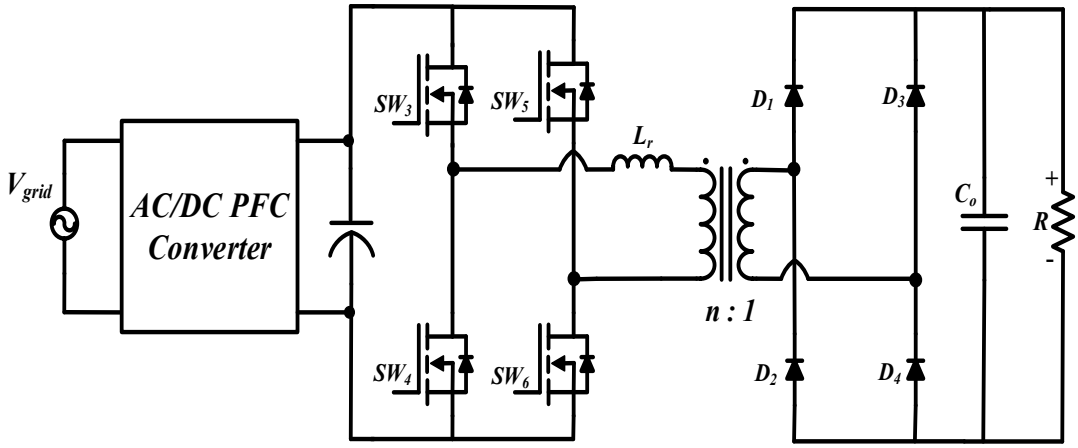


Fig. 4.2. Full bridge phase-shift PWM converter

4.2.2 Full bridge Phase-Shift PWM Converter

Fig. 4.2 shows the schematic of the full bridge phase-shift PWM converter. It is one of the most widely used topologies in medium power range for dc/dc conversion [58]–[62]. In this topology the primary side MOSFETs are turned-on with ZVS and the body diodes are turned-off with ZCS. In addition, control of the full-bridge phase-shift topology is easy to implement in contrast with frequency modulated resonant converter [63]. It offers better ZVS range compared to duty cycle modulation of full bridge isolated PWM buck converter discussed in 4.2.1. In light load condition, there is limited energy stored in Lr making the MOSFETs in the lagging leg lose ZVS features [63]. Moreover, during the time intervals when either both upper switches are on or both lower switches are on, the circulating current is high and causing higher conduction losses. Besides, the commutation of the secondary diodes causes high voltage overshoots and oscillations due to the high voltage of the battery pack. Also, it suffers from duty cycle loss, diode rectifier ringing along with secondary snubber requirement.

4.2.3 Full Bridge Series Resonant Converter

Fig. 4.3 illustrates the schematic of full bridge series resonant converter (FB-SRC). In this converter the switching frequency is higher than the resonant frequency of resonant tank L_r and C_r. The MOSFETs are turned-on with ZVS, and freewheeling diodes are turned-off with ZCS. ZVS is irreverent to different load conditions. One of the most attractive features of FB-SRC is that its circulating losses are relatively low. Moreover, FB-SRC has good short circuit protection performances; short circuit current could be easily regulated by boost the switching frequency [64]. However, the critical defect of FB-SRC lies in its unacceptable poor voltage

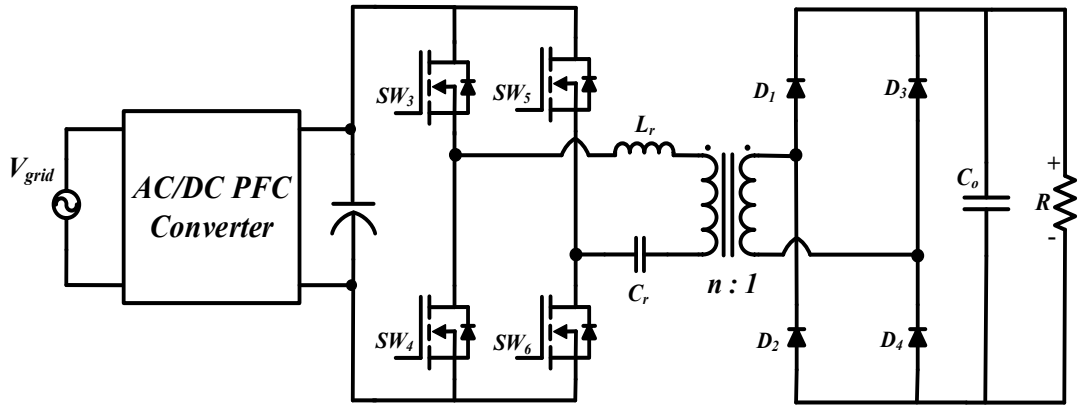


Fig. 4. 3. Full Bridge Series Resonant (FB-SRC) converter

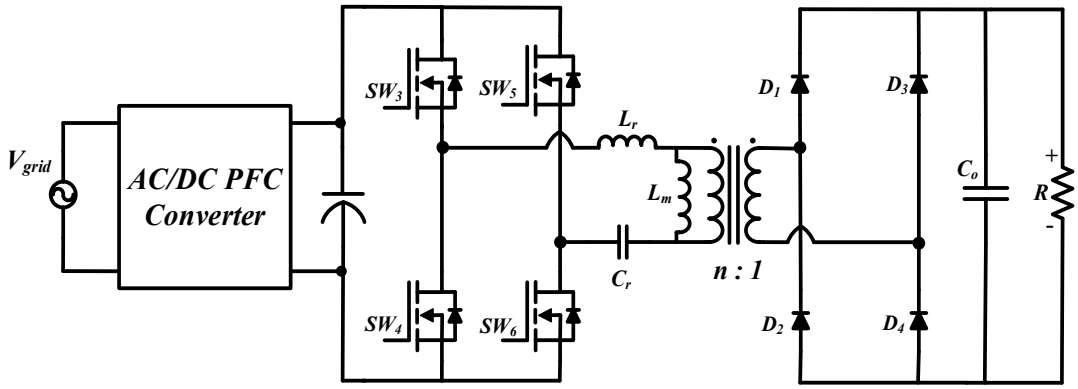


Fig. 4. 4. Full Bridge LLC Resonant Converter

regulation performance at light load condition. Slight perturbation in input voltage causes large scale of frequency shift in addition, frequency modulation control is required to the output voltage. This makes it hard to regulate the voltage and increases the switching losses and conduction losses. Moreover, secondary side diodes are turned off with very high di/dt, which corresponds to big reverse recovery losses. The converter also suffers from high peak current but is free from the problems of duty cycle loss and diode ringing hence, there is no requirement of secondary snubbers.

4.2.4 Full Bridge LLC Resonant Converter

Fig. 4.4. illustrates the schematic of a full bridge LLC resonant converter. This topology has been proved to be one of the most suitable candidates for the dc/dc conversion [65]–[68]. When the input impedance is inductive, turning-on of MOSFETs and turning-off of freewheeling didoes are ZVS and ZCS, respectively. When switching frequency is smaller than f_p, and the input impedance is still inductive, circulating losses of FB-LLC are higher than FB-SRC, but much smaller than full bridge phase shifted (FB-FS). The short circuit performance of LLC is not as good as FB-SRC but still acceptable.

Considering the limitations of the aforementioned topologies, a new two-stage isolated onboard battery charger is presented, utilizing a half-bridge LLC converter with synchronous rectification as back-end converter and bridgeless buck-boost derived converter proposed and analyzed in chapter 3 as front-end stage. Such a configuration utilizes minimum number of semiconductor devices than conventional chargers. Moreover as the second stage is an unregulated half-bridge LLC resonant converter with the implementation of Synchronous

Rectification (SR) on transformer secondary thus improving overall efficiency. Furthermore, loss analysis is done to obtain optimal dc-link voltage and evaluate overall performance.

4.3 Proposed converter and Design scheme

Fig. 4.5 shows the proposed two-stage isolated EV charger topology. In this circuit configuration, a single-phase bridgeless buck-boost converter is used for the front-end PFC, followed by an unregulated half-bridge series LLC resonant converter DC-DC converter.

The front end converter is bridgeless converter analyzed in Chapter 3. It is derived from the traditional buck-boost converter. The converter is operating in DCM mode to achieve natural PFC at AC mains. The front-end converter consist of one bidirectional switch, two diodes, one inductor, and two capacitors (voltage doubler). At the input mains, an LC filter is connected to filter out high frequency switching harmonics and draw pure sine wave current from the source. As the diode bridge rectifier is eliminated and only one semiconductor device is in current flowing path for one switching cycle, the overall conduction losses are reduced significantly. The diode has zero reverse recovery losses along with reduced voltage stress. This reduced voltage stress and conduction losses helps in reduction of overall weight of the proposed charger.

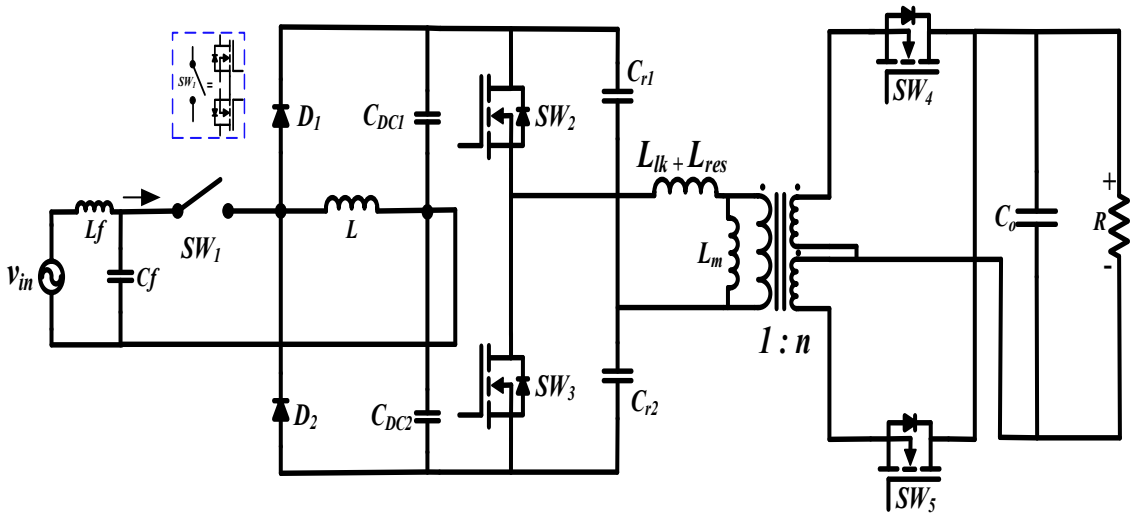


Fig. 4. 5. Proposed two-stage isolated EV charger configuration

Table 4. 1: Comparison of the proposed converter with the state-of-the art converters

Parameters	Full Bridge Isolated Buck	Full Bridge Phase Shift	Full Bridge Series Resonant	Full Bridge LLC Resonant	Proposed
Component Count	High	High	High	High	Low
Active Rectification	No	No	No	No	Yes
Modulation method	PWM	PWM	PFM	PFM	-
Additional filter inductor on secondary side	Yes	No	No	No	No
Short circuit protection performance	Bad	Bad	Moderate	Good	Good
MOSFETs switching losses in normal load	High, hard switching	Low, ZVS	Low, ZVS	Low, ZVS	Low, ZVS
Light load circulating losses	Low	High	Low	Moderate	Low
Light load switching losses	Low	High, ZVS feature lost	Moderate	Low	Low

The second stage is a half-bridge unregulated LLC resonant DC-DC converter to obatin the desired DC voltage of 65V while offering isolation. Synchronous rectification on secondary side is implemented to improve the overall efficiency of the converter. A comparative evaluation with the state-of- the-art back end isolated DC-DC topologies is provided in Table 4.1. that indicates the merits of this topology over the conventional system. Additional merits:

1. Less number of semiconductor device count as the application requires unidirectional flow of high current and low output voltage.
2. LLC resonant tank when reflected to secondary appear as a current source, thus making it suitable for charging applications, along with the capability to achieve ZVS at low loads.

The converter utilizes a center tap transformer along with synchronous rectification on transformer secondary to enhance the overall efficiency and decrease the cost of the charger. The operation of the second stage with a fixed duty cycle and switching frequency helps in reduction of control burden on the microcontroller. Moreover, soft-switching of half-bridge MOSFETs are observed due to resonant tank. Optimal design of resonant tank resulted in reduced peak and circulating current in the back-end converter. In addition, owing to the sinusoidal current through the transformer results in improved transformer utilization.

In the proposed battery charger, the front-end PFC converter concept controls the power transfer and the second stage is always operated at constant switching frequency and duty cycle. Henceforth, it is superior to the traditional converters where first stage is for the active PFC that requires three sensors and second stage to control the charging voltage and current. In the absence of the feedback control, the DC-DC converter acts as a voltage amplifier with a fixed gain, thus operating with minimum switching losses. As the stress on all the semiconductor devices tend to increase or decrease on the basis of dc-link voltage $V_{dc,\mathrm{k}}$, it needs to be optimized in order to achieve high overall efficiency. The proposed converter achieves PFC over the range of input voltage while maintaining a THD below 5%. It also maintains a stiff regulated DC voltage at the dc-link along with output voltage. Due to DCM operation, the sensor requirement is reduced to one voltage sensor and avoids the sensing of input voltage as well as current sensing.

The front-end bridgeless converter can be designed as per the equations listed in Table 4.2. The detailed derivations of each equation is mentioned in Chapter 3, subsection 3.5. Back-end converter gain equation and passive component can be designed as per procedure given by [69], [70]. The output-to-input relationship of the proposed configuration is a product of individual gains of two stages i.e. Front end and back end and can be defined as,

Table 4. 2: Design parameters of the front end converter

Parameters	Design Equations	
Average Output Current	$I_{o,avg} = \frac{V_{pk}^2 D^2 T_s}{4LV_o}$	(4.2)
Input Current	$I_{in} = \frac{V_{in} D^2 T_s}{2L} = \frac{V_{pk} D^2 T_s}{2L} \sin(\omega t) = I_{pk} \sin(\omega t)$	(4.3)
DCM Condition	$D < \frac{M}{(M+2)}$	(4.4)
Design of Inductor	$L < \frac{{V_{pk}}^2 {V_o}^2 T_s}{4P_o\left(V_o + 2V_{pk}\right)^2}$	(4.5)
Design of DC Link Capacitor	$C_o = \frac{2I_o}{\omega V_{o,ripple}}$	(4.6)
Gain of the Front End Converter	$G_{FE} = \frac{D}{1-D}$	(4.7)

$$\frac{V_{dc,link}}{V_{in,pk}} * \frac{V_{out}}{V_{dc,link}} = \frac{D}{1-D} * n * \left(\sqrt{\left(1 + \frac{1}{k}\left(1 - \left(\frac{f_O}{f_{sw}}\right)^2\right)\right)^2 + \left(\frac{\pi^2}{8} Q \left(\frac{f_O}{f_{sw}} - \frac{f_{sw}}{f_O}\right)\right)^2} \right)^{-1} \quad (4.8)$$

As, the LLC converter switching frequency f_{sw} is selected same as the resonant frequency, i.e. $f_{sw} = f_o$ to obtain resonant tank gain as unity and to minimize circulating current losses, (3.1) can be simplified by

$$\frac{V_{out}}{V_{in,pk}} = \frac{V_{dc,link}}{V_{in,pk}} * \frac{V_{out}}{V_{dc,link}} = \frac{D}{1-D} * n \quad (4.9)$$

Where D is the duty cycle of front-end converter and is defined by,

$$D < \frac{M}{(M+2)} \quad (4.10)$$

4.4 Loss Analysis

With the intention of selecting an optimal dc-link voltage, it is vital to derive a relationship between entire semiconductor losses and dc-link voltage $V_{dc,k}$, in order to diminish losses. Henceforth, a method for dc-link voltage selection is explained below by conducting a through loss analysis for the converter.

4.4.1 Front End Loss Analysis

MOSFETs conduction losses can be calculated by the RMS current expression that can be determined by switch current in a switching cycle and expressed as,

$$I_{sw,rms} = \frac{V_{in,pk} * D}{L * f_{sw}} \sqrt{\frac{D}{6}} \quad (4.12)$$

$$P_{SW_{BB},cond} = 2\left(I_{sw,rms}\right)^2 \times R_{DS,on,FE} \quad (4.13)$$

As the front-end converter is operating in DCM, the inductor core loss and winding losses are significant due to the large flux swing and high RMS current through inductor winding, thus it can be computed by

$$P_{L,losses} = \left[P_{c,limit} \times V_e + I_{L,rms}^2 \times R_{DCR}\right] \quad (4.14)$$

Where,

$$I_{l,rms} = \frac{V_{in,pk} * D}{L * f_{sw}} \sqrt{\frac{D}{6} + \frac{D}{12\pi V_o}\left(\frac{32V_{in,pk}}{V_o} - \frac{\pi}{2}\right)} \tag{4.15}$$

Diode losses comprise of turn-on losses, conduction losses and reverse recovery losses. Since, the PFC converter is operated in DCM, reverse recovery losses are the zero as current is zero in every switching cycle. Turn-on losses can be calculated as the product of average current I_d, and forward voltage V_f whereas the conduction losses can be calculated by estimating resistance of the diode [70] and is given as

$$P_{diode_{loss},FE} = 2\left[\left(I_{d,rms}\right)^2 \times R_d + \left(I_{d,avg} \times V_f\right)\right] \tag{4.16}$$

where,

$$I_{d,rms} = \frac{V_{in,pk} * DT_s}{2\sqrt{3}L} \sqrt{\frac{D}{\pi V_o}\left(\frac{32V_{in,pk}}{V_o} - \frac{\pi}{2}\right)} \tag{4.17}$$

$$I_{d,avg} = \frac{V_{in,pk}^2 D^2 T_{sw,FE}}{2LV_o} \tag{4.18}$$

The RMS current flowing through the dc-link capacitive filter is the difference between the diode RMS currents and the average output current [20] which can be calculated as

$$I_{Cdc,link,rms} = \frac{V_{in,pk} * D}{L * f_s} \sqrt{\frac{D}{12\pi V_o}\left(\frac{32V_{in,pk}}{V_o} - \frac{\pi}{2} - \frac{V_{in}^2 D^2 T_s}{2LV_o}\right)} \tag{4.19}$$

Thus loss due to capacitor ESR is given as

$$P_{C_{dc,link}} = I_{c,rms}^2 \times R_{C_{dc,link}ESR} \tag{4.20}$$

4.4.2 Back End Loss Analysis

The resonant current of LLC resonant converter $i_r(t)$ can be expressed as

$$i_r(t) = \sqrt{2} I_{pri,rms} sin(\omega t - \varphi) \tag{4.21}$$

where, $\omega = \frac{2\pi}{T_{sw,HB}}$

Since the output voltage clamps the magnetizing inductor in the first half of a PWM cycle and negative output voltage in the second half, the difference between i_r and i_{L_m} is the current flowing through the switch and is supplied to the load which is given by [70],

$$\frac{2}{T_{sw,BE}}\int_0^{2/T_{sw,BE}}\left(\sqrt{2}I_{pri,rms}sin(\omega t-\varphi)+\frac{V_oT_{sw,BE}}{4nL_m}-\frac{V_o}{nL_m}t\right)dt=\frac{nV_o}{R_L} \quad (4.22)$$

$$I_{sw_{BE},rms}=\frac{nV_o}{8R_L}\sqrt{\frac{2{R_L}^2}{n^4L_m^2f_{sw,BE}^2}+8\pi^2} \quad (4.23)$$

Thus, both primary switch conduction losses can be given by

$$P_{BE,cond}=2\times\left(I_{sw_{BE},rms}\right)^2\times R_{DS,BE} \quad (4.24)$$

As the LLC converter achieves ZVS turn-on, switching losses only comprises of losses due to turn-off. It is observed that when switch SW_4 turns off, it experiences linear operation. As the slope of V_{DS4} determines the slope of V_{DS3}, the discharge current through drain-source capacitance can be given as

$$I_{SW,3}=-C_{oss,BE}\frac{V_{dc,link}}{T_{off,BE}} \quad (4.25)$$

The current during turn-off of switch SW_4 can be given as

$$I_{SW_4,off}=I_{L_m,pk}+I_{SW,3} \quad (4.26)$$

$$=\frac{V_oT_{sw,BE}}{4nL_m}-C_{oss,BE}\frac{V_{dc,link}}{T_{off,BE}} \quad (4.27)$$

From (4.28) the switching losses can be calculated. Considering both the switches identical, the switching losses for primary side switches are given by

$$P_{SW_{BE},off}=0.1667\times f_{sw,BE}\times V_{dc,link}\left(\frac{V_o}{4nL_mf_{sw}}-\frac{C_{oss.BE}V_{dc,link}}{T_{off}}\right)\times T_{off} \quad (4.28)$$

Large magnetizing current tends to higher conduction losses because of higher circulating current. On the contrary low magnetizing current could result in loss of soft-switching in the MOSFETSs. Therefore, proper value of magnetizing inductance L_m needed to reduce circulating current and conduction losses. L_m energy should be high enough to discharge the output capacitance of primary switches. Too high inductance can cause low currents during dead-time which leads to bigger core size and loss of soft switching. Thus L_m can be calculated as

$$L_m < \frac{V_o * t_{dead} * T_{sw}}{8n * C_{oss} * V_{dc,link}} \tag{4.29}$$

As the proposed charger is for low-voltage high-current applications, secondary losses become significant and are accounted for in the loss analysis. Because of the synchronous rectification the switching losses are zero and losses are mainly dominated by the conduction losses in the switch secondary side RMS current can be given by

$$I_{SR,rms} = \frac{\sqrt{3}V_o}{24\pi R_L}\sqrt{12\pi^4 + \frac{(5\pi^2 - 48)R_L^2 T_{SW,BE}^2}{n^4 L_m^2}} \tag{4.30}$$

Thus, secondary switches conduction losses can be given by

$$P_{cond,SR} = 2\left[I_{SR,rms}^2 \times R_{DS,SR}\right] \tag{4.31}$$

The RMS ripple current through output capacitor can be given as the difference between the secondary resonant current and average output current, which can be given as

$$I_{C_o,rms} = \frac{V_o}{R_L}\sqrt{\frac{1}{96\pi}\left(12\pi^4 + \frac{(5\pi^2 - 48)R_L^2 T_{SW,BE}^2}{n^4 L_m^2}\right) - 1} \tag{4.32}$$

$$P_{C_o} = I_{C_o,rms}^2 \times R_{C_o,ESR} \tag{4.32}$$

Table 4. 3: Actual parameters and for loss analysis.

Parameter	Value	Parameter	Value	Parameter	Value
$R_{g,switch}$	4.5 Ω	V_f	0.8 V	$V_{f,SR}$	1.6 V
$Q_{GD,BB}$	11 nC	$R_{DS,HB}$	35 mΩ	L_m	150 µH
$Q_{GS,BB}$	19 nC	$Q_{GD,HB}$	11 nC	$R_{C_o,ESR}$	1.76mΩ
$R_{DS,on,BB}$	35 mΩ	$Q_{GS,HB}$	19 nC	R_L	4.225 Ω
R_{DCR}	15 mΩ	$C_{oss,HB}$	210 pF	V_{miller}	6.2 V
$R_{C_{dc,link}ESR}$	3.2mΩ	$C_{oss,SR}$	640 pF	$R_{g,driver}$	7.5 Ω
R_D	98 mΩ	$R_{DS,SR}$	28 mΩ	$Q_{GS,SR}$	18 nC
V_e	0.559cm^3	$P_{e,limit}$	500mW/cm^3	R_{DCR}	15mΩ

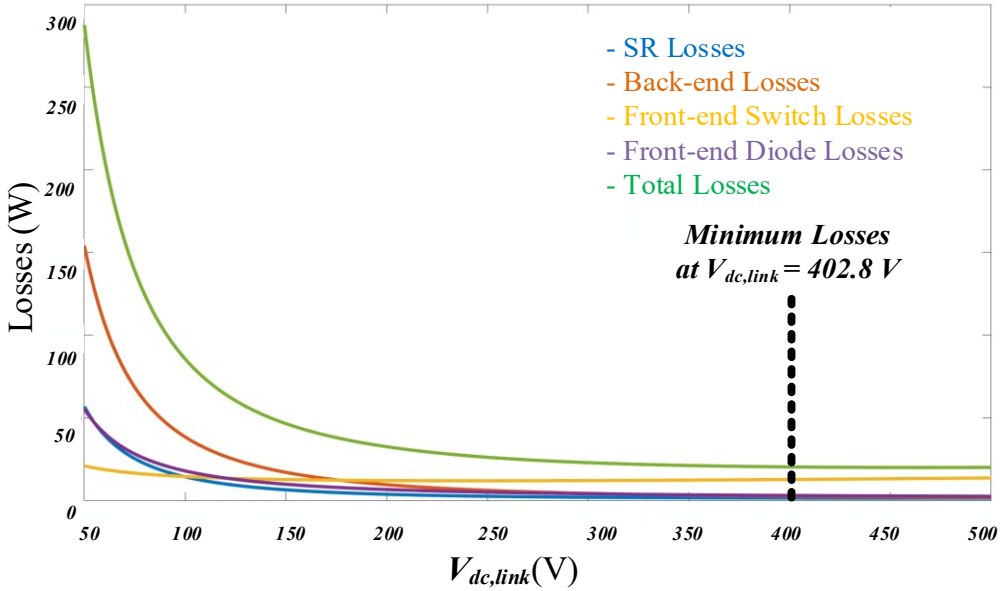


Fig. 4. 6. Calculated Losses according to various DC-Link Voltages.

Based on the loss analysis equations derived from the above sections, and using the components and parameters listed in Table 4.3, optimal DC-Link is selected as shown in Fig 4.6. At a dc-link voltage of 400 V the total losses are minimum. It is observed that the bridgeless buck-boost losses tend to increase considerably from the obtained optimal point due to high voltage stresses on semiconductor devices even though other losses reduce drastically. A dc-link voltage of 400 V is selected to design the proposed charger and the passive components are designed accordingly. On the selection of optimum dc-link voltage, the transformer turns ratio n can be calculated from (4.9).

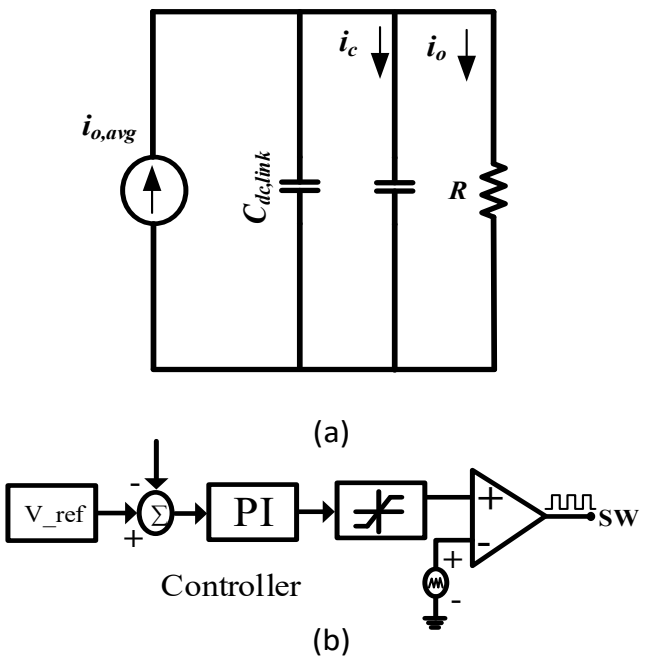


Fig. 4.7. (a) Equivalent circuit for small signal modelling. (b) Control Diagram.

4.5 Proposed Converter Small-Signal Model

Traditional two stage converters of battery chargers use complex control, which requires input voltage and current sensing along with PLL. Such systems pose a higher burden on microcontroller as more computation speed is required. The proposed converter mitigates these problems by limiting to sensor in total at the front end to control the output voltage. Whereas, the second stage acts like a voltage amplifier with a gain proportional to the turns ratio n, neglecting the dynamics offered by L_r and C_r. Thus the secondary side state variables can be referred to the primary as shown in Fig. 4.7(b). The small-signal model of the proposed converter is obtained by using the current injected equivalent circuit approach (CIECA) [42], [43]. This approach is better than the conventional state-space averaging approach as it becomes more cumbersome and complex in DCM. On the other hand, the CIECA approach is easier as it only models the transfer properties of the converter [42]. In CIECA, the entire circuit can be scaled down as shown in Fig. 4.7(a). The non-linear parameters of the circuit are linearized by injecting the average output current produced by the non- linear part. From Fig. 4.7(a)

$$\hat{\imath}_{o,avg} = \left(sC + \frac{1}{R}\right)\hat{v}_o \tag{4.33}$$

On applying perturbations to (4.2) we get

$$\hat{\imath}_{o,avg} = \frac{V_{pk}^2 D T_s}{2LV_o}\hat{d} + \frac{V_{pk} D^2 T_S}{2LV_o}\hat{v}_{pk} - \frac{i_{o,avg}}{V_o}\hat{v}_o \tag{4.34}$$

On equating (4.34), (4.33) and substituting $\hat{v}_{pk} = 0$

$$\frac{v_o(s)}{d_o(s)} = \frac{V_{pk} D}{K_{cond} M(sRC + 2)} \tag{4.35}$$

Where, $C = \frac{C_{dc,link} n^2 C_o}{C_{dc,link} + n^2 C_o}$, $M = \frac{V_o}{V_{pk}}$, and $R = \frac{R_L}{n^2}$.

The converter control to output transfer function is obtained by substituting the design parameters in (4.35). As the transfer function is a single-pole system, a simple PI controller $\left(K_p + \frac{K_i}{s}\right)$ is used to control the output voltage as shown in Fig. 4.7 (b). As the dc-link capacitor sees a voltage ripple of twice the line frequency, a PI controller with bandwidth lower than the 120Hz is selected with a phase margin of 60^0. The controller is tuned using sisotool in Matlab and the controller parameters are computed as $K_p = 0.00252$ and $\tau = 0.00361$. The output voltage is sensed using a hall-effect based LV-25P sensor. The sensed voltage is compared with the reference voltage and error is fed into the PI controller. The PI controller generates the duty cycle to control switch SW. A limiter is connected in order to limit the duty during start-up and overload conditions.

4.6 Result and Discussion

This section presents the simulation and experimental results of the proposed charger topology to validate the converter analysis and design.

4.6.1 Simulation Results

The proposed converter is simulated using PSIM 11.1 software to confirm the converter analysis and the design. The converter design specifications are given in Table 4.4. Using the designed parameters, the converter control-to-output transfer function is obtained from (4.35)

Table 4. 4: Converter design specifications.

Parameter	Value
Line voltage, $\boldsymbol{V_{in}}$ $\boldsymbol{RMS}$	110 $V_{RMS\ nominal}$
Input frequency, $\boldsymbol{f}$	60 Hz
Output power, $\boldsymbol{P_o}$	1.0 kW
Output voltage, $\boldsymbol{V_o}$	65 V
Switching frequency, $\boldsymbol{f_{sw}}$	50 kHz
Duty cycle, $\boldsymbol{D}$	0.638
Buck-Boost Inductance, $\boldsymbol{L}$	24.45 µH
DC link capacitance, $\boldsymbol{C_{DC1}}$, $\boldsymbol{C_{DC2}}$	82.4 µF
Output voltage ripple, $\boldsymbol{V_{o,ripple}}$	5% of output voltage (V_o)

and is given in (4.46). A PI-controller transfer function is designed for Phase Margin of 60^0 a bandwidth of 628.31 rad/sec. By taking $k_p = 0.0138$ and time constant $\tau = 0.0047$ controller is designed and implemented.

$$\frac{v_o(s)}{d(s)} = \frac{870}{1 + 0.0254s} \tag{4.36}$$

With the designed parameters and the designed controller, the circuit is simulated, and the results have been presented for the input frequency f = 60 Hz. The simulated input voltage and input current waveforms are shown in Fig. 4.8 (a). It is observed that input current is sinusoidal and in-phase with input voltage confirming the UPF operation of the charger. The output voltage and output current are shown in Fig. 4.8 (b) and can be observed that the output voltage settles at the reference voltage of 65V. Fig. 4.8 (c) and Fig. 4.8 (d) show the controller response during input voltage variation from 110 V to 80 V and 110 V to 130 V. The input current is closely tracking the input voltage both being in phase and shape. The inductor current waveform is shown in Fig. 4.8 (e) illustrating the DCM operation of the converter. Fig. 4.8 (f) shows the converter response for 50 to 100% load perturbation from 500 W to 1 kW. The output voltage is stable and tracking the reference voltage with a settling time of 10 ms, which confirms the robustness of the voltage controller. Fig. 4.8 (g) shows the ZVS turn-on operation of the back-end DC-DC converter. Switch turns on with zero voltage, thus confirming the soft switching of primary side half-bridge switches. Fig. 4.8 (h) shows the dc-link voltage variation during the transient condition. DC-link voltage tries to reduce for bigger

load changes as the duty cycle reduces drastically and dc-link capacitor supplies power to the load.

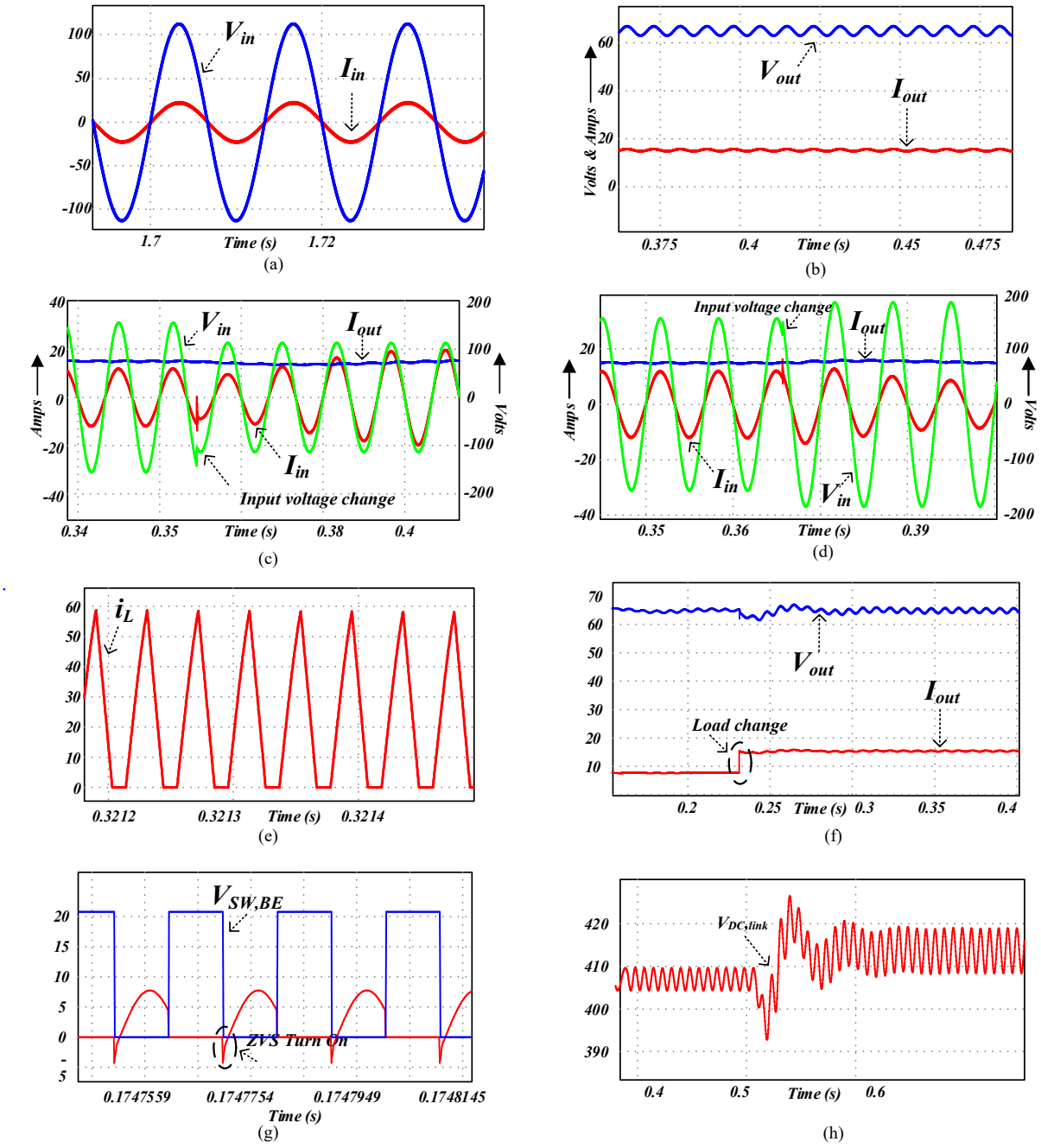
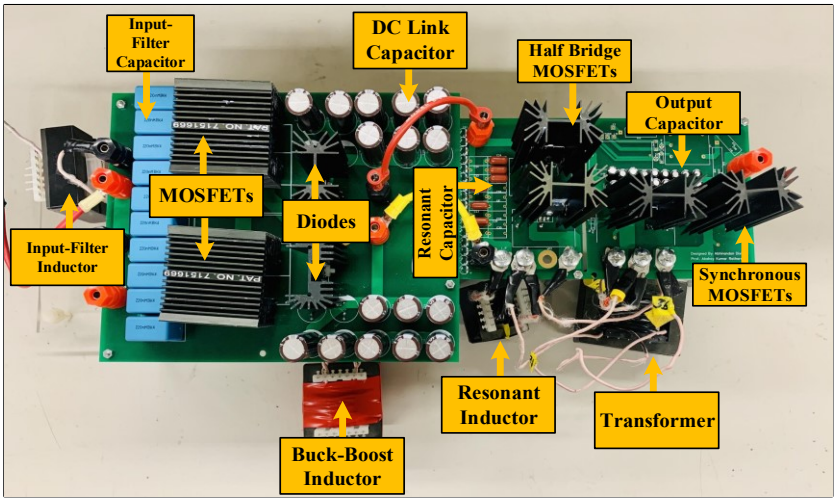
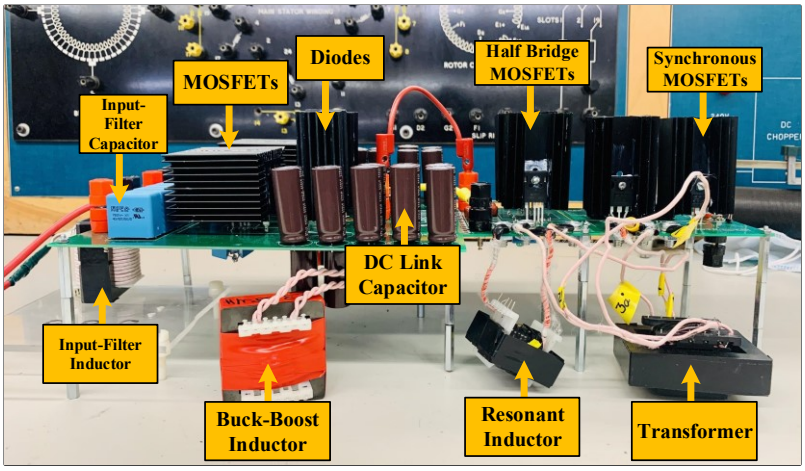


Fig. 4. 8. Simulation results (a) input voltage and current. (b) output voltage and current. (c) input voltage change from 110 V to 80 V. (d) input voltage change from 110 V to 130 V. (e) inductor current. (f) load change from 50% to 100% . (g) ZVS turn-on of half-bridge switch. (h) DC-link voltage variation during load change.



(a)



(b)

Fig. 4. 9. Experimental prototype of bridgeless converter (a) top view. (b) side view.

4.6.2 Experimental Results

To validate the analysis of the proposed converter and to verify the simulation results proof-of-concept laboratory hardware prototype rated at 1kW has been built with the same parameters used in the simulation. The hardware details are given in Table 4.5. The DSP TMS20F28335 is employed as a digital control platform to generate the gate signals for the converter. The hall-effect sensor LV-25P is employed to sense the converter output voltage. Fig. 4.9 (a) and Fig. 4.9 (b) show the top and side views of the experimental setup respectively. The converter nominal input voltage of 110 V RMS is been selected as per voltage-levels available in the lab. An approximate variation of 25% in input voltage has been

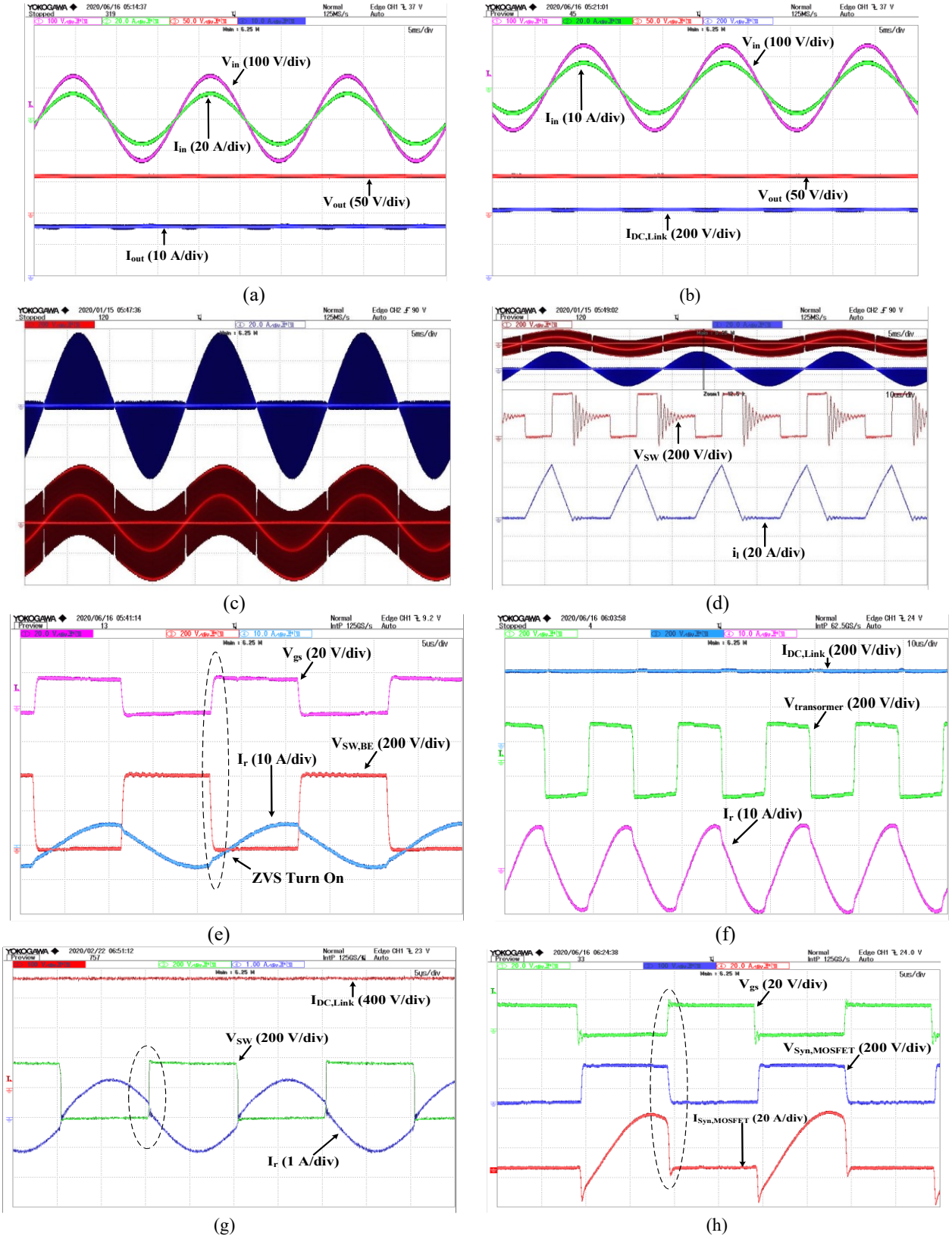


Fig. 4. 10. Experimental results (a) PFC operation at 1.0 kW b) input PFC and DC link voltage. (c) Switch voltage and inductor current (d) ZCS turn-on of switch. (e) Switch voltage, gate and resonant current. (f) Transformer primary voltage and current. (g) Resonance operation at a low load. (h) Synchronous rectification operation.

considered to validate the converter PFC operation. The output voltage of 65 V is as per [14]. The input filter parameters L_f and C_f are calculated for a corner frequency of 6 kHz. Fig. 4.10(a) shows that the input current is purely sinusoidal and in phase with the input voltage, thus achieving PFC at 1.0 kW. Fig. 4.10(b)shows the input volatge, the output volatge and the DC link voltage at rated power. The converter achives the PFC while maintaing the DC link volatge of 400 V and the output voltage of 65 V. Fig. 4.10 (c) shows the voltage stress that follows the sine envolpe and inductor current profile of the front-end converter having low frequency harmonics. The switch sees maximum voltage stress equal of $V_{pk} + \frac{V_{dc,link}}{2}$. Fig. 4.10(d) shows the zoomed version of Fig. 4.10 (c), the inductor current and the switch waveform at 500W output power where the inductor current is zero before turn-on confirming ZCS turn-on of switch SW. Fig. 4.10(e) shows ZVS turn-on operation of back end (half-bridge) MOSFETs, which confirms the soft switching of the switches. It is observed that the

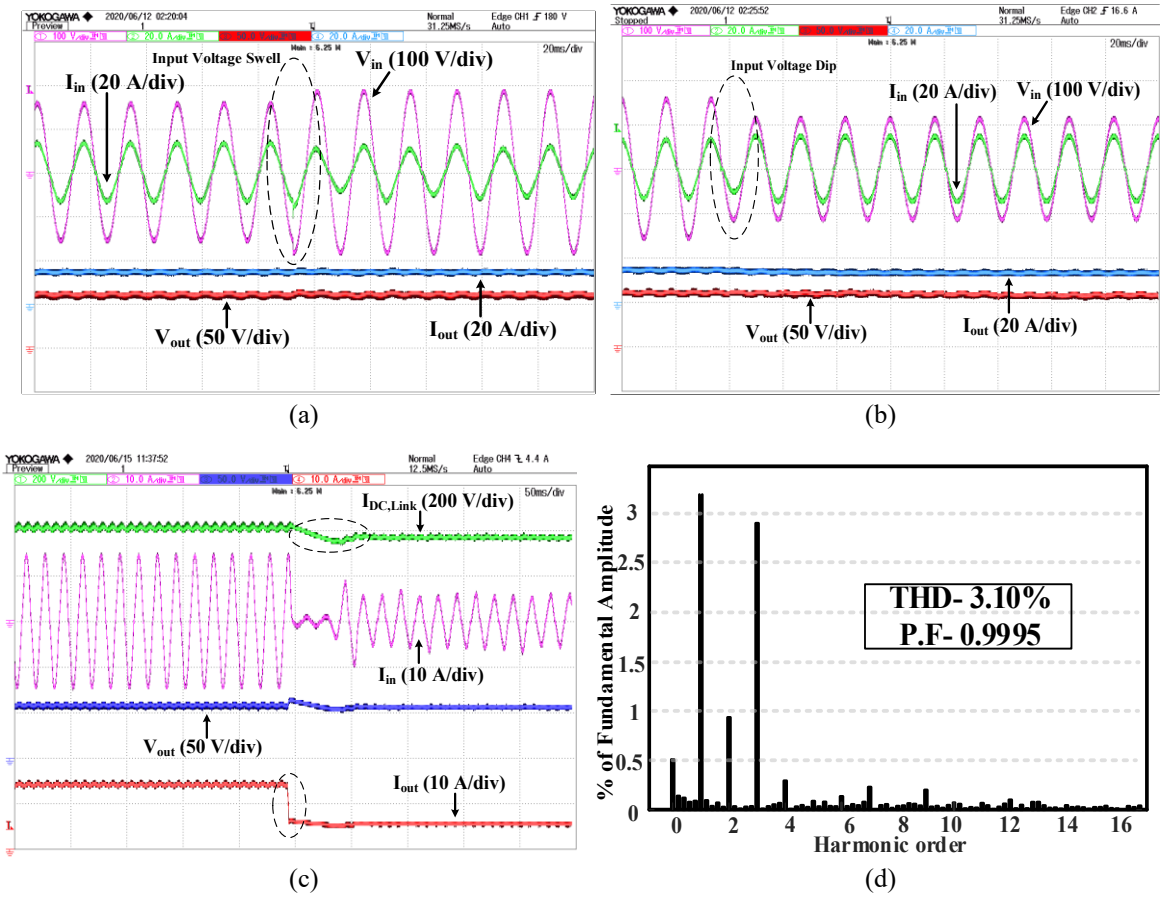


Fig. 4. 11. Converter response (a) Input voltage swell (b) input voltage dip (c) Load change from 100% to 20% (d) input current FFT at 1.0 kW

switch current is negative (body diode conduction using voltage across the switch) at the moment when the gate pulse is given, which confirms the ZVS operation. Fig. 4.10 (f) shows transformer primary voltage and current which is square and sinusoidal current, respectively thus posing no duty cycle loss. The DC link volatge remains constant. Fig.4.12 (g) shows the resonace operation of converter at a low load of 100W. Fig.4.10 (h) shows the syncrounus rectification on the seconaday side of the converter thus achieving higher efficiency.

In order to validate the robustness of the controller, input voltage perturbations are applied. Input voltage swell is applied form 110 V to 130 V as shown in Fig. 4.11 (a). It is seen that the input current remains sinusoidal and in-phase with input voltage thus validating the robustness of the controller. Similarly, the effect of the input voltage dip is shown in Fig. 4.11 (b). Input current increases in order to maintain the same power and remains in phase with the input voltage. In order to validate converter performance during load perturbactions, a load change from rated load to 20% load is applied as shown in Fig. 4.11 (c). It is observed that output voltage remains stiff at 65 V with and settles within 40ms, thus validating the controller design. Fig. 4.11 (d) shows the input current FFT at 1 kW. It is observed that input current THD is 3.10% with a power factor of 0.9995 which meets the IEC6100-3-2 standard.

As shown in Table 4. 6 it is to be noted that the second stage LLC converter poses comparatively higher efficiency over entire power range than convetional LLC converters.

Table 4. 5: Converter hardware specifications.

Components	**Specification**
DCM inductor L	24.45 µH
Resonant inductor L_r	78 µH
Resonant Capacitor C_{r_1}, C_{r_2}	PHE450XD5100JD15R06L2,10 nF*8
Transformer turns ratio, n	1:0.33:0.33
DC-link Capacitor, $C_{dc,link}$	82.4 µF*10*2, 450 VDC, UPZ2W820MHD
Output Capacitor, C_o	UVP2A100MPD1TD, 10 µF*18
Input capacitor, C_f	0.22 µF*10, 480 VAC, R76QR32204030J
Input inductor, L_f	371µH, 42 x 21 x 20, EE Ferrite Cores
Buck-boost MOSFETs, SW_1	UF3C120040K4S, SIC 1200V, 45mohm
Half-bridge MOSFETs, SW_3, SW_4	SCT3080AR, 650 V 30A
SR MOSFETs, SW_5, SW_6	STW75NF20, 200 V 75A
Schottky Diodes, D_1, D_2	RURG80100

Table 4.6: Efficiency of Two-Stage Converter for Various Power Levels

Power	LLC Converter Efficiency (%)	Bridgeless Buck-Boost Converter Efficiency (%)
100 W	90.2	91.2
250 W	92.4	93.3
500 W	96.6	95.8
750 W	97.2	96.3
1 kW	98.0	96.2

One of the main reason for improved efficiency of the DC-DC converter over entire range is fixed frequency, fixed duty operation as compared to the convetional LLC converter that incorporates frequency modulation in order to control charging voltage and current.

4.7 Conclusion

In this Chapter, an onboard battery charger is proposed, analyzed, designed, and tested. A new single-phase switched-mode bridgeless buck-boost topology is proposed for PFC with single sensor and reduced component count. In the second stage, a half bridge LLC resonant converter is employed to achieve high conversion efficiency over the full voltage range of the battery pack. The merits of the proposed converter are discussed and design guidelines are provided through theoretical analyses for both stages. A laboratory prototye of 1 kW is designed for 110 V, 60 Hz AC to of 65 V, 15A conversion. The experiment results are presented for validation. The first stage bridgeless buck-boost converter demonstrates UPF operation at the rated power and achieves THD less than 5%. In the second stage half bridge LLC converter, the switching losses, conduction losses are reduced to achieve good overall efficiency. Also, synchronus rectification is employed to enchance the efficiency. Loss analysis of the proposed topology has been presented in order to select an optimal value of DC-Link voltage to keep the losses minimum. With reduced sensors and high efficiency, the proposed charging topology is a potential candidate for battery charging application.

The next chapter deals with the the contributions of this research and the thesis. It also, provides the guidelines for the future scope of research.

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

This chapter discusses the contributions of this research and the thesis in section 5.1 and provides the guidelines for the future scope of research based on the findings in Section 5.2.

5.1 Contributions of Thesis

Grid connected plug-in electrified vehicles are considered as one of the most sustainable solutions to profoundly reduce both oil consumption and greenhouse gas emissions. However, charging the onboard battery pack more efficiently, conveniently, and with a smaller footprint is one of the most important challenges, which determine the acceptability of EVs among its consumers. The demand for PEVs battery charging with high-quality input current necessitates power factor corrected AC-DC converters. Moreover, these EV chargers desire high power density resulting into requirement of both higher efficiency (to reduce losses and device temperatures) and higher frequency operation (to reduce passive component sizes). The traditional battery chargers topologies lack with active power factor correction unit, and have poor THD along with low efficiency and increased switching and conduction losses. This thesis desertion focuses on AC-DC PFC (isolated and non-isolated) topologies as well as a new front end bridgeless topology as a solution to replace the presently employed topologies.

This thesis discretion contributes to the analysis and design of the buck-boost derived AC-DC PFC converters focusing on the minimizing the total number of components and improving the overall system efficiency. The proposed topologies not only achieves high power factor correction (PFC) but also obtain THD less than 5%. The proposed converters are studied, analyzed, and designed for DCM operation in order to simplify the control circuit and to reduce the number of sensors, which consequently increases the converter reliability and robustness. Simple control, high input power quality, improved efficiency, and improved reliability are the major highlights of the proposed DCM converter topologies as outlined in the following sub-sections.

5.1.1 Analysis and Design of Single-Stage DCM Operated Buck-Boost PFC AC Charger

The first contribution, presented in Chapter 2, is a single-phase single-cell non-isolated buck-boost PFC converter for the E-Rickshaw battery charging application. The highlights of the proposed converter are reduced overall size, bolstered up overall efficiency and possess simpler control with fewer conversion stages. High efficiency of 93.5 % and input current THD of 4.25 % are recorded from the developed prototype at rated output power along with a high power factor of 0.9990. The converter comprehends zero-current turn-on of the switches, and zero diode reverse recovery losses due to its DCM operation. The converter output is controlled by only one control loop and a single sensor. Experimental results demonstrated the proposed converter's inherent in-rush current limiting,

5.1.2 Single-Phase Switched Mode Bridgeless AC-DC Buck-Boost Derived Converter

In Chapter 3, the second contribution is presented as a new single-phase switched-mode bridgeless AC-DC buck-boost derived converter. The novelty of the proposed converter is demonstrated by comparing it with the state-of-the-art converters. The key contribution of the proposed converter is that only one semiconductor device from each phase is in the current conduction path throughout the converter operation which reduced the converter conduction losses, and increased the converter efficiency. The voltage stress is reduced by the DC-split output configuration in the proposed converter, which reduces the switching losses. The converter output is controlled by only one control loop and a single sensor making it less complex. An experimental prototype was built and tested in order to verify the concept. Key experimental waveforms were provided. The converter power factor and THD measurements were recorded at an output voltage of 400V and 80 - 130V wide input voltage range. The power factor exceeds from 0.9993 at half load to 0.9995 at full load. The proposed converter achieved a peak efficiency of 96% and an input current THD of 3.13 %.

5.1.3 An On-Board EV Charger Using Bridgeless PFC and LLC Resonant Converter

The third contribution, presented in Chapter 5, is a new two-stage isolated EV charger integrating a bridgeless PFC and LLC resonant converter. Bridgeless PFC buck-boost converter operating in DCM is used as a first stage to achieve PFC and high input THD. In the second stage, a half-bridge LLC converter is used to provide isolation and high efficiency to the overall power range. The proposed charger is designed for a 48V low voltage lead-acid battery pack. The proposed configuration uses only one sensor to control the output voltage by directly controlling the front-end switches. The control burden is reduced on the microcontroller by operating the second stage with constant duty and constant frequency. An experimental prototype was built and tested in order to verify the concept. The PFC stage achieves 3.13% THD and 96% conversion efficiency experimentally. While the dc/dc stage achieves 98% peak efficiency.

In addition to the above contributions, the following conclusions which are common to all the proposed topologies are abridged as follow:

- The proposed converters are designed for DCM operation and obtained UPF at AC mains with less input current distortion for different loads and for a wide range of supply voltage 80 to 130V.
- All the switches of the proposed converters are operated with zero current switching turn-on and diodes with zero reverse recovery losses which are characteristic of DCM operation.
- High current rated semiconductor devices are used because of the high peak current due to DCM operation.
- The converters' output voltage is regulated with a simple voltage control loop, and only a single sensor is required for PFC control implementation. This makes the proposed converters cost-effective, escalates the reliability, robustness to high-frequency noise, and the system power density.
- The small-signal models for all the converters are established using the CIECA approach, and a detailed discussion for the closed-loop controller design is provided.

- Detailed simulation results, as well as experimental results, are provided to validate the analysis, design, and feasibility.
- All the proposed converters show input current THD less than 5 %, and efficiency greater than 90 % are rated output power from the developed laboratory prototypes.

5.2 Scope of Future Work

Based on the research done in this thesis, the recommendations for the future research could focus on the following two aspects:

5.2.1 DCM Based Interleaved Bridgeless Buck-Boost Converter

The Bridgeless buck-boost PFC converter prototype presented in chapter 3 utilizes a single-phase configuration, which is suitable for low power levels. However, in order to achieve a higher power charging, the current stress on the circuit components increases. For the power MOSFETs, we can parallel multiple devices to achieve higher current capability. The interleaved is formed by two independent bridgeless buck-boost converters which are connected in parallel. The switching signals for the interleaved bridgeless buck-boost converter can have the same switching frequency and duty cycles with an artificial shift of the gate signals among different phases by a certain degree (180^0 phase shift), which would contribute to reducing the current ripples. Each converter has two switching stages, diodes D_1 and D_2 are always in the complementary state with the switches SW_1 and diodes $D_3$and D_4 being complementary to SW_2 respectively. Moreover, the input current equals the summation of both inductor current. Since the inductor ripple currents are out of phase, they can cancel with each other. Thus, the high-frequency input current ripple could be significantly reduced, so that the size of the input EMI filter could be reduced. Moreover, the input power of the converter is evenly shared between the two cells, thus the current stress on the semiconductor components as well as DCM inductor will be reduced by half. The schematic of an interleaved bridgeless buck-boost derived PFC converter is plotted in Fig. 5.1.

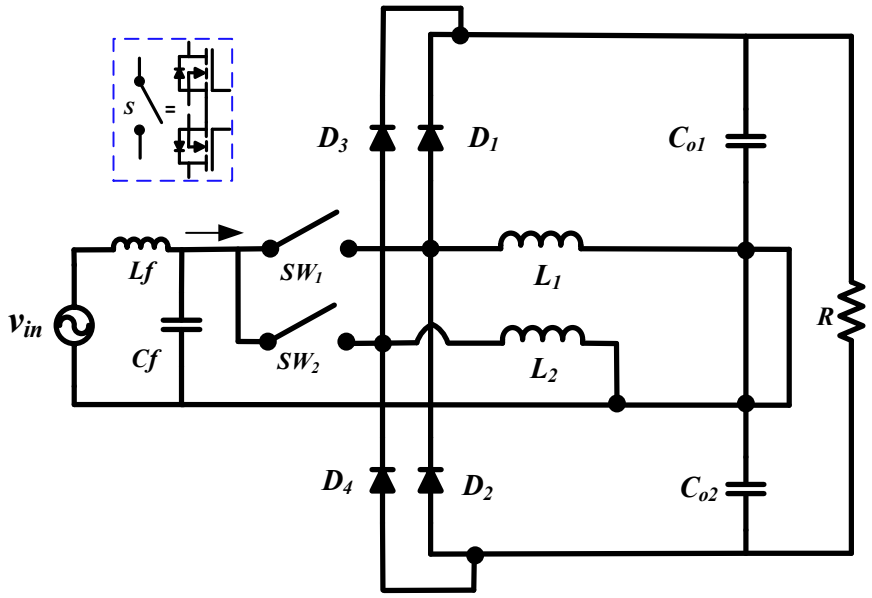


Fig. 5.1. Schematic of interleaved bridgeless buck-boost derived PFC converter

5.2.2 A High Power On-Board Bidirectional EV Charger Using Interleaved Bridgeless PFC and Full-Bridge LLC Resonant Converter

At present, all commercialized onboard EV chargers have unidirectional power flow from grid to vehicle (G2V). However, since most vehicles are parked an average for 95% of the time, it is predictable that batteries could be used to let power flow from the vehicle to the grid (V2G). In this emerging V2G technology, on-board chargers are required to have bidirectional power flow capability. When the vehicle is idle, the battery can feed power back to the grid if demand is high. In order to achieve the bidirectional power flow, both the front-end ac/dc PFC and the second stage isolated dc/dc topologies must be modified to operate in bidirectional power flow. Fig. 5.2 is a combination of interleaved bridgeless buck-boost derived converter and a bidirectional dual active bridge LLC converter, which is a derivative of full-bridge LLC resonant converter. When the energy is transferred from grid to battery, the active bridge on the secondary side of the transformer functions as a full bridge rectifier. When the energy is transferred from battery to grid, the secondary side active bridge functions as an inverter and the primary side active bridge functions as a rectifier. The interleaving on the front end can help in achieving higher power density along with high power factor and low THD. A controlled constant voltage (CV) and constant current (CC) charging methodology can also be implemented to switch between V2G and G2V modes. However, it

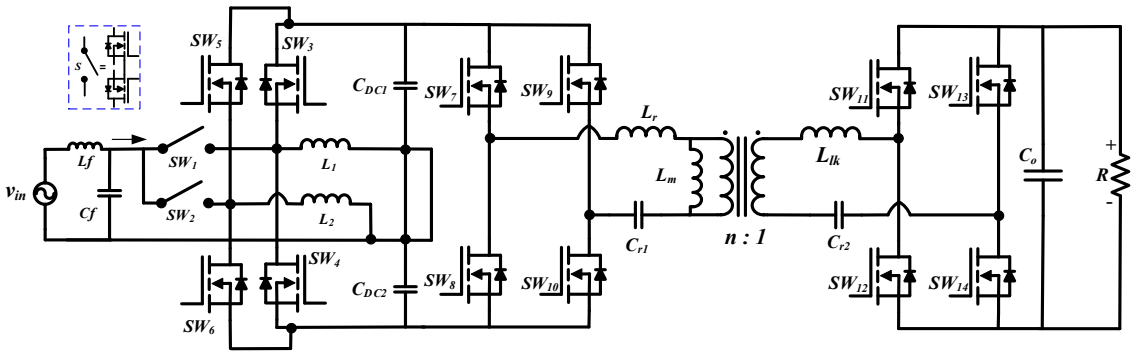


Fig. 5.2. Schematic of Interleaved Bridgeless PFC and Full-Bridge LLC Resonant converter

must be taken into account that bidirectional charging has not yet been implemented on any commercial PEV in the market. The challenges are predominantly are because of the bellow three conditions:

a. The additional cost of power electronics components.
b. There is a potential uncertainty of battery degradation due to frequent charging and discharging cycles, which might affect the overall battery life cycle.
c. Lack of infrastructure for net-metering from the energy utility company.

Future work would pursue accomplishing the bidirectional power flow of the onboard PEV chargers along with increased power density while exploring possible solutions to deal with the aforementioned challenges.

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List of Publications

Journal Paper

1) A. Dixit, **K. Pande**, S. Gangavarapu and A. K. Rathore, "DCM Based Bridgeless PFC Converter for EV Charging Application," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, doi: 10.1109/JESTIE.2020.2999595.

Conference Papers

1) A. Dixit, **K. Pande**, A. K. Rathore, R. K. Singh and S. K. Mishra, "Design & Development of On-Board DC Fast Chargers for E-Rickshaw," 2019 IEEE Transportation Electrification Conference (ITEC-India), Bengaluru, India, 2019, pp. 1-6, doi: 10.1109/ITEC-India48457.2019.ITECINDIA2019-40.
2) **K. Pande**, A. Dixit, A. K. Rathore, R. K. Singh, S. K. Mishra and J. Rodriguez , "Design & Development of Bridgeless Buck-Boost Derived PFC Converter for On-Board EV Charging Application" 2020 IEEE Energy Conversion Congress and Exposition (ECCE-Detroit, Michigan, USA) **[Accepted]**.
3) **K. Pande**, A. Dixit, S. Gangavarapu and A. K. Rathore, "Two-Stage On-Board Charger using Bridgeless PFC and Half-Bridge LLC Resonant Converter with Synchronous Rectification for 48V e-Mobility" 2020 IEEE Industry Applications Society Annual Meeting, Detroit, Michigan, USA **[Accepted]**.