Analysis and Design of Methods for Condition Monitoring of Capacitors in Multilevel Converters

Ronak Vivek Nemade

A Thesis

In the Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

For the Degree of Master of Applied Science at

Concordia University

Montreal, Quebec, Canada.

March 2021

CONCORDIA UNIVERSITY
SCHOOL OF GRADUATE STUDIES

This is to certify that the thesis prepared

By: Ronak Vivek Nemade

Entitled: Analysis and Design of Methods for Condition Monitoring of Capacitors in Multilevel Converters

and submitted in partial fulfillment of the requirements for the degree of

Master of Applied Science (Electrical and Computer Engineering)

Complies with the regulations of this University and meets the accepted standards with respect to originality and quality.

Signed by the final examining committee:

_____ Dr. Glenn Cowan	Chair
_____ Dr. Anjali Awasthi (CIISE)	Examiner, External to the program
_____ Dr. Glenn Cowan	Examiner
_____ Dr. Akshay Kumar Rathore	Supervisor

Approved by: _____
Dr. Yousef R. Shayan, Chair
Department of Electrical and Computer Engineering

March 18th, 2021
Date of Defence

_____
Dr. Mourad Debbabi, Interim Dean
Gina Cody School of Engineering and Computer Science

ABSTRACT

Analysis and Design of Methods for Condition Monitoring of Capacitors in Multilevel Converters

Ronak Nemade.

Concordia University, 2021

Multi-level converters are an important class of power electronics based systems that enable seamless conversion of electrical power from one form to another. Due to its distinct merits, it finds a vast scope of application in the fields such as renewable energy, electrical power transmission, adjustable speed drives, uninterrupted power supplies and custom power devices. These merits often come at a cost of increased complexity, higher number of power semiconductor devices and higher number of energy storage elements. Multi-level converters generates staircase waveform by use of high density capacitor banks. These capacitor banks are often subject to failure due to vaporization of electrolyte forming weakest link in reliability context. This thesis addresses reliability issue by proposing an online condition monitoring method for a three-level neutral point clamped multi-level converter which can be easily integrated with existing control methods. The proposed method provides an online estimate of existing capacitance in DC-link and helps increase in reliability in terms of preventive maintenance. The validity of proposed technique is obtained by verification of the method on a 3KVA laboratory developed experimental prototype. It also addresses reliability by developing tool in terms of analytical expressions which can be used as a ready reckoner for proper design of capacitor bank employed in five-level active neutral point clamped multi-level converter. Results from this developed tool are quantitatively verified with the results obtained from converter models developed over MATLAB Simulink environment confirming their accuracy.

Acknowledgement

I would like to express my sincerest gratitude, special appreciation and many thanks to my supervisor, Dr. *Akshay Kumar Rathore* for his guidance, supervision and his patience with me. I am thankful for his valued and timely suggestions not only for academics, and research work but also on personal life fronts. My success in learnings and completion of this thesis is based on his scientific knowledge, critical thinking and his continuous support.

The completion of this thesis also includes technical inputs and help from my colleagues in the Power Electronics and Energy Research (PEER) group. I would like to express thanks to *Dr. Sivanagaraju, Dr. Venkat, Swati, Dwaipayan, Karan* and *Abhinandandan* for their friendship and support. I would like to thank *Amit Chandra* my friend and my guide who helped me during the periods of depression and anxiety.

I would like to thank my parents (*Mr. Vivek Nemade* and *Mrs. Nilima Nemade*) and my brother *Hardik* for their continuous love and support.

In the end, I would like to acknowledge almighty God who kept me going during the hard times and helped me gain moral strength to complete this degree.

Table of Contents

LIST OF TABLES.....VIII

LIST OF FIGURES.....IX

LIST OF ABBREVATIONS.....XI

LIST OF SYMBOLS.....XII

CHAPTER 1: INTRODUCTION..... 1

1.1 Introduction 1

1.2 Literature Review 3

1.3 Research Objectives 6

1.4 Thesis Outline. 7

CHAPTER 2: CONTROL METHODS FOR MULTILEVEL CONVERTERS..... 8

2.1 Introduction 8

2.2 Hysteresis Current Control 8

2.3 Linear Control Method 10

2.3.1 Carrier based Pulse Width Modulation 10

2.3.2 Linear control method using Space Vector based Modulation 10

2.4 Predictive Control Method. 14

2.4.1 Finite Control Set Model Predictive Control 15

2.5 Synchronous Optimal Control 15

2.5.1 Synchronous Optimal Pulse Width Modulation 16

2.6 Potential Control Methods for Online Condition Monitoring 17

2.7 Conclusion 17

CHAPTER 3: A FINITE CONTROL SET MODEL PREDICTIVE CURRENT CONTROL OF 3-LEVEL NEUTRAL POINT CLAMPED CONVERTER WITH CONDITIONING MONITORING OF DC-LINK CAPACITORS..... 19

3.1 Introduction 19

3.2 Mathematical Modeling 19

3.2.1 Power Converter Model 19

3.2.2 Load Model 23

3.2.3 Discrete-Time Model for Prediction 23

3.3 Control Design 24

3.3.1 Conventional FCS-MPCC Scheme 24

3.3.2 Dynamic Neutral-Point Model and its Impedance Predictability in a Three-Level Converter 26

3.3.3 FCS-MPCC with Condition Monitoring 27

3.4 Algorithm Implementation 28

3.5 Choice of difference voltage injection frequency 30

3.6 Simulation results 30

3.7 Hardware Implementation and Results 34

3.7.1 Hardware Implementation 35

3.7.2 Experimental Results 37

3.8 Conclusion 41

CHAPTER 4: ANALYTICAL EVALUATION OF CAPACITOR CURRENT STRESS IN FIVE-LEVEL ACTIVE NEUTRAL POINT CLAMPED CONVERTER 42

4.1 Introduction 42

4.2 Principal of Operation 42

4.3 Defining mathematical expressions for conduction intervals. 43

4.3.1 Conduction function - Low frequency switch 43

4.3.2 Conduction function - High frequency switch 44

4.4 Analytical expressions for capacitor current stresses. 45

4.4.1 Flying capacitor current stress 46

4.4.2 DC-Link Capacitor current stress 46

4.5 Comparison of results with simulation..... 49

4.6 Conclusion..... 52

CHAPTER 5: CONCLUSIONS AND FUTURE WORK 53

5.1 Contributions of Thesis 53

- Finite control set MPCC of three-level NPC converter with conditioning monitoring of DC-link capacitors 53

- Analytical evaluation of capacitor current stress in five-level active neutral point clamped converter. 54

5.2 Scope of Future Work 54

5.2.1 Switching State Grouped Finite Control Set MPCC of multi-level converters with Condition Monitoring of DC-link Capacitors. 54

5.2.2 Control of Nested Neutral Point Clamped Converter with Condition Monitoring of DC-link Capacitors. 56

5.2.3 Finite Control Set Model Predictive Current Control of Modular Multilevel Converter with Condition Monitoring of Sub-Module Capacitors. 57

REFERENCES…… 59

LIST OF PUBLICATIONS…….…….. 65

List of Tables

Table 1.1 Different condition monitoring schemes for different converters 5

Table 2.1 Switching state and voltage vectors 12

Table 3.1 Switching states of inverter leg 20

Table 3.2 Voltage vectors and switching states 21

Table 3.3 Hardware specifications of prototype 34

Table 4.1 Switching states for 5L-ANPC leg 43

Table 4.2 Conduction function for low frequency operated switches 44

Table 4.3 Conduction function for flying capacitor 45

Table 4.4 Peak stresses in capacitors at operating conditions 49

List of Figures

Figure 1.1 Single leg of basic MLI topologies for 5-level configuration 2

Figure 1.2 Division of multi-level inverter classes [3]. 3

Figure 1.3 Classification of research efforts in direction of improving reliability 4

Figure 2.1 Power electronics based system 8

Figure 2.2 Hysteresis current control of three-phase inverter [29]. 9

Figure 2.3 Carrier based Pulse width modulator for a three-phase inverter [29]. 11

Figure 2.4 Principles of space vector based modulation (a) Voltage vectors and sector definition.[29] 12

Figure 2.5 Control scheme using Space Vector based Modulation [29]. 13

Figure 2.6 Classification of predictive control techniques [32]. 14

Figure 2.7 Synchronous optimal modulation [38]. 16

Figure 3.1 Three-phase three-level neutral point clamped inverter power circuit 20

Figure 3.2 Circuit with phase - B connected to neutral point. 22

Figure 3.3 Conventional Predictive Current Control for NPC Inverter 25

Figure 3.4 Dynamic neutral point model 26

Figure 3.5 FCS-MPCC of NPC inverter with Condition Monitoring 27

Figure 3.6 Flow chart of predictive control algorithm with condition monitoring 29

Figure 3.7 Currents with conventional FCS-MPCC Scheme 31

Figure 3.8 Capacitor voltage control with FCS-MPCC 31

Figure 3.9 Currents before and after difference voltage Injection 32

Figure 3.10 Injected difference voltage and estimated neutral point current 32

Figure 3.11 Filtered difference voltage and filtered neutral point current 33

Figure 3.12 Calculated impedance of dynamic model 34

Figure 3.13 3 kVA, three-level NPC inverter hardware prototype 35

Figure 3.14 Switched DC-link capacitor in hardware prototype 35

Figure 3.15 Block diagram of hardware implementation with feedbacks 36

Figure 3.16 Algorithm implemented in Digital Signal Processor 37

Figure 3.17 Impedance extraction at 5100 uF capacitance of dynamic model 38

Figure 3.18 Impedance extraction at 3300 uF capacitance of dynamic model 39

Figure 3.19 Load Current during condition monitoring 40

Figure 3.20 Extensive control action leading to increased switching 40

Figure 4.1 Five level Active Neutral Point Clamped Converter leg 42

Figure 4.2 Relation of flying capacitor conduction function with switching function 44

Figure 4.3 5L-ANPC converter configurations 45

Figure 4.4 Reference overlapping interval 48

Figure 4.5 Error in analytical expressions (modulation sweep) 50

Figure 4.6 Error in analytical expression (power factor angle sweep) 51

Figure 4.7 Locus of capacitor current stress (a) flying-capacitor (b) DC-link capacitor in 1-phase full-bridge configuration and (c) DC-link capacitor in 3-phase configuration 52

Figure 5.1 Flow chart of switching state grouped FCS-MPCC with condition monitoring 55

Figure 5.2 Nested neutral point clamped multilevel converter 56

Figure 5.3 Modular multilevel converter topology 57

List of Abbreviations

MLC	Multi–Level Converters
HVDC	High Voltage Direct Transmission
FACTS	Flexible Alternating Current Transmission System
ASD	Adjustable Speed Drives
AFC	Active Front-end Converters
CPD	Custom Power Devices
REG	Renewable Energy Generation
BESS	Battery Energy Storage System
EV	Electric Vehicles
AEC	Aluminum Electrolytic Capacitors
ESR	Equivalent Series Resistance
MMCs	Modular Multilevel Converters
SM	Sub Module
PWM	Pulse Width Modulated
RLS	Recursive Least Squared
FCS-MPCC	Finite Control Set Model Predictive Current Control
SVM	Space Vector Modulation
MPC	Model Predictive Control
NPC	Neutral Point Clamped
MATLAB	Matrix Lab
IGBT	Insulated Gate Bipolar Junction Transistors
RMS	Root Mean Square
FIR	Finite Impulse Response
ADC	Analogue to Digital
DAC	Digital to Analogue
ISR	Interrupt Service Routine
CLA	Control Logic Accelerator
IPC	Inter Processor Communication
5L-ANPC	Five Level Active Neural Point Clamped

List of Symbols

S_x	Switch x / Switching state
$v_a{}^*, v_b{}^*, v_c{}^*$	Reference modulating voltage signals
v_{cr}	Carrier voltage signal
v_{ab}	Line-to-line inverter voltage
v_{aN}	Inverter phase voltage
$\mathbf{v}^*$	Reference voltage vector
$\mathbf{V}$	Voltage vector
T_c	Carrier period
θ	Reference vector angle
N	Number of switching states
D_x	Diode x
z	Neutral Point
v_{c1}, v_{c2}	Capacitor voltages
v_Δ	Difference voltage
i_a, i_b, i_c	Load Currents
i_z	Neutral point current
L	Load Inductance
R	Load Resistance
$\mathbf{i}$	Load current vector
$\mathbf{e}$	Back emf vector
i_{c1}, i_{c2}	Capacitor currents
g	Cost function
λ_{dc}, λ_n	Weights
Z_{dyn}	Dynamic model Impedance
f_{inj}	Injected Frequency
n_c	Number of commutations
$v_\Delta{}^*$	Difference voltage reference
V_{dc}, U_c	DC-link voltage

VA	Volt amperes
C_1, C_2	DC-link capacitors
kVA	Kilo volt amperes
C_{fx}	Flying-capacitor
G	Conduction function
m	Modulation index
ϕ	Load power factor angle
$\cos\phi$	Load power factor
i_{cfx}	Instantaneous flying capacitor current
I_m	Maximum load current
I_{cfx}	RMS flying capacitor current
$i_{i\text{-}hb}$	Instantaneous half-bridge capacitor current
$I_{c\text{-}hb}$	RMS half-bridge capacitor current
$I_{avg\text{-}hb}$	Average half bridge current
$I_{c\text{-}fb}$	RMS full-bridge capacitor current
$I_{avg\text{-}fb}$	Average full bridge current
$I_{c\text{-}3\phi}$	RMS three-phase DC-link capacitor current
$\%\ error$	Relative error
$I_{c,rms,1,sim}$	RMS capacitor current in Simulation
$I_{c,rms,1,eqn}$	RMS capacitor current by analytical expression

CHAPTER 1: INTRODUCTION

1.1 Introduction

Electrical power available through the source is often different than the one desired by loads. This difference in form of electrical power is addressed by power electronics based power processing circuits. As the power handled by power processing circuits vary from few watts to mega-watts, the size of circuit and the semiconductor technology employed in them varies. A point of load power supply handling few watts of power are available in the form of integrated circuits which can be easily mounted on a printed circuit boards while a high voltage direct current (HVDC) based power transmission product handling mega-watts of power are available as an integrated system occupying large space. Though the integration size and power semiconductor device technology changes, the circuit configuration (electrical network) used to process electrical power more or less stays the same. These power processing circuits can be segregated into various classes based on the power converted from AC to DC, DC to DC, DC to AC or AC to AC. Multi-level converters is an important class of DC to AC conversion system generating AC voltage waveforms in form of a staircase. Multi-level converters (MLC) were developed to serve medium/high-power medium/high-voltage applications, by using low-voltage devices, because of limitation on the power semiconductor technology. Development of these converters led to the power electronic systems that have additional merits like better output voltage waveform quality, lower harmonic distortion of output and input currents, less *dv/dt* stress, reduced filter size, lower common-mode voltages and reduced electromagnetic interference [1, 2]. With advancement of semiconductor technology, analysis and integrating techniques multi-level structures are not only used for mega-watt scale power electronic products like drives and HVDC, but are also used for low power ultra-compact chip level class D-audio amplifier applications.

Basic configurations used to build MLC topologies include diode-clamped structure, flying-capacitor and cascaded H-bridge configurations as shown in Figure 1.1. Now, these basic MLC configurations have evolved as a mature technology and are used for various commercial and customized products for a wide power range (1kW to several MW) of applications such as high-voltage direct-current (HVDC) transmission, flexible ac transmission systems (FACTS),

adjustable speed drives (ASD), active front-end converters (AFC), custom power devices (CPD), battery energy storage systems

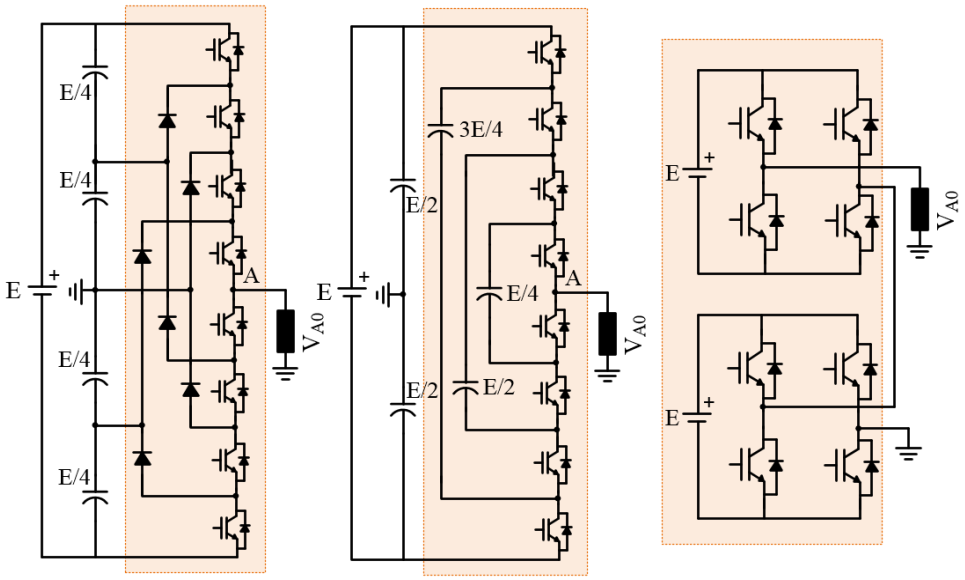

Figure 1.1 Single leg of basic MLI topologies for 5-level configuration

(BESS), electric vehicles (EV), renewable energy generation (REG), and more electric aircrafts [4-8]. Increased complexity of MLCs because of higher number of switching devices, which include complex control, uneven power distribution, reliability etc. These demerits have motivated researchers to find solutions based on basic MLC topologies. Various motivational factors that have contributed to research associated to the MLCs which can be listed as:

- **Converter Control:** Several control techniques of operating MLCs depending on application requirement.
- **Fault tolerant ability:** Fault tolerant ability enables the inverter to operate with abnormal working conditions such as faults on switching devices or dc sources, ensuring reliability with balanced operation.
- **Device Count:** To develop topology with appreciable reduction in device (switches/diodes/capacitors/dc-sources) count.
- **Requirement and Utilization of dc-sources:** Equal utilization of dc sources to contribute to the natural balancing of the DC-link voltages in closed loop applications. Reduction in dc source requirement increased the role of capacitors and thus, emerged self-balancing and voltage boosting topologies with and without galvanic isolation.

- **Device rating/ blocking voltages:** To develop the topology, involving identical device ratings and producing minimum device blocking voltages.
- **Modularity:** Topologies having modular configuration can easily be extended to higher levels.
- **Even power distribution:** Ability of the inverter to obtain required phase-voltage levels by distributing uniform power across all switches/units. This feature contributes to charge balance among the DC-link voltages.
- **Application area:** A critical analysis is carried out among the newly developed topologies in finding out its best application in the areas such as FACTS, HVDC, CPD, BESS, ASD, IPQC, EV and consumer electronics.

Extensive research activity enabled by stated motivational factors has resulted in proposal of numerous multilevel topologies and the methods to control them. Each of these topologies and its associated control having its own merits and demerits addresses specific application requirements. Thus, the classification of multilevel topologies available in literature is more or less based on the application requirements that mainly include number of phases, input to output isolation, voltage level boost, and availability of sources, power semiconductor switches connections and the symmetry of available voltage levels. Classification of MLC structures based on various circuit configurations is shown in Figure 1.2. [3]

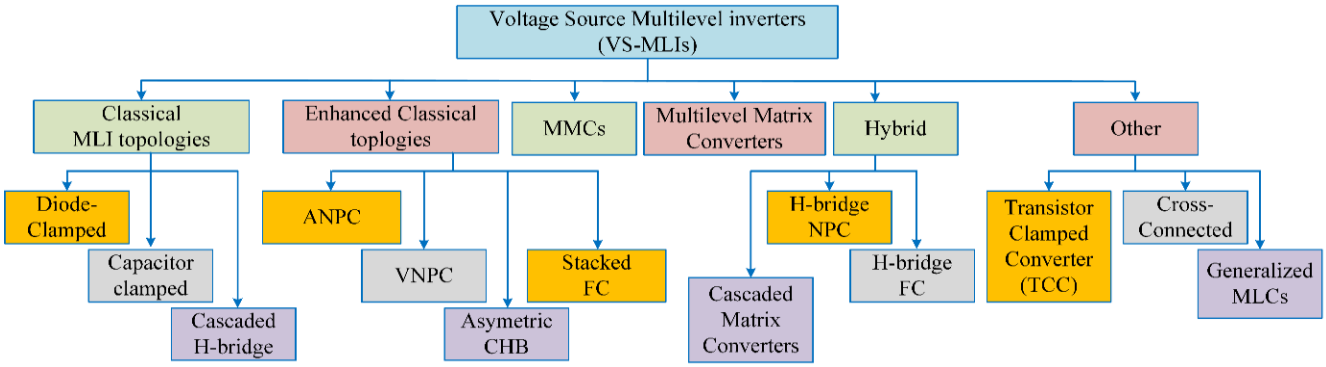

Figure 1.2 Division of multi-level inverter classes [3].

1.2 Literature Review

Basic and advanced MLC topologies essentially use multiple capacitors and power semiconductor switches connected in different configurations as basic building blocks. Due to the high capacitance per volume requirement and in order to reduce capacitor voltage ripple in the MLCs, aluminum electrolytic capacitors (AECs) are usually employed. Aluminum electrolytic capacitors

are subjected to wear-out failure due to vaporization of electrolyte and its loss over operational life [9]. According to load life test of capacitor manufacturers, a capacitor reaches end of its life-span when electrolyte is reduced by 40% or more. This 40% reduction in electrolyte can be translated into 20% reduction of capacitance from its initial value and 100% increase in equivalent series resistance (ESR). It is reported in literature that reduction in capacitance due to loss of electrolyte is responsible for the failure of power electronics system in 60% cases [10] forming weakest link in reliability context. A simple approach to improve system reliability would be to consider replacement of these capacitors when either of their electrical parameters bypass stated threshold levels of failure. Additionally, open-switch fault due to the lifting of bonding wire caused by the thermal cycling is a very common phenomenon [11]. Considering the reliability factors stated above, research efforts carried out to improve reliability of power electronic converters based systems can be segregated into three core areas as shown in Figure 1.3. Various techniques for the detection of open-switch fault are proposed, which involves sensing output voltages or load currents of converter. Open-switch fault ride through essentially involves bypassing the faulty path to operate the converter and hence, achieve desired voltage levels [12-14]. Offline methods have been proposed in [15, 16, 17] to evaluate the reliability of the converter in context to the life of capacitors. These methods involve the use of mission profile data along with probability theories to determine possible life time of capacitors. Online methods involve extraction of parameters by the sensing voltage and current components and thus predict health deterioration. Health deterioration is imperative to detect future system failure and replace failing devices before failure occurs.

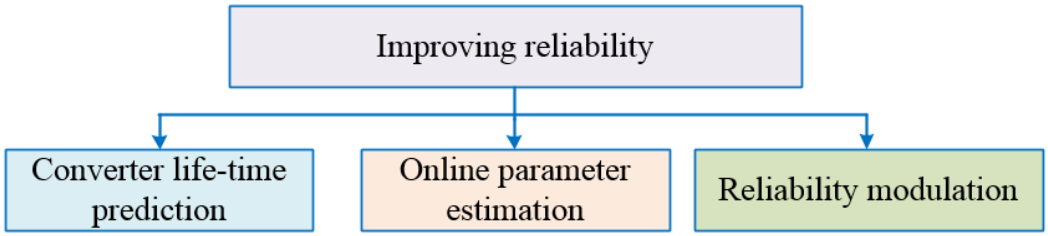

Figure 1.3 Classification of research efforts in direction of improving reliability

During past years, research on monitoring health of AECs used in power converters has been conducted and reported in [18-28]. In [18], an analogue circuit is used to capture voltage ripples across the output capacitor of a fly-back converter. This information is fed to the mathematical model in a digital signal processor to evaluate capacitance C and Equivalent Series Resistance

(ESR). In [19], inductor current is used to evaluate ESR of capacitor connected between solar panel and a boost converter. In [20], health of output capacitor in a boost converter operating as a PFC rectifier is evaluated using C and the ESR calculation models. In [21], the ESR of DC-link capacitor employed in a three-phase two-level converter is evaluated by injecting controlled ac current components. In [22], voltage injection method with support vector regression technique is used to evaluate DC-link capacitance in three-phase AC/DC/AC converter system. A non-invasive technique, which uses information on charge stored in DC-link capacitor of H-bridge is proposed to evaluate health of a DC-AC grid connected converter system in [23]. A quasi online technique using least mean squared approach is proposed in [24] to evaluate capacitance of DC-link capacitor of single-phase solar inverter. A hardware based life-cycle monitoring and voltage-managing device for DC-link electrolytic capacitors in pulse-width modulation converters is presented in [25]. A condition monitoring scheme of the DC-link capacitors in Pulse Width Modulated (PWM) inverter-fed induction machine drives with front-end diode rectifiers using forced current injection and Recursive Least Squared (RLS) method is proposed in [26]. A failure prediction scheme for Sub-Module (SM) capacitors in the Modular Multilevel Converters (MMCs) by monitoring the SM capacitor voltage oscillations and hence, evaluating its impedance at twice the fundamental frequency is proposed in [27]. In [28], naturally circulating low frequency currents along with RLS algorithm is used to evaluate SM capacitance of MMCs. The summary of above referred capacitor health monitoring techniques proposed for different power converter configurations is listed in Table 1.1. Research work in context to the online condition monitoring of the capacitors is limited to the basic converter topologies or two-level bridge legs. Though efforts in the same direction are made for the MLCs, it is limited to MMC topologies only.

Table 1.1 Different condition monitoring schemes for different converters

Reference	Power Converter	Estimated Parameter	Approach
[18]	Fly-back converter	C and ESR	Output voltage ripple
[19]	DC/DC boost converter	ESR	Inductor current ripple
[20]	AC/DC boost converter	C and ESR	C and ESR calculation model
[21]	3-ϕ 2-level AC/DC converter	ESR	Current injection with RLS
[22]	3-ϕ 2-level AC/DC/AC converter	C	Voltage injection with SVM regression

[23]	1-ϕ H-bridge 2-level converter	C	Net charge calculation
[24]	1-ϕ H-bridge 2-level converter	C and ESR	Voltage ripple with least mean square algorithm
[25]	3-ϕ 2-level DC/AC converter	ESR	Ratio of average power loss to capacitor current
[26]	3-ϕ 2-level DC/AC converter	C	Current injection with RLS method
[27]	Modular Multilevel converter	Z	Low-frequency current injection with RLS method
[28]	Modular Multilevel converter	C	Second harmonic impedance extraction

Out of the basic MLC topologies, three-level neutral-point clamped topology has found a noteworthy place as a basic building block in several commercial applications like adjustable speed drives, renewable energy grid integration, FACTS, solid state transformers, etc [1,2]. Therefore, possibility and a method of online health prediction of DC-link capacitors employed in a three-level converter as a basic block should be explored into. Sizing of DC-link capacitors is also an important aspect in system design for a specified application. Analytical expressions for the sizing of the capacitors aid as an important tool in initial design process.

1.3 Research Objectives

The objective of this thesis is to investigate the possibility and development of a technique that can be directly integrated in power converter control method and use it for the online health monitoring of DC-link capacitors in a three-level neutral point clamped converter system. Proper design of the capacitor bank employed in a multi-level converter is an important aspect that ensures reliable converter operation over its expected life cycle. An extended objective also includes development of analytical equations which can be readily used for sizing capacitor banks.

The objectives of this thesis are to:

1) Investigate possibility of development of a model, which enables use of methods for evaluating health of DC-link capacitors in three-level neutral point clamped converter.

2) Develop online method for evaluating health of DC-link capacitors in three-level neutral point clamped converter.
3) Validate the method with a high performance control scheme in hardware.
4) Develop analytical tools that enables preliminary design of capacitor bank in multilevel converter topology.

An attempt to achieve these objectives is explained briefly in the next section and in detail in the subsequent Chapters.

1.4 Thesis Outline.

In Chapter 2, control methods for multi-level converters are explored and explained. Potential existing control methods which can be integrated with the condition monitoring technique are then identified. High performance multilevel converter control method for drives application is justified.

In Chapter 3, conventional Finite Control Set Model Predictive Current Control (FCS-MPCC) scheme for three-level diode clamped converter is explained. Then based on the developed dynamic neutral point model of split capacitor bank, an indirect method to inject controlled neutral point voltage deviation between two capacitors is embedded. This embedded scheme is simulated in MATLAB Simulink environment. Proposed concept is validated on a three-level neutral point clamped converter prototype.

In Chapter 4, mathematical expressions specifying conduction intervals of the capacitors in five-level active neutral point clamped converter considering sine-triangle PWM are defined. Analytical expressions for the current stress in capacitors based on the conduction intervals are derived. Analytical expressions are validated for the several operating points of converter in MATLAB Simulink environment.

In Chapter 5, recommendation for future work associated with the condition monitoring of DC-link capacitors in three-level neutral point clamped converter system, a nested neutral point clamped converter system and MMC system is stated along with the conclusions of the thesis.

CHAPTER 2: CONTROL METHODS FOR MULTILEVEL CONVERTERS

2.1 Introduction

In a power electronic system, control of power flow is achieved by using a switching control logic implemented on a digital platform. A functional block diagram of a power electronic system is shown in Figure 2.1. A power converter control system encompasses a control method and its selection of which depends on the system constraints and technical specifications of the power converter. This Chapter reviews several control methods in their simplest forms that can be adopted in a multi-level converter. Classical hysteresis based current control, linear control that uses a carrier-based pulse width modulator (PWM) or space vector modulation (SVM), model predictive control (MPC), and an offline synchronous optimal control are studied. Finally, potential control methods to predict health of DC-link capacitors in three-level neutral point clamped converter are identified and explored in last section.

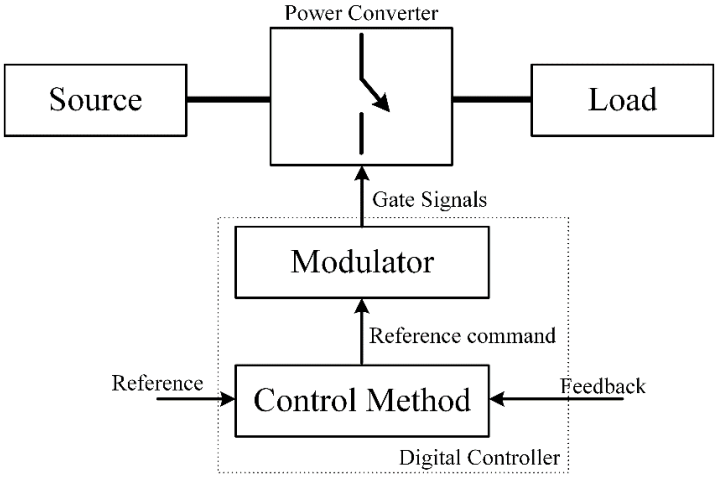

Figure 2.1 Power electronics based system

2.2 Hysteresis Current Control

The elementary concept of a hysteresis current control is to keep load current within the hysteresis limits by changing switching states of the switching devices of the converter whenever the load current moves out of the boundary [29, 30]. Figure 2.2 shows hysteresis control scheme for a three-phase two-level inverter. Sensed load current of each phase are compared with the references using

hysteresis comparator, which accepts current error as the input. Each comparator decides the switching states of the respective inverter leg devices (S_a, S_b, S_c) in such a way that the load currents are forced to stay within the limits of the hysteresis band.

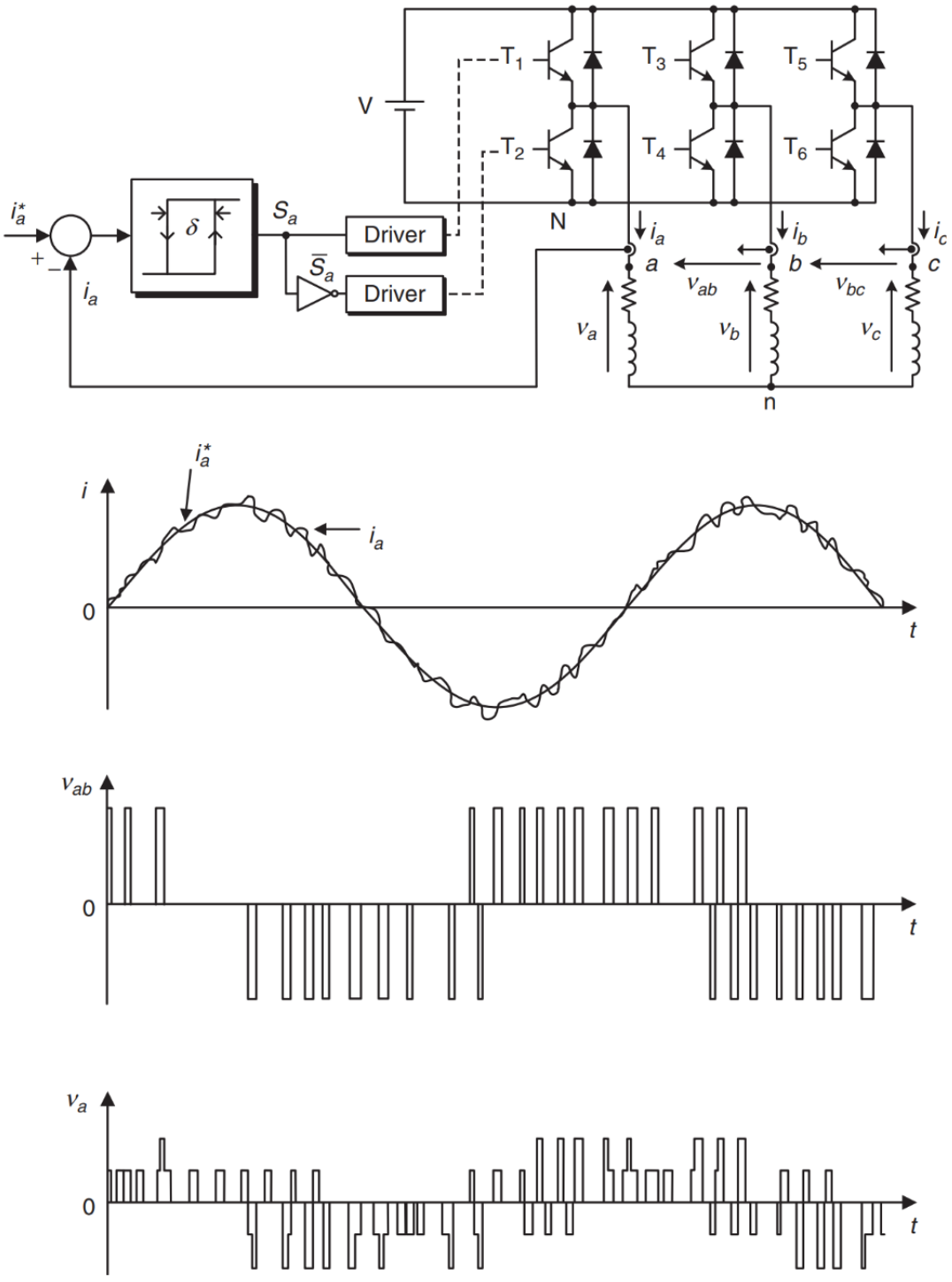

Figure 2.2 Hysteresis current control of three-phase inverter [29].

This control method is conceptually very simple, effective and its implementation avoids the use of complex circuits or digital processors. As far as dynamic performance is concerned, hysteresis controller is stable. The major drawback of hysteresis current control is that the switching frequency varies with the variation in the hysteresis width, load current, and the operating voltage conditions. Variable switching frequency can cause resonance problems. If this scheme is implemented in a digital controller, sampling frequency is required to be very high in order to keep the controlled variables within hysteresis band all the times.

2.3 Linear Control Method

If generation of gate control signals for the power semiconductor switches is considered using a pulse width modulator stage, one can linearize inherently nonlinear power converter. This enables control method to use a proportional – integral (PI) compensator for error compensation [31].

2.3.1 Carrier based Pulse Width Modulation

In a carrier based PWM, the reference voltage signal is compared with a carrier signal (triangular or saw-tooth waveform) and the output of the comparator is used to modulate the switching state of the power semiconductor switches. For a three-phase inverter, the reference voltage of each corresponding phase is compared with the carrier voltage, thus generating the switching states for the corresponding inverter leg. Figure 2.3 shows the comparison process where v_a^*, v_b^* and v_c^* are the sinusoidal three-phase reference voltages and v_{cr} is triangular carrier voltage. At any instant of time, when reference voltage is greater than carrier voltage gating signal for top switch S_x (x = a, b, c) is turned-on and turned-off when reference voltage is smaller than carrier voltage. Bottom switches for each leg operate in complement with the top switches along an appropriate dead-band. Operation of switches produces pole voltages, and line-to-line voltages v_{ab} which are shown in Figure 2.3.

2.3.2 Linear control method using Space Vector based Modulation

SVM is a type of PWM scheme, which is based on the vectorial representation of the three-phase voltages. Each voltage vector duration is calculated from the reference vector generated as command from the linear regulator. Inverter output voltages represented as vector is defined by

$$\mathbf{v} = \frac{2}{3}(v_{aN} + \boldsymbol{a}v_{bN} + \boldsymbol{a}^{\mathbf{2}}v_{cN}) \tag{2.1}$$

Where $\mathbf{a} = e^{j2\pi/3}$ and v_{aN}, v_{bN} and v_{cN} are phase-to-neutral voltages of the inverter. The output voltage of each inverter leg depends on its switching state and the voltage available on DC-link.

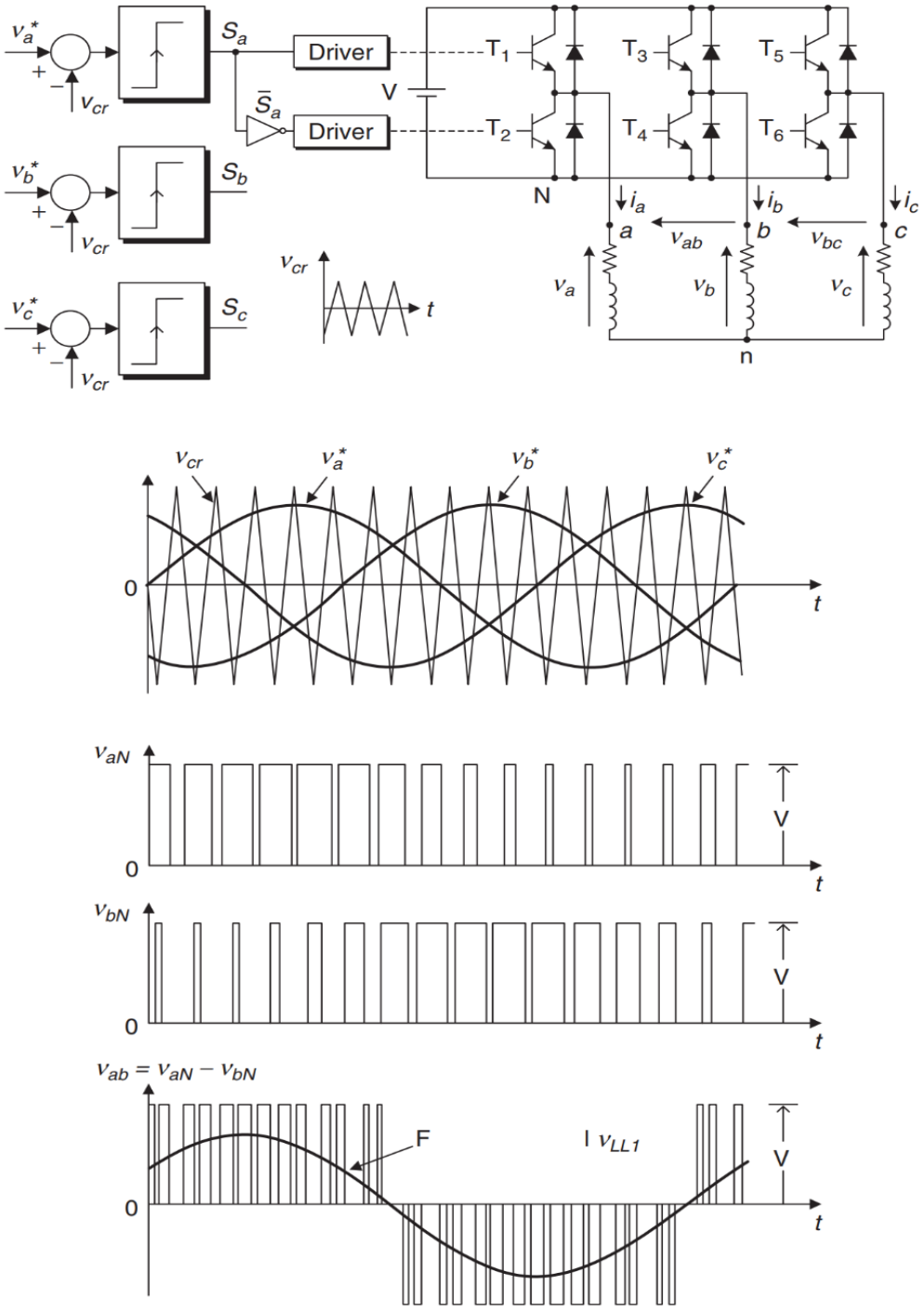

Figure 2.3 Carrier based Pulse width modulator for a three-phase inverter [29].

On accounting the switching states combination for the three-phase system, a three-phase two-level inverter generates the voltage vectors listed in Table 2.1and presented in Figure 2.4(a).

Table 2.1 Switching state and voltage vectors

S_a	S_b	S_c	Voltage vector **V**
0	0	0	$\boldsymbol{V}_0 = 0$
1	0	0	$\boldsymbol{V}_1 = \frac{2}{3}V_{dc}$
1	1	0	$\boldsymbol{V}_2 = \frac{1}{3}V_{dc} + j\frac{\sqrt{3}}{3}V_{dc}$
0	1	0	$\boldsymbol{V}_3 = -\frac{1}{3}V_{dc} + j\frac{\sqrt{3}}{3}V_{dc}$
0	1	1	$\boldsymbol{V}_4 = -\frac{2}{3}V_{dc}$
0	0	1	$\boldsymbol{V}_5 = -\frac{1}{3}V_{dc} - j\frac{\sqrt{3}}{3}V_{dc}$
1	0	1	$\boldsymbol{V}_6 = \frac{1}{3}V_{dc} + j\frac{\sqrt{3}}{3}V_{dc}$
1	1	1	$\boldsymbol{V}_7 = 0$

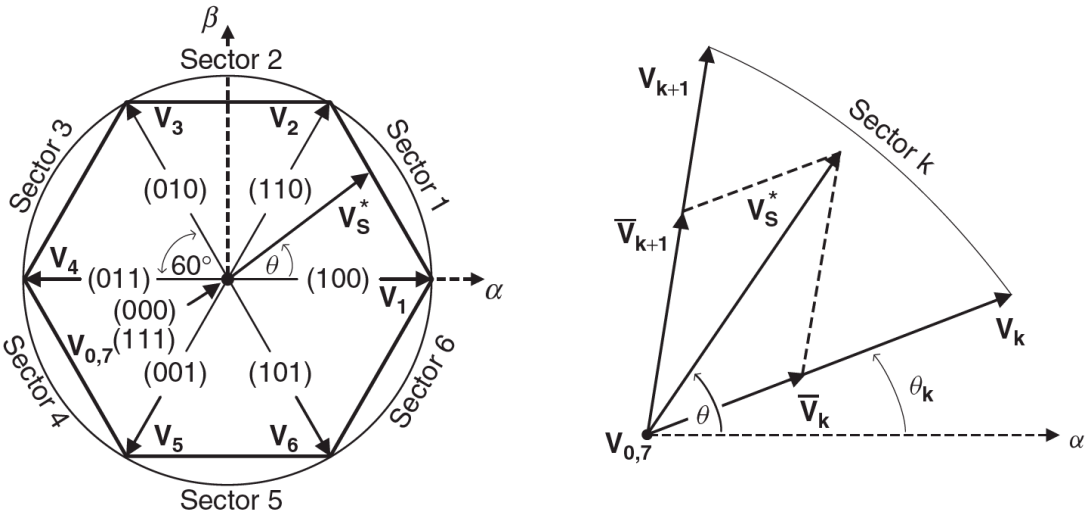

Figure 2.4 Principles of space vector based modulation (a) Voltage vectors and sector definition.[29]

Regions between each voltage vector can be considered as a sector. Hence, α – β plane can be divided into six sectors as shown in Figure 2.4(a). Based on the concept of voltage time balance, a given reference voltage vector generated by linear controller **v*,** located in a particular sector k,

can be synthesized using adjacent vectors $\mathbf{V}_k$, $\mathbf{V}_{k+1}$, and $\mathbf{V}_0$ which are applied for durations t_k, t_{k+1}, and t_0, respectively. This can be presented in the form of an equation as:

$$\mathbf{v}^* = \frac{1}{T_c}(\mathbf{V}_k t_k + \mathbf{V}_{k+1} t_{k+1} + \mathbf{V}_0 t_0) \tag{2.2}$$

$$T_c = t_k + t_{k+1} + t_0 \tag{2.3}$$

where T_c represents carrier duration and t_k/T_c , t_{k+1}/T_c and t_0/T_c are the duty cycles of their respective vectors. Using vector co-relation, the application time for each vector can be calculated as:

$$t_k = \frac{3T_c|\mathbf{v}^*|}{2V_{dc}}\left(\cos(\theta - \theta_k) - \frac{\sin(\theta - \theta_k)}{\sqrt{3}}\right) \tag{2.4}$$

$$t_{k+1} = \frac{3T_c|\mathbf{v}^*|}{V_{dc}}\frac{\sin(\theta - \theta_k)}{\sqrt{3}} \tag{2.5}$$

$$t_0 = T_c - t_k - t_{k+1} \tag{2.6}$$

Where θ corresponds the angle of reference vector $\mathbf{v}^*$and $\theta_k$is the angle of vector $\mathbf{V}_k$.

A conventional current control scheme using space vector based PWM scheme is shown in Figure 2.5. A PI controller processes the error between the load current vector and the reference current vector to generate a reference load voltage vector.

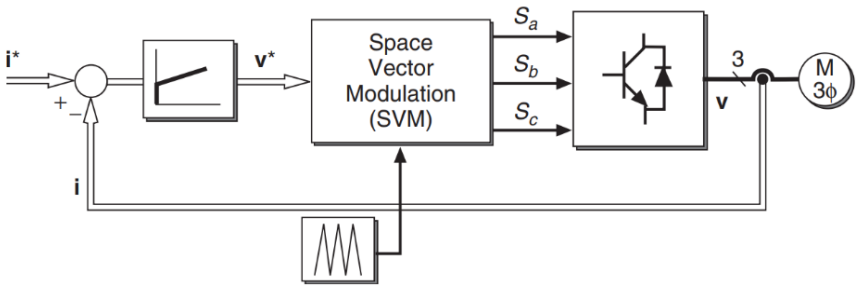

Figure 2.5 Control scheme using Space Vector based Modulation [29].

Linear control method obtains constant switching frequency by a fixed carrier waveform. The steady-state and dynamic performance of this control scheme depends on the controller parameters and on frequency of the reference current. A PI controller assures zero steady-state error for continuous reference frames. However, it presents a notable error for sinusoidal reference quantities. To overcome the problem of a PI controller compensation with sinusoidal references, a common solution is to use the present scheme after transferring coordinates from stationary to rotating reference frame in which the reference currents are converted into constant values.

2.4 Predictive Control Method.

Predictive control method encompasses a wide variety of controllers that find applications in power electronics based systems. Classification of various predictive control methods shown in Figure 2.6 is reported in [32]. Predictive control uses model of the system to predict future values of controlled variables. Predicted values of the controlled variables are used as the inputs to the controller, produce optimal actuation signals depending on the optimization criterion. In a trajectory based control, the variables are forced to follow a defined trajectory [33] while in a hysteresis based predictive control, optimization criteria is to keep the controlled variable in the limits of hysteresis band [34]. Optimal actuation in a deadbeat control makes error equal to zero in the next sampling interval [35,36]. Model predictive control (MPC) uses a flexible criterion, which is expressed as a cost function to be minimized [37]. Out of classified predictive control methods, deadbeat control and MPC with continuous control set uses a modulator while other controllers directly generate switching signals for the semiconductor switching devices. Controllers using the modulators will have constant switching frequency while controllers directly generating switching signals will have a variable switching frequency. Recently, medium/high power electronic systems are subjected to several system constraints and technical requirements like total harmonic distortion (THD), maximum current, maximum switching frequency, etc. All these constraints cannot be employed in modulator-based control schemes [38]. A simplified variant of MPC called finite control set MPC uses discrete nature of power electronic converters that simplifies the optimization problem, does not need a modulator and can be implemented online easily.

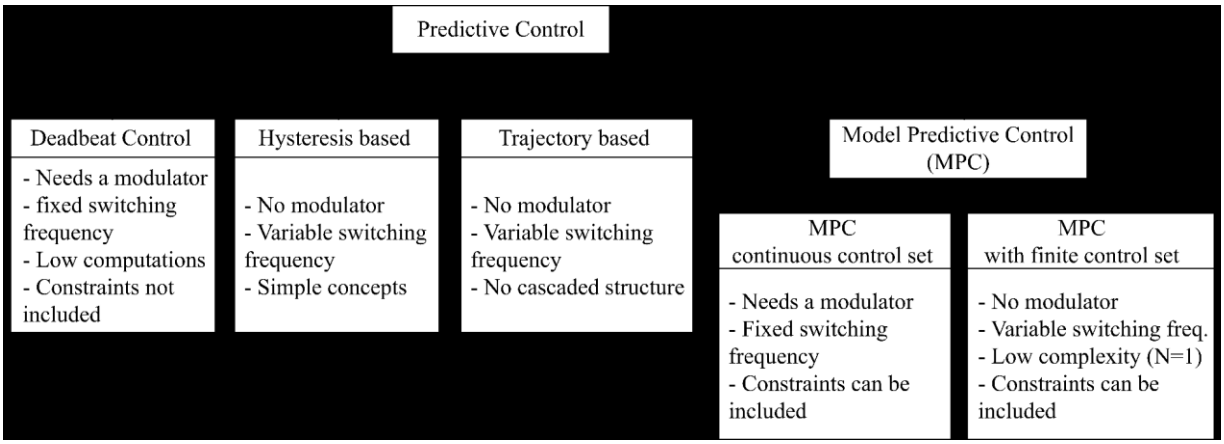

Figure 2.6 Classification of predictive control techniques [32].

2.4.1 Finite Control Set Model Predictive Control

Design stage of finite control set MPC for the control of power electronics based system involves several steps which are listed as follows:

- Modeling the power converter in terms of all possible switching states and its co-relation to the voltages and currents.
- Defining control cost function, which presents system behavior.
- Obtain discrete-time equivalent models that allow the prediction of controlled variables.

Modeling power converter involves considering power semiconductor switches operating in two discrete states, ON and OFF state. Therefore, the total number of possible switching states for a power electronic converter depends upon the number of different combinations of switching states for each semiconductor switch. Combinations that lead to the short circuit of DC-link are excluded. A general rule stating number of possible switching states N can be stated as

$$N = x^y \tag{2.7}$$

where, x represents possible states of each converter leg, and y is number of phases (or legs). Every application defines its own control requirements such as current control, voltage control, torque control, switching frequency constraints, etc. These requirements are expressed in the form of a cost function. A digital controller calculates optimal switching states, which minimizes this cost function. Though the elementary cost function to be defined is a measure of error between reference and predicted variables, it is possible to control different types of variables by including restrictions in the cost function. Discrete-time equivalents of a system model for prediction are obtained by using forward Euler method. System constraints such as low harmonic distortion, low device switching frequency and fast dynamic responses are achieved simultaneously using this method. A control technique, which achieves these constraints simultaneously using an offline modulation is worth noting and explained briefly in the next section.

2.5 Synchronous Optimal Control

Synchronous optimal control technique is developed specifically for motor drives applications. Similar to linear control methods, synchronous optimal control method uses linear regulators to achieve control of load variables.

2.5.1 Synchronous Optimal Pulse Width Modulation

To implement synchronous optimal PWM, sequences of switching state vector and their dwell time duration are pre-calculated for the entire range of the modulation index m. It is to be noted that this sequence forms a pulse pattern, which is repeated every fundamental cycle. Calculations are usually done offline, assuming steady-state operation and satisfying specified optimization criterion [39]. Optimization criterions include current distortion, switching losses and switch utilization. Block diagram of a synchronous optimal PWM is shown in Figure 2.7. Pre-calculated pulse patterns for all the operating conditions are saved in a form of a look-up table. Depending upon the modulation command coming from the control system, a pulse pattern is loaded and pulses are generated with specified dwell times in a sequence.

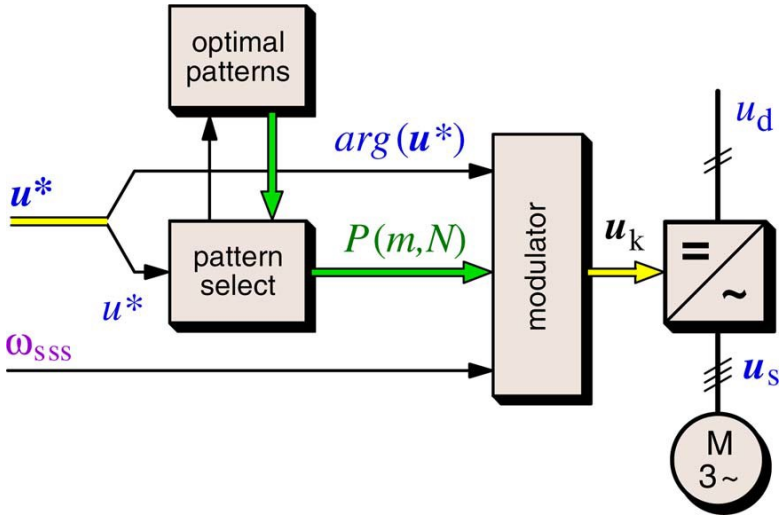

Figure 2.7 Synchronous optimal modulation [38].

This modulation technique inherently satisfies simultaneous requirements of lower harmonic distortion, and the device switching losses. One disadvantage of this modulation technique in its simplest form is in terms of dynamic performance as it is not able to maintain optimal pulse pattern during dynamic conditions. However, this disadvantage is overcome with advanced control methods [38].

2.6 Potential Control Methods for Online Condition Monitoring

Considering the objective of online health monitoring of DC-link capacitors in a three-phase three-level neutral point clamped converter operated as an inverter using dynamic neutral point model, the following advanced control methods listed below have potential application.

- Linear control method based on carrier PWM proposed in [40]. In this method, two DC-link capacitor voltages are balanced by use of a proportional regulator, which introduces an offset voltage proportional to degree of unbalance in the modulating signal used as a reference in carrier based PWM method. To ensure balanced capacitor voltages, reference to this regulator is zero. If the reference to the regulator is non-zero ie. A sinusoidal low frequency low amplitude quantity, the difference between two capacitor voltages will follow the same reference and hence provide ability to monitor health in terms of capacitance of dynamic neutral point model.
- Linear control method based on SVM proposed in [41]. In this control method, a space vector based modulation method is proposed where simultaneous voltage control, neutral point voltage control and switching loss reduction is achieved. Like carrier based control method, this modulation method has a potential for injecting sinusoidal DC-link capacitor voltage difference and hence ability of online condition monitoring.
- Finite control set model predictive control proposed in [42]. It uses model of a three-phase three-level neutral-point clamped converter. The cost function g is designed to include terms dedicated to achieve reference tracking, voltage balance in the DC-link, and reduction of device switching frequency. Importance of control variables in cost function is adjusted using respective weights. Inclusion of neutral point voltage control in the cost function and the ability to adjust its relative importance using weights makes this method a potential candidate to be used for online condition monitoring technique.

2.7 Conclusion

In this Chapter, various control methods, which have been used for the multi-level converters in their simplest form are reviewed. Out of these methods, and based on the condition monitoring requirement, potential control methods, which can readily utilize the dynamic neutral point model

are listed. Linear control method based on SVM provides high dynamic performance compared to the methods based on the carrier PWM. But ongoing continuous requirement on the reduction in harmonic distortion and reduction of device switching frequency with high dynamic performance in applications such as electric drives, linear control method with SVM is not sufficient enough. Synchronous optimal PWM method satisfies all the requirements of low harmonic distortion in load current and reduced device switching frequency while maintaining attribute of high dynamic performance. It achieves these desirable merits due to utility of linear regulators in control stage and utility of look-up table stored highly optimized pulse patterns. Reliability of multi-level converters depends on reliability of switches, gate driving circuitry and the energy storage elements viz. Aluminum electrolytic capacitors. Since bond wire failure of semiconductors in switches is addressed by reliability modulation and gate driving circuitry is robust due to use of advanced electronics circuitry, capacitors form the weakest link in reliability context. Online condition monitoring techniques requires timely injection of sinusoidal current/ voltage components. Use of offline look-up table limits integration of online condition monitoring in synchronous optimal control method. Finite control set model predictive control is simple, online and retains all desirable qualities like synchronous optimal PWM control. Due to high dynamic performance while retaining implementation simplicity this control technique is often found in Industrial applications. The concept of online health monitoring of DC-link capacitors used in three-phase three-level neutral point clamped converter is explored using finite control set model predictive control scheme.

The next Chapter introduces the concept of finite control set model predictive current control (MPCC) for three-level neutral point clamped converter operated as an inverter and explains the online condition monitoring concept embedded with this control method.

CHAPTER 3: A FINITE CONTROL SET MODEL PREDICTIVE CURRENT CONTROL OF 3-LEVEL NEUTRAL POINT CLAMPED CONVERTER WITH CONDITIONING MONITORING OF DC-LINK CAPACITORS.

3.1 Introduction

This chapter presents a Finite Control Set (FCS) Model Predictive Current Control (MPCC) scheme for a 3-level neutral point clamped (NPC) converter with condition monitoring of DC-link capacitors by evaluating impedance of dynamic neutral point model. First section describes mathematical modeling of three-level neutral point clamped inverter and connected load. Control design process of FCS-MPCC is presented in second section. Third section presents embedding of proposed condition monitoring method with FCS-MPCC. Proposed method is validated using MATLAB Simulink simulation environment in fourth section. Implementation and validation of the concept with laboratory developed hardware prototype is presented in the last section.

3.2 Mathematical Modeling

One of the elementary steps in designing FCS-MPCC for a power electronic system involves deriving model equations that represents behavior of the system. Since power electronic converter system is non-linear due to power semiconductors operating in ON-OFF states (saturated - cutoff regions), a power converter model can be derived using possible switching state combinations. Differential equations presenting a generic load model can be developed considering that the converter is connected to a three-phase balanced series connected resistive inductive and ac voltage source (RLE) load configuration.

3.2.1 Power Converter Model

Figure 3.1 shows a three-phase three-level NPC inverter circuit that converts electrical power from DC to AC form through power semiconductor switching devices (IGBTs). Each inverter leg consists of four active switches (IGBTs) and two clamping diodes where inner switches ($S_{2x}, S_{1x}{}'$)

and clamping diodes (D_{1x}, D_{2x}) enable the converter output terminal to be connected to the neutral point (z) of the DC-link.

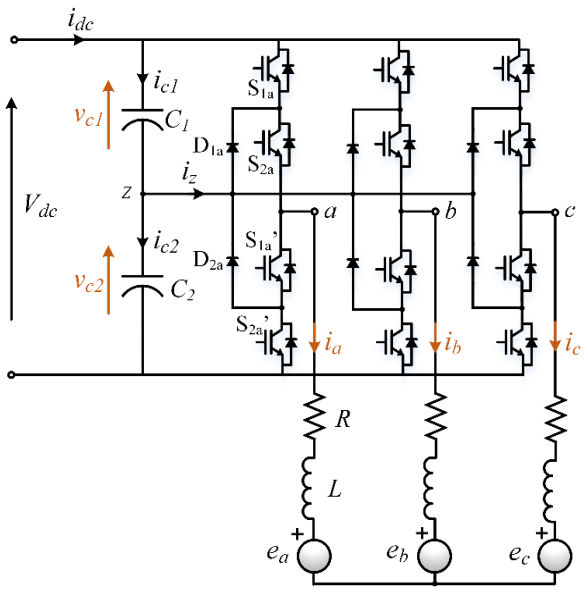

Figure 3.1 Three-phase three-level neutral point clamped inverter power circuit

Neutral point is obtained through midpoint of two series connected DC-link capacitors. Operation of each switch is represented by its switching function as,

$$S_{xy} = \begin{cases} 1, & \text{when switch is conducting} \\ 0, & \text{when switch is blocking} \end{cases} \tag{3.1}$$

The switching state variable S_x represents the switching state of phase x, with $x = \{a, b, c\}$. Considering switching states as stated in Table 3.1, switching state variable can take three values denoted by P, O and N that represent the switching combinations. This circuit configuration allows generation of three voltage levels at the output terminal with respect to neutral point (z). To account for the variation in neutral-point voltage and its effects, inverter leg voltages are represented in terms of voltage across capacitors instead of absolute values of DC link voltages. Forced variation of neutral-point voltage is essential for the requirements of condition monitoring aspect of the scheme which will be explained in the chapter later.

Table 3.1 Switching states of inverter leg

S_x	S_{x1}	S_{x2}	S_{x1}'	S_{x2}'	v_{xz}
P	1	1	0	0	V_{c1}
O	0	1	1	0	0
N	0	0	1	1	$-V_{c2}$

The pole voltage defined as voltage between the load terminal and the neutral point of DC-link for each inverter leg can be written by (3.2), (3.3) and (3.4) as,

$$v_{az} = S_{a1}v_{c1} + (S_{a2} - 1)v_{c2} \tag{3.2}$$

$$v_{bz} = S_{b1}v_{c1} + (S_{b2} - 1)v_{c2} \tag{3.3}$$

$$v_{cz} = S_{c1}v_{c1} + (S_{c2} - 1)v_{c2} \tag{3.4}$$

where, v_{c1}, v_{c2} are the voltages across the two capacitors.

Operation of each inverter leg is phase-shifted by 120°, therefore, using an unitary vector, **a** = $e^{j2\pi/3}$ inverter output voltage can be written in vector form as,

$$\mathbf{v} = \frac{2}{3}(v_{az} + \mathbf{a}v_{bz} + \mathbf{a}^2 v_{cz}) \tag{3.5}$$

Three phases and three possible switching states for each converter leg results in 27 unique switching state combinations. Let us consider a switching state combination (S_a,S_b,S_c) = (P,N,O), the output voltage vector corresponding to specified switching state combination can be derived as,

$$\begin{aligned}\mathbf{V}_{PNO} &= \frac{2}{3}\left(V_{c1}e^{j0} - V_{c2}e^{\frac{j2\pi}{3}} + 0e^{\frac{j4\pi}{3}}\right) \\ &= \left(\frac{2V_{c1}}{3} + \frac{V_{c2}}{3}\right) - j\frac{1}{\sqrt{3}}(V_{c2})\end{aligned} \tag{3.6}$$

Likewise, voltage vector for every possible switching state combination can be evaluated. The voltage vector for all switching state combinations are stated in Table 3.2. Each voltage vector can be represented by a distinct location in a two-dimensional complex plane.

Table 3.2 Voltage vectors and switching states

Space Vector	Switching State	Vector Definition	Vector Definition ($V_{c1} = V_{c2} = V_{dc}/2$)
$\mathbf{V}_0$	[PPP], [OOO], [NNN]	$0 + j\,0$	$0 + j\,0$
$\mathbf{V}_1$	[PPO]	$2V_{c1}/3 + j\,0$	$V_{dc}/3 + j\,0$
$\mathbf{V}_2$	[ONN]	$2V_{c2}/3 + j\,0$	$V_{dc}/3 + j\,0$
$\mathbf{V}_3$	[PPO]	$V_{c1}/3 + j\,(1/\sqrt{3})V_{c1}$	$V_{dc}/6 + j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_4$	[OON]	$V_{c2}/3 + j\,(1/\sqrt{3})V_{c2}$	$V_{dc}/6 + j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_5$	[OPO]	$-V_{c1}/3 + j\,(1/\sqrt{3})V_{c1}$	$-V_{dc}/6 + j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_6$	[NON]	$-V_{c2}/3 + j\,(1/\sqrt{3})V_{c2}$	$-V_{dc}/6 + j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_7$	[OPP]	$-2V_{c1}/3 + j\,0$	$-V_{dc}/3 + j\,0$
$\mathbf{V}_8$	[NOO]	$-2V_{c2}/3 + j\,0$	$-V_{dc}/3 + j\,0$

$\mathbf{V}_9$	[OOP]	$-V_{c1}/3 - j\,(1/\sqrt{3})V_{c1}$	$-V_{dc}/6 - j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{10}$	[NNO]	$-V_{c2}/3 - j\,(1/\sqrt{3})V_{c2}$	$-V_{dc}/6 - j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{11}$	[POP]	$V_{c1}/3 - j\,(1/\sqrt{3})V_{c1}$	$V_{dc}/6 - j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{12}$	[ONO]	$V_{c2}/3 - j\,(1/\sqrt{3})V_{c2}$	$V_{dc}/6 - j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{13}$	[PON]	$(2V_{c1}+ V_{c2})/3 + j\,(1/\sqrt{3})V_{c2}$	$V_{dc}/2 + j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{14}$	[OPN]	$(-V_{c1}+ V_{c2})/3 + j\,(1/\sqrt{3})(V_{c1}+ V_{c2})$	$0 + j\,(1/\sqrt{3})V_{dc}$
$\mathbf{V}_{15}$	[NPO]	$(-V_{c1} - 2V_{c2})/3 + j\,(1/\sqrt{3})V_{c1}$	$-V_{dc}/2 + j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{16}$	[NOP]	$(-V_{c1} - 2V_{c2})/3 - j\,(1/\sqrt{3})V_{c1}$	$-V_{dc}/2 - j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{17}$	[ONP]	$(-V_{c1}+ V_{c2})/3 - j\,(1/\sqrt{3})(V_{c1}+ V_{c2})$	$0 - j\,(1/\sqrt{3})V_{dc}$
$\mathbf{V}_{18}$	[PNO]	$(2V_{c1}+ V_{c2})/3 - j\,(1/\sqrt{3})V_{c2}$	$V_{dc}/2 - j\,(1/2\sqrt{3})V_{dc}$
$\mathbf{V}_{19}$	[PNN]	$(2V_{c1}+ 2V_{c2})/3 + j\,0$	$2V_{dc}/3 + j\,0$
$\mathbf{V}_{20}$	[PPN]	$(V_{c1}+ V_{c2})/3 + j\,(1/\sqrt{3})(V_{c1}+ V_{c2})$	$V_{dc}/3 + j\,(1/\sqrt{3})V_{dc}$
$\mathbf{V}_{21}$	[NPN]	$-(V_{c1}+ V_{c2})/3 + j\,(1/\sqrt{3})(V_{c1}+ V_{c2})$	$-V_{dc}/3 + j\,(1/\sqrt{3})V_{dc}$
$\mathbf{V}_{22}$	[NPP]	$-(2V_{c1}+ 2V_{c2})/3 + j\,0$	$-2V_{dc}/3 + j\,0$
$\mathbf{V}_{23}$	[NNP]	$-(V_{c1}+ V_{c2})/3 - j\,(1/\sqrt{3})(V_{c1}+ V_{c2})$	$-V_{dc}/3 - j\,(1/\sqrt{3})V_{dc}$
$\mathbf{V}_{24}$	[PNP]	$(V_{c1}+ V_{c2})/3 - j\,(1/\sqrt{3})(V_{c1}+ V_{c2})$	$V_{dc}/3 - j\,(1/\sqrt{3})V_{dc}$

Use of additional voltage level generated from series connected DC-link capacitor causes deviation in the voltages across the two capacitors. One such case when phase - B is connected to the neutral point (z) is shown in Figure 3.2. Upper and lower capacitors may charge or discharge depending on neutral point current direction.

Figure 3.2 Circuit with phase - B connected to neutral point.

The equation governing the neutral point current and the voltage difference between two capacitors is given by (3.7) and (3.8) respectively,

$$i_Z = (1 - S_{a1})S_{a2}i_a + (1 - S_{b1})S_{b2}i_b + (1 - S_{c1})S_{c2}i_c \tag{3.7}$$

$$\frac{dv_\Delta}{dt} = \frac{1}{C_1 + C_2} i_Z \tag{3.8}$$

where, $v_\Delta = v_{C1} - v_{C2}$.

3.2.2 Load Model

Accounting a generalized load model connected to inverter circuit as shown in Figure 3.1, differential equation that presents correlation of inverter phase voltage and dynamics of load current can be stated by,

$$v_{aZ} = L\frac{di_a}{dt} + Ri_a + e_a + v_{nz} \tag{3.9}$$

$$v_{bZ} = L\frac{di_b}{dt} + Ri_b + e_b + v_{nz} \tag{3.10}$$

$$v_{aZ} = L\frac{di_c}{dt} + Ri_c + e_c + v_{nz} \tag{3.11}$$

By substituting (3.9)-(3.11) into (3.5) a vector representation of (3.9)-(3.11) can be written as

$$\begin{aligned}\mathbf{v} = L\frac{d}{dt}\left(\frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c)\right) + R\left(\frac{2}{3}(i_a + \mathbf{a}i_b + \mathbf{a}^2 i_c)\right) \\ + \frac{2}{3}(e_a + \mathbf{a}e_b + \mathbf{a}^2 e_c) + \frac{2}{3}(v_{nz} + \mathbf{a}v_{nz} + \mathbf{a}^2 v_{nz})\end{aligned} \tag{3.12}$$

Thus inverter voltage vector **v**, load current vector **i** and emf vector **e** can be correlated as

$$\mathbf{v} = R\mathbf{i} + L\frac{d\mathbf{i}}{dt} + \mathbf{e} \tag{3.13}$$

3.2.3 Discrete-Time Model for Prediction

Prediction of variables to be controlled require discretization of continuous system variables over a specified sampling time T_s. Considering that the load can be modeled as a first order system, discretization process is a simple approximation of derivative. The derivative is approximated by replacing derivative quantity by a forward Euler approximation which can be stated by (3.14) as,

$$\frac{dx}{dt} \approx \frac{x[k+1] - x[k]}{T_s} \tag{3.14}$$

Equation (3.14) when substituted in (3.13) derives an expression that allows prediction of future load current vector at time $k + 1$, for each possible voltage vector $\mathbf{v}[k]$ generated by the converter. The expression can be stated as

$$\mathbf{i}^{\mathrm{p}}[k+1] = \left(1 - \frac{RT_s}{L}\right)\mathbf{i}[k] + \frac{T_s}{L}(\mathbf{v}[k] - \hat{\mathbf{e}}[k+1]) \tag{3.15}$$

where, $\hat{\mathbf{e}}[k]$ denotes estimated emf. The subscript **p** denotes the predicted variables.

The emf vector can be calculated from (3.13) considering measurements of the inverter voltage vector and current vector with the expression;

$$\hat{\boldsymbol{e}}[k] = \hat{\boldsymbol{e}}[k-1] = \mathbf{v}[k-1] - \frac{L}{T_s}\mathbf{i}[k] - \left(R - \frac{L}{T_s}\right)\mathbf{i}[k-1] \tag{3.16}$$

Similarly, the expression that allows prediction of difference voltage obtained by substituting (3.14) in (3.8) and can be stated by

$$v_{\Delta}{}^{\mathrm{p}}[k+1] = v_{\Delta}[k] + \frac{1}{C_1 + C_2}\, i_z[k] \tag{3.17}$$

where, $i_z[k]$ is every possible neutral point current for respective switching state combinations which is obtained using (3.7).

3.3 Control Design

For the sake of understanding, conventional FCS-MPCC for a three-phase three-level inverter will be explained first. Then the possibility of condition monitoring will be elaborated and finally FCS-MPCC scheme with condition monitoring will be discussed thoroughly.

3.3.1 Conventional FCS-MPCC Scheme

Block diagram of FCS-MPCC scheme for a three-phase three level inverter based system is shown in Figure 3.3. Future values of the load currents and capacitor voltages are predicted for 27 possible switching state combinations of inverter using (3.15), (3.18) and (3.19).

$$v_{c1}{}^{p}[k+1] = v_{c1}[k] + \frac{1}{C_1} i_{c1}[k] T_s \tag{3.18}$$

$$v_{c2}{}^{p}[k+1] = v_{c2}[k] + \frac{1}{C_2} i_{c2}[k] T_s \tag{3.19}$$

After obtaining predictions, a cost function g is evaluated for each switching state combination. The switching state combination that minimizes the cost function is selected and applied during the next switching period.

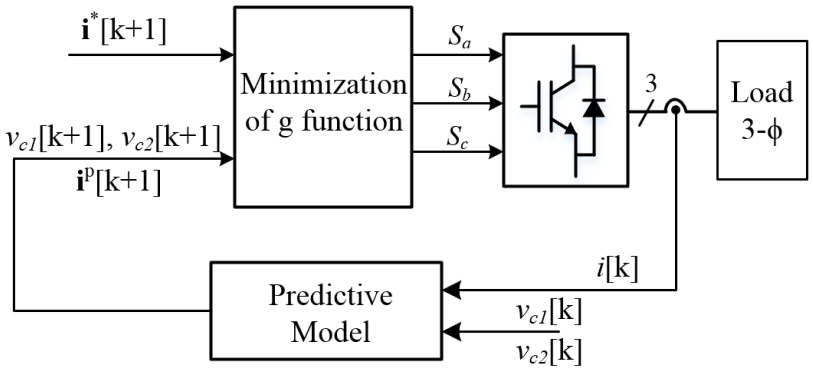

Figure 3.3 Conventional Predictive Current Control for NPC Inverter

The control requirements of three-level NPC Inverter are defined by:

- Load current reference tracking.
- Balancing voltages of DC link capacitors.
- Device switching frequency reduction.

The control requirements are formulated in the form of a cost function which is required to be minimized. The cost function to control three-phase three-level inverter is composed of

$$g = \left|{i_\alpha}^* - {i_\alpha}^P\right| + \left|{i_\beta}^* - {i_\beta}^P\right| + \lambda_{dc}|{v_{c1}}^P - {v_{c2}}^P| + \lambda_n n_c \qquad (3.20)$$

The first two terms constitute load current errors obtained as the difference of reference and predicted quantities in orthogonal trajectories. The third term in (3.20) measures the difference in predicted values of DC link capacitor voltages. These predicted voltages are calculated using (3.18) and (3.19). The last term accounts for the number of commutations required to switch from the present switching state combination to the switching state combination under evaluation. The weighting factors λ_{dc} and λ_n adjusts the relation between terms associated with reference tracking, voltage balance, and reduction of switching frequency within the function g.

3.3.2 Dynamic Neutral-Point Model and its Impedance Predictability in a Three-Level Converter.

As shown in Figure 3.4, when neutral point is accessed by the converter to obtain additional voltage level, a current flows through the neutral point (z). This current depends on the load phases connected to the neutral point and the load current flowing through each of these phases. Let us assume a condition in which neutral point current is in the positive direction. This current is composed of two parts, the first will charge the upper capacitor and the second will discharge the lower capacitor. Change in each capacitor voltage is due to these charging and discharging currents. This change in voltage is identical to the change in voltage of a configuration with two capacitors connected in parallel when fed by the same amount of current. Due to identical variation in the capacitor voltages, series connected neutral point configuration during dynamic condition can be modeled as two capacitors connected in parallel.

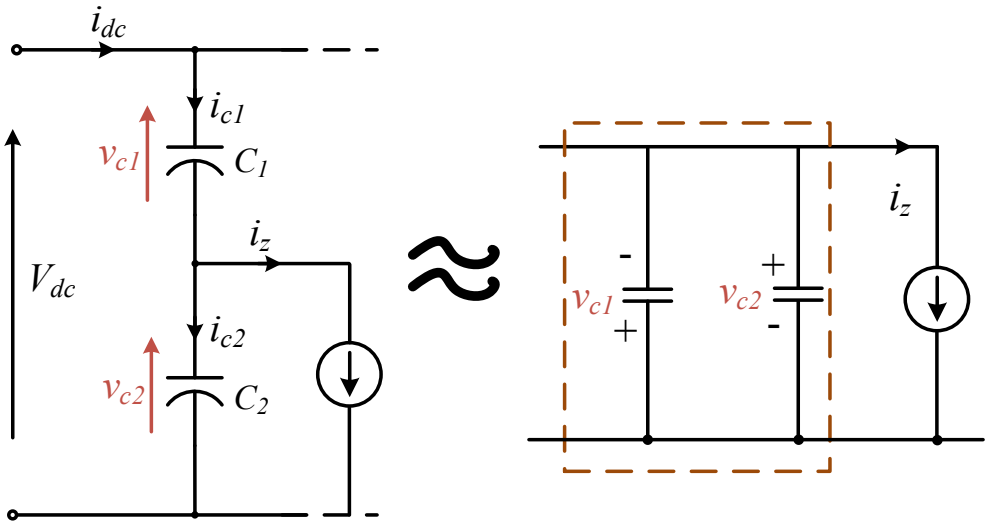

Figure 3.4 Dynamic neutral point model

Since neutral point current is a function of the switching state combination and load currents stated in (3.7). A controlled co-sinusoidal neutral point current can cause sinusoidal variation in voltage across dynamic model. Similarly, forcing sinusoidal variation of voltage difference between two DC-link capacitors will cause indirect injection of co-sinusoidal neutral point current i_z. This forced sinusoidal variation can be achieved appropriately by formulating cost function in a FCS-MPCC scheme. Root Mean Square (RMS) quantities of this injected current and the voltage

variation can be used to estimate Impedance of the dynamic model. Impedance of this equivalent configuration can be stated by,

$$Z_{dyn} = \frac{1}{2\pi f_{inj}(C_1 + C_2)} \tag{3.21}$$

Estimated impedance of dynamic neutral-point model can be used to monitor the condition of the capacitors to an extent. This concept can be exploited to obtain FCS-MPCC for a three-level NPC inverter with condition monitoring which is explained in the next section.

3.3.3 FCS-MPCC with Condition Monitoring

The FCS-MPCC scheme with condition monitoring for a three-phase three-level NPC inverter-based system is shown in Figure 3.5. The next values of the load currents are evaluated using (3.15). However, the future capacitor voltage difference is predicted using (3.17). Unlike the conventional scheme, this equation not only allows to maintain capacitor voltage balance, but also allows to control the difference voltage v_{Δ} as per the requirement. After obtaining the predictions, a cost function g (3.22) is evaluated for each switching state combination. Then, the switching state combination with minimum cost function is applied during the next switching period.

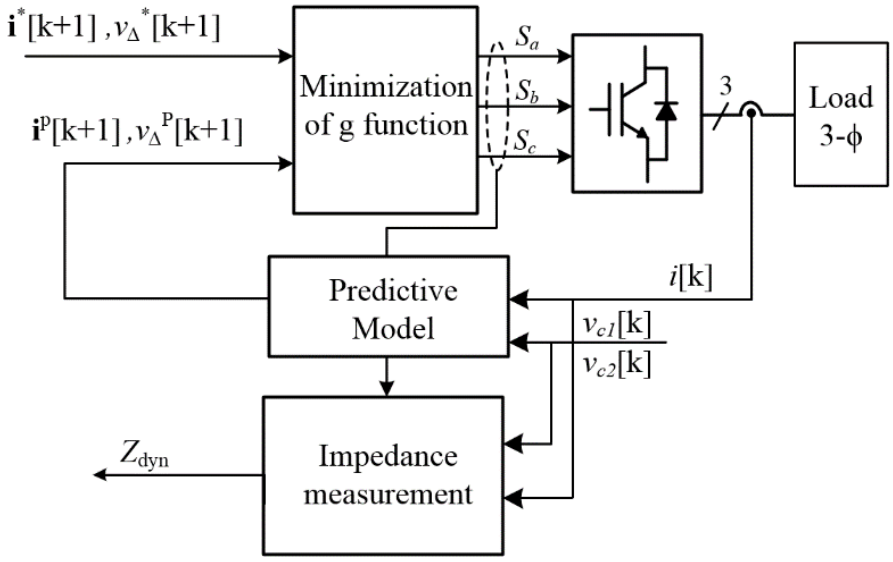

Figure 3.5 FCS-MPCC of NPC inverter with Condition Monitoring

The control requirements for FCS-MPCC with condition monitoring can be defined by:

- Load current reference tracking.
- Controlling difference voltage v_{Δ} of capacitors.
- Switching frequency reduction.

The control requirements are formulated in the form of a cost function, which is required to be minimized. The three-level inverter cost function is composed as:

$$g = |i_{\alpha}{}^{*} - i_{\alpha}{}^{\mathrm{p}}| + \left|i_{\beta}{}^{*} - i_{\beta}{}^{\mathrm{p}}\right| + \lambda_{dc}|v_{\Delta}{}^{*} - v_{\Delta}{}^{\mathrm{p}}| + \lambda_{n} n_{c} \tag{3.22}$$

Third term in (3.22) accounts for voltage difference errors. This term allows the control scheme to track a reference voltage difference $v_{\Delta}{}^{*}$. Maintaining $v_{\Delta}{}^{*}$ to zero will ensure balance of the voltages across the two capacitors. Any value of $v_{\Delta}{}^{*}$ other than zero can be achieved using (3.22). Difference voltage controllability enables dynamic model impedance estimation and hence, the condition monitoring ability. Use of third term eliminates the requirement of sensing DC current also. Other terms in cost function operate similar to the conventional scheme.

3.4 Algorithm Implementation

The FCS-MPCC algorithm in the form of a flow chart is shown in Figure 3.6. Since prediction algorithm has to predict controlled variables at the end of next switching interval and the digital computation requires a finite duration of time, two step predictive method is used. The control algorithm begins by sampling of the load currents and the individual capacitor voltages. The values of the load current vector **i** individual capacitor voltages v_{c1}, v_{c2} and emf vector **e** at the end of current sampling interval are predicted using applied voltage vector (switching state combination). A variable g_{op}, that will contain the lowest calculated value of the cost function evaluated by the algorithm so far is initialized to infinite. Then the scheme enters a loop where, for each possible switching state combination, the cost function (3.22) is evaluated considering current and voltage predictions obtained from (3.15) and (3.17), respectively. If, for a specific switching state combination, the evaluated cost function g is lower than g_{op}, that lower value of cost function is stored as g_{op} and the number associated to switching state combination is stored as j_{op}. The control loop ends when all 27 switching states have been evaluated. Switching state combination that produces the optimal value of g (minimal) is identified by variable j_{op} and will be applied to the

converter at the beginning of the next switching interval. The process is repeated again for the next switching interval.

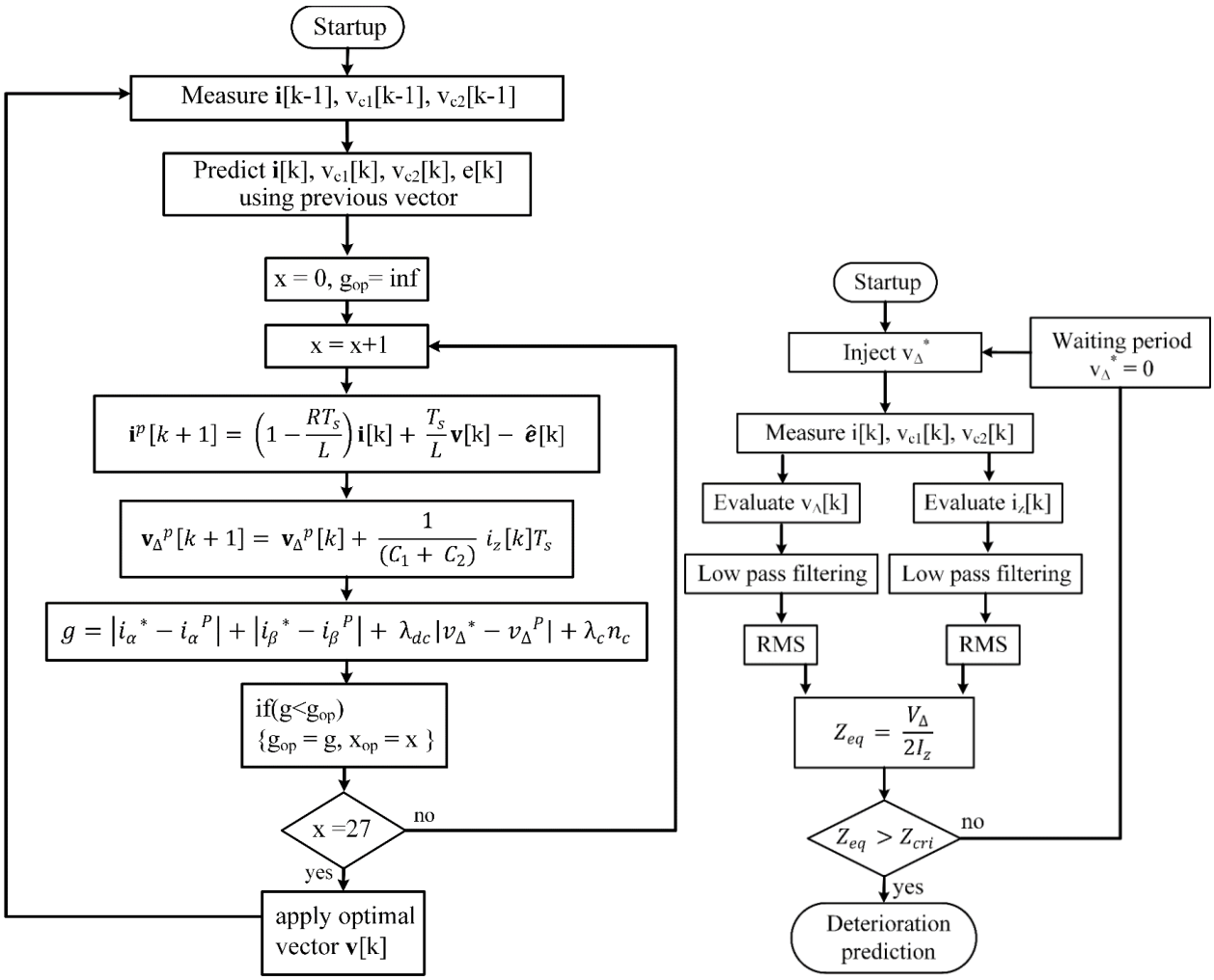

Figure 3.6 Flow chart of predictive control algorithm with condition monitoring

An auxiliary algorithm embeds condition monitoring inside FCS-MPCC, which is invoked in timely manner to evaluate impedance of dynamic neutral-point model. During normal operation, the auxiliary algorithm is in wait state with $v_\Delta{}^* = 0$ and the FCS-MPCC algorithm operates like conventional algorithm. When auxiliary algorithm leaves wait state after a stipulated amount of time, sinusoidal voltage difference is forced by $v_\Delta{}^*$ with a very low sub-harmonic frequency. Primary control algorithm forces the voltage difference to track reference voltage difference by indirect injection of neutral point current using the control cost function.

Sensed load currents and switching state combination are used to estimate neutral point current and difference voltage using (3.7) and $v_{C1}[k] - v_{C2}[k]$, respectively. Obtained Neutral point

current i_z and difference voltage v_Δ are filtered using low-pass FIR filter with a cutoff frequency of 60 Hz to extract sub-harmonic frequency components. Impedance of dynamic model is obtained as ratio of filtered difference voltage v_Δ to filtered neutral point current i_z. As capacitors in the DC-link deteriorates, its capacitance reduces. Reduction of capacitance causes increase in dynamic Impedance. If evaluated impedance is higher than its critical value, a deteriorated condition can be predicted.

3.5 Choice of difference voltage injection frequency

Proposed condition monitoring technique requires injection of sinusoidal difference voltage through control algorithm. Difference between the capacitor voltages is generated due to neutral point current, indicating requirement of indirect neutral point current injection. Correlation between sinusoidal voltage difference v_Δ and neutral point can be stated by,

$$i_z = 2\pi f_{inj}(C_1 + C_2)V_{\Delta m}\cos\omega_{inj}t \tag{3.23}$$

And maximum value of neutral point current can be given by,

$$i_{z,m} = 2\pi f_{inj}(C_1 + C_2)V_{\Delta m} \tag{3.24}$$

Total capacitance in DC-link is usually a large value, which is fixed and maximum difference voltage should be large enough for the voltage sensors to sense the difference voltage with good resolution. Hence for successful difference voltage injection, difference voltage injection frequency f_{inj} in (3.24) should be as low as possible to ensure right hand side of (3.24) is lower than the neutral point current injection capacity of the converter. Maximum injection frequency can be stated as,

$$f_{inj,max} \leq \frac{i_{z,m}}{2\pi(C_1 + C_2)V_{\Delta m}}$$

3.6 Simulation results

To study FCS-MPCC strategy and viability of condition monitoring, a three-level NPC inverter feeding an RL load is simulated in MATLAB® Simulink® environment. Control is implemented in the form of a code using MATLAB function block, executed at a sampling time of $25e^{-6}$. The system components (inverter, load) are simulated at a sampling frequency of $1e^{-6}$ depicting behavior of a continuous time system. Inverter DC-link voltage V_{dc} = 530 V and load parameters L = 5.974 mH, R = 6.25 Ω are considered for simulation. For benchmarking purpose, results for

conventional FCS-MPCC with step change in reference current amplitude from 21.21 A (3000 VA) to 11.21 A (1600 VA) at time t = 1 seconds is shown in Figure 3.7.

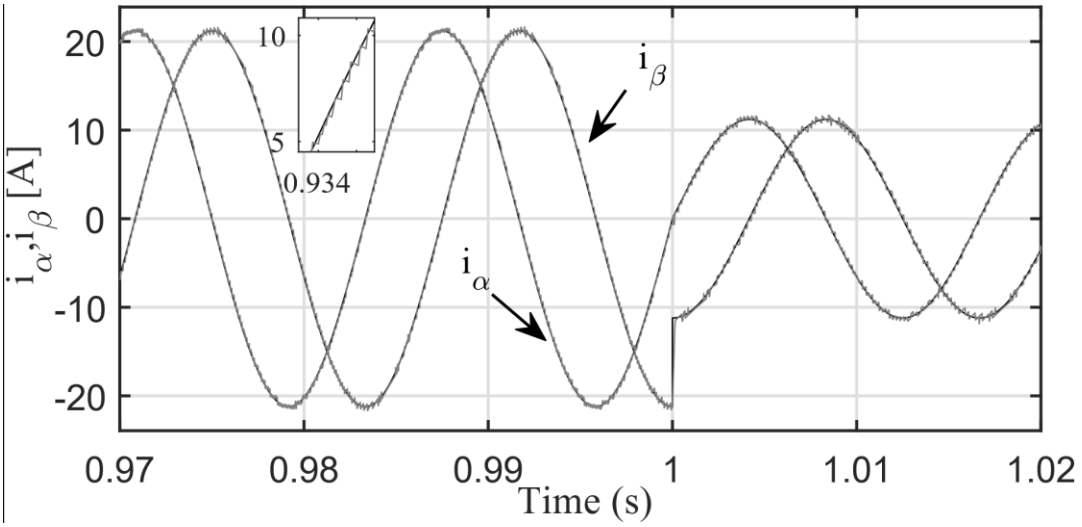

Figure 3.7 Currents with conventional FCS-MPCC Scheme

The currents shown in simulation results are the three-phase currents projected in two dimensional α-β plane. Stepped change in reference causes stepped change in β - component presenting high dynamic performance of the control method. Inverter currents follow reference currents through optimal switching of power semiconductor devices which can be seen by the zoomed section. During normal operating conditions the DC-link capacitor voltages are expected to be balanced. Balanced voltage in DC-link capacitors is achieved by proper adjustment of weight λ_{dc} and keeping the voltage difference reference $v_\Delta{}^*$ to be zero which can be observed in Figure 3.8.

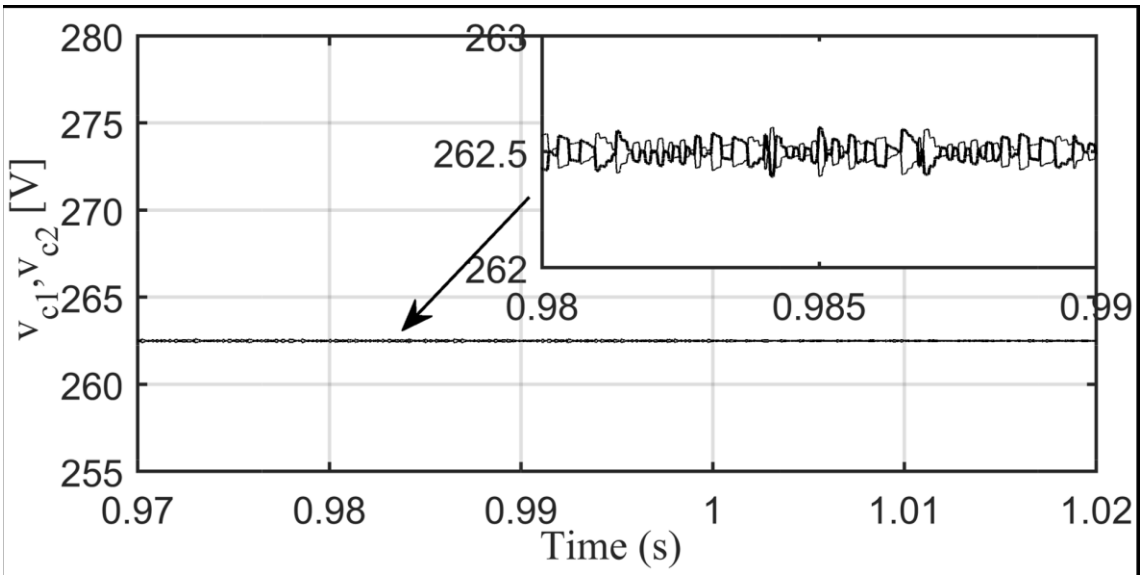

Figure 3.8 Capacitor voltage control with FCS-MPCC

To check the feasibility of the presented FCS-MPCC scheme with condition monitoring, predictive control algorithm in MATLAB function block is updated keeping the same simulation parameters. A sinusoidal difference voltage with 25 V peak, and 5 Hz frequency is injected in dynamic model using third term of (3.22) at time t= 1 second.

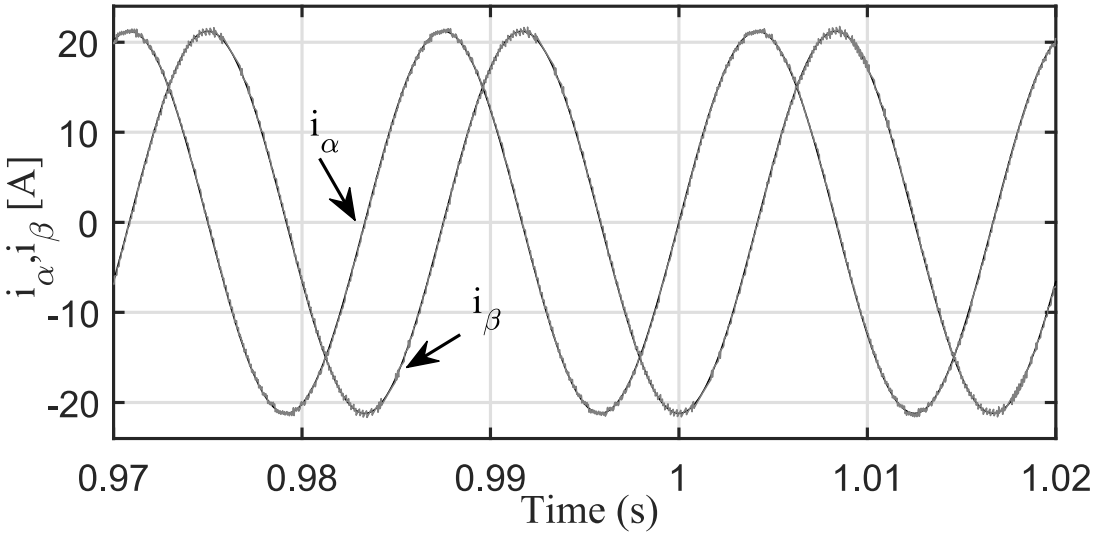

Figure 3.9 Currents before and after difference voltage Injection

Since the predicted currents use voltage vectors derived from the instantaneous capacitor voltages (ref Table 3.2), current control automatically accounts for the capacitor voltages being different from one another which can be observed from Figure 3.9.

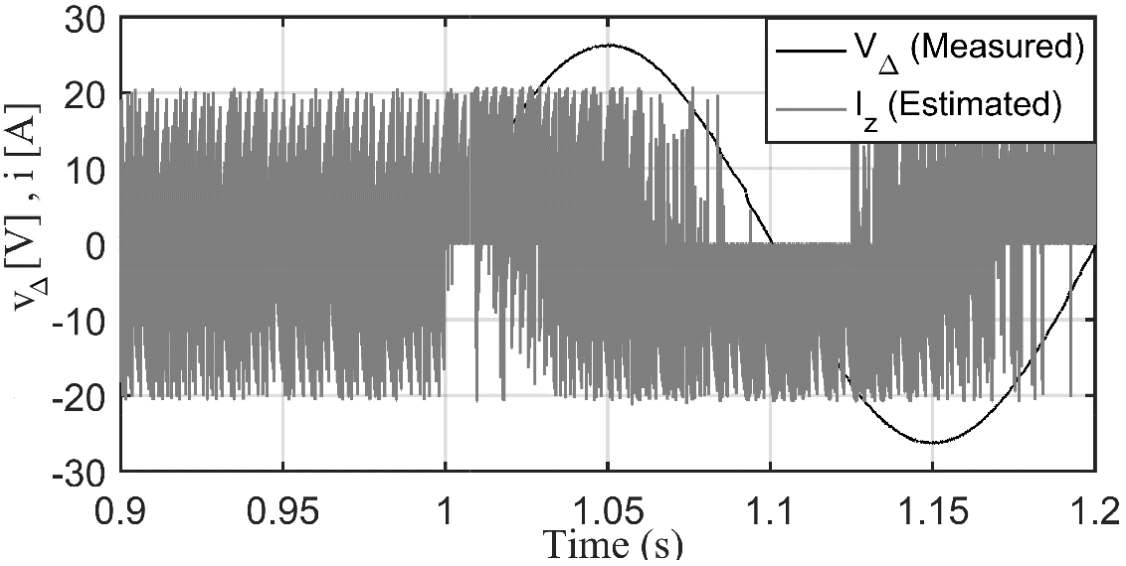

Figure 3.10 Injected difference voltage and estimated neutral point current

Control scheme forces the capacitor voltages to follow the reference voltage difference (v_{Δ}^{*}) trajectory. The formulated cost function (3.22) forces the capacitor voltages to follow the reference difference voltage trajectory by indirect injection of neutral point current i_z.

To validate (3.35) simulation studies are carried out for difference voltage v_{Δ}^{*} injection at several frequencies. Three frequency ranges were considered, 1) above fundamental frequency (f_{inj} > 60 Hz) 2) at fundamental frequency ($10\,Hz < f_{inj} \leq 60$ Hz) and 3) below minimum operational frequency $f_{inj} \leq$ 5Hz. For injection frequencies above $f_{inj} = 25$ Hz, the control algorithm was not able to track a sinusoidal voltage difference v_{Δ}^{*}. This was primarily due to two different reasons, 1) insufficient margin between converter switching frequency and the injection frequency 2) inability of converter to supply desired neutral point current. For injection frequencies between $10\,Hz < f_{inj} <$ 25 Hz, converter tracked reference difference voltage partially in form of a triangular wave indicating reduced neutral point current requirement. For injection frequencies below minimal operational frequency $f_{inj} \leq$ 5Hz, control algorithm was able to successfully track reference difference voltage indicating neutral point current requirement being matched by converter capacity at said operating point. Figure 3.10 shows the measured difference voltage and estimated neutral point current using (3.7) directly indicating that neutral point current is composed of load currents and their respective phase converter switching state. Low frequency components are extracted using a low pass, 50th order FIR filter with 10 Hz cutoff frequency from both the measured voltage difference and estimated neutral point current which is shown in Figure 3.11. A phase difference of 90^{o} between the filtered components clearly indicates response of capacitive network.

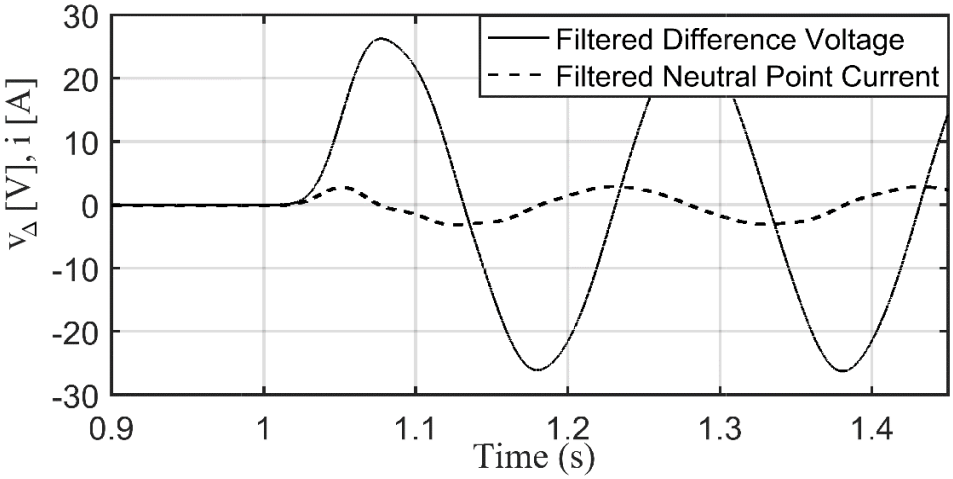

Figure 3.11 Filtered difference voltage and filtered neutral point current

For the simulated system, capacitance for upper capacitor C_1 was set to 2100 µF and lower capacitor was set to C_2 = 1680 µF. With these values, impedance of dynamic neutral point model can be calculated as:

$$Z_{dyn} = \frac{1}{2\pi f_{inj}(C_1 + C_2)} = \frac{1}{2\pi 5(2100 + 1680)10^{-6}} = 8.4208\ \Omega \qquad (3.23)$$

Impedance of dynamic model of neutral point is evaluated as ratio of RMS quantities of filtered voltage difference to filtered neutral point current and shown in Figure 3.11. Calculated values in Figure 3.12 clearly validates the FCS-MPCC with condition monitoring scheme. A decrease in capacitance will be easily observed in the impedance of dynamic model indicating deterioration of DC-link capacitors.

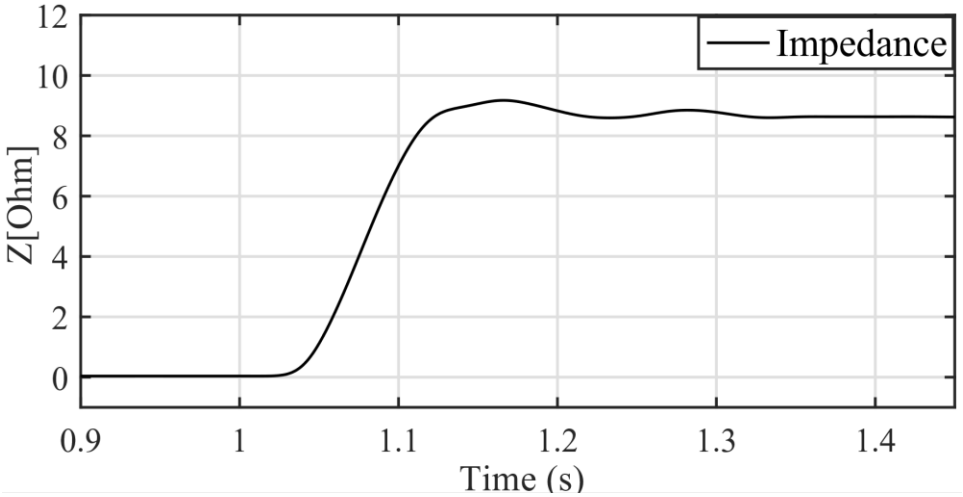

Figure 3.12 Calculated impedance of dynamic model

3.7 Hardware Implementation and Results

The method of condition monitoring embedded with FCS-MPCC scheme presented in previous section is validated by implementing it on a three-level NPC inverter experimental hardware prototype with RL load in this section. Specifications of hardware prototype are listed in Table 3.3

Table 3.3 Hardware specifications of prototype

Inverter Power	3 kVA
DC-link capacitor, C_f	3300 uF
DC-link capacitor, C_{var}	470 uF
DC-link voltage	200 V
Load Resistance	10 Ω
Load Inductance	5 mH

3.7.1 Hardware Implementation

Three phase three level neutral-point clamped inverter is formed using three Infineon manufactured (F3L200R07PE4) neutral point IGBT leg modules shown in Figure 3.13. The gate terminals of the IGBTs are driven using Infineon manufactured (F3L020E07-F-P_EVAL) gate driving circuitry.

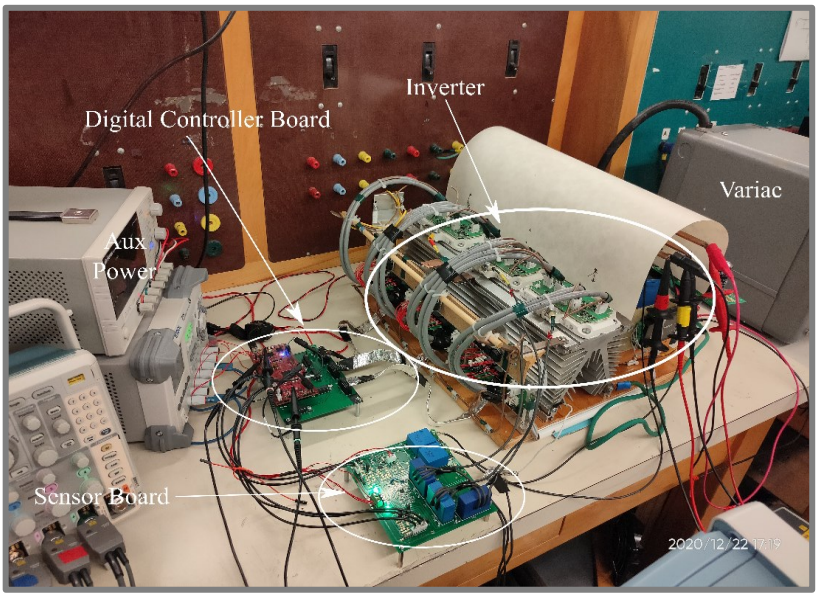

Figure 3.13 3 kVA, three-level NPC inverter hardware prototype

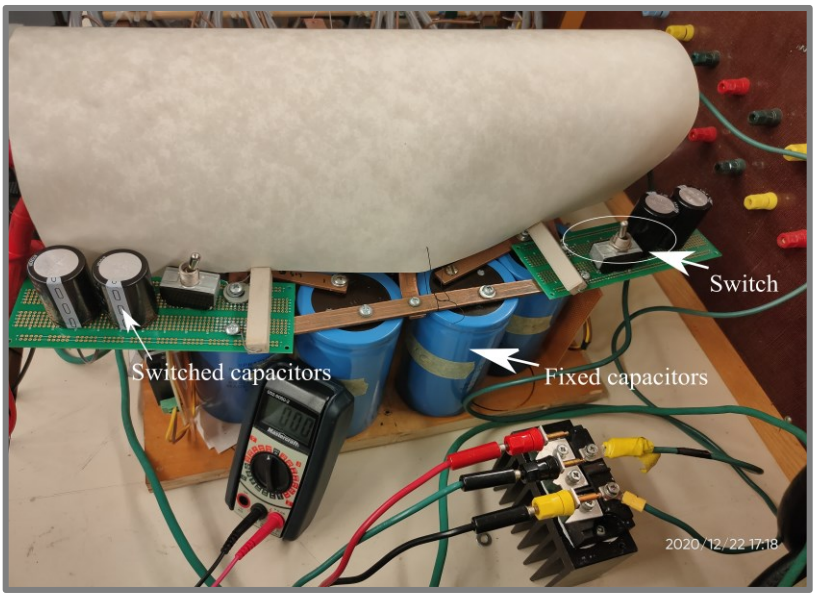

Figure 3.14 Switched DC-link capacitor in hardware prototype

Power in the DC-link is fed by a three-phase diode rectifier connected to three-phase mains through a VARIAC. To account variation of DC-link capacitance occurring due to deterioration of the capacitors, extra capacitors in series with single-pole single-throw switch are connected in parallel with the actual capacitors. The setup to achieve stepped variation of capacitance is shown in Figure 3.14. Block diagram of this experimental setup is shown in Figure 3.15.

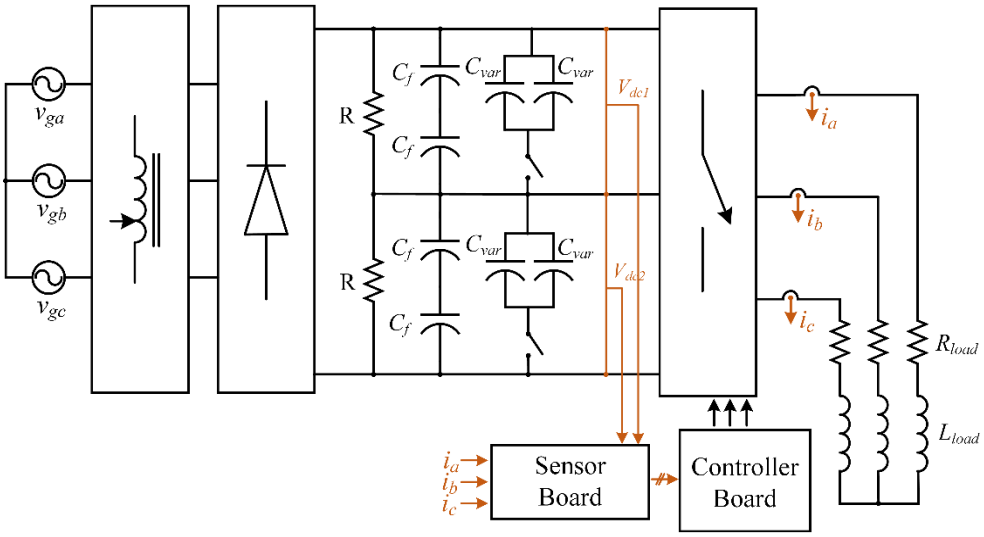

Figure 3.15 Block diagram of hardware implementation with feedbacks

Voltages across individual DC-link capacitors (upper and lower) are sensed using Hall-effect voltage sensors (LV 25-P). Load currents are measured using current transducer (LA 55-P). Sensed quantities are conditioned using OPAMP circuits and fed to the analogue to digital (ADC) channels of Digital Signal Processor. Controller board implements control algorithm digitally and feeds PWM signals to the converter circuit through gate driver board to achieve desired control.

FCS-MPCC with condition monitoring requires a digital signal processing platform to perform several time critical operations within a single sampling period duration which include:

- Predictive control algorithm.
- Impedance extraction algorithm.

Predictive control algorithm essentially requires iterative prediction of load current trajectory. Number of iterations depends upon the possible switching states of the converter to be controlled. Multilevel converters generally have larger number of switching states increasing the computational burden. Apart from this, simple filtering operation and RMS calculation of the quantities require extensive memory and computational power. The total time required for the

controller to perform calculations considering both the operations had to be lower than the available sampling period duration. To work around this problem, a dual core digital signal processor TMS320F28379D is used.

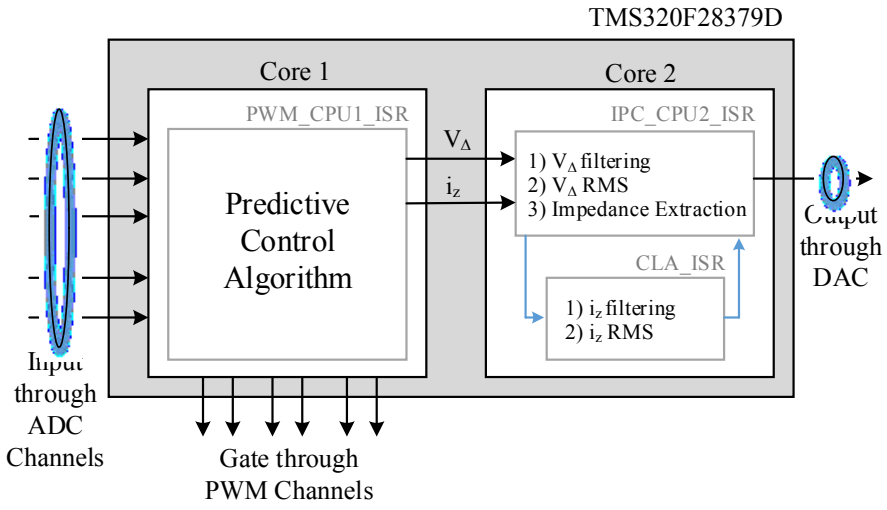

Figure 3.16 Algorithm implemented in Digital Signal Processor

Two operations are split among two CPU cores ensuring completion of calculations within the PWM sample time, which is shown graphically in Figure 3.16. Predictive control algorithm was executed in an Interrupt Service Routine (ISR) triggered by PWM timer operated to count for 200 μs in core -1. For every sampling period duration, i_z was estimated using (3.7) V_Δ was calculated using sensed capacitor voltages and fed to core-2 using Inter Processor Communication (IPC) message ram. Low pass filtering and RMS calculation was executed in ISR triggered by IPC channel. Independent operations on i_z and V_Δ were calculated in parallel using CPU-2 and control logic accelerator (CLA) associated with it. Evaluated impedance from these quantities are fed out of controller using a digital to analogue converter (DAC) after appropriate scaling.

3.7.2 Experimental Results

To validate the concept of condition monitoring along with FCS MPCC, DC-link capacitance C_1 and C_2 were set to 2550 uF each using the switch. The converter was operated with a fixed load current reference of 9A peak, 60 Hz. Initially, the voltage difference between two capacitors was set to 0V. Using watch window of Code Composer Studio Integrated development environment, voltage difference injection variable was enabled to inject a difference voltage of 20 V peak at 5 Hz frequency. Choice of injection frequency was based on neutral point current limits stated in

section 3.5 Figure 3.17 presents single-shot capture of results using Yokogawa DLM2024. Channel 3 presents GPIO bit coming from the digital signal controller indicating enabling of voltage injection. Channel 1 and 2 presents capacitor voltages which are controlled as per the requirement of operation. Enabling and injecting voltage difference causes sinusoidal variation in capacitor voltages with a phase difference of 180 degrees. Mathematical operator is used to represent the actual voltage difference that is injected in the dynamic model. Since calculated impedance is scaled and fed through DAC of processor, Channel 4 represents calculated impedance of dynamic model which comes out to be an analogue value equivalent to 6.3971 ohms that corresponds to 4980 uF of total capacitance in the dynamic model.

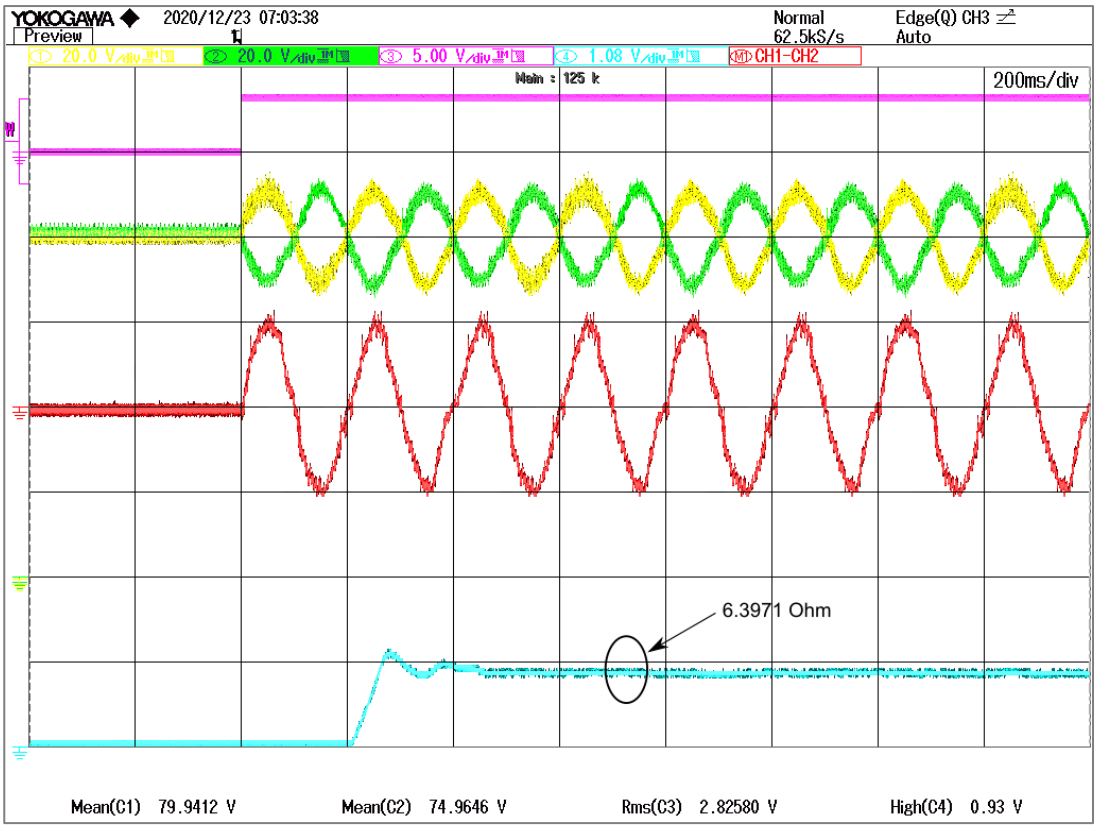

Figure 3.17 Impedance extraction at 5100 uF capacitance of dynamic model

Deterioration in capacitance is implemented in hardware by disconnecting the variable capacitors. Once again the converter is operated at the same operating point and a voltage difference is injected in the dynamic model, which is shown in Figure 3.18. Obtained analogue value from DAC is equivalent to 10.0097 ohms which corresponds to 3180 uF total capacitance in dynamic model. Reduction in DC-link capacitance causes increase in dynamic model impedance. This validates prediction of capacitance deterioration using signal injection.

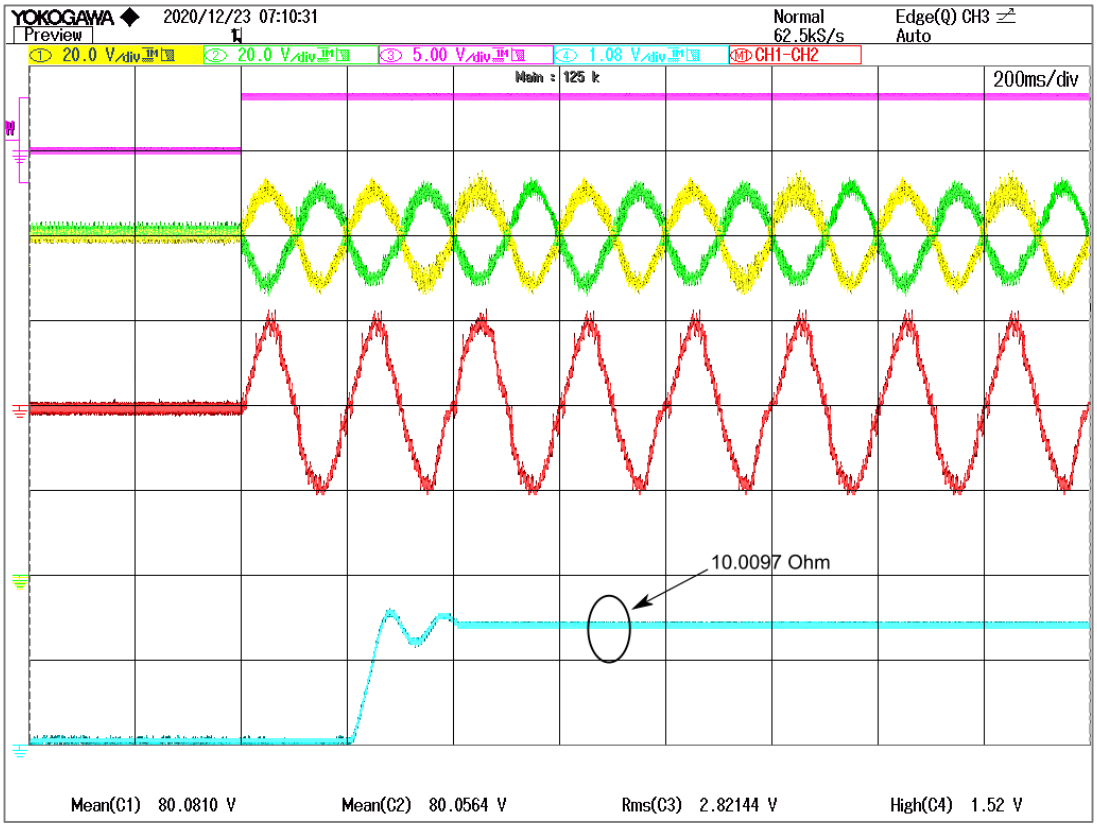

Figure 3.18 Impedance extraction at 3300 uF capacitance of dynamic model

During normal mode of operation, the highest priority in the cost function (3.22) is given to control the currents. However, due to requirement of sinusoidal voltage difference control of the capacitors during condition monitoring, priority is transferred temporarily to control DC-link capacitor voltages. This causes increase in load current distortion. Condition monitoring period is for negligible duration in comparison to the normal operational period. Hence, this deterioration is acceptable. One such case of currents through the load during condition monitoring phase is shown in Figure 3.19.

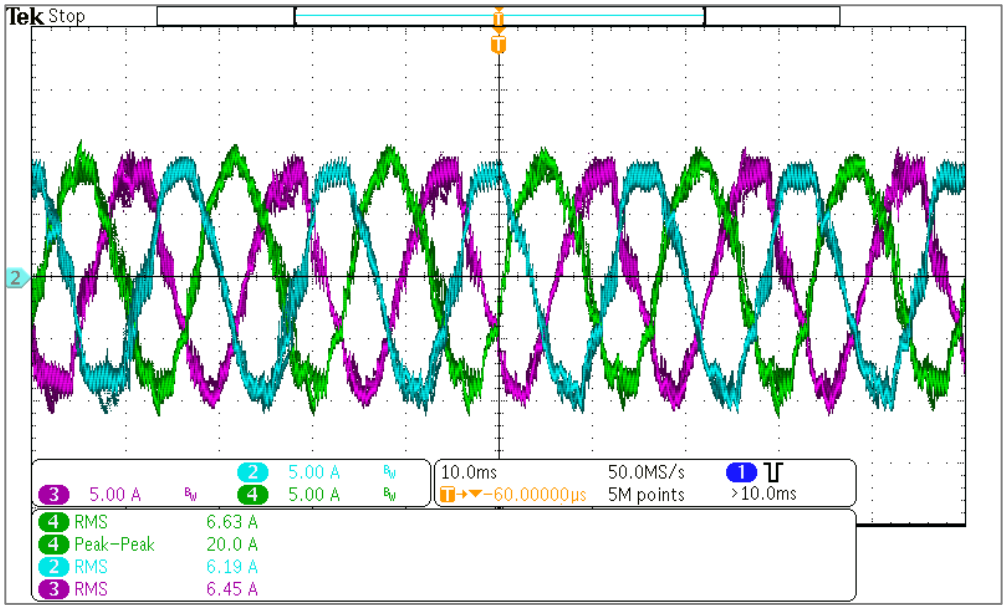

Figure 3.19 Load Current during condition monitoring

Whenever capacitor voltage difference tend to move very far away from the reference, the control algorithm applies voltage vectors which are less optimal but controls the capacitor voltage difference as desired in the reference this causes extensive control action by compromising on device switching losses and current control. Extensive control action near zero current crossing instants is due to increased capacitor voltage control priority during condition monitoring phase this can be observed by frequent change in its trajectory in Figure 3.20.

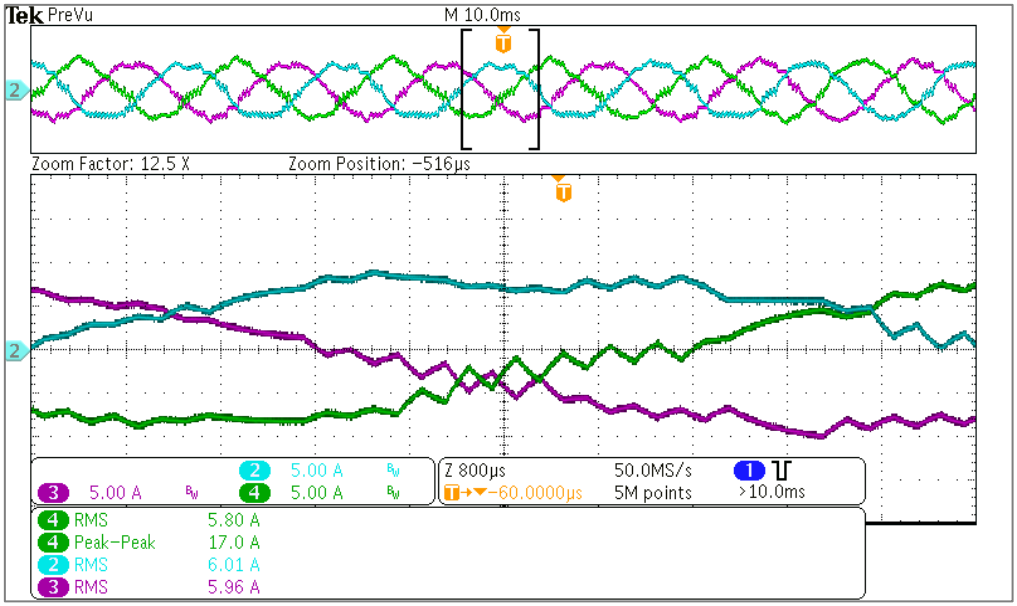

Figure 3.20 Extensive control action leading to increased switching

3.8 Conclusion

A condition monitoring method that gets embedded with finite control set model predictive current control of a three-level neutral point clamped multi-level inverter is proposed in this Chapter. The embedded condition monitoring method uses the concept of dynamic neutral point model. Dynamic neutral point model is obtained from dynamic behavior of neutral point of a three-level NPC inverter. The simulation results from MATLAB Simulink environment, and the experimental results from a 3 kVA experimental hardware prototype confirm the validity of dynamic model and the condition monitoring scheme. The neutral point model is subjected to injection of 20V sinusoidal voltage at 5 Hz frequency through cost function. Impedance for two different capacitance values is calculated online in the hardware. Information about reduction in capacitance due to deterioration of DC-link capacitors is be obtained using this method which is useful for improving reliability in terms of preventive maintenance of the converter.

Apart from online condition monitoring, proper design of the capacitor bank employed in a multi-level converter is an important aspect in terms of operational life cycle of a multi-level converter. Derivation of analytical expression which can be used as a ready tool for proper sizing of capacitor bank in five-level active neutral point clamped converter topology is explained in next Chapter.

CHAPTER 4: ANALYTICAL EVALUATION OF CAPACITOR CURRENT STRESS IN FIVE-LEVEL ACTIVE NEUTRAL POINT CLAMPED CONVERTER

4.1 Introduction

To prevent pre-lifetime deterioration of capacitor bank and hence failure of a multi-level converter, proper sizing of the capacitor bank employed in a multi-level converter configuration is important. This chapter presents analysis and development of the analytical expressions to determine capacitor current stress in a five-level active neutral point clamped converter (5L-ANPC). To facilitate understanding of the derivation process, principal of operation of 5L-ANPC leg is presented in first section. Based on an elementary PWM scheme for 5L-ANPC leg, conduction intervals of power semiconductor switches are expressed mathematically in second section. Using mathematical functions of conduction intervals, closed form of analytical expressions are derived in third section. Derived analytical expressions are validated using simulation models in MATLAB Simulink simulation environment in the last section.

4.2 Principal of Operation

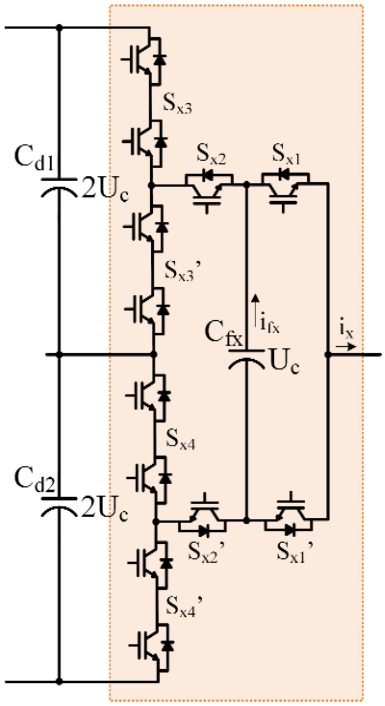

Figure 4.1 Five level Active Neutral Point Clamped Converter leg

Figure 4.1 presents circuit of a 5L-ANPC leg formed as a hybrid combination of three-level NPC and a flying capacitor clamped converter configurations. It is composed of four high-voltage, low-frequency (S_{x3},S_{x4},S_{x3}',S_{x4}') and four low-voltage, high-frequency (S_{x1},S_{x2},S_{x1}',S_{x2}') operated switches with a flying capacitor C_{fx}. where, x represents phase. Assuming DC-link voltage is constant and equal to $4U_c$, nominal voltages of upper, lower DC-link and flying capacitors C_{d1}, C_{d2} and C_{fx} are $2U_c$, $2U_c$ and U_c, respectively. Table 4.1 represents possible switching state combinations and hence generates five distinct pole voltage levels.

Table 4.1 Switching states for 5L-ANPC leg

S_{x4}	S_{x3}	S_{x2}	S_{x1}	V_{xo}	Formed By
1	1	1	1	$2U_c$	V_{cd1}
1	1	1	0	U_c	V_{cd1}- V_{cf}
1	1	0	1	U_c	V_{cf}
1	1	0	0	0	0
0	0	1	1	0	0
0	0	1	0	$-U_c$	$-V_{cf}$
0	0	0	1	$-U_c$	$-V_{cd2}$+ V_{cf}
0	0	0	0	$-2U_c$	$-V_{cd2}$

4.3 Defining mathematical expressions for conduction intervals.

Since the capacitors are charged and discharged through the switches operating at different switching frequencies, conduction interval of the switches form an important base to derive the mathematical expressions for the currents flowing through capacitors.

4.3.1 Conduction function - Low frequency switch

To define conduction function, let us consider pole voltage of leg to be U_c. Pole voltage level U_c can be obtained by two different switching state combinations as shown in Table 4.1. Pole voltage U_c is formed by the conduction path O - C_{d1} - S_{x3} - S_{x2} - C_{fx} - S_{x1}' - X and O - S_{x4} - S_{x2}' - C_{fx} - S_{x1} - X with current flowing in either of the directions. Though low frequency operated switch S_{x3} is on during positive half of load frequency cycle, it conducts only when pole voltage U_c is formed by path O - C_{d1} - S_{x3} - S_{x2} - C_{fx} - S_{x1}' - X. ie. When the switch S_{x2} conducts. Therefore, conduction function of switch S_{x3} can be defined as follow:

$$G_{x3} = S_{x3} * S_{x2} \tag{4.24}$$

where, S_{xi} represents switching function of i^{th} switch in x^{th} phase.

Likewise, the conduction function for all other low frequency operated switches in a leg is defined as shown in Table 4.2. This conduction function will be used to evaluate current stress over DC-link capacitor in next section.

Table 4.2 Conduction function for low frequency operated switches

Modulation Region	G_{x3}	G'_{x3}	G_{x4}	G'_{x4}
$1.0 \geq v_{ref\_x} \geq 0$	v_{ref_x}	0	$1 - v_{ref\_x}$	0
$0 \geq v_{ref\_x} \geq -1.0$	0	$\lvert v_{ref\_x} \rvert$	0	$1 - \lvert v_{ref\_x} \rvert$

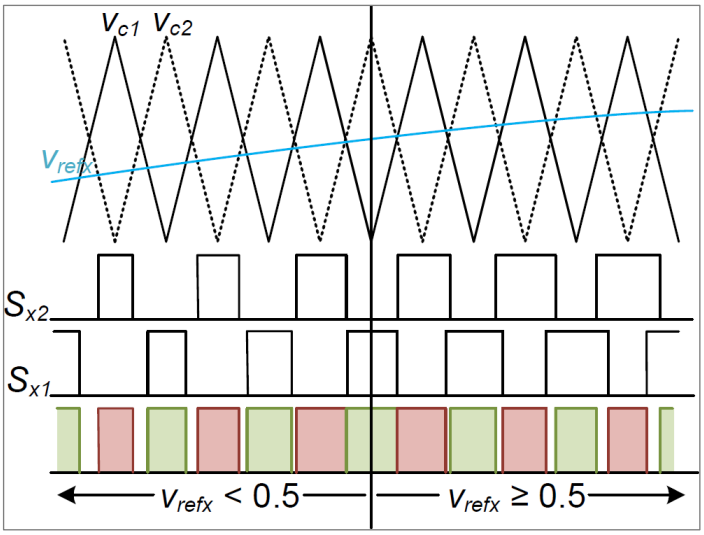

Figure 4.2 Relation of flying capacitor conduction function with switching function

4.3.2 Conduction function - High frequency switch

Since, the flying capacitor C_{fx} in 5L-ANPC phase leg is positioned between S_{x2}, S_{x1} and their complementary switches as shown in Figure 4.1, the conduction intervals of the flying capacitor depends upon the relationship between conduction intervals of switches S_{x2} and S_{x1}. Analysis is done using carrier shifted modulation technique stated in [43] as it is generic and has inherit flying capacitor voltage balancing. Figure 4.2 presents the relation between the conduction intervals of the switches S_{x2}, S_{x1} and its implication over conduction interval of the flying capacitor considering the above stated modulation technique. When reference signal magnitude is below half of the peak carrier amplitude, the capacitor conducts when either of the switches S_{x1}, S_{x2} are conducting. And when reference signal magnitude is above half of the peak carrier amplitude, capacitor conducts

over non-overlapping conduction intervals of the switches S_{x1}, S_{x2}. Thus, conduction function for the flying capacitor can be expressed as:

$$G_{fx} = S_{x2} \oplus S_{x1} \tag{4.25}$$

Function is further simplified and two separate mathematical representations of the flying capacitor conduction function are obtained as stated in Table 4.3. This function will be used as a base to evaluate current stress over flying capacitor in further section.

Table 4.3 Conduction function for flying capacitor

Modulation Region	G_{fx}
$1.0 \geq \lvert v_{refx} \rvert \geq 0.5$	$2(\lvert v_{refx} \rvert)$
$0.5 \geq \lvert v_{refx} \rvert \geq 0.0$	$2(1 - \lvert v_{refx} \rvert)$

4.4 Analytical expressions for capacitor current stresses.

Each 5L-ANPC leg has one flying capacitor. Current stress over this capacitor is dependent on the load current of respective leg. Hence, expression for flying capacitor current stress will be evaluated first. Then closed-form expressions for DC-link capacitor current stress in single-phase half-bridge, single-phase full-bridge and three-phase configuration shown in Figure 4.3 will be evaluated. Sinusoidal reference modulating signal is considered.

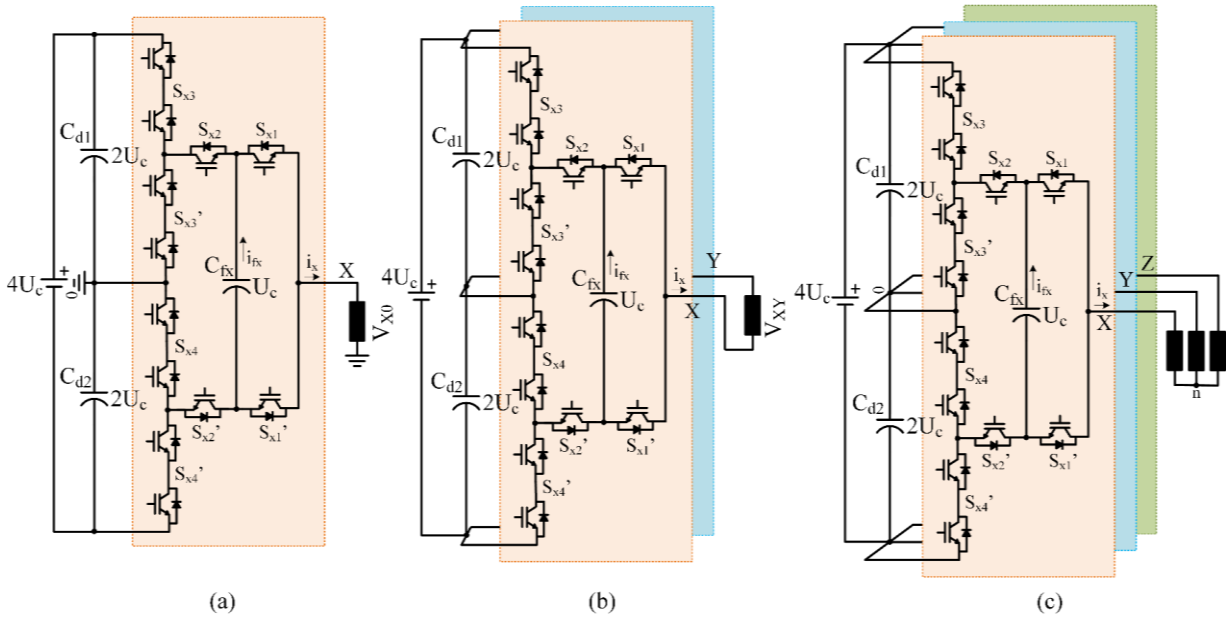

Figure 4.3 5L-ANPC converter configurations

4.4.1 Flying capacitor current stress

Instantaneous flying capacitor current (i_{cfx}) can be written as the product of the previously defined conduction function (4.25) and respective pole current (i_x) as:

$$i_{cfx} = G_{fx} i_x \tag{4.26}$$

$$v_{refx} = m \sin\omega t \tag{4.27}$$

For simplicity, the pole current harmonics are ignored. The pole current i_x for a 5L-ANPC leg modulated with reference signal stated in (4.27) and fundamental power factor angle being ϕ is defined as:

$$i_x = I_m \sin(\omega t - \phi) \tag{4.28}$$

Expression for the flying capacitor RMS current over fundamental-cycle can be written as:

$$I_{cfx} = \sqrt{\frac{1}{\pi}\int_0^{\pi} G_{fx}\, i_x^2 \, d\omega t} \tag{4.29}$$

Based on (4.26), (4.27), (4.28) and Table 4.3, (4.29) can be simplified to obtained closed form as;

$$I_{c\_cfx} = \begin{cases} \dfrac{mI_m^2}{\pi}\left[\dfrac{6 + 2\cos 2\phi}{3}\right] & m < 0.5 \\ \dfrac{I_m^2}{\pi}\left[\begin{array}{c} 2m + \pi - 4m\cos\omega t_1 - 2\,\omega t_1 \\ + \cos 2\phi \left(\dfrac{2 + 3\sin 2\omega t_1}{3}\right) \\ + \cos 2\phi\ (1+m)\left(\dfrac{\cos 3\omega t_1 - 3\sin\omega t_1}{3}\right) \end{array}\right] & m \geq 0.5 \\ where,\ \ \omega t_1 = \sin^{-1}\left({}^{1}/_{2m}\right) & \end{cases} \tag{4.30}$$

4.4.2 DC-Link Capacitor current stress

In a single 5L-ANPC leg shown in Figure 4.3(a), load current flows through DC-link only when the switch S_{a3} conducts. Therefore, instantaneous DC-link current ($i_{i\text{-}hb}$) can be written as the product of the switch S_{a3} conduction function (4.24) and load current (i_a) as:

$$i_{i-hb} = G_{a3} i_a \tag{4.31}$$

Considering the same assumptions from previous derivation, average DC-link current stress over fundamental cycle can be evaluated as:

$$I_{avg-hb} = \frac{1}{2\pi}\int_0^{2\pi} G_{a3} i_a \, d\omega t = \frac{mI_m}{4}\cos(\phi) \tag{4.32}$$

Similarly, DC-link RMS current can be expressed as:

$$I_{rms-hb}^2 = \frac{1}{2\pi}\int_0^{2\pi} G_{a3} i_a^2 \, d\omega t = \frac{mI_m^2}{2\pi}\left(\frac{3 + \cos(2\phi)}{3}\right) \tag{4.33}$$

DC-link capacitor RMS current ($I_{c\text{-}hb}$) can be obtained from derived expressions of DC-link average and RMS currents.

$$I_{c-hb} = \sqrt{\frac{mI_m^2}{2}\left[\frac{1}{\pi} - \frac{m}{16} + \cos(2\phi)\left(\frac{1}{3\pi} - \frac{m}{16}\right)\right]} \tag{4.34}$$

In a full-bridge configuration shown in Figure 4.3 (b), load currents flows through DC-link in both the half cycles of fundamental frequency. Therefore, the equations derived for half-bridge in (4.32), (4.33) and (4.34) can be easily extended for the full-bridge configuration as:

$$\begin{aligned} I_{avg-fb} &= \frac{mI_m}{2}\cos(\phi) \\ I_{rms-hb}^2 &= \frac{mI_m^2}{\pi}\left(\frac{3 + \cos(2\phi)}{3}\right) \\ I_{c-fb} &= mI_m^2\sqrt{\left[\frac{1}{\pi} - \frac{m}{8} + \cos(2\phi)\left(\frac{1}{3\pi} - \frac{m}{8}\right)\right]} \end{aligned} \tag{4.35}$$

Assuming modulation signals in three phase configuration being phase shifted by $2\pi/3$ radians and the respective load currents being harmonic free, expression for instantaneous DC-link current can be written as:

$$i_{i-3\phi} = G_{a3} i_a + G_{b3} i_b + G_{c3} i_c \tag{4.36}$$

Using (4.36), assuming three-phase conduction functions and currents being symmetric over fundamental cycle, average DC-link current ($I_{avg\text{-}3\phi}$) can be obtained as:

$$\begin{aligned} I_{avg-3\phi} &= \frac{1}{2\pi}\int_0^{2\pi} (G_{a3} i_a + G_{b3} i_b + G_{c3} i_c) \, d\omega t \\ &= \frac{3}{2\pi}\left(\int_0^{\frac{2\pi}{3}} G_{a3} i_a d\omega t + \int_0^{\frac{\pi}{3}} G_{c3} i_c d\omega t\right) \\ &= \frac{3mI_m}{4}\cos(\phi) \end{aligned} \tag{4.37}$$

The RMS DC-link current ($I_{rms\text{-}3\phi}$) in three-phase configuration can be expressed as:

$$I_{rms-3\phi} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (G_{a3}i_a + G_{b3}i_b + G_{c3}i_c)^2 \, d\omega t} \tag{4.38}$$

Owing to the symmetry of three-phase system, (4.38) can be reduced to:

$$I^2_{rms-3\phi} = \frac{3}{2\pi}\left(\int_0^{\pi} G_{a3}i_a^2 \, d\omega t + 2\int_0^{\frac{\pi}{3}} G_{a3}G_{c3}i_a i_c \, d\omega t\right) \tag{4.39}$$

It can be observed in (4.39) that RMS DC-link current expression for three-phase configuration has two components. First component presents the current due to operation of single phase leg and the other represents current during overlapping interval of two phase legs. To simplify the integration process of second component, conduction functions for each overlapping phase leg over the integrating interval are referred in Figure 4.4. The second component is formed as a product of two phase leg conduction functions and resulting product is equal to the conduction function having lowest interval. This results in $G_{a3} * G_{c3} = G_{a3}$ over the interval $[0, \pi/6]$ and $G_{a3} * G_{c3} = G_{c3}$ over the interval $[\pi/6, \pi/3]$ which can be observed in Figure 4.4.

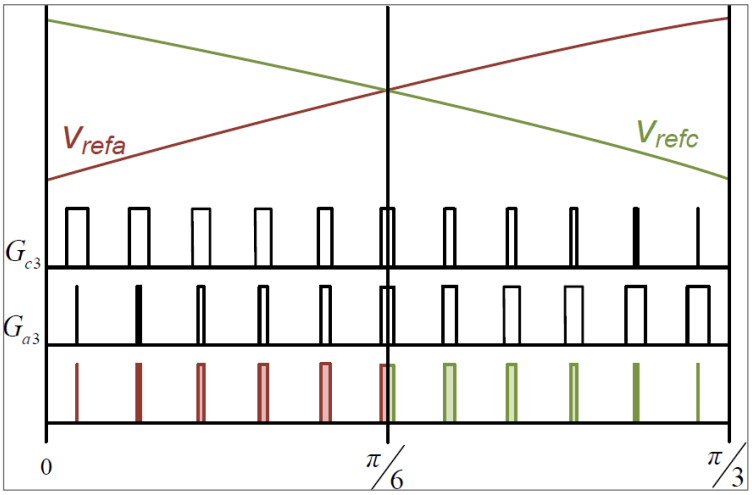

Figure 4.4 Reference overlapping interval

Thus, (4.39) can be simplified as:

$$I^2_{rms-3\phi} = \frac{3}{2\pi}\left(\int_0^{\pi} G_{a3}i_a^2 \, d\omega t + 2\int_0^{\frac{\pi}{6}} G_{a3}i_a i_c \, d\omega t + 2\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} G_{c3}i_a i_c \, d\omega t\right) \tag{4.40}$$

Integrals in (4.40) are evaluated to obtain closed form of RMS DC-link current ($I_{rms-3\phi}$) as:

$$I^2_{rms-3\phi} = \frac{\sqrt{3}I_m^2 m(3 + 2\cos(2\phi))}{4\pi} \tag{4.41}$$

Finally, DC-Link capacitor RMS current ($I_{c\text{-}3\phi}$) can be obtained as:

$$I_{c-3\phi} = \sqrt{\frac{mI_m^2\sqrt{3}}{4}\left[\frac{3}{\pi} - \frac{3\sqrt{3}m}{8} + \frac{\cos(2\phi)}{8}\left(\frac{16}{\pi} - 3\sqrt{3}m\right)\right]} \tag{4.42}$$

4.5 Comparison of results with simulation

In order to validate the analytical equations derived for both the capacitors, 5L-ANPC leg is connected and simulated as single-phase half-bridge, single-phase full-bridge and three-phase configurations shown in Figure 4.3 with discussed modulation technique in MATLAB Simulink environment. Since the currents are assumed harmonic free in the expressions and to simulate various conditions of power factor (cos ϕ), a controlled current source is connected across load side with controlling signal being sinusoidal in nature with a desired shift from modulating signal. Instantaneous currents flowing through the DC-link capacitors and the flying capacitors are sensed using current sensor blocks. Sensed currents are quantified in terms of root mean square (RMS) quantities over one cycle of load frequency (60 Hz). Similarly, the derived expressions are written in form of MATLAB scripts. The scripts are iterated over range of modulation index (m) and power-factor angle (ϕ) and thus obtaining quantitative current stress in the capacitors at various converter operating points. Table 4.4 lists global maximum for capacitor current stresses in various configurations obtained at different combinations of modulation index (m) and power factor angle (ϕ).

Table 4.4 Peak stresses in capacitors at operating conditions

$\left(\frac{I_{c-rms}}{I_{o-rms}}\right)$	C_{fc}	$C_{DC-link-3\phi}$	$C_{DC-link-fb}$	$C_{DC-link-hb}$
0.9307	m = 0.53 ϕ = 0°	-	-	-
0.6497	-	m = 0.61 ϕ = 0°	-	-
0.6515	-	-	m = 1.0 ϕ = 90°	-
0.5472	-	-	-	m = 1.0 ϕ = 0°

$$\%\ error = \frac{1}{I_{C,rms,1,sim}}\left(I_{c,rms,1,eqn} - I_{C,rms,1,sim}\right) \tag{4.43}$$

The relative error in the quantified capacitor current stresses from the derived expressions with respect to the MATLAB simulation stated by (4.20) is plotted for range of operational modulation index at a fixed power factor angle (ϕ) in Figure 4.5. Fixed power factor angles are the ones listed in Table 4.4 where capacitor current stress is maximum. For a flying capacitor connected in each phase leg (Figure 4.1), and DC-link capacitor with 3-phase configuration (Figure 4.3-c) maximum relative error occurs below m = 0.1. However, a power converter used for any application is usually operated above m = 0.2 where the error is limited below 0.16 %. For single phase half-bridge and full-bridge configurations, maximum error occurs at m = 0.25. In either of the cases, relative error is limited below 0.73% which is nominal.

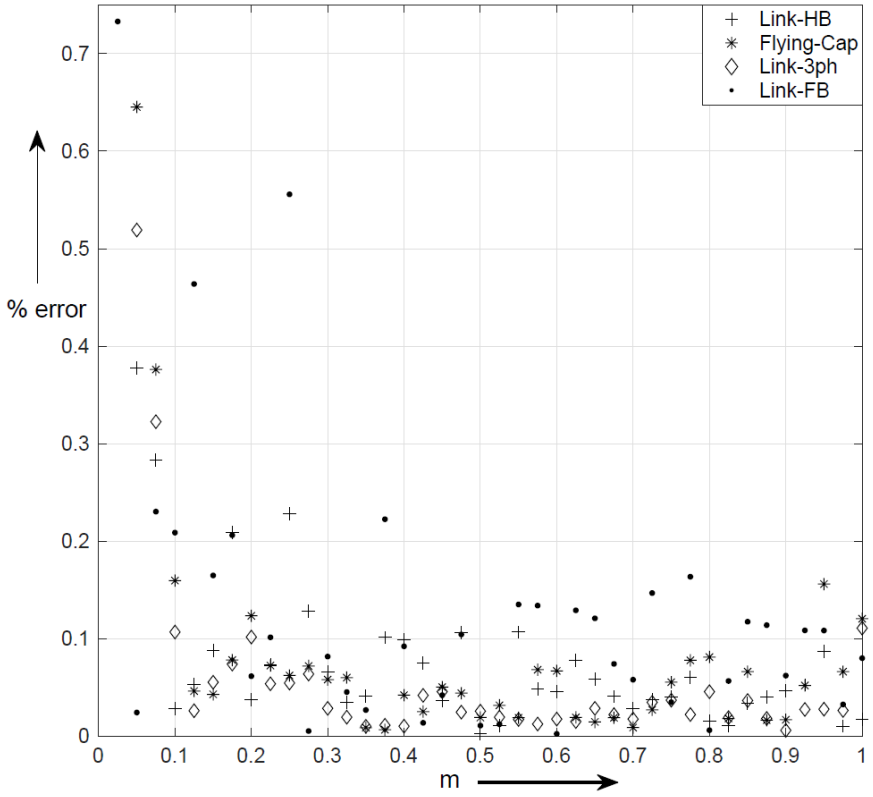

Figure 4.5 Error in analytical expressions (modulation sweep)

Similarly, Figure 4.6 presents relative error in results obtained by analytical equations for a range of power factor angles with fixed modulation index (m). Fixed modulation index are the values listed in Table 4.4 where capacitor current stress is maximum. In either of conditions, errors are limited to 0.73% validating the derived analytical expressions.

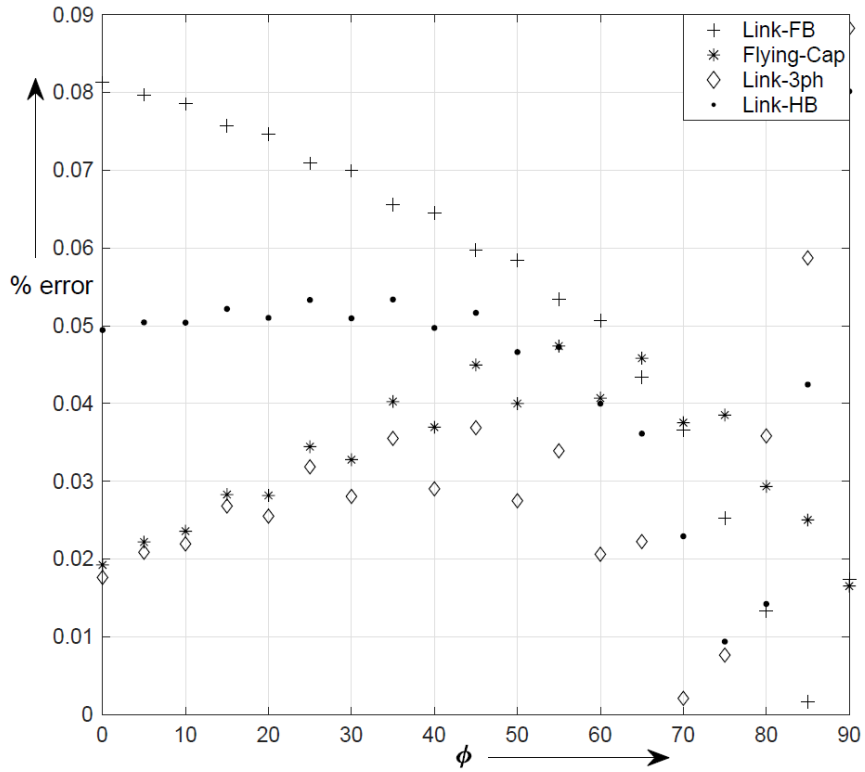

Figure 4.6 Error in analytical expression (power factor angle sweep)

To simplify capacitor bank design process employed in a 5L-ANPC converter by using these derived analytical tools, results obtained from the expressions for all the possible operating conditions in terms of modulation index (m), rated converter output current ($I_{o,rms}$) and power factor angle (ϕ) are plotted and presented in Figure 4.7 (a), (b) and (c). Sizing of capacitor bank for desired current stress involves use of datasheet which specifies maximum permissible current stress $I_{c,rms,dim}$ for a required working life of capacitor. Graphs in Figure 4.7 can be used as a ready tool in designing capacitor banks. For example one wishes to design capacitor bank for a single-phase 2 kW inverter with 200 V DC-link employing a 5L-ANPC leg connected in full bridge configuration to a grid of 120 V 60 Hz. With these specifications, the converter is expected to operate with modulation index ($1.0 \geq m \geq 0.85$), power factor angle ($10 \geq \phi \geq 0$) and load current ($16.6 \geq I_o \geq 0$). When referred to Figure 4.7 (a), maximum per-unit flying capacitor current stress comes out to 0.72. Hence, the flying capacitor bank should be able to handle 0.72*16.6 = 12A current. Similarly when referred to Figure 4.7 (b), maximum per unit DC-link capacitor current stress comes out to 0.6. Hence, DC-link capacitors should be selected that can handle 0.6*16.2 = 9.72A. Graphs in Figure 4.7 can be used to design capacitor banks for said converter configurations in any application.

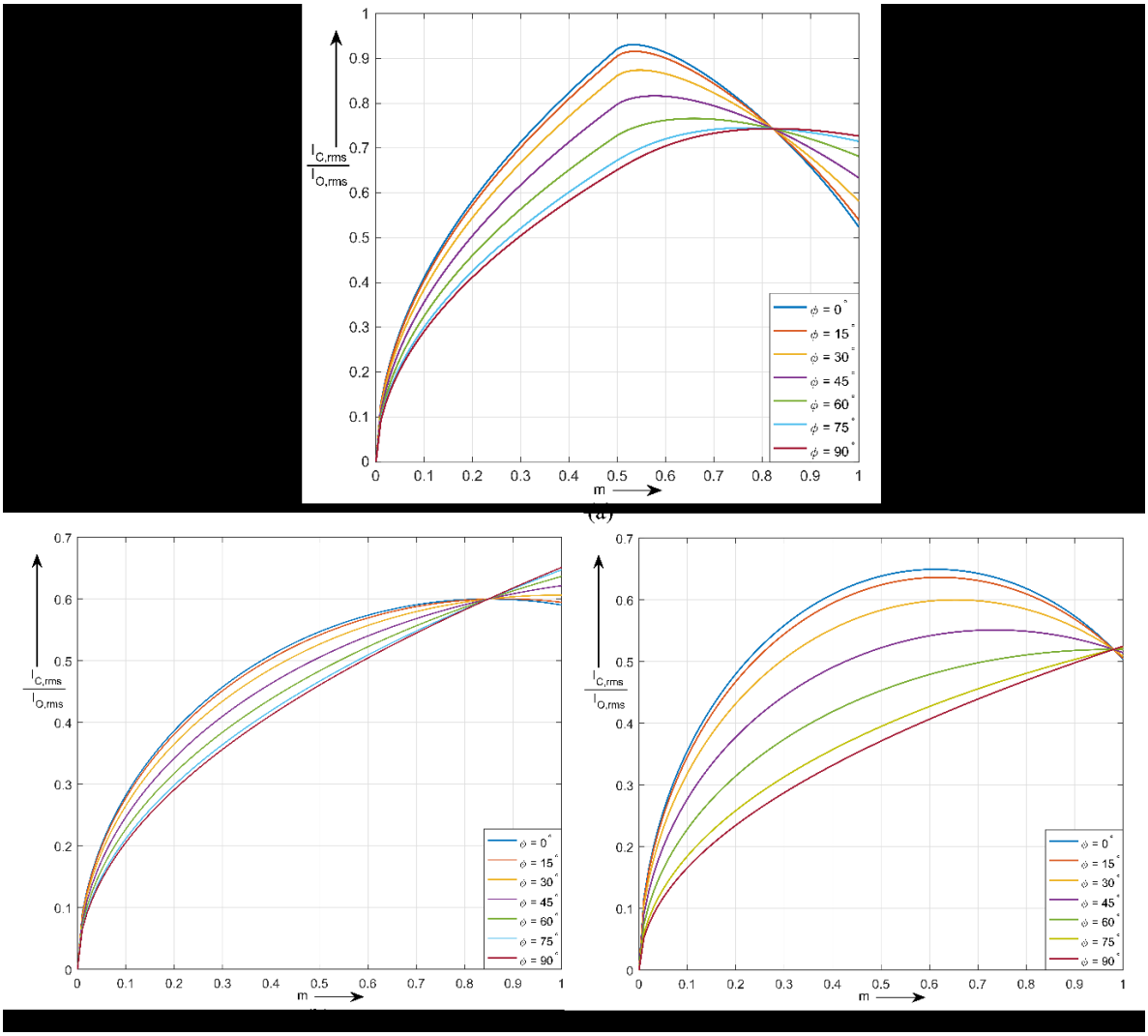

Figure 4.7 Locus of capacitor current stress (a) flying-capacitor (b) DC-link capacitor in 1-phase full-bridge configuration and (c) DC-link capacitor in 3-phase configuration

4.6 Conclusion

An analytical tool in form of closed expressions is developed that aids in proper design of capacitor banks employed in a power converter designed using 5L-ANPC leg. To derive the expressions, conduction intervals of capacitors are defined as functions using switching functions. Quantitative results from the expressions are compared with converter models developed in MATLAB Simulink simulation environment. For every possible operating point of the said converter configurations, maximum relative error is limited to 0.73% validating the expressions and its accuracy. Capacitor bank design process by using resulting graphs as ready reckoner tool is explained. This analytical tool design method can be extended to any multi-level converter.

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

This Chapter discusses the research contributions of this thesis in section 5.1 and provides guidelines for the future research based on findings in section 5.2.

5.1 Contributions of Thesis

Multilevel converters are an important power electronics based power conversion technology that finds applications in process industry, power transmission products, renewable energy integration, traction motor drives, FACTS, etc. It is often desired that such systems should be simple, efficient, high power dense, EMI/EMC complaint, should have high dynamic performance and often reliable over their operational life cycle. Multilevel converters produce stepped (staircase) voltage waveforms by connecting/disconnecting power semiconductor switches and the capacitor banks. Capacitor banks often use high-density aluminum electrolytic capacitors. Aluminum electrolytic capacitors tend to fail during operational life due to vaporization of electrolyte. Use of multiple capacitors adds to reliability concern of multilevel converters. This thesis focuses on the improving reliability of the multi-level inverter in terms of two different ways: (1) develop an online condition monitoring technique, which can be adopted in an existing control method enhancing the reliability by preventive maintenance and (2) develop an analytical tool for proper design of multi-level inverter in terms of sizing the capacitors that are outlined in the following sub-sections.

- Finite control set MPCC of three-level NPC converter with conditioning monitoring of DC-link capacitors

The first contribution, presented in Chapter 3, is proposal of a condition monitoring technique which can be integrated in existing control loop of a three-level NPC converter. This condition monitoring technique injects a sinusoidal very low frequency voltage difference across the voltages of the two capacitors used in three-level NPC converter forming the DC-link and hence evaluates the total capacitance. Voltage injection is achieved using existing power converter control scheme. The concept is validated over a 3kVA three-level NPC inverter experimental prototype operated with FCS-MPCC by online identification of DC-link capacitance. To implement this technique, constraints for current control and number of commutations are relaxed, resulting in an increase in converter switching frequency and deterioration of load current. Since

the duration of voltage injection for condition monitoring is very short, deterioration of performance over small interval has negligible effect over system. Timely online identification of DC-link capacitance will give vital information about capacitance degradation and hence reliability can be improved by preventive maintenance.

- Analytical evaluation of capacitor current stress in five-level active neutral point clamped converter.

The second contribution, presented in Chapter 4, is the development of analytical equations that can be directly used to evaluate the current stresses in the capacitors employed in a five-level ANPC converter leg for single-phase half bridge, single-phase full bridge and three-phase configurations. To derive closed expressions, conduction interval of capacitors in terms of switching intervals are identified and defined in terms of mathematical expressions. Current stresses on the capacitors measured by simulating the converter for said configurations and operating points in MATLAB Simulink environment are compared with the results obtained from derived analytical expressions. Maximum error in results between the two methods for all operating conditions is limited to 0.73% validating the expressions. These expressions can be used as a ready tool to calculate current stresses in capacitors and size them appropriately during converter design stage. The same methodology can be extended for other multi-level converter topologies.

Based on the research work presented in this thesis, recommendations for the potential future work include the following:

5.2 Scope of Future Work

5.2.1 Switching State Grouped Finite Control Set MPCC of multi-level converters with Condition Monitoring of DC-link Capacitors.

Online condition monitoring technique incorporated in FCS-MPCC scheme for the three-level diode clamped converter presented in Chapter 3 involves the prediction of variables for all possible switching state combinations, which is suitable for a digital controller having higher computational capability. However, in order to implement the same control scheme using a digital controller with lesser computational capability, switching state grouped FCS-MPCC with condition monitoring scheme can be used. A switching state grouped FCS-MPCC uses known information about

behavior of a particular switching state combination of a given multi-level inverter for a given load current on the DC-link capacitor voltage. i.e. weather a particular switching state combination at a particular load current will cause increase or decrease in capacitor voltage. Utility of this information and incorporating it in the control scheme causes reduction in number of control iterations. Flowchart of switching state grouped FCS-MPCC with CM is shown in Figure 5.1. Flowchart for injecting voltage difference between the two DC-link capacitors remains the same as that of the proposed scheme in Chapter 3.

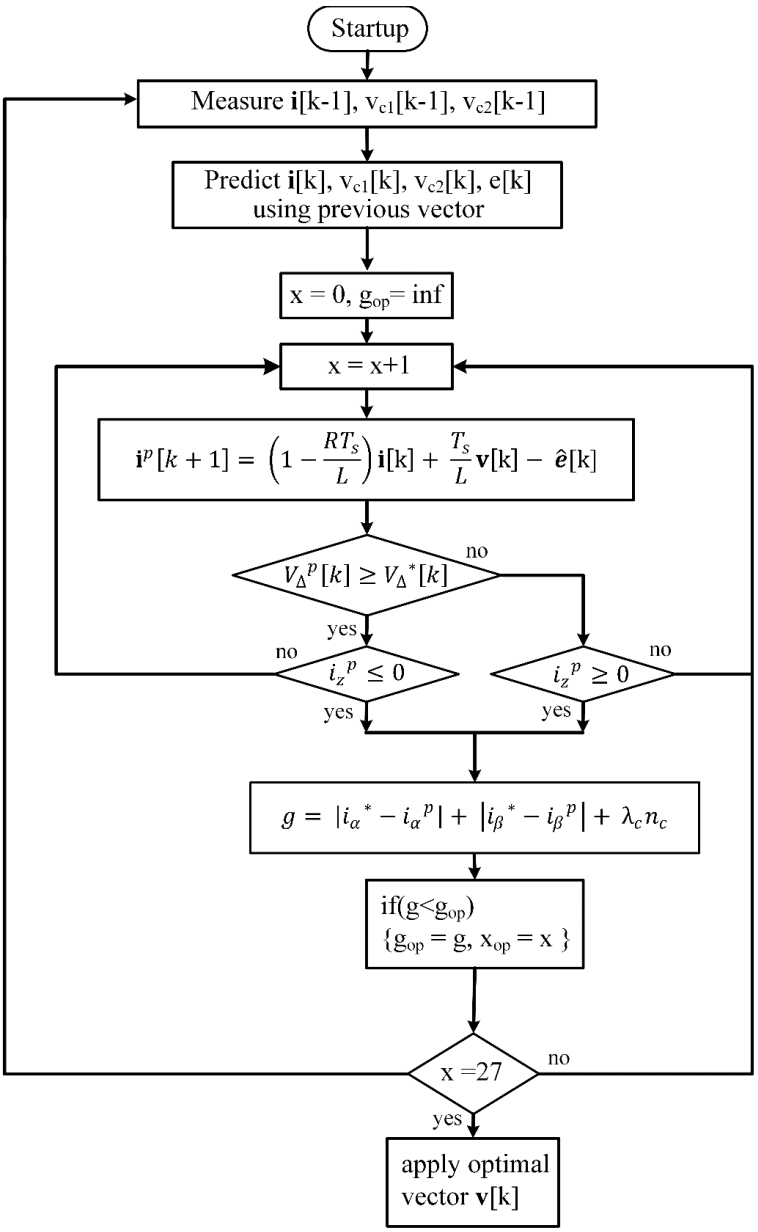

Figure 5.1 Flow chart of switching state grouped FCS-MPCC with condition monitoring

5.2.2 Control of Nested Neutral Point Clamped Converter with Condition Monitoring of DC-link Capacitors.

An advanced multilevel inverter topology, developed using combination of diode-clamped and capacitor-clamped multilevel configuration is shown in Figure 5.2. This converter configuration does not require addition of series connected switches even after scaling operational voltage to higher levels. Due to voltage scalability over wide operational voltage range, recently this converter topology has found a notable attention in academia and industry for high power drives applications [44, 45]. Reliability of this topology is a concern due to higher number of capacitors in a standard three-phase configuration. This topology needs online voltage control loop for the capacitors to overcome limitation of natural voltage control using PWM techniques [47]. Online condition monitoring using forced sinusoidal voltage control discussed in Chapter 3 can easily be implemented for this converter topology with existing online voltage control mechanism. Addition of online condition monitoring scheme will add to reliability of the system using this converter configuration.

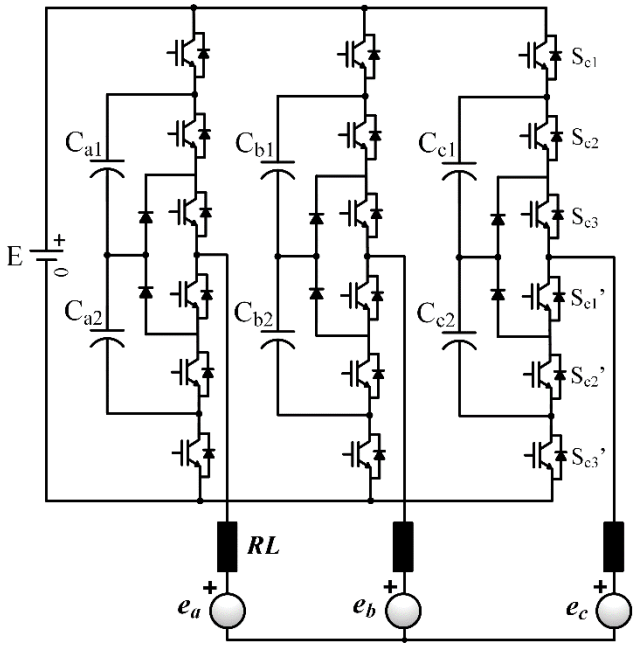

Figure 5.2 Nested neutral point clamped multilevel converter

5.2.3 Finite Control Set Model Predictive Current Control of Modular Multilevel Converter with Condition Monitoring of Sub-Module Capacitors.

Modular multilevel converter shown in Figure 5.3 is one of the most promising topologies for high-power applications with medium to high voltage range. This topology offers merits of modularity, power and voltage scalability, fault tolerance and operation without use of transformers. It has been explored and studied for several applications like HVDC power transmission systems, static synchronous compensators, unified power quality conditioners and medium voltage drives [48]. Though MMC offers numerous advantages, issues like circulating currents, capacitor voltage ripple, DC-bus faults and reliability due to the use of higher number of capacitors are still a concern. Reliability modulation which involves bypassing sub-module with open circuited switch due to bond wire failure is one aspect of improving reliability of the MMC system. However, over operational life cycle of the MMCs, the capacitors deteriorate.

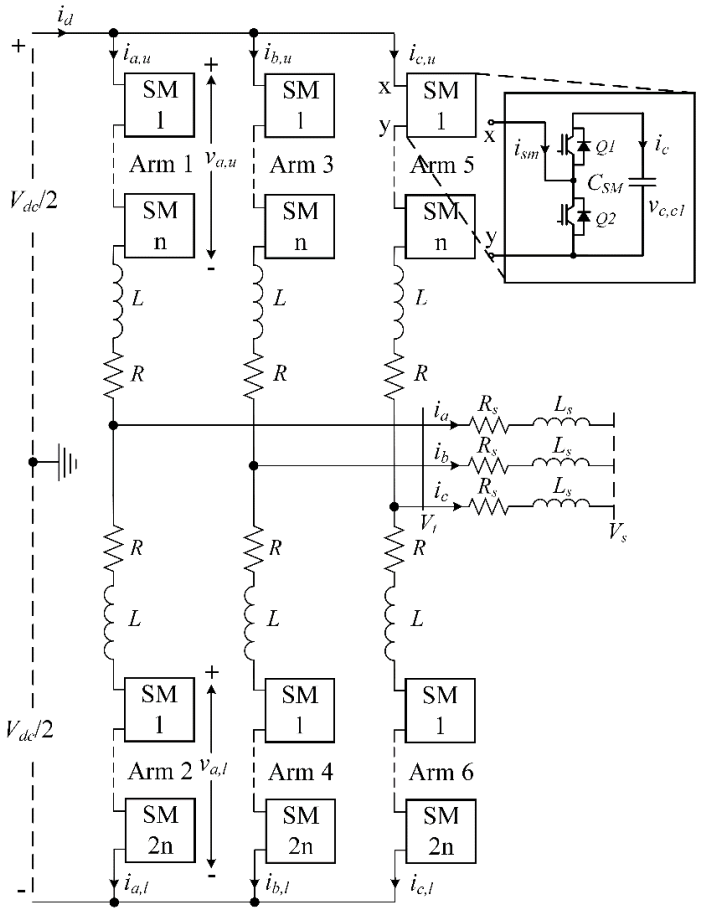

Figure 5.3 Modular multilevel converter topology

Online schemes that can estimate submodule capacitances, incorporated with existing converter control methods can prove beneficial in terms of preventive maintenance and thus improving reliability of the MMC system. Use of high performance control scheme such as MPC is always desirable for high power applications. A generic MPC scheme with condition monitoring of sub-module capacitors can be an important contribution towards improving reliability of the MMC system. This may include forced control of sub-module capacitor voltages at sub-harmonic frequencies or with a combination of multiple frequency components.

REFERENCES:

[1] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, Aug. 2002, doi: 10.1109/TIE.2002.801052.

[2] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," in IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.

[3] A. Edpuganti and A. K. Rathore, "A Survey of Low Switching Frequency Modulation Techniques for Medium-Voltage Multilevel Converters," in IEEE Transactions on Industry Applications, vol. 51, no. 5, pp. 4212-4228, Sept.-Oct. 2015, doi: 10.1109/TIA.2015.2437351.

[4] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," in IEEE Transactions on Industrial Electronics, vol. 49, no. 5, pp. 955-964, Oct. 2002, doi: 10.1109/TIE.2002.803174.

[5] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," in IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2930-2945, Dec. 2007, doi: 10.1109/TIE.2007.907044.

[6] L. Maharjan, S. Inoue and H. Akagi, "A Transformerless Energy Storage System Based on a Cascade Multilevel PWM Converter With Star Configuration," in IEEE Transactions on Industry Applications, vol. 44, no. 5, pp. 1621-1630, Sept.-Oct. 2008, doi: 10.1109/TIA.2008.2002180.

[7] H. Akagi, S. Inoue and T. Yoshii, "Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration," in IEEE Transactions on Industry Applications, vol. 43, no. 4, pp. 1041-1049, July-aug. 2007, doi: 10.1109/TIA.2007.900487.

[8] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth and R. C. N. Pilawa-Podgurski, "Design of a GaN-Based Interleaved Nine-Level Flying Capacitor Multilevel Inverter for Electric Aircraft Applications," in IEEE Transactions on Power Electronics, vol. 35, no. 11, pp. 12153-12165, Nov. 2020, doi: 10.1109/TPEL.2020.2989329.

[9] M. L. Gasperi, "Life prediction model for aluminum electrolytic capacitors," IAS '96. Conference Record of the 1996 IEEE Industry Applications Conference Thirty-First IAS Annual Meeting, San Diego, CA, USA, 1996, pp. 1347-1351 vol.3, doi: 10.1109/IAS.1996.559241.

[10] A. M. Imam, D. M. Divan, R. G. Harley and T. G. Habetler, "Real-Time Condition Monitoring of the Electrolytic Capacitors for Power Electronics Applications," APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 2007, pp. 1057-1061, doi: 10.1109/APEX.2007.357646.

[11] U. Choi, K. Lee and F. Blaabjerg, "Diagnosis and Tolerant Strategy of an Open-Switch Fault for T-Type Three-Level Inverter Systems," in IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 495-508, Jan.-Feb. 2014, doi: 10.1109/TIA.2013.2269531.

[12] B. Li, S. Shi, B. Wang, G. Wang, W. Wang and D. Xu, "Fault Diagnosis and Tolerant Control of Single IGBT Open-Circuit Failure in Modular Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 31, no. 4, pp. 3165-3176, April 2016, doi: 10.1109/TPEL.2015.2454534.

[13] X. Li, S. Dusmez, B. Akin and K. Rajashekara, "A New Active Fault-Tolerant SVPWM Strategy for Single-Phase Faults in Three-Phase Multilevel Converters," in IEEE Transactions on Industrial Electronics, vol. 62, no. 6, pp. 3955-3965, June 2015, doi: 10.1109/TIE.2014.2364555.

[14] J. Amini and M. Moallem, "A Fault-Diagnosis and Fault-Tolerant Control Scheme for Flying Capacitor Multilevel Inverters," in IEEE Transactions on Industrial Electronics, vol. 64, no. 3, pp. 1818-1826, March 2017, doi: 10.1109/TIE.2016.2624722.

[15] S. Peyghami, H. Wang, P. Davari and F. Blaabjerg, "Mission-Profile-Based System-Level Reliability Analysis in DC Microgrids," in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 5055-5067, Sept.-Oct. 2019, doi: 10.1109/TIA.2019.2920470.

[16] M. Musallam, C. Yin, C. Bailey and M. Johnson, "Mission Profile-Based Reliability Design and Real-Time Life Consumption Estimation in Power Electronics," in IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2601-2613, May 2015, doi: 10.1109/TPEL.2014.2358555.

[17] E. Gurpinar, Y. Yang, F. Iannuzzo, A. Castellazzi and F. Blaabjerg, "Reliability-Driven Assessment of GaN HEMTs and Si IGBTs in 3L-ANPC PV Inverters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 956-969, Sept. 2016, doi: 10.1109/JESTPE.2016.2566259.

[18] K. Yao, C. Cao and S. Yang, "Noninvasive Online Condition Monitoring of Output Capacitor's ESR and C for a Flyback Converter," in IEEE Transactions on Instrumentation and Measurement, vol. 66, no. 12, pp. 3190-3199, Dec. 2017, doi: 10.1109/TIM.2017.2749838

[19] M. W. Ahmad, N. Agarwal and S. Anand, "Online Monitoring Technique for Aluminum Electrolytic Capacitor in Solar PV-Based DC System," in IEEE Transactions on Industrial Electronics, vol. 63, no. 11, pp. 7059-7066, Nov. 2016, doi: 10.1109/TIE.2016.2582470.

[20] K. Yao, W. Tang, X. Bi and J. Lyu, "An Online Monitoring Scheme of DC-Link Capacitor's ESR and C for a Boost PFC Converter," in IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5944-5951, Aug. 2016, doi: 10.1109/TPEL.2015.2496267.

[21] X. Pu, T. H. Nguyen, D. Lee, K. Lee and J. Kim, "Fault Diagnosis of DC-Link Capacitors in Three-Phase AC/DC PWM Converters by Online Estimation of Equivalent Series Resistance," in IEEE Transactions on Industrial Electronics, vol. 60, no. 9, pp. 4118-4127, Sept. 2013, doi: 10.1109/TIE.2012.2218561

[22] A. G. Abo-Khalil and D. Lee, "DC-Link Capacitance Estimation in AC/DC/AC PWM Converters Using Voltage Injection," in IEEE Transactions on Industry Applications, vol. 44, no. 5, pp. 1631-1637, Sept.-Oct. 2008, doi: 10.1109/TIA.2008.2002181.

[23] M. W. Ahmad, P. N. Kumar, A. Arya and S. Anand, "Noninvasive Technique for DC-Link Capacitance Estimation in Single-Phase Inverters," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 3693-3696, May 2018, doi: 10.1109/TPEL.2017.2762341.

[24] N. Agarwal, M. W. Ahmad and S. Anand, "Quasi-Online Technique for Health Monitoring of Capacitor in Single-Phase Solar Inverter," in IEEE Transactions on Power Electronics, vol. 33, no. 6, pp. 5283-5291, June 2018, doi: 10.1109/TPEL.2017.2736162.

[25] M. A. Vogelsberger, T. Wiesinger and H. Ertl, "Life-Cycle Monitoring and Voltage-Managing Unit for DC-Link Electrolytic Capacitors in PWM Converters," in IEEE Transactions on Power Electronics, vol. 26, no. 2, pp. 493-503, Feb. 2011, doi: 10.1109/TPEL.2010.2059713.

[26] T. H. Nguyen and D. Lee, "Deterioration Monitoring of DC-Link Capacitors in AC Machine Drives by Current Injection," in IEEE Transactions on Power Electronics, vol. 30, no. 3, pp. 1126-1130, March 2015, doi: 10.1109/TPEL.2014.2339374.

[27] D. Ronanki and S. S. Williamson, "Failure Prediction of Submodule Capacitors in Modular Multilevel Converter by Monitoring the Intrinsic Capacitor Voltage Fluctuations," in IEEE Transactions on Industrial Electronics, vol. 67, no. 4, pp. 2585-2594, April 2020, doi: 10.1109/TIE.2019.2912771.

[28] K. Wang, L. Jin, G. Li, Y. Deng and X. He, "Online Capacitance Estimation of Submodule Capacitors for Modular Multilevel Converter With Nearest Level Modulation," in IEEE Transactions on Power Electronics, vol. 35, no. 7, pp. 6678-6681, July 2020, doi: 10.1109/TPEL.2019.2959074.

[29] M. P. Kazmierkowski, R. Krishnan, and F. Blaabjerg, Control in power electronics. Academic Press, 2002.

[30] N. Mohan, T. M. Undeland, and W. P. Robbins, Power electronics, 3rd ed. John Wiley & Sons, Inc., 2003.

[31] J. Holtz, “Pulsewidth modulation electronic power conversion,” Proceedings of the IEEE, vol. 82, no. 8, pp. 1194–1214, August 1994.

[32] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, “Predictive control in power electronics and drives,” IEEE Transactions on Industrial Electronics, vol. 55, no. 12, pp. 4312–4324, December 2008.

[33] P. Mutschler, “A new speed-control method for induction motors,” in Conference Record of PCIM’98, Nuremberg, pp. 131–136, May 1998.

[34] J. Holtz and S. Stadtfeld, “A predictive controller for the stator current vector of AC machines fed from a switched voltage source,” in International Power Electronics Conference, IPEC, Tokyo, pp. 1665–1675, 1983.

[35] T. Kawabata, T. Miyashita, and Y. Yamamoto, “Dead beat control of three phase PWM inverter,” IEEE Transactions on Power Electronics, vol. 5, no. 1, pp. 21–28, January 1990.

[36] O. Kukrer, “Discrete-time current control of voltage-fed three-phase PWM inverters,” IEEE Transactions on Industrial Electronics, vol. 11, no. 2, pp. 260–269, March 1996.

[37] S. Kouro, P. Cort´es, R. Vargas, U. Ammann, and J. Rodr´ıguez, “Model predictive control – a simple and powerful method to control power converters,” IEEE Transactions on Industrial Electronics, vol. 56, no. 6, pp. 1826–1838, June 2009.

[38] J. Holtz and X. Qi, "Optimal Control of Medium-Voltage Drives—An Overview," in IEEE Transactions on Industrial Electronics, vol. 60, no. 12, pp. 5472-5481, Dec. 2013, doi: 10.1109/TIE.2012.2230594.

[39] G. S. Buja and G. B. Indri, "Optimal Pulsewidth Modulation for Feeding AC Motors," in IEEE Transactions on Industry Applications, vol. IA-13, no. 1, pp. 38-44, Jan. 1977, doi: 10.1109/TIA.1977.4503359.

[40] A. Bendre, G. Venkataramanan, D. Rosene and V. Srinivasan, "Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation," in IEEE Transactions on Industrial Electronics, vol. 53, no. 3, pp. 718-726, June 2006, doi: 10.1109/TIE.2006.874424.

[41] Y. Jiao, F. C. Lee and S. Lu, "Space Vector Modulation for Three-Level NPC Converter With Neutral Point Voltage Balance and Switching Loss Reduction," in IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5579-5591, Oct. 2014, doi: 10.1109/TPEL.2013.2294274.

[42] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez and J. Pontt, "Predictive Control of a Three-Phase Neutral-Point-Clamped Inverter," in IEEE Transactions on Industrial Electronics, vol. 54, no. 5, pp. 2697-2705, Oct. 2007, doi: 10.1109/TIE.2007.899854.

[43] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez and J. Pontt, "Predictive Control of a Three-Phase Neutral-Point-Clamped Inverter," in IEEE Transactions on Industrial Electronics, vol. 54, no. 5, pp. 2697-2705, Oct. 2007, doi: 10.1109/TIE.2007.899854.

[44] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," in IEEE Transactions on Industry Applications, vol. 41, no. 2, pp. 655-664, March-April 2005, doi: 10.1109/TIA.2005.844382.

[45] Bin Wu; Mehdi Narimani, "Other Multilevel Voltage Source Inverters," in High-Power Converters and AC Drives, IEEE, 2017, pp.185-223, doi: 10.1002/9781119156079.ch9.

[46] M. Narimani, B. Wu, Z. Cheng and N. R. Zargari, "A New Nested Neutral Point-Clamped (NNPC) Converter for Medium-Voltage (MV) Power Conversion," in IEEE Transactions

on Power Electronics, vol. 29, no. 12, pp. 6375-6382, Dec. 2014, doi: 10.1109/TPEL.2014.2306191.

[47] A. Dekka and M. Narimani, "Capacitor Voltage Balancing and Current Control of a Five-Level Nested Neutral-Point-Clamped Converter," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10169-10177, Dec. 2018, doi: 10.1109/TPEL.2018.2810818.

[48] A. Dekka, B. Wu, R. L. Fuentes, M. Perez and N. R. Zargari, "Evolution of Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1631-1656, Dec. 2017, doi: 10.1109/JESTPE.2017.2742938.

Publications

Conference Paper

R. Nemade, A. K. Rathore, C. Cecati and C. Buccella, "Analysis of Capacitor Current Stress in Five-Level Active Neutral Point Clamped Converter," 2019 IEEE Industry Applications Society Annual Meeting, Baltimore, MD, USA, 2019, pp. 1-6, doi: 10.1109/IAS.2019.8912452.

R. Nemade, A. K. Rathore, "An Online Condition Monitoring Technique for DC-Link Capacitors in Three-Level Neutral Point Clamped Converter operated with Finite Control Set Model Predictive Current Control" 2021 IEEE Industry Applications Society Annual Meeting (Vancouver Convention Centre, Vancouver, British Columbia) **[Submitted]**.