Design and Improved Switching Transient Modeling for A GaN-based Three Phase Inverter

Yang Luo

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By: Yang Luo

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complies with the regulations of this University and meets the accepted standards with respect to originality and quality.

Signed by the final examining committee:

_____ Chair

Dr. Luiz A. C. Lopes

_____ Examiner

Dr. Chunyan Wang

_____ Examiner

Dr. Luiz A. C. Lopes

_____ Thesis Supervisor(s)

Dr. Chunyan Lai

_____ Thesis Supervisor(s)

Dr. Pragasen Pillay

Approved by _____

Dr. Yousef R. Shayan, Chair of Department

April 22, 2021 _____

Date of defense Dr. Mourad Debbabi, Dean,

Gina Cody School of Engineering and Computer Science

Abstract

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Yang Luo MASc.

Concordia University, 2021

In recent years, wide-bandgap devices (WBG) such as silicon carbide (SiC) and gallium nitride (GaN) transistors have drawn significant research attention in power conversion applications where higher efficiency, higher power density and lower cost are required, for example, in electric vehicle (EV) applications. Owing to its better figures of merit on on-resistance, switching speed and junction temperature, enhancement-mode GaN high electron mobility transistors (HEMTs) are able to be operated with switching frequency up to the megahertz range, through which the size of passive components in the power converters can be significantly reduced. Consequently, the power converter's integration level and power density can be increased.

In GaN-based power converters, the switching energy loss increases naturally along with the switching frequency, which is the dominant loss component. Consequently, it is always one of the top priority performances to be considered in research and development activities. For device manufacturers, with access to internal materials and dimensional parameters, physics-based device models are usually used. Although these models can reveal detailed characteristics of the devices, they are not accessible to the public and can be very time-consuming to develop. Analytical models, that can emulate the transistor's dynamic behaviour and predict the switching energy loss without consuming too much computing resources, are always an essential tool to help provide guidelines to engineers for circuit design and performance optimization purposes. This thesis develops a computationally inexpensive and straightforward switching transient model which proves to be more accurate than conventional model through simulation and experiments.

Currently, in the commercial market, there are only a few mature designs of GaN three-phase inverter products, and most of them are costly. This unavoidable phenomenon is led by

the fact that the gate driver and power loop design for GaN is demanding. Some companies such as EPC, Navitas and Power Integrations are committed to monolithic-integrated gate drivers, but they are complex and expensive. Thus, this thesis also aims to design a GaN-based three-phase inverter with low cost and low complexity in the gate drive circuit. In addition, to achieve high performance GaN-based inverter, parasitic components in the power loop have to be minimized. In this thesis study, parasitic parameters of the power loop are extracted through Ansys Q3D simulation and then validated through experimental test results. With accurate parasitic parameters, the layout of the PCBs is improved to achieve better inverter performance.

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CHAPTER 1 INTRODUCTION

1.1 Introduction of GaN HEMTs

After six decades of development, the performance of silicon devices has reached its limit and is difficult to meet the requirements required by the new generation of power conversion systems. As early as 2004, gallium nitride (GaN) high electron mobility transistors (HEMTs) made by Eudyna Corporation in Japan appeared [1]. However, acceptance outside of its application has been limited by the device cost as well as the inconvenient feature of depletion-mode operation, which means, if a negative voltage is not applied between the gate and the source electrode at the startup of a power converter, a short-circuit will occur. When the enhancement-mode (e-mode) GaN HEMTs designed by Efficient Power Conversion Corporation (EPC) was introduced in June 2009, GaN devices started to be manufactured at a relatively low cost and then entered the public [1]. Since then, many other international semiconductor companies such as Canada's GaN Systems, Germany's Infineon, Japan's Panasonic, and American's Transphorm announced their intention to manufacture GaN transistors for the power conversion market whose sample products are shown as in Figure 1.1. By now, the highest breakdown voltage that commercially available GaN devices can reach is

(a) GS66516T from GaN Systems

(b) IGO60R070D1 from Infineon

(c) PGA26E07BA from Panasonic

(d) TP65H035WSQA from Transphorm

Figure 1. 1 Products from different manufacturers

1200 V.

In recent years, GaN transistors have been drawing more and more attention for high power density and high efficiency power conversion applications due to its superior characteristics such as higher band gap, higher critical field and higher electron mobility as shown in Table 1.1 [1], which can lead to excellent electrical properties:

1) Lower intrinsic leakage currents and higher operating temperatures: The band gap of GaN material is around three times of that of Silicon (Si) which means the strength of the chemical bonds between the atoms in the lattice is stronger and thus an electron jumping from one site to another is more difficult.
2) Higher breakdown voltage: The critical breakdown electric field of GaN is ten times Si material which is up to 3.3 MV/cm. Consequently, GaN devices have a higher blocking voltage.
3) Faster switching frequency: GaN devices can be developed to operate at a switching frequency in the MHz level due to its small junction capacitance. Higher switching frequency is a dominant catalyst to enhance the performance of power conversion systems and reduce the system volume [2].
4) Lower on-resistance: GaN devices have a high electron saturation rate which is 2.8 times than Silicon, leading to a small on-resistance. This mainly contributes to lower conduction losses, therefore, higher overall efficiency can be attained.

Table 1. 1 Comparison between Silicon and GaN

Parameter	**Silicon**	**GaN**
Band gap E_g (eV)	1.12	3.39
Critical Field E_{Crit} (MV/cm)	0.23	3.3
Electron Mobility μ_n ($cm^2/V \cdot s$)	1400	1500
Permittivity ε_r	11.8	9
Thermal Conductivity λ (W/cm·K)	1.5	1.3
Saturated electron velocity (10^7cm/s)	1.0	2.8

Researchers and industries have been devoting a lot of energy and time to develop the potential of GaN devices in recent years. As an effective way to reduce the size of the system and increase the overall efficiency, GaN transistors have been used widely in different applications such as electrical vehicles, high speed railways, industrial motors, aerospace, smart grids, renewable energy generation, etc. [3]-[5], and it is proven that GaN HEMTs outperforms Si devices as a new-generation solution [6]-[8].

1.2 Literature review

In this section, a detailed review of the application and research status of GaN-based power conversion especially motor drive systems is provided.

In the high frequency, high efficiency DC/AC power conversion area, GaN HEMTs have also brought innovations to solve the demanding requirements from industry. For example, drives for servo motors and other high-speed motors may demand a fundamental excitation frequency of 1 kHz or more, with comparable sample and feedback rates for feedback and control. This requires the carrier frequency to be increased in the proportion to the motor speed. In conventional motor drive designs, silicon based IGBTs were used as the switching devices in the bridge leg of the inverter. Systems such as these are always constrained to a choice between coarse control, with barely ten steps per control cycle at 12 kHz of switching frequency, and high switching loss incurred by switching IGBTs at higher frequencies of tens of kilo-hertz. GaN HEMTs which can switch at over several hundred kilo-hertz with relative low switching loss, can eliminate this constraint. Besides, the increase in the PWM frequency also brings other advantages in motor drive applications such as reduced motor current ripple, lower motor losses and reduced filter size and cost. Figure 1.2 shows an example setup with a GaN-based motor drive.

As for the research progress on the three-phase inverter for motor drives, [9] compared the power conversion efficiency of a GaN inverter for different output powers with a conventional IGBT-based inverter. The GaN-based converter achieved over 98% efficiency from 100 W to 900 W as a result of the operation of the normally-off GaN transistors

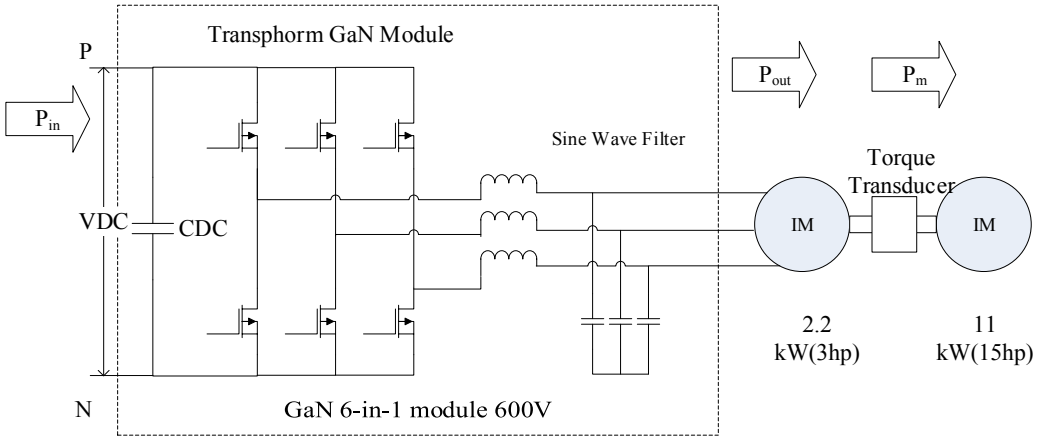


Figure 1. 2 Schematic of test setup for GaN based drive (Shirabe *et al*. 2012)

eliminating the fast recovery diodes which are needed to be connected in parallel with IGBTs in conventional inverters. It presented a successful operation at 900 W with the carrier frequency of 6 kHz and DC bus voltage of 200 V and it was verified by the experiment that the efficiency could reach as high as 99.3% which is the highest ever achieved in Si-IGBT inverters. The bidirectional conducting feature of GaN devices with low on-resistance significantly contributed to the improvement of efficiency.

[10] simulated a 1 kW Si-based and a GaN-based inverter for comparison of efficiency. Different load conditions and power factor angles using a synchronous motor load were set in the simulation to represent various operating conditions. The simulation results showed that the power losses in the Si-based inverter was about 8 times higher than those in the GaN-based inverter. The power conversion efficiency reached the highest point at full load condition with unity power factor where the corresponding efficiency of the GaN inverter was 99.41%, which is 4.89% absolute higher than the Si counterpart (94.52%). Moreover, even though the thermal conductivity of GaN devices is poorer than that of Si devices significantly, it was found that the cooling requirements of GaN-based inverter was less demanding due to its lower losses.

In [11], the switching behavior and switching loss were analyzed to evaluate the performance of GaN HEMTs. This paper proposed a three-phase inverter consisting of six 650 V, 30 A GaN HEMTs free from free-wheeling diodes and a sine-output filter. It was tested at different operating points by changing the motor frequency and the load in steps from no load to full load. The highest efficiency of the system was 97% at an output power of 1.5 kW. Moreover, the line currents waveforms and the line-to-line voltage waveforms were observed

to become pure sinusoidal after the filter which further reduced the motor losses.

In [12] and [13], the operating characteristics of a normally-on GaN HEMT device with a normally-off low voltage Si-based MOSFET in cascade were discussed, and the test results showed that it has the advantage of low switching, conduction losses, and operation without any external freewheeling diode. Further, the switching and conduction loss in the 6-in-1 GaN HEMT device operating at 100 kHz is seen to be much lower than the Si-based IGBT inverter operating at 15 kHz. The size of the output sine wave filter is very small and the loss in the sine wave filter is much lower than the extra losses in the motor without filter.

In [14], a three-phase motor drive system was proposed based on lateral enhancement-mode GaN devices with vertical power loop structure and common mode noise current propagation control. It was verified through experiments that the system could run stably at a switching frequency of 100 kHz for a long time. However, on each PCB, there is only one power bridge with corresponding gate circuits. Three separate bridges are needed to form a three-phase inverter. Consequently, the whole system is not compact enough.

[15] designed a 10 kW inverter whose overall boxed volume is only 0.57 Liters including the air space without any passive AC filters, which means it achieved a high power density of 17.5 kW/L. With forced air cooling and low parasitic inductance layout design in power loop, the inverter performed well both in thermally and electrically. However, in the design, gate loop and power loop are placed together on a PCB. Thus, the electromagnetic interference (EMI) noise may propagate through the parasitic parameters to the power stage and control circuits and bring electromagnetic compatibility (EMC) issues to the system.

As for the gate driver design, [16] and [17] address integration of gate driver circuits with half-bridge power stages in a depletion-mode GaN-on-SiC process, which reduces the gate-driver area by around 80% compared to the bootstrap gate structure, but it has high complexity and cost. Meanwhile, the drain turn-off rising edge is not adjustable, and it limits the design flexibility which is not optimal.

A solution using High Voltage BCD (Bipolar CMOS DMOS) technology is developed in [18], which is compact by integrating the whole driving circuits into a single die. It is suitable for high voltage GaN HEMTs with great peak current capability and fast input to output propagation. However, the value of the turn-on gate resistor is limited to 130 Ohms. The turn-

on speed and the gate-to-source voltage spike during the turn-on event cannot be controlled by varying the gate resistor. Thus, the dynamics performance of the device is limited.

[19] shows an interleaved step-down buck converter operating at switching frequency of 1 MHz using GaN power stage integrated circuits LMG5200, which is manufactured by Texas Instruments. The inclusion of an integrated driver circuit can significantly facilitate its implementation and reduce parasitic impedances. It has been proved that the physical dimension of the converter is reduced considerably and the parasitic parameters are low. However, the power stage is not suitable for high power applications.

In summary, different literatures have proven that GaN-based converter exhibits significantly higher overall efficiency than Si-based converters. However, a comprehensive understanding of the gate drive circuit design is also needed to develop the potential of GaN HEMTs to save energy and increase power density in power switching systems in the future.

1.3 Research objectives and publications

The main objective of this thesis is to design a three-phase inverter using the new generation GaN transistors. During the design process, new switching transient models that are more accurate for GaN HEMTs are proposed and validated. To successfully build an inverter requires an overall understanding of not only the switching characteristics of power switches, but that of the gate circuit considerations, component selection, associated electrical and physical specifications, PCB routing requirements, and so on. The work presented in the thesis goes through circuit design, device selection, PCB manufacture concerns and related design issues. The objectives of this thesis are listed below:

1. Development of improved models for turn-on and turn-off transient happening in GaN devices. The proposed switching on and switching off loss models are validated to be more accurate than the traditional ones based on the experimental test results.
2. Analysis of the third quadrant operation of GaN devices. The proposed reverse turn-on model is analyzed and applied to the GaN transistors in the half-bridge converter topology, which also helps to define a proper dead-time.
3. Statement of gate drive design considerations and design of a GaN-based three-phase

inverter using standard components and the fewest circuit blocks to maintain the simplicity of the circuit, and to provide knowledge for future development of this solution.

4. Investigation and extraction of the parasitic parameters in the PCB traces of the power loops to provide proof for further improvement on the layout of inverter and gate drive design.

Contributions in form of publications contain:

Y. Luo, S. N. Afrasiabi, C. Lai and P. Pillay, "An Improved Method to Estimate Turn-on Switching Loss of 650V GaN HEMTs in Hard-switching Topology," *2020 23rd International Conference on Electrical Machines and Systems (ICEMS)*, Hamamatsu, Japan, 2020.

J. Tian, C. Lai, Y. Luo, S. Turco, S. Gangavarapu, P. Kortan, L. V. Iyer, N. C. Kar, "A Comprehensive Analytical Switching Transients and Loss Modeling with Accurate Parasitic Parameters for Enhancement-mode Gallium Nitride Transistors," to be submitted to SAE International Journal of Electrified Vehicles.

1.4 Thesis outline

The rest of this thesis is divided into four chapters as described below:

In chapter 2, the operating principles and characterizations of GaN HEMTs are demonstrated. With different internal structure, the switching mechanism should also be of difference, but it is neglected in the traditional model. Using the conventional model for switching events, where the current bump and load condition are not considered and corresponding parasitic parameters are directly taken from the datasheet, a significant deviation can be found which indicates that it is not suitable for GaN-based switches. Consequently, an improved method is proposed through a more accurate switching transient model and parasitic parameter values. The plateau shifting is also considered to improve the accuracy of turn-off time estimation. The operation and performance of the double pulse test are demonstrated with the simulation results using LTspice software, and experimental results. The proposed model is proved to be more accurate than the traditional model.

In chapter 3, the target is to design a three-phase inverter with a compact structure and low complexity and cost. The design of the whole system mainly contains a three-phase inverter design, gate drive circuit design, and power supply board design. The major component selection is demonstrated based on the literature survey, and the considerations for the design of the GaN inverter are examined. The process includes a schematic picture and layout realization, which requires both circuit analysis and the understanding of basic design principles of PCB technology. The PCBs have been manufactured and assembled, with a heatsink attached to meet the cooling requirements.

In chapter 4, the troubleshooting process and some basic tests such as double pulse test and three-phase RL load tests on the inverter designed in chapter 3 are conducted and the results are presented. The problems found in the original design are demonstrated and also analyzed. The parasitic parameters are verified through Ansys Q3D software and experiments to help improve the second version where a more compact and effective design is expected. Both the gate drive circuit and the power loop are improved by using distributed capacitors and improvement on the layout settings. Moreover, more functions are added to the new design such as adjustable gate voltages, testing interfaces. Due to the timeline issue, the new version has been put into production but has not been assembled yet. But through the 3D simulation results in the software Ansys Q3D, the parasitic components are reduced by 60% on the loop parasitic inductance.

The last chapter is the conclusions and future outlook.

CHAPTER 2 CHARACTERIZATION AND SWITCHING TRANSIENT ANALYSIS OF GAN HEMT

2.1 Introduction

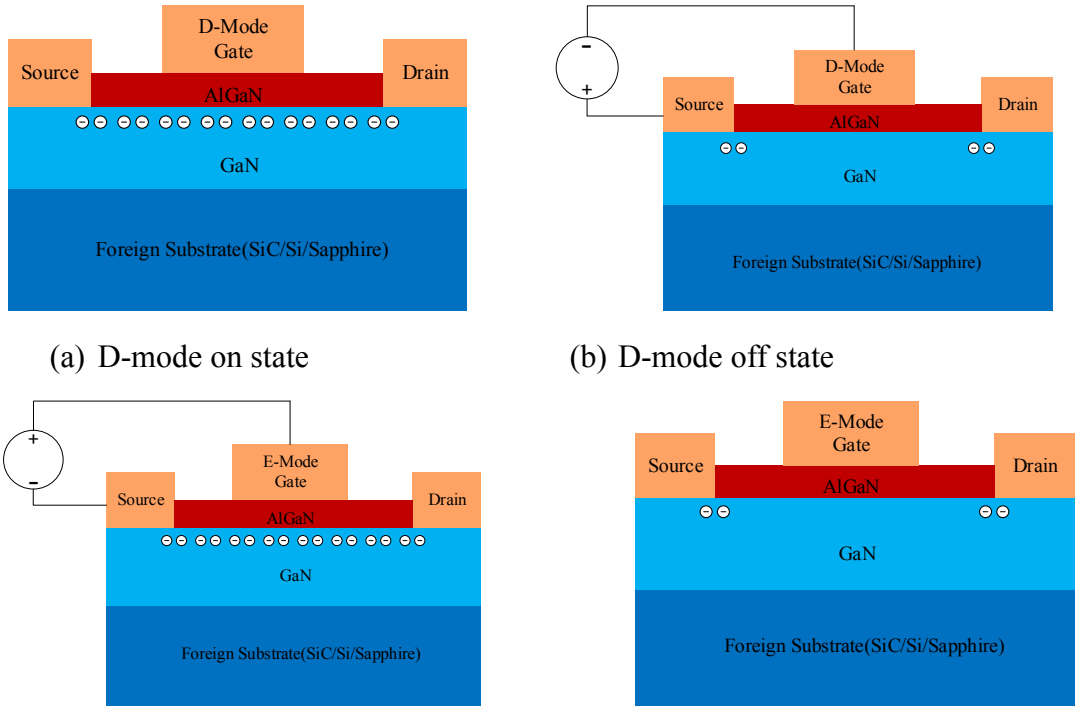
2.1.1 Operating principle of GaN transistors

There are generally two types of GaN HEMTs categorized by operating modes: the depletion mode (D-mode or normally-on mode) and the enhanced mode (E-mode or normally-off mode) as shown in Figure 2.1. Generally, the basic structure of GaN HEMT is very close to a power field effect transistor (FET) with three electrodes: gate, source, and drain which can be categorized as one type of voltage-controlled power switches.

For the D-mode GaN transistor shown in Figure 2.1(a), the source and drain electrodes pierce through the top AlGaN layer to form an ohmic contact with the underlying two-dimensional electron gas (2DEG). This creates a short-circuit between the source and the drain until the 2DEG "pool" of electrons is depleted and the semi-insulating GaN crystal can block the flow of current. In order to deplete the 2DEG, a gate electrode is placed on top of the AlGaN layer. In most of the early GaN transistors, this gate electrode was formed as a Schottky contact to the top surface. By applying negative voltage to this contact, the Schottky barrier becomes reverse biased and the electrons underneath are depleted. Therefore, in order to turn this device OFF, a negative voltage relative to both drain and source electrodes is needed as shown in Figure 2.1(b). Therefore, this depletion mode GaN transistor (D-mode GaN) is also called normally-on mode GaN, or high electron mobility transistor (HEMT).

The depletion operation mode GaN is commonly used in RF applications but has limited applications in the area of power conversion, as during the start-up of a power converter, a negative bias must first be applied otherwise a short-circuit will occur. An enhanced mode (or so-called normally-off) device would not suffer from this limitation and thus is suitable for use in power electronics converters. The E-mode GaN transistors behave in a similar way to silicon

power metal-oxide-semiconductor field-effect transistors (MOSFET). As shown in Figure 2.1(c), a positive gate-source voltage difference is applied on the gate electrode and attracts electrons into the channel to form a bidirectional channel between the source and drain. As the electrons are pooled in the 2DEG, the overall resistance of the conducting channel is very low. However, if the voltage is removed from the gate as in the case of Figure 2.1(d), the electrons underneath it disperses, removing the conductive channel and turning the device off. In contrast to most silicon power MOSFETs, which employ a vertical, through-die channel structure, the E-mode structure provides the transistor with a low gate charge, which contributes further to an improved figure of merit (FoM) and very-high-performance switching, well into the megahertz range.



(a) D-mode on state (b) D-mode off state

(c) E-mode on state (d) E-mode off state

Figure 2. 1 Basic depletion mode and enhanced mode GaN transistor structure [1]

2.1.2 Hard-switching loss analysis

When the enhancement-mode GaN transistor designed by Efficient Power Conversion Corporation (EPC) was introduced in June 2009, GaN devices started to enter the market of power conversion [1]. Compared with the state-of-the-art Silicon devices, GaN HEMTs can

operate under higher switching frequency while having a higher efficiency due to lower losses. It can be seen from Figure 2.2, the Silicon IGBT bears approximately 10 times higher turn-on and turn-off losses than the counterpart with GaN material [20].

In hard-switching topologies, GaN HEMTs are turned on and off at an extremely high speed, thus during the transition period significant losses will occur while the voltage and

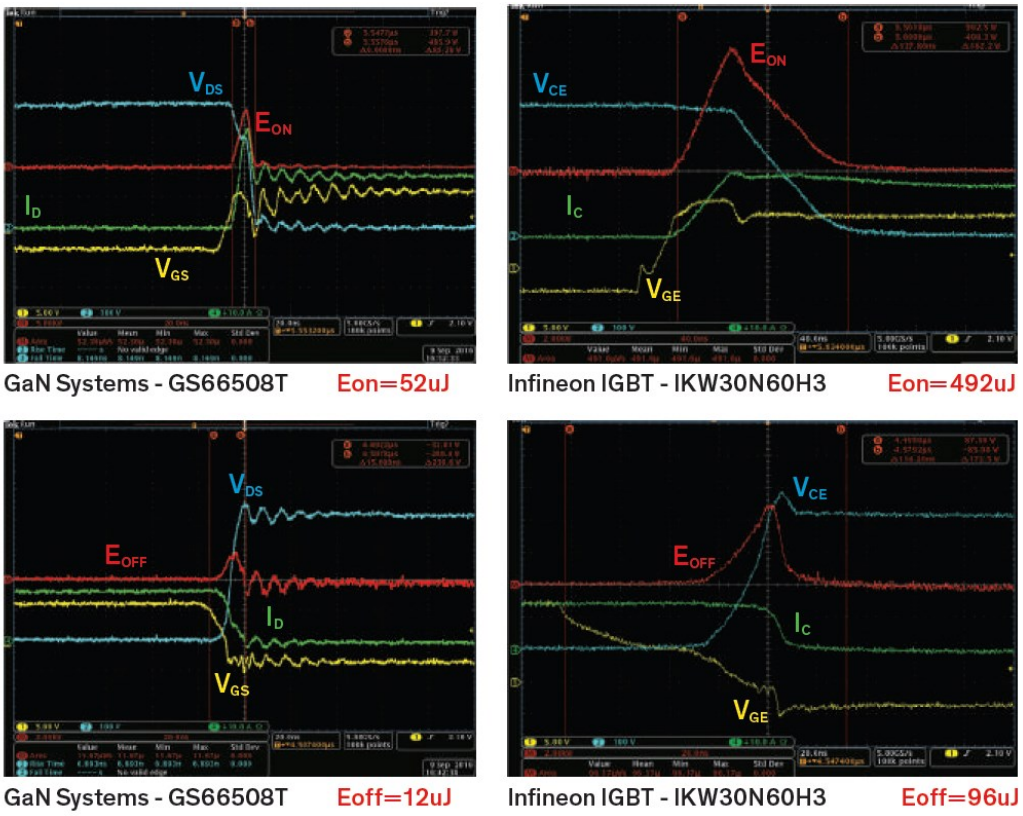


Figure 2. 2 Switching losses comparison between GaN HEMT and IGBT

current are in an overlapping region [21]. Since GaN HEMT is usually operated at much higher switching frequency, the switching losses especially in hard-switching topology contribute to the major part of total power loss which becomes a limitation of its application and lower the upper bound of its capability [22]. Thus, in order to help develop the full potential of GaN HEMT, it is valuable to gain an in-depth insight into the switching transient process and dynamic losses. As for the switching loss estimation of GaN, the turn-on loss of a GaN transistor is around 5 times higher than turn-off loss as can be observed from the results in [20]. Generally, the method to calculate the switching loss in GaN HEMTs is similar to that for the switching loss calculation in Silicon devices [1]. However, the difference between them should

be not be ignored to achieve a more precise estimation result. Take the turn-on process as an example, the rise time of drain-to-source current (I_{DS}) and fall-time of drain-to-source voltage (V_{DS}) are calculated first according to the approximate value of parasitic capacitance given in the datasheet. Secondly, the approximate losses can be derived [23]. However, the corresponding values provided in the datasheet are only obtained under a specific circumstance and they may be inaccurate in some other cases. Moreover, the traditional method considers the current rising trend to be smooth, which means the current spike is usually neglected in the traditional estimation method, because it is negligible for Silicon devices [24], [25]. However, ignoring the losses induced by the current overshoot will lead to a significant deviation when calculating the switching loss for GaN HEMTs.

Moreover, the symmetry of the conducting channel between the source and the drain electrode enables the GaN HEMT to conduct in the third quadrant mode where a freewheeling diode usually exists in Si-based converters but not needed to be paralleled in the GaN converter. Considering a half-bridge leg in a voltage source converter (VSC), two devices are turned on and off complementarily controlled by a Pulse Width Modulated (PWM) signal. Considering the non-ideal behavior of the devices, an interval of dead-time should be introduced before the subsequent turn-on to ensure safe operation. Even though the device manufacturers such as GaN Systems provide some application notes to guide the users to set the dead-time [26]-[27], the recommended values can be inadequate in some specific application scenarios. Through looking into the half-bridge structure, a more comprehensive model for the turn-off transient is also of value to help the designers choose appropriate dead-times and to develop the full potential of GaN devices.

[28] discusses the voltage fall/rise time scaling. They reveal the relationship between the transition time and operating voltage, reverse transfer capacitance, but the load condition is not considered. To evaluate the turn-off performance of GaN switches more precisely, a considerable deviation will occur if the load condition is not taken into consideration.

2.2 Switching event analysis

This section presents the traditional models for GaN HEMTs and describes the limitations.

2.2.1 Traditional turn-on model

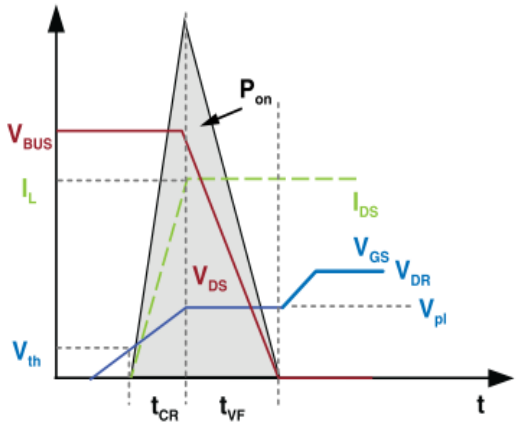


Figure 2. 3 Traditional turn-on transient

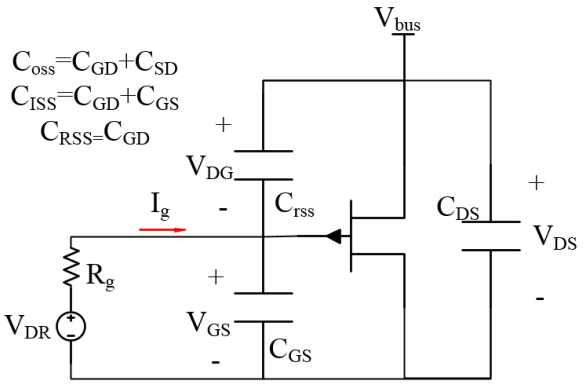


Figure 2. 4 Equivalent circuit of GaN HEMT

In hard-switching converters, low dynamic losses are the key to maintain high efficiency if they are driven at a high switching frequency. The dominant composition of the losses happens when, such as in a turn-on switching event, the current flows through the drain channel before the drain-to-source voltage commutates to zero. The traditional estimation method is assumed based on the transient process shown in Figure 2.3 [1]. The initial state of GaN HEMT is the off state. The voltage across the transistor is the DC bus voltage and no current is flowing through the channel (ignoring the leakage current). By adding a drive voltage (V_{DR}) between the gate electrode and the source electrode, the device starts to turn on. During the turn-on event, the transistor channel starts to conduct when the gate-to-source voltage (V_{GS}) reaches the threshold voltage (V_{th}). Then V_{GS} continues rising to the miller plateau voltage (V_{pl}) during which period the drain current (I_{DS}) rises from 0 to load current (I_L). This period is considered to be the transition-time of current (t_{CR}). After the completion of the current transition, another obvious feature during the V_{DS} decrease that V_{GS} keeps constant at V_{pl} during the voltage transition-time (t_{VF}) can also be observed.

In the traditional method to calculate the turn-on switching loss of GaN devices, a flat miller plateau is assumed, which considers the plateau voltage (V_{pl}) to be a constant value. In the voltage transition-time, the drain-to-source voltage (V_{DS}) decreases from the DC bus voltage down to zero. Under the assumption that the gate voltage is constant during the voltage transition period, the current that charges the internal gate-to-drain capacitor (C_{GD}), which is also the reverse transfer capacitor (C_{rss}), can be considered to be equal to the current flowing

through the gate electrode. Thus, C_{rss} starts to charge to remove the blocking voltage. After this process, the gate current goes back to the source electrode again and continues to charge the gate-to-source capacitor (C_{GS}).

Based on the demonstrated presupposition, in [1], an ideal assumption identical to the above mechanism is applied to calculate the switching losses of GaN devices during the hard-switching turn-on event. According to the equivalent circuit of the GaN HEMT shown in Figure 2.4, the charging current can be obtained through the gate drive voltage and the gate resistor (R_g) in the turn-on gate drive loop. Then, the current rise-time (t_{CR}) can be derived as (2-3).

$$Q_{GS(pt)} = I_g \times t_{CR} \tag{2-1}$$

$$I_g = \frac{V_{DR} - \frac{V_{pl}+V_{th}}{2}}{R_g} \tag{2-2}$$

$$t_{CR} = Q_{GS(pt)} \times \frac{R_g}{V_{DR} - \frac{V_{th}+V_{pl}}{2}} \tag{2-3}$$

with $$Q_{GS(pt)} = Q_{GS} \times \frac{V_{pl}-V_{th}}{V_{pl}} \tag{2-4}$$

where I_g is the current flowing through the gate electrode (either going to C_{rss} or C_{GS}); Q_{GS} and $Q_{GS(pt)}$ is charge required to increase V_{GS} from 0 to V_{pl} and from V_{th} to V_{pl} respectively.

The voltage fall-time (t_{VF}) can be derived with (2-5)-(2-7):

$$Q_{GD} = I_g \times t_{VF} \tag{2-5}$$

$$I_g = \frac{V_{DR}-V_{pl}}{R_g} \tag{2-6}$$

$$t_{VF} = Q_{GD} \times \frac{R_g}{V_{DR}-V_{pl}} \tag{2-7}$$

where the Q_{GD} is the charge required to change the gate-to-drain voltage down from blocking state to near zero.

Based on above analysis, the traditional method to calculate the turn-on loss can be summarized as equation (2-8):

$$E_{on} = \frac{V_{BUS} \times I_L}{2} \times (t_{VF} + t_{CR}) \tag{2-8}$$

In hard-switching converters especially in high switching frequency operation, the dynamic losses are the key to determine the efficiency and the key consideration of thermal design.

2.2.2 Traditional turn-off model

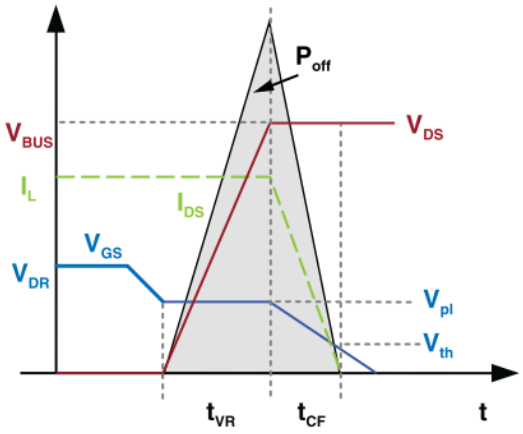


Figure 2. 5 Traditional turn-off transient

In the traditional method of estimating the turn-off loss of an enhancement-mode GaN HEMT, it is commonly accepted that the switching loss is caused during the overlapping region of device voltage and current as shown in Figure 2. 5 [1]. The initial state of the GaN HEMT is in on state with the load current flowing through the channel. The voltage across the transistor can be considered near zero. By applying an off control signal (usually 0V or -2 V/-3 V) between the gate electrode and the source electrode, the device starts to turn off. During the turn-off event, the drain-to-source voltage (V_{DS}) starts to increase when the gate-to-source voltage (V_{GS}) falls down to the miller plateau voltage (V_{pl}). After the voltage transition period (t_{VR}), the V_{GS} continues decreasing. When it reaches the threshold voltage (V_{th}), the drain current (I_{DS}) starts reducing from load current (I_L) to zero. This period is considered to be the transition-time of current (t_{CF}). The overlapping region includes both t_{VR} and t_{CF}, and the shaded area is considered to be the turn-off loss of the GaN transistor.

The equivalent circuit of GaN HEMT is also as in Figure 2. 4, but the gate current should be reversed. To calculate the turn-off switching loss of GaN devices, a flat miller plateau is assumed, which considers the plateau voltage (V_{pl}) to be a constant value. In voltage transition-time, the current that charges the internal gate-to-drain capacitor (C_{DG}) to DC bus voltage, which is also the reverse transfer capacitor (C_{rss}), can be considered to be equal to the current flowing through the gate electrode. Consequently, the voltage rise-time (t_{VR}) can be derived with (2-9) - (2-11):

$$Q_{GD} = I_g \times t_{VR} \tag{2-9}$$

$$I_g = \frac{V_{pl}}{R_g} \tag{2-10}$$

$$t_{VR} = Q_{GD} \times \frac{R_g}{V_{pl}} \tag{2-11}$$

where R_g represents the resistance in the gate loop for turn-off and the Q_{GD} is the charge required to change the drain-to-gate voltage from near zero to blocking state.

After this process, the gate current continues to discharge the gate-to-source capacitor (C_{GS}). The current fall-time (t_{CF}) can be derived as:

$$Q_{GS(pt)} = I_g \times t_{CF} \tag{2-12}$$

$$I_g = \frac{\frac{V_{pl}+V_{th}}{2}}{R_g} \tag{2-13}$$

$$t_{CF} = Q_{GS(pt)} \times \frac{R_g}{\frac{V_{th}+V_{pl}}{2}} \tag{2-14}$$

with $$Q_{GS(pt)} = Q_{GS} \times \frac{V_{pl}-V_{th}}{V_{pl}} \tag{2-15}$$

where Q_{GS} and $Q_{GS(pt)}$ is the charge required to increase V_{GS} from 0 to V_{pl} and from V_{th} to V_{pl} respectively.

Above all, the traditional method to calculate the turn-off loss can be summarized as equation (2-16):

$$E_{off} = \frac{V_{BUS} \times I_L}{2} \times (t_{VR} + t_{CF}) \tag{2-16}$$

2.3 Improved transient model

This section proposes an improved model which is computationally inexpensive and straightforward for turn-on and turn-off switching transients of GaN HEMTs in hard-switching topologies. The analytical results are compared with the simulation results from LTspice and the experimental results.

2.3.1 Proposed turn-on model

In the traditional method, it is obvious that the loss induced by the current overshoot is neglected, which in fact is a factor that should not be ignored when calculating the turn-on switching loss of GaN HEMTs. It is clear from [20] that the drain current in Silicon devices does not show an apparent overshoot when the device turns on, thus the process shown in Fig.1 can be used. However, since a superior characteristic that GaN HEMTs have over Silicon device is the much shorter rise time and fall time, the current needs to reach load current in a much smaller time interval. For example, the IGBT IKW30N60H3 manufactured by Infineon has a rise time of 33 ns and fall time of 22 ns [29]; while GaN HEMT GS66508 from GaN Systems has only a few nanoseconds for both rise and fall times [30]. Consequently, a current spike that cannot be ignored brought by displacement current happening during the transition period in GaN HEMT is much more severe than that in a silicon IGBT setup. This can also be observed in the double pulse test (DPT) simulation waveforms from LTspice as shown in Figure 2. 6. When the load current is set to be 30 A, at the turn-on commutation, the drain current goes up rapidly and reaches approximately 56 A then falls back to 30 A. When the current overshoot happens, the voltage across the device is still at a high level, thus, a significant estimation error will occur if the power dissipation due to the spike is not included.

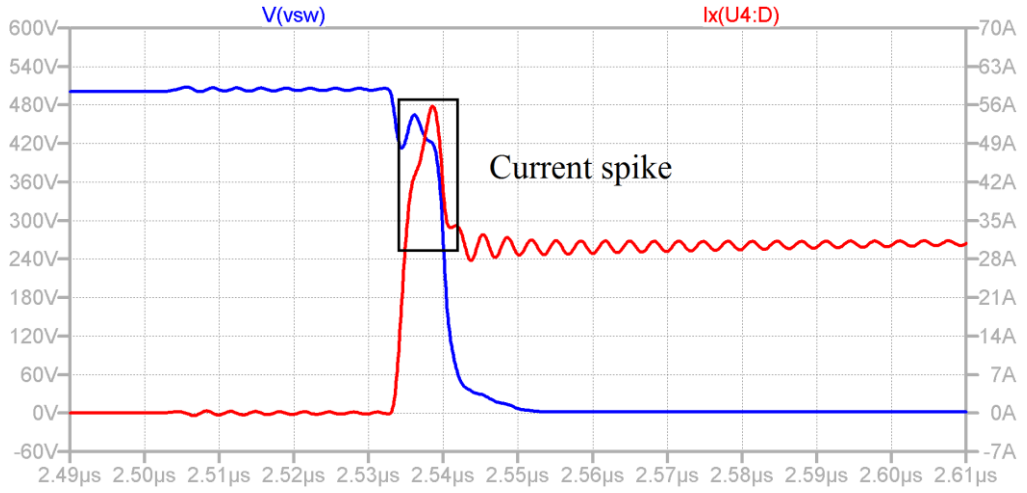


Figure 2. 6 Tun-on waveforms of DPT. V(vsw) is the drain-to-source voltage and Ix(U4:D) is the drain current.

The proposed transient analysis considers the current overshoot occurring at the current transition-time as shown in Figure 2.7. In fact, the current spike is led by the displacement current flowing in the bridge. Assuming the rise trend of current to be linear, the rising current in drain-to-source channel is composed of three parts: the average load current, and two displacement currents. In a half-bridge circuit, when the device under test (DUT) turns on, a discharging current flows through the output capacitor of DUT to bring the voltage cross the capacitor down from bus voltage to zero. Meanwhile, another displacement current also flows through the other device in the same bridge to charge the drain-to-source capacitor from zero to the blocking state [31]. To make it clear, one displacement current flows from DC bus to charge the output capacitor of the "turning-off" GaN device, while another one discharges the output capacitor of the "turning-on" GaN device. Then they merge with the load current in the drain channel leading to the current spike as shown in Figure 2.8. The time-independent extra losses due to the discharge of DUT and the charge of non-DUT are given by (2-9) and (2-10) respectively:

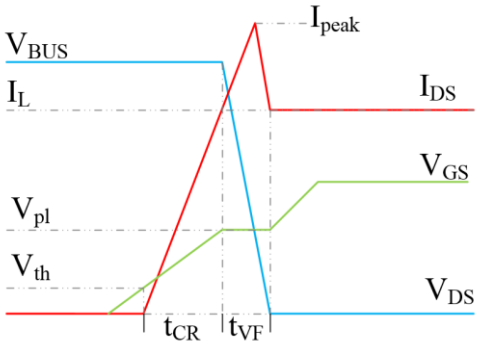


Figure 2. 7 Proposed turn-on transient

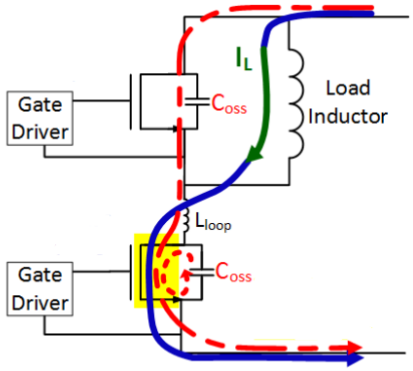


Figure 2. 8 Current components at turn-on

$$E_{C_{OSS\_DUT}} = \int_0^{V_{BUS}} C_{OSS} \times (V_{BUS} - v)dv \tag{2-9}$$

$$E_{C_{OSS\_non-DUT}} = \int_0^{V_{BUS}} C_{OSS} \times vdv \tag{2-10}$$

While the current bump in Figure 2. 7 is caused by the losses in (2-9) and (2-10) together, but usually when calculating the turn-off loss of non-DUT, the energy in (2-10) will be included. To avoid overrating the total loss, it should not be added into the turn-on switching loss.

Thus, the total turn-on energy can be described as:

$$E_{on} = \int_0^{t_{CR}+t_{VF}} v_{DS} \times i_{DS} dt - E_{C_{OSS}\_non-DUT} \quad (2\text{-}11)$$

One displacement current flows from the DC bus to charge the output capacitor of the "turning-off" GaN device, while another one discharges the output capacitor of the "turning-on" GaN device. Then they merge with the load current in the drain channel leading to the current spike. The peak value of displacement current can be estimated through the average current during interval t_{VF}:

$$I_{DS\_ave} = \frac{1}{2} * (I_{peak} - I_L) = \frac{2*Q_{oss}}{t_{VF}} \quad (2\text{-}12)$$

It is obvious from equation (2-11) that the accuracy of E_{on} is notably determined by the accuracy of transition time estimation and the energy caused by the output parasitics of the DUT.

2.3.2 Proposed turn-off model

In traditional topologies using Si IGBTs or MOSFETs, the freewheeling diodes take the responsibility of letting the current conduct in the reverse direction, and the turning-on process of the anti-parallel diodes makes slight difference to the total loss estimation. But for GaN-based converters, the characteristic of bi-directional conduction makes the switching-off event related to reverse turn-on event which happens in the meantime. In a half bridge, an obvious feature led by the topology itself is that, the voltages drops on the upper-side switch and the lower-side switch are always complementary. This means, if the upper-side device is supposed to turn-off, during this interval, two events are happening at the same time: The output capacitor of the upper-side switch is being charged while the corresponding capacitor of the lower-side device is being discharged. The sum of the blocking voltages of two capacitances should always equal to the DC bus voltage. From previous analysis, in section A, it is given by the traditional model that the turn-off speed is affected by the gate circuit design. However, it is usually neglected that the charging/discharging rate is also determined by the load condition. In practical situations, the time that the device needs to commute from on state to off is decided by the two factors mentioned according to different testing scenarios. For example, if the GaN transistors are turning off with a high DC bus voltage but low current, though the device can

commute in a few nanoseconds due to a low gate-off resistance design, the longer time needed by the other device in the same bridge to transfer from forward blocking mode to reverse conducting mode will drag the commutation speed down. Consequently, more transition time is needed to complete the full commutation. On the contrary, at low voltage but high load current, the output capacitance can be charged/discharged very quickly, then the gate loop would be the dominant factor which limits the commutation speed. In the traditional method, the transition time estimation are more adaptable for the low voltage, high current situations. However, it leads to a considerable deviation in high voltage, low current applications. In this section, the objective is to provide a more precise method to quantify the total switching-off time.

For convenience, the transition period happening within the freewheeling GaN transistor will be considered in this section. The mechanism is similar when applied to the turning on device but in the freewheeling device it can be seen more clearly as shown in the Figure 2. 9. With the symmetry of the lateral structure in GaN transistor [32], when the gate-to-drain voltage reaches the threshold voltage, the channel of the device turns on for reverse conduction. The displacement currents of i_{DS} offset the load current at the beginning thus the current flowing through the internal channel of the device is zero. The channel current increases with the dropping of the voltages on drain-to-source capacitance (output capacitance). When the channel current reaches load current (in reverse direction), the V_{DG} and V_{DS} reach near zero. This is when the device achieves full conducting in reverse conduction.

Based on the mechanism assumed above, the model for the reverse turn-on transient can

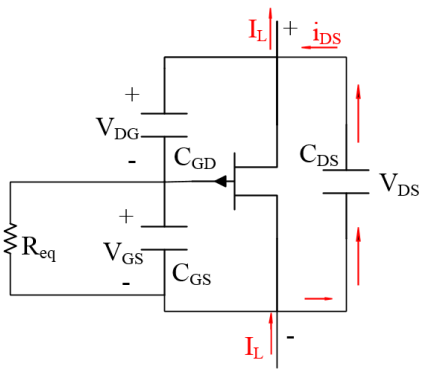


Figure 2. 9 Current path while reverse conducting

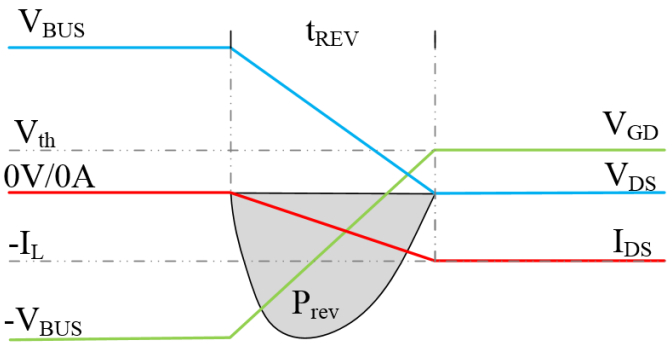


Figure 2. 10 Transient model for reverse conducting of the non-DUT

be built as in Figure 2. 10. The t_{REV} refers to the time needed to discharge the C_{DS} from blocking state to zero and it should be considered as the t_{VR} mentioned in the section A when the load causes a longer transition time. The transition time is determined by the time needed to fully discharge the C_{DS} (C_{OSS}) and external capacitor:

$$t_{REV} = \frac{-(Q_{OSS}+Q_{EX})}{I_{DS\_ave}} \tag{2-13}$$

Hypothetically, the current is supposed to increase linearly. It can be obtained as:

$$I_{DS\_ave} = \frac{-I_L}{2} \tag{2-14}$$

In summary, the real t_{VR} in equation (2-15) should be defined segmentally, which can be given by,

$$t^*_{VR} = \begin{cases} t_{VR}, & t_{VR} \geq t_{REV} \\ t_{REV}, & t_{VR} < t_{REV} \end{cases} \tag{2-15}$$

This is to claim that, the actual switching-off time should be influenced by both the gate circuit and the load condition. In other words, when a light load is carried, the longer t_{REV} induces a longer switching-off time. Conversely, at heavy load, the t_{VR} fixed by the gate loop defines the upper limit of the switching speed.

2.4 Accurate equivalent circuit parameters for loss calculation

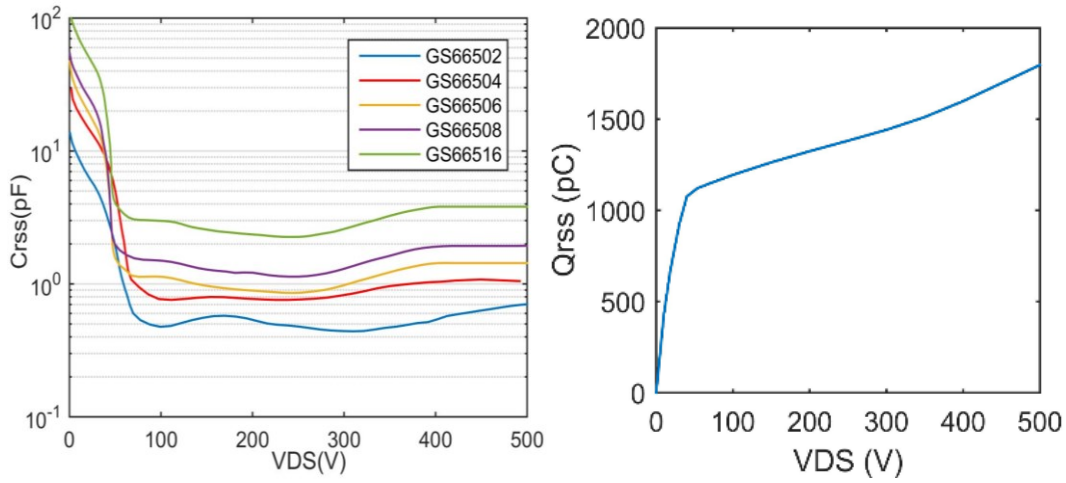
From the calculation of t_{CR} and t_{VF} using (2-1) ~ (2-4) and (2-5) ~ (2-7) respectively, it can be observed that the accuracy of the internal parameters of the device, such as Q_{GD}, Q_{DS} and V_{pl}, are of significance to obtain an accurate E_{on}. Therefore, the characteristics of the parameters will be explained in the following sections to obtain them precisely.

2.4.1 Reverse transfer capacitor and output capacitor characteristics

The accuracy of capacitance influences the transition time estimation considerably. For the switching losses of MOSFETs, the traditional method has been demonstrated in [22] which selects two values of C_{rss} at V_{DS}=V_{bus} and 0 V respectively and then the average value is used to estimate Q_{GD}. This assumption requires C_{rss} to be highly linear. However, for GaN HEMTs,

C_{rss} values varies nonlinearly when V_{DS} changes from 0 V to 500 V as shown in Figure 2.8 (a). Thus, the variation of C_{rss} must be taken into account for the accuracy of Q_{GD} (Q_{rss}). [25] has also put forward a method to calculate the switching time by means of calculating a group of small time intervals using a group of C_{rss}, then the combination of the time intervals is regarded as the transition time. However, this method brings bulky calculations since no standard formula can be clarified. To make the calculation more convenient, this chapter aims to find the linear relation between Q_{rss} and V_{DS}. Thus, this chapter proposes an improved method for calculating Q_{GD}.

Take GS66508T as an example, whose capacitance characteristics are shown in the Figure 2.9(a), the proposed method extracted numerous sampling points from the datasheet, and the



(a) (b)

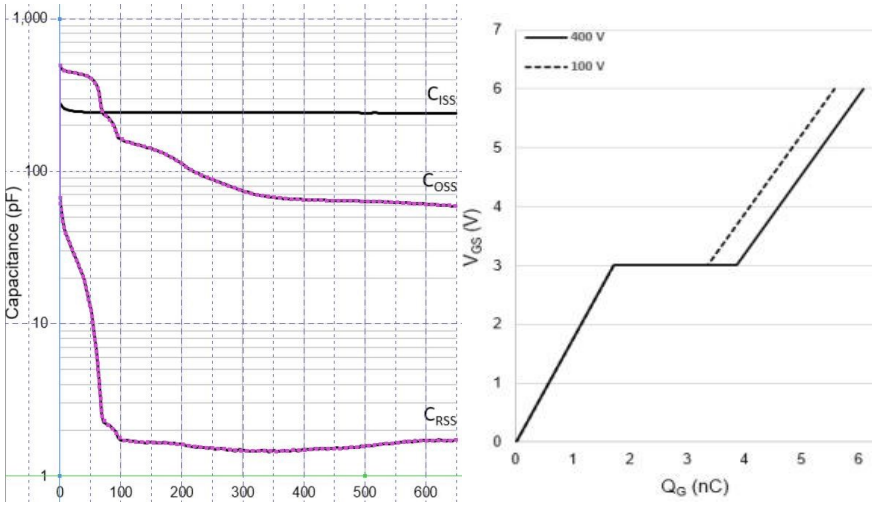
Figure 2. 11 Characteristics of GaN HEMTs. (a) Output capacitor. (b) Qrss.

sampling points are selected as closely as possible to make the scatter plot approximately identical to the original curve. Different distributing C_{rss} values are extracted to represent the reverse transfer capacitor at different voltage points. By integration, the Q_{GD} needed for different drain-to-source voltage levels can then be obtained. It is obvious that when the voltage level is above 100 V, the charge that the reverse transfer capacitor needs can be regarded as linear. Since 650 V GaN HEMTs are seldom utilized under 100 V, linear fitting the segment of voltage higher than 100V is sufficient for GaN HEMT switching loss estimation as in equation (2-16).

$$Q_{rss} = f(V_{BUS}) = K \times V_{BUS} \tag{2-16}$$

where K can be easily obtained by calculating the fitting slope of Q_{rss}-V_{DS} curve in Figure 2. 11(b). By selecting the Q_{rss} point from above function, the irregularity of capacitance can be eliminated, thus the subsequent calculation is facilitated.

Similar to Q_{rss}, Q_{DS} at different voltage levels can also be calculated through the integration method. Constant values of parasitic capacitors are also provided by the datasheet,



(a) (b)

Figure 2. 12 Characteristics of GS66508T. (a) Capacitance. (b) Gate charge.

but they are not representative enough since they are only for a specific test condition. The accuracy by means of integration and curve fitting is improved compared with traditional method and it contributes to the overall accuracy improvement in turn-on loss estimation.

As for the gate charge Q_{GS}, even though the datasheet also presents a gate charge characteristic curve as shown in Figure 2. 12 (b), it can be seen that a constant miller plateau is required to conform the curve. In fact, miller plateau shifting is another factor concerned in the proposed method, and it will be demonstrated in the next subsection.

2.4.2 Miller plateau voltage characteristics

Other than reverse transfer capacitor and output capacitor, the miller plateau voltage is also influenced by drain-to-source voltage and the load current. This phenomenon has also been mentioned in [33]. However, this varying factor is not included in the traditional loss estimation. Basically, V_{pl} increases with the increase of V_{DS} and I_L. The datasheet [30] does not mention the miller plateau voltage shifting with changes in V_{DS} and I_L in detail, but it can be

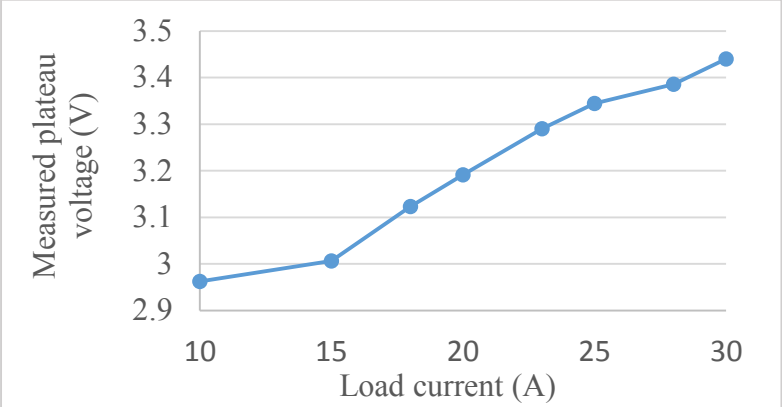


Figure 2. 13 Miller plateau shifting at V_{DS}=400 V

observed in the simulation software as recorded in Table 2.1. It can be seen that the difference among plateau voltage can reach about 0.6 volt when the operating condition changes from V_{DS}=200 V, I_L=10 A to V_{DS}=500 V, I_L=30 A. Figure 2. 13 also shows the miller plateau shifting with varying load current at V_{DS}=400 V. As a result, the turn-on characterization of GaN HMETs varies. Based on (2-1) and (2-2), as can be seen that a higher plateau voltage causes longer voltage transition-time because the turn-on gate current I_g gets reduced. Furthermore, higher plateau voltage also causes longer current transition-time because the charge required to reach the miller plateau $Q_{GS(pt)}$ also increases.

These two factors will be combined to calculate a more precise Q_{GD} and thus the accuracy of the estimation of transition-time will be improved. Consequently, switching loss can be assessed with lower error with the proposed method.

Table 2. 1 Miller plateau voltage

I_L(A) \ V_{DS}(V)	200	250	300	350	400	450	500
10	2.8721	2.9277	2.9416	2.9630	2.9626	2.9121	3.9832
20	3.1514	3.1742	3.2149	3.1737	3.1911	3.2098	3.2331
30	3.3931	3.4230	3.4334	3.4592	3.4340	3.4525	3.4760

2.5 Calculation and simulation results

The parameters for analytical calculations and DPT simulations through LTspice are listed in Table 2.2. The junction temperature of GaN HEMT is considered to be the same as ambient temperature, which is 25 °C. Different voltage and current levels are selected, and corresponding miller plateau voltage values obtained from Table 2.1 are used in the calculation. Q_{rss} is selected from Figure 2. 11 based on the operating conditions and Q_{GS} is also calculated in a similar way. Since Q_{GS} varies slightly under different circumstance when the bus voltage is above 200 V, Q_{GS} for charging the gate voltage from zero to 6 V is considered constant and selected from the datasheet to be 1.7 nC. The t_{VF}+t_{CR} are calculated. Corresponding values are measured from the simulation directly and are compared.

Table 2. 2 Simulation parameters

Junction temperature	25 ℃
V_{BUS}(V)	300/350/400/450/500
I_L(A)	10/20/30
V_{DR}(V)	+6/0
V_{th}(V)	+1.7
R_g(ohm)	10
Q_{GS}(nC)	1.7

Table 2. 3 Calculation by traditional method without capacitance fitting

	10A	20A	30A
	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)
300	28.57130309	28.57130309	28.57130309
350	33.34862755	33.34862755	33.34862755
400	38.15925419	38.15925419	38.15925419
450	42.82719403	42.82719403	42.82719403
500	47.47907193	47.47907193	47.47907193

Table 2. 4 Calculation by traditional method with capacitance fitting without miller plateau shifting

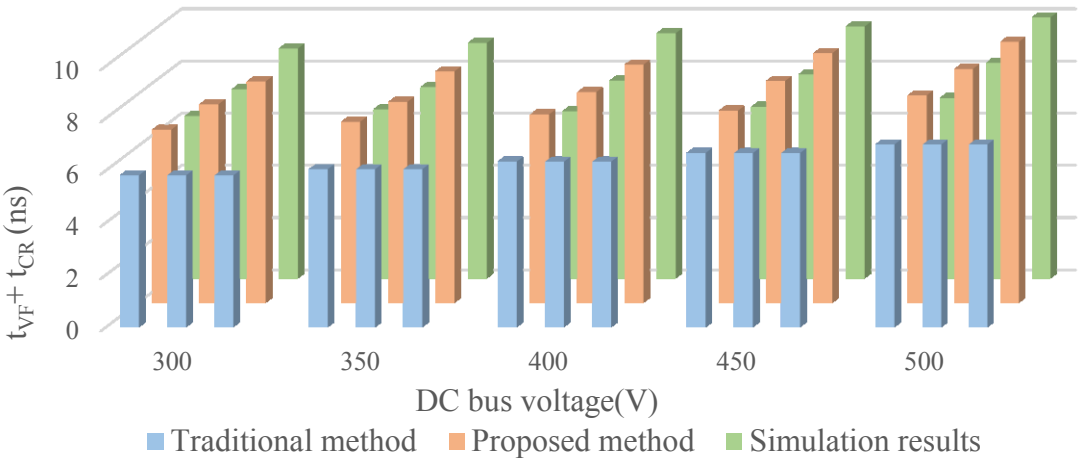
	10A	20A	30A
	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)
300	5.815799087	5.815799087	5.815799087
350	6.049465753	6.049465753	6.049465753
400	6.340465753	6.340465753	6.340465753
450	6.669799087	6.669799087	6.669799087
500	7.000799087	7.000799087	7.000799087

Table 2. 5 Calculation by proposed method considering miller plateau shifting

	10A	20A	30A
	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)
300	6.277524194	6.929992578	7.565997389
350	6.648172046	7.456797475	8.085763711
400	7.033769633	7.87092845	8.812810083
450	7.437613387	8.306769878	8.992118771
500	7.82536583	8.710865325	9.529679691

Table 2. 6 DPT simulation result

	10A	20A	30A
	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)	t_{VF}+ t_{CR}(ns)
300	6.219317	7.242873	8.807158
350	6.471781	7.329043	9.017354
400	6.396774	7.57279	9.292411
450	6.569867	7.81487	9.651914
500	6.901262	8.2561	9.735659



**For every series of voltage level, three different current conditions (10A,20A,30A) are presented from left to right.*

Figure 2. 14 Comparison among calculation and simulation results

Comparing Table 2.3 with Table 2.6, it is clear that the total transition time calculated by traditional method for Silicon MOSFETs is not suitable for switching loss calculation of GaN HEMTs due to the low accuracy. This is because, as has been mentioned in last chapter, the capacitance selection has great influence on the calculation accuracy. From Table 2.3 and Table 2.4, it should be noticed that for the same bus voltage, the transition time is the same. This phenomenon can be explained by equations (2.1) – (2.7): when V_{DR}, V_{th}, R_g and Q_{GS} are fixed, then $Q_{GS(pt)}$ and I_g are fixed at the same bus voltage level thus t_{CR} remains constant. On the other hand, because Q_{GD} depends on V_{bus} only, leading to a constant t_{VF} which does not conform the practical situation. Consequently, the proposed method considers the impact of a variable miller plateau voltage as shown in Table 2.5 and smaller difference is shown when compared with simulation results presented in Table 2.6.

At the condition of 10 A load current and bus voltage from 400~500 V, the transition time calculation by the traditional method shows closer agreement with the circuit simulation results. However, the final switching energy calculated and compared in Table 2.7 (The traditional method mentioned in the table and in the following section considers capacitance fitting but without miller plateau shifting), is still not accurate because of ignoring the current overshoot.

Table 2. 7 Turn-on loss estimation comparison with simulations

10A	Traditional Method (μJ)	Proposed Method (μJ)	Simulation Result (μJ)
400V	12.681	40.618	64.358
450V	15.007	48.622	67.439
500V	17.502	54.997	71.091

Summarized results at different load currents and bus voltage levels are shown in Figure 2. 15, which indicate that the proposed method gives more accurate estimation of turn-on switching loss for GaN HEMTs.

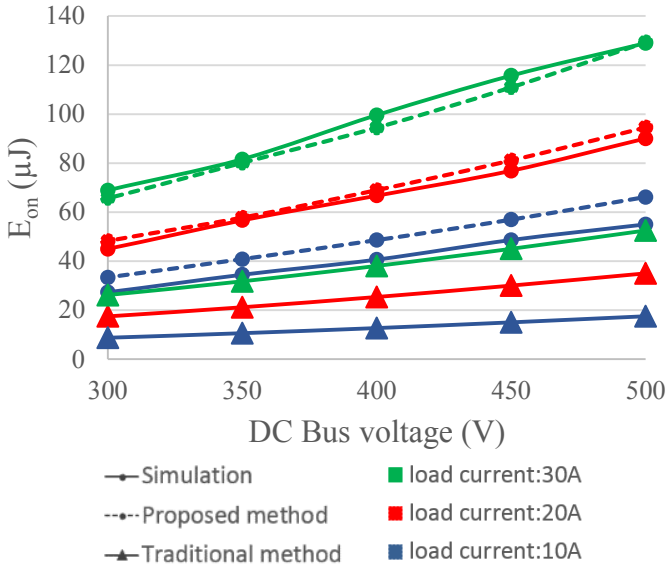


Figure 2. 15 Comparison between simulation and estimation

The results for the proposed turn-off model are presented as in Figure 2. 16. The calculation process also takes the capacitance curve fitting and plateau shifting into consideration. The red curve stands for the turn-off time obtained from the simulation at the testing condition of V_{BUS}=100 V and I_L ranging from 10 A to 60 A. It can be seen that, the t_{VR} calculated from equation (2-11) only conforms the simulation results when the load current is greater than around 36 A, while at lower current, the t_{REV} from equation (2-13) provides a better accuracy. This is because, at a given DC bus voltage, when the load current is at a low level, though the turn-off gate resistance is one of the limit which decides the turn-off time, the time needed for the output capacitance to switch from one state to another makes the transition

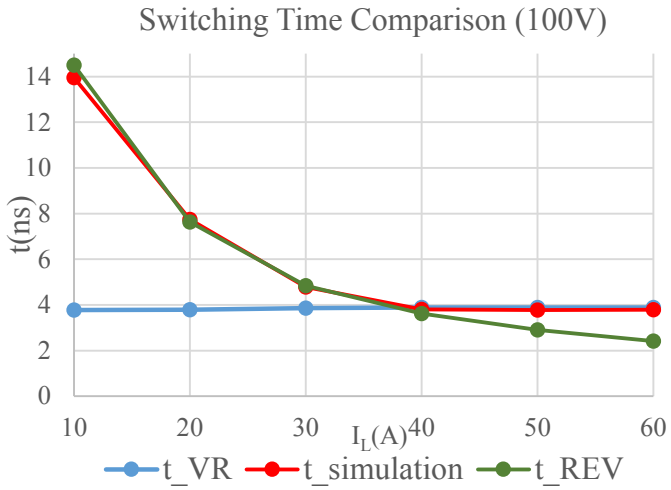


Figure 2. 16 Comparison between simulation and estimation of turn-off model

process longer. But at high current, how the gate loop is designed becomes the constraint of the switching speed. Figure 2.16 has validated that, the actual transition time at switching-off event should be determined by both gate loop and power loop, as concluded in equation (2-15).

2.6 Experimental results

2.6.1 Double pulse test experiment

The double pulse test is performed for capturing the switching transition waveforms of the voltage and current. Three-phase GaN inverter HGCB-6B-401120 manufactured by Headspring Inc. is used to conduct the test. The test circuit and experimental setup are shown

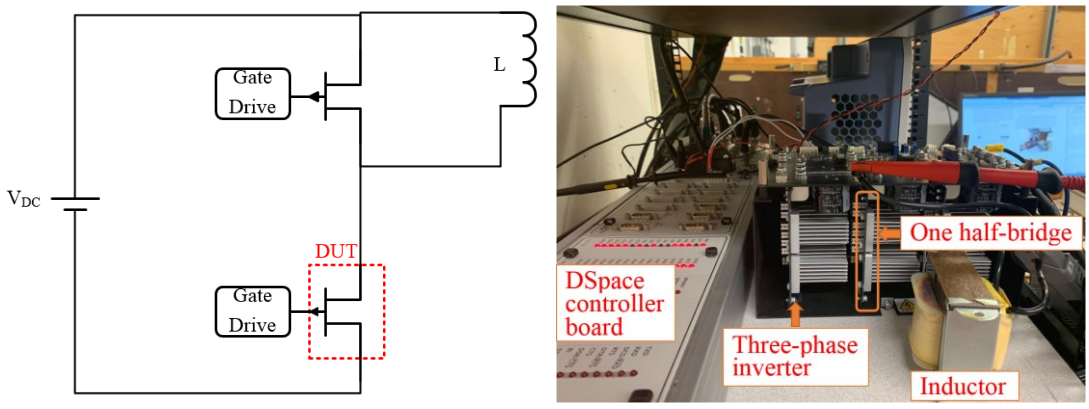
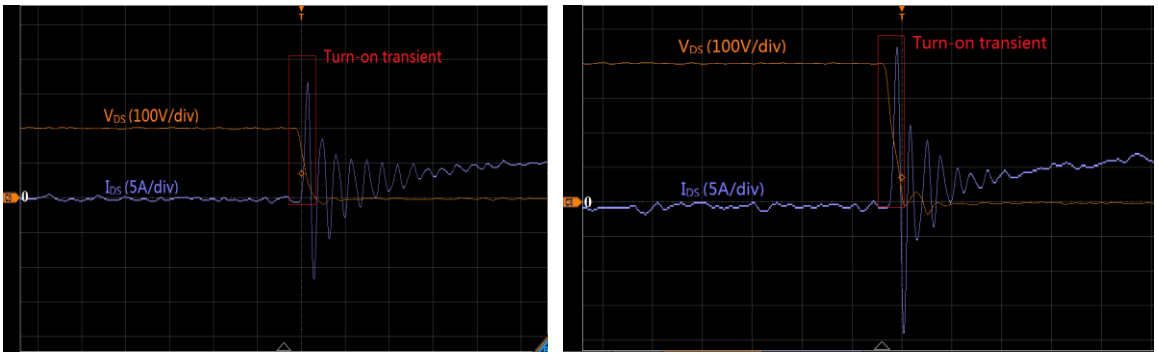


Figure 2. 17 DPT experiment. (a) The circuit. (b) Hardware setup.

in Figure 2. 17. The inverter is built with GS66508B GaN E-HEMT by GaN Systems. GS66508B has similar features as GS66508T, and the difference between them is that GS66508B is bottom cooled. Since only one half-bridge is needed for the double pulse test, one of the three bridges in the inverter is selected to build the circuit. The gating signals are generated by dSpace simulator and insulated from the main circuit. The heat sink and cooling fan are already installed properly in the inverter, and consequently the impact of temperature on switching losses can be neglected within a short period of time during the test.

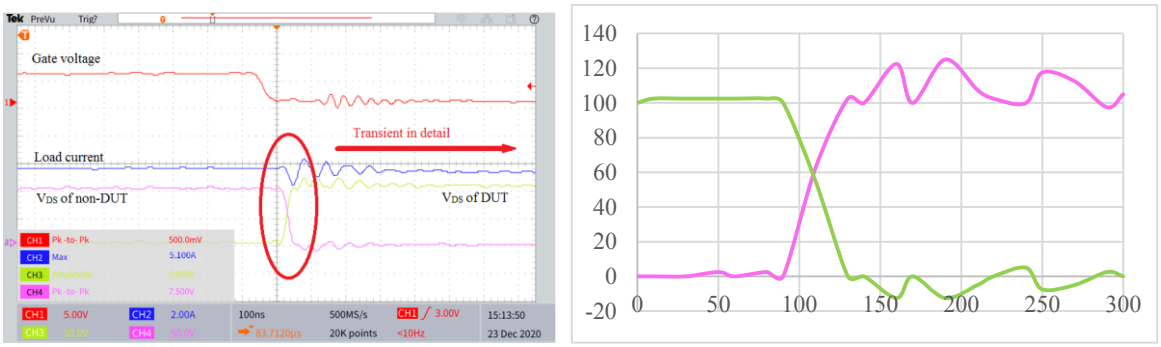
In the double pulse test, the switching-on transient process during the second gate-on pulse is focused since the first gate-on pulse given to the DUT is used to charge the inductor current to 5 A. Thus, the switching-on loss measured during the first gating-on interval does not include the energy contributed by the load current. When the gate-off signal is given on the DUT, which is the low-side switch, the up-side switch will be turned on after the dead time which is set to be 30ns in the experiment. In this interval, the energy stored in the inductor in the previous stage is releasing and the current is circulating through the up-side switch and the load. The current in the low-side switch reduces to zero at this stage. Then the second gate-on pulse will be generated to turn on the DUT again at the switching condition of V_{DS}=200 V/400 V while I_{DS} keeps at 5 A since the reduction in the inductor current is small and can be ignored. In this period, the waveforms of voltage and current are recorded to show the transient process.

The experimental waveforms based on double pulse test are shown in Figure 2. 18. It can be noticed that there is an obvious ringing on current existing at the beginning stage of turning on due to the parasitic stray inductance of the DC bus and the half-bridge module, which leads

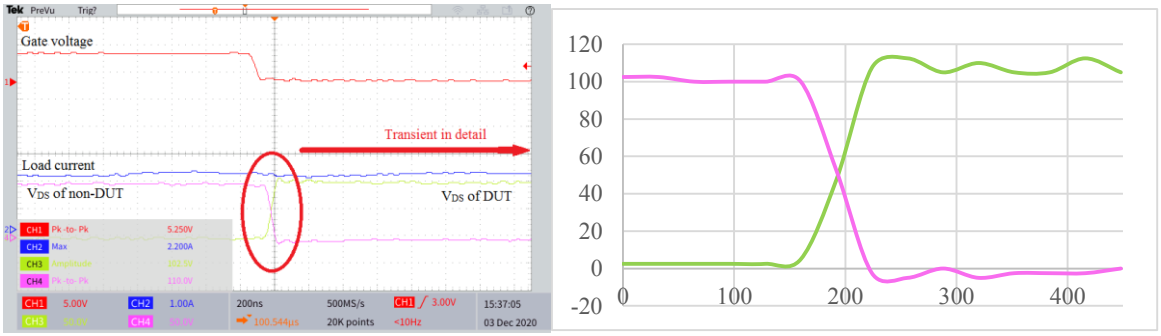


(a) (b)

Figure 2. 18 Turn-on transient waveforms of current and voltage. (a) At V_{DC}=200 V, I_{DS}=5 A. (b) At V_{DC}=400 V, I_{DS}=5 A



(a)



(b)

Figure 2. 19 Turn-off voltage transient waveforms of both switches. (a) At V_{DC}=100 V, I_{DS}=2 A. (b) At V_{DC}=100 V, I_{DS}=5 A

to higher losses than the ideal situation. But the first spike of rising current contributes the most and it includes the extra loss induced by the displacement current as has been discussed in the previous section. After the first overshoot of current, even though the ringing on the current is still happening, the voltage cross the GaN device has decreased to nearly zero thus the subsequent losses caused by the rest of the current ringing only have a trivial impact on the switching-on loss estimation. It can be seen that the tendency of the waveforms are consistent with the proposed turn-on transient model.

The turn-off transient is shown in Figure 2. 19. It can be concluded that the load condition does have an influence on the switching speed of GaN devices. At V_{BUS}=100 V and I_L=5 A, the turn-off switching time is around 32ns. When the load current is 2 A and the same DC bus voltage, the turn-off transient takes a longer time which is around 80ns. Compared with the calculation results based on the proposed turn-off model, which are 29 ns and 72.5 ns respectively, the error is within a small range. The error can be introduced by the parasitic components among the PCB traces and the parasitic capacitance induced by external load,

which can also make the charging and discharging process longer. This is because, when external capacitance are introduced into the circuit, it can be regarded that the output parasitic capacitance of the GaN device increases. Thus, in real situations, the turn-off time can be even longer due to the degradation of the load.

2.6.2 Results and discussion

Based on the same test condition of the double pulse test experiment, the calculation according to the traditional method and proposed method is performed and the comparative results are shown in Table 2.8 and Table 2. 9. It is obvious that the proposed method can provide a more accurate switching transient model than the tradition method. Since the stray inductance in the hardware is not taken into consideration, the results obtained from the experiment are greater than the calculated ones.

Table 2. 8 Turn-on loss estimation compared with experiments

5A	Traditional Method (μJ)	Proposed Method (μJ)	Experimental Result (μJ)
200V	2.713	14.019	19.921
400V	6.340	37.491	44.037

Table 2. 9 Turn-off time estimation compared with experiments

100V	Proposed Model (ns)	Experimental Result (ns)
5A	29	32
2A	72.5	80

Another implication is that, during the interval of reverse turn-on channel's building, due to the parasitic elements existing in the circuit, such as parasitic capacitance of the external load, a longer time is needed for the switches to achieve the fully-off state. In this chapter, the parasitic capacitances existing in the PCB is not included because they can be neglected compared to the capacitance introduced by the load. But in some other situations, where the capacitance effect is considerable, it should also be included. This also means that the designers

should be careful when design the layout of the power loop, since a capacitance effect needs to be kept as small as possible to help the GaN HEMT develop its potential of high switching speed.

2.7 Summary

This chapter puts forward an improved switching transient model for GaN HEMTs in hard switching topology. The proposed turn-on model considers current spikes and the turn-off model considers not only gate loop design, but also the load condition. In comparison with the traditional estimation method for Silicon transistors, the proposed switching loss which improves the switching time estimation is more reliable and accurate for GaN devices. In order to verify the results obtained from the proposed model, a double pulse test circuit is implemented with LTspice and hardware. It is validated in both simulation and experiment that the proposed method can provide closer switching time estimation than the traditional method by considering different features of GaN semiconductors, including the reverse transfer capacitance, output capacitance, and miller plateau voltage shifting. Therefore, the estimation accuracy of turn-on switching loss in GaN HEMTs is improved by the proposed method. In addition, the proposed estimation method can be applied for total switching loss calculations in different GaN HEMTs power converter applications. Moreover, the turn-off model can also contribute to the minimum dead-time setting to help reduce the dead-time loss.

CHAPTER 3 DESIGN OF A GAN-BASED THREE PHASE INVERTER

3.1 Introduction

After a few decades of development, GaN transistors have been accepted in the market and recognized to be promising which can stimulate the progress of industries and researches. Modern GaN transistors now compete with Si and SiC semiconductors and have been proved to perform well as a new generation of power electronic devices [2]-[6]. As a promising semiconductor material, the wide band-gap (WBG) material GaN has a wider band gap (more than 3.4 eV), higher critical breakdown electric field, higher anti-radiation ability and higher electronic saturation velocity [34]-[38]. In motor drive applications, low losses and high switching frequency is of significance when it comes to increasing the power density and the compactness of the system [39]. The improved pulse-width modulation (PWM) switching frequency can enable a reduction not only in motor current ripple, noise and losses in AC motors but also on the volume of passive components such as an LC filter which helps to provide ideal sinusoidal output waveforms. All the above advantages put together improves the overall efficiency of the system [40]-[41].

A reliable gate drive circuit design for the high power GaN based inverter must be achieved due to its demanding requirements on the gate voltage. Many designs of three-phase inverters have applied complicated gate drive circuits which are costly and equipped with excessive components which may also increase the gate loop parasitic inductance due to the equivalent series inductance (ESL) existing in the elements. In a half-bridge structure, which is a fundamental topology employed in different power converters, such as an inverter, a bootstrapping circuit is a simple and low cost solution has been widely used to supply the voltage required by the high-side transistor [42]-[43]. Some companies such as EPC, Navitas, and Power Integrations are committed to monolithic integration of GaN HEMTs, drivers, and logic circuits, but this kind of solution has high cost and complexity, also limited design flexibility.

3.2 Review of GaN power transistors and packaging technologies

Nowadays, there are many GaN transistors which are suitable for power conversion application commercially available from several vendors with blocking voltage up to 1,200 V (VisIC Technologies 2018) and current handling capability up to 120 A (GaN Systems 2018). In order to pick the best GaN power transistors for this 10 kW high power density inverter design, a comprehensive survey on existing GaN power transistors performance and their corresponding package technologies is conducted in order to compare the electrical capabilities. Table 3.1 shows the datasheet parameters comparison of dominant GaN devices from different manufacturers the blocking voltage above 600 V and current ratings more than 25 A. GaN Systems provide two product series of 650 V and 100 V blocking voltages. The latest 650 V/120 A GaN transistor is available for online order in 2018 in a bare die package on the GaN Systems' official website("GS-065-120-1-D" 2019). The SMT package transistors from GaN Systems (650 V/60 A) are available with both top and bottom side cooling. VisIC recently released its 1200 V level half-bridge module with gate driver and sensors in a compact size of 73mm*43mm*20mm which is the only half bridge module in this voltage range ("VM40HB120D-Ver1.20.Pdf" 2018). In addition to what have been listed, no one would neglect the Efficient Power Conversion (EPC) in the GaN HEMT area who is the first mature producer of E-mode GaN transistors and has a full series of products commercially available with current range from 0.5 A to 90 A and a blocking voltage up to 200 V. Among all the GaN devices introduced in this chapter, most of them utilize surface mount technology (SMT) except Transphorm which provides through hole TO package ("Transphorm GaN Power FET Portfolio" 2018).

Table 3. 1 Datasheet comparison of GaN devices commercially available from different manufacturers

Company	Part number	Operation mode	Mounting Style	Blocking voltage at 25°C	Continuous current at 25°C (A)	Rise time and turn ON delay (ns)	Fall time and turn OFF delay (ns)	R_{on} (mΩ)	Gate Charge (nC)	Reverse recovery charge (nC)
GaN Systems	GS66508B/P/T	Normally OFF	Surface Mounting	650	30	3.7+4.1	5.2+8	50	5.8	0
	GS66516B/T	Normally OFF	Surface Mounting	650	60	4.6+12.4	14.9+22	25	12.1	0
	GS-065-120-1-D	Normally OFF	Bare Die	650	120	NA	NA	12	25	0
VisIC	V18G65A	Normally ON	Surface Mounting	650	53	7.5+2	4.5+36	18	15	0
	V22N65A	Normally OFF	Surface Mounting	650	80	6.5+9	10.8+15.5	22	41	0
Trans-phorm	TPH3212PS	Normally OFF (cascode)	Through Hole	650	27	7.5+24	5+55.5	72	14.6	90
	TPH3205WSBQ	Normally OFF (cascode)	Through Hole	650	35	7.6+36	8.6+40	49	28	136
	TP65H050WS	Normally OFF (cascode)	Through Hole	650	36	11+51	11+86	50	16	125
	TP65H035WS	Normally OFF (cascode)	Through Hole	650	46.5	69+13.5	98.5+11.5	35	24	178
Pana-sonic	PGA26E07BA	Normally OFF	Surface Mounting	600	26	5.6+3.7	2.4+5.5	56	5	0
Infineon	IGO60R070D1/IGOT60R07	Normally OFF	Surface Mounting	600	31	9+15	13+15	55	5.8	0

The survey shows that the GaN System device (GS66516 series) is the most suitable discrete device among all other devices for a high power high density inverter. According to GaN Systems, their die fabrication technology makes the GaN HEMT die area highly scalable. This makes GaN Systems the first company to provide a 650 V discrete GaN device with 60 A current rating. In addition, the laminated SMD package used by GaN System offers ultra-low package inductance and top side cooling at the same time. Without paralleling multiple GaN devices, GS66516 series can achieve high current rating directly. Thus, the power density and

reliability of the inverter can be improved.

3.3 Major components selection

A three-phase inverter system can be roughly divided into three parts: Three-phase inverter, gate drive circuit and power supplies.

3.3.1 Three-phase inverter

The power transistors and the DC-link capacitor are the two major components of the inverter part. According to the survey demonstrated in last section, the GaN HEMT GS66516 series manufactured by GaN Systems is specifically selected in the design.

a) Power transistors

In general, the commercially available GaN HEMTs in the market can be classified into three types in accordance with heat dissipation: Top-side cooling, bottom-side cooling and double-sided cooling [44]-[45]. The thermal pad of top-side cooling GaN transistors is located on the top side and connected together with the source electrode which is on the bottom side. This enables the thermal pad of the device to be attached to the external heatsink directly. It should be noticed that a layer of interface material with High Voltage (HV) insulation should be placed between the thermal pad and the heatsink to improve the heat transfer performance and to avoid short circuits. In comparison, the bottom-side cooled transistor has its substrate located at the bottom side which requires the heat dissipation path to go through the FR4 PCB board using thermal vias beneath the device. However, the PCB area beneath the device is usually used as the current commutation loop as well. This causes a conflict between the heat dissipation and the current flowing path and limits the performance of electrical circuit dramatically. This conflict can be reflected in the example layout presented in [46] where it is difficult to satisfy both the thermal performance and the electrical performance at the same time with numerous thermal vias placed under the device. The double-sided cooling package GaN has around 30%~35% smaller thermal resistance compared to the single-sided cooling

package [45],[47]. However, it is challenging to balance the raised requirements of cooling design and the complexity of the system [48]. Thus, based on the survey above and considering the heat dissipation design, GS66516T is selected as the active switch used in the inverter design. According to GaN Systems, their GaNPX® packaging technology enables low inductance (less than 1nH) and low junction to case thermal resistance (0.2 ^{o}C/W) in a small package size. This makes GS66516T the first 650 V discrete GaN device with a high current rating of 60 A. Avoiding the difficulty of paralleling multiple devices to achieve high current [49]-[50], GS66516T allows at least 30 A ac operation.

b) DC-link capacitor

For three phase inverters, the DC-link capacitor is a critical passive component that requires relatively larger space with stringent requirements on the AC current rating and dc voltage ripple. In Figure 3.1, a typical circuit diagram of a voltage source fed three-phase inverter (VSI) connected to a dc bus voltage V_{in} is shown. The inverter drives an AC motor with three sinusoidal output currents. Six GaN switches are controlled to turn on and off by a Pulse Width Modulation (PWM) strategy to generate sinusoidal output voltage waveforms. The current of the three phases varies with the phase voltages based on load which is an ac motor in this situation.

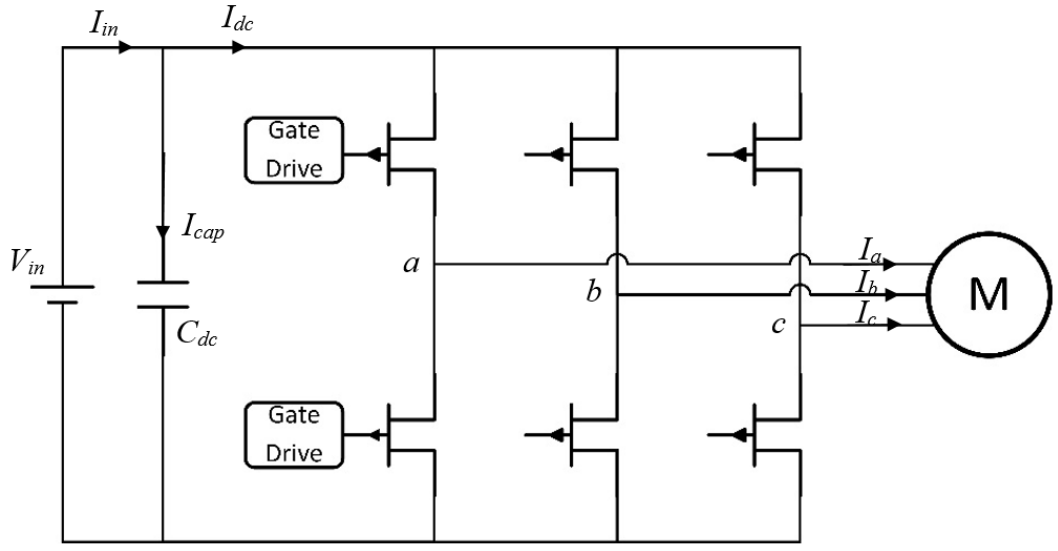


Figure 3. 1 Circuit diagram of a VSI system

In a VSI, the main functions of the DC-link capacitor is to [51]-[52]:

(1) Provide a low impedance path for high frequency currents: With frequency increasing, the existing inductive parasitic impedance in the power supply and cable also increases. On the contrary, the DC link capacitor impedance goes down so the high frequency components of AC current (ripple current) can be absorbed.

(2) Stiffen the DC bus: Remove the effects of stray inductance from the DC voltage source to the main power bridges so as to have a stable DC bus. Voltage fluctuation on the DC bus brings ripple to the output current which should be avoided.

As for the type of the capacitor, film capacitors have high ripple current rating and low ESR and ESL compared with electrolytic capacitors. Though electrolytic capacitors have higher capacitance/volume ratio than film ones, the ESR and ESL of electrolytic capacitors are higher than those of film capacitors so multiple electrolytics need to be connected in parallel to reduce the parasitic parameters, and that may increase the size of the inverter and reduce the power density which weaken the advantage of GaN-based systems. The volumetric efficiency typically ends up being much higher if film capacitors are used. On the other hand, the working lifetime rating of film capacitors is around 10 times of electrolytics [53]. Consequently, a film capacitor will be selected. Thus, when selecting the DC-link capacitor, the ripple current is an important factor [53]-[54].

The rms value of the inverter input current can be divided into two parts (dc and ac component) and calculated as:

$$I_{rms}^2 = I_{ac\_rms}^2 + I_{dc}^2 \tag{3-1}$$

The ac component will be absorbed by the DC-link capacitor thus the rms value of the capacitor current can be derived:

$$I_{C,rms}^2 = \sqrt{I_{rms}^2 - I_{dc}^2} \tag{3-2}$$

Reference [55] and [56] have presented a concrete analysis and derivation to determine the inverter rms and average value current:

$$I_{rms} = \frac{I_m}{\sqrt{2}} \times \sqrt{\frac{2\sqrt{3}}{\pi} \mathrm{M}(\frac{1}{4} + \cos^2 \varphi)} \tag{3-3}$$

$$I_{dc} = \frac{3}{4} M I_m \cos \varphi \tag{3-4}$$

Substituting (3-3) and (3-4) into (3-2):

$$I_{C,rms} = I_{N,rms}\sqrt{2\mathrm{M}[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M)]} \quad (3\text{-}5)$$

Where M is the modulation index; I_m is the peak value of the phase current; cosφ is the power factor; and φ the angle between the current and voltage vectors; $I_{N,rms}$ is the rms value of phase current. Figure 3.2 plots the normalized capacitor current to phase current vs. modulation index for several different power factors.

Most Permanent Magnet (PM) motors have power factors between 0.70 and 0.95. It is obvious that maximum capacitor current occurs when the M is between 0.6-0.75 where the capacitor current will be 0.55-0.65 times of the phase current.

Thus, the DC-link capacitor can be sized as:

$$C_{DC\_min} = \frac{I_{C,rms}}{\Delta V \times 2\pi f_{sw}} \quad (3\text{-}6)$$

Where ΔV is the ripple voltage allowed [57]. In this design, a 700 V, 160 μF capacitor is selected.

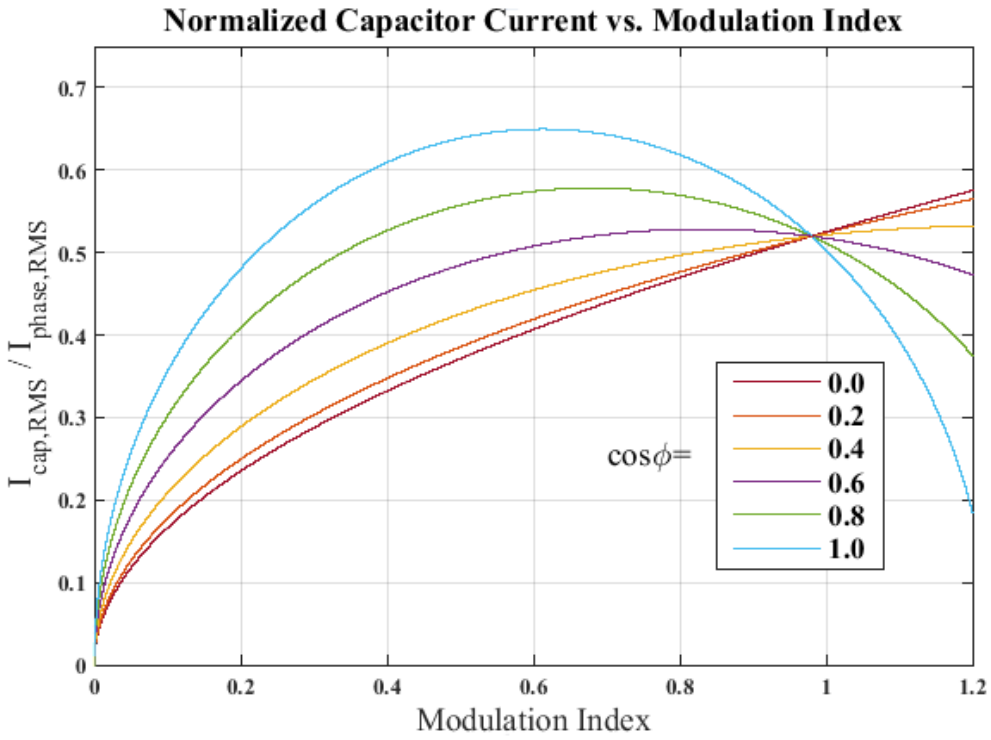


Figure 3. 2 Capacitor current normalized to phase current vs modulation index for power factors from 0 - 1.0

3.3.2 Gate drive circuit

a) Bootstrap topology

In a half-bridge structure, which is a fundamental topology employed in different power converter, such as an inverter, a bootstrap circuit is widely used to supply the voltage required by the high-side transistor [58]-[59]. In the design, a bootstrap circuit as shown in the Figure 3.3 is used to form the gate drive circuit to increase the simplicity and compactness of the circuit because it generates isolated power supplies for high-side and low-side GaN switches, which can help to reduce cost and avoid additional parasitic capacitance between the switching output and ground. The red-marked part in the Figure 3.3 indicates how the DC power supply is directly connected to low side gate driver and supplies to high side gate driver through the

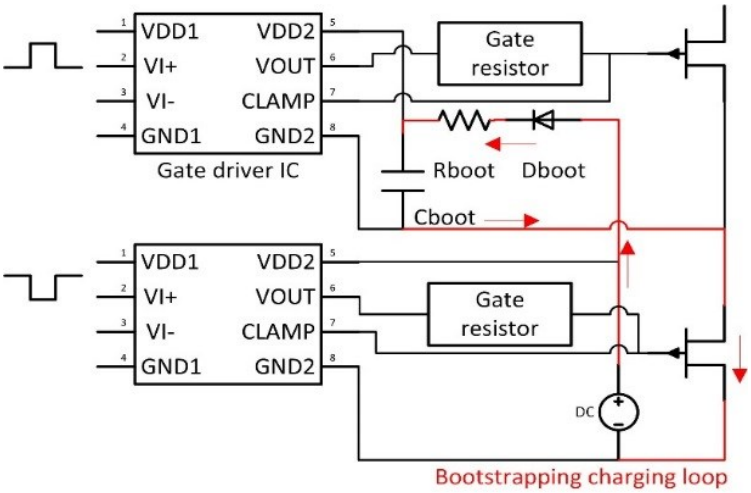


Figure 3. 3 Gate drive circuit for a single phase

bootstrap capacitor. It can be seen that, when the high side GaN HEMT is in the off state and the low side switch is on, the external DC supply charges the bootstrap capacitor (C_{boot}) through a diode (D_{boot}), a bootstrap resistor (R_{boot}) and the conducting low-side switch. When the high side GaN HEMT turns on and the low-side switch turns off, D_{boot} becomes reverse biased thus the bootstrap capacitor can supply VDD2 of the high side gate driver IC.

For the gate driver IC, the ADUM4121 manufactured by Analog Devices is used, which provides 5 kV rms isolation in the wide-body, 8-lead SOIC package and offers the advantage of true, galvanic isolation between the input and the output. With a range from 2.5 V to 6.5 V

supply at the input side, it can generate a 6 V supply at the output side to fit the turn-on gate drive voltage requirement of GaN HEMTs. The ADUM4121 gate driver also includes an internal Miller clamp which activates at 2 V on the falling edge of the output, supplying the gate with a low impedance path to reduce the risk of false turn on induced by miller effect [60].

To select the bootstrap capacitor, Silicon Labs Company has provided a convenient website to do the calculation [61].

The maximum total charge needed by the high-side gate (Q_{CB}) should be calculated first to ensure after maximum voltage drop the gate voltage can still keep the high-side switch in on state:

$$Q_{CB} = Q_G + (t_{Loff\_max} \times I_{DD2\_Q}) \tag{3-7}$$

Where Q_G is the total gate charge needed by the GaN HEMT and (see GaN HEMT datasheet); t_{Loff_max} represents the maximum time during each cycle that the low side switch is off; I_{DD2_Q} is the maximum quiescent input current for the high side driver (see driver IC datasheet).

The maximum voltage drop (Vboot) depends on the threshold gate drive voltage (Vth):

$$V_{boot} = V_{DC} - V_D - V_{th} \tag{3-8}$$

Where V_D is the forward voltage drop of the diode.

The value of C_{boot} is driven by the maximum allowable ripple of V_{boot}:

$$C_{boot} = \frac{Q_{CB}}{\Delta V_{boot}} \tag{3-9}$$

The purpose of R_{boot} is to limit the current in the first cycle at startup and to ensure the bootstrap capacitor can be properly refreshed during the worst case during low-side switch on time. The time constant of the RC circuit is R_{boot} x C_{boot}. As a starting point, it is suggested that resistor R_{boot} be selected such that minimum time that low side switch is on (t_{Lon_min}) is at least three times of the time constant.

$$R_{boot} \leq \frac{t_{Lon\_min}}{3 \times C_{boot}} \tag{3-10}$$

For the bootstrap diode, fast recovery low C_J diode is selected [62]-[63].

b) Turning-on spike

Due to the sensitivity of the gate operation margin, it is of significance to ensure that the gate-source voltage of the GaN HEMT is always in the safe range. An overshoot on the gate can damage the GaN HEMTs easily. Thus, when selecting the gate resistors, it is critical to ensure fast switching time and safe operation at the same time. For safety issues, there are two aspects that need to be taken into consideration: turn on transient and the miller effect. The gate voltage rising transient can be described by the second-order system step response [64]-[65].

As recommended by the datasheet [66], the gate-on drive voltage is set to be 6 V and it should not exceed 7 V due to the gate voltage limitation. Thus, the turn-on gate resistance ($R_{g,on}$) needs to be calculated to keep the gate-source voltage oscillations low, and without deteriorating the switching speed in the meanwhile [67]. From Figure 3.4, through Kirchhoff's voltage law, we can know that

$$v_{in}(t) = i(t) \times R_{g\_on} + L_g \times \frac{di(t)}{dt} + v_{GS}(t) \tag{3-11}$$

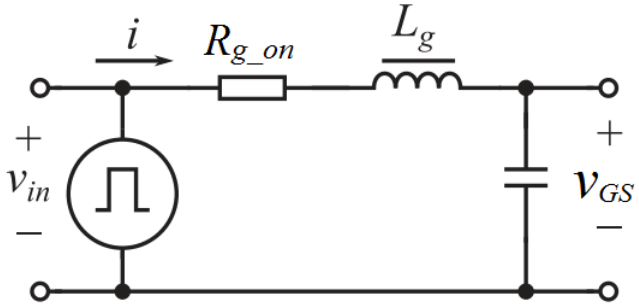


Figure 3. 4 Analysis of the dynamics of the gate-source voltage

By applying the Laplace transform and inserting

$$i(t) = C_{GS} \times \frac{dv_{GS}(t)}{dt} \tag{3-12}$$

The equation (3-13) which illustrates the dynamics from the gate driver to the gate voltage of the GaN device can be obtained:

$$\frac{V_{GS}(s)}{V_{in}(s)} = \frac{\frac{1}{L_g \times C_{GS}}}{s^2 + \frac{R_{g\_on}}{L_s} \times s + \frac{1}{L_g \times C_{GS}}} \tag{3-13}$$

Compared with the standard form of a second-order system, the state variable transfer function can be derived [68]:

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3-14}$$

where ζ represents the damping ratio and ω_n is the resonant frequency:

$$\zeta = \frac{R_{g\_on} \times \sqrt{C_{GS}/L_g}}{2} \tag{3-15}$$

$$\omega_n = \frac{1}{\sqrt{C_{GS} \times L_g}} \tag{3-16}$$

Where C_{GS} is the gate-source capacitance of GS66516T.

The second-order system step response under different damping coefficients are shown in Figure 3.5 [68].

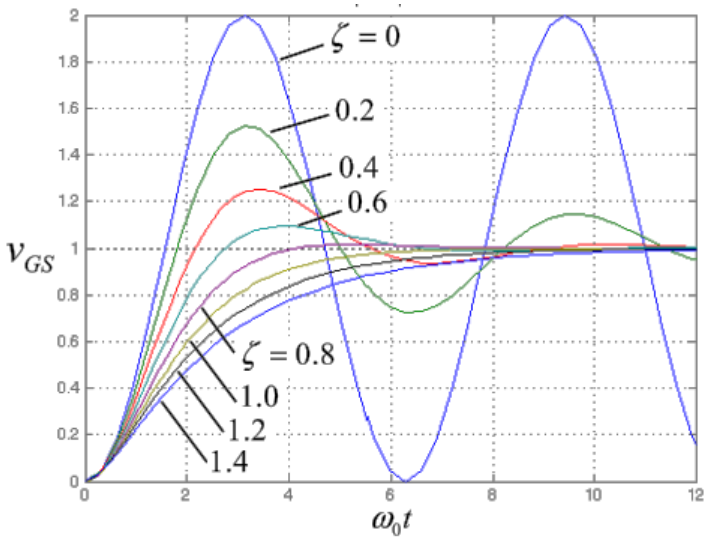


Figure 3. 5 The second-order system step response

To get a rapid rise time thus to fully develop the potential of GaN HEMT's fast switching speed, the resonant frequency ω_n should be great enough [65]. Therefore, the gate loop inductance L_g should be minimized because C_{GS} is an inherent characteristic of the GaN device. To prevent the gate voltage from exceeding the maximum rating, the damping coefficient cannot be too small. Eventually, R_{g_on} can be derived from (3-15) and expressed by (3-17):

$$R_{g\_on} \geq \zeta \times \sqrt{\frac{4 \times L_g}{C_{GS}}} \tag{3-17}$$

c) Miller effect

For a half-bridge topology, the miller effect is another problem that should be considered. During the high-side GaN HEMT turn-on transient, the high slew rate of drain to source voltage (V_{DS}) on the high-side GaN HEMT may cause a false turn-on on the low-side off-state GaN

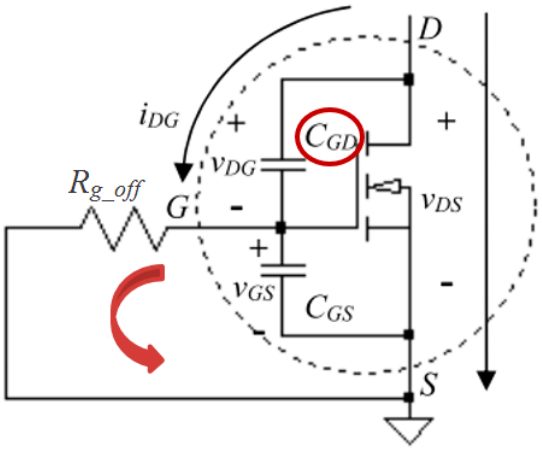


Figure 3. 6 The model of Miller effect

HEMT. This false turn-on sometimes is also called "Miller turn-on". This phenomenon can be explained by Figure 3.6. The $\frac{\mathrm{d}v_{DS}}{\mathrm{dt}}$ is coupled to the low-side gate electrode by the gate to drain capacitor, which is also called the Miller capacitor C_{GD} and can be expressed in (3-18) and (3-19),

$$i_{DG} = C_{GD} \times \frac{dv_{DG}}{dt} \tag{3-18}$$

$$v_{DG} = v_{DS} - v_{GS} \tag{3-19}$$

The gate to source capacitor is charged when the current i_{DG} flows through the gate loop which contains R_G and C_{GS}:

$$R_{g\_off} \times i_{DG} = v_{GS} \tag{3-20}$$

Once v_{GS} exceeds the gate threshold voltage V_{th}, which is 1.1 V - 2.6 V as given by the datasheet [66], the low-side off-state GaN HEMT will be unintentionally turned on and a short circuit may happen in the power loop. Then the power loss will become severe especially in the high switching frequency application and even worse, it may cause devastating consequence. Thus, the resistance of the gate drive circuit should meet the constrain as in equation (3-21):

$$R_{g\_off} \leq \frac{V_{th}}{i_{DG}} \tag{3-21}$$

It can be seen that to avoid the miller effect, the gate resistor for turning-off should be as small as possible. This conflicts with the design consideration for turning-on, thus it is better to separately design the turn-on loop and the turn-off loop as shown in Figure 3.7.

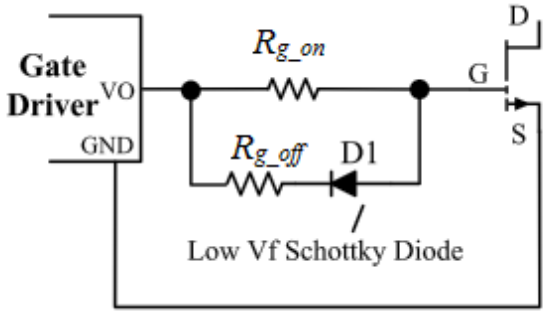


Figure 3. 7 Separate Rg_on/Rg_off gate drive circuit

d) Gate resistors

From Figure 3.5, it can be seen that a damping ratio of ζ =0.8 can be selected to maintain fast rise time, yet limited oscillation of V_{gs}. Considering the C_{gs} and assuming that the gate inductance is dominated by the ferrite bead, an external gate resistor of 10 Ohms is chosen for turning-on after considering the internal parasitic gate resistance [69].

According to the gate drive design application note released by GaN Systems [26], the gate-off resistor should be 5-10 times lower than the gate-on resistor to prevent Miller effect. Thus, considering the inherent parasitic resistance existing in the gate electrode of GaN HEMT, a gate-off resistor of 1 Ohm is selected for turning off. This may lead to a small negative overshoot during turning off, but as the limitation of the negative gate to source voltage is rated at -10 V [66], a slight spike during turning off transient will not pose a threat.

On the gate driver board, the current sensing circuits are also integrated for detection and safety purposes.

3.3.3 Power supply board

In addition to the inverter board and the gate drive board, there are other circuit blocks needed, such as DC-DC converters and gate signal process circuit. They are integrated together and placed on the third board called the ‘Power supply board’ as shown in Figure 3.8. This board is responsible for providing supplementary or additional help and support, on which there are 24 V to ±15 V DC-DC converters supplying to the measurement circuits, and 24 V to 5 V

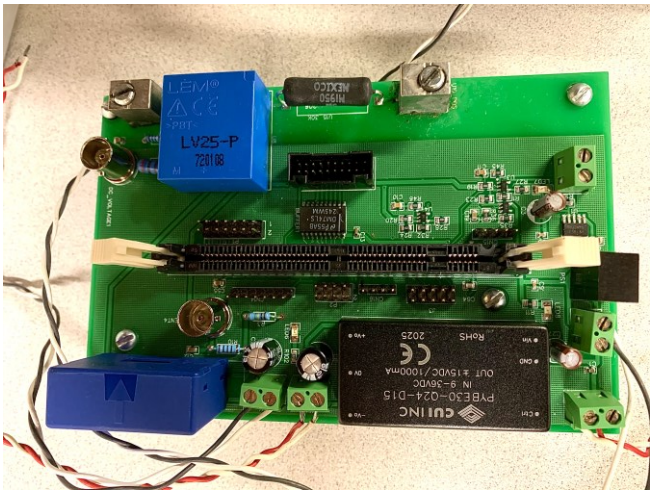
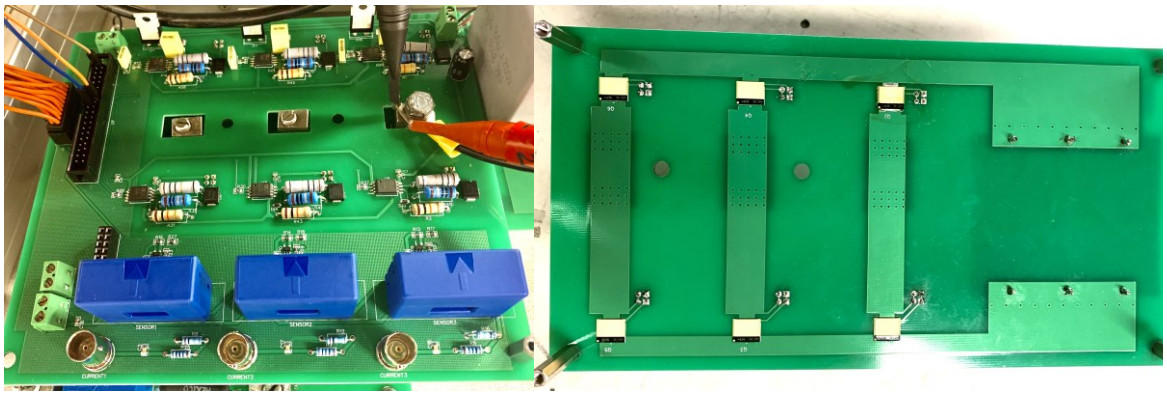


Figure 3. 8 Power supply board

converter supplying to the gate driver ICs, etc. In this way, only a 24 V external power supply is needed from which other levels of voltages can be obtained. Both DSP socket and dSpace connector are placed on this board to support two different control programs.

3.4 Board layout

Due to the sensitive characteristics of the gate voltage, the minimization on the parasitic parameters of gate loop is necessary. Another reason is that, the ground of the input of the gate driver should be separated from the ground of the main power loop to reduce the noise. Thus, the gate drive circuits are placed on a separate board (Figure 3.9 (a)) while the inverter board only contains power bridges (Figure 3.9 (b)). To make the gate loop as short as possible, the gate driver board will be connected to the inverter board vertically, which means, the gate driver board is placed directly above the inverter board and they are connected through male/female gate pins as shown in Figure 3.10. Multiple pins are paralleled together to strengthen the gate and the source. It can be noted that, three rectangular areas are cut on the gate driver board to make space for the output connectors on the inverter board. In summary, the size of the gate driver board is 17.7 cm * 15.5 cm, and the power board's size is 21 cm * 11.3 cm.



(a) (b)

Figure 3. 9 (a) Gate driver board (b) Inverter board

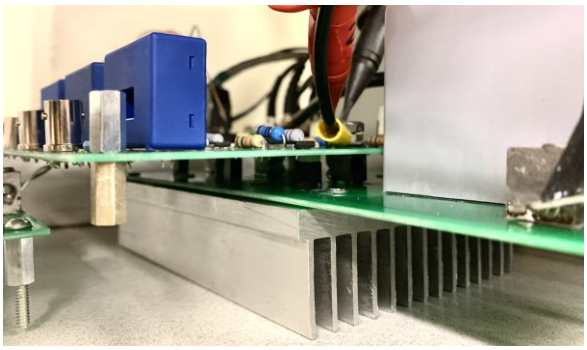


Figure 3. 10 Layout of gate drive circuit and three-phase inverter

The top-cooling type GaN switches are placed on the bottom side of the PCB, and the three output connectors are on the opposite side. Consequently, multiple through-holes are created to connect the top and bottom plane and to let the current flow between the two sides. The heat-sink is attached to the GaN switches on the bottom side with the thermal pad in between. There are also three current sensors integrated for control and safety purposes, then the output current of the three phases can be stretched out from the through-hole and go through the sensors. Additionally, since the exposed metal backside of the GaN HEMT is internally connected to source potential, corresponding holes are also etched underneath each gate and source pin for safety consideration, to avoid shorting of the pins to the heatsink.

3.5 Circuit function check

In this section, the testing on the inverter designed is first described, and then an improved version is also designed based on the problems found during the tests experiments. The steps performed are as follows:

Step 1: Voltage supplies check

Connect the 24 V power supply to the power supply board and then check the function of:

24 V to 5 V converter;

24 V to +15/-15 V converter;

5 V to 3.3 V converter;

3.3 V to 1.5 V converter.

Check the needed voltages can be provided to corresponding components (through soldering pins). During this step, small corrections were made due to inveracious soldering.

Step 2: Gate signals check

Check 5 V voltage from the power supply board is properly feeding to the gate driver board;

Check the 6 V power supply and make sure the ground of 6 V is isolated from that of 5 V;

Check the PWM signals generated by the DSpace from the DSpace side (on the DSpace control board);

Connect the DSpace control board with the DSpace connector (on the gate driver board) and check again through the connector DF51K-20DS-2C(800) to make sure the connection is good. The connector DF51K-20DS-2C(800) can also be used to monitor the DSpace signals.

Check the PWM signals from the gate pins to ensure the GaN switches can receive them.

Step 3: GaN switches check

Perform double pulse test on three legs respectively at 50 V DC bus voltage (with inductive load) to check if the six GaN switches are working properly. Make the high-side switch the DUT and then the low-side switch.

Step 4: Measurement function check

Check the +15/-15 V is properly feeding to the sensors and the current sensors are working well;

Connect the outputs of LA55-P measuring circuit to DSpace and do the calibration in DSpace.

3.6 Three-phase RL load test

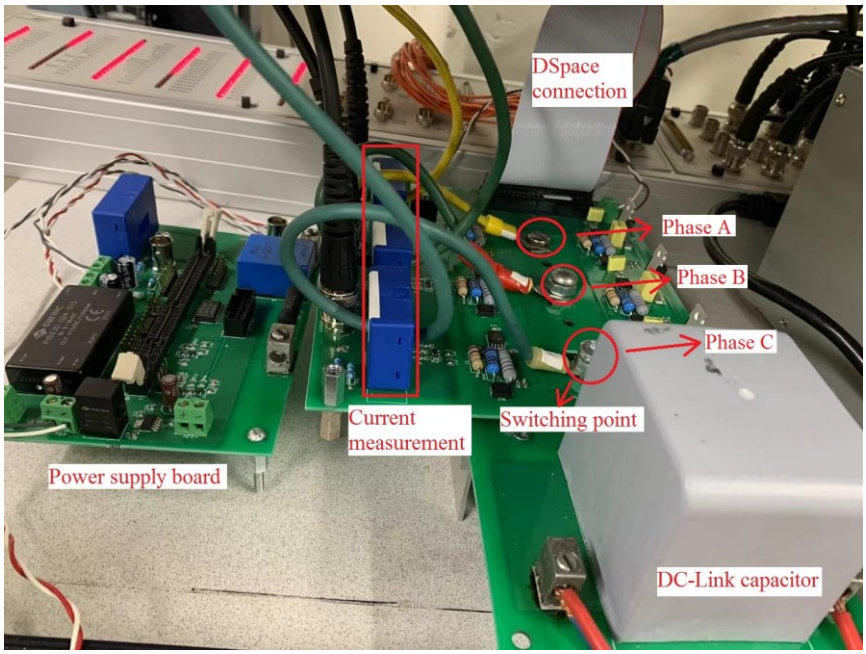


Figure 3. 11 Three-phase RL load test

After checking the function of three half bridges separately, a star-connected three-phase RL load is connected to the inverter to check the system. The circuit diagram is as in Figure 3. 1 where the motor is replaced with RL load. The final assembled system is shown as in Figure 3. 11. The power supply is used to supply a voltage of 100 V which is the maximum voltage it could output. The experiment specifications are listed in Table 3. 2.

Table 3. 2 Experiment specifications

Parameter	Value
Amplitude modulation ratio m_a	0.9
Fundamental frequency (Hz)	60
Switching frequency (kHz)	10
V_{BUS} (V)	100
Resistive load (Ω)	12.6
Inductive load (mH)	3.6

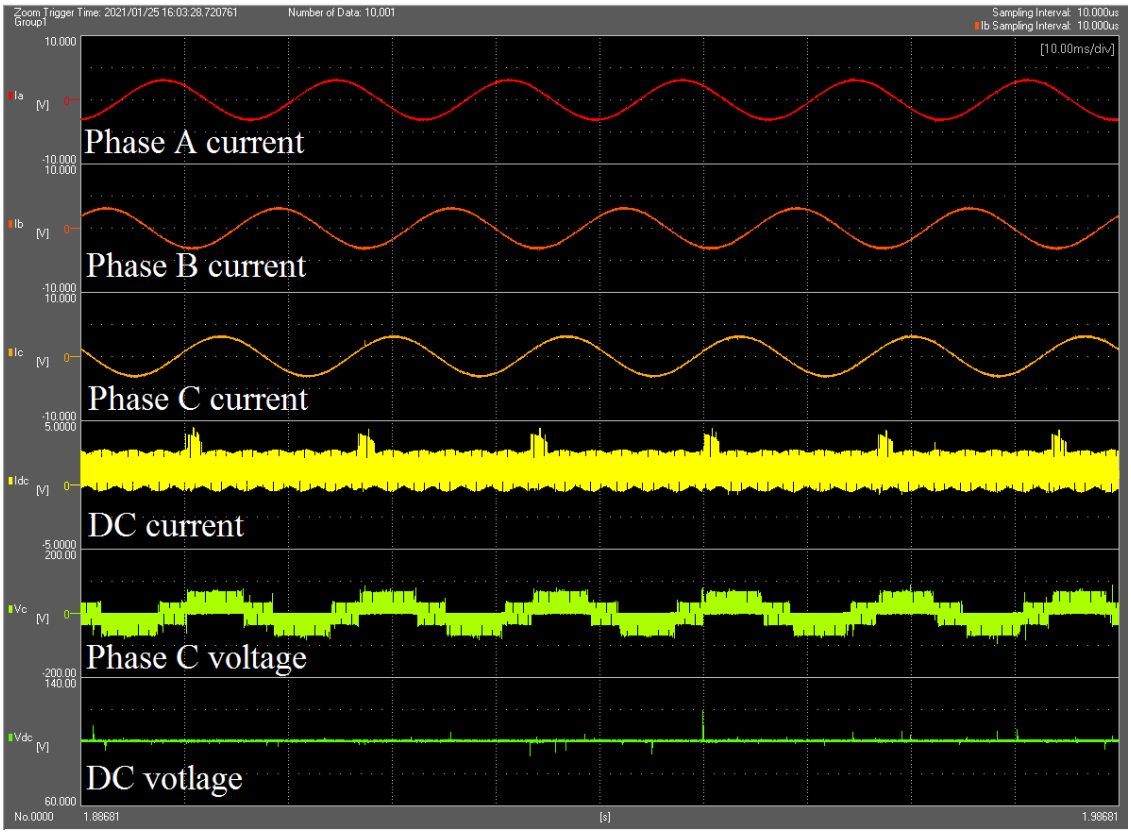


Figure 3. 12 Three-phase RL load testing waveforms

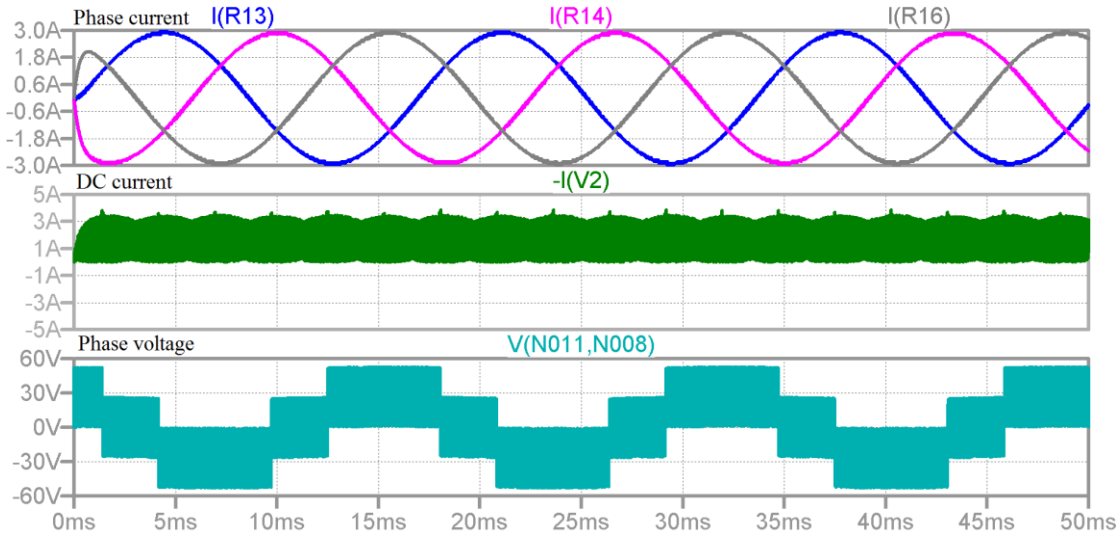


Figure 3. 13 Three-phase RL load simulation waveforms

The three-phase RL load test results are shown in Figure 3. 12 with the comparison to the corresponding simulation results shown in Figure 3. 13. The DC bus voltage is 100 V. The three phases currents are measured which show a sinusoidal shape. The other three channels are for DC current, phase voltage of phase C and DC voltage. Unfortunately, the other two phase voltages are not measured at the same time because the oscilloscope only has six channels.

These preliminary experiments show the potential benefits provided by the GaN-based inverter in the aspect of the quality of the output waves. The GaN-based inverter provides excellent current sinusoidal waves to the load withou an output filter. The author would have liked to perform more experiments in order to bring more insight of the system. However, further tests haven't been performed yet since they would require different test setups, equipment in particular for higher power levels, for which equipment was not directly available, and the timeline limited the amount of experiments data acquired.

3.7 Summary

In this Chapter, a three-phase system which includes an inverter board, a gate driver board and a power supply board is proposed and designed. A review on GaN power transistors is demonstrated first and the selections of the GaN device and the DC-link capacitor are illustrated based on the survey. Instead of commercially available monolithic gate drivers, which are expensive and inflexible, a bootstrap topology is used to drive the GaN HEMTs while using the fewest componens. According to the application notes published by GaN Systems and EPC, the design considerations for a bootstrap gate drive circuit are discussed. Many issues are taken into consideration including the gate overvoltage, shoot-through current caused by Miller effect and the calculation of gate resistors. As for the PCB design, relative PCB requirements about electrical and physical specifications are met when placing and routing components. The layout and the installation of the system are presented. The GaN-based system can be quite small and cost effective which has the fewest circuit blocks, standard componens, and high compactness. Finally, several test procedures are conducted to ensure that the function of each part of the system works properly. Corrections are made to the circuits before the three-phase RL load test. Then the RL load tests are performed with the DC bus voltage at 100 V, and the basic waveforms are given and compared with a finely matched three-phase simulation for the inverter. It is shown that the inverter designed can generate sinusoidal outputs as expected. However, due to the maximum output limit of the power supply, experiments at higher voltage has not been done yet.

CHAPTER 4 PARASITC PARAMETERS VERIFICATION AND IMPROVEMENT ON GAN INVERTER DESIGN

4.1 Introduction

Due to the fast-switching speed of GaN HEMTs, high dv/dt and di/dt are produced, which may induce ringing and electromagnetic interference due to the existence of parasitic elements in the packaging and the PCB traces [69], [70]. To improve the performance of GaN HEMTs at high frequencies, manufacturers have made efforts to improve the device characteristics and packaging. Different packaging techniques have also been developed and compared to provide minimum inherent parasitic inductances [71], [72]. With lower package parasitic inductance, the PCB layout becomes the main limiting factor in converter performance. When the device turns off, the energy stored in the stray inductance of a commutation loop may induce a voltage spike and ringing with the parasitic capacitances of the device, and potentially might lead to not only parasitic losses, but also an over-voltage breakdown which may damage the transistors [46], [73]. Consequently, the power loop inductance should be quantified and minimized in the design stage of PCB layout.

4.2 Parasitic extraction and verification

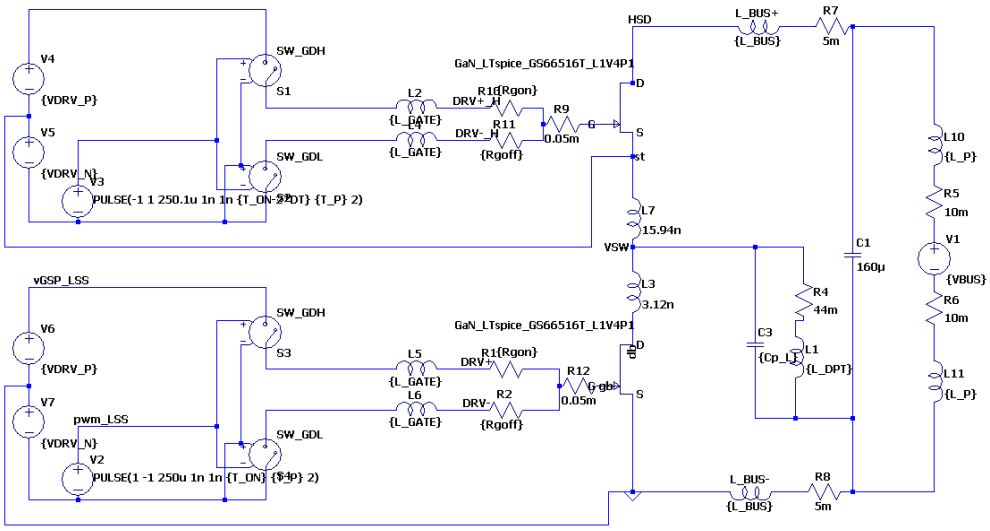
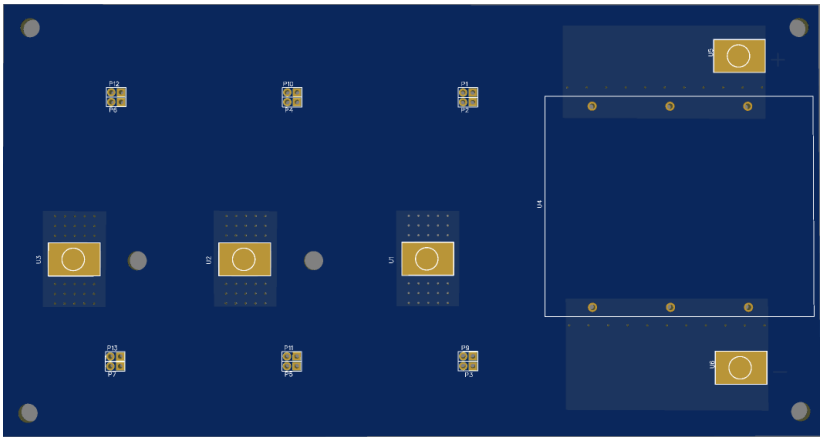
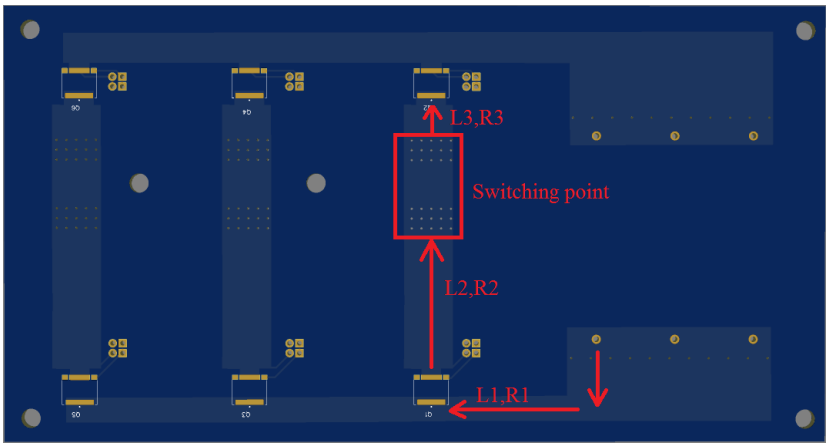


Figure 4. 1 DPT circuit in LTspice

To verify the parasitic parameters, a double pulse test (DPT) is conducted to obtain the DC bus current, load current and device voltages. The testing schematic is shown as in Figure 4. 1. The GaN-based inverter designed in Chapter 3 is used to perform the test. Different



(a)



(b)

Figure 4. 2 (a) Top layer layout (b) Bottom layer layout

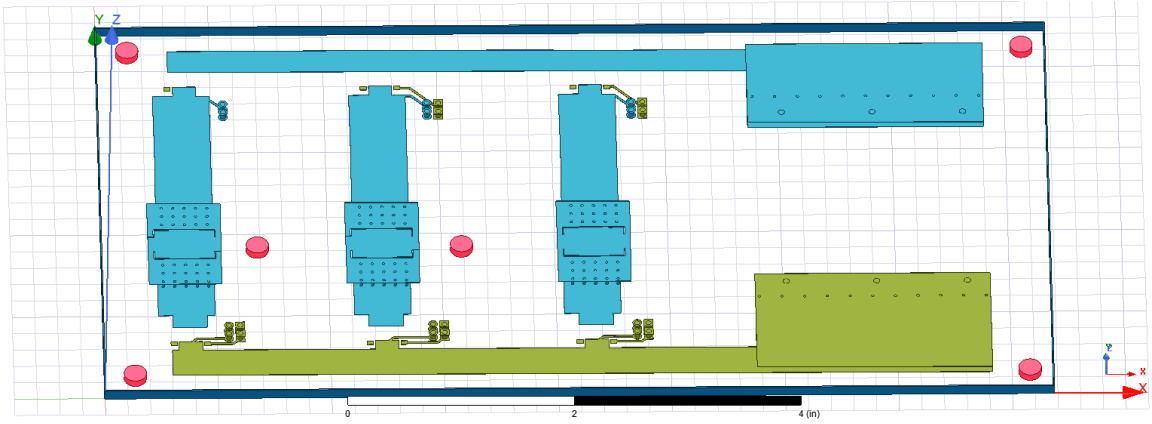
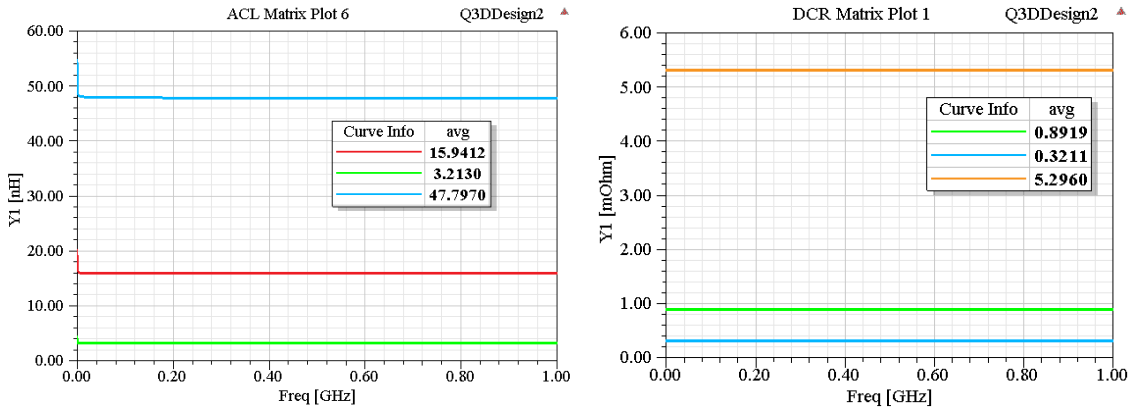


Figure 4. 3 3D model for the power board in Q3D



(a) (b)

Figure 4. 4 Q3D simulation results (a) parasitic inductance (b) parasitic resistance

parasitic components of the PCB are also included: the power loop inductance, the parasitic inductance from DC supply, the parasitic capacitance between elements and the load. The parasitic values are extracted from Ansys Q3D software [75]-[77]. The traces are divided as shown in the Figure 4. 2 through the segmentation method [78]. The 3D model is as shown in Figure 4. 3 and the results are given in Figure 4. 4 and concluded in the Table 4. 1. The L_{loop} and R_{LOOP} is the loop inductance and resistance respectively. L_{DC} represents the parasitic inductance introduced by the DC power supply and the connecting wires. The accuracy of the parameters can be verified by the Ltspice simulation and experimental results in the next section.

Table 4. 1 FEA Simulation results from Ansys-Q3D

Trace	Parasitic Inductance
L1	47.7970
L2	15.9412
L3	3.2130
L_{LOOP}	67nH
R_{LOOP}	11.8mΩ
L_{DC}	0.8μH

4.3 Experimental results

The test circuit and experimental setup are shown in Figure 4. 5. The whole system

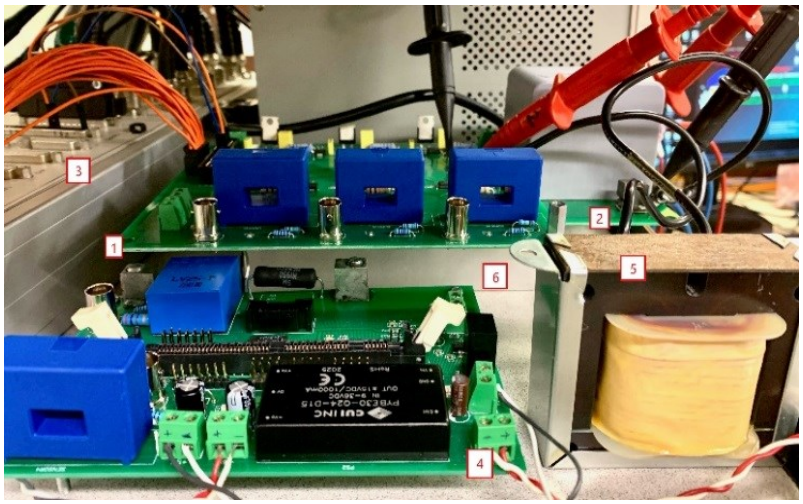


Figure 4. 5 Double pulse test set up

contains different parts: Part 1 marked in the figure is the gate driver board connected and installed right above the GaN-based inverter board (part 2) through male/female pins on the gate and source electrodes. The inverter is built with 650 V GS66516T GaN E-HEMT released by GaN Systems. The control signals are set and generated by dSpace control desk (part 3) and delivered to the gate board. The PCB of part 4 functions mainly as power supplies to provide corresponding voltages to the gate driver board. Part 5 is the inductor used as the load in the DPT. Moreover, with the properties of 650 V voltage and 60 A current capacity, a heat-sink is required to ensure the safety of operation.

Since GS66516T is top-side cooled transistors, the heat-sink (part 6) is installed on the same side as GaN devices, consequently the impact of temperature can be neglected within a short period of time during the test.

In the double pulse test, the switching-off moment after the first pulse and the switching-on transient process during the second gate-on pulse are focused since the first gate-on pulse given to the DUT is used to charge the inductor current to a load current of 5 A. When the gate-off signal is given on the device under test (DUT), which is the high-side switch, the low-side switch will be turned on after the dead time which is set to be 100 ns in the experiment. In this interval, the energy stored in the inductor in a previous stage is releasing and the current is circulating through the low-side switch and the load. The current in the DUT reduces to zero at this stage. Then the second gate-on pulse will be generated to turn on the DUT again at the switching condition of V_{DS}=100 V while I_{DS} keeps at 5 A since the reduction in the inductor

current is small and can be ignored.

The test conditions and equipment used are shown in the Table 4. 2. The current probe is clamped between the DC power supply and the DC bus positive terminal on the inverter board to measure the DC bus current. Due to the existence of parasitic inductance and DC bus capacitor, the load current is not completely consistent with the channel current flowing through the DUT. Two differential voltage probes are used to record the drain-to-source voltage waveforms of DUT and non-DUT respectively. Another voltage probe RT-ZP03 is to capture the gate voltage generated from dSpace simulator and then be used as the trigger condition on the oscilloscope.

Table 4. 2 Experiment specifications

Parameter/Device	Specification
Temperature	25 ℃ (room temperature)
Switching frequency (kHz)	10
V_{BUS}(V)	100
I_L(A)	5/2
V_{DR}(V)	+6/0
$R_{g(on)}/R_{g(off)}$ (ohm)	10/1
Current Probe	Tektronix TCP0030A
Voltage Probe	Yokogawa 700924 Differential Probe; Rohde & Schwarz RT-ZP03
Oscilloscope	Tektronix TBS 2000 Series
DC power supply	VOLTEQ MASTECH HY10010EX

Comparing the experimental results in Figure 4. 6, the simulation results and experimental results conforms well which means the parasitic parameters extracted from Q3D are reasonable. The DC bus current is showing a ringing frequency of around 35 μs, indicating a resonance frequency of 14.3 MHz. The parasitic inductance introduced by the DC power supply and the connecting wires can be estimated to be 0.8μH by:

$$2 * \pi * f_{ring} = \frac{1}{\sqrt{L_{DC}C_{DC}}} \quad (4\text{-}1)$$

Also, the parasitic parameters in the loop, mainly the parasitic capacitance of the inductor and the parasitic inductance of the PCB traces causes current ringing in the load current and the turn-off voltage. From the experimental results, a turn-off ringing with the resonance

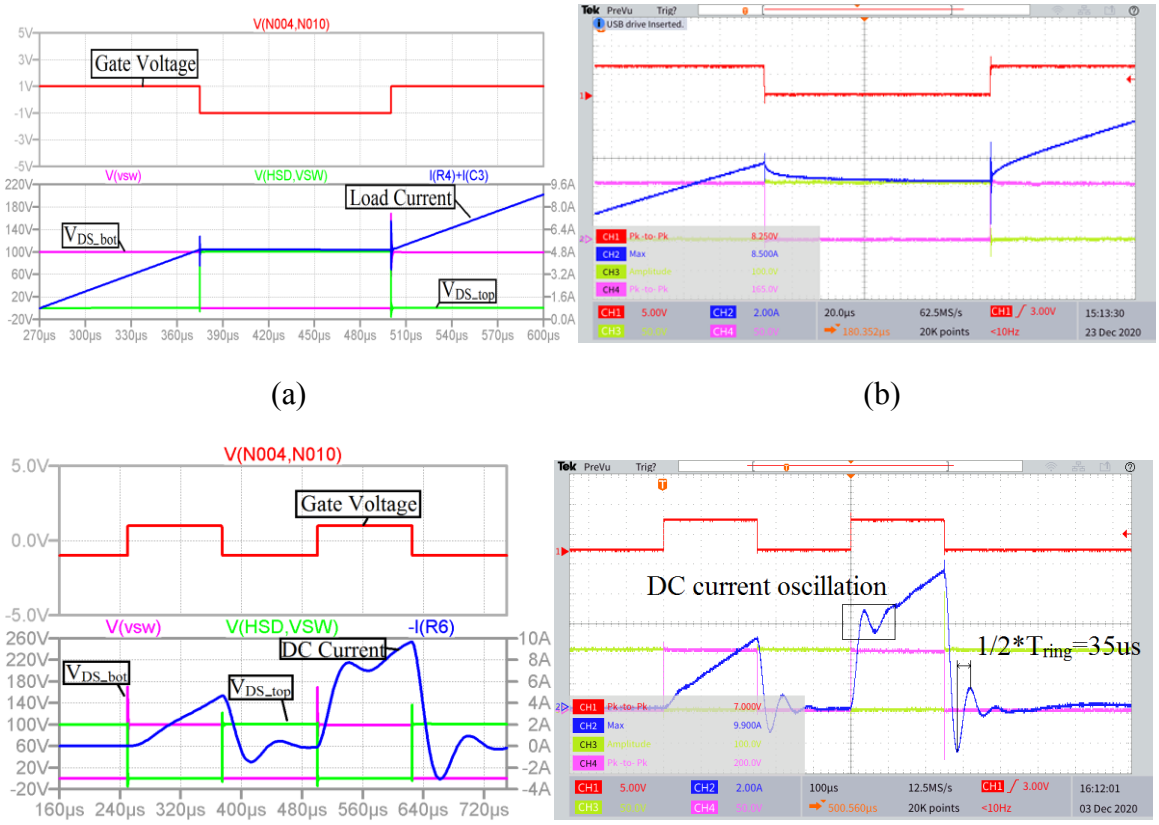


Figure 4. 6 DPT results with the blue curve representing (a) Load current, simulation (b) Load current, experiment (c) DC current, simulation (d) DC current, experiment

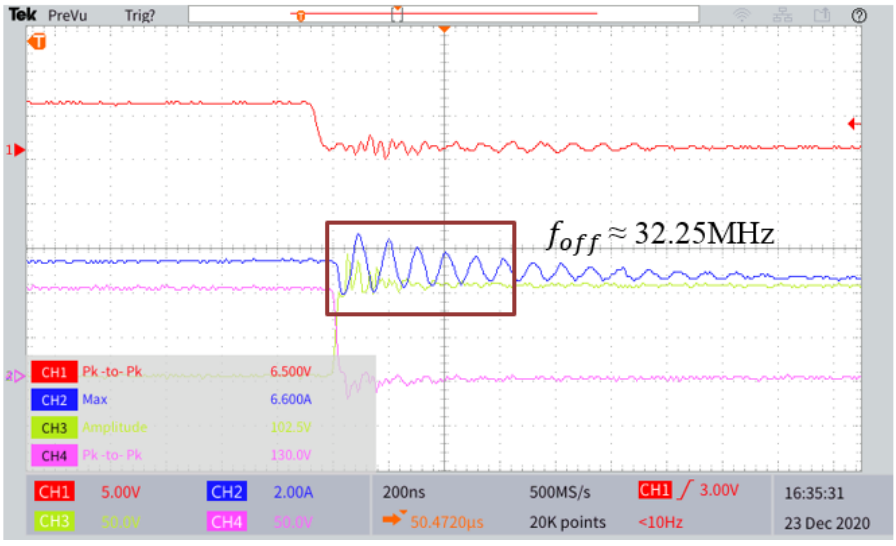
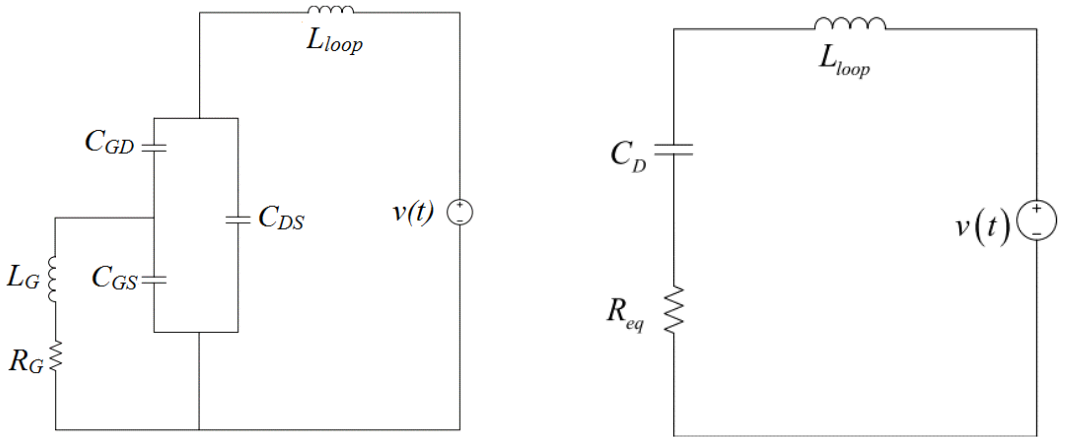


Figure 4. 7 Experimental results for turn-off oscillation

frequency of 32.25 MHz can be observed in Figure 4. 7.

The power loop parasitic inductances can be verified through the oscillation of the turn-off transient. One device is in reverse conducting and the turn-off device can be represented by



(a) (b)

Figure 4. 8 (a) Simplified turn-off circuit. (b) RLC equivalent circuit model

three capacitors as shown in Figure 4. 8 (a). The circuit can be further simplified into a RLC equivalent circuit as shown in Figure 4. 8 (b) [80], [81]. In this RLC loop, the oscillation frequency should match the resonance frequency of turn-off waveform. Then the resonance frequency can be approximated by:

$$X_{C_D} = \frac{X_{C_{DS}} \times X_{C_{GD}}}{X_{C_{GS}} + X_{C_{DS}} + X_{C_{GD}}} \tag{4-2}$$

$$2 * \pi * f_{off} = \frac{1}{\sqrt{L_{loop} * C_D}} \tag{4-3}$$

Where the L_{loop} represents the total parasitic inductance of the whole power loop. Through equation (4-2) – (4-3), where the capacitance can be extracted from the characteristic curve, C_D is calculated to be around 370 pF. Then the loop inductance can be calculated to be 65.8 nH. This also verified the extraction results obtained from Ansys Q3D in which the results show around 67 nH. Though the Q3D simulation results are slightly greater than the calculation results, we can know that the error is in a small range and the simulation results can be regarded as a proof when working on the improved layout. This can help further research on the improvement of the layout which requires a lower parasitic inductance of the loop.

4.4 Problems from design Version.1

Based on the experience of designing the first version of GaN inverter and the several tests, some problems are found:

a) The breakdown happened at the 6.2 V protection Zener diodes in the circuit to keep the gate voltage in the safe range which is from -10 V to 7 V, which means an overvoltage occurred at the gate. This phenomenon is noticed through the oscilloscope used to monitor the gate input signals at the DSpace side. The control signals from DSpace show some noise with an increase of the DC bus voltage. This is because, even though the ADuM4121 gate driver IC itself offers isolation between the input and the output, the input side is still affected by the power side. This means the layout of the gate driver board can be improved to provide a better separation between the input side and the output side.

b) In Version 1, both high-side and low-side switches are turned off at 0 V. However, in bootstrap topology, there can be a voltage fluctuation on the bootstrap capacitor. The bootstrap capacitor has a risk of overcharging when the lower device is reverse conducting in the charging loop. This is because the V_{DS} of low-side switch will be reflected to the supply voltage and it will be more severe when the reverse conducting current is high as shown in Figure 4. 9. When the current is 40 A, there is a voltage drop of 1 V. The bootstrap capacitor voltage can be represented by:

$$V_{BOOT} = V_{DR} - V_{DS(LOW)} - V_{F,D} \quad (4\text{-}4)$$

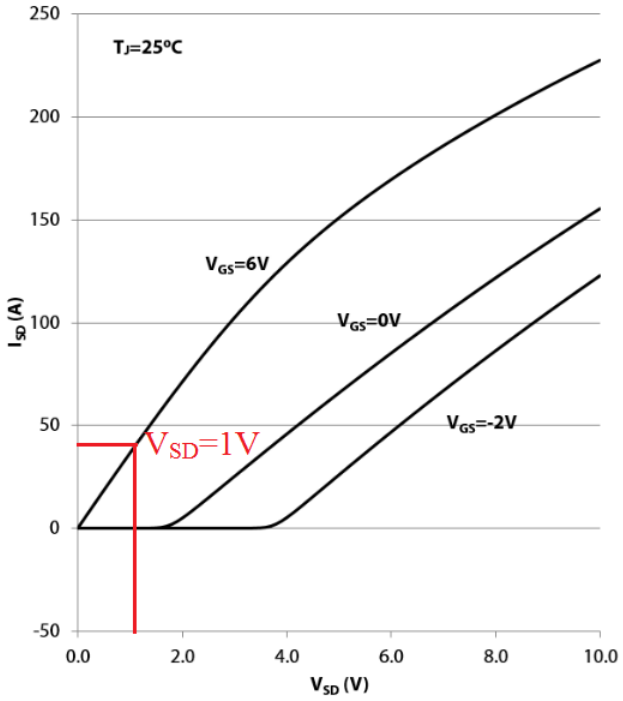


Figure 4. 9 GS66516T reverse conduction characteristics

During the high-side GaN HEMT turn-on interval, the high dV_{DS}/dt is coupled to the gate electrode of the low-side device due to the existence of the miller capacitor (C_{GD}). As has been discussed in chapter 3, the parasitic capacitors will be charged and the charging current will flow through the gate loop. With a higher bootstrap voltage, a higher i_{DG} will be coupled onto the low side. Once the gate-to-source voltage (V_{GS}) exceeds V_{th}, the off-state low-side device will be turned on unintentionally. This means, even though the low-side is connected to a stable supply, there is a risk of unintentionally turn-on at low side due to the high side fluctuation.

c) The current of Phase A and Phase B contain more harmonics than Phase C when the switching frequency increased from 10 kHz to 20 kHz. This is probably because, due to the design of the layout showing in previous chapters, the length of the power loop for phase A and phase B is longer than phase C, which leads to higher parasitic inductance. The Q3D results show that the furthest bridge has almost 3 times greater parasitic inductance than the nearest bridge. From reference [79], it can be known that the parasitics existing in the power loop and gate loop together make a contribution to the ringing on the gate voltage. The overvoltage happens on the phase A and phase B and causes noise as observed at the output side.

4.5 Improvement in design Version.2

4.5.1 The isolation between high-voltage side and low-voltage side

In the Version.2 design, the layout of the gate drive circuit is designed to have better isolation between the output side and the input side. Six gate driver ICs are aligned horizontally as shown in Figure 4. 10. In this way, all the input control signals from DSpace are kept away from the high voltage side and thus the signal interference can be suppressed. As for the connection, the gate driver board will be plugged onto the power board as before, which ensures a low parasitic inductance in the gate loop.

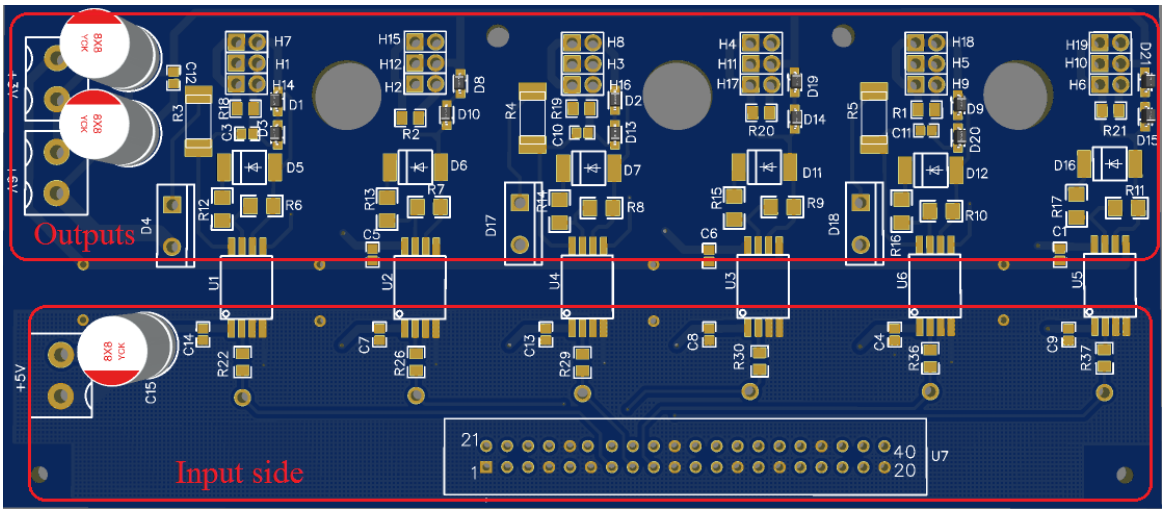


Figure 4. 10 Improved layout of gate drive circuit

4.5.2 Negative and adjustable gate voltage control for turn-off

Though GaN devices can be turned off at 0 V gate voltage, negative off voltage is added to the schematic for two objectives. First, a negative voltage can provide a safer operation as has been explained in previous section. Second, it can also benefit further researches about the effects of negative off voltages. The improvement of the gate circuit is shown as in Figure 4. 11. Since the IC ADUM4121 is a unipolar gate driver, this can be a straightforward way to generate negative turn-off voltage without increasing too much cost. Another advantage of this improvement is that, the gate voltage can be altered in terms of different needs. If a negative

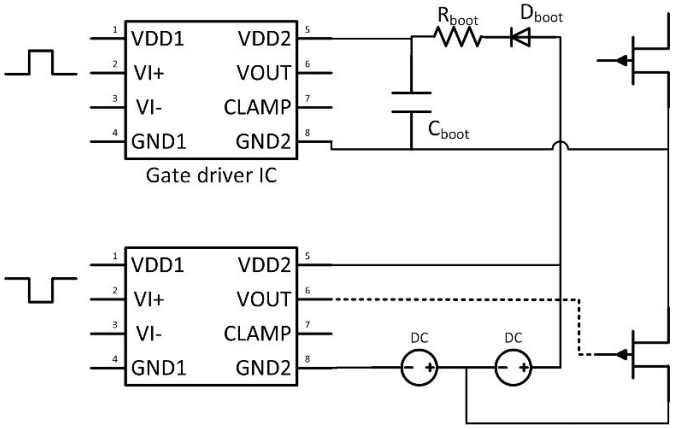


Figure 4. 11 Generation of negative turn-off voltage on low-side GaN HEMT using unipolar gate driver.

off voltage is not needed, a 0V can also be used by simply short-circuiting the connector.

4.5.3 Reduced and more balanced parasitic parameters

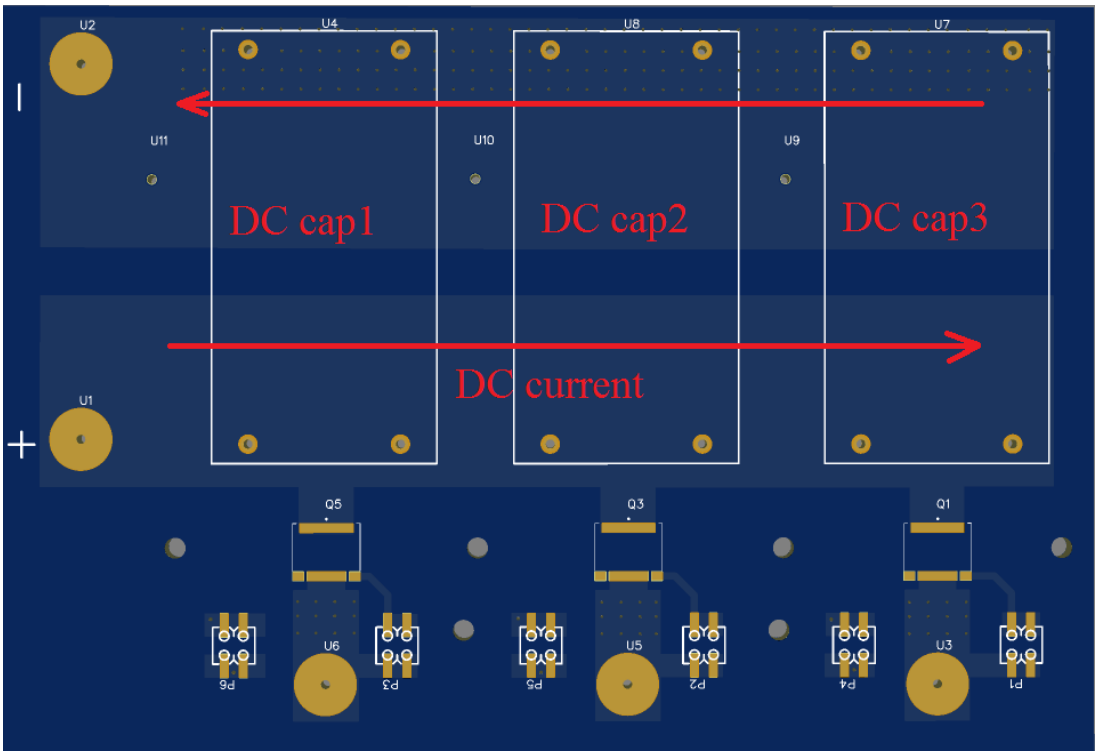


Figure 4. 12 The improved layout of power board – Top layer

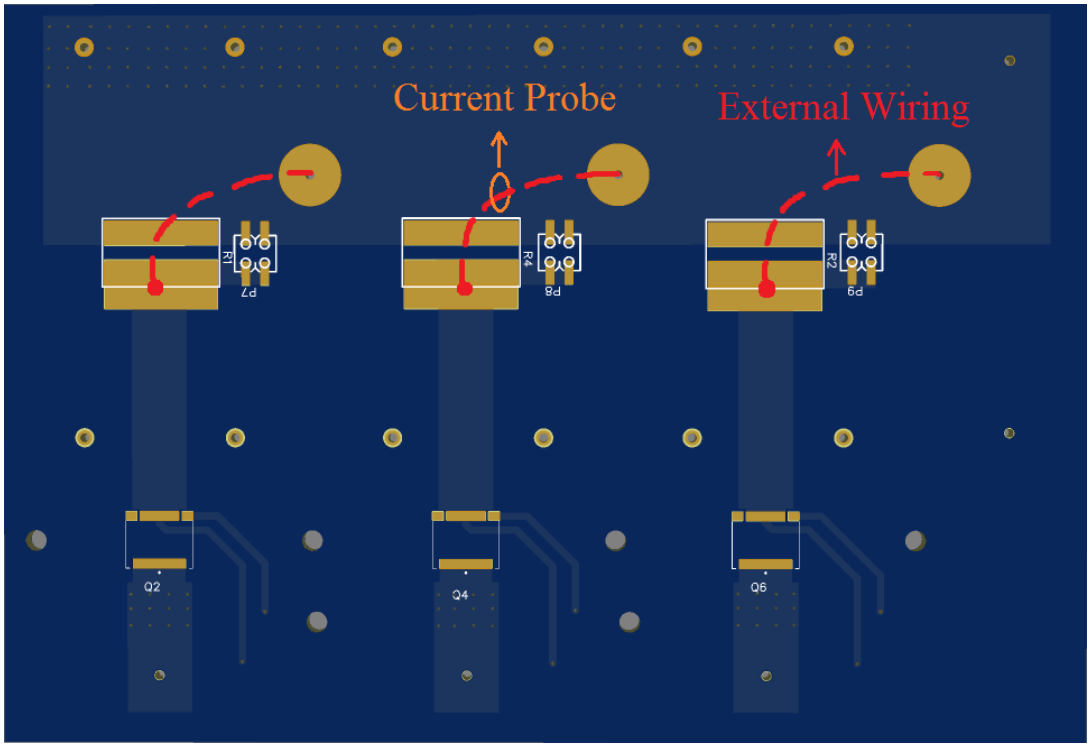


Figure 4. 13 The improved layout of power board – Bottom layer

In Version.2, instead of using a lumped capacitor as the DC-link capacitor, one distributed capacitor is used for each phase as shown in Figure 4. 12. This can help to make the length of every power loop equal to each other as the DC capacitor can be seen as the power supply. The parasitic inductance of the PCB traces are mostly dependent on the length of the loop when other parameters are the same. Consequently, the parasitic inductance can be more balanced. Moreover, the DC current flowing out of the DC+ and flowing into DC- can bring the benefit of magnetic flux cancellation. The current path through the devices is folded to increase the mutual coupling between the current through the two devices and the DC-link capacitor is also mounted near the devices as closely as possible, therefore the total parasitic inductance of

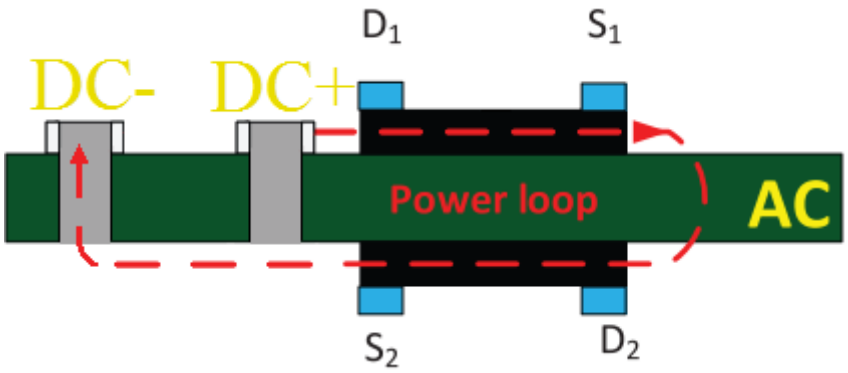


Figure 4. 14 Improved design power loop (side view)

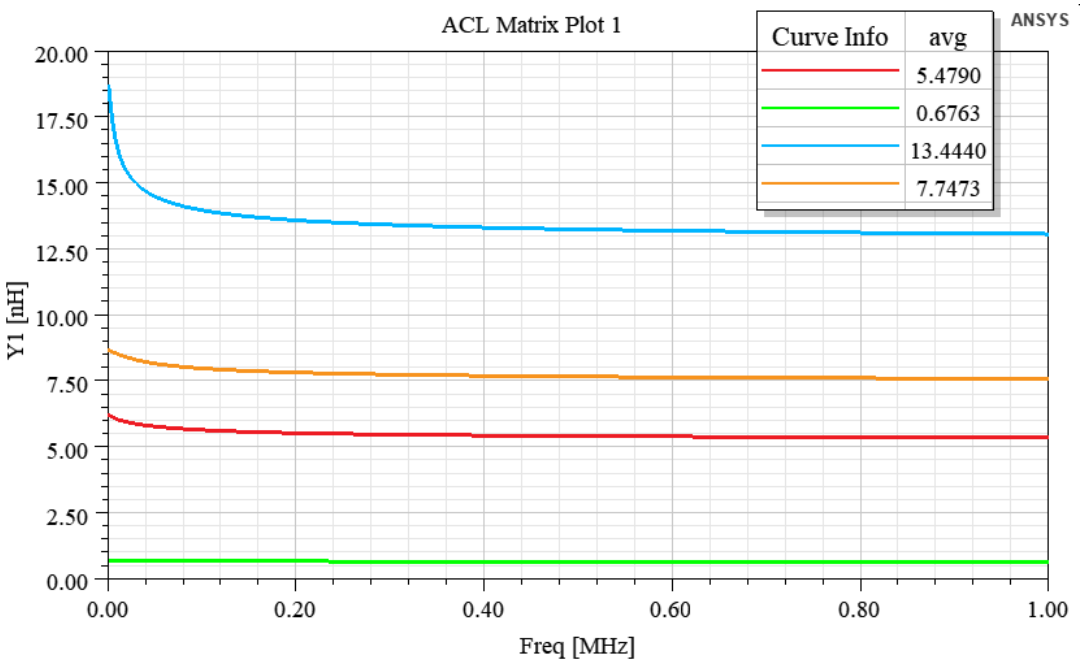


Figure 4. 15 Self-inductance extraction for each segment of the trace

current commutation loop can be reduced significantly due to self-cancellation compared with the Version.1 design. The side view of the layout is shown in Figure 4. 14, where the current through the top layer and the bottom layer are folded with opposite directions. The magnetic field cancellation can help to reduce the parasitic inductance in the loop. The Q3D simulation results for the second version of layout are shown as in Figure 4. 15 and Figure 4. 16. The summarized results are given in Table 4. 3.Compared with the first version, the total loop inductance for each bridge has been reduced by around 60%. Figure 4. 17 shows that, the

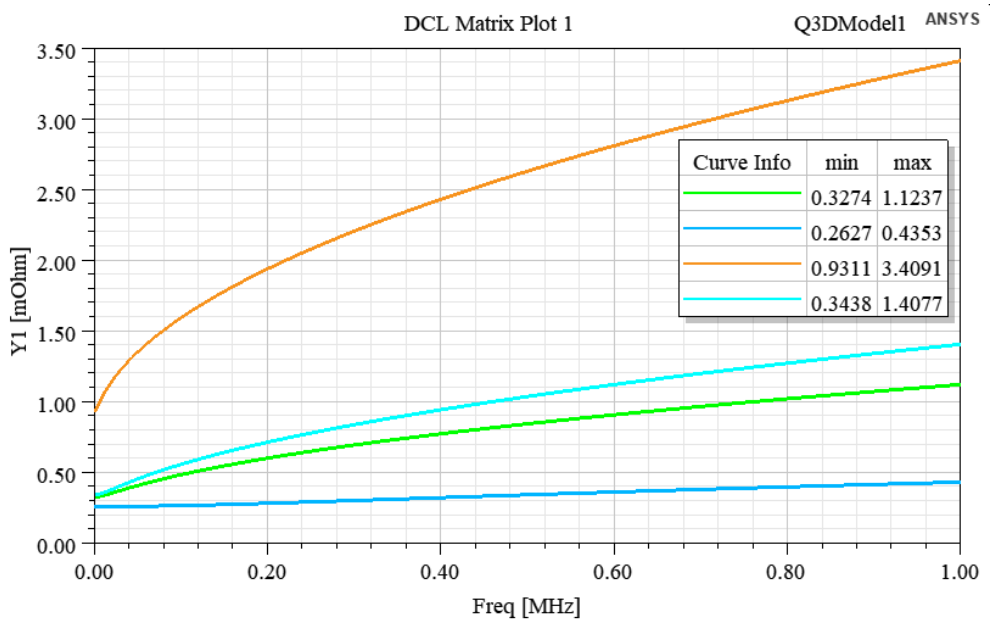


Figure 4. 16 Parasitic resistance extraction for each segment of the trace

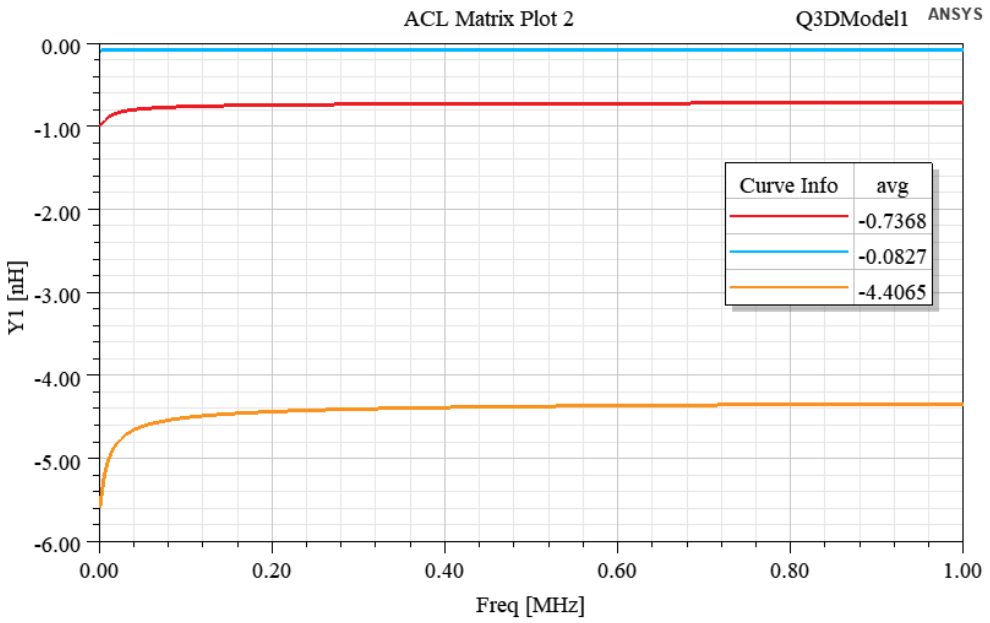


Figure 4. 17 Mutual inductance extraction between different segments

mutual inductances between main segments of the trace are negative, which means the magnetic flux cancellation can help to further reduce the total loop inductance. However, for this design, it is more demanding for the thermal managing. Two heatsinks are needed to wrap the PCB in between, which is similar to a “sandwich” structure.

Table 4. 3 Parasitic parameter extraction for Version 2 design

Parameter	Value
L_{loop}	27.35 nH
R_{loop}	6.3758 mΩ

4.5.4 More testing points

In the previous design, it was found that more testing points should be added. For example, other than the DSpace control signals, the signals injected into the gate electrode of GaN devices should also be added to have a better observation and to help orientate problem components.

Furthermore, to accurately measure the current going through the switches, two methods are used. Firstly, measurement resistors of 1 mOhm are added for each bridge. However, considering that the voltage drop can be probably influenced by the power loop, three external screw terminals are also reserved. By external wiring, the current can be measured through high band-width current probes directly as shown in Figure 4. 13.

4.6 Summary

In this chapter, the parasitic parameters of the power board designed in chapter 3 are extracted through a 3D model and verified by double pulse tests. The simulation waveforms conform well with the experimental results. The parasitic parameters can provide support to subsequent layout improvement.

Moreover, an improved version of GaN-based inverter is designed in terms of the

troubleshooting experience with the first version. The problems from the original version are defined and analyzed in theoretical aspect first, and are well addressed in the next version to have a better performance. The layout of the gate driver board and the power board are also reconsidered to provide better isolation between the high voltage side and the low voltage side and to reduce the effects of noise coupling. The gate circuit is also revised to have an adjustable gate-off voltage which can be chosen to be zero or negative values according to different needs. The parasitic inductance of the PCB traces also decreased considerably through the simulation by Ansys Q3D which proves that this second version has an improved layout. Finally, more testing points are also added to benefit further researches and experiments.

CHAPTER 5 CONCLUSION AND FUTURE WORK

5.1 Conclusion

This thesis mainly presented: 1) The switching characterization of enhancement-mode GaN HEMT. The switching on and switching off model are improved based on the traditional model, and proved more accurate; 2) A cost effective new-generation GaN-based three-phase inverter was designed and tested; 3) An improved power loop design is achieved to reduce the parasitic parameters in the three-phase inverter.

Chapter 2

In this chapter, the operating principles of enhancement-mode GaN transistors are introduced first. Then the traditional models for switching events are presented. However, the turn-on transient model given by the conventional method is not accurate enough for GaN switches due to inaccurate current commuting estimation and the turn-off model is not suitable for GaN HEMTs without considering the load condition. The peak value of current is estimated through average current calculation. Therefore, based on the traditional models and their limitations, improved switching transient models are proposed in this chapter. First of all, the current spike during turning on process is considered and the peak value of current is estimated through average current calculation. For turning-off event, a reverse turn on model is proposed to provide the transient time estimation for GaN HEMTs in half bridge application. Through the method of integral and linear curve fitting, more practical values of output capacitance charges are used to replace the traditional estimation. Moreover, plateau shifting is another factor that affects the accuracy of the switching energy estimation. The proposed switching model is straightforward and computationally inexpensive, and proves to have better accuracy than the traditional method through the verifications in both simulation and experiments.

Chapter 3

In this chapter, the considerations for the design of the new-generation GaN-based three phase inverter is summarized. A review of the development of GaN power transistor and package technologies is presented as the background for the project. Different packages of GaN

devices are compared to select the most suitable one for the design. The whole inverter system can be divided into three parts: the three-phase power board, the gate driver board, and the power supply board which provides the extra functions needed by the system. Bootstrap topology used in the design is of low cost and low complexity. The gate drive circuit design for the GaN switches need special attention in the respect of the turning-on spike, the miller effect and the selection of gate resistors. The assembling of the power board and the gate driver board is in a way of plug-in vertically to minimize the loop length for the gate control signals reaching the gate electrode of GaN transistors. The heatsink is also attached to form a complete inverter system with better thermal performance. The testing procedures are introduced and the three-phase RL load tests are performed to validate the functionality of the system.

Chapter 4

Chapter 4 mainly focuses on the tests and improvement on the GaN-based three phase inverter. Ansys Q3D software and theoretical analysis are used to provide an estimation and verification of the parasitic parameters of the PCBs. Problems found during the tests are defined and they are the fundamentals on which the next version is improved. In the second version of design, a stronger isolation between high-voltage and low-voltage sides is provided through an improved layout of gate drive circuit. The turn-off voltage can be used as 0V or negative, in other words, adjustable to deal with different applications and research needs. A better layout of the power inverter is also proposed to minimize the parasitic parameters of the PCB traces using the benefits of self-magnetic flux cancellation and the imbalance of the parasitics among the three phases is avoided to a great extent. The second version of design has been put into production. Though the experimental results have not been obtained yet, the advantages of the second version can be supported by the simulation results from Ansys Q3D, where the parasitics show a reduction of more than 60%.

5.2 Future work

The proposed research in this thesis can be further extended and some of the directions are discussed as follows:

1) The turn-on and turn-off models proposed for GaN HEMTs can be applied to additional

applications such as DC/DC converters, three-phase inverters to evaluate the efficiency.

2) The designed three-phase inverter can be tested at higher switching frequencies and tested on a motor to verify the performance and be compared with the traditional Si-based inverter with the respect to system efficiency, output harmonics, and so on.

3) The impacts of PCB parasitics can be further investigated. To be more specific, for each segment, the L_D, L_S, $L_{BUS,}$ their influences can be investigated individually.

4) Based on the second version designed, different turn-off voltages can be used to help understand and compare the impacts of 0V off operation and negative off operation in the respect of loss analysis and safe operation of GaN HEMTs.

REFERENCES

[1] Lidow, A. & Strydom, J. & Rooij, M. & Reusch, D, “GaN Transistors for Efficient Power Conversion: Second Edition”, 2014.

[2] B. Ozpineci and L. M. Tolbert, “Comparison of wide-bandgap semiconductors for power electronics applications”, 2004.

[3] X. Ding, Y. Zhou and J. Cheng, "A review of gallium nitride power device and its applications in motor drive," in CES Transactions on Electrical Machines and Systems, vol. 3, no. 1, pp. 54-64, March 2019.

[4] L. Spaziani and L. Lu, "Silicon, GaN and SiC: There's room for all: An application space overview of device considerations," 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, 2018, pp. 8-11.

[5] T. Satoh, K. Osawa and A. Nitta, "GaN HEMT for Space Applications," 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), San Diego, CA, 2018, pp. 136-139.

[6] L. Kou, J. Lu and P. Di Maso, "GaN HEMT Outperforms Silicon in Low Frequency Applications," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 255-260.

[7] M. Notarianni, B. Messant and P. Maynadier, "Using GaN HFET to replace MOSFET in DC/DC for space applications," 2019 European Space Power Conference (ESPC), Juan-les-Pins, France, 2019, pp. 1-3.

[8] K. S. Boutros, R. Chu and B. Hughes, "GaN power electronics for automotive application," 2012 IEEE Energytech, Cleveland, OH, 2012, pp. 1-4.

[9] T. Morita et al., “99.3% Efficiency of three-phase inverter for motor drive using GaN-based Gate Injection Transistors,” The 26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, 2011, pp. 481-484.

[10] D. Han, A. Ogale, S. Li, Y. Li and B. Sarlioglu, "Efficiency characterization and thermal study of GaN based 1 kW inverter," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 2344-2350.

[11] J. Lautner and B. Piepenbreier, “High Efficiency Three-Phase-Inverter with 650 V

GaN HEMTs,” International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2016, pp. 1-8

[12] K. Shirabe et al., "Efficiency Comparison Between Si-IGBT-Based Drive and GaN-Based Drive," in IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 566-572, Jan.-Feb. 2014.

[13] K. Shirabe et al., "Advantages of high frequency PWM in AC motor drive applications," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 2977-2984.

[14] X. Zhang, N. Haryani, Z. Shen, R. Burgos and D. Boroyevich, "Ultra-low inductance phase leg design for GaN-based three-phase motor drive systems," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, 2015, pp. 119-124.

[15] H. Li et al., "Design of a 10 kW GaN-based high power density three-phase inverter," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

[16] M. Cui et al., "Monolithic GaN Half-Bridge Stages With Integrated Gate Drivers for High Temperature DC-DC Buck Converters," in IEEE Access, vol. 7, pp. 184375-184384, 2019.

[17] Y. Zhang, M. Rodríguez and D. Maksimović, "Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages With Integrated Gate Drivers," in IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7926-7942, Nov. 2016.

[18] G. Cantone and F. Pulvirenti, "Integrated solutions and related technologies for gate drivers of GaN transistors," 2020 AEIT International Annual Conference (AEIT), Catania, Italy, 2020, pp. 1-6.

[19] L. S. Mai, S. A. Mussa, A. A. Schwertner and M. F. Schonardie, "A GaN FET Based 1MHz Switching DC-DC Three-Phase Interleaved Point of Load Buck Converter," 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 2020, pp. 421-425.

[20] RichardsonRFPD, “GaN & SiC Technologies for Power Electronics,” Rev.6, February 2019.

[21] G. Deboy, O. Haeberlen and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 2, pp. 89-100, 2017.

[22] P. Sojka, M. Pipiska and M. Frivaldsky, "GaN power transistor switching performance in hard-switching and soft-switching modes," 2019 20th International Scientific Conference on Electric Power Engineering (EPE), Kouty nad Desnou, Czech Republic, 2019, pp. 1-5.

[23] Y. Xiong, S. Sun, H. Jia, P. Shea and Z. John Shen, "New Physical Insights on Power MOSFET Switching Losses," in IEEE Transactions on Power Electronics, vol. 24, no. 2, pp. 525-531, Feb. 2009.

[24] D. Graovac, M. Piirschel, and A. Kiep, "MOSFET power losses calculation using the data-sheet parameters," 2006. [Online]. Available.

[25] J. Guo, H. Ge, Jin Ye and A. Emadi, "Improved method for MOSFET voltage rise-time and fall-time estimation in inverter switching loss calculation," 2015 IEEE Transportation Electrification Conference and Expo, Dearborn, MI, 2015, pp. 1-6.

[26] GaN Systems, Application Brief How to drive GaN Enhancement mode HEMT, Application Note, GN001, Apr 26th, 2016.

[27] GaN Systems, Application Guide Design with GaN Enhancement mode HEMT, Application Note, GN001, Feb 28th, 2018.

[28] R. Hou, J. Xu and D. Chen, "A multivariable turn-on/turn-off switching loss scaling approach for high-voltage GaN HEMTs in a hard-switching half-bridge configuration," 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 2017, pp. 171-176.

[29] Infineon, “High speed DuoPack: IGBT in Trench and Field stop technology with soft, fast recovery anti-parallel diode,” IKW30N60H3 datasheet, Rev.2.2, 12 March 2014.

[30] GaN Systems, “GS66508T, Top-side cooled 650 V E-mode GaN transistor,” datasheet, Rev 200402.

[31] E. A. Jones, F. Wang, D. Costinett, Z. Zhang and B. Guo, "Temperature-dependent

turn-on loss analysis for GaN HFETs," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 1010-1017.

[32] P. Williford et al., "Optimal Dead-time Setting and Loss Analysis for GaN-based Voltage Source Converter," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 2018, pp. 898-905.

[33] B. Sun, Z. Zhang and M. A. E. Andersen, "Switching transient analysis and characterization of GaN HEMT," 2018 3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG), Yi-Lan, 2018, pp. 1-4.

[34] Baliga B J. “Trends in power semiconductor devices”. IEEET rans. Electron Devices. vol. 43, no. 10, pp. 1717-1731, 1996.

[35] Qian Zhao ming, Zhang Jun ming, Sheng Kuang. “Status and development of power semiconductor devices and its applications”.Proceedings of the CSEE, vol. 34, no, 29, pp. 5149-5151, 2014.

[36] Rechard Eden. “Market forecasts for silicon carbide& gallium nitride power semiconductors”. in IEEE Applied Power Electronics Conference, 2012.

[37] Kuzuhara M.Nitride power devices:future perspec-tives”. in Int. RCIQE/CREST joint workshop,Hokkaido University, March, 2010, pp. 1-2.

[38] F. Yang, C. Xu and B. Akin, "Experimental Evaluation and Analysis of Switching Transient's Effect on Dynamic On-Resistance in GaN HEMTs," in IEEE Transactions on Power Electronics.

[39] K. Shirabe et al., "Advantages of high frequency PWM in AC motor drive applications," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 2977-2984.

[40] Z. Lyu, M. Yang, D. Xu, S. Shang and D. Xu, "Design and Research of GaN - Based Motor Drive System with LC Output Filter," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019, pp. 1-6.

[41] K. Shirabe et al., "Efficiency Comparison Between Si-IGBT-Based Drive and GaN-Based Drive," in IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 566-572, Jan.-Feb. 2014.

[42] P. M. Roschatt, S. Pickering and R. A. McMahon, "Bootstrap Voltage and Dead Time Behavior in GaN DC–DC Buck Converter With a Negative Gate Voltage," *in IEEE Transactions on Power Electronics,* vol. 31, no. 10, pp. 7161-7170, Oct. 2016.

[43] P. M. Roschatt, R. A. McMahon and S. Pickering, "Investigation of dead-time behaviour in GaN DC-DC buck converter with a negative gate voltage," *The 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia),* Seoul, 2015, pp. 1047-1052.

[44] P. Skarolek and J. Lettl, "GaN Transistors Cooling Options Comparison," 2019 International Conference on Electrical Drives & Power Electronics (EDPE), The High Tatras, Slovakia, 2019, pp. 323-326.

[45] GaN Systems, PCB Thermal Design Guide for GaN Enhancement Mode Power Transistors, Application Note, GN005 Rev 150212.

[46] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter," in IEEE Transactions on Power Electronics, vol. 29, no. 4, pp. 2008-2015, April 2014.

[47] H. Zhang and S. S. Ang, "Thermal simulation of gallion nitride power packages," 2016 China Semiconductor Technology International Conference, Shanghai, 2016, pp. 1-3.

[48] S. Moeller et al., "Application considerations for Double Sided Cooled Modules in Automotive Environment," CIPS 2020; 11th International Conference on Integrated Power Electronics Systems, Berlin, Germany, 2020, pp. 1-7.

[49] H. Li, et al., "Evaluation of high voltage cascode GaN HEMTs in parallel operation," In Proc. 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 990- 995.

[50] H. Li, et al., "Paralleled Operation of High-Voltage Cascode GaN HEMTs," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 815-823, Sept. 2016.

[51] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," in IEE Proceedings - Electric Power Applications, vol. 153, no. 4, pp. 535-543, July 2006.

[52] L. Xi, "Minimizing Dc Capacitor Current Ripple And Dc Capacitance Requirement

Of The Hev Converter/Inverter Systems," M.S. Thesis, Department of Electrical Engineering, Michigan State University, Lansing, MI, 2012.

[53] Jih-Sheng Lai, H. Kouns and J. Bond, "A low-inductance DC bus capacitor for high power traction motor drive inverters," Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344), Pittsburgh, PA, USA, 2002, pp. 955-962 vol.2.

[54] M. Salcone and J. Bond, "Selecting film bus link capacitors for high performance inverter applications," 2009 IEEE International Electric Machines and Drives Conference, Miami, FL, 2009, pp. 1692-1699.

[55] Kolar, J.W.; Wolbank, T.M.; Schrodl, M.: 'Analytical calculation of the RMS current stress on the DC link capacitor of voltage DC link PWM converter systems', IET Conference Proceedings, 1999, p. 81-89.

[56] Julia Zhang and Lei Jin. Modeling of DC link Capacitor Current Ripple for Electric Vehicle Traction Converter. OTREC-SS-634. Portland, OR: Transportation Research and Education Center (TREC), 2010.

[57] M. J. Mnati, J. K. Abed, D. V. Bozalakov and A. Van den Bossche, "Analytical and calculation DC-link capacitor of a three-phase grid-tied photovoltaic inverter," 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), Doha, 2018, pp. 1-6.

[58] P. M. Roschatt, S. Pickering and R. A. McMahon, "Bootstrap Voltage and Dead Time Behavior in GaN DC–DC Buck Converter With a Negative Gate Voltage," in IEEE Transactions on Power Electronics, vol. 31, no. 10, pp. 7161-7170, Oct. 2016.

[59] P. M. Roschatt, R. A. McMahon and S. Pickering, "Investigation of dead-time behaviour in GaN DC-DC buck converter with a negative gate voltage," The 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, 2015, pp. 1047-1052.

[60] Analog Devices, High Voltage, Isolated Gate Driver with Internal Miller Clamp, 2 A Output, Datasheet, Rev. 0, 2016.

[61] Silicon Labs, Isolation Bootstrap Web Calculator, online resource.

[62] Silicon Labs, AN486: High-Side Bootstrap Design Using ISODrivers in Power

Delivery Systems, Rev. 0.3, January, 2020.

[63] ON Semiconductor, AN-6076 Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC, Application Note, Rev. 2, January, 2018.

[64] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed. New York, NY, USA: Springer, 2001.

[65] Chi-Tsong Chen, Analog and digital control system design : transfer-function, state-space, and algebraic methods, Saunders College Publishing, 1993.

[66] GaN Systems, GS66516T Top-side cooled 650 V E-mode GaN transistor, Datasheet, Rev. 200402.

[67] O. Kreutzer, B. Eckardt, and M. Maerz, “Optimum gate driver design to reach SiC-MOSFETs full potential—Speeding up to 200 kV/μs,” in Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl., Blacksburg, VA, USA, 2015, pp. 41–46.

[68] Y. Niu, Y. Huang, C. Chen and Y. Chen, "Design Considerations of the Gate Drive Circuit for GaN HEMT Devices," 2018 Asian Conference on Energy, Power and Transportation Electrification (ACEPT), Singapore, 2018, pp. 1-6.

[69] A. B. Jørgensen, S. Bęczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jørgensen and S. Munk-Nielsen, "A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices," in IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2494-2504, March 2019.

[70] T. LaBella, B. York, C. Hutchens and J. Lai, "Dead time optimization through loss analysis of an active-clamp flyback converter utilizing GaN devices," 2012 IEEE Energy Conversion Congress and Exposition, Raleigh, NC, 2012, pp. 3882-3889.

[71] Z. Liu, X. Huang, F. C. Lee and Q. Li, "Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT," in IEEE Transactions on Power Electronics, vol. 29, no. 4, pp. 1977-1985, April 2014.

[72] Z. Liu, X. Huang, W. Zhang, F. C. Lee and Q. Li, "Evaluation of high-voltage cascode GaN HEMT in different packages," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, USA, 2014, pp. 168-173.

[73] H. Daou, M. Ameziani, D. Lhotellier, F. Costa, M. Petit and E. Labouré, "Dynamic electric model for IGBT power module based on Q3D® and Simplorer®: 3D Layout

design, stray inductance estimation, experimental verifications," 2016 International Conference on Electrical Systems, Toulouse, France, 2016, pp. 1-6.

[74] Texas Instruments, “Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN”, Application Report, SNOAA36, February 2019.

[75] A. Letellier, M. R. Dubois, J. P. F. Trovão and H. Maher, "Calculation of Printed Circuit Board Power-Loop Stray Inductance in GaN or High di/dt Applications," in IEEE Transactions on Power Electronics, vol. 34, no. 1, pp. 612-623, Jan. 2019.

[76] I. Kovacevic-Badstuebner, R. Stark, U. Grossner, M. Guacci and J. W. Kolar, "Parasitic Extraction Procedures for SiC Power Modules," CIPS 2018; 10th International Conference on Integrated Power Electronics Systems, Stuttgart, Germany, 2018, pp. 1-6.

[77] B. Sun, Z. Zhang and M. A. E. Andersen, "Research of PCB Parasitic Inductance in the GaN Transistor Power Loop," 2019 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Taipei, Taiwan, 2019, pp. 1-5.

[78] C. Che, H. Zhao, Y. Guo, J. Hu and H. Kim, "Investigation of Segmentation Method for Enhancing High Frequency Simulation Accuracy of Q3D Extractor," 2019 IEEE International Conference on Computational Electromagnetics (ICCEM), Shanghai, China, 2019, pp. 1-3.

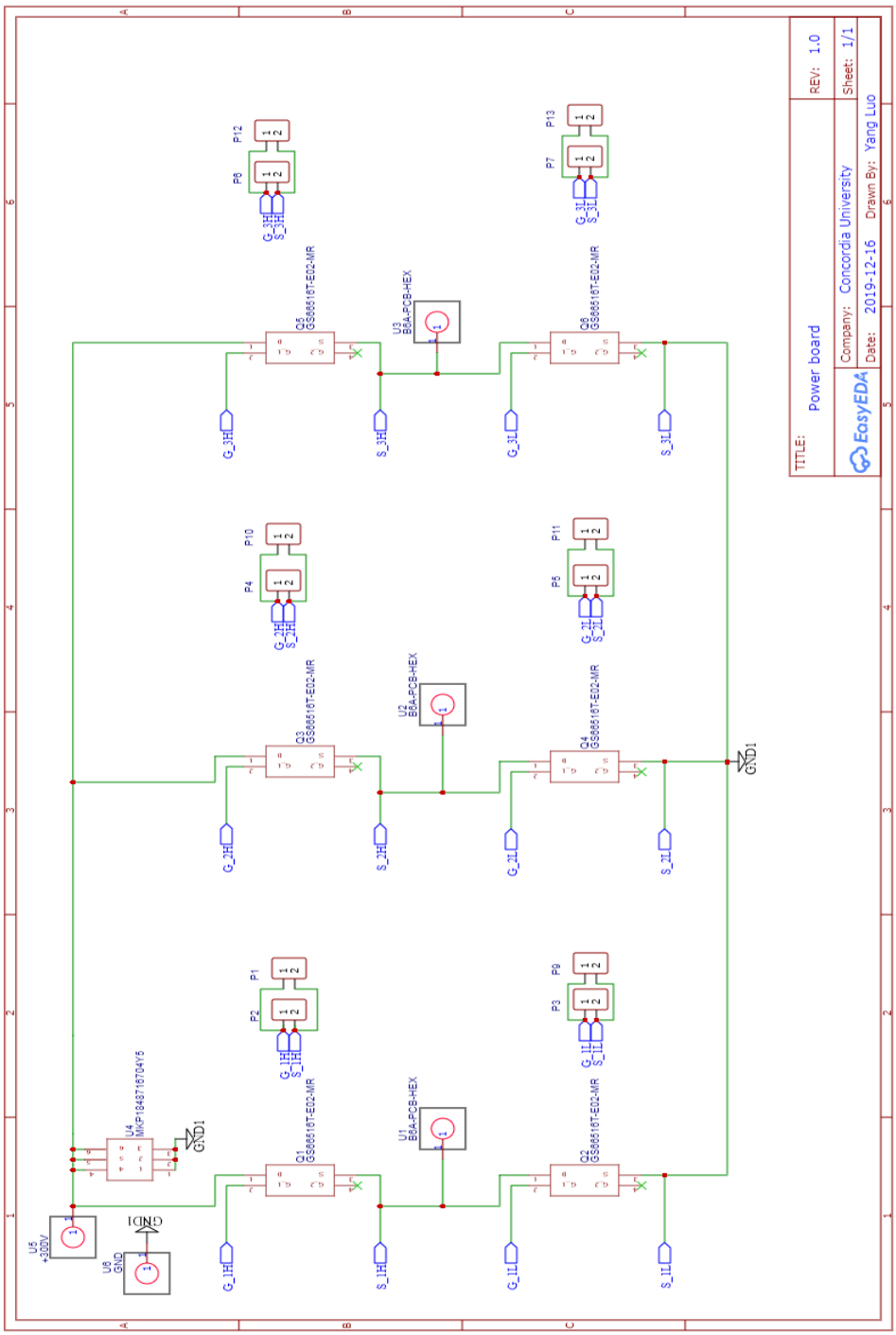
[79] J. P. Kozak et al., "An Analytical Model for Predicting Turn-ON Overshoot in Normally-OFF GaN HEMTs," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 99-110, March 2020.

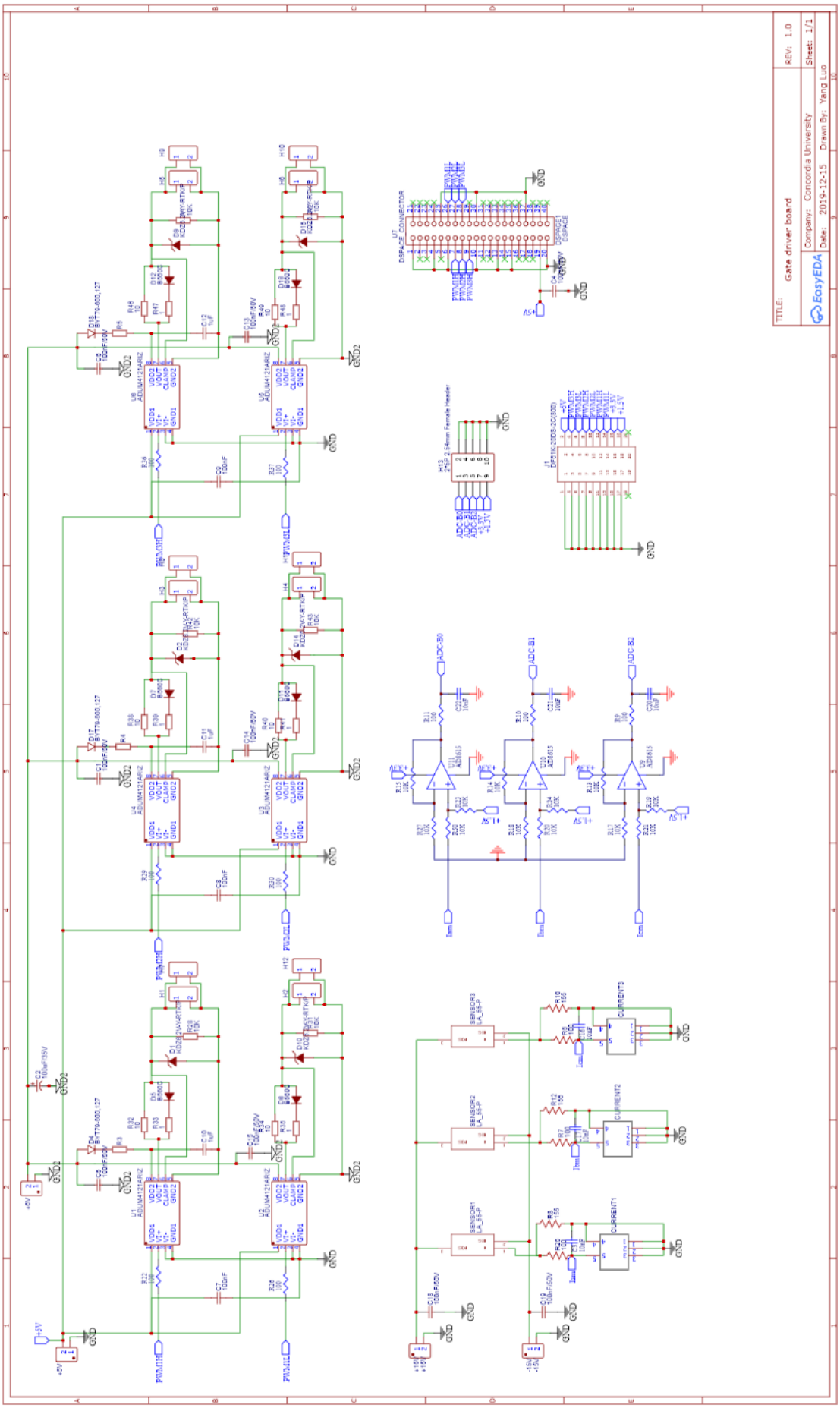
[80] T. Liu, R. Ning, T. T. Y. Wong and Z. J. Shen, "Modeling and Analysis of SiC MOSFET Switching Oscillations," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 747-756, Sept. 2016.

[81] T. Liu, R. Ning, T. T. Y. Wong and Z. J. Shen, "Equivalent circuit models and model validation of SiC MOSFET oscillation phenomenon," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016, pp. 1-8.

APPENDIX

1. Schematics

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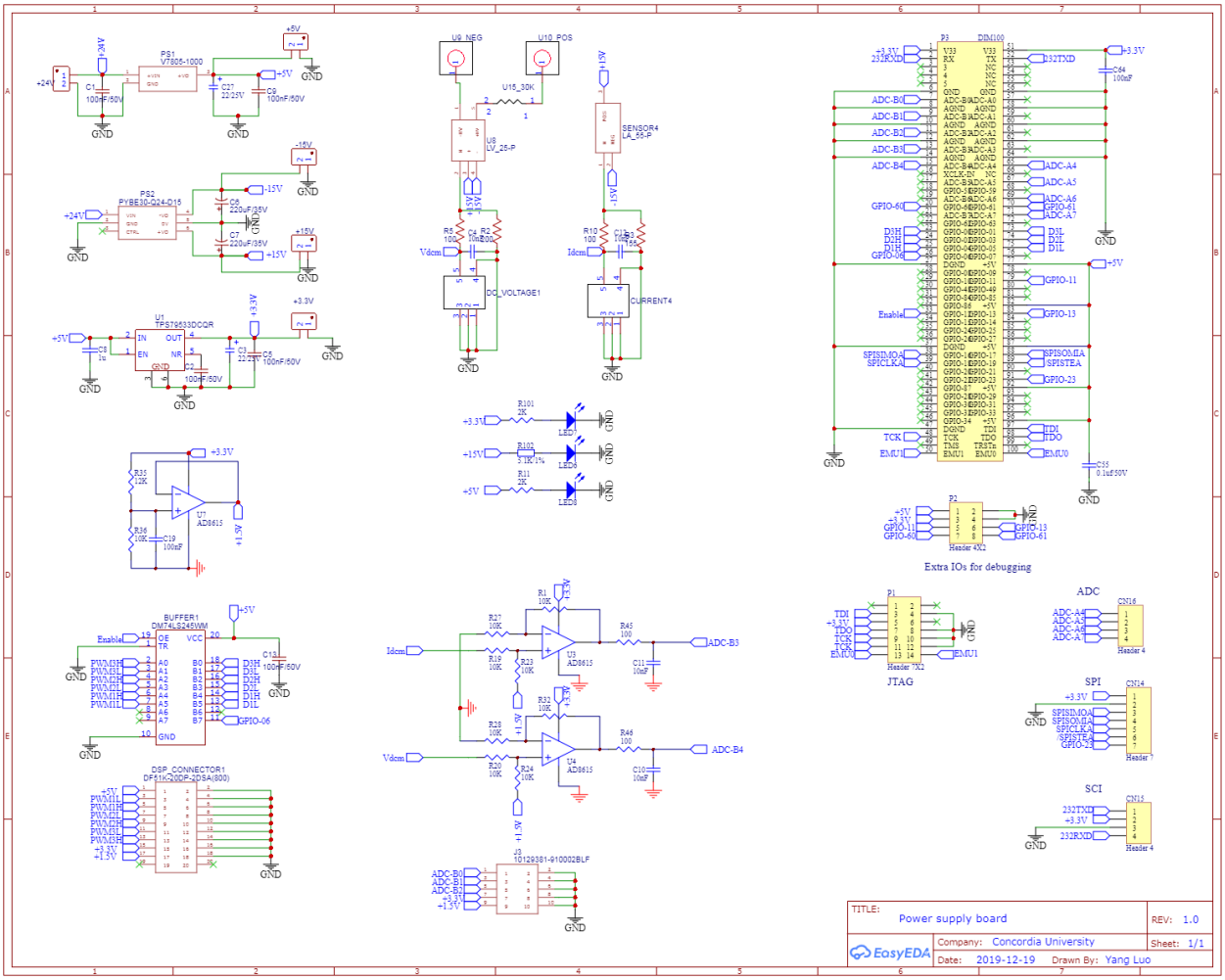
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U8
LV_25-P
SENSOR4
LA_55-P
DC_VOLTAGE1
CURRENT4
LED7
LED6
LED8
U7
AD8615
BUFFER1
DM74LS245WM
DSP_CONNECTOR1
DF51K-100P-2DSA(800)
U3
AD8615
U4
AD8615
J3
10129381-910002BLF
P3
DIM100
P2
Header 4X2
Extra IOs for debugging
P1
Header 7X1
JTAG
ADC
CN16
Header 4
SPI
CN14
Header 7
SCI
CN15
Header 4
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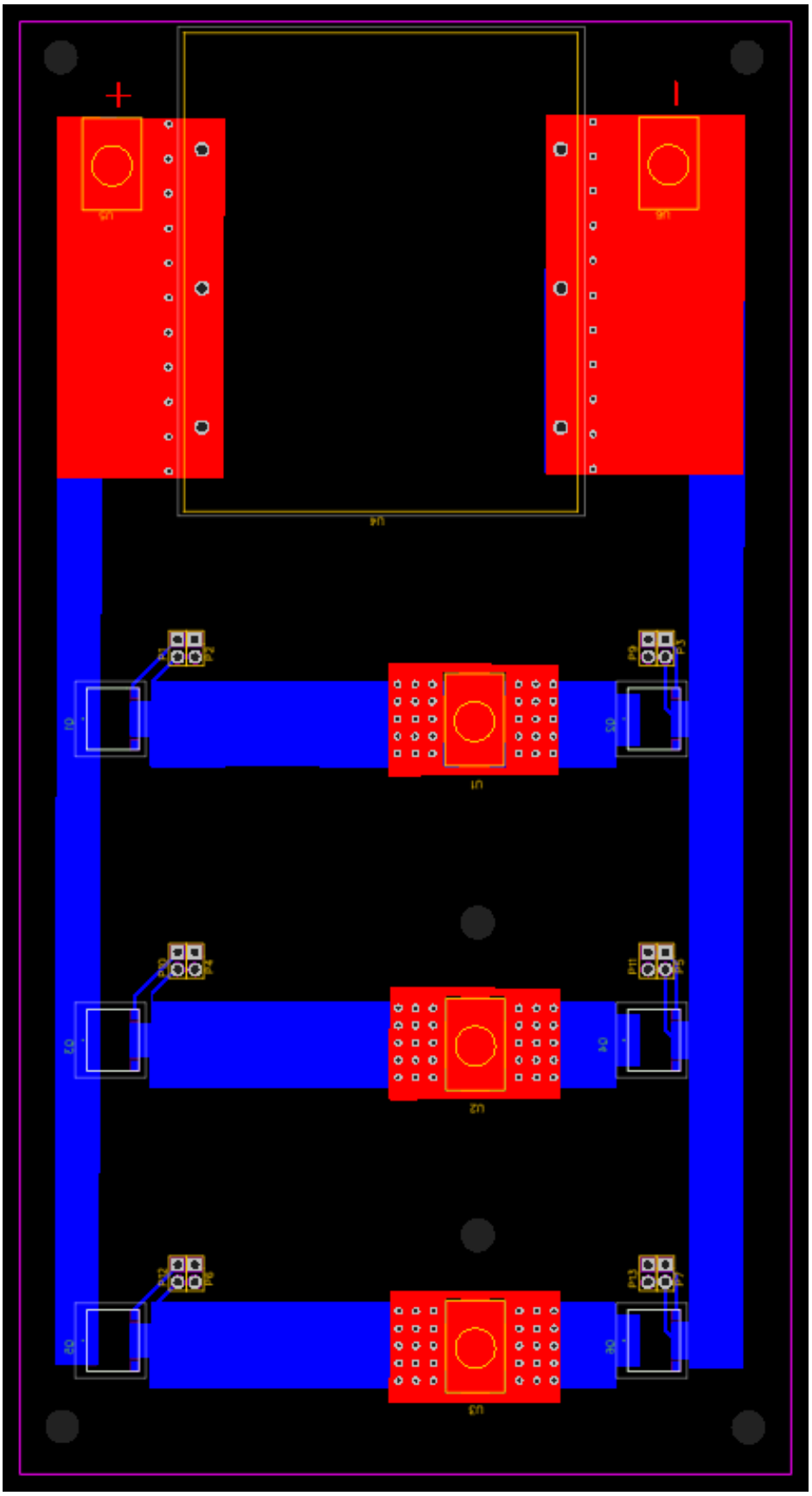
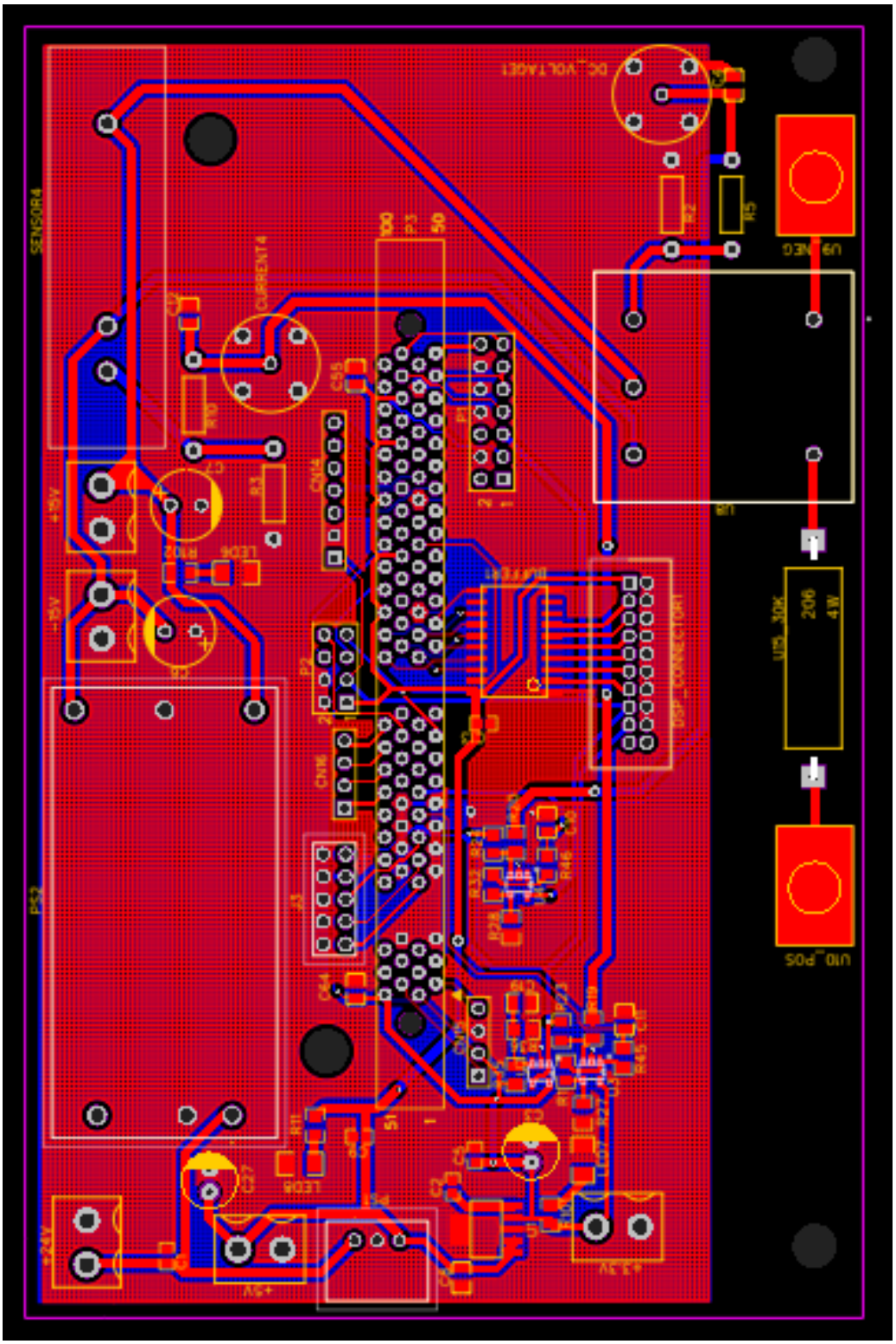
2. PCBs

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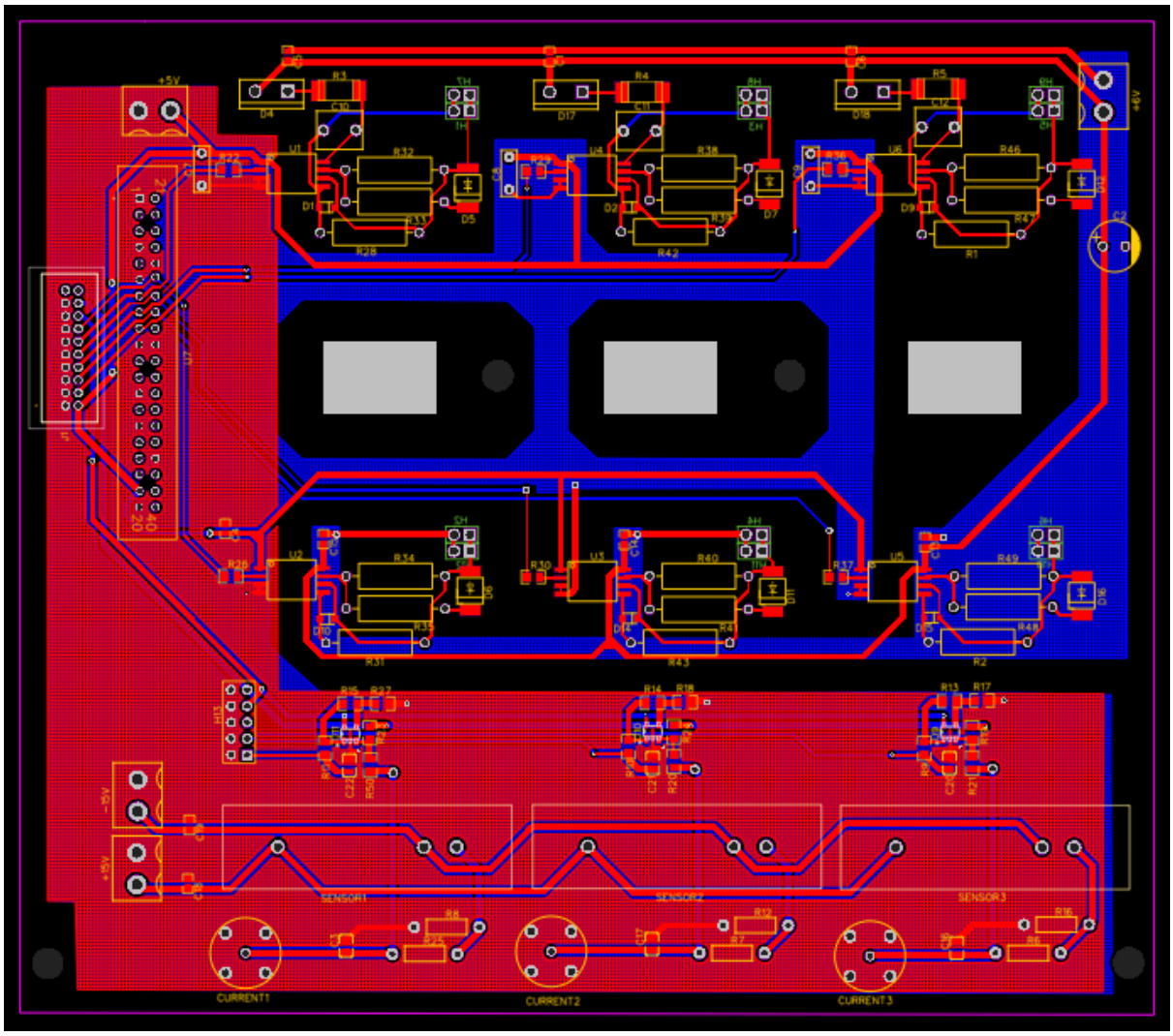
4W
+15V
-15V
+5V
+24V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+6V
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CURRENT2
CURRENT3
SENSOR1
SENSOR2
SENSOR3