Analysis and Design of Series LC Resonant-Pulse Assisted Soft-Switching Current-Fed DC/DC Converters

Swati Tandon

A Thesis

In the Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy (Electrical and Computer Engineering) at

Concordia University

Montreal, Quebec, Canada.

May 2021

CONCORDIA UNIVERSITY

SCHOOL OF GRADUATE STUDIES

This is to certify that the thesis prepared

By: Swati Tandon

Entitled: Analysis and Design of Series LC Resonant-Pulse Assisted Soft-Switching Current-fed DC/DC Converters

and submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy (Electrical and Computer Engineering)

complies with the regulations of this University and meets the accepted standards with respect to originality and quality.

Signed by the final examining committee:

_____ Chair
Dr. Yuhong Yan

_____ External Examiner
Dr. Ambrish Chandra

_____ External to the Program
Dr. Jun Yan

_____ Examiner
Dr. Luiz A. C. Lopes

_____ Examiner
Dr. Pragassen Pillay

_____ Supervisor
Dr. Akshay Kumar Rathore

Approved by: _____
Dr. Yousef R. Shayan, Chair of Department

May 20th, 2021 _____

Date of Defence Dr. Mourad Debbabi, Interim Dean
Gina Cody School of Engineering and Computer Science

ABSTRACT

Analysis and Design of Series LC Resonant-Pulse Assisted Soft-Switching Current-Fed DC/DC Converters

Swati Tandon, Ph.D.

Concordia University, 2021

The accelerating pace of electrification via renewable energy sources is shifting focus towards de-carbonization and distributed generation with the potential to combat increasing environmental crisis and to promote sustainable development. Renewable technologies have the potential to fulfil the electricity demand locally which eliminates the unwanted conversion stages, promoting DC microgrid concept, ultimately lowering the energy costs and easy energy access.

Alternative energy sources such as solar photovoltaic (PV) and fuel cell along with energy storage systems are promising for DC microgrid applications. However, the effective integration of these alternative energy sources still remains a challenge due to their low voltage output, unregulated and intermittent characteristics issuing a requirement of a dedicated power conditioning unit. To revolutionize the way these alternative sources are interfaced with a high voltage DC microgrid or to the conventional ac grid, dc/dc converters are expected to be power-dense, compact and extremely efficient. Current-fed dc/dc converters have strong application potential owing to their inherent merits.

Accomplishing the abovementioned objectives together with distinct merits offered by current-fed circuits, this thesis aims to exploit the quasi-resonance concept for achieving soft-switching and smooth commutation of the semiconductor switching devices. The proposed quasi resonant approach that utilizes the leakage inductance of transformer and a high frequency series resonant capacitor for a short period also termed as ‘resonant-pulse’, has been investigated in various current-fed converter topologies. Proposed converter class emphasize on simple and efficient design, without the use of additional snubber circuits and eliminates device turn-off voltage spike, which is a historical problem with traditional current-fed converters.

In this thesis, at first the proposed series resonant-pulse concept is implemented in single-phase current-fed push-pull and half-bridge configuration. The converter operation, control and performance are investigated for low voltage high current specifications. These converter configurations demonstrate good efficiency and compact structure with only two switching devices and simpler gate control requirement because devices having common ground with power supply.

The idea has then been extended to modular current-fed full-bridge topology. The proposed series resonant-pulse assisted converter enables wide range ZCS and turn-off spike elimination across the semiconductor switches. Modularity of this converter allows easy scalability for high power and voltage levels with significantly lower current and voltage stress, making it suitable for relatively higher power industrial applications.

Lastly, to achieve high power capability with high density, three-phase current sharing current-fed topology utilizing series resonant-pulse feature has been studied and investigated in detail. The proposed three-phase topology combines the benefits of current-sharing primary and load adaptive series resonant-pulse. As a result, these converters demonstrate promising attributes such as wide ZCS operation, reduced filtering requirement, lower component count, lower conduction losses etc.

Acknowledgment

First and foremost, I would like to express my sincere gratitude and immense appreciation to my supervisor, Prof. Akshay Kumar Rathore for his continuous support and guidance throughout this course. His scientific knowledge, critical thinking and passion for research has always inspired me and has been instrumental in successfully completing this programme. I am thankful for his patience and motivation for this research and writing this thesis.

I would also like to thank my doctoral committee members, Prof. Pragasen Pillay, Prof. Luiz A.C. Lopes, Prof. Jun Yan for their time, encouragement, and support in improving my thesis.

I gratefully acknowledge PEER lab and Concordia University (CU) for the top-notch research facility, and conducive environment which paved way for a successful career.

I extend my gratitude to Dr. Sivanagaraju, Dr. Mathews, Karan, and Abhinandan for their support in building experimental set-up, and for the insightful research discussions. Heartfelt thanks to my colleagues Venkata, Ronak, Dwaipayan, Koyelia for their constant moral support and kind assistance.

I would like to express my gratitude to my beloved parents, Mr. Arjun Dev Tandon and Mrs. Suman Tandon for being a driving force and also motivating me in pursuing doctoral studies. I am especially grateful to my partner Nitish for his unconditional love and support throughout my thesis. Also, I would like to thank my brother Yash and my sister Divya for always being there and encouraging me throughout this journey. Last but not the least, I would also like to remember my Grandmother Mrs. Roshni Tandon, for the blessings and love she has and will bestow upon me eternally from far above. To all of them, I dedicate this thesis.

Table of Contents

List of Tables

List of Figures

List of Symbols

V_{in}	Input Voltage
V_o	Output Voltage
L_{in}, L_1, L_2, L_3	Input inductor/boost Inductors
DT_s	Switch On-Time
D	Duty Cycle
$I_{O,Avg}$	Output Average Current
I_{in}	Input Current
M	Converter voltage Gain
$V_{o,ripple}$	Output Voltage Ripple
$C_o, C_{o1,} C_{o2}$	Output Capacitors
$L_r, L_{r1}, L_{r2}, L_{r3}$	Resonant Inductors
$C_r, C_{r1}, C_{r2}, C_{r3}$	Resonant Capacitors
f_s	Switching Frequency
f_r	Resonant Frequency
$R_L \; and \; R_{Load}$	Load Resistance
P_o	Converter Output Power
V_{ds}	Switch Voltage
i_{Lr}	Resonant Current
$I_{Sw,rms}$	Switch rms Current
T, T_1, T_2, T_3	High frequency transformer
Z_o, Z_r	Input Impedance
n	Transformer turns ratio
V_{Cr}	Resonant Capacitor Voltage
$1: n: n$	Transformer turns ratio
V_{AB}	Terminal Voltage across A and B
L_{lk}	Transformer leakage inductance

$R_{dS,on}$	Switch drain-to-source on resistance (front end)
$P_{c,limit}$	Inductor core loss limit, mW/cm^3
V_e	Effective core volume, cm^3
V_f	Buck-boost diode forward voltage
R_d	Buck-boost diode resistance
V_{gs}	Gate-to-source voltage
C_{oss}	Switch output capacitance

CHAPTER 1:

INTRODUCTION

1.1 Background

Global electricity consumption is rising at an unprecedent pace driven by increasing prosperity and urbanization in the emerging world. Even today, the majority of the energy demand is derived from the conventional fossil fuels, mainly coal and oil. Record high greenhouse gases and other toxic emissions from the excessive use of the fossil fuels, have resulted in dramatic climate change with the elevated levels of the air pollution [1]-[2]. According to the EIA report [3], the transportation and industrial sectors have been the primary energy consuming sectors in the United States and in other developed economies since 2000, with petroleum being the dominant fuel source as shown in Fig.1.1. As per the statistics, renewable integration remains minimum in the transportation sector. Moreover, major part of the world's total energy consumption and greenhouse gas emissions is driven by countries like China, the United States and India as highlighted in Fig.1.2 [4]. However, relatively slower growth in global energy consumption (1.3%) and carbon emissions is observed recently as compared to the historic high records in 2018 (2.8%) as witnesses in Fig.1.3 [5]. As a result, the climate change remains a major concern due to the upward trend in global CO_2 emissions and fossil fuel depletion.

This arises an urgent need to put a tenacious effort on bringing down the global emissions and resolving energy crisis. Therefore, today's energy mix is striving to shift focus from a dominant use of coal/petroleum to non-polluting renewable sources like solar, wind, geothermal along with other biofuels. Renewable sources are considered clean, inexhaustible and increasingly competitive for modern sustainable energy solutions. Progress in renewable sector is transforming the current energy systems around the globe. Despite increase in the share of renewables from 9.3% to 10.4%, renewable integration continues to face challenges in achieving a larger share of global electricity generation, due to the technology limitation, intermittency, lower efficiency as well as lenient policy measures [6]-[7].

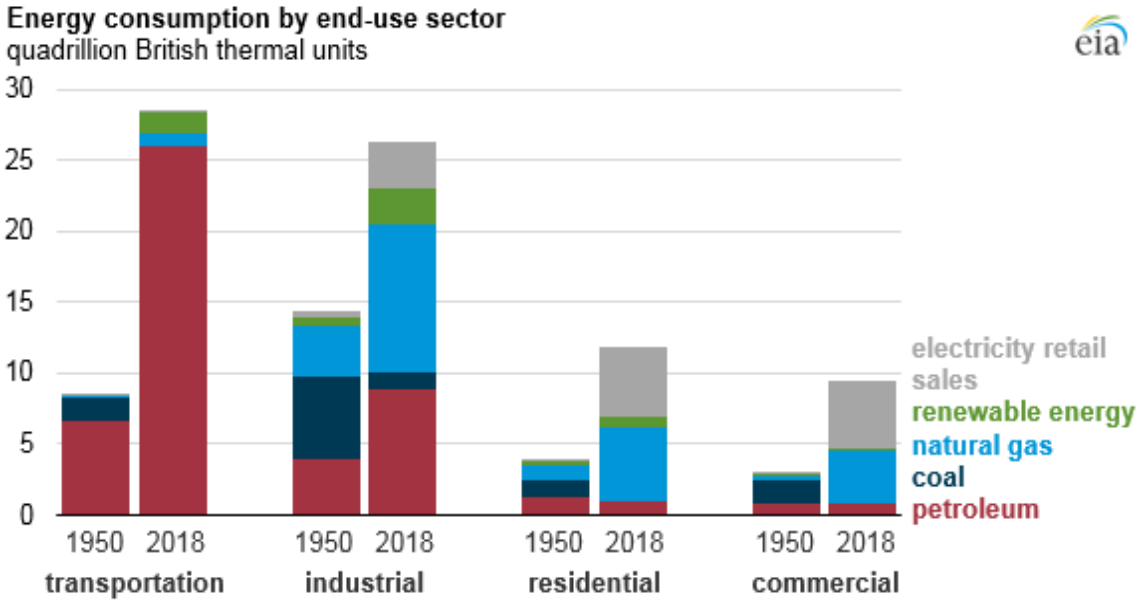


Fig. 1.1 US energy consumption by end-use sector (Source: EIA report).

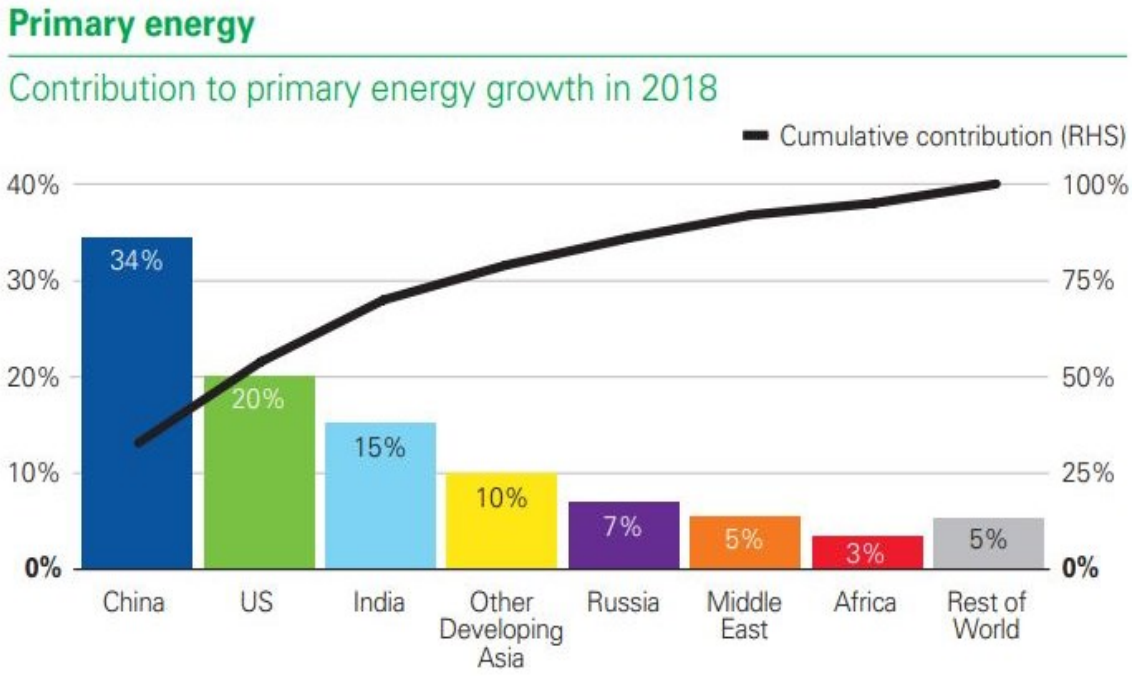


Fig. 1.2 Contribution to total World's energy consumption (Source: BP Statistical Review of World Energy).

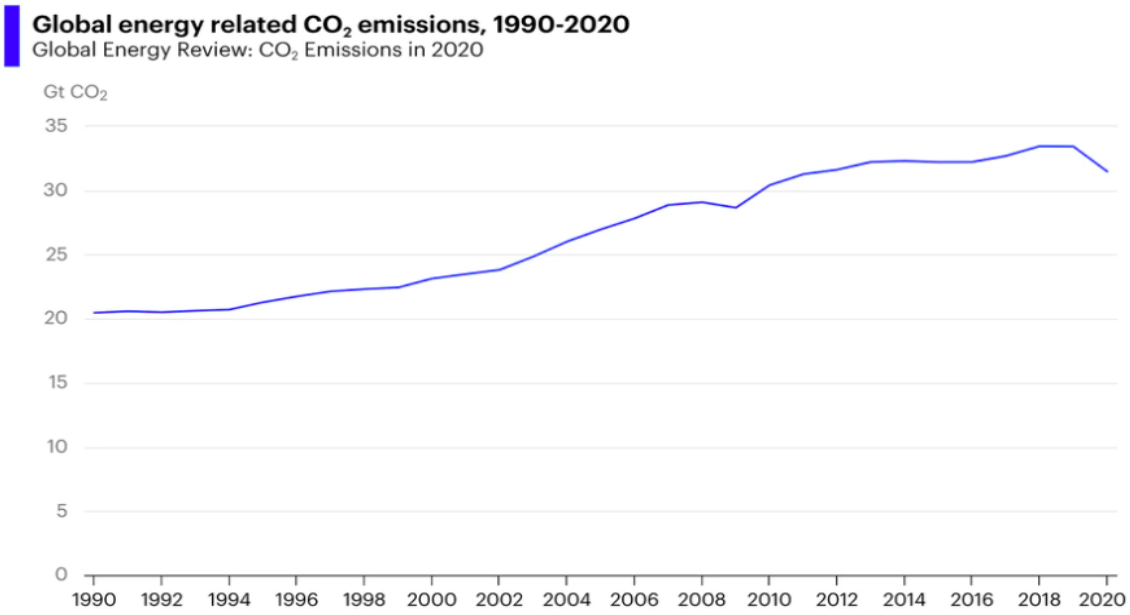


Fig. 1.3 Global energy related carbon emissions (source: International Energy agency 2021 release).

This calls for a coalition encompassing advanced renewable energy technologies, and increased proclivity to switch to low-carbon energy solutions, incentivized adoption, energy policies and societal preferences [8]-[9]. The restructuring of the global energy system to decarbonize the current energy scenario can be possible in the following ways;

Shift towards low-carbon electricity generation with reduced carbon emission per unit energy displacing coal/oil with other non-conventional energy sources.

(i) Shift towards clean mobility by replacing petroleum with electricity.

(ii) Fast deployment of low-cost low-carbon energy solutions and battery technologies to offer easy energy access in low-income countries.

(iii) Fuel diversity, competitive price, localized generation, with increasing installations

With these measures in place, it has been projected that by year 2050, more than 40% of the global electricity demand would be fulfilled by the renewable energy sources depicted in Fig. 1.4 [10]. As in the previous year 2019, the highest ever annual increment in global renewable power capacity is recorded to be more than 200 GW with a growth rate three times of the fossil fuel growth as shown in Fig. 1.5 [11]-[12]. Among all, solar photovoltaic (PV) has been the mainstream renewable energy source with more than 50% share (≈115 GW), followed by

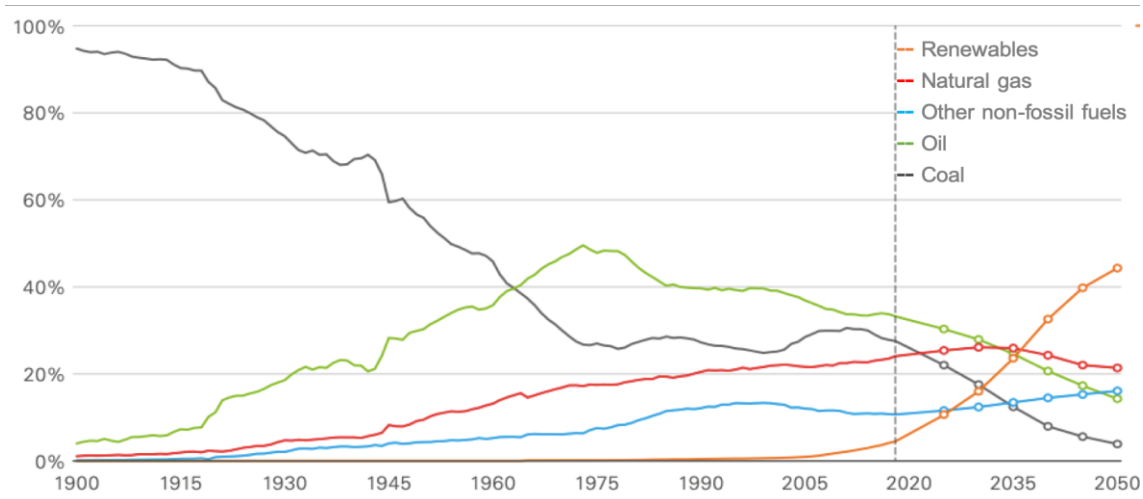


Fig. 1.4 Percentage share of different fuels in global energy consumption.

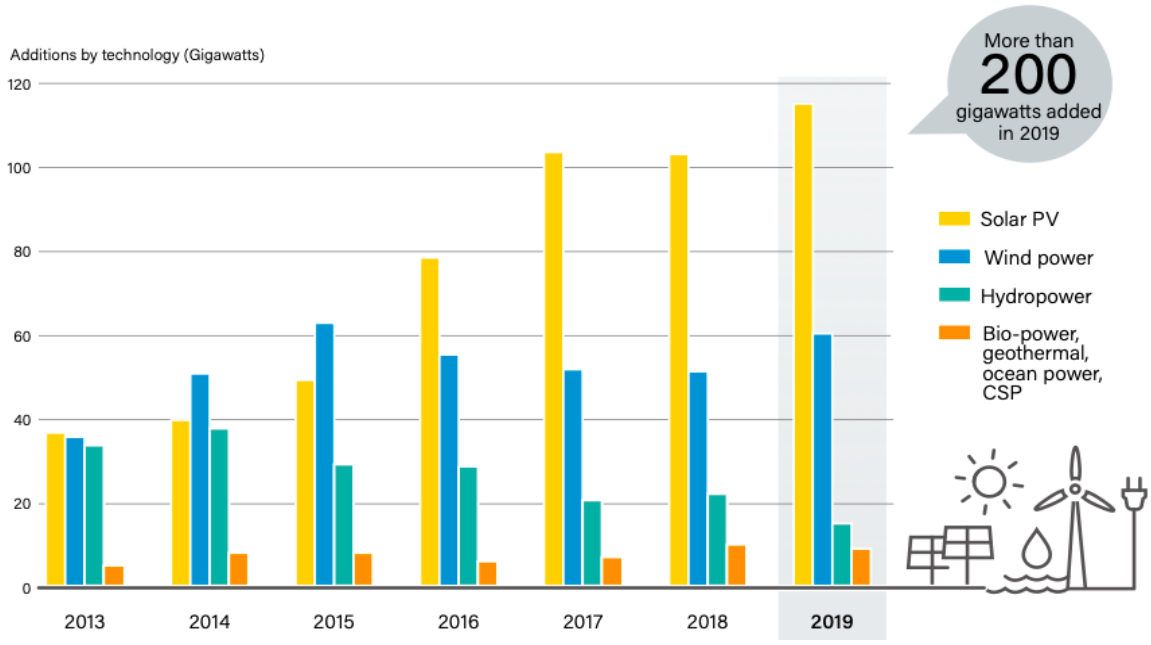


Fig. 1.5 Annual additions in renewable energy capacity by technology (source REN21).

wind energy with 30% share and hydropower with about 8% contribution. The global total solar PV capacity of 627 GW has been recorded in 2019, raising the global total installed capacity to 2,588 GW. Accelerated development in the renewable power sector is continued to be influenced by significant reduction in cost/kW, rising electricity demand, growing awareness, government policy and regulatory frameworks [12].

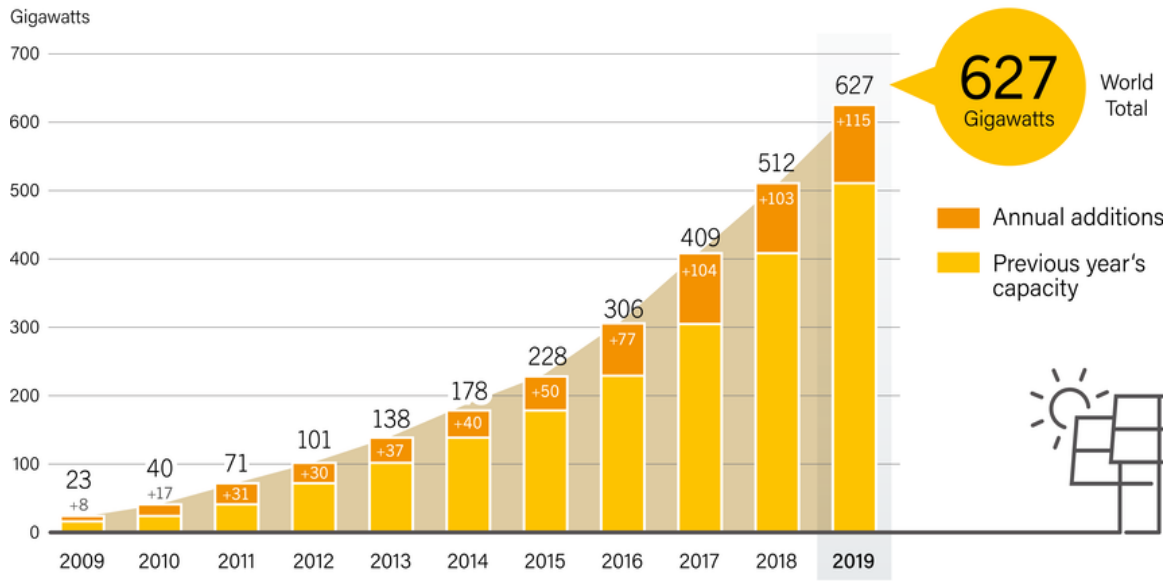


Fig. 1.6 Global solar PV installed capacity

1.2 Architecture of DC Microgrid /Nanogrid System

Driven by a laser-like focus on decarbonizing power generation and lower transmission cost, small-scale distributed energy systems are becoming popular with rapid integration of renewable power generation, battery storage, and modern dc-loads such as electric vehicles (EVs), data centers, etc. [13]-[14]. Moreover, localized installations and investment in clean energy technology have consistently scaled-up to tackle the impact of global climate change and ease of energy access in rural part of the world. Distributed generation by means of microgrids or conventional grid-connected application offers plethora of benefits that accelerate the global energy transition to a cleaner and sustainable fuel [15]-[18].

A typical microgrid architecture is shown in Fig. 1.7. Microgrids can be uniquely controlled when operated in standalone mode or in liaison with the main grid [19]-[20]. In present energy scenario, solar PV enabled microgrid systems are among the most competitive choices for the low-to-medium power residential, commercial and industrial applications [21]. Power from the low voltage renewable energy sources can be extracted to feed high voltage dc microgrid (380V) driving popular dc-loads such as modern data centers, EV charging centers, etc. Microgrid can also drive utility-scale solar inverter, UPS and motor drive applications with

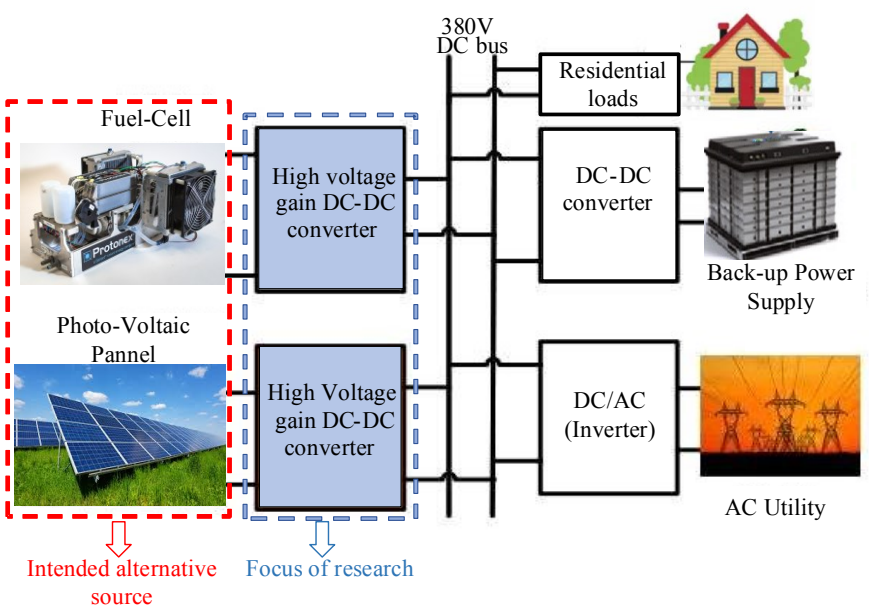


Fig. 1.7 Architecture of a typical microgrid system.

an additional inversion stage at 380 V intermediate dc link. The use of energy storage is critical for seamless power transfer with sources having inherent intermittent characteristics [22]-[24]. Moreover, having an energy storage system is a desirable feature even in grid connected system to prevent grid instability. In addition, small-scale decentralised generation with auxiliary energy storage system adds greater reliability and grid flexibility by providing backup power during grid interruptions and blackouts. The transition to clean energy system gives a boost to the local economies and benefit people across the world while reducing reliance on the conventional energy systems [25]-[27].

However, owing to the intermittent and peculiar characteristics of the low voltage renewable sources, their effective utilization is mostly limited by the conversion technologies and interfacing system [28]-[30]. To establish safe and efficient interconnection, it is necessary to carry out extensive research focusing on novel dc-dc interface to adapt to the inherent characteristics and seasonal variability of the renewable energy sources like solar PV/Wind [31]-[37]. Moreover, to match the voltage profile of the source and the load in a microgrid system, high voltage conversion ratio is required which cannot be achieved by non-isolated boost converters. As a result, a high frequency (HF) transformer isolated DC-DC converter becomes an integral part to interface low voltage sources to a high voltage DC microgrid, to account for the desired voltage gain and safety isolation between the converter

and utility line [38]-[39]. Furthermore, the most preferred PV/Fuel cell enabled systems are 30V-48V to deliver domestic power level, reduced cost and scalability. Therefore, this range is chosen for investigating the PV/fuel cell interfacing [40]-[41].

Besides, the cost of electricity from solar PV and other clean energy sources has fallen by an astounding number in the last decade, which in turn has accelerated the growth for distributed generation market offering promising solutions for the microgrid applications. While there is an increasing need to revolutionize the distributed energy system with eco-friendly sources, the technology interface is also required to be as efficient and effective as possible in terms of the cost and performance.

1.3 Challenges and Key Requisites of Low Voltage Non-Conventional Energy Sources

Despite numerous advantages, integration of solar PV/fuel-cells for microgrid applications experiences several operational challenges due to the obvious reasons of low dc output voltage, intermittent source profile with wide source voltage oscillation, complex control, seasonal variability, low reliability and high per unit cost. Moreover, given the ease of accessibility, high energy density, storage and transport capability, fuel cells are considered equally competitive clean energy source. As a result, dc-dc converters act as the key interfacing unit to effectively integrate the low-voltage renewable energy sources having the following features [42]-[43].

a) High voltage gain capability

Owing to the low dc voltage output (30-48V) from solar PV panel or fuel cell panel due to the operating characteristics, these sources cannot directly feed the high dc voltage (≈380V) required by the microgrid or distributed energy system. Therefore, high voltage gain (typically >10) is required to translate the low level of solar PV/fuel cell stack voltage into the high voltage at the dc bus.

b) Variability in source voltage

Unregulated and discontinuous DC output voltage from a typical solar PV array depends upon the available solar irradiance, ambient temperature and other factors whereas variable fuel inflow is responsible in case of a fuel-cell stack. Therefore, dc-dc interface must ensure satisfactory operation against wide source voltage variation.

c) Low input current ripple

Operating characteristics of these sources are highly influenced by the magnitude of the input current ripple. As current ripple increases, the average PV power reduces due to the loss of the maximum power point tracking (MPPT) while lifetime of the fuel-cell system is greatly affected along with its deteriorated performance and low efficiency.

d) Galvanic isolation

High frequency galvanic isolation allows improved safety, with reduced insulation and thermal requirements particularly in case of utility interconnection. Moreover, isolated dc-dc converters can easily deliver much higher voltage/current gain with additional design flexibility.

e) High density and high efficiency

To improve power density, higher switching frequency is preferred to realize the smaller size magnetics and filters, which in turn results in compact, low-cost and light-weight converter. However, higher switching frequency operation is limited by higher switching losses in the semiconductor devices arising the need for soft switching techniques.

f) Control flexibility and modularity

Dc-dc converter with lower switching device count results in better control flexibility due to reduced control logic generation and gate drive requirement. Moreover, modular structures are preferred with the ability to meet high power requirement and easy implementation.

1.4 Survey of DC/DC Converter Topologies for Low-Voltage High-Gain Applications

With the advancement in power electronics and the semiconductor devices, interfacing dc-dc converters with unique modulation and control are effectively exploited to harness maximum power from the low voltage renewables in hybrid microgrid system. This Section studies the literature on the dc/dc converter topologies. Based on the source functionality and type, they can be broadly classified into two major categories: Voltage-fed and Current-fed converters. Further, voltage fed and current fed converters can be classified into: Non-isolated and Isolated converters, Pulse width modulated (PWM) and Resonant converter, Unidirectional and Bidirectional converters [44]-[45]. This Section primarily focuses on the unidirectional isolated converter topologies suitable for solar PV or fuel cell integration.

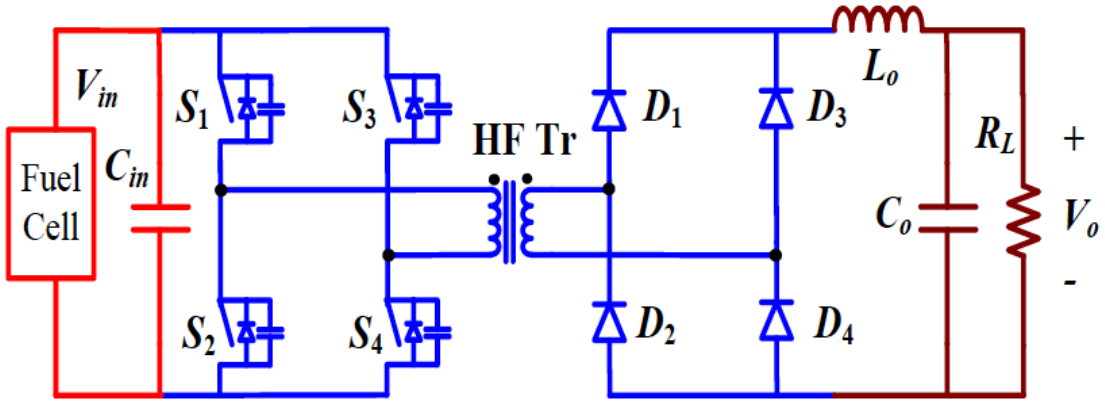
1.4.1 Voltage-fed Converters

Voltage-fed converters are typically driven by a constant DC voltage source or a battery. These converters exhibit buck-type characteristics and therefore, are preferred choice for fractional voltage gain (step-down) applications. These converters have large input current ripple due to high-pulsating/discontinuous input current and hence, require a large filter capacitor across the input. Among the isolated voltage-fed topologies, flyback and forward converters are a) single-ended voltage-fed converters with a transformer core flux swings in one quadrant only with a risk of transformer saturation, while b) double-ended converter topologies like half-bridge, full-bridge and push-pull have improved transformer utilization with flux swing occurring in two quadrants resetting the flux [46]-[48].

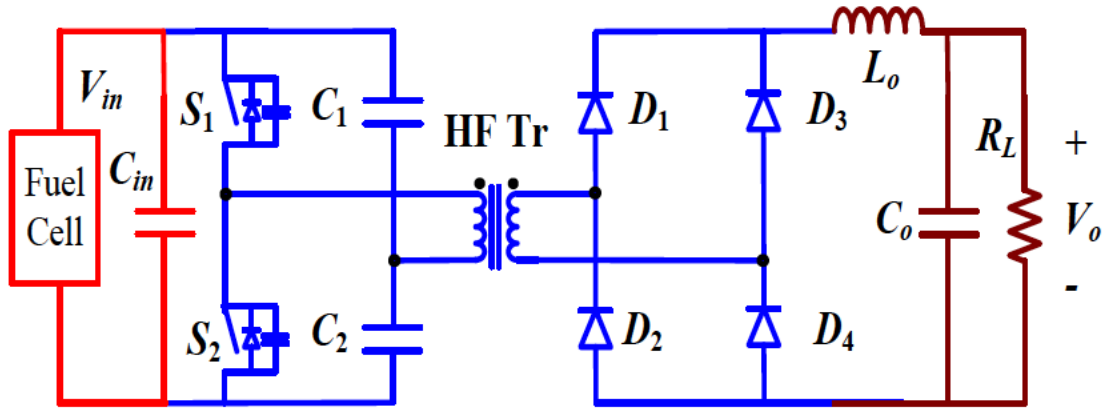
Therefore, flyback and forward converters are better suited for low power applications [49]. At high power level, transformer with large air gap would be required leading to higher leakage flux with extremely low conversion efficiency and relatively larger size and weight. However, these converters exhibit unique features such as swift dynamic response, relatively less complex design and easier converter start-up and shut-down operations [50]-[53].

For low voltage high current applications, double-ended popular voltage-fed topologies shown in Fig 1.8 (half-bridge, full-bridge and push-pull) are preferred over single-ended topologies. Half-bridge and push-pull configurations are meritorious owing to the low switch count, and reduced gate drive requirement. While having low component's count, the push-pull configuration does not utilize transformer core fully with $\sqrt{2}$ times higher kVA rating and higher semiconductor device stress ($2V_{\text{in}}$) due to the presence of the centre-taped transformer. Whereas the full-bridge configuration allows effective transformer utilization with easy scalability and modularity for high power applications. However, in order to be used for low voltage renewable applications (solar PV/ fuel-cell), these converters fully depend upon the high-frequency transformer to obtain the desired voltage gain due to inherent buck-derived nature, resulting in higher kVA and higher turns ratio [54]-[57].

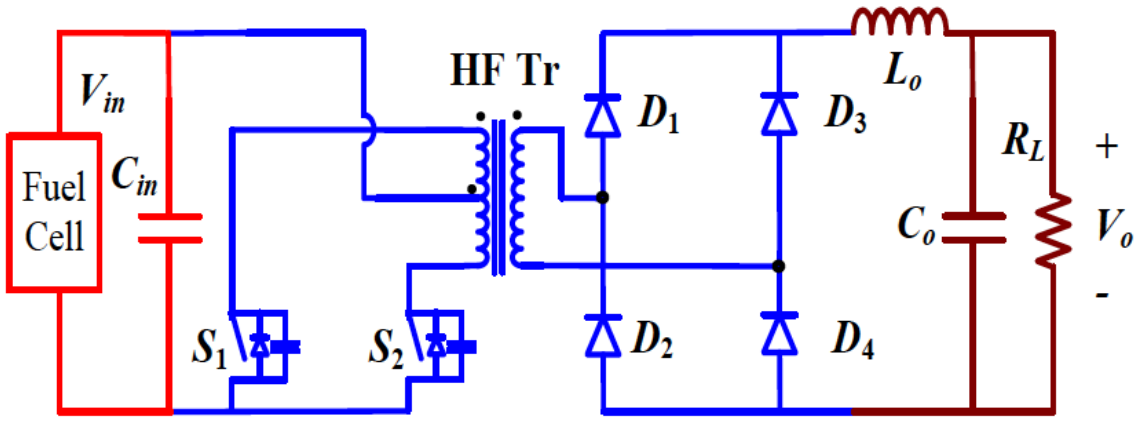
Further, large transformer leakage inductance can be exploited to achieve soft switching of the devices either zero voltage switching (ZVS) or zero current switching (ZCS) through pulse width modulation (PWM) or resonant techniques to achieve lower switching losses and satisfactory operation at high switching frequency.



(a)



(b)



(c)

Fig. 1.8 PWM controlled conventional isolated voltage-fed dc-dc converter topologies a) Full-bridge, b) half-bridge and c) push-pull.

ZVS operation of the most popular PWM controlled converters is studied by simply using device capacitance and transformer leakage inductance. However, high circulating currents together with duty-cycle loss and limited soft-switching range are the major drawbacks with PWM controlled converter. With loss of ZCS in lagging-leg at light load leads to compromised efficiency and EMI issues. Alternatively, the soft-switching range can be extended through various methods like increasing leakage inductance or by using additional series inductance; utilizing auxiliary circuits consisting of passive/active components. However, these methods jeopardize the converter efficiency with considerable power dissipation and complex design [58]-[59]. From the detailed review, a few major drawbacks associated with these converters are listed below:

1. Large transformer turns ratio for high voltage gain applications.
2. Limited soft-switching range.
3. High current stress owing to the high peak and circulating currents through the semiconductor devices and other magnetic components due to freewheeling period.
4. All three isolated bridge converters experience shoot through issue when two switches are simultaneously ON with no inherent short-circuit protection.
5. Rectifier diode ringing resulting in requirement of overrated secondary diodes.
6. Capacitor is unreliable and has relatively shorter lifetime.

1.4.2 Current-fed Converters

Current-fed converter acts a constant current source with significantly low input current ripple. Compared to its voltage-fed counterpart, boost derived current-fed topologies offer natural voltage gain reducing the burden on the HF transformer with significantly lower turns ratio [60]-[61]. An inherent voltage boosting action fosters high voltage conversion ratio, with simplified design and reduced component stresses. Moreover, natural commutation of the rectifier diodes results in negligible diode ringing and reverse recovery issues. However, these converters exhibit slow dynamic response due to continuous input inductor current resulting in relatively challenging start-up and shut-down operations [62]-[63].

Therefore, current-fed topologies with their obvious merits of high voltage gain, stiff dc source current, reduced transformer kVA rating, no duty-cycle loss and inherent short circuit protection have proven to be a desirable choice for the low voltage high current applications

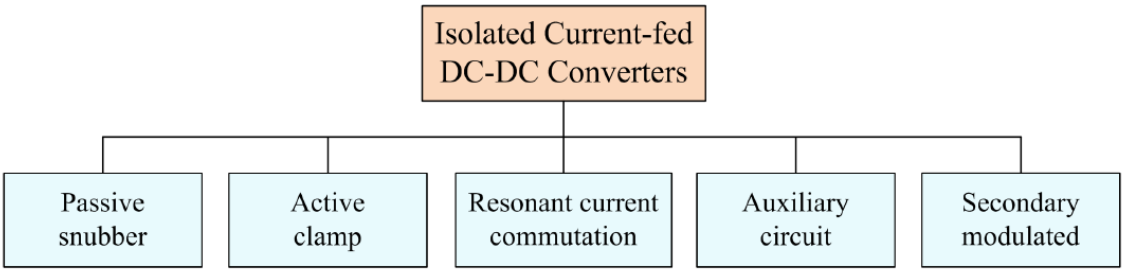


Fig. 1.9 Classification of isolated current-fed dc-dc converters.

(solar PV, fuel cell, batteries) as compared to its voltage-fed counterpart [62]. Also, the absence of large input dc filter capacitor, makes these converters more reliable unlike voltage-fed converters. Despite numerous merits, traditional current-fed converters suffer from historic problem of severe voltage overshoot across the semiconductor devices at their turn-off instant due to the energy stored in the leakage inductance. As a result, the use of high voltage rating devices with high $R_{ds,on}$ becomes unavoidable aggravating the conduction losses. Moreover, at high switching frequency, high switching losses together with large switch turn-off voltage spike, restricts the usage of traditional hard-switched converter [64]. Therefore, snubbing requirement becomes necessary to clamp the turn-off voltage spike as well as to prevent permanent failure of the device. This section focuses on various techniques to mitigate turn-off voltage spikes in traditional current-fed converters that have been reported in literature. Isolated current-fed converters can be classified as depicted in Fig. 1.9. Detailed description together with pros and cons with each of these converter categories are also covered in the subsequent section.

a) Dissipative and Regenerative Snubbing

Traditionally, dissipative and regenerative snubbing have been considered as a simple and straightforward approach to address the historic problem of large device turn-off voltage-spike. These methods utilize combination of resistance, capacitance and diode (RCD) in current-fed converters as reported in [65]-[67]. The dissipative snubber circuits operate on the energy transfer principle hence, dissipating the stored energy into RCD snubber circuit. These lossy snubbing methods are generally hard-switched and aims to alleviate the severity of large voltage overshoot across the semiconductor devices while compromising on the conversion efficiency. Alternatively, converters with LC snubber and flyback snubber transfers the

leakage energy to the load or source [68] improving efficiency at the cost of complex design and additional footprints. Fig. 1.10 illustrates current-fed full bridge converters with aforementioned snubber circuits.

b) Active-Clamping

Current-fed converters employing active clamping circuits are reported in [69]-[72] Various active clamp circuits are shown in Fig. 1.11. Active clamping circuits are implemented to clamp the device turn-off voltage spike using floating semiconductor switches and a large HF capacitor to recycle the energy stored in the leakage inductance. Additionally, ZVS of all the primary side semiconductor switches is achieved. Also, the ZVS at light load can be extended by using energy in magnetizing inductance of the transformer [73]-[74]. Active-clamping for three-phase topologies operating with ZVS are reported in [75]-[77]. However, the major limitations with active clamping circuit are increased current stress, circuit complexity, increased cost and volume for the same rated power with compromised boost capacity.

c) Auxiliary Circuits

Alternatively, the use of auxiliary circuits was introduced to assist zero current commutation of the semiconductor devices. These circuits allow reduced circulating currents while using more number of components and hence, complex configuration. Several current-fed converters with external auxiliary circuits were reported in the literature as shown in Fig. 1.12. Auxiliary circuit proposed in [78]-[79] exhibits improved boost capacity compared to the conventional active- clamp circuits. In most cases, auxiliary circuits contribute to the significant amount of losses in the converter.

d) Secondary Modulation

Full range soft-switching along with natural device voltage clamping is established through snubberless secondary modulation in current-fed converter proposed in [80] shown in Fig.1.13. ZCS commutation and effective device voltage clamping is accomplished by modulating the load side switching devices. The naturally-clamped secondary modulation technique is extended for various current-fed configurations as illustrated in Fig. 1.13 eliminating the need for external snubbers. Converter originality and boost capacity remains unaffected compared to other active-clamp methods while maintain high efficiency and soft-switching [81]-[86].

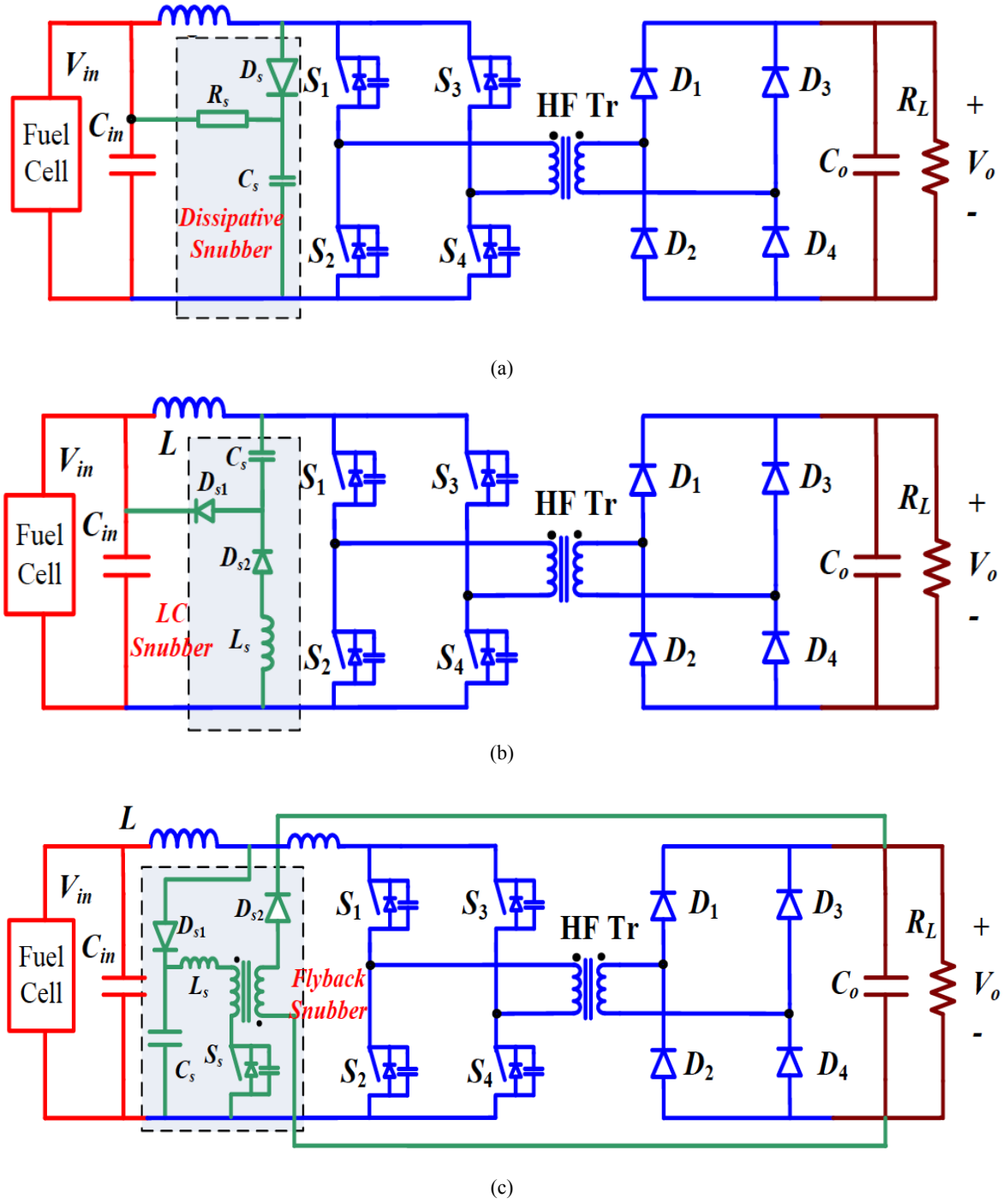


Fig. 1.10 Current-fed DC-DC converters with (a) dissipative snubber, (b) LC regenerative snubber and (c) flyback snubber.

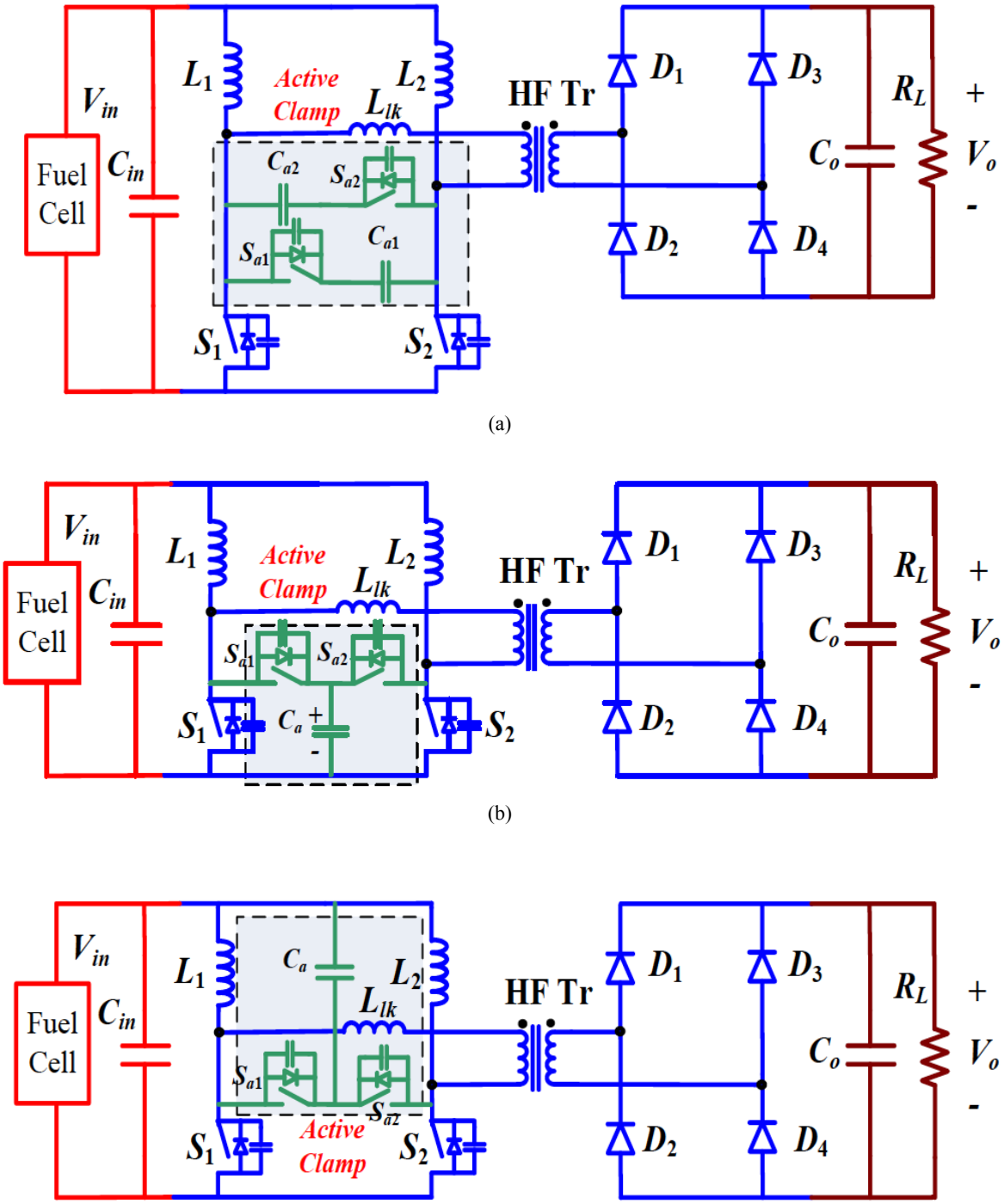


Fig. 1.11 Current-fed DC-DC converters with different configurations of active-clamp circuits.

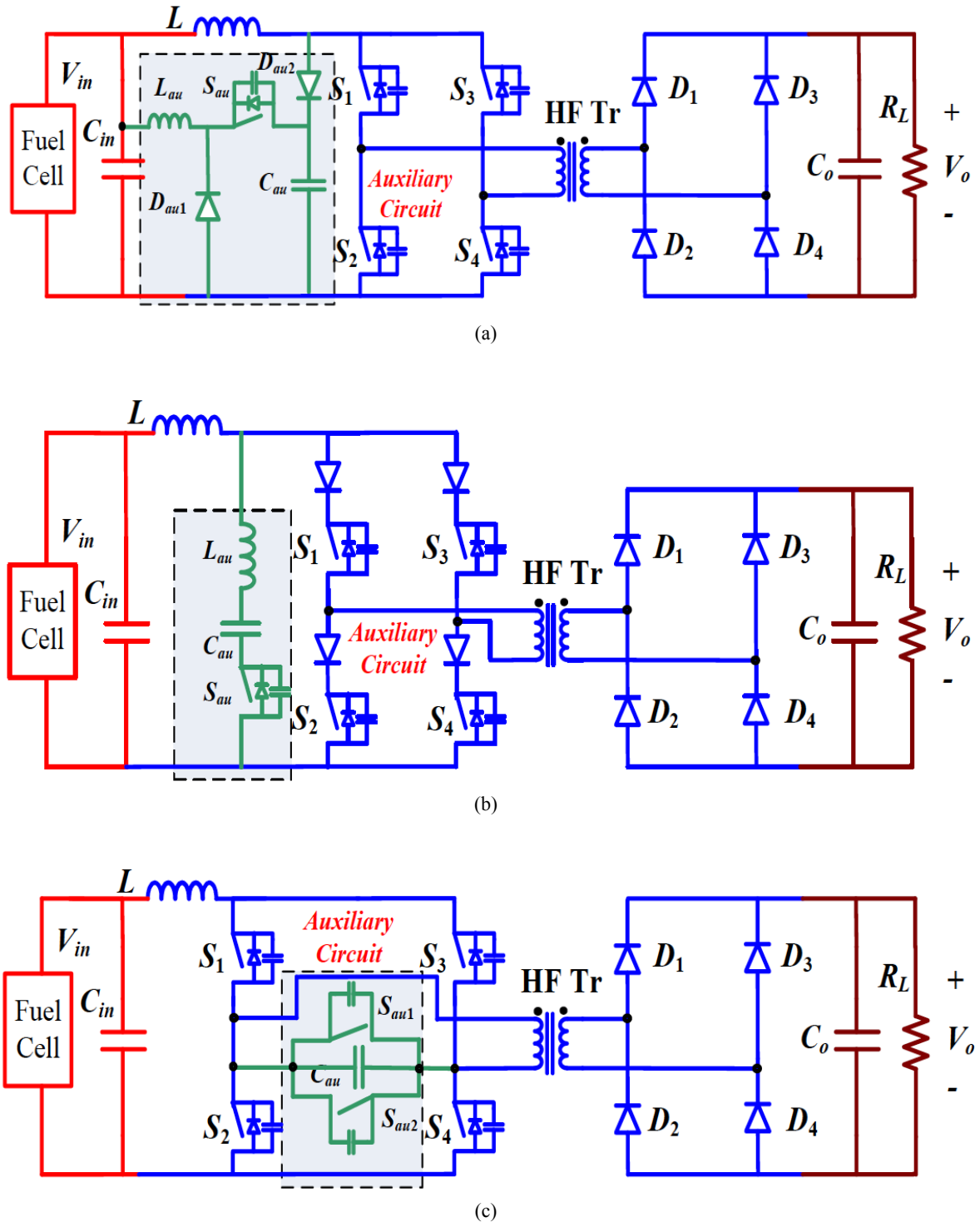


Fig. 1.12 Current-fed DC-DC converters with different configurations of auxiliary circuits.

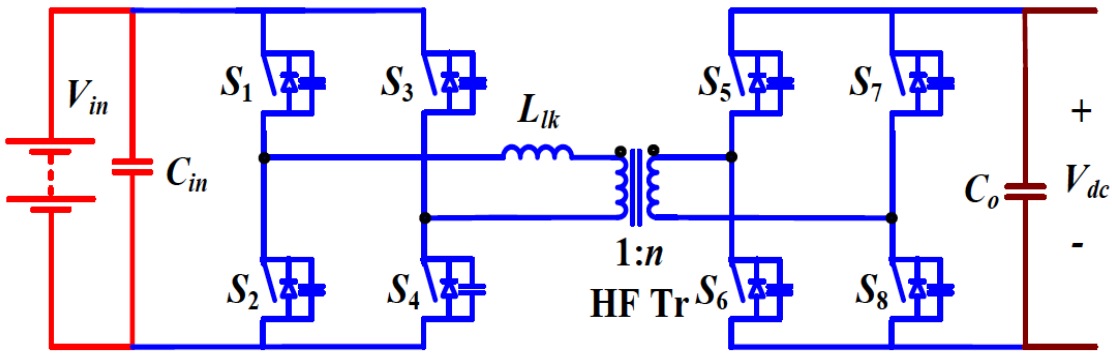


Fig. 1.13 Bidirectional snubberless naturally commutated current-fed full-bridge DC-DC converter.

Nevertheless, these converters are designed and built for bidirectional power flow applications (EV battery charging, fuel cell electric vehicle, UPS, energy storage etc). For unidirectional applications such as solar and fuel cells, the additional active switches and associated gate drive control incur additional cost and unwanted complexity.

1.4.3 Current-fed Resonant Converters

To realize efficient, compact and light-weight system, soft-switching converters incorporating resonant circuits have been extensively explored in the literature mainly for the voltage-fed topologies. The literature on current-fed resonant converters is relatively limited. To overcome the soft-switching range limitations of the PWM controlled current-fed converters, the resonant concept has been proposed and analyzed utilizing transformer non-idealities (leakage inductance) and other circuit parasitic to shape sinusoidally varying currents, that facilitates natural commutation of the semiconductor devices [87]-[90]. The classification of the resonant current-fed dc/dc resonant converters is presented in Fig. 1.14.

a) Conventional Resonant Converter

Conventional resonant converters are categorized as series resonant converter (SRC), parallel resonant converter (PRC) and series parallel resonant converter (SPRC) based on the resonant tank behavior with respect to the load [91]-[92]. These converters have been investigated in detail in the literature for popular low-to-medium power applications [93]-[100]. These converters enable either ZVS or ZCS of the devices depending on the impedance of the resonant tank (inductive/capacitive). These converters demand meticulous resonant

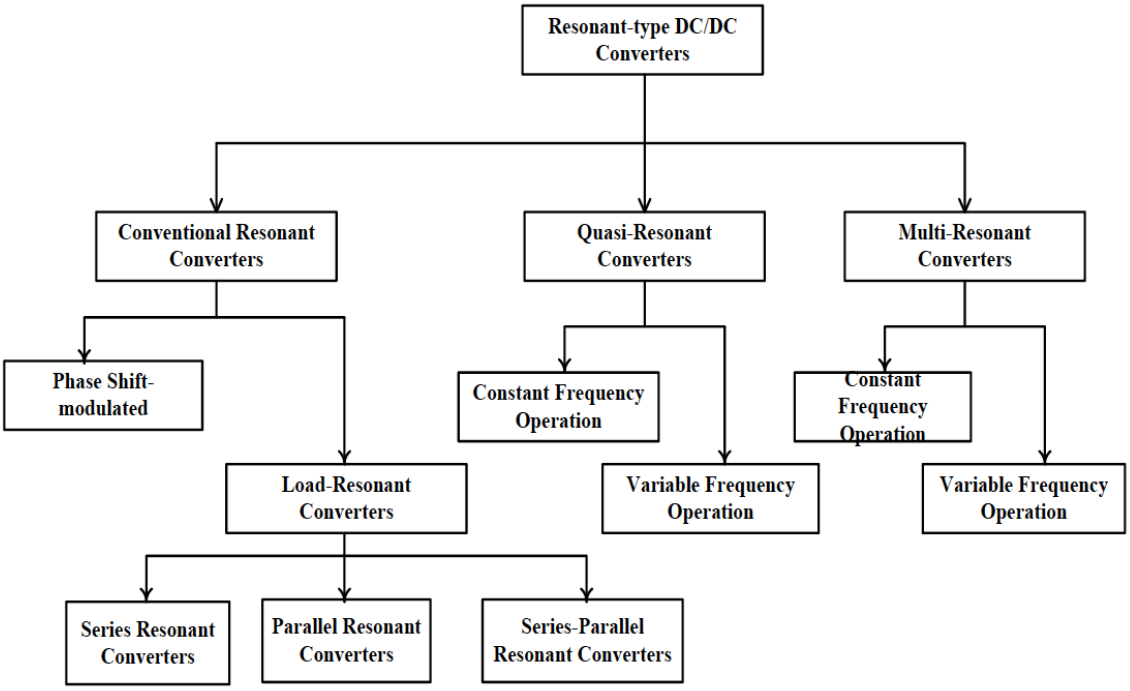


Fig. 1.14 The classification of the dc/dc resonant converter.

tank design to accomplish wide range soft-switching. SRCs are efficient over wide load range while compromising on voltage regulation under light load condition [101]-[110]. Voltage regulation problem can be taken care of by PRC with ZVS implementation. Nevertheless, unusually high circulating/leakage energy is witnessed, which degrades the converter light-load efficiency making these converters unsuitable for low voltage high current specifications. On the contrary, SPRC exhibits the combine features of series and parallel resonant converter. However, difficulty to maintain soft-switching over a wide source voltage and load operating range remains a major limitation with significantly high switching and conduction losses at high input voltage conditions [111]-[119].

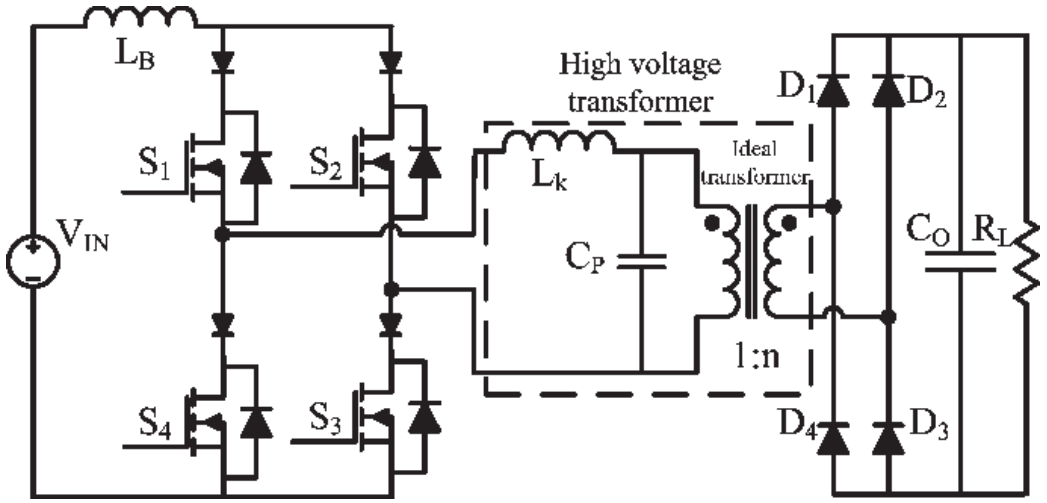
b) Quasi-resonant Converter

Quasi resonance converters (QRC) are modified version of conventional PWM converter, with resonant tank encompassing various parasitic of the converter such as the transformer leakage inductance, transformer winding capacitance, switch capacitance and diode junction capacitance are introduced in [120]-[121]. On substituting the power semiconductor switches in conventional PWM converters with resonant switches, the resonance operation results in quasi-sinusoidal waveforms for resonant switch current/voltage which are responsible for

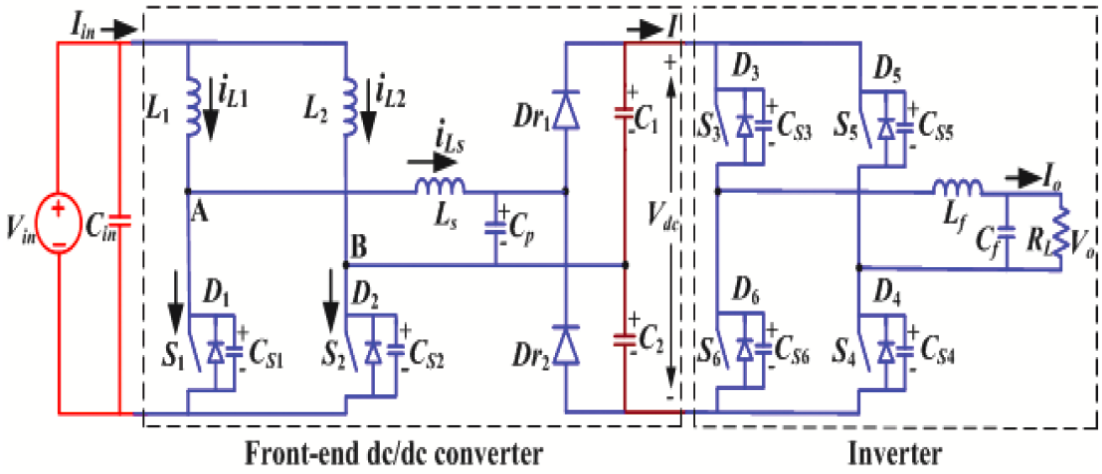
realizing ZCS or ZVS of the semiconductor devices. Thus, in QRCs the basic switching waveforms are modified keeping the originality of the conventional PWM converters. Quasi-resonant converters usually operate with variable frequency modulation with constant OFF/constant-ON time, respectively for ZVS/ZCS operation [122]-[125].

Quasi resonant converters are considered potentially meritorious compared to the conventional resonant converters as they utilize resonant feature for only a fraction of the switching period to facilitate voltage clamping and natural commutation of the semiconductor devices. Concept of ZCS operated impulse-commutation in current-fed full-bridge converter utilizing parallel LC resonant has been introduced by Chen et.al [126] shown in Fig, 1.15(a). The parallel LC resonant tank incorporates transformer leakage inductance, parasitic capacitance of transformer winding and output diode along with additional HF capacitor. By virtue of shunt connected resonant capacitor, it provides fixed resonant energy for all operating conditions. Therefore, at reduced converter loading, low value of input current takes longer time to charge the resonant capacitor to its rated peak voltage, resulting in significant duty-cycle loss [127]. Moreover, higher circulating current is witnessed at light load resulting in higher conduction losses, and hence reduced light-load efficiency. Another limitation is the significantly huge switching frequency variation even for the slight change in the input voltage. Similar quasi-resonant approach with parallel LC tank has also been studied and analyzed for various single-phase, and three-phase configurations such as half-bridge, full-bridge, push-pull [128]-[134] circuits as depicted in Fig.1.15 and Fig. 1.16 respectively.

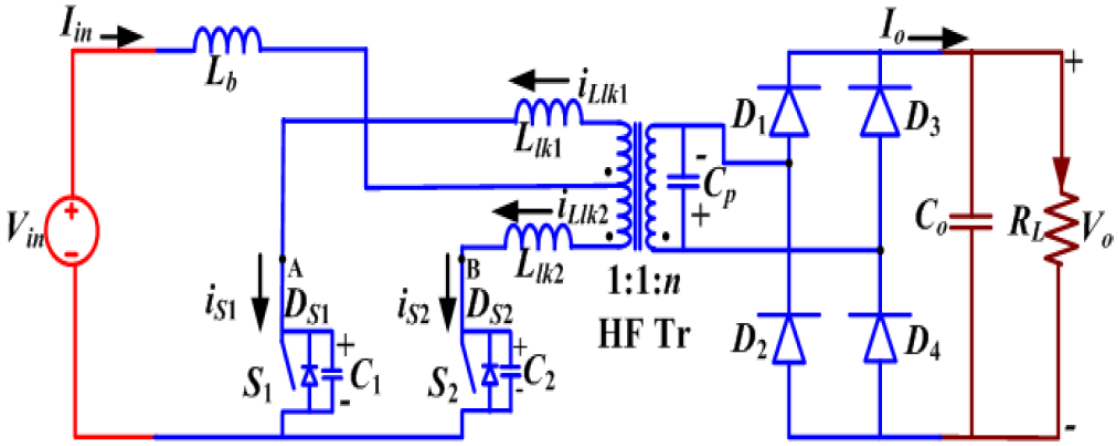
On reviewing several current-fed resonant topologies, major drawbacks that limit its use for low voltage high current specifications for high voltage gain applications, can be summarized as; a) meticulous design to operate under wide load current and source voltage range, b) significant circulating energy at partial load resulting in compromised efficiency, c) wide switching frequency range resulting in complex magnetics/filter design, and d) relatively higher peak values for quasi-sinusoidal waveforms. Due to some classical merits, quasi resonant converters have scope of improvement and are still the topic of research and investigation.



(a)

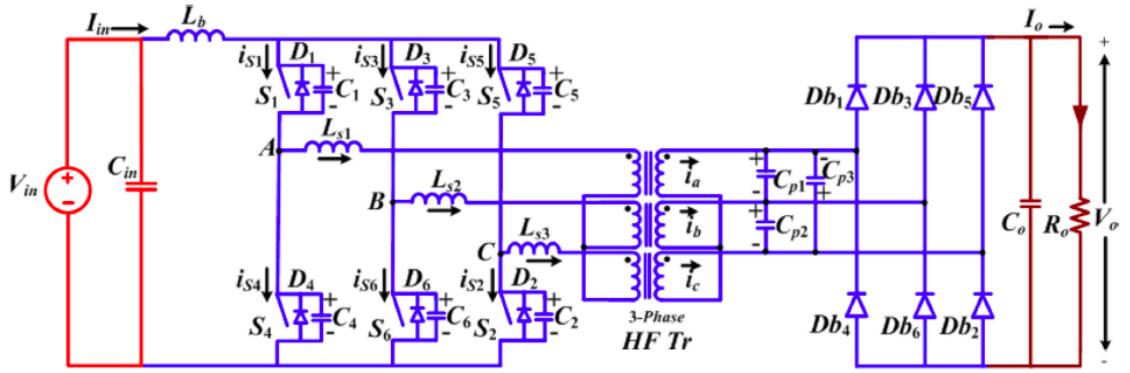


(b)

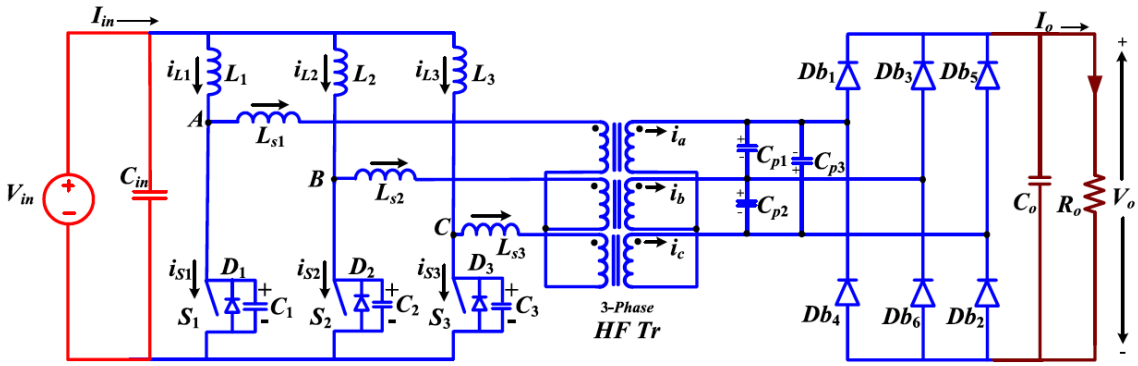


(c)

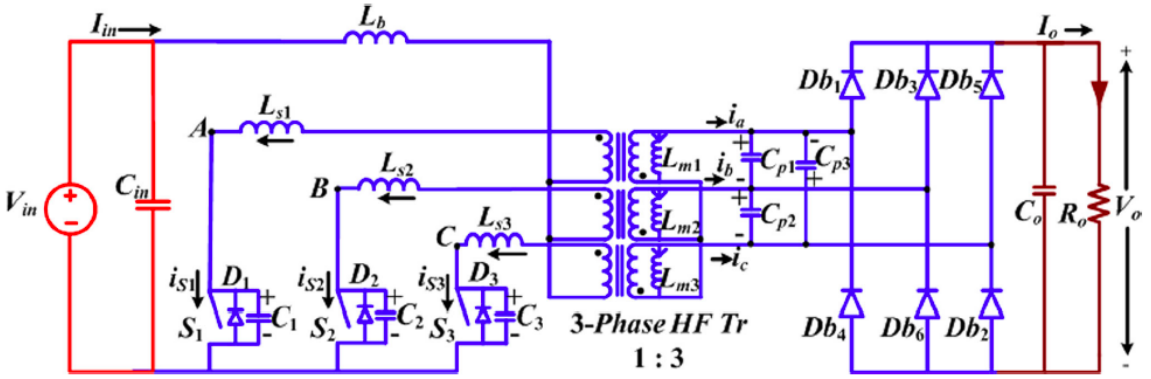
Fig. 1.15 Single-phase impulse commutated current fed dc/dc converter (a) Full-bridge, (b) front-end half-bridge and (c) push-pull configuration.



(a)



(b)



(c)

Fig. 1.16 Three-phase impulse commutated current fed dc/dc converter (a) modular full-bridge, (b) current-sharing three inductor and (c) push-pull configuration.

1.5 Research Problem and Objective

High-density, low cost, and light-weight are the most desirable attributes for any low power electronics system. To achieve these objectives, the most prevalent ways are to use fewer conversion stages, and by increasing the converter's switching frequency leading to reduced footprint with smaller inductors and output capacitors. However, higher switching frequency causes additional switching losses that deteriorates the efficiency and thermal performance. Maintaining soft switching of the semiconductor devices for the entire range of operation is one of the key requirements to enable efficient operation at high switching frequencies. This thesis focuses on developing simple soft-switching techniques to improve the overall performance of the HF DC/DC converter for wide operating range of load current and source voltage.

From the literature overview provided in Section 1.4, the current-fed converters are justified to be more plausible choice for the low voltage high current applications requiring high voltage gain over existing voltage-fed converters. However, a large voltage overshoot across the semiconductor devices at their turn-off is the major setback that diminishes the extraordinary merits of current-fed circuits. Several voltage-clamping circuits, through dissipative snubbers, active clamp circuits, and auxiliary circuits etc. are reported in the literature. However, these methods increase the component's count, design and control complexity, cost and volume, which in turn downgrades the performance of the converter. Alternatively, to resolve the voltage spike issue with improved performance, a gamut of soft-switching current-fed converters utilizing secondary modulation, resonant and quasi-resonant features are also reported in the literature in latter part of Section 1.4. However, the drawbacks outweigh the benefits offered by these converters.

Amongst several current-fed converter topologies reported in Section 1.4, quasi-resonant based approach forms the basis for this thesis due to simple configuration, low component count, simpler gate control requirement and low device rating. Nevertheless, the findings reported in primarily focused on the parallel resonance impulse-commutation, which is plagued with multiple demerits such as, relatively high peak and rms current at light load owing to the fixed resonant energy, duty-cycle loss, higher conduction losses and therefore, reduced light-load efficiency. Comparison of existing topologies with proposed resonance-pulse soft-switching converter has been discussed in terms of switching modulation technique,

component's count, voltage and current rating of the switches, soft-switching range, etc. in Table 1.1.

Therefore, to address these limitations and to achieve wide range ZCS while maintaining high efficiency, a series LC resonance-pulse based ZCS in current-fed circuits has been studied in the thesis. The series resonance-pulse based ZCS concept in current-fed topologies is less explored and hence, the thesis analyzes relevant topologies in current-fed converter family suitable for interfacing low voltage sources to high voltage DC bus systems.

The new series resonance-pulse technique utilizes the transformer leakage inductance and additional small HF capacitor to enable quasi-sinusoidal switch current waveforms to attain ZCS operation and voltage clamping of the semiconductor devices for wide range of source voltage and load current. Short resonance occurring during the conduction overlap of the devices is referred as 'resonance-pulse'. A typical resonance-pulse appears for a fraction of the switching period (nearly 10-15%) thereby creating less leakage in the circuit. The thesis identified and analyzed four promising current-fed configurations incorporating proposed series resonance-pulse circuits. The novel features of the proposed commutation technique can be summarized as:

1. Short-duration resonance (resonance-pulse) is implemented to realize ZCS turn-off.
2. Resonant circuit utilizes transformer leakage inductance and additional small HF capacitor for resonance operation.
3. Series connected resonant capacitor provides load-adaptive resonant energy as opposed to fixed resonant energy in parallel resonance.
4. Low circulating energy at light-loads due to load adaptive resonant energy. Therefore, low power loss is observed.
5. ZCS operation and natural device voltage clamping for wide variations in source voltage and load current.
6. Switching frequency variation is less sensitive to the source voltage variation than load variation.
7. Low component's count and simple configuration.
8. Negligible duty-cycle loss.

Table 1.1: COMPARISON OF THE EXISTING SOFT-SWITCHING CURRENT-FED FULL-BRIDGE TOPOLOGIES

	Active Clamped	**Secondary Modulated**	**Impulse Commutated**
Semiconductor count	4 Primary MOSFETs 4 Rectifier Diodes	4 Primary MOSFETs 4 Secondary MOSFETs	4 Primary MOSFETs 4 Rectifier Diodes
Additional Components	1 floating MOSFET 1 input inductor 1 large HF clamping capacitor	Load side active devices	1 HF capacitor 1 resonant inductor
Switch voltage stress	$\frac{V_{in}}{2(1-D)}$	$\frac{V_o}{n}$	$\frac{V_o}{n}$
Diode voltage stress	V_o	V_o	V_o
Soft-switching feature	ZVS of all switches	ZCS of primary switches, ZVS of load side switches	ZCS of all switches ZCS of diodes
Soft-switching range	Limited (hard switched at light load)	Load adaptive	Load adaptive
Modulation technique	PWM	PWM	Variable frequency
Circulating Current	High	Low	High
Duty Cycle loss	High	-	High
Circuit Complexity	Complex	Moderate	Simple

The very objectives of this thesis encompass identifying an appropriate switching/modulation technique, and analyzing the series resonant-pulse technique to achieve soft-switching in current-fed topologies to meet the high voltage gain requirement for the low voltage high current microgrid specifications. Therefore, with the combined benefits of the series resonant-pulse and the current-fed configure, the proposed series resonance-pulse assisted current-fed topologies are well suited for solar/fuel cell integration to DC microgrid. These converters can serve as promising interface in applications like battery charging, fuel-cell inverter, solar inverter, solar water pumping etc.

1.6 Thesis Contributions

The major contributions of the thesis are as follows:

1. The thesis introduces a novel series resonant-pulse soft-switching concept to obtain ZCS of the devices and to eliminate the device turn-off voltage spike without using any external snubber or clamping circuit. The proposed series resonance-pulse concept is analyzed and implemented for single phase topologies a) current-fed push-pull converter and b) current-fed half-bridge converter. These topologies are justified for low power applications. Detailed steady-state analysis is done to demonstrate the natural device commutation with zero current utilizing load adaptive resonant energy. The proposed resonant-pulse soft-switching enables wide range soft switching to accommodate inherent variability in source voltage. These converters demonstrate good efficiency and have simple structure with only two semiconductor controlled devices and simpler gate driving requirement because of common ground devices with power supply.
2. Series resonance-pulse assisted modular current-fed full-bridge converter studied and analyzed for moderately high power applications. Modularity of this converter allows easy scalability for high power levels. Number of such modules can be configured to achieve the desired power and output voltage levels. Moreover, with modular structure, current and voltage stress can be significantly reduced for high power industrial applications.
3. Series resonance-pulse assisted current-fed three-phase current sharing dc-dc converter is proposed and investigated for high power applications. This converter demonstrates potential applications requiring high-power density at high power level owing to the low

component's count. Wide range soft-switching and voltage clamping of the semiconductor is achieved.

1.7 Thesis Outline

The thesis has been organized into seven Chapters to highlight the major contributions. The layout is as follows:

1. In Chapter 2, a novel series resonant-pulse based soft-switching technique has been introduced to resolve the device turn-off voltage spike issue without the use of additional snubber circuit. The proposed series resonant-pulse is implemented for current-fed circuit with push-pull configuration at the source and output voltage-doubler to provide high voltage gain. Converter steady-state analysis and design guidelines are validated to demonstrate ZCS turn-off of the semiconductor switches. Benchmarking with existing soft-switching current-fed converters is covered in this Chapter. Simulation and experimental results validate the proposed design, operation and expected claims using PSIM 11.1 software and 500W laboratory prototype respectively.

2. In Chapter 3, a series resonant-pulse assisted current-fed half-bridge converter has been proposed and studied in detail for high voltage gain applications. The operation and performance of the converter are demonstrated through simulation results from PSIM 11.1 software, and the experimental results from a 500W hardware prototype.

3. In Chapter 4, a modular series resonance-pulse assisted current-fed full-bridge converter is conceptualized for relatively high power applications. Converter steady-state operation, and design procedure with an example to interface solar/fuel cells to high voltage dc bus are discussed. Simulation results are presented to demonstrate ZCS operation and device voltage clamping for wide operating range. Experimental results on a scaled-down 500 W prototype validate the proposed claims.

4. In Chapter 5, the proposed series resonance-pulse is extended to current-fed three-phase current sharing dc-dc converter topology. The proposed three-phase topology exhibit promising features like reduced filtering requirement, low component count, low

conduction losses etc. Steady-state analysis, and design are validated through simulation results and hardware experimentation on laboratory prototype rated at 1kW.

5. Chapter 6 presents the concluding remarks for this thesis and future scope of research.

1.8 Concluding remarks

This Chapter addressed the operating constraints and key challenges associated with low voltage renewable and non-conventional energy sources like solar PV, fuel-cell etc. Fundamental requirements for efficient design of a dc/dc power converter interface to comply with the specifications of a low voltage high current microgrid application are discussed in detail. Extensive literature survey of the existing converters suitable for aforementioned application is collated. Considering requirements of low voltage high current applications, it has been concluded that current-fed converters with inherent benefits like high voltage gain, low input current ripple, short circuit protection, etc. offer promising solution for such applications. Nevertheless, large turn-off voltage spike across semiconductor devices is a major limitation with conventional hard-switched current-fed converters. From the literature, quasi-resonant converters utilizing parallel LC resonant circuit exhibit number of advantages compared to the other soft-switching converters. However, due to fixed resonant energy, large peak and circulating currents are observed at light-loads. Therefore, efficiency is compromised. To address these limitations, a simple and straightforward approach utilizing transformer leakage inductance and a small series capacitor to facilitate smooth commutation eliminating voltage spikes has been identified as an efficient design to interface low voltage high current applications. The proposed soft-switching technique has been implemented in other potential current-fed converter topologies.

Detailed analysis and meticulous design of the identified series resonant-pulse assisted current-fed topologies has been performed to realize a short resonance-pulse during switching overlap period facilitating wide range ZCS of the devices. The viability of these series resonant-pulse assisted current-fed converters has been investigated for low voltage high current applications involving sources with inherent variation such as PV and fuel cells.

Chapter 2

Series Resonance-Pulse Assisted Current-Fed Push-Pull DC-DC Converter

1 Introduction

Despite superior features like high voltage gain, low source current ripple, and inherent short-circuit protection, hard switching of the semiconductor devices and large turn-off voltage spike across the switching devices compel the use of overrated components, undermining the extra-ordinary merits of the current-fed converters. Therefore, with a focus on achieving better device utilization, limiting the semiconductor device switching losses, and reducing the size and cost of the heat-sink associated with them, several soft-switching methods have been reported in the literature reviewed in Chapter 1. However, the dissipative circuits and active-clamp snubber circuits have been used to solve the voltage spike issue, at the expense of additional components, increased complexity, footprints and deteriorated converter performance in terms of voltage gain, cost and efficiency. Amongst other advanced soft-switching techniques, Quasi-resonant approach for the soft commutation and device voltage clamping has been acclaimed as a promising choice owing to its inherent ability to utilize lower resonant energy, with substantially lower circulating current and lower resonant current peak for wide operating range.

This Chapter introduces and investigates in detail, the concept of partial-resonance-pulse (one of a kind Quasi-resonant approach) in the current-fed push-pull converter topology to achieve zero-current switching (ZCS) of the semiconductor switches. Resonance pulse is established through a series LC resonant circuit, during switching overlap interval, which is referred as energy storage mode. The current is smoothly transferred from one outgoing switch to the other incoming switch with sufficient energy for anti-parallel diode conduction resulting in ZCS turn-off of the semiconductor switch. The proposed soft-switching converter effectively solves the historical problem of voltage spike across the switching devices at their turn-off and thus, eliminates the requirement of the snubber or the clamping circuit across them. This reduces the hardware complexity while making the converter snubberless,

TABLE 2.1 COMPARISON OF THE PROPOSED SOFT-SWITCHING CONVERTER WITH OTHER EXISTING SOFT-SWITCHING TECHNIQUES

Description	**Passive Snubbing**	**Active Snubbing**	**Secondary Modulation**	**Conventional Resonant**	**Resonant Pulse (Proposed)**
Control technique	Variable duty	Variable duty	Variable duty	Phase shift modulation	Variable Frequency
Type of switching	Hard switching	Soft switching (ZVS)	Soft switching (ZCS)	Soft switching (ZVS/ZCS)	Soft switching (ZCS)
Switch voltage stress	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_o}{n}$	$\frac{V_o}{n}$	$\frac{V_o}{2n} + V_{cr\_pk}$
Resonant energy	-	-	Fixed	Fixed/Adaptive	Load Adaptive
Soft-switching range	-	Hard switching at light loads	Wide range	Wide range	Wide range
Additional components	Passive circuitry	Floating Active devices and large capacitor	4 Load side Active Devices	Resonant Inductor/Capacitor	Resonant Inductor/Capacitor
Boost capacity	Compromised	Compromised	Compromised	Preserved	Preserved
Circuit complexity	Simple	Complex	Complex	Simple	Simple
Circulating currents and associated losses	High	High	Moderate	High	Low

compact, and cost-effective. Table 2.1 corroborates the merits of the proposed soft-switching method compared to the existing techniques reported in the Chapter 1. The distinct attributes of the proposed converter configuration presented in this Chapter are elaborated as follows:

1. Compared to traditional resonant converters, the commutation strategy targeted in this thesis employs resonance for short duration which is defined as resonance-pulse or partial resonance.
2. Series resonant tank energy being load adaptive helps in keeping lower circulating and peak currents under all operating conditions, that further limits the RMS current through the components resulting in the reduced heat sink size and overall higher efficiency.
3. Push-pull topology is advantageous by virtue of having only two switching devices with common ground with the source simplifying the gate driving requirements to cater cost and control limitations.
4. Push-pull configuration utilizes single boost inductor with relatively less components.
5. ZCS and voltage spikes elimination across the switching semiconductor devices allow high switching frequency operating with higher converter density.

The layout of this Chapter is as follows: Section 2.2 explains the steady-state operation of the proposed converter. Section 2.3 describes the steady-state analysis and mathematical expressions for each mode of converter operation. Section 2.4 illustrates the converter design procedure to determine the desired attributes with appropriate selection of the various component ratings for the given specifications. Section 2.5 shows simulation and experimental results together with the characteristic curves and loss distribution of the proposed converter. Concluding remarks are presented in Section 2.6.

2.2 Proposed Converter topology

Fig. 2.1. Illustrates the schematic of high frequency isolated series resonance-pulse current-fed push-pull converter with voltage doubler across the load. DC-DC boost configuration allows conversion from the variable low input voltage to a regulated fixed high voltage dc across the load utilizing single boost inductor and high frequency (HF) center-tapped

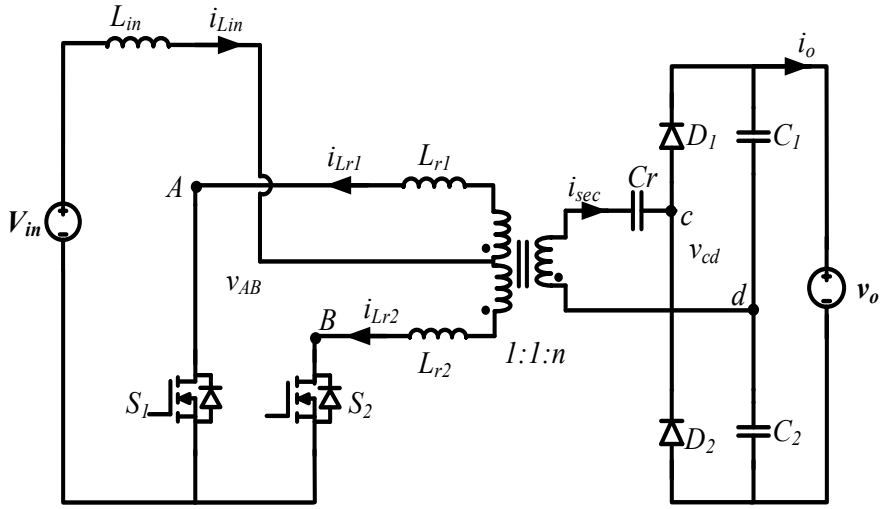


Fig. 2.1. Series-LC resonant-pulse ZCS current-fed push-pull converter with voltage doubler.

transformer to provide the required voltage gain. Push-pull topology features a pair of symmetrical switches S_1 and S_2 operated with gating signals phase shifted by 180º with duty ratio $D > 0.5$ which then periodically reverses the current polarity in the transformer primary. Therefore, continuous current is drawn from the source in both halves of the switching cycle resulting in steady input current with significantly low noise.

Unlike conventional resonant converters, a short resonance pulse is established using transformer leakage inductance and a series capacitance during conduction overlap of the switches. The energy stored during this interval assists in ZCS of the semiconductor devices preventing voltage spikes across the switches. Moreover, the proposed soft-switching converter offers reduced circulating and rms current, particularly, under light load condition owing to the load dependent series resonant energy. The amount of power transferred to the load is primarily controlled by the variable frequency modulation with a constant duty cycle. Moderate frequency variation is observed for source voltage variation as opposed to load fluctuations. The control objectives of the proposed converter topology are to achieve low ripple input current and snubberless commutation of the semiconductor switches with uniform output voltage regardless of variation in source voltage and load.

2.3 Steady State Operation of the Converter

Steady-state operation over one switching cycle is completed in total ten intervals utilizing theoretical waveforms shown in Fig. 2.2. This Chapter delineates the converter analysis for

five operating intervals due to the symmetry of operation and therefore, half switching cycle is discussed in detail. Equivalent circuits for the five operating intervals during half switching period are depicted in Fig. 2.3. For the simplified time-domain analysis, the following assumptions are outlined.

a) Sufficiently large boost inductor is assumed to maintain constant current.
b) All the semiconductor devices are ideal and lossless.
c) The output filter is large enough to maintain the constant output voltage.
d) Infinitely large magnetizing inductance of HF transformer is assumed.

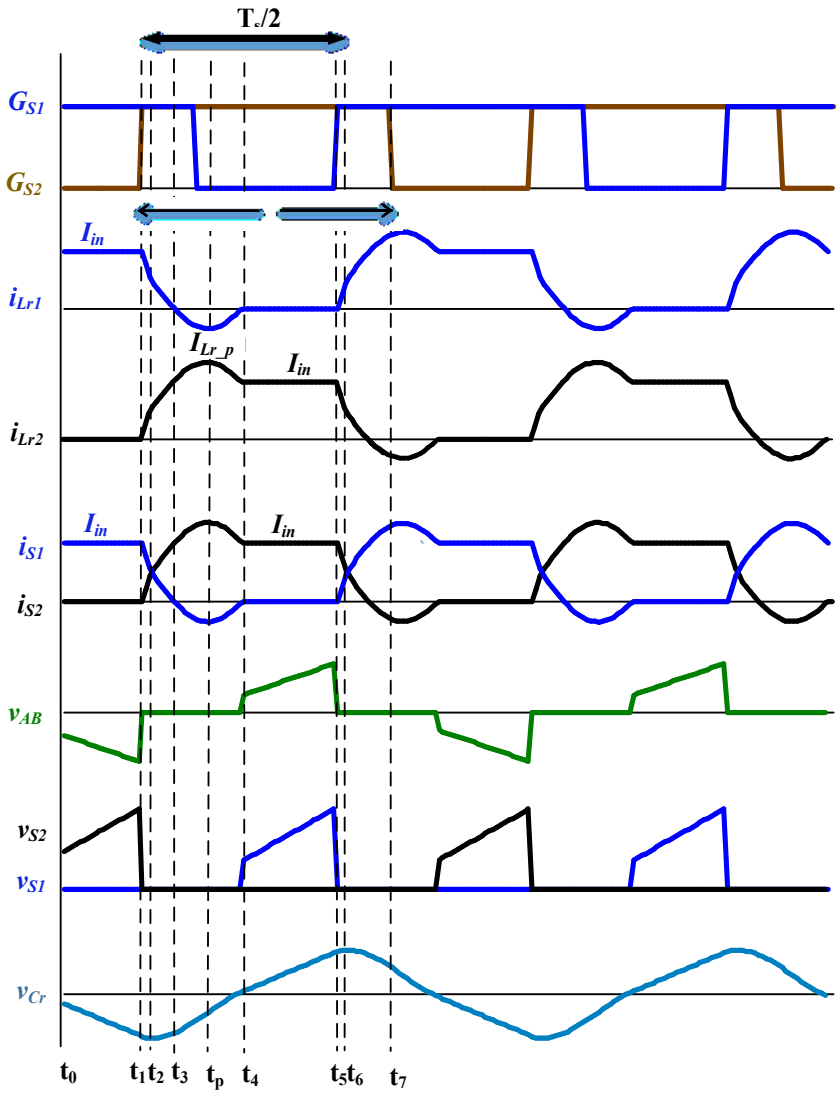
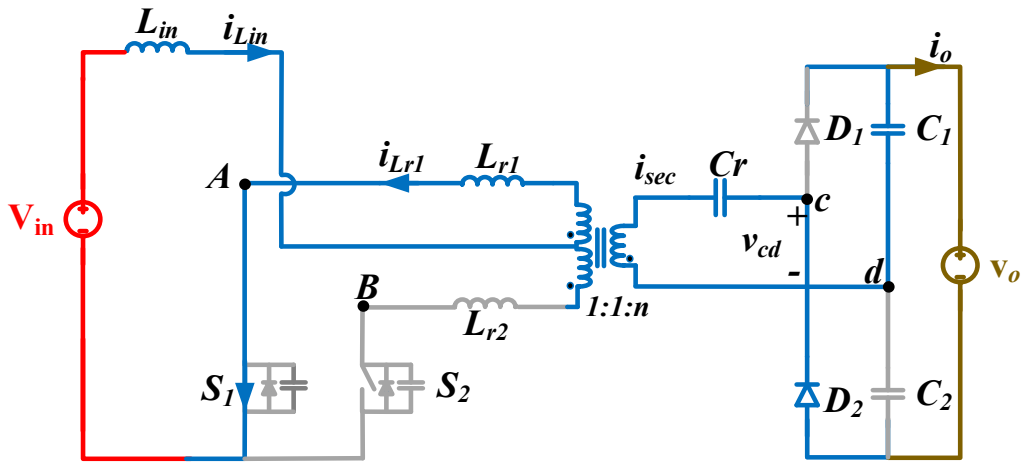
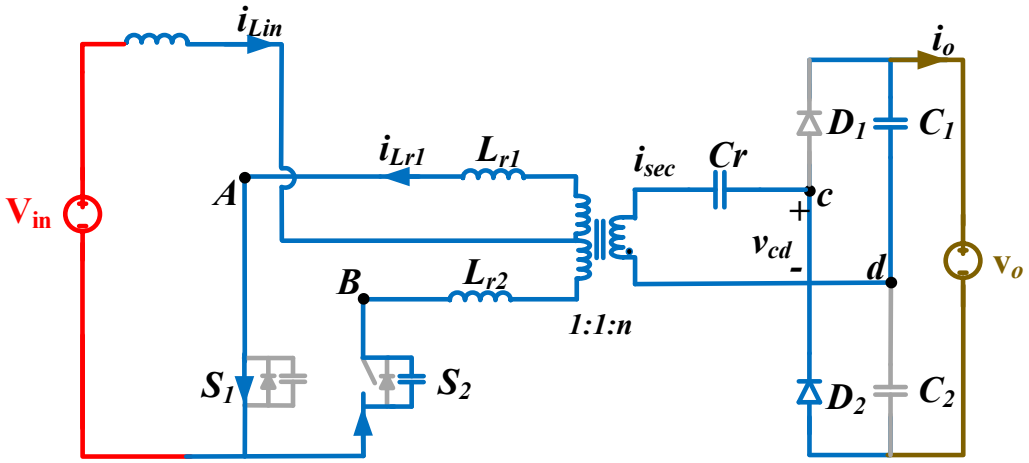


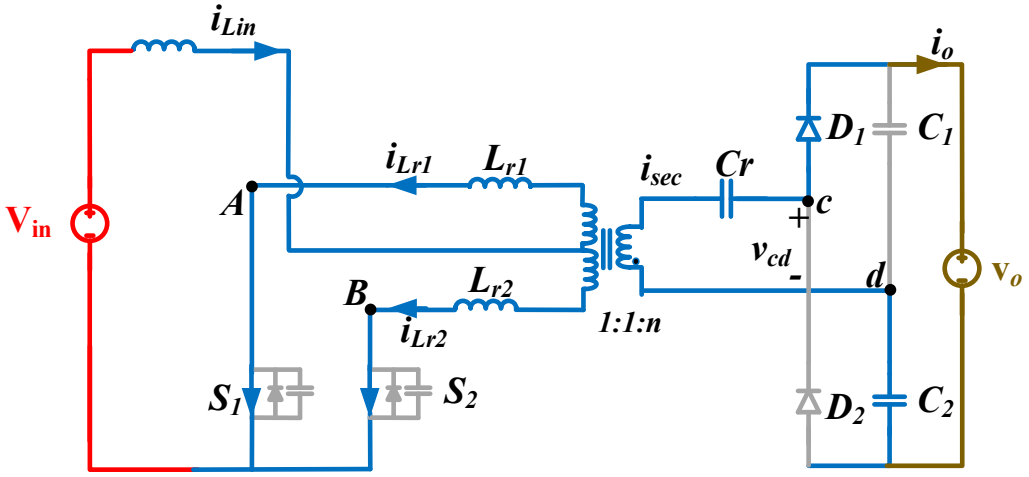
Fig. 2.2. Steady state operating waveforms of the proposed converter topology.


L_{in}
i_{Lin}
i_o
D_1
C_1
V_{in}
A
i_{Lr1}
L_{r1}
i_{sec}
Cr
c
v_{cd}
+
-
d
v_o
B
L_{r2}
1:1:n
S_1
S_2
D_2
C_2

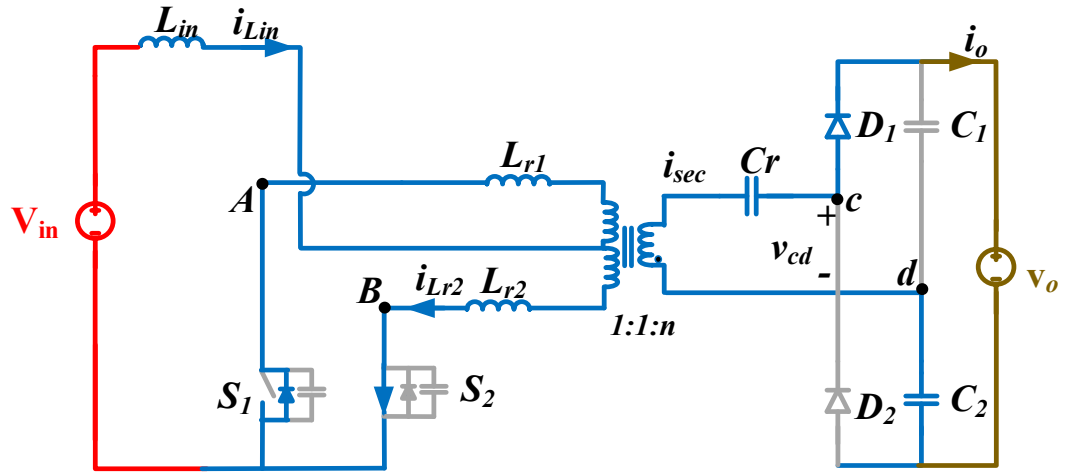
(a)


i_{Lin}
i_o
D_1
C_1
V_{in}
A
i_{Lr1}
L_{r1}
i_{sec}
Cr
c
v_{cd}
+
-
d
v_o
B
L_{r2}
1:1:n
S_1
S_2
D_2
C_2

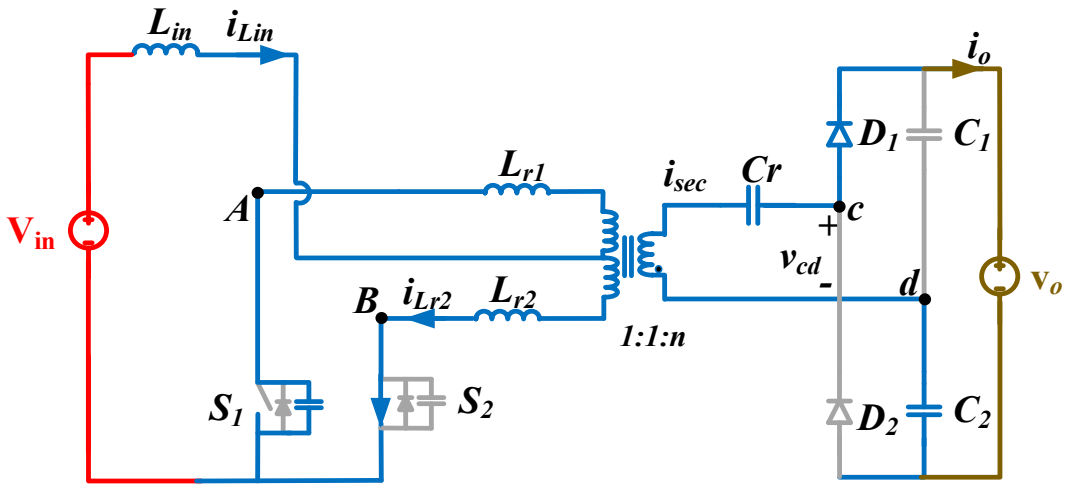
(b)


i_{Lin}
i_o
D_1
C_1
V_{in}
A
i_{Lr1}
L_{r1}
i_{sec}
Cr
c
v_{cd}
+
-
d
v_o
B
L_{r2}
i_{Lr2}
1:1:n
S_1
S_2
D_2
C_2

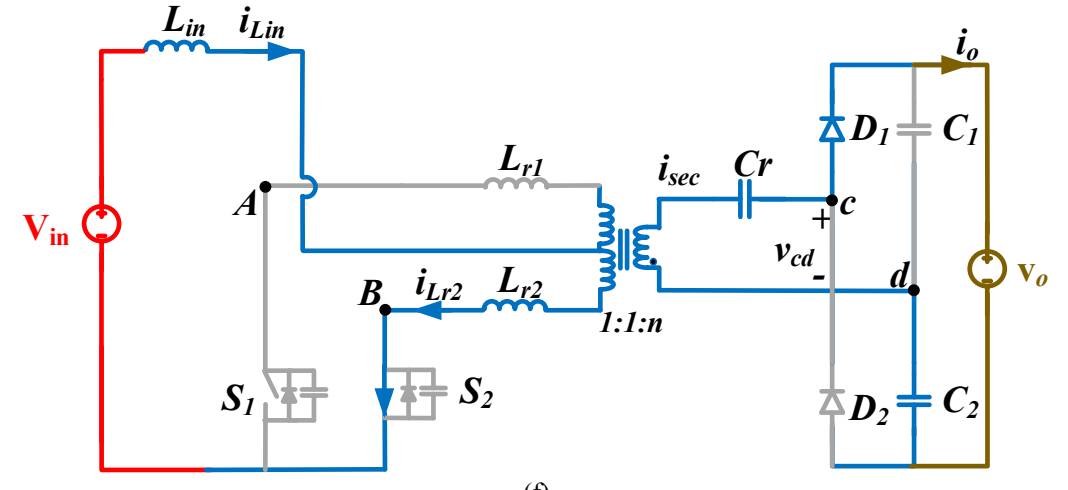
(c)



(d)



(e)



(f)

Fig. 2.3. The equivalent circuits during different operating intervals.

Time domain analysis helps derive the dynamic mathematical equations for each interval to facilitate accurate design of the converter. In addition, the analytical expressions assist in determining the component's ratings and investigate the theoretical converter performance.

a) *Interval 1 (t_0-t_1): (Energy transfer interval refer Fig. 2.3(a))*

Assuming switch S_1 to be conducting with a constant current I_{in} through transformer primary with inductor L_r. The inductor L_{r1} supplies the energy to the load through the diode D_2 and C_1 as shown in Fig. 4(a). During this interval, negative current at the secondary winding discharges the resonant capacitor C_r resulting in linearly decreasing bridge output voltage V_{AB}. Dynamic equations during this interval are represented as,

$$i_{S1}(t) = I_{in}, \qquad i_{Lr1}(t) = I_{in} \tag{2.1}$$

$$i_{S2}(t) = i_{Lr2}(t) = 0 \tag{2.2}$$

$$V_{cr}(t) = V_{cr}(t_o) + \frac{1}{C_r}\int_{t_o}^{t_1} -nI_{in}\, dt = V_{cr}(t_o) - \frac{nI_{in}}{C_r}(t - t_0) \tag{2.3}$$

$$V_{AB}(t) = -2\left(\frac{V_{out}}{2} + V_{cr}(t_1)\right)\frac{1}{n} \tag{2.4}$$

b) Interval 2 (t_1-t_2): (Transition interval refer Fig. 2.3(b))

Switch S_2 is turned-on at instant t_2, with a quick discharge of its intrinsic snubber capacitance C_{S2}. During this transition interval, the terminal voltage V_{AB} clamped to zero while transformer secondary voltage becoming positive with both switches remain conducting. The voltage across inductor L_{r2} rises with linearly increasing current through switch S_2. At this moment, current through S_1 begins to fall with the same slope. Converter equations representing this mode are as follows:

$$i_{S1}(t) = i_{Lr1}(t) = I_{in} - \frac{1}{nL_r}\left(\frac{V_{out}}{2} + V_{cr}(t_1)\right)(t - t_1) \tag{2.5}$$

$$i_{S2}(t) = i_{Lr2}(t) = \frac{1}{nL_r}\left(\frac{V_{out}}{2} + V_{cr}(t_1)\right)(t - t_1) \tag{2.6}$$

At the end of this mode:

$$i_{Lr1}(t_2) = i_{S1}(t_2) = \frac{I_{in}}{2} \tag{2.7}$$

$$i_{Lr2}(t_2) = i_{S2}(t_2) = \frac{I_{in}}{2} \tag{2.8}$$

$$V_{AB} = 0 \tag{2.9}$$

Assuming, this transition interval T_{21} to be very trivial, necessary hypothesis can be made;

$$V_{cr}(t_2) = V_{cr}(t_1) = -V_{cr\_pk} \tag{2.10}$$

From (2.5), (2.7) and (2.8), duration of this mode can be written as:

$$T_{21} = \frac{nI_{in}L_r}{2 * \left(\frac{V_{out}}{2} + V_{cr}(t_1)\right)} \tag{2.11}$$

c) Interval 3 (t_2-t_3): (Resonance mode Fig. 2.3(c))

With switch S_1 and S_2 conducting, resonance begins in the short circuit path between $(L_{r1} + L_{r2})$ and primary referred resonant capacitor $C_{r,eff}$ resulting in sinusoidally changing current through transformer primary and semiconductor switches. During this time, the resonant inductor stores energy with respective increase/decrease in the switch current. The switch and series inductor currents are represented as;

$$i_{S1}(t) = i_{Lr1}(t) = \frac{I_{in}}{2} - \frac{1}{nZ_o}\left(\frac{V_{out}}{2} + V_{cr_{pk}}\right) sin\omega_r(t - t_2) \tag{2.12}$$

$$i_{S2}(t) = i_{Lr2}(t) = \frac{I_{in}}{2} + \frac{1}{nZ_o}\left(\frac{V_{out}}{2} + V_{cr\_pk}\right) sin\omega_r(t - t_2) \tag{2.13}$$

At the end of this interval, current i_{Lr2} increases to I_{in} while the current through switch S_1 and L_{r1} reaches zero.

$$i_{S2}(t_3) = i_{Lr2}(t_3) = I_{in}\,, \qquad i_{S1}(t_3) = i_{Lr2}(t_3) = 0 \tag{2.14}$$

From (2.13) and (2.17), duration of this mode can be given as:

$$T_{32} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{nI_{in}Z_o}{2 * \left(\frac{V_{out}}{2} + V_{cr\_pk}\right)}\right) \tag{2.15}$$

d) Interval 4 (t_3-t_4): (ZCS interval Fig. 2.3(d) and 2.3(e))

Resonance period continues during this interval, with inductor current (i_{Lr2}) surpassing I_{in}. By virtue of this additional current, internal diode across the outgoing switch conducts before the gating signal is removed resulting in soft turn-off of the targeted switch. Resonance pulse terminates at instant t_4 when current i_{Lr2} again reaches I_{in}. During this interval, i_{Lr2} reaches its peak value (I_{Lr2_p}) at instant t_p which must exceed I_{in} to ensure ZCS under all conditions.

$$I_{Lr2\_p} > I_{in} \tag{2.16}$$

$$\frac{I_{in}}{2} + \frac{1}{nZ_o}\left(\frac{V_{out}}{2} + V_{cr\_peak}\right) > I_{in} \tag{2.17}$$

The peak current through primary switches can be estimated as,

$$I_{S2\_p} = I_{Lr2\_p} = i_{Lr2}(t_x) = \frac{I_{in}}{2} + \frac{1}{nZ_o}\left(\frac{V_{out}}{2} + V_{cr\_peak}\right) \tag{2.18}$$

From (2.15) and (2.16), time duration of this mode can be computed as:

$$T_{42} = \frac{1}{\omega_r}\left(\pi - \sin^{-1}\left(\frac{nI_{in}Z_o}{2 * \left(\frac{V_{out}}{2} + V_{cr\_pk}\right)}\right)\right) \tag{2.19}$$

$$T_{43} = T_{42} - T_{32} \tag{2.20}$$

e) Interval 5 (t_4-t_5): (refer Fig. 2.3(f))

At t_4, current i_{Lr2} reduces to I_{in} due to sinusoidal characteristics with switch S_2 conducting entirely transferring power from source to the load through diode D_1 and C_2 as shown in Fig. 2.3(f). During this interval, constant current flows through switch S_2 resulting in zero voltage across series inductor while the series capacitor charges linearly.

$$i_{S1}(t) = i_{Lr1}(t) = 0 \tag{2.21}$$

$$i_{S2}(t) = i_{Lr2}(t) = I_{in} \tag{2.22}$$

Duration of this interval is denoted as:

$$T_{10} = T_{54} = \frac{T_s}{2} - T_{41} \tag{2.23}$$

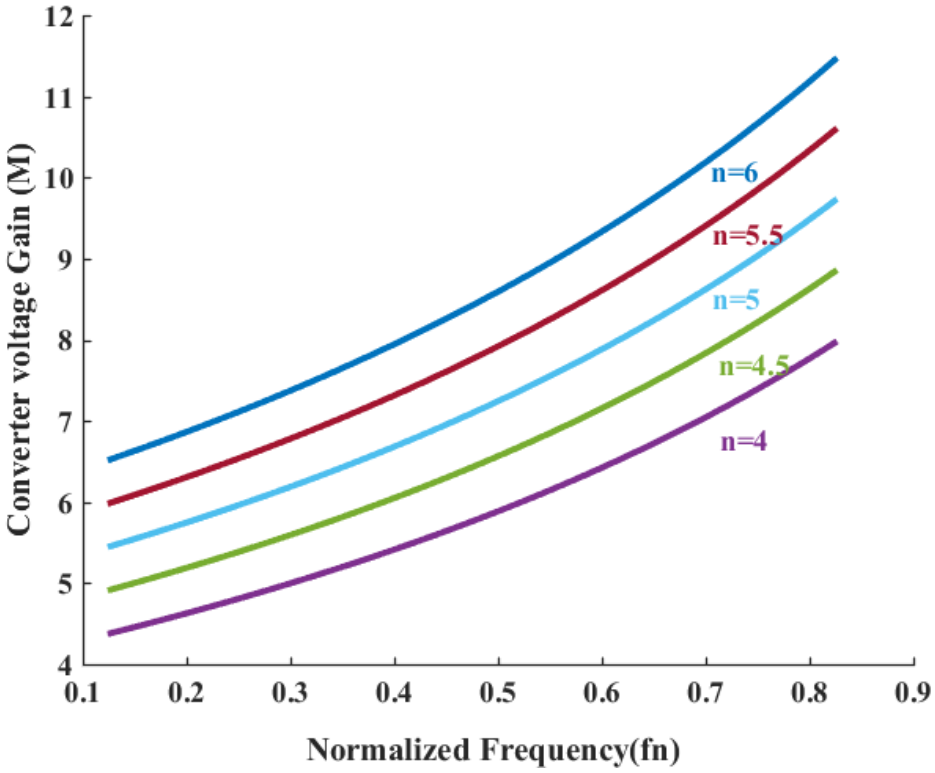


Fig. 2.4. Gain characteristic curves for the proposed current-fed push-pull converter.

2.3.1 Voltage gain of the converter

The voltage gain (M) dynamics of the converter is governed by a number of variables. The characteristic curve shown in Fig. 2.4 allows careful selection of the switching frequency range and the optimal turns ratio of the transformer to obtain the desired dc voltage gain for a given input-output voltage profile. Applying power balance principle and average output current expression, relation between input and output voltage can be obtained.

$$I_{in} * V_{in} = \frac{{V_o}^2}{R_{FL}} \tag{2.24}$$

$$I_{o,avg} = \frac{V_o}{R_{FL}} = \frac{I_{Lr,avg}}{n} = \frac{1}{n}.\frac{2}{T_s}\int_0^{T_s/2} i_{Lr}(t)\ dt \tag{2.25}$$

DC voltage gain of the proposed converter can be expressed as,

$$M = \frac{V_o}{V_{in}} = \frac{n\left(1 - \frac{f_n r_n X}{\pi}\left(1 - \sqrt{1-k^2}\right)\right)}{\left(1 - f_n\left(\frac{1}{2} - \frac{1}{2\pi} sin^{-1}k + \frac{k}{2\pi}\right)\right)} \quad (2.26)$$

where, n: Turns ratio of HF transformer; $k = \frac{M}{nr_nX}$;

f_n: Normalized frequency, $= \frac{f_s}{f_r}$

r_n: Normalized load resistance $= \frac{R_{FL}}{n^2\, Z_r}$

X: Constant defined as, $= \left(1 + \frac{2nV_{crp}}{V_o}\right)$

Gain variation occurs with disturbance in source voltage and load, which is compensated by modulating switching frequency in order to maintain stiff output voltage under all conditions.

2.3.2 Component stresses in the converter

Component's rating can be determined by the maximum voltage across and rms current appearing through them. The voltage stress across the switch is dependent on the referred resonant capacitor charge and reflected output voltage.

$$V_{DS,max} = \frac{2V_{cr\_pk}}{n} + \frac{V_o}{n} \quad (2.27)$$

and voltage stress across the rectifier diodes are governed by the output voltage,

$$V_{D1\_max} = V_{D2\_max} = V_o \quad (2.28)$$

Also, the switch voltage rating is critical in optimizing the switch conduction losses owing to its direct dependency on the device on-state resistance $R_{ds,on}$. Hence, lower voltage rating switches are preferred to have reduced conduction losses. Further, the rectifier diodes with low V_{FD} and Q_{RR} are selected to minimize diode conduction losses and EMI issues occurring at high-switching frequencies.

The rms current through the primary switches and the transformer inductance is given by:

$$I_{Lr1,2\_rms} = I_{Sw1,2\_rms}$$

$$= \left[I_{in}^2 \left(\frac{1}{2} - \frac{f_s}{f_r} \left(\frac{1}{4} - \frac{1}{8}\left(\frac{1}{k}\right)^2 + \frac{k}{6\pi} - \left(\frac{\sqrt{1-k^2}}{8\pi k} \right) \right) + \frac{1}{\pi} \left(\frac{1}{8}\left(\frac{1}{k}\right)^2 - \frac{1}{4} \right) sin^{-1}k \right) \right]^{\frac{1}{2}} \tag{2.29}$$

$$I_{D1-2,avg} = I_o \tag{2.30}$$

2.4 Converter Design

This section presents the detailed design guidelines of the proposed converter suited for low input voltage applications, ranging from 42–48V feeding a high voltage dc bus at 380V. The key objectives are 1) regulating stiff dc voltage across the load 2) soft-switching of the semiconductor devices against fluctuations in source voltage and load. ZCS is achieved by exploiting sinusoidally changing switch current due to series resonance feature. Design of the converter parameters significantly affects the losses in active and passive components which therefore influence the component's rating and converter efficiency of the converter. Henceforth, it is imperative to design converter parameters with minimum stresses on the components.

2.4.1 Selection of HF Transformer Turns Ratio

Converter voltage gain (M) has a direct correlation with the turns ratio (n) of HF transformer and the normalized frequency f_n as shown in Fig. 2.4. Moreover, it is observed that the turns ratio, n has a significant impact on the voltage and the current stresses in the semiconductor devices as evident from (2.27). It is, therefore, vital to control the conduction losses while accomplishing the desired voltage gain, by choosing a right combination of turns ratio and switching frequency. It can be construed that higher turns ratio could reduce the voltage stress across the semiconductor devices while increasing the currents on the primary side resulting in higher conduction/copper losses. Whereas, a smaller turns ratio would necessitate higher voltage rating switches while minimizing current stresses on the low voltage side. Considering previously mentioned issues, the turns ratio has been chosen as 1:1:4.5. For this design example, the switching frequency band is 80 kHz up to 200 kHz for V_{in} = 48V down to 42V.

2.4.2 ZCS boundary condition and selection of Z_o

Ideal design of the resonance pulse must ensure sufficient energy to maintain ZCS for the extended range of load and source voltage while restricting circulating current and conductions losses in the converter. Following are the necessary conditions to achieve ZCS under all conditions.

a) I_{Lr1_p} , $I_{Lr2\_p} > I_{in}$

This condition fulfils the requirement for the internal body diode conduction of the device to ensure smooth commutation. This condition requires adequate selection of the characteristic impedance, Z_o so as to maintain a right balance between peak resonant currents and the ZCS range. Maximum limit for the Z_o can be estimated using the following expression:

$$Z_o < \frac{\left(\frac{V_{out}}{2n} + V_{cr_{peak}}\right) * R_{FL} * V_{in}}{{V_{out}}^2} \tag{2.31}$$

A small value of Z_o enables the soft-switching of the devices for the extreme operating conditions of V_{in} = 42 V and 48 V at rated load. However, it is also desired to prevent the high circulating and peak current in the circuit, which may lead to higher conduction losses and poor efficiency.

b) $T_{32} < T_{overlap} < T_{42}$

Secondly, in order to preserve the ZCS for the extended operating range of load and source voltage, holding a constant overlap time is necessary with variable frequency modulation. This obliges a short variation in the duty cycle to account for the switching frequency variation resulting in a constant overlap period.

2.4.3 Design of resonant tank parameters

Resonant tank design procedure follows the following steps:

1. Selection of switching frequency f_{sw} for a maximum gain condition at V_{in} = 42V and full-load.
2. Estimation of f_r using (2.26) for a maximum gain condition.
3. Computation of maximum allowable characteristic impedance $Z_{o,maz}$ for the minimum source voltage (42V) using (2.31).

4. Selection of lower than $Z_{o,max}$ that satisfies (2.31) for smooth commutation with limited circulating current.

Utilizing characteristic impedance Z_o and resonant tank frequency f_r, parameters L_{r1}, L_{r2} and C_r are computed using the following expressions.

$$f_r = \frac{1}{2\pi\sqrt{(L_{r1} + L_{r2})\, C_{r\_ref}}}\,, \qquad Z_o = \sqrt{\frac{(L_{r1} + L_{r2})}{C_{r\_ref}}} \tag{2.32}$$

where C_{r_ref} is the primary referred series capacitance (C_r).

The computed value of L_{r1} and L_{r2} is $2.5\mu H$ and C_r is $8.5nF$, for this design example.

2.4.4 Input inductor calculation

To maintain low ripple current under all the operating conditions, the worst case inductor current needs to be considered for the inductor calculation. Therefore, for rated power with minimum source voltage of 42V, a worst-case input current is computed to be 11.9A. For this design example, allowing 5% ripple in the input current, the boost inductor value is computed. Moreover, the ripple content is affected by resonance pulse duration. Therefore, the input boost inductor for the proposed design is calculated using:

$$L_{in} = \frac{V_{in}\,(t_4 - t_1)}{\Delta I_{in}} \tag{2.33}$$

Where $t_{41} = t_4 - t_1$ is the effective resonance pulse period in one half-cycle.

2.4.5 Voltage doubler capacitor calculation

In the voltage doubler rectifier, the output capacitors are designed to filter the switching frequency noise components. Thus, the output capacitance equation is given by,

$$C_{o1}, C_{o2} = \frac{I_o}{2 f_s V_{o,ripple}} \tag{2.34}$$

where $V_{o,ripple}$ is the output voltage ripple.

2.5 Loss Distribution of the Proposed Converter

In this Section, the loss evaluation of the proposed converter is conducted to accurately estimate the efficiency of the converter with the proposed design. Mathematical expressions for the losses occurring in various active and passive components are reported in Table 2.2. Dependency of various converter parameters on the distinct loss component is studied in detail

TABLE 2.2: LOSS EQUATIONS OF THE PROPOSED CONVERTER

Loss Type	Equation
MOSFET conduction loss	$I_{sw,rms}{}^2 * R_{Ds,on}$
MOSFET switching loss (turn-on)	$\frac{1}{2} C_{oss} V_{sw}{}^2 f_{sw}$
Rectifier diode loss	$V_{Df} * I_{D,avg} + I_{D,rms}{}^2 * R_D + V_d\, Q_{rr}\, f_{sw}$
Input Boost inductor loss	$I_{in}{}^2 * R_{L,DC}$
HF Transformer loss	$I_{Lr,rms}{}^2 * R_{winding} + P_{C,limit}\, V_e$
Gate drive loss	$C_{iss} V_g^2 f_s$
Auxiliary (capacitor loss/stray loss)	$I_{cout,rms}{}^2 * R_{ESR}$

in this Section. It should be understood from Table 2.2 that the MOSFET conduction loss primarily depends on the rms current and device on-state resistance ($R_{ds,on}$) while the switch turn-on losses are governed by operating frequency and voltage appearing across drain-and-source. Moreover, rectifier diodes present negligible turn-on loss with finite reverse recovery/ turn-off loss. Furthermore, other major losses predominantly occur in center-tapped transformer and the input inductor. Utilizing analytical expressions presented in Section 2.4 together with information assimilated in Table 2.2. It can be interpreted that the overall loss in the converter is an ultimate function of three major parameters as given in matrix (2.35) which in turn determines the converter efficiency (η_{conv}).

$$\begin{bmatrix} I_{Sw,rms} \\ \frac{1}{2} C_{oss} V_{sw}{}^2 f_{sw} \\ P_{Core} \\ V_{Sw,rated} \end{bmatrix} = f\left(f_{sw}, n,\ R_{Ds,on}\right) \Rightarrow \eta_{conv} \tag{2.35}$$

Therefore, efficiency can be maximized by properly selecting these parameters $\left(f_{sw}, n,\ R_{Ds,on}\right)$ to minimize losses. For this experiment, in order to limit the switch turn-on and conduction losses, MOSFET with low output capacitance (C_{oss}) and low $R_{ds,on}$ is chosen. This is possible if lower voltage rating switches are employed. In addition, the SiC Schottky diodes are carefully chosen for the secondary side rectifier to assist in smooth turn-off with reduced reverse recovery loss. Likewise, EE ferrite core is used to design center-taped HF transformer allowing low magnetizing current ripple and limited core loss. Besides, the converter efficiency is further improved by developing in-lab optimized gate drive circuit with

separate gate resistors for turn-on and turn-off path. Henceforth, various loss components can be optimized by careful design of converter parameters with adequate semiconductor device rating for maximum efficiency.

2.6 Result and Discussion

This section presents the simulation and experimental results of the proposed converter to validate the converter analysis and design.

2.6.1 Simulation Results

To validate the mathematical analysis and to ensure the satisfactory operation of the proposed converter, steady-state simulation results are obtained from PSIM 11.0 software for the given converter specification in Table 2.3. Parameters obtained from converter design are listed in Table 2.4. Proposed topology is simulated with source voltage range of 42- 48V at different load currents to evaluate the steady-state performance. The simulated input inductor current and resonant inductor waveforms at full-load are shown in Fig. 2.5. Voltage clamping and ZCS of the switching devices (S_1 and S_2) have been achieved for variation in source

TABLE 2.3: CONVERTER DESIGN SPECIFICATIONS

Parameter	Value
Source voltage, $\boldsymbol{V_{in}}$	42-48 V
Maximum duty, $\boldsymbol{D}$	0.6
Output power, $\boldsymbol{P_o}$	500W
Output voltage, $\boldsymbol{V_o}$	380 V
Switching frequency, $\boldsymbol{f_s}$	80-200 kHz

TABLE 2.4: CONVERTER DESIGN PARAMETERS

Parameter	Value
Resonant Inductor, L_{r1}, L_{r2}	2.5μH
Resonant Capacitor, C_r	8.5nF
Input inductance, L_{in}	300μH
Output capacitance, C_{o1}, C_{o2}	80μF
Turns ratio, 1:1: n	1:1:4.5

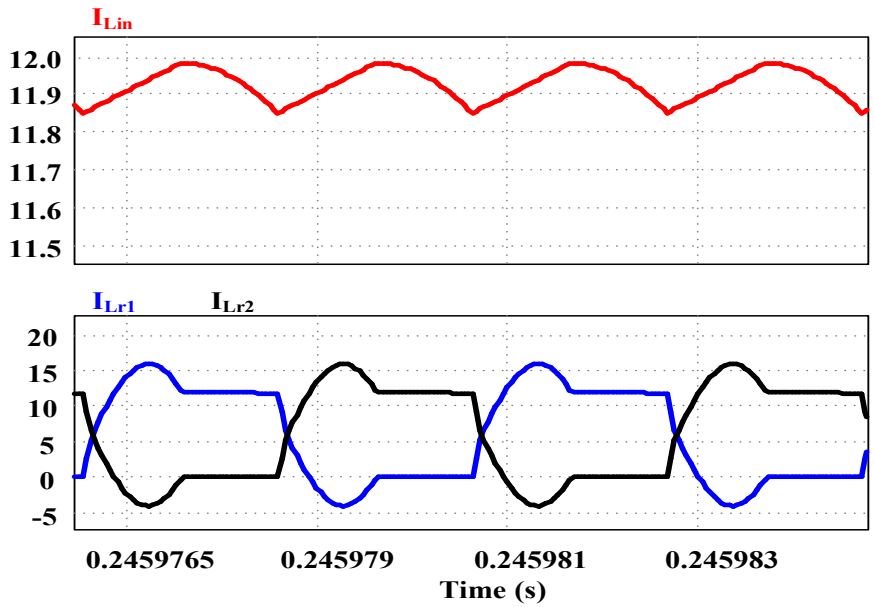
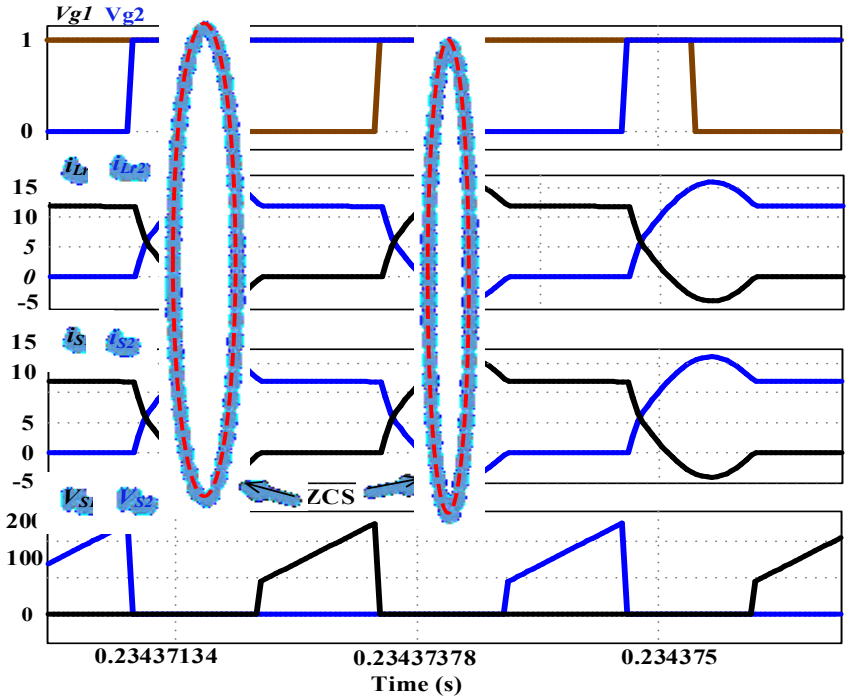
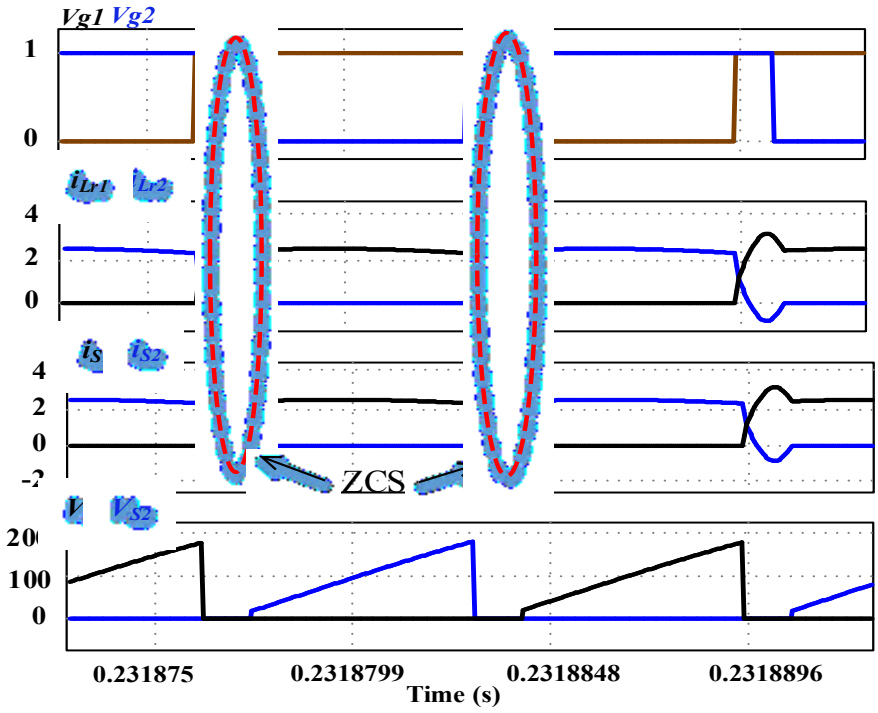


Fig. 2.5. Simulated waveforms depicting input inductor current and resonant inductor current at transformer primary for full-load (500W) operation.

voltage and load current. Semiconductor switch turn-off instant is highlighted for V_{in}= 42V and V_{in}= 48V in Fig. 2.6 and Fig 2.7 respectively. Series resonance concept is justified owing to the sinusoidally varying currents during gating overlap period, which naturally reduces the switch current to zero before the gating pulse is removed. The overshoot in the switch voltage is eliminated as evident in Fig. 2.6 and Fig. 2.7. Constant current, I_{in} through the transformer primary is observed when only one switch (S_1) is conducting resulting in linearly increasing capacitor charge and hence, linearly increasing voltage across the complimentary switch (S_2). The above-mentioned claims hold true for simulation results at light-load operation for source voltage V_{in}= 42V and V_{in}= 48V as demonstrated in Fig. 2.6(b) and Fig. 2.7(b) respectively. It should also be observed that the voltage stress across switching devices reduces with decrease in the load current. Soft-commutation at switch turn-off eliminates turn-off voltage spikes which is a fundamental drawback with current-fed converters. The output voltage and output current graphs for full-load (500W) and 20% load (100W) are shown in Fig. 2.8(a) and 2.8(b) respectively. Fig. 2.8 confirms that the proposed converter is able to achieve the regulated stiff output voltage for all the operating conditions by implementing variable frequency control. Output current is maintained at constant 1.3 A and 0.26A for the two extreme load points validating the efficient converter design.

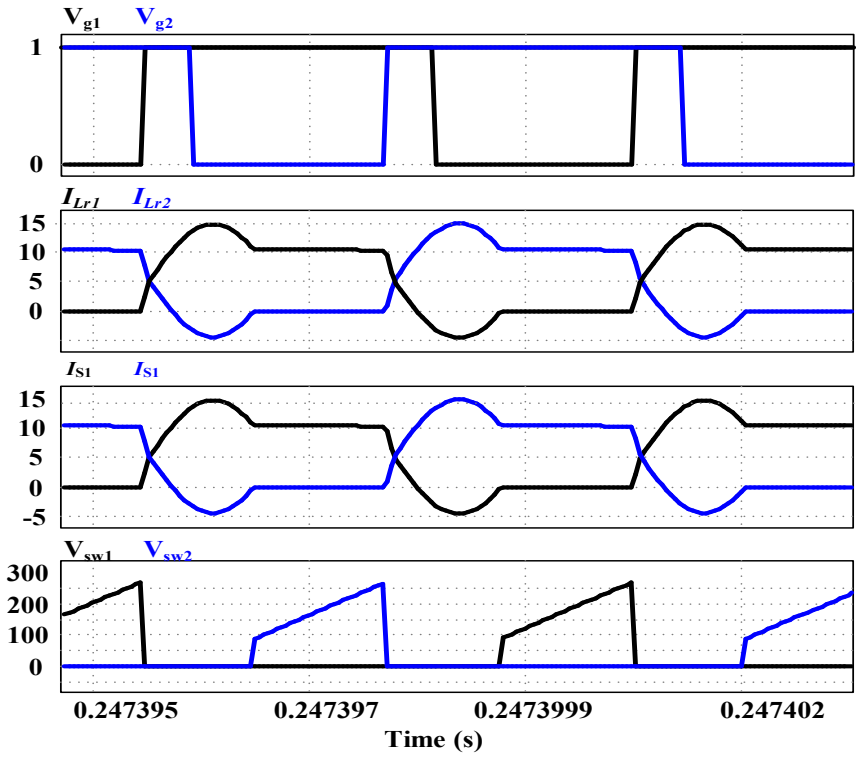


(a)

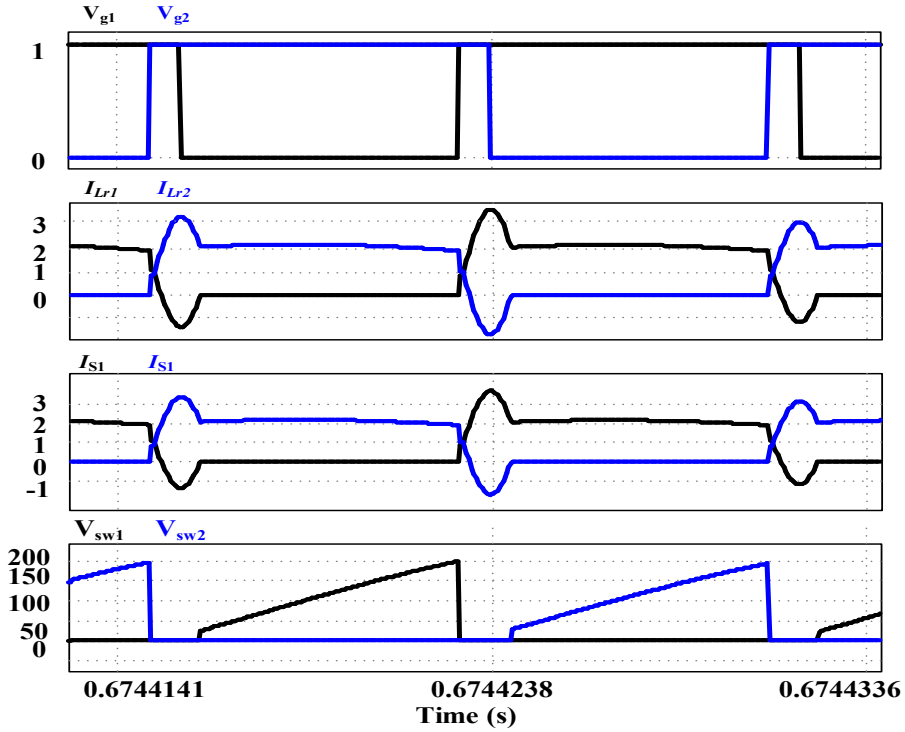


(b)

Fig. 2.6. Simulated waveforms depicting ZCS for primary side devices for V_{in}= 42V at (a) at full-load (500W) (b) light-load (100W) operation.

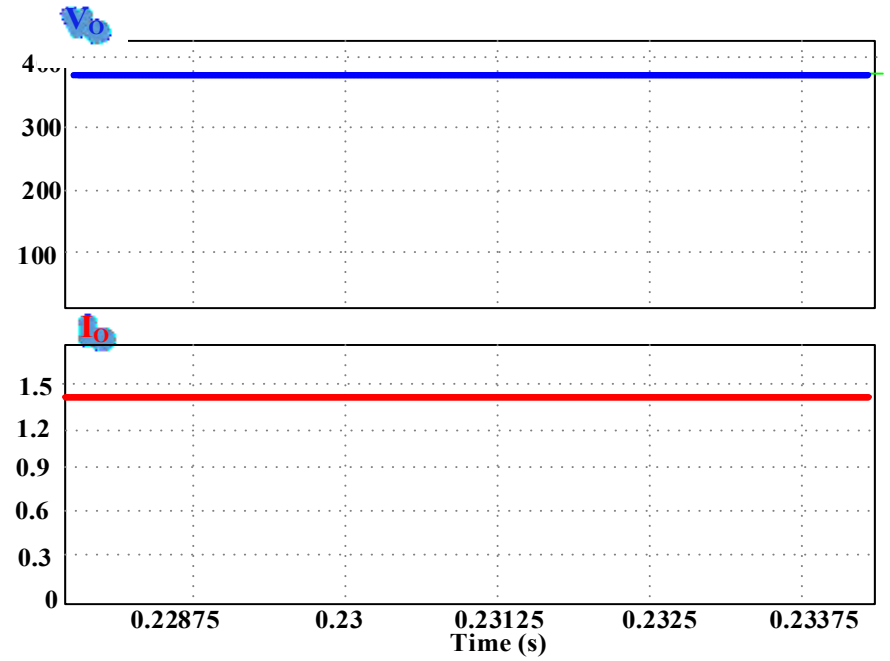


(a)

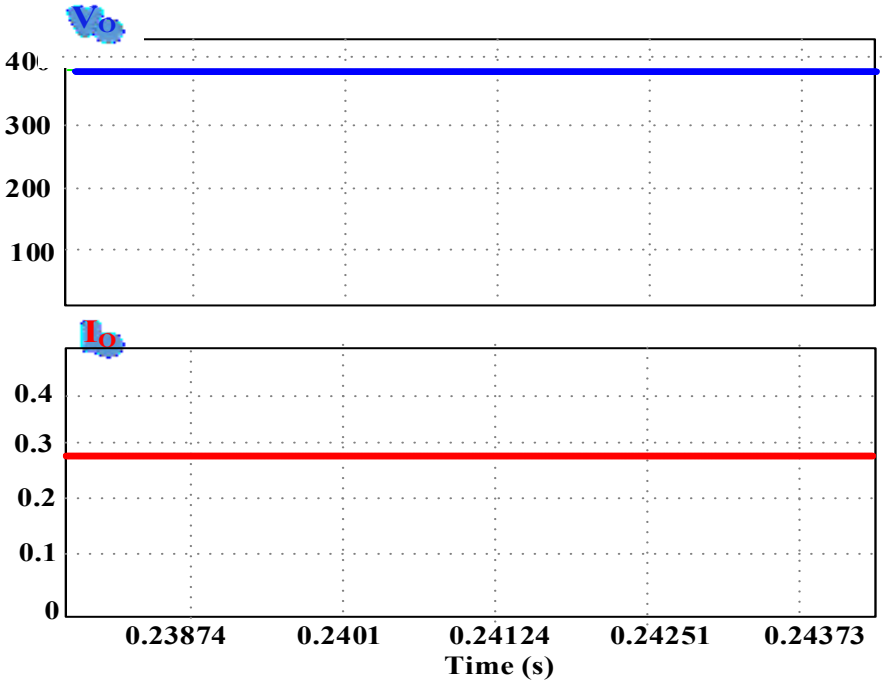


(b)

Fig. 2.7. Simulated waveforms depicting ZCS for primary side devices for V_{in}= 48V at (a) full-load (500W) and (b) light-load (100W) operation.



(a)



(b)

Fig. 2.8. Simulated waveforms for output voltage, V_o and output current I_o at (a) full-load (500W) and (b) light-load (100W) operation.

2.6.2 Experimental Results

A scaled-down 500W proof-of-concept laboratory prototype has been developed for the experimental verification of the analysis, design and the steady-state performance. The hardware module is developed for the same specifications used in simulation. Hardware component specifications are listed in Table 2.5. The TI DSP TMS20F28335 is used as a

TABLE 2.5: EXPERIMENTAL SETUP COMPONENT SPECIFICATIONS

Component	**Specifications**
Power switches, $\boldsymbol{S_1, S_2}$	SCT3060ALGC11-ND, 650V, 39A, 60mΩ
Input Boost inductors, L_{in}	55 x 28 x 21, EE Ferrite cores, 300μH
Series Resonant Inductor, L_{r1} and L_{r2}	EE ferrite core, L_{r1}= 1μH and L_{r2} = 0.7μH
Resonant capacitor, $\boldsymbol{C_r}$	HF Film capacitor, 8.5nF, 1000V
HF Centre Taped Transformer T_1	EE ferrite core, Primary turns, =10, 10 secondary turns = 45, L_{lk1}= 1.55μH, L_{lk2}= 1.8μH
Diodes, $\boldsymbol{D_{1-2}}$	STPSC20065D, 650V, 20A, V_f= 0.7V
Output capacitor, $\boldsymbol{C_1 C_2}$	80μF 450V electrolytic capacitor, 10nF film capacitor
Gate driver	HCNW3120

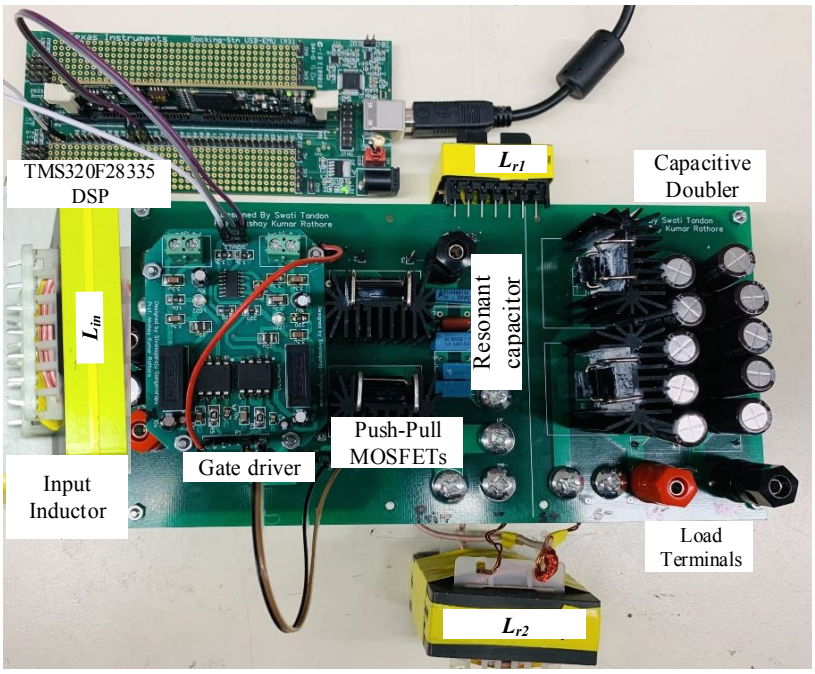


Fig. 2.9. Experimental setup of the proposed converter.

digital control platform to generate the gating signals for the converter in open-loop. Fig. 2.9 shows the top view of the hardware prototype. The experimental test results are recorded on digital storage oscilloscope.

Fig. 2.10(a) and (b) demonstrate the steady-state experimental waveforms under full-load (500W) condition for V_{in} = 42V and V_{in} = 48V respectively. It is observed that the voltage across the switch S_1 remains zero while the switch current (i_{S1}) goes negative during switching overlap, which then allows anti-parallel body diode conduction before the gating is forced off. This confirms soft-commutation of the MOSFET (S_1) with no overshoot in the switch voltage. Later the switch voltage starts rising, however, a slight ringing in the switch voltage can be seen due to device intrinsic snubber capacitor and parasitic inductance. In addition, the constant current is witnessed through the transformer primary when only one of the switches is conducting whereas sinusoidal current waveform is observed during gating overlap due to the resonance pulse for short duration. This leads to linearly charging the resonant capacitor (V_{Cr}) and hence, linearly increasing terminal volatge (V_{AB}) as depicted in Fig. 2.10(c). Similarly, the other switch S_2 also turns-off with ZCS in the remaining half switching cycle. Further, it should be noted that switching frequency is decreased from its maximum value ($f_{sw,max}$ = 200k Hz to 185 kHz) for a change in source voltage from 42V to 48V resulting in a regulated output voltage.

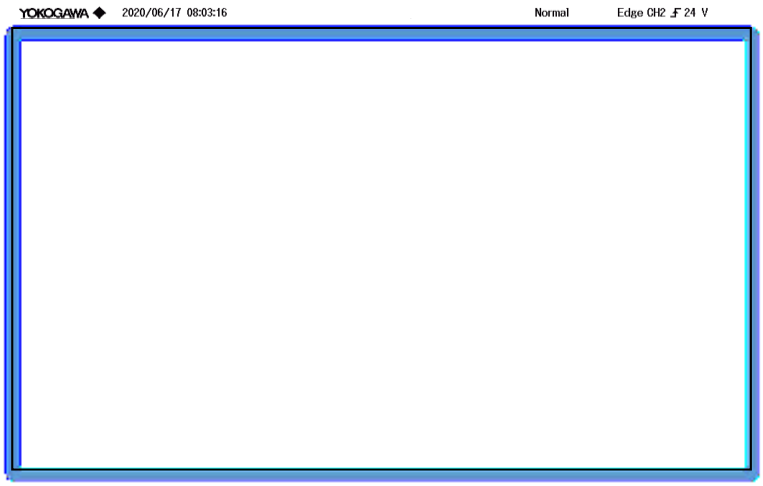
Fig. 2.11 (a) and (b) exhibit the experimental results confirming the ZCS turn-off and the voltage clamping of the semiconductor devices for half-load (250W) condition with two extreme source voltage points i.e V_{in} = 42V and V_{in} = 48V, respectively. Similar observations hold true for the half-load condition maintaing smooth commutation of the semiconductor devices. In addition, lower resonant energy with lower current peak and lower switch voltage are witnessed in Fig. 2.11(c). This results in relatively better conversion partial load efficiency compared to the other state-of-the-art converters.

Similarly, Fig. 2.12(a) and (b) respectively, validate the experimental steady-state operation under light-load (100W) condition for V_{in} = 42V and V_{in} = 48V, with duty ratio slightly lower than the full-load scenario in order to maintain constant overlap period for successful ZCS of the semiconductor devices. It is also witnessed from Fig. 2.12 that the resonance pulse covers very short portion of the switching cycle (particularly at low operating frequency) allowing lower resonant energy to bring soft switching without compromising on

the conversion efficiency. Likewise, the switch voltage remains zero at turn-off for extended time owing to the anti-parallel body diode conduction.

It is observed that the switch voltage stress decreases with decrease in output power further reducing the switching losses. The peak voltage stress across primary side MOSFETs are limited to ≈ 220V. However, a slight ringing in the switch voltage waveform can be seen due to device intrinsic snubber capacitor and PCB parasitic. It is also highlighted in Fig. 2.12(c), that peak of the switch current is significantly lower than the current peak at full-load condition. At the same time, the ratio of peak current to the input RMS current (I_{Lrp}/ I_{in}) is lower for the load below rated power, therefore, results in considerably lower conduction losses even at light load. Fig. 2.12(c) validates reduced values for the terminal voltage V_{AB}, the resonant inductor current I_{Lr}, and the resonant capacitor voltage V_{cr} resulting in lower switch voltage stress. It should be noted that V_{AB} is bipolar and balanced without any dc-offset. Fig. 2.13 presents the bar chart with varying resonant capacitor charge for different output power at nominal input voltage. This chart clearly elucidates the load dependent resonant energy, therefore utilizes lower resonant energy to bring soft switching at light-load condition.

As a result, the soft-commutation at turn-off eliminated the voltage spike which is an inherent problem with the current-fed converters. In addition, the experimental results confirm stiff voltage regulation under varying load and source voltage owing to the variable frequency control. Besides, Fig. 2.14 and Fig. 2.15 depict the experimental rectifier diode voltage and current waveforms for one leg with the extreme source voltages at full-load and light-load condition, respectively. ZCS turn-off of the diodes should be observed with blocking voltage equal to output voltage V_o. Utilizing Schottky diodes assisted in smooth turn-off with remarkably low reverse recovery and ringing. Fig. 2.16 interprets theoretical and measured switching frequency trend for the two extremities in the source voltage with different loading condition. The experimental switching frequency range is recorded to be 185–200 kHz at rated power. It is also witnessed from Fig. 2.16 that frequency deviation is subtle for large variations in input voltage as compared to the load change. Therefore, the proposed converter can operate safely from full-load down to 20% load with switching frequency band of 80-200 kHz. By using the analytical expressions derived in Section 2.4 and the datasheet specifications of the components used in the hardware prototype, the individual loss components for the rated power and 20% rated output power are calculated and listed in Table 2.6.

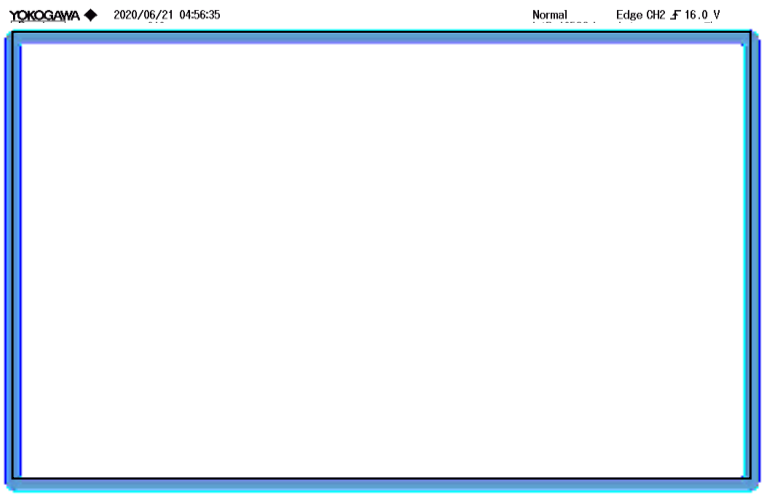


(a)

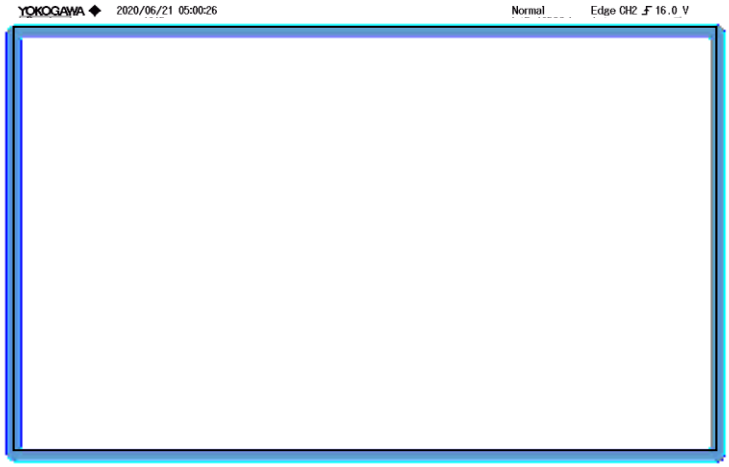
(b)

(c)

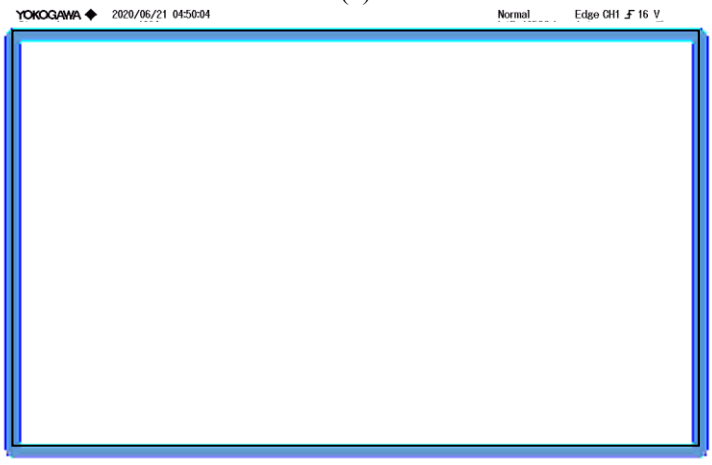
Fig. 2.10. Experimental waveforms for (a) gate-source voltage V_{gs1}, drain-source voltage V_{ds1}, switch current I_{S1} with V_{in} = 42V, f_{sw}=200 kHz *and* D = 0.63 (b) gate-source voltage V_{gs1}, drain-source voltage V_{ds1}, switch current I_{S1} with V_{in}= 48V, f_{sw}=185 kHz *and* D = 0.63 and (c) voltage $V_{AB,}$ resonant capacitor voltage V_{cr}, and series resonant tank current I_{Lr} at full load (500W).



(a)

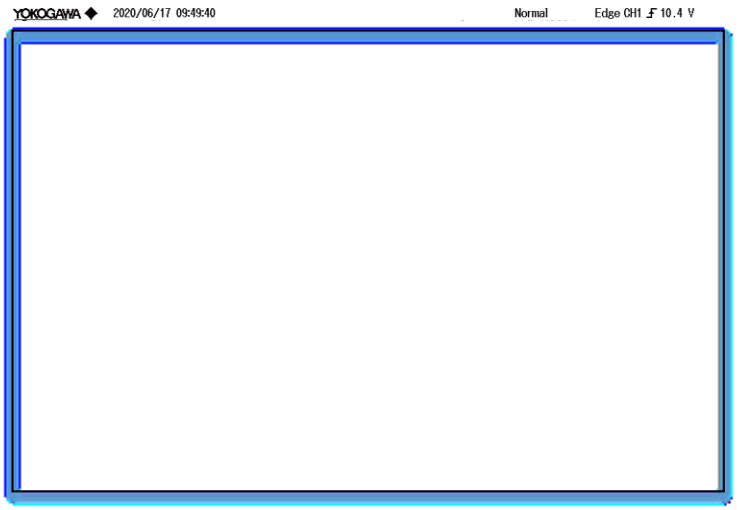


(b)

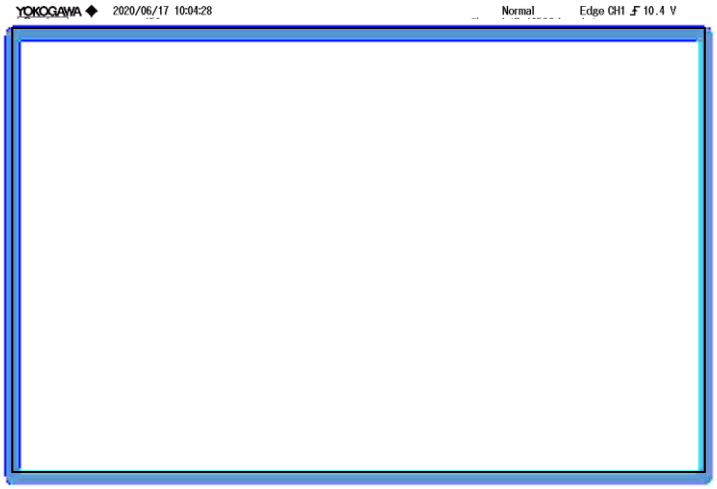


(c)

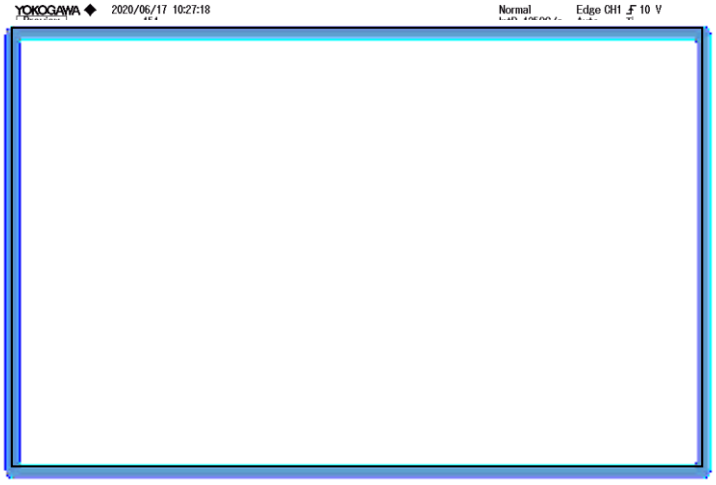
Fig. 2.11. Experimental steady-state waveforms for (a) gate-source voltage V_{gs1}, drain-source voltage V_{ds1}, switch current I_{S1} with V_{in} = 42V, f_{sw}=130 kHz *and* D= 0.63 (b) gate-source voltage V_{gs1}, drain-source voltage V_{ds}, switch current I_{S1} with V_{in}= 48V, f_{sw}=115 kHz *and* D= 0.63 (c) voltage $V_{AB,}$ resonant capacitor voltage V_{cr}, and series resonant tank current I_{Lr} at half load (250W).



(a)



(b)



(c)

Fig. 2.12. Experimental steady state waveform for (a) gate-source voltage V_{gs}, drain-source voltage V_{ds} , switch current I_{S1} with V_{in}= *42V*, f_{sw}=90 kHz *and D*=0.56 (b) gate-source voltage V_{gs}, drain-source voltage V_{ds} , switch current I_{S1} with V_{in}= *48V* , f_{sw}=75 kHz *and D*=0.56 (c) voltage $V_{AB,}$ resonant capacitor voltage V_{cr}, and series resonant tank current I_{Lr} at light-load (100W).

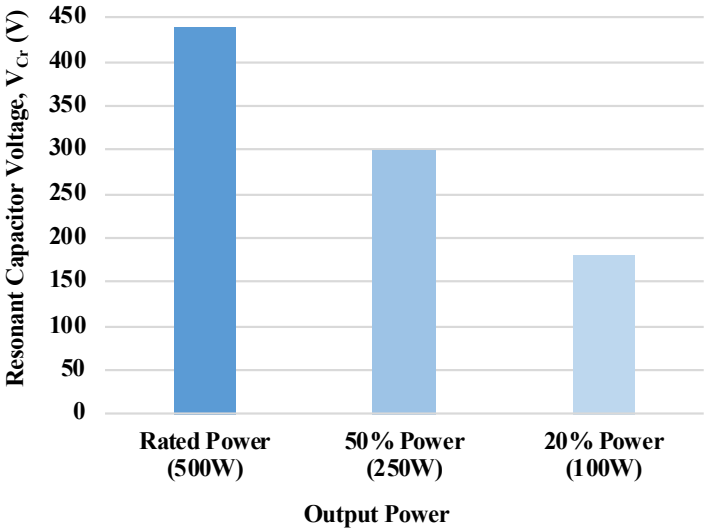


Fig. 2.13. Resonant capacitor charge for different output power at nominal input voltage.

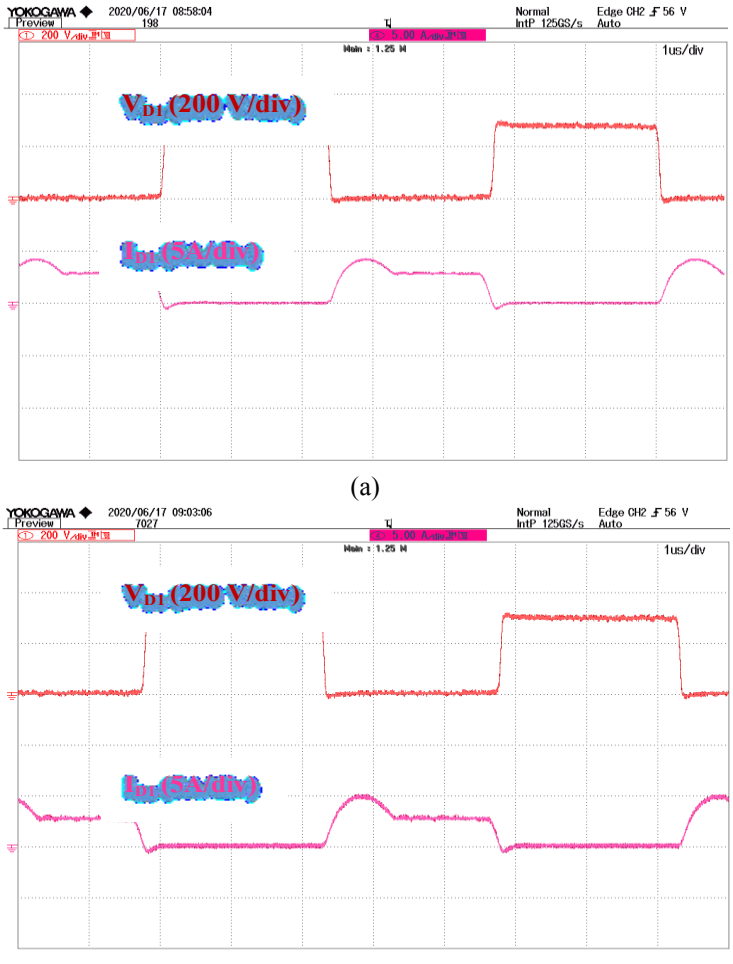


Fig. 2.14. Experimental results for secondary side rectifier diode current I_{D1} and voltage V_{D1} for (a) V_{in} = 42V and (b) V_{in} = 48V at full-load (500W).

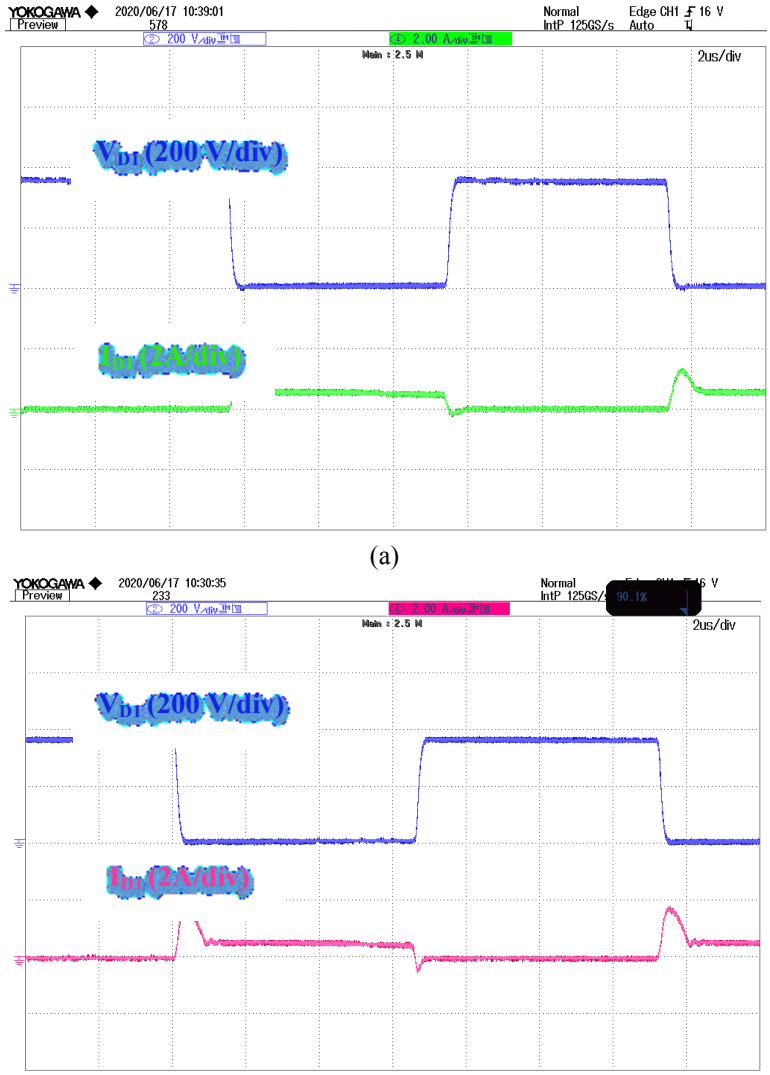


Fig. 2.15. Experimental results for secondary side rectifier diode current I_{D1} and voltage V_{D1} for (a) V_{in} = 42V and (b) V_{in} = 48V at light-load (100W).

Table 2.6 indicates that the conduction loss is the dominant segment predominantly occurring in semiconductor switches, diodes, HF transformer and input inductor. Determining these losses also assist in theoretical efficiency calculation. In this experiment, SiC based power devices are used with about 300-400 times lower drain-to-source ON-resistance (R_{DS_ON}) and exceptionally fast switching capabilities compared to the conventional silicon devices promoting compact magnetic components and heat sinks. Therefore, SiC devices can handle higher power densities leading to the cost saving and substantial performance

improvement.

Experimentally recorded efficiency curves for different loading condition at two extreme source voltages are depicted in Fig. 2.17. Maximum full-load efficiency of 96.2% for V_{in}= 48V and minimum efficiency of 93.2% for V_{in} = 42V is observed on the hardware prototype. The measured efficiency is very close to the calculated one validating mathematical analysis. The demonstrated results and discussion, validate the robustness of the proposed design for

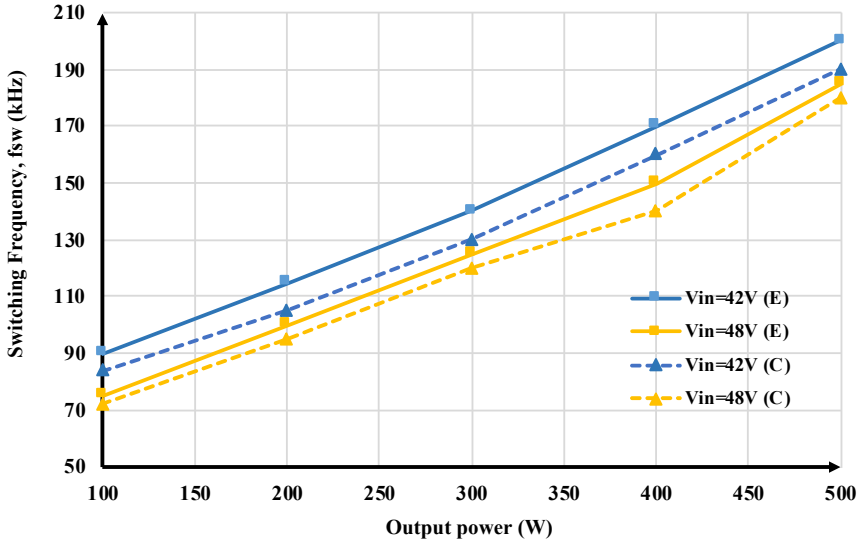


Fig. 2.16. Switching frequency trend with varying output power for two extreme input voltages (C: Calculated, E: Experimental value).

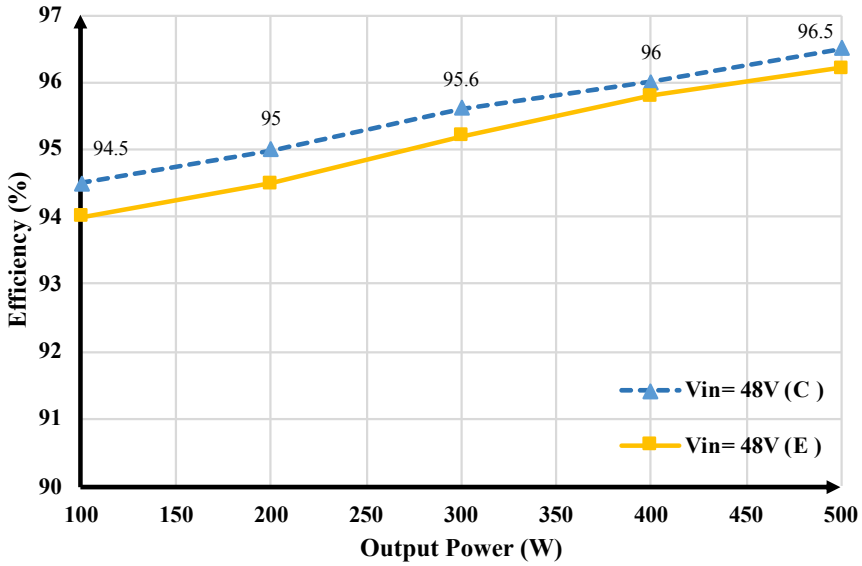


Fig. 2.17. Experimental efficiency curve with output power variation for nominal input voltage (C: Calculated, E: Experimental efficiency).

TABLE 2.6: CONVERTER ITEMIZED LOSSES AND THEORETICAL EFFICIENCY

Output power	500	100	500	100	W
Input voltage, V_{in}	48	48	42	42	V
Input current (rms)	10.41	2.08	11.90	2.38	A
Duty cycle, D	0.6	0.56	0.6	0.56	
Loss Type					
MOSFET conduction loss	9.0	1.1	10.80	1.0	W
MOSFET switching loss	1.40	0.85	1.38	0.80	W
Rectifier diode loss	2.10	1.60	2.50	1.50	
Total semiconductor losses	12.50	3.55	14.58	3.30	W
Input Boost inductor loss	2.50	0.80	3.50	0.95	W
HF Transformer loss	1.50	0.30	1.90	0.52	W
Gate drive loss	0.116	0.048	0.136	0.04	W
Auxiliary (capacitor loss/stray loss)	0.70	0.90	0.704	1.33	W
Total power losses	17.50	5.6	20.8	6.2	W
Efficiency	96.5	94.4	95.8	93.8	%

the source voltage variation, and load current conditions. Moreover, it can be established from the experimental results that the proposed design is able to achieve wide range ZCS and switch voltage clamping allowing safe integration of alternative energy sources with improved efficiency and high-power density.

2.7 Conclusion

In this Chapter, a current-fed push-pull ZCS dc-dc converter with series resonant circuit is investigated for low voltage sources. The steady-state operation, analysis and design have been explained in detail in this Chapter. The major accomplishments of the proposed converter include snubberless ZCS operation of the semiconductor devices with effective voltage clamping during their turn-off. By generating short series LC resonance-pulse, load adaptive ZCS is possible along with lower circulating and peak currents through the components. Therefore, this topology claims reduced conduction losses and lower switch voltage rating and heat sink requirements, thus reducing overall footprints. Moreover, push–pull topology allows the use of a single boost inductor and only two active devices having shared ground polarity with the source, hence, easing gate drive circuit with simpler current return loops and minimum filtering.

Scaled-down laboratory prototype has been built and tested to validate the analysis, operation, and design to verify the expected claims. The experimental waveforms are in state of concordance with the simulation results obtained from PSIM 11.1. The proposed resonance-pulse approach proves to be an effective and simple solution to resolve the innate problem with current-fed converter without compromising on the converter performance, cost and size. Peak efficiency of 96.2% has been recorded at the rated output power with source voltage, V_{in}= 48V for the developed laboratory hardware prototype. Hence, considering aforementioned merits, it is clear that the proposed push-pull design is well suited for medium power high voltage gain applications. Many such diverse applications include PV enabled back-up power supply, microinverter, etc.

Chapter 3

Series Resonance-Pulse Assisted Current-Fed Half-Bridge Converter

3.1 Introduction

Push-pull converter topology studied in Chapter 2 is justified for the low voltage high current applications utilizing inherent merits of current-fed circuits, particularly low input current ripple and high voltage gain. Despite the use of only two active semiconductor devices with common grounding feature, push-pull converters result in higher kVA rating of the HF transformer ($\sqrt{2}$ times) along with a complex centre tapped design and a risk of non-identical winding inductance. On the contrary, the half-bridge configuration proposed in this Chapter has the potential to deliver higher voltage gain with reduced transformer size (in terms of reduced turns ratio and reduced kVA) and simple circuit configuration. In half-bridge topology, source current ripple and voltage/current stress across various semiconductor switches, boost inductors, and HF transformer are reduced by nearly half. Therefore, this topology is a cost-effective solution owing to the lower component count, low rated components, smaller form factor with easy implementation and higher efficiency.

This chapter studies and analyses the application of the series resonance-pulse concept in current-fed half-bridge configuration to achieve the following objectives:

a) To eliminate the switch turn-off voltage spike facilitating smooth commutation of the semiconductor devices without compromising conversion efficiency.
b) To limit the circulating energy together with peak and rms current in the converter through the short-resonant-pulse.
c) Narrow switching frequency range for source voltage variation.

This Chapter investigates upon a series resonance-pulse concept for the current-fed half-bridge converter with operation, detailed mathematical analysis and design. This Chapter is organized as follows: Section 3.2 presents the converter steady-state operation and analysis with mathematical expressions for each interval. Section 3.3 illustrates the design procedure

with relevant design equations for given specifications. Section 3.4 presents steady-state simulation results and experimental results obtained from the scale-down hardware prototype rated at 500W to validate the proposed converter operation and design.

3.2 Current-fed Half-bridge DC/DC Converter Topology with Series LC resonant tank

Current-fed ZCS half-bridge dc-dc converter topology with interleaved boost at the primary and voltage-doubler rectifier at the secondary to offer higher voltage gain is shown in Fig. 3.1. Partial resonance is established using series LC resonant branch to realize ZCS of the semiconductor devices. A short resonance pulse appears during overlap conduction time of the two semiconductor switching devices (S_1 and S_2), causing natural current reduction in an outgoing device to zero before the gating signal is forced-off. The current from the outgoing switch is gradually transfers to the other incoming switch. Soft device turn-off eliminates the turn-off switching losses and more importantly, avoids additional snubber circuit to clamp the voltage spike across the semiconductor devices in current-fed converters.

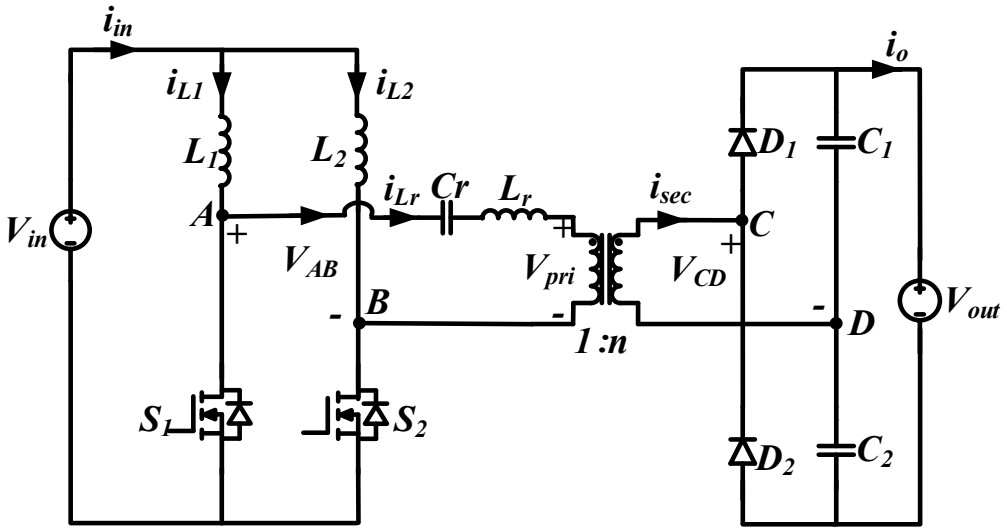


Fig. 3.1. Proposed series-LC resonant-pulse current-fed half bridge dc-dc converter topology.

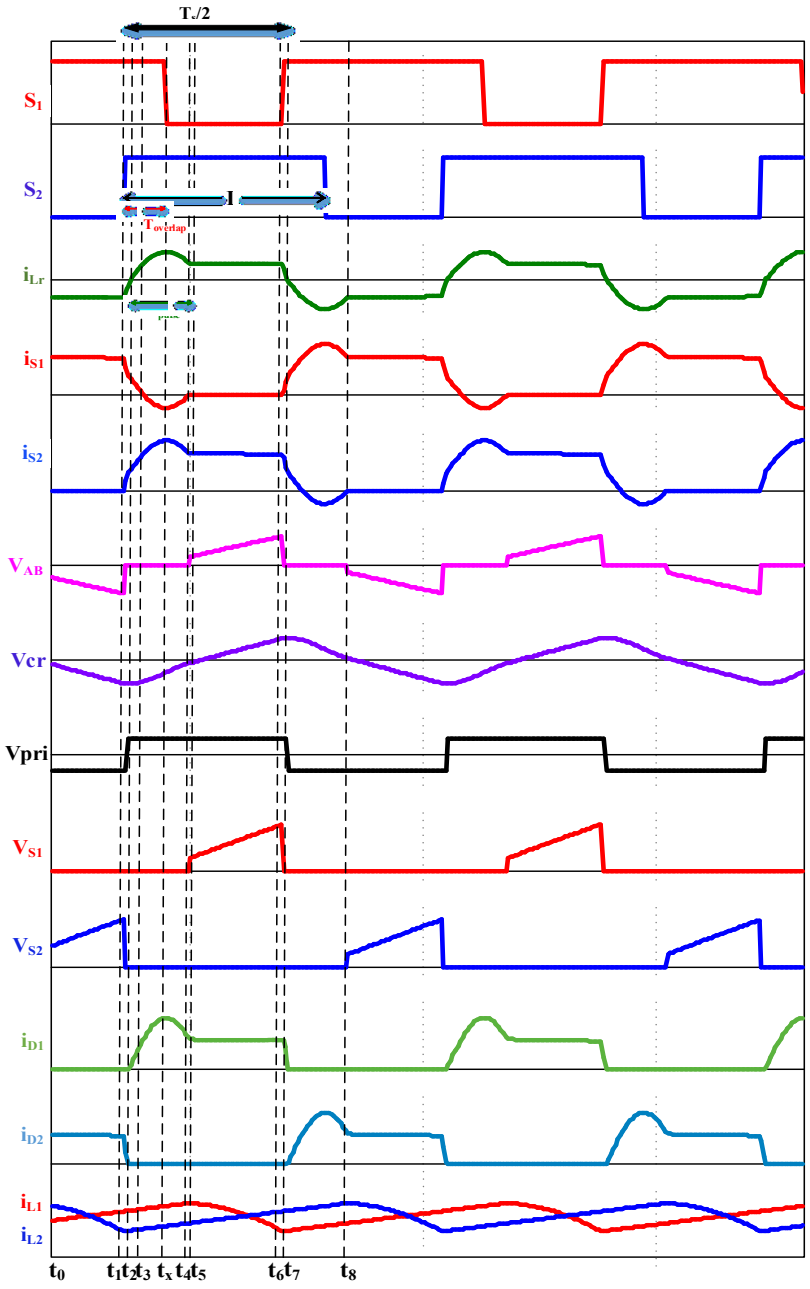


Fig. 3.2. Steady state operating waveforms for the current-fed half-bridge topology.

Fig. 3.2 shows the theoretical steady-state operating waveforms of the converter for D > 0.5 with switches S_1 and S_2 operated with gating signals 180º phase shifted, with a desired overlap. Series resonance-pulse is obtained by the transformer leakage inductance and an additional series capacitor to bring soft-switching of the switching devices. Moreover, due to the series resonant capacitor, the resonant energy is load-dependent that varies with the resonant tank

current $\left(V_{Cr} = \frac{1}{C_r}\int_{t_o}^{t} i_{Lr}(t)\,dt\right)$. Therefore, reasonably lower peak and rms current through the switches along with lower I_{Lrp}/I_{in} ratio are observed at light-load condition. As a result, circulating current in the circuit is remarkably reduced leading to reduced conduction losses. Power transfer is regulated by means of variable frequency constant overlap control with two major objectives; 1) regulated dc output voltage and 2) ZCS of the primary side active devices for variations in load current and input voltage. As the frequency decreases at light load, the overlap duration increases, therefore slight adjustment in duty cycle is desired to provide adequate overlap period ensuring soft-commutation of the semiconductor devices.

3.3 Steady State Operation and Analysis

Steady-state operation for the half switching period is explained for the steady-state analysis, which is divided into five major intervals as shown in Fig. 3.3. The analysis repeats for the other half cycle with other symmetrical devices conducting. Following assumptions are made in order to understand the operation and analysis of the converter:

1. All the semiconductor devices, inductors and capacitors are ideal and lossless.
2. Input inductors are sufficiently large to maintain constant current through them.
3. Output capacitors are large enough to maintain constant output voltage.
4. Transformer leakage inductance L_{lk} is considered as a part of the resonant tank circuit.

Interval 1 (t_0-t_1): (Fig. 3.3(a))

During this interval, switch S_1 is conducting while S_2 is off and transferring power to the load through diode rectifier D_2 as shown in Fig. 3.3(a). Current flowing through switch S_1 remains constant at I_{in} while a constant current $(-\frac{I_{in}}{2})$ flows through the transformer primary. This interval allows the resonant capacitor to charge linearly by the constant current resulting in linearly changing bridge voltage V_{AB}. Mathematical equations for the current through the resonant branch and semiconductor switches are given as;

$$i_{\mathrm{Lr}}(t) = -\frac{I_{in}}{2} \tag{3.1}$$

$$i_{\mathrm{S1}}(t) = I_{in} \quad and \quad i_{\mathrm{S2}}(t) = 0 \tag{3.2}$$

Voltage across the resonant capacitor can be expressed as,

$$V_{\mathrm{cr}}(t) = V_{\mathrm{cr}}(t_{\mathrm{o}}) + \frac{1}{C_{\mathrm{r}}}\int_{t_0}^{t} -\frac{I_{\mathrm{in}}}{2}dt \tag{3.3}$$

$$V_{\mathrm{cr}}(t) = V_{\mathrm{cr}}(t_{\mathrm{o}}) - \frac{I_{\mathrm{in}}}{2C_{\mathrm{r}}}(t - t_0) \tag{3.4}$$

Using boundary conditions, time duration for this interval can be calculated as:

$$T_{10} = \frac{T_s}{2} - T_{41} \tag{3.5}$$

Interval 2 (t_1-t_2): (Fig.* 3.3(b)*)

This interval begins when the switch S_2 is turned-on, with its internal capacitor discharges in a short interval of time. The current through the outgoing switch S_1 starts reducing while the current through the incoming switch S_2 starts increasing along with the increasing resonant current i_{Lr} due to positive voltage appearing across the resonant inductor. Mathematical equations during this interval can are presented below.

$$i_{\mathrm{Lr}}(t) = -\frac{I_{\mathrm{in}}}{2} + \frac{1}{L_r}\left(\frac{V_{out}}{2n} - V_{cr}(t)\right)(t - t_1) \tag{3.6}$$

$$i_{\mathrm{S1}}(t) = I_{\mathrm{in}} - \frac{1}{L_r}\left(\frac{V_{out}}{2n} - V_{cr}(t)\right)(t - t_1) \tag{3.7}$$

$$i_{\mathrm{S2}}(t) = \frac{1}{L_r}\left(\frac{V_{out}}{2n} - V_{cr}(t)\right)(t - t_1) \tag{3.8}$$

$$V_{\mathrm{cr}}(t) = V_{\mathrm{cr}}(t_1) + \frac{1}{C_r}\int_{t_1}^{t} i_{Lr}(t)\,dt \tag{3.9}$$

At the end of this interval, series resonant current, i_{Lr} linearly approaches zero and the bridge output voltage V_{AB} clamped to zero with positive voltage appearing across the transformer primary. Final values at instant t_2 are:

$$i_{Lr}(t_2) = 0,\ V_{AB} = 0 \tag{3.10}$$

From (3.6) and (3.10), duration of this mode T_{21} can be computed as:

$$T_{21} = \frac{I_{\mathrm{in}}L_r}{2 * \left(\frac{V_{\mathrm{out}}}{2n} - V_{\mathrm{cr}}(t_2)\right)} \tag{3.11}$$

From (3.9), $$V_{cr}(t_2) = -V_{cr\_peak} = V_{cr}(t_1) - \frac{3I_{in}}{8C_r}(T_{21}) \tag{3.12}$$

Interval 3 (t_2-t_3): (Fig. 3.3(c))

At instant t_2, current through the resonant branch reverses its polarity, which in turn alters the transformer primary reflected voltage to $\frac{V_{out}}{2n}$ causing diode D_1 to conduct. During this overlap period when both the switches are conducting, resonance initiates between L_r and C_r causing sinusoidally increasing current through the transformer primary. Consequently, the resonant current reaches to $I_{in}/2$ value with the outgoing switch current i_{S1} reaching zero. The equations governing this interval are given as follows;

The resonant tank parameters can be computed utilizing resonant frequency, (ω_o) and its characteristics impedance (Z_o).

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \ , \qquad Z_o = \sqrt{\frac{L_r}{C_r}} \ \ and \ \ \omega_o = \frac{1}{\sqrt{L_r C_r}} \tag{3.13}$$

Resonant current and switch current vary sinusoidally due to resonance, which are given by the following equations;

$$i_{Lr}(t) = \frac{V_{eff}}{Z_o} \ sin(\omega_o(t - t_2)) \tag{3.14}$$

$$i_{S1}(t) = \frac{I_{in}}{2} - \frac{V_{eff}}{Z_o} sin\omega_o(t - t_2) \tag{3.15}$$

$$i_{S2}(t) = \frac{I_{in}}{2} + \frac{V_{eff}}{Z_o} sin\omega_o(t - t_2) \tag{3.16}$$

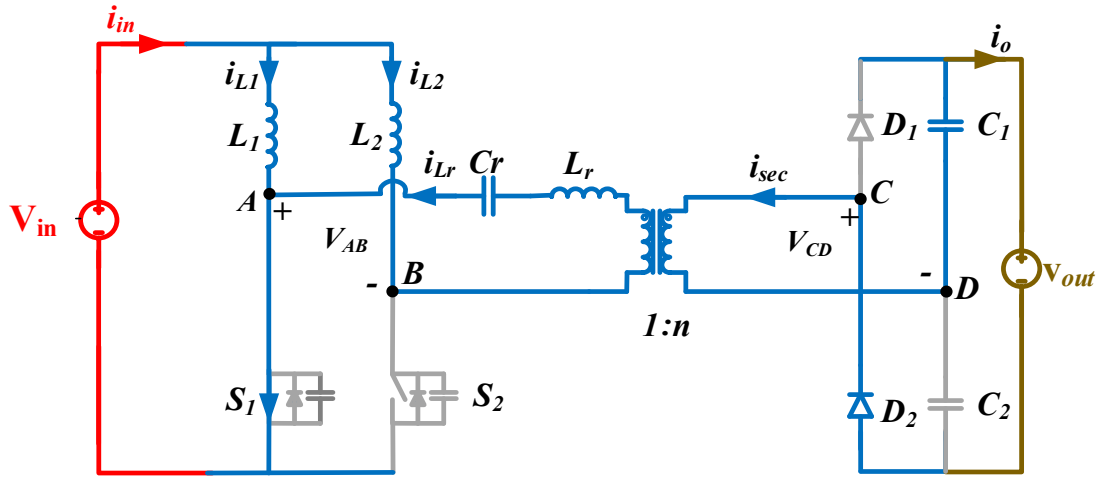
where V_{eff} can be expressed as:

$$V_{AB\_peak} = V_{eff} = \frac{V_{out}}{2n} + V_{cr\_peak} \tag{3.17}$$

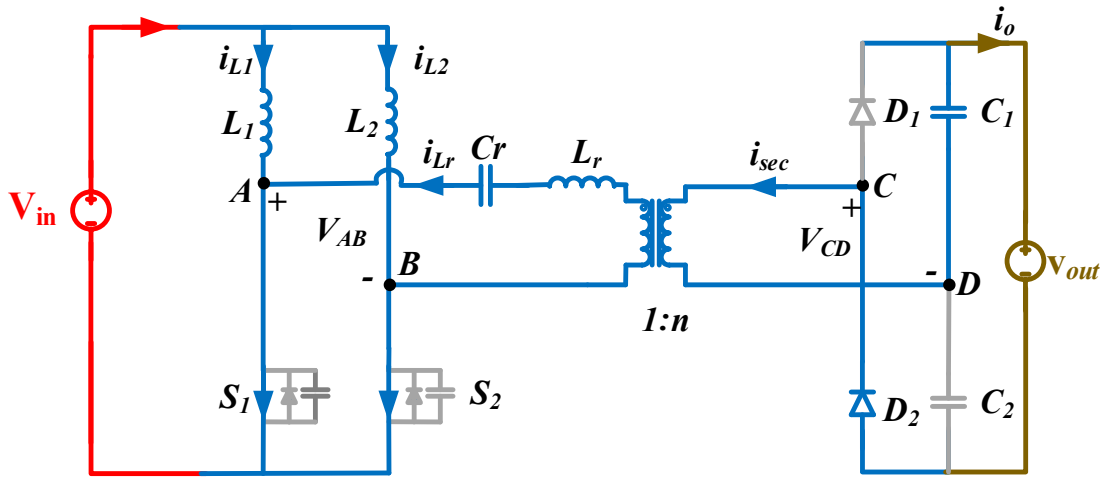
Further, V_{eff} can be written as:

$$V_{eff} = \frac{V_{out}}{2n} X \tag{3.18}$$

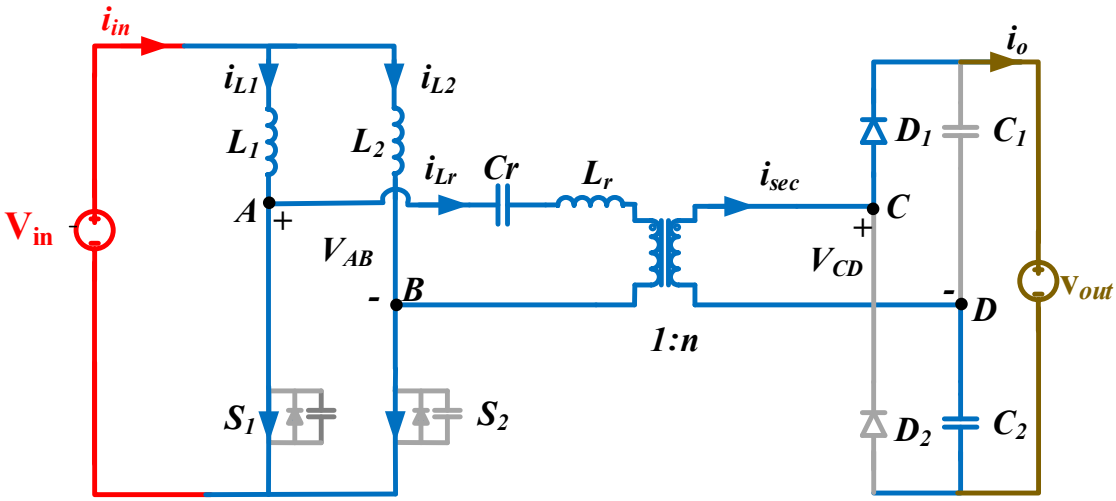
where X can be defined as, $$X = \left(1 + \frac{2nV_{cr\_peak}}{V_{out}}\right) \tag{3.19}$$


i_{in}
i_{L1}
i_{L2}
L_1
L_2
i_{Lr}
Cr
L_r
i_{sec}
i_o
D_1
C_1
V_{in}
A
V_{AB}
B
C
V_{CD}
D
V_{out}
1:n
S_1
S_2
D_2
C_2

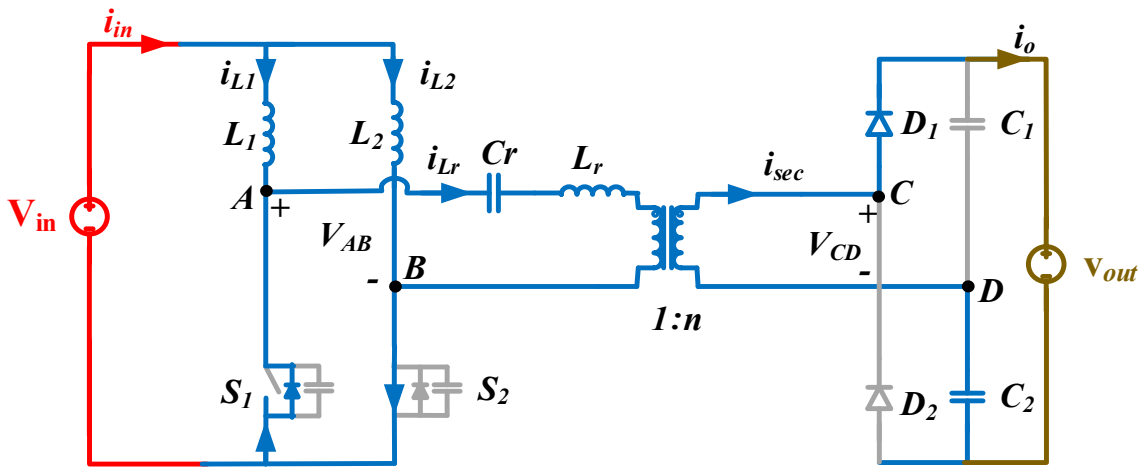
(a)


i_{L1}
i_{L2}
L_1
L_2
i_{Lr}
Cr
L_r
i_{sec}
i_o
D_1
C_1
V_{in}
A
V_{AB}
B
C
V_{CD}
D
V_{out}
1:n
S_1
S_2
D_2
C_2

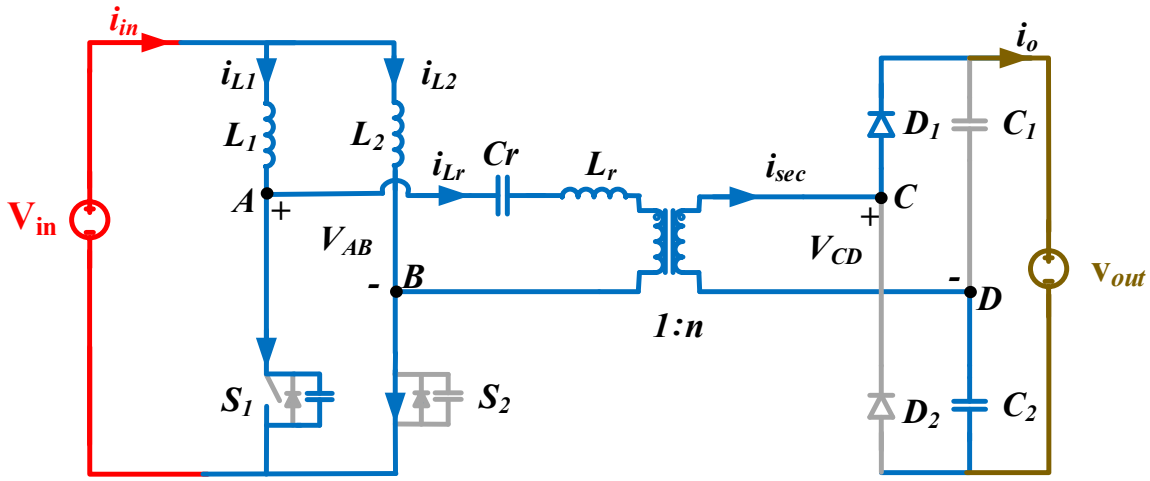
(b)


i_{in}
i_{L1}
i_{L2}
L_1
L_2
i_{Lr}
Cr
L_r
i_{sec}
i_o
D_1
C_1
V_{in}
A
V_{AB}
B
C
V_{CD}
D
V_{out}
1:n
S_1
S_2
D_2
C_2

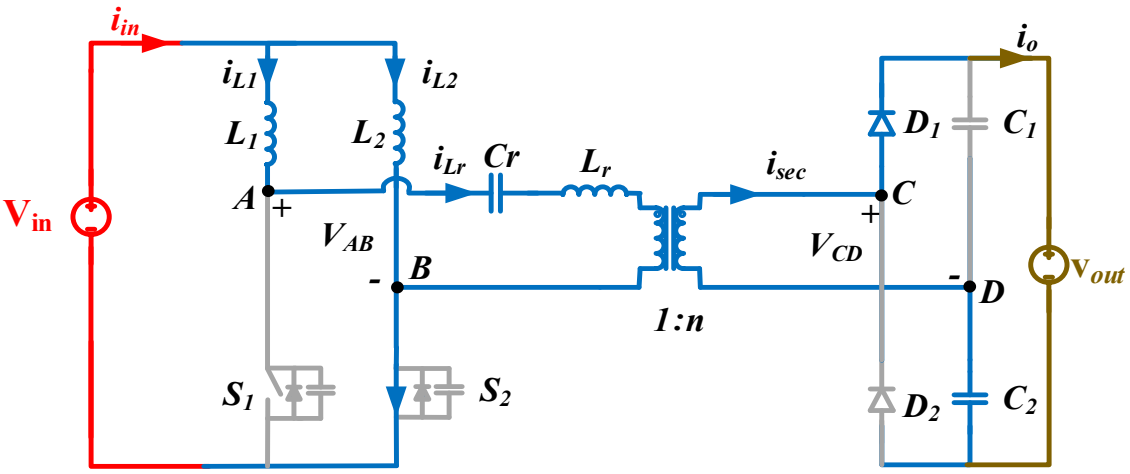
(c)


i_{in}
i_{L1}
i_{L2}
L_1
L_2
i_{Lr}
Cr
L_r
i_{sec}
i_o
D_1
C_1
V_{in}
A
V_{AB}
B
C
V_{CD}
D
V_{out}
1:n
S_1
S_2
D_2
C_2

(d)


i_{in}
i_{L1}
i_{L2}
L_1
L_2
i_{Lr}
Cr
L_r
i_{sec}
i_o
D_1
C_1
V_{in}
A
V_{AB}
B
C
V_{CD}
D
V_{out}
1:n
S_1
S_2
D_2
C_2

(e)


i_{in}
i_{L1}
i_{L2}
L_1
L_2
i_{Lr}
Cr
L_r
i_{sec}
i_o
D_1
C_1
V_{in}
A
V_{AB}
B
C
V_{CD}
D
V_{out}
1:n
S_1
S_2
D_2
C_2

(f)

At the end of this mode, $i_{Lr}(t_3) = \frac{I_{in}}{2},\ i_{S1}(t_3) = 0$ (3.20)

Using boundary condition (3.20) in (3.15), time duration of this mode can be computed as:

$$T_{32} = \frac{1}{\omega_o}\sin^{-1}\left(\frac{I_{in}Z_o}{2 * V_{eff}}\right) \tag{3.21}$$

Interval 4 (t_3-t_4): (Fig. 3(d))

Since resonance period remains active during this mode, the resonant current (i_{Lr}) crosses $I_{in}/2$ value with the switch current i_{S1} decreasing below zero letting its anti-parallel body diode to conduct. This allows ZCS turn-off of the switch S_1, eliminating large voltage spike across it. Moreover, the resonant current reaches its peak value during this interval, which can be estimated as:

$$I_{Lr\_peak} = i_{Lr}(t_x) = \frac{V_{eff}}{Z_o} \tag{3.22}$$

For successful ZCS operation, resonant current peak must exceed $I_{in}/2$. Therefore, the peak resonant current expression allows estimation of desired tank impedance.

a) $I_{Lr\_peak} > \frac{I_{in}}{2}$ results in,

$$\frac{V_{eff}}{Z_o} > \frac{I_{in}}{2} \tag{3.23}$$

$$\Rightarrow\ Z_o < \frac{2 * \left(\frac{V_{out}}{2n} + V_{cr_{peak}}\right)}{I_{in}} \tag{3.24}$$

The resonance period ends at $t = t_4$ and current i_{Lr} reduces to $\frac{I_{in}}{2}$ value. At the end of this interval, current through switch S_1 remains zero while switch S_2 takes over with a constant current I_{in} through it.

$$i_{Lr}(t_4) = \frac{I_{in}}{2}, \qquad i_{S1}(t_4) = 0\ \ and\ \ i_{S2}(t_4) = I_{in} \tag{3.25}$$

Using boundary condition (3.25), and substituting (3.21), the total duration of the resonant pulse can be considered as T_{42}, which is given by

$$T_{42} = \frac{1}{\omega_o}\left(\pi - \sin^{-1}\left(\frac{I_{in}Z_o}{2 * V_{eff}}\right)\right) \tag{3.26}$$

Further, duration of this mode can be given as, $T_{43} = T_{42} - T_{32}$

Interval 5 (t_4-t_5): (Fig. 3(e))

During this mode, with ZCS turn off of the switch S_1, the device capacitance across the switch S_1 gets charged immediately. The switch voltage V_{DS1} builds up and blocks the switch S_1. The duration t_{45} is very short, therefore, can be neglected for the calculations.

Consequently, after time instant t_5, the operating intervals repeat in identical manner for the remaining half-cycle when switch S_2 takes over with S_1 blocked. Power is transferred to the load through diode D_1 shown in Fig. 3.3(f). Therefore, half-switching period can be represented as,

$$T_{50} = T_{61} = \frac{T_s}{2} \tag{3.27}$$

3.4 Design of the Converter

The systematic design procedure for the proposed converter is illustrated in this Section. Determination of the values of the components along with their rating is explained. The comprehensive converter design includes voltage gain, ZCS boundary condition and resonant tank values. Optimal design facilitates limiting the circulating currents and thus the conduction losses. Detailed design equations for each component of the converter are derived.

3.4.1 Voltage gain of the proposed converter

From steady-state waveforms in Fig. 3.2, the average output current expression can be computed as:

$$I_{o,avg} = \frac{V_{out}}{R_{FL}} = \frac{I_{Lr,avg}}{n} = \frac{1}{n}.\frac{2}{T_s}\int_0^{T_s/2} i_{Lr}(t)\ dt \tag{3.28}$$

Also, considering lossless power transfer with 100% efficiency, the following relation can be obtained;

$$I_{in} * V_{in} = \frac{{V_{out}}^2}{R_{FL}} \tag{3.29}$$

Using (3.28) and (3.29), voltage gain expression in terms of converter parameters can be acquired as.

$$M = \frac{n\left(1 + \frac{f_n r_n X}{2\pi}\left(1 - \sqrt{1-k^2}\right)\right)}{\left(\frac{1}{2} - \frac{f_n}{2}\left(1 - \frac{1}{\pi}sin^{-1}k + \frac{k}{2\pi}\right)\right)} \tag{3.30}$$

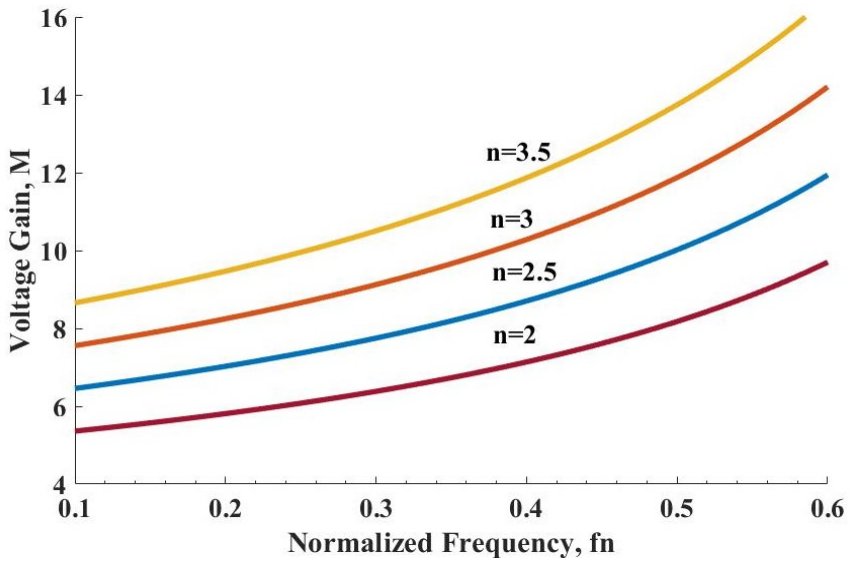


Fig. 3.4. Converter voltage gain characteristics.

where, n: Turn ratio of HFT, $k = \frac{M}{nr_nX}$;

f_n: Normalized frequency, $= \frac{f_s}{f_r}$;

r_n: Normalized load resistance, $= \frac{R_{FL}}{n^2 Z_o}$;

Voltage gain, M trend with normalized frequency, f_n for the different values of the turns ratio of HF transformer has been shown in Fig. 3.4. Gain characteristic curve assists in deciding optimal turns ratio of HF transformer to fulfil maximum voltage gain requirement. Moreover, to account for the variable voltage gain under different operating condition (e.g. input voltage and load current variation), theoretical switching frequency range can be computed using (3.30) to maintain constant voltage at the load. In this design example, the switching frequency range obtained is 50 kHz- 150 kHz for V_{in} range of 42V- 48V.

3.4.2 Voltage and current stresses in the converter

a) Voltage rating of the semiconductor switch primarily depends on the reflected output voltage across the transformer primary and peak resonant capacitor charge. Hence, the maximum switch voltage is load dependent and has linearly increasing characteristics due to the series capacitance in the conduction path.

$$V_{\mathrm{DS,rated}} = V_{\mathrm{cr\_peak}} + \frac{V_{out}}{2n} \tag{3.31}$$

Voltage rating of the rectifier diode is clamped at the output voltage.

$$V_{D1} = V_{D2} = V_{out} \tag{3.32}$$

b) Current rating of the components is decided by the rated root mean square (RMS) current flowing through them. Owing to the two interleaved boost inductors, current rating of the input inductor is $I_{in}/2$. From the steady-state waveforms, the switch conduction time can be utilized to derive the RMS current expressions. The switch rms current and the resonant inductor current are given by:

$$I_{\text{sw\_rms}} = \left[I_{in}^2 \left(\frac{1}{2} - \frac{f_s}{f_r} \left(\frac{1}{4} - \left(\frac{1}{4k}\right)^2 + \frac{k}{6\pi} - \left(\frac{\sqrt{1-k^2}}{8\pi k} \right) \right) + \frac{1}{\pi} \left(\left(\frac{1}{4k}\right)^2 - \frac{1}{2} \right) sin^{-1} k \right) \right]^{\frac{1}{2}} \tag{3.33}$$

$$I_{Lr\_rms} = \left[I_{in}^2 \left(\frac{1}{4} - \frac{1}{2}\frac{f_s}{f_r} \left(\frac{1}{4} - \left(\frac{1}{4k}\right)^2 + \frac{k}{6\pi} - \left(\frac{\sqrt{1-k^2}}{8\pi k} \right) \right) + \frac{1}{\pi} \left(\left(\frac{1}{4k}\right)^2 - \frac{1}{2} \right) sin^{-1} k \right) \right]^{\frac{1}{2}} \tag{3.34}$$

Rectifier diode current rating is governed by the average output current.

$$I_{D1-2} = I_{o,avg} \tag{3.34}$$

3.4.3 ZCS Boundary Condition

The resonant tank energy governs the soft switching range by storing sufficient energy for the body-diode conduction across the switch before its gating pulse is removed. The fundamental conditions for achieving ZCS under wide operating range can be summarized as;

a) $I_{Lr\_peak} > I_{in}/2$

From Fig. 3.2, it should be observed that the resonant current $i_{Lr}(t)$ must exceed $I_{in}/2$ value during gating overlap period proving a path for the internal body-diode conduction before the switch turns off. This condition poses a constraint on the selection of Z_o, which governs the ZCS range given by the following inequality:

$$Z_o < \frac{2 * \left(\frac{V_{out}}{2n} + V_{cr_{peak}} \right) * R_{FL} * V_{in}}{{V_{out}}^2} \tag{3.35}$$

Therefore, maximum value of Z_o can be determined from (3.35). Relatively smaller value of Z_o allows more energy to be stored in the resonant tank resulting in wider range of ZCS operation. However, lower Z_o leads to higher circulating currents and therefore more losses.

This calls for a conscientious resonant tank design to accomplish effective ZCS without aggravating the circulating/leakage currents.

b) $T_{pulse} > T_{overlap}$

Second vital condition requires resonant pulse duration to last longer than the gating overlap time. This ensures ZCS for wide range of load with large switching frequency.

As a result, the overlap time can be maintained constant by accommodating desired change in the operating frequency or by slightly varying the duty cycle. This implies:

$$T_{32} < T_{overlap} < T_{42} \tag{3.36}$$

3.4.4 Resonant Tank Design

Resonant tank impedance, Z_o being the critical parameter for the adequate resonant tank design must be calculated using extreme operating conditions with V_{in}= 42 to 48V at rated power. Once, the values of Z_o and resonant frequency f_r are determined, parameters L_r and C_r are obtained using the following flowchart in Fig. 3.5.

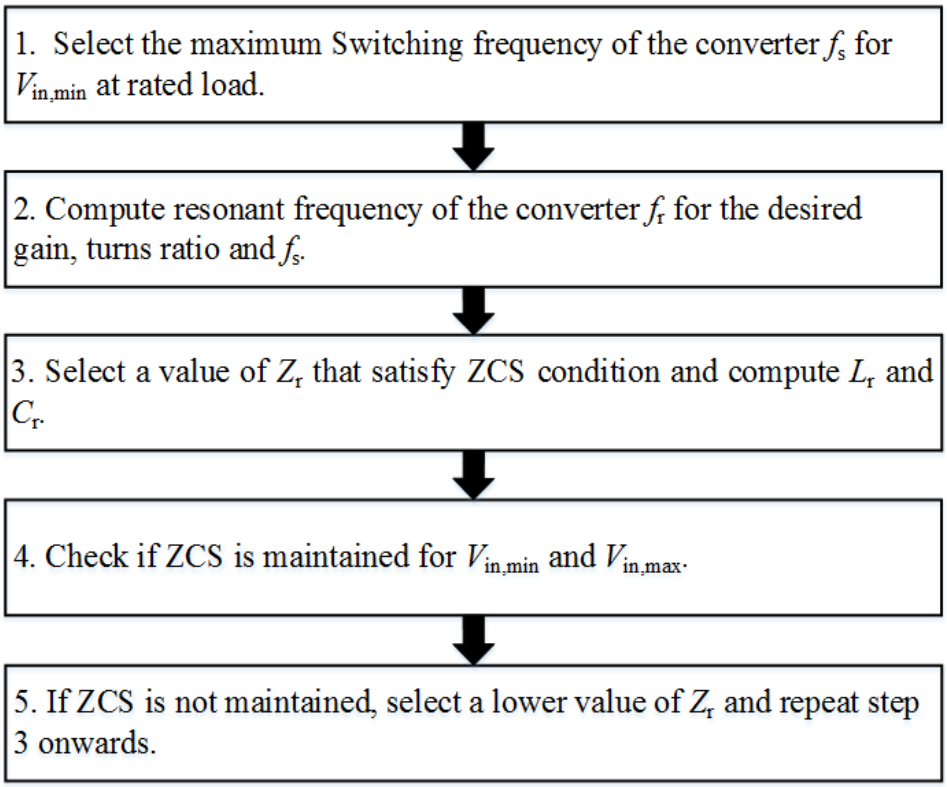


Fig. 3.5. Flowchart depicting the resonant tank design

3.4.5 Selection of Turns ratio of HF Transformer

As the static voltage gain of the converter is largely governed by the HF transformer turns ratio and normalized frequency as seen in (3.30). In this design example, turns ratio is expected to deliver maximum voltage gain with desired switching frequency at V_{in} = 42V at rated load while limiting the conduction losses. It should also be witnessed that the turns ratio directly affects the voltage and current stresses on the components. As a result, smaller turns ratio increases the voltage stress across the primary switches necessitating high voltage rating switches with inherently high on-state resistance ($R_{Ds,on}$). This further aggravates the conduction losses. Whereas, large turns ratio yields higher copper losses due to higher RMS current through the switch and resonant branch as evident from (3.36) further contributing to the conduction losses. Therefore, selection of turns ratio is a compromise between semiconductor switch rating and conduction losses. As a tradeoff, turns ratio of 2.5 is chosen for this design to meet the desired voltage gain while keeping minimum conduction losses.

3.4.6 Input Inductor Design

Input inductors are designed to have ripple-free source current. In this topology, ripple content primarily depends on the resonance pulse duration or the resonant frequency of the tank. The input boost inductor value for the allowable ripple (ΔI_{in}) is calculated as,

$$L_1 = L_2 = \frac{V_{in}\,(t_4 - t_1)}{\Delta I_{in}} \tag{3.37}$$

3.4.7 Output Capacitor Design

In a voltage doubler rectifier circuit, the two output capacitors carry half of the total output voltage (V_{C1}= V_{C2} =V_0/2). Output capacitors experience very low ripple content due to high switching frequency operation. The output capacitor value is computed based on the desired voltage ripple ($V_{o,ripple}$) using:

$$C_1 = C_2 = \frac{I_o}{2 f_s V_{o,ripple}} \tag{3.38}$$

3.5 Results and Performance

This Section presents the converter specifications given in Table 3.1 and the converter parameters given in Table 3.2 obtained using design equations presented in Section 3.4. Selection of the components is done to achieve minimum conduction losses under all operating condition. The proposed concept has been validated through simulation and experimental results for the set objectives.

3.5.1 Simulation Results

The steady-state operation and theoretical analysis has been verified using the PSIM 11.1.3 software and the detailed simulation results are presented in this Section. Open-loop control has been implemented to prove the proposed theory and analysis. Simulation results obtained with two extreme input voltages, V_{in} = 42 V and V_{in} = 48 V at rated-load (500W), and 20% load (100W) are illustrated in this Section. Fig. 3.6(a) and (b) depict the voltage appearing across the two switches and their respective gating signals at full-load and light-load condition. Switch voltage waveforms indicates linearly increasing trend due to series

TABLE 3.1 CONVERTER SPECIFICATIONS

Parameter	Value
Input Voltage, V_{in}	42-48V
Output voltage, V_{out}	380 V
Maximum output power, P_o	500W
Switching frequency, f_{sw}	50-150 kHz
Duty ratio, d	0.54-0.6

TABLE 3.2 DESIGN PARAMETERS

Parameter	Value
Resonant Inductor, L_r	3.5μH
Resonant Capacitor, C_r	73nF
Input Inductor, L_1, L_2	400μH
Output Capacitor, C_1, C_2	100μF
Turns ratio, n	2.5

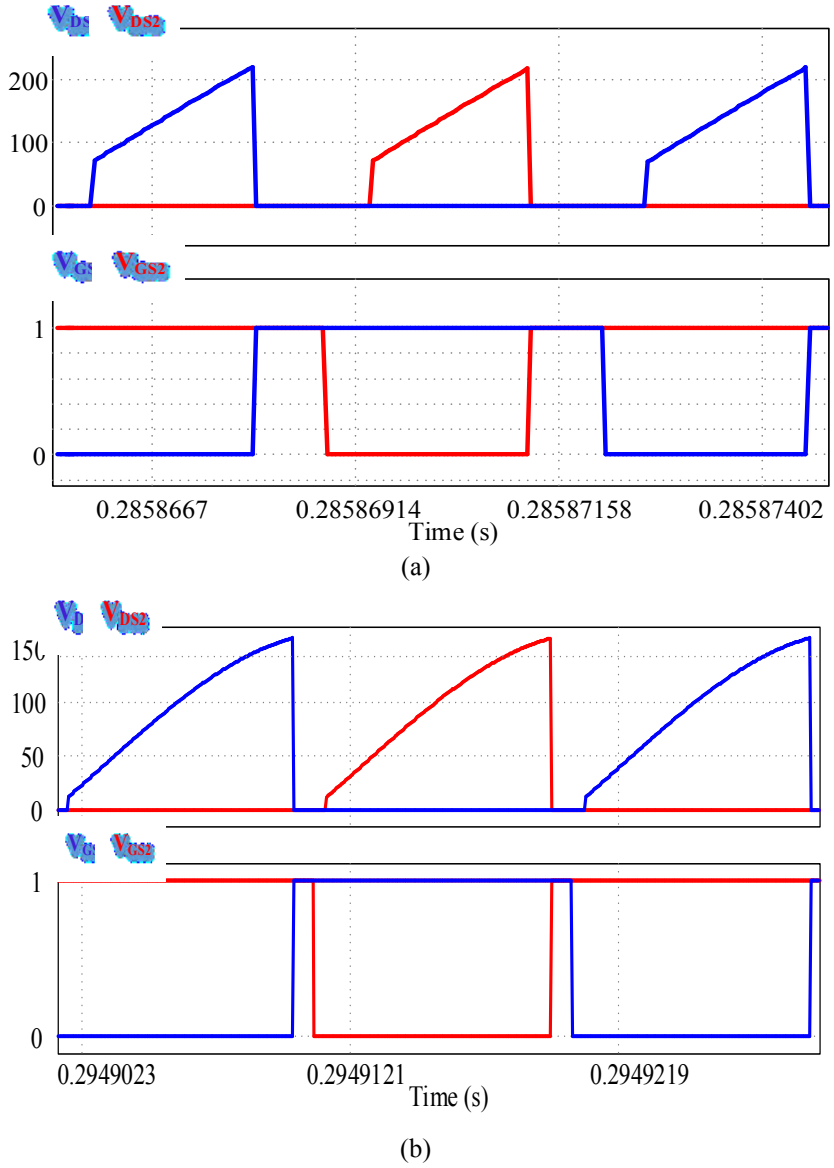
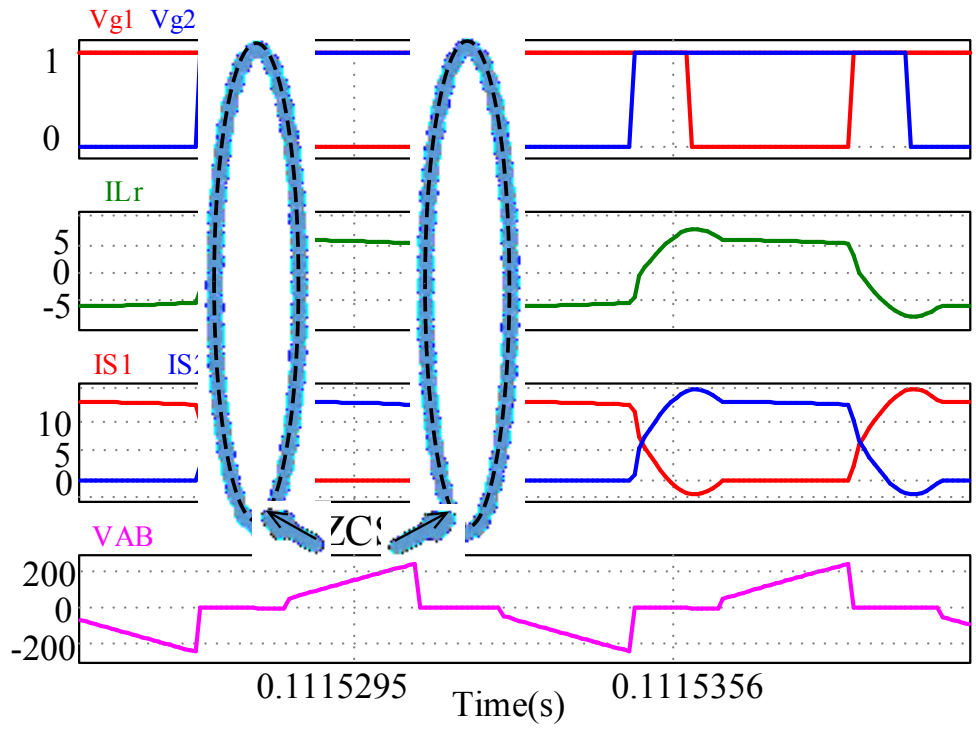
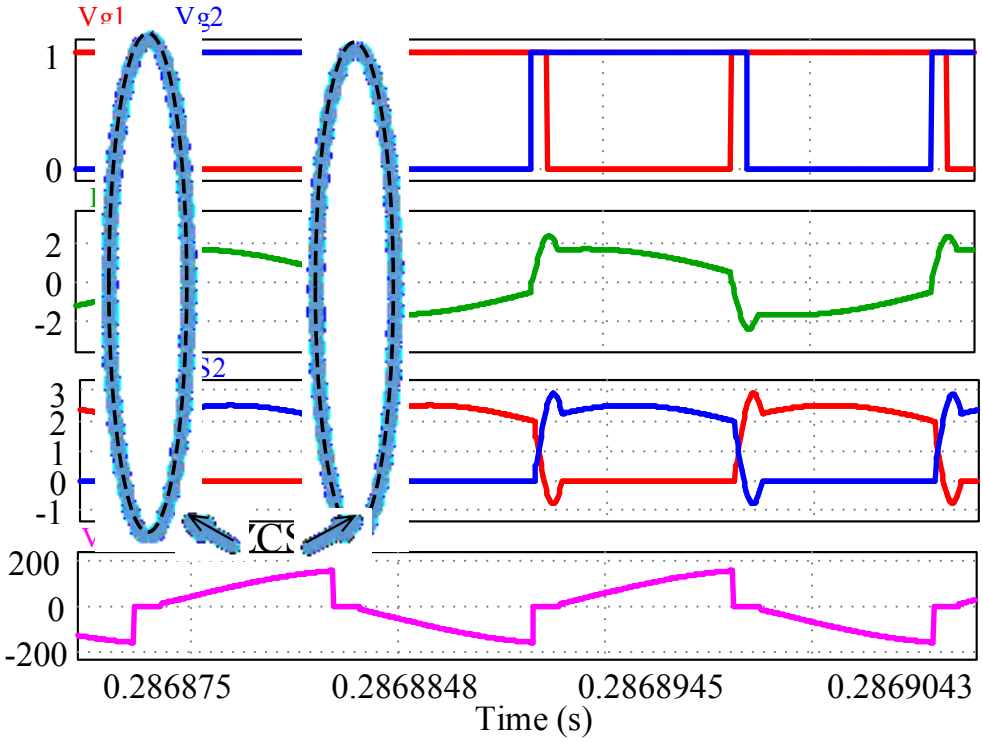


Fig. 3.6. Steady-state simulated waveforms for switch voltage, V_{DS1}, V_{DS2} with their respective gating signals V_{GS1} and V_{GS2} at (a) full-load (500W) (b) light-load (100W) condition.

resonant capacitor and validates the analysis. It should also be noted that the switch voltages are load dependent, and therefore, results in lower peak voltage for light-load condition. Simulation results depicted in Fig. 3.7(a) and 3.7(b) demonstrate ZCS of the semiconductor devices for $V_{in} = 42V$ at full-load and light-load condition respectively. The historical problem of the large turn-off voltage spike across the switching semiconductor devices is eliminated by effectively using the resonant inductor energy for the switch current to drop naturally to

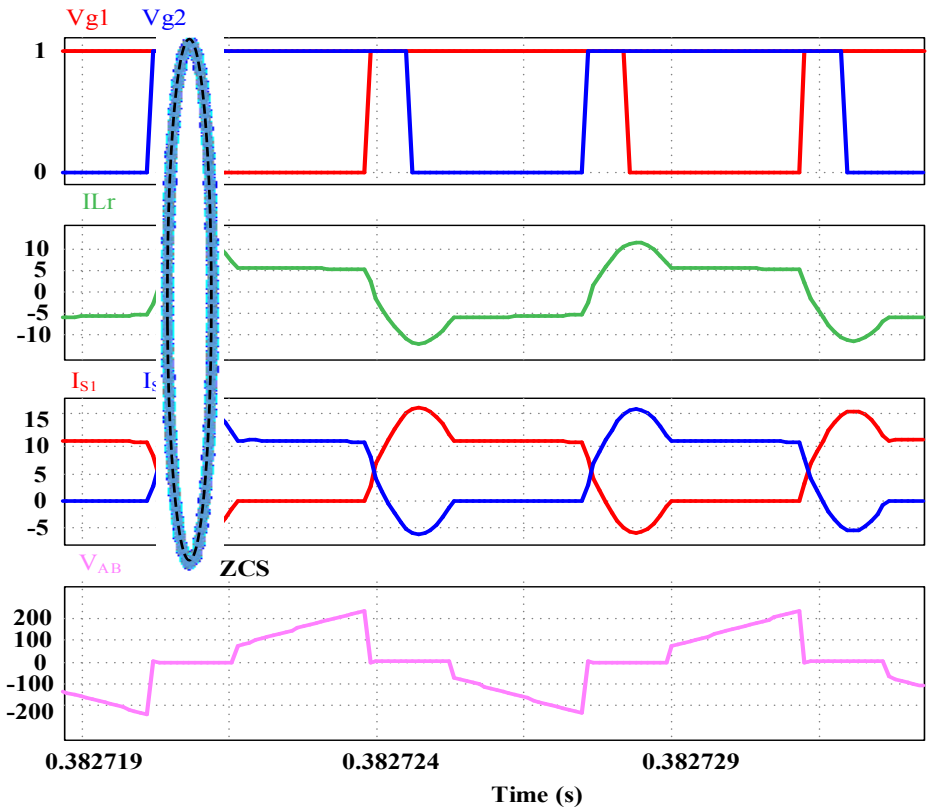


(a)

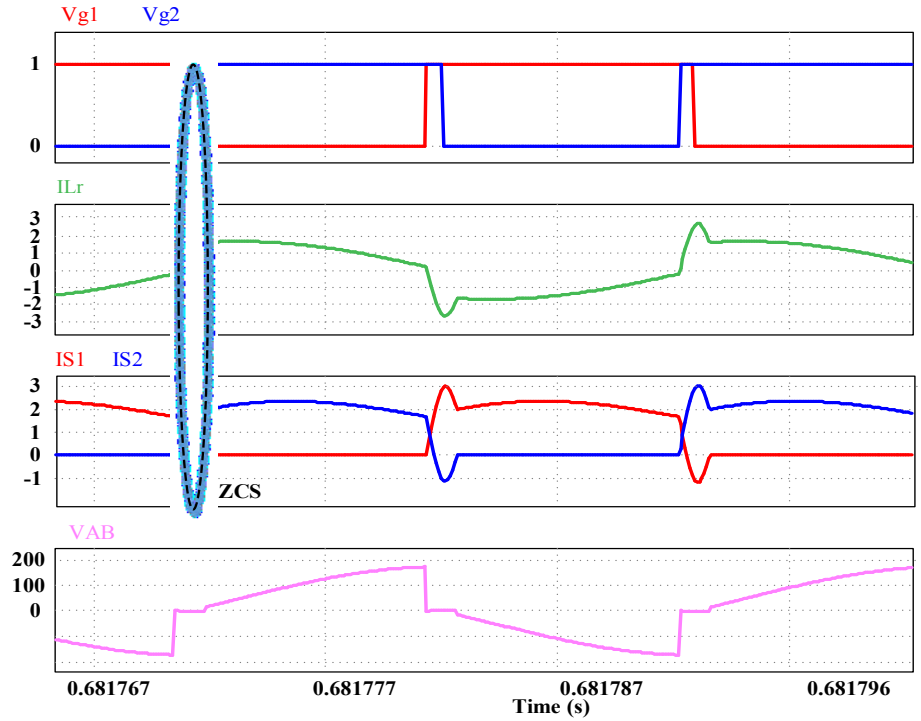


(b)

Fig. 3.7. Steady-state simulated waveforms depicting ZCS for primary side devices for V_{in}= 42V at (a) full-load (500W) and (b) light-load (100W) operation.

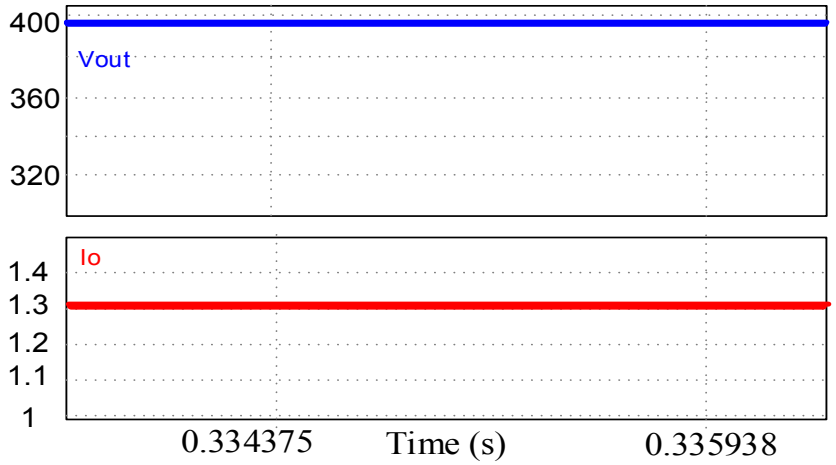


(a)

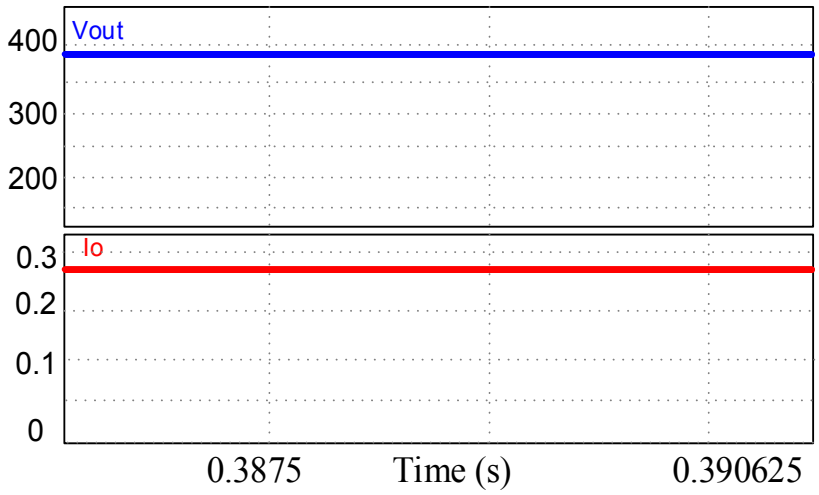


(b)

Fig. 3.8. Steady-state simulated waveforms depicting ZCS for primary side devices for V_{in} = 48V at (a) full-load (500W) and (b) light-load (100W) operation.



(a)



(b)

Fig. 3.9. Simulated waveforms for output voltage, V_o and output current I_o at (a) full-load (500W) and (b) light-load (100W).

zero and the anti-parallel diode conduction. Therefore, the gating pulse can be removed during the body-diode conduction time and the switch voltage V_{dS1} builds up gradually once the body-diode conduction terminates, eliminating any voltage spike. Fig. 3.7 also depicts the bipolar voltage waveform at the bridge output, V_{AB}, which is clamped to ($V_o/2n + V_{cr}$) in either direction. Moreover, the bridge output V_{AB} becomes zero during resonant period. Fig. 3.8(a) and 3.8(b) confirm successful ZCS operation and voltage clamping of the switches S_1 and S_2 for 48V source voltage under full-load and light-load condition respectively. It can be inferred from Fig. 3.8 that relatively higher current peak is witnessed as compared to the peak current value for 42V input. In addition, since lower resonant peak and lower leakage energy

is observed for light load condition in both cases (42V and 48V input), better part-load efficiency is recorded. Clearly, the ZCS operation is load adaptive owing to the series resonant feature. It can be concluded that the ZCS is maintained for the load variation from 100% to 20% without compromising converter efficiency. Fig. 3.9(a) and (b) affirm the strict output voltage regulation at 380V for full-load as well as light-load condition.

3.5.2 Experimental Results

A proof-of-concept, rated at 500W, laboratory prototype as shown in Fig. 3.10, is developed to evaluate the proposed converter operation and performance. Hardware components are selected based on their maximum voltage and current values estimated in the previous Section. Hardware details of the prototype are listed in Table 3.3. The high-frequency magnetic components including input inductors, resonant inductor and transformer are developed with EE ferrite core, and litz wire to minimize the magnetic losses. The converter is tested for different operating conditions listed in Table 3.4 and the detailed steady-state experimental waveforms are presented in this Section. The open loop control is implemented in the DSP TMS320F28335 to generate PWM signals. It has been verified in this section that experimental waveforms relate closely with the simulated steady-state operating waveforms.

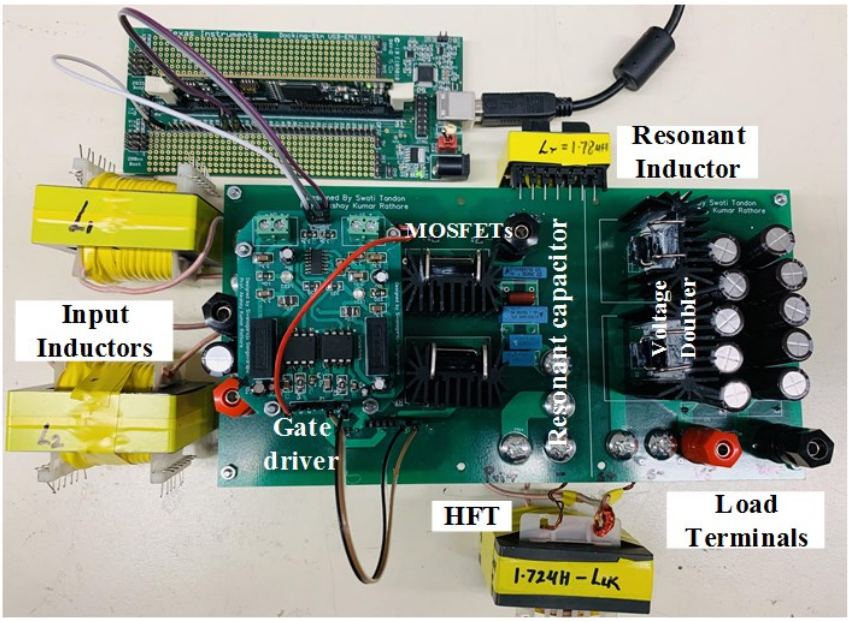


Fig. 3.10. Experimental setup of the proposed converter.

TABLE 3.3 HARDWARE COMPONENT SPECIFICATIONS

Component	Specifications
Boost inductors L_1, L_2	55 x 28 x 21 EE ferrite Core, 100μH
Converter Switches S_1, S_2	SCT3060ALGC11-ND, 650V,39A,60mΩ
Series Resonant Inductor, L_r	EE ferrite core, 1.78μH
Resonant Capacitor, C_r	73nF 1kV Film capacitor
HF Transformer, T_1	EE ferrite core, Primary turns, N_1 =10, secondary turns N_2 =25, L_{lk} = 1.724μH
Rectifier Diodes D_1, D_2	STPSC20065D, 650V, 20A, V_f= 0.8V
Output Capacitor, C_1, C_2	100μF 400V Electrolytic capacitor, 10nF film capacitor

Fig. 3.11 illustrates the steady-state experimental results for V_{in} = 42V at full-load (500W) operating at 150kHz switching frequency and 0.6 duty ratio. Fig. 3.11(a) shows the resonant capacitor voltage V_{cr}, half-bridge voltage V_{AB} and resonant current I_{Lr}. It should be observed that the capacitor charge varies linearly when only one of the switches conducts with the constant current through it, as opposed to the sinusoidally varying resonant current during switching overlap. Fig. 3.11(b) highlights no overshoot in the drain-to-source voltages across the two switches, V_{DS1}, V_{DS2} while the resonant current waveform i_{Lr} confirms ZCS turn-off of the semiconductor devices. Fig. 3.11(c) indicates the soft commutation instant of the semiconductor switch S1. From the i_{Lr} waveforms, it can be implied that the switch current naturally decreases to zero due to series resonance-pulse allowing body-diode conduction before the switch turns off. Therefore, gating signal V_{GS1} is removed during body-diode conduction period, thereby avoiding voltage overshoot across the switch.

TABLE 3.4 EXPERIMENTAL VALUES FOR DIFFERENT OPERATING CONDITIONS

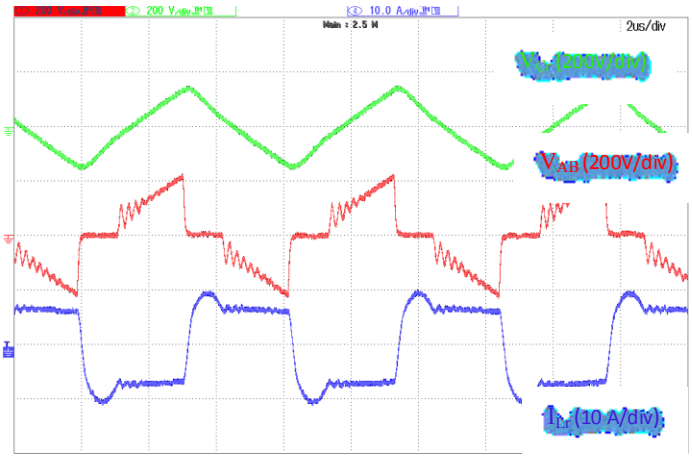
V_{in}	P_o	f_s	D
42V	500W	150 kHz	0.6
42V	100W	65 kHz	0.54
48V	500W	140 kHz	0.6
48V	100W	50 kHz	0.54

Fig. 3.12 demonstrates experimental results for input voltage V_{in} = 42V supplying only 20% of the rated power (100W). The converter operates at the switching frequency f_s = 65 kHz and duty cycle = 0.54 to regulate the load voltage and power. The steady-state operation holds good for the light-load condition as depicted in Fig. 3.12(a). Owing to the load adaptive feature, lower resonant capacitor voltage (V_{cr}) and lower voltage at the bridge output (V_{AB}) is observed. Fig. 3.12(b) depicts lower drain-to-source voltages across the switches S_1 and S_2 due to lower load current. Fig. 3.12(c) highlights the smooth commutation of the device current at turn-off eliminating any overshoot in the switch voltage. At light load, little resonant energy is required to commence body-diode conduction, resulting in the reduced overall conduction losses in the converter. Moreover, a slight variation in the duty cycle is needed to provide sufficient conduction overlap of the switches in order to preserve ZCS at light-load.

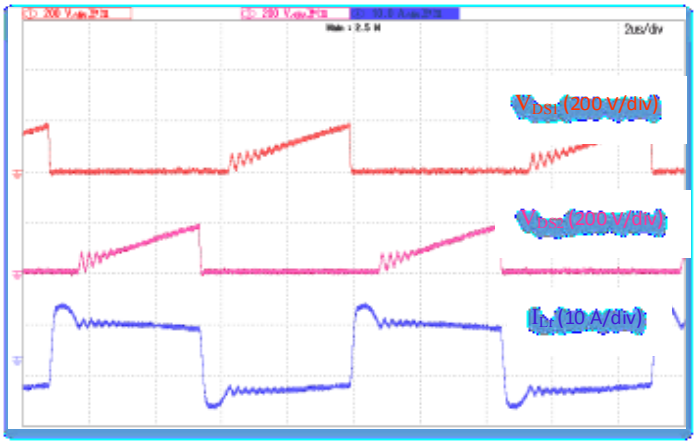
Fig. 3.13(a) and (b) show the steady-state experimental results with source voltage, V_{in} = 48V; at full-load (500W) with f_s = 140 kHz and light load (100W) with f_s = 50 kHz respectively. The sinusoidally decreasing resonant current i_{Lr} prompts the switch current to gradually reach zero before the gating pulse is removed. This confirms the ZCS turn-off of the semiconductor switches. However, it should be observed that the peak resonant current and ratio of I_{Lrp}/I_{in} are relatively higher for higher source voltages.

As a result, the experimental waveforms conclude that for the desired range of source voltage (42- 48V) and load (100%-20%), the semiconductor devices maintain ZCS turn-off with no overshoot across them as expected. It is clear that the attributes like ZCS and smooth commutation, without utilizing any external snubbing circuitry have been achieved even under partial load condition. Also, it is evident that the device commutation takes place during the switching overlap period, which changes with respect to switching frequency variation. Therefore, a slight duty cycle variation is essential to maintain desired overlap to attain ZCS with varying condition. Fig. 3.14(a) and 3.14(b) illustrate the input and output voltage and current waveforms (DC) demonstrating regulated and stiff DC output voltage of 380V with full-load and light-load current.

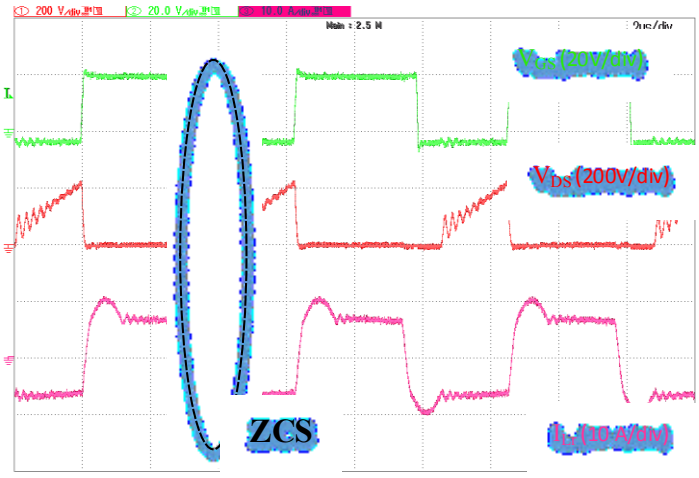
Fig. 3.15 depicts experimental current and voltage waveforms for the secondary side rectifier with V_{in}= 42V and 48V at different power levels. SiC Schottky diodes are selected to eliminate reverse recovery losses. From the demonstrated results and discussion, the proposed



(a)

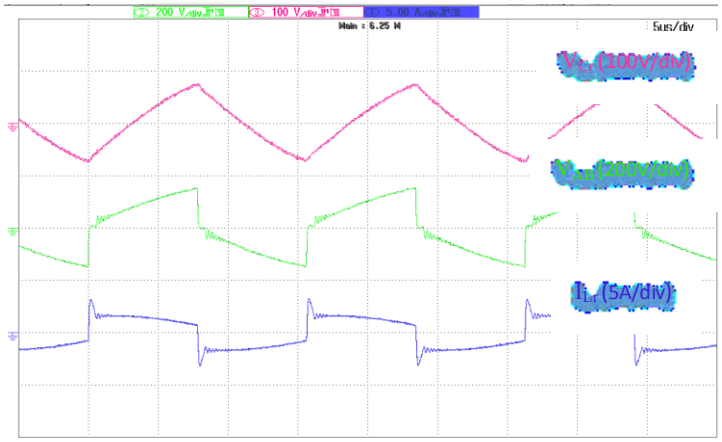


(b)

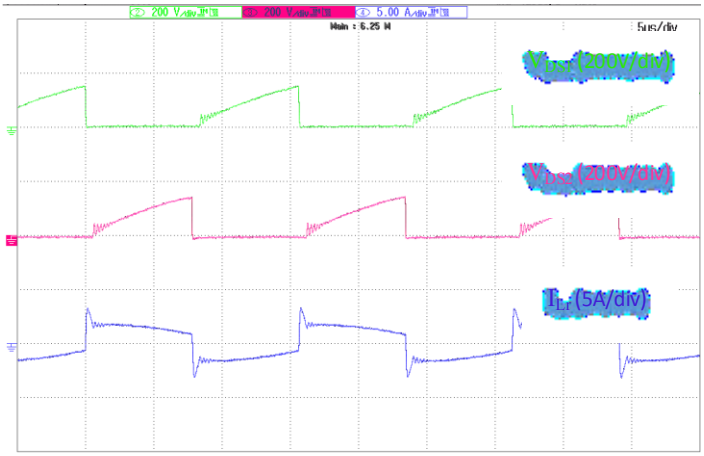


(c)

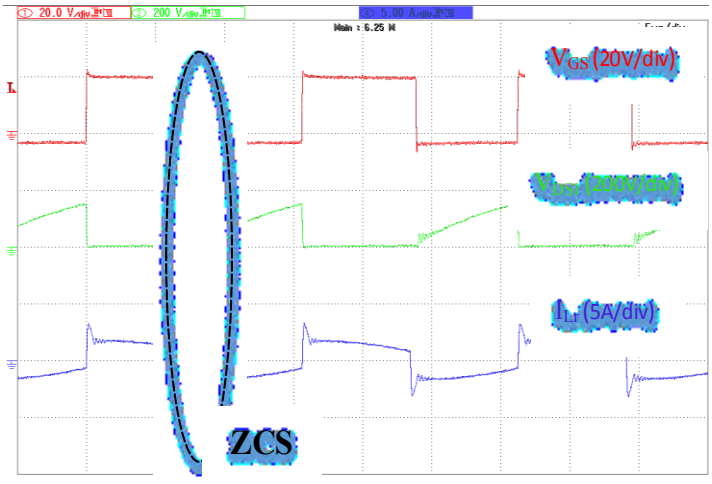
Fig. 3.11. Experimental steady-state waveform for V_{in}= 42V at full-load (500W) (a) resonant capacitor voltage V_{cr}, half-bridge output voltage V_{AB}, resonant current I_{Lr} b) drain-source voltage V_{DS1} of switch S_1, drain-source voltage V_{DS2} of switch S_2 and current flowing through series resonant tank I_{Lr} (c) gate-source voltage V_{GS}, drain-source voltage V_{DS} of switch S_1, resonant current I_{Lr}.



(a)

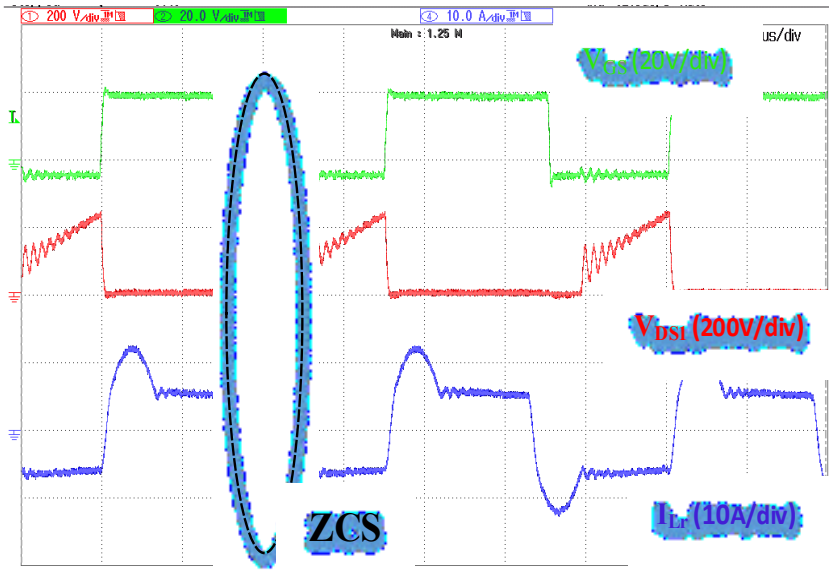


(b)

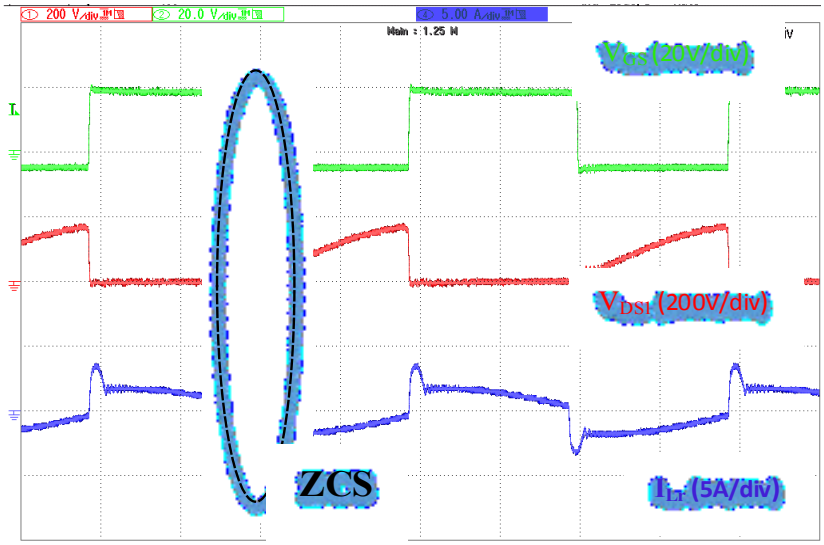


(c)

Fig. 3.12. Experimental steady-state waveforms for V_{in}= 42V at light-load (100W) (a) resonant capacitor voltage V_{cr}, half-bridge output voltage V_{AB}, current through series resonant tank I_{Lr} (b) drain-source voltage V_{DS1} of switch S_1, drain-source voltage V_{DS2} of switch S_2 and current flowing through series resonant tank I_{Lr} (c) gate-source voltage V_{GS}, drain-source voltage V_{DS} of switch S_1, resonant current I_{Lr}.

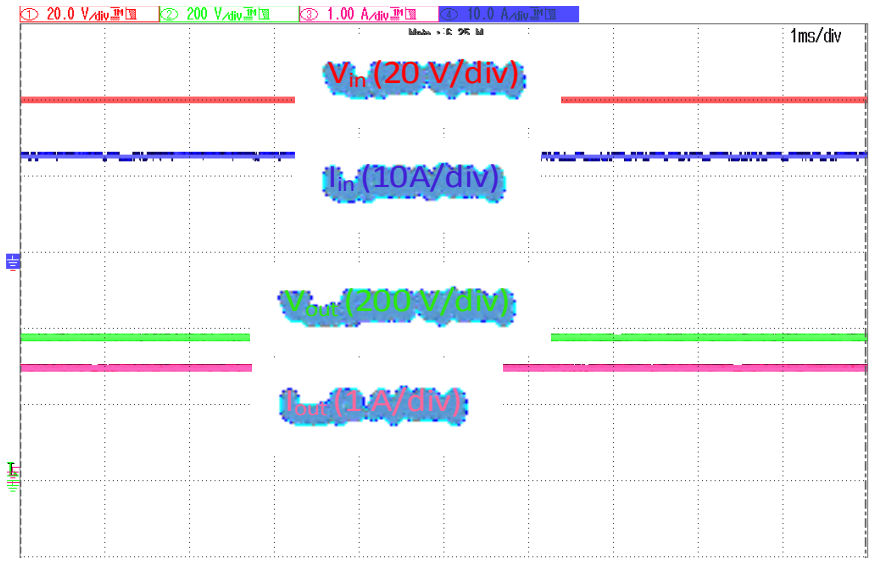


(a)

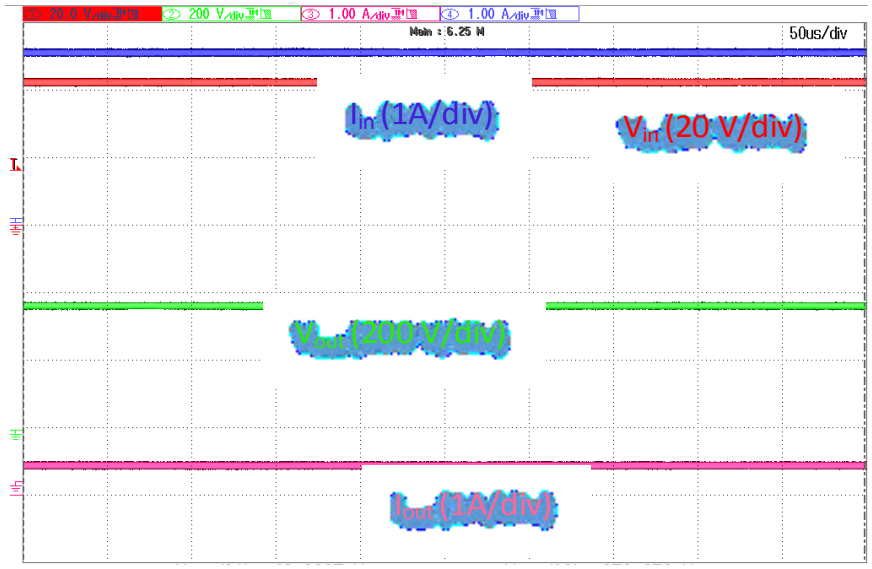


(b)

Fig. 3.13. Experimental steady-state waveform for V_{in} = 48V (a) gate-source voltage V_{GS}, drain-source voltage V_{DS1}, resonant current I_{Lr} at full-load (500W) (b) gate-source voltage V_{GS}, drain-source voltage V_{DS1}, resonant current I_{Lr} at 20% of the rated load (100W).

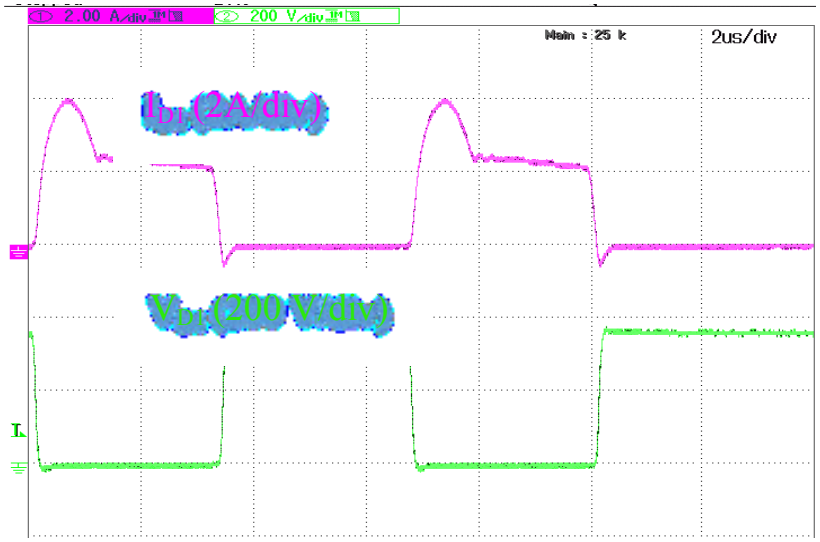


(a)

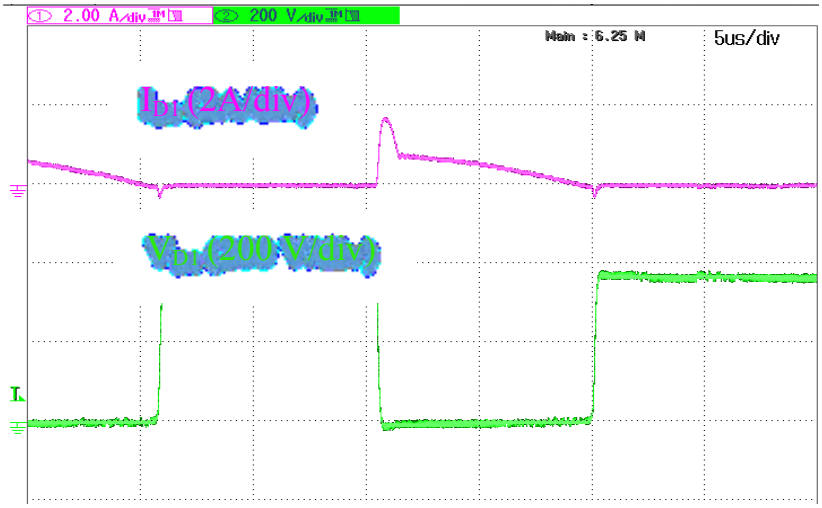


(b)

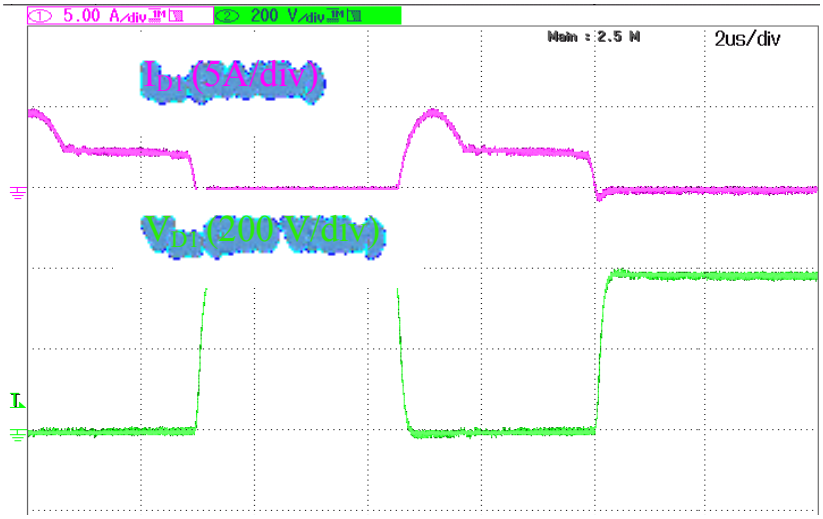
Fig. 3.14. Experimental steady-state waveform for average input voltage V_{in}, input current I_{in}, output voltage V_{out} and output current $I_{out.}$ with $V_{\text{in}} = 48\text{V}$ at (a) full-load (500W) and (b) 20% of the rated load (100W).


2.00 A/div
200 V/div
Mem : 25 k
2us/div
I_{b1}(2A/div)
V_{b1}(200 V/div)

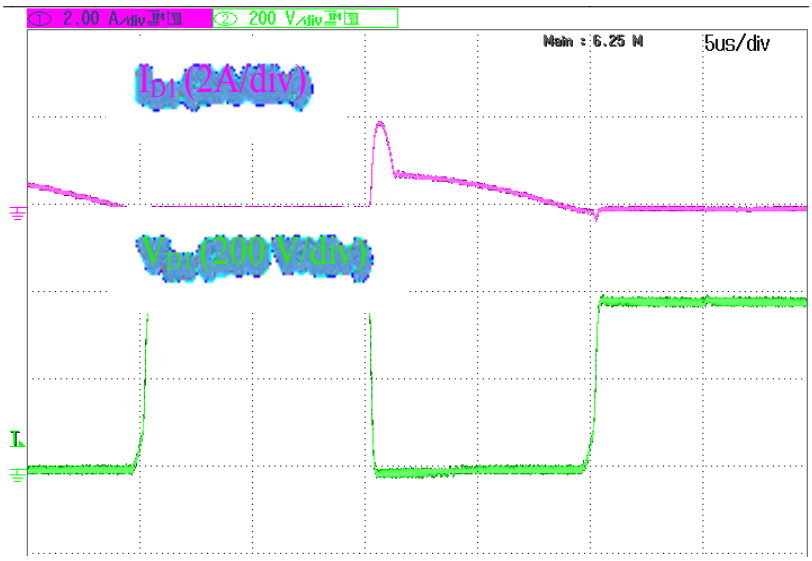
(a)


2.00 A/div
200 V/div
Mem : 6.25 M
5us/div
I_{b1}(2A/div)
V_{b1}(200 V/div)

(b)


5.00 A/div
200 V/div
Mem : 2.5 M
2us/div
I_{b1}(5A/div)
V_{b1}(200 V/div)

(c)



(d)

Fig. 3.15. Experimental results for secondary side rectifier diode current I_{D1} and voltage V_{D1} for (a) V_{in} = 42V at full-load (500W) (b) V_{in} = 42V at light-load (100W) (c) V_{in} = 48V at full-load (500W) and (d) V_{in} = 48V at light-load (100W).

converter acclaims load voltage regulation and ZCS operation throughout the variations in source voltage and load current. Moreover, the Fig. 3.16 highlights the device switching frequency trend with respect to the load variations for the input voltages of 42V and 48V. Switching frequency is varied to account for variable voltage gain at different operating loci (refer (3.30)). It is observed that the frequency variation is less sensitive to the input voltage variations at constant load. However, moderate frequency change is seen for the load variation from rated load till the half-load.

Measured experimental efficiency curve has been depicted in Fig. 3.17. Maximum efficiency of 97.2% for V_{in} = 48V at full-load operated at 140 kHz switching frequency and minimum efficiency of 94.3% for V_{in} = 42V at light-load operated at 65kHz has been recorded for the laboratory hardware prototype. Converter experiences higher losses at low input voltage owing to the higher current in the primary and higher device switching frequency.

Power loss distribution in the converter for 42V input at rated load is depicted in Fig. 3.18. It can be noticed that the conduction losses contribute to the major portion of the total losses. And therefore, MOSFETs with lower output capacitances and lower on-state resistance are

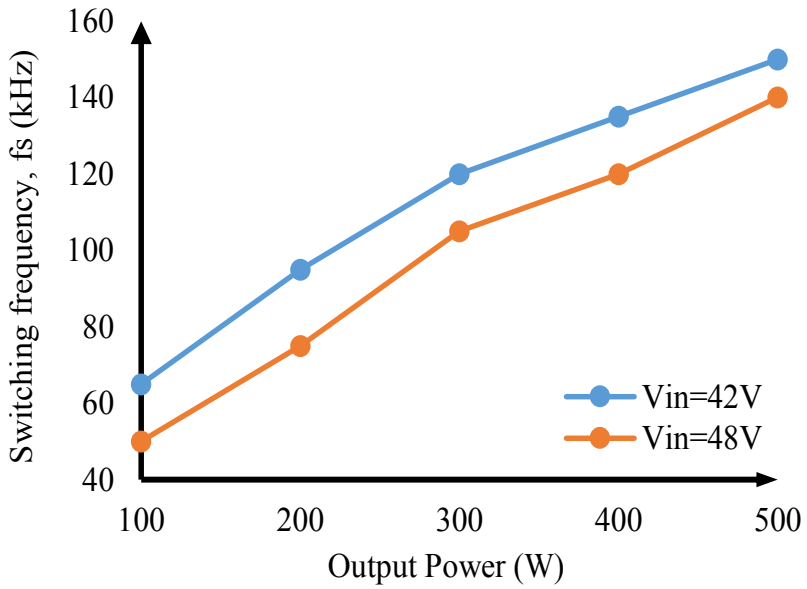


Fig. 3.16. Experimental switching frequency curve with output power variation.

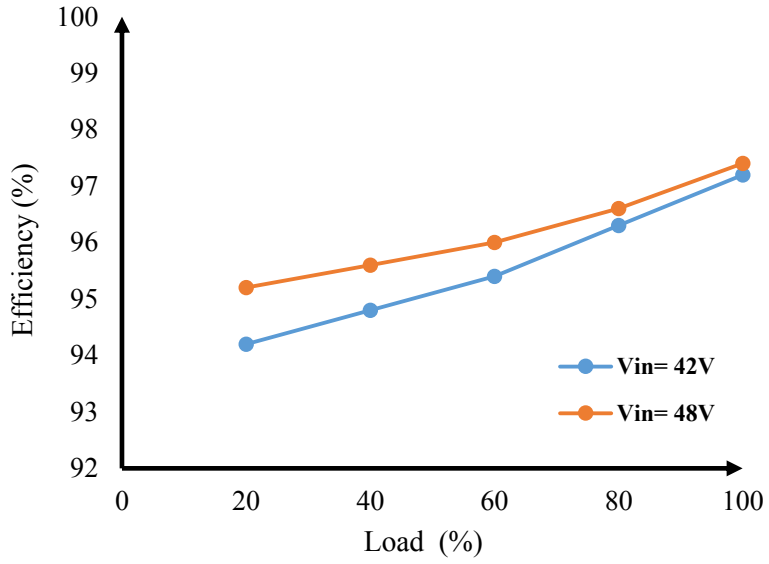


Fig. 3.17. Experimental efficiency curve with load variation of the prototype.

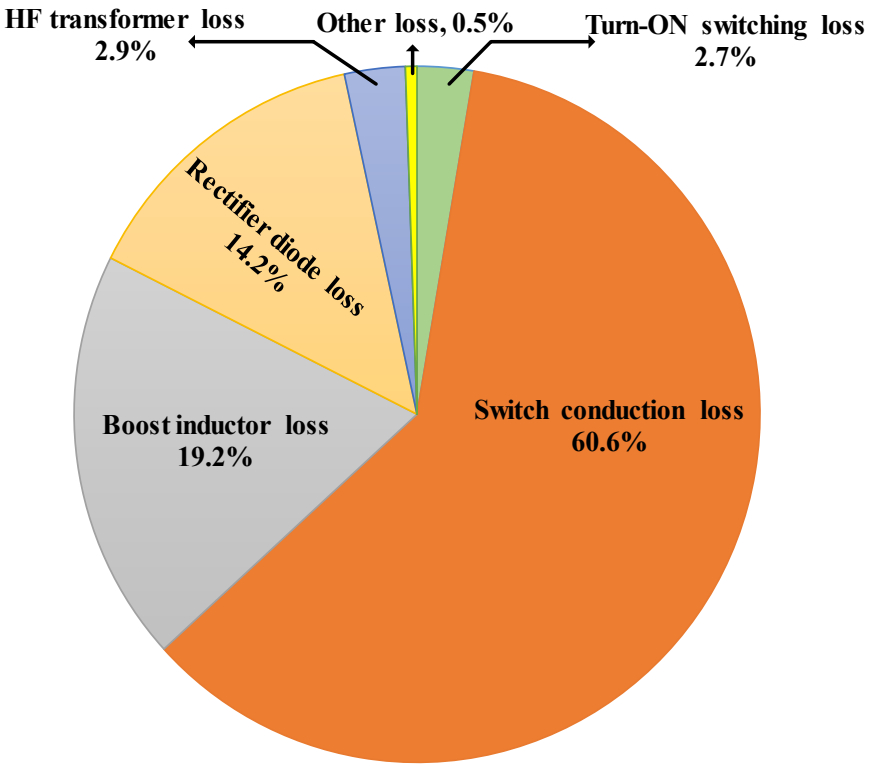


Fig. 3.18. Loss distribution in the converter for V_{in}= 42V at full load.

should be selected. Moreover, the losses incur in the hardware prototype can further be reduced by the optimal design and selection of the component with better quality printed circuit board (PCB) for the prototype.

3.6 Conclusion

A novel current-fed half-bridge topology with a series LC resonant tank to establish a short resonance pulse has been proposed and investigated in detail. The topology is derived from interleaved boost at the source and voltage doubler at the load side. The proposed circuit design eliminates the traditional requirement of a snubber circuit by clamping the device voltage at turn-off adding soft-commutation of the semiconductor devices. Short resonance pulse offers ZCS operation simultaneously restricting the peak as well as the circulating current through the components unlike conventional resonant converters. As a result, the use of overrated devices is relieved resulting in reduced cost and improved converter efficiency

in particular at light-load which is a major concern in resonant converters, particular for low voltage higher current applications.

This high gain topology offers additional merits of reduced HF transformer turns ratio, low semiconductor device count, low voltage stress across on MOSFET, and reduced gate driving requirement realizing compact, cost-effective and light-weight system. With interleaving two boost inductor at the input, source current ripple is almost negligible as they cancel each other out while supporting reduced current stress on each leg.

An experimental scale-down prototype rated at 500W has been built and tested to validate the proposed claims and steady-state operation. Maximum experimental hardware efficiency of 97.2% at full-load with 48V input, and minimum efficiency of 94.3% at 20%-load and 42V input is recorded. Moreover, ZCS operation, inherent boost ability and voltage doubler make this topology suitable for the high voltage gain applications such as solar integration to DC microgrid, modern data center, and solar/fuel-cell based battery charging.

Chapter 4

Modular Series LC Resonance-Pulse Current-Fed Full-Bridge DC-DC Converter

4.1 Introduction

In the previous Chapters, scope of the resonance-pulse concept for the soft-commutation of the semiconductor switches is studied and verified in two current-fed circuit topologies for low-to-medium power applications. For high power and high voltage specifications in various industrial applications, modular converters are widely accepted owing to their easy scalability, high-density, better fault-tolerant capability and adaptability. Multiple modules can support higher power level and enable a significant reduction in device current and voltage stress without compromising the system complexity. Moreover, a number of dc-dc converter modules can be connected in parallel/series at the input and the output to achieve the desired voltage and current levels along with desired voltage-gain with a minimum effort. However, the key challenge arises due to the higher number of power semiconductor with increased gate driver count and higher chances of false switching compromising reliability. Therefore, the module unit must possess optimized soft-switching capabilities and improved filtering leading to reliable system with remarkably low switching losses.

Further, renewable integration in DC microgrid application require variable voltage gain that's typically ranges between 8 and 12, which is plausible with the single-stage current-fed configurations. Alternative energy, sources like solar/fuel-cells generate low dc voltage output and intermittent characteristics with inherent variations in source voltage which further requires front-end dc-dc converter for voltage and regulation. Therefore, with the focus on achieving aforementioned objectives, the proposed modular converter is designed to meet the specifications of relatively high power applications compared to half-bridge and push-pull topologies including DC modern data center, auxiliary battery charging system, solar water pumping system, etc.

The distinct attributes of the proposed converter configuration presented in this Chapter are elaborated as follow:

1. Modular configuration has merits due to ease of implementation, and flexibility in the converter design and control.
2. Modular architecture supports converter individual blocks with relatively lower rating components allowing reduced cost, reduced thermal management and smaller form factor system for high-power applications.
3. With the flexibility of having submodules, modular converter offers higher redundancy with greater operation reliability.
4. Load adaptive resonant-pulse enables ZCS operation for the wide variation in source voltage (30V-58V) and load current, eliminating historic problem of high voltage spike across the semiconductor devices.
5. Lower peak currents and lower I_{Lrp}/I_{in} ratio are observed due to low resonant energy for output power below the rated power.

This Chapter elucidates the converter analysis, soft-switching operation and investigate the experimental performance of the proposed full-bridge topology (submodule). The submodule represents a two-leg full-bridge with four semiconductor switches. This Chapter is outlined as follows: Section 4.2 explains the proposed converter topology. Section 4.3 describes the steady-state time-domain analysis for different intervals with relevant mathematical equations. Section 4.4 illustrates the converter design procedure to allow appropriate selection of various component's ratings. Section 4.5 covers detailed simulation and experimental results together with loss evaluation of the proposed converter followed by concluding remarks presented in Section 4.6.

4.2 Proposed Converter topology

A modular architecture with current-fed full-bridge converter block that utilizes series resonance circuit to enable zero-current switching (ZCS) and voltage clamping of the semiconductor devices is depicted in Fig. 4.1. Series resonance circuit exploits the transformer leakage inductance and an external series capacitor. Overlap in switching states of the devices enforces a short resonance pulse, which naturally reduces the current to zero in the outgoing semiconductor devices eliminating the additional snubber requirement. The proposed converter maintains regulated output voltage for wide source voltage range by implementing

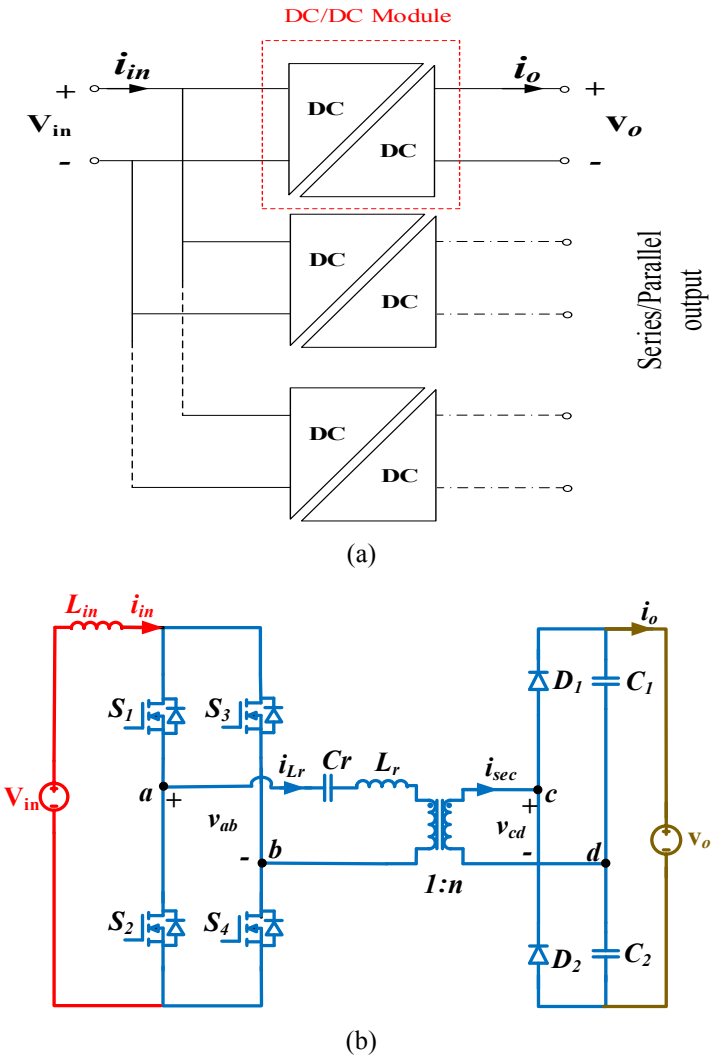


Fig. 4.1. Schematic for the (a) Modular architecture (b) Proposed current-fed full-bridge dc-dc converter module.

variable frequency control. Moderate frequency variation is observed for the entire range of operation. Switching signals for switch pair S_1, S_4 and S_2, S_3 are 180º phase shifted with identical duty ratio, $D > 0.5$ to provide necessary overlap for soft-commutation of the devices. Voltage boosting is accomplished by means of input boost inductor, high frequency transformer and capacitor doubler circuit. The current reversal in the transformer primary occurs periodically when overlap period commences resulting in negligible dc-offset preventing transformer saturation. Resonant capacitor stores load dependent energy due to its series connection which therefore allows significantly low portion of that energy to circulate

through components at light-load conditions resulting in comparatively high efficiency. Also, keeping the fixed resonant period, the energy handled by the resonant tank is purely dependent on the current passing through it.

4.3 Steady State Analysis of the Converter

This Chapter presents steady-state time domain analysis over a switching period with theoretical steady-state waveforms presented in Fig. 4.2. One complete switching period is covered in ten intervals, with first five intervals repeating in every half cycle due to symmetry in operation and therefore, only half switching period is summarized in this Section. Converter power flow circuits for the five operating intervals are illustrated in Fig. 4.3. Time domain

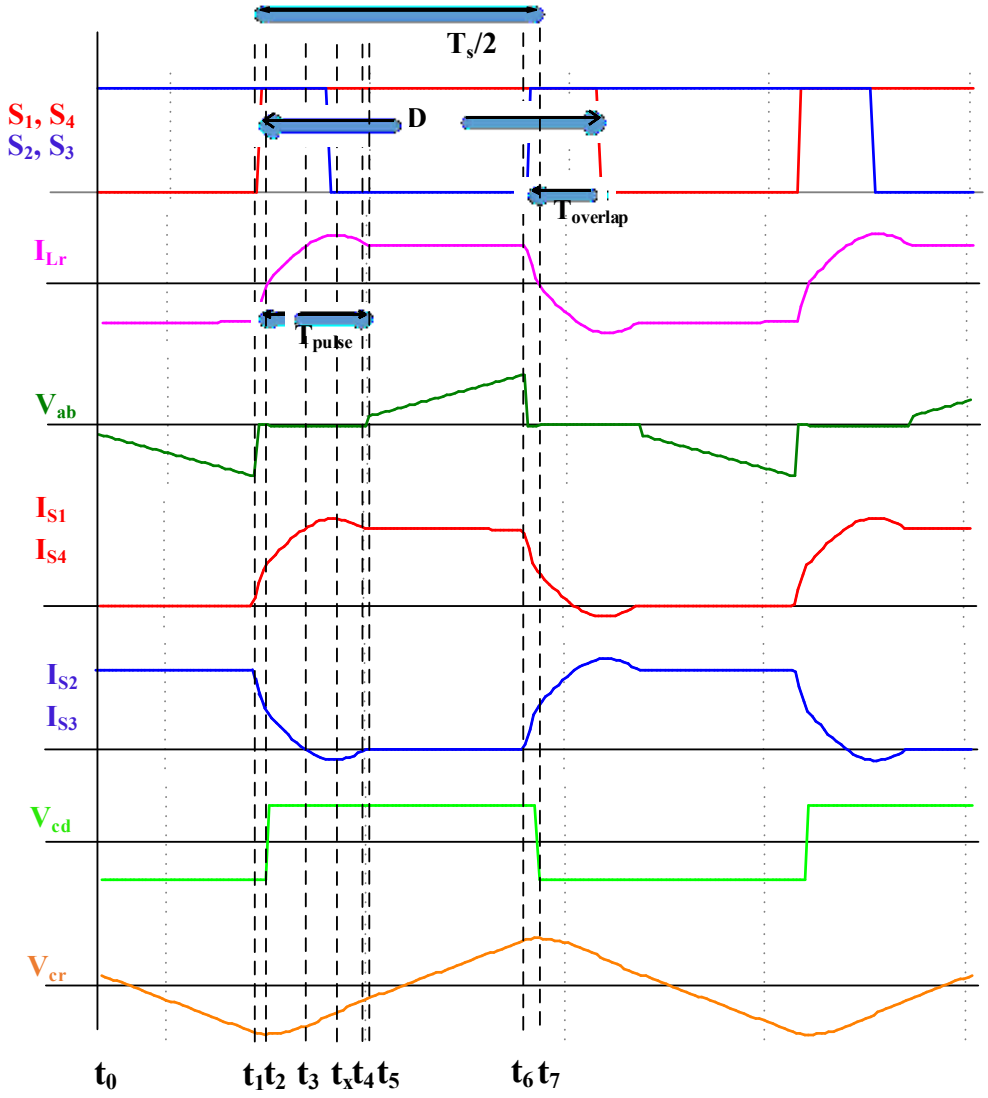
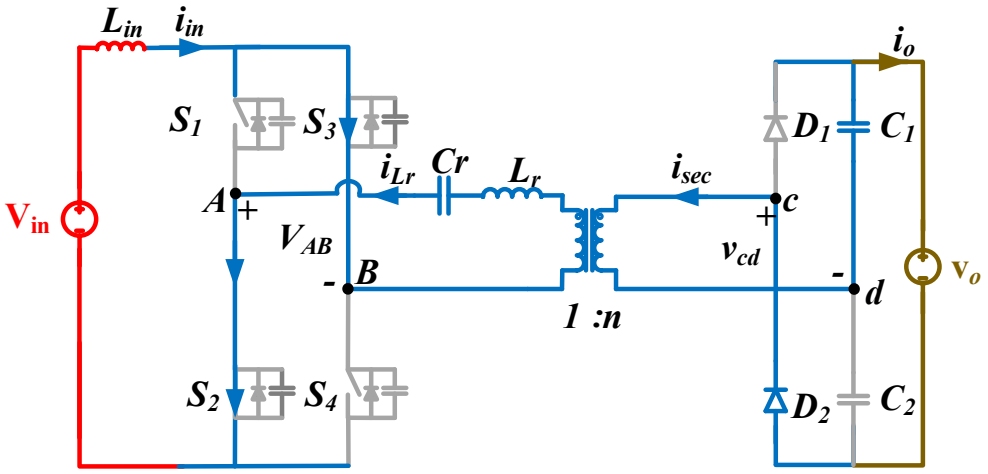
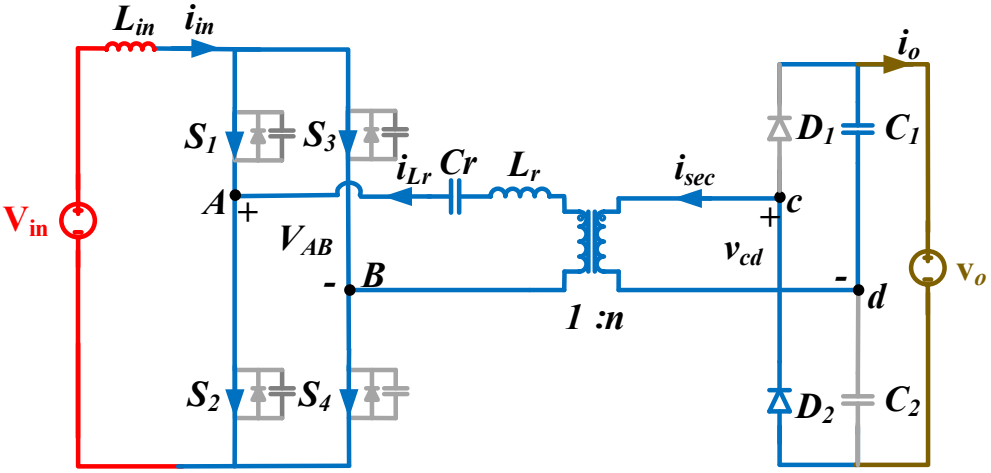


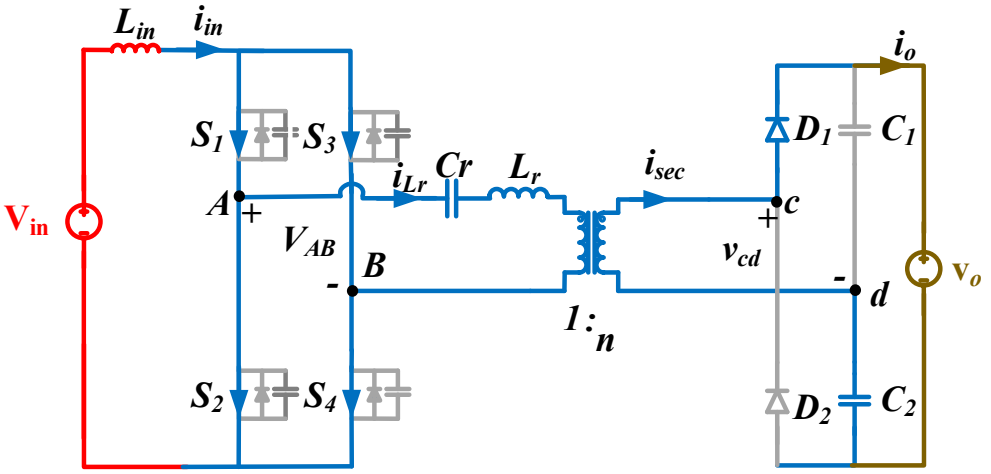
Fig. 4.2. Steady state operating waveforms of the proposed converter topology.


L_{in}
i_{in}
i_o
S_1
S_3
D_1
C_1
i_{Lr}
Cr
L_r
i_{sec}
V_{in}
A
+
V_{AB}
-
B
c
+
v_{cd}
-
d
v_o
1 :n
S_2
S_4
D_2
C_2

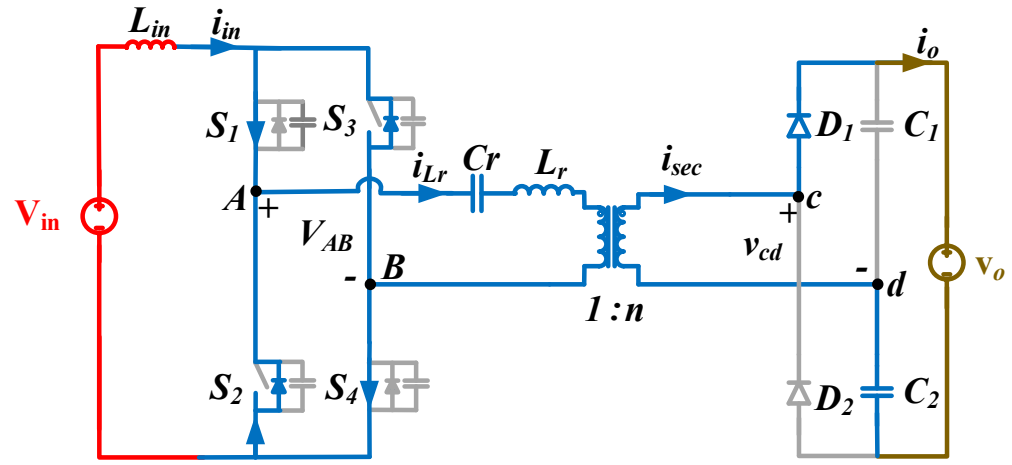
(a)


L_{in}
i_{in}
i_o
S_1
S_3
D_1
C_1
i_{Lr}
Cr
L_r
i_{sec}
V_{in}
A
+
V_{AB}
-
B
c
+
v_{cd}
-
d
v_o
1 :n
S_2
S_4
D_2
C_2

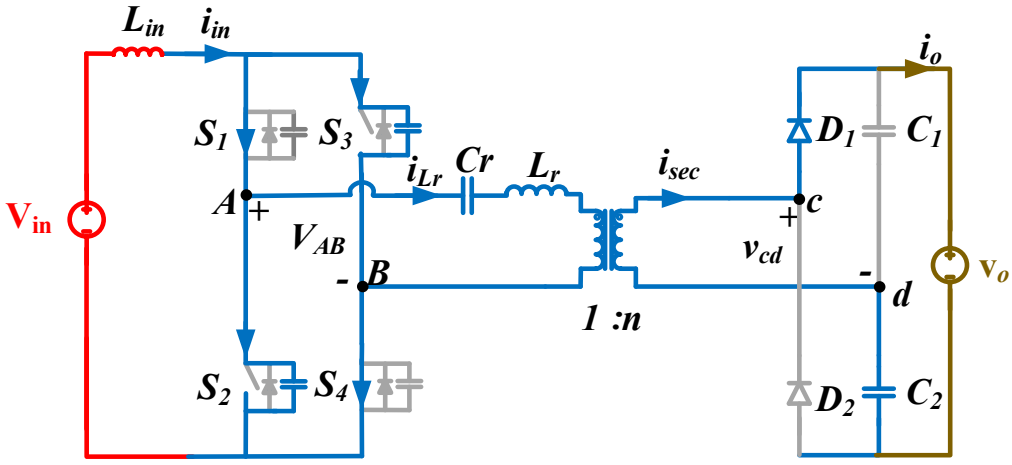
(b)


L_{in}
i_{in}
i_o
S_1
S_3
D_1
C_1
i_{Lr}
Cr
L_r
i_{sec}
V_{in}
A
+
V_{AB}
-
B
c
+
v_{cd}
-
d
v_o
1 :n
S_2
S_4
D_2
C_2

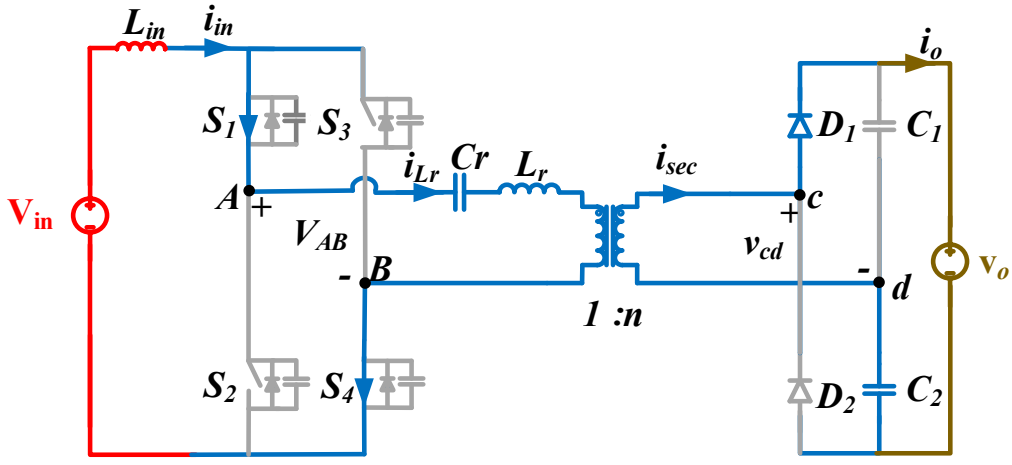
(c)



(c)



(d)



(e)

Fig. 4.3. Equivalent circuits during different operating interval.

analysis with adequate assumptions provide dynamic mathematical expressions during each interval, which then enable design of the converter with accurate estimation of component's ratings.

a) *Interval 1 (t_0-t_1): (Energy transfer interval refer Fig. 4.3(a))*

During t_0-t_1, the switches S_2 and S_3 are conducting allowing negative current through the transformer primary. Power is transferred to the load through diode D_2 as shown in Fig. 4.4(a). A negative voltage ($-\frac{V_o}{2n}$) appears across the transformer primary. In this interval, the series resonant capacitor is discharged due to negative current through the resonant tank resulting in linearly decreasing bridge output voltage.

$$i_{Lr}(t) = -I_{in} \tag{4.1}$$

$$i_{S2}(t) = i_{S3}(t) = I_{in} \; and \; i_{S1}(t) = i_{S4}(t) = 0 \tag{4.2}$$

$$V_{cr}(t) = V_{cr}(t_o) + \frac{1}{C_r}\int_{t_o}^{t} -I_{in}\, dt \tag{4.3}$$

At instant $t=t_1$, $$V_{cr}(t_1) = V_{cr1} = V_{cr}(t_o) - \frac{I_{in}}{C_r}T_{10} \tag{4.4}$$

$$V_{AB}(t_1) = (V_{cr1} - \frac{V_o}{2n}) \tag{4.5}$$

full-bridge output voltage V_{AB} is clamped to zero at the end of this interval.

b) Interval 2 (t_1-t_2): (refer Fig. 4.3(b))

At instant t_1, switch S_2 and S_3 are already conducting while S_1 and S_4 are turned-on and the device capacitance across the switches (S_1 *and* S_4) discharges rapidly in a short time. Now, current in the incoming switch pair S_1, S_4 starts increasing while the current through pair S_2, S_3 starts dropping, which can be expressed as:

$$i_{Lr}(t) = -I_{in} + \frac{1}{L_r}\left(\frac{V_o}{2n} - V_{cr}(t)\right)(t - t_1) \tag{4.6}$$

$$i_{S2}(t) = i_{S3}(t) = I_{in} - \frac{1}{2L_r}\left(\frac{V_o}{2n} - V_{cr}(t)\right)(t - t_1) \tag{4.7}$$

$$i_{S1}(t) = i_{S4}(t) = \frac{1}{2L_r}\left(\frac{V_o}{2n} - V_{cr}(t)\right)(t - t_1) \tag{4.8}$$

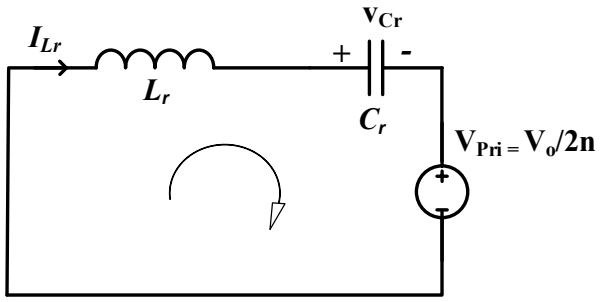


Fig. 4.4. Equivalent circuit during LC resonance period.

$$V_{cr}(t) = V_{cr}(t_1) - \frac{I_{in}}{2C_r}(t - t_1) \tag{4.9}$$

Current through the transformer primary increases linearly and reaches to zero at instant t_2.

$$i_{Lr}(t_2) = 0,\ V_{ab}(t_2) = 0 \tag{4.10}$$

$$V_{cr}(t_2) = -V_{crp} = V_{cr1} - \frac{I_{in}}{2C_r}T_{21} \tag{4.11}$$

From (4.6) and (4.10), time duration T_{21} can be computed as:

$$T_{21} = \frac{I_{in}L_r}{\frac{V_o}{2n} + V_{cr\_pk}} \tag{4.12}$$

Peak value of the series resonant capacitor charge can be estimated using

$$V_{cp} = \frac{I_{in}}{2C_r f_s}\left(1 - f_n\left(1 - \frac{1}{\pi}sin^{-1}\left(\frac{I_{in}Z_r}{V_{eq}}\right) + \frac{I_{in}Z_r}{2\pi V_{eq}}\right)\right) + \frac{V_o}{2n} \tag{4.13}$$

where $V_{eq} = \frac{V_o}{2n} + V_{cr\_pk}$

c) Interval 3 (t_2-t_3): (refer Fig.4. 3(c))

During this interval, all four switches are conducting. At instant t_2, the transformer current changes its polarity and the transformer primary voltage is clamped to $\frac{V_o}{2n}$ causing diode D_1 to conduct. Resonance period begins at the start of this instant interval, between L_r and C_r, which then results in sinusoidally increasing current through switch pair S_1, S_4 while current through switch pair S_2, S_3 decreases in the same manner. Resonant interval is analyzed using equivalent circuit depicted in Fig. 4.4. Therefore, the resonant frequency f_r and characteristics impedance Z_r are given as below:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}, \qquad Z_r = \sqrt{\frac{L_r}{C_r}} \tag{4.14}$$

$$i_{Lr}(t) = \frac{1}{Z_r}\left(\frac{V_o}{2n} - V_{cr}(t_2)\right) sin(\omega_r(t - t_2)) \tag{4.15}$$

$$i_{s1}(t) = i_{S4}(t) = \frac{I_{in}}{2} + \frac{1}{2Z_r}\left(\frac{V_o}{2n} - V_{cr}(t_2)\right) sin\omega_r(t - t_2) \tag{4.16}$$

$$i_{S2}(t) = i_{S3}(t) = \frac{I_{in}}{2} - \frac{1}{2Z_r}\left(\frac{V_o}{2n} - V_{cr}(t_2)\right) sin\omega_r(t - t_2) \tag{4.17}$$

$$V_{cr}(t) = \frac{1}{C_r}\int_{t_2}^{t} i_{Lr}(t)\, dt = \left(\frac{V_o}{2n} - V_{cr}(t_2)\right) * \cos\big(\omega_r(t - t_2)\big) \tag{4.18}$$

At the end of this interval, resonant current i_{Lr} reaches I_{in} while the current through switch S_2, S_3 reaches zero.

$$i_{Lr}(t_3) = I_{in} \tag{4.19}$$

$$i_{S2}(t_3) = i_{S3}(t_3) = 0 \tag{4.20}$$

From (4.15) and (4.19), time duration of this interval can be computed as:

$$T_{32} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{I_{in}Z_r}{\frac{V_o}{2n} + V_{crp}}\right) \tag{4.21}$$

d) Interval 4 (t_3-t_4): (refer Fig. 4.3(d))

During this interval, the resonance initiates between L_r and C_r with all the switches conducting. A positive voltage across the resonant inductor causes the transformer primary current to overpass I_{in}. This additional current allows the body diode conduction leading to ZCS turn-off of devices S_2 and S_3. During this interval, the resonant current reaches its peak value at instant t_x which can be estimated as

$$I_{LrP} = i_{Lr}(t_x) = \frac{1}{Z_r}\left(\frac{V_o}{2n} + V_{crp}\right) \tag{4.22}$$

for ZCS operation, $I_{Lr\_peak} > I_{in}$ which implies

$$Z_r < \frac{\left(\frac{V_o}{2n} + V_{cr_p}\right)}{I_{in}} \tag{4.23}$$

Resonance period terminates at instant t_4 and current I_{Lr} again reduces to I_{in}. At instant t_4, switch S_1 and S_4 take over and the power is transferred to the load through diode D_1.

$$i_{Lr}(t_4) = I_{in} \tag{4.24}$$

Time duration of this interval can be estimated using the following expression:

$$T_{42} = \frac{1}{\omega_r}\left(\pi - \sin^{-1}\left(\frac{I_{in}Z_r}{\frac{V_o}{2n}++V_{crp}}\right)\right) \tag{4.25}$$

$$T_{43} = T_{42} - T_{23} \tag{4.26}$$

e) Interval 5 (t_4-t_5): (refer Fig.4.3(e))

At t_4, the current i_{Lr} reaches I_{in} and the switches S_2 and S_3 have been turned off with ZCS, the device capacitance across gets charged to build voltage across the two switches.

$$i_{Lr}(t_4) = I_{\text{in}}\,, i_{\text{S1}}(t_4) = i_{S4}(t_4) = I_{\text{in}} \tag{4.27}$$

$$i_{\text{S2}}(t_4) = i_{\text{S3}}(t_4) = 0 \tag{4.28}$$

Consequently, time instant t_5 onwards, the operating intervals repeat in the same sequence for the other half-cycle when switch pair S_1 S_4 conduct and positive current flows through the transformer transferring the power to the load through diode D_1 as shown in Fig. 3(f). Therefore, the duration of the half-switching cycle is:

$$T_{50} = T_{61} = \frac{T_s}{2} \tag{4.29}$$

4.4 Converter Design

The following specifications are decided to interface a solar panel or fuel cell stack to DC bus: input voltage ranging from 30–58V; stiff dc bus voltage 380V, and rated power 500W (full-load). The systematic design procedure for the proposed converter is discussed next. This Section elaborates on the design guidelines to determine the converter parameters along with analytical expressions to determine component's rating. The design must ensure regulated

output voltage and ZCS operation of the semiconductor switches under given varying operating conditions.

4.4.1 DC voltage gain

Gain characteristics curve in Fig. 4.5 depicts the converter dc voltage gain variation with normalized frequency (f_n), for the different values of HF transformer turns ratio (n). This curve indicates multiple combination of the switching frequency (f_{sw}) and turns ratio to provide uniform output voltage for the given input voltage range at rated load. A mathematical relation between input-to-output voltage depend on various converter parameters can be obtained through the power balance theory and average output current expression. For simplified computations, all parameters are referred to the primary.

$$I_{in} * V_{in} = \eta \frac{{V_o}^2}{R_{FL}} \tag{4.30}$$

$$\left|I_{o,avg}\right| = \frac{V_o}{R_{FL}} = \frac{I_{Lr,avg}}{n} = \frac{1}{n} . \frac{2}{T_s} \int_0^{T_s/2} i_{Lr}(t)\ dt \tag{4.31}$$

$$= \frac{2f_{sw}}{n} \left[\int_{t_2}^{t_4} i_{Lr}(t)\ dt + \int_{t_4}^{t_6} I_{in}\ dt + \int_{t_6}^{t_7} i_{Lr}(t)\ dt \right] \tag{4.32}$$

where P_o, V_o, and R_{FL} represent output power, output voltage and equivalent full-load resistance respectively.

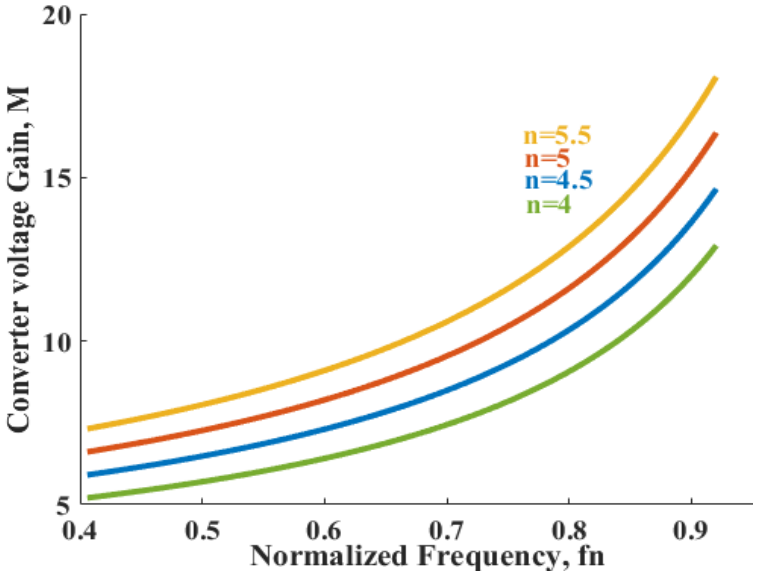


Fig. 4.5 Converter voltage gain characteristics curve.

With the knowledge of time intervals derived in section 4.3 and using (4.30) and (4.32), voltage gain expression in terms of control variables like f_n, V_o, V_{in} and load R_{fl} can be represented as:

$$\frac{V_o}{V_{in}} = M = \frac{n\left(1 - \frac{f_n r_n X}{2\pi}\left(1 - \sqrt{1-k^2}\right)\right)}{\left(1 - f_n\left(1 - \frac{1}{\pi} sin^{-1}k + \frac{k}{2\pi}\right)\right)} \tag{4.33}$$

where, n: Turn ratio of HF transformer; $k = \frac{2M}{nr_n X}$

f_n: Normalized frequency, $= \frac{f_{sw}}{f_r}$

r_n: Normalized load resistance, $= \frac{R_{FL}}{n^2 Z_r}$

X: Constant defined as, $= \left(1 + \frac{2nV_{crp}}{V_o}\right)$

Consequently, for a selected value of turns ratio, the output voltage can be maintained constant by varying converter switching frequency for load and source voltage variation.

4.4.2 Selection of semiconductor devices

I. Voltage stress:

The maximum voltage across the semiconductor device is estimated as:

$$V_{sw1-4,rated} = V_{crp} + \frac{V_o}{2n} \tag{4.34}$$

$$V_{D1} = V_{D2} = V_o \tag{4.35}$$

As evident from (4.34), peak voltage across the primary side semiconductor devices depends on the resonant capacitor charge and turns ratio of the HF transformer. Also, the switch voltage rating is critical in optimizing switch conduction losses owing to its dependency on $R_{ds,on,}$ which is intrinsic to the device rating. To further enhance the converter efficiency, rectifier diodes with low V_{FD} and negligible Q_{RR} are selected minimizing the diode conduction losses.

II. Current stress:

Rms current through for semiconductor devices and other components are given by the following expressions:

$$I_{sw\_rms} = \left[I_{in}^2 \left(\frac{1}{2} - f_n \left(\frac{1}{4} - \left(\frac{1}{4k} \right)^2 + \frac{k}{6\pi} - \left(\frac{\sqrt{1-k^2}}{8\pi k} \right) \right) + \frac{1}{\pi} \left(\left(\frac{1}{4k} \right)^2 - \frac{1}{2} \right) sin^{-1} k \right) \right]^{\frac{1}{2}} \quad (4.36)$$

$$I_{Lr\_rms} = \left[I_{in}^2 \left(1 - f_n \left(1 - \frac{1}{2} \left(\frac{1}{k} \right)^2 + \frac{2k}{3\pi} + \left(\frac{\sqrt{1-k^2}}{2\pi k} \right) \right) + \frac{1}{2\pi} \left(\left(\frac{1}{k} \right)^2 - 2 \right) sin^{-1} k \right) \right]^{\frac{1}{2}} \quad (4.37)$$

$$I_{D1-2,avg} = I_o \quad (4.38)$$

Current expressions allow theoretical calculation of their rms values and therefore, accurate estimation of the conduction losses given specifications. Rms current values also help in deciding current rating of the semiconductor devices and other components. The approximate switch rms currents are computed as 13.7A and 9.6 A for Vin = 30 V and 58 V, respectively at full load conditions.

4.4.3 Selection of HF Transformer Turns Ratio

Selection of HF transformer turns ratio is such that it must deliver the desired voltage gain for selected device switching frequency range while limiting the conduction losses of the devices. The turns ratio has significant impact on the voltage stress and current ratings and hence, power dissipation on the semiconductor devices as evident from (4.34), (4.36) and (4.37). Selecting a lower value of turns ratio can surge the maximum voltage across the primary side switches compelling the use of high voltage rating switches with inherently high on-state resistance, further escalating the conduction losses. Whereas, a large turns ratio yields higher switch RMS current as evident from (4.36) further contributes to the conduction loss in the devices as well as copper loss associated with the HF transformer. Therefore, selection of turns ratio is critical in appropriate switch selection with minimized conduction losses. For this design example, turns ratio of 5.2 is selected to meet the desired voltage gain and switching frequency range.

4.4.4 Soft switching boundary

Series resonant energy is utilized to achieve ZCS of the semiconductor devices under all operating conditions. The necessary condition is to ensure the switch current to reach zero before its gating signal is removed. It can be perceived from Fig. 4.2 that the peak of the

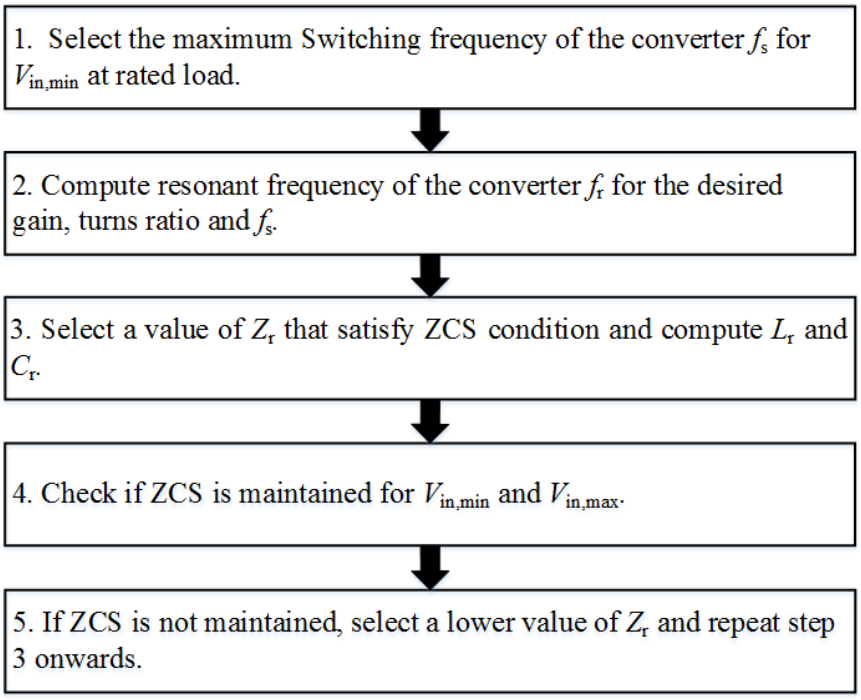


Fig. 4.6. Flowchart depicting the resonant tank design.

resonant current I_{LrP} must be greater than the input current I_{in} to allow anti-parallel body diode conduction before the gating pulse is forced off. This condition results in the following expression.

$$Z_r < \frac{2 * \left(\frac{V_o}{2n} + V_{cr_p}\right) * R_{FL} * V_{in}}{{V_o}^2} \tag{4.39}$$

Therefore, the value of Z_r should be computed, considering the peak resonant voltage and $V_{in,min}$. Moreover, the tank impedance decides the amount of circulating energy available for the effective ZCS of the switches. A higher value of Z_r causes lower leakage current but it may not sustain ZCS for wider operating range. Therefore, the value of Z_r should be carefully determined without intensifying peak and rms current. For this design example $Z_r = 6.45$ is selected and a trade-off occurs between the ZCS operating range, and the conduction losses.

4.4.5 Design of the resonant tank parameters

Adequate design of the resonant tank is critical in achieving full-range ZCS with reduced circulating currents and reduced conductions losses. After selecting the values of the maximum switching frequency and the turns ratio, the resonant frequency can be estimated

using gain expression. Therefore, utilizing characteristic impedance value and estimated resonant frequency, the resonant tank parameters are computed. The flow chart is shown in Fig. 4.6 and the values obtained for L_r and C_r to be 5.5μH and 132nF, respectively.

4.4.6 Duty Cycle Boundary

In the proposed converter, the resonant period defines the soft-switching boundary and therefore, the appropriate duty cycle can be determined to ensure ZCS from full-load down to light-load. This condition necessitates the turn-off of the semiconductor devices before the resonant pulse dies out. This implies:

$$T_{32} < T_{overlap} < T_{42} \tag{4.40}$$

where, $T_{overlap} = \frac{2D-1}{2} T_s$

Operating boundary for the duty cycle is given by the inequality.

$$D_{min} < D < D_{max} \tag{4.41}$$

where $D_{\min}$ and $D_{\max}$ can be calculated from Fig. 4.2 and time intervals given in section 4.3.

$$D_{min} = 0.5 + \frac{I_{in} L_r f_{sw}}{\frac{V_o}{2n} + V_{cr\_pk}} + \frac{f_{sw}}{2\pi f_r} \sin^{-1}\left(\frac{I_{in} Z_r}{\frac{V_o}{2n} + V_{crp}}\right) \tag{4.42}$$

$$D_{max} = 0.5 + \frac{I_{in} L_r f_{sw}}{\frac{V_o}{2n} + V_{cr\_pk}} + \frac{f_{sw}}{2\pi f_r} \sin^{-1}\left(\frac{I_{in} Z_r}{\frac{V_o}{2n} + V_{crp}}\right) + \frac{f_{sw}}{2 f_r} \tag{4.43}$$

Therefore, a duty ratio of 0.73 is selected to ensure ZCS for the entire range of source voltage at rated load condition. However, with the low switching frequency operation at light load condition, maintaining the resonant period constant (i.e. constant $T_{overlap}$) necessitates slight change in duty ratio.

4.4.7 Influence on Converter Efficiency

The theoretical loss estimation for the proposed converter is conducted to correctly estimate its efficiency with the proposed design. Referring to the loss formulas given in Appendix A.1, dependency of the various loss components on the converter efficiency can be evaluated. Starting with the conduction losses, which predominantly occur in semiconductor switching devices, input inductor, resonant inductor, rectifier diodes, and HF transformer, significantly affect the converter efficiency. MOSFET conduction loss primarily depends on

the MOSFET rms current, device intrinsic on-state resistance ($R_{ds,on}$) and output capacitance (C_{oss}) which are largely influenced by the device voltage rating. In addition, diode conduction loss depends on its forward blocking voltage and average current. The remaining portion of the conduction loss encompass HF transformer loss and inductor loss which largely depends on the input current, the resonant current and DC resistance of the transformer winding and inductors. On the other hand, MOSFET turn-on switching losses are influenced by device switching frequency and maximum voltage appearing across the drain-to-source terminals whereas diode switching losses are neglected due to negligible reverse recovery. The overall converter efficiency (η_{conv}) is given as.

$$\eta_{conv} = \frac{P_{rated} - P_{Core} - P_{condcution} - P_{switching}}{P_{rated}} \tag{4.44}$$

where,

$$P_{Conduction} = P_{MOSFET,Conduction} + P_{Diode,Conduction} + P_{transformer,copper} + P_{boost\ inductor} + P_{resonant\ inductor}$$

$$P_{switching} = P_{MOSFET,switching} + P_{Diode,switching}$$

$$P_{Core} = \text{transformer core loss}$$

Further, the efficiency can be related to various converter parameters:

$$\eta_{conv} = f\left(f_{sw}, n, V_{Sw,rated}, R_{ds,on}\right) \tag{4.45}$$

Considering efficiency as a paramount factor, parameters such as $f_{sw}, n,\ R_{ds,on}$ etc. must be optimized to achieve the minimum possible losses. This in turn necessitates appropriate selection of HF transformer turns ratio, switching frequency, semiconductor device ratings along with optimized design of the magnetic components to limit the losses associated with them. For this design example, SiC MOSFETs are adopted with remarkably low output capacitance (C_{oss}) and $R_{ds,on}$ for a comparable rated voltage limiting their overall losses. In addition, ultra-high speed SiC Schottky diodes are preferred for the diode rectifier to assist in smooth turn-off with diminished reverse recovery loss. Likewise, recommended design for the HF transformer comprise EE ferrite core and litz wire with inherently low dc resistance. Besides, in-house gate drive circuits with different turn-on and turn-off speed are recommended for improved performance. Further, with the knowledge of the analytical

expressions obtained in Section 4.4.2 together with the loss formulas, and the datasheet specifications of the hardware components, theoretical efficiency can be determined

4.5 Results and Discussion

This Section validates the proposed theory through detailed results obtained from the simulation performed in PSIM 11.0. Later, competency of the developed laboratory prototype is assessed through experimental testing with detailed discussion on experimental results and performance.

4.5.1 Simulation Results

Proposed converter module is simulated in PSIM 11.0 platform to validate the theoretical analysis and to ensure the satisfactory operation of the proposed converter with PWM signal generation from open-loop control. Converter parameters obtained from the Section 4.4 are mentioned in Table 4.1. This section illustrates the steady-state simulation results with the input voltage, V_{in} = 42V for full load (500W) and 20% load (100W) condition. Converter is operated with a switching frequency range of 150 kHz down to 75 kHz.

Fig. 4.7 depicts the simulated steady-state waveforms for the full-bridge output voltage across terminals A and B (V_{AB}), resonance capacitor voltage (V_{Cr}) and transformer primary voltage (V_{pri}) at full-load. The bridge voltage V_{AB} remains zero during the switching overlap time.

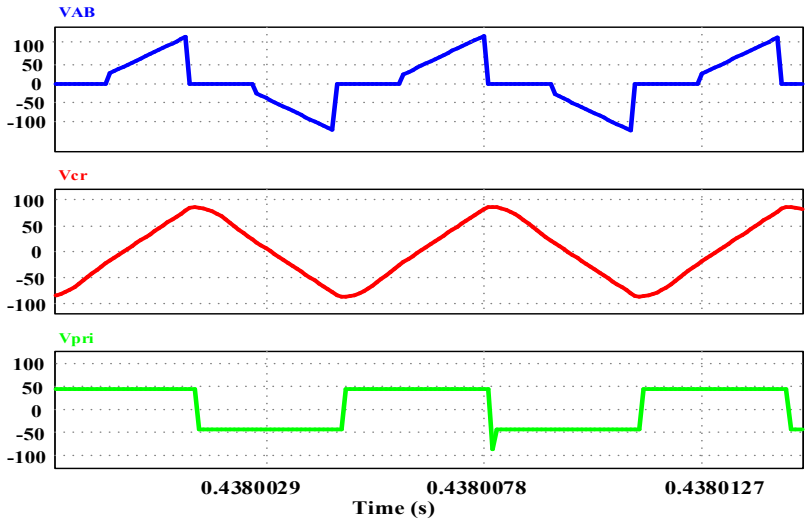
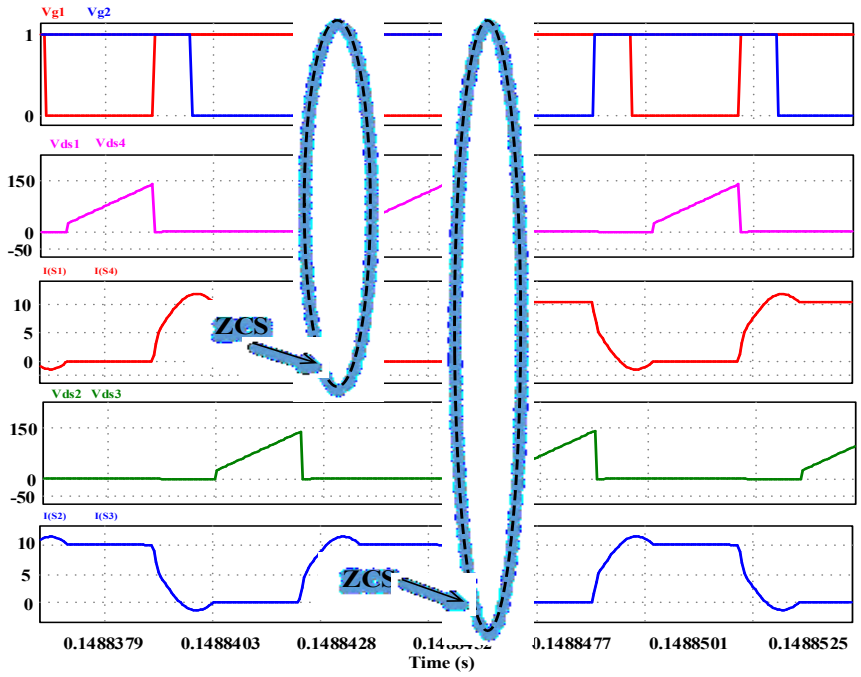
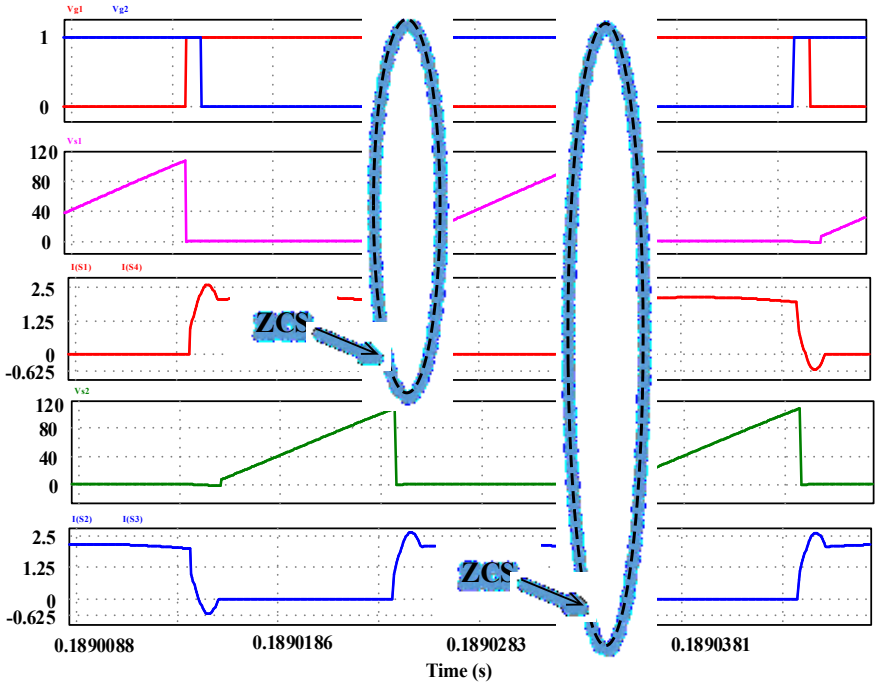


Fig. 4.7. Steady state waveforms for primary side bridge voltage, V_{AB} resonance capacitor voltage, V_{Cr} and transformer primary voltage at full-load.

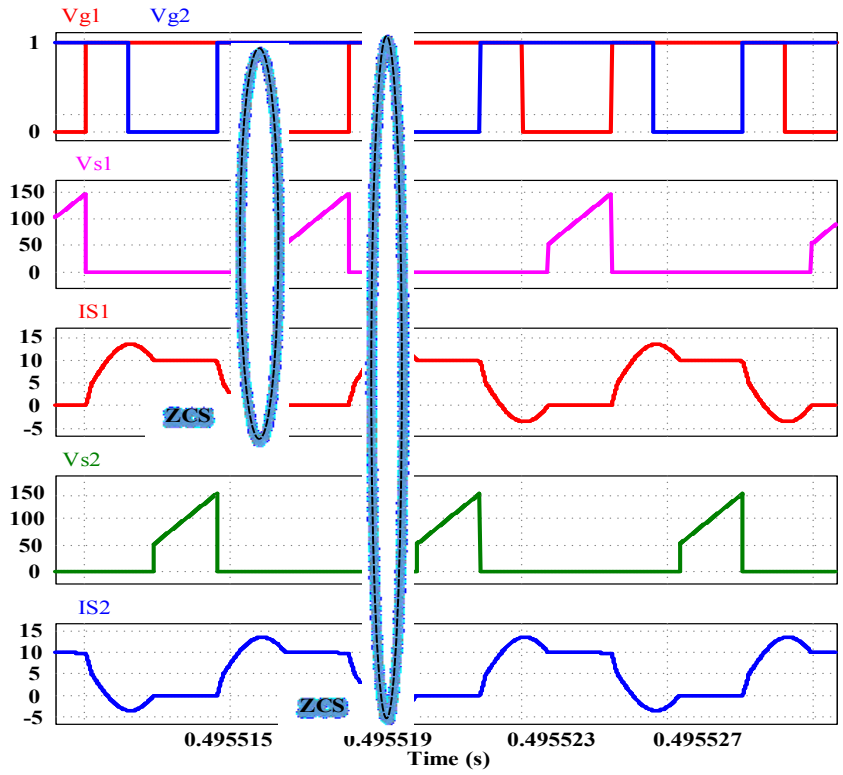


(a)

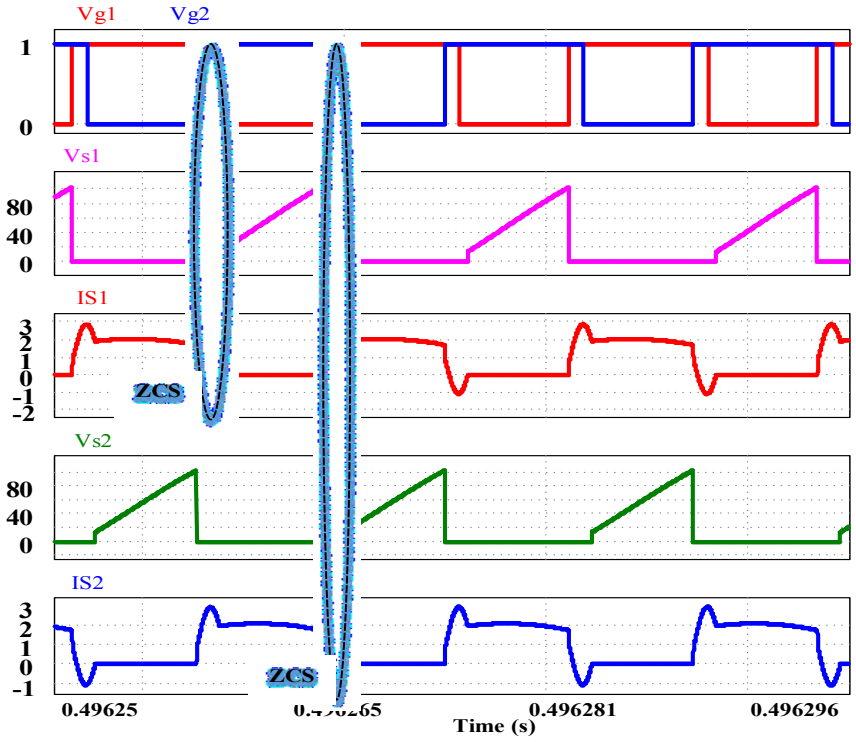


(b)

Fig. 4.8. Simulated waveforms depicting ZCS for primary side devices for V_{in} = 42V at (a) at full-load (500W) (b) light-load (100W) operation.

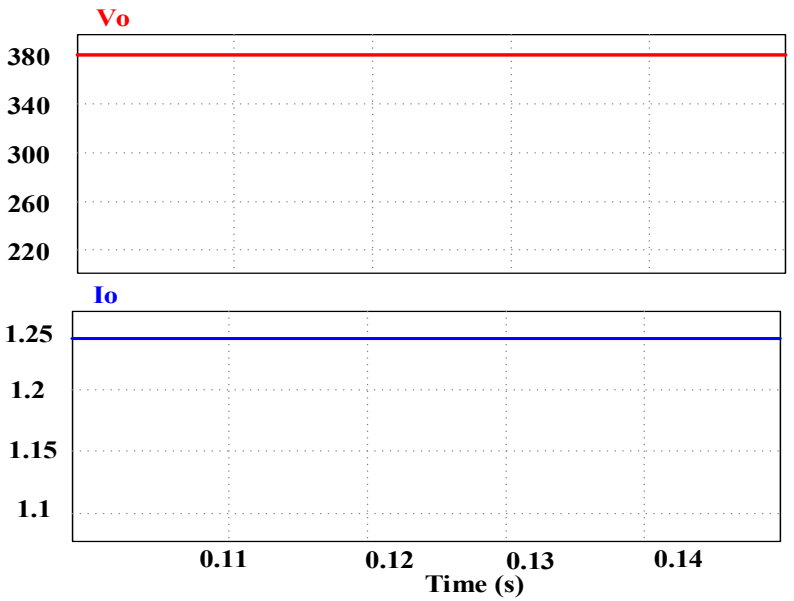


(a)

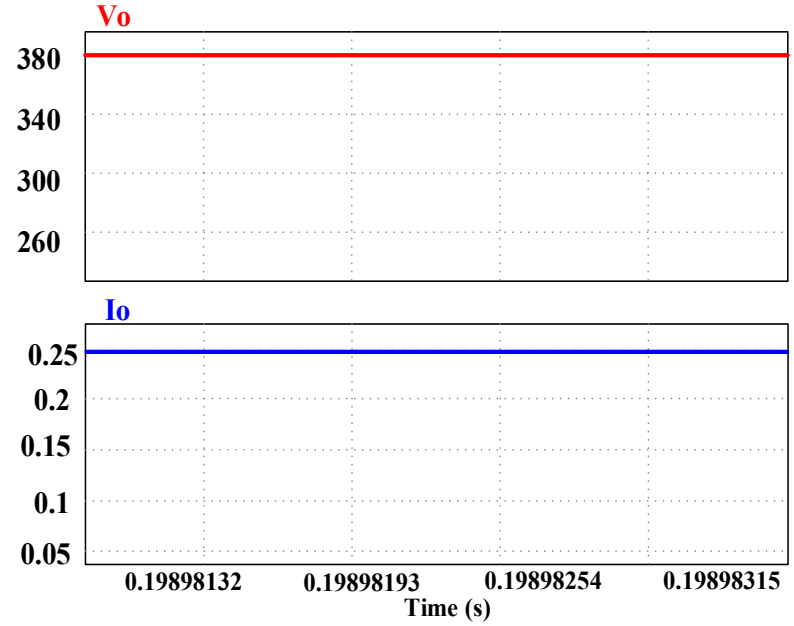


(b)

Fig. 4.9. Simulated waveforms depicting ZCS for primary side devices for V_{in} = 48V at (a) at full-load (500W) (b) light-load (100W) operation.



(a)



(b)

Fig. 4.10. Simulated waveforms for output voltage, V_o and output current I_o at (a) full-load (500W) (b) light-load (100W) operation.

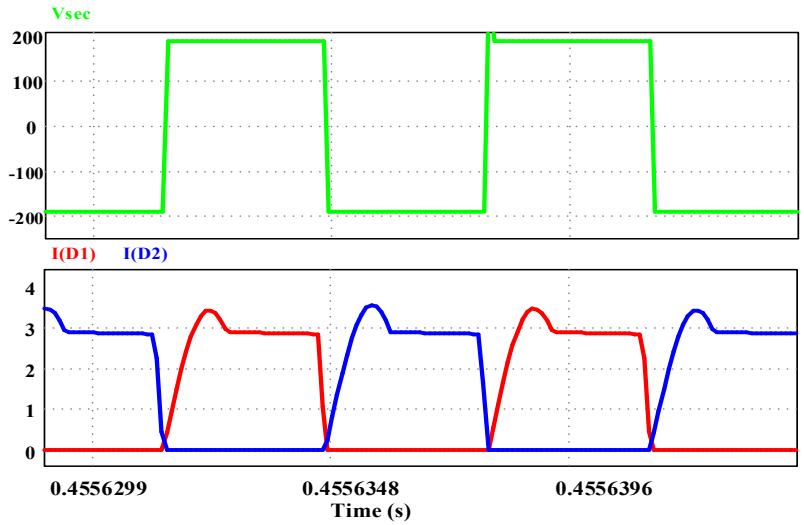


Fig. 4.11. Steady state waveforms for transformer secondary-side voltage, V_{sec} and diode current at full-load.

Linearly increasing capacitor voltage is observed owing to the constant current during that interval charging the resonant capacitor. Sinusoidally varying short resonance-pulse in switch current waveform during switching overlap period indicates an additional energy for the internal body diode conduction to facilitate soft-switching of the MOSFETs as depicted in Fig. 4.8. This causes natural reduction in the switch current, and therefore the gating pulse is removed once it goes below zero level. Simulation results in Fig. 4.8(a) and Fig. 4.8(b) illustrate soft-commutation of the primary side devices at V_{in}= 42V for the full-load and the light-load operation respectively. The highlighted switch turn-off instant also indicates no overshoot in the switch voltage. It can also be observed that the switch voltage is maintained zero and the switch current goes negative at turn-off, which confirms the body diode conduction. Converter is operated at 42V input voltage with switching frequency, f_{sw} =150 kHz for full-load (500W), whereas f_{sw} = 75 kHz at light-load (100W). Likewise, Fig. 4.9 demonstrates successful ZCS operation and voltage clamping of the switching devices at 48V input for the full-load and the light-load current. It should be observed that the switch current peak and the switch voltages are slightly higher for 48V input voltage as compared to 42V. Fig. 4.10(a) and Fig. 4.10(b) depict the output voltage and current at full-load and light-load, respectively. These waveforms also indicate uniform output voltage of 380V under different load condition. Fig. 4.11 depicts the voltage waveform appearing across the transformer secondary and the current flowing through secondary side diodes verifying natural turn-off.

Therefore, the proposed converter design has been validated for the variation in input voltage under full-load as well as light-load condition.

4.5.2 Experimental Results

Considering aforementioned design constraints, converter parameters are estimated which are listed in Table 4.1. A proof-of-concept 500W laboratory hardware prototype has been built to validate the proposed design, simulation results and to gauge experimental behaviour. This section illustrates steady-state experimental results from the laboratory prototype for the converter specifications listed in Table 4.2 with the hardware specifications in Table 4.3. The main objective is to validate the ZCS operation and expected claims of the proposed converter for the supply voltage range of 30V-58V at different load condition in accordance with the low voltage alternative source (solar panel, fuel-cell stack) profile. The gating signals for the semiconductor devices were generated using DSP TMS20F28335 in open loop. The gating signals for the complementary pairs S_1-S_4 and S_3-S_2 are 180° phase-shifted. Programmable dc power supply is used to emulate variable source voltage and a resistor bank is employed to mainitain uniform 380V dc across the load-terminal. HF

TABLE 4.1: DESIGN PARAMETERS

Parameter	Value
Resonant Inductor, L_r	5.5μH
Resonant Capacitor, C_r	132nF
Input Inductor, L_{in}	100μH
Output Capacitor, C_1, C_2	80μF
Turns ratio, n	5.2

TABLE 4.2: CONVERTER SPECIFICATIONS

Parameter	Value
Input Voltage, V_{in}	30-58V
Output voltage, V_o	380 V
Maximum output power, P_o	500W
Switching frequency, f_{sw}	135-160 kHz
Duty ratio, D	0.73

TABLE 4.3: HARDWARE SPECIFICATION OF THE LABORATORY PROTOTYPE

Component	**Specifications**
Boost inductor L_{in}	55 x 28 x 21 EE ferrite Core, 100μH
Converter Switches, $S_{1\text{-}4}$	SCT3060ALGC11-ND, 650V,39A,60mΩ
Series Resonant Inductor, L_r	EE ferrite core, 3.42μH
Resonant Capacitor, C_r	135nF 1kV Film capacitor
HF Transformer, T_1	EE ferrite core, Primary turns, N_1=10, secondary turns N_2=52, L_{lk}= 1.64μH
Rectifier Diodes D_1, D_2	STPSC20065D, 650V, 20A,V_f= 0.8V
Output Capacitor, C_1, C_2	80μF 450V electrolytic capacitor, 10nF film capacitor
Gate driver IC	HCNW3120
DSP Platform	TMS230F28335

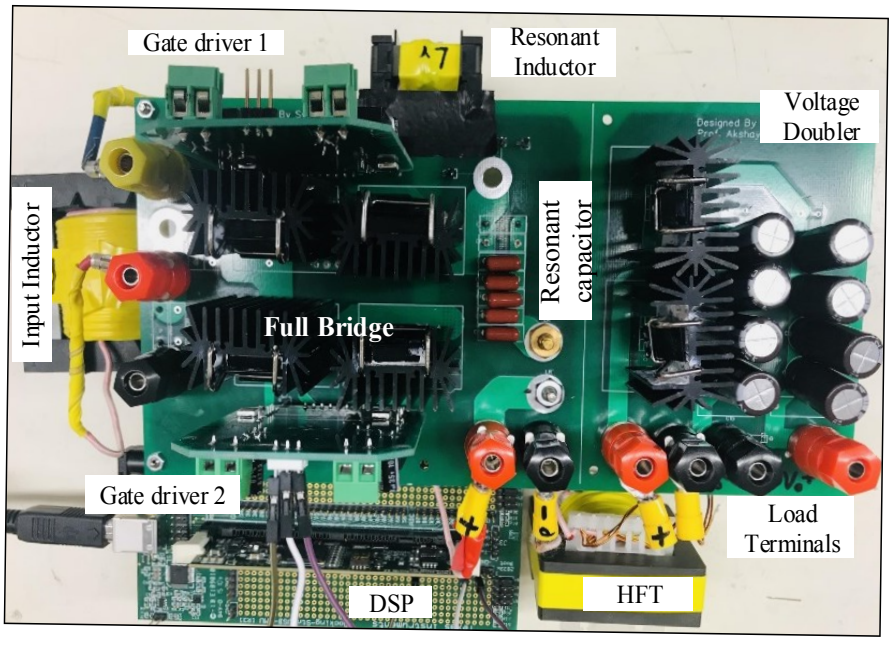


Fig. 4.12. Hardware prototype of the proposed converter.

transformer turns ratio of 1:5.2 is chosen to contribute towards the overall voltage-gain requirement. Fig. 4.12 shows an elevated view of the experimental setup. The experimental test results are recorded on Yogogawa digital storage oscilloscope.

Steady-state experimental results for case (1) with V_{in} = 30V at 500W and 160 kHz switching frequency are depicted in Fig. 4.13. The gating pulses for the switch pair S_1, S_4, resonant current I_{Lr} and voltage appearing across the switches V_{DS} are shown in Fig. 4.13(a). The commutation of the semiconductor devices occur during switching overlap, where resonance sets in, transferring the current from the outgoing switch pair (S_1, S_4) to the incoming switch pair (S_2, S_3). It should be noted that the short resonance results in sinusoidally varying transformer current that naturally decreases the switch current to zero. Later, its body diode takes over and the gating signal is removed after switch current reaches zero, thereby, preventing any overshoot across the switch with ZCS turn-off. It is also observed that a small amount of current flows through the internal body diode thereby limiting device losses. Fig. 4.13(b) depicts steady-state waveforms for the resonant capacitor charge V_{cr}, bridge voltage V_{AB} and resonant current I_{Lr} that matches closely with the analytical waveforms. It should be noted that the series capacitor charges linearly when only one switch pair is conducting owing to the constant current (I_{in}) and hence, defines the energy transfer region, transferring power from input to the load. The peak switch voltages are settled at 160V and a peak resonant current of 18.5A.

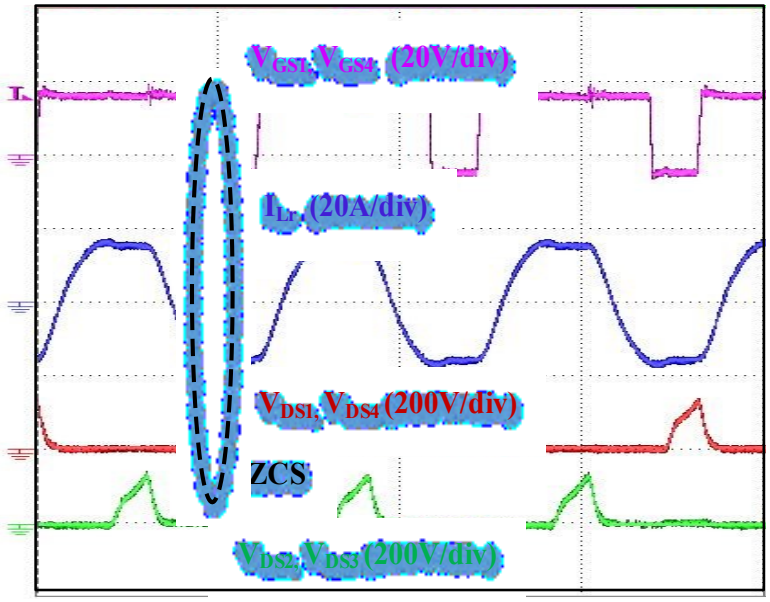
Fig. 4.14(a) depicts the steady-state experimental waveforms for case (2) with V_{in} = 40V and f_{sw}=150 kHz at full-load. It should be noted that sinusoidally varying resonant current allows body-diode conduction resulting in ZCS turn-off of the semiconductor devices and eliminates voltage spike at turn-off. Relatively higher I_{Lrp}/I_{in} ratio is observed for higher source voltages causing a relatively larger current to flow through the diode. Fig. 4.14(b) reflects marginal increase in resonant capacitor charge V_{cr}, and resonant current peak I_{Lrp} for step increase in source voltage.

Steady-state experimental results for case (3) with V_{in}= 50V at full-load with switching frequency at 140 kHz are illustrated in Fig. 4.15. Fig. 4.15(a) confirms ZCS operation of the devices at turn-off and alleviates voltage overshoot across them. Fig. 4.15(b) demonstrates the ttypical waveform of the resonant capacitor voltage, resonant current and full-bridge output voltage conforming the given analysis. Experimental results for case (4) with V_{in}= 58V and

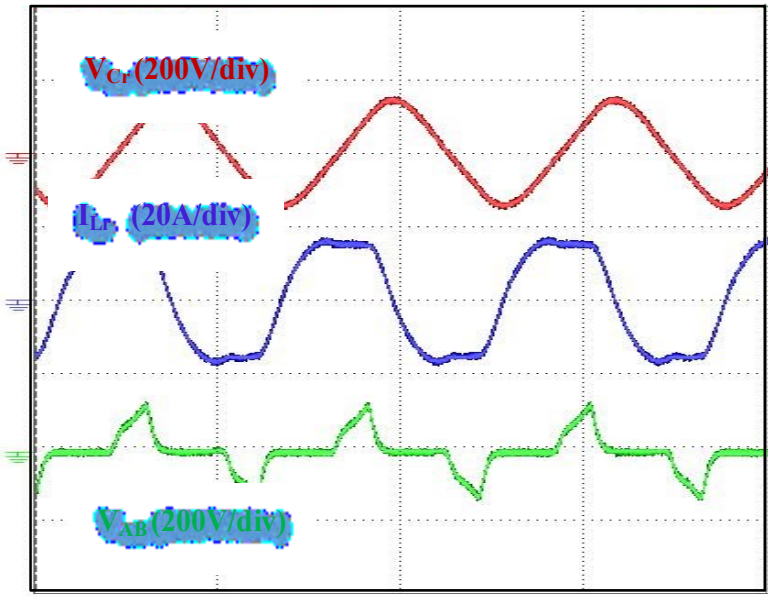
f_{sw} = 135 kHz at full-load are depicted in Fig. 4.16. In Fig. 4.16(a) natural commutation for the semiconductor devices for the worst case scenario (98% variation from the V_{min}) has been observed. Similar to the earlier cases, the proposed claims are true for this case as well. The proposed converter module further experience swell in the capacitor charge and resonant current peak as witnessed in Fig. 4.16(b). Therefore, it can be concluded that higher input voltage values result in relatively higher ratio of peak current to the input current (I_{Lrp}/ I_{in}) which in effect reflects increased capacitor voltage and increased switch voltage for higher source voltages. Furthermore, uniform load voltage of 380V has been attained through variable frequency modulation for all cases illustrated in Fig 4.17(a), (b), (c) and (d) .

The proposed modular design is also tested for variable load condition to evaluate its suitability for the wide range of applications. Additional experimental results for 80% load and 20% load are demonstarted. The proposed clamis hold true for loads below rated condition as witnessed in Fig. 4.18 and Fig. 4.19. It should be noted the peak voltage across switching devices, reduces with decrease in the load current owing to the load dependent resonant energy. The important point to note is that the ratio of peak current to the input current (I_{Lrp}/ I_{in}) is much lower at light load condition and therefore, results in improved part-load efficiency. It can be concluded that ZCS operation and device voltage clamping is preserved without compromising in the conversion efficiency for wide source voltage range. It is also perceived that the switching frequency variation is more sensitive to the load variations than source voltage variations. As a result, the proposed converter allows safe ZCS operation from full-load to 20% load with overall switching frequency range of 75-160 kHz.

Fig. 4.20 shows the steady-state experimental waveforms for current through and voltage across the rectifier diode for different source voltages at rated load condition. Natural commutation of diodes can be witnssed through these waveforms. As evident from Fig. 4.21, the maximum voltage stress experienced by the semicondcutor switches is limited to 200V. The findings in Fig. 4.21 elucidate the switching frequency trend with the source voltage variation for rated load and light-load condition. Narrow frequency band is observed for full-load condition that ranges between 135 kHz–160 kHz. This characteristic curve affirms the need for variable frequency operation to preserve output voltage regulation and natural commutation of the switching devices. It should also be observed that the frequency variation is less sensitive to the input voltage variation as compared to other state-of-the art topologies.

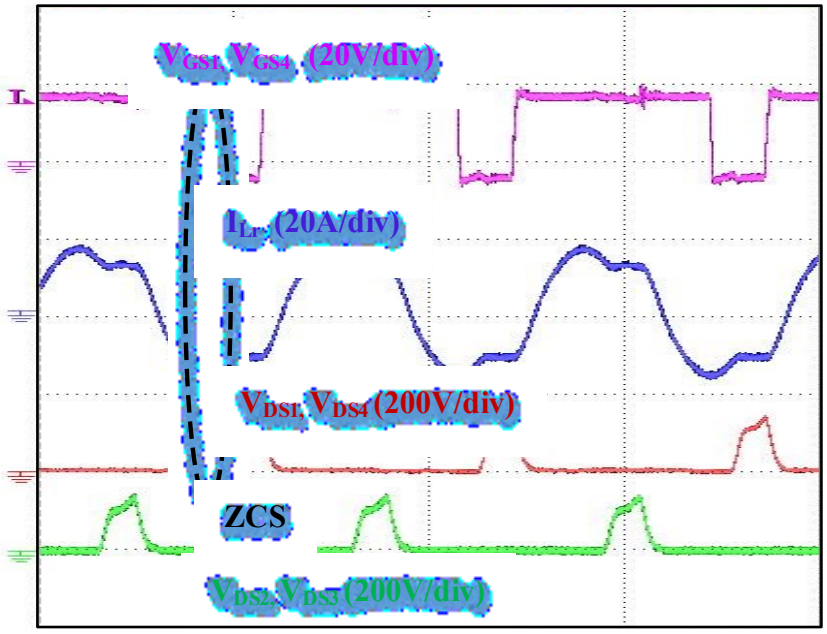


(a)

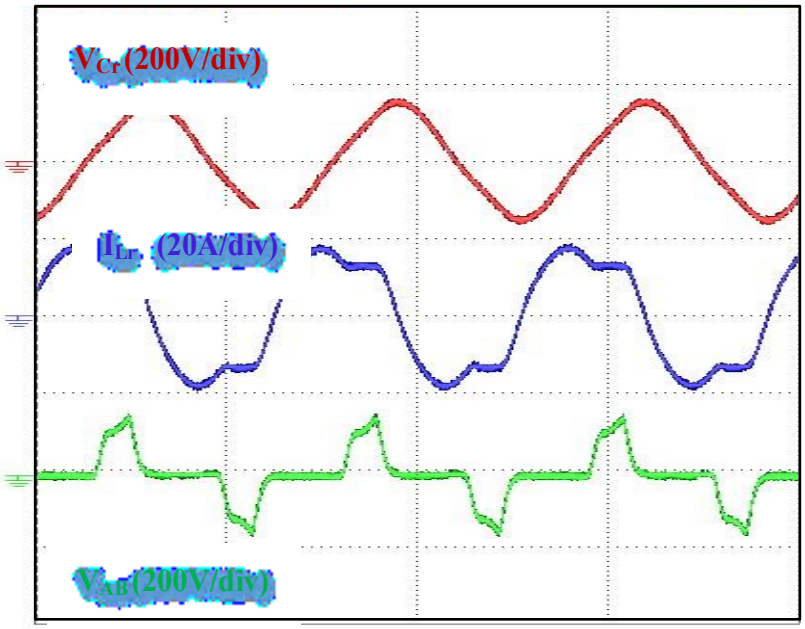


(b)

Fig. 4.13. Experimental results for V_{in} = 30V (a) Gate-source voltage V_{GS1}, V_{GS4}, resonant current I_{Lr}, and drain-to-source voltages (b) resonant capacitor charge V_{Cr}, resonant current I_{Lr} and bridge output voltage V_{AB} at full load (500W) (time scale: 5µs/div).

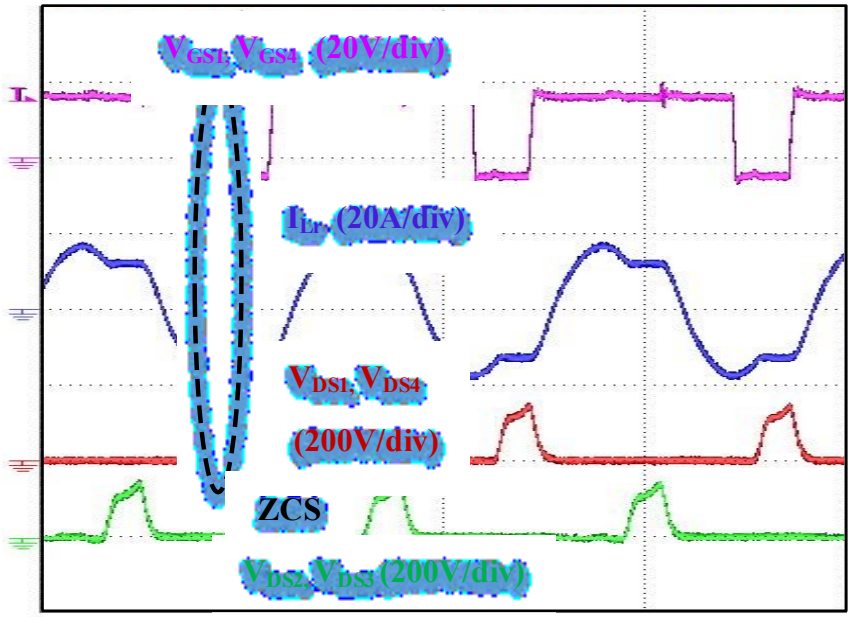


(a)

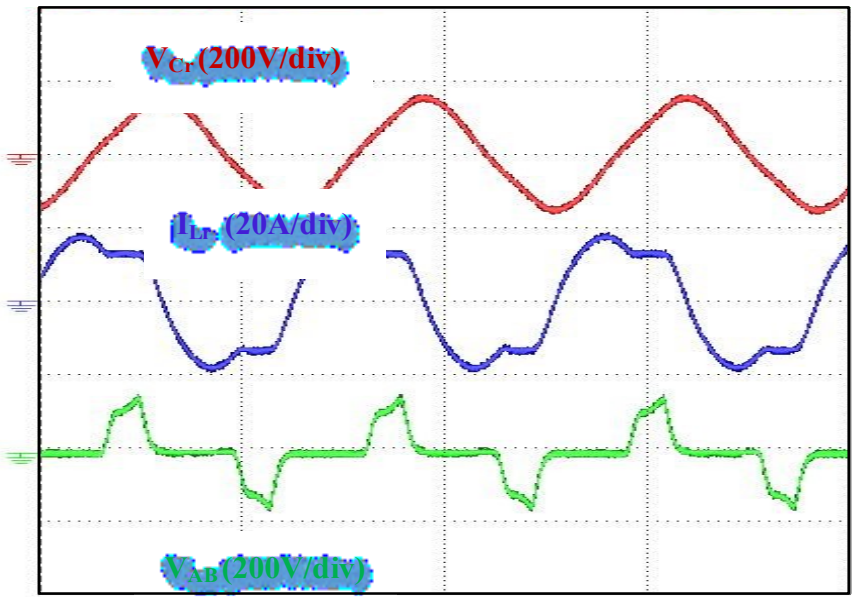


(b)

Fig. 4.14. Experimental results for V_{in} = 40V (a) Gate-source voltage V_{GS1}, V_{GS4}, resonant current I_{Lr}, and drain-to-source voltages (b) resonant capacitor charge V_{Cr}, resonant current I_{Lr} and bridge output voltage V_{AB} at full load (500W) (time scale: 5µs/div).

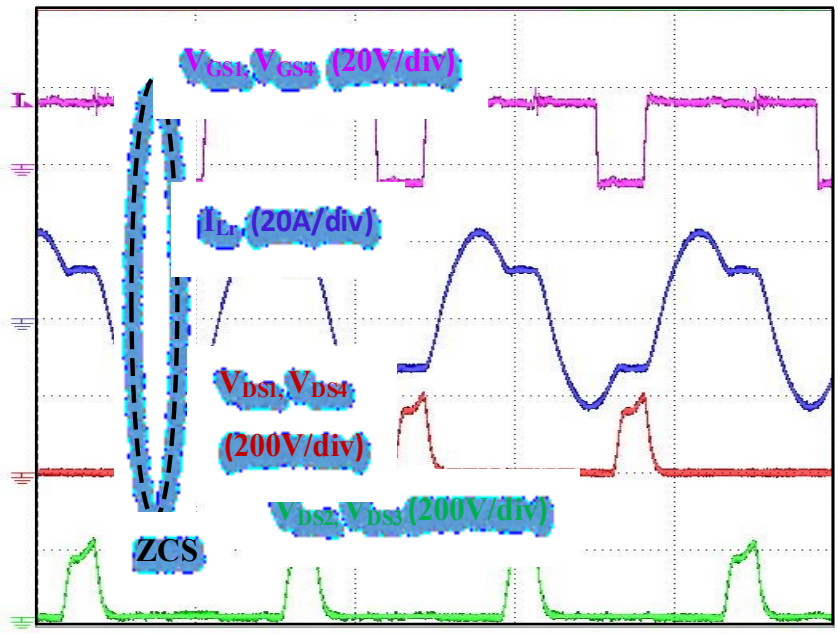


(a)

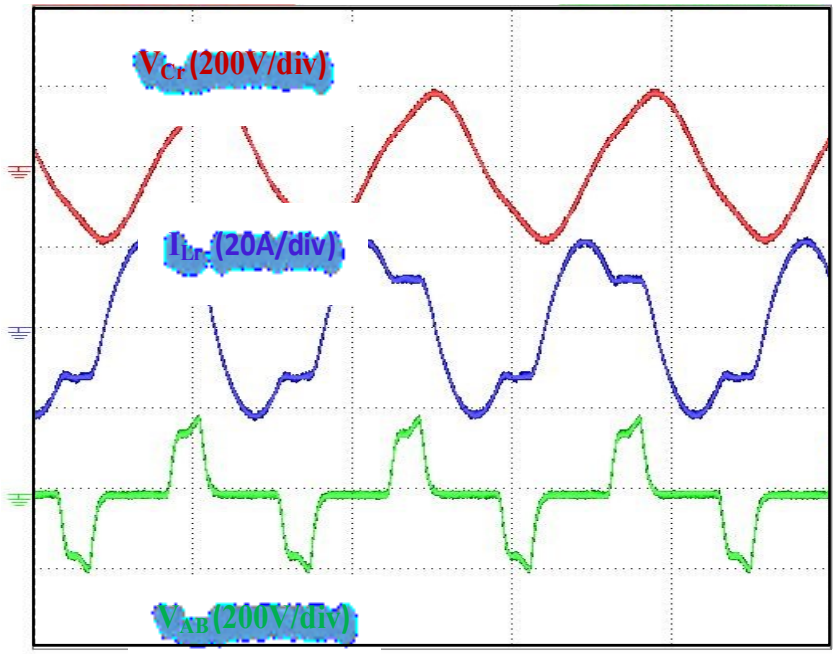


(b)

Fig. 4.15. Experimental results for V_{in} = 50V (a) Gate-source voltage V_{GS1}, V_{GS4}, resonant current I_{Lr}, and drain-to-source voltages (b) resonant capacitor charge V_{Cr}, resonant current I_{Lr} and bridge output voltage V_{AB} at full load (500W) (time scale: 5µs/div).

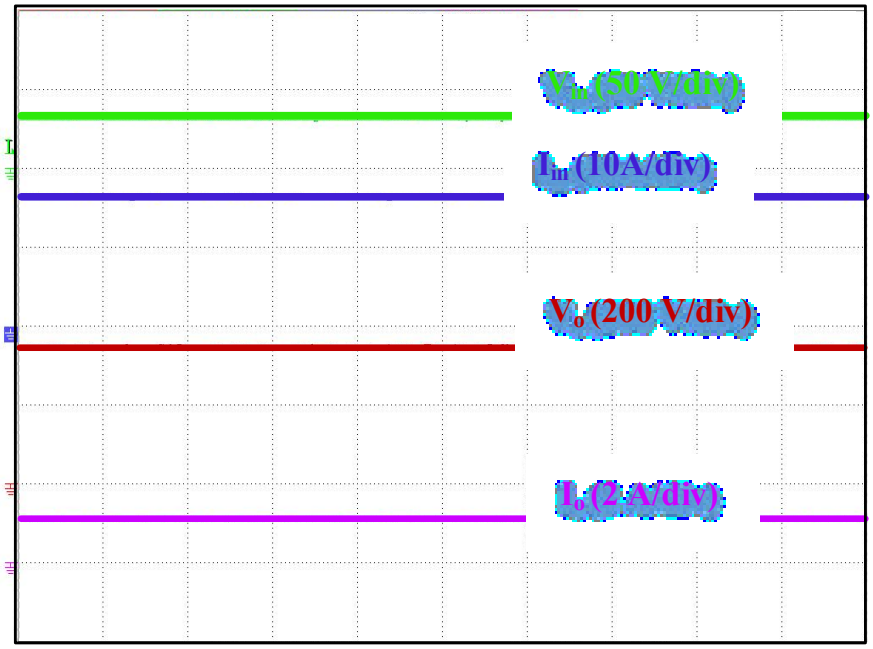


(a)

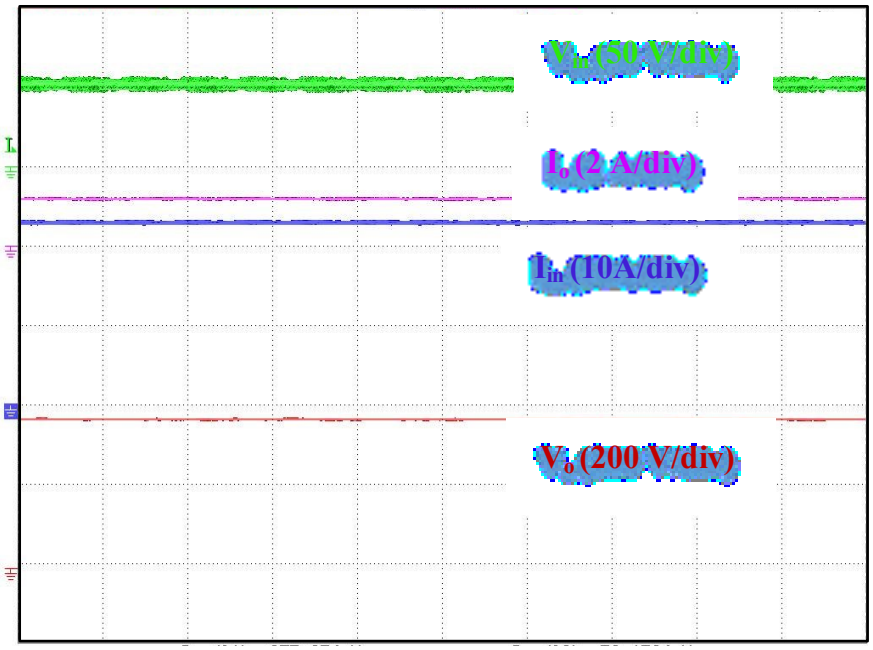


(b)

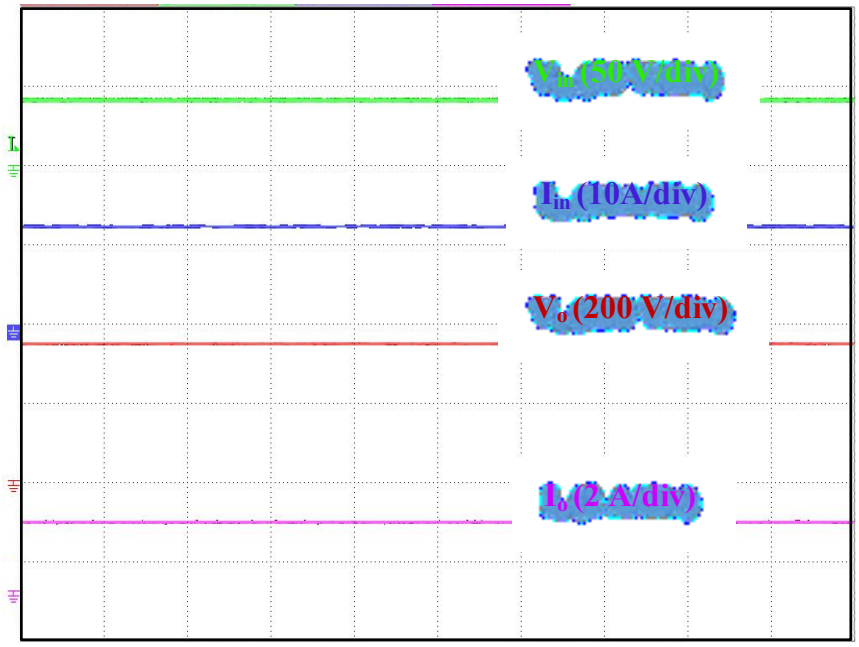
Fig. 4.16. Experimental results for V_{in} = 58V (a) Gate-source voltage V_{GS1}, V_{GS4}, resonant current I_{Lr}, and drain-to-source voltages (b) resonant capacitor charge V_{Cr}, resonant current I_{Lr} and bridge output voltage V_{AB} at full load (500W) (time scale: 5µs/div).


V_{in} (50 V/div)
I_{in} (10A/div)
V_o (200 V/div)
I_o (2 A/div)

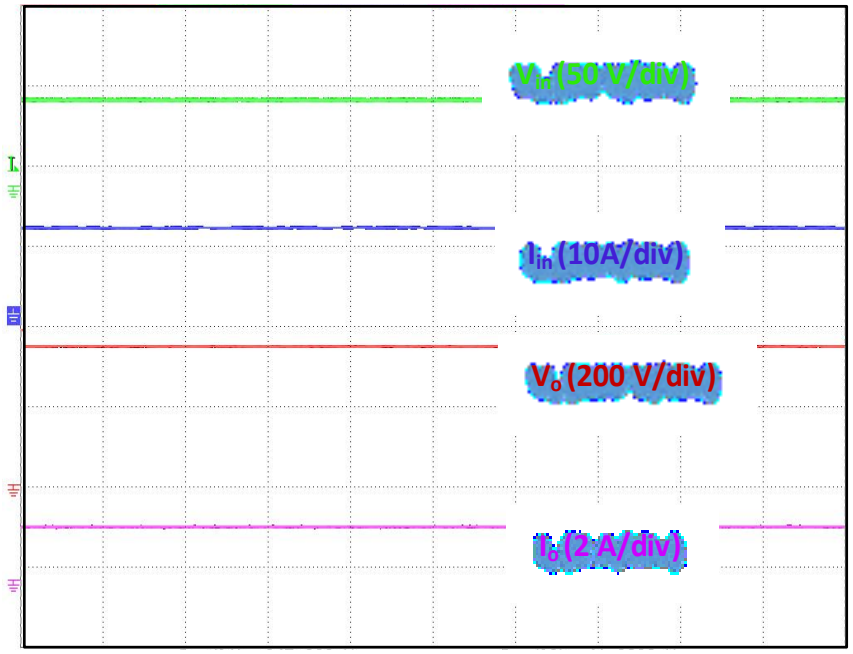
(a)


V_{in} (50 V/div)
I_o (2 A/div)
I_{in} (10A/div)
V_o (200 V/div)

(b)

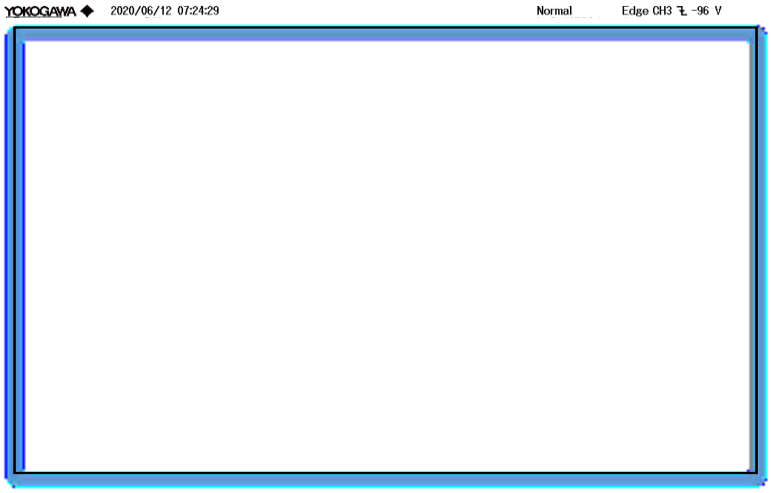


(c)

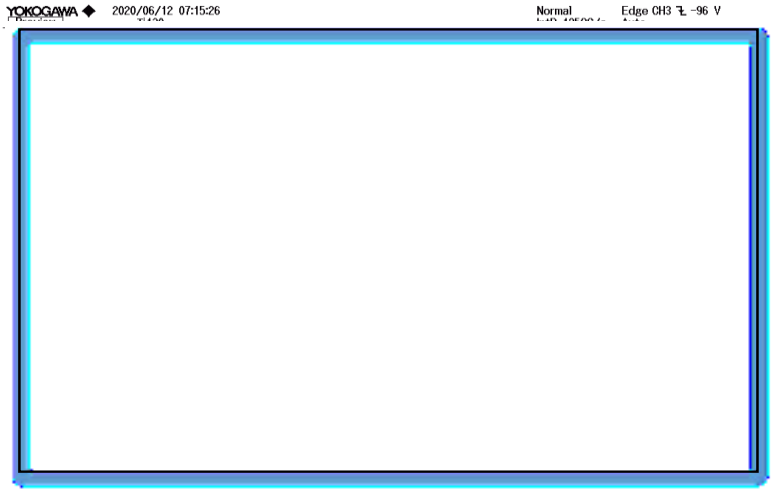


(d)

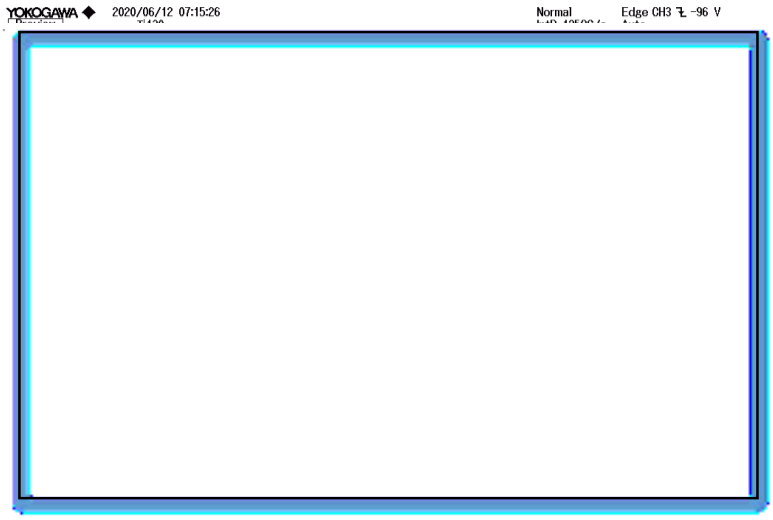
Fig. 4.17. Experimental results for Input current and voltage I_{in}, V_{in}, output current and voltage I_o, V_o with (a) V_{in} = 30V (b) V_{in} = 40V (c) V_{in} = 50V and (d) V_{in} = 58V at full load (500W) (time scale: 5µs/div).



(a)

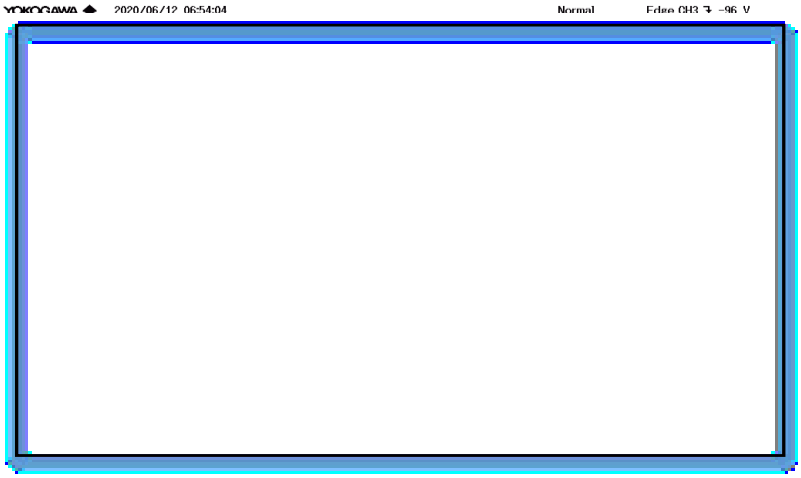


(b)

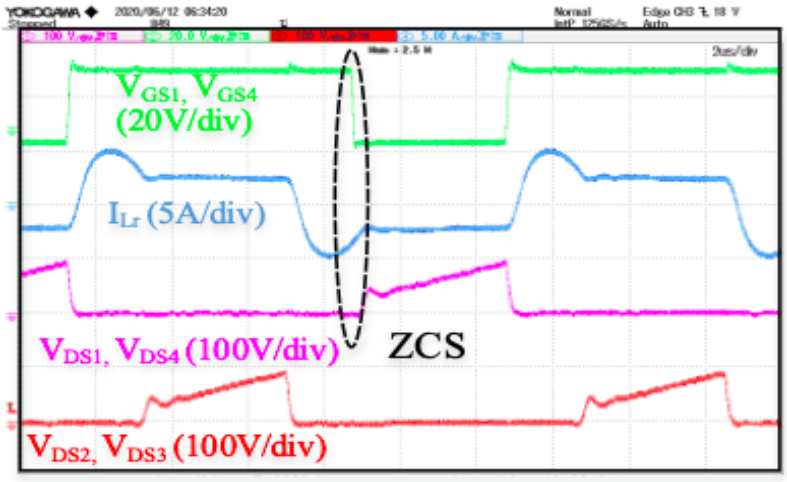


(c)

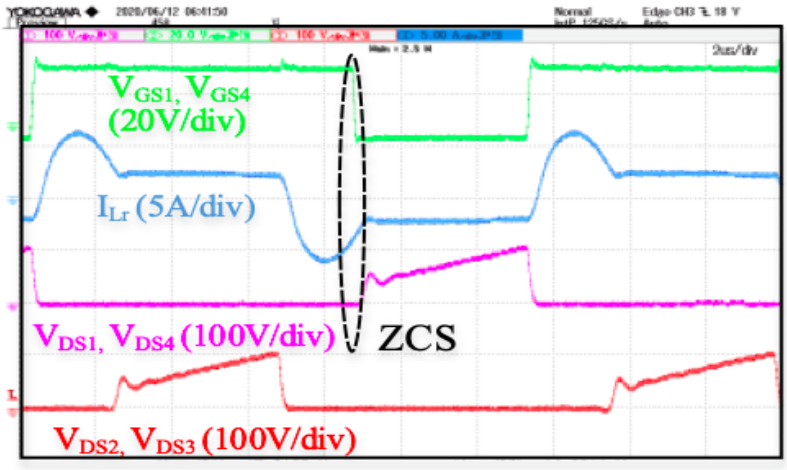
Fig. 4.18. Experimental steady state results for source voltages (a) V_{in} = 30V (b) V_{in} = 40V and (c) V_{in} = 50V at 80% load condition (time scale:2µs/div).



(a)



(b)



(c)

Fig. 4.19. Experimental steady-state results for source voltages (a) V_{in} = 30V (b) V_{in} = 40V and (c) V_{in} = 50V at 20% load condition (time scale: 2µs/div).

(a)

(b)

(c)

Fig. 4.20. Experimental results for rectifier diode current and voltage at rated-load (500W) for (a) V_{in} = 30V (b) V_{in}= 40V and (c) V_{in} = 50V.

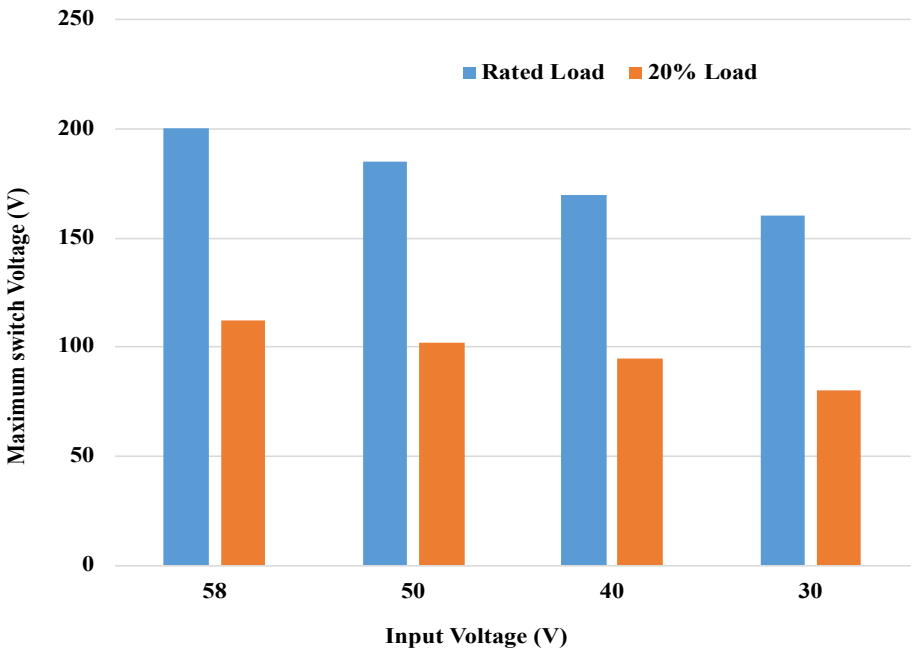


Fig. 4.21. Maximum switch voltage stress with input voltage variation.

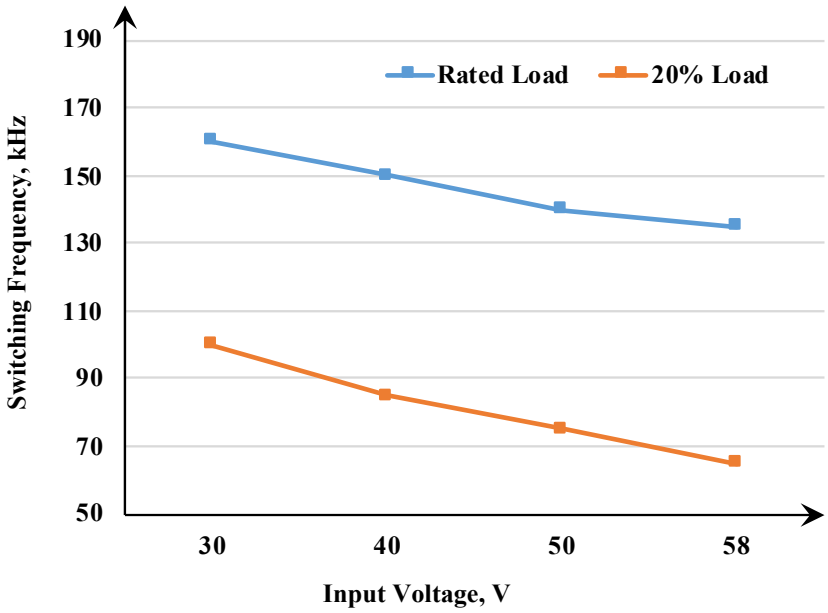


Fig. 4.22. Switching frequency variation with different input voltages.

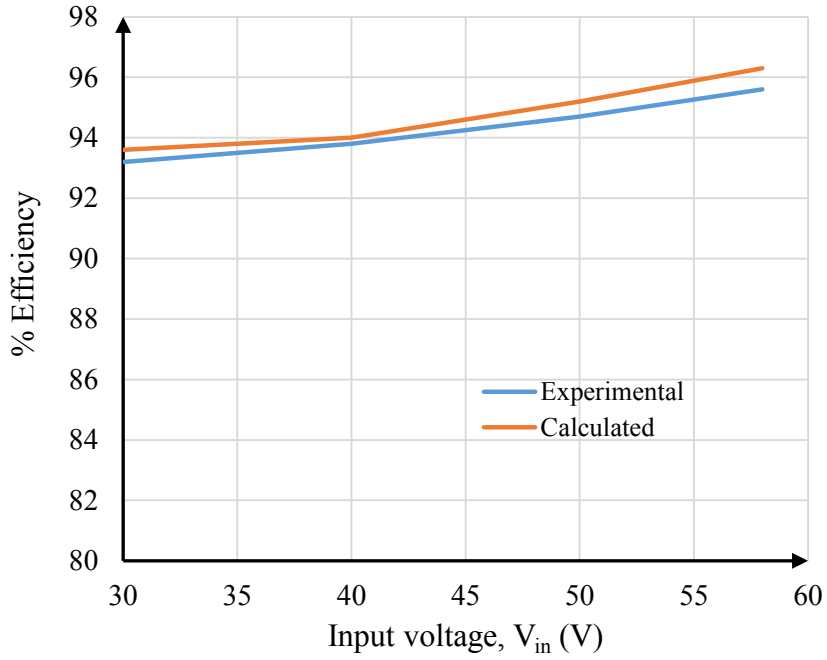


Fig. 4.23. Efficiency curves with input voltage variation at rated power.

Comparison between measured experimental efficiency and calculated efficiency at rated load for different source voltages is depicted in Fig. 4.22. Maximum full-load efficiency of 95.6% for V_{in}= 58V and minimum efficiency of 93.2% for V_{in}=30V is observed on the hardware prototype. Also, the maximum efficiency under light-load (20%) is recorded to be 93.5%. Table 4.4 depicts the converter power loss for different input voltages at rated load. The experimentally recorded efficiency values are in accordance with the calculated values validating the theoretical analysis. The individual component losses are computed using loss equations given in Table A.1 and the selected components datasheet parameters. It should also be observed that the switching losses are primarily due to hard turn-on of the primary side MOSFETs while the rectifier diodes hold negligible turn-on loss. Conduction loss covers the substantial part of the total converter loss, which are observed in semiconductor switches, diodes, HF transformer and boost inductor. Hardware prototype can further be optimized by careully tackling circuit paracitics and efficient printed circuit board (PCB) layout, eradicating the need for additional lossy snubbers.

TABLE 4.4: LOSS DISTRIBUTION AND THEORETICAL EFFICIENCY

Output power	500	500	500	500	W
Input Voltage	58	50	40	30	V
Input Current	8.62	10	12.5	16.66	A
Loss Type					
MOSFET conduction loss	11.23	13.53	20.22	21.78	W
MOSFET switching loss	2.29	2.14	1.84	1.58	W
Rectifier diode loss	2.51	2.31	2.11	1.81	
Total semiconductor losses	16.03	17.98	24.17	25.17	W
Input Boost inductor loss	1.55	2.25	3.75	5.64	W
HF Transformer loss	2.03	1.92	1.81	1.50	W
Gate drive loss	0.044	0.046	0.049	0.054	W
Auxiliary loss/stray loss	0.35	0.30	0.20	0.13	W
Total power losses	20.01	22.50	30.03	32.0	W
Efficiency	96.2	95.5	94.01	93.6	%

4.6 Conclusion

In this Chapter, a series resonant tank assisted partial resonance-pulse operated current-fed full-bridge dc/dc converter is conceptualized and analyzed for low voltage high current (solar, fuel-cell based) applications. The major objectives including zero current commutation and voltage-clamping of the semiconductor switches are achieved without any external snubber or clamping circuits. Resonance pulse is effectively implemented to obtain wide range ZCS of the semiconductor devices with significantly low circulating and peak currents. Furthermore, merits like stiff dc input current and lower circulating current help in avoiding overrated devices and large heat sinks, resulting in better efficiency and small size of the proposed converter module. Moreover, higher power level can be easily realized by utilizing proposed unit module in several configurations with higher control flexibility, competency for fault tolerant and easy maintenance.

Detailed experimental results obtained from the proof-of-concept hardware prototype rated at 500W are demonstrated to verify the proposed claims and converter performance. The experimental waveforms confirm theoretical analysis and simulation results from PSIM 11.1. Peak experimental efficiency of 95.6% at full-load power for 58V source voltage is recorded.

Owing to the load adaptive resonant energy, significantly lower voltage and current stresses are recorded for light load with relatively higher efficiency. Moreover, narrow switching frequency range (135 kHz-160 kHz) for wide source voltage variation (30-58V) at rated load allows seamless integration of alternative sources with huge variability in DC voltage. Many such applications include, PV enabled back-up power supply and constant power motor drive applications.

Chapter 5

Partial Resonance-Pulse Assisted Current-Fed Three-phase current sharing DC-DC Converter

5.1 Introduction

In the preceding Chapter, soft-switching single-phase full-bridge DC-DC converter is proposed and analyzed that offers, due to modularity, easier power scalability and simpler thermal requirements. However, paralleling of the power converters, interleaved and modular configurations suffer from high semiconductor device count resulting in high susceptibility to switch failures. Moreover, large number of semiconductor switches require additional gate driving circuits resulting in higher cost and larger volume system. Therefore, with the focus on achieving higher power handling capability and higher reliability, a three-phase current-sharing DC-DC converter topology using minimum semiconductor devices is proposed in this Chapter. Current-sharing three-inductor configuration prevents high current stresses across the primary side switches with simpler gate drive requirement along with the input current ripple cancellation.

Further, high power density being one of the most desirable features for many industrial applications necessitates high switching frequency operation. However, high switching losses, together with the inherent switch turn-off voltage spike in the current-fed converter, restrict the usage of traditional hard-switched configurations for achieving high-power density with acceptable efficiency. Therefore, to overcome these inherent limitations, short resonance pulse is adopted to facilitate zero-current switching (ZCS) and voltage clamping across the semiconductor devices. In addition, to meet the electrical characteristics of the DC microgrid applications of 380V, the proposed three-phase interleaving stage is used in conjunction with three single-phase high frequency transformers obtaining the desired voltage level and galvanic isolation.

The major contributions of the three-phase solution proposed in this Chapter are underlined as follows:

1. Current sharing architecture exhibits lower rms current through the power components, when compared to single-phase solutions for the equivalent power rating.
2. Low-ripple input current due to interleaving inductors making it suitable for the interconnection of low voltage high current applications, and may improve stack lifetime and efficiency in case of fuel cell source.
3. Use of only three semiconductor switches having the same ground reference, feature simplicity in the gate drive and control circuit.
4. Adaptive resonant-pulse feature enables lower peak current and lower I_{Lrp}/I_{in} ratio for the load below rated-load, significantly improving the light-load efficiency.
5. ZCS turn-off of the primary switches eliminating voltage spikes across the semiconductor devices.
6. Reduction in the filter size owing to the high frequency ripple at three times the switching frequency ($3*f_{sw}$).
7. Further, the system repair and maintenance are easy owing to three single-phase high frequency transformers, and can continue operation at lower power levels under faulty condition as well.

The objective of this Chapter is to study and analyse the series resonance-pulse concept for the soft commutation of the semiconductor switches in the proposed three-phase current-fed configuration for the seamless integration of variable voltage source to high voltage DC bus. With the aforementioned goal, this Chapter is organized as follows: Section 5.2 elaborates the operating principle, modulation strategy and the circuit characteristics of the proposed converter. Section 5.3 presents the steady-state analysis with mathematical expressions. Section 5.4 illustrates the converter design to support the theoretical verification and appropriate component's selection with a design example. Section 5.5 covers the steady-state simulation and the experimental results with the detailed efficiency analysis. Section 5.6 presents the concluding remarks.

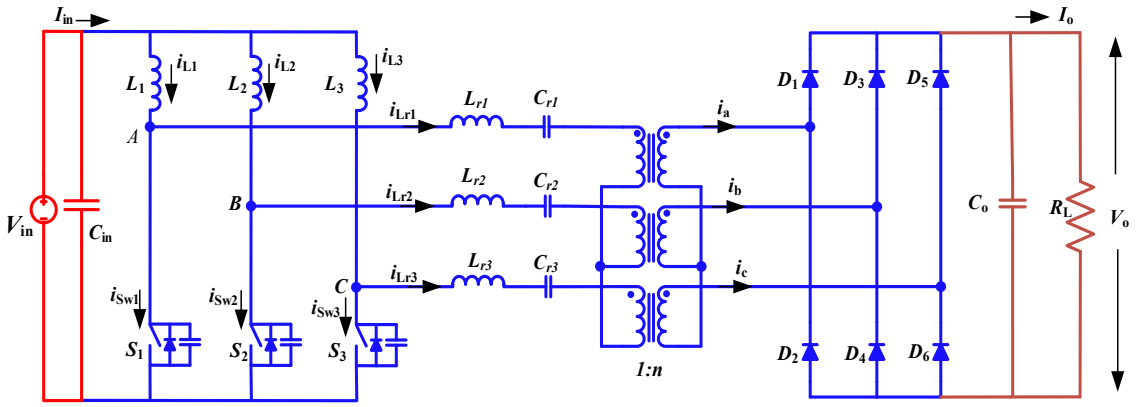


Fig. 5.1. Schematic for the proposed series-LC resonant-pulse current-fed three-phase current sharing

5.2 Proposed Converter Topology

Fig. 5.1 shows of a current-fed three-phase converter with, three star-connected single-phase high-frequency transformers and a three-phase rectifier bridge with capacitive output. Secondary windings of the high-frequency transformers feed the three-phase rectifier bridge. The transformer leakage inductances with additional series high frequency capacitances (C_{r1}, C_{r2} and C_{r3}) constitute the series resonant tank in each phase which facilitates device voltage clamping and ZCS commutation of the semiconductor devices during the overlap conduction duration eliminating the need for the external snubber or clamping circuit. The proposed current sharing topology is modulated with variable frequency constant overlap modulation technique obtaining load voltage regulation for wide operating range. Load dependent resonant capacitor charge due to its series placement exhibits significantly low leakage energy circulation through the components at light-load conditions resulting in relatively higher efficiency. The proposed topology is characterized by high voltage conversion ratio, low current ripple, low transformer turns-ratio in conjunction with ZCS commutation of the switches over a wider load range.

5.3 Steady State Analysis of the Converter

The steady-state operating waveforms of the proposed converter are shown in Fig. 5.2. Semiconductor switches in the primary are modulated with the gate signals phase shifted by 120º having a small overlap with duty ratio ranging between $0.33 < D < 0.66$. The mathematical analysis has been conducted out for one sixth of the switching cycle (t_1-t_8), since

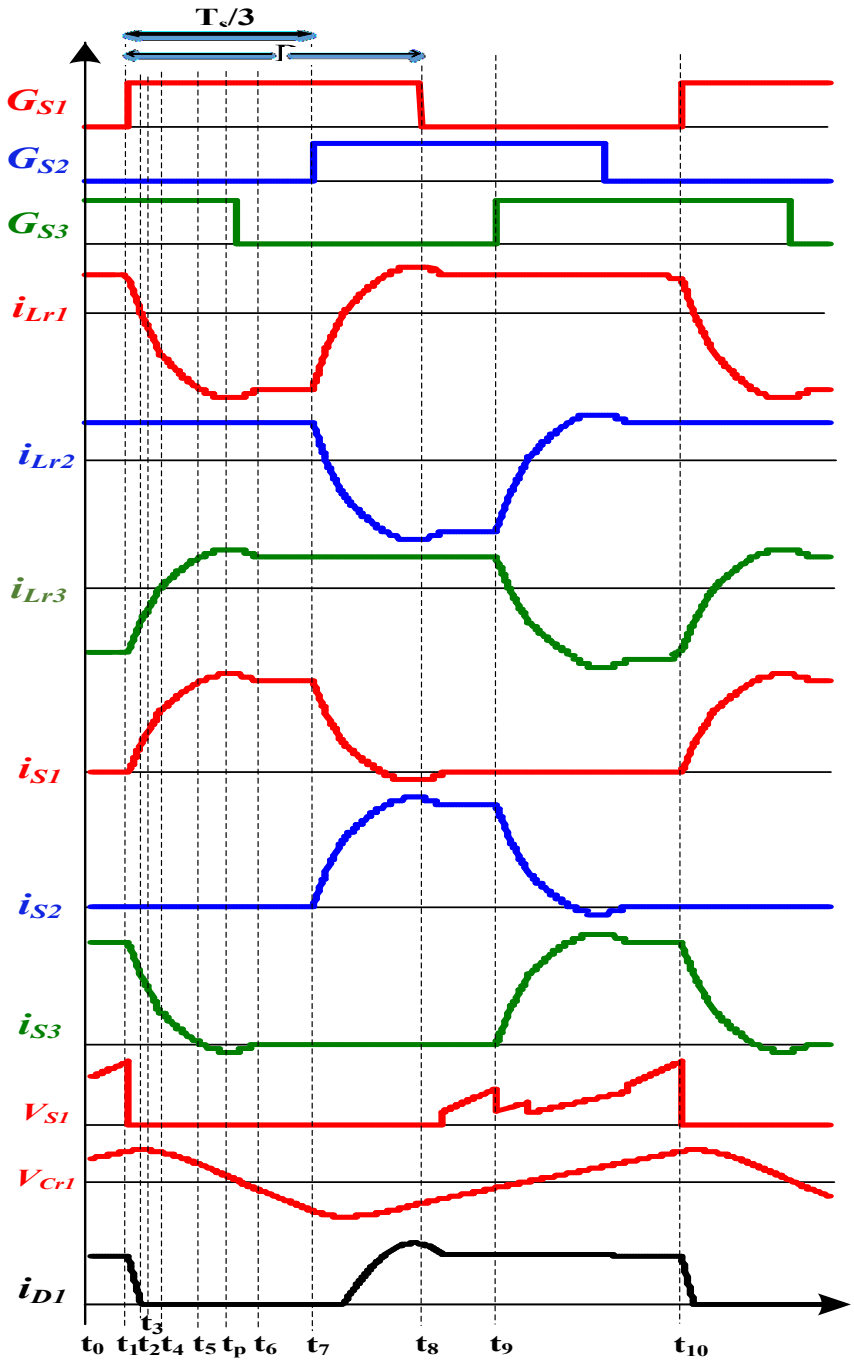
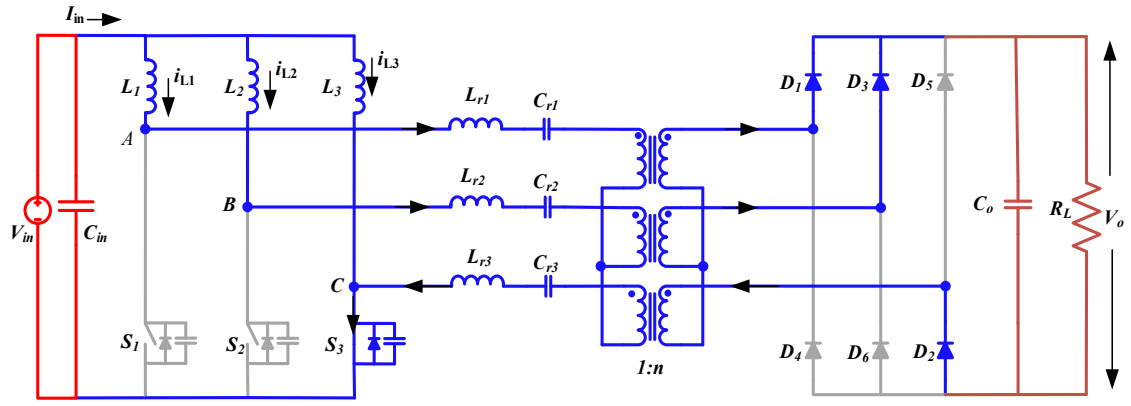


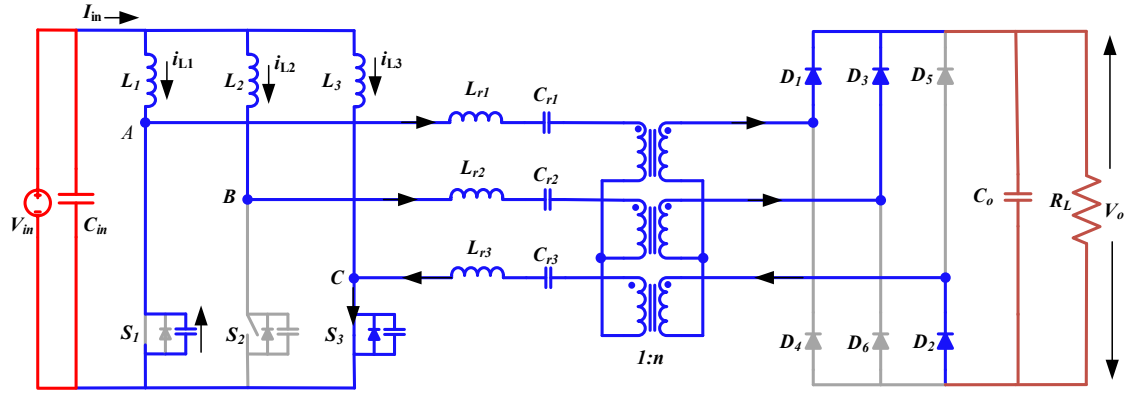
Fig. 5.2. Steady state operating waveforms of the proposed converter topology.

the converter operation is similar for every 30° sector. The operation of the converter during $T_s/3$ period is divided into 7 intervals. Current and voltage equations obtained during each interval help in determining the component's ratings and validating the converter performance analytically. To simplify the analysis, the high frequency transformers are modelled as ideal

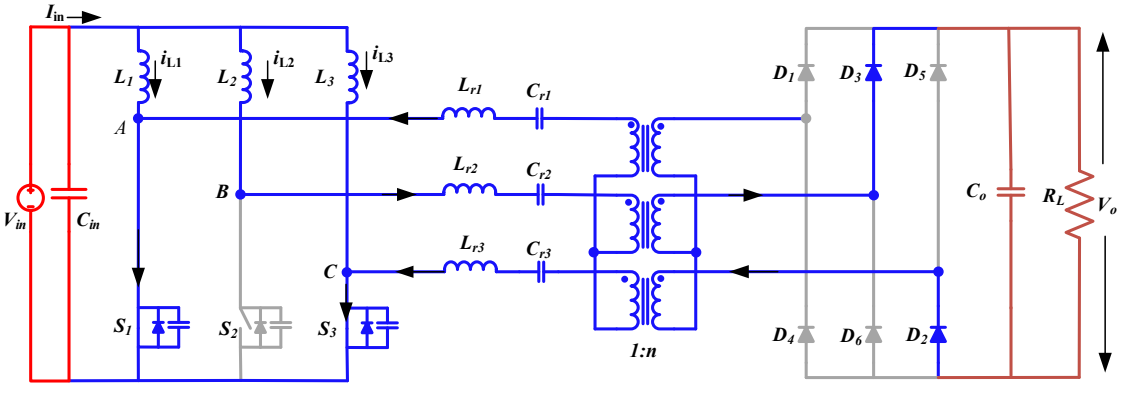
transformer assuming infinitely large magnetizing inductance. Moreover, it is assumed that the interleaving boost inductors and output capacitor are large enough to provide low ripple in the input current and across load voltage, respectively.



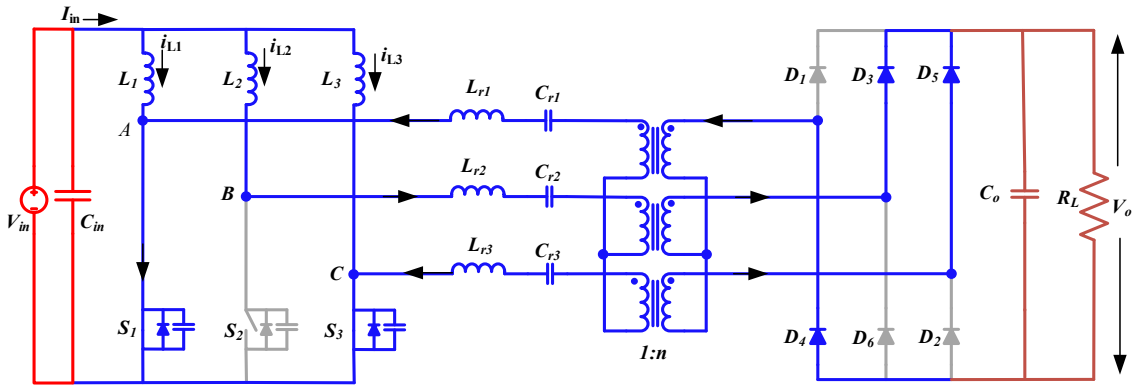
(a)



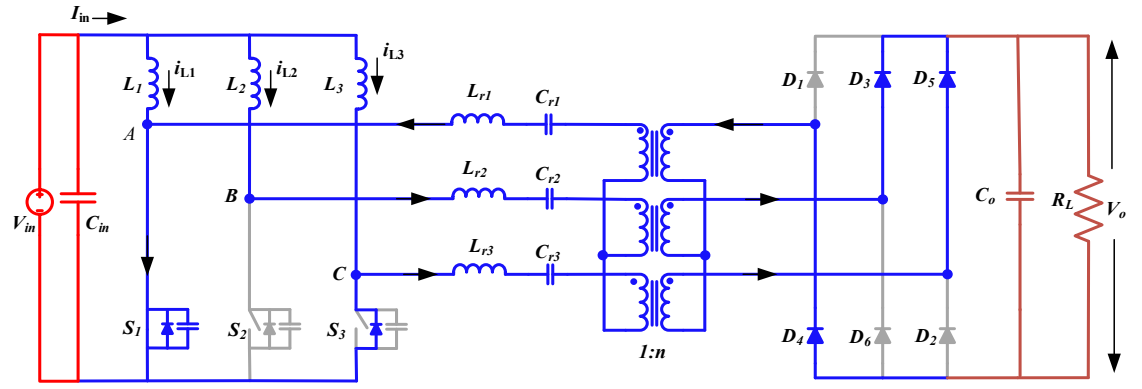
(b)



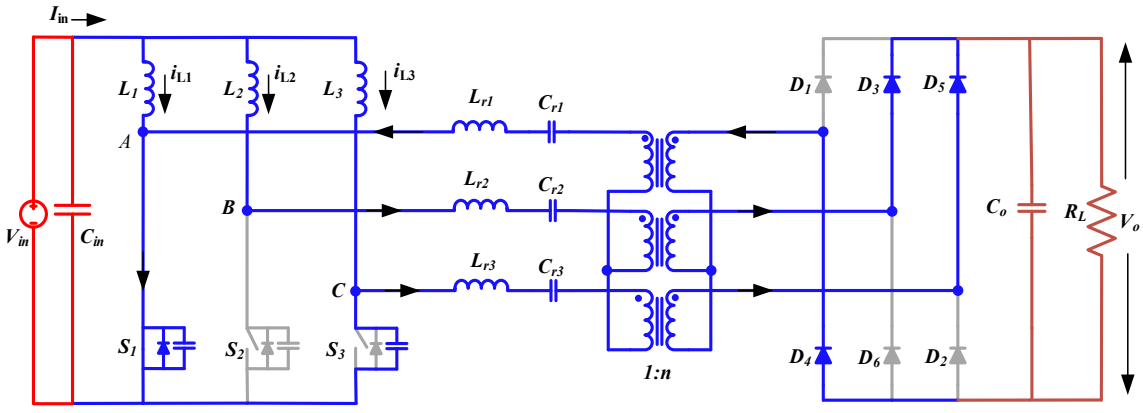
(c)



(d)



(e)



(f)

Fig. 5.3. Equivalent circuits representing different intervals of operation of the proposed three-phase configuration

Interval 1 (t_0-t_1): (Power transfer interval refer Fig. 5.3(a))

In this interval, switch S_3 is conducting with a constant current I_{in} through it while the other two switches (S_1 and S_2) are in blocking state. The boost inductor L_3 is charged with constant current $I_{in}/3$. Positive current flows through the series resonant branch in phase A and phase B with charging of resonant capacitors (C_{r1} and C_{r2}) during this time. Power transfer happens through rectifier diodes D_1, D_2 and D_3.

General charging equations of the series resonant capacitors can be given as:

$$V_{cr1}(t) = V_{cr1}(t_o) + \frac{1}{C_{r1}}\int_{t_o}^{t} \frac{I_{in}}{3} dt \tag{5.1}$$

$$V_{cr2}(t) = V_{cr2}(t_o) + \frac{1}{C_{r2}}\int_{t_o}^{t} \frac{I_{in}}{3} dt \tag{5.2}$$

Final values at the end of this interval with $t=t_1$ are:

$$i_{\mathrm{Lr1}}(t_1) = \frac{I_{in}}{3}, \qquad i_{\mathrm{Lr2}}(t_1) = \frac{I_{in}}{3}, \qquad i_{\mathrm{Lr3}}(t_1) = -\frac{2I_{in}}{3} \tag{5.3}$$

$$i_{S1}(t_1) = 0, \qquad i_{\mathrm{S2}}(t_1) = 0, \qquad i_{\mathrm{S3}}(t_1) = I_{in} \tag{5.4}$$

$$T_{10} = \frac{T_s}{3} - T_{42} - T_{21} \tag{5.5}$$

During this interval, the resonant inductor voltages are zero causing constant current through phase A, B and C.

Interval 2 (t_1-t_2): (Switch transition interval refer Fig. 5.3(b))

This interval begins when S_1 is turned on while S_3 still conducting. The internal capacitance across switch S_1, discharges rapidly through the switch. However, the discharge takes negligible time and hence, can be neglected in the analysis. Consequently, incoming device current i_{S1} increases whereas the current through S_3 decreases linearly. At the same time, resonant current through phase *A* (i_{Lr1}) and phase *C* (i_{Lr3}) decreases and increases respectively. Power transfer continues through the rectifier diodes D_1, D_2, and D_3. The mathematical expressions representing this interval includes current through resonant branch in phase A, B and C which are given as,

$$i_{\mathrm{Lr1}}(t) = \frac{I_{in}}{3} - \frac{1}{2L_r}\left(\frac{V_o}{n} + 2V_{crp}\right)(t - t_1) \tag{5.6}$$

$$i_{\mathrm{Lr2}}(t) = \frac{I_{in}}{3} \text{ (constant)} \tag{5.7}$$

$$i_{\mathrm{Lr3}}(t) = \frac{1}{2L_r}\left(\frac{V_o}{n} + 2V_{crp}\right)(t - t_1) - \frac{2I_{in}}{3} \tag{5.8}$$

While the switch currents are governed by these equations,

$$i_{\mathrm{S1}}(t) = \frac{1}{2L_r}\left(\frac{V_o}{n} + 2V_{crp}\right)(t - t_1) \tag{5.9}$$

$$i_{\mathrm{S2}}(t) = 0 \quad \text{(constant)} \tag{5.10}$$

$$i_{\mathrm{S3}}(t) = I_{in} - \frac{1}{2L_r}\left(\frac{V_o}{n} + 2V_{crp}\right)(t - t_1) \tag{5.11}$$

$$T_{21} = \frac{2I_{in}L_r}{3\left(\frac{V_o}{n} + 2V_{crp}\right)} \tag{5.12}$$

Final values at the end of this interval are:

$$i_{\mathrm{Lr1}}(t_2) = 0, \qquad i_{\mathrm{Lr2}}(t_2) = \frac{I_{in}}{3}, \qquad i_{\mathrm{Lr3}}(t_2) = -\frac{I_{in}}{3} \tag{5.13}$$

$$i_{\mathrm{S1}}(t_2) = \frac{I_{in}}{3}, \qquad i_{\mathrm{S2}}(t_2) = 0, \qquad i_{\mathrm{S3}}(t_2) = \frac{2I_{in}}{3} \tag{5.14}$$

Interval 3 (t_2-t_3): (Resonance interval refer Fig. 5.3(c))

With resonant current i_{Lr1} reaching zero at instant t_2, current reversal in the phase A takes place. Therefore, the rectifier diode D_1 turns off transferring current to another branch while switches S_3 and S_1 continue conduction. Series resonance initiates between inductance (L_{r1}+ L_{r3}) and equivalent series capacitor, $C_{\mathrm{r,eq}}$ causing sinusoidally varying current through the semiconductor devices and transformer primary branch. Mathematical equations during the resonant period are analyzed using the equivalent circuit shown in Fig. 5.4. The resonance occurs at frequency f_r with characteristics impedance Z_r which are given as,

$$f_r = \frac{1}{2\pi\sqrt{L_{req}C_{req}}} \tag{5.15}$$

$$Z_r = \sqrt{\frac{L_{req}}{C_{req}}} \tag{5.16}$$

$$where \qquad L_{req} = L_{\mathrm{r1}} + L_{\mathrm{r3}} \ \ and \ \ C_{req} = \frac{C_{r1} * C_{r3}}{C_{r1} + C_{r3}}$$

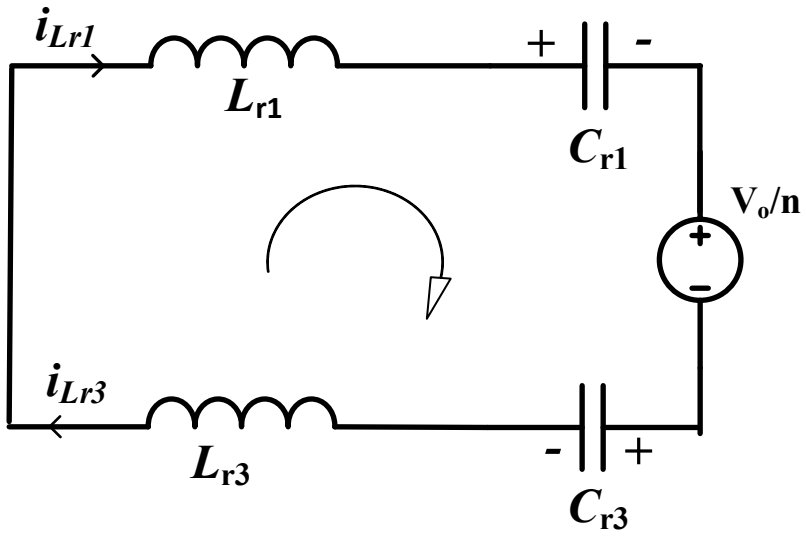


Fig. 5.4. Equivalent circuit during LC resonance period.

Resonant current equations in in phase A, B and C are given below:

$$i_{Lr1}(t) = -\left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_2) \tag{5.17}$$

$$i_{Lr2}(t) = \frac{I_{in}}{3} \tag{5.18}$$

$$i_{Lr3}(t) = \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_2) - \frac{I_{in}}{3} = 0 \tag{5.19}$$

Switch current equations are represented as;

$$i_{S1}(t) = \frac{I_{in}}{3} + \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_2) \tag{5.20}$$

$$i_{S2}(t) = 0 \tag{5.21}$$

$$i_{S3}(t) = \frac{2I_{in}}{3} - \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_2) \tag{5.22}$$

Final values at the end of this interval are:

$$i_{\mathrm{Lr1}}(t_3) = -\frac{I_{in}}{6}, \qquad i_{\mathrm{Lr2}}(t_3) = \frac{I_{in}}{3}, \qquad i_{\mathrm{Lr3}}(t_3) = -\frac{I_{in}}{6} \tag{5.23}$$

$$i_{\mathrm{S1}}(t_3) = \frac{I_{in}}{2}, \qquad i_{\mathrm{S2}}(t_3) = 0, \qquad i_{\mathrm{S3}}(t_3) = \frac{I_{in}}{2} \tag{5.24}$$

With the knowledge of above equations and final values of this interval, the time duration of this interval can be computed as

$$T_{32} = \frac{1}{\omega_r} sin^{-1}\left(\frac{I_{in}Z_r}{6\left(\frac{V_o}{n} + 2V_{crp}\right)}\right) \tag{5.25}$$

Interval 4 (t_3-t_4): (Resonance-pulse continues refer Fig. 5.3(d))

During this interval, the resonance continues with the leakage energy circulating through phase *A* and *C* resonant branch. The switch currents (i_{S1} and i_{S3}) and series resonant inductor current continue to increase and decrease sinusoaidally while switch S_2 remains in blocking mode. Also, the resonant capacitor voltage in phase A, V_{Cr1} starts to decrease due to negative current through L_{r1}. The resonant inductor currents and the switch currents equations describing this interval are given as:

$$i_{Lr1}(t) = -\frac{I_{in}}{6} - \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right)\sin\omega_r\,(t - t_3) \tag{5.26}$$

$$i_{Lr2}(t) = \frac{I_{in}}{3} \tag{5.27}$$

$$i_{Lr3}(t) = -\frac{I_{in}}{6} + \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right)\sin\omega_r\,(t - t_3) \tag{5.28}$$

$$i_{S1}(t) = \frac{I_{in}}{2} + \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right)\sin\omega_r\,(t - t_3) \tag{5.29}$$

$$i_{S2}(t) = 0 \tag{5.30}$$

$$i_{S3}(t) = \frac{I_{in}}{2} - \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right)\sin\omega_r\,(t - t_3) \tag{5.31}$$

Final values at the end of this interval are:

$$i_{\mathrm{Lr1}}(t_4) = -\frac{I_{in}}{3}, \qquad i_{\mathrm{Lr2}}(t_4) = \frac{I_{in}}{3}, \qquad i_{\mathrm{Lr3}}(t_4) = 0 \tag{5.32}$$

$$i_{\mathrm{S1}}(t_4) = \frac{2I_{in}}{3}, \qquad i_{\mathrm{S2}}(t_4) = 0, \qquad i_{\mathrm{S3}}(t_4) = \frac{I_{in}}{3} \tag{5.33}$$

Using above equations and final values of this interval, the time duration can be given as

$$T_{43} = \frac{1}{\omega_r} sin^{-1}\left(\frac{I_{in}Z_r}{6\left(\frac{V_o}{n} + 2V_{crp}\right)}\right) \tag{5.34}$$

Interval 5 (t_4-t_5): (refer Fig.5.3(e))

In this interval, switch current i_{S1} rises sinusoidally in positive direction and reaches I_{in} value whereas resonant current in phase C, i_{Lr3} crosses zero level and increases further in the positive direction. This further allows the switch current i_{S3} to naturally reduce to zero owing to the resonant characteristics. Expressions describing this interval are given as:

$$i_{Lr1}(t) = -\frac{I_{in}}{3} - \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_4) \tag{5.35}$$

$$i_{Lr3}(t) = \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_4) \tag{5.36}$$

$$i_{S1}(t) = \frac{2I_{in}}{3} + \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_4) \tag{5.36}$$

$$i_{S2}(t) = 0 \tag{5.37}$$

$$i_{S3}(t) = \frac{I_{in}}{3} - \left(\frac{V_o/n + 2V_{crp}}{Z_r}\right) sin\,\omega_r\,(t - t_4) \tag{5.38}$$

At the end of this interval, diodes D_1 and D_2 get reverse biased. Final values for this interval are:

$$i_{\mathrm{Lr1}}(t_5) = -\frac{2I_{in}}{3}, \qquad i_{\mathrm{Lr2}}(t_5) = 0, \qquad i_{\mathrm{Lr3}}(t_5) = \frac{I_{in}}{3} \tag{5.39}$$

$$i_{S1}(t_5) = I_{in}, \qquad i_{S2}(t_5) = 0, \qquad i_{S3}(t_5) = 0 \tag{5.40}$$

Utilizing above equations and final values of this interval, the time duration can be given as

$$T_{54} = \frac{1}{\omega_r} sin^{-1}\left(\frac{I_{in}Z_r}{3\left(\frac{V_o}{n} + 2V_{crp}\right)}\right) \tag{5.41}$$

Interval 6 (t_5- t_6): (body-diode conduction interval refer Fig. 5.3(e))

This interval begins with the switch current i_{S3} further crossing zero level in a sinusoidal fashion allowing enough current for the anti-parallel body diode (e.g., Intrinsic diode) to conduct. The internal diode of switch S_3 continues conducting during this interval therefore, the gating signal is forced-off during this time to achieve successful ZCS turn-off condition. To ensure ZCS commutation, the resonant current in phase C, i_{Lr3} must remain above $I_{in}/3$ level during this interval. Therefore, i_{Lr3} reaches its peak value (i_{Lr3_peak}) during this interval, which further allows determining ZCS boundary condition. At the end of this interval i_{S3} again reaches zero and the switch is blocked by a positive voltage across it. Final values for this interval can be summarised as:

$$i_{Lr1}(t_6) = -\frac{2I_{in}}{3}, \qquad i_{Lr2}(t_6) = 0, \qquad i_{Lr3}(t_6) = \frac{I_{in}}{3} \tag{5.39}$$

$$i_{S1}(t_6) = I_{in}, \qquad i_{S2}(t_6) = 0, \qquad i_{S3}(t_6) = 0 \tag{5.40}$$

Time duration for this interval can be given as

$$T_{65} = \frac{1}{\omega_r}(\pi - T_{52}) \tag{5.42}$$

Interval 7 (t_6- t_7): (Transition mode refer Fig. 5.3(f))

This interval begins with the ZCS turn-off of the switch S_3 eliminating overshoot in the device voltage. The device snubber capacitor gets charged instantly and the switch voltage increases linearly owing to the series resonant capacitor charge. After this interval, the charging and discharging of the series resonant capacitors take place in two different phases with constant current flowing through them. Therefore, the total duration of these seven intervals result in one-third of the switching period. Time duration of this interval is given as:

$$T_{76} = T_{10} = \frac{T_s}{3} - T_{61} \tag{5.43}$$

TABLE 5.1: SPECIFICATIONS OF THE PROPOSED CONVERTER

Parameter	Value
Input Voltage, V_{in}	42-48V
Output voltage, V_o	380 V
Maximum output power, P_o	1kW
Switching frequency, f_{sw}	80-150 kHz
Duty ratio, D	0.48-0.55

As a result, the proposed converter analysis repeats after $\frac{T_s}{3}$ interval in the same sequence for the remaining part of the switching cycle.

5.4 Converter Design

This section elaborates the systematic design approach for interconnection of low voltage sources to a high voltage dc bus rated at 380V. Critical design parameters are estimated to ensure uniform output voltage and soft switching against fluctuations in input voltage and load current. Specifications of the converter are decided to interface a solar or storage, with suitable input voltage ranging from 42–48V, to a 380V output across the load rated at 1kW. A design example pertaining to the specifications listed in Table 5.1 is illustrated step by step in this section. Moreover, analytical expressions are derived to determine the values and rating of the components and facilitate their selection.

5.4.1 DC voltage gain

Voltage gain relation helps in determining the desired operating point to regulate 380V at the output under different loading conditions. From Fig. 5.5, the desired operating region of the converter can be achieved with different combination of switching frequency and transformer turn-ratio. Assuming lossless power transfer to the load, voltage gain (M) can be obtained by analysing one of the three phases considering operating symmetry.

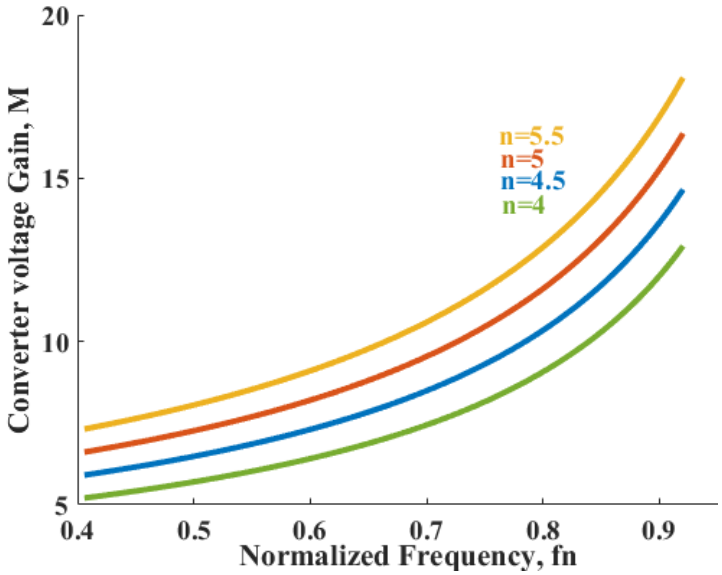


Fig. 5.5. Plot of converter voltage gain with respect to normalized frequency.

$$M = \frac{V_o}{V_{in}} = \frac{n\left(1 - \frac{3Xf_n r_n n(1-k^2)}{\pi}\right)}{\left(\frac{2}{3} - f_n\left(\frac{1}{2} + \frac{M}{r_n X n}\right)\right)} \tag{5.44}$$

where, n: turns ratio of the transformer, $k = \frac{M}{nr_nX}$;

f_n: Normalized frequency, $= \frac{f_{sw}}{f_r}$

r_n: Normalized load resistance, $= \frac{R_{FL}}{n^2 Z_r}$

X: Constant defined as, $= \left(1 + \frac{2nV_{crp}}{V_o}\right)$

where V_o, V_{crp}, and R_{FL} represent output voltage, peak resonant capacitor charge and equivalent full-load resistor, respectively.

As a result, constant output voltage can be assured by varying converter switching frequency for all the possible operating points.

5.4.2 Semiconductor device voltage and current rating

The peak voltage stress across the primary side MOSFETs are influenced by effective charge across series resonant capacitor in different phases and high frequency transformer turns ratio whereas output voltage is reflected across rectifier diodes.

$$V_{sw1-3,rated} = V_{cr\_effective} + \frac{V_o}{2n} \tag{5.45}$$

$$V_{D1-6} = V_o \tag{5.46}$$

Current rating of the semiconductor devices is decided based on the rms current through these components. The approximated expressions for the rms values are given as:

$$I_{sw1-3,rms} = I_{in}\sqrt{\left(\frac{1}{3} - f_n\left(\frac{4}{9} - \frac{1}{2}\left(\frac{nXr_n}{M}\right)^2 + \frac{7}{9}\frac{M}{2nXr_n}\right)\right)} \tag{5.47}$$

$$I_{D1-6,avg} = I_o/3 \tag{5.48}$$

The expressions presented in this section demonstrate that the peak switch voltage has a direct relation with the effective resonant capacitor charge while inverse relation with transformer turns ratio. Therefore, the switch voltage rating should be carefully chosen limiting the conduction losses in the semiconductor switch at low value. The losses occurring in the MOSFETs are predominantly influenced by its intrinsic characteristic parameters mainly on-state resistance, $R_{ds,on}$ and output capacitance, C_{oss}. Hence, selecting a MOSFET with lower $R_{ds,on}$ is conducive for maintaining higher efficiency with reduced conduction losses. Maximum voltage witnessed across the semiconductor device is limited to 220V. Whereas, the ultra-fast SiC diodes with low V_{FD} and low Q_{RR} are preferred for the enhanced converter efficiency. Analytical expressions for the rms current through the semiconductor devices and other components also allow theoretical estimation of conduction losses in the converter.

5.4.3 Selection of HF Transformer Turns Ratio

An ideal value of the transformer turns ratio must provide desired output voltage without aggravating the conduction losses in the converter. As witnessed, transformer turns ratio greatly influences the rms current values and voltage stresses of the semiconductor devices. This implies higher switch voltages due a lower turns ratio. This leads to high rating of the devices having higher ON-state resistance resulting in higher conduction losses. Whereas the transformer with high turns ratio requires larger core area and increased copper, leading to high transformer losses. Consequently, the selection of turn ratio involves a trade-off between

switch voltage rating and conduction losses. Considering efficiency as a prominent factor, lower value of turns ratio is advisable to have lower component ratings with limited conduction losses. For this design example, turns ratio of 5 is chosen.

5.4.4 ZCS boundary condition

The resonant tank energy dictates the soft switching range by providing adequate energy for the body-diode conduction before the switch turn-off. This is possible only if the resonant current peak in all three phases exceeds $I_{in}/3$ value during the switch overlap period. However, the resonant currents in phase A, B and C are inversely related to Z_r that implies higher current stress for lower values of Z_r. Selection of Z_r implicates a compromise between the ZCS operating boundary and the peak current stress. Hence, the maximum value of Z_r can be estimated using the inequality given below:

$$i_{Lr3}(t) > \frac{I_{in}}{3} \quad \Rightarrow \left(\frac{V_o/n + 2V_{crp}}{Z_r} \right) > \frac{I_{in}}{3} \tag{5.49}$$

$$\Rightarrow Z_{rmax} < 3\left(\frac{V_o/n + 2V_{crp}}{I_{in}} \right) \tag{5.50}$$

As a result, a value smaller than Z_{rmax} has been chosen for this design example to be able to drive a current higher than $I_{in}/3$.

5.4.5 Design of the resonant tank parameters

Resonant tank impedance Z_r and resonant frequency f_r, are chosen to maintain ZCS under full-load down to light-load for minimum input voltage through maximum input voltage conditions as indicated in Table 5.1. Step-by-step procedure involved the following steps:

a) Maximum switching frequency is chosen for the lowest gain condition for V_{in} = 48V.

b) Resonant frequency is computed knowing f_n value using (5.44).

c) Select Z_r to restrict peak resonant inductor current and to obtain ZCS over a full range of input voltage and load. In this design example, Z_r is chosen to be 12.8.

d) Lastly, L_r and C_r values for the resonant branch are computed using (5.15) and (5.16). The computed L_r and C_r values are 3.5 μH and 160 nF, respectively.

5.4.6 Duty ratio

As the resonant period dictates the soft-switching boundary, appropriate duty ratio must be chosen to provide necessary overlap between the conduction time of the switches. The amount of the resonant energy stored in the resonant capacitors must be higher than the energy stored in the resonant inductor as indicated in equivalent circuit. Therefore, the resonant pulse must sustain until the semiconductor device turns-off. The desired overlap time ($t_{overlap}$) can be obtained under full-load condition, with maximum switching frequency operation:

$$T_{32} < T_{overlap} < T_{42} \tag{5.51}$$

Or the operating boundary for the duty ratio can be given as.

$$D_{min} < D < D_{max} \tag{5.52}$$

Range of the operating duty ratio can be obtained by using minimum and maximum duty cycle values,

$$D_{min} = 0.33 + \frac{2I_{in}L_r f_{sw}}{3\left(\frac{V_o}{n} + 2V_{crp}\right)} + \frac{f_{sw}}{\pi f_r} sin^{-1}\left(\frac{I_{in}Z_r}{6\left(\frac{V_o}{n} + 2V_{crp}\right)}\right) + \frac{f_{sw}}{2\pi f_r} sin^{-1}\left(\frac{I_{in}Z_r}{3\left(\frac{V_o}{n} + 2V_{crp}\right)}\right) \tag{5.53}$$

$$D_{max} = 0.33 + \frac{2I_{in}L_r\, f_{sw}}{3\left(\frac{V_o}{n} + 2V_{crp}\right)} + \frac{f_{sw}}{2\pi f_r} \sin^{-1}\left(\frac{I_{in}Z_r}{6\left(\frac{V_o}{n} + 2V_{crp}\right)}\right) + \frac{f_{sw}}{2\pi f_r} sin^{-1}\left(\frac{I_{in}Z_r}{3\left(\frac{V_o}{n} + 2V_{crp}\right)}\right) + \frac{f_{sw}}{2f_r} \tag{5.54}$$

Therefore, to ensure ZCS for the entire range of source voltage and load, a duty ratio must lie within this range.

5.4.7 Boost Inductor calculation

In the proposed three-phase configuration, the three interleaved inductors are utilized at the input side. Each inductor carries 1/3rd of the total source current. Therefore, for a 1kW rated power and input voltage of 42V, a maximum current through each inductor is 8A. Hence, for a permissible current ripple of 0.5A, input inductor value is calculated as 200µH.

TABLE 5.2: DESIGN PARAMETERS

Parameter	Value
Resonant Inductor, $L_{r1\text{-}3}$	3.5μH
Resonant Capacitor, $C_{r1\text{-}3}$	160nF
Input Inductor, L_1 L_2 L_3	200μH
Output Capacitor, C_o	100μF
Turns ratio, n	5

5.5 Simulation and Experimental Results

This section validates the proposed theory through detailed results obtained from the simulation performed in PSIM 11.0. Further, operation and analysis of the developed proof-of-concept laboratory hardware prototype is tested to obtain experimental results followed by a detailed discussion on the experimental efficiency. The goal of this Section is to justify the advantages of adopting the proposed converter for low voltage high current applications. The operating principle and theoretical steady state waveforms of the converter are validated in this section.

5.5.1 Simulation Results

Following the design procedure given in Section 5.4 and utilizing converter specifications in Table 5.1, the calculated converter parameters are obtained as listed in Table 5.2. This section exemplifies the steady-state simulation waveforms obtained from PSIM 11.0.1 software to validate the proposed claims. The proposed three-phase current sharing topology has been examined for the source voltage range of 42V- 48V with load variation from 100% down to 20%. It has been witnessed that the simulation results follow the theoretical analysis and the design equations.

Fig. 5.6 depicts 120° phase shifted boost inductor current waveforms in current sharing three-leg primary with equally sharing the total source current. The waveforms demonstrate nearly constant current from the source supporting reduced filter requirement owing to the ripple frequency (3*f_{sw}). Fig. 5.7 highlights the steady-state simulation waveforms for the series resonant current in phase A, B and C with V_{in}= 42V at full-load (1000W). ZCS operation

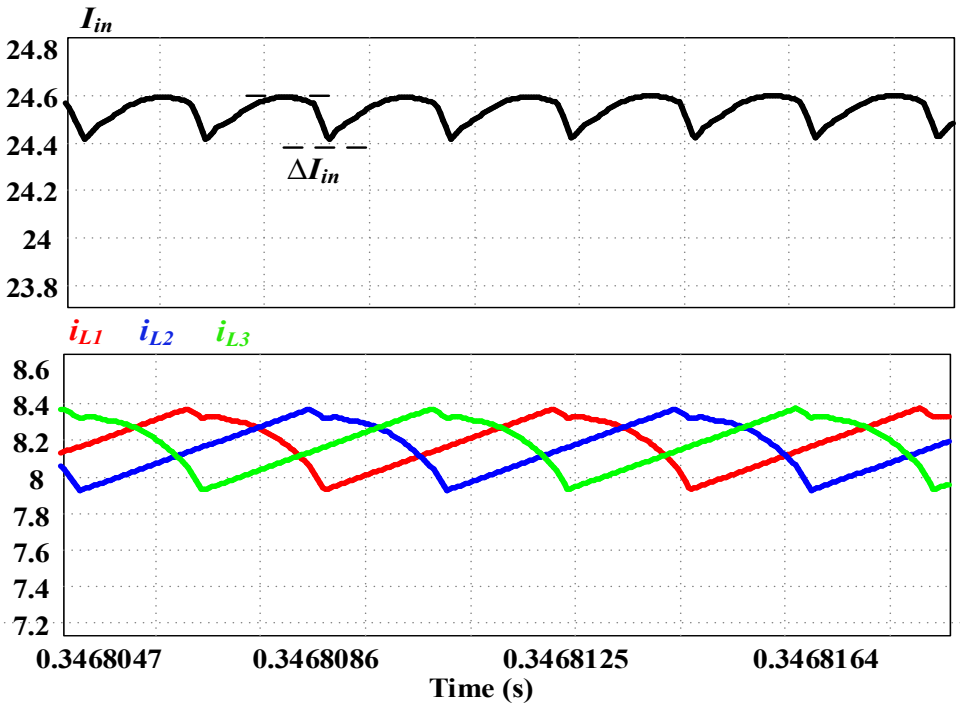


Fig. 5.6. Steady-state waveforms for Vin=42V at full-load (1000W) with input current I_{in} and boost inductor currents i_{L1}, i_{L2}, i_{L3}.

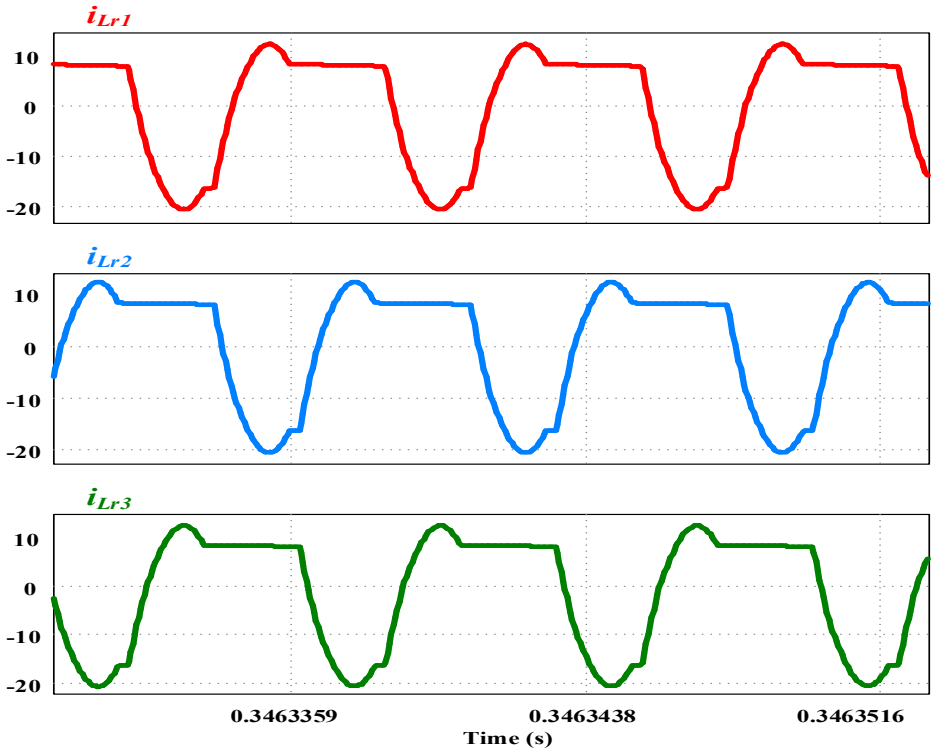
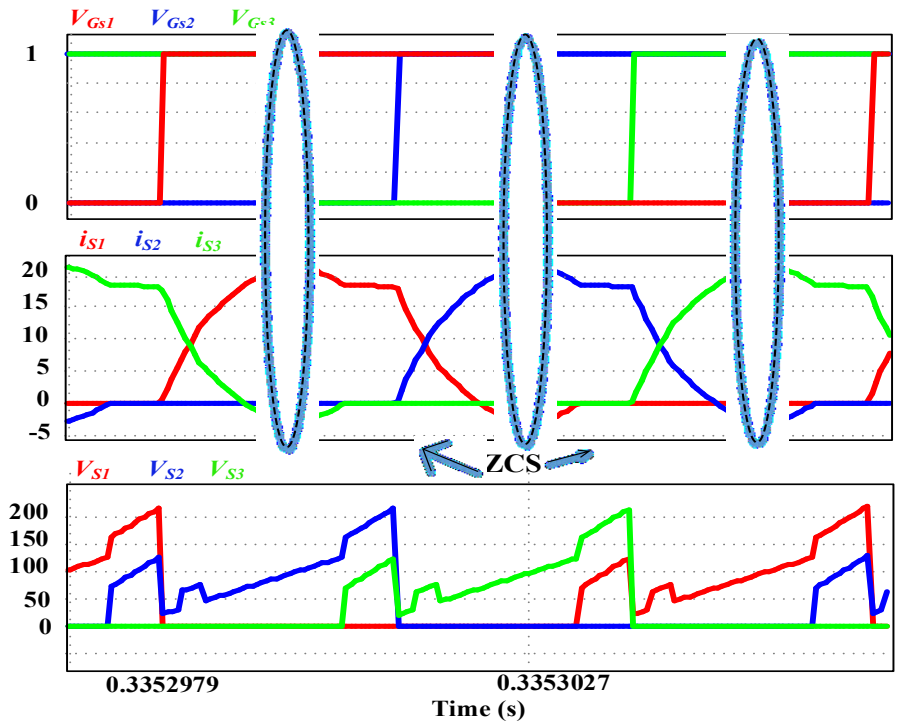
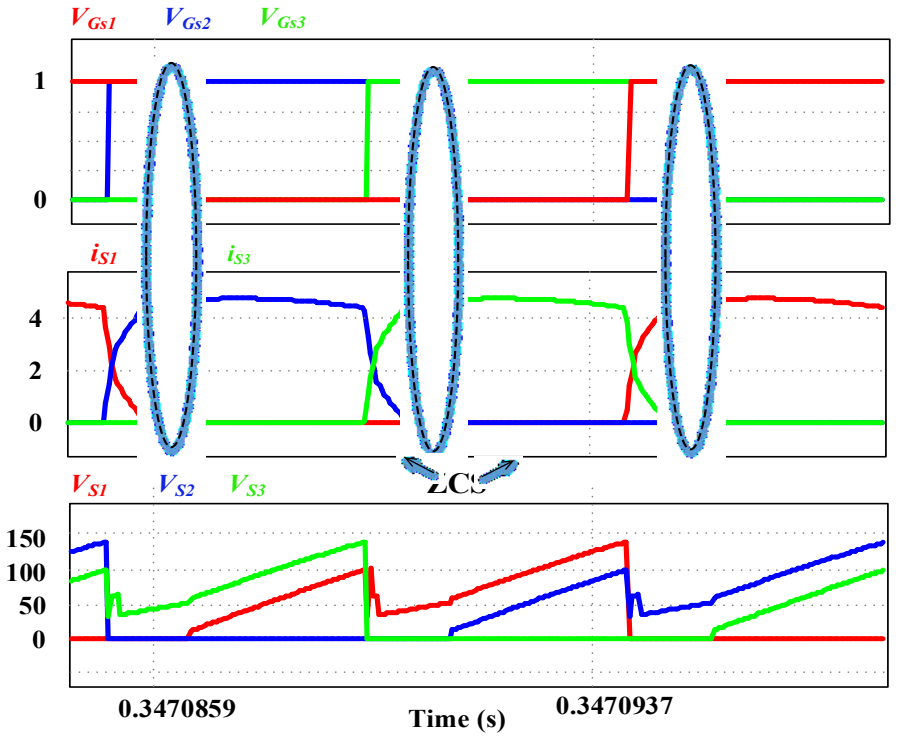


Fig. 5.7. Steady-state waveforms for V_{in}= 42V at full-load (1000W) depicting series resonant current through phase A, B and C.

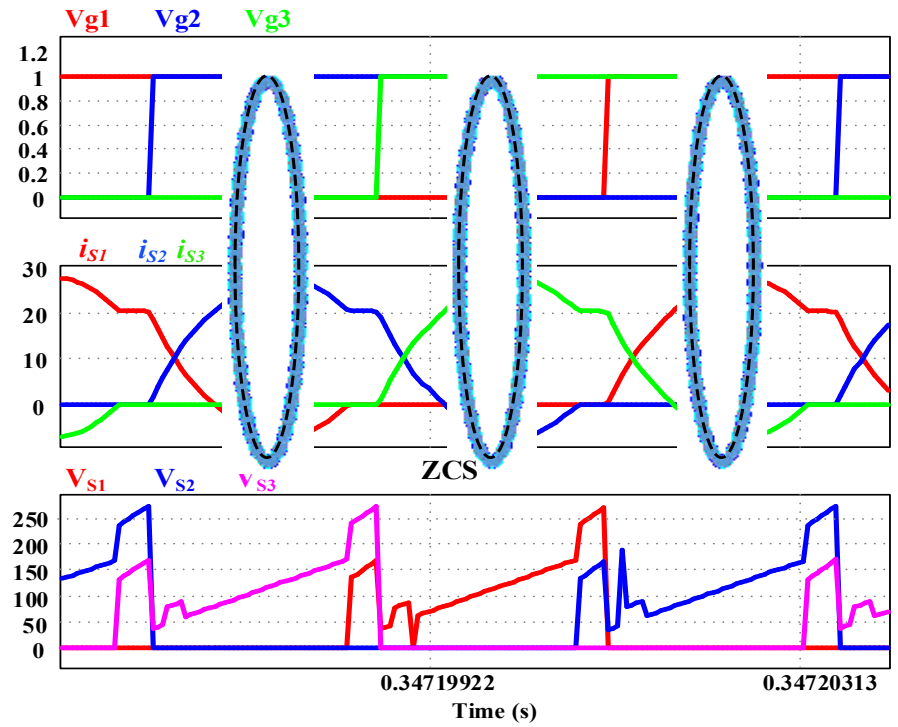


(a)

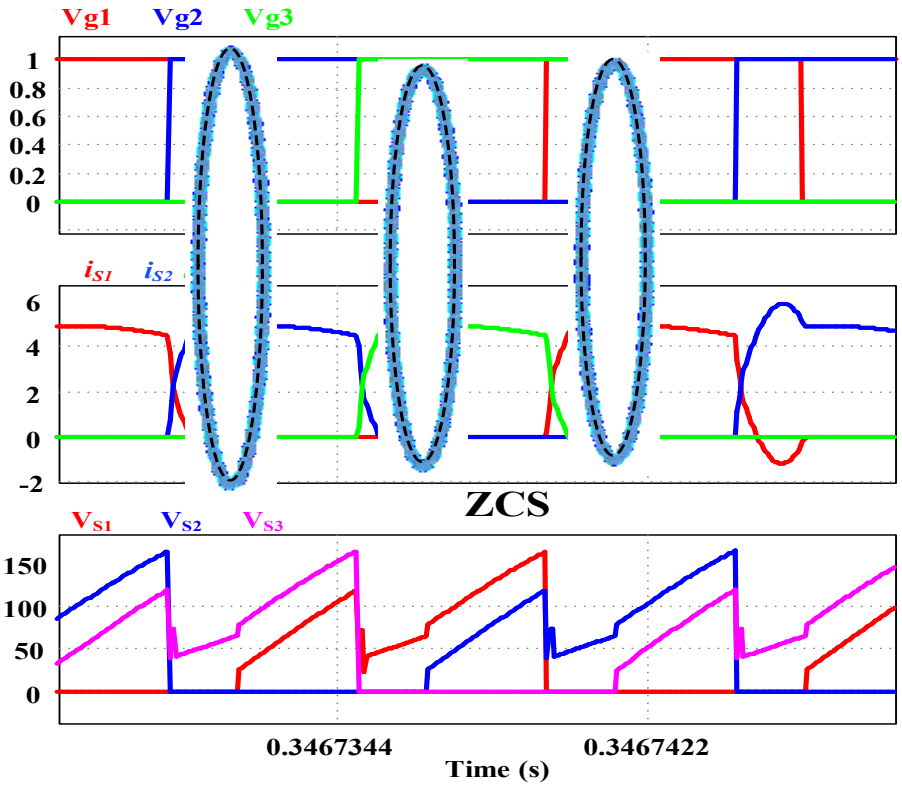


(b)

Fig. 5.8. Simulation results for V_{in} = 42V (a) at full-load (1kW) (b) at light-load (200W).



(a)



(b)

Fig. 5.9. Steady-state simulation results for V_{in} = 48V (a) at full-load (1kW) (b) at light-load (200W).

at turn-off instant is highlighted for the full-load and the light-load conditions in Fig. 5.8(a) and 5.8(b), respectively. Steady-state results at 1kW power operate with 150kHz switching frequency for V_{in} = 42V. It should be witnessed that the transition of the semiconductor devices occurs during gating overlap of the two switches. Series resonance-pulse is implemented that allows natural current transfer from an outgoing switch to the incoming switch within a short time. The sinusoidal characteristic during this resonance period, naturally reduces the switch current to zero followed by its body diode conduction. Therefore, the gating is removed during this time, avoiding switch voltage overshoot together with ZCS turn-off of the device. Constant current is witnessed with only single switch conduction and therefore, contributes to the power transfer region. This constant current region allows linearly increasing switch voltage due to the series capacitor in the respective resonant branch. The switch turn-off instant is highlighted with zero voltage across the switch, confirming body-diode conduction. Steady-state simulation results for 200W power operating with 90kHz switching frequency at V_{in} = 42V are exemplified in Fig. 5.8(b). In Fig. 5.8(b), successful ZCS at switch turn-off and clamped voltage across the primary MOSFET under light load condition is perceived. Lower $I_{Lrp}/(I_{in}/3)$ ratio at light load prove the load-dependent resonant energy.

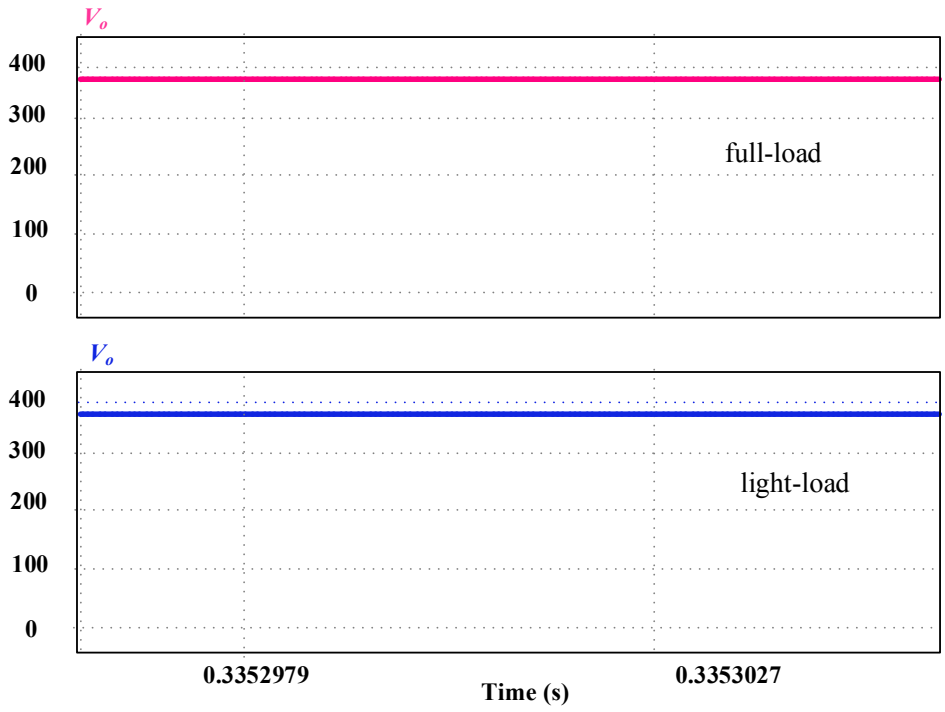


Fig. 5.10. Experimental results for voltage across and current through the rectifier diode for V_{in} = 42V (a) full-load (1kW) and (b) light-load (200W) condition.

This causes significantly low leakage energy resulting in higher light-load efficiency. Also, lower switch voltages are observed for the loads below rated power.

The claims hold true for the simulation results with V_{in} = 48V at different loading condition as depicted in Fig. 5.9. However, slightly higher switch current peaks are observed for higher source voltage. Regulated voltage of 380V is maintained across the load for the varying load conditions as shown in Fig 5.10. It is clear that in the proposed converter, wide range ZCS and device voltage clamping is preserved from full-load condition to light-load (200W) condition for set variation in source voltage with overall switching frequency range of 80-150kHz. It is also witnessed that the change in switching frequency is more profound with respect to the load fluctuations as opposed to the source voltage variations. In this case, the frequency range observed for 42V-48V input is 135 kHz–150 kHz at full-load condition. Therefore, the proposed converter is suitable to incorporate alternative energy sources with large variation in their output voltage.

5.5.2 Experimental Results

This section exhibits comprehensive steady-state results obtained from the proof-of-concept laboratory hardware prototype rated at 1kW as shown in Fig. 5.11 to verify the soft turn-off with ZCS and device voltage clamping. Table 5.2 and Table 5.3 list the converter parameter values and component's details used for the development of the hardware prototype, respectively. The proposed three-phase topology is modelled to achieve the set goals and the experimental results are analysed for various factors like efficiency, loss distribution and volume. Experimental analysis has been done for the source voltage range of 42V- 48V with load variation from full-load down to 20% load.

The proposed dc-dc converter allows conversion from low voltage into 380V dc with a variable voltage-gain capability. The converter employs high-speed MOSFETs with inherent reverse-blocking capability; SiC Schottky diodes for output diode bridge to avail minimum reverse recovery loss; three single-phase high-frequency transformers in star connection with 1:5 turns ratio are realized using high-permeability ferrite E-cores and litz wire thereby limiting core loss, and temperature rise. Open loop control is executed using a TMS320F28335 digital signal processor providing 120° phase-shifted gating signals. The experimental readings are taken on Yogogawa digital storage oscilloscope.

TABLE 5.3: COMPONENT SPECIFICATIONS OF THE LABORATORY PROTOTYPE

Component	**Specifications**
Boost inductors L_1, L_2, L_3	55 x 28 x 21 EE ferrite Core, 200μH
Primary Switches, S_1, S_2, S_3	SCT3060ALGC11 (650V, 39A,60mΩ)
Resonant Inductor, L_{r1-3}	EE ferrite core, 1.48μH
Resonant Capacitors, C_{r1-3}	160nF 1kV Film capacitor
3 Single phase HF Transformer	EE ferrite core, Primary turns, N_1=10, secondary turns N_2=50, L_{lk}= 1.64μH
Secondary Side Rectifier Diodes D_{1-6}	STPSC20065D (650V, 20A)
Output Capacitor, C_o	80μF 450V electrolytic capacitor, 10nF film capacitor
Gate driver IC	HCNW3120
Digital Controller	TMS230F28335 (Texas Instruments starter Kit)

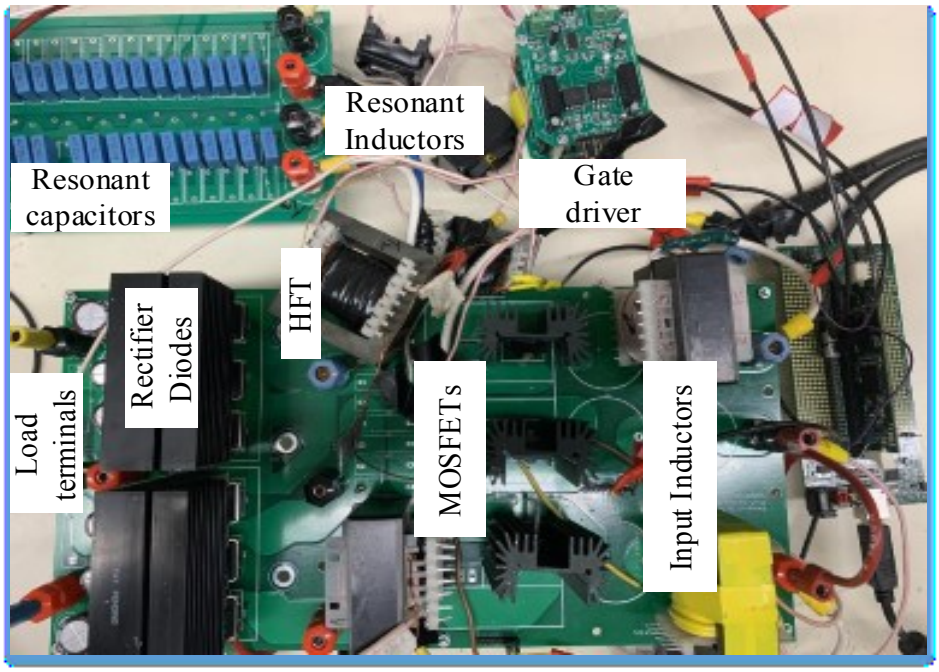


Fig. 5.11. Experimental prototype of the proposed converter.

Fig. 5.12(a) shows the measured input current I_{in} and three boost inductors current $I_{L1,}$ $I_{L2,}$ I_{L3} with V_{in} = 42V at full-load condition. It is highlighted in Fig. 5.12(a) that interleaving legs with 120◦ phase shifted currents improve the quality of input current as the current ripple remains reasonably low having ripple frequency 3*f_{sw}. Moreover, the interleaved legs reduce the component's stress and increase the power handling capacity of the converter. Fig. 5.12(b) depicts the series resonant current in phase A, phase B and phase C which are shifted by 120◦. Fig. 5.12(c) demonstrates smooth current commutation with ZCS of switch S_2 during the overlap duration. The gating signal for the targeted switch is removed once the current through it becomes zero, and consequently, the switch voltage (V_{ds2}) linearly ramps up to V_o/n. Successful ZCS operation was possible due to the sinusoidally varying transformer current, which eventually resulted in sinusoidal current through the switch ensuring body diode conduction before the switch turn-off instant. Moreover, during the overlap period the switch voltage drops to a lower value due to simultaneous charging/discharging of the series resonant capacitor in the two branches. In addition, the resonant current higher than I_{in}/3 mark appears during this overlap time ($t_{overlap}$ ≈ 1.16μs), allowing antiparallel body diode conduction and effective ZCS turn-off as shown in Fig. 5.12(c). It can also be noted that the peak switch voltages are limited at ≈220V and a resonant peak of 11.5A flows through each phase for nominal converter voltage of 42V. Similarly, the ZCS operation of the other two switches occur 120◦ and 240° after the targeted switch S_2 is turned off. Therefore, overvoltage spike in the switch voltage is prevented, avoiding any axillary clamping circuit or snubber requirement.

Fig. 5.13(a) and 5.13(b) highlight the current profiles at the input side along with 120° shifted boost inductors at V_{in} = 42V for light-load condition. Fig. 5.13(c) illustrates the zero current commutation and voltage spike elimination of the semiconductor switches for 200W power (light-load) with V_{in} = 42V and switching frequency 90kHz. Relatively lower switch voltages are witnessed for the partial load condition due to the lower resonant capacitor charge and low input current. Moreover, owing to the load adaptive series resonant energy, reasonably low $I_{Lrp}/(I_{in}/3)$ ratio is observed at light load condition leading to improved light-load efficiency.

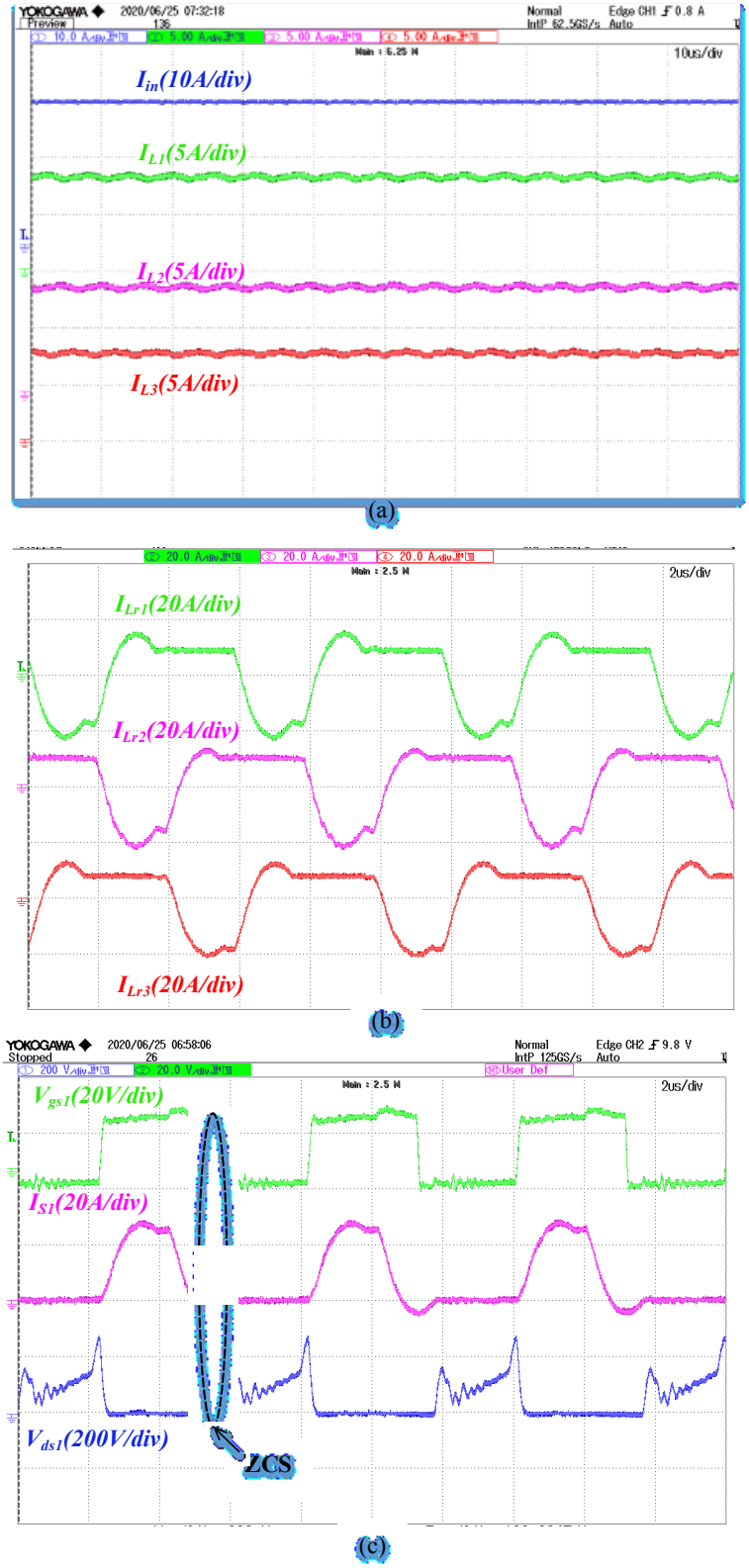


Fig. 5.12. Experimental steady-state waveforms for Vin=42V at full-load (1000W) (a) Input current I_{in}, boost inductor currents I_{L1}, I_{L2}, I_{L3} (time scale: 10μs/div) (b) series resonant current through phase A, B and C I_{Lr1}, I_{Lr2}, I_{Lr3} and (c) Gate-source voltage V_{GS1}, switch current I_{Sw1}, and drain-to-source voltage V_{ds1} (time scale: 2μs/div).

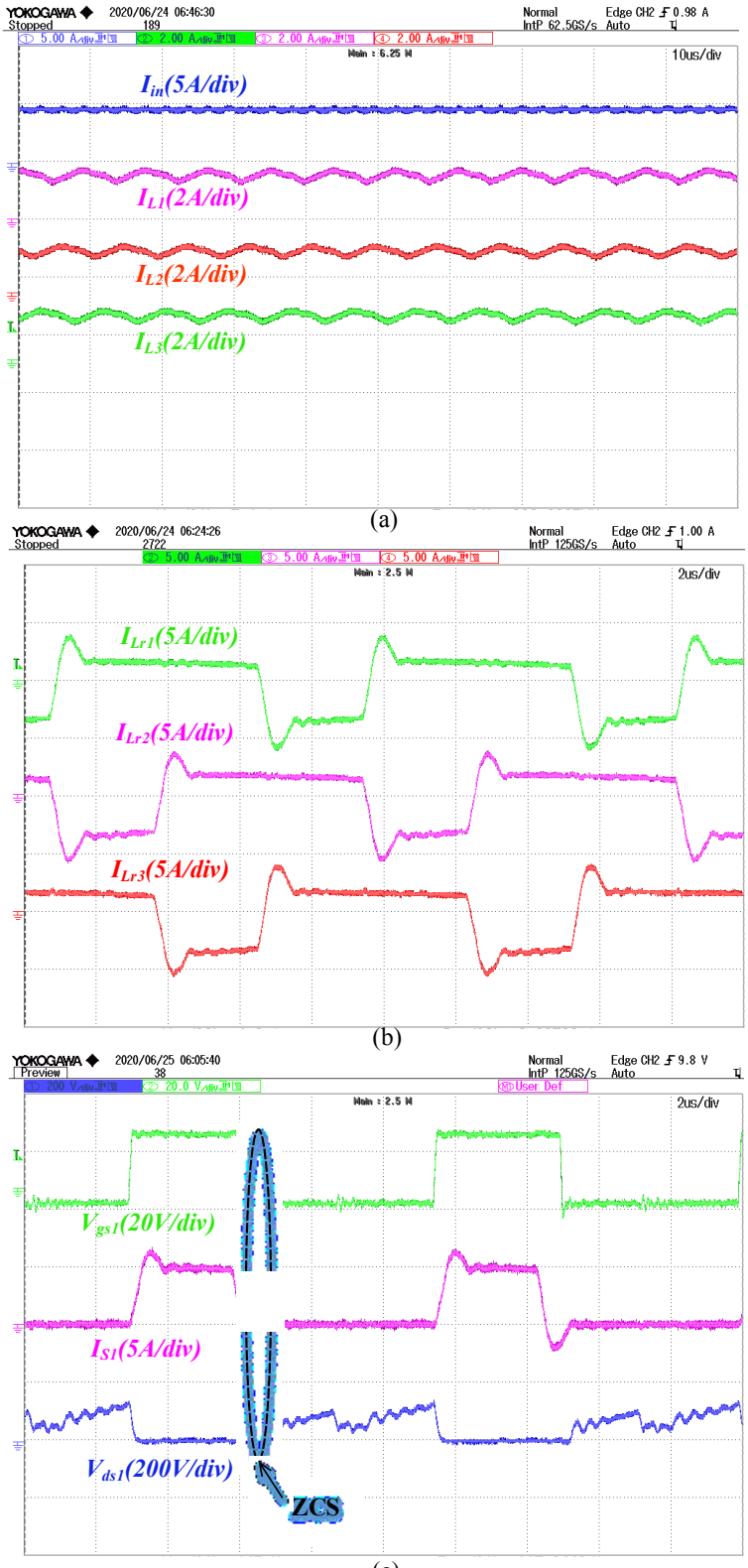
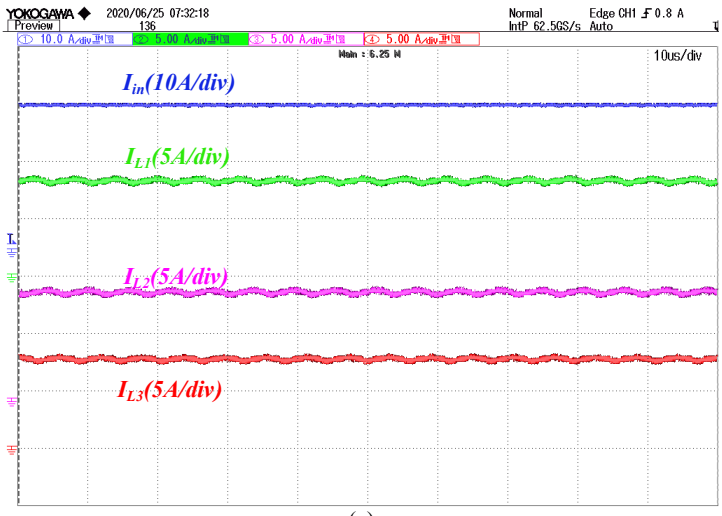
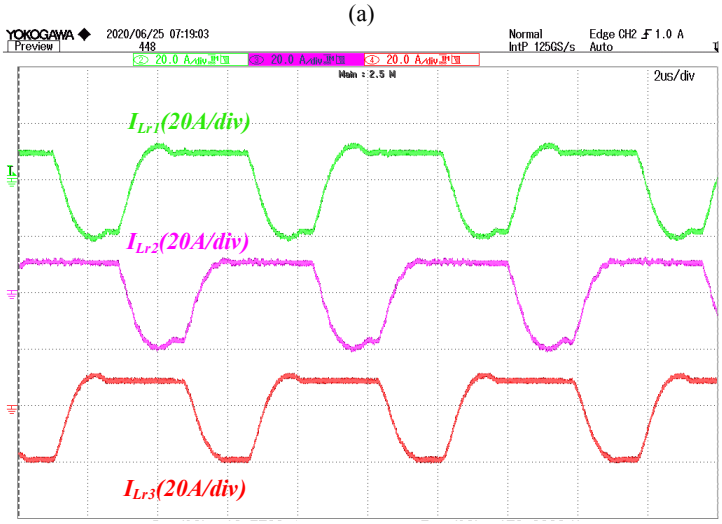


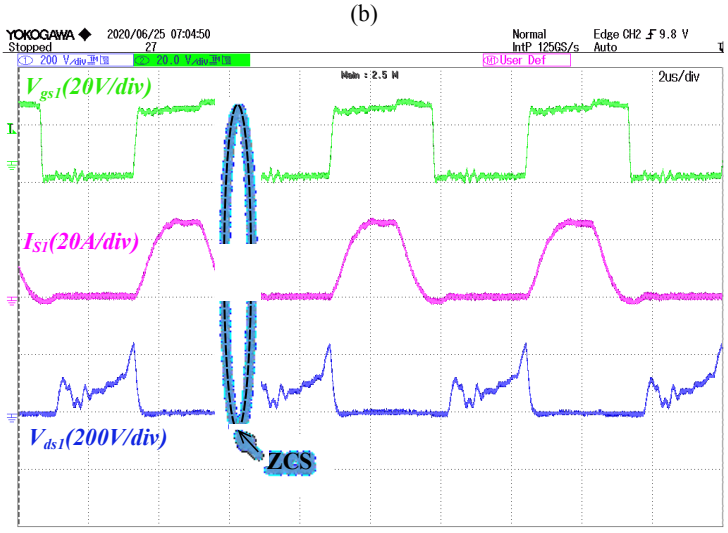
Fig. 5.13. Experimental steady-state waveforms for Vin= 42V at light-load (200W) (a) Input current I_{in}, boost inductor currents I_{L1}, I_{L2}, I_{L3} (time scale: 10μs/div) (b) series resonant current through phase A, B and C I_{Lr1}, I_{Lr2}, I_{Lr3} and (c) Gate-source voltage V_{GS1}, switch current I_{Sw1}, and drain-to-source voltage V_{ds1} (time scale: 2μs/div).



(a)



(b)



(c)

Fig. 5.14. Experimental steady-state waveforms for Vin=48V at full-load (1000W) (a) Input current I_{in}, boost inductor currents I_{L1}, I_{L2}, I_{L3} (time scale: 10μs/div) (b) series resonant current through phase A, B and C I_{Lr1}, I_{Lr2}, I_{Lr3} and (c) Gate-source voltage V_{GS1}, switch current I_{Sw1}, and drain-to-source voltage V_{ds1} (time scale: 2μs/div).

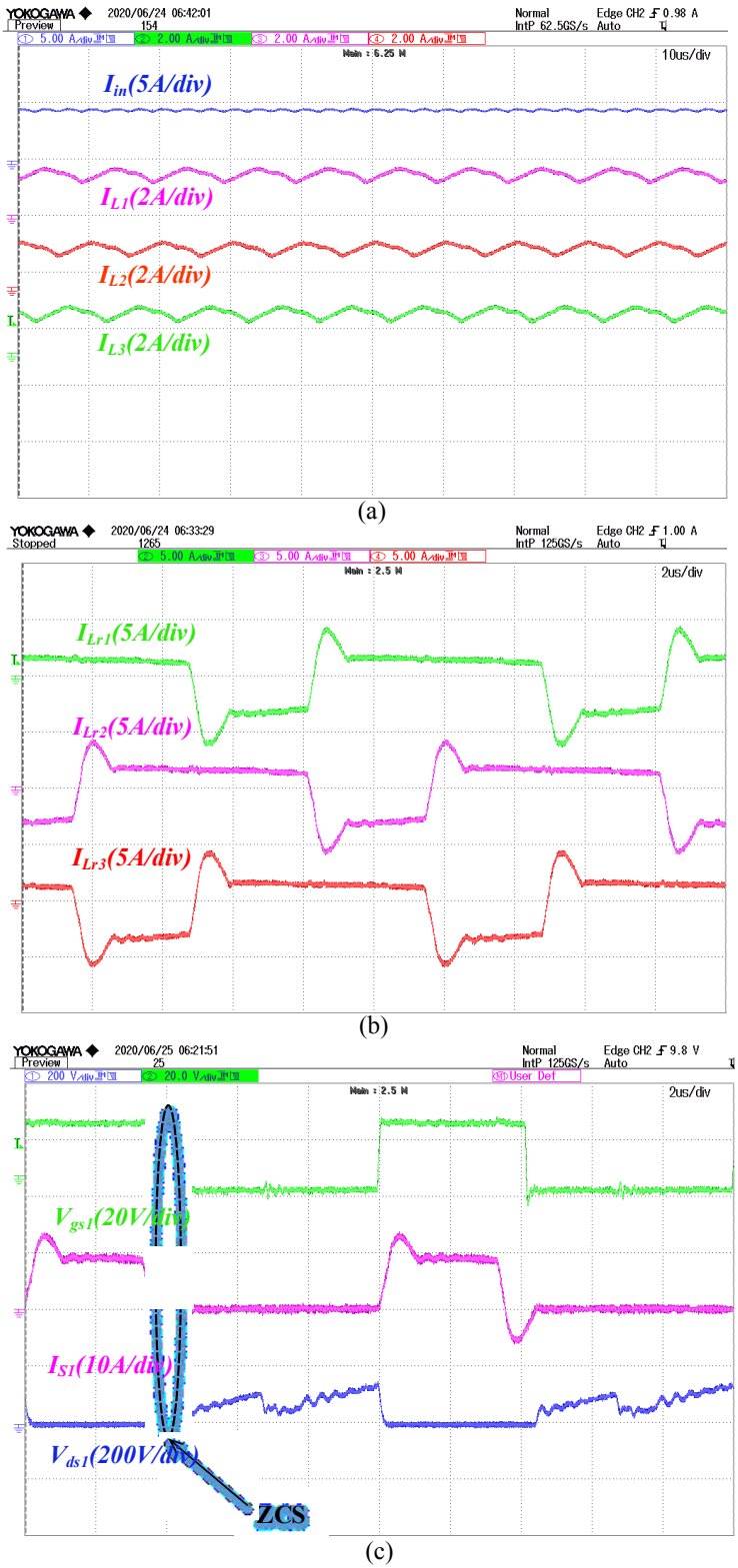
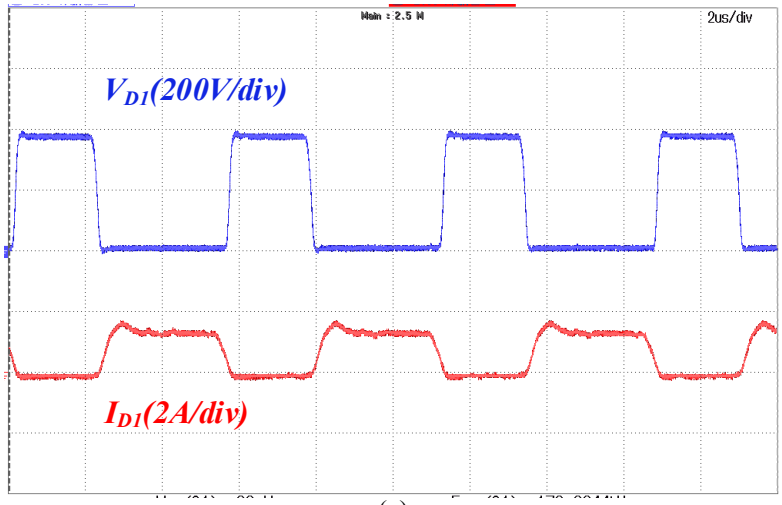
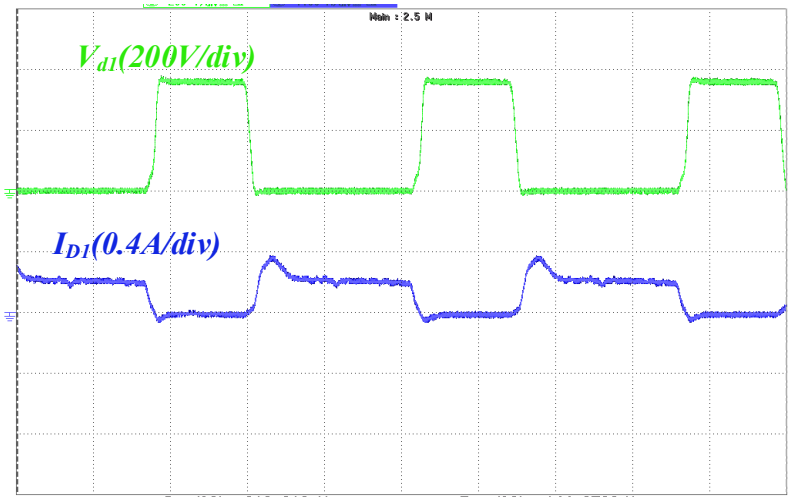


Fig. 5.15. Experimental steady-state waveforms for Vin= 48V at light-load (200W) (a) Input current I_{in}, boost inductor currents I_{L1}, I_{L2}, I_{L3} (time scale: 10μs/div) (b) series resonant current through phase A, B and C I_{Lr1}, I_{Lr2}, I_{Lr3} and (c) Gate-source voltage V_{GS1}, switch current I_{Sw1}, and drain-to-source voltage V_{ds1} (time scale: 2μs/div).

The experimentation is also performed with 48V source voltage at full-load and light-load condition to comply with the variable voltage source and load conditions in Fig. 5.14 and Fig. 5.15, respectively. The proposed claims hold true under these conditions as well confirming wide range ZCS. However, slightly higher peaks in switch current and higher $I_{Lrp}/(I_{in}/3)$ ratio are observed at higher source voltage. Moreover, a swell in in resonant capacitor voltage and switch voltage is observed for 48V input. The output rectifier diodes turn-off with zero current is shown in Fig. 5.16 and therefore, reverse recovery loss and voltage ringing can be avoided, further eliminating the need for the passive snubbers across the transformer secondary.



(a)



(b)

Fig. 5.16. Experimental results for voltage across and current through the rectifier diode for V_{in} = 42V (a) full-load (1kW) and (b) light-load (200W) condition.

The experimental results demonstrate wide range ZCS and device voltage clamping encompassing full-load to light-load operation. It should also be noticed that the circulating energy at rated load is limited by the proposed converter design resulting in reduced losses. Bringing down the current stress due to the interleaved legs across the source along with the ZCS turn-off and reduced semiconductor count, overall efficiency can be improved significantly making the converter well suited for the low voltage high current applications.

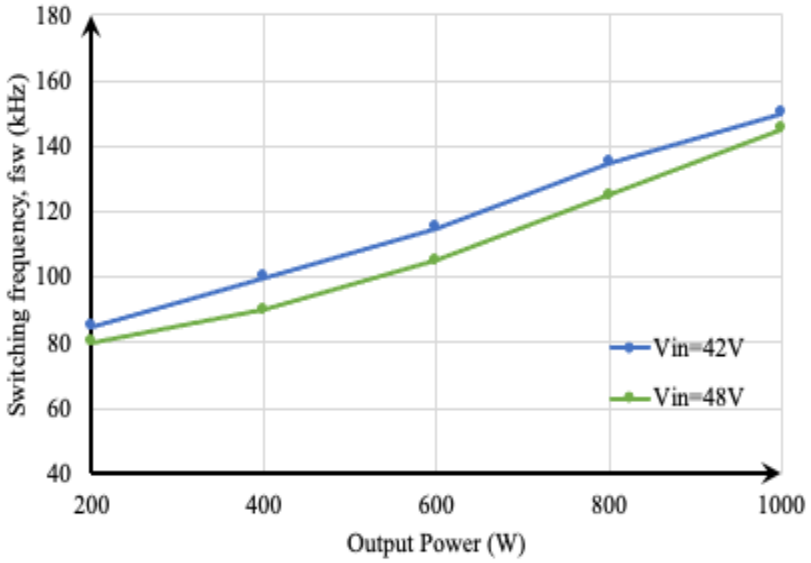


Fig. 5.17. Switching frequency graph with output power variation.

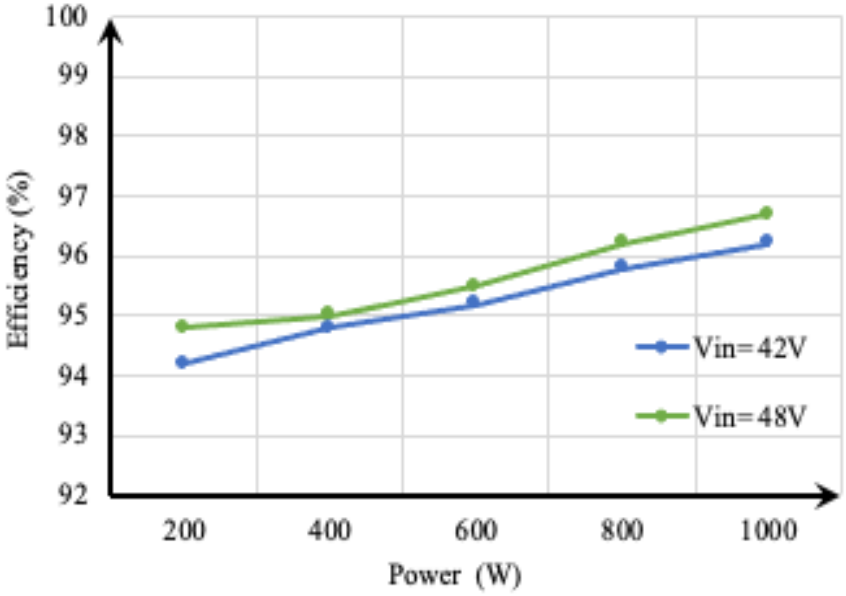


Fig. 5.18. Experimental efficiency trend with output power variation.

Fig. 5.17 depicts practical switching frequency range of 85-150kHz for the wide range of load and source, thereby allowing HF magnetics and reduced filter requirement. However, a major fluctuation in switching frequency is witnessed for the load variations compared to the source voltage variations, which makes the converter more suitable for sources with wide input range. It can be inferred that the change in f_{sw} is not very substantial for the input voltage variations. Hence, the variable frequency operation is indispensable to maintain regulated voltage, i.e $V_o \approx 380V$ across the load terminals under different scenarios.

The findings in Fig. 5.18 elucidate the experimental efficiency trend for the load variation at the boundary of input voltage range. The recorded peak efficiency is 96.7%, which is above par with the state-of-the-art dc-dc power conversion topologies. Also, the experimental efficiency under light-load is recorded to be 94.5%. Fig. 5.19 depicts the converter power loss distribution for the different load condition at nominal input voltage. From the curve, it should be inferred that the majority of the losses occur in the semiconductor devices and the boost inductors. The converter efficiency can be enhanced greatly by optimizing the component's selection, gate drive circuit and the printed circuit board. Experimental results validate the accuracy of the analysis and proves the feasibility of the proposed converter for high voltage gain high current dc-dc power conversion applications.

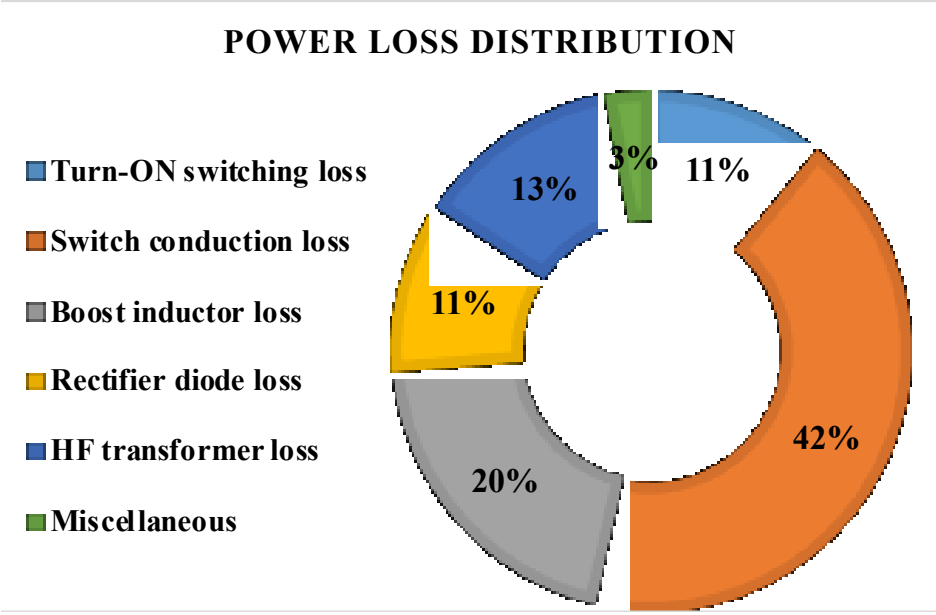


Fig. 5.19. Loss distribution in the proposed converter.

5.6 Conclusion

In this Chapter, a novel series resonant-pulse assisted current-fed three-phase interleaved configuration has been proposed. Interleaving legs at the primary prevent high current stress through the devices leading to low thermal requirement. Series resonance-pulse provides wide range ZCS operation and eliminates turn-off voltage spike, which has been a major drawback in traditional current-fed power converters, thereby avoiding the external snubbing requirement. Moreover, the proposed converter exploits load adaptive resonant energy to bring the circulating and peak current down compared to the traditional resonant converters.

Detailed operation, ccomprehensive steady-state analysis, and design procedure has been reported. With merits such as high voltage gain, low ripple source current, reduced passive/active component count and modular high-frequency isolation, the proposed converter is a promising candidate for interfacing unidirectional sources like fuel cells, solar panel and energy storage to utility grid at medium-to-high power levels. The merits and detailed operation are confirmed with simulation and experimental results.

Further, the proposed resonant-pulse based ZCS soft-switching can be conceptualized and investigated for the three-phase modular converter owing to the benefits of simple inductor, high reliability, and easy implementation for the high power applications.

CHAPTER 6:

CONCLUSIONS AND FUTURE WORK

This Chapter concludes the thesis and highlights the research contributions of the thesis in Section 6.1. Recommendations and brief description for the future scope of research has been discussed in Section 6.2.

6.1 Conclusion and Thesis Contributions

Isolated dc-dc converters are the key power electronics interface between low voltage alternative energy sources such as solar/fuel cell and high voltage dc microgrid. Wide operating range is crucial in these converters to extract maximum power from these sources with inherent variability. Selection and design of a dc-dc power converter with desired attributes is imperative to achieve high efficiency and high performance for applications such as data center and UPS, solar/fuel-cell based utility interactive inverters, and dc microgrid.

This thesis focuses on high frequency soft-switching converters for low cost, high-density, and light-weight system. Current-fed converters owing to their obvious merits like high voltage conversion ratio, low ripple input current, short-circuit protection, etc. are the potential candidate for low voltage high current specifications. Soft-switching in these converters resolve device turn-off voltage spike issue and allows safe operation at high frequency leading to compact and light-weight system. Several soft-switching techniques for current-fed topologies reported in the literature exhibit limitations such as limited soft-switching range, high peak and circulating current, increased circuit complexity, and compromised boost capacity that significantly hamper the conversion efficiency and cost. However, a quasi-resonant approach with parallel LC circuit reported in the literature was seen as a plausible solution for applications with wide load variation due to narrow switching frequency range.

Therefore, the primary objective of this thesis is to address the limitations in existing soft-switching converters and introduce a new soft-switching approach. The thesis contributes to the operation, analysis, design and development of a novel series resonant-pulse assisted soft-switching method for all potential current-fed converter topologies, to attain wide soft-switching operation of the switching device with voltage clamping. The idea exploits resonance-pulse generated through series LC resonant tank during overlap conduction time to

achieve Zero-current-switching (ZCS) of the semiconductor devices allowing natural reduction of the device current to zero. Contribution of each Chapter is summarized as follows:

In Chapter 2, the new series resonant tank based resonance-pulse commutation is studied and explained which utilizes load adaptive resonant energy to bring soft-switching of the semiconductor devices with significantly low circulating energy. At first, the proposed series resonant-pulse is implemented using transformer leakage inductance and an additional small HF series capacitor in an isolated single-phase current-fed push-pull topology. Detailed analysis and design of this topology has been reported. Constant-on time variable frequency modulation is implemented for load voltage regulation. Steady-state operation of the proposed converter is validated through simulations and experiments to demonstrate accomplishment of wide range ZCS and voltage clamping of the devices for load current and source voltage variations. The highlights of the proposed converter are small size, high efficiency and simpler gate control requirement with fewer components.

In Chapter 3, series resonant-pulse concept in current-fed half-bridge topology is analyzed and steady-state operation is explained. Successful ZCS operation and voltage clamping of the switching device for wide variations in load and source profile, validate the effectiveness of the proposed converter topology. Owing to the features like high voltage conversion ratio, simple structure, reduced current/voltage stress, reduced transformer kVA, and easy implementation, this converter is proved superior to the push-pull configuration presented in Chapter 2. The proposed converter operation and design is validated through experimental results obtained from the laboratory prototype rated at 500W and reported a peak efficiency of 97.2%.

In Chapter 4, the modular series resonance-pulse assisted current-fed full bridge converter is conceptualized for relatively high power microgrid applications. Load adaptive resonance-pulse due to series LC resonant circuit remains the fundamental for achieving wide range ZCS operation and voltage clamping of the devices while allowing reduced circulating current in the converter. In addition to these advantages, modularity of the proposed converter allows easy scalability and simple implementation, demonstrating high efficiency. Steady-state analysis and design have been verified through simulation and experimental results. The

novelty of the proposed soft-switching method is also demonstrated by comparing it with state-of-the-art soft-switching converters.

In Chapter 5, the concept of load adaptive series resonant-pulse has been extended to current-fed three-phase circuit to achieve better performance for high power applications. The converter comprehends zero-current turn-off and natural clamping of the switching devices and negligible diode reverse recovery loss. The three-inductor current sharing configuration at the input allows reduced input and output filtering requirements owing to $3x f_s$ ripple frequency. The key highlights of the proposed converter include reduced control burden owing to semiconductor devices having common source with supply, small filter size, ZCS operation and natural voltage clamping of the semiconductor devices for wide variation in load current and source voltage. Detailed steady-state analysis and converter design for the proposed three-phase topology have been reported and validated through experimental results on 1 kW prototype.

In addition to the above contributions, the following conclusions which are common to all the proposed topologies are abridged as follow:

- New soft-switching concept with load adaptive resonant feature is proposed and analyzed for the current-fed topologies to naturally commutate the semiconductor devices and clamp the voltage spikes.
- All semiconductor switches of the proposed current-fed topologies are operated with ZCS turn-off and clamps the voltage across the semiconductor devices with negligible reverse recovery losses in rectifier diodes.
- Relatively lower peak and circulating current are observed in all the proposed topologies leading to minimal conduction losses.
- The converters output voltage is regulated at 380V with a switching frequency modulation.
- Relatively low current/voltage stress compared to the parallel LC tank based soft-switching concept in the same topologies result in highly efficient, power-dense and cost-effective design.
- All the proposed converters exhibit high efficiency greater than 95 % for rated output power from the developed laboratory hardware proof-of-concept prototypes.

- Theses topologies eliminate the need of additional snubber or active clamping circuit to snub the voltage spikes at turn-off.

6.2 Future Scope of Research

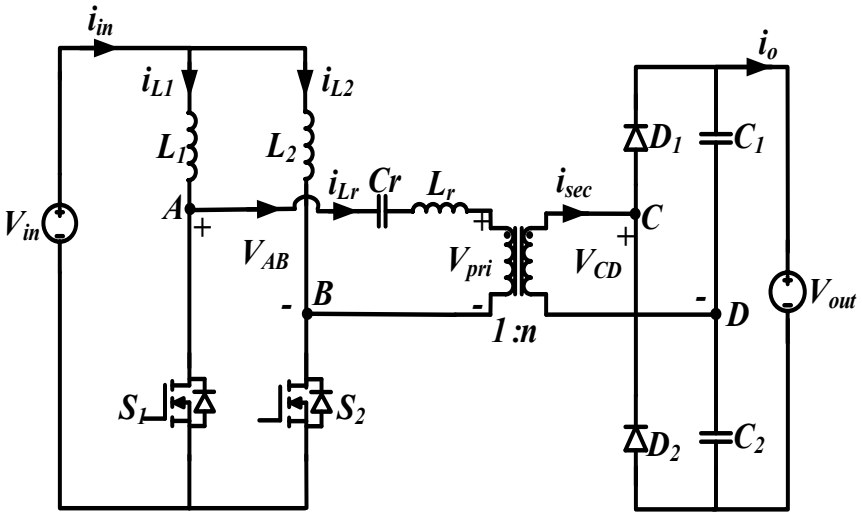
Based on the research accomplishments and outcomes of this thesis, the recommendations for further research are given as follows:

6.2.1 *Small-signal modelling and closed loop control implementation of series resonance-pulse current-fed half-bridge dc-dc converter*

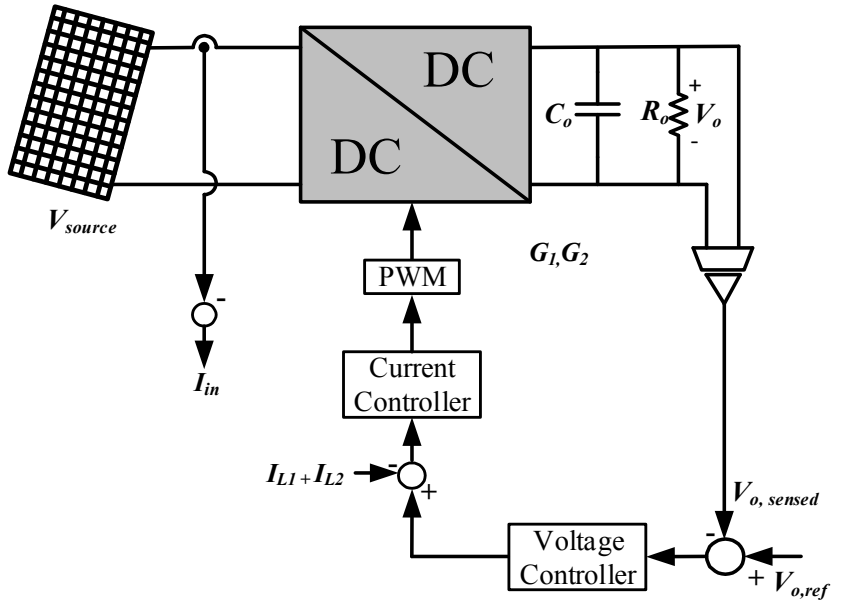
Unregulated characteristics, and discontinuous nature of alternative energy sources, demands for the efficient closed loop control to provide stable operation and regulated power flow. This thesis is focused on detailed steady-state operation and analysis of a series resonance-pulse based current-fed half-bridge converter proposed earlier in Chapter 3. However small signal modelling and transfer functions are required for closed loop design. Small-signal modelling is done using state-space averaging approach and a two-loop average current control is designed to regulate the output voltage under dynamic operation [135]-[137]. The controller is implemented using 2 proportional integral (PI) controllers as shown in Fig. 6.1, namely inner current loop PI controller and the other outer voltage loop PI controller in generates the current reference for the inner current loop. Performance of the designed controller against wide input voltage and load disturbance is validated using PSIM 11.1.5 software. Simulation results for the step change in load are presented at different source voltages to validate the proposed controller design and transient performance.

a) Small-signal modelling using state-space averaging

This Section covers the state-space modelling and transfer function derivation of the series resoannce pulse operated current-fed half-bridge dc-dc converters. Small signal ac analysis is accomplished adopting state-space averaging technique for each interval of operation with equations given in Table 6.1. For the simplified analysis, the following assumptions are



(a)



(b)

Fig. 6.1. (a) Converter schematic (b) Proposed two-loop control schematic

considered: 1) Identical input boost inductors with $L_1 = L_2$, 2) The transformer leakage inductance is considered part of the resonant inductor L_r, 3) the output capacitors C_1, C_2 are charged to half of the output voltage (V_o/2) and 4) All the components are ideal and lossless. State variables considered for the small signal modelling of this converter are: 1) resonant

TABLE 6.1: STATE EQUATIONS FOR DIFFERENT MODES OF OPERATION.

Mode 1(t_0-t_1)	*Mode 2(t_1-t_2) and Mode 3(t_2-t_3)*	*Mode 4(t_3-t_4)*
$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{cr} - \frac{V_o}{2n}$	$L_1 \frac{di_{L1}}{dt} = V_{in}$	$L_1 \frac{di_{L1}}{dt} = V_{in}$
$L_2 \frac{di_{L2}}{dt} = V_{in}$	$L_2 \frac{di_{L2}}{dt} = V_{in}$	$L_2 \frac{di_{L2}}{dt} = V_{in} - V_{cr} - \frac{V_o}{2n}$
$L_r \frac{di_{lr}}{dt} = 0, C_r \frac{dV_{cr}}{dt} = i_{lr} = i_{L1}$	$L_r \frac{di_{lr}}{dt} - V_{cr} - \frac{V_o}{2n} = 0$	$C_r \frac{dV_{cr}}{dt} = -i_{lr} = i_{L2}$
$C_{o1} \frac{dV_{Co1}}{dt} = \frac{i_{lr}}{n} - \frac{V_o}{R}$	$C_{o1} \frac{dV_{Co1}}{dt} = \frac{i_{lr}}{n} - \frac{V_o}{R}$	$C_{o1} \frac{dV_{Co1}}{dt} = -\frac{V_o}{R}$
$C_{o2} \frac{dV_{Co2}}{dt} = \frac{V_o}{R}$	$C_{o2} \frac{dV_{Co2}}{dt} = \frac{V_o}{R}$	$C_{o2} \frac{dV_{Co2}}{dt} = \frac{i_{lr}}{n} - \frac{V_o}{R}$

inductor current i_{Lr} 2) boost inductor currents i_{L1} and i_{L2} 3) output voltage V_o 4) input voltage V_{in} and 5) series resonant capacitor voltage V_{Cr}.

For state-space averaging, the average rate of change of i_{Lr} over one switching cycle is considered zero and the averaged state equations are given as:

$$L_1 \langle \frac{di_{L1}}{dt} \rangle = V_{in} - \left(V_{cr} + \frac{V_o}{2n} \right) d_{S1}, \qquad L_2 \langle \frac{di_{L2}}{dt} \rangle = V_{in} - \left(V_{cr} + \frac{V_o}{2n} \right) d_{S2} \tag{6.1}$$

$$L_r \frac{di_{lr}}{dt} = 0, \qquad C_r \langle \frac{dV_{cr}}{dt} \rangle = i_{L1} d_{S1} - i_{L2} d_{S2} \tag{6.2}$$

$$C_{o1} \langle \frac{dV_{Co1}}{dt} \rangle = \frac{i_{lr1}}{n} d_{S1} - \frac{V_o}{R}, \qquad C_{o2} \langle \frac{dV_{Co2}}{dt} \rangle = \frac{i_{lr2}}{n} d_{S2} - \frac{V_o}{R} \tag{6.3}$$

Here, i_{avg} is the average output capacitor current and is given by $\frac{i_{l1}}{n} d_{S1} + \frac{i_{ll2}}{n} d_{S2}$

Introducing perturbation in state variables such that, $i_{L1} = I_{L1} + \widehat{i_{L1}}$, $i_{L2} = I_{L2} + \widehat{i_{L2}}$, $v_o = V_o + \widehat{v_o}$, $v_{Co1} = V_{Co1} + \widehat{v_{co1}}$, $v_{Co2} = V_{Co2} + \widehat{v_{co2}}$, the modified state equations are as follows:

$$L_1 \langle \frac{d(I_{L1} + \widehat{i_{L1}})}{dt} \rangle = V_{in} - \left(V_{cr} + \frac{V_o}{2n} \right) d_{S1}, \qquad L_2 \langle \frac{d(I_{L2} + \widehat{i_{L2}})}{dt} \rangle = V_{in} - \left(V_{cr} + \frac{V_o}{2n} \right) d_{S2} \tag{6.4}$$

$$C_r \langle \frac{d(V_{cr} + \widehat{v_{cr}})}{dt} \rangle = (I_{L1} + \widehat{i_{L1}}) d_{S1} - (I_{L2} + \widehat{i_{L2}}) d_{S2} \tag{6.5}$$

$$C_{o1}\langle\frac{d(V_{Co1}+\widehat{v_{co1}})}{dt}\rangle=\frac{(I_{L1}+\widehat{i_{L1}})}{n}d_{S1}-\frac{(V_o+\widehat{v_o})}{R},C_{o2}\langle\frac{d(V_{Co2}+\widehat{v_{co2}})}{dt}\rangle=\frac{(I_{L2}+\widehat{i_{L2}})}{n}d_{S2}-\frac{(V_o+\widehat{v_o})}{R} \quad (6.6)$$

$$d_{S1}=0.5+f_{s1}\frac{I_L}{V_{dc}}K,\qquad d_{S2}=0.5+f_{s1}\frac{I_L}{V_{dc}}K \quad (6.7)$$

Also, substituting (6.7) in (6.4), (6.5) and (6.6) and considering $L=L_1+L_2$, $V_o=V_{Co1}+V_{Co2}$, $I_L=I_{L1}+I_{L2}$, *and* $f_s=f_{s1}=f_{s2}$ to obtain the transfer function with respect to switching frequency. Further, averaged equations in S-domain (Laplace) are considered to obtain desired transfer functions.

b) Closed-loop transfer functions

The Current loop and voltage loop transfer functions are given by,

$$\frac{\widehat{i_L}(s)}{\widehat{f_s}(s)}=\frac{\left(2C_o{V_o}^2\right)S+\frac{2{V_o}^2}{R}-\frac{I_LV_o}{2}-I_LC_r}{(C_o(L+L_r)V_o)S^2+(L_{r1}V_o-I_L(L+L_r)V_o+V_o2C_o)S+V_o\left(\frac{2\pi}{R}+0.5\right)+(2I_Lf_s)}$$

$$\frac{\widehat{V_o}(s)}{\widehat{i_{L1}}+\widehat{i_{L2}}}=\frac{((L+L_r)V_o)S+8I_Lf_s+\frac{V_o}{2}+f_s}{2V_oC_oS+\frac{4V_o}{R}}$$

Transfer function for the PI controllers used are given by,

$$T_{C1,2}(s)=K_p+\frac{K_i}{S}=\frac{K_p(S+K_i/K_p)}{S}$$

To obtain a positive phase margin (PM) of 60º at 15kHz gain crossover frequency, PI controller values K_p and K_i for current controller are obtained as K_p=0.276∗10^4 and K_i=4.013∗10^{-5}, respectively. PI controller values for the voltage control loop are obtained with chosen crossover frequency at 1 kHz and phase-margin of 60º as K_p=2.71 and K_i=0.057, respectively. Positive PM allows stablity to the system during dynamic conditions, which provides better control against large disturbances in source voltage and load current.

c) Simulation Results

For the converter specifications; input voltage V_{in} = 42-48 V, rated power, P_o= 500W, output voltage, V_o = 380 V, maximum switching frequency f_s = 150 kHz and the component values of L_r=3.5μH and C_r=73nF, $L_1=L_2$= 400μH, C_1= C_2=100μF, transfer functions are derived. Two-loop average current control is implemented in PSIM 11.1 to regulate the load voltage and control the power flow. It has been observed that inner control loop with faster

dynamics allows inductor current to change more swiftly compared to the output voltage, which has slower dynamics. The converter under study is subjected to a load disturbance from 100% to 50% of the rated power with source voltage of 42V as shown in Fig. 6.2 (a). Fig. 6.2 (b) depicts the converter waveforms for a load change from100 % to 50 % of the rated power to validate its performance under partial load condition. Fig. 6.3(a) and 6.3(b) demonstrate transient results for load change from 50% to 100% and from 50% down to 20% respectively. It has been observed that the semiconductor switches are turned-off at ZCS and output voltage is regulated at 380V under all condition. Moreover, the converter response is quick to the load change and settles to its desired value within 5ms. For further verification of the controller and converter's actual performance, experimental results should be obtained on the hardware prototype during transient operation at different loading conditions and varying source voltage.

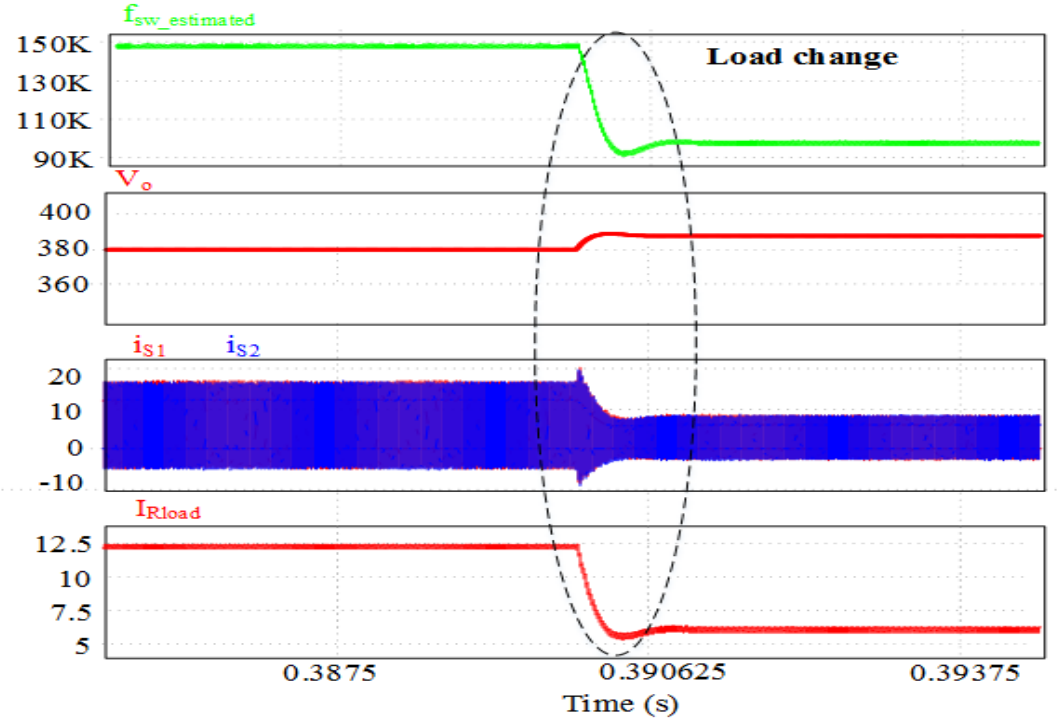
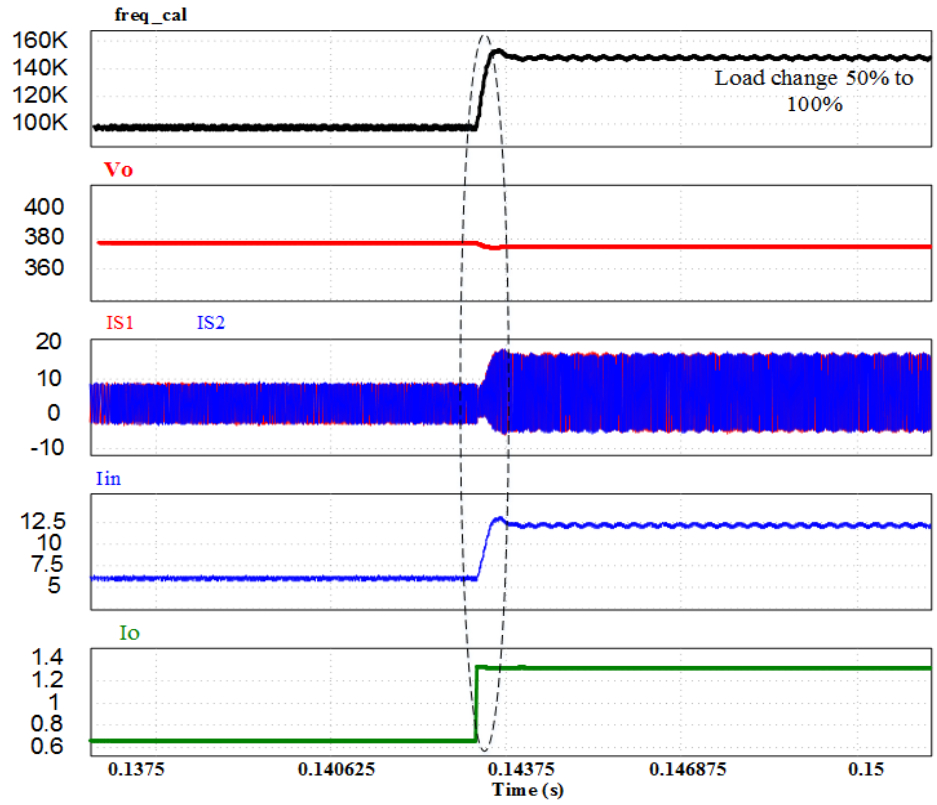
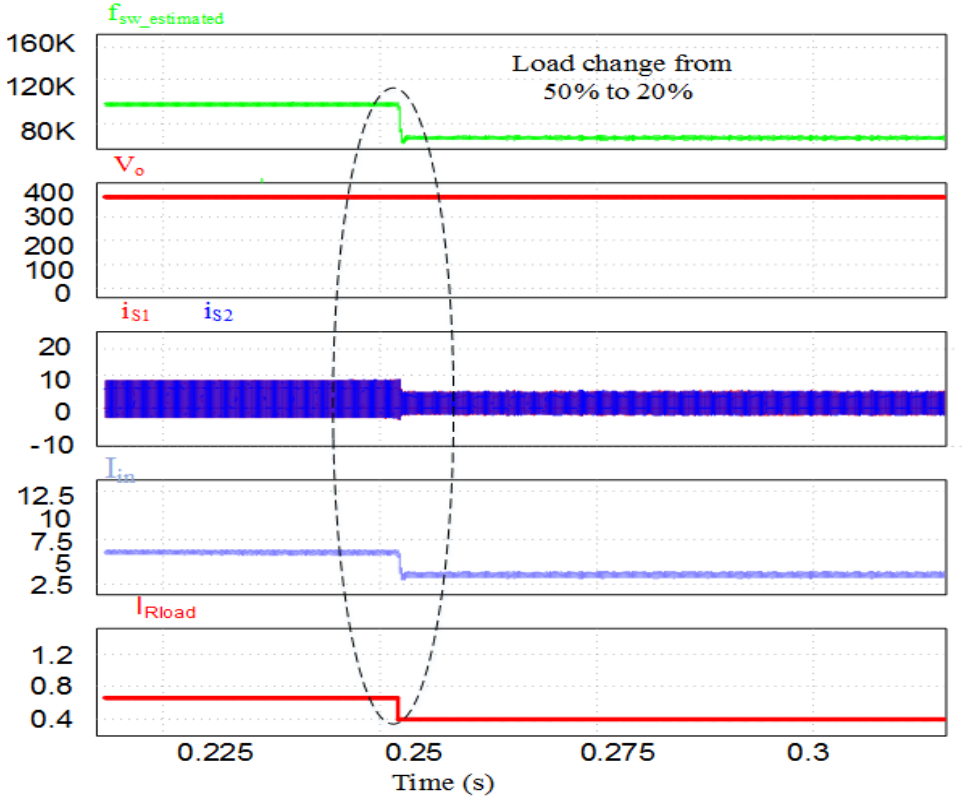


Fig. 6.2. Simulation results with V_{in}= 42V for load change from 100 % to 50 %.



(a)



(b)

Fig. 6.3. Simulation results for (a) load change from 50 % to 100 % (b) load change from 50 % to 20%.

6.2.2 *Series resonant-pulse assisted modular current-fed three-phase converter topology*

In this thesis, series resonance-pulse concept for the current-sharing three-phase current-fed topology was proposed and studied in Chapter 5. The same can be extended to other current-fed three-phase circuits. One potential converter configuration is a single inductor modular three-phase current-fed topology for high power applications (>5 kW). Various converter modules can be configured in series/parallel to supply high power levels while reducing the current stresses on the individual components. The benefits with modular architecture include: lower component's ratings, scalability, design flexibility and higher fault-tolerant capability.

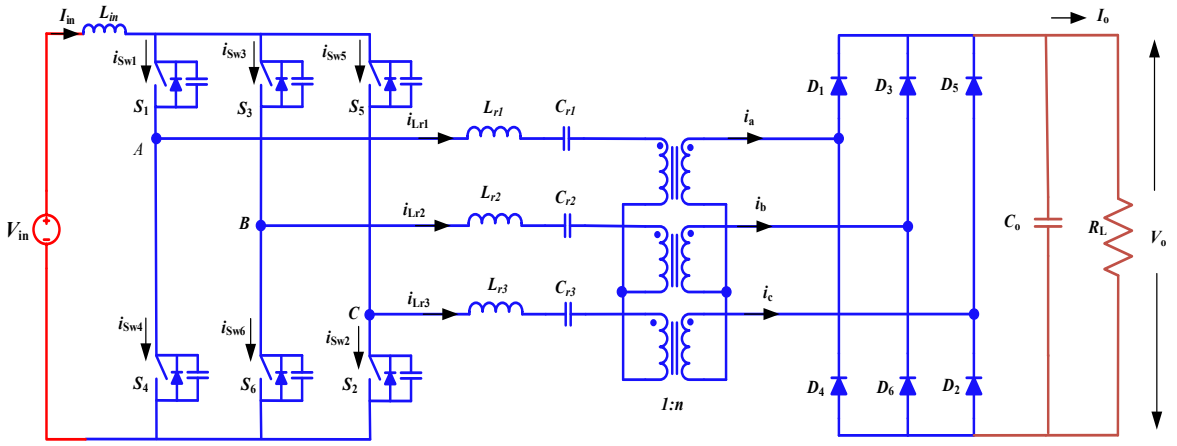


Fig. 6.4. Schematic of the series resonant-pulse assisted modular current-fed three-phase converter topology.

Bibliography

[1] Renewables. International Energy Agency, 2019.

[2] World energy outlook, International Energy Agency, 2019.

[3] International Energy Outlook. Energy Information Administration, 2018.

[4] BP Statistical review of Worlds Energy, 2019.

[5] IEA (2020), Key World Energy Statistics 2020, IEA, Paris https://www.iea.org/reports/key-world-energy-statistics-2020

[6] IEA (2020), Global Energy Review 2020, IEA, Paris https://www.iea.org/reports/global-energy-review-2020

[7] BP Energy outlook, 2020.

[8] Gielen D, Saygin D, et al.Renewable Energy Prospects: United States of America. A Renewable Energy Roadmap, Remap 2030: International Renewable Energy Agency; 2015.

[9] D. Gielen, F. Boshell, D. Saygin, M.D. Bazillian, N. Wagner, R. Gorini, The role of renewable energy in the global energy transformation, energy strategy Rev. 24 (2019) 38-50

[10] BP Statistical review of Worlds Energy, 2020.

[11] REN21, "Renewables 2018 global status report," (Paris: REN21 Secretariat), 2020.

[12] REN21, "Renewables 2018 global status report," (Paris: REN21 Secretariat), 2018.

[13] R. L. Steigerwald and R. E. Tompkins, "A Comparison of High-Frequency Link Schemes for Interfacing a DC Source to a Utility Grid," *Proceedings IEEE IAS'82*, Vol. 17, 1982, pp. 759-766.

[14] V. Rajagopalan, K. Al Haddad and J. Ayer, "Innovative Utility-Interactive D.C. to A.C. Power Conditioning System," *Proceedings of IEEE IECON '85*, Vol. 2, 18-22 November 1985, pp. 471-476.

[15] P. Biczel, "Power electronic converters in DC microgrid," *in Proc. Compat. Power Electron.,* 2007, pp. 1–6.

[16] G. K. Andersen, C. Klumpner, S. B. Kjaer and F. Blaabjerg, "A New Green Power Inverter for Fuel Cells," *Proceedings of IEEE PESC'02*, Vol. 2, 23-27 June 2002, pp. 727-733.

[17] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[18] Blazewicz, S.,"Distributed Energy Resources Integration Research Program Power Electronics Research Assessment." *Navigant Consulting, California Energy Commission*; vol. CEC-500-2005-206, Dec. 2005.

[19] S. D. G. Jayasinghe, D. M. Vilathgamuwa, and U. K. Madawala, “A new method of interfacing battery/supercapacitor energy storage systems for distributed energy sources," *in Proc. IPEC,* pp. 1211-1216, Oct 2010.

[20] Microgrids and distribution systems: An overview,” *in Proc. IEEE Power Energy Soc. Gen. Meeting,* Vancouver, BC, USA, 2013, pp. 1–5.

[21] J. D. van Wyk and F. C. Lee, “On a future for power electronics,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 2, pp. 59–72, Jun. 2013.

[22] A. T. Ghareeb, A. A. Mohamed, and O. A. Mohammed, “DC microgrids and distribution systems: An overview*,” in Proc. IEEE Power Energy Soc. Gen. Meeting*, Vancouver, BC, USA, 2013, pp.1–5.

[23] R. W. De Doncker, “Power electronic technologies for flexible dc distribution grids," *in Proc. Int. Power Electron. Conf. (IPEC - ECCE Asia)*, Hiroshima, 2014, pp. 736-743.

[24] M. Patterson, N. F. Macia and A. M. Kannan, "Hybrid Microgrid Model Based on Solar Photovoltaic Battery Fuel Cell System for Intermittent Load Applications," *in IEEE Transactions on Energy Conversion,* vol. 30, no. 1, pp. 359-366, March 2015.

[25] M. Nasir, H. A. Khan, A. Hussain, L. Mateen and N. A. Zaffar, "Solar PV-Based Scalable DC Microgrid for Rural Electrification in Developing Regions," *in IEEE Transactions on Sustainable Energy*, vol. 9, no. 1, pp. 390-399, Jan. 2018.

[26] S. Kumar Tiwari, B. Singh and P. K. Goel, "Design and Control of Microgrid Fed by Renewable Energy Generating Sources," *in IEEE Transactions on Industry Applications*, vol. 54, no. 3, pp. 2041-2050, May-June 2018.

[27] Q. Fu et al., "Microgrid Generation Capacity Design With Renewables and Energy Storage Addressing Power Quality and Surety," *in IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 2019-2027, Dec. 2012.

[28] A. Emadi, and S. S. Williamson, “Fuel cell vehicles: opportunities and challenges,” *IEEE PES meeting* 2004, pp. 1640-1645.

[29] V. Telukunta, J. Pradhan, A. Agrawal, M. Singh and S. G. Srivani, "Protection challenges under bulk penetration of renewable energy resources in power systems: A review," *in CSEE Journal of Power and Energy Systems,* vol. 3, no. 4, pp. 365-379, Dec. 2017.

[30] M. Nasir and E. Nasr-Azadani, "System performance in microgrids based hybrid PV systems," *2017 IEEE Power & Energy Society General Meeting,* Chicago, IL, USA, 2017, pp. 1-5.

[31] J. Wang, F. Z. Peng, J. Anderson, A. Joseph and R. Buffenbarger, “Low Cost Fuel Cell Converter System for Residential Power generation,” *IEEE Transactions on Power Electronics*, vol. 19, No. 5, pp. 1315-1322, 2004.

[32] Z. Li et al., "Adaptive Power Point Tracking Control of PV System for Primary Frequency Regulation of AC Microgrid with High PV Integration," *in IEEE Transactions on Power Systems*, doi: 10.1109/TPWRS.2021.3049616.

[33] S. A. Pattanaik and M. Mishra, "Integration of hybrid renewable energy and its control in grid connected and islanded mode," *2017 International Conference on Power and Embedded Drive Control (ICPEDC),* Chennai, India, 2017, pp. 14-19, doi: 10.1109/ICPEDC.2017.8081052.

[34] M. Nasir, S. Iqbal and H. A. Khan, "Optimal Planning and Design of Low-Voltage Low-Power Solar DC Microgrids," *in IEEE Transactions on Power Systems,* vol. 33, no. 3, pp. 2919-2928, May 2018.

[35] G. Fontes, C. Turpin, S. Astier, and T. A. Meynard, “Interactions between fuel cell and power converters: Influence of current harmonic on a fuel cell stack,” *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 670–678, Mar. 2007.

[36] M. Harfman-Todorovic, L. Palma, M. Chellappan and P. Enjeti, “Design Considerations for Fuel Cell Powered UPS,” *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2008, pp.1984- 1990.

[37] Li, Z., Zheng, Z., Xu, L. *et al.* A review of the applications of fuel cells in microgrids: opportunities and challenges. *BMC Energy* **1,** 8 (2019).

[38] F. L. Tofoli, D. C. Pereira, W. J. Paula, and D. S. O. Junior, “Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter,” *IET Power Electron.,* vol. 8, no. 10, pp. 2044–2057, Oct. 2015.

[39] M. A. Chewale, R. A.Wanjari, V. B.Savakhande and P. R.Sonawane, "A Review on Isolated and Non-isolated DC-DC Converter for PV Application," *2018 International Conference on Control, Power, Communication and Computing Technologies (ICCPCCT),* Kannur, India, 2018, pp. 399-404.

[40] K. Alluhaybi, I. Batarseh and H. Hu, "Comprehensive Review and Comparison of Single-Phase Grid-Tied Photovoltaic Microinverters," *in IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 2, pp. 1310-1329, June 2020.

[41] O. Ibrahim, N. Z. Yahaya and N. Saad, "Single phase inverter with wide-input voltage range for solar photovoltaic application," *2015 IEEE 15th International Conference on Environment and Electrical Engineering (EEEIC)*, Rome, Italy, 2015, pp. 139-143.

[42] R. Sharma and Hongwei Gao, "Low cost high efficiency DC-DC converter for fuel cell powered auxiliary power unit of a heavy vehicle," in *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 587-591, May 2006.

[43] M. Harfman Todorovic, L. Palma and P. Enjeti, "Design of a Wide Input Range DC-DC Converter with a Robust Power Control Scheme Suitable for Fuel Cell Power Conversion," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, 2004, pp.374-379.

[44] A. K. Rathore, High-frequency transformer isolated power conditioning system for fuel cells to utility interface. PhD thesis, 2008.

[45] P. Xuewei, Soft-switching current-fed power converters for low voltage high current applications. PhD thesis, 2014.

[46] A. K. Rathore and U. R. Prasanna, "Comparison of soft-switching voltage-fed and current-fed bi-directional isolated dc/dc converters for fuel cell vehicles," *in Proc. IEEE Int. Symp. Ind. Electron*., 2012, pp. 3212–3219.

[47] G. Moschopoulos, S. Bassan, Shumin Li and Qingyi Su, "Properties and characteristics of voltage-fed single stage converters," *Canadian Conference on Electrical and Computer Engineering,* 2005., Saskatoon, SK, Canada, 2005, pp. 1266-1269.

[48] R. Watson and F. C. Lee, "A soft-switched, full-bridge boost converter employing an active-clamp circuit," *in Proc. IEEE Power Electron. Spec. Conf.,* 1996, pp. 1948–1954.

[49] C. M. Wang, C. H. Su, and C. H. Yang, "Zvs-pwm flyback converter with a simple auxiliary circuit*," Proc. Electric Power Applications,* vol. 153, pp. 116-122, Jan 2006.

[50] H. S. H. Chung, W.-L. Cheung, and K. S. Tang, "A zcs bidirectional flyback dc/dc converter," *IEEE Trans. Power Electron*., vol. 19, pp. 1426-1434, Nov 2004.

[51] K.-W. Ma and Y.-S. Lee, "An integrated flyback converter for dc uninterruptible power supply*," IEEE Trans. Power Electron*., vol. 11, pp. 318-327, Mar 1996.

[52] K. Yoshida, T. Ishii, and N. Nagagata, "Zero voltage switching approach for flyback converter," *in Proc. 14th International Telecommunications Energy Conference, INTELEC* '92, pp. 324-329, Oct1992.

[53] D. H. Seo, O. J. Lee, S. H. Lim, and J. S. Park, "Asymmetrical pwm flyback converter," *in Proc. IEEE 31st Annual Power Electronics Specialists Conference (PESC),* vol. 2, pp. 848-852 vol.2, 2000.

[54] T. Chen and C. Chen, "Analysis and design of asymmetrical half bridge flyback converter," *Proc. Electric Power Applications*, vol. 149, pp. 433-440, Nov 2002.

[55] J. j. Shieh, T. j. Chiou, and T. M. Lee, “A closed-form oriented analysis and design for zero-voltage-switched asymmetrical half-bridge dc/dc forward converters," *in Proc. 1ST IEEE Conference on Industrial Electronics and Applications*, pp. 1-6, May 2006.

[56] Y.-H. Leu and C.-L. Chen, “Analysis and design of two-transformer asymmetrical half-bridge converter," *in Proc. IEEE 33rd Annual Power Electronics Specialists Conference (PESC),* vol. 2, pp. 943-948 vol.2, 2002.

[57] Y.-H. Len, C.-L. Chen, and T.-M. Chen, “Analysis and design for asymmetrical half-bridge forward mode converters," *in Proc. 4th IEEE International Conference on Power Electronics and Drive Systems*, vol. 1, pp. 126-130 vol.1, Oct 2001.

[58] H. Mao, J. Abu-Qahouq, S. Luo, and I. Batarseh, “Zero-voltage-switching half-bridge dc-dc converter with modified pwm control method," *IEEE Trans. Power Electron*., vol. 19, pp. 947-958, July 2004.

[59] T. F. Wu, J. C. Hung, J. T. Tsai, C. T. Tsai, and Y. M. Chen, “An active-clamp push-pull converter for battery sourcing applications,"*IEEE Trans. Ind. Appls*., vol. 44, pp. 196-204, Jan 2008.

[60] A. K. Rathore, "Current-fed DC/DC converters for high voltage gain and low voltage high current applications: An overview of topologies and modulation techniques," *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES),* Trivandrum, India, 2016, pp. 1-6.

[61] X. Pan, H. Li, Y. Liu, T. Zhao, C. Ju and A. K. Rathore, "An Overview and Comprehensive Comparative Evaluation of Current-Fed-Isolated-Bidirectional DC/DC Converter," *in IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2737-2763, March 2020.

[62] A. K. Rathore, A. K. S. Bhat, R. Oruganti, "A comparison of soft-switched DC–DC converters for fuel-cell to utility-interface application", *Proc. IEEE Power Convers. Conf*., pp. 588-594, 2007.

[63] M. Nymand and M. A. E. Andersen, “High-efficiency isolated boost dc/dc converter for high-power low-voltage fuel-cell applications," *IEEE Trans. Ind. Electron*., vol. 57, pp. 505-514, Feb 2010.

[64] E.-S. Kim, K.-Y. Joe, H.-Y. Choi, Y.-H. Kim, and Y.-H. Cho, “An improved soft switching bi-directional pspwm fb dc/dc converter*," in Proc. 24th Annual Conference of the IEEE Industrial Electronics Society, IECON '98,* vol. 2, pp. 740-743 vol.2, Aug 1998.

[65] T. Tanaka, T. Ninomiya, and K. Harada, “Design of a nondissipative turn-off snubber in a forward converter," *in Proc. 19th Annual IEEE Power Electronics Specialists Conference, PESC '88*, pp. 789-796 vol.2, April 1988.

[66] F. J. Nome and I. Barbi, “A zvs clamping mode-current-fed push-pull dc-dc converter," *in Proc. IEEE International Symposium on Industrial Electronics, ISIE* '98., vol. 2, pp. 617-621 vol.2, Jul 1998.

[67] V. Yakushev, V. Meleshin, and S. Fraidlin, “Full-bridge isolated current fed converter with active clamp,” *in Proc. 14th IEEE Appl. Power Electron. Conf. Expo.,* 1999, pp. 560–566.

[68] E. S. Park, S. J. Choi, J. M. Lee, and B. H Cho, “A soft-switching active clamp scheme for isolated full-bridge boost converter,” *in Proc. IEEE Appl. Power Electron. Conf.* Expo., 2004, vol. 2, pp. 1067–1070.

[69] J.-T. Kim, B.-K. Lee, T.-W. Lee, S.-J. Jang, S.-S. Kim, and C.-Y. Won, “An active clamping current-fed half-bridge converter for fuel-cell generation systems*,” in Proc. IEEE Power Electron. Spec. Conf*., 2004, pp. 4709– 4714.

[70] S.-K. Han, H.-K. Yoon, G.-W. Moon, M.-J. Youn, Y.-H. Kim, and K.- H. Lee, “A new active clamping zero-voltage switching PWM currentfed half-bridge converter,” *IEEE Trans. Power Electron*., vol. 20, no. 6, pp. 1271–1279, Nov. 2005.

[71] Q. Wu, M. Wang, W. Zhou, C. Huang, G. Liu and X. Wang, "High frequency active-clamped zero-current switching current-fed push-pull converter for micro-converter applications," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, USA, 2020, pp. 1273-1278.

[72] C. F. Moraes, E. G. Carati, J. P. da Costa, R. Cardoso and C. M. d. Oliveira Stein, "Active-Clamped Zero-Current Switching Current-Fed Half-Bridge Converter," *in IEEE Transactions on Power Electronics,* vol. 35, no. 7, pp. 7100-7109, July 2020.

[73] A. K. Rathore, A. K. S. Bhat, R. Oruganti, "Wide range ZVS active clamped L-L type current-fed dc-dc converter for fuel cells to utility interface: analysis design and experimental results", *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 473-485, 2012.

[74] U. R. Prasanna and A. K. Rathore, “Extended range ZVS active-clamped current-fed full-bridge isolated dc/dc converter for fuel cell applications: Analysis, design and experimental results,” *IEEE Trans. Ind. Electron.,* vol. 60, no. 7, pp. 2661–2672, Jul. 2013.

[75] Hanju Cha, Jungwan Choi and Enjeti, P.N., “A three-phase current-fed DC/DC converter with active clamp for low-DC renewable energy sources”, *IEEE Trans. on Power Electronics*, vol. 23, no. 6, pp. 2784 -2793, Nov. 2008.

[76] Y. Song et al., "A current-fed three-phase half-bridge dc-dc converter with active clamping," *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, USA, 2009, pp. 1362-1366.

[77] Sangwon Lee, Junsung Park and Sewan Choi, “A three-phase current-fed push–pull DC–DC converter with active clamp for fuel cell applications”, *IEEE Trans. on Power Electronics,* vol. 26, no. 8, pp. 2266-2277, 2011.

[78] T. F. Wu, Y. C. Chen, J. G. Yang, and C. L. Kuo, “Isolated bidirectional full-bridge dc/dc converter with a flyback snubber," *IEEE Trans. Power Electron*., vol. 25, pp. 1915-1922, July 2010.

[79] J. B. Banu and M. B. Moses, "A current fed full bridge DC-DC converter with an active flyback and passive auxiliary circuits," *2016 International Conference on Energy Efficient Technologies for Sustainability (ICEETS),* Nagercoil, India, 2016, pp. 382-387.

[80] U. R. Prasanna, A. K. Rathore and S. K. Mazumder, "Novel Zero-Current-Switching Current-Fed Half-Bridge Isolated DC/DC Converter for Fuel-Cell-Based Applications," *in IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1658-1668, July-Aug. 2013.

[81] A. K. Rathore and U. R. Prasanna, “Analysis, design, and experimental results of novel snubberless bidirectional naturally clamped ZCS/ZVS current-fed half-bridge dc/dc converter for fuel cell vehicles,” *IEEE Trans. Ind Electron*., vol. 60, no. 10, pp. 4482–4491, Oct. 2013

[82] P. Xuewei and A. K. Rathore, “Novel Interleaved Bidirectional Snubberless Soft-switching Current-fed Full-bridge Voltage Doubler forFuel Cell Vehicles,” *IEEE Trans. Power Electron.,* vol. 28, no. 12, Dec. 2013, pp. 5355-5546.

[83] P. Xuewei, A. K. Rathore, "Novel Bidirectional snubberless naturally commutated soft-switching current-fed full bridge isolated DC/DC Converter for fuel cell vehicles", *IEEE Trans. Ind. Electro*., vol. 61, no. 5, pp. 2307-2315, May 2014.

[84] P. Xuewei and A. K. Rathore, “Naturally clamped zero-current commutated soft-switching current-fed push-pull dc/dc converter: Analysis, design, and experimental results,” *IEEE Trans. Power. Electron.,* vol. 30, no. 3, pp. 1318–1327, Mar. 2015.

[85] P. Xuewei and A. K. Rathore, “Naturally clamped soft-switching current- fed three-phase bidirectional DC/DC converter,” *IEEE Trans. Ind. Elec- tron.*, vol. 62, no. 5, pp. 3316–3324, May 2015.

[86] S. Bal, A. K. Rathore and D. Srinivasan, "Naturally Clamped Snubberless Soft-Switching Bidirectional Current-Fed Three-Phase Push–Pull DC/DC Converter for DC Microgrid Application," *in IEEE Transactions on Industry Applications,* vol. 52, no. 2, pp. 1577-1587, March-April 2016.

[87] K. Liu, R. Oruganti and F. C. Lee, “Resonant switches-topologies and characteristics," *IEEE Trans. Power Electron*., vol. 2, no. 1, pp. 106-116, 1987.

[88] A. K. S. Bhat and S. B. Dewan, “DC-to-Utility Interface Using Sinewave Resonant Inverter,” *IEEE Proceedings,* Vol. 135, Part B, No. 5, September 1988, pp. 193-201.

[89] A. K. S. Bhat and S. B. Dewan, “Analysis and Design of a High-Frequency Link DC to Utility Interface Using Square-Wave Output Resonant Inverter,” *IEEE Transactions on Power Electronics*, Vol. 3, No. 3, July 1988, pp. 355-363.

[90] A. K. S. Bhat and S. B. Dewan, “ Resonant Inverters for Photo Voltaic Array to Utility Interface,” *IEEE Transactions on Aerospace and Electronic Systems*, Vol. AES-24, No. 4, July 1988, pp. 377-386.

[91] A. K. S. Bhat and M. M. Swamy, “Analysis of parallel resonant converter operating above resonance," *IEEE Trans. Aerosp. Electron. Syst.,* vol. 25, no. 4, pp.449-458, Jul. 1989.

[92] W. C. P. De Aragao Filho and I. Barbi, "A comparison between two current-fed push-pull DC-DC converters-analysis, design and experimentation," *Proceedings of Intelec'-International Telecommunications Energy Conference*, Boston, MA, USA, 1996, pp. 313-320.

[93] M. J. Ryan, W. E. Brumsickle, D. M. Divan, and R. D. Lorenz, “A new ZVS LCL-resonant push-pull DC-DC converter topology,” *IEEE Trans. Ind. Appl.,* vol. 34, no. 5, pp. 1164–1174, Sep./Oct. 1998.

[94] E. S. Kim, K. Y. Joe, H. Y. Choi, Y. H. Kim, Y. H. Cho, "An Improved Soft Switching Bi-directional PSPWM FB DC/DC Converter", *Proc. IEEE IECON*, pp. 740-743, 1998.

[95] C. Iannello, S. Luo, I. Batarseh, “Full bridge ZCS PWM converter for high-voltage high-power applications,” *IEEE Trans. Aerosp. Electron. Syst.,* vol. 38, no. 2, pp. 515-526, Apr. 2002.

[96] J. Zhang, J. S. Lai, R.-Y.Kim, and W.Yu,“High-power density design of a soft-switching high-power bidirectional DC–DC converter,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.

[97] L. D. Salazar and P. D. Ziogas, “Design oriented analysis of two types of three-phase high frequency forward SMR topologies,” in *Proc. 5th Annu. IEEE APEC*, Mar. 11–16, 1990, pp. 312–320.

[98] S. Jalbrzykowski and T. Citko, “Current-fed resonant full-bridge boost DC/AC/DC converter,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1198–1205, Mar. 2008.

[99] W. Chen, Z. Lu, X. Zhang, and S. Ye, “A novel ZVS step-up push-pull type isolated LLC series resonant dc-dc converter for UPS systems and its topology variations,” *in Proc. IEEE APEC, 2008*, pp. 1073–1078.

[100] H. Wang, Q. Sun, H. S. H. Chung, S. Tapuchi and A. Ioinovici, “A ZCS current-fed full-bridge pwm converter with self-adaptable soft switching snubber energy,” *IEEE Trans. Power Electron.,* vol. 24, no. 8, pp. 1977-1991, Aug. 2009.

[101] B. Yuan et al., "Analysis and design of a high step-up current-fed multiresonant DC–DC converter with low circulating energy and zero-current switching for all active switches", *IEEE Trans. Ind. Electron.,* vol. 59, no. 2, pp. 964-978, Feb. 2012.

[102] S. Manikandan and S. Venkatasubramanian, "Implementation of high efficiency current-fed push-pull converter using soft switching technique," *2012 International Conference on Computing, Electronics and Electrical Technologies (ICCEET),* Nagercoil, India, 2012, pp. 273-278.

[103] D. Chakraborty, A. K. Rathore, E. Breaz and F. Gao, "Parasitics assisted soft-switching and naturally commutated current-fed bidirectional push-pull voltage doubler," *2015 IEEE Industry Applications Society Annual Meeting, Addison,* TX, USA, 2015, pp. 1-8.

[104] A. Mousavi, P. Das and G. Moschopoulos, "A Comparative Study of a New ZCS DC–DC Full-Bridge Boost Converter With a ZVS Active-Clamp Converter," *in IEEE Transactions on Power Electronics,* vol. 27, no. 3, pp. 1347-1358, March 2012.

[105] K. Modepalli, R. Suryadevara and L. Parsa, "High-frequency isolated DC-DC converter for offshore wind energy systems," *2016 IEEE Energy Conversion Congress and Exposition (ECCE*), Milwaukee, WI, 2016, pp. 1-6.

[106] R. Kosenko, A. Chub and A. Blinov, "Full-soft-switching high step-up bidirectional isolated current-fed push-pull DC-DC converter for battery energy storage applications," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society,* Florence, Italy, 2016, pp. 6548-6553.

[107] S. D. Nugraha, O. A. Qudsi, D. S. Yanaratri, E. Sunarno and I. Sudiharto, "MPPT-current fed push pull converter for DC bus source on solar home application," *International conferences on Information Technology, Information Systems and Electrical Engineering (ICITISEE),* Yogyakarta, Indonesia, 2017, pp. 378-383

[108] Y. Zhang, L. Zhou, M. Sumner and P. Wang, "Single-Switch, Wide Voltage-Gain Range, Boost DC–DC Converter for Fuel Cell Vehicles," in *IEEE Transactions on Vehicular Technology*, vol. 67, no. 1, pp. 134-145, Jan. 2018

[109] L. Tarisciotti, A. Costabeber, L. Chen, A. Walker and M. Galea, "Current-Fed Isolated DC/DC Converter for Future Aerospace Microgrids," *in IEEE Transactions on Industry Applications,* vol. 55, no. 3, pp. 2823-2832, May-June 2019.

[110] R. Suryadevara and L. Parsa, "Adaptive Resonant Energy Realization in FB-ZCS DC-DC Converter Using Dual-Capacitor Circuit," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 5536-5541.

[111] Y. Yuan, L. Lai and Q. Wu, "A Current-Fed LCL Resonant Converter for Wide Output-Voltage Applications*," in IEEE Transactions on Industrial Electronics*, vol. 68, no. 5, pp. 3939-3948, May 2021.

[112] L. D. Salazar and P. D. Ziogas, "Design oriented analysis of two types of three-phase high frequency forward SMR topologies," in *Proc. 5th Annu. IEEE APEC*, Mar. 11–16, 1990, pp. 312–320.

[113] A. K. S. Bhat and L. Zheng, "Analysis and design of a three phase LCC type resonant converter," *in Proc. IEEE 27th Annu. Power Electronics Specialists Conf. (PESC '96),* vol. 1, Baveno, Italy, Jun. 23–27, 1996, pp. 252–258.

[114] L. Changrong, A. Johnson, and J.-S. Lai, "A novel three-phase high-power soft-switched DC/DC converter for low-voltage fuel cell applications," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1691–1697, Nov./Dec. 2005.

[115] M. Mohr and F. W. Fuchs, "Voltage Fed and Current Fed Full Bridge Converter for the Use in Three Phase Grid Connected Fuel Cell Systems," *IEEE 5th International Power Electronics and Motion Control Conference,* Shanghai, 2006, pp. 1-7.

[116] R. L. Andersen and I. Barbi, "A three-phase current-fed push-pull DC-DC converter," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 358–368, Feb. 2009.

[117] S. V. G. Oliveira and I. Barbi, "A Three-phase step-up DC–DC con- verter with a three-phase high-frequency transformer for DC renewable power source applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3567–3580, Aug. 2011.

[118] Z. Wang and H. Li, "Soft switching three-phase current-fed bidirectional DC-DC converter with high efficiency over a wide input voltage range," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 669–684, Feb. 2012.

[119] R. Suryadevara, T. Li, K. Modepalli and L. Parsa, "Three-phase current fed soft-switching DC-DC converter," *in Proc. 2017 IEEE 26th Int. Symp. Ind. Electron. (ISIE),* Edinburgh, 2017, pp. 899-904.

[120] W. A. Tabisz and F. C. Lee, "Principles of quasi- and multi-resonant power conversion techniques," *in Proc. IEEE International Symposium on Circuits and Systems*, pp. 1053-1056 vol.2, Jun 1991.

[121] K. H. Liu and F. C. Y. Lee, "Zero-voltage switching technique in dc/dc converters," *IEEE Trans. Power Electron.,* vol. 5, pp. 293-304, Jul 1990.

[122] K. H. Liu and F. C. Lee, “Resonant switches for a unified approach to improve performances of switching converters," *in Proc. International Telecommunications Energy Conference, INTELEC* '84, pp. 344-351, Nov 1984.

[123] T. F. Wu, Y. K. Chen, C. H. Yang, and S. A. Liang, “A structural approach to synthesizing and analyzing quasi-resonant and multi-resonant converters," *in Proc. 30th Annual IEEE Power Electronics Specialists Conference, PESC 99*, vol. 2, pp. 1024-1029 vol.2, 1999.

[124] M. F. Schlecht and L. F. Casey, “Comparison of the square-wave and quasi-resonant topologies," *IEEE Trans. Power Electron.,* vol. 3, pp. 83-92, Jan 1988.

[125] X.-Z. Zhang and S.-P. Huang, “Novel high frequency quasi-square-wave converter topologies," *in Proc. 13th International Telecommunications Energy Conference, INTELEC '91*, pp. 663-667, Nov 1991.

[126] R.-Y. Chen, T.-J. Liang, J.-F. Chen, R.-L. Lin, and K.-C. Tseng, “Study and implementation of a current-fed full-bridge boost DC-DC converter with zero-current switching for high voltage applications,” *IEEE Trans. Ind. Appl*., *vol. 44, no. 4, pp. 1218–1226, Jul./Aug. 2008.*

[127] K. R. Sree and A. K. Rathore, “Impulse commutated zero current switching current-fed push-pull converter: Analysis, design and experimental results,” *IEEE Trans. Ind. Electron.,* vol. 632, no. 1, pp. 363–370, Jan. 2015.

[128] K. R. Sree and A. K. Rathore, “Soft-Switching Non-Isolated Current-Fed Inverter for PV/Fuel Cell Applications,” *IEEE Trans. On Ind. Appl.,* vol. 52, no. 1, Jan./Feb. 2016.

[129] K. R. Sree, A. K. Rathore, "Impulse commutated zero current switching current-fed three-phase DC/DC converter", *IEEE Trans. Ind. Appl.,* vol. 52, no. 2, pp. 1855-1864, Mar. 2016.

[130] K. R. Sree and A. K. Rathore, “Analysis and design of impulse-commutated zero-current-switching single-inductor current-fed three-phase push–pull converter,” *IEEE Trans. On Ind. Appl.,* vol. 53, no. 2, Mar./Apr. 2017.

[131] Q. Wu, Q. Wang, J. Xu, H. Li and L. Xiao, "A High-Efficiency Step-Up Current-Fed Push–Pull Quasi-Resonant Converter With Fewer Components for Fuel Cell Application," *in IEEE Transactions on Industrial Electronics,* vol. 64, no. 8, pp. 6639-6648, Aug. 2017.

[132] S. K. Radha and A. K. Rathore, "Comparison and evaluation of three-phase current-fed impulse commutated ZCS DC/DC converter topologies with variable frequency modulation," *2016 IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering (UPCON),* Varanasi, 2016, pp. 641-646.

[133] V. Ivakhno, V. Zamaruiev, B. Styslo, A. Blinov, D. Vinnikov and R. Kosenko, "Wide ZVS Range Full Bridge DC-DC Converter with Quasi-Resonant Switching," *2020 IEEE 4th International*

Conference on Intelligent Energy and Power Systems (IEPS), Istanbul, Turkey, 2020, pp. 317-322.

[134] R. Suryadevara and L. Parsa, "FB-ZCS DC–DC Converter With Dual-Capacitor Resonant Circuit for Renewable Energy Integration With MVDC Grids," *in IEEE Transactions on Industry Applications,* vol. 56, no. 6, pp. 6792-6802, Nov.-Dec. 2020.

[135] Venkatraman, R., and Bhat, A.K.S.: 'Small-signal analysis of a softswitching, single-stage two-switch AC-to-DC converter'. *Proc. IEEE Power Electronics Specialists Conference*, June 2001, pp. 1824-1830.

[136] K. Khatun, V. R. Vakacharla, A. R. Kizhakkan and A. K. Rathore, "Small-Signal Analysis and Control of Snubberless Naturally Clamped Soft-Switching Current-Fed Push–Pull DC/DC Converter," *in IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4299-4308, July-Aug. 2020.

[137] R. W. Erickson and D. Maksimovic,´ Fundamentals of Power Electronics, 2nd ed. New York, NY, USA: Springer, 2001.

List of publications

Journal Papers

1. **S. Tandon** and A. K. Rathore, "Analysis and Design of Series LC Resonance-Pulse Based Zero-Current-Switching Current-Fed Half-Bridge DC-DC Converter," *in IEEE Transactions on Industrial Electronics,* doi: 10.1109/TIE.2020.3005104.
2. **S. Tandon** and A. K. Rathore, "Novel Series LC Resonance-Pulse-Based ZCS Current-Fed Full-Bridge DC–DC Converter: Analysis, Design, and Experimental Results," *in IEEE Transactions on Power Electronics,* vol. 36, no. 2, pp. 1844-1855, Feb. 2021, doi: 10.1109/TPEL.2020.3010178.
3. **S. Tandon** and A. K. Rathore, "Analysis and Design of Series LC Partial-Resonance-Pulse Based ZCS Current-Fed Push-Pull Converter," *in IEEE Transactions on Industry Applications*, doi: 10.1109/TIA.2021.3074109.
4. **S. Tandon,** A. K. Rathore and J. Rodriguez, "Partial Series Resonance Pulse Commutated Current-Fed Three-phase current sharing DC/DC Converter: ZCS Analysis, Design and Experimental Results," *in IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, doi: 10.1109/JESTIE.2021.3074876.

Conference Papers

1. **Swati Tandon** and A. K. Rathore, “Series Resonance-Pulse Assisted Current-Fed Three-phase Three-Inductor DC-DC Converter Topology”, *in Proc. IEEE PEDES, Jaipur, India, Dec 2020*.
2. **Swati Tandon** and A. K. Rathore, “Series LC resonance-pulse based zero current switching current-fed push-pull converter”, *in Proc. IEEE IAS Annual Meeting.* , Detroit, USA, 2020.
3. **Swati Tandon** and A. K. Rathore, “A ZVS series resonant current-fed PWM controlled DC-DC converter*” IEEE Transportation Electrification conference and Expo (ITEC),* Chicago, USA, 2020.
4. **Swati Tandon** and A. K. Rathore, “Series LC resonance pulse based zero current switching current-fed half-bridge DC-DC converter”, *IEEE Applied Power Electronics Conference (APEC), New Orleans, USA, March 2020*.
5. **Swati Tandon** and A. K. Rathore, “Current-fed full-bridge series LC resonance impulse ZCS commutated DC-DC converter*”, in Proc. IEEE PESGRE conf., Kerala, India, 2020*.
6. **Swati Tandon** and A. K. Rathore, “LCL resonant soft-switching single stage single-phase grid connected inverter”, *IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Xi’an, China, 2019.
7. [Accepted] **Swati Tandon** and A. K. Rathore, “Small-signal modelling and closed loop control implementation of series resonance-pulse current-fed half-bridge dc-dc converter”, *IEEE ECCE Asia, 2021*.

Appendix

TABLE A.1: LOSS EQUATIONS USED TO COMPUTE THE CONVERTER LOSSES

Description	Equation
Switch conduction loss	$I_{sw,rms}{}^2 * R_{Ds,on}$
Switch turn-on loss	$\frac{1}{2} C_{oss} V_{sw}{}^2 f_{sw}$
Total rectifier diode loss	$V_{Df} * I_{D,avg} + I_{D,rms}{}^2 * R_D + V_d\, Q_{rr}\, f_{sw}$
Total HF Transformer loss	$I_{Lr,rms}{}^2 * R_{winding} + P_{C,limit}\, V_e$
Total boost inductor loss	$I_{in}{}^2 * R_{L,DC} + P_{C,limit}\, V_e$
Gate drive loss	$C_{iss} V_g^2 f_s$
Capacitor loss	$I_{cout,rms}{}^2 * R_{ESR}$

where

$I_{sw,rms}$ = Switch rms current, A

$R_{DS,on}$ = Switch drain-to-source on-state resistance, Ω

V_{sw}, = Switch average voltage during turn-off, V

f_{sw} = Switching frequency, Hz

C_{oss} = Switch output capacitance, F

$I_{D,rms}$ = Diode rms current, A

R_D = Diode turn-on resistance, Ω

$I_{D,avg}$ = Diode average current, A

V_{Df} = Diode forward voltage, V

$R_{winding}$ = transformer dc resistance, Ω

$I_{L,rms}$ = boost inductor rms current, A

R_L = Inductor DC resistance, Ω

$I_{Cout,rms}$ = Capacitor ripple rms current, A

R_{ESR} = Capacitor equivalent series resistance, Ω

$Pc,limit$ = core loss limit, mW/cm^3

Ve = Effective core volume, cm^3

$Ciss$ = Switch input capacitance, F

f_{sw} = Switching frequency, Hz

Vg = Switch driving voltage, V

V_d= Diode blocking voltage, V

Q_{rr}= Diode reverse recovery charge