# Analog Filtering of EEG signals in the Presence of Artifact Signals

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# Abstract

## Analog Filtering of EEG signals in the Presence of Artifact Signals

Kwabena Asamoah

Recovery of bio-electric signals, such as EEG, ECG, have been routinely done in the past via sophisticated numerical algorithms and extensive computing resources. Current works on filtering of EEG signals does not clearly reveal the electronic circuit operations by which the artifact signals can be obtained to serve as a reference signal for filtering operation. A technique to isolate the artifact signals mixed with intended bio-electric signals (i.e., EEG), by using analog circuit components has been proposed in the thesis. The artifact signal band is assumed to be separated from the intended signal bands.

The novelty of the approach lies in recovering the artifact signal from the mixture of contaminated biomedical signals and then re-using it to recover the intended signals. Prior knowledge about the artifact signal is not needed, except for demonstration of the principles through simulation work. Data base of CMOSP 18 technology available in the VLSI laboratory of Concordia University has been used for all simulations.

The use of recovered artifact signal as a reference signal for the filtering process by elimination of the intended signal, is presented in the thesis. All these operations were easily implemented with analog circuit components. Further work along this direction will be very useful in developing wearable electronic devices for communication of point-of-care health data from a human body, wirelessly to distant medical center locations for further processing. This is expected to provide relatively inexpensive solutions toward current day trend of wireless point-of-care electronic circuits and systems for public health monitoring.

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# List of Acronyms

| | |
|---|---|
| AC | Alternating Current |
| ANFIS | Adaptive Neuro Fuzzy Interference System |
| BPFA | Array of Bandpass Filters |
| BSS | Blind Source Separation |
| CMOS | Complementary Metal-Oxide Semiconductor |
| CMRR | Common Mode Rejection Ratio |
| COMPR | Compressor block |
| DC | Direct current |
| D_AMP | Difference Amplifier block |
| ECG | Electrocardiogram |
| EEG | Electroencephalogram |
| EGG | Electrogastrogram |
| EOG | Electrooculogram |
| EXPDR | Expander block |
| IA | Instrumentational Amplifier |
| IC | Integrated Circuit |
| ICA | Independent Component Analysis |
| L | Channel length of a MOS transistor |

| | |
|---|---|
| LMS | Least Mean Square |
| MOS | Metal Oxide Semiconductor |
| NF | Array of Notch Filters |
| NMOS | Negative channel MOS |
| OA | Ocular Artifact |
| OPAMP | Operational Amplifier |
| PFE | Partial Fraction Expansion |
| PMOS | Positive Channel MOS |
| RLS | Recursive Least mean Square |
| SSE | Sum of the Squared Error |
| S_AMP | Summing Amplifier block |
| W | Channel Width of a MOS transistor |
| VLSI | Very Large-Scale Integration |

# List of Symbols

| | |
|---|---|
| $C_{OX}$ | Channel Oxide Capacitance of a MOS transistor |
| $dB$ | Decibels |
| $H(s)$ | Transfer Function |
| $D(s)$ | Denominator |
| $N(s)$ | Numerator |
| $g_m$ | Transconductance |
| $V_{DD}$ | Positive Supply Voltage |
| $V_{SS}$ | Negative Supply Voltage |
| $V_{TH}$ | Threshold voltage of a MOS transistor |
| $Q_p$ | Quality Factor |
| $\omega$ | Frequency in radians |
| $\omega_n$ | Zero frequency |
| $\omega_p$ | Pole frequency |
| $\mu_n$ | Carrier mobility through the channel |
| $\alpha$ | Alpha |
| $\beta$ | Beta |
| $\delta$ | Delta |
| $\gamma$ | Gamma |

# Chapter 1

# Introduction

Electronic circuits and systems pervade the modern world in diverse ways. One of these areas is human health care. While human health was at the realms of scientists in biology, physiology and medicine, advent of computers ushered in significant collaborations of activities among the above fronts. The computational power could be efficiently exploited to process data about various electromagnetic signals that are generated within the human body. Physiological signals are a sub-class of these electromagnetic signals. These can be detected by special sensors that deliver electrical signals corresponding to the body signals. Once the knowledge of the electrical signals is obtained, scores of electronic signal processing principles could be used to diagnose the health conditions of a human subject. This area of activities exploiting electronics in studying physiological signals forms the basis of the subject of bioelectronics and biomedical engineering.

An important aspect of working with bioelectronics signals is the availability of human subjects, electronic equipment, computers all in neighbouring locations. Advent of sub-micron transistors technology has led to the development of electronic devices that could be positioned inside a human body and communicate the status of the physiological signals inside the body to electronic and computing peripherals that are positioned outside the body. Since the sensors can be located inside a human body, the possibility of analysing the signals from a distance by using well-known radio communication principles exists. This is the underlying principle of point of health care systems. The bulky electronic and computing machineries need not be adjacent to the human subject whose body signals are the subject of investigation.

Among the various physiological signals, a sub-class that is electrical by nature can be designated as EXG, where **E**→ Electro, **X**→Gastro or, Cardio or, Retino or, Oculo or, Encephalo, **G**→ Graphic [1]. When we are interested in only one signal from the above list, the others could coexist as disturbances. The signal of interest is referred to as the 'intended' signal, while the disturbing signals are named as artifact signals. In this thesis, EEG signals have been chosen as the intended signal.

Physiological and non-physiological artifacts form the major types of artifact signals depending on the sources of generation. Physiological artifacts are mainly caused by biological activities from the human body such as eye movement and blinking, cardiac potential, muscular potential from the muscle activity, sweating and others [2]. Non-physiological artifacts are other interferences generated outside the human body, which includes power line noises, electromagnetic noises from the electrical components, etc. Figure 1.1 [3] present the summary of some of the various artifact signals that interfere with the EEG signals.

| Artifact types and sources | | | | | | |
|---|---|---|---|---|---|---|
| Physiological/internal | | | | Extra-physiological/external | | |
| Ocular | Cardiac | Muscle | Others | Instrumental | Interference | Movement |
| Eye blink<br>Eye movement<br>Eye flatter<br>REM sleep | ECG pulse | Chewing<br>Swallowing<br>Clenching<br>Sniffing<br>Talking<br>Scalp contraction | Gloss kinetic<br>Skin<br>Respiration | Electrode<br>Displacement and pop-up<br>Cable movement<br>Poor ground | Electrical<br>Magnetic<br>Sound<br>Optical<br>EM waves | Head movement<br>Body movement<br>Limbs movement<br>Tremor<br>Other movements |

Figure 1. 1. Artifact components in EEG signals [3]

### 1.1: Existing Practices for Recovery of EEG signals

The subject of monitoring and analyzing electrical signals generated in human brains (Electroencephalography, EEG) has been of interest to scientists and medical professionals to quantify the state of consciousness such as sleep, and to the study of neurological disorders such as epilepsy, since nearly one hundred years [4]. The work has traditionally been carried out in well established hospitals with expensive computing resources and human specialists. The EEG signals are invariably contaminated by the presence of electrical signals arising out of parts of the human body other than the brain. As mentioned earlier, these are termed artifact signals. The artifact signals are stochastic in nature and hence, cannot be suppressed effectively by a frequency selective system, such as bandpass filters. Hence, other alternative techniques much be adopted to suppress the artifact signals present in the biomedical signal of interest. Fig. 1.2(a) [5] represent the general overview of the artifact removal techniques.

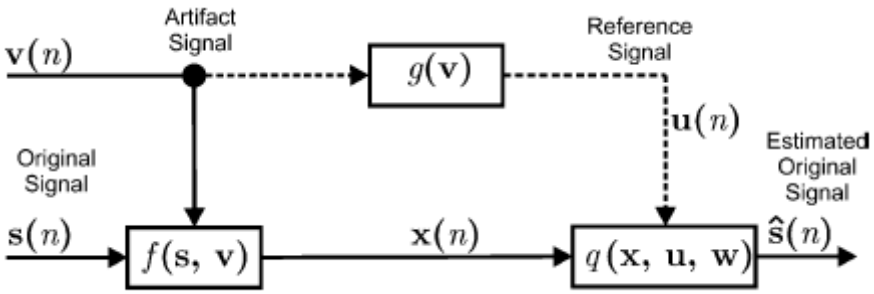



Figure 1. 2 (a). General framework of artifact removal [5]

In [5], the signal x(n) recorded during an experiment is a combination of the original desired signal s(n) contaminated with the artifact signal v(n). The function f represents as to how the two signals are combined to produce the signal at the recording site. This leads to tractable problem formulations as [5],

$$x(n) = s(n) + v(n) \tag{1.1}$$

Therefore, Fig.1.2(a) evolves to Fig.1.2b). Label (i) depicts the case when a reference signal u(n) is used to estimate v(n) (for instance, adaptive filtering) and (ii) the case when v(n) is estimated directly from x(n) (for example, blind source separation techniques) [5].

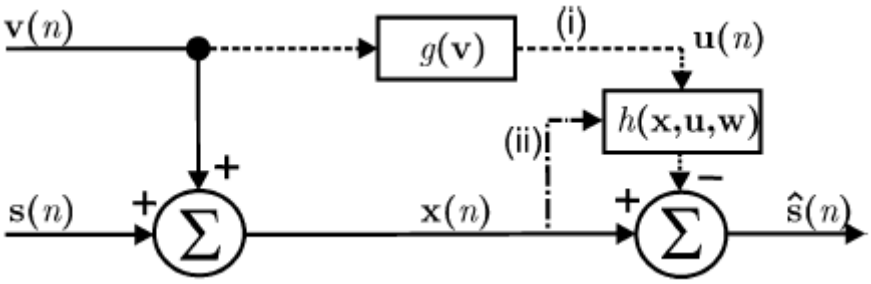



Figure 1. 2(b). Linear framework of artifact removal [5]

The use of adaptive cancellation of interfering signals using analog circuits and digital computer interface have been elaborated and demonstrated over fifty years ago [6,7]. Extensive research about the removal of artifact signals has been (and are still being) carried out by many interested researchers [2]– [8]. The other approaches used by these researchers involved the use of numerical algorithms such as regression [2], [3]-[9], and blind source separation [2]-[3], together with the deployment of mixed mode digital and analog signal processing sub-systems and adaptive filtering techniques [2], [3]-[8]. A brief review of these techniques in EEG data processing is presented below.

### 1.1.1: Regression algorithm

Regression analysis is a traditional way of identifying artifact samples and then removing sample that do not belong to the model. Observed artifact contaminated EEG signal and an artifact reference signal are common methods for removing some physiological artifacts such as ocular artifacts. The procedure includes estimating and removing the proportion of EOG components that appear in EEG signal using a least square criterion. The estimation process of EOG components using the determined coefficients is performed either in the time

domain or in the frequency domain. However, such regression analysis often fails when there is no reference channel available. In addition, EEG signal being a nonlinear and non-stationary process, linear regression is not the best choice in such application. Moreover, it can only be used to treat few particular types of artifacts, not all types.

### 1.1.2: Blind source separation

Blind source separation (BSS) is one of the most used methods, which focuses on the extraction the individual unknown source signals from their mixtures and possibly to estimate the unknown mixing channels using only the information within the mixtures observed at the output of each channel with no, or very limited, knowledge about the source signals and mixing channel.

Independent component analysis (ICA) is one of the techniques mostly used BSS in biomedical data analysis [2]. ICA isolates the noise from the EEG signals by decomposing signals into several independent components depending on the statistical independence of the signals. A standard linear ICA model is defined as,

$$\mathrm{x(t)} = \mathrm{A.\,s(t)} \tag{1.2}$$

The goal of the ICA algorithm is to retrieve the original sources $\mathrm{s(t)}$ from the observations $\mathrm{x(t)}$ by finding the estimation of A inverse matrix ($\mathrm{A^{-1}} = \mathrm{W}$) such that,

$$\mathrm{y(t)} = \mathrm{Wx(t)} \tag{1.3}$$

Fig. 1.3 presents the fundamental model of the ICA principle.

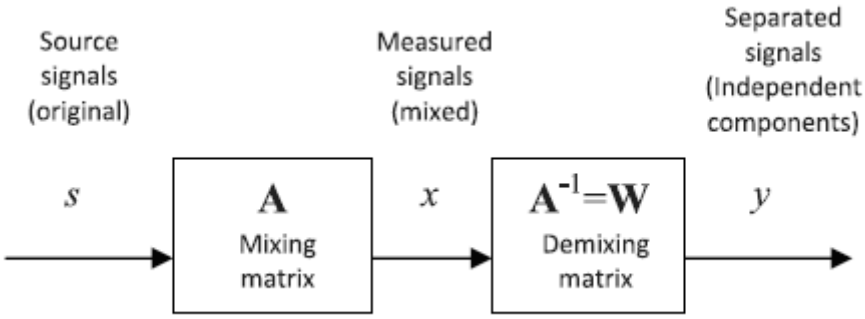



Figure 1. 3. Schematic of ICA [2]

One of the advantages of ICA is that it does not require additional signals for reference, since the algorithm itself does not require prior information. One of the major limitations is that the independent sources must be non gaussian in which the sources are assumed to be statistically independent. Also, ICA requires a manual visual inspection that makes it time consuming.

### 1.1.3: Adaptive filtering Methods

Conventional filtering methods are not very promising since they may attenuate not only the artifact signal component, but also the EEG signal due to overlapping frequency spectra [2]. Adaptive filtering can be used to overcome the time invariance characteristics of conventional filtering techniques. The main aim of adaptive filtering is to predict the cluster of artifact signal in the primary signal (i.e., contaminated biomedical signal) and then subtract that artifact from it. The recovered artifact signal used for adaptive filtering is referred to as a reference signal [2]. Technically, the reference signal is picked up by an additional channel that directly refers to the artifact sources. A reference input separated from the primary input is used to realize the noise canceller system (Fig. 1.4). Likewise, a reference signal is used for adaptive filtering operation reported in [6], [10].

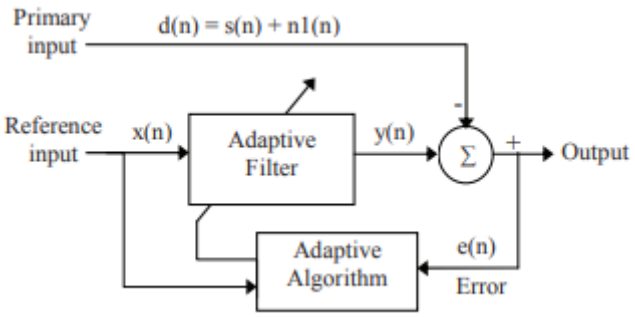



Figure 1. 4. Noise canceller system using adaptive filtering [2]

Adaptive filtering algorithm for noise removal can be classified in two categories [2]. These are linear and non-linear algorithms.

**a) Linear algorithm**

The linear algorithm mostly uses least mean square (LMS) algorithm for the adaptive filtering. The advantages of LMS are its computational simplicity, low memory usage and ease of implementation. LMS algorithm has the ability to adjust the filter coefficients to minimise the error. The recursive least mean square (RLS) is another algorithm that can be adopted in a linear algorithm for adaptive filtering. RLS algorithm uses a matrix operation which requires higher computational complexity, unlike LMS algorithm. This makes the implementation of RLS algorithm more complex and difficult to implement than the LMS algorithm.

**b) Non-linear algorithm**

The adaptive neuro fuzzy interference system (ANFIS) is one of the major categories of the non-linear algorithm [2]. ANFIS is a combination of a fuzzy interference system and artificial neural network. ANFIS comprises of five layers. ANFIS minimizes the sum of the squared error (SSE) by using hybrid learning algorithm, which combines least squares and back propagation gradient descent methods together.

In adaptive filtering of ocular artifact signals from human EEG [8], the authors focus on the removal of Ocular artifacts from EEG data by deploying adaptive segmentation of each segment of the signal to adaptive filtering. Estimates of ocular artifacts (OA) are obtained by suitably scaling the EOG. The OA estimates are then subtracted from the contaminated EEGs to yield artifact-free EEG signals using the UD algorithm [8]. UD algorithm is a numerically stable formulation of the RLS algorithm which is preferred to the LMS because of its superior convergence time, thus enabling it to cope better with different OAs each of which requires a different optimum set of the coefficient for effective removal.

The algorithm is used with MATLAB to separate the EEG signals from the artifact signals. Preliminary observations are carried out on vertical and horizontal EOG signals with suitably placed electrodes (Fig. 1.5). These are used in MATLAB simulation to recover the EEG signal data (Fig.1.6 on the next page).

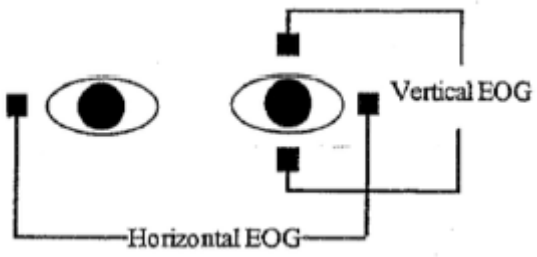



Figure 1. 5. The placement of the electrodes for recording of VEOG and HEOG [8]

Availability of a reference signal for adaptive filtering is not plausible in a point of care scenario. The subject is not supposed to be present physically in a medical clinic or hospital room to enable/assist in the extraction of the reference artifact signal. The subject will most likely be wearing a device which will sense the EEG signals of interest mixed with other artifact signals, such as EOG, ECG, and extraneous signals like motion signal due to walking, and the like.

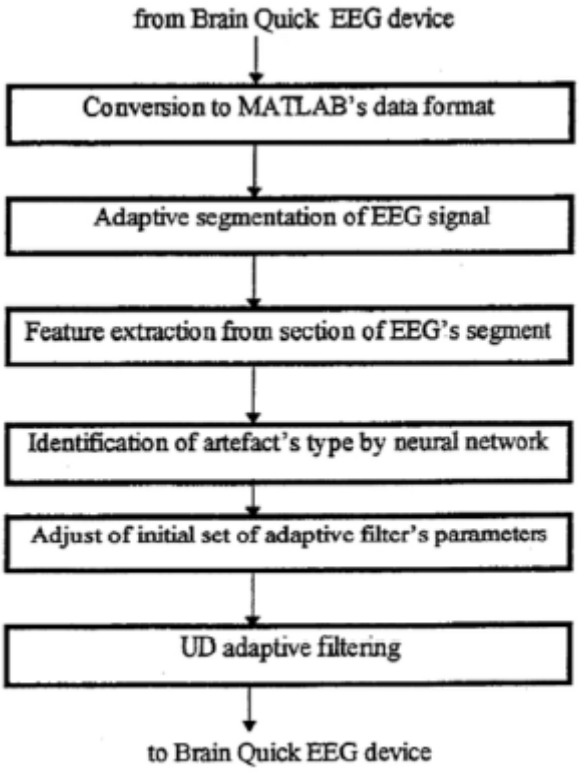



Figure 1. 6. Algorithm of EEG data pre-processing [8]

### 1.2: Objectives and Direction of Current Research

Artifact signals usually overlap with the EEG signals in both the spectral and temporal domains, which makes it difficult to use simple filtering or straight forward signal processing techniques [3]. From the previous studies, we know that a lot of algorithms have been developed in biomedical signal processing. Our objective is to develop a biomedical device which can be used for EEG signal detection and study as in a point of care system (i.e., mobile device in which a human subject can wear on the body). This will be achieved by using analog (or analog plus digital mixed mode) circuit techniques and principles. In our research, we will be proposing a system and provide results to give us the confidence that in near future we can create a device which can be fabricated in an integrated circuit technological laboratory and eventually distribute the knowledge and findings to industries who might be interested in developing the device into an industrial product.

The use of adaptive cancellation of interfering signals using analog circuits and digital computer interface with special impetus on EEG signal processing have been elaborated and demonstrated over fifty years ago [6,7]. Here, we embark on using a not yet published principle to recover the intended signal (i.e., EEG) mixed with artifact signals by separating the artifact signals from the mixture. This is made possible by passing the mixed signals through several notch filters where the notch filters are tuned to the respective intended signals. Thus, the system operates entirely in analog domain. A block diagram of our proposed system is shown in Fig. 1.7. A brief explanation of the operation of the several sub-systems follows. More details are provided in the upcoming chapters of the thesis.

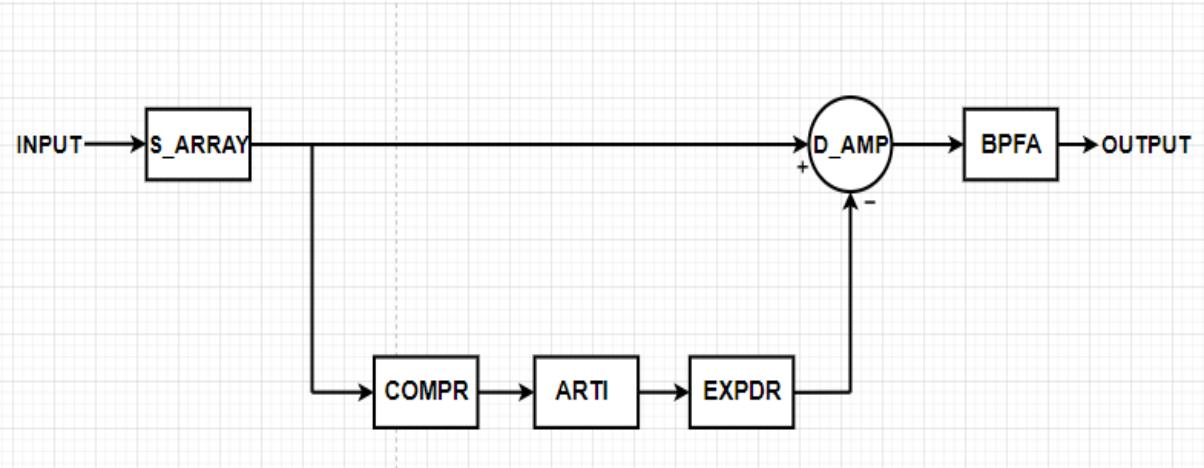



Figure 1. 7. The proposed system

S_ARRAY: This sub-block presents sensor devices (i.e., an array of EEG recording electrodes) mounted on a human mannequin. This node serves as the spot where the intended signal (i.e., EEG) and the artifact signals are combined as a natural mixture of physiological signals. In our experimental verification of the proposed system, we replace this function by a summing amplifier.

COMPR: This is a compressor system. The purpose of this unit is to compress high valued signals relative to low and moderate valued signals in the mixture of the intended and the

artifact signals. In reality, most of the artifact signals happens to be several times (10 or more) higher than the intended signals.

ARTI: This unit separates the artifact signals from the intended signals by utilizing of a bank of appropriate notch filters.

EXPDR: The expander block compensates for the effect of the COMPR on the magnitudes of the artifact signals. The output from the EXPDR is thus the artifact signals originally present with the intended signals in the sensor devices (S_AMP).

D_AMP: This functions as a difference amplifier which subtracts the artifact signals from the output of the S_AMP, thereby delivering the intended signals only.

BPFA: This contains an array of bandpass filters to selectively deliver the group of intended signals, present in the S_AMP to the OUTPUT. For good tracking performance, the bandpass filters are realized from the same group of notch filters present in the ARTI block.

### 1.3: Outline of the Thesis

The thesis is structured as given below.

Chapter 2 represents the basic theory and analytical model of several kinds of second order filters (i.e., low pass, high pass, band pass and notch filters). This chapter mainly focuses on the numerical analysis and implementation of a second order notch filter. The detailed effect of how the characteristics of the notch filter affect the signals passing through the notch system is also presented. Furthermore, a typical application of notch filters in processing of biomedical signal is elaborated in this chapter.

In Chapter 3, the detailed design and implementation of the various amplifiers (i.e., operational amplifier, summing amplifier, difference amplifier etc.) used in the proposed work are presented. This chapter focuses on the realization of passive resistors using MOS

transistors, which includes the implementation of high valued resistors (i.e., in giga-ohms range). Finally, the overall performance of these various amplifiers and MOS resistors using CMOS180 technology are also included in this chapter for validation purposes.

Chapter 4 focuses on the detailed analysis and implementation of the artifact recovery system used to retrieve the reference band of signals for adaptive filtering. The designs of the notch filters are also presented. Moreover, analysis of typical pure and contaminated EEG data is included in this chapter. This helps us to knows the various bands (i.e., Delta, Theta, Alpha, Beta band, etc.) present in the EEG data. Furthermore, the design of the compressor and expander circuits are also elaborated.

Chapter 5 present the verification of the proposed work using the same CMOS180 technology. Furthermore, this chapter also focuses on the generation of the ECG signal as an artifact signal to test the performance of the proposed system. The design and implementation of bandpass filters using the same notch filters presented in Chapter 4 to isolate the individual EEG bands are presented.

The thesis concludes with summary of the work done and some suggestions for possible future work in Chapter 6.

# Chapter 2

# Review of Notch Filter

In this chapter, we provide a general introduction to analog filters with special impetus on notch filters. The notch filters are the principal components of the adaptive filtering system that is the subject matter of the research work reported in this thesis.

### 2.1: Analytical Model of Analog filters

Analog filters are frequency selective networks that allow certain band of frequencies to pass and attenuate other frequencies. Filters as a linear system can be easily analysed and synthesized using network transformation in frequency domain. In continuous time domain, Laplace transform technique can be used to model the transfer function.

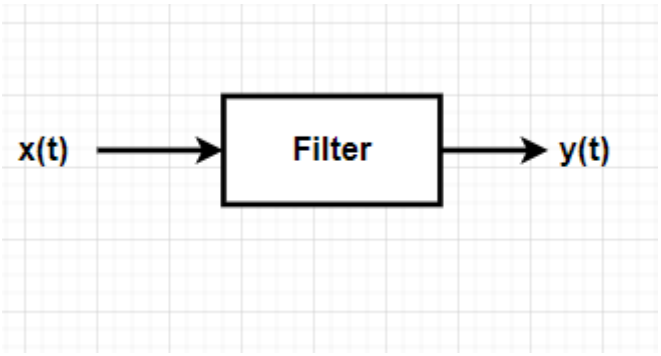



Figure 2. 1. Schematic representation of an analog filter

The schematic representation of a filter system in continuous time domain is shown in Figure 2.1. The filter transfer function can be defined in terms of Laplace transformed excitation X(s) and zero state response Y(s).

$$H(s) = \frac{L[y(t)]}{L[x(t)]} = \frac{Y(s)}{X(s)} = \frac{N(s)}{D(s)} = \frac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_0}$$

where $m \leq n$ for any realizable physical network, $N(s)$ and $D(s)$ are the numerator and denominator polynomial respectively and n is the order of the filter.

Filters are classified according to the filtering function they perform. If our aim is on the magnitude or attenuation characteristics, then we can categorize them as low pass, high pass, band pass and band reject filters. In some applications, if our consideration is only on the phase or delay specifications with no change in magnitude, the filters are considered as all pass networks or delay equalizers.

Table 2.1 shows the analytical expressions for the numerators $N(s)$ of standard second order filter transfer functions (biquads) and is different for different kinds of filters [11]. The denominator function $D(s)$ is the same for all filter types and given by

$$D(s) = s^2 + \left({\omega_p}/{Q_P}\right)s + {\omega_p}^2 \tag{1.2}$$

where $\omega_p$ is called as the pole frequency and $Q_P$ as the pole-Q or quality factor.

Table 2. 1. Standard biquad transfer functions

| Type of Filters | N(s) |
|---|---|
| Low pass | $H_o{\omega_p}^2$ |
| High pass | $H_o s^2$ |
| Band pass | $H_o\left({\omega_p}/{Q_P}\right)s$ |
| Band stop | $H_o(s^2 + {\omega_n}^2)$ |
| All-pass | $s^2 - \left({\omega_p}/{Q_P}\right)s + {\omega_p}^2$ |

## 2.2: Introduction to Notch Filters

In this section, we will introduce the characteristics of notch filters. The property of notch filter is to eliminate a specific frequency among several frequencies present in a complex signal. In biomedical applications, the notch filter is used principally to eliminate the power line frequency signal. In general, the notch filter could be a broadband elimination filter. In that case we do not call it as a notch filter but rather as band stop or band reject filter. Thus, a narrow band reject filter can be called a notch filter and wide band reject filter will be referred to as a band reject filter.

## 2.3: Seconder Order Notch Filter

The transfer function of a second order notch filter is given by

$$H(s) = \frac{s^2+{\omega_n}^2}{s^2+\frac{\omega_p}{Q_P}s+{\omega_p}^2} \tag{2.2}$$

where $\omega_n$ is the zero frequency of the filter. The relationships of the pole frequency and the zero frequency bring about the three notch filter characteristics which are standard notch, lowpass notch and high pass notch filter. Standard notch is achieved when the $\omega_p$ is equal $\omega_n$. In the notch when $\omega_n$ is less than $\omega_p$ the filter is known as high pass notch. If the $\omega_n$ is higher than $\omega_p$, the filter is referred as lowpass notch filter. These characteristics are illustrated in Figure 2.2 [12] on the next page.

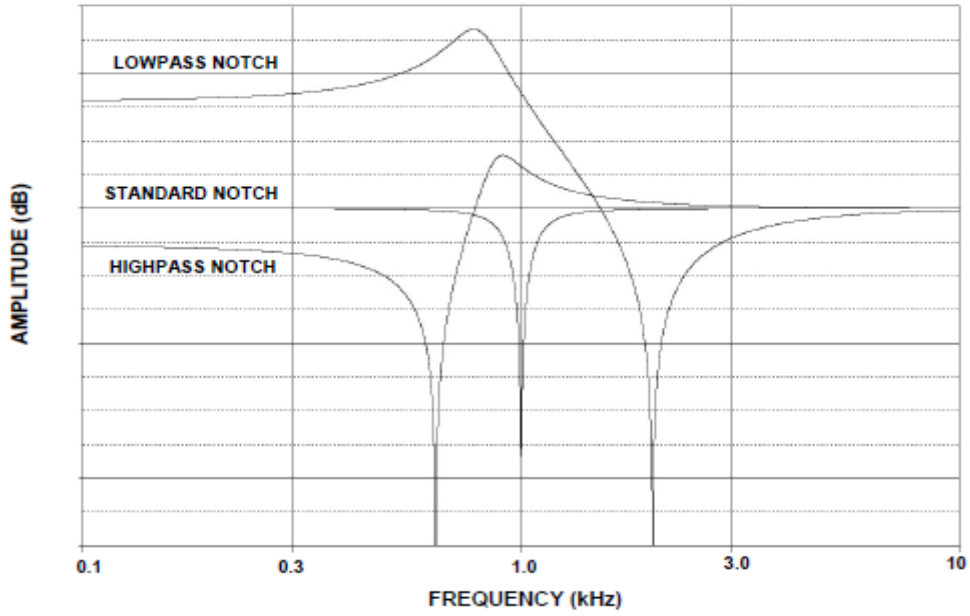



Figure 2. 2. Types of notch filters [12]

For example, a seconder order standard notch for a 60Hz power line will have the transfer function,

$$H(s) = \frac{s^2 + (2\pi\times60)^2}{s^2 + 60\pi s + (2\pi\times60)^2} \tag{2.3}$$

assuming $Q_p = 2$.

For instance, if a signal at frequency $\omega_1$ is input to a standard notch filter with notch frequency of $\omega_n$, the overall output of the notch filter in frequency domain will be given by (assuming $\omega_n = \omega_p$)

$$Y_1(s) = \left(\frac{\omega_1}{s^2+{\omega_1}^2}\right) \times \left(\frac{s^2+{\omega_n}^2}{s^2+\frac{\omega_n}{Q_P}+{\omega_n}^2}\right) \tag{2.4}$$

Using the principle of partial fraction expansion (PFE) [14], the overall output of the standard notch filter for a single frequency input at $\omega_1$, given by

$$Y_1(s) = \frac{As}{s^2+{\omega_1}^2} + \frac{B}{s^2+{\omega_1}^2} + \frac{Cs}{s^2+0.5\omega_n s+{\omega_n}^2} + \frac{D}{s^2+0.5\omega_n s+{\omega_n}^2} \tag{2.5}$$

The time domain response associated with $Y_1(s)$ in (2.5) will be [13],

$$y_1(t) = (A\cos\omega_1 t + B\sin\omega_1 t + Ce^{-\frac{1}{4}\omega_n t}\cos\left(\frac{\sqrt{15}}{4}\omega_n t\right) + \frac{4\sqrt{15}}{15}De^{-\frac{1}{4}\omega_o t}\sin\left(\frac{\sqrt{15}}{4}\omega_n t\right) \quad (2.6)$$

where

$$A = \frac{0.5\omega_n{\omega_1}^3 - 0.5{\omega_n}^3\omega_1}{{\omega_1}^4 - 1.75{\omega_n}^2{\omega_1}^2 + {\omega_n}^4} \quad (2.7a)$$

$$B = \frac{{\omega_1}^5 - {\omega_n}^2{\omega_1}^3 + {\omega_n}^2{\omega_n}^2\omega_1 + {\omega_n}^2{\omega_1}^3}{{\omega_1}^4 - 1.75{\omega_n}^2{\omega_1}^2 + {\omega_n}^4} \quad (2.7b)$$

$$C = -\frac{0.5\omega_n\omega_1({\omega_1}^2 - {\omega_n}^2)}{{\omega_1}^4 - 1.75{\omega_n}^2{\omega_1}^2 + {\omega_n}^4} \quad (2.7c)$$

$$D = \frac{{\omega_n}^2{\omega_1}^3 - {\omega_n}^2{\omega_1}^3 - 0.75{\omega_n}^4\omega_1 + \omega_1{\omega_n}^4}{{\omega_1}^4 - 1.75{\omega_n}^2{\omega_1}^2 + {\omega_n}^4} \quad (2.7d)$$

For a standard notch filter at 60 Hz (i.e., $\omega_p = \omega_n = 2 \times \pi \times 60\,\text{rad/secs}$) and setting input signal values at $\omega_2$ equal to $2 \times \pi \times 60\,\text{rad/secs}$ and $\omega_1$ equal to $2 \times \pi \times 5\,\text{rad/secs}$, and $2 \times \pi \times 10\,\text{rad/secs}$ successively, we can obtain the time domain responses of the filter using MATLAB. The graphical results are shown in Figures 2.3 (a) and (b), respectively. The red lines correspond to the input signal at 60 Hz (i.e., the null frequency). The output at the notch frequency, (i.e., 60Hz) remains nearly zero, as expected.

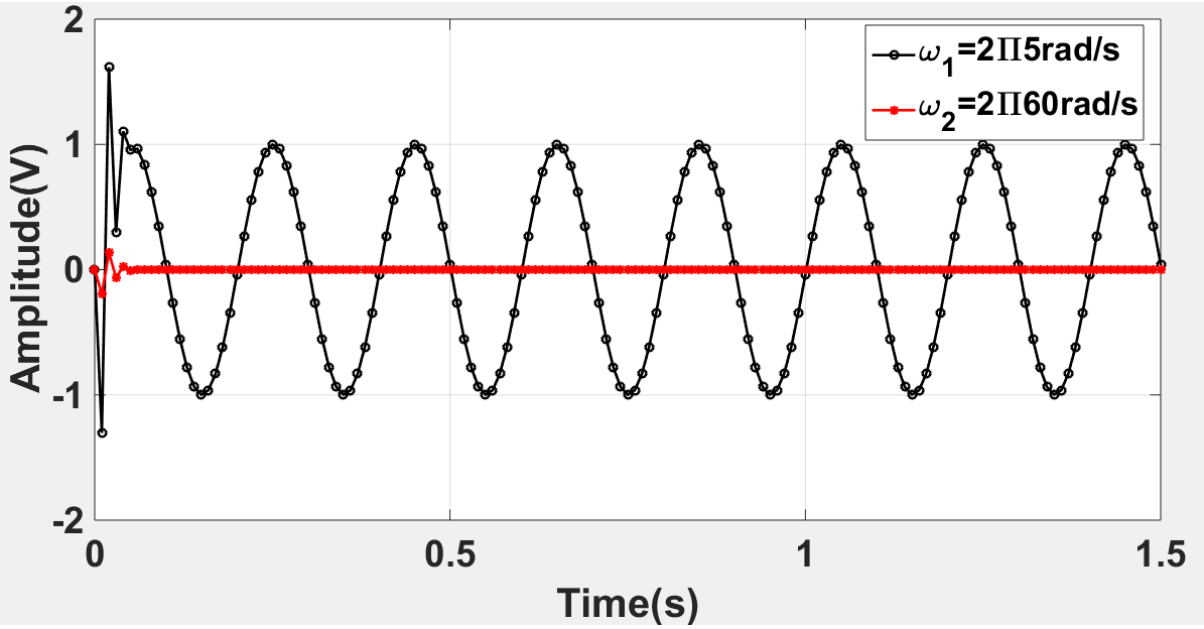



Figure 2. 3(a). Output of notch filter

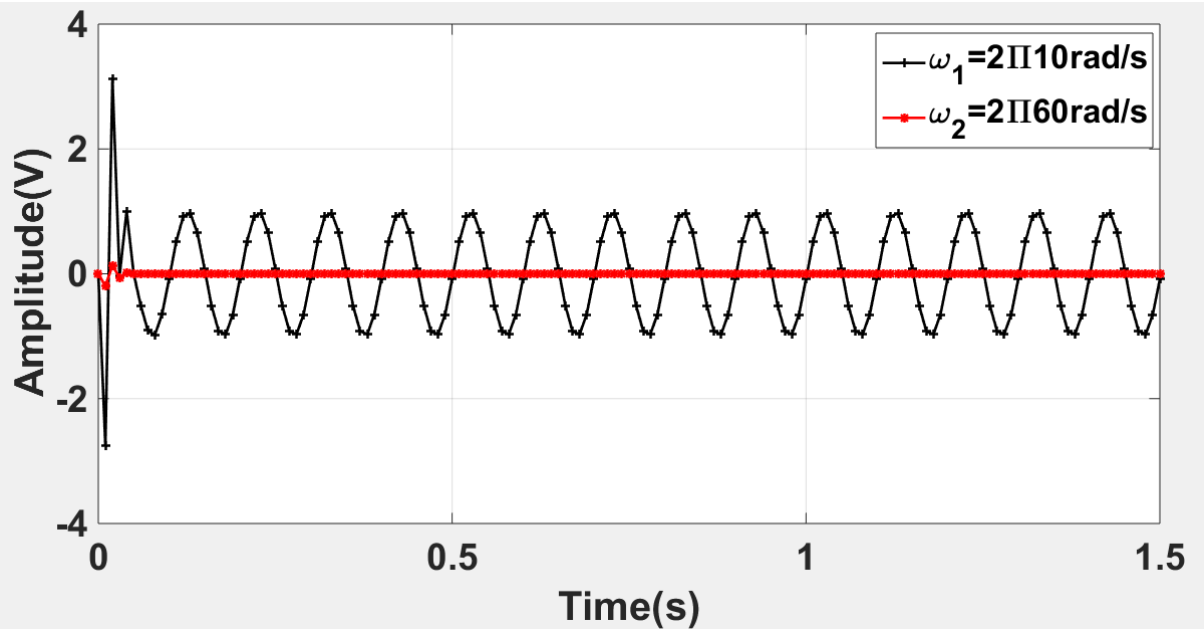



Figure 2. 3(b). Output of the notch filter

Thus, when input signal frequency is equal to the notch frequency, the signal is completely suppressed. However, if the signal frequency is not equal to the notch frequency, the signal is passed through the notch filter.

## 2.4: Further Characteristics of a Notch Filters

We have already seen that all input signals frequencies that are not equal to the notch frequency, the signals are transmitted. However, there are some changes in their magnitudes and in phases. These changes are small. For simple analysis we assume such changes as negligible. Figures 2.4(a)-(b) show the relative characteristics of a second order notch filter with different choices of $Q_p$ values. The notch frequency is 60Hz ($2\pi \times 60\,\mathrm{rad/s}$). For high $Q_p$ (i.e., 10, 20) the phase angle remains close to zero over wider frequency spans on either side of the null frequency. Similarly, the magnitude remains close to 1 (i.e., zero loss) over wider frequency spans on either side of the null frequency with higher values of $Q_p$. This is closer to an ideal behaviour.

Tables 2.2 and 2.3 present several numerical values of the phase angles associated with the graphs in Fig. 2.4(a) – (b).

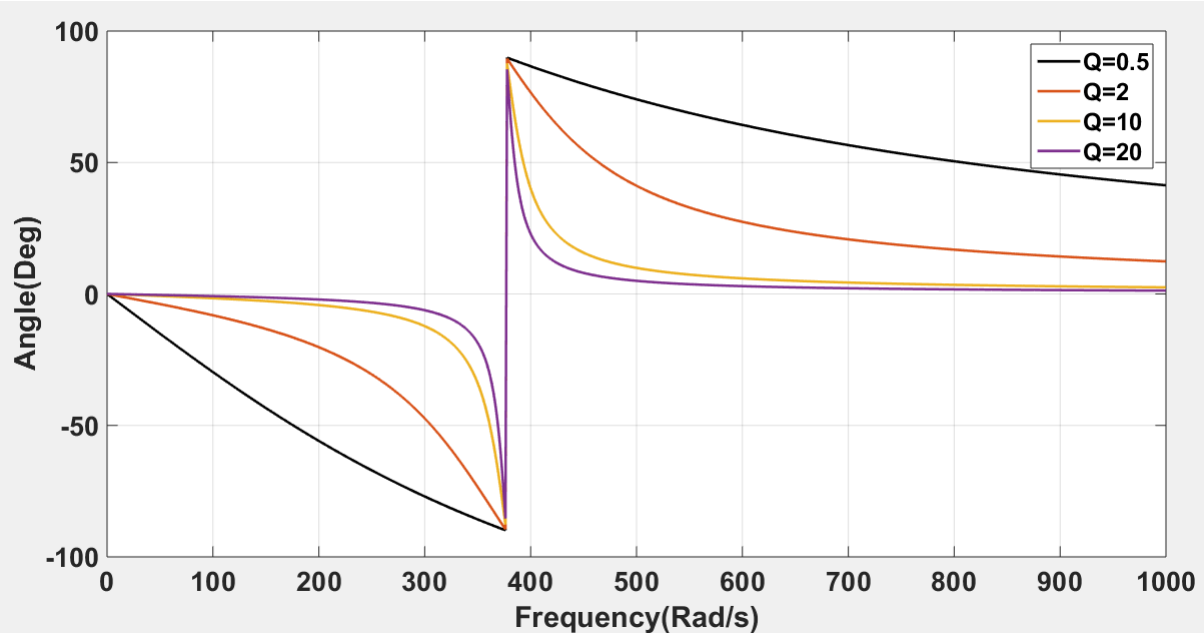



Figure 2. 4(a). Phase response of notch filter (60Hz) at different $Q_P$ values

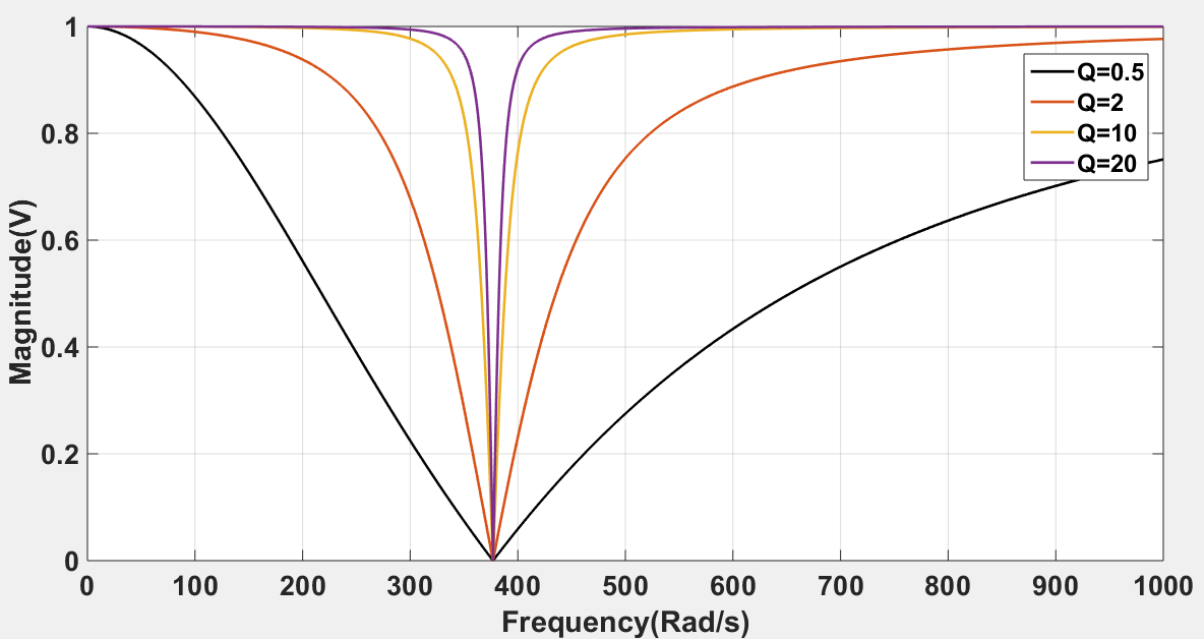



Figure 2. 4(b). Magnitude response of notch filter (60Hz) at different $Q_P$ values

Table 2. 2. Phase angle for different values of $Q_P$ ($f_0 = 60$Hz)

| Frequency (Hz) | Phase Angles in degrees (°) | | | |
|---|---|---|---|---|
| | $Q_p = 0.5$ | $Q_p = 2$ | $Q_p = 10$ | $Q_p = 20$ |
| 10 | -19.23 | -4.80 | -0.90 | -0.48 |
| 20 | -38.10 | -11.10 | -2.20 | -1.10 |
| 30 | -53.50 | -18.70 | -3.60 | -1.82 |
| 40 | -69.20 | -30.60 | -6.90 | -3.40 |
| 50 | -78.90 | 56.60 | -16.90 | -8.60 |
| 60 | $\pm$89.90 | $\pm$88.20 | $\pm$81.4 | $\pm$78.20 |

| | | | | |
|---|---|---|---|---|
| 70 | 82.50 | 58.20 | 17.9 | 9.20 |
| 80 | 70.80 | 35.20 | 8.70 | 4.40 |
| 90 | 67.00 | 30.40 | 6.85 | 3.40 |
| 100 | 61.80 | 25.10 | 5.00 | 2.60 |

Table 2. 3. Magnitudes for different values of $Q_P$ ($f_0 = 60$Hz)

| Frequency (Hz) | Magnitude (V) | | | |
|---|---|---|---|---|
| | $Q_p = 0.5$ | $Q_p = 2$ | $Q_p = 10$ | $Q_p = 20$ |
| 10 | 1.00 | 1.00 | 1.00 | 1.00 |
| 20 | 0.80 | 1.00 | 1.00 | 1.00 |
| 30 | 0.60 | 0.90 | 1.00 | 1.00 |
| 40 | 0.40 | 0.89 | 0.98 | 0.99 |
| 50 | 0.20 | 0.55 | 0.90 | 0.98 |
| 60 | 0.00 | 0.00 | 0.0001 | 0.0002 |
| 70 | 0.20 | 0.50 | 1.00 | 1.00 |
| 80 | 0.30 | 0.80 | 1.00 | 1.00 |
| 90 | 0.40 | 0.90 | 1.00 | 1.00 |

| | | | | |
|---|---|---|---|---|
| 100 | 0.50 | 0.90 | 1.00 | 1.00 |

The graphs in Fig. 2.4(a)-(b) show that signals away from the null frequency do not suffer substantial changes in magnitude or phase. So, these pass through the system unaltered. This can help estimating the range of signal frequencies that remain unaltered after passage through the notch filter. This objective is achieved by the ARTI subsystem shown in Fig.1.7 of the thesis. Details of the ARTI subsystem will be presented in Chapter 4 of the thesis.

### 2.5: Typical Application of a Notch Filter

In most biomedical signal processing, notch filters are mostly used in the elimination of 50Hz/60Hz power line frequency signal especially in the processing of electrocardiogram and electroencephalogram data for clinical purposes. Power line noise get easily picked up through electrode cables, electrical devices and the patient being monitored [15].

For instance, Fig.2.5 demonstrates the use of a 4$^{th}$ order LMF90 elliptic notch filter [15] to suppress the 60Hz power line frequency signal present in a typical EEG data.

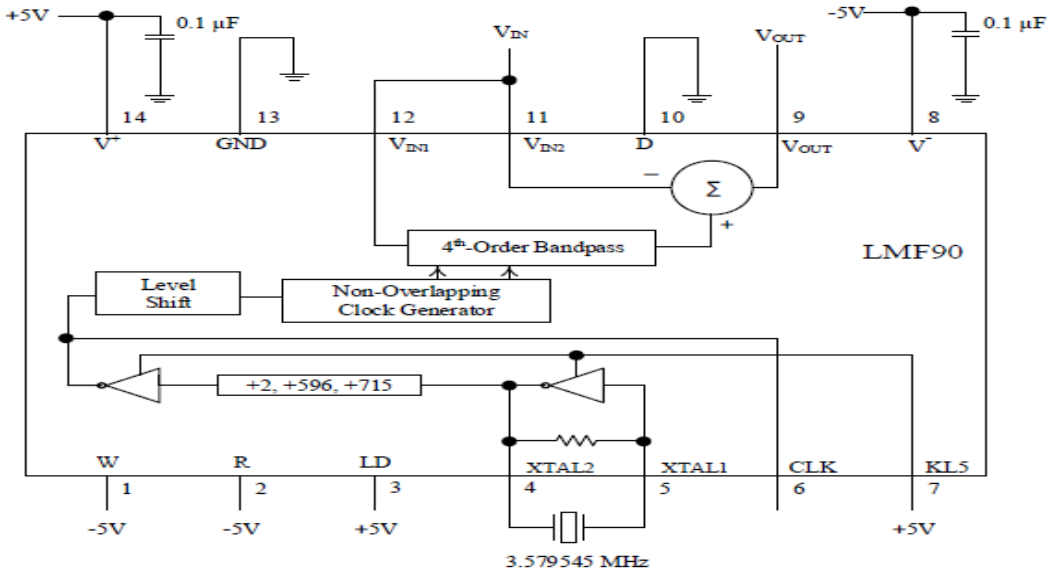



Figure 2. 5. Internal structure of LMF90 [15]

In contrast to eliminating the artifact signal data prior to the intended signal data with the subject in a hospital setup, it is possible to separate the artifact signal from the intended signal by notch filtering and then re-applying the artifact signal in the adaptive filtering loop to recover the intended signal. The recovered signal (i.e., EEG bands) can be Delta, Theta, or Alpha band etc. (as shown in Table 2.4[18]). The detailed design and analysis of how the notch filters are used in the proposed system (Fig.1.7) to retrieve the desired signals of interest will be addressed in the upcoming chapters of the thesis.

Table 2. 4. EEG rhythms with their corresponding frequency

| Rhythm | Delta | Theta | Alpha | Beta | Gamma |
|---|---|---|---|---|---|
| Frequency (Hz) | 0.5 - 4 | 4 - 8 | 8 -13 | 13 - 30 | $\geq 30$ |

**2.6: Conclusion**

In this chapter, we introduced the basic features and analytical characteristics of a notch filter and its utility in isolating a certain signal from other signals. We also elaborated as to how different $Q_p$ values of the notch filter affect the phase of the signals at frequencies other than the notch frequency. This will help us to develop a novel filtering system to eliminate the artifact signals in the mixture of desired and artifact signals. In the coming chapters, the analysis and implementation of the various subsystems shown in Fig. 1.7 using the modern CMOS technological process (TSMC 0.18mircon CMOS) will be addressed.

# Chapter 3

# Amplifiers in the Proposed System

The system proposed in Chapter 1 has several amplifiers. All these special-use amplifiers are realized using a basic Operational Amplifier (OPAMP) with additional circuitry to meet the special requirements. In this chapter, we will present the case of a typical OPAMP that has been introduced in [19] with application to EEG signals processing. This chapter also focuses on the analysis and design of the various typical amplifiers using CMOS180 technology. The simulation results of the various amplifiers are included to validate and confirm their operations.

### 3.1: Operational Amplifiers

The operational amplifier is the principal component in designing and implementing most of the analog circuits for signal processing. Some of the analog signal processing functions are amplification, integration, summation, etc. In this section, we will elaborate on the architecture, characteristics, and implementation of general two-stage operational amplifiers. The general architecture of operational amplifiers mostly consists of a differential stage ($A_1$), gain stage($A_2$), and sometimes a unity gain output ($A_3$) stage as illustrated in Figure 3.1. Generally, operational amplifiers are designed to have very high differential input resistance and very low output resistance.

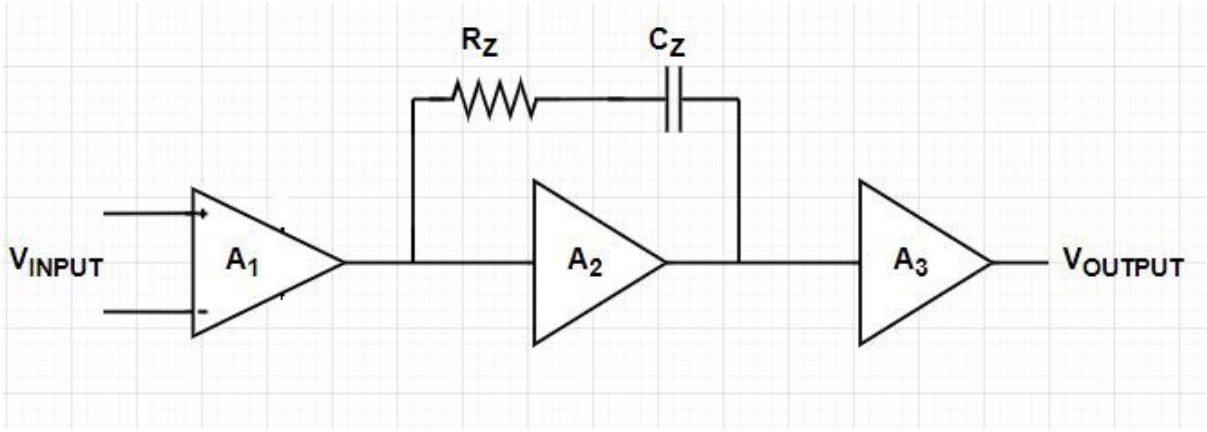



Figure 3. 1. Schematic representation of a two-stage OPAMP

The differential stage is mostly designed and implemented to have a high Common Mode Rejection Ratio (CMRR) to reject any interference signal common between the input terminals before it is further subjected to the gain stage for amplification. The introduction of the resistor $(R_Z)$ and capacitor $(C_Z)$ connected between the output of the differential stage and the gain stage output represents a compensational circuit for phase stability of the operational amplifiers.

**3.2: Design of the Operational Amplifier (OPAMP)**

In this section, we are going into the detailed design and implementation of the operational amplifier used in the proposed work, as has been addressed in [17]. The operational amplifier is implemented and simulated in CMOS18 (180 nano meter) technology. The schematic representation of the operational amplifier is shown in Figure 3.2 [17]. The operational amplifier comprises of three parts that include the bias circuit, the differential input stage, and the output gain stage. The OPAMP works from the voltage supplies $V_{DD} = +900\text{mV}, \text{and } V_{SS} = -900\text{mV}$. Table 3.1(a)-(e) present the AC parameters of the transistors M2, M4, M6, M9 and M11, respectively. These parameters are needed to calculate the gains of the differential input stage and of the output stage of the OPAMP. We denote the

transconductance and the drain to source resistance of the MOS transistor $M_i$, respectively (i = 1,2,3 ….22) by $gm_i$ and $r_{dsi}$ , respectively.

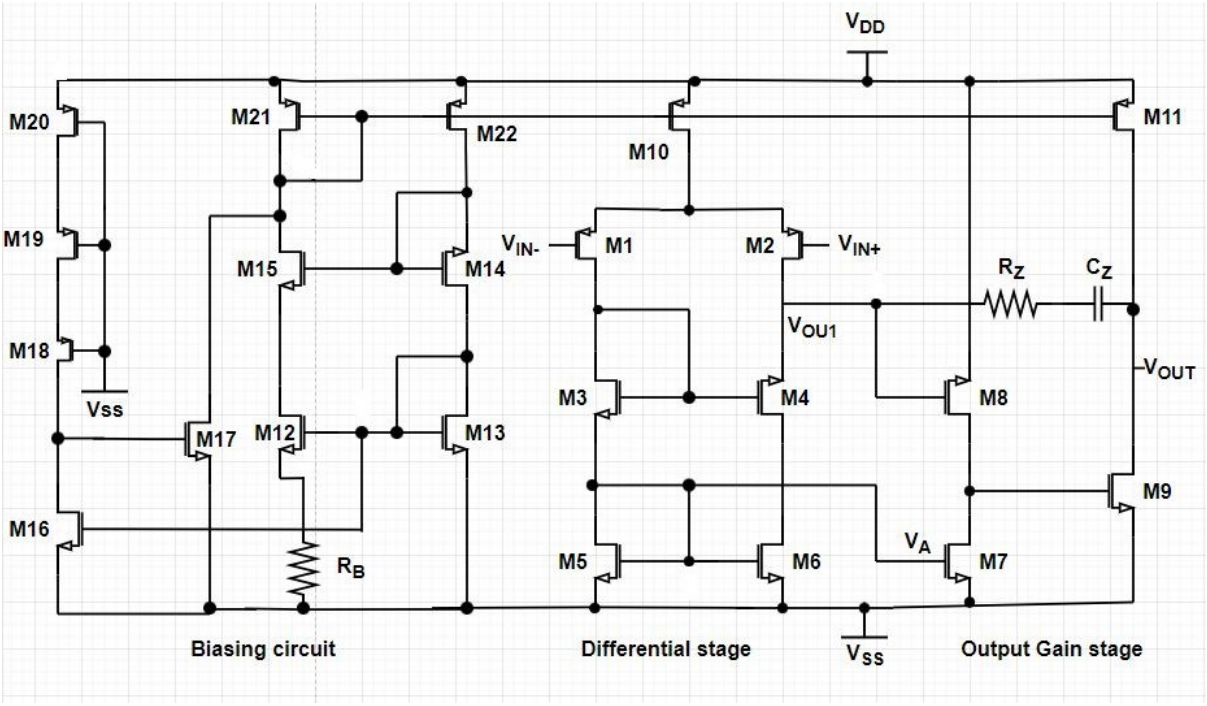



Figure 3. 2. Schematic representation of the OPAMP [17]

Table 3. 1. AC Parameters of transistors (a) M2, (b) M4, (c) M6, (d) M9 and (e) M11

| | |
|---|---|
| beta | 85.74u |
| cbtot | 62.11f |
| cdtot | 5.212f |
| cgd | 2.143f |
| cgs | 168.7f |
| cgtot | 182.1f |
| cstot | 204.3f |
| gam-eff | 468.1m |
| gds | 21.53n |
| gm | 11.56u |
| gmb | 3.443u |
| ibd | 1.888a |
| ibs | 1.884a |
| id | -1.125u |
| vbs | 233.5m |
| vds | -481.7m |
| vdsat | -165.2m |
| vgs | -666.5m |
| vod | -155.4m |
| vth | -511.1m |

(a)

| | |
|---|---|
| beta | 352.4u |
| cbtot | 43.96f |
| cdtot | 3.707f |
| cgd | 1.792f |
| cgs | 88.48f |
| cgtot | 108.9f |
| cstot | 115.3f |
| gam-eff | 490.6m |
| gds | 22.9n |
| gm | 18.93u |
| gmb | 4.495u |
| ibd | -27.13a |
| ibs | -2.215a |
| id | 1.125u |
| vbs | -479.8m |
| vds | 605m |
| vdsat | 104m |
| vgs | 604.9m |
| vod | 38.22m |
| vth | 566.6m |

(b)

| | |
|---|---|
| beta | 359.2u |
| cbtot | 54.11f |
| cdtot | 4.048f |
| cgd | 1.81f |
| cgs | 84.39f |
| cgtot | 109.9f |
| cstot | 118f |
| gam-eff | 496.2m |
| gds | 25.51n |
| gm | 18.82u |
| gmb | 5.461u |
| ibd | -2.226a |
| ibs | -969.7e-30 |
| id | 1.125u |
| vbs | 0 |
| vds | 479.8m |
| vdsat | 102.4m |
| vgs | 479.8m |
| vod | 37.13m |
| vth | 442.6m |

(c)

| | |
|---|---|
| beta | 713.5u |
| cbtot | 103.9f |
| cdtot | 6.795f |
| cgd | 3.49f |
| cgs | 165.9f |
| cgtot | 215.1f |
| cstot | 231.7f |
| gam-eff | 490.2m |
| gds | 41.91n |
| gm | 38.1u |
| gmb | 11.04u |
| ibd | -213.8p |
| ibs | -2.679e-27 |
| id | 2.29u |
| vbs | 0 |
| vds | 1.426 |
| vdsat | 102.8m |
| vgs | 480.1m |
| vod | 37.71m |
| vth | 442.4m |

(d)

| | |
|---|---|
| beta | 116.1u |
| cbtot | 100.1f |
| cdtot | 13.08f |
| cgd | 3.46f |
| cgs | 226.5f |
| cgtot | 245.3f |
| cstot | 284.4f |
| gam-eff | 475.1m |
| gds | 89.65n |
| gm | 19.38u |
| gmb | 6.357u |
| ibd | 21.32a |
| ibs | 461.7y |
| id | -2.291u |
| vbs | 0 |
| vds | -374.1m |
| vdsat | -195.6m |
| vgs | -641.1m |
| vod | -200.5m |
| vth | -440.6m |

(e)

### 3.2.1: Differential input stage

The PMOS transistors M1 and M2 form the differential input of the operational amplifier, which has the capability of suppressing common-mode interference signals and reducing the harmonic distortions that might be generated. The cascode structure formed by NMOS transistors M3 to M6 in the first stage helps in boosting the gain [17]. The differential input stage is a single-ended output stage providing a differential to single-ended conversion as shown in Figure 3.3.

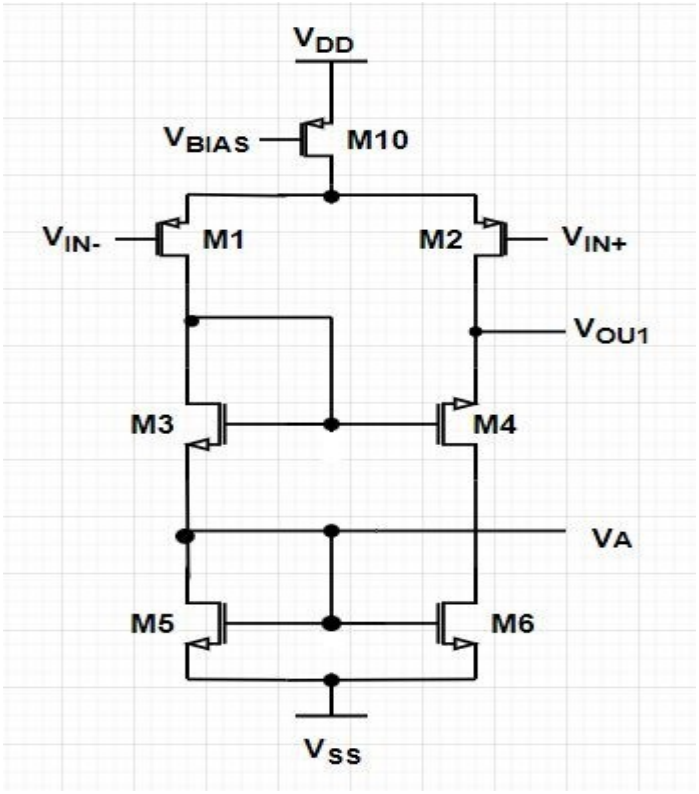



Figure 3. 3. Schematic representation of the differential input stage

Using nodal analysis at low frequency, the amount of gain $A_{V1}$ associated with differential input stage is given by

$$A_{V1} = \frac{V_{OU1}}{V_{IN}} = -gm_2 R_1 \tag{3.1a}$$

where

$$R_1 = r_{ds2} || r_{ds4} + \frac{1}{gm_6} = \frac{r_{ds4} \times r_{ds2}}{r_{ds4} + r_{ds2}} + \frac{1}{gm_6} \tag{3.1b}$$

$$V_{IN} = V_{IN+} - V_{IN-} \tag{3.1c}$$

From Table 3.1(a) and (b), we have

$$r_{ds2} = \frac{1}{g_{ds2}} = \frac{1}{21..54 \times 10^{-9}} = 46.425\text{M}\Omega$$

$$r_{ds4} = \frac{1}{g_{ds4}} = \frac{1}{22.9 \times 10^{-9}} = 43.687\text{M}\Omega$$

$$R_1 = \frac{r_{ds2} \times r_{ds4}}{r_{ds2} + r_{ds4}} + \frac{1}{gm_6} = 22.56\text{M}\Omega$$

Hence,

$$A_{V1} = 22.56 \times 10^6 \times 11.56 \times 10^{-6} = 260.79\,\text{V/V} \quad (3.2)$$

### 3.2.2: Output gain stage

The output gain stage is a common source amplifier, as shown in Figure 3.4, principally designed to further enhance the gain of the operational amplifier. Transistors M7 and M8 play a major role in the output stage by reducing the overdrive voltage at the output of M9. The transistors M10 and M11 in the differential and the output stage respectively form the current sink to produce proper bias [17]. The elements $R_Z$ and $C_z$ form the compensation circuit, which is responsible for the phase margin stability. The detailed design of the compensation circuit will be addressed in Section 3.2.4.

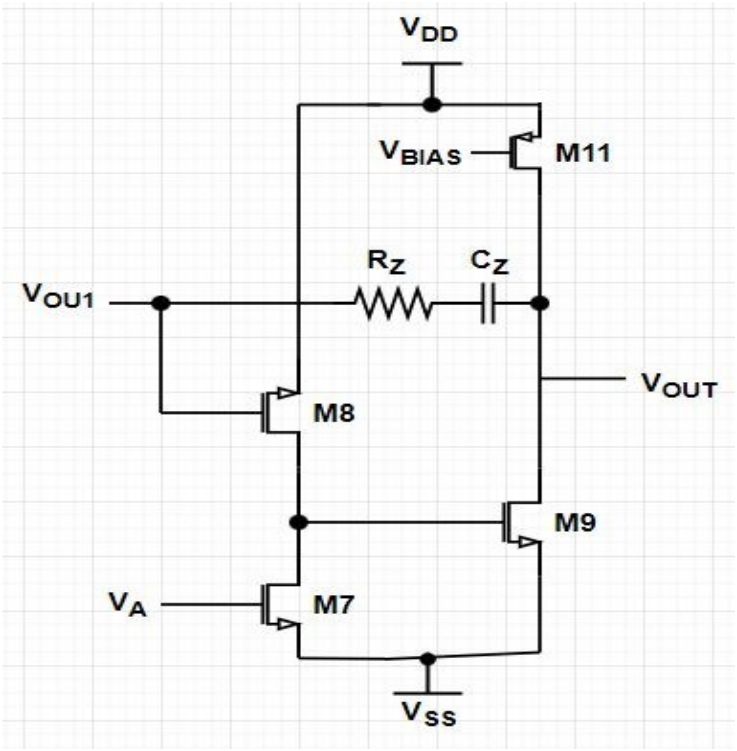



Figure 3. 4. Schematic representation of the output gain stage

The gain provided by the output gain stage at low frequency is given by

$$A_{V2} = \frac{V_{OUT}}{V_{OU1}} = +gm_9 R_2 \tag{3.3a}$$

where

$$R_2 = r_{ds11} || r_{ds9} = \frac{r_{ds9} \times r_{ds11}}{r_{ds9} + r_{ds11}} \tag{3.3b}$$

From Table 3.1(d) and (e), we also have

$$r_{ds9} = \frac{1}{g_{ds9}} = \frac{1}{41.91 \times 10^{-9}} = 23.86\text{M}\Omega$$

$$r_{ds11} = \frac{1}{g_{ds11}} = \frac{1}{89.65 \times 10^{-9}} = 11.15\text{M}\Omega$$

$$R_2 = \frac{r_{ds9} \times r_{ds11}}{r_{ds9} + r_{ds11}} = 7.59\text{M}\Omega$$

$$A_{v2} = 7.59 \times 10^6 \times 38.1 \times 10^{-6} = 289.18\,\text{V/V} \tag{3.4}$$

### 3.2.3: Overall gain of the OPAMP (at low frequencies)

The overall gain ($A_V$) of the operational amplifier shown in Fig.3.2 is given by

$$A_v = \frac{V_{OUT}}{V_{IN}}$$

$$A_v = \frac{V_{OU1}}{V_{IN}} \times \frac{V_{OUT}}{V_{OU1}} = A_{v1} \times A_{v2} \tag{3.5}$$

Using the values of $A_{v1}$ and $A_{v2}$ from (3.2) and (3.4) respectively, we have

$$A_{vdB} = 20\log(289.18 \times 260.79) = 97.58\text{dB}.$$

### 3.2.4: Design of the compensation circuit

Since the two-stage architecture has the disadvantage of having high impedances at the output of the differential stage ($V_{OU1}$) and the output gain stage ($V_{OUT}$), this will deteriorate the

phase margin of the OPAMP [19]. To rectify this situation, a compensation circuit is introduced with a series combination of $C_Z$ and $R_Z$, as shown in Figure 3.5. The detailed analysis is presented below.

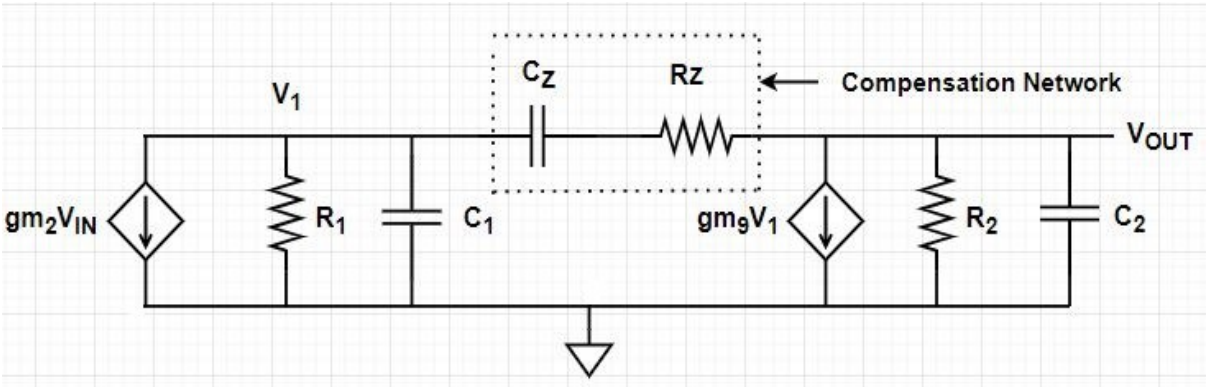



Figure 3. 5. A small signal model of the OPAMP for compensation analysis [19]

Consider the small signal model of the two stage OPAMP shown in Fig. 3.5, initially, we assume $R_Z = 0$ and perform nodal analysis concerning the input and output. The following transfer function is obtained [19], [20]:

$$\frac{V_{OUT}}{V_{IN}} = \frac{gm_2 gm_9 R_1 R_2 (1 - \frac{sc_Z}{gm_6})}{1 + sa + s^2 b} \tag{3.6}$$

where $R_1$ and $R_2$ have already been defined in (3.1b) and (3.3b), and

$$a = (c_2 + c_Z)R_2 + (c_1 + c_Z)R_1 + gm_9 R_1 R_2 c_Z \tag{3.7a}$$

$$b = R_1 R_2 \, (c_1 c_2 + c_1 c_Z + c_2 c_Z) \tag{3.7b}$$

$$c_1 = c_{db3} + c_{db5} + c_{gs6} \tag{3.7c}$$

$$c_2 = c_{db6} + c_{db1} \tag{3.7d}$$

In the above equations, $C_{db}$, $C_{gs}$, and $C_{gd}$ are the drain to bulk, gate to source, the gate to drain capacitances of the transistors (i.e., M2, M4 and M9) under consideration respectively. It is

possible to find approximate equations for the two poles based on the assumption that the poles are real and widely separated. This assumption allows us to express the denominator of (3.6) as [20]

$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) \tag{3.8}$$

The dominant pole, $\omega_{p1}$ is given by

$$\omega_{p1} = \frac{1}{gm_9 R_1 R_2 C_Z} \tag{3.9a}$$

whereas the non-dominant pole, $\omega_{p2}$, is given by

$$\omega_{p2} = \frac{gm_9}{c_1 + c_2} \tag{3.9b}$$

A resistor ($R_Z$) is connected in series to the Miller capacitor ($C_Z$) to move the right half-plane zero into the left half-plane to cancel the non-dominant pole, $\omega_{p2}$.

The zero is now determined by the relationship,

$$\omega_z = \frac{-1}{c_Z(\frac{1}{gm_9} - R_Z)} \tag{3.10}$$

Therefore, we can choose (3.10) to eliminate the right half-plane zero altogether.

$$R_Z \geq \frac{1}{gm_9} \tag{3.11}$$

$$c_Z = \left(2c_{gd2} + c_{db2}\right) + \left(2c_{gd4} + c_{db4}\right) + 2c_{gs9} \tag{3.12}$$

From Table 3.1 (a), (b) and (d) we have,

$c_Z = (2 \times 2.143 \times 10^{-15} + 5.21 \times 10^{-15}) + (2 \times 1.792 \times 10^{-15} + 3.70 \times 10^{-15}) + 2 \times 165.5 \times 10^{-15} = 374.65\text{fF}$.

From (3.11), we have

$$R_Z \geq \frac{1}{30.13 \times 10^{-6}} \geq 33.20K\Omega$$

The concept of designing and implementing compensation circuits (lead compensation) in a two-stage operational amplifier for phase margin stability has been adopted from [19], [20].

### 3.2.5: Biasing and start up circuit

Bias circuits are principal components of analog circuits for producing voltage or current references. The bias and start up circuit shown in Figure 3.6 is composed of transistors M12 to M22 and $R_B$, while the start-up circuit consists of transistors from M16 to M20. The transistors M21 and M22 form the current mirror to ensure that their DC drain currents are forced to be equal. The cascode structure of the bias circuit reduces the channel length modulation effect and ensures that the bias current is accurately equal on both sides (i.e., $I_{B1}$ and $I_{B2}$ as shown in Fig.3.6) [17].

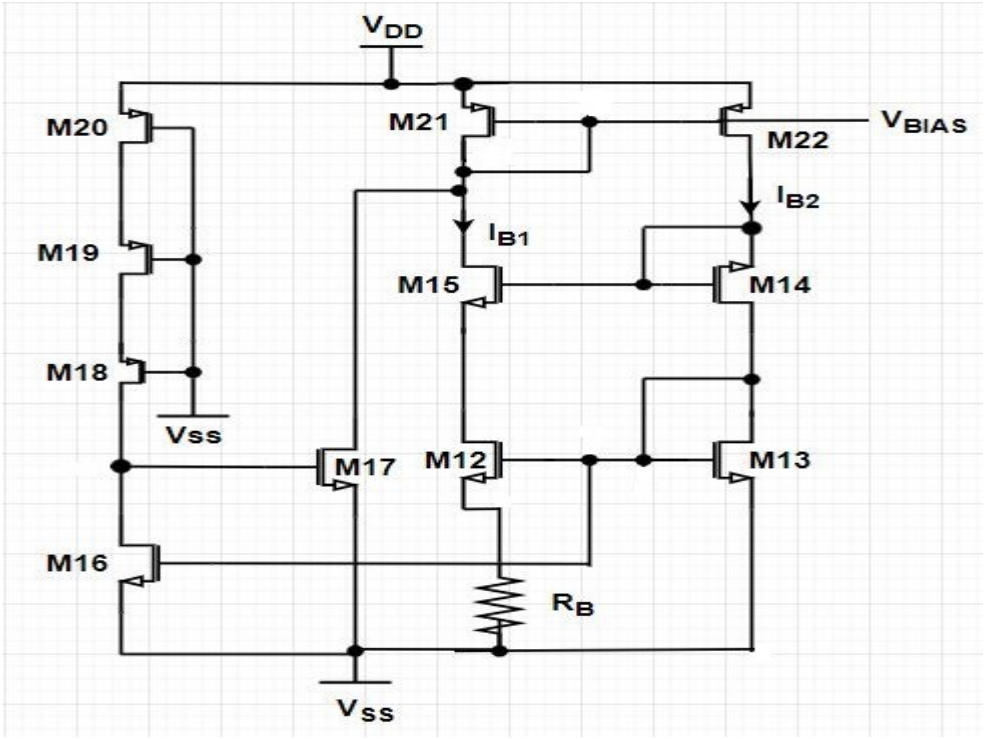



Figure 3. 6. Biasing circuit [17]

A start up circuit is required to bring up the bias current from zero current to its normal operating point. The start-up circuit is no longer used once the bias circuit is operating properly [18]. The aspect ratio of the transistors M18 to M20 is chosen carefully to provide very high channel resistance. Similarly, the aspect ratios of M16 and M17 are also chosen properly to provide very low resistance to the channels. Hence, there will be zero current in the start-up circuit when the bias circuit is functioning properly. The concept of getting very high and low channel resistances using MOS is addressed Section 3.3. To get appropriate bias voltage ($V_{BIAS} = 258.9mV$), the aspect ratio of the transistors and $R_B$ (1K) of the bias circuit is properly chosen to set the current $I_B = 1.17\mu A$.

### 3.3: Realization of Passive Resistors from MOS Transistors

Passive resistors occupy a very large area in integrated circuit (IC) design. Thus, passive resistors are not preferable in IC, since they cause compatibility problem in modern integrated circuit design.

However, the passive resistors $R_z$ and $R_B$ present in the compensation and the bias circuit are replaced by MOS transistors by choosing suitable aspect ratios $\left(W/L\right)$ of the transistors. MOS transistors have four regions of operation, which include cut-off, subthreshold, linear, and saturation region.

The MOS transistors used to replace $R_z$ and $R_B$ were set to operate under linear region by applying a reasonable bias voltage to its gate terminal. Further details in this respect are provided below.

The classical model equation for n-channel transistor operating in the triode region is given by

$$I_{DS} = \mu_n C_{OX} W/L \left(V_{ov} - 1/2\, V_{DS}\right)V_{DS} \quad V_{DS} < V_{GS} - V_{TH} \tag{3.13}$$

where $\mu_n$ is the carriers' mobility through the transistor channel, W is the width of the transistor, L is the length of the channel, $V_{DS}$ is the drain to source voltage, $V_{GS}$ is the gate to source voltage of the transistor, and $V_{TH}$ is the threshold voltage of the transistor.

Considering that a small $V_{DS}$ is used, then we can model the channel resistance $(r_{ds})$ of the transistor by

$$r_{ds} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \tag{3.14}$$

Hence, in the linear region we can define the effective channel resistance $(r_{ds})$ between the drain and the source of an n-channel transistor as

$$r_{ds} = \frac{L}{\mu_n C_{OX} W(V_{GS} - V_{TH})} \tag{3.15}$$

It can be noticed from (3.15) that, $r_{ds}$ is mainly dependent on the aspect ratio of the transistor, if a fixed $V_{GS}$ is applied. Thus, the resistance of any transistor increases when the aspect ratio decreases and vice versa. $\mu_n C_{OX}$ is the process transconductance parameter value of the transistor and $V_{TH}$ is always a constant value mainly depending on the CMOS technology being used.

### 3.4: Transistors Size Data and the Performance Parameters of the OPAMP

In this section, we present the various design parameters such as the aspect ratio of the transistors, power supply, etc., and the simulated results including the voltage gain, CMMR, phase margin, etc. of the operational amplifier used. The performance parameters and results are presented in Tables 3.2 and 3.3, respectively. The overall configuration of the OPAMP has been shown in Fig.3.2.

Table 3. 2. Design parameters for the OPAMP shown in Figure 3.2

| Transistors | W(microns) | L(microns) | $^{W}/_{L}$ |
|---|---|---|---|
| M1, M2 | 6.1 | 5 | $^{6.1}/_{5}$ |
| M3−M6 | 4.9 | 5 | $^{4.9}/_{5}$ |
| M7, M8 | 1 | 5 | $^{1}/_{5}$ |
| M9 | 9.6 | 5 | $^{9.6}/_{5}$ |
| M10, M11 | 8 | 5 | $^{8}/_{5}$ |
| M12, M13 | 4.9 | 5 | $^{4.9}/_{5}$ |
| M14−M17 | 4.5 | 0.5 | $^{4.5}/_{0.5}$ |
| M18−M20 | 0.5 | 17 | $^{0.5}/_{17}$ |
| M21, M22 | 2 | 5 | $^{2}/_{5}$ |
| $V_{DD} = 900\text{mV}, V_{SS} = -900\text{mV}$<br>$C_Z = 0.376\text{pF}, R_Z = 32.2\text{K}\Omega, R_B = 1\text{K}\Omega$ | | | |

Table 3. 3. Simulated results of the OPAMP

| Parameters | Values |
|---|---|
| Voltage Gain | 97.7 dB |
| Unity Gain Bandwidth | 30.2 MHz |
| Phase Margin | 53.5 deg |
| CMRR | 95.26 dB |
| Output Offset Voltage | 241.1 mV |
| Power Dissipation | 13.61 μW |

### 3.5: Summing Amplifier

In order to demonstrate the effectiveness of our proposed system to eliminate the artifacts, we use a summing amplifier to add artifact signals to the intended EEG signals to simulate a natural mixture of physiological signals. The summing amplifier emulates the sensor node that receives the intended EEG signal and the artifact signals as a natural mixture. In our case, a non-inverting summing amplifier is preferable to ensure that the combined output signal (contaminated EEG signal) is in phase with the input signals (artifact and intended signals).

In the case of a non-inverting summing amplifier, the inputs are applied to the non-inverting terminal (+) while the required negative feedback and gain $(A_V)$ is achieved by feeding back some portion of the output signal to the inverting terminal (-) of the OPAMP as shown in Fig 3.7 [21].

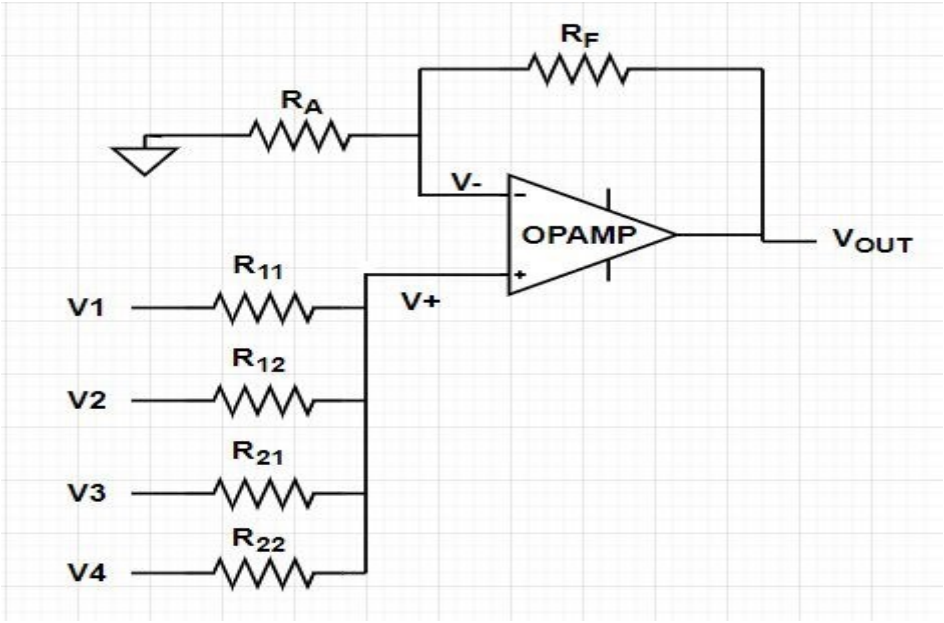



Figure 3. 7. Summing amplifier

If we consider four inputs to the non-inverting summing amplifier as shown in Figure 3.7, the current passing into the input terminal can be written as

$$I_{R11} + I_{R12} + I_{R21} + I_{R22} = 0 \tag{3.16}$$

$$\frac{V_1 - V_+}{R_{11}} + \frac{V_2 - V_+}{R_{12}} + \frac{V_3 - V_+}{R_{21}} + \frac{V_4 - V_+}{R_{22}} = 0 \tag{3.17}$$

If we set all input resistances to be equal i.e., $R_{11} = R_{12} = R_{21} = R_{22} = R$, then (3.17) can be simplified as

$$V_+ = \frac{V_1 + V_2 + V_4 + V_4}{4} \tag{3.18}$$

The standard equation for voltage gain of a non-inverting summing amplifier is given as

$$A_v = \frac{V_{OUT}}{V_{IN}} = \frac{V_{OUT}}{V_+} = 1 + \frac{R_F}{R_A} \tag{3.19}$$

$$V_{OUT} = \left(1 + \frac{R_F}{R_A}\right)\left(\frac{V_1 + V_2 + V_3 + V_4}{4}\right) \tag{3.20}$$

For the four inputs non-inverting summing amplifier configurations shown in Figure 3.7, setting the closed-loop voltage gain ($A_V$) to $4\,V/V$ such that $R_F = 3R_A$ will make $V_{OUT}$ equal to the sum of four inputs voltages $V_1,\ V_2, V_3,$ and $V_4$.

In our case, we set $R_{11} = R_{12} = R_{21} = R_{22} = R = 1K\Omega$. In (3.20), $R_A$ and $R_F$ are also set to $1K\Omega$ and $3K\Omega$, respectively, to ensure that the input signals combine appropriately at the output of the summer amplifier. In CMOS implementation of the summing amplifier, the passive resistances shown in Figure 3.7 are replaced by NMOS transistors operating under the triode region as discussed under Section 3.3. The exact channel resistances are obtained by varying the aspect ratio and applying a reasonable voltage supply to the various gate terminals of the MOS transistors. Figure 3.8 shows a schematic representation of the CMOS summing amplifier.

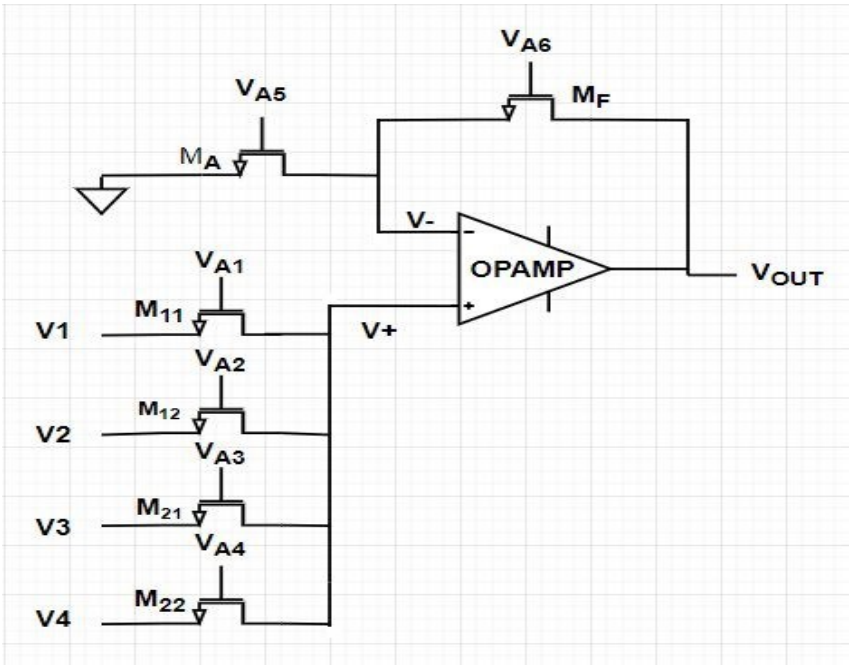



Figure 3. 8. CMOS Summing amplifier

In the above CMOS summing amplifier design, equal voltage supply ($V_A$) is applied to various gate terminals of the NMOS transistors such that $V_{A1} = V_{A2} = V_{A3} = V_{A4} = V_{A5} =$

$V_{A6} = V_A$ as shown in Figure 3.8. The design parameters of the CMOS summing amplifier are listed in Table 3.4.

Table 3. 4. Design parameters of the CMOS summing amplifier shown in Figure 3.8

| Transistors | W(microns) | L(microns) | $W/L$ |
|---|---|---|---|
| $M_{11}, M_{12}, M_{21}, M_{22}$ | 73.5 | 1.5 | $73.5/1.5$ |
| $M_A$ | 73.5 | 1.5 | $73.5/1.5$ |
| $M_F$ | 24.5 | 1.5 | $24.5/1.5$ |
| $V_{A1} = V_{A2} = V_{A3} = V_{A4} = V_{A5} = V_A = 500mV$ | | | |

**3.6: Difference Amplifier**

The difference amplifier is one of the major subsystems in both the ARTI block and the overall design to retrieve the artifact band signals. The difference amplifier was adopted from the instrumentational amplifier used in the amplification of biomedical signals as elaborated in [17]. This is shown in Figure 3.9. An instrumentation amplifier allows the amplification of the difference between the signals applied to its two input terminals ($V_{IN-}$, $V_{IN+}$) whiles not amplifying any signal common to both inputs.

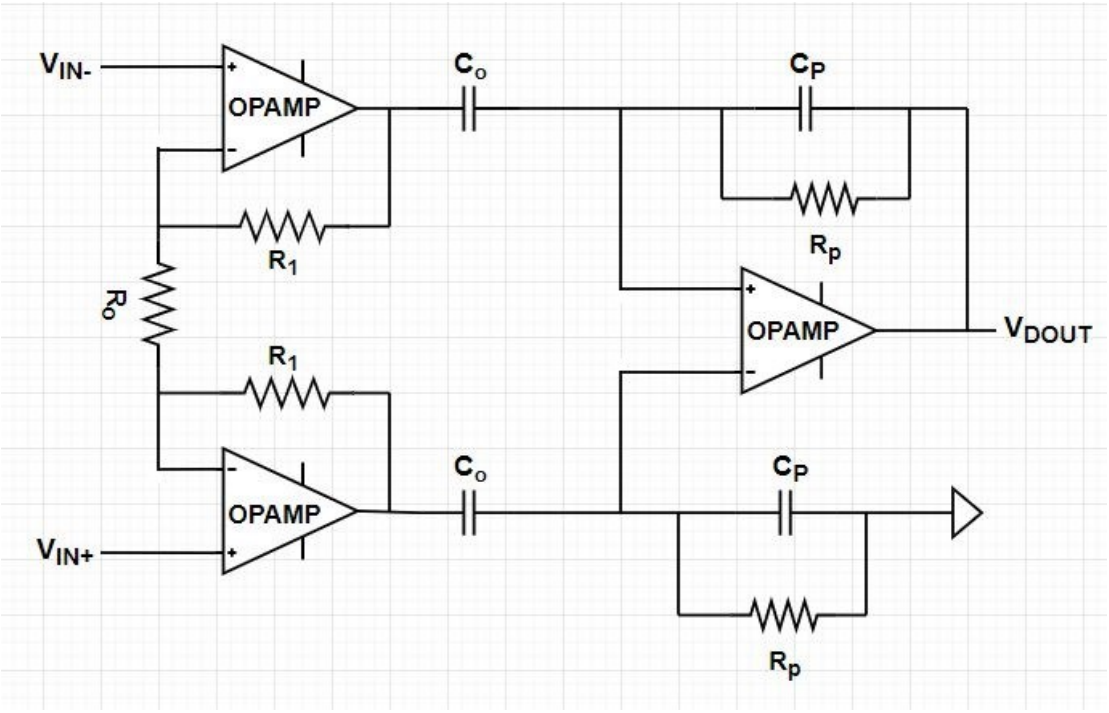



Figure 3. 9. Instrumentation amplifier [17]

The mid-band gain of the whole instrumentational amplifier is given by

$$G = \left(1 + \frac{2R_1}{R_O}\right)\left(\frac{C_0}{C_P}\right) \tag{3.21}$$

The lower 3dB cut off frequency is given by

$$F_L = \frac{1}{2\pi C_P R_P} \tag{3.22}$$

The mid-band gain of the instrumentational amplifier (IA) can be controlled by changing the values of the resistors as shown by (3.21).

For effective subtraction of the artifact signals from the natural mixture of the intended and artifact signals at the input of the adaptive system, the instrumentation amplifier is required to have unity mid-band gain. This will give a difference amplifier with unity gain. However, to get a unity gain from (3.21), the resistance $R_1$ is short-circuited (that's $R_1 = 0$ ) and capacitances $C_O$ and $C_p$ are set to have equal values ($C_O = C_p$) as illustrated in Figure 3.10.

The mid-band gain of the difference amplifier is independent of $R_P$. $R_P$ is set to have a high resistance value of the order of 10GΩ, to allow the passage of low frequencies such as the delta band of EEG and higher frequency signals through the proposed system.

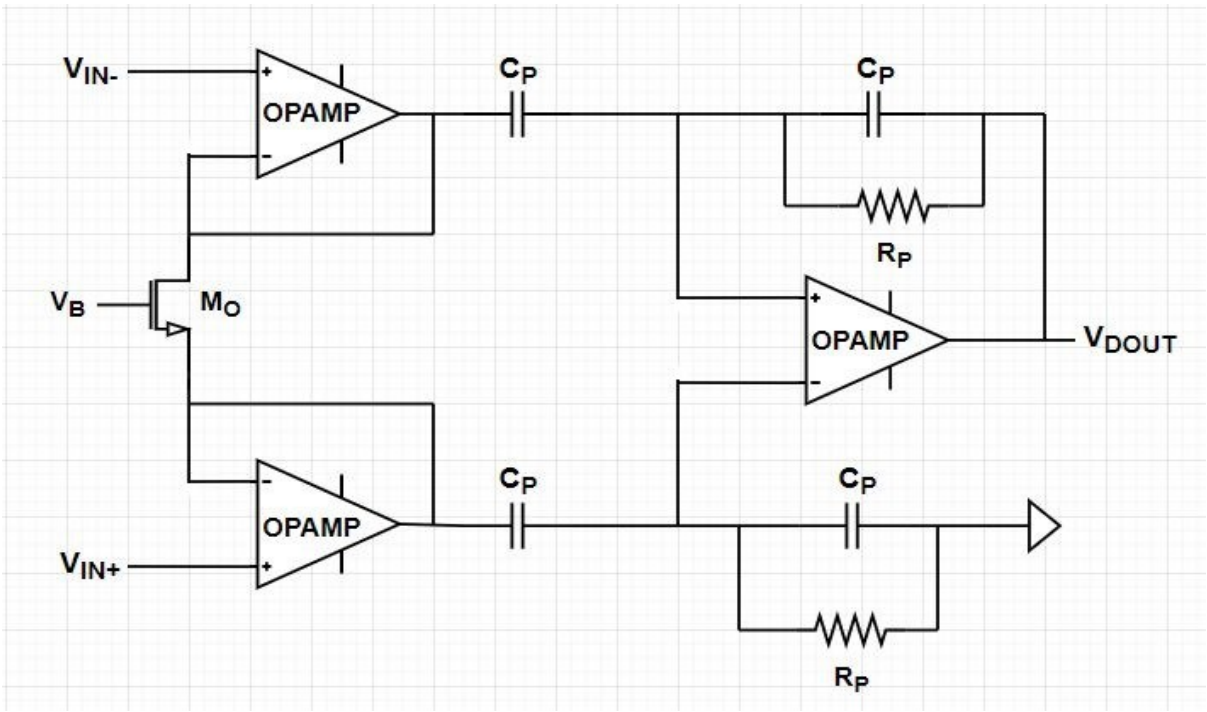



Figure 3. 10. Unity gain difference amplifier (D_AMP)

Referring to Table 2.4 of Chapter 2, it is noticed that the delta band with a frequency range of $0.5 - 4$ Hz has the lowest frequency band in the EEG signal. According to (3.22), the lower band (0.5Hz) of the delta band is used to compute the value of $R_P$. So, for a frequency of 0.5Hz, the time constant $R_P C_P$ would be very high. The capacitor $C_P$ is chosen with a value of 5pF, thereby resulting in a resistor of 63.7GΩ as shown by the following equation.

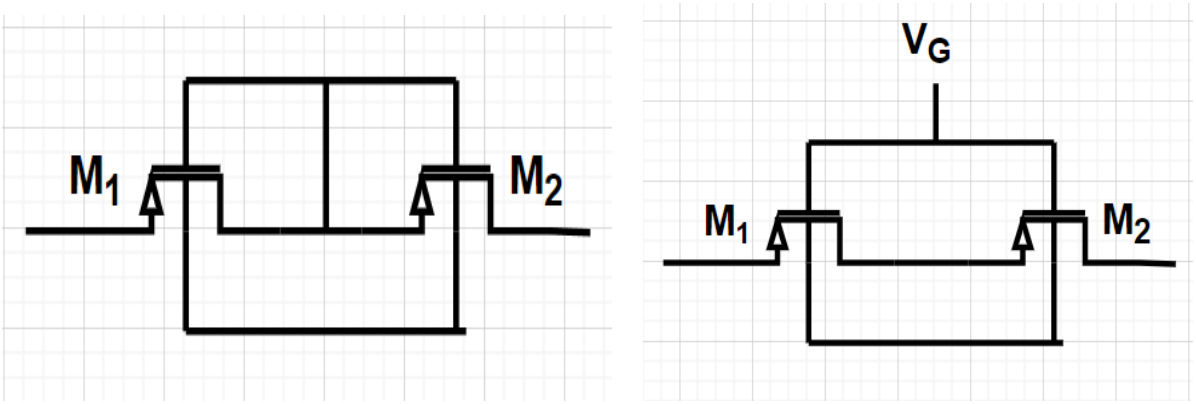
$$R_P > \frac{1}{2\pi \times F_L \times C_P} \tag{3.23}$$

To ensure the passage of all the EEG band signals including the delta band, then $R_P$ is taken to be $R_P > 63.7\text{G}\Omega$. Such a high resistance of $R_P$ cannot be realized in integrated circuit design. Another way of designing a high resistor value is the use of MOS pseudo resistor [22]- [24].

### 3.6.1: Implementation of MOS pseudo resistor

A resistor of hundreds of megaohms can be achieved when MOSFET is biased in the subthreshold region ($V_{GS} < V_{TH}$) and this kind of MOS resistor is commonly used together with a capacitor in recording of neural signals [22]. For $V_{GS} < V_{TH}$ , a very small amount of drain current flows through MOSFET. This current is called subthreshold current and corresponding region of operation is known as weak inversion or subthreshold region [23]. These large resistors are implemented using MOS pseudo resistor configuration purposely to reduce the design area and the power consumption of the system.

Figures 3.11(a) and 3.11(b) show the different configurations of the pseudo resistor circuits. The gate voltages of the Figure 3.11(a) are obtained by the virtue of the gates connected to the source and drain node of the respective transistors.




(a). Self-biased pseudo resistor (b). Pseudo resistor with an external bias ($V_G$)

Figure 3.11. Pseudo resistor configurations

These pseudo resistor configurations were carried out in CMOS18 technology using standard AC measurement configurations to know the range of resistance values that can be offered by these pseudo resistors circuit at different aspect ratios ($^{W}/_{L}$) of the MOS transistors. Figure

3.12 and Figure 3.13 shows the AC resistances characterisation of the respective pseudo resistor circuits. In the experiment, the bias voltage ($V_G$) of Figure 3.11(b) is set to 15mV.

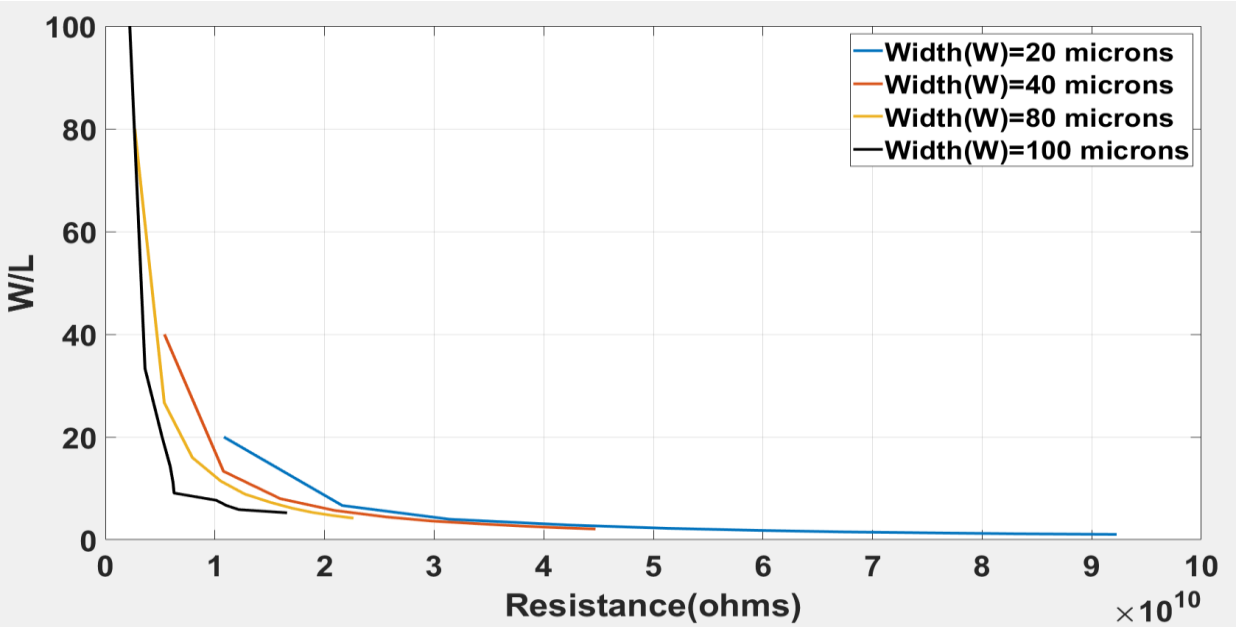



Figure 3.12. AC resistance characterisation of self-biased pseudo resistor

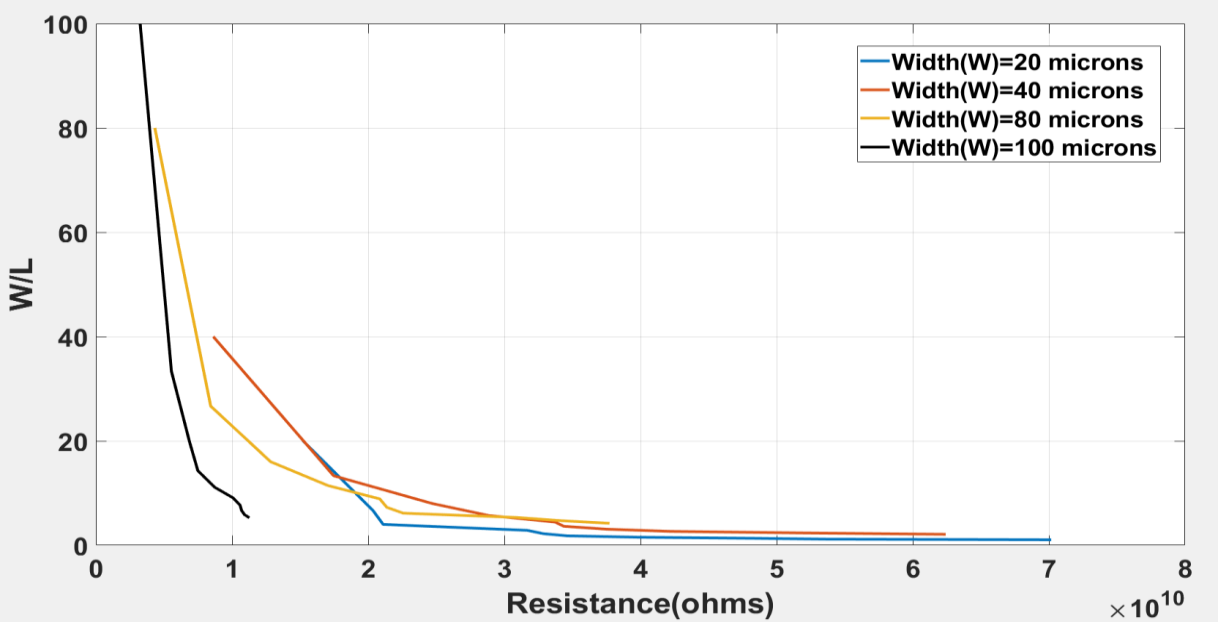



Figure 3.13. AC resistance characterisation of pseudo resistor with external biased voltage

From Figure 3.12 it may be noticed that resistance in order of 92.3 Giga-ohms can be obtained with W = 20 micron and $^{W}/_{L} = 1.05$. Similarly, from the Figure 3.13 we find that

a resistance of the order of 70.2 Giga-ohms can be obtained with $W = 20$ microns and $^{W}/_{L} = 1.05$. Hence, self-biased pseudo resistor configuration provides more resistance values compared to the pseudo resistor configuration with an external biased voltage with the transistors having the same aspect ratios. Since $R_P$ should be greater than 64.67 Giga-ohms, hence, $R_P$ calculated in (3.23) has been replaced by the configuration shown in Figure 3.11(b). $R_o$ in Fig. 3.9 is replaced by NMOS transistor $M_O$ (in Fig.3.10) operating under a linear region with an appropriate supply $(\text{i.e.}, V_B = 420\text{mV})$ . The design parameters of the unity gain difference amplifier are shown in Table 3.5. Figure 3.14 shows the frequency response of the unity gain difference amplifier.

Table 3. 5. Design parameters of the unity-gain difference amplifier

(refer to Figures 3.10 and 3.11(b))

| Transistors | W(micron) | L(micron) | $^{W}/_{L}$ |
|---|---|---|---|
| $M_0$ | 50 | 0.4 | $^{50}/_{0.4}$ |
| $M_1, M_2$ | 20 | 19 | $^{20}/_{19}$ |
| $C_O = C_P = 5\text{pF}, R_P = 70.2\text{G}\Omega, V_B = 420\text{mV}, V_G = 15\text{mV}$ | | | |

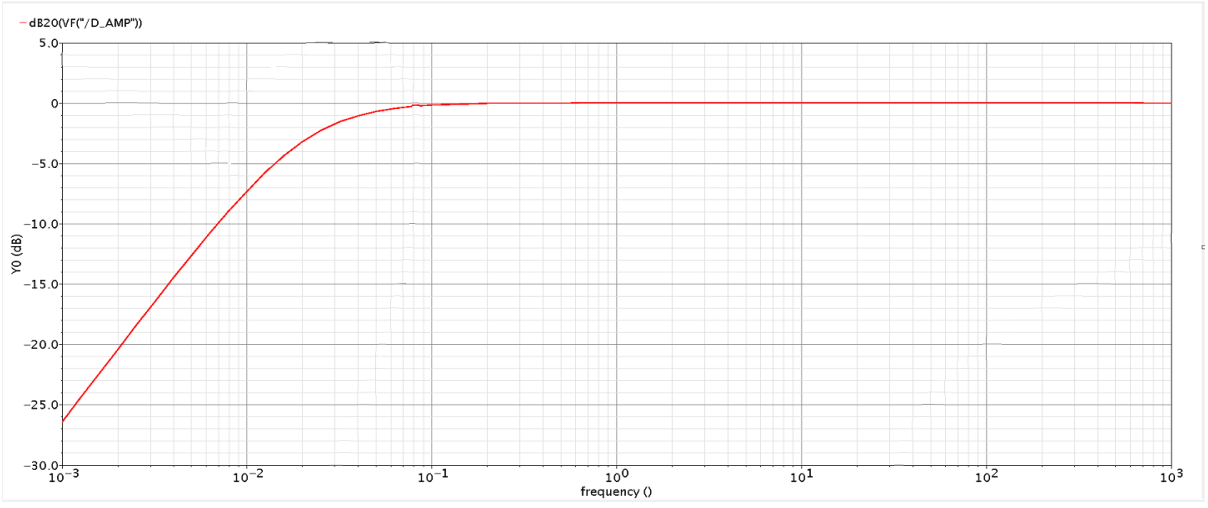



Figure 3.14. Frequency response of the unity gain difference amplifier (D_AMP)

### 3.7: Conclusion

In this chapter, we introduced the design of the operational amplifier used in our work. Detailed analysis of the various stages of the operational amplifier were addressed. Finally, the overall performance and simulation results of the operational amplifier have been included in this chapter. Implementation of high valued resistor using pseudo resistor configuration with MOS transistors has been exploited. In the following chapter the building blocks introduced in this chapter will be used to develop various sub systems proposed in Chapter 1 of the thesis. In Chapter 4, analysis and design considerations of the other subsystems depicted in Chapter 1 of the thesis will be addressed.

# Chapter 4

# Subsystems of the Proposed Analog System

In this chapter the design and implementation of several subsystems of the analog system proposed in Chapter 1 of the thesis will be elaborated upon. First, we will consider the implementation of the compressor and expander (i.e., compander) subsystem. The companding operation maintains the levels of the signals within the range of linear magnification by compressing high level signals at the input to the amplifier systems while expanding low level signals at the output of the amplifier system. We will also focus on the implementation of the artifact recovery system which is the ARTI subsystem shown in Fig.1.7, Chapter 1 of the thesis. The ARTI subsystem eliminates the band of intended signals by means of several band stop filters, thereby isolating the artifact signals from the intended signals. The band stop filters could be realised as second order notch filters. For the notch filters, active twin-T configuration has been adopted. All these subcircuits are implemented using CMOS18 (180 nano meter) technology available in the VLSI research laboratory of Concordia University.

### 4.1: The Compander

The word compander combines compressor and expander. The functional flow is shown in Figure 4.1 [25], where F stands for the expanding function that usually follows an exponential law [22]. The process chain usually includes $y \rightarrow x$ compression and $x \rightarrow y$ expansion.

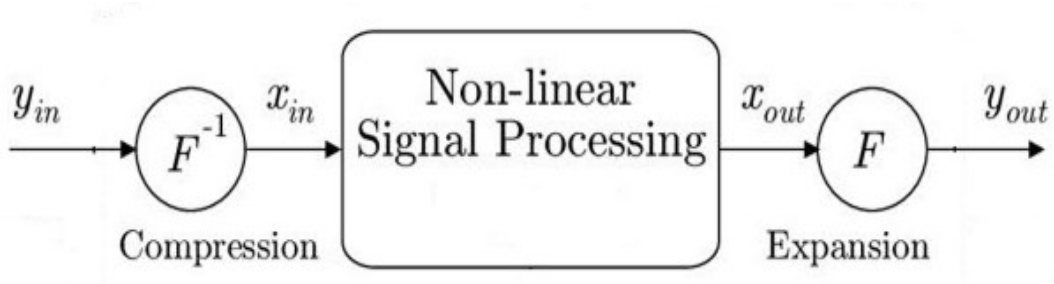



Figure 4. 1. Generalized companding principles [25]

### 4.1.1: Compressor and expander circuit

The desired signal (i.e., EEG signals) values are considerably of smaller magnitude compared to that of the artifact signals. In some cases, the levels of the artifact signals could become comparatively high, which would introduce non-linearity in the adaptive filtering system. In such case, a compander (i.e., compressor and expander) can be introduced to combat the nonlinearity.

A compressor reduces the amplitude levels of all the input signals (i.e., both the intended and artifact signals), but the reduction of higher levels (i.e., artifact signals) is more desirable in order to combat the potential non-linearity introduced by the high-level artifact signals. The intended signals will be compressed as well. However, the intended signals will be removed by the notch filters in the ARTI subsystem irrespective of how the compressor will act on the intended signals.

The compression can be achieved by utilising the nonlinear I-V characteristic of semiconductor diodes. With the diodes configured properly in a compressor circuit, the system will offer small attenuation to low amplitude signals (i.e., mostly the intended signals), while high attenuation to higher level (i.e., the artifact) signals. The expander is designed to nullify the effect of the compressor circuit. The expander circuit is principally designed to reinstate

the original levels of the artifact signals as it was at the output of the S_ARRAY amplifier system. The artifact signals appear at the output of the ARTI block (Fig.1.7 in Chapter 1).

Figure 4.2(a) depicts the operation of a typical compressor circuit. Consider that the input ($v_I$) to the compressor consists of several intended signals $S_{int}$ plus a host of artifact signal $S_{art}$ voltages. This can be represented by

$$v_I = \sum_1^m S_{int} + \sum_1^n S_{art} \qquad (4.1)$$

where the summations extend over m intended signals, and n artifact signals. One must remember that $v_I$ contains a mixture of signals arriving from the output of the S_ARRAY block (see Fig. 1.7).

For a positive valued signal, the diode D1 will conduct with an incremental resistance which is inversely proportional to the signal voltage $v_I$. For negative going signals, the diode D2 will act similarly. The incremental resistance of the diode remains high for low level signals and conversely, the incremental resistance remains low for high level signals. Thus, the voltage gain (i.e., ratio of diode incremental resistance to the input resistance $R_o$) of the system will be low for high level input, and the voltage gain will be high for low level input. This is a compression effect. The resistance $R_o$ across the OPAMP helps prevent crossover distortion when neither of the diodes is conducting fully.

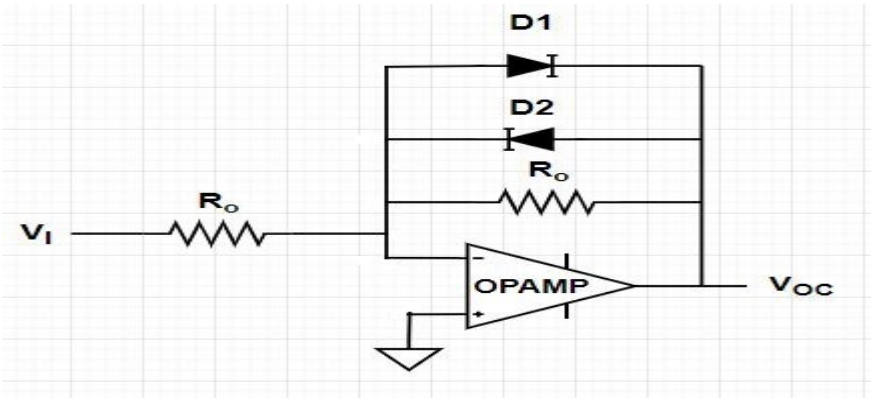



Figure 4. 2 (a). Compressor circuit (COMPR)

Figure 4.2(b) depicts a typical expander circuit with diodes. In this case the input $s_o$ will correspond to the compressed form of the second term ($\sum_1^n S_{art}$) in (4.1) after its passage through the ARTI subsystem, the compressed intended signals having been attenuated by the notch filters (NF) in the ARTI subsystem. The operation of the expander can be understood following a reasoning similar to that for the compressor.

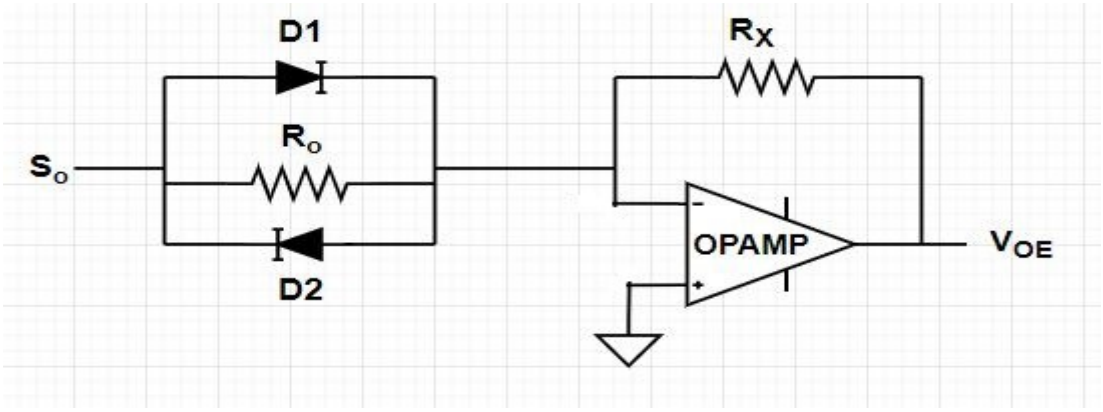
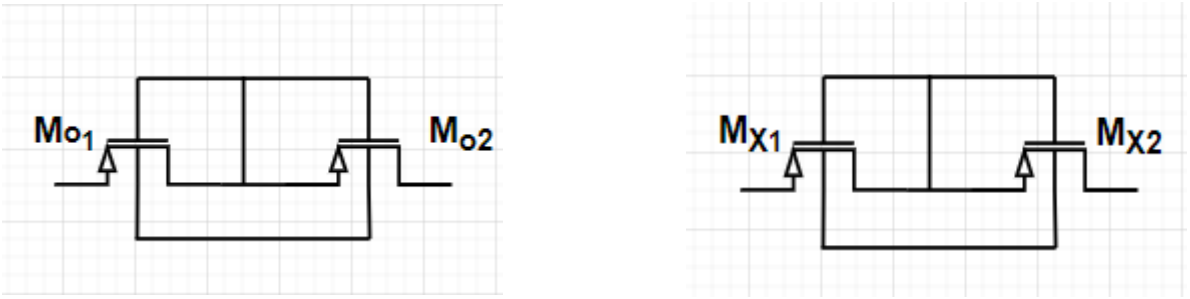



Figure 4. 2(b). Expander circuit (EXPDR)

The passive $R_O$ ($R_O = 180M\Omega$) in the compressor as well as the expander circuit is replaced by pseudo resistor configuration as shown in Fig. 4.3(a). Similarly, $R_X$ ($R_X$=380MΩ) in the expander circuit is replaced by another pseudo resistor configuration as shown in Fig. 4.3(b). $R_X$ is required to be different from $R_O$ to compensate for a lack of strict matching between the compression and expansion factors.




(a). Pseudo resistor ($R_O$)

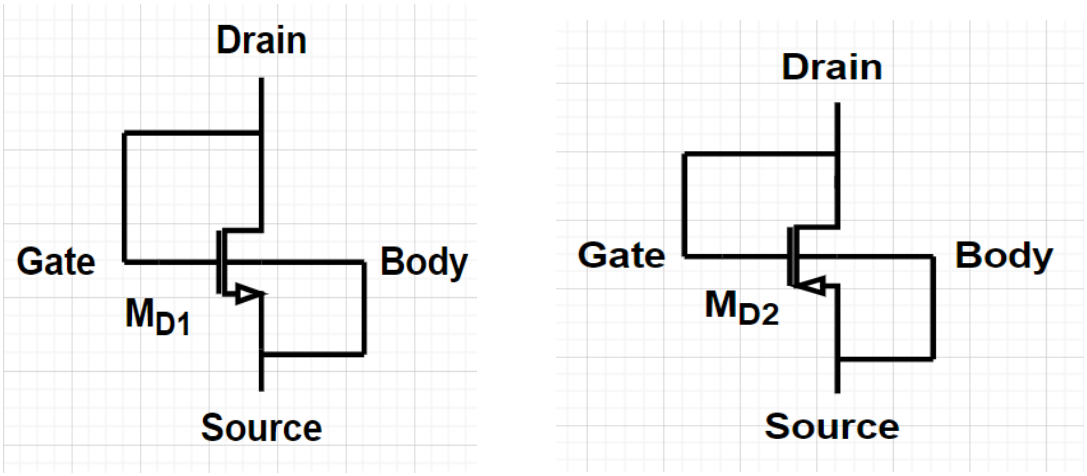
(b). Pseudo resistor ($R_X$)

Figure 4. 3. Pseudo resistor

The separated values are obtained by adjusting the $^{W}/_{L}$ ratios in the pseudo resistor configurations. The pertinent issues have been covered in section 3.6.1 of the previous chapter.

#### 4.1.1.1: Implementation of diode (D1 and D2) with MOS

In our case, gate-to-drain connected MOS transistors are used to implement the CMOS diodes. Thus, D1 is replaced by the gate to drain connected NMOS transistor as shown in Fig. 4.4(a). Similarly, diode D2 is replaced by the gate to drain connected PMOS transistor as illustrated in Fig. 4.4(b). We choose $W_p = 3W_n$ to ensure uniform mobility between the diodes made from the PMOS and NMOS transistors, where $W_p$ and $W_n$ are the widths of the PMOS and NMOS transistors, respectively. By virtue of the gate-drain connections the transistors operate in saturation regions.




(a). MOS diode (D1) (b). MOS diode (D2)

Figure 4. 4. MOS diode

#### 4.1.2: Results and performance parameters of the compander

This subsection focuses on the results and the design parameters of the compressor as well as the expander used in the proposed system. Figure 4.5 (a) and Figure 4.5 (b) present the input-output voltage characteristics of the compressor and the expander, respectively. The

range for the input voltage of the compressor is approximately $-0.5\text{V}$ to $+0.5\text{V}$ while that for the expander is approximately $-0.1\text{V}$ to $+0.1\text{V}$. The design parameters of the transistors in the expander and compressor circuits are listed in Table 4.1. The reversed orientation of each graph is due to the fact that the amplifiers in Figures 4.2(a) and 4.2(b) are inverting amplifiers.

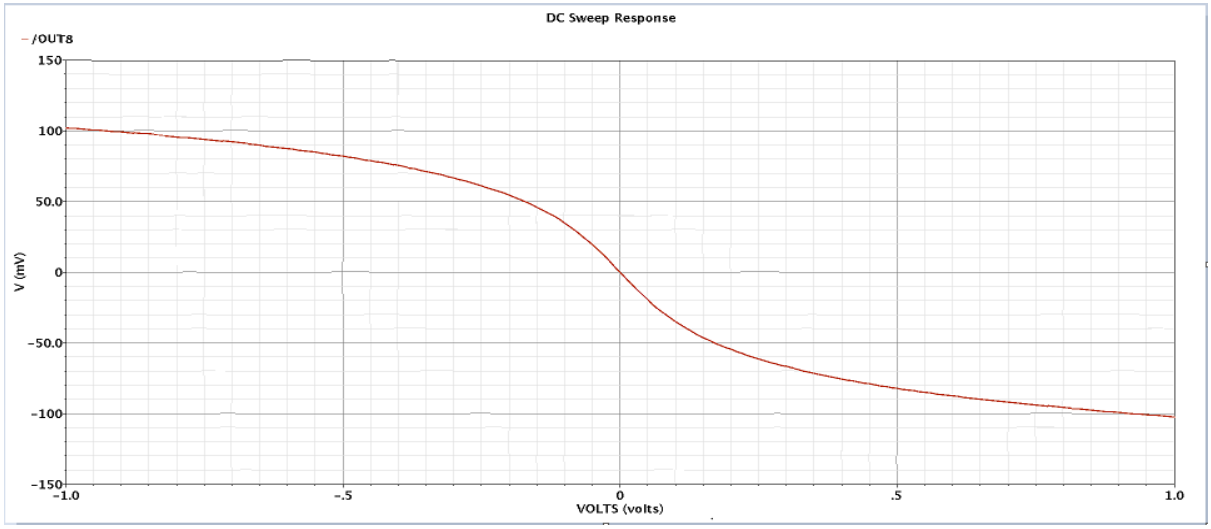



Figure 4. 5(a). Output-input voltage characteristics of the compressor

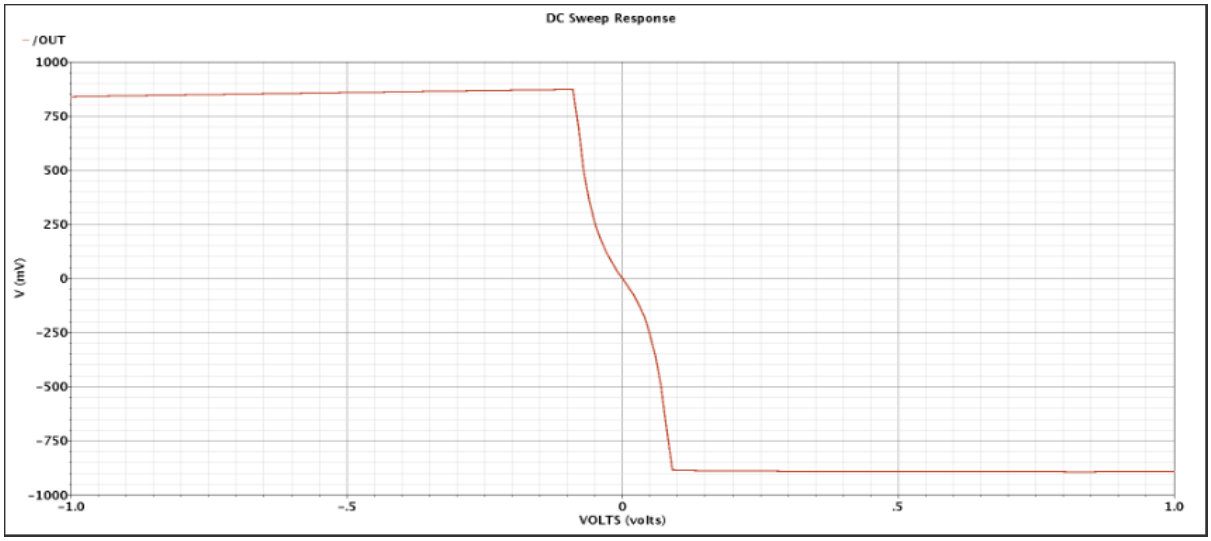



Figure 4. 5(b). Output-input voltage characteristics of the expander

Table 4. 1. Design parameters of the compander (refer to Figures 4.2, 4.3 and 4.4)

| Transistors | W(microns) | L(microns) | $^{W}/_{L}$ |
|---|---|---|---|
| $M_{O1}, M_{O2}$ | 100 | 0.18 | $^{100}/_{0.18}$ |
| $M_{X1}, M_{X2}$ | 50 | 0.18 | $^{50}/_{0.18}$ |
| $M_{D1}$ | 0.5 | 0.18 | $^{0.5}/_{0.18}$ |
| $M_{D2}$ | 1.5 | 0.18 | $^{1.5}/_{0.18}$ |

**4.2: ARTI System**

Consider that the input ($S_{ic}$) to the ARTI block consists of several compressed intended signals ($S_{intc}$) plus a host of compressed artifact signals ($S_{artc}$) from the compressor circuit, that is,

$$S_{ic} = \sum_1^m S_{intc} + \sum_1^n S_{artc} \tag{4.2}$$

where the summation extends over *m* compressed intended signals and *n* compressed artifact signals. The contaminated compressed signal $S_{ic}$ is then fed to a block of cascaded notch filters (NF1, NF2, …., NFm) in the ARTI system as shown in Figure 4.6. The various notch filters are tuned to the frequencies of the intended signals to eliminate all the compressed intended signals ($\sum_1^m S_{intc}$) and retain only the compressed artifact signals ($\sum_1^n S_{artc}$) at the output of the ARTI.

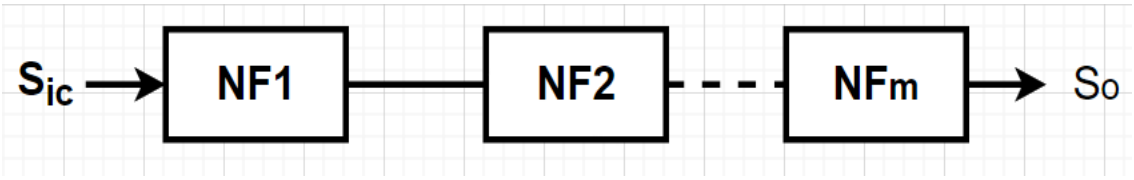



Figure 4. 6. ARTI block consisting of m notch filters

### 4.2.1: Design and implementation of the notch filters

In the proposed work, the active Twin T notch filter topology shown in Figure 4.7 is considered due to its high selectivity. An active Twin T notch filter is preferable to a passive Twin T notch filter, in view of the poor $Q_p$ factor in the latter arising out of resistive loses. A Feedback as shown in Fig.4.7 is employed to improve the quality factor.

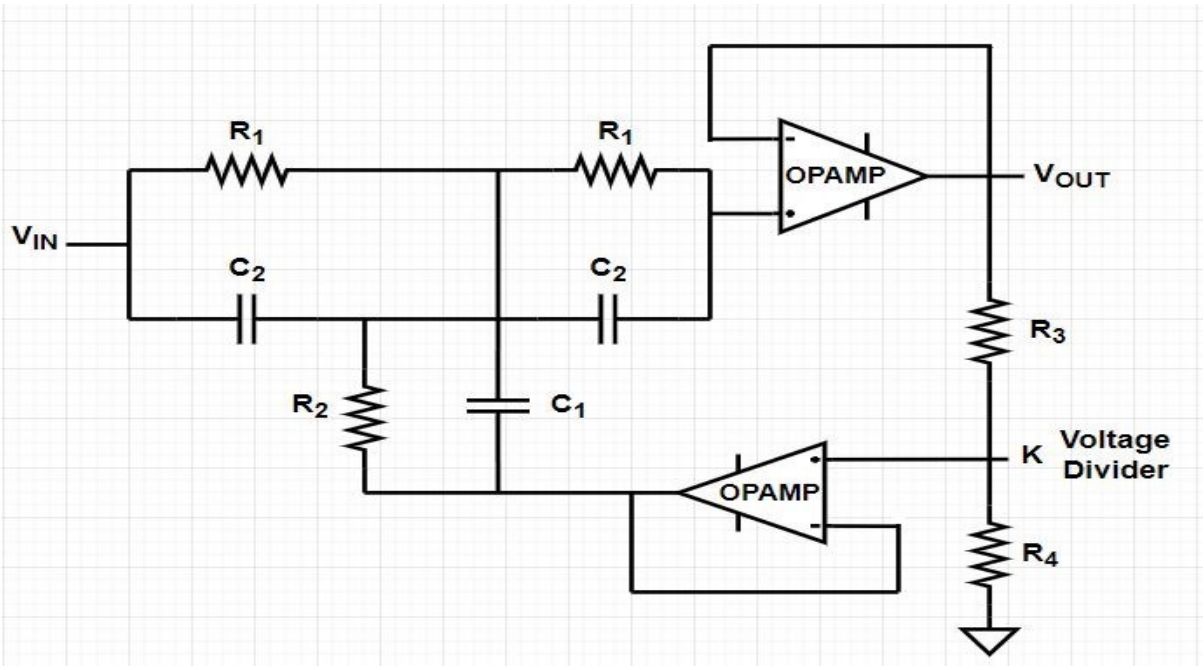



Figure 4. 7. Active twin T notch filter [26]

The value of the feedback signal (K) can be controlled by the resistors ($R_3$ and $R_4$) in the voltage divider which defines the quality factor ($Q_p$) of the notch filter [27]. The quality factor ($Q_P$) is given by [28]

$$K = \frac{R_4}{R_4+R_3} = 1 - \frac{1}{4Q_P} \tag{4.3}$$

and the notch frequency $f_n$ by [26],

$$f_n = \frac{1}{2\pi\sqrt{R1\times R2\times C1\times C2}} \tag{4.4}$$

We now chose $R_1 = 2R$ and $C_1 = 2C$ for the low pass filter-and $R_2 = R,\ C_2 = C$ for the high pass filter in Fig. 4.7.

Hence,

$$f_n = \frac{1}{2\pi\sqrt{2R\times R\times C\times 2C}} = \frac{1}{4\pi RC} \tag{4.5}$$

For implementing the notch filters in our simulation experiments, we will use the OPAMP [17] and pseudo resistor [22]-[24], which have been introduced already in Chapter 3 of the thesis.

### 4.2.2: Investigation related to the notch frequencies of the notch filters

In our case, a typical EEG signal contaminated by artifact signals was analysed in MATLAB to know the various frequency components of the EEG signals present. The null frequencies of the active notch filters in NF are tuned to be equal to these EEG frequencies.

Figure 4.8(a) depicts a typical frequency domain plot of an artifact contaminated EEG signal in an experiment to recover the EEG signal in an fMRI set up [29] (courtesy PERFORM center Concordia University). Figure 4.8(b) shows a similar plot of a sample of the EEG signal (i.e., intended signal) only. Comparing Figures 4.8(a) and 4.8(b), it is apparent that the EEG signals have strong components around 0.5Hz (δ-wave), and 10Hz (α-wave) with the artifacts principally spread over 0.2Hz to about 8.5 Hz, and from 12Hz onwards in Fig. 4.8(a). For the time being, we are ignoring the presence of β and γ waves of EEG signal. The purpose of the adaptive filter (Fig.1.7) is to recover the desired (EEG) signal (i.e., δ, and α) in real-time without using any computing machine.

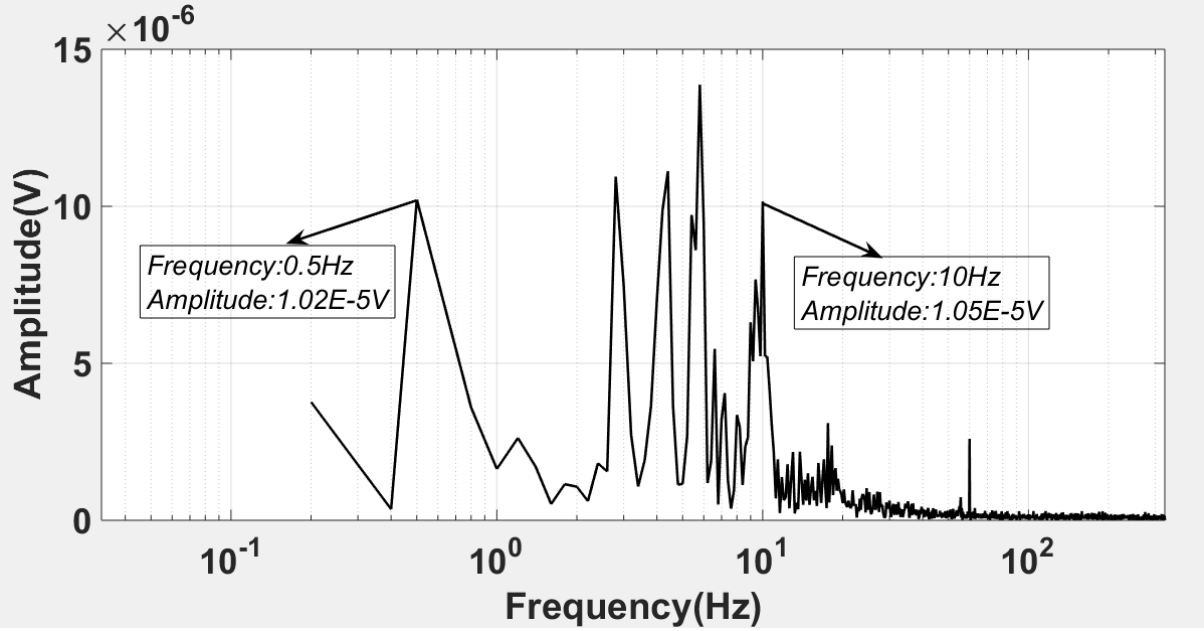



Figure 4. 8(a). Spectral density plot of the contaminated signal

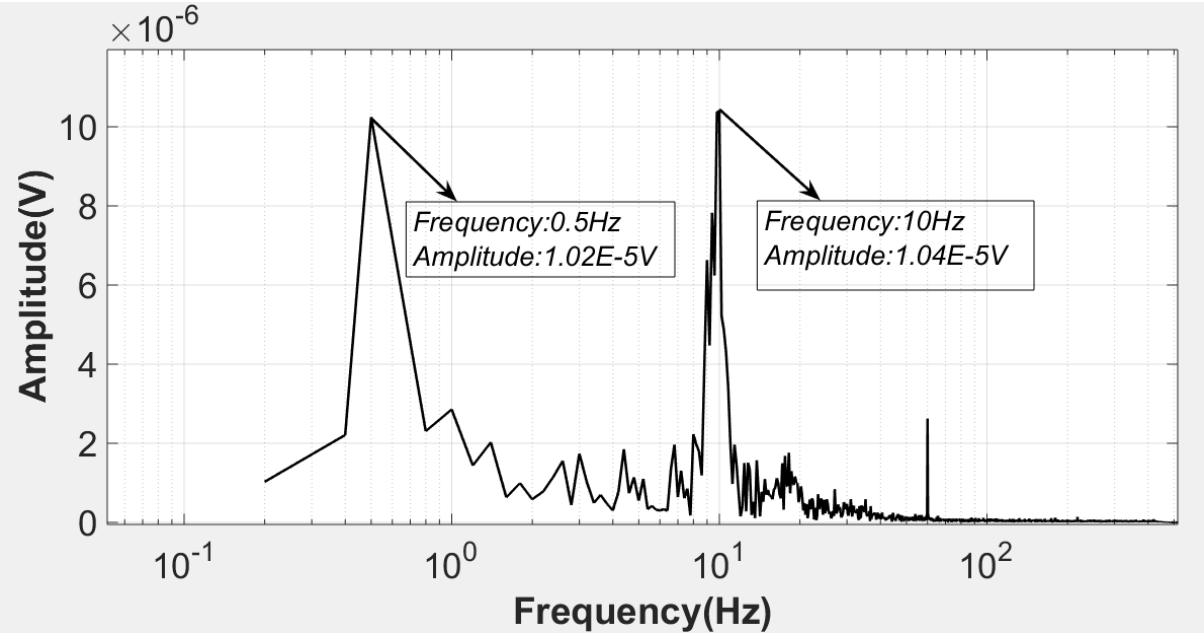



Figure 4. 8(b). Spectral density plot of the desired signal

### 4.2.3: Components design for the notch filters

Considering (4.5), for a null frequency of 0.5Hz, the time constant (RC) of the notch filter will be very high. A resistor value of $R = R_2 = 39.8G\Omega$ is obtained when a capacitor of value $C = C_2 = 4pF$ is chosen in designing a twin T notch filter. Hence, $R_1 = 2R$ and $C_1 = 2C$ will become $79.6G\Omega$ and $8pF$ respectively.

Similarly, for the 10Hz null frequency, the time constant (RC) will be somewhat lower. A capacitor value of $C = C_2 = 2.5pF$ results in a resistor value of $R = R_2 = 3.2G\Omega$. Hence, Hence, $R_1 = 2R$ and $C_1 = 2C$ of the active notch filter will become $6.4G\Omega$ and $5pF$ respectively.

According to the analysis of the standard second order notch filter in Chapter 2 of the thesis, it has been observed that signals away from the notch frequency experience negligible phase and magnitude changes when the notch filter has $Q_p \geq 10$. Hence, $Q_p = 10.25$ is considered in designing and implementation of twin T notch filters for both $0.5Hz$ and $10Hz$ null frequencies. Considering (4.3), resistor value of $R_3 = 3.2G\Omega$ and resistor $R_4 = 124.8G\Omega$ produces $Q_p = 10.25$.

These high resistance values can be conveniently realized in CMOS technology by adopting the MOS pseudo resistor configurations as we have already elaborated in subsection 3.6.1. The resistors in Figure 4.7 can be replaced by MOS pseudo resistors shown in Fig. 3.11(b) which is repeated here as Figure 4.9 by varying the aspect ratio of the PMOS transistors and adjusting the gate voltage ($V_G$) so that the transistor functions in the sub-threshold region of conduction. Referring to Figure 3.13, resistance of 30.1 Giga-ohms can be obtained with $W = 20$ micron and $W/L = 4$. In the case of the 0.5Hz notch frequency, to obtain exact value of $R_2 = 39.8G\Omega$, the width and the length of $M_{R1}$ as well as $M_{R2}$ are varied to 18μ and 5.6μ, respectively as shown in Fig. 4.9. The gate voltage ($V_G$) is set to $15mV$ for each transistor. Similarly, from the

Figure 3.13 we find that a resistance of 70.2 Giga-ohms can be obtained with $W = 20$ microns and $^{W}/_{L} = 1.05$. So, get $R_1 = 79.6G\Omega$ the widths of both $M_{R1}$ and $M_{R2}$ are varied to be 18µ, but the lengths are set to 17µ. The gate voltage ($V_G$) is also set to 15mV.

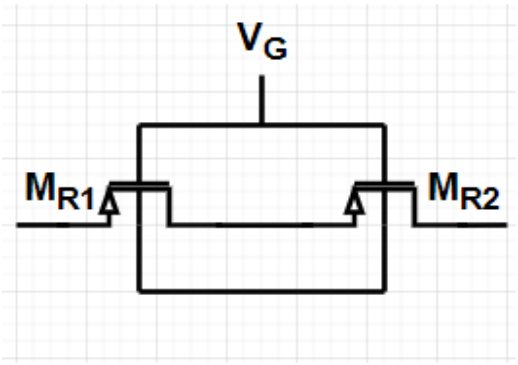



Figure 4. 9. Pseudo resistor

From the Figure 3.13 we find that a resistance of 4.33 Giga-ohms can be obtained with $W = 80$ microns and $^{W}/_{L} = 1.0$ . In the case of 10Hz notch frequency, to get $R_2 = 3.2G\Omega$, the widths and the lengths of $M_{R1}$ and $M_{R2}$ are set to 79.4µ and 1µ, respectively. The gate voltage ($V_G$) is set to 5mV. From the Figure 3.13, a resistance of 7.62 Giga-ohms can be obtained with $W = 40$ microns and $^{W}/_{L} = 1$. Similarly, to obtained $R_1 = 6.4G\Omega$ the widths and the lengths of both $M_{R1}$ and $M_{R2}$ are changed to 39.7µ and 1µ, respectively. The gate voltage ($V_G$) applied to the pseudo resistor in Fig.4.9 is set to 5mV.

Moreover, the voltage divider resistors, $R_3$ and $R_4$ in both 0.5 Hz and 10Hz notch frequency twin T notch filters are also replaced by the same MOS pseudo resistor configuration shown in Fig. 4.9. The resistor $R_3 = 3.2G\Omega$ is replaced by the circuit of Fig. 4.9 with the widths and lengths adjusted to 79.4µ and 1µ, respectively. The gate voltage ($V_G$) is set to 5mV. In the case of $R_4 = 124.8G\Omega$, the widths and the lengths of both $M_{R1}$ and $M_{R2}$ are set to 5µ and 2.6µ respectively, with the gate voltage ($V_G$) being 15mV.

We now present in Tables 4.2 and 4.3 the designed component parameters of the active Twin T notch filters used in our case. The attenuation depths of the notch filters are also included in the Tables. Figure 4.10 and Figure 4.11 depict the frequency responses of the notch filters with notch frequencies of 0.5Hz and 10Hz, respectively. The simulations were carried out using components from the CMOSP180 technological process, available in the VLSI laboratory of Concordia University.

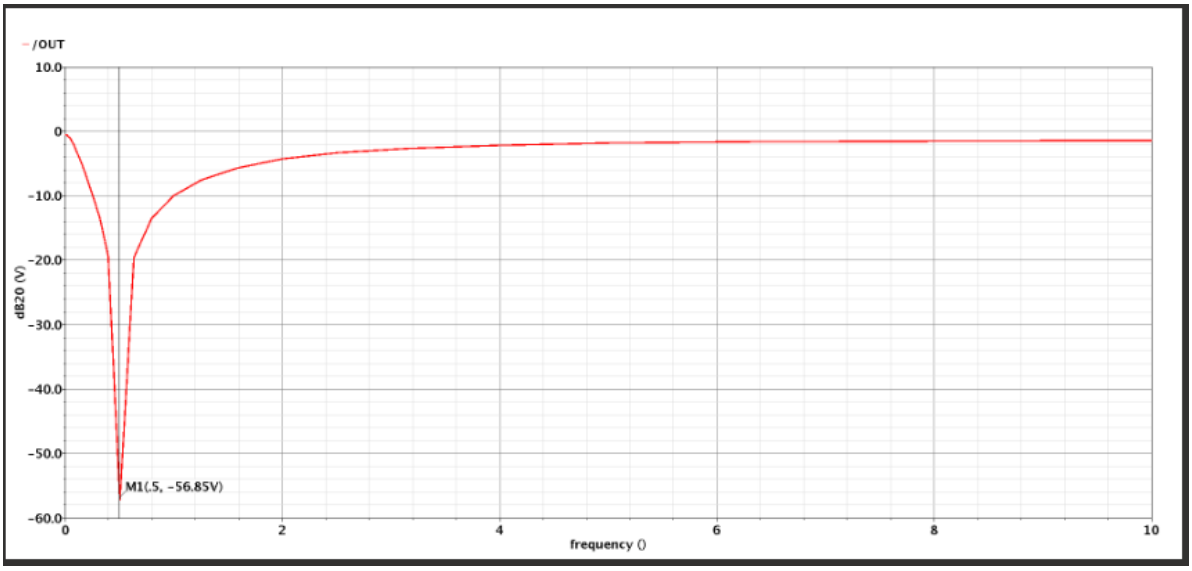



Figure 4. 10. Frequency response of notch filter with $f_n = 0.5$Hz

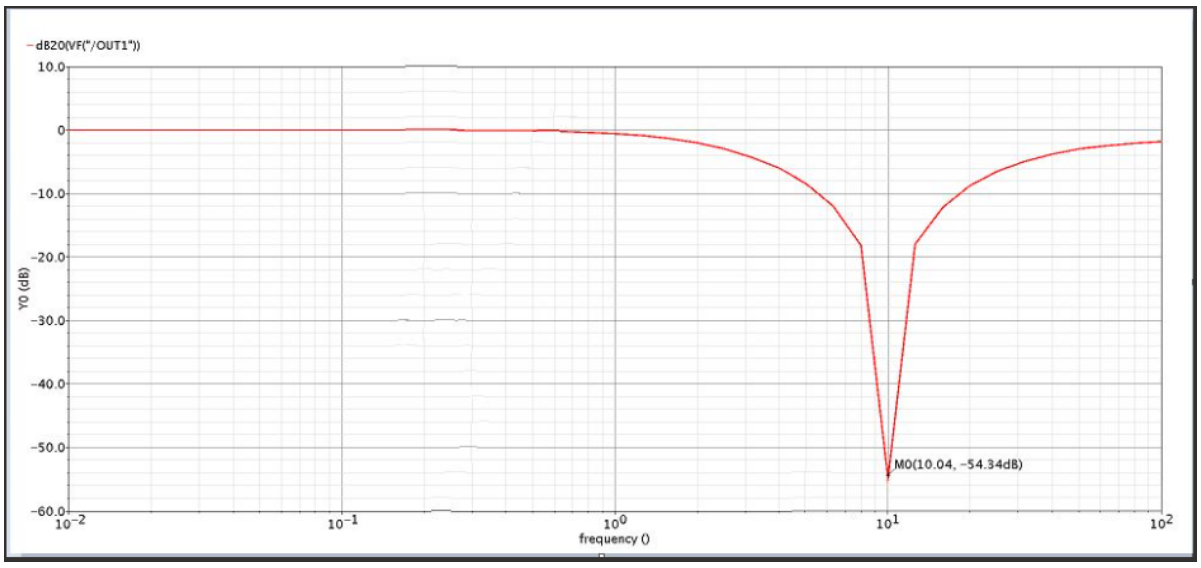



Figure 4. 11. Frequency response of notch filter with $f_n = 10$Hz

Table 4. 2: Design parameters and simulation results for the notch filter with $f_n = 0.5\text{Hz}$

| Transistors | W(microns) | L(microns) | $^{W}/_{L}$ |
|---|---|---|---|
| $M_{R1}, M_{R2}$ (for $R_2$) | 18 | 5.6 | $^{18}/_{5.6}$ |
| $M_{R1}, M_{R2}$ (for $R_1$) | 18 | 17 | $^{18}/_{17}$ |
| $M_{R1}, M_{R2}$ (for $R_3$) | 79.4 | 1 | $^{79.4}/_{1}$ |
| $M_{R1}, M_{R2}$ (for $R_4$) | 5 | 2.6 | $^{5}/_{2.6}$ |
| $R_1 = 79.68\text{G}\Omega, R_2 = 39.8\text{G}\Omega, R_3 = 3.2\text{G}\Omega, R_4 = 124.8\text{G}\Omega$<br>$C_1 = 8\text{pF}, C_2 = 4\text{pF}$ | | | |
| $Q_p = 10.25$ | | | |
| Attenuation Depth | | 56.85dB | |

Table 4. 3: Design parameters and simulation results for the notch filter with $f_n = 10\text{Hz}$

| Transistors | W(microns) | L(microns) | $^{W}/_{L}$ |
|---|---|---|---|
| $M_{R1}, M_{R2}$ (for $R_2$) | 79.4 | 1 | $^{79.4}/_{1}$ |
| $M_{R1}, M_{R2}$ (for $R_1$) | 39.7 | 1 | $^{39.7}/_{1}$ |
| $M_{R1}, M_{R2}$ (for $R_3$) | 79.4 | 1 | $^{79.1}/_{1}$ |
| $M_{R1}, M_{R2}$ (for $R_4$) | 5 | 2.6 | $^{5}/_{2.6}$ |
| $R_1 = 6.4\text{G}\Omega, R_2 = 3.2\text{G}\Omega, R_3 = 3.2\text{G}\Omega, R_4 = 124.8\text{G}\Omega$<br>$C_1 = 5\text{pF}, C_2 = 2.5\text{pF}$ | | | |

| $Q_p = 10.25$ | |
|---|---|
| Attenuation Depth | 54.84dB |

### 4.3: Conclusion

This chapter has focused on the detailed implementation of the compressor and expander circuits, which are parts of the system shown in Chapter 1. The design and implementation of active notch filters with notch frequencies of 0.5Hz and 10Hz, which are used to separate the intended EEG signals and the artifact signals, has been described. Finally, simulation results using transistors from CMOS 180nm technology have been included in this chapter.

# Chapter 5

# Validation Results for the Proposed System

This chapter describes the validation results for the analog processing system proposed in Chapter 1 of the thesis. Schematic level simulations using components from the CMOSP180 technological process, available in the VLSI laboratory of Concordia University have been carried out.

### 5.1: Validation of the Operating Principles of the Proposed System

Consider Fig.1.7 in Chapter 1 repeated here as Fig.5.1. The input amplifier block (S_ARRAY) receives the signals of interest (intended signals) plus artifact components coming from the sensor devices (i.e., an array of EEG recording electrodes). The intended signal values are of considerably smaller in magnitude than that of the artifact signals. The compressor reduces the amplitude levels of all the input signals, both the intended and artifact signals, but the reduction of higher-level artifact signal is more than that in the case of the intended signals. The ARTI block extracts the artifact signals by rejecting the intended signals. The operation with the ARTI block has been explained in Chapter four (Fig.4.6). The expander restores the magnitudes of the artifact signals to the levels that were present at the input of the compressor. The output of the expander constitutes the reference signal band which is used for the recovery of the intended signals. The operation is achieved by subtracting the reference signal band from the output of the S_ARRAY block (intended signal contaminated by the artifact signal). This is performed in the difference amplifier (D_AMP) shown in Fig.5.1. The output from the D_AMP is further processed using a bank of band-pass filters to obtain the intended signals. It is to be noted that in our case, we need only two band-pass filters since we are interested in

restoring only two of the four waves of the EEG signal, namely, the δ and α waves. The detailed design and implementation of these sub circuits except the BPFA sub block have been already discussed and analysed in the previous chapters.

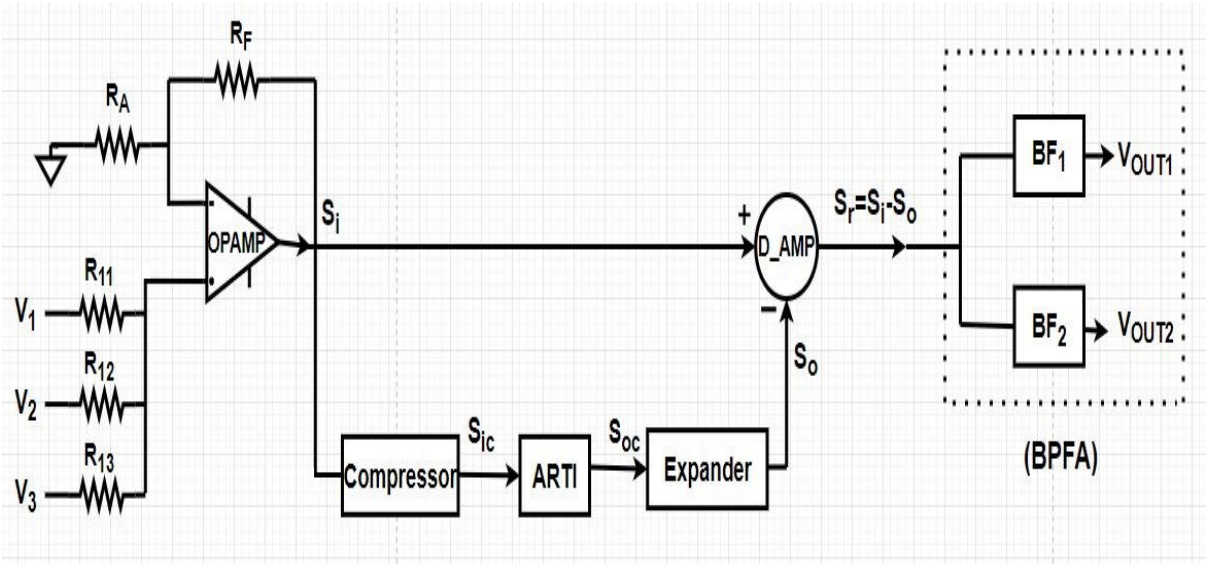



Figure 5. 1. The proposed system

**5.2: A Mixture of Two Sinusoidal Signals as the Artifact Signal**

In the experiment introduced earlier (Figure 5.1), the terminals V1 and V2 of the (S_ARRAY) block are fed with intended sinusoidal signals of 0.5Hz and 10 Hz with amplitudes of (20μV) and (35μV), respectively. In this experiment, we assume that the artifact signal is composed of a mixture of two sinusoidal signals one of 3Hz with an amplitude of 75μV and the other of 5Hz with an amplitude of 100μV. This artifact signal is fed to terminal V3. The compressor and expander circuits are the ones detailed in Chapter 4. The ART1 block consists of only two notch filters NF1 and NF2 tuned to 0.5 Hz and 10Hz, respectively. The different signal amplitudes are chosen with the condition that the artifact signals remain at levels higher than that of the intended signals.

Figures 5.2-5.7 depict the signals at various locations of the overall system. The results are produced by HSPICE S simulations on the VLSI CAD workstations in the VLSI laboratory of the Electrical and Computer Engineering department of Concordia University.

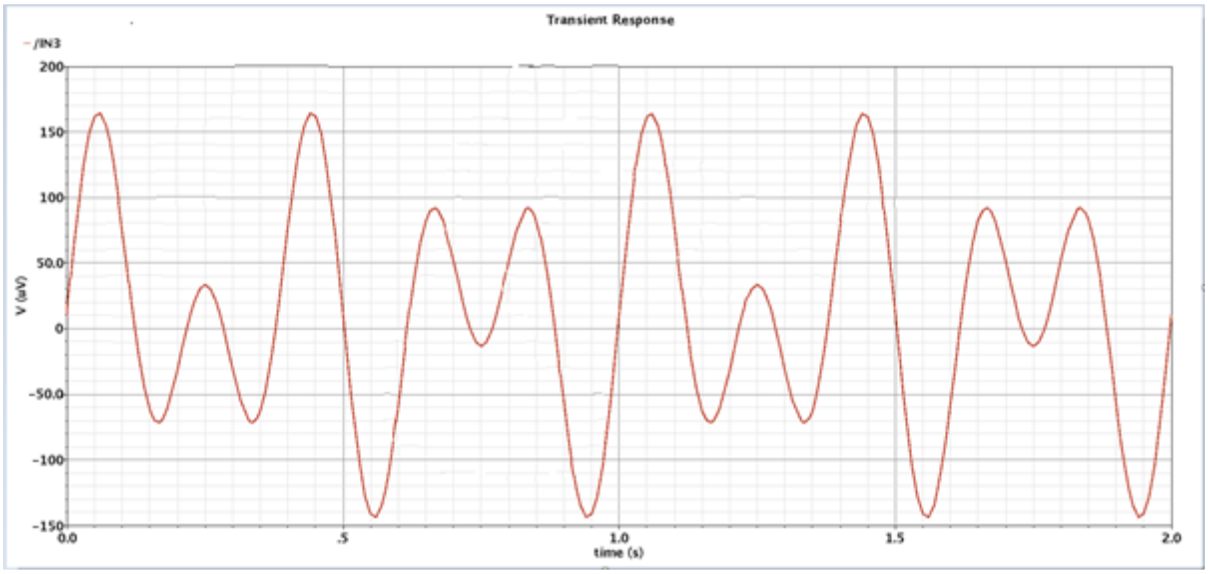



Figure 5. 2. Artifact signal $S_{art}$ applied to the terminal V3 in Fig. 5.1

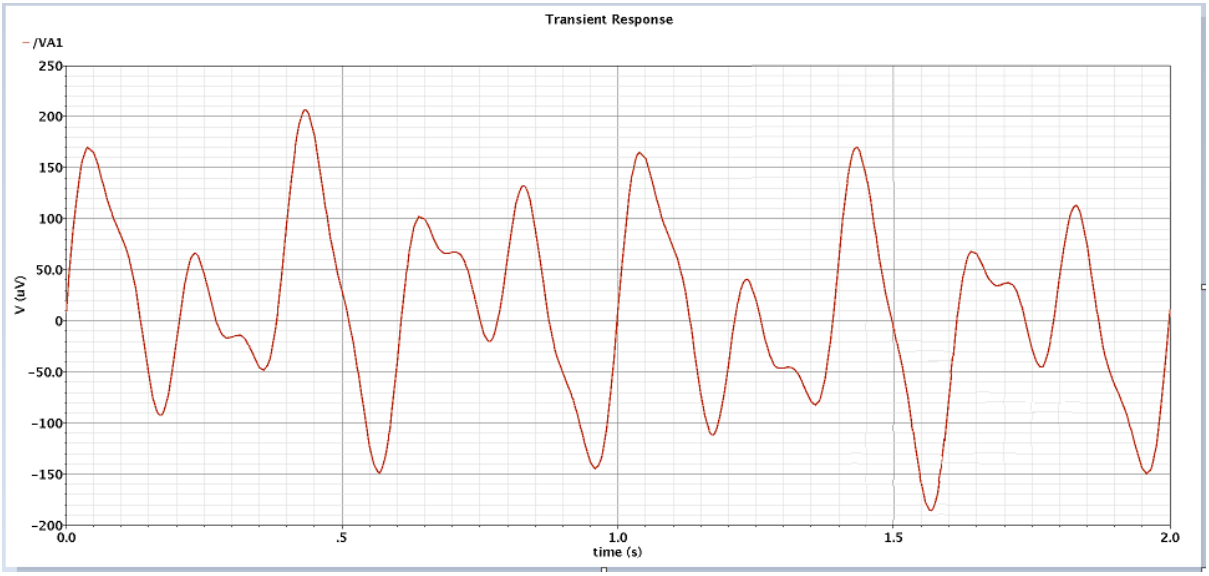



Figure 5. 3. Contaminated (desired plus artifact) signal $S_i$ at the output of the sensors array (S_ARRAY) in the system

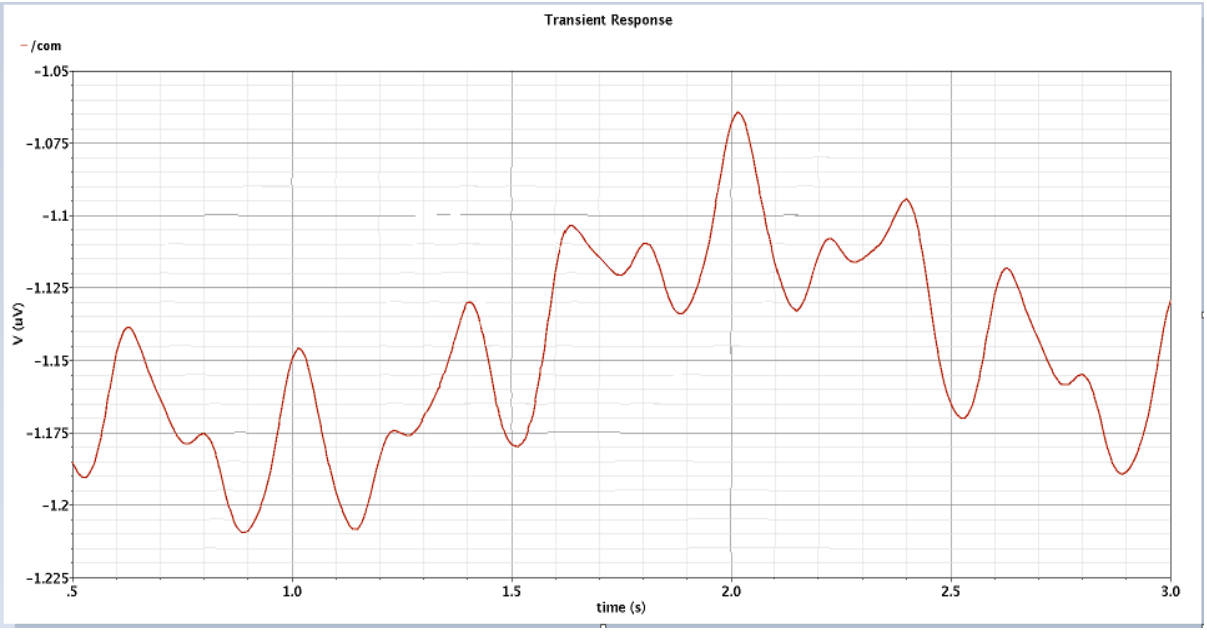



Figure 5. 4. Contaminated signal $S_{ic}$ at the output of the compressor (COMPR)

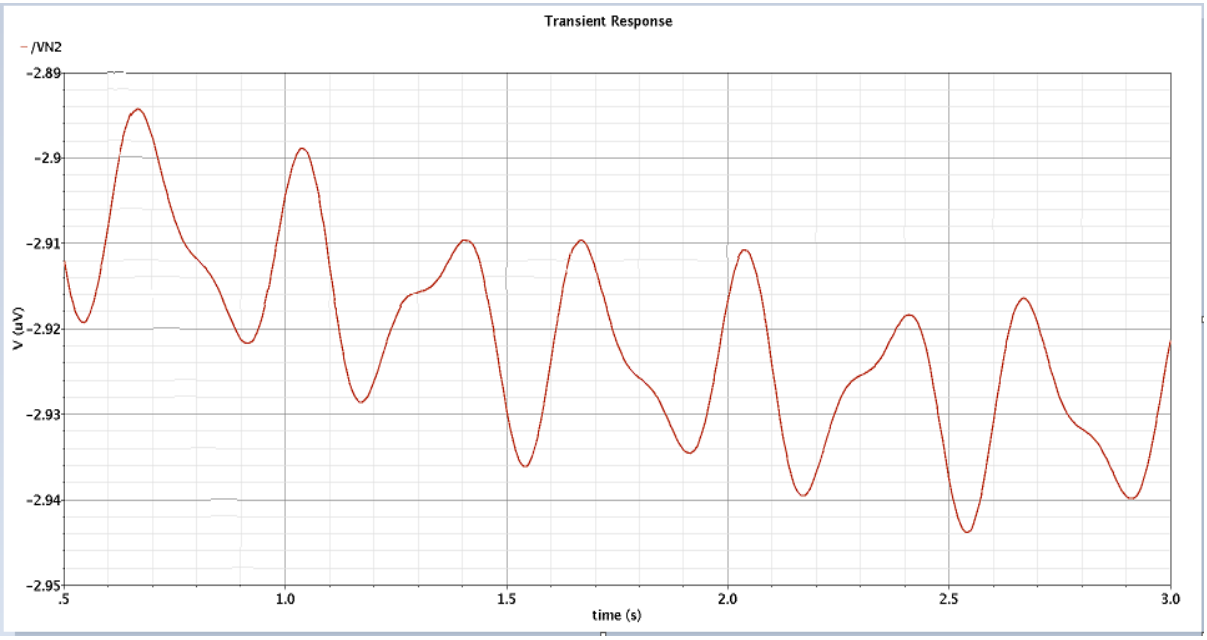



Figure 5. 5. Artifact signal $S_{oc}$ at the output of the cascaded notch filters in ARTI

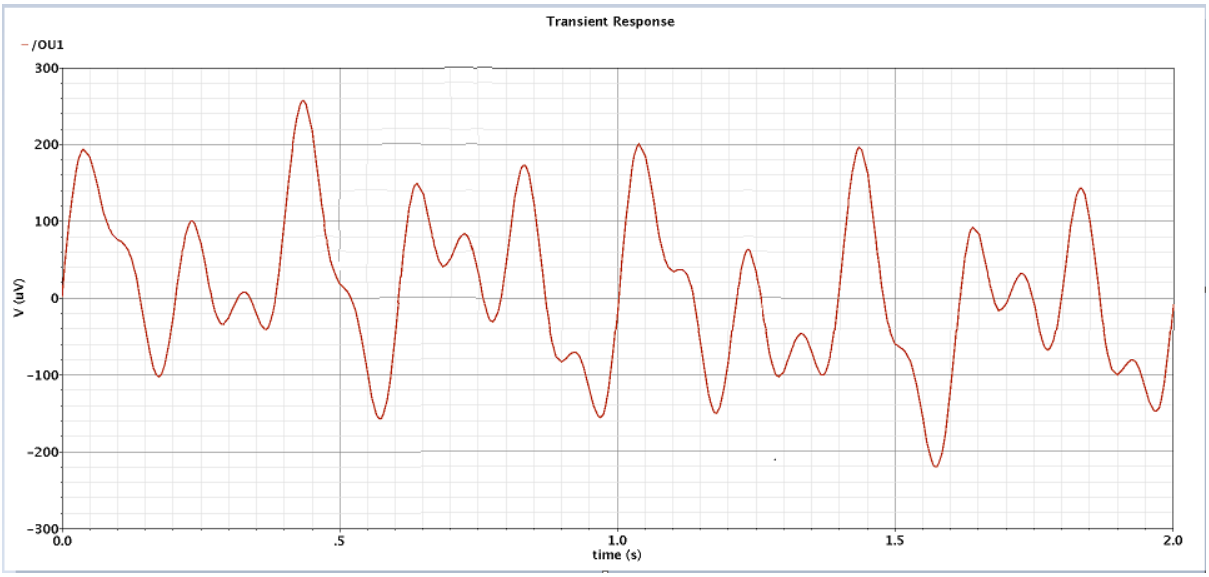



Figure 5. 6. Recovered artifact signal $S_o$ at the output of the expander (EXPDR)

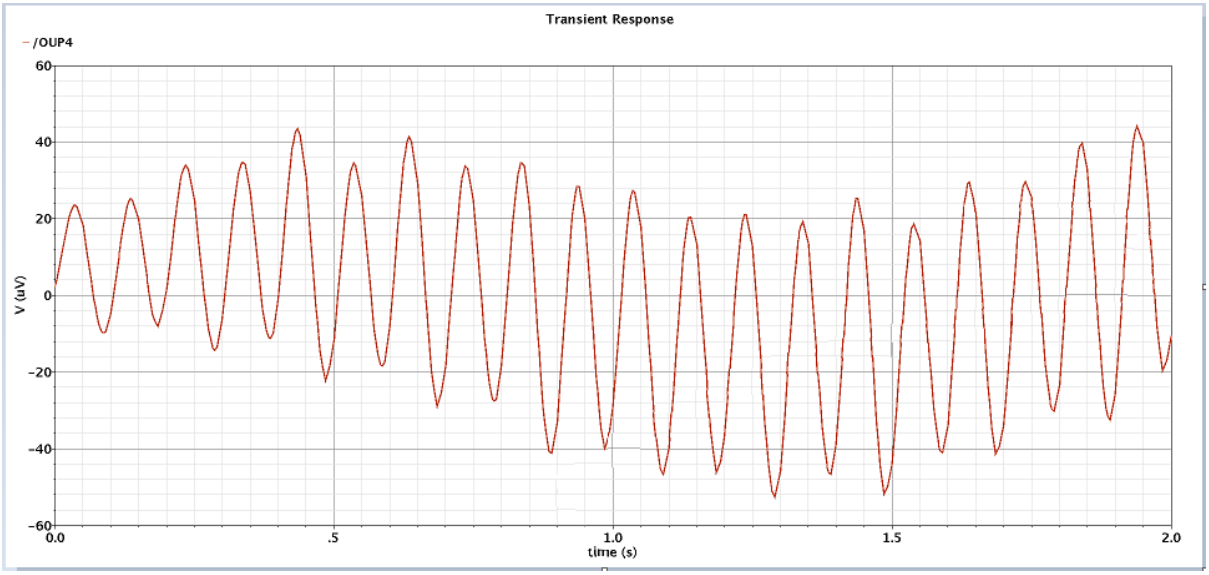



Figure 5. 7. Recovered desired signal $S_r$ at the output of D_AMP in Fig.5.1

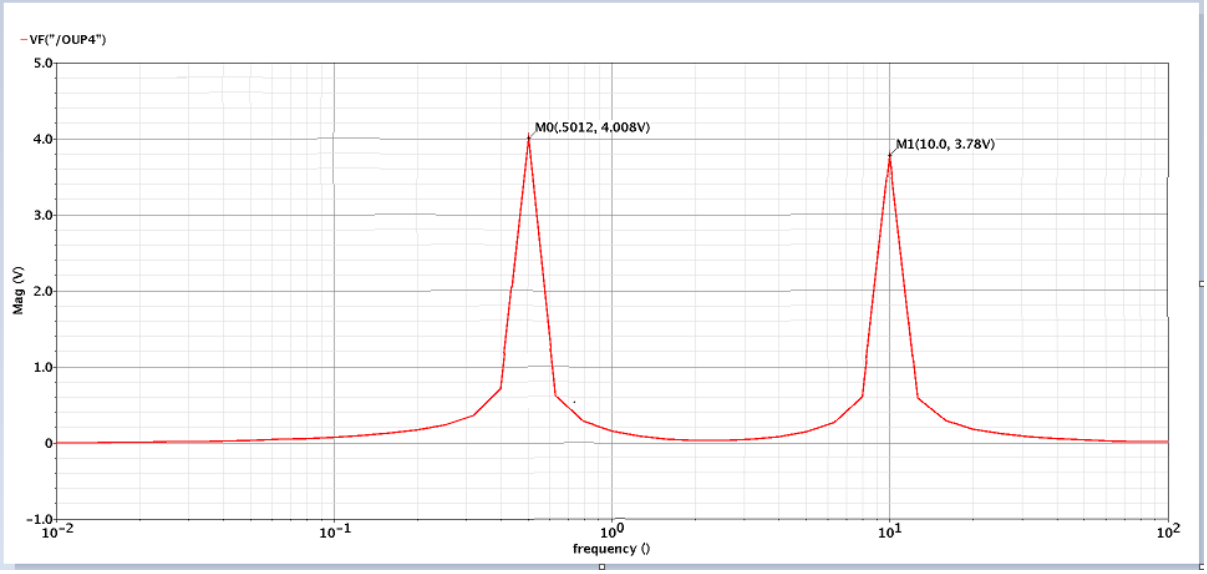



Figure 5. 8. Frequency spectrum at the output of D_AMP in Fig.5.1

Figure 5.2 shows the artifact signal applied to the terminal V3 of the S_ARRAY in the proposed system. Figure 5.3 shows the output of S_ARRAY. The signal $S_i$ at the output of the compressor as well as $S_{oc,}$ the output of the cascaded notch filters as shown in Fig. 5.4 and Fig. 5.5, respectively, experience non-uniform dc shift as the results of the non-linearity introduced by the compressor subsystem. The recovered artifact signal $S_o$ is shown in Fig. 5.6. Comparing the input artifact signal shown in Fig. 5.2 with that of the recovered artifact signal, it is seen that the latter has a few extra peaks superimposed on it. This is due to the fact that the notch filters in ARTI subsystems could not completely eliminate the intended signal to zero. The frequency spectrum shown in Fig. 5.8 validates that the interfering signal has been suppressed completely by the proposed system shown in Fig. 5.1.

### 5.3: Arbitrary Signal as Artifact Signal

In the previous section, we have presented the final phase in the retrieval scenario of the intended EEG signals in presence of an artifact signal that was a mixture of two sinusoidal signals (whose amplitudes were much higher than that of the intended signals), using the proposed filtering system. It is intuitive that a combination of several sinusoidal signals with

large amplitudes may be used to simulate an arbitrary artifact signal, the only requirement being that the constituents of the artifact signal do not contain the frequency components of the original EEG (i.e., the intended) signals; in such a case, the proposed system can be employed to eliminate such an artifact signal. To verify the above statement, a signal wave mimicking an ECG waveform [30] was created empirically to be used as an artifact signal using pulse input signals, several RC elements, integrators, and inverting amplifiers.

In this experiment, the terminals V1 and V2 of S_ARRAY are fed with intended signals at 0.5Hz (20μV) and 10Hz (35μV), respectively. The terminal V3 of the summing amplifier is fed with the ECG signal (artifact signal) shown in Fig. 5.9. Figures 5.9-5.15 show the simulation results at various locations of the proposed system, when the generated ECG signal is considered an artifact signal. Once again, it is clear from the frequency spectrum shown in Fig. 5.15 that the interfering signal has been suppressed completely by the proposed filtering system shown in Fig. 5.1 and the desired signal properly recovered.

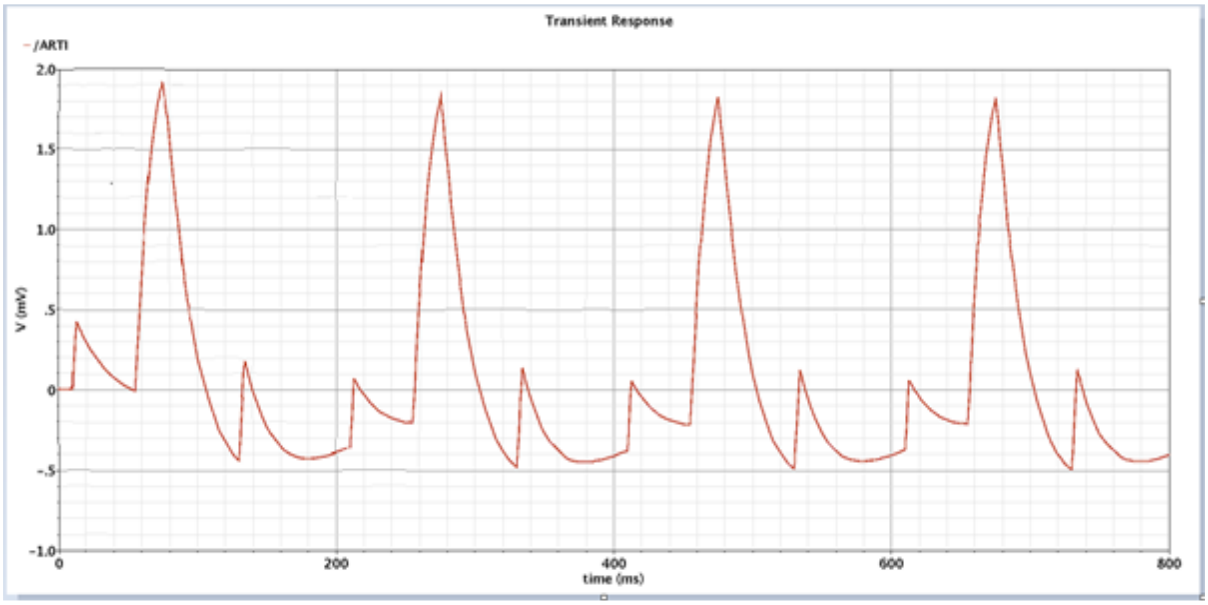



Figure 5. 9. Mimic ECG waveform as the artifact signal $S_{art}$ fed at terminal $V_3$ in Fig. 5.1

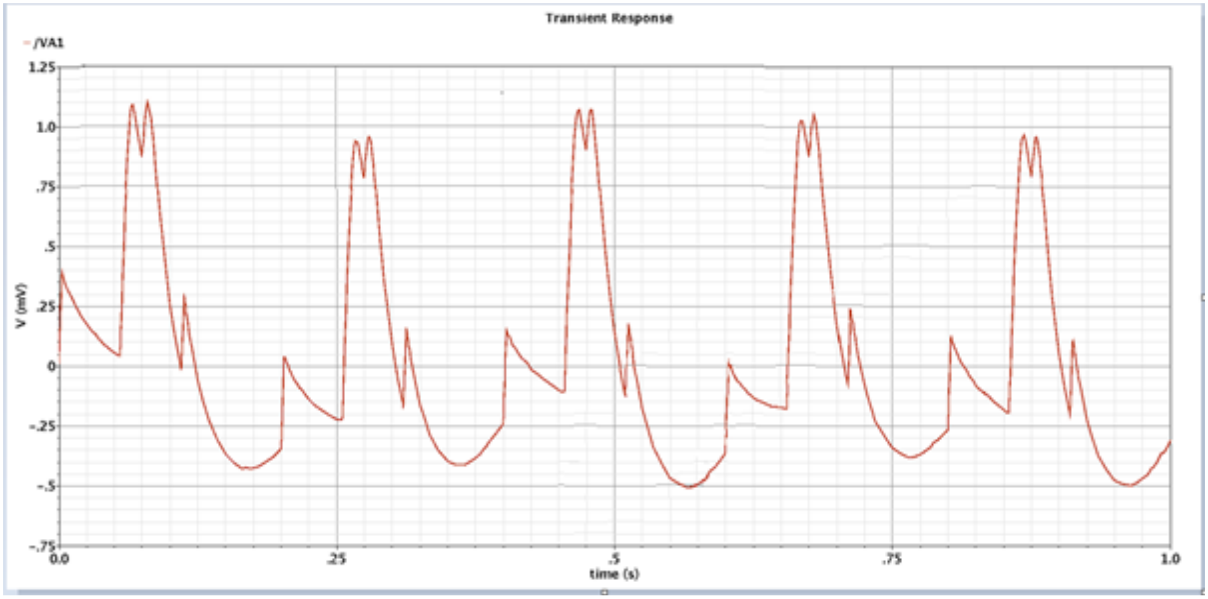



Figure 5. 10. Contaminated (desired plus artifact) signal $S_i$ at the output of the summer (S_ARRAY)

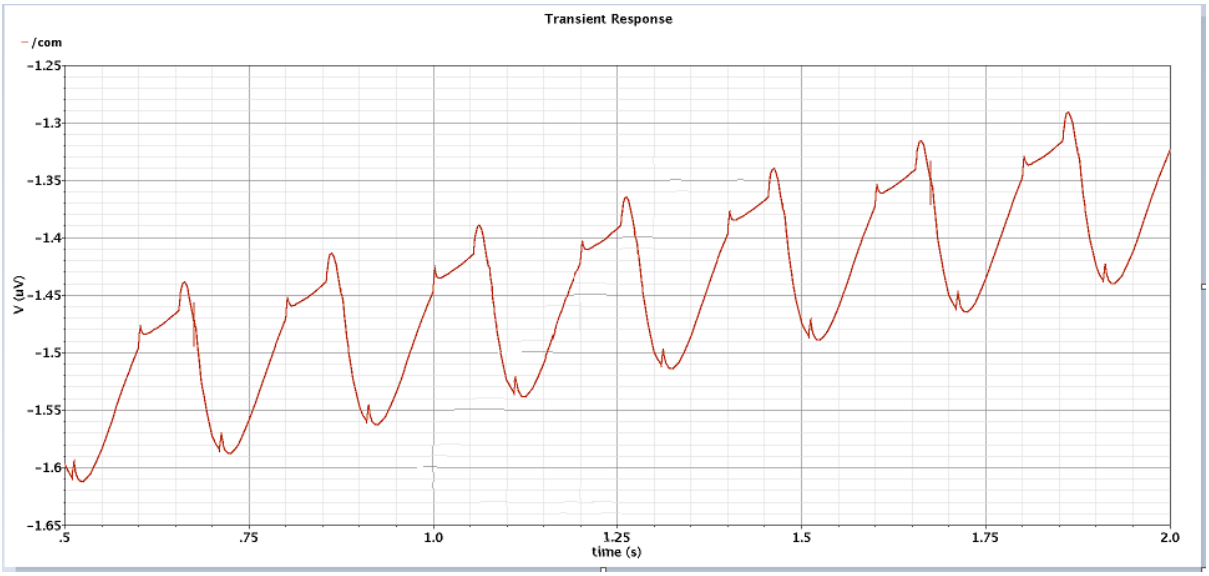



Figure 5. 11. Contaminated signal $S_{ic}$ at the output of the compressor (COMPR)

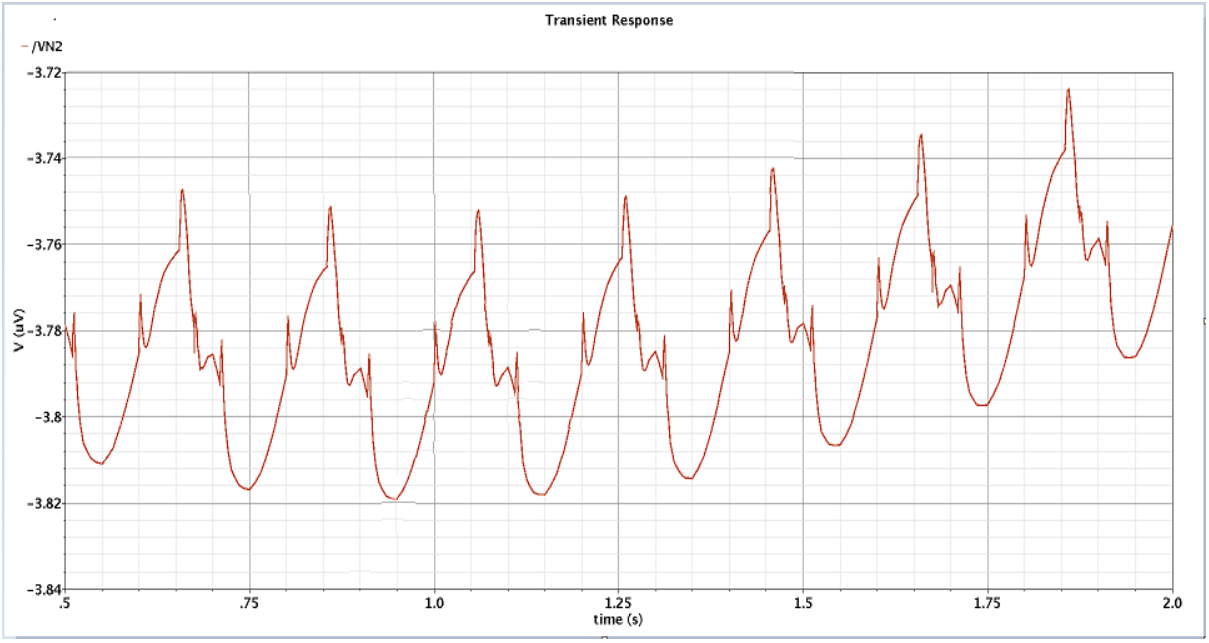



Figure 5. 12 Artifact signal $S_{oc}$ at the output of the cascaded notch filters in ARTI

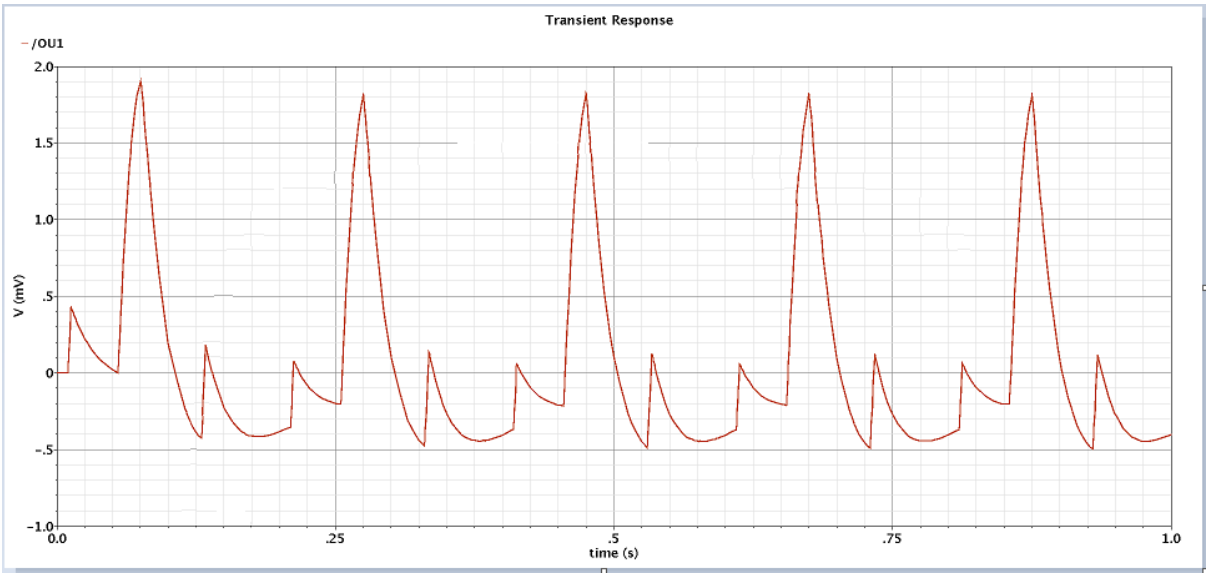



Figure 5. 13. Recovered artifact signal $S_o$ at the output of the expander (EXPDR)

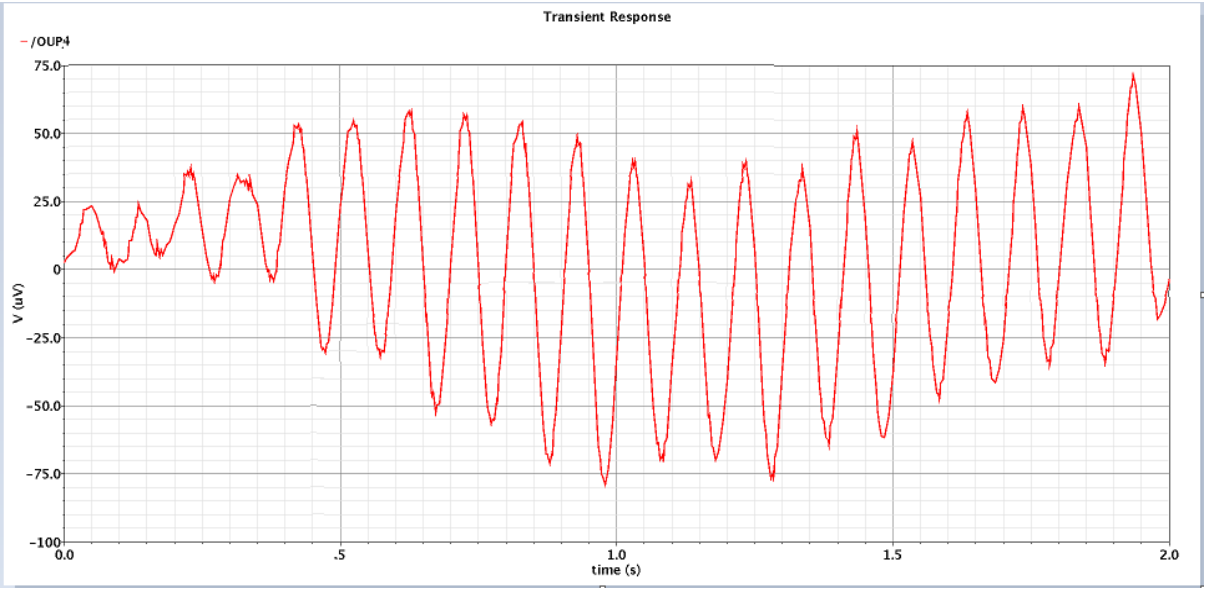



Figure 5. 14. Recovered desired signal $S_r$ at the output of D_AMP in Fig.5.1

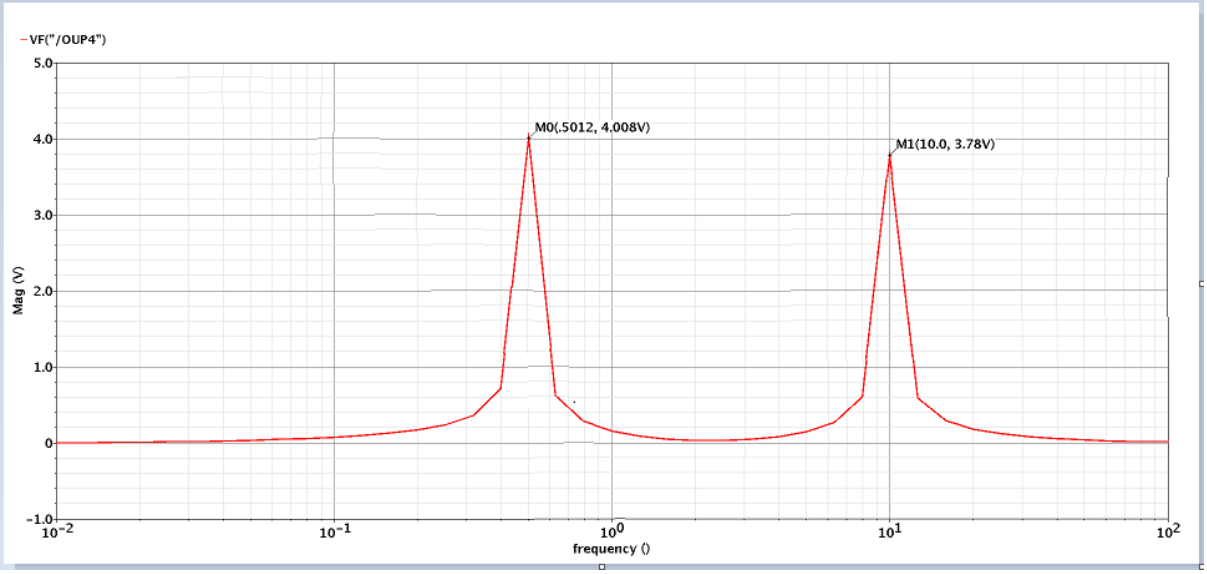



Figure 5. 15. Frequency spectrum at the output of D_AMP in Fig.1.5

It is seen from the above two experiments, that the artifact signals are completely suppressed by the proposed filtering system. The proposed system will have only the intended signals at the output of D_AMP shown in Fig.5.1. To separate the individual signals (i.e., 0.5Hz and 10Hz) present at the output of D_AMP, one needs to pass the combined signals through the band pass filter array (BPFA) explained in Section 5.4.

### 5.4: Band Pass Filter Array (BPFA)

Consider an array of bandpass filters, as shown in Figure 5.16. The first band pass filter is realized by feeding the output $S_r$ from the difference amplifier in Figure 5.1 to the positive terminal of another difference amplifier and also to the negative terminal of the difference amplifier, however, through the notch filter $NF_1$ that is used in the ART1 block. In a similar manner, the other ($m$ – 1) band pass filters are realized by using the various notch filter $NF_2$, …, $NF_m$ used in the ART1 block of Figure 5.1. It is clear from Figure 5.16 that for the $i$ th section, we have

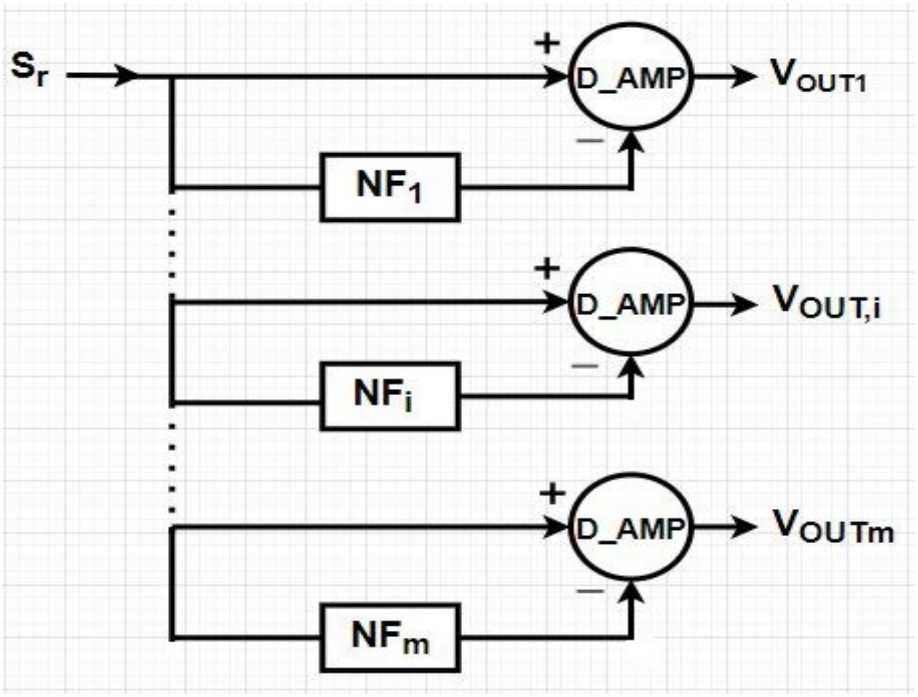



Figure 5. 16. Realization of the bandpass filters

$$\frac{V_{OUT,i}}{V_{in}} = \frac{V_{OUT,i}}{S_r} = \left(1 - \frac{s^2+\omega_i{}^2}{s^2+\frac{\omega_i}{Q_P}s+\omega_i{}^2}\right) = \frac{\frac{\omega_i}{Q_P}s}{s^2+\frac{\omega_i}{Q_P}s+\omega_i{}^2} \tag{5.1}$$

which is a second order BPF centered around the frequency $\omega_i$. Hence, only the signal at the frequency $\omega_i$ in $S_r$ will be retained $V_{OUT,i}$, while the other components will be eliminated. It

follows that when there are several frequency components present in the recovered EEG signals, a designer can use the above configuration to separate the individual EEG signals.

### 5.4.1: Output of $BF_1$ and $BF_2$

In our present case, there are only two individual EEG frequencies (namely, 10Hz and 0.5Hz) that are present at the output of the D_AMP shown in Fig.5.1. Hence, the bandpass filters at the above frequencies are implemented using the arrangement shown in Fig.5.16 using notch filters NF1 and NF2 operating at notch frequencies of 10Hz and 0.5Hz, respectively. Figures 5.17 and 5.18 show the experimental results for the outputs $V_{OUT1}$ and $V_{OUT2}$ of the two bandpass filters. It is clearly seen that the two original signals corresponding to the δ and $\alpha$ waves of the EEG signal have been recovered properly and the artefact signals have been completely eliminated.

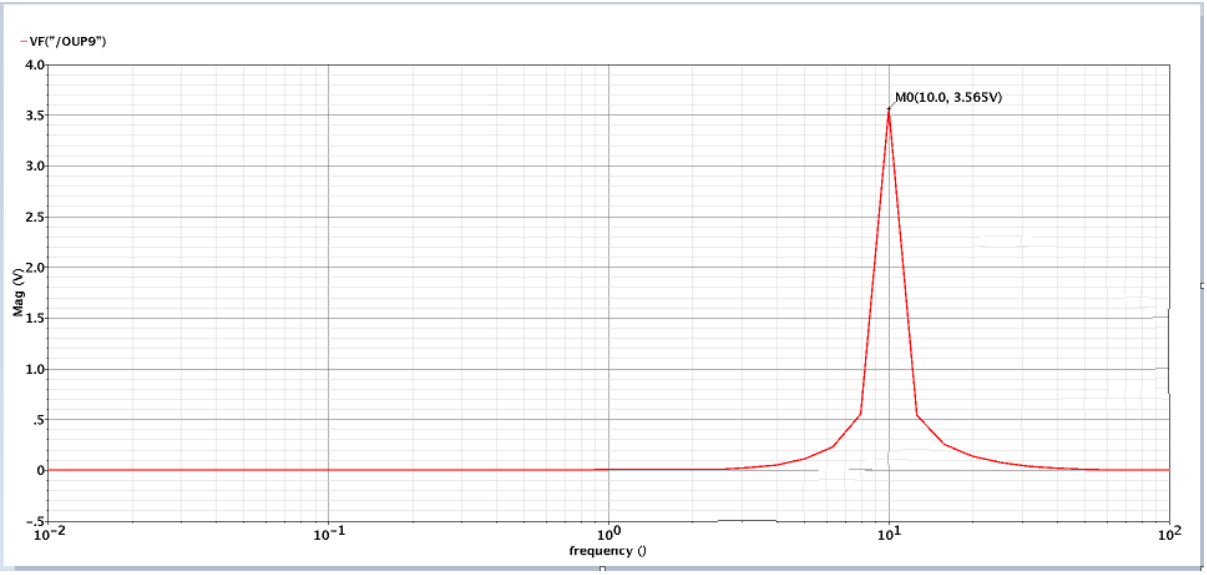



Figure 5. 17. Frequency spectrum of the output of $V_{OUT1}$ (10Hz)

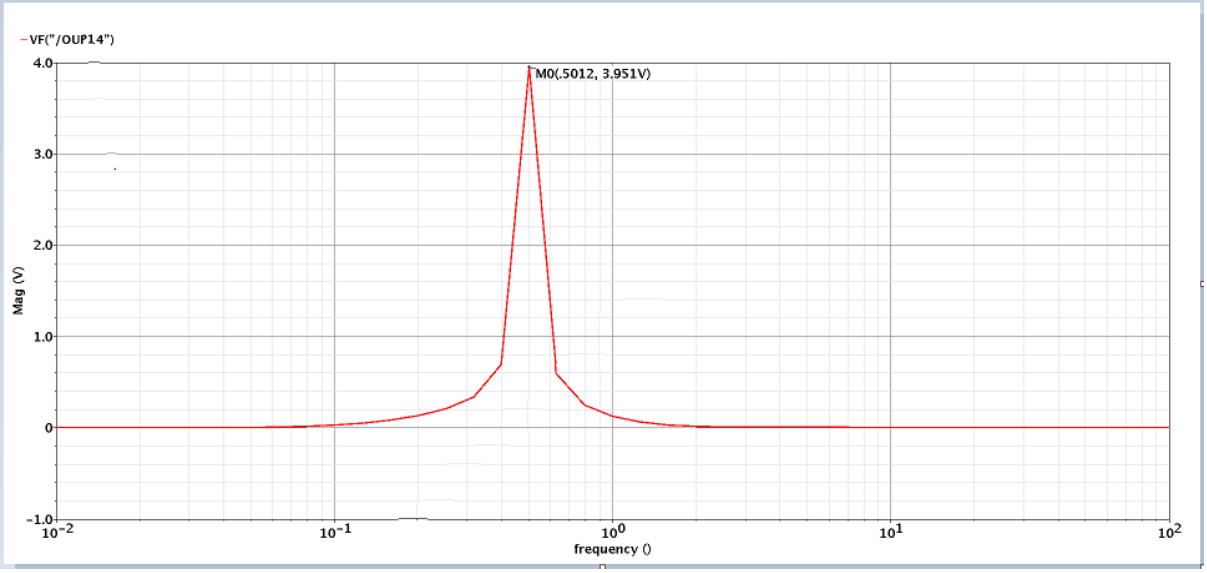



Figure 5. 18. Frequency spectrum of the output of $V_{OUT2}$ (0.5Hz)

Since we are only interested in our present case in extracting two species of the EEG signal, namely, the $\delta$ and $\alpha$ waves, we can have a very simple structure to extract the two waves from $S_r$ in a very simple manner without the need for the difference amplifier and the bandpass filter array (BPFA). This structure is shown in Figure 5.19. The recovered output signal $S_r$ from the difference amplifier, when fed to the notch filter NF2 with the notch frequency of 0.5Hz, the notch filter will supress the 0.5Hz signal and will result in the output $V_{OUT1}$ of the 10Hz as shown in Figure 5.17. Similarly, when the signal $S_r$ is inputted to the notch filter NF1 with the notch frequency of 10Hz, the notch filter will supress the 10Hz signal and will result in the output $V_{OUT2}$ of the 0.5Hz as shown in Figure 5.18.

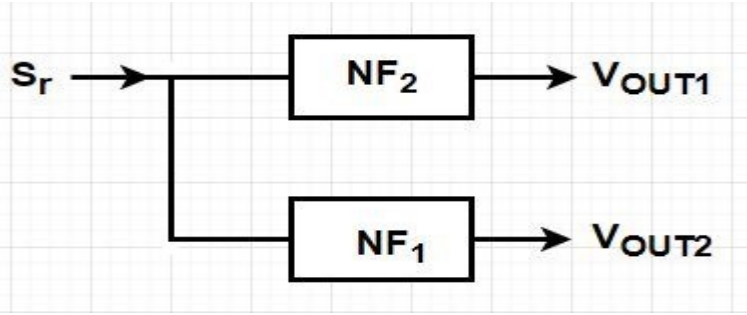



Figure 5. 19. Separation of the $\delta$ and $\alpha$ waves

## 5.5: Conclusion

In this chapter, we have presented the synopsis of the whole system proposed in chapter 1. We focused on the validation of our proposed system in separating the EEG desired signal corrupted by an artifact signal, by using a mixture of two sinusoidal signals as well as a mimic ECG-generated signal as artifact signals. The implementation and simulation of the proposed system were conducted at schematic capture level in CMOS180 technology.

# Chapter 6

# Conclusion and Future Works

This chapter summarizes the key contributions pertaining to the design, analysis and implementation of the proposed analog filtering system for eliminating artifact signals from contaminated EEG signal. It also highlights possible future research based on the work presented in the thesis.

### 6.1: Conclusion

- In Chapter 1, the motivation to propose a method to recover certain physiological signals in the presence of disturbing artifact signals is explained. Specific goal was to use analog/mixed mode circuit techniques to reach the objective. Analog circuit techniques quite often lead to saving in power and offer the possibility of real time observations. This also has potentials of hardware implementation using available integrated circuit technological process.

  It was quickly realized that an alternative means of elimination of the artifact signals is to remove the intended signal from a mixture of these two kinds of signals. Then, only the artifact signal remains available to be used as a reference signal to be discarded, as is the practice in many adaptive filtering system.

  This twist in recovering the artifact signals by elimination of the intended signal is the niche in the proposed work in contrast with the conventional adaptive filtering route. The domain of signals chosen was the EEG signals in view of the potential of coming up with an electronic device that can be adopted in

mobile health care systems. A review of currently published work on adaptive filtering was carried out, and a technique which has not yet been pursued by other researchers (to the best of the author's knowledge) has been introduced.

- From the basics of filtering theory of signals, it is known that a notch filter can eliminate a specific signal from a mixture of several signals. Thus, elimination of the intended signal by a notch filter to isolate the artifact signals seemed to be the right direction to adopt. However, the issue of imperfect filtering of the artifact signals arise when a component of the artifact signal remains close to the band of intended signals. Thus, we embarked on investigating the issue of decisive elimination of the artifact signal band, when these signals occur close to the stop band of the intended signals.

  In Chapter 2 of the thesis, a study of the characteristics of second order notch filters was carried out, which revealed that the higher the selectivity (i.e., $Q_p$) of the notch filter, more effective was the issue of isolating the artifact signals close to the null frequency. In such a case the magnitude and phase of the artifact signals close to the null frequency remain almost the same as the magnitude and phase of the signals further away from the null frequency. According to the numerical analysis via MATLAB, for high $Q_p$ the phase angle of the signals at the notch filter output remains close to zero over wider frequency spans on either side of the null frequency. Similarly, the magnitude remains close to unity (i.e., zero loss) over wider frequency spans on either side of the null frequency with higher values of $Q_p$. Thus, a high $Q_p$ (i.e., greater than or equal to 10) of the notch filter has been adopted for the artifact recovery subsystem in the proposed system.

Investigating the aspect of passage of the artifact signals, with no change of magnitude and phase through a notch filter tuned to the intended band of signals, is a new contribution in this thesis.

- Since our near-term goal was to develop an integrated circuit module for the proposed system, we paid attention to implementation of several standard amplifiers such as: Operational Amplifier, Difference Amplifier and so on. This work has been reported in Chapter 3 of the thesis. We adopted an operational amplifier circuit reported in the literature [17] and used the 180 nm CMOS technological process available in the VLSI research laboratory for implementing several amplifiers. We have implemented circuit resistances in the range of kilo ohms to tens of giga ohms using the same 180nm CMOS process.
- In some cases, the artifact signals could become too high, which would cause the various amplifiers in the system to become overloaded and saturated. To combat this, we introduced companding (i.e., compressing and expanding) in our adaptive filter. The compressor reduces the high-level artifact signals from overloading the amplifiers, while the expander restores the original levels of the artifact signals. The output of the expander constituted the band of reference signals (i.e., recovered artifact signals) to be subtracted from the original mixture of the intended plus the artifact signals. Introduction of companding in adaptive filter system is a new contribution.
- In order to validate the performance of the proposed filtering system in recovering the $\delta$ and $\alpha$ waves of an EEG signal corrupted by artifacts, two sine waves of 0.5Hz and 10Hz with amplitudes of ($20\mu V$) and ($35\mu V$), respectively, simulating these two waves are used and corrupted by two types of artifacts. In

the first case, two sinusoidal signals one of 3Hz with an amplitude of $75\mu V$ and the other of 5Hz with an amplitude of $100\mu V$ were combined to produce an arbitrary wave to be used as the artifact signal. In the second case, an arbitrary signal mimicking an ECG waveform was-created empirically to be used as the artifact signal. Through these two experiments, it has been shown that the proposed feedback system can successfully suppress the artifacts and recover the two desired waves ($\delta$ and $\alpha$ waves) of an EEG signal corrupted by artifact signals.

- Finally, it is to be noted that, even though the feedback system proposed had been validated for recovering only the $\delta$ and $\alpha$ waves of an EEG corrupted by artifacts, it can easily be extended to recover all the four waves of such an EEG signal.

**6.2: Possible Future Work**

(i) For the system proposed in the thesis we have used a second order notch filter. Since the notch filter must be strong enough to eliminate the intended signals by a large amount, higher order notch filters should be used in future configurations.

(ii) The next step will be to produce the physical layout of the components of the filtering system using a standard CMOS technological process.

(iii) The layout must be subjected to further simulations and validations to ensure reliable operations under variable environmental conditions.

(iv) The post layout data must be processed for fabrication in a foundry such as Canadian Microelectronics Corporation.

(v) The fabricated chips need be tested for correct operations (verifications).

(vi) The technology could be transferred to an interested industrial partner for further development and commercialization.

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# Appendices

**A.1. MATLAB codes used to simulate the magnitude response of the notch filter at different values of $Q_P$**

```
clc
close all;
i=sqrt(-1);
wn=2*pi*60;                    % Notch frequency
w=(0:0.2*wn/100:1000)/wn;
x=(wn*w)/wn;
num1=(1-x.^2);
den1=(1+(2*i*x)-(x.^2));
y1=num1./den1;
y1i=abs(y1);
plot(w,y1i)
hold on
num2=(1-x.^2);
den2=(1+(0.5*i*x)-(x.^2));
y2=num2./den2;
y2i=abs(y2);
plot(w,y2i)
hold on
num3=(1-x.^2);
den3=(1+(0.1*i*x)-(x.^2));
y3=num3./den3;
y3i=abs(y3);
```

```
plot(w,y3i)
hold on
num4=(1-x.^2);
den4=(1+(0.05*i*x)-(x.^2));
y4=num4./den4;
y4i=abs(y4);
plot(w,y4i)
axis ([0 2.5 0 1])
xlabel('frequency,rad/s');
ylabel('magnitude,V');
legend('Qp=0.5','Qp=2','Qp=10','Qp=20')
grid on
```

**A.2. MATLAB codes used to simulate the phase response of the notch filter at different values of $Q_P$**

```
clc
close all;
i=sqrt(-1);
wn=2*pi*60;              % notch frequency
w=(0:0.2*wn/100:1000)/wn;
x=((wn*w)/wn);
num1=(1-x.^2);
den1=(1+(2*i*x)-(x.^2));
y1=num1./den1;
y1i=abs(y1);
phaseangle=angle(y1);
```

```
phaseangle1=radtodeg(phaseangle);
plot(w,phaseangle1)
hold on
num2=(1-x.^2);
den2=(1+(0.5*i*x)-(x.^2));
y2=num2./den2;
y2i=abs(y2);
phaseangle=angle(y2);
phaseangle2=radtodeg(phaseangle);
%axis ([0 10 10^(-6) 10^(0)])
xlswrite('QPm=2.xlsx',[w(:),y2i(:)]);
plot(w,phaseangle2)
hold on
num3=(1-x.^2);
den3=(1+(0.1*i*x)-(x.^2));
y3=num3./den3;
y3i=abs(y3);
phaseangle=angle(y3);
phaseangle3=radtodeg(phaseangle);
plot(w,phaseangle3)
hold on
num4=(1-x.^2);
den4=(1+(0.05*i*x)-(x.^2));
y4=num4./den4;
y4i=abs(y4);
```

```
phaseangle=angle(y4);
phaseangle4=radtodeg(phaseangle);
axis ([0 2.5 -100 100])
plot(w,phaseangle4)
legend('Qp=0.5','Qp=2','Qp=10','Qp=20')
xlabel('frequency,rad/s')
ylabel('angle,deg')
grid on
```

### A.3. MATLAB codes used to simulate the pure EEG and contaminated EEG data

```
clc;
close all;
[d,s] = xlsread('Data.xlsx');
t = d(:,1);
v = d(:,2);
N=length(v);
L = length(t);
Ts = mean(diff(t));          % Sampling Interval (sec)
Fs = 1/Ts;                   % Sampling Frequency
Fn = Fs/2;                   % Nyquist Frequency
vc = v - mean(v);            % Subtract Mean (‘0 Hz’) Component
FTv = fft(vc)/L;             % Fourier Transform
bin_values = [0 : N-1];
fax_Hz = bin_values*Fs/N;    % Frequency Vector (Hz)
N_2 = ceil(N/25);            % Index Vector
mag=abs(FTv)*2;
```

```
semilogx(fax_Hz(1:N_2),mag(1:N_2))

ylabel('Amplitude(V)')

xlabel('Frequency(Hz)')

grid on
```

### A.4. MATLAB codes used in characterisation of pseudo resistors

```
clc;
close all;

%W=20 microns

[d,s] = xlsread('Data1.xlsx');

ar1 = d(:,1);

res1 = d(:,2);

plot(res1,ar1)

hold on

%w=40 microns

[d2,s2] = xlsread('Data2.xlsx');

ar2 = d2(:,1);

res2 = d2(:,2);

plot(res2,ar2)

hold on

%w=80 microns

[d3,s3] = xlsread('Data3.xlsx');

ar3 = d3(:,1);

res3 = d3(:,2);

plot(res3,ar3)

hold on
```

```
%w=100 microns
[d4,s4] = xlsread('Data4.xlsx');
ar4 = d4(:,1);
res4 = d4(:,2);
plot(res4,ar4)
xlabel('Resistance(ohms)')
ylabel('W/L')
legend('Width(W)=20 microns','Width(W)=40 microns','Width(W)=80
microns','Width(W)=100 microns')
grid on
```

**A.5. Path address for operational amplifier design**

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/OP_AMP/schematic/sch. cdb

**A.6. Path address for CMOS summing amplifier design**

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/SUMMER_CICUIT/schematic/sch. cdb

**A.7. Path address for pseudo resistor configuration**

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/pseudo_res/schematic/sch. cdb

**A.8. Path address for compressor circuit design**

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/COMPRESSOR_SUBCIRC/schematic/sch. cdb

**A.9. Path address for expander circuit design**

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/EXPANDER_SUBCIRC/schematic/sch. cdb

**A.10. Path address for notch filter design with null frequency of 0.5Hz**

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/NOTCH_FILTER_0.5Hz/schematic/sch. cdb

### A.11. Path address for notch filter design with null frequency of 10Hz

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/Notch_10hz_SUB/schematic/sch. cdb

### A.12. Path address for unity gain difference amplifier design

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/D_AMPLIF_SUB/schematic/sch. cdb

### A.13. Path address for the proposed filtering system

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/notch_design/schematic/sch. cdb

### A.14. Path address for arbitrary signal (ECG signal) generation

/nfs/home/k/k_samoa/CMOSP18/test_cmosp18/Artefact_Genera/schematic/sch. cdb