Multi-mode tri-state operation of a 4-switch bidirectional DC-DC converter for interfacing a supercapacitor to a DC grid

Qiong Wang

A Thesis

In the Department

Of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

For the Degree of Master of Science (Electrical and Computer Engineering) at

Concordia University

Montreal, Quebec, Canada

November 2022

CONCORDIA UNIVERSITY

School of Graduate Studies

This is to certify that the thesis prepared

By: **Qiong Wang**

Entitled: **Multi-mode tri-state operation of a 4-switch bidirectional DC-DC converter for interfacing a supercapacitor to a DC grid**

and submitted in partial fulfillment of the requirements for the degree of

Master of Applied Science (Electrical and Computer Engineering)

complies with the regulations of the University and meets the accepted standards with respect to originality and quality.

Signed by the final examining committee:

_____ Chair

Dr. Chunyan Lai

_____ External Examiner

Dr. Truong Nguyen

_____ Examiner

Dr. Chunyan Lai

_____ Thesis Supervisor

Dr. Luiz Antonio C. Lopes

Approved by:_____

Dr. Yousef R. Shayan, Chair,

Department of Electrical and Computer Engineering

_____

Dr. Mourad Debbabi, Dean,

Gina Cody School of Engineering and Computer Science

Abstract

Multi-mode tri-state operation of a 4-switch bidirectional DC-DC converter for interfacing a supercapacitor to a DC grid

Qiong Wang

Energy storage devices such as supercapacitors and batteries are frequently used to support DC nanogrids that employ renewable resources. They make the system more stable and reliable, by contributing to power balance with high charge/discharge rates. The 2-switch class C DC-DC converter with dual-state logic is widely used as the interface for supercapacitors to a DC nano grid. It presents slow dynamic response due to the Right-Half Plane (RHP) zero in the transfer function of V_o/D in Boost mode, when supercapacitors supply power to the DC grid. This converter also faces an issue of losing current control when the voltage of the supercapacitor is higher than that of the DC nanogrid. A 4-switch bidirectional DC-DC converter in the Buck-Boost mode that consists of two half-bridges and an intermediate inductor can be used as the interface. By using tri-state logic with fixed D_{off} , it can eliminate the RHP zero in the transfer function I_o/ D_{on} and control the current flow all the time. However, the voltage gain of the output voltage over the supercapacitor's voltage decreases because of the fixed D_{off}, which is an issue when the converter only operates in one mode and the supercapacitor voltage changes between half voltage (24 V) to rated voltage (48 V). Thus, the mode must be changed between Boost and Buck-Boost modes as the voltage in the supercapacitor varies.

The tri-state logic can present different sequences with the three states D_{on}, D_{off}, and D_{fw}. Thus the traditional pulse width modulation (PWM) technique using one modulating signal D_{on} cannot be used in the tri-state logic. This thesis proposes a flexible space vector modulation scheme, which concerns the modes of operation, the sequences of the tri-states, and the state of each switch. A smooth mode transition logic is presented to reduce the output current variation when the mode changes between the Boost and Buck-Boost modes. The main goal of this work is to regulate the output current at a set value, while the converter changes between the Boost and Buck-Boost modes as a function of the voltage gain (V_o/V_{in}) with the input voltage varying in a wide range. The analysis of the system and design of controllers are presented and verified. Simulation results

with the proposed modulation scheme and smooth mode transition logic, as well as experimental implementation, are presented and discussed.

ACKNOWLEDGEMENT

First, I would like to express my deep gratitude to Professor Luiz A. C. Lopes, his passion for research and positive attitude inspires me a lot, with his kind support, valuable instructions, professional guidance, and patience, I have this wonderful research journey.

Then, I would like to express my gratitude to my committee members, for their time and guidance through the review of the thesis. I would also like to thank my colleagues in the Power Electronics and Energy Research (PEER) group of Concordia University, your encouragement and support help me achieve my goals, special thanks to Gabriel Renan Broday, Yupeng Liu, Jingdi Wang, Ying Zuo, Neetusha Kalarikkal, Koteswara Rao Alla and Tamanwe Payarou who were always willing to help and share their valuable experiences.

Finally, I want to express my deepest appreciation and love to my husband and my parents, for their unconditional support, endless love, and heartful encouragement.

Table of Contents

List of Figures

List of Tables

Nomenclature

PV: Photovoltaics

SC: Supercapacitor

HESS: Hybrid Energy Storage System

ESS : Energy Storage System

DC: Direct Current

RHP : Right-Half Plane

D : Duty Cycle

PWM : Pulse Width Modulation

FW : Free-wheeling

RMS: Root mean square

ESR: Equivalent Series Resistance

PI: Proportional-integral.

PM: Phase Margin

LTF: Loop transfer function

MUX: Multiplexer

DSP: Digital Signal Processor

ADC: Analog-to-Digital Converter

GPIO: General Purpose Input/Output

CPU: Central Processing Unit

Chapter 1 Introduction

With today's increasing energy demand and depletion of non-renewable resources, renewable ones such as photovoltaics (PV), wind energy and fuel cells are increasingly considered and used in grid systems. Especially in some DC nano-grids, which are very efficient for residential power supply and small buildings. However, due to their fluctuating characteristics, these renewable resources cannot support the DC grid very reliably and stably. So, some energy storage devices, such as supercapacitors (SC) and batteries, connected to the grid through power electronic converters can be used for power balancing and voltage regulation by supplying rapidly changing currents [1]-[4]. A hybrid energy storage system (HESS) contains batteries and supercapacitors. One typical application of HESS is that a battery and a SC are connected to the DC grid through electronic converters, to support varying power demand caused by the changes in PV generation and loads [5][6]. The battery presents high energy density but low power density, while the SC provides high power density low energy density, giving high charge/discharge rates. In this thesis, the aim is to use a SC as an energy storage system (ESS) to support a 48 V DC bus in a DC nano-grid, with the voltage of the SC changing between half rated and rated voltage (48 V), to supply and absorb fast changing currents. This project could be applied in DC microgrids, small electric vehicles, and aircraft, and can be used to provide high voltage gain for SCs in a HESS.

The 2-switch class C DC-DC converter with dual-state (D_{on} and D_{off}) logic is frequently used as the interface for the supercapacitor in DC grids, with the SC placed at the low voltage side [5][7]. One issue is that during the transient response, the actual output power flow will change in the wrong direction following a variation in the reference value due to a presence of a Right-Half Plane (RHP) zero in the transfer function of the output voltage (V_o) with respect to the duty cycle (D) in Boost mode, with power flowing from the SC to the DC bus. This can be solved by using cascaded control loops with an inner current control loop and an outer voltage control loop. This compromises the dynamic response speed, since the bandwidth of the outer voltage control loop has to be about 20 % of the bandwidth of the inner current loop. The tri-state control (D_{on} and D_{off} and D_{fw}) logic can eliminate the RHP zero by including a free-wheeling segment/period (D_{fw}) of the inductor current. However, this requires an additional switch and diode for the converter and a multivariable (D_{on} and D_{off} or D_{fw}) modulation/control scheme [8]. In addition to the slow dynamic response, the 2-switch class C converter will lose the control of power flow when the voltage of

the DC grid drops below the voltage of the SC, with the conduction of the anti-parallel diodes of the converter. A 4-switch bidirectional Buck-Boost converter with two half-bridges and an intermediate inductor can solve this issue and can control the power flow with the SC voltage either higher or lower than the DC grid voltage [9].

The 4-switch bidirectional DC-DC converter can operate in Boost, Buck-Boost and Buck modes, but with conventional dual-state control in the Boost and Buck-Boost modes, the transfer function of the output current (I_o) or output voltage (V_o) with the duty cycle (D) also presents an RHP zero which slows down the dynamic response. The tri-state control logic used in a modified unidirectional Boost converter is extended for the 4-switch bidirectional DC-DC converter [10]. Unlike in the 2-switch converter, the 4-switch converter already includes all required switches/diodes for tri-state operation. The tri-state contains ON, OFF and free-wheeling (FW) states, and concerns a multivariable control problem with two variables of the three, usually the ON and OFF duty cycles, as control variables. But the control of the two state variables would lead to the appearance of cross-coupling transfer functions [11], what complicates the design of linear controllers. One method to avoid the cross-coupling transfer functions is to keep one of the durations of the three states constant, usually D_{off} [10]. In this case, the small-signal model employed to design the controllers becomes simple when the system is treated as single-variable.

The DC nano-grid typically consists of several energy resources interfaced through DC-DC converters to the DC bus. These are controlled either in a current limit mode or in a droop control mode [12] and can be modeled as a voltage source in series with an equivalent feeder resistance [10]. In this thesis, a supercapacitor is connected to a DC nano-grid, through a 4-switch bidirectional DC-DC converter operating with tri-state control logic with fixed D_{off}. The converter can inject power into the DC grid or draw power, charging the supercapacitor.

1.1 Problem statement and proposed solution

When a supercapacitor is used to provide fast varying positive and negative (output) currents for a DC nano-grid, a 4-switch bidirectional DC-DC converter can be used as the interface. The basic circuit scheme of 4-switch bidirectional DC-DC converter interfacing the SC to a DC nano-grid is shown in Figure 1-1. The DC nano-grid is modeled as a 48 V (V_{dc}) and a feeder impedance (R_f). The converter operates in tri-state control logic with an appropriate fixed value of D_{off} to

eliminate the RHP zero of the transfer function of output current I_o with respect to the duty cycle D_{on}. This provides a fast dynamic response compared with the conventional dual-state control logic, only using a single duty cycle control.

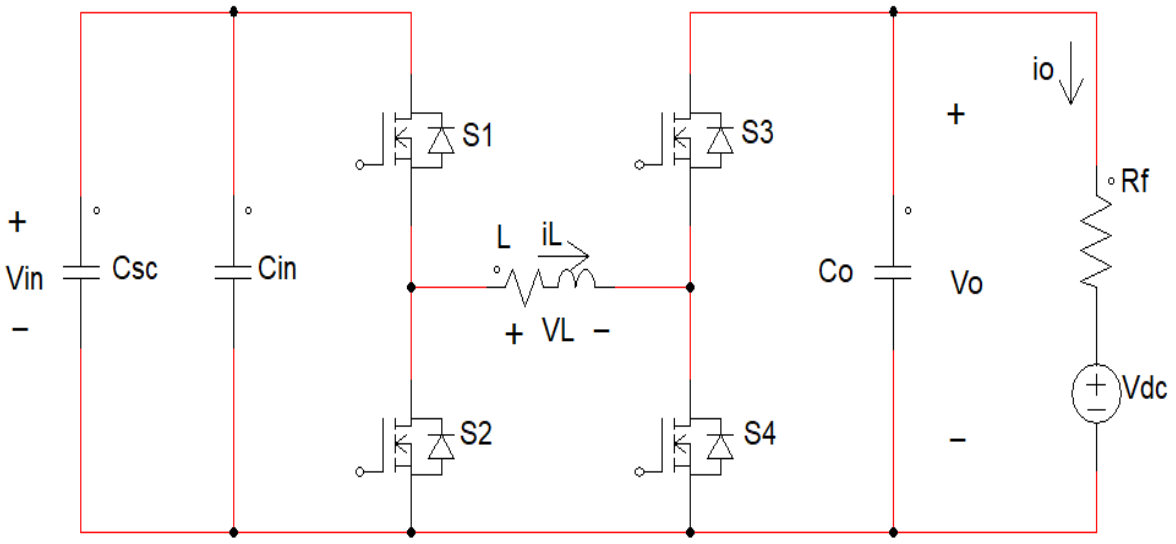

Figure 1- 1 4-switch bidirectional DC-DC converter connecting a SC to a DC nano-grid

The tri-state scheme, with ON, OFF, and free-wheeling states, can have several sequences**.** With different sequences of the tri-state D_{on}, D_{off} , and D_{fw} in one switching period, one cannot use the conventional pulse width modulation (PWM) logic, with only one modulating signal D_{on}, to get the gating signals for different modes of operation. A space vector type modulation scheme is developed to solve this problem and it can work in both analog and digital control. The space vector modulation scheme concerns the modes of operation, the sequences of the tri-states, to generate the gating signals sent to the switches. This modulation scheme is relatively flexible, and it should be able to extend to operate with quad-state logic [13]. However, in such a case, generating the gating signals of the switches with three modulating signals while realizing a specific sequence of states becomes more complicated.

In this thesis, the voltage of the SC (V_{in}) is usually lower or slightly higher than the voltage at the output of the power interface (V_o), thus the converter can operate in Boost and Buck-Boost modes. In principle, operation in the Buck-Boost mode should suffice, but with the fixed value of

D_{off}, the allowed voltage gain (V_o/V_{in}) is reduced. This becomes a serious constraint since the voltage of the SC should be allowed to vary in a wide range for maximizing the amount of energy that it can supply/absorb following a given DC grid power variation. Thus, a smooth mode transition logic for transitioning to and from the Boost mode should be included in the tri-state logic with a fixed D_{off}, to minimize the variations of the current when modes change. Besides, with negative/positive output current references, the voltage of SC increases/decreases, thus a protection logic is also considered to protect the SC, avoiding over-charging or over-discharging.

For the digital control, several digital control design approaches for switch mode power converter are presented and compared in [14]. The most recommended, the direct digital approach, can provide wide bandwidth while keeping the system stable and even performing better with a low sampling frequency. An issue caused by the RHP zero in the transfer function in the w-domain, limits the selection of the crossover frequency [15]. However, with a low sampling frequency chosen in this project to design a digital controller, the direct digital approach is used.

1.2 Scope and contribution of thesis

This thesis focuses on the design of the control loop for the 4-switch bidirectional DC-DC converter operating with tri-state logic interfacing a SC to the DC grid, implementing a space vector modulation scheme and mode transition logic for a wide input voltage range.

The main contributions of this thesis are as follows.

1) Design of the controllers for the current control loop to regulate the output current injecting or drawing from the DC grid to a SC.

2) Design and implement a space vector modulation scheme for the converter operating with tri-state control logic.

3) Design and test a dynamic transition logic between modes of operation to ensure the converting operating in a wide input range with small transition variations in the output current.

4) Validate the performance of the system with simulation and experimental tests.

1.3 Thesis outline

The structure of this thesis is as follows.

Chapter 2 discusses the implementation of the 4-switch bidirectional DC-DC converter with tri-state logic with duty cycle control interfacing a supercapacitor to a DC grid. It also presents the state-space averaging method to derive the transfer functions of the converter and simulation results by using space vector modulation scheme.

Chapter 3 discusses the problem of limited voltage gains due to a constant value of D_{off} for the converter operating in both Boost and Buck-Boost modes and presents and validates the solution by using smooth mode transition logic. It shows the final/complete simulation results of the converter operating in analog control and digital control.

Chapter 4 presents the experimental implementation and several test cases to validate the simulation results.

Chapter 5 presents the conclusion and suggestions for future research.

Chapter 2 Bidirectional 4-Switch DC-DC converter operating with tri-state logic

A 4-switch bidirectional DC-DC converter can be used to interface two storage devices such as supercapacitors and batteries or connect an energy storage device to a DC grid. In this project, the bidirectional converter is used for interfacing a supercapacitor (SC) to a DC grid rated at 48 V. The supercapacitor can provide or absorb power from the DC grid, and the goal of this project is to regulate the value of the output current injected to, or drawn from, the DC grid, under varying conditions. It is assumed that the voltage of the SC (V_{in}) remains between half and the rated voltage (48 V). In this chapter, the 4-switch bidirectional DC-DC converter operating with the tri-state logic is presented and compared to another operating with conventional dual-state control.

2.1 Circuit scheme with a bidirectional 4-switch DC-DC converter

The tri-state logic employed for the modified uni-directional Boost converter with an additional switch and diode [8] can be extended and used for this 4-switch bidirectional DC-DC converter [10]. An additional state free-wheeling D_{fw} is added to the dual-state D_{on} and D_{off} (the duty cycles meet the one switching period equation $D_{on} + D_{off} + D_{fw} = 1$), this tri-state modulation scheme can eliminate the RHP zero. However, the system becomes multi-variable, one can control two states of the three, usually the D_{on} and D_{off} duty cycles. The free-wheeling D_{fw} can be derived from the one switching period equation, but this method leads to the appearance of cross-coupling transfer functions [11] what complicates the design of linear controllers. One method is to keep one of the durations of the three states constant, usually D_{off} [10], thus the system can be treated as single-variable system, and the small-signal model employed to design the controllers becomes simple compared to the multi-variables system. Other methods can employ a dual-mode control scheme with parallel [16] or cascaded [17] control loops. In this project, the tri-state logic with fixed D_{off} is used. With the D_{off} fixed, one can control the output current, absorb, or supply, only with a standard single duty cycle control, D_{on}.

The 4-switch bidirectional DC-DC converter used in this project is shown in Figure 2-1. It contains two half-bridges and an intermediate inductor, connecting the SC (V_{in}) to the DC grid (V_{dc}) through a feeder impedance (R_f). The value of V_{dc} is 48 V, the value of the feeder impedance

R_f is 0.2 Ω, which represents the wire resistance. In this project, the output current is expected to be adjustable between -5 A and 5 A.

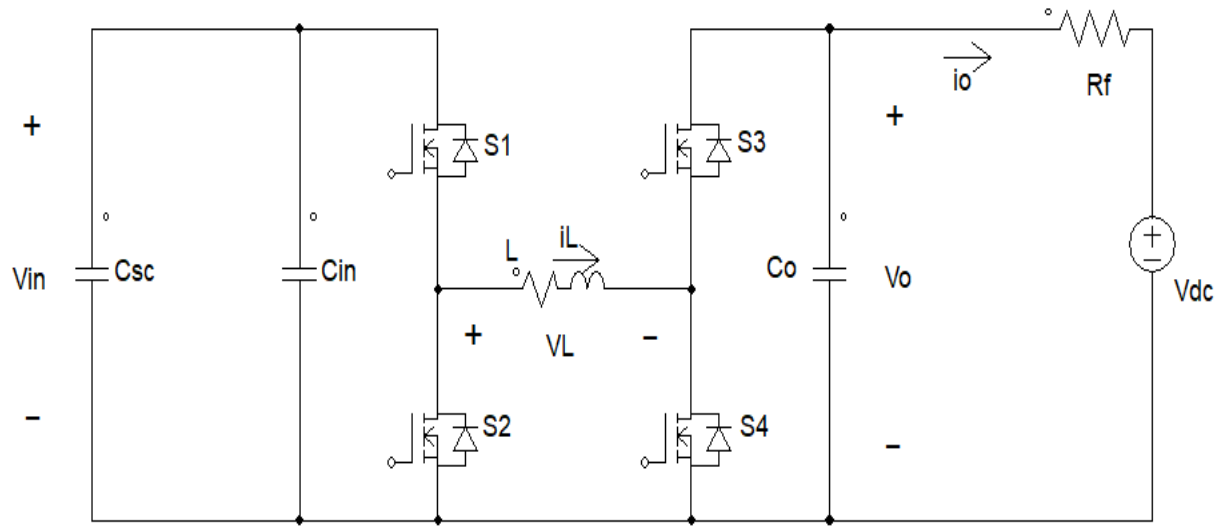

Figure 2- 1 The 4-switch bidirectional DC-DC converter connected to a DC bus

The switches in a half-bridge operate complementarily, so the four switches (S1, S2, S3 and S4) can present four possible "states" of operation with S1S3, S1S4, S2S3 and S2S4 ON. Four anti-parallel diodes, body diodes of MOSFETs, are modeled, what is essential for the converter to operate with bidirectional power flow. When the SC injects power into the DC grid ($V_o > V_{dc}$), the output current I_o is defined as positive as shown in the Figure 2-1, otherwise, the output current is defined as negative. The direction of the power flow determines whether $I_L >$ or < 0.

The four possible "states" of operation correspond to D_{on}, D_{offB} (OFF state in Boost mode), D_{offBB} (OFF state in Buck-Boost mode), and D_{fw}, respectively, and current paths in the four possible "states" of operation are presented in Figure 2-2 for $I_o > 0$, $I_L > 0$ and in Figure 2-3 for $I_o < 0$, $I_L < 0$. There one can see the conducting switches or diodes (D1, D2, D3 and D4).

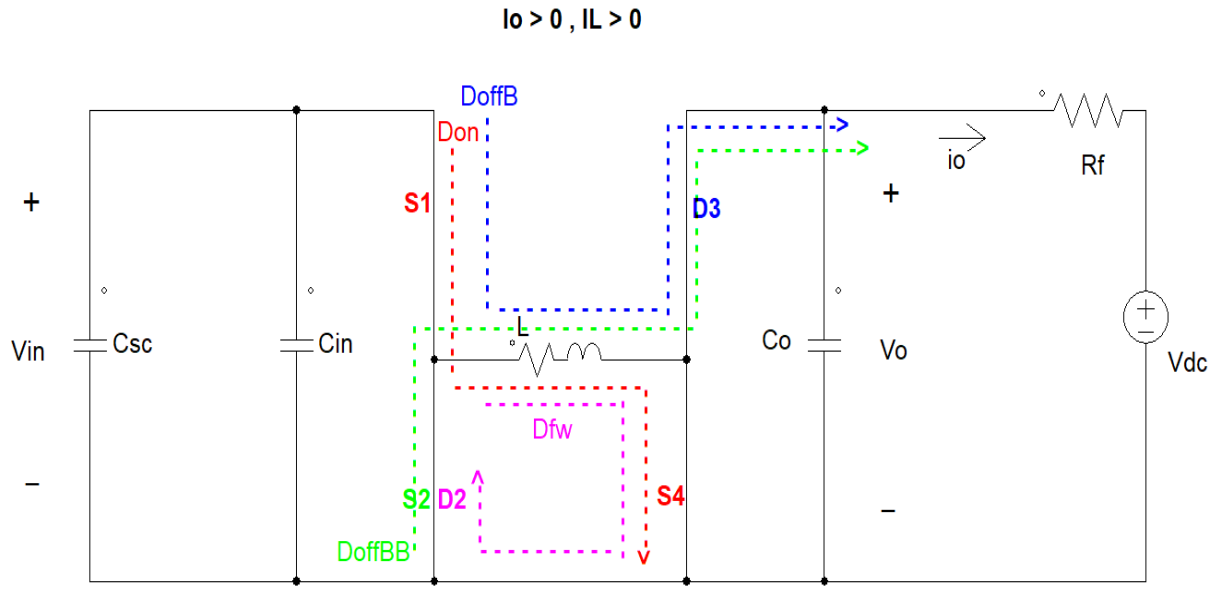

Figure 2- 2 The current paths in the four possible states for Io > 0, IL > 0 (Don in red color, DoffB in blue color, DoffBB in green color, Dfw in pink color)

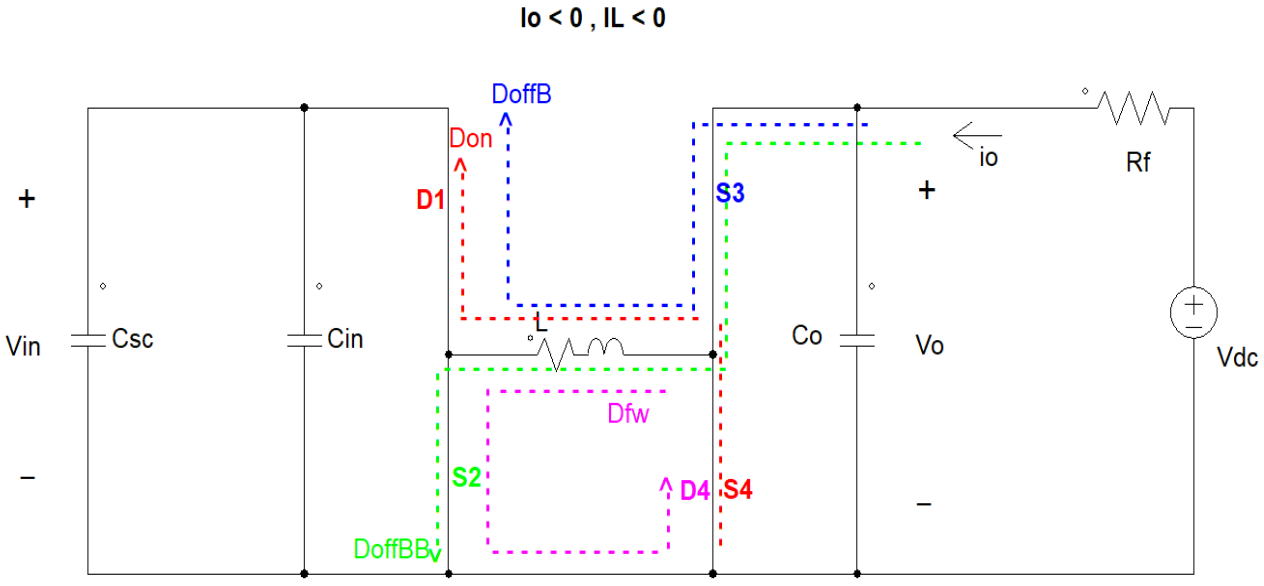

Figure 2- 3 The current paths in the four possible states with Io < 0 , IL < 0 (Don in red color, DoffB in blue color, DoffBB in green color, Dfw in pink color)

2.2 Tri-state operation with fixed Doff

The mode of operation of the 4-switch bidirectional converter with tri-state logic can be Boost, Buck-Boost and Buck modes. Since in the application considered in this project, the voltage of the SC (V_{in}) is changing between half-rated voltage to the rated voltage 48 V, which is lower or slightly higher than the output of the power interface (V_o), operation in the Boost and Buck-Boost mode is enough for all cases.

2.2.1 The selection of the value of fixed Doff

For tri-state logic, it is essential to make sure that the converter always operates with tri-state logic in steady-state. Since D_{off} is fixed at a constant value, a transient increase in D_{on} to increase the magnitude of I_L and I_o, requires a corresponding transient decrease in D_{fw}. Thus, a minimum value of D_{fw} (D_{fw_min}) in steady-state needs to be set, to provide a dynamic range of D_{on} for increasing I_L and I_o without saturating the controller. Likewise, a minimum value of D_{on} (D_{on_min}) is needed for decreasing the magnitude of I_L and I_o without saturating the controller and make sure the three states are used. In this project, the minimum values of D_{fw} and D_{on} are both set as 0.1. Then, the duration of the OFF duty cycle must be fixed at less than 0.8. A higher value of the fixed D_{off} reduces the intermediate inductor current (I_L) for a given output current (I_o) according to equation (2-1) and thus leads to higher efficiency and small size of the inductor. Conversely, a smaller D_{off} with D_{fw_min} can increase the transient of D_{on} (D_{on_max} = 1 - D_{off} - D_{fw_min}) and thus increase the voltage gain and have fast transient response. Therefore, by choosing an appropriate value for D_{off} to balance the efficiency and the transient response speed, is important. A procedure for computing a suitable D_{off} was presented in [19].

The equation of the average values of the inductor current I_L, output current I_o and D_{off} of the converter operating with tri-state logic is given by [10]

$$I_L = \frac{I_o}{D_{off}} \tag{2-1}$$

2.2.1.1 Selecting a suitable Doff in Boost mode of operation

The converter in this project interfaces a SC to the DC bus rated at 48 V. The SC operates with voltages between 24 V to 48 V. Considering a +/- 10% margin of the output voltage based on the rated DC bus voltage, the minimum output voltage is $0.9V_o$ (43.2 V) and the maximum output

voltage is $1.1V_o$ (52.8 V). Then the worst case in Boost mode, in terms of voltage gain, is using a SC voltage of 24 V and a DC grid voltage of 52.8 V. The gain equation derived considering that the average voltage in the inductor in steady-state is 0 V, is given by

$$Gain_{max} = \frac{V_{o\_max}}{V_{in\_min}} = \frac{D_{on}+D_{off}}{D_{off}} = \frac{1-D_{fw\_min}}{D_{off}} \quad (2\text{-}2)$$

With $D_{fw\_min} = 0.1$, $D_{off} \approx 0.4$ for operating in Boost mode, and the maximum input voltage for Boost mode is given by

$$V_{in\_max} = \frac{V_{o\_min}}{Gain_{min}} = V_o/(1 + \frac{D_{on\_min}}{D_{off}}) \quad (2\text{-}3)$$

When D_{off} is 0.4, the maximum input voltage is 0.8 V_o. For Boost mode of operation, assuming that V_o is at its minimum value, which is 43.2 V, with $D_{on\_min} = 0.1$ and $D_{off} = 0.4$. Therefore, for 24 V< V_{in} < 34.56 V and 43.2 V< V_o < 52.8 V, one can operate in the Boost mode with $D_{off} = 0.4$ and $D_{on\_min} = D_{fw\_min} = 0.1$. However, one would have to change to the Buck-Boost mode when V_{in} exceeds 34.56 V.

2.2.1.2 Selecting a suitable D_{off} in Buck-Boost mode of operation

In Buck-Boost mode of operation, the equation of the maximum voltage gain is by

$$Gain_{max} = \frac{V_{omax}}{V_{inmin}} = \frac{D_{on\_max}}{D_{off}} \quad (2\text{-}4)$$

Considering the worst case using a SC voltage of 24 V and a DC grid voltage of 52.8 V, after calculation, $D_{off} \approx 0.28$, and the minimum input voltage for the Buck-Boost mode is given by

$$V_{in\_min} = \frac{V_{o\_max}}{Gain_{max}} = V_o/(\frac{D_{on\_max}}{D_{off}}) \quad (2\text{-}5)$$

Therefore, for 24 V< V_{in} < 48 V and 43.2 V< V_o < 52.8 V, one can operate in the Buck-Boost mode with $D_{off} = 0.28$ and $D_{fw\_min} = 0.1$. However, using a relatively small value of D_{off} (0.28) and an output current of 5 A, requires the inductor current to be large as 17.85 A according to equation (2-1) and low efficiency, thus the value of D_{off} would be chosen higher than 0.28. Because of the limited input voltage range in Boost mode or Buck-Boost mode, in this project, the converter

operates in both Boost and Buck-Boost modes interfacing the SC to the DC grid, and the modes must change since the SC voltage varies between 24 V to 48 V. The overlap voltage range between Boost mode and Buck-Boost mode is given by

$$(V_{in_{maxBoost}} - V_{in_{minBuckBoost}})$$

Considering the operation of Boost and Buck-Boost modes, one can select a D_{off} value from the range of 0.28 to 0.4. In this project, D_{off} is fixed at 0.35 to have a large enough overlap voltage range between Boost and Buck-Boost modes which could give more safety space for mode transitions. The resulting overlap voltage range for D_{off} 0.35 is shown below.

$$V_{in_{maxBoost}} - V_{in_{minBuckBoost}} = \frac{V_o}{1+\frac{D_{on\_min}}{D_{off}}} - \frac{V_o}{\frac{D_{on\_max}}{D_{off}}} \approx 0.141V_o \qquad (2\text{-}6)$$

The value of the control variable should be $D_{on\_min} < D_{on} < 1 - D_{off} - D_{fw\_min}$ which is $0.1 < D_{on} < 0.55$.

2.2.2 Switching scheme for the Boost mode

The 4-switch bidirectional converter operates in Boost mode when the SC voltage (V_{in}) is *much* lower than the output voltage. One can see the current flow in the converter while operating in Boost mode with respect to the three states (D_{on}, D_{off} and D_{fw}) in Figure 2-4, Figure 2-5, and Figure 2-6.

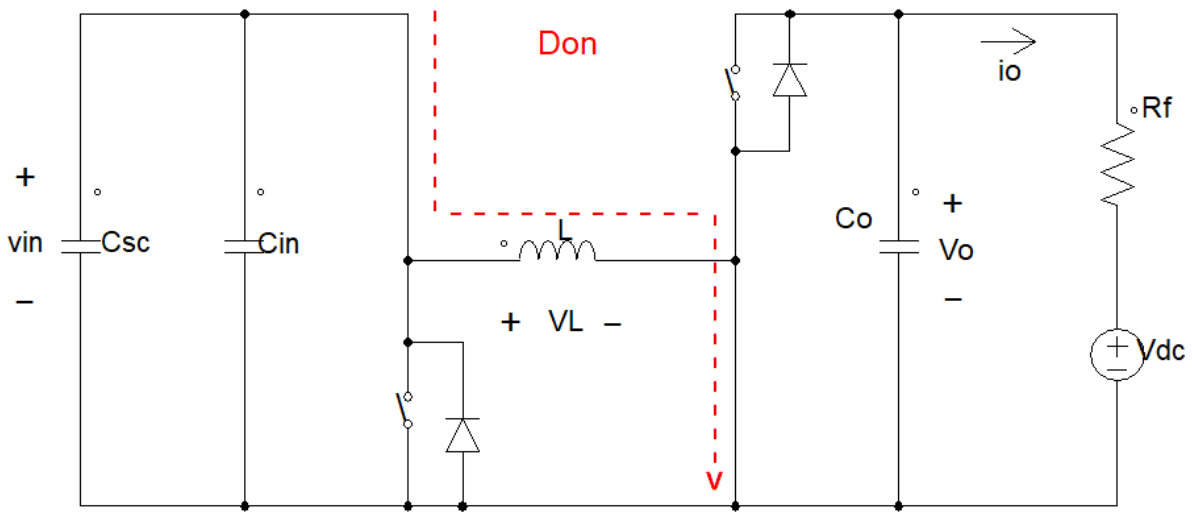

Figure 2- 4 Current flow during ON state in Boost mode with IL > 0 A

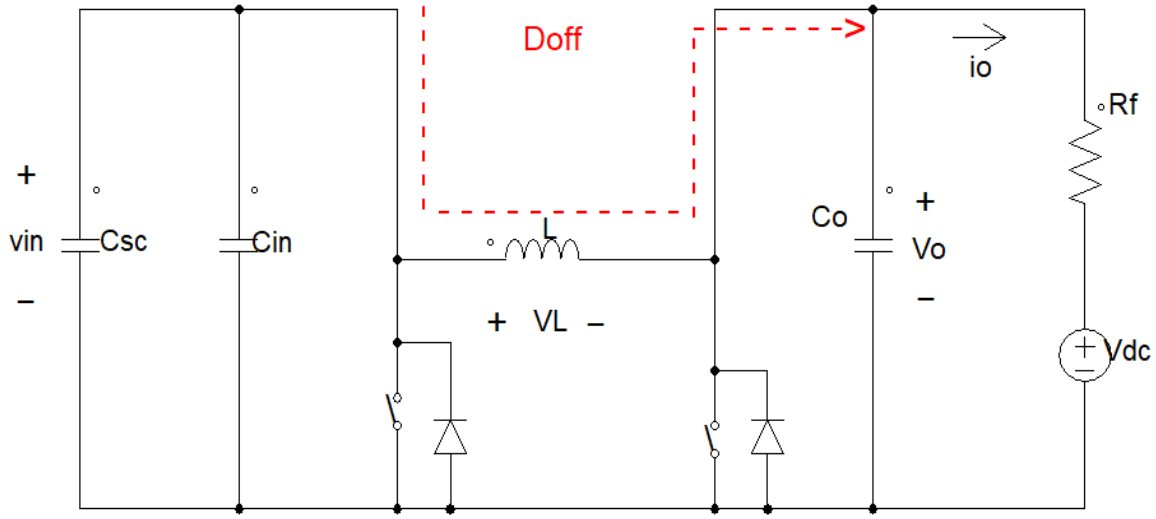

Figure 2- 5 Current flow during OFF state in Boost mode with IL > 0 A

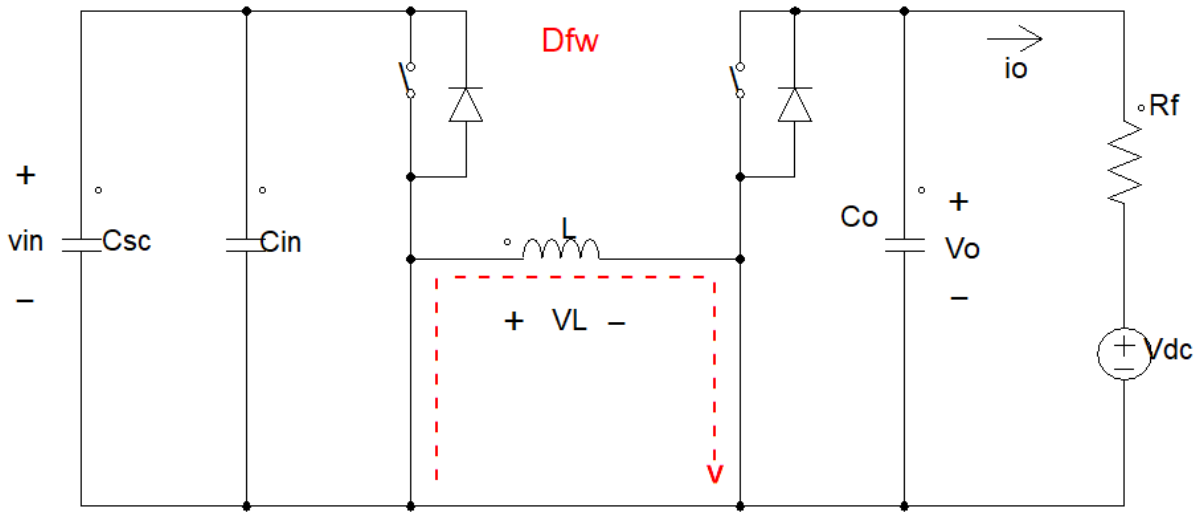

Figure 2- 6 Current flow during free-wheeling state in Boost mode with IL > 0 A

The truth table of all the switches for the three states of operation in Boost mode:

Table 2. 1 Truth table of 4-switches for Boost mode of operation

State/Switches	S1	S2	S3	S4
D_{on}	ON	OFF	OFF	ON
D_{off}	ON	OFF	ON	OFF
D_{fw}	OFF	ON	OFF	ON

In this mode of operation, the duty cycles of the various states are related by $D_{S14} + D_{S13} + D_{S24} = 1$.

The voltage gain and min/max input voltages for operation in Boost mode:

$$Gain = \frac{V_o}{V_{in}} = \frac{D_{s13}+D_{s14}}{D_{s13}} = \frac{D_{on}+D_{off}}{D_{off}} \quad (2\text{- }7)$$

$$V_{in\_min} = \frac{D_{off}\, V_{o\_max}}{D_{off}+D_{onMax}} = \frac{D_{off}\,(V_{dc}+I_{o\_max}R_f)}{1-D_{fw\_min}} \quad (2\text{- }8)$$

$$V_{in\_max} = \frac{D_{off}\, V_{o\_min}}{D_{off}+D_{on\_min}} = \frac{D_{off}\,(V_{dc}-I_{o\_max}R_f)}{D_{off}+D_{on\_min}} \quad (2\text{- }9)$$

With the parameters used in this project, D_{fw_min} = 0.1, D_{on_min} = 0.1, D_{off} = 0.35, V_{dc} = 48 V, I_{o_max} = 5 A, and the SC operating in the desired voltage range: 24 V to 48 V, the input voltage for the converter operating in Boost mode ranges from 24 V to 36.6 V. For a higher SC voltage, the converter should operate in Buck-Boost mode.

2.2.3 Switching scheme for the Buck-Boost mode

When the input voltage is lower or slightly higher than the output of the power interface (V_o), the converter operates in the Buck-Boost mode. The switching scheme only changes during the OFF state (D_{off}) compared to operating in Boost mode, which is shown in Figure 2-7. The OFF state in the Buck-Boost mode has switches S2 and S3 ON while the Off state in the Boost has S1 and S3 ON. The current flow path during the ON state (D_{on}) and the free-wheeling state (D_{fw}) are the same as shown in Figure 2-4 and 2-5 in Boost mode.

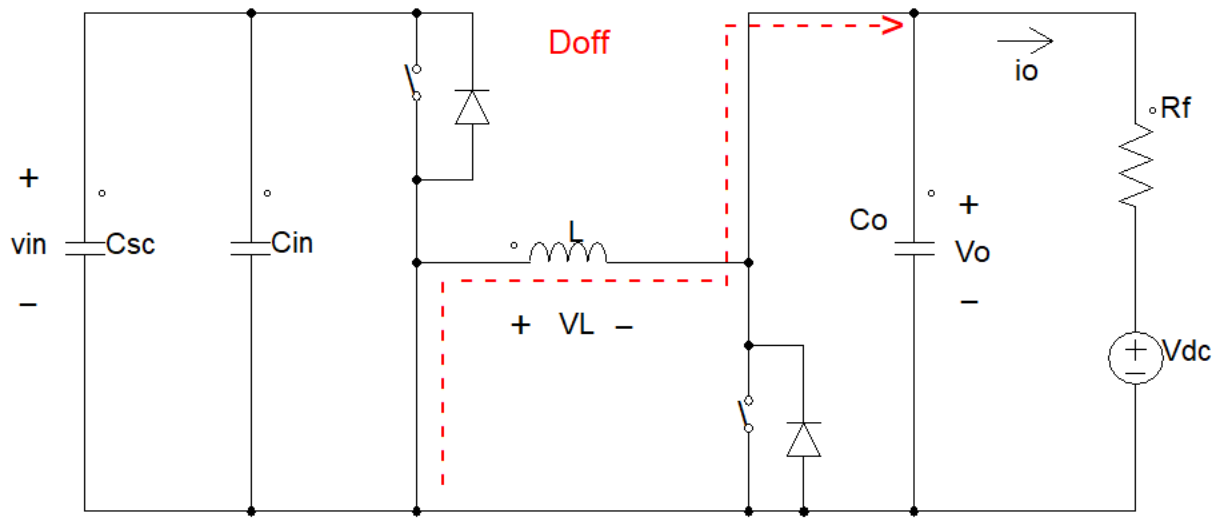

Figure 2- 7 Current flow during OFF state in Buck-Boost mode

The truth table of all the switches for the 3 states of operation in Buck-Boost mode:

Table 2. 2 Truth table of 4-switches for Buck-Boost mode of operation

State/Switches	S1	S2	S3	S4
D_{on}	ON	OFF	OFF	ON
D_{off}	OFF	ON	ON	OFF
D_{fw}	OFF	ON	OFF	ON

In this mode of operation, the duty cycles of the various states are related by $D_{S14} + D_{S23} + D_{S24} = 1$.

Table 2.3 illustrates conducting devices for $I_o > 0$ A and $I_o < 0$ A in the four possible "state" in both Boost and Buck-Boost modes.

Table 2. 3 Summary of conducting devices for Io > 0 A and Io < 0 A

State	$I_o > 0$ A	$I_o < 0$ A
D_{on}	S1S4	S4D1
D_{offB}	S1D3	S3D1
D_{offBB}	S2D3	S3S2
D_{fw}	S4D2	S2D4

The voltage gain and min/max input voltages for operation in the Buck-Boost mode:

$$Gain = \frac{V_o}{V_{in}} = \frac{D_{S14}}{D_{S23}} = \frac{D_{on}}{D_{off}} \quad (2\text{-}10)$$

$$V_{in\_min} = \frac{V_{o\_max} D_{off}}{D_{on\_max}} = \frac{D_{off}\,(V_{dc} + I_{o\_max} R_f)}{1 - D_{off} - D_{fw\_min}} \quad (2\text{-}11)$$

$$V_{in\_max} = \frac{V_{o\_min} D_{off}}{D_{on\_min}} = \frac{D_{off}\,(V_{dc} - I_{o\_max} R_f)}{D_{on\_min}} \quad (2\text{-}12)$$

With $D_{fw\_min} = 0.1$, $D_{on\_min} = 0.1$, $D_{off} = 0.35$, $V_{dc} = 48$ V, $I_{o\_max} = 5$ A, and the SC operating in the desired voltage range: 24 V to 48 V. When the converter operates in Buck-Boost mode, the range of the SC voltage is from 31.2 V to 48 V, and the overlap voltage range between Boost and Buck-Boost modes is from 31.2 V to 36.6 V.

Therefore, the voltage gains of output voltage with respect to input voltage for the converter operating in Boost and Buck-Boost can be shown in Table 2.4.

Table 2. 4 The range of voltage gain for the converter operating in Boost and Buck-Boost modes

	Boost	**Buck-Boost**	**Boost**	**Buck-Boost**
$\boldsymbol{Gain\_min}$	$\frac{D_{on\_min} + D_{off}}{D_{off}}$	$\frac{D_{on\_min}}{D_{off}}$	1.2857	0.2857
$\boldsymbol{Gain\_max}$	$\frac{D_{on\_max} + D_{off}}{D_{off}}$	$\frac{D_{on\_max}}{D_{off}}$	2.5714	1.5714

With 48 V DC nano grid, and +/- 5 A output current, the value of input voltage in Boost and Buck-Boost modes can be calculated as shown in Table 2.5.

Table 2. 5 Input voltage range of SC for the converter operating in Boost and Buck-Boost modes

	Boost	**Buck-Boost**	**Boost**	**Buck-Boost**
V_{in_min}	$\frac{D_{off}\left(V_{dc}+I_{o\_max}R_f\right)}{1-D_{fw\_min}}$	$\frac{D_{off}\left(V_{dc}+I_{o\_max}R_f\right)}{1-D_{off}-D_{fw\_min}}$	< 24 V	31.2 V
V_{in_max}	$\frac{D_{off}\left(V_{dc}-I_{o\_max}R_f\right)}{D_{on\_min}+D_{off}}$	$\frac{D_{off}\left(V_{dc}-I_{o\_max}R_f\right)}{D_{on\_min}}$	36.6 V	> 48 V

2.2.4 Possible sequences of states for Boost and Buck-Boost modes

There are two possible sequences for the three states: The sequence #1 D_{on} - D_{off} - D_{fw} and the sequence #2 D_{on} - D_{fw} - D_{off}. Assuming first that the SC voltage is lower than the output voltage($V_{in} < V_o$) and that the SC injects current to the DC grid ($I_o > 0$, $I_L > 0$). Figure 2-8 shows the theoretical waveforms of the inductor current, inductor voltage and switches ON in each state with the two sequences when the converter operates in Boost mode. Figure 2-9 shows the theoretical waveforms when the converter operates in Buck-Boost mode.

From Figure 2-8 and Figure 2-9, and it also has been shown in [10] that using sequence #1 for positive output current (I_o) and inductor current (I_L) could lead to a lower value of RMS current across inductor and the switches, thus lower power losses than using sequence #2 in both Boost and Buck-Boost modes of operation. Similarly, for negative output current (I_o) and inductor current (I_L), using sequence # 2 will lead to lower power losses than using sequence #1.

Thus, for lower power loss, depending on the direction of the output current and the values of the SC voltage (V_{in}), the 4-switch bidirectional DC-DC converter can operate in 4 possible modes: Boost mode sequence #1, Boost mode sequence #2, Buck-Boost mode sequence #1, and Buck-Boost mode sequence #2.

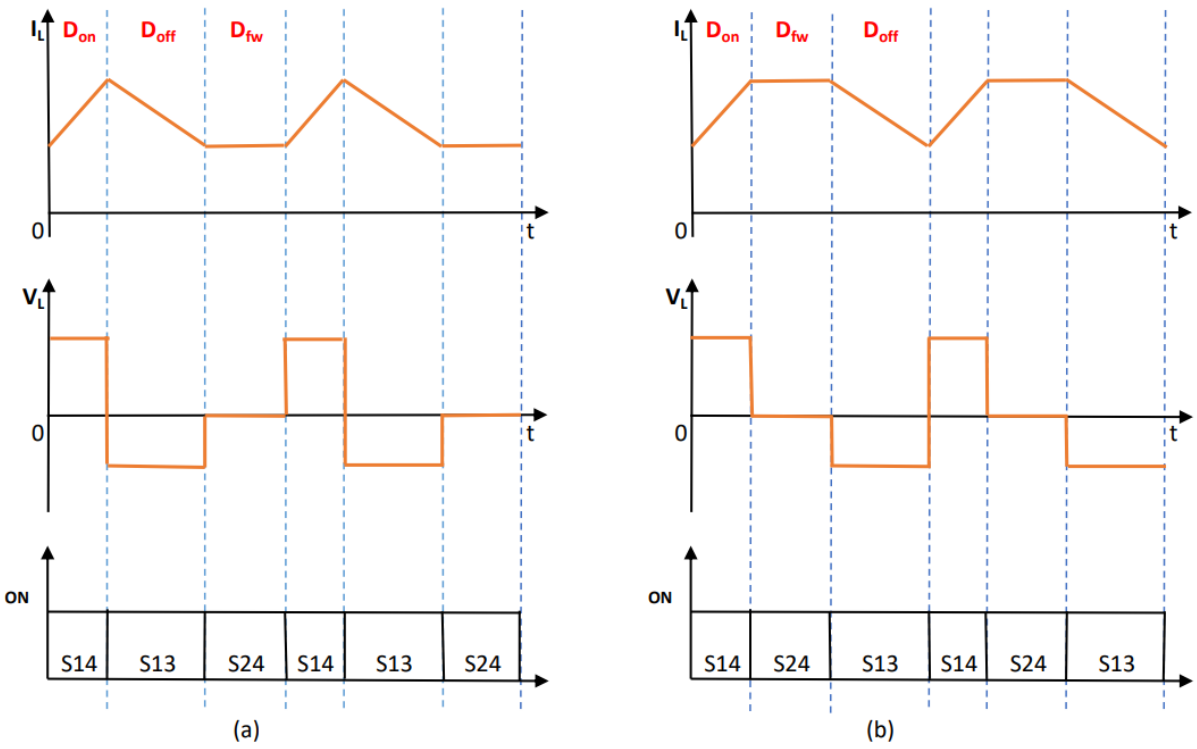

Figure 2- 8 Theoretical waveforms of inductor current, inductor voltage, ON switches for tri-state Boost mode of operation with (a) sequence #1 (b) sequence #2

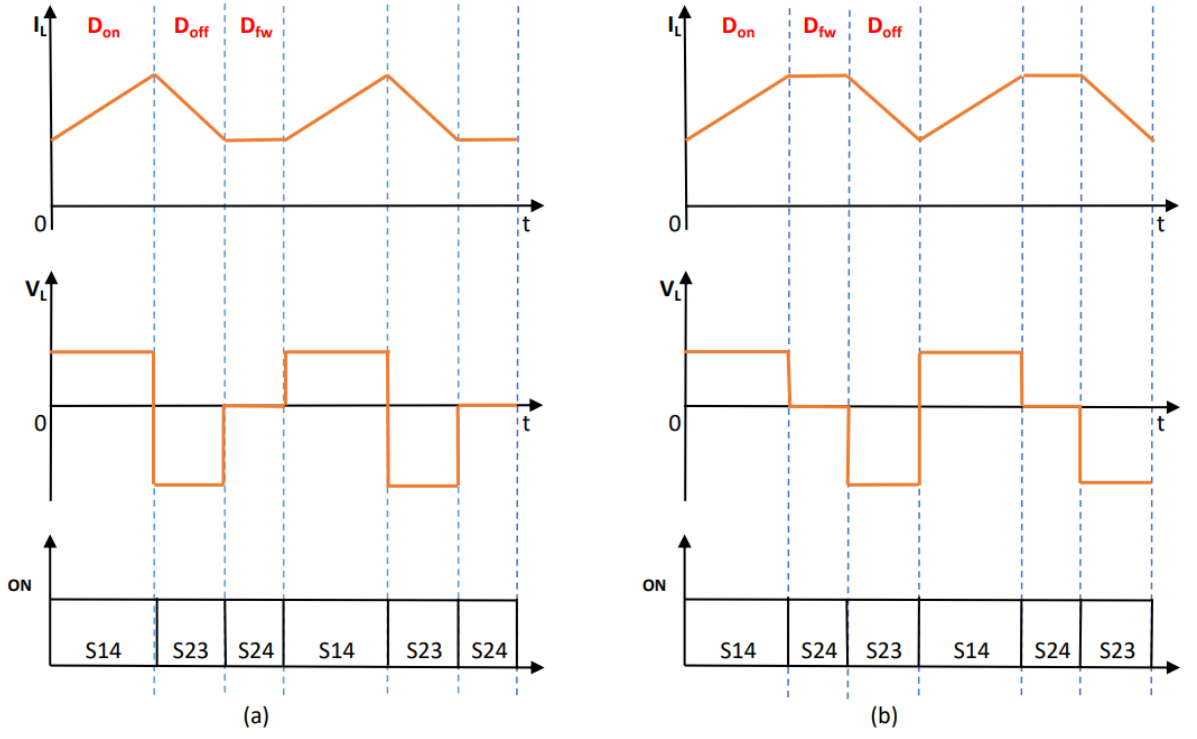

Figure 2- 9 Theoretical waveforms of inductor current, inductor voltage, ON switches for tri-state Buck-Boost mode of operation with (a) sequence #1 (b) sequence #2

2.2.5 Component selection and calculation

To get the desired 4-switch bidirectional DC-DC converter operating as expected, selecting the appropriate inductor and capacitors is important.

The system parameters using in this project are shown in Table 2.6.

Table 2. 6 System parameters

Parameter	value
Fixed D_{off} for tri-state operation	0.35
Switching frequency f_{sw}	50 kHz
R_f between output capacitor and DC bus	0.2 Ω
Input voltage V_{in}	24 V ~ 48 V
DC bus voltage V_{dc}	48 V
D_{on}	0.1 ~ 0.55
I_{ref}	±5 A
Output voltage V_o (V_{dc} +/- I_{ref} R_f)	47 V ~ 49 V

1) Inductor selection

To select the inductor for the power converter, one has to consider the ripple allowed for the inductor current in both Boost and Buck-Boost modes. Considering the worst-case ripple allowed for the system as 40% of the maximum I_L ($I_L = I_o / D_{off}$), which means

$$\Delta I_L \leq 40\% \frac{I_o}{D_{off}} \tag{2-13}$$

So $\Delta I_L < 6$ A with the system parameters $I_o = 5$ A , $D_{off} = 0.35$, D_{on}: 0.1 ~ 0.55, $f_{sw} = 50$ kHz.

In Boost mode of operation, the equation of the inductor current ripple is given by [19]

$$\Delta I_L = \frac{V_{in} D_{on}}{L f_{sw}} = \frac{V_o D_{on} D_{off}}{(D_{on} + D_{off}) L f_{sw}} \tag{2-14}$$

From the equation (2-14), the inductor current ripple increases when the value of D_{on} increases, and the biggest inductor current ripple is 6 A when the D_{on} is 0.55 and the maximum output voltage is 49 V.

$$\frac{V_{oMax}}{6 \times 50 \times 10^3 \times (\frac{1}{0.35} + \frac{1}{D_{onMax}})} \leq L_{Min}$$

$$L_{Min} \geq 35\ \mu H$$

In Buck-Boost mode of operation, the equation of the inductor current ripple is given by [19]

$$\Delta I_L = \frac{V_o D_{off}}{L f_{sw}} \quad (2\text{-}15)$$

In equation (2-15), the inductor current ripple is the max when V_o is 49 V with the fixed D_{off}.

$$\frac{0.35 \times V_{oMax}}{6 \times 50 \times 10^3} \leq L_{Min}$$

$$L_{Min} \geq 57\ \mu H$$

The inductor should be suitable for operating in both Boost mode and Buck-Boost mode, therefore, for both Boost and Buck-Boost modes, the inductance $L_{Min} \geq 57\ \mu H$. Due to the availability of parts, a 47 µH 32A inductor was employed, yielding a higher inductor current ripple in the Buck-Boost mode, what was found acceptable.

Since the peak inductor current increases with decreasing inductance, the peak inductor current for a 57 µH inductor in Buck-Boost mode is around 17.3 A ($I_{Lmax} = I_o/D_{off} + ½\ \Delta I_L$). With the selected inductor 47 μH, D_{off} = 0.35, D_{on} = 0.55, f_{sw} = 50 kHz, and V_o = 49 V, the inductor current ripple ΔI_L equals 7.29 A, then the peak inductor current is 17.9 A which is acceptable, though it is a little larger compared to the value getting from the original design specifications.

2) Output capacitor selection

This 4-switch bidirectional DC-DC converter is designed to connect a SC to an ideal DC grid through a feeder impedance which is 0.2 Ω. To select an appropriate output capacitor for this converter, assuming most of the current harmonics flow through the capacitor, then the capacitor should present at the switching (dominant harmonic) frequency an impedance (X_c) less of 10% of the feeder impedance/resistance, that is

$$X_c < 10\% R_f \quad (2\text{-}16)$$

Therefore

$$\frac{1}{2\pi f_{sw} C} < 10\% R_f$$

With f_{sw} = 50 kHz, R_f = 0.2 Ω,

$$C > 160\ \mu F$$

The ceramic capacitors, which are low ESR capacitors, are good to minimize the output voltage ripple. So, a capacitor bank with ten 4.7 µF ceramic capacitors and four 39 µF hybrid polymer aluminum electrolytic capacitors are used to get the output capacitance as 203 µF. Besides, the input capacitor bank has been selected the same as the output capacitor, since the converter is desired to be symmetrical.

2.3 Control strategy

2.3.1 State-space averaging method to derive the transfer functions of the converter

Assuming that the average value of the SC voltage (V_{in}) is smaller than the average value of the output voltage (V_o), and that the SC injects current into the DC bus, as shown in Figure 2-10.

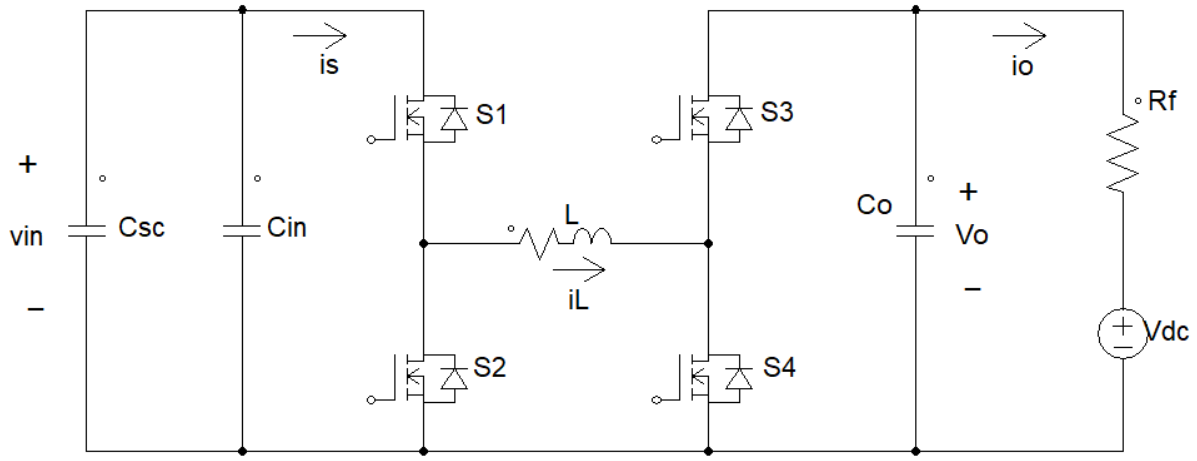

Figure 2- 10 The 4-switch bidirectional converter interfacing a SC to the DC bus

2.3.1.1 Derivation of the transfer function of converter operating in Boost mode *($V_{in} < V_o$)*

The current/power flow corresponding to each state while the converter operates in Boost mode are analyzed.

1) ON state: $t_{on} = D_{on}T_s$.

When S1-S4 are ON, the voltage across the inductor (v_L) is v_{in}, increasing the inductor current (i_L). The state equations are given below.

$$\left[L\frac{dI_L}{dt} = V_{in}\right], \left[V_o = V_{dc} + I_o R_f\right], \left[C_o\frac{dV_o}{dt} = -I_o\right] \quad (2\text{-}17)$$

2) OFF state: $t_{off} = D_{off}T_s$

When S1-S3 are ON, the voltage across the inductor is ($v_{in} - v_o$, with $V_{in} < V_o$), decreasing the inductor current. The equations for this state are given below.

$$\left[L\frac{dI_L}{dt} = V_{in} - V_o\right], \left[V_o = V_{dc} + I_o R_f\right], \left[C_o\frac{dV_o}{dt} = I_L - I_o\right] \quad (2\text{-}18)$$

3) Free-wheeling state: $t_{fw} = D_{fw}T_s$

When S2-S4 are ON. The voltage across the inductor is null and the inductor current remains constant. The equations for this state are given below.

$$\left[L\frac{dI_L}{dt} = 0\right], \left[V_o = V_{dc} + I_o R_f\right], \left[C_o\frac{dV_o}{dt} = -I_o\right] \quad (2\text{-}19)$$

With $D_{on} + D_{off} + D_{fw} = 1$, averaging the Boost converter differential equations gives:

$$L\frac{dI_L}{dt} = -D_{off}V_o + \left(D_{on} + D_{off}\right)V_{in} \quad (2\text{-}20)$$

$$V_o = V_{dc} + I_o R_f \quad (2\text{-}21)$$

$$C_o\frac{dV_o}{dt} = D_{off}I_L - I_o \quad (2\text{-}22)$$

Considering that D_{off} is fixed and introducing the small-signal perturbations around a base operating point.

$$L\frac{d(\tilde{\imath_L} + I_L)}{dt} = -D_{off}(\tilde{v_o} + V_o) + \left(\tilde{d} + D_{on} + D_{off}\right)(\tilde{v_{in}} + V_{in}) \quad (2\text{-}23)$$

$$C_o\frac{d(\tilde{v_o} + V_o)}{dt} = D_{off}(\tilde{\imath_L} + I_L) - (\tilde{\imath_o} + I_o) \quad (2\text{-}24)$$

$$\tilde{\imath_o} + I_o = \frac{\tilde{v_o} + V_o - V_{dc}}{R_f} \quad (2\text{-}25)$$

The linearized equivalent model with the above equations can be represented by

$$\frac{d\widetilde{\imath_L}}{dt} = -\frac{D_{off}}{L}\widetilde{v_o} + \frac{V_{in}}{L}\tilde{d} + \left(D_{on} + D_{off}\right)\widetilde{v_{in}} \quad (2\text{-}26)$$

$$\frac{d\widetilde{v_o}}{dt} = \frac{D_{off}}{C_o}\widetilde{\imath_L} - \frac{\widetilde{v_o}}{C_o R_f} \quad (2\text{-}27)$$

$$\widetilde{\imath_o} = \frac{\widetilde{v_o}}{R_f} \quad (2\text{-}28)$$

Choosing $\widetilde{\imath_L}$ and $\widetilde{v_o}$ as the state variables, to show the influence of variations of the duty cycle $\tilde{d}$ on the output current $\widetilde{\imath_o}$, the signal $\widetilde{v_{in}}$ can be seen as a disturbance signal to this system. The state space equations, can be obtained from equations (2-26), (2-27) and (2-28), the state space equations are given by

$$\begin{bmatrix} \frac{d\widetilde{\imath_L}}{dt} \\ \frac{d\widetilde{v_o}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{D_{off}}{L} \\ \frac{D_{off}}{C_o} & -\frac{1}{C_o R_f} \end{bmatrix} \begin{bmatrix} \widetilde{\imath_L} \\ \widetilde{v_o} \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix} \tilde{d} \quad (2\text{-}29)$$

$$\widetilde{\imath_o} = \begin{bmatrix} 0 & \frac{1}{R_f} \end{bmatrix} \begin{bmatrix} \widetilde{\imath_L} \\ \widetilde{v_o} \end{bmatrix} + \mathbf{0}\tilde{d} \quad (2\text{-}30)$$

The state space equations can be represented as below.

$$\begin{cases} \frac{d}{dt}\boldsymbol{X} = \boldsymbol{A}\boldsymbol{X} + \boldsymbol{B}d \\ i_o = \boldsymbol{C}\boldsymbol{X} + \boldsymbol{D}d \end{cases} \quad (2\text{-}31)$$

where

$$\boldsymbol{X} = \begin{bmatrix} \widetilde{\imath_L} \\ \widetilde{v_o} \end{bmatrix} \quad (2\text{-}32)$$

$$\boldsymbol{A} = \begin{bmatrix} 0 & -\frac{D_{off}}{L} \\ \frac{D_{off}}{C_o} & -\frac{1}{C_o R_f} \end{bmatrix} \quad (2\text{-}33)$$

$$\boldsymbol{B} = \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix} \quad (2\text{-}34)$$

$$\boldsymbol{C} = \begin{bmatrix} 0 & \frac{1}{R_f} \end{bmatrix} \quad (2\text{-}35)$$

$$\boldsymbol{D} = \mathbf{0} \quad (2\text{-}36)$$

Using Laplace transform on equation (2-31)

$$\begin{cases} sX(s) = \boldsymbol{A}X(s) + \boldsymbol{B}d(s) \\ i_o(s) = \boldsymbol{C}X(s) + \boldsymbol{D}d(s) \end{cases} \quad (2\text{-}37)$$

The transfer functions between the state variables and the control variable:

$$\frac{X(s)}{d(s)} = (s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B} \quad (2\text{-}38)$$

$$\boldsymbol{I} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (2\text{-}39)$$

Calculating the transfer function

$$s\boldsymbol{I} - \boldsymbol{A} = \begin{bmatrix} s & 0 \\ 0 & s \end{bmatrix} - \begin{bmatrix} 0 & -\frac{D_{off}}{L} \\ \frac{D_{off}}{C_o} & -\frac{1}{C_o R_f} \end{bmatrix} = \begin{bmatrix} s & \frac{D_{off}}{L} \\ -\frac{D_{off}}{C_o} & s + \frac{1}{C_o R_f} \end{bmatrix}$$

$$(s\boldsymbol{I} - \boldsymbol{A})^{-1} = \frac{1}{s\left(s + \frac{1}{C_o R_f}\right) - \frac{D_{off}}{L} \times \left(-\frac{D_{off}}{C_o}\right)} \begin{bmatrix} s + \frac{1}{C_o R_f} & -\frac{D_{off}}{L} \\ \frac{D_{off}}{C_o} & s \end{bmatrix}$$

$$= \frac{1}{s^2 + \frac{1}{C_o R_f} s + \frac{{D_{off}}^2}{L C_o}} \begin{bmatrix} s + \frac{1}{C_o R_f} & -\frac{D_{off}}{L} \\ \frac{D_{off}}{C_o} & s \end{bmatrix}$$

Therefore,

$$\frac{X(s)}{d(s)} = \frac{1}{s^2 + \frac{1}{C_o R_f} s + \frac{{D_{off}}^2}{L C_o}} \begin{bmatrix} s + \frac{1}{C_o R_f} & -\frac{D_{off}}{L} \\ \frac{D_{off}}{C_o} & s \end{bmatrix} \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix}$$

$$= \frac{1}{s^2 + \frac{1}{C_o R_f} s + \frac{{D_{off}}^2}{L C_o}} \begin{bmatrix} \frac{V_{in}}{L}\left(s + \frac{1}{C_o R_f}\right) \\ \frac{V_{in} D_{off}}{C_o L} \end{bmatrix}$$

Which leads to

$$\frac{X(s)}{d(s)} = \begin{bmatrix} \frac{i_L(s)}{d(s)} \\ \frac{v_o(s)}{d(s)} \end{bmatrix} = \begin{bmatrix} \frac{V_{in}}{L} \frac{s+\frac{1}{C_o R_f}}{s^2+\frac{1}{C_o R_f}s+\frac{D_{off}{}^2}{LC_o}} \\ \frac{V_{in} D_{off}}{C_o L} \frac{1}{s^2+\frac{1}{C_o R_f}s+\frac{D_{off}{}^2}{LC_o}} \end{bmatrix} \quad (2\text{-}40)$$

The transfer function of the output current i_o to the control signal d is

$$\frac{i_o(s)}{d(s)} = \boldsymbol{C}\frac{X(s)}{d(s)} + \boldsymbol{D} \quad (2\text{-}41)$$

Which is

$$\frac{i_o(s)}{d(s)} = \begin{bmatrix} 0 & \frac{1}{R_f} \end{bmatrix} \begin{bmatrix} \frac{V_{in}}{L} \frac{s+\frac{1}{C_o R_f}}{s^2+\frac{1}{C_o R_f}s+\frac{D_{off}{}^2}{LC_o}} \\ \frac{V_{in} D_{off}}{C_o L} \frac{1}{s^2+\frac{1}{C_o R_f}s+\frac{D_{off}{}^2}{LC_o}} \end{bmatrix} + 0$$

$$= \frac{V_{in} D_{off}}{R_f C_o L} \frac{1}{s^2+\frac{1}{C_o R_f}s+\frac{D_{off}{}^2}{LC_o}} \quad (2\text{-}42)$$

Replacing $\frac{L}{Doff^2}$ as L_{eq} in the equation (2-42), the input-output transfer function is shown below.

$$\frac{i_o(s)}{d(s)} = \frac{V_{in}}{(D_{off} R_f L_{eq} C_o)} \left[\frac{1}{s^2+\frac{s}{C_o R_f}+\frac{1}{L_{eq} C_o}} \right] \quad (2\text{-}43)$$

Where $Leq = \frac{L}{Doff^2}$.

2.3.1.2 Derivation of the transfer function of converter operating in Buck-Boost mode

The operation of the 4-switch bidirectional DC-DC converter in the Buck-Boost mode with tri-state logic is similar to the Boost mode. The switches corresponding to D_{on} state and free-wheeling state D_{fw} are the same ones as in the Boost mode. However, for the D_{off} state, switches S2 and S3 are turned ON instead of S1 and S3 in Boost mode. Therefore, the equations of the OFF-state change and are given by

$$\left[\frac{dI_L}{dt} = -\frac{V_o}{L}\right], \left[V_o = V_{dc} + I_o R_f\right], \left[C_o \frac{dV_o}{dt} = I_L - I_o\right] \quad (2\text{-}44)$$

With $D_{on} + D_{off} + D_{fw} = 1$, averaging the differential equations for the tri-state of Buck-Boost converter gives:

$$L \frac{dI_L}{dt} = -D_{off} V_o + D_{on} V_{in} \quad (2\text{-}45)$$

$$C_o \frac{dV_o}{dt} = D_{off} I_L - I_o \quad (2\text{-}46)$$

$$I_o = \frac{V_o - V_{dc}}{R_f} \quad (2\text{-}47)$$

Considering that D_{off} is fixed and introducing the small-signal perturbations around a base operating point.

$$\frac{d(\tilde{\imath_L} + I_L)}{dt} = -D_{off}(\tilde{v_o} + V_o) + (\tilde{d} + D_{on})(\tilde{v_{in}} + V_{in}) \quad (2\text{-}48)$$

$$C_o \frac{d(\tilde{v_o} + V_o)}{dt} = D_{off}(\tilde{\imath_L} + I_L) - (\tilde{\imath_o} + I_o) \quad (2\text{-}49)$$

$$\tilde{\imath_o} + I_o = \frac{\tilde{v_o} + V_o - V_{dc}}{R_f} \quad (2\text{-}50)$$

The linearized equivalent model of the above equations can be represented

$$\frac{d\tilde{\imath_L}}{dt} = -\frac{D_{off}}{L}\tilde{v_o} + \frac{V_{in}}{L}\tilde{d} + D_{on}\tilde{v_{in}} \quad (2\text{-}51)$$

$$\frac{d\tilde{v_o}}{dt} = \frac{D_{off}}{C_o}\tilde{\imath_L} - \frac{\tilde{v_o}}{C_o R_f} \quad (2\text{-}52)$$

$$\tilde{\imath_o} = \frac{\tilde{v_o}}{R_f} \quad (2\text{-}53)$$

Choosing $\tilde{\imath_L}$ and $\tilde{v_o}$ as the state variables, to show the influence of variations of the duty cycle $\tilde{d}$ on the output current $\tilde{\imath_o}$, the signal $\tilde{v_{in}}$ can be seen as a disturbance to this system. The state space equations can be shown below which are the same as the ones of the Boost mode of operation.

$$\begin{bmatrix} \frac{d\widetilde{i_L}}{dt} \\ \frac{d\widetilde{v_o}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{D_{off}}{L} \\ \frac{D_{off}}{C_o} & -\frac{1}{C_o R_f} \end{bmatrix} \begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_o} \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix} \tilde{d} \quad (2\text{-}54)$$

$$\widetilde{i_o} = \begin{bmatrix} 0 & \frac{1}{R_f} \end{bmatrix} \begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_o} \end{bmatrix} + \mathbf{0}\tilde{d} \quad (2\text{-}55)$$

Using the same calculation procedure as before, one can get the transfer function between state variables and control signal, also the transfer function between output current and control signal.

$$\frac{X(s)}{d(s)} = \begin{bmatrix} \frac{i_L(s)}{d(s)} \\ \frac{v_o(s)}{d(s)} \end{bmatrix} = \begin{bmatrix} \frac{V_{in}}{L} \frac{s+\frac{1}{C_o R_f}}{s^2+\frac{1}{C_o R_f}s+\frac{{D_{off}}^2}{LC_o}} \\ \frac{V_{in} D_{off}}{C_o L} \frac{1}{s^2+\frac{1}{C_o R_f}s+\frac{{D_{off}}^2}{LC_o}} \end{bmatrix} \quad (2\text{-}56)$$

$$\frac{i_o(s)}{d(s)} = \frac{V_{in}}{(D_{off} R_f L_{eq} C_o)} \left[\frac{1}{s^2+\frac{s}{R_f C_o}+\frac{1}{L_{eq} C_o}} \right] \quad (2\text{-}57)$$

Where $Leq = \frac{L}{{Doff}^2}$.

The transfer function of the output current to the control signal is the same in both Boost and Buck-Boost modes. Therefore, the same controller can control the converter to operate in Buck-Boost and Boost modes.

2.3.2 Single duty cycle control

With the transfer function of the output current with respect to d_{on}, a single duty cycle control scheme with a proportional integral (PI) controller can be used for this 4-switch bidirectional DC-DC converter.

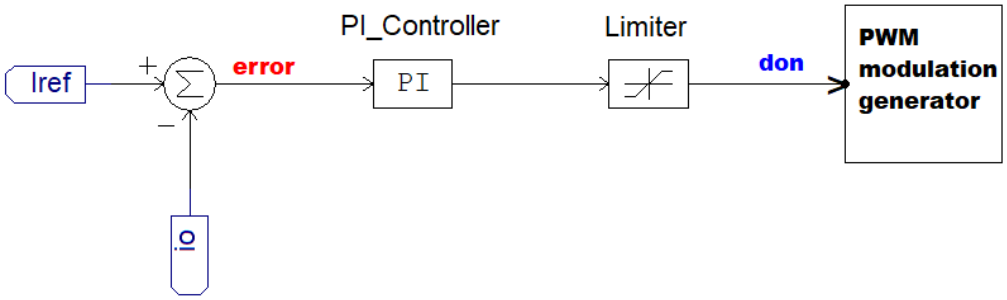

Figure 2- 11 Control scheme for the 4-switch bidirectional DC-DC converter

In Figure 2-11, the actual output current i_o is compared to the reference average output current I_{ref}. Then the error is fed into the PI controller which produces the initial control signal. After a limiter, the control signal d_{on} is between 0.1 and 0.55, the final modulation signal d_{on} is provided to the PWM modulation generator which generates the gating signals for the four switches.

2.3.3 Design of the PI controller

The bandwidth of the control loop is chosen as $f_x = 10\% f_{sw}$ and the phase margin is selected as 60° to design the controller. The switching frequency f_{sw} of the converter is 50 kHz, so the crossover frequency of the converter becomes:

$$\omega_x = 2\pi\, f_{sw}\, 10\% = 31415.9\, rad/s$$

Table 2.7 shows the basic parameters of the 4-switch converter to design the controller.

Table 2. 7 Nominal 4-switch converter parameters

Parameter	value
Inductor L	47 µH
Output capacitor C_o	203 µF
Fixed D_{off} for tri-state operation	0.35
R_f between output capacitor and DC bus	0.2 Ω
Input voltage V_{in}	48 V
Output voltage V_o	52.8 V

With the basic parameters, the transfer function of the plant becomes:

$$G(s) = \frac{i_o(s)}{d(s)} = \frac{8.804\times10^9}{s^2+2.463\times10^4 s+1.284\times10^7} \quad (2\text{-}58)$$

At the crossover frequency ($s = j\omega_x$),

$$G(j\omega_x) = \frac{i_o(j\omega_x)}{d(j\omega_x)} = \frac{88.04}{-9.74+7.73j} \quad (2\text{-}59)$$

The gain and the phase at the crossover frequency are computed:

$$|G(j\omega_x)| = 7.077, \qquad \angle G(j\omega_x) = -141.5382°$$

Figure 2-12 shows the Bode plot of the transfer function of the plant *G(s)*.

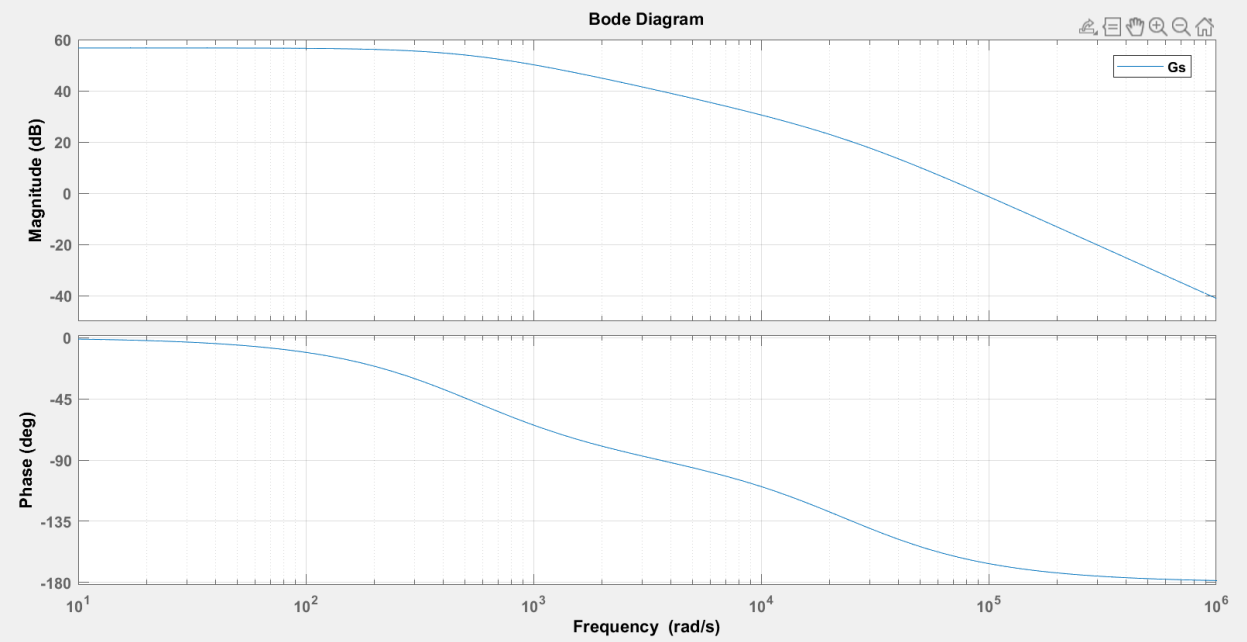

Figure 2- 12 Bode plot of the plant for the design of current loop

In general, it is ideal to have a high gain at the low frequency range to minimize the steady state error. Around the crossover frequency, maintaining a gain slope of -20 dB/dec can ensure an adequate phase margin, and at the high frequency range, a very small gain can minimize the

influence of the switching harmonics and overall noise. As shown in Figure 2-12, the gain of the plant is constant at low frequency, and the gain slope around the crossover frequency is - 40 dB/dec, therefore, a type 3 PI controller is selected in this project to increase the gain at lower frequency and achieve the desired -20 dB/dec at the crossover frequency.

The transfer function of the type 3 PI controller is given by:

$$Gc(s) = \frac{K_{PI}}{s\tau}\frac{(1+s\tau)^2}{(1+sT_P)^2} \quad (2\text{-}60)$$

Computing

$$|Gc(j\omega_x)| = \frac{1}{|G(j\omega_x)|} \approx 0.1413, \qquad \angle Gc(j\omega_x) = 60° - \left(180° + \angle G(j\omega_x)\right) \approx 21.54°$$

Therefore, the type 3 PI controller should present a phase lead of 21.54° and a gain of 0.1413 at the crossover frequency.

With the equations

$$\angle Gc(j\omega_x) = -90° + boost. \qquad 0° < boost < 180° \quad (2\text{-}61)$$

$$K = tan\left(\frac{boost}{4} + 45°\right) \quad (2\text{-}62)$$

The "boost" angle is calculated as 111.54° and $K \approx 3.25$.

The parameters in equation (2-60) can be calculated as follows.

$$\omega_m = \omega_x = 31415.9\, rad/s \quad (2\text{-}63)$$

$$\frac{1}{\tau} = \frac{\omega_m}{K} \quad (2\text{-}64)$$

$$\frac{1}{T_P} = K\omega_m \quad (2\text{-}65)$$

$$|Gc(j\omega_m)| = \frac{K_{PI}}{K}\frac{1+K^2}{1+\frac{1}{K^2}} \quad (2\text{-}66)$$

After the calculations:

$\tau = 103.37$ µs, $T_P = 9.8$ µs, and $K_{PI} = 0.0435$.

Figure 2-13 illustrates the Bode plot of the transfer function of the plant (*Gs*) and the loop transfer function (*Gs_pi*) with the designed type 3 PI controller. One can see that at the lower frequency range, the gain of the loop transfer function is increased compared to the transfer function of the plant, and the design specs ($\omega_x = 31415.9\ rad/\text{s}\ and\ PM = 60^{\circ}$) were accomplished.

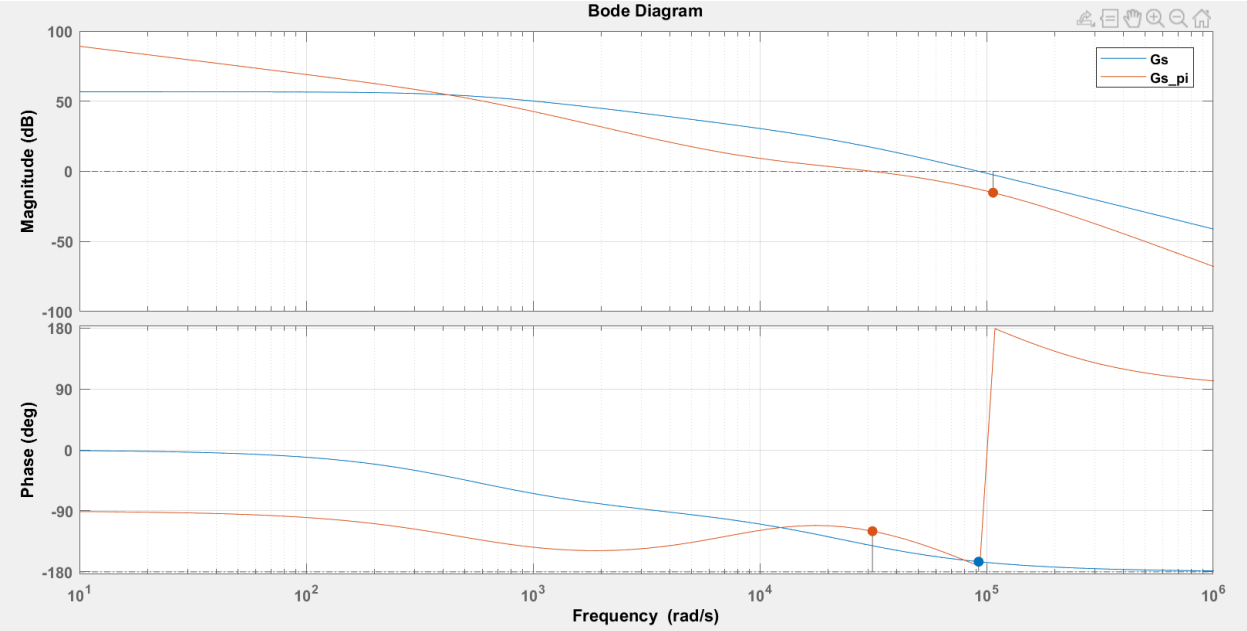

Figure 2- 13 Bode plot of the plant with a type 3 PI controller for the design of current loop

2.4 Conventional dual-state operation

The conventional dual-state scheme contains only the ON and OFF states, and can operate in Boost, Buck-Boost, and Buck modes. Without limit of the voltage gain caused by the fixed D_{off}. In principle, the converter with dual-state can operate in Buck-Boost mode when the input voltage varies in the range between 24 V to 48 V, which is used in this project to compare with the converter working with tri-state logic.

2.4.1 Switching scheme for Buck-Boost mode

Considering the current flow path of the 4-switch bidirectional converter in Figure 2-2 and Figure 2-3, the truth table of switches operating with dual-state in Buck-Boost mode are shown in Table 2.8.

Table 2. 8 Truth table of switches of the converter with dual-state in Buck-Boost modes

Dual-state Buck-Boost mode				
State/Switches	S1	S2	S3	S4
D_{on}	ON	OFF	OFF	ON
D_{off}	OFF	ON	ON	OFF

The transfer function of the output current (i_o) with respect to the control variable (d) in Buck-Boost mode of operation is given by [10]

$$\frac{i_o(s)}{d(s)} = \frac{V_o+V_{in}-SL_{eq}I_L(1-D_{on})}{(1-D_{on})R_f L_{eq} C_o}\left(\frac{1}{S^2+\frac{1}{C_o R_f}S+\frac{1}{L_{eq}C_o}}\right) \quad (2\text{-}67)$$

where $L_{eq} = \frac{L}{(1-D_{on})^2}$.

One can see that there is the RHP zero in equation (2-67), while there is no RHP zero in the transfer function of the converter operating with tri-state as evident from equation (2-57). Therefore, for the converter operating with dual-state logic, cascaded control loops with an inner inductor current control loop and an outer output current control loop can be used to avoid the RHP zero [10].

The scheme of the cascade control loops is shown in Figure 2-14.

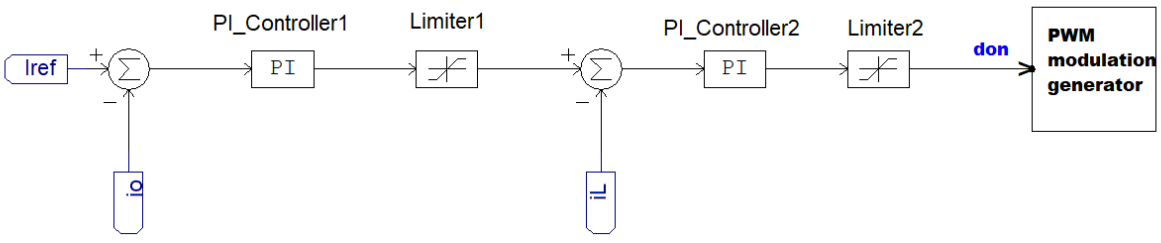

Figure 2- 14 The scheme of the cascade control loops for dual-state

2.4.2 Design controllers for the cascade control loops

For the dual-state Buck-Boost mode of operation, the controller for the inner inductor current control loop will be design first and then the controller for the outer output current control loop will be designed.

Table 2.9 shows the basic system parameters for the dual-state Buck-Boost mode of operation.

Table 2. 9 Basic parameters for design controller of the dual-state Buck-Boost mode of operation

Parameter	value
Inductor L	47 µH
Output capacitor C_o	203 µF
Switching frequency f_{sw}	50 kHz
R_f between output capacitor and DC bus	0.2 Ω
Input voltage V_{in}	24 V
V_o	52.8 V
I_o	5 A
D_{on}	0.68

For the inner current loop, and the transfer function of the inner plant is: [19]

$$\frac{i_L(s)}{d(s)} = \frac{(1-D)I_L + V_o C_o S + \frac{V_o}{R_f}}{C_o L S^2 + \frac{L}{R_f} S + (1-D)^2} \qquad (2\text{-}68)$$

To design the controller, the crossover frequency (f_x) is selected as 10% of the switching frequency (f_{sw}), and the phase margin is set as 60°.

The crossover frequency is:

$$\omega_x = 2\pi f_{sw}\, 10\% = 31415.9\, rad/s.$$

The gain and the phase of the plant at the crossover frequency are computed as:

$$|G_L(j\omega_x)| = 36.2621, \qquad \angle G_L(j\omega_x) = -90.2185°$$

Figure 2-15 shows the Bode plot of the transfer function of the inner plant (*sys_inner*).

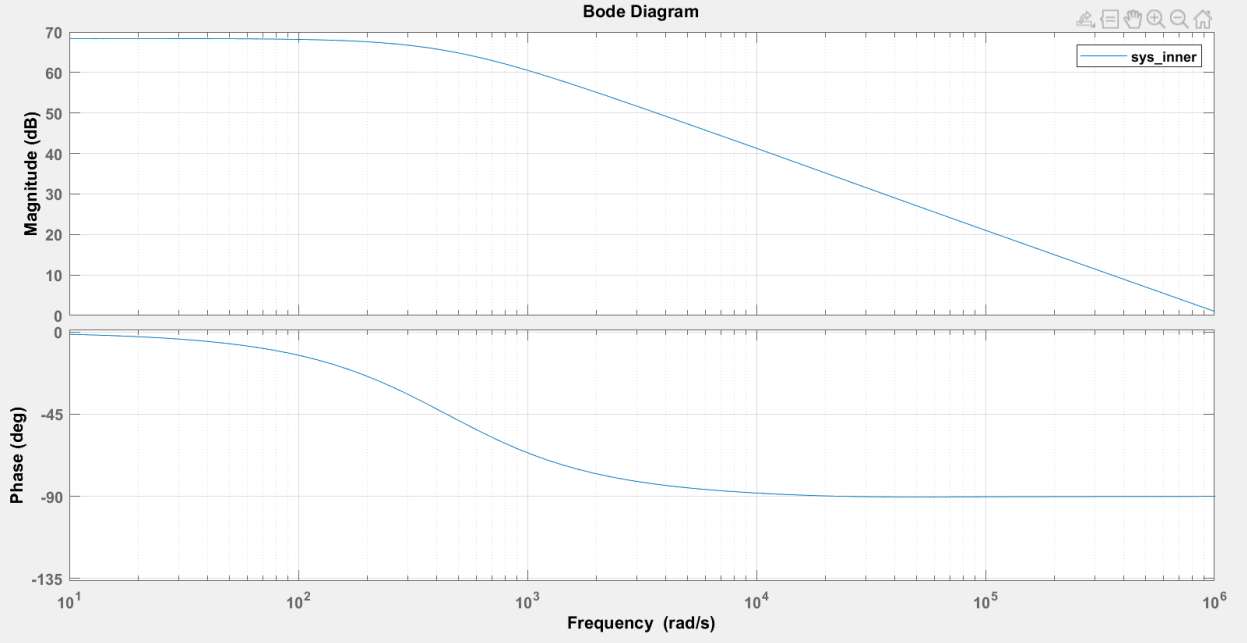

Figure 2- 15 Bode plot of the inner plant sys_inner

In Figure 2-15, one can see that the gain at the low frequency range is kept constant, and the slope of the plant at the crossover frequency is -20 dB/dec, thus, for this case, a type 2 PI controller is selected.

The transfer function of the type 2 PI controller is given by:

$$G_{L_C}(s) = K_{PI}\frac{1+s\tau}{s\tau}\frac{1}{1+sT_P} \quad (2\text{- }69)$$

Computing

$$|G_{L_C}(j\omega_x)| = \frac{1}{|G_L(j\omega_x)|} = 0.027, \qquad \angle G_{L_C}(j\omega_x) = 60° - \left(180° + \angle G_L(j\omega_x)\right) = -29.78°$$

With the equations

$$\angle G_{L_C}(j\omega_x) = -90° + boost. \qquad 0° < boost < 90° \quad (2\text{- }70)$$

$$K = tan\left(\frac{boost}{2} + 45°\right) \quad (2\text{- }71)$$

The "boost" angle is calculated as 60.21° and $K \approx 3.76$.

$$\omega_m = \omega_x = 31415.9\ rad/s \quad (2\text{- }72)$$

$$\omega_m = K\frac{1}{\tau} \quad (2\text{- }73)$$

$$\frac{1}{T_P} = K\omega_m \tag{2- 74}$$

After calculation:

$$\tau = 119.71\ \mu s,\ T_P = 8.46\ \mu s,\ K_{PI} = 0.0276.$$

Figure 2-16 shows the Bode plot of the transfer function of the inner plant (*sys_inner*) and the loop transfer function (LTF), with the designed PI controller. One can see that, with the designed type 2 PI controller, the design specs ($\omega_x = 31415.9\ rad/s\ and\ PM = 60^o$) were accomplished.

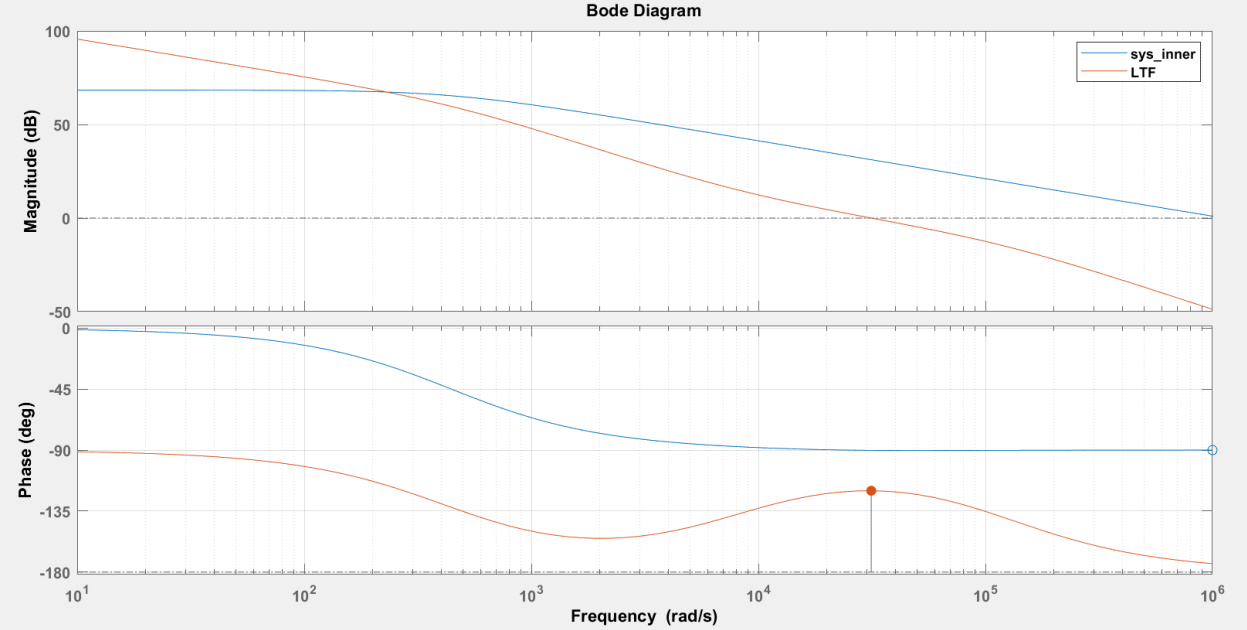

Figure 2- 16 Bode plot of the plant sys_inner and LTF

For the outer loop, the transfer function for the outer loop for controlling the injected current is given by,

$$\frac{i_o}{i_L} = \frac{1-D_{on}}{1+sR_fC_o} \tag{2- 75}$$

The outer control loop should be slower than the inner control loop, the crossover frequency of the outer control loop is chosen as 10% of the crossover frequency of the inner current loop, which is $\omega_o = \omega_x\ 10\% = 3141.59\ \text{rad/s}$, and the phase margin is chosen as 85°. Recall that in this case, the inner inductor current loop with unity feedback can be replaced by a unity gain.

The gain and the phase of the outer plant at the crossover frequency ω_o are computed as:

$$|G_o(j\omega_o)| = 0.3174, \qquad \angle G_o(j\omega_o) = -7.2687°$$

Figure 2-17 shows the Bode plot of the transfer function of the outer plant (*sys_outer*).

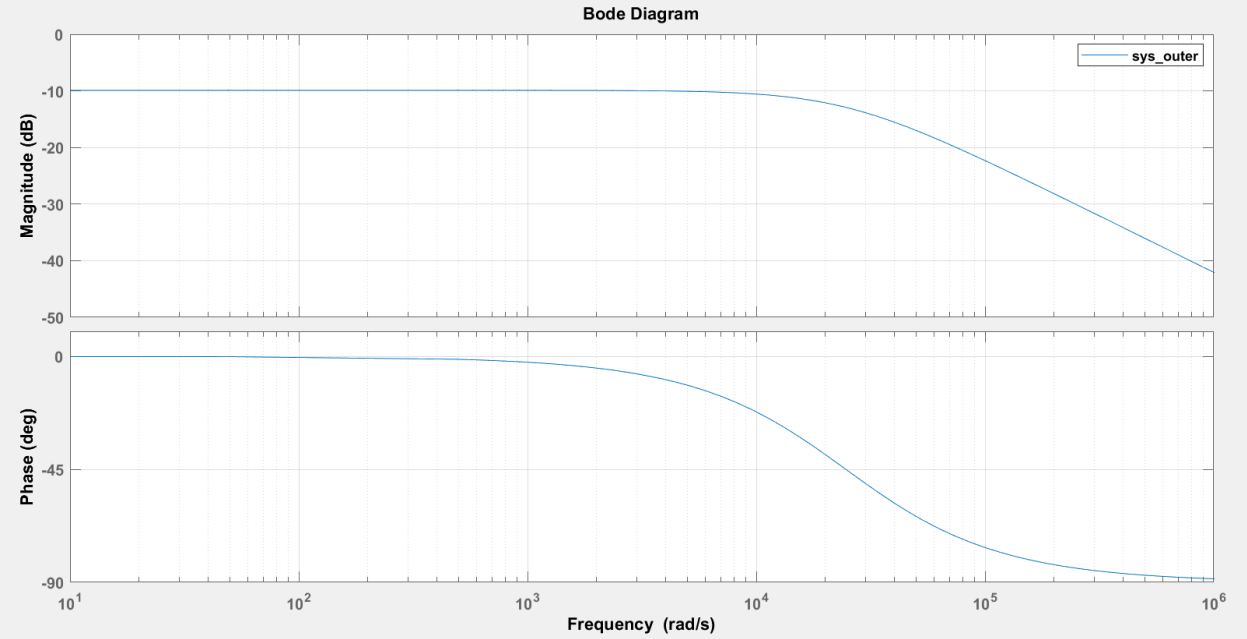

Figure 2- 17 Bode plot of the outer plant sys_outer

Figure 2-17 shows that the gain at the low frequency range is constant and the slop of the plant at the crossover frequency is 0, therefore, a type 2 PI controller is designed to achieve the desired slope of – 20 dB/dec there.

Using the same calculation procedure, the type 2 PI controller is designed the outer loop and the parameters are:

$$\tau = 311.17\ \mu s,\ T_P = 305.95\ \mu s,\ K_{PI} = 3.1503.$$

The Bode plot of the transfer function of the outer plant (*sys_outer*), and with the designed type 2 PI controller, the loop transfer function (LTF) are shown in Figure 2-18. With the designed PI controller, one can see that, the design specs (ω_o = 3141.59 rad/s and PM = 85^o) were accomplished.

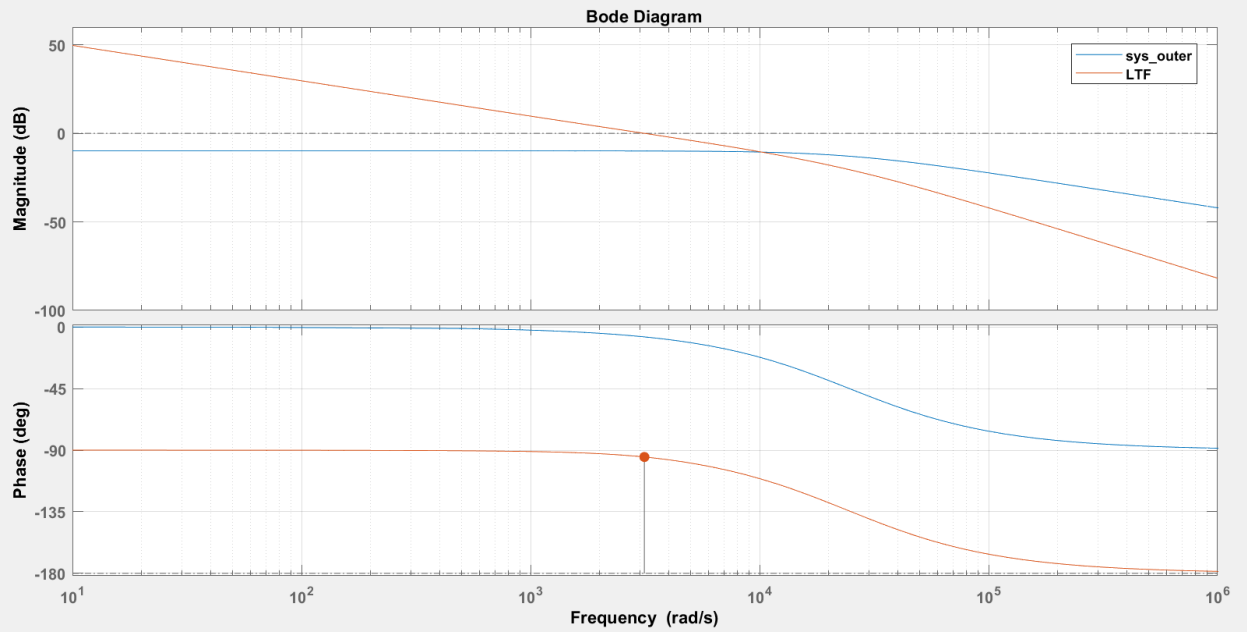

Figure 2- 18 Bode plot of the plant sys_outer and LTF

2.5 Simulation scheme

The performance of the tri-state logic applied to the 4-switch bidirectional DC-DC converter is verified with simulation using PSIM in both Boost and Buck-Boost modes of operation. For a rated 48 V DC bus, and the input voltage is in the range between 24 V and 48 V. Because of the limited voltage gains in the Buck-Boost and Boost modes with tri-state modulation, the converter must operate in two modes, to regulate the output current.

2.5.1 Space vector modulation scheme

The 4-switch bidirectional DC-DC converter can operate with tri-state in Boost mode or Buck-Boost mode. Depending on the value of the input voltage and the two possible sequences of states which were discussed previously, sequence #1 D_{on} -D_{off} - D_{fw} is selected for positive output current and sequence #2 D_{on} - D_{fw} - D_{off} for negative output current, the mode of operation can be divided into four modes, Mode 11 for Boost sequence #1, Mode 12 for Boost sequence #2, Mode 13 for Buck-Boost sequence #1 and Mode 14 for Buck-Boost sequence #2. Figure 2-19 shows how the mode of operation, Boost or Buck-Boost is determined by the input voltage (V_{in}) using a set-reset flip-flop and two comparators considering a hysteresis band between 35 V (VBO_{max}) and 32.5 V (VBB_{min}), which are common to the input voltage ranges of both Buck-Boost and Boost modes of

operation. The "4-input Multiplexer with two control inputs" sends the "mode of operation" (11, 12, 13 or 14) according to the control inputs 0 or 1 which are achieved from the values for signals BorBB (Boost = 0 and Buck-Boost = 1) as well as for Seq #1or #2, ($I_{ref} > 0$ (0) and $I_{ref} < 0$ (1)).

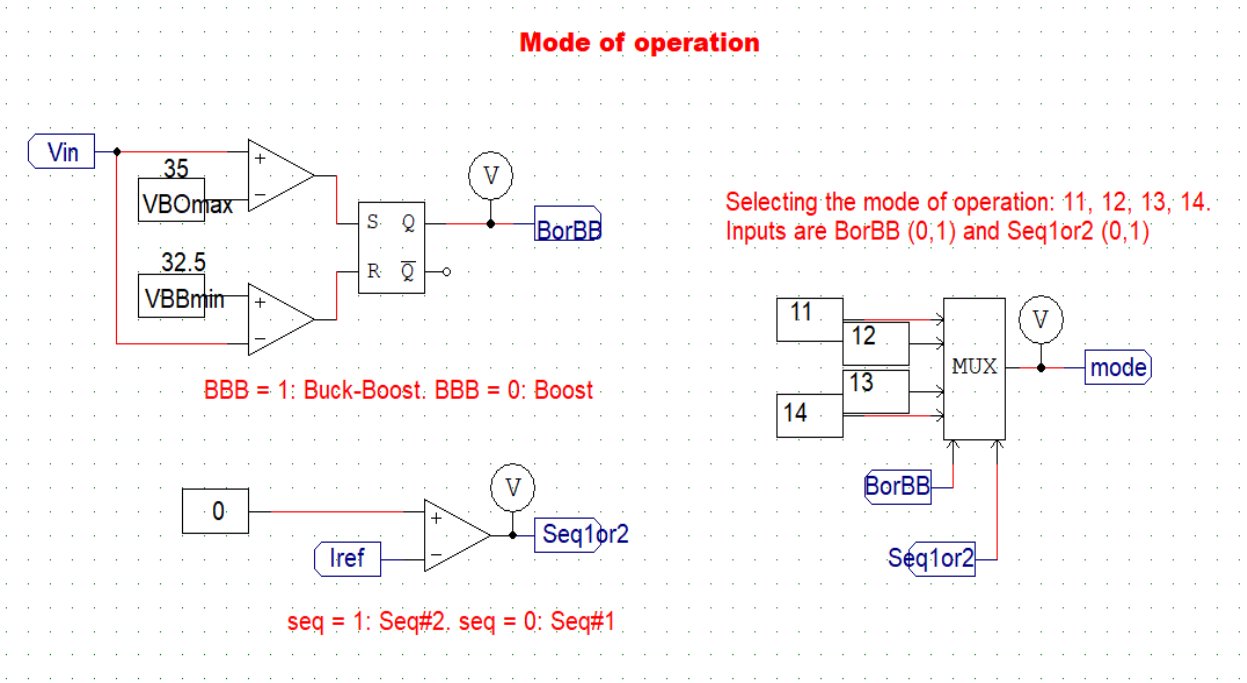

Figure 2- 19 Mode of operation

As two switches are ON at any given moment, there are four possible "states of operation." These can be defined, #1 is for S1 and S4 ON, #2 is for S2 and S4 ON, #3 is for S1 and S3 ON, #4 is for S2 and S3 ON. The definition of the states of operation is shown in Table 2.10. Recall that in the tri-state modulation scheme, there are an ON state, an OFF state and a free-wheeling state. The ON state is common to both Buck and Buck-Boost modes. The OFF state for the Buck-Boost mode (D_{offBB}) is different from that for the Boost mode (D_{offB}).

Table 2. 10 State of operation

State of operation #	Switches ON	Usage
1	S1 and S4 - (S_{14})	ON state for all modes of operation (D_{on})
2	S2 and S4 - (S_{24})	Free-wheeling state for all modes of operation (D_{fw})
3	S1 and S3 - (S_{13})	OFF state for the Boost mode of operation (D_{offB})
4	S2 and S3 - (S_{23})	OFF state for the Buck-Boost mode of operation (D_{offBB})

Therefore, the four "modes of operation" present the "sequences of states" shown in Table 2.11.

Table 2. 11 The sequences of states of the Mode of operation

Mode of operation	**Mode**	**Sequence of states – Duty cycles**	**Sequence of states – Switches**	**Sequence of states – States of operation**
11	Boost seq #1	$D_{on} - D_{offB} - D_{fw}$	$S_{14} - S_{13} - S_{24}$	1 – 3 – 2
12	Boost seq #2	$D_{on} - D_{fw} - D_{offB}$	$S_{14} - S_{24} - S_{13}$	1 – 2 – 3
13	Buck-Boost seq #1	$D_{on} - D_{offBB} - D_{fw}$	$S_{14} - S_{23} - S_{24}$	1 – 4 – 2
14	Buck-Boost seq #2	$D_{on} - D_{fw} - D_{offBB}$	$S_{14} - S_{24} - S_{23}$	1 – 2 – 4

The four modes of operation have different sequences of states in each period, as shown in Figure 2-20. One can see that the first "state of operation" of a switching period is always 1 (D_{on}) the second can be: 1) D_{off}, when $i_o > 0$ and one employs sequence #1 (signal *Seq1or2* = 0). This occurs for "Modes of operation" 11 and 13. Or 2) $D_{fw,}$ when $i_o < 0$ and one employs sequence #2 (signal *Seq1or2* = 1). This occurs for "Modes of operation" 12 and 14. In every period, the three states of operation look like a three-level signal, and each state of operation lasts T_{on} , T_{off} and T_{fw}. The *magnitude of each level* depends on the "number of the state." The duration of each state is: $T_{on} = D_{on}T_s$ (the value of the control parameter D_{on} is variable), $T_{off} = D_{off}T_s$ (D_{off} = 0.35) and $T_{fw} = T_s - T_{on} - T_{off}$ ($D_{fw} = 1 - D_{on} - D_{off}$).

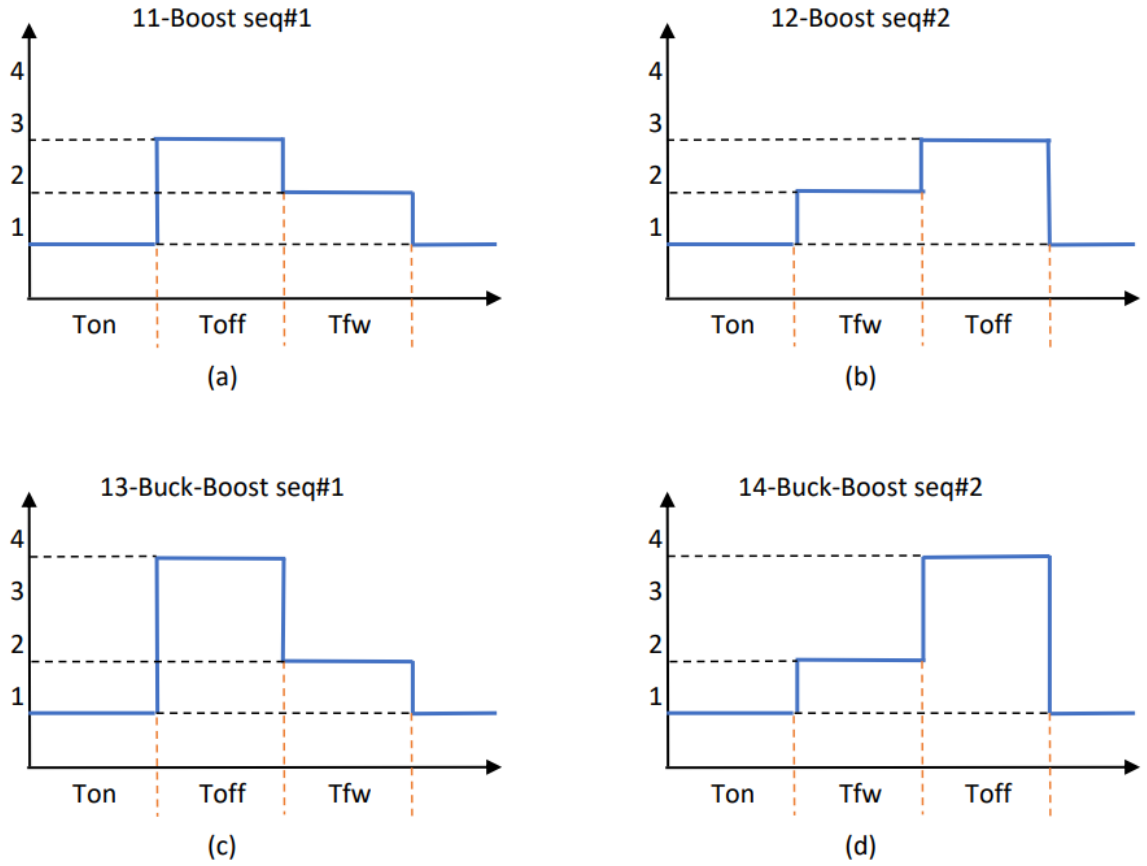

Figure 2- 20 Sequences of states of the 4 modes of operation a) 11-Boost seq #1, b) 12-Boost seq #2, c) 13-Buck-Boost seq #1, d) 14-Buck-Boost seq #2

A staircase signal with the three states of operation in tri-state Boost or Buck-Boost modes in every switching period, is shown in Figure 2-21. For the Pulse-Width Modulation (PWM), it employs a clock signal to start the first state in each period and two *outer timers* to start the internal two states.

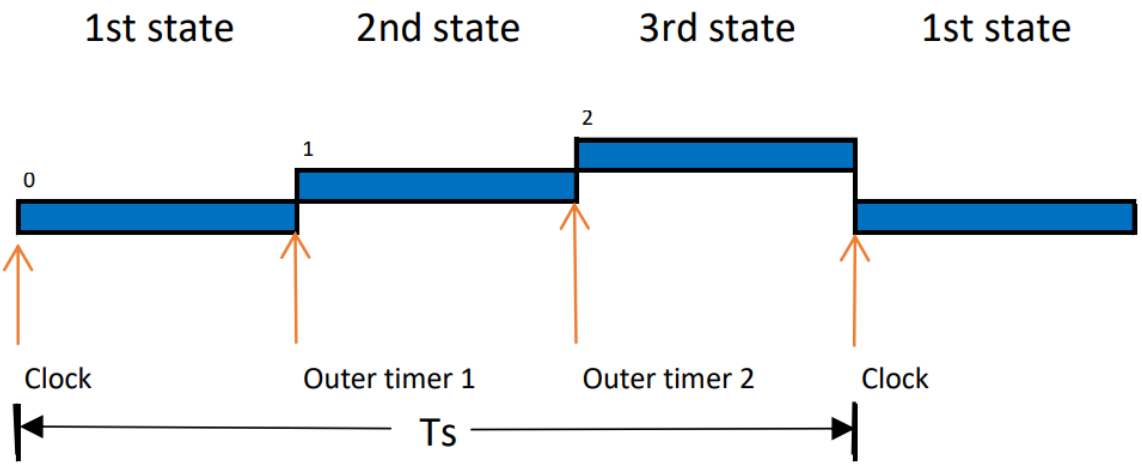

Figure 2- 21 Staircase signal in one period

The generation scheme of the Pulse-Width Modulation (PWM) is shown in Figure 2-22. It concerns essentially the duration of the three states of the sequence of states. The ramp carrier signal, with a peak value of 1V, is called *ramp*-1 and is created by the clock signal as the reset signal of an external resettable integrator. The clock signal is a square wave with a frequency of 50 kHz, and V_{peak} equaling 1. In the resettable integrator, the rising edge is set with "reset flag" = 0, the time constant is set as 1, the lower output limit is 0 and the upper output limit is 1. The input of the integrator is equal to the switching frequency (50 kHz).

The duration of the first "state of operation" of the "sequence of states" is obtained by comparing the D_{on} signal, in the inverting terminal/input, with the carrier *ramp*-1. This corresponds to a signal *outcomp1*. The duration of the second "state of operation" is obtained by comparing the delayed 7 µs (justified later) of the sum of the D_{on} signal added to either D_{off} or D_{fw}, in the inverting terminal, with the carrier (unity ramp). This depends on whether one is realizing a sequence #1 or #2, respectively. This corresponds to a signal *outcomp2*. The choice off adding either D_{off} or D_{fw}, to D_{on}, depends on the control input signal *Seq1or*2 of the 2-input multiplexer (MUX), whose possible control inputs are either 0 or 1. The complete staircase signal *pre_seq* is obtained by adding signals *outcomp1* and *outcomp2*, which will be used for creating signal *Sequence* required for obtaining the gating signals of S1 and S3. It should be noted that signal *pre_seq* concerns only the durations of the states in the sequence of states while signal *Sequence* also shows the number of the first, second and third state of the sequence of states, as shown in Figure 2-20.

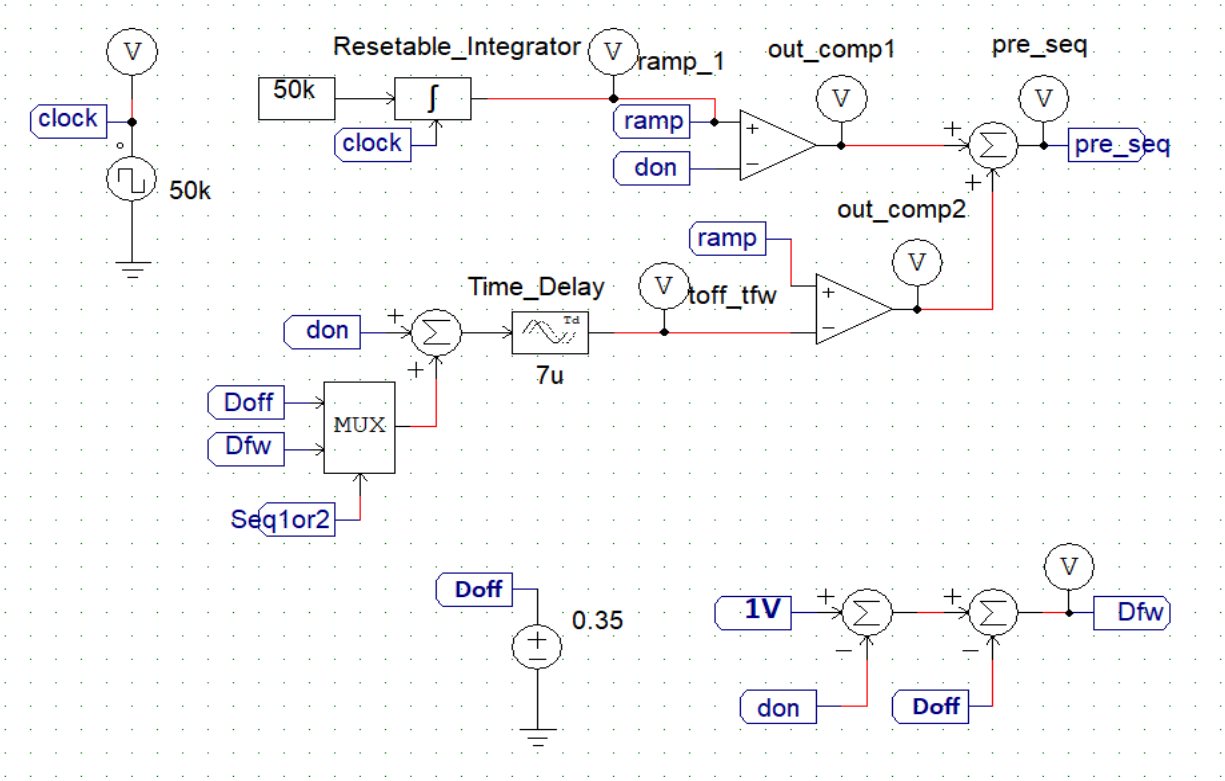

Figure 2- 22 Total three states of operation signal pre_seq

The 7 µs time delay is added considering that the value of D_{on} is not constant and might change in a switching period. Figure 2-23 illustrates the theory of 7 µs time delay usage. The switching frequency is 50 kHz, one-period time T_s is 20 µs. Considering that D_{off} is constant and equal to 0.35, T_{off} is 7 µs. When the value of the *Seq1or2* is 0, the MUX sends the value of D_{off} to add with D_{on}. One should make sure the value of the control signal ($D_{on1} + D_{off}$) that defines the duration of the second state is based on the value of the control signal D_{on1} used in the determination of the duration of the first state (the solid red curve), rather than the value of ($D_{on} + D_{off}$) (the blue dash curve). Therefore, the ($D_{on} + D_{off}$) signal needs to be delayed by T_{off} . Thus, one should use signal ($D_{on} + D_{off}$) delayed by 7 µs (the solid green curve). One should note that the time delay does not affect the PWM results when *Seq1or2* is 1, since it is D_{fw} to add with D_{on} that is (1- D_{off}), which is constant for the second state.

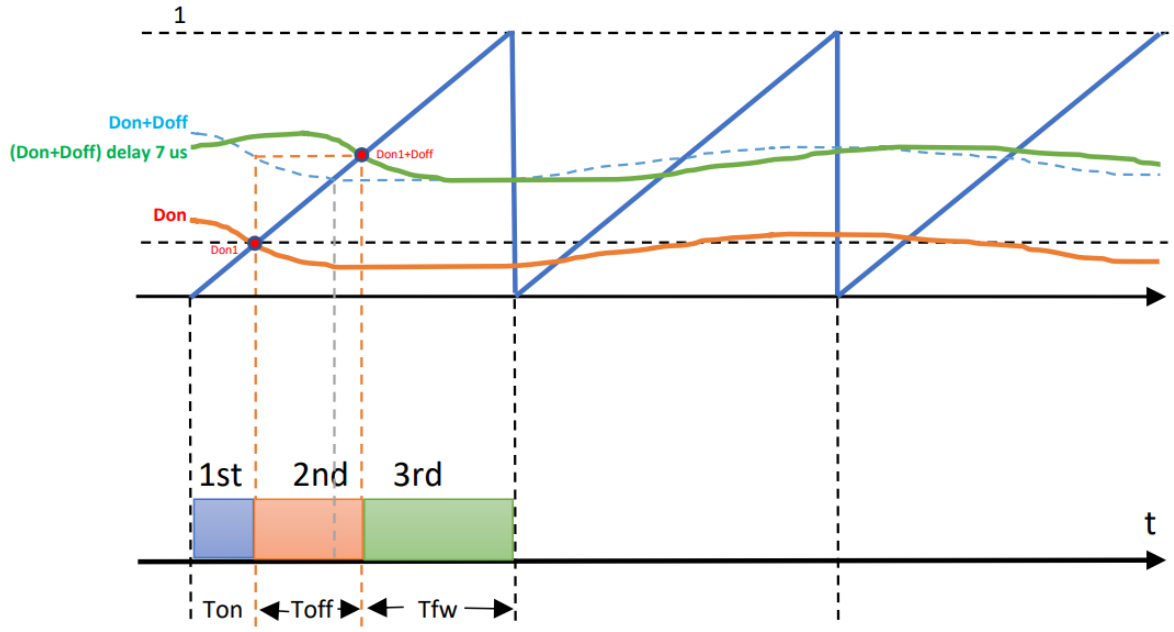

Figure 2- 23 Usage of 7 us time delay

Figure 2-24 illustrates the *Sequence* generation scheme. The actual "sequence of state", variable *Sequence*, presents the appropriate sequence of "states of operation," including the number and the duration of the state. Using a MUX with four inputs (possible states) with a control input which is signal *pre_seq* (D_{on}, D_{off} or D_{fw}, D_{fw} or D_{off}), a staircase with values 0, 1 and 2. One can see that the first "state of operation" is always 1, as shown in Table 8. The second and third states of operation depend on the "Mode of operation" which can have values 11, 12, 13 and 14. If one subtracts the value of variable "mode" by 11, one determines the control inputs (0, 1, 2 and else) of MUX1 and MUX2 with the number of the second and third states (2, 3 or 4) of that "*mode*" (11, 12, 13 or 14).

With the signal *Sequence*, the gating signals of switches S1 (G_{S1}) and S3 (G_{S3}) can be obtained considering the state of S1 and S3 at each of the four possible "states of operation" (1, 2, 3 and 4), by the subcircuit shown in Figure 2-25. The gating signals for S2 and S4 are complementary to S1 and S3, respectively. It is assumed that $G_{Sx} = 0$ for the switch OFF and = 1 for the switch ON. S1 is ON during D_{on} and D_{offB} and S3 is ON during D_{offB} and D_{offBB}. The gating signals subcircuit is implemented with a "MULTIPLEXER (4-input 1-control)", and the possible control inputs are (0, 1, 2 and else.). Since the values of the signal *Sequence* are 1, 2, 3 and 4, the control inputs of the

MUX are achieved by subtracting “1” from the values for the “states of operation” of signal *Sequence*.

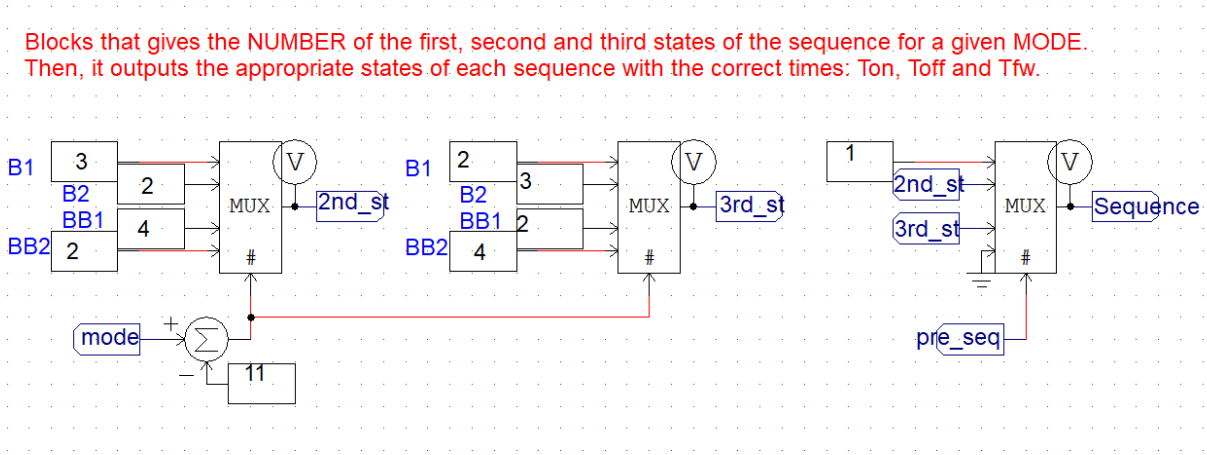

Figure 2- 24 Sequence generation scheme for gating signals

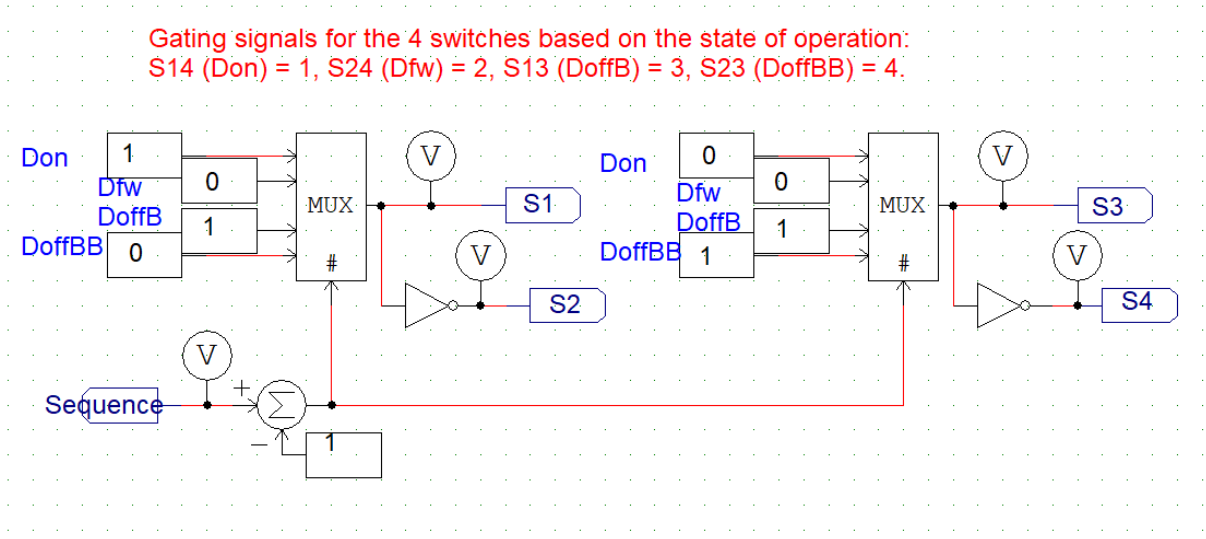

Figure 2- 25 Gating signals for the 4 switches

The final space vector modulation scheme is shown below in Figure 2-26.

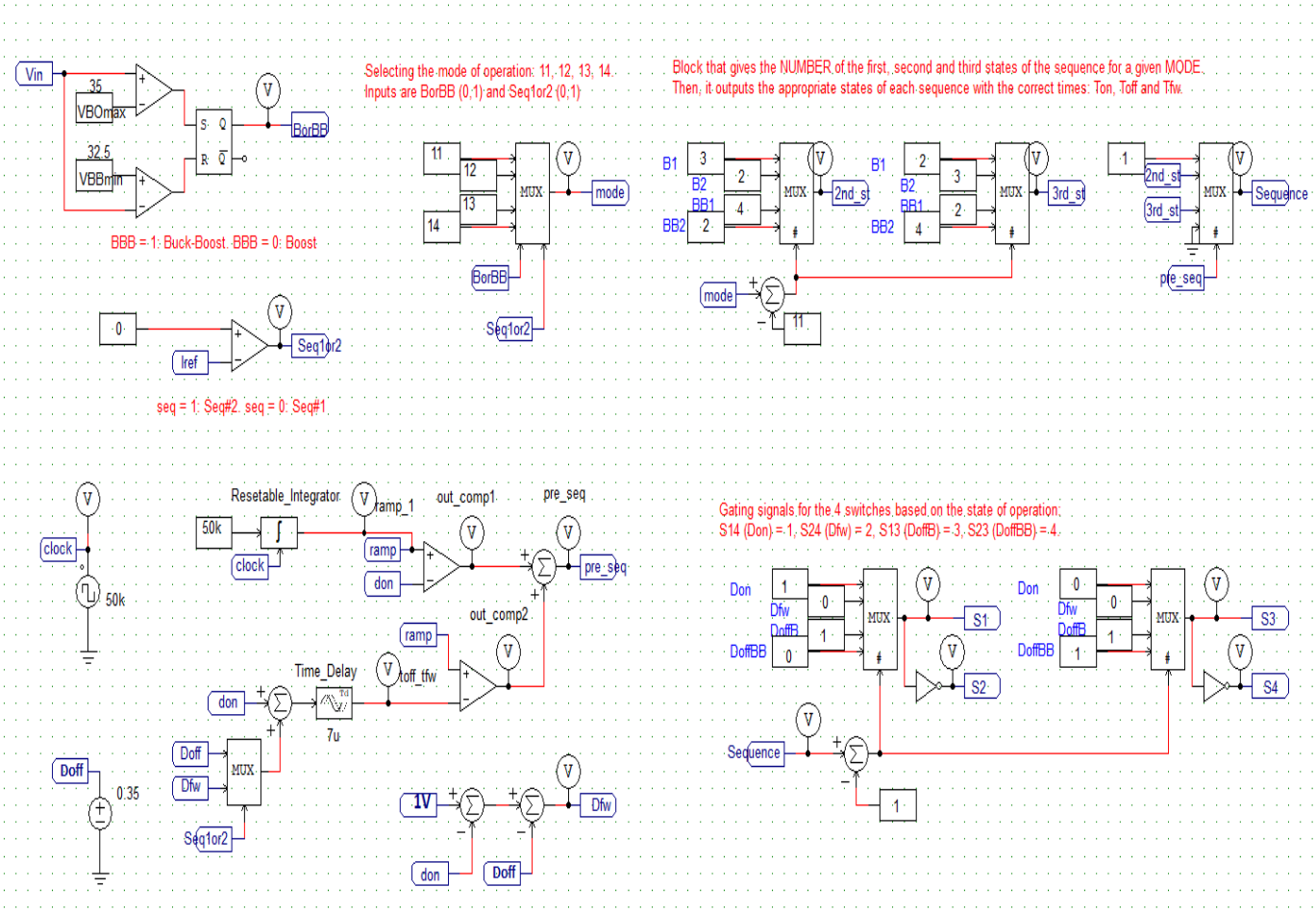

Figure 2- 26 Final space vector modulation scheme

2.5.2 Circuit scheme with tri-state logic

The simulation circuit scheme of the 4-switch bidirectional DC-DC converter and the single current control loop are shown in Figure 2-27. Parameters D_{off} = 0.35, L = 47 µH, C_{in} = C_o = 203 µF, R_f = 0.2 Ω, V_{dc} = 48 V and f_{sw} = 50 kHz.

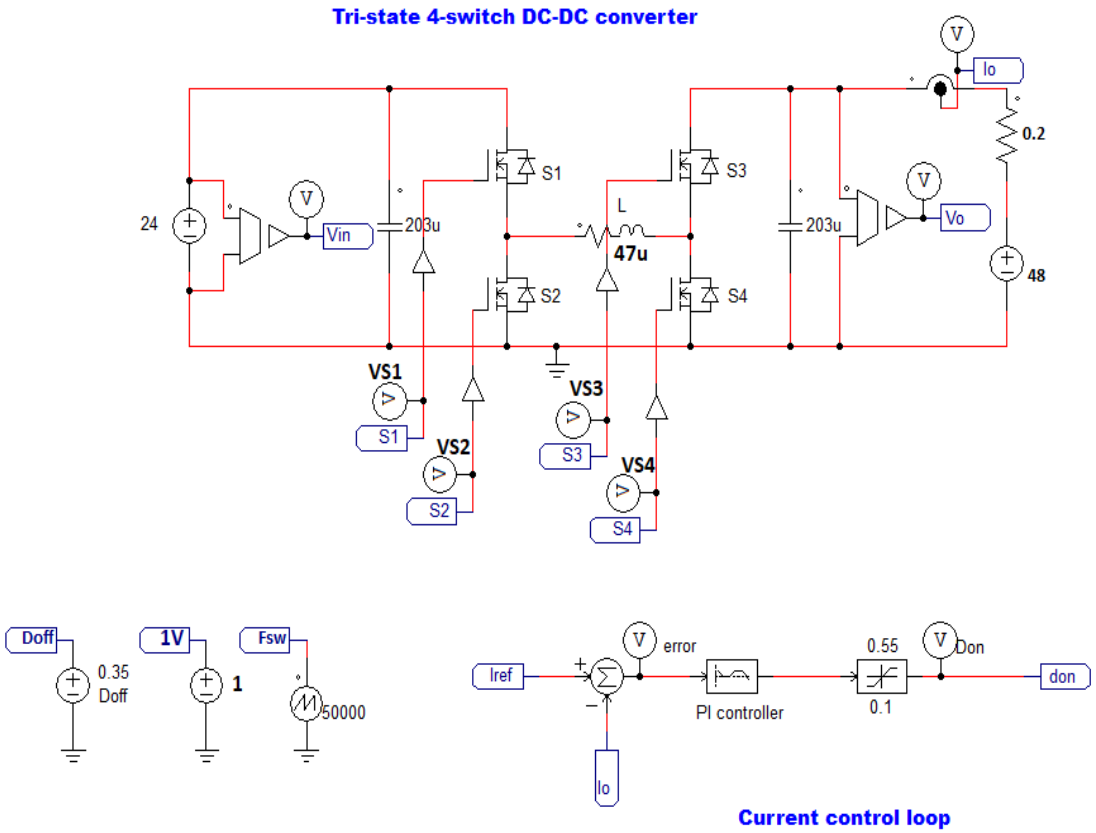

Figure 2- 27 Scheme of the converter and current control loop

2.5.3 Simulation scheme with tri-state logic in Boost and Buck-Boost modes

To validate the performance of the space vector modulation scheme and the converter operating with tri-state logic, using one type 3 PI controller (τ = 103.37 µs, T_P = 9.8 µs, and K_{PI} = 0.0435, designed with crossover frequency 5 kHz and phase margin 60°) for the output current loop with the single duty cycle control, two cases are tested in Boost mode and Buck-Boost mode, respectively.

For the Boost mode of operation, the input voltage is selected as 24 V ($D_{on} \approx 0.36$) for case 1 considering the worst case operating in Boost mode when the SC voltage varies from the half-rated voltage to the rated voltage. Figure 2-28 and Figure 2-29 show the performance of the space vector modulation scheme of case 1.

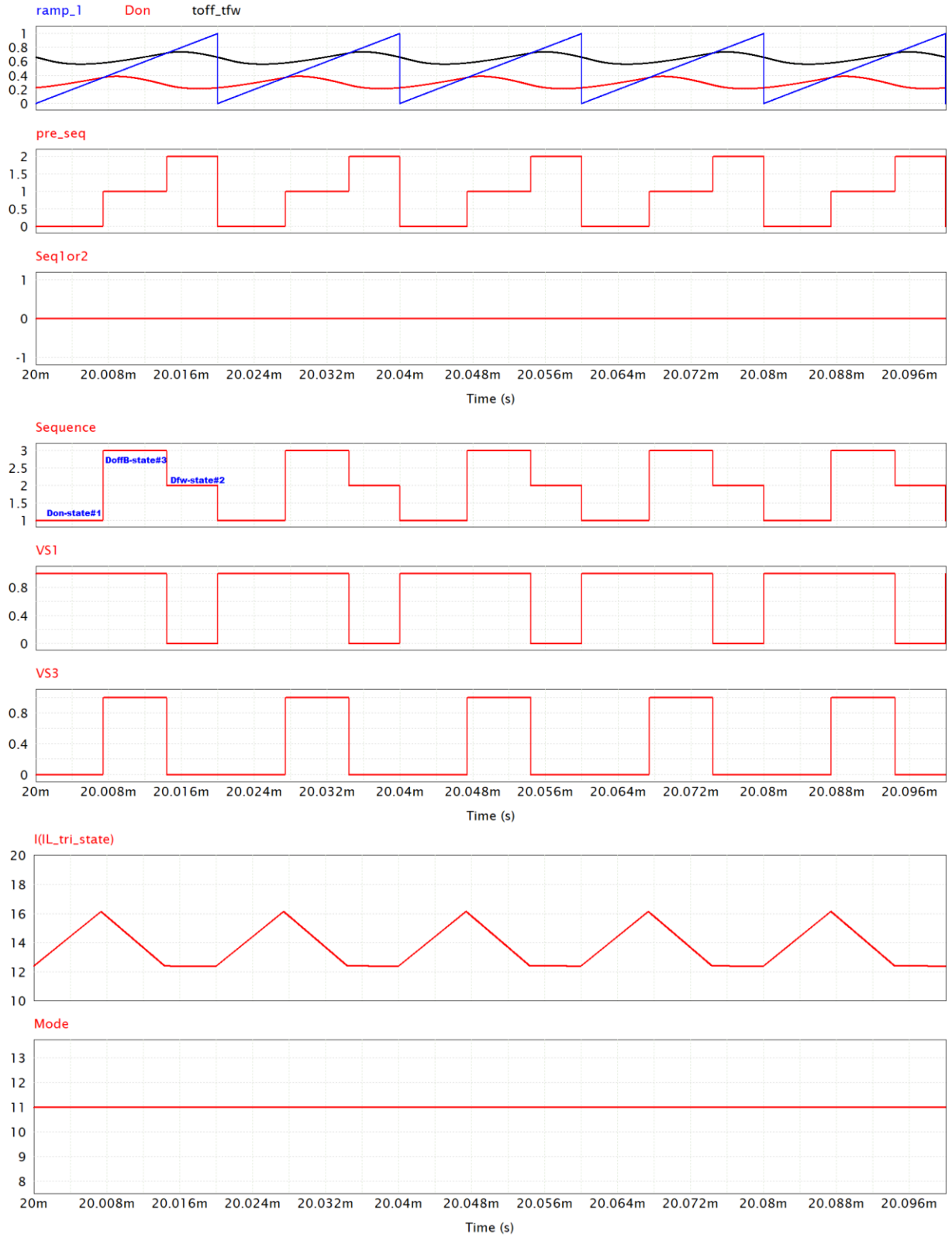

Figure 2- 28 a) PWM, with waveforms of ramp_1 (blue), Don (red), toff_tfw (black), pre_seq and Seq1or2; b) Sequences of the states of operation and gating signals for S1 and S3, c) Inductor current and Mode. (Case 1: V_{in} = 24 V, I_{ref} = 5 A)

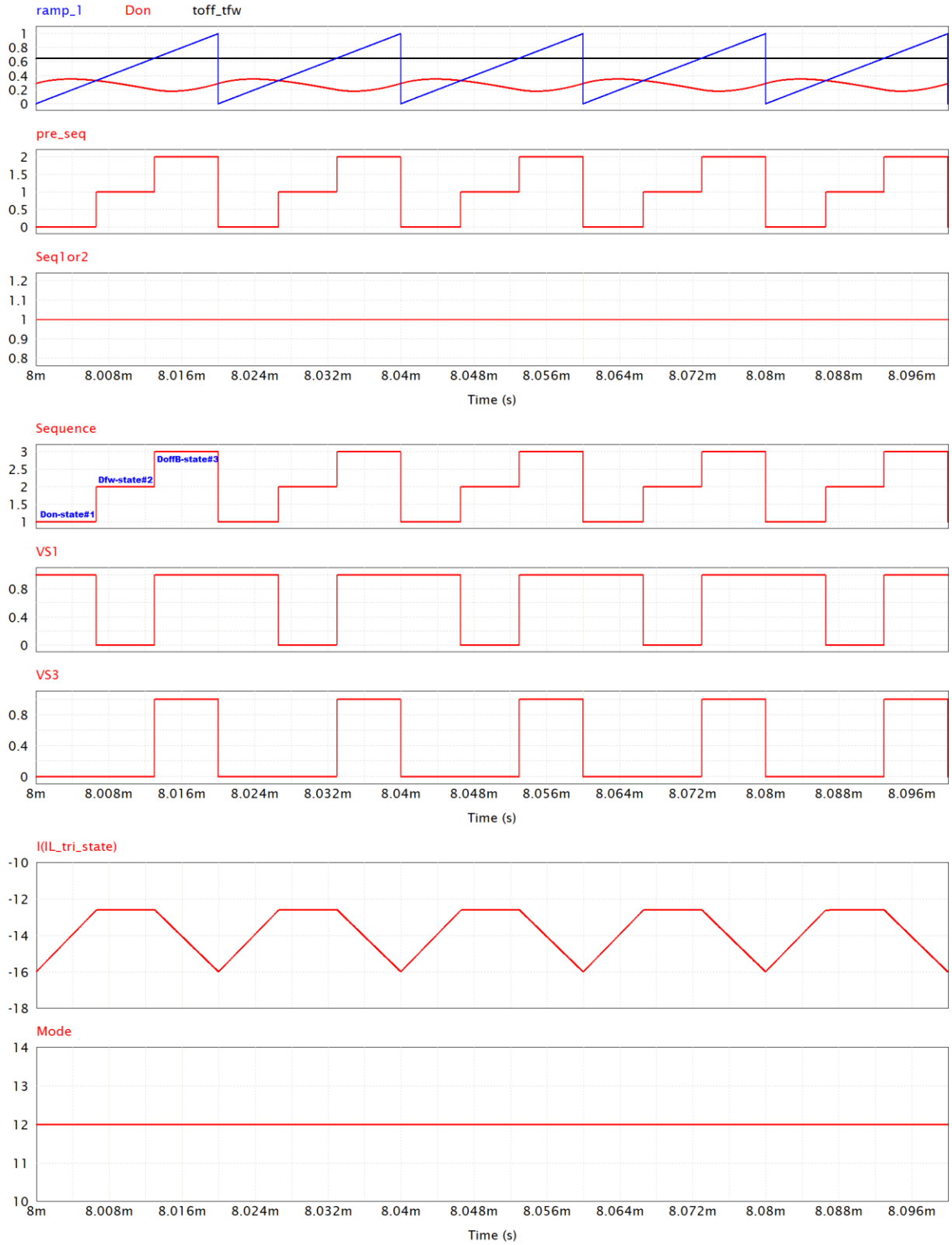

Figure 2- 29 a) PWM, with waveforms of ramp_1 (blue), Don (red), toff_tfw (black), pre_seq and Seq1or2 ; b) Sequences of the states of operation and gating signals for S1 and S3, c) Inductor current and Mode. (Case 1: V_{in} = 24 V, I_{ref} = -5 A)

In case 1, the value of V_{in} is 24 V, and the reference current is 5 A. The value of variable *mode* is 11, Boost - sequence #1, and the tri-state sequence is D_{on} - D_{off} - D_{fw}. One can see that the PWM in Figure 2-28 a), the values of *pre_seq* are 0, 1, 2 in every period, getting from D_{on} and $t_{off}\_t_{fw}$ compared with the *ramp*-1 signal, and the signal *Sequence* in Figure 2-28 b) shows the values 1-3-2 as defined in Table 2.11. With the desired modulation scheme, the waveform of the inductor current is as discussed in Figure 2-8. It increases with S_{14} ON during D_{on} and then decreases during D_{off} when S_{13} is ON, injecting the current into the grid, then keeps the same value during D_{fw} until the next cycle. Likewise, for case 2 with a negative output current (-5 A), Figure 2-29 shows the space vector modulation scheme of the mode 12, presenting the *Sequence* and the waveform of the inductor current as discussed before. Therefore, the space vector modulation scheme works as expected for the converter operating in Boost mode.

The waveform of signal $t_{off}\_t_{fw}$ used in the PWM generation, presents a ripple for case 1 in Figure 2-28 a) and is constant for case 2 in Figure 2-29 a). That is because in case 1, the value of $t_{off}\_t_{fw}$ equals to (D_{on} + D_{off}) for 5 A reference, so it changes when the value of D_{on} changes. Conversely, in case 2, the value of $t_{off}\_t_{fw}$ equals to (D_{on} + D_{fw}) for – 5 A reference, which equals to a constant value (1- D_{off}) with the fixed D_{off}, despite the values of D_{on} and D_{fw} change.

Figure 2-30 illustrates the performance of the designed control loop with simulation results of the main currents of case 1, with 24 V input voltage and 48 V for the DC bus. The 4-switch bidirectional DC-DC converter operates in Boost mode, to regulate the output current I_o at the value of 5 A. In the figure, one can see that the reference current varies in a step-like manner between 5 A and -5 A. The value of average output current is 5 A, and the actual value of the average inductor current is a little less than 14.3 A(5/0.35 A), about 13.75 A, that is because the ratio of $I_o/I_L = D_{off}$ is for the conventional dual-state modulation scheme, while for tri-state with constant D_{off}, the gain is a bit lower because the free-wheeling state takes place with the lowest inductor current magnitude (I_{Lmin}) in our application. The error is relatively small and will not be considered in this case. For the ratio I_o/I_L to be D_{off}, one should create an inductor current waveform that is trapezoidal with equal durations for the free-wheeling state at max and minimum currents. This is left as a suggestion for future work. The step-up and step-down transitions are also for testing the performance of the single current control loop and the stability of the system. The simulation results show that: with V_{in} = 24 V, I_{ref} = +/- 5 A, the output current waveform ($I_{out\_tri\_state}$) is regulated and follows the reference quite accurately in steady state. For positive I_{ref}, the converter

works in Mode 11 (Boost sequence #1) and for negative I_{ref}, the converter works in Mode 12 (Boost sequence #2), as set in the Mode of operation. For both the step-down and step-up transitions, the output current reaches the set point quickly, after around 0.26 ms and 0.25 ms, with a little overshoot, the output reaches the steady state very quickly.

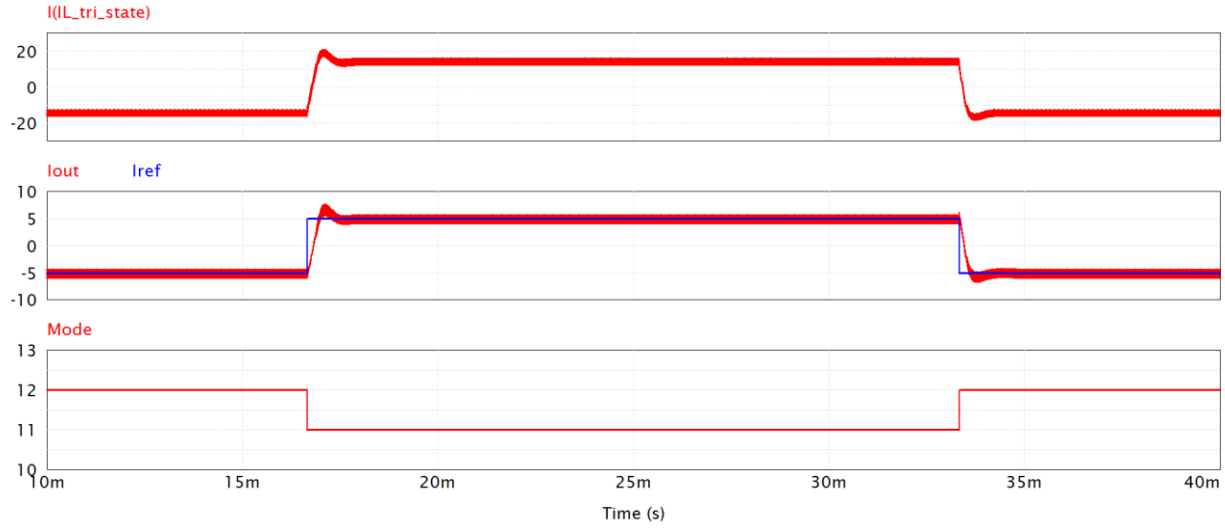

Figure 2- 30 Simulation results of the converter operating tri-state Boost mode (Vin=24 V)

Similarly, to test the Buck-Boost mode of operation, the input voltage is selected as 45 V(D_{on} ≈ 0.36) for case 2, coincidentally, with the same value of D_{on} as in the case 1 for the Boost mode.

Figure 2-31 and Figure 2-32 show the performance of the space vector modulation scheme of case 2. One can see that in Figure 2-31, with 45 V input voltage and 5 A reference current, the mode of operation is 13, and the tri-state sequence is D_{on} - D_{off} - D_{fw}. The PWM in Figure 2-31 a), the values of *pre_seq* are 0, 1, 2 in every period, getting from D_{on} and $t_{off}\_t_{fw}$ compared with the *ramp*-1 signal, and the signal *Sequence* in Figure 2-31 b) the *Sequence* shows the three-level signal with values 1-4-2 as shown Figure 2-21 and Table 2.11. With the desired modulation scheme, the waveform of the inductor current is as discussed in Figure 2-7 for Buck-Boost mode. Similarly, Figure 2-32 shows the signal *Sequence* and the waveform of the inductor current for the Boost mode and sequence #2, mode 14, where the tri-state sequence is D_{on} - D_{fw} - D_{off}. Thus, the space vector modulation scheme works very well for the converter operating in both Boost mode and Buck-Boost mode, with positive and negative output currents, sequences #1 and #2. The waveform of signal $t_{off}\_t_{fw}$ presents a ripple in case 1 in Figure 2-31 a) and keeps constant in case 2 in Figure 2-32 a) as discussed in Boost mode.

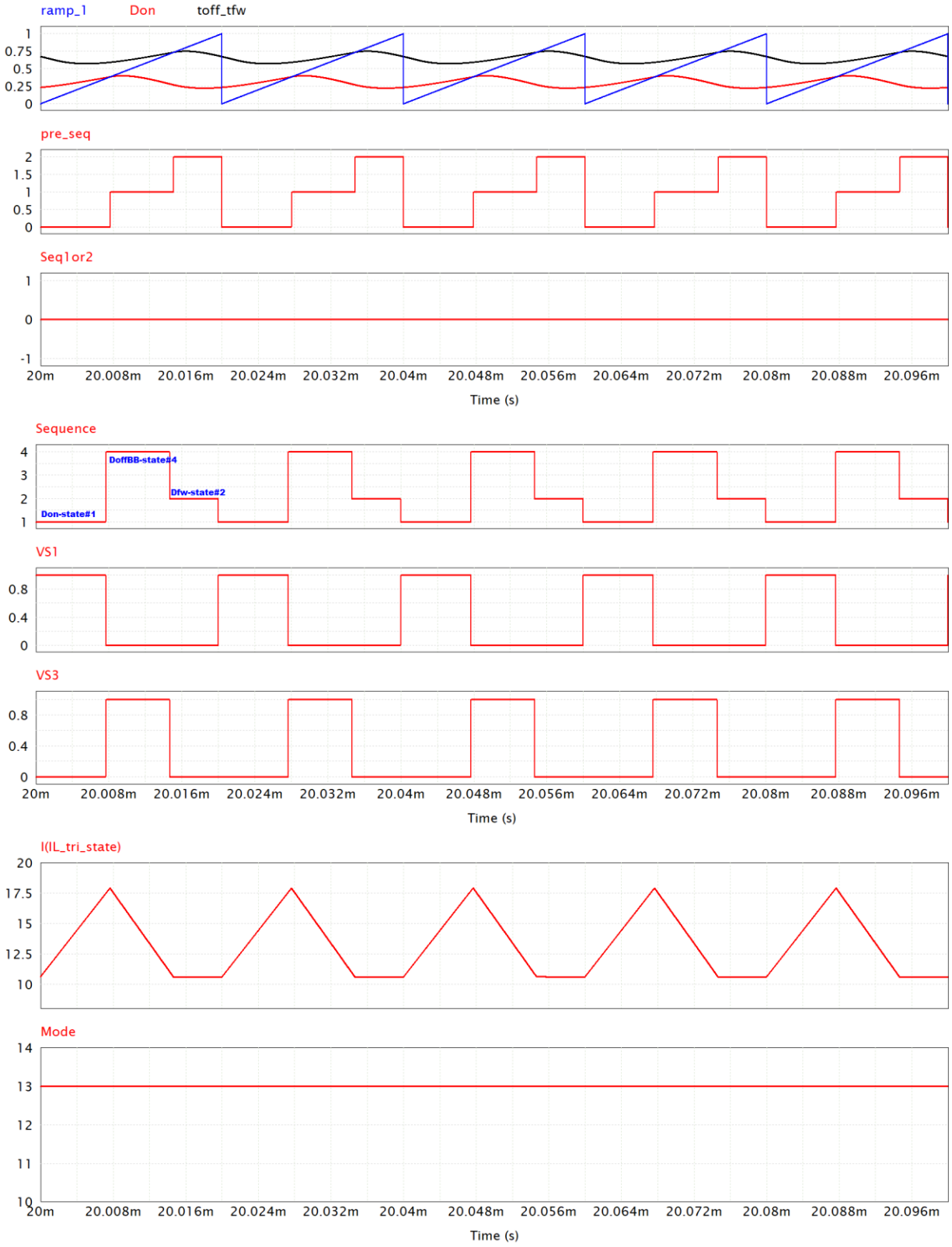

Figure 2- 31 a) PWM, with waveforms of ramp_1 (blue), Don (red), toff_tfw (black), pre_seq and Seq1or2 ; b) Sequences of the states of operation and gating signals for S1 and S3, c) Inductor current and Mode. (Case 2: Vin = 45 V, Iref = 5 A)

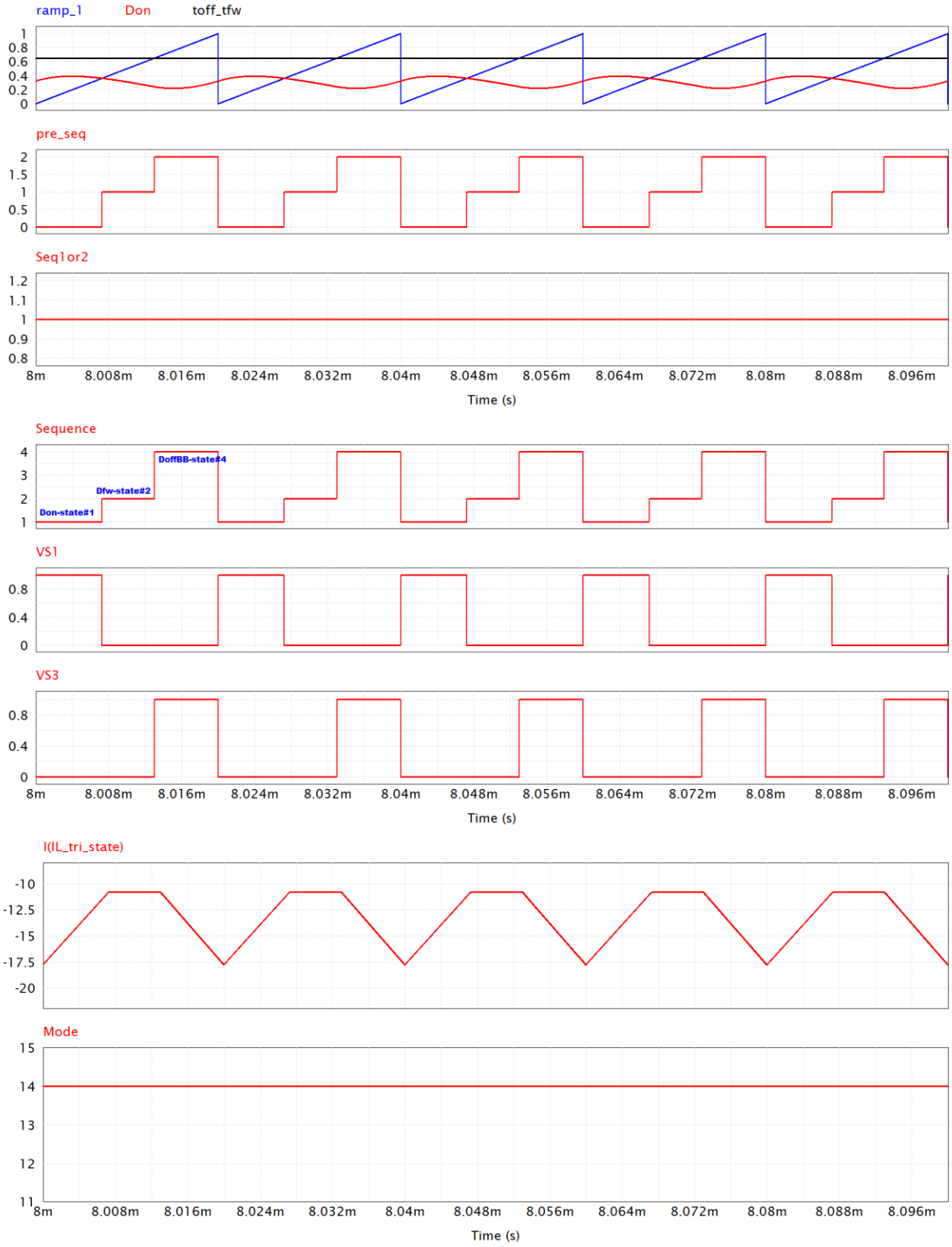

Figure 2- 32 a) PWM, with waveforms of ramp_1 (blue), Don (red), toff_tfw (black), pre_seq and Seq1or2 ; b) Sequences of the states of operation and gating signals for S1 and S3, c) Inductor current and Mode. (Case 2: Vin = 45 V, Iref = -5 A)

Figure 2-33 shows the simulation results of the output current ($I_{out\_tri\_state}$), inductor current $I(I_{L\_tri\_state})$ and signal *mode* when the converter operates with tri-state Buck-Boost mode with 45 V input voltage. Like the results of case 1 for Boost mode, the output current follows the reference quite well and it is regulated accurately at the value of 5 A for both positive and negative reference values (± 5 A). For positive I_{ref}, the converter works in Mode 13 (Buck-Boost sequence #1) and for negative I_{ref}, the converter works in Mode 14 (Buck-Boost sequence #2). At the step-down and step-up transitions, the output current responds quickly and reaches the steady state very fast. The rise time of the step-up transient response is around 0.17 ms and the rise time of the step-down transient response is around 0.16 ms. The step-down transient response of Buck-Boost mode is a little faster than the one of Boost mode. It is because the value of V_o during D_{off} state equals to V_L (D_{on}: $V_L = V_{in}$) in Buck-Boost mode, while it equals to (V_{in}-V_L) in Boost mode where during D_{on} state, $V_L = V_{in}$, the larger V_L leads to a larger inductor current and then I_o. Thus, the Buck-Boost mode would have a little faster transient response.

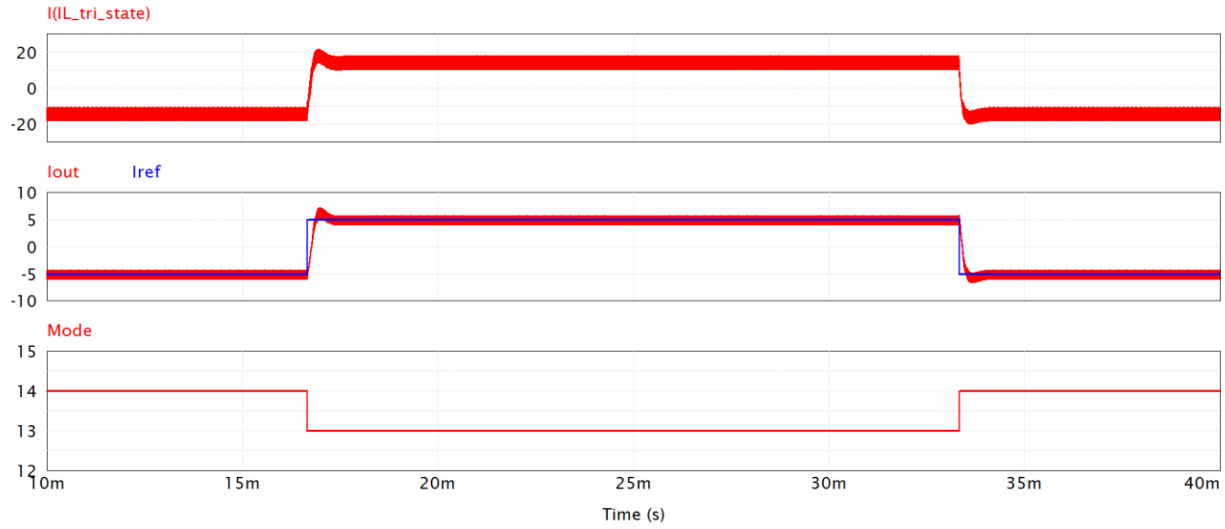

Figure 2- 33 Simulation results of the converter operating tri-state Buck-Boost mode (Vin=45 V)

For these two cases, with the same value of D_{on} ($D_{on} \approx 0.36$), the 4-switch bidirectional DC-DC converter can operate well in both Boost and Buck-Boost modes using the same designed type 3 PI controller with the single duty cycle control.

2.5.4 Comparison to conventional dual-state operation

A comparison of the transient response for the converter operating with tri-state and conventional dual-state is done for two cases. For the conventional dual-state control, cascaded control loops are used with a type 2 PI (τ = 119.71 µs, T_P = 8.46 µs, K_{PI} = 0.0276, designed with crossover frequency of 5 kHz and phase margin 60°) controller for the inner inductor current control. A type 2 PI (τ = 311.17 µs, T_P = 305.95 µs, K_{PI} = 3.1503, was designed with crossover frequency of 1 kHz and phase margin 85°) controller for the outer output current control. The simulation results of the converter operating with dual-state control along with those of the tri-state control in Boost mode and Buck-Boost mode are shown in Figure 2-34 and Figure 2-35, respectively.

The simulation results show the waveforms of the output current of tri-state ($I_{out\_tri\_state}$) in red color, the output current of dual-state ($I_{out\_dual\_state}$) in blue color and the reference (I_{ref}) in black color. In Figure 2-34, one can see that for V_{in} = 24 V and the tri-state converter operating in Boost mode, both $I_{out\_tri\_state}$ and $I_{out\_dual\_state}$ track the reference well, and the tri-state shows significant advantage in transient response. $I_{out\_tri\_state}$ rises faster by about 0.4 ms than $I_{out\_dual\_state}$ for both step-down and step-up transitions with acceptable overshoots. In Figure 2-35, for V_{in} = 45 V and the tri-state converter operating in Buck-Boost mode, $I_{out\_tri\_state}$ rises faster by about 0.34 ms at the step-up transition, and faster by about 0.24 ms at the step-down transition. Besides, the waveform of $I_{out\_tri\_state}$ reaches the steady state earlier than the waveform of $I_{out\_dual\_state}$.

The converter operating with tri-state logic uses one type 3 PI controller for the single duty cycle control loop while when working with the dual-state logic it uses cascaded control loops with an inner inductor current and outer output current loop for a total of two type 2 PI controllers. Recall that in such a case, the outer loop must be slower than the inner one. As a result, the tri-state schemes show faster response.

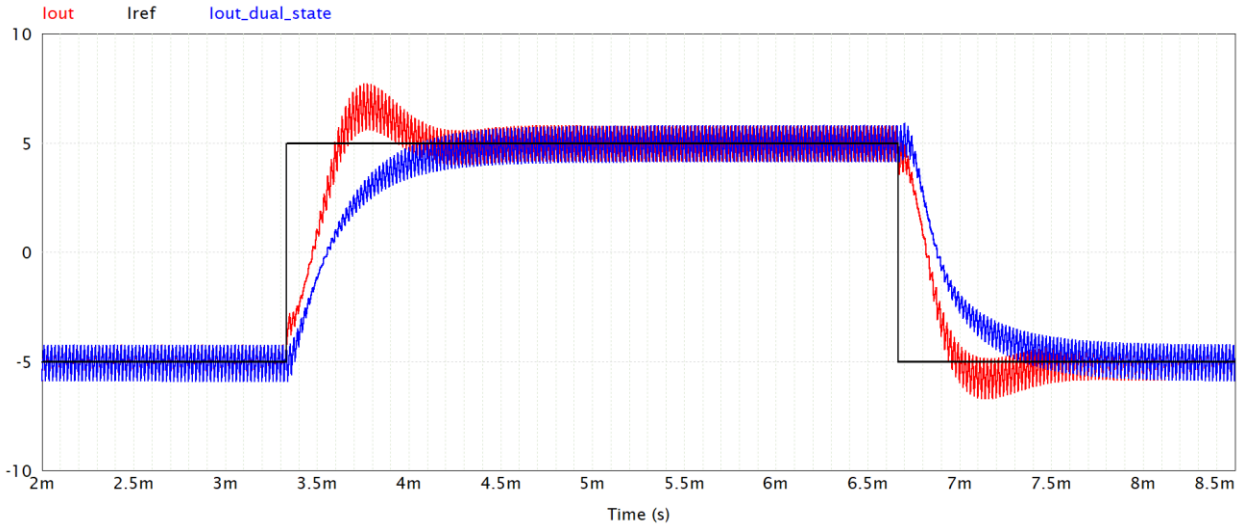

Figure 2- 34 Simulation results of the converter with tri-state and dual-state for case 1 (Vin = 24 V, Boost mode)

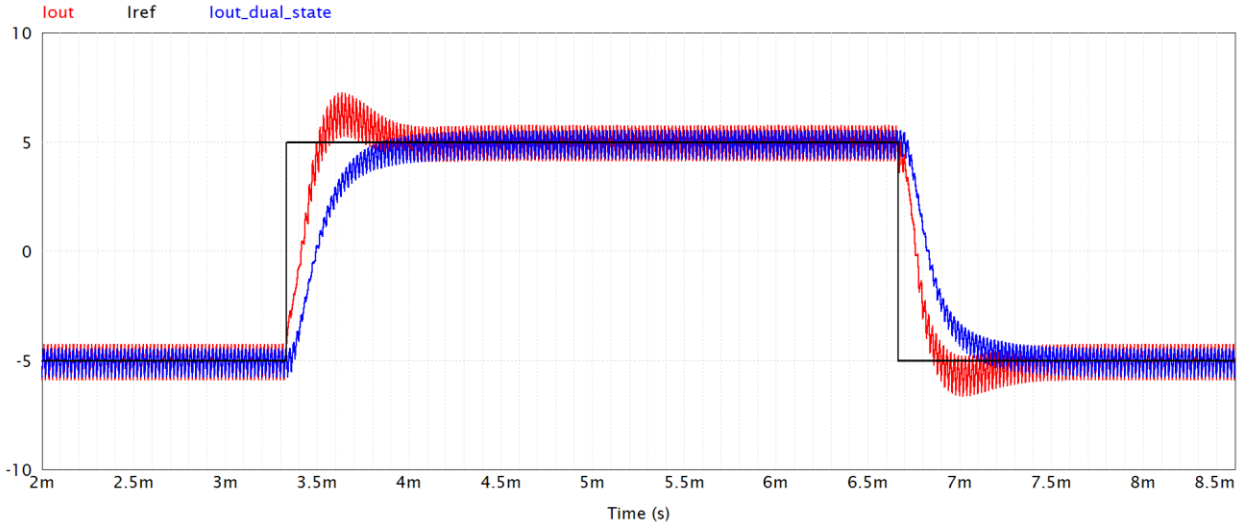

Figure 2- 35 Simulation results of the converter with tri-state and dual-state for case 2 (Vin = 45 V, Buck-Boost mode)

2.6 Summary

This Chapter discusses the implementation of the 4-switch bidirectional DC-DC converter with tri-state logic for interfacing a supercapacitor to a DC grid, operating with fixed D_{off} in both Boost mode and Buck-Boost mode. The selection of the fixed value of D_{off}, the intermediate inductor, capacitors, mode of operation and a single current control are presented. The design of the PI controllers for tri-state and conventional dual-state, to regulate the output current at the set value, are presented. The space vector modulation scheme is discussed and presented. Some tests are done to validate the performance of the converter operating with tri-state in Boost or Buck-Boost using the single duty cycle control, and comparisons with the converter operating in dual-state are also discussed. Since the 4-switch bidirectional DC-DC converter will be used to interface a SC to the DC grid, it should be able to operate knowing that in this case, the voltage of the SC varies between half rated to rated. With the limited voltage range for the tri-state Boost and Buck-Boost modes because of the fixed value of D_{off}, the mode needs to change between Boost and Buck-Boost mode. Thus, a smooth mode transition scheme between the Boost and Buck-Boost modes will be discussed and presented in Chapter 3.

Chapter 3 Transition between modes of operation

The converter is designed for interfacing the SC to the DC grid, while the voltage of the SC varies between 24 V to 48 V. In the conventional dual-state scheme, operation in the Buck-Boost mode would suffice. However, in the tri-state scheme, the converter needs to change between Boost and Buck-Boost mode because of the limited input voltage range caused by the fixed D_{off}. The effectiveness of the Boost mode of operation or Buck-Boost mode of operation has been verified in the last chapter. In this chapter, a smooth mode transition scheme will be discussed and validated by simulation, and an overvoltage and undervoltage protection logic is included to prevent the input energy storage device from over-charging and over-discharging.

3.1 Selection of mode of operation

The issue of the limited input voltage range of the SC for the converter operating with tri-state in Boost and Buck-Boost was presented in section 2.2.3. For $D_{off} = 0.35$, assuming $V_{dc} = 48$ V, the converter can operate in the Boost mode with the input voltage in the range from 24 V to 36.6 V. Likewise, the converter can operate in the Buck-Boost mode in the range from 31.2 V to 48 V. One can see that the converter cannot operate in only Boost mode or Buck-Boost mode while the SC voltage varies between 24 V and 48 V. Therefore, the converter needs to switch modes between Boost and Buck-Boost modes, within the two switchover points 35 V (VBO_{max}) and 32.5 V (VBB_{min}) which were shown previously in the Figure 2-19 mode of operation.

In principle, one could select an input voltage value, switchover point, between 31.2 and 36.6 V that would define the mode of operation. If the input voltage is lower than this value, the converter operates in the Boost mode. If it is higher, in the Buck-Boost mode. However, noise and variations in the output reference current could lead to frequent changes in the mode of operation which could degrade the performance of the converter. Therefore, a hysteresis-based scheme was employed to prevent this issue, with values equal to 32.5 V and 35 V. The mode transition logic also considers the current positive or negative to decide transition mode at 35 V or 32.5 V, because the charging/discharging of the SC with negative/positive currents leads to the increase/decrease of the SC voltage. 35 V is set as the switchover point from Boost mode to Buck-Boost mode, and 32.5 V is the switchover point from Buck-Boost mode to Boost mode. To illustrate the process of switching of modes, let's assume that the output current is 5 A, and the SC voltage (V_{in}) is relatively

high, the converter operates in Buck-Boost mode sequence #1 discharging the SC. Then, the input voltage decreases while the converter continues to inject current into the DC grid, when V_{in} is lower than 32.5 V, due to insufficient voltage gain, the converter will change to operate in Boost mode sequence #1 to avoid the risk of D_{on} saturation. For a negative output current of -5 A, assuming that V_{in} is low, at 24 V, and the converter operates in Boost mode sequence # 2. Since the SC is being charged, the input voltage will increase. When V_{in} becomes 35 V, the mode of operation will change to Buck-Boost mode sequence #2. The Figure 3-1 shows an illustration of the mode of operation considering the mode transition between Boost and Buck-Boost modes.

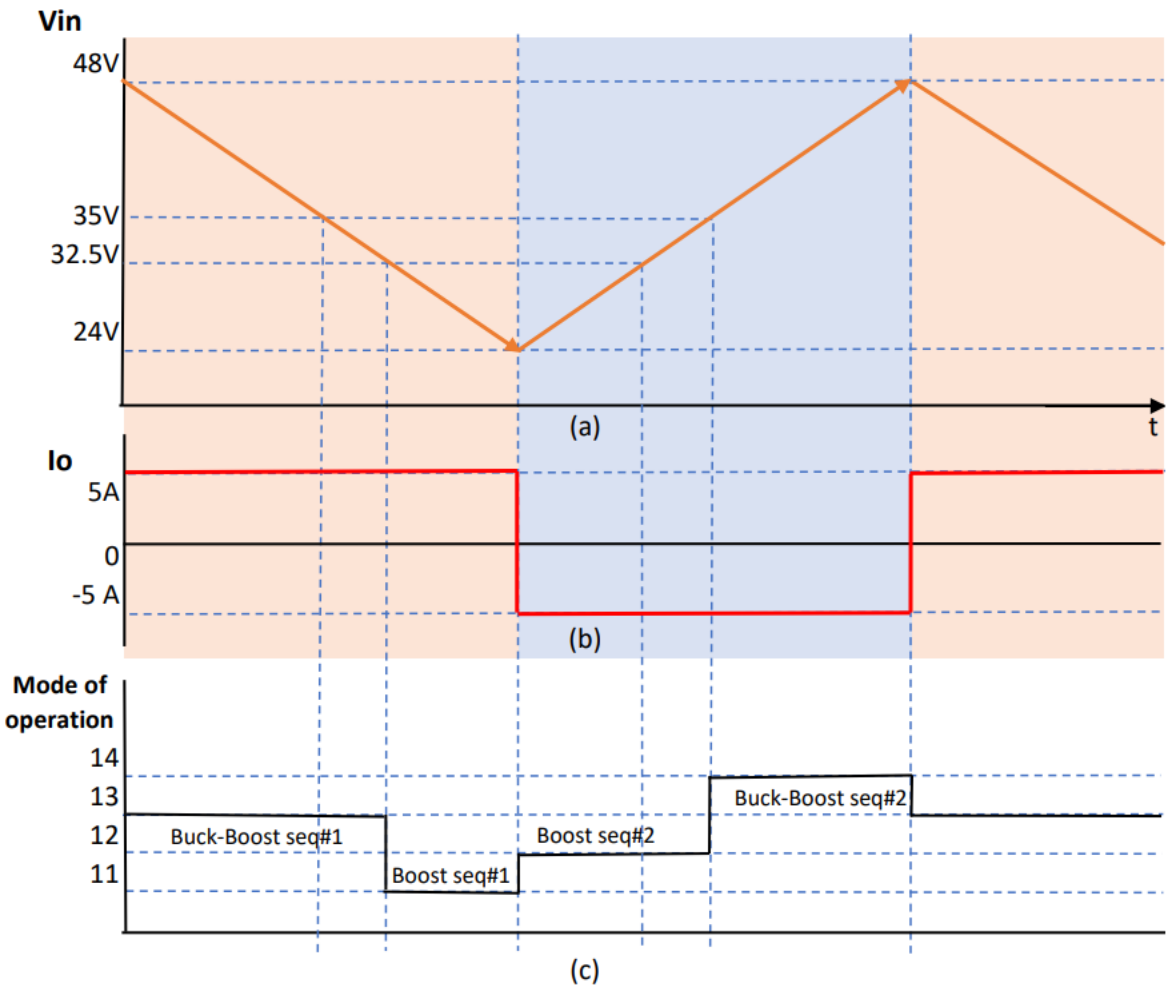

Figure 3- 1 Mode of operation considering the mode transition (a) Vin varies between 24 V to 48 V (b)Output current Io (C) mode of operation

3.2 A dynamic transition between modes of operation

The $i_o(s)/d\ (s)$ transfer functions of the 4-switch converter operating with tri-state and constant D_{off} in the Boost and Buck-Boost are identical, and the same PI controller is used for both modes of operation. However, as the output to input voltage gain (V_o/V_{in}) of Boost mode is different from the one of Buck-Boost mode with the same value of D_{on} coming from the PI controller, only changing the mode of operation of the converter when V_{in} comes to the two switchover points, can lead to undesired variations in the value of the output current. Therefore, a smooth mode transition logic is required.

In Figure 3-1, one sees that at the switchover points, only the mode of operation, that is, Boost or Buck-Boost mode changes. The sequence does not change considering the same direction of I_o. Thus, the effect of changing sequences is avoided here and the value of V_o ($V_o = I_oR_f + V_{dc}$) keeps the same at the switchover points for both modes. Therefore, the voltage gain of the Boost mode is the same as the voltage gain of the Buck-Boost mode when the mode changes. One can get the relationship between D_{onB} and D_{onBB} shown in equation (3-1) with the constant D_{off}.

$$Gain_{switchover\_points} = \frac{D_{onB}+D_{off}}{D_{off}} = \frac{D_{onBB}}{D_{off}} \qquad (3\text{-}1)$$

Therefore, a Mode Transition Block is added to the current control loop as shown in Figure 3-2. The output of the PI controller (*vopi*) is treated differently to get different values of D_{on} for different modes: D_{onB} is for Boost mode and D_{onBB} is for Buck-Boost mode, to reduce variations in the value of the output current and keep the voltage gain at the switchover points, this function logic is fulfilled by using "c code" in PSIM, for the verification by simulation.

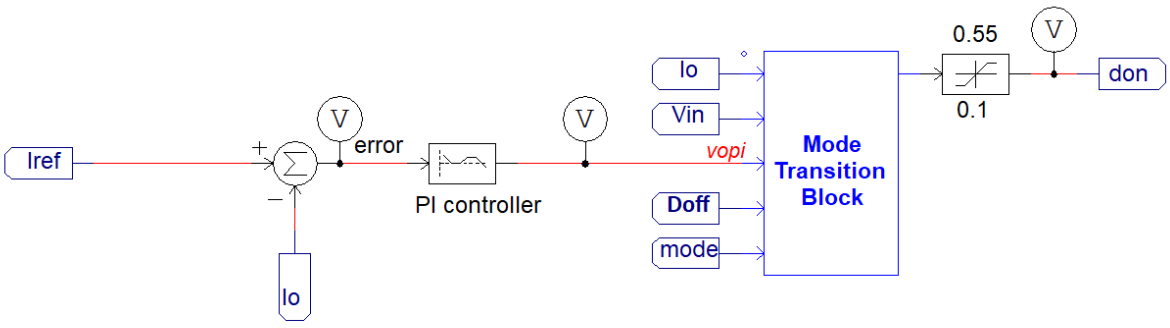

Figure 3- 2 Current control loop added with a Mode Transition Block

Considering the following case: V_{in} is "low", and the converter operates in Boost mode, with the SC absorbing the current from the DC grid. With the increasing of V_{in}, the mode of operation changes to Buck-Boost at the switchover point of 35 V. During the Boost mode, the output of the PI controller, *vopi*, corresponds to the value of D_{onB}. During the transition to Buck-Boost mode, assuming that the error in the absorbed current is zero, the value of *vopi* remains constant. Thus, D_{onB} needs to be changed to D_{onBB}. Based on the equation (3-1), to make sure that the voltage gain does not change, D_{off} is added to the output of the PI controller *vopi*, to obtain D_{onBB}. Likewise, when the mode of operation has to change from Buck-Boost to Boost at the value of 32.5 V input voltage, D_{off} should be subtracted from the output voltage of the PI, to obtain D_{onB}. Figure 3-3 shows the c code for this smooth mode transition logic, and Figure 3-4 shows the flow chart of the smooth mode transition logic.

```
x1: Io   x2: Vin   x3:  VoPI   x4: Doff   x5: mode
if (x1 < 0&& x5 ==14)    // If Io is negative and mode 14,
   {if(35<=x2<=48)    // if Vin is larger than 35 V and less than Vinmax 48V,
        y1=x3+x4;      // Don= VoPI + Doff.
    else                //   Else, Don=VoPI.
        y1=x3;}
else
{if (x1 > 0&& x5 ==11)   // If Io is positive and mode 11,
   {if(24<=x2<32.5)  // if Vin is lower than 32.5 V and higer than Vinmin 24V,
        y1=x3-x4;     // Don= VoPI – Doff.
    else               // Else, Don=VoPI.
         y1=x3;}
else                   //Else, Don=VoPI.
   y1=x3;}
```

Figure 3- 3 C code for smooth mode transition

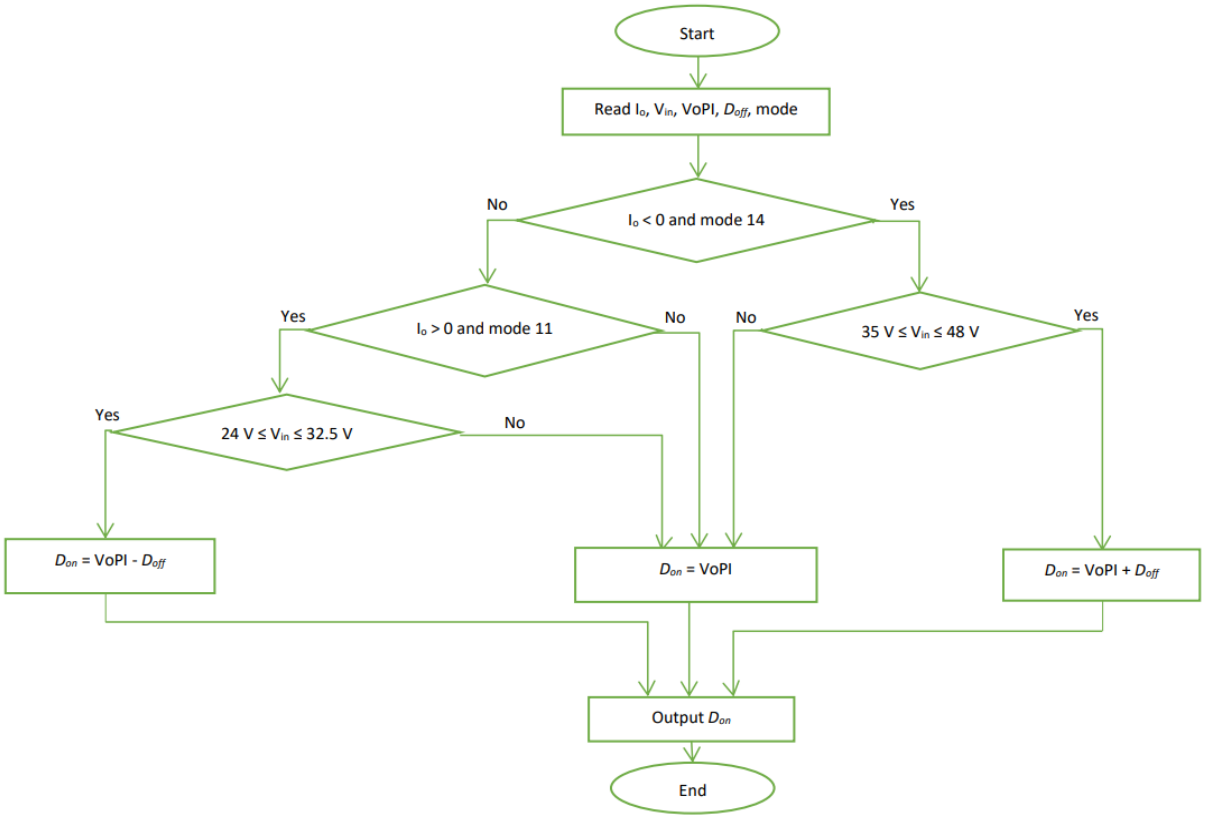

Figure 3- 4 Flow chart for smooth mode transition

3.3 Protection logic for SC voltage

To protect the supercapacitor, one should limit the current the interface injects/draws into/from the DC grid when the SC operates beyond the desired voltage range: 24 V to 48 V. Consider 24 V as the over-discharging limit and 48 V as the over-charging limit. Consider the case when the interface operates with a positive output reference current, and the SC voltage V_{in} decreases. When V_{in} is lower than 24 V, the protection logic works to change the reference current to 0 A to prevent the SC from over-discharging. Similarly, when the SC is charging, with a negative output reference current, when V_{in} is over 48 V, the protection logic prevents the SC from over-charging by changing the reference current to 0 A, as shown in Figure 3-5.

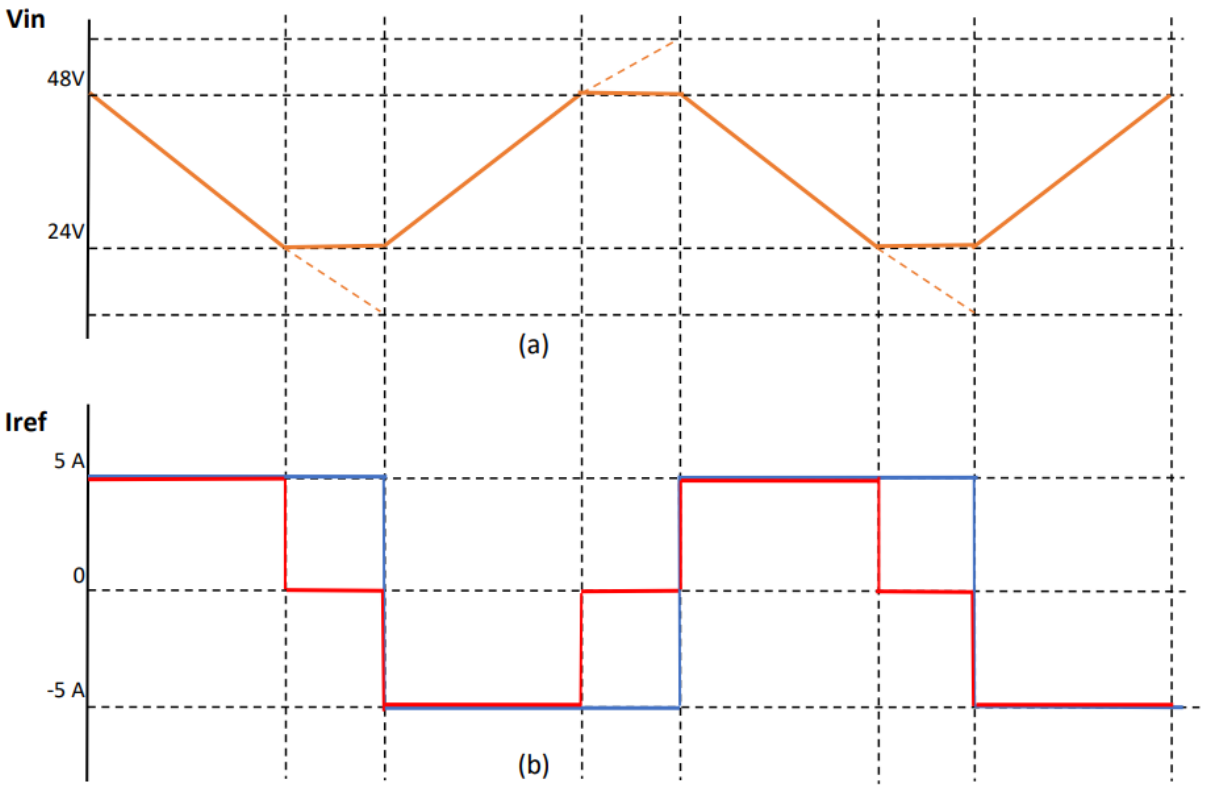

Figure 3- 5 Protection of SC from overcharging and over-discharging (a) V_{in} varies between 24 V to 48 V (b) Changes of Iref (Original Iref: in solid blue line; modified Iref: in solid red line)

Figure 3-6 illustrates the schematic diagram of the protection logic. Considering the small oscillation of V_{in} when keeping the output current at 0 A, the hysteresis is included for the two limit values. The *Iref_modulator* signal is then compared with the output current i_o. Finally, the complete output current control scheme can be shown in Figure 3-7.

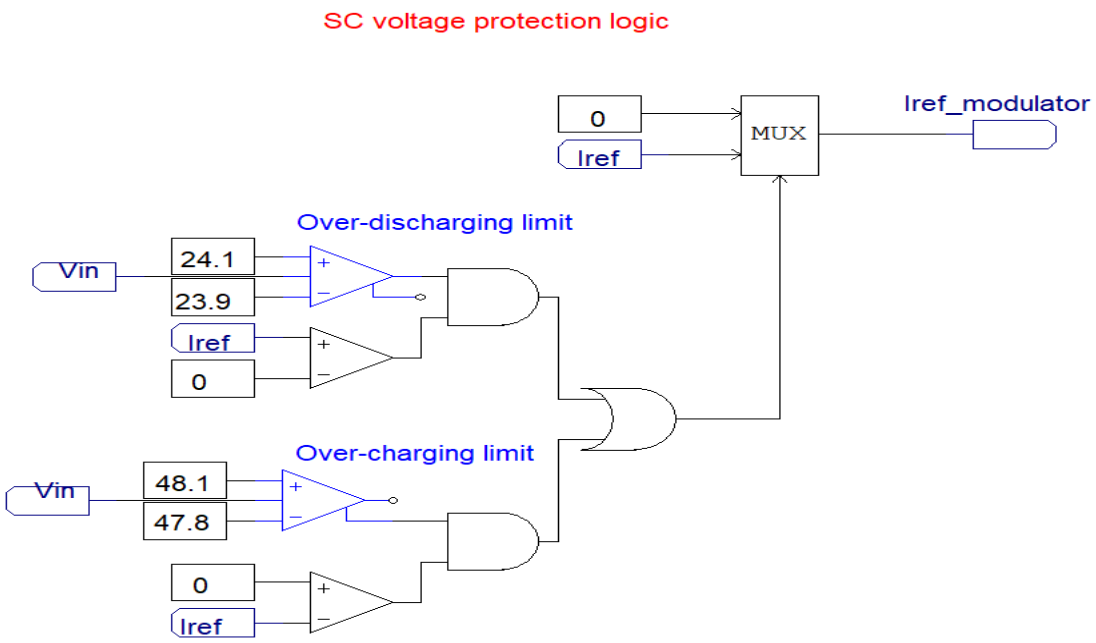

Figure 3- 6 The SC voltage protection logic.

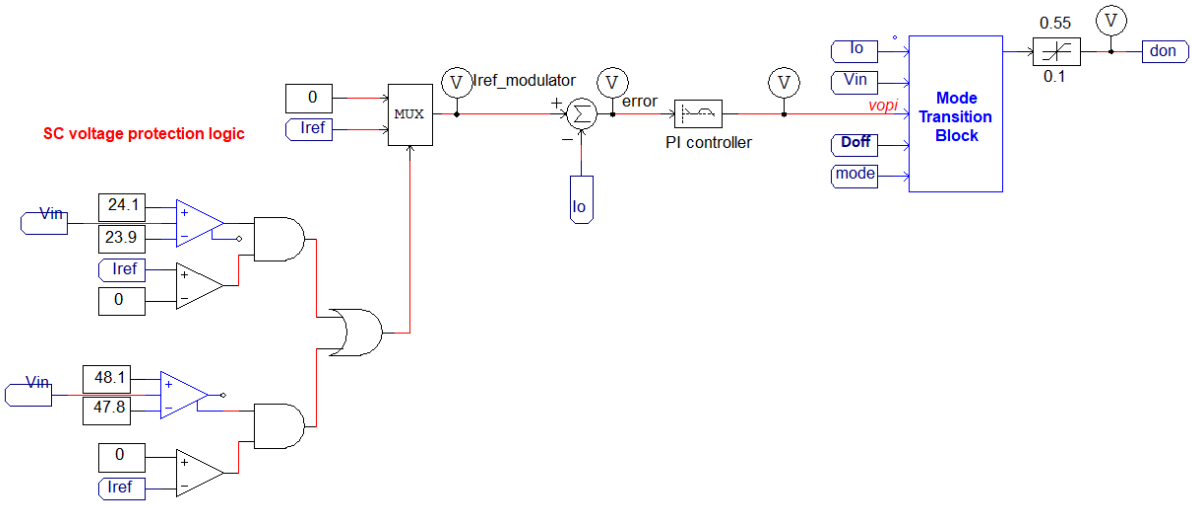

Figure 3- 7 Final current control loop with SC voltage protection logic and mode transition block

3.4 Simulation results

3.4.1 Final simulation scheme

The final simulation scheme is shown in Figure 3-8. It includes the 4-switch DC-DC converter, the current control loop with SC voltage protection logic, the mode transition block and finally,

the space vector modulation scheme that defines the mode of operation and generating gating signals for tri-state Boost and Buck-Boost operation.

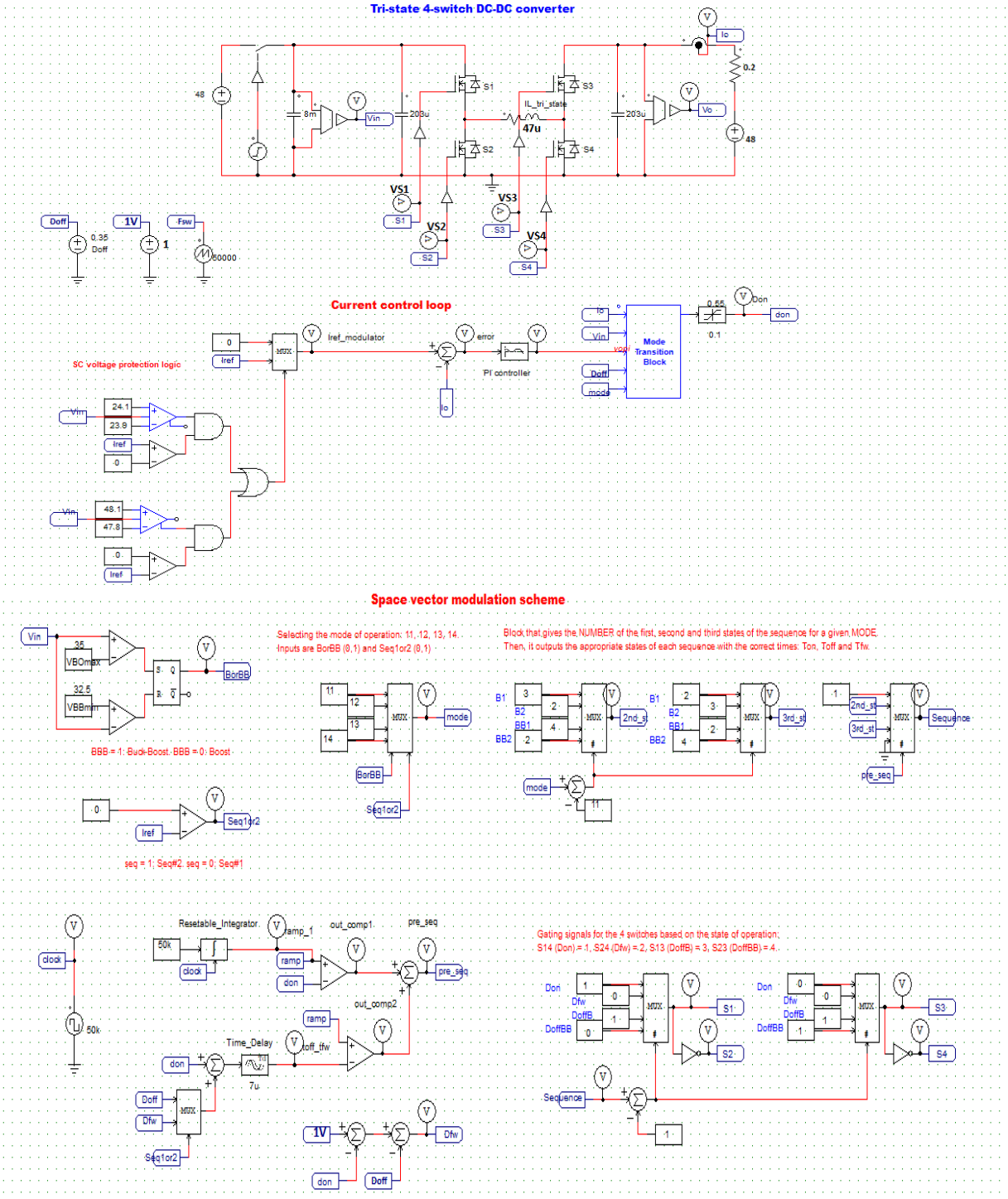

Figure 3- 8 Final simulation scheme

3.4.2 Simulation results with a fixed input voltage

To evaluate the smooth mode transition between modes, the converter first operates with a fixed input voltage (33 V) which is common to both Boost and Buck-Boost modes of operation. The mode of operation is set to change between Mode 13 and Mode 11 for a constant reference output current of 5 A. Then, between Mode 14 and Mode 12 for a constant reference output current of -5 A.

Figure 3-9 shows the simulation results for a reference output current of 5 A, the mode is set to change from Mode 13 to Mode 11 and then back to Mode 13. There one can see that with the smooth mode transition logic, the variations in the injected current due to changes in the mode of operation of the converter are very small, as opposed to the waveform of the output current without the logic which shows significant variations when the mode changes. Similarly, in Figure 3-10, the simulation results for the reference output current at -5 A and the mode is set to change from Mode 14 to Mode 12 and then to Mode 14, shows that the smooth mode transition logic leads to better and improved performance.

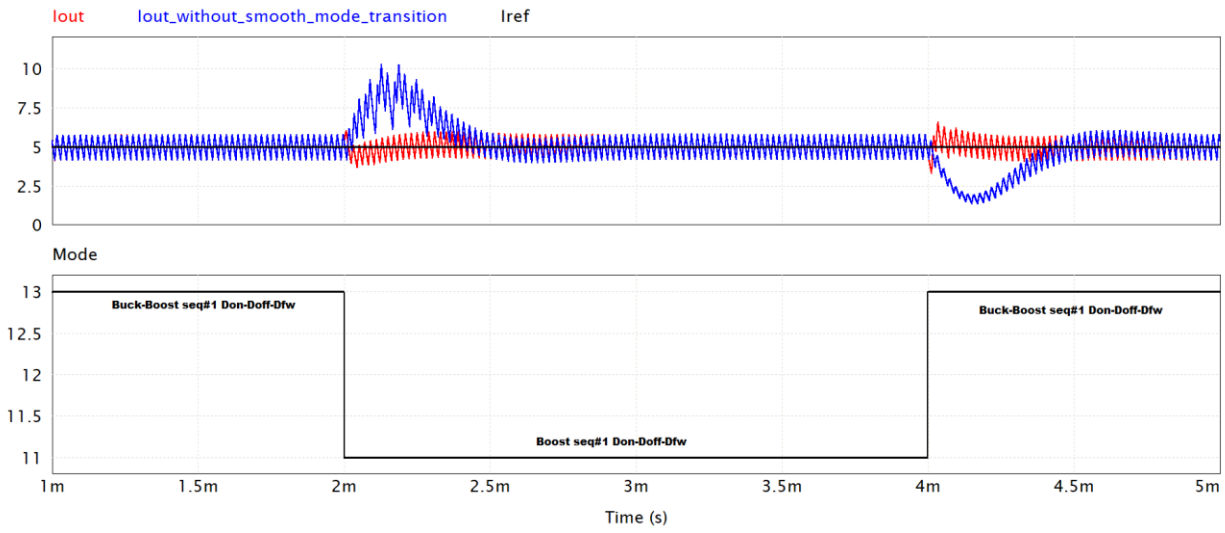

Figure 3- 9 Change of mode of operation: Boost to Buck-Boost to Boost for Iref = 5 A and Vin = 33 V. Without a smooth mode transition (blue curve) and with a smooth mode transition (red curve).

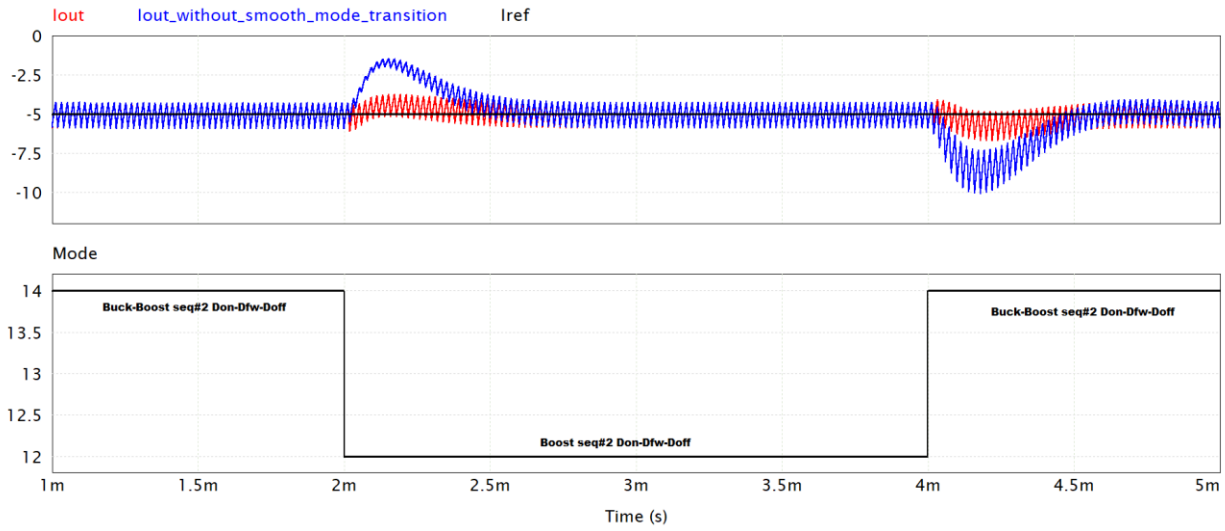

Figure 3- 10 Change of mode of operation: Buck-Boost to Boost to Buck-Boost for Iref = -5 A and Vin = 33 V. Without a smooth mode transition (blue curve) and with a smooth mode transition (red curve).

3.4.3 Simulation results as the input voltage varies

As the input voltage varies in a wide range, (24 V to 48 V), due to the power injected into the DC grid by the SC interface, a test with a 8 mF capacitor as SC is conducted to validate the smooth mode transition logic and the single PI controller and duty cycle adjustment control scheme.

In principle, the converter operating in the Buck-Boost mode should suffice. However, with tri-state logic and the constant D_{off}, the limitation of the value of D_{on} leads to a narrow input voltage range if the converter only operates in the Buck-Boost mode. Figure 3-11 shows the performance of the converter operating only in the tri-state Buck-Boost mode with constant D_{off}. There one sees that the converter can no longer track the reference output current, a square wave varying from -5 to 5 A with 17 Hz frequency and 0.5 duty cycle (Figure 3-11 a), when the input voltage falls below a certain value, about 30 V (Figure 3-11 b). This is because of the maximum limit of the value of D_{on} (Figure 3-11 d).

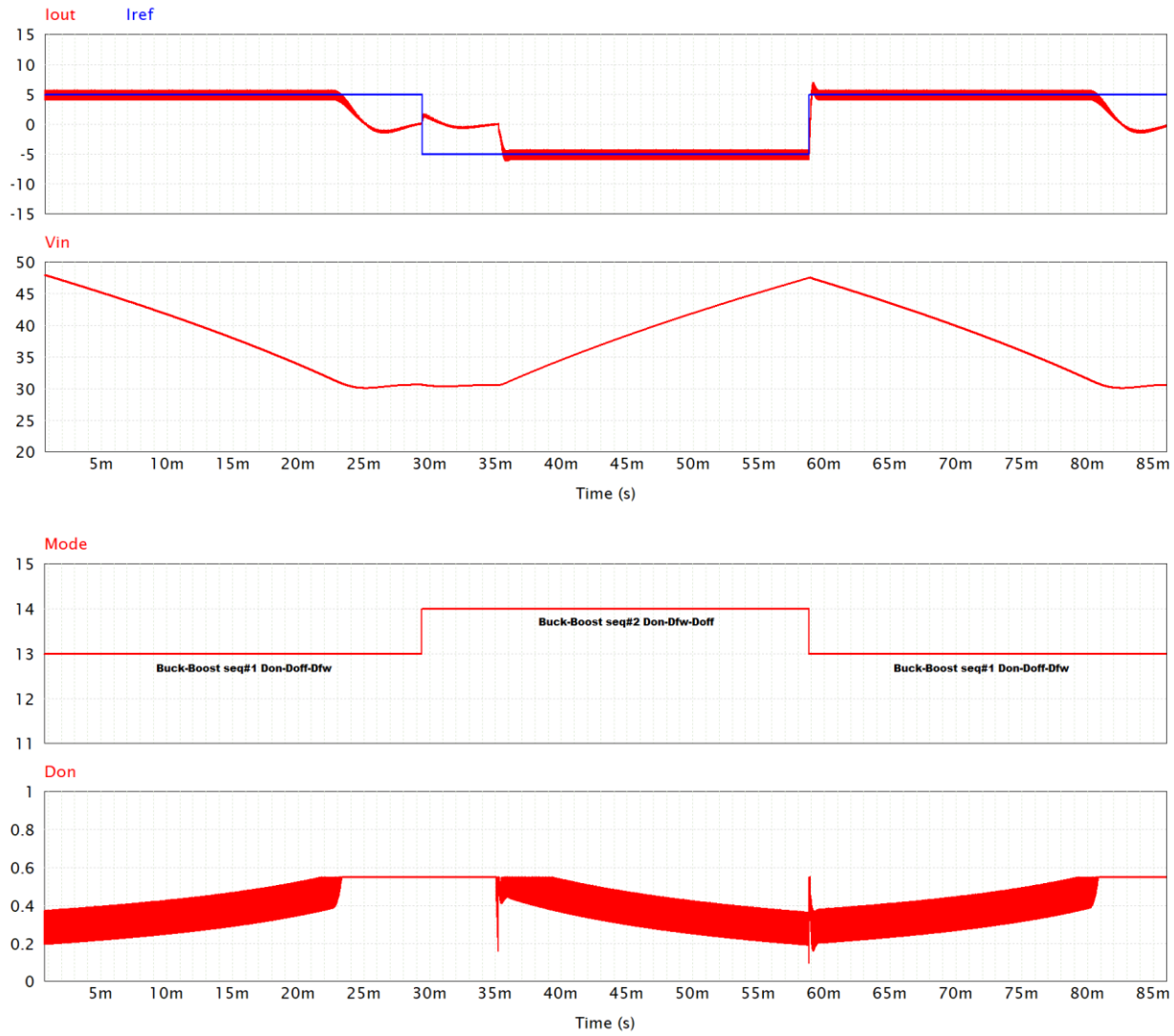

Figure 3- 11 a) Reference (blue) and actual output current (red), b) Input/supercapacitor voltage, c) Mode of operation, d) Don.

Figure 3-12 shows the converter operating in both Boost and Buck-Boost modes with the automatic mode transition. The reference output current I_{ref} is the same as before. One can see that the actual output current I_{out} tracks the reference very well and performs very quickly transient response. The rise time of step-down transition is around 0.25 ms and about 0.2 ms for step-up transition (Figure 3-12 a), and both step-down and step-up transitions reach steady state very quickly. The voltage of the supercapacitor varies between 48 V and 24 V as expected for this type of application in Figure 3-12 b). Finally, one can see in Figure 3-12 c) and d), the output of the type 3 PI controller and the signal that is used as D_{on} to the PWM modulator, depending on the mode of operation of the converter: Boost or Buck-Boost. Figure 3-12 d) illustrates how the smooth

mode transition scheme works: When a transition from Buck-Boost to Boost occurs, D_{on} is increased by D_{off} and when the transition is from Boost to Buck-Boost, D_{on} is decreased by D_{off} .With the smooth mode transition scheme, the output current presents minor transients seen in the top waveform when a mode transition occurs.

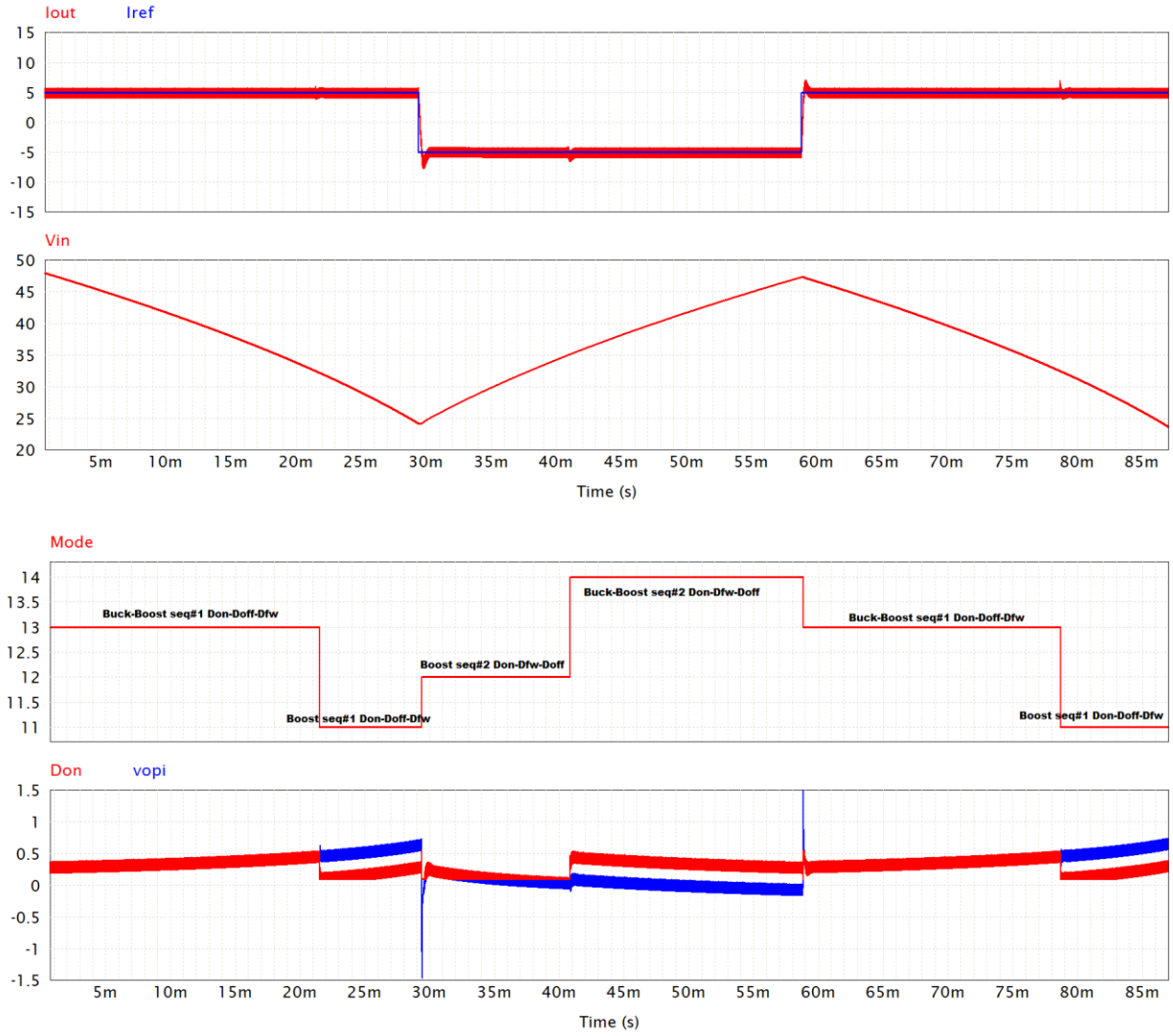

Figure 3- 12 a) Reference (blue) and actual output current (red), b) Input/supercapacitor voltage, c) Mode of operation, d) Output voltage of the current PI controller (blue curve) and Don (red curve).

Once the reference output current presents a longer duration for both 5 A and -5 A as shown in Figure 3-13, the voltage of the supercapacitor will decrease below 24 V and increase above 48 V. The latter can actually damage a supercapacitor rated at 48 V. On the other hand, for low input voltages, due to voltage gain constraints even in the Boost mode, the converter will not be able to

keep injecting current into the DC bus. Figure 3-14 shows how the input voltage protection logic works to keep the supercapacitor's voltage within the desired voltage range, from 24 V to 48 V. This is achieved by keeping the output current at 0 A if the reference output current is such that will take the capacitor voltage outside its specified range.

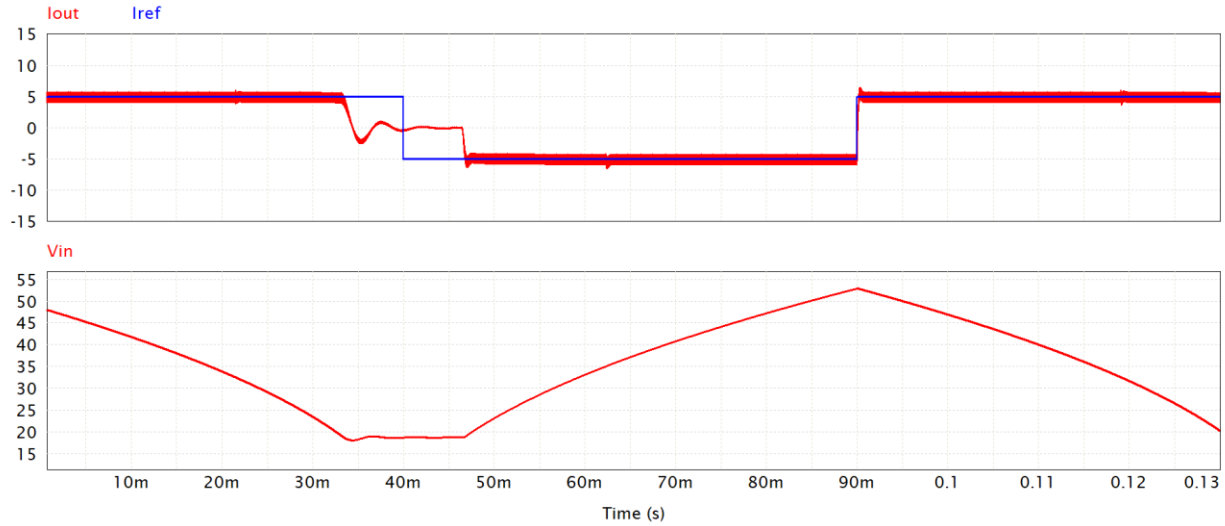

Figure 3- 13 a) Reference (blue) and actual output current (red) without the input voltage protection logic b) Input/supercapacitor voltage

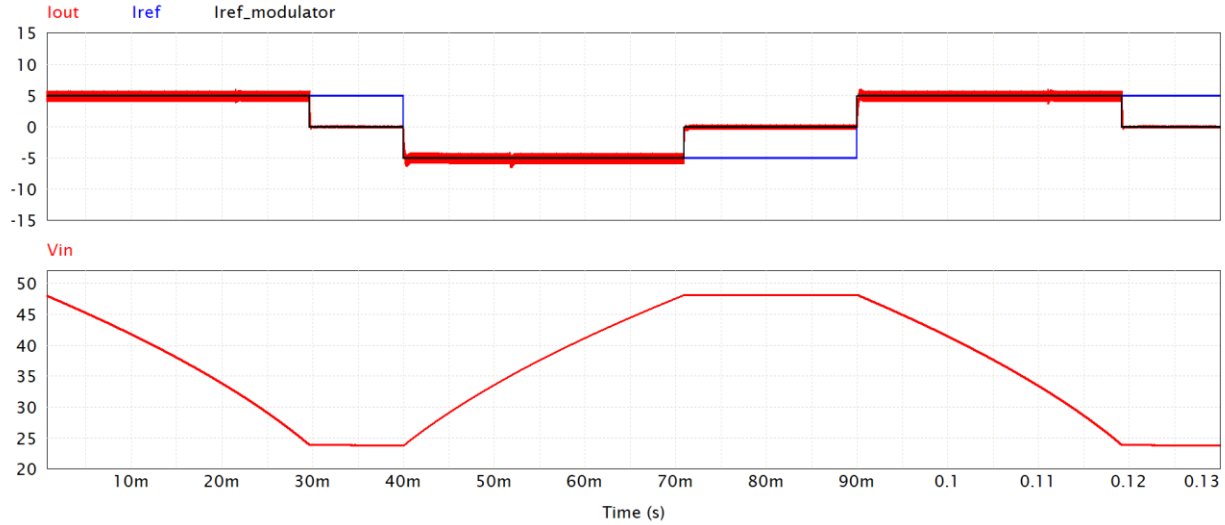

Figure 3- 14 a) Reference and actual output current with the input voltage protection logic b) Input/supercapacitor voltage

3.5 Simulation verification for experiments

An experimental prototype of the bidirectional 4-switch DC-DC converter was also used in another existing set-up and some of its parameters and components had to be modified to be able to be used in both studies. Thus, the value of the input and output capacitors of this work are adjusted to 637 µF as the ones in the set-up. By using bigger capacitors compared to the designed ones, the input and output current ripples will become smaller. Before the experimental implementation, simulation verification of the digital control scheme will be done with models of different peripherals of a DSP F28335 in the SimCoder module [20] in PSIM, which is the same as the one (Texas Instrument DSP "TMS320F28335" [21]) used in the experimental prototype.

3.5.1 Design the digital controller using direct digital approach

To design the digital controller, the sampling frequency used for the feedback output current sensor is chosen the same as the switching frequency 50 kHz. For stable operation with the experimental setup, the bandwidth of the converter has to be limited within 1/20th of the sampling frequency [19], thus the crossover frequency of the experimental setup is selected as 2 kHz in this project, and the phase margin is set as 60°.

Final parameters in the set-up for experiments are shown in Table 3.1.

Table 3. 1 Parameters in the setup for experiments

Parameter	value
Inductor L	47 µH
Output capacitor C_o	637 µF
Fixed D_{off} for tri-state operation	0.35
R_f between output capacitor and DC bus	0.2 Ω
Input voltage V_{in}	48 V
Output voltage V_o	52.8 V
Sampling frequency f_s	50 kHz

The transfer function of the plant in s-domain with the above parameters is

$$G(s) = \frac{i_o(s)}{d(s)} = \frac{2.806\times10^9}{s^2+7849s+4.092\times10^6} \quad (3\text{-}2)$$

Mapping $G(s)$ to the z-domain using a zero-order-hold (ZOH) with a sampling frequency (f_s) 50 kHz, one can get

$$G(z) = \frac{0.5328z+0.5057}{z^2-1.853z+0.8547} = 0.5328\frac{z+0.949}{(z-0.9888)(z-0.8644)} \quad (3\text{-}3)$$

By using the direct digital approach, the controller is designed in the w-domain first and then transferred to the z-domain. This is achieved by using w-transformation and the reverse relationship given by [18]

$$z = \frac{1+\frac{T_S}{2}w}{1-\frac{T_S}{2}w} \quad (3\text{-}4)$$

$$w = \frac{2}{T_S}\frac{z-1}{z+1} \quad (3\text{-}5)$$

Where $T_s = 1/f_s$.

Thus, equations (3-4) and (3-5) can be rewritten as

$$z = \frac{1+10^{-5}w}{1-10^{-5}w}$$

$$w = 10^5\frac{z-1}{z+1}$$

The transfer function of the plant in the w-domain is

$$G(w) = G(z)\left(z = \frac{1+\frac{T_s}{2}w}{1-\frac{T_s}{2}w}\right) = 0.5328\frac{\frac{1+10^{-5}w}{1-10^{-5}w}+0.949}{(\frac{1+10^{-5}w}{1-10^{-5}w}-0.9888)(\frac{1+10^{-5}w}{1-10^{-5}w}-0.8644)}$$

$$= -7.3\times10^{-3}\frac{(w+3.8\times10^6)(w-10^5)}{(w+563)(w+7273)} \quad (3\text{-}6)$$

The controller is designed to fulfill a crossover frequency f_c at 2 kHz and phase margin 60° in the s-domain.

In the w-domain, the crossover frequency v_c is given by

$$v_c = \frac{2}{T_s} tan\left(\frac{w_c T_s}{2}\right) = 12633.88\, rad/s \qquad (3\text{-}7)$$

Where

$$\omega_c = 2\pi f_c = 12566.37\, rad/s$$

There is a small change in the crossover frequency v_c which is caused by the distortion in the frequency when mapping from the z-domain to the w-domain.

At the crossover frequency v_c

$$|G(jv_c)| = 15.2082 \qquad \angle G(jv_c) = -154.53°$$

To get 60° phase margin, the controller should provide

$$\angle G_c(jv_c) = 60° - \angle G(jv_c) - 180° = 34.53°$$

Therefore, a lead compensator is designed to provide a lead angle 34.53°

Let the lead compensator be presented as

$$G_c(w) = k\frac{w+z}{w+p} \qquad (0 < z < p) \qquad (3\text{-}8)$$

Choose the pole and the zero so that

$$\begin{cases} \sqrt{pz} = v_c \\ sin\, 34.53° = \frac{\alpha-1}{\alpha+1} \\ \alpha = \frac{p}{z} \end{cases} \qquad (3\text{-}9)$$

After calculation.

$$\begin{cases} \alpha = 3.6168 \\ p = 24026.9692 \\ z = 6643.1567 \end{cases}$$

The gain of the open loop at v_c should be 1, that is

$$|G_c(jv_c)||G(jv_c)| = 1$$

$$k\left|\frac{jv_c + 6643.1567}{jv_c + 24026.9692}\right| \times 15.2028 = 1$$

The gain of the controller is calculated and equals to 0.125, and the digital control in the w-domain is

$$G_c(w) = 0.125\frac{w+6643.1567}{w+24026.9692} \quad (3\text{-}10)$$

Transferring the controller to the z-domain.

$$G_c(z) = G_c(w)\left(w = \frac{2}{T_s}\frac{z-1}{z+1}\right) = 0.1075\frac{z-0.8754}{z-0.6125} \quad (3\text{-}11)$$

Checking the steady state error of one step input 1[n] for the control loop:

$$\lim_{z\to 1}\frac{1}{1+G_c(z)G(z)} = \lim_{z\to 1}\frac{1}{1+0.1075\frac{z-0.8754}{z-0.6125}\times 0.5328\frac{z+0.949}{(z-0.9888)(z-0.8644)}} \approx 0.04$$

With the reference 5 A output current, the magnitude is five times of one step input that is 5[n], thus the steady state error of the control loop will be about 0.2.

To get zero steady-state error for a step input, the open loop $G_c(z)G(z)$ should have at least one pole at 1, since the plant has no poles at 1, a lag compensator is added to the controller with a pole at 1, and a zero at 0.9888 to minimize their effect on the transient response and cancel one of the poles of the plant. Therefore, the final digital controller is shown below.

$$G_c(z) = 0.1075\frac{z-0.8754}{z-0.6125}\times\frac{z-0.9888}{z-1} \quad (3\text{-}12)$$

3.5.2 Simulation scheme for generating the code used in the DSP

In digital control, one can see that in Figure 3-15, an ADC module of the DSP F28335 is used to convert the analog signals into digital signals and then the digital signals are processed by the current control loop. Since the input range of the ADC module is from 0 to +3 V, the actual measured values of input voltage v_{in}, output voltage v_o, and output current i_o need to be "conditioned" with appropriate gains and level shifts to make sure these values are well within the input range of the ADC module. Then, the process is reversed to obtain the actual values of

voltages and currents to be used by the DSP for control purposes. Besides, the output current is negative when drawing power from the grid, thus an offset (level shift) of 1.5 V for the output current is also considered after the gain to make sure all the output current can be sent accurately to the ADC module. This conditioning circuit is on the sensor board, and the details are shown in the Appendix. The hysteresis for the input voltage protection is also realized in the digital domain. Illustrating the hysteresis block for the maximum input voltage as an example, the value of the output NAND logic "a" changes (0 or 1) when the input voltage reaches the upper limit (48.1 V) or lower limit (47.8 V) depending on the signal is rising or falling. That is when the input voltage equals or is lower than 47.8 V, the value of the "L" terminal is 0 so the value of "b" is 1, and the value of the "H" terminal is 1. Thus the output NAND logic "a" is 0 regardless of the former value of "b", with the input voltage rising and exceeding 47.8 V but lower than 48.1 V. The value of "H" terminal keeps at 1, the value of "L" terminal changes to 1, with the unit delays, the NAND logic which compares the value of "H" terminal (which is 1) and the former value of "b" (which is 1) will keep an output value of "a" at 0. When input voltage equals or is higher than 48.1 V, the value of the "H" terminal is 0, thus the output NAND logic "a" is 1 regardless of the former value of "b", the value of the "L" terminal is 1 and the value of "b" will be 0; with the input voltage falling and lower than 48.1 V but higher than 47.8 V, the value of "H" terminal changes to 1, the value of "L" terminal keeps at 1, with the unit delays, the NAND logic which compares the value of "H" terminal (which is 1) and the former value of "b" (which is 0) will keep an output value of "a" at 1. The value of "a" is used in the protection logic discussed in chapter 3.3.

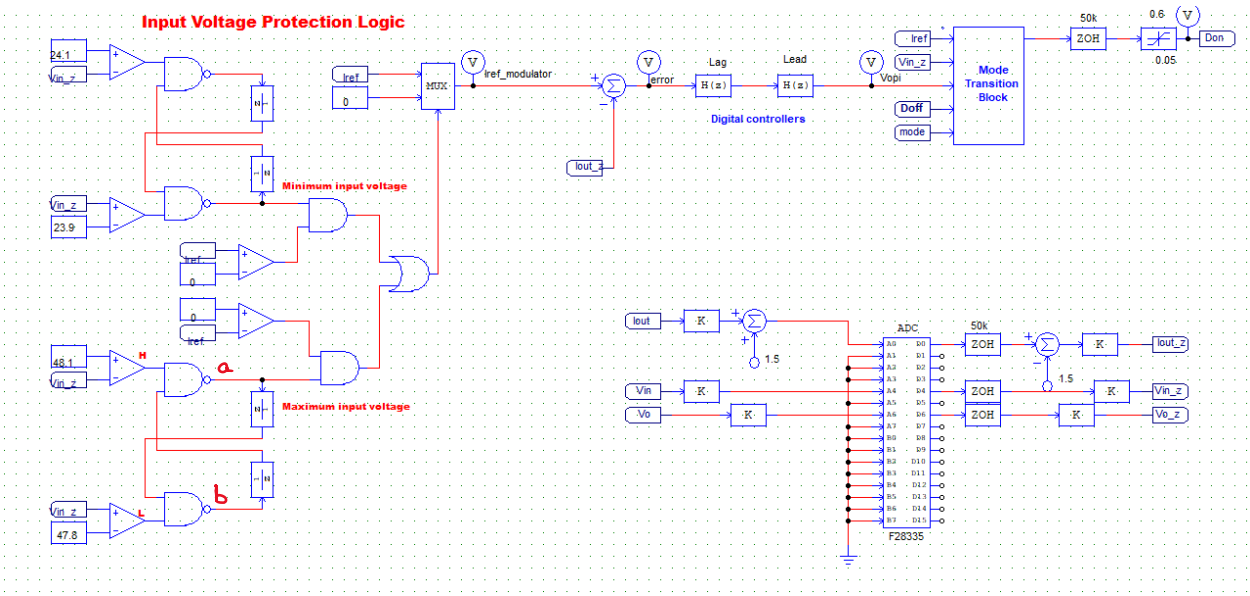

Figure 3- 15 The ADC module and digital current control loop

The gating signals for the four switches are generated by using Enhanced PWM Modules (ePWM) of F28335. One 1-phase PWM block as a reference ePWM and one 1-phase PWM block with phase shift for S1 and S2, and another 1-phase PWM block for S3 and S4. These three ePWM blocks have the same settings: triangular carrier wave starting low, peak-to-peak value "1" and 50 kHz sampling frequency. For all the four modes of operation (Mode 11, Mode 12, Mode 13, Mode 14), S3 is only ON during the OFF states, so the input of the 1-phase PWM for S3 is D_{off}, and the gating signal of S4 is the complement of S3. For the input of the 1-phase PWM with phase shift for S1 and S2, it has different input values in Boost and Buck-Boost modes, therefore, with the value of signal *BorBB* (Boost = 0 and Buck-Boost = 1) sent to a multiplexer with 2 inputs, the values of (D_{on} + D_{off}) for Boost mode or D_{on} for Buck-Boost is sent as an input of the one 1-phase PWM block to generate the gating signals, and the calculation procedure of the values of phase shift for S1 in the four modes of operation is shown below.

The input and output waveforms of an ePWM generator with the triangular carrier wave in start-low mode are shown in Figure 3-16. In the start-low mode, the ePWM positive output PWMA is low at the beginning of the switching cycle, and it is high when the carrier wave is greater than the value V_H - (v_m - V_L) [20]. In this project, the positive output PWMA is used for S1 or S3 and the PWMB is used for S2 or S4, the value of V_H is set to 1, and the value of V_L is set to 0.

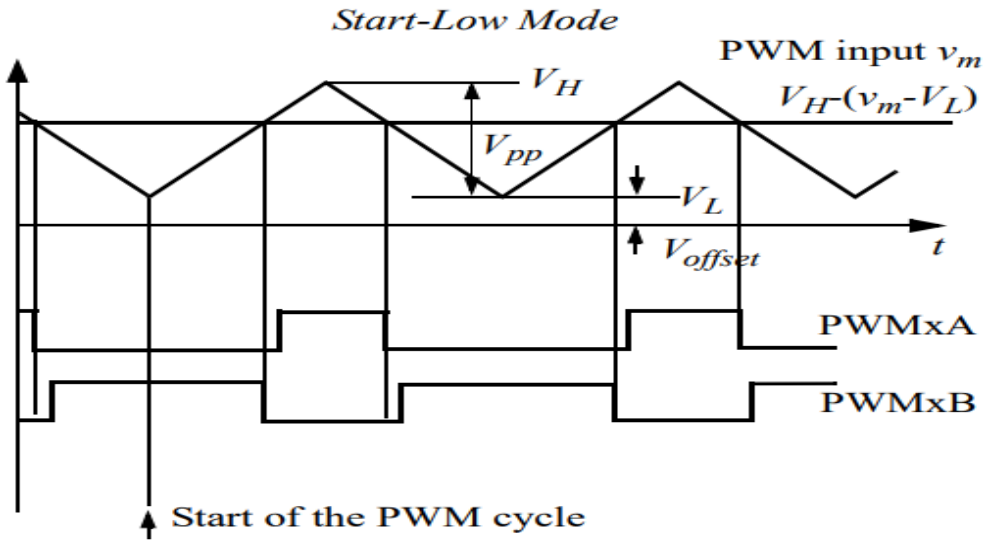

Figure 3- 16 Input and output waveforms of a ePWM generator of F28335 [20].

The phase shift value is in degree, and it is 360° for one switching cycle. For a negative phase shift, the output will be shifted to the right (lagging) of the switching cycle with respect to the reference ePWM generator output, and with a positive phase shift, the output will be shifted to the left (leading) of the switching cycle [20].

For Mode 11: the Boost mode $D_{on} - D_{off} - D_{fw}$, the input and output waveforms of the ePWM blocks of S1 and S3 are shown in Figure 3-17, without considering the dead time. One can see that gating signal waveform of S1 needs to lead phase α to synchronize with the gating signal waveform of S3 in every period, since during OFF state, S1 and S3 are both ON.

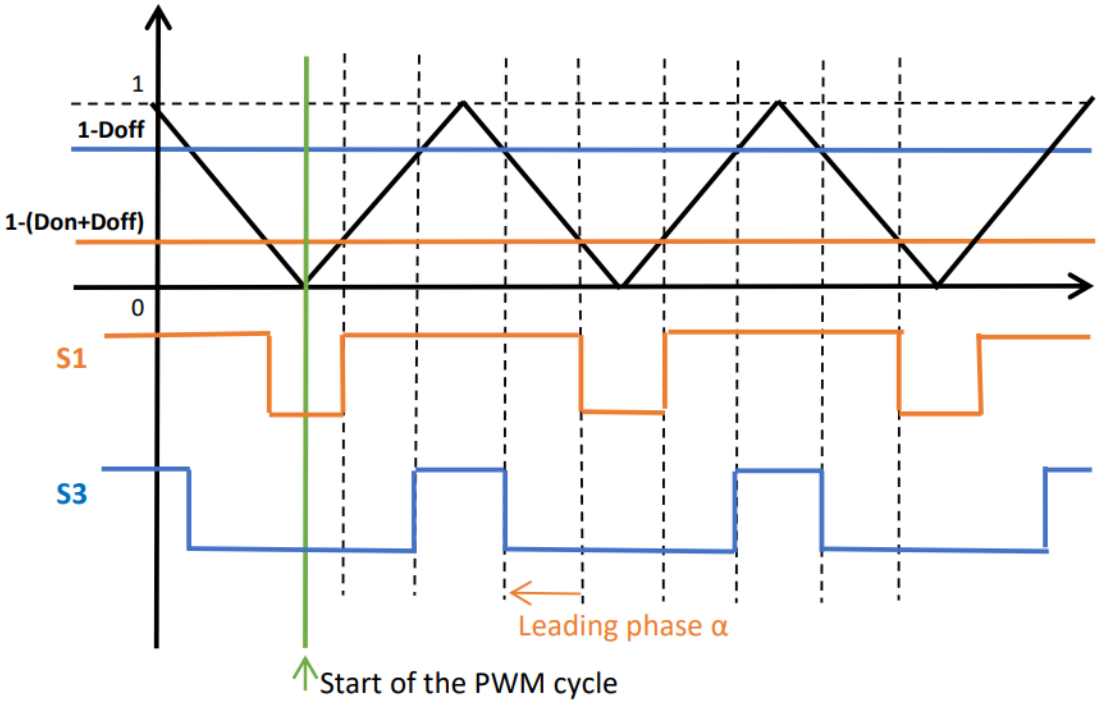

Figure 3- 17 Input and output waveforms of the ePWM blocks of S1 and S3 in Mode 11 (S1 in orange color, S3 in blue color)

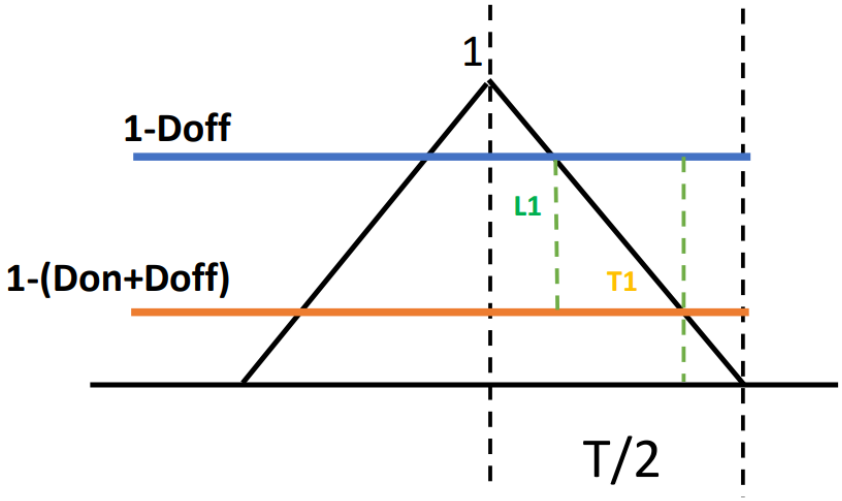

Figure 3- 18 Triangle carrier wave with the control signals of S1 and S3 in one period (S1 in orange color, S3 in blue color)

The triangular carrier waveform with the control signals of S1 and S3 in one period is shown in Figure 3-18. The value of the leading phase α can be calculated using following equations.

$$\frac{T_1}{T/2} = \frac{L_1}{1} = \frac{D_{on}}{1} \qquad (3\text{-}13)$$

$$\frac{360°}{\alpha} = \frac{T}{T_1} \tag{3- 14}$$

Therefore, for Mode 11, the value of phase shift of the ePWM block for S1 should be:

$$\alpha = 180° D_{on}$$

Similarly, the values of the phase shift of S1 for the four modes of operation can be calculated and shown in Table 3.2, Since these values are relative phase shifts between S1 and S3, it does not change the phase shift values when adding dead time for the switches.

Table 3. 2 Phase shift of the ePWM block for S1

Mode of operation	The phase shift for ePWM block for S1
Mode 11	$180° D_{on}$
Mode 12	$-180° D_{on}$
Mode 13	$180°(D_{on} + D_{off})$
Mode 14	$-180°(D_{on} + D_{off})$

The mode of operation which is illustrated in Figure 2-19 is also realized in the digital domain, by adding unit delays with 50 kHz sampling frequency. The mode of operation and ePWM blocks for the four switches are presented in Figure 3-19, with the value 0, 1, 2, or 3 that one gets from the Mode subtracted 11, sent to a 4-input MUX. The value of the phase shift is forwarded to the 1-phase PWM block with the phase shift for the gating signal of S1 and S2.

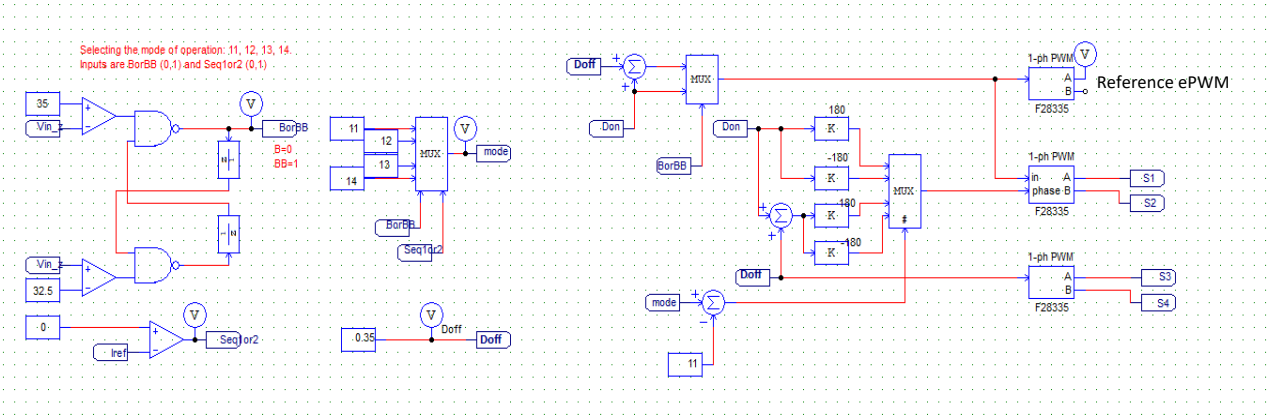

Figure 3- 19 Mode of operation and ePWM blocks for the four switches

The total digital simulation scheme is shown in Figure 3-20.

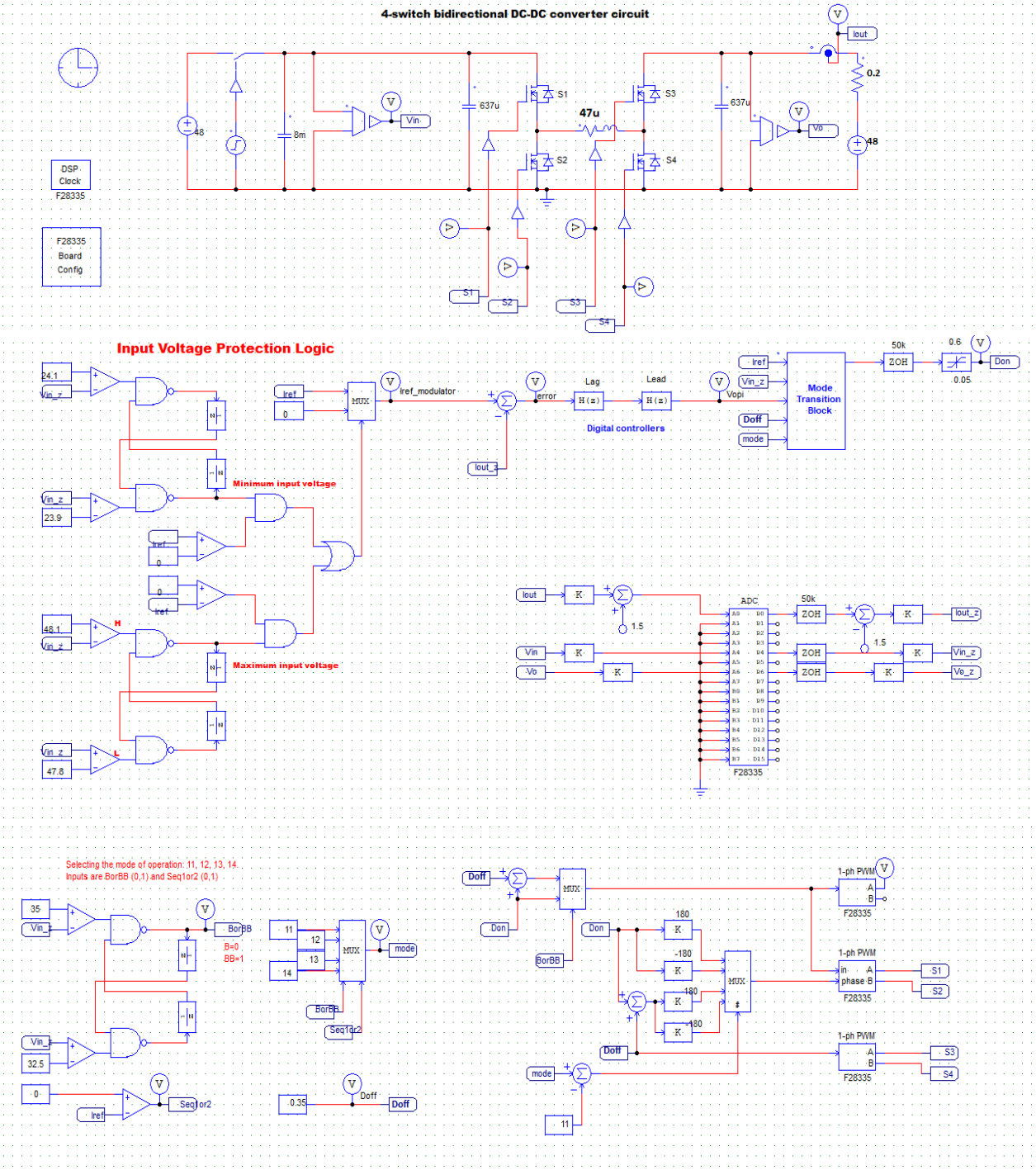

Figure 3- 20 Digital simulation scheme

3.5.3 Simulation results

The digital controller designed with new parameters and the digital simulation scheme are tested in this section. The performance of the converter with tri-state modulation is validated in both Boost (24 V) and Buck-Boost (45 V) modes, shown in Figure 3-21 and 3-22, respectively. One can see that in both modes, the output current can track the reference (± 5 A) very well. The output current responds very quickly and reaches the steady state fast at the step-up and step-down transitions in both Boost and Buck-Boost modes, while it rises a little more rapidly in Buck-Boost mode than in Boost mode where the reason is discussed in analog control.

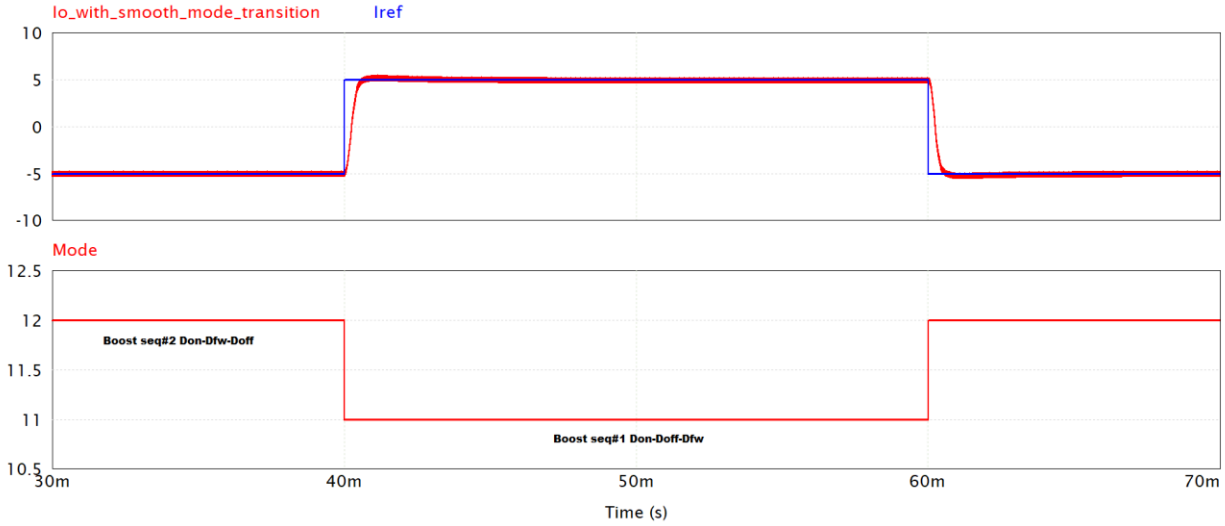

Figure 3- 21 Digital simulation results of the converter with tri-state in Boost mode (Vin = 24 V)

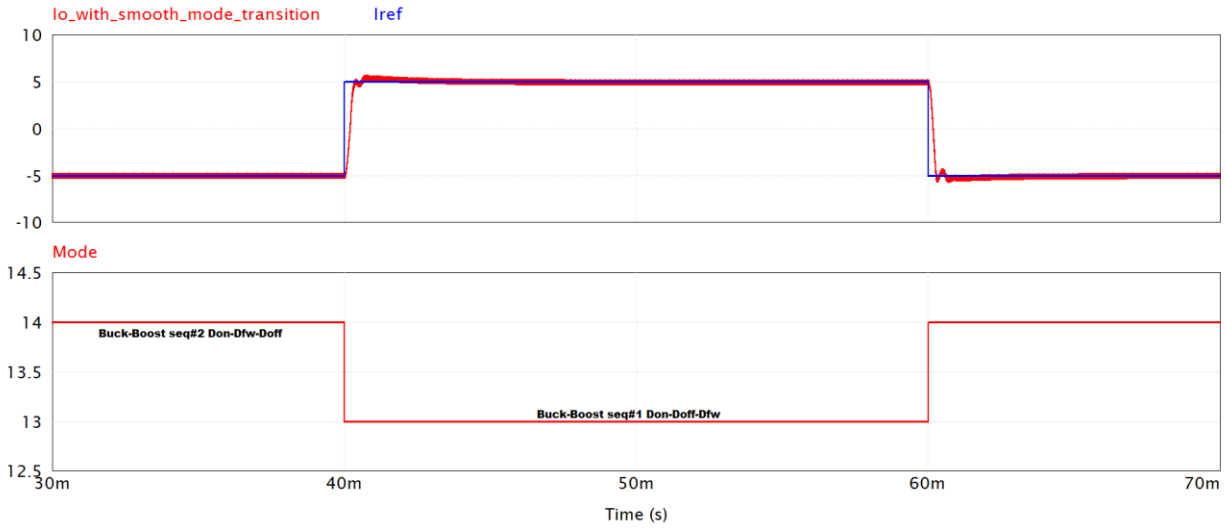

Figure 3- 22 Digital simulation results of the converter with tri-state in Buck-Boost mode (Vin = 45 V)

Simulation results with a constant input voltage 33 V for the smooth mode transition logic are shown in Figure 3-23 and Figure 3-24. There one can see that with a constant input voltage, the smooth mode transition logic has a large impact on reducing variations of the output current during transitions between Boost and Buck-Boost modes, for both positive and negative reference. The results without the smooth mode transition logic present large current variations nearly 9 A when mode changes.

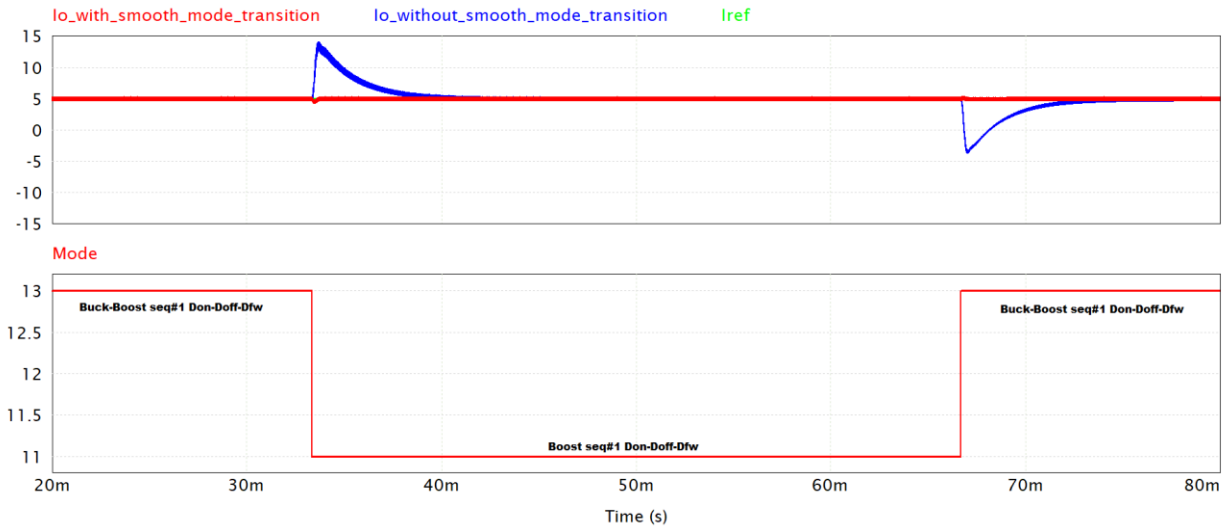

Figure 3- 23 Change of mode of operation in digital control: Boost to Buck-Boost to Boost for Iref = 5 A and Vin = 33 V. Without a smooth mode transition logic (blue curve) and with a smooth mode transition logic (red curve).

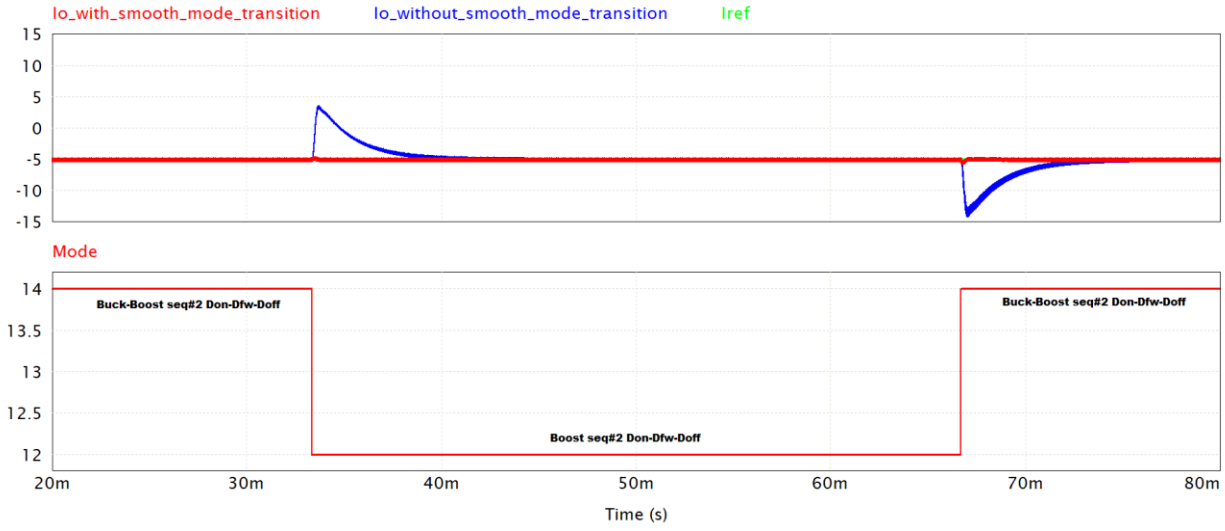

Figure 3- 24 Change of mode of operation in digital control: Boost to Buck-Boost to Boost for Iref = -5 A and Vin = 33 V. Without a smooth mode transition logic (blue curve) and with a smooth mode transition logic (red curve).

Figure 3-25 illustrates the simulation results tested with a 20 mF capacitor in a wide input voltage (24 V- 48 V), with the smooth mode transition logic. In the figure, with a positive reference, the converter operates in Buck-Boost mode sequence 1 with 48 V input voltage, and the input voltage decreases when the converter is injecting current into the grid. When the input voltage comes to a transition point of 32.5 V, the mode changes to Boost mode sequence 1. Then, when the reference changes to a negative, the capacitor is charged, and its voltage increases from 24 V to 48 V. Finally, when it comes to a transition point of 35 V, the mode changes from Boost mode sequence 2 to Buck-Boost mode sequence 2. During the total process, one can see that the output current tracks the reference very well and has tiny current variations when mode changes between Boost and Buck-Boost modes.

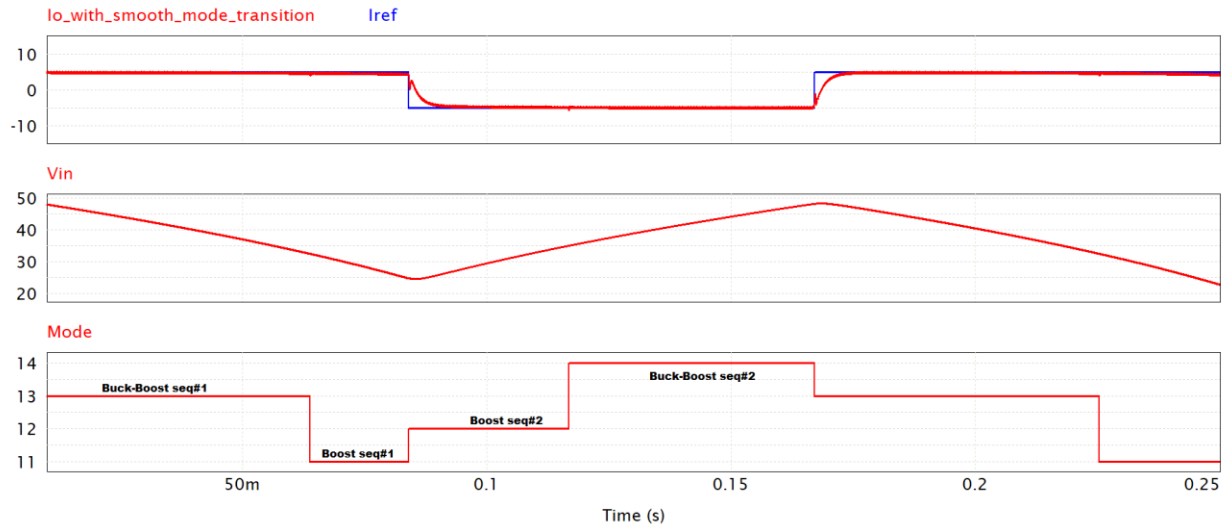

Figure 3- 25 The 4-switch converter operating with a wide input voltage in digital control: a) Reference and actual output current, b) Input/supercapacitor voltage, c) Mode of operation

3.6 Summary

This Chapter discusses how the smooth mode transition logic works for the 4-switch bidirectional DC-DC converter operating between Boost and Buck-Boost modes, with the input voltage varying between 24 V and 48 V. The smooth mode transition using c code is shown and the input voltage protection logic, to prevent undervoltage and overvoltage across the supercapacitor, is designed and illustrated. Several cases are run to evaluate the smooth mode transition logic with a constant input voltage of 33 V, with the variable input voltage, and cases with and without the input voltage protection logic are also shown. Simulation verification for the

experimental tests with updated parameters and designed digital controller was presented and verified. The experimental implementation will be presented in Chapter 4.

Chapter 4 Experimental Implementation

The primary goal of this work is to implement a signal duty cycle control for regulating the output current of a 4-switch bidirectional DC-DC converter with tri-state logic, operating in both Boost and Buck-Boost modes with a wide input voltage range of a supercapacitor, by using the smooth mode transition logic. The experimental setup is illustrated in this chapter, and some different experimental cases are presented and discussed.

4.1 Experimental setup

The experimental prototype [22] of the 4-switch bidirectional DC-DC converter is implemented in this work, using a modified board of a Texas Instruments (TI) converter "LM5170EVM-BIDIR Bidirectional Converter Evaluation Module" [23] which was also used for another research. The board consists of four MOSFETS, arranged in two half-bridges, with respective gate driver circuits, a capacitor bank of 637 μF in both input and output, and a 47 μH inductor connected between the two half-bridges. The input and output voltages and the output current are sensed by hall-effect based voltage and current sensors on the PCB board of the converter. A signal conditioning circuit is used for converting the sensed current and voltages into voltage values that can be supplied to a DSP F28335 (Texas Instrument DSP "TMS320F28335"): 0 – 3 V. Codes for the F28335 are generated in PSIM, from the simulation files, and imported in Code Composer Studio [24]. Experimental results are presented using a ROHDE&SCHWARZ oscilloscope available in the PEER laboratory, Concordia University.

One can see in Figure 4-1 the block diagram of the experimental setup. The 4-switch bidirectional DC-DC converter is implemented on the PCB board connecting with the DSP and sensors measurement board. In this project, the converter operating with tri-state can interface a supercapacitor to a DC grid, or two energy storage devices. Considering the devices availability in the lab, a DC power supply parallel with a resistor through a diode for charging and discharging is used for emulation of the DC bus. For the supercapacitor, two 16 V 58 F series-connected supercapacitors are used in the verification experiments with varying input voltage. Based on the datasheet, the voltage protection limits are set as 14 V and 26 V, thus the SCs need to be charged higher than 14 V, before it can be connected to the circuit for transient power support. A soft

starting scheme consisting of a switch (S5) in series with a resistor R_{in} and in parallel with another switch (S6), is added between the input source and the converter. This prevents large in-rush currents from the supercapacitor to the input filter capacitor of the converter. After connecting the storage unit or charged SC to the converter, S5 will be closed first to charge the input capacitor C_{in}, then S6 is closed to short the resistor R_{in}, to conduct the experimental tests.

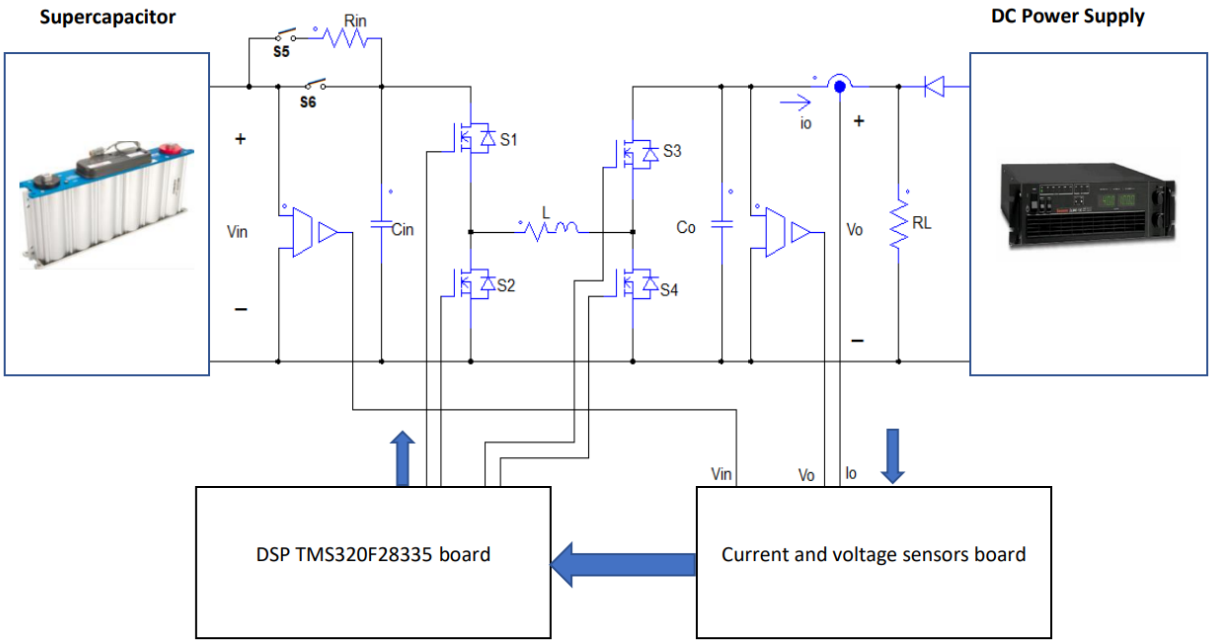

Figure 4- 1 The block diagram of experimental setup

Figure 4-2 shows the experimental setup, which is assembled in the laboratory. One can see that a DC power supply (A) and a resistor (B) are used to charge supercapacitors (C), the 4-switch bidirectional DC-DC converter (D) interfaces SCs and a DC power supply (F) parallel with load resistor RL (E) through a diode. The experimental results are presented on the oscilloscope (H). Figure 4-3 presents a snapshot of the 4-switch bidirectional DC-DC converter board and sensors board and the DSP F28335 board.

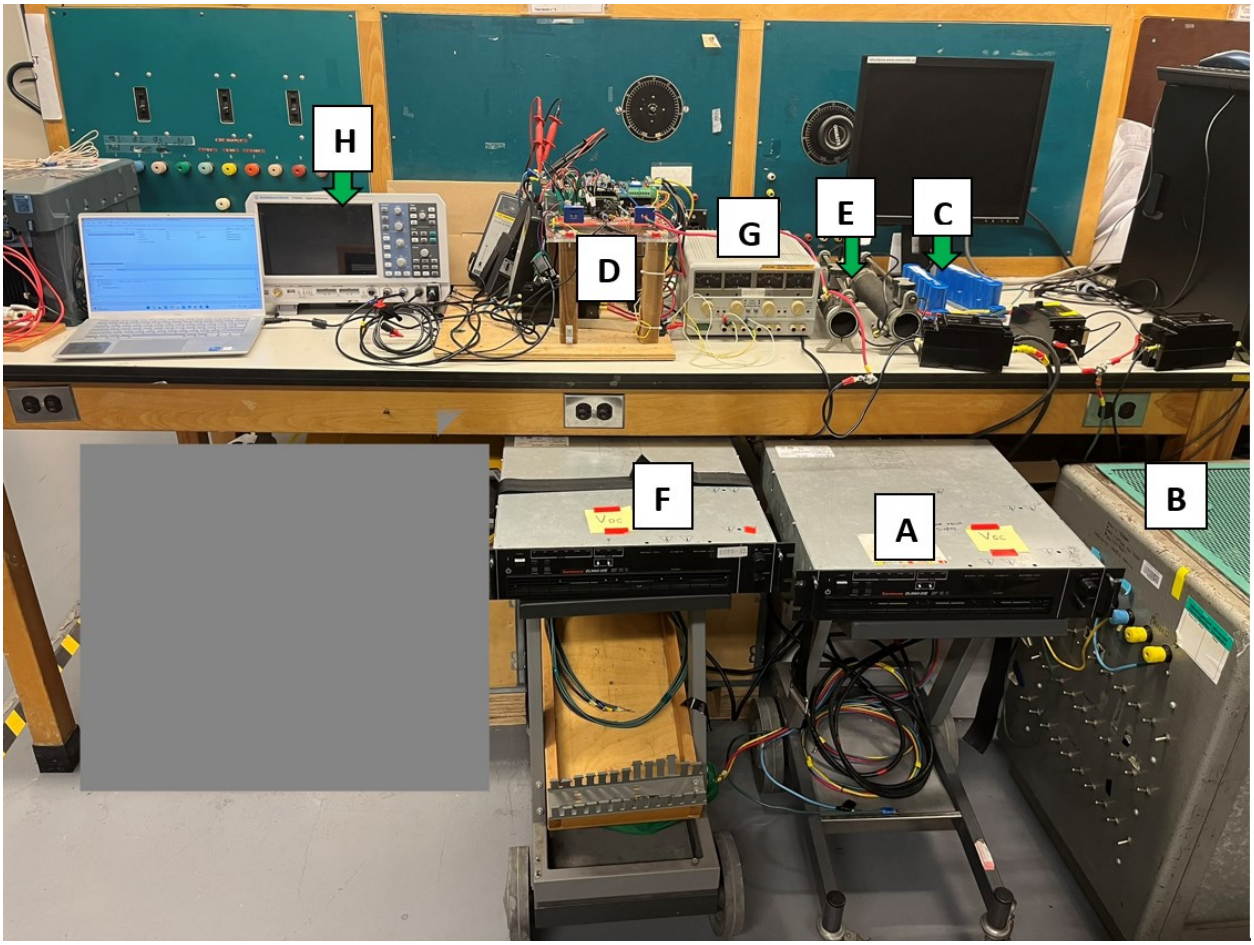

Figure 4- 2 The experimental setup.(A) DC power supply for charging SC. (B) Resistor. (C) Supercapacitors. (D) 4-switch bidirectional DC-DC converter board, DSP F28335 board and current sensors and conditioning circuit board. (E) Load resistor. (F) DC power supply. (G) DC power supply for switches and sensors. (H) Oscilloscope.

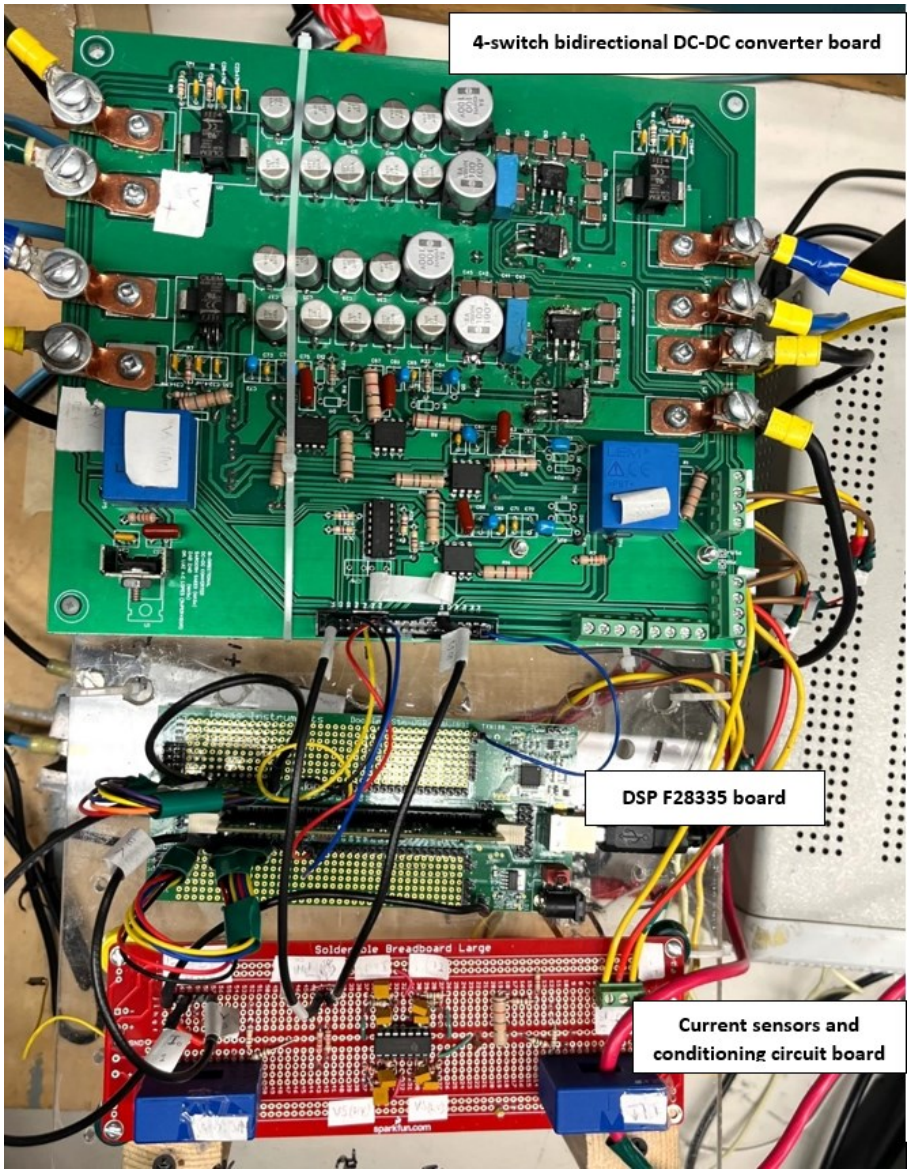

Figure 4- 3 4-switch bidirectional DC-DC converter board, DSP F28335 board and current sensors and conditioning circuit board.

4.2 Experimental results

4.2.1 Open loop test

In this project, the bidirectional DC-DC converter can operate in both Boost and Buck-Boost mode. In the tests conducted in the laboratory, a supercapacitor was used in one side and a uni-directional, source only, DC power supply in the other. In order to prevent reverse power flow in the power supply, a diode and a “shunt resistor” are employed along with the power supply. The resistor is calculated so that the current it draws from the power supply is higher than the maximum

current the DC can inject in its bus. In this way, the voltage at that bus is clamped to the voltage set at the DC power supply. Recall from Figure 2-19 and Table 2-11 that there are four modes of operation, with positive or negative output current reference. To check the converter performance, the gating signals of the four switches in the four modes of operation are tested first. The experimental gating signals of the four switches are obtained from the GPIO 2, GPIO 3, GPIO 4, and GPIO 5 of the F28335, with high value 3.3 V for switch ON and low value 0 V for switch OFF. For gating the four MOSFETs, +15 V potential is provided from an onboard power supply to turn the MOSFET "ON" and - 8.5 V potential is provided to turn the MOSFET "OFF" [22].

4.2.1.1 The impact of phase shift in the ePWM of S1

The impact of the phase shift in ePWM of S1 is verified, and two tests in Boost mode are shown as examples. The output of the reference ePWM obtained from GPIO 0 of the F28335 and gating signals of S1, S2, and S3 are presented on the oscilloscope, to show the gating signal of S1 leading or lagging phase α with respect to the reference ePWM output based on Table 3.2. With given values: $D_{on} = 0.5$, $D_{off} = 0.35$ and $D_{fw} = 0.15$, and setting signal $BorBB = 0$ (Boost mode). The test settings of *Seq1or2* and expected results of phase α shown in Table 4.1.

Table 4. 1 Test setting and expecting results for phase shift impact

	Equation of α	Value of α (Degree)	Time duration in one switching cycle respect to α (μs)	Mode of operation
Seq1or2 = 0	$180°D_{on}$	90°	5	Mode 11
Seq1or2 = 1	$-180°D_{on}$	−90°	−5	Mode 12

In Figure 4-4, one can see cursor 1 for gating signal of S1 (C2 in pink color) leading (move to left) by 5 μs with respect to cursor 2 for the output of the reference ePWM (C1 in blue color). The gating signal of S2 (C3 in light blue color) is a complement to gating signal of S1, and the gating signals of S1, S2, and S3 (C4 in green color) present the right sequence D_{on} - D_{off} - D_{fw} in Mode 11 in one switching period 20 μs, with 50 kHz switching frequency. Similarly, in Figure 4-5, one can see cursor 1 for the gating signal of S1 lagging (move to the right) by 5 μs with respect to cursor 2 for the output of the reference ePWM, and the gating signals of S1, S2, and S3 present the right sequence D_{on} - D_{fw} - D_{off} in Mode 12 in one switching period. Thus, the equations of phase shift are validated, and work as expected.

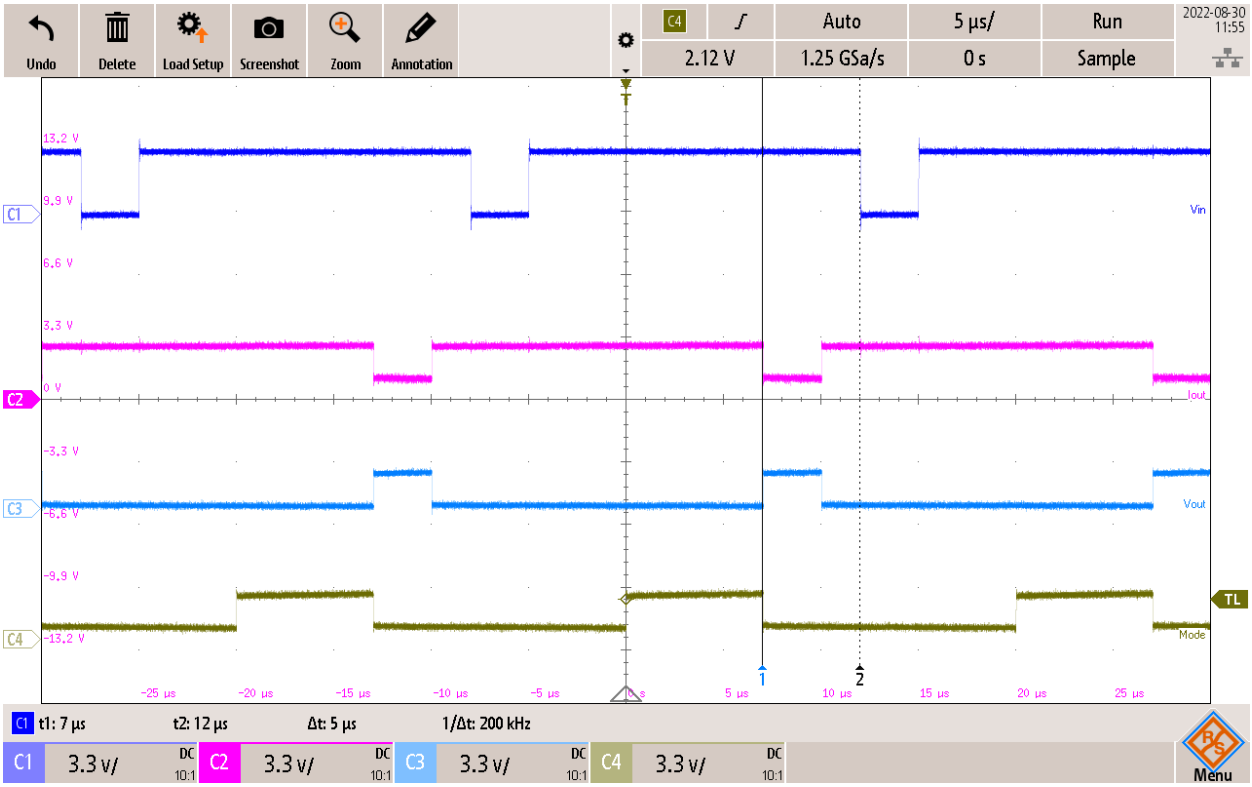

Figure 4- 4 Output of reference ePWM (C1 in blue color) and gating signals of S1 (C2 in pink color), S2 (C3 in light blue color) and S3 (C4 in green color) in Mode 11

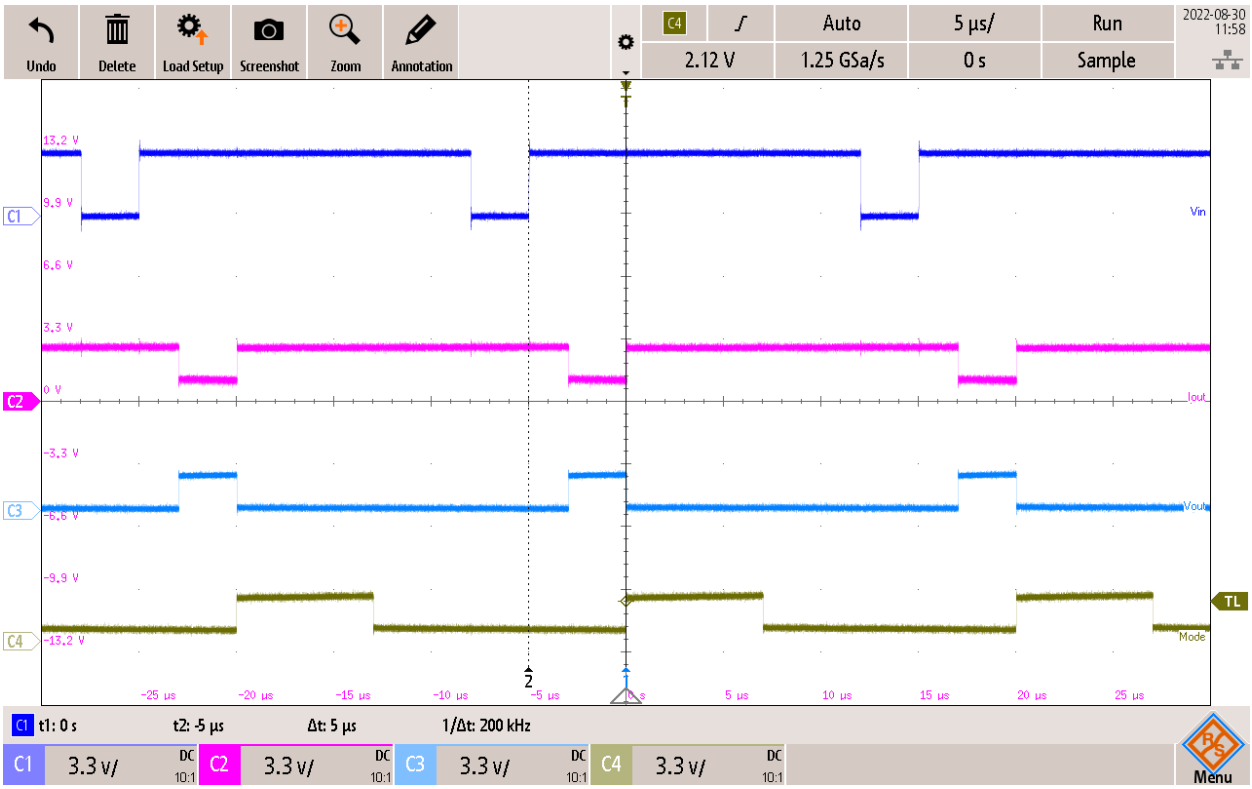

Figure 4- 5 Output of reference ePWM(C1 in blue color) and gating signals of S1(C2 in pink color), S2 (C3 in light blue color)and S3(C4 in green color) in Mode 12

4.2.1.2 Mode of operation test

The gating signals of the four switches are tested in four modes of operation with constant value/duration of each state.

The duty cycles of the three states are set as : D_{on} = 0.4, D_{off} = 0.35, D_{fw} = 0.25.

1) Mode 11

This mode of operation is for Boost mode with sequence D_{on} - D_{off} - D_{fw}. The gating signals should be

- S1 : ON during both ON and OFF states (D_{on} & D_{off}) with a total duty cycle 0.75
- S2 : complement to S1
- S3 : only ON during the OFF state (D_{off}) with a total duty cycle 0.35
- S4 : complement to S3

The converter operates in Boost mode, S1 is kept ON during ON and OFF state and then turns off during the free-wheeling state (D_{fw}), so the ON duration of S1 should be 0.75 T_s.

The experimental results are displayed on the oscilloscope screen. In Figure 4-6, one can see the four gating signals in Mode 11. It shows that the switching frequency is 49.99 kHz, and S1 is ON with duty cycle 0.7496 as analyzed. S2 is complement to S1 and S4 is complement to S3.

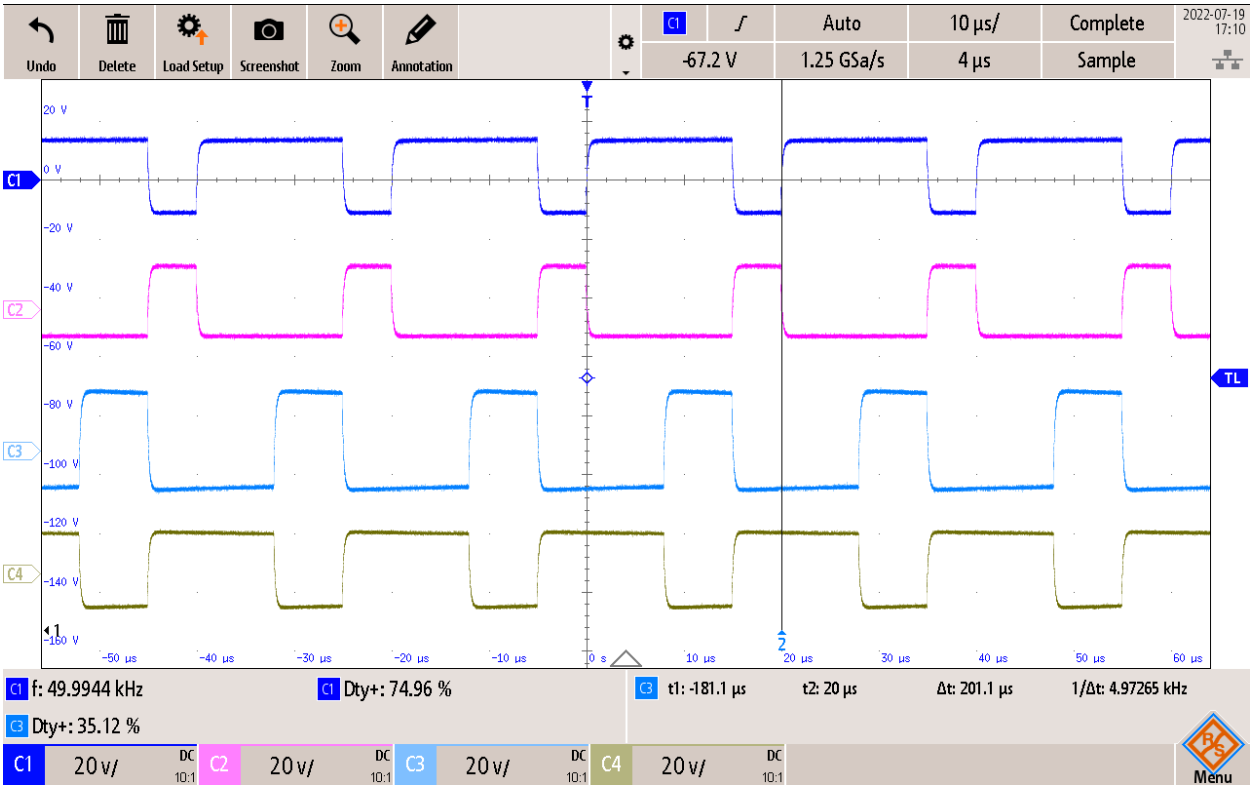

Figure 4- 6 Gating signals for the four switches in Mode 11. (C1--- S1, C2 --- S2, C3 --- S3, C4 --- S4)

2) Mode 12

This mode of operation is also for the Boost mode but with sequence D_{on} - D_{fw} - D_{off}. The gating signals should be

- S1 : switching with a total duty cycle of 0.75
- S2 : complement to S1
- S3 : only ON during the OFF state (D_{off}) with a total duty cycle of 0.35
- S4 : complement to S3

Figure 4- 7 illustrates the gating signals of the four switches in Mode 12, with the free-wheeling state in the middle. The duration time of the ON-state for each switch in every period is the same as in Mode 11, since it is still Boost mode. S2 and S4 are ON during the free-wheeling state, and it is followed with S1 and S3 ON during the OFF state.

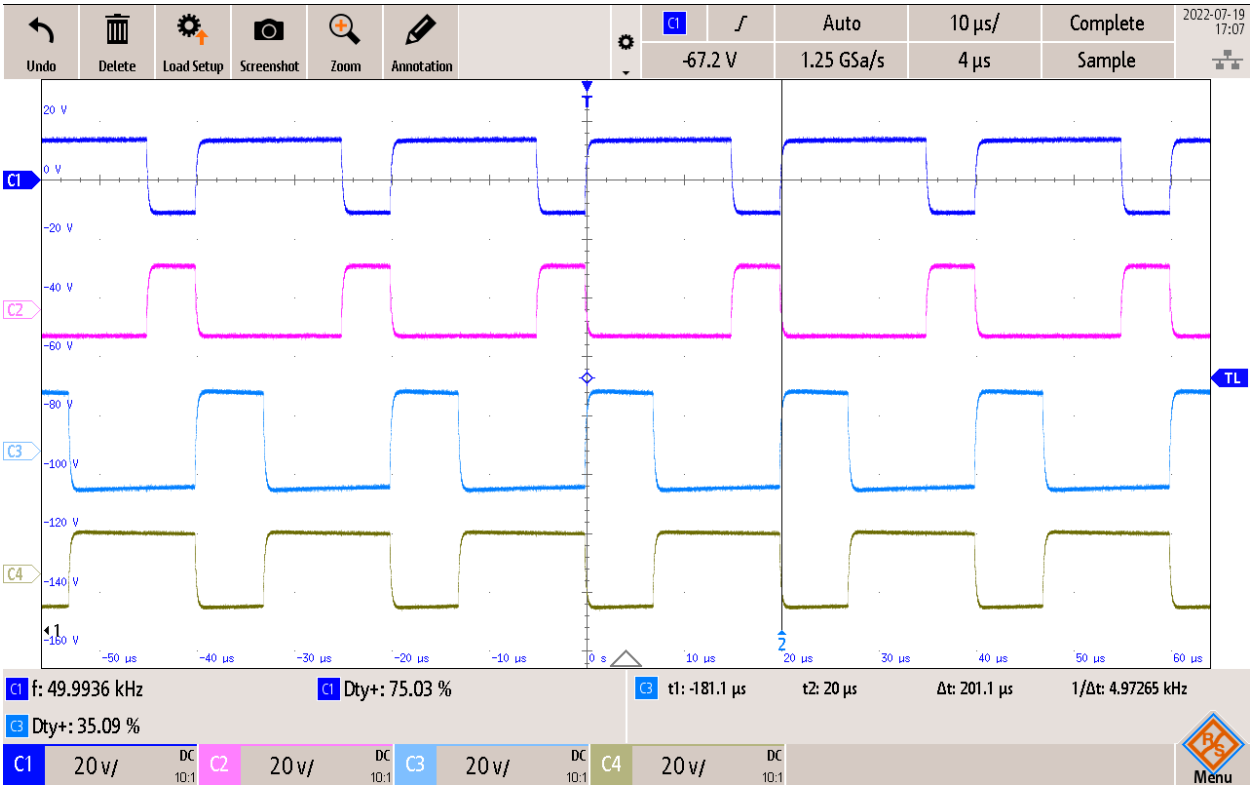

Figure 4- 7 Gating signals for the four switches in Mode 12. (C1--- S1, C2 --- S2, C3 --- S3, C4 --- S4)

3) Mode 13

This mode of operation is for Buck-Boost mode with sequence D_{on} - D_{off} - D_{fw}. The gating signals should be

- S1 : only ON during ON state (D_{on}) with duty cycle of 0.4
- S2 : complement to S1
- S3 : only ON during the OFF (D_{off}) state with a duty cycle of 0.35
- S4 : complement to S3

Figure 4-8 illustrates the gating signals of the four switches in Mode 13, the Buck-Boost mode. In this mode, S1 is ON with a duty cycle 0.4 as the value of D_{on}, and S2 is ON during both ON and OFF states (D_{on} & D_{off}). S2 and S3 are ON during OFF state (D_{off}) after S1 and S4 ON. One can recognize the gating signals are ON as shown in Table 2.11.

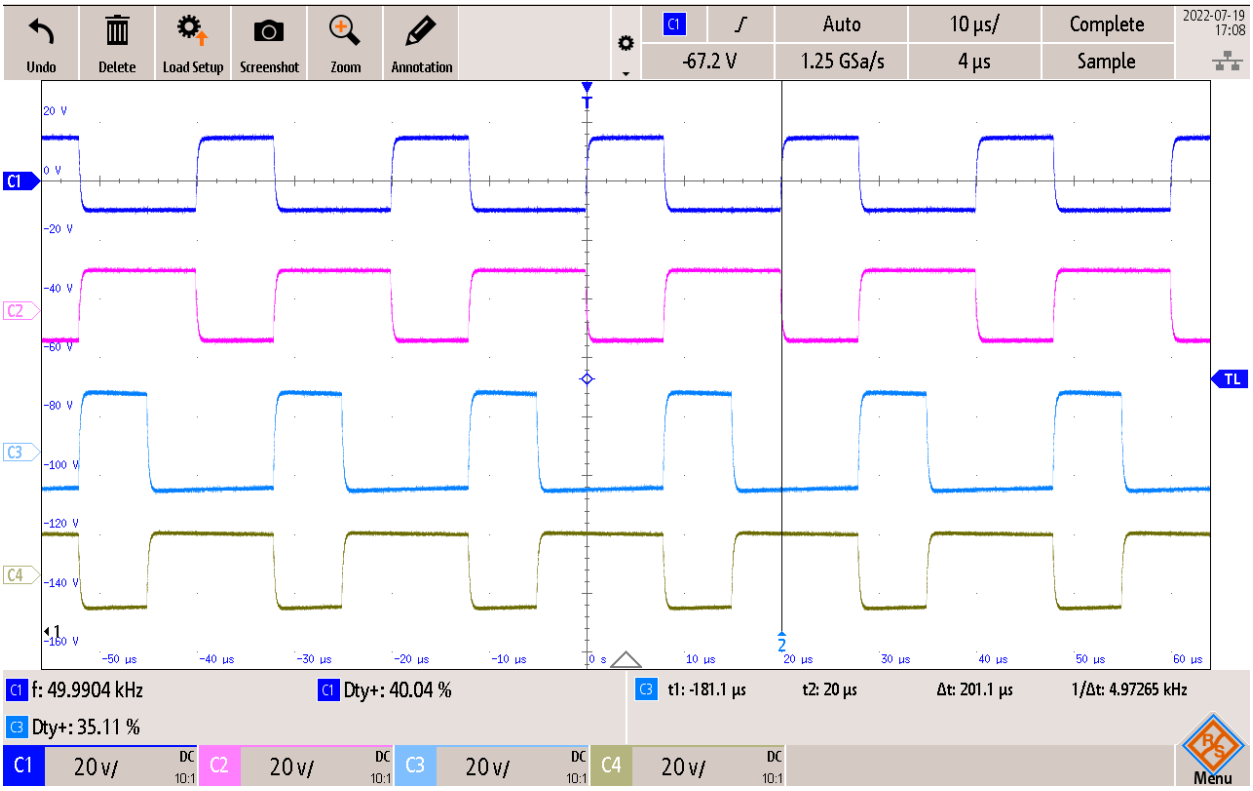

Figure 4- 8 Gating signals for the four switches in Mode 13. (C1--- S1, C2 --- S2, C3 --- S3, C4 --- S4)

4) Mode 14

This mode of operation is for Buck-Boost mode with sequence D_{on} - D_{fw} - D_{off}. The gating signals should be

- S1 : switching with duty cycle 0.4
- S2 : complement to S1
- S3 : only ON during the OFF state (D_{off})
- S4 : complement to S3

Figure 4- 9 illustrates the gating signals of the four switches in Mode 14, with the free-wheeling state in the middle, and the four switches are ON or OFF as analyzed in the Buck-Boost mode.

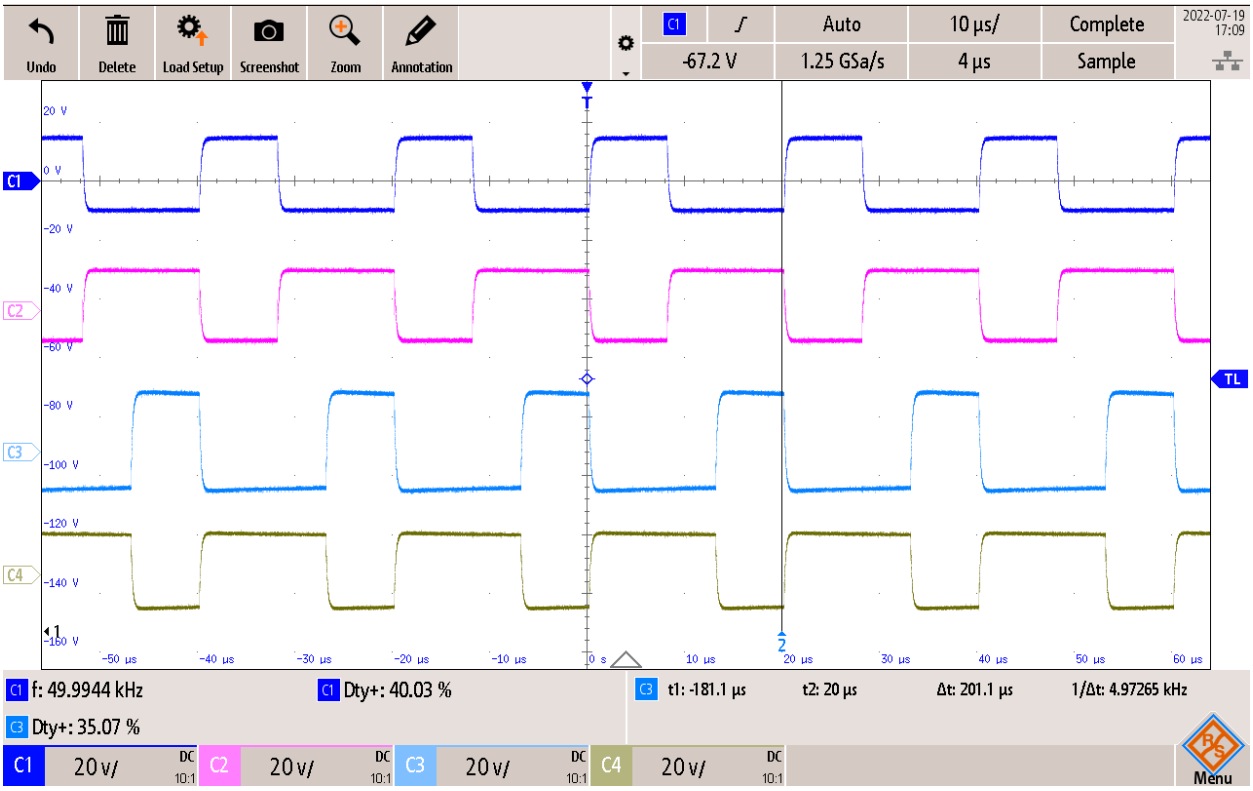

Figure 4- 9 Gating signals for the four switches in Mode 14. (C1--- S1, C2 --- S2, C3 --- S3, C4 --- S4)

In all four test cases, the shapes of the gating signals of the four switches are matched with the mode of operation, and the switching frequency and the duty cycle of S1 are shown as analyzed in each mode.

4.2.1.3 Boost mode test

A dead time of 0.2 µs is added in the ePWM blocks of the the four switches in the experimental tests, to prevent the complementay switches (S1 and S2, S3 and S4) from being ON at the same time which will short circuit the power source and damage devices. Thus, the duty cycle shown on the oscilloscope will be a little less than the theoretical values.

To test the Boost mode of operation in open loop, only using a DC power supply, replacing the supercapacitor in the input side (V_{in}) and a load resistor, in the output (V_o). The DC power supply is set to 24 V, and the reference current is set at 5 A. Then, the output voltage should be 50.55 V with 10.11 Ω load, the expected value of D_{on} based on the equation (2-7) can be calculated, and the value of each state is shown as below

$$D_{on} = 0.39,\ D_{off} = 0.35,\ D_{fw} = 0.26$$

Figure 4-10 illustrates the experimental results of the Boost mode with positive reference, that is Mode 11. S1 remains ON during D_{on} and D_{off} states. In the figure, one can see that the duty cycle of S1 and S3 are a little less than the mathematical values because of the dead time. The value of ouput current is 4.5439 A which is a little less than 5 A, which is caused by the power losses of the circuit. These are not modeled in the derivation of the voltage gain of the converter.

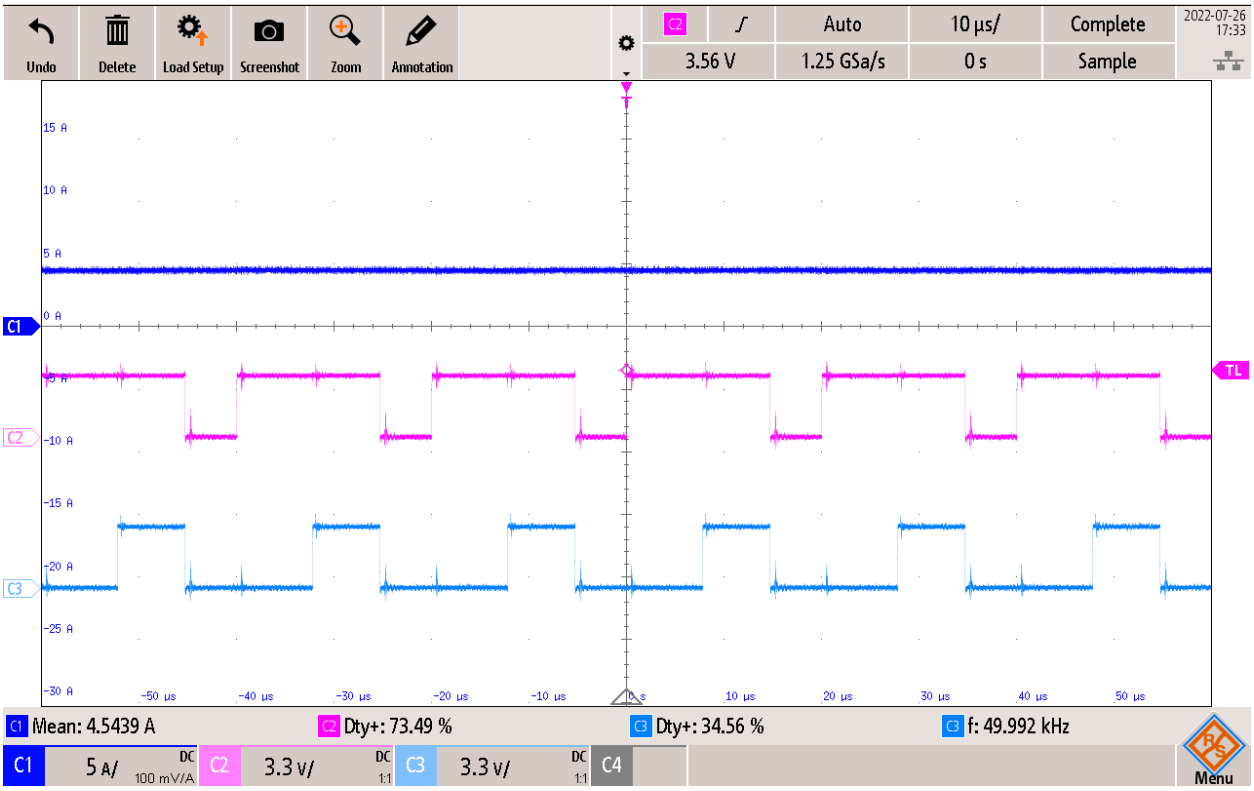

Figure 4- 10 Output current and gating signals for open loop test in Boost mode.
C1 (blue): output current, C2 (pink): gating signal of S1, C3 (light blue): gating signal of S3

4.2.1.4 Buck-Boost mode test

To test the Buck-Boost mode of operation only using a DC power supply and a load resistor, as in the previous test. The DC power source is set to supply 36 V, and the reference current is set at 5 A. Then, the output voltage should be 50.55 V with 10.11 Ω load. The expected value of D_{on} based on the equation (2-10) can be calculated, and the value of each state is shown as below

$$D_{on} = 0.49,\ D_{off} = 0.35,\ D_{fw} = 0.16$$

Figure 4-11 illustrates the experimental results of Buck-Boost mode with positive reference, that is Mode 13. With the set values of the three states, one can see that the value of the output current is lower than expected as in the Boost mode. The reason is the power losses of the circuit.

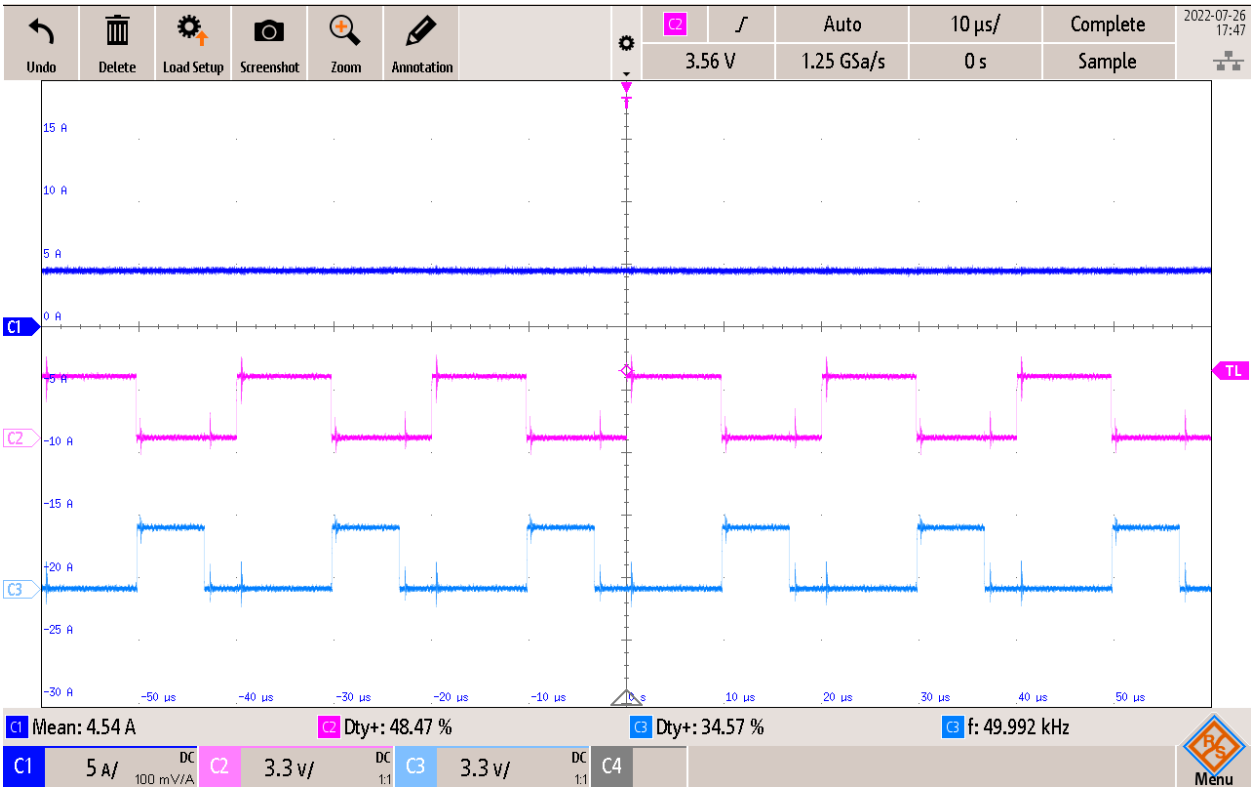

Figure 4- 11 Output current and gating signals for open loop test in Buck-Boost mode.
C1 (blue): output current, C2 (pink): gating signal of S1, C3 (light blue): gating signal of S3

4.2.3 Closed-loop test

The closed-loop operation is also tested with the DC power supply and the resistance load of 10.11Ω. With the values of input voltage of the converter: 24 V for Boost mode and 36 V for Buck-Boost mode, the control loop in the DSP F28335 can calculate the value of D_{on} based on the output current from current sensor for different reference values. Based on the error, the digital controller provides a modulation signal that is send to the ePWM blocks to generate the gating signals. The reference current is set to change from 5 A to 4 A then back to 5 A, to verify whether the digital controller regulates the output current at the set values and track the reference.

Figure 4-12 illustrates the closed-loop experimental results tested with 24 V input voltage (C1 in blue color), for the converter operating in Boost mode. One can see that the output current (C2 in pink color) is regulated at the reference current 5 A or 4 A, and follows the reference signal changing from 5 A to 4 A and then to 5 A. It presents speedy dynamic responses at the step-down and step-up current transitions. The output current shows small current ripples with the large output capacitors used on the setup. The output voltage (C3 in light blue color) has the same changing tendency as the output current.

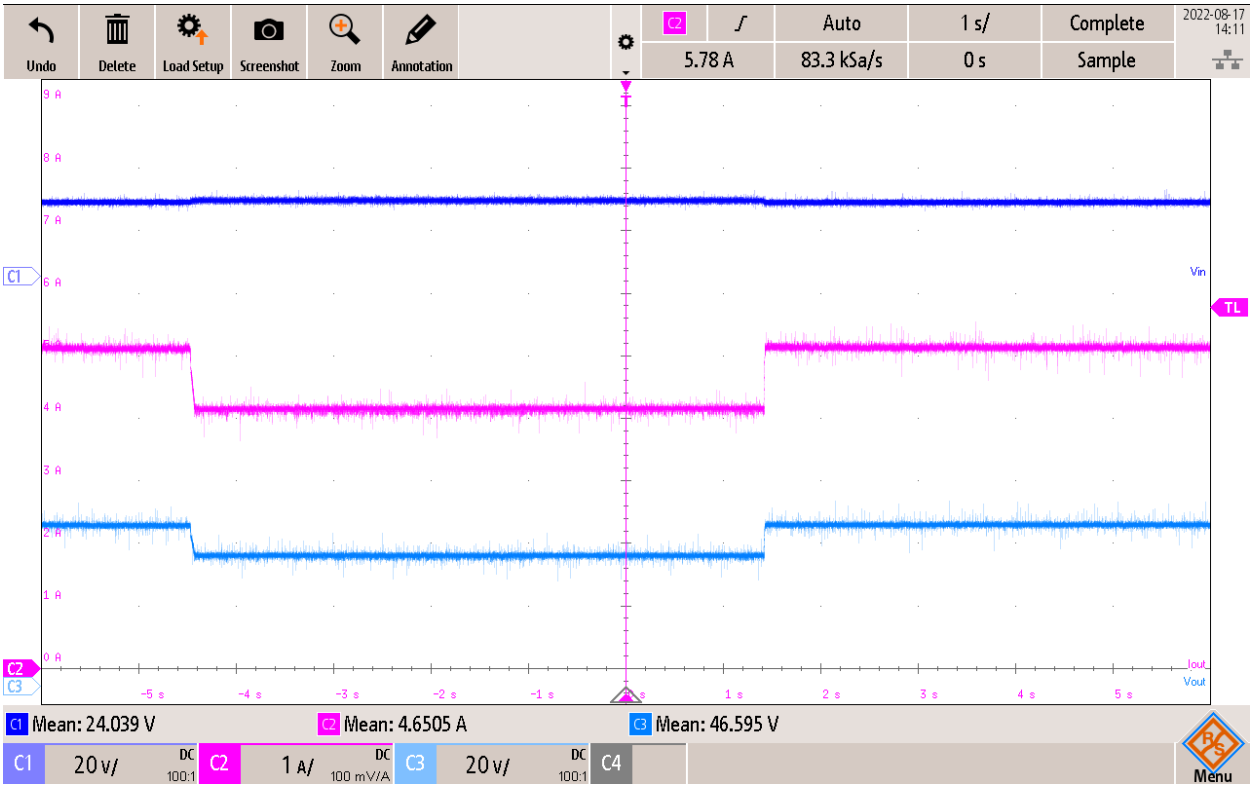

Figure 4- 12 Experimental results with input voltage 24 V in Boost mode.
C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage

Figure 4-13 illustrates the experimental results tested with 36 V input voltage (C1 in blue color) in Buck-Boost mode. One can see that the output current (C2 in pink color) tracks the reference current signal changing from 5 A to 4 A and then to 5 A, presenting fast dynamic responses at the step-down and step-up current transitions. The output current shows small current ripples and the output voltage (C3 in light blue color) has the same changing tendency as the output current. With the experimental results of the closed-loop test in both Boost and Buck-Boost modes, the output

current tracks the reference signal very well and presents fast dynamic responses. So the designed digital controller works as expected.

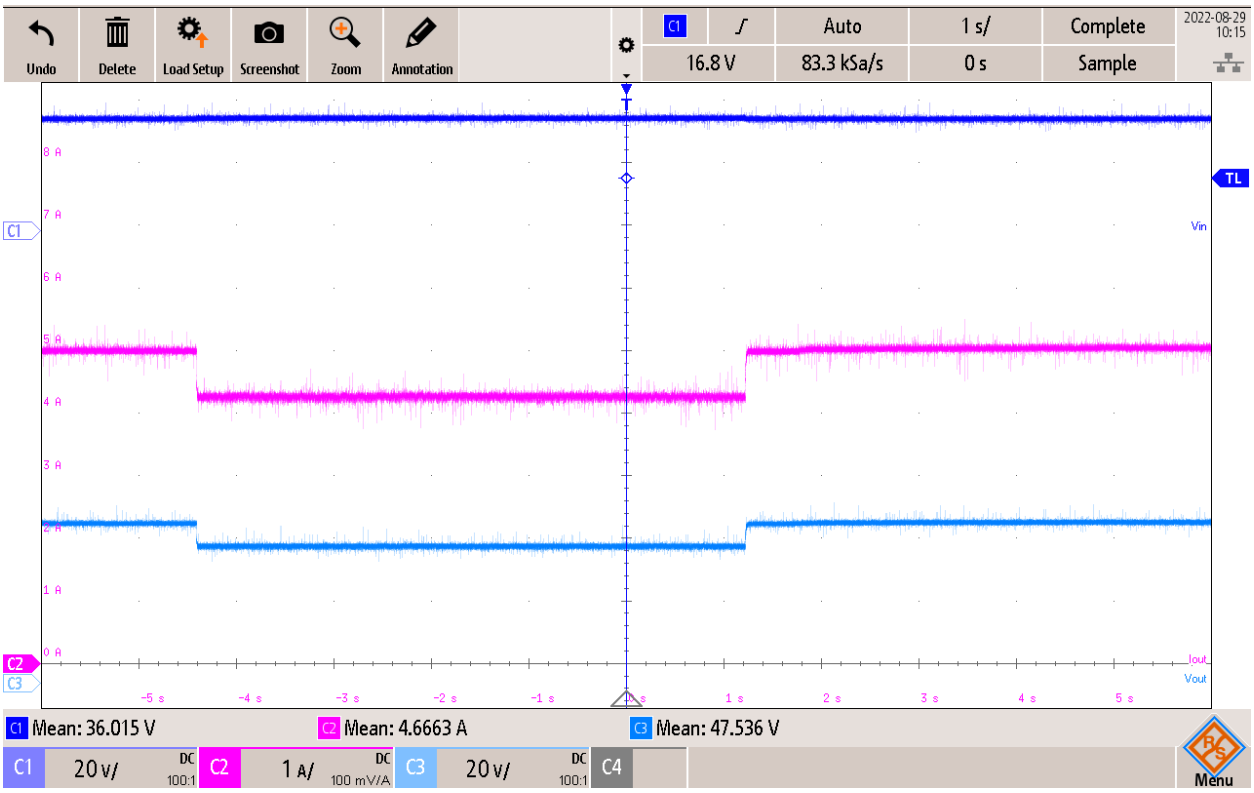

Figure 4- 13 Experimental results with input voltage 36 V in Buck-Boost mode.
C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage

4.2.4 Mode transition logic test

The mode transition logic is tested with a constant input voltage. The DC power supply is set to supply a constant input voltage at 33 V for the converter, and a 10.11 Ω resistor is connected to the output of the converter. The reference output current is set at 5 A, so the output voltage will be 50.55 V. The value of signal BorBB is set to change between 0 and 1 by using a square wave voltage source with frequency 0.1 Hz, 0.5 duty cycle, DC offset equaling 0 and V_{peak_peak} equaling 1. In this way, the mode of operation can change between Boost mode (Mode 11) and Buck-Boost mode (Mode 13). The value of the Mode of operation subtracted by 11 is sent to the digital output of F28335, with a high value of "1" as Mode 13, and a low value of "0" as Mode 11.

Experimental results without the smooth mode transition logic are shown in Figure 4-14. One can see that the input voltage (C1 in blue color) is about 33.197 V, with the mode of operation (C4

in green color) changing from Mode 13 to Mode 11 and then back to Mode 13 (variable value of C4: 1-0-1). The output current (C2 in pink color) has a mean value of 4.9518 A but presents large current spikes at the mode transitions, and the output voltage (C3 in light blue color) also has large voltage variations at the mode transitions. One can see the values of the current variations at the transitions in Figure 4-15 and Figure 4-16. When the mode changes from Buck-Boost mode to Boost mode in Figure 4-15, the output current increases sharply from around 5 A to about 6.9 A, then back to about 5 A after 25 ms. And when the mode changes from Boost mode to Buck-Boost mode in Figure 4-16, the output current decrease sharply from around 5 A to about 2.1 A, then back to about 5 A after 25 ms. Therefore, without the smooth mode transition logic, when the mode changes between Boost and Buck-Boost modes, the output voltage and output current present large voltage/current spikes at the mode transitions, which cause power losses and might damage devices.

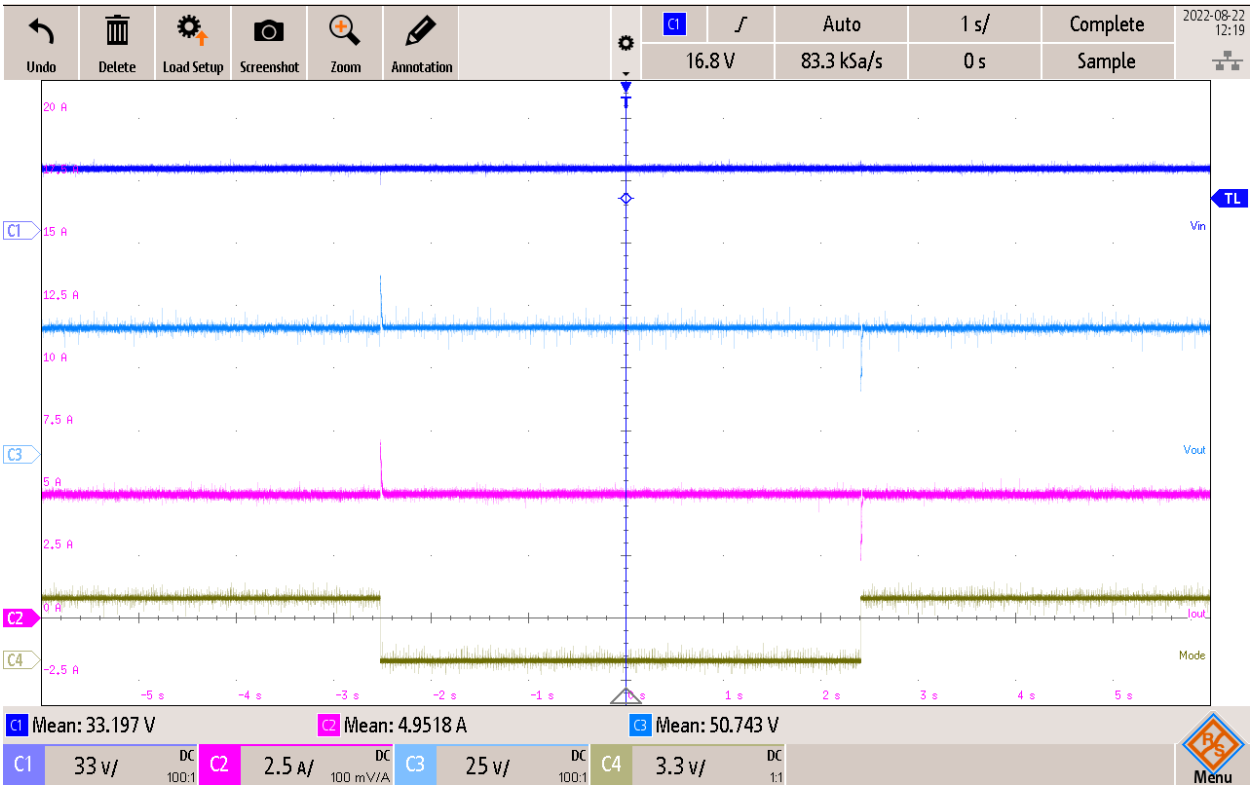

Figure 4- 14 Experimental results without smooth mode transition logic. C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage, C4 (green): from Mode 13(high value) to Mode 11(low value) to Mode 13

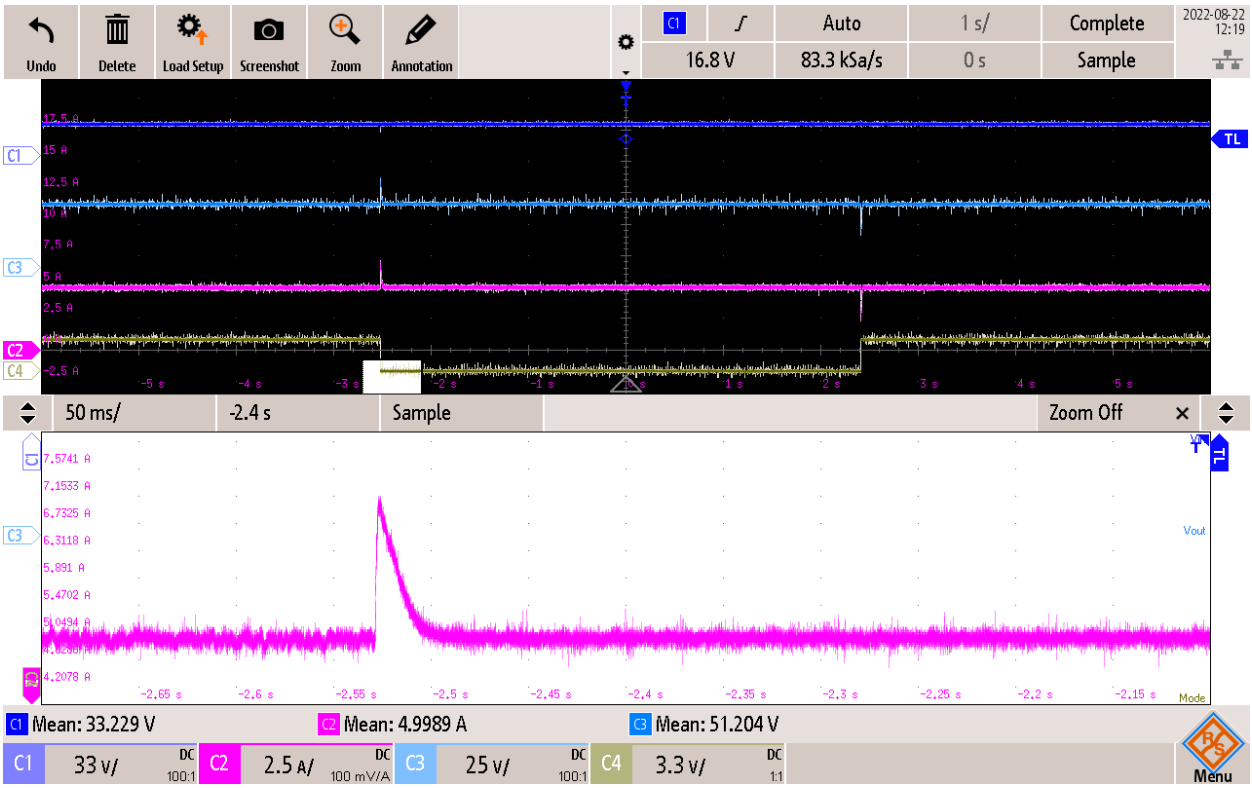

Figure 4- 15 Output current variation without smooth mode transition logic. C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage, C4 (green): Mode 13 (high value) and Mode 11 (low value)

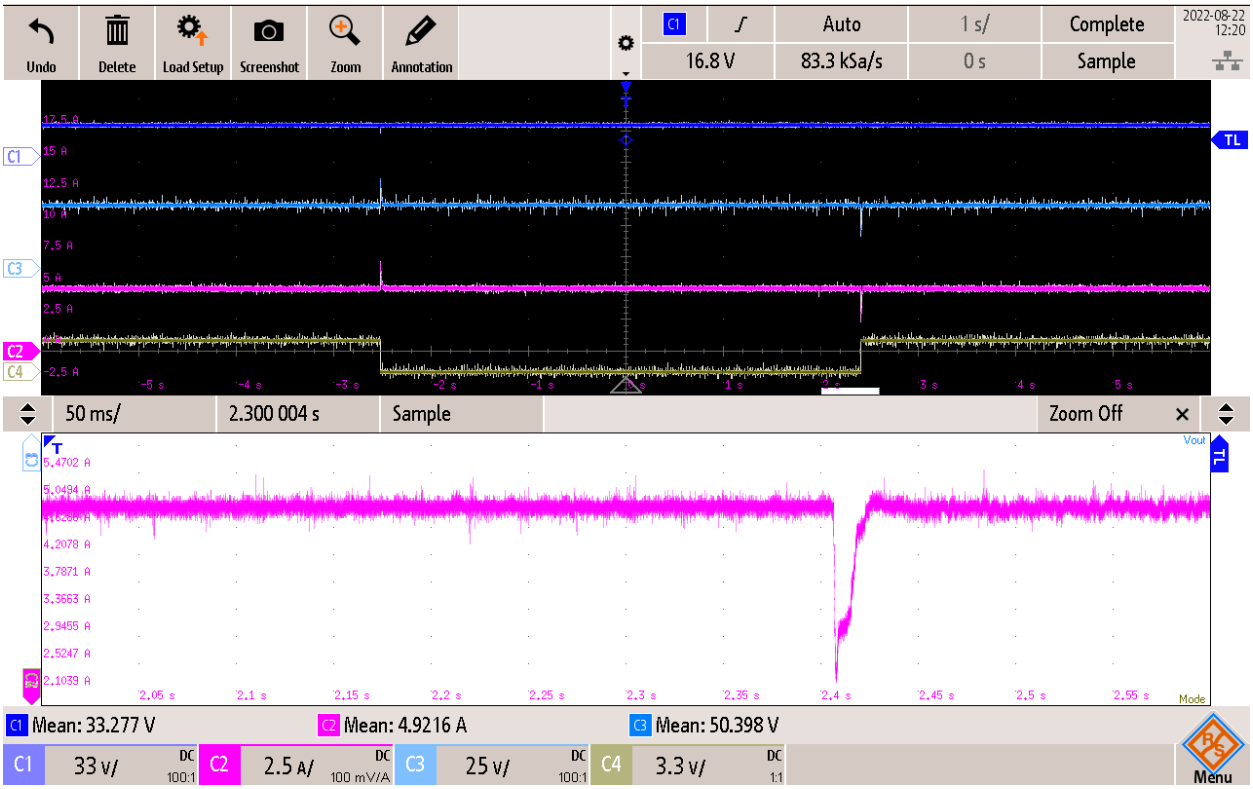

Figure 4- 16 Output current variation without smooth mode transition logic. C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage, C4 (green): Mode 13 (high value) and Mode 11 (low value)

After adding the smooth mode transition logic, experimental results are presented in Figure 4-17, Figure 4-18, and Figure 4-19. In Figure 4-17, one can see that the input voltage (C1 in blue color) is about 33.039 V, with the mode of operation (C4 in green color) changing from Mode 13 to Mode 11 and then back to Mode 13 (variable value of C4: 1-0-1). The output current (C2 in pink color) has a mean value of 5.0372 A, with a very tiny current variation at the transition from Mode 13 to Mode 11, and the output voltage (C3 in light blue color) has the same changing tendency. One can see the variation of the output current at the transition from Buck-Boost mode to Boost mode in Figure 4-18. It changes a little, from around 5 A to about 5.4 A, then back to about 5 A very quickly, and when the mode changes from Boost mode to Buck-Boost mode in Figure 4-19, the output current presents a very tiny current variation that can be neglected. Therefore, the smooth mode transition logic works very well when the mode changes between Boost and Buck-Boost modes, the output current present presents tiny current variations at mode transitions.

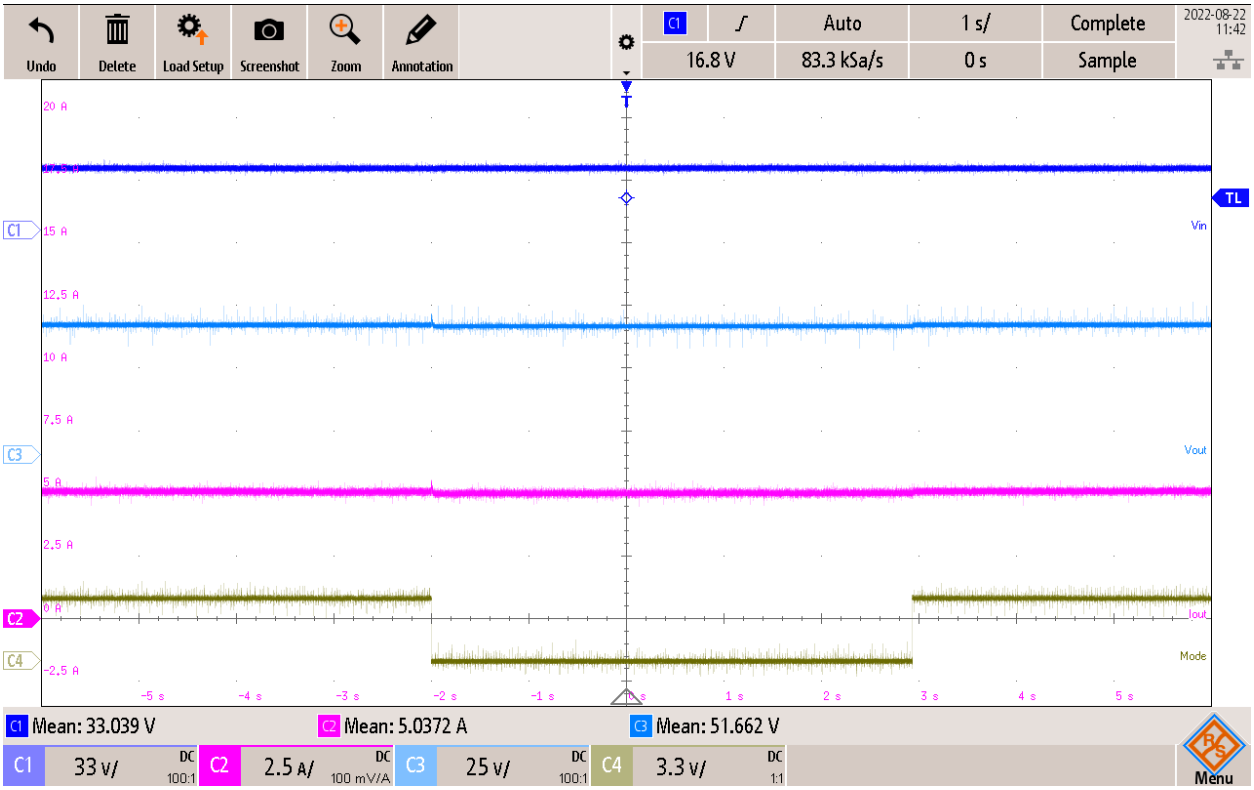

Figure 4- 17 Experimental results with smooth mode transition logic. C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage, C4 (green): from Mode 13 (high value) to Mode 11 (low value) to Mode 13

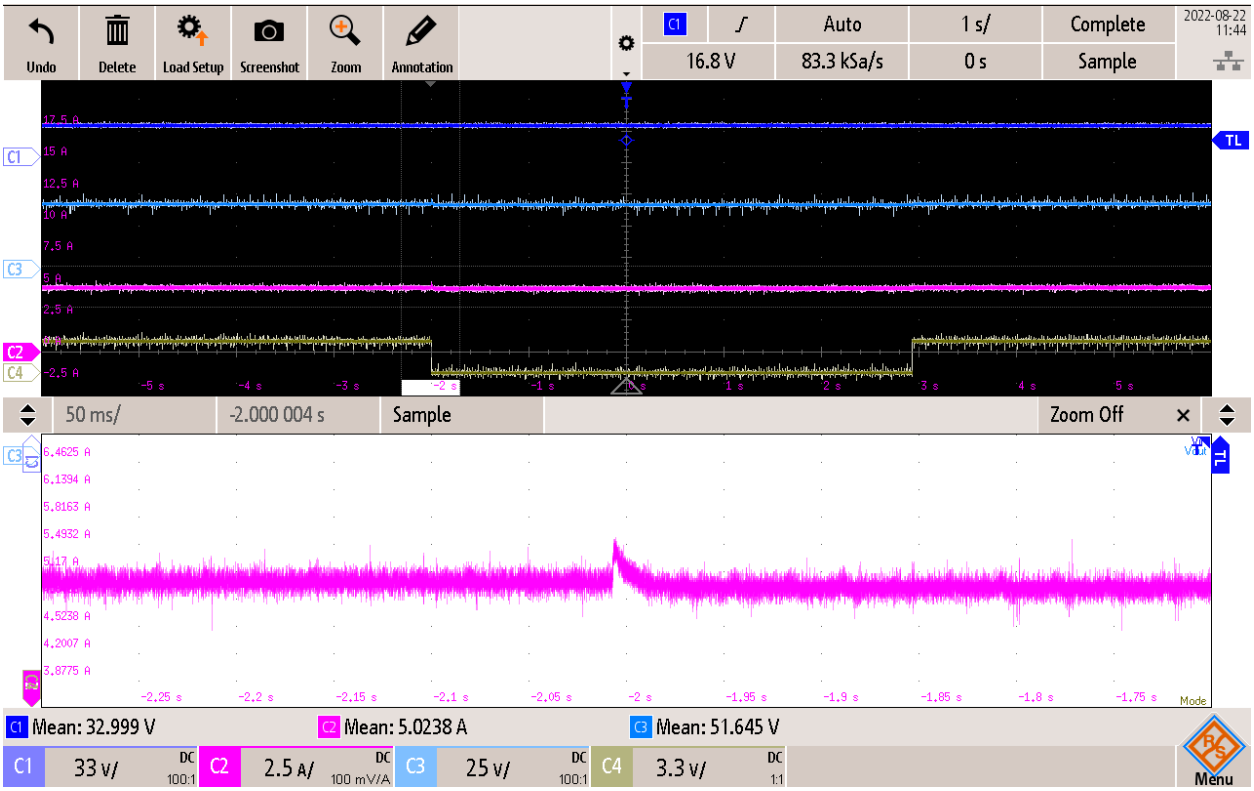

Figure 4- 18 Output current variation with smooth mode transition logic. C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage, C4 (green): Mode 13 (high value) and Mode 11 (low value)

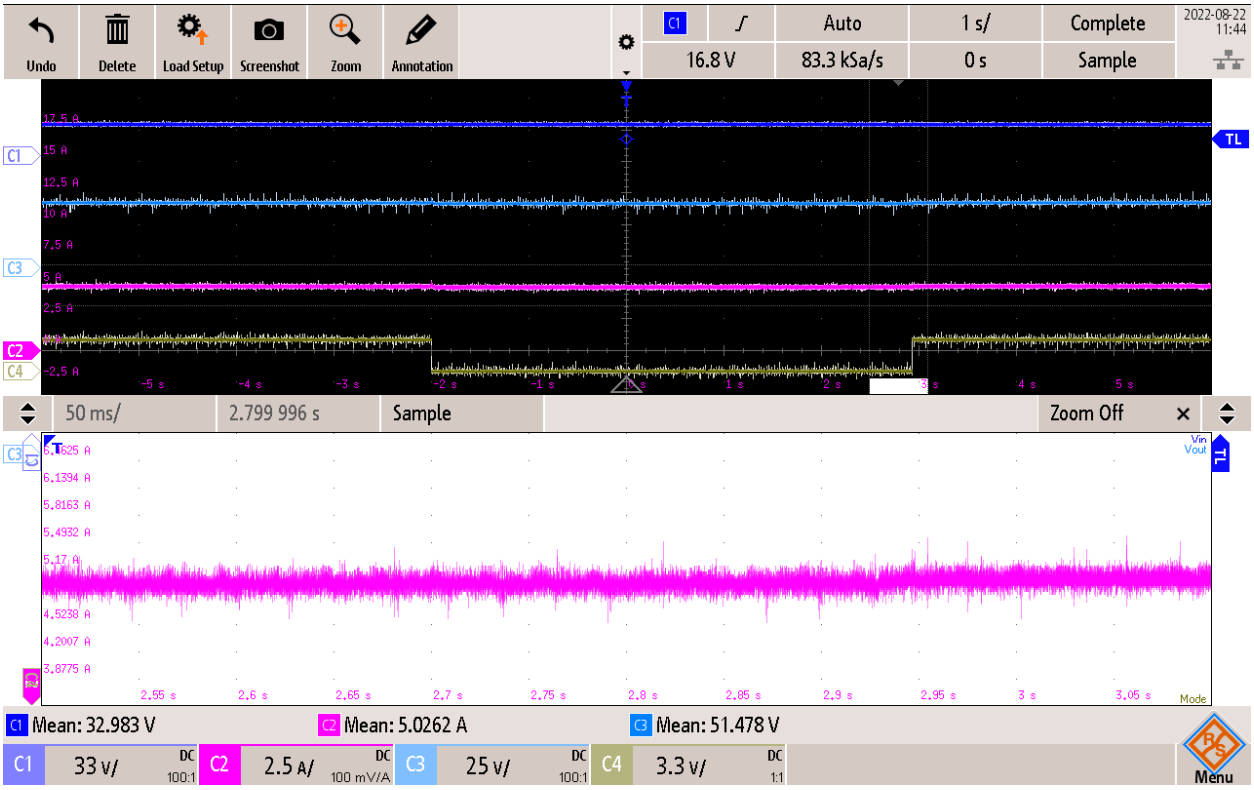

Figure 4- 19 Output current variation without smooth mode transition logic. C1 (blue): input voltage, C2 (pink): output current, C3 (light blue): output voltage, C4 (green): Mode 13 (high value) and Mode 11 (low value)

4.3 A supercapacitor test

Two 16 V 58 F supercapacitors (SCs) from Maxwell are connected in series to get an equivalent 32 V 29 F capacitance. Based on its datasheet, the limits for the input voltage protection are set as 14 V and 26 V. To test the bidirectional control of the output current with the converter interfacing SC with varying voltage, a DC power supply paralleled with a 5.6 Ω resistor through a diode is used at the output. Before the test, the SCs are charged to 14.5 V. Considering safety charging, and discharging of the SC and also presenting the experimental results with more details, the reference output current is set as +/- 1 A. Thus the voltage of the SC is expected to change between 14 V and 26 V because of the input voltage protection logic. Besides, as the SC voltage changes, the mode of operation of the converter should change between Boost and Buck-Boost modes.

Figure 4-20 presents the experimental results with reference current of -1 A, what should lead to the supercapacitor to charge, increasing its voltage. In the figure, one can see that the output voltage (C2) is set constant, and the output current (C3) changes from 0 A to -1 A and tracks the reference current at -1 A. Thus the SCs are charged and the input voltage (C1) increases from minimum voltage (14 V) to maximum (26 V). The mode (C4) changes from Boost mode to Buck-Boost as the input voltage increases. The output current ripple changes when the mode of operation changes. When the input voltage reaches the "overvoltage protection" limit of 26 V, the input voltage protection logic works to prevent the input voltage going higher. Thus, the voltage of SC keeps stable at 26 V with an output current equal to 0 A from 120 s on, in the figure.

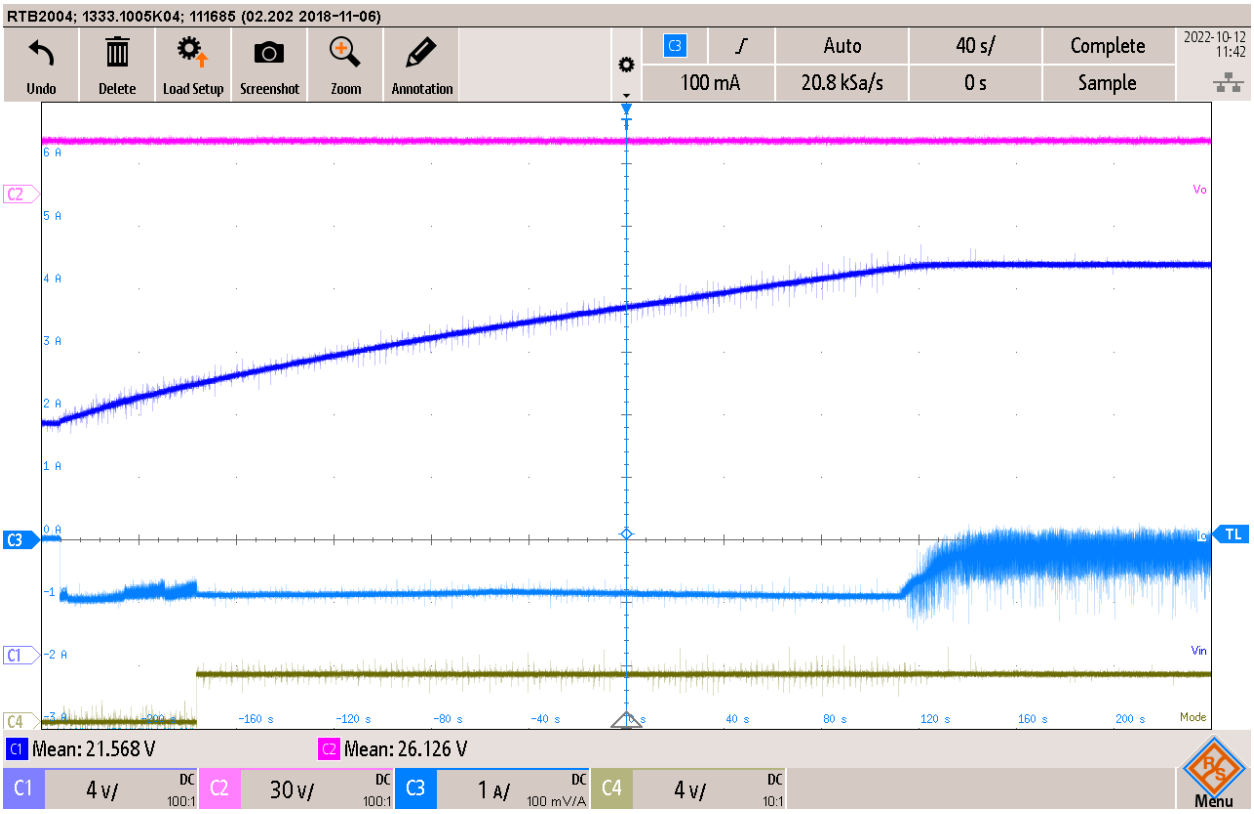

Figure 4- 20 Experimental results of the converter with varying input voltage for -1 A reference current. C1 (blue): input voltage, C2 (pink): output voltage, C3 (light blue): output current, C4 (green): Buck-Boost mode (high value) and Boost mode (low value)

Figure 4-21 presents the experimental results with reference current of 1 A, what should lead to the supercapacitor to discharge, decreasing its voltage. In the figure, one can see that the reference current, and the output current (C3) change from 0 A to 1 A and the converter operates in Buck-Boost mode. As the SCs discharge and the input voltage (C1) decreases, the mode of operation (C4) changes from Buck-Boost mode to Boost mode. There is a tiny current variation at the mode transition. When the input voltage decreases to the "undervoltage protection" limit of 14 V, the input voltage protection logic works to prevent the input voltage from going lower, from 80s on, in the figure.

From Figure 4-20 and Figure 4-21, the output current tracks the reference current +/- 1 A well, and the voltage protection logic works fine to prevent the SC voltage from going too high or too low. With the smooth mode transition logic, the converter operates in Boost and Buck-Boost modes with small current variations when the mode changes. The output current presents ripples tracking 0 A when the input voltage protection logic works, which could be the future work to improve the experimental performance of the protection logic.

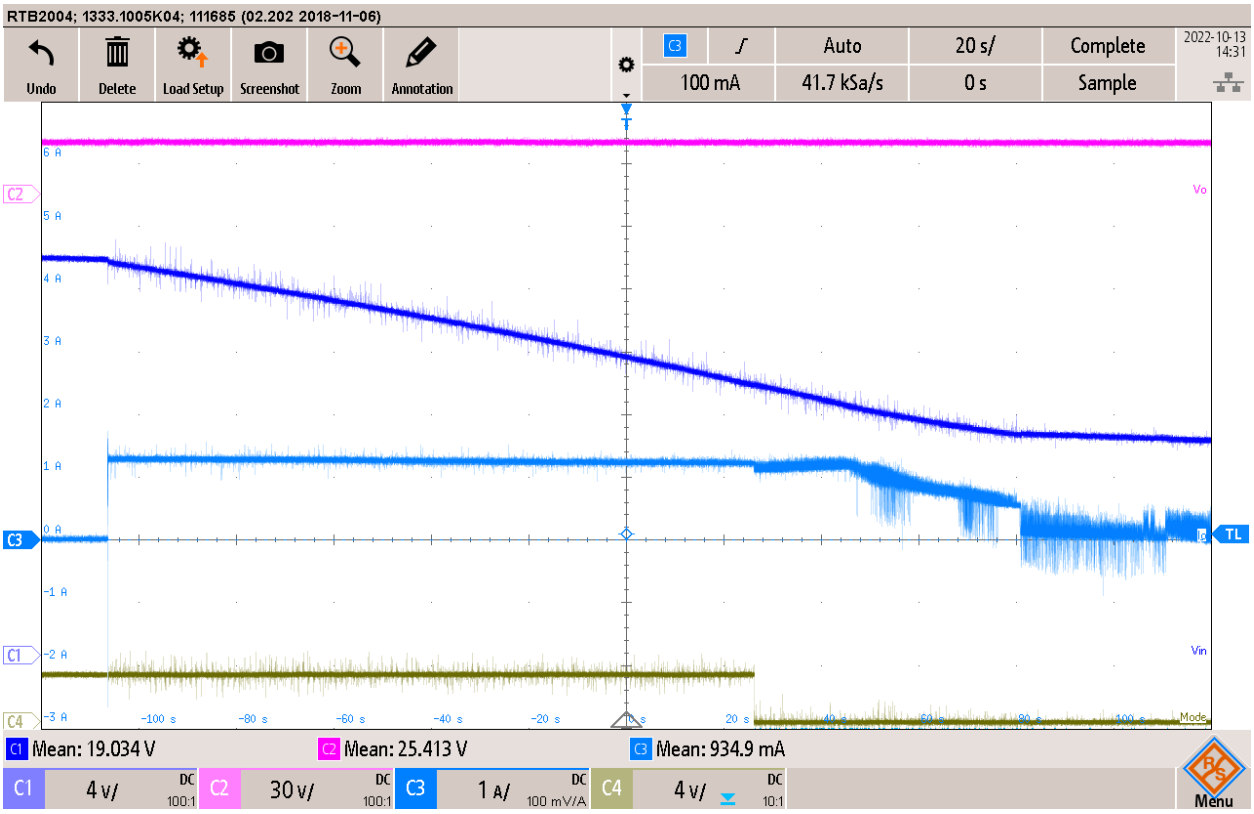

Figure 4- 21 Experimental results of the converter with varying input voltage for 1 A reference current. C1 (blue): input voltage, C2 (pink): output voltage, C3 (light blue): output current, C4 (green): Buck-Boost mode (high value) and Boost mode (low value)

4.4 Summary

Chapter 4 presents the experimental setup, and several experimental tests are discussed. The impact of the phase shift is presented and validated. The gating signals for the four modes of operation are checked first. Open loop test and closed-loop test for the converter operating in Boost and Buck-Boost modes are presented, showing that the digital controller regulates the output current to track the reference current very well with tri-state logic. With a constant voltage of 33 V input voltage for positive 5 A reference output current, the smooth mode transition logic is tested by changing the mode between Mode 11 and Mode 13. One observes less current variations when the mode changes compared with the experiment results without using the smooth mode transition logic. The experimental results of the converter connecting SCs to a DC source illustrate the capability of bidirectional power flow control of the converter with tri-state logic operating with a wide input voltage range. Lastly, that the input voltage protection logic works fine.

Chapter 5 Conclusions

5.1 Summary

This thesis presented a control scheme for a 4-switch bidirectional DC-DC converter for interfacing a supercapacitor to a 48 V DC bus. In order to eliminate the Right-Half Plane zero from the transfer function relating the output current/voltage to the duty cycle, a tri-state control logic with an inductor current free-wheeling segment/state is employed. This, on the other hand, leads to a multi-variable control problem which can be circumvented with a fixed value for one of the three "states", in this case, D_{off}. However, this action reduces the voltage range for which the converter can operate in the Boost and Buck-Boost modes. This is a significant drawback in cases such as the one considered in this work, where the input/supercapacitor voltage is expected to vary in a relatively wide range, from rated to half rated. The solution is to identify when the mode of operation needs to be changed and come up with a logic that allows such changes with minimum impact on the output/injected current. This has been achieved in this work along with a suitable modulation scheme and digital control scheme that has been implemented in a DSP. Simulation results are presented and validate the smooth mode transition logic and the space vector modulation scheme. Moreover, a designed digital controller and several different peripherals of a TI-DSP (F28335) are used, and its performance is verified by means of simulation and experimental tests.

In Chapter 2, the implementation of the 4-switch bidirectional DC-DC converter with tri-state logic for interfacing a supercapacitor to a DC grid is presented. Calculations were made for the required intermediate inductor and capacitors for the converter. Since the primary goal of the converter is to control the injected/absorbed current at +/-5 A when the converter operates in Boost and Buck-Boost modes, a space vector modulation scheme, and a single duty cycle control scheme with a PI controller are designed to achieve the primary goal. The converter with tri-state logic and fixed D_{off} presents a simpler control loop design and faster transient response than the conventional dual-state control scheme as demonstrated by means of PSIM simulation.

With the fixed value of D_{off}, the input voltage range becomes narrow, in Chapter 3, a smooth mode transition logic is discussed and presented to solve this issue, so that the converter could change modes between Boost and Buck-Boost modes when the input voltage varies in a wide range, with a tiny current variation, compared to without using the smooth mode transition logic.

An input voltage protection logic is presented to prevent the supercapacitor from over-charging and over-discharging. The performance of the converter connecting a supercapacitor to the DC grid with the smooth mode transition logic and input voltage protection logic is validated and presented with several PSIM simulation tests. A digital controller is designed with parameters in a setup for experiment by using direct digital approach. Preliminary simulations of the final experimental tests are done and presented with the designed digital controller and ePWM blocks of the TI-DSP F28335 in PSIM.

In Chapter 4, the experimental set-up is presented, and some experimental tests are shown and discussed for the smooth mode transition logic. The experimental results are very similar to those in the simulation verification. The results show that the ePWM blocks used for the four switches generate accurate gating signal waveforms based on different modes of operation. With a constant voltage 33 V DC supply, the mode of operation is changed between Mode 11 and Mode 13 for positive 5 A reference output current. It presented much improved results in the experimental tests compared to without using the smooth mode transition logic. Overall, the main goal of this thesis was to regulate the output current at the set value when the bidirectional DC-DC converter interfaces a supercapacitor to a DC bus with tri-state logic, operating in Boost and Buck-Boost mode with a wide input voltage range. The experimental results of the converter connecting a SC to a DC source shows that the main goal is achieved.

5.2 Future work

As future work, the following is suggested:

1) In this work, the proposed space vector modulation scheme was not implemented in experimental verification since it involves the hardware CPU bandwidth of the DSP F28335 and managing the interrupt service routine of the various tasks. One of the potential future developments can be to implement the space vector modulation scheme in hardware for experimental verification.
2) A scheme for connecting the 4-switch converter to a DC bus smoothly. There, the output voltage of the converter is adjusted to the voltage of the DC bus prior to closing a DC breaker/switch so as to avoid high current transients.
3) Include droop based and current limiting control loops for the current injected by the supercapacitor interface into the DC bus, along with other distributed energy resources.

Bibliography

[1] A. M. Gee, F. V. P. Robinson and R. W. Dunn, "Analysis of Battery Lifetime Extension in a Small-Scale Wind-Energy System Using Supercapacitors," in *IEEE Transactions on Energy Conversion*, vol. 28, no. 1, pp. 24-33, March 2013, doi: 10.1109/TEC.2012.2228195.

[2] S. Teleke, L. Oehlerking and M. Hong, "Nanogrids with energy storage for future electricity grids," *2014 IEEE PES T&D Conference and Exposition*, 2014, pp. 1-5, doi: 10.1109/TDC.2014.6863235.

[3] B. Wang, M. Zarghami and M. Vaziri, "Energy management and peak-shaving in grid-connected photovoltaic systems integrated with battery storage," *2016 North American Power Symposium (NAPS)*, 2016, pp. 1-5, doi: 10.1109/NAPS.2016.7747844.

[4] Z. Cabrane, M. Ouassaid and M. Maaroufi, "Management and control of the integration of supercapacitor in photovoltaic energy storage," *2017 International Conference on Green Energy Conversion Systems (GECS)*, 2017, pp. 1-6, doi: 10.1109/GECS.2017.8066128.

[5] S. K. Kollimalla, M. K.Mishra and N. L. Narasamma, “Design and Analysis of Novel Control Strategy for Battery and Supercapacitor Storage System,” in *IEEE Transactions on Sustainable Energy*, Vol. 5, No. 4, Oct. 2014, pp. 1137-1144.

[6] H. Wang and J. Zhang, "Research on charging/discharging control strategy of battery-super capacitor hybrid energy storage system in photovoltaic system," *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 2694-2698, doi: 10.1109/IPEMC.2016.7512723.

[7] U. Manandhar, N. R. Tummuru, S. K. Kollimalla, A. Ukil and G. H. Beng, "Validation of Faster Joint Control Strategy for Battery- and Supercapacitor-Based Energy Storage System," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3286 - 3295, 2018.

[8] K. Viswanathan, R. Oruganti, and D. Srinivasan, “A Novel Tri-State Boost Converter with Fast Dynamics,” in *IEEE Transactions on Power Electronics*, Vol. 17 No. 5, Sep. 2002, pp. 677-683.

[9] F. Caricchi, F. Crescimbini, F. G. Capponi and L. Solero, “Study of a Bidirectional Buck-Boost Converter Topologies for Application in Electrical Vehicle Motor Drives,” in *IEEE Applied Power Electronics Conference and Exposition*, Feb. 1998, pp. 287-293.

[10] A. Choubey and L. A. C. Lopes. "A Tri-State 4-Switch Bidirectional Converter for Interfacing Supercapacitors to DC Micro-Grids." In *2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1-6. IEEE, 2017.

[11] M. He, F. Zhang, J. Xu, P. Yang and T. Yan, "High Efficiency Two-Switch Tri-State Buck-Boost Power Factor Correction Converter with Fast Dynamic Response and Low-Inductor Current Ripple," *IET Power Electron*, 2013, Vol. 6, Iss. 8, pp. 1544-1554.

[12] D. Boroyevich, R. Brasov, I. Cvetkovic, D. Dong, R. Burgos, F. Wang, and F. Lee, "Future electronic power distribution systems: A contemplative view," in *Proc. 12th IEEE International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, May 2010, pp. 1369–1380.

[13] Broday, Gabriel R., Gilney Damm, William Pasillas-Lépine, and Luiz A. C. Lopes. 2021. "A Unified Controller for Multi-State Operation of the Bidirectional Buck–Boost DC-DC Converter" *Energies* 14, no. 23: 7921. https://doi.org/10.3390/en14237921.

[14] Y. Duan and H. Jin, "Digital controller design for switchmode power converters," *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, 1999, pp. 967-973 vol.2, doi: 10.1109/APEC.1999.750486.

[15]G. Abbas, J. Gu, U. Farooq, A. Raza and M. U. Asad, "Problems in constructing a discrete-time controller using frequency response plots in w-plane," *2017 International Symposium on Wireless Systems and Networks (ISWSN)*, 2017, pp. 1-6, doi: 10.1109/ISWSN.2017.8250012.

[16] K. Viswanathan, R. Oruganti, and D. Srinivasan, "A Dual-Mode Control of Tri-state Boost Converter for Improved Performance," in *IEEE Transactions on Power Electronics*, Vol. 20 No. 4, Jul. 2005, pp. 790-797.

[17] I. Aharon, A. Kuperman and D. Shmilovitz, "Analysis of Dual-Carrier Modulator for Bidirectional Noninverting Buck-Boost Converter," in *IEEE Transactions on Power Electronics*, Vol. 30, No. 2, Feb. 2015, pp. 840-848.

[18] Katsuhiko Ogata, "Discrete-Time Control Systems", Pearson Education, 2nd edition, 2002, ISBN: 8178083353, 9788178083353.

[19] Shutoshkumar Choubey, “A tri-state 4-switch bidirectional converter for interfacing supercapacitors to DC nano-grids”. Master’s thesis, Concordia University.

[20] Powersim Inc, “SimCoder-User-Manual”, July 2019. [Online]. Available: https://powersimtech.com/wp-content/uploads/2021/01/SimCoder-User-Manual.pdf, [Accessed 02 September 2021].

[21] Texas Instrument, “TMS320F2833x, TMS320F2823x Digital Signal Controllers (DSCs)”,

February 2021. [Online]. Available: https://www.ti.com/lit/ds/symlink/tms320f28235.pdf?ts=1657331716333, [Accessed 02 September 2021].

[22] Muhammad Ali Akbar, “Shunt Connected Power Conditioner with Energy Storage for a Hydrogen Fuel Cell System Supplying a DC Nanogrid”. Master’s thesis, Concordia University.

[23] Texas Instrument, "LM5170 48V-12V Bidirectional Converter Evaluation Module," 5 December 2016. [Online]. Available: LM5170EVM-BIDIR Evaluation board | TI.com. [Accessed 13 October 2021].

[24] Powersim Inc, “Auto Code Generation for F2803X Target”, August 2017. [Online]. Available:https://psim.powersimtech.com/hubfs/PDF%20Tutorials/Embedded%20Code%20Gen/Tutorial-Auto-Code-Generation-for-F2803x-Target-11.1.pdf. [Accessed 2 June 2021].

Appendix

An interface power conditioning circuit [22] shown in Figure 1 is used to process the voltage and current sensors' signals to the DSP.

The analog output voltage signals of the voltage sensor and current sensor are very weak with long wires transmission to DSP. The interface power conditioning circuit is used between sensors and DSP to avoid long wires transmission and protect the signals from noise as much as possible and limit the signals in the input range of the DSP F28335 (0 – 3 V).

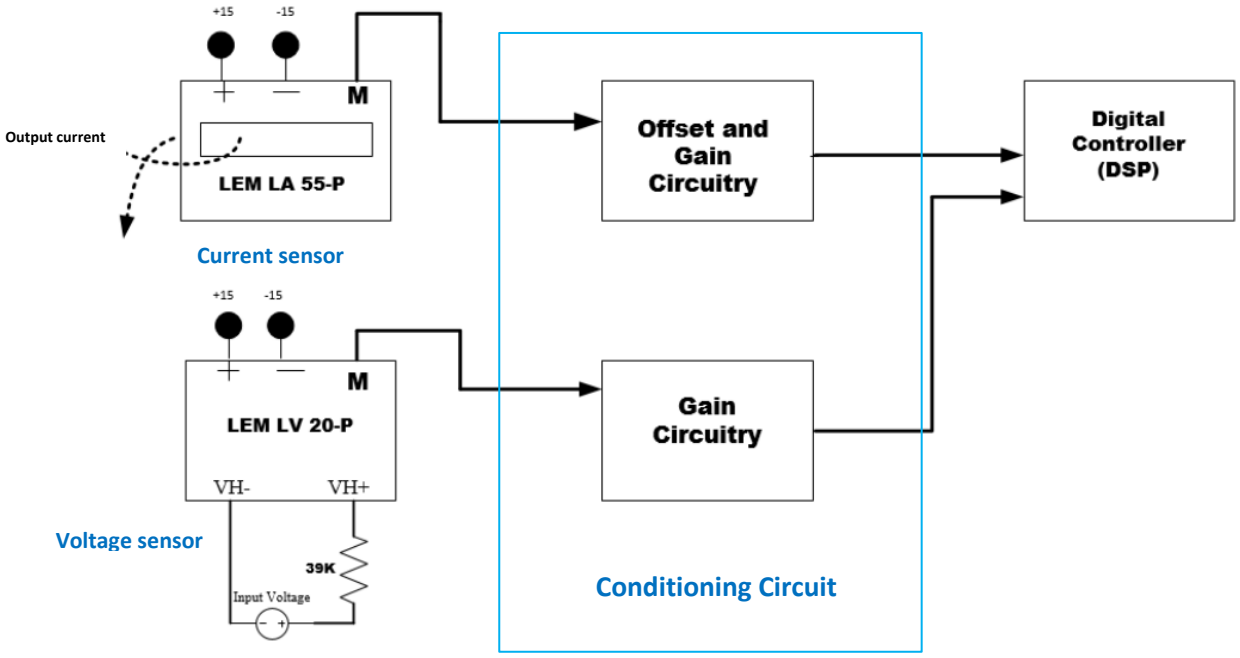

Figure 1 The interface power conditioning circuit

The analog output voltage signal of the output current could be positive or negative, it is processed and sent to the conditioning circuit that contains a unity gain voltage op-amp circuit and an offset of 1.5 V provided by a resistor voltage divider.

Figure 2 shows the unity gain circuit for current sensors. The transfer function of this op-amp circuit is:

$$V_o = \left[\frac{Z_1+R_2}{R_2}\frac{Z_4}{Z_4+R_3}V_2\right] - \frac{Z_1}{R_2}V_1 \qquad (1)$$

With $R_1 = R_2 = R_3 = R_4$, this equation can be simplified as

$$V_o = V_2 - V_1 \quad (2)$$

Where the value of V_1 is 1.5 V, provided by a resistor voltage divider. In equation (2), V_o equals to V_{in} , the gain of the amplifier is unity. This unity amplifier could isolate the input side of the circuit from the output side completely.

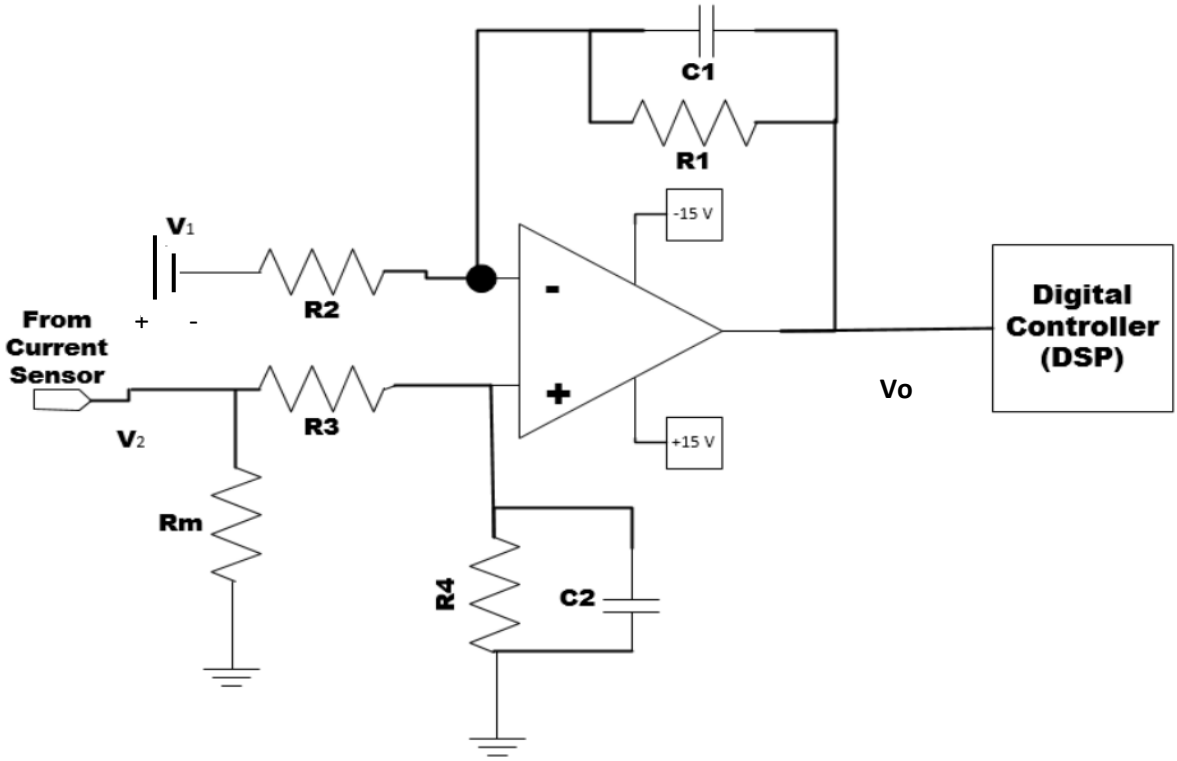

Figure 2 Unity gain circuit for current sensor

The unity gain circuit for voltage sensor is similar to the one for current sensor, replacing the 1.5 V with ground. The resistors and capacitors that are being used in unity gain circuit for current sensor are given in the Table 1 and in unity gain circuit for voltage sensor are given in Table 2.

Table 1 Parameters for current sensor measurement and unity gain offset circuitry

C1(pF)	C2(pF)	R1(Ω)	R2(Ω)	R3(Ω)	R4(Ω)	Rm(Ω)
820	820	39 k	39 k	39 k	39 k	100

Table 2 Parameters for voltage sensor measurement and unity gain circuitry

C1(nF)	C2(nF)	R1(Ω)	R2(Ω)	R3(Ω)	R4(Ω)	Rm(Ω)
2.2	2.2	22 k	22 k	22 k	22 k	100