Efficient Computational Methodologies for Multi-Objective Optimization of Distributed Energy Resources (DER) Inverters

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A Thesis

In the Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy (Electrical and Computer Engineering)

at

Concordia University

Montreal, Quebec, Canada.

February 2023

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ABSTRACT

Efficient Computational Methodologies for Multi-Objective Optimization of Distributed Energy Resources (DER) Inverters

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Concordia University, 2023.

The paralleling of power converters connected to the grid for power-sharing is a widely used technique. In this context, the design framework for a low-cost, lightweight, compact, and high-performance optimum configuration is an open research problem. This thesis proposes an innovative Multi-Objective Hierarchical Optimization Design Framework (MO-HO-DF) for an Alternating Current (AC) grid interface with N interleaved H-bridges, each with M parallel "to-be-determined" switches, connected through coupling inductances (L_f). A total of eight Figures of Merit (FOMs) were identified for the design framework optimization. A rigorous model of the power electronic system is presented. Next, a highly computationally efficient algorithm for the estimation of the required frequency modulation ratio (m_f) to meet current harmonic performance requirements for any given configuration is proposed. Then, the concept and implementation of the algorithm are presented for the MO-HO-DF. The effectiveness of the design optimization framework is demonstrated by comparing it to a base case solution. Finally, the design calculations are validated via Piecewise Linear Electrical Circuit Simulation (PLECS) software with manufacturer-provided Three-Dimensional (3D) power semiconductor models that include thermal modelling.

In particular, when an H-bridge is interfaced with a single-phase grid, it requires controllers to regulate the voltages and currents in the system. In this context, the static optimization of controllers responsible for Direct Current (DC) bus voltage regulation and AC regulation, considering time-domain and frequency-domain behaviours, is an open research problem. Firstly, this thesis proposes a method to obtain FOMs with the use of inbuilt functions in MATLAB software. Then for the Type-II Proportional+Integral (PI) controller, a single-variable two-objective convex optimization is proposed. Next, for the Proportional+Multi-Resonant (PMR) controller, three-variable five-objective convex optimization is proposed. The design of the PMR controller is a multi-variable problem that can inherit the principles of a hierarchical framework and leverage the effect of a design variable on the final optimization result. Thus, the work on PMR controller design optimization is extended to a three-level hierarchical design framework and evaluates all six possible paths for optimization. Finally, enhanced macro-model-based MATLAB simulation results are provided to verify the performance of controller designs and generate statistical insights.

Thesis Supervisor: Dr. Luiz Antonio Correa Lopes
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ACKNOWLEDGEMENT

I express my heartfelt gratitude to my thesis supervisor, Dr. Luiz Lopes, a world-renowned expert in Power electronics, High power converters, and Distributed generation, for providing me with guidance, motivation, and encouragement to accomplish this research work. It is truly an honour and privilege to work with him. This thesis work would not have been possible without his trust in me and allowing me to work under his supervision. I gratefully acknowledge the financial support provided: FRS bursaries, NSERC Discovery grants, and Teaching Assistantships. I thoroughly enjoyed the Power electronics-II course work, most importantly, the never to miss assignments and lecture tasks. I also take time to remember how on many occasions, he helped me despite his busy schedules, specifically concerning the review of research work to meet the timelines of my Ph.D. program.

I am grateful to Dr. Rastko Selmic for being a great support and providing mentorship from the beginning of my Ph.D. program. He was always available to clarify doubts, and most importantly the simple examples provided to understand the concepts in multi-agent control systems were impressive. On several occasions, he offered the best possible help to succeed in my Ph.D. Program.

I am thankful to Dr. Mina Yazdanpanah for her clarity in teaching and patiently clearing doubts, which made it easier to succeed in digital signal processing coursework.

I am grateful to my department chair, Dr. Yousef Shayan, for being very kind and helpful. His positive outlook and administrative support really helped me to succeed in my Ph.D. Program. All I can say, he is the best department chair.

I am thankful to Dr. Walter Lucia for his constructive feedback during the Ph.D. Proposal exam, specifically on convex optimization.

I am grateful to Dr. Kash Khorasani, a world-renowned expert in control, optimization, and artificial intelligence, for his constructive feedback and for sharing his expert opinion on my Ph.D. Seminar report. I am truly humbled for sharing his valuable time, despite his busy schedule, to provide inputs to enhance my Ph.D. thesis.

I am grateful to Dr. Ambrish Chandra, a world-renowned expert in power distribution and renewable energy systems, for accepting to be an external examiner of my Ph.D. thesis. It is truly an honour and privilege that my Ph.D. thesis is examined by him.

I am thankful to the Department of Electrical and Computer Engineering's office staff Ms. Tatyana Bobrova (Department Administrator), Ms. Sheryl Tablan (Graduate Program Coordinator), and Ms. Audrey Veilleux (Graduate Program Coordinator) for their professionalism and courteous responses whenever help was needed.

I am thankful to Concordia University for providing the Concordia University International Tuition award of excellence so that I can study at a low school fee. Special thanks to

Dr. Akshay Rathore for recommending me for this award and for admission to the Ph.D. Program with financial support. Specifically, with my socioeconomic background, it would have been impossible to come to Canada without this financial support. I also want to thank Dr. Akshay Rathore for accepting, with a great heart, my wish to work under the supervision of Dr. Luiz Lopes.

I am grateful to the Government of Canada and the Government of Quebec for providing financial assistance through various social schemes.

I also express my heartfelt gratitude to my M.Tech. Thesis supervisor at the Indian Institute of Technology Kanpur, Dr. Shyama P. Das, who in 2010 provided me with the rarest and brightest opportunity of doing an M.Tech. Thesis in the three-phase Photovoltaic grid integration. A journey in his Static Control laboratory was the most intellectually transformative one.

I am extremely grateful to my teachers from the Indian Institute of Technology Kanpur, Dr. Shyama P. Das, Dr. Parthasarathi Sensarma, Dr. Santanu K. Mishra, Dr. S. C. Srivastava, Dr. Ram Prasad Potluri, and Dr. Saikat Chakrabarti for their inspiring quality of research thought leadership, and imparting state of the art knowledge through their valuable teachings. Their teachings have laid a strong foundation in the research domains of Power Electronics, Electrical Machine Drives, Power Systems, and Control Systems.

I also express my sincere thanks to my immediate senior in my undergraduate (B.E.) days, Dr. Venkata Srinivas Kadagala, who encouraged me for higher studies and provided me with mentorship and guidance, which boosted my academic excellence. Specifically, with his guidance, I could get hold of the right textbooks at Sir Sarvepalli Radhakrishnan Bhavan (Library) at my institute campus and prepared my own notes for many of the undergraduate subjects in electrical and electronics engineering.

I sincerely thank the entire Tata Steel family for providing me with great opportunities, coaching, mentorship, sponsorship, and inculcating Leadership with strong business core ethics and values.

Dedicated to

My Mother, Venkata Ratnamma Vaddipalli (née Najana)

My Father, Venkata Naidu Vaddipalli.

Golden dreams
Scars that are as deep as the heart
are hidden in the River of Life.

Even if the Hills and Creeks come in the way
Even if the Valleys split it into half
The River of Life will never stop
The River of Life will never tire.

- Translated lyrics of the Telugu-language song "Jeva Nadhi" (River of Life),
Baahubali: The Beginning (2015).

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Nomenclature

$\mathbb{N}$	Natural numbers.
$f(x)$	Deterministic component of the probabilistic model.
$2\omega_c$	3dB bandwidth of PR controller.
$4NM$	Total number of switches in the power conversion system.
$\boldsymbol{\beta_r}$	A row vector of $\mathbf{V}$, representing three variables: k_i, k_p, and ω_c.
$\boldsymbol{\gamma_r}$	A weight matrix used in finding the best controller parameters of PMR controller, with NLWC method.
$\boldsymbol{\kappa_r}$	A weight matrix used in finding the best controller parameters of PMR controller, with LWC method.
$\boldsymbol{\lambda_v}$	Weight vector of FOMs, with LWC method, for the Type-II PI controller to regulate DC bus voltage.
$\boldsymbol{\omega_c}$	Set of all values of ω_c, considered in the PMR controller design.
$\boldsymbol{\phi_g}$	A column matrix containing the phase angles of the fundamental component of output AC for cases #3 to #16.
$\boldsymbol{\phi_{ng}}$	A column matrix containing the phase angles of the fundamental component of output AC for cases #19 to #32.
$\boldsymbol{\sigma_r}$	Weight vector of FOMs, with LWC method, for the PMR controller to regulate output AC.
$\boldsymbol{\sigma_v}$	Weight vector of FOMs, with LWC method, for the Type-II PI controller to regulate output AC.
Δi	Current loop tracking error.
ΔT_{ch}	Amount of temperature rise in the junction of the switch due to $R_{th,ch}$.
ΔT_{ha}	Amount of temperature rise in the junction of the switch due to $R_{th,ha}$.
ΔT_{jcf}	Amount of temperature rise in FWD device due to $R_{th,jcf}$.

ΔT_{jcr} Amount of temperature rise in REV device due to $R_{th,jcr}$.

Δv Voltage loop tracking error.

δv Absolute value of dead-time compensation voltage, v_{dt}.

ΔV_{dc} Voltage ripple across the DC bus capacitor.

δ Phase angle of H-bridge output voltage.

ϵ Random error of the probabilistic model.

η Power conversion efficiency.

$\hat{I}$ DC component of grid current, obtained via linearized small signal modelling.

$\hat{I}_{pv}$ DC component of PV Array current, obtained via linearized small signal modelling.

$\hat{P}_g$ DC Component of instantaneous AC power delivered to the grid.

$\hat{U}_g$ DC component of grid voltage, obtained via linearized small signal modelling.

$\hat{V_{dc}}$ DC component of DC bus voltage, obtained via linearized small signal modelling.

λ A variable used in generating different weight combinations for FOMs, in a Type-II PI controller design.

λ_{01x} Weights of FOMs in f_{01}, where $x \in 1, 2, 3, 4$.

λ_{02x} Weights of FOMs in f_{02}, where $x \in 1, 2$.

λ_{xyi} Composite objective function weights, $\forall x \in (1, 4), y \in (1, 2)$ and $i \in \mathbb{R}$, where x, and y refer to the number of the Level and the number of the objective function, respectively.

$\mathbb{R}$ Real numbers.

$\mathbb{R}^n$ Set of n-tuples of Real numbers.

$\mathbb{W}$ Whole numbers.

$\mathbf{E_1}$ A column matrix containing the composite Normalized FOM value, in a Type-II PI controller design, for different weight combinations obtained using the LWC method.

$\mathbf{E_2}$ A column matrix containing the composite Normalized FOM value, in a Type-II PI controller design, for different weight combinations obtained using the NLWC method.

$\mathbf{K_0}$ A vector containing best controller parameters and the corresponding FOMs, obtained for a PMR controller, to regulate output AC, designed with NLWC method.

$\mathbf{k_i}$ Set of all values of k_i, considered in the PMR controller design.

$\mathbf{K_n}$ A vector containing best controller parameters and the corresponding FOMs, obtained for a PMR controller, to regulate output AC, designed with NLWC method, for the Path#n, where $n = \{1, 2..6\}$.

$\mathbf{k_p}$ Set of all values of k_p, considered in the PMR controller design.

$\mathbf{N_x}$ A matrix containing Type-II PI controller FOMs, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop Type-II PI controller transfer function.

$\mathbf{R_0}$ A vector containing best controller parameters and the corresponding FOMs, obtained for a PMR controller, to regulate output AC, designed with LWC method.

$\mathbf{R_g}$ A column matrix containing the maximum resonant gain of the open loop transfer function of the current loop, for the cases involving the PMR controller.

$\mathbf{R_n}$ A vector containing best controller parameters and the corresponding FOMs, obtained for a PMR controller, to regulate output AC, designed with LWC method, for the Path#n, where $n = \{1, 2..6\}$.

$\mathbf{S_{x1}}$ A vector containing best controller parameters and the corresponding FOMs, obtained for a Type-II PI controller, designed with LWC method, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$\mathbf{S_{x2}}$ A vector containing best controller parameters and the corresponding FOMs, obtained for a Type-II PI controller, designed with NLWC method, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$\mathbf{V}$ A matrix, where each row contains values of k_i, k_p, and ω_c in three different columns.

$\mathbf{x_1}$ A column matrix containing the percentage overshoot of output current for a change in the reference command signal at t=0.5s, for all 32 cases.

$\mathbf{x_2}$ A column matrix containing the designed value of overshoot for a unit step-input, for all 32 cases.

$\mathcal{C}_i(\phi_{mi}, \boldsymbol{\lambda_i})$ Convex hull, with LWC method, for the Type-II PI controller to regulate output AC.

$\mathcal{C}_i(\phi_{mi}, \boldsymbol{\sigma_i})$ Convex hull, with NLWC method, for the Type-II PI controller to regulate output AC.

$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\lambda_r})$ Convex hull, with LWC method, for the PMR controller to regulate output AC.

$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\sigma_r})$ Convex hull, with NLWC method, for the PMR controller to regulate output AC.

$\mathcal{C}_v(\phi_{mv}, \boldsymbol{\lambda_v})$ Convex hull, with LWC method, for the Type-II PI controller to regulate DC bus voltage.

$\mathcal{C}_v(\phi_{mv}, \boldsymbol{\sigma_v})$ Convex hull, with NLWC method, for the Type-II PI controller to regulate DC bus voltage.

$\mathcal{F}_{xn}(\phi_{mx})$ Normalized FOM of Type-II PI controller, where $n \in \{1, 2\}$, $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$\mathcal{G}_n(\boldsymbol{\beta_r})$ Normalized FOM of PMR controller, where $n \in \{1, 2, 3, 4, 5\}$.

$\mathcal{L}(x, \lambda, \mu)$ Lagrangian function.

μ Population mean.

∇ Gradient operator.

ω_0 The frequency at which PR controller's magnitude peak is obtained.

ω_1 Fundamental frequency in radians per second.

ω_l, ω_h Location of poles in a Type-II PI controller.

ω_l Location of zero for in a Type-II PI controller.

ω_s Switching frequency in radians per second.

ω_{gcr} Gain cross-over frequency of $G_i(s)H_r(s)$.

ω_{gcx} Gain cross-over frequency of $G_x(s)T_{2x}(s)$, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

ω_{hx} High-frequency pole of Type-II PI controller transfer function, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

ω_{lx} Low-frequency pole of Type-II PI controller transfer function, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$\overline{V_{dc}}$ Average voltage across the DC bus capacitor.

ϕ Phase angle of the grid current with respect to the grid voltage.

ϕ_{mr} Phase margin of $G_i(s)H_r(s)$.

ϕ_{mx} Phase margin of $G_x(s)T_{2x}(s)$, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$\psi_1(t)$ Phase of the H-bridge output voltage.

ρ Correlation coefficient.

σ Population standard deviation.

$\mathbf{C}$ Constant value of design variable.

$\mathbf{O}$ Optimized value of design variable.

$\mathbf{V}$ Variable that is varied in a Level of optimization.

.xml eXtensible Markup Language file.

THD_i^* Theoretical value of THD_i obtained for a grid current of I^*.

C1P1 Case#1 and Path#1 of the optimization.

C1P2 Case#1 and Path#2 of the optimization.

C2P1 Case#2 and Path#1 of the optimization.

C2P2 Case#2 and Path#2 of the optimization.

C3P1 Case#3 and Path#1 of the optimization.

C3P2 Case#3 and Path#2 of the optimization.

C4P1 Case#4 and Path#1 of the optimization.

C4P2 Case#4 and Path#2 of the optimization.

Cost Total cost of PSDs and coupling inductances.

C$ Price in Canadian Dollars.

M Million.

ode23tb(stiff/TR-BDF2) Implicit Runge-Kutta formula with a first stage that is a trapezoidal rule step and a second stage that is a backward differentiation formula of order 2.

ode8(Dormand-Prince) Eighth-order Dormand-Prince formula to compute the model state at the next time step as an explicit function of the current value of the state and the state derivatives approximated at intermediate points.

powergui Environment block for Simscape Electrical Specialized Power Systems models.

pValue Probability of obtaining test results at least as extreme as the result actually observed, under the assumption that the null hypothesis is correct.

$\tilde{i}(s)$ Small perturbation component of grid current.

$\tilde{u}_g(s)$ Small perturbation component of grid voltage.

$\tilde{v}_{ab}(s)$ Small perturbation component of PV-fed H-bridge output voltage.

$\tilde{V}_{dc}$ Small perturbation component of DC bus voltage.

ξ Lagrange multiplier.

ζ Damping factor of the RC snubber design.

A_{sink} Area of the heat sink with an aluminum fin thickness of 2mm.

B_η Ratio of computation time with the LWC method to computation time with the NLWC method, for a given multi-objective convex optimization problem.

boost Phase boost obtained with a Type-II PI Controller.

C Convex set.

C_p Parasitic capacitance of IGBT.

C_s Snubber circuit capacitance.

C_{bc} Base-Collector capacitance of IGBT.

C_{be} Base-Emitter capacitance of IGBT.

C_{ce} Collector-Emitter capacitance of IGBT.

C_{dc} DC bus capacitance.

C_{os} Output capacitance of IGBT.

$D(s)$ Second-order polynomial in the denominator of $H_1(s)$.

d_i Euclidean distance.

DW Test statistic for the Durbin-Watson.

E Energy to handled by the coupling inductance.

E_c Maximum energy to be handled by the DC bus capacitor.

E_{abs} Energy to be stored by the DC bus capacitor.

E_{del} Energy to be delivered by the DC bus capacitor.

E_{off} Turn-off energy loss.

E_{on} Turn-on energy loss.

E_{rr} Reverse recovery energy loss.

f_1 Fundamental frequency in Hz.

F_r Ringing frequency of the voltage across the IGBT, during the turn-off.

f_s Switching frequency of the H-bridge.

f_{01} Normalized composite FOM, with cost functions of coupling inductance and price of PSD, corresponding to 8 best solutions.

f_{02} Normalized composite FOM, with cost functions related to the required cooling effort and efficiency of power conversion, corresponding to 8 best solutions.

f_{x1} Normalized composite objective function in Level-x, $\forall\ x \in (1,2,3,4)$.

f_{x2} Normalized composite objective function in Level-x, $\forall\ x \in (1,2,3,4)$.

$f_{xn}(\phi_{mx})$ FOM of Type-II PI controller, where $n \in \{1,2\}$, $x \in \{i,v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$G_i(s)$ Transfer function of current loop.

$g_n(\boldsymbol{\beta_r})$ FOM of PMR controller, where $n \in \{1,2,3,4,5\}$.

$G_v(s)$ Transfer function of voltage loop.

G_x Gate terminal of the switch S_x, where $x \in \{1,2,3,4\}$.

g_x Gate signal to be applied at G_x of the switch S_x, where $x \in \{1,2,3,4\}$.

$H_i(s)$ Transfer function of current loop controller.

$H_n(s)$ Transfer function of the PR controller to track the frequency $n\omega_0$, where n is the order of the harmonic.

$H_r(s)$ Transfer function of the PMR controller.

$H_v(s)$ Transfer function of voltage loop controller.

$H_1(s)$ Transfer function of PR controller.

$H_{rKn}(s)$ PMR controller transfer function with the controller parameters in $\mathbf{K}_n$, where $n = \{1,2..6\}$.

$H_{rRn}(s)$ PMR controller transfer function with the controller parameters in $\mathbf{R}_n$, where $n = \{1,2..6\}$.

$i(t)$ Grid current.

I RMS current through the inductor.

$I_{\mathrm{h,max}}$ Maximum value of harmonic amplitudes of grid current.

I^* Reference value for grid current.

I_s Grid current obtained in the PLECS simulation.

$I_{av,f}$ FWD average current of the switch.

$I_{av,r}$ REV average current of the switch.

i_{dc} H-bridge input current.

I_g RMS grid current.

I_{hl} Magnitude of a harmonic component.

i_{pv} PV Array output current.

i_{ref} Current to be regulated by the current loop controller.

$I_{rms,f}$ FWD RMS current of the switch.

$I_{rms,r}$ REV RMS current of the switch.

I_{rms} H-bridge output RMS current.

I_{test} Test current of the PSD to measure energy loss.

$iN(t)$ Ouput current of N^{th} H-bridge, in a scheme of N parallel H-bridges.

$j_v\,(z)$ v^{th} Bessel function of the first kind.

k_2 Proportional gain of the Type-II PI controller.

k_i Integral gain of the PR controller/PMR controller.

k_p Proportional gain of PR controller/PMR controller.

k_{2x} Proportional gain of Type-II PI controller transfer function, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

L_e Internal emitter inductance of IGBT.

L_f Coupling inductance.

L_p Circuit stray inductance of IGBT.

$L_\$$ FOM of Coupling inductance: Cost/Price.

L_v FOM of Coupling inductance: Volume.

L_w FOM of Coupling inductance: Weight.

M Number of parallel PSDs.

$m_a(t)$ Amplitude modulation signal.

m_a Amplitude modulation index.

m_f Frequency modulation ratio.

$m_{a,min}$ Minimum value of amplitude modulation index.

m_{pr} Percentage overshoot of the unity feedback transfer function of $G_i(s)H_r(s)$, subjected to a unit step input.

m_{px} Percentage overshoot of the unity feedback transfer function of $G_x(s)T_{2x}(s)$, subjected to a unit step input, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$N(s)$ Second-order polynomial in the numerator of $H_1(s)$.

N Number of parallel DER inverters.

$P(t)$ Real Power.

P Price of the coupling inductance.

p_g Instantaneous AC power delivered to the grid.

p_{ac} Total power on the AC side of PV-fed H-bridge.

P_{cl} Conduction power loss.

p_{dc} Total power on the DC side of PV-fed H-bridge.

P_F Single switch power loss in FWD.

P_{loss} Power losses in the H-bridges and Coupling inductances.

P_R Single switch power losses in REV.

P_{sw} Switching power loss.

pdc_ϕ The amount of phase angle advance for the modulation signal.

$PSD_\$$ Total semiconductor cost/price.

Q_p Quality factor of $1/D(s)$.

Q_z Quality factor of $N(s)$.

Q_{rr} Reverse recovery charge of the diode.

R^2 Explains to what extent the variance of one variable explains the variance of the second variable.

R_c ESR of DC bus capacitor.

R_d On-state resistance of Diode.

R_f Ohmic loss representation of the coupling inductance.

R_g Open loop transfer function's gain in the current loop due to PMR controller at ω_1.

R_s Snubber circuit resistance.

$R_{d,f}$ The inverse slope of the tangent drawn on FWD V-I characteristics of a switch.

$R_{d,r1}$ The inverse slope of the tangent drawn on REV V-I characteristics of a switch.

$R_{d,r2}$ The inverse slope of the tangent drawn on DT V-I characteristics of a switch.

R_{on} On-state resistance of IGBT.

$R_{th,ca}$ Thermal resistance from case to ambient atmosphere.

$R_{th,ch}$ Thermal resistance of the thermal interface material.

$R_{th,haf}$ Required thermal resistance value based on the FWD device.

$R_{th,har}$ Required thermal resistance value based on the REV device.

$R_{th,ha}$ Thermal resistance from heat sink to ambient air.

$R_{th,jcf}$ Thermal resistance of the forward conducting device.

$R_{th,jcr}$ Thermal resistance of the reverse conducting device.

$R_{th,jh}$ Thermal resistance from PSD's junction to heat sink.

$R_{th,sd}$ Interactive thermal resistance between FWD and REV device.

s variable s in the complex frequency domain/s-domain.

SNx Switch of N^{th} H-bridge, $x \in \{1, 2, 3, 4\}$, in a scheme of N parallel H-bridges.

T_a Ambient air temperature.

T_d Temperature tolerance for the design safety consideration of a heat sink.

t_d Dead-time of two switches in the same leg.

T_j^* The value of junction temperature used in the heat sink design.

T_s Time period of the carrier signal.

$T_{2x}(s)$ Type-II PI controller transfer function, where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop.

$t_{d,off1}$ Turn-off delay time of IGBT at junction temperature 25°C.

$t_{d,off2}$ Turn-off delay time of IGBT at junction temperature 150°C.

$t_{d,off}$ Maximum turn-off delay time of IGBT considering the variation of junction temperature.

$t_{d,on1}$ Turn-on delay time of IGBT at junction temperature 25°C.

$t_{d,on2}$ Turn-on delay time of IGBT at junction temperature 150°C.

$t_{d,on}$ Maximum turn-on delay time of IGBT considering the variation of junction temperature.

t_{dt} Dead-time between two switches of the same leg.

$T_{j,av}$ Actual junction temperature averaged over the fundamental period.

$T_{j,f}$ The junction temperature of the FWD device.

$T_{j,max}$ Maximum junction temperature of the device.

$T_{j,r}$ The junction temperature of the REV device.

t_{off} Switch turn-off delay time.

t_{on} Switch turn-on delay time.

$T_{rKn}(s)$ Unity feedback transfer function of $G_i(s)H_{rKn}(s)$.

$T_{rRn}(s)$ Unity feedback transfer function of $G_i(s)H_{rRn}(s)$.

t_{rr} Rise time of the unity feedback transfer function of $G_i(s)H_r(s)$, subjected to a unit step input.

t_{rx} Rise time of the unity feedback transfer function of $G_x(s)T_{2x}(s)$, subjected to a unit step input.

$u_g(t)$ Grid voltage.

U_g RMS grid voltage (considering fundamental component).

V Volume of the coupling inductance.

v Fundamental component of H-bridge output voltage.

V_d Forward voltage drop of Diode.

V_f Forward voltage drop of IGBT.

$V_{0,f}$ Intercept on the V-axis for the tangent drawn on FWD V-I characteristics of a switch.

$V_{0,r1}$ Intercept on the V-axis for the tangent drawn on REV V-I characteristics of a switch.

$V_{0,r2}$ Intercept on the V-axis for the tangent drawn on DT V-I characteristics of a switch.

$v_{ab}(t)$ Output voltage of PV-fed H-bridge.

V_{dc+} Maximum voltage across the DC bus capacitor.

$V_{dc,min}$ Minimum DC bus voltage.

$v_{dc,ref}$ DC bus reference voltage.

V_{dc-} Minimum voltage across the DC bus capacitor.

V_{dc} DC bus voltage.

v_{dc} DC bus voltage provided as feedback to the voltage loop controller.

v_{dt} Dead-time compensation voltage.

$V_{g,max}$ Maximum gate drive voltage.

$V_{g,min}$ Minimum gate drive voltage.

V_g Gate drive voltage.

V_{sat} On-state voltage drop across the switch.

V_{test} Test voltage of the PSD to measure energy loss.

W Weight of the coupling inductance.

Z_f Coupling impedance.

Acronyms

2DEG 2-Dimensional Electron Gas. 23

3D Three-Dimensional. 50

AC Alternating Current. xviii, 2–8, 11–14, 20, 21, 53, 56, 58, 60, 61, 72, 77, 80, 98, 101, 110–112

AI Artificial Intelligence. 110

AMD Advanced Micro Devices. 93

ARSPWM Asymmetrical Regular Sampled Pulse Width Modulation. 13, 21, 48, 61

BES Bulk Electric System. 1

BPS Bulk Power System. 2

CPU Central Processing Unit. 18, 93

CSP Concentrated Solar Power. 9

DC Direct Current. 2–4, 6–8, 12–14, 18, 21, 54–58, 61, 68, 71, 77, 79, 93, 95, 98, 103

DER Distributed Energy Resources. 1, 2, 4–6, 10, 11, 13, 14, 16, 103, 112

DERA Distributed Energy Resources Aggregation. 2, 4

DT Dead-Time mode. 24

DW test Durbin-Watson test. 27, 28

EK Kelvin Emitter. 23

ESR Equivalent Series Resistance. 53, 55

ESS Energy Storage System. 4, 6, 7, 10, 11, 13, 16, 110, 111

FACTS Flexible Alternating Current Transmission Systems. 3

FFT Fast Fourier Transform. 50

FOM Figure Of Merit. 38

FOMs Figures Of Merit. 16–18, 20, 31, 32, 34, 37–40, 45, 46, 63, 65, 67, 68, 111

FWD Forward mode. 23, 25, 26

GaN Gallium Nitride. 22–25

GDDR Graphics Double Data Rate. 93

GPU Graphics Processing Unit. 93

HEMT High-Electron-Mobility Transistor. 22–25

HVAC High Voltage Alternating Current. 3

HVDC High Voltage Direct Current. 3

i3.0 Industry 3.0. 5, 110, 112, 113

i4.0 Industry 4.0. 5, 6, 12, 110, 112, 113

IEC International Electrotechnical Commission. 4

IEEE Institute of Electrical and Electronics Engineers. 4, 6, 12, 33, 109

IGBT Insulated-Gate Bipolar Transistor. 22, 24, 25, 46, 93, 95–98, 111, 112

IPOSIM Infineon Online Power Simulation Platform. 112

kW kilo Watt. 4

LBC Little Box Challenge. 5

LCL Inductor-Capacitor-Inductor. 112

LTI Linear Time-Invariant. 13, 18, 63

LWC Linear Weight Constraint. xiii, 71–73, 75, 77–84, 87–90, 112

MATLAB MATrix LABoratory. 18, 30, 32, 37, 60, 67, 68, 92, 93, 95–98, 103, 110, 112

MO-CO-DF Multi-Objective Convex Optimization Design Framework. 112, 113

MO-HO-DF Multi-Objective Hierarchical Optimization Design Framework. 17, 46, 110–112

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor. 22–25, 46

MPP Maximum Power Point. 55

MPPT Maximum Power Point Tracking. 6

MW Mega Watt. 4

NERC North American Electric Reliability Corporation. 1

NLWC Non-Linear Weight Constraint. xv, 71–73, 75–84, 87–90, 112

P-V Power-Voltage. 55

PCC Point of Common Coupling. 3, 10

PDC Phase Delay Compensation. 48

PI Proportional+Integral. 13, 14, 17, 18, 58, 61, 63, 64, 68, 71, 74, 75, 77, 79, 80, 90, 92, 94, 101, 103, 104, 110–112

PLECS Piecewise Linear Electrical Circuit Simulation. 17, 18, 47, 48, 50, 51

PMR Proportional+Multi-Resonant. xiii, 14, 17, 18, 58, 60, 61, 65, 67, 68, 72, 74, 75, 83–88, 90, 92–94, 101, 103, 104, 110–112

PR Proportional+Resonant. 58

PSD Power Semiconductor Device. 12, 22, 23, 35, 37–39, 46, 47, 51, 93, 110–112

PSDs Power Semiconductor Devices. 12, 20, 37, 38, 111

PV PhotoVoltaic. 4, 6–11, 14, 18, 53–55, 68, 98, 110, 111

RAM Random-Access Memory. 93

RES Renewable Energy Sources. 4, 5, 13

REV Reverse mode. 23–26

RMS Root Mean Square. 22

Si Silicon. 22, 24, 25, 46, 111

SiC Silicon Carbide. 22–25, 46

SK Kelvin Source. 23

SPSS Solar Plus Storage System. 6–8

SPWM Sinusoidal Pulse Width Modulation. 21

THD_i Total Harmonic Distortion of Current. xxii, 17, 20, 30, 32, 33, 48, 92, 98, 104

UPF Unity Power Factor. 48, 49, 96

V-I Voltage-Current. 55, 95

VOC Voltage-Oriented Control. 13

Chapter 1

Introduction

> But if you rely upon situational decision-making - if you pursue near-term goals while maintaining the flexibility of changing course if a better STRATEGY or OPPORTUNITY presents itself - you will always be climbing higher. To put a finer point on the Mario Kart Theory of Talent: every vehicle has a chance of winning the race, as long as you operate the vehicle according to its jagged profile.
>
> DR. LARRY TODD ROSE
> *first author of* Dark Horse: Achieving Success Through the Pursuit of Fulfillment*, and the* Leader of the Laboratory for the Science of Individuality at Harvard University.

1.1 Definitions

1.1.1 Bulk Electric System

The following definition of Bulk Electric System (BES) was provided by North American Electric Reliability Corporation (NERC) [1].

All Transmission Elements operated at 100 kV or higher and Real Power and Reactive Power resources are connected at 100 kV or higher. This does not include facilities used in the local distribution of electric energy. Element is defined in the NERC Glossary as: "Any electrical device with terminals that may be connected to other electrical devices such as a generator, transformer, circuit breaker, bus section, or transmission line. An element may be comprised of one or more components."

1.1.2 Distributed Energy Resources

The following definition of Distributed Energy Resources (DER) is provided by NERC [2].

A DER is any resource on the distribution system that produces electricity and is not otherwise included in the formal NERC definition of the BES.

DER includes any non-BES resource (e.g. generating unit, multiple generating units at a single location, energy storage facility, micro-grid, etc.) located solely within the boundary

of any distribution utility, Distribution Provider, or Distribution Provider-under frequency load shedding only, including the following.

1. Distribution Generation
2. Behind The Meter Generation
3. Energy Storage Facility
4. Distributed Energy Resources Aggregation (DERA)
5. Micro-grid
6. Cogeneration
7. Emergency, Stand-by, or Back-Up generation

DER, as defined above, is generally interconnected to a distribution provider's electric system at the primary voltage (≤ 100 kV but > 1 kV) and/or secondary voltage (≤ 1 kV). As such, the effect of aggregated DER is not fully represented in Bulk Power System (BPS) models and operating tools.

1.1.3 Inverter

An apparatus which converts Direct Current (DC) into Alternating Current (AC).

1.2 Evolution of the Electric Grid Infrastructure

1.2.1 Industry 1.0

Industry 1.0 was about mechanization and steam power involving a mechanical wheel. There was no concept of an electric grid by then.

1.2.2 Industry 2.0

> The invention of the wheel was perhaps rather obvious; but the invention of the invisible wheel, made of nothing but a magnetic field, was far from obvious, and that is what we owe to Nikola Tesla.
>
> — Prof. Reginald Kapp
> *Former Professor of Electrical Engineering at University College London.*

The pearl street station [3, 4], the first-ever electricity generating station, was started by Edison in 1882. The pearl street station was a 110 V DC system operated to cater to a limited number of consumers, small loads, and constrained to a small geographical area. The large-scale transmission and distribution of DC power generation were limited. Primarily

due to the line losses and poor voltage regulation. However, pearl street station was seminal to the modern age's large-scale electrification. The inventions of significant contributions in electrical machinery by Nikola Tesla at Westinghouse Electric Corporation to address the distance of transmission have led to power generation with AC. The series of inventions(1880-1890) by Tesla on AC systems and Edison on DC systems, widely known as the "war of the currents", won by Tesla. One of the first-ever built AC generating plants, the Ames Hydro-electric Generating Plant [5], was functional in 1891. A transformer to step up/step down the voltages has enabled the power transmission and interconnection of generation plants to the electric grid. The AC power transmission has limitations on cost w.r.to the distance of overhead power transmission and underground cable transmission required for connecting regions separated by water. The first-ever High Voltage Direct Current (HVDC) transmission [6] was reported in 1882 by Oskar Von Miller, though it didn't see much development during this era, it later turned out be the effective solution to the problems that originated with long-distance AC transmission.

To summarize, this era started with the DC method of power generation. It was distributed and operated in islanded mode. Then with an AC system, it progressed to a connected generation, transmission, and distribution.

1.2.3 Industry 3.0

> B. Jayant Baliga invented [7] the insulated gate bipolar transistor (USP4969028, USP5998833), a semiconductor power switch that has reduced gasoline consumption by 10% and improved electrical energy efficiency by more than 40%. A tiny chip that controls energy usage, the IGBT is used in household appliances, cars, solar panels, fluorescent lighting, medical equipment, bullet trains, and more.
>
> *upon induction into the National Inventors Hall of Fame in 2016.*

The third industrial revolution started around 1970, known as the digital revolution. Developments in power semiconductor technology contributed to the growth of power electronics applications for the electrical grid infrastructure. The critical applications around the 1980s include Flexible Alternating Current Transmission Systems (FACTS) [8, 9] and HVDC [10, 11]. HVDC mainly addresses the technical challenges with High Voltage Alternating Current (HVAC) transmission over a length. i.e. capacitance issues with underground cable transmission and inductance issues with overhead line transmission. FACTS improved the transmission capability, stability of a power line and power quality at the Point of Common Coupling (PCC).

This rapid growth of power electronics applications and computer-based automation led to increased connectivity among power generation units and improved stability. Hence, increasing the reliability of the electrical grid. However, over time, conventional power generation units, mainly thermal power generation, have contributed to environmental pollution. It led to the summer of 1988 being the hottest on record [12]. Pollution further led to the rise of sea levels due to the melting of the Antarctica ice cap. Hence the voice for action on

global climate change has begun towards the beginning of the 21st century. An international treaty, the Kyoto protocol was signed in 1997 by 41 countries and the European Union to address climate change.

Though Renewable Energy Sources (RES) such as solar or wind were in use at this time, their penetration into the electric grid was inadequate. Thus, many countries worldwide have revised their policies and provided incentives to promote RES. One significant change was to bring deregulation in the electricity markets. For example, low-power grid-connected systems have seen a phenomenal rise due to deregulation in the electricity markets, and complying with standards: Institute of Electrical and Electronics Engineers (IEEE)1547 [13]/International Electrotechnical Commission (IEC)61727.

Another name for solar power is PhotoVoltaic (PV) power. It is because of the principle of PV effect involved in the production of the flow of electrons. PV power can be generated in a few kilo Watt (kW) to Mega Watt (MW) by merely a series or/and parallel combinations of lower-rated PV Panels. Individual users can generate solar power on their rooftops in the order of a few kW. Large PV farms run by corporate utilities generate power of the order of MW. This power can be *integrated* into the electric grid or used in islanded mode. Solar power is a DC, and integration of the same to the AC electric grid or operating in islanded mode to run AC loads would require a power electronic converter: DC/AC Inverter.

Conventional power generation schemes of coal, hydro, and nuclear can use a single synchronous generator to produce AC power rated at a few hundred MW. The typical rating of a unit is anywhere between 500MW to 1500MW. Renewable such as wind, the typical offshore wind turbine size is rated at 2 to 3MW. However, this is not the case with solar power. A PV panel produces about 100W to 200W, and one would need many of them to be connected in series to increase the open-circuit voltage and parallel to increase the short-circuit current rating of the PV Array. Thus multiple DC/AC Inverters of a few kW can be used to interface a total of 1 MW or higher to the AC electric grid in a PV power station. It gives rise to the concept of DER integration into the grid. The aggregated formation of DER units as a single virtual resource is called DERA. For example, in 2016, California Independent System Operator formed a 4,900MW of DERA, a single virtual resource of the largest size.

In the present thesis introduction, to give an example of DC/AC Inverter usage in a DER system, a PV system with an Energy Storage System (ESS) is selected. However, the DER is not just PV-based or battery-based, it can be a collective of other power generation sources such as wind, biomass, tidal, fuel cell etc. Thus the deployment of DC/AC Inverters for interfacing DER with the electric grid gained importance. This DC/AC Inverter is known as DER Inverter. The conventional AC electric grid, the infinite bus of huge inertia, is now penetrated with a large number of power electronic converters of small inertia

- to harness the maximum power from the source.
- to transfer the power to the electric grid or use it locally (islanded mode).
- to store the energy in batteries or fuel cells.

To summarize, this era saw

- Transmission and distribution technologies to address the improved power flow, improved stability and improved power quality.
- Proliferation of renewable energy sources and energy storage systems followed by a subsequent emphasizing of the need for DER Inverter to interface with the AC grid.

1.2.4 Industry 4.0

> In God we trust, all others must bring data.
>
> — Dr. W. Edwards Deming
> *Electrical Engineer, Statistician and the Chief Architect of Japan's rise to world economic superpower from rock bottom.*

Industry 4.0 (i4.0) started around 2011 and was built on computerization and industrialization, which saw a rise during Industry 3.0 (i3.0). The current era of i4.0 has seen a large number of data-intensive applications for pure data storage or cloud computing. Cloud solutions again need reliable power supplies with well-designed cooling, and these cloud systems are often located in remote locations, running on RES. Hence, leading to the energy-efficient running of data centres.

A company like Google would require a microgrid for itself to run its data center. In 2014, Google announced the Little Box Challenge (LBC) competition with prize money of $1M [14–17]. LBC was a global competition, and a team from Belgium won the prize money. *The gist of the objective is to design a grid-connected inverter of a 2kW rating that is roughly ten times smaller than state-of-the-art while meeting the stringent performance specifications.* To further add to the energy efficiency and use of sustainable energy for data centers, in 2016, Microsoft launched an underwater data center running on off-shore wind power.

The Kyoto protocol was in place since 1997, but it was not successful. Hence Paris Climate Agreement, an international treaty to reduce carbon emissions was signed by 197 countries in 2016. This treaty was not legally binding but of voluntary nature. A large-scale effort for clean energy such as solar got further momentum post this agreement.

If all the current agreements (i.e., pledges), if met by all the members of the United Nations, global warming could only limited by 2.4°C. As the scale of efforts by the members of the United Nations was not sufficient to effectively address climate change, in 2021, at the 26$^{\text{th}}$ United Nations Climate Change Conference held in Glasgow (United Kingdom), it was agreed by all the 197 member nations to further reduce carbon emissions, along with financial support to poor/developing countries for clean energy to limit the global warming by 1.5°C. This conference (i.e., Pledge) is also widely known as 26th Conference of Parties (COP26).

1.2.5 Distributed Energy Resources Inverter

The deployment of DER has seen the rise, and operating them in a microgrid is a favourable situation. However, a large-scale penetration into the existing electric grid would require

standards for its operation to maintain reliability. In 2018, the IEEE Standard for the Specification of Microgrid Controllers IEEE 2030.7-2017 [18] is provided. This specific IEEE standard emphasizes one of the four design principles of i4.0: autonomous operation, and the decentralized control of DER.

The present thesis deals with the design philosophy for parallel DER inverters and philosophy of controller design for a DER inverter, pertinent to the current industrial revolution,i4.0.

The following section explains a specific example of a DER Inverter with PV and ESS. The functionality of the DER Inverter is more than just a bi-directional power transfer. The typical functionalities of DER include

- Primary frequency support (frequency-watt).
- Voltage-Var and Voltage-Watt support.
- Low/ High Voltage and Frequency ride through.
- Reactive power support.

1.3 Applications of Distributed Energy Resources Inverter

The PV array's output power depends on the temperature and irradiance. The Maximum Power Point Tracking (MPPT) algorithm extracts the peak power available from the PV array. A DC optimizer is a DC/DC converter with MPPT. Similarly, the PV inverter is a DC/AC inverter with MPPT. A DC optimizer would require a DC/AC Inverter to interface it to the AC grid. A PV Inverter involves a single-stage of power conversion.

A grid-connected PV system is required to supply the power as per the dispatch requirement. Since the maximum power delivered by a PV array varies by the atmospheric conditions, it is essential to have battery storage to

- Store the excess power, when the PV array's output is above the dispatch requirement.
- Supply the deficit power when the PV array's output is below the dispatch requirement.

In a PV based power generation scheme, depending on the point of integration of the storage system, the following two types of Solar Plus Storage System (SPSS) architectures [19] can be considered.

- DC-Coupled SPSS.
- AC-Coupled SPSS.

In the following architectures of the power conversion system, the AC electric grid can be a single-phase or three-phase. Here, the direction of the active power flow is shown using a double arrow. Depending on the application, DER Inverter can have a different name such as PV Inverter, ESS Inverter etc., as explained in the following.

1.3.1 Direct Current Coupled Solar Plus Storage System

The DC-coupled storage would need a DC/DC converter to charge or discharge the battery, and this is called ESS converter. Fig. 1.1 and Fig. 1.2 are DC-coupled SPSS with a double-stage power conversion and a single-stage power conversion, respectively. Here DC Optimizer and ESS Converter must be power conversion systems with minimum active power flow capabilities of uni-directional and bi-directional, respectively.

The DC-Coupled SPSS has a high panel-to-inverter (DC/AC) ratio, supports low-voltage energy harvest, and benefits from clipping recapture. The ESS converter can store energy produced by the PV array, thus preventing power loss, even if the grid interfacing converter is down for either scheduled maintenance on the electric grid or in the case of curtailment signals sent by concerning electric grid managing authorities.

A grid-connected DC/AC Inverter has bi-directional current-conducting switches to provide the path for freewheeling currents. Hence it is capable of bi-directional active power flow. The PV Inverter can also do a reverse active power flow if behind-the-meter storage of power from the AC electric grid to a battery pack is required.

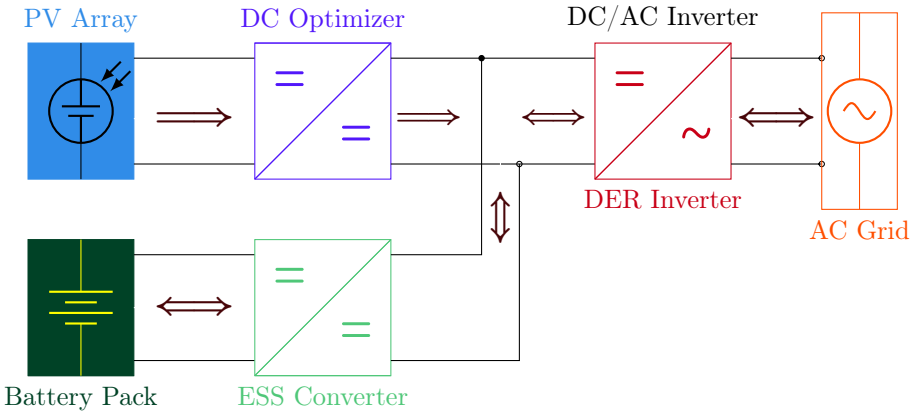

Figure 1.1: DC coupled solar plus storage system1

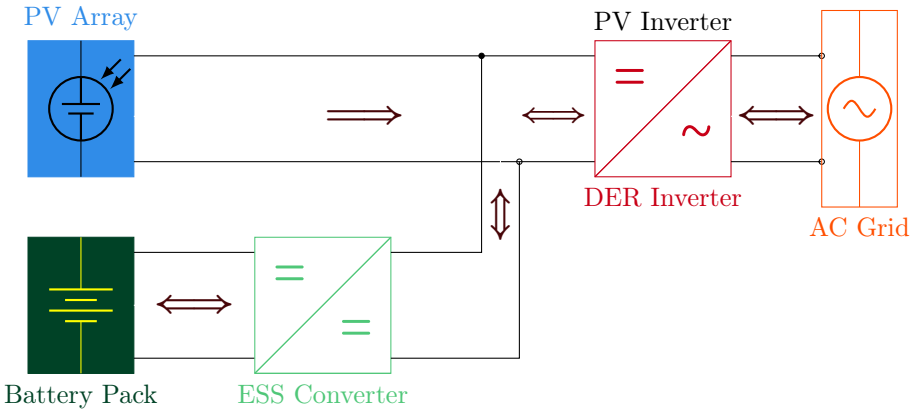

Figure 1.2: DC coupled solar plus storage system2

1.3.2 Alternating Current Coupled Solar Plus Storage System

Fig. 1.3 and Fig. 1.4 are AC-Coupled SPSS with a double-stage of power conversion and a single-stage of power conversion, respectively. Here a DC optimizer with uni-directional power flow capabilities would suffice. The maximum power dispatch to the AC grid can be done independently (or together) from both PV Array and battery pack. This architecture can offer better primary frequency regulation with the presence of two grid-connected inverters. Similarly, reactive power support is superior to the other two architectures.

A DC optimizer is shown in Fig. 1.3, which facilities low-voltage energy harvest. Whereas, this is not possible for the scheme shown in Fig. 1.4. The architecture shown in Fig. 1.4 has clipping losses and curtailment losses.

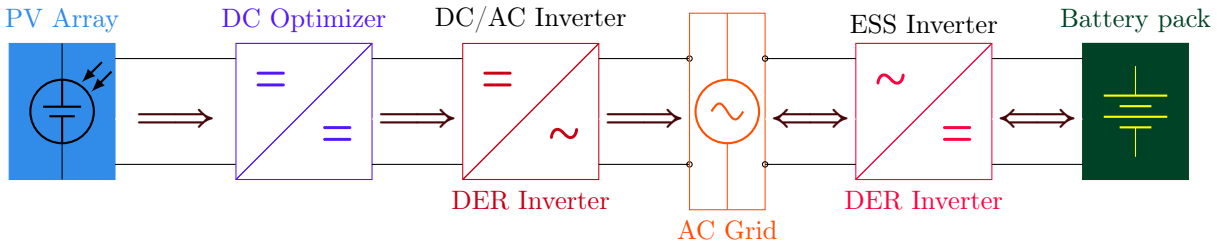

Figure 1.3: AC coupled solar plus storage system1

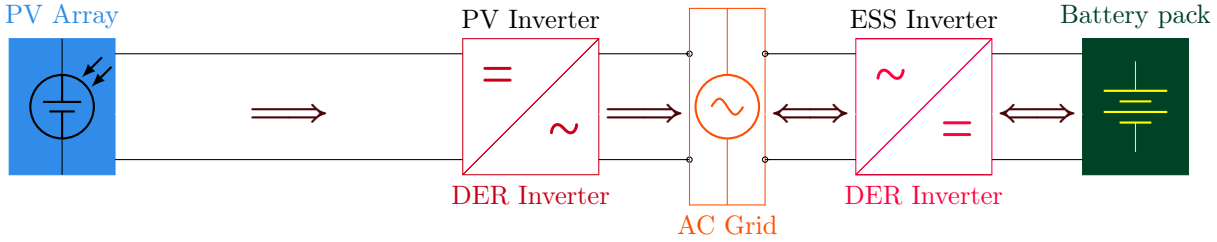

Figure 1.4: AC coupled solar plus storage system2

1.4 Motivation

> Computational modelling is becoming the third paradigm of modern sciences, as predicted by the Nobel Prize winner Ken Wilson in the 1980s at Cornell University. This so-called third paradigm complements theory and experiment to problem-solving.
>
> *Computational Optimization: An Overview* [20]
> X.-S. Yang and S. Koziel

.

1.4.1 Action Required on Climate Change

1.4.1.1 Global Warming

Ozone (O_3), carbon dioxide (CO_2), chlorofluorocarbons (CFCs and HCFCs), water vapour (H_2O), Methane (CH_4) and nitrous oxide (N_2O) are the greenhouse gases responsible for trapping the sun's heat in planet earth's atmosphere. This process of trapping the heat is called the greenhouse effect, which makes the planet earth livable [21].

Specifically, CO_2 plays a vital role in preventing the freezing of life on earth, and without CO_2, the average temperature of planet earth could fall by 33°C [21].

For the past century, burning the fossil fuels such as coal, oil, and natural gas caused more greenhouse gas emissions, ultimately leading to an imbalance in the earth's energy balance and increasing the greenhouse effect. This increased greenhouse effect led to a much warmer Earth, and the long-term warming is called Global warming [22].

1.4.1.2 Climate Change

Climate change is defined [23] as gradual changes in all the interconnected weather elements on earth over approximately 30 years.

1.4.1.3 Keeling Curve

In 1960, Dr. Charles David Keeling, a pioneer in the modern science of climate change [24,25], *First time* showed that atmospheric CO_2 concentration was rising at the south pole at a rate consistent with estimates of fossil-fuel emissions. The publication [25] has two significant findings: firstly, of the natural seasonal "breathing" of the earth and secondly, of the rise in atmospheric CO_2 due to the combustion of fossil fuels by industry and to land use changes.

CO_2, like other greenhouse gases, is found naturally in the earth's atmosphere. Based on the ice core data, an indirect measurement of earth's CO_2 shown in Fig. A.1, Fig. A.2 and Fig. A.3, shows that atmospheric concentration of CO_2 remained relatively stable for eight hundred thousand years at around 280 parts per million (ppm). However, since the beginning of the Industrial Revolution, also known as the Technological Revolution, in the 18th century, the burning of fossil fuels has significantly increased atmospheric concentration of CO_2, as shown by the direct measurement data in Fig. A.3. Today, the concentration of CO_2 in the atmosphere stands at about 420ppm, i.e., an increase of over 50%.

Thus to bring down the CO_2 emissions, more usage of sustainable energy sources such as solar energy [26, 27], wind energy, hydroelectric energy, tidal energy, geothermal energy and fuel cells (assuming the hydrogen is obtained sustainably) is required. Specifically, solar energy can be harvested by using Concentrated Solar Power (CSP) systems to produce thermal energy or one can use the principle of the PV effect to generate electricity. For CSP systems, Direct Normal Irradiance is an important factor to consider and the data for the same is shown in Fig. B.1. In PV systems, to generate electricity, PV power potential is an important factor of consideration, and the same is shown in Fig. B.2.

1.4.2 Technological Revolution 4.0/Industry 4.0

As explained above the need for sustainable energy sources, the sources are by nature very much distributed. The application of the ESS and PV Array is explained with example scenarios shown in Fig. 1.1, Fig. 1.2, Fig. 1.3, and Fig. 1.4. ESS/PV can be interfaced to the nearest PCC of the existing electric grid with a DER Inverter.

1.4.3 Principles of Economics

While economics is an integral part of power system generation, transmission and distribution, this was never the case with the power conversion system such as DER Inverter. Given the large role that DER Inverter is going to play in the future electric grid infrastructure where it will be used by utility companies, businesses, and individuals, it is also imperative to consider the economics of DER Inverter. For example, some times efficiency of the DER Inverter can be traded for a system that can be designed at a lower cost. Merely increasing efficiency or increasing the power density at the expense of an increased cost is not justified because many counties around the world have a weak economy and not many customers can afford it.

Given a diverse set of candidate solutions, the principle of equity ensures fairness in the selection of the best candidate, whereas the principle of equality doesn't. Specifically, the principle of equity is a solution for addressing the inherent imbalance in social systems and objective functions that exhibit inflation characteristics.

1.4.4 Statement of a 2019 Nobel Prize Laureate

NDTV Interviewer [28]: In very simple terms, what is the difference between your economics and traditional economics?
Dr. Abhijit V. Banerjee: I think what we do in economics, or we try to avoid in economics, is sort of building this large castle out of many, many pieces that we think are self-evident. People behave in this way. Therefore this must happen. Therefore that other thing must happen. It is a long syllogism that is built on very little. This is traditional economics. We go the other way and try to be skeptical at every step. We want to say, maybe people actually don't behave that way. Maybe actually one of these shibboleths of economics is false. *So we start asking that question from the beginning. We also build our own castle.* But hopefully, it is built on things we have tested and have some idea that it is plausible.

1.5 Direction Setting for the Thesis

Given the brief history of electric grid infrastructure evolution, the value additive motivation, the need for ESS, and PV Power Potential, it is imperative to discover the methods and techniques for the design of the DER inverter and its controllers. Thus accordingly thesis is divided into two major parts.

1.5.1 Part I

> The day science begins to study non-physical phenomena, it will make more progress in one decade than in all the previous centuries of its existence.

NIKOLA TESLA
Inventor, electrical engineer, mechanical engineer, and futurist.

Fig. 1.5 shows N modules of DER Inverters connected to the AC electric grid via coupling inductance (L_f). This DER Inverter design is intended for an ESS application shown in Fig. 1.3 or Fig. 1.4. In this context, propose an innovative design framework for a low-cost, lightweight, compact, and high-performance optimum configuration.

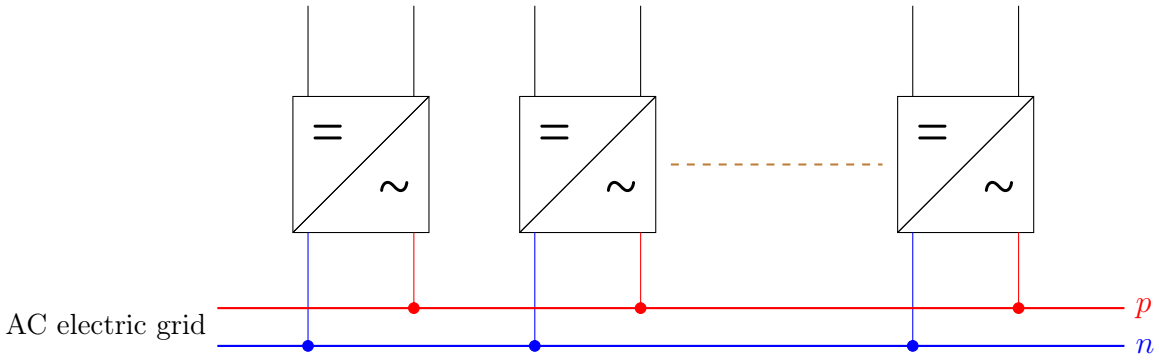

Figure 1.5: Distributed power generation/storage using 'N' modules (p:Phase, n:Neutral).

1.5.2 Part II

> Apparently insignificant variations of an initial condition in a nonlinear dynamic system may produce unexpected consequences of immense proportions.

PROF. EDWARD NORTON LORENZ
Mathematician, Meteorologist and the founder of Modern Chaos theory.

In particular, when a DER Inverter is fed from a PV source as shown in Fig. 1.2 or Fig. 1.4, propose an innovative framework for the design of the DER Inverter's linear control system.

1.6 On the need for Multi-Objective Optimization

The literature review here establishes the need for *multi-objective optimization* techniques to address the problems considered in **Part I** and **Part II** of the thesis.

1.6.1 Literature Review: Part I

The technological progress, along with i4.0, has seen a rise in the need and development of compact and lightweight power electronic systems [16, 29]. In general, the power density improves by increasing the switching frequency, thus reducing passive filtering requirements to meet given harmonic constraints. However, as the power level increases, the use of high switching frequencies becomes an issue because of the increase in electromagnetic interference, magnetic core loss and mostly, semiconductor switching losses. One way to mitigate this problem is by interleaving N power converter modules: One can synthesize waveforms with low harmonic distortion while operating with lower switching frequencies [30, 31]. Another is to use M parallel Power Semiconductor Devices (PSDs) to realize a higher current rating device.

Paper [32] reports an approach for calculating the optimal number of cascaded H-bridges (N) for a DC-AC converter based on a trade-off between efficiency and power density. The power density evaluation considers the volume of the coupling inductance (L_f) and heatsink. This design method also ensures a current ripple of less than 1% and maintains compliance with IEEE519 [33]. Paper [34] builds on this, to achieve a minimum volume realization of the desired DC side capacitance. Paper [35] presents an analysis of the cost-efficiency trade-off for the selection of the Power Semiconductor Device (PSD).

In both [32] and [34], the required switching frequency (f_s) to meet the harmonic standard is found by sweeping f_s over a wide range of frequencies and performing repeated calculations. This is not a computationally efficient approach mostly when a high number of switches are available. While [32] considers a single empirical model for the PSD, [34] uses one SiC-MOSFET loss data for the PSD loss evaluation. Neither approach considers the optimum choice of PSD. Another limitation of [32] and [34] is that the dimension of optimization is just two.

The paralleling of M lower current PSDs can be economical for the realization of a higher current rating device. It also reduces the conduction losses, thus improving efficiency [35,36]. Parallel PSDs are considered in [34], but no optimization is involved in the choice of M. Paper [36] discusses the optimization of M for a high-efficiency design of a DC-AC converter. In general, the increase of M and/or N has positive effects, but the downsides are the associated semiconductor cost and increased switch count ($4NM$). In this part of the thesis, the optimal combination of N and M is determined by considering a cost-efficiency trade-off scenario.

Based on the above, it is evident that in order to obtain an AC grid interface that is compact, lightweight, efficient and low-cost, there are a number of trade-offs to be considered along with system/performance constraints. For that, one should employ *multi-objective optimization* techniques to determine:

- Power Semiconductor Device (PSD).
- Coupling inductance (L_f).
- The number of parallel switches (M).
- The number of parallel H-bridges (N).

1.6.2 Literature Review: Part II

The conventional method of power generation, fed from fossil fuels such as coal or natural gas, causes carbon emissions responsible for climate change. These carbon emissions and subsequent climate changes cause natural disasters such as wildfires and floods. Henceforth a necessity for a paradigm shift in the method of power generation originated to ensure the sustainability of the planet earth. The commitment to sustainability in many parts of the world is progressing from carbon-neutral to carbon-free energy. Now, to stand with the pledge requires the integration of RES and ESS into the existing electric grid [30, 37–41]. The synchronous generators interface the conventional method of power generation, and to interface RES or ESS, it needed its twin, i.e., DER Inverter. DER Inverter is an apparatus, which converts the DC to AC, and vice-versa.

The DER Inverter involves a switched-mode power conversion process. Thus it is a nonlinear system, and DER Inverter demands a nonlinear controller. To use linear controllers, one needs the Linear Time-Invariant (LTI) model describing the dynamics of the DER Inverter. For the system, in consideration in this part of the thesis, the plant model is known, and an LTI model of the system dynamics can be obtained easily using linearized small-signal modelling.

The DER Inverter can be a single-phase or three-phase type. In three-phase systems, for AC regulation, one can use Voltage-Oriented Control (VOC) scheme using the synchronous reference frame theory [37, 42] to ensure a zero steady-state error in the output AC. By transforming the AC quantities to DC components, the infinite DC gain of the Proportional+Integral (PI) controller can drive the actual d-q currents to the target values without introducing steady-state errors. Paper [37] uses a Type-II PI controller without any optimization involved in the controller parameter values selection.

For the digital implementation of the controller, Asymmetrical Regular Sampled Pulse Width Modulation (ARSPWM) is used. In this, freezing the command signal at each half of the carrier period introduces a quarter-carrier-period transport delay [42, 43]. One option in this situation is to design the controller with the consideration of the delay [42, 44] or use the phase delay compensation to nullify the delay effect [37, 43]. Similarly, the effect of delay due to computation in the control loop can be dealt with by using an appropriate method. In this part of the thesis, to address the phase delay due to transport delay, a phase delay compensation method [44] is used, and phase delay due to computation is neglected.

Paper [42] presents an approach to select the optimal values of controller parameters of a PI Controller for a target value of phase margin considering transport delay and sampling delay. The design in [42], aims for a maximum value of gain crossover frequency (i.e., bandwidth) for the current loop considering the transport delay, which is introduced due to ARSPWM. Typically, in a linear control system design, two aspects are paramount: relative stability and speed of response. In time-domain analysis, relative stability and speed of response are assessed through percentage overshoot and rise time, respectively. In frequency domain analysis, relative stability and speed of response are examined through phase margin and bandwidth, respectively. It is to be noted that the bandwidth of the current loop can't be increased more than 0.1 times the switching frequency, owing to the linearized small signal model used for the control loop design. In this context, the optimal design approach in [42] leaves us with an open question: what must be the right value of the phase margin for the

system design?

In a single-phase system, for AC regulation, typically Proportional+Multi-Resonant (PMR) controller [45–51] is used, as the regular PI controllers have a small gain for the fundamental frequency component of the tracking AC signal, resulting in steady-state error. The literature [45–51] that incorporates the PMR controller in the design of the control system doesn't involve optimal parameter values for the PMR controller, considering the time-domain and frequency-domain analysis.

Texas Instrument's design manual [52] provides a graphical user interface, powerSUITE, with their products to tune the parameters of the PMR controller. The proposed tuning method is manual and could be laborious and thus not an efficient and smart approach. Moreover, the user has to make a judgement by seeing the frequency response plot, which doesn't include any information on time-domain behaviour. Paper [51] provides an optimal range of values for 3dB bandwidth ($2\omega_c$), selecting proportional gain (k_p) as per the requirement of the system dynamics, and suggests tuning of the integral gain (k_i) to make the resonant peak as high as possible. In this context, what must be the right choice of k_p, k_i and ω_c is an open research problem.

In this part of the thesis, a PV-fed single-phase DER Inverter is considered. A Type-II PI controller, an excellent choice for DC bus voltage regulation, is employed. Paper [42] provides an evaluation between the PMR controller and PI controller in terms of tracking error and didn't analyze the effect of controllers on current harmonic performance. Thus, for AC regulation, the Type-II PI controller and PMR controller, both are considered for current harmonic performance evaluation.

To determine the right choice of controller parameters in a Type-II PI Controller, considering time-domain and frequency-domain behaviour, one should employ a *multi-objective optimization* technique to determine the controller transfer function's

- Proportional gain (k_2)
- Location of zero (ω_l)
- Location of poles (ω_l, ω_h)

To determine the right choice of controller parameters in a PMR Controller, considering time-domain and frequency-domain behaviour, one should employ a *multi-objective optimization* technique to determine the controller transfer function's

- Proportional gain (k_p)
- Integral gain (k_i)
- 3dB bandwidth ($2\omega_c$)

1.7 Literature Review on Multi-Objective Optimization

The literature review here underscores the main aspects of a *multi-objective optimization* technique, which are to be used to solve the problems defined in **Part I** and **Part II** of the thesis.

Multi-objective optimization is widely used in power engineering [53–61]. The number and choice of objective functions [54] will vary depending on the application. It is observed [53] that constraints in the optimization also play a vital role.

Paper [54] considers fourteen design variables and six objective functions to find the optimal design parameters of a permanent magnet synchronous generator. This design uses a six-dimensional *Pareto*. Paper [53] considers thirteen design variables and two-objective functions in two isolated design problems to find the optimal design parameters of a wound-field flux switching machine. This design uses a two-dimensional *Pareto*. The two isolated-design problems concern the manufacturing standpoint and performance standpoint. Paper [55] uses three objective functions and *selection criteria* to arrive at a final solution for a switched reluctance motor drive.

The choice of objective functions further decides the scale of complexity involved in the optimization. Here the complexity refers to the computation of the objective functions and the computation process [62] in finding the optimal solution. Paper [63] uses Monte-Carlo simulations for analytical calculations of battery degradation, which demands heavy computation resources, thus highlighting the need for efficient computational methods/processes. Paper [64] discusses optimized charging patterns considering multiple objectives such as battery ageing, charging speed, and energy conversion efficiency. This multi-objective optimization uses a battery electro-thermal aging model for studies, which demands heavy computation resources, thus underscoring the necessity of *efficient computational method/process*. Paper [62] reduces the complexity involved in the multi-objective optimization by reducing the *number of function calls* with the sequential-stage optimization strategy.

Objective functions are blended to form a single weighted function, and one needs to *normalize* the objective functions to prevent biased sampling [65].

1.8 Literature Review on Stackelberg Leadership Model

> The best result will come from everyone in the group doing what's best for himself ... and the group.
>
> *A Beautiful Mind (2001), American biographical drama on the life of* Prof. John Forbes Nash

Stackelberg's leadership model [66] was first introduced by Heinrich Freiherr von Stackelberg in his book *market structure and equilibrium* in 1934. This model uses a leader-follower strategy and works on sequential game theory. The problems in this class are widely known as multi-level problems.

To find the solution to a multi-level problem [67–79, 79–87] the principle of backward induction is used, i.e., from the outermost problem, *determine the sequence of optimal actions*. The decision at one level (the leader) affects the decision at a below level (the follower). In this game theory model, the leader has the first-mover advantage. In the literature [67–72], typically, multi-level problems are considered bi-level problems.

Thesis [68] considered a bi-level optimization for the control of a two-level energy storage

system. In this, fast-acting short-term ESS and slow-acting long-term ESS are considered in two different levels. The fast-acting short-term ESS is the first to respond to the power fluctuation, later the power fluctuation is met by slow-acting ESS, which also has a large storage capacity compared to fast-acting ESS.

Thesis [72] considers a bi-level problem and proposes a hierarchical operational scheme for a charging system to optimize the quality of service for electric vehicle users while meeting the stability of the power grid. In this, the lower-level optimally allocates power supply to electric vehicles within a charging station, and the upper-level balances charging demand among multiple charging stations.

Paper [86] considers two levels for the design optimization of the IIR filter using a hierarchical approach and obtains a filter with the lowest order while meeting performance objectives.

The parameterization of ordinary differential equations can be hard to solve due to a large number of optimization variables, and paper [87] considers a bi-level problem. Instead of simultaneous solving of the variables, paper [87] considers a hierarchical approach, where two sets of parameters are solved in an inner-subproblem (follower), and that computed information of parameters is passed on to the outer-level (leader) to calculate the remaining set of parameters. In this way, the number of parameters to solve is broken into two levels, leading to an efficient computing approach, i.e., due to individual dimensions of the inner-subproblem and outer-subproblem being lower than the original problem. Paper [87] makes the optimization efficient by *avoiding repeated numerical simulations*.

1.9 Positioning of the Literature Review

The following sections explain the specific *multi-objective optimization* strategies used to solve the problems defined in **Part I** and **Part II** of the thesis.

1.9.1 Part I

Stackelberg model is considered in multi-objective optimization of the DER inverter for the following two reasons.

- DER inverter, a switched-mode power conversion system, could have a high number of variables and more Figures Of Merit (FOMs).
- The optimization variable in the outer-most level (leader) can have the first-mover advantage.

To introduce this Stackelberg model-based multi-level multi-objective optimization in the design of *power electronic systems*, for the sake of convenience, some variables are not considered and many of the variables are selected based on prior knowledge of the system. In this part of the thesis, as the number of variables in the optimization is four, a four-level design framework algorithm with eight FOMs is considered. If the optimization problem has any extra variables, a strategy must be devised as to how to break those extra variables into different levels and in how many levels.

Two FOMs are related to the amplitude of the harmonic component and THD_i of the grid current. To avoid repeated numerical simulations or repeated analytical calculations, the FOMs related to grid current are considered as constraints and are calculated before the optimization in the form of the required frequency modulation ratio.

Now at each level, two multi-objective functions are formulated based on the desired *optimal sequence of optimization*. The multi-objective function weights are assigned based on priority.

Now at each level, in the multi-objective optimization, for each sub-problem, the trade-off is evaluated using the Pareto front [53–57, 62, 88–91]. This scenario leads to a set of optimal solutions constituting the *Pareto* front. While a *Pareto* front gives a set of optimal solutions, to further narrow down the solution space, a utopia point [92] based technique as a *selection criterion* is considered.

The demonstration of the efficacy of design optimization is vital. In [93] efficacy of multi-level optimization is demonstrated by comparison with a base case design as a single level. A similar approach is considered here.

1.9.2 Part II

If the number of variables in the design problem is just one, then a hierarchical framework is not applicable, and this is the case with the Type-II PI controller design. Thus to solve the design problem of the Type-II PI controller, principles of convex optimization [94–96] are employed. On the other hand, the design of the PMR controller is a multi-variable problem that can inherit the principles of a hierarchical framework [44, 86, 87] to leverage the effect of any variable [44]. Thus firstly, the PMR controller is designed as a convex optimization problem. Then PMR controller is designed using all the possible six paths, in a three-variable multi-objective convex optimization problem, with a three-level hierarchical framework.

1.10 Thesis Organization

The contents of the thesis are organized as follows. **Part I** of the thesis is presented in **Chapter 2** and **Chapter 3**. **Part II** of the thesis is presented in **Chapter 4**, **Chapter 5**, and **Chapter 6**.

Chapter 2 proposes the techniques/methods for the computation of the cost functions involved in design optimization. A derived analytical expression for output current for phase-shifted parallel H-bridges is shown and will be used to calculate the total harmonic distortion of the output current. Different types of semiconductor manufacturer data used in the optimization and their power loss calculation methods are discussed. A robust statistical approach is proposed to model the cost functions of coupling inductances for the design optimization framework. A computationally efficient algorithm is proposed to estimate the required frequency modulation ratio to meet the current harmonic performance requirements. Finally, a summary of the FOMs involved in the proposed innovative Multi-Objective Hierarchical Optimization Design Framework (MO-HO-DF) is tabulated.

In **Chapter 3**, the algorithm for the proposed design optimization framework, the results of the design optimization, and a test case validation with Piecewise Linear Electrical Circuit

Simulation (PLECS) Simulation are presented. The optimization results are shown for a wide range of scenarios considered, then the benefits and limitations of the proposed design optimization framework are discussed. A test case is considered for the current harmonic validation and thermal performance Vs efficiency validation for one of the best solutions obtained in this part of the thesis.

In **Chapter 4**, the techniques/methods for the computation of the cost functions involved in the design optimization of linear controllers are presented. For the PV-fed grid-connected Inverter, to model the dynamics, LTI models are derived. It also presents the choice of PV Array, selection of DC bus capacitance and dead-time compensation method used. The control block diagrams concerning the problem of design optimization are developed. Two algorithms are proposed for the computation of the linear control system's FOMs: one for the Type-II PI Controller and one for the PMR Controller.

In **Chapter 5**, the fundamentals required to solve the convex optimization problem considered in this part of the thesis are briefly discussed with simple examples. Two algorithms are proposed for the multi-objective convex optimization of the Type-II PI controller and PMR Controller. The design optimization of the PMR Controller is considered for a hierarchical framework with six possible paths. Then, an algorithm is proposed for a three-level hierarchical framework. The optimization results are provided for 18 convex optimization problems considered in this part of the thesis and are verified through unit step responses and bode plots. Finally, for the PMR controller, a discussion is provided on the number of problems in each path of optimization, Central Processing Unit (CPU) utilization, and evaluation of the benefits.

In **Chapter 6**, first, the macro-model of H-bridge and details of the computer considered in this part of the thesis are explained. Second, detailed continuous-time simulation results and insightful discussion is provided for one of the cases considered for the MATrix LABoratory (MATLAB) simulation. Third, the discrete-time simulation is conducted for all 32 cases to compare the impact of the Type-II PI controller and PMR controller on the current harmonic performance. Fourth, statistical analysis is carried out to establish the nature of the relationship between the phase delay and resonant gain. Fifth, statistical analysis is performed to determine the type of relationship between the actual value of the overshoot and the designed value of the overshoot.

In **Chapter 7**, first, the summary of contributions for the research work concerning **Part I** and **Part II** of the thesis are discussed. Second, the conclusions for the two parts of the thesis are provided, along with an integrated conclusion statement of the thesis. Third, the potential for commercialization is discussed.

Part I

Design Philosophy for Energy Storage System Inverters

Chapter 2

Figures of Merit

Ideas are no one's monopoly. Think big, think fast, and think ahead.

MR. DHIRUBHAI AMBANI
founder of Reliance Industries.

The objective of this Chapter is to define and explain the method of determination of power conversion FOMs and computation of some of the FOMs involved in the design optimization of a single-phase 6kVA (120V/50A), 60Hz bi-directional AC grid interface with N multiple interleaved H-bridges, each with M parallel "to-be determined" PSDs, connected through coupling inductances (L_f).

2.1 Current Harmonic Performance

The amplitudes of individual harmonic components and the Total Harmonic Distortion of Current (THD_i) are of paramount importance for AC grid interfaces [33]. The magnitude of a harmonic component (I_{hl}) and the THD_i are used as constraints in the optimization. This section presents the evaluation of the current harmonic performance for the case of N interleaved H-bridges with M parallel switches. The output of each H-bridge is interfaced with the utility grid via a coupling inductance (L_f), whose ohmic resistance (R_f) is also modelled as shown in Fig.2.1. There, one can also see the potential use of M parallel PSDs.

The fundamental component of grid voltage (u_g) can be expressed as

$$u_g(t) = \sqrt{2}U_g \sin \omega_1 t. \tag{2.1}$$

Where ω_1 is the fundamental frequency in radians per second. The fundamental component of the voltage at the output of every H-bridge is assumed to be

$$v(t) = \sqrt{2}V \sin \underbrace{(\omega_1 t + \delta)}_{\psi_1(t)}. \tag{2.2}$$

It is calculated in order to have a grid current $i(t)$ with a certain magnitude and lagging the grid voltage by a certain angle (ϕ). In terms of phasors

$$V \angle \delta = U_g \angle 0 + \underbrace{(R_f + j\omega_1 L_f)}_{Z_f} \frac{I \angle -\phi}{N}. \tag{2.3}$$

To synthesize the inverter voltage, the minimum value of required DC bus voltage ($V_{dc,min}$) for operation with linear Sinusoidal Pulse Width Modulation (SPWM) is

$$V_{dc,min} = \max_{0 \le \phi \le 2\pi} \left| U_g \angle 0 + Z_f \frac{I \angle -\phi}{N} \right|. \tag{2.4}$$

The N H-bridges are interleaved and modulated using a ARSPWM scheme to synthesize the fundamental component of output voltage (v). The phase of the carrier signal for the x^{th} H-bridge is given as

$$\psi_{sx}(t) = \omega_s t + \frac{(x-1)}{N}\pi; \quad x \in (1, N). \tag{2.5}$$

Where ω_s is the switching frequency in radians per second. An expression describing the components of the current waveform injected into the AC grid is required for calculations concerning harmonic distortion. In [97], the expression for the output voltage of single-phase H-bridge with ARSPWM is given. From there, the double variable Fourier series model for $i(t)$ can be derived as

$$\begin{aligned} i(t) = \frac{m_f A(1)}{|Z_f(1)|} \sin\left(\psi_1(t) - \gamma(1)\right) - \frac{\sqrt{2}U_g}{|Z_f(1)|} \sin\left(\omega_1 t - \gamma(1)\right) + N \sum_{n=2}^{\infty} \frac{A(n)}{p' |Z_f(n)|} \sin(n\psi_1(t) - \gamma(n)) \\ + \sum_{x=1}^{N} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{A(n,m)}{q' |Z_f(n,m)|} \sin(2m\psi_{sx}(t) + (2n-1)\psi_1(t) - \gamma(n,m)). \end{aligned} \tag{2.6}$$

Where the constants (p', q'), amplitude modulation index (m_a) and frequency modulation ratio (m_f) are defined as

$$p' = \frac{n}{m_f}; q' = 2m + \frac{(2n-1)}{m_f}; m_a = \frac{\sqrt{2}V}{V_{dc}}; m_f = \frac{\omega_s}{\omega_1} = \frac{f_s}{f_1}, \tag{2.7}$$

The amplitudes, impedances and phase angles defined as

$$A(n) = 1.27 J_n\left(0.5 p' m_a \pi\right) \sin\left(0.5 n\pi\right) V_{dc} \tag{2.8a}$$

$$A(n,m) = 1.27 J_{2n-1}\left(0.5 q' m_a \pi\right) \cos\left([m+n-1]\pi\right) V_{dc} \tag{2.8b}$$

$$Z_f(n) = R_f + jn\omega_1 L_f \tag{2.8c}$$

$$Z_f(n,m) = R_f + j(2m\omega_s + (2n-1)\omega_1) L_f \tag{2.8d}$$

$$\gamma(n) = \tan^{-1}\left(n\omega_1 L_f / R_f\right) \tag{2.8e}$$

$$\gamma(n,m) = \tan^{-1}\left((2m\omega_s + (2n-1)\omega_1) L_f / R_f\right). \tag{2.8f}$$

Where $j_v(z)$ is the v^{th} Bessel function of the first kind.

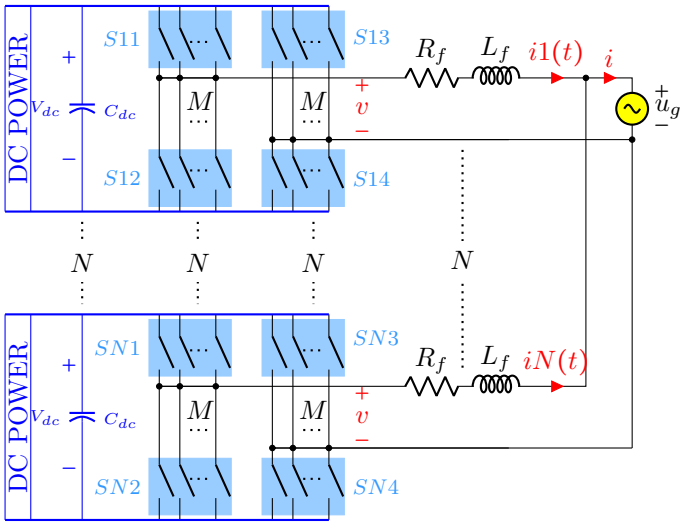

Figure 2.1: Grid-connected interleaved H-bridges with parallel switches

2.2 Power Conversion Efficiency

The power conversion efficiency (η) is defined as

$$\eta = \left(\frac{U_g I_g \cos\phi}{U_g I_g \cos\phi + P_{loss}} \right) \times 100. \tag{2.9}$$

Where the Power loss is defined as

$$P_{loss} = 4NMP_{sw} + 4NMP_{cl} + I_g^2 R_f / N. \tag{2.10}$$

P_{sw} is the switching power loss and P_{cl} is the conduction power loss in one PSD. It is assumed that the Root Mean Square (RMS) value of the inductor current is $1/N$ of the RMS value of the injected current, I_g.

2.2.1 Power Semiconductor Device Technology

In this part of the thesis, semiconductors (discrete and modules) with three distinct technologies: Silicon (Si)-Insulated-Gate Bipolar Transistor (IGBT), Silicon Carbide (SiC)-Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), and Gallium Nitride (GaN)-High-Electron-Mobility Transistor (HEMT) are considered for design optimization. The schematic symbols for three technologies are shown in Fig.2.2. The key aspects of three types of devices are,

- Si-IGBT is a combination of two individual semiconductors i.e. IGBT and anti-parallel diode printed on a single chip and connected typically by a bond-wire [98].

- SiC-MOSFET is a bi-directional current switch due to the presence of the body diode. Some SiC Modules can have zero/negligible reverse recovery loss depending on the diode manufacturing.
- GaN-HEMT is a bi-directional current switch with no diode i.e. absence of the reverse recovery losses. However, reverse conduction is possible because of the 2-Dimensional Electron Gas (2DEG) channel [99].
- Manufacturers offer some devices with the terminals Kelvin Emitter (EK) or Kelvin Source (SK), which are also considered in this part of the thesis. These terminals reduce gate drive loop inductance, thus reducing switching energy losses [100].

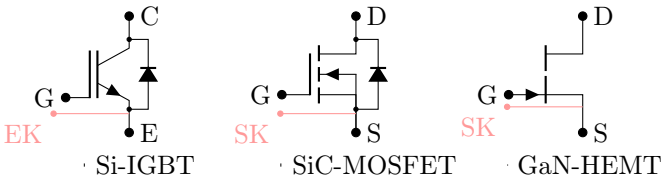

Figure 2.2: Power semiconductor devices (PSDs)

A total of 147 devices are considered for the design optimization, and the details such as voltage classes, current ampere rating range, price range, and device count by manufacturer wise are provided in Table.2.1. Devices with a positive temperature coefficient are less prone to thermal runaway problems and hence considered for paralleling of switches.

Table 2.1: Power semiconductor devices

Device technology	Voltage class	Current (A)	Price per switch	Device count (manufacturer wise)
Si-IGBT	600 V, 650 V, 1200 V	(10 – 80)A	(1.59 – 11.24) C$	Infineon–91
SiC-MOSFET	650 V, 900 V, 1000 V, 1200 V	(4.7 – 63)A	(4.68 – 51.72) C$	Infineon–17, Wolfspeed CREE–30
GaN-HEMT	650 V	(2.6 – 30)A	(6.65 – 24.26) C$	GaN Systems–9

The switches in Fig.2.1 have a power transistor and an anti-parallel diode/body diode/2DEG channel. The switch conduction periods are named Forward mode (FWD) when the transistor conducts (downwards, in Fig.2.1), and Reverse mode (REV), when the diode/ 2DEG [99] channel conducts (upwards, in Fig.2.1).

2.2.2 Switching Power Losses

The total switching power losses in a single PSD for any operating point (V_{dc}, I_{rms}) given as [101]

$$P_{sw} = \left[\frac{\sqrt{2}V_{dc}I_{rms}}{\pi V_{test}I_{test}}\right](E_{on} + E_{off} + E_{rr})f_s. \tag{2.11}$$

Where, E_{on} and E_{off} are the turn-on energy loss and turn-off energy loss corresponding to FWD specified at test voltage (V_{test}) and test current (I_{test}). E_{rr} is the reverse recovery

energy loss corresponding to REV. Typically, E_{rr} is not specified in the datasheet, but it can be calculated as [102, 103]

$$E_{rr} = 0.25 V_{test} Q_{rr}. \tag{2.12}$$

Where Q_{rr} is the reverse recovery charge of the diode.

2.2.3 Conduction Power Losses

The conduction loss (P_{cl}) is calculated from the V-I characteristics in the datasheet for the following conditions shown in Table.2.2.

Table 2.2: Conduction losses

V_g	Mode	Si-IGBT	SiC-MOSFET/ GaN-HEMT
$V_{g,max}$	FWD	$V_{0,f} I_{av,f} + I^2_{rms,f} R_{d,f}$	$I^2_{rms,f} R_{d,f}$
$V_{g,max}$	REV	$V_{0,r1} I_{av,r} + I^2_{rms,r} R_{d,r1}$	$I^2_{rms,r} R_{d,r1}$
$V_{g,min}$	DT	$(V_{0,r2} I_{av,f} + I^2_{rms,f} R_{0,r2}) t_{dt} f_s$	

Where the gate drive voltage (V_g) of the switch is varying between $V_{g,min}$ and $V_{g,max}$. $V_{0,f}$, $V_{0,r1}$ and $V_{0,r2}$ are the intercepts on the V-axis of their respective tangents drawn on V-I characteristics [102, 103]. $R_{d,f}$, $R_{d,r1}$ and $R_{d,r2}$ are the inverse slopes of their respective tangent drawn on V-I characteristics. t_{dt} is the dead-time between two switches of the same leg leading to Dead-Time mode (DT) conduction losses and these will be part of the reverse conducting element of the switch. For Si-IGBT, the anti-parallel diode is not influenced by the gate voltage, thus the reverse characteristics specified at $V_{g,max}$ can be used for DT. The average and RMS currents for the three modes can be computed [102, 103] as

$$I_{av,f} = I_{rms}(0.225 + 0.177 m_a \cos(\phi + \delta))/NM \tag{2.13a}$$

$$I_{rms,f} = I_{rms}\sqrt{(0.707 + 0.6 m_a \cos(\phi + \delta))}/NM \tag{2.13b}$$

$$I_{av,r} = I_{rms}(0.225 - 0.177 m_a \cos(\phi + \delta))/NM \tag{2.13c}$$

$$I_{rms,r} = I_{rms}\sqrt{(0.707 - 0.6 m_a \cos(\phi + \delta))}/NM. \tag{2.13d}$$

2.3 Required Cooling Effort

The H-bridge shown in Fig.2.1 has four switches. The N interleaved H-bridges with M parallel switches will lead to a switch count of $4NM$. Typically all the devices are mounted on a single heat sink [29]. The heat sink defines the isotherm environment for semiconductor switches.

2.3.1 Thermal Resistance Equivalent Circuit

Fig.2.3 shows the thermal resistance equivalent circuit for any (N, M) configuration. Where $R_{th,jcf}$, $R_{th,jcr}$, $R_{th,ch} = 0.25$°C/W, P_F and P_R are thermal resistance of the forward conduct-

ing device, the thermal resistance of the reverse conducting device, the thermal resistance of the thermal interface material, single switch power losses in FWD and single switch power losses in REV respectively. Some semiconductor modules come with a pre-applied thermal interface material. The thermal resistance of the interface material is already included in the specification device's thermal resistance.

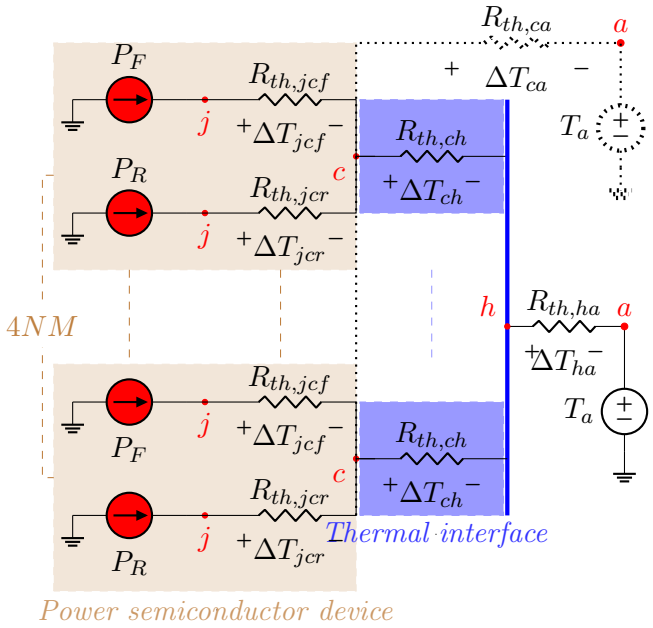

Figure 2.3: Thermal resistance equivalent circuit

2.3.2 Calculation of the Junction Temperature

If the device is mounted to a heat sink using a thermal interfacing material [104], where it can be considered as $(R_{th,jh} + R_{th,ha}) \ll R_{th,ca}$, From Fig.2.3, the junction temperature of any device is given as

$$T_{j,f} = P_F R_{th,jcf} + P_R R_{th,sd} + (P_F + P_R) R_{th,ch} + 4NM R_{th,ha} (P_{sw} + P_{cl}) + T_a \tag{2.14}$$

$$T_{j,r} = P_R R_{th,jcr} + P_F R_{th,sd} + (P_F + P_R) R_{th,ch} + 4NM R_{th,ha} (P_{sw} + P_{cl}) + T_a. \tag{2.15}$$

Where T_a, $T_{j,f}$ and $T_{j,r}$ are ambient air temperature, the junction temperature of the FWD device, and the junction temperature of the REV device. $R_{th,sd} = 0.15°\text{C/W}$ is the interactive thermal resistance between FWD and REV devices in the case of Si-IGBT. $R_{th,sd} = R_{th,jcf} = R_{th,jcr}$ in the case of SiC-MOSFET and GaN-HEMT.

2.3.3 Required Thermal Resistance of the Heat Sink

The required thermal resistance of the heat sink will be [105]

$$R_{th,ha} = \min(R_{th,haf}, R_{th,har}). \tag{2.16}$$

Where $R_{th,haf}$, $R_{th,har}$ are the required thermal resistance value based on the FWD device, and the required thermal resistance value based on the REV device respectively and given as

$$R_{th,haf} = \frac{T_j^* - T_a - P_F R_{th,jcf} - P_R R_{th,sd} - (P_F + P_R) R_{th,ch}}{4NM(P_{sw} + P_{cl})}. \tag{2.17}$$

$$R_{th,har} = \frac{T_j^* - T_a - P_R R_{th,jcr} - P_F R_{th,sd} - (P_F + P_R) R_{th,ch}}{4NM(P_{sw} + P_{cl})}. \tag{2.18}$$

Where T_j^* is given as

$$T_j^* = T_{j,max} - T_d. \tag{2.19}$$

Where $T_{j,max}$, T_d = 40°C are rated maximum junction temperature of the device and the design safety consideration.

2.3.4 Role of Required Thermal Resistance in Heat Sink Sizing

Now, given a required thermal resistance ($R_{th,ha}$), one may realize this using either a natural cooling design (passive cooling) or forced cooling design (active cooling). These two methods of realization can lead to different sizes of heat sinks. For example, specific details such as fin thickness, fan speed or geometry will influence the heat sink size. As heat sink size is inversely proportional to the required thermal resistance, in essence, a large value of required thermal resistance ($R_{th,ha}$) is best. To further explain this phenomenon, the area (A_{sink}) of the heat sink with an aluminum fin thickness of 2mm can be observed as [106]

$$A_{sink} \approx \left(\frac{89.44}{R_{th,ha}}\right)^{1.62} cm^2 \tag{2.20}$$

There could be a limit on how low $R_{th,ha}$ can be. Thus one can use the constraint to limit this to a value of their choice based on the availability of options to realize the heat sink. The option to provide constraints in the design optimization is shown in Table.2.7 and Table.3.4.

2.4 Modelling the Cost Functions of Filter Inductance

Establishing an approximate relationship of the cost, weight, and volume against any value of coupling inductance (L_f) and current (I) is needed for the design optimization framework. These parameters are related to the energy stored in the inductance given as

$$E = 0.5 L_f I^2. \tag{2.21}$$

A probabilistic model [107] is to be built with data on 61 Hammond manufacturing inductors with inductance values (3 μH to 10 mH) and current ratings (8 A - 150 A) [108] for the variables: weight (W), volume (V) and price (P). The probabilistic model can be expressed as

$$y = \underbrace{f(x)}_{\text{deterministic component}} + \underbrace{\epsilon}_{\text{random error}} \tag{2.22}$$

Where y, x are the dependent variables ($W/\ V/\ P$), independent variable (E) respectively.

2.4.1 Evaluation of the Deterministic Component

Regression modelling is used to evaluate the deterministic component. The regression model uses the robust curve fitting [109] based on bisquare weighing. The deterministic components are evaluated as

$$\ln W = (\beta_{w0} + \beta_{w1} \ln E) \tag{2.23}$$

$$\ln V = (\beta_{v0} + \beta_{v1} \ln E) \tag{2.24}$$

$$P = (\beta_{c0} + \beta_{c1} E). \tag{2.25}$$

The statistical measures are presented in Table.2.3. The statistical measures presented here are evaluated using Data1 of Fig.2.4(a), Fig.2.4(c) and Fig.2.4(e) for (2.23), (2.24) and (2.25) respectively. The confidence interval here is 95%.

The null hypothesis in a tStat test is that the estimated coefficient is zero [110]. The aforementioned null hypothesis, for all the coefficient estimates shown in Table.2.3, can be rejected [110, 111] because the pValue is less than the common alpha level of 0.05. A large absolute tStat value and a very small pValue present a strong piece of evidence [110–112] for the statistical significance of the coefficients. A R^2 value close to 1 shows the goodness-of-fit [110] of the regression model. Hence, the presence of statistical significance along with goodness-of-fit concludes that the regression models built are robust.

Table 2.3: Statistical measures: robust fitness

Equation	Coeff.	Estimate	tStat	pValue	R^2
(2.23)	β_{w0}	-7.44	-52.076	6.7e-44	0.984
	β_{w1}	0.7098	54.01	1.2e-44	
(2.24)	β_{v0}	-5.7606	-44.301	5.5e-47	0.983
	β_{v1}	0.73097	58.459	6.2e-54	
(2.25)	β_{c0}	17.851	7.7797	1.3e-10	0.996
	β_{c1}	8.77e-05	115.27	3.6e-71	

2.4.2 Evaluation of the Random Error

If the regression model has effectively captured the dependent variable in terms of the independent variable(s), then the residues [113] must be completely random. It ensures that the effect from any unknown parameters such as raw materials, technology etc. that might influence the determination of dependent variables (W, V, P) would only possibly lead to a random error, and this is explained using the absence of serial correlation [113]. As explained in the previous section, now with a good fit with regression modelling, this random error can be neglected. The randomness in the residues is determined using the Durbin-Watson test

(DW test) [114,115]. The DW test result corresponding to statistical measures presented in Table.2.3 is shown in Table.2.4.

Table 2.4: Durbin-Watson test

Equation	pValue	DW static
(2.23)	0.8575	2.0889
(2.24)	0.7139	1.9382
(2.25)	0.6581	2.1292

The null hypothesis in a DW test is that the residuals are uncorrelated [115]. The aforementioned null hypothesis can't be rejected because pValue is greater than the common alpha level of 0.05. Hence, the presence of randomness in the residues. The DW static close to 2 indicates that there is no serial auto-correlation among residue [116]. Fig.2.4(b), Fig.2.4(d), and Fig.2.4(f) show the residual values plotted against the fitted values for the corresponding curve fittings shown in Fig.2.4(a), Fig.2.4(c), and Fig.2.4(e), respectively.

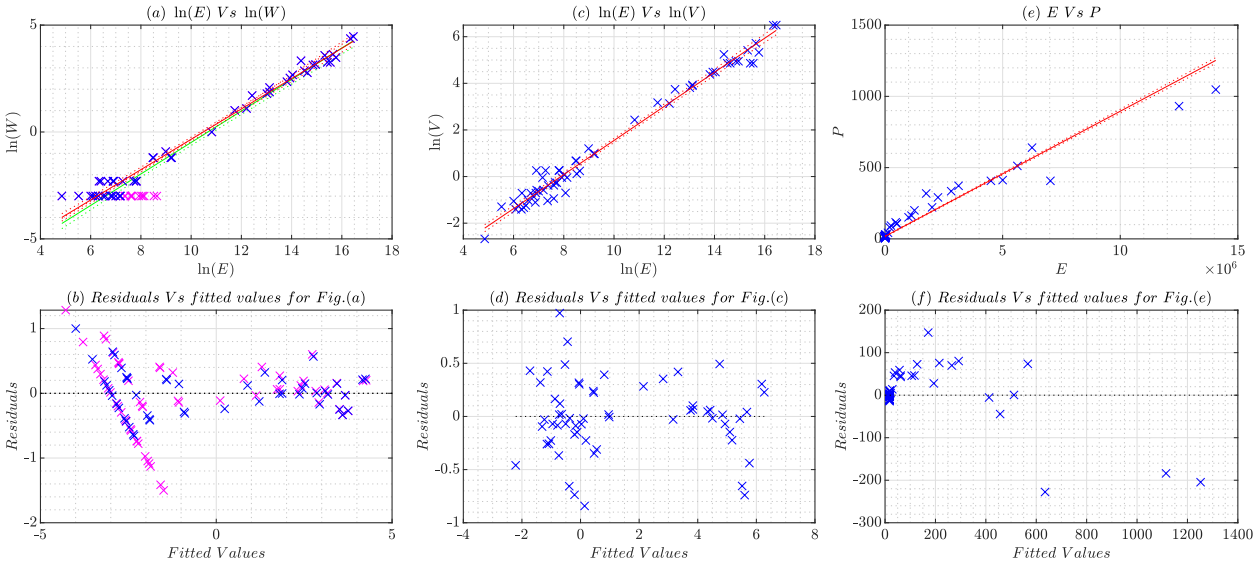

Figure 2.4: Analysis of curve fitting and it's residues (× Data1,– Fit1, × Data2, – Fit2,)

If the DW test indicates weak randomness, this implies insufficient capture of the dependent variable in terms of the independent variable. It is the initial situation with weight model (2.23). The DW test for (2.23) using Data2 gives a pValue almost close to the typical alpha level of 0.05 with a DW static of 1.54. Thus, there is no strong evidence to accept the null hypothesis of the DW test. Now, the idea here is to break/weaken the pattern. As shown in Fig.2.4(a), the initial data (Data2) is analyzed and found that excluding the data points with residues less than -0.5 leads to data (Data1) that improves the random error. A DW static close to 2 with a pValue greater than the typical alpha value of 0.05 is obtained. It presents strong evidence to accept the null hypothesis of the DW test. The improvement of the weight model, with DW test, can be seen in Table.2.5.

Table 2.5: Durbin-Watson test for the weight model (2.23)

Data Set	pValue	DW static	best
Data2	0.0511	1.5415	✗
Data1	0.8575	2.0889	✔

Better statistical measures are also achieved with Data1, as shown in Table.2.6. Hence, the strategy adopted to improve the weight model (2.23) is justified.

Table 2.6: Improvement of weight model (2.23) using Durbin-Watson test

Data Set	Coeff.	Estimate	tStat	pValue	R^2
Data2	β_{w0}	-7.8529	-38.066	3.2e-43	0.959
	β_{w1}	0.73621	37.112	1.3e-42	
Data1	β_{w0}	-7.44	-52.076	6.7e-44	0.984
	β_{w1}	0.7098	54.01	1.2e-44	

2.4.3 Cost, Weight and Volumes for Optimization

A total of 28 values of inductance are considered for the optimization framework. Their values vary between $2\mu H$ to $6000\mu H$ as shown in Fig.2.5.

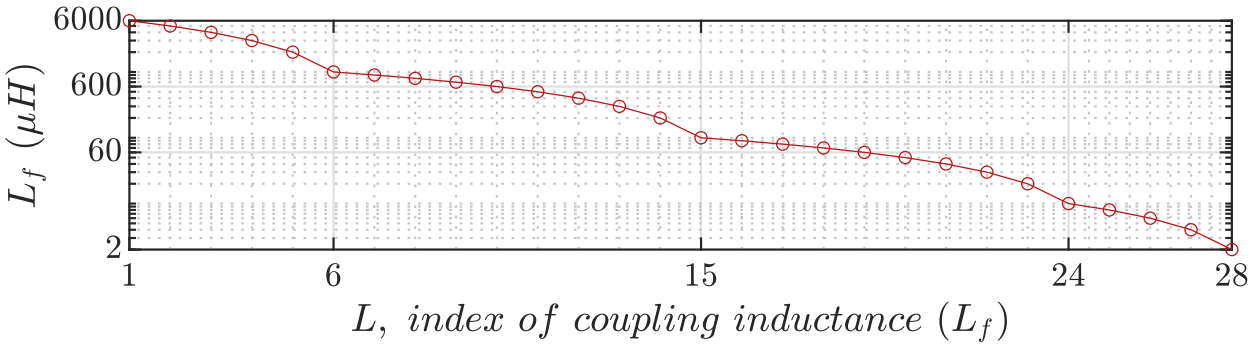

Figure 2.5: Coupling inductance and its index number

Since the use of N interleaved H-bridges is envisaged, the RMS value of the inductor current is given by I_g/N. Thus the total number of inductors will be $28 \times N$. With the candidate values for L_f and N, one can compute the energy related to each inductor (2.21). The FOMs for weight, volume and price from (2.23), (2.24) and (2.25), are established as

$$L_w = NW \tag{2.26}$$

$$L_v = NV \tag{2.27}$$

$$L_\$ = NP \tag{2.28}$$

2.5 Required Frequency Modulation Ratio

Any choice of (N, L_f) demands a specific m_f of the power conversion to meet the current harmonic performance targets: THD_i and I_{hl}. The knowledge of the m_f is also essential to determine other FOMs: $R_{th,ha}$ and η. The Algorithm 1 is developed in MATLAB and it determines the required m_f for different possible configurations described by (N, L_f).

Algorithm 1 starts with the calculation of m_f for $n = \min(N) = 1$ and $l = l_m = \max(L) = 28$; ends with $n = \max(N) = n_m = 8$ and $l = \min(L) = 1$. Here, one computes the minimum m_f required to meet current harmonic performance requirements for all values of m_a from $m_{a,min}$ to 1. The $m_{a,min}$ is given as

$$m_{a,min} = \left(\frac{1}{V_{dc}}\right) \min_{0 \le \phi \le 2\pi} \left| U_g \angle 0 + Z_f \frac{I \angle -\phi}{N} \right|. \tag{2.29}$$

Searching for the required m_f, for all configurations, with normal programming can be very time-consuming. Here, normal programming refers to an initial value of 1 for the m_f in every configuration of (N, L_f), and increments the loop by 1, till one finds the m_f that satisfies current harmonic performance requirements. However, with the following improvements in the Algorithm 1, the computation time for the complete algorithm is brought down to 20 minutes.

- *Initial guess:* The decrease of N or L_f is accompanied by an increase in the required m_f to meet the current harmonic performance targets. This information is leveraged and the initial guess in the estimation of the m_f is continuously adapted to reduce the computation burden. e.g., If $N = 2$, the initial guess of m_f for (N, l) configuration will be the m_f obtained for $(N-1, l)$ configuration.

- *Binary search inspired estimation:* A binary search inspired estimation (i.e., repeatedly dividing the m_f number by two) technique is used to determine m_f with a minimum number of iterations.

Fig.2.6 shows the estimated minimum values of m_f that meet the harmonic constraints shown in Table.2.7 for various N values. These are computed for all 28 values of Lf considered in this part of the thesis.

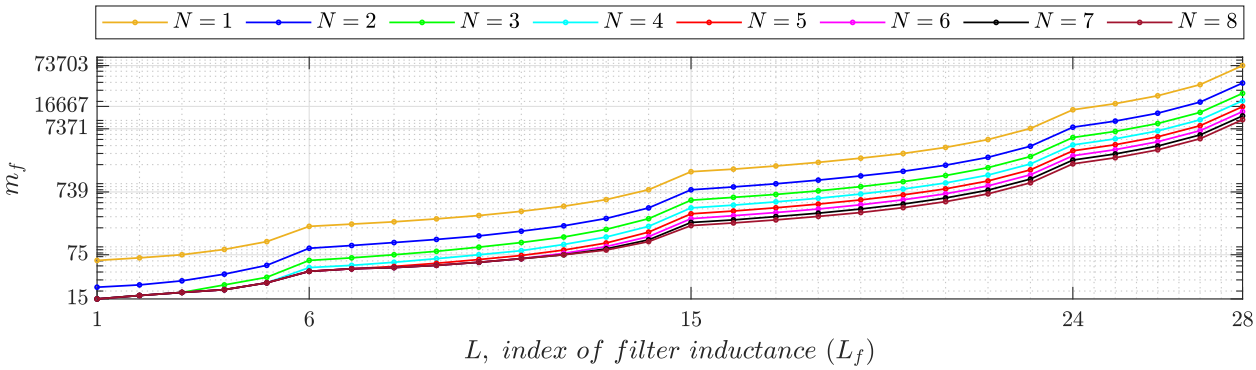

Figure 2.6: Estimated m_f values for 28 values of L_f and N = 1 to 8.

Algorithm 1: Estimation of the Required Frequency Modulation Ratio

input : System specifications
output: Estimated frequency modulation ratios

for $n \leftarrow 1$ **to** n_m **do**
  for $l \leftarrow l_m$ **to** 1 **do**
    $i \leftarrow 1$
    Calculate $m_{a,min}$
    for $m_a \leftarrow m_{a,min}$ **to** 1 **by** $(1 - m_{a,min})/10$ **do**
      if $l = l_m$ & $n = 1$ **then**
        $m_{f0} \leftarrow 166667$
      else if $n = 1$ **then**
        $m_{f0} \leftarrow d(n, l+1)$
      else
        $m_{f0} \leftarrow d(n-1, l)$
      $flag = 0, j = 1$
      $d(j,:) = [0, m_{f0}, \texttt{floor}(0.5 m_{f0}), 1]$
      while $flag = 0$ **do**
        Calculate $\mathrm{THD_i}$, $\mathrm{I_{h,max}}$
        $d(j,4) \leftarrow \mathrm{THD_i} < 1$ & $\mathrm{I_{h,max}} < 0.8$
        $j \leftarrow j + 1$
        if $d(j-1,4) = 1$ **then**
          $u \leftarrow \texttt{floor}\ ((d(j-1,1) + d(j-1,3))/2)$
          $d(j,:) \leftarrow [d(j-1,1), d(j-1,3), u, 1]$
        else
          $u \leftarrow \texttt{floor}\ ((d(j-1,2) + d(j-1,3))/2)$
          $d(j,:) \leftarrow [d(j-1,3), d(j-1,2), u, 0]$
        if $d(j,3) = d(j-1,3)$ **then**
          $flag \leftarrow 1$
          if $\texttt{mod}\ (d(j,2), 2) = 0$ **then**
            $m_{f1} \leftarrow d(j,2) + 1$
          else
            $m_{f1} \leftarrow d(j,2)$
      $m_{f2}(1,i) \leftarrow m_{f1}$
      $i \leftarrow i + 1$
    $m_f(n,l) \leftarrow \texttt{max}\ (m_{f2}(1,:))$

2.6 Goals and Constraints of FOMs

Table.2.7 summarizes the FOMs associated with low-cost, lightweight, compact and high-performance bi-directional AC grid interface. It also shows their goals, constraints and related equations as considered in this part of the thesis.

Table 2.7: Figures of Merit

S.No.	Figure of Merit	Goal	Constraint	Eq.
1	THD_i	Target	$\text{THD}_\text{i} < 1\%$	(2.6)
2	I_{hl}	Target	$I_{hl} < 0.8\%$	(2.6)
3	$1/(1 + R_{th,ha})$	Minimize	$R_{th,ha} \geq 0.1°\text{C/W}$	(2.16)
4	$100 - \eta$	Minimize	$\eta > 97\%$	(2.9)
5	$PSD_\$$	Minimize	$PSD_\$ + L_\$ \leq \$800$	(2.30)
6	$L_\$$	Minimize		(2.28)
7	L_v	Minimize	-	(2.27)
8	L_w	Minimize	-	(2.26)

Where the total Semiconductor Cost ($PSD_\$$) for any (M, N) configuration is given as

$$PSD_\$ = 4NM \times (\text{price per switch}). \tag{2.30}$$

All FOMs are restated to the goal of minimization to be able to blend FOMs into one objective function, if necessary.

2.7 Summary

This chapter has presented the methods required for computing the FOMs involved in the design optimization considered in this part of the thesis. The proposed innovation uses a derived analytical expression i.e., a double-variable Fourier series expression of the total output current, to calculate the total harmonic distortion.

A total of 147 power semiconductor device data sheets are downloaded from three different manufacturers' websites. All 147 devices' characteristics are studied and used a physical scale to measure the slopes and intercepts of curves that are essential to computing the power losses of devices. All of this data is stored in an excel sheet, to be later used by the optimization program running in MATLAB. This type of manufacturer's data-based approach reduces the uncertainty in design optimization and provides an optimal solution close to the practical scenario.

A lumped thermal resistance equivalent circuit for the power conversion system is discussed. Then it is shown with an example that the size of the heat sink is inversely proportional to the required thermal resistance. In other words, the greater the required thermal resistance, the lesser the required cooling effort.

A robust statistical modelling technique is proposed to estimate the volume, weight, and cost/price of coupling inductance as a function of energy to be stored. The proposed method provides a robust linear model for the FOMs of the coupling inductance. Having this robust linear model removes the uncertainty that may come with the optimization.

For the considered power conversion system, one needs to select the frequency modulation ratio, which decides the THD_i. For a given m_f, one can calculate the THD_i using the

double-variable Fourier series expression of the total output current, but then how to choose the m_f that can keep the $\mathrm{THD_i}$ below 1%? To address this, a computationally efficient algorithm for estimating the required frequency modulation ratio (m_f) to meet current harmonic performance requirements of grid-connected systems, compliance with IEEE519 [33], is proposed.

Chapter 3

Optimization Algorithm and Results

> Apart from values and ethics which I have tried to live by, the legacy I would like to leave behind is a very simple one - that I have always stood up for what I consider to be the right thing, and I have tried to be as fair and equitable as I could be.
>
> — Mr. Ratan Tata
> *Chairman Emeritus, Tata Sons and Tata Group.*

3.1 Multi-Objective Hierarchical Optimization

Hierarchical optimization [86, 87] involves breaking down the problem into multiple levels of inner sub-problems and outer sub-problems. These sub-problems are lower in dimension when compared to the overall optimization problem. This reduces the complexity in the FOMs trade-off assessment. The trade-off in each sub-problem is evaluated using the Pareto front [53–57, 62]. This scenario leads to a set of optimal solutions constituting the Pareto front. The best solution from the Pareto front needs to be known to move to its outer sub-problem in hierarchical optimization. The next section explains the determination of the best solution using the Utopia point [92].

3.1.1 Concept of the Best Solution

Fig.3.1 shows various solutions obtained with two objective functions (f_1, f_2), which are to be minimized. The Pareto front is evaluated for the set of solutions defined by these objective functions. The solutions that are not on the Pareto front are dominated solutions. Let (x_i, y_i) be the i^{th} solution on the Pareto front. The minimum and maximum of individual objective function values on the Pareto front are given as (x_{min}, y_{min}) and (x_{max}, y_{max}) respectively. The (x_{min}, y_{min}) is called the Utopia point. The normalized Euclidean distance (d_i) from the Utopia point to any i^{th} solution on the Pareto front is given as

$$d_i = \sqrt{\left(\frac{x_i - x_{min}}{x_{max}}\right)^2 + \left(\frac{y_i - y_{min}}{y_{max}}\right)^2}. \tag{3.1}$$

Then, the solution with the minimum of d_i is the best solution.

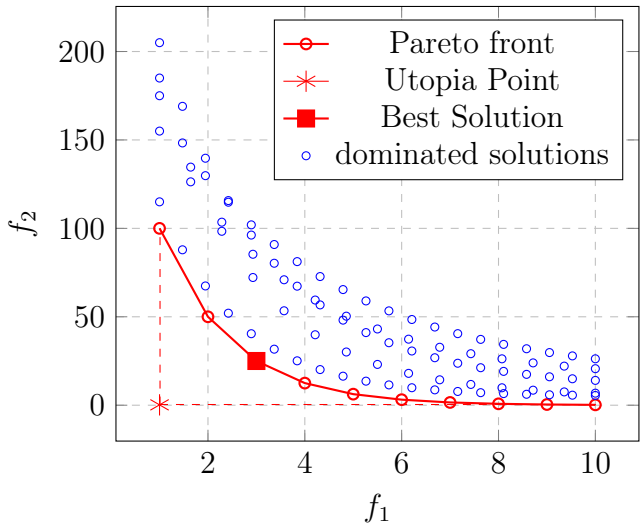

Figure 3.1: Illustration of a Pareto optimization

3.1.2 Choices in the Levels of the Optimization

This part of the thesis considers (N, M, L_f, PSD) as design configuration parameters. Accordingly, a four-level optimization is chosen. The four levels are namely Level-4, Level-3, Level-2 and Level-1. The innermost sub-problem is at Level-4, and the outermost sub-problem is at Level-1. The optimization starts at Level-4 and moves up to Level-1. Algorithm 2 shows the implementation of multi-objective hierarchical optimization. Before going to the description of the algorithm, the following sections describe the rationale for the choice of a specific configuration parameter from the available set of (N, M, L_f, PSD), in each Llevel for the optimization.

3.1.2.1 Choices in Level-4 and Level-3

Level-4 and Level-3 deal with selecting the PSD and value of coupling inductance (L_f), respectively. The PSD is chosen first for two reasons. First, because for any given H-bridge configuration (N, M, L_f) one wants to evaluate how far the limits on the efficiency and the heat sink size can be pushed cost-effectively. This is done with the choice of the objective functions (3.2) and (3.3) that emphasize cost and power losses. Second, from Table.3.1, it is also evident that the choice of optimization of PSD before coupling inductance is better because of less number of sub-problems.

Once the best PSD, out of 147 candidates, is chosen for every configuration defined by (N, M, L_f), 1792 sub-problems, one moves forward to choose the *right value of coupling inductance* by again pushing the limits on efficiency and heat sink size. This is achieved with objective functions (3.4) and (3.5) that focus on the coupling inductance parameters and power losses of the PSD.

Table 3.1: Number of sub-problems in Level-3 and Level-4

Path	Level-4	Level-3	Total
PSD $\longrightarrow$ L_f	$N \times M \times count(L_f)$ $8 \times 8 \times 28 = 1792$	$N \times M$ $8 \times 8 = 64$	1852 ✓
$L_f \longrightarrow$ PSD	$N \times M \times count(PSD)$ $8 \times 8 \times 147 = 9408$	$N \times M$ $8 \times 8 = 64$	9472 ✗

3.1.2.2 Choices in Level-2 and Level-1

Post the Level-4 and Level-3 optimization, one has two options (N, M) to consider for optimization in Level-2 and Level-1. The change of the N or the M is associated with a different degree of impact.

If N is increased,

- The effective switching frequency at the output gets increased, thus facilitating a lower value of m_f for any given value coupling inductance to meet the THD_i. This leads to lower switching power losses.
- The average and RMS switch currents reduce by $1/N$ times, leading to a total reduction of conduction losses by $1/N$ times.

If M is increased,

- There is no impact on the effective switching frequency at the output. Hence no impact on switching power losses.
- The average and RMS switch currents reduce by $1/M$ times, leading to a total reduction of conduction losses by $1/M$ times.

Thus it is evident that the degree of impact with a change of the N or the M is different. Further analysis of optimization results is needed to determine the effects of the Path. Hence the optimization scenario is conducted in two Paths. In Path#1, in Level-2, fix the N value and vary M to choose the best M. In Path#2, in Level-2, fix the M value and vary N to choose the best M. Therefore, in Path#1, in Level-1, it will be finding the best value of N. In Path#2, in Level-1, it will be finding the best value of M. As can be seen in Algorithm 2, α_m, β_m refers to the maximum number of iterations of the outermost loop and second outermost loop respectively. In Level-1, there is one sub-problem. However, in Level-2, the number of sub-problems is decided by the choice of Path. In Path#1, in Level-2, the maximum number of sub-problems is equal to the maximum value of N and this leads to $\alpha_m = n_m$ and $\beta_m = n_m$. In Path#2, in Level-2, the maximum number of sub-problems is equal to the maximum value of M and this leads to $\alpha_m = m_m$ and $\beta_m = n_m$.

In addition to limiting the maximum number of iterations based on the choice of Path, the solutions should be calculated as per the choice of Path. For example, in Path#1, the outermost loop is for N and the second outermost loop is for M, this means, one calculates (N, M, L_f, PSD) solutions in Level-2 for a fixed value of N, with an inner loop increment of

M. i.e. For a fixed H-bridge configuration, vary the number of parallel switches from 1 to $\texttt{max}(M) = m_m$, and find the best M. Then, move to the second value of N, and repeat this up to the $\texttt{max}(N) = n_m$. A similar explanation goes for Path#2 with the outermost loop for M and the second outermost loop for N.

3.1.3 Optimization Algorithm

The input to the Algorithm.2 are: m_f, f_1, $I_{av,f}$, $I_{av,r}$, $I_{rms,r}$, $I_{rms,r}$, I_{rms}, V_{dc}, PSDs data sheets information, the array of coupling inductance values (L_f), coupling inductance FOMs and targets of FOMs. The best solution will be the single optimal solution given by the optimization algorithm. Before starting the Level-4 optimization, the FOMs are calculated for the configurations (solutions) described by (N, M, L_f, PSD). Then, only those solutions with their FOMs satisfying constraints as shown in Table.3.4 are stored and processed in the optimization. The three PSD types have different formulas for power loss calculations, as explained in the Section 2.2. Hence, the solutions are computed by PSD type using different subroutines (containing standard formulas) written in MATLAB and are stored into separate 2D arrays: v_a, v_b and v_c; later merged into a 2D array v_l. Each row in v_l corresponds to one solution, where all the FOMs information is stored in different columns.

Algorithm 2: Multi-Objective Hierarchical Optimization

input : System parameters
output: Best Solution

$i_2 \leftarrow 1$
for $\alpha \leftarrow 1$ **to** α_m **do**
  $i_3 \leftarrow 1$
  for $\beta \leftarrow 1$ **to** β_m **do**
    $i_4 \leftarrow 1$
    for $l \leftarrow 1$ **to** l_m **do**
      $v_a \leftarrow$ Si-IGBT solutions
      $v_b \leftarrow$ SiC-MOSFET solutions
      $v_c \leftarrow$ GaN-HEMT solutions
      $v_l = [v_a; v_b; v_c]$
      $[f_{41}, f_{42}] \leftarrow \texttt{Normalize}\ (v_l)$
      $v_{l4}(i_4) \leftarrow \texttt{eValPareto}\ (f_{41}, f_{42})$
      $i_4 \leftarrow i_4 + 1$
    $[f_{31}, f_{32}] \leftarrow \texttt{Normalize}\ (v_{l4})$
    $v_{l3}(i_3) \leftarrow \texttt{eValPareto}\ (f_{31}, f_{32})$
    $i_3 \leftarrow i_3 + 1$
  $[f_{21}, f_{22}] \leftarrow \texttt{Normalize}\ (v_{l3})$
  $v_{l2}(i_2) \leftarrow \texttt{eValPareto}\ (f_{21}, f_{22})$
  $i_2 \leftarrow i_2 + 1$
$[f_{11}, f_{12}] \leftarrow \texttt{Normalize}\ (v_{l2})$
$v_{l1} \leftarrow \texttt{eValPareto}\ (f_{11}, f_{12})$

3.1.3.1 Normalization of Objective Functions

In any Level-x, $\forall x \in (1,4)$, the composite objective functions f_{x1} and f_{x2} are formed using the subroutine `Normalize()` as follows.

- normalize each FOM to a scale of 0 to 1.
- composite objective functions are formed by adding FOMs multiplied by their respective weights: $\lambda_{xyi} \ \forall \ x \in (1,4),\ y \in (1,2)$ and $i \in \mathbb{R}$. Where x, and y refer to the number of the Level and the number of the objective function, respectively.

The weights are chosen to keep the composite objective function values between 0 and 1.

3.1.3.2 Evaluation of Best Solution

The evaluation of the Pareto front and finding the best solution is the same as described earlier in the "concept of the best solution." This is performed using the subroutine `eValPareto()`.

3.1.4 Formulation of Multi-Objective Functions

The formulation of normalized multi-objective functions for different levels is detailed in the following.

3.1.4.1 Multi-Objective Functions in Level-4

Level-4 deals with selecting the best PSD for a specific configuration: (N, M, L_f). Now for each specific configuration (N, M, L_f), 1792 sub-problems, when one compares different PSD, the η and $R_{th,ha}$ have a positive correlation and vary by different amounts depending on the device specifications. Thus, a composite objective function in this regard would help to derive maximum advantage. The evaluation of trade-off at this level is between maximizing η and $R_{th,ha}$ (3.3), while minimizing semiconductor cost ($PSD_\$$) (3.2) among 147 PSDs. The normalized objective functions are formulated as

$$f_{41} = PSD_\$ \tag{3.2}$$

$$f_{42} = \lambda_{421}(1/(1 + R_{th,ha})) + \lambda_{422}(100 - \eta). \tag{3.3}$$

Thus, in Level-4, the trade-off between f_{41} and f_{42} finds the best PSD for any specific configuration of (N, M, Lf).

3.1.4.2 Multi-Objective Functions in Level-3

The aim at this level is to find the best value of coupling inductance, among 28 possible values, for a specific configuration defined by (N, M), 64 sub-problems. For that, one considers the PSD calculated in level-4 for the given (N, M, L_f) combination. The trade-off in this Level is between the two normalized objective functions, f_{31} and f_{32} defined as

$$f_{31} = \lambda_{311}L_\$ + \lambda_{312}L_v + \lambda_{313}L_w \tag{3.4}$$

$$f_{32} = \lambda_{321}(1/(1 + R_{th,ha})) + \lambda_{322}(100 - \eta). \tag{3.5}$$

The trade-off sought here is between the inductance's cost-volume-weight and the resulting power losses in the switches. It should be noted that along with each value of L_f, there is a m_f required to achieve the specified THD_i. As the value of the coupling inductance reduces, the required m_f increases, which tends to increase the power losses in the switches. Since N and M are fixed while finding the right value of coupling inductance, the switch count ($4NM$) is constant, leading to fixed semiconductor cost. Hence $PSD_\$$ is not needed in any objective function.

3.1.4.3 Multi-Objective Functions in Level-2

In Level-2, for each configuration (N, M), the best PSD and L_f have already been selected. After Level-3 optimization, one has path#1 and path#2 to consider. If one takes Path#1, in Level-2, one determines the *right number of parallel switches (M).* If one takes Path#2, in Level-2, one determines the *right number of parallel H-bridges(N).* Irrespective of the choice of the Path, the trade-off in Path#1 for right M and in Path#2 for right N, is found using normalized objective functions defined as

$$f_{21} = \lambda_{211} L_\$ + \lambda_{212} L_v + \lambda_{213} L_w + \lambda_{214} PSD_\$ \tag{3.6}$$

$$f_{22} = \lambda_{221}(1/(1 + R_{th,ha})) + \lambda_{222}(100 - \eta). \tag{3.7}$$

3.1.4.4 Multi-Objective Functions in Level-1

The outermost level is Level-1. If one takes Path#1, the best choice of (M, L_f, PSD) has already been found for different values of N. Thus, this Path finds the *right number of parallel H-bridges (N).* If one takes Path#2, the best choice of (N, L_f, PSD) has already been found for different values of M. Thus, this Path finds the *right number of parallel switches (M).* Similar to Level-2, irrespective of the choice of the Path, the trade-off in Path#1 for right N and in Path#2 for right M, is found using normalized objective functions defined as

$$f_{11} = \lambda_{111} L_\$ + \lambda_{112} L_v + \lambda_{113} L_w + \lambda_{114} PSD_\$ \tag{3.8}$$

$$f_{12} = \lambda_{121}(1/(1 + R_{th,ha})) + \lambda_{122}(100 - \eta) \tag{3.9}$$

3.2 Optimization Scenarios and Results

The change of constraints and weightage of FOMs have an impact on the best solution. Hence, design optimization is an iterative process [56]. The defined objectives and constraints can get further modified depending on the obtained results. Thus, in this part of the thesis, four optimization cases with different sets of weights for the FOMs are considered. These are namely Case#1, Case#2, Case#3 and Case#4. In Case#1, the optimization is carried out by considering equal priority for all the FOMs in an objective function. When one reduces the efficiency constraint, the Pareto gets more solutions. Now it is of interest to see how the best solution will be impacted. Based on the obtained results of Case#1, it is found that the total cost ($PSD_\$ + L_\$$) is on the higher side. The increased total cost is due to a higher $PSD_\$$. Hence a new criterion with increased weightage for $PSD_\$$ and reduced constraint on η is considered for Case#2. Case#2 results have led to solutions with reduced total

cost. Hence, in Case#3, a further increase in precedence for $PSD_\$$ and reduced constraint on $PSD_\$ + L_\$$ is considered. Finally, to obtain further low-cost solutions, in Case#4, by keeping the priority of FOMs in an objective function the same as in Case#3, a further reduced constraint on $PSD_\$ + L_\$$ is considered. These four scenarios of optimization are carried out using Path#1 and Path#2. Thus, the total number of best solutions will be 4×2=8.

3.2.1 Optimization Scenarios

Table.3.2 summarizes the optimization scenarios and the associated terminology used in the following sections. The 'Notation' column in the table represents the specific Case and Path of the optimization.

Table 3.2: Optimization scenarios with Path#1 and Path#2

Case	Path	Best solution	Notation
Case#1	Path#1	best solution#1	C1P1
	Path#2	best solution#2	C1P2
Case#2	Path#1	best solution#3	C2P1
	Path#2	best solution#4	C2P2
Case#3	Path#1	best solution#5	C3P1
	Path#2	best solution#6	C3P2
Case#4	Path#1	best solution#7	C4P1
	Path#2	best solution#8	C4P2

3.2.1.1 Weights of FOMs

Table.3.3 shows the weights of FOMs for multi-objective functions in different Levels of optimization. They are the same for Levels 4 and 3 and different for Levels 2 and 1. Since each case of optimization is evaluated for two paths, the weights of FOMs are considered as same for both Paths. For example, CiP1 and CiP2, with i = 1, 2 and 3, will have the same weights for FOMs in Level-4, Level-3, Level-2 and Level-1. Now one can see that weightages of $PSD_\$$ in Case#1, Case#2, Case#3 and Case#4, in Level-2 and Level-1, are 25%, 33%, 50% and 50% respectively.

3.2.1.2 Constraints on FOMs

Table.3.4 shows the constraints on FOMs for different scenarios of optimization. As one moves from Case#1 to Case#4, one can notice reduced constraints on η and/or $PSD_\$ + L_\$$.

Table 3.3: Weights of FOMs for different optimization scenarios

Notation	Level	Weights of FOMs
C1P1 & C1P2	Level-4	$\lambda_{421} = \lambda_{422} = 0.5$
	Level-3	$\lambda_{311} = \lambda_{312} = \lambda_{313} = 1/3$ $\lambda_{321} = \lambda_{322} = 0.5$
	Level-2	$\lambda_{211} = \lambda_{212} = \lambda_{213} = \lambda_{214} = 0.25$ $\lambda_{221} = \lambda_{222} = 0.5$
	Level-1	$\lambda_{111} = \lambda_{112} = \lambda_{113} = \lambda_{114} = 0.25$ $\lambda_{121} = \lambda_{122} = 0.5$
C2P1 & C2P2	Level-4	$\lambda_{421} = \lambda_{422} = 0.5$
	Level-3	$\lambda_{311} = \lambda_{312} = \lambda_{313} = 1/3$ $\lambda_{321} = \lambda_{322} = 0.5$
	Level-2	$\lambda_{211} = \lambda_{212} = \lambda_{213} = 2/9,\ \lambda_{214} = 1/3$ $\lambda_{221} = \lambda_{222} = 0.5$
	Level-1	$\lambda_{111} = \lambda_{112} = \lambda_{113} = 2/9,\ \lambda_{114} = 1/3$ $\lambda_{121} = \lambda_{122} = 0.5$
C3P1, C3P2, C4P1, & C4P2	Level-4	$\lambda_{421} = \lambda_{422} = 0.5$
	Level-3	$\lambda_{311} = \lambda_{312} = \lambda_{313} = 1/3$ $\lambda_{321} = \lambda_{322} = 0.5$
	Level-2	$\lambda_{211} = \lambda_{212} = \lambda_{213} = 1/6,\ \lambda_{214} = 1/2$ $\lambda_{221} = \lambda_{222} = 0.5$
	Level-1	$\lambda_{111} = \lambda_{112} = \lambda_{113} = 1/6,\ \lambda_{114} = 1/2$ $\lambda_{121} = \lambda_{122} = 0.5$

Table 3.4: Constraints on FOMs for different optimization scenarios

Notation	η	$R_{th,ha}$	$PSD_\$ + L_\$$
C1P1 & C1P2	$\geq 98\%$	≥ 0.1°C/W	$\leq$ \$800
C2P1 & C2P2	$\geq 97\%$	≥ 0.1°C/W	$\leq$ \$600
C3P1 & C3P2	$\geq 97\%$	≥ 0.1°C/W	$\leq$ \$400
C4P1 & C4P2	$\geq 97\%$	≥ 0.1°C/W	$\leq$ \$200

3.2.2 Optimization Results

There are eight optimization scenarios as described in Table.3.2. These eight scenarios lead to the eight best solutions, described in Table.3.2. Here, the cost is the sum of the price of coupling inductances and the semiconductors. In Level-1, there is one sub-problem. However, from Level-4 to Level-3, the number of sub-problems in each Level is more than one. It is trivial to display all the sub-problems of Pareto optimization at each Level. Hence, only one sample sub-problem for each Level, from Level-4 to Level-3, is shown for all eight scenarios. This sample sub-problem is also the sub-problem that leads to the best solution after Level-1 optimization.

Fig.3.2, Fig.3.3, Fig.3.4, Fig.3.5, Fig.3.6, Fig.3.7, Fig.3.8 and Fig.3.9 illustrate the optimization, using one sample sub-problem for each Level, in C1P1, C1P2, C2P1, C2P2, C3P1, C3P2, C4P1 and C4P2 respectively. Here, if the best solution has a configuration (N=n_b, M=m_b, L_f=L_{fb}, PSD=PSD_b), then a Level-4 sub-problem for (N=n_b, M=m_b, L_f=L_{fb}), Level-3 sub-problem for (N=n_b, M=m_b) are shown. Now for Level-2, one has two paths of optimization, which in turn modify the parameter of optimization. If the scenario involves Path#1, then the sub-problem for (N=n_b) is shown. If the scenario involves Path#2, then the sub-problem for (M=m_b) is shown.

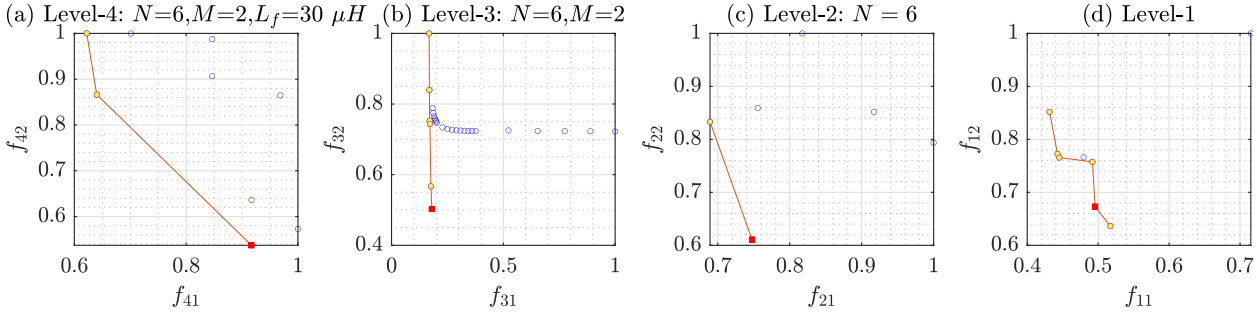

Figure 3.2: Illustration of C1P1 (■ best solution, −○ Pareto front, ○ dominated solutions)

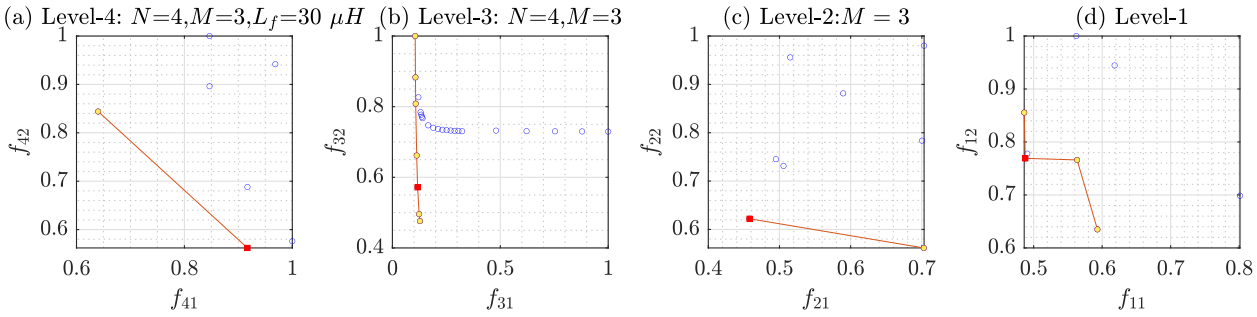

Figure 3.3: Illustration of C1P2 (■ best solution, −○ Pareto front, ○ dominated solutions)

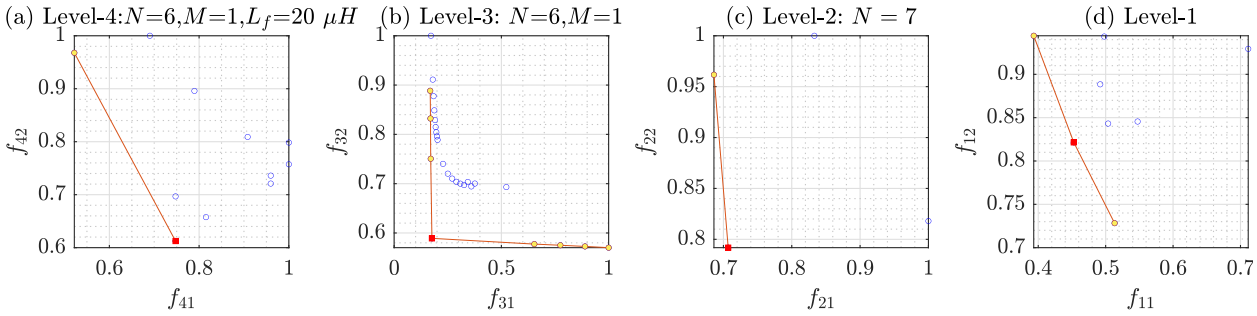

Figure 3.4: Illustration of C2P1 (■ best solution, −○ Pareto front, ○ dominated solutions)

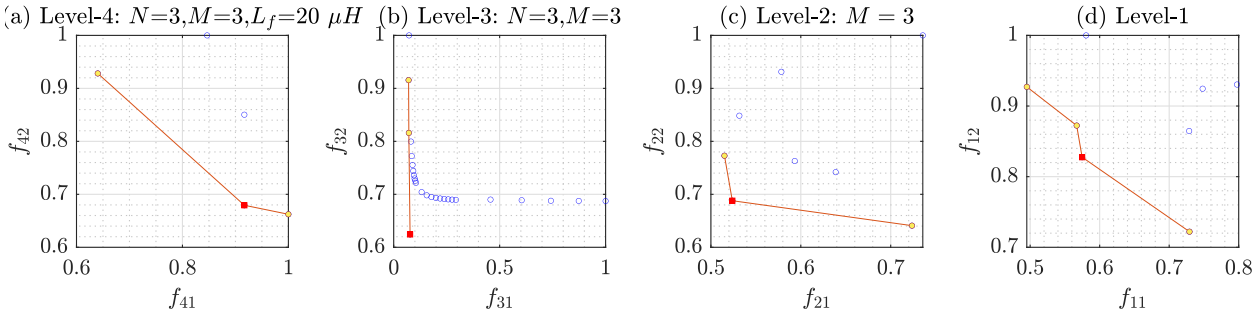

Figure 3.5: Illustration of C2P2 (■ best solution, −○ Pareto front, ○ dominated solutions)

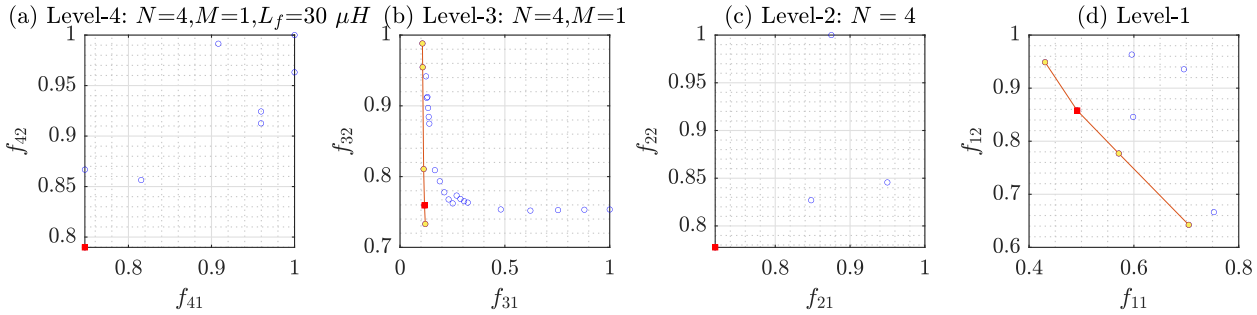

Figure 3.6: Illustration of C3P1 (■ best solution, −○ Pareto front, ○ dominated solutions)

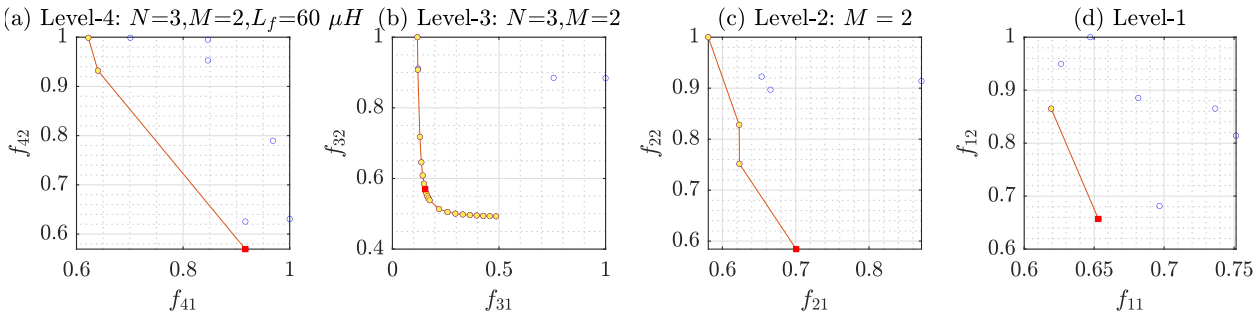

Figure 3.7: Illustration of C3P2 (■ best solution, −○ Pareto front, ○ dominated solutions)

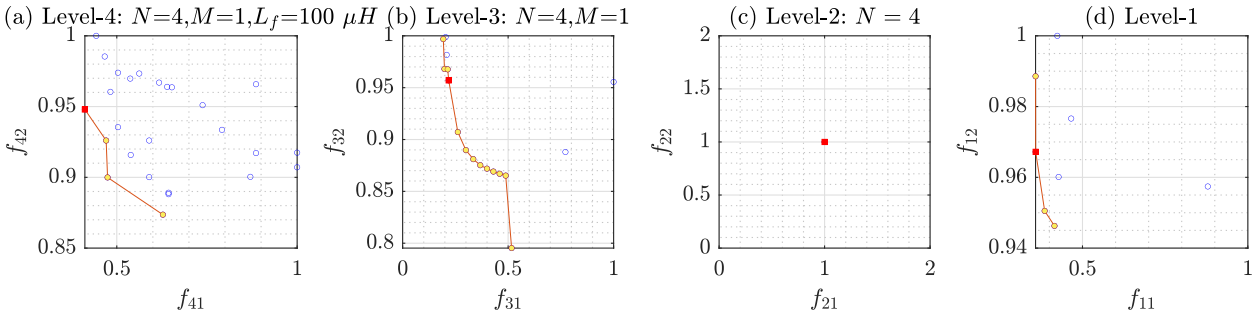

Figure 3.8: Illustration of C4P1 (■ best solution, –○ Pareto front, ○ dominated solutions)

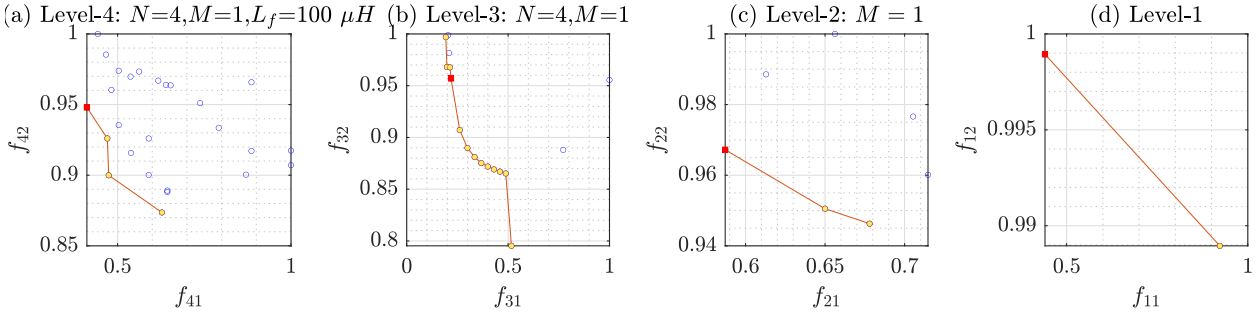

Figure 3.9: Illustration of C4P2 (■ best solution, –○ Pareto front, ○ dominated solutions)

The optimization post the Level-1 gives the best selection of (N, M, L_f, PSD). Table.3.5 presents the best solutions for the eight scenarios.

Table 3.5: Best solutions obtained for eight different scenarios of optimization

Parameter	#1	#2	#3	#4	#5	#6	#7	#8
PSD	C3M0060065K		C3M0060065K		C3M0060065K		IKP30N65H5	
L_f	30 μH	30 μH	20 μH	20 μH	30 μH	60 μH	100 μH	
(N, M)	$(6, 2)$	$(4, 3)$	$(6, 1)$	$(3, 3)$	$(4, 1)$	$(3, 2)$	$(4, 1)$	
m_f	921	1365	1381	2683	1365	897	413	
V_{dc}	179 V	179 V	179 V	179 V	179 V	179 V	179 V	
L_w	0.22 kg	0.26 kg	0.17 kg	0.22 kg	0.26 kg	0.48 kg	0.62 kg	
L_v	49.74 cm^3	59.99 cm^3	36.98 cm^3	50.94 cm^3	59.99 cm^3	113.71 cm^3	144.63 cm^3	
η	99.11 %	98.94 %	98.43 %	98.34 %	97.87 %	98.5 %	97.2 %	
$R_{th,ha}$	2.08°C/W	1.79°C/W	1.1°C/W	1.1°C/W	0.76°C/W	1.22°C/W	0.57°C/W	
Cost	$721.57	$686.14	$414.43	$514.72	$276.86	$362.71	$124.39	

Here one can notice that C4P1 and C4P2 lead to the same solution (#7 and #8). Where as the other six scenarios of optimization C1P1, C1P2, C2P1, C2P2, C3P1 and C3P2 leads to different best solutions #1, #2, #3, #4, #5 and #6 respectively. These eight best solutions are assessed for trade-off using objective functions similar to Level-1. The objective functions

are given as

$$f_{01} = \lambda_{011} L_{\$} + \lambda_{012} L_v + \lambda_{013} L_w + \lambda_{014} PSD_{\$} \tag{3.10}$$

$$f_{02} = \lambda_{021}(1/(1 + R_{th,ha})) + \lambda_{022}(100 - \eta) \tag{3.11}$$

If an equal priority of FOMs is considered for weights i.e. $\lambda_{011} = \lambda_{012} = \lambda_{013} = \lambda_{014} = 0.25$, $\lambda_{021} = \lambda_{022} = 0.5$, the trade-off can be seen in Fig.3.10(a). It can be seen that the best of the best solutions is given by #2. Besides, it can be noticed that solutions #6, #7 and #8 have become dominated solutions.

If the weights of FOMs are considered with much increased priority to $PSD_{\$}$ i.e. $\lambda_{011} = \lambda_{012} = \lambda_{013} = 1/9$, $\lambda_{014} = 2/3$, $\lambda_{021} = \lambda_{022} = 0.5$, the trade-off can be seen in Fig.3.10(b). Now it can be seen that solution #3 is the best of the best solutions. The solutions #1, #2, #3 and #5 have remained to be Pareto efficient. Whereas solutions #6, #7 and #8 have become non-dominated solutions, and solution #4 has become a dominated solution.

It can be noticed from Fig.3.10 that solutions #1, #2, #3 and #5 remained on the Pareto front irrespective of the weightage of FOMs.

3.2.2.1 Compact and High-Efficiency Solutions

As seen in Fig.3.10, solutions #1 and #2 are best in terms of efficiency and required thermal resistance of heat sink, as they are to the right extreme of the Pareto front, lowest f_{01} (3.10).

3.2.2.2 Compact and Low-Cost Solutions

Again from Fig.3.10, the left extreme of the Pareto front, which posses the solutions that are best in terms of coupling inductance FOMs and cost of semiconductor, lowest f_{02} (3.11), points to solution #5, with an equal priority of FOMs. If an increased priority for $PSD_{\$}$ is considered, then solutions #7 and #8 are best.

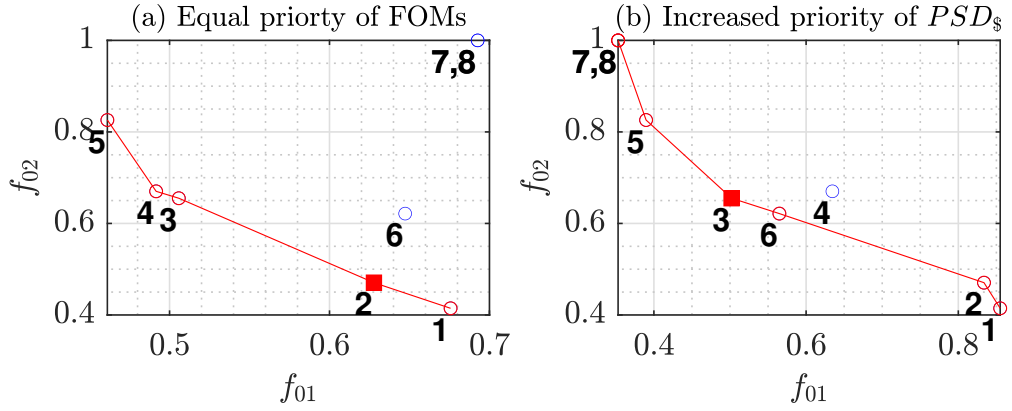

Figure 3.10: Level-0 optimization (■ best solution, –○ Pareto front, ○ dominated solutions)

3.2.3 Benefits

The best solutions for the eight scenarios are shown in Table.3.5. These eight best solutions, with two of them being the same, emerged as the best from a total maximum number of solutions: $8 \times 8 \times 28 \times 147 = 263424$, without enforcement of constraints. Now two of the best solutions #5 and #8 are selected to evaluate the benefits against a base case, leading to Improvement#5 and Improvement#8 respectively, shown in Table.3.6. The base case is selected as Level-4 optimization with N=1, M=1 and Si-IGBT technology. A lowered constraint on efficiency, $\eta \geq 95\%$, is considered along with the set of constraints listed in Table.2.7 to formulate the solution space and obtain the base case. The rationale for considering L_f=1000 μH is based on a literature application [117], a single-phase on-board bidirectional plug-in electric vehicle (PEV) charger that can provide reactive power support to the utility grid in addition to charging the vehicle battery.

The idea of providing a benefits evaluation is to showcase the efficacy of the algorithm in finding the best solutions from the available set of solutions. As shown in Table.3.6, the base case has a switch count of 4, and the best solutions (#5, #8) have a different switch count of 16. The improvements obtained concerning miniaturization and efficiency compared to the base case are because of the optimal choice of PSD, the optimal choice of L_f, the optimal choice of parallel switches (M), and the optimal choice of parallel interleaved H-bridges (N). These optimal selections that show the associated improvements are discovered through the proposed design framework.

As shown by Improvement#8, in Table.3.6, an improvement in all the FOMs is achieved. A much-increased improvement of all FOMs is achieved with a superior technology SiC-MOSFET, shown in Improvement#5, at an increase in investment. These two best solutions have effectively demonstrated the benefits of the proposed MO-HO-DF and its effectiveness in finding optimal solutions.

Table 3.6: Evaluation of benefits against a base case

Parameter	Base case	Improvement#8	Improvement#5
(N, M)	$(1, 1)$	-	-
PSD	IKW75N65EL5	-	-
L_f	1000 μH	$\downarrow$ 1 order	$\approx \downarrow\downarrow$ 2 orders
m_f	211	-	-
V_{dc}	207 V	$\downarrow$ 28 V	$\downarrow$ 28 V
L_w	5.67 kg	$\approx\downarrow$ 9 times	$\approx\downarrow\downarrow$ 22 times
L_v	1476.8 cm^3	$\approx\downarrow$ 10 times	$\approx\downarrow\downarrow$ 25 times
η	96.75 %	$\uparrow$ 0.45%	$\uparrow\uparrow$ 1.12%
$R_{th,ha}$	0.39°C/W	$\uparrow$ 0.18°C/W	$\uparrow\uparrow$ 0.37°C/W
Cost	\$149.53	$\downarrow$ \$25.14	$\uparrow$ \$127.33

3.2.4 Limitations

The obtained "best solutions" can be changed if one considers different component costs. While the configuration parameters N, M, L_f and the THD_i are absolute, the Price and the availability of some of the best devices are not. The cost of PSD and coupling inductance are considered with reasonable accuracy, and associated gate drive costs and sensor costs are not considered. Hence, a truly accurate prediction of the cost of an entire design is beyond the scope of this part of the thesis.

However, this is the first step in the path of developing cost-effective solutions with design optimization. Nevertheless, in principle, the optimization results even change when one changes constraints or associated functions.

3.3 Test Case Validation

The concept of optimization proposed in this part of the thesis makes use of the rigorous analysis of the power electronic systems with analytical mathematical calculations. Thus, it is of paramount importance to validate the current harmonic performance, power conversion efficiency and thermal performance. The validation is performed using Piecewise Linear Electrical Circuit Simulation (PLECS) software.

3.3.1 Current Harmonic Performance

The validation of current harmonic performance is presented for the case of the best solution #2 and #5, shown in Table.3.5. i.e. N=4, L_f=30μH. This configuration requires a m_f=1365, to meet the current harmonic performance targets as specified in Table.2.7. This m_f translates into an effective output switching frequency of the total output current as $2 \times N \times m_f \times 60 = 655.2$ kHz, thus enabling a high-bandwidth current control.

Now, for N=4,L_f=30μH with m_f=1365, THD_i^* is evaluated for different operating currents, I^*, as shown in Table.3.7 using (2.6).

Table 3.7: THD_i^* Vs Current phase angle (ϕ) from theoretical calculations

Case	m_a	δ (rad)	I^* (A)	THD_i^* (%)
1	0.94906	0.0011769	$50 \angle 0°$	0.996
2	0.94956	9.632e-05	$50 \angle 45°$	0.996
3	0.94919	−0.0010404	$50 \angle 90°$	0.996
4	0.94817	−0.0015695	$50 \angle 135°$	0.998
5	0.94709	−0.0011793	$50 \angle 180°$	0.999
6	0.94659	−9.6623e-05	$50 \angle 225°$	0.999
7	0.94696	0.0010429	$50 \angle 270°$	0.999
8	0.94799	0.0015698	$50 \angle 315°$	0.998

The simulation is performed in PLECS with ARSPWM. The asymmetrical regular sampling involves the sampling of the modulation signal twice in any carrier interval, and the modulation signal needs a Phase Delay Compensation (PDC) [43]. This is achieved by advancing the modulation signal before sampling by a phase angle given as

$$pdc_{\phi} = \frac{90^{\circ}}{m_f} \tag{3.12}$$

As can be seen in Fig.3.12, $m_a(t)$ is the original signal. $m_a(t)$ (with PDC) is the phase advanced form of $m_a(t)$. $\psi_{s1}(t)$ is the carrier signal of 1st H-bridge. At every peak of $\psi_{s1}(t)$, $m_a(t)$ (with PDC) is sampled and hold to give $m_a(t)$ (discrete).

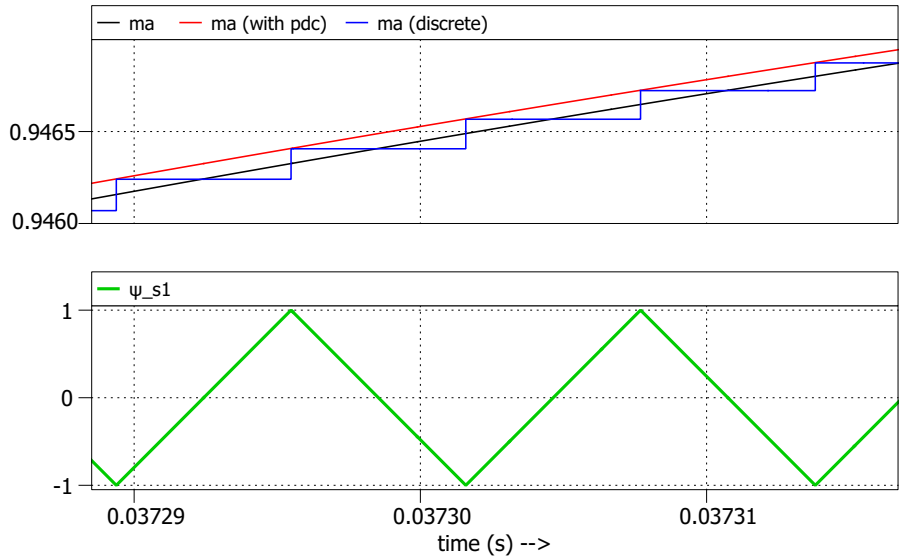

Figure 3.11: Discretization of the modulation signal of 1st H-bridge (segmented view)

The simulation results for different cases shown in Table.3.7, can be seen in Fig.3.12 and Table.3.8. Where $i: x^{\circ}$, refers to the current (i) A, injected into the grid at an angle of x°. Here, the grid voltage is the reference phasor at 0°, measured in Volts.

THD_{i} from the simulation result is added for comparison in Table.3.8. The total output current, I_s, obtained from the simulation result is shown in Table.3.8. Here one can also see the difference between the theoretical value of current (I^*) and simulation result (I_s), signifying the imbalance of parallel H-bridge output currents. The maximum difference in the currents can be noticed as 0.418% of the fundamental component. Thus, the simulation results effectively show the bi-directional power flow capability of the proposed grid interface, meeting the current harmonic performance targets.

Fig.3.13 shows the effect of the phase shift of carriers on the current ripple cancellation for the Case: 1(Table.3.7), injection of rated current (A) with Unity Power Factor (UPF) into the grid.

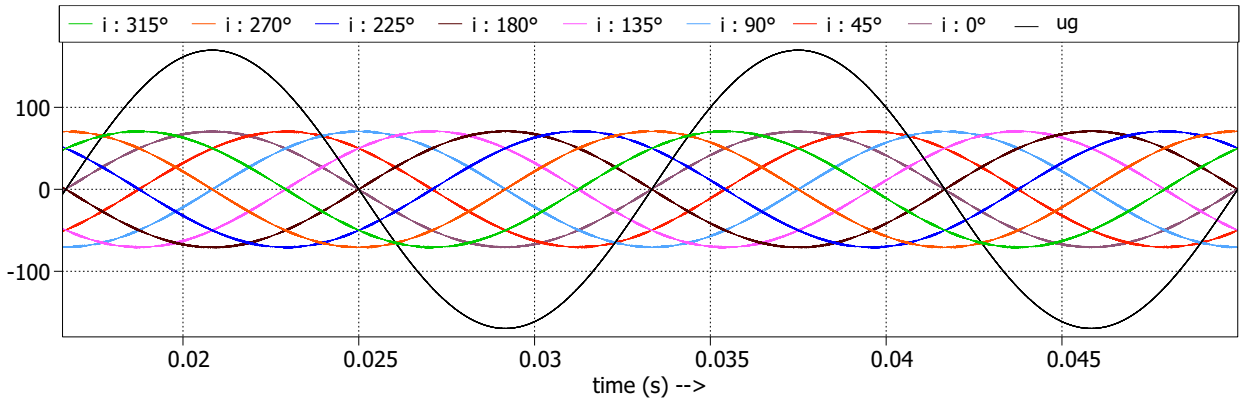

Figure 3.12: Rated current at different phase angles into the grid (units

Table 3.8: THD_i Vs Current phase angle (ϕ) from Simulation

Case	I (A)	THD_i (%)	$I^* - I_s$ (A)
1	$49.861 \angle -0.18°$	0.999	$0.209 \angle 48.36°$
2	$49.789 \angle 44.98°$	1.000	$0.212 \angle 49.70°$
3	$49.855 \angle 90.139°$	0.9997	$0.189 \angle 50.19°$
4	$49.996 \angle 135.03°$	0.998	$0.026 \angle 53.70°$
5	$50.024 \angle 180.039°$	0.999	$0.042 \angle 54.84°$
6	$50.002 \angle 225.004°$	1.000	$0.004 \angle 105.19°$
7	$50.046 \angle 269.958°$	0.999	$0.059 \angle 51.41°$
8	$50.001 \angle 315.082°$	0.998	$0.072 \angle 224.25°$

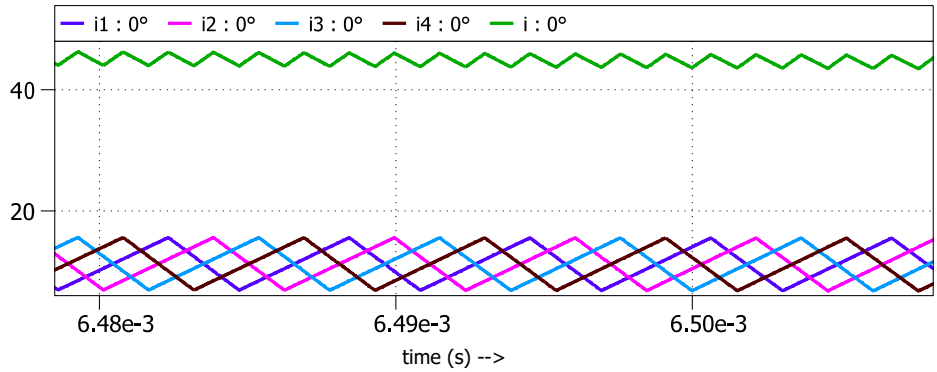

Figure 3.13: Injection of rated current with UPF into the grid (segmented view)

In the case of '$N = 4$', interleaved H-bridges with unipolar modulation, the odd sideband harmonics will appear around the integer multiples of effective frequency modulation ratio, $2 \times N \times m_f = 10920$. The odd sideband harmonic amplitudes of $i(t)$ around $8m_f$ are computed using (2.6) for the Case, injection of rated current with UPF into the grid; These harmonics

are shown in Fig.3.14 and compared with the Fast Fourier Transform (FFT) of PLECS simulation, that shows the peak values of each component. The I_{hl} of any harmonic, as specified in Table.2.7 is less than 0.8% of the fundamental component: $50\times\sqrt{2}\times0.8/100 = 0.56$ A. Based on the comparison between the computation result and simulation result, it can be concluded that (2.6) provides an accurate calculation of the current harmonics of the interleaved H-bridges.

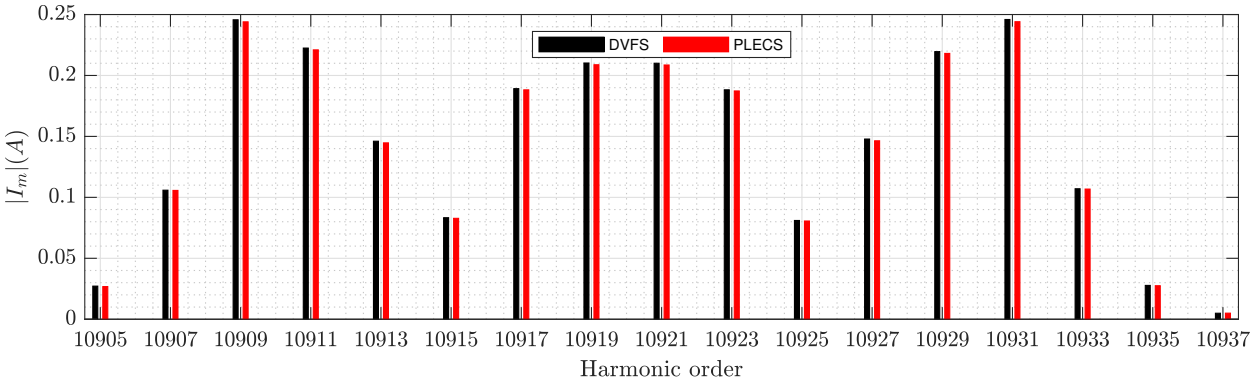

Figure 3.14: FFT Verification for first side band harmonics

3.3.2 Thermal Performance Vs Efficiency

The validation is presented for the best solution#5 presented in Table.3.5 using Case: 1(Table.3.8). The simulation is performed in the PLECS with Wolfspeed (formerly CREE Inc.) provided .xml file of the Three-Dimensional (3D)-switch model in conjunction with thermal modelling to calculate the efficiency and verify thermal performance. Fig.3.15 shows the continued-fraction circuit for the junction to case thermal behaviour of the switch. This continued-fraction circuit reflects the real, physical setup of the power semiconductor. A first-order thermal capacitance model for the heat sink is considered.

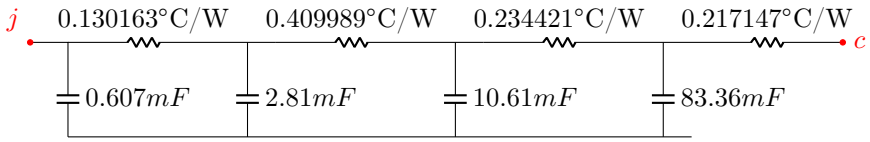

Figure 3.15: Continued-fraction circuit (Cauer model) of C3M0060065K

Fig.3.16(a) shows the variation of efficiency (η) with the junction temperature of the switch. Fig.3.16(b) shows the actual junction temperature averaged over the fundamental period ($T_{j,av}$). The steady-state values for power conversion efficiency (η) and $T_{j,av}$ are obtained as 98.07% and 121.36°C, respectively. The efficiency varies slightly with the junction temperature. The obtained value of junction temperature is lower, and efficiency is higher than their respective projected values for best solution#5, as shown in Table.3.5. It is because the design of the heat sink considers power losses specified at maximum junction temperature.

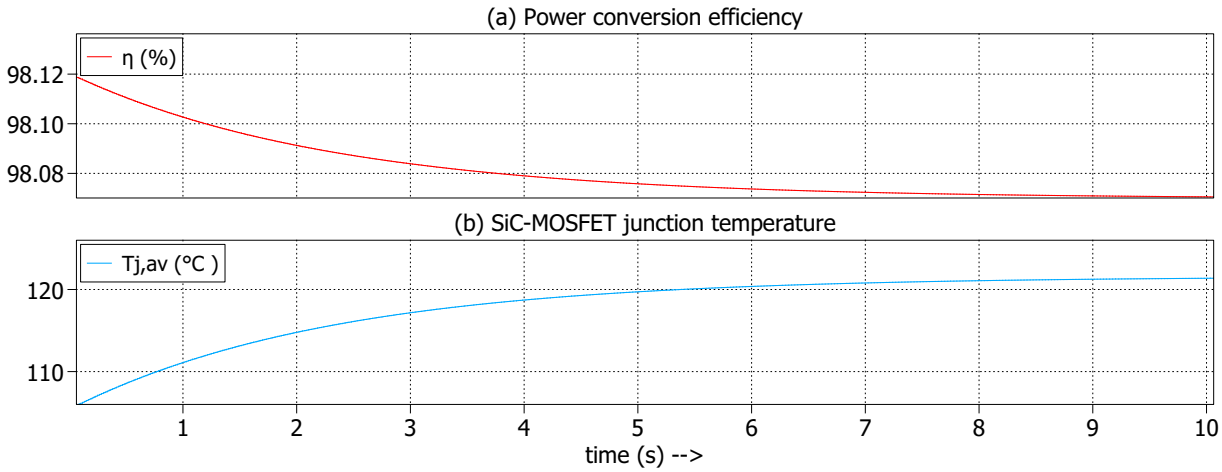

Figure 3.16: Thermal performance vs Efficiency

3.4 Summary

This chapter has presented the optimization algorithm, optimization results and a test case validation for one of the best solutions obtained. Firstly, a definition of what is meant by the best solution is provided. i.e., the solution closest to the utopia point. Second, the rationale for the choice of objective functions at each level is provided for the proposed four-level hierarchical framework. Third, an optimization algorithm for the four-level hierarchical framework is proposed. Fourth, the optimization results are obtained for a total of four cases, where each case of optimization is performed in two paths.

Fifth, a base case is selected to evaluate the effectiveness of the best solutions obtained from design optimization. Numerous publications that concern the improvement of power conversion efficiency dealt with topology and control. However, against conventional wisdom, a step has been taken to see the impact of the choice of the PSD. In other words, if the goal is to improve efficiency, can the right choice of PSD make a difference? In a power conversion system design, any trade-off between two conflicting objectives, improvement in one of the objectives is achieved at the expense of another objective. Can the inclusion of a non-physical entity (cost/price) make a difference in the optimization? It is discovered that the inclusion of the choice of PSD, semiconductor cost, and filter inductance cost into the optimization led to the improvement in all the FOMs, as evident from Improvement#8. Specifically, *through the proposed hierarchical optimization, when the objective functions have a scientific basis for being conflicting in nature, improvement is obtained in all FOMs.*

Sixth, one of the best solutions is selected for validation with PLECS simulation software. The selected best solution validates the harmonic components and total harmonic distortion. A 360° operation of the power conversion system is shown, and THD is validated for the 360° range of operation.

Part II

Philosophy of Controller Design for a Photovoltaic Inverter

Chapter 4

Figures of Merit

> Out of compassion for them, I, who dwell within their hearts, destroy the darkness born of ignorance, with the luminous lamp of knowledge.
>
> *Bhagavad Gita (The Song by God): Chapter 10, Verse 11.*

4.1 PV-fed Grid-connected H-bridge

The main objective of this section is to determine the plant transfer functions of PV-fed grid-connected H-bridge, rated 6 kVA (120 V /50 A), 60 Hz AC grid interface [44].

4.1.1 LTI Model

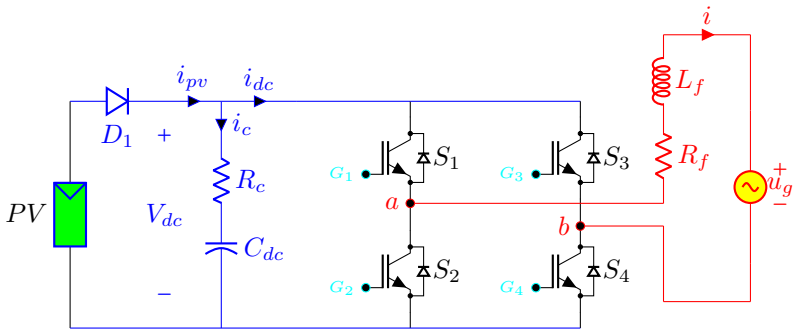

Figure 4.1: PV-fed H-bridge interfaced to the utility grid

Equations representing the dynamics of power conversion system shown in Fig. 4.1 by neglecting the Equivalent Series Resistance (ESR) of the capacitor, R_c, are as follows

$$v_{ab}(t) = \underbrace{\left(R_f i(t) + L_f \frac{di(t)}{dt}\right)}_{v_l(t)} + u_g(t) \tag{4.1}$$

$$p_{dc} = v_{dc} i_{pv} + \frac{d}{dt}\left(\frac{1}{2} C_{dc} v_{dc}^2\right) \tag{4.2}$$

$$p_{ac} = u_g i + R_f i + \frac{d}{dt}\left(\frac{1}{2} L_f i^2\right). \tag{4.3}$$

From (4.1), one can obtain the linearized small signal model concerning the regulation of output current as

$$G_i(s) = \frac{\tilde{i}(s)}{\tilde{v}_{ab}(s)}\bigg|_{\tilde{u}_g(s)=0} = \frac{1}{R_f + sL_f}. \tag{4.4}$$

Equation (4.4) is valid only for frequency variations much smaller than the switching frequency as the averaging process is performed over a switching period. As a thumb rule [118], the equivalent model may be taken to be a good approximation of the real converter for a dynamic range of about a tenth of the switching frequency.

A feed-forward loop to compensate for the impact of the small variations in grid voltage (u_g) and its block diagram concerning the regulation of output current is shown in Fig. 4.2.

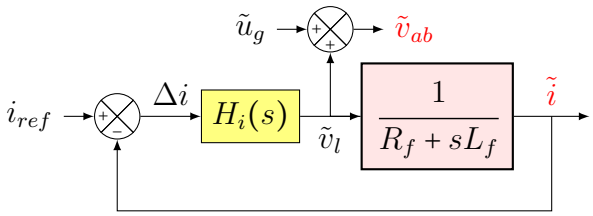

Figure 4.2: Regulation of output current

From (4.2) and (4.3), with $p_{ac} = p_{dc}$, the linearized small signal model concerning the regulation of DC bus voltage can be obtained as

$$G_v(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{i}(s)} = \frac{\hat{U}_g + 2\hat{I}R_f + sL_f\hat{I}}{\hat{I}_{pv} + sC_{dc}\hat{V}_{dc}}. \tag{4.5}$$

Here, if $x(t)$ is a continuous time-varying signal then its linearized small signal model will have the small perturbation component and DC component represented by $\tilde{x}$ and $\hat{X}$, respectively. From (4.5), the block diagram concerning the regulation of DC bus voltage is shown in Fig. 4.3. It can be observed that the typical operating region of a PV Array involves negative impedance characteristics, accordingly, the voltage loop is considered.

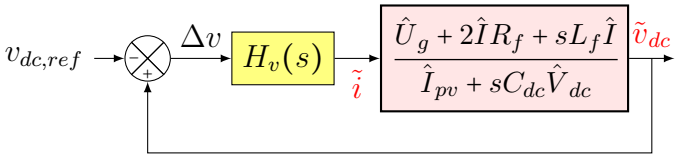

Figure 4.3: Regulation of DC bus voltage

From Fig. 4.2 and Fig. 4.3, it is evident that the output of $H_v(s)$ corresponds to the peak value of current reference i_{ref}. This peak value is multiplied by a sinusoidal signal,

which is regulated by the controller $H_i(s)$. Thus the voltage regulation loop is much slower in comparison to the current regulation loop. For this specific case, as the DC bus voltage contains a second-order harmonic, the controller $H_v(s)$ should also act as a low pass filter to the second harmonic error in Δv.

4.1.2 Choice of the Configuration of PV Array

In this part of the thesis, a PV Array with 75 panels of Canadian Solar Inc. make is considered. Each panel can deliver a power of 80.15W at its Maximum Power Point (MPP). The panels are configured as five parallel strings, with each string having 15 panels as a series connected. At an irradiance of 1000W/m^2, the considered configuration of the PV array would have V-I and Power-Voltage (P-V) characteristics for two ambient temperatures as shown in Fig. 4.4. Hence the considered configuration can deliver a maximum power of 6011.25W at an ambient temperature, irradiance, and operating voltage values of 25°C and 1000W/m2 and 262.5V, respectively. These operating conditions also correspond to a PV Array current of 22.9A.

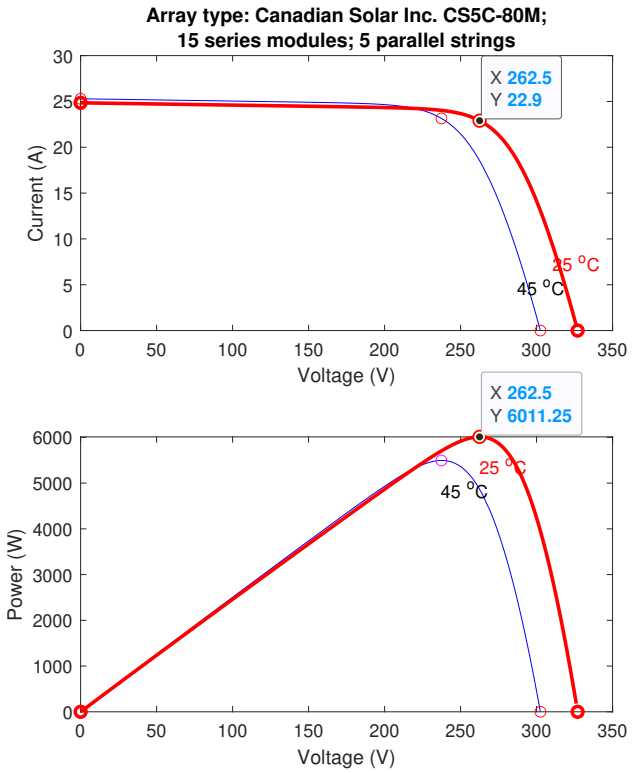

Figure 4.4: Characteristics of PV array for irradiance of 1000 W/m2

4.1.3 Selection of DC Bus Capacitance

In the following analysis, for design simplification, the ESR of the capacitor, R_c, is neglected. In the context of Fig. 4.1, the sizing of the DC bus capacitor [39, 119] is determined based on the ability

- to filter high-frequency switching currents, thereby a smooth DC bus voltage is achieved.
- to provide energy buffer between mains cycles.

In Fig. 4.1, the instantaneous AC power delivered to the grid is given as

$$p_g = \sqrt{2}U_g \sin\omega_1 t \times \sqrt{2}I_g \sin(\omega_1 t - \phi). \tag{4.6}$$

When $\phi = 0$, the instantaneous AC power is given as

$$p_g = U_g I_g \left(1 - \cos(2\omega_1 t)\right). \tag{4.7}$$

Fig. 4.5 shows the visualization of (4.7) for one cycle of grid voltage. Where $E_{abs} = E_c$ and $E_{del} = E_c$ are the energy to be stored and energy to be delivered, respectively, in a quarter time period of the gird voltage.

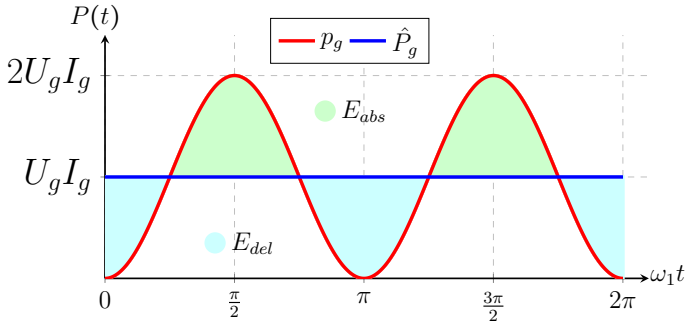

Figure 4.5: Instantaneous power

The maximum energy to be handled by the DC bus capacitor is given as

$$E_c = 2\int_0^{\frac{\pi}{4\omega_1}} \left(p_g - \hat{P}_g\right) dt = \frac{1}{2}C_{dc}\left(V_{dc-}^2 - V_{dc+}^2\right). \tag{4.8}$$

Where V_{dc+} and V_{dc-} are the maximum voltage and minimum voltage, respectively, across the capacitor. This can be further simplified as

$$E_c = 2U_g I_g \int_0^{\frac{\pi}{4\omega_1}} \cos(2\omega_1 t)\, dt \tag{4.9}$$

$$E_c = C_{dc}\underbrace{\left(\frac{(V_{dc+} + V_{dc-})}{2}\right)}_{\overline{V_{dc}}}\underbrace{(V_{dc+} - V_{dc-})}_{\Delta V_{dc}}. \tag{4.10}$$

Where $\overline{V_{dc}}$ and ΔV_{dc} are the average voltage and voltage ripple, respectively, of the DC bus capacitor. Now, upon integration and simplification of the above two equations

$$E_c = \frac{U_g I_g}{\omega_1}\left(\sin(2\omega_1 t)\Big|_0^{\frac{\pi}{4}}\right) = C_{dc}\overline{V_{dc}}\,\Delta V_{dc}. \tag{4.11}$$

upon applying integration limits and simplifying the equations

$$E_c = \frac{U_g I_g}{\omega_1} = C_{dc}\overline{V_{dc}}\,\Delta V_{dc}. \tag{4.12}$$

The required value of DC bus capacitance is given as

$$C_{dc} = \frac{U_g I_g}{\omega_1 \overline{V_{dc}}\,\Delta V_{dc}}. \tag{4.13}$$

If one considers the case: $\overline{V_{dc}} = 262.5\text{V}$, $\Delta V_{dc} = 8\text{V}$, $U_g = 120\text{V}$, $I_g = 50\text{A}$, and $\omega_1 = 2 \times \pi \times 60$ rad/sec, the required DC bus capacitance will be

$$C_{dc} = \frac{120 \times 50}{2 \times \pi \times 60 \times 262.5 \times 8} = 7.5788\text{mF}. \tag{4.14}$$

4.1.4 Dead-Time Compensation

To avoid shoot-through of the DC bus through the switches of the same leg, shown in Fig. 4.1, a dead-time, t_{dt}, is a must between the gating signals of the turn-off of the outgoing switch and the turn-on of the incoming switch. This delay introduces a load-dependent magnitude and phase error in the output voltage [120] i.e., when the current is positive, based on average value theory, the net effect over one carrier cycle is the loss of average voltage δv. Similarly, for negative current, there is a net gain of average voltage δv. The approximate δv based on current feedback method is given as [120]

$$\delta v = \left(\frac{t_{dt} + t_{on} + t_{off}}{T_s}\right)[\overline{V_{dc}} - V_{sat} + V_d] + \left(\frac{V_{sat} - V_d}{\overline{V_{dc}}}\right) m_a(t) + \frac{V_{sat} + V_d}{2}. \tag{4.15}$$

Where t_{on} is the switch turn-on delay time, t_{off} is the switch turn-off delay time, T_s is the time period of the carrier signal, V_{sat} is the on-state voltage drop across the switch, V_d is the diode forward voltage drop and $m_a(t)$ is the modulation signal. In practice, if the driver of the switches of the inverter has a relatively large value of dead-time, then it is necessary to compensate for the effect of the dead-time, as the distortion-related harmonics of fundamental frequency become more pronounced. The dead-time compensation can be accomplished by providing compensation to the modulation signal with the feed-forward term v_{dt} at the summing junction for $\tilde{v}_{ab}$, as shown in Fig. 4.2. Here v_{dt} is given as

$$v_{dt} = \begin{cases} +\delta v & \text{if } i(t) > 0 \\ -\delta v & \text{otherwise.} \end{cases} \tag{4.16}$$

4.1.5 Plant Transfer Functions

The choice of parameters for the specific problem considered in this part of the thesis is based on [44], and the parameters are as follows: $R_f = 10\text{m}\Omega$, $L_f = 1\text{mH}$, $C_{dc} = 7.5788\text{mF}$, $\hat{U}_g = 120\sqrt{2}\text{V}$, $\hat{I} = 50\sqrt{2}\text{A}$, $\hat{V}_{dc} = 262.5\text{V}$, and $\hat{I}_{pv} = 22.9\text{A}$. The obtained transfer functions

of the plants can be seen as

$$G_i(s) = \frac{\tilde{i}(s)}{\tilde{v}_{ab}(s)}\bigg|_{\tilde{u}_g(s)=0} = \frac{1}{0.001s + 0.01} \tag{4.17}$$

$$G_v(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{i}(s)} = \frac{0.05s + 171.1}{1.989s + 22.9}. \tag{4.18}$$

4.2 Controllers and Control Block Diagrams

PI controllers are very effective in the regulation of DC signals due to infinite gain at zero frequencies, whereas they provide reduced performance for the regulation of AC signals. Here, PMR controllers find a place, due to the feasibility to increase the gain at AC frequencies [51]. In this section, some insights into the two types of controllers used in this part of the thesis, are presented.

4.2.1 Type-II PI Controller

A PI controller has one pole and one zero. A Type-II PI controller [37, 121] of the form as shown in (4.19), has an additional pole in comparison to a PI controller. The additional pole provides more attenuation of harmonics and more importantly simplifies the calculation of the controller parameters. This simplification would be useful in building algorithms.

$$T_{2x}(s) = k_{2x}\left(\frac{1 + s/\omega_{lx}}{s/\omega_{lx}}\right)\left(\frac{1}{1 + s/\omega_{hx}}\right) \tag{4.19}$$

The asymptotic bode plot of (4.19) can be seen [121] in Fig. 4.6. The limit on phase boost that one can achieve with (4.19) can be noted as $0° < boost < 90°$. A Type-II PI controller can be used for the regulation of DC voltage and AC. Thus the respective controllers can be identified as

$$T_{2v}(s) = k_{2v}\left(\frac{1 + s/\omega_{lv}}{s/\omega_{lv}}\right)\left(\frac{1}{1 + s/\omega_{hv}}\right) \tag{4.20}$$

$$T_{2i}(s) = k_{2i}\left(\frac{1 + s/\omega_{li}}{s/\omega_{li}}\right)\left(\frac{1}{1 + s/\omega_{hi}}\right). \tag{4.21}$$

4.2.2 PMR Controller

A typical Proportional+Resonant (PR) controller with a 3dB bandwidth $2\omega_c$, to regulate a signal of frequency ω_0, is given as [51]

$$H_1(s) = k_p + \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2}. \tag{4.22}$$

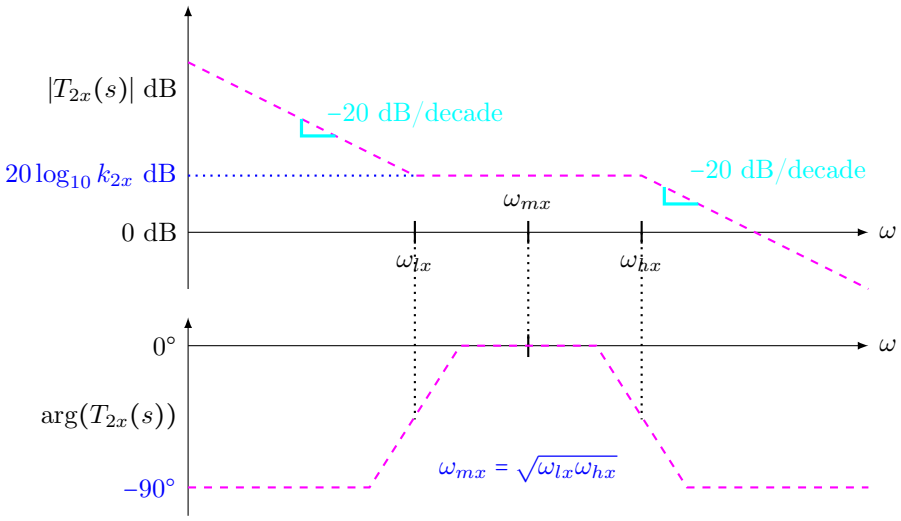

Figure 4.6: Asymptotic bode plot of $T_{2x}(s)$

To gain some insights, (4.22) can be rewritten as

$$H_1(s) = k_p \frac{N(s)}{D(s)} \tag{4.23}$$

where

$$N(s) = \left(\frac{s}{\omega_0}\right)^2 + \left(\frac{s}{\omega_0 Q_z}\right) + 1 \tag{4.24a}$$

$$D(s) = \left(\frac{s}{\omega_0}\right)^2 + \left(\frac{s}{\omega_0 Q_p}\right) + 1 \tag{4.24b}$$

where

$$k_z = 1 + \frac{k_i}{k_p}, \qquad Q_p = \frac{\omega_0}{2\omega_c}, \qquad Q_z = \frac{\omega_0}{2\omega_c k_z} = \frac{Q_p}{k_z}. \tag{4.25}$$

As seen in (4.23), $N(s)$ and $D(s)$ are second-order polynomials. Q_p and Q_z are the quality factors of $1/D(s)$ (i.e., of poles) and $N(s)$ (i.e., of zeroes), respectively. The resonant gain of $H_1(s)$ in dB i.e., on a logarithmic scale, is a scalar addition of $20\log(k_p)$ and resonant gains provided by $N(s)$ and $1/D(s)$. For $Q_p > 2$ and $Q_z > 2$, the asymptotic bode plots [122] of $1/D(s)$ and $N(s)$ is as shown in Fig. 4.7 and Fig. 4.8, respectively. Thus for $Q_p > 2$ and $Q_z > 2$, the approximate resonant gain of $H_1(s)$ can be given as

$$20\log\left(k_p \frac{Q_p}{Q_z}\right) = 20\log\left(k_p k_z\right) = 20\log\left(k_p + k_i\right). \tag{4.26}$$

As one can see in (4.25), $Q_p > 2$ always holds good, but Q_z gets influenced by k_i and k_p. Q_z takes values far lower than 2, and (4.26) would not be a good estimate. To calculate a

precise value of open loop transfer function gain in the current loop due to PMR controller, MATLAB function `bode` () can be used as explained in Algorithm 4.

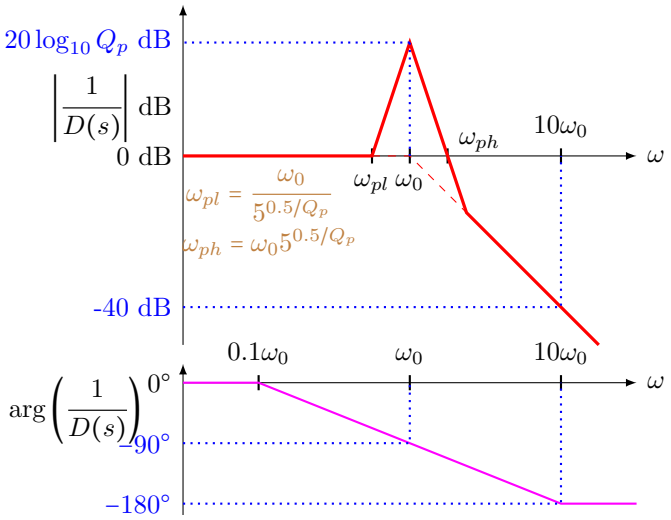

Figure 4.7: Asymptotic bode plot of $1/D(s)$ for $Q_p > 2$

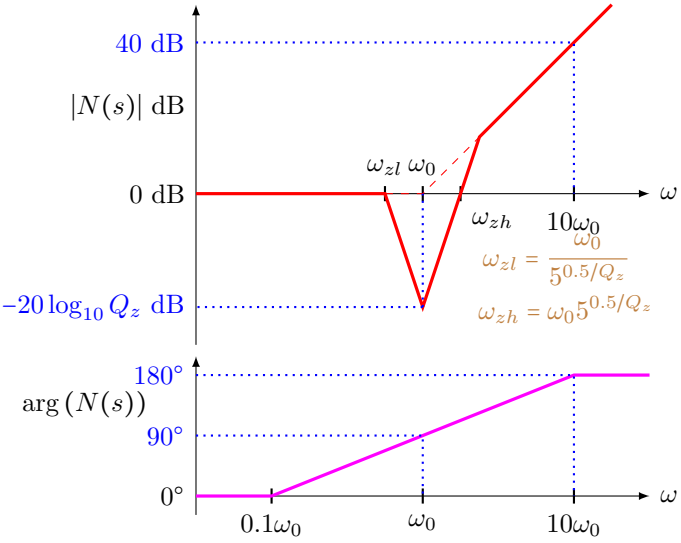

Figure 4.8: Asymptotic bode plot of $N(s)$ for $Q_z > 2$

Equation (4.22) shows the expression of PMR controller for a single frequency ω_0. For the system shown in Fig. 4.1, the regulator responsible for current regulation as described in Fig. 4.2 should track the AC signal with fundamental frequency ω_0 and reject (i.e., attenuate) the odd harmonic multiples of ω_0. To achieve the said objective, a controller as described in (4.27) is needed [51, 52].

$$H_r(s) = k_p \sum_{n=1,3,5,7,9} H_n \tag{4.27}$$

Where

$$H_n(s) = k_p \left[\frac{\left(\frac{s}{n\omega_0}\right)^2 + \left(\frac{s}{n^2\omega_0 Q_z}\right) + 1}{\left(\frac{s}{n\omega_0}\right)^2 + \left(\frac{s}{n^2\omega_0 Q_p}\right) + 1} \right] \tag{4.28}$$

Equation (4.27) in the context of Fig. 4.2, can be visualized as shown in Fig. 4.9 i.e., $H_r(s)$ would be used for the realization of $H_i(s)$. As can be seen from (4.27) and (4.28), with the selection of n and ω_0, one has

$$H_r(s) = g(\boldsymbol{\beta_r}) = g(k_i, k_p, \omega_c) \tag{4.29}$$

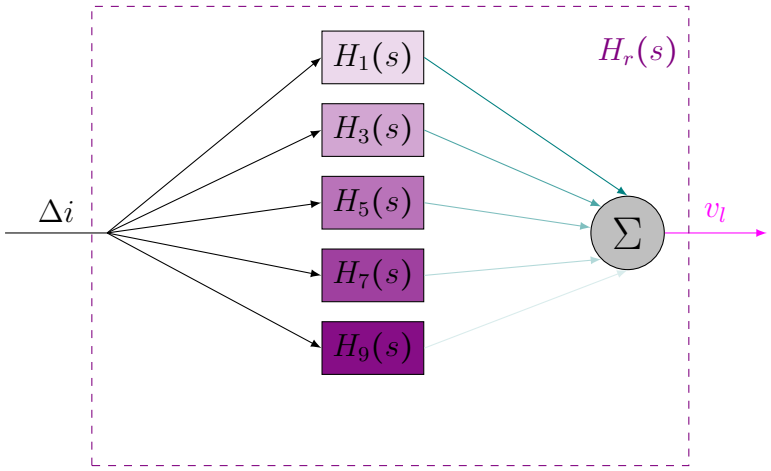

Figure 4.9: Structure of PMR controller for the AC current regulation

4.2.3 Control Block Diagrams

The control block diagram concerning the power conversion system as shown in Fig. 4.1 is drawn in Fig. 4.10. This block diagram is derived from Fig. 4.2 and Fig. 4.3 with the inclusion of dead-time compensation [120]. $f_s = 211 \times 60 = 12660$Hz is considered. The gate signals from the ARSPWM block are processed to the dead-time block to introduce dead-time between the switches of the same leg. The dead-time block outputs gate signals g_1, g_2, g_3 and g_4 to be applied to the gates G_1, G_2, G_3 and G_4, respectively of the switches S_1, S_2, S_3 and S_4.

To see the effectiveness of PMR controller optimization, a base case and optimization case are considered. In both cases, the DC bus voltage regulation is performed using the Type-II PI controller. The control block diagram concerning the base case is shown in Fig. 4.11. The base case is a scenario where the AC regulation is achieved using a Type-II PI controller. The control block diagram concerning the general optimization case is shown in Fig. 4.12. The general optimization case is a scenario where the AC regulation is achieved using a PMR controller.

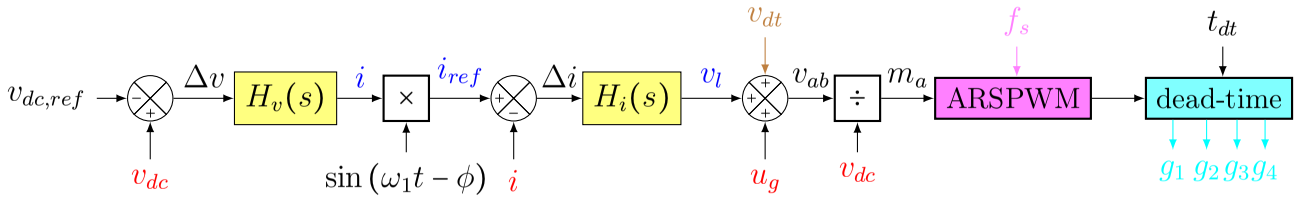

Figure 4.10: Block diagram of closed-loop control of PV-fed grid-connected H-bridge

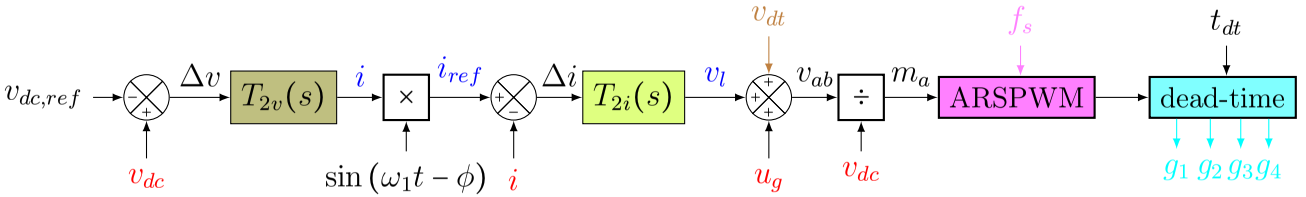

Figure 4.11: Base case of optimization: block diagram of closed-loop control of PV-fed grid-connected H-bridge

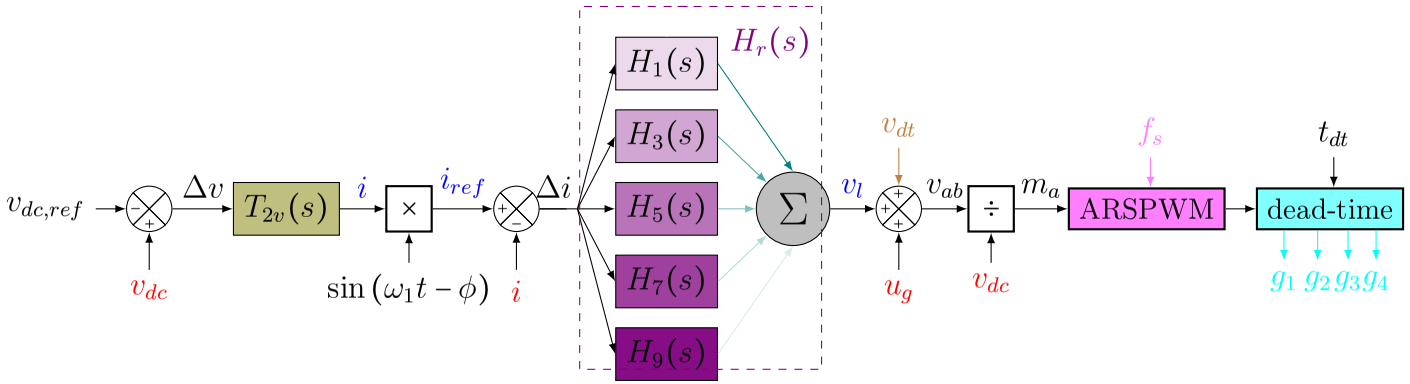

Figure 4.12: General optimization case: block diagram of closed-loop control of PV-fed grid-connected H-bridge

4.3 Computation of FOMs

The first step to analyzing the transient and steady-state behaviour of a control system is to obtain the mathematical model of a system, as explained in Section 4.1. Then one can use time-domain and/or frequency-domain analysis to understand the system behaviour and modify those behaviours using appropriate controllers.

Control systems are inherently time-domain systems subjected to time-varying inputs. The system behaviour can be determined through standard test signals such as unit impulse, unit step or unit ramp. Specifically, as the nature of the transient response depends on the system poles and not on the type of input, one can use any of the standard test signals. On the other hand, a switched-mode power conversion system design is inherently a frequency-domain system. In the frequency-domain analysis of a LTI system, a sinusoidal signal with a wide range of frequencies is applied to the system, i.e., to draw a bode plot.

Though it is possible to predict the time domain behaviour of the system from its frequency domain characteristics, there is no specific equation that one can use to map the characteristics and vice-versa. Thus, in this part of the thesis, a unit-step input is used for time-domain characteristics evaluation, which is sufficient to reveal the nature of the transient response. A bode plot is used for the frequency-domain characteristics evaluation, which is very important from a power electronics systems design standpoint.

4.3.1 FOMs with Type-II PI Controller

Let $G_x(s)$ be the plant transfer function. t_{rx} and m_{px} are the rise time and percentage overshoot, respectively, of the unity feedback transfer function of $G_x(s)T_{2x}(s)$. ϕ_{mx} and ω_{gcx} are the phase margin and gain cross-over frequency, respectively, of $G_x(s)T_{2x}(s)$. Where $x \in \{i, v\}$, $x = i$ denotes the current loop and $x = v$ denotes the voltage loop. The FOMs with Type-II PI controller for the formulation of the convex optimization problem in obtaining $T_{2v}(s)$ and $T_{2i}(s)$ are detailed in Table 4.1. Here ω_s is the switching frequency (f_s) in rad/sec. It can be observed that FOMs considered for convex optimization are non-negative and all have their goal as a problem of minimization or target type.

Table 4.1: FOMs and Goals with Type-II PI Controller

S.No.	FOM	Goal	Constraint
1	t_{rx}	Minimize	-
2	m_{px}	Minimize	$1\% \leqslant m_{px} \leqslant 50\%$
3	$90 - \phi_{mx}$	Minimize	$10^\circ \leqslant \phi_{mx} \leqslant 90^\circ$
4	ω_{gcx}	Target	$\omega_{gcv} = \omega_s/1000$ $\omega_{gci} = \omega_s/10$

Algorithm 3 describes the method to obtain the FOMs. The required controller parameters of $T_{2x}(s)$ are computed using `typePI` (arguments), then the FOMs for the convex optimization of Type-II PI controller are evaluated. Here, `allmargin` (arguments) usage is

optional and of trivial nature for this algorithm. However, `allmargin` (arguments) is used as an exception handler for any incorrect input of the transfer function $G_x(s)$ or any other unforeseen errors with the target specifications. All the computed data for each value of phase margin, ϕ_m, is stored in a matrix $\mathbf{N_x}$, where each row contains the values of t_{rx}, m_{px} and associated controller parameters. Fig. 4.13(a) and Fig. 4.13(b) show the computed data using Algorithm 3 of $G_v(s)T_{2v}(s)$ and $G_i(s)T_{2i}(s)$, respectively.

Algorithm 3: FOMs with Type-II PI controller

```
input  : Gx(s), ωgcx
output: Nx
/* MATLAB function                                              */
/* MATLAB struct array field                                    */
1  i ← 1
2  for j ← 10 to 90 by 0.1 do
3      [T2x(s), kx, ωlx, ωhx] ← typePI (Gx(s), j, ωgcx)
4      Cx(s) ← feedback (Gx(s)T2x(s), 1)
5      D← stepinfo(Cx(s))
6      trx ← D.RiseTime * 1000
7      mpx ← D.Overshoot
8      if 1 ⩽ mpx ⩽ 50 then
9          A← allmargin(Gx(s)T2x(S))
10         if A.Stable = 1 ∧ length(A.PhaseMargin) = 1 then
11             φmx ← A.PhaseMargin
12             if φmx ⩽ 90 then
13                 Nx(i,:) ← [trx, mpx, 90 − φmx, kx, ωlx, ωhx]
14                 i ← i + 1
15 function typePI(G(s), φm, ωgc)
16     [mag, phase] ← bode(G(s), ωgc)
17     k ← 1/mag
18     boost ← (φm − 90 − phase)
19     α ← tan ((0.5boost + 45)π/180)
20     ωl ← ωgc/α
21     ωh ← αωgc
22     return [T2(s), k, ωl, ωh]
```

If one observes the design of the Type-II PI controller, the controller parameters are obtained for a single target value of gain crossover frequency with the variation of the target phase margin. In this context, the objective functions based on the data can be visualized as in (4.30).

$$f_{x1}(\phi_{mx}) = t_{rx}, \forall\ x \in \{i, v\},\ \omega_{gcx} = \text{constant} \tag{4.30a}$$

$$f_{x2}(\phi_{mx}) = m_{px}, \forall\ x \in \{i, v\},\ \omega_{gcx} = \text{constant} \tag{4.30b}$$

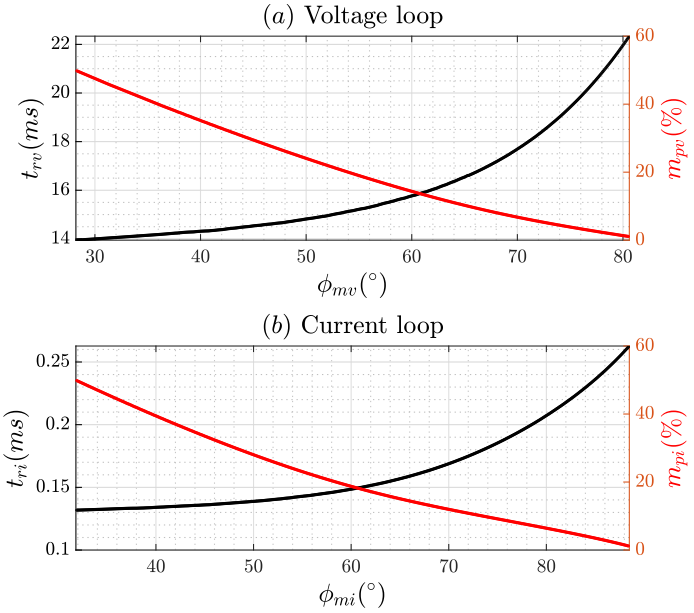

Figure 4.13: FOMs of TYPE-II PI controller

4.3.2 FOMs with PMR Controller

t_{rr} and m_{pr} are the rise time and percentage overshoot, respectively, of the unity feedback transfer function of $G_i(s)H_r(s)$. ϕ_{mr}, ω_{gcr}, and R_g are the phase margin, gain cross-over frequency, and resonant gain, respectively, of $G_i(s)H_r(s)$ at ω_1. The FOMs with PMR controller for the formulation of the convex optimization problem in obtaining $H_r(s)$ are detailed in Table 4.2. It can be observed that FOMs considered for convex optimization are non-negative and all have their goal as a problem of minimization type.

Table 4.2: FOMs with PMR controller

S.No.	FOM	Goal	Constraint
1	t_{rr}	Minimize	-
2	m_{pr}	Minimize	$1\% \leqslant m_{pr} \leqslant 50\%$
3	$90 - \phi_{mr}$	Minimize	$10^\circ \leqslant \phi_{mr} \leqslant 90^\circ$
4	$\omega_s - \omega_{gcr}$	Minimize	$\omega_{gcr} \geqslant 1.2 \times 9 \times \omega_1$ $\omega_{gcr} \leqslant 1.1 \times \omega_s/10$
5	$80 - R_g$	Minimize	$R_g \leqslant 80\text{dB}$

Algorithm 4 describes the computation of FOMs. The parameter range in (4.29) is considered as

$$\mathbf{k_i} = \{k_i \in \mathbb{N} \mid k_i \leqslant 1400\} \tag{4.31a}$$

$$\mathbf{k_p} = \{k_p \in \mathbb{R} \mid k_p = 0.01n, n \in \mathbb{N}, 1 \leqslant n \leqslant 200\} \tag{4.31b}$$

$$\boldsymbol{\omega_c} = \{\omega_c \in \mathbb{R} \mid \omega_c = 5 + 0.25n, n \in \mathbb{N}, 1 \leqslant n \leqslant 40\}. \tag{4.31c}$$

Algorithm 4: FOMs with PMR controller

```
   input  : G_i(s), ω_s, V
   output: N_r
   /* MATLAB function                                                  */
   /* MATLAB struct array field                                        */
 1 y ← length(V)
 2 N_r ← zeros(y, 8)
 3 ω_1 ← 2π60
 4 i ← 1
 5 for j ← 1 to y do
 6     k_i =V(j, 1)
 7     k_p =V(j, 2)
 8     ω_c =V(j, 3)
 9     H_1(s) ←PRC(ω_1, 1, ω_c, k_p, k_i)
10     H_3(s) ←PRC(ω_1, 3, ω_c, k_p, k_i)
11     H_5(s) ←PRC(ω_1, 5, ω_c, k_p, k_i)
12     H_7(s) ←PRC(ω_1, 7, ω_c, k_p, k_i)
13     H_9(s) ←PRC(ω_1, 9, ω_c, k_p, k_i)
14     H_r(s) ← H_1(s) + H_3(s) + H_5(s) + H_7(s) + H_9(s)
15     O_r(s) ← G_i(s)H_r(s)
16     C_r(s) ← feedback (O_r(s), 1)
17     D ← stepinfo(C_r(s))
18     t_rr ← D_r.RiseTime ∗ 1000
19     m_pr ← D_r.Overshoot
20     if 1 ⩽ m_pr ⩽ 50 then
21         A← allmargin(O_r(s))
22         if A.Stable = 1 ∧ length(A.PhaseMargin) = 1 then
23             φ_mr ← A.PhaseMargin
24             ω_gcr ← A.PMFrequency
25             [mag, ∼] ← bode(O_r(s), ω_1)
26             R_g ← 20 log_10(mag)
27             if (1.2 × 9 × ω_1 ⩽ ω_gcr ⩽ 1.1 × ω_s/10) ∧ (10° ⩽ φ_mr ⩽ 90)∧ (R_g ⩽ 80) then
28                 N_r(i, :) ← [t_rr, m_pr, 90 − φ_mr, ω_s − ω_gcr, 80 − R_g, k_i, k_p, ω_c]
29                 i ← i + 1
30 N_r(i : y, :) ← []
31 function PRC(ω_1, n, ω_c, k_p, k_i)
32     k_pz ← 1 + (k_i/k_p)
33     Q_p ← ω_1/(2 ∗ ω_c)
34     Q_z ← Q_p/k_pz
35     num ← [(1/(nω_1))^2, 1/(Q_z n^2 ω_1), 1]
36     den ← [(1/(nω_1))^2, 1/(Q_p n^2 ω_1), 1]
37     H(s) ← k_p tf(num, den)
38     return H(s)
```

The three-dimensional array i.e., the combination of all vectors corresponding to three parameters of (4.29) generated using `combvec` (arguments). `combvec` (arguments) is a MATLAB function available with Deep Learning Toolbox. The output of `combvec` (arguments) is transposed as per the convenience of programming style.

$$\mathbf{V} = \texttt{transpose}(\texttt{combvec}(\mathbf{k_i}, \mathbf{k_p}, \boldsymbol{\omega_c})) \tag{4.32}$$

The PMR controller for a n^{th} order of harmonic is evaluated using `PRC` (arguments), and then the FOMs for the convex optimization of the PMR controller is evaluated. Here, `allmargin` (arguments) usage is very pertinent and of non-trivial nature for this algorithm. All the computed data for each row vector of $\boldsymbol{\beta_r}$ is stored in a matrix $\mathbf{N_r}$, where each row is a vector containing the FOMs and associated PMR controller parameters. Fig. 4.14 shows three snapshots of computed data using Algorithm 4. Fig. 4.14(a)-(c), shows the variation of parameters in the FOMs with k_i, $k_p = 1$ and $\omega_c = 6$. Fig. 4.14(d)-(f), shows the variation of parameters in the FOMs with k_p, $k_i = 600$ and $\omega_c = 6$. Fig. 4.14(g)-(i), shows the variation of parameters in the FOMs with ω_c, $k_i = 300$ and $k_p = 1$.

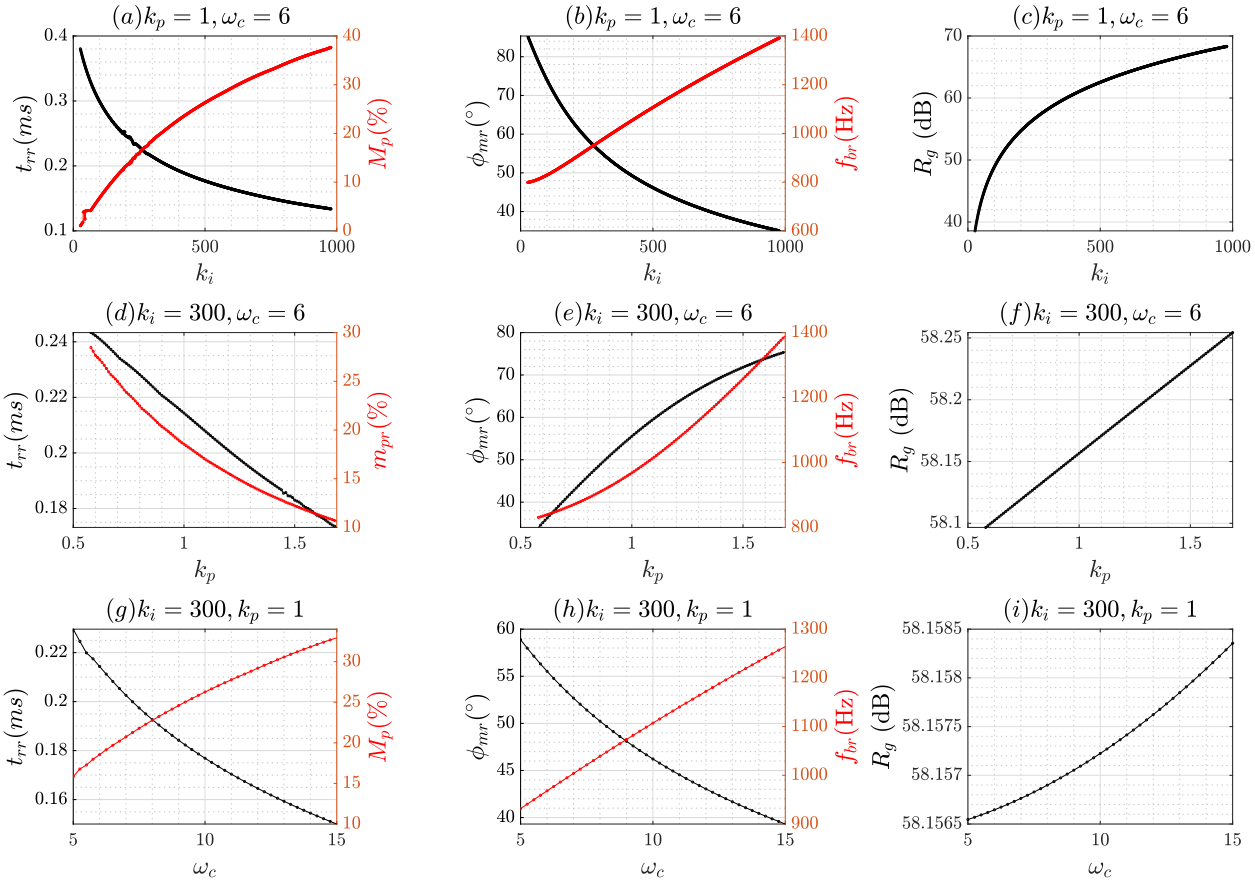

Figure 4.14: Snapshot of variation of parameters in the FOMs with the change of controller parameter values of the PMR controller

If one observes the design of the PMR controller, the controller parameters are varied to obtain FOMs. In this context, the objective functions based on Algorithm 4 can be written

as in (4.33).

$$g_1(\boldsymbol{\beta_r}) = t_{rr} \tag{4.33a}$$
$$g_2(\boldsymbol{\beta_r}) = m_{pr} \tag{4.33b}$$
$$g_3(\boldsymbol{\beta_r}) = 90 - \phi_{mr} \tag{4.33c}$$
$$g_4(\boldsymbol{\beta_r}) = \omega_s - \omega_{gcr} \tag{4.33d}$$
$$g_5(\boldsymbol{\beta_r}) = 80 - R_g \tag{4.33e}$$

4.4 Summary

This chapter has presented the methods required for calculating the FOMs involved in the design optimization considered in this part of the thesis. The proposed innovation uses MATLAB inbuilt functions, unit step response and bode plot to compute the cost functions. This *proposed computation method would be a cornerstone of the smart design of controllers, an enabler of the transition to i4.0.*

The LTI models for the DER inverter are derived. A PV array with rated peak power of 6011.25W is selected. The DC bus is designed for a voltage ripple of 8V. Insights are provided into the behaviour of the controller's transfer functions and cost functions involved in the optimization, which are essential to tackle the optimization problem. Specifically, the *conflicting nature of cost functions* is clearly shown for the Type-II PI controller and PMR controller, i.e., the problem is established.

Chapter 5

Optimization Algorithm and Results

> No one lights a lamp and puts it under a basket. Instead, everyone who lights a lamp puts it on a lamp stand. Then its light shines on everyone in the house.
>
> *Matthew (God's Word Translation): Chapter 5, Verse 14.*

5.1 Preliminaries

In this section, first, the concepts relevant to understanding and solving the problem of convex optimization from [95, 96] are introduced. Later, the problem formulation is completed step-by-step.

5.1.1 Definitions in Convex Optimization

5.1.1.1 Affine Set

A set $C \subseteq \mathbb{R}^n$ is affine [95] if the line through any two distinct points in C lies in C, i.e., if for any $x_1,\ x_2 \in C$ and $\lambda \in \mathbb{R}$, one has $\lambda x_1 + (1-\lambda)x_2 \in C$. In other words, C contains the linear combination of any two points in C, provided the coefficients in the linear combination sum to one. It can be noted that the affine set is unbounded. The affine dimension of a set C is the dimension of its affine hull i.e., if $C \subseteq \mathbb{R}^5$, the affine dimension is five.

5.1.1.2 Convex Set

A set $C \subseteq \mathbb{R}^n$ is convex [95] if the line segment between any two points in C lies in C, i.e.,

$$x_1,\ x_2 \in C,\ 0 \leqslant \lambda \leqslant 1 \implies \lambda x_1 + (1-\lambda)x_2 \in C \tag{5.1}$$

It can be observed that a convex set is bounded and a convex set is a special case of the affine set. The convex hull of a set C, denoted **conv** C, is the set of all convex combinations

of points in C given as

$$\textbf{conv } C = \left\{ \sum_{i=1}^{k} \lambda_i x_i \mid x_i \in C, \lambda_i \geqslant 0, \sum_{i=1}^{k} \lambda_i = 1 \right\} \tag{5.2}$$

5.1.1.3 Convex Function

A function $f : \mathbb{R}^n \rightarrow \mathbb{R}$ is convex [95] if domain of f is a convex set and if for all $x_1, x_2 \in$ domain of f, with $0 \leqslant \lambda \leqslant 1$, one has

$$f(\lambda x_1 + (1-\lambda)x_2) \leqslant \lambda f(x_1) + (1-\lambda) f(x_2). \tag{5.3}$$

Geometrically [95], (5.3) refers to a line segment between $(x_1, f(x_1))$ and $(x_2, f(x_2))$, which lies above the graph of f i.e., f is a convex function. The convex hull, **conv** C is always convex.

5.1.2 Concept of Scaling

In Multi-objective optimization problems, when two or more objectives are compared or blended to form a single objective function, then the scaling [44] of the data is a must to eliminate the effect of variation or range of values in one data set of one objective function with another. Typically, in data science, two methods are widely used for scaling. i.e., standardization and normalization.

For the data set $\mathbf{Y}$ i.e., the population which follows a normal distribution, the i^{th} element is transformed to a new space through the process of standardization as Y_{si} and is given by (5.4).

$$\mathbf{Y_{si}} = \frac{\mathbf{Y_i} - \mu}{\sigma} \tag{5.4}$$

Where σ is the population standard deviation and μ is the population mean.

For the data set $\mathbf{Y}$ i.e., population, the i^{th} element is transformed to a new space through the process of normalization as Y_{ni} and is given by (5.5). Equation (5.5) is a preferred choice [96] for the convex optimization problem because the transformed data set is always non-negative. The implementation of (5.5) is provided in Algorithm 5.

$$\mathbf{Y_{ni}} = \frac{\mathbf{Y_i} - \texttt{min}(\mathbf{Y})}{\texttt{max}(\mathbf{Y}) - \texttt{min}(\mathbf{Y})} \; ; \; Y_{ni} \in \mathbb{R}, 0 \leqslant Y_{ni} \leqslant 1 \tag{5.5}$$

The functional representation of FOMs in Table 4.1 and Table 4.2 are provided in (4.30) and (4.33), respectively. The functions in (4.30) and (4.33) are normalized with the Algorithm 5 and identified as (5.6) and (5.7), respectively.

$$f_{xn}(\phi_{mx}) \xrightarrow{normalized} \mathcal{F}_{xn}(\phi_{mx}) \; \forall \; x \in \{v, i\}, \; n \in \{1, 2\} \tag{5.6}$$

$$g_n(\boldsymbol{\beta_r}) \xrightarrow{normalized} \mathcal{G}_n(\boldsymbol{\beta_r}) \; \forall \; n \in \{1, 2, 3, 4, 5\} \tag{5.7}$$

Algorithm 5: Normalization

input : $\mathbf{F}, z$
output: $\mathbf{F_n}$
/* MATLAB function */
1 **function** `normalized`$(\mathbf{F}, z)$
2 **if** `numel`$(\mathbf{F}) > 0$ **then**
3 **for** $k \leftarrow 1$ **to** z **do**
4 $\mathbf{F_n}(:,k) \leftarrow \dfrac{\mathbf{F}(:,k) - \texttt{min}(\mathbf{F}(:,k))}{\texttt{max}(\mathbf{F}(:,k)) - \texttt{min}(\mathbf{F}(:,k))}$
5 **return** $\mathbf{F_n}$

5.2 Convex Hull of Multi-Objective Optimization

The convex hull for the multi-objective problem would need an appropriate choice of weight constraint. In this scenario, one can have two types of constraints [95, 96]: Linear Weight Constraint (LWC) and Non-Linear Weight Constraint (NLWC).

5.2.1 Type-II PI Controller for Voltage Loop

The Type-II PI controller (4.20) is employed to regulate the DC bus voltage of the system shown in Fig. 4.1. The two control architectures shown in Fig. 4.11 and Fig. 4.12 use the designed controller. In this context, for the design of (4.20), the convex hulls for the scenarios of LWC and NLWC, with the normalized objective functions described in (5.6) are given as (5.8a) and (5.9a), respectively.

$$\mathcal{C}_v(\phi_{mv}, \boldsymbol{\lambda_v}) = \left\{ \sum_{n=1}^{2} \lambda_{vn} \mathcal{F}_{vn}(\phi_{mv}) \;\middle|\; \mathcal{F}_{vn}(\phi_{mv}) \in C,\ \lambda_{vn} = 0.01k, k \in \mathbb{W}, k \leqslant 100, \sum_{n=1}^{2} \lambda_{vn} = 1 \right\} \tag{5.8a}$$

$$\boldsymbol{\lambda_v} = \begin{pmatrix} \lambda_{v1} & \lambda_{v2} \end{pmatrix} \tag{5.8b}$$

$$\mathcal{C}_v(\phi_{mv}, \boldsymbol{\sigma_v}) = \left\{ \sum_{n=1}^{2} \sigma_{vn} \mathcal{F}_{vn}(\phi_{mv}) \;\middle|\; \mathcal{F}_{vn}(\phi_{mv}) \in C, \sigma_{vn} = 0.01k, k \in \mathbb{W}, k \leqslant 100, \sum_{n=1}^{2} \sigma_{vn}^2 = 1 \right\} \tag{5.9a}$$

$$\boldsymbol{\sigma_v} = \begin{pmatrix} \sigma_{v1} & \sigma_{v2} \end{pmatrix} \tag{5.9b}$$

5.2.2 Type-II PI Controller for Current Loop

The Type-II PI controller (4.21) is employed to regulate the output alternating current of the system shown in Fig. 4.1. The control architecture shown in Fig. 4.11 uses the designed controller. In this context, for the design of (4.21), the convex hulls for the scenarios of LWC and NLWC with normalized objective functions described in (5.6), are given as (5.10a) and

(5.11a), respectively.

$$\mathcal{C}_i(\phi_{mi}, \boldsymbol{\lambda_i}) = \left\{ \sum_{n=1}^{2} \lambda_{in} \mathcal{F}_{in}(\phi_{mi}) \;\middle|\; \mathcal{F}_{in}(\phi_{mi}) \in C, \lambda_{in} = 0.01k, k \in \mathbb{W}, k \leqslant 100, \sum_{n=1}^{2} \lambda_{in} = 1 \right\} \tag{5.10a}$$

$$\boldsymbol{\lambda_i} = \begin{pmatrix} \lambda_{i1} & \lambda_{i2} \end{pmatrix} \tag{5.10b}$$

$$\mathcal{C}_i(\phi_{mi}, \boldsymbol{\sigma_i}) = \left\{ \sum_{n=1}^{2} \sigma_{in} \mathcal{F}_{in}(\phi_{mi}) \;\middle|\; \mathcal{F}_{in}(\phi_{mi}) \in C, \sigma_{in} = 0.01k, k \in \mathbb{W}, k \leqslant 100, \sum_{n=1}^{2} \sigma_{in}^2 = 1 \right\} \tag{5.11a}$$

$$\boldsymbol{\sigma_v} = \begin{pmatrix} \sigma_{v1} & \sigma_{v2} \end{pmatrix} \tag{5.11b}$$

5.2.3 PMR Controller for Current Loop

The PMR controller (4.27) is employed to regulate the output AC of the system shown in Fig. 4.1. The control architecture shown in Fig. 4.12 uses the designed controller. In this context of the design of (4.27), the convex hulls for the scenarios of LWC and NLWC with normalized objective functions described in (5.7) are given as (5.12a) and (5.13a), respectively.

$$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\lambda_r}) = \left\{ \sum_{n=1}^{5} \lambda_{rn} \mathcal{G}_n(\boldsymbol{\beta_r}) \;\middle|\; \mathcal{G}_n(\boldsymbol{\beta_r}) \in C, \lambda_{rn} = 0.02k, k \in \mathbb{W}, k \leqslant 50, \sum_{n=1}^{5} \lambda_{rn} = 1 \right\} \tag{5.12a}$$

$$\boldsymbol{\lambda_r} = \begin{pmatrix} \lambda_{r1} & \lambda_{r2} & \lambda_{r3} & \lambda_{r4} & \lambda_{r5} \end{pmatrix} \tag{5.12b}$$

$$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\sigma_r}) = \left\{ \sum_{n=1}^{5} \sigma_{rn} \mathcal{G}_n(\boldsymbol{\beta_r}) \;\middle|\; \mathcal{G}_n(\boldsymbol{\beta_r}) \in C, \sigma_{rn} = 0.02k, k \in \mathbb{W}, k \leqslant 50, \sum_{n=1}^{5} \sigma_{rn}^2 = 1 \right\} \tag{5.13a}$$

$$\boldsymbol{\sigma_r} = \begin{pmatrix} \sigma_{r1} & \sigma_{r2} & \sigma_{r3} & \sigma_{r4} & \sigma_{r5} \end{pmatrix} \tag{5.13b}$$

5.2.4 Min-Max Principle

All the six convex hulls defined in (5.8a), (5.9a), (5.10a), (5.11a), (5.12a), and (5.13a) would require the correct choice of weights defined in (5.8b), (5.9b), (5.10b), (5.11b), (5.12), and (5.13), respectively, to find the minimum of $\mathcal{C}_v(\phi_{mv}, \boldsymbol{\lambda_v})$, $\mathcal{C}_v(\phi_{mv}, \boldsymbol{\sigma_v})$, $\mathcal{C}_i(\phi_{mi}, \boldsymbol{\lambda_i})$, $\mathcal{C}_i(\phi_{mi}, \boldsymbol{\sigma_i})$, $\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\lambda_r})$, and $\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\sigma_r})$, respectively. If the weights chosen are too low or too high, then it causes an inadequate representation of one of the FOMs to the multi-objective function and the total objective function value could be too low [96]. One way to ensure that the total value will not be too low is to pick the maximum objective function value solution [96].

To do this [96]

- Vary the weights and find the *minimum* of the total objective function value for each combination of weights.
- Now, determine the *maximum* value from the minimum total objective function values obtained for each combination of weight.

This process of finding the maximum of the minimum is called the min-max principle [96].

5.2.5 Method of Lagrange's Multipliers

To find the maximum or minimum of a function $p(x, \lambda)$ subjected to the equality constraint $q(\lambda) = 0$

$$\mathcal{L}(x, \lambda, \xi) = p(x, \lambda) + \xi q(\lambda) \tag{5.14}$$

Where ξ is the Lagrange multiplier. Then the maximum or minimum of $p(x, \lambda)$ is located at the solution that is found by solving (5.15).

$$\nabla p = \xi \nabla q \tag{5.15a}$$
$$q(x) = 0 \tag{5.15b}$$

The generalized proof of the min-max principle using Lagrange multipliers for n objective functions with multiple variables for the cases of LWC and NLWC is provided in [96]. Here two sample problems are solved based on the proof provided in [96], and to shed some light on the salient differences between the two constraint methods, and the envisaged benefit(s) with LWC and/or NLWC.

5.2.6 Example with LWC

Consider the following example

$$p(x, \lambda) = \lambda_1 x_1 + \lambda_2 x_2 + \lambda_3 x_3 \tag{5.16}$$
$$q(\lambda) = \lambda_1 + \lambda_2 + \lambda_3 - 1 \tag{5.17}$$

then one has

$$\nabla p = \begin{pmatrix} \lambda_1 \dot{x_1} & \lambda_2 \dot{x_2} & \lambda_3 \dot{x_3} & x_1 & x_2 & x_3 \end{pmatrix}^\top \tag{5.18a}$$
$$\nabla q = \begin{pmatrix} 0 & 0 & 0 & 1 & 1 & 1 \end{pmatrix}^\top \tag{5.18b}$$

from (5.15) and (5.18)

$$x_1 = x_2 = x_3 = \xi \tag{5.19a}$$
$$\lambda_1 + \lambda_2 + \lambda_3 = 1 \tag{5.19b}$$
$$\lambda_1 \dot{x_1} = \lambda_2 \dot{x_2} = \lambda_3 \dot{x_3} = 0 \tag{5.19c}$$

As explained before, λ_1, λ_2 and λ_3 are selected based on min-max principle [96]. One can see that $p(x, \lambda)$, which is convex, at its minimum, will achieve same value for x_1, x_2 and x_3.

5.2.7 Example with NLWC

Consider the following example

$$p(x, \lambda) = \lambda_1 x_1 + \lambda_2 x_2 + \lambda_3 x_3 \tag{5.20}$$
$$q(\lambda) = \lambda_1^2 + \lambda_2^2 + \lambda_3^2 - 1 \tag{5.21}$$

then one has

$$\nabla p = \begin{pmatrix} \lambda_1 \dot{x_1} & \lambda_2 \dot{x_2} & \lambda_3 \dot{x_3} & x_1 & x_2 & x_3 \end{pmatrix}^\top \tag{5.22a}$$
$$\nabla q = \begin{pmatrix} 0 & 0 & 0 & 2\lambda_1 & 2\lambda_2 & 2\lambda_3 \end{pmatrix}^\top \tag{5.22b}$$

from (5.15) and (5.22)

$$\frac{x_1}{\lambda_1} = \frac{x_2}{\lambda_2} = \frac{x_3}{\lambda_3} = 2\xi \tag{5.23a}$$
$$\lambda_1^2 + \lambda_2^2 + \lambda_3^2 = 1 \tag{5.23b}$$
$$\lambda_1 \dot{x_1} = \lambda_2 \dot{x_2} = \lambda_3 \dot{x_3} = 0 \tag{5.23c}$$

As explained before, λ_1, λ_2 and λ_3 are selected based on min-max principle [96]. One can see that $p(x, \lambda)$, which is convex, at its minimum, will achieve same value for x_1/λ_1, x_2/λ_2 and x_3/λ_3. Thus a x_i with the greatest value will have the largest weight λ_i so that its contribution to the total cost function is further increased [96].

5.3 Multi-Objective Convex Optimization

Among the six convex hulls considered in this part of the thesis, four are for the Type-II PI Controller and two are for the PMR Controller. In this context, two algorithms based on the min-max principle are presented here for the Type-II PI controller and the PMR controller.

5.3.1 Type-II PI Controller

As seen in Algorithm 6, the input $\mathbf{N_x}$, which is the output of the Algorithm 3, where each row has information on FOMs for a specific value of the phase margin of the loop being designed along with the controller parameters. Here, x specifies whether it is the voltage loop or the current loop for which the controller is being designed.

First, the functions are normalized using the `normalized` (arguments). Here the second argument specifies up to what number of columns in $\mathbf{N_x}$ one wants to normalize. Algorithm 6 is used to obtain four solutions as shown in Table 5.1. S.No#1 and S.No#2 of Table 5.1 corresponds to the design of Type-II PI controller for $T_{2v}(s)$, to regulate the v_{dc}, as shown in Fig. 4.11 and Fig. 4.12. Here the output of Algorithm 3, $\mathbf{N_v}$ is given as an input to

Algorithm 6. Then, in Algorithm 6, lines #2 to #8 computes the solution $\mathbf{S_{v1}}$ i.e., using LWC method and lines #9 to #15 computes the solution $\mathbf{S_{v2}}$ i.e., using NLWC method.

S.No#3 and S.No#4 of Table 5.1 corresponds to the design of Type-II PI Controller for $T_{2i}(s)$, to regulate the $i(t)$, as shown in Fig. 4.11. Here the output of Algorithm 3, $\mathbf{N_i}$ is given as an input to Algorithm 6. Then, in Algorithm 6, lines #2 to #8 computes the solution $\mathbf{S_{i1}}$ i.e., using linear weight constraint method and lines #9 to #15 computes the solution $\mathbf{S_{i2}}$ i.e., using non-linear weight constraint method.

Algorithm 6: Two-Objective Convex Optimization

input : $\mathbf{N_x}$
output: $\mathbf{S_{x1}}, \mathbf{S_{x2}}, \mathbf{a_1}, \mathbf{b_1}, \mathbf{a_2}, \mathbf{b_2}$
/* MATLAB function */
1 $\mathbf{F_n} \leftarrow$ `normalized`$(\mathbf{N_x}, 2)$
2 i $\leftarrow 1$
3 **for** $\lambda \leftarrow 0$ **to** 1 **by** 0.01 **do**
4 $\quad$ e $\leftarrow \lambda \mathbf{F_n}(:,1) + (1-\lambda)\mathbf{F_n}(:,2)$
5 $\quad$ $[\mathbf{E_1}(\mathsf{i}), \mathbf{I_d}(\mathsf{i})] \leftarrow$ `min`(e)
6 $\quad$ i $\leftarrow$ i + 1
7 $[\mathbf{a_1}, \mathbf{b_1}] \leftarrow$ `max`$(\mathbf{E_1})$
8 $\mathbf{S_{x1}} \leftarrow \mathbf{F_n}(\mathbf{I_d}(\mathsf{b}), :)$
9 i $\leftarrow 1$
10 **for** $\lambda \leftarrow 0$ **to** 1 **by** 0.01 **do**
11 $\quad$ e $\leftarrow \lambda \mathbf{F_n}(:,1) +$ `sqrt`$((1-\lambda^2))\mathbf{F_n}(:,2)$
12 $\quad$ $[\mathbf{E_2}(\mathsf{i}), \mathbf{I_d}(\mathsf{i})] \leftarrow$ `min`(e)
13 $\quad$ i $\leftarrow$ i + 1
14 $[\mathbf{a_2}, \mathbf{b_2}] \leftarrow$ `max`$(\mathbf{E_2})$
15 $\mathbf{S_{x2}} \leftarrow \mathbf{F_n}(\mathbf{I_d}(\mathsf{b}), :)$

5.3.2 PMR Controller

As seen in Algorithm 7, the input $\mathbf{N_r}$, which is the output of the Algorithm 4, is a matrix. Where each row has information on FOMs for a specific value of k_i, k_p and ω_c of the PMR controller. Firstly, the functions are normalized using the `normalized` (arguments). Lines from #4 to #6 show the initialization of matrices with zeros to reduce computation overhead due to memory allocation. The lines from #6 to #12 of the algorithm can provide the solution for both LWC and NLWC methods. The objective function weights, which is a matrix, an input to the algorithm determines the weight constraint method employed. The matrices $\boldsymbol{\kappa_r}$ and $\boldsymbol{\gamma_r}$ are obtained from (5.24) and (5.25), respectively. The weight matrices $\boldsymbol{\kappa_r}$ and $\boldsymbol{\gamma_r}$ provide the solutions for LWC and NLWC methods, respectively.

S.No#5 and S.No#6 of Table 5.1 corresponds to the design of PMR Controller for $H_r(s)$, to regulate the $i(t)$, as shown in Fig. 4.12. Here the output of Algorithm 4, $\mathbf{N_r}$ is given as an input to Algorithm 7. In this situation, when Algorithm 7 is supplied with the weight

matrices $\boldsymbol{\gamma_r}$ and $\boldsymbol{\sigma_r}$ it provides outputs $\mathbf{R_0}$ and $\mathbf{K_0}$, respectively.

$$\boldsymbol{\kappa_r} = \left\{ \boldsymbol{\lambda_r} \;\middle|\; \lambda_{rn} = 0.02k, k \in \mathbb{W}, k \leqslant 50, \sum_{n=1}^{5} \lambda_{rn} = 1 \right\} \tag{5.24a}$$

$$\boldsymbol{\lambda_r} = \begin{pmatrix} \lambda_{r1} & \lambda_{r2} & \lambda_{r3} & \lambda_{r4} & \lambda_{r5} \end{pmatrix} \tag{5.24b}$$

$$\boldsymbol{\gamma_r} = \left\{ \boldsymbol{\sigma_r} \;\middle|\; \lambda_{rn} = 0.02k, k \in \mathbb{W}, k \leqslant 50, \sum_{n=1}^{5} \sigma_{rn} = 1 \right\} \tag{5.25a}$$

$$\boldsymbol{\sigma_r} = \begin{pmatrix} \sigma_{r1} & \sigma_{r2} & \sigma_{r3} & \sigma_{r4} & \sigma_{r5} \end{pmatrix} \tag{5.25b}$$

Table 5.1: Description on solutions from Algorithm 6 and Algorithm 7

S.No.	reference	Convex hull	Algorithm's choice	input	method	output
1	Fig. 4.11, Fig. 4.12	$\mathcal{C}_v(\phi_{mv}, \boldsymbol{\lambda_v})$	Algorithm 6	$\mathbf{N_v}$	LWC	$\mathbf{S_{v1}}$
2	Fig. 4.11, Fig. 4.12	$\mathcal{C}_v(\phi_{mv}, \boldsymbol{\sigma_v})$	Algorithm 6	$\mathbf{N_v}$	NLWC	$\mathbf{S_{v2}}$
3	Fig. 4.11	$\mathcal{C}_v(\phi_{mi}, \boldsymbol{\lambda_v})$	Algorithm 6	$\mathbf{N_i}$	LWC	$\mathbf{S_{i1}}$
4	Fig. 4.11	$\mathcal{C}_v(\phi_{mi}, \boldsymbol{\sigma_v})$	Algorithm 6	$\mathbf{N_i}$	NLWC	$\mathbf{S_{i2}}$
5	Fig. 4.12	$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\lambda_r})$	Algorithm 7	$\mathbf{N_r}, \boldsymbol{\kappa_r}$	LWC	$\mathbf{R_0}$
6	Fig. 4.12	$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\sigma_r})$	Algorithm 7	$\mathbf{N_r}, \boldsymbol{\gamma_r}$	NLWC	$\mathbf{K_0}$

Algorithm 7: Five-Objective Convex Optimization

input : $\mathbf{N_r}, \lambda$
output: $\mathbf{S}$
/* MATLAB function */
function WC($\mathbf{N_r}, \boldsymbol{\lambda}$)
    $\mathbf{F_n} \leftarrow$ normalized($\mathbf{N_r}, 5$)
    y $\leftarrow$ length($\boldsymbol{\lambda}$)
    $\mathbf{E_1} \leftarrow$ zeros(y, 1)
    $\mathbf{I_d} \leftarrow$ zeros(y, 1)
    for i $\leftarrow$ 1 **to** y **do**
        $\mathbf{E_t} \leftarrow \boldsymbol{\lambda}(\mathsf{i},1)\mathbf{F_n}(:,1) + \boldsymbol{\lambda}(\mathsf{i},2)\mathbf{F_n}(:,2)$
        $+\boldsymbol{\lambda}(\mathsf{i},3)\mathbf{F_n}(:,3) + \boldsymbol{\lambda}(\mathsf{i},4)\mathbf{F_n}(:,4) + \boldsymbol{\lambda}(\mathsf{i},5)\mathbf{F_n}(:,5)$
        $[\mathbf{E_1}(\mathsf{i}), \mathbf{I_d}(\mathsf{i})] \leftarrow \min(\mathbf{E_t})$
    $[\sim, \mathsf{b}] \leftarrow \max(\mathbf{E_1})$
    $\mathbf{S} \leftarrow \mathbf{N_r}(\mathbf{I_d}(\mathsf{b}), :)$
return S

5.4 Multi-Objective Hierarchical Convex Optimization

Among all the multi-objective optimization problems shown in Table 5.1, #1 to #4 involve single-variable objective functions, whereas #5 and #6 involve multi-variable objective functions. Thus the concept of the hierarchical approach [44] applies to the convex hulls described in #5 and #6. Both #5 and #6 involve objective functions determined by three variables, defined in $\boldsymbol{\beta_r}$. When the number of variables is three, the number of all possible paths one can have is $3 \times 2 \times 1 = 6$. Table 5.2 shows all the possible six paths for the two types of weight constraint methods chosen: LWC and NLWC. Let the three variables be x, y and z, then in

- Level-3: for each x and y, vary the value of z and select the best value of z.
- Level-2: for each x, vary the value of y and select the best value of y, where the value of z is the best value selected from Level-3.
- Level-1: vary the value of x and select the best value of x, where the value of y and z are the best value selected from Level-2 and Level-3, respectively.

Table 5.2 shows the choice of the variable for optimization in each level. The output of the Algorithm 8 is a single row matrix, where this single row is one of the rows of the $\mathbf{N_r}$ obtained from Algorithm 4. The Algorithm 8's output from LWC and NLWC methods is stored as $\mathbf{R_n}$ and $\mathbf{K_n}$, respectively, where $n = \{1, 2..6\}$ correspond to the path number.

5.5 Optimization Results

5.5.1 Type-II PI Controller

As explained in Algorithm 6, and shown in Table 5.1, the solutions obtained for the design of Type-II PI controller for the regulation of DC bus voltage and the output AC are detailed in Table 5.3 and Table 5.4, respectively.

The bode plot of the plant and its open loop transfer function with the Type-II PI Controller for the obtained solutions can be seen in Fig. 5.5 and Fig. 5.6 for the voltage loop design and current loop design, respectively. Similarly, the unit step response of the unity feedback system obtained with the plant and Type-II controller can be seen in Fig. 5.3 and Fig. 5.4, concerning the voltage loop design and current loop design, respectively.

LWC and NLWC methods in Algorithm 6 evaluate the minimum of the multi-objective function for each value of the λ. The minimum obtained for each value of λ is stored as $\mathbf{E_1}$ and $\mathbf{E_2}$ for LWC and NLWC methods, respectively. The plot of $\mathbf{E_1}$ and $\mathbf{E_2}$ can be seen in Fig. 5.1 concerning voltage loop design and Fig. 5.2 concerning the current loop design.

For the voltage loop design, as can be seen in Fig. 5.1, the maximum of minimums is obtained at $\lambda = 0.39$ and $\lambda = 0.62$ for LWC and NLWC methods, respectively. The values of multi-objective functions $\mathbf{E_1}$ and $\mathbf{E_2}$ at the maximum point are 0.24483 and 0.34197, respectively. For the current loop design, as can be seen in Fig. 5.2, the maximum of minimums is obtained at $\lambda = 0.49$ and $\lambda = 0.7$ for LWC and NLWC methods, respectively. The values of multi-objective functions $\mathbf{E_1}$ and $\mathbf{E_2}$ at the maximum point are 0.24272 and 0.34317, respectively.

Table 5.2: Description on different paths and their solutions from Algorithm 8 (**C**: constant, **V**: variable, **O**: *optimized*)

S.No.	Path	LEVEL-3			LEVEL-2			LEVEL-1			convex hull	Algorithm's input	Algorithm's method	Algorithm's output
		C	**V**	**O**	**C**	**V**	**O**	**C**	**V**	**O**				
1	Path#1	k_i, k_p	ω_c	-	k_i	k_p	ω_c	-	k_i	k_p, ω_c				$\mathbf{R_1}$
2	Path#2	k_i, ω_c	k_p	-	k_i	ω_c	k_p	-	k_i	ω_c, k_p				$\mathbf{R_2}$
3	Path#3	k_p, k_i	ω_c	-	k_p	k_i	ω_c	-	k_p	k_i, ω_c	$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\lambda_r})$	$\mathbf{N_r}, \boldsymbol{\kappa_r}$	LWC	$\mathbf{R_3}$
4	Path#4	k_p, ω_c	k_i	-	k_p	ω_c	k_i	-	k_p	ω_c, k_i				$\mathbf{R_4}$
5	Path#5	ω_c, k_i	k_p	-	ω_c	k_i	k_p	-	ω_c	k_i, k_p				$\mathbf{R_5}$
6	Path#6	ω_c, k_p	k_i	-	ω_c	k_p	k_i	-	ω_c	k_p, k_i				$\mathbf{R_6}$
7	Path#1	k_i, k_p	ω_c	-	k_i	k_p	ω_c	-	k_i	k_p, ω_c				$\mathbf{K_1}$
8	Path#2	k_i, ω_c	k_p	-	k_i	ω_c	k_p	-	k_i	ω_c, k_p				$\mathbf{K_2}$
9	Path#3	k_p, k_i	ω_c	-	k_p	k_i	ω_c	-	k_p	k_i, ω_c	$\mathcal{C}_r(\boldsymbol{\beta_r}, \boldsymbol{\sigma_r})$	$\mathbf{N_r}, \boldsymbol{\gamma_r}$	NLWC	$\mathbf{K_3}$
10	Path#4	k_p, ω_c	k_i	-	k_p	ω_c	k_i	-	k_p	ω_c, k_i				$\mathbf{K_4}$
11	Path#5	ω_c, k_i	k_p	-	ω_c	k_i	k_p	-	ω_c	k_i, k_p				$\mathbf{K_5}$
12	Path#6	ω_c, k_p	k_i	-	ω_c	k_p	k_i	-	ω_c	k_p, k_i				$\mathbf{K_6}$

Algorithm 8: Multi-Objective Hierarchical Convex Optimization

```
   input  : N_r, λ, P
   output: L
   /* MATLAB function                                                    */
 1 P ← [6,7;6,8;7,6;7,8;8,6;8,7]
 2 L_1 ← zeros(6,1)
 3 for a ← 1 to 6 do
 4     c_1 ← P(a,1)
 5     c_2 ← P(a,2)
 6     U_1 ← unique(N_r(:,c_1))
 7     U_2 ← unique(N_r(:,c_2))
 8     y_1 ← numel(U_1)
 9     y_2 ← numel(U_2)
       /* LEVEL-1                                                        */
10     n ← 1
11     L_1 ← zeros(y_1,8)
12     for i ← 1 to y_1 do
           /* LEVEL-2                                                    */
13         m ← 1
14         L_2 ← zeros(y_2,8)
15         for j ← 1 to y_2 do
               /* LEVEL-3                                                */
16             Q ← (N_r(:,c_1) = U_1(i))∧
17                  (N_r(:,c_2) = U_2(j))
18             L_3 ← N_r(Q,:)
19             if ~ isempty(L_3) then
20                 L_2(m,:) ← WC(L_3,λ)
21                 m ← m + 1
22         L_2(m : y_2,:) ← []
23         if ~ isempty(L_2) then
24             L_1(n,:) ← WC(L_2,λ)
25             n ← n + 1
26     L_1(n : y_1,:) ← []
27     if ~ isempty(L_1) then
28         L(a,:) ← WC(L_1,λ)
```

5.5.1.1 Voltage Loop: Benefits of Design Optimization for Type-II PI Controller

The best solutions for the Type-II PI controller to regulate the DC bus voltage are detailed in Table 5.3. It can be observed that both LWC and NLWC methods point to the same solution. To evaluate the benefits of design optimization, two base cases are selected as shown in Table 5.5. Where % improvement#1 and % improvement#2 refer to the improvement against base case#1 and base case#2, respectively, with the best solution obtained using

Table 5.3: Best solutions of Type-II PI controller for the voltage loop

item	$\mathbf{S_{v1}}$	$\mathbf{S_{v2}}$	unit
method	LWC	NLWC	-
k_{2v}	0.93417	0.93417	-
ω_{lv}	27.518	27.518	rad/sec
ω_{hv}	229.94	229.94	rad/sec
ω_{gcv}	79.54	79.54	rad/sec
t_{rv}	15.94	15.94	ms
m_{pv}	13.16	13.16	%
ϕ_{mv}	61.4	61.4	degree

Table 5.4: Best solutions of Type-II PI controller for the current loop

item	$\mathbf{S_{i1}}$	$\mathbf{S_{i2}}$	unit
method	LWC	NLWC	-
k_{2i}	7.9545	7.9545	-
ω_{li}	1529.8	1688.8	rad/sec
ω_{hi}	41362	37468	rad/sec
ω_{gci}	7954.51	7954.51	rad/sec
t_{ri}	0.1643	0.15914	ms
m_{pi}	12.981	14.358	%
ϕ_{mi}	68.3	66.1	degree

LWC or NLWC method.

In improvement#1, one can notice that an improvement of 2.33% in the phase margin of the system with respect to the base case#1 is accompanied by an 8.388% decrease in the percentage of overshoot at the expense of 1.09% increase in the rise time. In improvement#2, one can notice that an improvement of 33.33% in the phase margin of the system with respect to the base case#2 is accompanied by a 55.34% decrease in the percentage of overshoot at the expense of 9.67% increase in the rise time.

5.5.1.2 Current Loop: Benefits of Design Optimization for Type-II PI Controller

The best solutions of the Type-II PI controller to regulate the output AC are detailed in Table 5.4. It can be observed that both LWC and NLWC methods point to different solutions. Now to evaluate the benefits of design optimization, two base cases are selected as shown in Table 5.6 and Table 5.7. Where % improvement#31 and % improvement#41 refer to

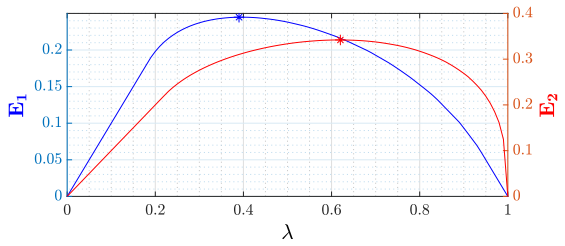

Figure 5.1: Voltage loop: plot of $\mathbf{E_1}$ and $\mathbf{E_2}$ from Algorithm 6

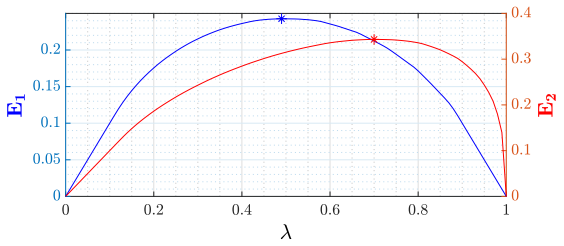

Figure 5.2: Current loop : plot of $\mathbf{E_1}$ and $\mathbf{E_2}$ from Algorithm 6

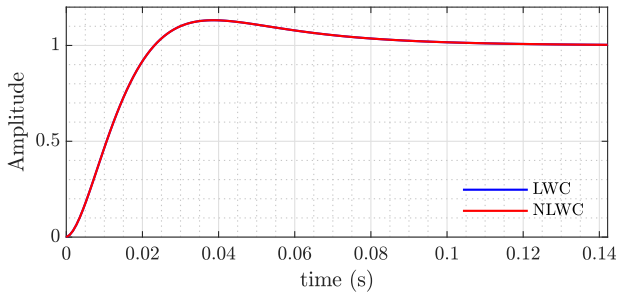

Figure 5.3: Voltage loop: unit step responses of the unity feedback systems

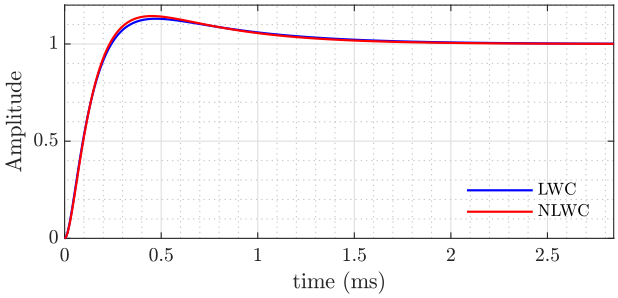

Figure 5.4: Current loop: unit step responses of the unity feedback systems

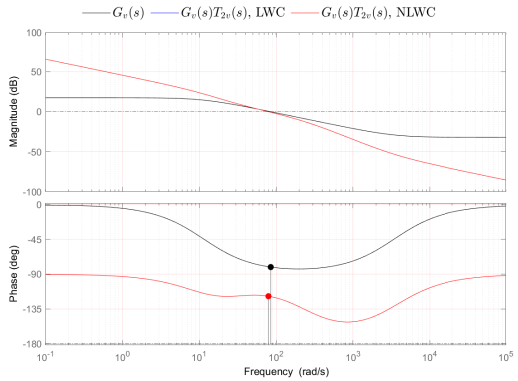

Figure 5.5: Bode plots of voltage loop

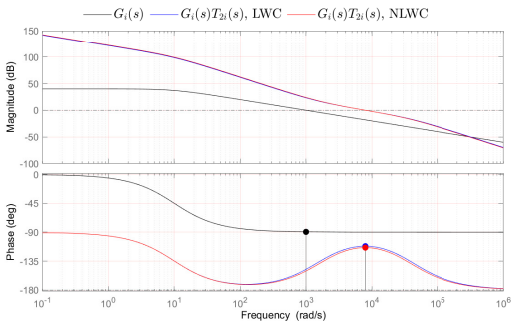

Figure 5.6: Bode plots of current loop

the improvement against base case#3 and base case#4, respectively, with the best solution obtained using the LWC method. Similarly, % improvement#32 and % improvement#42 refer to the improvement against base case#3 and base case#4, respectively, with the best solution obtained using the NLWC method.

In improvement#31, one can notice that an improvement of 13.83% in the phase margin of the system with respect to the base case#3 is accompanied by a 30.71% decrease in the percentage of overshoot at the expense of 10.62% increase in the rise time. In improvement#41, one can notice that an improvement of 51.77% in the phase margin of the system with respect to the base case#4 is accompanied by a 61.25% decrease in the percentage of overshoot at the expense of 20.79% increase in the rise time.

Table 5.5: The benefit of the best solutions for Type-II PI controller for the voltage loop against the design without optimization

item	base case#1	base case#2	unit	% improvement#1	% improvement#2
method	-	-	-	-	-
k_{2v}	0.93417	0.93417	-	-	-
ω_{lv}	28.611	41.026	rad/sec	-	-
ω_{hv}	221.15	154.23	rad/sec	-	-
ω_{gcv}	79.54	79.54	rad/sec	-	-
t_{rv}	15.768	14.534	ms	$\uparrow$ 1.09	$\uparrow$ 9.67
m_{pv}	14.365	29.469	%	$\downarrow$ 8.388	$\downarrow$ 55.34
ϕ_{mv}	60	45	degree	$\uparrow$ 2.33	$\uparrow$ 33.33

Table 5.6: The benefit of the LWC method best solution for Type-II PI controller for the current loop against the design without optimization

item	base case#3	base case#4	unit	%improvement#31	%improvement#41
method	-	-	-	-	-
k_{2i}	7.9545	7.9545	-	-	-
ω_{li}	2136.8	3300.7	rad/sec	-	-
ω_{hi}	29612	19170	rad/sec	-	-
ω_{gci}	7954.51	7954.51	rad/sec	-	-
t_{ri}	0.14852	0.13602	ms	$\uparrow$ 10.62	$\uparrow$ 20.79
m_{pi}	18.735	33.503	%	$\downarrow$ 30.71	$\downarrow$ 61.25
ϕ_{mi}	60	45	degree	$\uparrow$ 13.83	$\uparrow$ 51.77

In improvement#32, one can notice that an improvement of 10.16% in the phase margin of the system with respect to the base case#3 is accompanied by a 23.36% decrease in the percentage of overshoot at the expense of 7.15% increase in the rise time. In improvement#42, one can notice that an improvement of 46.88% in the phase margin of the system with respect to the base case#4 is accompanied by a 57.144% decrease in the percentage of overshoot at the expense of 16.99% increase in the rise time.

5.5.1.3 Observation

From the perspective of the principle of equity, it can be observed that when the NLWC method is employed in the design optimization, the %improvement in all three cost functions is better (fairer) in comparison to when the LWC method is employed. This can be verified by seeing that % improvements in Table 5.7 are better than Table 5.6. Specifically, the

%improvements with the NLWC method provide an improved phase margin and decreased percentage overshoot at a lesser expense of an increase in the rise time, compared to the LWC method.

Table 5.7: The benefit of the NLWC method best solution for Type-II PI controller for the current loop against the design without optimization

item	base case#3	base case#4	unit	%improvement#32	%improvement#42
method	-	-	-	-	-
k_{2i}	7.9545	7.9545	-	-	-
ω_{il}	2136.8	3300.7	rad/sec	-	-
ω_{hi}	29612	19170	rad/sec	-	-
ω_{gci}	7954.51	7954.51	rad/sec	-	-
t_{ri}	0.14852	0.13602	ms	$\uparrow$ 7.15	$\uparrow$ 16.99
m_{pi}	18.735	33.503	%	$\downarrow$ 23.36	$\downarrow$ 57.144
ϕ_{mi}	60	45	degree	$\uparrow$ 10.16	$\uparrow$ 46.88

‘

5.5.2 PMR Controller

A total of 14 convex optimization problems are considered for the design of the PMR controller. Of the 14, two do not involve the concept of hierarchical optimization, and the obtained solutions are saved as $\mathbf{R}_0$ and $\mathbf{K}_0$ for the LWC and NLWC methods, respectively. It is to be noted that the subscript 0 denotes no hierarchy in the optimization.

The six convex optimization problems that concern six different paths of hierarchical optimization with the LWC method are stored as $\mathbf{R}_n$, where n specifies the Path number. Similarly, with the NLWC method, the obtained solutions are stored as $\mathbf{K_n}$. The parameters of FOMs detailed in the Table 4.2 and PMR controller (4.27) parameters for the obtained solutions $\mathbf{R}_n$ and $\mathbf{K}_n$, where $n \in \{0, 1, 2..6\}$ is shown in Fig. 5.7. The generalized findings and critical findings from Fig. 5.7 are as follows.

5.5.2.1 Generalized Findings

- LWC method can leverage the effect of hierarchical framework to extremize one or more FOMs. Whereas the NLWC method maintains the FOMs in a tight band irrespective of the Path of optimization.
- While extremizing any FOM with the LWC method, other FOMs could potentially suffer. In this case, the constraints on FOMs could be suitably chosen to find the best solution.
- The underlying philosophy of LWC and NLWC methods such as the principle of equality and the principle of equity, respectively, can be observed.

5.5.2.2 Objective Findings

- In the optimization problem, the current loop bandwidth is set to a maximum value = 12660 × 0.1 × 1.1 = 1392.6Hz. It can be seen that with the NLWC method, solutions that are obtained in all Paths, and the one obtained without hierarchy, naturally attain a value very close to the maximum available bandwidth. Thus current loop bandwidth need not be selected as a FOM in the optimization, reducing the number of FOMs from five to four. However in the optimization problem, a constant on the current loop bandwidth should be used.

- In Path#4, with the LWC method, the phase margin is extremized at the cost of resonant gain.

- In Path#3, with the LWC method, the resonant gain is extremized at the cost of phase margin.

- Path#6 with the LWC method offers inferior optimization results.

- Maximum value of resonant gain and smallest rise time without much sacrificing of other FOMs is obtained in Path#3 with the NLWC method.

- Maximum value of phase margin and smallest percentage overshoot, without much sacrificing of other FOMs is obtained in Path#0 (i.e., no hierarchy) with NLWC method.

To summarize, *the hierarchical framework also has a role to play in leveraging the effect of a design variable in the optimization of the final result.*

The controller parameters of the PMR controller transfer function, as seen in (4.27), are obtained along with the solutions $\mathbf{R}_n$ and $\mathbf{K}_n$, and the corresponding controller transfer functions are defined as $H_{rRn}(s)$ and $H_{rKn}(s)$, respectively. The bode plot of the PMR controllers for the obtained solutions can be seen in Fig. 5.8 and Fig. 5.9 for the methods LWC and NLWC, respectively.

The bode plot of open loop transfer functions $G_i(s)H_{rRn}(s)$ and $G_i(s)H_{rKn}(s)$ along with the plant transfer function, can be seen in Fig. 5.10 and Fig. 5.11 for the methods LWC and NLWC, respectively.

The unity feedback system's transfer functions of the plant with the different PMR controllers obtained via the LWC method are defined as

$$T_{rRn}(s) = \frac{G_i(s)H_{rRn}(s)}{1 + G_i(s)H_{rRn}(s)} \ \forall \ n \ \in \ 0, 1, 2..6. \tag{5.26}$$

The unity feedback system's transfer functions of the plant with the different PMR controllers obtained via the NLWC method are defined as

$$T_{rKn}(s) = \frac{G_i(s)H_{rKn}(s)}{1 + G_i(s)H_{rKn}(s)} \ \forall \ n \ \in \ 0, 1, 2..6. \tag{5.27}$$

The unit step response of transfer functions defined in (5.26) and (5.27) can be seen in Fig. 5.12 and Fig. 5.13 concerning the methods LWC and NLWC, respectively.

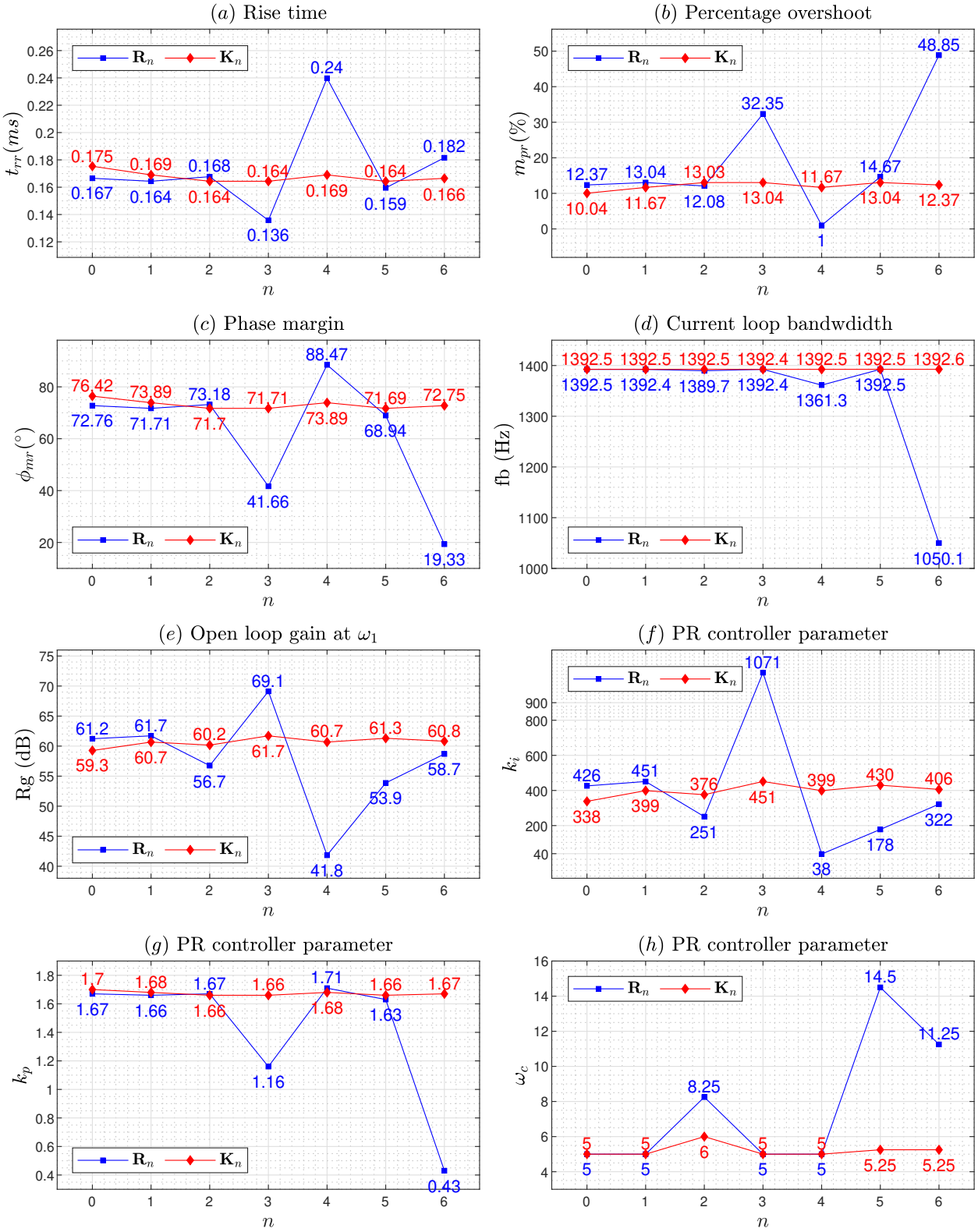

Figure 5.7: The parameters of FOMs and PMR controller parameters for the obtained solutions $\mathbf{R}_n$ and $\mathbf{K}_n$, where $n \in \{0, 1, 2..6\}$

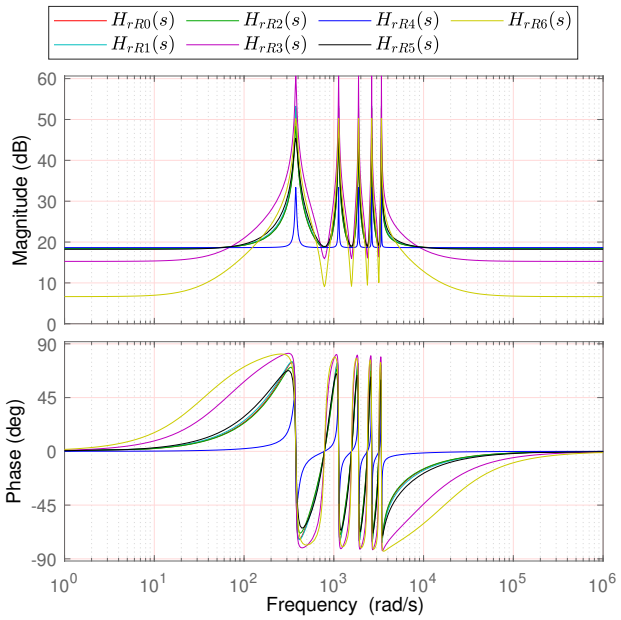

Figure 5.8: LWC: bode plots of PMR controllers

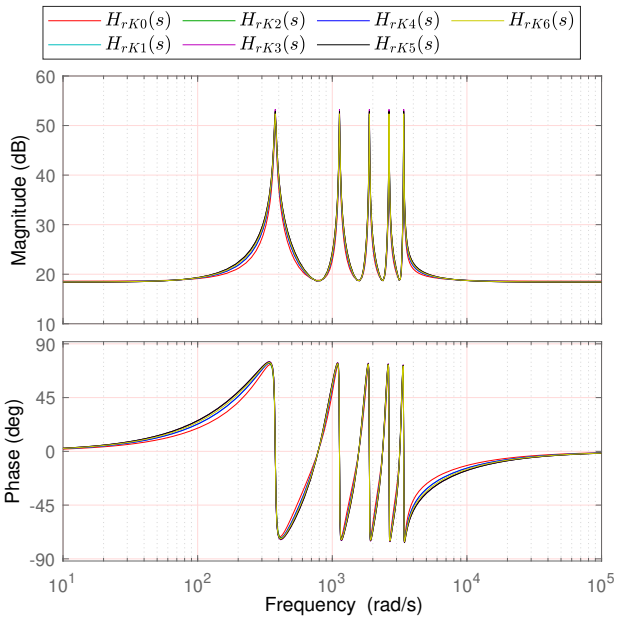

Figure 5.9: NLWC: bode plots of PMR controllers

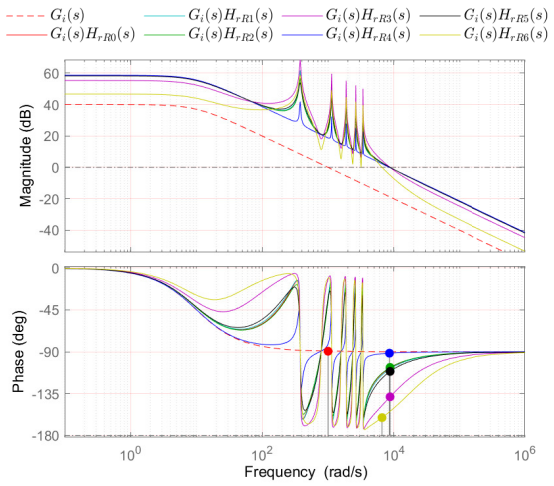

Figure 5.10: LWC: bode plots of plant and its open loop transfer function with PMR controllers

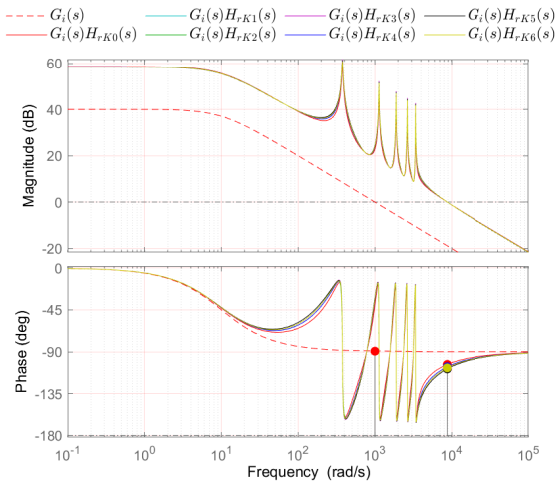

Figure 5.11: NLWC: bode plots of plant and its open loop transfer function with PMR controllers

5.6 A Perspective on Computation Time

5.6.1 Dimensions

The variables involved in this multi-objective function optimization of the PMR controller are defined in (4.31a), (4.31b) and (4.31c). The best solutions of the PMR controller that

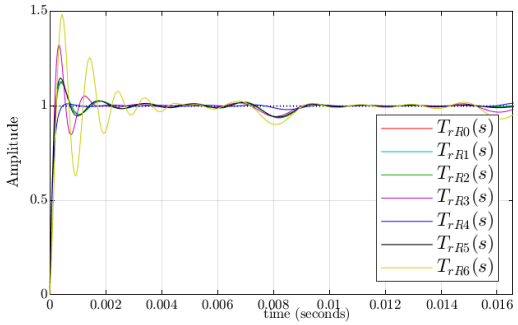

Figure 5.12: LWC: unit step responses of the unity feedback systems

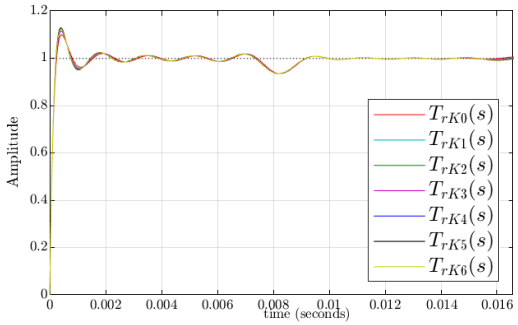

Figure 5.13: NLWC: unit step responses of the unity feedback systems

are listed in Table 5.1 and Table 5.2 are obtained using Algorithm 7 and Algorithm 8, respectively. Here (5.24), (5.25) are the multi-objective function weight combinations obtained using LWC and NLWC methods, respectively. The 14 convex optimization problems chosen for the design of the PMR controller involve picking one solution from 2571509 solutions i.e., approximately, selecting one out of 2.6M solutions, as can be understood from Table 5.8.

Table 5.8: Dimensions in the FOMs of PMR controller design

item	value	reference
$\texttt{length}(\mathbf{k_i})$	1400	(4.31a)
$\texttt{length}(\mathbf{k_p})$	200	(4.31b)
$\texttt{length}(\boldsymbol{\omega_c})$	41	(4.31c)
$\texttt{length}(\mathbf{V})$	$1400 \times 200 \times 41 = 11.48\text{M}$	(4.32)
$\texttt{length}(\mathbf{N_r})$	2571509	Algorithm 4
% of solutions	22.4%	2571509/11.48M

$\mathbf{N_r}$ is a matrix containing solutions that satisfied the constraints on FOMs with each row containing one solution. In this, the number of unique values for each controller parameter is provided in Table 5.9.

Table 5.9: Dimensions of PMR controller parameters that satisfied FOMs constraints

parameter	item	value
k_i	$\texttt{length}(\texttt{unique}(\mathbf{N_r}(:,6)))$	1309
k_p	$\texttt{length}(\texttt{unique}(\mathbf{N_r}(:,7)))$	137
ω_c	$\texttt{length}(\texttt{unique}(\mathbf{N_r}(:,8)))$	41

The number of multi-objective function weight combinations for (5.24) and (5.25) is provided in Table 5.10.

Table 5.10: Dimensions involved in determining the weights of the multi-objective function of the PMR controller

item	value	reference	used in	note
$\texttt{length}(\boldsymbol{\kappa}_r)$	289463	(5.24)	Algorithm 7, 8	LWC
$\texttt{length}(\boldsymbol{\lambda}_r)$	31029	(5.25)	Algorithm 7, 8	NLWC

5.6.2 Number of Problems in each Level

The number of problems in each level and a maximum number of problems in a chosen Path are provided in Table 5.11. Here the columns L1, L2 and L3 refer to the maximum number of problems in Level-1, Level-2 and Level-3, respectively. It can be observed here that Path#1 and Path#3 have the same number of problems. Similarly, Path#2 and Path#5. Similarly, Path#4 and Path#6.

Table 5.11: Maximum number of problems for the six paths

item	L1	L2	L3	Max. No. of problems
Path#1	1	1309	137	$1 \times 1400 \times 200 = 179333$
Path#2	1	1309	41	$1 \times 1400 \times 41 = 53669$
Path#3	1	137	1309	$1 \times 200 \times 1400 = 179333$
Path#4	1	137	41	$1 \times 200 \times 41 = 5617$
Path#5	1	41	1309	$1 \times 41 \times 1400 = 53669$
Path#6	1	41	137	$1 \times 41 \times 200 = 5617$

5.6.3 Time Consumed per Problem

PMR controller (4.27) parameters for the obtained solutions $\mathbf{R}_n$ and $\mathbf{K}_n$, where $n \in \{0, 1, 2..6\}$ is shown in Fig. 5.7. For the obtained solutions, the computation time involved is shown in Fig. 5.14(a). In this context, the benefit, B_η, is the ratio of computation time with the LWC method to computation time with the NLWC method for a given multi-objective convex optimization problem and is shown in Fig. 5.14(b).

From Fig. 5.7 and Fig. 5.14(b) it is evident that NLWC should be the preferred choice over the LWC. Given the maximum number of problems as in Table 5.11 and corresponding computation times with LWC and NLWC methods in Fig. 5.14(a), the computation time per one problem is shown in Table 5.12.

It can be observed here that Path#1 and Path#3 have the same number of problems, but different computation times per problem. Similarly with other paths. The size of the data set that is processed in one problem will have a significant impact on the time it takes to finish the problem.

Table 5.12: Time consumed per one problem in the design of PMR controller

item	LWC	NLWC	B_η
No hierarchy	1111s	116.96s	9.4989
Path#1	400.97ms	22.813ms	17.577
Path#2	121.13ms	29.203ms	4.1477
Path#3	213.67 ms	20.809 ms	10.268
Path#4	280.55 ms	32.593 ms	8.6076
Path#5	99.484 ms	12.305 ms	8.80848
Path#6	279.31 ms	32.215 ms	8.6702

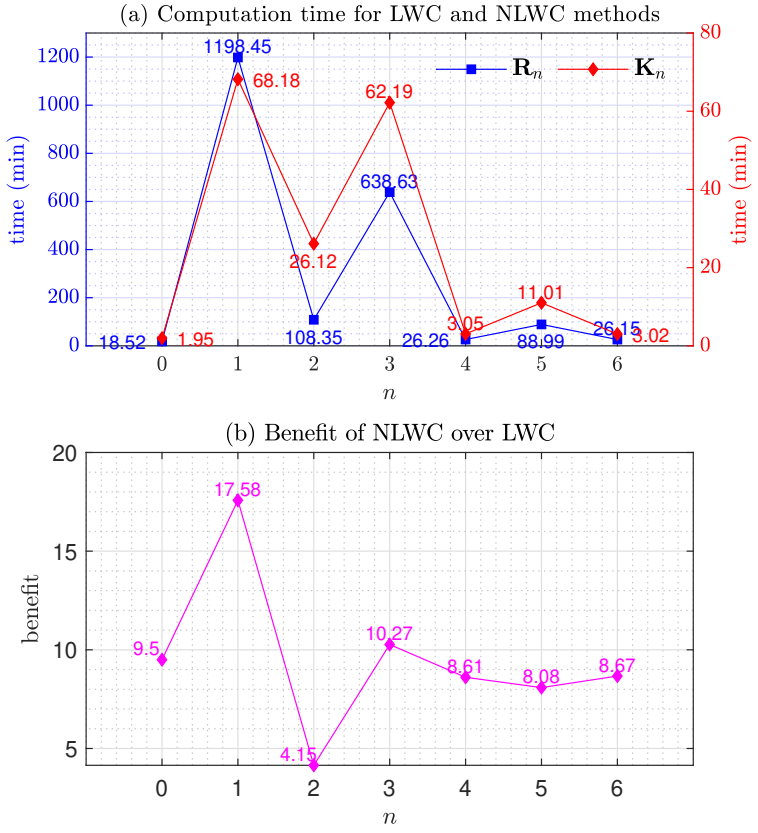

Figure 5.14: Computation time and benefit (B_η) of NLWC over LWC

5.6.4 CPU Utilization

Fig. 5.15 shows the CPU usage peaking to 100% from an initial value of around 3% in the evaluation of $\mathbf{R}_0$ with Algorithm.7. Fig. 5.15 can be observed in the sequence A-B-C-D. Here the algorithm needs to process the complete data set of $\mathbf{N_r}$. The CPU clock speed is also around the maximum value. MATLAB uses a multi-threaded computation by default and thus it seeks to maximize resource utilization based on the algorithm architecture. In

this part of the thesis, no explicit parallel computing is considered.

Fig. 5.16 shows the CPU usage going to around 20% from an initial value of around 3% in the evaluation of $\mathbf{R}_1$ with Algorithm.8. Fig. 5.16 can be observed in the sequence E-F-G-H. Here the algorithm needs to process only pieces of the data set of $\mathbf{N_r}$ at a given instance. The CPU clock speed is not up to the maximum value. Though MATLAB has inbuilt multi-threaded computation since no explicit parallel computing is considered, resource utilization is poor. This calls for parallel computing, as the computing machine used in this part of the thesis has 8 cores.

In a larger context where hierarchical optimization is considered for larger systems for example electrical power systems, then the concept of distributed computing and parallel computing can be further explored.

5.7 Summary

This chapter has presented the optimization algorithms and optimization results. Firstly, the fundamentals required to formulate and solve a multi-objective convex optimization problem are explained. Second, the multi-objective convex optimization problems for the design optimization of the Type-II PI controller and PMR controller are provided. Third, three optimization algorithms are proposed to solve the different types of controller design optimization. Fourth, optimization results are provided and validated with a unit step response plot and bode plot.

Fifth, it is shown that the nonlinear weight constraint method is a better objective function weight tuning method compared to the linear weight constraint method. Specifically, the *%improvements with the NLWC method provide an improved phase margin and decreased percentage overshoot at a lesser expense of an increase in the rise time, compared to the LWC method.*

Sixth, the *significance of the hierarchical framework in leveraging the effect of a design variable in the optimization of the final result is demonstrated.*

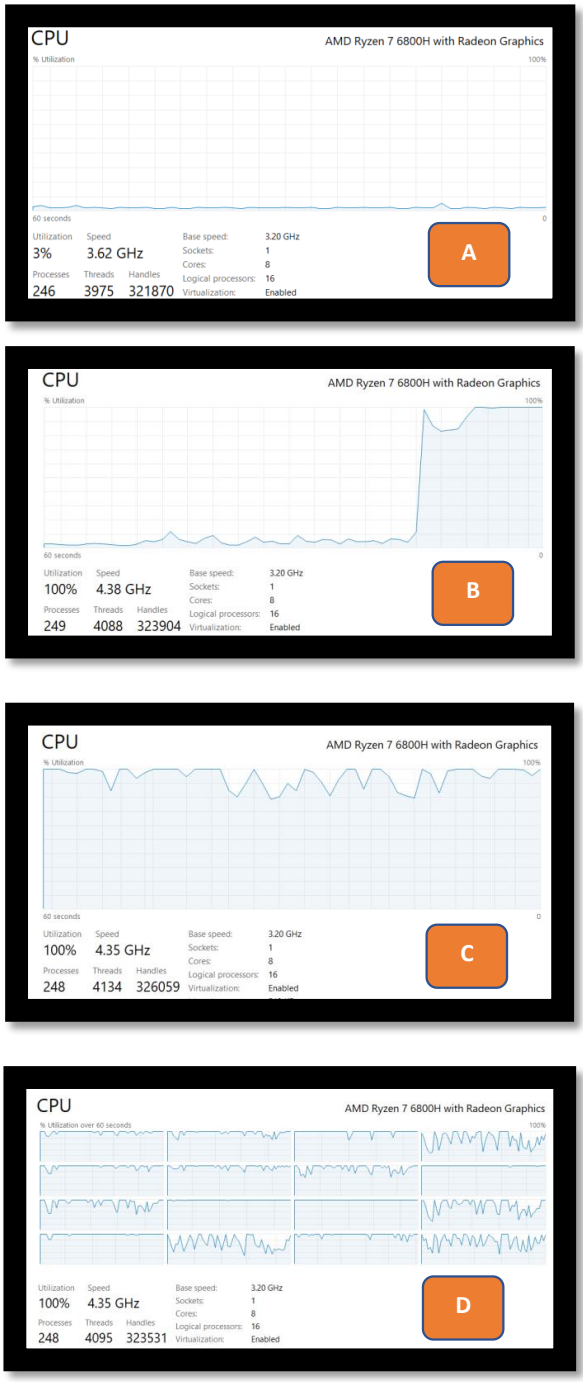

Figure 5.15: CPU usage when Algorithm 7 is run to evaluate $\mathbf{R}_0$

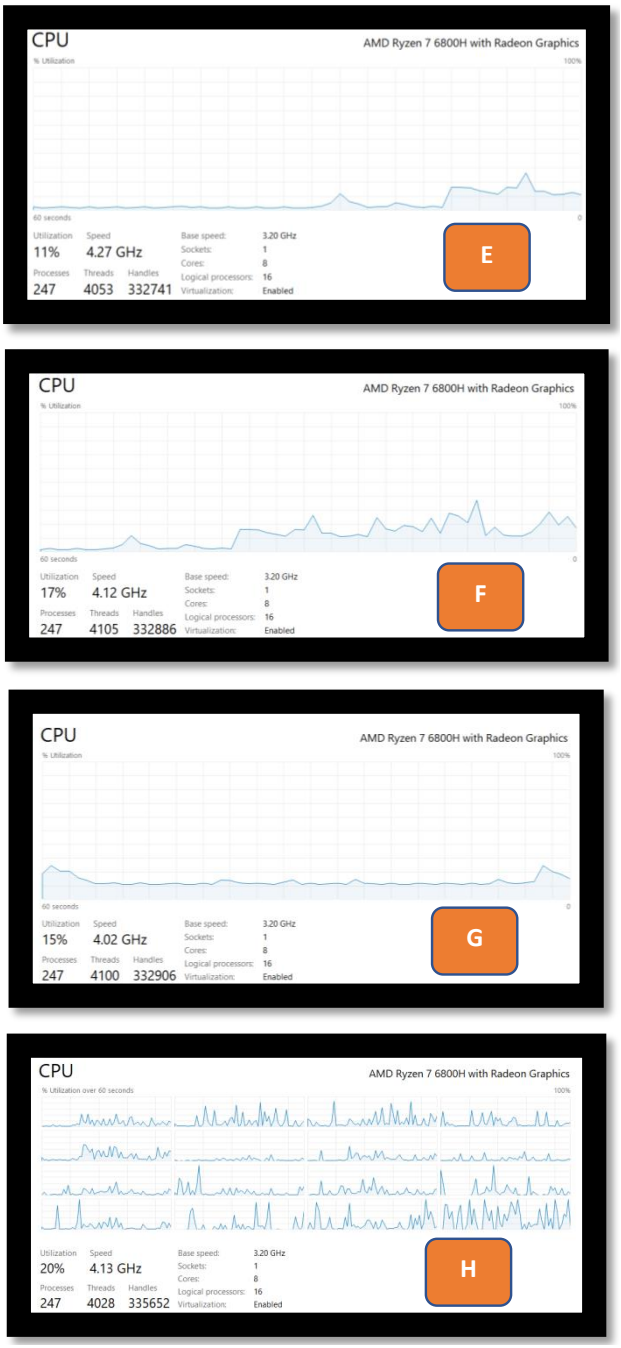

Figure 5.16: CPU usage when Algorithm 8 is run to evaluate $\mathbf{R}_1$ i.e., hierarchical optimization with Path#1 and LWC method

Chapter 6

Harmonic Performance Evaluation and Statistical Insights

> By the sun and its brightness, and the moon as it follows it, and the day as it unveils it, and the night as it conceals it! And by heaven and 'the One' Who built it, and the earth and 'the One' Who spread it! And by the soul and 'the One' Who fashioned it, then with 'the knowledge of' right and wrong inspired it! Successful indeed is the one who purifies their soul.
>
> *Quran, Chapter 91 (The Sun), Verses 1-9.*

6.1 MATLAB Simulation

6.1.1 Scenarios Considered for the MATLAB Simulation

The MATLAB simulation is conducted for two broad scenarios: ideal grid voltage and non-ideal grid voltage. The ideal grid voltage and non-ideal grid voltage are considered as (6.1) and (6.2), respectively.

$$u_g(t) = \sqrt{2}U_g \sin(\omega_1 t) \tag{6.1}$$

$$u_g(t) = \sqrt{2}U_g \sin(\omega_1 t) + 0.03\sqrt{2}U_g \sin(5\omega_1 t) + 0.02\sqrt{2}U_g \sin(7\omega_1 t) + 0.01\sqrt{2}U_g \sin(9\omega_1 t) \tag{6.2}$$

In total, two voltage loop controllers and 16 current loop controllers are designed using convex optimization as explained in Table 5.1 and Table 5.2. The two voltage loop controllers point to the same solution as shown in Table 5.3. Thus in total, 32 cases are considered for the MATLAB simulation as detailed in Table 6.1, to see how these numbers in the best solutions translate into physics such as THD_i. For all cases, the voltage controller of Type-II PI is used with the controller parameters as detailed in Table 5.3. The controller parameters for the Type-II PI controller and PMR controller for the current loop are detailed in Table 5.4 and Fig. 5.7. Table 6.1 lists the transfer functions considered in the current loop for all 32 cases. The control block diagram used in the MATLAB simulation for the cases with Type-II PI

controller and PMR controller can be seen in Fig. 4.11 and Fig. 4.12, respectively.

6.1.2 Details of the Computer used for Running the MATLAB

The computer with the details mentioned in Table 6.2 is used for running all the Programs and Simulink-related files developed in MATLAB.

Table 6.2: Details of computer used for running the MATLAB

Item	Detail
Computer	ASUS TUF A17 TUF707RC-DS71-CA
RAM	16 GB DDR5
CPU	AMD Ryzen 7 6800H with Radeon Graphics
CPU Cores	8(physical), 16(logical)
CPU Clock speed	3.2 GHz (base), 4.8 GHz (turbo)
GPU	NVIDIA GeForce RTX 3050 GDDR6 4GB
GPU Clock speed	1.5 GHz (base), 1.7 GHz (Turbo)
Hard-drive type	Solid state drive
Operating System	Windows 11 Home

6.1.3 Macro-Model of H-bridge

A macro-model considers the power electronic switching device's behaviour account in the simulation with the implementation of the IGBT switch defined for this purpose in MATLAB. At the macro level, the behaviour of IGBT switching transitions can be taken into account in the MATLAB simulation with the inclusion of the capacitance and inductances as discussed in the following. The steady-state behaviour of the switch can be considered with the MATLAB simulation as: When the switch is off, it is an open circuit and when the switch is on, it is modelled by its conduction characteristics. The PSD considered in Fig. 4.1 is an IGBT with the product ID IKW75N65EL5 [123].

6.1.3.1 Capacitance

IGBT has an inter-electrode capacitance [123] between all of its three terminals as shown in Fig. 6.1. Inter-electrode capacitance can be approximated [124] as open circuit, open circuit and manufacturer-specified capacitance value for DC signal, medium frequency signal (i.e., small signal) and high-frequency signal (i.e., large signal), respectively. The switching transition i.e., turn-on or turn-off is a large signal phenomenon. Apart from the inter-electrode capacitance, parasitic capacitance (C_p) due to PCB is present and is considered between the Collector and Emitter of the IGBT [123]. From Fig. 6.1, the large signal model

Table 6.1: Current loop controller and different cases for MATLAB Simulation

Case	grid voltage	controller	current loop TF	Note
1	ideal	Type-II PI	$G_i(s)T_{2i}(s)$, LWC	-
2			$G_i(s)T_{2i}(s)$, NLWC	-
3		PMR	$G_i(s)H_{rR0}(s)$	-
4			$G_i(s)H_{rR1}(s)$	Path#1
5			$G_i(s)H_{rR2}(s)$	Path#2
6			$G_i(s)H_{rR3}(s)$	Path#3
7			$G_i(s)H_{rR4}(s)$	Path#4
8			$G_i(s)H_{rR5}(s)$	Path#5
9			$G_i(s)H_{rR6}(s)$	Path#6
10			$G_i(s)H_{rK0}(s)$	-
11			$G_i(s)H_{rK1}(s)$	Path#1
12			$G_i(s)H_{rK2}(s)$	Path#2
13			$G_i(s)H_{rK3}(s)$	Path#3
14			$G_i(s)H_{rK4}(s)$	Path#4
15			$G_i(s)H_{rK5}(s)$	Path#5
16			$G_i(s)H_{rK6}(s)$	Path#6
17	non-ideal	Type-II PI	$G_i(s)T_{2i}(s)$, LWC	-
18			$G_i(s)T_{2i}(s)$, NLWC	-
19		PMR	$G_i(s)H_{rR0}(s)$	-
20			$G_i(s)H_{rR1}(s)$	Path#1
21			$G_i(s)H_{rR2}(s)$	Path#2
22			$G_i(s)H_{rR3}(s)$	Path#3
23			$G_i(s)H_{rR4}(s)$	Path#4
24			$G_i(s)H_{rR5}(s)$	Path#5
25			$G_i(s)H_{rR6}(s)$	Path#6
26			$G_i(s)H_{rK0}(s)$	-
27			$G_i(s)H_{rK1}(s)$	Path#1
28			$G_i(s)H_{rK2}(s)$	Path#2
29			$G_i(s)H_{rK3}(s)$	Path#3
30			$G_i(s)H_{rK4}(s)$	Path#4
31			$G_i(s)H_{rK5}(s)$	Path#5
32			$G_i(s)H_{rK6}(s)$	Path#6

of IGBT will have its output capacitance defined as [124]

$$C_{os} = C_{ce} + C_{bc} \tag{6.3}$$

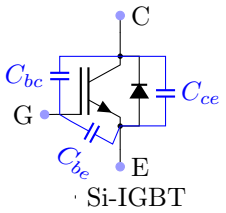

Figure 6.1: High-frequency model of IGBT

Typically data sheets only provide output capacitance (C_{os}) value instead of inter-electrode capacitance. The output capacitance determines the turn-off characteristics of the switch. To begin with, in this part of the thesis, only $C_{os} + C_p$ is considered as one element of capacitance across the body diode. The value of $C_{os} + C_p$ is also essential to the design of the snubber circuit for the IGBT. The capacitance values are defined in Table 6.3.

6.1.3.2 Inductances

The internal emitter inductance (L_e) measured 5mm from the case is considered [123]. Typically for an IGBT chip, L_e would be low in comparison to a module IGBT. L_e is specified as a parameter value in the IGBT model available in the MATLAB Simulink. The circuit stray inductance (L_p) [123, 125, 126] is a lumped representation of the distributed inductances within a commutation loop. For MATLAB simulation, the stray inductance (L_p) is considered as $0.5L_p$ and $0.5L_p$ in the positive DC bus and negative DC bus, respectively at the input side of the H-bridge. These inductances are responsible for the voltage spike one sees on top of the DC bus voltage when a switch is in the turn-off transition. The value of $L_e + L_p$ is essential to the design of the snubber circuit for the IGBT. The MATLAB Simulink model will account for the internal inductances only if the simulation is carried out over a continuous time. The inductance values are defined in Table 6.3.

6.1.3.3 Conduction Characteristics

For the forward conducting transistor, on-state resistance (R_{on}) and forward voltage drop (V_f) are calculated based on the tangents drawn to the V-I characteristics of the switch [44]. For the reverse conducting diode: on-state resistance (R_d) and forward voltage drop (V_d) are considered. Table 6.3 shows the values considered in the simulation.

6.1.3.4 Dead-Time of the Switches

The turn-on delay time ($t_{d,on}$) and turn-off delay time ($t_{d,off}$) are used in the calculation of the required dead time between switches of the same leg. These delay times are a function of

the junction temperature of the IGBT [123]. The required dead-time, considering the wide operating range of junction temperature can be calculated as follows

$$t_{d,on} = \texttt{max}(t_{d,on1}, t_{d,on2}) \tag{6.4}$$

$$t_{d,off} = \texttt{max}(t_{d,off1}, t_{d,off2}) \tag{6.5}$$

$$t_d > 1.2(t_{d,off} - t_{d,on}). \tag{6.6}$$

Where $t_{d,on1}$ and $t_{d,on2}$ are the turn-on delay time at junction temperatures 25°C and 150°C, respectively. $t_{d,off1}$ and $t_{d,off2}$ are the turn-off delay time at junction temperatures 25°C and 150°C, respectively. The dead-time is chosen to be at least 20% higher than the minimum required dead-time. The dead-time value and its related calculations are shown in Table 6.3.

6.1.3.5 Optimized RC Snubber

The ringing frequency of the voltage across the switch during the turn-off due to the capacitance and inductance in the commutation loop is given as [127]

$$F_r = \frac{1}{2\pi\sqrt{(L_e + L_p)(C_{os} + C_p)}}. \tag{6.7}$$

The optimized RC snubber circuit parameters can be determined as

$$R_s = \frac{1}{2\zeta}\sqrt{\frac{L_e + L_p}{C_{os} + C_p}} \tag{6.8}$$

$$C_s = \frac{1}{2\pi R_s F_r}. \tag{6.9}$$

Where ζ is the damping factor of the RC snubber design. The dead-time value and its related calculations are detailed in Table 6.3. For ζ=0.5, during switch turn-off, the collector-to-emitter voltage of the IGBT takes a maximum of around 720V. It is then brought down to about 400V by increasing ζ to 6. It is to be observed that the control loop design is performed using small-signal modelling. Theoretically, it is expected that control loop dynamics are independent of the large-signal behaviour of the switch and commutation loop parasitics.

6.1.4 Results of the Simulation for the Case#26

The continuous-time simulation with the MATLAB settings defined in Table 6.4 is considered for Case#26 listed in Table 6.1, and its results are shown in Fig. 6.2 and Fig. 6.3. When it is a continuous-time simulation, the user-defined value of internal emitter inductance for IGBT is included. Fig. 6.2(a) show the injection of current into the non-ideal grid at the UPF. Fig. 6.2(b) show the regulation of output current just near the zero crossing. Fig. 6.2(c) show the regulation of output current at the sinusoidal peak. It can be observed that the mean value of the output current near the zero crossing exhibits a phase delay with respect to the reference signal.

Table 6.3: MATLAB simulation parameters, RC snubber calculations and dead-time calculations

Parameter	description	value	Inclusion in simulation	Reference
C_{os}	output capacitance of IGBT	150pF	external element	IKW75N65EL5
C_p	stray capacitance	30pF	external element	IKW75N65EL5
L_e	internal emitter inductance	13nH	defined in MATLAB model for IGBT	IKW75N65EL5
L_p	commutation loop stray inductance	40nH	external element	IKW75N65EL5
V_f	forward voltage drop of IGBT	0.9V	defined in MATLAB model for IGBT	IKW75N65EL5
R_{on}	on-state resistance of IGBT	2.99mΩ	defined in MATLAB model for IGBT	IKW75N65EL5
V_d	diode forward voltage drop	0.87V	defined in MATLAB model for diode	IKW75N65EL5
R_d	diode on-state resistance	7.07mΩ	defined in MATLAB model for diode	IKW75N65EL5
$t_{d,on1}$	turn-on delay time	40ns	-	IKW75N65EL5
$t_{d,on2}$	turn-on delay time	39ns	-	IKW75N65EL5
$t_{d,off1}$	turn-on delay time	330ns	-	IKW75N65EL5
$t_{d,off2}$	turn-on delay time	275ns	-	IKW75N65EL5
t_d	dead-time	316ns	defined in MATLAB on/off delay block	(6.6)
F_r	ringing frequency	51.5MHz s	-	(6.7)
ζ	damping factor of RC snubber design	6	-	-
R_s	snubber resistance	1.43Ω	defined in MATLAB model for IGBT	(6.8)
C_s	snubber capacitance	2.16nF	defined in MATLAB model for IGBT	(6.9)

Fig. 6.2(d)-(f) shows the regulation of DC bus voltage. It can be observed that DC bus voltage is designed for a voltage ripple of 8V, and the obtained result is in agreement with the same as evident from Fig. 6.2(d). Fig. 6.2(g)-(i) shows the current delivered by the PV array. Fig. 6.2(j)-(l) shows the current at the input of the H-bridge. Fig. 6.2(m)-(o) shows the DC bus capacitor current. It can be seen that a large percentage of the H-bridge input current's 120Hz component is supplied by the capacitor, but not the source i.e., the PV array.

Fig. 6.3(a)-(b) shows the current of IGBT switch S_1 considered in Fig. 4.1. Similarly, Fig. 6.3(c)-(d) shows the voltage across the IGBT Switch S_1. Fig. 6.3(e) show the dead-time compensation voltage v_{dt} for one cycle of output current. Fig. 6.3(f) show the dead-time compensation voltage v_{dt} for approximately three carrier cycles. Fig. 6.3(g) show the delaying of the IGBT switch S_1 gate signal. Fig. 6.3(h) show the delaying of the IGBT switch S_2 gate signal. Fig. 6.3(i) show the delayed gating pulses given to IGBT switches S_1 and S_2.

Fig. 6.3(j) show the delayed gating pulses given to IGBT switches S_1 and S_2 in one carrier period. For the aforesaid carrier period, Fig. 6.3(k) and Fig. 6.3(n) show the IGBT switch S_1 current and voltage, respectively. For the aforesaid carrier period, Fig. 6.3(l) and Fig. 6.3(m) show the IGBT switch S_1 turn-off transition and turn-on transition, respectively. The effectiveness of the RC snubber design considered in this part of the thesis can be observed here. Since this is just an improved Macro-Model which doesn't completely consider the high-frequency model of IGBT, the reproduction of rise and fall characteristics of voltage and current similar to an IGBT is not possible.

Table 6.4: MATLAB simulation settings used for continuous-time simulation

Item	Selection	Located in
Simulation type	Continuous	powergui
Preference	Disable ideal switching	powergui
Solver Type	Variable-step	Model configuration
Solver	ode23tb(stiff/TR-BDF2)	Model configuration
Relative tolerance	1e-8	Model configuration
Absolute tolerance	1e-8	Model configuration

6.2 Controllers Evaluation for Current Harmonic Performance

The discrete-time simulation with the MATLAB settings defined in Table 6.5 is conducted for the 32 cases listed in Table 6.1. For a case of discrete-time simulation, $L_e = 0$. Fig. 6.4(a) and Fig. 6.4(i) show the THD_i of output AC for the cases considered under ideal-gird and non-ideal grid, respectively, for all 32 cases listed in Table 6.1. Similarly, Fig. 6.4(b) and Fig. 6.4(j) show the peak value of the fundamental component of the output AC for the cases considered under the ideal-gird and non-ideal grid, respectively. Similarly, Fig. 6.4(c)-

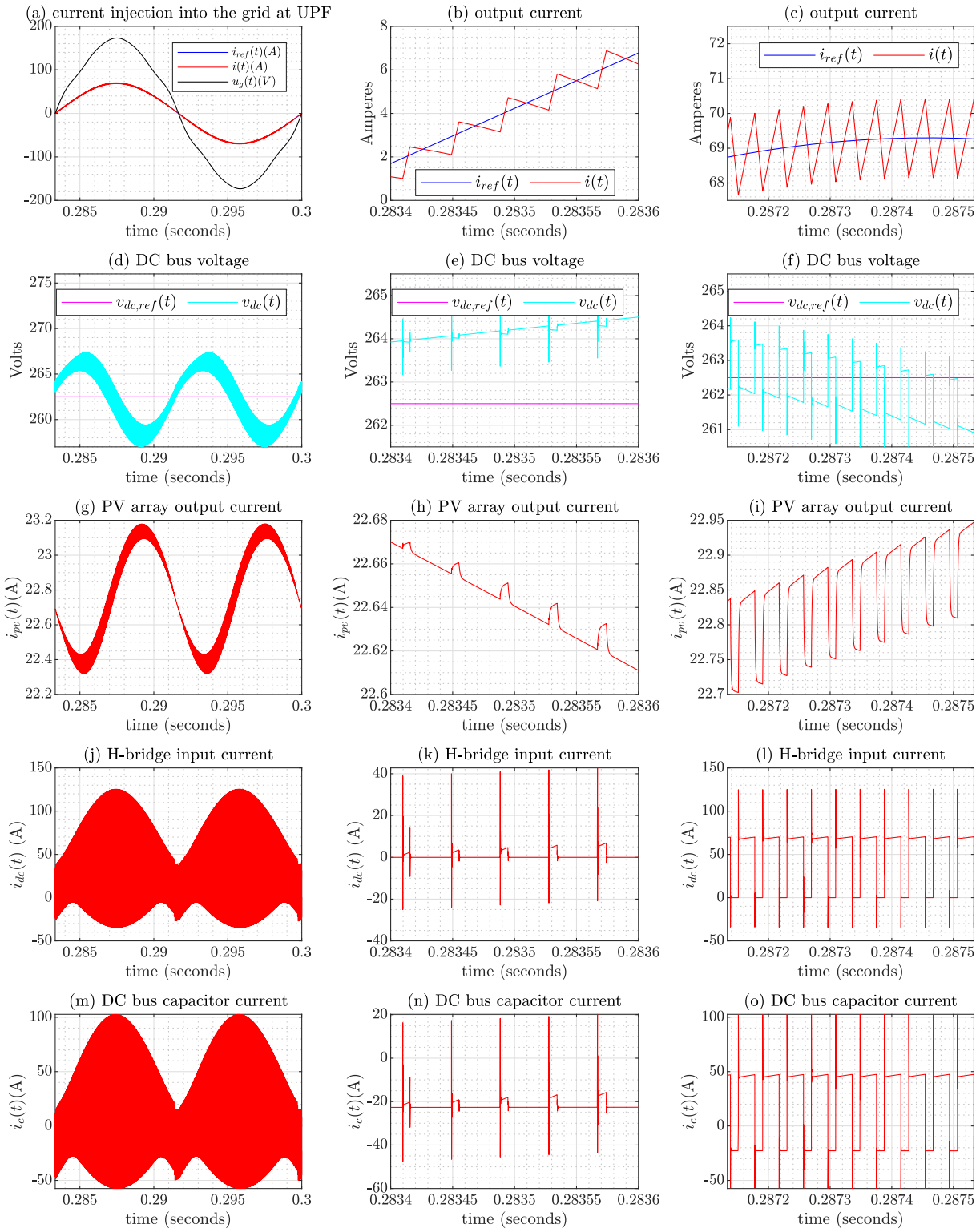

Figure 6.2: Voltage and current waveforms of the inverter operation for the Case#26 with the MATLAB settings defined in Table 6.4, i.e., continuous-time simulation.

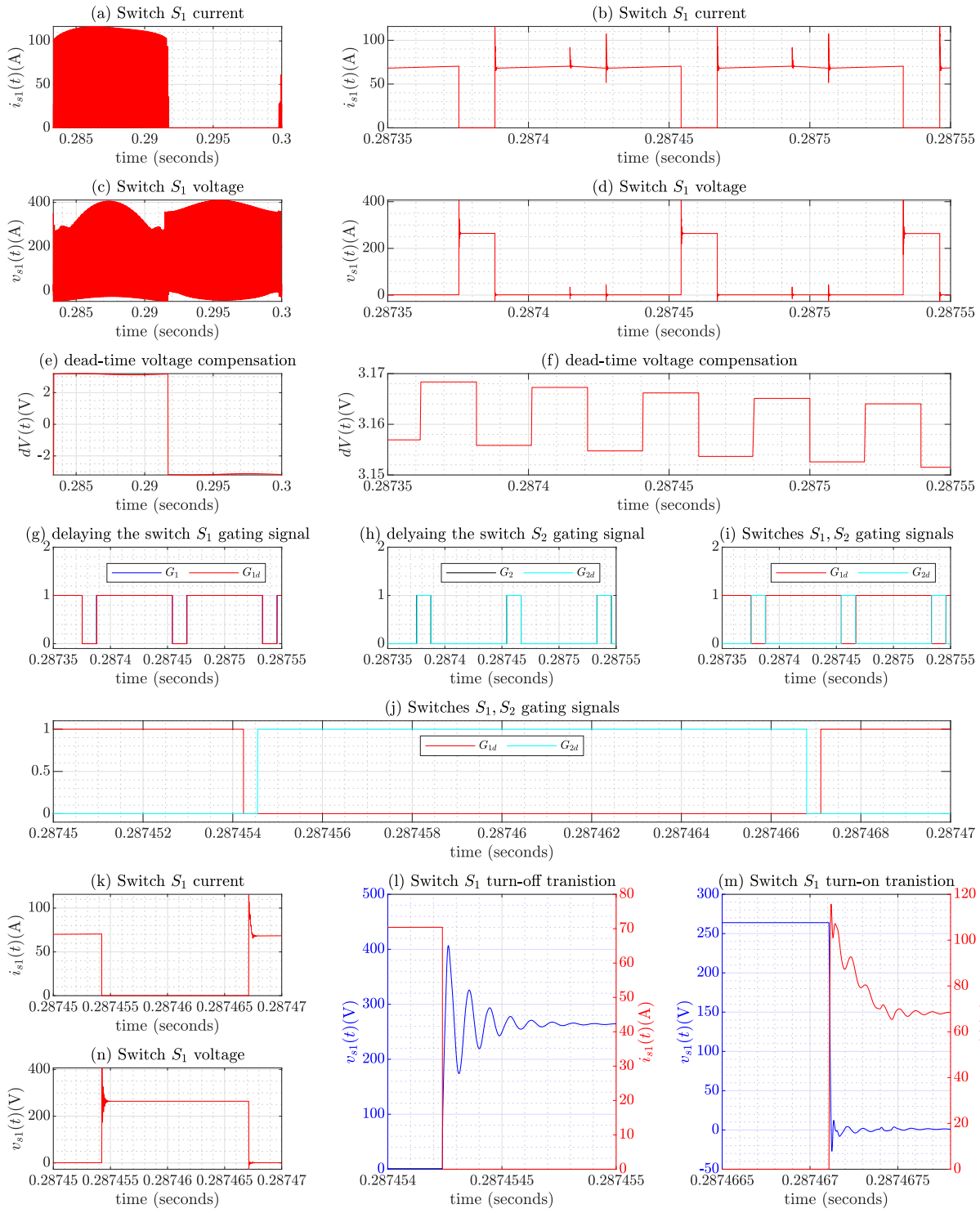

Figure 6.3: Voltage and current waveforms of the inverter switching element and dead-time voltage compensation for the Case#26 with the MATLAB settings defined in Table 6.4, i.e., continuous-time simulation.

(h) and Fig. 6.4(k)-(p) show the peak value of the odd harmonics of the output AC for the cases considered under ideal-gird and non-ideal grid, respectively.

As the PMR controller considered in this part of the thesis has controllers for odd harmonics up to the 9^{th} order, its effect can be noticed i.e., the attenuation of odd harmonics with the PMR controller. Though the PMR controller provided a better attenuation compared to the Type-II PI controller, its impact is not too big. That is to say for 50Hz/60Hz which is the standard across various countries around the world for grid-connected systems, the application of any one of two controllers offers good performance. However, if an H-bridge is used for a higher fundamental component of output current, for example, in a 400Hz system, it is clear that the PMR controller would be a better choice in comparison to the Type-II PI controller.

Table 6.5: MATLAB simulation settings used for discrete-time simulation

Item	Selection	Located in
Simulation type	Discrete	powergui
Sample time	7.8989e-08s	powergui
Solver Type	Fixed-step	Model configuration
Solver	ode8(Dormand-Prince)	Model configuration

6.3 Statistical Insights

6.3.1 Phase Delay Correlation with Resonant Gain

Let $\boldsymbol{\phi_g}$ and $\boldsymbol{\phi_{ng}}$ be the phase angle of the fundamental component of output AC for cases #3 to #16 and cases #19 to #32, respectively i.e., considering only the PMR controller cases. Here discrete-time simulation is used. $\mathbf{R_g}$ is the gain of the open loop transfer function of the current loop for the cases involving the PMR controller. Fig. 6.5 shows the phase angle of the fundamental component of output AC and its reference signal provided to the PMR controller as can be seen in Fig. 4.12. The correlation between the phase angle of the fundamental component of the output AC and resonant gain can be seen in Table 6.6.

Table 6.6: Phase delay correlation with resonant gain

data-set1	data-set2	Correlation	ρ	p-value
$\mathbf{R_g}$	$\boldsymbol{\phi_g}$	Pearson	0.91887	3.4496e-06
$\mathbf{R_g}$	$\boldsymbol{\phi_{ng}}$	Pearson	0.91768	3.7558e-06
$\mathbf{R_g}$	$\boldsymbol{\phi_g}$	Spearman	0.99558	1.0592e-13
$\mathbf{R_g}$	$\boldsymbol{\phi_{ng}}$	Spearman	1	0

The Pearson test is used to find the strength and direction of the linear relationship between two variables. Spearman test is also known as the rank test and is used to find the

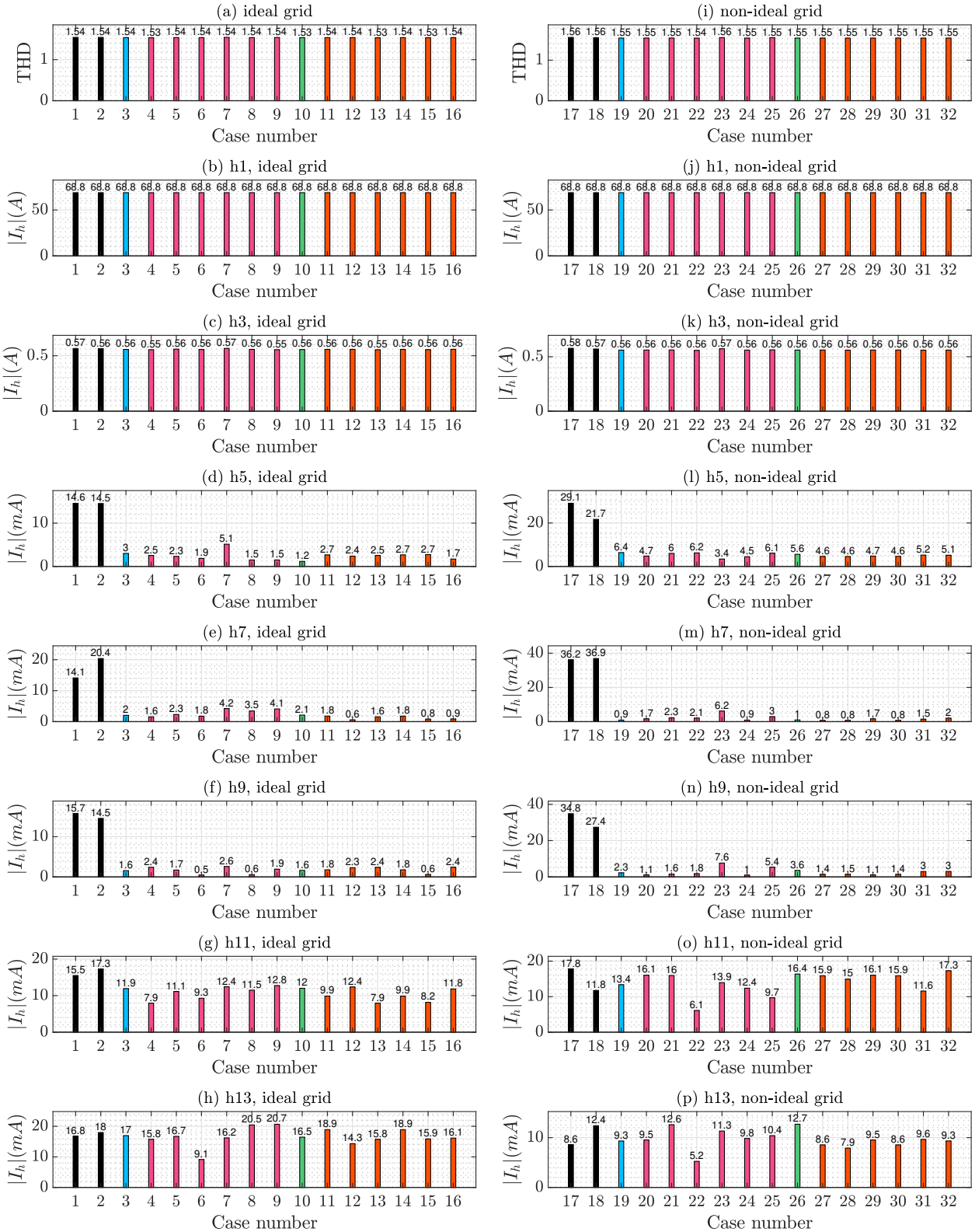

Figure 6.4: H-bridge output current's THD, fundamental component and odd-multiples of the fundamental component with the MATLAB settings defined in Table 6.5.

monotonicity in the relationship of two variables under examination. Table 6.6 shows that the phase angle delay and resonant gain have almost a perfect correlation.

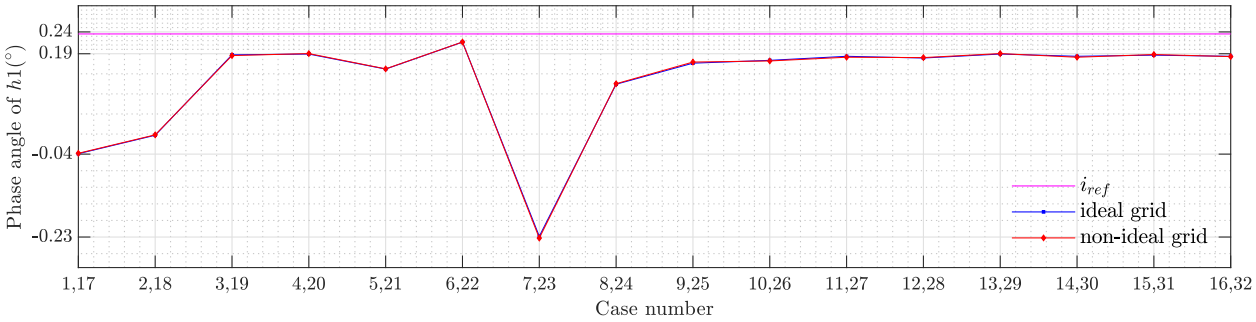

Figure 6.5: Illustration of phase delay: phase angle of output current's fundamental component with respect to the reference signal

6.3.2 Actual Overshoot Correlation with Designed Overshoot

The discrete-time simulation with the MATLAB settings defined in Table 6.5 is conducted for the cases #17 to #32 listed in Table 6.1. All 16 simulation scenarios concern the case where a non-ideal grid scenario as defined by (6.2) is considered. For all the 16 cases considered, the DC bus voltage reference is increased by 10% at t = 0.36s and brought back to the original value at t = 0.5s, and the corresponding results are shown in Fig. 6.6, Fig. 6.7 and Fig. 6.8 for the cases #17 to #22, #23 to #28, and #29 to #32, respectively.

The simulation results concerning the Type-II PI controller in the current loop, i.e., case #17 and #18 are shown in Fig. 6.6 (a)-(b) and Fig. 6.6 (c)-(d), respectively. The simulation results concerning the PMR controller, designed without hierarchy in the optimization, i.e., case #19 and #26 are shown in Fig. 6.6 (e)-(f) and Fig. 6.7 (g)-(h), respectively. The simulation results concerning the PMR controller, designed with hierarchy in the optimization, i.e., for the case #20 to #25 are shown in Fig. 6.6 (g)-(h), Fig. 6.6 (i)-(j), Fig. 6.6 (k)-(l), Fig. 6.7 (a)-(b), Fig. 6.7 (c)-(d), and Fig. 6.7 (e)-(f). The simulation results concerning the PMR controller, designed with hierarchy in the optimization, i.e., for the case #27 to #32 are shown in Fig. 6.7 (i)-(j), Fig. 6.7 (k)-(l), Fig. 6.8 (a)-(b), Fig. 6.8 (c)-(d), Fig. 6.8 (e)-(f), and Fig. 6.8 (g)-(h).

Based on the discrete-time simulation with the non-ideal grid scenario, along with harmonic performance evaluation shown in Fig. 6.4, the following inferences can be drawn.

- Irrespective of the type of controller and its specific parameters used in the regulation of the current loop, there is no noticeable difference in either transient performance or steady-state performance. i.e., all 16 case's waveforms look almost identical in the time domain to a human eye.
- The harmonic performance of the 16 cases can be seen in Fig. 6.4. Here one can see PMR controllers offer a better attenuation of low-order odd-multiple harmonics. This attenuation may be insignificant or significant depending on the intended application.
- For the specific impactful application considered in this thesis, i.e., DER inverter, the choice of controller seems trivial.

It can be observed that while designing the current loop a unit step-input is used to measure the percentage overshoot i.e., a broad range of frequency components in the input, however, the input that goes to the actual system is a sinusoidal signal. In a relative sense, one expects to see some sort of correlation between the designed overshoot and the actually obtained overshoot.

Let $\mathbf{x_1}$ and $\mathbf{x_2}$ are the percentage overshoot of output current for a change in the reference command signal at t=0.5s and the designed value of overshoot for a unit step-input, respectively as shown in Fig. 6.9, for the simulation results of cases #17 to #32, as seen in Fig. 6.6, Fig. 6.7 and Fig. 6.8. For the considered $\mathbf{x_1}$ and $\mathbf{x_2}$, the linear correlation and rank correlation are provided in Table 6.7. The linear correlation between $\mathbf{x_1}$ and $\mathbf{x_2}$ is positive

Table 6.7: Correlation between actual overshoot and design overshoot

data-set1	data-set2	Correlation	ρ	p-value
$\mathbf{x_1}$	$\mathbf{x_2}$	Pearson	0.3299	0.21209
$\log(\mathbf{x_1})$	$\log(\mathbf{x_2})$	Pearson	0.75552	0.00071
$\mathbf{x_1}$	$\mathbf{x_2}$	Spearman	0.78761	0.00029

but insufficient data to prove it. The transformed variables of $\mathbf{x_1}$ and $\mathbf{x_2}$ are $\log(\mathbf{x_1})$ and $\log(\mathbf{x_2})$, respectively. These transformed variables have a strong positive correlation, supported by evidence of a p-value less than 0.05. It can be seen that $\mathbf{x_1}$ and $\mathbf{x_2}$ have strong monotonicity in the relationship evaluated using the Spearman test, supported by evidence of a p-value less than 0.05.

6.4 Summary

This chapter has presented an evaluation of the impact of the choice of controllers on the current harmonic performance and used simulation results to generate statistical insights. The strong literature advocates that PMR controller is superior to PI controllers because of the inadequate gain of the PI controller at the fundamental frequency. Now is this accepted notion true for all fundamental frequencies? If so, on what basis? Specifically, for gird-connected systems, where one has 50/60 Hz.

To counter the accepted opinion, one would first need the best choice of controller parameters. Thus the best controller parameters obtained in the previous chapter are used here. Then *it is discovered that the impact of the choice of the controller on current harmonic distortion is negligible. Henceforth, for a grid-connected system, from a THD_i perspective, the choice of Type-II PI controller or PMR controller is trivial.*

However, if one considers *phase delay in the tracking of the output current signal*, a higher gain of the controller at fundamental frequency would be beneficial, and *the PMR controller would be the right choice for output current regulation in grid-connected systems.*

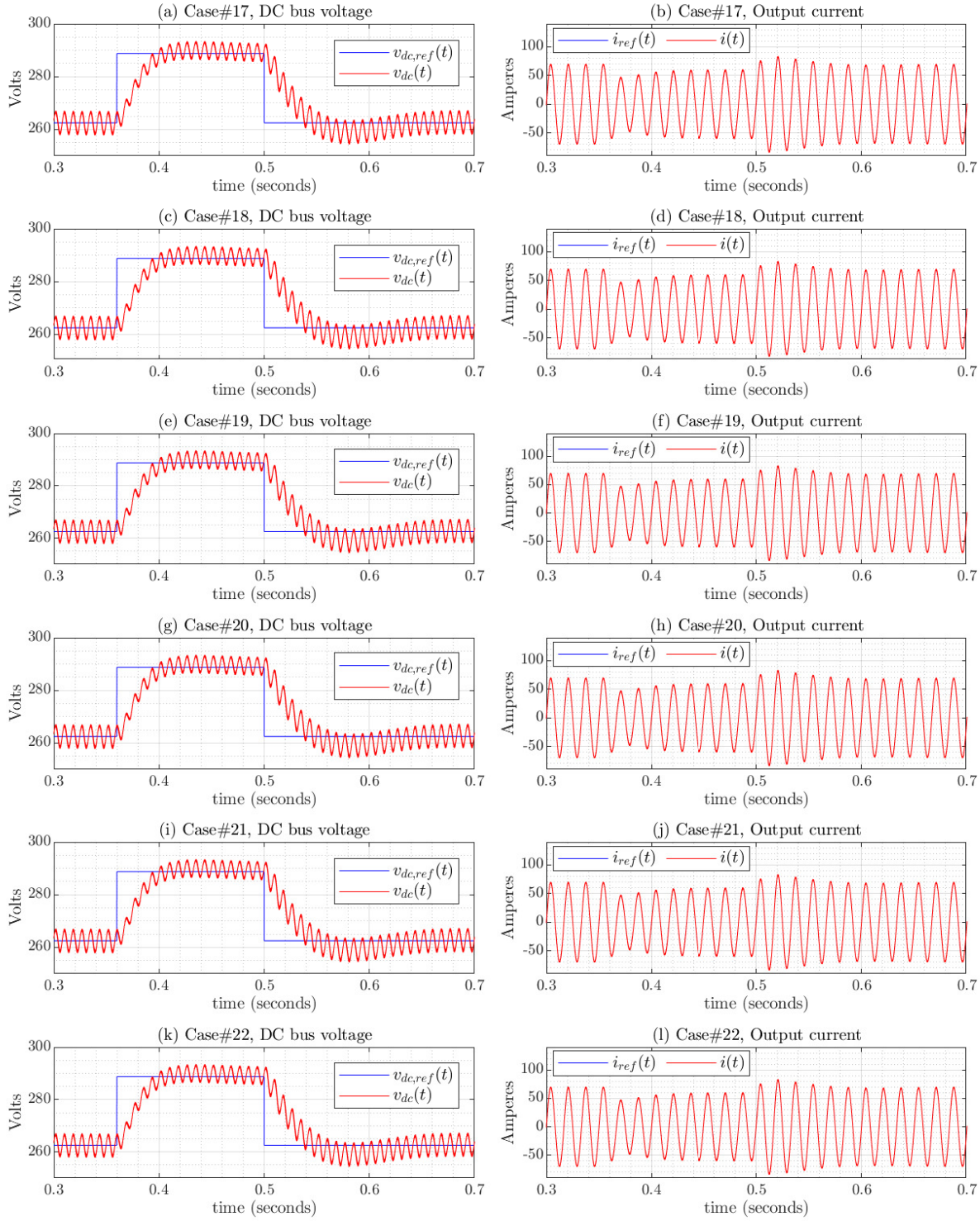

Figure 6.6: MATLAB simulation results of Cases #17 to #22 with the MATLAB settings defined in Table 6.5, i.e., discrete-time simulation.

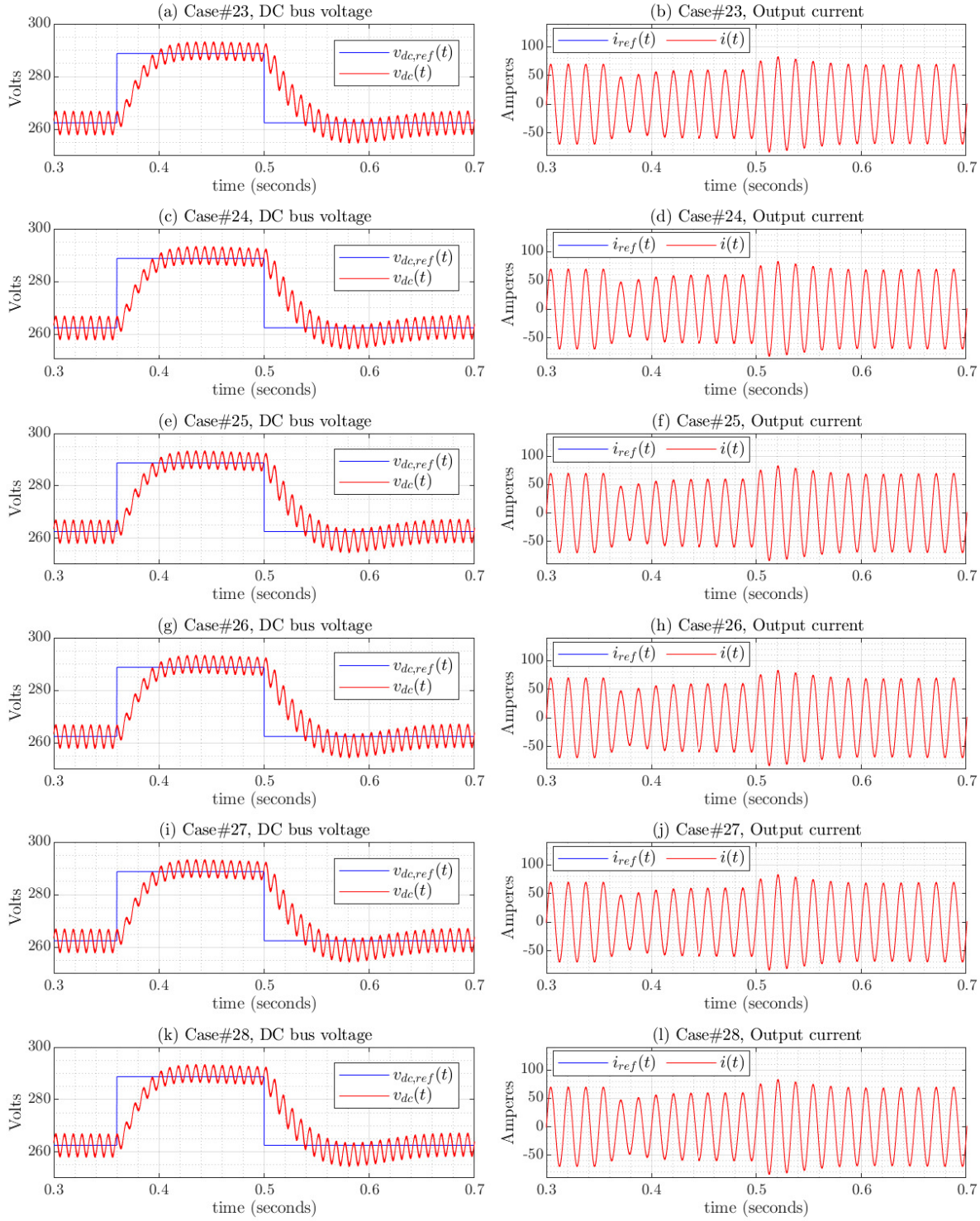

Figure 6.7: MATLAB simulation results of Cases #23 to #28 with the MATLAB settings defined in Table 6.5, i.e., discrete-time simulation.

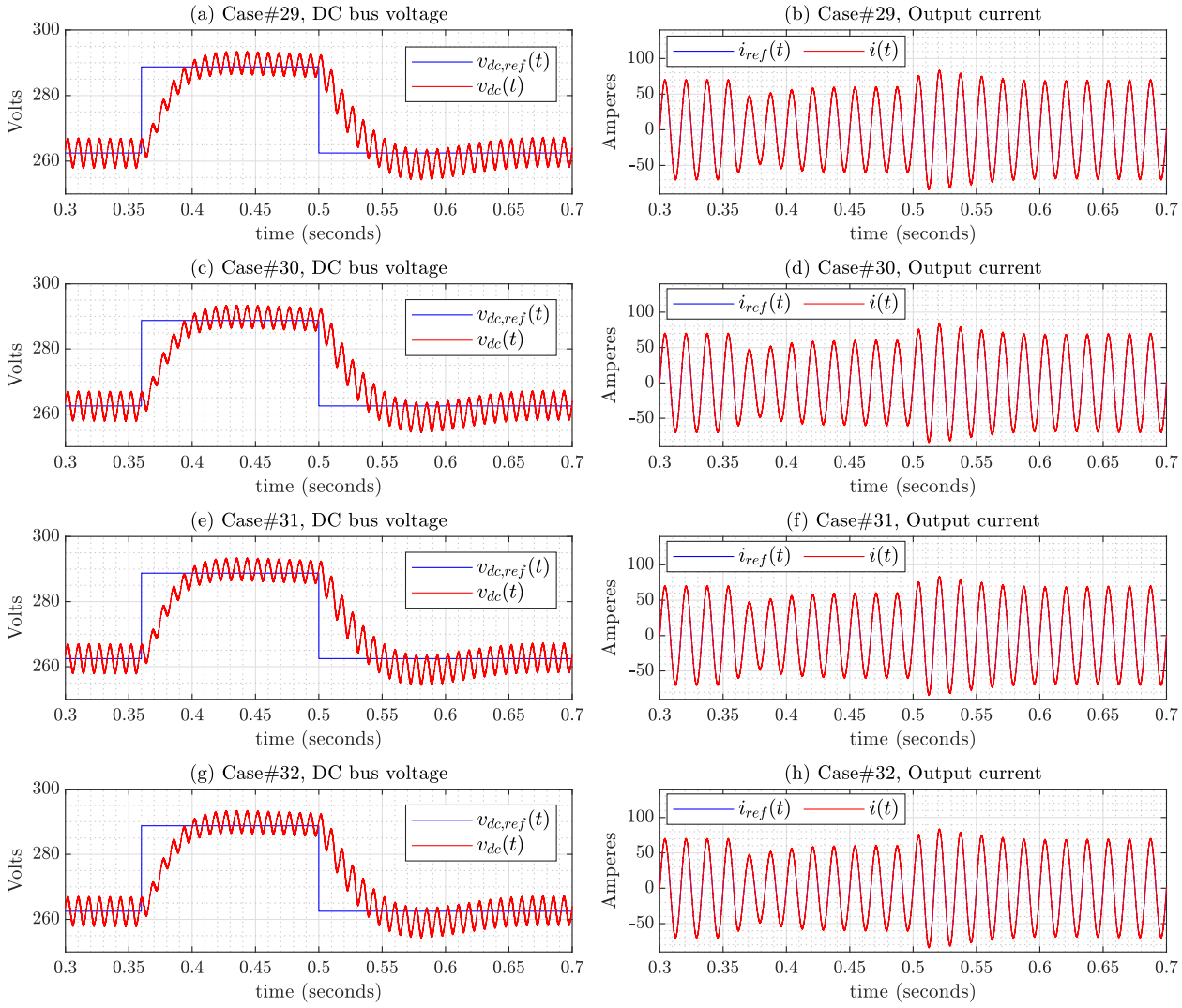

Figure 6.8: MATLAB simulation results of the cases #29 to #32 with the MATLAB settings defined in Table 6.5, i.e., discrete-time simulation.

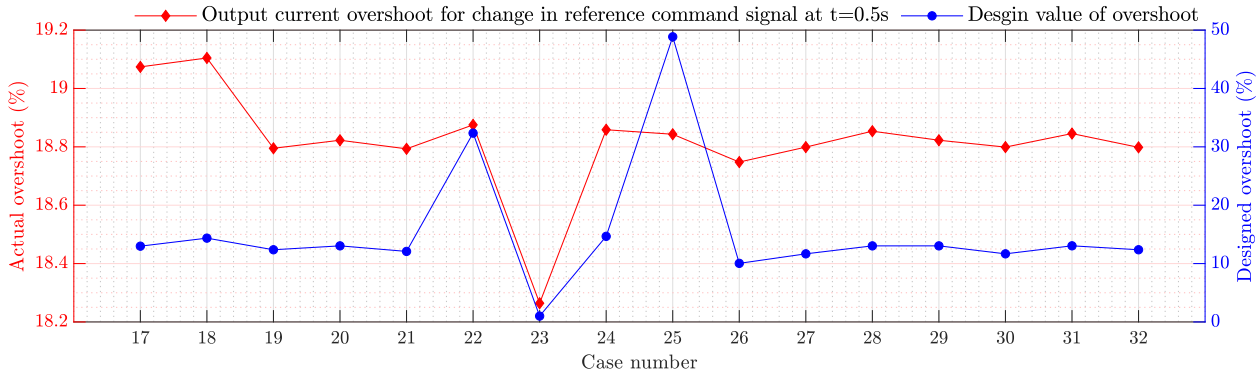

Figure 6.9: Overshoot measured from MATLAB simulation results and the designed value of Overshoot for a unit-step input for the Cases #17 to #32 as can be seen in Fig. 6.6, Fig. 6.7 and Fig. 6.8

Contributions, Conclusion, and Commercialization

Chapter 7

Summary

> Science is often misrepresented as "the body of knowledge acquired by performing replicated controlled experiments in the laboratory." Actually, science is something broader: the acquisition of reliable knowledge about the world.
>
> PROF. JARED DIAMOND
> *Civilization Scholar and Professor of Geography at UCLA.*

7.1 Contributions

7.1.1 Contributions: Part I

The contributions and novelty of this part of the thesis are

1. A manufacturer data-based, computational design optimization of grid-connected power electronic systems is proposed, for the first time.

2. Computational design optimization is further made efficient by proposing a computationally efficient algorithm for estimating the required frequency modulation ratio (m_f) to meet current harmonic performance requirements of grid-connected systems, compliance with IEEE519 [33].

3. The approach of manufacturer data inclusion in the design optimization reduces the uncertainty in design optimization and provides an optimal solution close to the practical scenario.

4. A Robust statistical modelling technique is proposed to estimate volume, weight, and cost of coupling inductance as a function of energy to be stored.

5. Most practical problems are hierarchical in nature. This principle is employed in other fields of engineering. However, this is the first time proposed for power electronic systems design. Here, an H-bridge is considered a fundamental topology, all other

changes such as N, M, L_f, and PSD lead to a new topology. Hence proposed a four-level optimization.

6. Finally, by integrating the aforementioned features, a novel Multi-Objective Hierarchical Optimization Design Framework (MO-HO-DF) to address the gap in the constrained design optimization w.r.t cost, weight, volume and high-performance of the bi-directional AC grid interface for an Energy Storage System (ESS) is proposed.

7.1.2 Contributions: Part II

The contributions and novelty of this part of the thesis are

1. Industry 4.0 (i4.0) is the optimization of computerization that took place in Industry 3.0 (i3.0). In this context, a computational design optimization of a linear control system for a PhotoVoltaic (PV)-fed grid-connected power electronic system is proposed for the first time.

2. Convex optimization is about the finest details, and the solution of convex optimization is a global solution. In continuation to the decades-long research in the design of controllers, the open research problems in the design of the Type-II PI controller and PMR controller, considering the time-domain and frequency-domain behaviour, are solved with convex optimization.

3. Extensive investigation of convex optimization problems in the design of a controller for a PV Inverter's linear control system is considered. Specifically, this part of the thesis solved 18 convex optimization problems, six of which are multi-objective convex optimization problems, and 12 are multi-objective hierarchical convex optimization problems.

4. Enhanced Marco-Model is implemented in the MATLAB simulation. This is the first step towards building a robust power electronic simulation model in MATLAB that can give results comparable to hardware experimentation. It is to be observed that the control loop design is performed using small-signal modelling, and theoretically speaking, control loop dynamics are largely independent of the large-signal behaviour of the switch and commutation loop parasitics.

5. For a PMR controller, statistical significance between the resonant gain and the phase delay of the output AC, is established for the first time. Statistical significance can be further used to build statistical algorithms, and to develop Artificial Intelligence (AI) algorithms.

6. For a PMR controller, statistical significance between the response of the control system to a standard test signal and sinusoidal excitation, is established for the first time.

7.2 Conclusion

7.2.1 Conclusion I

The design of a bi-directional AC grid interface, for an Energy Storage System (ESS), with desirable features such as high efficiency, high power density, low harmonic distortion and low cost involves numerous trade-offs that are hard to manage. This part of the thesis presented an innovative Multi-Objective Hierarchical Optimization Design Framework (MO-HO-DF) which allows the determination of the key parameters of an AC interface with interleaved H-bridges. These are the Number of parallel H-bridges (N), the number of parallel switches (M), Power Semiconductor Device (PSD) and coupling inductance (L_f). It employs a four-level design framework that breaks down the original problem into inner and outer sub-problems, thus reducing the order and complexity of the optimization problem. This leads to a set of optimal solutions constituting a Pareto front. The best solution among them is moved to an outer sub-problem in the hierarchical optimization until the best solution is identified.

The probabilistic model of coupling inductance Figures Of Merit (FOMs) for the design optimization framework is presented in detail. Four cases with two optimization paths were presented in this part of the thesis, in search of the optimal configuration considering eight FOMs. It considered the options of up to eight (N) H-bridges, each with up to eight (M) parallel switches interfaced by one of 28 possible coupling inductance values and 147 PSDs of three different types.

The selected optimized solutions presented many benefits compared to a base case found using standard single-level optimization procedure with N=1, M=1 and Si-IGBT technology. These include a reduction of multiple orders of magnitude for the coupling inductance with increased efficiency, reduced cooling effort, a significant decrease in weight and volume and achieved in a cost-efficient manner. The proposed design framework enables the user to tailor the system performance to their specific needs as demonstrated by the various optimal solutions shown in Table.3.5.

7.2.2 Conclusion II

The design of a Type-II PI controller for a PhotoVoltaic (PV) Inverter's control system with desirable features such as low rise time, low percentage overshoot, high phase margin and high bandwidth is an open research problem in the decades-long research of the design of controllers. This part of the thesis proposed a single-variable two-objective convex optimization method to design a Type-II PI controller for both voltage-loop and current-loop.

The design of a PMR controller for a PV Inverter's control system with desirable features such as low rise time, low percentage overshoot, high phase margin, high bandwidth and high resonant gain is an open problem. This part of the thesis proposed a three-variable five-objective convex optimization method to design a PMR controller for the current loop. The work on PMR controller design optimization is extended to a three-level hierarchical design framework, where all possible six paths are investigated, and the effect of each Path of optimization on the final result is shown.

In total, 18 convex optimization problems are solved in this part of the thesis: 9 problems

each with the LWC method and NLWC method. It is found that the NLWC method offers better optimization results than the LWC method, and also NLWC method has less time complexity. For a PMR controller, through statistical analysis, it is shown that there is a monotonicity between actual overshoot and design overshoot, and the resonant gain has a perfect correlation and monotonicity with the phase delay caused in the control loop.

Finally, a MATLAB simulation study is conducted with an enhanced macro-model of IGBT to compare the performance of the Type-II PI controller with the PMR controller for the output AC regulation under ideal-gird and non-ideal grid conditions. The benefit of resonant controllers usage up to the 9^{th} harmonic is shown.

7.2.3 Integrated Conclusion Statement

Optimization is the gist of the current phase of the technological revolution (i.e., i4.0), and given the need for interfacing of sustainable energy resources via DER Inverter, this thesis critically examined the efficient computation methodologies and techniques of multi-objective optimization for the DER Inverter. In this process of examination, firstly, a Multi-Objective Hierarchical Optimization Design Framework (MO-HO-DF), then a Multi-Objective Convex Optimization Design Framework (MO-CO-DF) is proposed.

This thesis also used and then examined the social science concepts such as the principle of hierarchy, the principle of equality, and the principle of equity. Specifically, the principle of equity tackles the objective functions that are inflated. The concepts developed in the thesis, in the context of DER Inverter, are *first of their kind and pertinent to the current phase of the technological revolution.* The developed techniques can be applied to a wide range of problems in engineering and sciences.

7.3 Commercialization Potential

7.3.1 Part I

The manufacturer data-based optimization technique proposed in Part-I of the thesis can be utilized to *automate* the *smart design* of power electronic systems. In particular, one can easily obtain different types of products to cater to different segments of customers: low-cost solutions and high-power density (compact, but at high cost) solutions. The proposed technique can further incorporate Inductor-Capacitor-Inductor (LCL) filter design into the optimization framework to make the DER Inverter suitable for the islanded operation.

Infineon Online Power Simulation Platform (IPOSIM) is a platform for loss and thermal calculation of Infineon power modules, and discrete devices. Thus if the power semiconductor manufacturers such as Infineon also incorporate the design optimization proposed in Part I, into their online simulation software, then this would be what one calls a *transition from i3.0 to i4.0.* In particular, Infineon has a huge database of power semiconductor devices. Alternatively, any company that manufactures and sells DER Inverter can develop its database of PSD, or can make an agreement with power semiconductor manufacturers to obtain the PSD database.

7.3.2 Part II

C2000 compensation designer is one of the tools in powerSUITE, a graphical user interface-based design software of Texas Instruments. The MO-CO-DF proposed in part II of the thesis can be used to *automate* the *smart design* of controllers for the power electronic systems. Henceforth a *transition from i3.0 to i4.0* and enhancing the end-user experience by multi-fold times.

> In a gentle way, you can shake the world.
>
> — Mahatma Gandhi
> *Lawyer, Politician, Social activist, and Writer.*

Appendix A

Oceanography Data

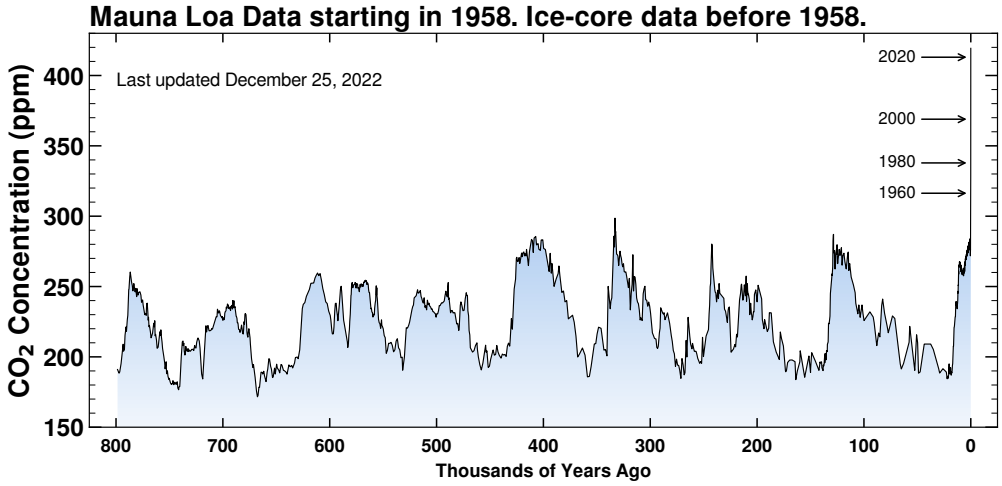

Figure A.1: CO_2 data before 1958 going back 800,000 years, © Scripps institution of oceanography at UC san diego

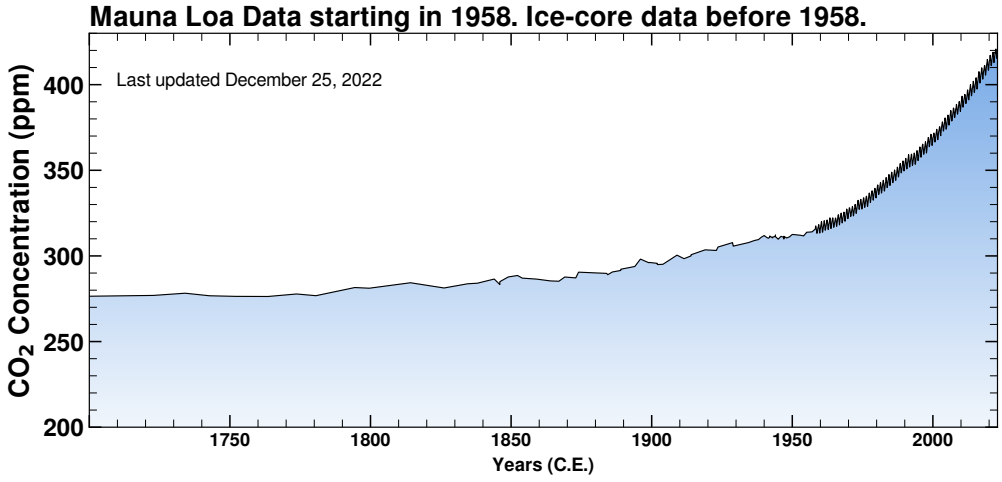

Figure A.2: CO_2 data before 1958 going back 2000 years, © Scripps institution of oceanography at UC san diego

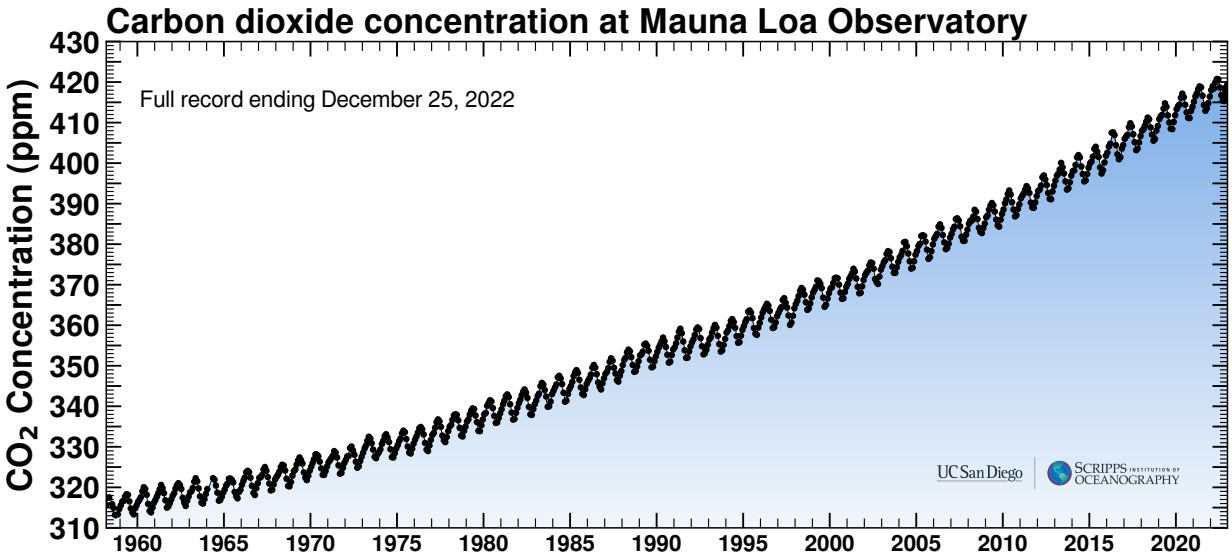

Figure A.3: Keeling curve, © Scripps Institution of Oceanography at UC San Diego

Appendix B

Photovoltaic Power Potential

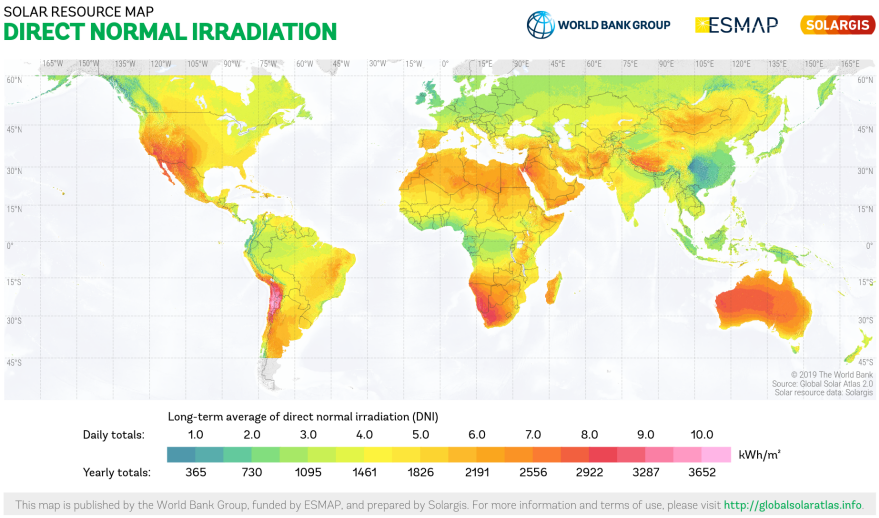

Figure B.1: Direct normal irradiation, © Solargis, Slovakia.

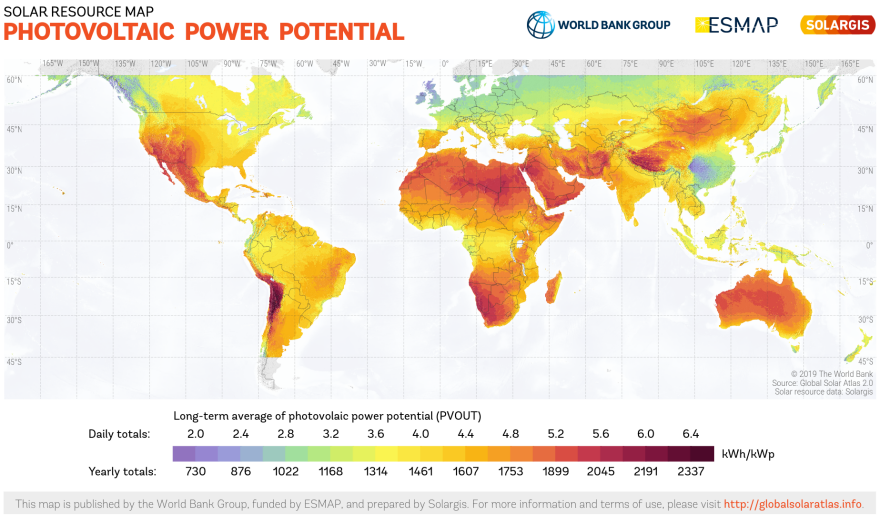

Figure B.2: Photovoltaic power potential, © Solargis, Slovakia.

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