Low-Power Class-D Amplifier for Industrial Applications

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Abstract

Low-Power Class-D Amplifier for Industrial Applications

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This dissertation investigates the design and development of fully differential switching (class-D) amplifiers optimized for high efficiency, linearity, and compact integration, tailored to low-power applications such as industrial servo valves, hall effect sensors, and low-power actuators. These loads, commonly employed in automotive and other critical power systems, require differential sine wave inputs at frequencies ranging from several kilohertz to $10\,\mathrm{kHz}$. Traditional linear amplifiers (Class A, B, and AB) are constrained by low efficiency and significant thermal management requirements, while switching amplifiers, despite their inherent efficiency advantages, pose challenges in mitigating nonlinearities and distortions.

The first major contribution is the development of a low-power Selective Harmonic Elimination Pulse-Width Modulation (SHEPWM)-based full-bridge inverter, featuring a novel FPGA hardware implementation. Unlike conventional SHEPWM systems focused on high-power, fixed-frequency applications ($50\,\mathrm{Hz}$–$60\,\mathrm{Hz}$), this work extends SHEPWM to low-power systems operating at high fundamental output frequencies ($4\,\mathrm{kHz}$–$10\,\mathrm{kHz}$). A unique FPGA-based architecture enables real-time configurability of output amplitude and frequency, offering flexibility without excessive computational or storage demands. Experimental results demonstrate harmonic elimination up to the 34^{th} order, achieving total harmonic distortion (THD) below 5.1% and efficiency improvements of up to 17.3% compared to natural PWM (NPWM). By integrating this design into a compact system-in-package (SiP) utilizing Gallium-Nitride (GaN) power transistors, the inverter minimizes the printed circuit board (PCB) footprint compared to conventional discrete implementations. This

integration offers a robust and versatile solution for next-generation low-power industry applications.

The second contribution is the design and analysis of a Double Integral Sliding Mode Control (DISMC)-based class-D amplifier. Theoretical work forms the foundation of this research, involving a rigorous analysis of reaching and stability conditions to derive optimal controller gains. The proposed controller employs a double-loop strategy that uses the integrals of inductor current and output voltage tracking errors to ensure robust tracking and stability under varying operating conditions. The theoretical findings are validated through extensive simulation and experimental studies, demonstrating the DISMC's superior disturbance rejection, enhanced transient response, and reliability compared to conventional proportional-integral (PI) controllers.

By combining innovative control techniques such as SHEPWM and DISMC with compact and efficient hardware designs, this research advances the state-of-the-art in switching amplifier technology. The outcomes offer practical solutions for compact, high-performance systems, addressing critical requirements in modern industrial applications while paving the way for future advancements in power electronics.

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Lastly, I would like to thank everyone who, in one way or another, contributed to the completion of this thesis. This milestone is not only mine but a reflection of the collective effort of those who have supported me along the way.

Dedication

I dedicate this dissertation to my parents, Omar Osman and Aynur Abdurehim, who raised me with unwavering love and support. Despite coming from a small, remote town in the far west of the Uyghur region, they encouraged me to pursue the best education possible. Their belief in me extended even further when they supported my journey to Canada to pursue my Ph.D., fully aware that it might be the last time we would see each other. I hold on to the hope that, despite the political challenges we face, I will be able to reunite with them within their lifetime.

Contents

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List of Abbreviations

3D Three-Dimensional.

AC Alternating Current.

ADC Analog-to-Digital Converter.

BOM Bill of Materials.

BRAM Block Random Access Memory.

CDA Class-D Amplifier.

CPIO Configurable Power Input/Output.

CPIOS Configurable Power Input/Output System.

DC Direct Current.

DISMC Double Integral Sliding Mode Control.

DSP Digital Signal Processing.

EMI Electromagnetic Inteference.

ESR Equivalent Series Resistance.

FET Field Effect Transistor.

FPGA Field Programmable Gate Array.

FSM Finite State Machine.

GaN Gallium-Nitride.

GD Gate Driver.

GUI Graphic User Interface.

HDL Hardware Description Language.

IC Integrated Circuit.

ISMC Integral Sliding Mode Control.

KCL Kirchhoff's Current Law.

KVL Kirchhoff's Voltage Law.

LPF Low-Pass Filter.

LSB Least-Significant Bit.

LTCC Low-Temperature Co-fired Ceramics.

LUT Look-up Table.

MCU Micro-Controller Unit.

MEMS Micro-Electro-Mechanical-System.

MI Modulation Index.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

NPWM Natural Pulse Width Modulation.

PC Personal Computer.

PCB Printed Circuit Board.

PDM Pulse Density Modulation.

PGND Power Ground.

PI Proportional-Integral.

PSRR Power Supply Rejection Ratio.

PSU Power Supply Unit.

PWM Pulse Width Modulation.

RMS Root Mean Square.

SHEPWM Selective Harmonic Eliminated Pulse Width Modulation.

SiP System-In-Package.

SMC Sliding Mode Control.

SMPS Switch Mode Power Supply.

SNR Signal-to-Noise Ratio.

SPI Serial Peripheral Interface.

SU Switching Unit.

SW Switch.

SysGen System Generator.

THD Total Harmonic Distortion.

THD+N Total Harmonic Distortion plus Noise.

UART Universal Asynchronous Receiver/Transmitter.

VHDL VHSIC Hardware Description Language.

List of Symbols

α_k	k^{th} switching angle in SHEPWM
β	Scaling factor for the output voltage
$\boldsymbol{A}$	Coefficient vector of state variables
$\boldsymbol{B}$	Coefficient vector of control law
$\boldsymbol{C}$	m-dimentional coefficient vector of switching fucntion
$\boldsymbol{x}$	State variables vector
$\Delta\alpha$	Switching angle resoultion
η	Power efficiency of the converter
$\hat{v}_{\text{car}}$	Peak amplitude of a carrier signal
ω	Angular frequency in radian/second
ω_{LC}	Cut-off frequency of LC filter in radian/second
ω_n	Natural frequency
$\triangle I_{\text{L}}$	Inductor peak-to-peak current
ζ	Damping ratio
a_0	DC component of a Fourier series
a_n	Coefficient of the n^{th} order harmonic of the cosine term in a Fourier series

b_n Coefficient of the n^{th} order harmonic of the sine term in Fourier series

C Capacitor of the output filter

$C_{\mathrm{DS-H}}$ Drain-source capacitance of a high-side transistor

$C_{\mathrm{DS-L}}$ Drain-source capacitance of a low-side transistor

$C_{\mathrm{GD-H}}$ Gate-drain capacitance of a high-side transistor

$C_{\mathrm{GD-L}}$ Gate-drain capacitance of a low-side transistor

$C_{\mathrm{GS-H}}$ Gate-source capacitance of a high-side transistor

$C_{\mathrm{GS-L}}$ Gate-source capacitance of a low-side transistor

$C_{\mathrm{OSS-H}}$ Output capacitance of a high-side transistor

$C_{\mathrm{OSS-L}}$ Output capacitance of a low-side transistor

C_{BTL} Bridge-tied capacitor

C_{bus} Bus capacitor

C_{par} Parasitic output capacitance at the switching-node

D Duty cycle

f_{CLK} Clock frequency

f_{LC} Cut-off frequency of LC filter

f_{SW} Switching frequency of the converter

f_{T} Fundamental output frequency

I_{AVERAGE} Inductor average current

$I_{\mathrm{C(RMS)}}$ Capacitor RMS current

I_{C} Capacitor current

I_{DD} Input current for a controller

I_{IN} Input current for a power stage

I_{L} Inductor current

I_{out} Output current

I_{PEAK} Inductor peak (max) current

I_{VALLEY} Inductor valley (min) current

I_{DS} Drain-source current

$I_{\mathrm{IN(AVE)}}$ Average input current of the inverter

$I_{\mathrm{OUT(RMS)}}$ RMS value of the dofferential output current signal

i_{ref} Reference current

I_m Peak amplitude of steady-state output current

I_{RR} Reverse recovery current in a diode

$K_{i\mathrm{i}}$ Integral gain of of the current control

$K_{i\mathrm{v}}$ Integral gain of of the voltage control

$K_{p\mathrm{i}}$ Proportional gain of of the current control

$K_{p\mathrm{v}}$ Proportional gain of of the voltage control

L Inductor of the output filter

M The number of modualtion index number

M_{HS} High-side power transistor

M_{LS} Low-side power transistor

N The total number of switching angle numbers in SHEPWM

n Harmonic order

N_{f} The number of fundamental output frequency

$P_{\mathrm{CAP(ESR)}}$ Conduction loss in a capacitor

P_{COSS} Output capacitance loss in the MOSFET

P_{ctrl} Controller operation loss

P_{D} Dead-time loss

P_{G} Gate charge loss

$P_{\mathrm{L(DCR)}}$ Conduction loss in an inductor

$P_{\mathrm{ON-H}}$ Conduction loss for high-side transistor

$P_{\mathrm{ON-L}}$ Conduction loss for low-side transistor

$P_{\mathrm{SW-H}}$ Switching loss for high-side transistor

$P_{\mathrm{SW-L}}$ Switching loss for low-side transistor

P_{DIODE} Reverse recovery loss in a diode

R Load resistor

R_{DCR} DC resistance of an inductor

R_{ESR} Equivalent series resistance of a capacitor

$R_{\mathrm{ON-H}}$ Turn-on resistance of a high-side transistor

$R_{\mathrm{ON-L}}$ Turn-on resistance of a low-side transistor

R_{BTL} Bridge-tied load

$R_{\mathrm{DS(ON)}}$ Drain-source turn on resistance of a transistor

R_{PATH} Path resistance from converter input supply to output node

S	Sliding surface
$s(x)$	Switching function of state variables
T	Fundamental period of sinewave output signal
t	Time
t_{Df}	Dead-time in falling
t_{Dr}	Dead-time in rising
$t_{\mathrm{f-H}}$	Fall time of a high-side transistor
$t_{\mathrm{f-L}}$	Fall time of a low-side transistor
t_{OFF}	Transistor turn-off time
t_{ON}	Transistor turn-on time
$t_{\mathrm{r-H}}$	Rise time of a high-side transistor
$t_{\mathrm{r-L}}$	Rise time of a low-side transistor
t_{d}	Dead-time
T_s	Sampling period
t_{RR}	Reverse recovery time in a diode
u	Control law
u_{eq}	Equivalent control law
V_{DD}	Input supply voltage for the controller and/or gate driver
V_{D}	Body-diode voltage of a power transistor
v_{C}	Capacitor voltage
V_{DS}	Drain-source voltage

V_{HS} Gate voltage of high-side transistor

V_{IN} Input supply voltage to a power stage

V_{LS} Gate voltage of low-side transistor

V_{L} Inductor voltage

$V_{\text{OUT(RMS)}}$ RMS value of the differential output voltage signal

V_{PWM} PWM input signal of a gate driver

V_{ref} Reference voltage

V_{signal} Input signal of an amplifier

V_{SW} Switching node voltage

v_c Control signal

V_m Peak amplitude of steady-state output voltage

Chapter 1

Introduction

Low-power loads, such as industrial servo valves, hall effect sensors, and low-power actuators, often operate using a differential output sine wave, and are commonly used in industries such as automotive and other critical power systems. The typical operating frequency of these loads ranges from several kHz to $10\,\mathrm{kHz}$. The choice of amplifier architecture plays a critical role in achieving both high efficiency and linearity. Traditional amplifiers, such as Class A, B, and AB, suffer from limited efficiency, requiring bulky heat sinks that increase the size and weight of the overall power delivery system.

Switching amplifiers, by contrast, offer significantly higher efficiency, eliminating the need for large heat sinks and relaxing thermal design constraints. However, their inherently nonlinear operation, caused by the switching of power transistors between on and off states, introduces unwanted distortions at the amplifier output if not carefully designed. Although switching amplifiers are more efficient than their linear counterparts, this does not guarantee consistently high efficiency across all operating ranges. Switching losses are intrinsic to these amplifiers, and a trade-off must be made between switching and conduction losses.

Digital control of switching amplifiers benefits from process scaling and the ease of configurability, whereas analog circuits are limited by reduced supply voltages and decreased linearity. However, since the loads are inherently analog, there is still a need for sensing amplifiers, signal conditioning, and the conversion of analog signals into the digital domain. Integrating both the

power stage and readback circuitry can occupy significant board space, leading to increased system size and cost.

In this research, we focus on designing fully differential switching amplifiers that deliver high efficiency to the load while improving linearity and accuracy, all within a compact board size. Gallium-Nitride (GaN) power transistors are employed in the power stage due to their small footprint and fast switching capabilities. Two control and modulation techniques are explored: Selective Harmonic Eliminated Pulse Width Modulation (SHEPWM), aimed at reducing the switching activity of the power transistors to achieve superior efficiency in low-power operating ranges, and Double Integral Sliding Mode Control (DISMC), known for its robustness and high accuracy, utilizing a double-loop control strategy. The goal is to achieve superior performance in both efficiency and linearity, while also minimizing the overall system size through the integration of power stages and readback circuitry into a system-in-package (SiP). Furthermore, the digital control is implemented on an Field Programmable Gate Array (FPGA) platform, offering versatility by allowing easy adjustments to control parameters. This flexibility enables fine-tuning of the system to achieve optimal performance under varying operating conditions, making it adaptable to different application requirements.

1.1 Motivation

Recent advances in microelectronic fabrication have enabled the development of smaller and lighter power electronics boards. However, reducing system volume and replacing bulky power electronic components with reconfigurable units is essential to further minimize overall size and effectively distribute power to various loads operating under different conditions. In automotive and other industrial applications where safety is critical, designing redundancy is crucial to ensure continuous operation despite potential component failures. Such a system can be described as a Configurable Power Input/Output System (CPIOS), as illustrated in Figure 1.1. The main components of the CPIOS include:

1. An array of Configurable Power Input/Output (CPIO) units, which can be integrated into a SiP to reduce size and weight.

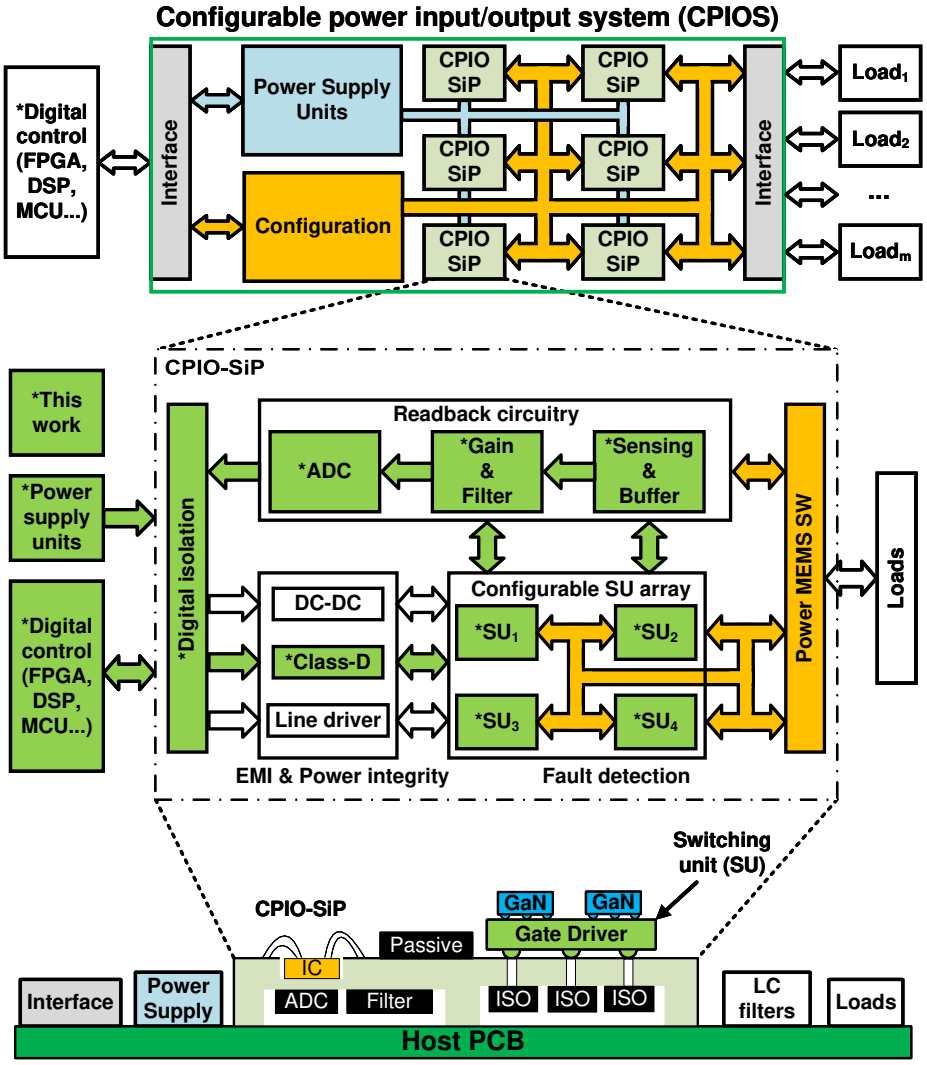


Figure 1.1: The block diagram of CPIOS

2. Power Supply Units (PSUs) that regulate the power of the CPIO-SiP.

3. A configuration system that interconnects the CPIO-SiP units, determining which units operate and replacing any that fail.

4. An interface to a digital control unit such as a FPGA, Digital Signal Processing (DSP) board, or Micro-Controller Unit (MCU), which controls the system.

5. An interface to the load, connecting the CPIO-SiP array to various loads.

With such a CPIOS system, different power topologies such as Direct Current (DC)-DC buck-boost converters, Class-D Amplifiers (CDAs), and line drivers within CPIO can be controlled with a digital control unit to drive different loads. Additionally, redundancy of the CPIO-SiP is ensured, allowing for control and configuration to decide which unit to operate and to replace any failed CPIO system, thus ensuring continued operation of the CPIOS.

The major component of the CPIOS is the CPIO design. The CPIO consists of:

1. Configurable Switching Units (SUs) array. Each SU includes a gate driver and power devices such as GaN. Given that the SU is the most critical part, it is essential to design for redundancy and ensure continuous operation of the system.

2. Readback circuitry, which includes sensing and buffer circuits, filters to remove high-frequency noise and provide gain for the desired signal, and Analog-to-Digital Converters (ADCs) to convert the measured output signals to digital signals.

3. Digital isolation, which isolates the FPGA from the entire CPIO system.

4. Power Micro-Electro-Mechanical-System (MEMS) Switchs (SWs), which serve as the configuration interface between the SUs and the loads. The continuous operation of the system is achieved by the MEMS SWs in case of failures in the critical SUs.

5. Other components specific to different control systems, such as DC-DC converters, CDAs, and line drivers.

6. A fault detection system, which performs early diagnostic detection of system failures or aging components to enable early failure detection.

7. Research on Electromagnetic Inteference (EMI) and power integrity among the subsystems, aiming to reduce interferences between subsystems, such as noisy high-power SUs and other sensitive low-power analog circuits in the readback subsystem. This also ensures efficient power delivery from the source to the destination, maintaining the power integrity of the system.

1.2 Focus of This Work

This work focuses on elaborating the methods and techniques for designing the CPIO. The research primarily investigates the design of the SUs, readback circuits, and control algorithms. The CPIO can be integrated into a SiP to reduce the footprint size and weight of the electronic board. However, this integration largely depends on the current available SiP technology and the selection of components to be integrated. In terms of electronic design, the major components of the CPIO remain largely unchanged.

To deliver efficient power to the load, Switch Mode Power Supplies (SMPS) are advantageous due to their highly efficient operation and the elimination of heat sinks compared to class-A, B, and AB amplifiers. This enables the reduction of the PCB area and thermal budget of the electronic system. CDAs are a type of SMPS that can deliver arbitrary voltage/current waveforms to the load, unlike DC-DC converters which regulate the output voltage/current to a constant value. In this work, most of the loads require a sine wave output voltage/current, while a few require a DC output. The CDA in a full-bridge topology is chosen to deliver differential output voltages/currents efficiently to the load.

This work is a collaboration between researchers in different fields to achieve the final goal of CPIOS. The research areas in this work include the blocks of SU, sensing and buffer circuits, gain and filter stages, ADCs, digital isolation, and control algorithms for the CDA, which are highlighted with an asterisk (*) in Figure 1.1.

The differential output power delivered from the CDA is primarily intended for low-power loads. The major power-consuming blocks in the CPIO are the SUs, or power stages. For low output power, switching losses in power stages dominate over conduction losses. Therefore, one of the challenges of this research is to decrease the switching frequency of the CDA without sacrificing THD. To address this, the SHEPWM technique is investigated in this work. SHEPWM is particularly attractive because it significantly reduces the switching frequency of Pulse Width Modulation (PWM) while canceling lower-order harmonics, thereby improving efficiency. This makes SHEPWM an ideal choice for applications requiring high efficiency and low harmonic distortion, aligning with the objectives of this research.

In addition to SHEPWM, this work explores the application of Sliding Mode Control (SMC) to address the challenges associated with precise control of the CDA. The gain of a CDA is directly influenced by the input supply voltage, which can degrade output accuracy in the presence of ripples or noise. Traditional feedback mechanisms typically compensate after the power stage for simplicity, but this research investigates feedback after the LC filter to directly improve the accuracy of the output voltage/current at the load. SMC is particularly well-suited for this purpose due to its robustness against parameter variations and external disturbances. By leveraging SMC, this work aims to enhance the load/line regulation, achieve precise regulation of output voltage/current, and ensure stable operation under varying conditions. Together, these attributes make SMC a powerful tool for improving the performance and reliability of the CDA.

1.2.1 Problem Statement

Efficiently delivering differential output power to low-power loads using CDA presents several challenges, particularly in applications requiring high efficiency, low distortion, and compact design. Unlike high-power electronics, low-power systems demand innovative solutions to address issues such as switching losses, dynamic load conditions, and precise control of output voltage/current. Furthermore, the integration of advanced control techniques, such as SHEPWM and SMC, into low-power CDA design introduces additional complexities.

The key challenges identified in this research are as follows:

- **P1**: Existing implementations of SHEPWM are primarily designed for high-power electronics, characterized by fixed filter sizes, fixed output frequencies, and minimal load variation. A detailed review of these implementations is provided in Section 2.4. However, adapting SHEPWM for low-power applications with diverse operating conditions and dynamic load variations remains an unexplored research area.

- **P2**: Minimizing the PCB footprint size is critical for low-power systems. Power stages and digital isolators occupy significant board area, necessitating exploration of new SiP technologies to integrate these components and reduce the overall footprint.

- **P3**: Discrete implementation of DISMC for CDA applications remains largely unexplored.

Challenges such as phase delay introduced by the LC filter and the high-frequency switching dynamics need to be addressed.

- **P4**: While double-loop DISMC has been successfully implemented in DC-DC converters, its application to CDA systems is complicated by the time-varying nature of the reference signal. Stability analysis for such systems remains an open research problem.

By addressing these challenges, this research aims to advance the design of CDA systems for low-power applications, leveraging the unique capabilities of SHEPWM and SMC to achieve high efficiency, precise control, and compact integration.

1.2.2 Research Objectives

The primary objective of this research is to design a full-bridge CDA that efficiently delivers differential output power to the load while addressing the identified challenges. This involves tailoring advanced techniques such as SHEPWM and SMC to meet the unique requirements of low-power applications.

To address the challenges outlined in Section 1.2.1, the following specific research objectives are defined:

- **O1**: Investigate and adapt the SHEPWM technique to reduce the switching frequency of the CDA without compromising THD for low-power applications. Develop a unique FPGA-based architecture to implement SHEPWM, enabling on-the-fly configuration of inverter outputs to dynamically adjust to varying load conditions. (Addresses problem statement **P1**)

- **O2**: Develop a tailored SHEPWM approach to accommodate a wide range of operation and variable load conditions in low-power systems. Simultaneously, explore a new SiP technologies to minimize the PCB footprint by integrating power stages and digital isolators, thereby reducing the overall size of the CDA. (Addresses problem statement **P2**)

- **O3**: Conduct an in-depth investigation into the development of a discrete DISMC framework for CDA systems. This research aims to address the fundamental challenges posed by phase

delays inherent in the system dynamics, ensuring robust and precise control under varying operational conditions. (Addresses problem statement **P3**)

- **O4**: Explore the application of double-loop DISMC to CDA systems, considering the time-varying nature of the reference signal, and perform stability analysis to ensure reliable operation. (Addresses problem statement **P4**)

By achieving these objectives, this research aims to advance the state of the art in low-power CDA design, enabling high efficiency, precise control, and compact integration.

1.3 Fundamentals of Class-D Amplifiers

CDAs, first introduced in 1958, have seen a significant rise in popularity in recent years Gaalaas (2006). Also known as switching amplifiers or digital amplifiers, CDAs represent a notable advancement in amplifier technology, particularly due to their high efficiency and compact design. Unlike traditional linear amplifiers (class A, B, and AB), which operate transistors in their linear region and consequently suffer from substantial power losses and heat dissipation, CDAs use a different approach to amplification. Even a well-designed class AB amplifier experiences significant power dissipation because its midrange output voltages are generally far from either the positive or negative supply rails. This results in large drain-source voltage drops, producing substantial instantaneous power dissipation.

In contrast, CDAs employ a topology that significantly reduces power dissipation. Figure 1.2 illustrates the basic CDA open-loop block diagram. The input signal (V_{signal}) is modulated to generate small voltage pulses (V_{PWM}). Among various modulation techniques, PWM is the most common. The output power stage of a class-D amplifier switches between the positive ($+V_{\text{IN}}$) and negative ($-V_{\text{IN}}$) power supplies to produce a train of large voltage pulses at the switching node, V_{SW}. This power stage, also known as a half-bridge, contains two output transistors: a high-side transistor (M_{HS}) and a low-side transistor (M_{LS}).

The PWM signal (V_{PWM}) cannot directly drive the half-bridge power transistors due to their large size. Therefore, a gate driver circuit is typically used to drive the gate terminals of the power

transistors. The gate voltages (V_{HS} and V_{LS}) for the high-side and low-side power transistors are turned on in a complementary manner to avoid cross-conduction, a function usually managed by the gate driver. Sometimes, the controller generates complementary PWM signals if the gate driver lacks a dead-time generation block.

This switching mechanism is efficient because the output transistors carry zero current when not switching and maintain a low drain-source voltage (V_{DS}) when conducting current. As a result, the product of current (I_{DS}) and voltage (V_{DS}) is minimized, leading to significantly lower power dissipation compared to linear amplifiers. By driving the transistors either fully on or fully off, CDAs minimize the time spent in high-power dissipation states, thereby achieving greater efficiency.

The amplified switching node voltage (V_{SW}) is then filtered by an LC filter to reconstruct the original input signal (V_{signal}). The LC filter effectively removes the high-frequency switching components, allowing the desired low-frequency signal to pass through, thereby recreating a clean and amplified version of the original input signal at the output.

The primary advantage of CDAs is their high efficiency, which results in significantly lower power and heat dissipation compared to other amplifier classes. Consequently, the heat sinks typically required for other amplifiers can be greatly reduced or even eliminated. However, one drawback of CDAs is that their output signal is a square wave at full power, which must be filtered before being applied to the load. This necessitates the use of an LC filter, which occupies Printed Circuit Board (PCB) space and increases the Bill of Materials (BOM). Additionally, CDAs generate switching noise due to the rapid switching of power transistors and the presence of parasitic inductances and capacitances. This noise can increase EMI radiation and degrade the power integrity of other sensitive analog circuits.

For PWM, the two popular modulation schemes are AD and BD modulation, where D stands for Class-D, and A and B denote the order in which they were invented. Figures 1.3a and 1.3b show how the H-bridge operates with an AD modulation scheme, which essentially has two states. The high-side and low-side transistors in each half-bridge are switched alternately. When the high-side transistor is ON, the low-side is OFF, and vice versa. The switching node voltage V_{SW2} is a complement of V_{SW1}. The differential switching node voltage produces a two-level switching waveform as shown in Figure 1.4a.

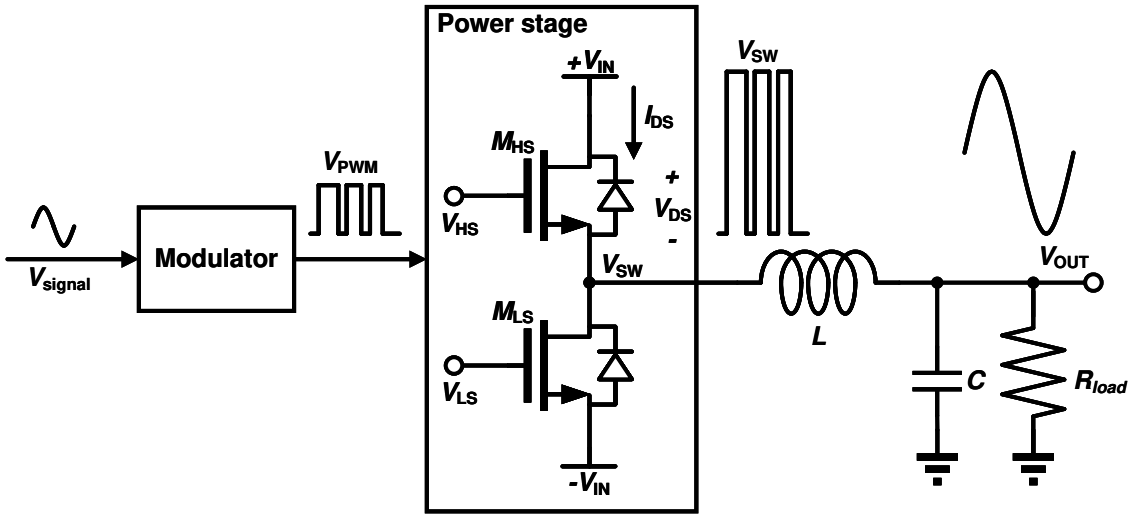
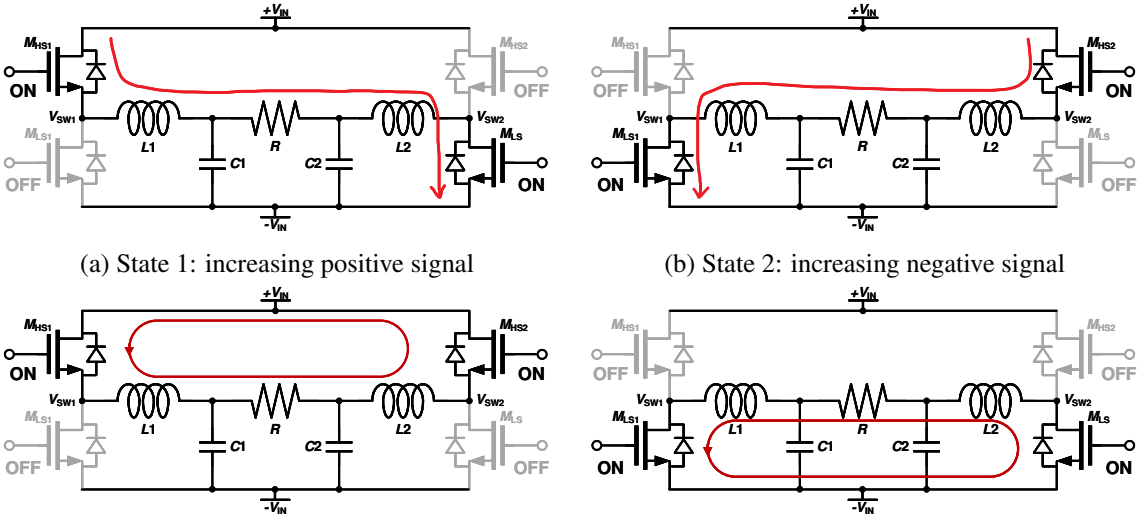


Figure 1.2: class-D amplifier open-loop block diagram

In BD modulation, there are four states as shown in Figure 1 (a), (b), (c), and (d) depending on the input signal conditions: increasing positive signal, increasing negative signal, decreasing positive signal, and decreasingly negative signal. The differential switching node voltage produces a three-level switching waveform as shown in Figure 1.4b. Both half-bridges operate in a complementary fashion, which helps to balance the output and reduce common-mode noise. By using complementary signals, BD modulation minimizes the EMI and improves overall noise performance.



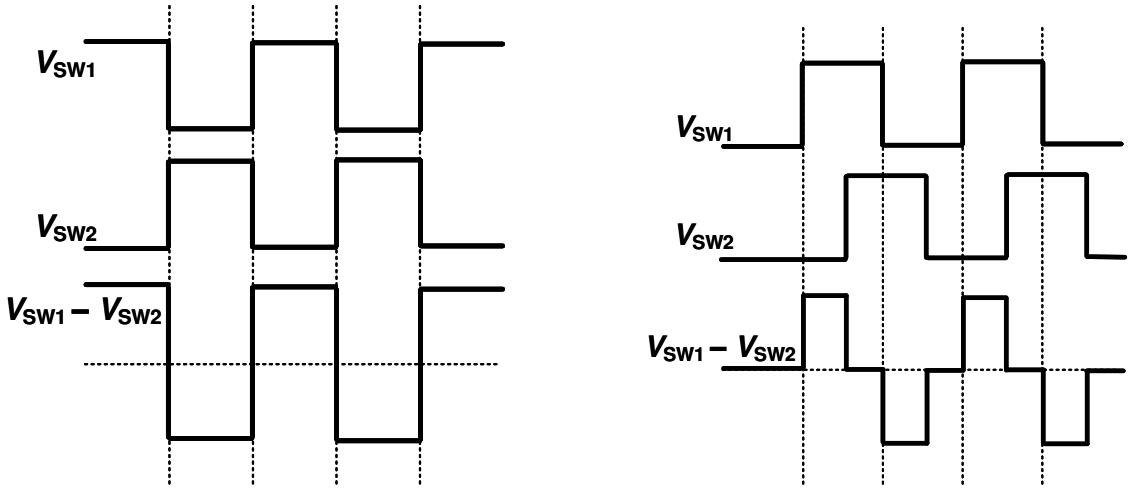
(a) State 1: increasing positive signal

(b) State 2: increasing negative signal

(c) State 3: decreasing positive signal

(d) State 4: decreasing negative signal

Figure 1.3: Full-bridge output stage operation



(a) AD modulation (b) BD modulation

Figure 1.4: Full-bridge switching waveform

Class-D modulators can be implemented in various ways. Here we introduces some fundamental concepts. The most common modulation technique is PWM. In PWM, the input signal is compared to a triangular or ramp waveform running at a fixed carrier frequency, generating a stream of pulses at the carrier frequency. Within each carrier period, the duty cycle of the PWM pulse is proportional to the amplitude of the input signal.

Another modulation technique is Pulse Density Modulation (PDM), where the number of pulses in a given time window is proportional to the average value of the input signal. Unlike PWM, PDM has ”quantized” pulse widths that are multiples of the modulator clock period. One-bit sigma-delta modulation is a form of PDM. Sigma-delta modulation spreads high-frequency energy over a wide range of frequencies rather than concentrating it at multiples of a carrier frequency as PWM does. This distribution can offer an EMI advantage.

Recently, self-oscillating amplifiers have been developed. These amplifiers include a feedback loop that determines the switching frequency of the modulator, rather than relying on an external clock. High-frequency energy in self-oscillating amplifiers is often more evenly distributed than in PWM. The feedback loop enables excellent performance, but because the loop is self-oscillating, it is challenging to synchronize with other switching circuits or connect to digital sources without first converting the digital signal to analog.

To effectively compare the performance of the CDA, it is crucial to understand its performance

metrics. These metrics can be categorized into three main groups: time domain measurements, frequency domain measurements, and power measurements.

1. Time Domain Measurements: These include both steady-state operation and dynamic performance. Dynamic performance encompasses line and load transitions, as well as the quantified ability for line and load regulation.

2. Frequency Domain Measurements: This category includes THD, Total Harmonic Distortion plus Noise (THD+N), Signal-to-Noise Ratio (SNR), and PSRR.

3. Power Measurements: The primary metric in this group is power efficiency.

Each of these metrics provides valuable insights into the performance and suitability of a CDA for various applications.

1.4 Thesis Outline and Publications

The first chapter of this thesis provides the motivation, scope, and objectives of the research. Additionally, this chapter introduces the fundamental concepts of CDA operation, offering a foundation for understanding the advanced techniques discussed in subsequent chapters.

Chapter 2 presents a comprehensive review of the existing literature related to CDAs, focusing on several key areas. In Section 2.1, the various sources of power dissipation in CDAs are reviewed, highlighting their impact on efficiency. The CDA architectures and modulation techniques discussed in the literature are reviewed in Section 2.2. Section 2.3 provides the necessary background information on the SHEPWM technique, followed by a review of the latest advancements and current state of the art in SHEPWM techniques in Section 2.4. Section 2.5 presents the fundamental principles of SMC, providing the necessary background for its application in CDAs. Section 2.6 reviews research and developments in SMC techniques, focusing on their implementation in power electronics.

Chapter 3 details the design, simulation, and experimental results of the SHEPWM inverter. Section 3.1 describes the design methodology and implementation of the SHEPWM inverter. The simulation and experimental results are presented and discussed in Section 3.2, providing a thorough

analysis of the inverter's performance. The chapter concludes with Section 3.3, which summarizes the findings and offers recommendations for improvement. This chapter led to one conference paper and one journal paper as the first author, along with two conference papers as the second author. The key contributions of this chapter include bridging the gap in utilizing the SHEPWM technique, which has primarily been applied in high-power grid applications, to its implementation in a low-power inverter where higher frequencies can also be employed with high efficiency. Furthermore, the on-the-fly configuration of the SHEPWM inverter output is achievable with the unique SHEPWM architecture introduced in this chapter. Additionally, the SHEPWM inverter is implemented in a compact 3-D LTCC SiP technology, demonstrating that size reduction compared to traditional boards is feasible.

Chapter 4 focuses on the design and evaluation of the DISMC for CDAs. Section 4.1 explains the design approach and methodology used to implement the DISMC. The performance of the DISMC CDA is evaluated through simulation and experimental results in Section 4.2, followed by a detailed discussion. The chapter concludes with Section 4.3, providing a summary of the findings and their implications for future research. This chapter led to one conference paper and is expected to result in one journal paper. The key contributions of this chapter include not only the theoretical contribution of defining the stability condition and determining the controller gain but also the experimental demonstration that DISMC can be implemented in CDA, where the reference signal is time-varying, complicating the stability analysis of the controller compared to DC-DC converters, where the reference is constant. Furthermore, it shows that DISMC outperforms traditional proportional-integral (PI) controllers in terms of handling large signal variations, such as line and load regulations.

The final chapter, Chapter 5, provides a comprehensive summary of the research conducted, highlighting key contributions and findings. It includes recommendations for future work and potential areas for further investigation.

The papers are listed below in chronological order.

- N. Ly, **N. Aimaier**, A. H. Alameh, Y. Blaquière, G. Cowan, and N. G. Constantin, "A High Voltage Multi-Purpose On-the-fly Reconfigurable Half-Bridge Gate Driver for GaN

HEMTs in 0.18-μm HV SOI CMOS Technology," *2020 18th IEEE International New Circuits and Systems Conference (NEWCAS)*, Montreal, QC, Canada, 2020, pp. 178–181, doi: 10.1109/NEWCAS49341.2020.9159781.

- **N. Aimaier**, N. Ly, G. Nobert, Y. Blaquière, N. Constantin, and G. Cowan, "SHEPWM Class-D Amplifier with a Reconfigurable Gate Driver Integrated Circuit," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021, pp. 1–5, doi: 10.1109/ISCAS51556.2021.9401689.

- V. H. Nguyen, **N. Aimaier**, *et al.*, "A Reconfigurable Power System-in-Package Module using GaN HEMTs and IC Bare Dies on LTCC Substrate: Design - Implementation - Experiment and Future Directions," *2022 20th IEEE International New Circuits and Systems Conference (NEWCAS)*, Quebec City, QC, Canada, 2022, pp. 188–192, doi: 10.1109/NEWCAS52662.2022.9842234.

- **N. Aimaier**, N. Constantin, and G. Cowan, "A Pulsewidth Modulation Based Double Integral Sliding Mode Controller for Class-D Amplifiers," *2023 IEEE 14th International Conference on Power Electronics and Drive Systems (PEDS)*, Montreal, QC, Canada, 2023, pp. 1–5, doi: 10.1109/PEDS57185.2023.10246506.

- **N. Aimaier**, Y. Blaquière, N. G. Constantin, and G. E. R. Cowan, "An FPGA-Based On-the-Fly Reconfigurable Low-Power SHEPWM Inverter With a Compact SiP Implementation," *IEEE Transactions on Power Electronics*, vol. 39, no. 5, pp. 5942–5953, May 2024, doi: 10.1109/TPEL.2024.3364534.

- **N. Aimaier**, Y. Blaquière, N. G. Constantin and G. E. R. Cowan, "A PWM-Based Discrete Double Integral Sliding Mode Current Controller Design for a Class-D Amplifier," submitted to *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

Chapter 2

Literature Review

In this chapter, a review of the most recent literature has been conducted. Given the focus on designing a low-power full-bridge CDA, it is imperative to delve into the mechanisms responsible for power losses within the CDA. Section 2.1 thoroughly examines all power losses within the CDA. An overview of CDA architectures and their implementations, along with a brief description of existing modulation techniques, is provided in Section 2.2. Subsequently, in Section 2.3, the chapter delves into the background of SHEPWM, which plays a crucial role in reducing switching losses. Then, the current state-of-the-art SHEPWM techniques are reviewed. Additionally, the background of a robust non-linear controller with a feedback loop, specifically SMC, is discussed in Section 2.5, with an emphasis on its current advancements and different derivatives in the realm of converters. Finally, Section 2.6 offers insights into the state-of-the-art techniques employed in power converters, including SMPS and CDA fields.

2.1 Class-D Amplifier (CDA) Power Dissipation Sources

In this section, a power loss estimation for the half-bridge converter is reviewed. Figure 2.1 depicts the circuit diagram of a half-bridge CDA, including parasitic capacitances and resistors. The switching node voltage and inductor current waveform are given in Figure 2.2.

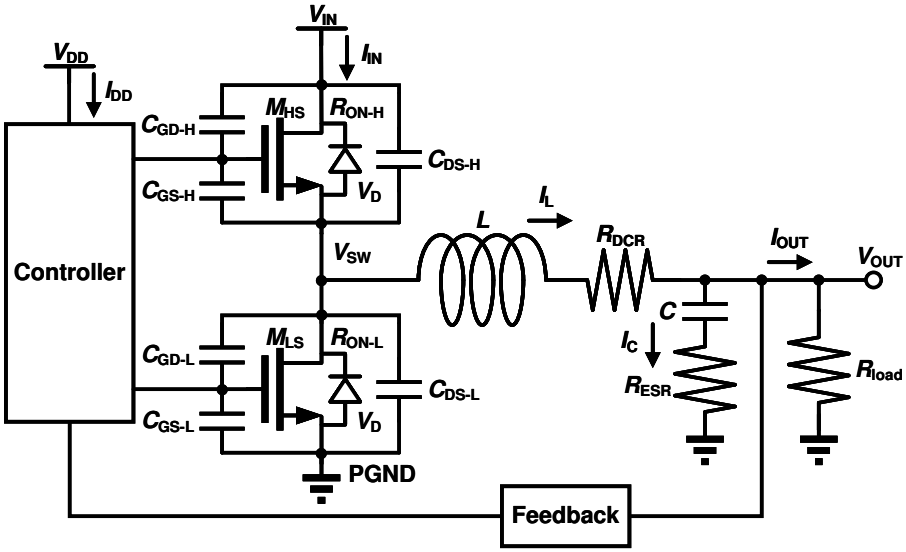


Figure 2.1: Circuit diagram of the half-bridge class-D amplifier for power loss analysis.

The calculation of power loss for the half-bridge CDA is as follows:

- Conduction loss:

$$\text{①}\ P_{\mathrm{ON-H}} = I_{\mathrm{OUT}}^2 \times R_{\mathrm{ON-H}} \times D \tag{1}$$

$$\text{②}\ P_{\mathrm{ON-L}} = I_{\mathrm{OUT}}^2 \times R_{\mathrm{ON-H}} \times (1-D) \tag{2}$$

where I_{OUT} is the output current, $R_{\mathrm{ON-H}}$ and $R_{\mathrm{ON-L}}$ are the turn-on resistance of a high-side and low-side transistors, D represents the duty cycle, denoting the duration of the high-side power Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) turn-on time, while $(1-D)$ corresponds to the turn-off time.

- Switching loss:

$$\text{③④}\ P_{\mathrm{SW-H}} = \frac{1}{2} \times V_{\mathrm{IN}} \times I_{\mathrm{OUT}} \times (t_{\mathrm{r-H}} + t_{\mathrm{f-H}}) \times f_{\mathrm{SW}} \tag{3}$$

$$\text{⑤⑥}\ P_{\mathrm{SW-L}} = \frac{1}{2} \times V_{\mathrm{D}} \times I_{\mathrm{OUT}} \times (t_{\mathrm{r-L}} + t_{\mathrm{f-L}}) \times f_{\mathrm{SW}} \tag{4}$$

where $t_{\mathrm{r-H}}$ and $t_{\mathrm{f-H}}$ are the rise and fall time of the high-side transistor, f_{SW} is the switching

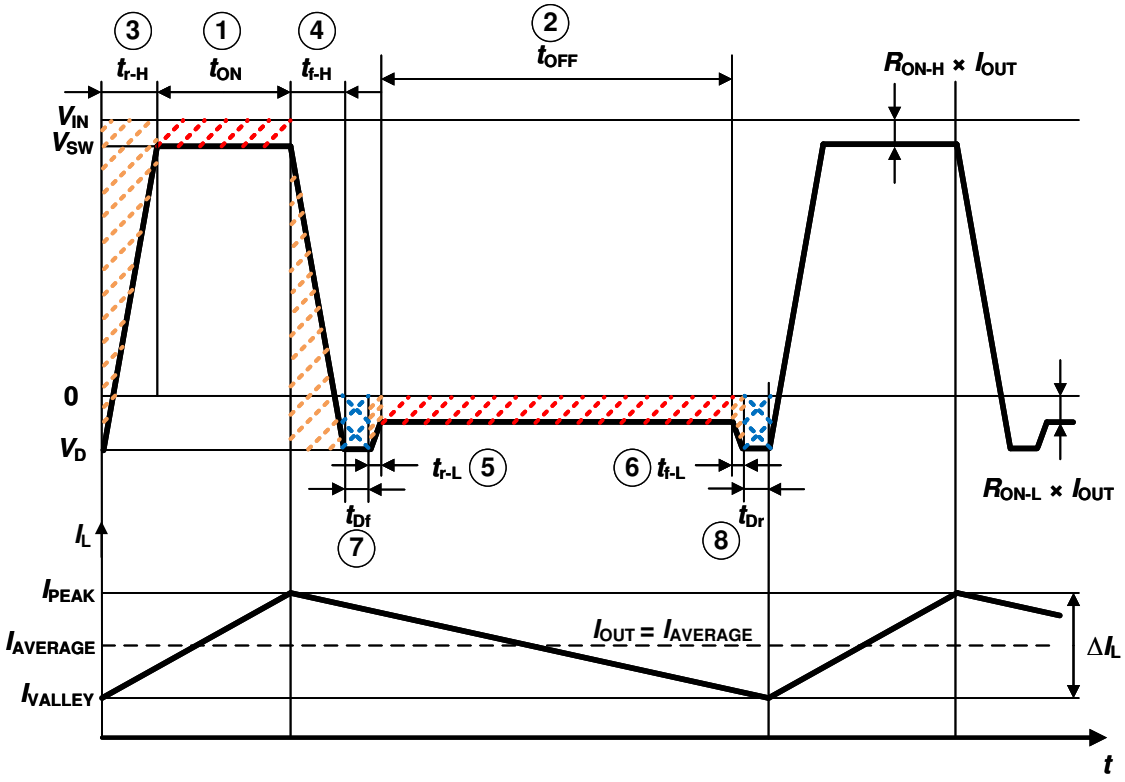


Figure 2.2: The diagram of switching node voltage and inductor current waveform and power loss.

frequency of the converter, V_{D} is the voltage drop of the body diode, $t_{\mathrm{r-L}}$ and $t_{\mathrm{f-L}}$ are the rise and fall time of the low-side transistor.

- Dead-time loss:

$$⑦⑧\ P_{\mathrm{D}} = V_{\mathrm{D}} \times I_{\mathrm{OUT}} \times (t_{\mathrm{Dr}} + t_{\mathrm{Df}}) \times f_{\mathrm{SW}} \tag{5}$$

where t_{Dr} and t_{Df} are the dead-time in rising and falling.

- Controller operation loss:

$$P_{\mathrm{ctrl}} = V_{\mathrm{DD}} \times I_{\mathrm{DD}} \tag{6}$$

where V_{DD} and I_{DD} are the controller operating voltage and current.

- Gate charge loss:

$$P_{\mathrm{G}} = (C_{\mathrm{GS-H}} + C_{\mathrm{GS-L}}) \times V_{\mathrm{DD}}^2 \times f_{\mathrm{SW}} \tag{7}$$

where $C_{\mathrm{GS-H}}$ and $C_{\mathrm{GS-L}}$ are the gate-source capacitance of the high and low side transistors.

- Output capacitance loss in the MOSFET:

$$P_{\mathrm{COSS}} = \frac{1}{2} \times (C_{\mathrm{OSS-H}} + C_{\mathrm{OSS-L}}) \times V_{\mathrm{IN}}^2 \times f_{\mathrm{SW}} \tag{8}$$

where

$$C_{\mathrm{OSS-H}} = C_{\mathrm{DS-H}} + C_{\mathrm{GD-H}} \tag{9}$$

$$C_{\mathrm{OSS-L}} = C_{\mathrm{DS-L}} + C_{\mathrm{GD-L}} \tag{10}$$

where $C_{\mathrm{DS-H}}$ and $C_{\mathrm{DS-L}}$ are the drain-source capacitance of the high and low side transistors, $C_{\mathrm{GD-H}}$ and $C_{\mathrm{GD-L}}$ are the gate-drain capacitance of the high and low side transistors.

- Conduction loss in inductor:

$$P_{\mathrm{L(DCR)}} = I_{\mathrm{OUT}}^2 \times R_{\mathrm{DCR}} \tag{11}$$

where R_{DCR} is the DC resistance of the inductor.

- Conduction loss in capacitor:

$$P_{\mathrm{CAP(ESR)}} = I_{\mathrm{C(RMS)}}^2 \times R_{\mathrm{ESR}} \tag{12}$$

where $I_{\mathrm{C(RMS)}}$ is the capacitor Root Mean Square (RMS) current, R_{ESR} is the Equivalent Series Resistance (ESR) of the capacitor.

- Reverse recovery loss:

$$P_{\mathrm{DIODE}} = \frac{1}{2} \times V_{\mathrm{IN}} \times I_{\mathrm{RR}} \times t_{\mathrm{RR}} \times f_{\mathrm{SW}} \tag{13}$$

where I_{RR} is the peak value of body-diode reverse recovery current, and t_{RR} is the body-diode reverse recovery time.

Additionally, it's worth noting that power losses arising from factors such as ripple current in the inductor and magnetic core losses are also present. However, these losses, while related to switching frequency, are of relatively minor significance and have been excluded from the discussion due to their negligible impact on the overall assessment.

In a half-bridge CDA, the total power loss is the sum of all the aforementioned losses. Among these, conduction loss and switching loss of the power transistors are predominant. Typically, losses proportional to the output current I_{OUT} are categorized as conduction losses, while losses proportional to the switching frequency f_{SW} are categorized as switching losses. From the above power loss equations, in low-power CDA designs where the output current is small, switching losses dominate over conduction losses. Therefore, it is crucial to reduce the switching frequency of the CDA. However, this reduction compromises the THD.

In contrast, when increasing the output power, conduction losses start to rise and eventually surpass switching losses. In this scenario, increasing the switching frequency becomes desirable to achieve better THD. As the output current increases, so does the power delivered to the load. Consequently, the efficiency of the CDA can remain high since the turn-on resistance and other parasitic resistances from the input voltage to the output voltage path are relatively small.

It is worth noting that in the full-bridge topology, the inductor current flows both into and out of one side of the half-bridge. When the inductor current flows out of the half-bridge, the switching mechanism is hard-switching, where the switching node voltage V_{SW} is solely pulled up by turning on the high-side power transistor, consuming power. However, when the inductor current flows into the half-bridge, as shown in Figure 2.3, it contributes partially to the rise of V_{SW} during the dead-time (t_{d}) by charging the parasitic output capacitance (C_{par}) in the switching node before the high-side transistor turns on. During this period (from t_0 to t_1 in the figure), no power is consumed. Once the dead-time is over, the rest of the rise in V_{SW} (from t_1 to t_2) is contributed by turning on the high-side power transistor, which is faster but also consumes power.

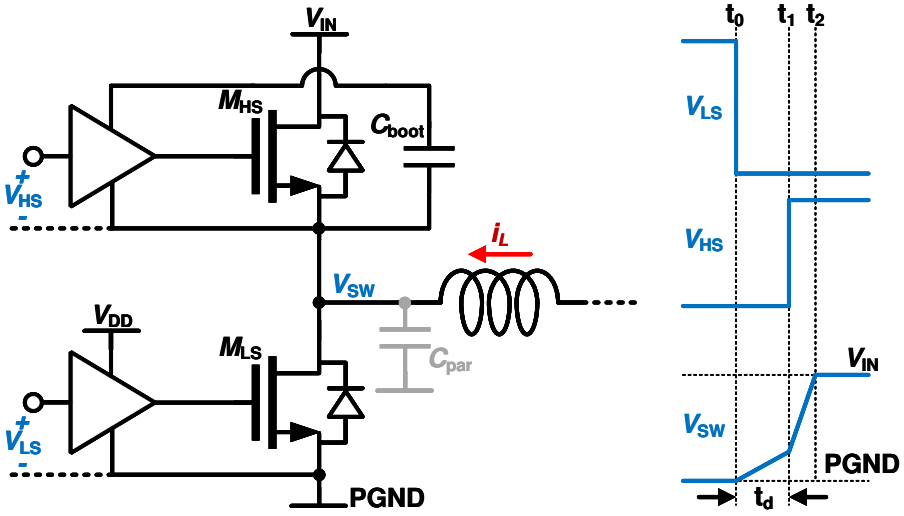


Figure 2.3: Timing diagram of switching waveform when indcutor current flows into a half-bridge (Ma et al. (2015))

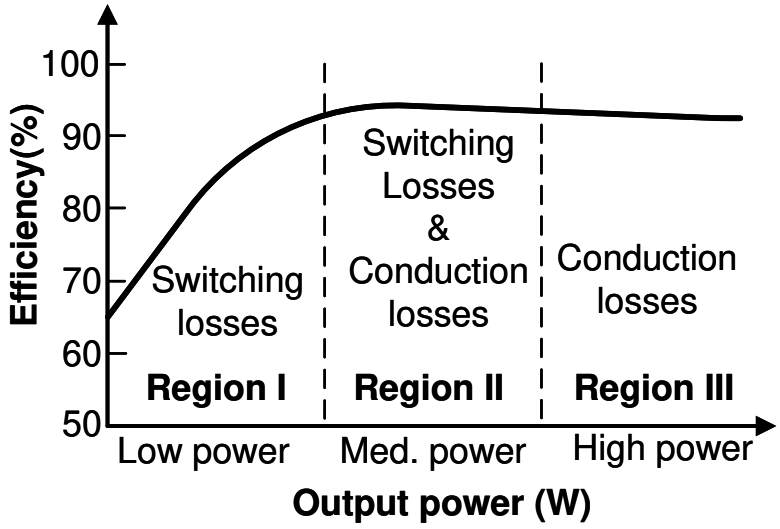


Figure 2.4: Efficiency diagram of a CDA versus output power, illustrating the dominant loss in the output power region.

Figure 2.4 illustrates the efficiency diagram of a CDA versus the output power, highlighting the dominant loss in different output power regions. Region I, II, and III represent low-power, medium-power, and high-power operation regions of the CDA, respectively. In Region I, switching losses dominate; in Region II, both switching and conduction losses are significant; and in Region III,

conduction losses surpass switching losses. Depending on the specific application and the CDA's operating power region, one can target specific losses for optimization to achieve better efficiency in that region.

2.2 Class-D Amplifier Architectures and Modulation Techniques

This literature review examines the principal components and control strategies of CDA systems, focusing on architectural structures, modulation techniques, and feedback topologies. By analyzing the main developments and methodologies in CDA design, this review provides a thorough overview of the current approaches in the field, evaluating the benefits and drawbacks of different architectural choices and control mechanisms.

First, existing CDA structures will be reviewed with an emphasis on architectural configurations. In this examination, three primary categories—fully analog CDA, fully digital CDA, and mixed-signal CDA architectures—will be considered, each presenting distinct advantages and design challenges in achieving optimal efficiency, linearity, and fidelity in class-D amplification.

Second, modulation techniques employed in class-D amplifier design will be reviewed, as these play a critical role in shaping the amplifier's performance and suitability for various applications. Depending on the specific requirements—such as efficiency, linearity, or spectral characteristics—different modulation strategies are applied. This review will examine the most commonly used techniques in the literature, highlighting their distinct features, advantages, and limitations. By comparing methods such as PWM, SHEPWM, and Delta-Sigma Modulation, this section will provide insights into the modulation choices available for optimizing CDA performance across a range of operational contexts.

2.2.1 Class-D Amplifier Structures

Most CDAs are for audio applications, therefore numerous publications are available for audio CDAs. Very few published CDAs are for industrial or automotive applications. But generally, their structures can be classed into three different categories. In the first category are CDAs that are designed using analog circuits. Choi et al. (2012); Kovačević, Pešić-Brdjanin, and Galić (2018);

W.-C. Wang and Lin (2016) reported such CDAs and their input signals are analog signals (Figure 2.5). Input analog signals are summed with feedback signals and create error signals which will be compared with ramped signals. The PWM signals are generated at the output of comparators and non-overlapping PWM signals are derived which will drive the power MOSFETs. Such an analog CDA's modulation technique uses an analog modulator.

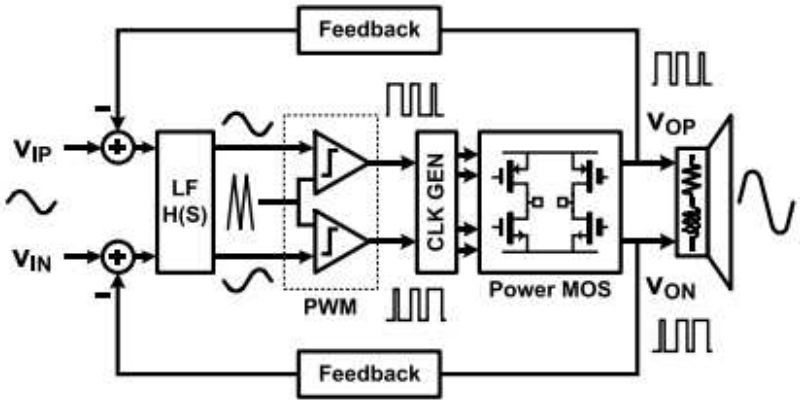


Figure 2.5: Analog class-D amplifier block diagram (W.-C. Wang and Lin (2016))

The second category is CDAs that are designed in digital circuits. Chang and Wu (2016); Kuo and Liou (2019); McKenzie and Ng (2018); M. Wang, Jiang, Song, and Brooks (2010) reported such CDAs and they use a digital PWM modulator (Figure 2.6). The input signals are available in digital audio form. The digital CDA uses an ADC in its feedback loop because CDA's output is an analog signal while the input is a digital signal. The operation principle is the same as an analog CDA where the input signal is summed with the feedback signal and the error signal is accumulated by the loop filter. The error signal from the loop filter is quantized using a digital comparator and the generated PWM signal drives the power stage.

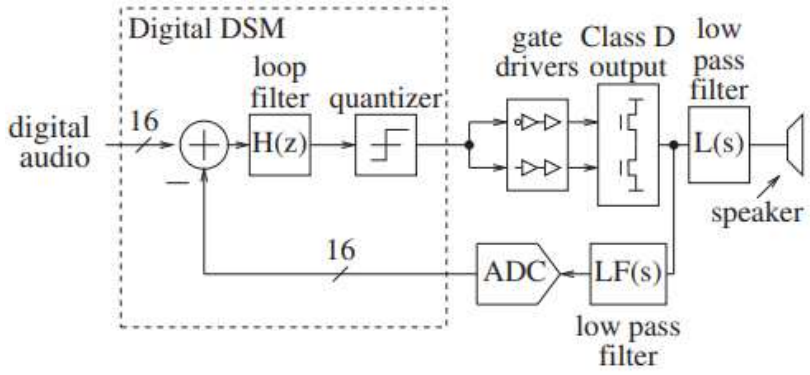


Figure 2.6: Digital class-D amplifier block diagram (McKenzie and Ng (2018))

The third category is CDAs that are designed in mixed-signal circuits. Berkhout and Dooper (2010); Guanziroli, Bassoli, Crippa, Devecchi, and Nicollini (2012) reported such CDAs. Their input signals are in digital form and use a digital PWM modulator (Figure 2.7). However, the feedback path and loop filter are implemented in analog circuits and analog PWM is generated to drive the power stage.

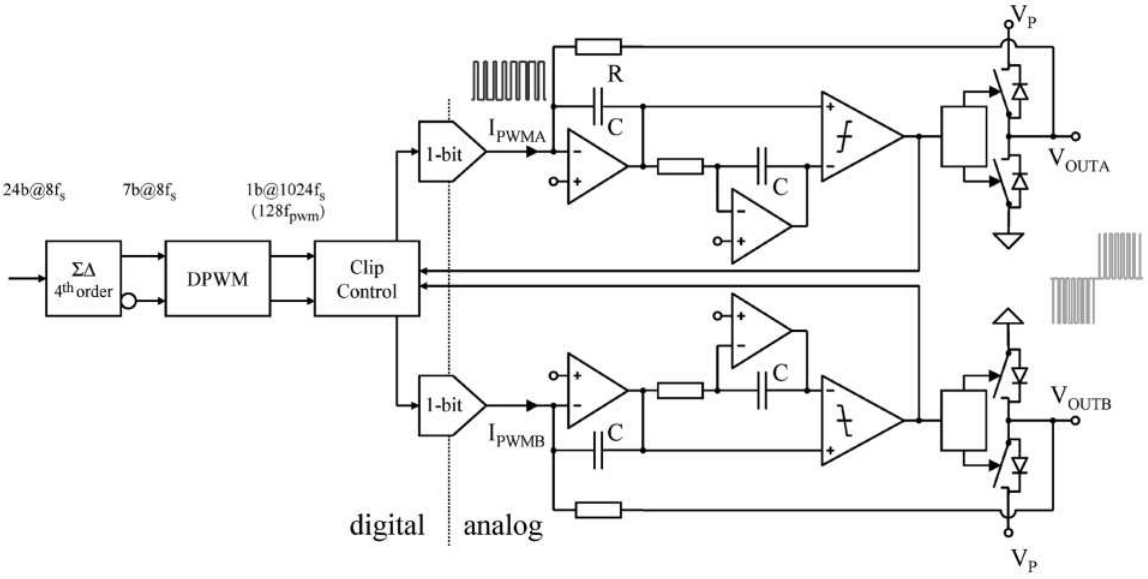


Figure 2.7: Digital class-D amplifier block diagram (Berkhout and Dooper (2010))

Depending on the applications and requirements of the system, the CDA's structures discussed above have their advantages and disadvantages. Analog CDA is used in applications where input

signals are available as analog signals, and its feedback system does not require complex ADC.

Most of the input signals are available in digital form due to the increasing demand for digital electronics and it is easy to store audios in digital format. So, most of the CDA's front-end uses a digital modulator for easy processing of the input signals. Pure digital CDAs, however, still require ADC in its feedback. The mixed-signal CDAs combine the advantages of both analog and digital CDAs, use digital PWM modulator in front-end, and analog circuits are used for the back-end. Such a structure gets rid of ADC and complex signal processing in the feedback loop. Most of the existing power stage topologies use full-bridge differential output. This power topology generates two or three-level PWM at the output depending on the modulation technique it uses. As discussed before, multilevel inverters that use more than three-level topologies have advantages over fewer-level topologies in reducing the THD and filter size. There are very few publications in CDAs that use multilevel topologies whereas most of the multilevel topologies are reported in DC-DC converters. This is because the duty cycle of CDA's PWM is always changing but DC-DC converters' PWM duty cycle is fixed. This makes the signal processing of multilevel CDA even more complex. Høyerby, Jakobsen, Midtgaard, and Hansen (2016) reports state-of-the-art multilevel CDA. Its general structure is the same as an analog CDA, where it uses a fourth-order analog loop filter to get rid of an ADC in the feedback loop.

It is noteworthy that many existing CDAs implement feedback after the power output stage. This design choice is often due to practical constraints in integrating the low-pass filter (LPF) within the chip, as most CDAs are implemented as integrated circuits without internal LPFs. Consequently, the power stage output is typically the only point available for feedback within these chips. Only a limited number of studies have explored feedback configurations that incorporate the LPF W. Yu et al. (2009). The majority of previously reviewed literature utilizes "incomplete feedback" (see Figure 2.8), where the feedback loop does not include the LPF. In contrast, "complete feedback" which integrates the LPF, effectively suppresses the non-linear effects of the inductor. By including the LPF in the feedback path, CDAs employing complete feedback achieve more accurate output at the load, though they require more complex compensation. Additionally, W. Yu et al. (2009) reports that "complete feedback" not only improves output accuracy but also reduces THD compared to the same CDA using "incomplete feedback".

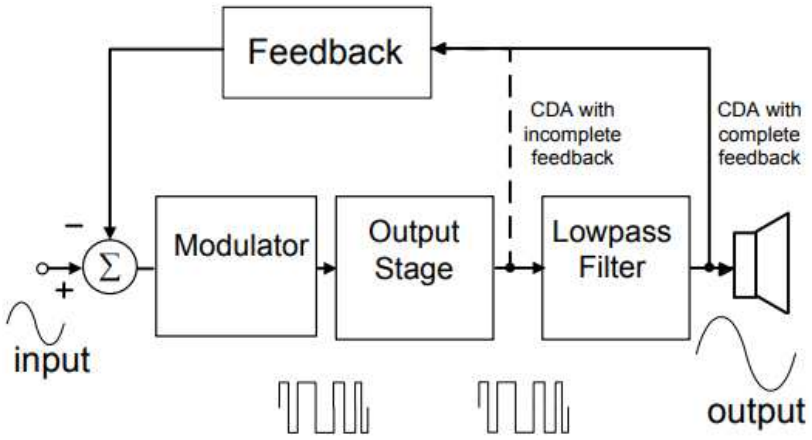


Figure 2.8: Two different feedback types in CDA (W. Yu et al. (2009))

2.2.2 Class-D Amplifier Modulation Techniques

PWM and PDM are two widely used modulation schemes in CDAs, and both can be implemented in either fully analog or digital designs.

PWM is generally preferred over PDM due to its straightforward implementation and intuitive operational principles. However, PWM introduces significant EMI because of the high-frequency carrier signal and its harmonics. To address this issue, the fully analog CDA presented in Nagari, Allier, Amiard, Binet, and Fraisse (2012) employs PWM modulation with spread spectrum clocking, achieving an 11 dB reduction in carrier EMI energy and a -72 dB total harmonic distortion plus noise (THD+N) at 1.2 W with an 8 Ω load. Fully digital CDAs are less common, as the use of an ADC in the feedback loop can compromise loop stability. Nevertheless, digital-input CDAs are popular due to the ease of processing digital audio sources. Consequently, many CDAs are designed with digital input and analog feedback structures, as discussed in the previous section. For digital-input CDAs, some designs convert Pulse Code Modulation (PCM) to PWM using a multi-bit digital noise-shaper followed by a counter Grosso, Botti, Stefani, and Ghioni (2001), while others employ PCM to PDM conversion with a single-bit high-frequency digital noise-shaper Philips, van den Homberg, and Dijkmans (1999).

PDM requires a significantly higher switching frequency to achieve performance comparable to that of PWM. A study in Gaalaas, Liu, and Nishimura (2005) demonstrates a hysteretic technique

to reduce switching speed, utilizing a fully analog PDM with a 7th-order Delta-Sigma Modulator, achieving -90 dB THD+N at 1 W output into a 6 Ω load. In contrast, a fully digital PDM implementation in Ihs and Dufaza (2010) employs a 5th-order DSM, reaching -75 dB THD+N at 0.8 W into an 8 Ω load. Although higher-order Delta-Sigma Modulator can yield lower THD+N, they also risk stability issues, introducing a trade-off between phase margin and THD+N in the selection of DSM order. Unlike PWM, PDM avoids carrier frequency interference and its harmonics within the signal band of interest. However, the high switching frequency required by PDM contributes to increased power loss.

SHEPWM is a notable, albeit less commonly utilized, modulation technique in CDAs. The foundational theory of SHEPWM was first introduced in Patel and Hoft (1973), with the majority of existing research focusing on three-phase, high-power electronic applications where the load frequency remains fixed. This technique employs a Fourier Transform on the PWM signal, utilizing mathematical methods to selectively eliminate specific harmonics by reducing them to zero. SHEPWM has been adapted for use in multilevel inverters, as illustrated in Manai, Armi, and Besbes (2019), where a Flying Capacitor Multilevel Inverter (FCMI) effectively cancels lower-order harmonics. In this three-phase, high-power inverter application, triple-order harmonics are inherently canceled, and the remaining low-order harmonics are further mitigated through advanced mathematical techniques. Compared to traditional PWM and PDM, SHEPWM operates at a significantly lower switching frequency, leading to substantial reductions in switching losses within the system. However, one of the principal challenges of SHEPWM is maintaining the voltage balance of the flying capacitor. This issue persists because no universal mathematical solution can address all modulation indices, thereby restricting the achievable voltage amplitudes at the load to specific values. Further discussion on the background and current state-of-the-art developments in SHEPWM will be provided in subsequent sections.

Several studies have reported on CDAs utilizing nonlinear control techniques, specifically SMC Ge and Chang (2009); Hussein, Mohieldin, Hussien, and Eladawy (2016); Pillonnet, Abouchi, Cellier, and Nagari (2009); Pinar and Weaver (2014); Rojas-Gonzalez and Sanchez-Sinencio (2009);

Rojas-González and Sánchez-Sinencio (2007); Torres, Colli-Menchi, Rojas-Gonzalez, and Sanchez-Sinencio (2011); Torres, Colli-Menchi, Rojas-González, and Sánchez-Sinencio (2010); X. Wu, Zaman, Zheng, Khan, and Ali (2019); Ying, Ling, Qing-De, and Yao-hua (2008); S.-H. Yu and Tsai (2010); S.-H. Yu and Tseng (2011). These works claim improved efficiency, lower THD, and enhanced PSSR. In these implementations, CDAs achieve higher efficiency since SMC eliminates the need for a triangular carrier signal, reducing power consumption. Improved THD performance is attributed to SMC's typically high switching frequencies, which help to reduce chattering effects and enhance signal fidelity, though at the expense of increased switching losses. Due to the robustness and disturbance insensitivity of SMC, these studies also report higher PSSR. A common feature across these works is the implementation of SMC in continuous-time systems using analog IC technology, as continuous-time operation allows state variables to remain close to the sliding surface. In contrast, discrete-time SMC can only operate in a quasi-SMC scheme, where control events are limited to sampling instants. As a result, state variables may deviate from the sliding surface between sampling periods, degrading overall system performance. Consequently, very few studies have explored discrete-time SMC in CDAs or addressed its impact on robust performance.

To mitigate chattering effects and reduce THD, the switching frequency of an SMC-based CDA should be sufficiently high. However, this approach decreases overall system efficiency due to the increased switching losses in power transistors. One method to reduce the effective switching frequency per transistor is to implement a multilevel topology; for instance, S.-H. Yu and Tseng (2011) employs a nine-level cascaded H-bridge topology. While S.-H. Yu and Tseng (2011) achieves a THD+N of less than $0.027\,\%$ across the audio band ($20\,\mathrm{Hz} - 20\,\mathrm{kHz}$), the efficiency reaches only $80\,\%$ at an output power of $8.3\,\mathrm{W}$. A notable disadvantage of the cascaded H-bridge topology is its requirement for two isolated DC sources, which is suboptimal for applications where only a single DC source is available. Additionally, the study does not report performance metrics for output power levels below $8.3\,\mathrm{W}$. Further discussion on the background and current state-of-the-art developments in SMC will be provided in subsequent sections.

2.3 Background of Selective Harmonic Eliminated Pulse Width Modulation (SHEPWM) Technique

Recent advances in power transistors have facilitated the development of smaller and lighter power electronics boards. Among these, GaN devices are considered among the most promising candidates for switch-mode converters due to their fast switching capability and compact size Chung, McKenzie, and Ng (2016); Gedz, Lazebnyi, Onikienko, and Vlasjuk (2018); Ly et al. (2020); Mauerer and Kolar (2018); Sangid et al. (2018); Seidel and Wicht (2018). However, to achieve further reduction in overall system size and improve power distribution across different loads and varying conditions, it is necessary to replace conventional bulky power electronic components with reconfigurable power electronics units. Reconfigurability contributes to size reduction by integrating multiple functionalities within a single, adaptable module. This flexibility eliminates the need for multiple discrete power circuits, each tailored for specific load conditions. As a result, a reconfigurable power unit can dynamically allocate power based on load requirements, optimizing space and reducing the number of components needed. To realize such reconfigurable systems, a heterogeneously integrated SiP on a low-temperature co-fired ceramic (LTCC) substrate is a particularly promising approach. This solution not only supports the integration of diverse components but also provides high 3D integration density, along with superior thermal and electrical performance Bayer et al. (2020); Nobert, Alameh, Ly, Constantin, and Blaquière (2021).

Low-power loads, such as industrial servo valves, hall effect sensors, and low-power actuators, find common usage in a wide range of industries, including automotive, industrial automation, and critical power systems. These applications necessitate precise control, sensing, and measurement of diverse parameters. In such scenarios, the switching losses of power devices in the inverter play a dominant role compared to conduction losses due to their operation at extremely low AC load currents. The operation frequency of these loads is usually in the range of several kHz to $10\,\mathrm{kHz}$. A Natural Pulse Width Modulation (NPWM), where a reference sinewave is compared with a carrier signal to generate the PWM signal, needs to operate with a high switching frequency to reduce the THD at the cost of high-switching losses Jahmeerbacus and Sunassee (2014). This reduces the overall efficiency of the converter.

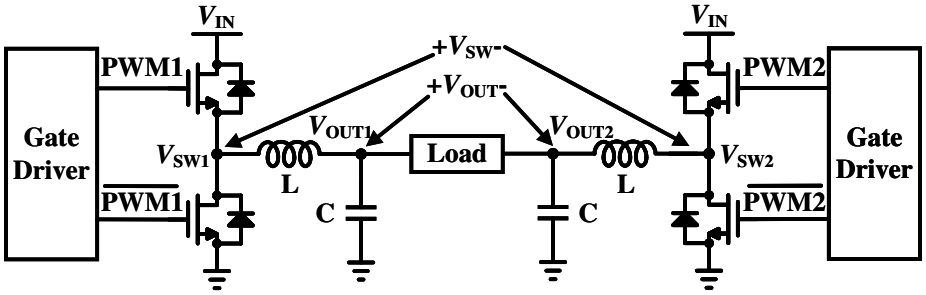


Figure 2.9: Schematic of a full-bridge inverter output stage.

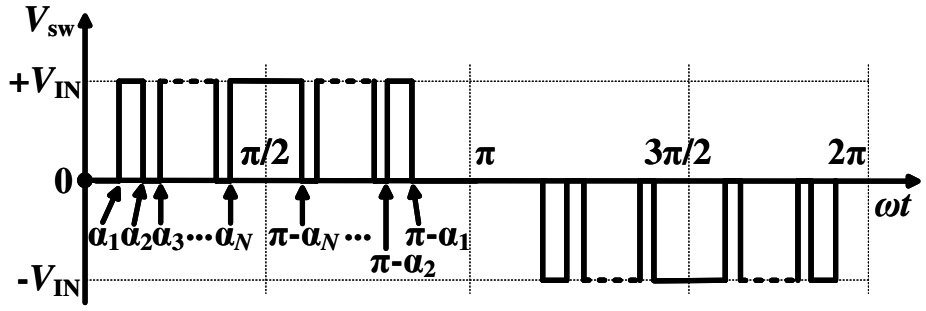


Figure 2.10: A three-level odd-symmetrical SHEPWM waveform.

Unlike an NPWM inverter, the SHEPWM technique reduces switching losses by predetermining the switching angles of the PWM signal, which eliminates lower-order harmonics and enables low THD without increasing the switching frequency of the power transistors. A three-level differential SHEPWM signal can be generated at the differential switching nodes (+V_{SW}- in Figure 2.9), where PWM1 and PWM2 are driven by two Gate Drivers (GDs). Lower-order harmonics at V_{SW} can be cancelled by expanding the Foureir Series of the switching node voltage and make lower-order harmonics (except the fundamental component) equal to zero. Meanwhile, the higher-order harmonics are suppressed by a low-pass LC filter, resulting in a single-tone AC output signal (+V_{OUT}-) delivered to the load.

A three-level PWM is depicted in Figure 2.10 with N switching angles per quarter cycle. V_{SW} can be represented by a Fourier Series as follows:

$$V_{\mathrm{SW}}(\omega t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{14}$$

where a_0 is the DC component, n is the harmonic order, ω is the angular frequency in rad/second, t is time, a_n are the coefficients of the cosine terms, and b_n are the coefficients of sine terms. In signals with odd quarter-wave symmetry, specific Fourier Series coefficients naturally become zero due to the inherent properties of the waveform. This symmetry ensures that the DC component, represented by a_0, is eliminated, preventing any undesired offset in the signal. Additionally, all cosine coefficients, a_n, are also equal to zero, indicating that the waveform lacks even-harmonic content, which is a key characteristic of odd-symmetric signals. Moreover, the sine coefficients corresponding to even-order harmonics, such as b_2, b_4, and up to b_{2n}, are inherently zero, which significantly reduces the presence of these harmonics in the frequency spectrum. This natural harmonic cancellation simplifies the control and design of the switching waveform, as it inherently eliminates certain undesired harmonic components without requiring additional filtering or modulation efforts. By leveraging this odd quarter-wave symmetry, the output waveform becomes more spectrally efficient, reducing distortion and improving the overall linearity of the system. Thus, (14) can be simplified to:

$$V_{\mathrm{SW}}(\omega t) = \begin{cases} \sum_{n=1}^{\infty} b_n \sin(n\omega t) & \text{for odd } n \\ 0 & \text{for even } n \end{cases} \tag{15}$$

where

$$b_n = \frac{1}{\pi} \int_0^{2\pi} V_{\mathrm{SW}}(\omega t) \sin(n\omega t) d(\omega t) \tag{16}$$

If the inverter input voltage is V_{IN}, then b_n can be expressed as:

$$b_n = \frac{4V_{\mathrm{IN}}}{n\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(n\alpha_k) \tag{17}$$

where k is an integer number ($1 < k < N$) and a_k is the k^{th} switching angle in Figure 2.10. Equation (17) can be expanded to the following equations:

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cdots \pm \cos(\alpha_N) & = \frac{\pi}{4V_{\text{IN}}} b_1 \\ \cos(3\alpha_1) - \cos(3\alpha_2) + \cdots \pm \cos(3\alpha_N) & = \frac{3\pi}{4V_{\text{IN}}} b_3 \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cdots \pm \cos(5\alpha_N) & = \frac{5\pi}{4V_{\text{IN}}} b_5 \\ \qquad\qquad \cdots & \\ \cos(n\alpha_1) - \cos(n\alpha_2) + \cdots \pm \cos(n\alpha_N) & = \frac{n\pi}{4V_{\text{IN}}} b_n \end{cases} \tag{18}$$

which must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \cdots < \alpha_N < \frac{\pi}{2} \tag{19}$$

To cancel lower odd harmonics, b_3 to b_n in Eq. (18) are set to equal to zero. b_1 is the amplitude of the fundamental output signal and b_1/V_{IN} is defined as the Modulation Index (MI). To solve for N unknown switching angles, N equations are needed, and N-1 odd harmonics can be cancelled. More switching angles mean more harmonic cancellation, however, solving the non-linear transcendental equations becomes more complicated and hardware resources for implementation increase as well. In addition, for small MI PWM signals, the pulses get narrow near 0° and 180°, therefore, a higher FPGA clock frequency (f_{CLK}) is needed for a better timing resolution for the switching angles, especially for an increased number of switching angles.

2.4 State-of-the-Art of Selective Harmonic Eliminated Pulse Width Modulation (SHEPWM) Technique

SHEPWM was first introduced in Patel and Hoft (1973, 1974). Since then, numerous papers have been published on SHEPWM theory, particularly focusing on solving the nonlinear transcendental equations necessary to determine the optimal switching angles Ahmad, Iqbal, Ali, Rahman, and Ahmed (2021); Ahmed et al. (2020); Czarkowski, Chudnovsky, and Selesnick (2002); Etesami,

Farokhnia, and Fathi (2015); Janabi, Wang, and Czarkowski (2020); Li, Zhang, and Li (2022); C. Wang et al. (2022); Yang et al. (2015, 2016, 2017). These research efforts have significantly advanced the mathematical techniques used to find switching angles that minimize harmonic distortion while maintaining desired output voltage characteristics.

As highlighted in problem statement **P1** in Section 1.2.1, previous experimental research on the SHEPWM technique has primarily been conducted in mid-to-high power applications with fixed, low output frequencies. Detailed hardware implementations in these studies were either omitted or only briefly described. For instance, works such as Iqbal et al. (2019); Manai, Armi, and Besbes (2017); Perez-Basante et al. (2020); Sharifzadeh, Vahedi, and Al-Haddad (2018); Siddique, Mekhilef, Padmanaban, Memon, and Kumar (2021); M. Wu et al. (2020); Yang, Lan, Zhang, and Tang (2018); Yang et al. (2015) focused on fundamental output frequencies (f_{T}) of approximately 50 Hz, with DC supply voltages ranging from 60 V to 200 V. In Zhao, Jin, Wang, and Sun (2016), an output frequency of 60 Hz was achieved with a DC supply voltage of 127 V. Additionally, Cheng, Xu, Chen, and Chen (2021) analyzed the dynamic response of the SHEPWM technique under a step change in output voltage, demonstrating the behavior when transitioning from 0 to 200 V.

Ahmed, Sheir, and Orabi (2017) introduced a method for real-time calculation of switching angles and showcased its application in a cascaded full H-bridge inverter with MI variations. Despite these advances, the majority of experimental studies remain limited to fixed output frequencies, which poses a challenge for applications that require variable frequency operation. To the best of the author's knowledge, there has yet to be a comprehensive study that details the implementation of a SHEPWM inverter capable of supporting variable output frequencies.

The standard approach for hardware realization of the SHEPWM technique typically involves the use of FPGAs or DSPs to generate the PWM signals. However, the existing literature Iqbal et al. (2019); Manai et al. (2017); Perez-Basante et al. (2020); Sharifzadeh et al. (2018); Siddique et al. (2021); M. Wu et al. (2020); Yang et al. (2018, 2015) often lacks sufficient detail regarding the hardware design, which complicates efforts to replicate or build upon these systems. This lack of transparency in hardware implementation remains a significant barrier to broader adoption and further innovation in the field of SHEPWM applications.

This dissertation presents a compact 3D SiP design (research objective **O2**) of a low-power

full-bridge SHEPWM inverter with reconfigurable AC outputs that can be adjusted dynamically, focusing on high-frequency applications to overcome the limitations of previous works (research objective **O1**). As there is no existing literature on low-power SHEPWM inverters and their associated THD relationship with MI and fundamental output frequency, this study explores these critical aspects over a broad range of MI and output frequencies (ranging from several kHz to 10 kHz). Additionally, the FPGA-based hardware implementation described in this work, which utilizes MATLAB^{TM} SIMULINK^{TM}, is straightforward and easily replicable (research objective **O1**).

2.5 Background of Sliding Mode Controller (SMC) Technique

SMC, a specific type of variable structure control, holds significant promise for application in CDAs due to the inherent ON/OFF nonlinear control characteristics of the power stage. SMC is known for its robustness against parameter variations, disturbances, and modeling errors. In the context of CDAs, uncertainties such as variations in transistor behavior due to manufacturing tolerances, aging, temperature fluctuations, external disturbances like load variations, and discrepancies between the ideal mathematical model and real-world dynamics may affect performance. Additionally, switching dynamics and imperfections in the power stage, such as parasitic elements and higher-order harmonics, introduce further complexities. By designing a sliding surface, the system can be driven towards this surface, leading to stable operation despite these uncertainties. In CDAs, SMC can offer precise and efficient control over the switching behavior of the transistors, contributing to improved performance and reliability Hung, Gao, and Hung (1993).

In an ideal scenario, SMC would operate at an infinite switching frequency to closely track the reference signal's controllable variable states. However, this is impractical for power converters due to limitations such as switching losses, power efficiency degradation, and the physical constraints of switching components. As a common solution to address this, a hysteresis band is often applied in SMC to constrain the switching frequency. Nevertheless, employing a hysteresis band introduces its own challenges. Notably, it results in a variable switching frequency, and if not chosen judiciously, the upper limit of the switching frequency may become excessively high, leading to a degradation

in the converter's power efficiency. One approach to mitigate this issue is to implement an adaptive hysteresis band, which fixes the switching frequency but increases the complexity of implementation. Conversely, a PWM based SMC offers a fixed switching frequency determined by the carrier frequency. This grants the designer flexibility in determining the switching frequency, allowing for optimizing other parameters of the system Sebaaly, Vahedi, Kanaan, Moubayed, and Al-Haddad (2016); Tan, Lai, and Tse (2006); Tan, Lai, Tse, and Cheung (2005); Tan, Lai, and Tse (2008a, 2008b); Tan, Lai, Tse, Martinez-Salamero, and Wu (2007); X. Wu et al. (2019).

Figure 2.11 shows two different operation states of a half-bridge. High-side and low-side transistors (M_{HS} and M_{LS}) turn on and off periodically but are complementary to each other. SMC controls two state variables: inductor current (i_{L}) and capacitor voltage (v_{C}). According to Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL), we can write:

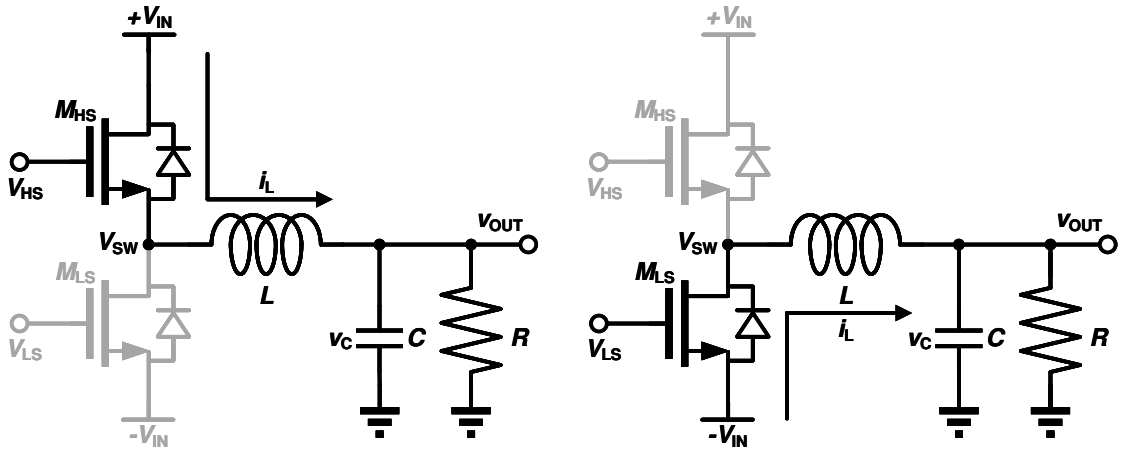


Figure 2.11: A half-bridge two-state operation.

$$\begin{cases} v_{\mathrm{C}} = V_{\mathrm{SW}} - V_{\mathrm{L}} \\ i_{\mathrm{L}} = i_{\mathrm{C}} + i_{\mathrm{OUT}} \end{cases} \tag{20}$$

which can also be written as,

$$\begin{cases} v_{\mathrm{C}} = V_{\mathrm{SW}} - L\frac{di_{\mathrm{L}}}{dt} \\ i_{\mathrm{L}} = C\frac{dv_{\mathrm{C}}}{dt} + i_{\mathrm{OUT}} \end{cases} \tag{21}$$

where v_{C} is the capacitor voltage, equals to the output voltage v_{OUT}, V_{SW} is the switching node

voltage, and its value changes between $+V_{\text{IN}}$ and $-V_{\text{IN}}$ depending on which switch turns on, V_{L} is the inductor voltage, i_{L} is the inductor current, i_{C} is the capacitor current, and i_{OUT} is the output current which flows through the load.

We can finally write down the dynamic state equation in matrix form as,

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_{\text{SW}}, \quad V_{\text{SW}} = \begin{cases} +V_{\text{IN}} & \text{if } V_{\text{HS}} = 1 \\ -V_{\text{IN}} & \text{if } V_{\text{LS}} = 1 \end{cases} \tag{22}$$

If we describe state variables in a vector form as $\boldsymbol{x}$, then the above equation can be represented by the state equation:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \tag{23}$$

where $\boldsymbol{x} = [i_{\text{L}}\ v_{\text{C}}]^T$, and $\boldsymbol{u}$ represents the control law, with $\boldsymbol{A}$ and $\boldsymbol{B}$ being the coefficients of $\boldsymbol{x}$ and $\boldsymbol{u}$, respectively, the next step is to design a control law $\boldsymbol{u}$ that ensures the desired system behavior.

$$\boldsymbol{u} = \begin{cases} +V_{\text{IN}} & \text{if } \boldsymbol{s}(\boldsymbol{x}) > 0 \\ -V_{\text{IN}} & \text{if } \boldsymbol{s}(\boldsymbol{x})) < 0 \end{cases} \tag{24}$$

where $\boldsymbol{s}(\boldsymbol{x})$ is the switching function. A switching function generally includes state variables and can be expressed as a linear transformation, i.e.,

$$\boldsymbol{s}(\boldsymbol{x}) = \boldsymbol{C}\boldsymbol{x} \tag{25}$$

where $\boldsymbol{C}$ is an m-dimensional vector. When $\boldsymbol{s}(\boldsymbol{x}) = 0$, a switching surface (sliding surface) can be obtained. The above equations indicate that designing an SMC consists of two steps:

(1) Design a sliding surface $\boldsymbol{s}(\boldsymbol{x}) = 0$, which is a function of state variables.

(2) Design a control law $\boldsymbol{u}$ such that the state equation represents the dynamics of the system, and $\boldsymbol{u}$ drives the state variables to the equilibrium point.

The physical meaning of SMC in the above two steps are:

(1) Reaching mode: given that state variables have any initial conditions, and control law $\boldsymbol{u}$ drives any state $\boldsymbol{x}$ to the sliding surface. The reaching condition can be achieved when,

$$\begin{cases} \dot{\boldsymbol{s}} > 0 & \text{if } \boldsymbol{s} < 0 \\ \dot{\boldsymbol{s}} < 0 & \text{if } \boldsymbol{s} > 0 \end{cases} \tag{26}$$

or, equivalently,

$$\boldsymbol{s}\dot{\boldsymbol{s}} < 0 \tag{27}$$

(2) Sliding mode: when state $\boldsymbol{x}$ reaches the sliding surface, control law $\boldsymbol{u}$ ensures that state $\boldsymbol{x}$ stays on the sliding surface and drives the state to the origin point. In this way, the overall system is globally asymptotically stable.

Figure 2.12 illustrates the sliding mode and the difference between an ideal sliding mode and a quasi-sliding mode. It is desirable that state $\boldsymbol{x}$ stays on the sliding surface $s(\boldsymbol{x}) = 0$ and moves to the origin point without deviating from the sliding surface. However, in the real world with a finite switching frequency, the state $\boldsymbol{x}$ stays nearby the sliding surface, and usually, a band is designed on the two sides of the sliding surface to ensure that state $\boldsymbol{x}$ would not deviate from the designed band. This causes a chattering effect and is not desirable, as it degrades the performance of the system.

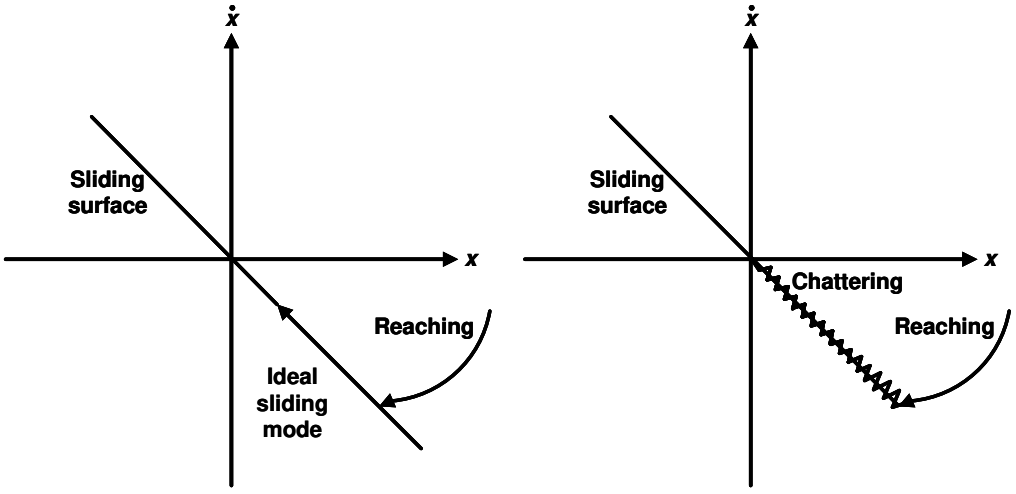


Figure 2.12: Sliding mode illustration.

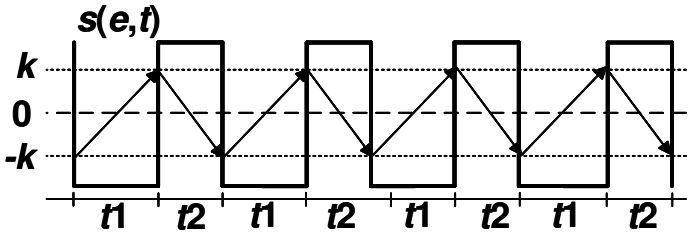


Figure 2.13: A diagram illustrating the reaching mode condition of the SMC.

To better understand, a simple reference tracking system using the SMC was designed (Figure 2.14) and simulated using SIMULINK. An analog filter with a cut-off frequency of 20 kHz replaced the LC filter for simplicity. The gate driver and power stage are implemented as a relay. The objective is to design a sliding surface ($\boldsymbol{x}$) and control law (V_{SW}) that depends on the SF. The designed SF is:

$$s(V_{e1}, t) = V_{e1}(t) + KV_{e2}(t) \tag{28}$$

where,

$$V_{e1}(t) = V_i - V_{\text{out}} \tag{29}$$

$$V_{e2}(t) = \dot{V}_{e1}(t) \tag{30}$$

where K is the first-order derivative coefficient. The goal is to design a control law such that SMC output changes according to the sign of sliding surface:

$$V_{\text{sw}} = \begin{cases} +V_{\text{IN}} & \text{when } s(V_{e1}, t) > 0 \\ -V_{\text{IN}} & \text{when } s(V_{e1}, t) < 0 \end{cases} \tag{31}$$

The simulation result is shown in Figure 2.15. It shows that the output voltage (V_{out}) tracks the input voltage (V_i), and the error voltage (V_{e1}, first column second row in Figure 2.15) between them is below 7 mV with 1 V input and output voltage. There is no amplification (gain) between V_{out} and V_i because the relay in Figure 2.14 used a unit amplitude, which means the feedback gain is also a unity gain. The SF is around zero with a band width of ± 0.02 V. Ideally, the SF should be

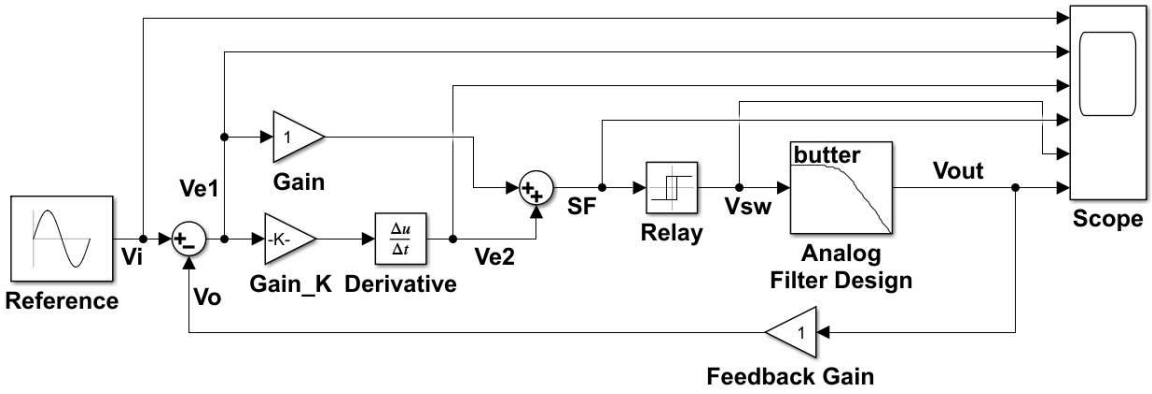


Figure 2.14: Simulink schematic of a reference tracking system using SMC.

zero so that there is no error between V_{out} and V_{i} (no chattering effect), but that requires an infinite switching frequency at the switching node (V_{SW}, second column second row in Figure 2.15).

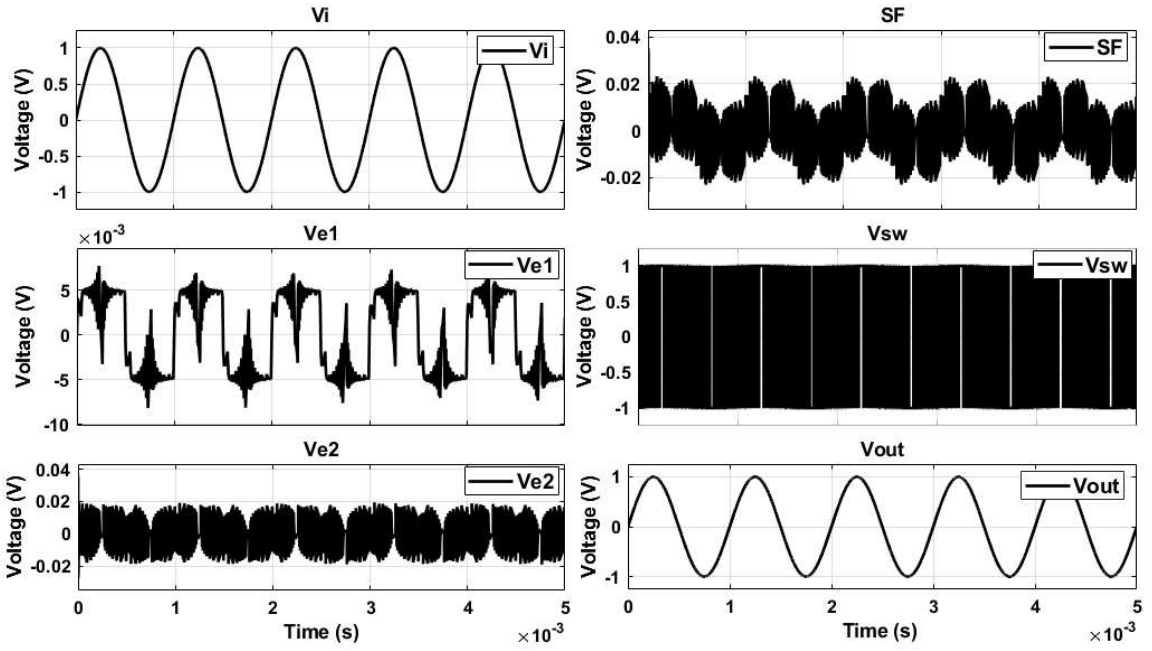


Figure 2.15: Simulink simulation of the reference tracking system using SMC.

In the real physical world, usually a hysteresis window is designed to achieve a finite switching frequency at the switching node. In a simple SMC design, the switching frequency depends on several parameters, which can be calculated using the equation below:

$$f_{\text{SW}} = \frac{1}{2k}\frac{R}{L}\left(1 - \frac{v_{\text{C}}}{V_{\text{IN}}}\right) \tag{32}$$

where k is the hysteresis window, R is the load resistor, L is the inductor value of the LC filter, v_C is the capacitor output voltage, and V_{IN} is the power stage voltage.

2.6 State-of-the-Art of Sliding Mode Controller (SMC) Technique in Class-D Amplifiers

There exist various approaches to define the SMC, with the most prevalent being a fusion of state variables and their derivatives Ding, Zheng, Sun, and Wang (2018); Ma and Han (2004); Ma and Zhang (2005); Rojas-González and Sánchez-Sinencio (2007); Sahu, Maity, Mahakhuda, and Samal (2014); Tan, Lai, Cheung, and Tse (2005). These controllers leverage the sliding mode concept to achieve robust control by driving the system states onto a specified sliding surface and maintaining them there, despite the presence of system uncertainties and external disturbances. To address steady-state error more effectively, some studies have incorporated an additional integral term into the state variables, resulting in the Integral Sliding Mode Controller (ISMC) Brisilla and Rani (2019); Hussein et al. (2016); Pinar and Weaver (2014); Tan, Lai, Tse, and Cheung (2005); Tan, Lai, Tse, and Wu (2006); Torres et al. (2011). The ISMC enhances the ability of the controller to reject persistent disturbances and reduces steady-state error, thereby improving overall system performance.

To further augment this error reduction, a subset of publications has introduced a second integral term, leading to the development of the DISMC Harirchi, Rahmati, and Abrishamifar (2011); Pradhan and Subudhi (2016); Tan et al. (2008b); X. Wu et al. (2019). This advanced control approach has shown promise in applications requiring higher precision and robustness by incorporating both integral actions, thereby providing enhanced disturbance rejection and reduced chattering effects. However, the DISMC concept remains largely unexplored in CDAs, especially with respect to discrete implementations (problem statement **P3**). The main challenge in applying DISMC to CDAs lies in the time-varying nature of the reference signal inherent in AC tracking systems.

This variability complicates the dynamic equations and makes determining appropriate controller gains more difficult, often requiring sophisticated design methodologies and computational tools (problem statement **P4**).

The use of digital DISMC presents significant advantages in the realm of SMPS and similar high-frequency power electronic applications. Unlike traditional analog implementations, which are tied to specific technology nodes and can require substantial redesigns to accommodate different application requirements, digital controllers provide unparalleled flexibility. Adjustments and updates can be made through software reprogramming, allowing for rapid iteration and customization. This adaptability simplifies the design and testing processes while improving the system's robustness to parameter variations and external disturbances. Moreover, digital implementations facilitate the incorporation of advanced control algorithms, such as adaptive and predictive control techniques, which can be seamlessly integrated to optimize performance.

The potential of DISMC in CDAs is particularly noteworthy given the increasing shift toward digital control in modern power electronics. The ability to implement complex control strategies, achieve precise waveform tracking, and enhance power efficiency through reduced switching losses makes exploring digital DISMC implementations a promising avenue for future research in CDA applications (research objective **O3**). This exploration could open new opportunities for creating highly adaptable, efficient, and robust audio amplification systems capable of meeting the demanding requirements of contemporary electronic devices.

This dissertation presents a new application of the discrete DISMC in full-bridge CDAs, a domain where its use has not been explored before, as previous studies have focused on DC-DC converters. In DC-DC converters, the reference signal remains constant, whereas in CDAs, the reference signal is time-varying. To address this, the research introduces a unique reaching and stability analysis to derive the appropriate DISMC controller gain for CDAs (research objective **O4**). Additionally, this dissertation investigates the discrete implementation of DISMC, a technique traditionally applied in the analog domain, where its fast signal processing capabilities are well-established. However, in the digital domain, feedback loop delay becomes a critical factor, which has been considered in the context of this work. These contributions provide a comprehensive understanding of DISMC in both continuous and discrete domains, highlighting its advantages and

challenges when applied to CDAs.

Chapter 3

SHEPWM Inverter with a Compact SiP Implementation

In the pursuit of different methods for low-power applications, various linear amplifier topologies such as Class A, B, AB, and C were initially considered. These amplifiers offer low THD; however, they inherently suffer from reduced efficiency when compared to switching amplifiers. Additionally, alternative architectures for sine wave generation, such as direct digital synthesis and arbitrary waveform generators, presented significant difficulties in delivering more than $1\,\mathrm{W}$ output power.

Existing works on SHEPWM techniques primarily target high-power systems operating at a narrow fundamental output frequency range, typically around $50\,\mathrm{Hz}$ or $60\,\mathrm{Hz}$. These studies assume fixed filter designs optimized for such frequencies, ensuring effective harmonic suppression and system efficiency. However, no prior work has explored the challenges of applying SHEPWM across a wide range of fundamental output frequencies—specifically from $4\,\mathrm{kHz}$ to $10\,\mathrm{kHz}$—while maintaining a fixed filter cutoff frequency. This unexplored area is critical for low-power applications where frequency adaptability and efficient harmonic control are essential.

In this work, to achieve research objectives **O1** and **O2**, we address these challenges by developing a novel FPGA-based architecture tailored for wide-frequency SHEPWM operation, which will

be implemented in an LTCC SiP. LTCC technology is selected not only for its high level of component integration on both sides of the substrate, but also for additional advantages such as the ability to print and embed passive components, and the use of via fill and substrate materials with superior thermal conductivity compared to traditional PCBs—features that have been utilized in other research studies. However, the exploitation of these LTCC properties is not the objective of this dissertation. The design supports on-the-fly configurability of the inverter output, allowing dynamic adjustment of both the modulation index and the fundamental frequency without requiring extensive storage or computationally intensive real-time calculations. The FPGA architecture achieves this flexibility through the efficient implementation of the SHEPWM algorithm, enabling precise harmonic elimination across a broad frequency range while adhering to the constraints imposed by a fixed filter design.

By investigating wide-frequency operation with SHEPWM and introducing a resource-efficient, dynamically configurable FPGA architecture, this work contributes significantly to the field. It demonstrates the feasibility of extending SHEPWM techniques to low-power systems with diverse operational requirements, achieving high efficiency and harmonic performance across varying frequencies.

This chapter is organized as follows: Section 3.1 discusses the design of the SHEPWM full-bridge inverter, detailing the converter topology and control strategy. Section 3.2 presents both simulation and experimental results to validate the proposed design, highlighting its performance in low-power applications. Finally, Section 3.3 provides a conclusion to this chapter, summarizing the key findings and contributions of the work.

3.1 Design of SHEPWM Full-Bridge Inverter

In this work, an FPGA was chosen to implement the SHEPWM technique due to its advantages in optimizing mathematical operations, offering enhanced interface capabilities, and supporting higher clock frequencies.

While application specific integrated circuits (ASICs) can provide superior performance in high-volume, specialized applications due to their customization, their development comes with significantly higher initial costs, longer design cycles, and reduced flexibility, making them unsuitable for this design. On the other hand, MCUs are attractive for their cost-effectiveness, low power consumption, and simpler development process. However, MCUs typically operate at lower clock frequencies, which can limit the resolution of switching angles—an issue that becomes especially critical at high fundamental frequencies. The choice of FPGA was driven by:

(1) Mathematical Operations Optimization: In this work, several multiplications were used. FPGAs are inherently adept at executing mathematical operations, particularly multiplications, due to their tailored optimization. Their ability to perform math and logic operations in parallel significantly boosts efficiency and speed—a significant advantage over microcontrollers, which are primarily optimized for sequential processing.

(2) Interface Optimization: The designed system includes multiple interfaces with the controller, a configuration that aligns optimally with the FPGA architecture. In the designed SHEPWM inverter architecture, the setup includes not only two PWM interfaces to the LTCC SiP but also includes gate driver configuration interfaces. These interfaces facilitate both writing and reading of shift registers within the gate driver. These shift registers configure different driving strengths and deadtime. In contrast, MCUs typically encounter limitations in terms of available interfaces.

(3) Rapid prototyping and Development: the FPGA's capacity for implementing digital logic coupled with the sophisticated tools available significantly reduces prototyping development time. For instance, this work highlighted the implementation of the SHEPWM algorithm through the Xilinx System Generator for DSP embedded into Simulink. This integration expedited algorithm validation and Hardware Description Language (HDL) code generation within the Simulink environment. This accelerated process minimizes the development time disparity between FPGAs and MCUs.

(4) Storage Availability: FPGAs offer the advantage of readily available embedded storage resources, such as block random access memory (BRAM), which can be used without additional costs. This provides efficient data storage and retrieval, supporting complex control algorithms and intermediate data management. Compared to ASICs, which may require external memory interfaces, FPGAs have built-in storage resources, making them more versatile and cost-effective for the design.

In conclusion, the unique combination of optimized mathematical operations, interface compatibility, rapid prototyping capabilities, team expertise, advantageous clock frequency, and embedded storage makes the FPGA the most suitable choice for achieving the high-resolution switching angles required in this research. For prototyping and iterative development, an FPGA offers the optimal balance between performance, development time, and cost.

This work demonstrates a low-power full-bridge SHEPWM inverter with on-the-fly reconfigurable AC outputs in a compact 3D SiP, with an emphasis on high-frequency applications to address the shortcomings of the aforementioned works. As no low-power SHEPWM inverter along with its output THD relationship with MI and the fundamental output frequency is reported in the literature, this work investigates these key aspects with a full range of MI and a wider range of output frequencies (several kHz to $10\,\mathrm{kHz}$). Furthermore, a detailed FPGA hardware implementation in MATLAB$^{\mathrm{TM}}$ SIMULINK$^{\mathrm{TM}}$ is described in this work, which is simple and can be replicated easily. The method of FPGA hardware implementation is straightforward and does not require any knowledge of an HDL.

The architecture of the FPGA for SHEPWM is designed using System Generator (SysGen) for DSP, which is fully integrated into MATLAB Simulink. HDL codes are generated automatically using SysGen after validating the SHEPWM block's function using Simulink. The proposed method is simple, cost-effective, and has the capability of on-the-fly configuration of both output amplitude and frequency. The detailed hardware implementation along with Simulink simulations are described in detail in this section.

Selecting the appropriate number of switching angles for generating a fundamental sine wave

output significantly impacts both the THD and power consumption of the SHEPWM inverter. Although increasing the number of switching angles enables the cancellation of more lower-order harmonics, thereby reducing THD, there are practical limitations to this approach. As the number of switching angles rises, solving the corresponding transcendental equations becomes increasingly challenging. Moreover, the reduction in THD becomes less pronounced with a higher number of switching angles.

Figure 3.1 illustrates the THD after filtering SHEPWM waveforms with 13, 15, and 17 switching angles per quarter cycle in Matlab. The filtering is performed using a second-order filter with a cut-off frequency of $20\,\mathrm{kHz}$, applied to fundamental output frequencies of $5\,\mathrm{kHz}$ and $4\,\mathrm{kHz}$. The MI remains constant at 0.4167 for all waveforms. The results demonstrate that while an increase in the number of switching angles from 13 to 15 yields a noticeable reduction in THD, the improvement from 15 to 17 angles is minimal, particularly at higher fundamental output frequencies. This indicates that further increasing the number of switching angles provides diminishing returns in THD reduction.

Additionally, there are cases where solutions to the transcendental equations do not exist as the number of switching angles increases. Higher switching frequencies at the power stage also lead to increased switching losses, counteracting the benefits of additional switching angles. Thus, the THD advantages of increasing the number of switching angles must be carefully weighed against these practical constraints.

The example used in this work targets 17 switching angles per quarter-cycle, which eliminates 16 odd harmonics. That means 3^{rd} to 33^{rd} odd harmonics are cancelled and even harmonics do not exist in the odd symmetric SHEPWM signal. Therefore, the 35^{th} harmonic is the first tone following the cancelled harmonics. The equations are solved in MATLAB by guessing the initial switching angles. The resulting optimal switching angles in degrees for different MI are given in Table 3.1 and plotted in Figure 3.2. In Table 3.1, the odd index switching angles $(\alpha_1, \alpha_3, \ldots, \alpha_{17})$ are the rising edges and the even index switching angles $(\alpha_2, \alpha_4, \ldots, \alpha_{16})$ are the falling edges of the SHEPWM signal. The second row is the set of initial (guessed) switching angles common for all the modulation indices (MIs). Subsequent rows show the solutions for optimal switching angles for each MI from 0.2 to 0.9. As seen in the table, the solved optimal switching angles for all MI are in the vicinity of

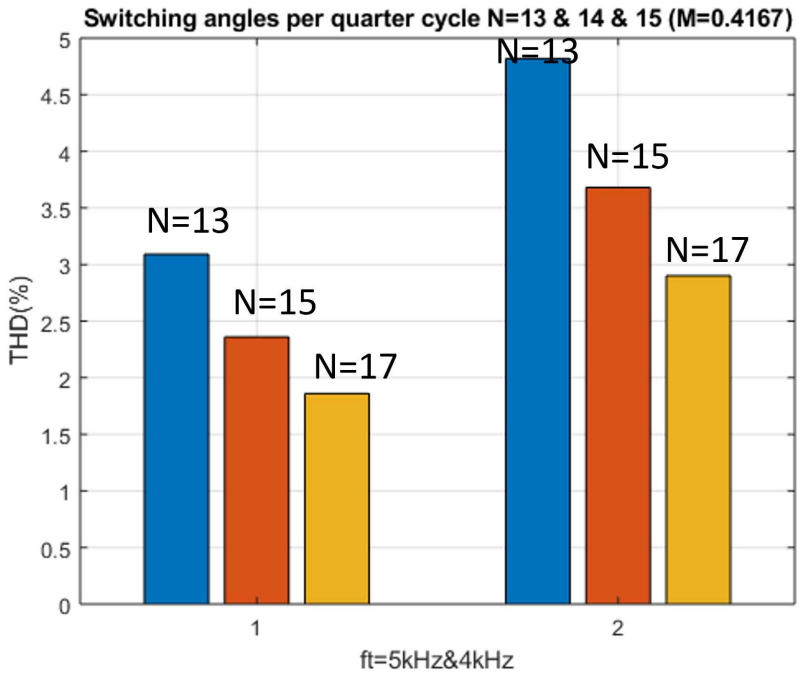


Figure 3.1: THD of second-order filtered output for various switching angle counts at fundamental output frequencies of $5\,\mathrm{kHz}$ and $4\,\mathrm{kHz}$

initial switching angles.

3.1.1 Proposed SHEPWM FPGA Architecture

In this work, the precomputed optimal switching angles are stored in a Look-up Table (LUT), implemented using a BRAM in the FPGA. To avoid reprogramming the FPGA when generating different AC output signals at the load, the switching angles (first half period) of different amplitude and frequency output signals can be stored in the LUT so that configuring outputs on-the-fly is achieved by simply sending a command signal to the FPGA.

A counter-based methodology is used to generate the pulses according to the computed switching angles, as shown in Figure 3.3. In this work, 17 ($N = 17$) optimal switching angles per quarter-cycle are used. When the counter (ramp signal in Figure 3.3) equals each switching angle (horizontal line), PWM signals change their logic levels. Switching angles in the first half-period (α_1 to α_{2N}) are used to generate the PWM1 signal and α_{2N+1} to α_{4N} are used to generate the PWM2 signal. PWM1 and PWM2 drive the full-bridge GaN devices from two sides and a three-level differential

Table 3.1: INITIAL GUESSED AND CALCULATED OPTIMAL SWITCHING ANGLES IN DEGREES FOR DIFFERENT MODULATION INDICES (MI)

MI	$\alpha_1\uparrow^a$	$\alpha_2\downarrow^b$	$\alpha_3\uparrow$	$\alpha_4\downarrow$	$\alpha_5\uparrow$	$\alpha_6\downarrow$	$\alpha_7\uparrow$	$\alpha_8\downarrow$	$\alpha_9\uparrow$	$\alpha_{10}\downarrow$	$\alpha_{11}\uparrow$	$\alpha_{12}\downarrow$	$\alpha_{13}\uparrow$	$\alpha_{14}\downarrow$	$\alpha_{15}\uparrow$	$\alpha_{16}\downarrow$	$\alpha_{17}\uparrow$
	10.03^c	11.00^c	20.00^c	21.94^c	29.97^c	32.83^c	39.94^c	43.60^c	49.90^c	54.26^c	59.87^c	64.74^c	69.84^c	75.06^c	79.81^c	85.14^c	89.67^c
0.2	9.81	10.16	19.63	20.31	29.46	30.46	39.31	40.60	49.19	50.72	59.10	60.83	69.03	70.91	79.00	80.97	89.00
0.3	9.71	10.22	19.43	20.45	29.17	30.66	38.94	40.86	48.75	51.05	58.61	61.21	68.52	71.35	78.48	81.45	88.49
0.4	9.60	10.28	19.21	20.56	28.85	30.83	38.54	41.10	48.29	51.34	58.10	61.57	67.99	71.76	77.95	81.92	87.99
0.5	9.48	10.33	18.97	20.65	28.51	30.98	38.11	41.30	47.79	51.61	57.56	61.90	67.43	72.16	77.40	82.38	87.47
0.6	9.35	10.36	18.73	20.72	28.15	31.09	37.65	41.45	47.25	51.82	56.97	62.19	66.83	72.53	76.82	82.83	86.94
0.7	9.21	10.38	18.46	20.76	27.76	31.15	37.15	41.55	46.66	51.97	56.33	62.41	66.16	72.85	76.19	83.27	86.39
0.8	9.07	10.37	18.16	20.75	27.33	31.15	36.59	41.56	45.99	52.01	55.58	62.52	65.39	73.08	75.47	83.67	85.81
0.9	8.90	10.33	17.83	20.67	26.82	31.03	35.92	41.41	45.17	51.84	54.63	62.36	64.36	73.05	74.49	83.96	85.09

^{a} $\uparrow$ indicates the rising edge of the switching angle, ^{b} $\downarrow$ indicates the falling edge of the switching angle, ^{c} Initial guessed switching angles.

PWM signal is obtained at the switching nodes as shown in Figure 2.9.

The proposed SHEPWM architecture in SysGen for DSP, fully integrated into MATLAB Simulink, is shown in Figure 3.4. The critical signals within the core are labeled as output port "Out" and these are monitored both in simulation and measurement to ensure the correct operation of the SHEPWM core. The architecture is illustrated in Figure 3.5, detailing the number of MIs and frequencies for better understanding. The architecture can be divided into two major blocks: the configuration block and the computing block. Each block is further divided into sub-blocks, with the bit length of each signal indicated in Figure 3.5. The description of the two major blocks is as follows.

The configuration block: This block reads the input "Data" that the user sends to the FPGA, setting a particular MI and inverter fundamental output frequency. The field Data [3:0] and [7:4] specify different output frequencies and MIs. The reserved Data [13:8] can be used if more output waveform is needed. Enable/disable function of PWMs generation is controlled by Data [14]. Data [15] loads the "Address Counters" through the Finite State Machine (FSM) so that the first switching angle of a specific MI is indexed in "LUT_NCnt". This mechanism allows real-time user-specific MI selection when a new "Data" is sent to the FPGA.

The computing block: This block consists of logic for generating the switching signals PWM1 and PWM2. All calculations in the FPGA are based on fixed-point unsigned arithmetic. The calculated optimal switching angles (α_k) of the first half-cycle (α_1 to α_{2N}) for different MIs are normalized (NCntA/B $= f_{\mathrm{CLK}} \times \alpha_k \,/\, 360°$) to FPGA clock frequency (f_{CLK}) and pre-stored in a dual port LUT, "LUT_NCnt". Up to 16 periods ($T = 1/f_{\mathrm{T}}$) of different inverter AC output signals are stored in another LUT, "LUT_T". The counters AddrA and AddrB are initialized with the first

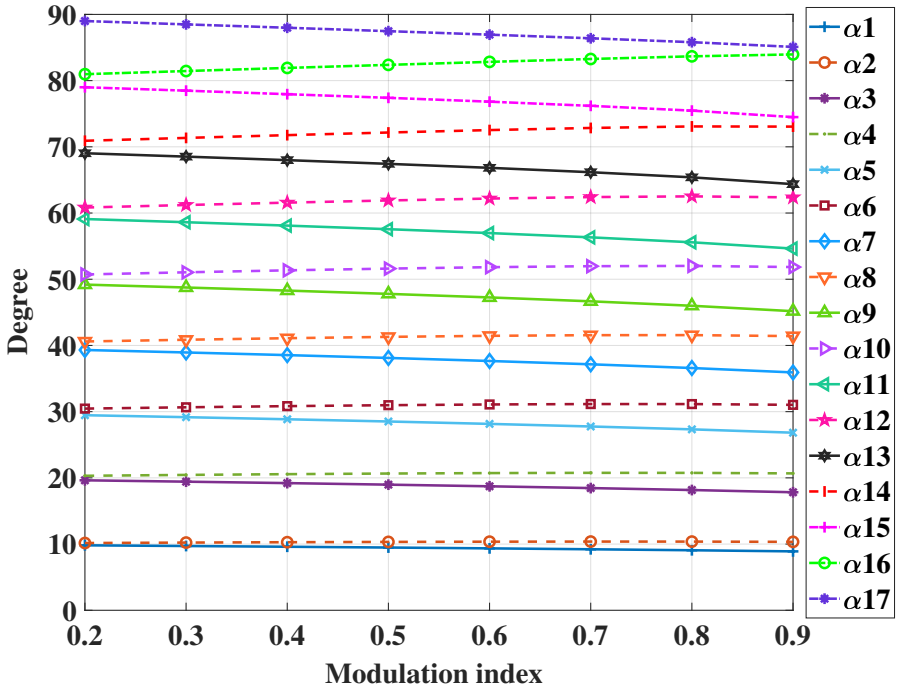


Figure 3.2: The 17 optimal switching angles per quarter-cycle for different modulation indices.

switching angle of a specific MI when "LoadAddr" or "Reset" is asserted then count when their respective enable signals "EnAddrA" and "EnAddrB" are asserted. The "Period" of the inverter output signal from "LUT_T" is multiplied by normalized switching angles to generate the absolute switching angles: ACntA $= T \times$ NCntA, ACntB' $= T \times$ NCntB. As PWM2 is phase shifted by 180° with respect to PWM1, the final absolute switching angles for the second half-cycle (ACntB) are achieved by adding a period-dependent offset to ACntB', which is performed by the sub-block "Offset". This "Offset" block reduces the memory size of "LUT_NCnt" since switching angles from α_{2N+1} to α_{4N} are not stored in the LUT. As the switching angles are normalized to f_{CLK} (200 MHz in this work), the largest number in "LUT_NCnt" is $2{\cdot}10^8$. The outputs of this 2-port LUT require NCntA/B $=$ ceil$(\log_2(f_{\mathrm{CLK}}))$ bits, totaling 28 bits, to represent the normalized switching angles. As a result of the structure in Figure 3.5, the size of LUT_AddrMI, the 2-port LUT_NCnt and the LUT_T are ceil$(\log_2(M{\cdot}2N))$, $M{\cdot}2N{\cdot}$ceil$(\log_2(f_{\mathrm{CLK}}))$ and $N_{\mathrm{f}}{\cdot}$ceil$(\log_2(f_{\mathrm{CLK}}))$ bits respectively, where M is the number of modulation indices and N_{f} is the number of fundamental output frequencies. The total LUT size in Figure 3.5 is 1.98 kB, while the implementation for these experiments,

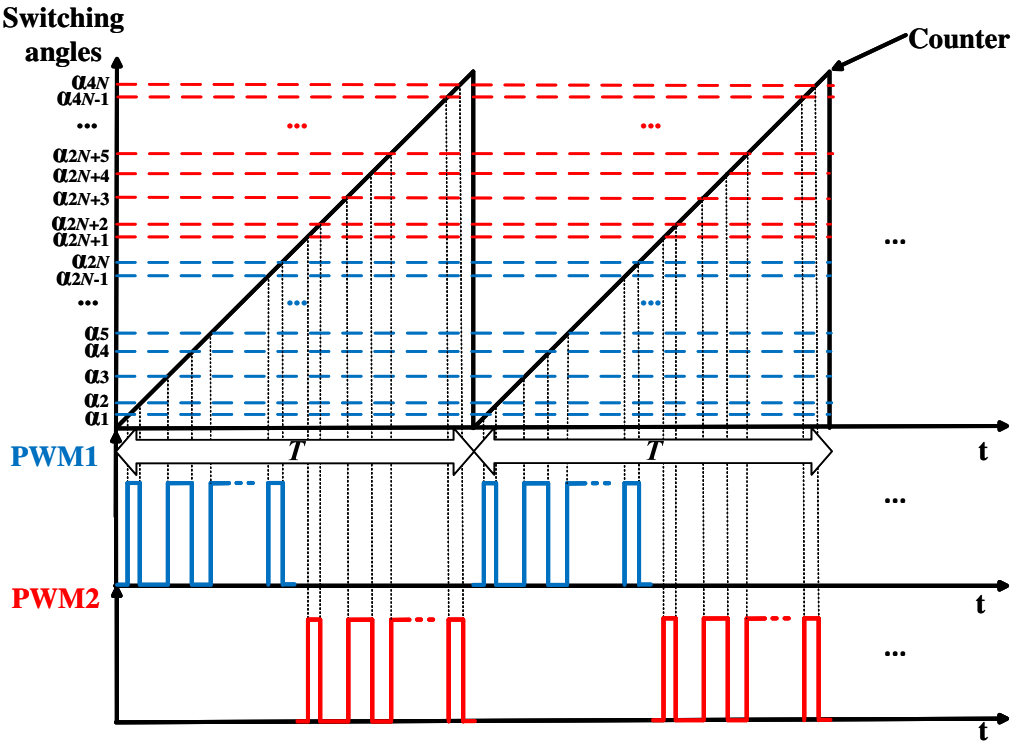


Figure 3.3: Generating the SHEPWM pulses using a counter-based methodology.

with $M = 8$, $N_{\mathrm{f}} = 7$ and $N = 17$, is 0.985 kB.

With the equations provided in Table 3.2, it becomes straightforward to calculate the LUT size when employing different numbers of Modulation indices (M), frequencies (N_f), switching angles (N), or FPGA clock frequencies (f_{CLK}).

In Table 3.1, the switching angles have been pre-computed using MATLAB and the floor method, with deliberate inclusion of an extensive number of decimal points to ensure the precision of the angles, followed by truncation. For simplicity, only two decimal points are shown in the

Table 3.2: Lookup Table (LUT) size of the FPGA architecture in Figure 3.5

LUT	Formula	$M = 16$, $N_{\mathrm{f}} = 16$, $N = 17$ (bits)	Total (bits)
LUT_AddrMI :	$M{\cdot}\mathrm{ceil}(\log_2(M{\cdot}2N))$	16×10	160
LUT_NCnt :	$M{\cdot}2N{\cdot}\mathrm{ceil}(\log_2(f_{\mathrm{CLK}}))$	$16 \times 2 \times 17 \times 28$	15232
LUT_T :	$N_{\mathrm{f}}{\cdot}\mathrm{ceil}(\log_2(f_{\mathrm{CLK}}))$	16×28	488
		Total:	1.98 kB

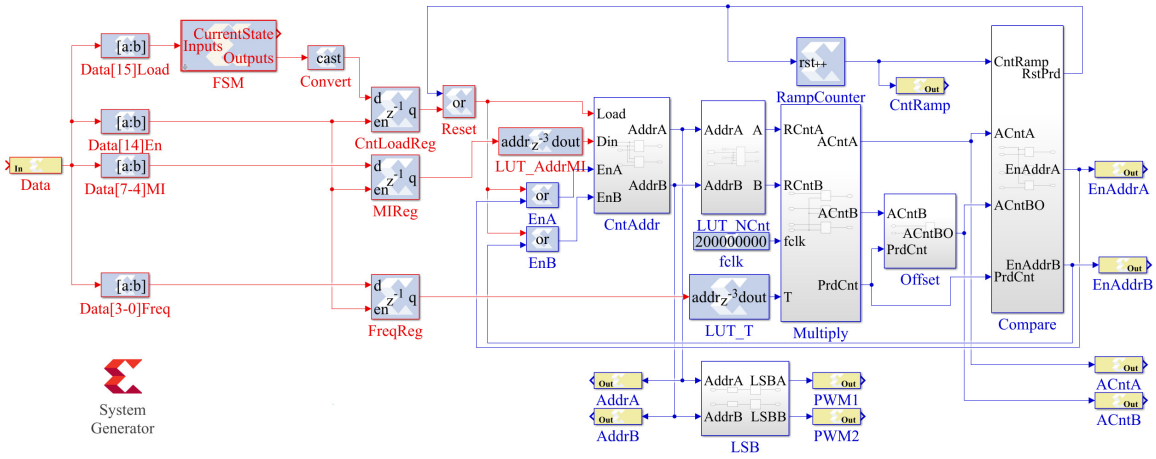


Figure 3.4: The designed SHEPWM core in Xilinx System Generator.

Table 3.3: Lookup Table (LUT) size of the SHEPWM experiment in this work

LUT	Formula	$M = 8$, $N_\mathrm{f} = 7$, $N = 17$ (bits)	Total (bits)
LUT_AddrMI :	$M{\cdot}\mathrm{ceil}(\log_2(M{\cdot}2N))$	8×9	72
LUT_NCnt :	$M{\cdot}2N{\cdot}\mathrm{ceil}(\log_2(f_\mathrm{CLK}))$	$8 \times 2 \times 17 \times 28$	7616
LUT_T :	$N_\mathrm{f}{\cdot}\mathrm{ceil}(\log_2(f_\mathrm{CLK}))$	7×28	196
		Total:	0.985 kB

table. The SHEPWM signal with the lower switching frequency gets more switching angle resolution than the higher switching frequency since f_CLK is fixed in the FPGA. The switching angle resolution in degrees can be calculated as:

$$\Delta\alpha = \frac{360^\circ \times f_\mathrm{T}}{f_\mathrm{CLK}} \tag{33}$$

where f_T is the fundamental output frequency. With $f_\mathrm{CLK} = 200\,\mathrm{MHz}$, the switching angle resolution of the different fundamental output frequencies is given by Table 3.4.

Table 3.4: SWITCHING ANGLE RESOLUTION IN DEGREES FOR DIFFERENT FUNDAMENTAL OUTPUT FREQUENCY

f_T (kHz)	4	5	6	7	8	9	10
Resolution (10^{-3} degree)	7.2	9.0	10.8	12.6	14.4	16.2	18

SysGen simulation results of important signals in the computing block are shown in Figure 3.6.

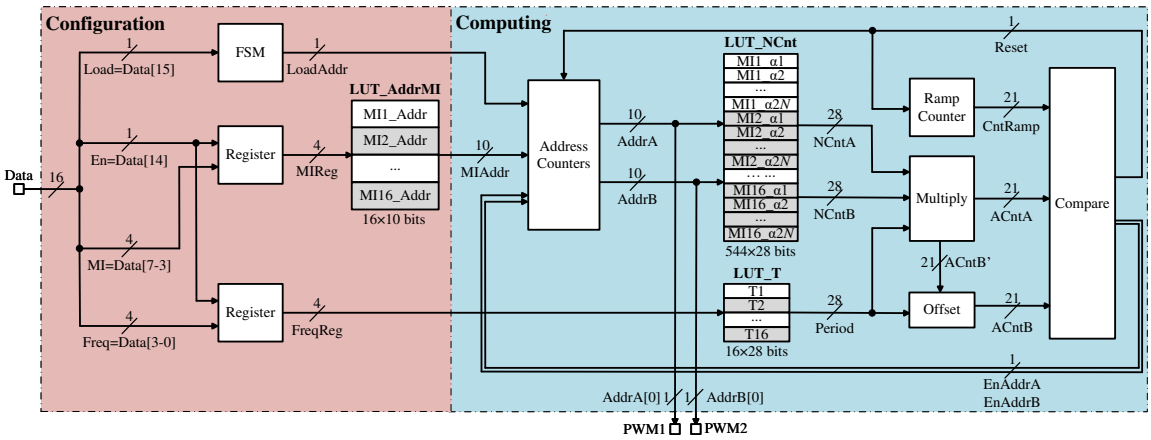


Figure 3.5: The SHEPWM architecture on the FPGA with $M = 16$ MIs and $N_{\mathrm{f}} = 16$ frequencies, employing $N = 17$ switching angles.

A periodic counter's ("Ramp Counter" sub-block) output signal "CntRamp" is compared with the final absolute switching angles "ACntA" and "ACntB" (first-row in Figure 3.6). When they are equal, the comparator triggers "EnAddrA" and "EnAddrB" respectively (second-row in Figure 3.6) so that address of the next switching angle is indexed in "LUT_NCnt" (third-row in Figure 3.6). The signal CntRamp is then compared with the next absolute switching angle. This continues until all the switching angles within the same MI are compared with CntRamp. When the "Ramp Counter" counts to one full inverter output period, which is given by "LUT_T", the comparator output resets the "Ramp Counter" to zero, and loads the "Address Counters" so that the first switching angle of the same MI is indexed in "LUT_NCnt". For example, the first half-period of switching angles of MI = 0.1 occupies the first 34 addresses in "LUT_NCnt", and all the corresponding switching angles of MIs from 0.1 to 0.9 with a step of 0.1 are pre-stored in "LUT_NCnt". If the user sends a new input "Data" to the FPGA with a MI $= 0.9$, then "Address Counters" point to the address index (AI) of 272 $[(9-1) \times 34]$ in "LUT_NCnt". For MI $= 0.9$, the switching angles occupy the AI from 272 to 306 (Figure 3.6).

Finally, the two PWM signals are obtained from the Least-Significant Bit (LSB) of signals AddrA and AddrB (third to fourth-row in Figure 3.6).

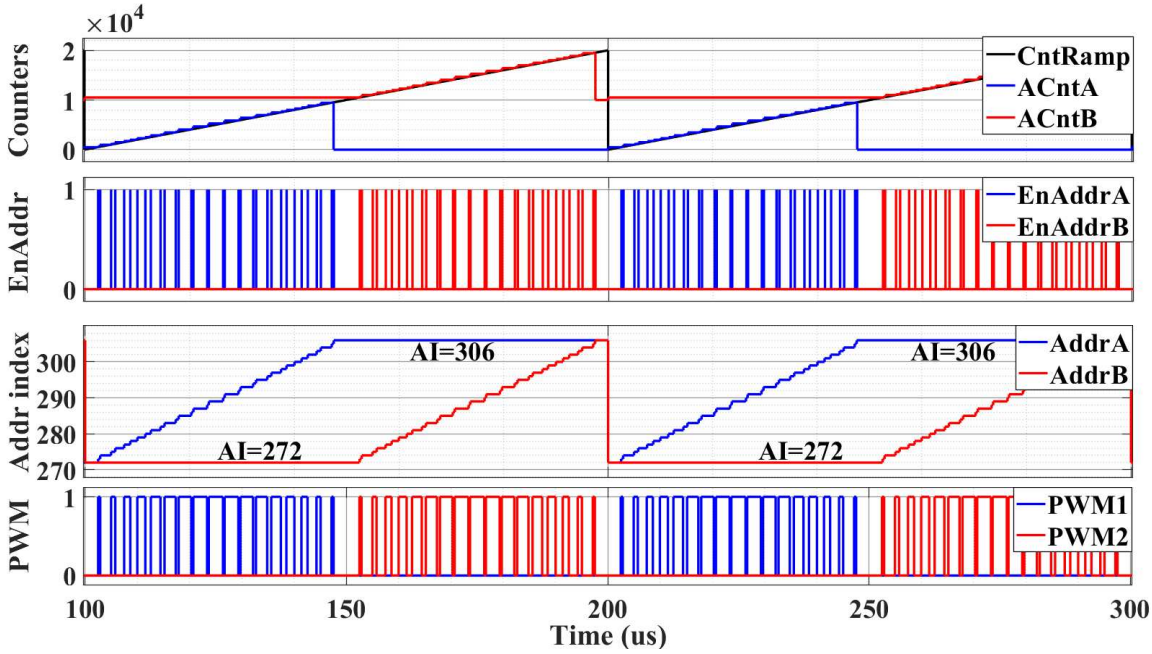


Figure 3.6: SHEPWM simulation showing critical FPGA signals in Figure 3.5.

3.1.2 On-the-Fly Configuration of AC Output Signals

The proposed SHEPWM architecture can configure the PWM output signals on-the-fly, directly from the Personal Computer (PC) commands without reprogramming the FPGA. As a result, a variable output frequency and/or amplitude can be generated at the inverter output. Figure 3.7 shows relevant FPGA signals during on-the-fly configuration. When a reconfiguration command is sent from the PC, the optimal switching angles are applied immediately, while the ramp counter waits for the next peak count to take effect. Consequently, the new waveform, with updated amplitude and frequency, is generated in the next period. Figure 3.8 shows V_{SW}, extracted from PWM1 and PWM2. A second-order Butterworth analog filter with a cut-off frequency of 20 kHz filters V_{SW} to give the differential output signal V_{OUT}.

From t = 0.1 ms to t = 0.87 ms, a waveform with MI = 0.9 and $f_{\mathrm{T}} = 5$ kHz is generated. At t = 0.9 ms the waveform parameters are updated to MI = 0.5 and $f_{\mathrm{T}} = 10$ kHz . Finally at t = 1.7 ms a waveform with MI = 0.7 and $f_{\mathrm{T}} = 7$ kHz is generated. It can be seen in Figure 3.7 (Top) that the higher frequency PWM signal's ramp counter peak is lower than in the case of a lower frequency PWM signal. The third row within Figure 3.7 shows that smaller MI signals occupy lower AI. The

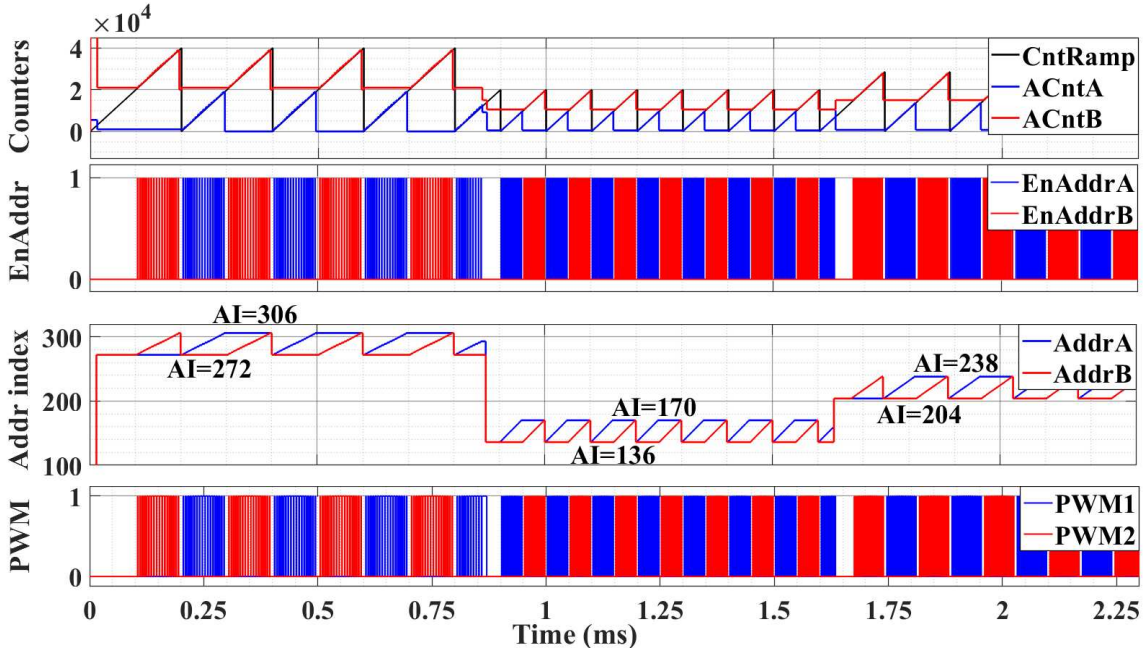


Figure 3.7: FPGA signals during on-the-fly configuration.

discontinuity in the waveform between different MI and output frequency in Figure 3.8 is due to uploading new "Data" information from the MATLAB Graphic User Interface (GUI) and resetting the FSM in the SHEPWM block. Nevertheless, the results show that the on-the-fly configuration of different AC output signals in real-time is achievable with this architecture.

3.1.3 SHEPWM Inverter System Implementation

The overall SHEPWM inverter system implementation is described in this section. Figure 3.9 shows the architecture of the inverter. The system includes the MATLAB GUI, Nexys Video Artix-7 FPGA board, and a custom host PCB. The input "Data" and GD configuration bits are sent from the MATLAB GUI through a Universal Asynchronous Receiver/Transmitter (UART) interface. The SHEPWM block generates two PWMs using a 200 MHz clock signal that gives 5 ns timing resolution of the switching angles. Faster clock frequency means better timing resolution of the switching angles but at the cost of more severe FPGA timing constraints and higher power dissipation. The host PCB includes the auxiliary power systems (not shown in Figure 3.9), an LTCC SiP which consists of digital isolators, two custom-designed reconfigurable GDs Ly et al. (2020) and GaN Field Effect Transistors (FETs) (EPC2012C), and a hybrid second-order LC LPF. The digital isolators

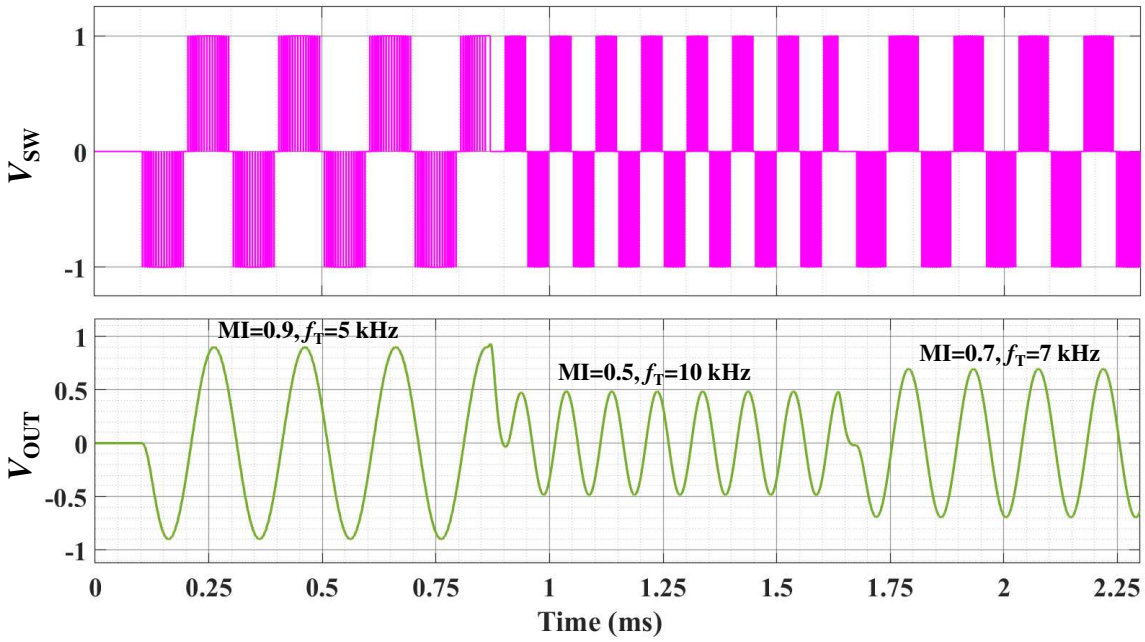


Figure 3.8: The effect of on-the-fly configuration on the amplitude and frequency of the inverter output waveform.

protect the FPGA from any voltage/current spikes from the host PCB that circulates back to the FPGA. They also convert 3.3 V logic signals from the FPGA to 5 V logic for the GDs. Two GDs drive an H-bridge of GaN FETs and generate a three-level differential PWM signal at the switching nodes.

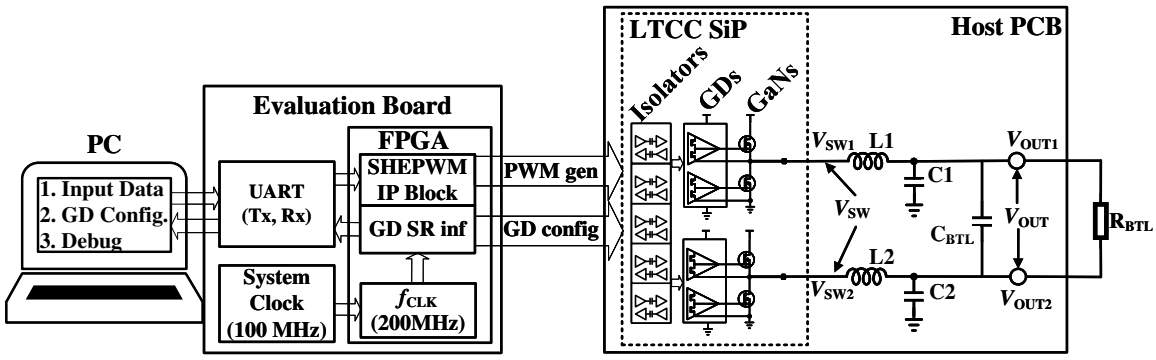


Figure 3.9: The architecture of the SHEPWM inverter.

The highest fundamental output frequency achieved in this work is 10 kHz. Consequently, it is essential for the LC filter's cutoff frequency to exceed this value to prevent attenuation of the output voltage. To ensure robust performance, a cutoff frequency of approximately 20 kHz is selected.

While higher-order LC filters, such as a 4th order, are available, they come at the cost of doubling the size of the current second-order LC filter. Since one of the primary objectives of this work is to minimize the inverter's size, opting for higher-order filters is not favourable. Lower-order filters exhibit a gentler attenuation slope at high frequencies, which, in the context of SHEPWM modulation, exacerbates the issue of uncancelled harmonic power at high frequencies, resulting in increased THD at the output. Therefore, considering both filter size and THD performance, we choose a 2nd order LC filter with a cutoff frequency of approximately 20 kHz as the most suitable option.

Figure 3.10 shows the LTCC SiP in which digital isolators, GDs and GaN FETs are integrated with its size referenced to a Canadian two-dollar coin. The two GD Integrated Circuits (ICs) and some digital isolators on the bottom of the LTCC substrate are located in cavities to reduce the thickness of the SiP. More information about designing the LTCC SiP, its specifications and implementation can be found in Nguyen et al. (2022); Nobert et al. (2021).

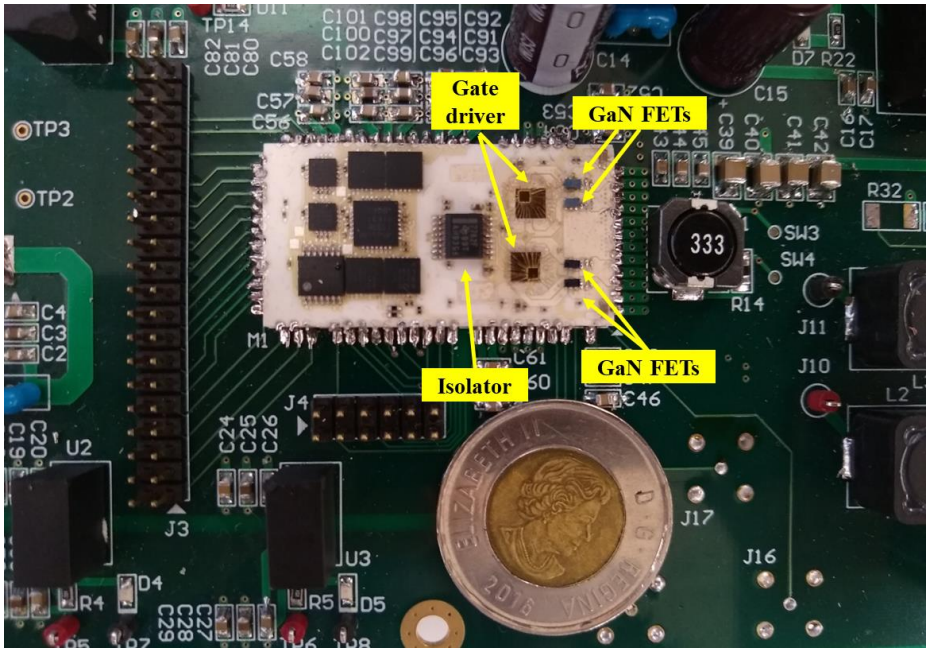


Figure 3.10: LTCC SiP with a Canadian two-dollar coin (diameter=28mm) as a reference.

3.2 Simulation and Experimental Results of Designed SHEPWM Inverter

In this section, the simulation and experimental results of the SHEPWM inverter system are presented. The generated SHEPWM waveform from MATLAB is imported into the LTspice environment (Figure 3.11) in which real component values and models are used. The SHEPWM waveform drives the inputs of the gate driver and the amplified SHEPWM signal at the power stage is filtered out by the LC filter. The SHEPWM inverter was simulated using the conditions given in Table 3.5 with two different loads. The simulated singled-ended switching node voltages (V_{SW1} and V_{SW2}), differential switching node voltage (V_{SW}) and differential output voltage (V_{OUT}) for MI $= 0.9$, $f_{\mathrm{T}} = 10\,\mathrm{kHz}$ are shown in Figure 3.12. It can be seen that a sinusoidal AC output signal with the correct MI and fundamental output frequency (f_{T}) is extracted from the three-level SHEPWM signal.

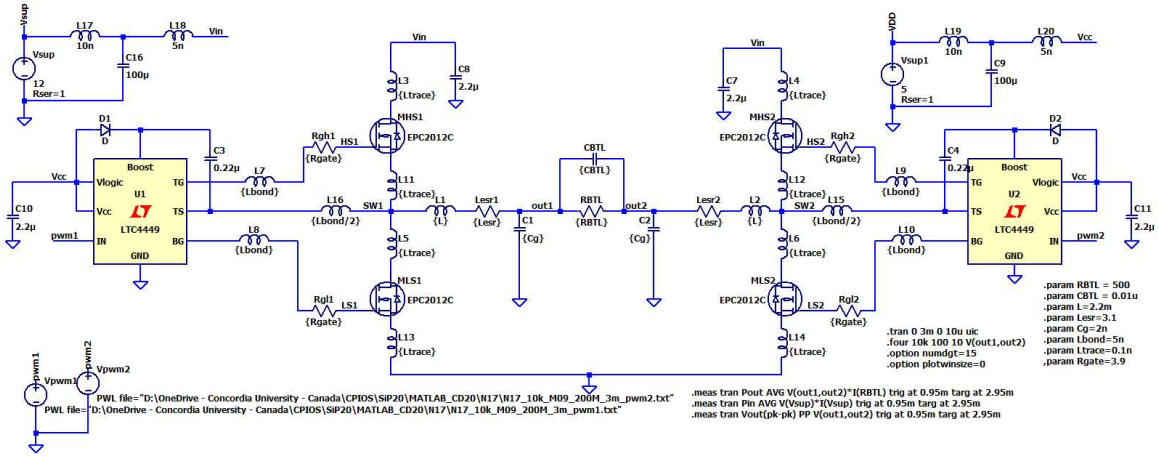


Figure 3.11: SHEPWM inverter output stage schematic in LTspice

The experimental test setup of the SHEPWM inverter is shown in Figure 3.13. Single probes are used to probe the single-ended switching node voltages (V_{SW1} and V_{SW2}) and output voltages (V_{OUT1} and V_{OUT2}). Differential probes are used to probe the differential switching node voltage (V_{SW}) and output voltage (V_{OUT}). Figures 3.15 and 3.16 show the measured output waveforms for these signals. It can seen in Figure 3.15 that there are 17 switching angles per quarter cycle in the measured differential switching node voltage (V_{SW}). In other words, 17 rectangle pulses are

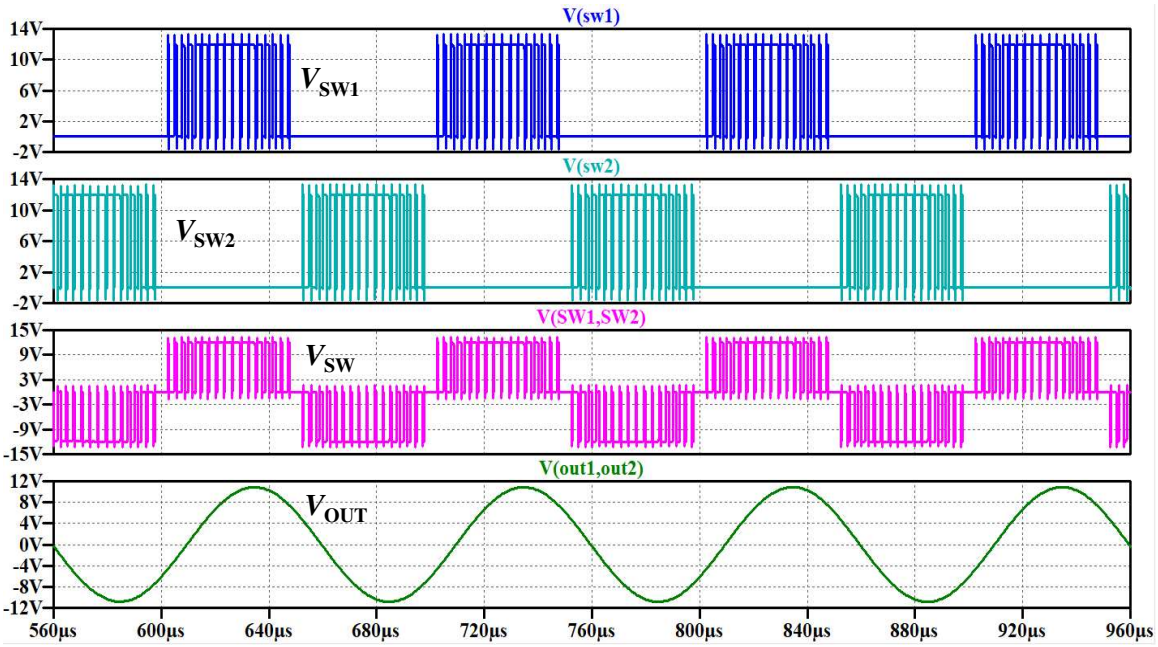


Figure 3.12: Singled-ended switching node voltages (V_{SW1} and V_{SW2}), differential switching node (V_{SW}) and output voltage (V_{OUT}) waveforms from LTspice simulations.

generated in both positive and negative half-periods in V_{SW} with a peak-to-peak value of $24\,\mathrm{V}$. The measured differential output voltage (V_{OUT}) has amplitude of approximately $21.3\,\mathrm{V}$ and frequency of $10\,\mathrm{kHz}$, which matches the simulation results in Figure 3.12.

The frequency spectrum of the measured switching node voltage (V_{SW}) is given in Figure 3.17, where each harmonic's power is normalized to the fundamental harmonic's power. The fundamental output frequency (1^{st} harmonic) in this measurement is $10\,\mathrm{kHz}$. It can be seen from the figure that lower-order harmonics up to 34 are suppressed as expected. Some lower-order harmonics are not fully eliminated due to timing errors introduced in the SHEPWM signal by the GD and power transistors, however, their power is very low compared to the fundamental's power as shown in Table 3.6, in which the first 50 harmonics' normalized power is given.

The SHEPWM inverter's output THD is measured according to the equation below:

$$\mathrm{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_i^2}}{V_1} \tag{34}$$

where V_i is the RMS value of the i^{th} harmonic voltage. The output THD and its relationship between

Table 3.5: SHEPWM INVERTER TEST CONDITIONS

Parameters	Values
DC input voltage (V_{IN})	$12\,\mathrm{V}$
Supply voltage for gate driver IC	$5\,\mathrm{V}$
Modulation index (MI)	$0.2 - 0.9$
Output voltage range (peak to peak)	$4.8\,\mathrm{V} - 21.6\,\mathrm{V}$
Fundamental output frequency (f_{T})	$4\,\mathrm{kHz} - 10\,\mathrm{kHz}$
Bridge tied loads ($\mathrm{R_{BTL}}$)	$50\,\Omega/500\,\Omega$
Bridge tied capacitors ($\mathrm{C_{BTL}}$)	$0.1\,\mu\mathrm{F}/0.01\,\mu\mathrm{F}$
Gate driver dead time	$35\,\mathrm{ns}$
Inductors L1, L2	$270\,\mu\mathrm{H}/2.2\,\mathrm{mH}$
DC resistance of L1, L2	$0.248\,\Omega/3.1\,\Omega$
Capacitors C1, C2	$47\,\mathrm{nF}/2\,\mathrm{nF}$

MIs and fundamental output frequencies are shown in Figure 3.18a. The results show that the THD is low for high MI and output frequencies, and it increases gradually with decreasing MI and output frequency. This can be explained by the high power of the harmonic immediately after the cancelled harmonics (35^{th} harmonic in Figure 3.17), which is suppressed by the LPF more for higher output frequencies since the filter's cut-off frequency is fixed at $20\,\mathrm{kHz}$. For small MI SHEPWM, more power is concentrated in the harmonics after the cancelled harmonics. With a faster FPGA clock frequency (Eq. (33)), the angle resolution gets better at smaller MI and THD at the output can be further reduced but at the cost of more hardware resources and accurate digital logic timing control. Overall, THD is equal or lower than 5.1% for MI 0.2 to 0.9 and output frequency from $5\,\mathrm{kHz}$ to $10\,\mathrm{kHz}$ (THD $= 5.08\%$ for MI $= 0.2$ and $f_{\mathrm{T}} = 5\,\mathrm{kHz}$). The THD difference at the inverter output between simulation and measurement for different MI and the fundamental output frequency is given in Figure 3.18b in which the simulated THD is lower than the measured one. The THD difference is larger in the regions of smaller MI and larger output frequencies. This is because short pulses with a fast-switching frequency at the switching node are more sensitive to timing errors. From the figure, it can be seen that the THD difference is less than 1% for most of the region, and MI degrades the measured THD more than the output frequency.

Although the higher switching frequency SHEPWM signal exhibits a lower switching angle resolution (Table 3.4), its output THD is lower compared to the lower switching frequency SHEPWM

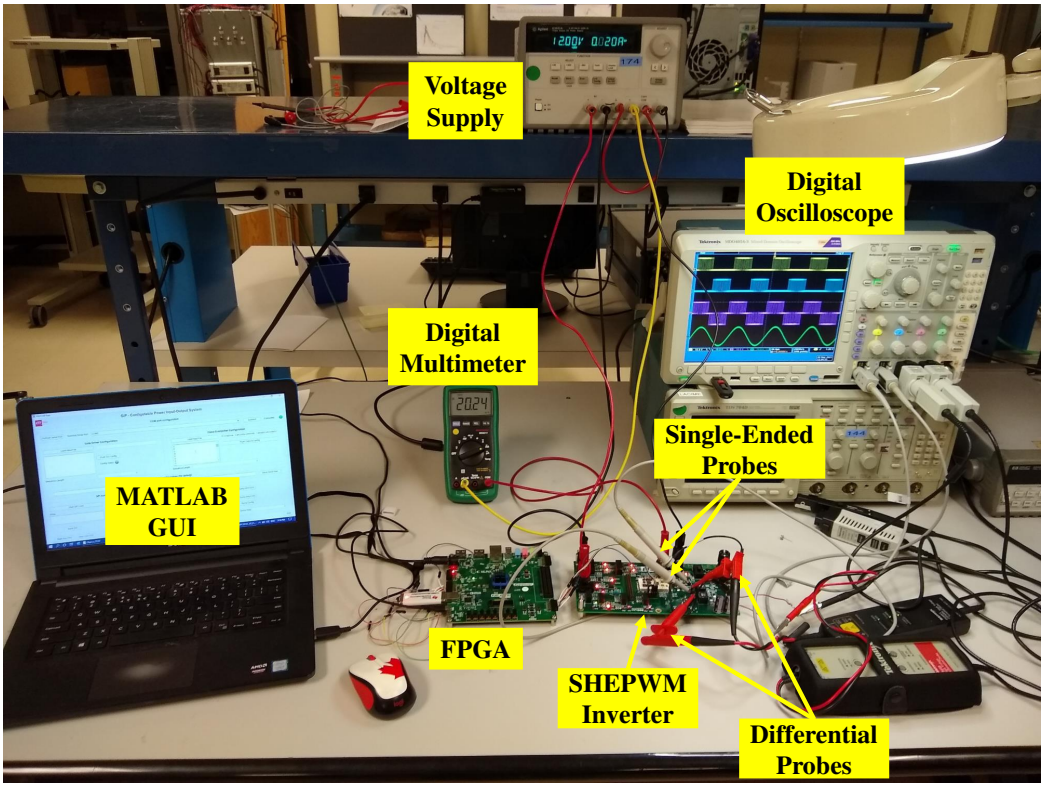


Figure 3.13: SHEPWM inverter experimental test setup.

signals. Consequently, the degradation in THD for lower output signals cannot be attributed primarily to the switching angle resolution. Even when adopting SHEPWM in a closed-loop control to achieve the ideal switching angles, the enhancement in THD output is almost insignificant. The THD degradation is primarily due to the fixed cutoff frequency of the LC low-pass filter, where higher switching frequency SHEPWM signals attenuate high-order harmonics more compared to lower switching frequency SHEPWM signals.

The power efficiency of the SHEPWM inverter is measured according to the equation below:

$$\eta = \frac{V_{\mathrm{OUT(RMS)}} \times I_{\mathrm{OUT(RMS)}}}{V_{\mathrm{IN}} \times I_{\mathrm{IN(AVE)}}} \tag{35}$$

where $V_{\mathrm{OUT(RMS)}}$ and $I_{\mathrm{OUT(RMS)}}$ are the RMS values of the differential output voltage and current, V_{IN} is the inverter DC input voltage, and $I_{\mathrm{IN(AVE)}}$ is the average input current of the inverter. The inverter's efficiency is simulated and compared to an NPWM inverter.

Figure 3.19 shows the power efficiency of the inverter for different output power, where dashed

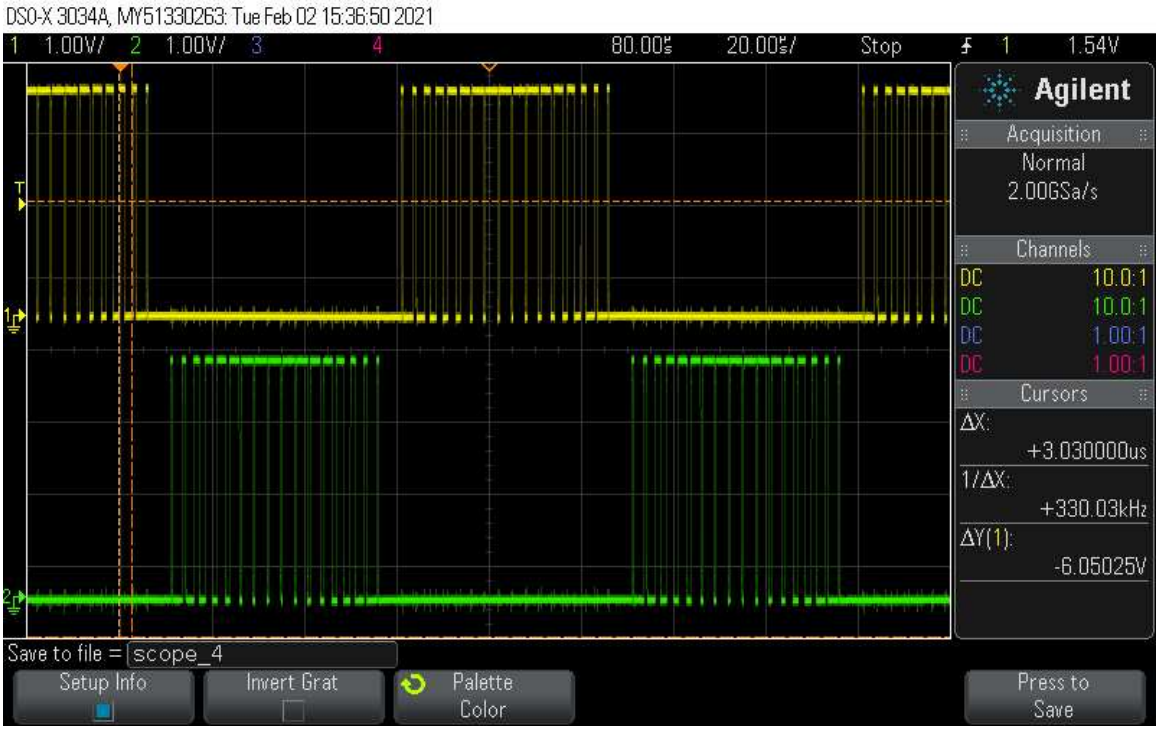


Figure 3.14: SHEPWM signals from FPGA for MI = 0.9 and $f_{\mathrm{T}} = 10\,\mathrm{kHz}$.

lines are for simulated efficiency and solid lines are for measured efficiency. For the same inverter conditions and output THD, the SHEPWM inverter has better efficiency than NPWM. The results showed that at fundamental output frequencies of $4\,\mathrm{kHz}$, $7\,\mathrm{kHz}$, and $10\,\mathrm{kHz}$, the SHEPWM inverter, with an output power of $0.12\,\mathrm{W}$, exhibited an average efficiency improvement of 17.3%, 11.7%, and 4.2% over the NPWM inverter, respectively. Conversely, when the output power was increased to $1.2\,\mathrm{W}$, the efficiency advantage of SHEPWM, while slightly reduced, remained notable, with an average improvement of 2.3%, 6.2%, and 6.9%, respectively.

For the SHEPWM inverter, the switching frequency at the switching node is scaled with the fundamental output frequency since there are fixed 34 rising/falling edges per one sine-wave cycle. However, there is no fixed switching period for the SHEPWM signal, and the switching frequency is instead a quasi-switching frequency. That is, for a $10\,\mathrm{kHz}$ fundamental output frequency, the switching node has a $340\,\mathrm{kHz}$ quasi switching frequency, and for the $7\,\mathrm{kHz}$ and $4\,\mathrm{kHz}$ fundamental output frequency, the quasi switching frequency is $238\,\mathrm{kHz}$ and $136\,\mathrm{kHz}$ respectively. One thing is clear that the switching losses happen during the finite rising/ falling time (where GaN FETs'

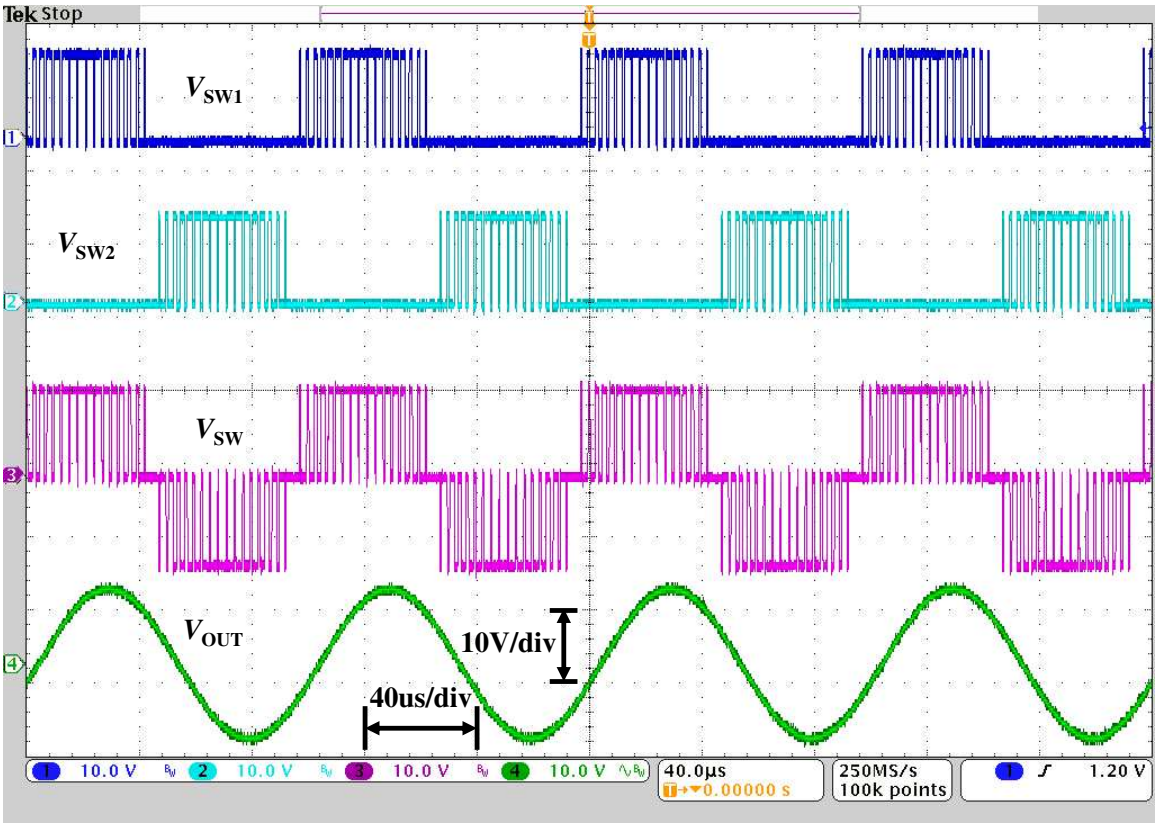


Figure 3.15: Measured single-ended switching node voltages (V_{SW1} and V_{SW2}), differential switching node (V_{SW}) and output voltage (V_{OUT}) waveforms for MI = 0.9 and $f_{\mathrm{T}} = 10\,\mathrm{kHz}$.

drain-source voltage and current overlap), and the rising/falling edges count can be compared with NPWM. For the same inverter conditions and output THD, the NPWM inverter has a switching frequency of 370 kHz, 256 kHz and 148 kHz for the fundamental output frequency of 10 kHz, 7 kHz and 4 kHz, respectively. This implies that the SHEPWM exhibits lower switching activity compared to the NPWM, resulting in reduced switching losses dissipated in the SHEPWM.

For the same output power ($V_{\mathrm{OUT(RMS)}} \times I_{\mathrm{OUT(RMS)}}$), SHEPWM and NPWM have the same conduction loss ($P_{\mathrm{con}} = I^2_{\mathrm{OUT(RMS)}} \times R_{\mathrm{PATH}}$), where R_{PATH} is the path resistance from input supply to output voltage, including the GaN FET's turn on resistor ($R_{\mathrm{DS(ON)}}$), inductor series resistance, and any parasitic resistance in the path. The rest of the power losses come from the switching losses, which are proportional to the switching frequency of the inverter. These switching losses include but are not limited to switching loss due to the finite turning on/off time of the power transistors, gate charge loss due to charging and discharging of the gate capacitance of the power

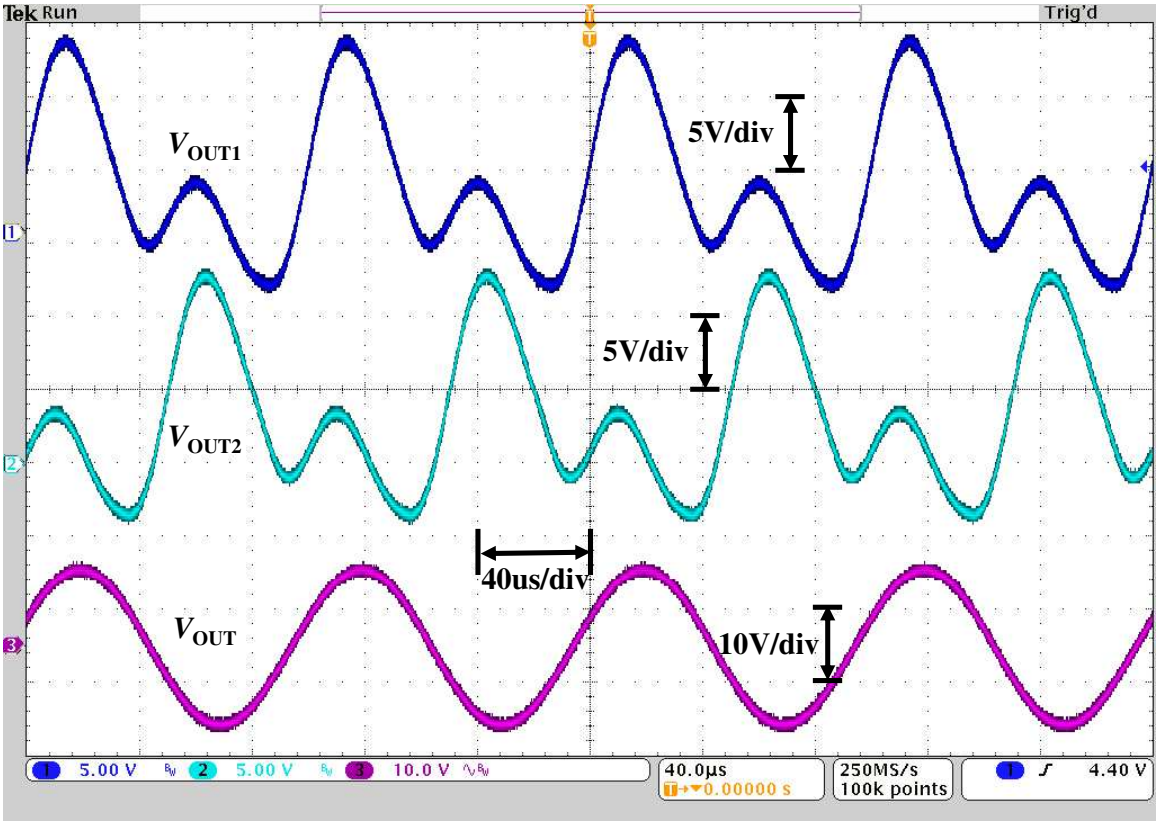


Figure 3.16: Measured inverter single-ended (V_{OUT1} and V_{OUT2}) and differential (V_{OUT}) output signals for MI = 0.9 and $f_{\mathrm{T}} = 10\,\mathrm{kHz}$.

transistors, dead-time loss due to the freewheeling conduction loss of the body diode of the power transistors, and some power loss due to the ripple current on the inductor. Therefore, to achieve lower THD than SHEPWM, NPWM would need to operate at an even higher switching frequency, incurring more switching losses that could degrade the overall inverter efficiency.

For the SHEPWM inverter, the efficiency is higher for the lower output frequency since the switching frequency at the switching node is scaled with the fundamental output frequency. The measured efficiency is less than the simulated efficiency, and the difference in efficiency is obvious for small output power but decreases for large output power. This can be attributed to the predominant switching losses at lower output power levels, and it is possible that the model accuracy of the gate driver and GaN FETs may not be optimal. Also, calculating the exact switching losses is almost impossible because the effect of the parasitic inductive components significantly alters the

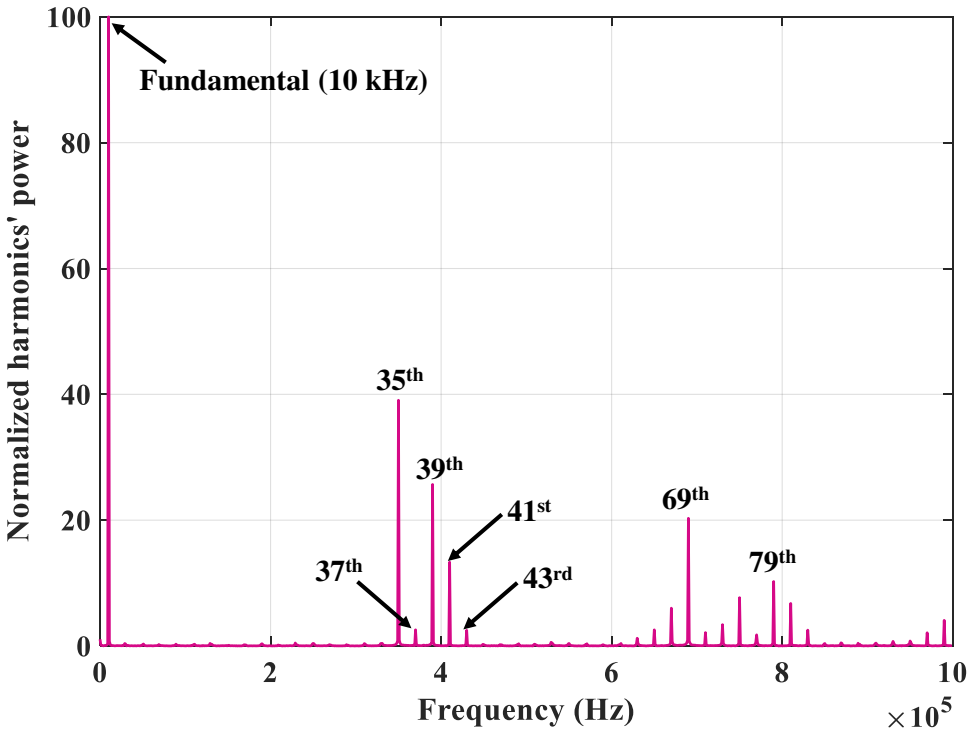


Figure 3.17: Spectrum of the measured differential switching node voltage (V_{SW}).

current and voltage waveform, as well as the switching times during the switching process. In addition, variables such as GaN FET capacitor values, gate threshold voltage, driver output impedance, and others introduce uncertainty in the calculation of switching losses in the GaN FET.

Another observation from Figure 3.19 is the efficiency advantage of SHEPWM over NPWM is large for the low-power inverter but reduced for the high-power inverter. There are two reasons for this. One is as the power increases, the conduction loss increases. Hence, the switching losses from less switching activity from SHEPWM are insignificant. Secondly, SHEPWM consistently operates in hard-switching mode, whereas NPWM incorporates a partial soft-switching mechanism. Soft-switching is known for its higher efficiency compared to hard-switching. As the load current increases, the dominance of soft-switching becomes more pronounced in NPWM. In SHEPWM the switching node has a switching activity when there is only a current going out of the switching node, and there is no switching activity when there is a current going into the switching node (Figure 3.15). On the other hand, in NPWM there is continuous switching activity on both switching

Table 3.6: POWER OF THE HARMONICS OF THE DIFFERENTIAL SWITCHING NODE VOLTAGE (V_{SW})

Harmonic	Normalized Power	Harmonic	Normalized Power	Harmonic	Normalized Power	Harmonic	Normalized Power	Harmonic	Normalized Power
1	100	11	0.25	21	0.09	31	0.39	41	13.32
2	0.07	12	0.01	22	0.03	32	0.05	42	0.03
3	0.32	13	0.26	23	0.22	33	0.41	43	2.49
4	0.02	14	0.01	24	0.01	34	0.08	44	0.04
5	0.24	15	0.07	25	0.42	35	39.06	45	0.23
6	0.05	16	0.05	26	0.04	36	0.08	46	0.04
7	0.12	17	0.15	27	0.16	37	2.57	47	0.03
8	0.01	18	0.03	28	0.01	38	0.13	48	0.01
9	0.16	19	0.36	29	0.08	39	25.67	49	0.14
10	0.02	20	0.02	30	0.03	40	0.03	50	0.05

*Fundamental frequency is 10 kHz; Each harmonic's power is normalized to the 1st harmonic. The DC harmonic's normalized power is 1.07.

nodes. For half of the sine-wave cycle, the current flows out of the switching node, indicating hard-switching. During the other half-cycle, the current flows into the switching node, charging the output capacitance of the GaN FET. This contributes to the rising of the switching node during dead-time. After the dead-time concludes, the remaining rise of the switching node is attributed to the gate driver pulling up, which consumes power. With increasing load current, the output capacitor charges more rapidly, leading to reduced power consumption from the gate driver Ma et al. (2015).

We observed the one-side half-bridge waveforms for both SHEPWM and NPWM at low output power, plotted in Figure 3.20 and Figure 3.21. Positive current indicates inductor current flowing out of the half-bridge, while negative current denotes current flowing into the half-bridge. From the SHEPWM waveforms, we observed switching activities only during the half-cycle when inductor current flows out of the half-bridge, indicating purely hard-switching. No switching activity occurs during the other half-cycle when the inductor current flows into the half-bridge; the switching node voltage remains low, indicating no switching losses during this period. Only conduction losses result from the inductor series resistance and the low-side power transistor turn-on resistance ($R_{DS(ON)}$). Similar waveforms can be observed for the other half-bridge, confirming that SHEPWM involves only hard switching.

In NPWM, however, switching activities occur both when inductor current flows out and into the half-bridge. When the inductor current flows out of the half-bridge, hard-switching is involved,

whereas, when it flows into the half-bridge, partial soft-switching occurs. Figure 3.22 presents enlarged waveforms of NPWM when the inductor current reaches its negative peak value. As depicted, the switching node voltage rises to 0.3 V at the end of the dead-time. The subsequent rise from 0.3 V to 12 V (input voltage V_{IN}) results from the high-side power transistor turning on. Figure 3.23 illustrates the same waveforms at high output power, nearing the peak value of negative inductor current. Here, the switching node voltage rises to 7.5 V at the end of the dead-time, consuming no switching loss. The remaining rise from 7.5 V to 12 V is attributed to the high-side power transistor turning on, consuming minimal power. It's important to note that the inductor current is a sine wave, and this partial soft-switching diminishes as the negative inductor current amplitude decreases, eventually becoming hard-switching when the inductor current becomes positive.

Although the proposed SHEPWM architecture demands a higher memory footprint due to the storage of precomputed switching angles across multiple modulation indices and output frequencies, its runtime computational complexity remains comparatively low. In NPWM, a continuous sinusoidal reference must be generated (e.g., using a CORDIC block or a sine LUT), and a high-frequency carrier waveform is compared with the reference in real time, requiring frequent comparisons and arithmetic operations. When modulation parameters such as amplitude or frequency vary dynamically, additional computation is needed to scale or adjust the reference waveform accordingly. In contrast, all heavy computation in the SHEPWM approach—namely solving transcendental equations for switching angles—is performed offline. During runtime, the modulation process is carried out by simply reading the angle values from look-up tables and comparing them with a ramp counter, without requiring any real-time trigonometric evaluation or waveform synthesis. Hence, while SHEPWM involves greater memory usage and slightly more logic for configuration and LUT addressing, it avoids the continuous arithmetic operations characteristic of NPWM As a result, the steady-state operation of the SHEPWM architecture incurs no significant computational overhead compared to NPWM.

This work is compared with other recent works based on the power stage structure, the number of switching node voltage levels, DC bus voltage(s), MI range, fundamental output frequency, transitions per quarter period, and capability of configuring the AC outputs on-the-fly, as shown in Table 3.7. For a multilevel cascaded H-Bridge topology, more than one isolated DC source is

required. Depending on the topology, voltage level and switching angle numbers, multilevel inverters' MIs may or may not be continuous in the full range of MI. For discontinuous MI, there is no solution for the optimal switching angles in some regions of MI, therefore, the inverter cannot generate an output voltage with the specific amplitude. Works in Yang et al. (2017) and M. Wu et al. (2020) have discontinuous MI ranges and only minimum and maximum MIs are given in Table 3.7. In Ahmed et al. (2017), an on-the-fly configuration of output amplitude is presented but at the cost of complex online computation of real-time switching angles. The proposed method in this article is simple, cost-effective, and has the capability of on-the-fly configuration of both inverter output amplitude and frequency. It is worth noting that the fundamental SHEPWM technique detailed in this work can be readily extended to high-power converters operating with kilowatt range. This extension primarily involves increasing the input voltage for power transistors and adjusting the LC filter component values (ensuring that the power rating of the power transistors and LC filter components are suitable for the kilowatt range) to meet the specific requirements of higher power levels.

Table 3.7: COMPARISON TO OTHER WORKS

	Power stage structure	Voltage levels	DC bus voltage	Modulation index (MI)	Fundamental output frequency (f_T)	Transitions per quarter period	On-the-fly config of AC outputs
Yang et al. (2017)	Cascaded H-Bridge	13	18×15 V	0 – 3.4 (discontinuous)	50 Hz	9	No
Yang et al. (2015)	H-Bridge	3	100 V	0 – 0.83 (continuous)	50 Hz	8	No
M. Wu et al. (2020)	Hybrid-clamped	4	150 V	0 – 1.15 (discontinuous)	50 Hz	7	No
Perez-Basante et al. (2020)	Module Multilevel	-	200 V	0.1 – 1 (continuous)	50 Hz	17	No
Zhao et al. (2016)	Cascaded H-Bridge	7	3×50 V	1.65 – 2 (continuous)	60 Hz	3	No
Ahmed et al. (2017)	Cascaded H-Bridge	7	3×40 V	0.1 – 1.04 (continuous)	50 Hz	3	Yes (MI only)
Buccella et al. (2023)	Cascaded H-Bridge	33	150 V	0 – 0.9678 (continuous)	47 – 63 Hz	N/A	No
Kala, Sharma, Jately, Joshi, and Yang (2024)	Cascaded H-Bridge	11	5×12 V	0.45 – 0.845 (discontinuous)	50 Hz	5	Yes (MI only)
This work	H-Bridge	3	12 V	0.2 – 0.9 (continous)	4 – 10 kHz	17	Yes (MI and f_T)

3.3 Conclusions

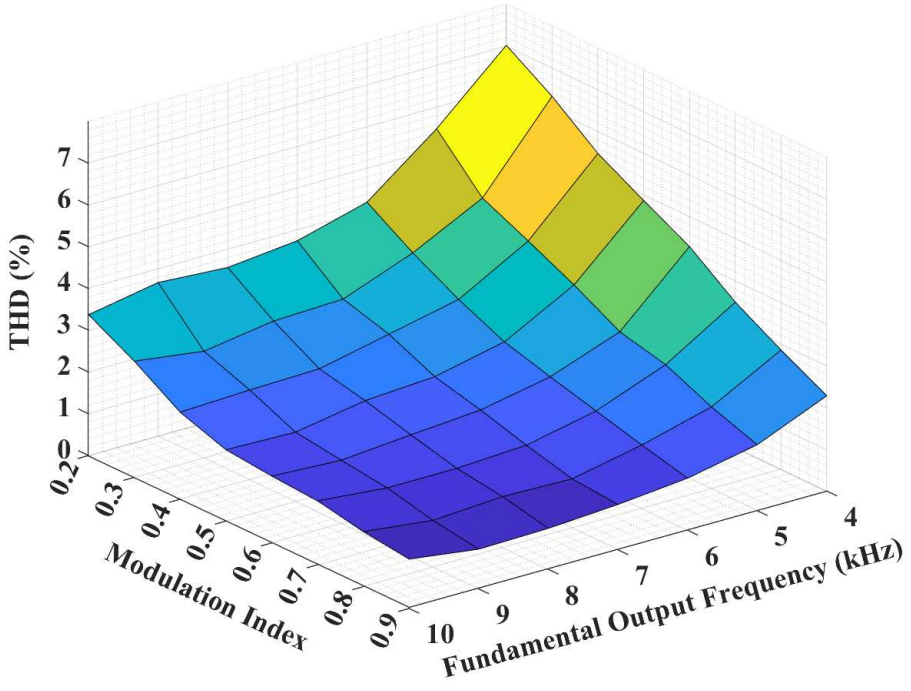
In this work, a full-bridge low-power inverter design is presented through the utilization of an open-loop configuration combined with a novel FPGA hardware implementation. Firstly, a low-power Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) inverter operating at

high fundamental output frequencies ranging from $4\,\mathrm{kHz}$ to $10\,\mathrm{kHz}$ is showcased. This work diverges from the conventional focus on high-power applications with fixed, low-output frequencies of $50\,\mathrm{Hz}$ or $60\,\mathrm{Hz}$, offering a novel perspective on the application of SHEPWM in low-power systems. Importantly, this research is the first to investigate and address the challenges associated with achieving high-efficiency operation across a wide frequency range while maintaining a fixed filter cutoff frequency.

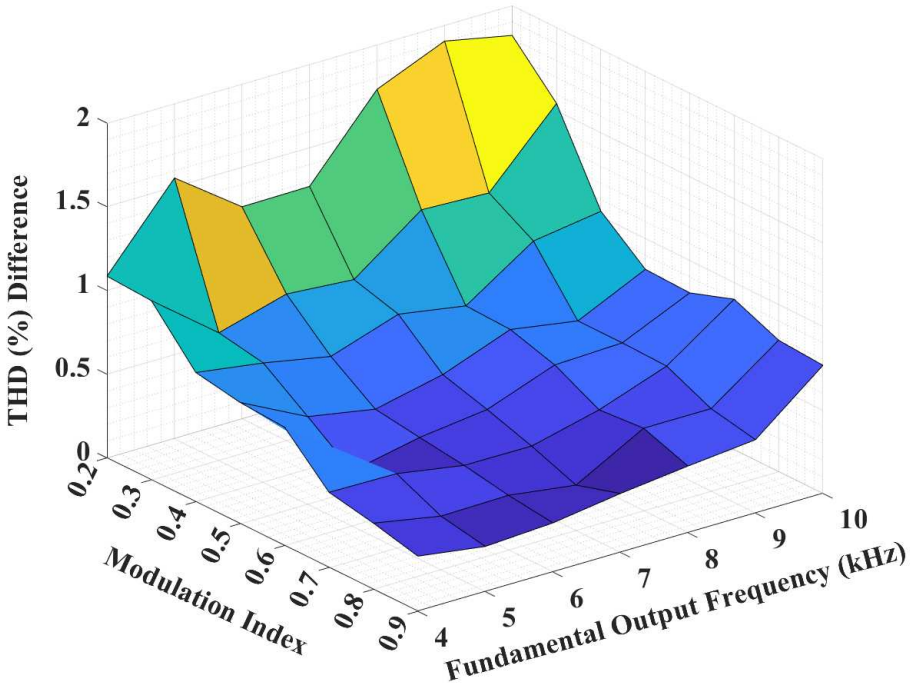
Secondly, a unique FPGA-based architecture implementing the SHEPWM algorithm is introduced, marking a key innovation in this field. This architecture supports on-the-fly configurability of the inverter output, enabling dynamic adjustment of both amplitude and fundamental frequency in real time. Unlike traditional approaches that rely on fixed configurations or computationally intensive methods, this architecture achieves adaptability without excessive storage or complex calculations. This flexibility not only enhances the versatility of the SHEPWM algorithm but also addresses practical constraints in low-power applications, making it a robust solution for diverse operating conditions.

Furthermore, the integration of compact 3D components within a SiP demonstrates the potential for significant reductions in PCB area. This SiP design serves as a dual-purpose solution, capable of supporting both DC-AC inversion and DC-DC conversion. While the current implementation utilizes only a subset of the SiP components, this work highlights the potential for developing even more compact and efficient SiP designs with a minimized PCB footprint, paving the way for future advancements in integrated power electronics.

In summary, this work not only broadens the applicability of SHEPWM to low-power systems with wide-frequency operation but also introduces a new innovative architectural design and SiP integration strategies. These contributions collectively advance the state-of-the-art in inverter design, offering a unique and versatile solution for next-generation low-power industry applications.

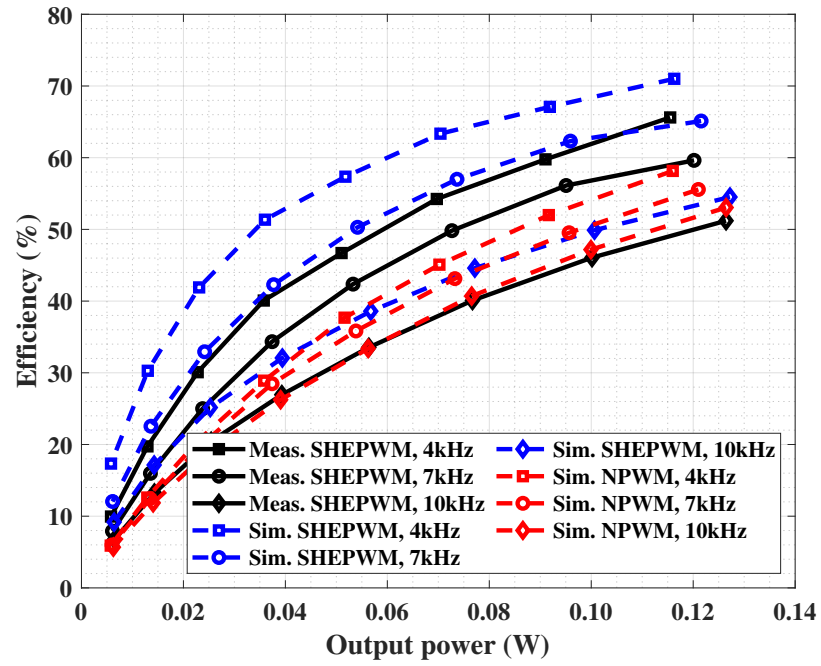


(a)

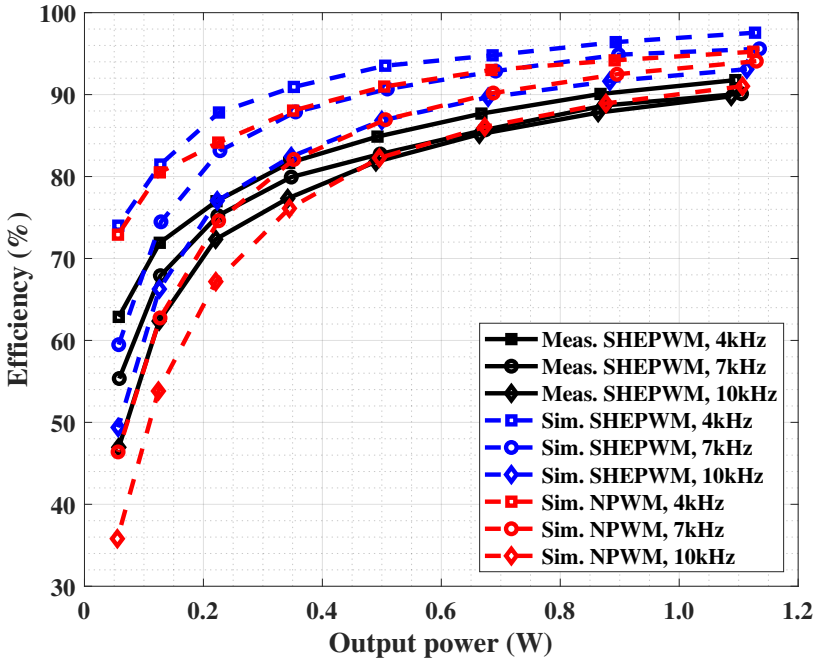


(b)

Figure 3.18: (a) Measured THD versus different modulation indices and output frequencies, (b) THD difference between simulation and measurement.



(a)



(b)

Figure 3.19: Power efficiency comparisons of the SHEPWM and NPWM inverters for the same output THD (a) P_{out}=0.12 W, (b) P_{out}=1.2 W.

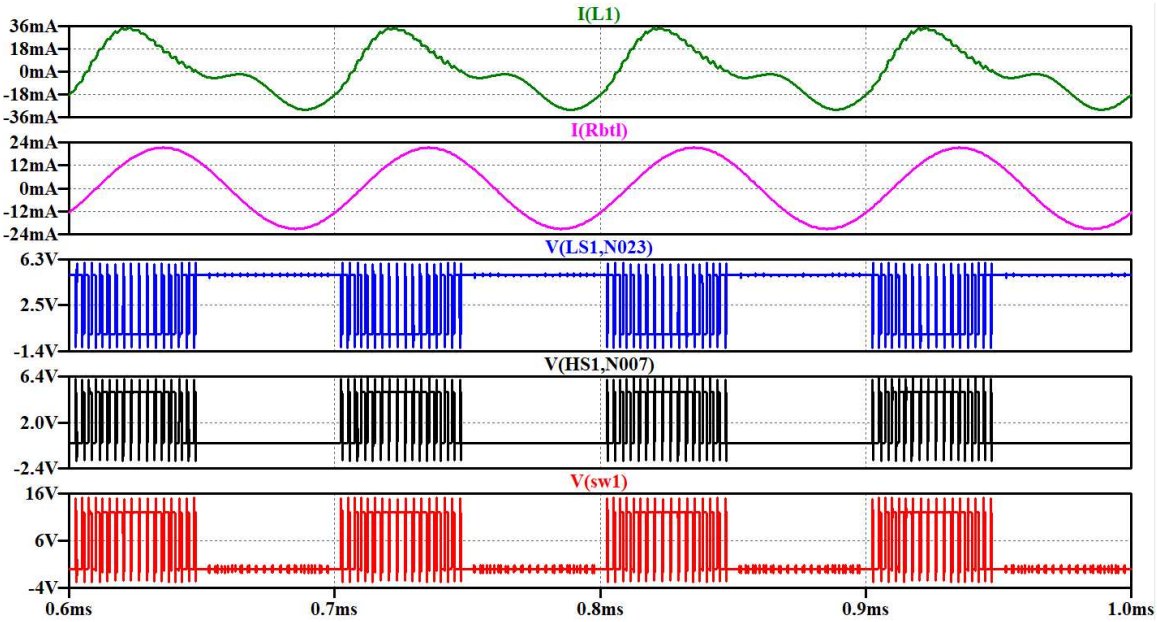


Figure 3.20: SHEPWM inverter waveform showing one branch inductor and load current, high and low side gate-source voltages, and switching node voltage

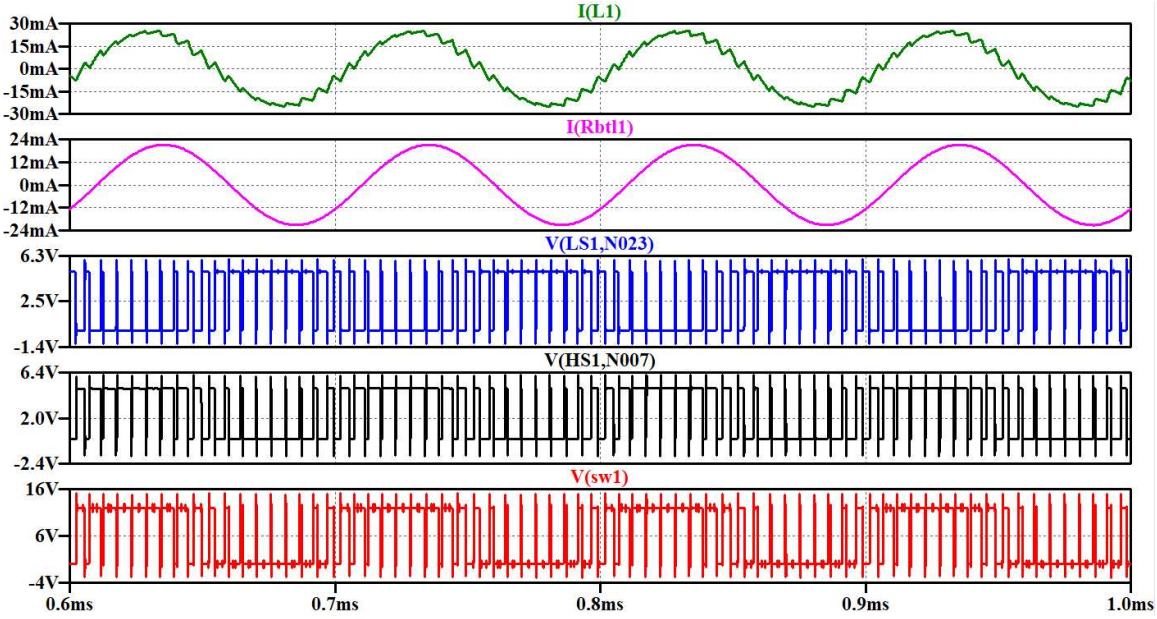


Figure 3.21: NPWM inverter waveform showing one branch inductor and load current, high and low side gate-source voltages, and switching node voltage

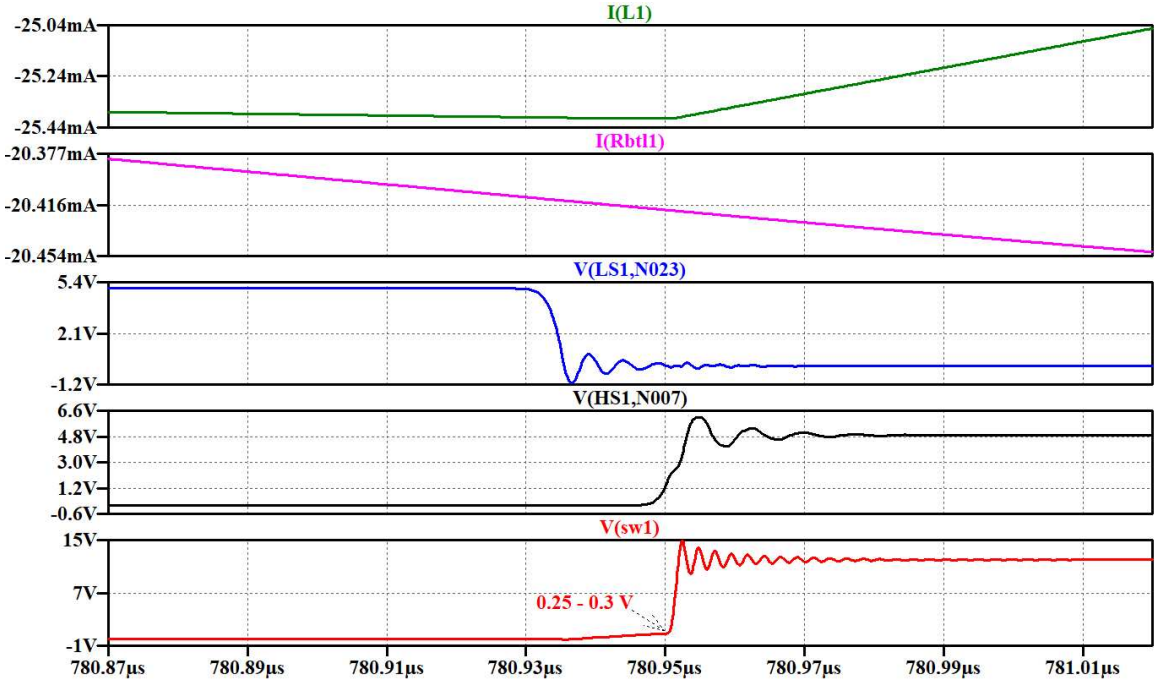


Figure 3.22: NPWM inverter in light load: negative inductor current contributing to the rising of switching node voltage during dead-time

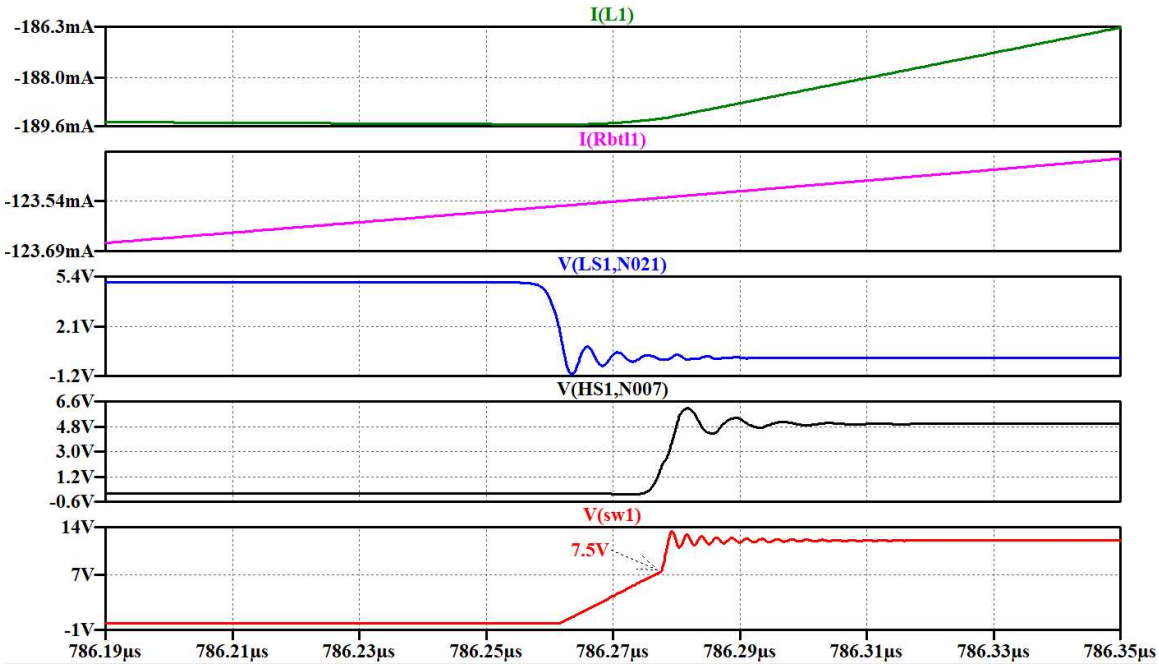


Figure 3.23: NPWM inverter in heavy load: negative inductor current contributing to the rising of switching node voltage during dead-time

Chapter 4

Discrete DISMC for a Class-D Amplifier

Sliding mode control (SMC) is a robust control technique widely employed in systems characterized by nonlinearity, parameter variations, and external disturbances. The core principle of SMC lies in driving the system states to a designed sliding surface, where they are then maintained by the inherent robustness of the control law. While SMC has traditionally been implemented in analog domains due to its continuous-time switching behavior, advancements in digital technology have spurred a growing interest in discrete-time implementations. DISMC extends the capabilities of conventional SMC by incorporating an additional integral action, resulting in improved dynamic performance, enhanced disturbance rejection, and better steady-state accuracy. This makes DISMC particularly well-suited for power electronic applications such as CDAs, where precision, efficiency, and stability are critical.

This work introduces a new approach to stability analysis and controller gain determination for DISMC in CDAs (**O4**). The proposed method is validated through MATLAB Simulink simulations and experimental trials, demonstrating its efficacy in both digital and analog domains.

One key objective of this work (**O3**) is to validate the discrete DISMC design in double-loop configurations for CDAs, with a specific focus on current mode control. While SMC has traditionally been implemented in the analog domain due to its continuous switching behavior, there is a growing shift among control engineers toward digital implementation. This trend is particularly relevant for systems with discontinuous behaviors like CDAs, where digital control offers increased

flexibility. Previous studies have primarily utilized voltage error as the state variable in SMC, resulting in a single-loop feedback control structure. In contrast, the approach presented in this work incorporates both voltage and current errors as state variables, forming a double-loop configuration. This configuration enhances performance in several key areas, including output voltage regulation, transient response, and robustness to load variations.

Although the inherent chattering effect of SMC can be exacerbated in the digital domain compared to its analog counterpart, the increasing availability of high-speed digital processing hardware is making discrete-time controllers more feasible. Consequently, discrete DISMC implementations in CDAs are gaining prominence as digital controllers become more capable of matching the performance of analog systems.

The chapter is organized as follows: Section 4.1 derives the mathematical model of the CDA output stage, the equivalent control signal based on DISMC is derived, followed by the determination of controller gains using the reaching and stability conditions. Subsequently, the equivalent discrete-time control signal is formulated. Section 4.2 presents the system-level design of the CDA, along with simulation and experimental results and their analysis. Finally, Section 4.3 provides the conclusion of this work.

4.1 Design of the DISMC

4.1.1 Modeling the Class-D Amplifier Output Stage

The full-bridge CDA output stage is depicted in Figure 4.1. The symbols for the left and right branches in Figure 4.1 are denoted as 1 and 2, respectively, following their respective symbols, where 1 represents the left branch and 2 represents the right branch. Throughout this dissertation, the analysis and design of the CDA are based on the half-bridge topology, which is then expanded to the full-bridge topology. Therefore, for simplicity, the numbers for the left and right branches are omitted.

In Figure 4.1, the half-bridge CDA output stage comprises a DC voltage source (V_i), bus capacitors (C_{bus}) that split the DC voltage source into equal and opposite polarities, GD, high-side and low-side power transistors, an inductor (L), a capacitor (C), and a load resistor (R).

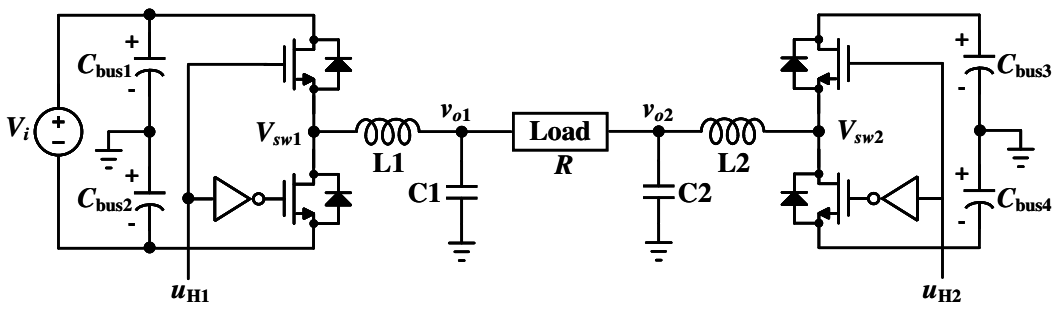


Figure 4.1: Schematic of a full-bridge inverter output stage.

By using the state-space averaging model, the ideal average model of the half-bridge CDA in Figure 4.1 can be described as:

$$\begin{cases} L\frac{di_L}{dt} = \frac{V_i}{2}(2u_{\mathrm{H}} - 1) - v_o \\ C\frac{dv_o}{dt} = i_L - \frac{v_o}{R/2} \end{cases} \tag{36}$$

where i_L is the inductor current, v_o is the half-bridge output voltage, $u_{\mathrm{H}} = 1$ when the high-side power transistor turns on, and $u_{\mathrm{H}} = 0$ when the low-side turns on. Since the analysis is based on a half-bridge, the effective load resistance is R/2. In DC-DC converters, the duty cycle, which typically ranges between 0 and 1, is commonly employed. However, in DC-AC operation, modulation depth (u) is frequently utilized instead of the duty cycle, with u being calculated as $2u_{\mathrm{H}}$ - 1. Equation (36) can be rewritten by utilizing u as follows:

$$\begin{cases} L\frac{di_L}{dt} = \frac{V_i}{2}u - v_o \\ C\frac{dv_o}{dt} = i_L - \frac{v_o}{R/2} \end{cases} \tag{37}$$

From Eq. (37), it can be seen that u ranges from -1 to 1. This corresponds to the operation of the CDA in Figure 4.1, where the load voltage ranges from $-V_i$ to V_i, as it is configured in bipolar mode.

4.1.2 Design of a Discrete Double Integral Sliding Mode Controller for Class-D Amplifier

The design process of any SMC typically involves four steps. Firstly, it entails deriving the switch-model of the power stage by analyzing all the switch states and defining the relevant state variables that require control. Secondly, a sliding surface, comprised of these state variables, is proposed. Thirdly, the control law is derived. Lastly, the existence and stability conditions are verified. This involves deriving controller gains to ensure the trajectory of the state variables remains close to the sliding surface, while the stability condition ensures that system dynamics approach the equilibrium point.

In this section, we first derive the control law, followed by the application of reaching and stability conditions to determine the controller gains. Subsequently, we convert the continuous-time control signal to a discrete-time control signal, which is then applied to the CDA using discrete-time DISMC.

4.1.2.1 Derivation of the Double Integral Sliding Mode Control Signal

The proposed DISMC utilizes both the output voltage error and the inductor current error as the controlled state variables. Incorporating the output voltage error as a state variable enables precise regulation of the output voltage, while the inclusion of the inductor current error ensures close maintenance of the inductor current to the desired reference value. Analogous to conventional current mode control, the proposed controller generates the reference inductor current profile by amplifying the output voltage error. Incorporating the double integral of both controlled state variables ensures the presence of at least one integral term in the control law, which we will derive later. This inclusion aims to minimize steady-state error across a wide operating region, encompassing various

operational switching frequencies. Therefore, the state variables are defined as:

$$\begin{cases} e_1 = i_{\text{ref}} - i_L \\ e_2 = V_{\text{ref}} - \beta v_o \\ e_3 = \int (e_1 + e_2) dt \\ e_4 = \int [\int (e_1 + e_2) dt] dt \end{cases} \tag{38}$$

where i_{ref} is the reference inductor current, V_{ref} is the reference voltage, β is the feedback scaling factor of the output voltage. The reference inductor current relationship with error voltage can be described as:

$$i_{\text{ref}} = K(V_{\text{ref}} - \beta v_o) \tag{39}$$

where K is the scaling coefficient.

First-order derivatives of state variables are:

$$\begin{cases} \dot{e}_1 = K\dot{V}_{\text{ref}} - \frac{\beta K}{C} i_c - \frac{V_i}{2L} u + \frac{v_o}{L} \\ \dot{e}_2 = \dot{V}_{\text{ref}} - \frac{\beta}{C} i_c \\ \dot{e}_3 = e_1 + e_2 \\ \dot{e}_4 = \int (e_1 + e_2) dt \end{cases} \tag{40}$$

where i_c is the capacitor current flowing through the capacitor C1 or C2.

Define the sliding surface as the weighted combination of the state variables:

$$S = a_1 e_1 + a_2 e_2 + a_3 e_3 + a_4 e_4 \tag{41}$$

where a_1 to a_4 are the associated coefficients of state variables.

The equivalent control signal of the DISMC can be found when the first-order derivative of the sliding surface is equal to zero:

$$\dot{S} = a_1 \dot{e}_1 + a_2 \dot{e}_2 + a_3 \dot{e}_3 + a_4 \dot{e}_4 = 0 \quad \Rightarrow u_{eq} \tag{42}$$

The derived equivalent control signal from Eq. (42) is:

$$\begin{aligned} u_{eq} =& \frac{2L}{V_i}(K + \frac{a_2}{a_1})\dot{V}_{\text{ref}} - \frac{2\beta L}{CV_i}(K + \frac{a_2}{a_1})i_c + \frac{2v_o}{V_i} + \frac{2a_3L}{a_1V_i}(V_{\text{ref}} - \beta v_o) \\ &+ \frac{2a_3L}{a_1V_i}[K(V_{\text{ref}} - \beta v_o) - i_L] + \frac{2a_4L}{a_1V_i}\int (V_{\text{ref}} - \beta v_o)dt \\ &+ \frac{2a_4L}{a_1V_i}\int [K(V_{\text{ref}} - \beta v_o) - i_L]dt \end{aligned} \tag{43}$$

As evident from Eq. (43), the equivalent control relies on data regarding capacitor current, output voltage, and inductor current. Another formulation of the equivalent control equation can be deduced from Eq. (42) as follows:

$$\begin{aligned} u_{eq} =& \frac{2a_2L}{a_1V_i}\dot{V}_{\text{ref}} + \frac{2L}{V_i}\dot{i}_{\text{ref}} + \frac{4a_2\beta L}{a_1CRV_i}v_o + \frac{2v_o}{V_i} - \frac{2a_2\beta L}{a_1CV_i}i_L + \frac{2a_3L}{a_1V_i}(V_{\text{ref}} - \beta v_o) \\ &+ \frac{2a_3L}{a_1V_i}(i_{\text{ref}} - i_L) + \frac{2a_4L}{a_1V_i}\int (V_{\text{ref}} - \beta v_o)dt + \frac{2a_4L}{a_1V_i}\int (i_{\text{ref}} - i_L)dt \end{aligned} \tag{44}$$

Equation (43) and Eq. (44) yield the same outcome. However, implementing the control signal from Eq. (43) is more straightforward, while Eq. (44) is convenient for analyzing the stability conditions, which will be utilized later.

The average dynamics of an SMC-based system are equivalent to the average dynamics of a PWM-controlled system, where

$$-1 \leq u_{eq} = d = \frac{v_o}{V_i/2} = \frac{v_c}{\hat{v}_{\text{car}}} \leq 1 \tag{45}$$

where d is the duty cycle of a PWM controlled system, v_c is the control signal of DISMC, and $\hat{v}_{\text{car}}$ is the peak amplitude of carrier signal. The v_c can be deduced from Eq. (45) as follows:

$$\hat{v}_{\text{car}} = \frac{V_i v_c}{2v_o} = \beta\frac{V_i}{2}, (\beta = \frac{v_c}{v_o}) \tag{46}$$

Hence, the control signal can be found as:

$$v_c = u_{eq} \times \hat{v}_{\text{car}} = u_{eq} \times \beta\frac{V_i}{2} \tag{47}$$

Substituting Eq. (43) into Eq. (47), the final expression of the control signal is:

$$\begin{aligned} v_c =& K_1\dot{V}_{\text{ref}} - K_2 i_c + \beta v_o + K_3(V_{\text{ref}} - \beta v_o) + K_3[K(V_{\text{ref}} - \beta v_o) - i_L] + K_4 \int (V_{\text{ref}} - \beta v_o)dt \\ &+ K_4 \int [K(V_{\text{ref}} - \beta v_o) - i_L]dt \end{aligned} \tag{48}$$

where

$$K_1 = \beta L(K + \frac{a_2}{a_1}) \qquad K_2 = \frac{\beta^2 L}{C}(K + \frac{a_2}{a_1})$$
$$K_3 = \beta L\frac{a_3}{a_1} \qquad K_4 = \beta L\frac{a_4}{a_1}$$

4.1.2.2 Reaching condition

The reaching condition states that the equivalent control in Eq. (43) must drive the state variables to the vicinity of the sliding surface. This can be expressed as the following condition:

$$\begin{cases} \dot{S}_{s\to 0^+} < 0, \text{ when } u_{eq} = 1 \\ \dot{S}_{s\to 0^-} > 0, \text{ when } u_{eq} = -1 \end{cases} \tag{49}$$

The reaching condition in Eq. (49) can be analyzed in two cases below to derive the inequality that the controller must comply with.

Case 1: $\dot{S} < 0$. By substituting $u_{eq} = 1$ into Eq. (42), the inequality below can be derived as follows:

$$K_1\dot{V}_{\text{ref}} - K_2 i_c + K_3(e_1 + e_2) + K_4 e_3 < \beta(\frac{V_i}{2} - v_o) \tag{50}$$

Case 2: $\dot{S} > 0$. By substituting $u_{eq} = -1$ into Eq. (42), the inequality below can be derived as follows:

$$-K_1\dot{V}_{\text{ref}} + K_2 i_c - K_3(e_1 + e_2) - K_4 e_3 < \beta(\frac{V_i}{2} + v_o) \tag{51}$$

When developing an SM controller with a static sliding surface, a practical approach involves designing the sliding coefficients to meet the existence conditions for steady-state operations. In this

context, the time-varying state variables v_o, i_L, and i_c (assuming the stability of the DC input voltage V_i) can be replaced with their anticipated maximum/minimum or steady-state parameters. These parameters can be derived from the design specifications. This methodology yields the following more comprehensive inequality equations, which assist in narrowing down the range of sliding surface coefficients.

$$\begin{cases} K_1\dot{V}_{\text{ref}(max)} - K_2 i_{c(min)} + K_3(e_{1(max)} + e_{2(max)}) + K_4 e_{3(max)} < \beta(\frac{V_i}{2} - v_{o(max)}) \\ -K_1\dot{V}_{\text{ref}(min)} + K_2 i_{c(max)} - K_3(e_{1(min)} + e_{2(min)}) - K_4 e_{3(min)} < \beta(\frac{V_i}{2} + v_{o(min)}) \end{cases} \tag{52}$$

4.1.2.3 Stability condition

Once the reaching condition is achieved, it is desirable for the state variables to remain in the vicinity of the sliding surface. Here, we first derive the ideal sliding dynamics of the system, and then establish an equilibrium point at the origin of the sliding surface. Subsequently, we ensure that both the current and voltage state variables at the equilibrium point meet the stability condition.

By replacing u in Eq. (37) with the equivalent control u_{eq} in Eq. (44), the ideal sliding dynamics of the system can be derived as:

$$\begin{cases} \frac{di_L}{dt} = & \frac{2a_2\beta}{a_1 CR} v_o - \frac{a_2\beta}{a_1 C} i_L + \frac{a_2}{a_1}\dot{V}_{\text{ref}} + \dot{i}_{\text{ref}} + \frac{a_3}{a_1}(V_{\text{ref}} - \beta v_o) + \frac{a_3}{a_1}(i_{\text{ref}} - i_L) \\ & + \frac{a_4}{a_1}\int (V_{\text{ref}} - \beta v_o)dt + \frac{a_4}{a_1}\int (i_{\text{ref}} - i_L)dt \\ \frac{dv_o}{dt} = & \frac{i_L}{C} - \frac{2v_o}{CR} \end{cases} \tag{53}$$

Here, we assume that DISMC drives the state variables to the sliding surface, and eventually to the equilibrium point and there is no outside disturbance. Then, there is no tracking error of the reference signal. At the equilibrium point:

$$V_O = V_m \sin(\omega_o t); \;\; I_L = I_m \sin(\omega_o t) \tag{54}$$

$$V_{\text{ref}} - \beta V_O = 0; \;\; I_{\text{ref}} = I_L = K(V_{\text{ref}} - \beta V_o) \tag{55}$$

where V_O and I_L are the steady-state output voltage and inductor current, V_m and I_m are the peak

amplitude of steady-state output voltage and inductor current, ω_o is the fundamental output frequency in radian per second. Substituting Eq. (54) and Eq. (55) into Eq. (53), equilibrium point steady-state equations can be derived as:

$$\begin{cases} \frac{2a_2\beta}{a_1CR}V_m\sin(\omega_o t) - \frac{a_2\beta}{a_1C}I_m\sin(\omega_o t) + \frac{a_2\beta}{a_1}V_m\omega_o\cos(\omega_o t) = 0 \\ V_m\omega_o\cos(\omega_o t) = \frac{I_m}{C}\sin(\omega_o t) - \frac{2V_m}{CR}\sin(\omega_o t) \end{cases} \tag{56}$$

Next, by linearizing the ideal dynamics around the equilibrium point, that is to separate the steady-state large signals and small ac signals, Eq. (53) becomes:

$$\begin{cases} \frac{d(I_L+\tilde{i}_L)}{dt} = & \frac{2a_2\beta}{a_1CR}(V_o+\tilde{v}_o) - \frac{a_2\beta}{a_1C}(I_L+\tilde{i}_L) + \frac{a_2}{a_1}\dot{V}_{\text{ref}} + \dot{I}_{\text{ref}} + \frac{a_3}{a_1}[V_{\text{ref}} - \beta(V_o+\tilde{v}_o)] \\ & + \frac{a_3}{a_1}[I_{\text{ref}} - (I_L+\tilde{i}_L)] + \frac{a_4}{a_1}\int[V_{\text{ref}} - \beta(V_o+\tilde{v}_o)]dt + \frac{a_4}{a_1}\int[I_{\text{ref}} - (I_L+\tilde{i}_L)]dt \\ \frac{d(V_o+\tilde{v}_o)}{dt} = & \frac{I_L+\tilde{i}_L}{C} - \frac{2(V_o+\tilde{v}_o)}{CR} \end{cases} \tag{57}$$

where variables with the tilde sign indicate small ac signals. To further process Eq. (57) to separate the large and small ac signals, applying equilibrium point equations Eq. (54) and Eq. (55) in Eq. (57), the following equations can be derived:

$$\begin{cases} I_m\omega_o\cos(\omega_o t) + \frac{d\tilde{i}}{dL} = & \frac{2a_2\beta}{a_1CR}V_m\sin(\omega_o t) + \frac{2a_2\beta}{a_1CR}\tilde{v}_o - \frac{a_2\beta}{a_1C}I_m\sin(\omega_o t) - \frac{a_2\beta}{a_1C}\tilde{i}_L \\ & + \frac{a_2\beta}{a_1}V_m\omega_o t\cos(\omega_o t) + I_m\omega_o\cos(\omega_o t) - \frac{a_3\beta}{a_1}\tilde{v}_o - \frac{a_3}{a_1}\tilde{i}_L \\ & - \frac{a_4\beta}{a_1}\int\tilde{v}_o dt - \frac{a_4}{a_1}\int\tilde{i}_L dt \\ V_m\omega_o\cos(\omega_o t) + \frac{d\tilde{v}_o}{dt} = & \frac{I_m}{C}\sin(\omega_o t) + \frac{\tilde{i}_l}{C} - \frac{2V_m}{CR}\sin(\omega_o t) - \frac{2\tilde{v}_o}{CR} \end{cases} \tag{58}$$

Assuming that at the equilibrium point $V_o \gg \tilde{v}_o$ and $I_L \gg \tilde{i}_L$, closely monitoring Eq. (56) and Eq. (58), the large signals cancel out in Eq. (58), leaving only small ac signals, which must satisfy

the stability condition.

$$\begin{cases} \frac{d\tilde{i}_L}{dt} = & (\frac{2a_2}{a_1CR} - \frac{a_3}{a_1})\beta\tilde{v}_o - (\frac{a_2\beta}{a_1C} + \frac{a_3}{a_1})\tilde{i}_L - \frac{a_4\beta}{a_1}\int \tilde{v}_o dt - \frac{a_4}{a_1}\int \tilde{i}_L dt \\ \frac{d\tilde{v}_o}{dt} = & \frac{\tilde{i}_L}{C} - \frac{2\tilde{v}_o}{CR} \end{cases} \tag{59}$$

The objective now is to determine if the small-signal model in Eq. (59) is stable. Let us assume $x = \tilde{i}_L$ and $y = \tilde{v}_o$, enabling us to rewrite Eq. (59) as:

$$\begin{cases} \dot{x} = \gamma_1 y - \gamma_2 x - \gamma_3 \int y dt - \gamma_4 \int x dt \\ \dot{y} = \gamma_5 x - \gamma_6 y \end{cases} \tag{60}$$

where

$$\gamma_1 = \frac{2a_2\beta}{a_1CR} - \frac{a_3\beta}{a_1} \qquad \gamma_2 = \frac{a_2\beta}{a_1C} + \frac{a_3}{a_1} \qquad \gamma_3 = \frac{a_4\beta}{a_1}$$
$$\gamma_4 = \frac{a_4}{a_1} \qquad \gamma_5 = \frac{1}{C} \qquad \gamma_6 = \frac{2}{CR}$$

Rearranging Eq. (60), a third-order differential equation in terms of small signal output voltage can be expressed as:

$$\frac{1}{\gamma_5}\dddot{y} + (\frac{\gamma_2 + \gamma_6}{\gamma_5})\ddot{y} + (\frac{\gamma_2\gamma_6 + \gamma_4}{\gamma_5} - \gamma_1)\dot{y} + (\frac{\gamma_4\gamma_6}{\gamma_5} + \gamma_3)\int y dt = 0 \tag{61}$$

Taking the Laplace transform ($Y = \mathcal{L}(y)$) of Eq. (61),

$$Y^3 + (\gamma_2 + \gamma_6)Y^2 + (\gamma_2\gamma_6 - \gamma_1\gamma_5 + \gamma_4)Y + (\gamma_4\gamma_6 + \gamma_3\gamma_5) = 0 \tag{62}$$

Applying Routh-Hurwitz criteria to Eq. (62), the system will be stable if the following conditions

are met:

$$\begin{cases} \gamma_5 > 0 \\ \gamma_2 + \gamma_6 > 0 \\ \gamma_2\gamma_6(\gamma_2 + \gamma_6) + \gamma_2\gamma_4 - \gamma_1\gamma_5(\gamma_2 + \gamma_6) - \gamma_3\gamma_5 > 0 \\ \gamma_4\gamma_6 + \gamma_3\gamma_5 > 0 \end{cases} \tag{63}$$

Inequalities in Eq. (63) further narrow down the region of the designed sliding surface coefficients from the existence condition. Directly solving the third-order differential equation in Eq. (62) becomes challenging which has three distinct root values. To simplify, let us factorize Eq. (62) into the product of first-order and second-order systems in a standard form, and make the system dominated by the second-order system.

$$\begin{aligned} Y^3 + b_2Y^2 + b_1Y + b_0 &= (Y + p)(Y^2 + 2\omega_n\zeta Y + \omega_n^2) \\ &= Y^3 + (2\omega_n\zeta + p)Y^2 + (\omega_n^2 + 2\omega_n\zeta p)Y + p\omega_n^2 = 0 \end{aligned} \tag{64}$$

$$\begin{cases} b_2 = & 2\omega_n\zeta + p = \gamma_2 + \gamma_6 \\ b_1 = & \omega_n^2 + 2\omega_n\zeta p = \gamma_2\gamma_6 - \gamma_1\gamma_5 + \gamma_4 \\ b_0 = & p\omega_n^2 = \gamma_4\gamma_6 + \gamma_3\gamma_5 \end{cases} \tag{65}$$

where p represents one of the poles (root value), ω_n denotes the natural frequency, and ζ stands for the damping ratio. The system also features two other poles at $-\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$. Let's assume the system exhibits critical damping, with $\zeta = 1$, which implies that the other two real poles are both at $-\omega_n$. If the system is predominantly characterized by a second-order system, this implies that the third pole is at least ten times greater than the other two poles. Hence, the following conditions

Table 4.1: SYSTEM PARAMETERS

Parameters	Values
DC input voltage (V_{i})	24 V
Inductor (L_1, L_2)	112 µH
Capacitor (C_1, C_2)	0.56 µF
Load resistor (R)	20 Ω
Reference voltage (V_{ref})	2.4 V (peak)
Carrier voltage (V_{car})	2.4 V (peak)
Carrier frequency ($f_s w$)	520 kHz
β	0.2

Table 4.2: CALCULATED COEFFICIENTS

Parameter	Values	Parameters	Values
γ_1	-6.61×10^3	a_4/a_1	2.693×10^8
γ_2	-2.17×10^4	β	0.2
γ_3	5.38×10^7	K	20
γ_4	2.69×10^8	K_1	2.24×10^{-4}
γ_5	1.78×10^6	K_2	5.89
γ_6	1.78×10^5	K_3	0.167
a_2/a_1	-0.103	K_4	3.03×10^3
a_3/a_1	1.482×10^4		

must be met:

$$\begin{cases} \zeta = & 1, \text{ (critical damping)} \\ p = & 10\omega_n, \text{ (dominated by second-order)} \end{cases} \tag{66}$$

With the natural frequency ω_n being the same as the cut-off frequency of the LC filter ($\omega_n = \omega_{LC} = 2\pi f_{LC}$), and by combining the system parameters in Table 4.1, the coefficients are solved as shown in Table 4.2.

4.1.2.4 Design of the Discrete-time DISMC

To enable the implementation of continuous SMC in a digital processor, SMC is discretized as DSMC with a sampling time T_s to facilitate practical application. Utilizing the derivative definition and considering that the system sampling period T_s is much shorter than the fundamental period T,

we obtain the following formula:

$$\dot{e}(k) \approx \frac{e(k) - e(k-1)}{T_s} \tag{67}$$

The continuous-time state variables in Eq. (38) become the discrete-time state variables as follows:

$$\begin{cases} e_1(k) = i_{\text{ref}}(k) - i_L(k) \\ e_2(k) = V_{\text{ref}}(k) - \beta v_o(k) \\ e_3(k) = e_3(k-1) + [e_1(k) + e_2(k)]T_s \\ e_4(k) = e_4(k-1) + e_3(k)T_s \end{cases} \tag{68}$$

Therefore, the control signal in Eq. (48) is discretized as follows:

$$\begin{aligned} v_c(k) =& K_1\dot{V}_{\text{ref}}(k) - K_2 i_c(k) + \beta v_o(k) + K_3(v_{\text{ref}}(k) - \beta v_o(k)) \\ &+ K_3[K(v_{\text{ref}}(k) - \beta v_o(k)) - i_L(k)] \\ &+ K_4[e_2(k-1) + (v_{\text{ref}}(k) - \beta v_o(k))T_s] \\ &+ K_4[e_1(k-1) + [K(v_{\text{ref}}(k) - \beta v_o(k)) - i_L(k)]T_s] \end{aligned} \tag{69}$$

As the fundamental output period T is much larger than the sampling period T_s, the controller gains derived earlier can be utilized for the discrete-time controller gains when implementing the control signal v_c in a discrete-time fashion.

The discrete-time DISMC block diagram for the full-bridge CDA is shown in Figure 4.2. The output stage variables v_o, i_c, and i_L are measured and discretized before being used in discrete-time DISMC. The control signal $v_c(k)$ in Figure 4.2 is implemented as Eq. (69). The term $K_1\dot{V}_{\text{ref}}(k)$ in Eq. (69) is ignored since K_1 is very small. The control signal v_c is compared with the carrier signal v_{car} to generate the PWM signals that drive the power transistors in the full-bridge. The reference signals $V_{\text{ref1}}(k)$ and $V_{\text{ref2}}(k)$ are internally generated from the FPGA and are phase-shifted

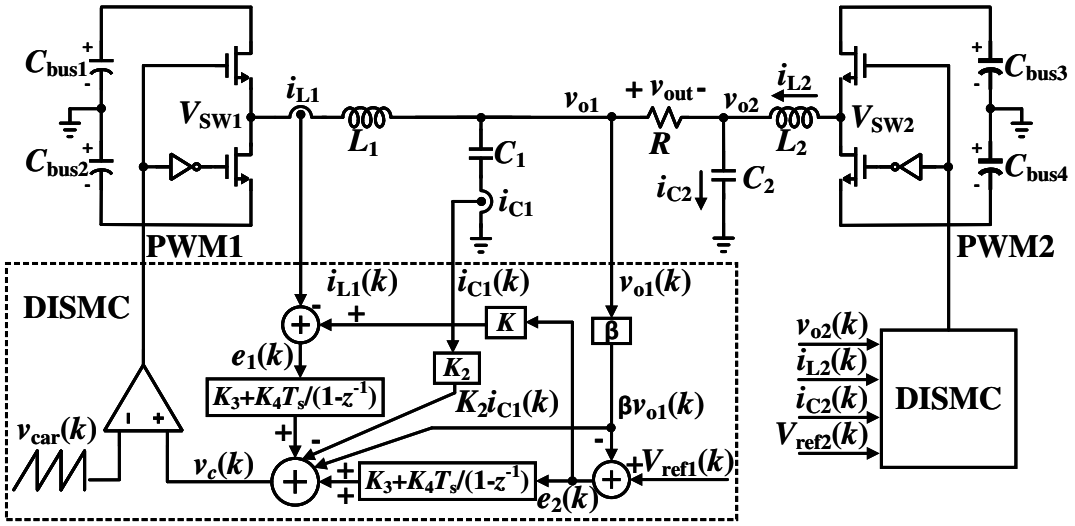


Figure 4.2: Discrete-time DISMC block diagram for a full-bridge CDA.

by 180°.

4.1.3 System Level Design of the DISMC Class-D Amplifier

In this section, the system implementation of the CDA, the simulation conditions and results, and the experimental results are presented and analyzed.

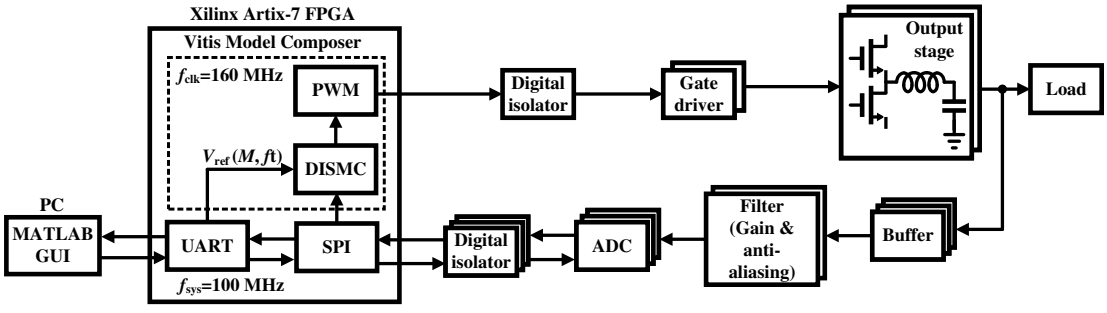


Figure 4.3: The system architecture of the designed class-D amplifier

To validate the functionality and demonstrate the performance of the proposed discrete-time DISMC algorithm, a closed-loop system for the CDA is designed as shown in Figure 4.3. In the system, the buffer stage consists of sensing amplifiers where CDA output stage variables i_L, i_c, and v_o are measured. Small shunt resistors are used to measure the current variables. The filter stage

in hardware is implemented as a Multiple Feedback (MFB) configuration and serves the purpose of providing gain (amplifying current signals and attenuating the voltage signals) so that it meets the full input range of ADC. It also serves the purpose of an anti-aliasing filter to remove the noise above the Nyquist frequency before the measured signals go into the ADC. The measured signals are discretized by 12-bit ADCs with a sampling time of T_s, then through digital isolators which serve the purpose of isolating the whole CDA from the FPGA. The FPGA code is written in VHSIC Hardware Description Language (VHDL) and the design consists of:

1. A Serial Peripheral Interface (SPI) for communicating between the FPGA and ADCs,

2. A UART for writing the configuration bits to ADCs, and reading the ADC outputs for debugging purposes, and writing/setting the modulation index (M) and fundamental output frequency (f_t) of the reference signal inside the DISMC block,

3. The proposed DISMC plus PWM generation, which is designed in Vitis Model Composer (formerly known as System Generator) embedded into the MATLAB/Simulink environment. The MATLAB GUI on the PC is used for writing/reading the commands from the FPGA. The generated PWM signals from the FPGA go through digital isolators to drive the gate driver which eventually drives the power transistors in the CDA output stage.

4.1.3.1 Design of DISMC class-D amplifier in Vitis Model Composer

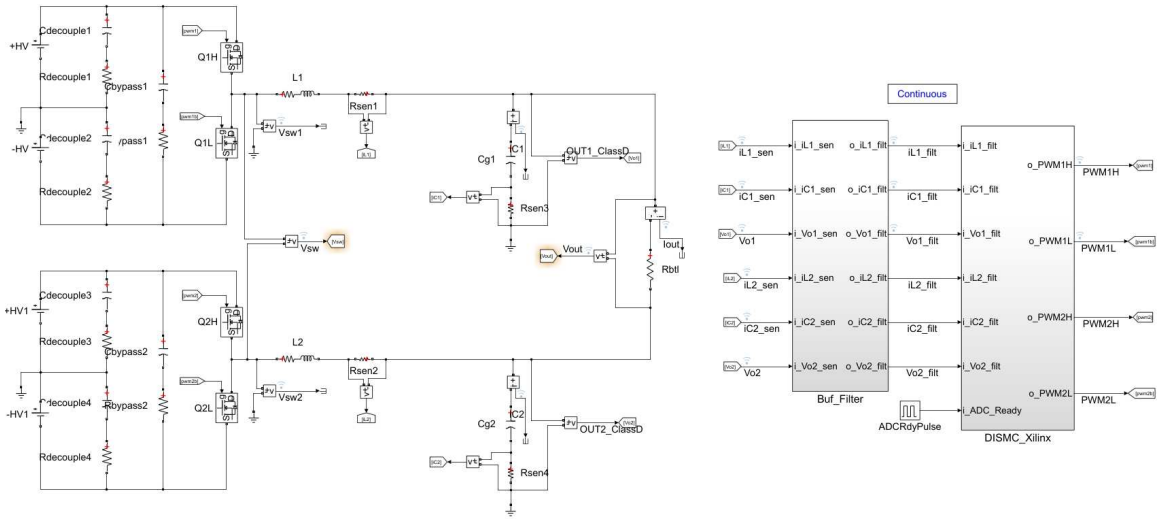


Figure 4.4: The full-bridge class-D amplifier design in Vitis Model Composer (System Generator)

The entire CDA with the DISMC was designed and simulated using Xilinx Vitis Model Composer (formerly known as System Generator), which is compatible with MATLAB Simulink. The designed full-bridge CDA is shown in Figure 4.4. The full-bridge CDA, depicted in Figure 4.4, can be divided into three major parts: the power output stage, the buffer and filter stage, and the DISMC stage.

- The power output stage: This stage includes the full bridge with power transistors, LC filters, and a load resistor. The current from the LC filter's inductor and capacitor is sensed using small shunt resistors, and single-ended output voltages from each branch are directly sensed.
- The buffer and filter stage: This stage mainly includes gain circuits for sensing voltage and current, as well as anti-aliasing filters. The purpose of this stage is to perform current-to-voltage conversion, scale the sensed voltages to within the range of the ADC full scale, and reduce noise before quantization.
- The DISMC block: This stage is shown in Figure 4.5. It processes the sensed voltages and currents from the previous buffer and filter stage and generates two duty cycle commands for both branches of the full bridge. These duty cycle commands are then compared with a ramp signal to generate two main PWM signals, along with their complementary signals, to drive the power transistors.

An ADC ready logic signal serves as an input to the DISMC. Whenever new ADC sampled data arrives at the DISMC block inside the FPGA from the ADC, the ADC ready logic signal goes "high" for one clock cycle, updating the corresponding registers. The implementation of the DISMC, as shown in Figure 4.2, in Vitis Model Composer is illustrated in Figure 4.6. The error signal, resulting from the subtraction of the reference signal and the scaled output voltage, is fed into a proportional-integral block to generate the $PIeV$ signal. The current reference is generated by scaling the error signal and is subtracted from the inductor current, which is then fed into another proportional-integral block to generate the $PIei$ signal. Finally, the two proportional-integral outputs, along with the scaled output voltage and the sensed capacitor current, are summed to generate the duty cycle command, the dn signal.

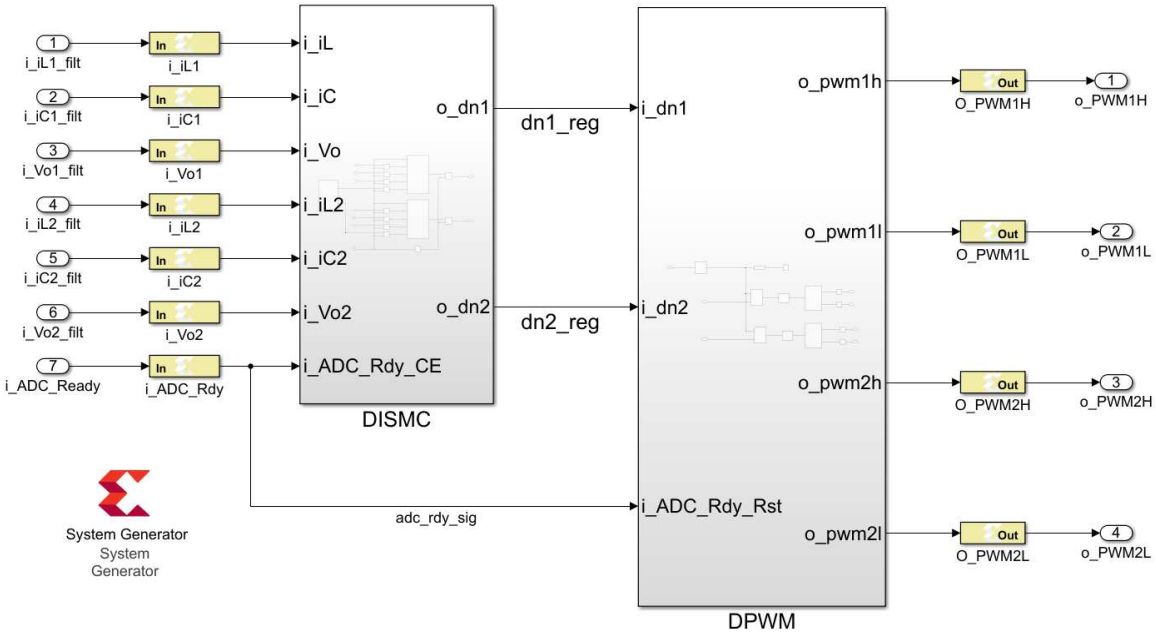


Figure 4.5: The top level DISMC showing I/Os

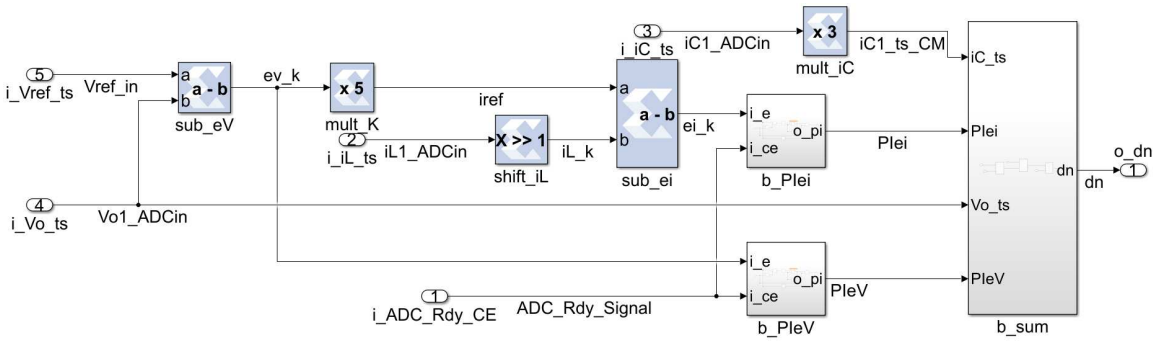


Figure 4.6: The implementation of DISMC in Xilinx blocksets in Vitis Model Composer

The proportional-integral (PI) block is implemented as shown in Figure 4.7, following Eq. (69). The corresponding registers are updated (enabled) each time new ADC samples are received. To prevent windup, which is a common issue in PI/PID controllers, the integral path output is constrained by user-defined binary point selection. When the predefined limit is reached, the integral path output becomes saturated.

The digital pulse width modulation (DPWM) block is illustrated in Figure 4.8. The ramp signal is generated by a counter, which resets upon the arrival of a new ADC sample, ensuring that the switching frequency of the converter matches the ADC sampling rate. The two duty cycle commands from the DISMC are then compared with the ramp signal to generate the PWM signals,

while their complementary signals are produced using dead-time blocks.

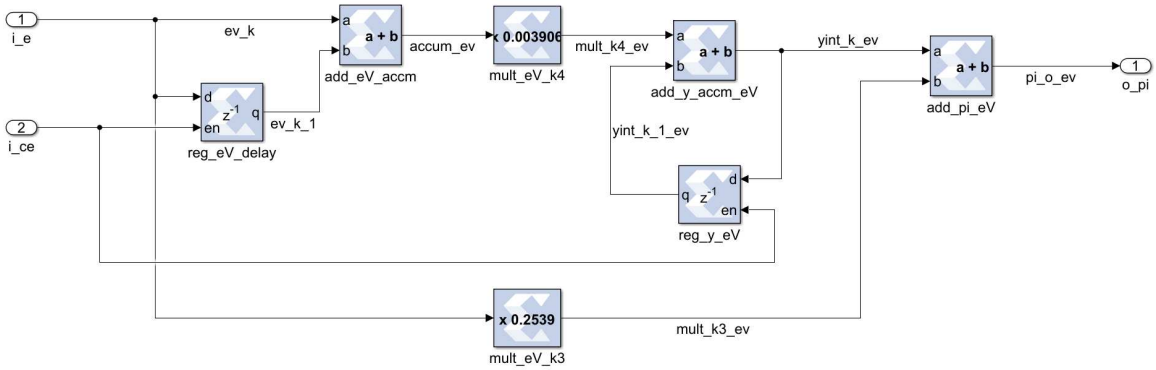


Figure 4.7: The implementation of proportional-integral in DISMC

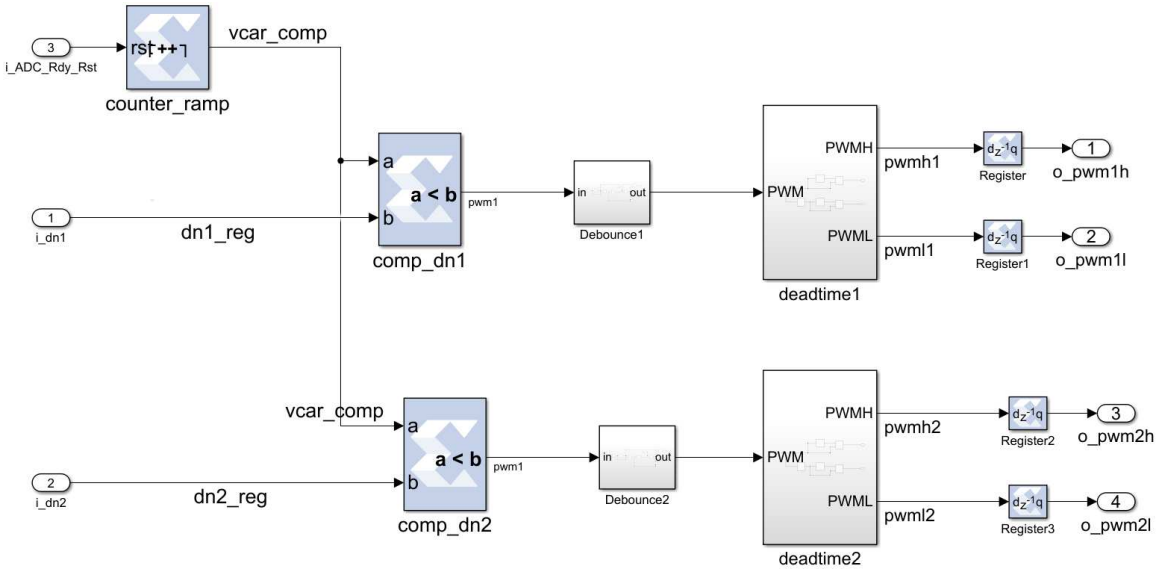


Figure 4.8: The digital pulse width modulation block

4.1.3.2 DISMC IP integration and FPGA architecture in Vivado Design Suite

The designed DISMC, developed using Xilinx Vitis Model Composer, is compiled as an Intellectual Property (IP) core and imported into the Vivado Design Suite as an IP block, as shown in Figure 4.9. The I/O pins of this block include an ADC ready logic signal, which goes high for one clock cycle whenever a new ADC sample is available, along with six channels of 12-bit ADC data corresponding to the output voltage, inductor current, and capacitor current. Additionally, the block has a clock input and four PWM output signals.

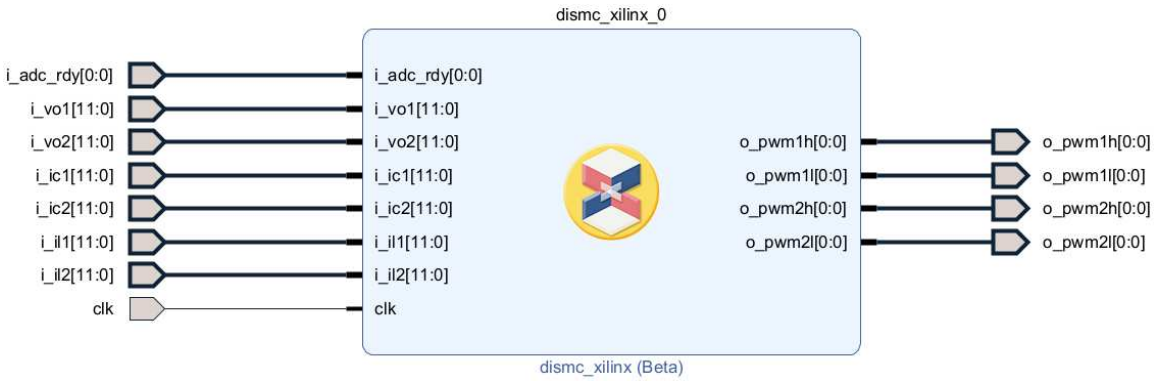


Figure 4.9: The DISMC IP in Vivado imported from Xilinx Vitis Model Composer

The DISMC IP block is then integrated into the top-level FPGA design, with the architecture depicted in Figure 4.10. The FPGA design includes the following components: a SPI master, an SPI state machine, an asynchronous FIFO, and the PWM control block (DISMC IP). Note that the UART interface, used to program the ADC through SPI, is not shown in the block diagram. The functionality of each block is as follows:

- **SPI Master**: The design includes three SPI masters, each controlling one of the three ADC slaves. The interface features the master out, slave in (MOSI) line, used to configure the ADCs. The ADCs, ADS7253 from Texas Instruments (TI), are configured in single serial data out (SDO) mode, where two analog input channels are converted to digital signals and transmitted via a single master in, slave out (MISO) line. Consequently, the three ADCs provide a total of six channels of digital output. The SPI clock operates at $25\,\mathrm{MHz}$, derived from the main $100\,\mathrm{MHz}$ FPGA clock using a clock divider. The chip select (CS) pin, which is active low, is shared among the three ADCs for slave selection.

- **SPI State Machine**: This block deserializes the ADC output data, creating a 72-bit bus from the six ADC channels. Additionally, it generates an ADC ready signal when new ADC frame data is available.

- **Asynchronous FIFO**: This block is responsible for clock domain crossing (CDC), where the ADC data is transferred from the $100\,\mathrm{MHz}$ domain to the $160\,\mathrm{MHz}$ domain. The PWM control block operates at a higher clock frequency of $160\,\mathrm{MHz}$ to achieve higher resolution for the PWM signals and to minimize errors when generating the ramp signal.

- **PWM Control**: This block, implemented as the DISMC IP generated from Xilinx Vitis Model Composer, reads the ADC data, processes it, and generates four PWM signals for the full-bridge class-D amplifier.

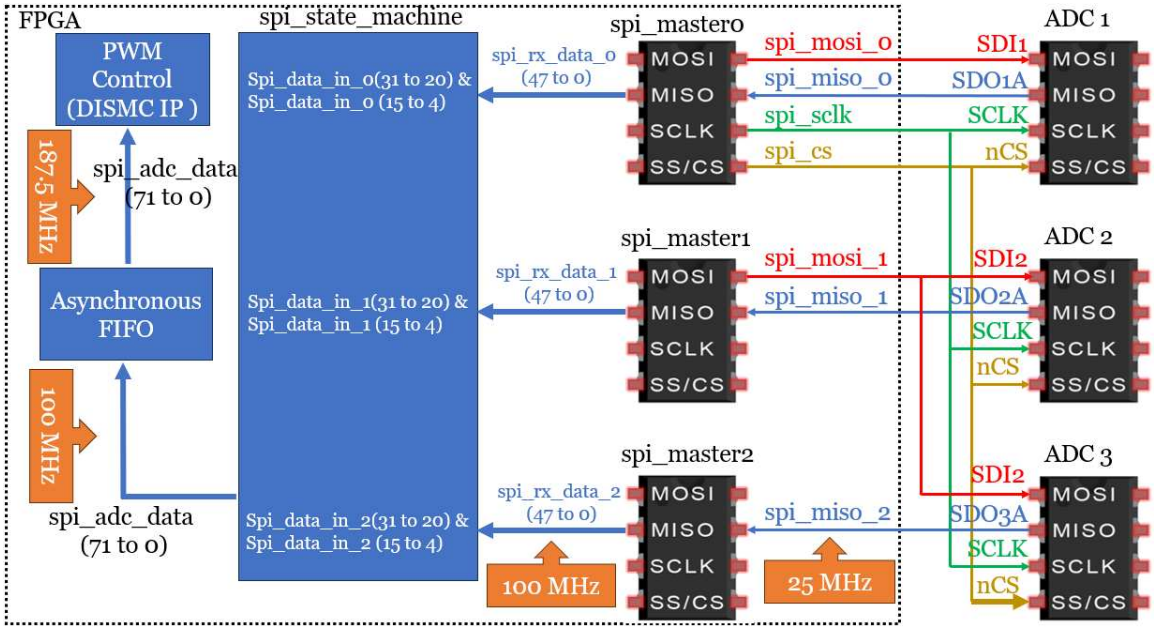


Figure 4.10: The FPGA block diagrams and its interaction to ADCs

4.2 Simulation and Experimental Results of Designed DISMC

The CDA system is simulated in the MATLAB/Simulink environment. The designed system is divided into analog and digital parts. The analog parts utilize continuous-time Simulink blocks, including the output stage, buffer, and filter. The filter incorporates gain blocks and a second-order Butterworth filter with a cutoff frequency of $250\,\mathrm{kHz}$. The ADC interface, DISMC, and PWM generation blocks are implemented using fixed-point digital processing blocks in Xilinx Vitis Model Composer. The ADC is configured as 12-bit with a sampling time of $1.92\,\mu\mathrm{s}$. The DISMC block operates at $160\,\mathrm{MHz}$ and generates synchronized PWM signals with the same period as the ADC sampling time, resulting in a PWM switching frequency of around $520\,\mathrm{kHz}$. The remaining conditions utilize the system specifications provided in Table 4.1.

The steady-state and dynamic performance of the DISMC is compared with that of the ISMC

and PI controllers. First, the ISMC and PI controller gains are derived based on the same full-bridge amplifier architecture. The controller gains are calculated using an identical controller bandwidth, ω_n. The controllers are implemented in Vitis Model Composer, similar to the DISMC. For the ISMC, the control signal is derived using the same procedures as the DISMC, with the coefficients distinguished by adding a prime ($'$) symbol. The derived control signal for the ISMC is:

$$\begin{aligned} v_c'(k) =& K_1'\dot{V}_{\text{ref}}(k) - K_2' i_c(k) + \beta v_o(k) + K_3'(v_{\text{ref}}(k) - \beta v_o(k)) \\ &+ K_3'[K'(v_{\text{ref}}(k) - \beta v_o(k)) - i_L(k)] \end{aligned} \tag{70}$$

The calculated coefficients for the ISMC are as follows:

$$K' = 20 \qquad K_1' = 4.34 \times 10^{-4}$$
$$K_2' = 6 \qquad K_3' = 0.044$$

The current-controlled PI controller is designed as shown in Figure 4.11. The error voltage between the output voltage and the reference voltage is fed into the voltage-controlled PI controller ($PI_{\text{v}}(z)$) to produce the reference current. The error current between the reference current and the inductor current is fed into the current-controlled PI controller ($PI_{\text{i}}(z)$) to generate the duty cycle command, which will subsequently be used to generate the PWM signal. The two PI controllers are expressed as:

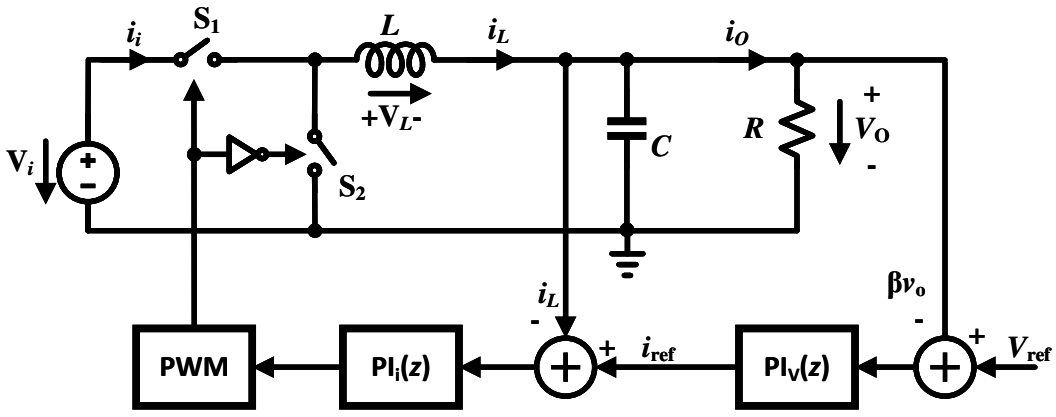


Figure 4.11: Steady-state operation of DISMC, ISMC, and PI controllers compared to a reference signal.

$$PI_{\mathrm{v}}(z) = K_{pv} + \frac{K_{iv}T_s}{1 - z^{-1}} \tag{71}$$

$$PI_{\mathrm{i}}(z) = K_{pi} + \frac{K_{ii}T_s}{1 - z^{-1}} \tag{72}$$

where K_{pv} and K_{iv} are the proportional and integral gains for outer voltage control, and K_{pi} and K_{ii} are the proportional and integral gains for inner current control. The calculated PI controller gains are:

$$K_{pv} = 0.196 \qquad K_{iv} = 9.26 \times 10^3$$

$$K_{pi} = 12.993 \qquad K_{ii} = 3.47 \times 10^4$$

The steady-state operation of the full-bridge CDA at a peak output current of 1 A (2 A peak-to-peak) using the DISMC, ISMC, and PI controllers is depicted in Figure 4.12. The scaled output voltage of these controllers and the reference voltage are provided. It can be observed from the figure that all controllers successfully track the reference signal. However, the steady-state error of the DISMC is the smallest, followed by the PI controller, and then the ISMC.

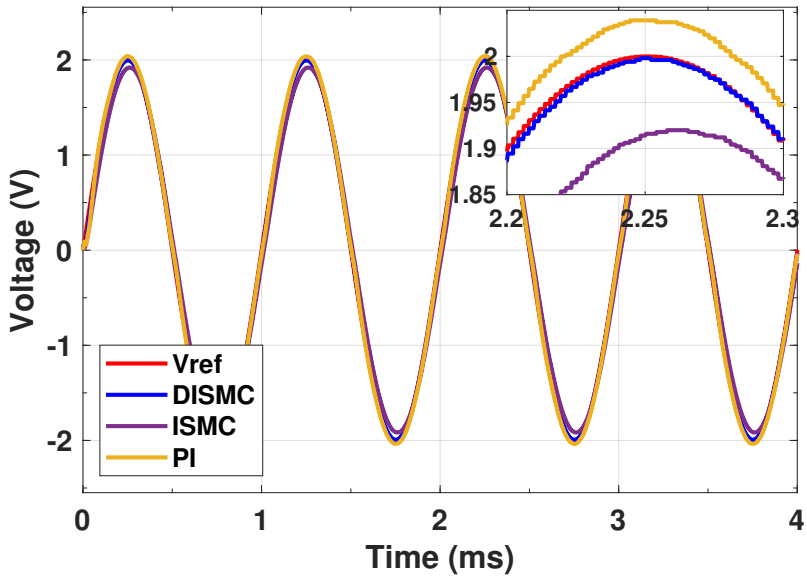
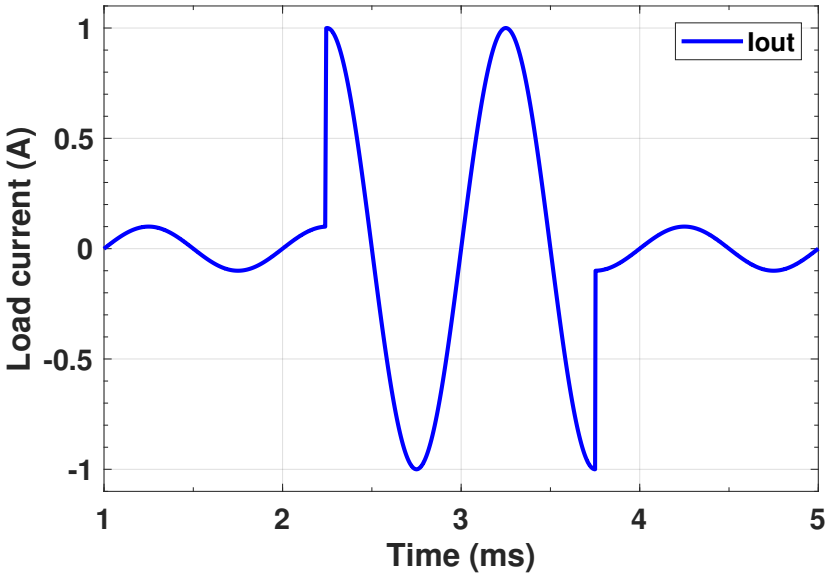


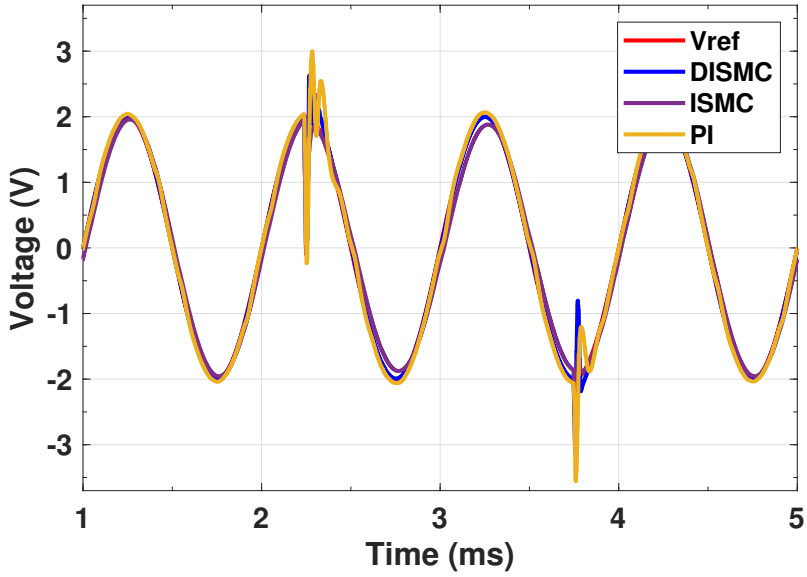
Figure 4.12: Steady-state operation of DISMC, ISMC, and PI controllers compared to a reference signal

The dynamic performance of these controllers is simulated under load and line transients. In

the load transient scenario, the peak load current starts at 0.1 A, jumps to 1 A, and then returns to 0.1 A. The resulting output voltages of these controllers are shown in Figure 4.13, with a zoomed view of the output voltage response provided in Figure 4.14. Overall, the ISMC controller exhibits less peaking and faster recovery to the nominal voltage compared to the DISMC and PI controllers. Although the DISMC controller shows less peaking than the PI controller, it exhibits more pronounced ringing when transitioning from heavy to light load. The PI controller, on the other hand, takes longer to regulate back to the steady-state voltage level.

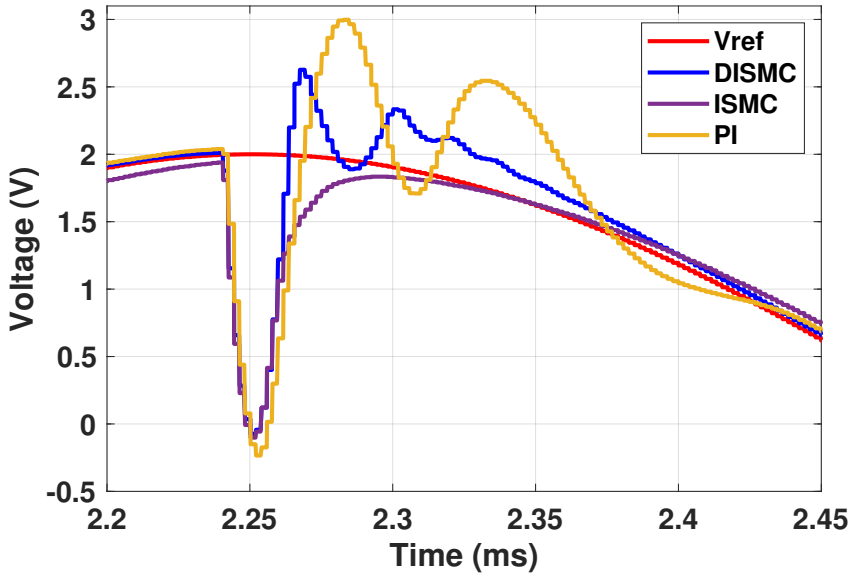


(a)

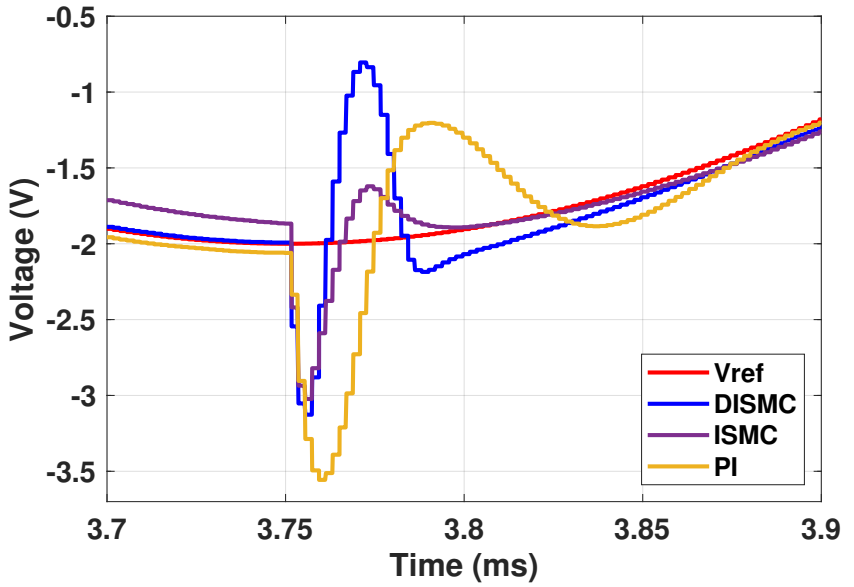


(b)

Figure 4.13: (a) Load current transient from 0.1 A to 1 A and back to 0.1 A. (b) Load transient response of DISMC, ISMC, and PI controllers.



(a)

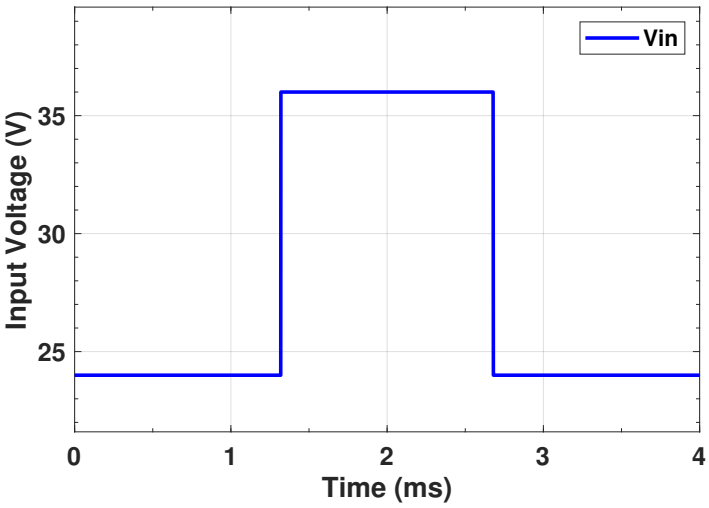


(b)

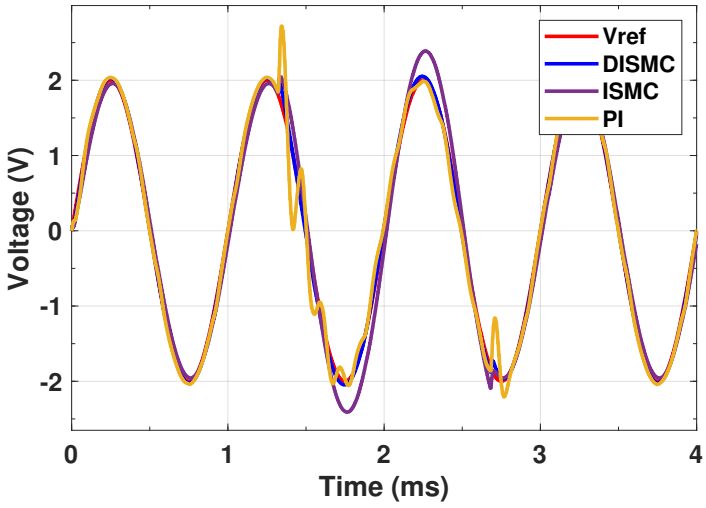
Figure 4.14: (a) Enlarged load transient response from light load to heavy load. (b) Enlarged load transient response from heavy load to light load.

In the line transient response simulation, the input voltage jumps from 24 V to 36 V, then back to 24 V. The output voltage response to the line transient is depicted in Figure 4.15. The enlarged region of the line transient response is shown in Figure 4.16. It can be seen from the figure that the PI controller exhibits significant peaking compared to DISMC and ISMC, and nearly becomes

unstable. The ISMC, on the other hand, has smaller peaking but the output voltage becomes larger in the higher input voltage region due to poor line regulation, returning to the normal output voltage when the input voltage returns to the normal value of 24 V. Among all the controllers, DISMC demonstrates the best line transient response in terms of minimal peaking and the ability to quickly regulate back to normal operation.

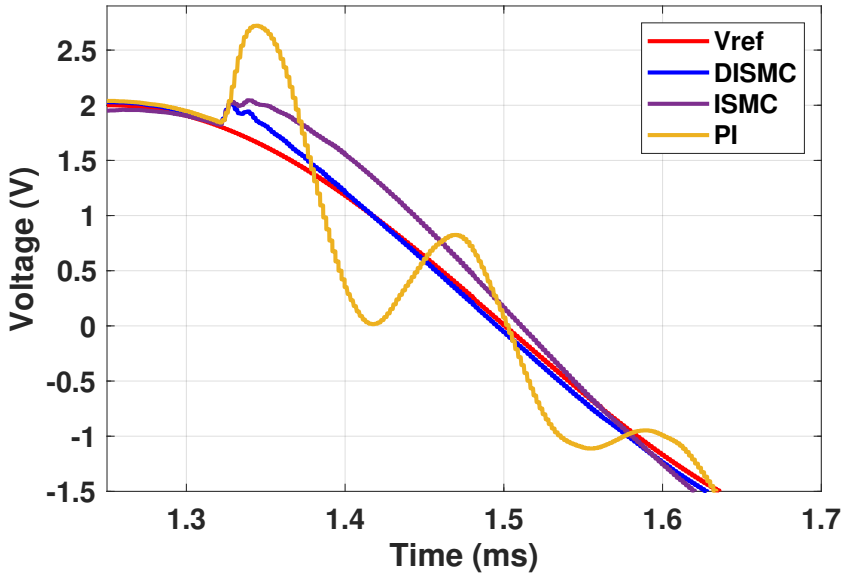


(a)

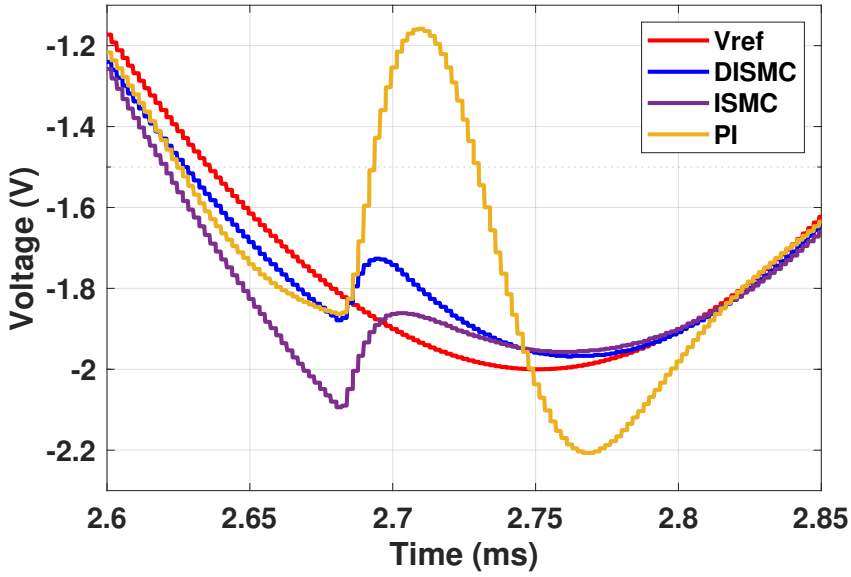


(b)

Figure 4.15: (a) Input voltage transient from 24 V to 36 V and back to 24 V. (b) Line transient response of DISMC, ISMC and PI controllers at light load of 0.1 A.



(a)



(b)

Figure 4.16: (a) Enlarged line transient response from 24 V to 36 V. (b) Enlarged line transient response from 36 V to 24 V.

The CDA was implemented on a PCB to validate the performance of the proposed DISMC by evaluating both its steady-state and dynamic behavior. The designed PCB is illustrated in Figure 4.17, with annotations indicating each stage, while the corresponding component part numbers are provided in Table 4.3. The test setup for the DISMC-controlled CDA is depicted in Figure 4.18.

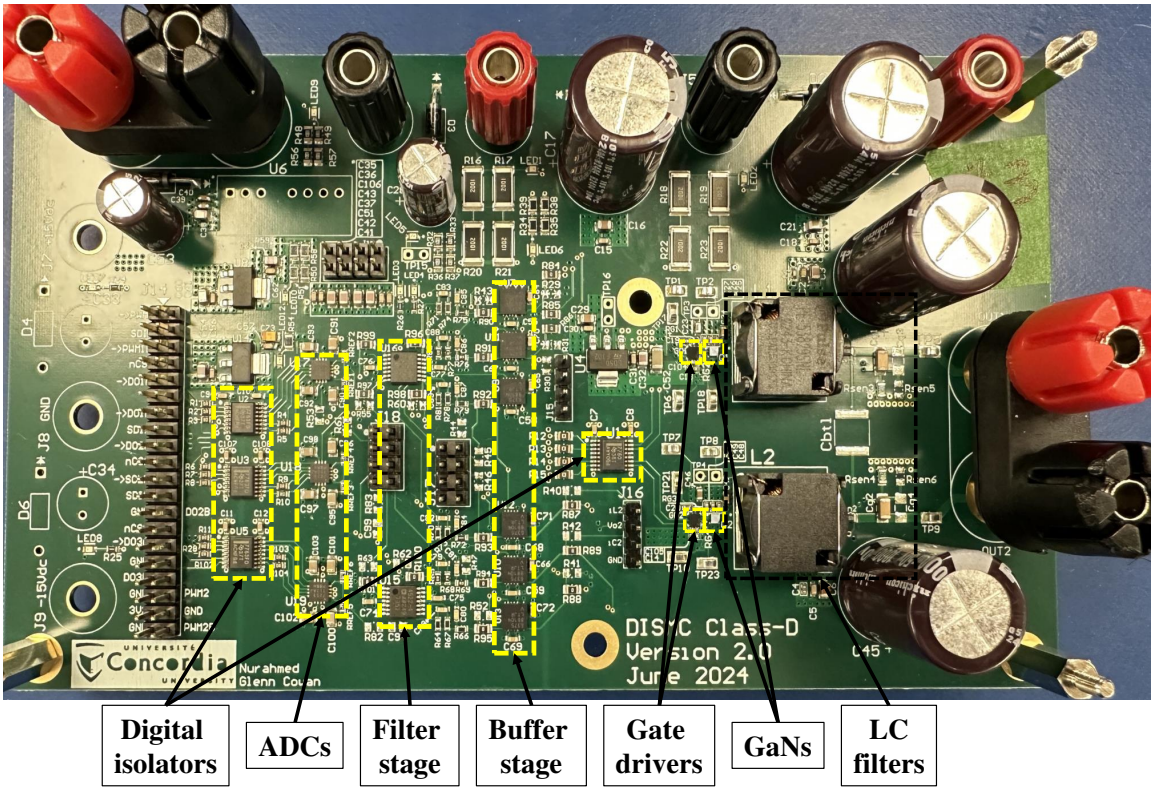


Figure 4.17: The prototype of DISMC class-D amplifier

In this setup, the power supplies include a 24 V bus voltage for the power stage, ± 15 V for the buffer and filter stages, and 7 V as the input voltage for the linear low-dropout (LDO) regulators, which generate 5 V and 3.3 V for the ADC's analog and digital circuits, respectively.

Steady-state operation: The DISMC CDA was tested under steady-state conditions for different modulation indices and frequencies. Two differential probes were used to measure and display the differential switching node voltage, V_{SW}, and the output voltage, V_{OUT}, on the oscilloscope.

Table 4.3: COMPONENT PART NUMBERS

Component	Part number
Gate driver	LMG1205
GaN FET	EPC2106
Buffer amplifier	LT6375
Filter amplifier	ADA4522
ADC	ADS7253
Digital isolator	ISO7760 & ISO7763
FPGA	Xilinx Artix-7

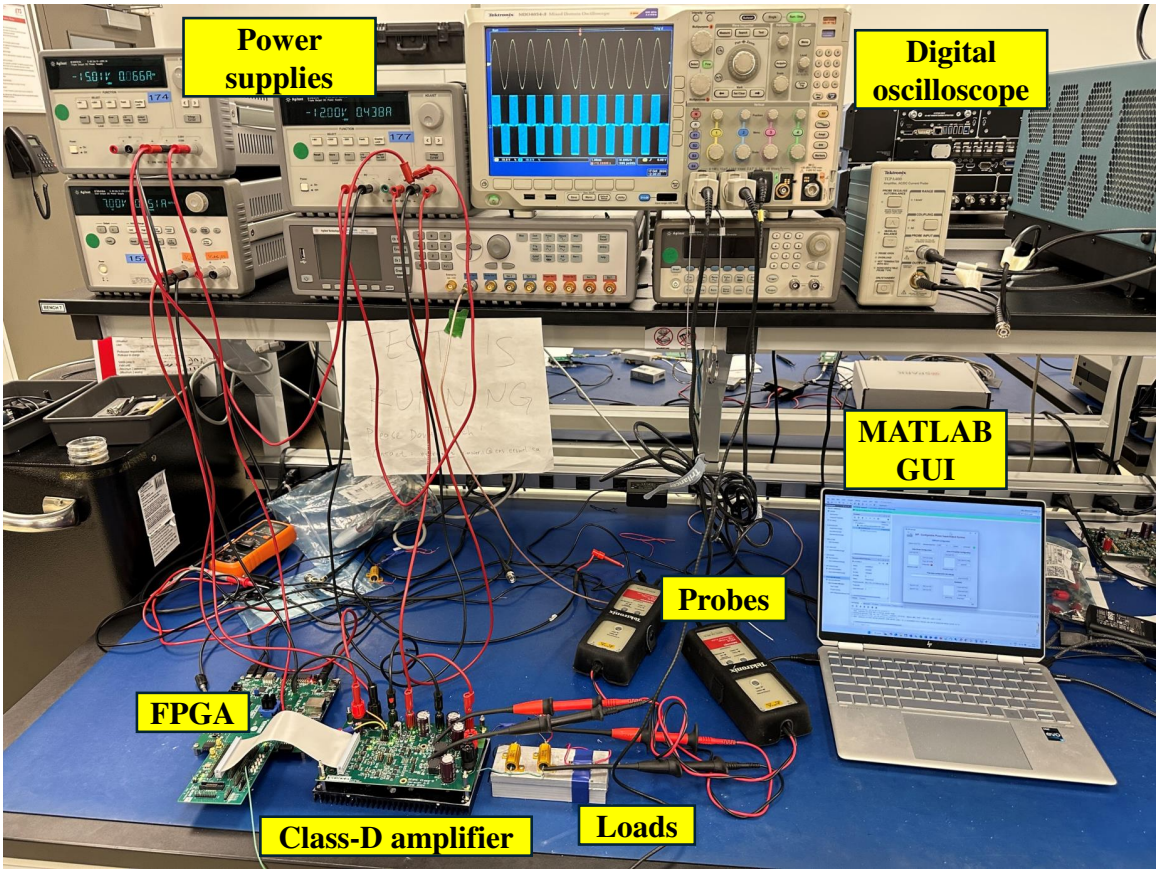


Figure 4.18: Test setup for the DISMC class-D amplifier

Figures 4.19 and 4.20 show the V_{OUT} and V_{SW} waveforms at 1 kHz and 10 kHz, respectively. Figure 4.21 presents a zoomed-in view of the switching node voltages (V_{SW1} and V_{SW2}) along with the differential output voltage. The waveforms of V_{SW1} and V_{SW2} confirm the BD modulation scheme of the CDA. As shown in Figure 4.21a, when V_{OUT} is positive, V_{SW1} exhibits a longer turn-on time compared to V_{SW2}, and vice-versa when V_{OUT} is negative. These observations indicate that the CDA operates as expected in steady-state conditions.

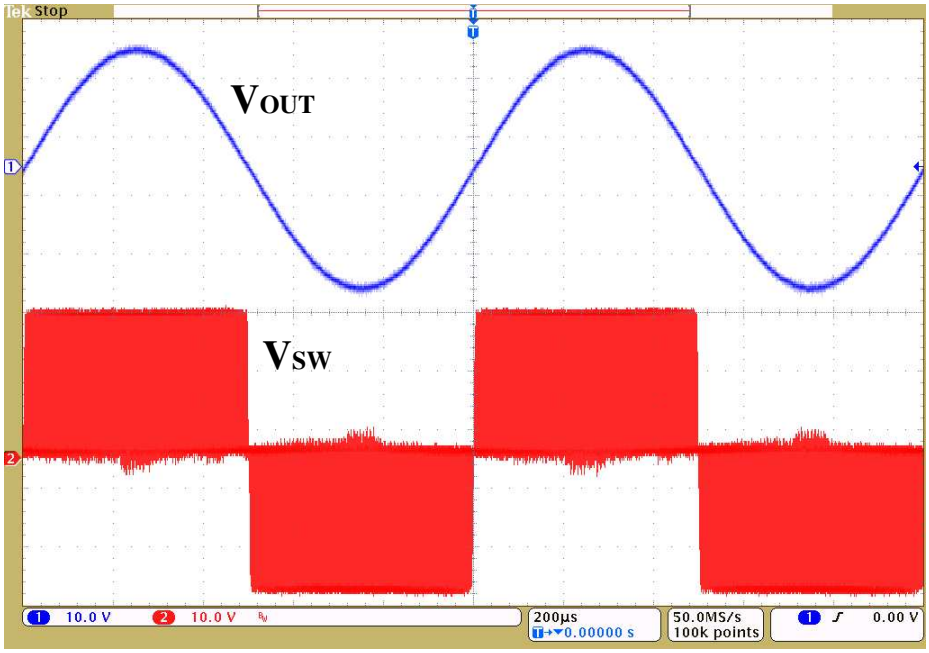


Figure 4.19: Experimental results of steady state operation of 1 kHz output

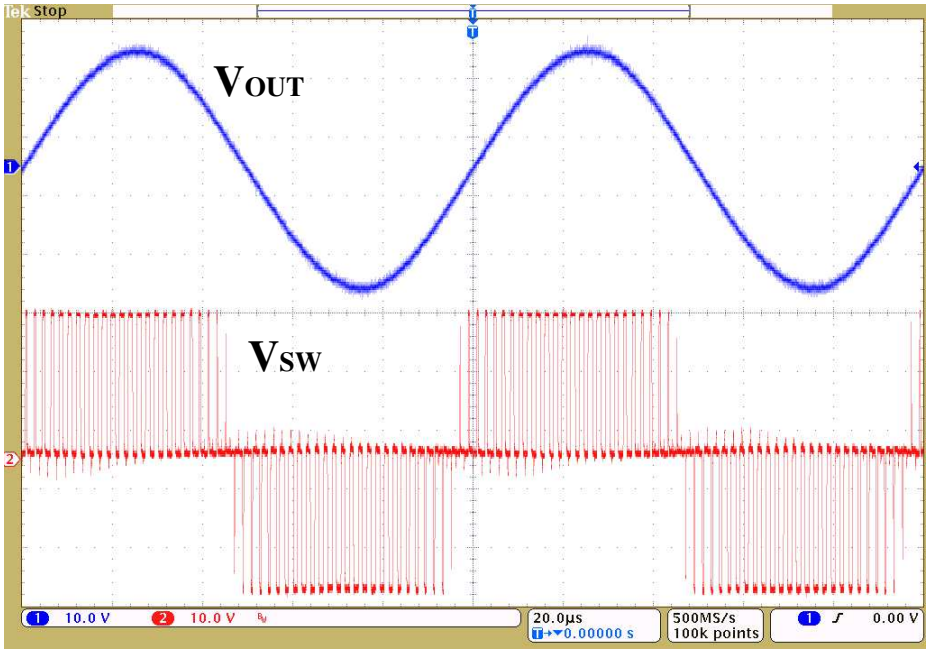
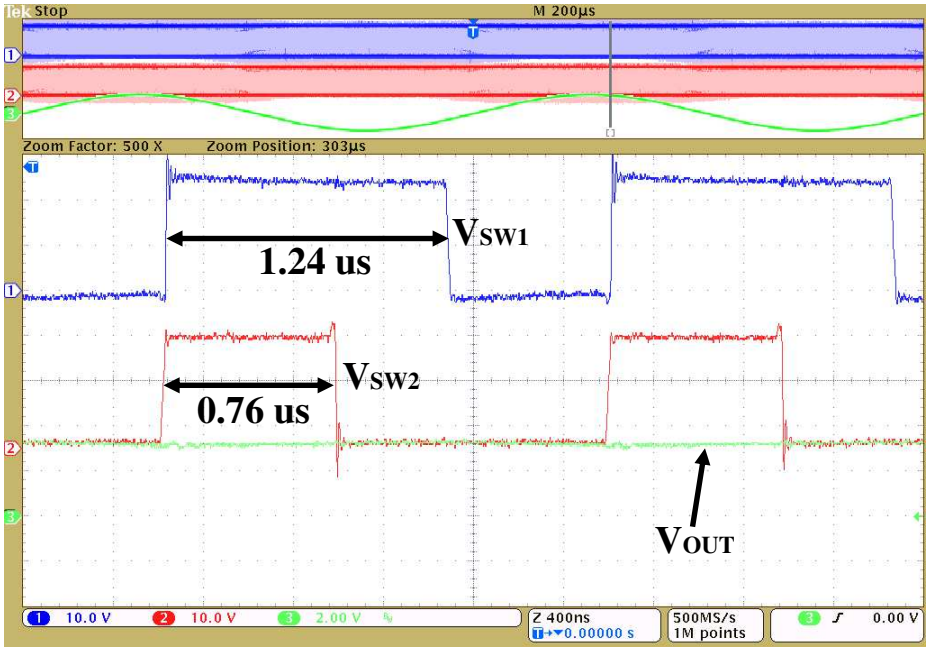
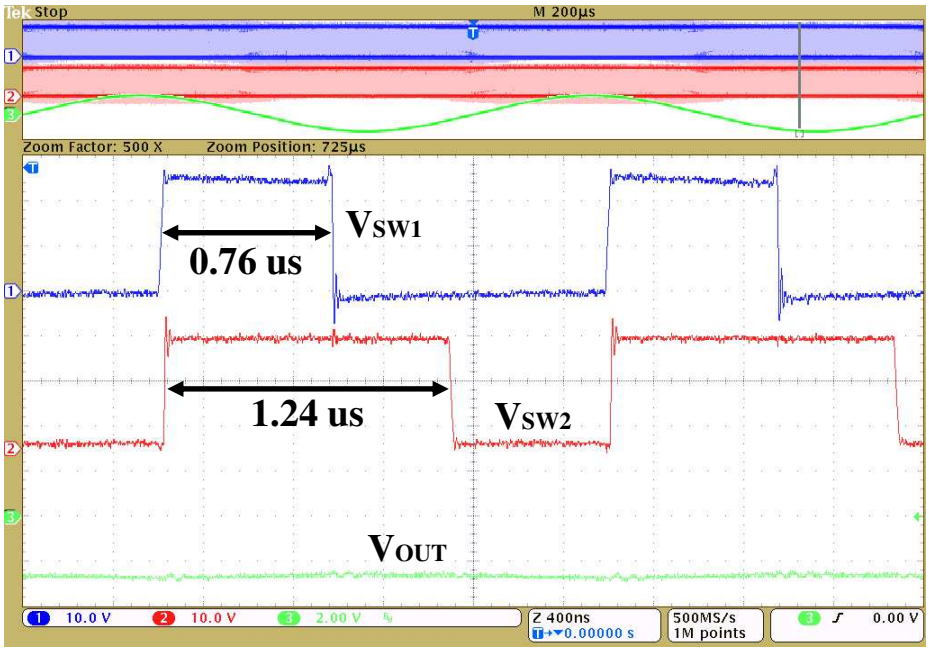


Figure 4.20: Experimental results of steady state operation of 10 kHz output



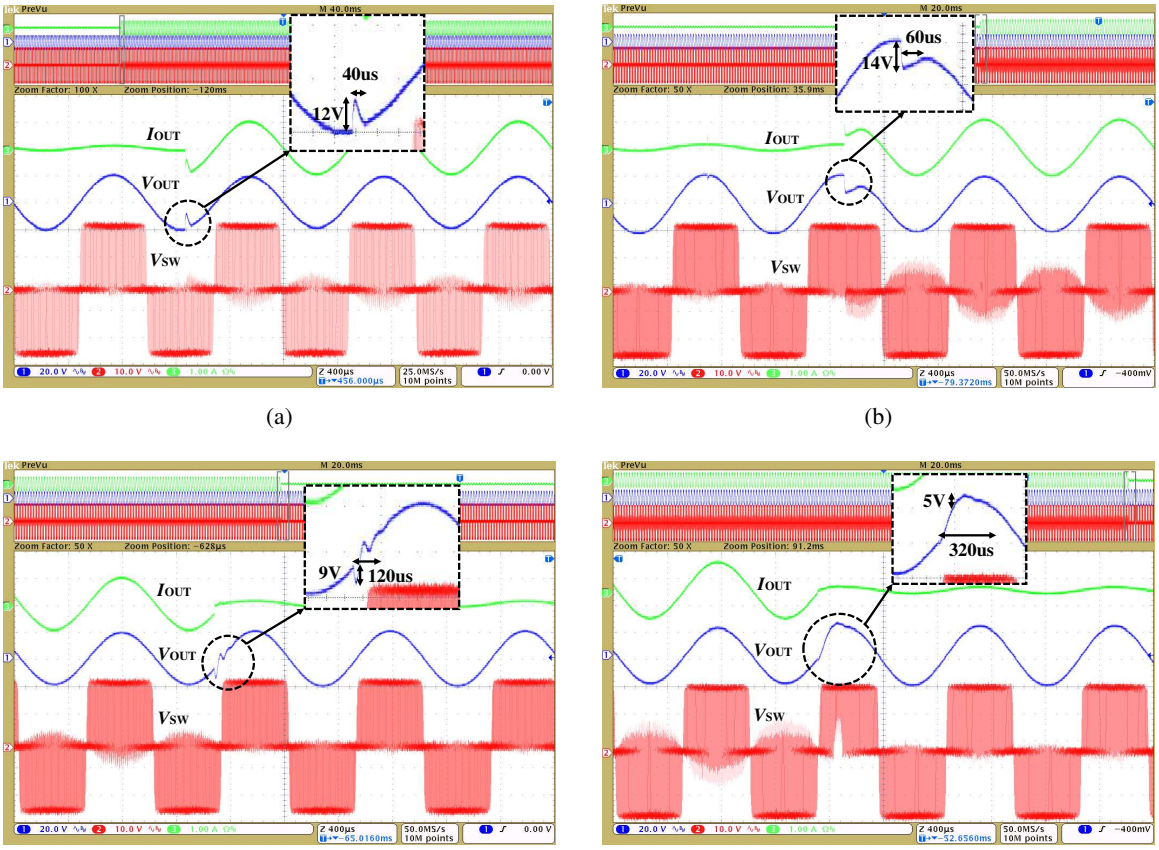
(a)



(b)

Figure 4.21: Experimental results of steady state operation showing both branches switching nodes and differential output voltage waveform. (a) When output voltage is positive (b) when output voltage is negative

Dynamic Response: The load response of the DISMC CDA was evaluated under a step load change from 20 Ω to 200 Ω, and the results were compared to those of a PI controller using the same system parameters. Figures 4.22a and 4.22b illustrate the transition from a light load (200 Ω) to a



(a) (b)

(c) (d)

Figure 4.22: Experimental results of dynamic response under step load changes. (a) Light load jumps to high load, (a) DISMC (b) PI, Heavy load jumps to light load, (c) DISMC (d) PI.

heavy load ($20\,\Omega$) for the DISMC and PI controllers, respectively. Two key aspects were observed: the extent of voltage deviation from the nominal voltage trajectory and the time required to regulate the voltage back to steady-state. For the DISMC controller, the output voltage deviated by $12\,\mathrm{V}$ and returned to normal operation within $40\,\mu\mathrm{s}$, whereas the PI controller exhibited a deviation of $14\,\mathrm{V}$ and required $60\,\mu\mathrm{s}$ for regulation. This indicates that the DISMC controller showed better performance than the PI controller in terms of both voltage deviation and regulation time, though the improvement was relatively small. For the transition from a heavy load to a light load, the DISMC controller showed a slightly larger voltage deviation of $9\,\mathrm{V}$ compared to $5\,\mathrm{V}$ for the PI controller. However, it achieved a significantly faster regulation time of $120\,\mu\mathrm{s}$ compared to $320\,\mu\mathrm{s}$ for the PI controller, with reduced distortion.

It is important to note that the comparison between the DISMC and PI controller presented in

this dissertation was conducted under identical system specifications and on the same PCB-level implementation. While many existing works on DISMC have been realized at the integrated circuit (IC) level—where inherent advantages such as minimized parasitics and reduced propagation delays contribute to enhanced performance—this dissertation focuses on a discrete PCB-level implementation. At this level, the effects of delay, signal distortion, and parasitic elements are more pronounced, making direct performance comparisons with IC-level implementations less meaningful. Therefore, the comparative analysis provided in this work is limited to the PCB level and specifically contrasts the performance of the proposed DISMC with that of a conventional PI controller under consistent conditions.

Frequency measurement: The THD was measured across different modulation indices, and the results are shown in Figure 4.23. A THD as low as 0.83% was observed. However, the THD increases as the modulation index decreases or increases beyond a certain range. At lower modulation indices, the increase in THD is attributed to the reduced resolution of the ADC output due to lower voltage levels. Conversely, at higher output voltages, the CDA output becomes more distorted because of fixed design parameters, such as the scaling coefficients of the reference current and the integral coefficients. As the output voltage increases, fine-tuning of these parameters is required to reduce distortion.

4.3 Conclusions

A CDA based on DISMC was designed and validated through both simulation and experimental results. The design process began with the state-space model of the CDA, from which the control signal was derived, using the inductor current and output voltage tracking errors, along with their integrals, as state variables. The reaching and stability conditions were thoroughly analyzed, and the controller gains were subsequently determined. The full-bridge CDA was simulated, tested, and compared with a conventional PI controller. The results demonstrated that the proposed DISMC operates reliably and offers improved tolerance to load and line variations compared to the PI controller. Additionally, the DISMC exhibited superior immunity to large signal transitions and achieved faster regulation speeds than the PI controller.

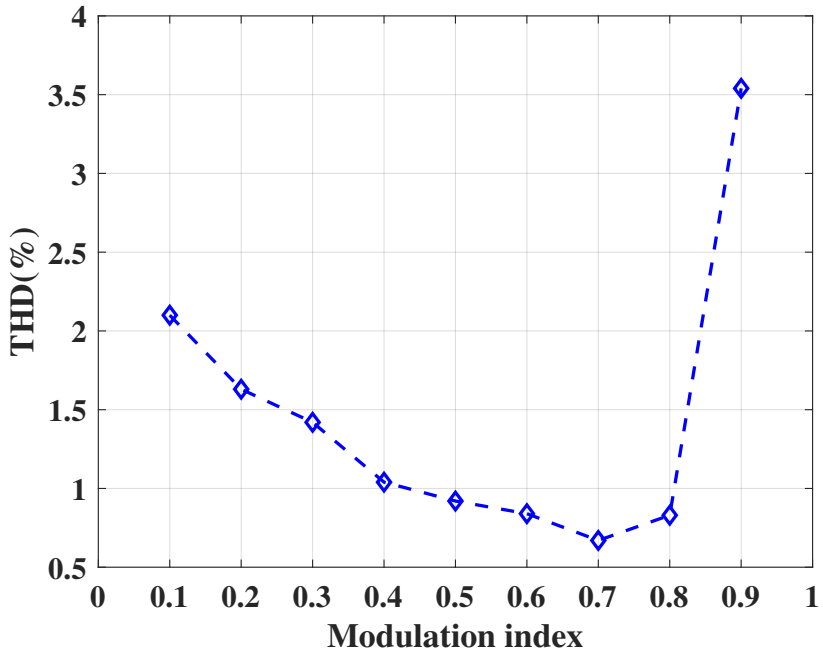


Figure 4.23: Measured THD versus modulation index

A critical insight gained during this work is the central role of precise output voltage and inductor current sensing in achieving low-distortion performance. Since the DISMC algorithm heavily relies on real-time feedback of these signals to compute the control law, any sensing inaccuracy or noise directly impacts the controller's effectiveness. Inaccurate measurements can result in distorted output waveforms, degraded signal tracking, and increased THD. Therefore, special care must be taken in the design of the sensing circuitry, including the selection of high-precision components, implementation of low-noise analog front-ends, and use of appropriate filtering techniques to preserve the fidelity of the feedback signals.

Chapter 5

Conclusions and Future Work

This chapter presents a comprehensive summary of the key findings and contributions of this research on fully differential switching amplifiers. The work addressed critical challenges in achieving high efficiency, linearity, and compact design for low-power applications, particularly for differential-output sine wave loads in industries such as automotive and critical power systems. By leveraging GaN power transistors and advanced control techniques—SHEPWM and DISMC—this research demonstrated significant advancements over traditional amplifier architectures.

The conclusions of this study are discussed, focusing on the improvements achieved in efficiency, linearity, and integration. In addition, this chapter outlines recommendations for future research, exploring opportunities to further enhance the performance of switching amplifiers, integrate emerging technologies, and address the limitations encountered during this work. These recommendations aim to serve as a foundation for continued progress in the development of efficient and robust amplifier systems for low-power applications.

5.1 Conclusions

This research has presented significant advancements in the design and implementation of low-power switching amplifiers and inverters, addressing key challenges in achieving high efficiency, linearity, and adaptability for low-power (several mW to W) industry applications. A full-bridge

low-power inverter utilizing SHEPWM was developed, targeting high fundamental output frequencies ranging from 4 kHz to 10 kHz. Unlike conventional approaches focused on high-power, low-frequency applications, this work demonstrated the feasibility and effectiveness of SHEPWM in low-power systems, achieving efficient operation across a wide frequency range while maintaining a fixed filter cutoff frequency.

The introduction of an innovative FPGA-based hardware architecture for SHEPWM implementation marked another key contribution. This architecture provided real-time configurability of output amplitude and frequency, enabling dynamic adaptation to varying operating conditions without requiring extensive storage or computational resources. This flexibility significantly enhanced the practical applicability of the SHEPWM algorithm in low-power systems, making it a robust and versatile solution.

Additionally, the integration of compact 3D components within a SiP design demonstrated the potential for substantial reductions in PCB area. The SiP design was shown to support both DC-AC inversion and DC-DC conversion, offering a versatile and space-efficient solution for integrated power electronics. While the current implementation utilized only a subset of the SiP components, the work highlighted promising opportunities for further miniaturization and optimization in future designs.

Furthermore, the development and validation of a fully differential CDA based on DISMC showcased the efficacy of advanced control techniques in improving system performance. Through simulation and experimental results, the proposed DISMC was shown to offer superior tolerance to load and line variations, faster regulation speeds, and better immunity to large signal transitions compared to conventional PI controllers.

In summary, this research has contributed to the advancement of low-power switching amplifiers and inverters through innovative control strategies, hardware architectures, and integration techniques. These findings not only address existing limitations but also pave the way for future developments in efficient and compact power electronics for low-power applications.

5.2 Recommendations for Future Work

Given the precision achieved in the open-loop configuration, as evidenced by the low errors in both switching angles (and consequently THD) and MI, future work could focus on integrating closed-loop control to further enhance the performance of the SHEPWM technique. Closed-loop control has the potential to dynamically adjust switching angles and modulation indices in real-time, addressing variations in load and line conditions. This could significantly improve the robustness and adaptability of the system, particularly in applications requiring stringent harmonic suppression and precise output regulation under variable operating conditions. The fine control over the modulation index achieved in this work, combined with the multifunctional capabilities of the SiP design, provides a strong foundation for such advancements. The integration of closed-loop feedback could leverage real-time sensing and signal conditioning to enable automated error correction, further reducing harmonic distortion and improving overall system efficiency. Additionally, closed-loop control could enhance the scalability of the SHEPWM technique, allowing it to adapt to a broader range of load types and operational scenarios. In the SHEPWM technique, since the THD tends to be higher at lower fundamental frequencies, one potential direction for future work is to scale up the number of switching angles at these frequencies. This approach could enhance the cancellation of lower-order harmonics, thereby improving overall spectral performance.

In this work, discrete GaNFETs were employed as power transistors, leveraging their compact size and superior switching capabilities. While this approach effectively demonstrated the advantages of GaNFETs in achieving high efficiency and fast switching performance, future research could focus on integrating GaNFETs with gate driver circuitry on the same die. This integration has the potential to significantly reduce the overall system size and improve performance. By eliminating the need for wire bonding between the GaNFETs and gate drivers, such integration would minimize parasitic inductance, which is a primary contributor to switching ringing and voltage overshoots. Reducing these parasitics not only improves switching performance but also enhances system reliability by mitigating issues such as shoot-through and EMI. Additionally, the integration of GaNFETs and gate drivers could lead to simplified PCB layouts and reduced assembly complexity, further contributing to the miniaturization of power electronics systems.

In DISMC, the system typically requires sensing of output voltage, inductor current, and capacitor current. For a full-bridge configuration, this necessitates a total of six signal conditioning channels and six ADC channels, which can be considered relatively complex. However, since output voltage and capacitor current are inherently related, there is potential to reduce the number of sensing channels. Specifically, by exploiting the relationship between these two variables, it may be possible to eliminate one of the channels, thereby reducing the total number of channels required to four in the full-bridge design. However, this reduction introduces a challenge: the output voltage and capacitor current are phase-shifted by 90 degrees, which requires careful handling to ensure accurate measurement and control. To maintain system performance and stability, the controller design would need to incorporate more sophisticated computational techniques, such as phase compensation or advanced filtering algorithms, to account for this phase shift. These methods would allow for the effective use of fewer sensing channels without compromising the precision and reliability of the control system. Future research could focus on developing such advanced techniques for reducing the number of sensing channels in DISMC-based systems. By optimizing the controller's ability to handle phase shifts and relationships between sensing variables, the overall system complexity could be reduced, leading to simpler designs and lower costs while maintaining performance. This would make DISMC more practical for real-world applications, particularly in compact and cost-sensitive power electronics systems. The controller gains in this work are derived using an output scaling factor of 0.2, with a reference voltage peak value of $2.4\,\mathrm{V}$, resulting in an output voltage of $24\,\mathrm{V}$ peak-to-peak. This is half of the maximum achievable output voltage of $48\,\mathrm{V}$ peak-to-peak. If the output scaling factor or reference voltage amplitude changes, the controller gains must be adjusted accordingly. In this study, the same controller gains, derived for a fixed output voltage, are used across all modulation indices. As a result, a higher THD is observed at a modulation index of 0.9. To reduce THD at higher modulation indices, the controller gains should be optimized for each specific condition. A promising approach for future work would be to implement an adaptive control scheme that senses the output voltage and adjusts the controller gains dynamically using a lookup table (LUT). This LUT would store precomputed controller gains for different output voltage levels or modulation indices, ensuring consistently low THD across the entire operating range.

Future work could explore using multilevel topologies, particularly the flying capacitor multilevel configuration, to reduce the size of the LC filter in converters. By balancing the flying capacitor voltage at half of the converter's input voltage, a five-level switching waveform is achieved, which closely resembles a sine wave and reduces the need for large LC filters. However, in SHEPWM, voltage balancing is challenging as not all switching patterns support every modulation index, limiting achievable output voltages. In contrast, DISMC, using standard PWM modulation, can achieve all modulation indices and corresponding output voltages, making it more suitable for maintaining flying capacitor voltage balance. This flexibility allows for more efficient voltage regulation and the use of smaller LC filters, contributing to a more compact converter design. Future research could focus on optimizing DISMC-based control for multilevel topologies to further reduce converter size and improve performance.

Appendix A

DISMC Class-D Amplifier Printed Circuit Board

The top level schematic of double integral sliding mode control (DISMC) class-D amplifier (CDA) is shown below A.13.

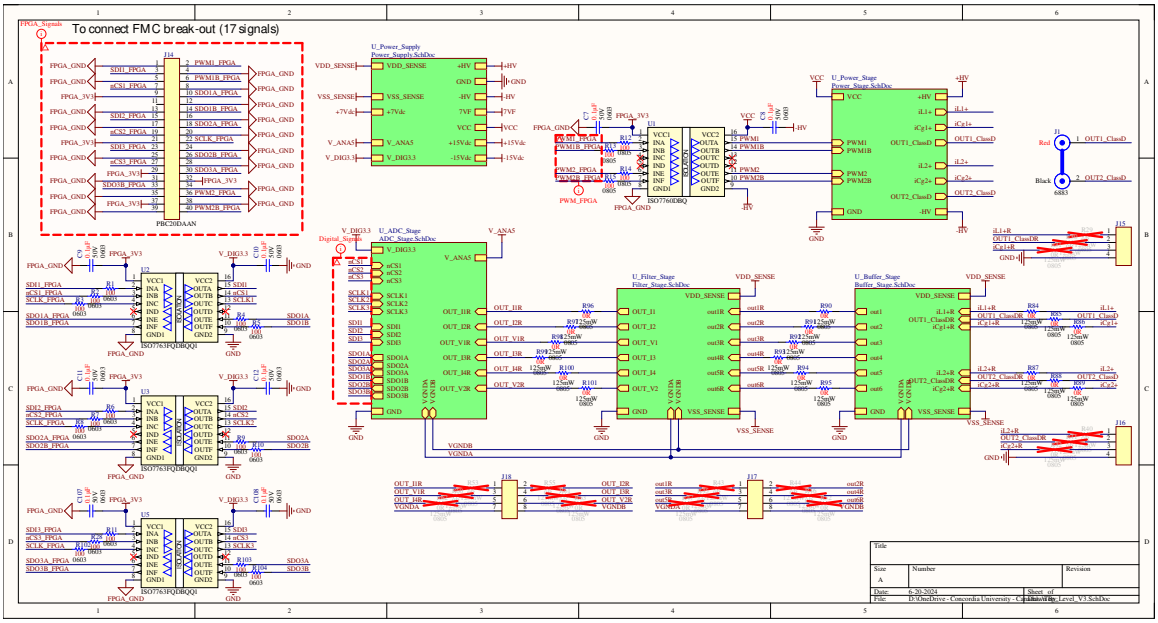


Figure A.1: Top level schematic

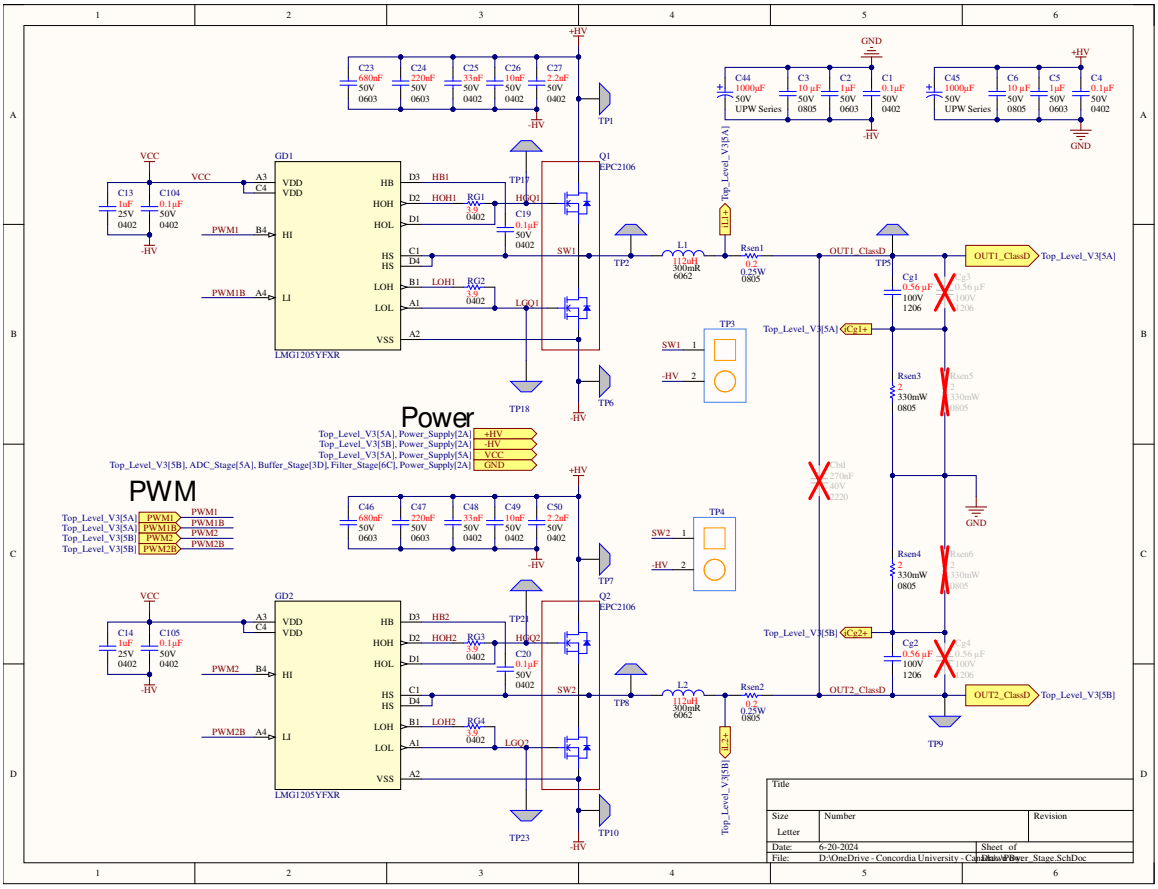


Figure A.2: Power stage including gate drivers, power GaNFETs and LC filters

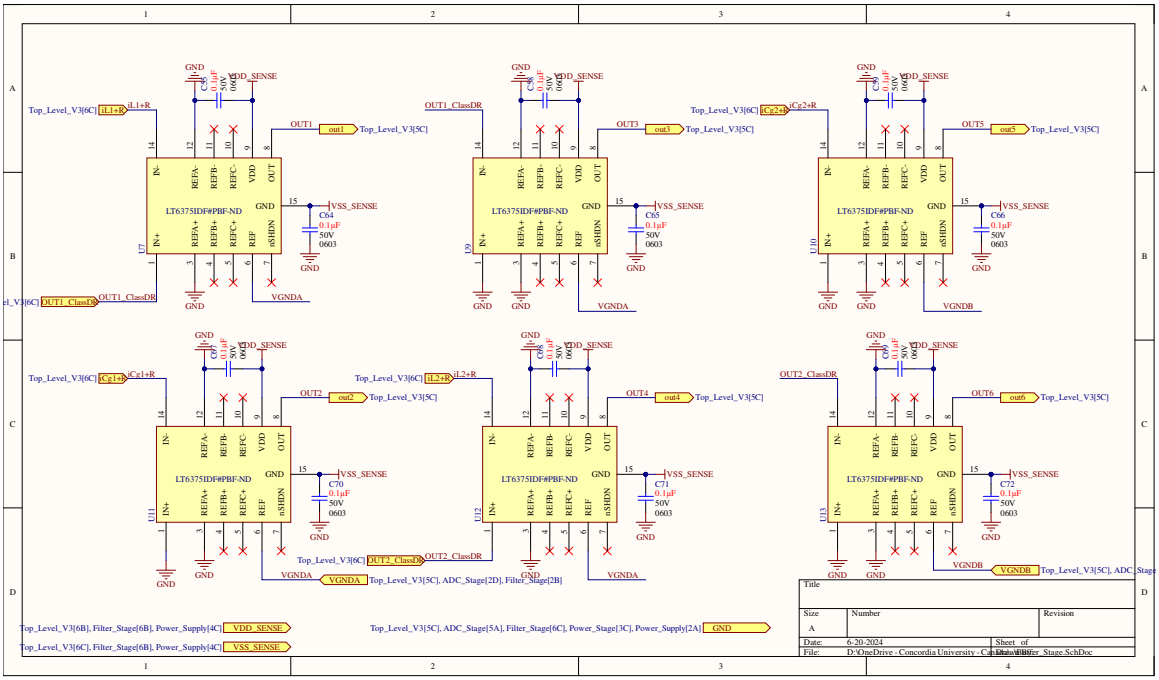


Figure A.3: Buffer stage

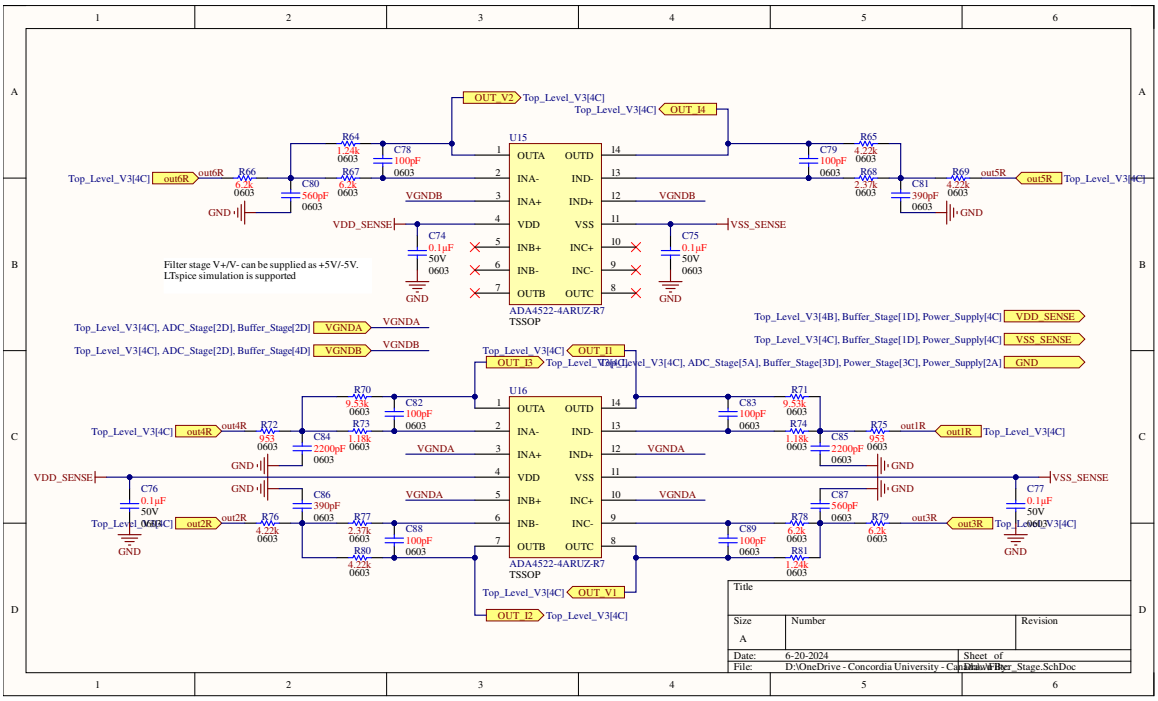


Figure A.4: Filter stage

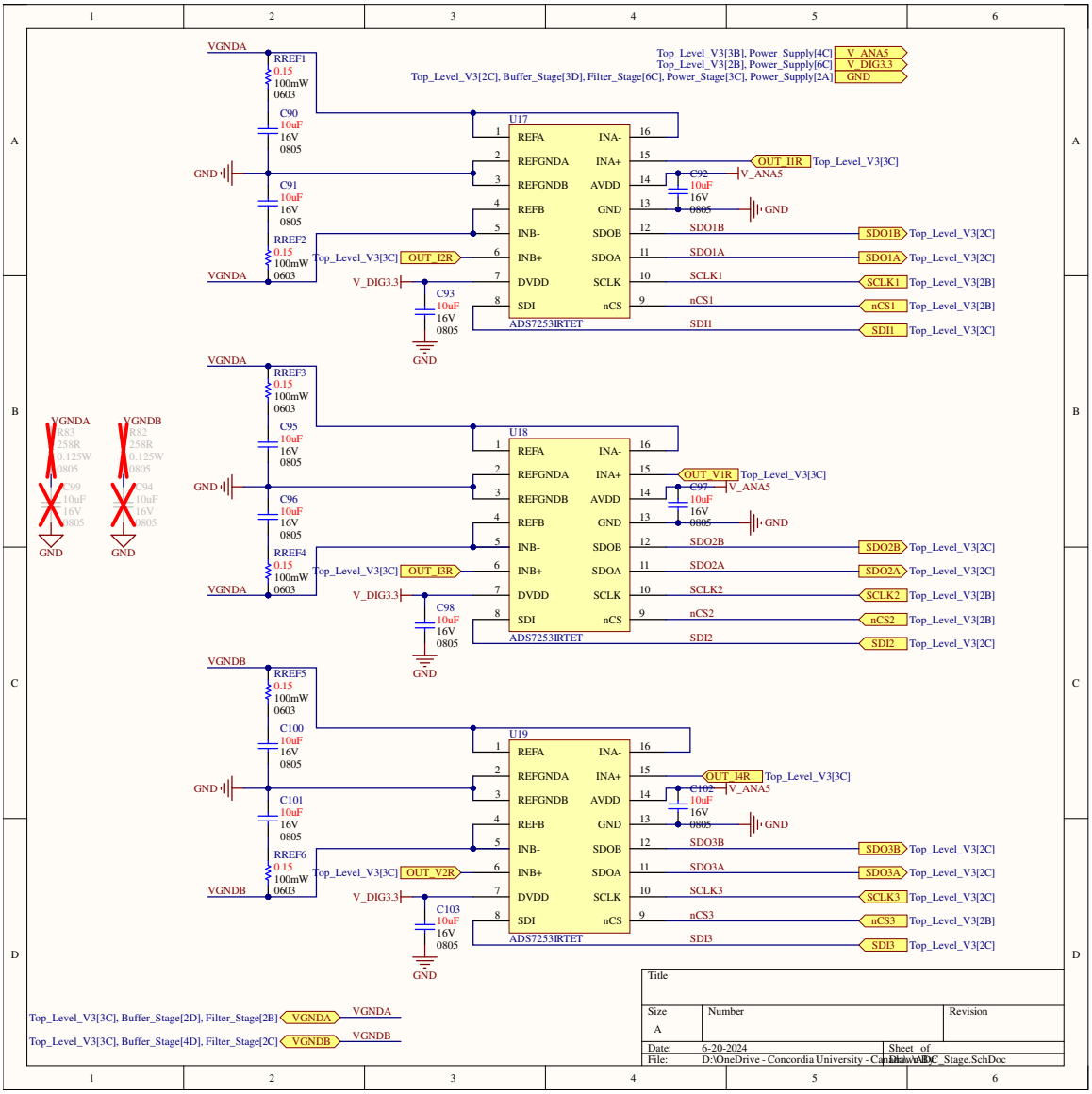


Figure A.5: Analog to digital converters

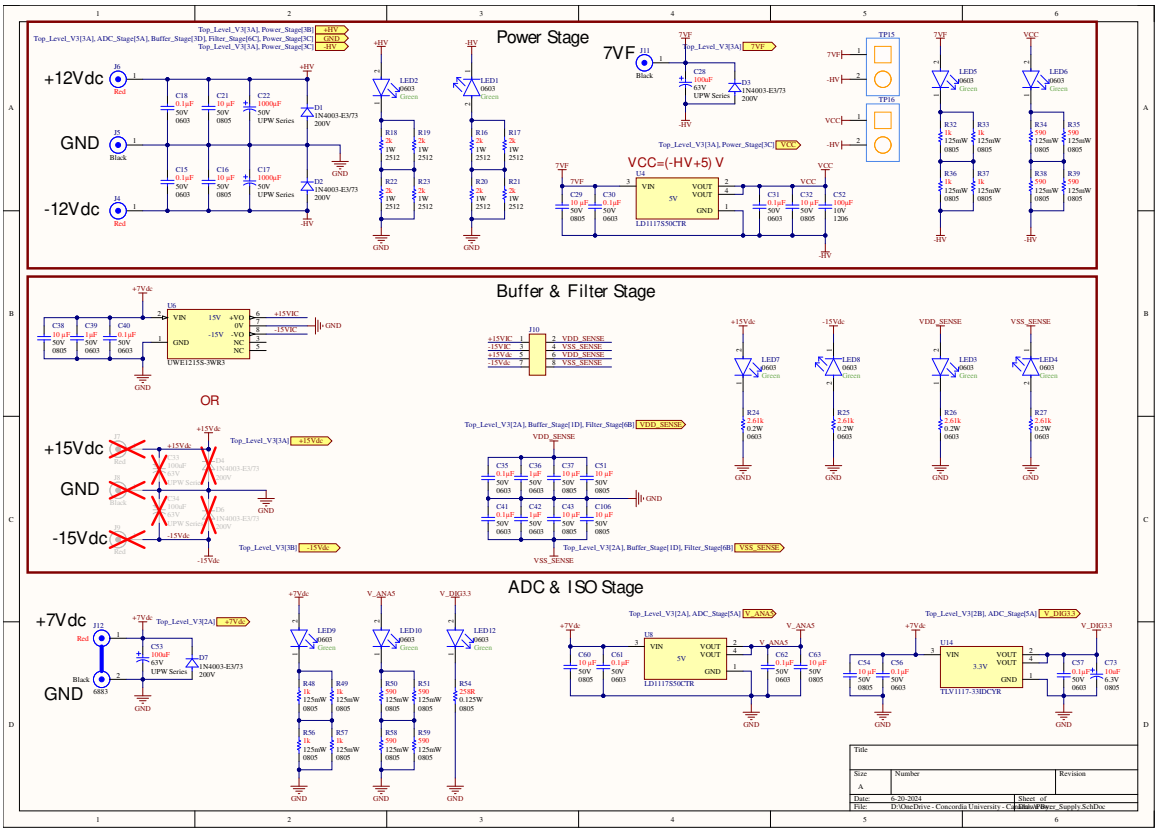


Figure A.6: Power supplies

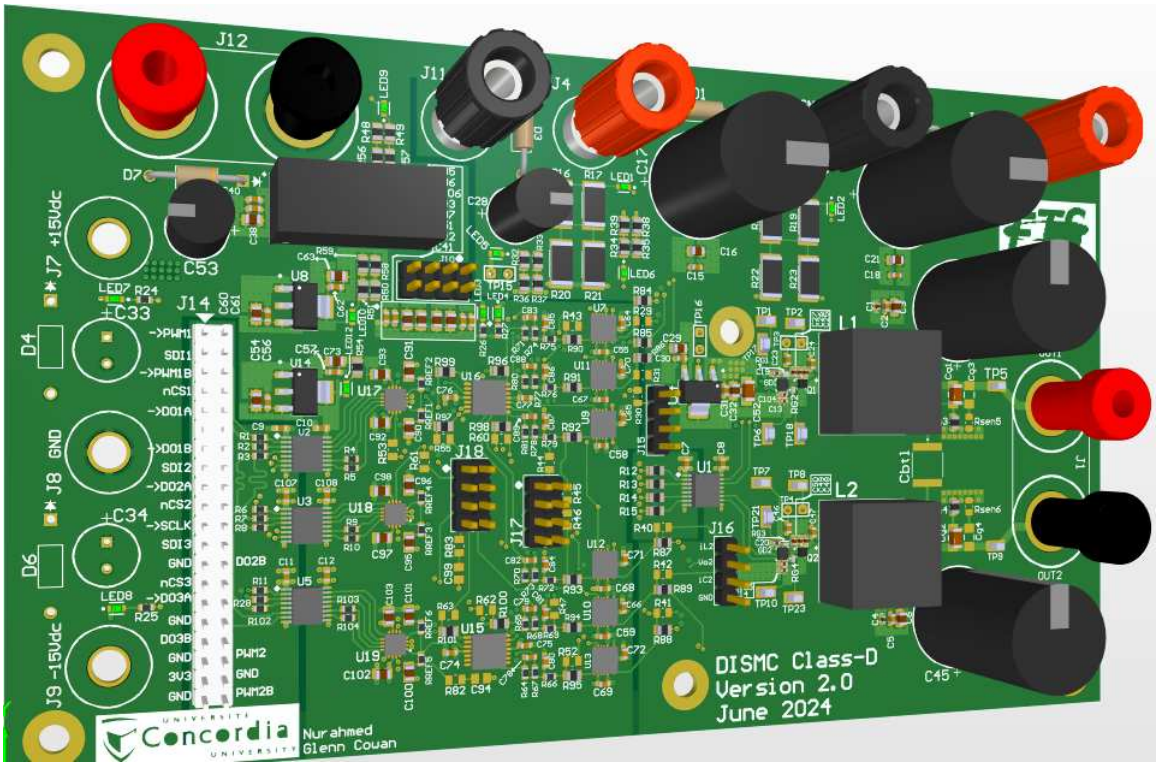


Figure A.7: 3D view of the DISMC Class-D PCB

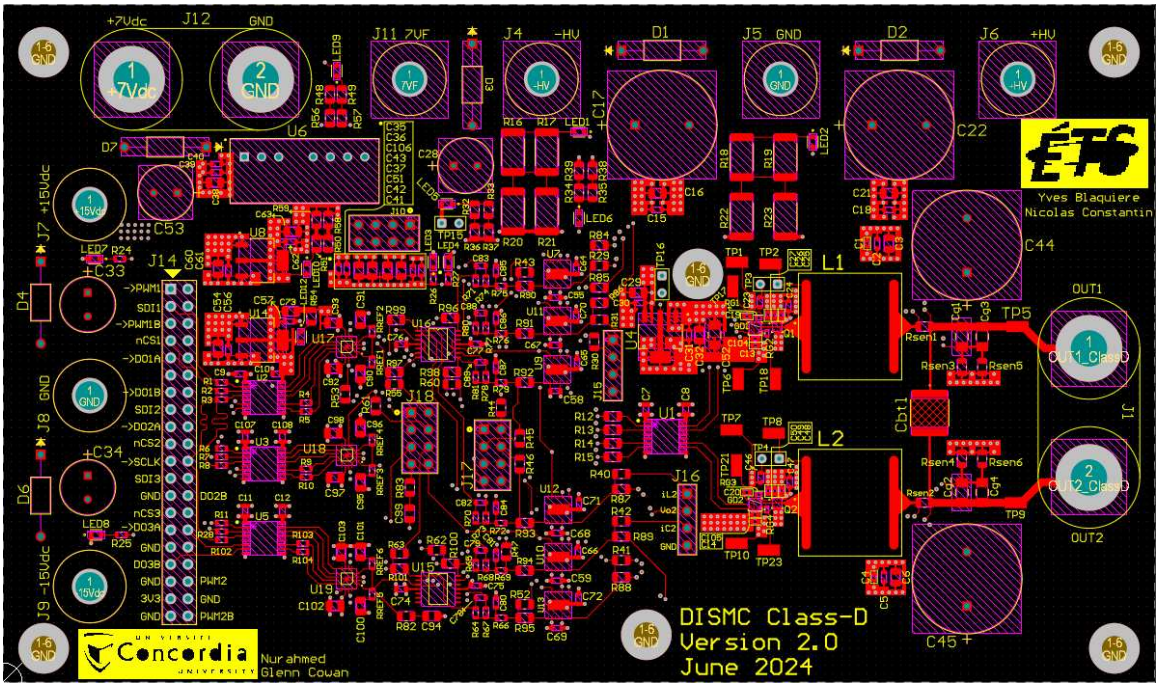


Figure A.8: Layer 1 of the PCB - components placement and signal traces on top

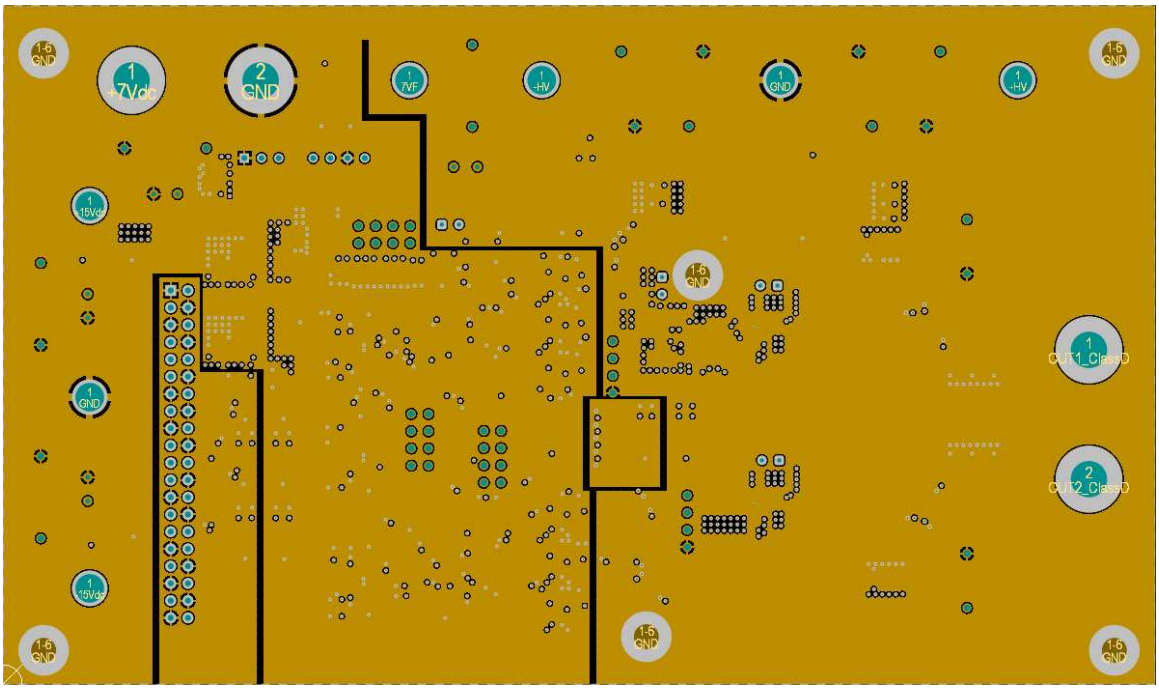


Figure A.9: Layer 2 of the PCB - ground planes

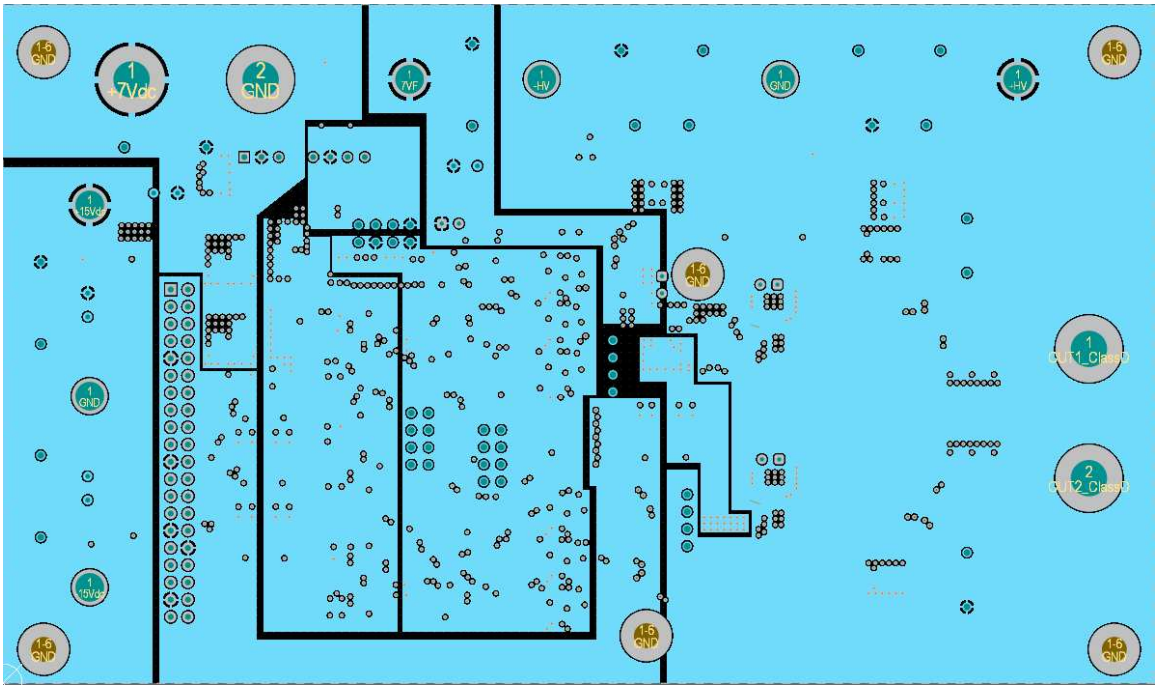


Figure A.10: Layer 3 of the PCB - power planes

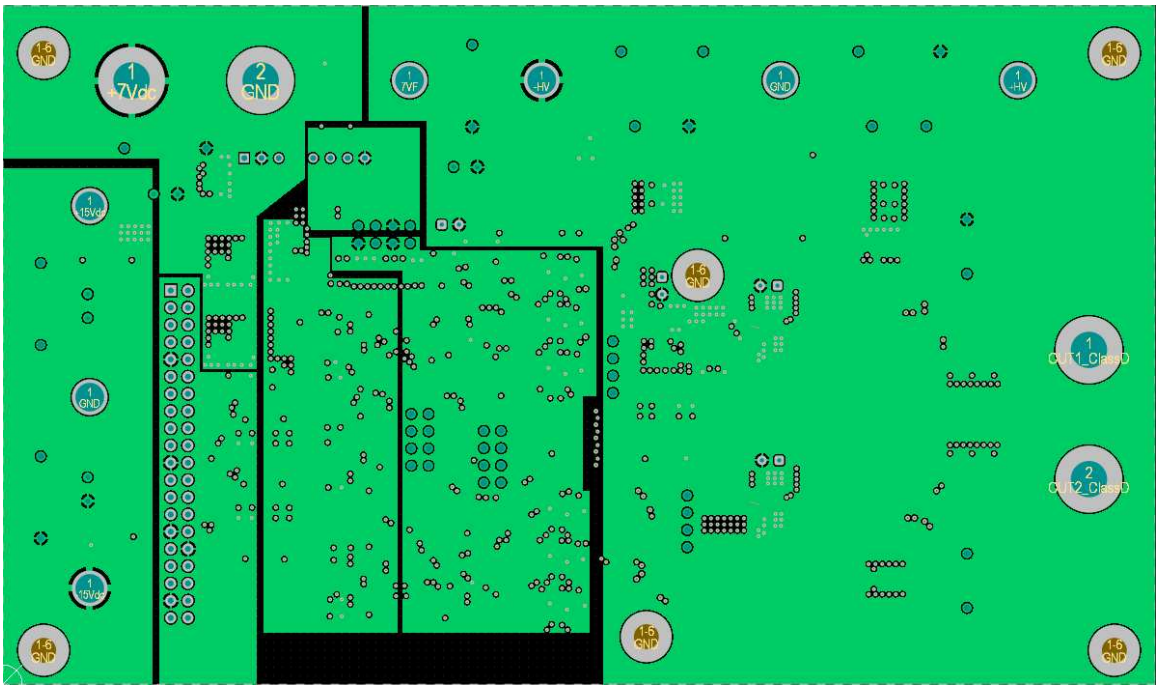


Figure A.11: Layer 4 of the PCB - power planes

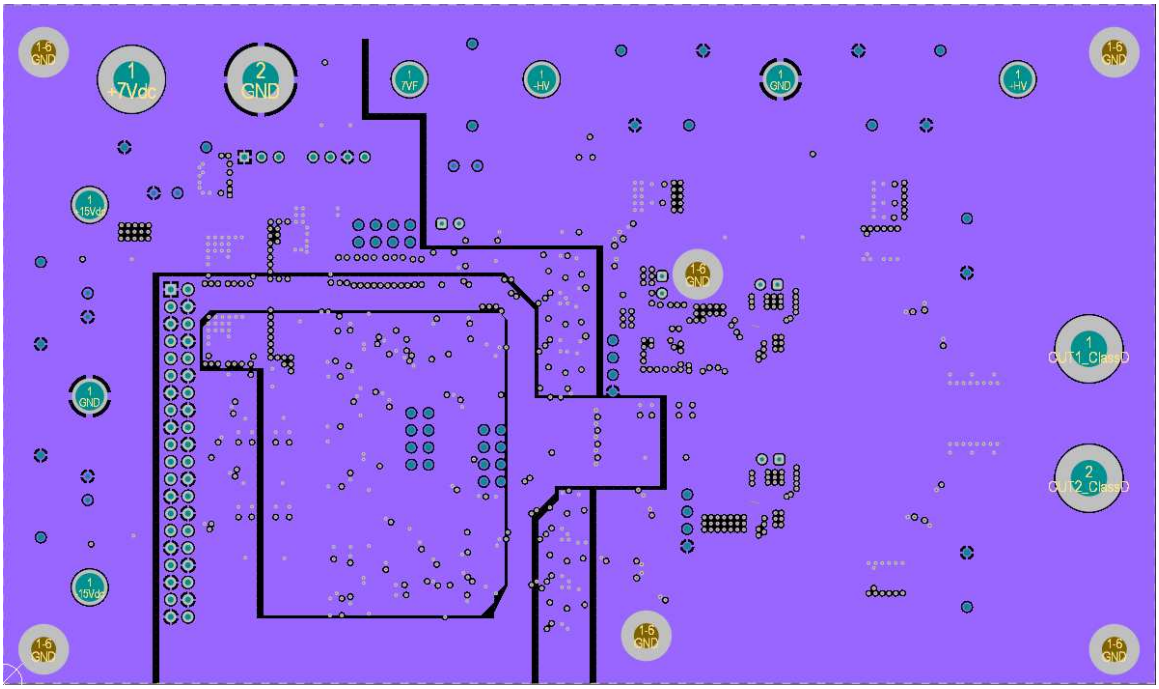


Figure A.12: Layer 5 of the PCB - ground planes

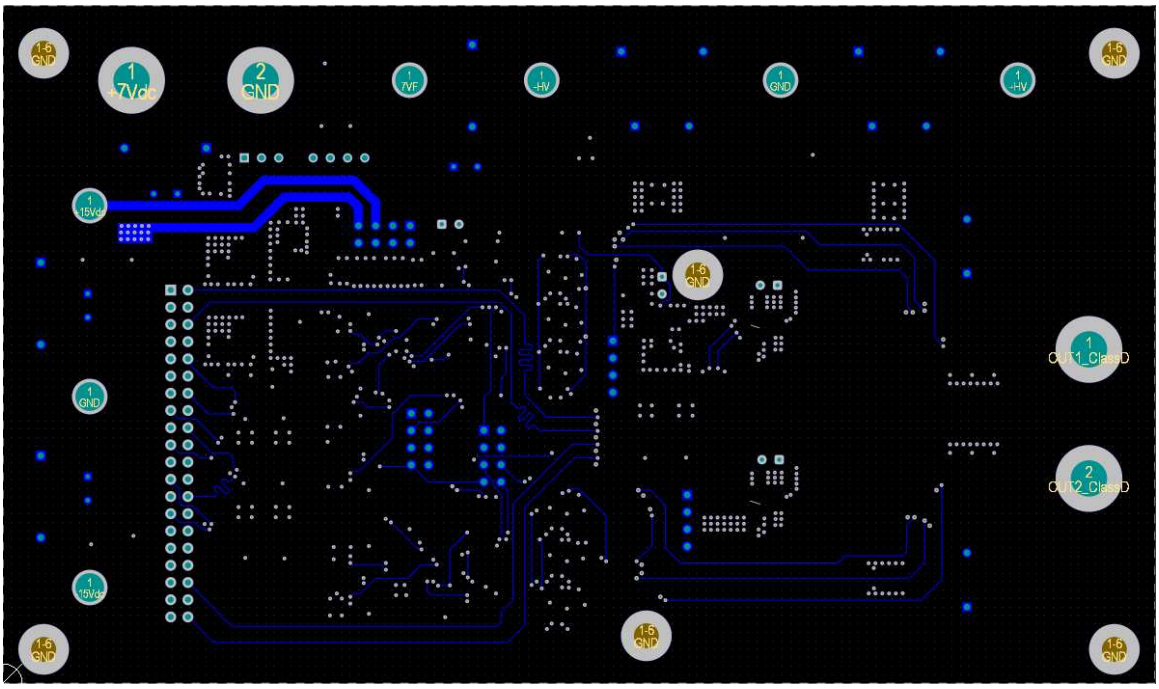


Figure A.13: Layer 6 of the PCB - signal traces on bottom

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