Design and Implementation of a Linear Optical Receiver

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This is to certify that the thesis prepared

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Abstract

Design and Implementation of a Linear Optical Receiver

Sara Radfar

Rising internet traffic from AI and bandwidth-intensive applications has increased the demand for fast, low-power optical links in modern data centers. Multi-level modulation schemes such as four-level pulse amplitude modulation (PAM-4) improve spectral efficiency and throughput while relaxing bandwidth requirements. However, PAM-4 imposes strict linearity demands on the optical receiver's analog front-end, particularly the main amplifier.

This thesis presents a highly linear, power-efficient main amplifier for PAM-4 and NRZ optical receivers, implemented in 65-nm CMOS. The design uses a g_m/g_m topology with interleaved active feedback (IAFB) to extend bandwidth without passive inductors. Linearity is further improved by reducing third-order distortion through resistive voltage dividers at the feedback inverters' inputs and by increasing their gain. Post-layout simulations show superior bandwidth, linearity, and vertical eye opening (VEO) compared to a conventional Cherry–Hooper amplifier, including a 67% reduction in total harmonic distortion (THD) at a 500-mV_{pp} output swing.

To mitigate channel impairments, equalization is integrated directly into the main amplifier by introducing a pole within the active feedback loop. This removes the need for a separate continuous-time linear equalizer (CTLE), reducing chip area and power. The proposed amplifier is part of a four-channel differential optical receiver, fabricated with a total chip area of 2 mm × 1 mm. Post-layout results indicate 10-Gb/s per-channel operation for both NRZ and PAM-4, with about 30 mW power consumption per channel.

Acknowledgments

I would like to express my sincere gratitude to my supervisor, Prof. Glenn Cowan, for his invaluable guidance throughout this program. I have gained significant knowledge from his expertise and passion for analog and mixed-signal IC design, and I am truly grateful for the opportunity to be part of his enthusiastic team at Concordia University.

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Words cannot fully convey my gratitude to my beloved family, whose love and support have carried me through this journey. To my mother, who has always been my greatest source of encouragement and has inspired me to pursue ambitious goals. To my father, whom I lost during this program. Thank you for always believing in me; your presence is deeply missed. And to my sister, Marjan, a constant source of support; thank you for setting the bar so high and showing me what is possible.

Lastly, I would like to thank my husband, Amin, with all my heart. We began this journey together, and I could not have made it through without his unwavering support. He has always been by my side, seeing the best in me and reminding me of my capabilities when I needed it most.

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Chapter 1

Introduction

The exponential growth of internet traffic, driven by bandwidth-intensive services and AI applications, has necessitated a rapid expansion of data centers, which rely heavily on high-speed interconnects. AI workloads require massive data movement between GPUs, TPUs, and storage systems, demanding ultra-fast, high-bandwidth communication. However, electrical interconnects often become bottlenecks due to their high-frequency losses and limited capacity. As a result, optical interconnects have become essential, offering superior speed, reliability, and power efficiency compared to their electrical counterparts [1]. Optical transceivers enable high-bandwidth, low-latency connections in data centers, allowing efficient model training and inference, which is critical for modern AI applications.

To increase data transmission rates in optical links, intensity modulation and direct detection (IMDD) transceivers are widely used. While 2-level pulse amplitude modulation (PAM-2), often referred to non-return-to-zero (NRZ) signaling, requires a very large circuit bandwidth at high speeds, multi-level modulation formats such as PAM-4 reduce this bandwidth requirement. PAM-4, which encodes two bits per symbol using four discrete amplitude levels, has become widely adopted due to its improved spectral efficiency over PAM-2 (NRZ). This allows for a higher data rate while maintaining reduced bandwidth requirements. However, PAM-4 introduces new design challenges, including reduced signal level separation, increased susceptibility to noise and distortion, and stringent linearity requirements for the analog front-end [2].

Optical receiver design is critical in PAM-4 systems, as the eye diagram becomes both vertically

and horizontally compressed. To ensure proper detection, an analog front-end must exhibit high linearity, wide bandwidth, and low noise. Due to the possibility of insufficient Transimpedance Amplifier (TIA) gain to achieve logical levels, a high-gain amplifier, known as the main amplifier (MA), is required after the TIA. The nonlinearity of the optical receiver is primarily dictated by the final stages of the MA. Among various topologies, the Cherry-Hooper (CH) amplifier is a common choice due to its wide bandwidth [3,4]. However, studies have shown that its linearity is insufficient for PAM-4 optical links [5]. To address this, the g_m/g_m amplifier topology, which consists of a transconductor followed by a diode-connected inverter load to cancel transconductor nonlinearities, has been explored [5–7]. While g_m/g_m amplifiers offer superior linearity, their bandwidth is lower than that of CH amplifiers, necessitating the use of bandwidth extension techniques, especially in less advanced technologies.

1.1 Motivation

High-speed optical communication systems require efficient receiver designs to handle increasing data rates and bandwidth demands. Designing optical receivers for high-speed NRZ signaling demands an extremely wide bandwidth, which presents significant design challenges. To overcome this limitation, multi-level signaling schemes such as PAM-4 have been introduced.

In PAM-4 systems, receiver design is particularly challenging due to the reduced vertical and horizontal eye openings, which degrade signal integrity. The analog front-end must exhibit high linearity, wide bandwidth, and low noise to accurately recover the transmitted signal. Furthermore, to be competitive with NRZ receivers, PAM-4 receivers must operate at low voltages, demonstrate robustness against process and temperature variations, and minimize chip area [5].

A key limitation in the design of PAM-4 optical receivers is the nonlinear behavior of conventional main amplifiers, which can distort the signal levels and degrade system performance. The Cherry-Hooper amplifier, a common choice for broadband design, offers a wide bandwidth but lacks sufficient linearity for PAM-4. In contrast, the g_m/g_m-based topology demonstrates enhanced linearity, making it a promising candidate for linear optical receivers. However, its limited bandwidth necessitates additional extension techniques to meet high-speed performance requirements.

To enhance bandwidth without relying on passive inductors, the interleaving active feedback (IAFB) technique [8] has been developed. In this work, the combination of a g_m/g_m-based main amplifier with IAFB results in a highly linear PAM-4 main amplifier, making it a strong candidate for high-speed optical receiver designs.

As data rates continue to rise, signal degradation due to channel impairments, such as attenuation, inter-symbol interference (ISI), and impedance mismatches, becomes increasingly significant, leading to elevated bit error rates and degraded system performance. In linear-drive optical receiver architectures, the front-end amplifier drives a lossy channel before the signal reaches the clock and data recovery (CDR) unit. This intermediate channel introduces frequency-dependent loss and ISI, especially for multilevel signaling schemes like PAM-4. To mitigate these effects, receiver-side equalization becomes essential. This work focuses on the design of an equalizing main amplifier that incorporates high-frequency peaking (HFP) within the front-end itself [9]. By embedding equalization directly into the main amplifier, this approach reduces the need for a separate continuous-time linear equalizer (CTLE) stage, enabling a more compact and energy-efficient receiver solution.

1.2 Publications and Contributions of the Author

1) S. Radfar and G. Cowan, "Linearity Enhancement for Inverter-Based Optical Receivers Employing Active Feedback," IEEE Midwest Symp. on Circuits and Systems (MWSCAS), Springfield, MA, USA, 2024.

2) S. Radfar and G. Cowan, "Interleaving Active Feedback in Inverter-Based Optical Receivers for Bandwidth Extension and Linearity Improvement," IEEE Int. Symp. on Circuits and Systems (ISCAS), Singapore, 2024.

1.3 Thesis Organization

Chapter 2 begins by introducing modulation formats, eye diagrams, and key linearity metrics used in optical transceivers, such as Total Harmonic Distortion (THD) and Ratio Level Mismatch (RLM), to evaluate performance in PAM-4 systems. Then it reviews inverter-based optical receiver designs and examines a bandwidth extension technique that avoids the use of inductors. Finally,

the chapter discusses methods for embedding equalization capability into the receiver front-end to compensate for losses introduced by the downstream electrical channel, with a particular emphasis on HFP.

In **Chapter 3**, a methodology for designing and further enhancing a highly linear main amplifier is proposed, with simulation results presented and compared to the commonly used Cherry-Hooper amplifier topology and the g_m/g_m-based topology.

Chapter 4 explores an approach to equalizing the main amplifier without using a separate CTLE stage. The technique is implemented on the proposed highly linear main amplifier, enhancing the signal integrity of the structure when used with a lossy transmission line. This results in a power- and area-efficient linear main amplifier.

Chapter 5 discusses the implementation of the proposed linear optical receiver with the equalizing main amplifier, designed for fabrication in 65 nm CMOS technology. The method for making the structure fully differential is detailed, and post-layout simulation results are presented.

Finally, **Chapter 6** compares the proposed linear optical receiver to existing ones, summarizes the thesis, and presents future objectives.

Chapter 2

Background and Literature Review

Illustrated in Fig. 2.1, the initial stage of a standard CMOS optical receiver (RX) consists of a photodiode (PD) followed by a transimpedance amplifier (TIA). Since the PD generates a small current and most subsequent processing is voltage-based, the TIA is employed to convert the input current into a voltage signal. However, the TIA output may not provide sufficient voltage swing to reach logical levels, necessitating the use of a high-gain stage, known as the main amplifier (MA). The MA significantly influences the overall linearity of the receiver and plays a critical role in its performance. In this chapter, after introducing two main concepts and linearity metrics in optical transceivers, we explore inverter-based MA designs and review existing methods from the literature aimed at improving linearity, bandwidth, and reducing inter-symbol interference (ISI).

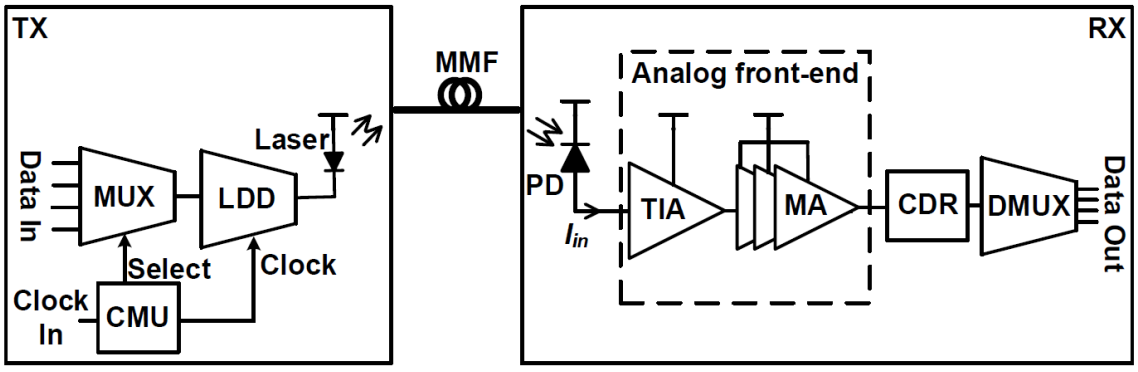


Figure 2.1: Block diagram of a typical short-reach optical link [9].

2.1 Modulation Formats

In high-speed communication systems, digital data is commonly transmitted using pulse amplitude modulation (PAM), as described in Fig. 2.2 [10]. The simplest form is PAM-2, also known as non-return-to-zero (NRZ) (Fig. 2.2 (a)), where each symbol represents a single bit using two distinct signal levels, typically a high level for logic 1 (L_1) and a low level for logic 0 (L_0). The signal maintains its level throughout the bit period (T_b), which is why it is referred to as "non-return-to-zero". NRZ is decoded at the receiver by comparing the signal against a single threshold level (L_d) once per unit interval (UI). To achieve higher data rates without reducing the UI, a more advanced modulation scheme like PAM-4 can be used, which is shown in Fig. 2.2 (b). PAM-4 transmits two bits per symbol (T_{sym}) by dividing the full voltage or optical power range into four distinct levels, thus requiring three decision thresholds for decoding denoted as L_{d0}, L_{d1}, and L_{d2} in Fig. 2.2 (b). While PAM-4 doubles the data rate for a given symbol rate, it also reduces the spacing between signal levels, demanding better noise performance and linearity. Consequently, PAM-4 offers bandwidth efficiency at the cost of increased design complexity and signal integrity challenges.

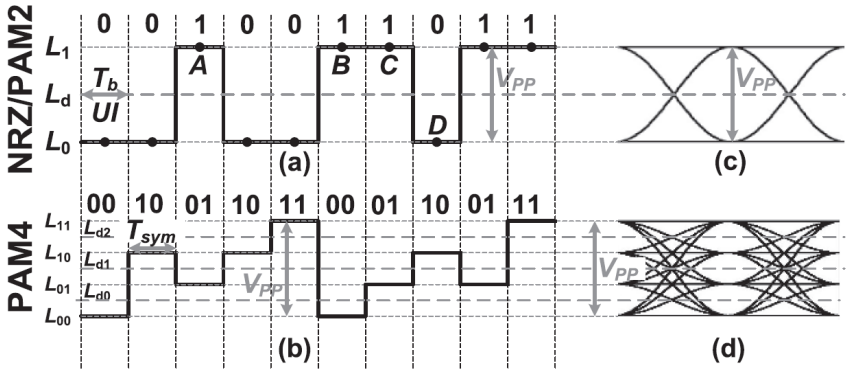


Figure 2.2: Time-domain representations of signals used to encode binary data include: (a) an example of an NRZ (PAM-2), (b) an example of a PAM-4 signal, (c) the eye diagram corresponding to PAM-2, and (d) the eye diagram for PAM-4 [10].

2.2 Eye Diagram

The eye diagram is a widely used technique for evaluating signal quality in wired communication systems. As shown in Fig. 2.3 (a) and (c), segments of the signal shown with different line

styles (typically two UIs long) are extracted and superimposed to create a composite view, resulting in the eye diagram illustrated in Fig. 2.3 (b) and (d) [10]. This visualization provides insight into signal integrity and timing behavior. In the absence of inter-symbol interference (ISI), as in Fig. 2.3 (a) and (b), the sampled values corresponding to logic 1 at the decision point (usually at 1 UI) are tightly clustered around a consistent voltage level, independent of the surrounding bit pattern. In contrast, when ISI is present, as demonstrated in Fig. 2.3 (c) and (d), the amplitude of a logic 1 may vary depending on the previous bits. For instance, a 1 following a sequence of 0s may appear with reduced amplitude compared to a 1 following another 1, indicating distortion and degradation in signal quality.

In Fig. 2.3 (b) and (d), the vertical eye opening (VEO) is defined as the distance between the minimum '1' level (or maximum '0' level) and the decision threshold L_d. This implies that the total distance between the maximum '0' and minimum '1' levels is technically twice the VEO. Although the decision threshold is assumed to lie at the midpoint of the eye in this context, throughout this thesis, we refer to the full distance from the maximum '0' to the minimum '1' level simply as the VEO. As illustrated in Fig. 2.3 (d), significant ISI introduced by the channel or circuit reduces the eye opening.

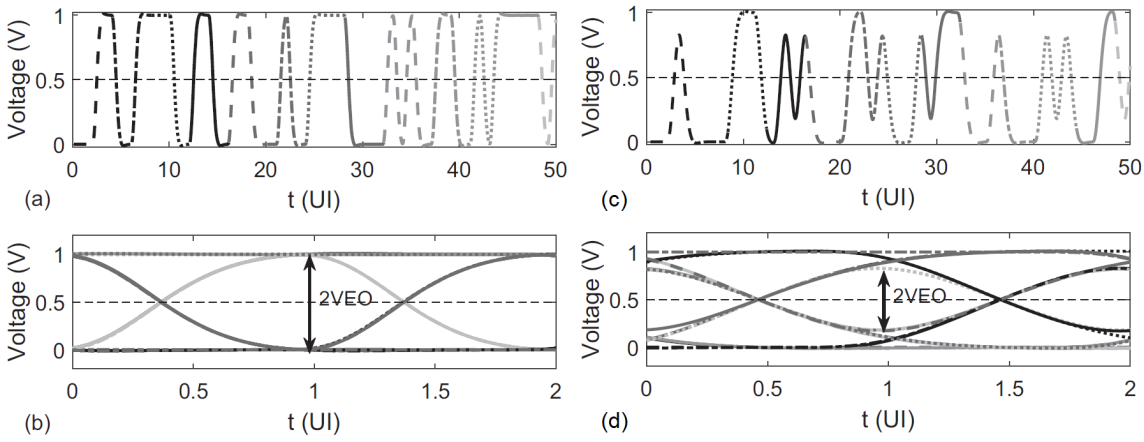


Figure 2.3: Formation of an eye diagram by dividing the signal into segments of two unit intervals long: (a) NRZ signal; (b) resulting eye diagram, indicating minimal inter-symbol interference (ISI); (c) NRZ signal; (d) corresponding eye diagram, showing noticeable ISI effects [10].

2.3 Linearity Metrics in Optical Transceivers

2.3.1 Total Harmonic Distortion (THD)

Nonlinearities in the optical receiver introduce residual ISI that cannot be fully corrected, even with optimized equalization parameters. Linearity is typically characterized by metrics such as total harmonic distortion at specific input amplitudes and frequencies.

If we approximate the input/output characteristic of a memoryless analog circuit by the following polynomial

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots, \tag{2.1}$$

when the value of x is small, the output $y(t)$ can be approximated as

$$y(t) = \alpha_1 x.$$

This approximation suggests that α_1 represents the small-signal gain near $x = 0$. We can assess the nonlinearity of a circuit by introducing a sinusoidal input and analyzing the harmonic components present in the output signal [11]. Substituting $x(t) = A\cos(\omega t)$ in (2.1) yields

$$\begin{aligned} y(t) &= \alpha_1 A\cos(\omega t) + \alpha_2 A^2\cos^2(\omega t) + \alpha_3 A^3\cos^3(\omega t) + \ldots \\ &= \alpha_1 A\cos(\omega t) + \frac{\alpha_2 A^2}{2}[1 + \cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3\cos(\omega t) + \cos(3\omega t)] + \ldots \end{aligned} \tag{2.2}$$

In (2.2), we observe that higher-order terms generate higher harmonics. Specifically, even-order terms produce even harmonics, while odd-order terms generate odd harmonics. The n^{th}-order harmonic distortion (HD_n) is defined as the ratio of the amplitude of the n^{th} component to that of the fundamental.

The linearity of an analog circuit is typically quantified by the square root of the sum of squares for all orders of harmonic distortion [11]. This metric is commonly referred to as "total harmonic

distortion" (THD) and can be defined as

$$\text{THD} = \sqrt{HD_2^2 + HD_3^2 + \dots} \tag{2.3}$$

Reported linear optical receiver designs typically maintain THD below 2.5% for output swings ranging from 400 mV_{pp} to 600 mV_{pp} [5,12]. Some works demonstrate enhanced linearity, achieving THD as low as 1.77% at 500 mV_{pp} [13], while others report up to 5% THD at higher swings [14]. These results suggest a practical target of $<$2.5% THD for high-speed linear receivers operating in this swing range.

2.3.2 Ratio Level Mismatch (RLM)

The bit error rate (BER), defined as the ratio of incorrectly received bits to the total number of transmitted bits, is a critical metric for evaluating the reliability of a communication link. A BER of 10^{-12} is commonly targeted in high-speed systems. However, PAM-4 signaling inherently exhibits a smaller vertical eye opening compared to NRZ, making it more difficult to achieve such low BER values, especially in high-loss channels. Transitioning from a two-level signal (NRZ) to a four-level signal (PAM-4) requires adjustments to both the transmitter and receiver to accommodate the increased signal complexity [10].

In a PAM-4 system, the transmitter must generate four distinct signal levels instead of the two used in NRZ. At the receiver end, the signal must be processed using three decision thresholds to distinguish between these levels, unlike NRZ, which only requires one. Furthermore, the transceiver must maintain a high degree of linearity to accurately interpret the multi-level signal.

A common metric used to evaluate PAM-4 transceiver performance is ratio level mismatch (RLM), which measures how evenly spaced the four signal levels are. In a steady-state condition, where ISI is minimal due to the transmission of enough consecutive identical digits, the signal levels are denoted as V_0 through V_3 (Fig. 2.4) [10]. The midpoint of the signal, V_{mid}, represents the average of the highest and lowest levels

$$V_{\text{mid}} = \frac{V_3 + V_0}{2} \tag{2.4}$$

Based on this midpoint, the relative signal levels for the "01" and "10" symbols, denoted as ES_1 and ES_2, are calculated using the following expressions

$$ES_1 = \frac{V_1 - V_{\text{mid}}}{V_0 - V_{\text{mid}}}, \quad ES_2 = \frac{V_2 - V_{\text{mid}}}{V_3 - V_{\text{mid}}} \tag{2.5}$$

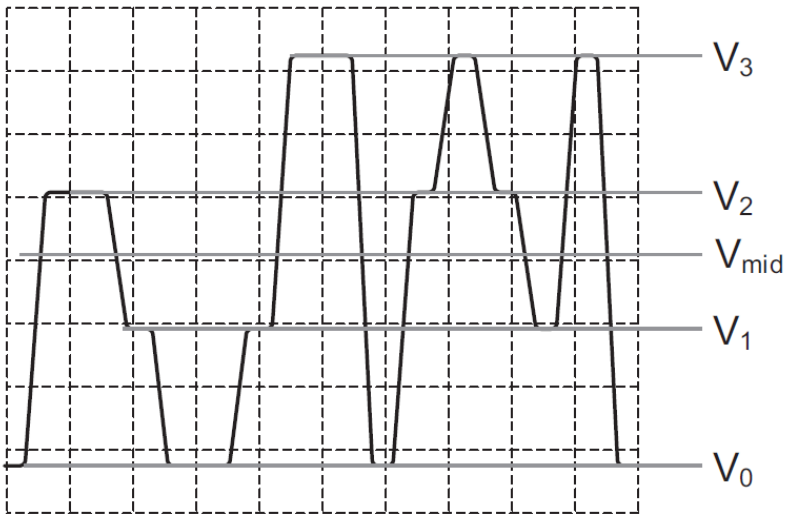


Figure 2.4: Signal level definitions for ratio level mismatch [10].

Ideally, these values should both equal $1/3$ to ensure symmetrical spacing. The RLM value is defined as the minimum of four terms

$$\text{RLM} = \min(3ES_1, 3ES_2, (2 - 3ES_1), (2 - 3ES_2)) \tag{2.6}$$

When the signal levels are perfectly balanced, RLM reaches its ideal value of 1. In practical systems, RLM values above 0.95 are generally considered acceptable. However, while useful, RLM does not account for other critical aspects of signal integrity, such as ISI or timing misalignment between the sub-eyes [10].

2.4 Inverter-based Main Amplifiers

Although inverters are commonly linked to digital circuits, the inverter has proven to be a highly adaptable analog building block for a wide range of applications, as extensively explored in [15,16]. Its class AB operation enables it to achieve an effective compromise between low noise, low power consumption, and broad bandwidth, while still maintaining a satisfactory level of linearity. In the following sections, we will examine one of the most commonly used inverter-based main amplifiers in optical receivers and then explore a suitable alternative for PAM-4 optical receivers.

2.4.1 Cherry-Hooper (CH) Amplifier

The Cherry-Hooper (CH) amplifier based on CMOS inverters consists of two cascaded inverters, shown in Fig. 2.5. A resistive feedback, R_F, is applied around the second stage to enhance the amplifier's bandwidth. In this configuration, the first stage operates as a transconductance stage, converting input voltage to current, while the second inverter together with the feedback resistor realizes a transresistance amplifier. This inverter-based CH topology is extensively utilized across multiple data rates and CMOS process nodes, making it a versatile solution in high-speed analog circuit design [3,17,18].

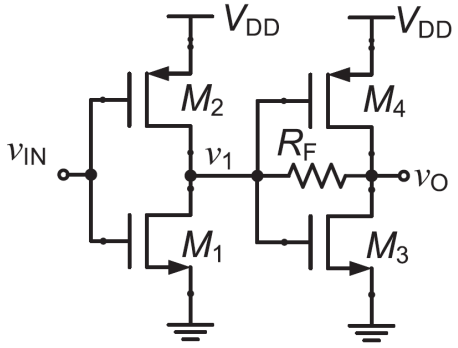


Figure 2.5: Inverter-based Cherry-Hooper amplifier.

The CH amplifier is widely favored in high-speed analog design for its superior bandwidth performance compared to simpler topologies, such as cascaded first-order gain stages. While two cascaded stages typically produce real poles, the CH configuration introduces complex conjugate

poles, resulting in a peaked frequency response that effectively extends the bandwidth. Designers can also adjust the damping factor by tuning circuit parameters such as the transconductance, g_m, feedback resistance, R_F, and parasitic capacitances, offering valuable flexibility in optimizing amplifier performance [10].

Another key advantage of the CH topology is its efficient handling of capacitive loading. The second stage operates as a transresistance amplifier, performing current-to-voltage conversion while presenting a lower equivalent output resistance than a simple resistive load. This reduced output resistance minimizes the RC time constant, contributing to further bandwidth enhancement [10]. However, the CH amplifier lacks the high linearity required for PAM-4 optical receivers, necessitating the use of a more linear gain stage that also maintains high bandwidth.

2.4.2 g_m/g_m Amplifier

When an analog inverter (Fig. 2.6 (a)) is biased at the midpoint between the maximum and minimum power supply voltages, both the n-channel and p-channel transistors operate in the saturation region. In this condition, the inverter has the maximum possible gain and serves as a linear transconductor [16]. The overall transconductance of the block is the result of adding the small-signal transconductance of both NMOS and PMOS transistors. This simple two-transistor circuit has only two nodes, i.e., input and output nodes. Therefore, it removes the concern of additional parasitic poles that might degrade the bandwidth [5]. The efficiency of the analog inverter transconductor in terms of noise, power consumption, and bandwidth, all while maintaining a satisfactory level of linearity performance, has made it a foundational cell that can be applied to accomplish various functions [7, 19, 20]. The output current of the transconductor of Fig. 2.6 (a) can be written as

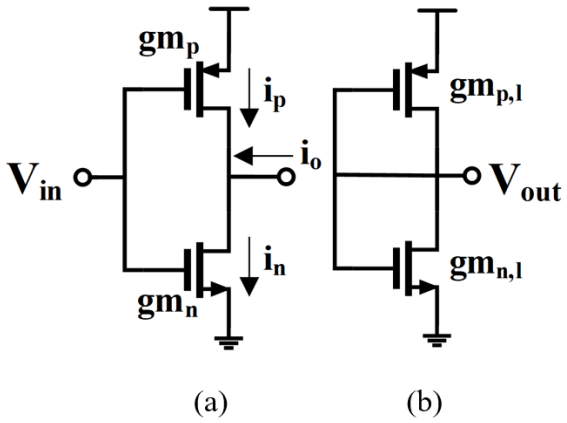


Figure 2.6: Schematic diagram of (a) a transconductor, and (b) diode-connected inverter.

$$i_o = i_n - i_p \approx (k_n V_{\text{ov,n}} + k_p V_{\text{ov,p}}) v_i + \left(\frac{k_n}{2} - \frac{k_p}{2}\right) v_i^2 \tag{2.7}$$

where $k = \mu C_{\text{ox}} \left(\frac{W}{L}\right)$ and $V_{\text{ov}} = V_{\text{GS}} - V_t$. This expression is derived under the square-law assumption of MOSFETs operating in saturation. The current-voltage equation shows that if $k_n = k_p$, the second-order nonlinearity cancels out. In the event of a mismatch, the second-order nonlinearity is only proportionate to $k_n = k_p$. Mobility degradation caused by the transverse electric field and channel length modulation results in the creation of odd-order nonlinearities. These nonlinearities can pose challenges, especially when operating in low-supply voltages [5]. Fig. 2.6 (b) represents a shorted (diode-connected) inverter. [5] demonstrates that an inverter-based transconductor loaded with a diode-connected inverter called a g_m/g_m amplifier (Fig. 2.7), offers much better linearity compared to the CH amplifiers. The reason for calling it a g_m/g_m amplifier is that the total gain of the block in Fig. 2.7 is equal to $G_m/G_{m,L}$ where G_m and $G_{m,L}$ denote the total transconductances of the transconductor and load stages, respectively. A detailed discussion of the higher linearity of the g_m/g_m amplifier can be found in [16]. When NMOS and PMOS transistors have nearly equal threshold voltages, negligible channel length modulation, and operate in saturation, the output voltage of the unity gain g_m/g_m amplifier in Fig. 2.7 can be expressed as [21]

$$V_{\text{out}} = V_{\text{DD}} - V_{\text{in}} \tag{2.8}$$

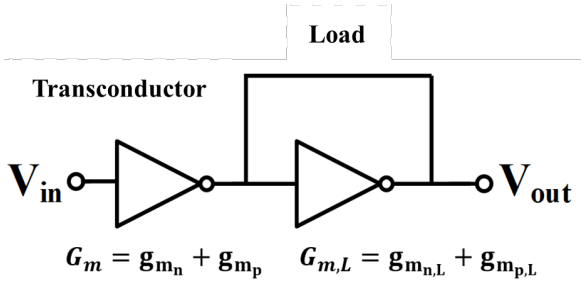


Figure 2.7: Block diagram of the g_m/g_m amplifier.

demonstrating a linear voltage transfer characteristic. Importantly, this linearity holds as long as the nonlinearity of the transistors is predominantly odd-order.

Fig. 2.8 illustrates three different inverter-based pseudo-differential amplifier designs to investigate their linearity according to their loads. The sizes of the inverters are chosen to have a DC gain of 2 in all structures and equal power consumption. Moreover, these amplifiers operate with a 1 V power supply and have the same differential peak-to-peak swing of 600 mV.

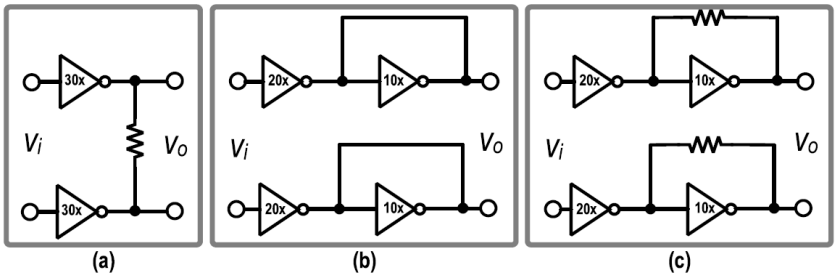
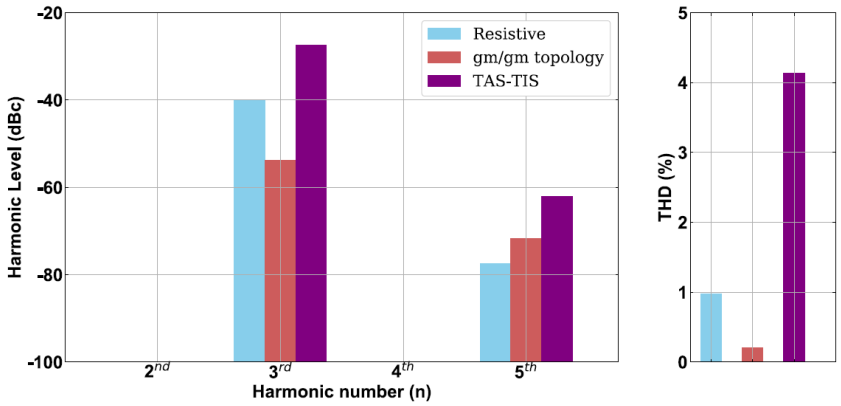


Figure 2.8: Comparison of different amplifier topologies. (a) Resistive load amplifier. (b) g_m/g_m amplifier. (c) TAS-TIS (Cherry-Hooper) amplifier [5].

The load of the transconductor of Fig. 2.8 (a) is an ideal resistor. The second transconductor is loaded with diode-connected inverters, and the third one is the well-known CH amplifier, which is widely used in optical receivers. The linearity of these structures is shown in Fig. 2.9 in terms of harmonic levels and THD. As can be seen, the transconductor with diode-connected inverter loads (g_m/g_m topology) has the best linearity, i.e., the lowest 3rd-order harmonic level and THD. On the other hand, the Cherry-Hooper amplifier represents the worst linearity. Other than high linearity, the superiority of using the diode-connected inverter loads instead of an actual resistor in Fig. 2.8 (a) and (b) is occupying a much smaller area and also eliminating one design parameter, i.e.,

resistance, to have the desired gain, bandwidth, and output impedance [5]. Moreover, the g_m/g_m architecture exhibits better PVT insensitivity, as both transconductances, i.e., G_m and $G_{m,L}$, are typically affected similarly.



(a) (b)

Figure 2.9: Linearity comparison of different amplifier topologies: (a) Harmonic levels, (b) THD [5].

In a pseudo-differential structure (Fig. 2.10), the g_m/g_m amplifiers exhibit common-mode gain, which can degrade performance. To address this issue, cross-coupled inverters are introduced. The use of diode-connected and cross-coupled inverters was first introduced by [6], but was later analyzed in greater depth by [15], particularly in the context of transconductors. Fig. 2.11 illustrates the linear transconductance structure proposed by [15], designed for use in linear, tunable integrators in very high-frequency continuous-time integrated filters. In this configuration, Inv4,5 serve as diode-connected load inverters, while Inv3,6 function as the cross-coupled inverters.

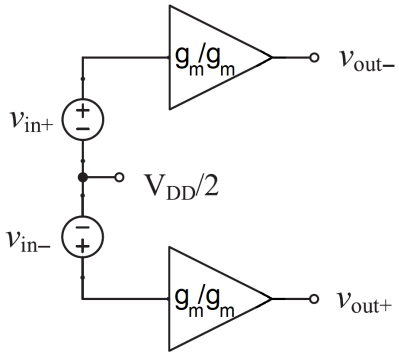


Figure 2.10: g_m/g_m amplifiers in a pseudo-differential structure.

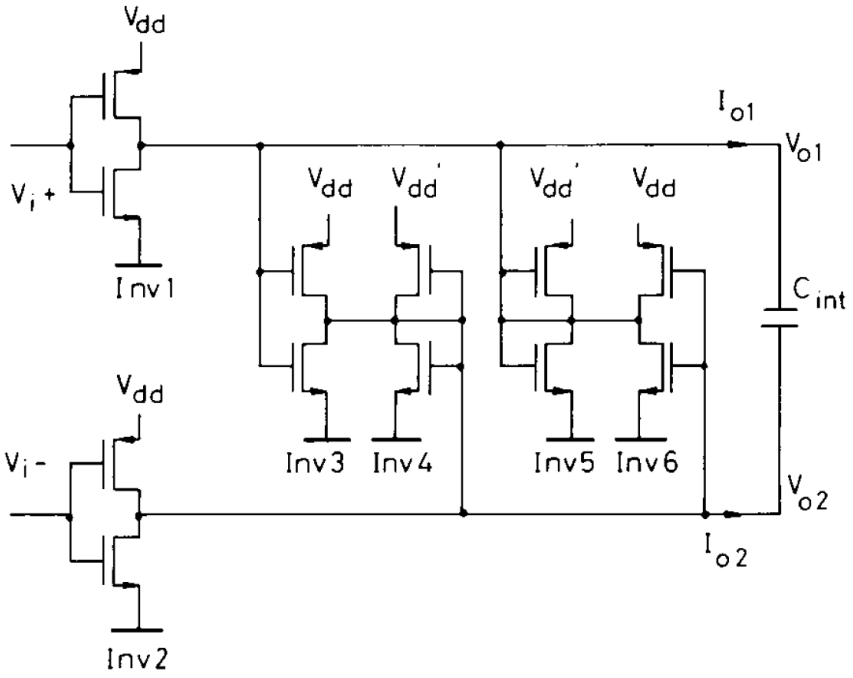


Figure 2.11: Linear transconductance structure proposed in [15].

As shown in Fig. 2.12, [5] proposed a linear optical receiver for 100 Gb/s/λ PAM-4 optical links based on the g_m/g_m amplifier. Similar to Nauta's design, cross-coupled inverters were employed to achieve common-mode rejection and minimize mismatch. Additionally, an inverter-based single-to-differential converter with a diode-connected inverter load was used, offering lower phase offset and group delay compared to configurations with an open inverter load [5].

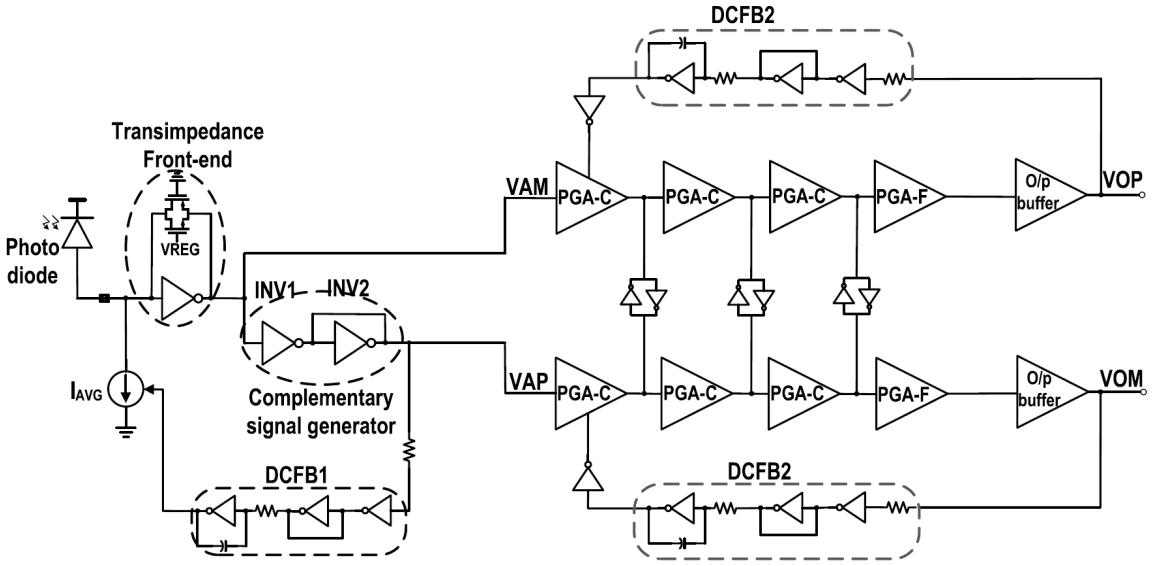


Figure 2.12: Schematic of the proposed linear optical receiver in [5].

The discussed literature demonstrates that the g_m/g_m amplifier can be an excellent candidate for use as a linear main amplifier. However, compared to the CH amplifier, it suffers from limited bandwidth due to the repeated real poles in the cascaded g_m/g_m structure, which compresses the bandwidth more than the complex-conjugate poles of a second-order CH amplifier. Therefore, bandwidth extension techniques must be employed to compensate for this limitation. [5] addressed this by placing an inductor within the feedback loop of the TIA, effectively shielding the input capacitance of the inverter and thereby achieving high bandwidth with minimal in-band peaking. While this method is effective, the use of inductors results in significant chip area consumption, motivating the exploration of inductor-less alternatives.

2.5 Inductorless Bandwidth Extension Techniques

2.5.1 Interleaving Active Feedback (IAFB)

Incorporating negative feedback into the MA circuitry enhances both linearity and bandwidth. This section examines how active negative feedback can be leveraged for bandwidth extension. By applying this technique, it is possible to achieve high bandwidth without the use of inductors.

In a cascade of amplifiers used in the MA circuit, the total bandwidth can be written as [22]

$$BW_{\text{tot}} = BW_{\text{cell}} \cdot \sqrt[2m]{\sqrt[n]{2} - 1} \tag{2.9}$$

where n is the number of cascaded stages with m^{th}-order Butterworth frequency response, and BW_{cell} is the bandwidth of a unit amplifier cell. Moreover, if A_{tot} is defined as the total gain of the MA circuit, the gain-bandwidth product of the unit gain cell will be equal to [23]

$$GBW_{\text{cell}} = \frac{BW_{\text{tot}}}{\sqrt[2m]{\sqrt[n]{2} - 1}} \cdot \sqrt[n]{A_{\text{tot}}} \tag{2.10}$$

Fig. 2.13 shows the required gain-bandwidth product of a unit amplifier cell within the MA circuit for $m = 1, 2,$ and 3 when $A_{\text{tot}} = 40\,\text{dB}$ and $BW_{\text{tot}} = 10\,\text{GHz}$. Given this plot, the larger n, the less the required gain-bandwidth product of a unit cell. However, by increasing the number of identical cascaded stages, the descending trend of the required GBW_{cell} does not continue and starts to saturate. It should be noted that by having a large n, the MA's power consumption increases, and the MA's input-referred noise degrades due to the reduced gain per unit gain cell [8]. Therefore, it is important to choose an optimal value for n, typically 4 or 5.

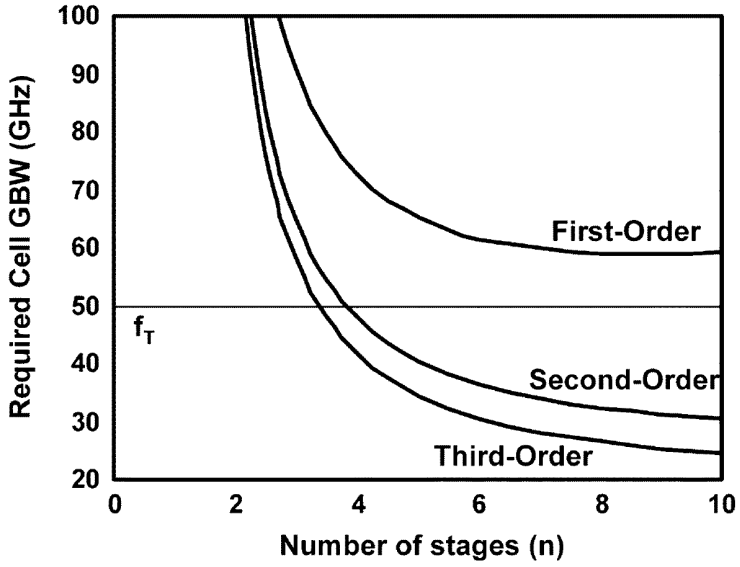


Figure 2.13: The relationship between the GBW product and the number of stages for $A_{\text{tot}} = 40\,\text{dB}$ and $BW_{\text{tot}} = 10\,\text{GHz}$ [8].

Another conclusion that can be extracted from Fig. 2.13 is that reaching the required gain-bandwidth product using first-order amplifier cells within the MA circuit is not practical in a standard 180 nm CMOS technology, which has an f_T of 50 GHz [8]. However, in the cascading of four second- and third-order 10 dB gain stages, the required GBW_{cell} is 49 and 41 GHz, respectively. Based on the transition frequency of the technology, without using the inductive peaking technique, the required specifications cannot be met even by employing second-order gain stages [22]. The IAFB bandwidth extension technique is investigated for the cascade of third-order amplifier cells.

Fig. 2.14 shows the block diagram and circuit schematic of a conventional third-order amplifier, which includes active feedback. If each first-order gain cell and active feedback cell is characterized by the transfer functions of

$$G_{1-3}(s) = \frac{G_m R}{1 + sRC}, \quad G_f(s) = \frac{G_{mf} R}{1 + sRC} \tag{2.11}$$

respectively, then the overall transfer function of the third-order system can be written as [8]

$$H_{3\text{rd}}(s) = \frac{G_1(s) \cdot G_2(s) \cdot G_3(s)}{1 + G_1(s) \cdot G_2(s) \cdot G_f(s)} = \frac{G_m^3 R^3}{(1 + sRC)^3 + G_m^2 G_{mf} R^3} \tag{2.12}$$

where G_m and G_{mf} denote the transconductance of each differential pair, and R and C are the resistive and capacitive loads per stage.

If $\omega_0 = \frac{1}{RC}$, $A_0 = G_m R$, and $\beta = G_{mf} R$, equation 2.12 can be simplified to [8]

$$H_{3\text{rd}}(s) = \frac{A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3 + A_0^2 \beta} \tag{2.13}$$

which has one non-dominant real pole and two dominant conjugate poles.

Fig. 2.15 (a) shows the trend of gain-bandwidth characteristics as a function of the feedback gain β with $A_0 = 2.5$. Obviously, by increasing β, the normalized -3 dB bandwidth increases, but it leads to reduced gain. Fig. 2.15 (b) is illustrated to investigate the gain flatness of this third-order system. According to this plot, as β increases, gain peaking increases as well. Hence, while applying active feedback to third-order gain stages can improve the bandwidth, it cannot be considered a useful technique for extending bandwidth because it causes a noticeable increase in

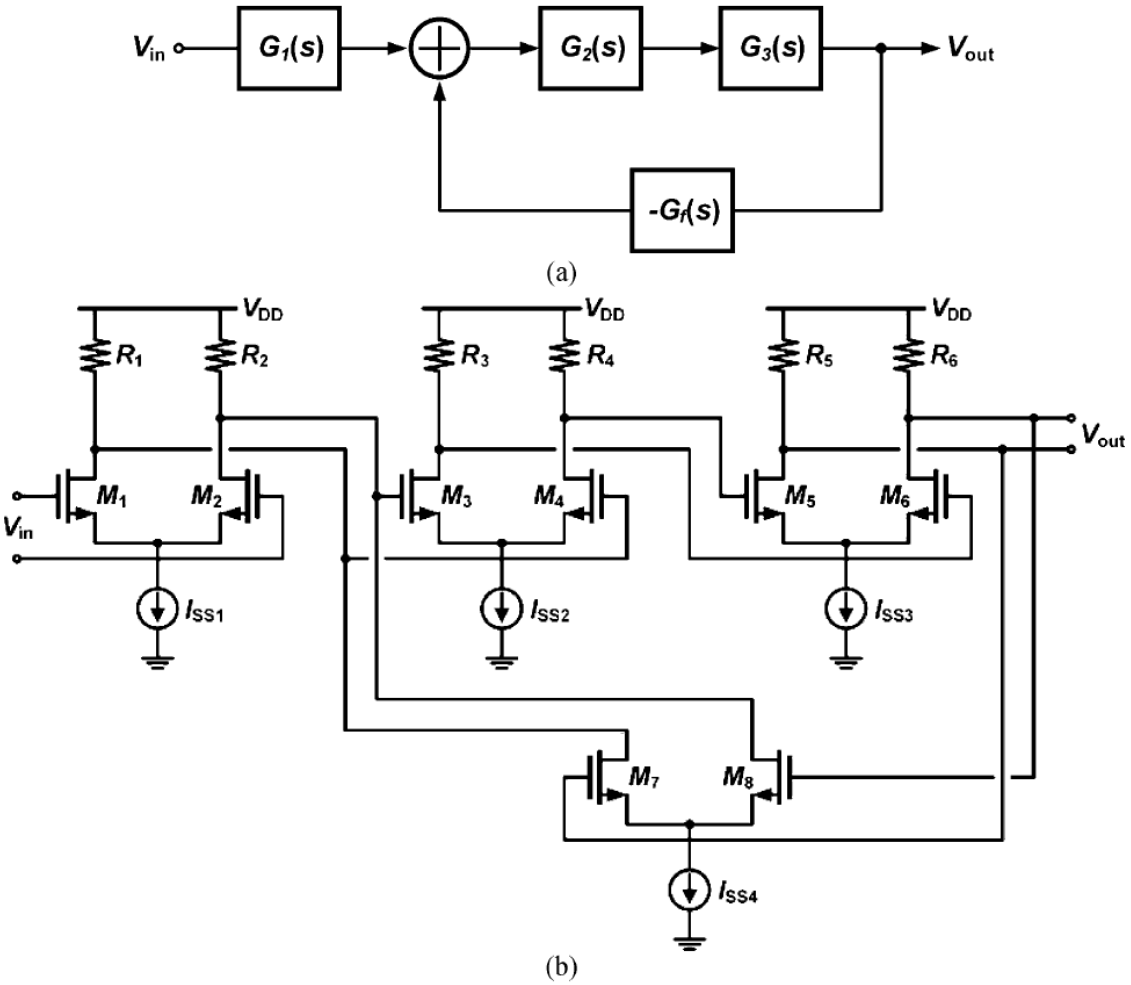
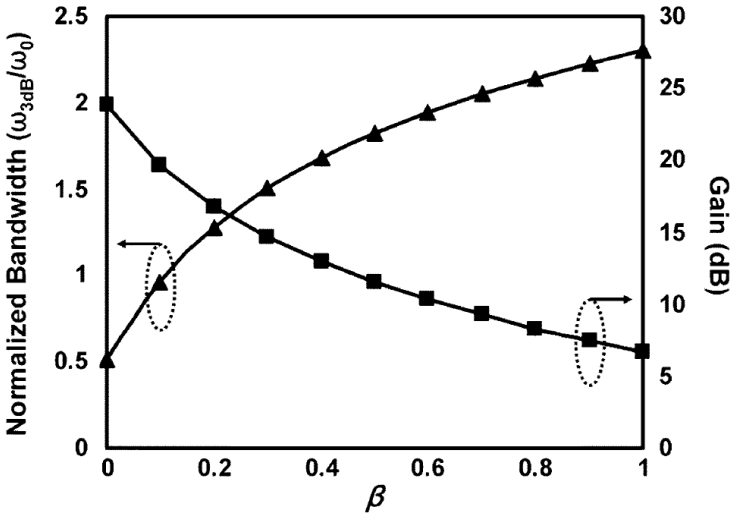
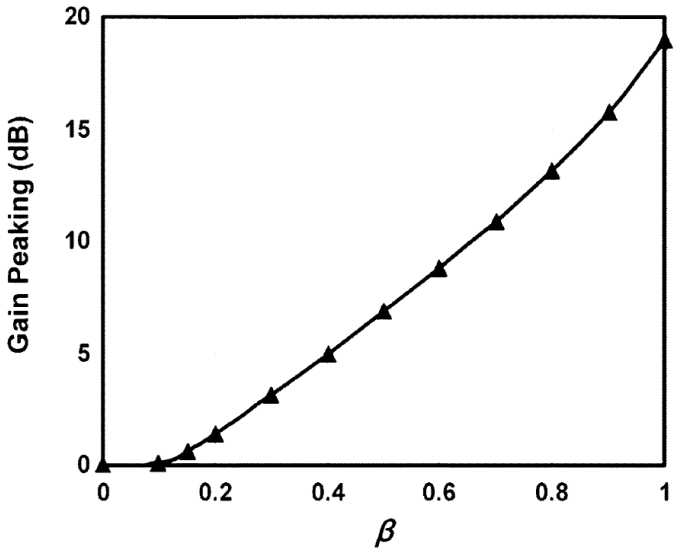


Figure 2.14: (a) Block diagram and (b) circuit schematic of conventional third-order gain stages with active feedback [8].

the associated gain peaking [8].



(a)



(b)

Figure 2.15: Variations of (a) gain and normalized bandwidth, and (b) gain peaking of the conventional third-order amplifier by increasing the feedback gain β [8].

A practical technique to enhance the bandwidth while maintaining gain flatness is to apply IAFB to the system. Fig. 2.16 illustrates the cascaded third-order stages with interleaving active feedback.

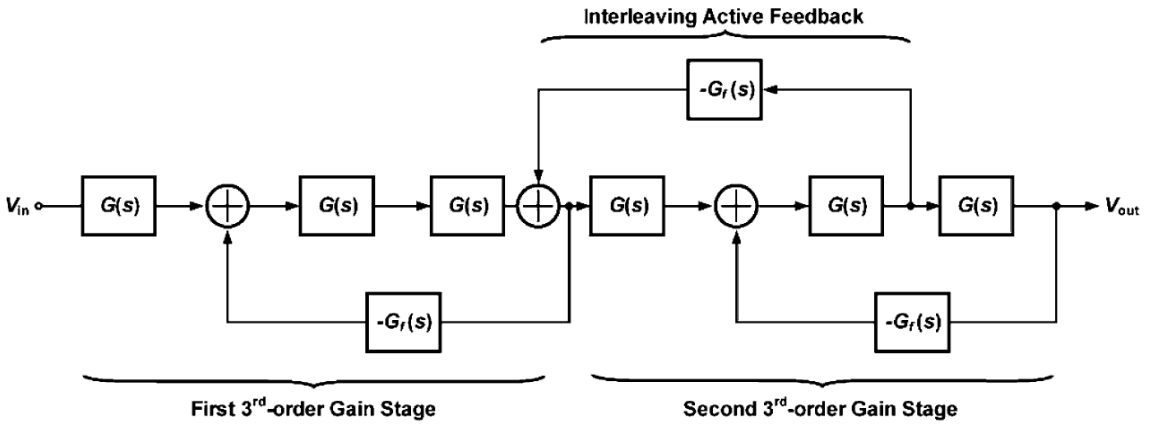


Figure 2.16: Block diagram of the cascaded third-order stages with the proposed interleaving feedback in [8].

The transfer function of the system is given by [8]

$$H(s) = \frac{G^6(s)}{1 + 3G^2(s)G_f(s) + G^4(s)G_f^2(s)} \tag{2.14}$$

which can be written as two third-order transfer functions with different feedback gains as follows

$$H(s) = H_A(s) \cdot H_B(s) = \frac{G_3(s)}{1 + 2.62\,G_2(s)G_f(s)} \cdot \frac{G_3(s)}{1 + 0.38\,G_2(s)G_f(s)} \tag{2.15}$$

In 2.15, $H_A(s)$ and $H_B(s)$ represent two conventional third-order systems similar to Fig. 2.14 (a), but with dissimilar feedback gains of -2.62 and -0.38, respectively. With different feedback gains, now each $H_A(s)$ and $H_B(s)$ has three poles with different locations than 2.12. In other words, pole splitting occurs, as shown in Fig. 2.17.

Fig. 2.18 (a) shows that with $\beta = 0.3$, $H_A(s)$ and $H_B(s)$ represent a relatively large gain peaking. However, cascading these two third-order stages leads to a considerable improvement in gain flatness. Moreover, the frequency response of the cascaded third-order gain stages with and without IAFB is illustrated in Fig. 2.18 (b). Given this plot, both bandwidth and gain flatness are noticeably improved.

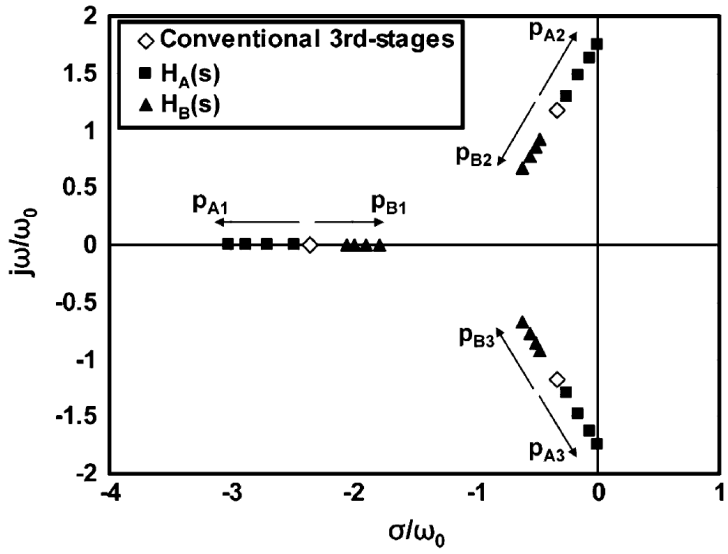


Figure 2.17: Pole splitting behavior of the proposed feedback technique in [8].

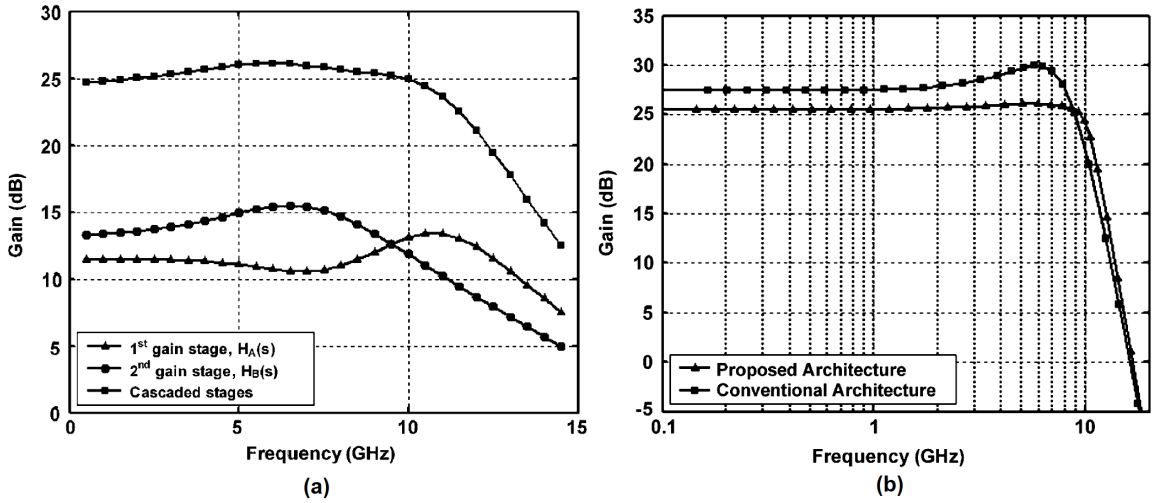


Figure 2.18: (a) Simulated frequency response of the cascaded architecture with nonuniform third-order gain stages; (b) Simulated frequency response of the cascaded third-order gain stages [8].

2.6 Equalizing the Electrical Channel in Optical Receivers

Fig. 2.19 (a) illustrates the block diagram of an optical receiver system. Following the main amplifier stage, the signal passes through an electrical channel, which may represent a PCB trace or a coaxial cable in an electrical link. As the data rate increases, the pulse response of the channel begins to exhibit significant ISI, a common issue in high-speed electrical link standards [10].

Receiver-side equalization is essential in modern high-speed data transmission systems to compensate for signal degradations caused by the transmission channel, particularly in systems using copper interconnects [24]. Without equalization, these impairments can lead to significant signal distortion, resulting in eye closure and increased BER, thereby degrading overall system performance and reliability. To address this, a continuous-time linear equalizer (CTLE) is typically employed after the channel.

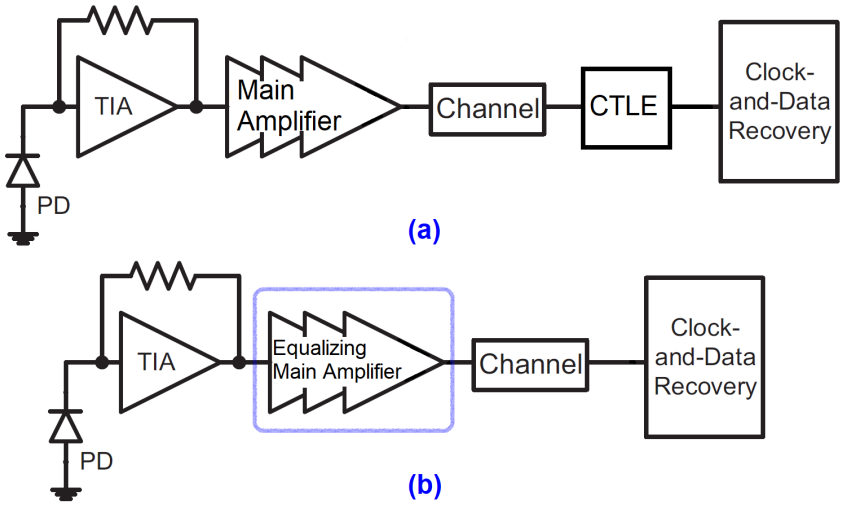


Figure 2.19: Block diagram of an optical receiver link: (a) employing a CTLE stage for equalization, and (b) utilizing an equalizing main amplifier to compensate for channel losses.

As illustrated in Fig. 2.20, the CTLE compensates for the channel's frequency-dependent losses by approximating the inverse of the channel's frequency response, thereby flattening the overall response up to the Nyquist frequency (i.e., $f_{bit/2}$). This frequency shaping enhances the high-frequency components of the received signal, which are increasingly attenuated as data rates rise, leading to ISI and degraded signal integrity. Due to practical design tradeoffs, the CTLE provides only partial equalization, with the remaining compensation typically handled by a decision feedback equalizer (DFE) [24].

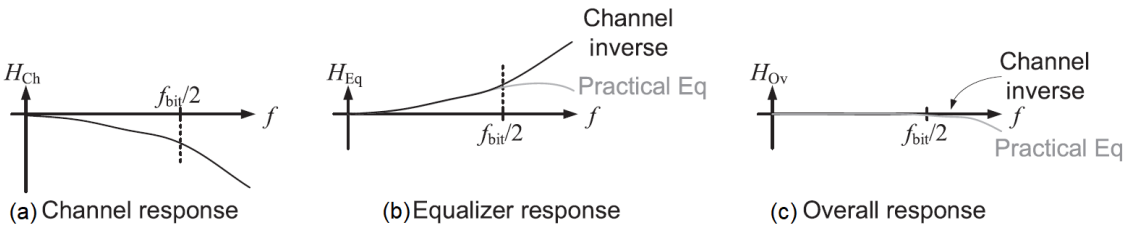


Figure 2.20: Equalization as channel inversion: (a) frequency response of the channel; (b) frequency response of an equalizer; (c) overall frequency response [10].

The CTLE achieves its frequency-shaping characteristics by introducing a zero and a pole in its transfer function, typically implemented through resistive and capacitive degeneration in a differential amplifier [24]. The placement of these frequencies governs the equalizer's ability to provide gain at higher frequencies while preserving unity gain at low frequencies. The eye diagram at the CTLE output is then analyzed to ensure signal clarity, and a programmable boost factor is introduced to fine-tune the high-frequency gain [24]. Since a single stage offers limited boosting, multiple CTLE stages may be cascaded, but at the cost of increased power consumption and potential bandwidth reduction. To address these limitations, inductive peaking is often employed to extend bandwidth without significantly increasing power usage [25]. This technique enhances high-frequency performance by mitigating the effects of parasitic capacitances, albeit at the expense of a larger chip area due to the use of passive inductors.

In the following, we explore an approach that integrates equalization directly into the main amplifier without introducing additional circuitry or passive elements in the optical receiver, thereby reducing power consumption and chip area.

2.6.1 Equalizing Main Amplifier (EMA)

A beneficial approach in high-speed optical receivers is to incorporate high-frequency peaking (HFP) in the MA to extend bandwidth. Properly tuned HFP, particularly near the Nyquist frequency, helps compensate for bandwidth limitations caused by other components in the optical link, thereby improving signal integrity. These bandwidth constraints often arise due to parasitic capacitances, packaging effects, and the limited gain-bandwidth product of active devices. By boosting the high-frequency components of the signal, HFP ensures signal integrity and maintains the overall link

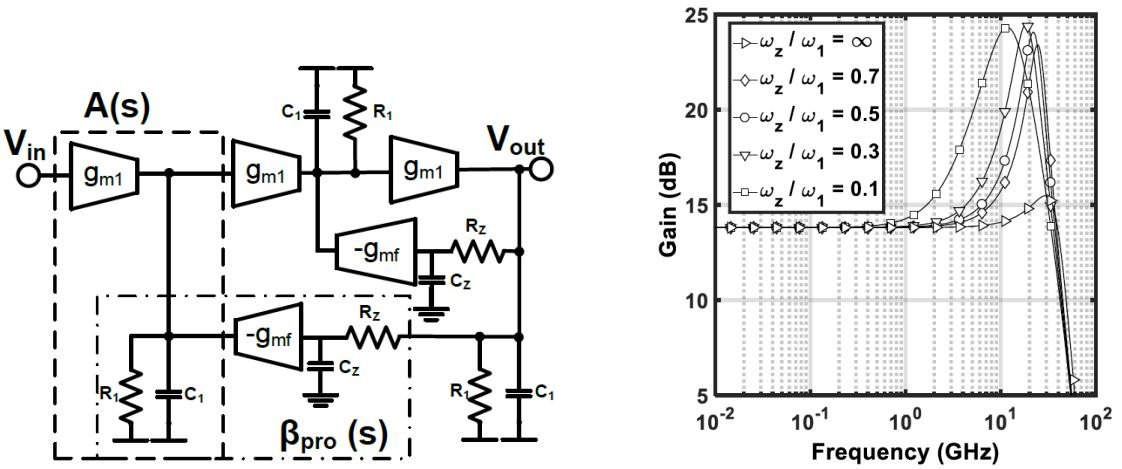
performance.

A traditional method for achieving HFP, as described in [26], involves using passive inductors in both shunt and series configurations between stages of a programmable gain amplifier. This technique compensates for performance variations in multi-mode fibers and extends bandwidth. However, passive inductors occupy large silicon areas, complicate integration, and may introduce substrate coupling issues, making them less desirable for compact and power-efficient designs.

To overcome these challenges, [27] proposes an active feedback-based MA design that introduces a carefully placed pole in the feedback loop. Rather than extending the MA's intrinsic bandwidth, this approach compensates for the limited bandwidth of the preceding TIA, thereby enhancing the overall frequency response of the receiver front-end. By eliminating the need for passive inductors, it reduces chip area and avoids substrate coupling issues. The feedback pole is strategically placed to provide gain peaking in the desired frequency range, ensuring sufficient signal amplification at high frequencies.

Integrating HFP within the main amplifier stage itself allows the MA to perform the role of a CTLE. As illustrated in Fig. 2.19 (b), this integration simplifies the receiver front-end architecture by removing the need for a separate CTLE block. The result is a more compact design with lower power consumption, which is critical for high-speed optical communication systems where energy efficiency is a primary concern. Additionally, the equalizing main amplifier (EMA) contributes to improved signal-to-noise ratio (SNR) and jitter tolerance. Compensating for high-frequency losses ensures cleaner eye diagrams and more reliable data recovery at the clock and data recovery (CDR) unit.

Figure 2.21 (a) presents the block diagram of the third-order nested feedback gain stage using the HFP technique proposed in [27]. The first-order gain cell, $A(s)$, is represented by the transconductance of the input device g_{m1}, load resistance R_1, and load capacitance C_1. The adjustable active feedback cell, $\beta_{\text{pro}}(s)$, is modeled by the transconductance $-g_{mf}$.



(a) (b)

Figure 2.21: Block diagram of (a) the third-order EMA in [27] with a LPF inserted in each feedback path (b) amplitude response of the EMA for various ratios of ω_Z/ω_1 .

In this design, two poles are introduced in the feedback loops using R_Z resistors to create an adjustable HFP while maintaining the low-frequency gain. The transfer function of the third-order nested feedback block is described in 2.16, where $A_1 = g_{m1}R_1$ and $\omega_1 = (R_1C_1)^{-1}$ represent the DC gain and cutoff frequency of the first-order gain cell, respectively. The DC feedback gain is given by $\beta_1 = g_m f R_1$, and $\omega_Z = (R_Z C_Z)^{-1}$ is the cutoff frequency of the low-pass filter introduced, which is assumed to have minimal loading on the output node.

$$H_{EMA}(s) = \frac{A_1^3\left(\frac{s}{\omega_Z}+1\right)}{\left(\frac{s}{\omega_1}+1\right)^3\left(\frac{s}{\omega_Z}+1\right) + A_1\beta_1\left(\frac{s}{\omega_1}+1\right) + A_1^2\beta_1} \tag{2.16}$$

The effect of varying ω_Z on the amplitude response of the proposed EMA is shown in Fig. 2.21 (b). For a fixed β_1, HFP can be introduced independently of the low-frequency gain. As ω_Z decreases, the peak of the amplitude response shifts to a lower frequency.

This approach integrates the equalization functionality into the gain stage, enabling the circuit to maintain the performance advantages of conventional equalizer-based designs while enhancing energy efficiency by eliminating the need for a separate equalizer stage.

2.7 Conclusion

In this chapter, we focused on inverter-based main amplifiers for optical receivers. According to linearity metrics such as THD, the g_m/g_m structure exhibits superior linearity compared to the widely used CH amplifier. However, the CH topology provides a wider bandwidth. To overcome this limitation, we investigated an inductorless bandwidth extension technique for the g_m/g_m amplifier, aiming to avoid the additional chip area associated with inductors. Lastly, to enhance the eye diagram and mitigate ISI, two receiver-side equalization strategies were explored: incorporating CTLE stages and implementing HFP within the analog front end. Among these, equalizing the main amplifier through HFP proved to be a promising solution for linear-drive systems, as it effectively compensates for channel losses without adding additional CTLE stages or increasing power consumption in the receiver front end.

Chapter 3

Linear Main Amplifier

The preceding sections have reviewed the fundamental concepts of high-speed, linear optical receiver design, covering existing linearization techniques, bandwidth enhancement methods, and equalization approaches reported in the literature. From this chapter onward, we present the proposed receiver architecture and the associated design techniques, which form the original contributions of this thesis.

In this chapter, we propose a highly linear PAM-4 optical receiver based on the g_m/g_m topology, implemented in 65 nm CMOS technology. The interleaving active feedback (IAFB) technique [8] enhances bandwidth without relying on passive inductors. By combining g_m/g_m main amplifiers with the IAFB technique, the proposed receiver achieves a data rate of 50 Gb/s (25 GBaud/s) while maintaining a total harmonic distortion (THD) of less than 2% at a 500 mV_{pp} output swing. To further improve linearity, resistive voltage dividers are incorporated into the feedback loops, reducing THD to below 0.6% at the same output swing.

3.1 g_m/g_m-based Main Amplifier Design

3.1.1 Bandwidth Extension Technique

Implementing negative feedback can improve both the bandwidth and linearity of a circuit. The poles can be shifted to higher values, and the pole quality factor (Q) can be improved by introducing negative feedback, thus extending the bandwidth [8]. As nonlinearity can be perceived

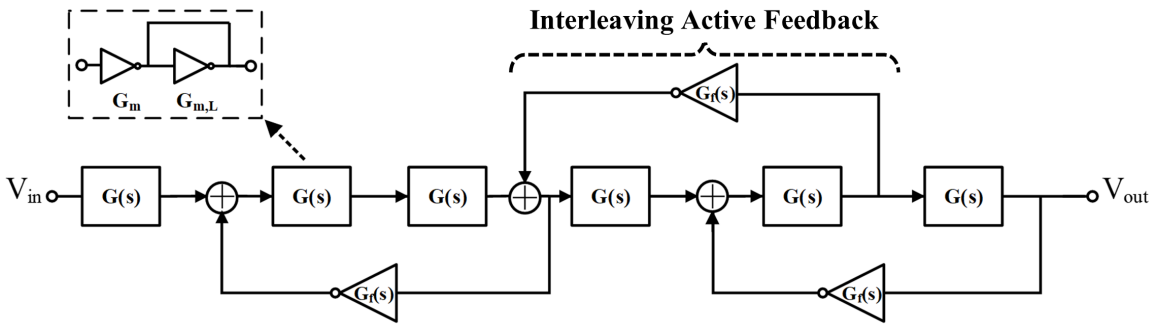


Figure 3.1: Block diagram of the proposed PAM-4 linear main amplifier using g_m/g_m-based amplifiers and IAFB technique.

as fluctuations in the small-signal gain with the input level, negative feedback is also anticipated to suppress such variations, resulting in improved linearity for the closed-loop system [11]. [8] introduces the IAFB technique to enhance the bandwidth of the cascaded third-order amplifier cells through the pole-splitting phenomenon. While negative active feedback can improve bandwidth, it can increase gain peaking [8]. Nevertheless, the IAFB technique can increase bandwidth with reasonable gain flatness through a combination of low and high Q pole pairs.

Fig. 3.1 shows the proposed linear main amplifier based on the g_m/g_m topology and the IAFB technique. This configuration comprises six stages of inverter-based transconductors, known for their high linearity, loaded by diode-connected inverters, and employs IAFB to boost bandwidth. Notably, this design exhibits considerably superior linearity compared to a six-stage cascade of Cherry-Hooper (CH) amplifiers with equivalent input voltage and gain. Furthermore, the IAFB approach has led to a broader bandwidth when compared to its CH amplifier-based counterpart. The subsequent section delves into the design methodology and simulation results of the proposed linear main amplifier and offers a comparison with the widely employed CH amplifier.

3.2 Design Methodology and Simulation Results

3.2.1 PMOS to NMOS Ratio

The proposed linear main amplifier is designed in 65 nm CMOS technology. It operates with a 1 V supply voltage. Let us first consider Fig. 3.1 without any feedback. In the open-loop design,

each g_m/g_m cell is designed to have a gain of 2. In advanced technology like 16 nm FinFet, the n-channel and p-channel transistors have identical mobility and threshold voltage. Moreover, the g_m of the transistors is about 10 times larger than g_{ds}, which makes it possible to ignore channel length modulation [21]. Hence, if the size of the load inverter in Fig. 2.7 is reduced to half that of the transconductor, achieving a gain of 2 is straightforward. However, in 65 nm CMOS technology, the mobility of the NMOS and PMOS transistors is not the same, and g_{ds} must be considered in the calculations.

Based on our simulations, the g_m/g_m amplifier has the highest linearity when the PMOS transistor's width is 2.5 times larger than NMOS's. Therefore, considering this ratio and channel length modulation, in the open-loop design, the width of NMOS in the transconductor and load inverters is 10 μm and 2.7 μm, respectively. The PMOS transistors are 2.5 times larger than their corresponding NMOS transistors. Using these dimensions, each g_m/g_m amplifier in Fig. 3.1 has a gain of 2, giving a total gain of 64 for the six cascaded g_m/g_m amplifiers.

3.2.2 Gain Selection

The next step is to add the negative active feedback loops and the IAFB to the circuit, which all consist of single inverters. To have a reasonable comparison, using the transfer function of (2.14), the total gain of the proposed circuit is kept at 64 by increasing the gain of each g_m/g_m cell.

As previously mentioned, negative active feedback causes gain peaking, and IAFB reduces it. Fig. 3.2 shows the frequency response of the proposed design with different combinations of gains for the forward blocks ($G(s)$) and feedback inverters ($G_f(s)$) to have a total gain of 64. It can be seen that increasing the gain of the feedback inverters increases both bandwidth and gain peaking. The amount of gain peaking for the different combinations of $G(0)$ and $G_f(0)$ is demonstrated in Fig. 3.2.

IAFB can result in significant pole-splitting if the loop gain becomes excessively large. This pole-splitting can lead to a situation where a pair of conjugate poles shifts into the right half-plane, making the system unstable. Fig. 3.3 illustrates the pole locations of the proposed main amplifier for different combinations of $G(s)$ and $G_f(s)$ DC gains to have a total gain of 64. This plot shows that the far-right pair of conjugate poles moves toward the right half-plane by increasing the feedback

gain and the forward gain. To ensure a stable system, the poles of the transfer function of (2.14) must have negative real parts. Therefore, we must be careful in choosing the design point to avoid instability and unbounded dynamic response.

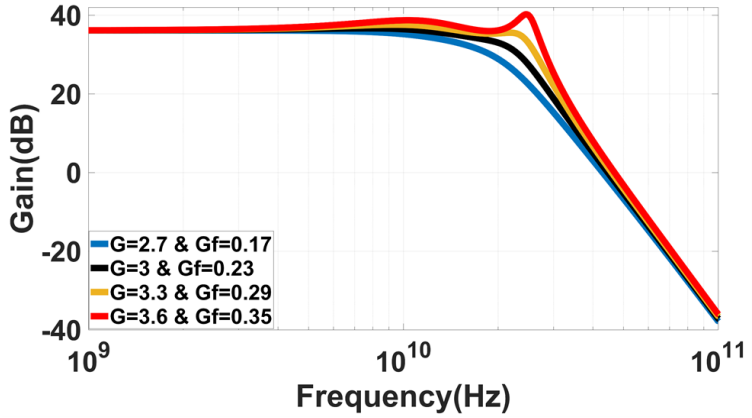


Figure 3.2: Gain peaking for different combinations of $G(0)$ and $G_f(0)$ to have a total gain of 64.

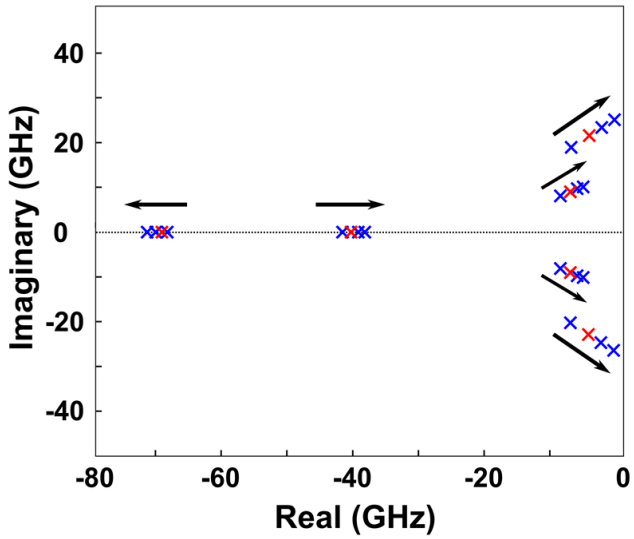


Figure 3.3: Pole location variations of the proposed design for different combinations of $G(s)$ and $G_f(s)$ to have a total gain of 64. The red markers represent the pole locations of the design with $G(0)$=3 and $G_f(0)$=0.23.

Fig. 3.4 shows how vertical eye-opening (VEO) changes in different combinations of $G(0)$ and $G_f(0)$. The largest VEO happens at $G(0)$=3.3 and $G_f(0)$=0.29, but as $G(0)$ and $G_f(0)$ increase, the jitter of the eye diagram gets larger. Based on these trade-offs, the forward and feedback gains are set to $G(0) = 3$ and $G_f(0) = 0.23$, resulting in NMOS transistor widths of 1.28 μm and 723 nm for

the transconductor and diode-connected inverters, respectively. To compare the frequency response of the g_m/g_m-based design with and without feedback and the CH-based design, Fig. 3.5 is plotted. It is evident that the feedback has significantly improved the bandwidth of the g_m/g_m circuit. The ratio of 2.5 between PMOS and NMOS transistor widths is kept in all three configurations, and each CH stage is designed to have a gain of 2. At the same total gain of 64 (36 dB), the g_m/g_m-based circuit with three negative active feedback has the widest bandwidth.

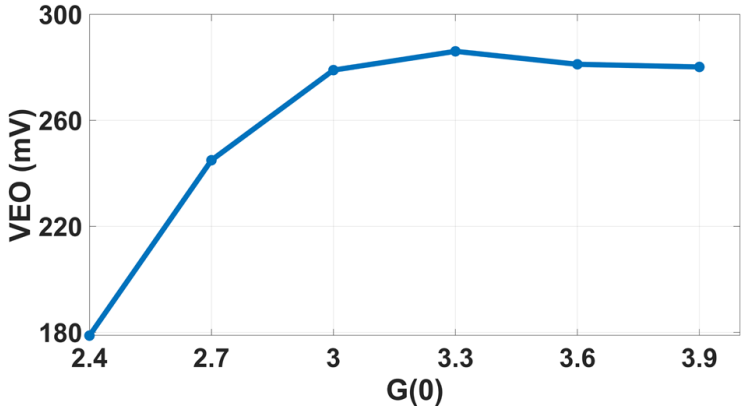


Figure 3.4: VEO variations of the six-stage g_m/g_m design with IAFB in different combinations of $G(0)$ and $G_f(0)$.

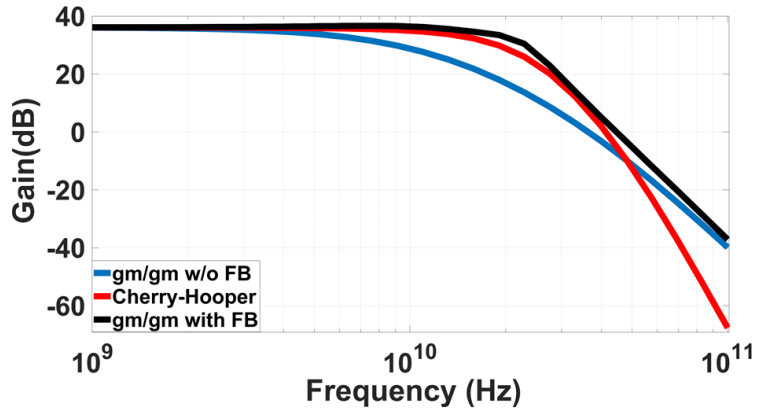


Figure 3.5: Frequency response of the six-stage g_m/g_m-based design with and without IAFB at $G(0)$=3 and $G_f(0)$=0.23, and six-stage CH-based amplifier.

To investigate the linearity of the g_m/g_m-based design with and without feedback and the CH amplifier, the THD of these topologies is plotted in Fig. 3.6 for a range of input voltage. The CH amplifier has the worst linearity (highest THD) in the entire range of the input voltage. The linearity

of the open-loop g_m/g_m amplifier is the best in small input voltage amplitudes while adding feedback improves linearity at higher voltages. Linear feedback usually improves linearity. However, when applied to inverter-based designs, the feedback network, built from the same circuit elements as the forward gain path, introduces nonlinearity. Specifically, the feedback inverter whose input is connected to the overall output sees a very large input signal, exceeding its linear range. Its distortion cannot be easily eliminated, explaining why the IAFB design does not exhibit better linearity across all input voltages compared to the open-loop design. We also designed and simulated the fully differential configuration of the proposed design and expected to see a noticeable decrease in the THD due to the elimination of the even-order harmonics. However, the amount of the THD reduction was insignificant.

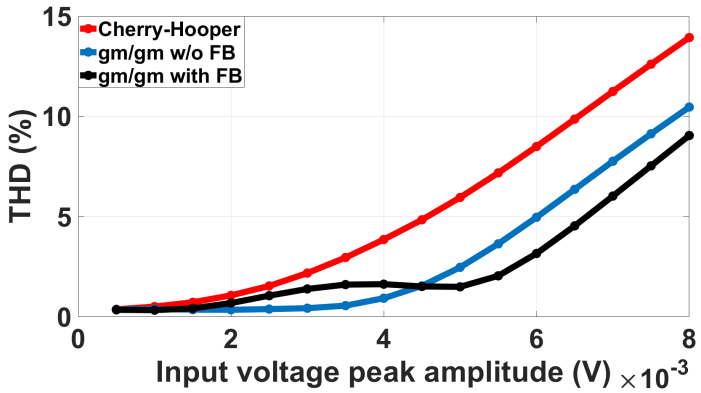


Figure 3.6: THD of the six-stage g_m/g_m-based design with and without IAFB at $G(0)$=3 and $G_f(0)$=0.23, and six-stage CH-based main amplifier.

A pseudo-random bit source (PRBS) is given to a conventional shunt-feedback TIA input (shown in Fig. 3.7), and the output of the TIA is connected to the proposed main amplifier. Among various TIA circuit topologies, the shunt-feedback TIA is the most widely used due to its superior gain and noise performance [28]. Fig. 3.8 (a) displays the eye diagram of the circuit in the NRZ signaling scheme at $G(0)$=3 and $G_f(0)$=0.23, and Fig. 3.8 (b) represents it in PAM-4 format with a unit interval (UI) of 40 ps. The circuit configuration remains unchanged between the two signaling formats. Fig. 3.9 (a) and (b) demonstrates the NRZ and PAM-4 eye diagrams for CH-based topology, respectively. Apart from the higher bandwidth and better linearity than the CH-based design, the proposed design also represents a larger VEO.

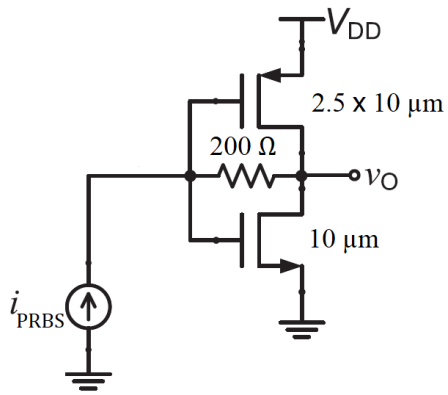


Figure 3.7: Schematic of the shunt-feedback TIA used in the optical receiver.

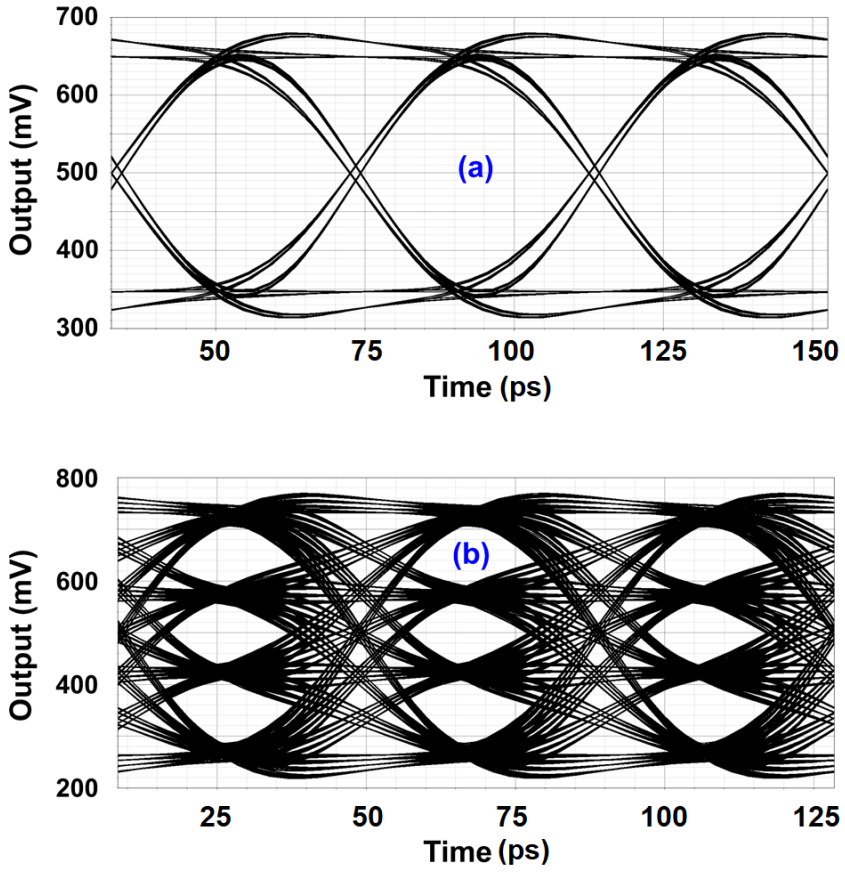


Figure 3.8: The eye diagrams of the proposed design in a) NRZ, b) PAM-4 at $G(0)$=3 and $G_f(0)$=0.23 with 40 ps of UI.

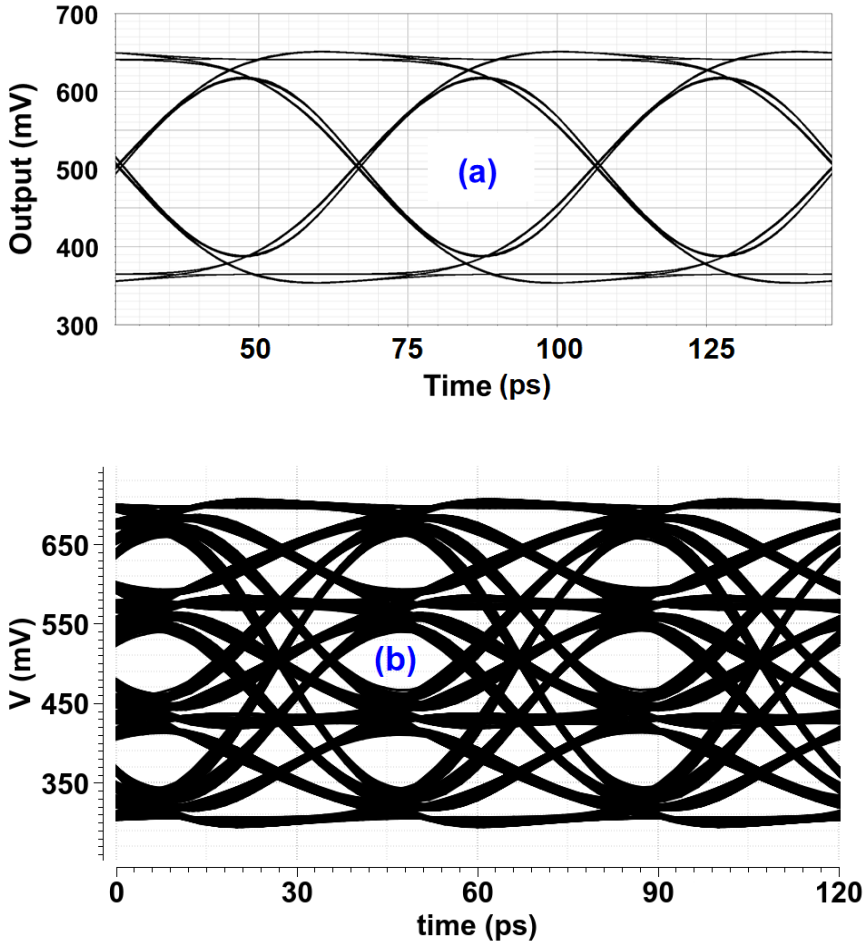


Figure 3.9: The eye diagrams of the CH-based design in a) NRZ, b) PAM-4 with 40 ps of UI.

3.3 Linearity Improvement

In Fig. 3.6, it was noted that the linearity of the open-loop six-stage g_m/g_m amplifier performed best at lower input voltage amplitudes, while the addition of feedback improved linearity at higher voltages. The degraded linearity of the proposed design at smaller input voltages is mainly due to the feedback inverter receiving a large signal from the overall output, causing it to operate outside its linear range and introduce distortion that the feedback loop cannot suppress. The following section introduces a method to enhance the linearity of the proposed design at lower input voltage amplitudes.

3.3.1 Effect of Third Nonlinear Coefficients on THD

Fig. 3.10 shows the block diagram of a third-order amplifier with three identical gain cells. In the absence of feedback, the transfer characteristic of a basic amplifier (e.g. G_1 in Fig. 3.10) using power series can be expressed as the following polynomial [29]

$$v_i = a_1 v_s + a_2 v_s^2 + a_3 v_s^3 + \dots \tag{3.1}$$

where a_i denotes the nonlinearity coefficients. a_1 is equal to the gain of the amplifier, and a_3 contributes to the third harmonic distortion (HD_3) which plays the main role in an amplifier's nonlinearity. Similar to (3.1), we can write the input voltage and output current relationship of the feedback block, i.e. G_f in Fig. 3.10, as $i_o = f_1 v_{fb}\left(1 + (f_3/f_1)v_{fb}^2\right)$. The effect of increasing the third polynomial coefficient, i.e., f_3, on the THD of an amplifier is investigated through the third-order amplifier of Fig. 3.10 in Simulink. Fig. 3.11 demonstrates the impact of f_3 and c_3 on the amplifier's nonlinearity. In this simulation, initially, the ratios of $(a_3/a_1), (b_3/b_1), (c_3/c_1),$ and (f_3/f_1), are equal to 0.01. Then, f_3 has been increased gradually while keeping all other coefficients constant. The same procedure is repeated for c_3. According to Fig. 3.11, the THD of the amplifier increases significantly by increasing the third polynomial coefficient of the feedback block, f_3. However, increasing c_3 does not impact the THD noticeably.

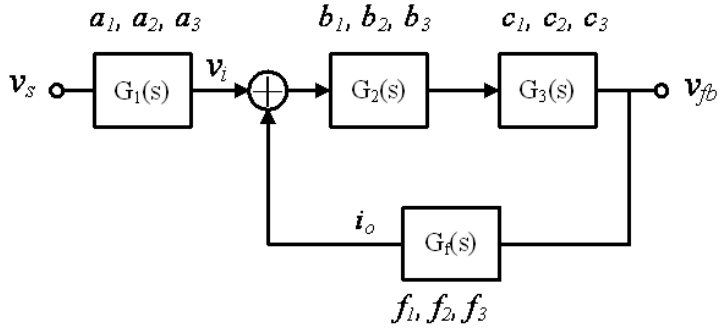


Figure 3.10: Block diagram of a third-order amplifier with feedback.

In the equation for i_o, if we substitute v_{fb} by $v'_{fb} = v_{fb}/2$, and f_1 and f_3 with $f'_1 = 2f_1$ and

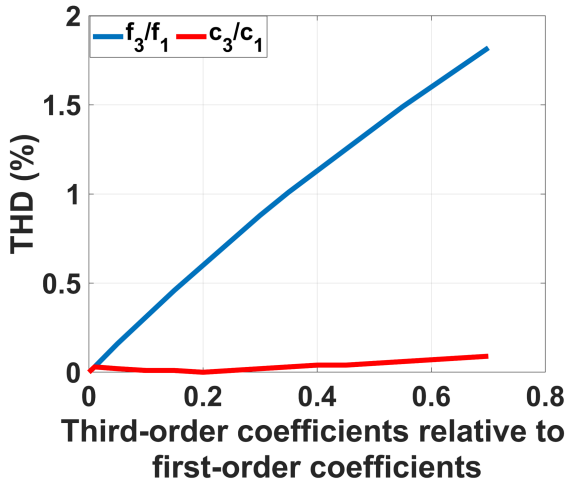


Figure 3.11: THD variations when increasing the third nonlinear coefficients.

$f_3' = 2f_3$, respectively, we will have

$$i_o' = f_1 v_{fb} + \frac{f_3}{4} v_{fb}^3 \tag{3.2}$$

Equation (3.2) can be interpreted as follows: by scaling down the input voltage of the feedback block (G_f) by a factor greater than 1 (e.g., dividing by 2) and correspondingly increasing f_1 and f_3, the contribution of f_3 is reduced proportionally (e.g., by a factor of 4 for a scale of 2). As a result, the THD decreases.

3.3.2 Resistive Voltage Division in Feedback Loops

Based on the above discussion, to address the increased nonlinearity observed in smaller input voltage amplitudes of the previously proposed design (Fig. 3.1), the modified structure of Fig. 3.12 is presented. The $G(s)$ blocks consist of g_m/g_m amplifiers, and the active feedback circuits are inverters. In this improved structure, the voltages at the input of the feedback inverters are halved by resistive voltage dividers. To have the same total gain of 64 V/V in both designs, transistor widths in the feedback inverters have been doubled. With the increased gain in the feedback inverters, their transconductance increases. Regardless of the transconductance value, the inverters have a certain linear input range. Therefore, by increasing the transconductance and applying a smaller input, the feedback inverters can tolerate larger amplitudes. However, this approach increases chip area due to

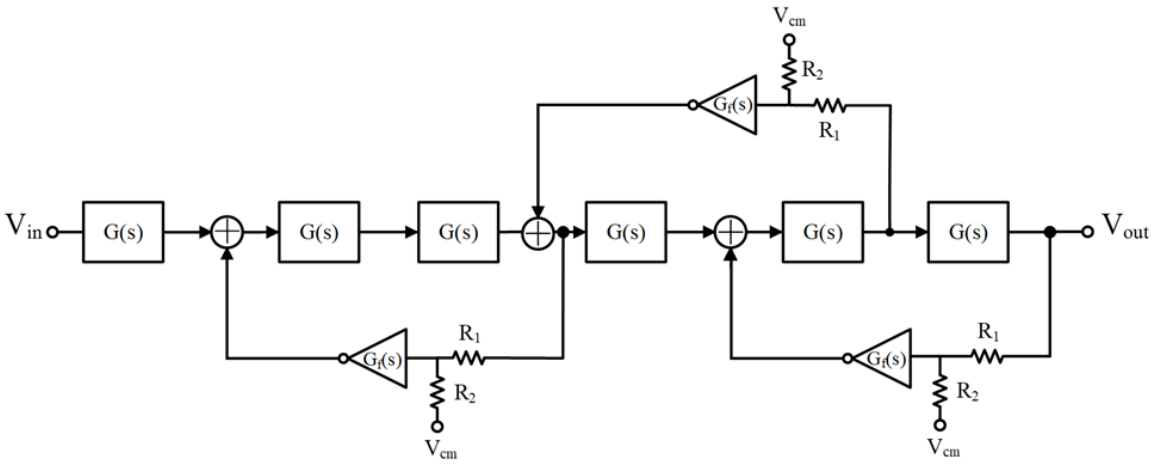


Figure 3.12: Block diagram of the proposed PAM-4 linear main amplifier using g_m/g_m-based amplifiers and IAFB technique with resistive voltage dividers.

the use of passive resistors and slightly raises power consumption because of the additional circuitry required to generate V_{cm}.

3.3.3 Design Methodology and Simulation Results

As discussed in Section 3.2.1, based on our simulations, the g_m/g_m amplifier has the highest linearity when the PMOS transistor's width is 2.5 times larger than the NMOS's in 65 nm CMOS technology. Similarly, based on the overall transfer function of the main amplifier and to have a total gain of 64 V/V, the $G(0)$ and $G_f(0)$ gains are chosen to be 3 and 0.23, respectively. The reason for this is to have low gain peaking, a safe margin for circuit stability, large VEO, and low jitter. The design methodology is discussed in detail in section 3.2.2. In this design, the overall gain of the feedback loops, including G_f and the voltage dividers, is set to 0.23, and each of the forward cells, i.e., G, has a gain of 3.

Fig. 3.13 shows how the THD of the different designs changes when increasing the input voltage amplitude. According to this simulation result, thanks to the added voltage dividers in the feedback loops, the proposed design has the lowest THD in the entire range of the input voltage. To reduce the input voltage of the feedback inverter by 2, we can employ different resistor values. In Fig. 3.13, R_1 and R_2 are set to 800 Ω. Moreover, the width of the NMOS transistor in G_f is increased to 1.275 μm to maintain the total gain of 64. Based on the simulation results, this resistance value

gives the lowest THD across the entire range of input voltage amplitudes. Furthermore, the RLM has improved from 0.94 in the previous design (Fig. 3.1) to 0.98 in the enhanced design (Fig. 3.12).

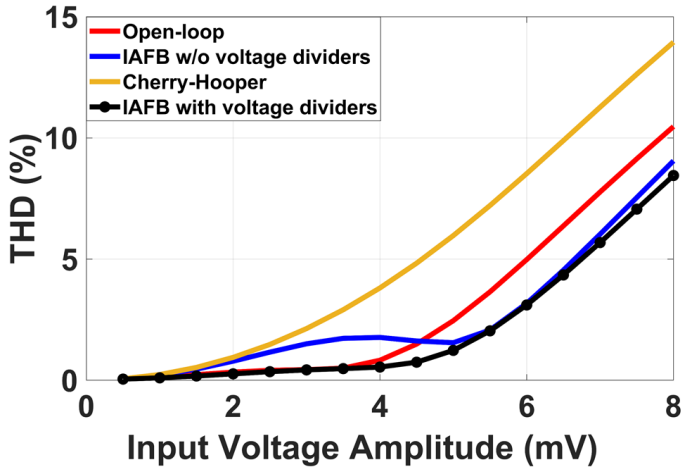


Figure 3.13: THD variations of different structures when increasing the input voltage amplitude.

High-frequency peaking (HFP) can help enhance the bandwidth of the main amplifier. In [27], HFP is realized by inserting a resistor in the active feedback loop of a main amplifier. This resistor along with the gate capacitance of the active feedback introduces a pole in the feedback loop, and therefore, increases the bandwidth. Employing a resistive voltage divider in the feedback loop of the proposed circuit in Fig. 3.12 has a similar impact on the bandwidth. In Fig. 3.14 the impact of increasing the resistors' values on HFP is illustrated. Due to HFP, the larger the resistor values, the wider the bandwidth. However, very large amplitude peaking can make the circuit unstable by shifting the poles to the right half-plane. This is another reason for setting R_1 and R_2 equal to 800 Ω.

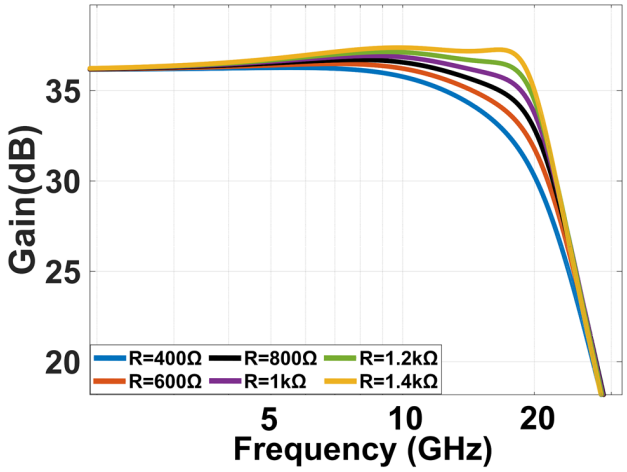


Figure 3.14: HFP and bandwidth variations of the proposed design when increasing the resistor values.

To compare the frequency response of the proposed design (Fig. 3.12) with its open-loop structure, the previously designed main amplifier with IAFB and without voltage dividers in the feedback loops (Fig. 3.1), and the widely used CH amplifier, Fig. 3.15 is plotted. In this figure, all configurations are designed to have a low-frequency gain of 64 ($\sim$ 36.1 dB). With equal gain, IAFB-based designs with and without voltage dividers have the largest bandwidth. However, the bandwidth of the proposed design can be enhanced further by increasing the resistors' values. In other words, with the adopted linearity enhancement method, we can achieve the largest bandwidth and best linearity simultaneously, compared to the other three structures.

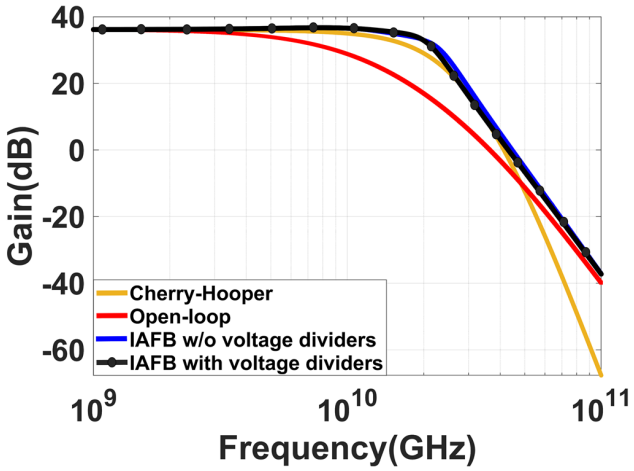


Figure 3.15: Frequency responses of all four structures.

A PRBS is given to a conventional shunt-feedback TIA input, and the output of the TIA is connected to the proposed main amplifier. Fig. 3.16 (a) displays the eye diagram of the circuit in the NRZ signaling scheme, and Fig. 3.16 (b) represents it in PAM-4 format with a UI of 40 ps. Regarding the eye diagrams, the proposed optical receiver has the best performance at $R_{1,2}$ = 400 Ω, due to the minimum HFP. The performance comparison of all four simulated optical receivers (TIA+MA) in single-ended mode is summarized in Table 3.1. Since main amplifiers are the main contributors to optical receivers' nonlinearity, THD is reported only for the MA circuitry.

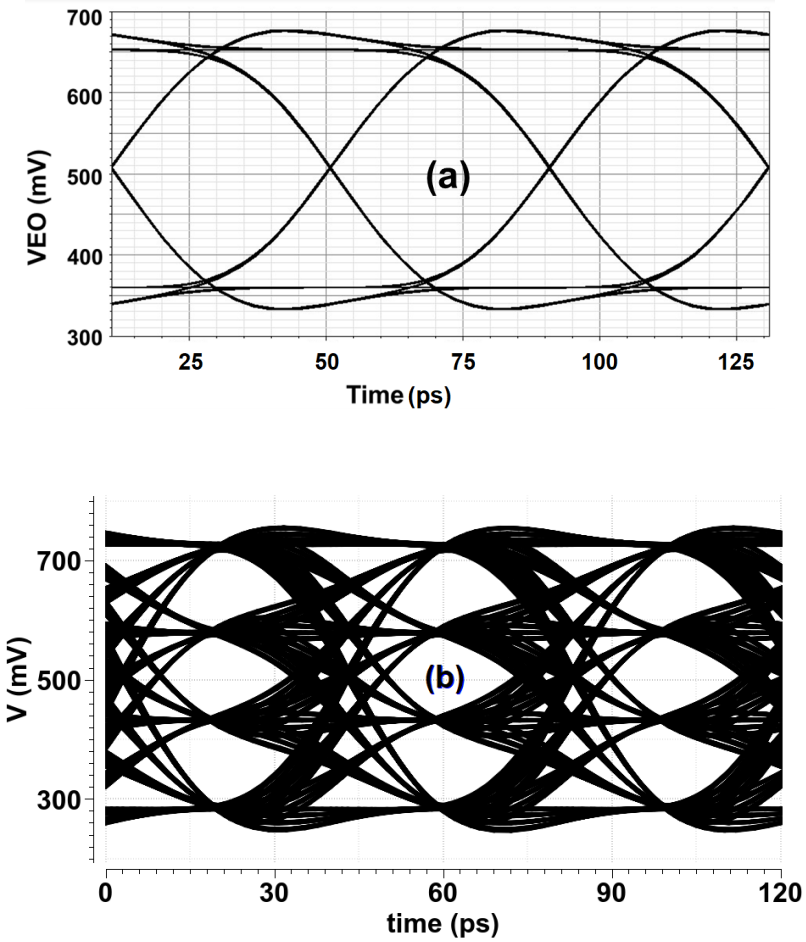


Figure 3.16: The eye diagrams of the proposed design with enhanced linearity in a) NRZ, and b) PAM-4 with 40 ps of UI.

Table 3.1: Simulation Results Comparison Summary

	Cherry-Hooper amplifier	**Open-loop g_m/g_m-based**	**Fig. 3.1**	**Fig. 3.12***
Transimpedance gain (dBΩ)	78.1	78.1	78.1	78.1
THD** @ 1 GHz (%)	3.81	0.83	1.77	0.578
NRZ VEO*** (mV)	227	71.5	279	273.4
RLM	0.893	–	0.942	0.984
Output noise (mV_{rms})	18.65	11.34	19.7	17.93
Input referred noise (μA_{rms})	2.96	5.71	2.54	2.36
Power dissipation (mW)	18.66	12.75	11.67	15.83

* $R_{1,2} = 400\ \Omega$

** Input voltage of ± 4 mV, and the output swing of > 500 mV_{pp}

*** Input current of ± 18 μA

3.4 Conclusion

A highly linear main amplifier is proposed based on the g_m/g_m amplifier and IAFB technique for PAM-4 optical receivers with a data rate of 50 Gb/s and 25 Gb/s for NRZ signaling. The proposed design's bandwidth, linearity, and VEO are compared to those of the CH amplifier. Simulation results show that the g_m/g_m-based configuration offers a wider bandwidth than the CH amplifier when applying the IAFB technique. Moreover, at the same input, the linearity and VEO of the proposed circuit are superior to those of the CH amplifier. To the best of the authors' knowledge, the proposed design is the first example of the IAFB-based topology using inverter-based amplifiers. Then, a method to enhance linearity in the proposed g_m/g_m-based main amplifier with negative active feedback loops is introduced. Through calculations and simulations, it is observed that decreasing the input voltage of the feedback inverters reduces the third nonlinearity coefficient. This concept is implemented by integrating resistive voltage dividers into the feedback loops and increasing the gain of the feedback inverters. Consequently, this method addresses the challenge of the IAFB technique's inability to mitigate nonlinearity at lower input voltages compared to the open-loop design due to surpassing the linearity range of the final feedback inverter. Our simulations demonstrate about a 67% decrease in the THD of the proposed main amplifier at about 500 mV_{pp}

output swing, compared to the first designed circuit.

Chapter 4

Equalizing Main Amplifier

This chapter discusses the design of an equalizing main amplifier (EMA) for high-speed optical receivers in linear-drive architectures. It focuses on integrating high-frequency peaking (HFP) to incorporate equalization into the optical receiver front-end without the need for separate CTLEs or passive inductors. Using this technique, an equalizing g_m/g_m-based main amplifier is proposed. The nested feedback technique is employed to improve equalization for more lossy transmission lines.

4.1 Impact of Channel Losses

Channel losses significantly impact signal integrity, particularly in high-speed optical links, and must be carefully addressed in optical receiver design. The proposed optical receiver in Chapter 3 (Fig. 3.12) performs reasonably well in NRZ format simulated with the channel model of a measured high-speed PCB trace at 10 Gb/s with moderate-loss, as evidenced by the open eye diagram in Fig. 4.1 (a). However, the PAM-4 eye diagram of this design using the same channel model, shown in Fig. 4.1 (b), is nearly closed. Moreover, since most high-speed buses in modern computing systems are built differentially, it is practical to characterize interconnect behavior using multimode S-parameters [30]. Therefore, when the proposed optical receiver is assessed in a differential configuration with a high-loss channel modeled as a 4-port differential system [30], the NRZ eye becomes completely closed, as illustrated in Fig. 4.2 (b), despite appearing open when driving a 50 Ω load in

Fig. 4.2 (a). These results highlight the need for an equalizing feature to mitigate channel-induced losses and reopen the eye. This becomes even more critical when these same channels are driven by circuits implemented in advanced technology nodes capable of operating at higher data rates, where frequency-dependent attenuation increases linearly with frequency. The following section presents the design process of incorporating the equalizing feature into the proposed linear main amplifier.

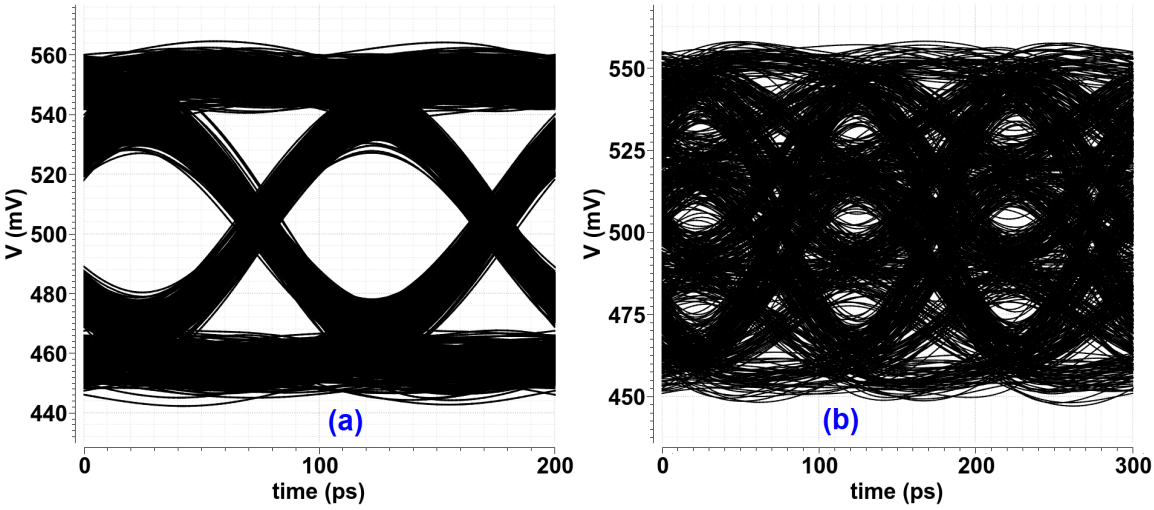


Figure 4.1: a) NRZ, and b) PAM-4 eye diagram of the proposed linear optical receiver in Chapter 3 at 10 and 20 Gb/s, respectively, when simulated with a measured PCB trace channel model.

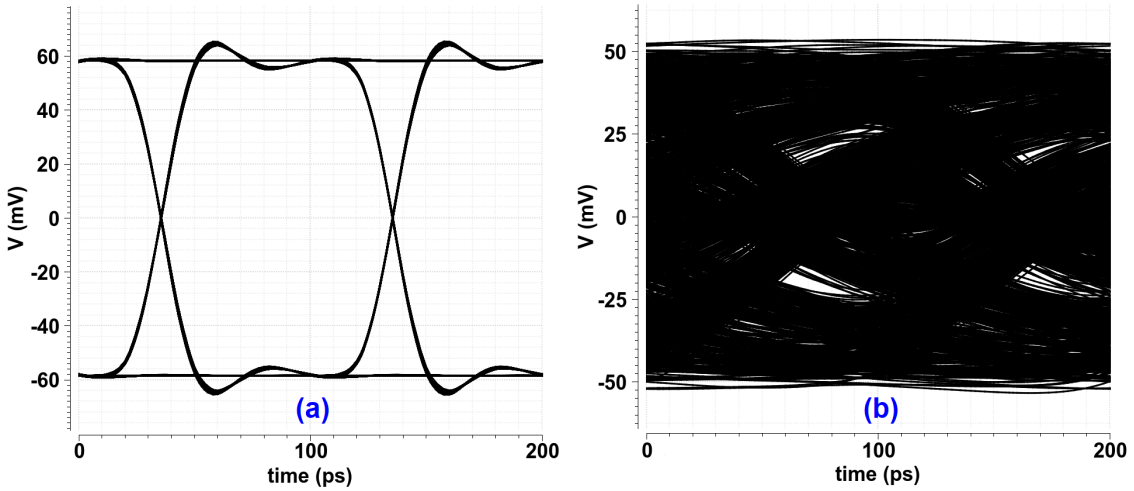


Figure 4.2: NRZ eye diagram of the proposed linear optical receiver in Chapter 3 at 10 Gb/s in differential structure when a) driving a 50 Ω load, b) simulated with a high-loss channel modeled as a 4-port differential system [30].

4.2 Equalizing MA Based on a Third-Order Gain Stage

As discussed in Chapter 3, the proposed linear main amplifier in Fig. 3.12 demonstrates HFP due to the resistive voltage dividers in the feedback loops, which allow for bandwidth extension. This feature can be used to equalize the transmission line (channel) that follows the main amplifier. Starting with the third-order stage shown in Fig. 4.3 and adopting a similar approach to [27], we can express the transfer functions of the first-order gain and feedback cells as follows

$$G(s) = \frac{G_m R_1}{1 + sR_1C_1}, \quad G_f(s) = \frac{G_{mf}\, R_1}{(1 + sR_1C_1)(1 + sR_hC_h)} \tag{4.1}$$

where R_1 and C_1 represent the load resistance and capacitance of the first-order gain cell, while R_h and C_h are the load resistance and capacitance at the input of the feedback cell. Note that $G_f(s)$ is the gain from the output, V_{out} to the summing junction.

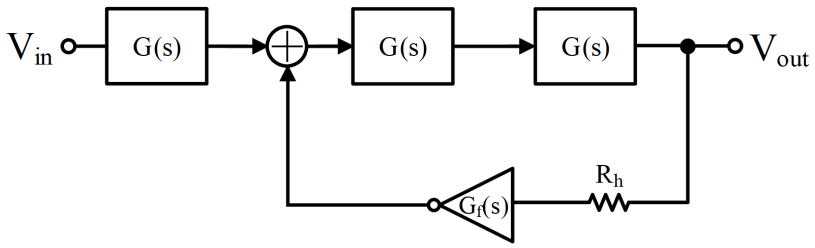


Figure 4.3: Equalizing third-order gain stage.

The transfer function of the third-order block is

$$H_{3\text{rd}}(s) = \frac{G_1(s)\, G_2(s)\, G_3(s)}{1 + G_2(s)\, G_3(s)\, G_f(s)} \tag{4.2}$$

where $G_1 = G_2 = G_3 = G$. If we define $\omega_1 = (R_1C_1)^{-1}$, $\omega_h = (R_hC_h)^{-1}$, $\alpha = G_mR_1$, and $\beta = G_{mf}R_1$, by substituting $G(s)$ and $G_f(s)$ into equation (4.2), we obtain

$$H_{3\text{rd}}(s) = \frac{\alpha^3 \left(1 + \frac{s}{\omega_h}\right)}{\left(1 + \frac{s}{\omega_1}\right)^3 \left(1 + \frac{s}{\omega_h}\right) + \alpha^2\beta} \tag{4.3}$$

As shown in (4.3), the resistor R_h in the feedback loop of the third-order gain stage forms a pole with the parasitic capacitances at the input of the feedback cell, resulting in the introduction

of a zero in the overall transfer function. In the absence of such zeros, the system exhibits an all-pole response, where the gain gradually decreases at higher frequencies due to the dominant poles. Although all-pole systems can exhibit peaking when the quality factor (Q) of the poles is high, this peaking is typically narrowband and not suitable for effective equalization in broadband applications. In contrast, the presence of a zero introduces a broad gain boost at higher frequencies, counteracting the natural roll-off of the amplifier. This gain enhancement is essential for extending the effective bandwidth and achieving the desired equalization effect in high-speed communication systems. Carefully positioning the pole-zero pair enables an equalizing effect, enhancing the frequency response, and improving the integrity of the signal. By setting the zero below the Nyquist frequency (e.g. 5 GHz for a 10 Gb/s data rate), high-frequency peaking is initiated early enough to compensate for the channel and amplifier roll-off while avoiding unnecessary low-frequency gain. The complex-conjugate poles located above the Nyquist limit the extent of high-frequency gain, preserving stability. This pole–zero configuration produces controlled equalization, resulting in a flatter response in the vicinity of the Nyquist frequency.

The position of poles on the complex plane significantly impacts system behavior. Similar to second-order systems, each complex-conjugate pole pair in a higher-order system can be locally modeled as a second-order system, where the Q and the damping ratio (ζ) are related by $Q = 1/2\zeta$. A high-Q pole lies closer to the imaginary axis, indicating lower damping and a sharper peak in the frequency response near the pole frequency. This leads to a narrow bandwidth and increases the risk of instability. In contrast, a low-Q pole lies further from the imaginary axis, resulting in greater damping and a broader, more attenuated frequency response around the pole frequency. For a fixed natural frequency (ω_n), this configuration yields a wider bandwidth, a more stable system, and a smoother roll-off without sharp peaks. Carefully controlling the Q factor of poles is crucial in designing circuits that require both stability and wideband performance.

Fig. 4.4 illustrates how Q and ζ of the conjugate poles in the third-order gain stage of Fig. 4.3 vary with the feedback resistor R_h. As R_h increases, the zero frequency $\omega_h = (R_h C_h)^{-1}$ decreases, leading to a reduction in Q and an increase in damping, which results in more stable but slower system dynamics. This behavior is shaped by the relative values of ω_1 and ω_h, which control the pole and zero locations, while the scaling parameters α and β influence the gain and damping

through their effect on the denominator of (4.3). These parameters collectively determine the degree of high-frequency peaking, which is intentionally introduced to compensate for channel loss.

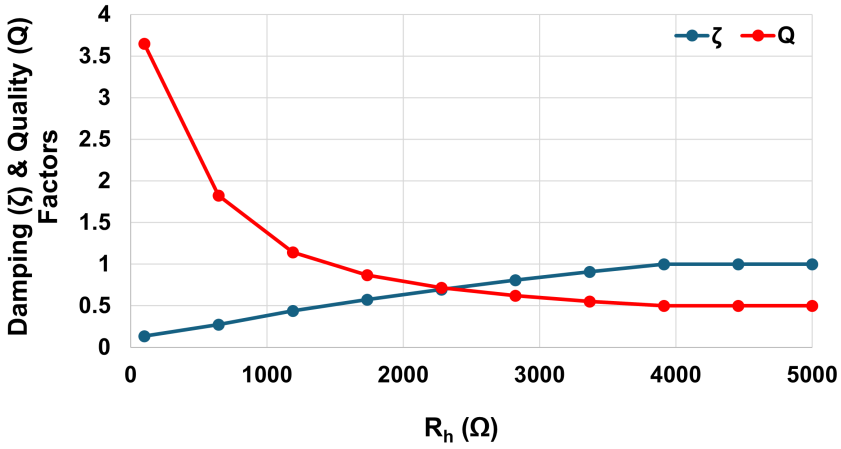


Figure 4.4: Variations of the third-order gain cell's conjugate poles' quality and damping factors when decreasing the zero frequency or increasing R_h.

As a starting point, R_h is set to 2.3 kΩ, where the Q factor and damping ratio ζ of the complex conjugate poles are equal to 0.7. The effect of varying the pole Q while keeping R_h constant on the frequency response of the third-order gain cell is shown in Fig. 4.5. In this analysis, the Q factor of a complex conjugate pole pair is varied while maintaining a constant pole magnitude. For each Q value, the corresponding pole locations are calculated, and a transfer function with a fixed zero is constructed. The resulting Bode plots illustrate the impact of the Q factor on the frequency response, particularly in terms of peaking behavior and bandwidth variation. As anticipated, increasing Q from 0.1 to 1 reduces damping, resulting in greater gain peaking at higher frequencies.

To see the effect of Q on equalizing the third-order gain stage, a transmission line model [31] has been cascaded with it. The channel includes both conductor and dielectric losses, modeled using a distributed RLGC network. Key parameters include a characteristic impedance of 50 Ω, a line length of 0.6 m, and a propagation velocity of 1.5×10^8 m/s. Conductor losses are modeled with a DC resistance of 0.5 Ω/m and a frequency-dependent skin-effect term scaled by 60 Ω/m at 10 GHz. Dielectric losses are captured using a loss tangent of 0.017, applied through a frequency-dependent capacitance model. Fig. 4.6 (a) and (b) illustrate how varying the pole Q affects the frequency and pulse responses of the overall cascaded structure. As shown, when Q is around 0.7, the ISI is

minimized, and the frequency response remains flat around 5 GHz, i.e., the Nyquist frequency for the 10 Gb/s data rate.

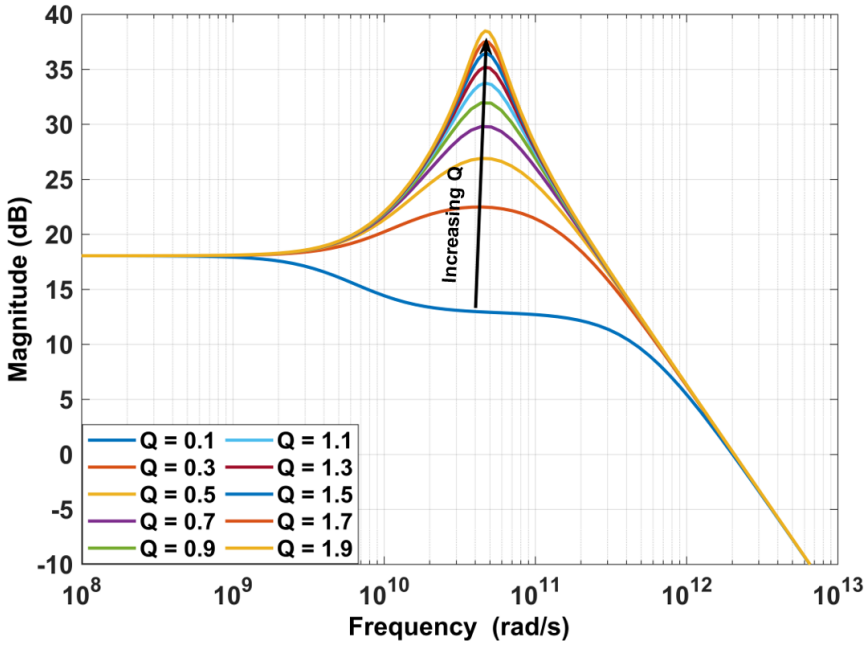


Figure 4.5: High-frequency peaking of the third-order equalizing amplifier when increasing pole Q from 0.1 to 1.9.

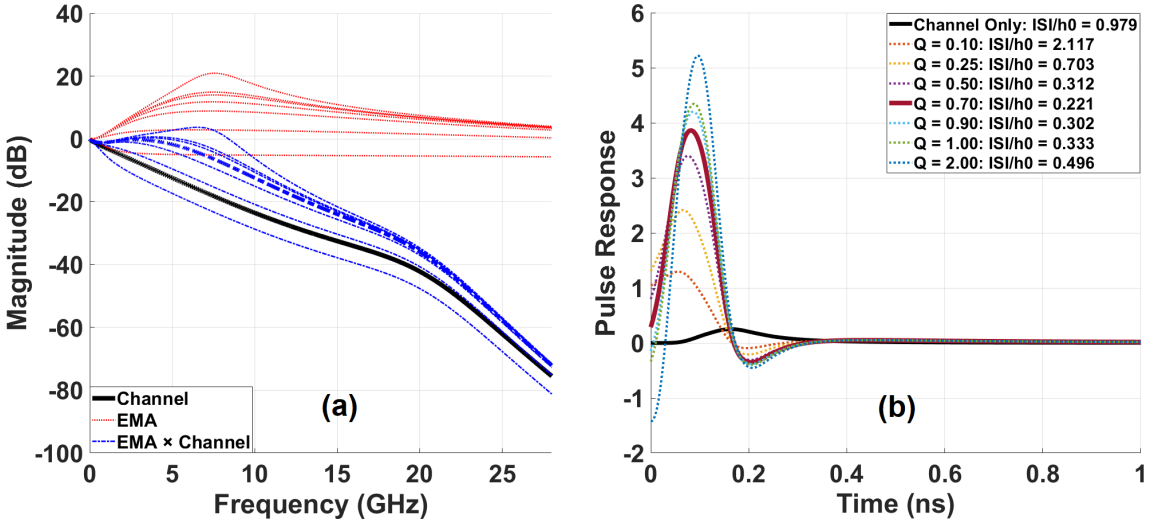


Figure 4.6: (a) Frequency responses of the channel model Carusone:2007, the third-order EMA, and their cascade for different pole-Q values; (b) Pulse responses of the cascaded channel and third-order EMA for various pole Q values.

The nested feedback architecture shown in Fig. 2.21 employs a third-order feedback loop in

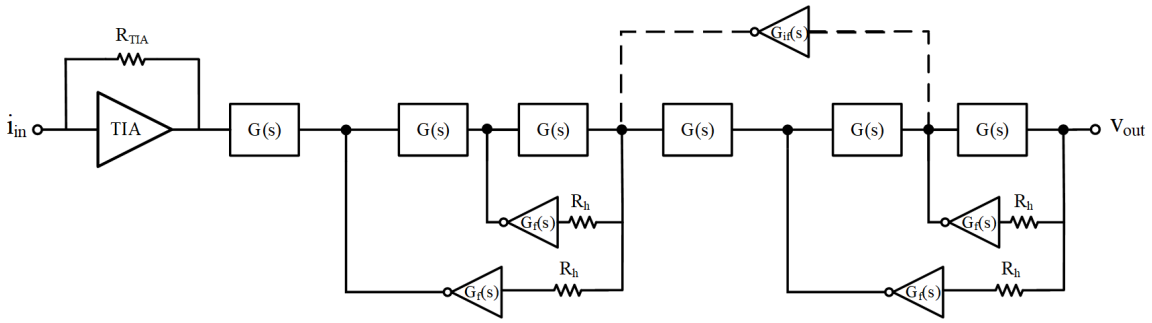


Figure 4.7: Proposed linear optical receiver with equalizing main amplifier.

which the core gain stage is a second-order active feedback amplifier. This second-order stage is embedded within the higher-order loop, forming a nested feedback structure. The nested configuration introduces a feedforward zero in the loop gain, enhancing the stability margin compared to both conventional third-order and third-order interleaved designs [32]. Simulation results also demonstrate improved equalization performance for more lossy channels. To leverage these benefits, a nested feedback loop incorporating an R_h resistor is added to the third-order gain stage and cascaded with another third-order nested feedback block, as illustrated in Fig. 4.7. Similar to the linear main amplifier proposed in Chapter 3, the $G(s)$ blocks consist of g_m/g_m amplifiers, while the $G_f(s)$ blocks are inverters. With R_h = 2.3 kΩ, the main amplifier exhibits $\sim$ 5 dB of HFP to compensate for channel losses.

A PRBS connected to a shunt-feedback TIA is used to generate the eye diagrams for this structure. Fig. 4.8 (a) shows the NRZ eye diagram at the channel input, while Fig. 4.8 (b) displays the eye diagram at the channel output, clearly demonstrating the equalizing effect of the proposed main amplifier. The VEO has increased from 49 mV in Fig. 4.1 (a) to 63.2 mV in this design. Furthermore, the PAM-4 eye diagram in Fig. 4.9 (a) highlights the improved equalization capability of the proposed design compared to the previous result shown in Fig. 4.1 (b). The total harmonic distortion (THD) has improved from 1.48% to 1.23%, and the ratio level mismatch (RLM) has increased from 0.88 to 0.93. Fig. 4.9 (b) presents the PAM-4 eye diagram of the proposed EMA with the same channel model shortened by 25%. All the above simulations were performed using the measured high-speed PCB trace channel model.

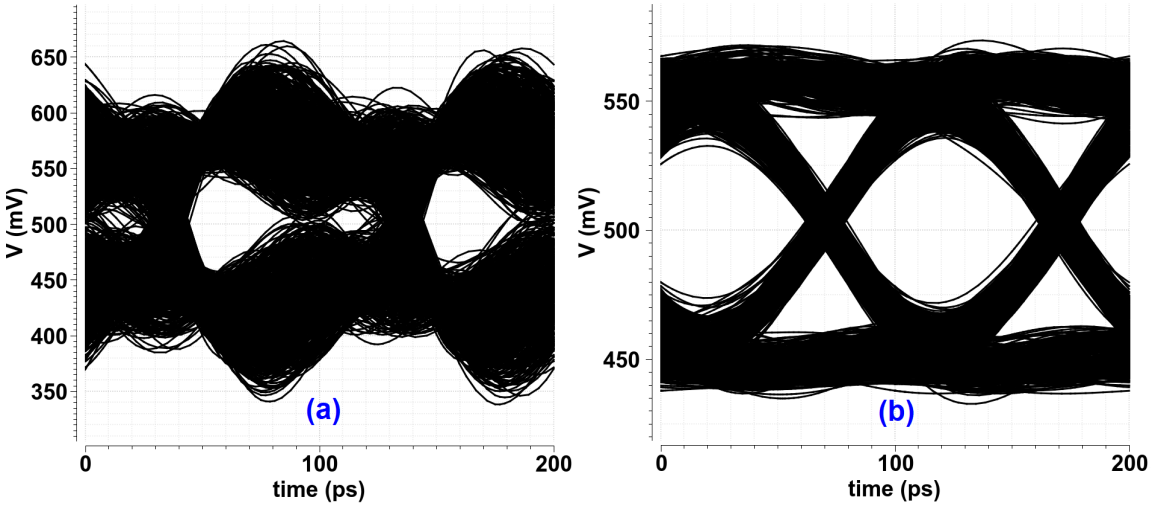


Figure 4.8: NRZ eye diagram of the proposed equalizing main amplifier at 10 Gb/s data rate (a) at the input of the measured channel and (b) at the output of the measured channel.

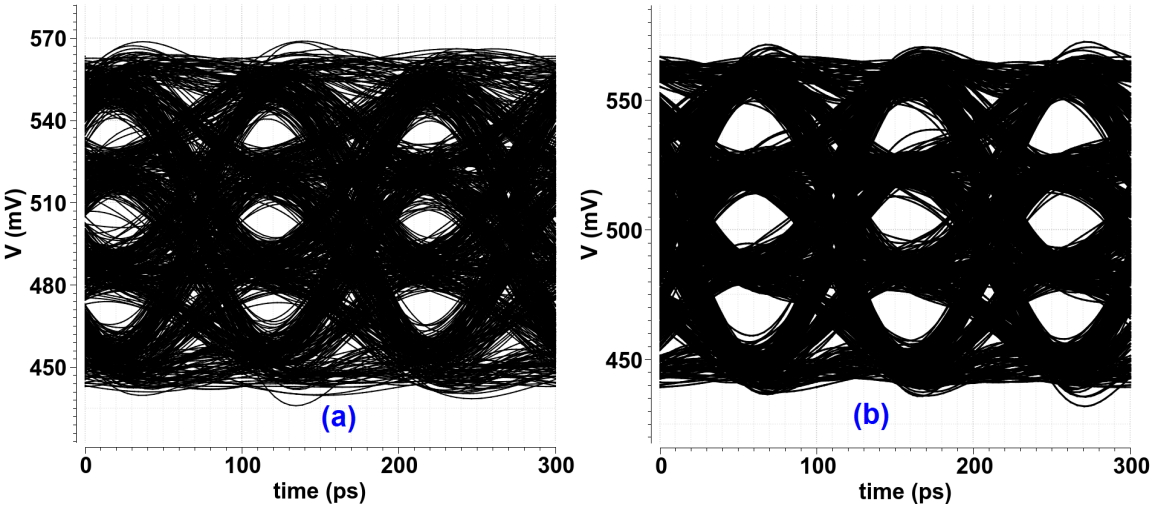


Figure 4.9: PAM-4 eye diagram of the proposed equalizing main amplifier at a 20 Gb/s data rate using (a) the measured PCB trace channel model and (b) a 25% shorter version of the same channel model.

To address the severe attenuation introduced by the high-loss 4-port differential channel [30], a stronger equalization is required, which can be achieved by increasing the amplitude of HFP. Fig. 4.10 illustrates the frequency response of the equalizing main amplifier when connected to an AC-grounded 50 Ω load. Given this plot, HFP increases as the resistor R_h increases. It is observed that the HFP shows negligible improvement beyond R_h = 15 kΩ. Therefore, R_h is set to 20 kΩ,

resulting in an HFP of approximately 6.9 dB.

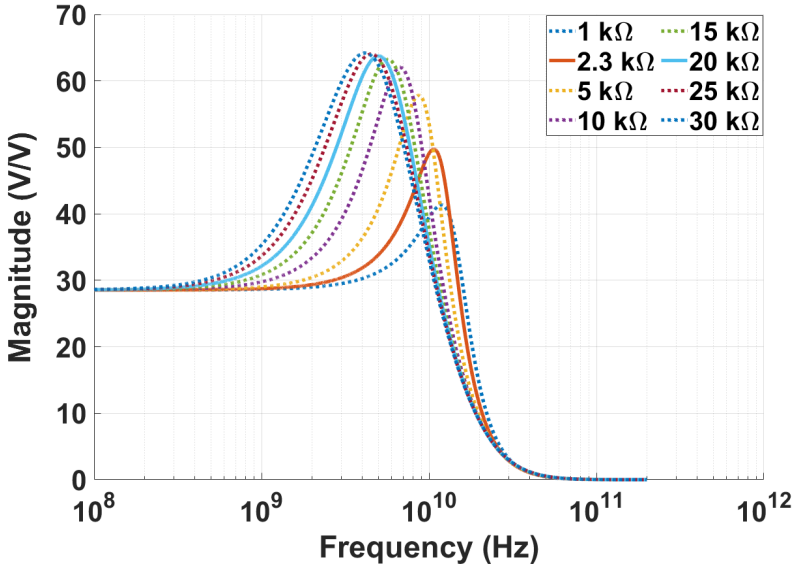


Figure 4.10: Frequency response of the proposed EMA when increasing R_h.

Fig. 4.11 presents the NRZ eye diagram of the proposed EMA when connected to the high-loss differential channel [30]. In addition to the VEO improving from 0 mV in Fig. 4.2 (b) to 42 mV in Fig. 4.11 (b), the voltage swing between the constant 0 and constant 1 levels is also larger. Compared to Fig. 4.2 (a), the NRZ eye diagram in Fig. 4.11 (a) exhibits significant overshoot when the differential EMA drives a 50 Ω load. This enhanced peaking effectively compensates for the severe channel losses.

Simulation results show that incorporating interleaving active feedback (IAFB), indicated by the dashed connections in Fig. 4.7, into the EMA, while maintaining constant overall gain, reduces the THD to 1% at the same output swing. However, due to the pole-splitting phenomenon that was discussed in Section 3.2.2, this configuration reduces gain peaking, thereby degrading the equalization capability and resulting in a smaller VEO in both NRZ and PAM-4 eye diagrams.

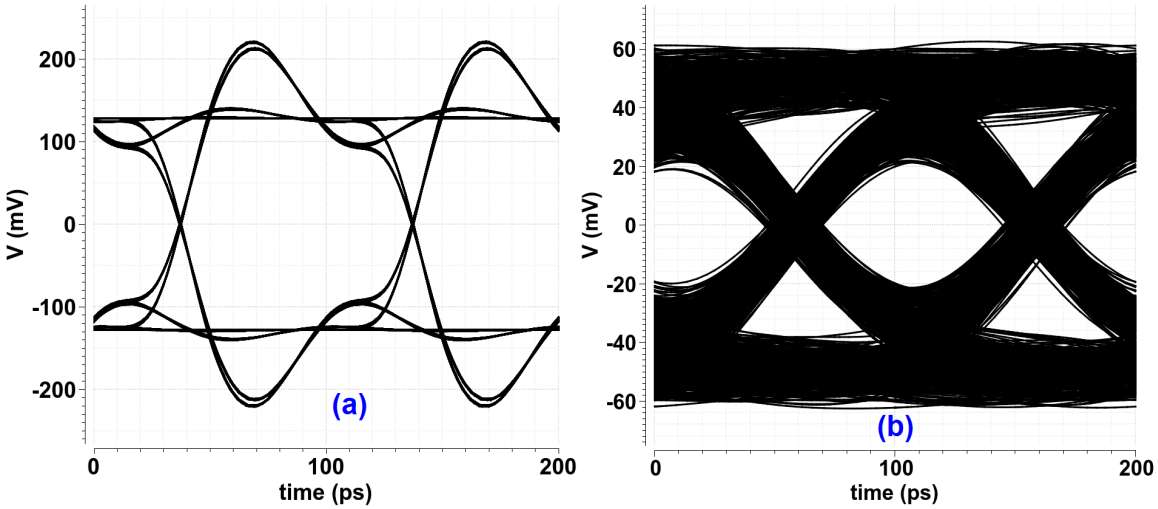


Figure 4.11: NRZ eye diagram of the proposed EMA at 10 Gb/s in differential structure when a) driving a 50 Ω load, b) simulated with a high-loss channel modeled as a 4-port differential system [30].

4.3 Conclusion

The equalizing main amplifier achieves HFP by introducing a pole in the active feedback loops, enabling effective equalization without the drawbacks of passive inductors or the need for an additional CTLE stage. In this chapter, the equalization feature is integrated into the proposed linear main amplifier using a nested feedback technique, where a resistor is used to introduce the desired pole. This approach reduces chip area and power consumption while preserving optimal gain and bandwidth, thereby enhancing the overall performance of high-speed optical receivers.

Chapter 5

Design and Implementation of a Differential Linear Optical Receiver with an Equalizing Main Amplifier

This chapter begins by presenting the differential design of the proposed linear optical receiver, which incorporates an equalizing main amplifier. Post-layout simulation results are then provided, followed by a detailed overview of the chip fabrication process, including layout implementation and wire-bonding to the custom high-speed PCB. The chip was developed as part of an industrial collaboration, targeting 10 Gb/s NRZ operation in a 65 nm CMOS technology for integration into a prototype optical transceiver.

5.1 Fully Differential Design

High-speed transceivers rely on differential circuit topologies and genuinely differential I/O signals, as these approaches offer strong resistance to common-mode noise and improve power supply rejection. Additionally, many related digital blocks, such as analog-to-digital converters (ADCs), are designed to work best with fully differential inputs. In the following, the design approach for implementing the fully differential optical receiver is presented.

5.1.1 Cross-Coupled Inverters

As discussed in section 2.4.2, [15] and [5] employ cross-coupled inverters, as illustrated in Fig. 5.1, to achieve a pseudo-differential architecture. This arrangement increases common-mode rejection and helps reduce mismatch by partially coupling the two branches. Intuitively, when a portion of the signal from one branch is added to the other, input mismatches are effectively canceled at the output [5]. The size of the cross-coupled inverters determines the extent of amplitude and phase mismatch cancellation. However, larger cross-coupled inverters introduce additional loading on the signal path, which reduces bandwidth [5]. Moreover, to prevent the formation of a latch, their sizes are chosen to be smaller than those of the transconductor and load inverters in the g_m/g_m design.

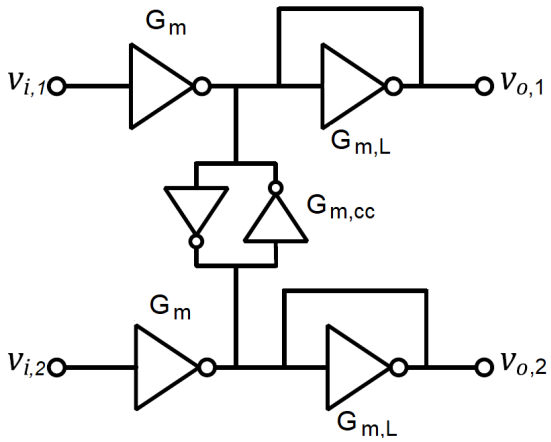


Figure 5.1: Pseudo-differential gain stage with cross-coupled inverters.

The optimal point for introducing the single-ended to differential conversion is immediately after the front-end, where the signal swing is still low, as this minimizes the risk of nonlinearity [5]. As shown in Fig. 5.2, cross-coupled inverters are employed to convert the proposed single-ended linear optical receiver into a fully differential design. The cross-coupled inverters introduce a negative resistance that increases the net driving-point impedance, which in turn enhances the overall gain. To maintain a constant total gain equal to the previous designs in Chapter 3, the gain of the forward cells ($G(s)$) and the feedback cells ($G_f(s)$) are reduced to 2 and 0.19, respectively. Additionally, the TIA resistors (R_{TIA}) and the feedback resistors (R_h) can be independently tuned via

transmission gates (T-gates), enabling adjustment of both the TIA gain and the degree of equalization in the main amplifier. Furthermore, the interleaved active feedback (IAFB) loops, implemented using the $G_{if}(s)$ inverters, can be enabled to enhance the linearity of the proposed design, but at the cost of smaller eye openings.

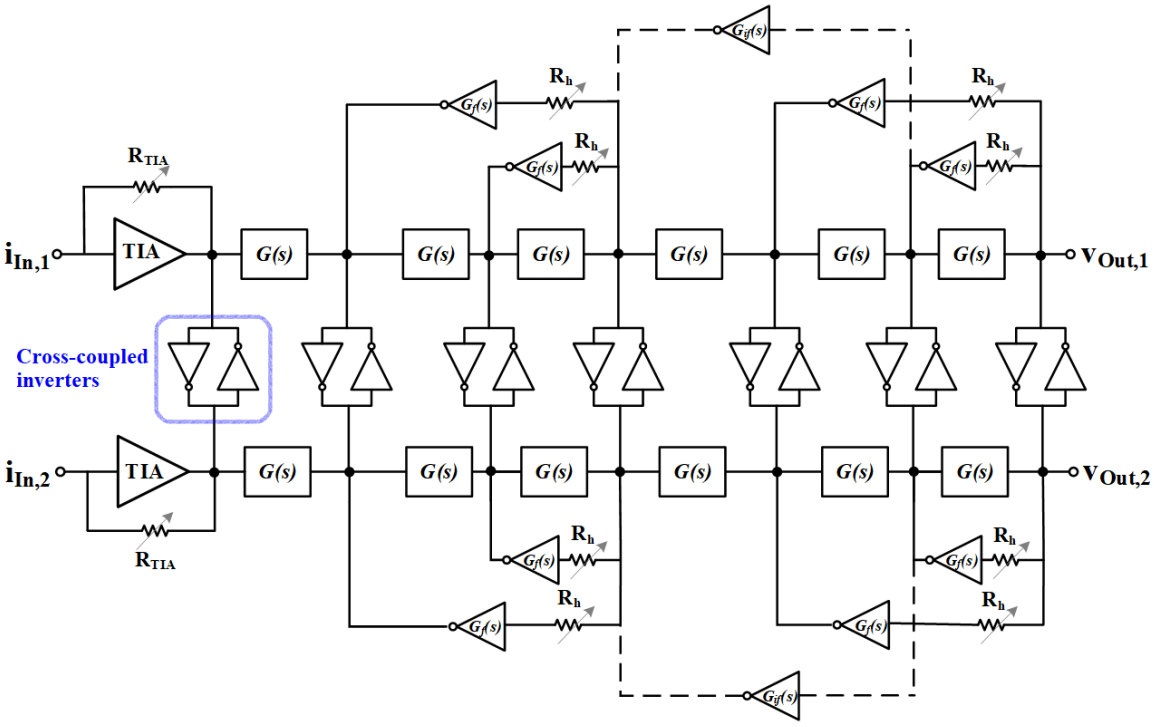


Figure 5.2: Proposed differential linear optical receiver.

5.1.2 Differential Photodiodes

Generating true differential signals is not inherently straightforward in intensity modulation and direct detection (IMDD) links, since the photodetector (PD) is naturally single-ended. Traditional approaches overcome this by employing additional electronic circuits at the front end, such as dummy or replica TIA stages [33, 34], and single-to-differential (S2D) amplifiers [5, 35]. While these methods can provide differential outputs, they often suffer from transimpedance gain mismatch and bandwidth degradation, and generally require extra amplification stages that can cause linearity issues [36]. This increased complexity is manageable for NRZ signaling, but becomes a significant challenge for more advanced modulation formats such as PAM-4.

An alternative approach presented in the literature, while still operating within the IMDD framework, involves generating fully differential signals directly at the PD level [36]. As shown in Fig. 5.3, instead of relying solely on electronic post-processing, the optical signal is split into two equal parts and directed to two matched PDs, each biased in a complementary fashion. This fully-differential configuration PD scheme allows the direct generation of complementary photocurrents that feed into a differential TIA. The main advantage of this approach is the elimination of complex S2D electronic blocks, resulting in a simpler and more robust receiver architecture that is inherently suited for high-speed and advanced modulation formats. Additionally, this method avoids the large on-chip DC-blocking capacitors required in other schemes, which can introduce significant parasitic capacitance and increase chip area, an important consideration for bulk CMOS processes.

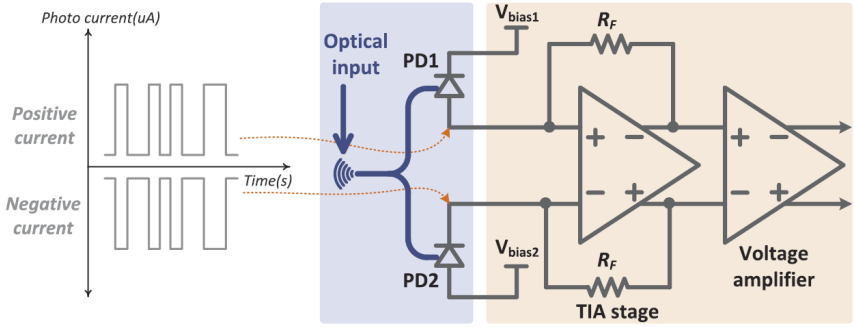


Figure 5.3: Architecture of the proposed differential optical receiver in [36].

The primary trade-off of the fully differential PD approach compared to the single-ended case with the same input optical power is a slight reduction in signal-to-noise ratio (SNR), about 3 dB, since the available optical power is split between two detectors and the noise from both PD arms is uncorrelated [36]. However, the overall benefits, integration, reduced complexity, and suitability for low-voltage, low-power operation, outweigh this drawback for many short-reach communication applications. Therefore, this architecture was adopted in our design of the differential TIA.

5.2 4-Channel Linear Optical Receiver Chip Design

Fig. 5.4 presents the block diagram of the designed 4-channel optical receiver. It features differential PDs that generate complementary current signals at the differential inputs. These signals

are converted to voltage by a shunt-feedback TIA. The resulting voltage is then amplified by the equalizing main amplifier (EMA) stage, which also applies deliberate over-equalization to compensate for channel losses in the follow-on transmission line. Due to the unipolar nature of the optical signal, a DC offset compensation (DCOC) block is incorporated into the optical receiver to ensure that the differential output is centered around 0 V. The shift register is used to tune the TIA gain and the feedback resistor values in the main amplifier.

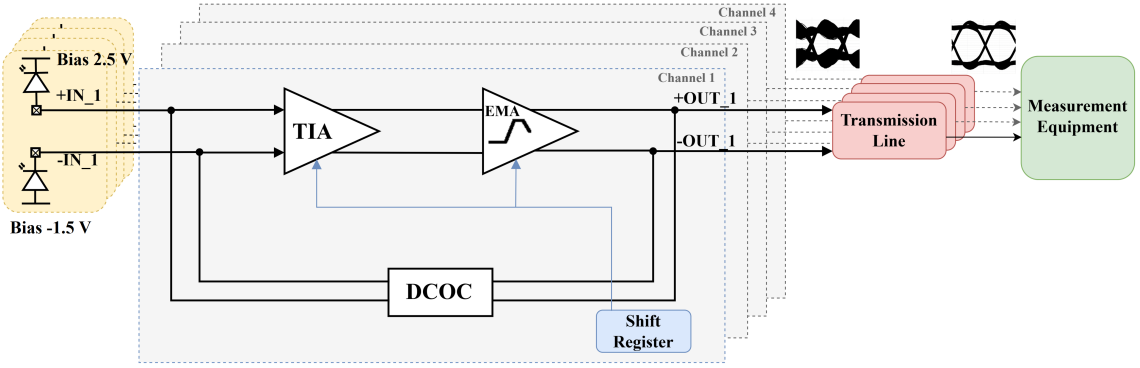


Figure 5.4: Block diagram of the 4-channel differential optical receiver.

5.2.1 Layout Design

Fig. 5.5 shows the layout of the main circuitry for a single channel of the proposed optical receiver, implemented in 65 nm CMOS technology. As labeled in the figure, it consists of a differential shunt-feedback TIA followed by a six-stage differential main amplifier. Transmission gates (T-gates) are included to enable tunability of the receiver. Additionally, 20 kΩ resistors are integrated for operation under very high-loss channel conditions. The whole analog front-end circuitry occupies an area of 7781.5 $\mu\mathrm{m}^2$. It is notable to mention that a typical spiral passive inductor of 500 pH has an area of approximately 300 $\mu\mathrm{m}^2$ x 350 $\mu\mathrm{m}^2$, which is extremely larger than the analog circuitry of the proposed optical receiver. Notably, as shown in the figure, a typical 500 pH spiral passive inductor alone occupies approximately $300, \mu\mathrm{m} \times 350, \mu\mathrm{m}$, which is significantly larger than the entire analog circuitry of the proposed optical receiver. This comparison highlights the substantial area savings and reinforces the importance of adopting an inductorless design.

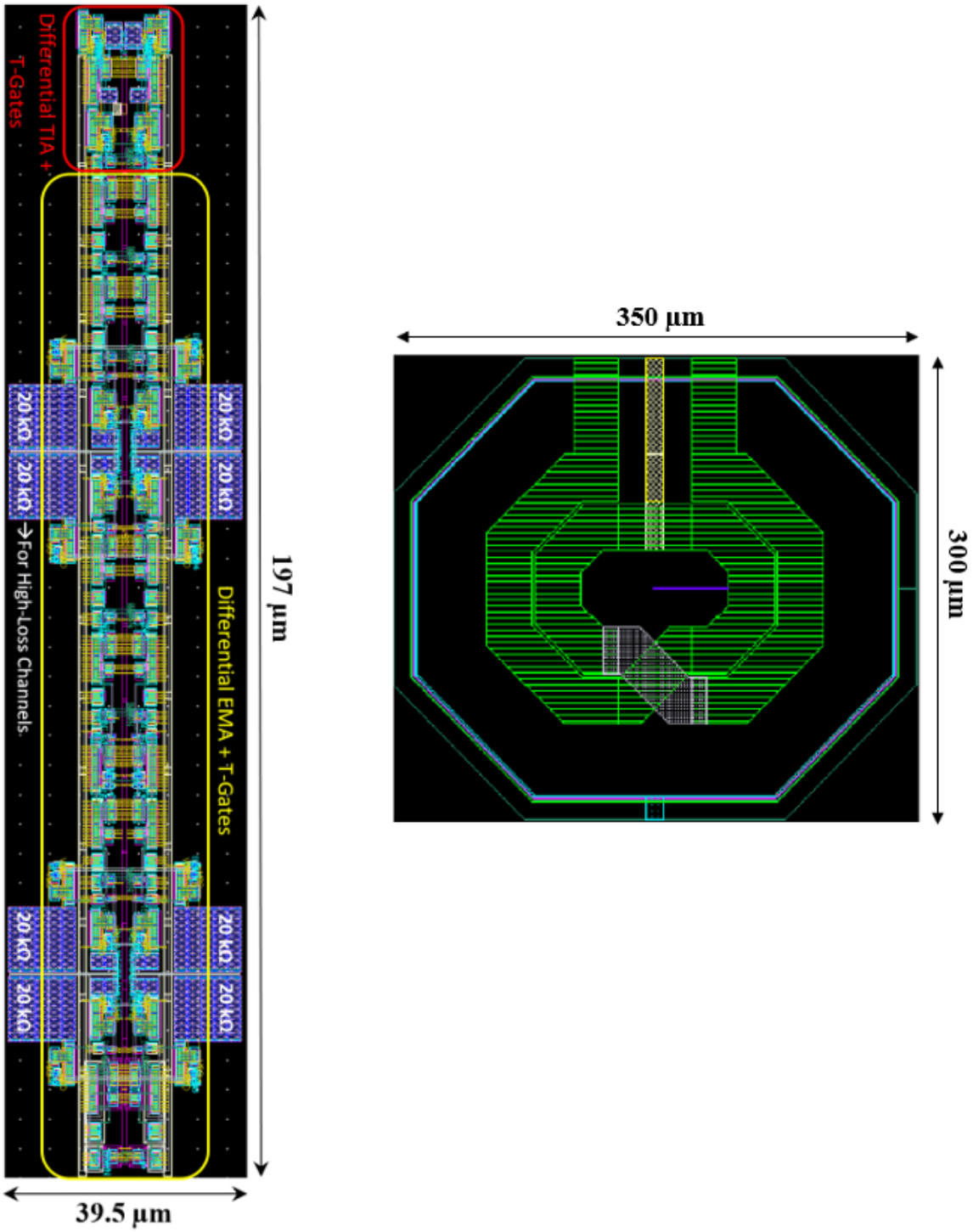


Figure 5.5: Layout of the main circuitry of a single channel of the proposed differential optical receiver.

5.2.2 Post-layout Simulation Results

The proposed optical receiver operates with a 1 V supply and consumes around 30 mW of power per channel. The frequency response of a single channel of the optical receiver when driving a 50 Ω load is shown in Fig. 5.6, based on both schematic-level and post-layout simulations. The low-frequency gain is approximately 79.5 dB Ω, and the -3 dB bandwidth in the post-layout simulation is 6.7 GHz, while in the schematic-level simulation, the bandwidth is 11.8 GHz. The red curve represents the frequency response of the optical receiver when connected to the measured high-speed PCB trace channel model (grey curve) in post-layout simulation. Compared to the schematic-level simulation, the reduction in bandwidth is expected, primarily due to parasitic capacitance and resistance present in the extracted layout. For low-ISI systems, a bandwidth of approximately 50% to 70% of the data rate is typically required. Therefore, the proposed optical receiver is expected to support a data rate of approximately 10 Gb/s per channel, or 40 Gb/s in total in NRZ format.

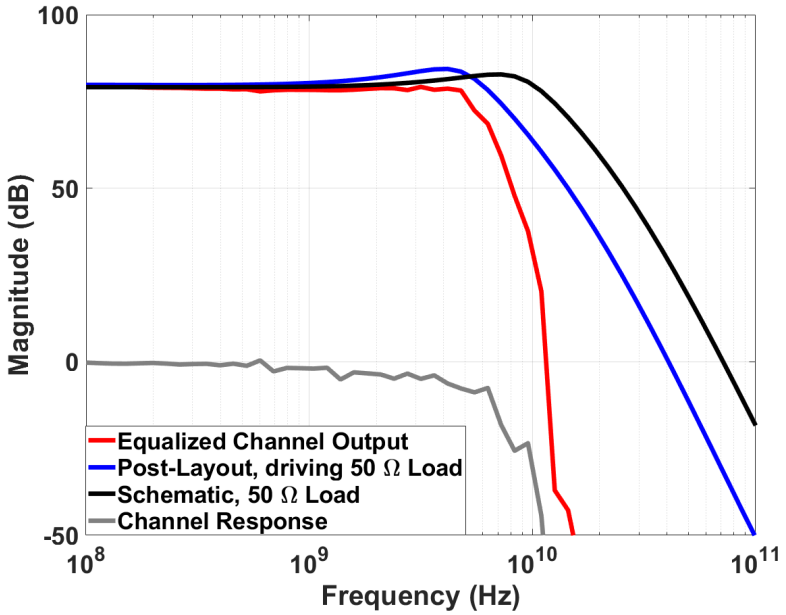


Figure 5.6: Frequency response of the proposed optical receiver driving a 50 Ω load, shown for both schematic-level and post-layout simulations (black and blue), the measured high-speed PCB trace channel model (grey), and the cascaded response of the optical receiver and the channel (red).

Based on simulations, while setting $R_h = 400\ \Omega$ and adding the cross-coupled inverters, the EMA achieves 7.6 dB of high-frequency peaking (HFP), which is sufficient to equalize the channel.

Therefore, the R_h resistors can be set to 400 Ω or 20 kΩ to adjust the equalization strength. The NRZ eye diagram of the optical receiver when driving a 50 Ω load is illustrated in Fig. 5.7 (a). Fig. 5.7 (b) and (c) show the eye diagrams of the optical receiver at the input and output of the measured high-speed PCB trace channel model at 10 Gb/s, respectively, while the IAFB loops are disabled. The results demonstrate that the equalization provided by the main amplifier effectively compensates for channel losses and improves both the vertical and horizontal eye openings. Enabling the IAFB mitigates the overequalization seen in Fig. 5.7 (d), resulting in the improved eye diagram of Fig. 5.7 (c), but at the cost of a smaller VEO.

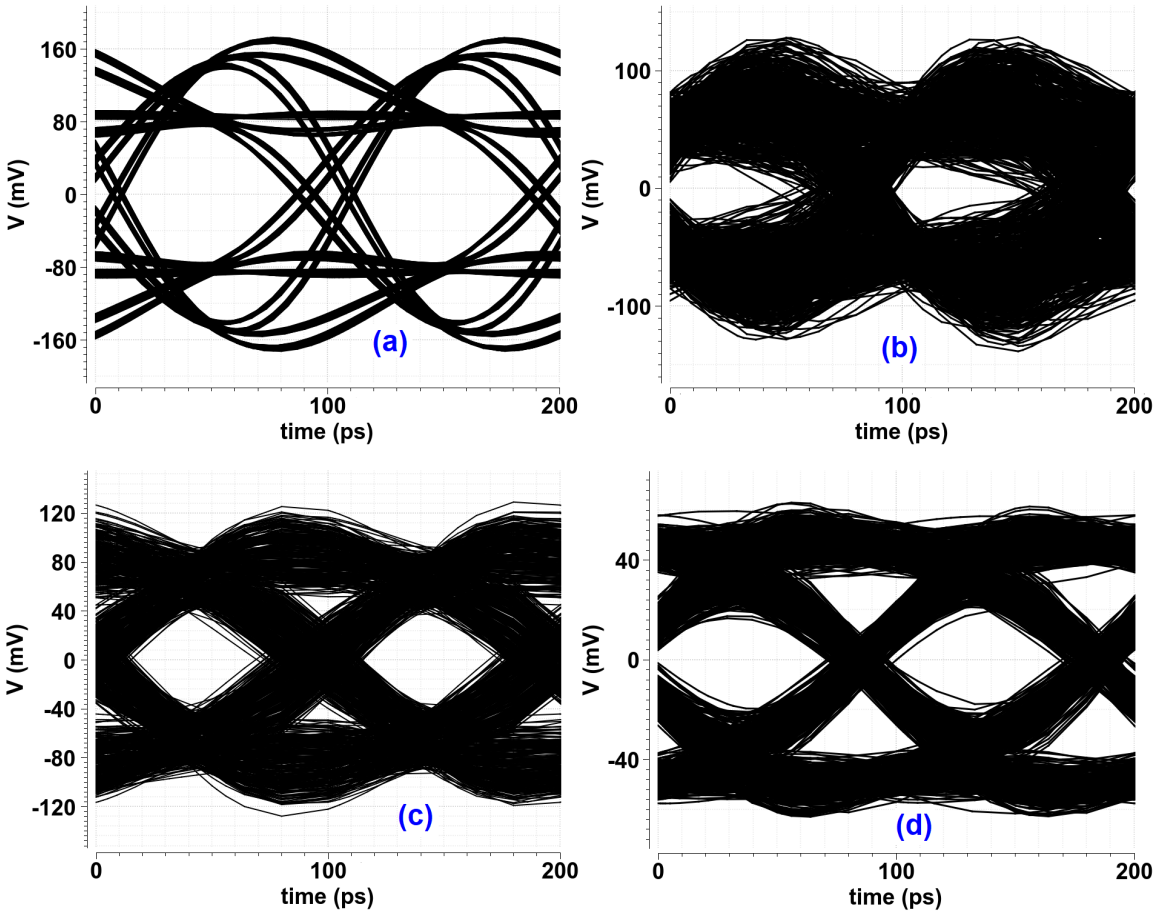


Figure 5.7: NRZ eye diagram of the proposed optical receiver at 10 Gb/s data rate in post-layout simulation a) when driving a 50 Ω load, b) at channel's input, c) at channel's output, and d) at channel's output when the IAFB is enabled.

The PAM-4 eye diagram of the optical receiver at 10 Gb/s, captured at the output of the transmission line model, is shown in Fig. 5.8. The RLM of this eye diagram is 0.98, and the THD at an output swing of 285 mV_{pp} is 1.28%. As discussed earlier, enabling the IAFB loops improves the linearity of the optical receiver and reduces the THD to 0.72% at the same output swing. However, this comes at the cost of weaker equalization and smaller eye openings due to the reduced HFP.

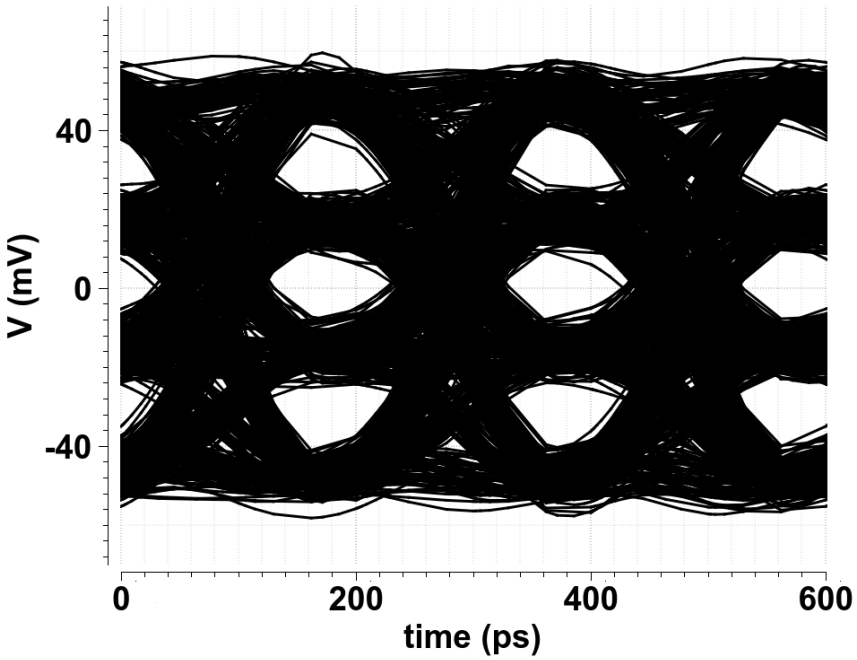


Figure 5.8: PAM-4 eye diagram of the proposed linear optical receiver in post-layout simulation at 10 Gb/s at the output of the measured high-speed PCB trace channel model.

Under very high-loss channel conditions [30], the proposed design is capable of generating an NRZ eye diagram at 5 Gb/s with a VEO of 58 mV, as shown in Fig. 5.9 (b), when the 20 kΩ R_h resistors are enabled. Fig 5.9 (a) illustrates the NRZ eye diagram of the circuit when only driving a 50 Ω load at the same data rate.

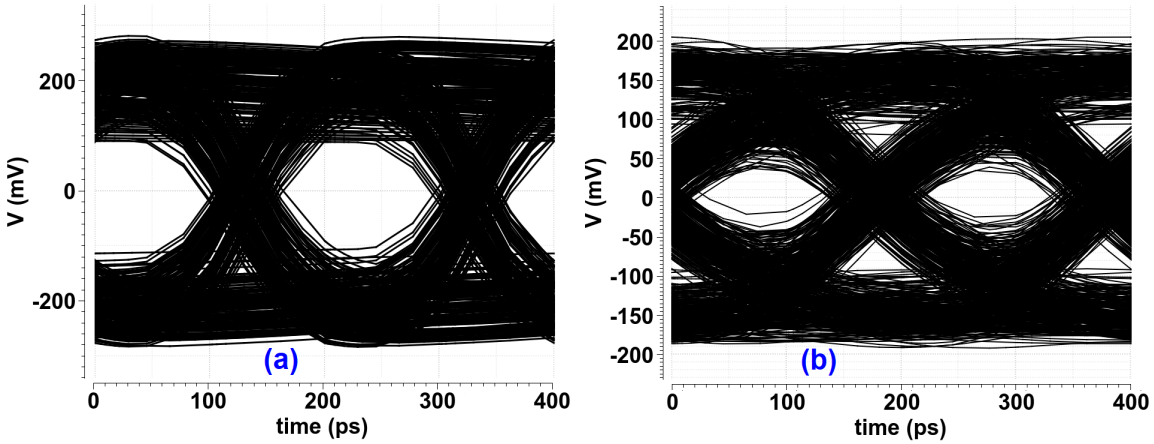


Figure 5.9: NRZ eye diagram of the proposed optical receiver at 5 Gb/s in post-layout simulation a) when driving a 50 Ω load, b) at the output of the very high-loss channel.

The device dimensions and component values used for 10 Gb/s operation in 65 nm CMOS technology are summarized in Table 5.1. As outlined in Section 3.2.1, a PMOS-to-NMOS width ratio of 2.5 is maintained throughout all segments of the circuit.

Table 5.1: Device Dimensions and Component Values in the 4-Channel Optical Receiver Design.

Circuit	**TIA**		**Main Amplifier**		**Feedback Loops**		**CC-inverters**
Component	W_{NMOS}	R_{TIA}	W_{NMOS} transconductor	W_{NMOS} load	W_{NMOS}	R_h	W_{NMOS}
Value	10 μm	190 Ω & 290 Ω	10 μm	3 μm	1.1 μm	400 Ω & 20 kΩ	2 μm

5.2.3 Chip Floorplan of the 4-Channel Optical Receiver

Fig. 5.10 shows the layout of the complete 4-channel optical receiver, including the pad ring and seal ring. As illustrated, the main analog front-end occupies a small portion of the chip. The total chip area is 2 mm^2. The layout includes 16 I/O pads, with each differential signal pair placed between two GND pads to enhance isolation and minimize coupling. Additionally, four pads are allocated for the shift register to control the T-gates, along with four VDD pads and four GND pads for power distribution.

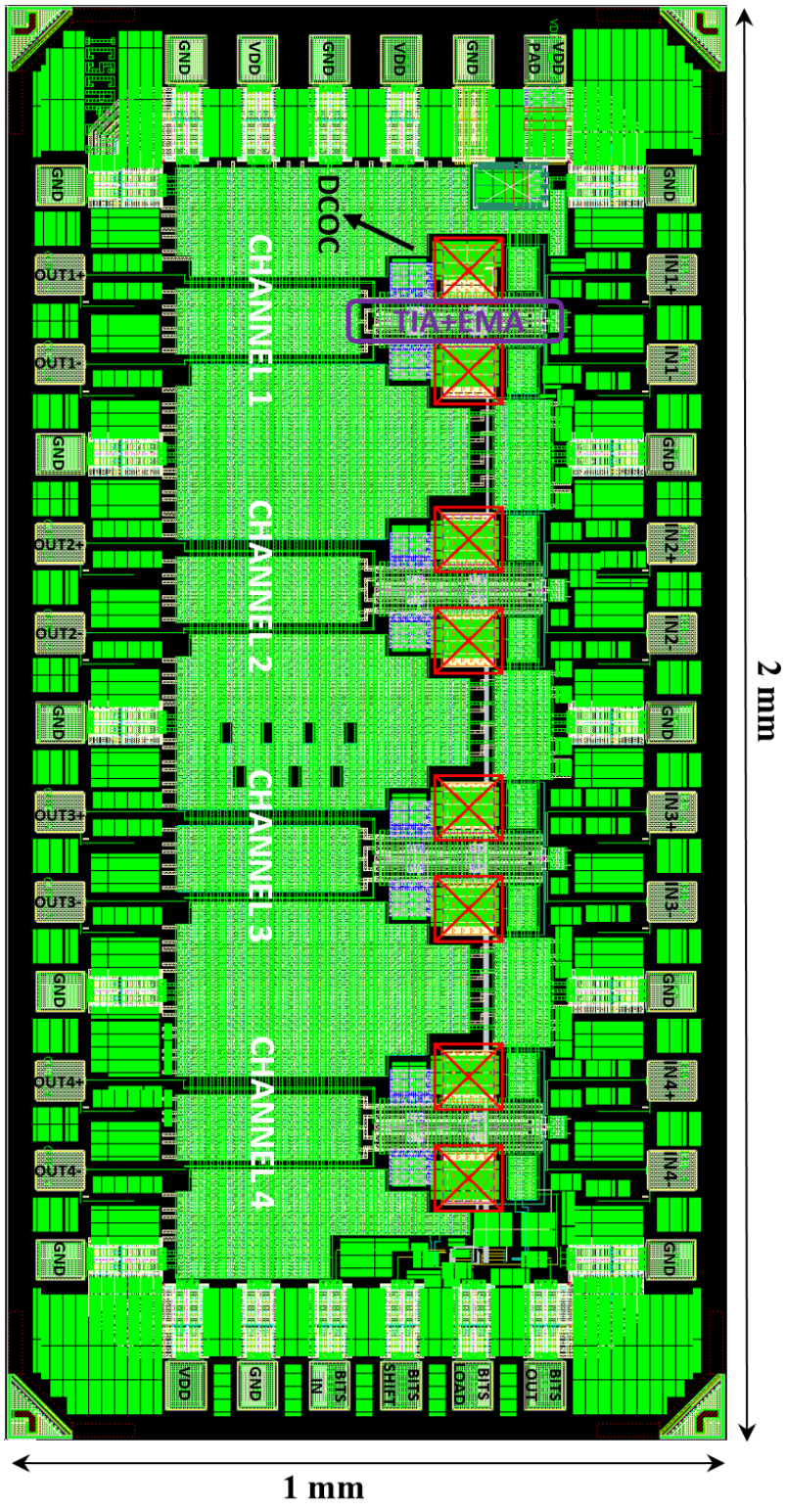


Figure 5.10: Complete layout of the proposed 4-channel optical receiver with I/O pads and a seal ring.

5.2.4 Fabricated Chip in 65 nm CMOS Technology

Fig. 5.11 shows the high-speed PCB designed for electrical measurements, with the fabricated chip of the proposed 4-channel linear optical receiver wire-bonded to it. The measurement process is in its early stages, and the results will be presented in a future publication.

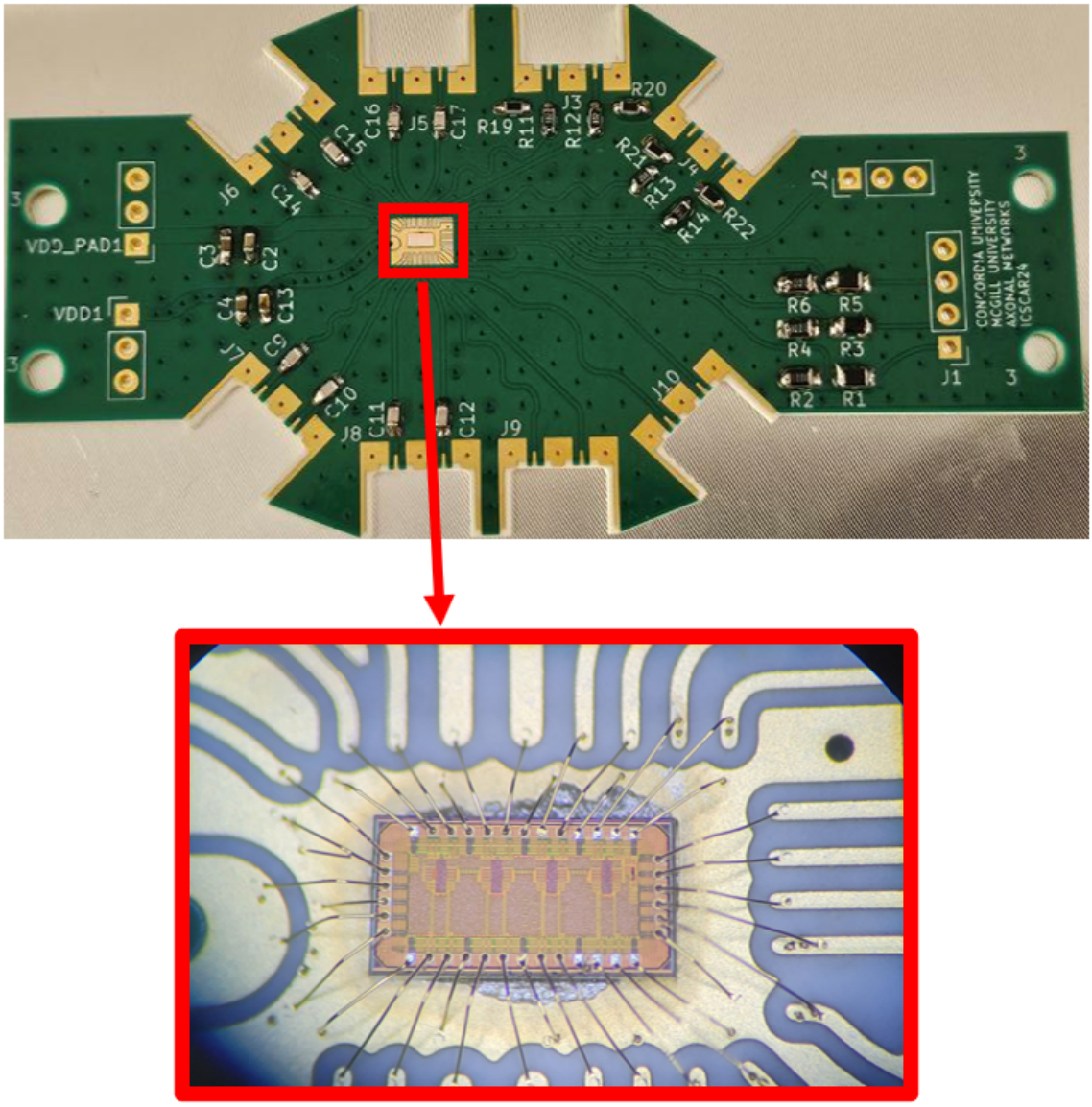


Figure 5.11: Fabricated chip of the proposed 4-channel linear optical receiver wire-bonded onto the designed high-speed PCB for electrical measurements.

5.3 Conclusion

In this chapter, the design process of the proposed 4-channel differential optical receiver with equalizing main amplifier, from layout to fabrication, was presented. A fully differential architecture was achieved using cross-coupled inverters and a fully-differential photodiode structure. Post-layout simulation results, including the effects of the transmission line model, were discussed. The fabricated chip occupies an area of 2 mm × 1 mm and consumes approximately 30 mW of power per channel in post-layout simulation. The design supports data rates of 10 Gb/s per channel in both NRZ and PAM-4 formats.

Chapter 6

Comparison and Conclusion

6.1 Comparison of the Proposed Optical Receiver

This section presents a comparison between the proposed optical receiver and other state-of-the-art designs reported in the literature. It should be noted that the performance metrics of the proposed design are based on post-layout simulations, as chip measurements are still in progress. In contrast, most published works report measured results. Although this limits the direct comparability of certain parameters, the post-layout simulations account for extracted parasitics and provide a realistic estimate of post-fabrication performance. Furthermore, it is important to consider the impact of technology scaling, as many recent high-performance designs are implemented in more advanced nodes, such as BiCMOS, FinFET, or sub-65 nm CMOS technologies. These platforms offer significant advantages in speed, linearity, and power efficiency, which must be taken into account when evaluating the proposed 65 nm CMOS design.

In most optical receivers, passive inductors are commonly employed for bandwidth extension [5, 12, 13], and an additional stage of CTLE is typically introduced to compensate for channel losses [36, 37]. In contrast, the proposed design employs negative active feedback loops to enhance bandwidth and integrates the equalization functionality directly into the main amplifier. This eliminates the need for both inductors and additional CTLE stages, resulting in two key benefits: (1) lower power consumption (31.2 mW/channel) compared to most prior works, and (2) a smaller chip area (1 mm $\times$ 2 mm for four channels) relative to other four-channel designs such as [12], which

occupies 1.785 mm × 3.285 mm.

Recent designs implemented in more advanced technology nodes, such as 16 nm FinFET [5], 22 nm FDSOI [12], and 28 nm CMOS [13], benefit from higher bandwidths primarily due to the reduced parasitic capacitances of smaller transistors. In contrast, the proposed optical receiver, despite being fabricated in a relatively older 65 nm CMOS technology, achieves strong linearity performance, with a THD of 2.3% at a 400 mV_{pp} output swing. This suggests that applying the same design methodology, particularly the use of negative active feedback in the g_m/g_m-based structure and integrated equalization, in a more advanced node could yield even greater performance improvements in terms of bandwidth, linearity, and power efficiency.

Table 6.1 provides a performance summary and comparison of the proposed linear optical receiver with state-of-the-art designs, highlighting its competitive linearity and power efficiency.

Table 6.1: The Performance Comparison and Summary

Reference	[5]	[14]	[13]	[37]	[12]	**This work**
Technology	16 nm FinFET	130 nm BiCMOS	28 nm CMOS	40 nm Bulk CMOS	22 nm FDSOI	65 nm CMOS
BW extension/ Equalization Technique	Passive inductors	Negative impedance converter (NIC) CTLE	Passive inductors	Passive inductors/ CTLE	Passive inductors	3rd-order IAFB/ Equalizing main amplifier
Linearity Technique	g_m/g_m amplifiers	Emitter degeneration	Variable Gain Amplifier	Tunable gain	Overload mitigation circuit	g_m/g_m amplifiers
Data rate (Gb/s per Channel)	106.25 (PAM-4)	112 (PAM-4)	up to 200	50 (PAM-4)	106.25 (PAM-4)	10 (NRZ/PAM-4)
Transimpedance Gain (dBΩ)	78	70	78	66	74	Low frequency: 79.7 High frequency: 84.4
Bandwidth (GHz)	27	37∼48	42	23.4	28	6.7
THD (%)	< 2 @ 600 mV$_{pp}$	< 5 @ 600 mV$_{pp}$	1.77 @ 500 mV$_{pp}$	< 3 @ 400 mV$_{pp}$	< 2.5 @ 550 mV$_{pp}$	2.3 @ 400 mV$_{pp}$
Noise (pA/$\sqrt{\text{Hz}}$)	16.7	19.8	18	10.12	11	19.7
Power Consumption (mW per Channel)	60.8	254	319	125.4	155	31.2
Power Consumption (pJ/bit)	0.57	2.27	1.6	2.51	1.46	3.12
Chip Area (mm x mm)	1.24 x 1.16 (single channel)	1.5 x 1 (single channel)	1 x 1 (single channel)	1.7 x 1.1 (dual-channel)	3.285 x 1.785 (four-channel)	2 x 1 (four-channel)
Result Type	Measurement	Measurement	Measurement	Measurement/ Post-layout simulation	Measurement	Post-layout simulation

6.2 Conclusion

This thesis presented the design and analysis of a linear and power-efficient optical receiver front-end for high-speed NRZ and PAM-4 signaling, implemented in a 65 nm CMOS technology.

The primary focus was on enhancing linearity and equalization while maintaining low power consumption and compact chip area.

In the first part of the work, a highly linear main amplifier was proposed based on a g_m/g_m topology combined with IAFB. Simulation results demonstrated that, compared to the conventional CH amplifier, the proposed configuration offers improved bandwidth, linearity, and VEO at the same input swing. To the best of the author's knowledge, this is the first implementation of an IAFB-based topology using inverter-based amplifiers. In addition, a method for improving linearity was introduced by reducing the input voltage of the feedback inverters through resistive voltage dividers and increasing the feedback gain. This approach addressed the limitation of IAFB circuits in maintaining linearity at lower input voltages. Simulations confirmed that the proposed method resulted in approximately a 67% reduction in THD at an output swing of 500 mV_{pp}.

The second part of the work focused on integrating equalization directly into the main amplifier through a nested active feedback structure. A high-frequency pole was introduced in the feedback loop using a resistor, enabling effective equalization without relying on passive inductors or an additional CTLE stage. This design choice resulted in reduced chip area and power consumption while maintaining sufficient gain and bandwidth, making it suitable for compact and energy-efficient optical receiver systems.

The final part of the thesis detailed the design and layout of a four-channel differential optical receiver incorporating the proposed equalizing linear main amplifier. A fully differential architecture was realized using cross-coupled inverters and differential photodiodes. Post-layout simulations, including transmission line modeling, showed that the receiver supports 10 Gb/s data rates per channel in both NRZ and PAM-4 formats. The fabricated chip occupies an area of 2 mm × 1 mm and consumes approximately 30 mW per channel based on post-layout simulation results.

Overall, the proposed design demonstrates competitive performance in terms of linearity, equalization, and power efficiency, despite being implemented in a relatively older 65 nm CMOS technology. The techniques presented in this work are scalable and could potentially yield enhanced performance when applied in more advanced technology nodes, such as FinFET, BiCMOS, or sub-65 nm CMOS processes.

6.3 Future Works

While this thesis has demonstrated the effectiveness of the proposed main amplifier architecture through post-layout simulations, several opportunities remain for further investigation and enhancement. Future work can focus on:

- Experimental validation, both electrical and optical, to ensure the receiver's robustness and efficiency in real-world high-speed optical communication systems. This includes verifying the linearity (THD, RLM), bandwidth, power consumption, and equalization capabilities under realistic operating conditions. Measurement results will provide deeper insight into the impact of parasitic effects, process variation, and layout-induced mismatches.

- Enhanced equalization and adaptivity for PAM-4 signaling at data rates exceeding 10 Gb/s. While the current design demonstrates strong equalization performance for NRZ, its effectiveness for PAM-4 at higher speeds is limited due to narrower eye openings and greater sensitivity to parasitic effects. These limitations could be mitigated through layout optimization to reduce coupling and interconnect capacitance, which become increasingly critical at higher data rates. Furthermore, future designs could incorporate programmable gain amplifiers (PGAs), digitally configurable feedback paths, and on-chip calibration circuits to enable real-time adaptation of gain and peaking in response to varying channel conditions and to improve robustness against process, voltage, and temperature (PVT) variations. For example, [5] presents a dynamic voltage scaling (DVS) scheme that allows precise control over bandwidth and peaking under aggressive bandwidth extension. In [13], three variable gain amplifiers (VGAs), each comprising a complementary transconductor followed by a Gilbert cell, are employed to maintain signal integrity and linearity across different gain settings. The Gilbert cell enables 12 dB of gain control with improved linearity at low gain, while the complementary structure reduces load current for a given transconductance.

- Improving noise performance. Since this thesis primarily focused on the design of a linear and equalizing main amplifier, future work could investigate techniques aimed at reducing the output noise, thereby enhancing the overall sensitivity of the optical receiver. While conventional

shunt-feedback TIAs are widely regarded as offering the best gain-noise trade-off, their performance is fundamentally limited by the inverse relationship between gain, bandwidth, and noise. To overcome these limitations, some studies have proposed architectures that optimize the overall front-end noise performance without compromising sensitivity. For example, [38] demonstrates a high-sensitivity optical receiver using a high-gain, low-bandwidth multistage shunt-feedback TIA cascaded with a four-tap finite impulse response (FIR) decision feedback equalizer (DFE) to mitigate ISI. In a different approach, [12] addresses the linearity-noise trade-off by introducing an overload mitigation circuit with a variable input resistor and a dummy TIA, which redirects excess current without affecting the phase response.

Appendix A

High-speed PCB Design

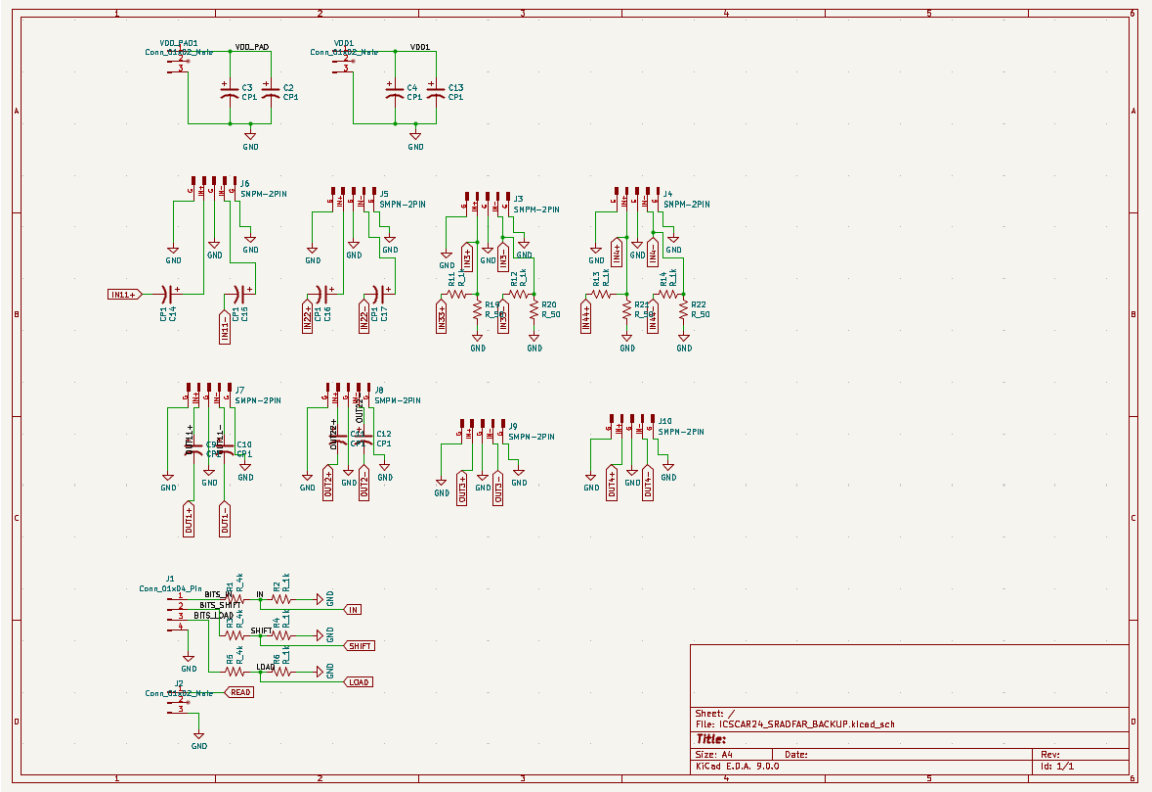


Figure A.1: High-speed PCB KiCad schematic.

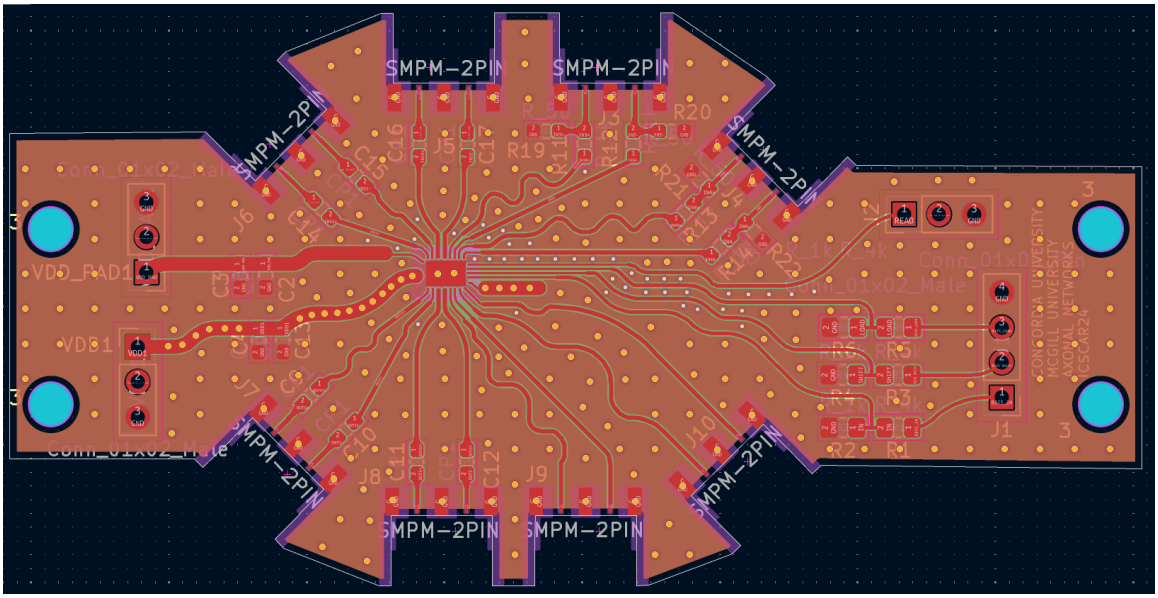


Figure A.2: High-speed PCB KiCad design.

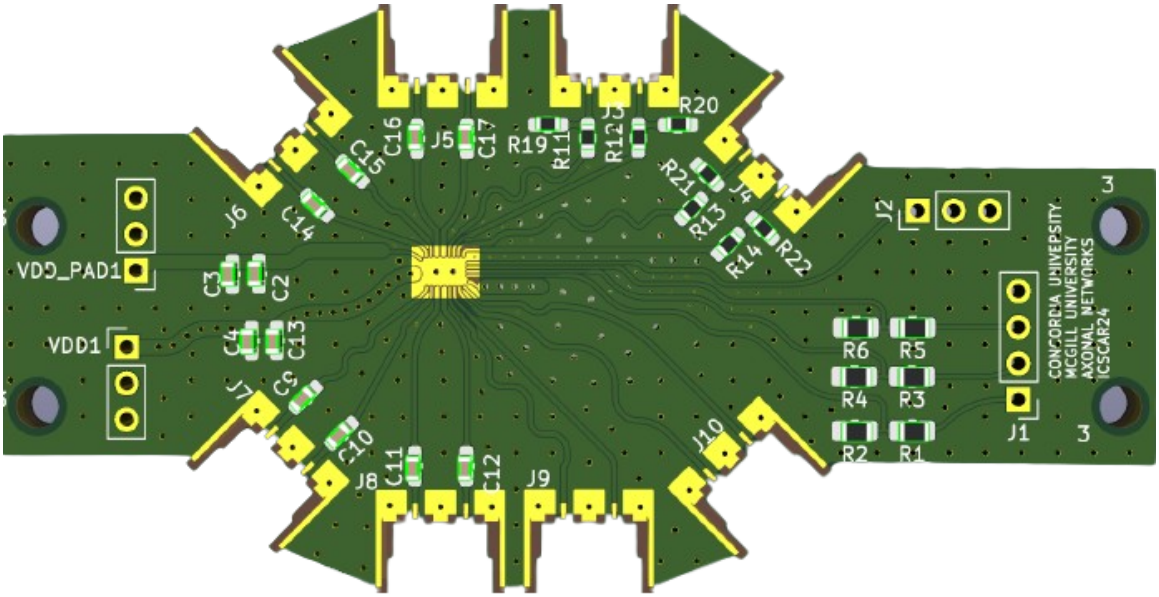


Figure A.3: High-speed PCB KiCad 3D design.

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