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A LINE AND LOAD INDEPENDENT ZERO VOLTAGE SWITCHING DC/DC FULL BRIDGE CONVERTER TOPOLOGY

Wen Kang

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In

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ABSTRACT

A line and load independent zero voltage switching dc/dc full bridge converter topology

Wen Kang

Full bridge dc/dc converter topology is extensively applied in medium to high power conversion. In a power level up to 3 kW, the full bridge converter now employs MOSFET switches. High efficiency, high power density, high reliability and low EMI are some of the most desirable features in these applications, particularly for computer and telecom systems.

To achieve these features, soft switching techniques are normally employed. However, the conventional soft switching full bridge converter topologies would either lose the soft switching at some operating conditions, or become rather complex in design and implementation for a few kilo watts applications.

This thesis presents and analyzes an improved zero voltage switching dc/dc full bridge converter topology. The proposed topology employs asymmetrical auxiliary circuits that consist of only a few passive components. However, the advantage of the proposed topology is significant: it achieves soft switching independent of line and load conditions.

Detailed steady state and dynamic analyses are performed to understand the operating principle of the proposed topology and its performance. A dc blocking capacitor is essential to prevent the current sense transformer from saturation, and the study of this thesis shows that contrary to the conventional pulse width modulated full bridge converter, the peak current mode control can still be used along with the blocking capacitor in a phase shift full bridge converter. Design procedure for industrial application is presented. Experimental and simulation results of a prototype 500 W 350-400 Vdc to 55 Vdc converter operating at 100 kHz verify the analysis and design, and show an overall efficiency of greater than 97% at full load.

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LIST OF ACRONYMS

AC	Alternative Current
ACMC	Averaged Current Mode Control
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductor
ESR	Equivalent Series Resistor
FB	Feedback
IGBT	Isolated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCMC	Peak Current Mode Control
PWM	Pulse Width Modulation
rms, RMS	Root Mean Square value
VMC	Voltage Mode Control
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

LIST OF PRINCIPAL SYMBOLS

Δ_+ and Δ_-	positive and negative voltage pulse width, respectively
θ	phase shift angle expressed in fraction of a switching cycle period
C_{a1} and C_{a2}	auxiliary circuit input voltage splitter capacitors
C_o	output filter capacitor
C_s	dc component blocking series capacitor
C_{sb1}, C_{sb2}, C_{sb3}, and C_{sb4}	snubber capacitors for each of the four switches, respectively
D_1, D_2, D_3 and D_4	individual duty ratio of the four switches, respectively
D_{o1} and D_{o2}	two output rectifier diodes of the full bridge converter
D_R	duty ratio of the output rectifier diodes
d_1, d_2, d_3 and d_4	individual switching dead time of the four switches respectively
f_s	switching frequency
I_{La1} and I_{La2}	peak value of the current through the two auxiliary inductors L_{a1} and L_{a2}, respectively
I_{Lopeak} and $I_{Lovalley}$	peak and valley values of the current through the output inductor L_o, respectively
I_o	nominal output current
i_{ds1}, i_{ds2} i_{ds3} and i_{ds4}	instantaneous drain current of the four switches, respectively
i_p	instantaneous primary current of the power transformer
k	turns ratio of the power transformer primary to secondary windings
L_{a1} and L_{a2}	auxiliary circuit inductors

L_o	output filter inductor
P_o	output power of the converter
S_1, S_2, S_3, and S_4	four switches of the full bridge converter
s	Laplace transform variable
T_r	power transformer
T_s	switching cycle period
t	time variable
t_d	switching dead time
u_{ds1}, u_{ds2} u_{ds3} and u_{ds4}	instantaneous drain to source voltage of the four switches, respectively
V_d	nominal input dc voltage
V_{dc}	dc bias voltage
V_o	nominal output voltage
v_c	instantaneous voltage of the dc blocking capacitor C_s
v_o	instantaneous output voltage

CHAPTER 1

INTRODUCTION

1.1 General Introduction

Full-bridge dc/dc converters are extensively used in medium to high power level applications. For most of these applications, particularly those for the computer and telecommunication systems, the most desirable features of the converter are high efficiency, high power density, high reliability and low Electro-Magnetic Interference (EMI).

Unfortunately, the standard full bridge topology operates in hard switching, and the hard switching converter is unable to achieve high efficiency and high power density for the following reasons: in order to achieve high power density, the switching frequency is normally increased, because at increased frequencies, the converter can employ smaller sized power magnetics and capacitors, both of which are the largest devices of a power converter. However, as the switching frequency increases, the switching losses associated with the turning on and off of switches will become excessive. These losses greatly reduce the converter's overall efficiency, and high power density is not achievable due to the resultant high cooling requirements.

To solve these problems, soft switching techniques are normally used. Basically there are two types of the soft switching techniques: Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). Either of the techniques can greatly reduce and even completely eliminate the switching losses in the converter. However, it is well understood that ZVS is more advantageous for a MOSFET switch topology than the ZCS.

High power level full bridge converters usually use IGBT switches, due to IGBT's low

conduction losses and higher power capability. However, IGBT is not as fast as MOSFET, and its switching frequency can not be increased beyond 50 kHz even if softly switched. Contrary to IGBT, MOSFET is a resistive device when it is turned on, and the conduction losses are higher as compared to IGBT at high power levels. However, MOSFET is a faster device and is able to operate up to a few MHz.

As mentioned before, the approach to achieve high power density is to operate the converter at a higher switching frequency. For power levels up to 3 kW, the full-bridge converters now employ MOSFET switches. In most of these converters, ZVS is used to increase the overall efficiency and alleviate the thermal problems. However, in the following section, it will be seen that these converters lose ZVS under some operating conditions, causing potential thermal problems and lowering the reliability of the converter.

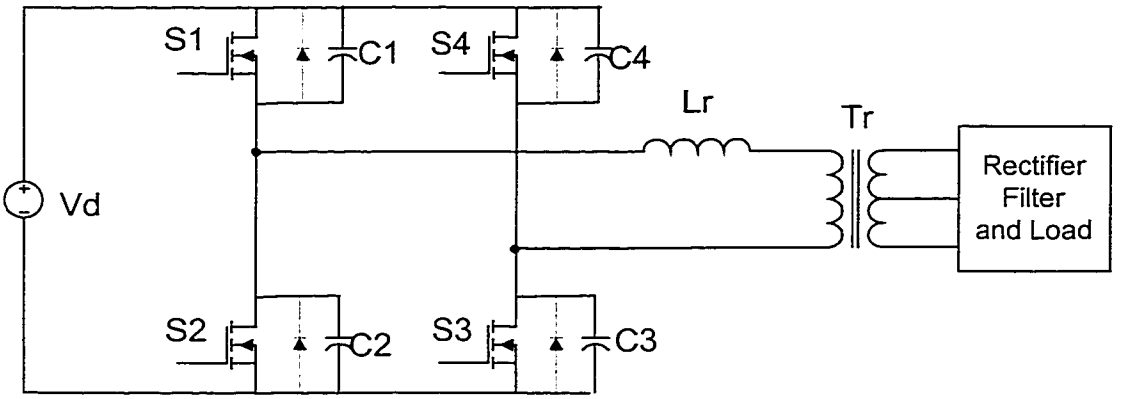
1.2 Review of Existing ZVS Full Bridge Topologies

1.2.1 ZVS full bridge topologies with passive mechanism

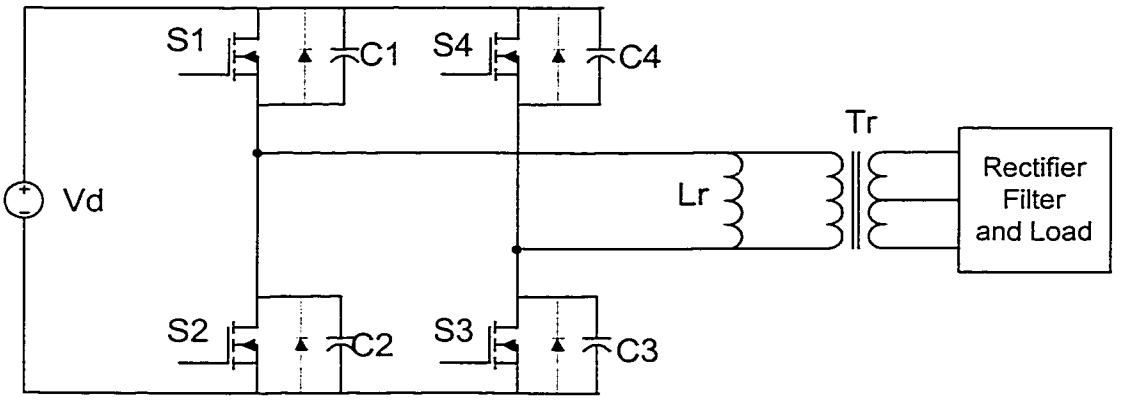
Fig. 1.1 shows two typical full bridge topologies that achieve ZVS with passive components [1-7]. In Fig. 1.1a, ZVS is achieved by placing an inductor in series with the power transformer, while in Fig. 1.1b it is achieved by placing an inductor in parallel with the power transformer. In both topologies, a snubber capacitor is placed across each switch. In a practical configuration, the series inductor may be the leakage inductor of the power transformer, the parallel inductor may be the magnetizing inductor of the power transformer, and the snubber capacitor may be the inherent drain-to-source capacitor of the MOSFET switch. Addition of only one component to the full bridge converter makes these topologies the simplest.

The basic operating principles to achieve ZVS in these two topologies are as follows.

(i) ZVS turn-off is achieved by holding the drain-to-source voltage of the MOSFET at zero or very low during the turn off transient. This is accomplished by the snubber capacitor. At turn-off, the snubber capacitor significantly slows down the rate of rise of the drain to source voltage of the pertinent switch. In this way, the overlap between the decreasing drain current and rising drain-to-source voltage of each switch is greatly reduced, or even completely eliminated, and so are the switching losses.



a. ZVS topology with series inductor



b. ZVS topology with parallel inductor

Fig. 1.1 ZVS full bridge converter topologies using passive devices.

(ii) ZVS turn-on is achieved by completely discharging the snubber capacitors of the switches before they are turned on. During the dead time of the gating of the bridge switches, the discharging of the snubber capacitors is made possible by the residual current in the series inductor in the topology of Fig. 1.1a, or the parallel inductor in the topology of Fig. 1.1b.

In comparison of these two topologies in Fig. 1.1, the one with the series inductor can achieve ZVS even when there is a short circuit (or over loading) across the load, while the other one that has the parallel inductor maintains ZVS operation even when there is an open circuit (or no load) across the output terminals. Both topologies are simple. However, both of them suffer from their own shortcomings.

The drawbacks of the topology with series inductor (Fig. 1.1a) are:

(i) Loss of ZVS at no load or light-load. This is because the complete discharge of snubber capacitors depends on the stored energy in inductor L_r and the energy is proportional to the square of the peak value of the primary current. When the load is light, the primary current is low, and consequently the stored inductor energy is also low. This energy is not sufficient to deplete the snubber capacitor in the dead time. Thus, ZVS is lost at turn-on.

(ii) Reduction of the effective duty ratio because of the voltage drop on the series inductor. This results in higher primary current and conduction losses of the switches.

The drawbacks of the topology with parallel inductor (Fig. 1.1b) include the following.

(i) Loss of ZVS under over load or short-circuit conditions. This is because, when the output terminals have a short circuit, the large load current, when it is reflected into the primary side, overrides the parallel inductor current and cancel its function to achieve ZVS.

(ii) Increased conduction losses and reduced efficiency at light load. This is because the

circulating current flowing along the parallel inductor, switch and the input dc line is almost independent of the load level. At light load, the circulating current becomes significant compared to the load current, and this remarkably increases the total conduction losses at light load.

It is seen that, both topologies lose ZVS under certain operating conditions. The loss of ZVS results in the following problems: (i) increased size of heat sink due to switching losses, (ii) higher EMI due to high di/dt of the snubber discharging current when the switch is turned on, and (iii) reduced reliability due to reverse recovery current of the body diodes.

1.2.2 Soft switching full bridge topologies with active mechanism

Fig. 1.2 shows a soft switching full bridge topology with active components [6-13]. It employs two symmetrical auxiliary circuits, each of which is controlled through an auxiliary bi-directional switch. In order to control the current through the auxiliary inductors, each bi-directional switch must be implemented by using two anti-paralleled unidirectional switches. By proper timing, the current building up in the auxiliary inductor discharges the snubber capacitor of the pertinent switch to achieve its ZVS turn-on, or overcomes the tail current of the pertinent switch to achieve ZCS turn-off. Soft switching can be achieved under all operating conditions, thereby overcoming the aforementioned drawbacks existing in the topologies shown in Fig. 1.1. Specifically, it achieves soft switching even under both extreme operating conditions, namely no load and output short circuit conditions, and there is no reduction of the effective duty ratio.

The topology in Fig. 1.2 is originally developed for high power full-bridge converters using IGBTs. For lower power level applications, when MOSFETs are used, the topology of Fig. 1.2 is directly converted into Fig. 1.3.

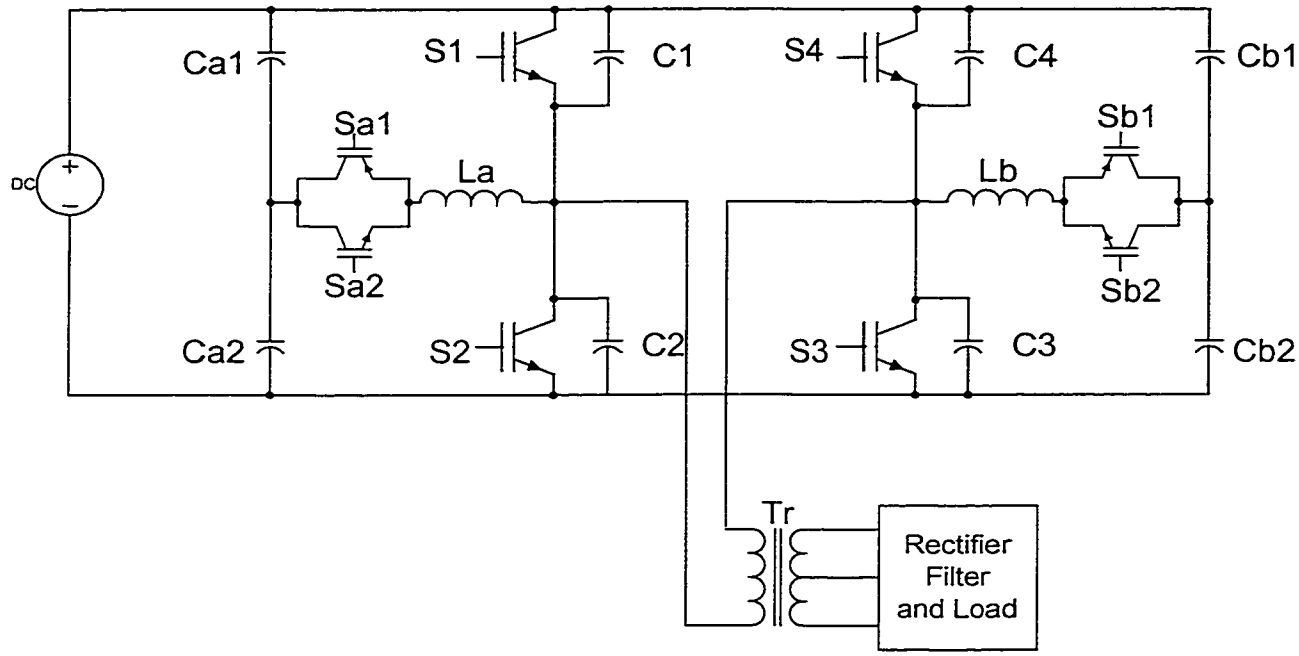


Fig. 1.2 Soft switching full bridge converter IGBT topology using active auxiliary circuits.

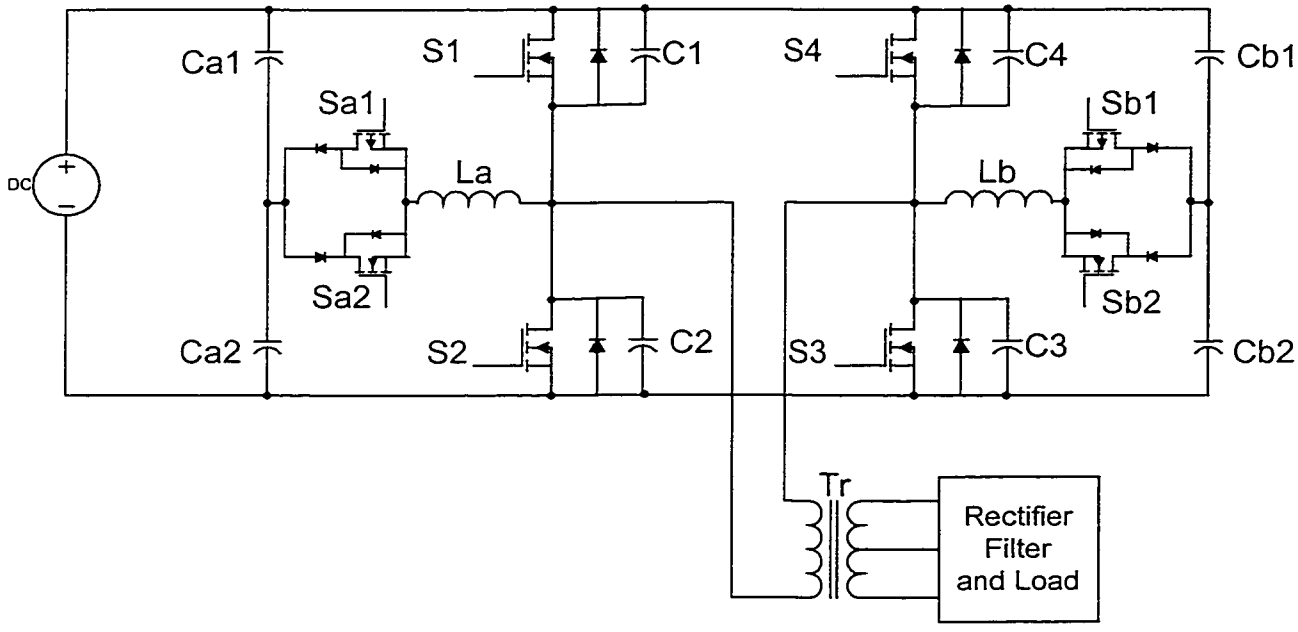


Fig. 1.3 ZVS full bridge converter MOSFET topology using active auxiliary circuits based on the original IGBT topology in Fig. 1.2.

As seen from Fig. 1.3, each unidirectional switch in the auxiliary circuit requires an additional fast speed diode in series with a MOSFET. The topology becomes rather complicated and costly for low power level applications. Simplified ZVS topologies shall be developed to overcome these problems.

1.3 Objectives and Scope of the Study

The objectives of the study are as follows:

(i) Presenting a simplified but improved ZVS full bridge topology,

(ii) Characterizing the proposed topology for industrial applications,

(iii) Generating the design procedure.

The scope of this thesis is limited within the following frame:

(i) Steady state analysis,

(ii) Averaged state space small signal analysis,

(iii) Concept verification through simulations performed in Pspice and Psim, and

(iv) Experimental results of the prototype converter.

1.4 Thesis Outline

The thesis is organized in the following structure.

In Chapter 2, the proposed topology is presented, and the steady state analysis is performed to understand its steady states characteristics and properties. Simulation and experimental results are also presented as proofs of concept.

In Chapter 3, the proposed topology under dynamic conditions is analyzed, including the effects of the asymmetry in gating patterns of the full bridge switches, protection of the current

sense transformer from saturation, and the small signal model of the proposed topology. It also points out that with phase shift Pulse Width Modulation (PWM) technique, the Peak Current Mode Control (PCMC) can still be used along with the dc blocking capacitor that is employed to prevent the current sense transformer saturation. Compensation of the feedback loop to dynamically stabilize the converter is also discussed.

In Chapter 4, asymmetrical auxiliary circuits are suggested to optimize the converter performance, and a design procedure oriented for industrial applications is generated based on the analysis performed in the previous chapters. A design example is also given.

Conclusions of the thesis work are drawn in Chapter 5, followed by suggestions for future work.

CHAPTER 2

PROPOSED ZVS CONVERTER TOPOLOGY AND THE STEADY STATE ANALYSIS

2.1 Introduction

An improved line and load independent ZVS full bridge converter topology is presented in this chapter. This topology is simply a combination of a conventional full bridge converter and an auxiliary circuit that consists of a few passive components. However, the advantages of the topology are remarkable: (i) it achieves ZVS independent of the line and load conditions, and the power circuit as well as its control is just that of the conventional full bridge converter, (ii) ZVS independent of line and load conditions results in smaller heatsinks for the switches and also the capability of operating the converter at high frequency, (iii) the design of the converter can follow the well understood and well developed procedure to facilitate industrial application.

To better understand the operating principle and performance characteristics of the proposed topology, and to provide reference in optimal design procedure in Chapter 4, a detailed steady state analysis is performed in this chapter.

In this chapter, the proposed topology is presented in Sec. 2.2. The steady state analysis is performed in Sec. 2.3. Simulation results are shown in Sec. 2.4, followed by the conclusions.

2.2 Circuit description

Fig. 2.1 shows the proposed ZVS full bridge converter topology. It consists of two functional sub-circuits. One sub-circuit is a conventional full bridge converter, which is referred to as the power circuit hereafter. The other is the auxiliary circuit shown in the shaded area.

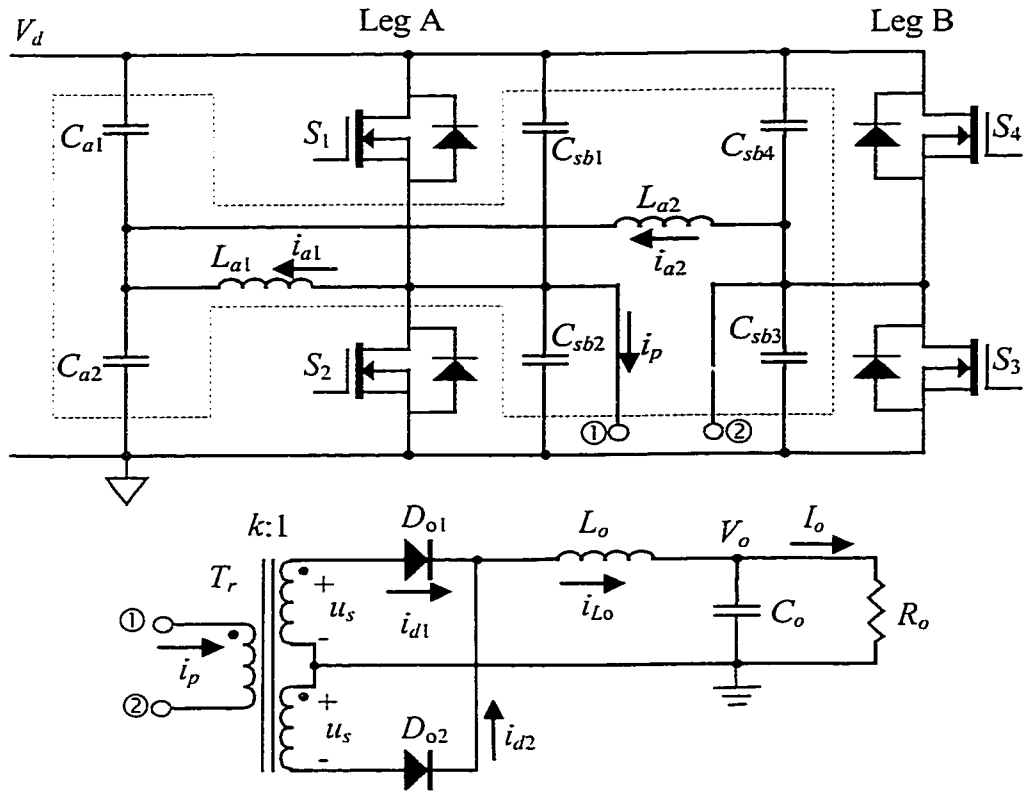


Fig. 2.1 The proposed ZVS full bridge converter topology.

The power circuit employs the following devices: (i) S_1, S_2, S_3, and S_4, four MOSFET switches, (ii) T_r, the power transformer with a turns ratio of k, (iii) D_{o1} and D_{o2}, two rectifier diodes, (iv) L_o and C_o, the output filter, and (v) R_o, the load.

The auxiliary circuit is comprised by eight passive devices, i.e., (i) C_{sb1}, C_{sb2}, C_{sb3}, and C_{sb4}, four drain-to-source snubber capacitors, each connected across one switch, (ii) C_{a1} and C_{a2}, a capacitor voltage divider, and (iii) L_{a1} and L_{a2}, two auxiliary inductors.

Phase shift PWM is used as the control technique to regulate the output voltage. The reasons for choosing the phase shift technique is to be able to use the PCMC which will be detailed in Chapter 3. For power transfer, the power circuit operates almost in the same way as does a conventional full bridge converter, and the auxiliary circuit hardly interferes with this

transfer. However, the auxiliary circuit does have significant influences on the switching transients of the switches: it simply removes the switching losses from all the switches during both turn-on and turn-off transients.

2.3 Steady State Analysis

Since conventional phase shift full bridge converters have been extensively addressed in the literature, only the operation of the auxiliary circuit will be discussed in detail in this chapter.

In the following analysis, the time varying variables such as the current and voltage of the principal components and devices are determined. Based on these variables, the performance of the converter can be illustrated, and quantities such as the root mean square (rms), average or peak current and voltage of these components can be obtained. These quantities determine the ratings of the components and they will be used in the design procedure in Chapter 4.

In the analysis presented below, a closed form solution is obtained by solving a set of differential equations in each interval and by matching the boundary conditions at the boundary of the intervals. The initial conditions are a function of the operating frequency f_s, the input line voltage V_d and the output power P_o. They can be obtained by the iterative process such as Newton-Raphson method.

2.3.1 Assumptions and some constants for the analysis

The following assumptions are made for the steady state analysis:

(i) The steady state conditions have been established and the converter is running in the Continuous Conduction Mode (CCM) at the input dc voltage V_d, producing the nominal output voltage V_o and delivering the power of P_o to a constant load.

(ii) The gating of switches on *Leg A*, namely S_1 and S_2, is leading the gating of switches on

Leg B, or S_3 and S_4, by a phase shifted angle θ (expressed as a fraction of a switching period), and θ is determined by the control circuit to regulate the output voltage,

(iii) the switching frequency is f_s,

(iv) all components and devices have ideal properties and characteristics, i.e.,

(1) T_r: losses and leakage inductance are negligible, and the core does not saturate,

(2) L_o, L_{a1} and L_{a2}: all inductors are ideal inductors with zero losses, and their inductances are constant,

(3) C_o, C_{a1}, C_{a2}, C_{sb1}, C_{sb2}, C_{sb3}, and C_{sb4}: all capacitors are ideal capacitors, their equivalent series resistance (ESR) and equivalent series inductance (ESL) are negligible, and their capacitances are constant,

(4) S_1, S_2, S_3, and S_4: all switches are ideal, having negligible conduction losses, and zero parasite capacitances,

(5) D_{o1} and D_{o2}: both diodes are ideal, having a forward voltage drop of 0 V and negligible reverse recovery time.

(6) The magnetizing inductance of the power transformer is so great that the magnetizing current is negligible.

(v) There is a very short dead time, t_d, between the ON states of the two switches on each leg of the bridge,

(vi) C_{sb1} and C_{sb2} have equal capacitance value, and so do C_{sb3} and C_{sb4},

(vii) C_{a1} and C_{a2} have equal capacitance value, and they are large enough to establish a constant and ripple free voltage during the steady state operation.

Under these assumptions, the operating principle is illustrated with key waveforms shown in Fig. 2.2. Each switching cycle can be divided into eight distinct intervals.

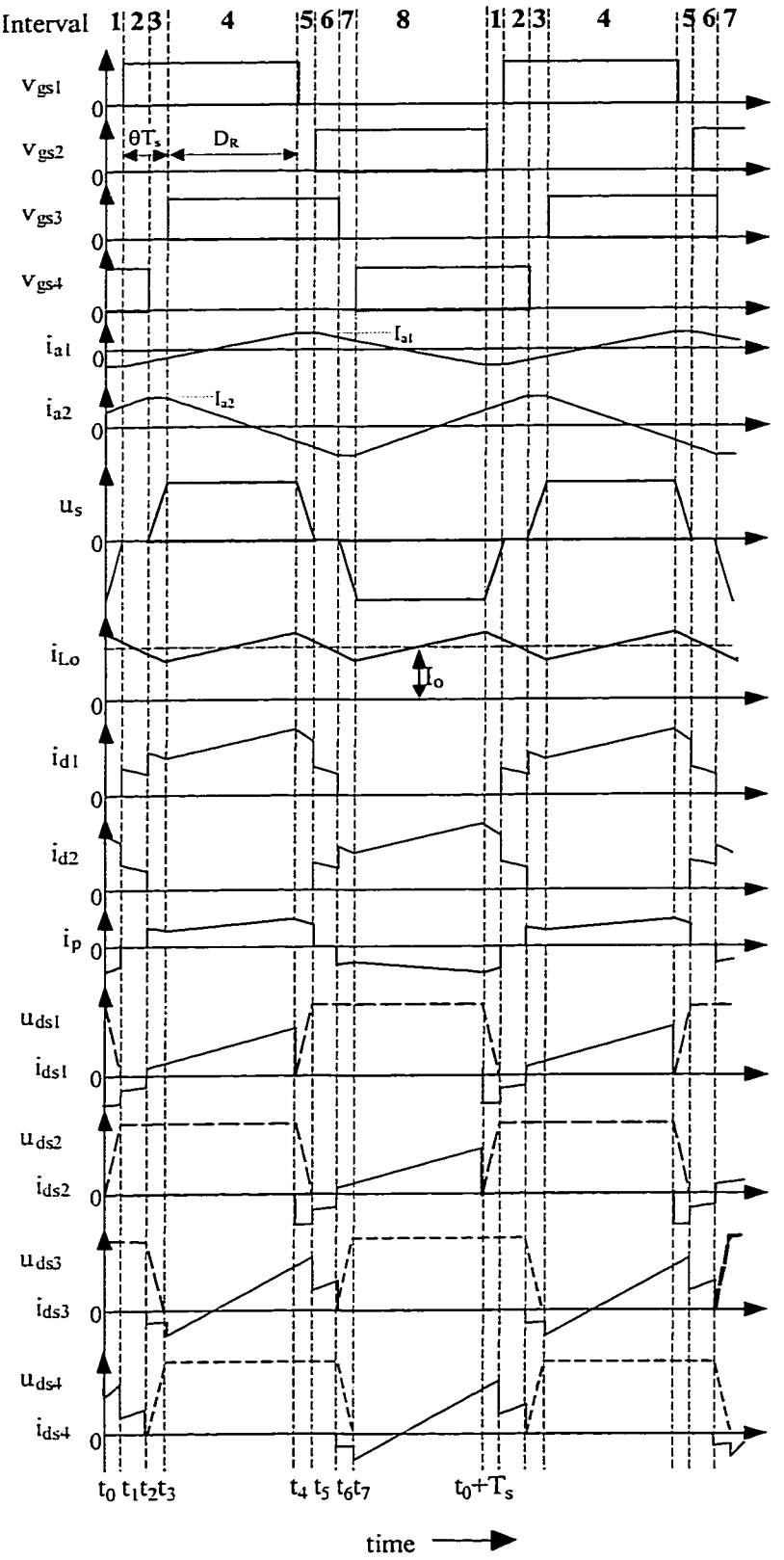


Fig. 2.2 Key waveforms of the proposed converter topology. The dead time and switching transient are exaggerated.

For convenience, the following constants used in the analysis are defined.

In steady state, the effective duty ratio D_R of each output diode is determined by

$$D_R = \frac{kV_o}{2V_d} \tag{2-1}$$

and it is also equal to

$$D_R = \frac{1}{2} - t_d f_s - \theta \tag{2-2}$$

where t_d is the switching dead time, f_s the switching frequency and θ the phase shifted angle expressed as a fraction of one switching cycle.

For the power circuit, the current flowing through the output inductor has the saw-tooth waveform biased by the output dc current I_o. Defining I_{Lopeak} and $I_{Lovalley}$ as the peak and valley values of this saw-tooth shaped current, respectively, then there are:

$$I_{Lopeak} = \frac{1}{2}\frac{(\frac{V_d}{k} - V_o)}{L_o}\frac{D_R}{f_s} + I_o = \frac{(V_d - kV_o)V_o}{4f_s V_d L_o} + I_o \tag{2-3}$$

$$I_{Lovalley} = -\frac{(V_d - kV_o)V_o}{4f_s V_d L_o} + I_o \tag{2-4}$$

For the auxiliary circuit, C_{a1} and C_{a2} act as a voltage divider, each holding half the input voltage V_d. When the two switches on each leg are switched alternately and symmetrically with little dead time in between, the auxiliary inductors L_{a1} and L_{a2} each see alternating positive and negative voltage for equal intervals. For example, when S_1 is ON for the duration of half cycle minus t_d, L_{a1} sees the voltage across C_{a1} that is $V_d/2$, and when S_2 is ON, it sees the voltage across C_{a2} in opposite polarity that is $-V_d/2$. Then the current through L_{a1} alternatively rises and

falls in linear mode. The magnitude of the total variation of this fluctuating current is determined by

$$\Delta I_{a1} = \frac{V_d}{2L_{a1}}\left(\frac{1}{2f_s} - t_d\right) \tag{2-5}$$

When both S_1 and S_2 are OFF, because the dead time is assumed very short, the current through L_{a1} can be considered constant during the dead time interval.

Similarly, the fluctuations in the current through L_{a2} are determined by

$$\Delta I_{a2} = \frac{V_d}{2L_{a2}}\left(\frac{1}{2f_s} - t_d\right) \tag{2-6}$$

It is noticed that C_{a1} and C_{a2} are in the auxiliary current loops. Because of the capacitors, the steady state auxiliary inductor currents have no dc components. Thus, these currents have a triangle waveform that is symmetrical about zero. Defining I_{a1} and I_{a2} as the peak values of the currents through L_{a1} and L_{a2} respectively, then they are:

$$I_{a1} = \frac{V_d}{4L_{a1}}\left(\frac{1}{2f_s} - t_d\right) \tag{2-7}$$

$$I_{a2} = \frac{V_d}{4L_{a2}}\left(\frac{1}{2f_s} - t_d\right) \tag{2-8}$$

2.3.2 Steady state analysis of each interval

In the last interval of the previous cycle, both S_2 and S_4 were ON while both S_1 and S_3 OFF. The primary winding of T_r saw a constant voltage, $-V_d$, and D_{o1} was reverse biased and D_{o2} forward biased. Thus the output inductor current was reflected back the primary side via D_{o2} and T_r. The drain current of S_2 was the sum of primary current and the auxiliary inductor current I_{a1},

and it reached its peak value at the end of the last cycle. This peak value is given by

$$I_1 = I_{a1} + \frac{I_{Lopeak}}{k} \tag{2-9}$$

A. Interval 1 ($t_0 \leq t < t_1$)

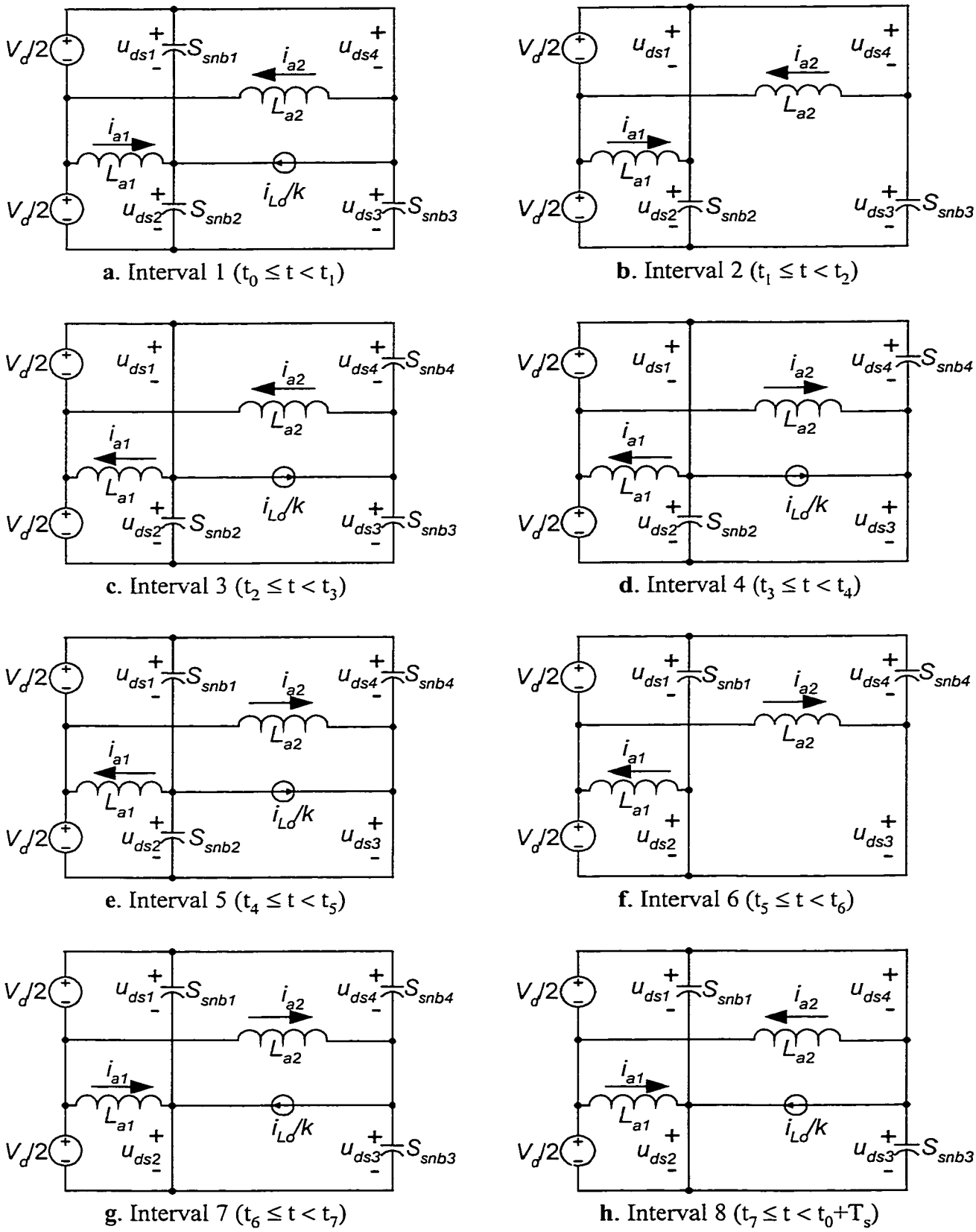
At the beginning of this interval, S_2 is turned off and no other switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.3a.

As S_2 is OFF I_1, which is the total current flowing into Leg A, starts to charge C_{sb2} and discharge C_{sb1}. Consequently u_{ds1}, the drain-to-source voltage of S_1, is decreasing while u_{ds2} is increasing. At the same time, S_4 remains ON and S_3 OFF. Then T_r continues to see a negative voltage during this interval. This keeps D_{o1} reverse biased and D_{o2} forward biased. Under this condition, the output inductor current is reflected back into the primary side through D_{o2}, and the primary current is still flowing into Leg A.

Because this interval is usually very short, the inductor current i_{a1} and i_{Lo} can be considered constant. Then, the drain-to-source voltages of both switches on *Leg A* are governed by the following equations:

$$\begin{cases} -C_{snb1}\dfrac{du_{ds1}(t)}{dt} + C_{snb2}\dfrac{du_{ds2}(t)}{dt} = I_1 \\ u_{ds1}(t) + u_{ds2}(t) = V_d \end{cases} \tag{2-10}$$

Taking the initial conditions that $u_{ds1}(t_0)=V_d$ and $u_{ds2}(t_0)=0$, and remembering $C_{snb1}=C_{snb2}$, then the solution of (2-10) is found to be the following:



a. Interval 1 ($t_0 \le t < t_1$)

b. Interval 2 ($t_1 \le t < t_2$)

c. Interval 3 ($t_2 \le t < t_3$)

d. Interval 4 ($t_3 \le t < t_4$)

e. Interval 5 ($t_4 \le t < t_5$)

f. Interval 6 ($t_5 \le t < t_6$)

g. Interval 7 ($t_6 \le t < t_7$)

h. Interval 8 ($t_7 \le t < t_0+T_s$)

Fig. 2.3 Equivalent circuits in different intervals.

$$u_{ds1}(t) = V_d - \frac{I_{a1} + I_{Lopeak}/k}{2C_{sb1}}(t - t_0) \tag{2-11}$$

$$u_{ds2}(t) = \frac{I_{a1} + I_{Lopeak}/k}{2C_{sb2}}(t - t_0) \tag{2-12}$$

It is seen from (2-12) that because of C_{sb2}, u_{ds2} rises slowly, providing the ZVS condition for the switch to turn off. Thus, a nearly lossless turn-off is achieved on S_2.

Within this interval u_{ds1} falls to zero volts and u_{ds2} reaches V_d, then the body diode of S_1 latches in to give i_{a1} a path to flow. This clamps u_{ds1} at zero in the rest of this interval, providing the ZVS condition for S_1 to turn on.

It is also noticed that although the auxiliary current i_{a1} joins the load current to exert more current stress on S_2 at its turn-off, the auxiliary current is enhanced by the load current in discharging the snubber of S_1, preparing the ZVS condition for $S_1$to turn on.

After u_{ds1} reaches zero, the primary winding of T_r will see a zero voltage as S_4 is still ON. As required by L_o, both D_{o1} and D_{o2} start to share the output inductor current i_{Lo} in the freewheeling mode as in a conventional full bridge converter. Thus the primary current i_p stops flowing and only i_{a1} flows into *Leg A*. In the meantime, the current that flows through S_4 only consists of i_{a2} which is the current of the auxiliary inductor L_{a2}. It is found that

$$i_{a2}(t) = \frac{V_d}{2L_{a2}}(t - t_0 - \frac{\theta}{f_s}) + I_{a2} \tag{2-13}$$

The duration of this interval is the switching dead time t_d, i.e.,

$$t_1 - t_0 = t_d \tag{2-14}$$

B. Interval 2 ($t_1 \leq t < t_2$)

At the beginning of this interval, S_1 is turned on under ZVS condition. Thus a nearly lossless turn-on switching is achieved on S_1. No other switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.3b.

As S_1 is ON, L_{a1} sees a constant voltage established by C_{a1}. Then i_{a1} starts to increase linearly from its negative peak as governed by

$$i_{a1}(t) = \frac{V_d}{2L_{a1}}(t - t_1) - I_{a1} \tag{2-15}$$

As both S_1 and S_4 are ON, the primary winding of T_r still sees zero voltage. Thus both output rectifier diodes conducts to freewheel the output inductor current, and no current flows through the primary winding. Hence there is still the single current i_{a2} flowing through S_4 as governed by (2-13).

The duration of this interval is determined by the phase shift angle that is required to regulate the output voltage as well as by the dead time:

$$t_2 - t_1 = \frac{\theta}{f_s} - t_d \tag{2-16}$$

and the phase shift angle expressed as a fraction of a switching cycle period, is approximately governed by

$$\theta = \frac{1}{2} - \frac{kV_o}{2V_d} - t_d f_s \tag{2-17}$$

C. Interval 3 ($t_2 \leq t < t_3$)

At the beginning of this interval S_4 is turned off. No other switching action takes place

during this interval. The equivalent circuit of this interval is shown in Fig. 2.3c.

When S_4 is off, i_{a2} reaches its positive p-eak value I_{a2}. Similar to Interval 1, this current starts to charge C_{sb4} and discharge C_{sb3}. Thus u_{sb4} starts to rise from zero while u_{sb3} decreases from V_d.

During this interval T_r starts to see a posi.tive voltage because S_1 is already ON. Thus D_{o1} is forward biased and D_{o2} reverse biased. The total output inductor current that is at its valley value now starts to flow through D_{o1}, forcing a primary current to flow. Therefore the current flowing out of Leg B is i_{a2} minus the reflected output inductor current during the discharging/charging interval.

As this interval is very short, i_{a2} is almost constant at its peak value I_{a2}. So is the output inductor current at its valley value as given in (2–4). Similar to Interval 1, it is found that

$$u_{ds3}(t) = V_d - \frac{I_{a2} - I_{Lovalley}/k}{2C_{sb3}}(t - t_2) \tag{2-18}$$

$$u_{ds4}(t) = \frac{I_{a2} - I_{Lovalley}/k}{2C_{sb4}}(t - t_2) \tag{2-19}$$

Owing to C_{sb4} u_{sb4} can only rise slowly, providing the ZVS condition for S_4 to turn off. Thus a nearly lossless turn-off is achieved on S_4.

Contrary to the switches on Leg A as seen from (2-18) and (2-19), the load current relieves S_4's turn-off current stress from i_{a2}, but it also reduces the strength of i_{a2} in discharging the snubber capacitor of S_3. In order to prepare the ZVS condition for S_3 to turn on, I_{a2} must be greater than the reflected load current. Otherwise ZVS turn-on would be lost in C_{sb3}. This shows the opposite effect of the load current on two different legs and this phenomenon shall be

observed in designing the auxiliary circuit.

The duration of this interval is determined by the dead time:

$$t_3 - t_2 = t_d \tag{2-20}$$

D. Interval 4 ($t_3 \le t < t_4$)

At the beginning of this interval S_3 is turned on under ZVS condition. Thus a nearly lossless turn-on is achieved for S_3. No other switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.3d.

As S_3 is ON, L_{a2} sees a constant negative voltage established by C_{a2}. i_{a2} starts to decrease linearly, as given by

$$i_{a2}(t) = -\frac{V_d}{2L_{a2}}(t - t_3) + I_{a2} \tag{2-21}$$

During this interval the drain currents of S_1 and S_3 are the combination of i_p with i_{a1} and i_{a2}, respectively. It is found that,

$$i_{ds1}(t) = \frac{V_d}{2L_{a1}}(t - t_1) - I_{a1} + \frac{1}{k}\left[\frac{V_d - kV_o}{kL_o}(t - t_2) + I_o - \frac{(V_d - kV_o)V_o}{4f_s L_o V_d}\right] \tag{2-22}$$

$$i_{ds3}(t) = \frac{V_d}{2L_{a2}}(t - t_3) - I_{a2} + \frac{1}{k}\left[\frac{V_d - kV_o}{kL_o}(t - t_2) + I_o - \frac{(V_d - kV_o)V_o}{4f_s L_o V_d}\right] \tag{2-23}$$

The duration of this interval is determined by the duty ratio that is required to regulate the output voltage:

$$t_4 - t_3 = \frac{D_R}{f_s} = \frac{kV_o}{2f_s V_d} \tag{2-24}$$

It is equivalent to

$$t_4 - t_3 = \frac{1}{2f_s} - t_d - \frac{\theta}{f_s} \tag{2-25}$$

E. Intervals 5 through 8

The analysis of the circuit in the last four intervals of this switching cycle is similar to the first four intervals, except for the opposite switching activities on the switches. The equivalent circuit of this interval is shown in Fig. 2.3e though h. The analysis will not be repeated here.

After Interval 8, another switching cycle begins and operation of the circuit repeats the process from Intervals 1 through 8.

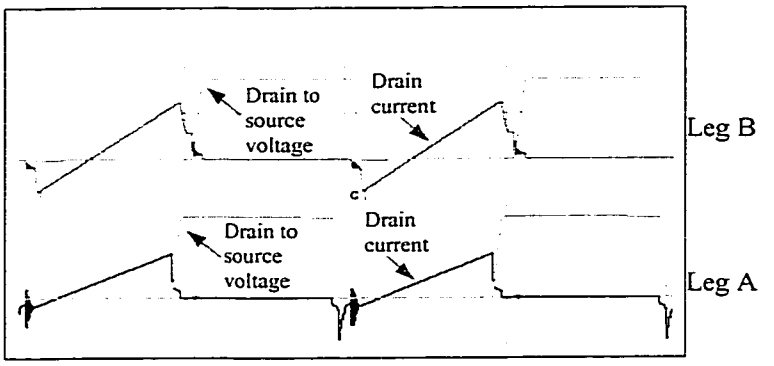
2.4 Simulation Results

Simulation of the proposed converter topology is performed with the Pspice software. Table 2.1. shows the principal parameters of the circuit used in simulation. Since the drain-to-source voltage and drain current of the two switches on the same leg have exactly the same waveforms but out of phase, the waveforms of S_1 on Leg A and S_3 on Leg B are shown below instead of that of all four switches.

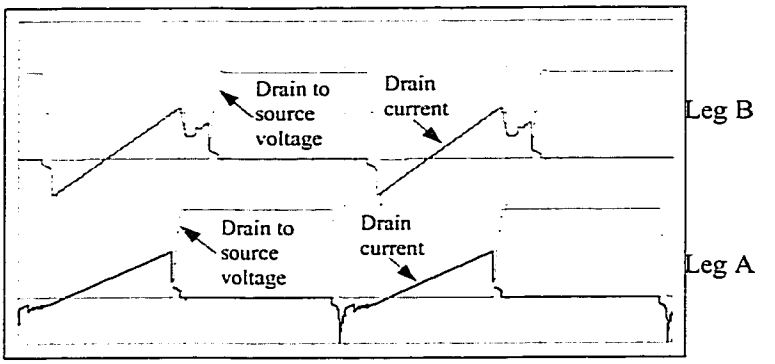
Fig. 2.4 shows the voltage and current waveforms of the switches under full load and different input voltage. It is seen that ZVS on each switch is achieved at both turn-on and turn-off under all these conditions.

Table 2.1 Principal Parameters of the Simulation Circuit

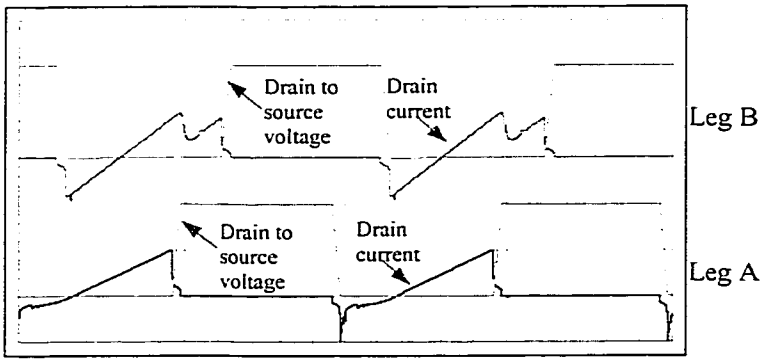
parameter	value	parameter	value
k	5.5:1	C_{sb3}, C_{sb4}	1n F
t_d	400 ns	L_{a1}	200 μH
C_{a1}, C_{a2}	1 μF	L_{a2}	100 μH
C_{sb1}, C_{sb2}	1 nF	S_1, S_2, S_3, S_4	IRFP460



a. Low line full load: V_d =350 V.

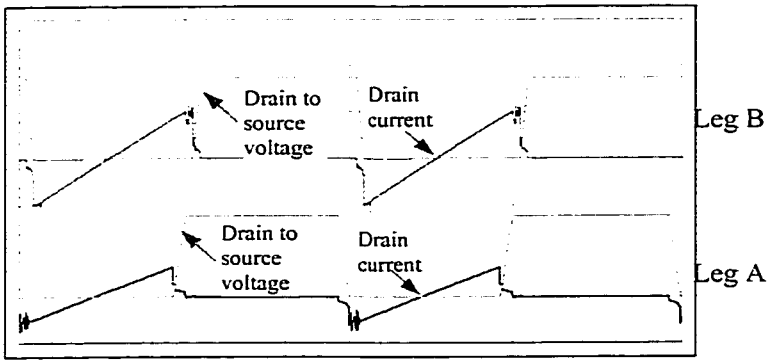


b. Medium line full load: V_d =380 V

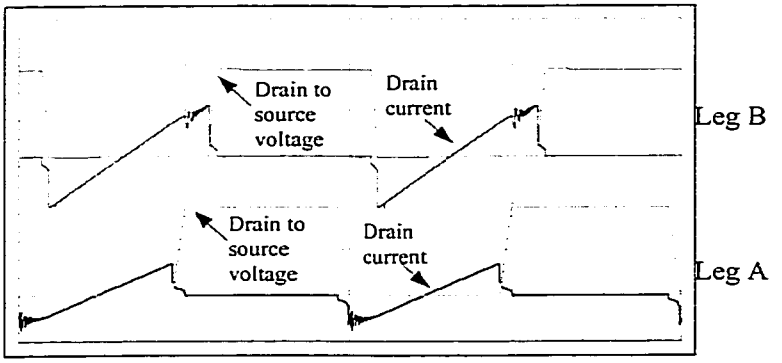


c. High line full load: V_d =400 V

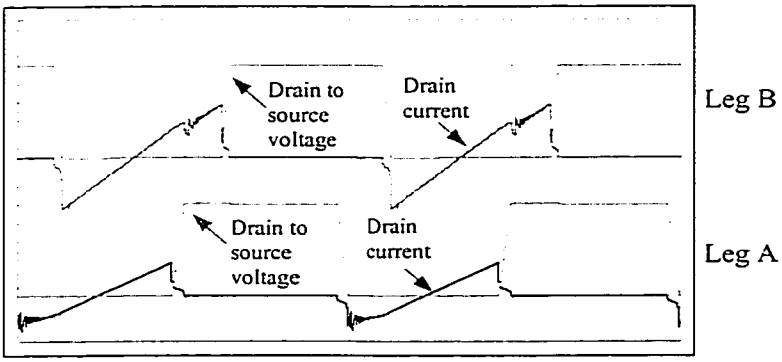
Fig. 2.4 The current and voltage waveforms of switches on both legs of the bridge at full load condition. P_o=500W. Scale: voltage-200V/div., current-5A/div. time-5μs/div.



a. Low line light load: V_d =350 V

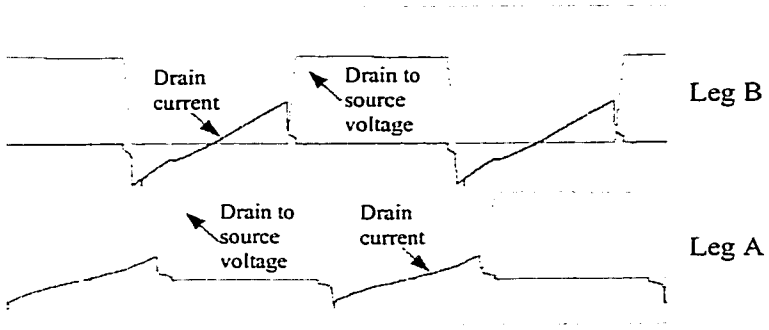


b. Medium line light load: V_d=380 V

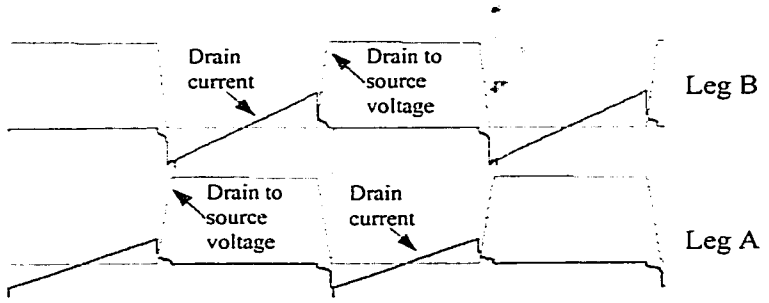


c. High line full light load: V_d=400 V

Fig. 2.5 The current and voltage waveforms of switches on both legs of the bridge at light load condition. Po=50W (10% rated load). Scale: voltage-200V/div., current-5A/div. time-5μs/div.



a. Simulation results under open circuit condition. V_d=380 V, P_o=0 W.



b. Simulation results under short circuit condition. V_d=380 V.

Fig. 2.6 The current and voltage waveforms of switches on both legs under extreme operating conditions.

Fig. 2.5 shows the voltage and current waveforms of the switches under 10% of the rated load and different input voltage conditions. It is seen that ZVS is also achieved on each switch at both turn-on and turn-off under all these conditions.

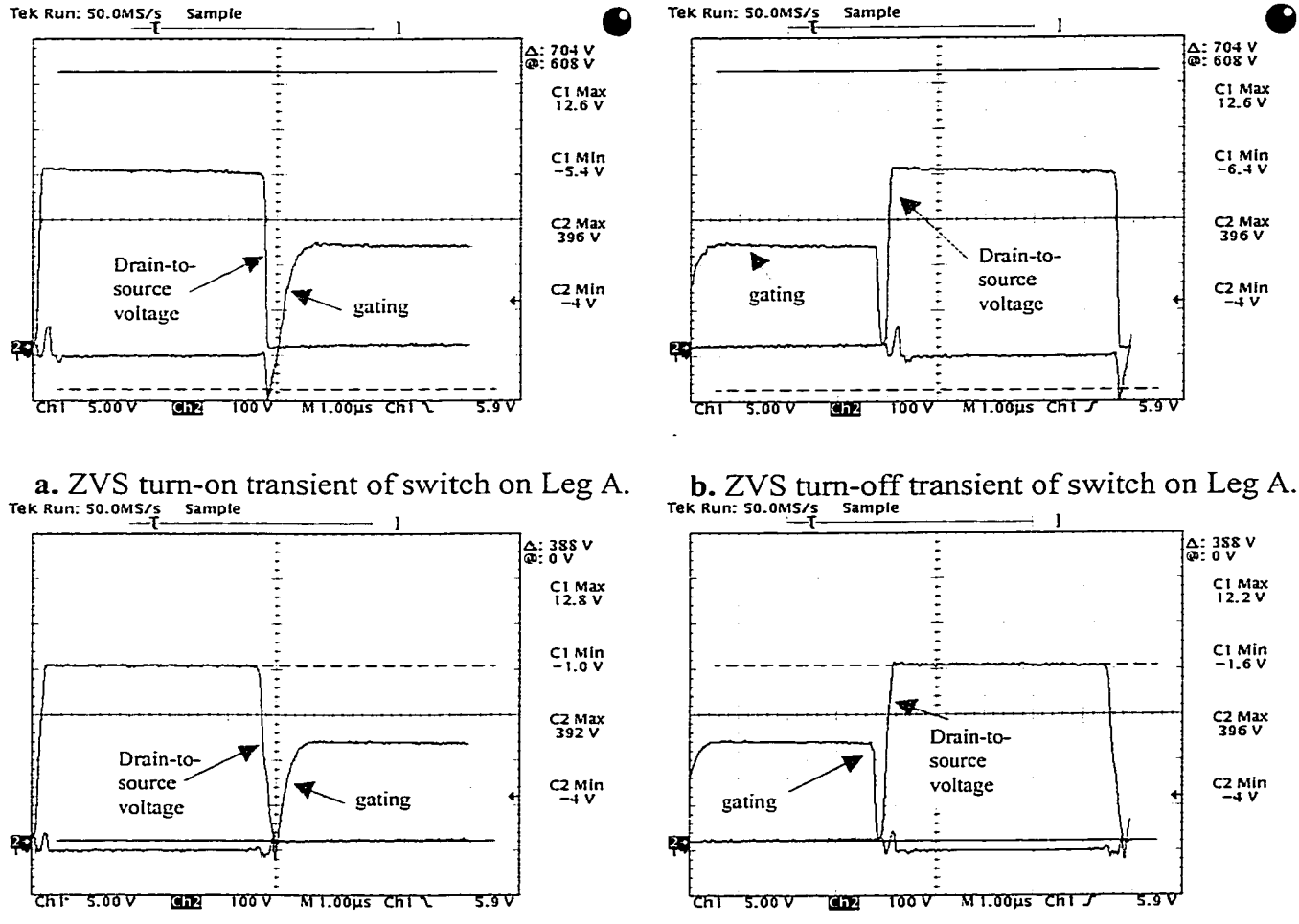
Fig. 2.6 shows the voltage and current waveforms of the switches under extreme operating conditions, i.e., the open or short circuit conditions. It can be concluded that ZVS is still achieved under these extreme conditions.

In summary, as seen from Fig. 2.4, Fig. 2.5 and Fig. 2.6, ZVS at turn-on and turn-off on each switch is achieved under all line and load conditions. All these prove the concepts of the

proposed topology, i.e., ZVS is achieved independent of line and load conditions.

2.5 Experimental Results

A 500 W, 300-400 V dc to 55 V dc prototype converter operating at 100 kHz was built to prove the concepts of the proposed topology. Listed in Table 2.1 are the principal parameters of the prototype converter.



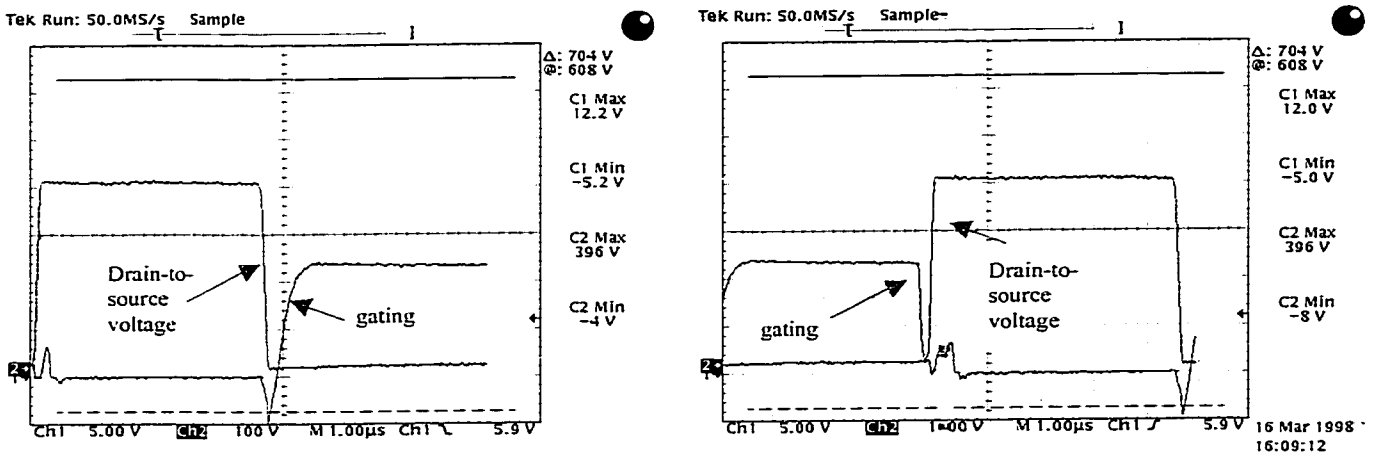
a. ZVS turn-on transient of switch on Leg A.

b. ZVS turn-off transient of switch on Leg A.

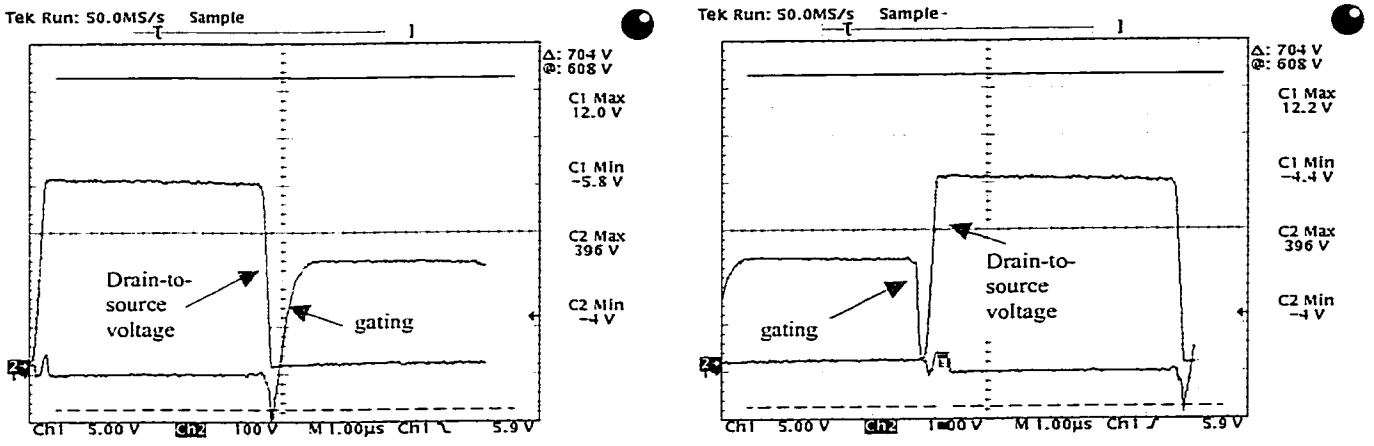
c. ZVS turn-on of the switches on Leg B.

d. ZVS turn-off of the switches on Leg B.

Fig. 2.7 The gating and drain-to-source voltage waveforms of the switches under full load condition. f_s=128 kHz, V_o=55 V, P_o=500 W, V_d=390 V.
Vertical scales: 100V/div. for the drain voltage, 10V/div. for the gating signal. Timing: 1μs/div.



a. ZVS turn-on of the switches on Leg A. **b.** ZVS turn-off of the switches on Leg A.



c. ZVS turn-on of the switches on Leg B. **d.** ZVS turn-off of the switches on Leg B.

Fig. 2.8 The gating and drain-to-source voltage waveforms of the switches under light load condition. f_s=128 kHz, V_o=55 V, P_o=50 W, V_{dc}=390 V.
Vertical scales: 100V/div. for the drain voltage, 5V/div. for the gating signal. Timing: 1µs/div.

Fig. 2.7 shows the gating signal and the drain-to-source voltage of the under full load condition. The waveforms of only one switch from each leg are shown. The other switch has the same waveform with a 180° phase delay.

In Fig. 2.7 the drain current is not shown for the reason that putting the current probe to measure the current requires a long hook of wire inserted into the circuit, and the inductance of long wire hook will interfere with the normal operation and the wire hook can easily pick up

noises. Without detecting the drain current, it can still be concluded from Fig. 2.7 that each switch has ZVS switching at both turn-on and turn-off under all those conditions. Because, the gating signal comes after the drain to source voltage completely drops to zero, and it is withdrawn completely before the drain to source voltage starts to rise from zero.

Fig. 2.8 shows the gating signal and the drain to source voltage waveforms of the switches under 10 % of the rated load condition. Similarly, it can be concluded that ZVS is achieved on each switch under all those conditions.

Fig. 2.9 shows the overall efficiency as a function of the output power. It is seen that, the efficiency is almost constant (>97%) over the range from 100% down to 50% rated load, but it will drop gradually below this range. This is because the conduction losses in the auxiliary circuit which are independent of the output load, become significant at reduced load.

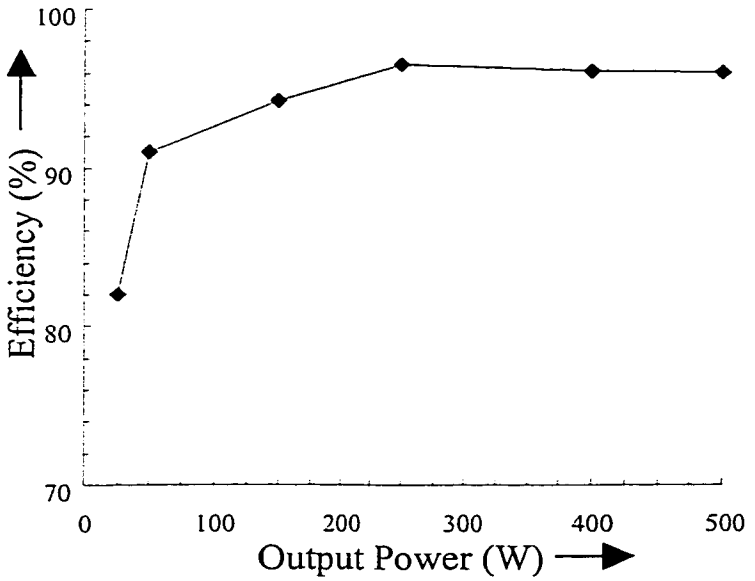


Fig. 2.9 The overall efficiency as a function of output power. Operating conditions: f_s=128 kHz, V_o=55 V, V_d=390 V.

2.6 Conclusions

The steady state analysis, simulation and experimental results have shown that the proposed ZVS full bridge dc/dc converter topology is advantageous in the following aspects:

(i) It achieves ZVS independent of the line and load conditions, thereby overcoming the drawbacks in the existing soft switching full bridge converter topologies,

(ii) It employs a simple auxiliary circuit that consists of passive components only; thus the control of the converter is not complicated,

(iii) The power circuit is the same as a conventional full bridge converter. This makes the design and implementation of the proposed topology much easier.

In short, the proposed ZVS full bridge topology is an attractive solution for general applications of power level up to 3 kW.

CHAPTER 3

DYNAMIC ANALYSIS

3.1 Introduction

The steady state analysis presented in the previous chapter assumed that the gating of the switches on each leg was in perfect symmetry. However, this symmetry is hardly true in reality. When the gating becomes asymmetrical, it will result in a dc voltage component in the output of the bridge legs, and this dc voltage may saturate the current sense transformer.

A simple solution to this problem is to insert a dc blocking capacitor between the bridge and the current sense transformer. However, a conventional opinion about the addition of this dc blocking capacitor is that PCMC is no longer applicable to the full bridge converter. In fact, this opinion is only true for the conventional PWM full bridge converter. This chapter will demonstrate that PCMC can still be used in the phase shift PWM full bridge converter.

To achieve the closed loop stability is another important issue. To reveal the dynamic properties of the proposed converter topology, the small signal model will be derived in this chapter using averaged state space equations.

Although the auxiliary circuit is critical in achieving ZVS of proposed topology, it just circulates the currents inside the auxiliary circuit and it hardly affects the power transfer of the converter. Thus, the auxiliary circuit has negligible influences on the dynamic properties of the power circuit, and it will be excluded from the discussion in the rest of this chapter.

In Sec. 3.2, the gating asymmetry and the flux imbalance in the current sense transformer will be addressed. In Sec. 3.3, the topology will be modified and analyzed, to overcome the gating asymmetry problem. The small signal model will be established in Sec. 3.4. The transfer

function for PCMC will be derived in Sec. 3.5 along with an example of the straightforward compensation to stabilize the closed loop. Simulation results will be presented in Sec. 3.6, followed by the conclusions.

3.2 Flux Imbalance Problems

3.2.1 Use of current transformer

Current transformer is usually used in the medium to high power level converters to replace the simple but lossy series resistor current sensor. In a current mode controlled converter, the current transformer serves efficiently as a current sensor that feeds back the sensed current information to the controller. In a voltage mode controlled converter, it is used for over current protection.

The current sense transformer is normally made from a small toroidal core. Because a toroidal core is unable to have an air gap, the current transformer can easily be saturated by a small dc voltage component. When saturation happens in the sensor, the control loop loses the feedback signal and the converter loses regulation that may destroy the precious loads it powers.

For the full bridge topology, the current sensor can be located either on the secondary side or on the primary side, and it is concluded in [19] that putting it on the primary side is advantageous mainly for smaller size and the input/output isolation. However, located on the primary side, it faces risks of saturation owing to the dc voltage in the output of the bridge legs.

3.2.2 DC voltage component in the output of the bridge legs

In the proposed topology shown in Fig. 2.1, a dc voltage component may be present at the output of the bridge legs when the gating of the switches is not in perfect symmetry. This

asymmetry may be either static or dynamic. Although it is normally slight, the asymmetry is inevitable in any real converter because of the following major factors:

(i) Random deviation of individual switches from each other in time response to gating signal due to product parameter spans;

(ii) Unequal duty ratios and dead times between the switches on the two legs because of the manufacturing limitation of the control chips;

(iii) Thermal effects on component parameters; and

(iv) Sudden changes in the phase shift angle due to fast transients in the input voltage or output load.

When the dc voltage component exists, it could easily saturate the current sense transformer due to the aforementioned reasons.

3.2.3 PCMC protects the power transformer but not the current sense transformer

With PCMC, when flux imbalance in the power transformer occurs, no matter what the reason, the magnetizing current reflects this imbalance by showing a dc bias. Because the sensor sees the sum of the magnetizing current and the load current, this dc bias in the magnetizing current changes the arrival time of the peak of the sensed current. The arrival of the peak current commands the control circuit to adjust the phase shift angle. In this way the duration of magnetizing/demagnetizing period is adjusted such that the flux balance is re-established in the power transformer.

When the output of the bridge legs has a dc voltage component, the magnetizing current of the power transformer may have a dc bias. Unlike the small, non-air-gapped current censor transformer core, the power transformer usually has an air gapped core. This air gap stores the dc

magnetizing energy and keeps the core from saturation.

However, current sense transformer is still vulnerable to the dc voltage because it does not have an air gap to store any dc magnetizing energy.

3.3 Flux Balancing

3.3.1 Solution to the saturation problem of the current sense transformer

A direct solution to the saturation problem of the current sense transformer is to block this dc component by inserting a small capacitor in series with sensor and power transformers. This is illustrated in Fig. 3.1, where the dc blocking capacitor is labeled C_s. The capacitor C_s blocks the dc voltage component, thus eliminating the flux imbalance and preventing saturation.

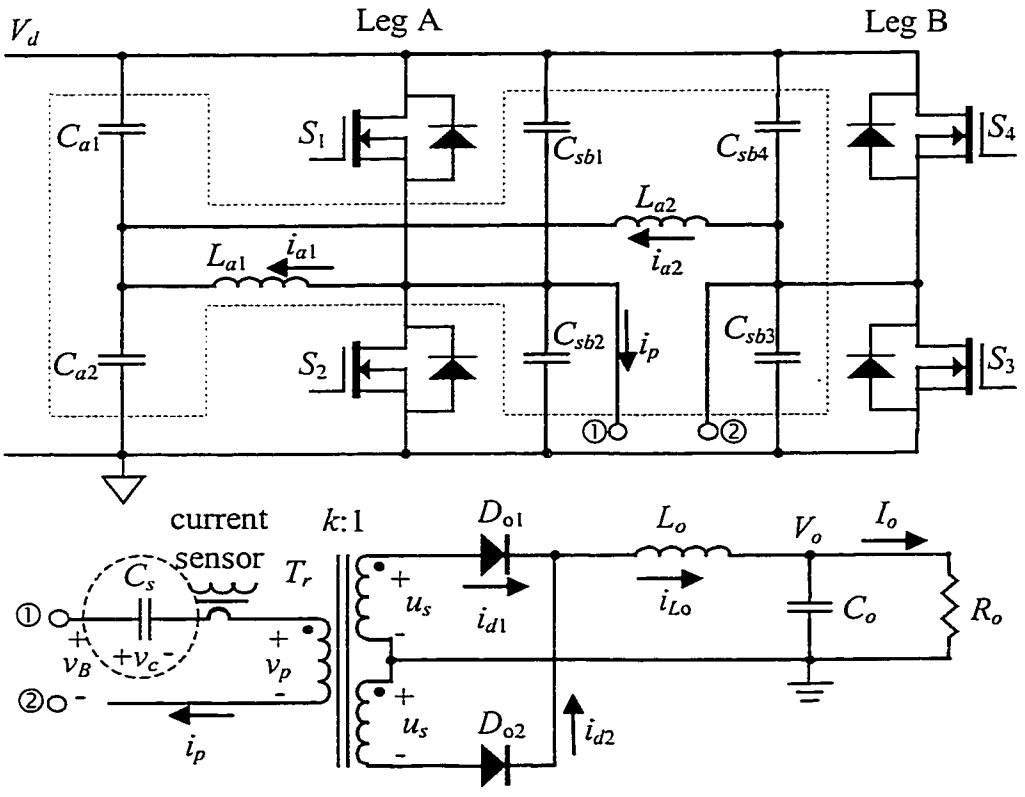


Fig. 3.1 ZVS full bridge converter with dc blocking capacitor C_s.

However, the addition of the series dc blocking capacitor increases the reverse voltage stress on the output rectifier diodes. This problem comes from both the dc voltage and ripple voltages across the capacitor. Due to voltage superimposition, the dc voltage across the capacitor and its ripples will be alternatively added on top the input voltage in two consecutive half switching cycles. Then the power transformer will see the input voltage being increased by the voltage across the blocking capacitor. The increased voltage will be reflected into the secondary side, and it will increase the reverse voltage on the diodes in the rectification stage. To limit the voltage stress, a larger capacitor shall be used to suppress the ripple voltages. But a too large capacitor will be both expensive and bulky. A trade-off should be made to select the capacitor.

R. D. Middlebrook pointed out that in a conventional PWM full bridge converter PCMC can not be used along with the dc blocking capacitor. This can be explained as follows. Assume a positive dc voltage is built up across the blocking capacitor for whatever reasons, this voltage is deducted from the input voltage during the positive voltage pulse of one switching cycle. Thus the current slope is reduced and the peak current comes at a later time to expand the positive voltage pulse. Contrarily, the dc voltage across the blocking capacitor is added on top of the input voltage during the consecutive negative voltage pulse and it increases the current slope. Thus, the peak current comes at an earlier time and the negative voltage pulse is cut shorter. Because, during the rest of the cycle all switches are OFF and the capacitor sees an open circuit, there are residual charges left on the capacitor due to the unbalanced voltage pulses and this further increase the dc voltage across the capacitor. In the following cycle, the increased dc voltage will further expand the positive voltage pulse and decrease the negative voltage pulse. One cycle after another, the dc voltage across the capacitor increases continuously and it will eventually cut off the power flow from the input to the load.

However, in a phase shift PWM full bridge converter, the dc blocking capacitor will see the short circuit during the phase shift intervals. Because of the short circuit, any extra charges on the dc blocking capacitor will be discharged and the voltage across the capacitor will not run away from its equilibrium value after each cycle. Thus, PCMC can still be used along with the dc blocking capacitor. Detail analysis will be presented below.

3.3.2 Analysis of the dc voltage component

To be generic, the following assumptions are made :

(i) The duty ratios of the four switches S_1, S_2, S_3 and S_4 of the bridge in Fig. 2.1 are respectively D_1, D_2, D_3 and D_4;

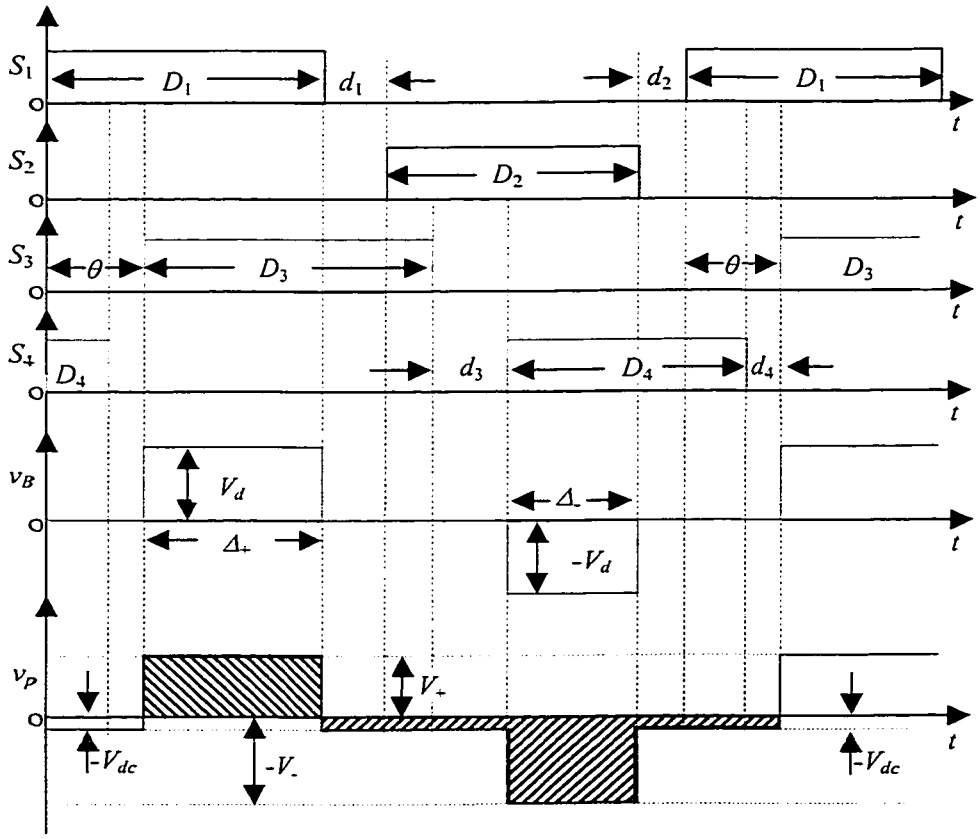


Fig. 3.2 Timing sequence of the asymmetrical gating pattern. v_B is the bridge output voltage, v_p is the voltage seen after the dc blocking capacitor.

(ii) The dead time between the hind edge of D_1 and front edge of D_2 is d_1, and that between the hind edge of D_2 and front edge of D_1 is d_2;

(iii) The dead time between the hind edge of D_3 and front edge of D_4 is d_3, and that between the hind edge of D_4 and front edge of D_3 is d_4;

(iv) The phase shift angle, expressed as a fraction of a switching period, is θ; and

(v) All dead times are very small as compared to the switching period,

Fig. 3.2 shows the time sequence of the asymmetrical gating signals and key waveforms. Based on the above assumptions, there are the following relationships:

$$D_1 + d_1 + D_2 + d_2 = 1 \tag{3-1}$$

$$D_3 + d_3 + D_4 + d_4 = 1 \tag{3-2}$$

Therefore, the positive voltage pulse has a magnitude of V_d, and its pulse width as a fraction of a switching period is determined by

$$\Delta_+ = D_1 - \theta \tag{3-3}$$

and the negative voltage pulse has a magnitude of $-V_d$, and its pulse width as a fraction of a switching period is determined by

$$\Delta_- = 1 - d_2 - (\theta + D_3 + d_3) \tag{3-4}$$

The dc voltage component of such periodical bipolar voltage pulses is determined by

$$V_{dc} = (\Delta_+ - \Delta_-)V_d \tag{3-5}$$

Substituting (3-3) and (3-4) into (3-5), and replacing the number "1" with (3-1) and (3-2), it yields

$$V_{dc} = \frac{D_1 - D_2 + D_3 - D_4 - d_1 + d_2 + d_3 - d_4}{2} V_d \tag{3-6}$$

In an ideal case the gating is in perfect symmetry, then there are D_1=D_2=D_3=D_4 and

$d_1=d_2=d_3=d_4$. Thus, as seen from (3-6), there will be no dc voltage component in the output voltage of the bridge.

Unfortunately, the asymmetry of gating inevitably exists in reality because of the aforementioned factors. Therefore, as seen from (3-6), a dc voltage component may exist and it shall not be overlooked.

3.3.3 Flux balancing by adding a series dc blocking capacitor

As mentioned previously, if no corrective means is taken, the dc voltage given in (3-6) will appear across the series connected current sense transformer and power transformer, and eventually it will drive the current sensor into saturation, if it does not saturate the power transformer.

When a capacitor is put in series with the current sensor and power transformers, this capacitor will block the dc voltage component such that the transformers become blind to the dc voltage component, and this forces balanced flux excursion in the transformer cores.

When the dc blocking capacitor is used, as seen from Fig. 3.1, the positive and negative dc voltage pulses seen by the current sense transformer are governed respectively by

$$V_+ = V_d - V_{dc} \tag{3-7}$$

$$V_- = -V_d - V_{dc} \tag{3-8}$$

and they have the pulse widths determined by (3-3) and (3-4), respectively. During the silent intervals between these two pulses, the transformer sees a voltage of $-V_{dc}$ for a total time of $(1-\Delta_+-\Delta_-)$. Hence volt-second products of the voltage pulses seen by the series connected transformers are:

(i) Positive voltage pulse volt-second product:

$$V_+ \cdot \Delta_+ \cdot T_s = V_d \Delta_+ T_s - V_{dc} \Delta_+ T_s \tag{3-9}$$

(ii) Negative voltage pulse volt-second product:

$$V_- \cdot \Delta_- \cdot T_s = -V_d \Delta_- T_s - V_{dc} \Delta_- T_s \tag{3-10}$$

(iii) Silent intervals volt-second product:

$$-V_{dc} \cdot (1 - \Delta_+ - \Delta_-) \cdot T_s = -V_{dc} T_s + V_{dc} \Delta_+ T_s + V_{dc} \Delta_- T_s \tag{3-11}$$

where T_s is the period of a switch cycle.

The total volt-second product in one cycle is the sum of above three equations. Substituting (3-5) into the summation, it yields zero. This means a balanced volt-second product in one cycle. Because the sensor and power transformers are in series, then both of their magnetizing inductors have a balanced volt-second product, or balanced flux excursion. In other words, this achieves flux balancing in the current sense transformer and prevents it from possible saturation.

3.4 Small Signal Model

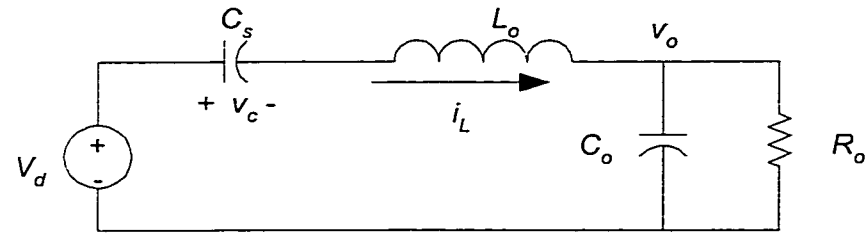
3.4.1 Modes of operation and the equivalent circuits

As stated previously, the circuit operation seen from the secondary side has three distinct modes when the converter is in CCM. Specifically in these three modes, the output stage sees respectively, (i) a positive input voltage when both S_1 and S_3 are ON and D_{o1} is conducting, (ii) a positive input voltage when both S_2 and S_4 are ON and D_{o2} is conducting, and (iii) a positive voltage across C_s in the rest of the switching cycle. In all three modes, the effects of the current sense transformer is ignored because it is equivalent to a negligible resistor due to the high turns ratio of the current transformer.

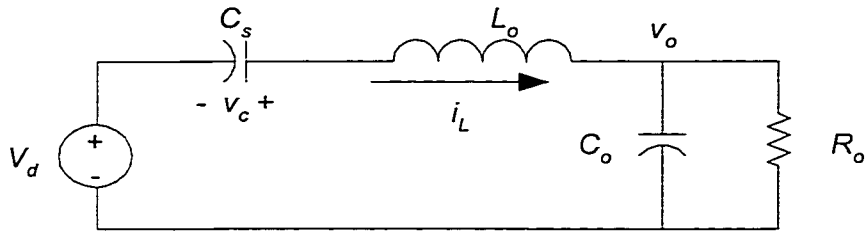
Fig. 3.3 shows equivalent output circuits of these three modes seen on the secondary side of the power transformer. When D_{o1} and D_{o2} conduct in Modes 1 and 2 respectively, the output inductor sees different end of C_s; thus C_s flips its direction in Modes 1 and 2.

It is noticed that the equivalent circuit of Mode 3 uses the absolute voltage of C_s. It is because when the actual dc voltage across C_s is positive, D_{o1} will conduct in this mode, and when it is negative, D_{o2} will conduct. Thus the dc voltage across C_s seen by the output inductor is always positive in Mode 3.

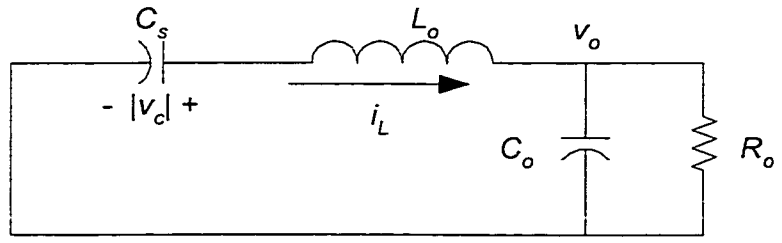
A unity turns ratio k is assumed for convenience in the following discussion.



a. Mode 1. Duration: Δ_+



b. Mode 2. Duration: Δ_-



c. Mode 3. Duration: $1-\Delta_+-\Delta_-$

Fig. 3.3 Equivalent circuits in three different modes each switching cycle.

3.4.2 State space equations

A. *Mode 1*

In this mode both S_1 and S_3 are ON, and D_{o1} is conducting while D_{o2} is blocked. Thus the state space equations for this mode are as follows.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & -\frac{1}{L_o} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} & 0 \\ \frac{1}{C_s} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_o \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \end{bmatrix} \cdot V_d \tag{3-12}$$

The duration of this mode is Δ_+ that is determined by (3-3).

B. Mode 2

In this mode both S_2 and S_4 are ON, and D_{o2} is conducting while D_{o1} is blocked. Thus the state space equations for this mode are defined by

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & \frac{1}{L_o} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} & 0 \\ -\frac{1}{C_s} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_o \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \end{bmatrix} \cdot V_d \tag{3-13}$$

The duration of this mode is Δ_- that is determined by (3-4).

C. *Mode* 3

In this mode either S_1 and S_4, or S_2 and S_3, are both ON. Then the bridge output voltage is zero. Due to CCM either D_{o1} or D_{o2} (but not both if the dc voltage across C_s is not zero) must conduct to continue the output inductor current i_L, depending on the polarity of the voltage across C_s. Generally, the state space equations for this mode can be expressed as

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \\ \frac{d|v_c|}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & \frac{1}{L_o} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} & 0 \\ -\frac{1}{C_s} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_o \\ |v_c| \end{bmatrix} \tag{3-14}$$

The duration of this mode is $1-\Delta_+-\Delta_-$.

3.4.3 Averaged state space equations

For each cycle, the averaged state space equations are obtained by weighted summing of (3-12) (3-13) and (3-14), i.e. by applying (3-12)·Δ_++(3-13)·Δ_-+(3-14)·$(1-\Delta_+-\Delta_-)$. This yields:

$$\begin{cases} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & \frac{1-2\Delta_+}{L_o} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} & 0 \\ \frac{2\Delta_+ - 1}{C_s} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_o \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{\Delta_+ + \Delta_-}{L_o} \\ 0 \\ 0 \end{bmatrix} \cdot V_d & \text{if} \quad V_{dc} \geq 0 \\ \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & \frac{2\Delta_- - 1}{L_o} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} & 0 \\ \frac{1-2\Delta_-}{C_s} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_o \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{\Delta_+ + \Delta_-}{L_o} \\ 0 \\ 0 \end{bmatrix} \cdot V_d & \text{if} \quad V_{dc} < 0 \end{cases} \tag{3-15}$$

In the following only the case of $V_{dc}\geq 0$ is discussed. The other case can be easily analyzed following a similar procedure and the results are similar.

Defining the following two constants

$$\alpha = 1 + D_1 - d_2 - D_3 - d_3 \tag{3-16}$$

$$\beta = 1 - 2D_1 \tag{3-17}$$

Substituting (3-3), (3-4) into (3-15), and using above two constants to simplify the results, it yields:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & \frac{\beta+2\theta}{L_o} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} & 0 \\ -\frac{\beta+2\theta}{C_s} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L \\ v_o \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{\alpha-2\theta}{L_o} \\ 0 \\ 0 \end{bmatrix} \cdot V_d \tag{3-18}$$

3.4.4 DC and AC models

Decomposing each variable into DC and AC components, i.e.,

$$\begin{cases} v_o \rightarrow V_o + \tilde{v}_o \\ i_L \rightarrow I_L + \tilde{i}_L \\ \theta \rightarrow \theta + \tilde{\vartheta} \\ V_d \rightarrow V_d + \tilde{v}_d \\ v_c \rightarrow V_{dc} + \tilde{v}_c \end{cases} \tag{3-19}$$

Substituting (3-19) into (3-18), and rearranging the result, it yields:

$$\begin{cases} L_o \frac{d\tilde{i}_L}{dt} = -(V_o + \tilde{v}_o) + (\alpha - 2\theta - 2\tilde{\vartheta})(V_d + \tilde{v}_d) + (\beta + 2\theta + 2\tilde{\vartheta})(V_{dc} + \tilde{v}_c) \\ C_o \frac{d\tilde{v}_o}{dt} = (I_L + \tilde{i}_L) - \frac{1}{R_o}(V_o + \tilde{v}_o) \\ C_s \frac{d\tilde{v}_c}{dt} = -(\beta + 2\theta + 2\tilde{\vartheta})(I_L + \tilde{i}_L) \end{cases} \tag{3-20}$$

A. DC model

From (3-20), the DC model of the circuit is obtained as:

$$\begin{cases} V_o = (\alpha - 2\theta)V_d + (\beta + 2\theta)V_{dc} \\ I_L = \frac{V_o}{R_o} \end{cases} \tag{3-21}$$

B. AC model

Also from (3-20), the AC model is obtained as:

$$\begin{cases} L_o \dfrac{d\tilde{i}_L}{dt} = -\tilde{v}_o + (\alpha - 2\theta)\tilde{v}_d - 2(V_d - V_{dc})\tilde{\vartheta} + (\beta + 2\theta)\tilde{v}_c - 2(\tilde{v}_d - \tilde{v}_c)\tilde{\vartheta} \\ C_o \dfrac{d\tilde{v}_o}{dt} = \tilde{i}_L - \dfrac{1}{R_o}\tilde{v}_o \\ C_s \dfrac{d\tilde{v}_c}{dt} = -(\beta + 2\theta)\tilde{i}_L - 2I_L\tilde{\vartheta} - 2\tilde{i}_L\tilde{\vartheta} \end{cases} \tag{3-22}$$

3.4.5 Small signal model

Under small perturbations or seeking the small signal model, the second order terms in the AC model are ignored; thus the small signal model of the proposed converter topology is given as:

$$\begin{cases} L_o \dfrac{d\tilde{i}_L}{dt} = -\tilde{v}_o + (\alpha - 2\theta)\tilde{v}_d - 2(V_d - V_{dc})\tilde{\vartheta} + (\beta + 2\theta)\tilde{v}_c \\ C_o \dfrac{d\tilde{v}_o}{dt} = \tilde{i}_L - \dfrac{1}{R_o}\tilde{v}_o \\ C_s \dfrac{d\tilde{v}_c}{dt} = -(\beta + 2\theta)\tilde{i}_L - 2I_L\tilde{\vartheta} \end{cases} \tag{3-23}$$

3.5 Transfer Function of the Power Circuit in the PCMC and Loop Compensation

3.5.1 PCMC versus the Voltage Mode Control (VMC) and the Averaged Current Mode Control (ACMC)

PCMC is the most popular control technique for full bridge converter topology. In addition to its protection of the power transformer from saturation, PCMC inherently has the function of voltage feed forward control. For instance, as soon as the input voltage has a step up change the slope of the inductor current will be increased at once. The current sensor will directly detect the change of slope of the sensed current, and it sees that the peak of the current

comes at an earlier time. This commands the control circuit to increase the phase shift angle immediately. The increased phase shift angle reduces the effective duty ratio of the switches, cutting off the possible overflow of energy to the output and thus keeping the output voltage at the regulated point. Similarly, as the input voltage steps down, the control circuit directly detects the change via the sensed current and decreases the phase shift angle immediately. This increases the effective duty ratio to regulate the output voltage. In this way, the output regulation against the input voltage variations is fulfilled before the output voltage is actually affected.

Contrarily VMC does not have the voltage feed forward function, and the output regulation against the input voltage variations is comparatively slow. Because the controller can only detect the input variations after the output voltage has already been affected, and adjustment of the phase shift angle can only be made after the detection. Therefore it is concluded that current mode control is faster than VMC.

ACMC also has the voltage feed forward control function, and it claims better performance than PCMC [16]. However, PCMC is simpler in implementation as the control circuit directly uses the sensed pulses of the output inductor current, and closing the current loop is as simple as injecting a proper slope compensation signal. ACMC is more complicated as the control circuit has to synthesize and reconstruct the total shape of the output inductor current from the sensed current pulses. Besides, it requires complex compensations around the current error amplifier of the current loop to close the current loop, in addition to the compensation around the voltage error amplifier.

Owing to the reasons above, PCMC is the most popular control technique for the full bridge converter.

3.5.2 Transfer function and control loop

Fig. 3.4 shows the block diagram of a PCMC loop of the converter. With PCMC the slope compensation technique must be employed, otherwise a sub-harmonic oscillation would happen and the loop becomes unstable [14-16].

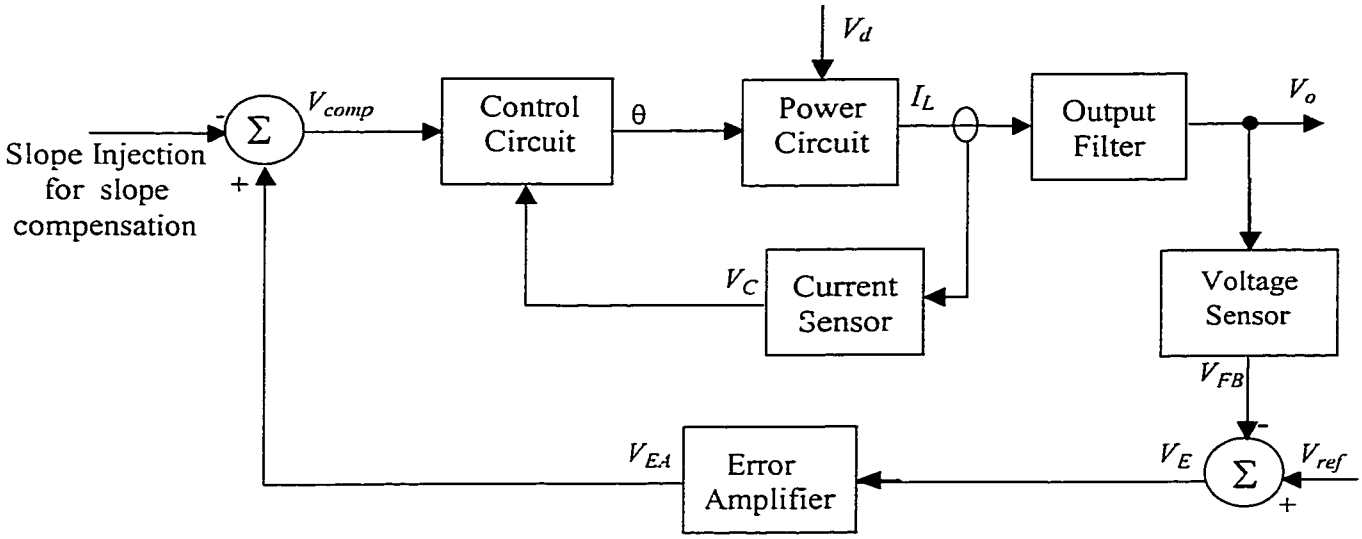


Fig. 3.4 The block diagram of the peak current mode control feedback loops.

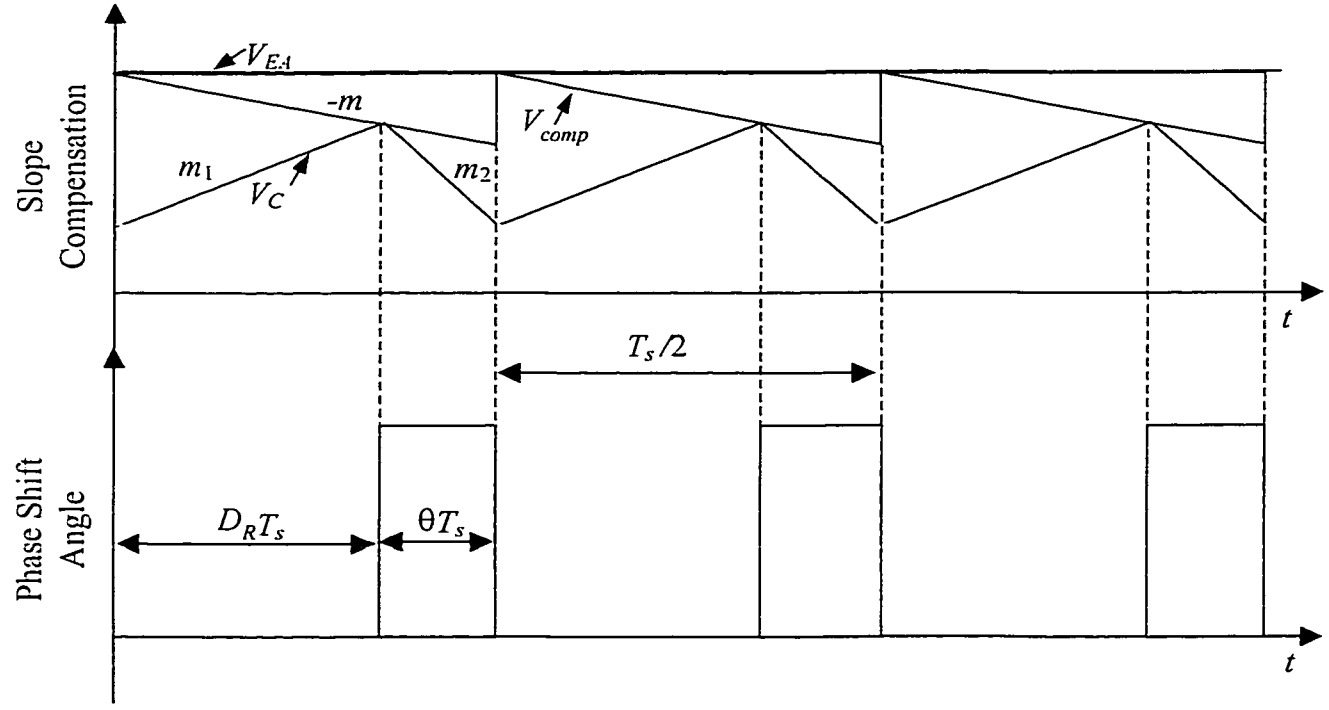


Fig. 3.5 Generating of the phase shift angle in PCMC.

The operating principle of PCMC is as follows: There are two loops, an inner current loop and an outer voltage loop. The inner loop senses the output inductor current I_L, transferring it into a voltage V_C through the current sensor. The outer loop senses the output voltage V_o and compares the sensed signal with the reference voltage V_{ref}, and this producing the error voltage V_E. V_E is amplified to produce V_{EA}, and V_{EA} is modified by the injected slope compensation signal, producing V_{comp}. Both V_C and V_{comp} are used by the control circuit to generate the phase shift angle θ. The power circuit is controlled by θ to dictate the output inductor current that is filtered by the output filter to produce the nominal output voltage V_o.

Assume the injected slope compensation signal has a slope of m, and the rising slope of the inductor current seen after the current sensor is m_1, and its falling slope is m_2. Also assume the current sensor resistor is R_s that senses the inductor current through a current transformer, and the turns ratio of the current transformer is 1: k_c, then there are

$$m_1 = \frac{(V_d - V_o)R_s}{k_c L_o} \tag{3-24}$$

$$m_2 = \frac{V_o R_s}{k_c L_o} \tag{3-25}$$

According to [16], the phase shift angle is determined by the following equation

$$\frac{R_s}{k_c} I_L = V_{EA} - m(\frac{1}{2} - \theta)T_s - \frac{m_2}{4}\theta T_s \tag{3-26}$$

By selecting $m \geq \frac{1}{2} m_2$, the current loop is stabilized [16]. Then only the stabilization of the outer voltage loop is left.

The closed inner current loop is a part of the outer voltage loop. The transfer function from the amplified error voltage V_{EA} to the output inductor current I_L shall be found to determine

the closed loop compensation around the voltage error amplifier. The rest of the power circuit is the output filter that has the transfer function from the inductor current i_L to the output voltage v_o.

It is understood that the inner current loop is usually a faster loop than the outer voltage loop. In this sense, the output voltage is usually considered constant from the point of view of the inner current loop, and this simplifies the analysis.

Using the similar designations as in (3-19), letting V_{EA} be replaced with its dc and ac components, ignoring the second order terms and neglecting the variations in V_o, then there is

$$\tilde{\vartheta} = \frac{R_s}{k_c \gamma} \tilde{i}_L - \frac{1}{\gamma} \tilde{v}_{EA} \tag{3-27}$$

where,

$$\gamma = mT_s - \frac{R_s T_s V_o}{2k_c L_o} \tag{3-28}$$

Solving (3-23), and substituting (3-27) into the result, then the following equation is obtained:

$$\begin{aligned} L_o C_s \frac{d^2 \tilde{i}_L}{dt^2} + \frac{2R_s C_s (V_d - V_{dc})}{k_c \gamma} \frac{d\tilde{i}_L}{dt} + (\beta + 2\theta)[\beta + 2\theta + \frac{2I_L R_s}{k_c \gamma}]\tilde{i}_L \\ = C_s(\alpha - 2\theta)\frac{d\tilde{v}_d}{dt} + \frac{2C_s(V_d - V_{dc})}{\gamma}\frac{d\tilde{v}_{EA}}{dt} + \frac{2(\beta + 2\theta)I_L}{\gamma}\tilde{v}_{EA} \end{aligned} \tag{3-29}$$

Taking the Laplace transform of (3-29), and using the following designations,

$$\begin{cases} \pounds(\tilde{v}_o) = \hat{v}_o(s) \\ \pounds(\tilde{v}_{EA}) = \tilde{v}_{EA}(s) \\ \pounds(\tilde{v}_d) = \hat{v}_d(s) \\ \pounds(\tilde{i}_L) = \hat{i}_L(s) \end{cases} \tag{3-30}$$

then the transfer function from output of the error voltage amplifier to the output inductor current is given by

$$\frac{\hat{i}_L(s)}{\hat{v}_{EA}(s)} = \frac{[s2C_s(V_d - V_{dc}) + 2I_L(\beta + 2\theta)]/\gamma}{s^2 L_o C_s + s\frac{2R_s C_s(V_d - V_{dc})}{k_c\gamma} + (\beta + 2\theta)(\beta + 2\theta + \frac{2I_L R_s}{k_c\gamma})} \tag{3-31}$$

And the transfer function from the input voltage to the output inductor current is given by

$$\frac{\hat{i}_L(s)}{\hat{v}_d(s)} = \frac{sC_s(\alpha - 2\theta)}{s^2 L_o C_s + s\frac{2R_s C_s(V_d - V_{dc})}{k_c\gamma} + (\beta + 2\theta)(\beta + 2\theta + \frac{2I_L R_s}{k_c\gamma})} \tag{3-32}$$

Bringing back the real, non-unity power transformer turns ratio k, namely replacing V_d with V_d/k, V_{dc} with V_{dc}/k, and C_s with k^2C_s, and substituting R_s with R_s/k to correct for the primary current sensing gain, and substituting I_L with V_o/R_o, then there are:

$$\frac{\hat{i}_L(s)}{\hat{v}_{EA}(s)} = \frac{[s2kR_o C_s(V_d - V_{dc}) + 2V_o(\beta + 2\theta)]}{\gamma R_o[s^2 L_o k^2 C_s + s\frac{2R_s C_s(V_d - V_{dc})}{k_c\gamma} + (\beta + 2\theta)(\beta + 2\theta + \frac{2V_o R_s}{k_c k\gamma R_o})]} \tag{3-33}$$

$$\frac{\hat{i}_L(s)}{\hat{v}_d(s)} = \frac{sk^2 C_s(\alpha - 2\theta)}{s^2 L_o k^2 C_s + s\frac{2R_s C_s(V_d - V_{dc})}{k_c\gamma} + (\beta + 2\theta)(\beta + 2\theta + \frac{2V_o R_s}{k_c k\gamma R_o})} \tag{3-34}$$

From (3-23), the output filter has the following transfer function

$$\frac{\hat{v}_o(s)}{\hat{i}_L(s)} = \frac{R_o}{sR_o C_o + 1} \tag{3-35}$$

Thus, the transfer function from the output of the error voltage amplifier to the output of the converter is determined by:

$$\frac{\hat{v}_o(s)}{\hat{v}_{EA}(s)} = \frac{1}{sR_o C_o + 1} \cdot \frac{[s2kR_o C_s(V_d - V_{dc}) + 2V_o(\beta + 2\theta)]}{\gamma[s^2 L_o k^2 C_s + s\frac{2R_s C_s(V_d - V_{dc})}{k_c\gamma} + (\beta + 2\theta)(\beta + 2\theta + \frac{2V_o R_s}{k_c k\gamma R_o})]} \tag{3-36}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_d(s)} = \frac{R_o}{sR_o C_o + 1} \cdot \frac{sk^2 C_s(\alpha - 2\theta)}{s^2 L_o k^2 C_s + s\frac{2R_s C_s(V_d - V_{dc})}{k_c\gamma} + (\beta + 2\theta)(\beta + 2\theta + \frac{2V_o R_s}{k_c k\gamma R_o})} \tag{3-37}$$

The transfer functions (3-36) and (3-37) indicate that the power circuit is a third order

system. Letting C_s=infinite, then the transfer functions degrade into the second order. This implies that, in order to simplify the closed loop compensation, C_s shall be selected large enough such that the zero and pole that it brings into the loop can cancel each other.

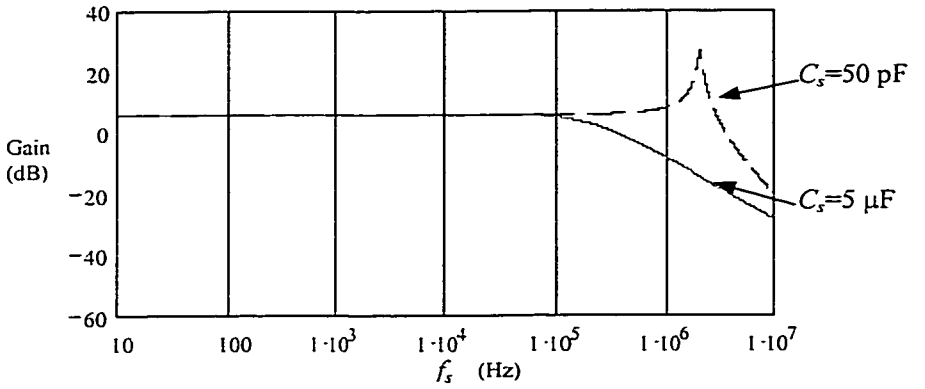


Fig. 3.6 Effects of C_s on the closed current loop gain.

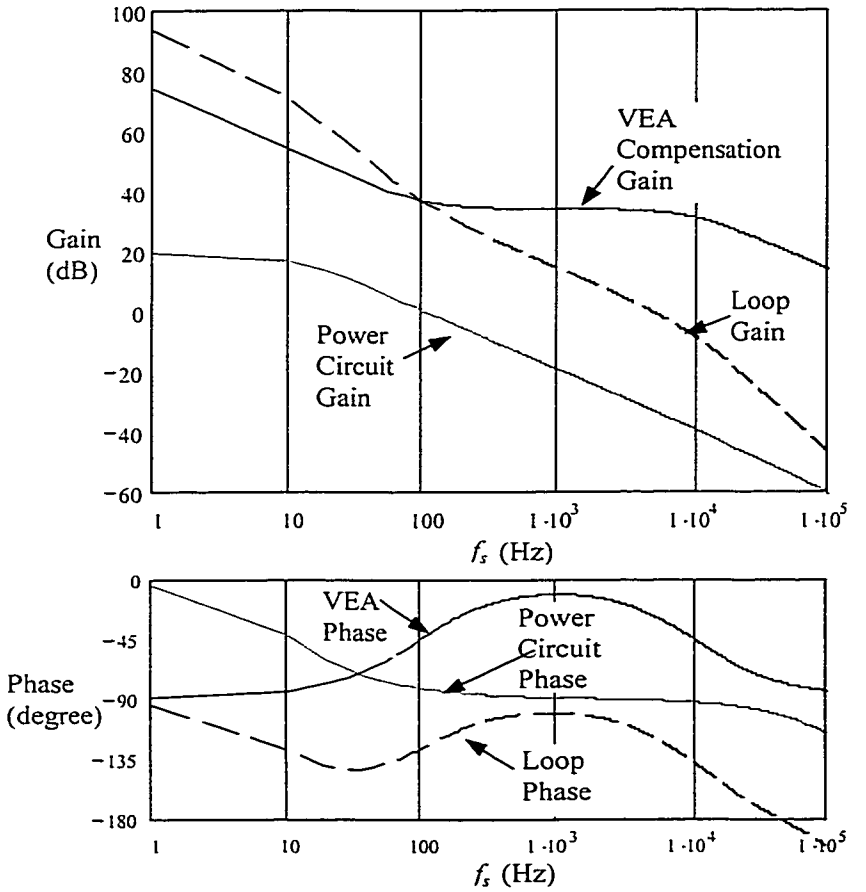


Fig. 3.7 The Bode Plot of the power circuit in PCMC and proposed compensation.

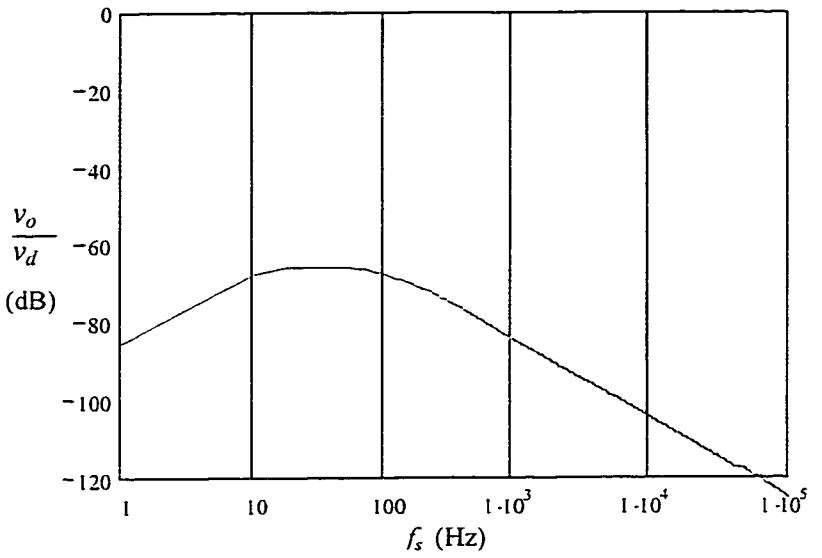


Fig. 3.8 The Bode Plot of the transfer function from the input to the output.

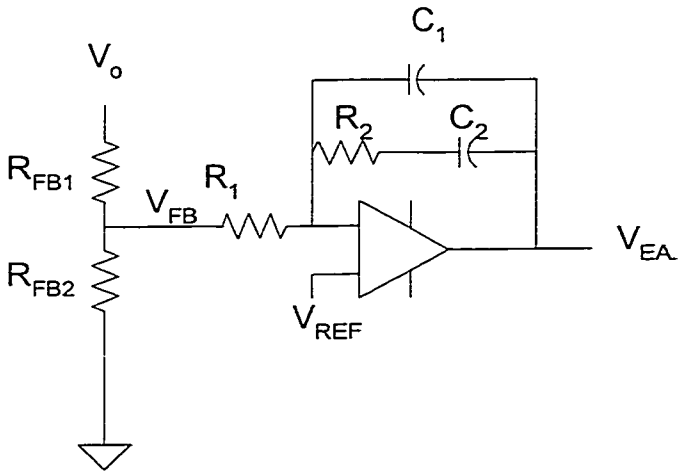


Fig. 3.9 A Type-II compensation around the error voltage amplifier.

However, even if C_s is very small, the pole and zero that it introduces are out of interest in most designs. Fig. 3.6 compares the closed current loop transfer function, namely (3-33), under two different C_s values. With the small value C_s the transfer function shows the under damped oscillation, the oscillation happens above 1 MHz. According to A. D. Middlebrook [17], the open loop crossover frequency shall be lower than one sixth the switching frequency. For a

converter switched at a few hundreds kilohertz, the oscillation frequency caused by C_s is much higher than the cross over frequency, and its effects will be well filtered out by the output filter.

Fig. 3.7 shows the Bode plot of the power circuit of prototype converter. The principle parameters of the prototype converter are listed in Tables 3.1 and 4.1.

Fig. 3.8 shows the Bode plot of the transfer function from the input to the output. It is seen that the gain of this transfer function is well below -65 dB. It means that any variations in the input voltage are well attenuated. This proves the advantages of voltage feed forward function of PCMC from another point of view: any variations in the input voltage hardly affect the output voltage.

C_s is selected 5 μF (see Sec. 4.3.4), the nominal switching frequency is 100 kHz. It is found (in MathCAD) that the zero and pole coming from the dc blocking capacitor are both near 620 Hz; thus they virtually cancel each other and become invisible. The transfer function now has only two visible poles. The first pole (around 10 Hz) is from the output filter, and the second one (around 100 kHz) comes from the closed current loop. Between these two poles the power circuit gain (from the output of EA to the output port) is attenuated by a slope of –20 dB/dec. This makes compensation around the error amplifier much easier.

Fig. 3.9 shows a Type II compensation [18] around the error voltage amplifier EA. The following components are selected for the compensation: R_{FB1}=1 MΩ, R_{FB2}=100 kΩ, R_1=200 Ω, R_2=110 kΩ, C_1=150 pF, C_2=15 nF. To target a crossover frequency at 5 kHz, the compensation around EA brings a zero at 100 Hz and two poles, one at 0 Hz and the other at 10 kHz. The pole at 0 Hz enhances the dc gain, while the second pole at 10 kHz is introduced to suppress the switching noise and also to tailor the phase margin.

Looking back at Fig. 3.7, the total open loop now meet the stability criteria: the slope of

loop gain at –20 dB/dec. around the crossover frequency (5 kHz), a phase margin of about 61°, and a gain margin of about -38 dB.

It shall be pointed out that the compensation of Fig. 3.9 shall not be considered generic. Compensation shall be adjusted according to the power circuit parameters. After all, as long as the zero and pole coming from C_s become invisible, the compensation is straightforward as elaborated in [14-16].

3.6 Simulation Results

Simulation based on the prototype converter is carried out using PSIM to verify the analysis in this chapter.

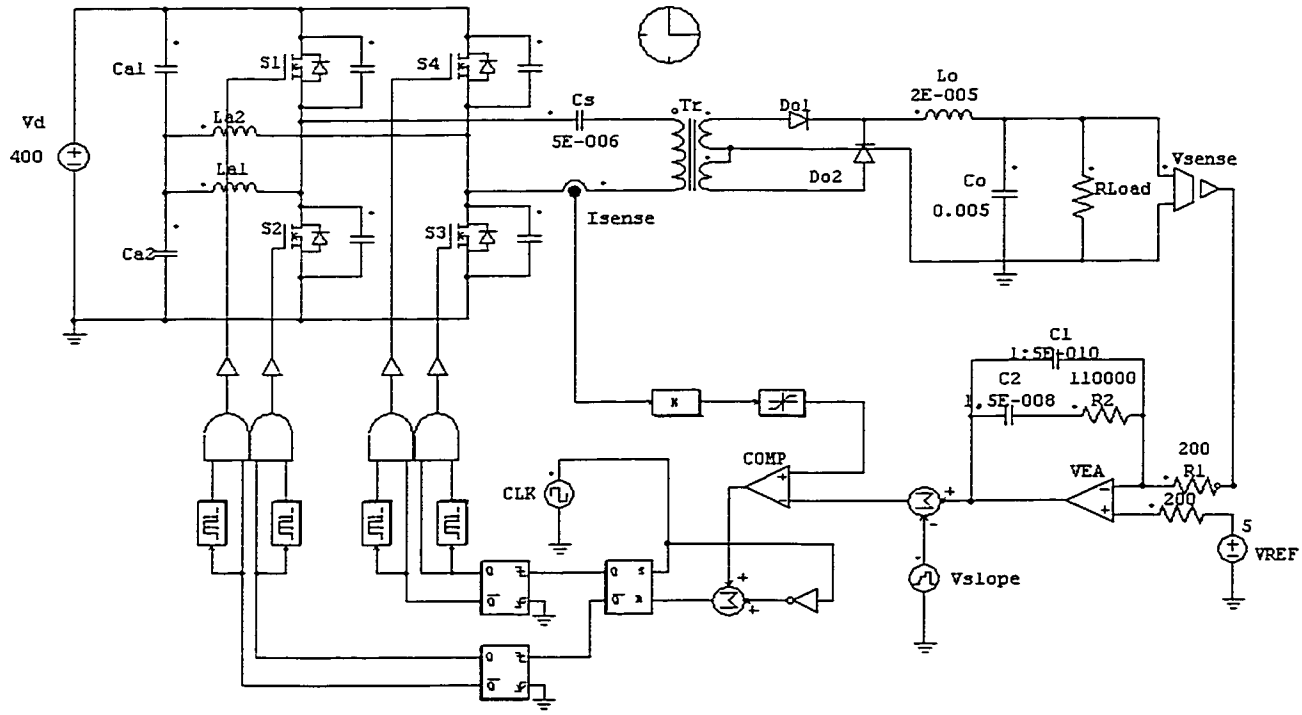


Fig. 3.10 Circuit schematic for simulation using PSIM. The feedback control is PCMC.

Table 3.1 The Asymmetrical Gating Patterns

Gating Pattern for Leg A		Gating Pattern for Leg B	
D_1	0.40	D_3	0.45
D_2	0.52	D_4	0.5
d_1	0.05	d_3	0.03
d_2	0.03	d_4	0.02

Fig. 3.10 shows the schematic for the simulation. PCMC is employed in the feedback loop. The principal parameters are defined according to Table 4.1. The current sensor is at the primary side. The slope compensation injects a slope of 1/2 times the output inductor current falling slope. The phase shift angle is determined by the positive current pulse sensed by the current sensor.

3.6.1 Flux Balancing against asymmetrical gating pattern

Fig. 3.11 shows the asymmetrical gating patterns on all four switches. This asymmetry is exaggerated in this simulation to demonstrate the problems it causes. Table 3.1 shows this asymmetry. From (3-6), the dc voltage arising from this asymmetry is –36 V when V_d = 400 V.

Fig. 3.12 shows the spectrum of the bridge output voltage. A dc voltage component of 36.0 V is resulted from the gating asymmetry. This dc voltage will saturate the current transformer if it is not blocked.

Fig. 3.13 shows the effects of inserting the series dc blocking capacitor C_s. Because of C_s, the power transformer primary voltage V_p is shifted such that it gets rid of the dc voltage component. When the load is 55 V 15 A (0.825 kW), the ripple voltage on the capacitor is about 2.72 V peak to peak for a capacitor value of 5 μF.

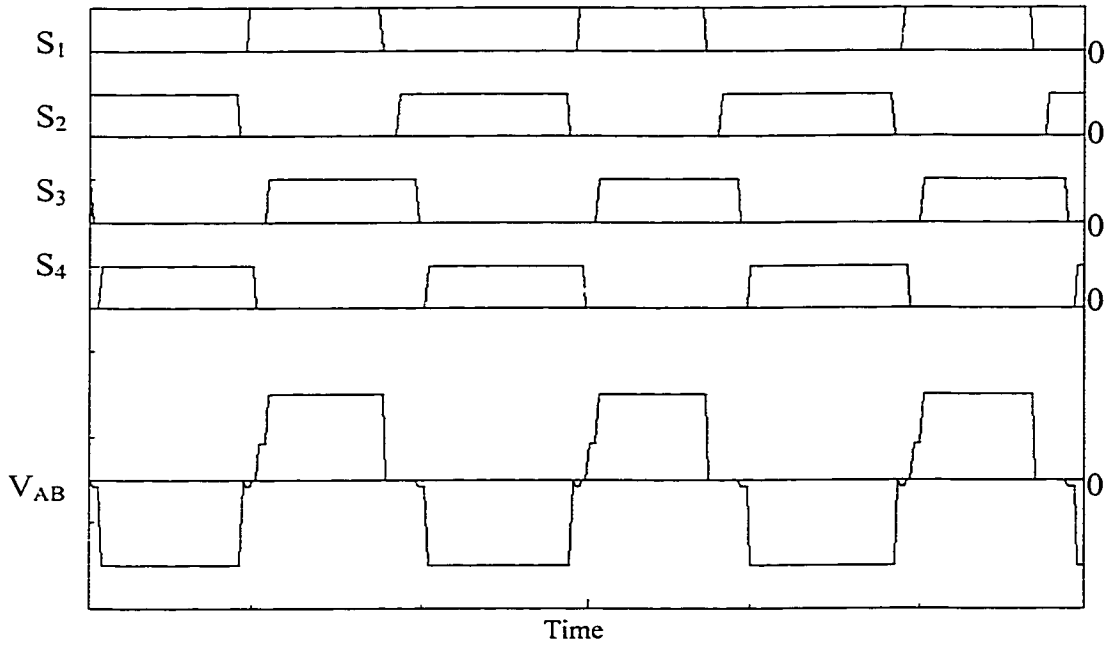


Fig. 3.11 Asymmetrical gating and the output voltage of the two bridge legs, V_{AB}.

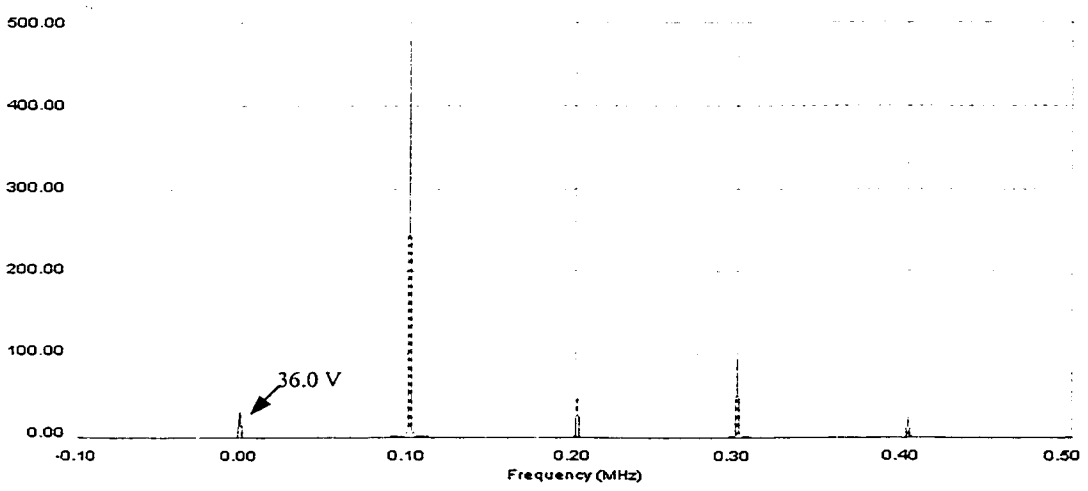


Fig. 3.12 Spectrum of the bridge output voltage V_{AB} shown in Fig. 3.11. The transformers see this voltage

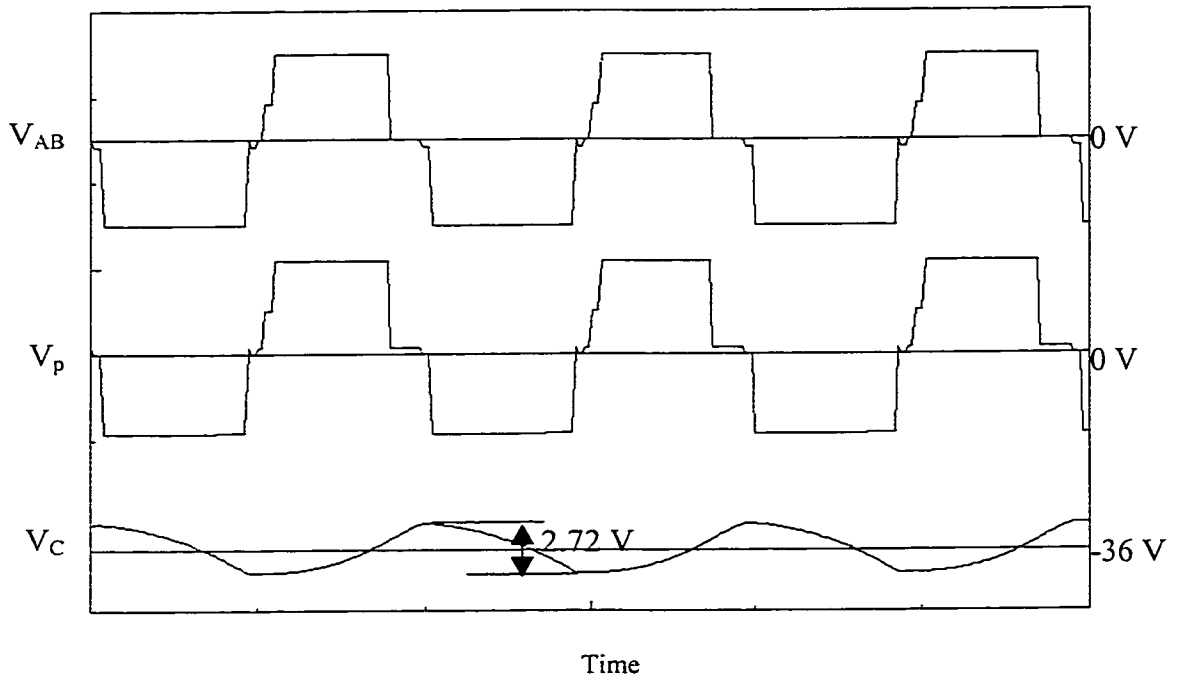


Fig. 3.13 Effects of the series dc blocking capacitor C_s. The bridge output voltage seen after the series dc blocking capacitor is shifted up by V_{dc}. Load current is 15 A.

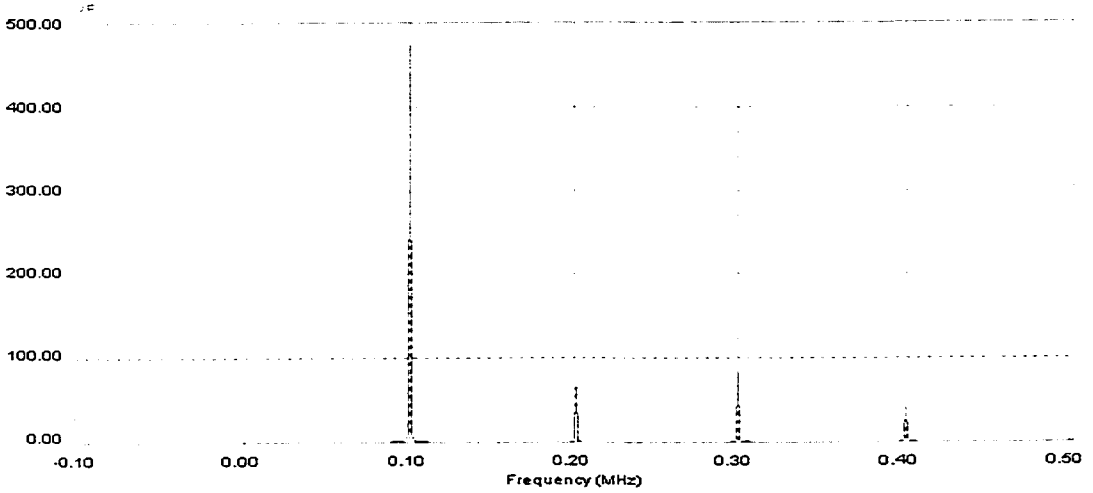


Fig. 3.14 Spectrum of the bridge output voltage seen by the transformers after the dc blocking capacitor C_s. The dc component is removed completely.

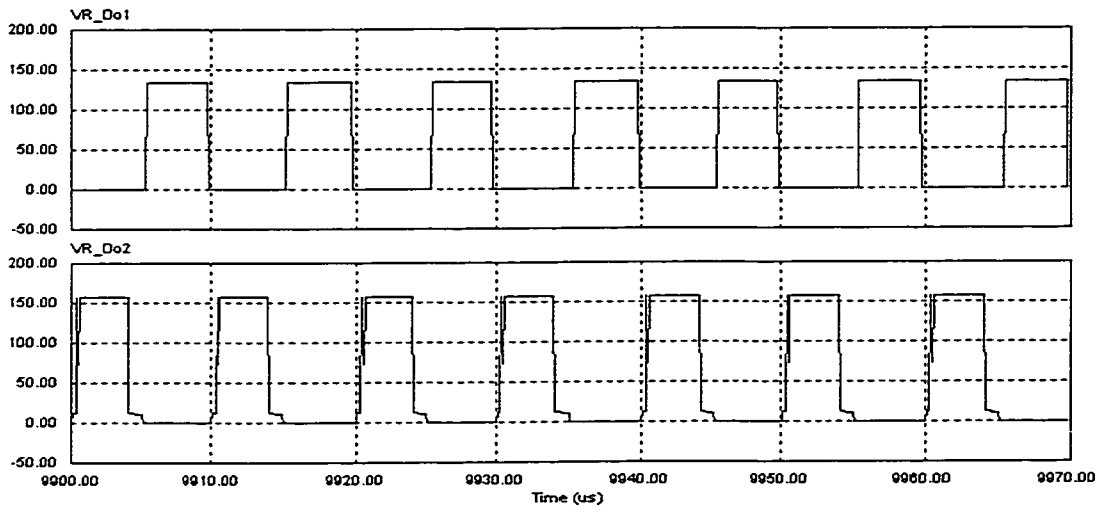
Fig. 3.14 shows the spectrum of the bridge output voltage seen after the dc blocking capacitor. As seen, it is dc component free. This guarantees the flux balancing in the current sense transformer and prevents it from saturation.

3.6.2 Other influences of the dc blocking capacitor

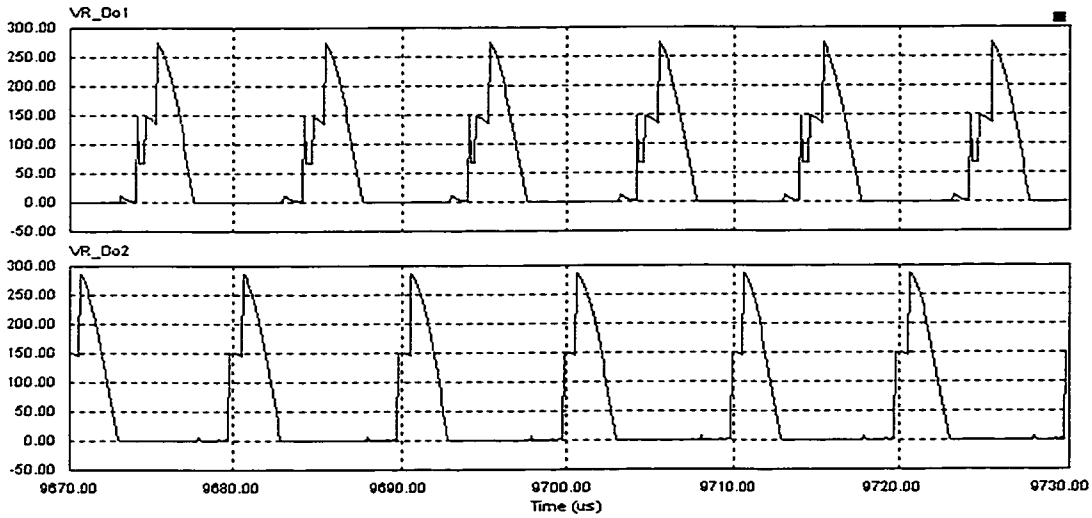
Fig. 3.15 shows influences of the value of the dc blocking capacitor on the reverse voltage stress of the rectifier diodes. It is clearly seen that one of the diode suffers from higher reverse voltage stress when gating asymmetry exists. It also shows that a smaller capacitor will adversely increase the reverse voltage stress on both diodes and may easily break them down.

Fig. 3.16 shows the secondary current under the influence of the dc blocking capacitor. It shows that the output inductor current will have alternative ramps, owing to the shifted dc voltage level by the dc blocking capacitor. The waveforms of the currents through the two diodes are no longer symmetrical. However, their average current is equal to each other, due to the dc blocking of the capacitor C_s. That means, the conduction losses on the diodes do not change.

Fig. 3.17 shows the ZVS operation under the influence of the dc blocking capacitor. It shows that, even under the exaggerated gating pattern asymmetry, ZVS is still achieved.



(a) The reverse voltage stress on the rectifier diodes when $C_s = 5$ μF.



(b) The reverse voltage stress on the rectifier diodes when $C_s = 5$ nF.

Fig. 3.15 Influences of the value of the dc blocking capacitor on the reverse voltage stress of the rectifier diodes. A smaller capacitor adversely increases the reverse voltage stress.

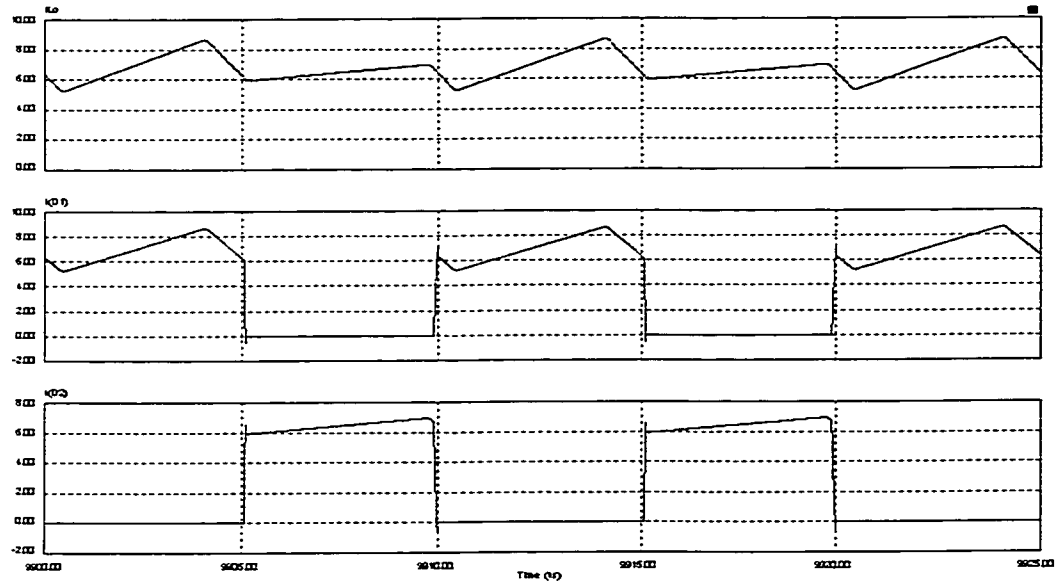


Fig. 3.16 Influences of the dc blocking capacitor on secondary currents. Load power 500 W.

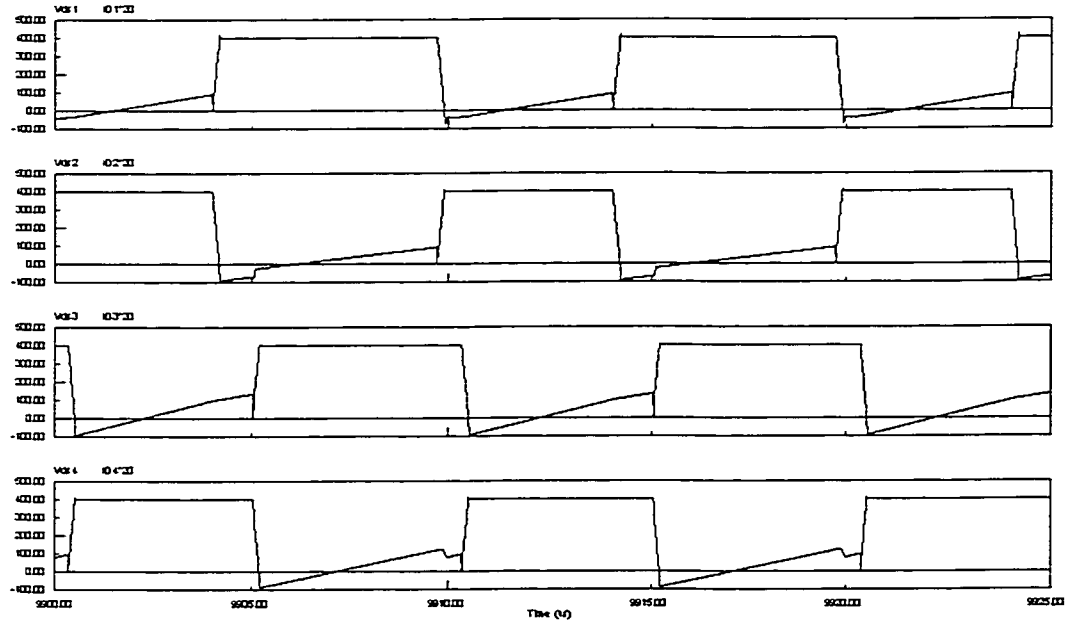


Fig. 3.17 Influences of the dc blocking capacitor on ZVS switching.

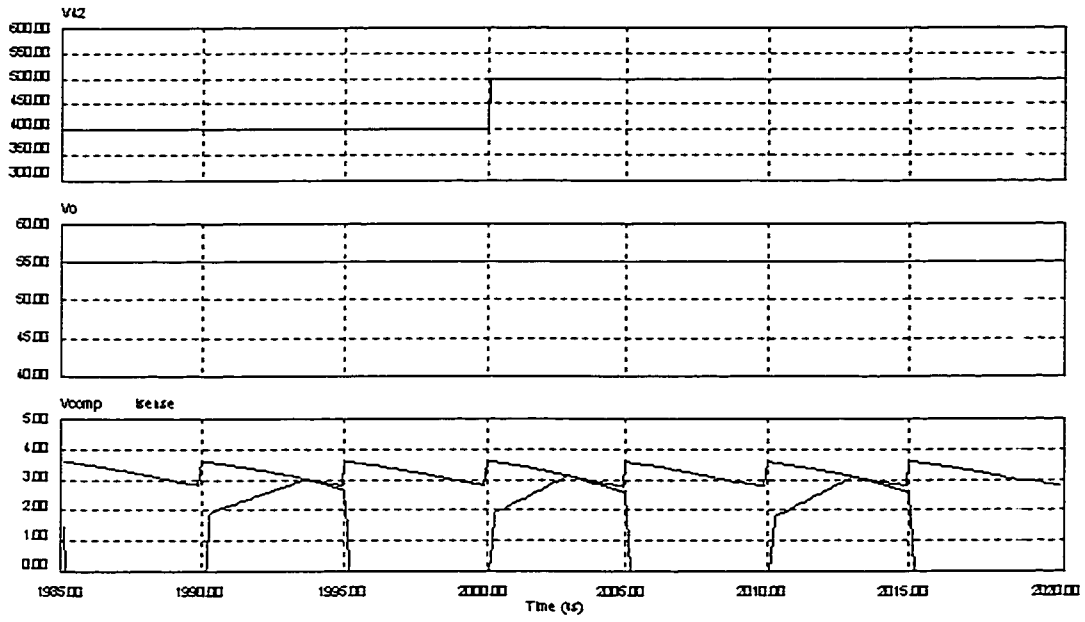
3.6.3 Step Responses

Fig. 3.18 shows converter response to step changes in the input voltage. The steps are exaggerated in this simulation to demonstrate the control signal variations. It is seen that the PCMC circuit adjusts itself immediately, because the sudden change of the sensed current slope arising from the input voltage step changes. Consequently, the output voltage is hardly affected, neither when the input voltage steps up nor when it steps down.

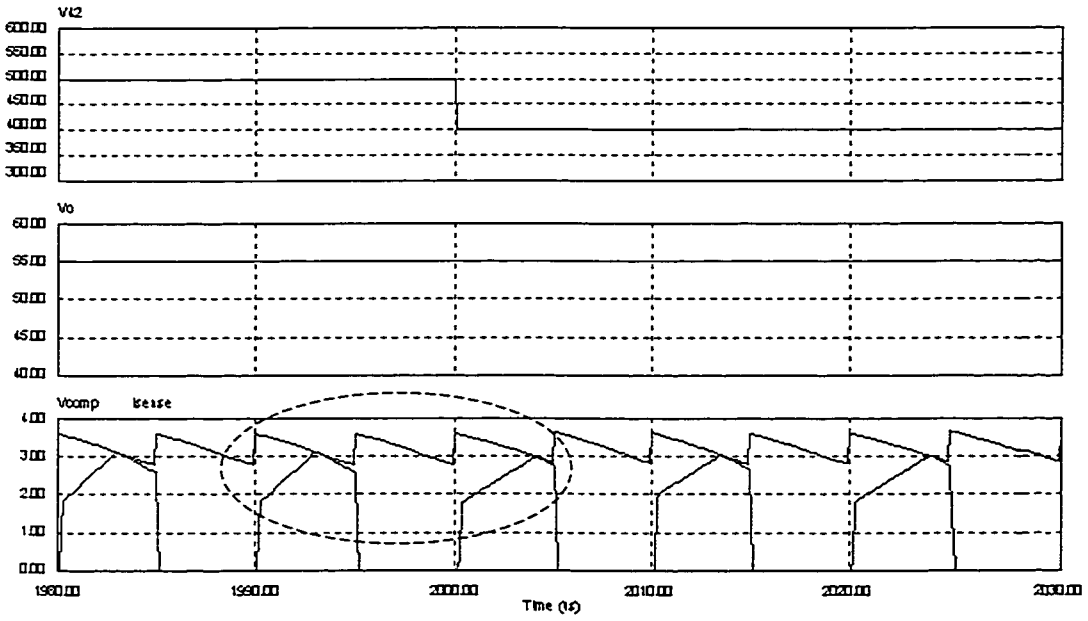
Fig. 3.19 and Fig. 3.20 show the converter response to the step load between 6 A to 26 A. It is seen that the output voltage transient is a well damped response, and it recovers its regulation point (55 V) within 1 ms. This confirms with the loop design. The control signal shown in the detailed views also verify the PCMC design in simulation circuit.

3.6.4 DC blocking series capacitor voltage under dynamic conditions

Fig. 3.21 and Fig. 3.22 show voltage across the dc blocking capacitor as well as the magnetizing current and the primary current under step load conditions. The magnetizing current of the current sense transformer is proportional to that of the power transformer. It is seen that, the voltage across the dc blocking capacitor undergoes a transient following exaggerated large load step changes (between 6 and 26 amperes). However, the capacitor voltage does not permanently run away under these dynamic conditions, and it enters a new steady state after about 0.5 ms under such a large step load transient. It is seen that the magnetizing current is also stable and its transient completes in less than 0.2 ms.

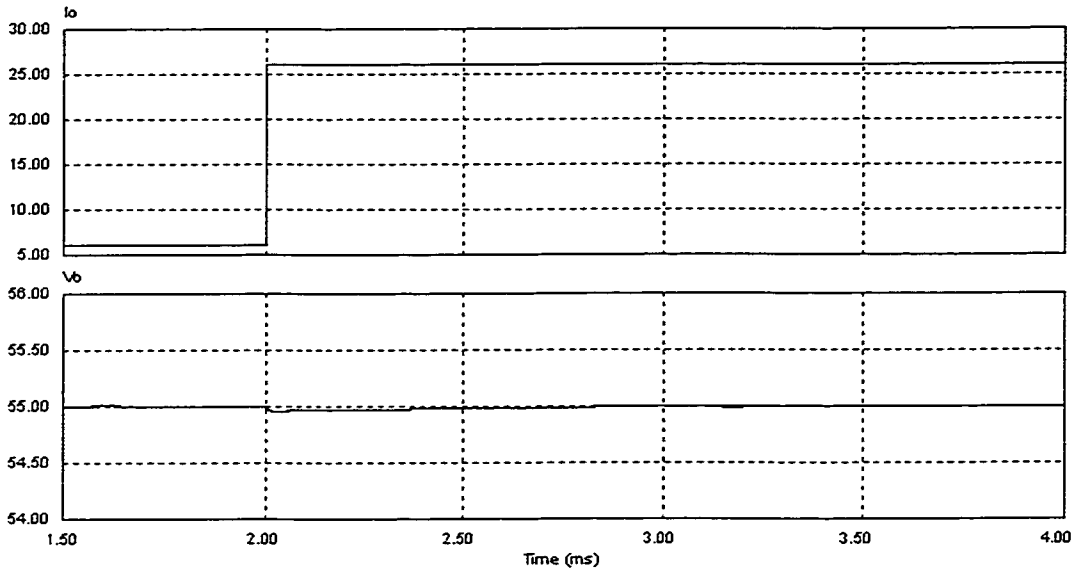


(a) Input voltage steps up from 400 V to 500 V. Load power 500 W.

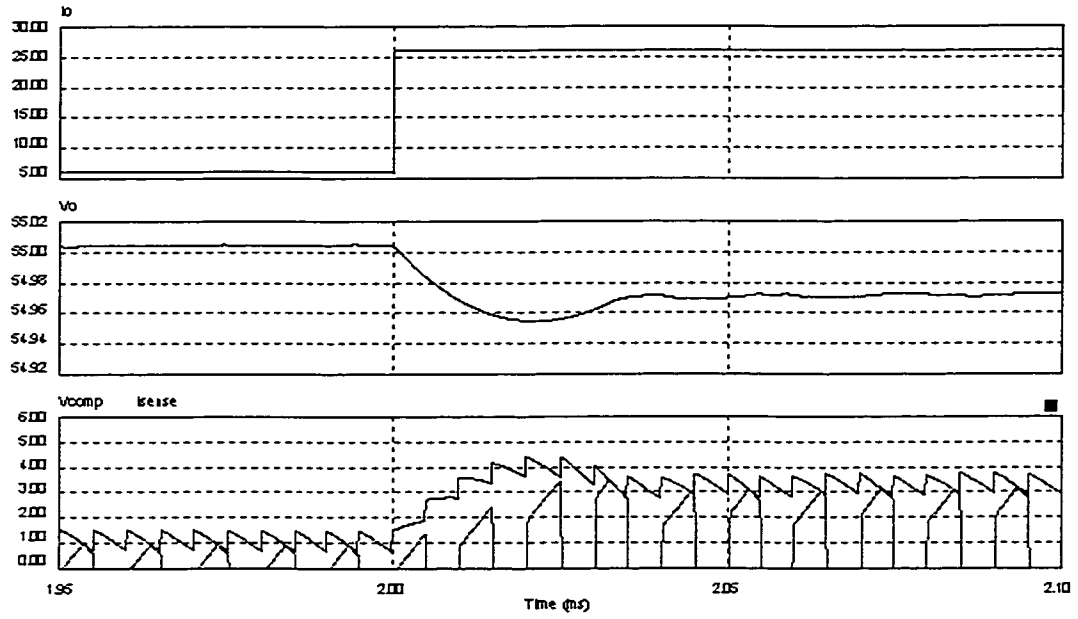


(b) Input voltage steps down from 500 V to 400 V. Load power 500 W.

Fig. 3.18 Input voltage step responses. The steps are exaggerated in this simulation.

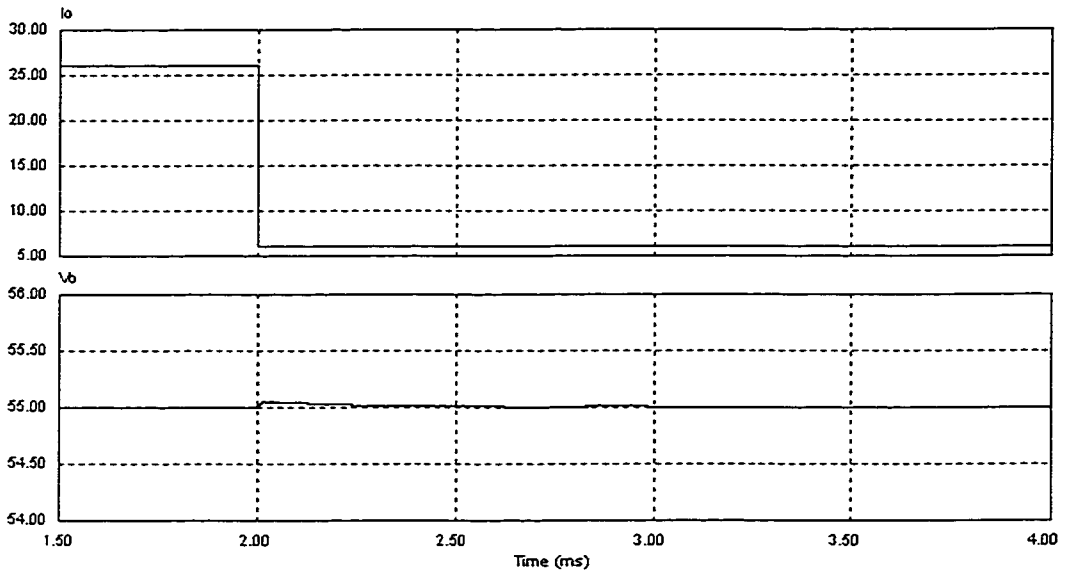


(a) Output current steps up from 6 A to 26 A. Overview.

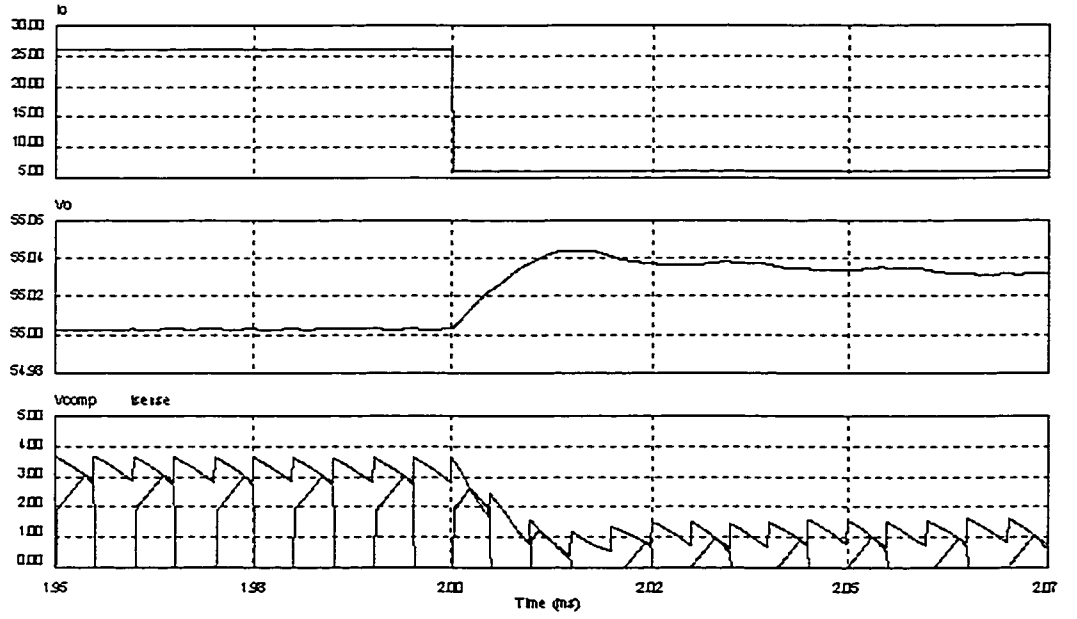


(b) Detailed view of the output current step up and the control signals.

Fig. 3.19 Converter responses to load current stepping up, and the control signal variations.



(a) Output current steps down from 26 A to 6 A. Overview.



(b) Detailed view of the output current step down and the control signals.

Fig. 3.20 Converter responses to load current stepping down, and the control signal variations.

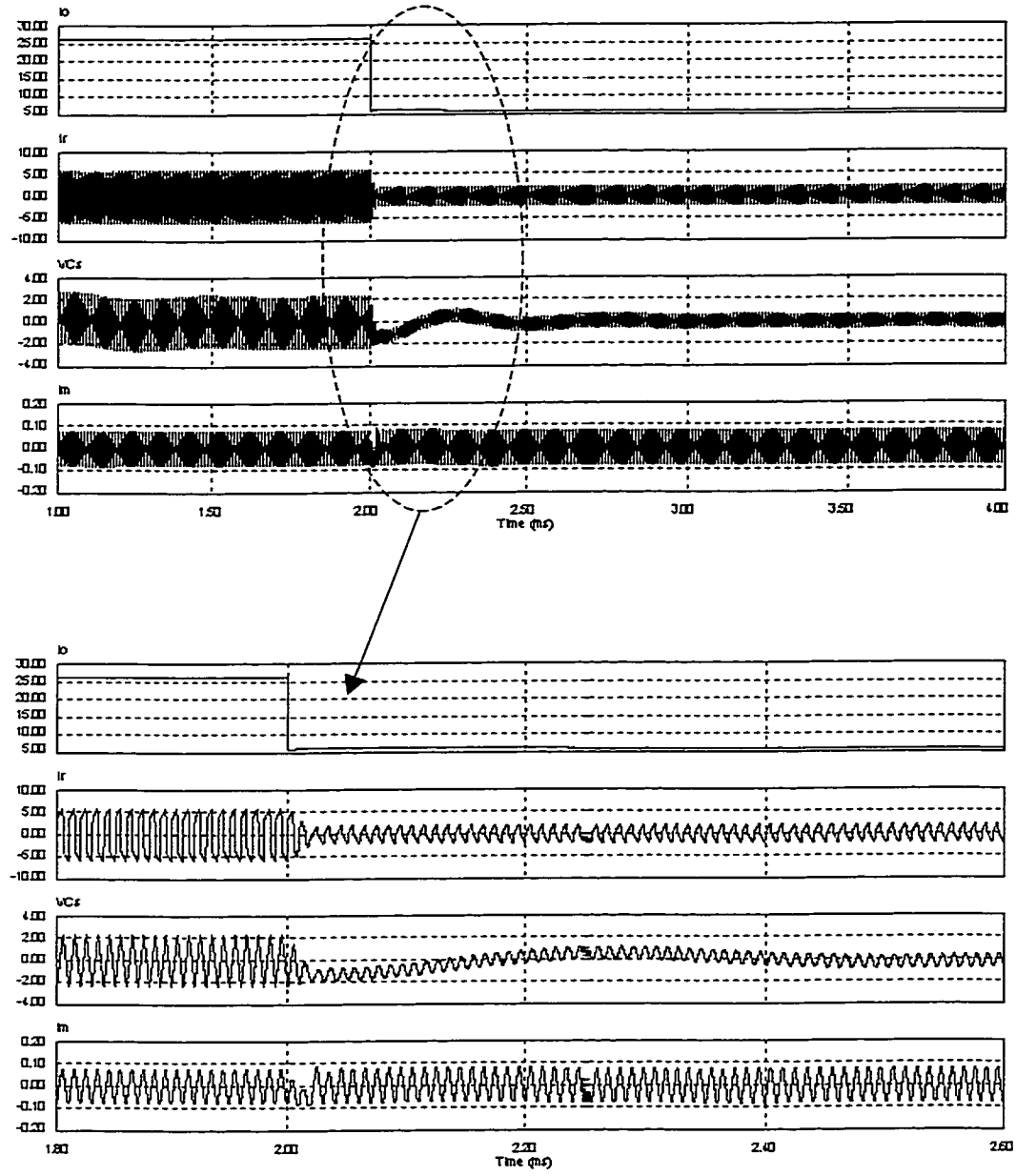


Fig. 3.21 Magnetizing current and dc blocking capacitor voltage under load down step. Overview and detailed view

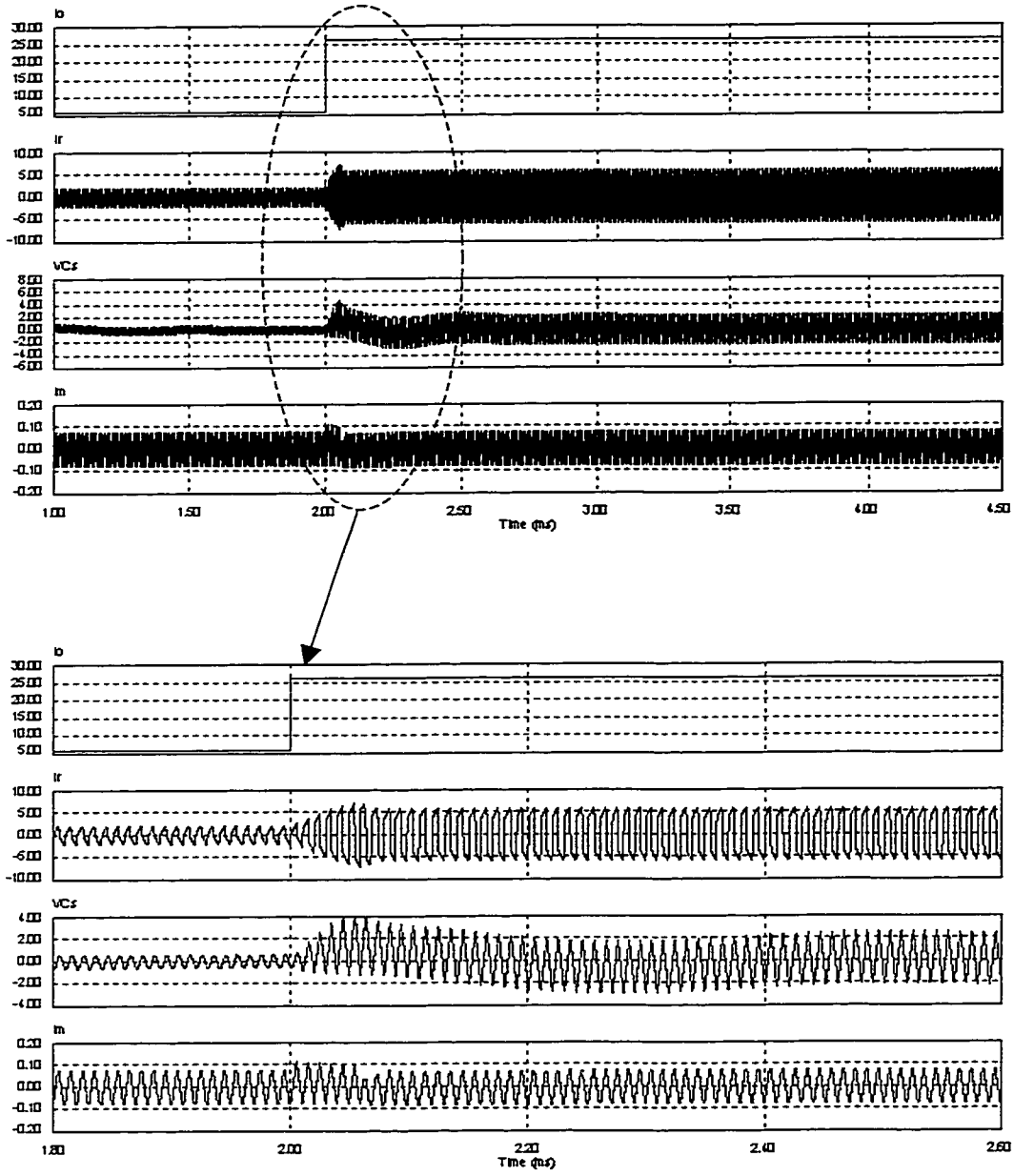


Fig. 3.22 Magnetizing current and dc blocking capacitor voltage under load up step. Overview and detailed view.

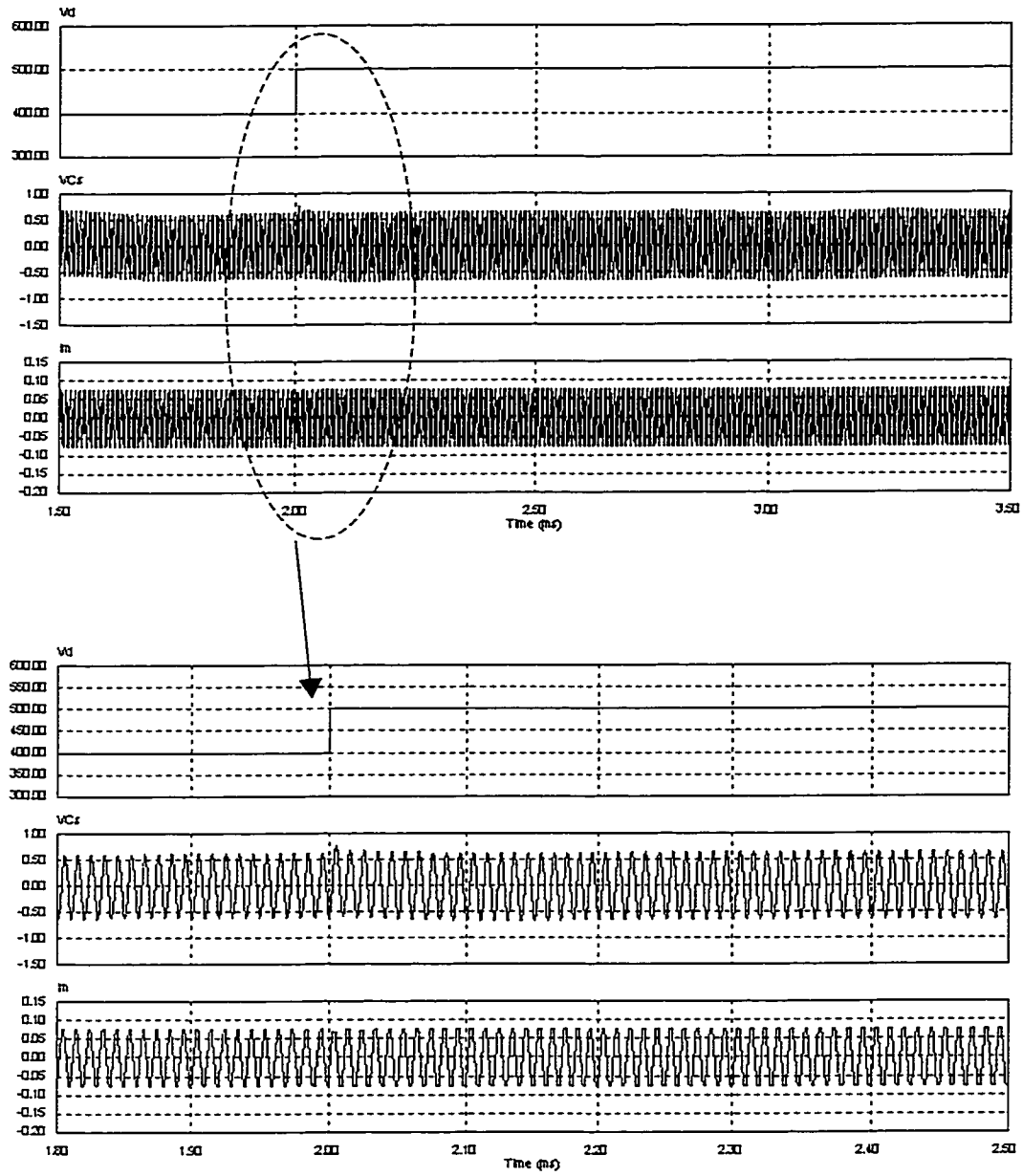


Fig. 3.23 Magnetizing current and dc blocking capacitor voltage under input voltage up step. Overview and detailed view.

Fig. 3.23 shows voltage across the dc blocking capacitor as well as the magnetizing current and the primary current under input voltage step change. It is seen that the changes in the input voltage hardly affect these variables, except for a slight and fast transient of the capacitor

voltage immediately following the step. This is because of the PCMC directly adjusts the phase shift angle within one cycle, and leaves the gating asymmetry to be insignificant and negligible.

3.7 Conclusions

The following conclusions can be made:

(i) The gating pattern of the bridge switches is hardly purely symmetrical in a real circuit, and this asymmetry will saturate the current sense transformer if it does not saturate the power transformer.

(ii) The current sense transformer saturation can be easily prevented by employing a small dc blocking capacitor in series with the power transformer and the flux excursion in the current sense transformer as well as the power transformer will be balanced.

(iii) The small signal model is established and the transfer function for the peak current mode control has been derived for general application. It is found that the presence of the dc blocking capacitor has little visible effects on the power circuit transfer function.

(iv) Simulation is carried out and the simulation results verify the analysis and design. And the converter is dynamically stable.

CHAPTER 4

DESIGN PROCEDURE

4.1 Introduction

This chapter presents a design procedure of the auxiliary circuit for the proposed ZVS full bridge converter topology for general purpose applications. As seen from the previous chapters, the proposed topology is simply a combination of a conventional full bridge converter, an auxiliary circuit and a dc blocking capacitor. Because the design for the conventional full bridge converter has already been well addressed in the literature, this chapter will only discuss the optimal design of the auxiliary circuit and the selection of the dc blocking capacitor.

It has been emphasized in the previous chapter that the gating pattern is hardly purely symmetrical and without treatment, it would eventually drive the current sense transformer into saturation. However, unlike the exaggerated gating asymmetry in Chapter 3, this asymmetry is unnoticeable over the short time in a real circuit. The commercial products of phase shift PWM controllers in today's market shows very subtle gating asymmetry. UC1879 from Unitrode, for example, displays a typical gating asymmetry for about 100 ns or 1% of a switching cycle at 100 kHz [20]. All this means that the design procedure can be safely derived according to the steady state analysis in Chapter 2, as long as the dc blocking capacitor is employed to treat the gating asymmetry problem.

It will be revealed in Sec. 4.2 that an asymmetrical auxiliary circuit for the two bridge legs will be advantageous in optimizing the design. The benefits from the asymmetry in the auxiliary circuit will reduce the conduction losses arising from the circulating current in the auxiliary circuit. It also reduces the size and weight of the auxiliary inductors. Hence

asymmetrical auxiliary circuit will improve the overall efficiency of the converter and minimize its total weight and costs.

In Sec. 4.3 the design procedure is presented based on the analysis in the previous chapters. In Sec. 4.4 a design example is given. A prototype circuit based on the design example is built to prove the concepts of this thesis.

4.2 Optimizing the Design by Employing the Asymmetrical Auxiliary Circuit

The following discussion is under the assumption that Leg A in Fig. 2.1 or Fig. 3.2 is the leading leg, i.e., the gating of the switches on Leg A is always coming ahead of the gating of pertinent switch on Leg B which is the lagging leg.

It is understood that the auxiliary inductors are essentially required in the proposed topology to achieve ZVS turn-on of the switches, by providing the current to discharge the snubber capacitor that may be a combination of both external snubber capacitor and the MOSFET internal capacitor or the internal capacitor alone.

Particularly, to successfully discharge the snubbers for Leg A within the switching dead time t_d, the discharging current is required to be

$$I_{A\_discharge} \geq \frac{C_{sb1,2} V_d}{t_d} \tag{4-1}$$

and for Leg B, it is required to be

$$I_{B\_discharge} \geq \frac{C_{sb3,4} V_d}{t_d} \tag{4-2}$$

From (2-3), (2-7), (2-9) and (2-11), the discharging current for switches on Leg A has a magnitude determined by

$$I_{A\_discharge} = \frac{V_d}{8L_{a1}}\left(\frac{1}{2f_s} - t_d\right) + \frac{1}{2k}\left[I_o + \frac{(V_d - kV_o)V_o}{4f_s V_d L_o}\right] \tag{4-3}$$

Similarly from (2-18), for the switches on Leg B, it has a magnitude determined by

$$I_{B\_discharge} = \frac{V_d}{8L_{a2}}\left(\frac{1}{2f_s} - t_d\right) - \frac{1}{2k}\left[I_o - \frac{(V_d - kV_o)V_o}{4f_s V_d L_o}\right] \tag{4-4}$$

It is seen that the load current, or more accurately, the output inductor current, assists the auxiliary current flowing through L_{a1} in discharging the snubber capacitor on Leg A, while it counteracts the auxiliary current through L_{a2} in discharging the snubber capacitor on Leg B.

For some designs, the dead time is fixed and limited to be very short by the chosen commercial controller products. In such cases, the external snubber capacitor should be small or maybe not even be used. Otherwise high discharging currents would be required to achieve ZVS turn-on, as seen from (4-1) and (4-2). Now all the snubber capacitors are only the inherent capacitors of the MOSFET switches and they are almost the same in value. Therefore as seen from (4-1) to (4-4), L_{a1} is not necessarily required to provide a discharging current as high as should L_{a2} do. Considering the auxiliary current results in conduction losses, L_{a1} can be selected to be larger than L_{a2} to reduce the auxiliary current and thus to reduce the conduction losses. This leads to the asymmetry of the auxiliary circuit.

The asymmetrical auxiliary circuit should be chosen from another point of view:

It is noticed that when one switch on a leg is turned off, its snubber capacitor is charging up. Specifically, (2-9) shows the current stress on S_2 when it is turned off at the beginning of Interval 1 each switching cycle. S_1 sees the same current stress at the beginning of Interval 5. Substituting (2-3) and (2-7) into (2-9), the turn-off current stress on the switches of Leg A (the leading leg) is determined by

$$I_{A\_sw\_off} = \frac{V_d}{4L_{a1}}\left(\frac{1}{2f_s} - t_d\right) + \frac{1}{k}\left[I_o + \frac{(V_d - kV_o)V_o}{4f_s V_d L_o}\right] \quad (4\text{-}5)$$

Similarly as seen from Sec. 2.3.2.C, each switch on Leg B (the lagging leg) sees the following current stress when it is turning off:

$$I_{B\_sw\_off} = \frac{V_d}{4L_{a2}}\left(\frac{1}{2f_s} - t_d\right) - \frac{1}{k}\left[I_o - \frac{(V_d - kV_o)V_o}{4f_s V_d L_o}\right] \quad (4\text{-}6)$$

Equations (4-5) and (4-6) indicate that when the auxiliary circuit is in symmetry, i.e., $L_{a1} = L_{a2}$, the switches on Leg A suffer from a higher turn-off current stress than those on Leg. B.

Should ZVS turn-off be successful in all four switches, the snubber for each switch on Leg A should have a higher capacitance than that for each switch on Leg B, so as to limit the dv/dt of its drain-to-source voltage to be below a certain level. By keeping the dv/dt low, the circuit will greatly reduce the overlap of the dropping drain current and the rising drain-to-source voltage, so that a ZVS turn-off is achieved. Obviously a larger capacitor is required to slow down the rising of the drain-to-source voltage of the switch under a higher current stress.

Now that there is a difference in the turn-off current stress for the switches on different legs, the snubber capacitors for Leg B switches are not necessarily as large as those for Leg A switches. Again, this shows the reason to employ the asymmetrical auxiliary circuit.

In summary, choosing the asymmetrical auxiliary circuit will optimize the design.

4.3 Design of the Auxiliary Circuit

4.3.1 Assumptions

The following are assumed to be known:

(i) The design of the power circuit, namely L_o, C_o, k, etc.

(ii) I_o, full load current

(iii) $V_{d\max}$ and $V_{d\min}$, input dc voltage range

(iv) V_o, nominal output voltage

(v) f_s, switching frequency

(vi) $D_{\max}$, maximum duty ratio

(vii) t_d, switching dead time

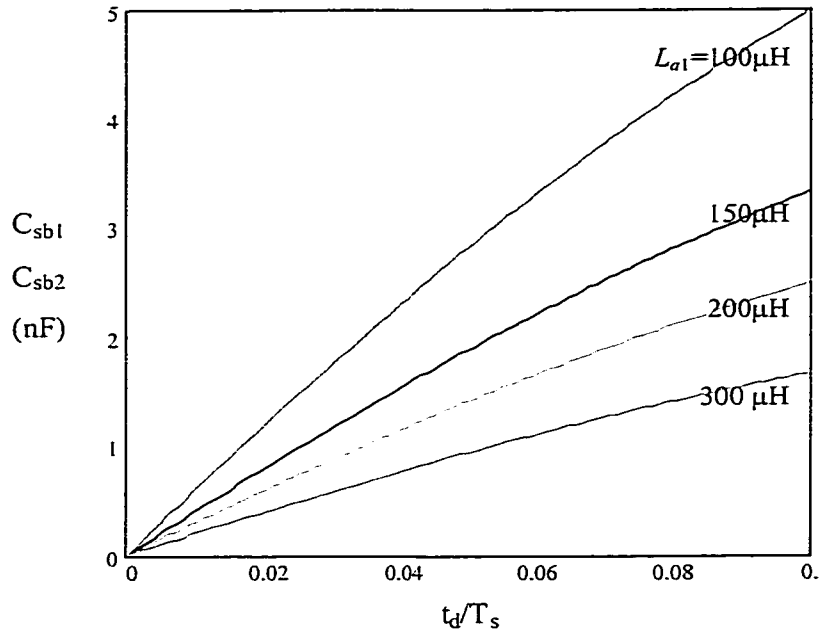
4.3.2 Selection of L_{a1}, L_{a2}, C_{sb1}, C_{sb2}, C_{sb3} and C_{sb4}

To achieve ZVS turn on, the snubber capacitors shall be completely discharged within the dead time t_d, under all operating conditions. Because the auxiliary inductors determine the values of the discharging currents, and the required discharging currents are determined by snubber capacitors, thus the selection of the auxiliary inductors and the snubber capacitors are correlated.

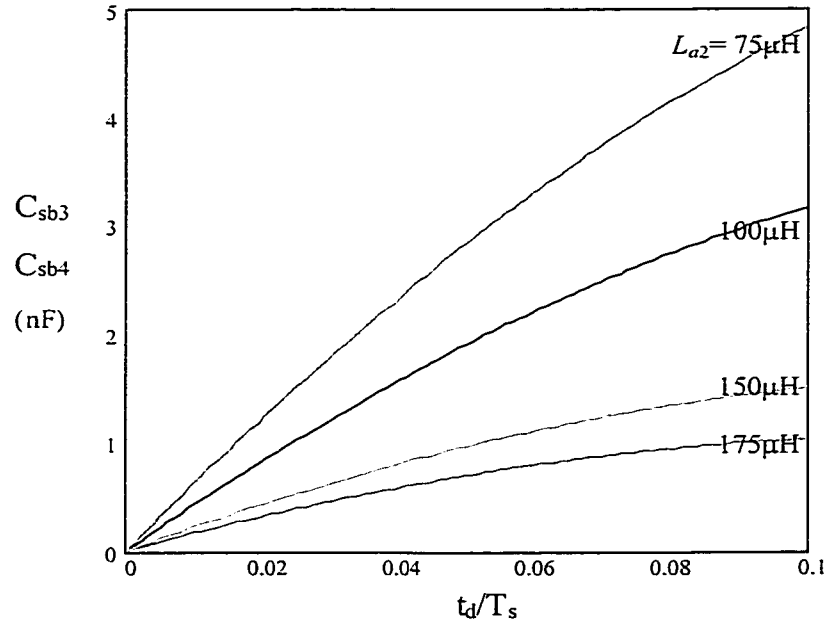
Seen from (4-1) and (4-3), to guarantee the complete discharge of the snubber capacitors for Leg A under all line and load conditions, the following equation shall be satisfied.

$$C_{sb1} = C_{sb2} \le \frac{t_d}{8L_{a1}}\left(\frac{T_s}{2} - t_d\right) \tag{4-7}$$

As mentioned previously, the load current assists the auxiliary current to discharge snubber capacitors on Leg A. When (4-7) is satisfied even under no load condition which is the worst case for Leg A switches, the Leg A snubbers can still be completely discharged, not to mention under full load. It is also seen that ZVS on Leg A is inherently independent of the input voltage.



a. C_{sb1} and C_{sb2} vs. t_d and L_{a1}



b. C_{sb3} and C_{sb4} vs. t_d and L_{a2}

Fig. 4. 1 The example design curves for selecting the auxiliary inductors and the permitted maximum snubber capacitors. f_s=100 kHz, V_d=350-400 V, V_o=55V, k=5.5:1, L_o=20 μH, and full load at 500 W.

Similarly, from (4-2) and (4-4), for Leg B, the following equation must be satisfied.

$$C_{s-b3} = C_{sb4} \le \frac{t_d}{8L_{a2}}(\frac{T_s}{2} - t_d) - \frac{t_d}{2kV_{d\min}}(I_o - \frac{V_{d\min} - kV_o}{4V_{d\min} f_s L_o} V_o) \tag{4-8}$$

It is seen that the load current counteracts the auxiliary current to discharge the snubbers on Leg B. As (4-8) is satisfied at the minimum input voltage and full load which is the worst case, the snubber will be discharged under all other operating conditions. In this way ZVS for Leg B will also become independent of line and load conditions.

Fig. 4. 1 shows an example of the selection curves of the snubber capacitors as functions of t_d and the auxiliary inductors. It is seen that for a dead time of 400 ns when all the snubbers are selected to be 1 nF, the auxiliary inductor for Leg A or the leading leg, shall be about 200 μH, while that for the lagging leg (Leg B) shall be 100 μH.

4.3.3 Selection of C_{a1}, C_{a2}, the capacitor type voltage divider

The two capacitors are employed to establish and hold almost dc voltages with little ripples for the proper operation of the auxiliary circuit. Assume the permitted ripple voltage on these two capacitors is about 2 % of the input line voltage, then approximately they are:

$$2\% \cdot \frac{C_{a1} + C_{a2}}{2} V_d \ge \frac{1}{2} |I_{a2} - I_{a1}| \frac{T_s}{2} \tag{4-9}$$

Substituting (2-7) and (2-8) into (4-9), and considering C_{a1}=C_{a2}, then (4-9) yields:

$$C_{a1} = C_{a2} \ge \frac{1}{2\%} \cdot \frac{|L_{a1} - L_{a2}|}{32 f_s^{\,2} L_{a1} L_{a2}} \tag{4-10}$$

In the example, these two capacitor values shall be greater than 0.8 μF and 1 μF capacitors are selected for the prototype converter..

4.3.4 Selection of C_s, the DC voltage blocking capacitor

As discussed in Chapter 3, the major problem with the dc blocking capacitor is that it increases the reverse voltage stresses on the output rectifier diodes. As the dc voltage component is usually low because of the slight gating pattern asymmetry in a real circuit, the ac voltage ripples on the dc blocking capacitor are the major concerns for the increased voltage stress.

The peak reverse voltage stress on the rectifier diodes happens at the end of their duty ratio. It is the moment the capacitor is fully charged by the load current. Thus the maximum increased voltage stress is approximately determined by

$$\Delta V_r = \frac{I_o}{f_s k^2 C_s} \tag{4-11}$$

This increase of the voltage stress shall be limited to prevent the diode from breaking down. In the example circuit given below, assuming this increase is below 10 V, (4-11) yields a capacitor value of 0.33 μF. To further suppress the increased voltage stress, a 5 μF capacitor is actually selected in the prototype converter.

4.4 A Design Example

According to the design criteria given in this chapter, an example circuit (the prototype) is designed. The principal parameters and selected devices are listed in Table 4.1.

Table 4.1 Example Circuit

parameter	value	parameter	value/device
$V_{d\min}/V_{d\max}$	350 V/400 V	C_{a1}, C_{a2}	1 μF, each
V_o	55 V	C_{sb1}, C_{sb2} C_{sb3} and C_{sb4}	1 nF, each
I_o	10 A	L_{a1}/L_{a2}	200 μH/100 μH
k	5.5:1	C_s	5 μF
L_o/C_o	20 μH/5000 μF	S_1, S_2, S_3, S_4	IRFP460
t_d	400 ns	D_{o1}, D_{o2}	MUR3020

CHAPTER 5

SUMMARY AND CONCLUSIONS

5.1 Summary

A line and load independent ZVS full bridge dc/dc converter topology employing asymmetrical auxiliary circuits has been presented and analyzed in this thesis. By achieving ZVS under all operating conditions, the overall conversion efficiency has been enhanced, the thermal problems on the switches are relieved, and the switching frequency can be further increased to reduce the converter's physical size. Therefore high efficiency and high power density can be achieved.

This work can be summarized as follows.

In Chapter 1, the conventional ZVS full bridge dc/dc converter topologies are reviewed. There are typically two approaches to achieve ZVS. The first is the passive approach, and the second one the active approach. It is found that the passive approach can only achieve ZVS conditionally, and it could lose ZVS at light load or over load conditions, while the active approach is too complicated for applications of power level below 3 kW.

In Chapter 2, a line and load independent ZVS full bridge dc/dc converter topology is presented. It is derived from the conventional active approach, but simplified by employing passive components only. The operating principle is described and the steady state analysis is performed. It is found that ZVS can be achieved under all operating conditions. The analysis is verified with simulation and experimental results on a 128 kHz, 500 W, 400 V to 55 V prototype converter. More than 97 % overall efficiency is obtained at full load in the prototype.

In Chapter 3, the dynamic properties of the proposed topology are explored. It is noticed

that a small dc blocking capacitor is essentially required to prevent the current sense transformer from saturating. It also is also shown that unlike in a conventional PWM full bridge converter, PCMC can be still used along with such a dc blocking capacitor in a phase shifted full bridge converter. Small signal model of the topology is derived based on the averaged state space equations. Simulation results are presented to verify the analysis and design.

In Chapter 4, the asymmetrical auxiliary circuit for two different bridge legs is proposed to optimize the design. By using asymmetrical auxiliary circuits, the conduction losses resulting from the circulating currents in the auxiliary circuit are minimized, further enhancing the overall efficiency. A design procedure is developed, and component selection curves and criteria are presented for the general purpose applications, and an example is given.

5.2 Conclusions

The following conclusions can be drawn.

(i) The proposed topology is simple and it achieves ZVS independent of line and load conditions. It only involves two inductors, two dc capacitors and four snubber capacitors. In some applications the snubber can be the MOSFET inherent capacitance, which further simplifies the design.

(ii) The control as well as the power circuit design is nothing more than the conventional full bridge converter. This minimizes the development time and facilitates its application.

(iii) Asymmetrical auxiliary circuits should be employed to minimize the conduction losses arising from the current in the auxiliary circuits. This helps to increase the overall efficiency.

(iv) The addition of a small dc blocking capacitor will prevent the current sense transformer

from saturating. This in turn relaxes the design of the gate drive circuit in achieving gating pattern symmetry, because asymmetrical gating pattern can now be easily handled by the dc blocking capacitor.

(v) The addition of the dc blocking capacitor has little visible influence on the converter's dynamic properties. However, it will increase the reverse voltage stress on the output rectifier diodes if the chosen value is too small.

(vi) The 500 W, 400 Vdc to 55 Vdc, 128 kHz prototype converter has demonstrated about 97% overall efficiency under full load.

(vii) The major disadvantage of the proposed topology is the high current in the auxiliary circuit. As for the lagging leg, the auxiliary current must be higher than the load current to successful discharge the snubber capacitor of the switches to achieve a ZVS turn-on. This results in considerable conduction losses. For the prototype circuit, the rms current of the switch on the lagging leg is increased by about 53%, and this increases the conduction losses on these switches by about 135%, or by 0.7 W in each IRFP460 switch on that leg at full load.

The contributions of this work include:

(i) Detailed steady state analysis of the proposed converter topology,

(ii) Detailed dynamic analysis,

(iii) Proposing the asymmetrical auxiliary circuit for optimal design,

(iv) Development of the design curves and criteria for general purpose industrial applications,

(v) Verification of design and analyses from experimental and simulation results,

(vi) Obtaining a high efficiency of 97% at full load.

5.3 Suggestions for future work

As mentioned previously, ZVS in the proposed converter topology is achieved at the costs of increased conduction losses. If the proposed converter topology is switched at low voltage, i.e., the snubber capacitors are not completely discharged when the switches are turned on, then the auxiliary circuit does not need to provide such high currents as shown in this thesis. This will reduce the conduction losses, although there are some switching losses due to the non-ZVS operation. An optimal low voltage switching condition, that results in the highest efficiency, may be found. Thus it is worthwhile to investigate the overall efficiency at low voltage switching instead of ZVS.

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