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**AN AC-AC INVERTER FOR HIGH FREQUENCY  
POWER DISTRIBUTION SYSTEM**

**Guo Wennan**

**A Thesis**

**in**

**The Department**

**of**

**Electrical and Computer Engineering**

**Presented in Partial Fulfillment of the Requirements  
for the Degree of Master of Applied Science at  
Concordia University  
Montreal, Quebec, Canada**

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## ABSTRACT

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### AN AC-AC INVERTER FOR HIGH FREQUENCY POWER DISTRIBUTION SYSTEM

Guo Wennan

Future computer and telecommunication power distribution systems require the power source to be high frequency ac type and be combined with line current Power Factor Correction that satisfies IEC 1000-3-2 standard. In addition, low power applications require high efficiency, high power density and cost effectiveness. This thesis provides a solution to low power ac-ac inverter for the future computer and telecommunication power distribution systems, which complies with the above requirements.

The proposed high frequency ac-ac inverter operates under Zero Voltage Switching (ZVS) throughout the whole range of the line voltage and load. Hence, high efficiency can be realized under high switching frequency. A unified controller is introduced in the proposed ac-ac inverter to control the dc-ac stage and the PFC stage at the same time. The controller is simple and the DC bus voltage can be well limited for all line and load conditions. Hence, cost effectiveness can be realized.

In the thesis, two types of PFC stage converters (Boost and Buckboost) are presented to compare the performance of the ac-ac inverter. Principle of operation and steady state analysis of the proposed topology are given. Performance characteristics, design procedures and computer simulation results are presented to guide the design. Experimental results from a prototype of 100kHz, 30V<sub>ac</sub>/250W output, 90-265V<sub>ac</sub> input, are presented to confirm the analysis and performance of the proposed ac-ac inverter.

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## LIST OF ACRONYMS

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<i>CCM</i>	Continuous Conduction Mode
<i>DCM</i>	Discontinuous Conduction Mode
<i>EMI</i>	Electromagnetic Interference
<i>PF</i>	Power factor
<i>PFC</i>	Power Factor Correction
<i>THD</i>	Total Harmonics Distortion
<i>AP</i>	Area Product
<i>HFPDS</i>	High Frequency Power Distribution System

## LIST OF PRINCIPLE SYMBOLS

---

$\delta$	Phase shift angle
$\phi$	Phase lag angle
$\eta$	Efficiency
$B_m$	Peak flux density (T)
$C_p$	Parallel branch capacitor of the <i>Resonant Network</i> (uF)
$C_s$	Series branch capacitor of the <i>Resonant Network</i> (uF)
$C_{s1}$ to $C_{st}$	Snubber capacitors of the full bridge
$D$	Duty cycle of the full bridge
$D_{boost}$	Duty cycle of the boost converter
$D_{buckboost}$	Duty cycle of the buckboost converter
$f_{boost}$	Switching frequency of the <i>Boost Converter</i> (Hz)
$f_{buckboost}$	Switching frequency of the <i>Buckboost Converter</i> (Hz)
$f_L$	Line frequency (Hz)
$f_{sw}$	Switching frequency of the <i>Full Bridge Inverter</i> (Hz)
$I_{cp}$	<i>rms</i> value of the current through the parallel capacitor (A)
$i_{Lin}$	Current through input inductor (A)

$i_{L_{in},peak,k}$	$k^{th}$ peak current through input inductor (A)
$\hat{i}_{L_{in},peak,k}$	Maximum peak current through input inductor (A)
$I_{lp}$	<i>rms</i> value of the current through the parallel inductor (A)
$I_{oB,boost}$	Boundary current between DCM and CCM of boost converter
$I_{oB,buckboost}$	Boundary current between DCM and CCM of buckboost converter
$I_s$	<i>rms</i> value of the current through the series branch (A)
$k_u$	Winding packing factor
$l_g$	Total length of air gap
$L_{in}$	PFC stage inductor (uH)
$L_p$	Parallel branch inductor of the <i>Resonant Network</i> (uH)
$L_s$	Series branch inductor of the <i>Resonant Network</i> (uH)
$m$	Gate Signal Constant
$N$	Main transformer turn ratio
$N_p$	Main transformer primary side turn number (turn)
$N_s$	Main transformer secondary side turn number (turn)
$R_{boost}$	Equivalent load of boost converter ( $\Omega$ )
$R_{buckboost}$	Equivalent load of buckboost converter ( $\Omega$ )
$R_d$	Final output load ( $\Omega$ )
$\mu_0$	Magnetic field constant (H/m)

$\mu_r$	Relative permeability of core
$V_{boost}$	DC bus voltage of boost implementation (V)
$V_{buckboost}$	DC bus voltage of buckboost implementation (V)
$v_{in}$	<i>AC</i> line input voltage (V)
$V_{in}$	<i>rms</i> value of <i>AC</i> line input voltage (V)
$V_o$	<i>rms</i> value of output voltage (V)
$v_{rec}$	<i>AC</i> line input voltage after diode rectifier (V)
$X_{cp}$	Impedance of the <i>Resonant Network</i> parallel capacitor
$X_p$	Impedance of the <i>Resonant Network</i> parallel inductor
$X_s$	Impedance of the <i>Resonant Network</i> series branch

# CHAPTER 1

## INTRODUCTION

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### 1.1 GENERAL

Future computer and telecommunication power distribution systems may require power transfer between the power distribution system and electronic cards through magnetic coupling, which means that the power distribution system should be of ac type [1] [2] [3] [4] [5]. In addition, in order to reduce the size and weight of the power converter, the switching frequency of the ac source should be high. Furthermore, due to the pending European Standard, IEC 1000-3-2 [6], the Power Factor Correction (PFC) has gained more and more attention in recent years. Therefore, PFC inevitably becomes another issue that should be included in the design of the high frequency ac source for the future computer and telecommunication power distribution systems.

This thesis tries to provide a solution to low power, high frequency ac-ac inverter that complies with the above-mentioned requirements.

## 1.2 PROBLEM DEFINITION

The main challenges in the ac-ac inverter design is to provide a high input power factor with restricted DC bus voltage and low cost, and to supply a constant high frequency sinusoidal output voltage with high efficiency. Section 1.2.1 and 1.2.2 describe these issues in detail.

### 1.2.1 Power Factor Correction

#### 1.2.1.1 Conventional Two-Stage Power Factor Correction

The block diagram of a conventional two-stage PFC converter is given in Fig. 1.1. The first stage is usually a boost, buckboost (or flyback) converter, which is introduced to correct the power factor and also supply DC voltage to the next stage as its input. The second stage can be a dc-dc or dc-ac converter. The two stages are independent from each other and have a controller of their own. The controller of the PFC stage has a current and voltage loop. It senses the line voltage waveform and forces the input current to track the sinusoidal line voltage to achieve unity input power factor.

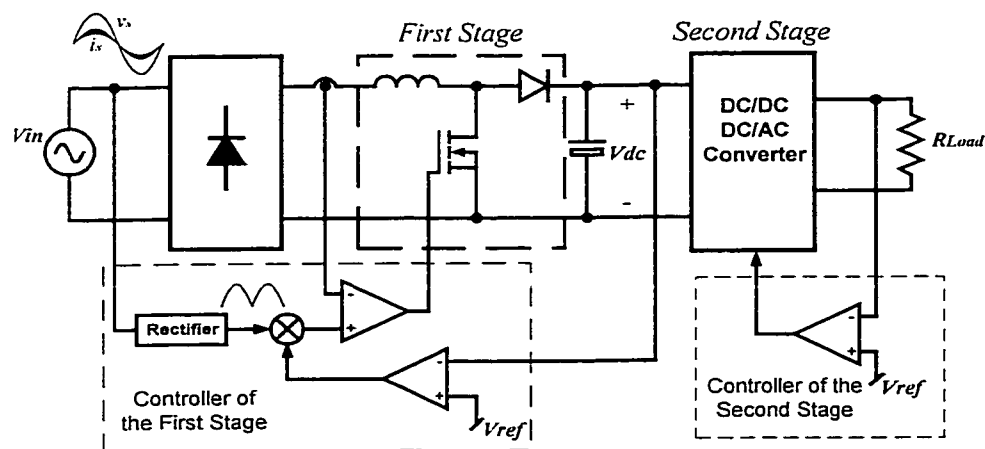


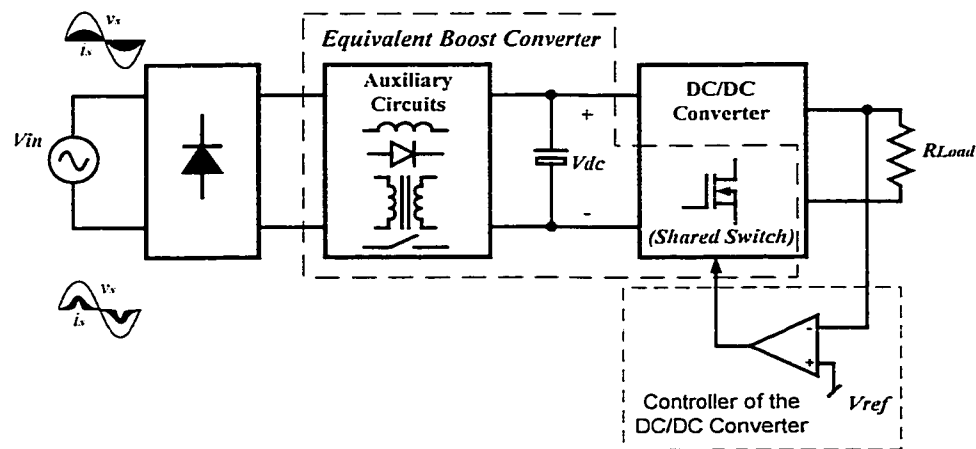
Fig. 1.1 Block Diagram of conventional Two-Stage PFC converters



The advantage of this topology is that it can provide almost unity power factor and a controllable constant DC bus voltage, which is independent from the second stage. However, it needs two separate controllers, which will increase the complexity and the cost of the converter. Since cost reduction is one of the main factor concerned in low power applications, the conventional two-stage PFC topology is not suitable for this design.

### 1.2.1.2 Single-Stage Power Factor Correction

Single-Stage PFC techniques have been studied thoroughly in recent years. There are many approaches to it [7] [8] [9] [10], but normally those proposed topologies have some auxiliary circuits to implement PFC. Fig. 1.2 gives the conceptual structure of those single-stage PFC converters. However, no matter what the forms of the auxiliary circuits are, they are substantially a boost equivalent circuit followed by a dc-dc converter. The switch of the boost equivalent circuit is integrated in the dc-dc converter. Thus no separate switch is needed for the boost equivalent circuit. Since the boost equivalent circuit and the dc-dc converter are sharing the same switch or switches, they will receive the same control signal, yielding economical control circuitry [11].



**Fig. 1.2** Block diagram of Single-Stage PFC converters

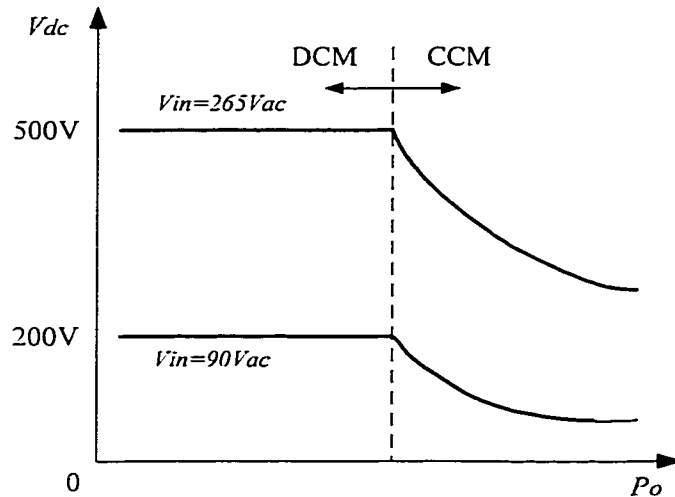
In order to keep the DC bus voltage within a relative low level in those topologies, the dc-dc converter and the boost equivalent circuit are normally designed to enter Discontinuous Conduction Mode (DCM) at low load. The dc-dc converter can be a forward [7], a full bridge [8] [9], or a flyback converter [10]. While both the dc-dc converter and the boost equivalent circuit are working in DCM, the output voltages of the dc-dc converter and the boost equivalent circuits are load dependent. However, when they are combined together, the influence of load on DC bus voltage is minimized. Therefore the DC bus voltage becomes load independent and a relatively low DC bus voltage can be realized. Table 1.1 gives the relationship between the DC bus voltage and the load for different combinations of conduction modes.

Combinations of Conduction Mode		DC Bus Voltage $V_{dc}$
Equivalent Boost Circuit	DC-DC Converter (Forward, Flyback, Full Bridge)	
CCM (Load Independent)	CCM (Load Independent)	Load Independent
CCM (Load Independent)	DCM (Load Dependent)	Load Dependent
DCM (Load Dependent)	CCM (Load Independent)	Load Dependent
<b><i>DCM (Load Dependent)</i></b>	<b><i>DCM (Load Dependent)</i></b>	<b><i>Load Independent</i></b>

**Table 1.1** Relationship between the DC bus voltage and the load for different combinations of conduction mode

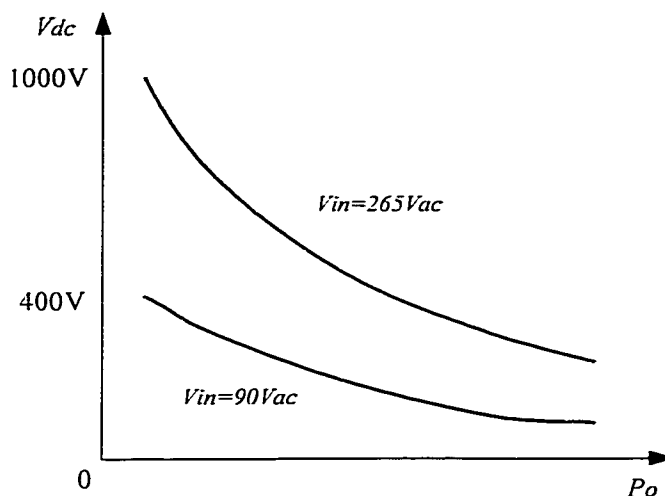
Fig. 1.3 shows the DC bus voltage as a function of load for universal line voltage. When either the boost equivalent circuit or the dc-dc converter is working in CCM, the DC bus voltage is increasing as the load is decreasing. When both the boost equivalent circuit

and the dc-dc converter are working in DCM, the DC bus voltage keeps constant regardless of the load changes.



**Fig. 1.3** DC bus voltage as a function of load for different line input voltage

However, as will be analyzed later in Chapter 4, the output voltage of the proposed ac-ac inverter in this thesis is load independent. If the above single-stage PFC strategy is adopted, there is no *Conduction Mode Combination* to choose. Therefore when load is decreasing, and the boost equivalent circuit enters DCM, the DC bus voltage will increase accordingly. Theoretically, the DC bus voltage can be extremely high at low load. Fig. 1.4 gives the DC bus voltage as a function of load for this case.



**Fig. 1.4** DC bus voltage as a function of load for universal line voltage

A major difficulty in designing a universal line input single-stage PFC converter is to limit the bulk capacitor voltage within  $450V_{dc}$ , which is the voltage limitation of commercially available capacitors. Some single-stage PFC ac/dc converter can achieve this design goal [10] by introducing additional dimensions, but what this thesis presents is a ac-ac inverter which is different from above-mentioned dc-dc converters. There is no *Conduction Mode Combination* to choose and the above mentioned methods do not apply.

### ***1.2.2 Efficiency and Constant Frequency Resonant Technique***

The ac-ac inverter for computer and telecommunication power distribution systems is required to supply high frequency sinusoidal voltage. The frequency of the output voltage must be constant, therefore the switching frequency is required to be fixed. High efficiency is also required by the inverter.

Conventional hard switching topologies are simple and easy to implement, but they are obviously not suitable for the high frequency ac-ac inverter due to their following drawbacks [12]:

1. The switches are subjected to high switching stress.
2. High switching power losses increase linearly with the switching frequency, hence high efficiency and small size of cooling devices become impossible.
3. Large  $dv/dt$  and  $di/dt$  caused by hard switching produces significant Electromagnetic Interference (EMI) [13].

Adding snubber circuits around the switches can reduce the switching stress and switching losses of the switches. However, the switching power losses are shifted from the switches to the snubber circuits, so there is no reduction in the overall switching power losses [12].

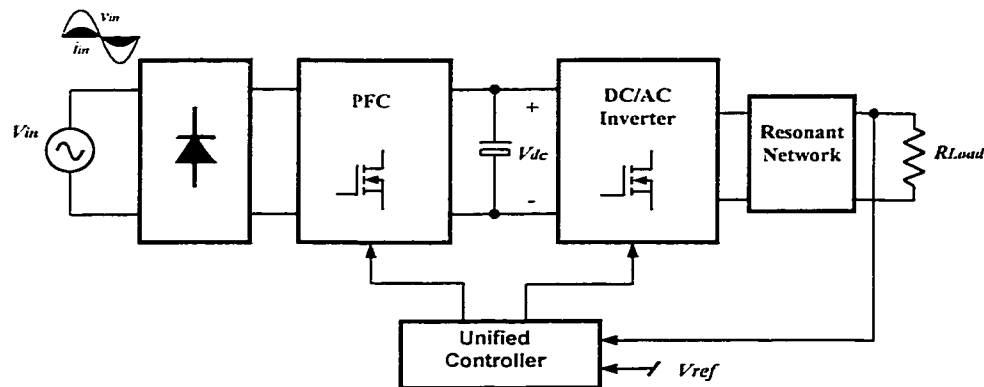
Zero-voltage switching techniques enable switches switch at a high frequency with zero switching losses. Topologies presented in reference [14][15] operate under zero-voltage switching. However they are implemented under variable frequency control, which means the switching frequency is not fixed. Thus, a constant frequency output voltage can not be obtained from the ac-ac inverter.

Reference [16][17][18] present multiple elements resonant converter topologies, which have constant frequency operation. However they only reduce part of the switching losses and exhibit higher conduction losses. Thus, they can not provide a satisfactory efficiency for the high frequency ac-ac inverter.

### 1.3 PROPOSED TOPOLOGY

Different types of PFC topologies have been discussed in section 1.2.1. The conventional two-stage PFC topology needs two separate controllers, which increases the complexity and cost. Typical single-stage PFC topologies [7] [8] [9] [10] are simple and cost effective, but will result in high DC bus voltage for the proposed ac-ac inverter [19].

Fig. 1.5 gives the block diagram of the proposed PFC high frequency inverter, in which a separate stage is introduced to correct power factor. A unified controller is introduced to control the PFC stage and the dc-ac stage at the same time. In the proposed topology, a separate PFC controller for the power factor stage is saved. In addition, the DC bus voltage can be well controlled to satisfy the limitations of commercial capacitors. The cost of the converter is therefore reduced.



**Fig. 1.5** Block diagram for proposed PFC high frequency ac-ac inverter

The dc-ac inverter and the *Resonant Network* together can generate the required constant high frequency sinusoidal output voltage. Zero-voltage switching can be realized for all the switches throughout the whole switching cycle under all load variations. Thus, a high efficiency can be achieved. In addition, the output voltage of the ac-ac inverter

demonstrates very good load independent characteristics. Details will be given thoroughly in Chapter 4.

## **1.4 THESIS OBJECTIVE**

The objectives of this thesis are:

- Propose a high frequency low power ac-ac inverter with PFC.
- Realize ZVS for the dc-ac stage throughout the line voltage and load variations so that high efficiency can be achieved.
- Achieve high input power factor that satisfies IEC 1000-3-2 standards.
- Maintain a low DC bus voltage for universal line voltage and required load range.
- Develop steady state analysis and demonstrate performance. Give design procedure and design example to guide the design process.
- Use simulation and experimental results to verify the theoretical analysis.

## **1.5 THESIS OUTLINE**

The content of this thesis are organized as follows:

Chapter 2 presents a *Boost Converter* implemented power factor corrected ac-ac inverter. Circuit description and principle of operation are given. Performance

characteristics are given to guide the design. Simulation and experimental results are given in the end.

Chapter 3 presents a *Buckboost Converter* implemented power factor corrected ac-ac inverter. The structure of this chapter is similar to that of Chapter 2.

Chapter 4 gives the detailed analysis of the resonant dc-ac stage. Principle of operation, operation modes, and steady state analysis are given. Performance characteristics are presented to guide the design. Simulation and experimental results are given in the end to illustrate the achieved goal of the design.

Chapter 5 gives the design procedure and example of the proposed high frequency ac-ac inverter. Actually used components in the experiment are also listed in detail.

Chapter 6 gives the summary of the thesis. Suggestions for future work on this topic are presented.



## CHAPTER 2

# BOOST IMPLEMENTED PFC

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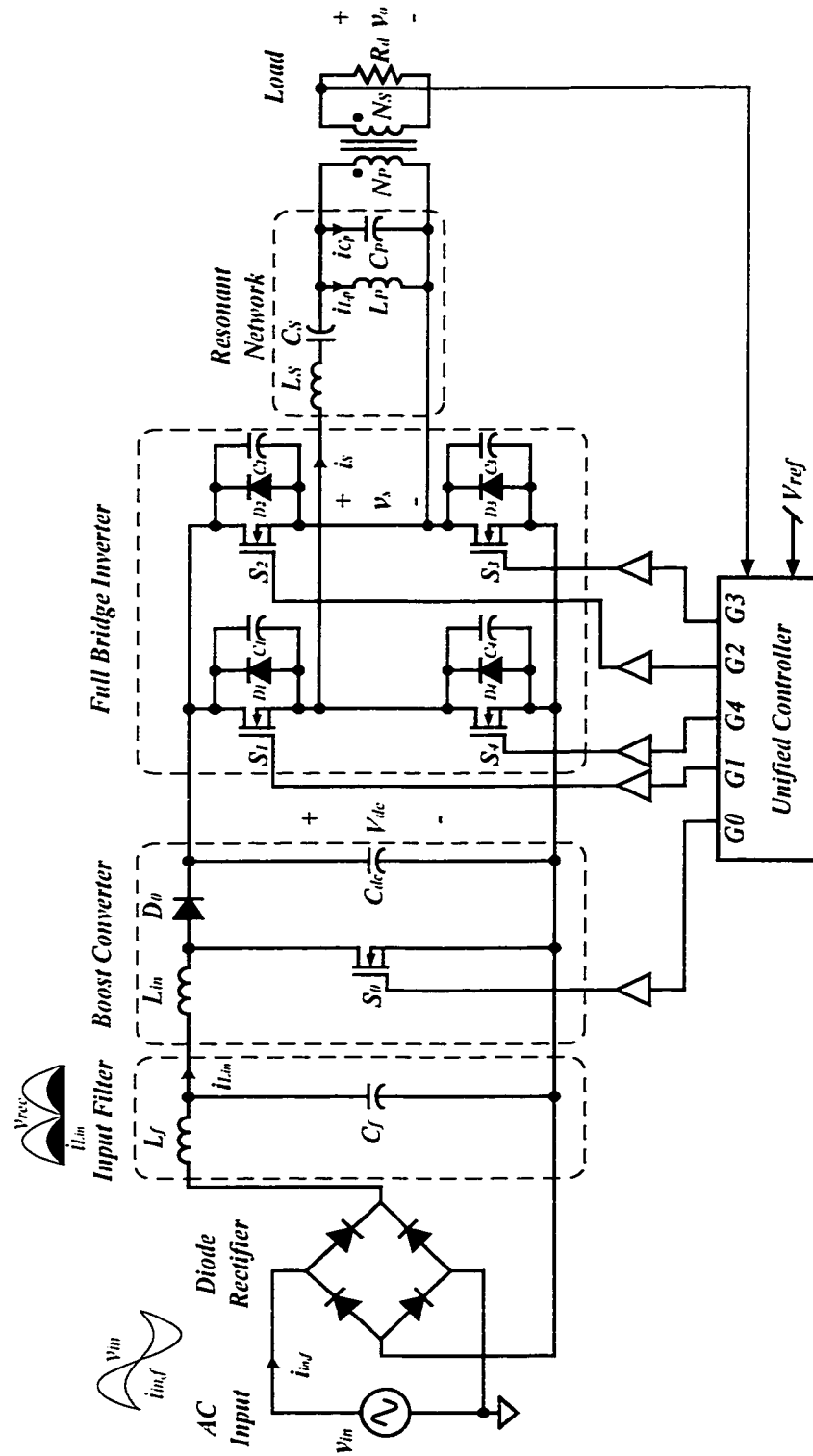
### 2.1 INTRODUCTION

This chapter presents an ac-ac inverter with a PFC stage implemented by a boost converter [20]. A unified controller is introduced to control the two stages. The analyzed example operates at a fixed frequency of 100kHz with a rated output power of 250W and a rated output voltage of 30V<sub>ac</sub>. In order to achieve a high input power factor, the boost converter is designed to work in Discontinuous Conduction Mode (DCM).

In the following sections, the description and analysis will be mainly focused on the *Boost Converter*. The detail analysis on the dc-ac stage will be given in Chapter 4. DC bus voltage, duty cycle, input power factor, and peak input current for different input voltages and loads are the main factors that will be analyzed in this chapter.

Circuits description and operation principles will be given in section 2.2 and 2.3 respectively. Steady state analysis is given in section 2.4. Performance characteristics are given in section 2.5 to guide the design. Simulation and experimental results are given in section 2.6 to verify the steady state analysis. Suggestions on the application of this proposed topology are also given at the end of this chapter.

## 2.2 DESCRIPTION OF PROPOSED TOPOLOGY

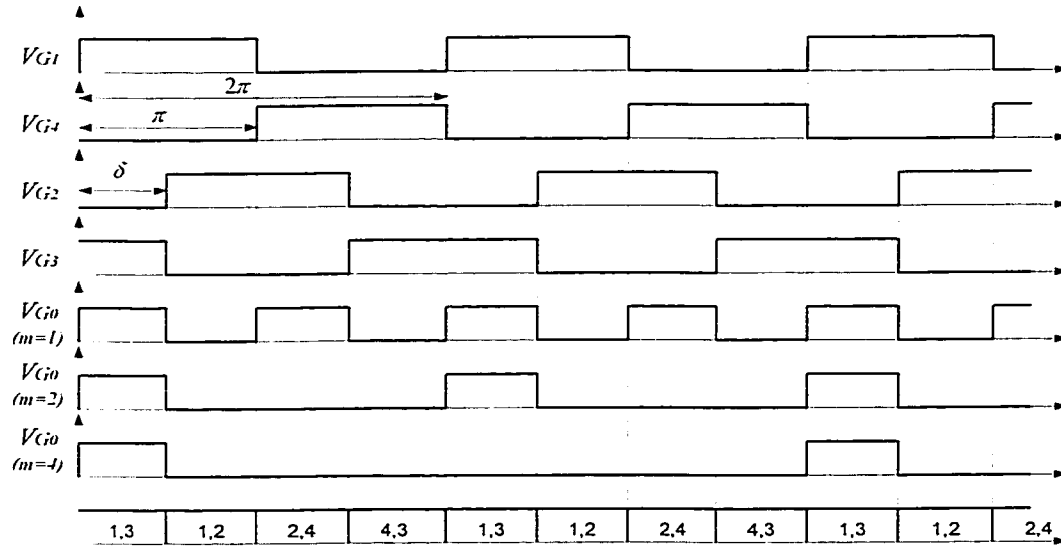


**Fig. 2.1** Proposed high frequency ac-ac inverter with boost PFC

Fig. 2.1 gives the proposed high frequency ac-ac inverter, which consists of the follow parts:

- ***Input Filter***: It is made up of high frequency capacitors and inductors to filter out the high frequency harmonics contained in the line current.
- ***Diode Rectifier***: The *Diode Rectifier* provides rectified ac input voltage to the *Boost Converter*.
- ***Boost Converter***: The *Boost Converter* is designed to work in Discontinuous Conduction Mode to correct the power factor and provide a DC bus voltage to the *Full Bridge Inverter* simultaneously. Its input is from the *Diode Rectifier* and its gate signal is generated by the *Unified Controller*.
- ***Full Bridge Inverter***: The dc-ac stage adopts a full bridge topology with phase-shifted gating signal control pattern. It generates a high frequency quasi-square voltage waveform at its output.
- ***Resonant Network***: The *Resonant Network* is made up of capacitors and inductors. It converts the quasi-square voltage waveform from the *Full Bridge Inverter* into a sinusoidal waveform. At the same time, it can let the *Full Bridge inverter* work under ZVS to reduce the switching losses.
- ***Unified Controller***: The *Unified Controller* gets the feedback from the output voltage and generates phase shifted signal to the four switches of the *Full Bridge Inverter* as well as the gate signal for the *Boost Converter* at the same time.

The gate signals of the proposed topology are illustrated in Fig. 2.2, where  $V_{G1}$ ,  $V_{G2}$ ,  $V_{G3}$ , and  $V_{G4}$  are the phase shifted gate signals to the *Full Bridge Inverter*.  $\delta$  is the phase shift angle.  $V_{G0}$  is the gate signal to the *Boost Converter*.  $V_{G0}$  is generated whenever  $S_1$  and  $S_3$ , or  $S_2$  and  $S_4$  are conducting at the same time, see  $V_{G0}$  ( $m=1$ ) in Fig. 2.2. However, in order to reduce the DC bus voltage, we may not keep all the pulses shown in  $V_{G0}$  ( $m=1$ ). We may keep only  $1/m$  of them ( $m$  here is called *Gate Signal Constant*). For example, when  $m=1$ , we keep all the pulses, see  $V_{G0}$  ( $m=1$ ). When  $m=2$  or  $4$ , we keep  $1/2$  or  $1/4$  of the pulses respectively, see  $V_{G0}$  ( $m=2$ ) and  $V_{G0}$  ( $m=4$ ).

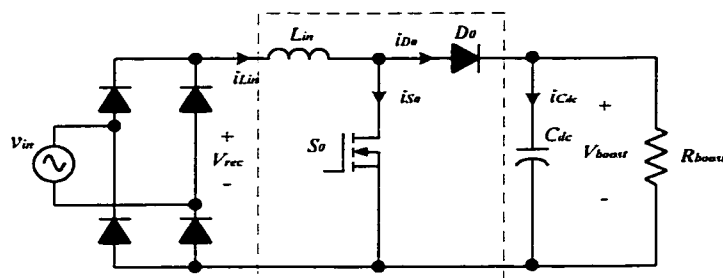


**Fig. 2.2** Gate signals generated by the *Unified Controller*

## 2.3 PRINCIPLE OF OPERATION

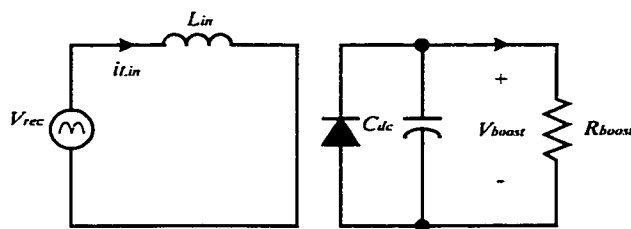
Fig. 2.3 gives the simplified circuits for the boost PFC stage, in which  $R_{boost}$  is the equivalent load for the *Boost Converter*. The only difference between this topology and the standard boost converter is that the input of this topology is a rectified sinusoidal voltage waveform instead of a DC voltage source. This difference makes PFC possible. In order to

have high power factor, the *Boost Converter* should be designed to work in Discontinuous Conduction Mode (DCM) [21].



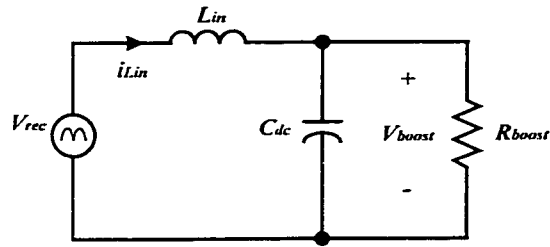
**Fig. 2.3** Boost Converter after Diode Rectifier with equivalent load

There are three different operation switching intervals for the boost PFC stage during a single switching cycle. The first interval starts when the boost switch  $S_0$  is turned on. The rectified input voltage is therefore applied to the inductor  $L_{in}$  through the switch  $S_0$ . The bulk capacitor  $C_{dc}$  supplies the power to the output load. The equivalent circuit for this interval is given in Fig. 2.4. Key waveforms of this interval are shown in Fig. 2.7:  $t_0-t_1$ .



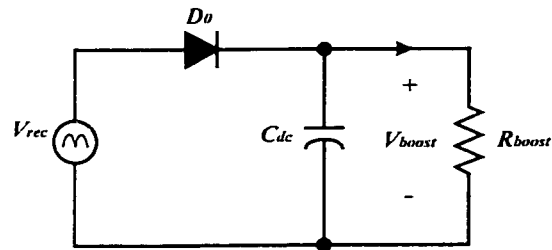
**Fig. 2.4** Equivalent circuit for interval one

The second interval begins with the turn-off of switch  $S_0$ . The input power and the energy stored in the inductor  $L_{in}$  is transferred to the buck capacitor  $C_{dc}$  through diode  $D_0$ . The equivalent circuit for this interval is given in Fig. 2.5. Key waveforms of this interval are shown in Fig. 2.7:  $t_1-t_2$ .

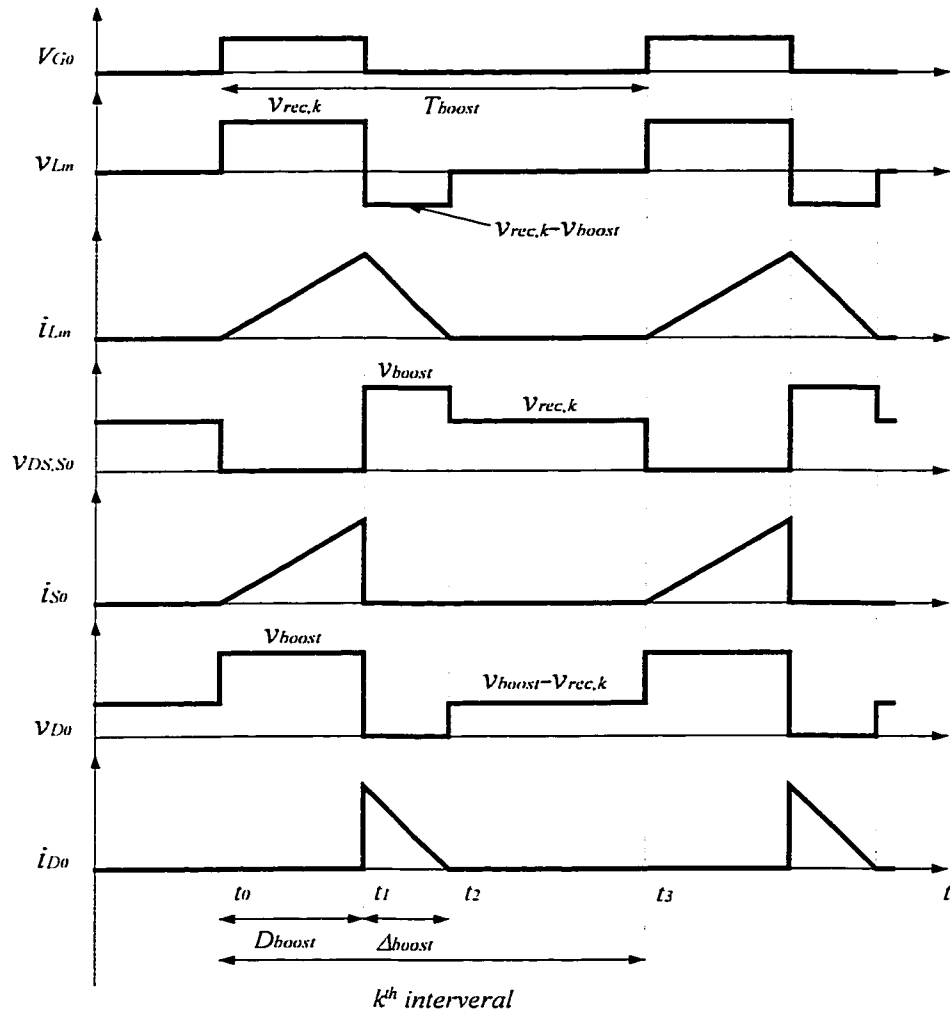


**Fig. 2.5** Equivalent circuits for interval two

In the third interval, switch  $S_0$  is still off, same as in interval two, but no current is circulating through inductor  $L_{in}$ . Diode  $D_0$  is reverse biased, which means no power is transferred from the input to the output. The bulk capacitor  $C_{dc}$  supplies the load alone. The equivalent circuit for this interval is given in Fig. 2.6. Key waveforms of this interval are shown in Fig. 2.7:  $t_2-t_3$ .



**Fig. 2.6** Equivalent circuits for interval three

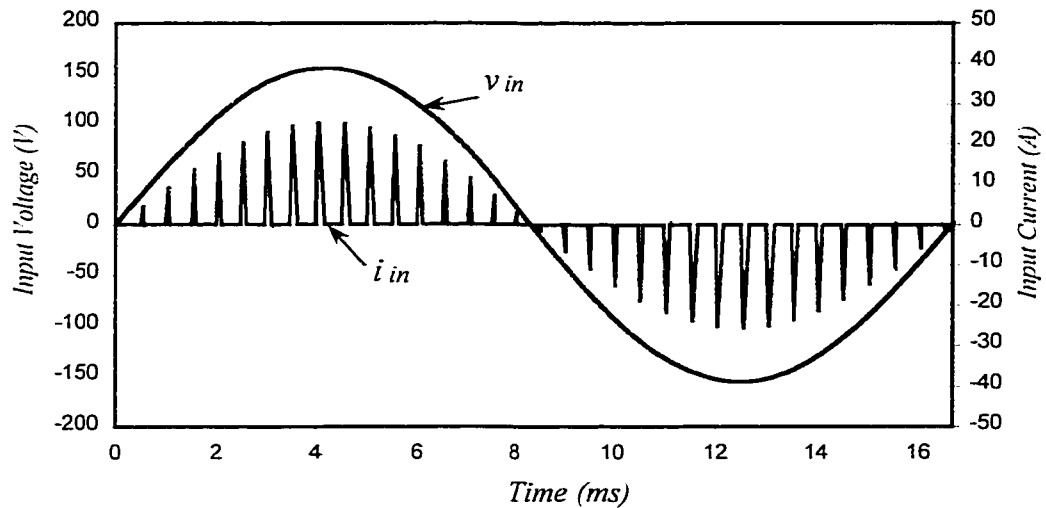


**Fig. 2.7** Key waveforms of the Boost PFC stage

From Fig. 2.7, we can see that the current through inductor  $L_{in}$  is a discontinuous triangular waveform. The peak of  $i_{Lin}$  forms a 60Hz line frequency sinusoidal envelop, which is forced by the rectified input voltage

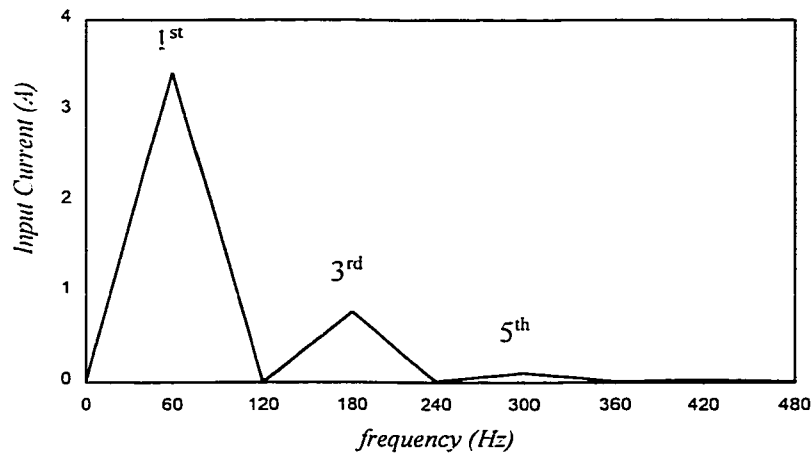
[21]. Fig. 2.8 gives a simulation example for the line voltage and current waveforms. As we can see, the line current has a 60Hz sinusoidal envelop with many high frequency components, which can be filtered by the *Input Filter*. After being filtered, the line current can be nearly a sinusoidal waveform, which results in high input Power Factor

(PF) and low Total Harmonics Distortion (THD). The switching frequency of the simulation is chosen to be only 2kHz to have a clear picture of the line current.



**Fig. 2.8** Simulated input line voltage and current with 2kHz switching frequency

Fig. 2.9 gives the simulated spectrum of the line current at low frequency. High frequency harmonics is not given because the *Input Filter* can easily filter them out. However, the low frequency harmonics: 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup> are not easily eliminated, so the design is mainly focused on reducing the low frequency harmonics.



**Fig. 2.9** Simulated low frequency harmonic spectrum of the input current



## 2.4 STEADY STATE ANALYSIS

This section will only give the steady state analysis of the boost PFC stage. DC bus voltage, input power factor, and input peak current will be studied thoroughly. The steady state analysis of the *Full Bridge Inverter* will be given in Chapter 4.

### 2.4.1 Duty Cycle and DC Bus Voltage

Eq.(2-1) gives the equation for boost in DCM:

$$D_{boost} = \sqrt{2 \cdot \frac{V_{boost}}{V_{in}} \cdot \left( \frac{V_{boost}}{V_{in}} - 1 \right) \cdot \frac{L_{in} \cdot f_{boost}}{R_{boost}}} \quad (2-1)$$

The gate signals for the *Full Bridge Inverter* and the *Boost Converter* have already been given in Fig. 2.2. “ $\delta$ ” is the phase shift angle. The duty cycle of the *Full Bridge Inverter* is defined as:

$$D = \frac{\delta}{\pi} \quad (2-2)$$

The transformer turn ratio of the *Full Bridge Inverter* is:

$$N = \frac{N_p}{N_s} \quad (2-3)$$

The relationship between the rms output voltage  $V_o$  and the DC input voltage  $V_{boost}$  of the *Full Bridge Inverter* is given in Eq.(2-4). The derivation of the equation will be given in section 4.4 and Appendix A1. The equation indicates that the output voltage of the *Full Bridge Inverter* is load independent.

$$V_o = \frac{1}{N} \cdot 0.9 \sin \frac{\delta}{2} \cdot V_{boost} \quad (2-4)$$

$$P_o = P_{boost} \cdot \eta \quad (2-5)$$

Hence,

$$\frac{V_{boost}^2}{R_{boost}} \cdot \eta = \frac{V_o^2}{R_d} \quad (2-6)$$

By substituting (2-4) into (2-6), we can get the expression for the equivalent load of the *Boost Converter*.

$$R_{boost} = \frac{V_{boost}^2}{V_o^2} \cdot R_d \cdot \eta = \frac{N^2}{\left(0.9 \sin \frac{\delta}{2}\right)^2} \cdot R_d \cdot \eta \quad (2-7)$$

From Fig. 2.2, we can get the duty cycle of the *Boost Converter*, where  $m$  is the *Gate Signal Constant*:

$$D_{boost} = \frac{1}{m} \cdot D \quad (2-8)$$

The switching frequency of the *Boost Converter* is:

$$f_{boost} = \frac{2 f_{sw}}{m} \quad (2-9)$$

Substitute Eq.(2-2), (2-4), (2-7), (2-8) and (2-9) into Eq.(2-1), we get:

$$D = \sqrt{\frac{V_o}{V_m} \cdot \left( \frac{V_o}{V_m} - \frac{0.9 \sin \frac{D \cdot \pi}{2}}{N} \right) \cdot \frac{4m \cdot L_{in} \cdot f_{sw}}{R_d \cdot \eta}} \quad (2-10)$$

For given input line voltage, output voltage and load, we can calculate out the duty cycle of the *Full Bridge Inverter* by solving Eq.(2-10).

Combine Eq.(2-2), (2-4) and (2-10), we get the DC bus voltage  $V_{boost}$ .

$$V_{boost} = \frac{V_o^2 - V_m^2}{V_o^2 - \frac{V_m^2 \cdot D^2 \cdot R_d \cdot \eta}{4m \cdot L_{in} \cdot f_{sw}}} \quad (2-11)$$

As we have pointed out in section 1.2.1.2, the DC bus voltage is load dependent. It is determined by the value of inductor  $L_{in}$ , switching frequency  $f_{sw}$  and the *Gate Signal Constant*  $m$ . In order to limit the DC bus voltage within an acceptable range, those parameters need to be carefully designed. In section 2.5, characteristic curves will be given in detail to guide the design.

### 2.4.2 Peak Current of the Converter

Eq.(2-12) gives the expression of the ac line input voltage.

$$v_m(t) = \sqrt{2}V_m \sin(2\pi f_l \cdot t) \quad (2-12)$$

When the switch  $S_0$  is turned on (interval one), the voltage across the inductor  $L_{in}$  is the rectified ac input voltage, given in Eq.(2-13):

$$v_{Lin} = v_{rec}(t) = |v_{in}(t)| = \left| \sqrt{2}V_{in} \sin(2\pi f_L \cdot t) \right| \quad (2-13)$$

Due to the high switching frequency  $f_{boost}$  of the *Boost Converter*, the rectified input voltage  $v_{rec}$  can be assumed constant within the  $k^{th}$  switching interval. The number of switching intervals during one line cycle is given in Eq.(2-14).

$$n = \frac{f_{boost}}{f_l} \quad (2-14)$$

Thus, the up slop of the current through the inductor  $L_{in}$  during the  $k^{th}$  interval is :

$$\frac{di_{L_{in}, up, k}}{dt} = \frac{\left| \sqrt{2}V_{in} \sin(2\pi k / n) \right|}{L_{in}} \quad (2-15)$$

The peak current through the inductor  $L_{in}$  during the  $k^{th}$  interval is:

$$i_{L_{in}, peak, k} = \frac{\left| \sqrt{2}V_{in} \sin(2\pi k / n) \right|}{L_{in}} \cdot \frac{D_{boost}}{f_{boost}} \quad (2-16)$$

The maximum peak current through the inductor  $L_{in}$  during one line cycle is:

$$i_{L_{in}, peak, max} = \frac{\sqrt{2}V_{in}}{L_{in}} \cdot \frac{D_{boost}}{f_{boost}} \quad (2-17)$$

The maximum peak current through the switch  $S_0$ , diode  $D_0$  and diode rectifier are the same as the maximum peak current through the inductor  $L_{in}$ :

$$i_{S_0, peak, max} = i_{D_0, peak, max} = i_{L_{in}, peak, max} = \frac{\sqrt{2}V_{in}}{L_{in}} \cdot \frac{D_{boost}}{f_{boost}} \quad (2-18)$$

Substitute Eq.(2-8) and (2-9) into Eq.(2-17), we get the maximum input peak current, where D is given in Eq.(2-10).

$$\dot{i}_{L_{in}, peak, max} = \frac{\sqrt{2}V_{in} \cdot D}{2L_{in} \cdot f_{sw}} \quad (2-19)$$

When the switch  $S_0$  is off (interval two), the voltage across the inductor  $L_{in}$  becomes:

$$v_{L_{in}} = \left| \sqrt{2}V_{in} \sin \omega_{line} t \right| - V_{boost} \quad (2-20)$$

Thus, the down slop of the current through the inductor  $L_{in}$  during the  $k^{th}$  interval becomes:

$$\frac{di_{L_{in}, dv, k}}{dt} = \frac{\left| \sqrt{2}V_{in} \sin(2\pi k / n) \right| - V_{boost}}{L_{in}} \quad (2-21)$$

### 2.4.3 Boundary between DCM and CCM

The output current of the *Boost Converter* is:

$$I_{boost} = \frac{V_{boost}}{R_{boost}} = \frac{V_{boost}}{R_d \cdot \eta} \cdot \frac{\left( 0.9 \sin \frac{D\pi}{2} \right)^2}{N^2} \quad (2-22)$$

The boundary of the output current of the *Boost Converter* is [12]:

$$I_{OB, boost} = \frac{V_{boost}}{2L_{in} \cdot f_{boost}} \cdot D_{boost} \cdot (1 - D_{boost})^2 \quad (2-23)$$

In order to let the *Boost Converter* work in DCM, the output current of it must be smaller than the boundary current.

$$I_{boost} < I_{OB, boost} \quad (2-24)$$

Substitute Eq. (2-8), (2-9), (2-22) and (2-23) into Eq.(2-24), we get the expression that judge the *Boost Converter* is in DCM or not.

$$\frac{\left(0.9 \sin \frac{D\pi}{2}\right)^2}{D \cdot \left(1 - \frac{1}{m} D\right)^2} < \frac{N^2 \cdot R_d \cdot \eta}{4L_{in} \cdot f_{sw}} \quad (2-25)$$

#### 2.4.4 Input Current Power Factor

The expression for the input current power factor is given in Eq.(2-26). The fundamental and harmonics can be measured from the spectrum, such as the one shown in Fig. 2.9.

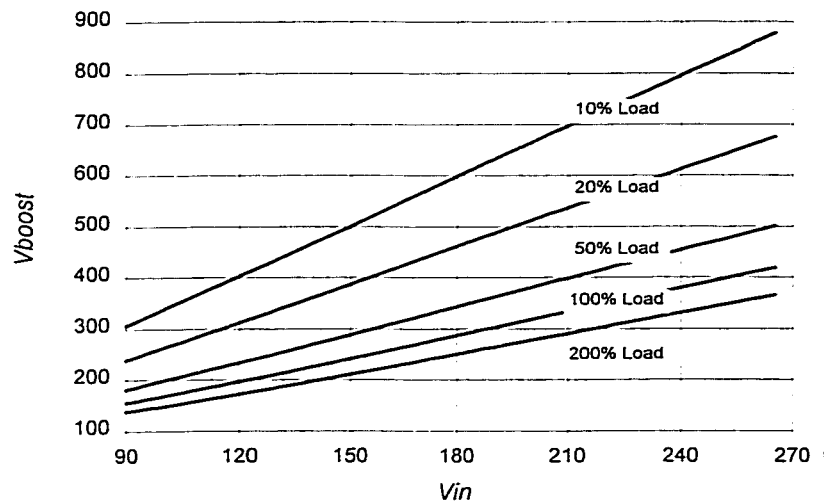
$$PF = \frac{I_{s1}}{\sqrt{I_{s1}^2 + I_{s3}^2 + I_{s5}^2 + I_{s7}^2 + \dots}} \quad (2-26)$$

## 2.5 PERFORMANCE CHARACTERISTICS

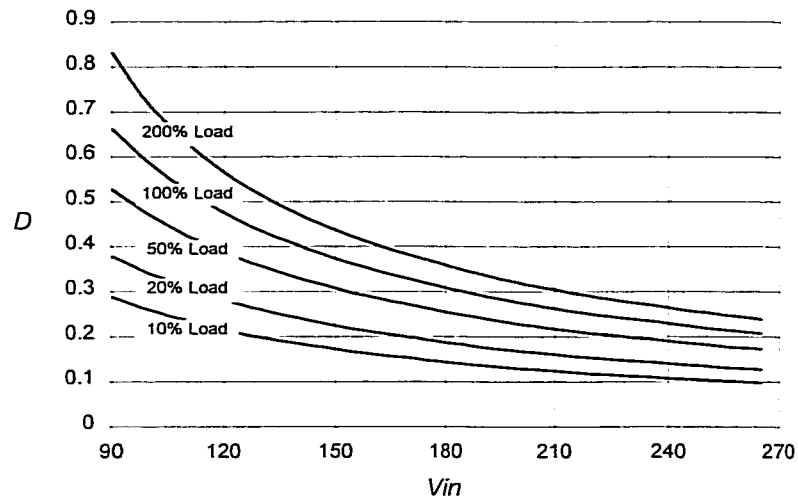
The performances of the PFC stage refers to the range of the DC bus voltage, the range of the duty cycle, the maximum unfiltered input peak current and the input power factor. In this section, performance characteristics will be given in detail corresponding to different load, transformer turn ratio, input inductor, and *Gate Signal Constant m*.

### 2.5.1 Effect of Load on Performance

Fig. 2.10 gives the curves of the DC bus voltage versus input voltage for various load, which illustrates that the DC bus voltage is load dependent. When load is decreasing, the DC bus voltage is increasing. Theoretically the DC bus voltage can be infinite, which means the proposed inverter has to work within a certain range of load. Fig. 2.11 gives the characteristics of the duty cycle versus load. The lower the load is, the smaller the duty cycle will be.



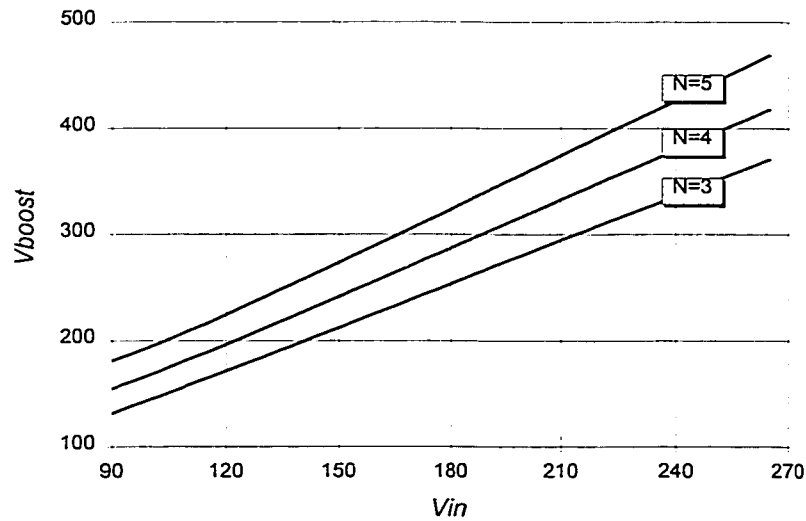
**Fig. 2.10** DC bus voltage versus input voltage for various loads  
(at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $N=4$ ,  $L_{in}=30\mu H$ ,  $m=4$ )



**Fig. 2.11** Duty cycle versus input voltage for various loads (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $N=4$ ,  $L_{in}=30\mu H$ ,  $m=4$ )

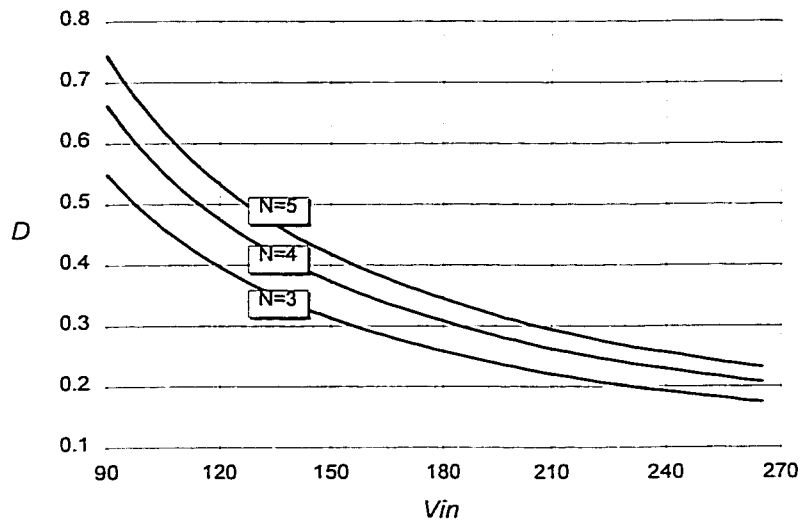
### 2.5.2 Effect of Transformer Turn Ratio on Performance

The transformer turn ratio of the *Full Bridge Inverter* will affect the DC bus voltage and the duty cycle. The larger the turn ratio is, the larger the DC bus voltage and the duty cycle will be, see Fig. 2.12 and Fig. 2.13.



**Fig. 2.12** DC bus voltage versus input voltage for various transformer turn ratio (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=30\mu H$ ,  $m=4$ )



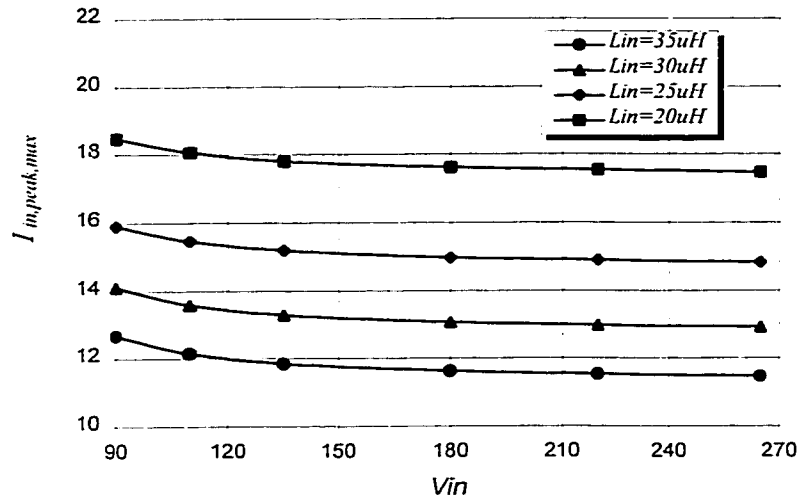


**Fig. 2.13** Duty cycle versus input voltage for various transformer turn ratio (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=30\mu H$ ,  $m=4$ )

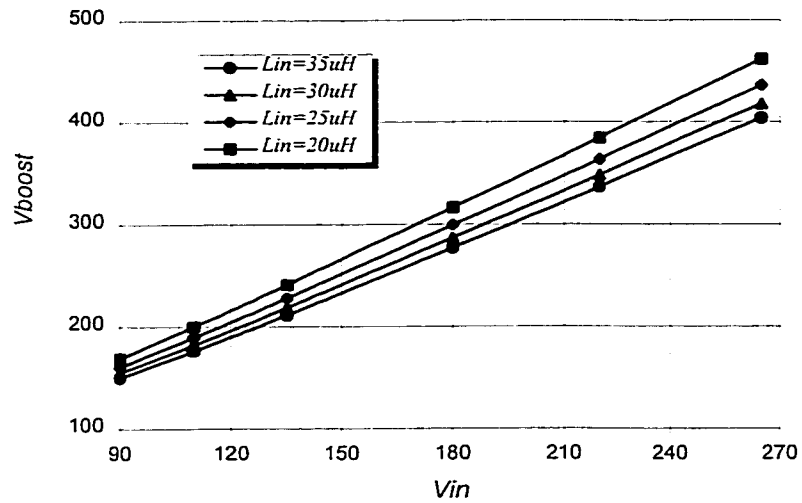
### 2.5.3 Effect of Input Inductor $L_{in}$ on Performance

In order to have a high input power factor, we prefer the *Boost Converter* to work in DCM. Therefore, inductor  $L_{in}$  should be small enough to enable the *Boost Converter* to work in DCM. Fig. 2.14 gives the relationship between the maximum peak current and the inductor value (all simulated points for different  $L_{in}$  are in DCM). However,  $L_{in}$  can not be too small, otherwise the maximum input peak current will be too high, which will result in a high current stress on related components, hence would increase the cost accordingly. Therefore,  $L_{in}$  should be designed to its maximum value so that it reduces the switch stress and keeps DCM operation as well.

Fig. 2.15 shows that a smaller  $L_{in}$  will result in a higher DC bus voltage. However, the influence of  $L_{in}$  on the DC bus voltage is not very significant. Therefore, in the design,  $L_{in}$  is not expected to contribute much in reducing the DC bus voltage.



**Fig. 2.14** Maximum input peak current versus input voltage for various  $L_{in}$  (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $N=4$ ,  $m=4$ )

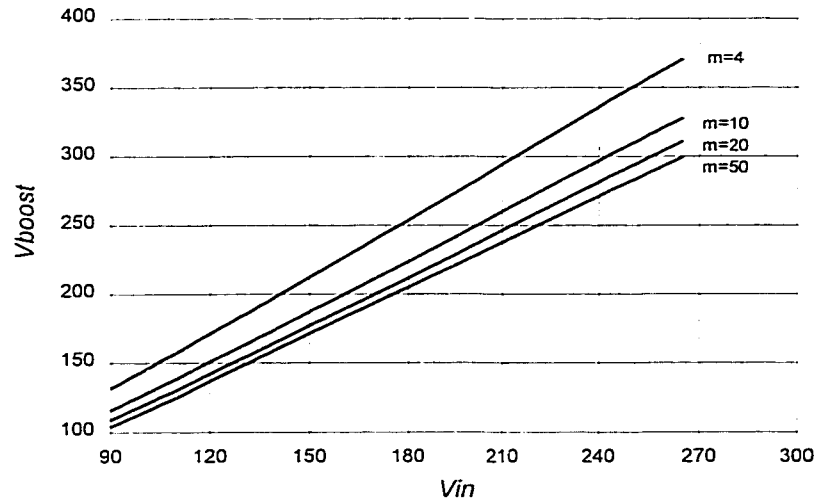


**Fig. 2.15** DC bus voltage versus input voltage for various  $L_{in}$  (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $N=4$ ,  $m=4$ )

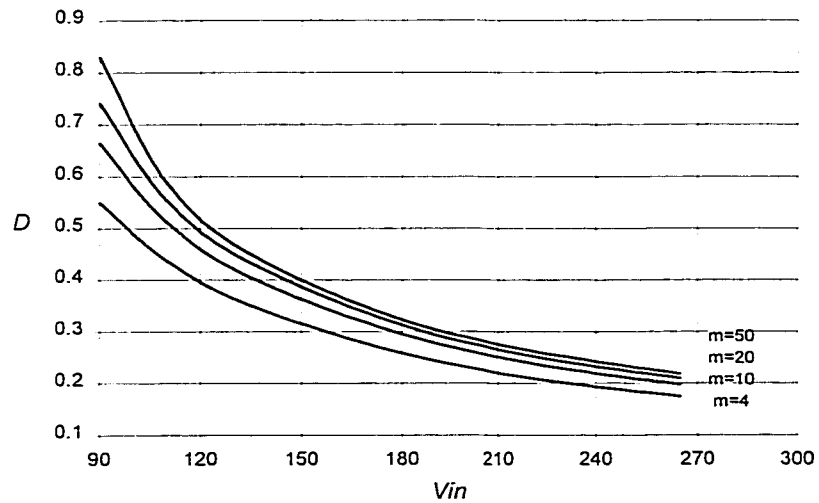
### 2.5.4 Effect of Gate Signal Constant $m$ on Performance

Fig. 2.16 to Fig. 2.19 illustrate the effects of gate signal constant  $m$  on the DC bus voltage and the duty cycle. Increasing  $m$  is the main means to reduce the DC bus voltage.

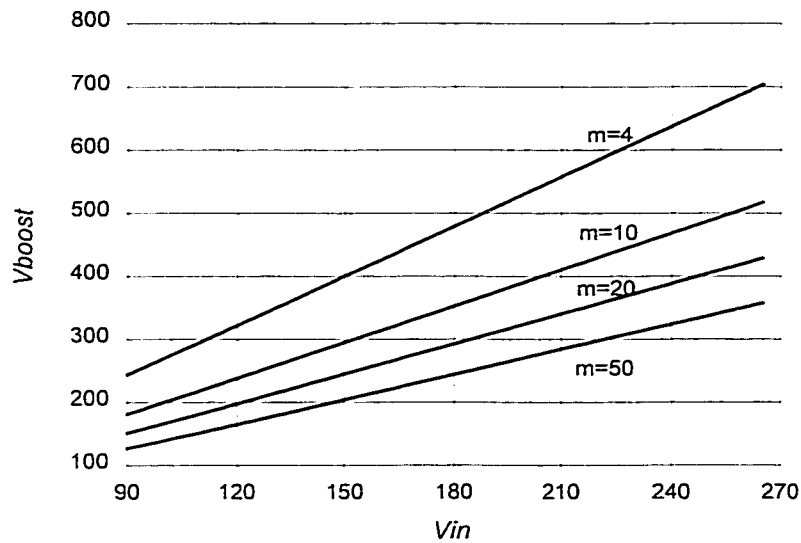
Moreover, if  $m$  is increased, the range of the duty cycle will be narrowed. A narrow range of the duty cycle is preferred in the design of the *Full Bridge Inverter*, which will be analyzed in Chapter 4.



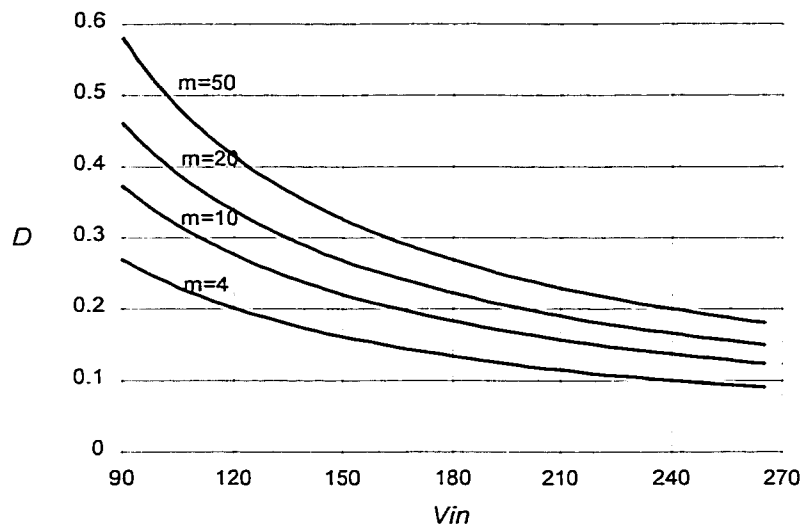
**Fig. 2.16** DC bus voltage versus input voltage for various  $m$  at rated load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=30\mu H$ ,  $N=4$ )



**Fig. 2.17** Duty cycle versus input voltage for various  $m$  at rated load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=30\mu H$ ,  $N=4$ )



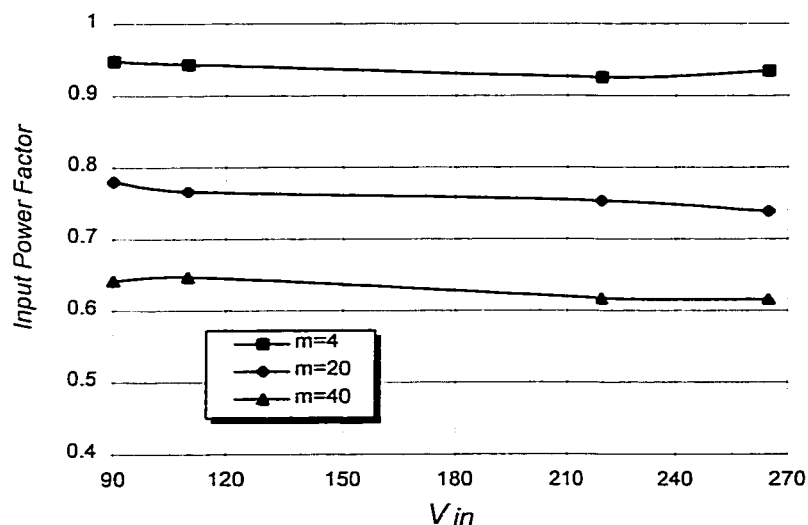
**Fig. 2.18** DC bus voltage versus input voltage for various  $m$  at 10% rated load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=36\Omega$ ,  $L_{in}=30\mu H$ ,  $N=4$ )



**Fig. 2.19** Duty cycle versus input voltage for various  $m$  at 10% rated load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=36\Omega$ ,  $L_{in}=30\mu H$ ,  $N=4$ )

The DC bus voltage can be reduced significantly by increasing  $m$ . However, there is a trade off between the DC bus voltage and the input power factor. A larger  $m$  will result in a poor power factor, see Fig. 2.20. Therefore, in order to reduce the DC bus voltage and

keep a relative high power factor, a compromised has to be made while selecting the value of  $m$ .



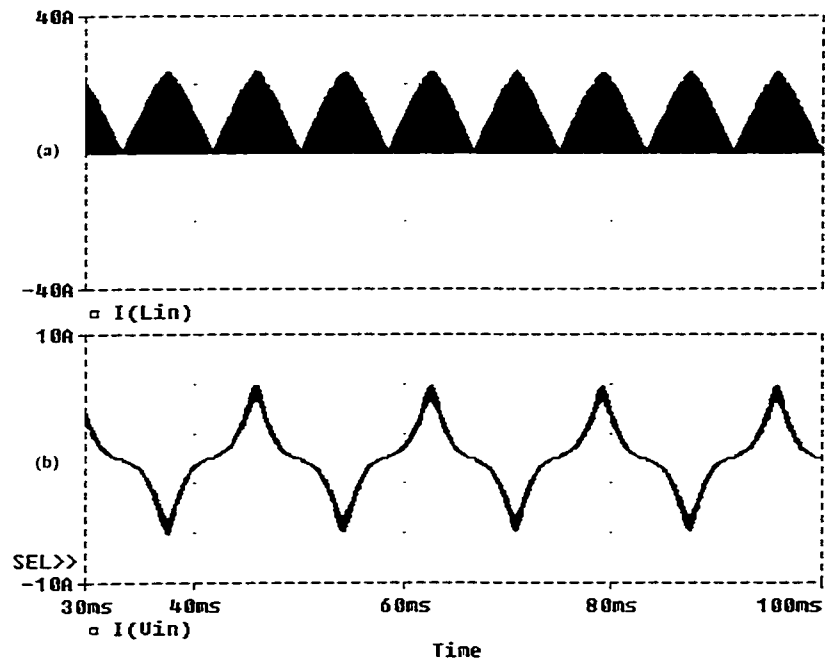
**Fig. 2.20** Input Power Factor as a function of input voltage for various  $m$  (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=15\mu H$ ,  $N=4$ )

## 2.6 SIMULATION AND EXPERIMENTAL VERIFICATIONS

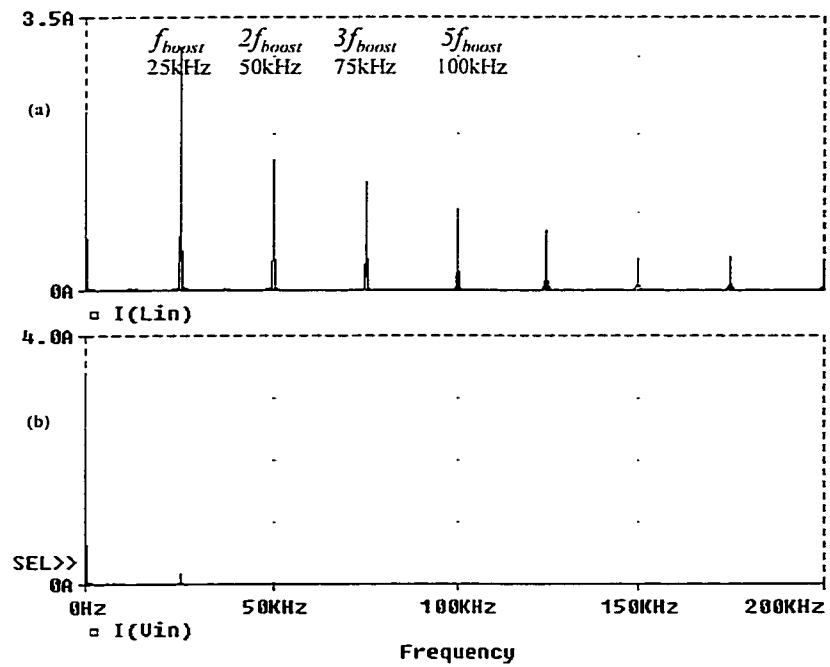
Simulation and experimental waveforms are presented in this section to verify the steady state analysis. Collected data are also tabulated and plotted to compare with the theoretical predictions. The simulation and experiment circuits are based on the design example given in Chapter 5, which has a  $30V_{ac}$ , 100kHz output voltage, 250W output power, with 90-265 $V_{ac}$  input voltage. The detailed specifications are given in section 5.1.

### 2.6.1 Simulation Waveforms

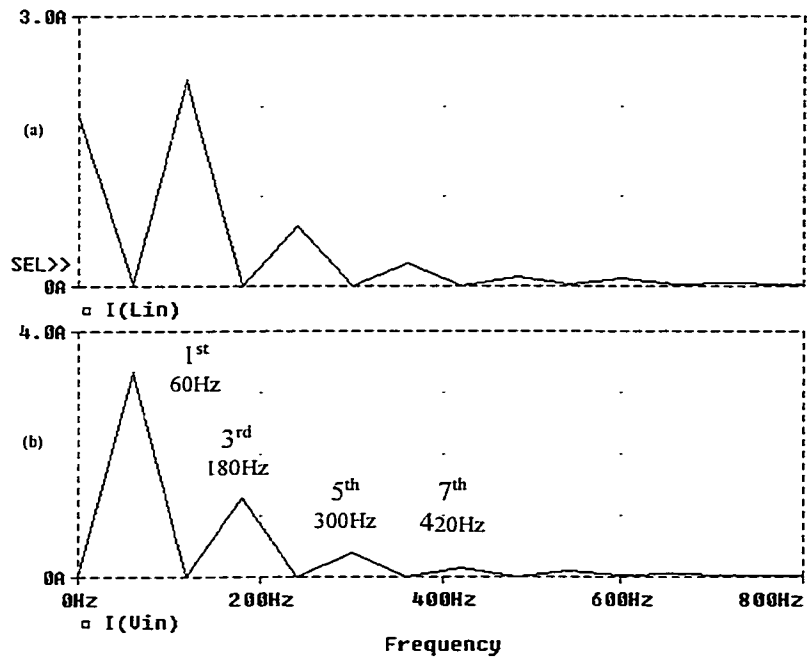
Fig. 2.21 to Fig. 2.25 give the simulation waveforms of the *Boost Converter* in the ac-ac inverter. The simulation is running at 110 $V_{ac}$  input, 250W output power.



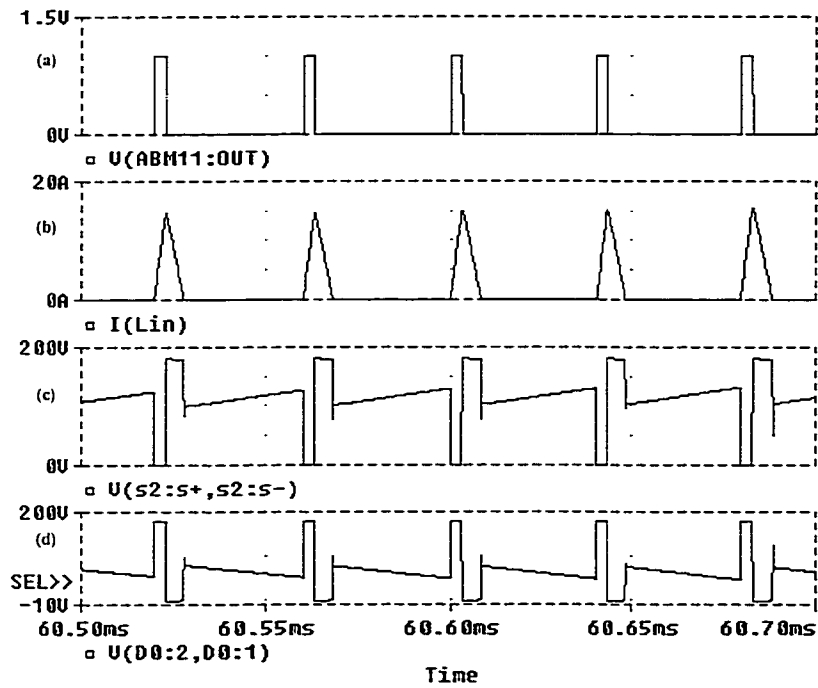
**Fig. 2.21** (a) Simulation waveform of the boost inductor current;  
 (b) Simulation waveform of the filtered input current



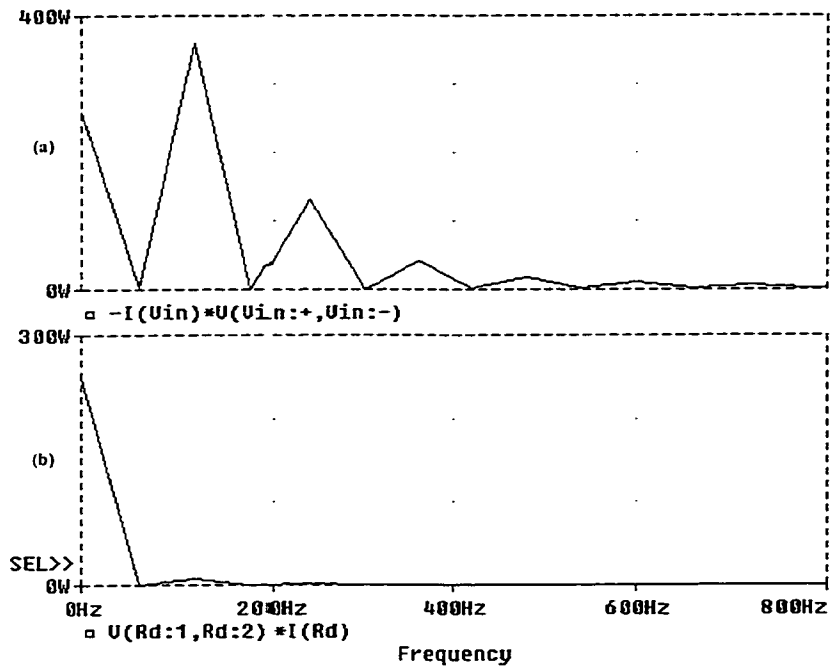
**Fig. 2.22** (a) Simulated high frequency harmonic spectrum of the boost inductor current;  
 (b) Simulated high frequency harmonic spectrum of the filtered line current



**Fig. 2.23** (a) Simulated low frequency harmonic spectrum of the boost inductor current;  
 (b) Simulated low frequency harmonic spectrum of the filtered line current



**Fig. 2.24** (a) Simulation waveform of the gate signal of the *Boost Converter*;  
 (b) Simulation waveform of the boost inductor current after zoom;  
 (c) Simulation waveform of the voltage across the boost switch;  
 (d) Simulation waveform of the voltage across the boost diode



**Fig. 2.25** (a) Simulated frequency spectrum of input current times input voltage;  
 (b) Simulated frequency spectrum of output current times output voltage

Fig. 2.22 (a) verified the operation principle given in section 2.3. The discontinuous current through the boost inductor contains high frequency harmonics, which are at the frequency of  $f_{boost}$ ,  $2f_{boost}$ ,  $3f_{boost}$  and so on. However, the *Input Filter* can filter them out. Fig. 2.22 (b) shows that almost all the high frequency harmonics have been filtered out from the input current. The THD of the input current is smaller than 5%.

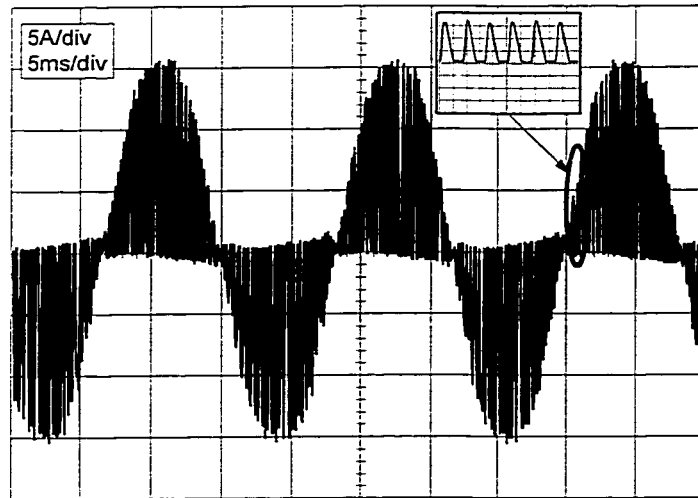
Fig. 2.23 (b) gives the low frequency harmonics of the input current. They satisfy the requirement of IEC-100-3-2. The measured input power factor is 0.904.

Fig. 2.24 verified the waveform prediction given in section Fig. 2.7. The dc component of the frequency spectrum given in Fig. 2.25 (a) and (b) shows that the input power equals to the output power, which means there is no substantial error in the proposed topology.

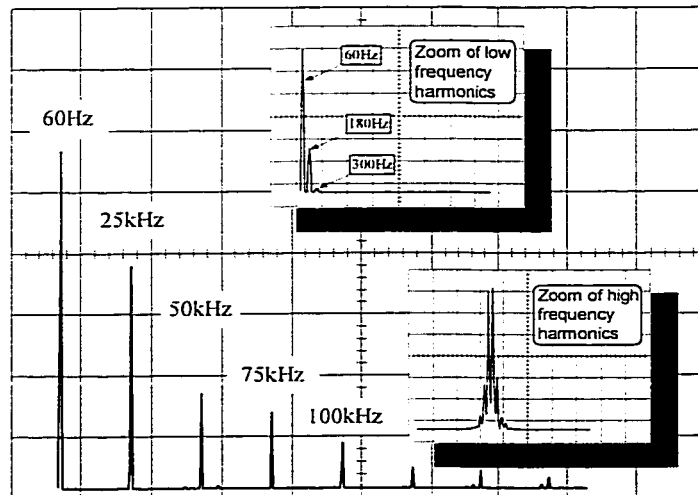


## 2.6.2 Experimental Waveforms

Fig. 2.26 gives the experimental waveform of the unfiltered input current, which shows that the *Boost Converter* is working in DCM. Fig. 2.27 gives the high frequency and low frequency harmonics of the input current. The recorded distribution of the high frequency harmonics verified the simulated frequency spectrum given in Fig. 2.22.



**Fig. 2.26** Experimental waveform of the line current without the *Input Filter* (at 110V<sub>ac</sub> input, 250W output)



**Fig. 2.27** Measured frequency harmonic spectrum of the unfiltered line current (at 110V<sub>ac</sub> input, 250W output)

Fig. 2.28 gives the experimental waveforms of the line voltage and the filtered line current. Fig. 2.29 gives the harmonic distribution and magnitude of the measured line current. It shows that the proposed topology satisfies the requirement of IEC-1 000-3-2.

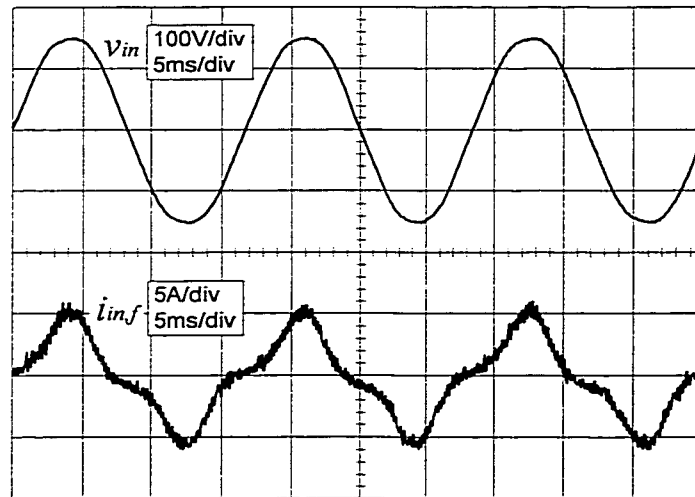


Fig. 2.28 Experimental waveforms of the line voltage and the filtered line current (at 110V<sub>ac</sub> input, 250W output power)

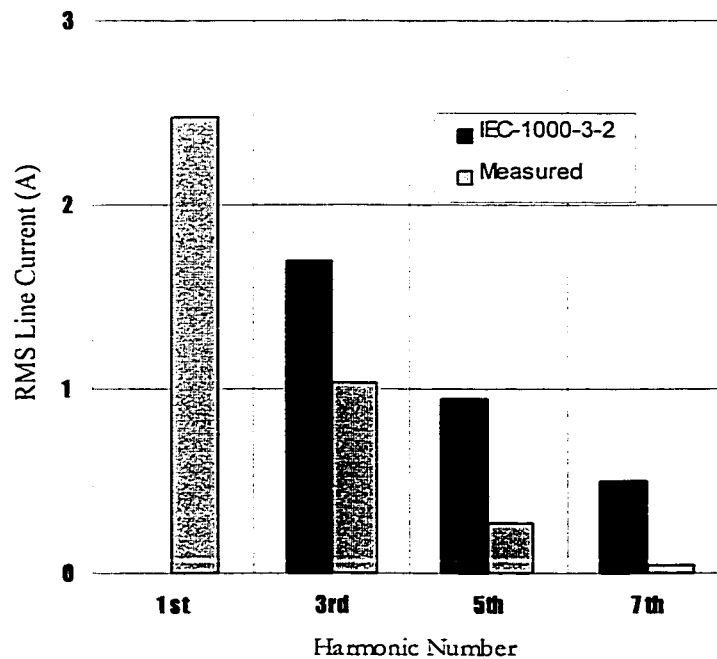


Fig. 2.29 Measured harmonics of the unfiltered line current compared with IEC 1000-3-2 limits

Fig. 2.30 plots the measured experimental DC bus voltage for all load and line voltage variations. It shows that the DC bus voltage can be limited within  $450V_{dc}$ . Fig. 2.31 plots the measured overall efficiency of the experimental prototype for all load and line voltage variations. The prototype has the highest efficiency of up to 90% at  $90\text{-}135V_{ac}$  input and  $100\text{-}185W$  output.

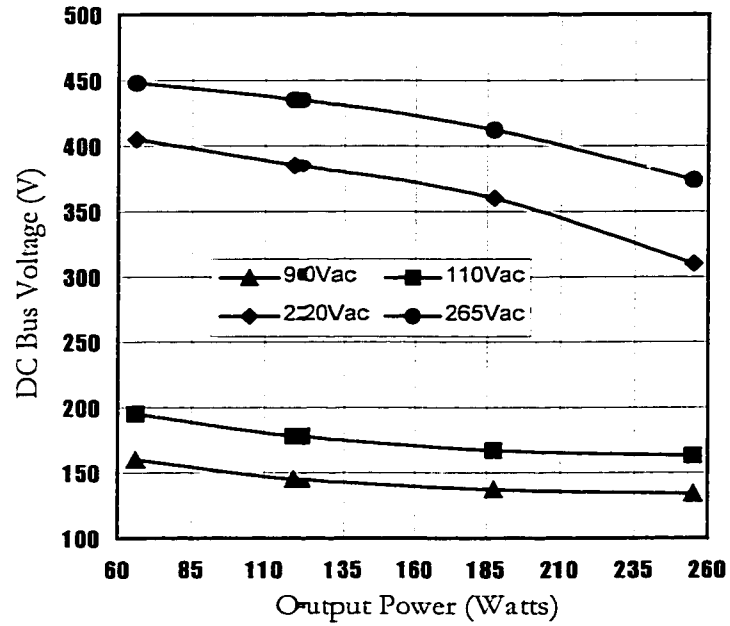
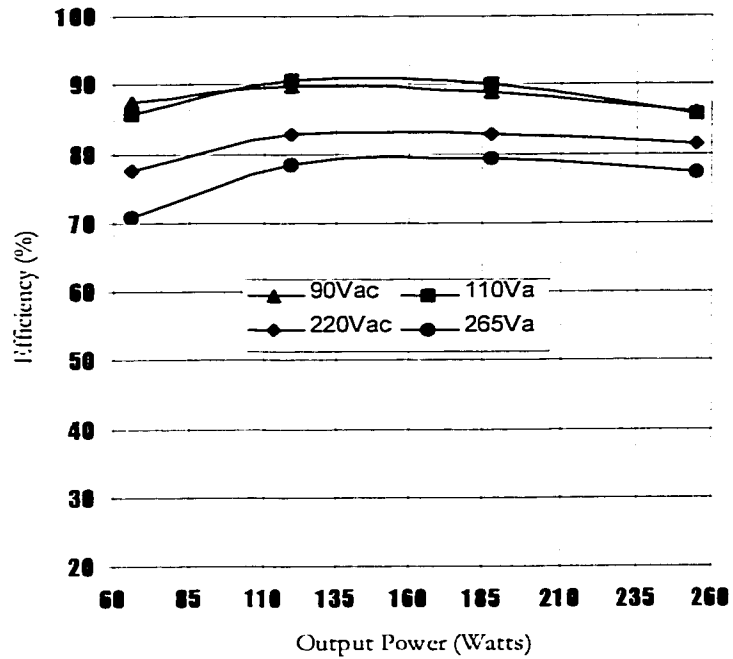


Fig. 2.30 Measured DC bus voltage versus load for various line voltage

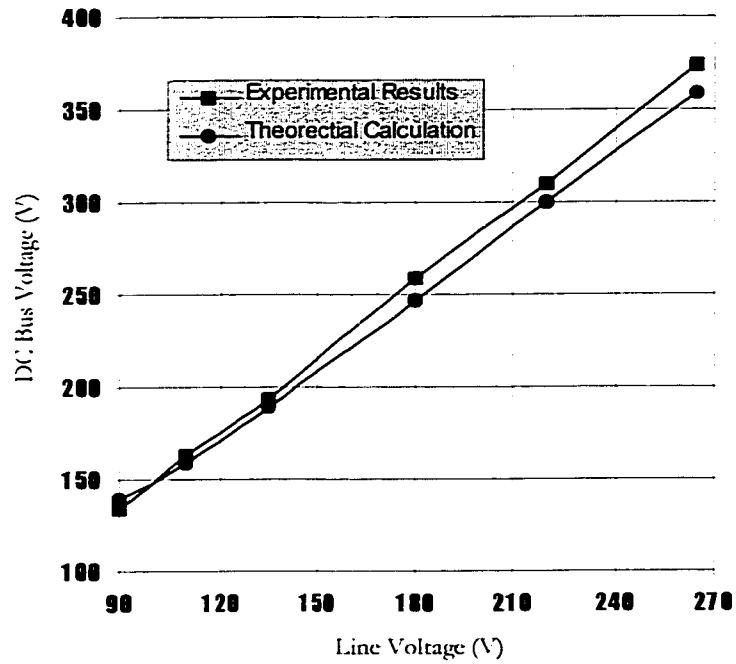


**Fig. 2.31** Measured overall efficiency

### ***2.6.3 Comparison of Experiment, Simulation and Theoretical Analysis***

Fig. 2.32 gives the comparison of the DC bus voltage between experiment results and theoretical calculation, which shows that the theoretical prediction is very accurate.

Table 2.1 tabulates the value of duty cycle and DC bus voltage for theoretical calculation, simulation and experimental results. The comparison shows that the predictions are very close to simulation and experimental results.



**Fig. 2.32.** Measured dc bus voltage versus theoretical calculation at 110V<sub>ac</sub> input and 100% output power

V <sub>in</sub> (V)	Duty Cycle			DC bus voltage (V)		
	Theoretical	Simulation	Experiment	Theoretical	Simulation	Experiment
90	0.663	0.59	0.606	155	157	134
110	0.524	0.49	0.483	182	188	163
135	0.417	0.403	0.39	219	223	194
180	0.308	0.30	0.283	287	295	259
220	0.25	0.24	0.238	348	364	310
265	0.207	0.22	0.198	418	432	374

**Table 2.1** Comparison of duty and DC bus voltage between theoretical calculation, simulation and experimental results

## 2.7 CONCLUSION

The proposed topology in this chapter can greatly reduce the DC bus voltage and keep a relative high input Power Factor. However, through theoretical analysis, simulation and experimental results show that the DC bus voltage is at the edge of  $450V_{dc}$  when the input voltage reaches its maximum  $265V_{ac}$ , and the load is reduced to its minimum. In addition, experimental results show that the prototype has the highest efficiency at 90-135 $V_{ac}$  input. Therefore, the proposed inverter is suitable for 90-265 $V_{ac}$  input and 250W output applications, and especially very attractive in 90-135 $V_{ac}$  input and 250W output applications.

## CHAPTER 3

# BUCKBOOST IMPLEMENTED PFC

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### 3.1 INTRODUCTION

Chapter 2 has presented a boost converter to implement PFC. Its DC bus voltage is at the edge of  $450V_{dc}$  at high line voltage and minimum load. Therefore, a further reduction of the DC bus voltage is attempted in this chapter.

In this chapter, a buckboost converter is presented to substitute the boost converter in the PFC stage [22] [23]. Other circuits remain the same. The proposed topology can keep the DC bus voltage within  $450V_{dc}$  for universal line voltage. High power factor is maintained and the auxiliary control circuit is very simple.

The organization of this chapter is similar to that of Chapter 2. Principle of operation is given in section 3.2. Steady state analysis is given in section 3.3. Performance characteristics are given in section 3.4 to guide the design. Conclusions are made in section 3.6.

### 3.2 PRINCIPLE OF OPERATION

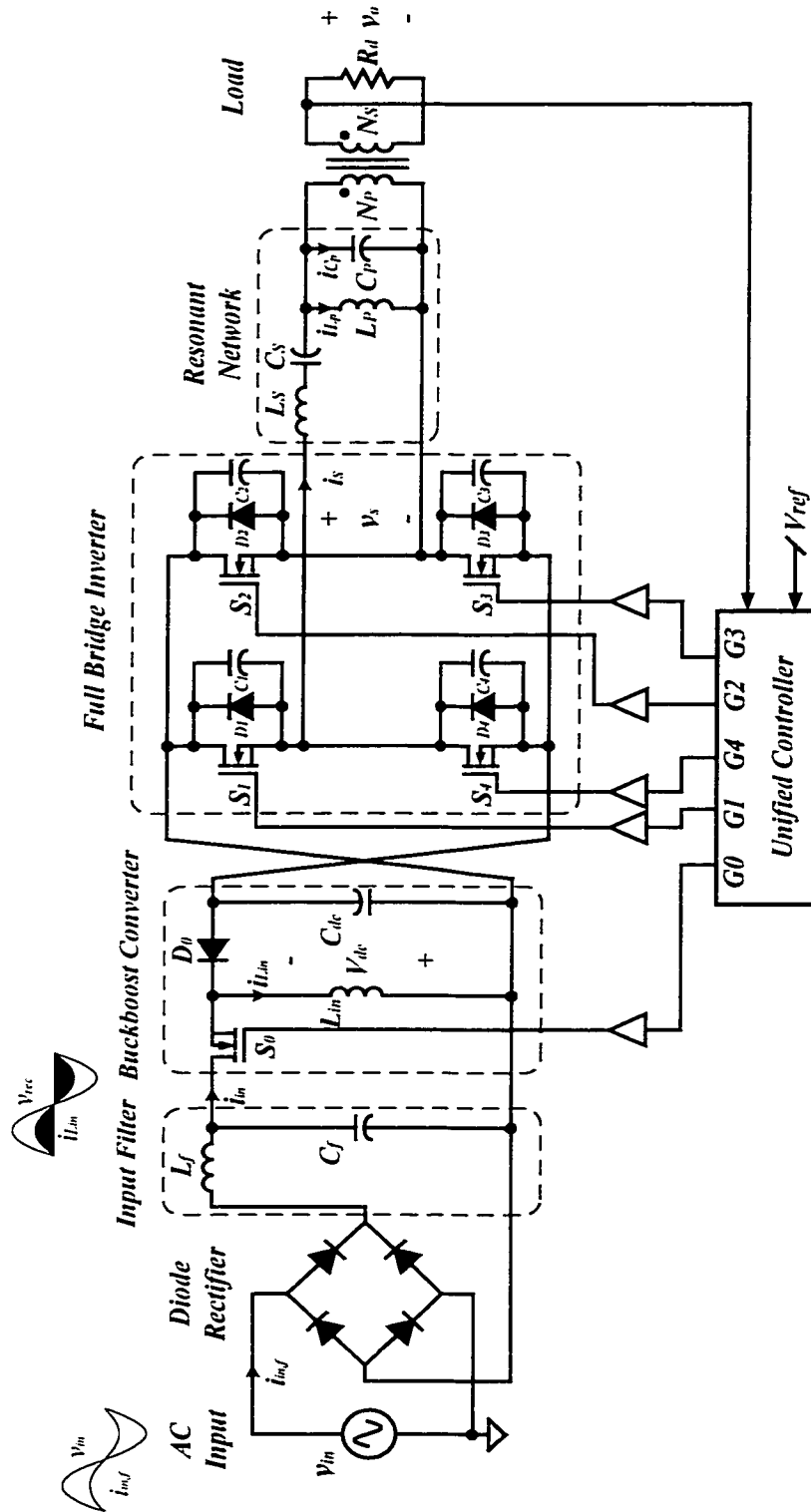
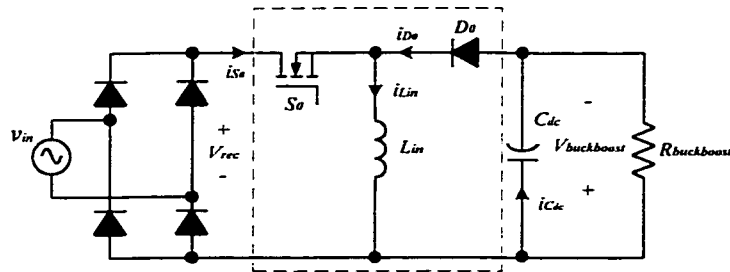


Fig. 3.1 Proposed high frequency ac-ac inverter with buckboost PFC

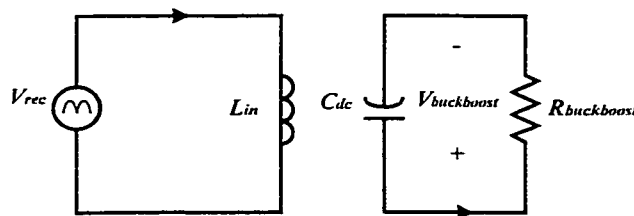


Fig. 3.2 gives the proposed inverter with buckboost PFC stage. The simplified circuit for the PFC stage is given in Fig. 3.2, in which  $R_{buckboost}$  is the equivalent load for the buckboost converter. In order to have high power factor, the *Buckboost Converter* is designed to work in DCM. Therefore, similar to the boost converter in Chapter 1, there are three different operation intervals for the buckboost PFC stage during a single switching cycle.



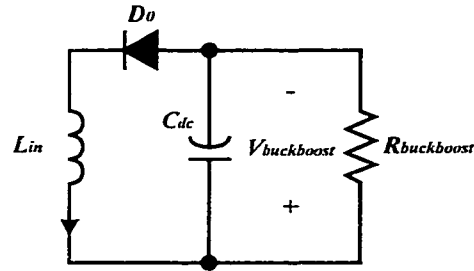
**Fig. 3.2** Buckboost converter after *Diode Rectifier* with equivalent load

The first interval starts when the switch  $S_0$  is turned on. The rectified input voltage is therefore applied to the inductor  $L_{in}$  through the switch  $S_0$ . The bulk capacitor  $C_{dc}$  supplies the power to the output load. The equivalent circuit for this interval is given in Fig. 3.3. Key waveforms of this interval are shown in Fig. 3.6:  $t_0-t_1$ .



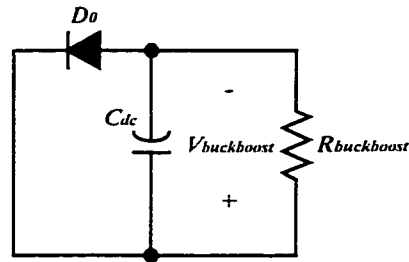
**Fig. 3.3** Equivalent circuits of buckboost during interval one

The second interval begins with the turn-off of switch  $S_0$ . The energy stored in the inductor  $L_{in}$  is transferred to the buck capacitor  $C_{dc}$  through diode  $D_0$ , see Fig. 3.4. Key waveforms of this interval are shown in Fig. 3.6:  $t_1-t_2$ .



**Fig. 3.4** Equivalent circuits of buckboost during interval two

In the third interval, switch  $S_0$  is still off, same as in interval two, but no current is circulating through inductor  $L_{in}$ . Diode  $D_0$  is reverse biased, which means no power is transferred from the input to the output. The bulk capacitor  $C_{dc}$  supplies the load alone, see Fig. 3.5. Key waveforms of this interval are shown in Fig. 3.6:  $t_2-t_3$ .



**Fig. 3.5** Equivalent circuits of buckboost during interval three

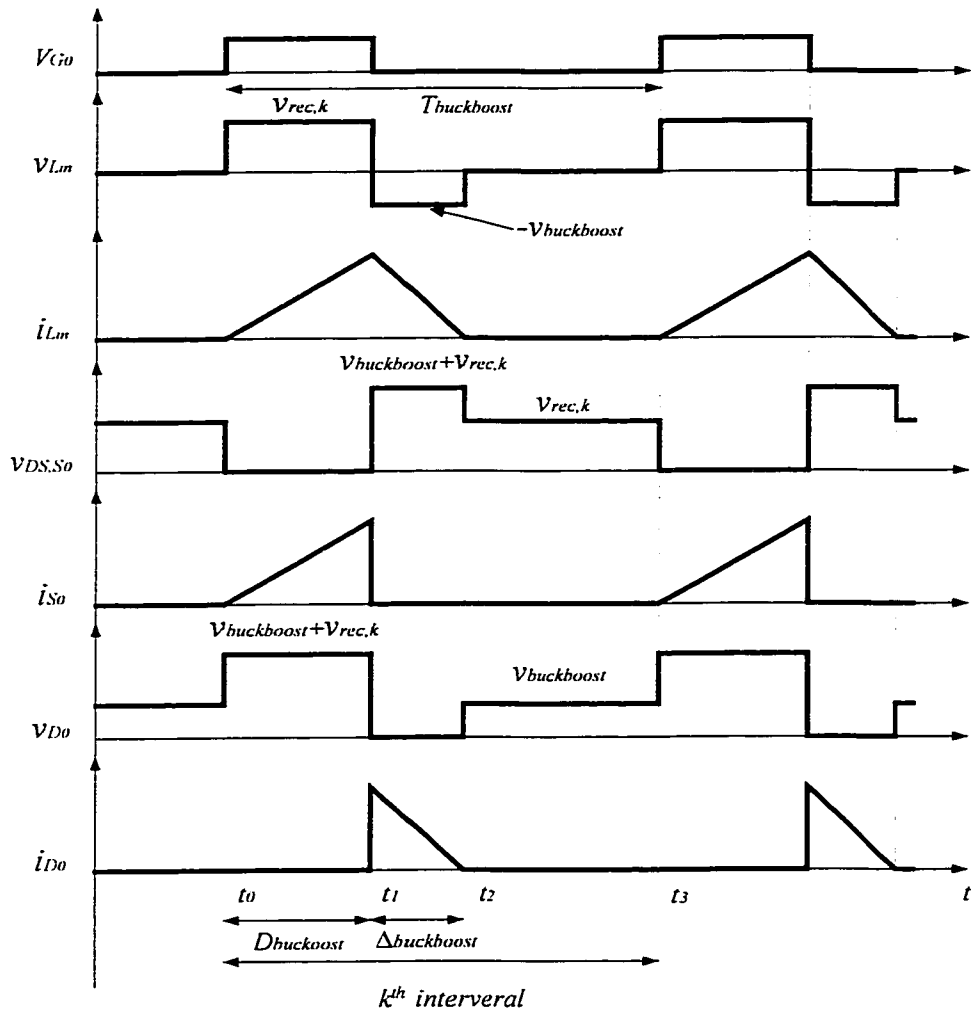


Fig. 3.6 Key waveforms of the *Buckboost Converter*

### 3.3 STEADY STATE ANALYSIS

#### 3.3.1 Duty Cycle and DC Bus Voltage

Eq.(3-1) gives the equation for buckboost in DCM, where  $R_{buckboost}$  is the equivalent load of the *Buckboost Converter*.

$$D_{buckboost} = \frac{V_{buckboost}}{V_{in}} \sqrt{\frac{2L_{in} \cdot f_{buckboost}}{R_{buckboost}}} \quad (3-1)$$

$$D = \frac{\delta}{\pi} \quad (3-2)$$

The turn ratio of *Full Bridge Inverter* is:

$$N = \frac{N_p}{N_s} \quad (3-3)$$

The relationship between rms output voltage  $V_o$  and DC input voltage  $V_{buckboost}$  of the *Full Bridge Inverter* is given in Eq.(3-4). The derivation of the equation will be given in section 4.4 and Appendix A1.

$$V_o = \frac{1}{N} \cdot 0.9 \cdot \sin \frac{\delta}{2} \cdot V_{buckboost} \quad (3-4)$$

The power transferred by the *Buckboost Converter* equals to that of the output.

$$P_o = P_{buckboost} \cdot \eta \quad (3-5)$$

Hence,

$$\frac{V_{buckboost}^2}{R_{buckboost}} \cdot \eta = \frac{V_o^2}{R_d} \quad (3-6)$$

By substitute (3-4) into (3-6), we can get the expression of the equivalent load of the *Buckboost Converter*.

$$R_{buckboost} = \frac{V_{buckboost}^2}{V_o^2} \cdot R_d \cdot \eta = \frac{N^2}{\left(0.9 \sin \frac{\delta}{2}\right)^2} \cdot R_d \cdot \eta \quad (3-7)$$

From Fig. 2.2, we get the the duty cycle of the *Buckboost Converter*:

$$D_{buckboost} = \frac{1}{m} \cdot D \quad (3-8)$$

The switching frequency of the *Buckboost Converter* is:

$$f_{buckboost} = \frac{2f_{sw}}{m} \quad (3-9)$$

Substitute Eq.(3-2), (3-4), (3-7), (3-8) and (3-9) into (3-1), we get:

$$D = \frac{V_o}{V_{in}} \sqrt{\frac{4m \cdot L_{in} \cdot f_{sw}}{R_d \cdot \eta}} \quad (3-10)$$

For a given input and output voltage and load, we can calculate out the duty cycle of the *Full Bridge Inverter* by using Eq.(3-10). Combine Eq.(3-2), (3-4) and (3-10), we can get the DC bus voltage  $V_{buckboost}$ .

$$V_{buckboost} = \frac{NV_o}{0.9 \sin \left( \frac{V_o}{2V_{in}} \cdot \sqrt{\frac{4m \cdot L_{in} \cdot f_{sw}}{R_d \cdot \eta}} \cdot \pi \right)} \quad (3-11)$$

(3-11) indicates that the DC bus voltage is load dependent and determined by the value of inductor  $L_{in}$ , switching frequency  $f_{sw}$  and *Gate Signal Constant*  $m$ .

### 3.3.2 Peak Current of the Converter

The peak current through inductor  $L_{in}$  during the  $k^{th}$  interval is given in Eq.(3-12), where  $n$  is the number of intervals:

$$i_{Lin, peak, k} = \frac{|\sqrt{2}V_{in} \sin(2\pi k / n)|}{L_{in}} \cdot \frac{D_{buckboost}}{f_{buckboost}} \quad (3-12)$$

The maximum peak current through inductor  $L_{in}$  in one line cycle is:

$$i_{Lin, peak, max} = \frac{\sqrt{2}V_{in}}{L_{in}} \cdot \frac{D_{buckboost}}{f_{buckboost}} \quad (3-13)$$

Substitute Eq.(3-8), (3-9) into Eq.(3-13), we get the maximum input peak current.

$$i_{Lin, peak, max} = \sqrt{2}V_o \cdot \sqrt{\frac{m}{L_{in} \cdot f_{sw} \cdot R_d \cdot \eta}} \quad (3-14)$$

### 3.3.3 Boundary between DCM and CCM

The output current of the *Buckboost Converter* can be expressed as:

$$I_{buckboost} = \frac{V_{buckboost}}{R_{buckboost}} = \frac{V_{buckboost}}{R_d \cdot \eta} \cdot \frac{\left(0.9 \sin \frac{\delta}{2}\right)^2}{N^2} \quad (3-15)$$

The boundary of the output current of the *Buckboost Converter* is given below [12]:

$$I_{OB, buckboost} = \frac{V_{buckboost}}{2L_{in} \cdot f_{buckboost}} \cdot (1 - D_{buckboost})^2 \quad (3-16)$$

In order to let the *Buckboost Converter* work in DCM, the output current of it must be smaller than the boundary current.

$$I_{buckboost} < I_{OB, buckboost} \quad (3-17)$$

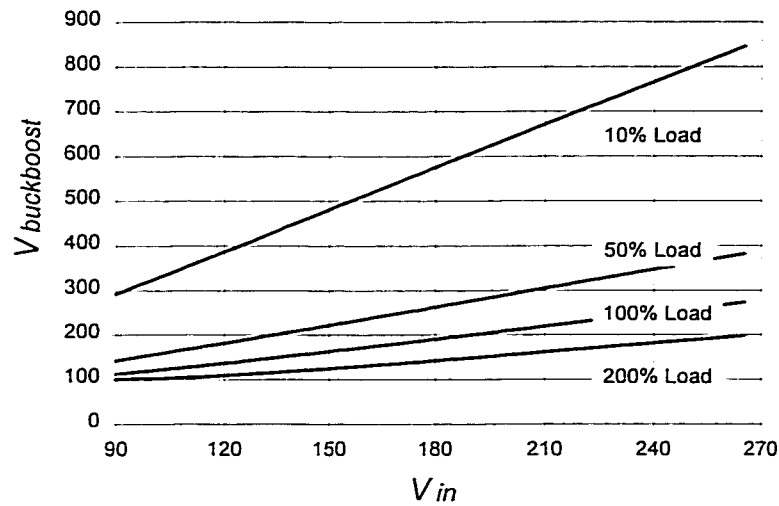
Substitute Eq.(3-8), (3-9) and (3-15) into Eq.(3-17), we get the equation that judge the *Buckboost Converter* is in DCM or not.

$$\frac{\left(0.9 \sin \frac{\delta}{2}\right)^2}{D\left(1 - \frac{1}{m} D\right)^2} < \frac{m \cdot N^2 \cdot R_d \cdot \eta}{4L_{in} \cdot f_{sw}} \quad (3-18)$$

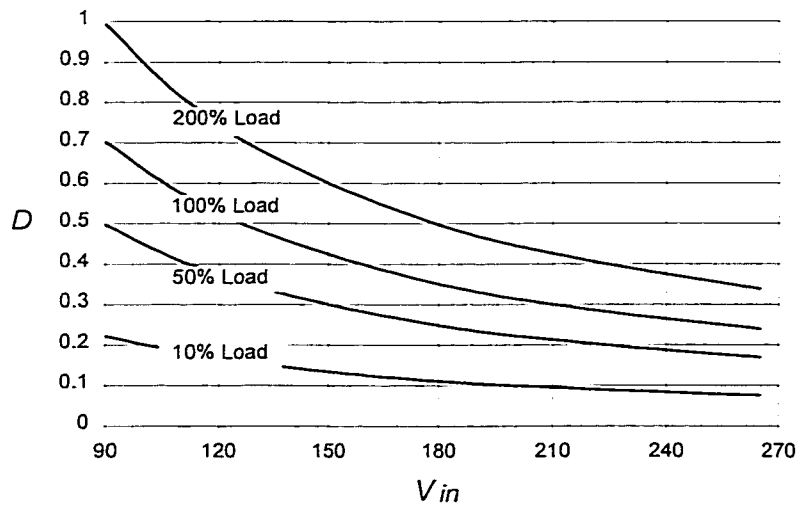
### 3.4 PERFORMANCE CHARACTERISTICS

#### 3.4.1 Effect of Load on Performance

Similar to the *Boost Converter*, the DC bus voltage of the *Buckboost Converter* is load dependent. The DC bus voltage can be very high at light load. Fig. 3.7 and Fig. 3.8 give the characteristics of the DC bus voltage and the duty cycle versus load.



**Fig. 3.7** DC bus voltage versus input voltage for various loads (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $N=3$ ,  $L_{in}=20\mu H$ ,  $m=2$ )

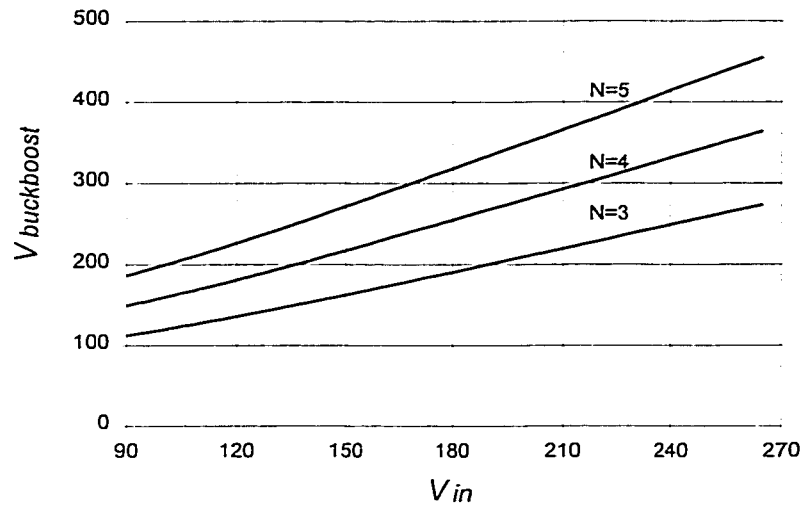


**Fig. 3.8** Duty cycle versus input voltage for various load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $N=3$ ,  $L_{in}=20\mu H$ ,  $m=2$ )

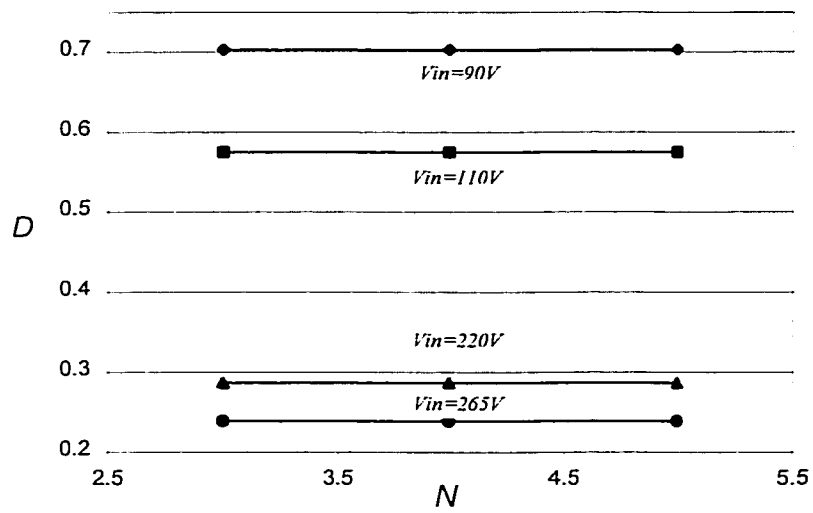
### 3.4.2 Effect of Transformer Turn Ratio on Performance

The effect of transformer turn ratio on the DC bus voltage is given in Fig. 3.9. Fig. 3.10 shows that the duty cycle is independent from the transformer turn ratio.





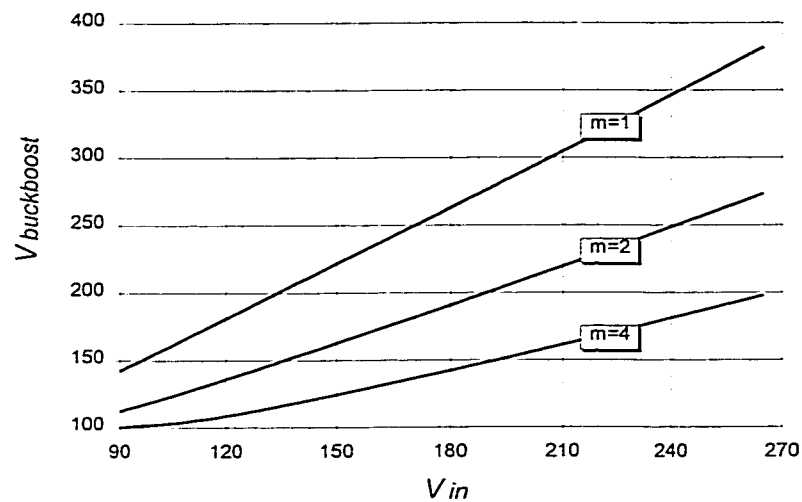
**Fig. 3.9** DC bus voltage versus input voltage for various transformer turn ratio (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=20\mu H$ ,  $m=2$ )



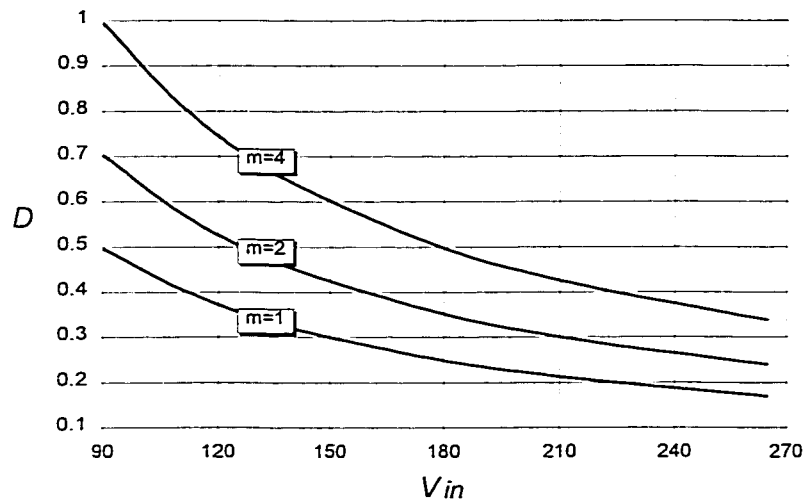
**Fig. 3.10** Duty cycle versus input voltage for various transformer turn ratio (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=20\mu H$ ,  $m=2$ )

### 3.4.3 Effect of $m$ on Performance

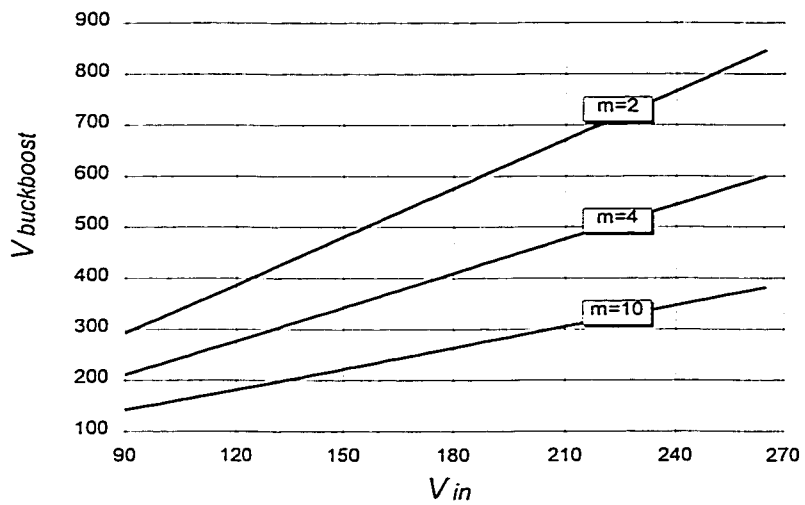
Fig. 3.11 to Fig. 3.14 illustrate the effect of *Gate Signal Constant*  $m$  on the DC bus voltage and the duty cycle. Increasing  $m$  is the main means to reduce the DC bus voltage at light load. However, for the *Buckboost* implemented PF corrected inverter,  $m$  can not be too large. Otherwise, at low line and heavy load, the DC bus voltage can not go high enough to maintain the required output voltage. In this design  $m$  is suggested to be 2 or 4.



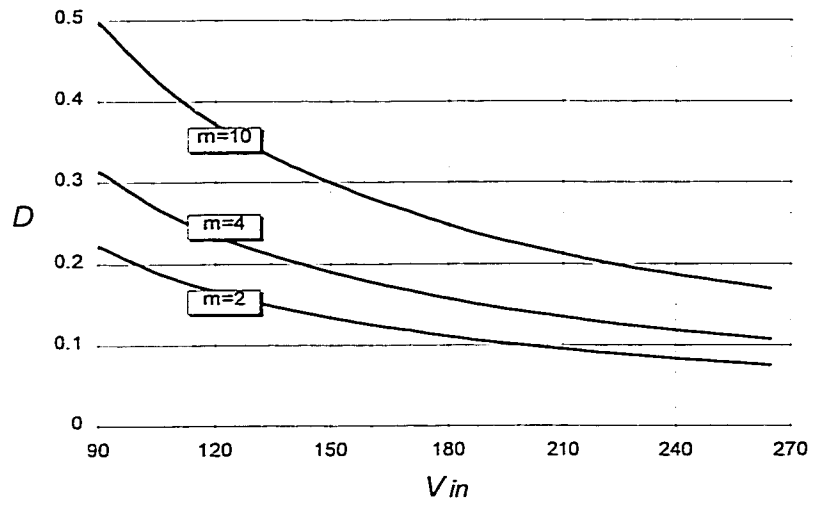
**Fig. 3.11** DC bus voltage versus input voltage for various  $m$  at rated load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100\text{KHz}$ ,  $R_d=3.6\Omega$ ,  $L_{in}=20\mu\text{H}$ ,  $N=3$ )



**Fig. 3.12** Duty cycle versus input voltage for various  $m$  at rated load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=3.6\Omega$ ,  $L_{in}=20\mu H$ ,  $N=3$ )



**Fig. 3.13** DC bus voltage versus input voltage for various  $m$  at 10% rated load (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=36\Omega$ ,  $L_{in}=20\mu H$ ,  $N=3$ )



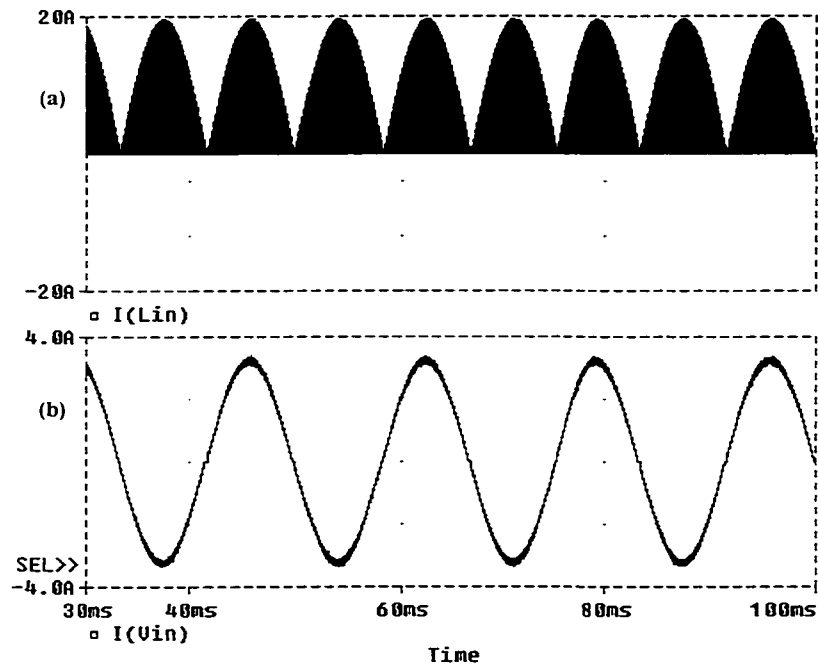
**Fig. 3.14** Duty cycle versus input voltage for various  $m$  at 10% rated load  
 (at  $V_o=30V_{ac}$ ,  $f_{sw}=100KHz$ ,  $R_d=36\Omega$ ,  $L_{in}=30\mu H$ ,  $N=3$ )

### 3.5 SIMULATION AND EXPERIMENTAL VERIFICATION

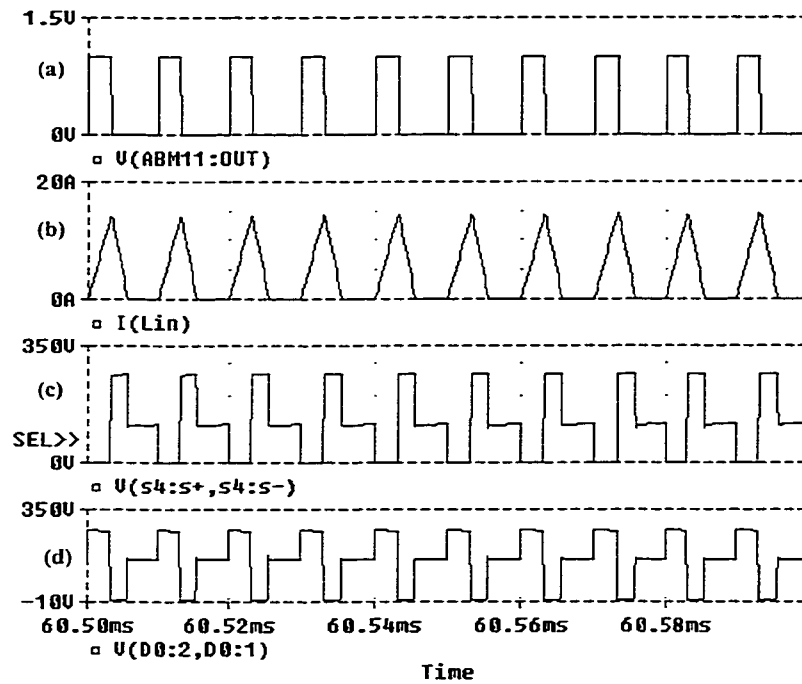
Similar to section 2.6 the simulation and experiment circuits in this section are based on the design example given in Chapter 5, which has a  $30V_{ac}$ ,  $100kHz$  output voltage,  $250W$  output, with  $90-265V_{ac}$  input voltage. The detailed specifications are given in section 5.1.

#### 3.5.1 Simulation Results

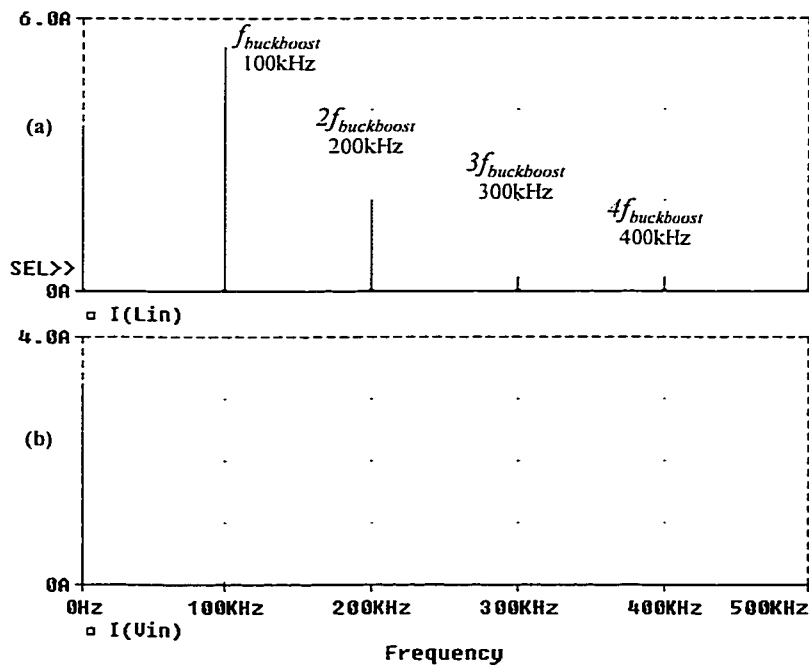
Fig. 3.15 to Fig. 3.18 give the simulation waveforms of the *Buckboost Converter* in the ac-ac inverter. The simulation is running at  $110V_{ac}$  input,  $250W$  output power.



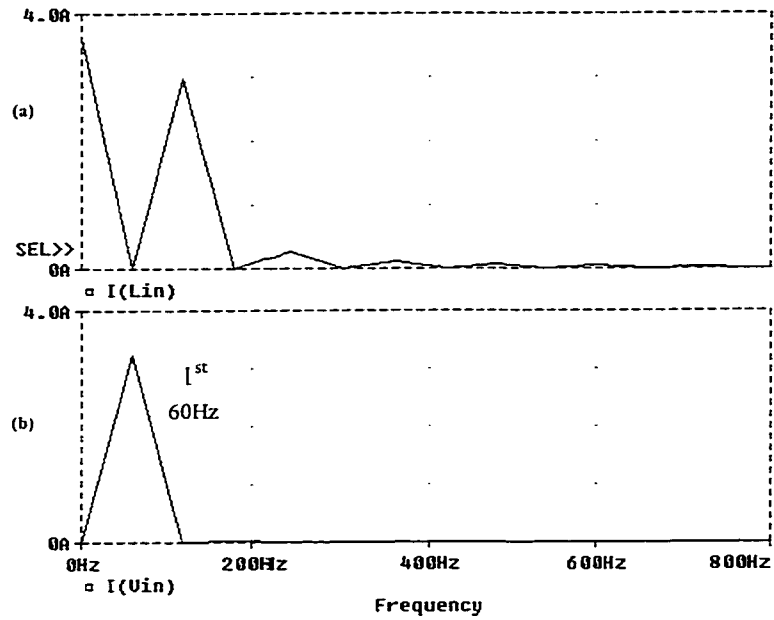
**Fig. 3.15** (a) Simulation waveform of the buckboost inductor current;  
(b) Simulation waveform of the filtered input current



**Fig. 3.16** (a) Simulation waveform of the *Buckboost Converter* gate signal; (b) Simulation waveform of the buckboost inductor current after zoom; (c) Simulation waveform of the voltage across the buckboost switch; (d) Simulation waveform of the voltage across the buckboost diode



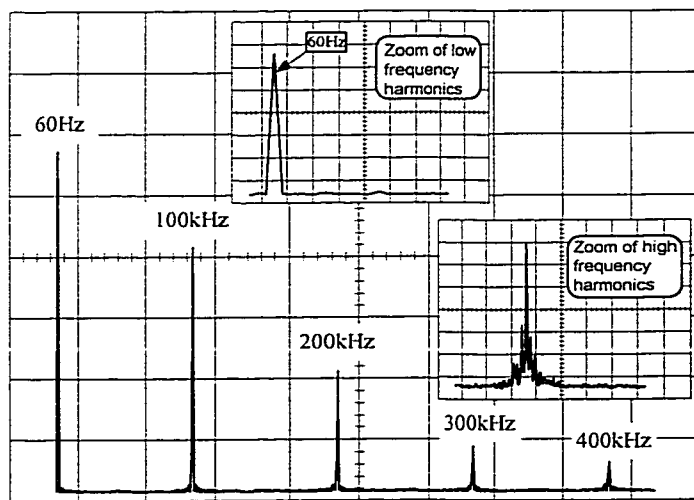
**Fig. 3.17** (a) Simulated high frequency harmonic spectrum of the buckboost inductor current; (b) Simulated high frequency harmonic spectrum of the filtered line current



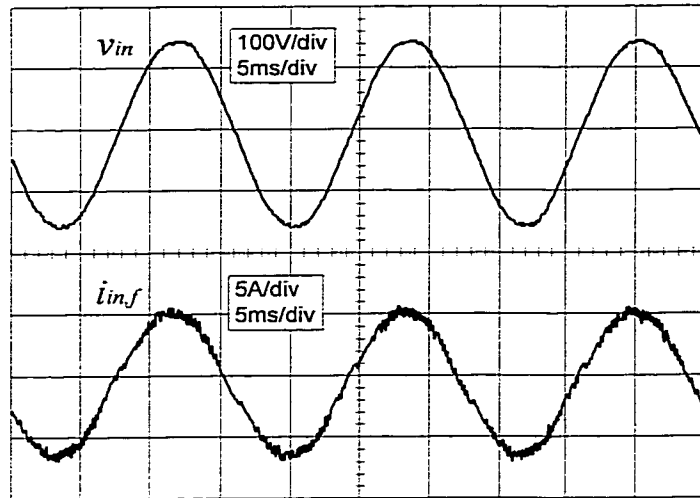
**Fig. 3.18** (a) Simulated low frequency harmonic spectrum of the buckboost inductor current; (b) Simulated low frequency harmonic spectrum of the filtered line current

### 3.5.2 Experimental Results

Fig. 3.19 shows the harmonics of the unfiltered line current. The high frequency harmonics can be filtered out by the *Input Filter*. The filtered line current waveform is given in Fig. 3.20. A power factor of 0.991 can be achieved.



**Fig. 3.19** Measured harmonics of unfiltered line current



**Fig. 3.20** Experimental waveforms of line voltage and filtered line current (at 110V<sub>ac</sub> line input and 250W output)

Table 3.1 gives the measured experimental data. The input power factor of the buckboost implementation is higher than that of the boost implementation, and its DC bus voltage is lower. However, the voltage stress on the buckboost diode and switch is almost twice of the boost diode and switch.

$V_{in}$ (V)	PF	$V_{dc}$ (V)	$V_{D0}, V_{S0}$ (V)	$V_o$ THD
90	0.988	138.5	252.3	0.00%
110	0.991	149.2	261.1	1.34%
135	0.990	170.1	320.5	2.02%
180	0.991	213.1	427.8	2.83%
220	0.982	258.8	513.7	3.04%
265	0.975	310.8	580.1	3.26%

**Table 3.1** Measured experimental data for various input voltages at 250W



### **3.6 CONCLUSION**

Simulation and experimental results show that the buckboost implemented PFC stage has a very high input power factor of 0.99. The DC bus voltage is lower than that of the boost implementation. However, in the worst case, the buckboost diode and switch will tolerate a voltage stress up to twice of the DC bus voltage.

## CHAPTER 4

# FULL BRIDGE ZVS RESONANT INVERTER

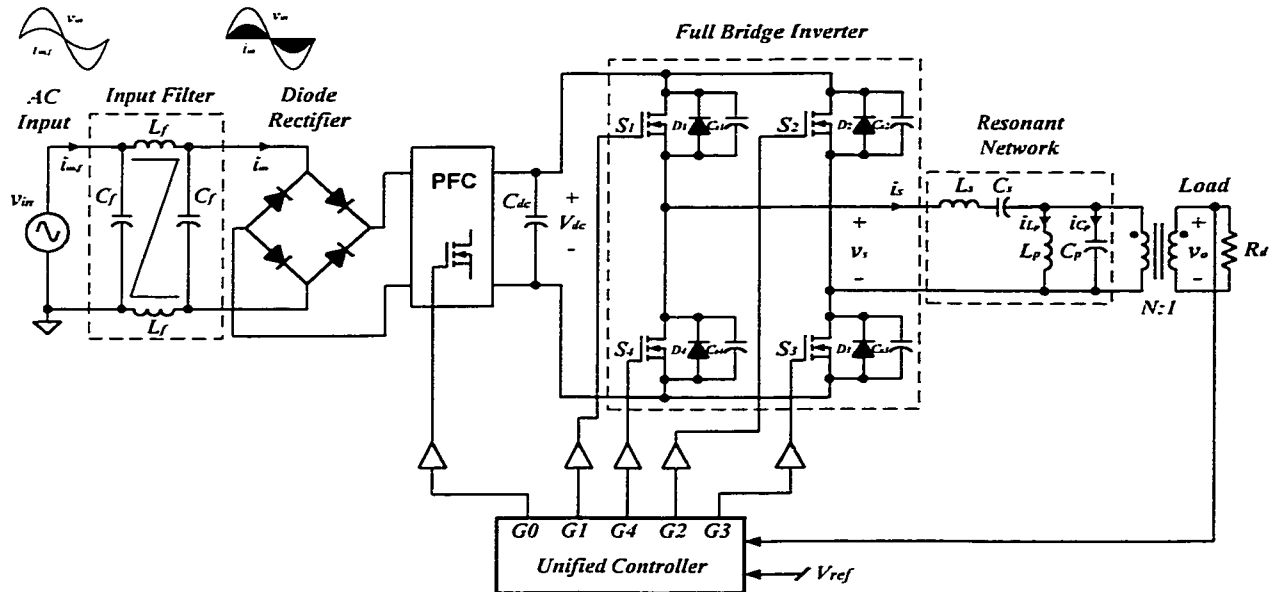
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### 4.1 INTRODUCTION

This chapter presents a high frequency dc-ac inverter operating under ZVS achieved by a *Resonant Network*. The proposed inverter adopts full bridge topology with phase-shift control pattern. The output frequency of the inverter is determined by the switching frequency. The amplitude of the output voltage is controlled by the phase-shift angle. Near zero switching losses and very low output voltage Total Harmonics Distortion (THD) can be achieved. Low conduction and circulating losses can also be achieved by optimizing the circuit parameters.

Principle and modes of operation are described thoroughly in section 4.2 and 4.3 respectively to understand the behavior of the circuits. Steady state analysis of the proposed inverter is presented in section 4.4. Performance characteristics are also given in section 4.5 to guide the design.

## 4.2 PRINCIPLE OF OPERATION



**Fig. 4.1** Proposed high frequency full bridge inverter

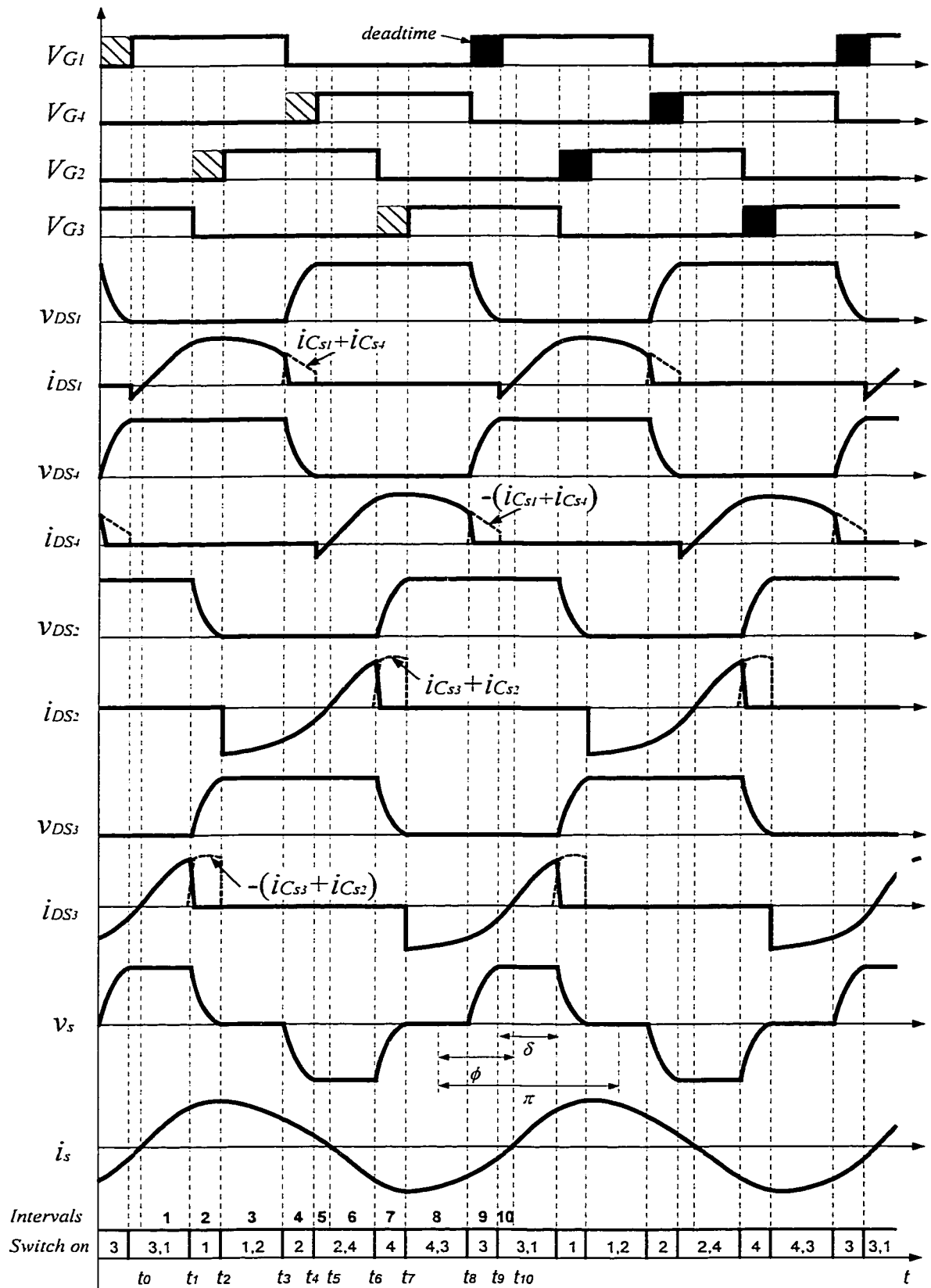
The *Full Bridge Inverter* adopts phase-shift control pattern so that zero-voltage switching can be realized in the proposed topology [24] [25]. The output of the *Full Bridge Inverter* is a quasi-square voltage waveform, which is converted into sinusoidal waveform by the *Resonant Network*.

The *Resonant Network* consists of a series and parallel branch. The series branch is made up of an inductor  $L_s$  and a capacitor  $C_s$ . The parallel branch consists of a parallel inductor  $L_p$  and capacitor  $C_p$ . The series branch is tuned to the switching frequency so that the fundamental component of the quasi-square waveform can pass without magnitude reduction and the harmonics can be stopped by the series branch. The parallel branch can be either tuned or off tuned, depending on specific applications [26].

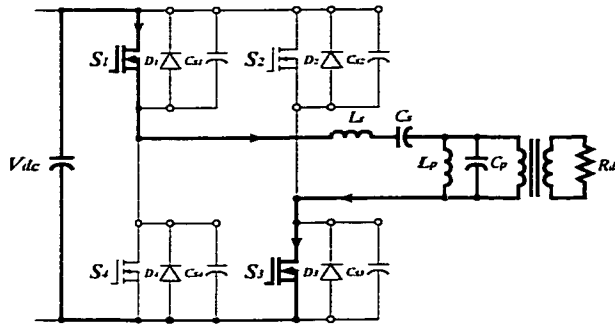
If the series and the parallel branch are both tuned, the *Full Bridge Inverter* and the *Resonant Network* form an ideal voltage source [18]. The output voltage is load independent and the current through the series branch decreases from rated value to zero as the load decreases from rated value to zero. Under this operation mode, the output current of the *Full Bridge Inverter* is in phase with its output voltage. Thus the right leg switch  $S_2$  and  $S_3$  are turned on under zero-voltage and the left leg switch  $S_1$  and  $S_4$  are turned off under zero-voltage. The turn off zero-voltage can be achieved by placing snubber capacitors across the switches. Hence, only two switches have turn on losses under this mode.

However, in high frequency applications, where frequency dependent losses are crucial, we hope all the turn on and turn off losses can be eliminated. In the proposed high frequency inverter, the series resonant branch is tuned, but the parallel branch is off tuned. The resonant frequency of the parallel branch is larger than the switching frequency, i.e.  $f_p > f_{sw}$ , so that the *Resonant Network* as a whole is inductive. Therefore, the output current of the *Full Bridge Inverter* lags its output voltage. As a result, turn on zero-voltage switching can be achieved for all the four switches. Turn off losses can also be eliminated if snubber capacitors are placed across the switches and if sufficient deadtime is given between the gating signals of the switches on the same leg. Fig. 4.2 clearly illustrates that all the four switches are turned on and off under zero-voltage.

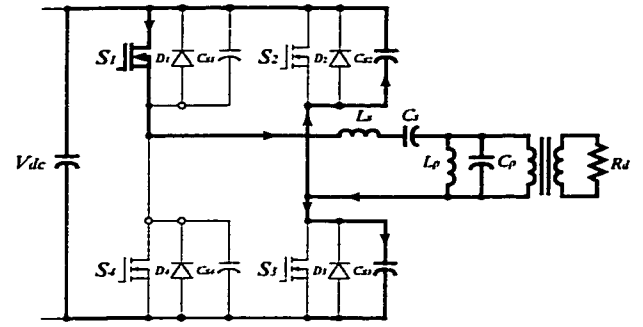
Since the series branch is tuned, the output voltage is load independent. Its frequency is determined by the switching frequency and its amplitude is controlled by the phase-shift angle.



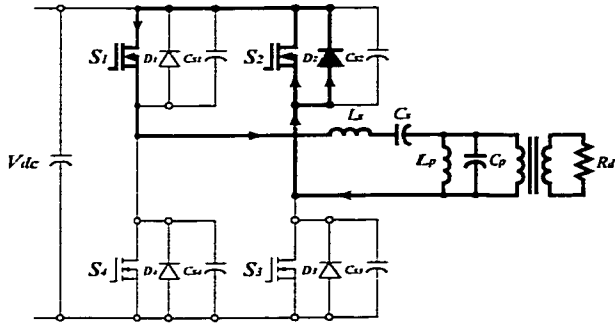
**Fig. 4.2** Key waveforms of the *Full Bridge Inverter*



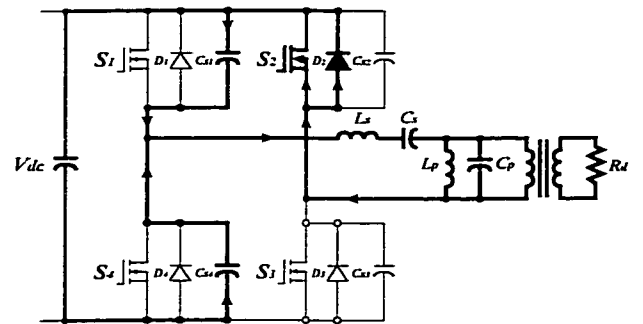
(a) Interval 1 ( $t_0 \sim t_1$ )



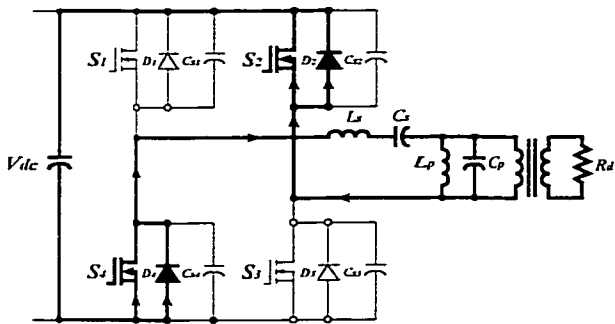
(b) Interval 2 ( $t_1 \sim t_2$ )



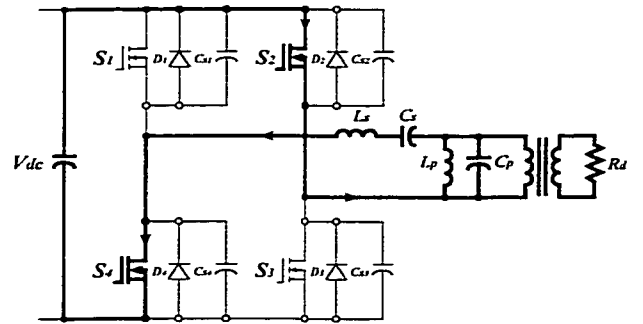
(c) Interval 3 ( $t_2 \sim t_3$ )



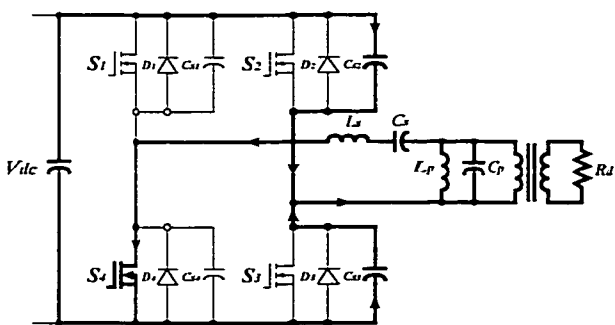
(d) Interval 4 ( $t_3 \sim t_4$ )



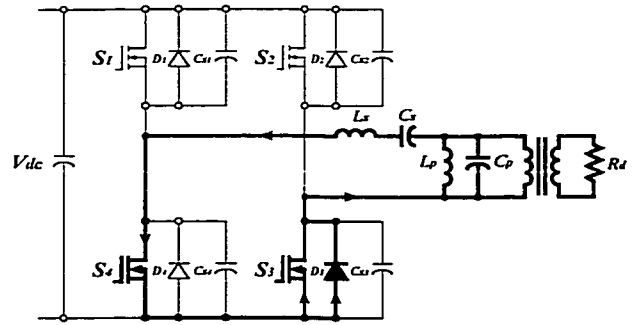
(e) Interval 5 ( $t_4 \sim t_5$ )



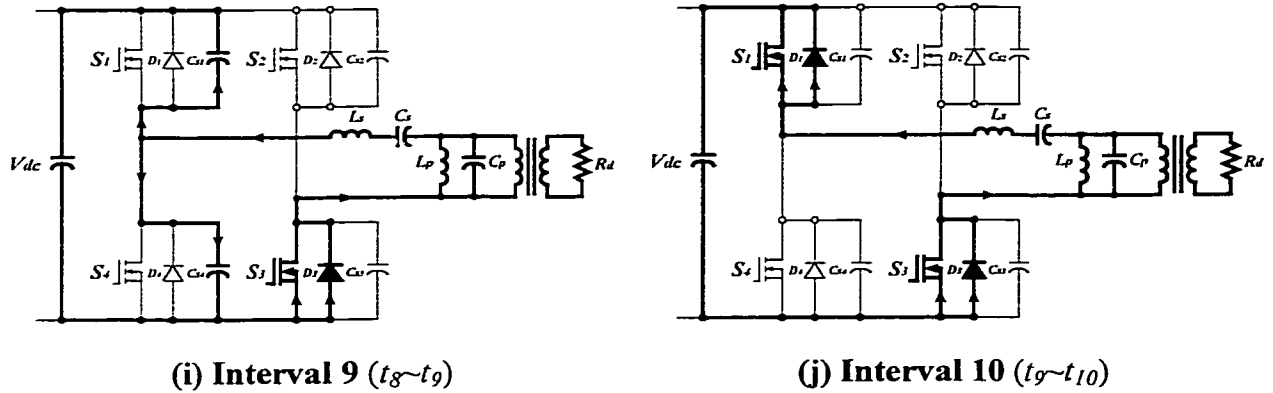
(f) Interval 6 ( $t_5 \sim t_6$ )



(g) Interval 7 ( $t_6 \sim t_7$ )



(h) Interval 8 ( $t_7 \sim t_8$ )



**Fig. 4.3** Current paths of the inverter during various intervals corresponding to the key waveforms given in Fig. 4.2

### 4.3 MODES OF OPERATION

The operation of the inverter can be divided into 10 different intervals during one switching cycle. After one switching cycle, the intervals repeat themselves. The key waveforms of the inverter have already been given in Fig. 4.2. The current path of each interval that corresponds to the waveforms in Fig. 4.2 is given in Fig. 4.3 (a-j).

- **Interval 1 ( $t_0 \sim t_1$ ):**

This interval starts at  $t_0$ , see Fig. 4.2. Switch  $S_1$  and  $S_3$  are conducting at the same while switch  $S_2$  and  $S_4$  are off. The power is delivered from the input to the output through switch  $S_1$  and  $S_3$ . The current path of this interval is given in Fig. 4.3 (a).

- **Interval 2 ( $t_1 \sim t_2$ ):**

During this interval, switch  $S_3$  is turned off, but switch  $S_1$  is still on. As we have analyzed in section 4.2, the *Resonant Network* is designed to be inductive so that the output

current of the *Full Bridge Inverter* will lag the voltage. Therefore, the primary current will maintain the same direction as that in interval 1. The primary current charges the snubber capacitor  $C_{S3}$  from zero to the DC bus voltage, and discharges capacitor  $C_{S2}$  from the DC bus voltage to zero simultaneously, see Fig. 4.3 (b). If the snubber capacitor  $C_{S3}$  is large enough, a near zero turn off loss can be achieved for switch  $S_3$ . Since this interval is determined by the delaytime between the gate signals of switch  $S_2$  and  $S_3$ , the delaytime should be long enough so that before switch  $S_2$  is turned on the snubber capacitor  $C_{S2}$  can be fully discharged. Otherwise, the rest of the energy stored in the snubber capacitor  $C_{S2}$  can not be pulled into the *Resonant Network* but dissipated in switch  $S_2$ .

- **Interval 3 ( $t_2 \sim t_3$ ):**

During this interval, switch  $S_1$  and  $S_2$  are conducting. The primary current will remain the same direction and circulate in the loop formed by switch  $S_1$ ,  $S_2$  and body diode  $D_2$ , see Fig. 4.3 (c). In this interval, the current flowing through the switch  $S_2$  is from source to drain, which shunts the body diode, thus reduces conduction losses.

- **Interval 4 ( $t_3 \sim t_4$ ):**

Switch  $S_1$  is turned off and only switch  $S_2$  is conducting. The primary current keeps the same direction. Snubber capacitor  $C_{S1}$  is charged, and  $C_{S4}$  is discharged during this interval, see Fig. 4.3 (d). In order to ensure the snubber capacitor  $C_{S1}$  and  $C_{S4}$  can be entirely charged and discharged respectively, the deadtime between switch  $S_1$  and  $S_4$  should be long enough.

- **Interval 5 ( $t_4 \sim t_5$ ):**



Switch  $S_4$  is turned on, and switch  $S_2$  is still on. The primary current is circulating through switch  $S_2$  and  $S_4$  from source to drain. The current will also go through body diode  $D_2$  and  $D_4$ , thus reduce conduction losses, see Fig. 4.3 (e). This interval will exist only if the lag angle  $\phi > (\pi - \delta)/2$ . If  $\phi = (\pi - \delta)/2$ , the circuits will skip to interval 6.

- **Interval 6 ( $t_5 \sim t_6$ ):**

The primary current changes its direction, going through switch  $S_2$  and  $S_4$  from drain to source. The power is transferred from input to output, see Fig. 4.3 (f).

- **Interval 7 ( $t_6 \sim t_7$ ):**

Switch  $S_2$  is turned off. The primary current is charging snubber capacitor  $C_{S2}$  and discharging snubber capacitor  $C_{S3}$  through switch  $S_4$  at the same time, see Fig. 4.3 (g).

- **Interval 8 ( $t_7 \sim t_8$ ):**

Switch  $S_3$  is turned on. The primary current is circulating through switch  $S_3$ ,  $S_4$  and diode  $D_3$  at the same time, see Fig. 4.3 (h). The current flowing through switch  $S_3$  is from source to drain.

- **Interval 9 ( $t_8 \sim t_9$ ):**

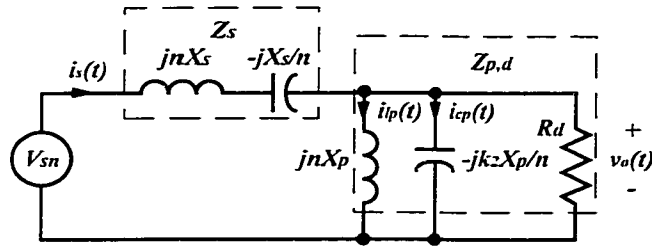
Switch  $S_4$  is turned off at the beginning of this interval. Switch  $S_3$  is reverse conducting. Snubber capacitor  $C_{S1}$  is discharged, and  $C_{S4}$  is charged, see Fig. 4.3 (i).

- **Interval 10 ( $t_9 \sim t_{10}$ ):**

Switch  $S_1$  is and  $S_3$  are conducting at the same time. However, the primary current will flow from drain to source. Body diode  $D_1$  and  $D_3$  is also conducting, thus shunt the current, see Fig. 4.3 (j).

#### 4.4 STEADY STATE ANALYSIS

The following assumptions are made first to simplify the steady state analysis: (1) The output voltage of the *Full Bridge Inverter* is an ideal quasi-square waveform, see Appendix A1, Fig A.1. (2) The transformer turn ratio is one. (3) The resonant inductors and capacitors are ideal. (4) The load is resistive.



**Fig. 4.4**  $n^{\text{th}}$  harmonic equivalent circuit (per unit) of the inverter

The  $n^{\text{th}}$  harmonic equivalent circuit is given in Fig. 4.4, where the series branch is tuned to the switching frequency and the parallel branch is off tuned.  $X_s$  is the impedance of the series inductor and capacitor at switching frequency.  $X_p$  is the impedance of the parallel inductor.  $X_{cp}$  is the impedance of the parallel capacitor, and  $R_d$  is the load resistance.

***Three important constants:***

$k_1$ ,  $k_2$  and  $k_3$  are given in Eq.(4-1), (4-2) and (4-3) respectively. They are the key constants used in the following steady state analysis.

$$k_1 = X_s / X_p \quad (4-1)$$

$$k_2 = X_{cp} / X_p \quad (4-2)$$

$$k_3 = X_p / R_d \quad (4-3)$$

**Output voltage of the Full Bridge Inverter:**

Ideally, the output voltage of the *Full Bridge Inverter* is a quasi-square waveform. Therefore, we can get the fourier series for the quasi-square waveform as below. The derivation of this fourier series is given in Appendix A1.

$$v_s(t) = \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{n\pi} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \sin n\omega t \quad (4-4)$$

**Current through the series branch:**

The overall impedance of the *Resonant Network* is given in Eq.(4-4):

$$Z_n = Z_s + Z_{p,d} = \text{Re}(Z_n) + \text{Im}(Z_n) \cdot j \quad (4-5)$$

Where:

$$\text{Re}(Z_n) = \frac{R_d}{1 + (R_d / X_p)^2 \cdot (n / k_2 - 1 / n)^2} \quad (4-6)$$

$$\text{Im}(Z_n) = \frac{X_s \cdot (n - 1 / n) + \frac{X_s R_d^2}{X_p^2} \cdot (n - 1 / n)(n / k_2 - 1 / n)^2 - \frac{R_d^2}{X_p} \cdot (n / k_2 - 1 / n)}{1 + \left(\frac{R_d}{X_p}\right)^2 \cdot (n / k_2 - 1 / n)^2} \quad (4-7)$$

$$|Z_n| = \sqrt{\text{Re}(Z_n)^2 + \text{Im}(Z_n)^2} \quad (4-8)$$

$$\phi_n = \tan^{-1} \left| \frac{\text{Im}(Z_n)}{\text{Re}(Z_n)} \right| \quad (4-9)$$

Therefore, the current through the series branch is given:

$$i_s(t) = \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{n\pi|Z_n|} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \sin(n\omega_s t - \phi_n) \quad (4-10)$$

***Phase lag angle of the Resonant Network:***

The phase lag angle of the *Resonant Network* will determine whether ZVS can be achieved in the *Full Bridge Inverter* or not. If the resonant components are properly designed, the current through the series branch will be very close to a sinusoidal waveform. Therefore, we can ignore the harmonics to calculate the phase lag angle:

$$\phi = \tan^{-1} \left. \frac{\text{Im}(Z_n)}{\text{Re}(Z_n)} \right|_{n=1} = \tan^{-1} \left[ -\frac{1}{k_3} \cdot \left( \frac{1}{k_2} - 1 \right) \right] \quad (4-11)$$

***Minimum phase-shift angle of the Full Bridge Inverter:***

In order to achieve ZVS for the *Full Bridge Inverter*, the phase lag angle of the *Resonant Network*  $\phi > \frac{\pi - \delta}{2}$ . Fig. 4.2 clearly illustrated this. Thus, the minimum phase-shift angle is given below:

$$\delta_{\min} = \pi - 2\phi = \pi - 2 \cdot \tan^{-1} \left[ -\frac{1}{k_3} \cdot \left( \frac{1}{k_2} - 1 \right) \right] \quad (4-12)$$

***Voltage across the series capacitor:***

The expression of the voltage across the series capacitor is given:

$$v_{cs}(t) = i_s(t) \cdot (-jX_s / n) = - \sum_{n=1,3}^{\infty} \frac{4V_{dc}X_s}{n^2 \pi |Z_n|} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega_s t - \phi_i) \quad (4-13)$$

**Voltage across the series inductor:**

The expression of the voltage across the series capacitor is given:

$$v_{cs}(t) = i_s(t) \cdot (-jX_s / n) = - \sum_{n=1,3}^{\infty} \frac{4V_{dc}X_s}{n^2 \pi |Z_n|} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega_s t - \phi_i) \quad (4-14)$$

**Output voltage across the load:**

The output voltage across the load is:

$$v_o(t) = v_s(t) \cdot \frac{Z_{p, Load}}{Z_{p, Load} + Z_s} = \frac{v_s(t)}{|Z_i| \angle \phi_i} = \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{n\pi |Z_i|} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \sin(n\omega_s t - \phi_i) \quad (4-15)$$

Where,

$$\frac{Z_{p, Load}}{Z_{p, Load} + Z_s} = \frac{1}{Z_i} = \frac{1}{|Z_i| \angle \phi_i} \quad (4-16)$$

$$Z_i = \text{Re}(Z_i) + \text{Im}(Z_i) \cdot j \quad (4-17)$$

$$|Z_i| = \sqrt{\text{Re}(Z_i)^2 + \text{Im}(Z_i)^2} \quad (4-18)$$

$$\text{Re}(Z_i) = 1 - \frac{X_s}{X_p} \cdot (n - 1/n) \cdot (n/k_2 - 1/n) \quad (4-19)$$

$$\text{Im}(Z_i) = \frac{X_s}{R_d} \cdot (n - 1/n) \quad (4-20)$$

$$\phi_i = \tan^{-1} \frac{\text{Im}(Z_i)}{\text{Re}(Z_i)} \quad (4-21)$$

If the *Resonant Network* is properly designed, the output harmonics should be very small, therefore they can be ignored. Then the rms value of the output voltage is given below [18]:

$$V_o = 0.9 \cdot \sin \frac{\delta}{2} \cdot V_{dc} \quad (4-22)$$

**Current through the parallel capacitor:**

$$i_{cp}(t) = \frac{v_o(t)}{-jk_2 X_p / n} = \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{\pi |Z_i| k_2 X_p} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega t - \phi_i) \quad (4-23)$$

**Current through the parallel inductor:**

$$i_{lp}(t) = \frac{v_o(t)}{jnX_p} = -\sum_{n=1,3}^{\infty} \frac{4V_{dc}}{n^2 \pi |Z_i| X_p} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega t - \phi_i) \quad (4-24)$$

**RMS values of the resonant components:**

Since the current through the series or parallel branch is near sinusoidal, we can ignore the harmonics, and get the rms value of the voltage and current approximately:

The rms value of the voltage across the series capacitor and inductor is:

$$V_{cs} = V_{ls} = \left| -\sum_{n=1,3}^{\infty} \frac{4V_{dc} X_s}{n^2 \pi |Z_n|} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega t - \phi_i) \right|_{n=1} \quad (4-25)$$

The rms value of the current through the series branch is:

$$\begin{aligned} I_s = |i_s(t)| &= \left| \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{n\pi |Z_n|} \cdot \sin \cdot \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \sin(n\omega t - \phi_i) \right|_{n=1} \\ &= \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{R_d} \cdot \sqrt{1 + (1/k_3)^2 \cdot (1/k_2 - 1)^2} \end{aligned} \quad (4-26)$$

The rms value the circulating current in the parallel inductor is:

$$\begin{aligned}
I_{ip} = |i_{ip}(t)| &= \left| \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{\pi |Z_i| X_p} \cdot \sin \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega_s t - \phi_i) \right|_{n=1} \\
&= \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{X_p}
\end{aligned} \tag{4-27}$$

The rms value of the circulating current through the parallel capacitor is:

$$\begin{aligned}
I_{cp} = |i_{cp}(t)| &= \left| \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{\pi |Z_i| k_2 X_p} \cdot \sin \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega_s t - \phi_i) \right|_{n=1} \\
&= \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{k_2 X_p}
\end{aligned} \tag{4-28}$$

The rms value of the output load current is:

$$\begin{aligned}
I_o = |i_o(t)| &= \left| \sum_{n=1,3}^{\infty} \frac{4V_{dc}}{\pi R_d} \cdot \sin \frac{n\delta}{2} \cdot \sin \frac{n\pi}{2} \cdot \cos(n\omega_s t - \phi_i) \right|_{n=1} \\
&= \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{R_d}
\end{aligned} \tag{4-29}$$

***Relationship between resonant currents and load current:***

Combine Eq.(4-26) and (4-29), get:

$$\frac{I_s}{I_o} = \sqrt{1 + (1/k_3)^2 \cdot (1/k_2 - 1)^2} \tag{4-30}$$

Combine Eq.(4-27) and (4-29), get:

$$\frac{I_{ip}}{I_o} = \frac{1}{k_3} \tag{4-31}$$

Combine Eq.(4-28) and (4-29), get:

$$\frac{I_{cp}}{I_o} = \frac{1}{k_2 k_3} \quad (4-32)$$

**The total circulating losses are:**

$$P_{cl} = I_p^2 r_p = \left( \frac{I_s}{k_2} \right)^2 \cdot r_p = \left[ \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{k_2 R_d} \right]^2 \cdot r_p = \frac{0.81 \sin^2(\delta/2) \cdot V_{dc}^2}{k_2^2 R_d^2} \cdot r_p \quad (4-33)$$

**The worst THD of the output voltage**

The worst Total Harmonics Distortion of the output voltage happens when the load resistor is infinite. Therefore, the rms value of the  $n^{\text{th}}$  harmonics of the output voltage is:

$$V_{o,n} \Big|_{R_d \rightarrow \infty} = \frac{0.9 \sin(n\delta/2) \cdot V_{dc}}{n |Z_{in}|_{R_d \rightarrow \infty}} = \frac{0.9 \sin(n\delta/2) \cdot V_{dc}}{n [1 - k_1(n-1/n)(n/k_2 - 1/n)]} \quad (4-34)$$

The fundamental component of the output voltage is:

$$V_{o,1} = V_{o,n} \Big|_{R_d \rightarrow \infty, n=1} = \frac{0.9 \sin(n\delta/2) \cdot V_{dc}}{n [1 - k_1(n-1/n)(n/k_2 - 1/n)]} \Big|_{n=1} = 0.9 \sin \frac{\delta}{2} \cdot V_{dc} \quad (4-35)$$

Therefore, the worst THD is given below:

$$THD = \frac{\sqrt{\sum_{n=3.5}^{\infty} V_{o,n}^2}}{V_{o,1}} = \frac{\sqrt{\sum_{n=3.5}^{\infty} \left\{ \frac{0.9 \sin(n\delta/2)}{n \cdot \left[ 1 - \frac{k_1}{k_2} \left( n - \frac{1}{n} \right) \left( n - \frac{k_2}{n} \right) \right]} \right\}^2}}{0.9 \sin(\delta/2)} \quad (4-36)$$

**Snubber Capacitors:**

The value of the snubber capacitors are chosen in such a way that the allowable rise time  $t_{ar}$  is much larger than the specified rise time  $t_r$  for the switches in order to reduce the



turn off losses to an acceptable level. In practice,  $t_{ar}=3t_r$  [26]. The minimum value for snubber capacitors across switch  $S_l$  and  $S_r$  is:

$$C_{s1,4} = \frac{\sin\left(\frac{\delta_{\max}}{2}\right) \sqrt{1 + \frac{1}{k_3^2} \cdot \left(\frac{1}{k_2} - 1\right)^2}}{\pi^2 N^2 R_d f_{sw}} \left[ -\sin\left(\frac{\delta_{\max}}{2} + \phi + \omega t_{ar}\right) + \sin\left(\frac{\delta_{\max}}{2} + \phi\right) \right] \quad (4-37)$$

The minimum snubber capacitors across switch  $S_2$  and  $S_3$  should be:

$$C_{s2,3} = \frac{\sin\left(\frac{\delta_{\max}}{2}\right) \sqrt{1 + \frac{1}{k_3^2} \cdot \left(\frac{1}{k_2} - 1\right)^2}}{\pi^2 N^2 R_d f_{sw}} \left[ \sin\left(\frac{\delta_{\max}}{2} - \phi + \omega t_{ar}\right) - \sin\left(\frac{\delta_{\max}}{2} - \phi\right) \right] \quad (4-38)$$

### ***Determination of Minimum Deadtime***

The delaytime should be long enough so that the snubber capacitors can be fully discharged before the switches are turned on. The minimum deadtime between the gate signals of the switch  $S_l$  and  $S_r$  is given in Eq.(4-39), where  $\delta$  is at its minimum and  $R_d$  is at its maximum.

$$t_{d1,4} = \frac{1}{2\pi f_{sw}} \left\{ \pi - \arcsin \left[ \sin\left(\frac{\delta_{\min}}{2} + \phi\right) - \frac{\pi^2 N^2 R_{d,\max} C_{sf,sw}}{\sin\left(\frac{\delta_{\min}}{2}\right) \sqrt{1 + \frac{1}{k_3^2} \left(\frac{1}{k_2} - 1\right)^2}} \right] - \left(\frac{\delta_{\min}}{2} + \phi\right) \right\} \quad (4-39)$$

The minimum deadtime between the gate signal of the switch  $S_2$  and  $S_3$  is:

$$t_{d2,3} = \frac{1}{2\pi f_{sw}} \left\{ \arcsin \left[ \frac{\pi^2 N^2 R_{d, \max} C_s f_{sw}}{\sin \frac{\delta_{\min}}{2} \sqrt{1 + \frac{1}{k_3^2} \left( \frac{1}{k_2} - 1 \right)^2}} + \sin \left( \frac{\delta_{\min}}{2} - \phi \right) \right] - \left( \frac{\delta_{\min}}{2} - \phi \right) \right\} \quad (4-40)$$

### **Rating of Resonant Components:**

The rms value of the current through the series branch is:

$$I_s = \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{N^2 R_d} \cdot \sqrt{1 + (1/k_3)^2 \cdot (1/k_2 - 1)^2} \quad (4-41)$$

The rms value the circulating current in the parallel inductor is:

$$I_{lp} = \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{2\pi f_{sw} L_p} \quad (4-42)$$

The rms value of the circulating current through the parallel capacitor is:

$$I_{cp} = \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{2\pi f_{sw} k_2 L_p} \quad (4-43)$$

### **Rating of switches:**

RMS value of the switch current:

$$I_{RMS, S1} = I_{RMS, S4} = \sqrt{\frac{1}{2\pi} \int_0^{\pi - \omega t_d} \left\{ \sqrt{2} I_s \sin \left[ \omega t - \phi + \frac{1}{2} (\pi - \delta) \right] \right\}^2 d\omega t} \quad (4-44)$$

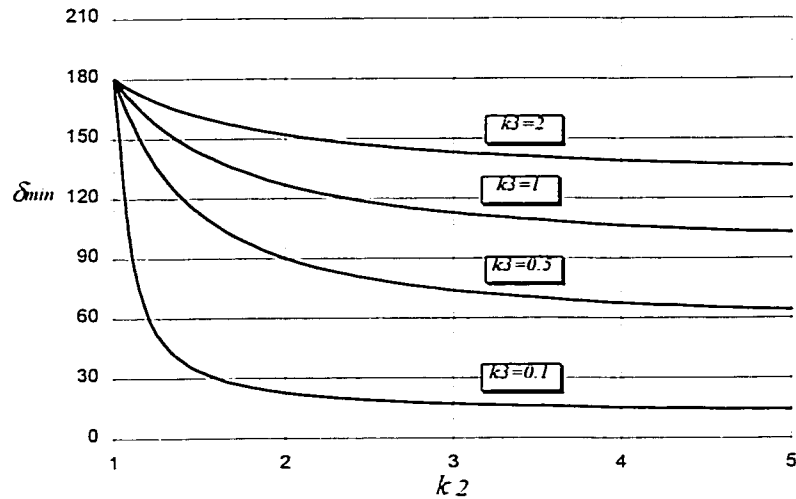
$$I_{RMS, S2} = I_{RMS, S3} = \sqrt{\frac{1}{2\pi} \int_0^{\pi - \omega t_d} \left\{ \sqrt{2} I_s \sin \left[ \omega t - \phi - \frac{1}{2} (\pi - \delta) + \omega t_d \right] \right\}^2 d\omega t} \quad (4-45)$$

## 4.5 PERFORMANCE CHARACTERISTICS

### 4.5.1 Minimum Phase-shift Angle

The phase lag angle  $\phi$  of the *Resonant Network* is essential in determining the zero-voltage switching of the *Full Bridge Inverter*.  $\phi$  is determined by the resonant components and load, the minimum phase-shift angle is given in Eq.(4-12). Fig. 4.5 gives the relationship between  $\delta_{min}$  and  $k_2$  for various  $k_3$ . We can see that, when  $k_2=1$ ,  $\delta_{min}$  always equals to  $180^\circ$ . This is because that when  $k_2=1$ , the parallel branch is also tuned. The *Full Bridge Inverter* and the *Resonant Network* therefore together form an ideal voltage source. When the ideal voltage source supplies a resistive load, the load current and voltage will be in phase (i.e.  $\phi=0^\circ$ ). Hence,  $\delta_{min}=180^\circ$ .

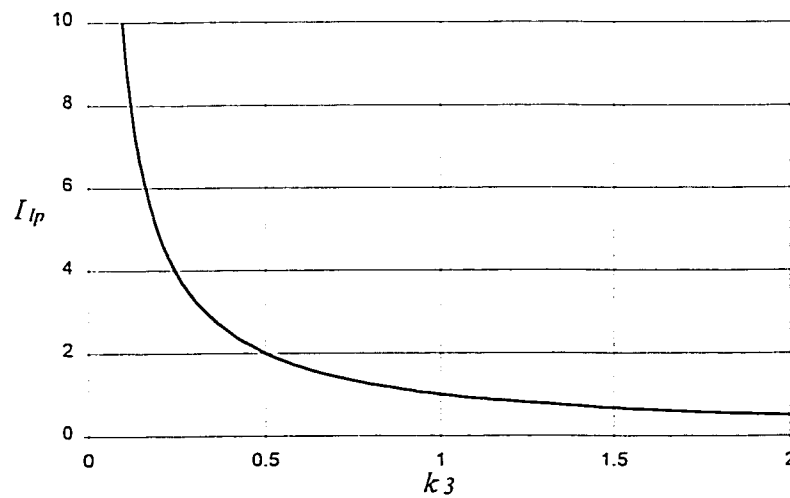
In order to let  $\delta_{min}$  as small as possible,  $k_2$  must be larger than 1 and  $k_3$  should be as small as possible. Note, when all the resonant components are selected, if the load resistor increases,  $k_3$  will decrease, which means at light load, the phase lag angle will be larger than that of rated load. Hence, the minimum phase-shift angle can be smaller at light load.



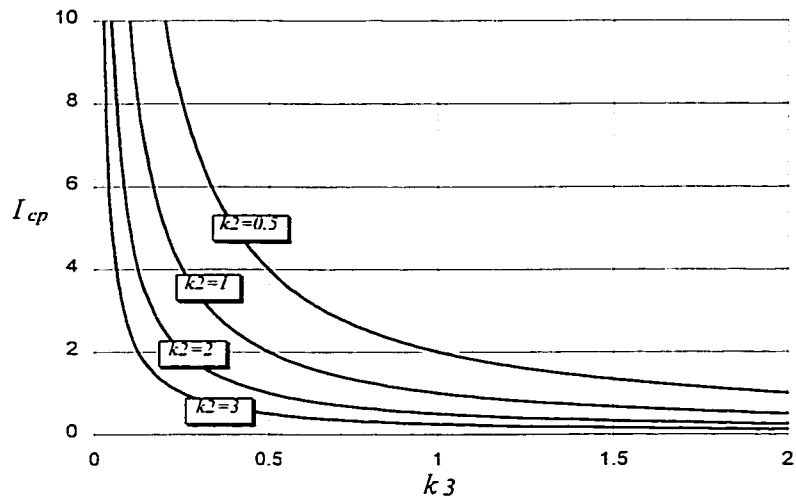
**Fig. 4.5** Minimum phase shift-angle  $\delta_{min}$  (degree) versus  $k_2$  for various  $k_3$

#### 4.5.2 Circulating Current

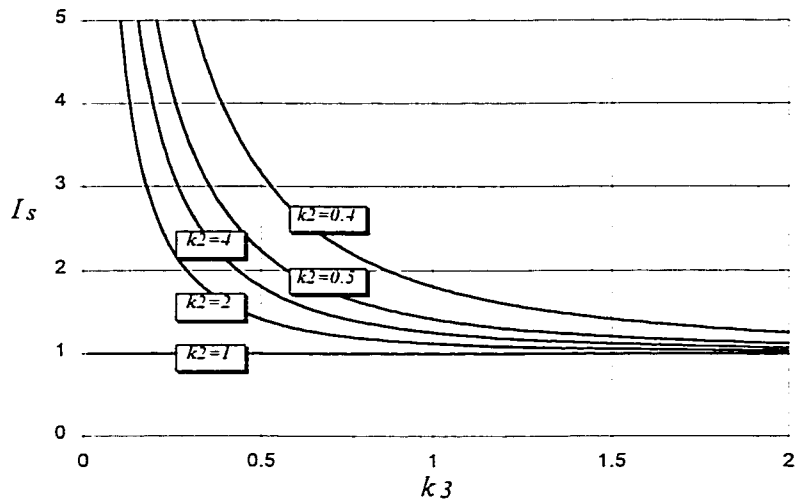
Fig. 4.6, Fig. 4.7 and Fig. 4.7 give the circulating currents as functions of  $k_3$ . For the sake of reducing the circulating losses, we prefer  $k_3$  to be as large as possible. However,  $k_3$  can not be too large, otherwise the minimum phase-shift angle is too small, see Fig. 4.5. A compromise has to be made while selecting the value for  $k_3$ .



**Fig. 4.6** Circulating current (per unit) through parallel inductor  $L_p$  versus  $k_3$



**Fig. 4.7** Circulating current (per unit) through capacitor  $C_p$  versus  $k_3$  for various  $k_2$



**Fig. 4.8** Current (per unit) through series branch versus  $k_3$  for various  $k_2$

### 4.5.3 Total Harmonic Distortion of the Output Voltage

Fig. 4.9 and Fig. 4.10 give the worst output voltage THD as function of  $k_1$  and  $k_2$ . We see that when  $k_2=1$  (i.e. the parallel branch is tuned), at  $\delta=120^\circ$ , the THD of the output voltage is zero. When  $k_2 \neq 1$  (i.e. the parallel branch is off tuned), this point shifts a little bit around  $\delta=120^\circ$ .

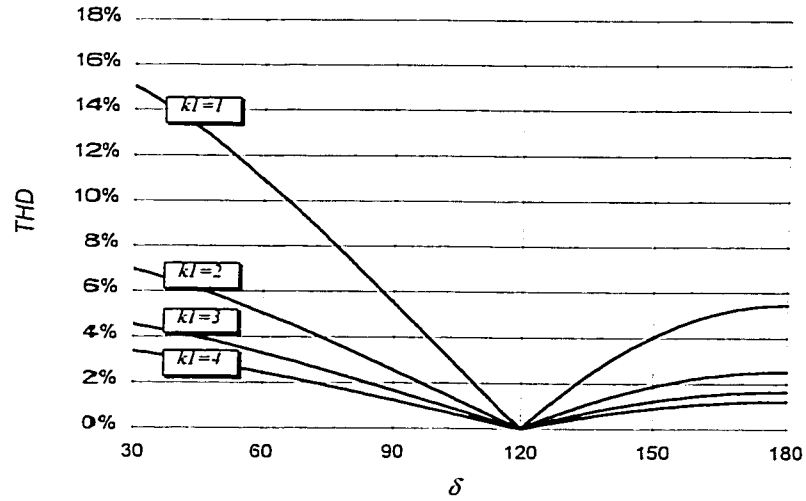


Fig. 4.9 THD as function of phase-shift angle  $\delta$  for various  $k_1$  (at  $k_2=1$ )

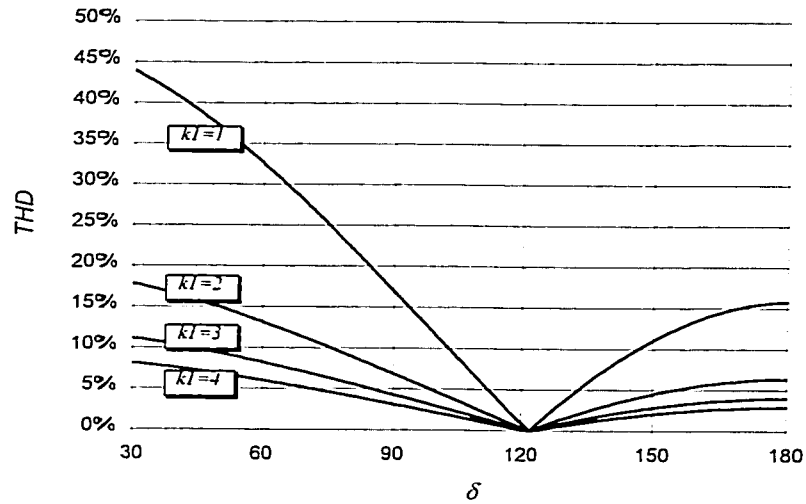


Fig. 4.10 THD as function of phase shift-angle  $\delta$  for various  $k_1$  (at  $k_2=2$ )

Eq.(4-36) has given the expression of the output THD, in which  $k_1/k_2$  as a whole has big influence on the value of THD. However, if  $k_2$  changes, but  $k_1/k_2$  remains the same, THD will be almost the same. Curve  $k_1=1$  ( $k_2=1$ ) in Fig. 4.9 and curve  $k_1=2$  ( $k_2=2$ ) in Fig. 4.10 is an example.

If we want to reduce the output THD, one way is to increase the value of the parallel capacitor  $C_p$ , because a larger capacitor can absorb more harmonics current. According to Eq.(4-36), we can get the same conclusion. When capacitor  $C_p$  increases,  $k_2$  decreases but  $k_1$  remains unchanged, therefore, the output THD is reduced, see Fig. 4.9 and Fig. 4.10.

We can also increase the impedance of the series branch components (i.e. increase the value of inductor  $L_s$  and decrease the value of capacitor  $C_s$ ) to reduce the output THD. It is because that larger series impedance can let more harmonics voltage drop on it. According to Eq.(4-36), when the series branch impedance is increased, then  $k_1$  increases but  $k_2$  remains the same, therefore the output THD is reduced.

We must be aware that changing the value of the parallel inductor  $L_p$  does not help much in reducing the output THD, because when inductor  $L_p$  changes,  $k_2$  changes, but  $k_1/k_2$  remains the same. Then, according to Eq.(4-36), the output THD will remain nearly the same.

#### ***4.5.4 The Effect of Transformer Location on Performance***

In section 4.4, the steady state analysis does not include the transformer. However, the location of the transformer will have some impact on the *Resonant Network* components. As we have discussed in Chapter 2 and Chapter 3, the transformer turn ratio of the proposed inverter is greater than 1. If the transformer is located after the Resonant Network, then the circulating current is large, hence more circulating losses. If the transformer is located after the *Resonant Network*, the voltage across the resonant

components is large. Table 4.1 and Table 4.2 give an example to show the effect of transformer location on the resonant current and voltage.

	$L_s$	$C_s$	$L_p$	$C_p$
Value	$6.875\mu H$	$0.3684\mu F$	$1.146\mu H$	$1.105\mu F$
Current (rms)	$22.44A$	$22.4A$	$41.65A$	$20.83A$
Voltage (rms)	$96.9V_{ac}$	$96.9V_{ac}$	$30V_{ac}$	$30V_{ac}$

**Table 4.1** Values and ratings for resonant components (transformer before the *Resonant Network* at  $N=4$ ,  $k_1=6$ ,  $k_2=4$ ,  $k_3=0.2$ ,  $I_{o, rated}=8.33A$ )

	$L_s$	$C_s$	$L_p$	$C_p$
Value	$110\mu H$	$23nF$	$18.33\mu H$	$69nF$
Current (rms)	$5.61A$	$5.61A$	$10.41A$	$5.2A$
Voltage (rms)	$387.5V_{ac}$	$387.5V_{ac}$	$120V_{ac}$	$120V_{ac}$

**Table 4.2** Values and ratings for resonant components (transformer after the *Resonant Network* at  $N=4$ ,  $k_1=6$ ,  $k_2=4$ ,  $k_3=0.2$ ,  $I_{o, rated}=8.33A$ )

The location of the transformer is determined by the specific application. If the output is low voltage but large current, the transformer should be placed after the *Resonant Network* to reduce the circulating current. If the output is high voltage but low current, the transformer is better to be placed after the *Resonant Network* to reduce the voltage stress across the resonant components.

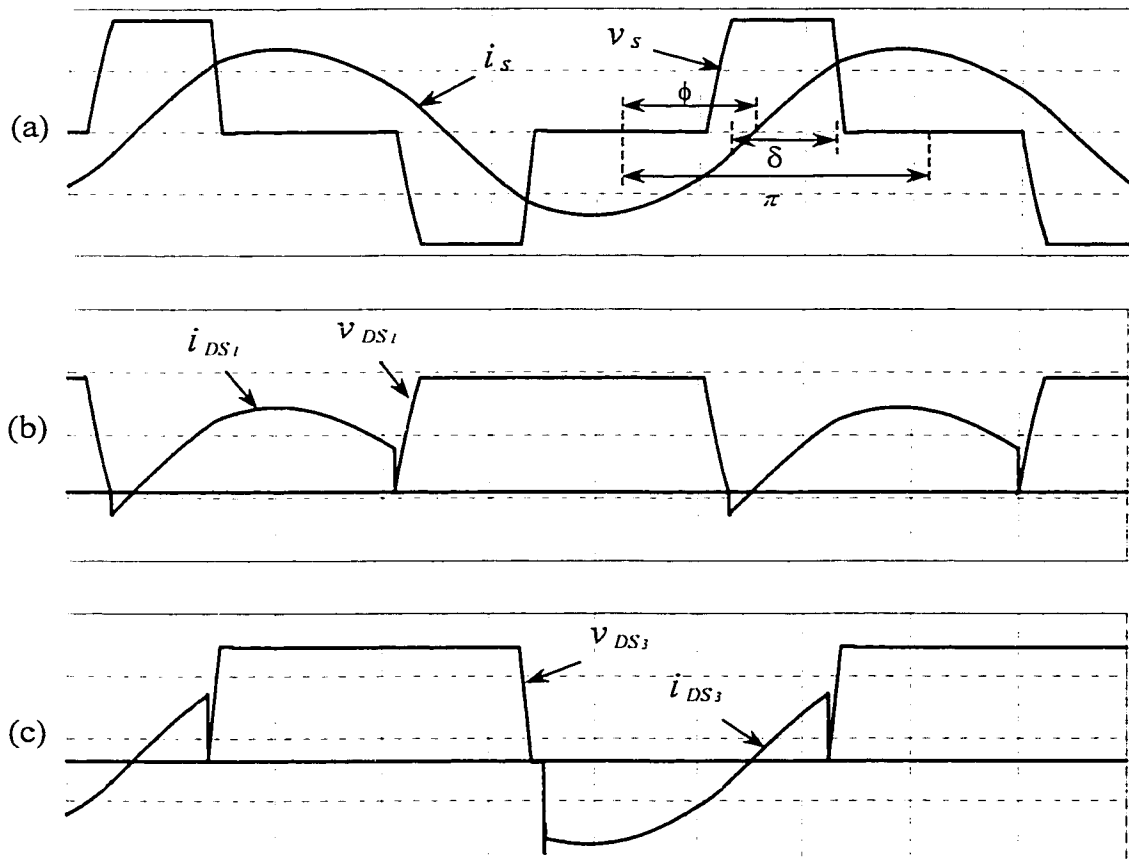


## 4.6 SIMULATION AND EXPERIMENTAL VERIFICATIONS

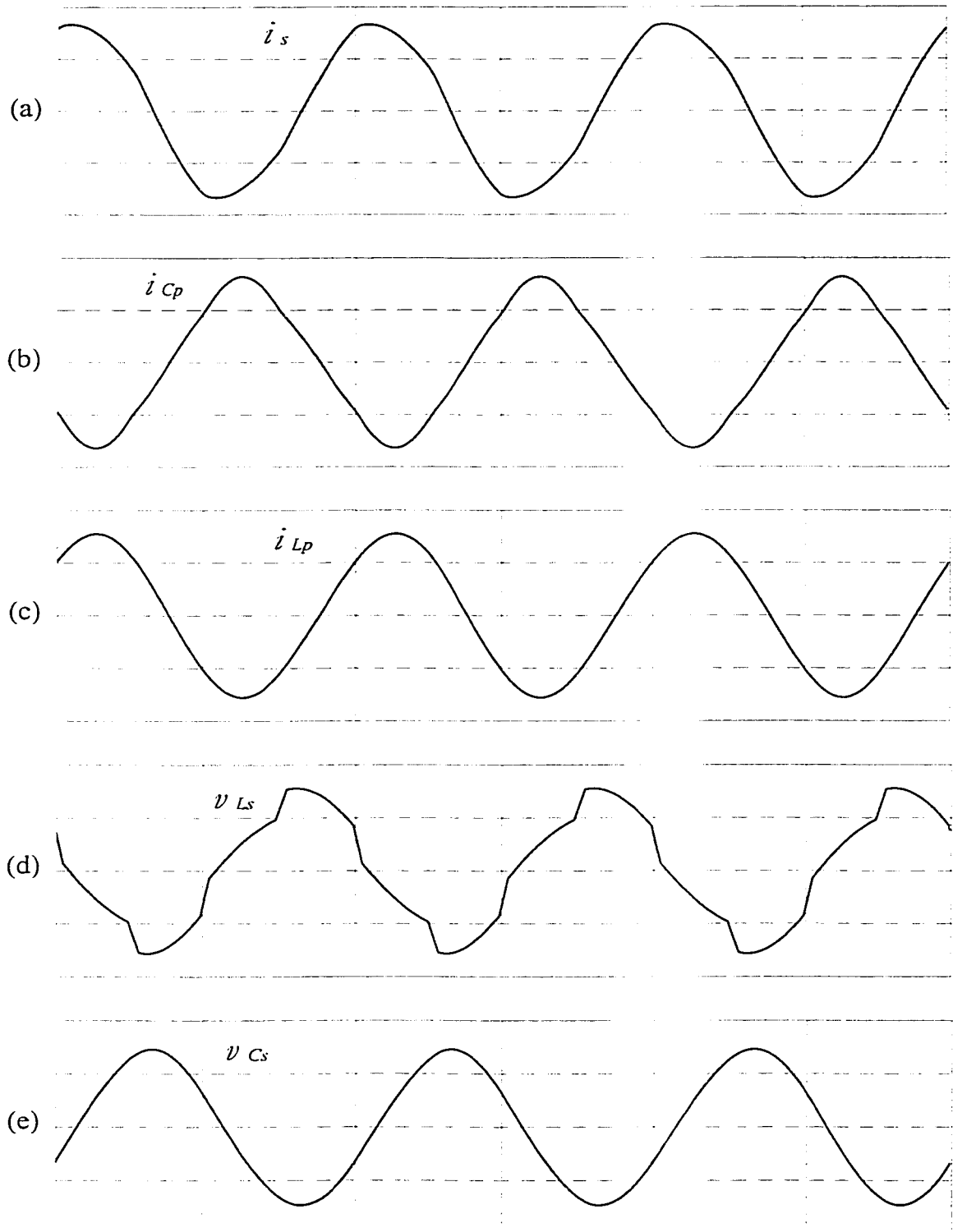
The simulation and experiment circuits are based on the design example given in Chapter 5, which has a  $30V_{ac}$ , 100kHz output voltage, 250W output.

### 4.6.1 Simulation Waveforms

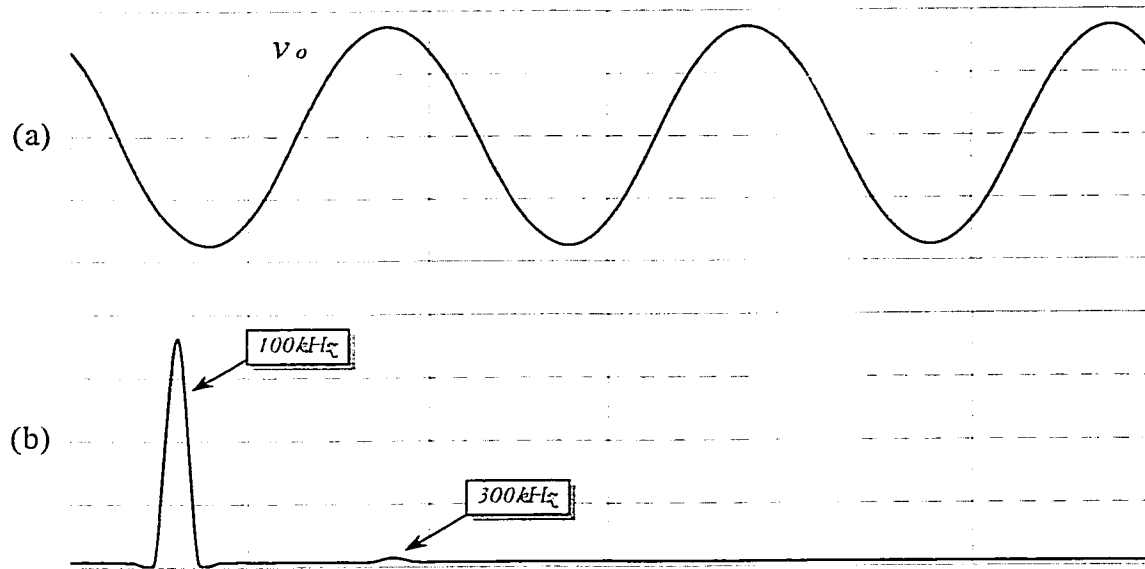
Fig. 4.11 to Fig. 4.13 gives the simulation waveforms, which are simulated at  $110V_{ac}$  input with  $30V_{ac}$  output voltage at 100kHz and 250W output power.



**Fig. 4.11** Simulation waveforms of the *Full Bridge Inverter*  
(a) Output voltage and current of the *Full Bridge Inverter*; (b) Drain to source voltage and current of switch  $S_1$ ; (c) Drain to source voltage and current of switch  $S_3$



**Fig. 4.12** Simulation waveforms of the *Resonant Network*  
 (a) Current through the series branch; (b) Current through the parallel capacitor; (c) Current through the parallel inductor; (d) Voltage across the series inductor; (e) Voltage across the series capacitor



**Fig. 4.13** Simulation waveform of the output voltage  
 (a) Waveform of the output voltage ( $30V_{ac}$  at 100kHz); (b) Frequency spectrum of the output voltage (THD=2%)

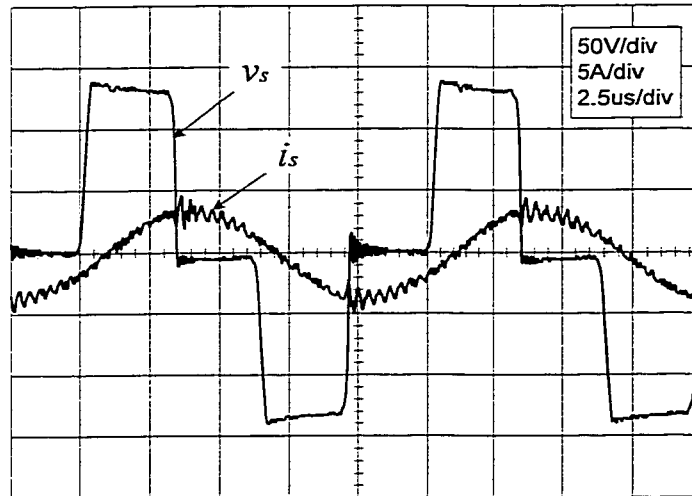
Fig. 4.11 gives the PSpice simulation waveforms of the *Full Bridge Inverter*, which shows that ZVS is achieved in the dc-ac stage. The voltage and current waveforms of switch  $S_1$  and  $S_3$  also verified the prediction given in Fig. 4.2.

Fig. 4.12 gives the current and voltage waveforms of the resonant components. Fig. 4.12 (a) shows that the current through the series branch is nearly sinusoidal, which verifies the prediction given in section 4.4, page 70.

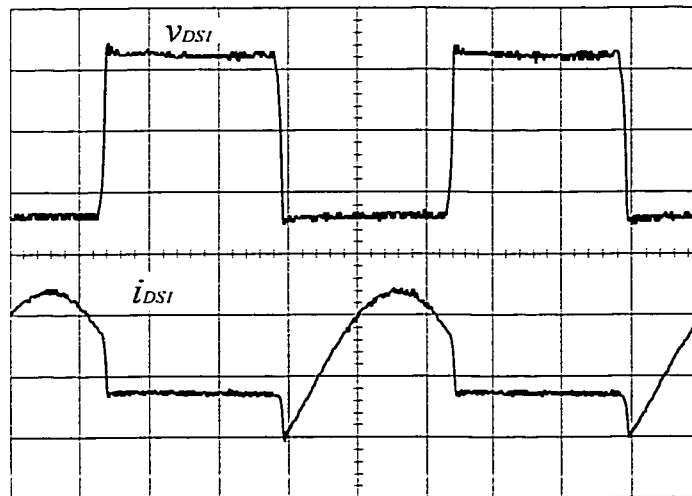
Fig. 4.13 gives the simulated output voltage and its frequency spectrum. The harmonics of the output voltage distribute at 300kHz, 500kHz, and so on. The Total Harmonic Distortion of the output voltage is as low as 2%.

## 4.6.2 Experimental Results

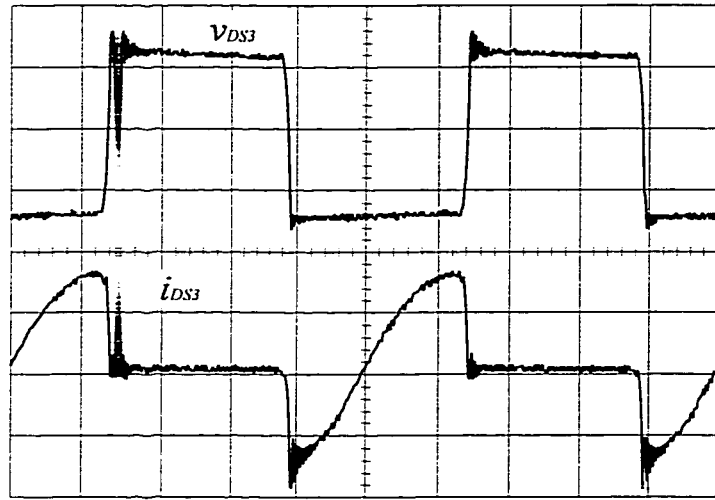
Fig. 4.14 to Fig. 4.18 give the experimental waveforms, which are measured at  $110V_{ac}$  input and  $250W$  output. Fig. 4.14, Fig. 4.15 and Fig. 4.16 verified the waveforms given in Fig. 4.2 and Fig. 4.11. They also show that zero voltage switching is achieved.



**Fig. 4.14** Experimental waveforms of the output voltage and current of the *Full Bridge Inverter* (at  $110V_{ac}$  line input,  $P_o=250W$ )

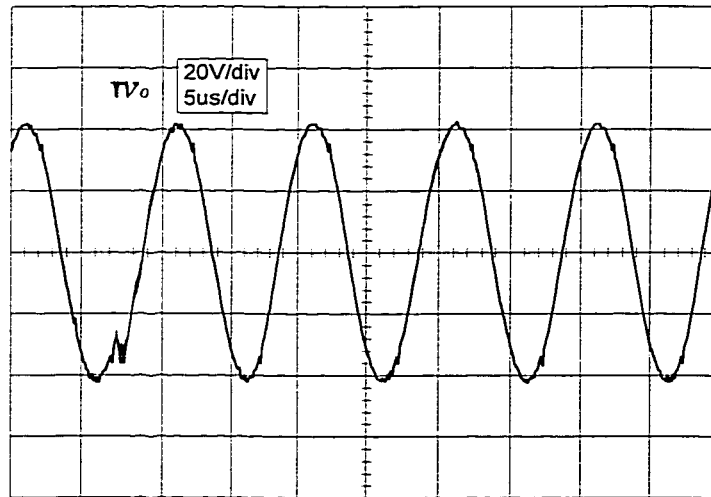


**Fig. 4.15** Experimental voltage and current waveforms switch 1

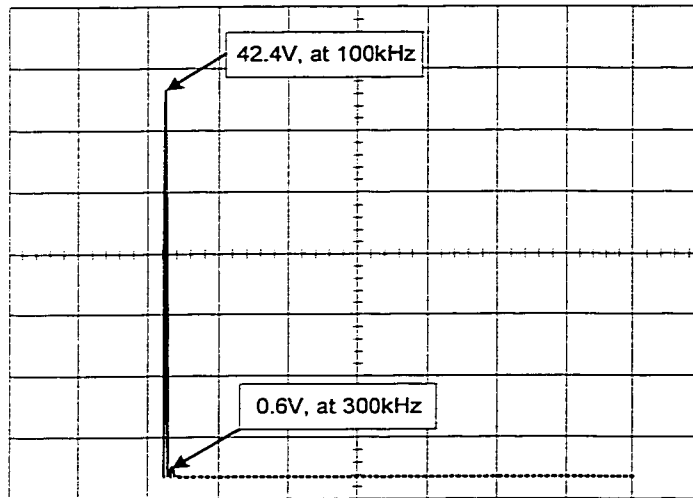


**Fig. 4.16** Experimental voltage and current waveforms switch 3

The waveform of the final output voltage is given Fig. 4.17. Its frequency spectrum is given in Fig. 4.18, from which its THD can be calculated out to be as low as 1.4%.



**Fig. 4.17** Experimental waveform of the output voltage (at 110V<sub>ac</sub> line input, P<sub>o</sub>=250W)



**Fig. 4.18** Measured harmonics of the output voltage, THD=1.4%  
(at 110V<sub>ac</sub> line input, P<sub>o</sub>=250W)

## CHAPTER 5

# DESIGN PROCEDURES AND EXAMPLES

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In this chapter, a boost implemented high frequency ac-ac converter will be given to show the design procedure of the ac-ac inverter. The buckboost implementation follows the same design procedure, and most of the parameters are the same. Therefore, the design procedure of the buckboost implementation will not be given. However, a design example of boost and buckboost will both be given in the end of this chapter.

### 5.1 DESIGN SPECIFICATIONS

It is required to design a 250W output, input current power factor corrected high frequency ac-ac inverter with the following specifications:

- Input Line Voltage:  $V_{in}=90-265V_{ac}$  at 60Hz
- Output Voltage:  $V_o=30V_{ac}$  at 100KHz
- Output Voltage Total Harmonic Distortion: THD<5%
- Input Current Power Factor: PF>0.86
- Input Current Harmonics: match the requirements of IEC-1000-3-2

## 5.2 DESIGN PROCEDURE

Boost implementation is presented to give the design procedure in this section. The design procedure of the buckboost implementation is similar to that of the boost implementation.

### 5.2.1 Determination of Gate Signal Constant $m$ and Inductor $L_{in}$

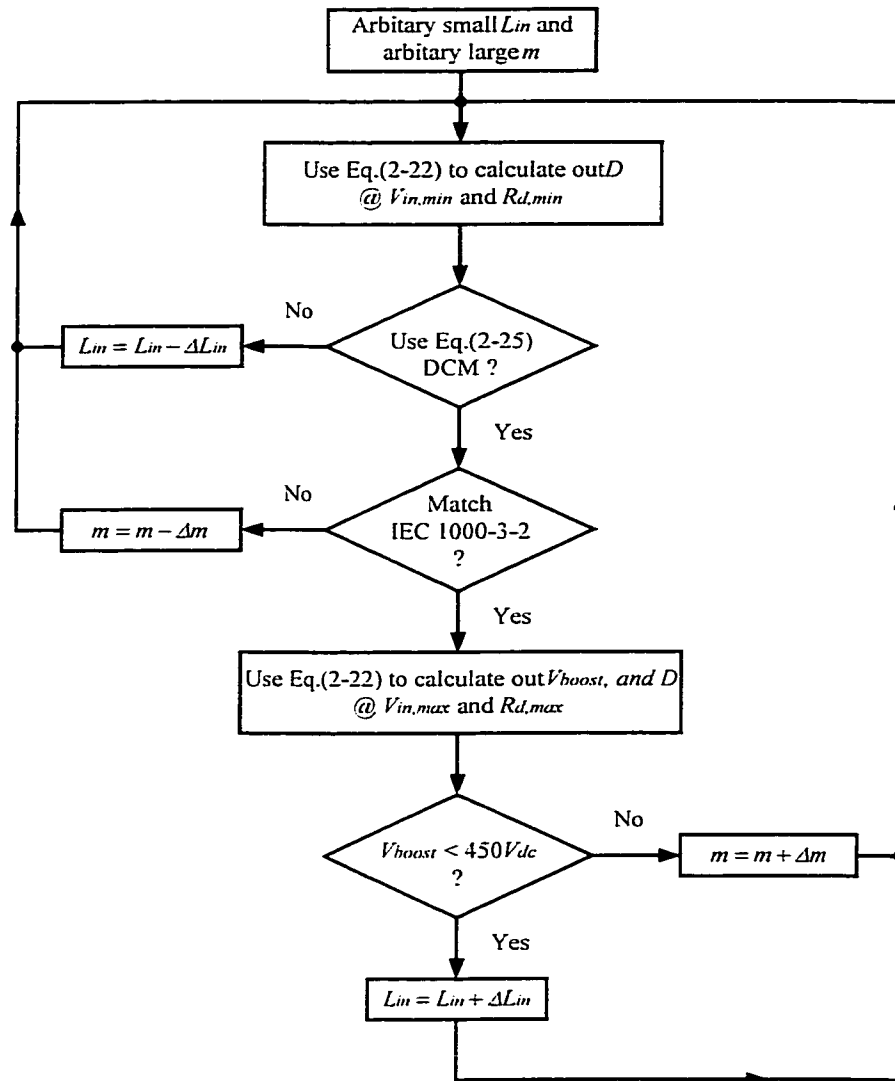
The goal of designing the PFC stage is to achieve a high power factor, low DC bus voltage, and low current stress. Power factor and current stress are related to the value of inductor  $L_{in}$ . The value of  $L_{in}$  should be designed to its maximum in such a way that at low line heavy load, the DCM operation of the PFC stage can be maintained and the current stress can be minimized. The DC bus voltage is mainly determined by the *Gate Signal Constant*  $m$ , which also affects power factor.  $m$  should be designed to its maximum so that at high line light load, the DC bus voltage is smaller than  $450V_{dc}$ , and the power factor is kept high in the mean time. The design procedures to find out the maximum  $L_{in}$  and maximum  $m$  are given in Fig. 5.1.

The range of  $L_{in}$  and  $m$  can also be very easily narrowed down from the performance characteristics given in section 2.5.3 and 2.5.4. In addition, with the help of computer simulation, the value of  $m$  and  $L_{in}$  can be optimized as below.

$$m = 8 \quad (5-1)$$

$$L_{in} = 25 \mu H \quad (5-2)$$





**Fig. 5.1** Design procedures to find out maximum  $L_{in}$  and  $m$

### 5.2.2 Determination of Key Constants $k_1$ , $k_2$ and $k_3$

Key constant  $k_1$ ,  $k_2$ , and  $k_3$  can be selected from the performance characteristics given in section 4.5.1, 4.5.2, and 4.5.3. And with the optimization of simulation tools, they are determined as below.

$$k_1 = 4.4 \quad (5-3)$$

$$k_2 = 1.5 \quad (5-4)$$

$$k_3 = 0.27 \quad (5-5)$$

### 5.2.3 Determination of Resonant Components:

After the three constant  $k_1$ ,  $k_2$  and  $k_3$  are determined, the values of the resonant components are given from Eq.(5-6) to Eq.(5-9):

$$L_s = \frac{k_1 k_2 N^2 R_d}{2\pi f_{sw}} \quad (5-6)$$

$$C_s = \frac{1}{2\pi f_{sw} k_1 k_2 N^2 R_d} \quad (5-7)$$

$$L_p = \frac{k_2 N^2 R_d}{2\pi f_{sw}} \quad (5-8)$$

$$C_p = \frac{1}{2\pi f_{sw} k_2 N^2 R_d} \quad (5-9)$$

### 5.2.4 Rating of Resonant Components:

The rms value of the current through the series branch is:

$$I_s = \frac{0.9 \sin(\delta/2) \cdot V_{dc}}{N^2 R_d} \cdot \sqrt{1 + (1/k_3)^2 \cdot (1/k_2 - 1)^2} = 5.6 A \quad (5-10)$$

The rms value the circulating current in the parallel inductor is:

$$I_{ip} = \frac{0.9 \sin(\delta / 2) \cdot V_{dc}}{2\pi f_{sw} L_p} = 10.3 A \quad (5-11)$$

The rms value of the circulating current through the parallel capacitor is:

$$I_{cp} = \frac{0.9 \sin(\delta / 2) \cdot V_{dc}}{2\pi f_{sw} k_2 L_p} = 10.3 A \quad (5-12)$$

### 5.2.5 Current Rating of switches:

RMS value of the switch current:

$$\begin{aligned} I_{RMS, S1} &= I_{RMS, S4} \\ &= \sqrt{\frac{1}{2\pi} \int_0^{\pi - \omega t_d} \left\{ \sqrt{2} I_s \sin \left[ \omega t - \phi + \frac{1}{2} (\pi - \delta) \right] \right\}^2 d\omega t} = 2.1 A \end{aligned} \quad (5-13)$$

$$\begin{aligned} I_{RMS, S2} &= I_{RMS, S3} \\ &= \sqrt{\frac{1}{2\pi} \int_0^{\pi - \omega t_d} \left\{ \sqrt{2} I_s \sin \left[ \omega t - \phi - \frac{1}{2} (\pi - \delta) + \omega t_d \right] \right\}^2 d\omega t} = 2.5 A \end{aligned} \quad (5-14)$$

### 5.2.6 Determination of boost diode and switch

The maximum peak current through the boost diode and switch can be calculated out through (2-6):

$$I_{Lin, p} = \frac{\sqrt{2} V_{in}}{L_{in}} \cdot \frac{D_{boost}}{f_{boost}} = 20 A \quad (5-15)$$

### 5.2.7 Determination of boost inductor

The maximum peak current through the boost inductor is given in (5-15). The rms current through the boost inductor  $I_{in}$  is:

$$I_{L_{in}, rms} = \frac{P_{in, max}}{I_{in, min}} = 3A \quad (5-16)$$

### 5.2.8 Implementation of Control Circuits

The implementation of the control circuits is very simple.  $V_{G1}$ ,  $V_{G2}$ ,  $V_{G3}$ , and  $V_{G4}$  can be generated by a phase-shift controller such as UC3875N.  $V_{G0}$  can be generated by the logic circuits given in Fig. 5.2, in which 74121 is monostable multivibrator, and  $V_{G1}$ ,  $V_{G3}$  are from the output of the phase-shift controller.

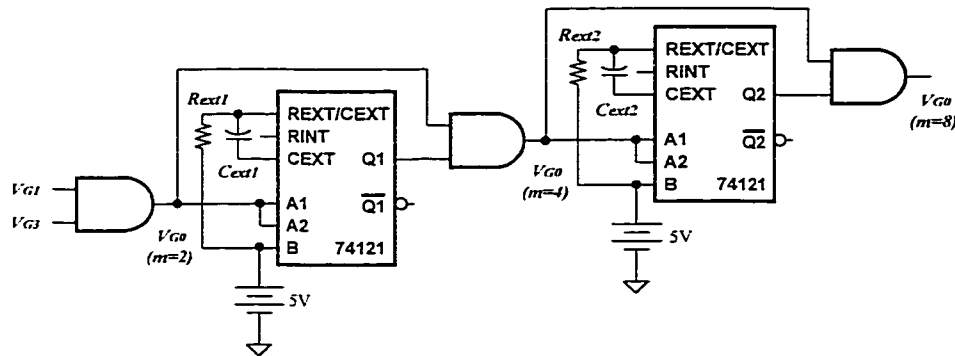


Fig. 5.2 Logic circuits that generate  $V_{G0}$  for different  $m$

## 5.3 DESIGN EXAMPLES

Table 5.1 lists the components used in the boost implemented high frequency ac-ac inverter. Table 5.2 gives the component list of buckboost implementation.

<b>Component and Parameter</b>	<b>Value and Device</b>
$L_s$ (series inductor)	110uH, Philips Ferrite Core: CP-PQ32/30
$C_s$ (series capacitor)	22nF/800Vdc, Sprague polypropylene film capacitor
$L_p$ (parallel inductor)	25uH, Philips Ferrite Core: CP-PQ32/30
$C_p$ (parallel capacitor)	68nF/600Vdc, Sprague polypropylene film capacitor
$T_r$ (main transformer)	4:1, TDK Ferrite Core: PC40EI30-Z
$L_{in}$ (boost inductor)	25uH, Philips Ferrite Core: CP-PQ26/20
$C_{dc}$ (bulk capacitor)	3x330uF/450Vdc, United Chemicon SMH aluminum electrolytic capacitor
$S_0, S_1, S_2, S_3, S_4$ (switches)	500V/20A, International Rectifier: IRFP460
$D_0$	600V/8A, Motorola ultrafast rectifier: MUR1660CT
$C_{s1}, C_{s2}, C_{s3}, C_{s4}$ (snubber capacitors)	1nF/600Vdc, Sprague polypropylene film capacitor

**Table 5.1** LISTS OF COMPONENTS (BOOST IMPLEMENTATION)

<b>Component and Parameter</b>	<b>Value and Device</b>
$L_{in}$ (buckboost inductor)	25uH, Philips Ferrite Core: CP-PQ26/20
$D_0$ (buckboost diode)	600V/8A, Motorola ultrafast rectifier: MUR1660CT

**Table 5.2** LISTS OF COMPONENTS FOR BUCKBOOST IMPLEMENTATION

## CHAPTER 6

# CONCLUSIONS

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### 6.1 SUMMARY

This thesis provides a solution to low power high frequency ac-ac inverter for computer and telecommunication distribution system. Boost and buckboost implemented power factor correction topologies are presented. Analysis and comparison of these two approaches are given.

Experimental results show that the proposed inverter has a high input power factor, which complies with IEC-1000-3-2 standards. The DC bus voltages of the two approaches are well limited for the universal line voltage. The implementation of the control circuits is simple. The output voltage is load independent with very low THD (<2%). The overall efficiency can be above 85% if properly designed.

The boost implementation is very attractive for 90-135V<sub>ac</sub> input, 150-250W output applications. The buckboost implementation is very attractive for 90-265Vac input, 100-150W applications. The overall efficiency of the boost implementation is higher than that of the buckboost implementation. However, the buckboost implementation has lower DC bus voltage and a higher input power factor.

## **6.2 CONTRIBUTIONS**

The major contributions of this thesis are:

- (1) Proposed a topology for low power high frequency ac-ac inverter for high frequency telecommunication and computer distribution system.
- (2) High input power factor, low output THD, limited DC bus voltage, high efficiency and low cost are achieved.
- (3) Two approaches are presented and compared, which is
- (4) Theoretical analysis and design procedures are given.
- (5) A laboratory prototype is built and experimental results verified the theoretical analysis and computer simulation.

## **6.3 SUGGESTIONS FOR FUTURE WORK**

- (6) Optimization of components and layout design using PCB.
- (7) A control methodology for fast transient response.
- (8) Stadbility study of the inverter system with the high frequency distribution loads [30].

## REFERENCE

- [1] Praveen K. Jain, and Humberto Pinheiro, "Hybrid high frequency ac power distribution architecture for telecommunication systems," in *IEEE Transactions on Aerospace and Electronics Systems*, Vol. 35, No. 1, January 1999, pp. 138-147.
- [2] NASA, "Status of 20kHz space station power distribution technology," *Publication TM 100781, NASA*.
- [3] Drobnik, J. "High frequency alternating power distribution for telecommunication systems," in *Proceedings of INTELEC 1994*, pp. 174-182.
- [4] J. Drobnik, L. Huang, P. Jain, and R. Steigerwald, "PC platform power distribution system: past application, today's challenge and future direction," in *IEEE International Telecomm. Energy Conf. (INTELEC) Proc.*, paper no. 2-1, June, 1999.
- [5] Laszlo Huber, and Milan M. Jovanovic, "Evaluation of ac VRM topologies for high-frequency power distribution systems," in *IEEE Applied Power Electron. Conf.*, 2001, pp. 160-166.
- [6] International Standard IEC 1000-3-2, *Electromagnetic Compatibility (EMC), part 3, First Edition, 1995*.
- [7] Matteo Daniele, Praveen K. Jain, and Géza Joós, "A single-stage power-factor-corrected ac/dc converter," in *IEEE Transactions on Power Electronics*, Vol. 14, No. 6, November 1999, pp. 1046-1055.
- [8] Praveen K. Jain, José R. Espinoza, and Nasser A. Ismail, "A single-stage zero-voltage zero-current-switched full-bridge DC power supply with extended load power range,"



- in *IEEE Transactions on Industrial Electronics*, Vol. 46, No.2, April 1999, pp. 261-270.
- [9] Mei Qiu, Gerry Moschopoulos, Humberto Pinheiro, and Praveen K. Jain, "Analysis and design of a single stage power factor corrected full-bridge converter," in *IEEE APEC '99, Rec.*, pp. 119-125.
- [10] Qun Zhao, and Fred C. Lee, "Design optimization of an off-line input harmonic current corrected flyback converter," in *IEEE PESC '99, Rec.*, pp. 91-97.
- [11] R. Redl, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage," in *IEEE PESC '94, Rec.*, pp. 1137-1144.
- [12] Ned Mohan, Tore M. Undeland, and William P. Robbins, "Power Electronics: Converters, Applications, and Design", Second Edition, *John Wiley & Sons, Inc. 1995*.
- [13] John C. Fluke, "Controlling Conducted Emissions by Design", *Van Nostrand Reinhold, 1991*.
- [14] Robert L. Steigerwald, "A comparison of half-bridge resonant converter topologies," in *IEEE Transactions on Power Electronics*, April 1988, pp. 174-182.
- [15] Liu, R., and Lee, C. Q. "Series resonant converter with third-order commutation network," in *IEEE Transactions on Industrial Electronics*, May 1984, pp. 181-191.
- [16] Tsai, F.S., Materu, P., and Lee, F. C. "Constant frequency clamped mode resonant converters," in *IEEE Transactions on Power Electronics*, September/October 1988, pp. 460-473.

- [17] Bhat, A. "Analysis and design of a fixed frequency LCL-type series resonant converter," in *IEEE Proceeding of Applied Power Electronics Conference, February 1992*, pp. 253-260.
- [18] Praveen K. Jain, M. Tanju, "A 20KHz hybrid resonant power source for the space station," in *IEEE Transaction on Aerospace and Electronic Systems, Vol. 25, No.4, July 1989*, pp. 491-496.
- [19] Jindong Zhang, Milan M. Jovanovic, and Fred C. Lee, "Comparison between CCM single-stage and two-stage boost PFC converters," in *IEEE APEC'99, Rec.*, pp. 335-341.
- [20] Wennan Guo, and Praveen K. Jain, "An ac-ac inverter with build-in power factor correction, soft-switching and a unified controller," in *IEEE Applied Power Electronics Conference, 2001*, pp.153-159.
- [21] A. R. Prasad, P. D. Ziogas, and S. Manias, "An active power factor correction technique for three phase diode rectifiers," in *IEEE PESC'89, Rec.*, pp. 58-66.
- [22] Wennan Guo, and Praveen K. Jain, "A power factor corrected ac-ac inverter topology using a unified controller for high frequency power distribution architecture," in *IEEE Power Electronics Specialists Conference, 2001* (in press).
- [23] Wennan Guo, and Praveen K. Jain, "Comparison between boost and buckboost implemented PFC inverter with build-in soft switching and a unified controller," in *IEEE Power Electronics Specialists Conference, 2001* (in press).

- [24] Praveen K. Jain, D. Bannard, and M. Cardella, "A phase-shift modulated double tuned resonant DC/DC converter: analysis and experimental results," in *IEEE Transaction on Aerospace and Electronic Systems*, Vol. 25, No.4, July 1989, pp. 491-496.
- [25] Bill Andreycak, "Phase shifted, zero voltage transition design considerations and the UC3875 PWM controller," in *Unitrode Application Note*, May 1997.
- [26] Praveen K. Jain, Harry Soin, and Martin Cardella, "Constant frequency resonant DC/DC converters with zero switching losses," in *IEEE Transaction on Aerospace and Electronic Systems*, Vol. 30, No.2, April 1994, pp. 534-543.
- [27] Ned Mohan, "Tutorial 1: Cycle-by-Cycle Average (CCA) Modeling of Switch-Mode Power Electronics Converters in PSpice," 1999.
- [28] Ned Mohan, "Tutorial 2: Designing Feedback Controllers in Switch Mode DC Power Supplies by PSpice: Explained by Two Examples of Voltage-Mode and Current-Mode Control," 1999.
- [29] Ned Mohan, "Tutorial 3: Designing Feedback Controller in Power-Factor-Correction (PFC) Circuits Using PSpice: Explained by an Example," 1999.
- [30] Steve Burns, "Distributed Power, what causes these systems to oscillate?" in *PCIM* May 1999, pp. 14-22.

# APPENDIX

## A1. OUTPUT VOLTAGE OF RESONANT NETWORK

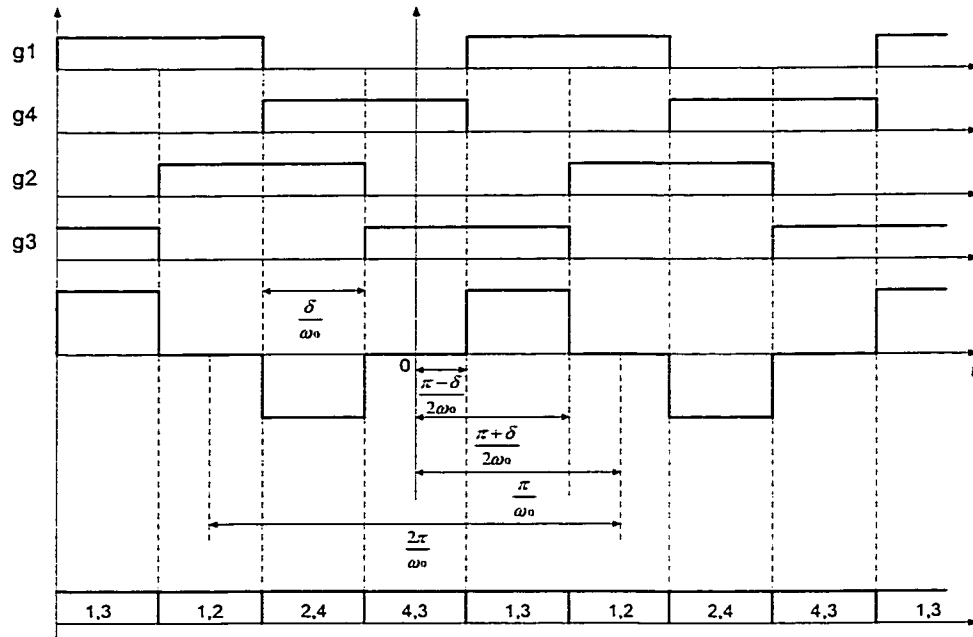


Fig A.1 Gate Signal and Transformer Primary Voltage

$$f(t) = \begin{cases} 0 & 0 < t < \frac{\pi - \delta}{2\omega_0} \\ V_{dc} & \frac{\pi - \delta}{2\omega_0} < t < \frac{\pi + \delta}{2\omega_0} \\ 0 & \frac{\pi + \delta}{2\omega_0} < t < \frac{\pi}{\omega_0} \end{cases} \quad (\text{A-1})$$

$$b_n = \frac{l}{2} \int_0^t f(t) \sin\left(\frac{n\pi t}{l}\right) dt \quad (\text{A-2})$$

$$b_n = \frac{2\omega_0}{\pi} \int_{\omega_0}^{\pi} f(t) \sin\left(\frac{n\pi t}{\pi / \omega_0}\right) dt \quad (\text{A-3})$$

$$b_n = \frac{2\omega_0}{\pi} \int_{\frac{\pi-\delta}{2\omega_0}}^{\frac{\pi+\delta}{2\omega_0}} \sin(n\omega_0 t) dt \quad (\text{A-4})$$

$$b_n = \frac{4}{n\pi} \cdot \sin \frac{n\pi}{2} \cdot \sin \frac{n\delta}{2} \quad (\text{A-5})$$

$$V_{o,1} = b_n|_{n=1} \cdot V_{dc} = \frac{4}{\pi} \cdot \sin \frac{\pi}{2} \cdot \sin \frac{\delta}{2} \cdot V_{dc} = 0.9 \sin \frac{\delta}{2} \cdot V_{dc} \quad (\text{A-6})$$

## A2. TRANSFORMER DESIGN

$$P_{in} := 300$$

$$f := 100 \cdot 10^3$$

$$k_p := 0.5$$

$k_p$ : Primary area factor

$$k_u := 0.78 \cdot 0.8 \cdot (1 - 0.35)$$

$k_u$ : Winding packing factor

$$k_t := 1.0$$

$k_t$ : RMS current factor

$$k := k_p \cdot k_u \cdot k_t$$

$k$ : Overall copper utilization factor.

$$B := 100 \cdot 10^{-3}$$

$B$ : Peak flux density, half of the flux density swing, T

$$AP := \left( \frac{10 \cdot P_{in}}{k \cdot 2 \cdot B \cdot f} \right)^{1.143}$$

$AP$ : Area product ( $= A_e \cdot A_{cw}$ ),  $\text{cm}^4$

$$AP = 0.708$$

(Theoretical calculated product area,  $\text{cm}^4$ )

According to the theoretical calculated product area, choose TDK ferrit core: PC40E130-Z. Hence get the following parameters:

$$A_e := 111$$

$A_e$ : Effective core area,  $\text{mm}^2$

$$A_{cw} := 75.6$$

$A_{cw}$ : Cross-sectional winding area of core,  $\text{mm}^2$

$$V_e := 6440$$

$V_e$ : Effective core volume

The new Area Product is larger than the calculated one:

$$AP := A_e \cdot A_{cw} \cdot 10^{-4} \quad AP = 0.839$$

Corresponding to the core size, choose bobbin: BE-30-1110CP, and Accessory item: FE-30-F. Hence get the following parameters:

$$l_w := 61$$

$l_w$ : Average length of turns around bobbin, mm

$$A_w := 44.5$$

$A_w$ : Cross-sectional winding area of bobbin,  $\text{mm}^2$

## Calculate transformer turn number:

$$V_p := 120$$

$V_p$ : primary winding voltage, rms value

$$n := 4$$

$n$ : transformer turn ratio

$$N_p := \text{floor}\left(\frac{10^6 \cdot V_p}{4.44 f \cdot B \cdot A_e}\right)$$

$\text{floor}(x)$ : return the smaller integer

$$N_s := \text{ceil}\left(\frac{N_p}{n}\right)$$

$\text{ceil}(x)$ : return the bigger integer

$$N_p = 24 \quad N_s = 6$$

## Choose wire size:

$$k_u := 0.78 \cdot 0.8$$

Modify the winding packing factor, because of using the bobbin winding area instead of the core winding area.

$$A_{pri} := k_p \cdot k_u \cdot A_w$$

$A_{pri}$ : Effective Primary area,  $\text{mm}^2$

$$A_{wp} := \frac{A_{pri}}{N_p}$$

$A_{wp}$ : Primary wire area,  $\text{mm}^2$

$$A_{wp} = 0.579$$

Choose AWG #20 (AWG area:  $0.5264 \text{mm}^2$ )

$$A_{wp} := 0.5264$$

$$A_{sec} := A_{pri}$$

$$A_{ws} := \frac{A_{sec}}{N_s}$$

$A_{ws}$ : Secondary wire area,  $\text{mm}^2$

$$A_{ws} = 2.314$$

Choose AWG #14 (AWG area:  $2.0959$ )

$$A_{ws} := 2.0959$$

## Calculate copper losses:

$$\rho := 1.558$$

$\rho$ : Resistivity of copper at 0 degree,  $\mu\Omega/\text{cm}$

$$R_t := 0.004$$

$R_t$ : Temperature coefficient of copper at 0 degree

$$T := 50$$

T: Working temperature

$$\rho_{tc} := \rho \cdot (1 + R_t \cdot T)$$

$\rho_{tc}$ : Resistivity of copper at T degree,  $\mu\Omega/\text{cm}$

$$I_s := 8.333$$

$I_s$ : Secondary rms current

$$I_p := \frac{I_s}{\left(\frac{N_p}{N_s}\right)}$$

$I_p$ : Primary rms current

$$R_1 := \rho_{tc} \cdot \frac{l_w \cdot N_p}{A_{wp} \cdot 0.8} \cdot 10^{-5}$$

Only 0.8 of the wire area is copper

$$P_{\text{copper1}} := I_p^2 \cdot R_1$$

$$P_{\text{copper1}} = 0.282$$

$$R_2 := \rho_{tc} \cdot \frac{l_w \cdot N_s}{A_{ws} \cdot 0.8} \cdot 10^{-5}$$

$$P_{\text{copper2}} := I_s^2 \cdot R_2$$

$$P_{\text{copper2}} = 0.283$$

$$P_{\text{copper}} := P_{\text{copper1}} + P_{\text{copper2}}$$

$P_{\text{copper}}$ : Copper losses of the core, W

$$P_{\text{copper}} = 0.565$$



## A3. RESONANT INDUCTOR DESIGN

### Resonant Inductor Design

#### Estimation for Area Product:

$$L := 110 \cdot 10^{-6}$$

L: Inductor value

$$I_{rms} := 5.6$$

I<sub>rms</sub>: rms current through the series resonant inductor, A

$$I_p := \sqrt{2} \cdot I_{rms}$$

I<sub>p</sub>: Peak current through the series resonant inductor, A

$$k_u := 0.78 \cdot 0.8 \cdot (1 - 0.35)$$

k<sub>u</sub>: Winding packing factor

$$B := 140 \cdot 10^{-3}$$

B: Peak flux density, half of the flux density swing, T

$$AP := \left( \frac{L \cdot I_p \cdot I_{rms} \cdot 10^4}{450 \cdot B \cdot k_u} \right)^{1.143}$$

AP: Area product (=A<sub>e</sub>·A<sub>cw</sub>), cm<sup>4</sup>

$$AP = 2.094$$

(Theoretical calculated product area, cm<sup>4</sup>)

According to the theoretical calculated product area, choose TDK ferrit core: PC40PQ32/30G-12. Hence get the following parameters:

$$A_e := 161$$

A<sub>e</sub>: Effective core area, mm<sup>2</sup>

$$A_{cw} := 149.6$$

A<sub>cw</sub>: Cross-sectional winding area of core, mm<sup>2</sup>

$$V_e := 11970$$

V<sub>e</sub>: Effective core volume

The new Area Product is larger than the calculated one:

$$AP := A_e \cdot A_{cw} \cdot 10^{-4} \quad AP = 2.409$$

Corresponding to the core size, choose bobbin: BPQ32/30-1112CP, and Accessory item: FPQ32/30-A. Hence get the following parameters:

$$l_w := 67.1$$

l<sub>w</sub>: Average length of turns around bobbin, mm

$$A_w := 95.3$$

A<sub>w</sub>: Cross-sectional winding area of bobbin, mm<sup>2</sup>

### Calculate inductor turn number:

$$\mu_r := 1$$

$\mu_r$ : Relative permeability of core

$$\mu_0 := 4 \cdot \pi \cdot 10^{-7}$$

$\mu_0$ : Magnetic field constant (H/m)

$$N := \text{floor}\left(\frac{L \cdot I_p}{B \cdot A_e \cdot 10^{-6}}\right)$$

floor(x): return the smaller integer

$$N = 38$$

ceil(x): return the bigger integer

$$l_g := \frac{\mu_r \cdot \mu_0 \cdot N^2 \cdot A_e \cdot 10^{-6}}{L} \cdot 10^3$$

$l_g$ : Total length of air gap, mm

$$l_g = 2.656$$

### Choose wire size:

$$k_u := 0.78 \cdot 0.8$$

Modify the winding packing factor, because of using the bobbin winding area instead of the core winding area.

$$A_{ew} := k_u \cdot A_w$$

$A_{pri}$ : Effective winding area, mm<sup>2</sup>

$$A_{wa} := \frac{A_{ew}}{N}$$

$A_{wa}$ : Wire area, mm<sup>2</sup>

$$A_{wa} = 1.565$$

Choose AWG #16 (AWG area: 1.3224mm<sup>2</sup>)

$$A_{wa} := 1.3224$$

### Calculate copper losses:

$$\rho := 1.558$$

$\rho$ : Resistivity of copper at 0 degree,  $\mu\Omega/\text{cm}$

$$R_t := 0.004$$

$R_t$ : Temperature coefficient of copper at 0 degree

$$T := 50$$

T: Working temperature

$$\rho_{tc} := \rho \cdot (1 + R_t \cdot T)$$

$\rho_{tc}$ : Resistivity of copper at T degree,  $\mu\Omega/\text{cm}$

$$R_l := \rho_{tc} \cdot \frac{l_w \cdot N}{A_{wa} \cdot 0.8} \cdot 10^{-5}$$

Only 0.8 of the wire area is copper

$$P_{\text{copper}} := I_{\text{rms}}^2 \cdot R_l$$

$P_{\text{copper}}$ : copper losses, W

$$P_{\text{copper}} = 1.413$$

### Calculate core losses:

From the **Core Loss Curve** given by TDK, at  $f_s=100\text{kHz}$ ,  $B=140\text{mT}$ , the core loss per  $\text{m}^3$  for PC40 material is  $130\text{kw}/\text{m}^3$ , therefore the core loss is:

$$P_{\text{core}} := 130 \cdot 10^3 \cdot V_e \cdot 10^{-9}$$

$P_{\text{core}}$ : Core losses of the core, W

$$P_{\text{core}} = 1.556$$

### Total losses and total temperature rise:

$$P_{\text{total}} := P_{\text{copper}} + P_{\text{core}}$$

$$P_{\text{total}} = 2.969$$

From the **Temperature Rise vs. Total Loss Curve** given by TDK, at  $P_{\text{total}}=2.969\text{W}$ , get the temperature rise of the core is 50 degree.

## Parallel Inductor Design

### Estimation for Area Product:

$$L := 18 \cdot 10^{-6}$$

L: Inductor value

$$I_{rms} := 10.4$$

I<sub>rms</sub>: rms current through the series resonant inductor, A

$$I_p := \sqrt{2} \cdot I_{rms}$$

I<sub>p</sub>: Peak current through the series resonant inductor, A

$$k_u := 0.78 \cdot 0.8 \cdot (1 - 0.35)$$

k<sub>u</sub>: Winding packing factor

$$B := 120 \cdot 10^{-3}$$

B: Peak flux density, half of the flux density swing, T

$$AP := \left( \frac{L \cdot I_p \cdot I_{rms} \cdot 10^4}{450 \cdot B \cdot k_u} \right)^{1.43}$$

AP: Area product (=A<sub>e</sub>·A<sub>cw</sub>), cm<sup>4</sup>

$$AP = 1.299$$

(Theoretical calculated product area, cm<sup>4</sup>)

According to the theoretical calculated product area, choose TDK ferrit core: PC40PQ32/20G-12. Hence get the following parameters:

$$A_e := 170$$

A<sub>e</sub>: Effective core area, mm<sup>2</sup>

$$A_{cw} := 80.8$$

A<sub>cw</sub>: Cross-sectional winding area of core, mm<sup>2</sup>

$$V_e := 9420$$

V<sub>e</sub>: Effective core volume

The new Area Product is larger than the calculated one:

$$AP := A_e \cdot A_{cw} \cdot 10^{-4} \quad AP = 1.374$$

Corresponding to the core size, choose bobbin: BPQ32/20-1112CP, and Accessory item: FPQ32/20-A. Hence get the following parameters:

$$l_w := 67.1$$

l<sub>w</sub>: Average length of turns around bobbin, mm

$$A_w := 42.9$$

A<sub>w</sub>: Cross-sectional winding area of bobbin, mm<sup>2</sup>

### Calculate inductor turn number:

$$\mu_r := 1$$

$\mu_r$ : Relative permeability of core

$$\mu_0 := 4 \cdot \pi \cdot 10^{-7}$$

$\mu_0$ : Magnetic field constant (H/m)

$$N := \text{floor}\left(\frac{L \cdot I_p}{B \cdot A_e \cdot 10^{-6}}\right)$$

floor(x): return the smaller integer

$$N = 12$$

ceil(x): return the bigger integer

$$l_g := \frac{\mu_r \cdot \mu_0 \cdot N^2 \cdot A_e \cdot 10^{-6}}{L} \cdot 10^3$$

$l_g$ : Total length of air gap, mm

$$l_g = 1.709$$

### Choose wire size:

$$k_u := 0.78 \cdot 0.8$$

Modify the winding packing factor, because of using the bobbin winding area instead of the core winding area.

$$A_{ew} := k_u \cdot A_w$$

$A_{pri}$ : Effective winding area, mm<sup>2</sup>

$$A_{wa} := \frac{A_{ew}}{N}$$

$A_{wa}$ : Wire area, mm<sup>2</sup>

$$A_{wa} = 2.231$$

Choose AWG #14 (AWG area: 2.0959mm<sup>2</sup>)

$$A_{wa} := 2.0959$$

### Calculate copper losses:

$$\rho := 1.558$$

$\rho$ : Resistivity of copper at 0 degree,  $\mu\Omega/\text{cm}$

$$R_t := 0.004$$

$R_t$ : Temperature coefficient of copper at 0 degree

$$T := 50$$

T: Working temperature

$$\rho_{tc} := \rho \cdot (1 + R_t \cdot T)$$

$\rho_{tc}$ : Resistivity of copper at T degree,  $\mu\Omega/\text{cm}$

$$R_l := \rho_{tc} \cdot \frac{l_w \cdot N}{A_{wa} \cdot 0.8} \cdot 10^{-5}$$

Only 0.8 of the wire area is copper

$$P_{copper} := I_{rms}^2 \cdot R_l$$

$P_{copper}$ : copper losses, W

$$P_{copper} = 0.971$$

### Calculate core losses:

From the **Core Loss Curve** given by TDK, at  $f_s=100\text{kHz}$ ,  $B=120\text{mT}$ , the core loss per  $\text{m}^3$  for PC40 material is  $110\text{kw}/\text{m}^3$ , therefore the core loss is:

$$P_{core} := 110 \cdot 10^3 \cdot V_e \cdot 10^{-9}$$

$P_{core}$ : Core losses of the core, W

$$P_{core} = 1.036$$

### Total losses and total temperature rise:

$$P_{total} := P_{copper} + P_{core}$$

$$P_{total} = 2.007$$

From the **Temperature Rise vs. Total Loss Curve** given by TDK, at  $P_{total}=2.007\text{W}$ , get the temperature rise of the core is 40 degree.

## A4. BOOST AND BUCKBOOST INDUCTOR DESIGN

### Calculate copper losses:

$$\rho := 1.558$$

$\rho$ : Resistivity of copper at 0 degree,  $\mu\Omega/\text{cm}$

$$R_t := 0.004$$

$R_t$ : Temperature coefficient of copper at 0 degree

$$T := 50$$

$T$ : Working temperature

$$\rho_{tc} := \rho \cdot (1 + R_t \cdot T)$$

$\rho_{tc}$ : Resistivity of copper at  $T$  degree,  $\mu\Omega/\text{cm}$

$$R_l := \rho_{tc} \cdot \frac{l_w \cdot N}{A_{wa} \cdot 0.8} \cdot 10^{-5}$$

Only 0.8 of the wire area is copper

$$P_{\text{copper}} := I_{\text{rms}}^2 \cdot R_l$$

$P_{\text{copper}}$ : copper losses, W

$$P_{\text{copper}} = 0.971$$

### Calculate core losses :

From the **Core Loss Curve** given by TDK, at  $f_s=100\text{kHz}$ ,  $B=120\text{mT}$ , the core loss per  $\text{m}^3$  for PC40 material is  $110\text{kw}/\text{m}^3$ , therefore the core loss is:

$$P_{\text{core}} := 110 \cdot 10^3 \cdot V_e \cdot 10^{-9}$$

$P_{\text{core}}$ : Core losses of the core, W

$$P_{\text{core}} = 1.036$$

### Total losses and total temperature rise:

$$P_{\text{total}} := P_{\text{copper}} + P_{\text{core}}$$

$$P_{\text{total}} = 2.007$$

From the **Temperature Rise vs. Total Loss Curve** given by TDK, at  $P_{\text{total}}=2.007\text{W}$ , get the temperature rise of the core is 40 degree.

### Calculate inductor turn number:

$$\mu_r := 1$$

$\mu_r$ : Relative permeability of core

$$\mu_0 := 4 \cdot \pi \cdot 10^{-7}$$

$\mu_0$ : Magnetic field constant (H/m)

$$N := \text{floor}\left(\frac{L \cdot I_p}{B \cdot A_e \cdot 10^{-6}}\right)$$

floor(x): return the smaller integer

$$N = 16$$

ceil(x): return the bigger integer

$$l_g := \frac{\mu_r \cdot \mu_0 \cdot N^2 \cdot A_e \cdot 10^{-6}}{L} \cdot 10^3$$

$l_g$ : Total length of air gap, mm

$$l_g = 1.531$$

### Choose wire size:

$$k_u := 0.78 \text{--} 0.8$$

Modify the winding packing factor, because of using the bobbin winding area instead of the core winding area.

$$A_{ew} := k_u \cdot A_w$$

$A_{pri}$ : Effective winding area, mm<sup>2</sup>

$$A_{wa} := \frac{A_{ew}}{N}$$

$A_{wa}$ : Wire area, mm<sup>2</sup>

$$A_{wa} = 1.197$$

Choose AWG #18 (AWG area: 0.8343mm<sup>2</sup>)

$$A_{wa} := 0.8343$$



### Calculate copper losses:

$$\rho := 1.558$$

$\rho$ : Resistivity of copper at 0 degree,  $\mu\Omega/\text{cm}$

$$R_t := 0.004$$

$R_t$ : Temperature coefficient of copper at 0 degree

$$T := 50$$

T: Working temperature

$$\rho_{tc} := \rho \cdot (1 + R_t \cdot T)$$

$\rho_{tc}$ : Resistivity of copper at T degree,  $\mu\Omega/\text{cm}$

$$R_l := \rho_{tc} \cdot \frac{l_w \cdot N}{A_{wa} \cdot 0.8} \cdot 10^{-5}$$

Only 0.8 of the wire area is copper

$$P_{copper} := I_{rms}^2 \cdot R_l$$

$P_{copper}$ : copper losses, W

$$P_{copper} = 0.227$$

### Calculate core losses:

From the **Core Loss Curve** given by TDK, at  $f_s=100\text{kHz}$ ,  $B=125\text{mT}$  (The reason  $B=125\text{mT}$  instead of  $B=250\text{mT}$  is because the curve is drawn for 2 quadrants topologies, for 1 quadrant topologies, the peak flux density should be divided by 2 to enter the curve to find the core losses), the core loss per  $\text{m}^3$  for PC40 material is  $100\text{kw}/\text{m}^3$ , therefore the core loss is:

$$P_{core} := 100 \cdot 10^3 \cdot V_e \cdot 10^{-9}$$

$P_{core}$ : Core losses of the core, W

$$P_{core} = 0.549$$

### Total losses and total temperature rise:

$$P_{total} := P_{copper} + P_{core}$$

$$P_{total} = 0.776$$

From the **Temperature Rise vs. Total Loss Curve** given by TDK, at  $P_{total}=832\text{W}$ , get the temperature rise of the core is 30 degree.