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CAPACITOR COMMUTATED CONVERTERS FOR HVDC TRANSMISSION SYSTEM

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A Thesis

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Abstract

CAPACITOR COMMUTATED CONVERTERS FOR HVDC TRANSMISSION SYSTEM

Anup Mazumder

The operation of HVDC systems using conventional Line Commutated Converters (LCCs) operating with weak AC systems becomes unreliable due to frequent commutation failures which can occur for any small disturbance in the AC networks. These commutation failures may eventually initiate other disturbances such as voltage or frequency instability in the AC networks.

Furthermore, each LCC station consumes huge amounts of reactive power (between 55-60% of the rated DC power) which is supplemented by large capacitor banks and the filters. This increases the converter station cost and may result in operational problems such as the development of low frequency resonance with the AC network.

Chances of commutation failure can be greatly reduced by using Capacitor Commutated Converters (CCCs). The commutation capacitor (CC) increases the commutation margin. Furthermore, with the recent developments in filter design, it is now possible to design a narrow bandpass filter (High Q) using far less capacitance. Hence, use of such filters can reduce the problem of low frequency resonance and provide better reactive power management. In this thesis, the performance of an HVDC system based on CCCs interact-

ing with weak AC networks is evaluated in terms of its dynamic/transient behaviour.

The thesis starts with a brief survey of the present state of the art in HVDC systems. This is followed by the descriptions of different subsystems of the CIGRE benchmark model. The basic control characteristics of HVDC systems are discussed and their implementations are described using block diagrams. Finally, different tests are carried out by applying varying faults and step changes in the control parameters.

PSCAD/EMTDC simulation package is used to model the CIGRE benchmark and its various control circuits.

The performance of the CCC is compared with conventional LCC using the same benchmark model. Finally, a modified version of CCC configuration, namely Hybrid Converter Combination (HCC) configuration is presented. This configuration uses a combination of both a traditional LCC and a CCC. Its viability is assessed in terms of technical suitability and lower overall cost.

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Dedicated to :

my mother, Smt. Nirmala Mazumder

my father, (Late) Sukumar Mazumder and

my brother, (Late) Swarup Mazumder

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List of Abbreviations

AC	- Alternating Current
DC	- Direct Current
HVAC	- High Voltage AC
HVDC	- High Voltage DC
SC	- Short Circuit
SCR	- Short Circuit Ratio
CC	- Commutation Capacitor
CCC	- Capacitor Commutated Converter
CSCC	- Controlled Series Capacitor Converter
TCSC	- Thyristor Controlled Series Capacitor
PSCAD	- Power System Computer Aided Design
EMTDC	- Electromagnetic Transient DC
IGBT	- Insulated Gate Bi-polar Transistor
VSC	- Voltage Source Converter
CO	- Current Order
CIGRE	- The Conseil International des Grands Reseaux Electriques
EMTP	- Electromagnetic Transient Programme
VDCL	- Voltage Dependent Current Limiter
CEA	- Constant Extinction Angle
LCC	- Line Commutated Converter
HCC-UP	- Hybrid Converter Combination with CC in the upper bridge
HCC-LO	- Hybrid Converter Combination with CC in the lower bridge
VCO	- Voltage Controlled Oscillator
PI	- Proportional and Integral
AO	- Alpha Order
AOr	- Alpha Order rectifier
AOi	- Alpha Order inverter
GO	- Gamma Order
SLG	- Single Line to Ground
VV	- Valve Voltage
CM	- Current Margin

Chapter -1

Introduction

1.1 Background to HVDC Systems

Since most power generating stations have been developed at remote sites from load centres, the need for bulk power transfer over long distance arises. It is practical and economical to transmit power at high voltage levels to minimize transmission line losses. Out of two available means of power transmission, such as HVAC and HVDC, the latter is advantageous for the following reasons:

1. The cost per unit length of transmission is cheaper for HVDC than for AC transmission,
2. A DC transmission tower has less visual profile (and lower environmental impact) than an equivalent AC transmission,
3. The break even distance for submarine cable transmission is much less than that of overhead transmission. AC power transmission through cable becomes impractical for distances more than 50 km but transmission of power by DC cable is feasible even for a distance of 600 km,
4. DC Link enables power transfer between two asynchronous systems,
5. Power control through a DC link is faster.

Conventional two terminal HVDC systems have been using line commutated converters at both ends. These converters rely on the AC network line voltage for commutation. Hence performance of the conventional converters are greatly affected by the AC network strength. Network strength of the AC system is measured by Short Circuit Ratio (SCR) which is defined as

$$SCR = (SC\ Level\ of\ the\ AC\ Bus) / (DC\ Power)$$

A system is said to be weak if SCR is less than 3. A weak system is more sensitive to voltage fluctuations which causes problems in the HVDC transmission system, and special control methods may be needed to partially alleviate this problem.

In developing countries the demand for electricity is growing at a high rate due to industrial development. As a net effect, load centres keep growing larger. Power utilities are left with the choice of either adding capacity locally or importing power to load centres from remote sources. Capacity addition often implies a large investment and it may be coupled with environmental impacts. This increasing gap between supply and demand often results in making the existing power systems weaker with increasing demand. Consequently, it is now being envisaged that HVDC systems need to interact with AC networks with a SCR as low as 1.8.

Importing power to such a weak AC network using conventional converters is not a very reliable proposition because conventional converters suffer from frequent commutation failures. During commutation failure, power through the DC link becomes zero. This momentary interruption of power may have repercussions on AC networks at both ends. It

may cause voltage and frequency instability which may lead to a total shut down for a longer period of time. Also, frequent commutation failures can cause permanent damage to the valves.

Recent studies have focussed on the improvement of the commutation process by using series capacitors in the commutation circuit. This can reduce the chances of a commutation failure occurring.

1.2 Problem Definition

HVDC systems have been using conventional converters which depend on the AC network voltage for commutation. The voltage condition of the network is a function of the network strength which is expressed by its short circuit ratio (SCR). Increasingly, due to growing gap between supply and demand, HVDC systems need to interact with AC networks having a very low value of SCR. As a result, line commutated converters experience more frequent commutation failures in new installations. Also, an HVDC system with a long DC cable link may face the same problem even when it interacts with a strong AC system. Besides, a conventional converter consumes reactive power of the order of 55-60% of the rated DC power. Large filters and capacitor banks used for the purpose of compensation increase the cost of the converter station and may result in operational problems such as the development of low frequency resonance with the AC network.

The concept of using a capacitor for commutation purposes was developed back in the 1950's, but no initiative towards its implementation was taken because of one or more of the following reasons.

- The AC systems were usually quite strong, i.e. SCR was not low
- Problems of resolving economically the extra voltage stresses across the converter valves did not exist
- Difficulty in management of reactive power. In the case of a CCC, total reactive power requirement being low (approximately 15% of the rated DC power), it is necessary to have filters only for the purposes of harmonic elimination and not for reactive power supply. The very nominal reactive power variation is manageable by switching a small capacitor bank. However, due to manufacturing constraints it was not possible to utilize filters with low values of capacitance at high Q-values. Such filters would easily go out of tune resulting in poor filtering. But recent developments in filter design have resulted in techniques for easily tuning high-Q filters using low values of capacitance [4]. Such filters can now be designed primarily for harmonic filtering.

1.3 Literature Survey on Capacitor Commutated Converters

1.3.1 A Technical Assessment of Artificial Commutation of HVDC Converters with Series Capacitors [2]

The authors in [2] have discussed the principle of artificial commutation and how the operational range, in terms of firing angle, can be extended beyond normally attainable range. They have modeled a three phase full wave bridge configuration with series capacitors added in the commutation circuit. They have established the mathematical relationship(s) among commutation voltage, direct current, overlap angle, firing angle and voltage across the capacitor and provided the iterative solution using comprehensive computer programs. In converter operation, valves undergo varying stresses throughout the cycle.

The authors in [2] have presented the instantaneous value of the valve voltage for eight different periods over a complete cycle. Finally, they have presented a detailed comparison between natural and artificial commutation considering selected system ratings of V_{LL} = 100 kV, I_{dc} = 1000 amps, X_L = 11.1 ohms and f = 50 Hz and concluded that:

- For a given system, the range of permitted firing angles is determined by the values of the capacitor C and the direct current,
- Operating range can be increased by a reduction in the value of the capacitance at the expense of increase peak valve voltage,
- For a given set of conditions, the overlap angle reduces below that for natural commutation with high, but not proportionally higher, rate of change of current at the end of commutation, and
- Commutation failure is less likely to occur because of the tendency for the commutation margin to be increased for a decrease in AC system voltage or increase in direct current.

1.3.2 Capacitor Commutated Converters for HVDC [4]

In [4], the authors have discussed the concept of Capacitor Commutated Converter (CCC) and how the introduction of the commutation capacitor (CC) can improve the performance of a conventional HVDC system by reducing the chances of commutation failure and reactive power consumption/demand of the converter stations.

Because of the additional commutation voltage, the operating range of the rectifier delay angle and the inverter extinction angle is increased. Consequently, the operation of

the rectifier and the inverter can be achieved with smaller values of alpha and gamma respectively. The reactive power consumptions of both the converter stations are therefore reduced. Studies show that in case of the HVDC system with conventional converters, the reactive power requirement varies with the load. Therefore, the switching of shunt capacitor bank is necessary as the load varies. But in the case of an HVDC system with CCC, the reactive power requirement is limited to a very low (about 0.14 p.u.) value. The need for switching of the shunt capacitor bank can thereby be reduced or eliminated. Also, with extended operating range of alpha/gamma, the system has more flexibility of sharing the reactive power by the converter stations though the total reactive power remains same for any particular load.

Simulation results show that with constant load current and firing angle, commutation margin increases with decrease in AC bus voltage and vice versa. The authors in [4] have concluded that successful commutation is possible even when the AC bus voltage is close to zero. Transient analysis shows that CCC can successfully commutate with reduced AC bus voltage. Also, because of the presence of the commutation capacitor, peak fault current and its duration is less. Load rejection overvoltage performance of the CCC option is better than that of the conventional option. As the commutation voltage is current dependent, any sudden change in direct current may cause a momentary imbalance in the commutation voltage which may make a valve reach its critical commutation margin. The authors in [4] have discussed a control strategy to prevent this momentary voltage imbalance.

Even though CCC has higher power transfer capacity, it has certain drawbacks. The

voltage stress of the valves and the insulation level of the converter transformer are higher. Also, because of smaller overlap angle the level of harmonic currents is higher.

Finally the authors in [4] have conducted cost analysis taking care of all practical aspects e.g. higher voltage stress on valve and higher insulation level of the transformer winding and the reduced size of the transformer and filter, and have concluded that HVDC transmission with CCC is economical as compared to the conventional option which consists of line commutated converters (LCC) only.

1.3.3 Capacitor Commutated Converter Circuit Configurations for DC Transmission [5]

The authors in [5] have identified commutation failure as the major problem of the conventional HVDC system specially while interacting with weak AC networks or strong AC networks with long DC cable link. They have described two different configurations of converters, namely, Capacitor Commutated Converter (CCC) and the Controlled Series Capacitor Converter (CSCC). In CCC, the commutating capacitor is placed between the transformer and the valves, whereas in the case of CSCC it is placed between the AC network and the converter transformer. A comparative simulation study has been carried out using PSCAD/EMTDC.

Since CCC and CSCC have improved performance with respect to Maximum Available Power (MAP), therefore stability limit as compared to the conventional configuration is improved. The Stability limit is increased to 1.44 p.u. and 1.34 p.u. for CCC and CSCC, respectively The valve voltage stress is also increased. Both the configurations require

reduced reactive power, and hence the size of the shunt capacitor is reduced. Results show that reactive power requirement is only 15% of the rated power as compared to 55-60% in the case of the conventional option which consists of LCC only. Also, the magnitude of the harmonic currents is more for these two configurations because of reduced commutation overlap.

Transient analysis shows that both CCC and CSCC exhibit smooth recovery against the application of typical AC bus faults. Also, both can easily ride through disturbances such as a remote AC fault without any commutation failure.

The authors in [5] have overcome the ferroresonance problem which is encountered for a certain fixed value of the commutation capacitor. They have over come this problem by using Thyristor Controlled Series Capacitor (TCSC). Simulation result shows that ferroresonance problem has been fully eliminated when capacitor control is used.

Finally, it is concluded that both CCC and CSCC have improved immunity from commutation failure, lower load rejection and increased stability margin as compared to the conventional option. Hence, these two options can be considered suitable for use at the inverter end in a long DC cable system.

1.3.4 Impact of Capacitor Commutated Converters in AC Systems with multiple DC Infeed [6]

In [6], the authors have investigated the possibility of the degradation of the overall performance of HVDC systems consisting of several cable links (multiple infeed) between strong and weak AC networks at the rectifier and inverter end respectively.

They have considered the Norwegian Power Grid which has many pre-existing conventional DC links. With another one or two links in the planning stage, they have carried out studies to find out a suitable option such as conventional or CCC for the new links. In the simulation, all existing links are lumped and represented by a DC link with conventional converters at both ends. Similarly, all the new links are lumped and represented by a DC link with conventional converters at sending end and CCC at the receiving end. Three cases are studied:

i) The existing link alone

ii) The planned link alone

iii) The combined system i.e. both existing link and the planned link together.

Special controls are used to prevent total collapse of the inverter DC voltage and for successful recovery of the system.

Various disturbances (i.e. three phase remote fault, step change in current order, load change and load rejection) are applied to the systems. Compiling all the results, they have concluded that in such a multi infeed system involving long submarine DC cables the over all performance would be better if any one of the links is chosen to have a CCC inverter.

1.3.5 Application of Capacitor Commutated Converters in multi-infeed HVDC schemes [7]

In [7], the authors have investigated the suitability of various inverter options in a multi- infeed HVDC system. The Norwegian Power Grid [6] is considered for the study. They have modeled the whole system with two HVDC links having conventional convert-

ers at the rectifier end interacting with two separate strong AC networks. At the inverter side, a common and weak AC network is considered. One of these two link, having a total capacity of 1600 MW, represents all existing links where as the other, having a total capacity of 1200 MW, represents all the links in the planning stage. Similar controls to [6] are adopted. Three distinct cases are studied:

- Case -I (Conventional) - Both 1600 MW and 1200 MW links have conventional inverters,
- Case -II (Mixed) - The 1600 MW link has conventional inverters and the 1200 MW link has CCC inverters, and
- Case -III (CCC) - Both 1600 MW and 1200 MW links have CCC inverters.

Transient studies such as load rejection overvoltage, remote AC fault, fault at the AC bus of the inverter and step change to direct current order are carried out. Considering all the results, the authors have concluded that all options provide a level of performance that falls within generally acceptable limits but conventional alternative has in general the better performance.

They finally concluded that if load rejection overvoltage are not of critical importance then the conventional alternative has in general the better performance.

1.3.6 An AC Active Filter for use at Capacitor Commutated HVDC Converters [8]

In [8], the authors have discussed the usefulness of an active filter for elimination of low order harmonics (11th and 13th) from the AC side of the HVDC system using a CCC.

In case of CCC or CSCC, filters are needed mainly for harmonic elimination and provide only a very small amount of reactive power support. Such filters with very low MVAR rating are more susceptible to de-tuning. In some cases, continuously tuned inductors are used to cope with this problem. The authors have described how the re-tuning of filters can be effectively realized by using an active filter developed by using a PWM technique.

The voltage of each phase is taken as a reference to the respective FFT block which determines the magnitude and phase of the targeted harmonics (here 11th and 13th) separately. The output of the FFT block is fed to a control system which re-calculates the real and imaginary parts of each harmonic voltage. A PI controller is used to control each part separately. At the output of the control system a combined waveform is obtained which is used as a voltage order for the PWM inverter. The output of the Voltage Source Converter (VSC) is applied to a transformer whose secondary injects the counter current into the converter bus to eliminate the low order characteristic harmonics.

Finally, taking an active filter into consideration, they have modeled a 1200 MW, 600 km long cable HVDC system having conventional rectifiers at one end and CCC inverters at the other end interacting with strong and weak AC system at the rectifier and inverter ends respectively. In the transient study, a three phase fault was applied at the inverter bus. The response of the DC bus voltage shows a smooth recovery. Also the controller is tested by using a 50% step in Current Order (CO) and the result shows that harmonic current is also reduced with the DC current order and the system responds quite well to the step change.

The authors in [8] have concluded that an active filter is a very attractive alternative to

passive/continuous tuned filter for CCC HVDC system application.

1.3.7 Evaluation of Classical, CCC and TCSC Converter Schemes for Long Cable Projects [9]

In [9], the authors have compared the features and simulated dynamic performance of series compensated and conventional HVDC converters with respect to long cable transmissions. Two series compensated converter technologies namely CCC and TCSC are included. In the CCC, the commutating capacitor is placed between the converter transformer and the valves whereas in the TCSC it is located between the AC network and the converter transformer. The conventional converters on the other hand, are connected directly to the converter transformers.

They pointed out that conventional technology is well established and can be best used between relatively strong AC networks where the need for AC filtering is moderate and reactive power balance is not a critical factor. Also, in classic HVDC converters, the basic problems involved were higher reactive power demand, higher sensitivity to inverter side AC network disturbances specially when a DC cable link is used.

The authors in [9] have carried out simulation studies with data of a planned project to transmit 2100 MW via an under-sea cable over a distance of 670 km. Comparison shows that the series compensated designs such as CCC and TCSC, improve the performance of HVDC transmissions connecting weak AC networks in terms of increased power flow and improved stability of the AC network, reduced load rejection over-voltages and consumed smaller amount of reactive power. Reduced reactive power means savings in capacitor

banks and breakers, and also the maintenance of the AC yard equipment is reduced.

With the above new converter designs, the HVDC technology for feeding weak networks is improved, and the choice among the three converter designs could be based on the type of AC network that will be fed by the HVDC transmission. Each design has its own advantages, but the properties of each design point to somewhat different applications.

Finally the authors in [9] concluded that

- The classic design is the cost effective solution for connecting relatively strong AC networks, where the demands of AC filtering are moderate and where there are only moderate demands on reactive power balance.
- The CCC design is a cost efficient solution for connecting weak AC networks, since a high power transfer can be combined with a high stability margin in the inverter network. The stability does not have to rely on additional equipment, such as synchronous condensers or additional series compensation.
- The TCSC design, in connection with an HVDC converter, is suitable for the same range of applications as those with the CCC, with performance compatible with the CCC design, but with reduced cost efficiency.

1.3.8 Predictive Firing Angle Calculation for Constant Effective Margin Angle Control of CCC - HVDC [10]

In [10], the authors proposed a predictive firing angle calculation method for Capacitor Commutated Converter (CCC). They have formulated the relations among various param-

eters for the commutation and post commutation periods. Because of the presence of the CCC, the relationship among α, μ, γ, V_{ac} and I_{dc} are complex and an iterative method is used for the solution. Also, the convergence of the solution depends on the initial values of α and μ and they have found out various combination of α and μ for which convergence is possible.

Three cases are investigated for three different sizes of the commutation capacitor. They have incorporated this predictive angle calculation algorithm to the controller and tested the system by applying steps in direct current and AC bus voltage.

1.4 Thesis Objectives

The objectives of this thesis are:

- To evaluate the performance of an HVDC system based on Capacitor Commutated Converters (CCC) in terms of its steady state and dynamic/transient behaviour, and
- To modify the CCC configuration and evaluate this modified version namely a Hybrid Converter Combination (HCC), using both traditional line commutated converter and a capacitor commutated converter to access its viability in terms of technical suitability and lower cost.

1.5 Methodology

An HVDC system based on the CIGRE HVDC benchmark is chosen for study [13]. The system consists of subsystems e.g. AC networks, converters, filters, converter trans-

formers and a DC link. The whole system is modeled by using the PSCAD/EMTDC simulation package [23]. Also, control and protection circuits are developed. This benchmark is used to study the performance of a system with Capacitor Commutated Converters (CCC). Using the capacitor commutated converter for one bridge and line commutated converter for the other bridge, a new configuration namely HCC, is developed and some modifications are proposed to achieve independent control of converters. The same benchmark model is used to study the performance of conventional and proposed hybrid configurations. Finally, a comparative study of the dynamic and steady state performances of these three systems is made.

1.6 Thesis Outline

In chapter 2, background information to HVDC systems is presented. Each subsystem of the HVDC system is described briefly. Also, overall control and protection strategies are discussed.

In chapter 3, different converter configurations are presented, the effect of the capacitor in the commutation circuit and the control implementations are discussed

In chapter 4, behaviour of the HVDC system under transient conditions is discussed. Different fault conditions are applied. Also, controllers are tested by applying steps in current order/gamma order. Finally results are presented and analyzed.

In chapter 5, conclusions from this study and recommendations for further work are provided.

1.7 Thesis Contributions

The dynamic performance of a modified converter configuration namely Hybrid Converter Combination (HCC) is studied and compared with two other configurations namely LCC and CCC. Study reveals that:

- HCC option can be considered as a special case of CCC where one of the capacitor banks is out of service due to some contigency. The ability to operate the station with this contingency is an improvement in the security of the power supply.

Chapter 2

HVDC System and Control Strategy

2.1 Introduction

The main objective of this thesis is to evaluate the performance of an HVDC system using different converter configurations. Hence, an HVDC system model is required for this purpose. A benchmark model for the study of HVDC systems has been developed by CIGRE [13] (The Conseil International des Grands Reseaux Electriques), an international association based in France. Both manufacturers and users from all over the world have been using this benchmark model for testing and evaluating the performance of controllers for HVDC systems.

In this chapter, we consider the CIGRE benchmark-based HVDC system operating with weak AC networks and its control strategy.

2.2 CIGRE Benchmark-Based HVDC System

Figure 2.1 represents an HVDC system based on the CIGRE benchmark [13]. The values (e.g. ratings etc.) proposed are fictitious and do not represent any particular scheme. The system has been particularly selected to have an operationally difficult configuration. The original CIGRE benchmark is a 12-pulse bipolar system but in this study, a 12-pulse

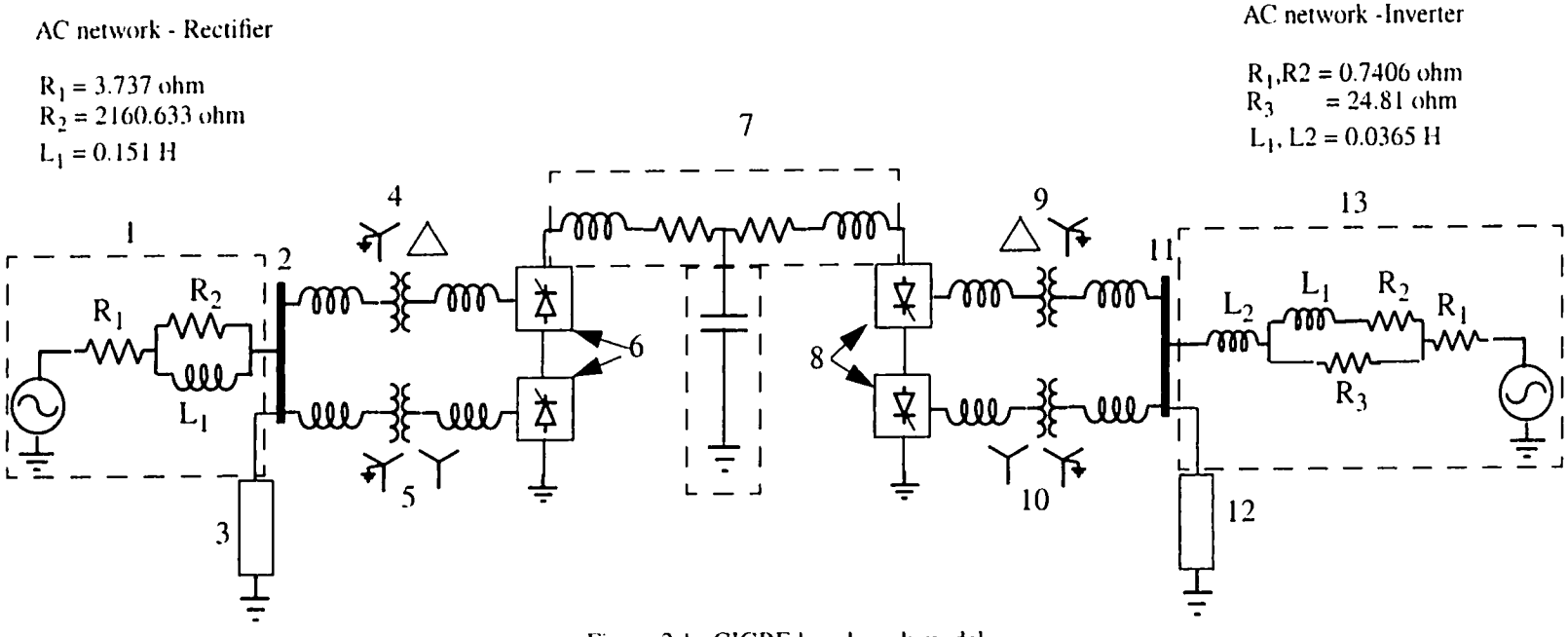


Figure 2.1 : CIGRE benchmark model

Legend

1. Rectifier side AC Network
2. Rectifier Commutation Bus
3. Rectifier side Filter & Capacitor Bank
4&5. Rectifier Transformer
6. Rectifier side 12-Pulse Converter Unit
7. DC cable with smoothing reactor
8. Inverter side 12-Pulse Converter Unit
9&10. Inverter Transformer
11. Inverter Commutation Bus
12. Inverter side Filter & Capacitor Bank
13. Inverter side AC Network

monopolar configuration is considered. This reduces the computer simulation time and minimizes memory requirements. At each end, the DC link interacts with weak AC systems having a Short Circuit Ratio (SCR) of 2.5. The CIGRE benchmark is based on a fundamental frequency of the AC systems of 50 Hz. The inverted tree form (figure 2.2) shows different subsystems and control systems of the benchmark.

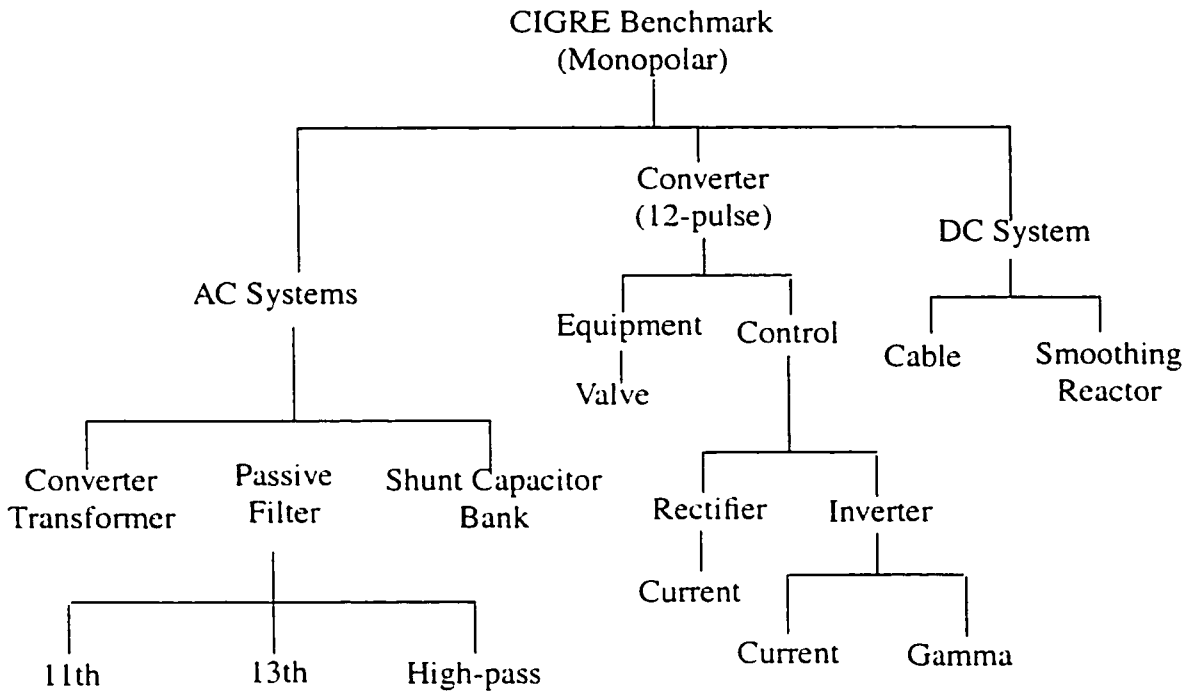


Figure 2.2: Inverted tree showing subsystems of the CIGRE benchmark

2.3 Description of Subsystems

The following subsections describe the operation of the various subsystems.

2.3.1 AC Network

The HVDC system is connected to a 50 Hz AC network at each end. The AC network

is represented by the Thevenin equivalent of the whole system behind the AC bus. In this benchmark a weak AC network is considered for each end; the impedance angles of the AC systems (84° at the rectifier end and 75° at the inverter end) are chosen to provide the necessary damping to the systems. Also, source parameters are selected such that both the sending end and the receiving end AC systems have an impedance peak near 100 Hz (i.e. second harmonic). The purpose of such selection is to create stringent operational conditions for the controllers.

2.3.2 AC Filter

The main purpose of the AC filters is to eliminate harmonics produced by the converters. Thus, unwanted harmonics are prevented from entering the AC system. The 12-pulse converter system generates characteristic harmonics of the order of 11th, 13th, 23rd, 25th, 35th, 37th and so on. In this simulation, passive tuned shunt R-L-C are used for removing lower order harmonics (i.e. 11th and 13th) and a high-pass filter is used for higher order harmonics (23rd and above). The design procedure and the frequency response of the filters are provided in the Appendix.

2.3.3 Shunt Capacitor Bank

The filters also generate a fixed amount of reactive power at the fundamental frequency. The reactive power requirement of the converters varies with the load. Passive shunt filters are used to supply 70 - 80% of the total reactive power requirement of each converter station. The remaining reactive power is compensated for by the capacitor banks. In this simulation, capacitor banks are represented by a fixed capacitor. The

arrangement of filters and the capacitor banks are shown in figure 2.3. Calculations for capacitor sizing are shown in the Appendix.

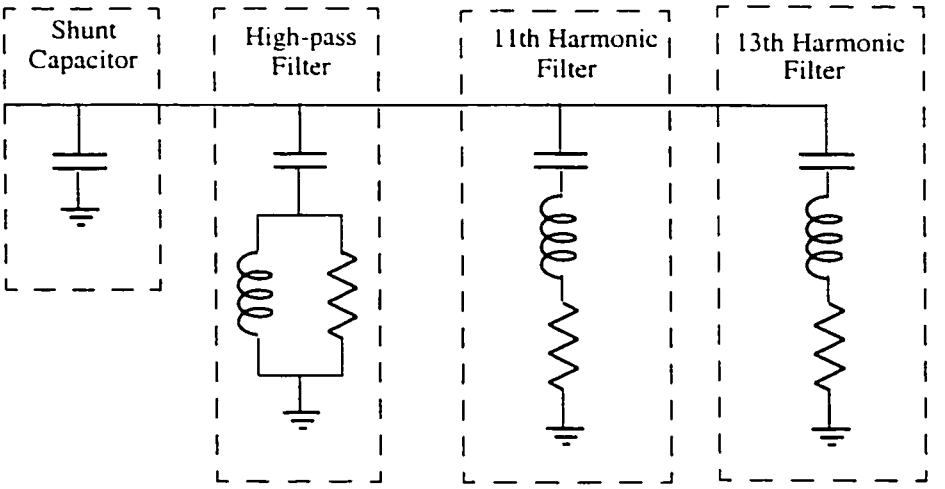


Figure 2.3: AC filter bank

2.3.4 Converter Transformer

In a 12-pulse converter system, two 6-pulse converter units are connected in series. Each 6-pulse converter unit is connected to the secondary of a converter transformer. The size and the voltage rating of each converter transformer is equal and their combination is suitable to handle the rated power at the rated voltage. Secondary (valve side) windings of one transformer are connected in STAR configuration and the other transformer windings in DELTA configuration to help cancel out some of the characteristic harmonics. The primary windings of each transformer are connected in STAR configuration with the neutral solidly grounded. Grounding provides a path for zero sequence currents caused by any asymmetrical fault in the AC system. The leakage reactance of the transformer is chosen as 18% (typical value) which is sufficient to limit the fault current through the valves. In

practice, it is always economical to design a single unit, three-phase transformer, but sometimes it becomes necessary to split the transformer into three single-phase units to facilitate transportation. In this simulation, a single unit of a three-phase transformer is considered. Converter transformers are provided with an On Line Tap Changer (OLTC), generally of the order of ±15 %. In the event of any variation in the AC system voltage, the operating delay angle of the converter shifts immediately and it is brought back again to the normal position by means of a comparatively slow acting OLTC. In this simulation no tap changer is considered because we are concerned only with transient phenomena. Calculations of transformer sizing are presented in the Appendix.

2.3.5 Converter

The converter unit does the conversion from AC to DC and vice versa. In the 12-pulse model used here, the primary windings of the converter transformers at both ends of the DC link are solidly grounded.

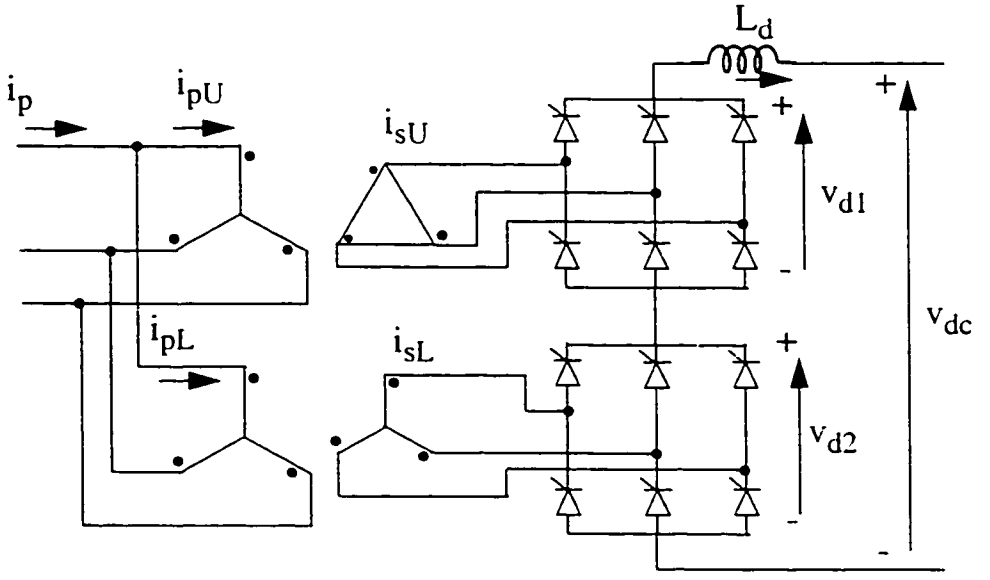


Figure 2.4: 12-pulse converter arrangement

Each 12-pulse converter unit consists of two 6-pulse converter bridges connected in series at the DC side. AC side of each converter bridge is connected to a separate converter transformer. Figure 2.4 shows a 12-pulse converter arrangement. The equivalent circuit of both the converters i.e. rectifier and the inverter, are shown in figures 2.10 and 2.11, respectively. The converter valves are protected against voltage surges by means of R-C snubber circuits and current surges by means of a smoothing reactor. The effect of snubber parameters on valve voltages are discussed in section 2.4.1

2.3.6 DC System

The DC system consists of DC cable, DC filters and smoothing reactor. In this simulation, a T-network is used to represent the DC cable. Since the inductance of the DC cable is very low, it is neglected in the simulation.

DC filters are used to eliminate higher order harmonics which may otherwise cause interference with nearby voice frequency communication circuits. For an HVDC system using a cable as a transmission link, this interference problem does not arise. Hence, DC filters are not used in this simulation with a cable.

A smoothing reactor is usually included in each pole of the converter station to satisfy the following requirements:

1. Make the commutation process more robust by limiting the rate of change of direct current,
2. Form a DC filter in combination with the cable capacitance to smooth the direct cur-

rent so that a continuous current is maintained even at light load conditions.

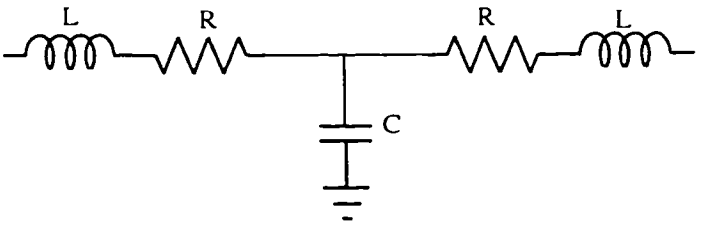


Figure 2.5: T- equivalent circuit to represent the DC cable link with smoothing reactor

The equivalent circuit for the DC cable along with smoothing reactor is shown in figure 2.5

2.4 Thyristor Modeling

In practice, a series combination of thyristors is used to achieve the required valve voltage handling capacity. Each thyristor is protected against a high rate of rise of voltage and current.

In PSCAD/EMTDC, a valve is modeled by an ideal switch having two distinct states i.e. ON and OFF. In the ON-state the valve is represented by a very small resistance (here it is $0.01\,\Omega$) and in the OFF state it is represented by a very high resistance (here it is 100 $M\Omega$). Also, there is a snubber circuit to protect the valve against a rapid rise in voltage. Large smoothing reactor protects the valves against rapid rise in current. The valve and its equivalent model are shown in figure 2.6

In this model, turn on and turn off time are not considered. But the model takes care of

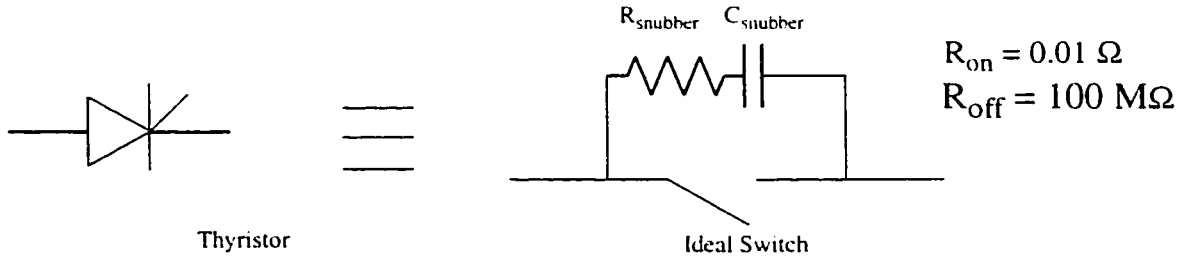


Figure 2.6: Equivalent circuit for the thyristor switch

the Reverse Recovery time. In all simulations the value of Reverse Recovery time is taken as 555μs which is equivalent to 10°.

2.4.1 Choice of Snubber Parameters

Snubber parameters i.e. $R_{snubber}$ and $C_{snubber}$ have an effect on the valve voltage. These parameters are not specified in the CIGRE benchmark. It is a fact that inappropriate values for $R_{snubber}$ and $C_{snubber}$ can lead to poor operation, over voltages and cause an erroneous measurement in delay angle specially when interacting with weak AC networks.

In figures 2.7a and 2.7b the effect of snubber resistance and capacitance are shown. It is evident from the figures that resistance has more impact on the valve voltage than the capacitor. The parameters $R_{snubber}$ and $C_{snubber}$ are adjusted until the satisfactory commutation voltage across the valve is obtained. In this simulation the value of $R_{snubber}$ =5000Ω and $C_{snubber}$ = 0.05μF were selected for the snubber. However, it is to be noted that these values have no correlation with an actual snubber circuit used in practice.

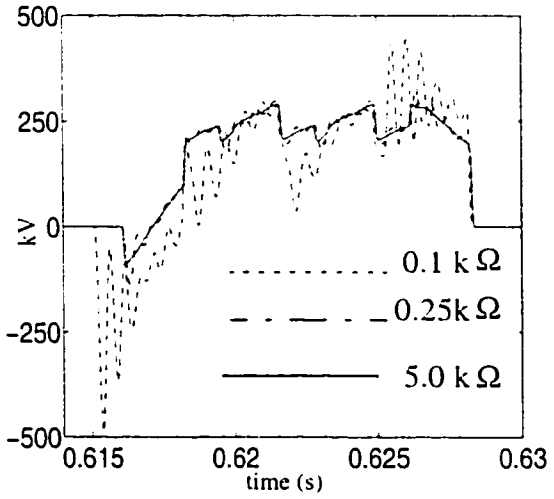


Figure 2.7a: Variation of VV with $R_{snubber}$

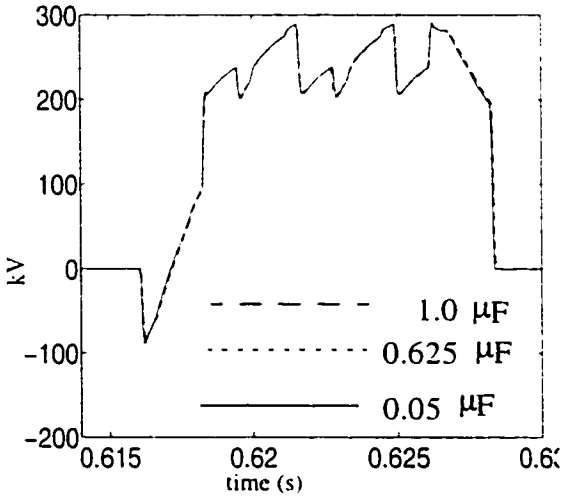


Figure 2.7b: Variation of VV with $C_{snubber}$

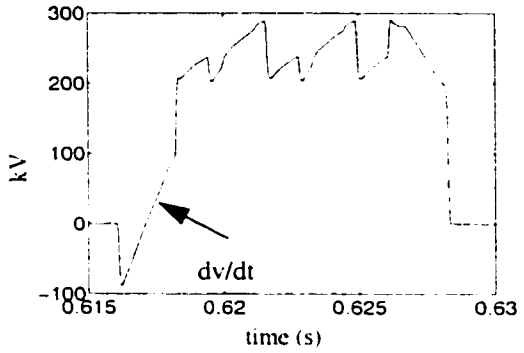


Figure 2.8a: Valve voltage showing dv/dt

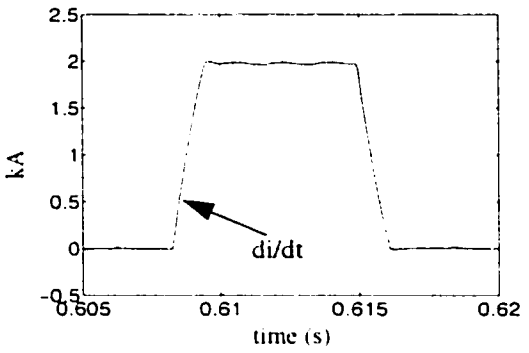


Figure 2.8b: Valve current showing di/dt

2.5 Analysis of Converter Bridge

Figure 2.9 shows a conventional 6-pulse converter bridge

The following assumptions are made for the analysis of the converter:

- Direct current I_{dc} is constant,
- Valves are ideal switches, and
- AC system is strong (infinite).

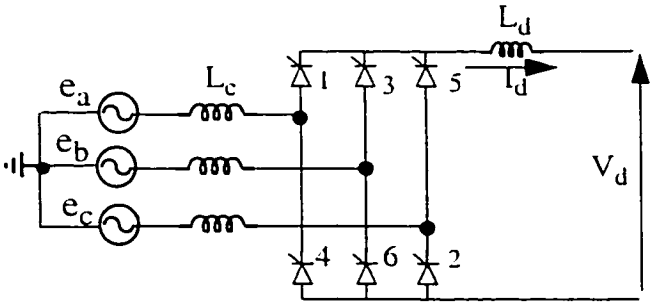


Figure 2.9: 6-pulse bridge circuit

Due to the leakage reactance of the converter transformer, commutation from one valve to the next is not instantaneous. An overlap period is necessary and depending on the magnitude of the leakage reactance, either two, three or four valves may conduct at any one time.

The analysis of the bridge gives the following DC output voltages:

For a Rectifier:

$$V_{dcr} = V_{dcor} \cdot \cos\alpha - R_{cr} \cdot I_{dc} \qquad (1)$$

where

$$V_{dcor} = \frac{3}{\pi} \cdot \sqrt{2} \cdot V_{LLr} \text{ and}$$

$$R_{cr} = \frac{3}{\pi} \cdot \omega \cdot L_{cr}$$

For an Inverter:

There are two options possible depending on the choice of the delay angle or extinction angle as the control variable

$$V_{dci} = V_{dcoi} \cdot \cos\beta + R_{ci} \cdot I_{dc} \qquad (2)$$

$$V_{dci} = V_{dcoi} \cdot \cos\gamma - R_{ci} \cdot I_{dc} \qquad (3)$$

where

$$V_{dcoi} = \frac{3}{\pi} \cdot \sqrt{2} \cdot V_{LLi}$$

and

$$R_{ci} = \frac{3}{\pi} \cdot \omega \cdot L_{ci}$$

with

V_{LLr}/V_{LLi} = Line to Line voltage of the ac bus Rectifier/Inverter respectively

V_{dcr}/V_{dci} = DC voltage at the Rectifier/Inverter respectively

V_{dcor}/V_{dcoi} = Open circuit dc voltage at the Rectifier/Inverter respectively

I_{dc} = Direct current in the DC link

R_{cr}/R_{ci} = Equivalent commutation resistance at the rectifier/inverter respectively

R_L = Resistance of the DC link

L_{cr}/L_{ci} = Leakage inductance of the rectifier/inverter transformer respectively

α = Delay angle

β = Advance angle at the inverter, ($\beta = \pi - \alpha$)

γ = Extinction angle at the inverter, ($\gamma = \pi - \alpha - \mu$)

μ = Overlap angle

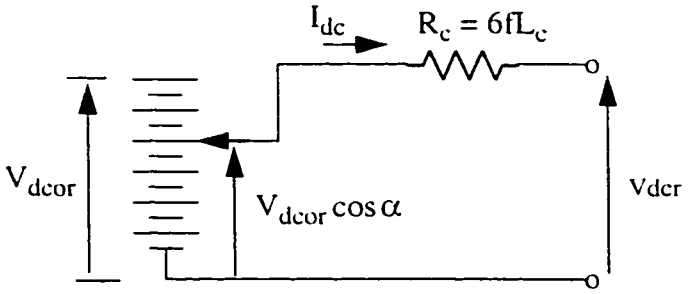


Figure 2.10: Equivalent circuit of rectifier

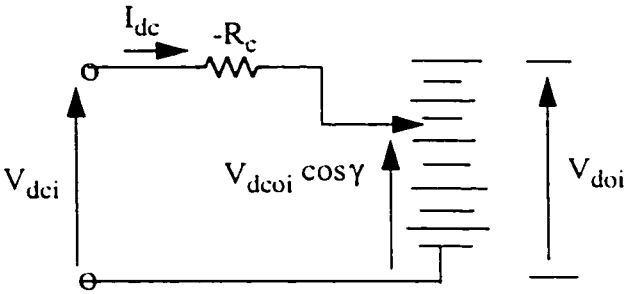


Figure 2.11: Equivalent circuit of inverter

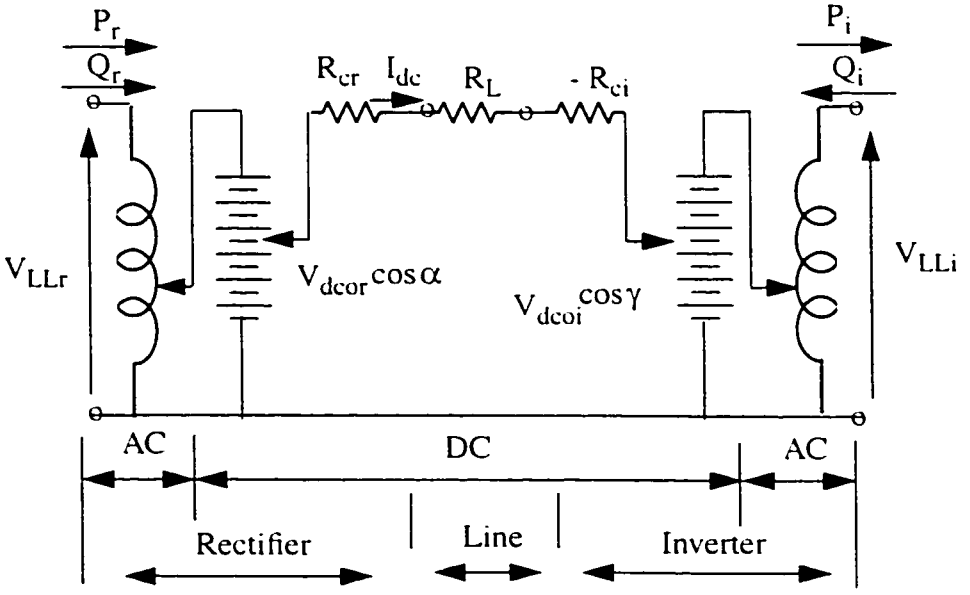


Figure 2.12: Equivalent circuit of two terminal HVDC system

2.6 Purpose of Control

The main purposes of the control strategy employed are to:

1. Limit maximum direct current to avoid valve damage
2. Keep the DC voltage level high to reduce power transmission loss
3. Maintaining a minimum extinction angle to avoid commutation failure
4. Maintaining a minimum firing angle to reduce reactive power consumption

2.6.1 Control Strategy

An HVDC system can transport large amounts of power which can be accomplished under tightly controlled conditions. Both the direct current and voltage can be precisely controlled to effect the desired power transfer.

An equivalent circuit for the DC link is shown in figure 2.13. The direct current is given by

$$I_{dc} = \frac{V_{dcr} - V_{dci}}{R_{dc}} = \frac{V_{dcor}\cos\alpha - V_{dcoi}\cos\gamma}{R_{cr} + R_L - R_{ci}} \qquad (4)$$

From equation (4), the control of I_{dc} can be achieved by:

1. Varying the Rectifier DC voltage
2. Varying the Inverter DC voltage

The rectifier side DC voltage can be controlled by two ways:

- Varying delay angle α (fast control)
- Varying AC side voltage by means of transformer tap changer (slow control)

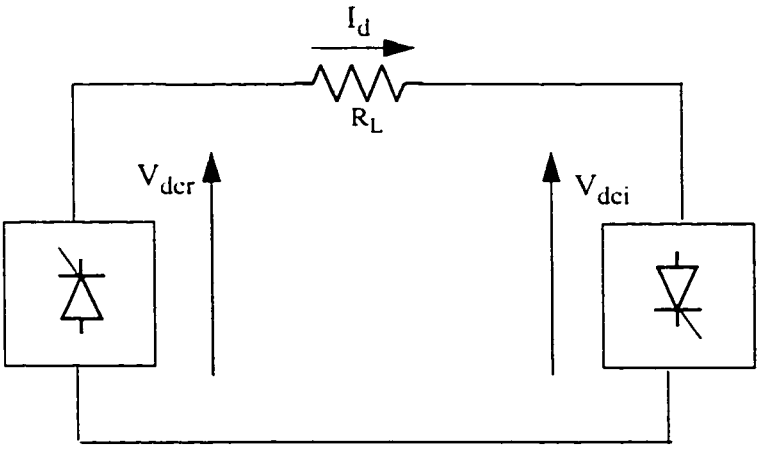


Figure 2.13: Equivalent circuit of DC link

Similarly, Inverter side DC voltage can be controlled by two ways:

- Varying advance angle β (fast control)
- Varying AC side voltage by means of tap changer (slow control)

The DC power transmitted is given by

$$P_{dc} = V_{dc} \times I_{dc}$$

Three characteristics, as defined by equations (1) - (3), are shown in figure 2.14.

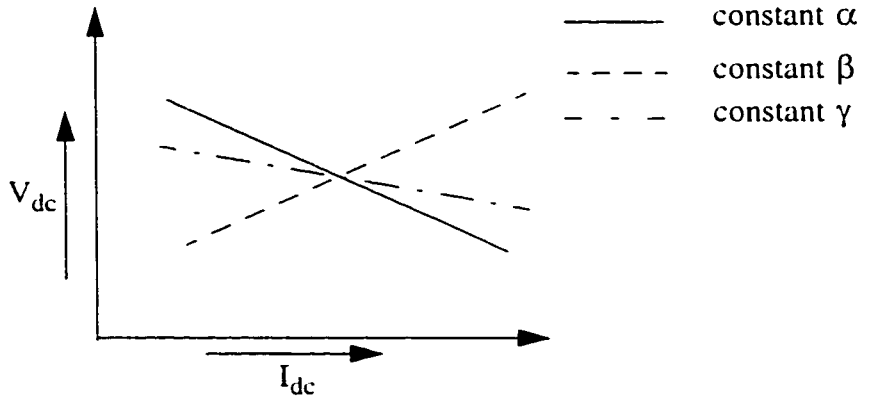


Figure 2.14: Choice of control strategy for DC link [15]

2.6.2 Control Characteristics

Under steady state conditions in a two terminal HVDC system, the inverter is assigned the task of controlling the DC voltage by maintaining a minimum Constant Extinction Angle (CEA) which causes the DC voltage V_{dc} to droop with increasing direct current I_{dc}. This is shown by the CEA characteristic PQ in figure 2.15. The weaker the AC system at the inverter, the steeper the droop.

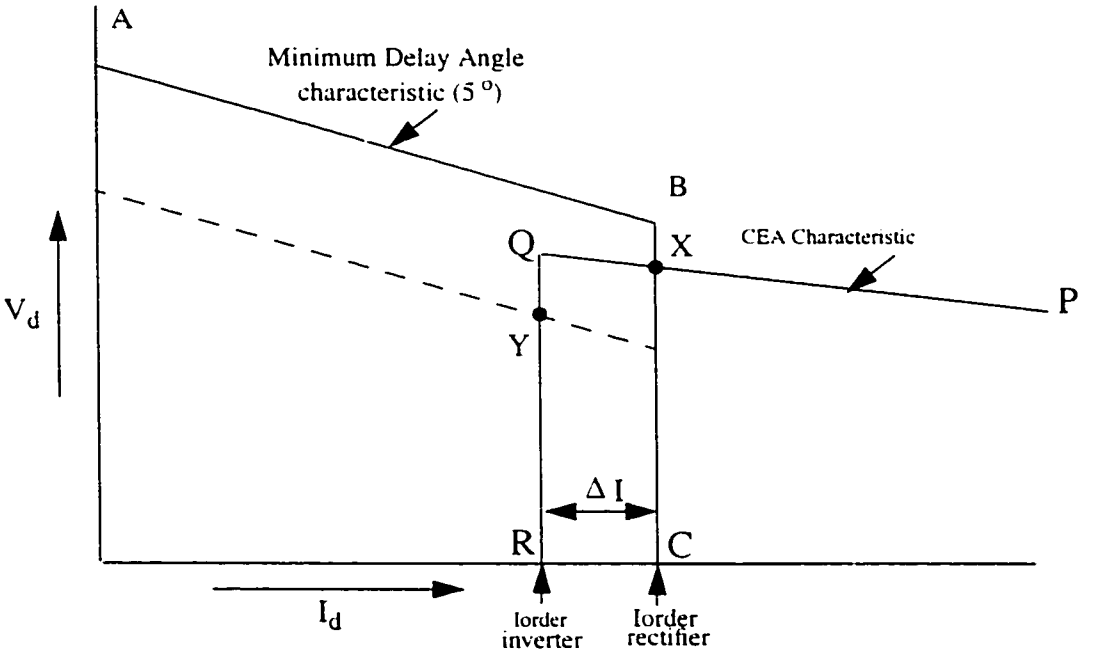


Figure 2.15: Control characteristics [15]

If the inverter is operating at a minimum constant γ characteristic, then the rectifier must control the direct current. In figure 2.15 the vertical line BC represents the rectifier constant current characteristic. The point X of intersection of these two characteristics (i.e.

line BC and line PQ) gives the operating point under steady state for the DC link. This operating point is reached by the action of the OLTC of the converter transformers at the inverter end.

The OLTC of the converter transformers at the rectifier end are controlled to adjust their tap settings so that the delay angle α has a working range between 10° to 20° for maintaining the constant current setting I_{order}. The delay angle characteristic is shown by the line AB in Figure 2.15. If there is any voltage rise in the rectifier side AC bus, the immediate implication on the DC system will be the current increase. The delay angle will immediately be increased to maintain I_{dc} constant. Should the delay angle deviate from a set value, then the OLTC starts its action and reduces the voltage to bring back the delay angle to its normal operating point.

If there is a voltage dip, opposite action takes place. Rectifier current controller decreases the delay angle to maintain I_{dc} constant. But for a larger voltage dip, it is not possible to decrease the delay angle lower than the minimum limit (=5°), and the rectifier current controller loses its control over the current.

To counter act this situation, inverter side converter is also provided with a current controller. The constant current characteristic of the inverter is shown by the vertical line QR in figure 2.15. However, the current demanded by the inverter I_{di} is less than the current demanded by the rectifier I_{dr} by the current margin ΔI which is typically about 0.1 p.u. The current margin is selected to be large enough to avoid any malfunction due to the presence of harmonics in the direct current.

Now, with the inverter current controller, if there is any voltage dip in the AC bus of the rectifier, the current will immediately reduce and the operating point moves from point X to point Y which is on the inverter constant current characteristic QR. At this point current is reduced to 0.9 p.u. of its previous value and the voltage control of the DC link will shift to the rectifier. However power transmission will largely be maintained near 90% of its original value.

If there is any small change in the AC network voltage at the inverter end, the system will behave accordingly, as described above.

2.6.3 Modified Control Characteristics

The control strategy described above is used under steady state operation. However, following modifications are done to maintain power flow even under system disturbances.

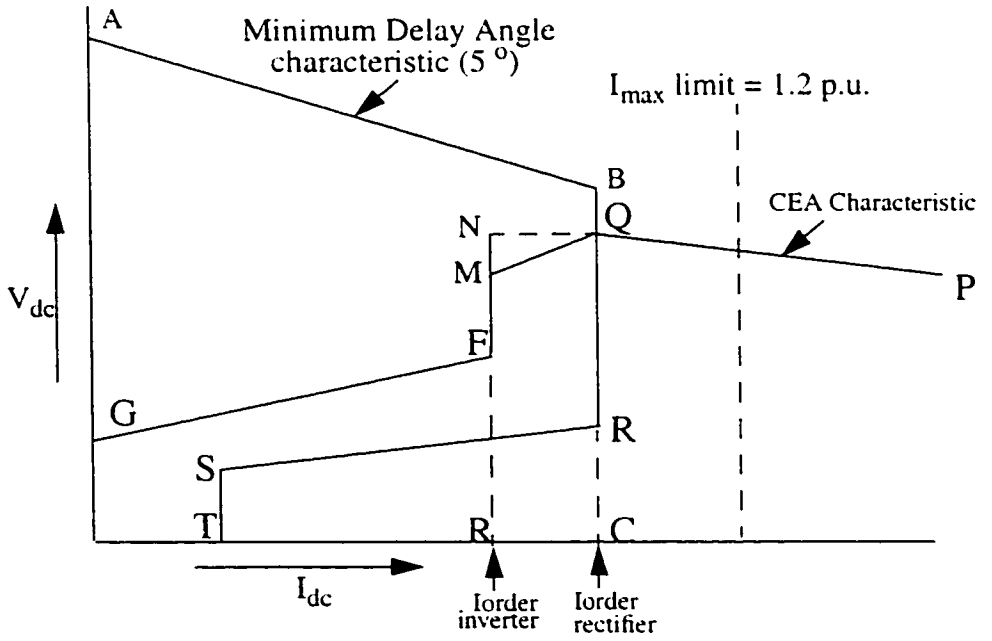


Figure 2.16: Modified control characteristics [15]

Figure 2.16 shows the modified control characteristics. Two new characteristics are included as a protective modification. This modification is made to limit the direct current reference as a function of the DC voltage. This modification assists the DC link to recover smoothly from faults. During disturbances when the AC voltage at the rectifier or the inverter is depressed, the current through the link is brought to a minimum value by means of the Voltage Dependent Current Limiter (VDCL). Line R-S-T and F-G represent the VDCL characteristics for the rectifier and inverter, respectively. The line F-G is also called the α_{min}-in-inverter characteristic as it prevents the inverter from operating in the rectifier region by imposing an alpha-minimum-limit of about $110°$.

When the inverter interacts with a weak AC system, the slope of the CEA control mode characteristic is quite steep and may cause multiple crossover points with the rectifier characteristic. To avoid this possibility, the inverter CEA characteristic is usually modified into either a constant beta characteristic (line QM) or a constant voltage characteristic (line QN) within the current error region.

2.7 Summary

In this chapter, an HVDC system based on the CIGRE Benchmark is presented. Descriptions of various subsystems such as AC networks, filters, converters, converter transformers and DC cable are presented. Modeling of each subsystem is performed by using PSCAD/EMTDC simulation package. The control strategies employed are also discussed.

Chapter 3

Converter Configurations and Control Implementation

3.1 Introduction

An HVDC system with a long DC cable is prone to commutation failures because the cable has a large capacitance which discharges whenever there is a voltage dip in the inverter side AC network. Each occurrence of a commutation failure stresses the valves for a certain period of time before the protective controller comes into action. Thus, frequent commutation failures can lead to system problems and possible damage of the valves. To overcome this problem different converter configurations have been suggested.

In this chapter, besides the conventional converter configuration, two other converter configurations are proposed. Certain important aspects of these converters such as commutation, commutation overlap angle, extinction angle and commutation margin are discussed. In addition block diagrams of the different control loops are also shown. Finally, a design procedure for selecting the parameters of the PI controllers is presented.

3.2 Commutation, Commutation Overlap Angle, Extinction Angle and Commutation Margin

In a 6-pulse bridge converter (figure 2.9), commutation means the transfer of current from one valve to another in the same row. This is achieved by successive triggering of valves in a sequential manner provided the incoming valve is forward biased and the trig-

gering pulse is applied.

If the commutation circuit is resistive, the transfer of current takes place instantly. But in practice the converter transformer has leakage reactance which acts as a commutation reactance and commutation is delayed. This delay in commutation is expressed by the Commutation Overlap Angle μ. The value of this angle depends on the commutation reactance, the direct current and the commutation voltage.

Also, depending on the commutation overlap angle, 2 or 3 valves take part in the commutation. For an inverter, the outgoing valve must get sufficient time to regain its full blocking property. Hence, it must stop conduction well before the positive zero crossing of the AC bus voltage, otherwise commutation failure will occur. The time interval between the end of commutation and the instant of positive zero crossing of the AC bus voltage is known as the Extinction Angle γ.

Commutation margin [4] is the angle between the end of commutation and the positive zero crossing of the valve voltage. For the Line Commutated Converter (LCC) configuration, extinction angle and commutation margin are equal.

3.3 Line Commutated Converter (LCC) Configuration

The single line diagram of a 12-pulse conventional converter for an HVDC system is shown in figure 3.1. The leakage reactance X_L of the converter transformer is also the commutation reactance for the LCC configuration.

In figure 3.2, the steady-state valve-voltage and the commutation voltage that are obtained from the simulation are depicted. In figure 3.3, the extinction angle and the commutation overlap angle are shown in expanded form. Point A indicates the end of commu

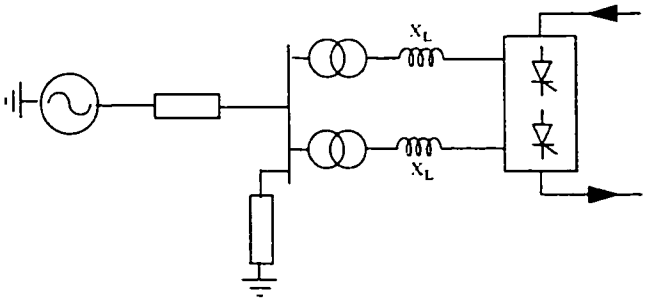


Figure 3.1: Line Commutated Converter (LCC) configuration

tation and B indicates the instant of AC bus voltage and the valve voltage positive zero crossing. Hence, the extinction angle and the commutation margin is the same for the LCC

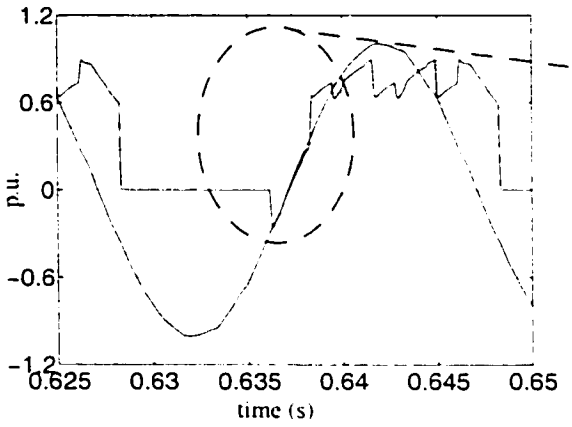


Figure 3.2: Commutation voltage and valve voltage for LCC configuration

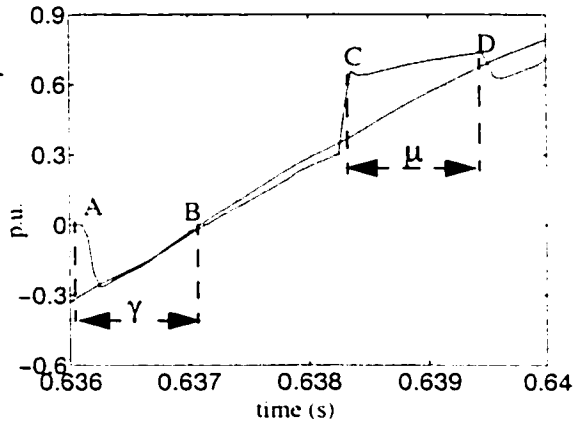


Figure 3.3: Extinction angle and commutation overlap angle for LCC configuration

configuration. During this interval AB, the voltage across the outgoing valve is negative and the valve has to regain its full blocking property within the time period AB. It is important to note that if the outgoing valve fails to regain its full blocking property, it may start conducting again giving rise to a commutation failure. The time interval CD indicates the commutation overlap angle μ which is approximately equal to $20°$.

3.4 Capacitor Commutated Converter (CCC) Configuration

As already discussed in section 3.1, the DC cable poses a problem for the HVDC system because of its high discharge current. This problem is overcome by inserting a capacitor in each phase of the commutating circuit. Figure 3.4 shows the single line diagram of a 12-pulse Capacitor Commutated Converter (CCC) configuration.

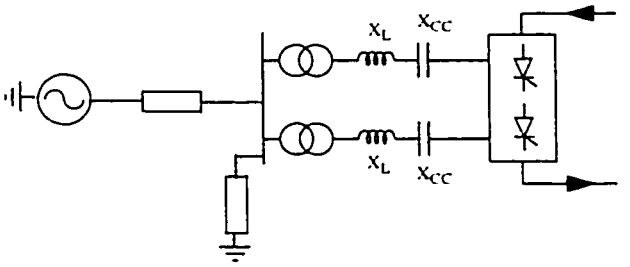


Figure 3.4: Capacitor Commutated Converter (CCC) configuration

The basic arrangement is the same as that of the conventional configuration except for the presence of the commutation capacitor CC. The reactance of the commutation capacitor is represented by X_{CC}.

In figure 3.5 the steady-state valve-voltage and the AC bus voltage that are obtained from simulation are depicted. Figure 3.6 shows the extinction angle, commutation overlap angle and the commutation margin in detail. From this figure, it is evident that the commutation capacitance introduces a phase lag to the valve voltage and as a result the instant of positive zero crossing of the AC bus voltage and that of the valve voltage does not coincide. In figure 3.6, AB and AC indicate the extinction angle and the commutation margin, respectively. It is clearly observed that CCC configuration has a larger commutation mar-

gin, which means that the chances of a commutation failure are reduced as compared to the case of the LCC configuration.

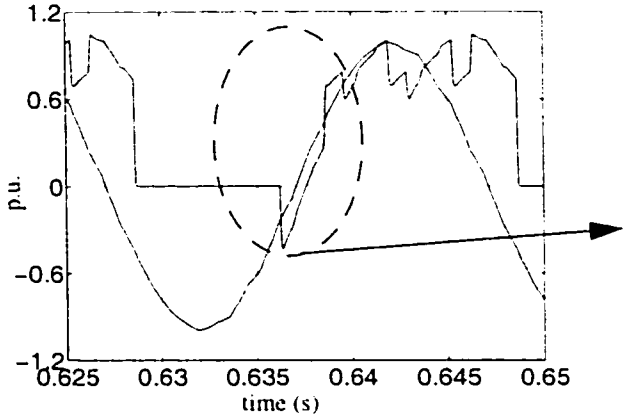


Figure 3.5: Commutation voltage and valve voltage for CCC configuration

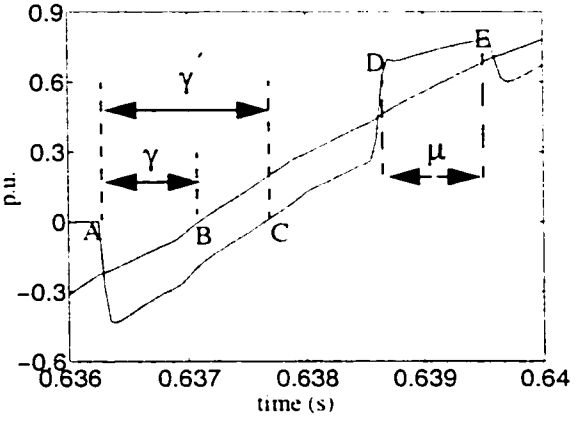


Figure 3.6: Extinction angle and commutation overlap angle for CCC configuration

Interpreted alternatively, this means that the CCC configuration has much more flexibility to operate the system with a lower value of gamma. In simulation studies for the CCC, the operating value of gamma is set at 12°.

3.5 Commutation Overlap Angle for CCC Configuration

The time interval DE in figure 3.6 indicates the overlap angle (μ) for the CCC configuration. It is less than the overlap angle for the LCC configuration as obtained from simulation and shown in figure 3.3. This establishes the fact that, because of the presence of the commutating capacitor the effective commutation reactance is reduced. Also, because of the lower commutation overlap angle, the magnitude of the harmonics is higher, but the order of harmonics is the same as that of the LCC configuration. Details of these harmonics are given in the Appendix.

3.6 Valve Stresses

In the case of the conventional converter, the secondary line voltage of the converter transformer appears across the valve. But in the case of the CCC configuration, the commutation capacitor provides an additional voltage (I_{dc} * X_{cc}) to the valve. As a result, the voltage stress of the valve increases.

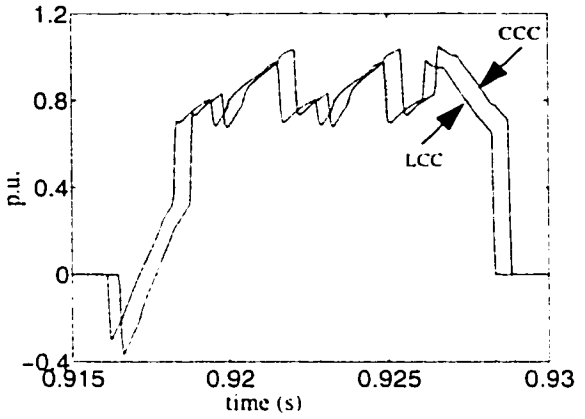


Figure 3.7: Comparison of valve stress for LCC and CCC configurations

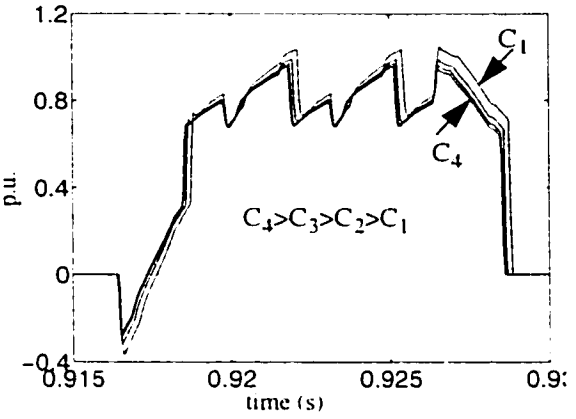


Figure 3.8: Variation of valve stress with CC size

Figure 3.7 shows the steady-state valve-voltages for the LCC and CCC configurations, as obtained from simulations. It is evident that the valve with the CCC configuration has higher peak stress than that with the LCC configuration.

3.7 Size of Commutation Capacitor

The valve voltage stresses are inversely proportional to the size of the commutation capacitor. In this study, we have limited the acceptable increase in voltage stress across the valve in the CCC configuration to be 10% greater than a comparable LCC configuration.

The commutation margin also varies inversely with the commutation capacitor size. The smaller the size of the commutation capacitor, the more the commutation margin and the better the performance with respect to commutation failures. Since the voltage stresses increase the cost of the valve directly, it becomes the limiting factor to decide the size of the commutation capacitor. The variation of the voltage stress of the valve with commutation capacitor size is shown in figure 3.8.

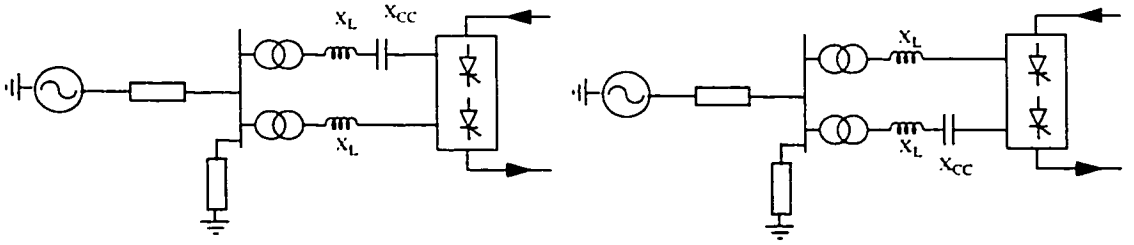
3.8 Reactive Power Generation

Apart from increasing the commutation margin, the commutation capacitor also generates capacitive reactive power. Hence, the size of the shunt capacitor bank can be proportionately reduced to maintain the constant reactive power supplied to the bridge. Details of the shunt capacitor bank for different converter configurations are shown in the Appendix. Also, this reactive power generation increases with the increase of load. Hence the net reactive power variation with load is reduced. This is definitely an added advantage from the point of view of shunt capacitor switching to match load requirements.

3.9 Hybrid Converter Combination (HCC) Cofiguration

Figure 3.9 shows the single line diagram of the Hybrid converter configuration. In this configuration, both conventional and capacitor commutated converters are used. Depending on the location of the commutation capacitor two different configurations are possible. The configuration with the commutation capacitor is placed in the upper converter is denoted by HCC-UP. The other in which the commutation capacitor is placed in the lower converter is denoted by HCC-LO. Ideally there should be no operational behaviour differ-

ence between these two configurations. But because of the different connections of the converter transformer i.e. STAR or DELTA, the net effect of the commutation capacitor may be different. Hence, each configuration is studied separately.



(a) HCC-UP (b) HCC-LO

Figure 3.9: Hybrid Converter Combination (HCC) configuration

3.10 Implementation of Control

It is well known that proportional type of controllers have the limitation that it is often difficult to find a proper gain so that the steady-state and the transient responses satisfy their respective requirements [24]. In practice, single gain parameter is seldom sufficient to meet the design requirements on two performance criteria. It is, therefore, logical to perform other operations, in addition to the proportional control on the actuating signal.

Both Proportional plus Integral (PI) and Proportional plus Derivative (PD) controllers are fast in action but PI controller has an advantage over PD controller that it can reduce the steady state error of the system under consideration to zero. Besides, PD controller has the characteristic of a high-pass filter which tends to propagate noise and disturbances throughout the system.

Therefore, PI controllers are used to independently control the following three variables:

1. Rectifier current,
2. Inverter current, and
3. Inverter extinction angle, gamma

As converter plant is inherently non linear, optimization of controller gain parameters is difficult. In practice, controllers are pre-tested in a physical simulator environment to obtain appropriate gain settings while final adjustment is done at site. The design of the PI controller is discussed in a later part of this chapter.

3.10.1 Control Loop in Rectifier

The block diagram of the control loop for the rectifier is shown in figure 3.10. Rectifier Current Order (CO) is derived from the current reference (I_{ref}) and the output of the Voltage Dependent Current Limiter (VDCL). Selection of CO is made by the 'MIN SELECT' block. VDCL acts as a protective device in this control loop.It produces a curre-

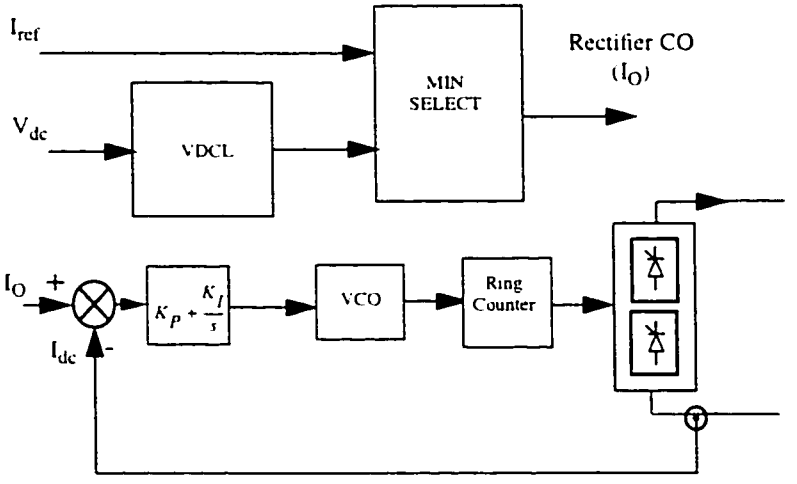


Figure 3.10: Block diagram of the rectifier control loop for LCC, CCC and HCC configurations

nt output in response to the inverter DC voltage that it receives as input. Figure 3.11 shows the VDCL characteristic. It has three distinct portions:

- Portion 1:

The upper part gives an output of 1 p.u. for the inverter DC voltage, $V_{dc} \geq 0.9$ p.u. This part prevents the VDCL from acting under small variations in the AC network voltage. Thus steady state CO remains unaffected.

- Portion 2:

The middle part of the characteristic gives a CO proportional to the input and helps the DC link maintain a power flow of reduced lower order as a function of the moderate depression in the AC network voltage.

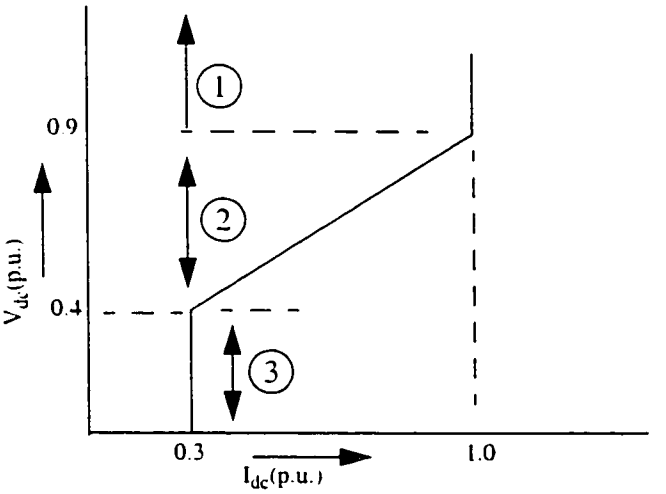


Figure 3.11: VDCL characteristic

- Portion 3:

The lower part of the characteristic takes the preventive measure to reduce the CO to a low value (here it is 0.3 p.u.) as soon as the inverter side DC voltage falls below a specified limit. In our simulations, this limit is set to 0.4 p.u. Hence, during a DC fault or commuta-

tion failure, this characteristic helps the DC link maintain a very low current and protects the valves from damage.

The CO acts as the current reference for the rectifier alpha order. It is compared with the measured direct current to obtain an error signal. This error signal is fed to the PI controller whose output is used to activate a Voltage Controlled Oscillator (VCO).

The voltage pulses generated by the VCO are synchronised with the commutation voltage and applied to the valves in a proper sequence through a ring counter.

3.10.2 Control Loop in Inverter for LCC and CCC Configurations

The block diagram of the inverter control loop for the LCC and CCC configurations is shown in figure 3.12. As already discussed, in the inverter mode of operation, a commutation failure can occur if the extinction angle is too small. Hence, preventive measures must be taken so that the inverter can follow a minimum Constant Extinction Angle Characteristic (CEA). This characteristic is achieved by a gamma loop in the inverter control circuit. The minimum gamma is selected from the twelve valve voltages and an error signal is derived from the measured minimum gamma (γ_{meas}) and the desired gamma (γ_{ref}).

Since only one converter can maintain current control in the DC link, the inverter current controller is often biased off by a current margin signal (ΔI) which is subtracted from the current order (I_O). The selection between two controllers at the inverter is made by a "MIN SELECT" block.

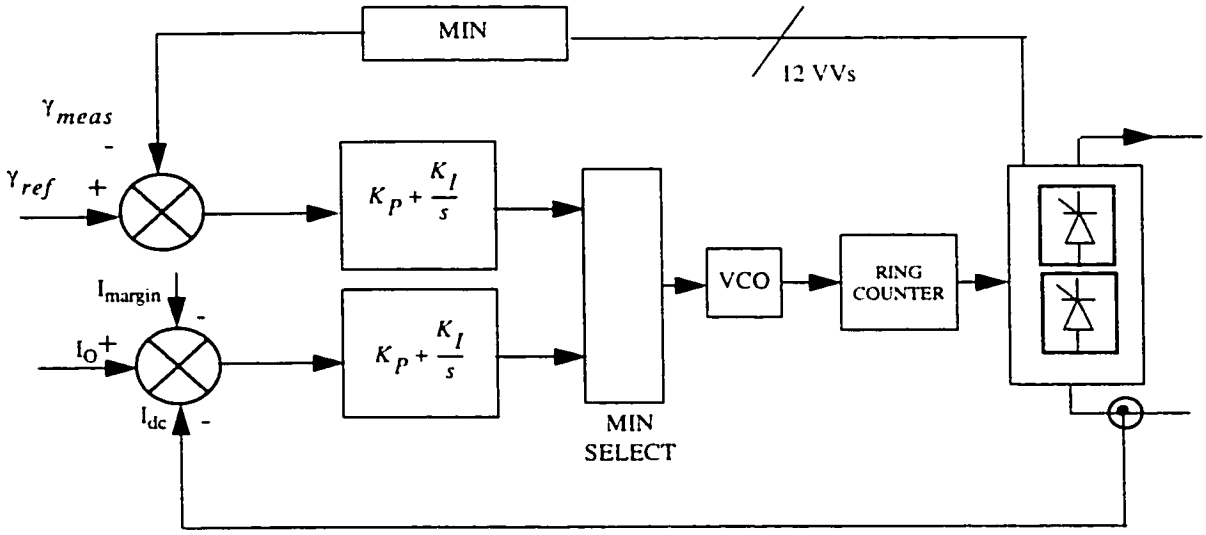


Figure 3.12: Block diagram of the inverter control loop for LCC and CCC configurations

3.10.3 Control Loop in Inverter for HCC Configuration

In case of the HCC configuration, the rectifier side converters are configured in the same way as that of the LCC or CCC but at the inverter side where some modifications are done to achieve independent control of the upper and lower converter. Since the operating ranges of gamma for the upper and lower converters are different, two separate and independent gamma controllers are used. The block diagram of the inverter control loop for the HCC configuration is shown in figure 3.13. Operation of each gamma controller is similar to that described for LCC or CCC configuration.

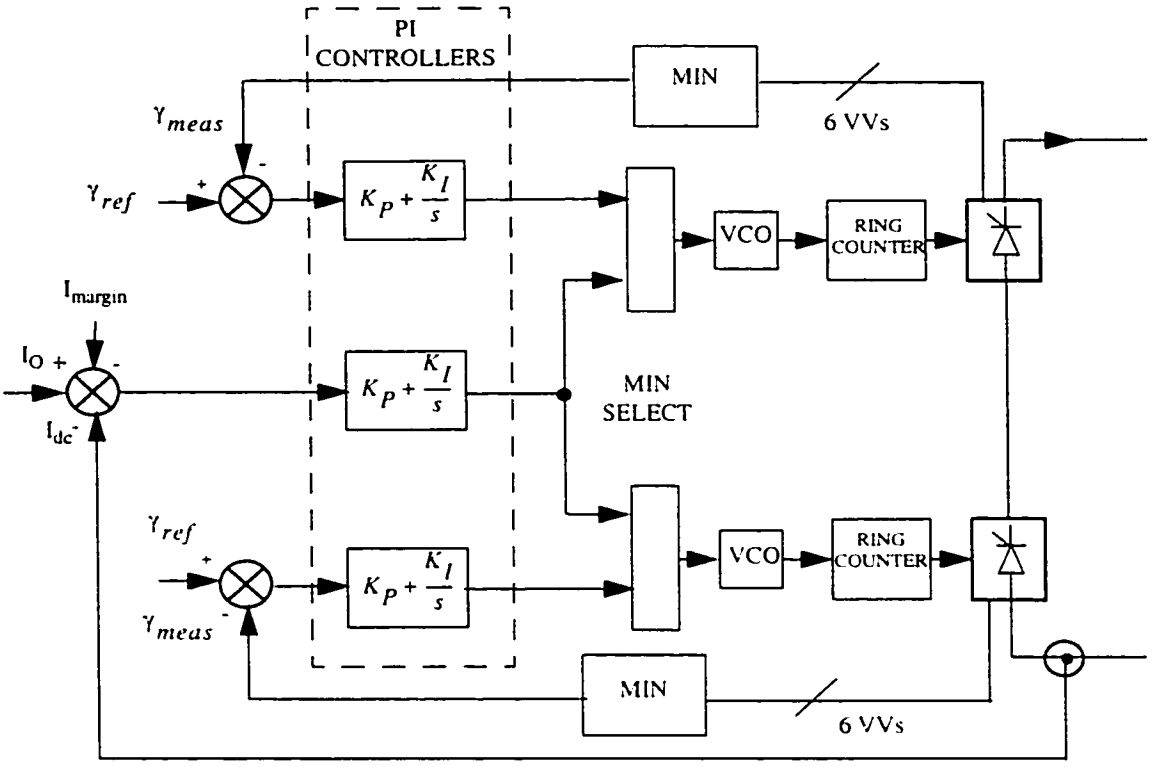


Figure 3.13: Block diagram of the inverter control loop for HCC configuration

3.11 PI Controller

For a two terminal HVDC system under normal conditions, the rectifier is assigned the duty of maintaining constant direct current while the inverter is assigned the duty of maintaining constant DC voltage (gamma). Both ends of the system rely on the traditional PI controllers to provide fast control action. Figure 3.14 shows the block diagram of the PI controller used for controlling current or gamma. The basic structure of the controller is the same except for the reference and the measured quantities.

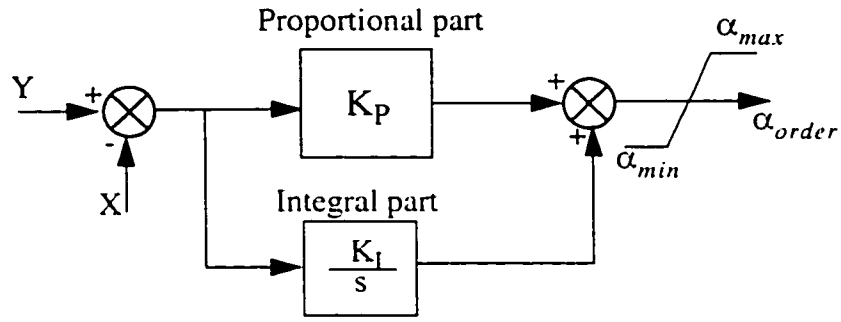


Figure 3.14: Block diagram of the PI controller

In case of a current controller Y represents the reference current (I_{ref}) and X represents the measured direct current (I_{dc}). In the case of the gamma controller, Y represents the reference gamma (γ_{ref}) and X represents the measured gamma (γ_{meas}). In both cases, an error signal is generated for the PI controller. The transfer function of the PI controller is given by

$$G_{CONT}(s) = K_P + \frac{K_I}{s}$$

where Kp is the proportional gain and K_I is the integral gain of the controller.

The transient performance of the DC link depends very much on the parameters of the

PI controllers. The dynamic response of the current controller is affected by the combination of short circuit level at the commutation bus and by the converter commutation reactance and the AC network equivalent impedance at the commutation bus. Therefore, the tuning of the controller parameters (K_P and K_I) is a function of all the net converter commutation resistance. This resistance may vary with the network operating conditions and is affected by the AC network contigencies. As a result, parameters of the PI controller used for HVDC systems are optimum only for a limited range of operation. Also prior knowledge of the system dynamics is required to optimize these parameters. This limitation can be overcome by using modern controllers based on Neural Networks [21] or Fuzzy logic [25].

3.11.1 PI Controller Design

The following sections describe the design of the PI controllers.

3.11.1.1 Rectifier Current Controller

Ignoring the effect of impedance of the AC sides, the models for the rectifier and the inverter are identical. The simplified transfer function [12] of the converter is

$$G_{CONV}(s) = \frac{K_C}{1 + \tau_C s} \quad \text{and that of the measuring device is} \quad G_{MEAS}(s) = \frac{K_M}{1 + \tau_M s}$$

Taking the cable into consideration, the transfer function of the converter system is

$$G_{SYS}(s) = \frac{K_C(RCs + 1)}{(1 + \tau_C s)(R^2 Cs + 2R)}$$

Where, K_C = gain of the converter = 1.35 V_{LL} (V_{LL} is line to line voltage in kV)

τ_C = time constant of the converter = 0.005 sec

K_M = gain of the measuring device = 0.5

τ_M = time constant of the measuring device = 0.0012 sec

R = resistance of the cable (upto mid point) = 2.5 Ω

C = capacitance of the cable = 26 μF

Preliminary selection of the gain parameters for the controllers is achieved by Bode plot taking the relative stability requirements (gain margin and phase margin) into consideration. Matlab is used to compute the gain margin and the phase margin. By trial and error, the gains are selected in such a way that the gain margin > 6 dB and phase margin between 40° - 60° are obtained. The Bode plots of the rectifier control system are shown in figure 3.15.

3.11.1.2 Inverter Current Controller

Following similar procedure the approximate parameters for the inverter PI controller are obtained. The Bode plots for the inverter control system is shown in figure 3.16. A similar procedure is followed for designing the parameters of the gamma controller.

Although the parameters obtained here are approximate only, they are useful as starting values for the simulation. More precise values of controller parameters are obtained from further detailed simulation. This is carried out by adjusting the controller gains until the desired time responses to the step input are obtained. The values of the controller gains are given in Table 1 and the response of different controllers are depicted in Chapter 4.

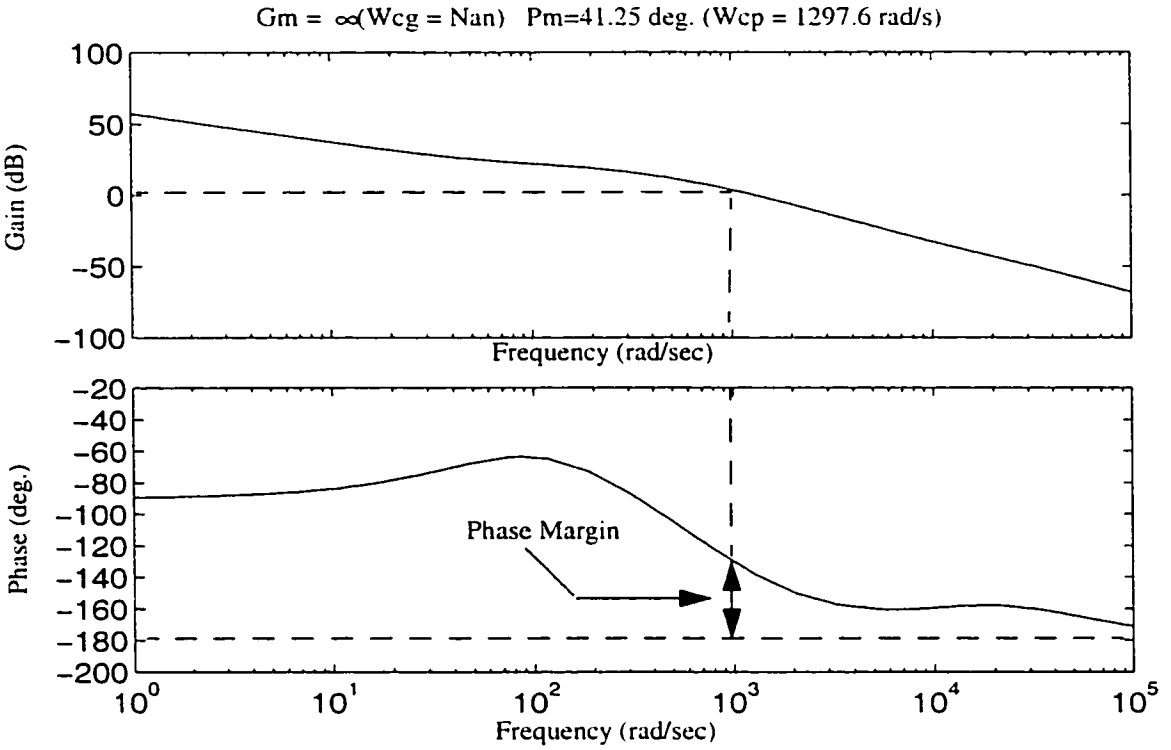


Figure 3.15 : Bode plot of the rectifier control system

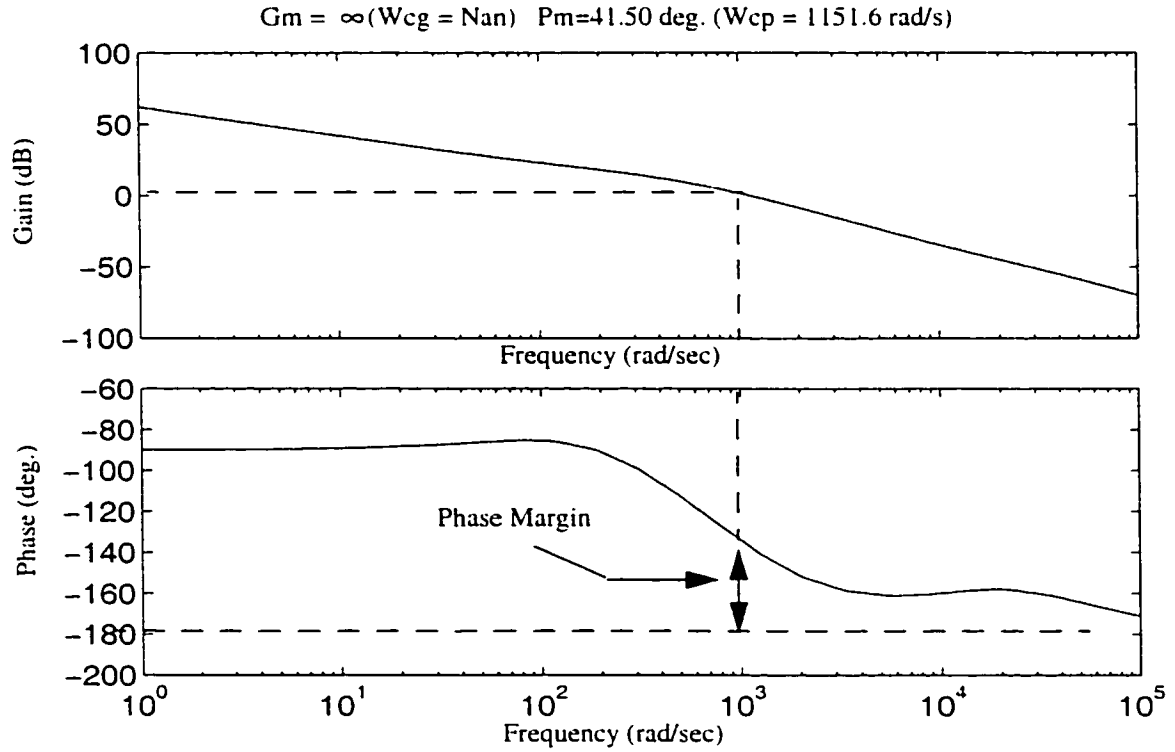


Figure 3.16 : Bode plot of the inverter control system

Table 1: Controller Gains

Gain	Controller		
	Rectifier	Inverter	
	current	current	gamma
K_P	Calculated = 0.45 Used = 0.70	Calculated = 0.35 Used = 0.75	Calculated = * Used = 0.75
K_I	Calculated = 25 Used = 40	Calculated = 45 Used = 50	Calculated = * Used = 15

* Value not available at the time of printing

3.12 Summary

Different converter configurations are presented in this chapter. The effect of commutation capacitors on gamma margin, commutation overlap angle and valve voltage stresses are shown. Control loops for different configurations are described using block diagrams. Finally, design procedure for the PI controllers are described.

Chapter 4

Behaviour of HVDC System under Transient Conditions

4.1 Introduction

Since the transient performance of an HVDC system is greatly affected by the strength of the connected AC networks, such an HVDC system (interacting with weak AC networks) must be tested more thoroughly under different transient conditions. As the system controllers are used for control purposes as well as protection purposes, it is very important to test the operation of the controllers (current and gamma controllers as well as the protection circuit such as VDCL) under various transient conditions.

In this chapter, results of different transient tests such as symmetrical and asymmetrical AC faults, DC fault, sudden load rejection, step changes in current order and gamma order, are presented.

4.2 Initialization of the HVDC system

A systematic procedure is followed for smooth and steady building up of DC link voltage. In practice, this is done either manually (through communication between operators in each station) or automatically.

In case of simulation, the AC system takes about 3 cycles to ramp up to the full steady state value. The converters are blocked for this period to avoid commutation failure(s).

Also, the ability of the DC link to start is a function of the controls and the alpha minimum setting of the inverter. If the alpha minimum of the inverter is set too high (say 120° or more), the inverter may have difficulty commutating from a zero current condition.

In figure 4.1, control characteristic is redrawn. The initial values of the alpha for the rectifier and the inverter are set to 85° and 110°, respectively. These settings help the DC link voltage and current start from a very low value. On V_{dc}-I_{dc} plane (figure 4.1),the

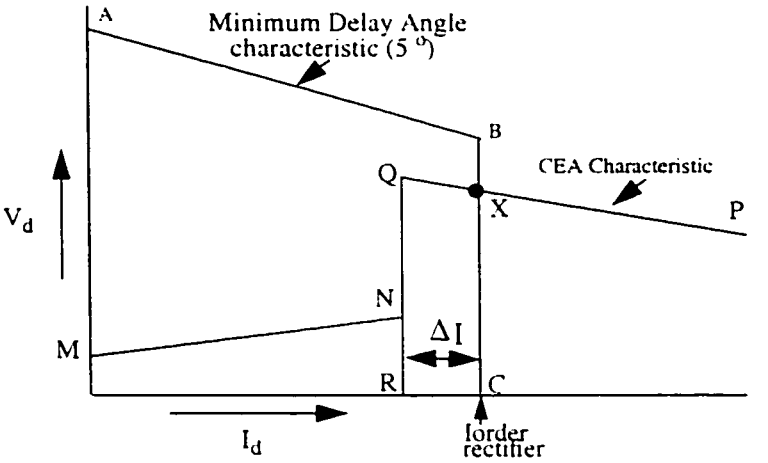


Figure 4.1 : Characteristics on V_{dc}-I_{dc} plane to explain initialization of an HVDC system

operating point follows the alpha-min-in-inverter characteristic (line MN) until it reaches the inverter constant current characteristic (line QR). During this period, the rectifier side alpha decreases. The firing angles of both the rectifier and the inverter vary simultaneously during the constant current operation of the inverter until the point Q on CEA characteristic is reached. A switch-over from the inverter cur

rent controller to the rectifier current controller takes place and the steady state operating point X is reached.

4.3 Controller Tests

The three controllers which control the operation of HVDC system are

1. Rectifier current controller
2. Inverter current controller
3. Inverter gamma controller

Each controller is optimized individually by applying small signal disturbances to the respective controller as follows.

1. Step change in rectifier current order
2. Step change in inverter current order
3. Step change in inverter gamma order

4.3.1 Step Change in the Rectifier Current Order

A step of 0.1 p.u. in current order is applied at t=0.5 s. The order is kept at 0.9 p.u. for a duration of 200 ms. The step is withdrawn at t=0.7 s and original current order is restored. To avoid any interaction from the inverter current controller, a sufficient current margin (CM), of the order of 0.2 p.u. is set temporarily; this has the impact of biasing off the inverter controller. Responses of the rectifier current controller for all configurations such as LCC, CCC, HCC-UP and HCC-LO are shown in figures 4.2 through 4.5. It is observed that the responses are well controlled and stable. Also, from the traces of the alpha orders, it is evident that the direct current is controlled by the rectifier current controller by varying the alpha order rectifier (AOr) where as the alpha order inverter (AOi) stays at the same value indicating that the inverter current controller plays no role in controlling the current.

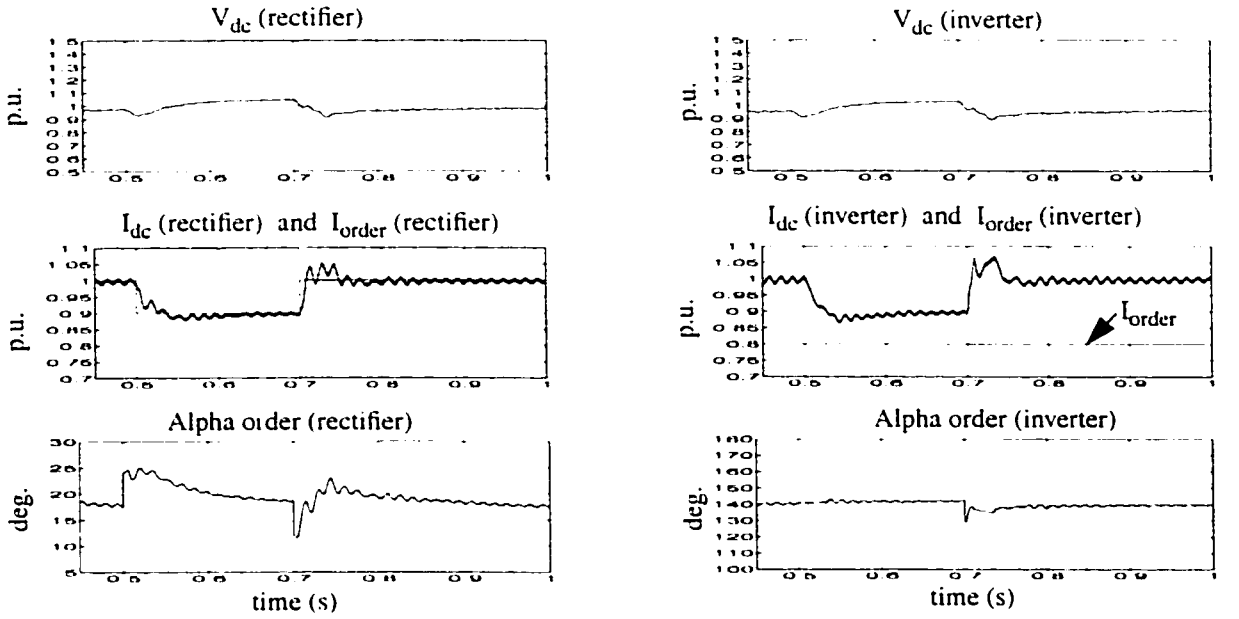


Figure 4.2 : 10% step change in the rectifier current order - LCC configuration

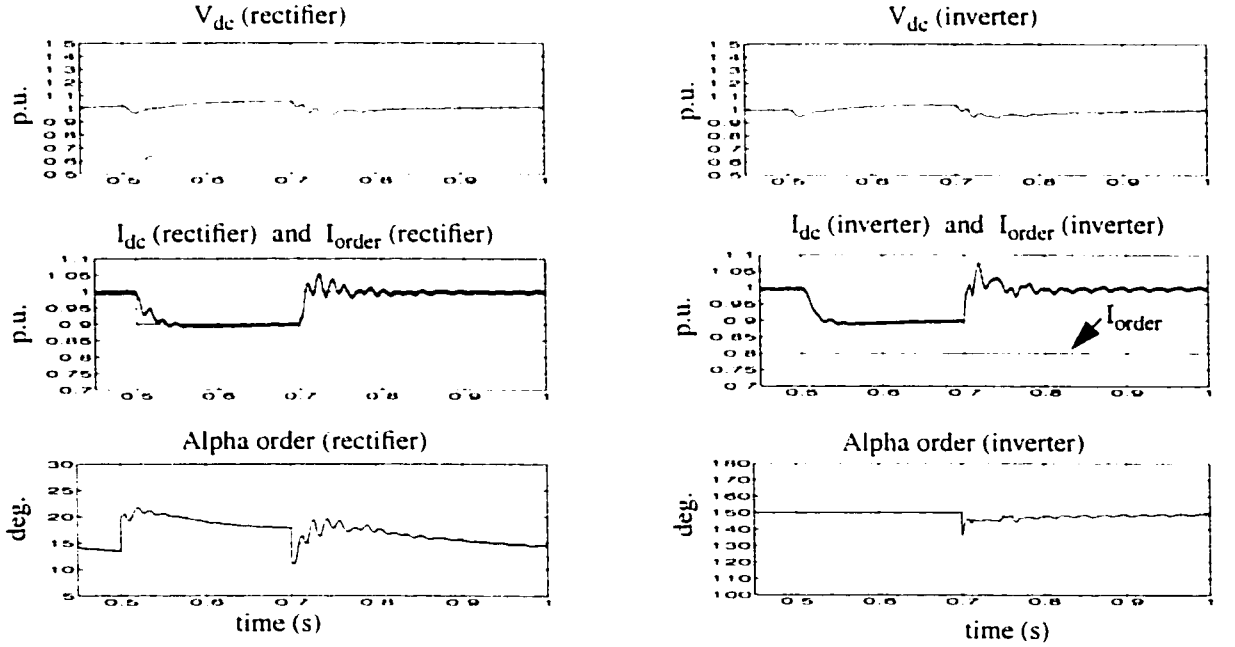


Figure 4.3 :10% step change in the rectifier current order - CCC configuration

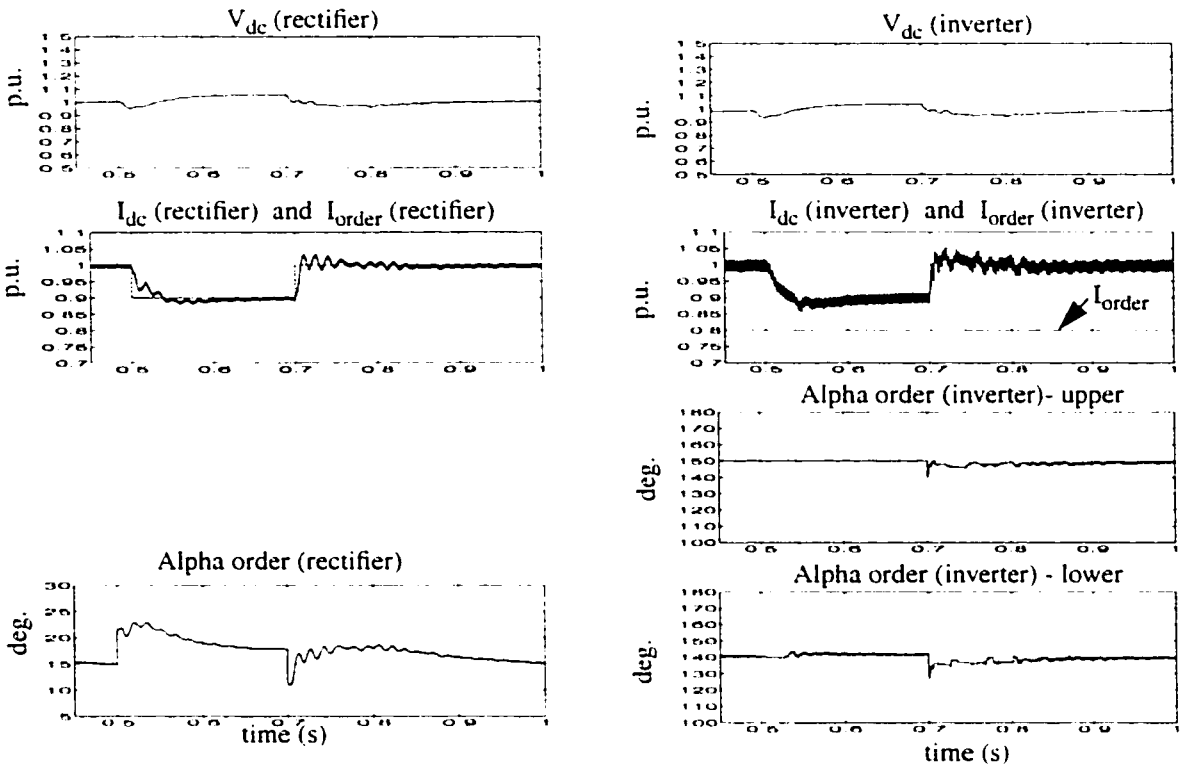


Figure 4.4 : 10% step change in the rectifier current order - HCC-UP configuration

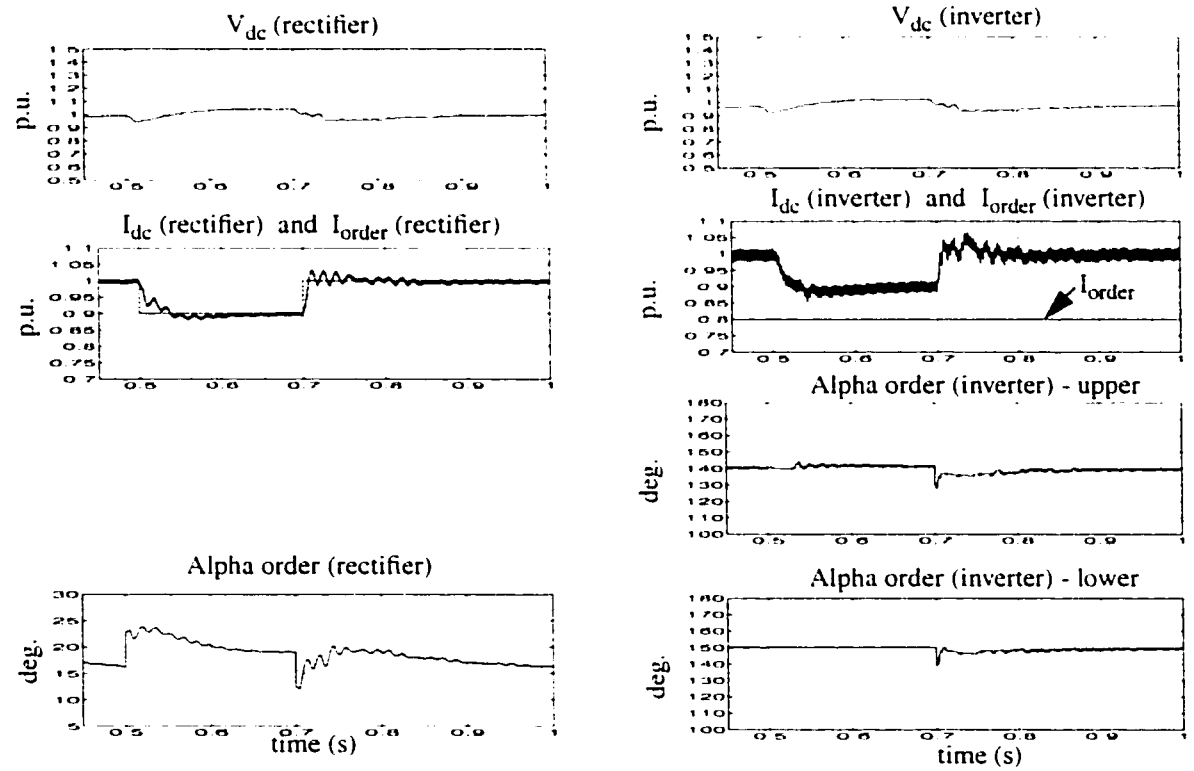


Figure 4.5 :10% step change in the rectifier current order - HCC-LO configuration

4.3.2 Step Change in the Inverter Current Order

A similar step as mentioned in section 4.3.1 is applied to the current order after restoring the CM to its normal value of 0.1 p.u. To bring the inverter current controller in operation, rectifier side AC voltage is brought down to 0.9 p.u. of rated value and this brings down the value of the alpha order rectifier to its lower limit (=5°). Different parameters such as V_{dc}, I_{dc}, alpha order rectifier and alpha order inverter are monitored and results with different configurations such as LCC, CCC, HCC-UP and HCC-LO are shown in figures 4.6 through 4.9. It is observed that the responses are well controlled and stable. Also, the steady state values are attained within a very short period of time (50 ms). From the response of the alpha order inverter it can be concluded that the control of I_{dc} is carried out by the inverter current controller only since the alpha order rectifier stays at its lower limit signifying that the rectifier current controller has lost its control over the current.

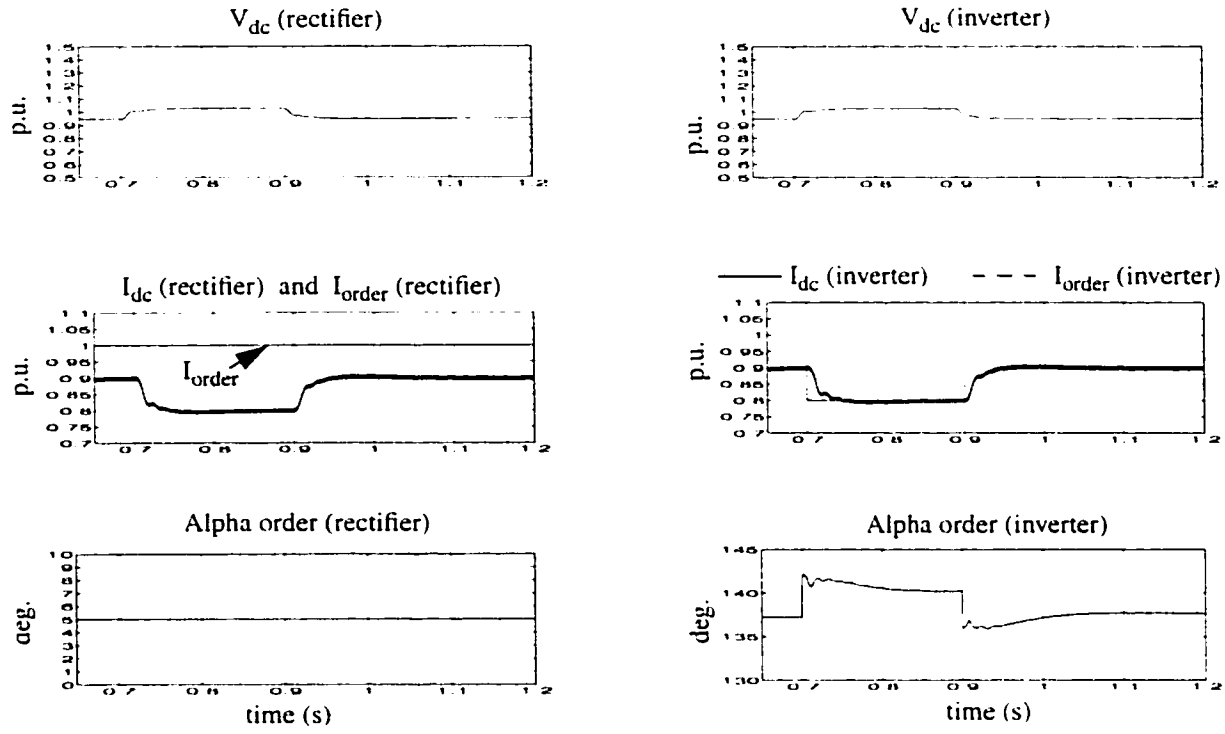


Figure 4.6 : 10% Step change in the inverter current order - LCC configuration

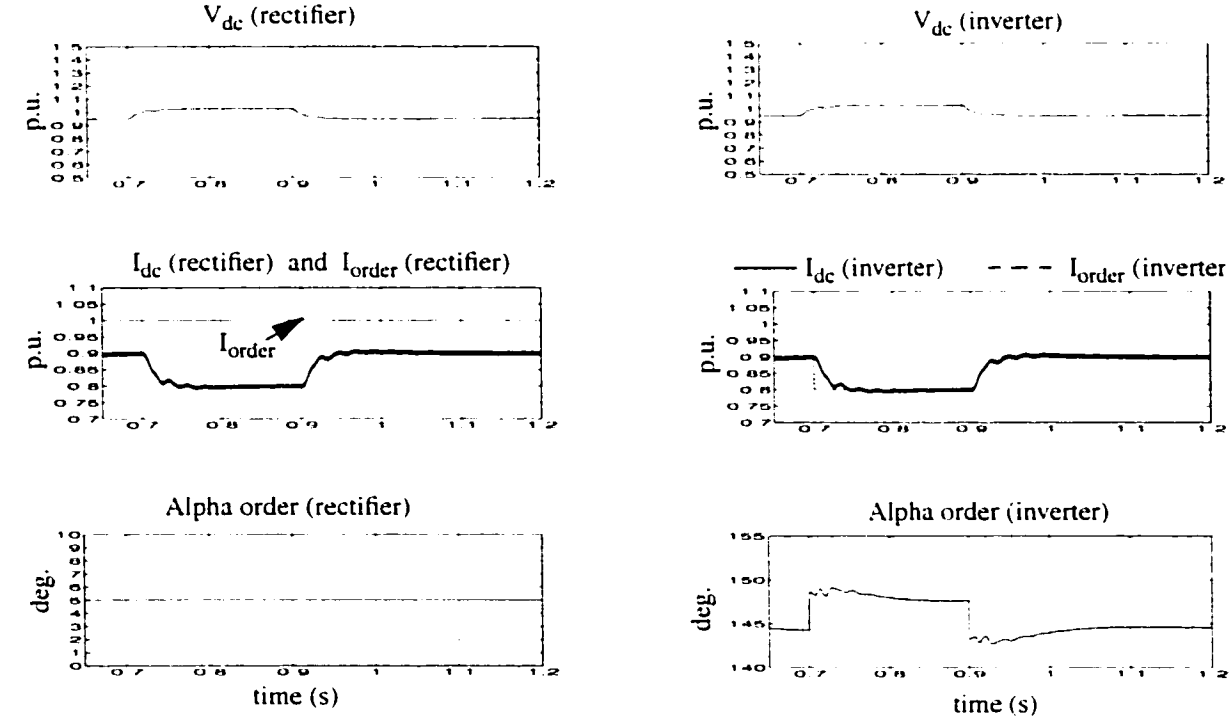


Figure 4.7 : 10% Step change in the inverter current order - CCC configuration

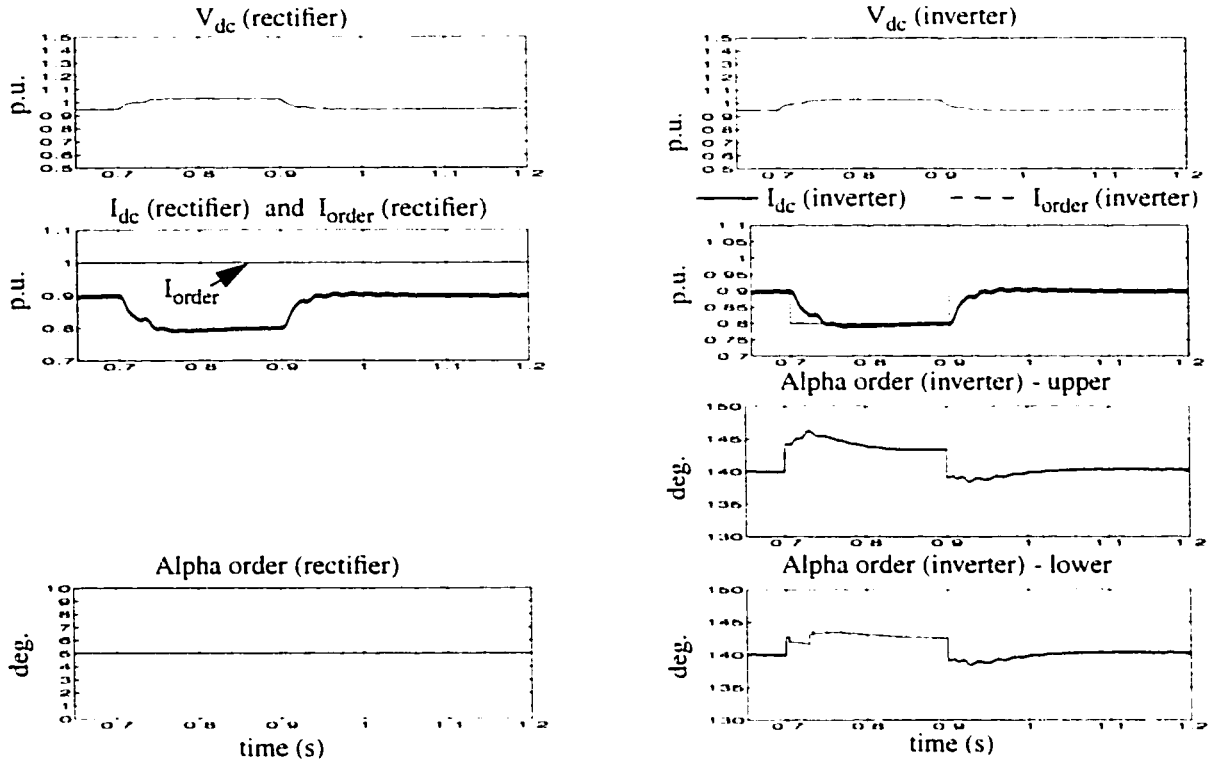


Figure 4.8 : 10% step change in the inverter current order - HCC-UP configuration

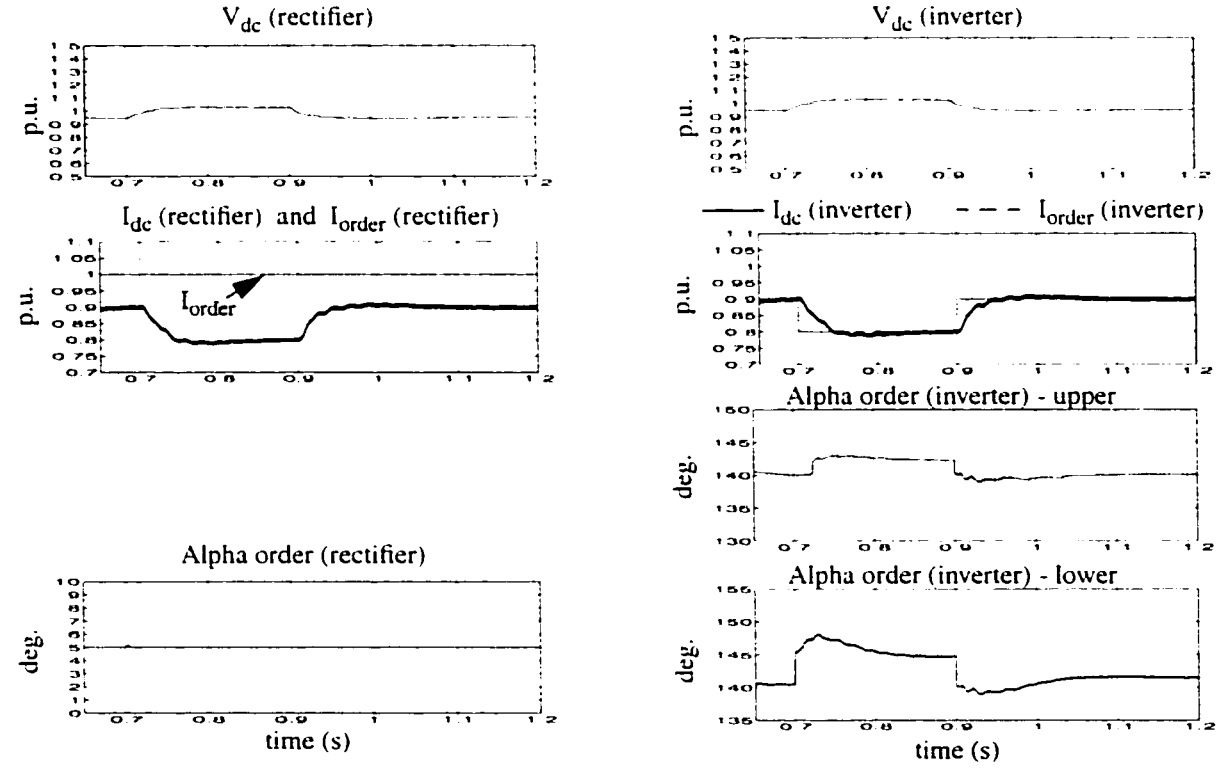
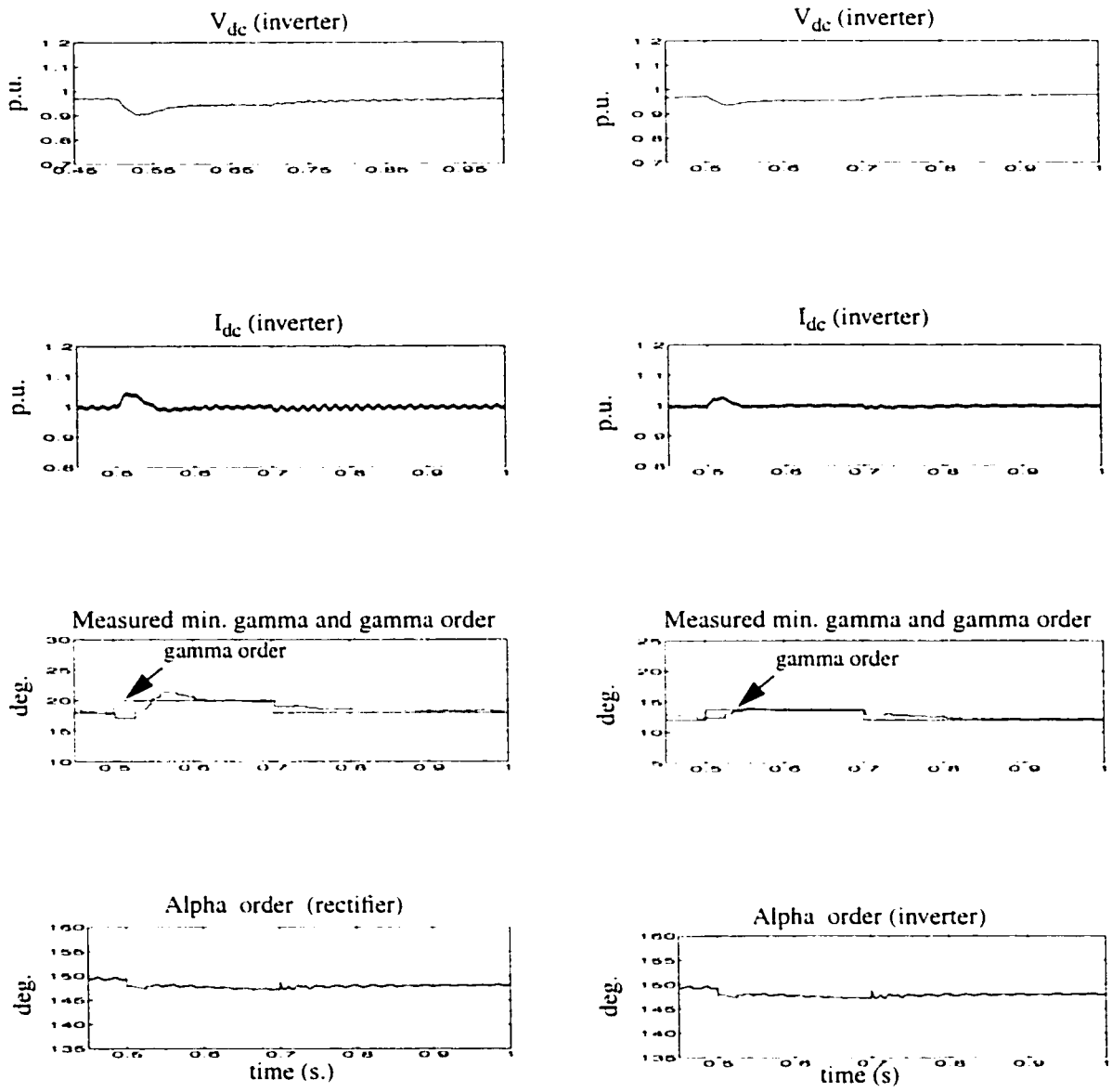


Figure 4.9 : 10% step change in the inverter current order - HCC-LO configuration

4.3.3 Step Change in the Inverter Gamma Order

A step change of 2° is applied to gamma order (GO) at t=0.5 s and withdrawn at t=0.7 s. In case of LCC and CCC configurations, operating point of the gamma is same for both the upper and the lower inverter. Hence, a single gamma controller is used. But in case of HCC-UP and HCC-LO configurations, operating point of gamma is different for the upper and the lower inverters. So, two separate gamma controllers are used. In later cases, step change is applied only to one controller at a time. Different parameters such as V_{dc}, I_{dc}, measured minimum gamma, alpha order rectifier and alpha order inverter are monitored. Results are shown in figures 4.10 through 4.12. It is observed that the responses are well controlled and stable with average time of response varying between 50 ms to 100 ms depending on the configuration of the converter.



LCC configuration

CCC configuration

Figure 4.10 : 2 deg. step change in the inverter gamma order- LCC and CCC configurations

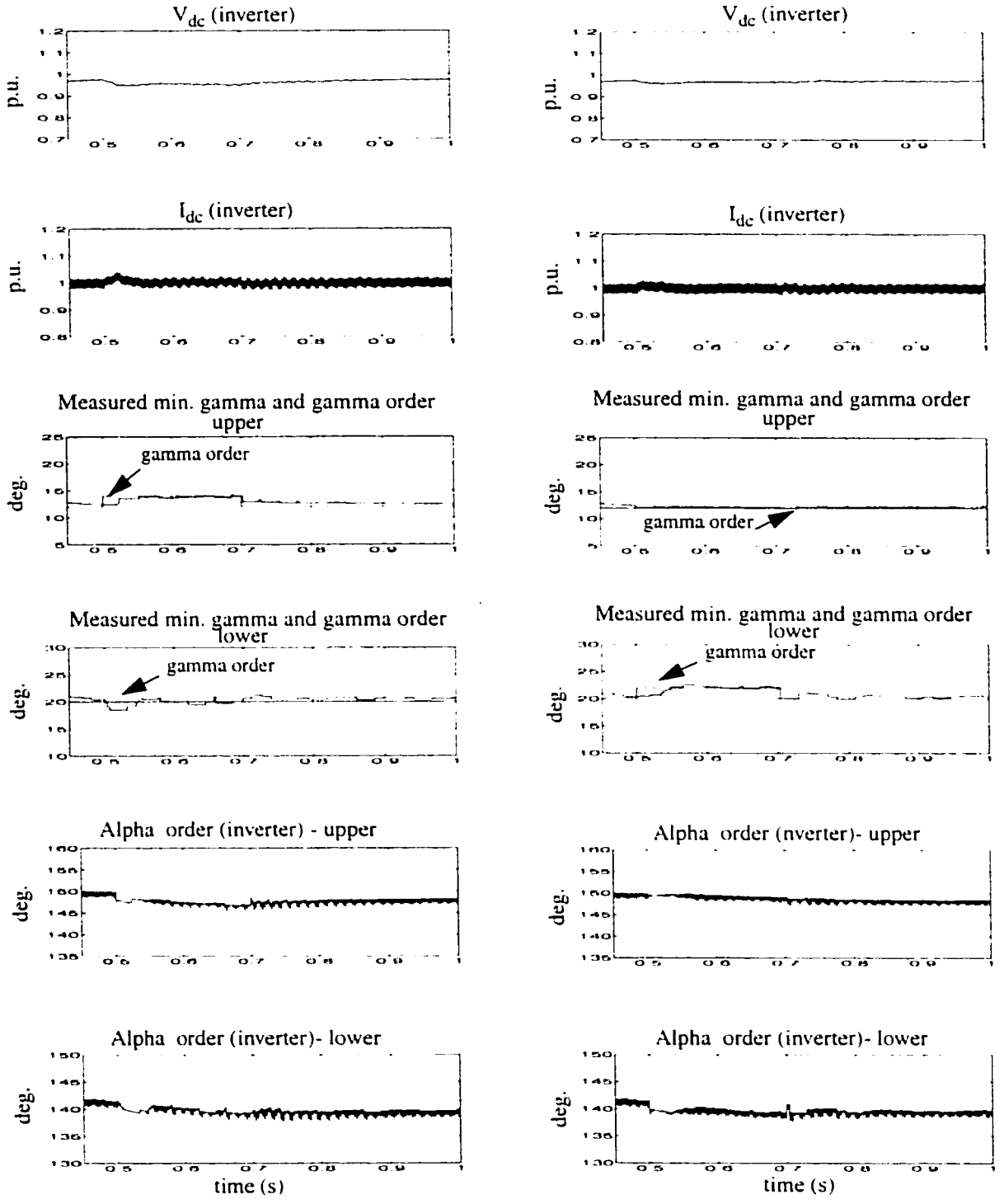


Figure 4.11 : 2 deg. step change in the inverter gamma order - HCC-UP configuration

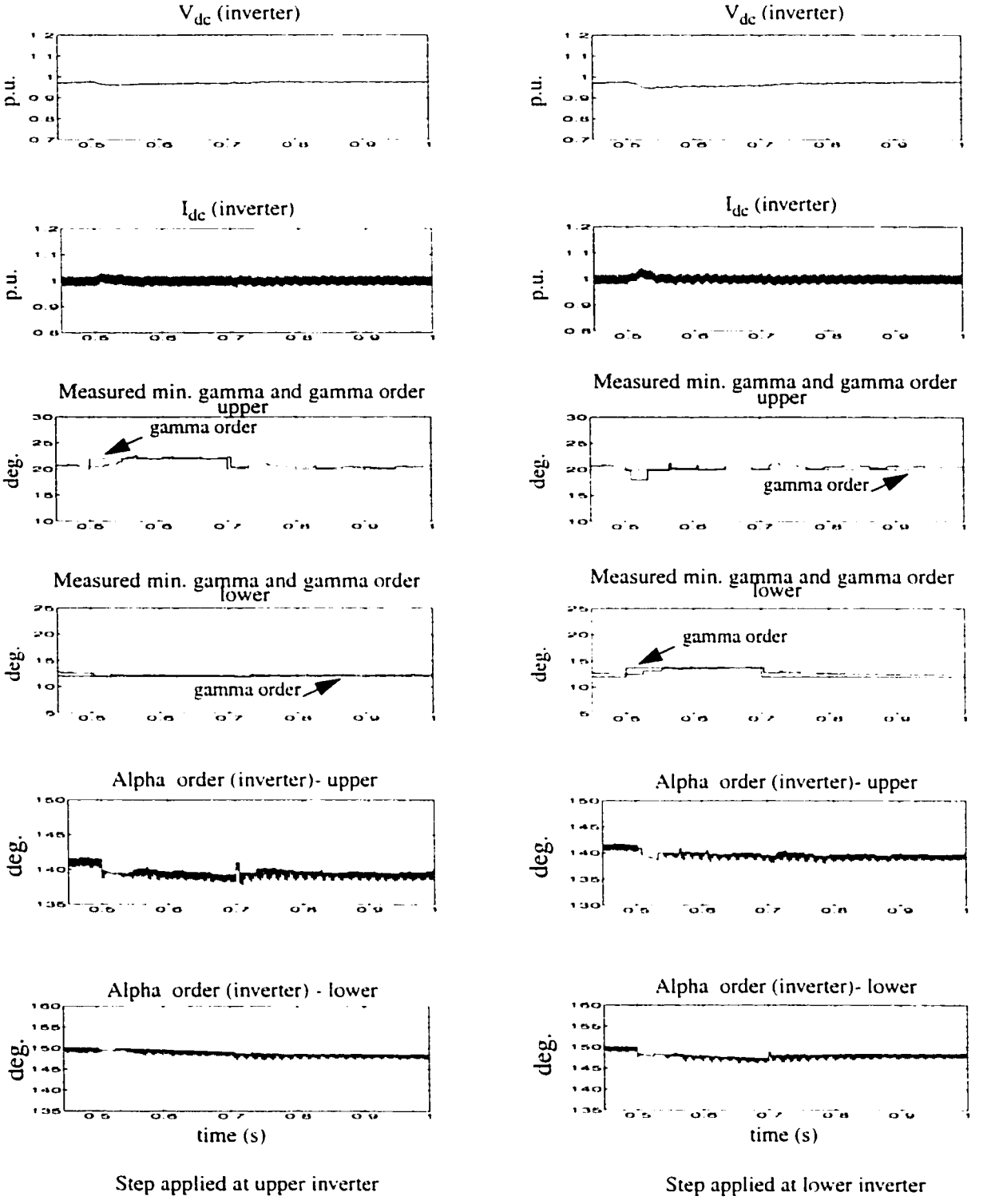


Figure 4.12 : 2 deg. step change in the inverter gamma order - HCC-LO configuration

4.4 Mode Shift Test

It has already been discussed in Chapter 2 that the converter station at the inverter side of an HVDC system is also provided with a current controller. This controller comes into action only when the rectifier side current controller loses its control after attaining the lower limit of the AOr (=5°).Under this situation control mode shifts from the rectifier current control to the inverter current control. This shifting of control helps the HVDC system maintain the power flow close to 90% of the rated power and avoid a complete interruption.

The mode shift test is, therefore, an important test to verify the above feature. Results of the mode shift test are shown in figures 4.13 through 4.16.

With normal operating conditions (i.e. V_{dc}, I_{dc} = 1 p.u. and AOr = 15°), at t=0.7 s, AC side voltage of the rectifier is reduced by approximately 10%. This reduction of voltage is sufficient to push the AOr to its minimum limit (=5°). Under this situation rectifier current controller loses its control and the I_{dc} is maintained at 0.9 p.u. by the inverter current controller. At t=0.9 s, a step of 0.1 p.u. is applied to the current order. The I_{dc} falls to 0.8 p.u. as expected. The AOr remains at its minimum value signifying its loss of control over the current. At t= 1.1 sec., the step is withdrawn and I_{dc} rises to 0.9 p.u. Finally, at t=1.3 s, rectifier side AC voltage is brought back to 1 p.u. Another transition in the mode of control takes place. This time it is from inverter current controller to the rectifier current controller. The original operating conditions are regained.

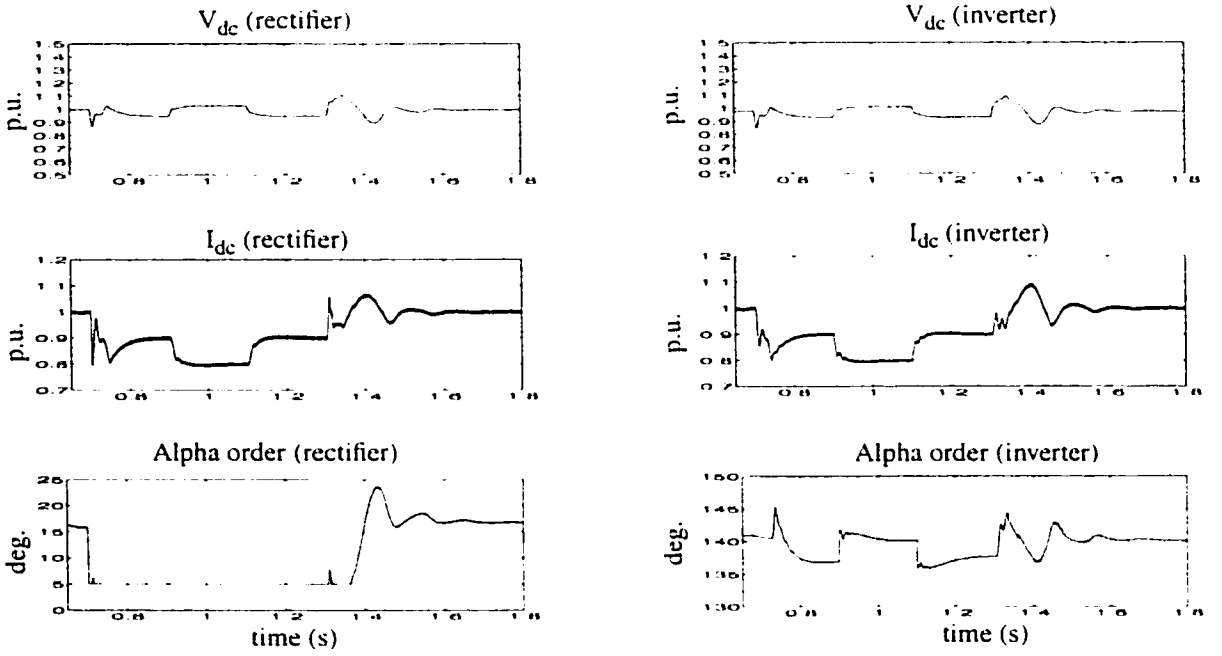


Figure 4.13 : Mode shift test - LCC configuration

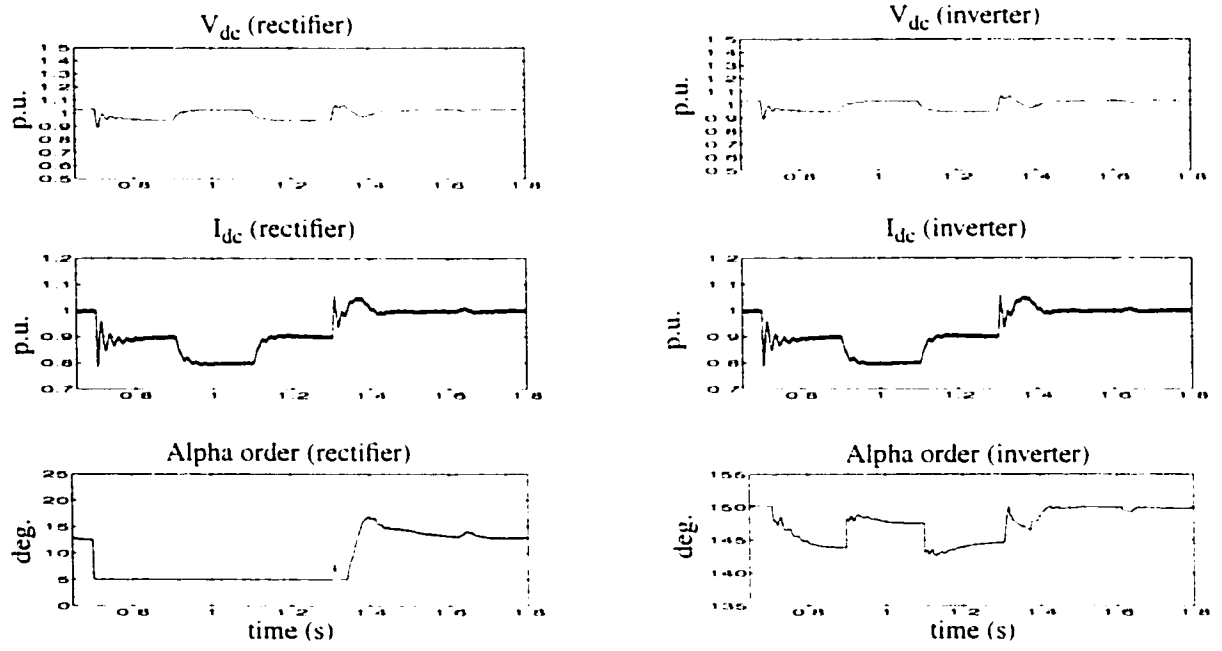


Figure 4.14 : Mode shift test - CCC configuration

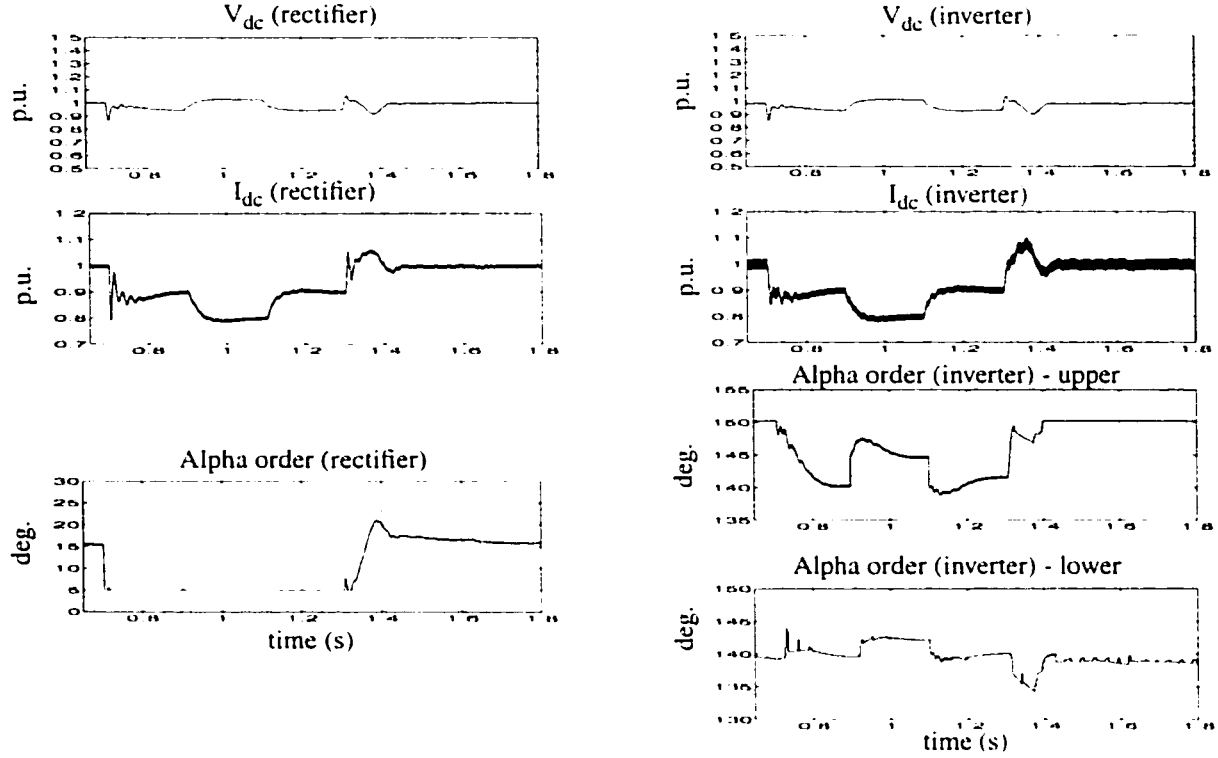


Figure 4.15 : Mode shift test - HCC-UP configuration

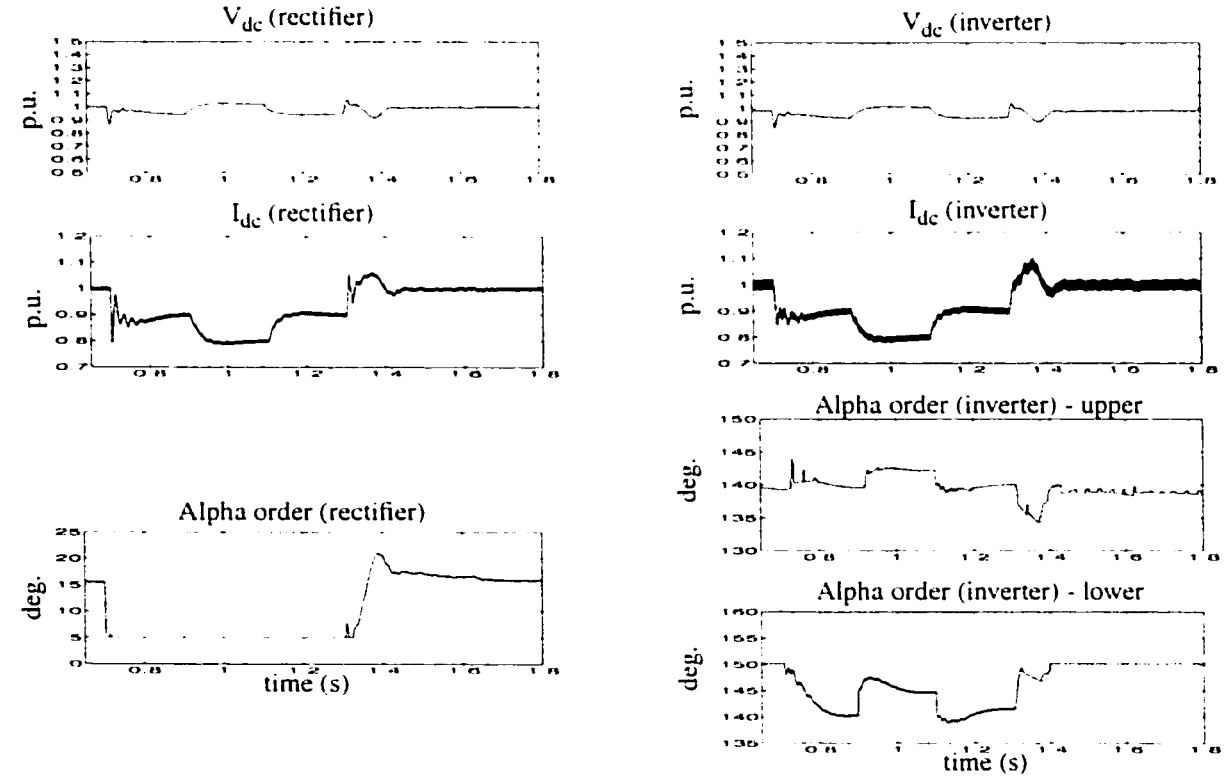


Figure 4.16 : Mode shift test - HCC-LO configuration

4.5 Fault Tests

In the following sections results of various fault tests conducted on HVDC system with different converter configurations are presented and discussed.

4.5.1 Remote Three Phase Fault on AC Network of the Inverter

A three phase symmetrical fault is typically the most severe fault that occurs in AC networks. A remote 5 cycle fault is initiated at t=0.5 s in such a way that it causes a 20% dip in the AC bus voltage (V_{bus}). The behaviour of certain parameters such as V_{dc}, I_{dc}, AO and bus phase voltages (V_a,V_b and V_c) are monitored and results are shown in figures 4.17 through 4.20. It is observed that the behaviour of V_{dc} for the LCC configuration is distinctly different from that of the other configurations. The V_{dc} for this case collapses and attains negative value of -0.5 p.u. during the fault. This indicates that the conventional converter has experienced the commutation failure. But the traces of V_{dc} for the other configurations CCC, HCC-UP and HCC-LO, indicate that these converters have not shown any commutation failure. It is also observed that the direct current shoots up as soon as the fault occurs. Voltage Dependent Current Limiter (VDCL) comes into action immediately to bring this fault current to a very low value (here it is set to 0.3 p.u.) to protect the valves from damage. The action of the VDCL is evident from the trace of I_{dc} as shown in the above mentioned figure. It is also observed that the peak fault current is as high as 2.6 p.u. for the LCC while it is 1.4 p.u. and 1.8 p.u. for the CCC and HCC (UP and LO) respectively. The lower value of peak fault current in CCC and HCC (UP and LO) may be due to the presence of the commutation capacitor in the fault path. It is also worth noting that the inverter valves have experienced higher peak fault current as compared to the rectifier

valves. The obvious reason is that during the fault the cable capacitance has discharged through the inverter valves contributing additional current to the fault.

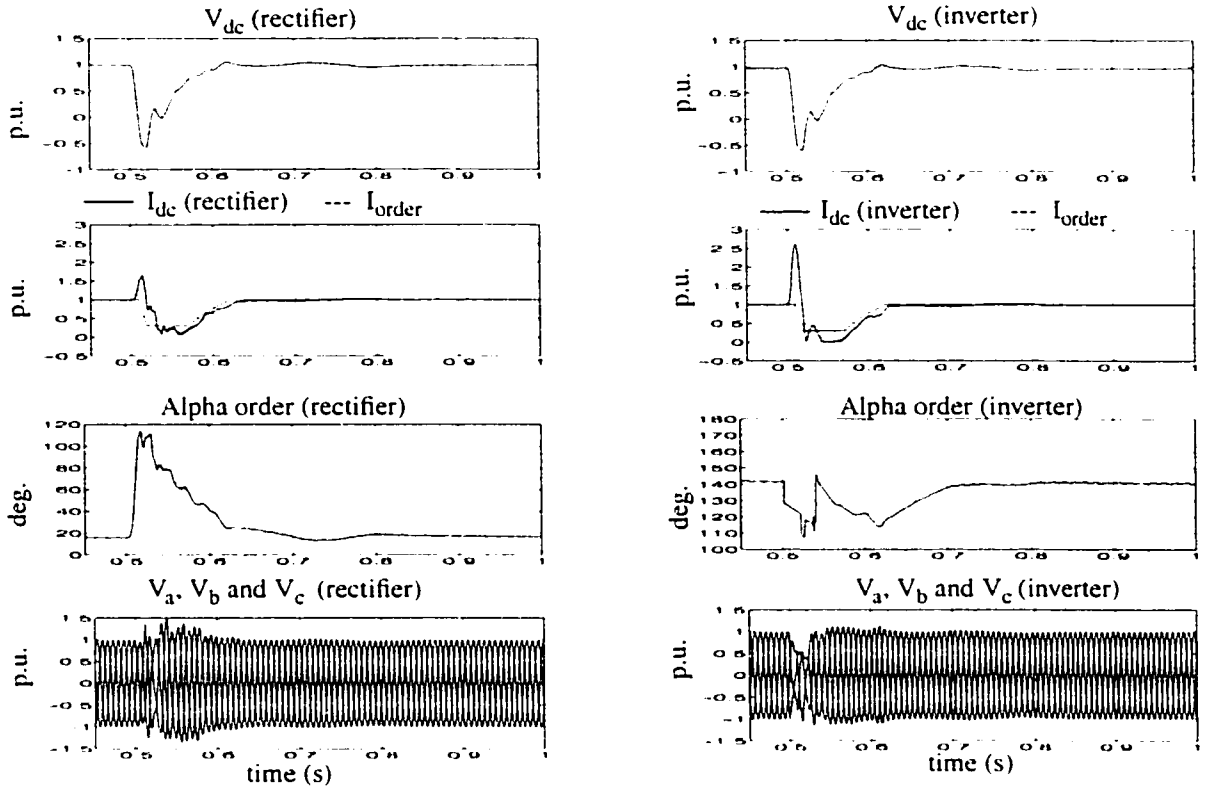


Figure 4.17 : Remote three phase fault at the inverter AC network - LCC configuration

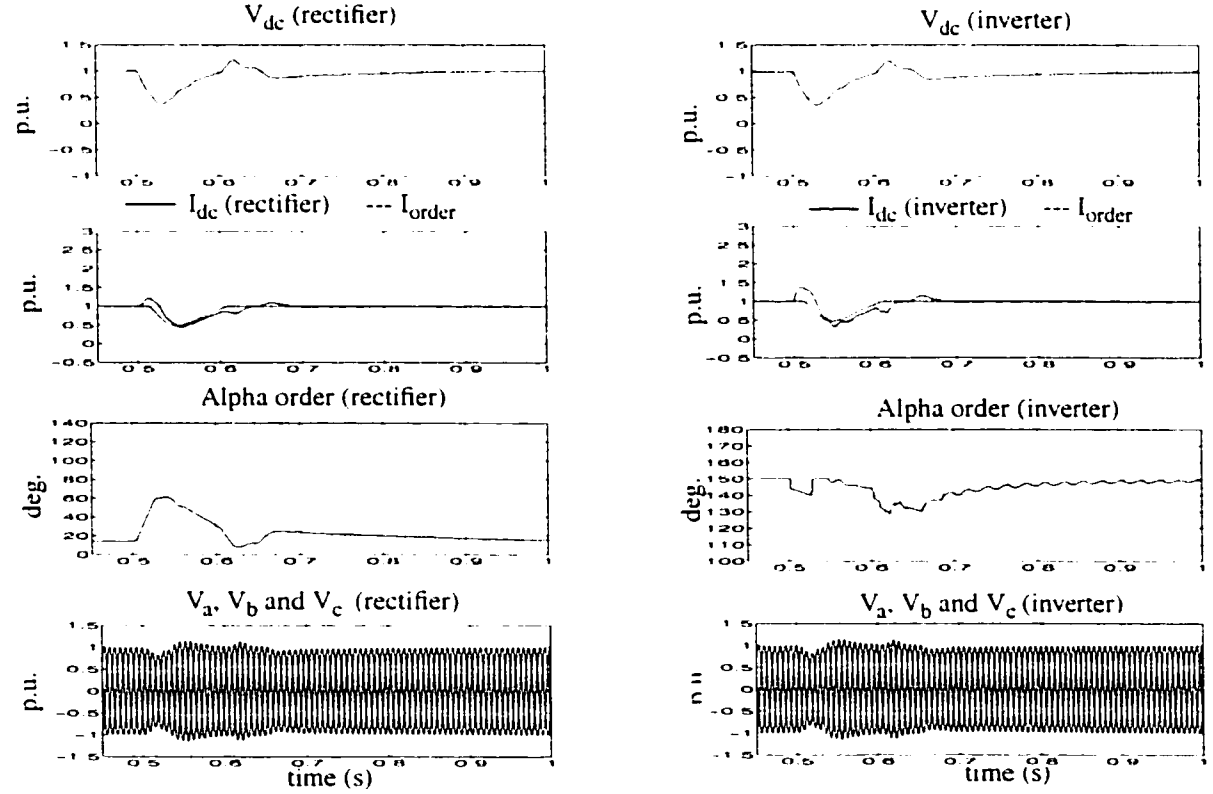


Figure 4.18 : Remote three phase fault at the inverter AC network - CCC configuration

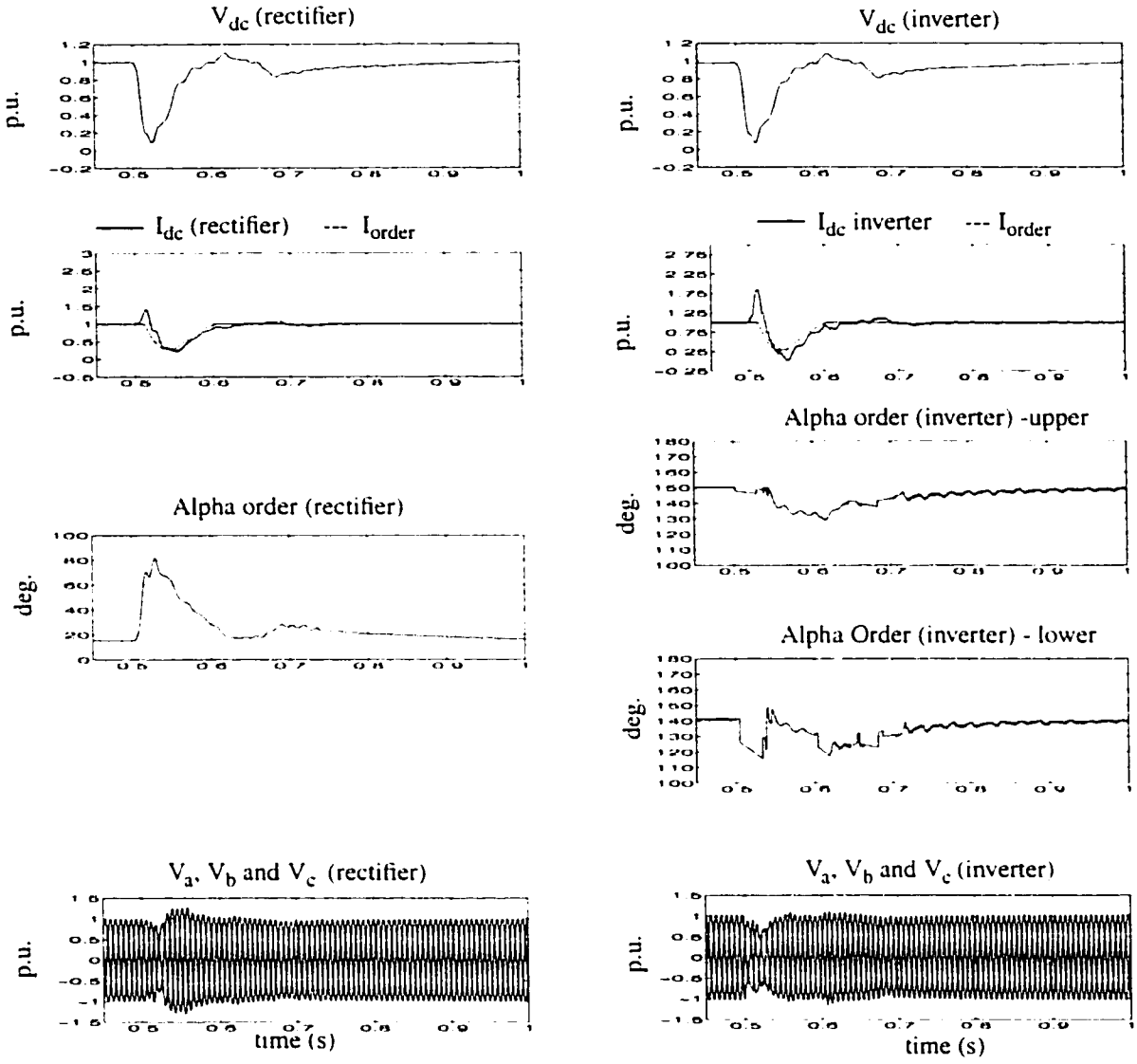


Figure 4.19 : Remote three phase fault at the inverter AC network - HCC-UP configuration

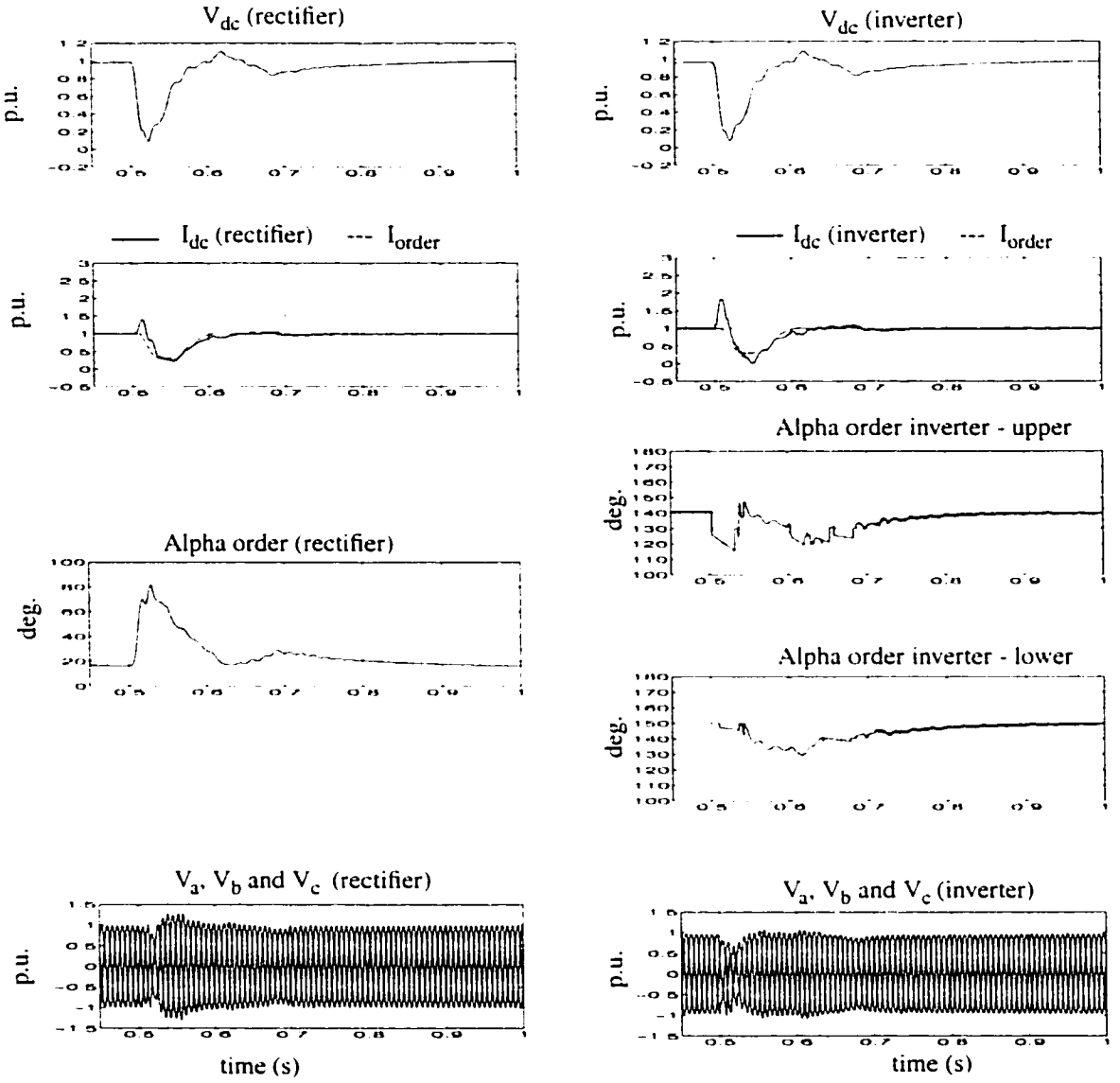


Figure 4.20 : Remote three phase fault at the inverter AC network - HCC-LO configuration

4.5.2 Remote SLG Fault on AC Network of the Inverter

Although the Single Line to Ground (SLG) Fault is not that much more severe in magnitude than a three phase fault, it has different implications on the system because of its asymmetrical nature. Also, in practice, this type of fault occurs more frequently than any other fault. A remote 5 cycle fault is simulated in a similar manner as described in the previous section and the same parameters are monitored. Results are shown in figures 4.21 through 4.24.

As expected, during remote SLG fault, the V_{dc} of respective converter configuration, behaves in a very similar manner as it does during remote three phase fault. This means that conventional converter shows a commutation failure whereas the other types of converters do not. The peak value of the fault current for the conventional converter is of the order of 2 p.u. which is less than that observed during a three phase fault for the same converter configuration. For other converter configurations, the peak fault current is limited within 1.3 p.u. which is less than that of the three phase fault for the respective configurations. Also, I_{dc}, for all the configurations, contains second harmonic component which is the characteristic of such type of fault.

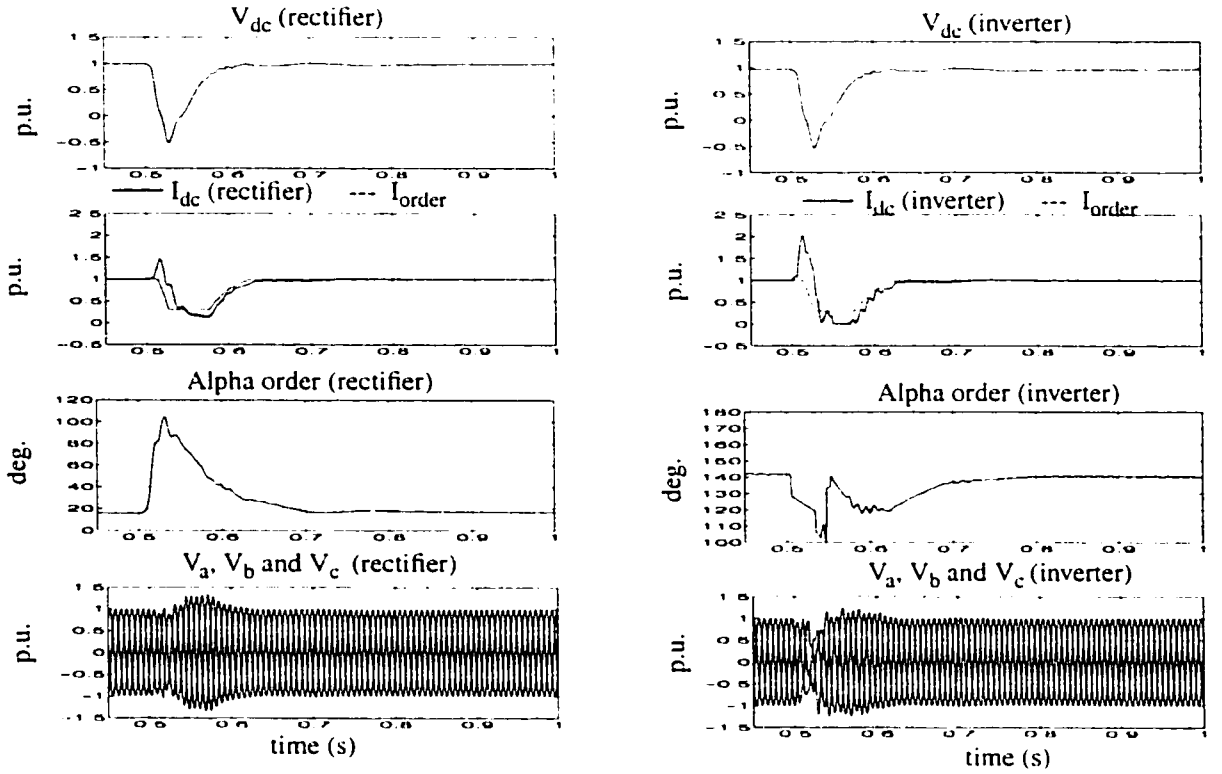


Figure 4.21 : Remote SLG fault at the inverter AC network - LCC configuration

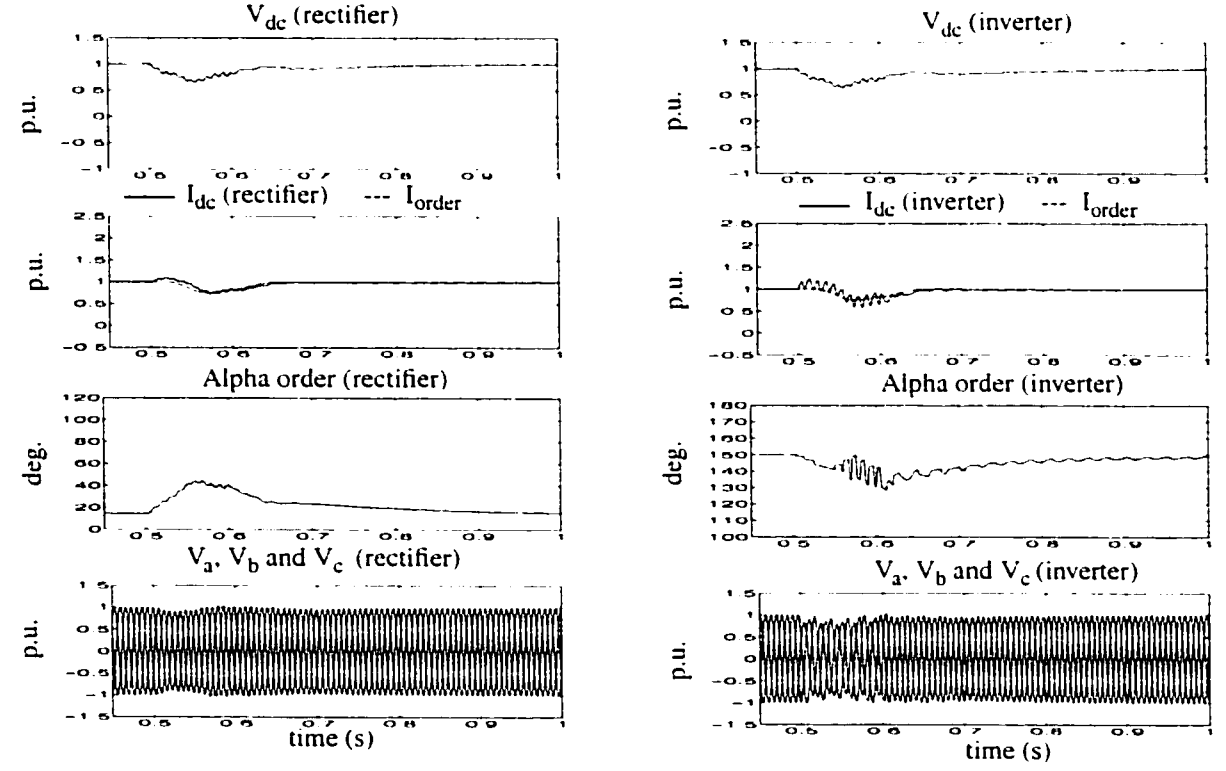


Figure 4.22 : Remote SLG fault at the inverter AC network - CCC configuration

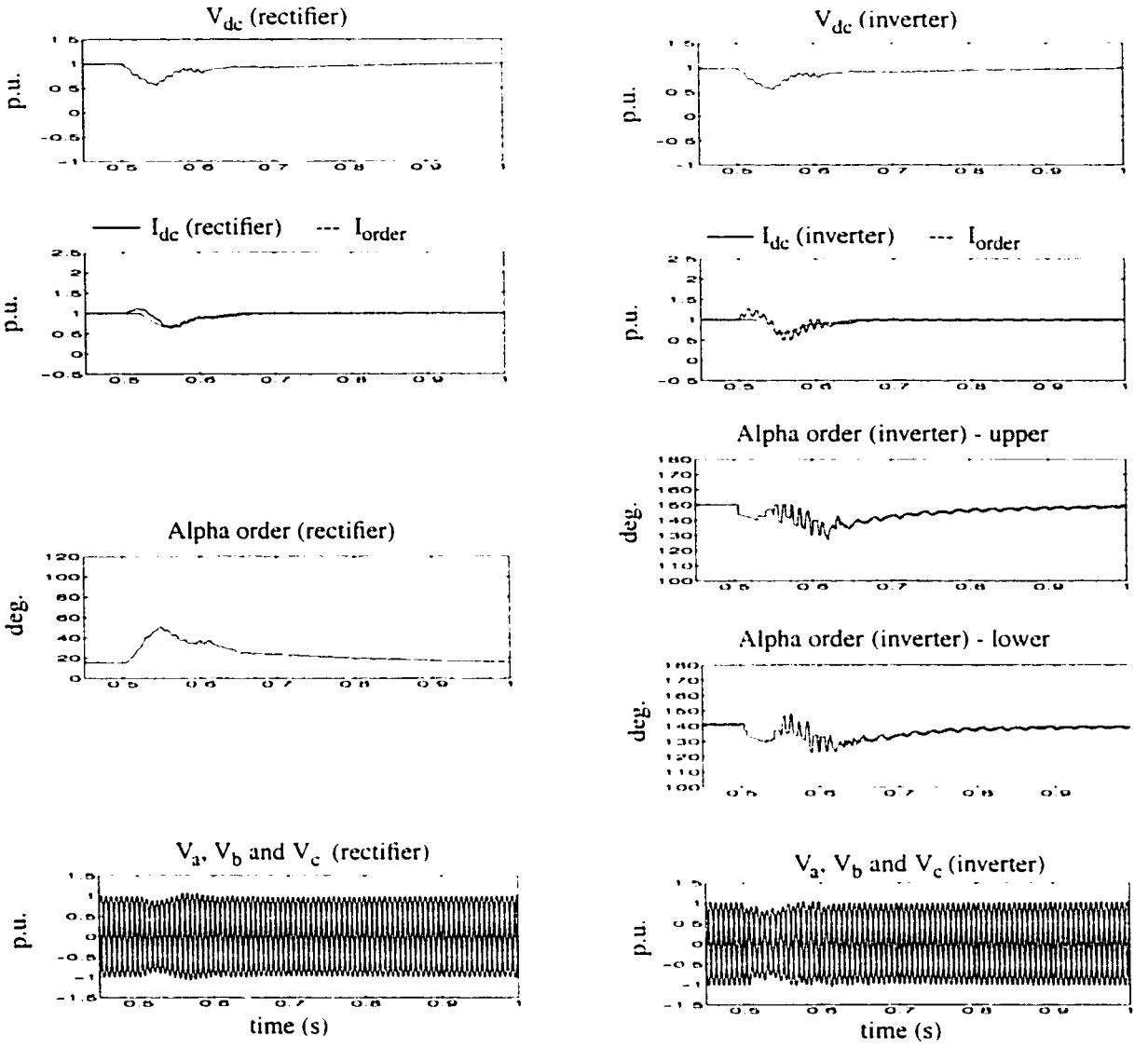


Figure 4.23 : Remote SLG fault at the inverter AC network - HCC-UP configuration

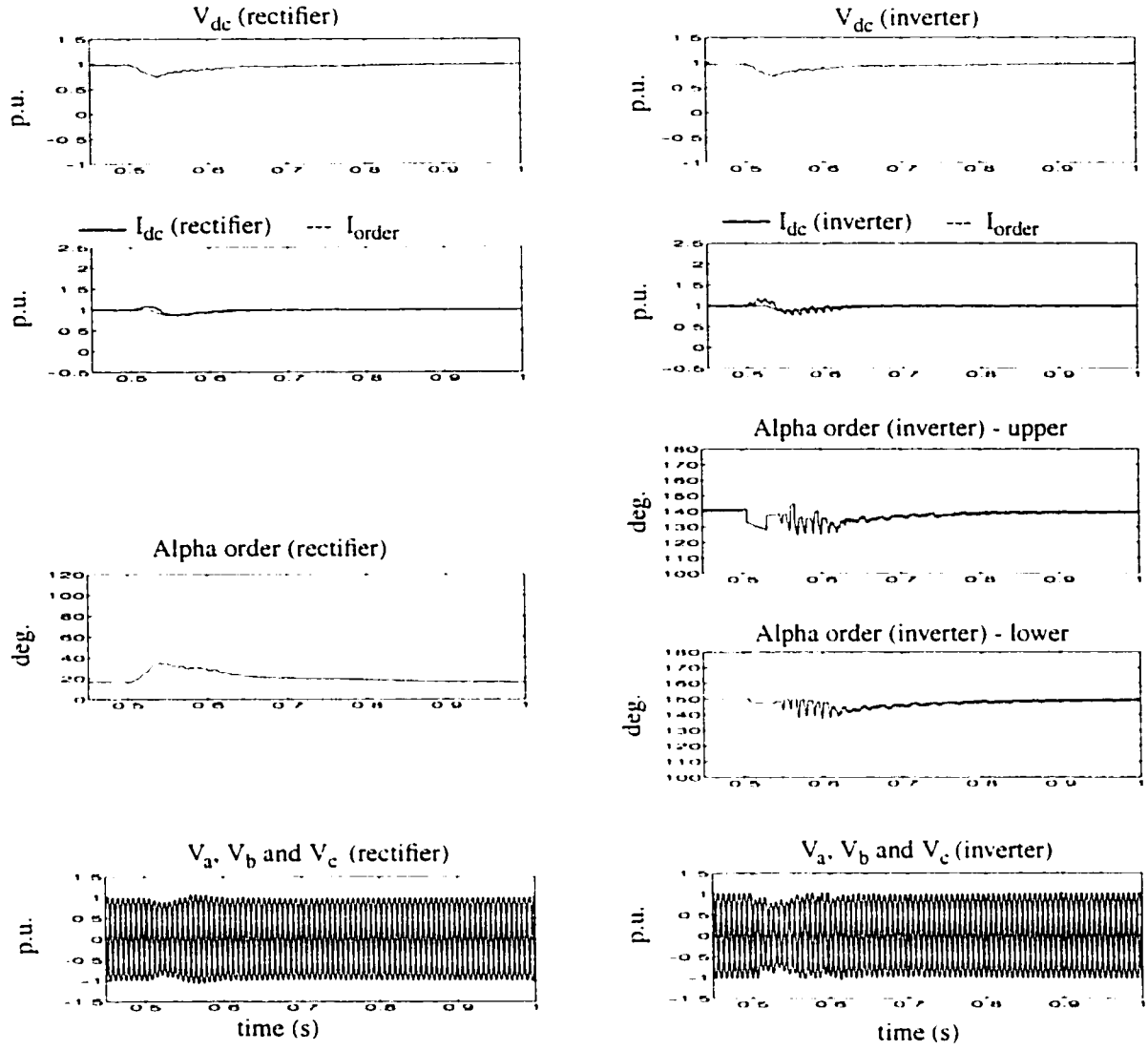


Figure 4.24 : Remote SLG fault at the inverter AC network - HCC-LO configuration

4.5.3 Inverter Side DC Line Fault

A DC line fault is studied to see the dynamic performance of the system during and after the fault. In fact, DC fault is the most severe fault for the converter valves at the rectifier end. A fault is simulated on the inverter side DC line at t =0.5 s. for a duration of more than 3 cycles and same parameters as before are monitored. Results are shown in figures 4.25 through 4.28. During DC fault, the DC voltage collapses. The current through the converter valves at the rectifier end rises to 1.75 p.u. instantly. The current through the valves of the converters at the other end is zero because of the location of the fault. During the fault the VDCL plays a similar role as described in section 4.5.1.

Furthermore, a special action namely Force Retard (FR) action has been initiated. The FR action increases the delay angle of the rectifier valves to 150 deg. This causes the rectifier to operate as an inverter. This FR action helps extinguish the current in the DC line quickly. This action persists until the DC fault is cleared. The system achieves smooth recovery of voltage and current after the fault is cleared. The action of the VDCL and the force retard action can be observed clearly from the trace of the inverter I_{dc}. Also, behaviour of V_{dc}, I_{dc}, AO etc. are identical for all the configurations LCC, CCC, HCC-UP or HCC-LO. This is due to the fact that circuit conditions during DC fault remain same for all the converter configurations.

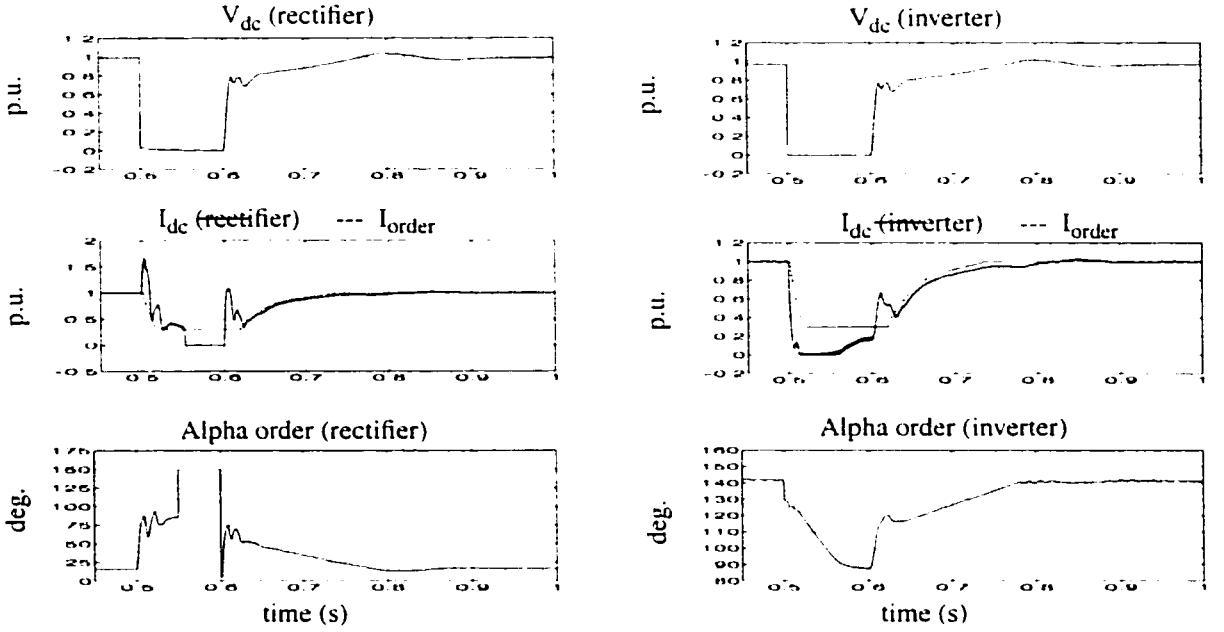


Figure 4.25 : Inverter side DC line faullt - LCC configuration

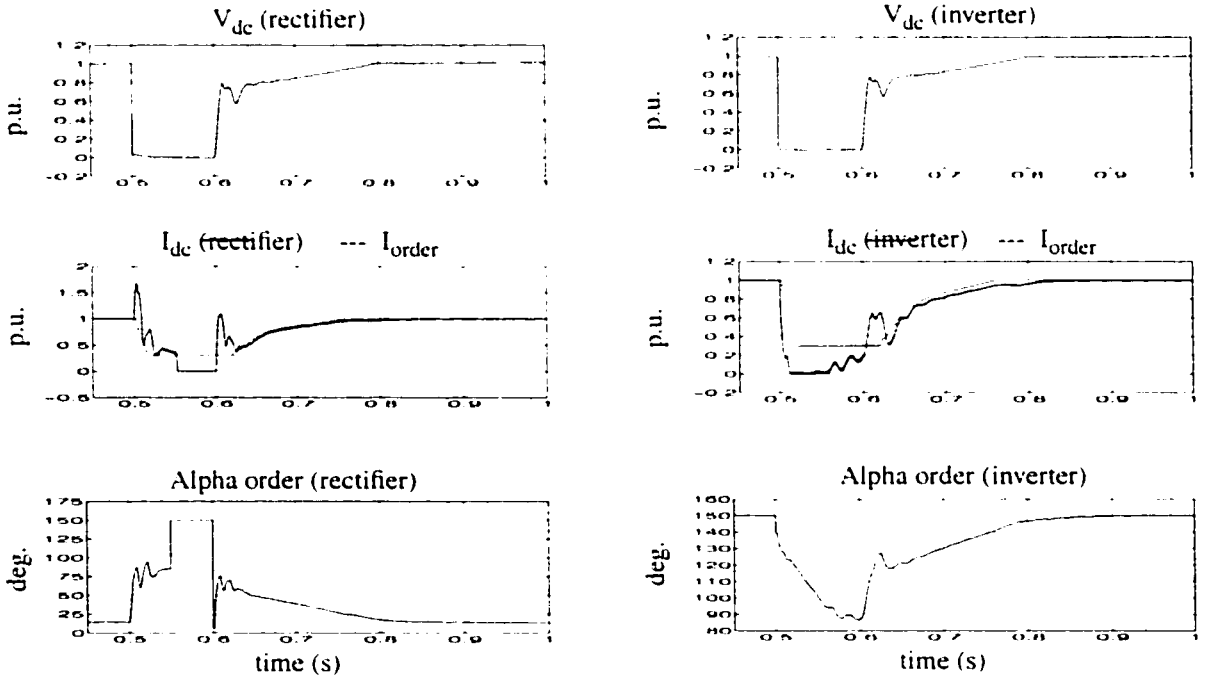


Figure 4.26 : Inverter side DC line fault - CCC configuration

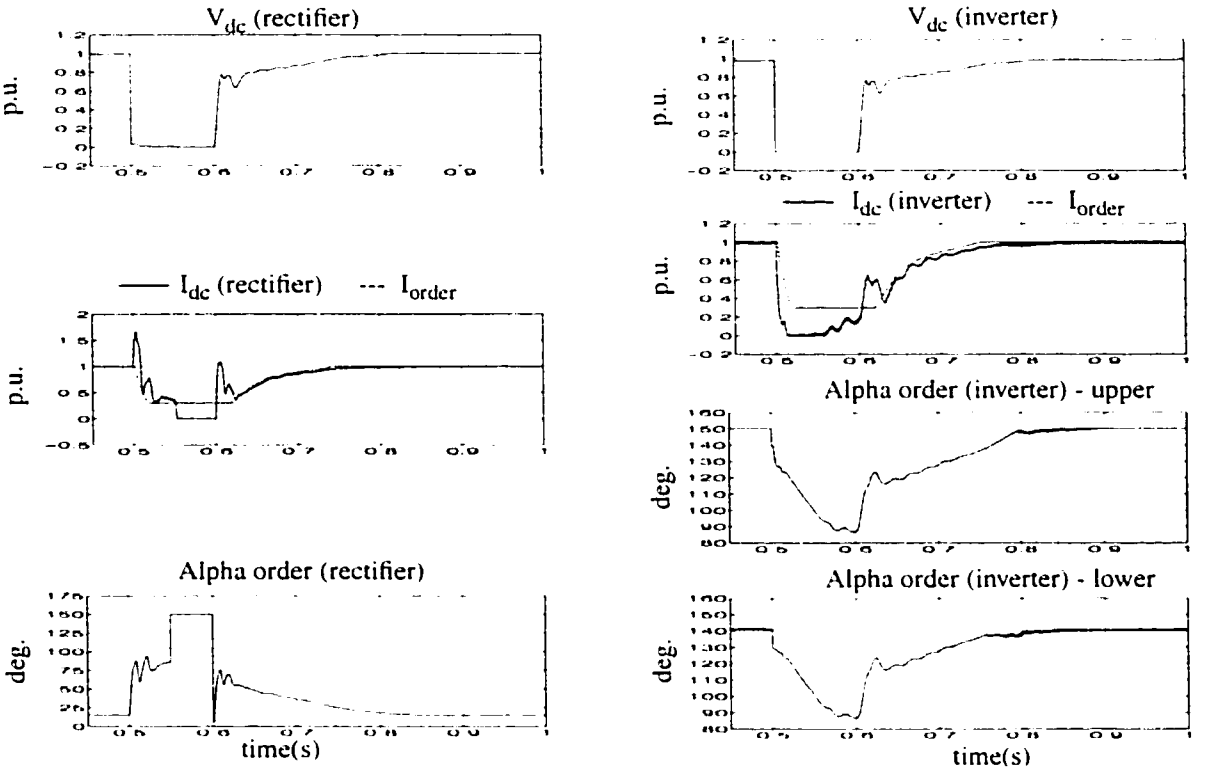


Figure 4.27 : Inverter side DC line fault - HCC-UP configuration

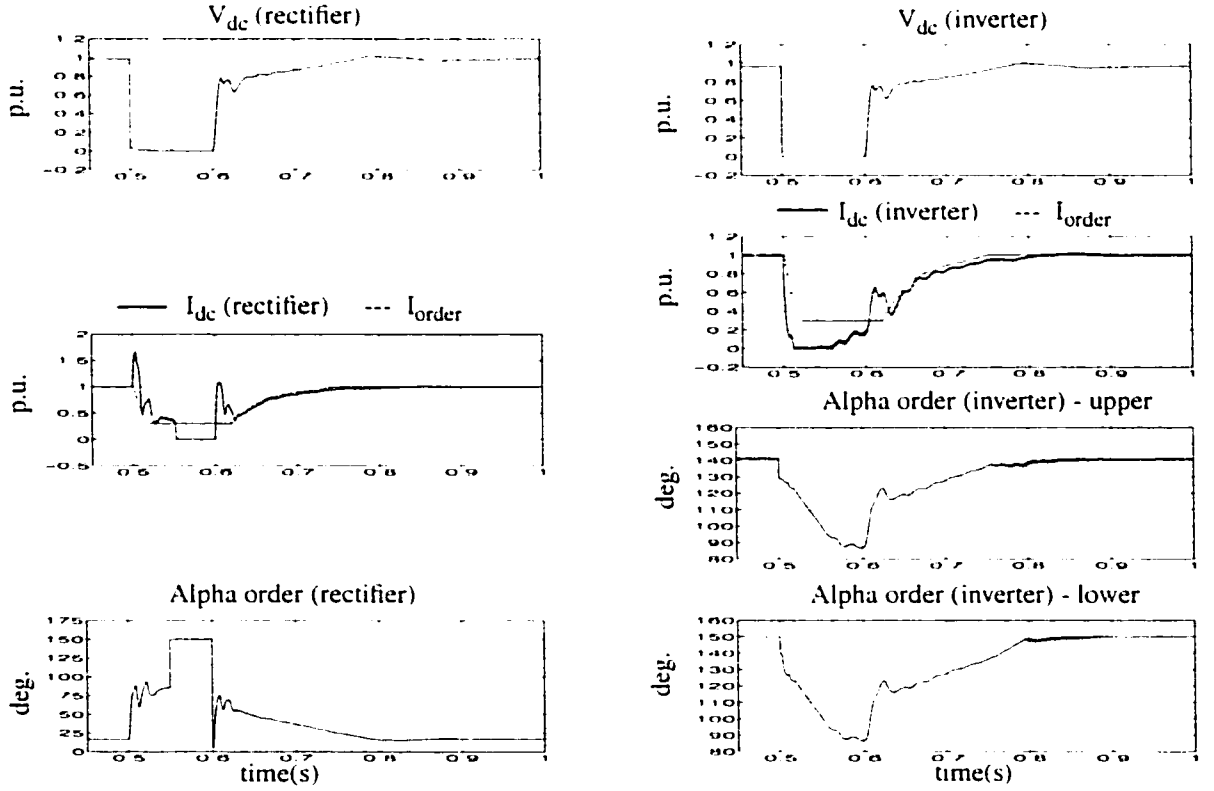


Figure 4.28 : Inverter side DC line fault - HCC-LO configuration

4.6 Load Rejection Over-voltage

This test is carried out to see the system behaviour under sudden load rejection. Under normal operating condition, each converter station consumes reactive power of the order of 55-60% of rated DC power. This reactive power is supplied by means of the shunt capacitors and the filter banks. Sudden load rejection causes interruption of the power flow and this results momentarily in over compensated AC systems at both ends of the DC system because of a lack of demand of reactive power. In the test simulation here, this condition is created by blocking firing signals to the rectifier valves at the instant t = 0.5 s. AC voltages on both sides are monitored. The results are shown in figure 4.29. The results show that the conventional system has the maximum load rejection over-voltage and the CCC system has the least. This is predictable since the conventional system gets the most reactive power and the CCC system gets the least reactive power from the commutation bus. Again it is worth noting that the load rejection over-voltages at the rectifier bus remain the same for all the configurations because of same reactive power supplied by the bus.

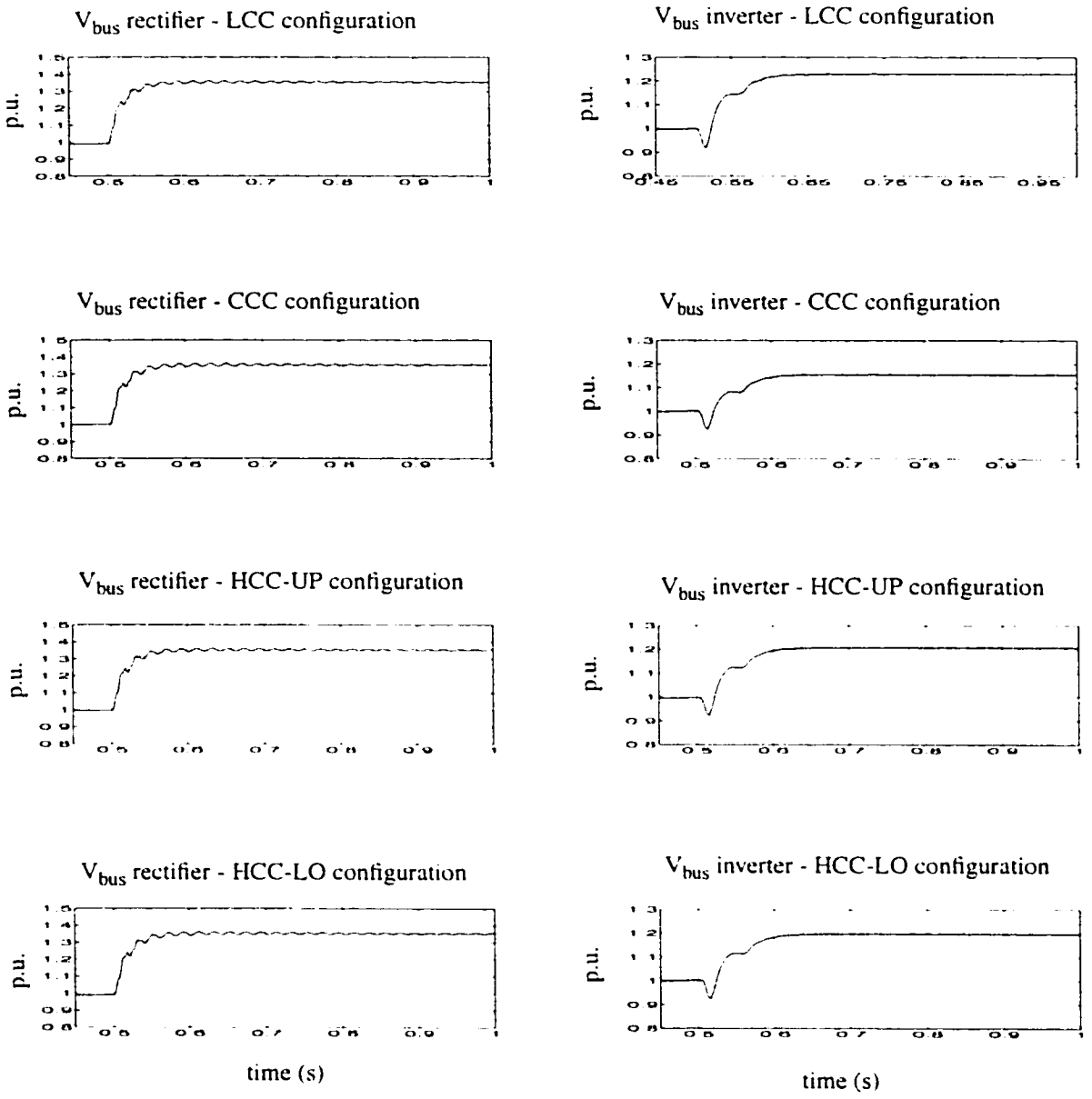


Figure 4.29 : Load rejection over-voltage at the converter AC bus

Table 2: Comparative Results

Test Cases	LCC	CCC	HCC-UP	HCC-LO
10% step at RCO	I_{dci} $M_p = 7\%$ $t_s = 70ms$	I_{dci} $M_p = 8\%$ $t_s = 70ms$	I_{dci} $M_p = 2\%$ $t_s = 50ms$	I_{dci} $M_p = 3.5\%$ $t_s = 50ms$
10% step at ICO	I_{dci} M_p = Nil $t_s = 50ms$	I_{dci} M_p = Nil $t_s = 60ms$	I_{dci} M_p = Nil $t_s = 50ms$	I_{dci} M_p = Nil $t_s = 50ms$
2° step at IGO	γ_{meas} $M_p = 10\%$ $t_s = 100ms$	γ_{meas} M_p = Nil $t_s = 70ms$	U γ_{meas} M_p = Nil $t_s = 60ms$ L γ_{meas} M_p = Nil $t_s = 100ms$	U γ_{meas} M_p = Nil $t_s = 90ms$ L γ_{meas} M_p = Nil $t_s = 80ms$
Mode Shift Test	Change over from rectifier mode to inverter mode and vice versa	Change over from rectifier mode to inverter mode and vice versa	Change over from rectifier mode to inverter mode and vice versa	Change over from rectifier mode to inverter mode and vice versa
3-Ph. fault	CF $I_{dcr}(pk) = 1.7$ p.u. $I_{dci}(pk) = 2.7$ p.u. VDCL-3 operated Smooth recovery	NCF $I_{dcr}(pk) = 1.2$ p.u. $I_{dci}(pk) = 1.4$ p.u. VDCL-2operated Smooth recovery	NCF $I_{dcr}(pk) = 1.4$ p.u. $I_{dci}(pk) = 1.76$ p.u. VDCL-3 operated Smooth recovery	NCF $I_{dcr}(pk) = 1.4$ p.u. $I_{dci}(pk) = 1.8$ p.u. VDCL3 operated Smooth recovery
SLG fault	CF $I_{dcr}(pk) = 1.5$ p.u. $I_{dci}(pk) = 2.0$ p.u. VDCL3 operated Smooth recovery	NCF $I_{dcr}(pk) = 1.1$ p.u. $I_{dci}(pk) = 1.3$ p.u. VDCL-2 operated Smooth recovery	NCF $I_{dcr}(pk) = 1.1$ p.u. $I_{dci}(pk) = 1.3$ p.u. VDCL-2 operated Smooth recovery	NCF $I_{dcr}(pk) = 1.1$ p.u. $I_{dci}(pk) = 1.3$ p.u. VDCL-2 operated Smooth recovery
DC fault	Vdc = 0 $I_{dcr}(pk) = 1.7$ p.u. $I_{dci} = 0$ VDCL-3 operated FRA taken place Smooth recovery	Vdc = 0 $I_{dcr}(pk) = 1.7$ p.u. $I_{dci} = 0$ VDCL-3 operated FRA taken place Smooth recovery	Vdc = 0 $I_{dcr}(pk) = 1.7$ p.u. $I_{dci} = 0$ VDCL-3 operated FRA taken place Smooth recovery	Vdc = 0 $I_{dcr}(pk) = 1.7$ p.u. $I_{dci} = 0$ VDCL-3 operated FRA taken place Smooth recovery
LROV	$V_{busr} = 1.35$ p.u. $V_{busi} = 1.23$p.u.	$V_{busr} = 1.35$ p.u. $V_{busi} = 1.15$p.u.	$V_{busr} = 1.35$ p.u. $V_{busi} = 1.20$p.u.	$V_{busr} = 1.35$ p.u. $V_{busi} = 1.20$p.u.

Notation:

RCO => Rectifier Current Order
ICO => Inverter Current Order
IGO => Inverter Gamma Order
CF => Commutation Failure
NCF => No Commutation Failure

M_p => Peak overshoot, t_s => Settling time
VDCL3 => VDCL characteristic portion 3
LROV => Load Rejection Over Voltage
FRA => Force Retard Action
U => Upper, L => Lower, γ_{meas} => γ measured

4.7 Summary

In this chapter, behaviour of different parameters such as V_{dc}, I_{dc}, AOr, AOi, AC bus voltages etc. under various transient conditions such as step change in different controller reference parameters, AC/DC faults, load rejection etc. are monitored and results are presented. Four different converter configurations namely, LCC, CCC, HCC-UP and HCC-LO are considered for the study. Each configuration is tested with an HVDC system interacting with weak AC networks and the results are analyzed.

Chapter 5

Conclusions

A comparative study of an HVDC system is carried out in this thesis. Three different converter configurations namely, the LCC, CCC and HCC are considered for the HVDC system. The HVDC system employed for the study is based on the CIGRE HVDC benchmark model traditionally used for dynamic analysis. PSCAD/EMTDC simulation package is used for performing the dynamic analysis.

Dynamic analysis of the HVDC system with conventional Line Commutated Converters (LCC) at the inverter end, shows that converters suffer a commutation failure when a remote AC 3-phase fault or a SLG fault occurs.

Similar studies are carried out using Capacitor Commutated Converters. Results show that with the same conditions applied to the AC network, there is no commutation failure. Also, the peak short circuit current and load rejection over-voltage are much lower when compared to those of the conventional configuration. Under steady state conditions, commutation capacitors produce reactive power which reduces not only the shunt capacitor size but also the number of circuit breakers for switching the capacitor banks.

Finally, a new configuration is studied. This configuration, namely HCC, is composed of a combination of a line commutated converter (LCC) and a capacitor commutated con-

verter (CCC) bridge. Depending on the location of the commutation capacitor (either upper or lower bridge), two distinct situations arise. As the upper and the lower bridges operate with different delay angles (but with constant minimum extinction angle characteristic), two different gamma controllers are used. Control circuits are modified to achieve desired characteristics. No modification is necessary in the current controller circuit.

The HCC configuration was studied next. Similar tests (as in those conducted for LCC or CCC configurations) were carried out. Both HCC configurations show much better performance as compared to the conventional configuration. Some of their performances are comparable to those of the CCC configuration. Hence, HCC-UP or HCC-LO options can be a good replacement of the CCC configuration in terms of reduced cost because fewer number of commutating capacitors are required and less switchyard space is required for commutating capacitors.

Thesis contributions

A modified version of the CCC configuration, called the Hybrid Converter Combination (HCC), is proposed. The dynamic performance of this modified version is studied and its performance is compared with two other configurations namely the LCC and CCC. It is established that the HCC option can be considered as a special case of the CCC where one of the capacitor banks is out of service due to some contingency. The ability to operate the station with this contingency is an improvement in the security of supply.

The study carried out here provides detailed information about a new version of the

CCC which is presently not available elsewhere. It is therefore anticipated that these details will be helpful to the utility planners and the manufacturers for further study.

Recommendations for future work

In case of HCC configuration, the commutation circuit is different for the upper and the lower converter. As a result, the presence of low order characteristic harmonics (such as 5th and 7th) is observed. A more detailed study can therefore be done considering the addition of 5th and 7th harmonic filters at the expense of the shunt capacitor.

Also in this study, a 12-pulse monopolar HVDC system is considered to minimize computer memory usage and to achieve higher speed of simulation. It will, therefore, be more practical to model a complete bipolar HVDC system for study. In that case, four different options with HCC configuration (because of various combinations depending on the location of the CCC) are to be studied.

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APPENDIX - A

Transformer Sizing and Filter Design

Inverter Transformer

DC Power to be delivered, $P_{dci} = 1000$ MW

DC voltage level, $V_{dci} = 500$ kV

DC rated current, $I_{dci} = \frac{P_{dci}}{V_{dci}} = \frac{1000}{500} = 2$ kA

Rectifier firing angle, $\alpha = 15°$

Minimum extinction angle, $\gamma = 18°$

R.M.S. value of the secondary line current (valve side)

$$I_{LLi} = \frac{\sqrt{2}}{\sqrt{3}} \times I_{dci} = 1.633\text{kA}$$

Let line voltage (valve side) of the inverter transformer = V_{LLi}

MVA of each transformer, $S_{Ti} = \sqrt{3} \times V_{LLi} \times I_{LLi}$ = Base MVA

$$S_{Ti} = \sqrt{3} \times V_{LLi} \times 1.633 = 2.82844\ V_{LLi} \qquad \text{(A.1)}$$

Base impedance, $Z_{basei} = \frac{V_{LLi}^2}{S_{Ti}} = \frac{V_{LLi}^2}{2.82844\ V_{LLi}} = 0.35355 V_{LLi}$ (A.2)

Transformer leakage reactance, $X_L = 0.18pu = 0.18 \times 0.35355 V_{LLi} = 0.06364 V_{LLi}$

We know,

$$\frac{V_{dci}}{2} = 1.35 \times V_{LLi} \times \cos\gamma - \frac{3 \times I_{dci} \times X_{Li}}{\pi}$$

Putting the values of V_{dci} and γ, we have $250 = 1.284 V_{LLi} - 0.1215 V_{LLi}$.

Therefore, $V_{LLi} = 215.0753$ kV

Rating of the inverter transformer, $S_{Ti} = 608.3248$ MVA

Turns Ratio

STAR/DELTA transformer, $k = \frac{230/(\sqrt{3})}{215.0753} = 0.617$

STAR/STAR transformer, $k = \frac{230/(\sqrt{3})}{215.0753/(\sqrt{3})} = 1.069$

Rectifier Transformer

Cable resistance, $R_{cab} = 5\ \Omega$

Voltage drop, $V_{drop} = I_{dci} \times R_{cab} = 10$ kV

Cable loss, $P_{cable} = 20$ MW

DC power to be delivered, $P_{dcr} = P_{dci} + P_{cable} = 520$ MW

DC voltage level, $V_{dcr} = V_{dci} + V_{drop} = 510$ kV

DC rated current, $I_{dcr} = \frac{P_{dcr}}{V_{dcr}} = 2$ kA

Rectifier firing angle, $\alpha = 15°$

R.M.S. value of the secondary line current (valve side),

$$I_{LLr} = \frac{\sqrt{2}}{\sqrt{3}} \times I_{dcr} = 1.633\text{kA}$$

Let line voltage (valve side) of the rectifier transformer = V_{LLr}

MVA of each transformer, $S_{Tr} = \sqrt{3} \times V_{LLr} \times I_{LLr}$ = Base MVA

$$S_{Tr} = \sqrt{3} \times V_{LLr} \times 1.633 = 2.82844\ V_{LLi} \tag{A.3}$$

$$\text{Base impedance, } Z_{baser} = \frac{V_{LLr}^{\ 2}}{S_{Tr}} = \frac{V_{LLr}^{\ 2}}{2.82844 V_{LLr}} = 0.35355 V_{LLr} \tag{A.4}$$

Transformer leakage reactance, $X_L = 0.18 pu = 0.18 \times 0.35355 V_{LLr} = 0.06364 V_{LLr}$

We know,

$$\frac{V_{dcr}}{2} = 1.35 \times V_{LLr} \times \cos\alpha - \frac{3 \times I_{dcr} \times X_{Lr}}{\pi}$$

Putting the values of V_{dcr} and α, we have $255 = 1.304 V_{LLr} - 0.1215 V_{LLr}$

Therefore, $V_{LLr} = 215.6526$ kV

Rating of the rectifier transformer, $S_{Tr} = 609.9578$ MVA

Turns Ratio

STAR/DELTA transformer, $k = \frac{345/(\sqrt{3})}{215.6526} = 0.924$

STAR/STAR transformer, $k = \frac{345/(\sqrt{3})}{215.6526/(\sqrt{3})} = 1.599$

Filter Design

We know for 12-pulse converter the characteristic harmonics on AC sides are of the order of

$$h = pq \mp 1$$

where p is the pulse number, q is any integer. It is normal practice to use shunt R-L-C tuned filter for lower order harmonics and high-pass filter for higher order harmonics.

Low Pass Filter

V_{LL} = Line to Line voltage = 345 kV

V_{ph} = Phase voltage = $V_{LL}/\sqrt{3}$ kV

R, L and C = Resistance, Inductance and Capacitance of the filter respectively

Q = Quality factor = $\frac{\omega_r L}{R} = 200$

Total MVAR requirement = 125

MVAR per phase, $Q_{LP} = 125/3$

Filter impedance, $Z = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}$

$$Z^2 = R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2 = \frac{\omega^2 L^2}{Q^2} + \left(\frac{\omega^2 LC - 1}{\omega C}\right)^2$$

defining $\omega_r = \frac{1}{\sqrt{LC}}$ the above equation becomes

$$Z^2 = \frac{\omega^2/\omega_r^2 + Q^2(\omega^2/\omega_r^2 - 1)^2}{Q^2 \cdot \omega^2 \cdot C^2}$$

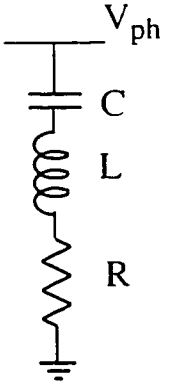

Figure A1: R-L-C filter

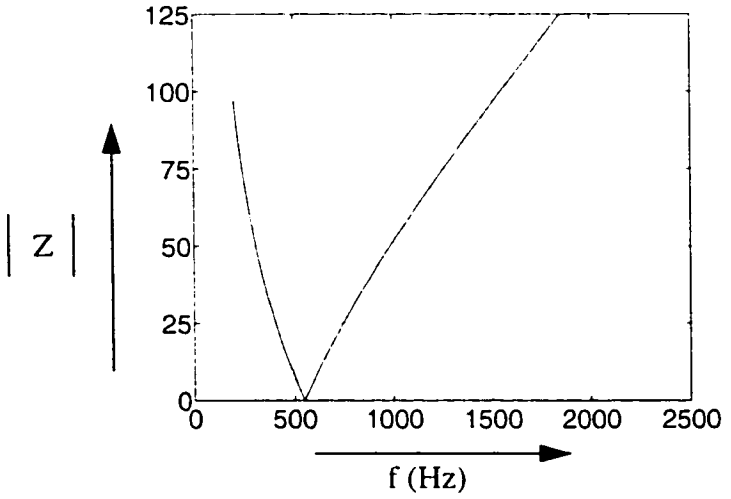

Figure A2: Frequency response of R-L-C filter

Now, $Q_{LP} = \frac{V_{ph}^2}{Z^2 \cdot \omega C}$ defining $\frac{\omega}{\omega_r} = M$ and replacing Z^2 we have

$$C = \frac{Q_{LP}}{V_{ph}^2} \cdot \left(\frac{M^4 + Q^2 \cdot (M^2 - 1)^2}{Q^2 \cdot \omega} \right) \qquad \text{(A.5)}$$

$$L = \frac{1}{\omega_r^2 \cdot C} \text{ and } R = \frac{\omega L}{Q}$$

For 11th harmonic filter $M = \frac{1}{11} = 0.09090909$ and $\omega_r = 550$ Hz. By solving equation A.1, we get C = 3.288 uF, L = 0.0255 H and R = 0.0400 Ω.

High-pass Filter

Let, R, L and C = Resistance, Inductance and Capacitance of the filter respectively

$$Z = \frac{1}{j\omega C} + \left(\frac{1}{R} + \frac{1}{j\omega L}\right)^{-1} \tag{A.6}$$

Defining following quantities

Resonant Frequency, $\omega_r = \frac{1}{\sqrt{LC}}$

Per unit frequency, $f^* = \frac{\omega}{\omega_r} = \frac{f}{f_r}$

Characteristic impedance, $X_o = \sqrt{\frac{L}{C}}$

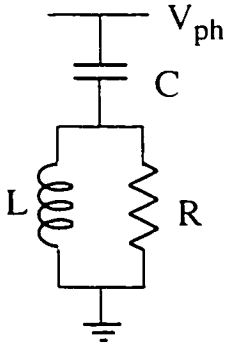

Figure A3: High-pass filter

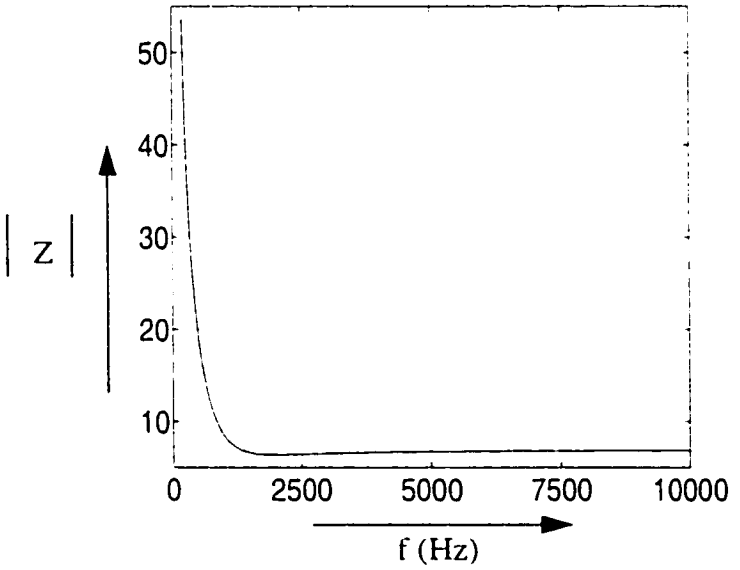

Figure A4: Frequency response of high-pass filter

Quality factor, $Q = \frac{R}{X_o}$

Replacing with above quantities, equation A.2 becomes

$$Z = \frac{1}{jf^*} + \left(\frac{1}{Q} + \frac{1}{jf^*}\right)^{-1}$$

Q is an index of sharpness of tuning. Value of Q varies between 0.5 - 2.0

Total reactive power requirement = 250 MVAR

Reactive power requirement per phase, Q_{HP}= 250/3 MVAR

As the impedance of the parallel branch is negligible, we can write

$$Q_{HP} = V_{ph}^{\ 2} \cdot \omega C \text{ or } C = \frac{Q_{HP}}{V_{ph}^{\ 2} \cdot \omega}$$

$$L = \frac{1}{\omega_r^{\ 2} \cdot C}$$

considering $Q = 0.75$ and $\omega_r = 24 \times 50$ we have, C =6.685 uF, L=0.0026 H and R =14.878 Ω

Shunt Compensation

Let shunt capacitance = C_{sh}

Total reactive power requirement = 125 MVAR

Reactive power requirement per phase, Q_{SH}= 125/3 MVAR

So, $Q_{SH} = V_{ph}^{\ 2} \cdot \omega C_{sh}$ putting values for Q_{SH}, V_{ph} and ω

$$C_{sh} = 3.342 \text{ uF}$$

Details of filter parameters for both rectifier side and inverter side are presented in Table 3.

Table 3: Signals Monitored

Signal No.	Rectifier-side	Signal No.	Inverter-side
1	Phase - A voltage	9	Phase - A voltage
2	Phase - B voltage	10	Phase - B voltage
3	Phase - C voltage	11	Phase - C voltage
4	AC bus voltage (RMS)	12	AC bus voltage (RMS)
5	DC Voltage	13	Line Current
6	DC Current	14	Valve Line Current - Upper Bridge
7	Alpha Order	15	Valve Line Current - Lower Bridge
8	Current Order	16	DC Voltage
		17	DC Current
		18	Alpha Order *
		19	Current Order *
		20	Gamma reference *
		21	Measured Minimum Gamma *
		22	Valve Stress - Upper Bridge
		23	Valve Stress - Lower Bridge

* For HCC configuration signals for upper and lower converters are monitored separately

Table 4: Test Cases

Test No.	Test Description
1	Step Change in Rectifier Current Order
2	Step Change in Inverter Current Order
3	Step Change in Inverter Gamma Order
4	Mode Shift Test
5	Remote Three Phase Fault on Inverter side AC network
6	Remote Single Line to Ground fault on Inverter side AC network
7	Inverter side DC Line Fault
8	Load Rejection Over-voltage

Table 5: Details of Filter Parameters

Parameters	Rectifier				Inverter			
	11th	13th	High pass	Shunt COMP.	11th	13th	High pass	Shunt COMP.
R (ohm)	0.0400	0.0285	14.878	-	0.0178	0.0127	6.6125	-
L (H)	0.0255	0.0181	0.0026	-	0.0113	0.0081	0.0012	-
C (μF)	3.288	3.303	6.685	-	7.397	7.433	15.04	-
Q factor	200	200	0.75		200	200	0.75	-
C_{sh} (μF)	-	-	-	3.342	-	-	-	9.355

COMP. => Compensation

Table 6: Details of Characteristic Harmonics

Configuration	Shunt Capacitor (μF)	5th (kA)	7th (kA)	11th (kA)	13th (kA)	gamma
LCC	9.355	-	-	0.1138	0.0728	18°
CCC	0.25	-	-	0.1334	0.0916	12°
HCC-UP	6.0	0.1965	0.1432	0.0856	0.0486	upper = 12° lower = 20°
HCC-LO	4.75	0.2004	0.1480	0.0809	0.0456	upper = 20° lower = 12°

APPENDIX - B

Background of HVDC Simulation Package/Tools [23]

EMTDC is a simulator of electric networks with a capability to model complex power electronics and controls. When run under the PSCAD graphical user interface, the PSCAD/EMTDC combination becomes a powerful means of visualising the complexity of the portions of the electric power system.

EMTDC is a transient simulator which has been evolving since the mid-1970s. Originally inspired by Dr. Hermann Dommel from his classic April 1969 IEEE paper published in the Transactions on Power Apparatus and Systems.

Transient simulation has changed greatly since 1970s. The first early version of EMTDC were run at Manitoba Hydro on mainframe computers using IBM punched cards. Only one or two cases a day could be submitted and run so coding and program development were tortuously slow compared with what can be accomplished today. As computers developed, more sophisticated file handling systems become available.

With users demand for efficiency and simplicity, Manitoba HVDC Research Centre embarked on developing the PSCAD graphical user interface to facilitate simulation studies on EMTDC. PSCAD/EMTDC version 2 was created in the early 1990s for the use on UNIX workstation. A new version is now available for use in Windows environment. In this study PSCAD/EMTDC version 2 is used as simulation tools.

APPENDIX - C

List of Publications

Paper submitted on this research

A. Mazumder and V.K. Sood, "Comparative Study of HVDC System with Capacitor Commutated Converters", accepted for publication in the 7 th International Conference on Modeling and Simulation of Electric Machines, Converters and Systems (ELECTRIMACS 2002) August 18-21, 2002, École de technologie supérieure, Montreal, Canada