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A RESONANT AC/DC CONVERTER FOR HIGH FREQUENCY POWER DISTRIBUTION SYSTEMS

FARIBORZ MUSAVI

A Thesis

In

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ABSTRACT

A RESONANT AC/DC CONVERTER FOR HIGH FREQUENCY POWER DISTRIBUTION SYSTEMS

FARIBORZ MUSAVI

A Resonant AC/DC Converter for High Frequency Power Distribution Systems is presented in this thesis. The proposed converter employs a resonant network consisting of a few passive components. With this resonant network, the converter can attain close to unity power factor and very small total harmonic distortion under all load conditions. The operating principle of the circuit is demonstrated, and the steady state analysis is performed including the effect of leakage inductance. Based on the analysis, criteria for optimal design are given. Experimental and simulation results of a prototype converting the input AC voltage of 28 V rms at 1 MHz, to 1.6 Volt DC at 20 A are given to verify the proof of concept, and analytical work reported in this thesis.

ACKNOWLEDGEMENT

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Dedicated to my parents

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LIST OF ACRONYMS

AC	Alternative Current
CCM	Continuous Conduction Mode
CPU	Central Processing Unit
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductor
ESR	Equivalent Series Resistor
FB	Feedback
HF	High Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PF	Power Factor
PWM	Pulse Width Modulation
rms	Root Mean Square value
SB	Silver Box
SR	Synchronous Rectifier
THD	Total Harmonic Distortion
VRM	Voltage Regulator Module

LIST OF PRINCIPLE SYMBOLS

□	control angle of main switches
ϕ	phase angle of resonant current in series branch with respect to input voltage
θ	phase angle between input current and voltage
ω_o	angular input frequency in radians
C_o	output filter capacitor
C_P	resonant network parallel capacitor
C_S	resonant network series capacitor
D	duty ratio of main switches
f_o	input voltage frequency
f_s	switching frequency
I_t	current through the series branch of resonant network
I_S	current in the input of converter
I_o	nominal output current
I_{tp}	current through the primary side of transformer
i_t	instantaneous series branch current in resonant network
i_S	instantaneous input current
k	turns ratio of the power transformer primary to secondary windings
L_S	resonant network series inductor

L_{lk}	leakage inductance of the transformer
n	number of harmonics in the input current and resonant network
N_1/N_2	turns ratio of the power transformer
P_o	output power of the converter
Q_1 and Q_2	two main switches of the converter
R_o	the converter load
R_{eq}	equivalent load transferred to the primary side of transformer
SR_1 and SR_2	two switches of the synchronous rectifiers
T_r	power transformer
V_o	nominal output voltage
V_{ref}	output reference voltage
V_S	nominal input voltage
V_{TP}	voltage across the primary side of transformer
v_{TP}	instantaneous voltage of transformer in primary side
v_S	instantaneous input voltage
Z_{P1}	fundamental impedance of parallel branch in resonant network
Z_{Pn}	n^{th} impedance of parallel branch in resonant network
Z_{S1}	fundamental impedance of series branch in resonant network
Z_{Pn}	n^{th} impedance of series branch in resonant network

CHAPTER 1

INTRODUCTION

1.1 General Introduction

Telecommunication and computer systems have gone through dramatic changes in the last decade to obtain higher speed, larger capability and more advanced functions. As an indispensable part of these systems, the power aspect in terms of power quality, conversion efficiency, reliability, density and cost is becoming an increasingly important issue to attain the advanced performance goals of the entire system.

Continuous advances in semiconductor technology result in ever-increasing functional densities and processing speed of electronic systems. To allow higher processing speed and to minimize power consumption, supply voltage are being reduced in new logic families. With the simultaneous increase in power demand and decrease in supply voltage level, new challenges are presented for the power systems. To decrease power consumption and increase the speed, the next generation of computer microprocessors is expected to operate at a much lower voltage, 0.5V to 1.5V, a much higher current, 50 A to 150 A, at a clock rate above 1 GHz and to exhibit current slew rate of 5 A/ns.

Moreover, the total voltage tolerance will become much tighter. In the future, the total voltage tolerance will be 2% (for 1.6 V output, the voltage deviation can only be ± 32 mV). Generally, these power supplies are required to have a high power density

and to operate with a high efficiency. To meet these requirements and to provide a fast transient response, the power conversion must be performed at a high switching frequency, so the following challenges are the result of the above trends:

(i) Load currents are steadily increasing with the time.

(ii) Operating voltages are decreasing as a result of smaller transistors.

(iii) Slew rate from the active mode to the sleep mode and vice versa has been increasing.

(iv) Power densities are steadily going up with time. It is always required to provide more power and occupy less space.

(v) Efficiency of converters has remained constant at approximately 80%.

Table1-1 is given the specification of future power supplies for new generation microprocessors [3]:

Table1- 1: The specification of future VRM.

Load current	50 ~150 A
Output voltage	0.5 ~ 1.5 V
Slew rate	5 A/ns
Efficiency	> 80%
Density	High
Output voltage tolerance	± 2%

In order to select an optimum power system configuration for a specific product in telecommunication, each system has to be considered separately from many points of

view. Therefore, in the following sections, we will first know the advances in computer performance and its impact on power processing, and then we will see options for powering telecommunications equipment, to be able to justify our selected architecture.

1.2 Power Delivery System of Computers

The power system configuration in the computer is shown conceptually in Figure1-1. From AC utility to the processor (CPU), power delivery system consists of a system power supply (commonly known as "Silver Box" (SB)), voltage regulator module (VRM), decoupling capacitors, processors and distribution [1].

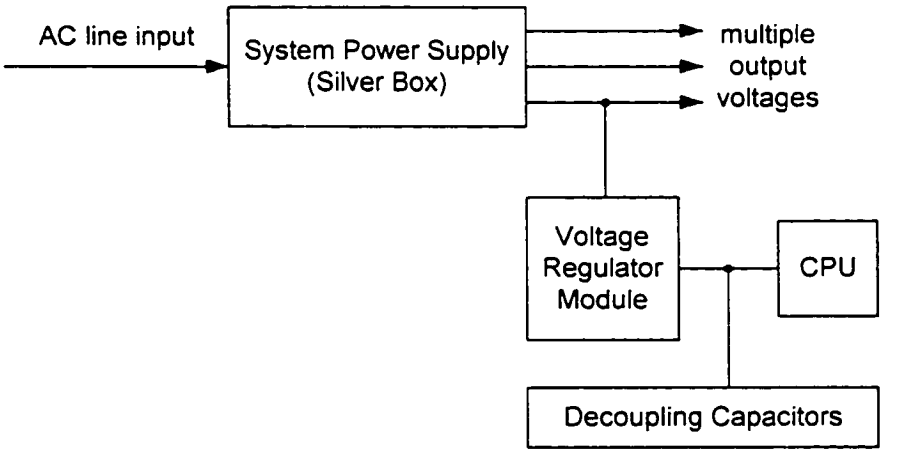


Figure1- 1: CPU Power Delivery System

The silver box converts the input line AC voltage into DC bus voltage. In the early days of Intel486™ processor, SB could directly power the processor since it was easy to maintain 5% voltage tolerance under 1 A load. But starting from the Pentium® processor generation, with more and more system components drawing higher current

(>10 A) at lower voltage (<3.3 V), local VRMs have to re-process the intermediate voltage from SB into lower DC voltage. Another fact is that as the speed of processor increases, they are becoming a more dynamic load to their power supplies. To reduce the effect of parasitic impedance of VRM-load connection on the power supply transient response, VRM must be located next to the load (on-board conversion), and a large number of de-coupling capacitors are required to be connected across the processor.

From SB to VRM, the power distribution is traditionally implemented in DC domain. A novel technique know as high frequency AC distribution opens a new horizon for powering the future computer systems. Introduction and comparison of all possible power distribution architecture are described later on in the following sections.

1.3 Advances in Computer Performance and Its Impacts on Power Processing

Microprocessor roadmaps indicate a continuing upward-slope in clock frequency Figure1-2 and transistor density Figure1-3 to achieve higher performance [1,2]. Increases

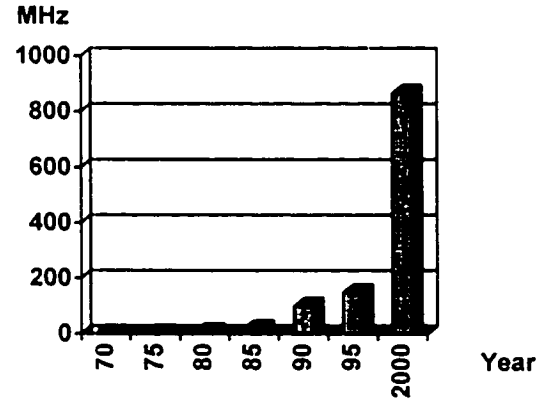


Figure1- 2: Internal Clock Frequency

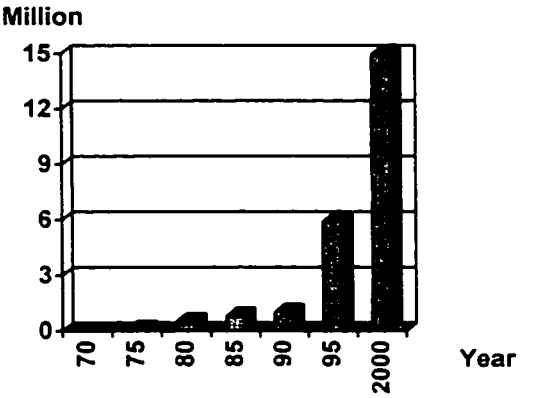


Figure1- 3: Number of transistors

Table1- 2: Advances in processor speed and its impact on power supply

YEAR	PROCESSOR	SPEED	V_{cc}	I_{cc}
1979	8086	5 ~ 8 MHz	5.0 V	<<1 A
1985	Intel386™	16 ~ 20 MHz	5.0 V	<1 A
1989	Intel486™	25 ~ 100 MHz	3.3/5.0 V	1 A
1993	Pentium®	60 ~ 66 MHz	5.0 V	3 A
1994	Pentium®	90 ~ 233 MHz	2.8/3.3 V	5 A
1995	Pentium® Pro	150 ~ 200 MHz	3.1/3.3 V	15A
1997	Pentium® II	233 ~ 300 MHz	2.8 V	14 A
2000	Pentium® III	500 ~ 866 MHz	1.65 V	14 A

in the processor speed and transistor density have impacted the PC power supply industry significantly, as shown in Table1-2. Compared to Intel486™ processor, in Pentium® III processor, speed has increased by 9 times, V_{cc} voltage has decreased lower than 2 V, and I_{cc} current is up by more than a factor of 10.

1.3.1 Low Supply Voltage with Tighter Tolerance

In Table1-2, the trend of voltage scaling of power supply is derived from the consideration of power dissipation. The major source of power dissipation in the processor is the dynamic power loss P_D, which is directly related to the processor speed, gate output capacitance C and the square of supply voltage V_{cc}:

$$P_D = \alpha C V_{cc}^2 f_c / 2 \qquad (1\text{-}1)$$

Where, α is activity scale (0.0 ~ 1.0), and f_c is the clock frequency. This expression refers to a single gate. Total dynamic power dissipation is the sum of all the gates active at any instant-of-time. Currently, due to the dramatic increase in clock rate and transistor count, a reduction in supply voltage is the most effective method for reducing dynamic power loss. This technique is referred to as "voltage scaling". It also allows a reduction in feature size and thinner oxide layers needed for higher transistor density packing. Therefore, 1.65 V in Table1-2 is only a transient stage. The processor supply voltage in future generation of processors will decrease to 0.5 V ~ 1.5 V.

In order to ensure the accurate high speed data transition, voltage scaling technique requires much tighter tolerance on the power supply. Currently, the voltage tolerance is

5% (for 3.3 V VRM output, the voltage deviation can be ± 165mV). In the future, the total voltage tolerance will be 2%, which means for 1.6 V VRM output, the voltage deviation can only be ± 32 mV. For this kind of accuracy, the need for low voltage, precision, temperature stable, and low noise references is a must.

1.3.2 High Supply Current with Tight Slew Rate

Because more devices are packed on a single processor chip and processor function at higher frequencies, future processors are expected to draw a much higher current, up to 50 ~150 A, and present much higher slew rate, up to 1 A/ns ~ 5 A/ns. The most dramatic load transient occurs in the processor transition from the sleep mode (typical load current ≤ 5 A) to the active mode (typical load current ≥ 50 A) and vice versa. Currently, it is in the range of 10 ~ 100 A/ μ s, for processors operating at around 500 MHz. In future, it will be expected to be 1 ~ 5 A/ns, or even higher.

1.3.3 Large Load Transient

Figure1-4 shows the typical process supply voltage waveform during large load transient. There are two voltage drops that can be observed. The initial voltage deviation caused by the interaction of parasitic interconnection inductance and de-coupling capacitance. After this voltage drop spike, the transient response is governed by the power stage parameters (output filter) and the bandwidth of control loop. To keep supply voltage within the required tight load regulation rang, design consideration for VRM output filter and control loop are becoming more critical issues [5,6].

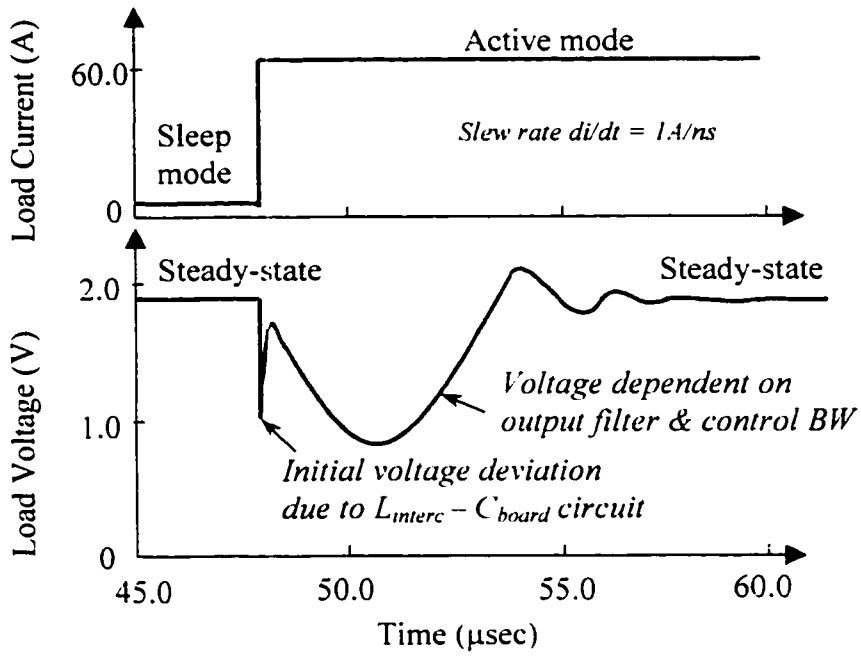


Figure1- 4: Typical processor supply voltage waveform during the load transition

1.4 Overall Power Architecture

The trend of supplying low voltage with tight regulation and high current with high slew rate in a cost-effective manner is not only related to VRM and the distribution between VRM and processor, but also involves the overall power architecture. Three powering options: low voltage DC distribution, high voltage DC distribution, and high frequency AC distribution will be briefly described below[1,4,10,11,15].

1.4.1 Low Voltage DC Distribution

In the early days of computer systems, lower speed and fewer components were involved; the silver box implemented by a very slow power supply with multiple outputs

was able to meet the requirements of every power demand. Therefore, the simplest and commonly employed approach in powering the computer system is the so-called low voltage DC distribution [1,15], as shown in Figure1-5. The silver box converts the AC line input voltage into several low DC voltages, which then are distributed through the shelf bus bar or back plane to the various system cards. Most low voltages on each card serve only as the input for several VRMs where these voltages are converted into even lower voltage levels but at higher currents. Also, on each card, a current limiting circuit may have to be used to limit the inrush current during the "hot insertion" of the card.

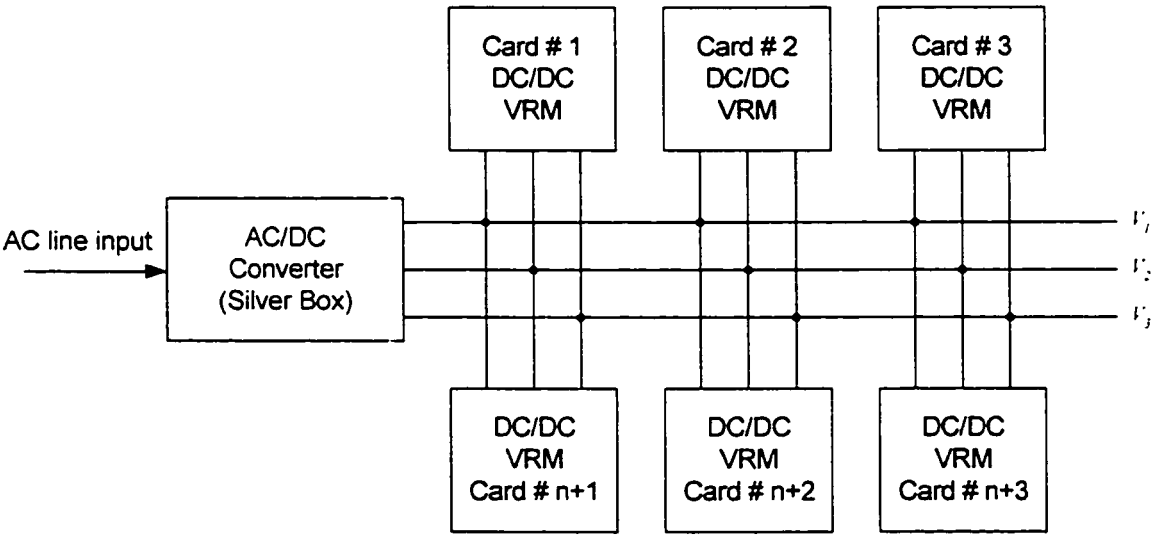


Figure1- 5: Low voltage DC power distribution

This power scheme is relatively simple, however, it is no longer capable of providing power quality used in the modern and future digital electronics for the following reasons:

(i) Additional supply voltages, such as +15 V, +5 V, +3.3 V, -5.2 V etc., are required;

(ii) Very fast transient response at low supply voltage is not practical from a single buck converter;

(iii) Distribution of a heavy current through the bus bar or back plane introduces loss and requires a large amount of space for heavy wiring;

(iv) The heat generated in the power conversion process is concentrated within the converter, which may result in a necessity to use forced air cooling;

(v) Static and dynamic load regulations with tight tolerances at low voltages need regulation at the point-of-use;

(vi) Cross regulation effects between the outputs of a single bulk converter increases the problems with tight regulation requirement.

1.4.2 High Voltage DC Distribution

Since some draw backs of previous low voltage DC distribution are direct results of distribution of low voltage at high current levels, better performance can be expected if a higher voltage is used as the intermediate voltage supplying the VRMs. Figure1-6 shows the configuration of the high voltage DC distribution [1.3].

In this power scheme, the silver box generates only a single voltage at a much higher voltage level (typically 48 V DC), and then the point-of-use power supplies (PUPS) distributed on each system card convert this intermediate voltage into the required voltage level.

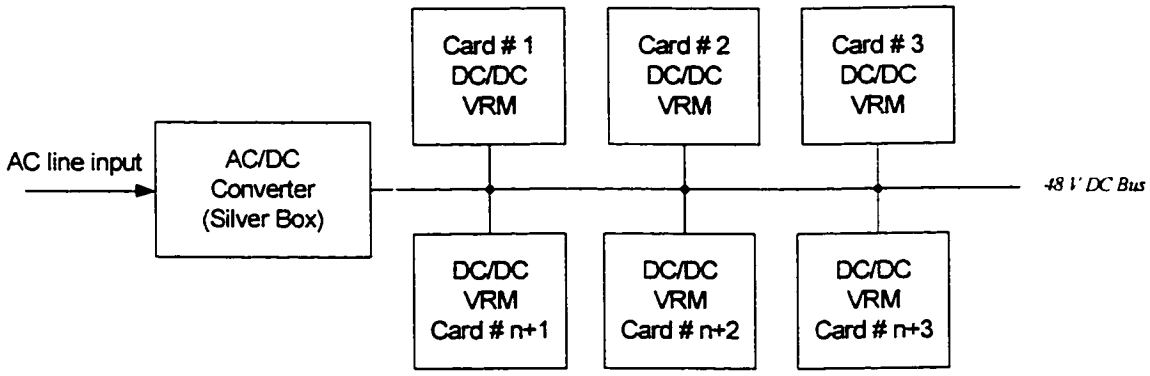


Figure1- 6: High voltage DC power distribution

High voltage DC distribution has some advantages over the low voltage DC power distribution as follows:

(i) Heat produced by the power conversion is distributed through the whole system;

(ii) The loss within the back plane is minimized since higher voltage and thus smaller current is distributed;

(iii) Voltage regulation at the point-of-use is excellent;

Although many publications have shown the further performance improvements of such power distribution systems, it still suffers from the following problems:

(i) Distributed input filters are required for isolation from converter interaction and they are sensitive to impedance instability;

(ii) More components, filter and converters add a high cost to the system, take a large board space, and lower the system reliability;

(iii) No provision to efficiency deal with negative high *di/dt*;

(iv) Inrush current limiting circuit on each card is still needed if "hot insertion" of the system cards is required.

Therefore, several research woks have been done for an improved power distribution scheme, which could provide all the advantages of high voltage DC distribution, but at fewer component, lower cost, smaller size, and higher reliability. A novel technique, high frequency AC power distribution, for the future computer system will be introduced in the next sub-section.

1.4.3 High Frequency AC Power Distribution

The concept of high frequency AC (HFAC) power distribution system was first proposed by NASA some 25 years ago. Since then a number of industries have been working on this new powering scheme for other applications [1,6,13,14,17]. The basic configuration of the HFAC power distribution system is shown in Figure1-7.

The silver box generates high frequency AC voltage. The HFAC is distributed through the back plane to the various system cards, where it will be converted to the specific DC voltage level by the local AC/DC converter (ACVRM).

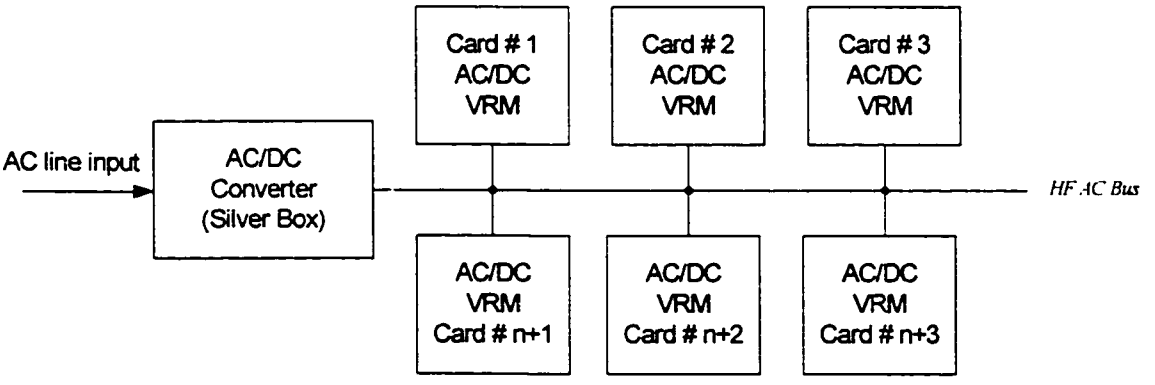
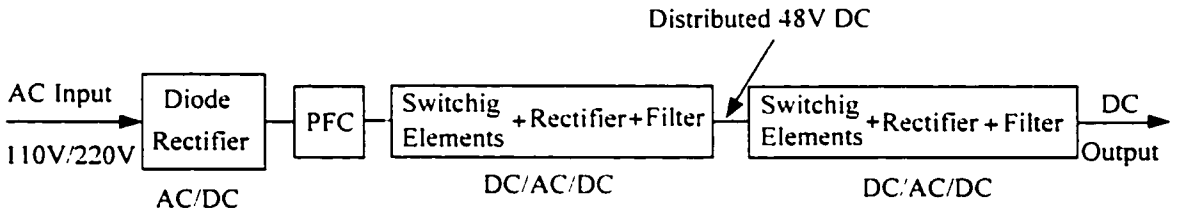


Figure1- 7: High frequency AC power distribution

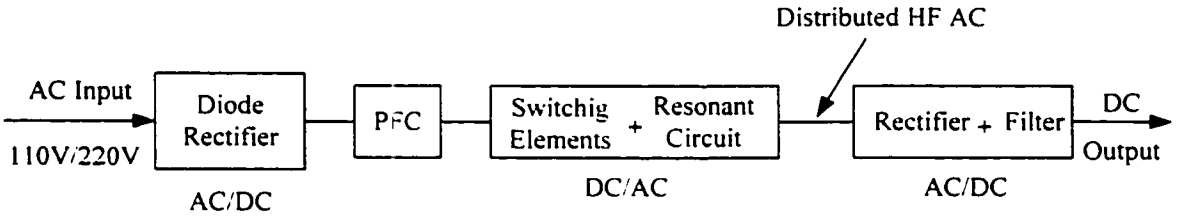
This new scheme not only combines the advantages of the existing DC powering scheme but also brings new features, which are technically impossible in DC domain. The main features of this powering scheme are discussed as following:

(i) Excellent transient response. For a properly designed wide-band width feedback control, the large-signal transient response is mainly determined by the response of output filter [6]. Since no low-pass filter is present at the output of the inverter, the feedback loop in AC domain can be closed at a much higher frequency than in case of DC domain.

(ii) Reduced power conversion stages as shown in Figure1-8. This results in higher efficiency, lower cost, smaller size, and better reliability.



(a)



(b)

Figure1- 8: (a) High Voltage DC Distribution system (b) HF AC Distribution System

(iii) Active energy steering. The energy corresponding to the positive current step must be provided by power delivery system. During the negative current step, however, energy could be either stored or damped. Damping is technically the simplest, but results in poor efficiency. In HFAC distribution, the excess energy can easily be steered to high frequency bus side and be re-used when needed.

(iv) Simple current limit. The resonant circuits which are incorporated in both silver box and ACVRM provide inherent short-circuit protection at the power interface (fuse-less protection) and limited power transfer to the load (elimination of fire hazard). Therefore, the inrush current can be limited without any other additional circuit if "hot insertion" of the system card required.

(v) Reduction of thermal stress. This not only increases the system reliability, but also may allow the system to operate with convection cooling rather than the forced air cooling. The elimination of fans will further improve the overall reliability and reduce the maintenance requirement.

(vi) Connector-less power transfer. This feature, which is technically impossible to be implemented into DC power scheme, becomes the most attractive potential in HFAC power distribution. The transformer used in AC/DC converter can serve as media for magnetic coupling between the back-plane (on which has the main power tracking) and the removable load card (on which has the point-of-use AC/DC converter). To achieve this, the transformer must be constructed in such a way that one half (which contain the primary winding) will be physically located on the load card together with AC/DC converters. The energy then can be coupled

through the magnetic field only, without any metallic connection. This solution has the potential to offer a substantial improvement in system reliability due to the elimination of power connector.

1.5 Thesis Objectives

This thesis presents a High Frequency AC/DC Converter for new generation of microprocessors and telecom systems. The main objectives of the thesis are:

(i) To develop the topology of HF AC/DC converter. The proposed topology should meet the stringent requirements as follows: tight voltage regulation, fast transient response, high efficiency, high power density, low EMI, and constant operating frequency;

(ii) To present the steady-state and dynamic performance and characteristics of proposed converter topology;

(iii) To present the control scheme used to achieve the best dynamic performance;

(iv) To verify with results from simulation performed in Psim and Pspice;

(v) To present design characteristics of the converter based on the steady-state analyses, which help in understanding the internal working of the converter;

(vi) To generate design procedure and curves for industrial applications;

(vii) To specify the design guidelines with a design example to assist in the design process.

1.6 Thesis Outline

The thesis is organized in the following structure:

In Chapter 2, the possible topologies and the proposed topology are presented. The simplified analysis is performed to understand its steady states characteristics and properties. Simulation results are also presented as proofs of concept. The simulation under a real condition is presented which leads us to the next chapter.

In chapter 3, the proposed topology under a real condition is analyzed, considering the effect of leakage inductance and all inductances and resistors in series with the switches. The results from simplified analyses and detailed analyses are compared with the simulation to justify the analyses.

In chapter 4, the proposed topology under dynamic condition is analyzed. This includes small signal modeling and space-state averaging to linearize the power stage for finding the power stage transfer function, which leads us to compensate the feedback loop to dynamically stabilize the converter. At the end of this chapter, the converter responses to the step changes in the load are shown to verify the design in simulation.

In chapter 5, a design procedure oriented for industrial applications is generated based on the analyses performed in the previous chapters. A design example is also given.

In chapter 6, a summery of the thesis is given. A conclusion and contribution of the thesis are discussed. Suggestions for future works in this area are also suggested.

CHAPTER 2

A RESONANT AC/DC CONVERTER FOR HIGH FREQUENCY DISTRIBUTION SYSTEMS

2.1 Introduction

A resonant AC/DC converter for high frequency distribution systems is presented in this chapter. Dr. P.K. Jain at CAL CORPORATION first invented this topology during the development of AC/DC converters for a high frequency technology for the Canadian Space Station Program [19]. In this thesis, the same idea of resonant converter topology is held. However it is now implemented for even higher frequency applications using MOSFETs as the main switches in the primary side of the transformer, and synchronous rectifiers in the secondary side of the transformer.

The proposed converter topology converts a high frequency AC voltage to a controlled output DC voltage while drawing close-to-sinusoidal input current with a near unity power factor. This topology uses only one conversion stage, which results in higher efficiency, and lower weight and volume. Also, the operating frequency of converter is constant and synchronized with the input frequency. Together with the distortion less input current and constant frequency, the EMI/electromagnetic compatibility (EMC) filter requirements are minimized.

The converter circuit employs an input resonant network to convert the single-phase high-frequency sinusoidal voltage source into a sinusoidal high-frequency bi-directional current source. The output of this current source is rectified by synchronous

rectification and is controlled by a bi-directional switch. The controlled rectified current is then filtered to obtain a constant voltage across load. A generic diagram of the AC/DC converter is shown in Figure 2-1. This converter consists of:

(i) Resonant Network: For converting the single-phase high frequency sinusoidal input AC voltage to a sinusoidal high-frequency bi-directional current source;

(ii) Current Controller: Connected in parallel to the resonant network to receive the sinusoidal high-frequency current output of resonant network and provide the desired output current from the converter. The current controller consists of two controlled switches, Q_1 and Q_2, connected in series back to back to each other;

(iii) Transformer: To provide matching output voltage, and isolation for the output load;

(iv) Synchronous Rectifiers: Connected to the secondary of transformer, to convert the bi-directional current into a unidirectional current;

(v) Output filter: Connected to the synchronous rectifier to provide an essentially ripple free, substantially DC output voltage.

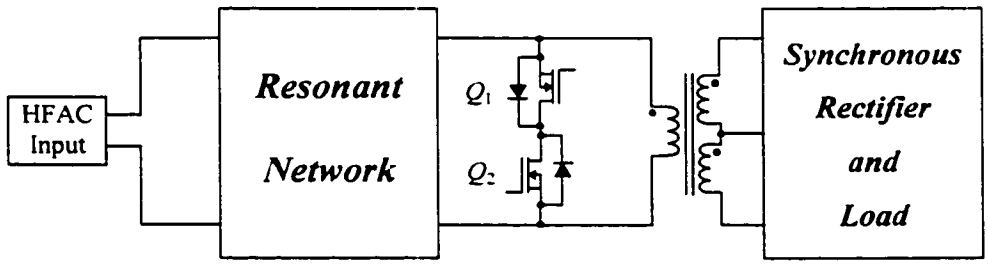


Figure2- 1: A generic diagram of AC/DC converter

In order to understand the operating principle and performance characteristics of

the proposed topology, and to provide reference in design procedure in Chapter 5, the steady state analysis is performed in this chapter. The outline of this chapter is as follows:

The proposed topology is presented in Section 2.2. The steady state analysis is performed in Section 2.3. Simulation results are given in Section 2.4 to verify the concepts and theoretical analysis. At the end of this chapter, some conclusions are drawn.

2.2 Circuit Description

Figure2-2 shows the proposed HF AC/DC converter topology. In this type of converter, the resonant network comprises a parallel capacitor C_P, a series inductor L_S and a series capacitor C_S. The capacitor C_P is connected in parallel with the input source. Both the inductor L_S and capacitor C_S are connected in series after capacitor C_P. The resonant circuit components, C_P, L_S and C_S, are selected such that a close-to-unity input power factor and a sinusoidal alternating current of near constant amplitude through components C_S and L_S under full-load to short circuit condition, are obtained when the single-phase high frequency, sinusoidal waveform AC source voltage V_S is applied to the input of the resonant network.

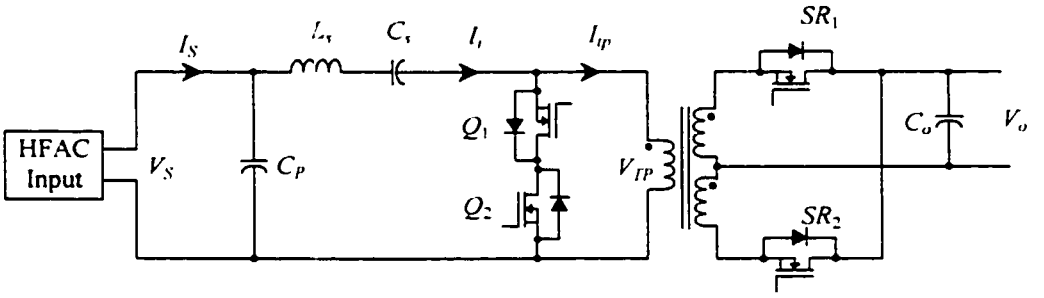


Figure2- 2: The proposed HF AC/DC converter topology.

The main switches Q_1 and Q_2 control the amount of resonant circuit output current that is needed to be rectified to achieve the desired DC output voltage and load current.

2.3 Steady State Analysis

This section describes the steady state analysis of the circuit during two switching states. The purpose of this analysis is to obtain characteristics of the converter, which aid in designing the converter. The analysis will be performed with the assumptions made below. In the analysis, the time varying variables such as the current and voltage of the principle components and devices are determined. Based on these variables, the performance of the converter can be illustrated, and the quantities such as power factor (PF), total harmonic distortion (THD) and output voltage can be obtained. These quantities are used to design the converter as presented in Chapter 5. In the analysis presented below, a set of equations solved in frequency domain as a function of the duty cycle α, the input line voltage V_S and the output power P_o.

2.3.1 Assumptions and Some Constants for the Analysis

To perform the steady state analysis, the following assumptions are made:

(i) The steady state conditions have been established and the converter is running at an input AC voltage V_S, producing the nominal output voltage V_o and delivering a power of P_o to a static load.

(ii) The gating of main switches Q_1 and Q_2, is synchronizing the gating of switches SR_1 and SR_2.

(iii) The switching frequency is constant f_s.

(iv) All components and devices have ideal properties and characteristics, i.e.,

(1) T_r: losses and leakage inductance are negligible, and the core does not saturate.

(2) L_S is a pure inductor and its losses are negligible, and its inductance is constant,

(3) C_o, C_S, and C_P: all capacitors are pure, their equivalent series resistance (ESR) and equivalent series inductance (ESL) are negligible,

(4) Q_1, Q_2, SR_1, and SR_2: all switches have negligible conduction losses, and the inherent capacitances are 0 F.

(5) The magnetizing inductance of the power transformer is so great that the magnetizing current is negligible.

(v) C_o is large enough to maintain constant and ripple free voltage during the steady state operation.

(vi) Under these assumptions, the operating principle is illustrated with key waveforms shown in Figure 2-3. Each switching cycle can be divided into two distinct intervals.

2.3.2 Operating Principle

Figure 2-3 shows the operating waveforms. At the position of cycle where $\omega_0 t = \phi$, SR_1 is conducting and the input resonant current i_r is charging the output capacitor C_o until $\omega_0 t = \phi + \alpha$ where the switches Q_1 and Q_2 are turned on. At this time, the input current is instantaneously transferred from SR_1 to Q_1 and Q_2 to end the charging period of C_o. At $\omega_0 t = \pi + \phi$ the resonant input current flowing through Q_1 and Q_2 goes

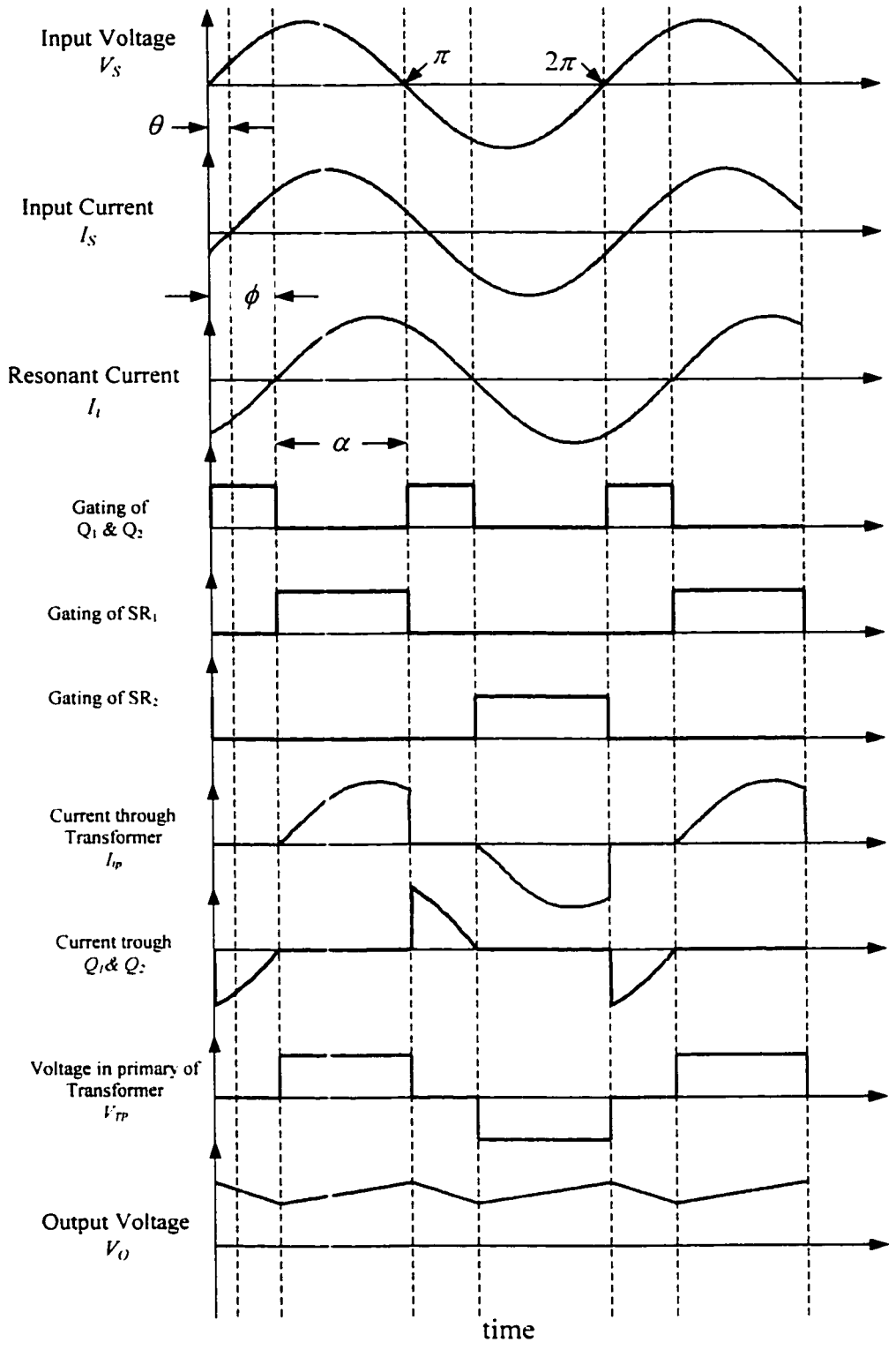


Figure2- 3: Key waveforms of the proposed converter topology. The switching transient is exaggerated.

to zero, thereby the gating signal ends. At this instant, SR_2 conducts and carries the negative input resonant current. The rectification of SR_2 changes the direction of this current at the output and starts the charging of the capacitor C_o. At $\omega_0 t = \pi + \phi + \alpha$, the current flowing through SR_2 goes to zero, because Q_1 and Q_2 are gated on and carry the current at the input.

2.3.3 Steady State Analysis of Each Interval

Under the assumptions made, the simplified n[th] harmonic equivalent circuit of the converter is shown in Figure2-4, which contains two voltage sources.

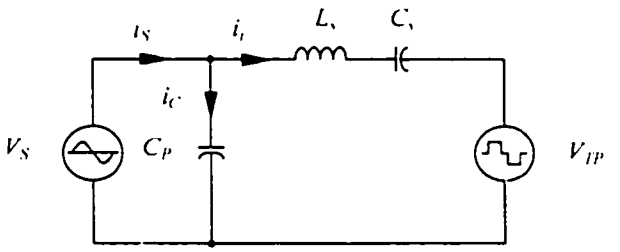
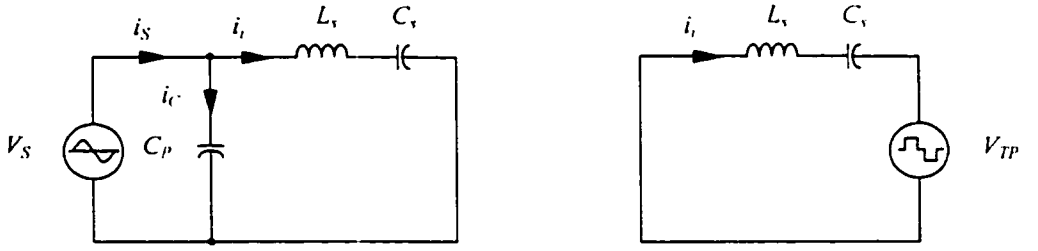


Figure2- 4: The n[th] harmonic equivalent circuit of the proposed converter



(a) **(b)**

Figure2- 5: The n[th] harmonic equivalent circuit considering separated voltage sources.

The theorem of superposition is used in obtaining the various currents and voltages of the converter circuit. Figure2-5 (a) shows the equivalent circuit with only the input source V_S, and Figure2-5 (b) shows the equivalent circuit with only the output source V_{TP}.

For convenience, some constants are defined below. In steady state, the parallel and series impedance for the fundamental and n^{th} harmonics are determined by:

$$Z_{P1} = -j\frac{1}{\omega_o C_P} = -jX_{Cp} \qquad (2\text{-}1)$$

$$Z_{Pn} = \frac{-jX_{C1}}{n} \qquad (2\text{-}2)$$

$$Z_{S1} = j\omega_o L_S - j\frac{1}{\omega_o C_S} = j(X_{Ls} - X_{Cs}) \qquad (2\text{-}3)$$

$$Z_{Sn} = njX_{Ls} - \frac{jX_{Cs}}{n} \qquad (2\text{-}4)$$

Since the input voltage source V_S is sinusoidal and contains no harmonics, the following relation presents:

$$v_S = \sqrt{2}V_S Sin(\omega_o t) \qquad (2\text{-}5)$$

The input current due to source V_S is given by:

$$i_{S1} = \frac{v_S}{Z_{t1}} = \frac{\sqrt{2}V_S Sin(\omega_o t)}{-j|Z_{t1}|} = \frac{\sqrt{2}V_S}{|Z_{t1}|}Cos(\omega_o t) \qquad (2\text{-}6)$$

where:

$$Z_{t1} = \frac{-jX_{Cp}\cdot j(X_{Ls} - X_{Cp})}{-jX_{Cp} + j(X_{Ls} - X_{Cs})} = \frac{-j[X_{Cp}(X_{Ls} - X_{Cs})]}{(X_{Ls} - X_{Cs} - X_{Cp})} \qquad (2\text{-}7)$$

The transformer primary voltage has a quasi-square waveform expressed in the

following Fourier series:

$$v_{TP} = \sum_{n=1,3}^{\infty} \frac{4V_{TP}}{n\pi} Sin\frac{n\alpha}{2} Sin(n\omega_o t - \frac{n(\alpha + 2\phi - \pi)}{2}) \qquad (2\text{-}8)$$

The input current due to source v_{TP} is given by:

$$i_{S2} = \sum_{n=1,3}^{\infty} \frac{4V_{TP}}{n\pi|Z_{Sn}|} Sin\frac{n\alpha}{2} Cos(n\omega_o t - \frac{n(\alpha + 2\phi - \pi)}{2}) \qquad (2\text{-}9)$$

The total input current is given by:

$$i_S = i_{S1} + i_{S2} = \frac{\sqrt{2}V_S}{|Z_{t1}|} Cos(\omega_o t) + \sum \frac{4V_{TP}}{n\pi|Z_{Sn}|} Sin\frac{n\alpha}{2} Cos(n\omega_o t - \frac{n(\alpha + 2\phi - \pi)}{2})$$

$$i_S = \frac{\sqrt{2}V_S}{|Z_{t1}|} Cos(\omega_o t) + \sum \frac{4V_O}{n\pi|Z_{Sn}|} \frac{N_1}{N_2} Sin\frac{n\alpha}{2} Cos(n\omega_o t - \frac{n(\alpha + 2\phi - \pi)}{2}) \qquad (2\text{-}10)$$

(i) Determination of Angle ϕ:

The following equation shows the current in the series branch of resonant network due to the source V_S:

$$i_{t1} = \frac{v_S}{Z_{S1}} = \frac{\sqrt{2}V_S Sin(\omega_o t)}{j|Z_{S1}|} = \frac{-\sqrt{2}V_S}{|Z_{S1}|} Cos(\omega_o t) \qquad (2\text{-}11)$$

and the current in the same branch due to the output source v_{TP} is given by:

$$i_{t2} = \sum_{n=1,3}^{\infty} \frac{4V_{TP}}{n\pi|Z_{Sn}|} Sin\frac{n\alpha}{2} Cos(n\omega_o t - \frac{n(\alpha + 2\phi - \pi)}{2}) \qquad (2\text{-}12)$$

so the resonant current in this branch according to theorem of superposition is:

$$i_t = i_{t1} + i_{t2} = \frac{-\sqrt{2}V_S}{|Z_{S1}|} Cos(\omega_o t) + \sum \frac{4V_O}{n\pi|Z_{Sn}|} \frac{N_1}{N_2} Sin\frac{n\alpha}{2} Cos(n\omega_o t - \frac{n(\alpha + 2\phi - \pi)}{2}) \qquad (2\text{-}13)$$

The resonant Current is $i_i = 0$ at $\omega_o t = \phi$, therefore, from Equation (2-13) the following relations are obtained:

$$\frac{-\sqrt{2}V_S}{|Z_{S1}|}Cos\phi + \sum \frac{4V_O}{n\pi|Z_{Sn}|}\frac{N_1}{N_2}Sin\frac{n\alpha}{2}Cos(n\phi - \frac{n(\alpha+2\phi-\pi)}{2}) = 0$$

$$\frac{\sqrt{2}V_S}{|Z_{S1}|}Cos\phi = \sum \frac{4V_O}{n\pi|Z_{Sn}|}\frac{N_1}{N_2}Sin\frac{n\alpha}{2}Cos\frac{n(\pi-\alpha)}{2}$$

$$Cos\phi = \sum \frac{2\sqrt{2}}{n\pi}\frac{V_O}{V_S}\frac{Z_{S1}}{|Z_{Sn}|}\frac{N_1}{N_2}Sin\frac{n\alpha}{2}Cos\frac{n(\pi-\alpha)}{2} \qquad (2\text{-}14)$$

For a given control angle α, the value of ϕ would have been calculated by using Equation (2-14), if the value of $\frac{V_O}{V_S}$ were known. The value of $\frac{V_O}{V_S}$ can be obtained by setting the input power equal to the output power.

Since the input voltage source contains no harmonics, the product of the fundamental input current, the input voltage and the fundamental cosine angle between the two, determines the input power. This leads us to the next sub-section.

(ii) Output Voltage Control:

Output voltage control is provided by controlling the current controller pulse width (gating of Q_1 and Q_2) other word angle α.

By substituting n = 1, the fundamental time-varying input current from Equation (2-10) is given by:

$$i_{Sf} = \frac{\sqrt{2}.V_S}{|Z_{11}|}Cos(\omega_i t) + \frac{4V_O}{\pi|Z_{S1}|}\frac{N_1}{N_2}Sin\frac{\alpha}{2}Cos(\omega_o t - \frac{\alpha+2\phi-\pi}{2}) \qquad (2\text{-}15)$$

The fundamental time-varying current from Equation (2-15) can be simplified by:

$$i_S = C.Sin(\omega_0 t + \theta) \tag{2- 16}$$

and

$$A.Cos(x) + B.Sin(x) = C.Sin(\omega_0 t + \theta) \tag{2- 17}$$

where: $C = \sqrt{A^2 + B^2}$ and $\theta = \tan^{-1}(A/B)$, it is carried out that the A and B parameters are:

$$A = \frac{\sqrt{2}}{|Z_{t1}|} V_S + \frac{4V_O}{\pi . Z_{S1}|} \frac{N_1}{N_2} Sin\frac{\alpha}{2} Sin\frac{2\phi + \alpha}{2} \tag{2- 18}$$

$$B = \frac{-4V_O}{\pi . |Z_{S1}|} \frac{N_1}{N_2} Sin\frac{\alpha}{2} Cos\frac{2\phi + \alpha}{2} \tag{2- 19}$$

The input power is given by: $P_i = V_S I_S Cos(\theta) = V_S \frac{C}{\sqrt{2}} Cos(\theta) = \frac{V_S}{\sqrt{2}} B$, therefore:

$$P_i = \frac{2\sqrt{2}}{\pi |Z_{S1}|} \frac{N_1}{N_2} V_O V_S Sin\frac{\alpha}{2} Cos\frac{2\phi + \alpha}{2} \tag{2- 20}$$

The output power is given by:

$$P_O = \frac{V_O^2}{R_O} \tag{2- 21}$$

Since the input power is equal to the output power, the following relation is obtained from Equation (2-20) and Equation (2-21):

$$\frac{V_O^2}{R_O} = \frac{-2\sqrt{2}}{\pi |Z_{S1}|} V_O V_S \frac{N_1}{N_2} Sin\frac{\alpha}{2} Cos(\frac{2\phi + \alpha}{2})$$

or

$$\frac{V_O}{V_S} = \frac{-2\sqrt{2}}{\pi|Z_{S1}|}\frac{N_1}{N_2} R_O . Sin\frac{\alpha}{2} Cos(\frac{2\phi+\alpha}{2}) \qquad (2\text{-}22)$$

Substituting $\frac{V_O}{V_S}$ from Equation (2-22) into Equation (2-14), we have:

$$\tan\phi = \frac{[\frac{16}{\pi^2}(\frac{N}{N_2})^2 Sin\alpha \sum_{n=1,3}^{\infty} \frac{1}{n}\frac{R_0}{|Z_{Sn}|} Sin\frac{n\alpha}{2} Cos\frac{n(\pi-\alpha)}{2}]+1}{\frac{8}{\pi^2}(\frac{N_1}{N_2})^2 Sin^2\frac{\alpha}{2} \sum_{n=1,3}^{\infty} \frac{1}{n}\frac{R_0}{|Z_{Sn}|} Sin\frac{n\alpha}{2} Cos\frac{n(\pi-\alpha)}{2}} \qquad (2\text{-}23)$$

For a given angle α, output load R_0 and impedance Z_S the value of ϕ is obtained. Figure2-6 shows the graph of control angle α versus resonant current angle ϕ for different values of Z_S. Figure 2-7 shows the output voltage versus control angle. For different values of $\frac{N_1}{N_2}$ and Z_{S1} the converter output voltage has been drawn. The lower the series impedance is, the higher the output voltage is. All graphs are done in Mathcad.

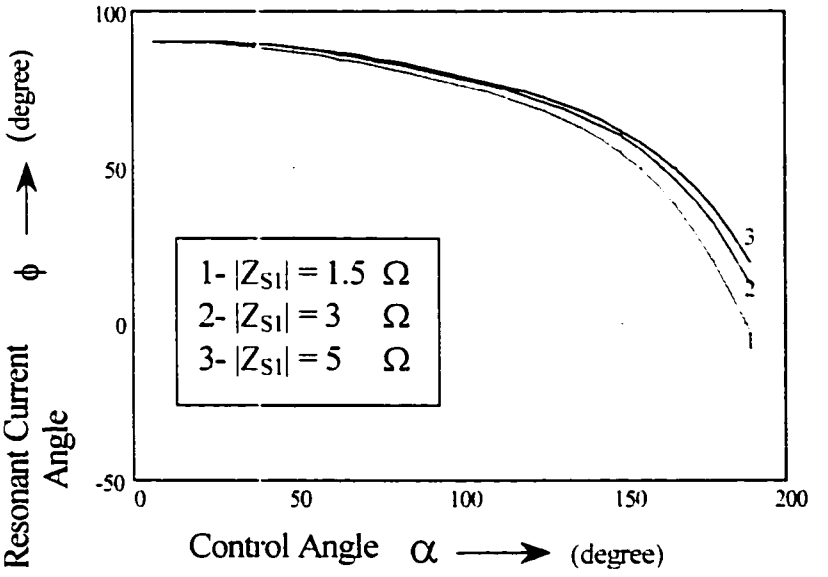


Figure2- 6: Control angle versus resonant angle

(iii) Input Current Total Harmonic Distortion:

The total harmonic distortion (THD) of the input current is defined as:

$$THD = \frac{\sqrt{\sum_{n\neq 1} I_n^{\,2}}}{I_1}$$

Therefore:

$$THD = \frac{4.V_0}{\pi.C}\frac{N_1}{N_2}\sqrt{\sum_{n\neq 1}\left(\frac{1}{n.|Z_{Sn}|}Sin\frac{n\alpha}{2}\right)^2} \qquad (2\text{-}24)$$

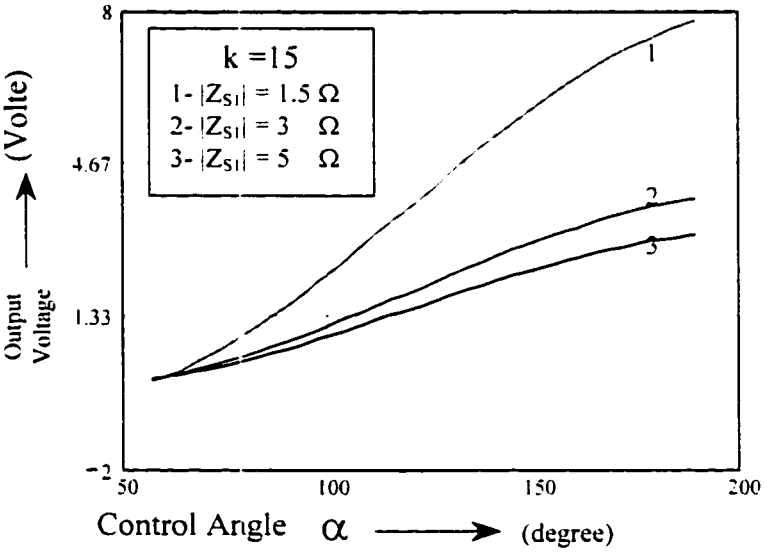


Figure2- 7: Output voltage versus control angle

Figure2-8 shows THD for different values of series and parallel impedance. According to the graphs, for greater values of α, we have less THD. Due to the fact that the operating point is around α =120°, a very low THD is attainable.

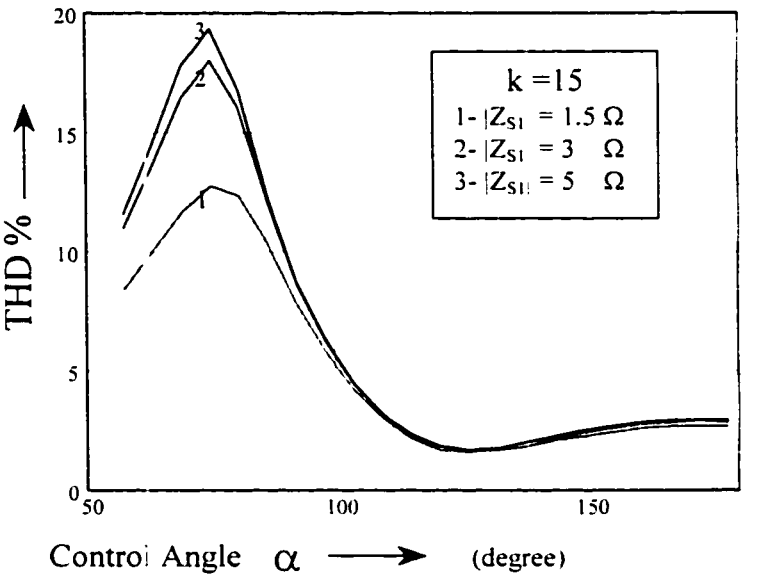


Figure2- 8: Total Harmonic Distortion

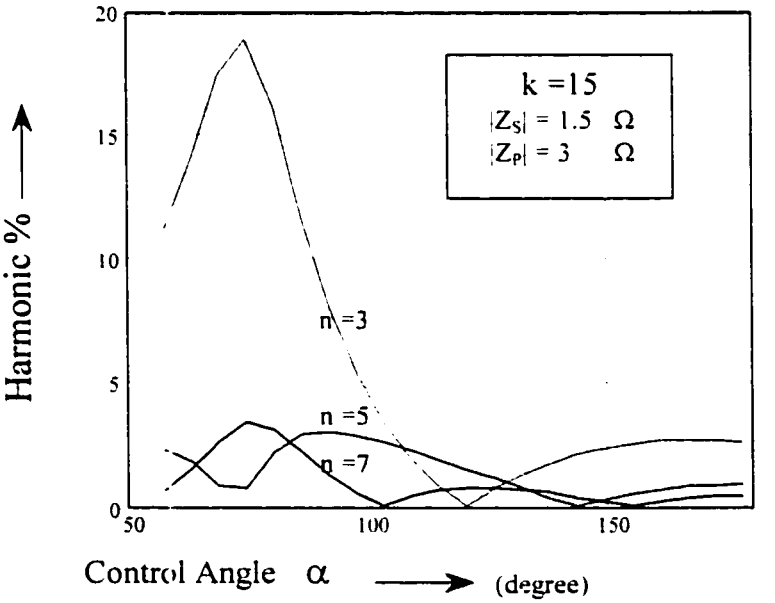


Figure2- 9: The Harmonics % of input current

Figure2-9 shows the %Harmonic of input current. As it is expected, the 3rd harmonic is the least at α =120°, and very severe at the other points. After that, the 5th harmonic is the most severe one and the rest are less.

(iv) Input Power Factor:

The converter input power factor is given by:

$$PF = -\frac{Cos\theta}{\sqrt{1+THD^2}} \qquad (2\text{-}25)$$

Figure 2-10 shows the power factor versus the control angle. As expected, the power factor is close to unity in almost all condition.

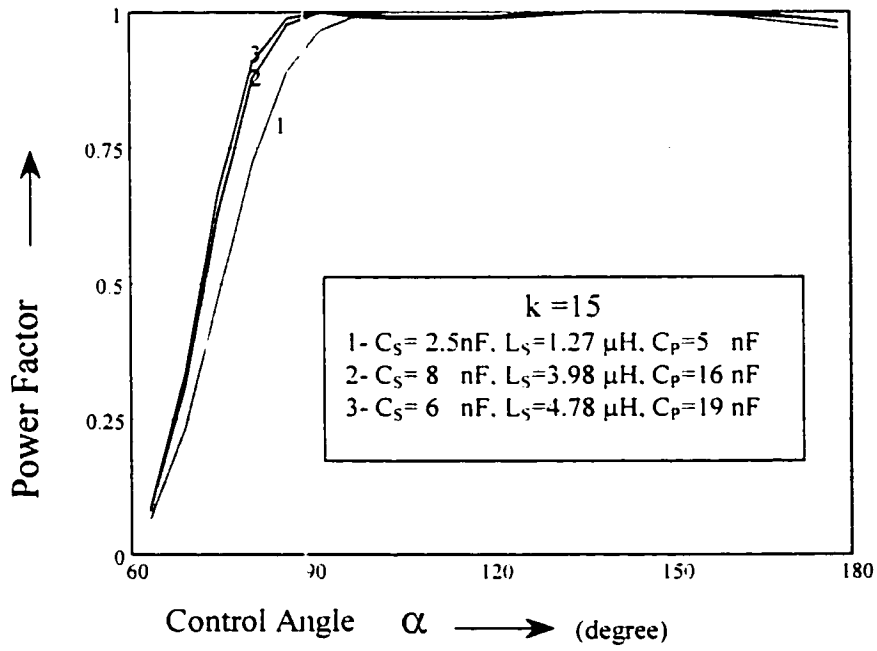


Figure2- 10: Power Factor versus control angle

2.4 Simulation Results

Simulation of the proposed converter topology is performed with PSIM software. This simulation is first done without considering the leakage inductance to verify the concept of analysis carried out in this chapter, and to find out whether the statements are correct. Table2-1 shows the principle parameters of the circuit used in simulation.

Table2- 1: Principle Parameters of the Simulated Circuit without considering the leakage inductance

Parameter	Value	Parameter	Value
V_S	30 V rms	C_o	480 μF
P_o	80 W	C_S	6.8 nF
f_S	2 MHz	L_S	4.4 μH
k	15:1:1	C_P	20 nF

Figure 2-11 shows the input voltage and current along with the output voltage. As expected, the input voltage and current are almost in the same phase, so the power factor is close to unity and that is what expected. To find out the current and voltage in different branches in the converter, it was assumed that voltage in primary side of the transformer to be quasi-square wave. Figure 2-12 shows the voltage in primary and secondary of the transformer, and it proves that the assumption made is right.

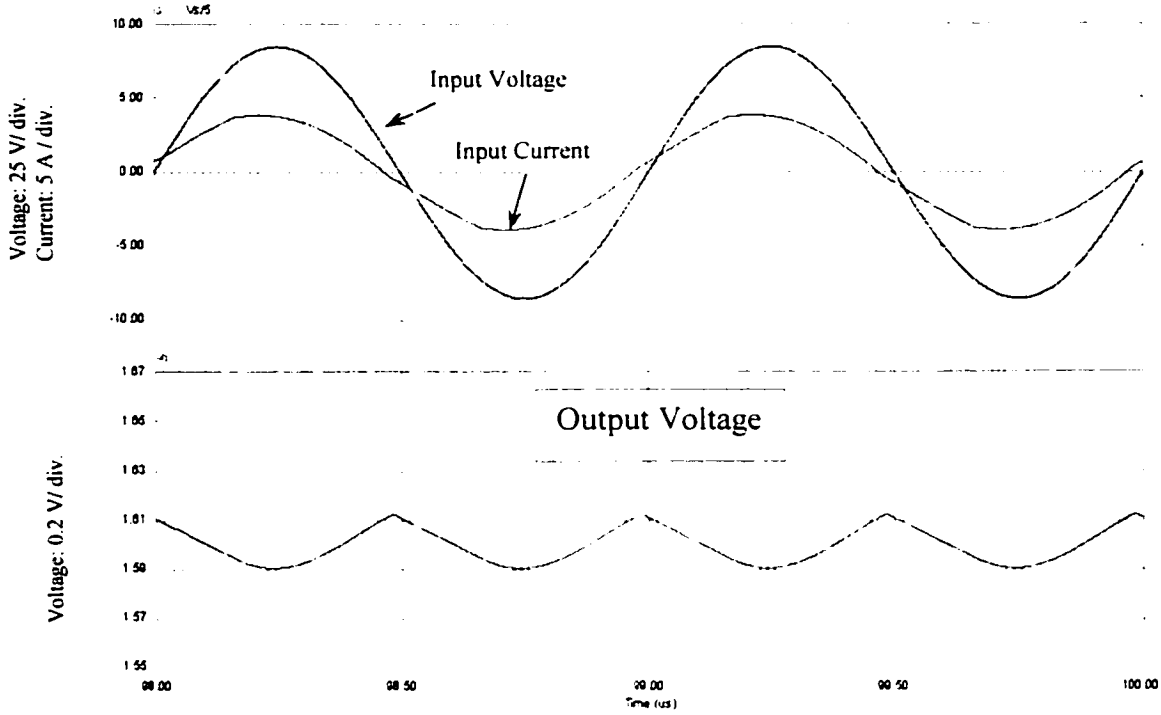


Figure2- 11: The input voltage and current and output voltage of converter

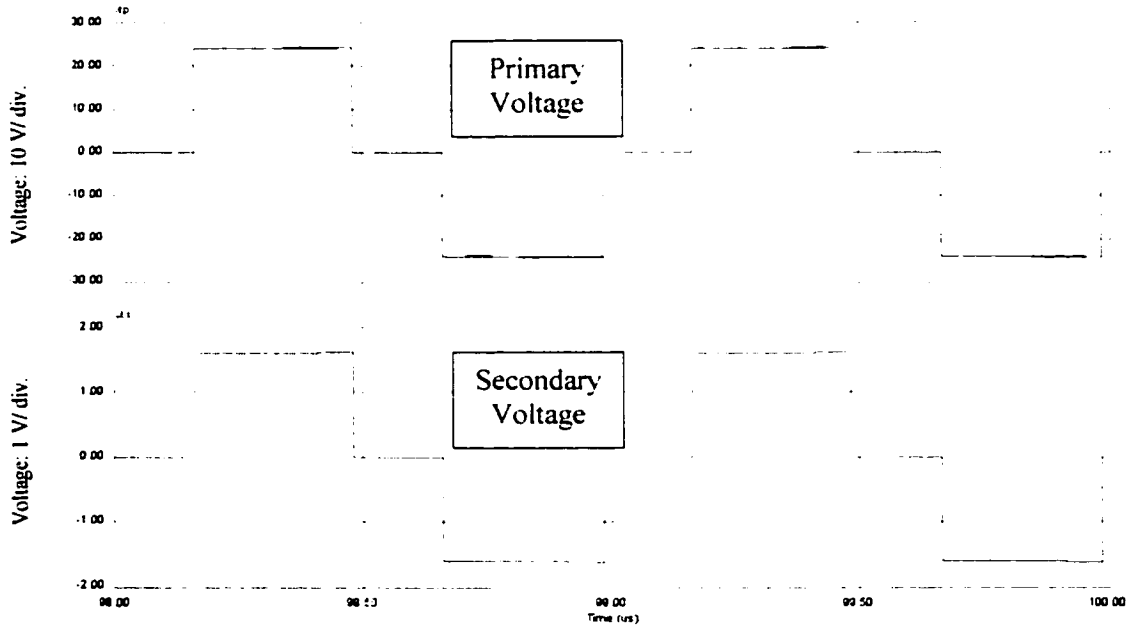


Figure2- 12: The voltages in primary and secondary of transformer

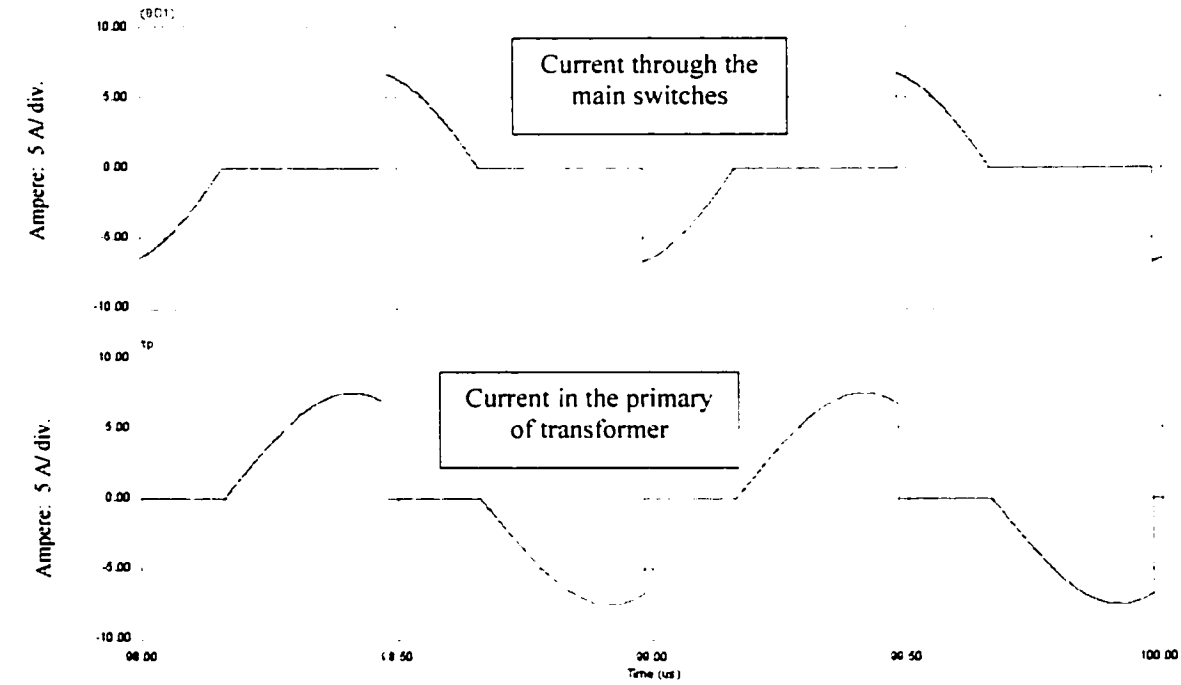


Figure2- 13: Current in the switches and primary of transformer

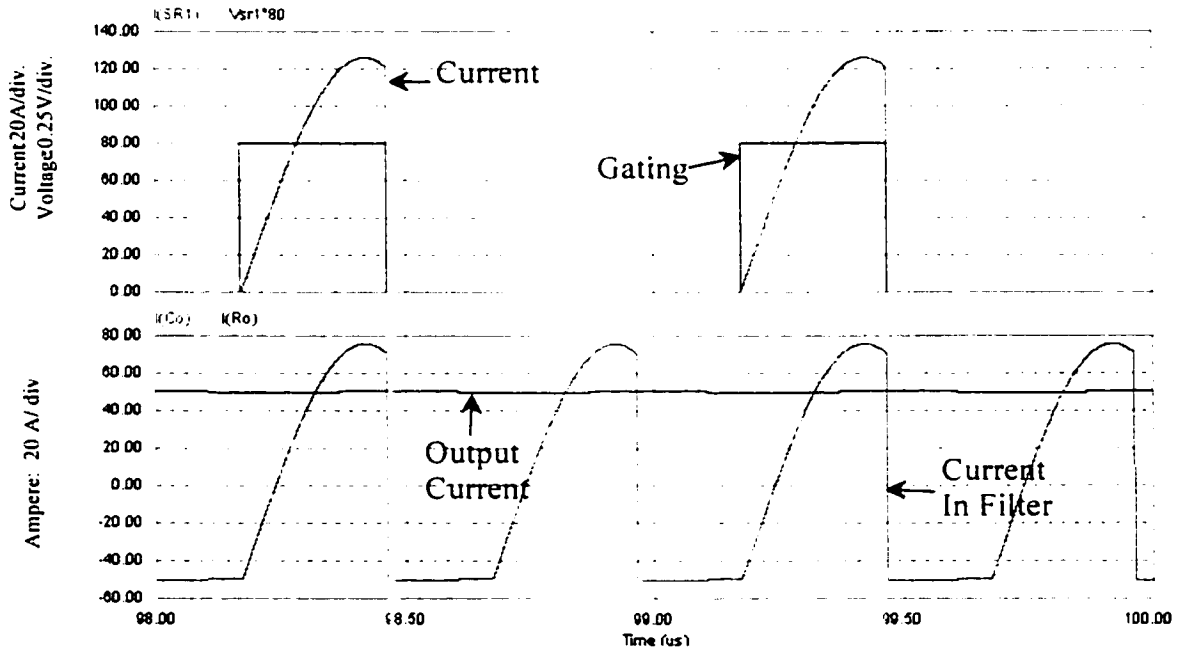


Figure2- 14: UP; Current in SR_1 and Gating of SR_1
Down; Current in C_o and Output Current

Figure2-13 shows the current in the switches and primary of the transformer. Due to the fact that the transformer considered to be ideal without any leakage inductance, the current in the primary side of the transformer has a sharp fall, and in the switches has a sharp rise, which in practice it does not occur. This is discussed later in the next chapter.

Figure 2-14 shows the current in the secondary, gating of synchronous rectifier, output current and current in the output filter capacitor.

The next simulation is done with considering the leakage inductance, resistance and inductance in series with the switches, ESL and ESR in series with the output filter capacitor without changing any parameters used in previous simulation to compare the result with the simplified simulation. Table 2-2 shows the principle parameters of the circuit used in simulation.

Table2- 2: Principle Parameters of the Simulated Circuit with considering the leakage inductance

Parameter	Value	Parameter	Value
V_S	30 V rms	C_o	480 µF
f_o	1 MHz	C_S	6.8 nF
f_S	2 MHz	L_S	4.4 µH
k	15:1:1	C_P	110 nF
R_{ds} (SR_1 & SR_2)	3 mΩ	R_{ds} (Q_1 & Q_2)	10 mΩ
L_{sw} (SR_1 & SR_2)	2 nH	L_{sw} (Q_1 & Q_2)	10 nH
L_{lk}	0.5 µH	P_o	80 W

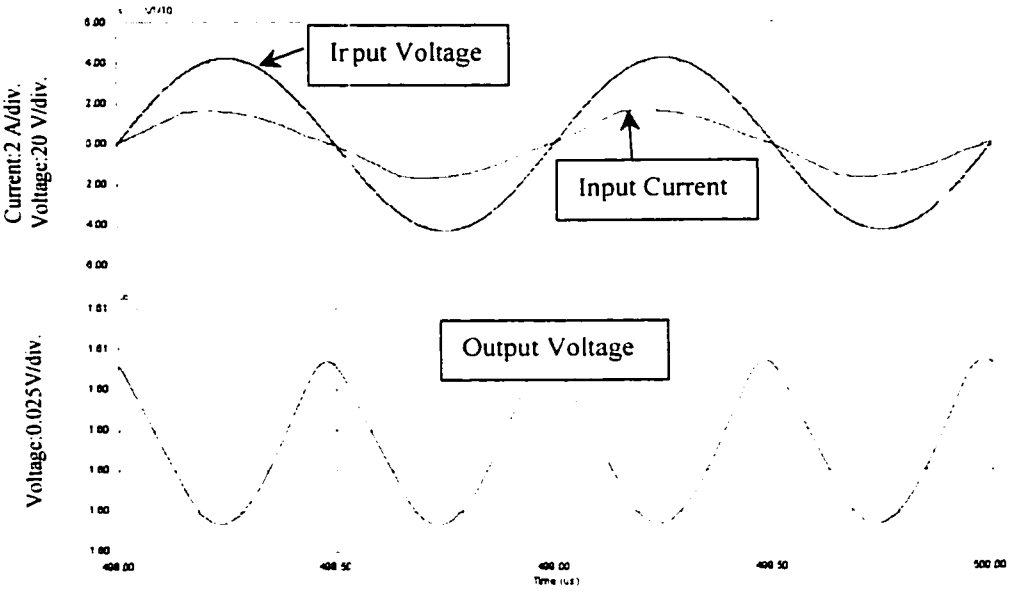


Figure2- 15: The input voltage and current (up) and output voltage of converter (down)

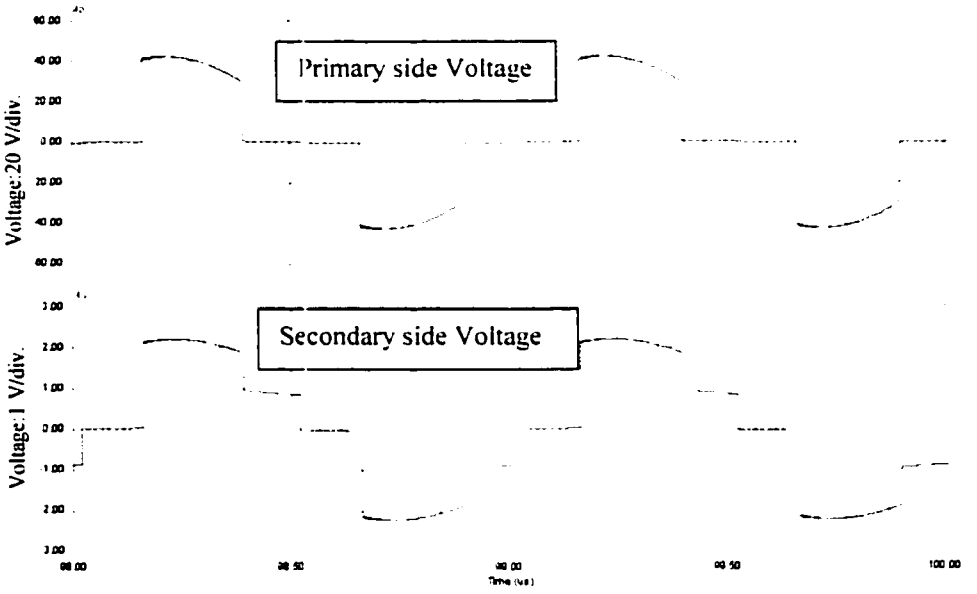


Figure2- 16: The voltages in the primary (up) and secondary of transformer (down)

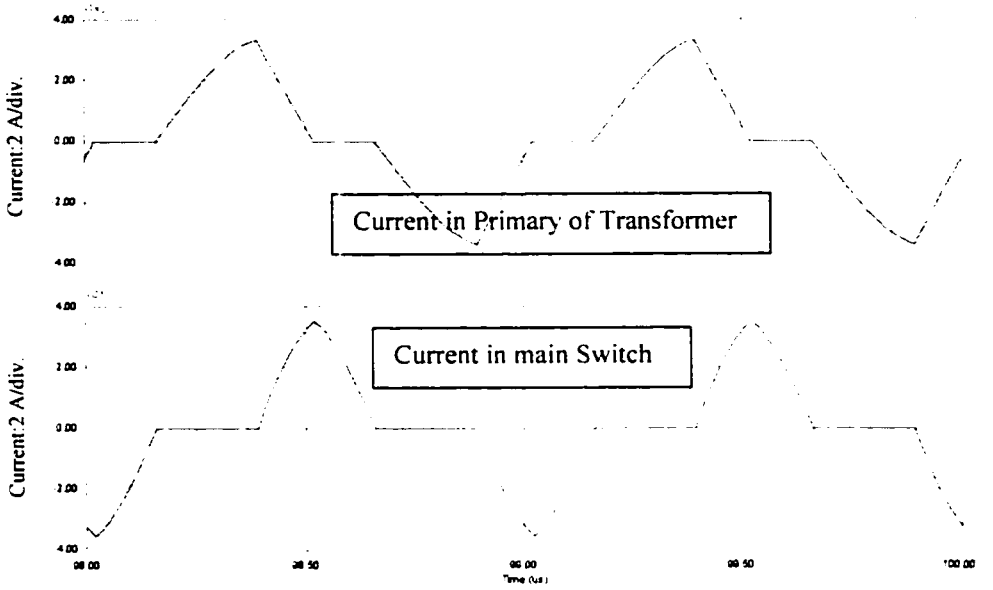


Figure2- 17: Current in primary of transformer (down) and the main switches (up)

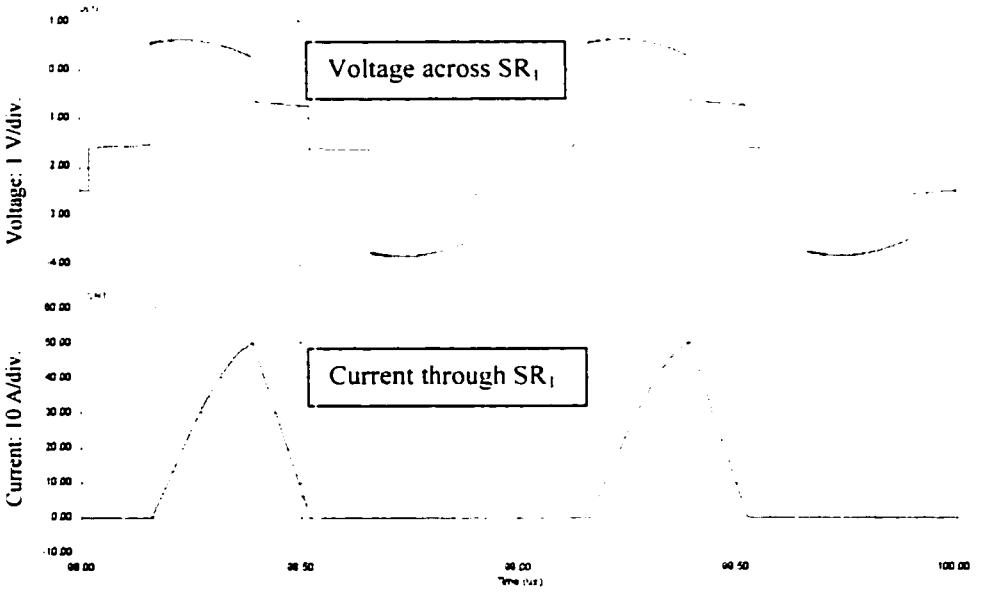


Figure2- 18: Current and voltage across the synchronous rectification SR_1

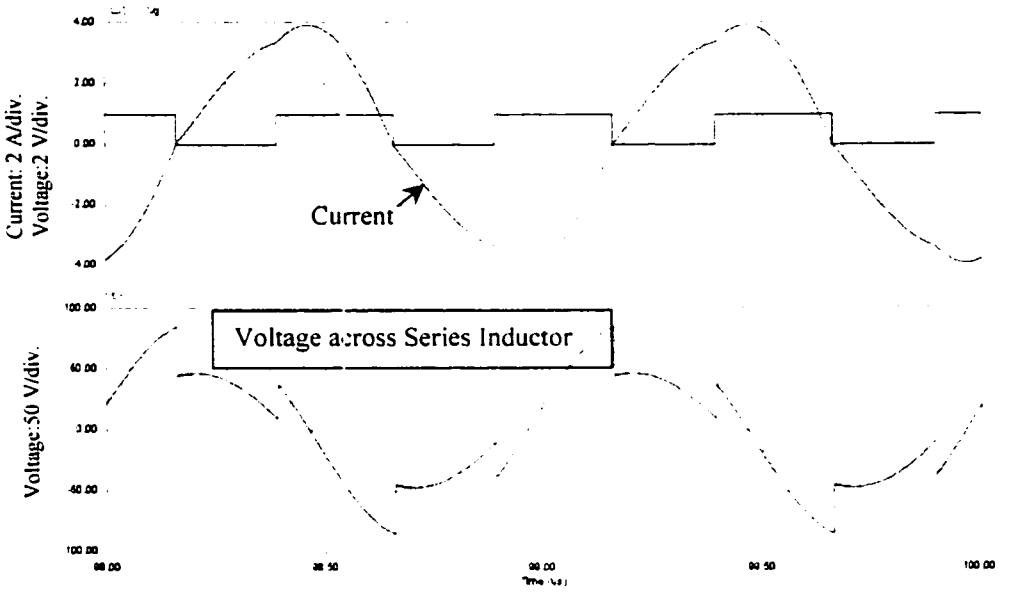


Figure2- 19: Current in resonant series branch, gating of the main switches (up) and voltage across resonant inductor (down)

2.5 Conclusion

Simulation of the proposed converter topology is performed with PSIM software without considering the leakage inductance and with considering it. According to simulation results given in Figure 2-15 to Figure 2-19, it is found that the voltage across the primary side of the transformer was not a quasi-square wave anymore. Also the current in this side didn't have a sharp fall because of the presence of leakage inductance, which is severe in very high frequency. The other important issue is the input current, which was not at the same phase as it was before in the simplified case. Therefore the power factor was not as it is calculated, so the parallel capacitor in the resonant tank is increased to shift the input current and attain better power factor. To get the same output

voltage, either the gating of main switches has to be decreased or the series inductor in resonant network has to be reduced, which has to be compromised. Based on all these dissimilarity, to assume a quasi-square wave in the primary of the transformer, on which the simplified analysis was based, is not valid anymore. Therefore this voltage has to be replaced by a new model with considering the leakage inductance, which leads us to the next chapter.

CHAPTER 3

EFFECT OF LEAKAGE INDUCTANCE

3.1 Introduction

This chapter presents the mathematical analyses of the proposed converter topology with considering the leakage inductance in the primary side of the transformer as well as the inductor and resistor in series with the switches. As seen from the chapter 2, it is assumed that the voltage in the primary side of the transformer is a quasi-square wave, to find out the voltage and current in principle devices and components of converter. But in practice, due to a very high operating frequency, the leakage inductance has significant impact on the performance of the converter and it has to be taken into account in the analyses.

The outline of this chapter is as follows. In Section 3.2, the converter behavior is described under real conditions. In section 3.3, the steady state is performed and an equivalent voltage source to the primary of transformer derived. In section 3.3, the simulation is performed to prove our analysis done in this chapter and to make a comparison between these two cases and the simulation. Finally in section 3.5, a conclusion is drawn.

3.2 Circuit Description

Figure3-1 shows the equivalent circuit of the circuit by considering the leakage inductance. The goal in next section is to find out a voltage source to be placed after

resonant network. Therefore, in Section 3.3, an equivalent voltage source to the primary of the transformer is presented.

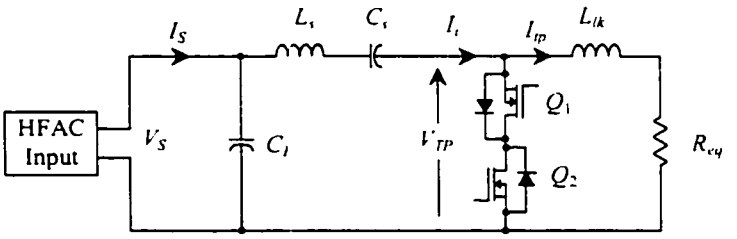


Figure3- 1: The equivalent circuit of proposed topology with considering leakage inductance

As can be seen in Figure 3-2, the equivalent circuit of proposed topology consists of a resistive load and an inductive load. The resistive load is the resistance in series with the synchronous rectifiers and the load all reflected to the primary side. The inductive load consists of the secondary leakage inductance of the transformer plus inductance in series with synchronous rectifiers all reflected to the primary side added to the leakage inductance in the primary side of the transformer.

3.3 Steady State Analysis

This section describes the steady state analyses of the circuit during two switching states. The purpose of this analysis is to obtain the practical characteristics of the converter, which aids in designing the converter.

The analysis is performed with the assumptions made below. Although we take into account the effect of leakage inductance, there is still some assumptions made. In the

analysis, the time varying variables such as the current and voltage of the principle components and devices are determined. Based on these variables, the performance of the converter can be illustrated, and the quantities such as power factor, total harmonic distortion and output voltage can be obtained. These quantities are used to compare with results from Chapter 2, and to design the converter as presented in Chapter 5.

In the analysis presented below, a set of equations is solved in time domain and frequency domain as a function of the control angle α, the input line voltage V_S and the output power P_o.

3.3.1 Assumptions and Some Constants For the Analysis

Although the leakage inductance is considered in the analysis, but to perform the steady state analysis, the following assumptions are still made:

(i) The steady state conditions have been established and the converter is running at an input AC voltage V_S, producing the nominal output voltage V_o and delivering a power of P_o to a static load.

(ii) The gating of main switches Q_1 and Q_2, is synchronizing the gating of switches SR_1 and SR_2,

(iii) The switching frequency is constant f_s.

(iv) All components and devices have ideal properties and characteristics, i.e.,

(1) T_r: losses are negligible, and the core does not saturate,

(2) L_S Is a pure inductor and its losses are negligible, and its inductance is constant,

(3) C_o, C_S, and C_r: all capacitors are pure capacitors, their equivalent series resistance (ESR) and equivalent series inductance (ESL) are negligible,

(4) Q_1, Q_2, SR_1, and SR_2: all switches have negligible conduction losses, and the inherent capacitances are 0 F,

(5) The magnetizing inductance of the power transformer is so great that the magnetizing current is negligible.

(v) C_O is large enough to maintain constant and ripple free voltage during the steady state operation.

Under these assumptions, the operating principle is illustrated with key waveforms shown in Figure 3-2.

3.3.2 Operating Principle

Figure 3-2 shows the operating waveforms. At the position of cycle where $\omega_0 t = \phi$, SR_1 is conducting and the input resonant current i_r is charging the output capacitor C_o until $\omega_0 t = \phi + \alpha$ where the switches Q_1 and Q_2 are turned on. At this time, the input current has to be instantaneously transferred from SR_1 to Q_1 and Q_2 to end the charging period of C_o. However, due to the leakage inductance in the primary side of the transformer, this current does not go to zero instantaneously. At $\omega_0 t = \pi + \phi$ the resonant input current flowing through Q_1 and Q_2 goes to zero, thereby the gating signal ends. At this instant, SR_2 conducts and carries the negative input resonant current. The rectification of SR_2 changes the direction of this current at the output and starts the charging of the capacitor

C_o. At $\omega_0 t = \pi + \phi + \alpha$, the current flowing through SR_2 must go to zero, because Q_1 and Q_2 are gated on, but the leakage inductance does not allow the current through it to reach zero instantaneously.

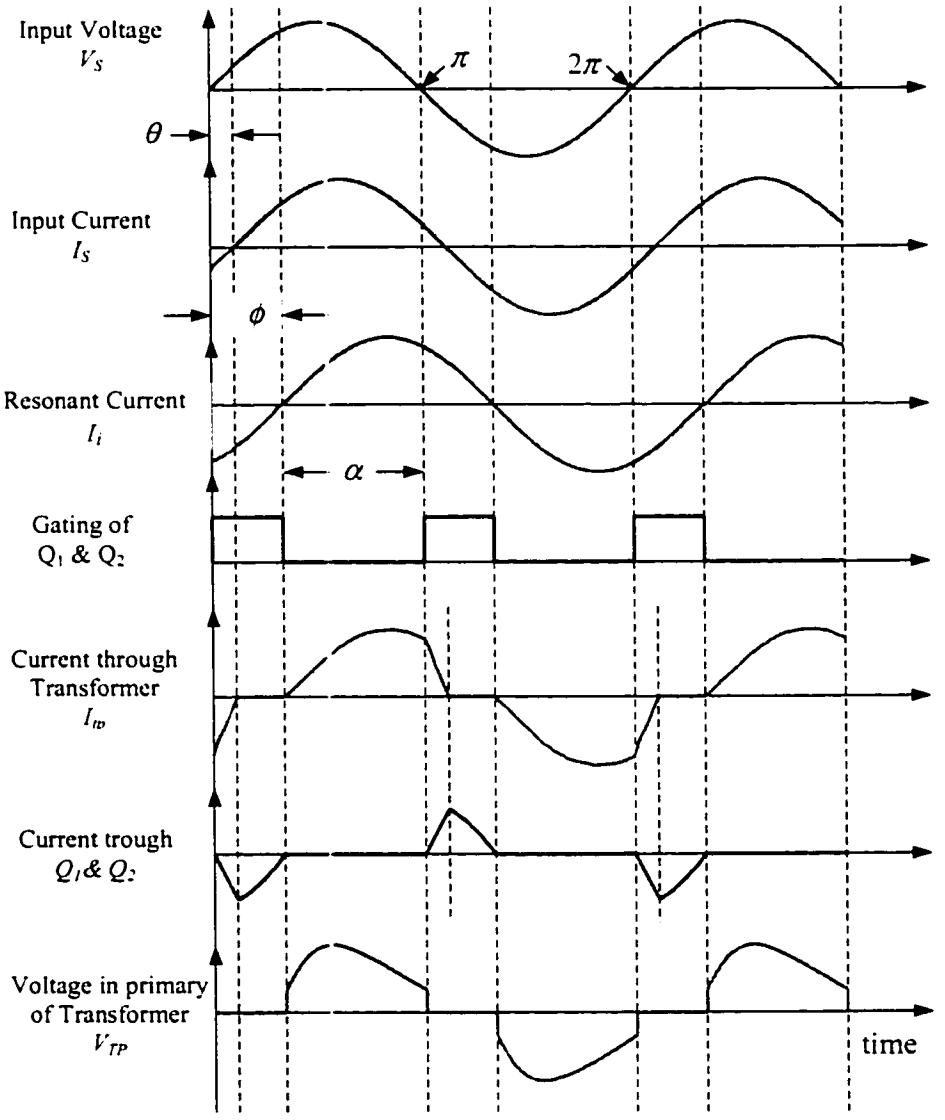


Figure3- 2: Key waveforms of the proposed converter topology. The switching transient is exaggerated.

3.3.3 Steady State Analysis

Under the assumptions made, the simplified n^{th} harmonic equivalent circuit of the converter is shown in Figure 3-3, which contains two voltage sources.

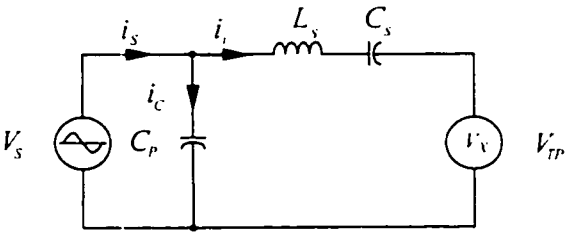


Figure3- 3: The n^{th} harmonic equivalent circuit considering the leakage inductance

The theorem of superposition is used in obtaining the various currents and voltages of the converter circuit. Figure 3-4 (a) shows the equivalent circuit with only the input source V_S.

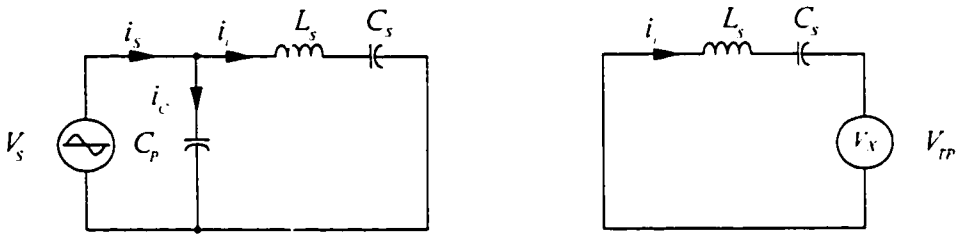


Figure3- 4: The n^{th} harmonic equivalent circuit considering separated voltage sources

Figure 3-4 (b) shows the equivalent circuit with the only output source V_{TP}. Therefore, we have to first find out the voltage across the primary of the transformer.

When the main switches are off, the current in the series resonant branch is expressed by:

$$v_S(t) = (L_S + L_{lk})\frac{di_1}{dt} + \frac{1}{C_S}\int i_1 dt + R_{eq} i_1 \qquad (3\text{-}1)$$

where

$$v_S = \sqrt{2} V_S Sin(\omega_o t) \qquad (3\text{-}2)$$

A particular answer for Equation (3-1) is:

$$i_1 = E.Cos(\omega_o t) + F.Sin(\omega_o t) \qquad (3\text{-}3)$$

where

$$E = \frac{\sqrt{2}.V_S.\omega_o}{L_S + L_{lk}}[(\omega_S^2 - \omega_o^2)^2 + (2.\xi.\omega_o)^2]^{-1}.(\omega_S^2 - \omega_o^2) \qquad (3\text{-}4)$$

$$E = \frac{\sqrt{2}.V_S.\omega_o}{L_S + L_{lk}}[(\omega_S^2 - \omega_o^2)^2 + (2.\xi.\omega_o)^2]^{-1}.(2.\xi.\omega_o) \qquad (3\text{-}5)$$

and

$$\omega_S = \sqrt{\frac{1}{C_S(L_S + L_{lk})}} \qquad (3\text{-}6)$$

$$\xi = \frac{R_{eq}}{2(L_S + L_{lk})} \qquad (3\text{-}7)$$

The voltage across the primary side of the transformer can be derived by:

$$v_X = L_{lk}\frac{di_1}{dt} + R_{eq} i_1 \qquad (3\text{-}8)$$

This voltage can be expressed by:

$$v_X = M.Cos(\omega_o t) + N.Sin(\omega_o t) \qquad (3\text{-}9)$$

where

$$M = R_{eq}.E + L_{lk}.F.\omega_o \tag{3- 10}$$

$$N = R_{eq}.F - L_{lk}.E.\omega_o \tag{3- 11}$$

In all the above derived equations, we have:

$$R_{eq} = \frac{8}{\pi^2}.(\frac{N_1}{N_2})^2(R_o + R_{SR_1}) \tag{3- 12}$$

Finally, the voltage in the primary side of the transformer can be expressed as:

$$v_{TP}(t) = \begin{cases} v_X & \phi < t < \phi + \alpha \\ 0 & \phi + \alpha < t < \phi + \pi \\ v_X & \phi + \pi < t < \phi + \pi + \alpha \\ 0 & \phi + \pi + \alpha < t < \phi + 2\pi \end{cases} \tag{3- 13}$$

For convenience, some constants are defined below. In the steady state, the parallel and series impedance for the fundamental and n^{th} harmonics are determined by:

$$Z_{S1} = j\omega_o L_S - j\frac{1}{\omega_o C_S} = j(X_{Ls} - X_{Cs}) \tag{3- 14}$$

$$Z_{Sn} = njX_{Ls} - \frac{jX_{Cs}}{n} \tag{3- 15}$$

$$Z_{P1} = -j\frac{1}{\omega_o C_P} = -jX_{Cp} \tag{3- 16}$$

$$Z_{Pn} = \frac{-jX_{Cp}}{n} \tag{3- 17}$$

Since the input voltage source V_S is sinusoidal and contains no harmonics, it is presented by the Equation (3-2).

The input current due to source V_S is given by:

$$i_{S1} = \frac{v_S}{Z_{t1}} = \frac{\sqrt{2}V_S Sin(\omega_o t)}{-j|Z_{t1}} = \frac{\sqrt{2}V_S}{|Z_{t1}|} Cos(\omega_o t) \qquad (3\text{-}18)$$

Where:

$$Z_{t1} = \frac{-jX_{Cp}.j(X_{Ls} - X_{Cp})}{-jX_{Cp} + j(X_{Ls} - X_{Cs})} = \frac{-j[X_{Cp}(X_{Ls} - X_{Cs})]}{(X_{Ls} - X_{Cs} - X_{Cp})} \qquad (3\text{-}19)$$

The Fourier series of the transformer primary voltage can be expressed by:

$$v_{TP} = \sum_{n=1,2}^{\infty} (a_n.Cos(n\omega_o t) + b_n.Sin(n\omega_o t)) \qquad (3\text{-}20)$$

where

$$a_n = \frac{1}{\pi} \int_{\phi}^{\phi+2\pi} v_{TP}(t).Cos(n\omega_o t)dt$$

$$= \frac{Q}{2\pi}\{\frac{-Cos[(n+1)(\phi+\alpha)-\beta]}{n+1} + \frac{-Cos[(1-n)(\phi+\alpha)-\beta]}{1-n} + \frac{Cos[(n+1)\phi-\beta]}{n+1}$$

$$+ \frac{Cos[(1-n)\phi-\beta]}{1-n} + \frac{-Cos[(1+n)(\phi+\pi+\alpha)-\beta]}{1+n} + \frac{-Cos[(1-n)(\phi+\pi+\alpha)-\beta]}{1-n}$$

$$+ \frac{Cos[(n+1)(\phi+\pi)-\beta]}{n+1} + \frac{Cos[(1-n)(\phi+\pi)-\beta]}{1-n} \qquad (3\text{-}21)$$

and

$$b_n = \frac{1}{\pi} \int_{\phi}^{\phi+2\pi} v_{TP}(t).Sin(n\omega_o t)dt$$

$$= \frac{Q}{2\pi}\{\frac{Sin(1-n)(\phi+\alpha)-\beta]}{1-n} + \frac{-Sin[(1+n)(\phi+\alpha)-\beta]}{1+n} + \frac{-Sin[(1-n)\phi-\beta]}{1-n}$$

$$+ \frac{Sin[(n+1)\phi-\beta]}{n+1} + \frac{Sin[(1-n)(\phi+\pi+\alpha)-\beta]}{1-n} + \frac{-Sin[(1+n)(\phi+\pi+\alpha)-\beta]}{1+n}$$

$$+ \frac{-Sin[(1-n)(\phi+\pi)-\beta]}{1-n} + \frac{Sin[(1+n)(\phi+\pi)-\beta]}{1+n} \qquad (3\text{-}22)$$

where

$$Q = \sqrt{M^2 + N^2} \tag{3- 23}$$

The input current due to source v_{TP} is given by:

$$i_{S2} = \sum_{n=1,2}^{\infty} \left(\frac{a_n}{|Z_{Sn}|} Cos(n\omega_o t) + \frac{b_n}{|Z_{Sn}|} Sin(n\omega_o t)\right) \tag{3- 24}$$

The total input current is given by:

$$i_S = \frac{\sqrt{2}V_S}{|Z_{S1}|} Cos(\omega_o t) + \sum_{n=1,..}^{\infty} \left(\frac{a_n}{|Z_{Sn}|} Cos(n\omega_o t) + \frac{b_n}{|Z_{Sn}|} Sin(n\omega_o t)\right) \tag{3- 25}$$

(i) Determination of Angle ϕ:

The following equation shows the current in the series branch of resonant network due to the source V_S:

$$i_{t1} = \frac{v_S}{Z_{S1}} = \frac{\sqrt{2}V_S Sin(\omega_o t)}{j|Z_{S1}|} = \frac{-\sqrt{2}V_S}{|Z_{S1}|} Cos(\omega_o t) \tag{3- 26}$$

And the current in the same branch due to the output source V_{TP} is given by:

$$i_{t2} = i_{S2} = \sum_{n=1,2}^{\infty} \left(\frac{a_n}{|Z_{Sn}|} Cos(n\omega_o t) + \frac{b_n}{|Z_{Sn}|} Sin(n\omega_o t)\right) \tag{3- 27}$$

So the resonant current in this branch according to theorem of superposition is:

$$\begin{aligned} i_t &= i_{t1} + i_{t2} \\ &= \frac{-\sqrt{2}V_S}{|Z_{S1}|} Cos(\omega_o t) + \sum_{n=1,2}^{\infty} \left(\frac{a_n}{|Z_{Sn}|} Cos(n\omega_o t) + \frac{b_n}{|Z_{Sn}|} Sin(n\omega_o t)\right) \end{aligned} \tag{3- 28}$$

The resonant Current is $i_r = 0$ at $\omega_0 t = \phi$, therefore from Equation (3-28) the following relations are obtained:

$$\frac{-\sqrt{2}V_S}{|Z_{S1}|}Cos\phi + \sum_{n=1,2}^{\infty}(\frac{a_n}{|Z_{Sn}|}Cos(n\phi) + \frac{b_n}{|Z_{Sn}|}Sin(n\phi)) = 0$$

$$Cos\phi = \frac{\sqrt{2}}{2}\sum_{n=1,2}^{\infty}(\frac{|Z_{S1}|}{|Z_{Sn}|}\frac{a_n}{V_S}Cos(n\phi) + \frac{|Z_{S1}|}{|Z_{Sn}|}\frac{b_n}{V_S}Sin(n\phi)) \qquad (3\text{-}29)$$

For a given control angle α, the value of ϕ would have been calculated by using Equation (3-29), if the value of $\frac{V_O}{V_S}$ were known. The value of $\frac{V_O}{V_S}$ can be obtained by setting the input power equal to the output power.

Since the input voltage source contains no harmonics, the product of the fundamental input current, the input voltage and the fundamental cosine angle between the two determines the input power, which leads us to the next sub-section.

(ii) Output Voltage Control:

Output voltage control is provided by controlling the current controller pulse width (gating of Q_1 and Q_2) other word angle α.

By substituting n = 1 the fundamental time-varying input current from Equation (3-25) is given by:

$$i_{Sf} = \frac{\sqrt{2}.V_S}{|Z_{t1}|}Cos(\omega_0 t) + \frac{a_1}{|Z_{S1}|}Cos(\omega_0 t) + \frac{b_1}{|Z_{S1}|}Sin(\omega_0 t) \qquad (3\text{-}30)$$

where

$$a_1 = \frac{Q}{2\pi}[-Cos(2\phi + 2\alpha - \beta) - 2(\phi + \alpha)Sin\beta + Cos(2\phi - \beta) + 2\phi.Sin\beta] \quad (3\text{-}31)$$

$$b_1 = \frac{Q}{2\pi}[-Sin(2\phi + 2\alpha - \beta) + 2(\phi + \alpha)Cos\beta + Sin(2\phi - \beta) - 2\phi.Cos\beta] \quad (3\text{-}32)$$

The fundamental time-varying current from Equation (3-30) can be simplified by:

$$i_S = C.Sin(\omega_0 t + \theta) \quad (3\text{-}33)$$

and

$$A.Cos(x) + B.Sin(x) = C.Sin(\omega_0 t + \theta) \quad (3\text{-}34)$$

where: $C = \sqrt{A^2 + B^2}$ and $\theta = \tan^{-1}(A/B)$, it is carried out that A and B parameters are:

$$A = \frac{\sqrt{2}}{|Z_{t1}|}V_S + \frac{a_1}{|Z_{S1}|} \quad (3\text{-}35)$$

$$B = \frac{b_1}{Z_{S1}|} \quad (3\text{-}36)$$

Since the input voltage source contains no harmonics, the product of the fundamental input current, the input voltage and the fundamental cosine angle between the two determines the input power. The input power is given by:

$$P_i = V_S I_S Cos\theta = V_S \frac{C}{\sqrt{2}} Cos\theta = \frac{V_S}{\sqrt{2}} \frac{b_1}{|Z_{S1}|} \quad (3\text{-}37)$$

The output power is given by:

$$P_O = \frac{V_O^2}{R_O} \quad (3\text{-}38)$$

Since the input power is equal to the output power, the following relation is obtained from Equation (3-37) and Equation (3-38):

$$\frac{V_O^2}{R_O} = \frac{V_S}{\sqrt{2}} \frac{b_1}{|Z_S|}$$

or

$$\frac{V_O}{V_S} = \frac{R_o}{\sqrt{2}} \frac{b_1}{|Z_{S1}|} \qquad (3\text{-}39)$$

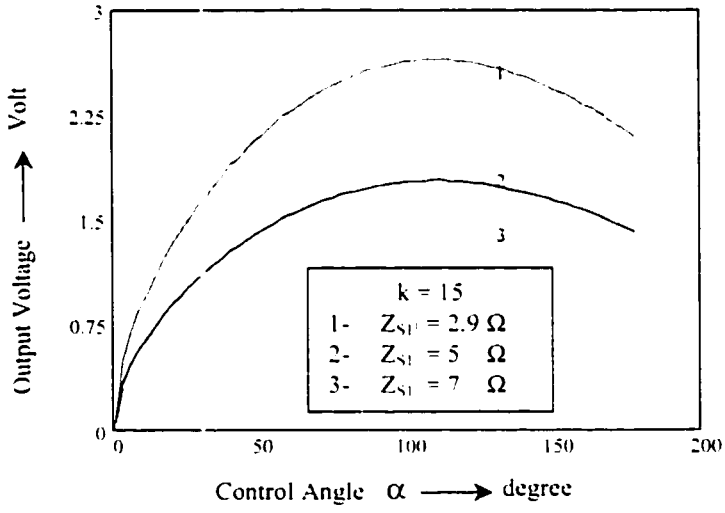


Figure3- 5: Output voltage versus Control angle

Figure 3-5 shows the output voltage versus control angle. For the same values of $\frac{N_1}{N_2}$ and Z_{S1} the converter output voltage has been drawn. As can be seen, the output voltage has a drop in comparison with the simplified case. This is due to the drop of voltage across the leakage inductance and series inductance of synchronous rectifiers.

(iii) Input Current Total Harmonic Distortion:

The total harmonic distortion (THD) of the input current is defined as:

$$THD = \frac{\sqrt{\sum_{n\neq 1} I_n^{\,2}}}{I_1}$$

where $I_n^{\,2} = \frac{a_n^{\,2} + b_n^{\,2}}{|Z_{Sn}|^2}$ and $I_1 = \sqrt{(\frac{\sqrt{2}.V_S}{|Z_{t1}|} + \frac{a_1}{|Z_{S1}|})^2 + (\frac{b_1}{|Z_{S1}|})^2}$.

Therefore:
$$THD = \frac{\sqrt{\sum_{n\neq 1}^{\infty} \frac{a_n^{\,2} + b_n^{\,2}}{|Z_{Sn}|^2}}}{\sqrt{(\frac{\sqrt{2}.V_S}{|Z_{t1}|} + \frac{a_1}{|Z_{S1}|})^2 + (\frac{b_1}{|Z_{S1}|})^2}} \qquad (3\text{-}40)$$

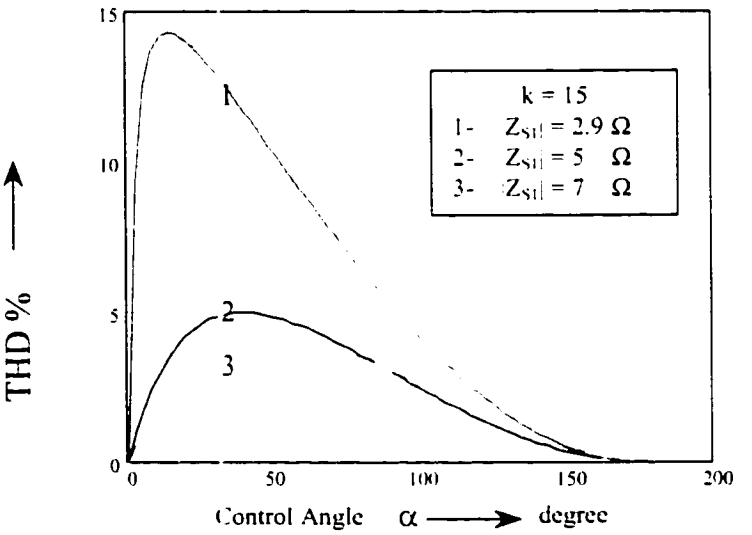


Figure3- 6: Total harmonic distortion

Figure3-6 shows THD for different values of series and parallel impedance. According to the graph, the THD is still as comparable as in the ideal case.

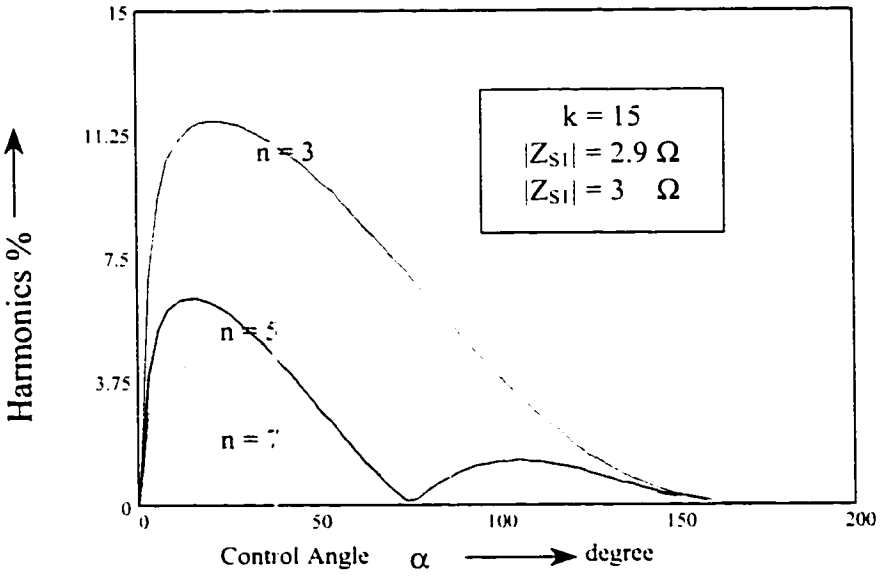


Figure3- 7: The Harmonics% of input current

Figure3-7 shows the %Harmonic of input current. As it is expected, the 3rd harmonic is the most severe one. The 5th harmonic is the next most severe and the rest are less severe.

(iv) Input Power Factor:

The converter input power factor is given by:

$$PF = \frac{Cos\theta}{\sqrt{1+THD^2}} \qquad (3\text{-}41)$$

Figure3-8 shows power factor versus control angle in converter by considering the leakage inductance. As can be seen, the power factor is just close to unity in a narrow range of control angle, which was not the case in the simplified analyses.

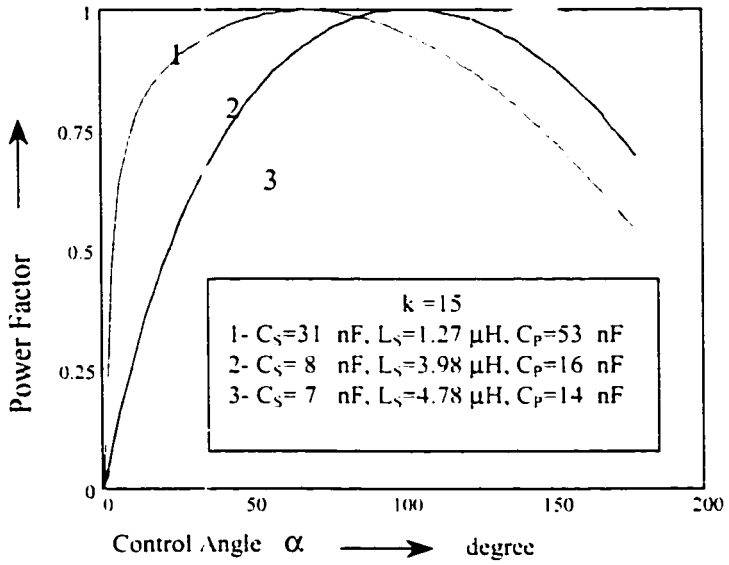


Figure3- 8: Power factor versus control angle

3.4 Simulation Results

Simulation based on the prototype converter is carried out using OrCAD to verify analyses done in this chapter. Table3-1 shows the principle parameters of the circuit used in simulation.

Table3- 1: Principle Parameters of the Simulated Circuit in OrCAD

Parameter	value	parameter	value
V_S	30 V rms	C_o	480 µF
P_o	80 W	C_S	6.8 nF
f_S	2 MHz	L_S	3.8 µH
k	15:1:1	C_P	12 nF
SR_1 & SR_2	IRL 3803	L_{lk}	0.5 µH

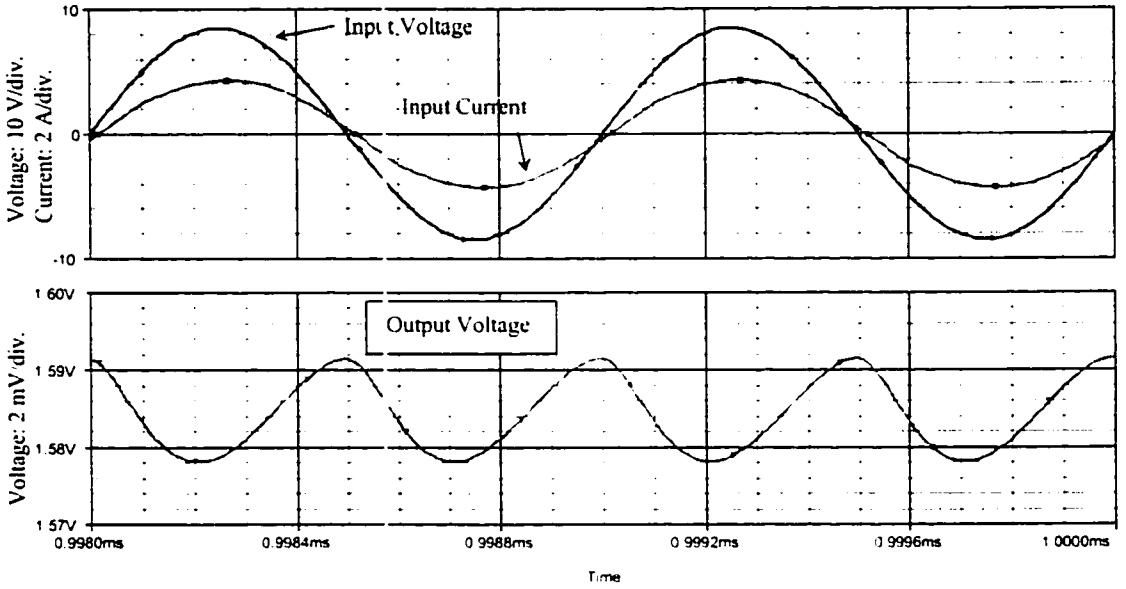


Figure3- 9: The input voltage and current and output voltage

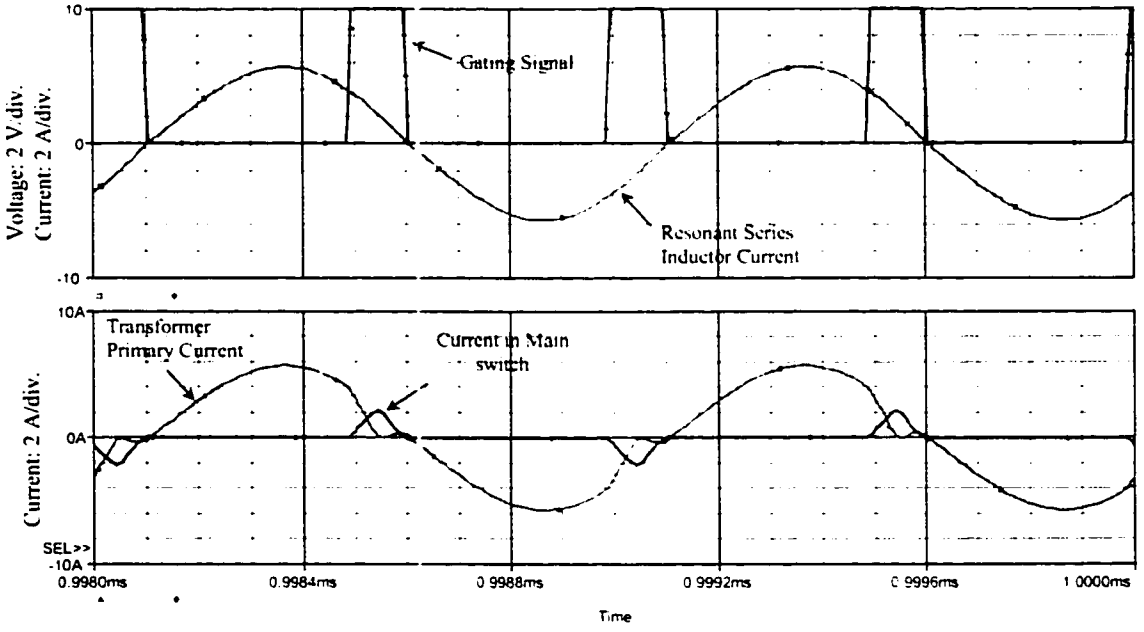


Figure3- 10: Current in the switches, primary of transformer and resonant series inductor

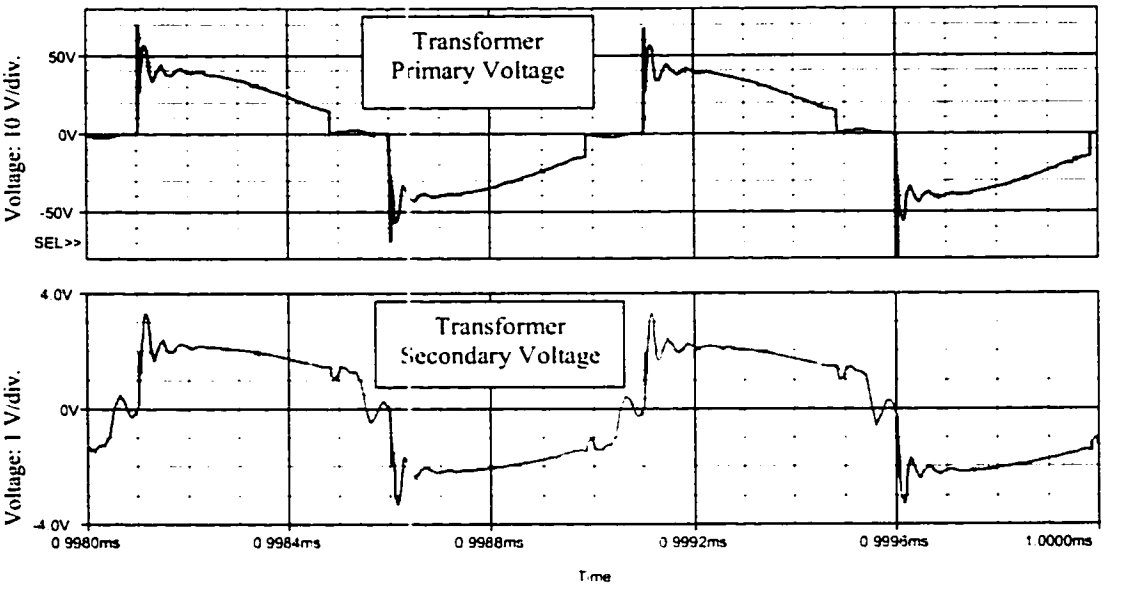


Figure3- 11:The voltage in the primary and secondary of transformer

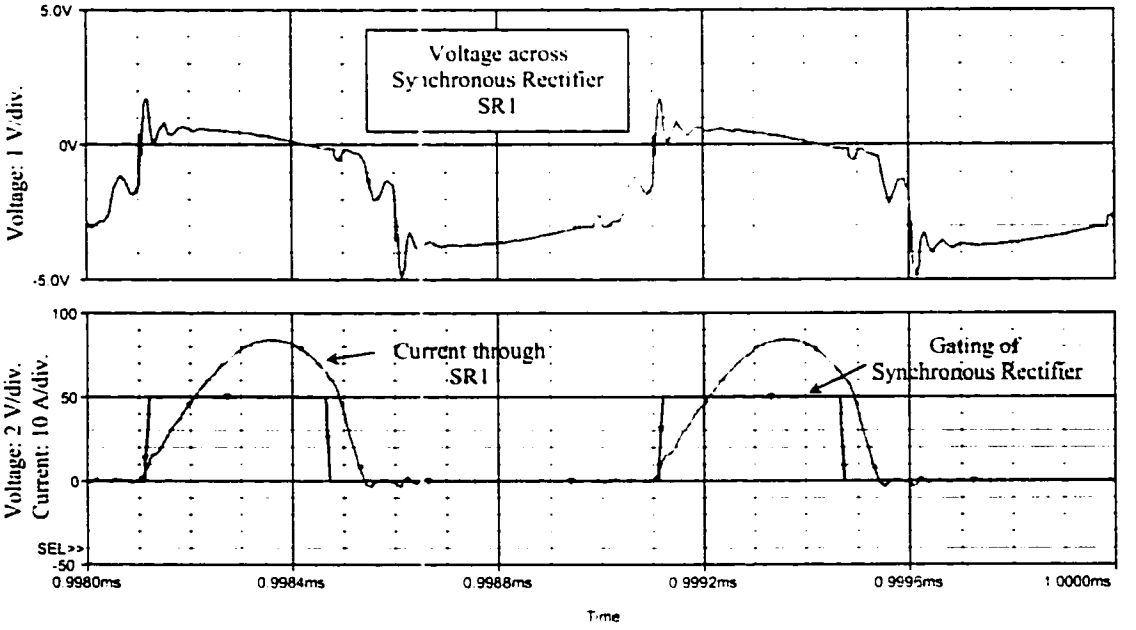


Figure3- 12: Voltage, Current and gating of SR_1

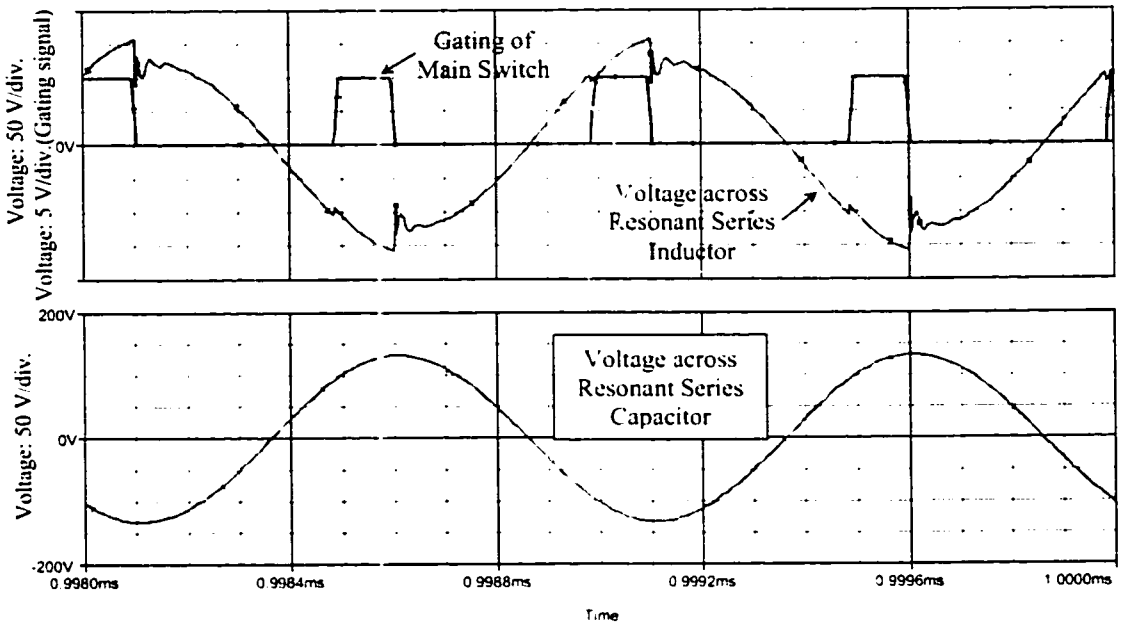


Figure3- 13: Voltage across series resonant inductor and capacitor, and gating of the main switches

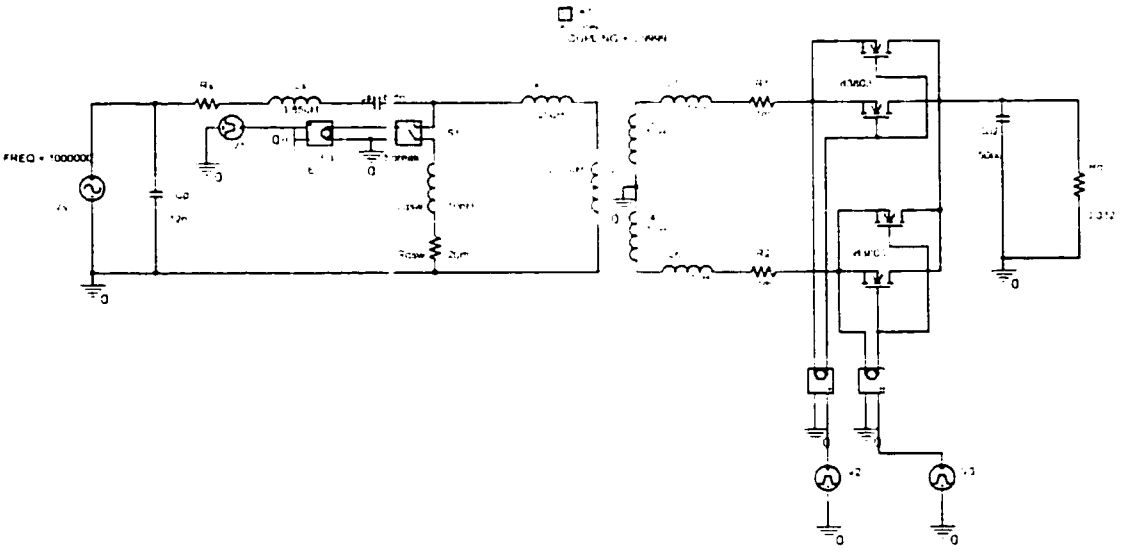


Figure3- 14: The circuit simulated in OrCAD

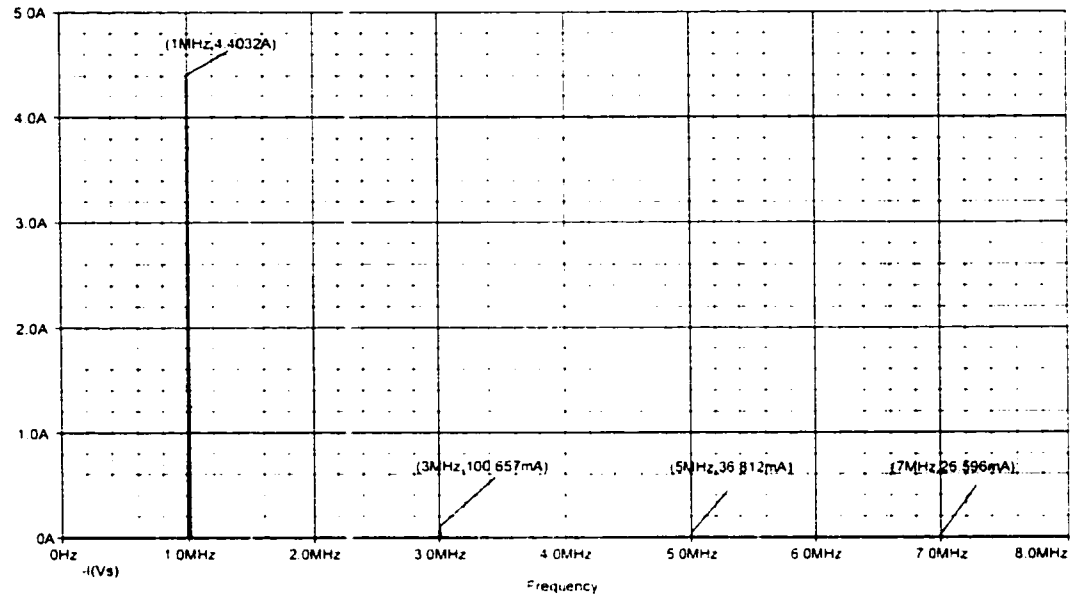


Figure3- 15: Harmonics due to input current of converter

Figure 3-9 shows the input voltage and current along with the output voltage. As it was expected through the analyses carried out in MathCAD, the power factor is not as comparable as it was when it was in the simplified case, so the voltage and current in the input are not exactly at the same phase.

It is discussed earlier n this chapter, due to presence of leakage inductance in the transformer, the current in the primary side of transformer did not have a sharp fall, and in the switches, it did not have a sharp rise. Figure 3-10 shows the current in the switches and primary of transformer.

Also the voltage in the primary side and secondary side were not a quasi-square wave anymore. Figure 3-11 shows the voltage in primary and secondary of transformer.

Figure 3-12 shows the current in the secondary side of the transformer, gating of synchronous rectifier and the voltage across it. Figure 3-13 shows the voltage across the series resonant capacitor and inductor along with the gating of the main switches. Figure 3-14 shows the simulation circuit used in OrCAD 9.1 to verify the design.

Table3- 2: Comparison of Analyses done and simulation in OrCAD

	Simplified Analysis	Detailed Analysis	OrCAD Simulation
L_S	3.98 µH	3.98 µH	3.98 µH
C_S	7.9 nF	7.9 nF	7.9 nF
C_P	15.9 nF	15.9 nF	15.9 nF
k	15	15	15
L_{lk}	0	0.475 µH	0.475 µH
θ	1.132°	6.833°	5.424°
ϕ	64°	60°	55.02°
α	144°	144°	144°
D	0.2	0.2	0.2
PF	1	0.993	0.995
I_1(rms)	3.677 A	4.188 A	3.89 A
THD%	2.192%	0.62%	3.106%
I_3/I_1%	1.417%	0.354%	2.698%
I_5/I_1%	0	0.282%	1.284%
I_7/I_1%	0.239%	0.213%	0.848%
η	90%	70%	68.9%
V_o	1.78	1.68	1.6

Figure 3-15 shows the input current harmonics of the converter that has been used to carry out the data for Table3-2. This table shows a comparison between the analyses carried out in simplified analysis and practical analysis with considering the effect of leakage inductance and the simulation in OrCAD. It is concluded that at the same control angle, transformer ratio, and resonant tank components, the power factor is

smaller in practical case and simulation than the simplified case. Also, there is a voltage drop in this case, which is due to the leakage inductance.

3.5 Conclusion

Simulation of the proposed converter topology is performed with the OrCAD software and the result is as it was expected. The current in the primary of transformer did not have an instantaneous fall, due to the presence of leakage inductance. In the detailed analysis, the assumption made does not take care of THD, as the main concern was the output voltage and input power factor. Therefor, THD in the detailed analysis is much lower than the simplified analysis is. Consequently, the output voltage and power factor are attained lower than the simplified analysis case. It is seen that the converter has a unity power factor in a narrower range of control angle in comparison with the simplified case. But with a proper design of operating point, a unity power factor is attained in full load as well as a small harmonics distortion in the input current.

CHAPTER 4

DYNAMIC PROPERTIES

4.1 Introduction

Understanding the dynamic properties of a converter is one of the most critical issues. In this chapter, the transfer function of power stage for the proposed converter topology is derived by the method of averaging the state space equations. Then an error amplifier is selected to provide the required compensation. At the end, the simulation result and responses to the step change in load is presented followed by conclusion.

Although the resonant network of the proposed topology changes the input voltage source to a current source, they don't come to the picture when the power stage transfer function is derived. Therefore, the resonant elements don't have any influence on the dynamic properties of the power circuit. For this reason, the input voltage source and the resonant network are considered to be a current source for the sake of simplification. Therefore the proposed topology can be simplified as shown in Figure4-1.

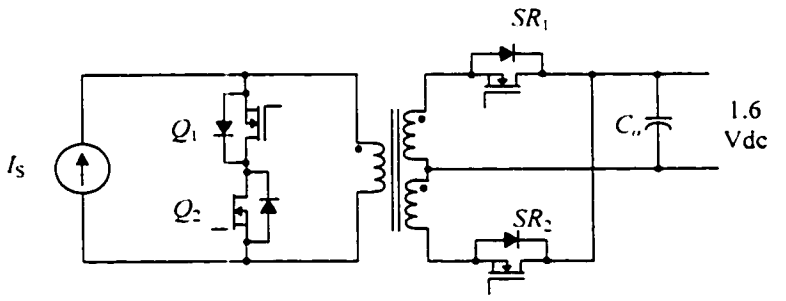


Figure4- 1: The simplified proposed topology

In Section 4.2.1, the state space averaging is used to obtain power stage transfer function. The controller is designed in Section 4.2.2. Simulation and response to step changes is presented in Section 4.3, and a conclusion is drawn at the end of this Chapter.

4.2 Control of HF AC/DC Converter

The output voltage of VRM is regulated to be within a specified tolerance band (e.g., ± 5% around its nominal value) in response to changes in the output load and the input line voltages. This is accomplished by using a negative-feedback control system, shown in Figure 4-2, where the converter output voltage v_o is compared with its reference value V_{ref}. The error amplifier produces the control voltage v_c, which is used to adjust the duty ratio d of the switches in the converter.

If the power stage of the AC/DC converter in Figure 4-2 can be linearized, then the Nyquist stability criterion and the Bode plots can be used to determine the appropriate compensation in the feedback loop for the desired steady state and transient responses.

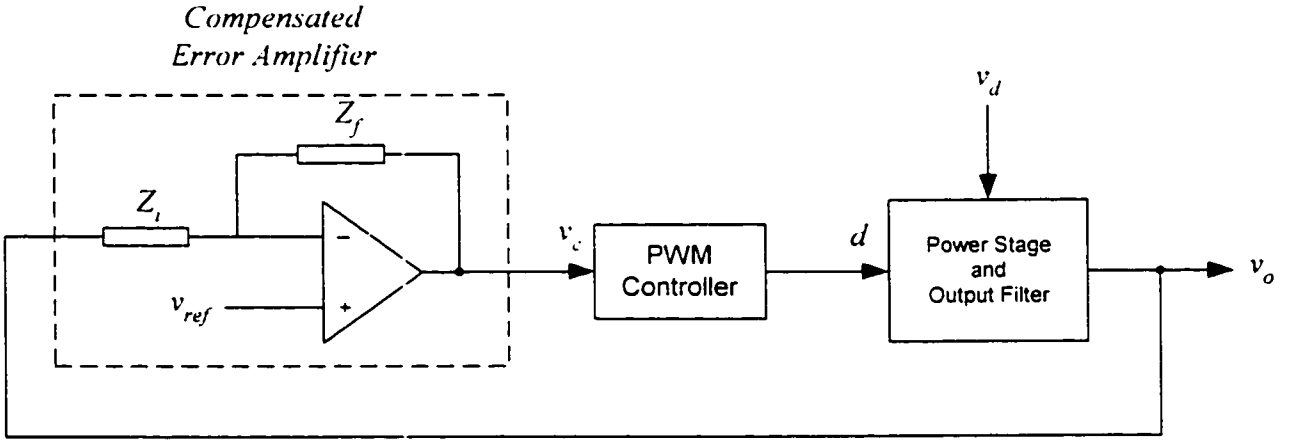


Figure4- 2: Voltage regulation feedback control system

4.2.1 Linearization of The Power Stage Using State-Space Averaging

The goal of the following analyses is to obtain a small signal transfer function $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$, where $\tilde{v}_o$ and $\tilde{d}$ are small perturbations in the output voltage v_o and the switching duty ratio d, respectively, around their steady state dc operating values V_o and D. The procedure is as follows:

(i) State-Variable Description for Each Circuit State: In the converter, there are two circuit states: one state corresponds to when the switches Q_1 and Q_2 are on, and the other one when these switches are off, as shown in Figure 4-3.

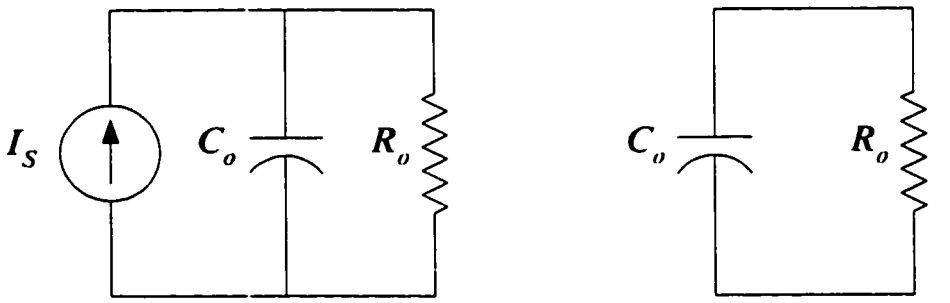


Figure4- 3: The circuit states, (a) when the switches are on (b) when the switches are off

During each circuit state, the linear circuit is described by means of the state-variable vector x consisting of the capacitor voltage. In the circuit description, the equivalent series resistance (ESR) of the output capacitor neglected. Therefore, during each circuit state, we can write down the following equations:

$$\dot{x} = A_1 x \qquad \text{during } d \,.\, T_S \tag{4- 1}$$

$$\dot{x} = A_2 x + B_2 i_S \qquad \text{during } (1\text{-}d) \,.\, T_S \tag{4- 2}$$

where A_1 and A_2 are state matrices and B_2 is a vector.

The output can be described in terms of their states variables alone as:

$$v_o = C_1 x \qquad \text{during } d \,.\, T_S \tag{4- 3}$$

and

$$v_o = C_2 x \qquad \text{during } (1\text{-}d) \,.\, T_S \tag{4- 4}$$

where C_1 and C_2 are transposed vectors.

(ii) Averaging the State-Variable Description Using the Duty Ratio d; To produce an average description of the circuit over a switching period. the equations corresponding to the foregoing states are time weighted and averaged. resulting in the following equations:

$$\dot{x} = [A_1 d + A_2 (1-d)]x + [B_2 (1-d)] \cdot i_S \tag{4- 5}$$

$$v_o = [C_1 d + C_2 (1-d)]x \tag{4- 6}$$

(iii) Introducing Small ac Perturbation and Separation into ac and dc Components: Small ac perturbations. represented by "~", are introduced in the dc steady state quantities. Therefore.

$$x = X + \tilde{x} \tag{4- 7}$$

$$v_o = V_o + \tilde{v}_o \tag{4- 8}$$

$$d = D + \tilde{d} \tag{4- 9}$$

and

$$i_S = I_S + \tilde{i}_S \tag{4- 10}$$

Using Equations (4-7) through (4-10) in Equation (4-5) and recognizing that in steady state, $\dot{X} = 0$,

$$\dot{\tilde{x}} = [A_1 D + A_2(1-D)]X + [(A_1 - A_2)\tilde{d}]X + [A_1 D + A_2(1-D)]\tilde{x} + [B_2(1-D)I_S - B_2\tilde{d}I_S + B_2(1-D)\tilde{i}_S +$$
terms containing products of $\tilde{d}$, $\tilde{x}$ and $\tilde{i}_S$ (to be neglected) (4- 11)

where

$$A = A_1 D + A_2(1-D) \tag{4- 12}$$

$$B = B_1 D + B_2(1-D) \tag{4- 13}$$

The steady state equatior can be obtained from Equation (4-11) by setting all the perturbation terms and their derivatives to zero. Therefore, the steady state equation is:

$$[A_1 D + A_2(1-D)]X + [B_2(1-D)]I_S = 0 \tag{4- 14}$$

and therefore in Equation (4-11):

$$\dot{\tilde{x}} = [(A_1 - A_2)X]\tilde{d} + [A_1 D + A_2(1-D)]\tilde{x} - B_2\tilde{d}I_S + [B_2(1-D)]\tilde{i}_S \tag{4- 15}$$

Similarly, using Equations (4-7) through (4-10) in Equation (4-6) results in:

$$V_o + \tilde{v}_o = [C_1 D + C_2(1-D)]X + [(C_1 - C_2)\tilde{d}]X + [C_1 D + C_2(1-D)]\tilde{x} \tag{4- 16}$$

In Equation (4-16), the steady state output voltage is given as

$$V_o = CX \tag{4- 17}$$

and therefore,

$$\tilde{v}_o = [C_1 D + C_2(1-D)]\tilde{x} + [(C_1 - C_2)\tilde{d}]X \tag{4- 18}$$

Using Equations (4-14) and (4-17), the steady state voltage transfer function is:

$$\frac{V_o}{I_S} = -CA^{-1}B \tag{4-19}$$

(iv) Transformation of the ac Equations into s-Domain to Solve for the Transfer Function: Equations (4-15) and (4-18) consist of the ac perturbations. Using Laplace transformation in Equation (4-15),

$$s \cdot \tilde{x}(s) = A\tilde{x}(s) + [(A_1 - A_2)X - B_2 I_S]\tilde{d}(s) + B_2(1-D)\tilde{i}_S(s) \tag{4-20}$$

or

$$\tilde{x}(s) = [sI - A]\{[(A_1 - A_2)X - B_2 I_S]\tilde{d}(s) + B_2(1-D)\tilde{i}_S(s)\} \tag{4-21}$$

where I is a unity matrix. Using Laplace transformation in Equation (4-18) and expressing $\tilde{x}(s)$ in terms of $\tilde{d}$ and by assuming the current source is an ideal source so $\tilde{i}_S = 0$ from Equation (4-21) results in the desired transfer function $T_p(s)$ of the power stages:

$$T_p(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = C[sI - A]^{-1}[(A_1 - A_2)X - B_2 I_S] + [(C_1 - C_2)X] \tag{4-22}$$

Let $x = v_o$ in the circuit of Figure 4-3. Then, in the circuit of Figure4-3(b) with the switches off,

$$i = R_o C_o \dot{x} \tag{4-23}$$

In matrix form, this equation can be written as:

$$\left[\dot{x}\right] = \left[\frac{1}{R_o C_o}\right][x] + [0]\cdot[I_S] \tag{4- 24}$$

therefore,

$$A_1 = \left[\frac{1}{R_o C_o}\right] \tag{4- 25}$$

and

$$B_1 = [0] \tag{4- 26}$$

The output voltage in both the circuit states is given as:

$$v_o = x \tag{4- 27}$$

Therefore, in the Equations (4-3) and (4-4):

$$C_1 = C_2 = [1] \tag{4- 28}$$

In the circuit of Figure 4-3(a) with the switches on:

$$I_S = \frac{x}{R_o} + C_o \dot{x} \tag{4- 29}$$

In matrix form, this equation can be written as:

$$\left[\dot{x}\right] = \left[\frac{-1}{R_o C_o}\right][x] + \left[\frac{1}{C_o}\right]\cdot[I_S] \tag{4- 30}$$

therefore,

$$A_1 = \left[\frac{-1}{R_o C_o}\right] \tag{4- 31}$$

and

$$B_1 = \left[\frac{1}{C_o}\right] \tag{4- 32}$$

Therefore A and C are simplified as:

$$A = A_1 D + A_2(1-D) = \frac{D}{R_o C_o} - \frac{1-D}{R_o C_o} = \frac{2D-1}{R_o C_o} \tag{4- 33}$$

and

$$C = C_1 D + C_2(1-D) = 1 \tag{4- 34}$$

and B remains unaffected as:

$$B = B_2(1-D) = \frac{1-D}{C_o} \tag{4- 35}$$

Using Equations (4-31) through (4-35) in Equation (4-32) yields:

$$T_p(s) = \frac{2 \cdot V_o - R_o \cdot I_s}{sR_o C_o - 2D + 1} \tag{4- 36}$$

To find out the assumed current source, we consider this current source has the waveform as given in Figure 4-4:

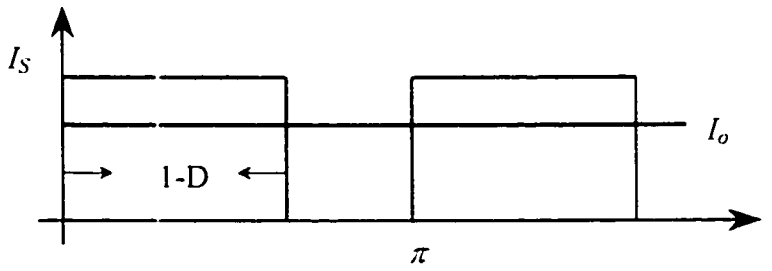


Figure4- 4: The assumed current source waveform

The current in one switching cycle will be as defined below:

$$I_o = \frac{1}{\pi}\int_0^{(1-D)\pi} I_S \, dt = (1-D)I_S \tag{4-37}$$

Therefore, we can find:

$$I_S = \frac{I_o}{1-D} \tag{4-38}$$

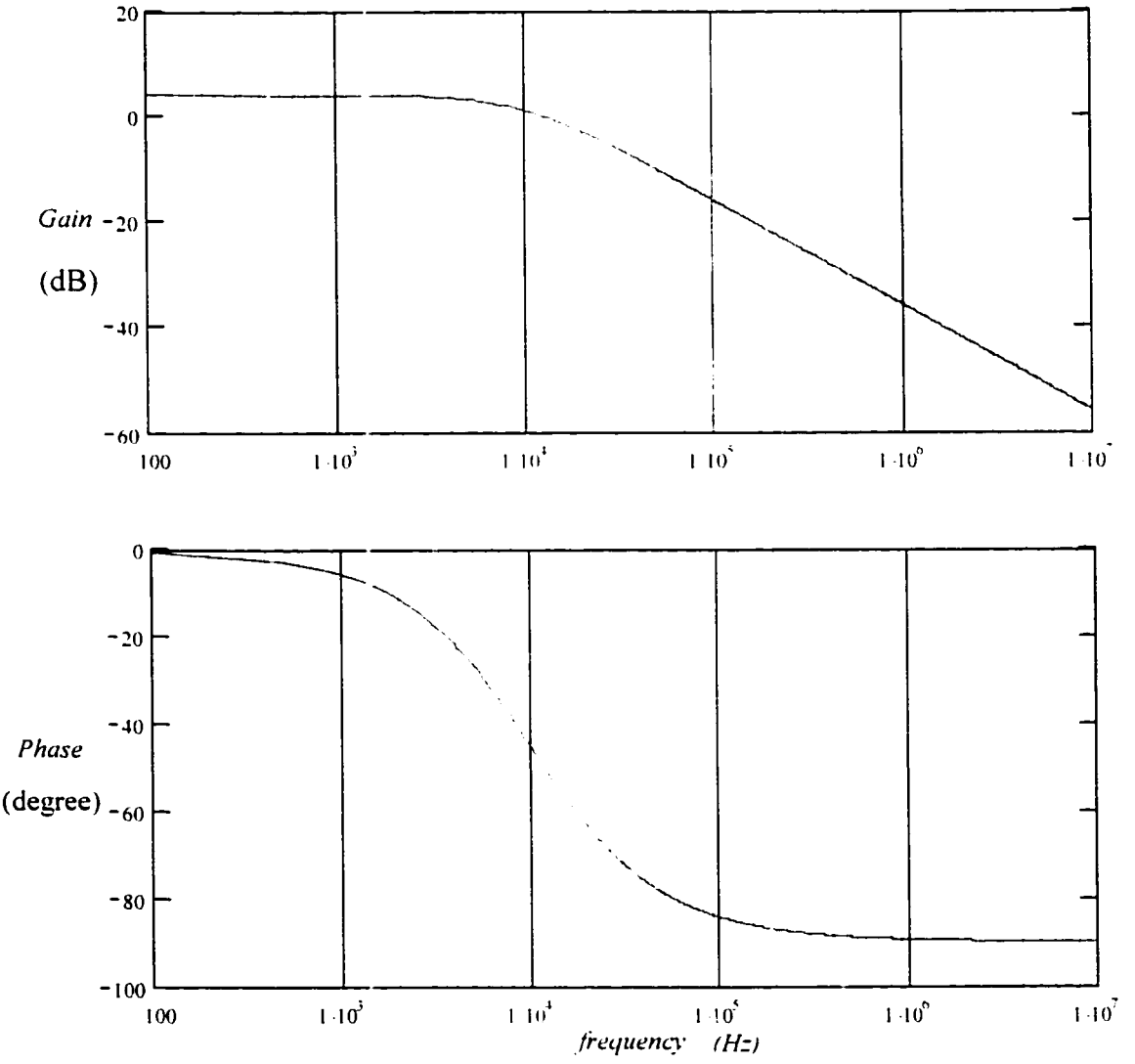


Figure4- 5: Gain characteristic and Phase characteristic of power stage

Replacing in Equation (4-36), the power stage transfer function will be:

$$T_I(s) = \frac{1-2D}{1-D}\frac{V_o}{sR_oC_o - 2D + 1} \qquad (4\text{-}39)$$

Figure 4-5 shows the Bode plot for the transfer function in Equation (4-39) using the numerical values given below and plotted in MathCAD.

$C_o = 480\ \mu F$

$R_o = 0.032\ \Omega$

$V_o = 1.6\ V$

$D = 1/3$

4.2.2 Compensation of The Voltage Loop

A type-2 error amplifier is used to provide the required compensation. This was chosen because at the chosen cross over frequency, the power stage introduces a phase lag of approximately 90 degree. The desired crossover frequency is chosen in such a way that $f_c = \frac{1}{10} f_s$ which is

$$f_c = \frac{1}{10} \times 2 \times 10^6 = 2 \times 10^5 \quad Hz \qquad (4\text{-}40)$$

or

$$\omega_c = 2\pi \times 2 \times 10^5 \quad rad/\sec \qquad (4\text{-}41)$$

Figure 4-6 shows a type-2 compensation around the error voltage. The transfer function for this controller is given by:

$$G_c(s) = \frac{K_c}{s} \frac{(1 + \frac{s}{\omega_{Z,b}})}{(1 + \frac{s}{\omega_{P,b}})} \qquad (4\text{-}42)$$

The design procedure for a type-2 controller is given below.

(i) The phase boost ϕ_{boost} needed at the cross over frequency is:

$$\phi_{boost} = -90^\circ + \phi_{pm} - \phi_{PS} \qquad (4\text{-}43)$$

where ϕ_{PS}, a negative value, is the phase of the power stage at the cross over frequency.

(ii) This phase boost is achieved by placing a zero and a pole as expressed below:

$$\omega_{Z,b} = \frac{\omega_c}{k} \qquad (4\text{-}44)$$

$$\omega_{P,b} = k.\omega_c \qquad (4\text{-}45)$$

where,

$$k = \tan(45^\circ + \frac{\phi_{boost}}{2}) \qquad (4\text{-}46)$$

(iii) Calculate K_c in Equation (4-42) such that the product of the power stage transfer function given in Equation (4-39) and the controller has a unity gain (that is *0 dB*) at the cross over frequency.

The following values are selected for compensation:

$\phi_m = 60^\circ, \phi_{boost} = 58^\circ$, therefore k =3.487 and $\omega_{Z,b} = \frac{\omega_c}{k} = 360325 \quad rad/\sec$,

$\omega_{P,b} = k.\omega_c = 4382286 \quad rad/\sec$, and the components selected for compensation are:

R_{FB1}=1 MΩ, R_{FB2}=100 KΩ, R_1=1000 Ω, R_2= 3.6 KΩ, C_1=750 pF and C_2=68 pF.

where,

$$\frac{1}{R_2 C_1} = \omega_{Z,h} \tag{4- 47}$$

$$\frac{1}{R_1 C_2} = K_c \frac{\omega_{P,h}}{\omega_{Z,h}} \tag{4- 48}$$

$$\frac{1}{R_1 R_2 C_1 C_2} = K_c \cdot \omega_{P,h} \tag{4- 49}$$

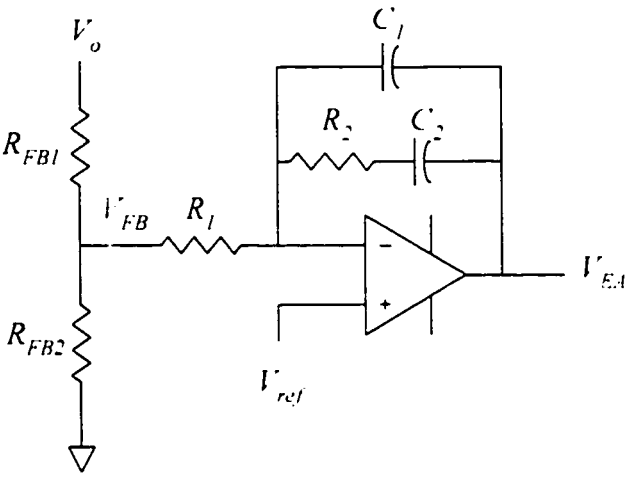


Figure4- 6: Type-2 compensation around the error voltage amplifier

Figure 4-7 shows the Bode plot of controller. As it is expected, the zero and pole frequencies represent points where the error amplifier gain slope changes. A zero represents a +1 change in gain slope and a pole presents a −1 change in gain slope.

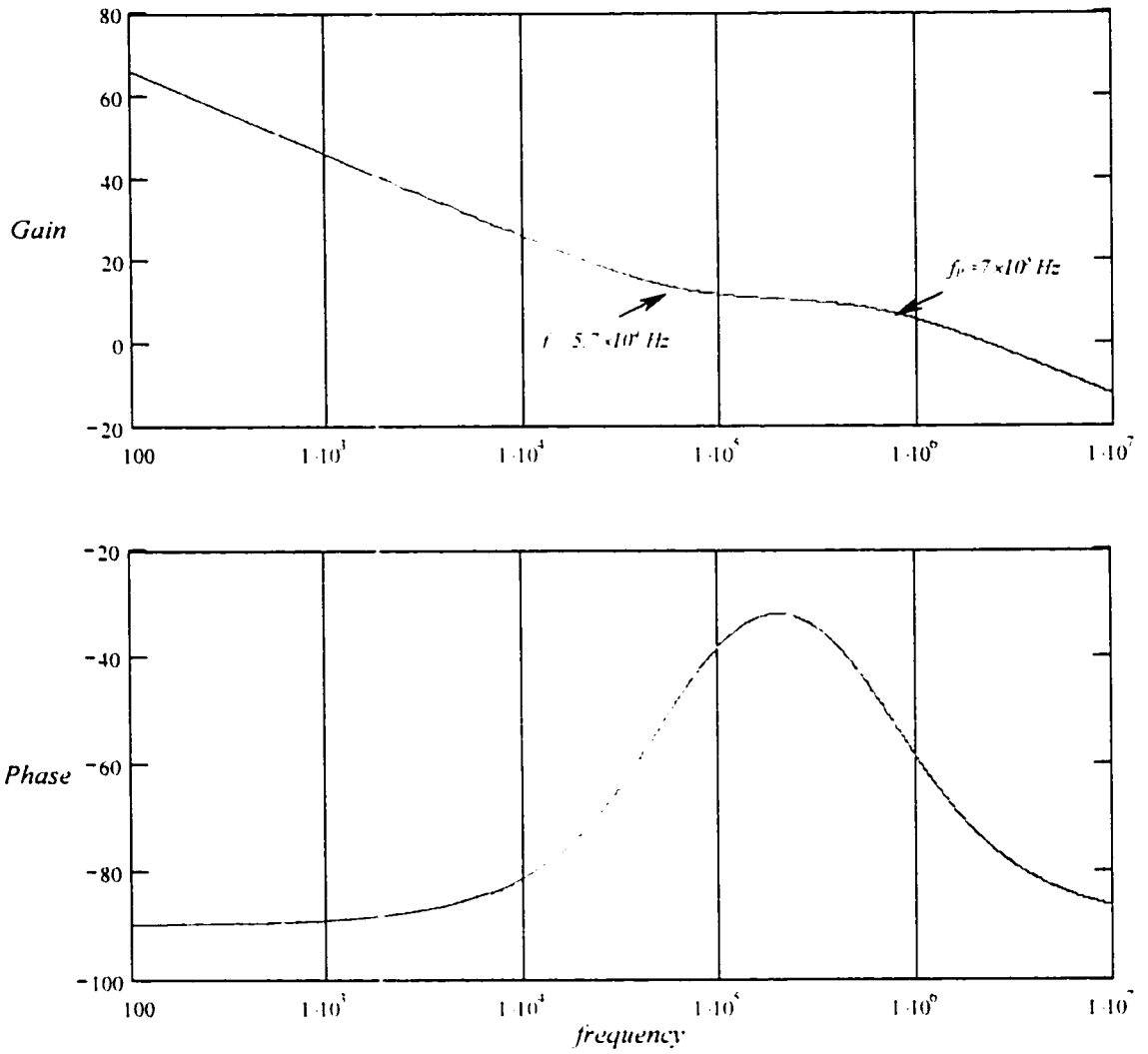


Figure4- 7: Gain characteristic and Phase characteristic of Controller

Recall that the first criterion for a stable loop is that at the frequency f_{co} where the total open loop gain is unity (0 dB), total open loop phase shift must be short of 180° by the desired phase margin, which has herein been taken as 60°.

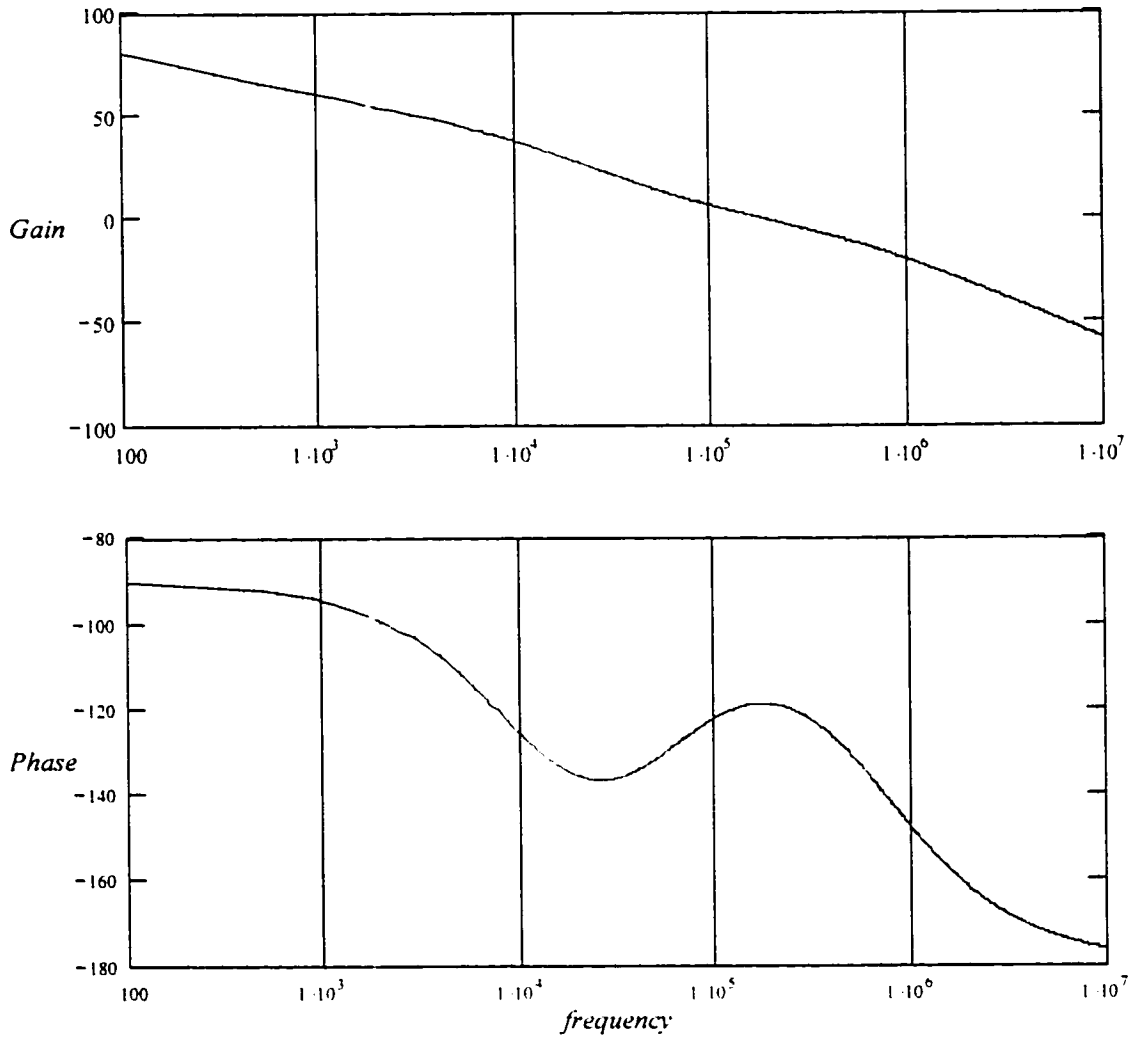


Figure4- 8: Gain characteristic and Phase characteristic of Open Loop

As can be seen in Figure4-8, the open loop gain is forced to be zero at cross over frequency. For the loop to be stable, total open loop phase shift at that frequency should be short of 180° by as large a value as possible. The amount by which it is short of 180° is the phase margin. In this case, the phase margin is 60°, as it was designed.

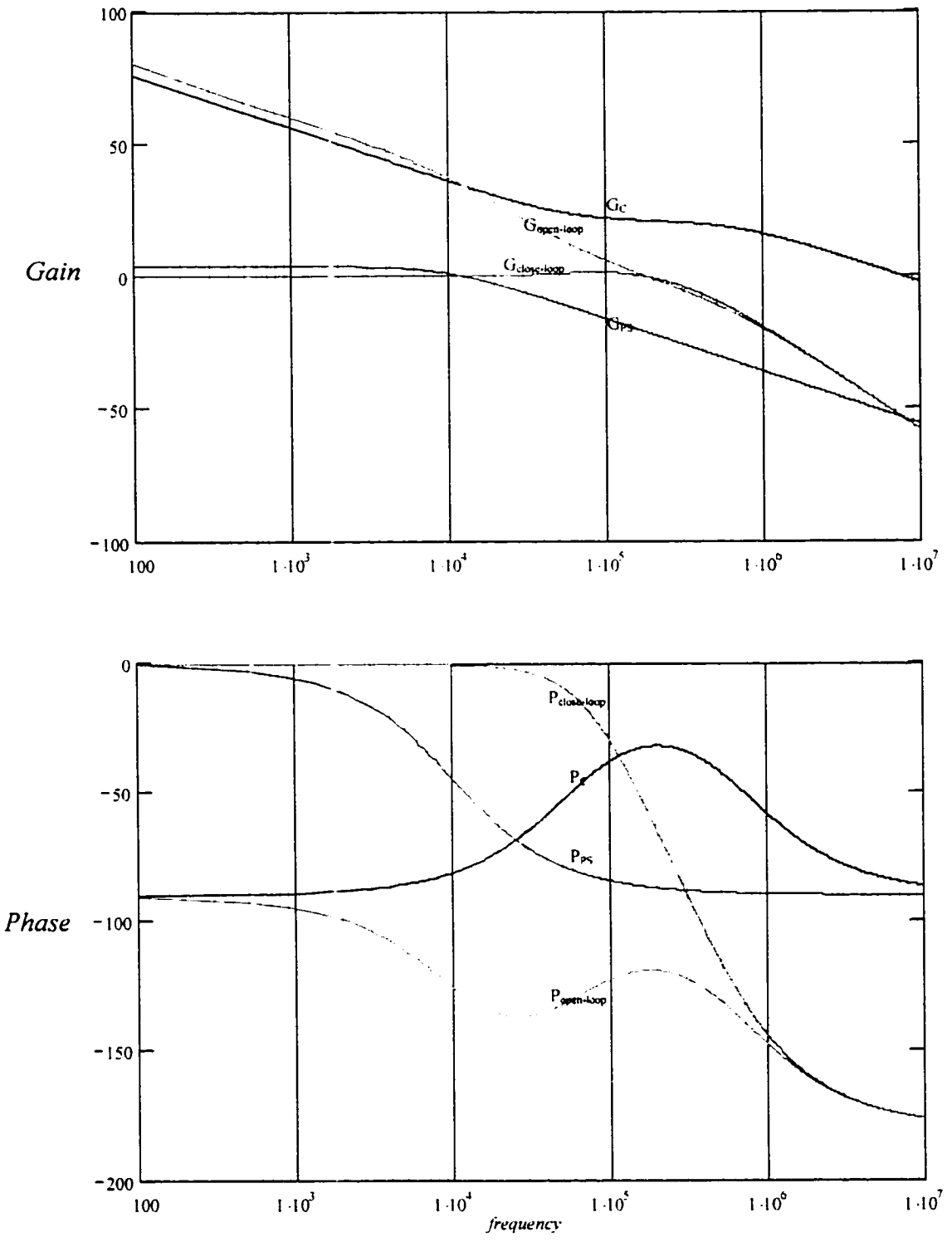


Figure4- 9: Gain and Phase characteristics of all Transfer Functions

4.3 Simulation Results

Simulation based on the prototype converter is carried out using PSIM to verify the analysis in this chapter. Figure 4-10 shows the schematic for simulation of the converter using PSIM.

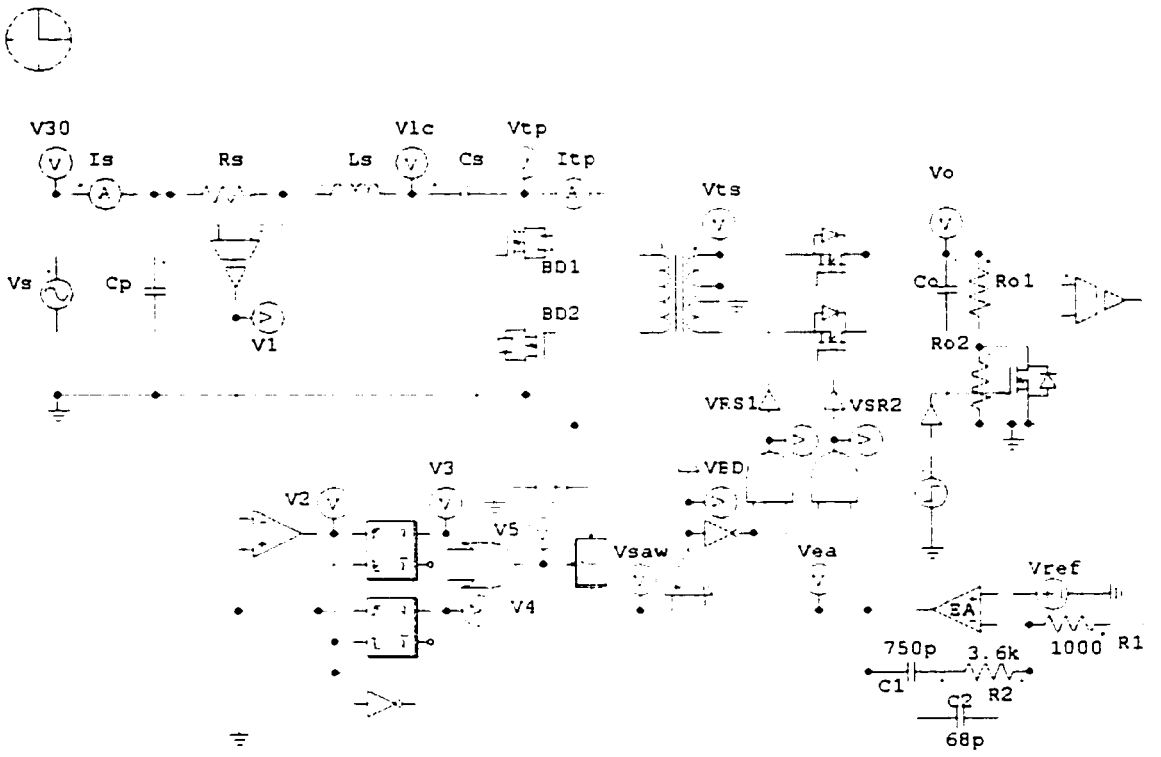


Figure4- 10: Circuit schematic for simulation using PSIM

4.4 Step Change Responses

In the following discussion the converter response to the step changes in the load are shown to verify the design in simulation. Figure 4-11 and Figure 4-12 show the converter response to the step load from 8 A to 50 A.

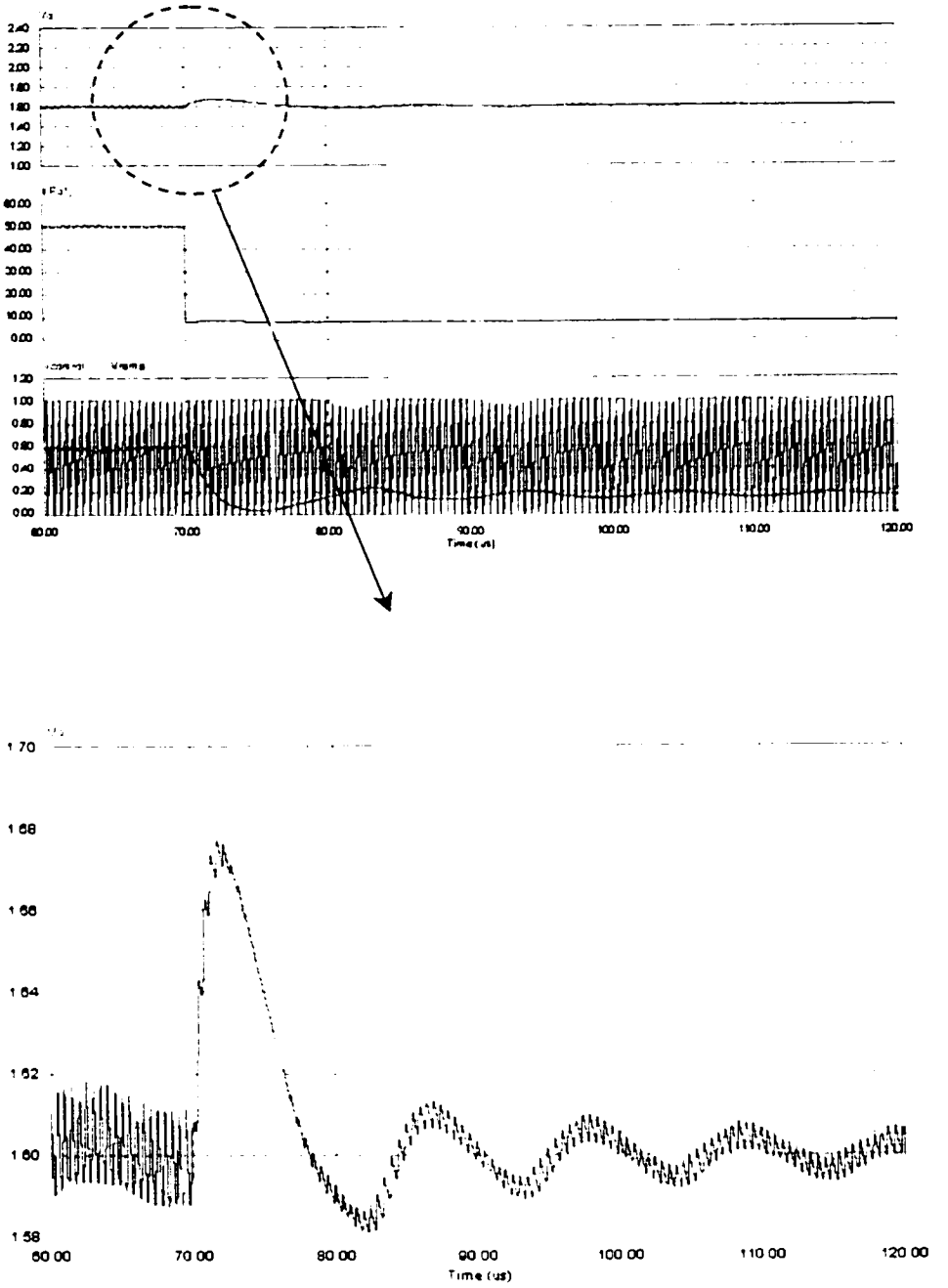


Figure4- 11: Output current step down from 50A to 8A with detailed view of output voltage and control signal.

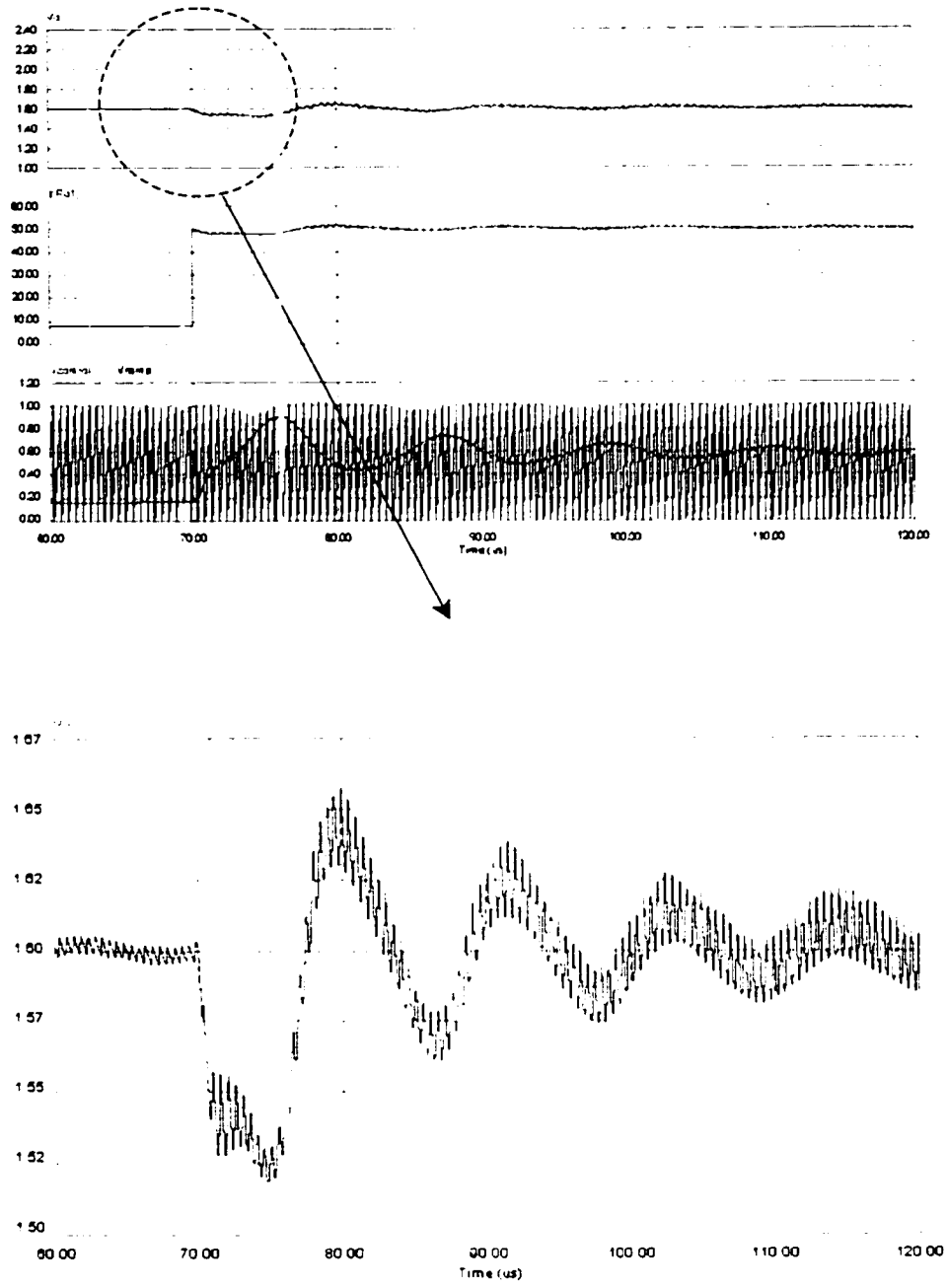


Figure4- 12: Output current steps up from 8A to 50A with detailed view of output voltage and control signal.

It is seen that the output voltage transient is a well-damped response, and it recovers its regulation point (1.6 V) in less than 50 μs. This confirms with the loop design. The control signal shown in the detailed figures views also verify the design in simulation circuit. The steps are exaggerated to demonstrate the control signal variations. It is seen that the control circuit adjusts itself immediately, so the output voltage is hardly affected, neither when the load steps up nor when it steps down.

4.5 Conclusion

In this chapter, first the state space modeling was established and the transfer function of the power stage had been derived for general application. It is found that the presence of the resonant network had no effect on the power stage transfer function. A compensation voltage error amplifier using PWM controller was designed. The closed loop was judged based on the basis of Bode Plots drawn for the transfer functions. Simulation was carried out and the simulation results verified the analysis and design, and it showed the stability of the converter and satisfies all requirements of fast response, overshoot and under-shoot limitations.

CHAPTER 5

DESIGN AND DEVELOPMENT OF PROTOTYPE CONVERTER

5.1 Introduction

This chapter presents a procedure for designing the proposed converter. A design example is given to illustrate the design process for the selection of proper converter components. The design of the converter is based on the characteristic curves derived in chapter 3 and the other considerations such as output voltage ripple, input current total harmonic distortion, and proper turn-on and turn-off of the main switches and synchronous rectifiers are also taken into effect presenting the design example.

The outline of this chapter is as follows:

Section 5.2 presents the design objectives for the converter that was proposed and analyzed in chapter 3. A design example follows and demonstrates the selection of components of the converter.

Section 5.3 presents simulated and experimental waveforms which validate the design process.

Section 5.4 summarizes the main points of this chapter.

5.2 Design of The Proposed Converter

The design specification and design procedure of the proposed converter are presented in this section.

5.2.1 Design Objectives and Specifications

The converter is designed to meet the following objectives:

1) The resonant network must be such a way that insures the input current of the source is almost in phase with the source voltage.

2) The operating frequency must be constant.

3) The total harmonic distortion of the input current must be very small under all load conditions together with the minimized EMI/electromagnetic compatibility (EMC) filter requirements.

4) The gating of the main switches must be synchronized with the gating of the synchronous rectification.

The specifications for the design of the converter are as follows:

(i) $P_o=32\ W$, output power at full load

(ii) $V_o=1.6\ V$, nominal output voltage

(iii) $V_{in}=28\ V\ rms$, nominal input voltage

(iv) $f_s=1\ MHz$, nominal input frequency

(v) $f_s=2\ MHz$, switching frequency

(vi) $k=10:1:1$, transformer turns ratio

(vii) $V_{ripple}=\pm 2\%$, peak to peak output ripple voltage specification

5.2.2 Design Procedure and Example

The design procedure is divided into two parts:

(i) Design of the power circuit

(ii) Design of the control circuit

5.2.2.1 Design of Power Circuit

The guidelines for the design of the power circuit are presented in this sub-section. The equations and curves used have been previously derived in chapter 2 and chapter 3.

a) Resonant Network:

The resonant network consists of C_P, C_S, and L_S. To select the proper values of the resonant network, first the series impedance in the resonant network has to be selected. The relation between the series impedance, transformer ratio and the increase in resonant series branch current is given by:

$$Z_S = \frac{8}{\pi^2}\frac{1}{\sqrt{\lambda^2-1}}\left(\frac{N_1}{N_2}\right)^2 R_L \qquad (5\text{-}1)$$

where λ is the increase in current in series branch when the converter is in no load, and the main switches are conducting fully. Here in this example λ is been selected to be $\lambda = 1.3$. Figure 5-1 shows the transformer ratio versus series branch impedance in resonant network for different values of λ. As it can be seen in the graph, for the transformer ratio of 10, and the desired value of λ, the impedance in the series branch will be $Z_S = 5\ \Omega$. Other words, $X_{Ls} - X_{Cs}$ has to be equal to 5 Ω.

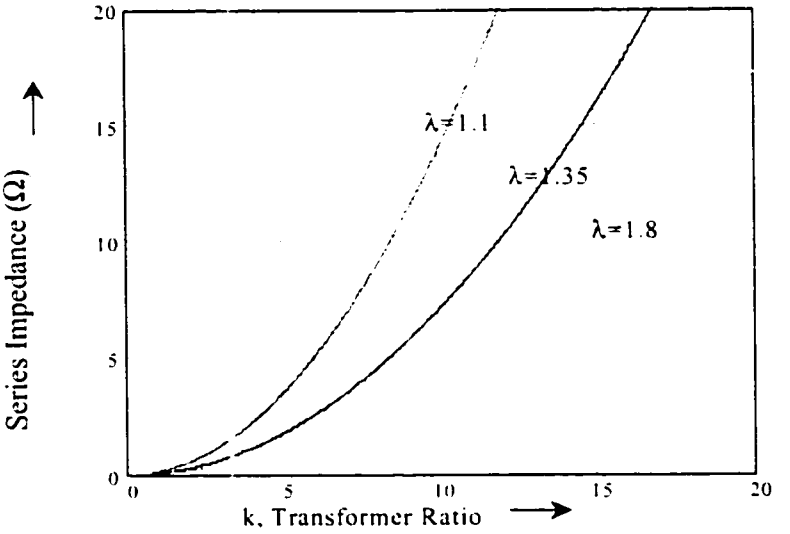


Figure 5- 1: The transformer ratio versus series branch impedance

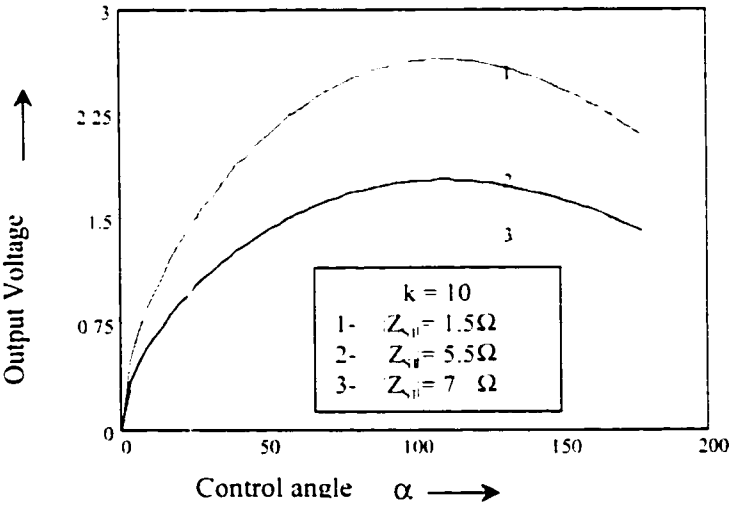


Figure 5- 2: Output voltage versus Control angle

At this point, it has to be verified that the selected impedance can satisfy the voltage requirement. Figure 5-2 shows the control angle versus output voltage. As can be seen, at a selected value of control angle, the output voltage is 1.6 volt, which means the selected value for resonant series branch impedance is a proper design.

Once the selection of series impedance in resonant tank is made, the values for the resonant elements (L_S and C_S) have to be found. Figure 5-3 shows the effect of different values of series impedance on THD. The greater value of L_S is, the less THD is attainable. Therefore, to acquire an improved THD, a great value of impedance for inductor is desirable. On the other hand, the value of capacitor can not be so low. A practical value for C_S is chosen to be 6.8 nF, and then according to that, the value of L_S is chosen 4.5 μH.

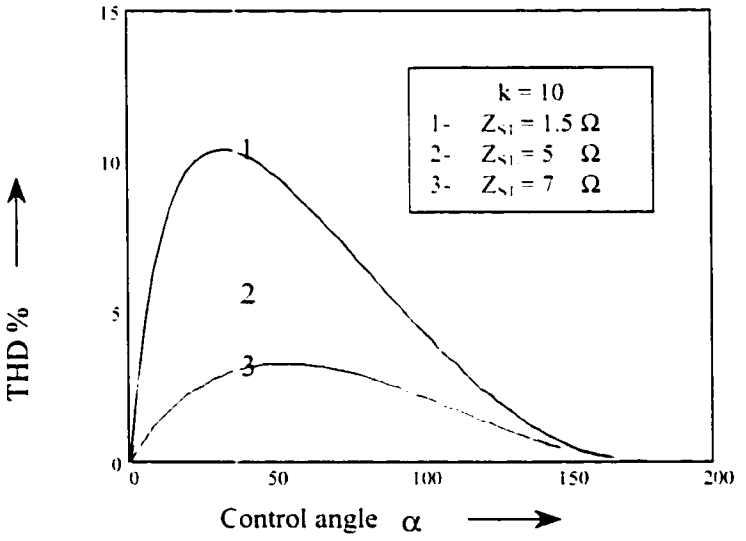


Figure 5- 3: THD versus control angle

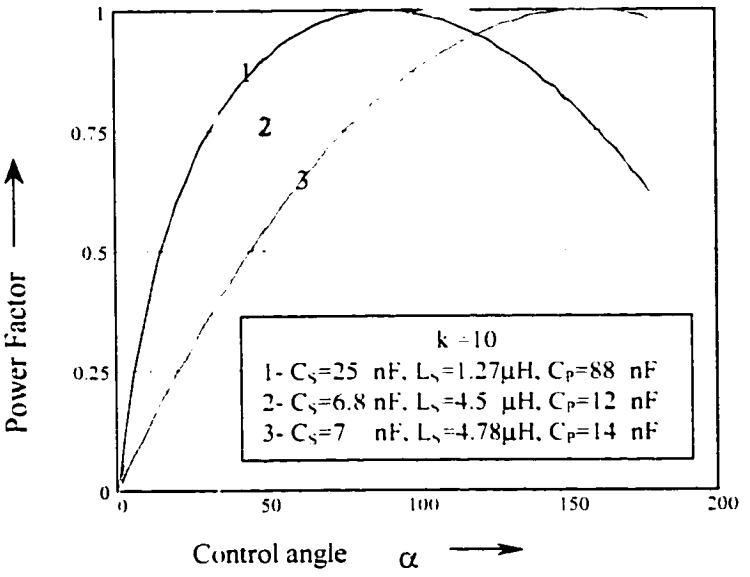


Figure 5- 4: Power factor versus control angle

The purpose of using parallel capacitor is to attain a close to unity power factor as well as a small THD in the input current of converter. As can be seen in Figure 5-4, the proper value for this capacitor is 12 nF. After finding the values of resonant components, the most important concern is finding out voltage stresses across these components.

The maximum voltage across parallel capacitor is the same as the input maximum voltage, therefore:

$$V_{C_p\ max} = 40 \quad Volt \qquad (5\text{-}2)$$

And for the series capacitor, the maximum voltage is:

$$V_{C_s\ max} = 188 \quad Volt \qquad (5\text{-}3)$$

The maximum current through the series inductor is:

$$I_{L_{S\ max}} = \frac{V_S}{Z_S} = \frac{40}{5} = 8 \quad Amp. \qquad (5\text{-}4)$$

b) Power Transformer;

All designs are based on PHILIPS Data Handbook MA01 for Magnetic Products. First the core type and ferrite material have to be selected. For the power of 32 W, the selected core type is EFD20, and the ferrite material is 3F4. Since the operating frequency is 1MHz, the LITZ wires in the primary side of the transformer have to be wound, and due to the high current in the secondary side of the transformer, copper sheets has to be used.

c) Main Switches;

To select a proper switch in the primary side as the main switches, the current and voltage across the switches have to be calculated. The maximum current is the same as the maximum current through the series inductor, which occurs in no load, when these two switches are fully conducted.

$$I_{Q1\&2_{rms}} = 8 \quad Amp. \qquad (5\text{-}5)$$

The voltage across each switch is given by:

$$V_{Q1\&2_{rms}} = R_{eq} \times I_{Transformer} = 52 \quad Volt \qquad (5\text{-}6)$$

Therefore good selection for the main switches would be IRF540.

d) Synchronous Rectifiers;

The maximum current that goes through each switch is:

$$I_{SR1\&2_{rms}} = (\frac{N_1}{N_2}) I_{Transformer} = 80 \quad Amp. \qquad (5\text{-}7)$$

Therefore, due to a very high current in the synchronous rectifiers, these switches have to be chosen in such a way that have the least possible Drain to Source resistor $R_{ds(on)}$. A good selection for these two switches is HUF76143P3.

e) Output Capacitor;

The output capacitor acts as an energy storage element. It stores energy, when the input voltage and current are near their peak and provides this energy to the output load when the line is low. The output capacitor filters out the second harmonic current that flows through the synchronous rectifiers. The criterion for the selection of this capacitor is the amount of tolerable ripple in the output voltage, as well as ESL and ESR of the output capacitor. The selected capacitors are 100 μH and 10 μH capacitors that can be placed in parallel to get the desired value. These capacitors are TDK capacitors, which are new, and have very low ESR and ESL.

5.2.2.1 Design of Control Circuit

The main issue in design of control circuit is to generate gating signals, which are synchronized with the current in the series branch of resonant tank. Figure 5-5 shows the principle of this control loop.

As can be seen, a Current Transformer senses the current in the series branch of resonant tank, and then this current is changed to a voltage. This voltage is then compared to a constant voltage to get a signal, which is in phase with that particular current. Then a triangle waveform is made to be compared with the feedback signal, coming from Error Amplifier. The IC used in this controller is UC3823.

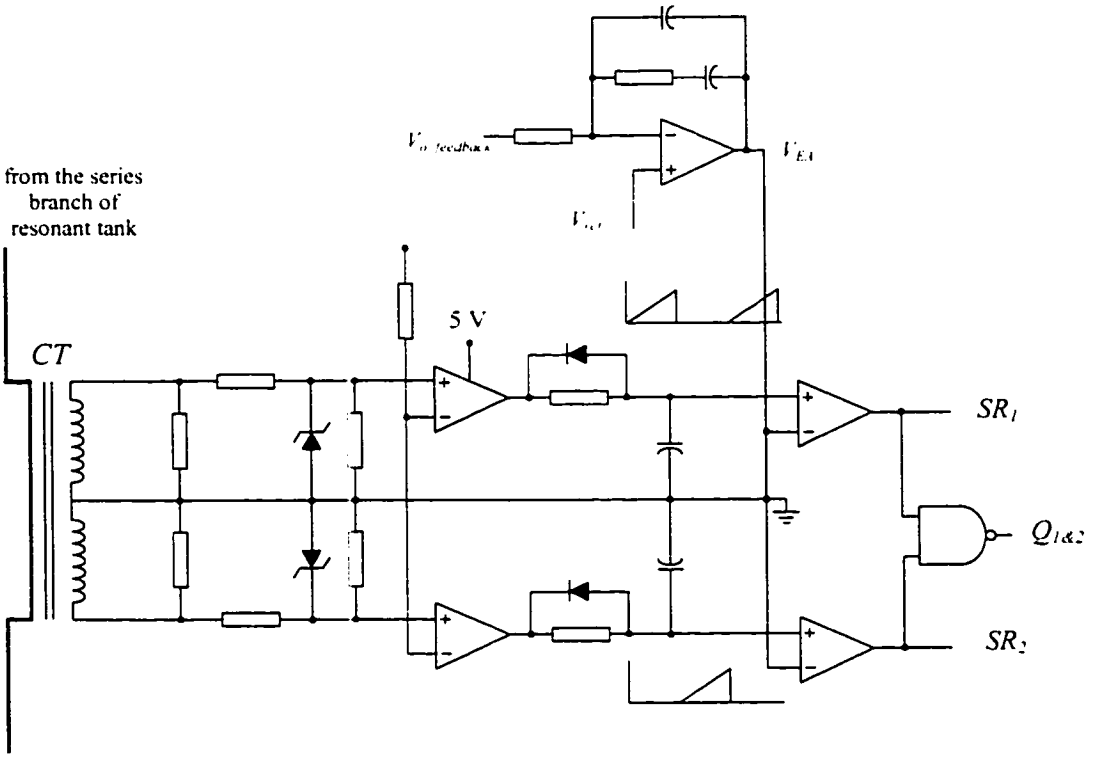


Figure 5- 5: Design of Control Loop for CPU VRM

5.3 Simulation and Experimental Results

The feasibility of the converter presented in this chapter was verified by results obtained from a 32 W experimental prototype switching at 2 MHz. The value of resonant inductor used was L_S = 4.4 μH, resonant series capacitor C_S = 6.8 nF, and resonant parallel capacitor of C_P = 15 nF. A higher value of output capacitor was used than what predicted theoretically as a small inductor was placed in between to make a π filter to reduce the ripples in the output voltage. HUF76143P3 was the MOSFET used for the

synchronous rectification. To avoid heating up the switches, two switches were placed in parallel as a synchronous rectifier.

According to design criteria given in this chapter, an example circuit (the prototype) is designed. The principle parameters and selected devices used in simulation are listed in Table5-1.

Table5- 1: Principle Parameters of the Simulation Circuit in PSIM

Parameter	Value	Parameter	Value
V_S	28 V rms	C_o	480 µF
P_o	32 W	C_S	6.8 nF
f_S	2 MHz	L_S	4.4 µH
k	8.8:1:1	C_P	15 nF

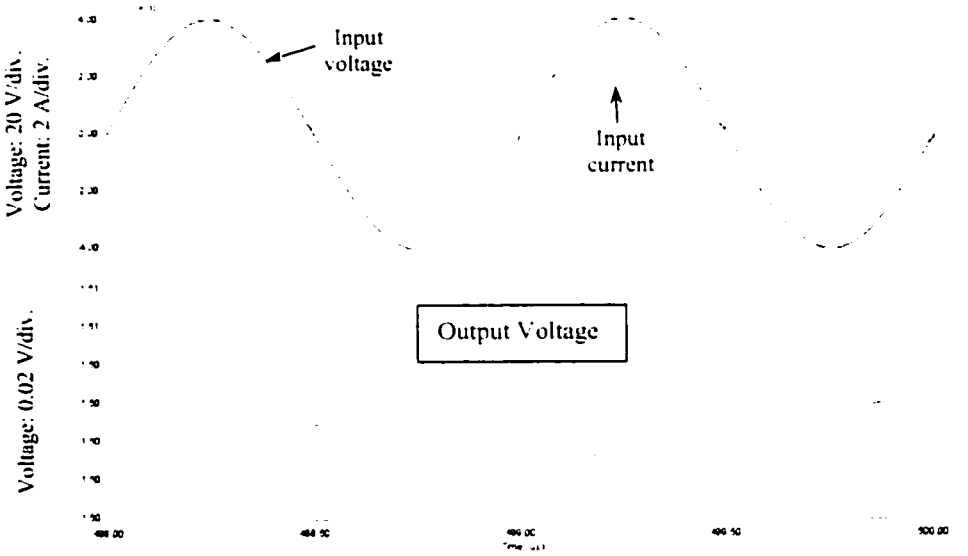


Figure 5- 6: Input current and voltage, and output voltage

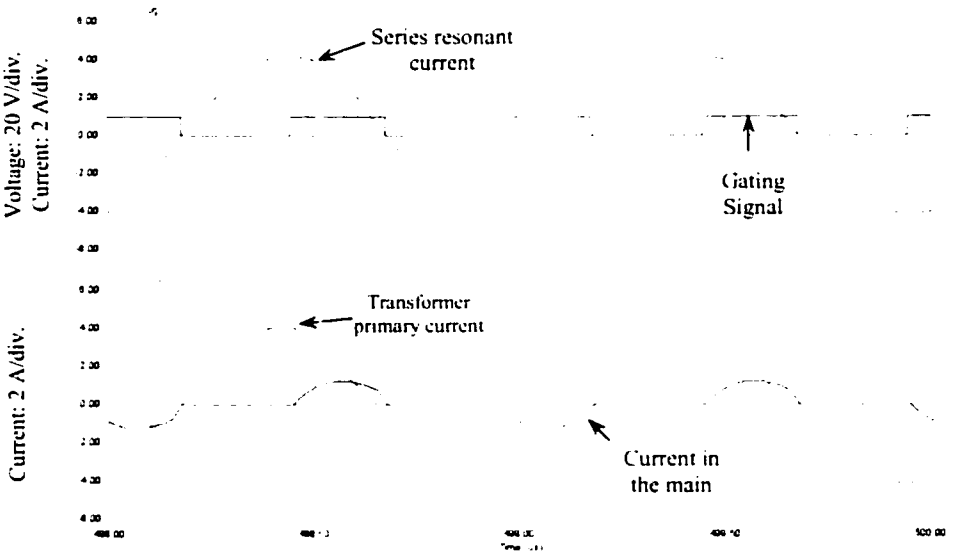


Figure 5- 7: Current in series branch and gating of the main switches Current in the main switches and the primary of transformer

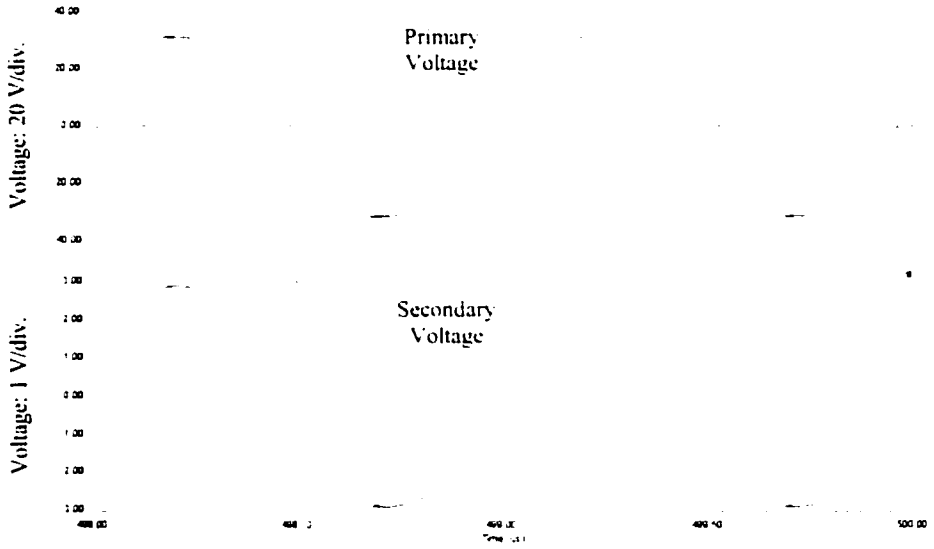


Figure 5- 8: Voltage in the primary and secondary of the transformer

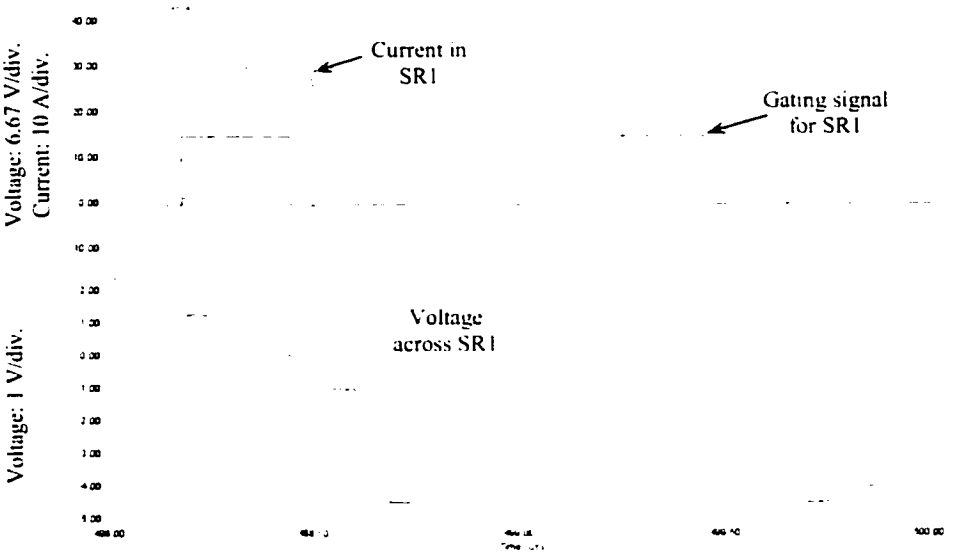


Figure 5- 9: Current, voltage, and gating of SR_1

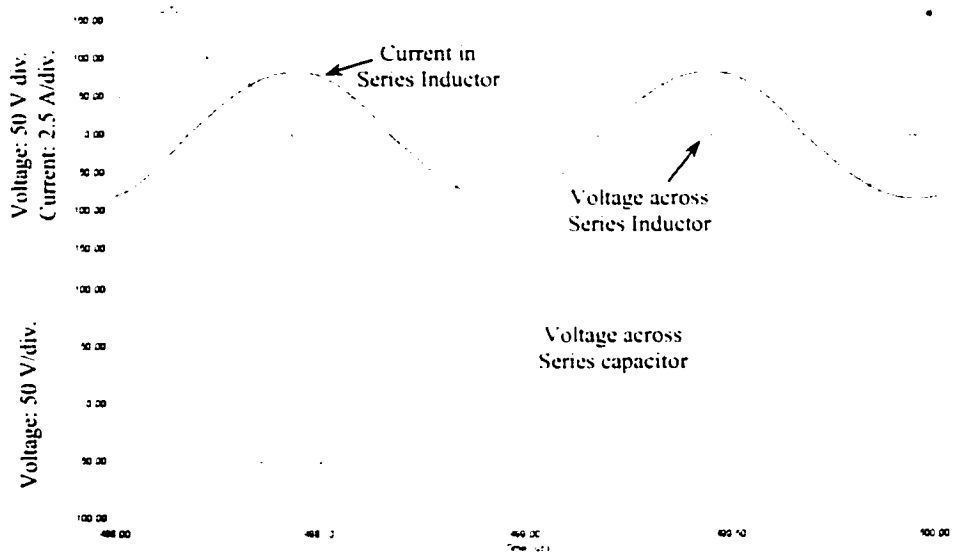
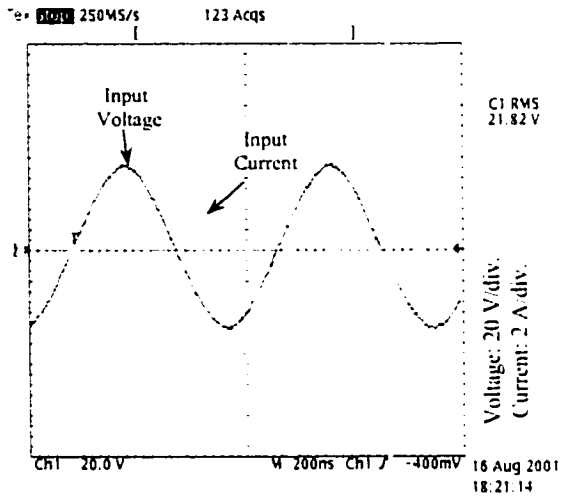
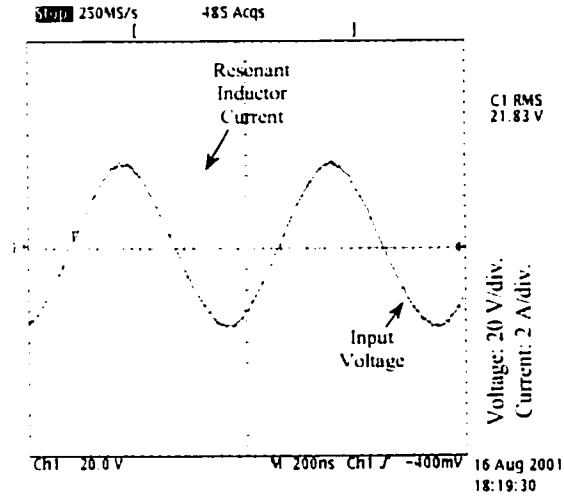


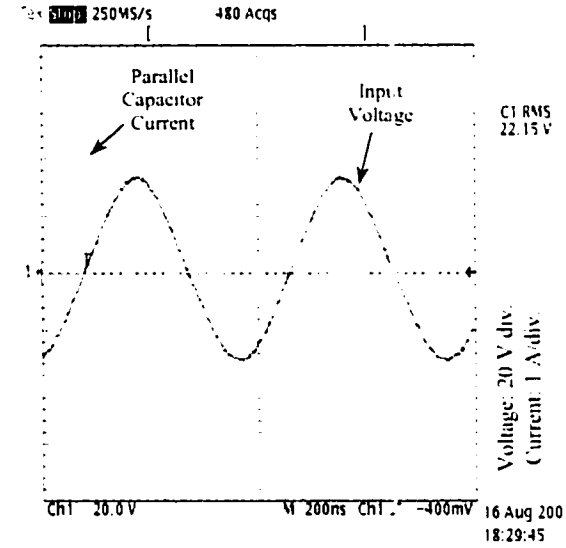
Figure 5- 10: Current and voltage of series inductor, and voltage of series capacitor



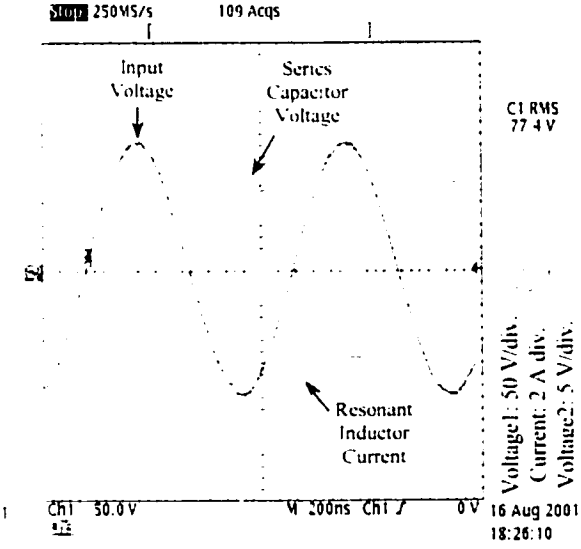
(a) Input Voltage and Current



(b) Input Voltage, Resonant Inductor Current

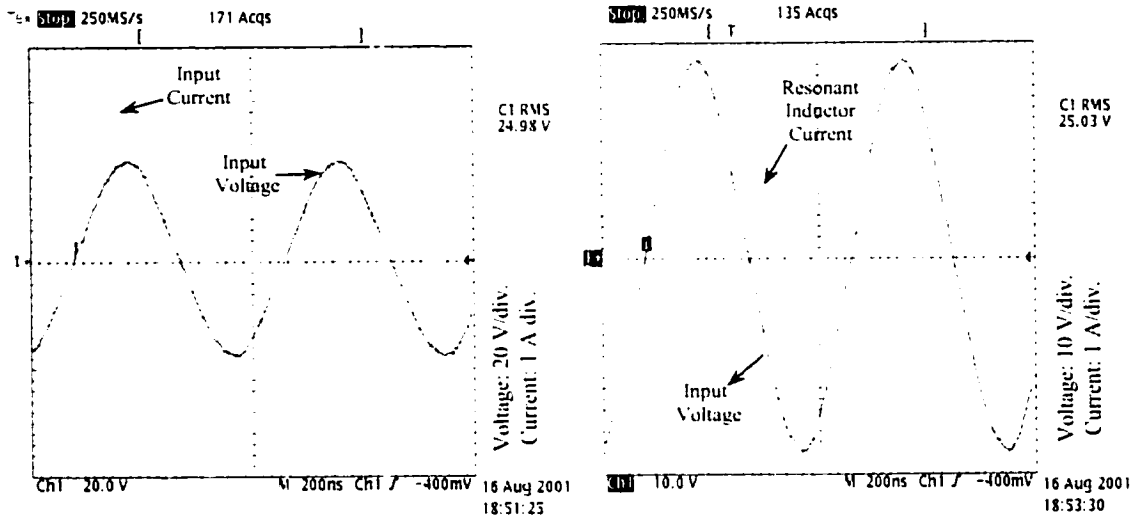


(c)Input Voltage, Parallel Capacitor Current



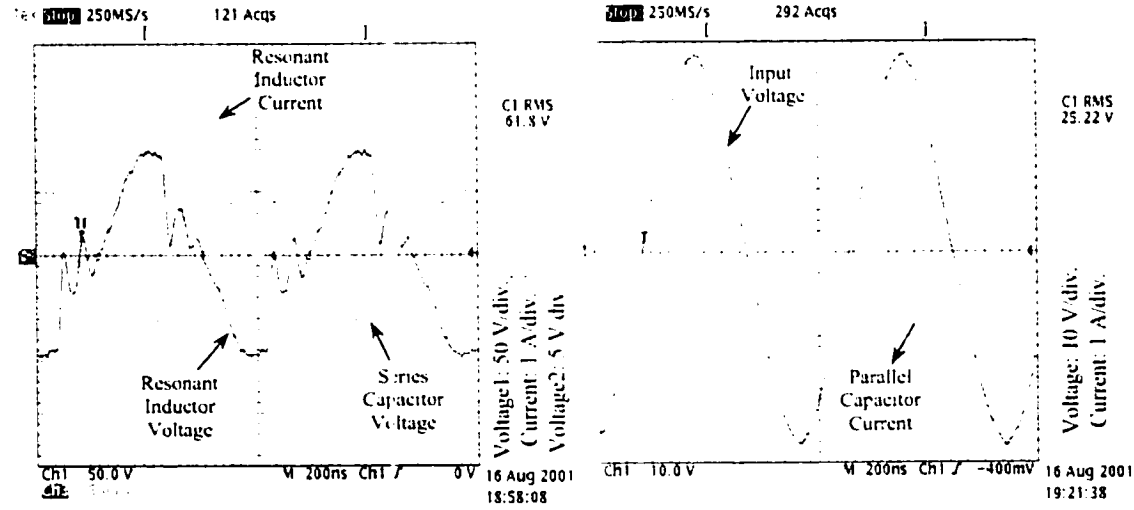
(d)Input & Resonant Capacitor voltage and Resonant Inductor voltage

Figure 5- 11: Current and Voltage in different branches and devices when both main switches are fully conducting



(a) Input Voltage and Current

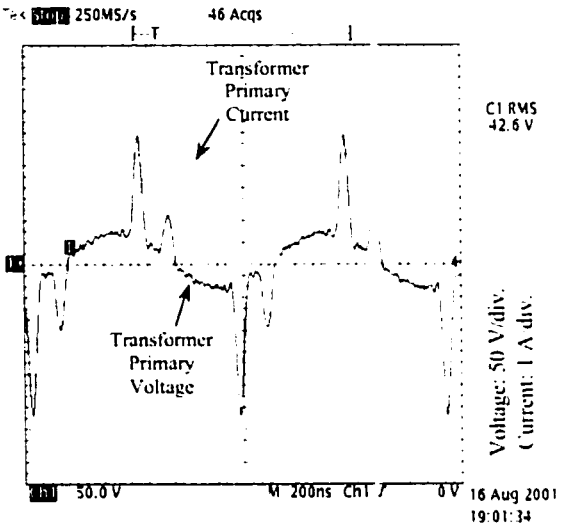
(b) Input Voltage, Resonant Inductor Current



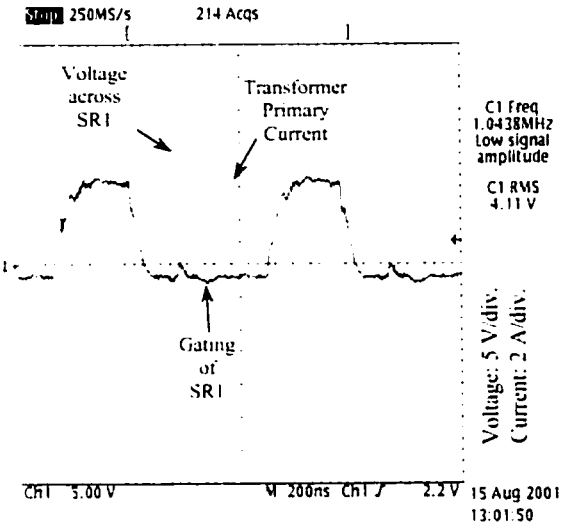
(c) Inductor & Resonant Capacitor voltage Resonant Inductor Current

(d) Input Voltage, Resonant Parallel Capacitor current

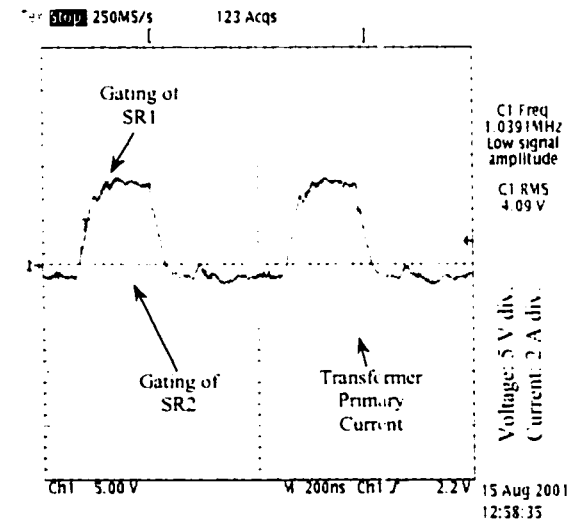
Figure 5- 12:Current and Voltage in different branches and devices when both two switches are fully off



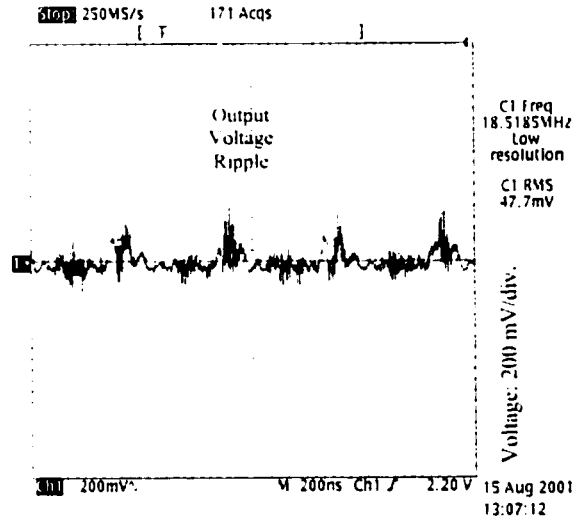
(a) Voltage and Current in Primary of Transformer



(b) Current and gating of SR_1, Transformer Primary Current



(c) Gating of SR_1&SR_2, Transformer Primary Current



(d) Output Voltage Ripple

Figure 5- 13:Current and Voltage in different branches and devices when both main switches are fully off

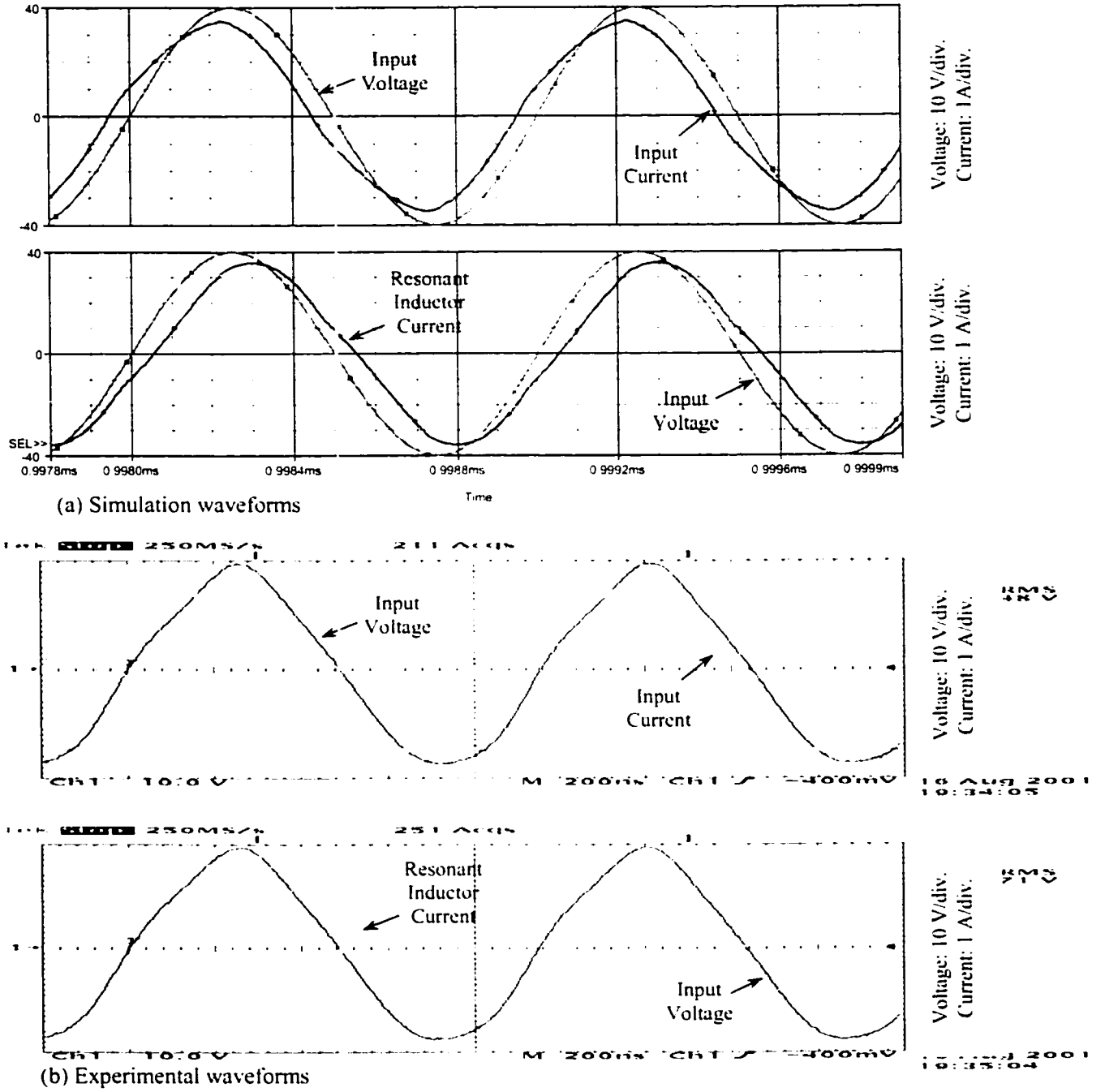


Figure 5- 14: Input Voltage, Input Current - Input voltage. Resonant Inductor Current

(a) Simulation result (b) Experimental result

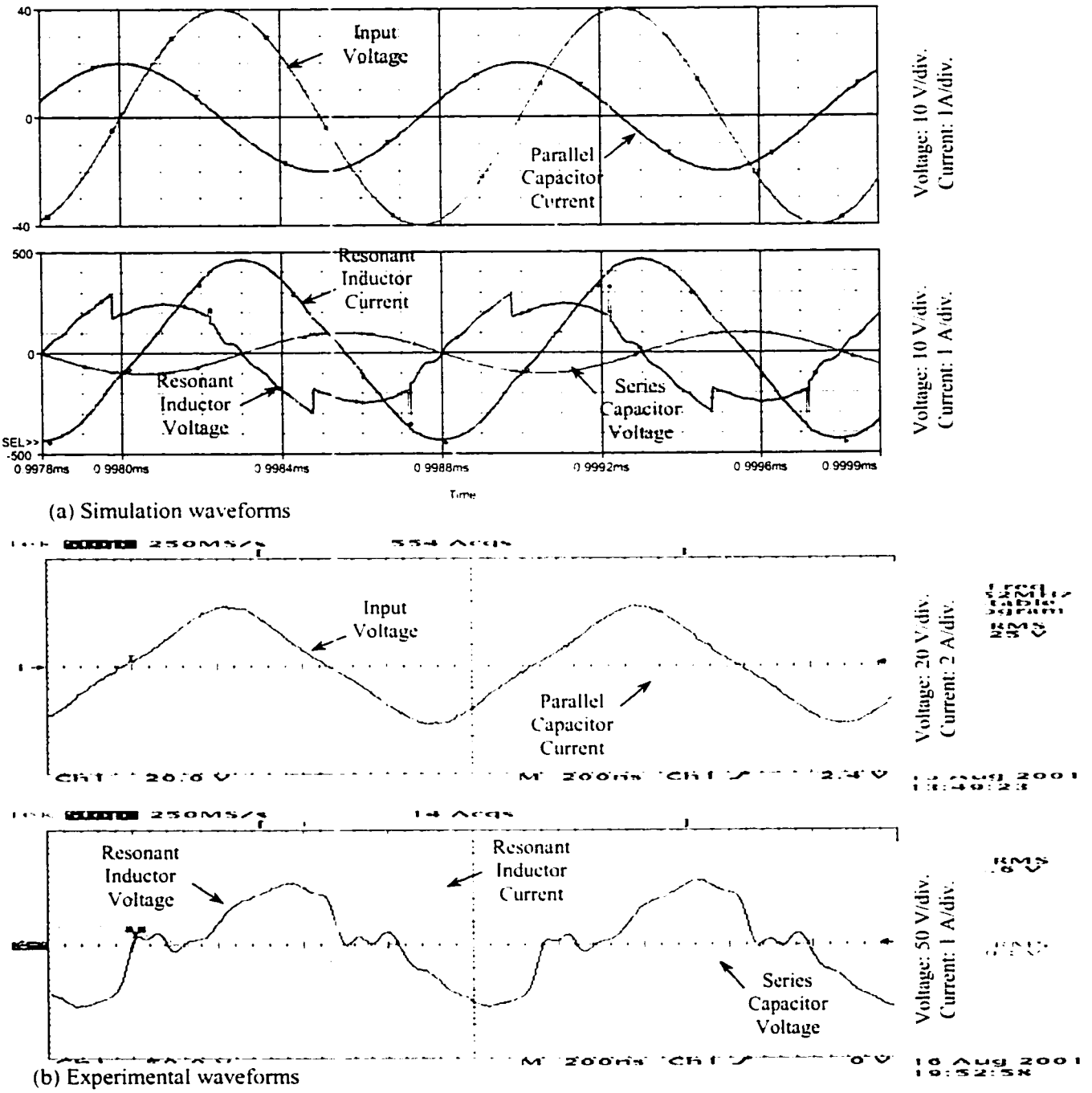
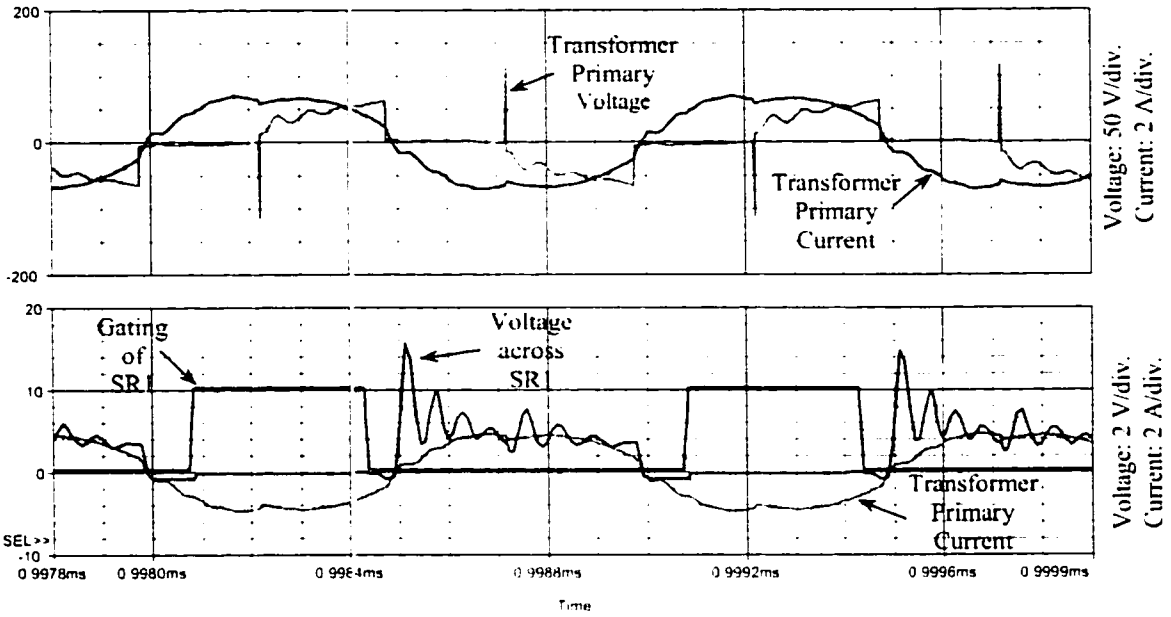
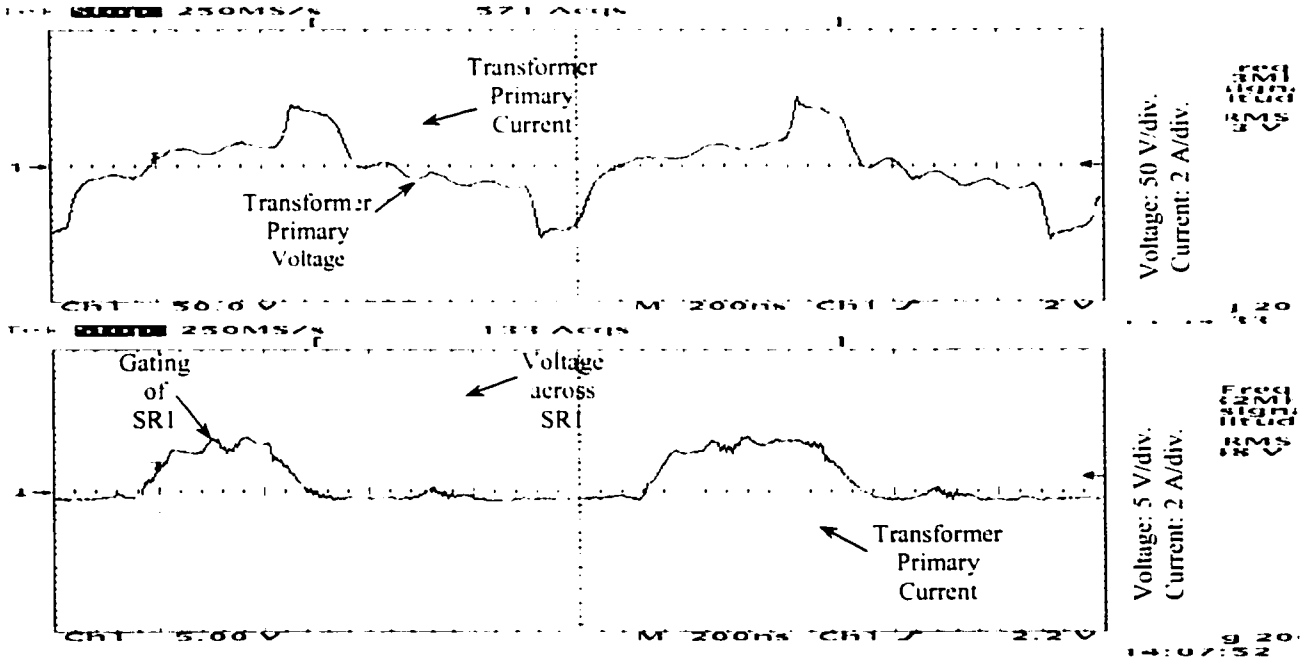


Figure 5- 15:Input Voltage, Resonant Capacitor Current – Resonant Capacitor and inductor Voltage and Resonant Inductor Current (a) Simulation Results (b) Experimental Results



(a) Simulation waveforms



(b) Experimental waveforms

Figure 5- 16: Voltage and current in primary of transformer – Current and Gating Voltage of SR1 and current in Primary of transformer (a) Simulation (b) Experimental

As can be seen, Figure5-11 shows the experimental results when both main switches are fully conducting. Figure5-12 and Figure5-13 shows the experimental results when both main switches are fully off and the results are as expected. Figure5-14 to Figure5-16 shows the experimental along with the simulation results. Due to the fact that the gating is not as it assumed in all analyses, therefore, the results are not like the simulation and analysis.

5.4 Conclusion

In this chapter, design guidelines were laid down and a design example was presented to the proposed converter. Use was made of the characteristic curves presented in chapter 3, and equations were developed in this chapter to assist in the selection of the component values of the converter.

From the design example a prototype was developed from which experimental results were taken. Simulation results were also presented. Both simulation and experimental results verify that in the input, a close to unity power factor with very small THD, and almost constant sinusoidal current in the series branch of converter was attainable. The results match the simulated results too and prove the validity of the design procedure used.

CHAPTER 6

SUMMARY AND CONTRIBUTIONS

6.1 Summary

This thesis proposed a resonant AC/DC converter for high frequency AC VRM for high frequency power distribution systems. The primary objective was to achieve a rigid current source to the load and a sinusoidal input current in phase with the source voltage. This has been done by proper selection of resonant network operating at very high frequency. By operating at a very high frequency, the converter's physical size was reduced. Therefore high frequency and high power density could be achieved.

This work is summarized as follows:

In chapter 1, the overall power architectures are reviewed.

In chapter 2, a unity power factor resonant AC/DC converter for HF AC VRM is presented. The operating principal is described and the steady state analysis is performed. It is found that the leakage inductance of the transformer has a big impact on the performance of the converter. Then the analysis was verified by the simulation results of a prototype converting the input AC voltage of 30 V rms at 1 MHz, to 1.6 V DC at 50 A.

In chapter 3, the effect of leakage inductance on the converter is explored. Again the operating principal is described and the steady state analysis is performed with considering the leakage inductance of the transformer. It is noticed that a rigid current source can be achieved in all load conditions, but the power factor is close to unity in full load.

In chapter 4, the dynamic property and control theory for the converter is explained and a voltage compensator is designed. The power stage transfer function is derived based on the averaged state space equations. Simulation results are presented to verify the analysis and design.

In chapter 5, the HF AC/DC converter is proposed to optimize the design. By designing a proper resonant network, we could get a rigid current source to the load and close to unity power factor. A design procedure is developed, component selection curves and criteria are presented for the general-purpose application, and an example is given.

6.2 Contributions

The contributions to this work include:

(i) The main contribution is analysis of AC/DC resonant converter for the application including the effect of leakage inductance.

(ii) The development of performance characteristics of the proposed converter.

(iii) Development of easy to follow design procedure for the proposed converter.

(iv) Verification of design and analysis from experimental and simulation results.

(v) Detailed dynamic analysis.

6.3 Suggestion for Future Work

In order to extend the work presented in this thesis the following topics can be examined:

(i) It was seen that turning on the main switches under the voltage, causes switching losses therefore lower efficiency. We may improve the overall efficiency by using ZVS techniques in turning on the main switches.

(ii) It can be examined whether the result of this thesis can be extended by using trapezoidal waveform in the input of the converter instead of sinusoidal waveform.

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APPENDIX 1

Mathematical Analyses carried out in MathCAD for Chapter 2

Defining Some Constant Values:

$\alpha := 0, 0.1 .. 3.3$ $\quad Z_{S1} := 1.5$ $\quad Z_{S2} := 3$ $\quad Z_{S3} := 5$

$k := 15$ $\quad R_o := 0.032$ $\quad V_S := 30$

$\phi 1 := \frac{\pi}{3}$ $\quad \phi 2 := \frac{\pi}{3}$ $\quad \phi 3 := \frac{\pi}{2.81}$

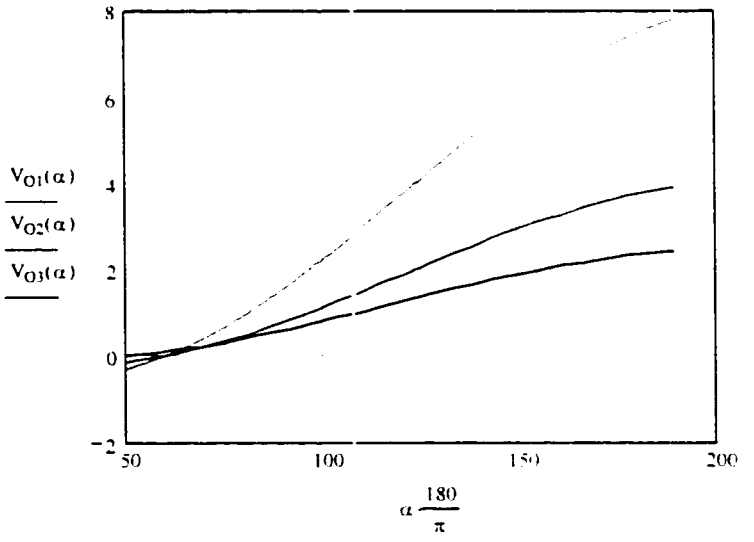
Defined Formulas:

$$V_{O1}(\alpha) := \frac{-2\sqrt{2}\cdot V_S}{\pi} k \cdot \frac{R_o}{Z_{S1}} \cdot \sin\left(\frac{\alpha}{2}\right) \cdot \cos\left(\frac{2\phi 1 + \alpha}{2}\right)$$

$$V_{O2}(\alpha) := \frac{-2\sqrt{2}\cdot V_S}{\pi} k \cdot \frac{R_o}{Z_{S2}} \cdot \sin\left(\frac{\alpha}{2}\right) \cdot \cos\left(\frac{2\phi 2 + \alpha}{2}\right)$$

$$V_{O3}(\alpha) := \frac{-2\sqrt{2}\cdot V_S}{\pi} k \cdot \frac{R_o}{Z_{S3}} \cdot \sin\left(\frac{\alpha}{2}\right) \cdot \cos\left(\frac{2\phi 3 + \alpha}{2}\right)$$

The Out put Voltage as a Function of Control Angle:



$$V_{O1}\left(110 \frac{\pi}{180}\right) = 2.992$$

$$V_{O2}\left(110 \frac{\pi}{180}\right) = 1.496$$

$$V_{O3}\left(144 \frac{\pi}{180}\right) = 1.776$$

Defining Some Constant Values:

$V_s := 30 \quad V_o := 1.6 \quad m := 1,2..15 \quad k := 15 \quad \phi := \frac{\pi}{3} \quad \alpha := 0, 0.02.. 3.14$

$X_{Cs1} := 20 \quad X_{Cs2} := 6.5 \quad X_{Cs3} := 26.25$

$X_{Ls1} := 25 \quad X_{Ls2} := 8 \quad X_{Ls3} := 30$

$X_{Cp1} := 11 \quad X_{Cp2} := 3.1 \quad X_{Cp3} := 8.2$

The Impedance of Resonant Tank:

$$Z_{t1} := \frac{X_{Cp1}\cdot(X_{Ls1} - X_{Cs1})}{X_{Ls1} - X_{Cs1} - X_{Cp1}} \qquad Z_{t2} := \frac{X_{Cp2}\cdot(X_{Ls2} - X_{Cs2})}{X_{Ls2} - X_{Cs2} - X_{Cp2}} \qquad Z_{t3} := \frac{X_{Cp3}\cdot(X_{Ls3} - X_{Cs3})}{X_{Ls3} - X_{Cs3} - X_{Cp3}}$$

$Z_{s1} := X_{Ls1} - X_{Cs1} \qquad Z_{s2} := X_{Ls2} - X_{Cs2} \qquad Z_{s3} := X_{Ls3} - X_{Cs3}$

To Find out Parameters, A - B - C and angle θ :

$$A_1(\alpha) := \frac{\sqrt{2}\cdot V_s}{Z_{t1}} + \frac{4V_o}{\pi\cdot Z_{s1}}\cdot k\cdot\sin\left(\frac{\alpha}{2}\right)\cdot\sin\left(\frac{2\phi + \alpha}{2}\right) \qquad B_1(\alpha) := \frac{-4V_o}{\pi Z_{s1}}\cdot k\cdot\sin\left(\frac{\alpha}{2}\right)\cdot\cos\left(\frac{2\phi + \alpha}{2}\right)$$

$$C_1(\alpha) := \sqrt{(A_1(\alpha))^2 + (B_1(\alpha))^2} \qquad \theta_1(\alpha) := \operatorname{atan}\left(\frac{A_1(\alpha)}{B_1(\alpha)}\right) \qquad Z_{s1}(m) := (2m - 1)\cdot X_{Ls1} - \frac{X_{Cs1}}{2m - 1}$$

$$A_2(\alpha) := \frac{\sqrt{2}\cdot V_s}{Z_{t2}} + \frac{4V_o}{\pi\cdot Z_{s2}}\cdot k\cdot\sin\left(\frac{\alpha}{2}\right)\cdot\sin\left(\frac{2\phi + \alpha}{2}\right) \qquad B_2(\alpha) := \frac{-4V_o}{\pi Z_{s2}}\cdot k\cdot\sin\left(\frac{\alpha}{2}\right)\cdot\cos\left(\frac{2\phi + \alpha}{2}\right)$$

$$C_2(\alpha) := \sqrt{(A_2(\alpha))^2 + (B_2(\alpha))^2} \qquad \theta_2(\alpha) := \operatorname{atan}\left(\frac{A_2(\alpha)}{B_2(\alpha)}\right) \qquad Z_{s2}(m) := (2m - 1)\cdot X_{Ls2} - \frac{X_{Cs2}}{2m - 1}$$

$$A_3(\alpha) := \frac{\sqrt{2}\cdot V_s}{Z_{t3}} + \frac{4V_o}{\pi\cdot Z_{s3}}\cdot k\cdot\sin\left(\frac{\alpha}{2}\right)\cdot\sin\left(\frac{2\phi + \alpha}{2}\right) \qquad B_3(\alpha) := \frac{-4V_o}{\pi Z_{s3}}\cdot k\cdot\sin\left(\frac{\alpha}{2}\right)\cdot\cos\left(\frac{2\phi + \alpha}{2}\right)$$

$$C_3(\alpha) := \sqrt{(A_3(\alpha))^2 + (B_3(\alpha))^2} \qquad \theta_3(\alpha) := \operatorname{atan}\left(\frac{A_3(\alpha)}{B_3(\alpha)}\right) \qquad Z_{s3}(m) := (2m - 1)\cdot X_{Ls3} - \frac{X_{Cs3}}{2m - 1}$$

Harmonics Of Input Current:

$$I_1(\alpha) := \frac{C_3(\alpha)}{\sqrt{2}} \qquad I_3(\alpha) := \frac{4 \cdot V_o}{3\sqrt{2} \cdot \pi \cdot Z_{s3}(2)} \cdot k \cdot \sin\left(\frac{3\alpha}{2}\right)$$

$$I_5(\alpha) := \frac{4 \cdot V_o}{5\sqrt{2} \cdot \pi \cdot Z_{s3}(3)} \cdot k \cdot \sin\left(\frac{5\alpha}{2}\right) \qquad I_7(\alpha) := \frac{4 \cdot V_o}{7\sqrt{2} \cdot \pi \cdot Z_{s3}(4)} \cdot k \cdot \sin\left(\frac{7\alpha}{2}\right)$$

THD of Input Current:

$$THD1(\alpha) := \frac{4V_o}{\pi \cdot C_1(\alpha)} k \sqrt{\sum_{m=2}^{15} \left[\frac{1}{(2m-1) \cdot Z_{s1}(m)} \cdot \sin\left[\frac{(2m-1) \cdot \alpha}{2}\right]\right]^2}$$

$$THD2(\alpha) := \frac{4V_o}{\pi \cdot C_2(\alpha)} k \sqrt{\sum_{m=2}^{15} \left[\frac{1}{(2m-1) \cdot Z_{s2}(m)} \cdot \sin\left[\frac{(2m-1) \cdot \alpha}{2}\right]\right]^2}$$

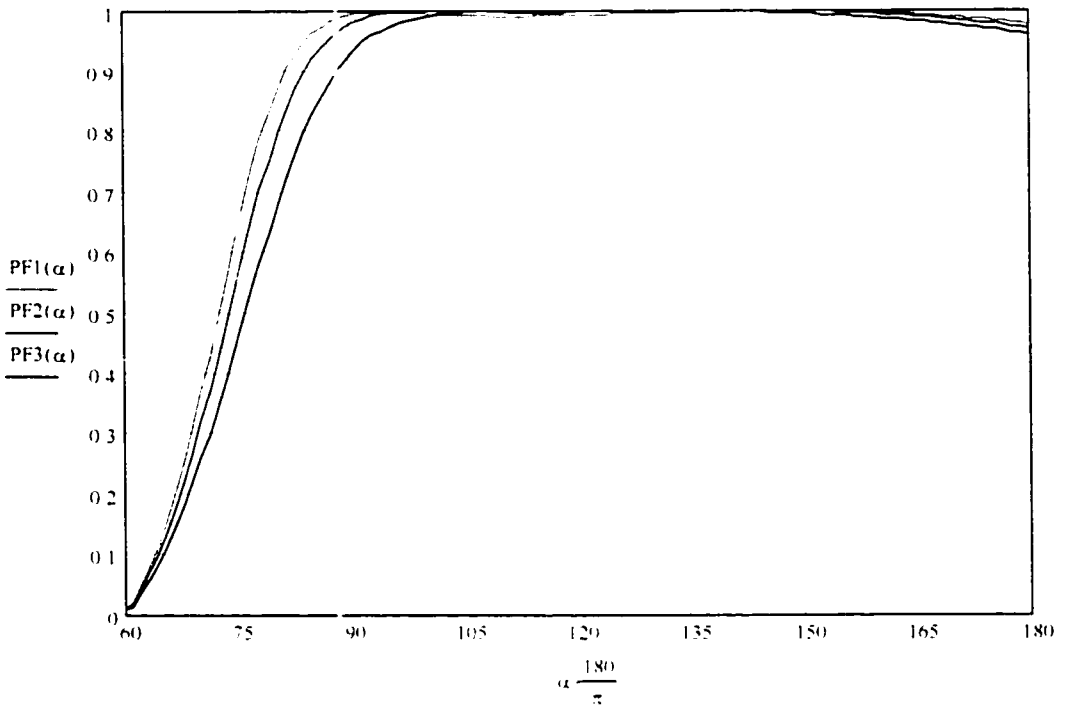
$$THD3(\alpha) := \frac{4V_o}{\pi \cdot C_3(\alpha)} k \sqrt{\sum_{m=2}^{15} \left[\frac{1}{(2m-1) \cdot Z_{s3}(m)} \cdot \sin\left[\frac{(2m-1) \cdot \alpha}{2}\right]\right]^2}$$

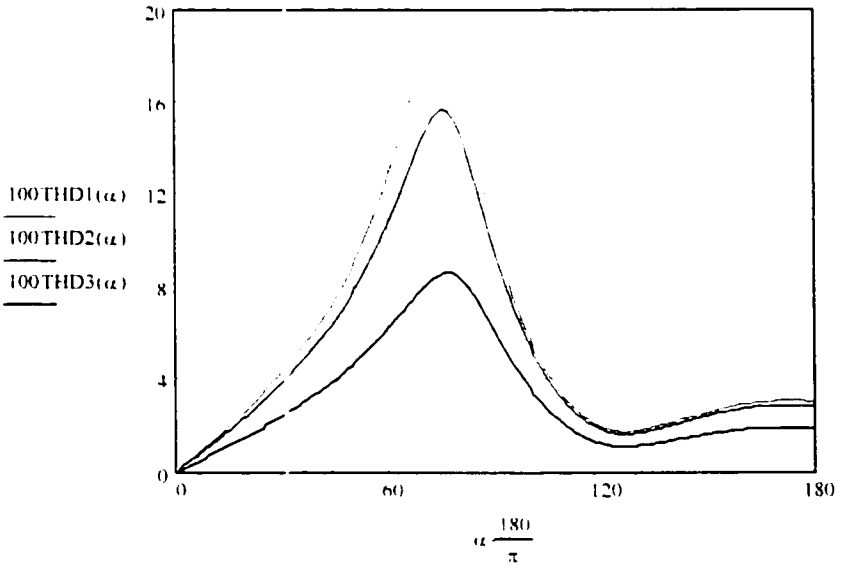
Power Factor:

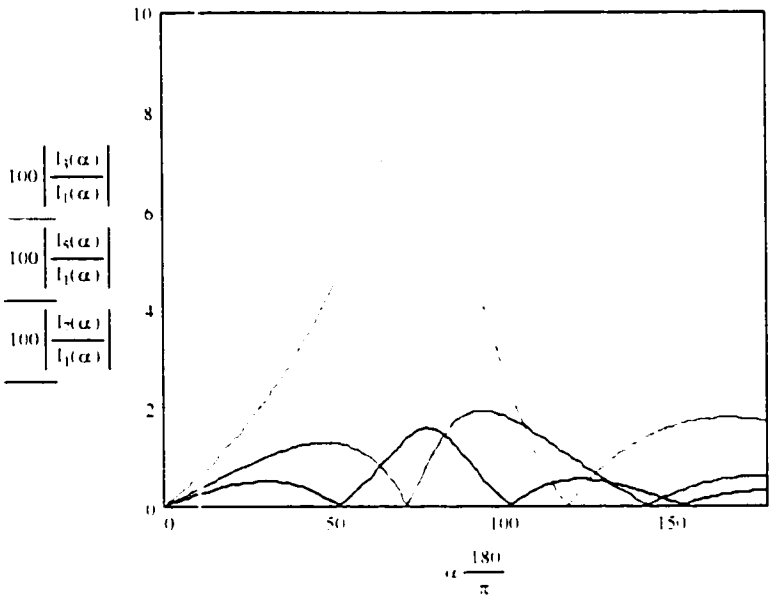
$$PF1(\alpha) := \frac{\cos(\theta_1(\alpha))}{\sqrt{1 + (THD1(\alpha))^2}} \qquad PF2(\alpha) := \frac{\cos(\theta_2(\alpha))}{\sqrt{1 + (THD1(\alpha))^2}} \qquad PF3(\alpha) := \frac{\cos(\theta_3(\alpha))}{\sqrt{1 + (THD1(\alpha))^2}}$$

Some Calculated Values:

$$PF1\left(144\frac{\pi}{180}\right) = 1 \qquad \theta_1\left(144\frac{\pi}{180}\right)\cdot\frac{180}{\pi} = 1.132 \qquad 100THD1\left(144\frac{\pi}{180}\right) = 2.335$$


PF1(α)
PF2(α)
PF3(α)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
60
75
90
105
120
135
150
165
180
α 180/π


100THD1(α)
100THD2(α)
100THD3(α)
20
16
12
8
4
0
0
60
120
180
α 180/π



$$100\left|\frac{I_3\left(144\frac{\pi}{180}\right)}{I_1\left(144\frac{\pi}{180}\right)}\right| = 1.417$$

$$100\left|\frac{I_5\left(144\frac{\pi}{180}\right)}{I_1\left(144\frac{\pi}{180}\right)}\right| = 0$$

$$100\left|\frac{I_7\left(144\frac{\pi}{180}\right)}{I_1\left(144\frac{\pi}{180}\right)}\right| = 0.239$$

Some Constant Values:

$k := 15 \quad R_0 := 0.032 \quad m := 1,2..45 \quad \alpha := 0, 0.01.. 3.3$

$X_{Ls1} := 5 \quad X_{Cs1} := 3.5 \quad X_{Ls2} := 10 \quad X_{Cs2} := 7 \quad X_{Ls3} := 25 \quad X_{Cs3} := 20$

$Z_{S1}(m) := (2m - 1)\cdot X_{Ls1} - \frac{X_{Cs1}}{2m - 1} \quad k1 := 15 \quad k2 := 15 \quad k3 := 15$

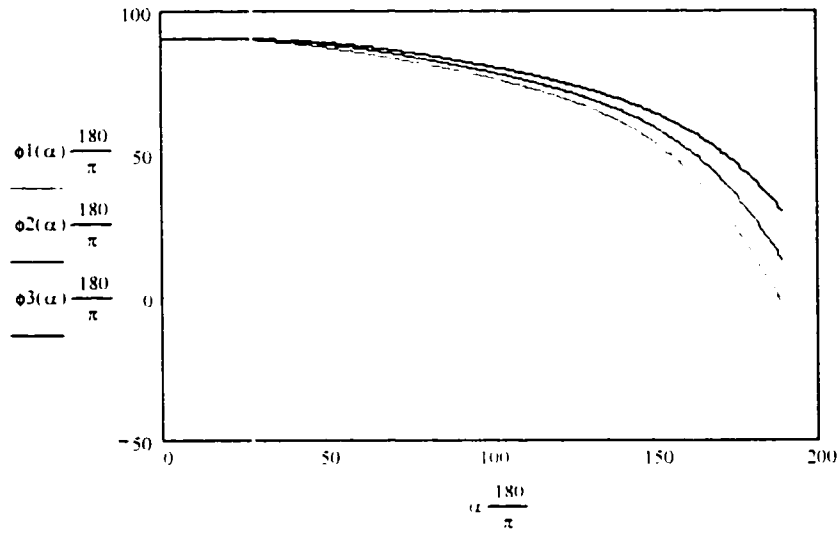
$Z_{S3}(m) := (2m - 1)\cdot X_{Ls3} - \frac{X_{Cs3}}{2m - 1} \quad Z_{S2}(m) := (2m - 1)\cdot X_{Ls2} - \frac{X_{Cs2}}{2m - 1}$

Defined Formulas:

$$\phi 1(\alpha) := \operatorname{atan}\left[\frac{\frac{16}{\pi^2}\cdot k1^2\cdot\sin(\alpha)\cdot\left[\sum_{m=1}^{5}\frac{1}{2m-1}\cdot\frac{R_0}{Z_{S1}(m)}\cdot\sin\left[\frac{(2m-1)\cdot\alpha}{2}\right]\cdot\cos\left[\frac{(2m-1)\cdot(\pi-\alpha)}{2}\right]\right]+1}{\frac{8}{\pi^2}\cdot k1^2\cdot\left(\sin\left(\frac{\alpha}{2}\right)\right)^2\cdot\left[\sum_{m=1}^{45}\frac{1}{2\cdot m-1}\cdot\frac{R_0}{Z_{S1}(m)}\cdot\sin\left[\frac{(2m-1)\cdot\alpha}{2}\right]\cdot\cos\left[\frac{(2m-1)\cdot(\pi-\alpha)}{2}\right]\right]}\right]$$

$$\phi 2(\alpha) := \operatorname{atan}\left[\frac{\frac{16}{\pi^2}\cdot k2^2\cdot\sin(\alpha)\cdot\left[\sum_{m=1}^{5}\frac{1}{2m-1}\cdot\frac{R_0}{Z_{S2}(m)}\cdot\sin\left[\frac{(2m-1)\cdot\alpha}{2}\right]\cdot\cos\left[\frac{(2m-1)\cdot(\pi-\alpha)}{2}\right]\right]+1}{\frac{8}{\pi^2}\cdot k2^2\cdot\left(\sin\left(\frac{\alpha}{2}\right)\right)^2\cdot\left[\sum_{m=1}^{45}\frac{1}{2\cdot m-1}\cdot\frac{R_0}{Z_{S2}(m)}\cdot\sin\left[\frac{(2m-1)\cdot\alpha}{2}\right]\cdot\cos\left[\frac{(2m-1)\cdot(\pi-\alpha)}{2}\right]\right]}\right]$$

$$\phi 3(\alpha) := \operatorname{atan}\left[\frac{\frac{16}{\pi^2}\cdot k3^2\cdot\sin(\alpha)\cdot\left[\sum_{m=1}^{5}\frac{1}{2m-1}\cdot\frac{R_0}{Z_{S3}(m)}\cdot\sin\left[\frac{(2m-1)\cdot\alpha}{2}\right]\cdot\cos\left[\frac{(2m-1)\cdot(\pi-\alpha)}{2}\right]\right]+1}{\frac{8}{\pi^2}\cdot k3^2\cdot\left(\sin\left(\frac{\alpha}{2}\right)\right)^2\cdot\left[\sum_{m=1}^{45}\frac{1}{2\cdot m-1}\cdot\frac{R_0}{Z_{S3}(m)}\cdot\sin\left[\frac{(2m-1)\cdot\alpha}{2}\right]\cdot\cos\left[\frac{(2m-1)\cdot(\pi-\alpha)}{2}\right]\right]}\right]$$



$$\phi 1\left(150\frac{\pi}{180}\right)\cdot\frac{180}{\pi} = 53.924$$

$$\phi 2\left(150\frac{\pi}{180}\right)\cdot\frac{180}{\pi} = 59.136$$

$$\phi 3\left(150\frac{\pi}{180}\right)\cdot\frac{180}{\pi} = 64.196$$

APPENDIX 2

Mathematical Analyses carried out in MathCAD for Chapter 3

The constant values:

$V_s := 30$ $V_o := 1.6$ $f := 10^6$ $X_{Cs2} := 5.1$ $X_{Cs1} := 20$ $X_{Cs3} := 23$

$\alpha := 0, 0.05 .. \pi$ $\omega_o := 2 \cdot \pi \cdot f$ $X_{Ls2} := 8$ $X_{Ls1} := 25$ $X_{Ls3} := 30$

$m := 2, 3 .. 50$ $X_{Cp2} := 3$ $X_{Cp1} := 10$ $X_{Cp3} := 11.25$

$k := 15$ $\phi := \frac{\pi}{3}$ $D := 0.2$ $X_{Ll2} := 0.05 \cdot X_{Ls2}$ $X_{Ll1} := 0.15 \cdot X_{Ls1}$ $X_{Ll3} := 0.1 \cdot X_{Ls3}$

$R_O := 0.032$ $C_{s1} := \frac{1}{\omega_o \cdot X_{Cs1}}$ $C_{s2} := \frac{1}{\omega_o \cdot X_{Cs2}}$ $C_{s3} := \frac{1}{\omega_o \cdot X_{Cs3}}$

$L_{s1} := \frac{X_{Ls1}}{\omega_o}$ $L_{s2} := \frac{X_{Ls2}}{\omega_o}$ $L_{s3} := \frac{X_{Ls3}}{\omega_o}$

$R_{eq} := \frac{8}{\pi^2} \cdot k^2 \cdot R_O$ $C_{p1} := \frac{1}{\omega_o \cdot X_{Cp1}}$ $C_{p2} := \frac{1}{\omega_o \cdot X_{Cp2}}$ $C_{p3} := \frac{1}{\omega_o \cdot X_{Cp3}}$

$L_{l1} := 0.1 \cdot L_{s1}$ $L_{l2} := 0.1 \cdot L_{s2}$ $L_{l3} := 0.1 \cdot L_{s3}$

The defined values:

$\xi 1 := \frac{R_{eq}}{2(L_{l1} + L_{s1})}$ $\xi 2 := \frac{R_{eq}}{2(L_{l2} + L_{s2})}$ $\xi 3 := \frac{R_{eq}}{2(L_{l3} + L_{s3})}$

$\omega_{s1} := \frac{1}{\sqrt{C_{s1} \cdot (L_{s1} + L_{l1})}}$ $\omega_{s2} := \frac{1}{\sqrt{C_{s2} \cdot (L_{s2} + L_{l2})}}$ $\omega_{s3} := \frac{1}{\sqrt{C_{s3} \cdot (L_{s3} + L_{l3})}}$

$\omega_{d1} := \frac{1}{\sqrt{L_{s1} \cdot C_{s1}}}$ $\omega_{d2} := \frac{1}{\sqrt{L_{s2} \cdot C_{s2}}}$ $\omega_{d3} := \frac{1}{\sqrt{L_{s3} \cdot C_{s3}}}$

$\omega_{r1} := \sqrt{\omega_{s1}^2 - \xi 1^2}$ $\omega_{r2} := \sqrt{\omega_{s2}^2 - \xi 2^2}$ $\omega_{r3} := \sqrt{\omega_{s3}^2 - \xi 3^2}$

$\omega_o := 2 \cdot \pi \cdot f$

The calculated parameters:

$$F1 := \frac{\sqrt{2}\cdot\omega_o\cdot V_s}{L_{s1}+L_{11}}\cdot\left[\left(\omega_{s1}^{\,2}-\omega_o^{\,2}\right)^2+\left(2\cdot\xi1\cdot\omega_o\right)^2\right]^{-1}\cdot 2\cdot\xi1\cdot\omega_o$$

$$E1 := \frac{\sqrt{2}\cdot\omega_o\cdot V_s}{L_{s1}+L_{11}}\cdot\left[\left(\omega_{s1}^{\,2}-\omega_o^{\,2}\right)^2+\left(2\cdot\xi1\cdot\omega_o\right)^2\right]^{-1}\cdot\left(\omega_{s1}^{\,2}-\omega_o^{\,2}\right)$$

$$F2 := \frac{\sqrt{2}\cdot\omega_o\cdot V_s}{L_{s2}+L_{12}}\cdot\left[\left(\omega_{s2}^{\,2}-\omega_o^{\,2}\right)^2+\left(2\cdot\xi2\cdot\omega_o\right)^2\right]^{-1}\cdot 2\cdot\xi2\cdot\omega_o$$

$$E2 := \frac{\sqrt{2}\cdot\omega_o\cdot V_s}{L_{s2}+L_{12}}\cdot\left[\left(\omega_{s2}^{\,2}-\omega_o^{\,2}\right)^2+\left(2\cdot\xi2\cdot\omega_o\right)^2\right]^{-1}\cdot\left(\omega_{s2}^{\,2}-\omega_o^{\,2}\right)$$

$$F3 := \frac{\sqrt{2}\cdot\omega_o\cdot V_s}{L_{s3}+L_{13}}\cdot\left[\left(\omega_{s3}^{\,2}-\omega_o^{\,2}\right)^2+\left(2\cdot\xi3\cdot\omega_o\right)^2\right]^{-1}\cdot 2\cdot\xi3\cdot\omega_o$$

$$E3 := \frac{\sqrt{2}\cdot\omega_o\cdot V_s}{L_{s3}+L_{13}}\cdot\left[\left(\omega_{s3}^{\,2}-\omega_o^{\,2}\right)^2+\left(2\cdot\xi3\cdot\omega_o\right)^2\right]^{-1}\cdot\left(\omega_{s3}^{\,2}-\omega_o^{\,2}\right)$$

$$M1 := R_{eq}\cdot E1 + L_{11}\cdot F1\cdot\omega_o \qquad N1 := R_{eq}\cdot F1 - L_{11}\cdot E1\cdot\omega_o \qquad M3 := R_{eq}\cdot E3 + L_{13}\cdot F3\cdot\omega_o$$

$$M2 := R_{eq}\cdot E2 + L_{12}\cdot F2\cdot\omega_o \qquad N2 := R_{eq}\cdot F2 - L_{12}\cdot E2\cdot\omega_o \qquad N3 := R_{eq}\cdot F3 - L_{13}\cdot E3\cdot\omega_o$$

$$Q1 := \sqrt{M1^2+N1^2} \qquad \beta1 := \operatorname{atan}\left(\frac{M1}{N1}\right)$$

$$Q2 := \sqrt{M2^2+N2^2} \qquad \beta2 := \operatorname{atan}\left(\frac{M2}{N2}\right) \qquad \beta(\alpha) := \phi - \frac{\pi-\alpha}{2}$$

$$Q3 := \sqrt{M3^2+N3^2} \qquad \beta3 := \operatorname{atan}\left(\frac{M3}{N3}\right)$$

The input current of power supply, and voltage in the primary side of transformer:

$$t := 0, 10^{-9} .. 50 \cdot 10^{-6}$$

$$v_s(t) := \sqrt{2} \cdot V_s \cdot \sin(\omega_0 \cdot t)$$

$$i_L(t) := E1 \cdot \cos(\omega_0 \cdot t) + F1 \cdot \sin(\omega_0 \cdot t)$$

$$g(t) := \text{if}\left[\text{mod}(\omega_0 \cdot t, \pi + \phi) \le (1 - D) \cdot \pi, 0, 1\right]$$

$$V_{s1}(t) := Q1 \cdot \sin(\omega_0 \cdot t + \beta 2)$$

$$v_{PT}(t) := \text{if}\left[\text{mod}(\omega_0 \cdot t, \pi + \phi) \le (1 - D) \cdot \pi, V_{s1}(t), 0\right]$$

$$Z_{t1} := \frac{-X_{Cp1} \cdot (X_{Ls1} - X_{Cs1})}{X_{Ls1} - X_{Cs1} - X_{Cp1}} \qquad Z_{t2} := \frac{-X_{Cp2} \cdot (X_{Ls2} - X_{Cs2})}{X_{Ls2} - X_{Cs2} - X_{Cp2}} \qquad Z_{t3} := \frac{-X_{Cp3} \cdot (X_{Ls3} - X_{Cs3})}{X_{Ls3} - X_{Cs3} - X_{Cp3}}$$

$$Z_{s1} := X_{Ls1} - X_{Cs1} \qquad Z_{s2} := X_{Ls2} - X_{Cs2} \qquad Z_{s3} := X_{Ls3} - X_{Cs3}$$

$$Z_{s1}(m) := m \cdot X_{Ls1} - \frac{X_{Cs1}}{m} \qquad Z_{s2}(m) := m \cdot X_{Ls2} - \frac{X_{Cs2}}{m} \qquad Z_{s3}(m) := m \cdot X_{Ls3} - \frac{X_{Cs3}}{m}$$

The calculated parameters:

$$a1(\alpha, m) := \frac{Q}{\pi}\left[\frac{\cos[(m-1)(\alpha+\phi)-\beta]}{m-1} - \frac{\cos[(1-m)(\alpha+\phi)-\beta]}{1-m} - \frac{\cos[(m-1)\phi-\beta]}{m-1} + \frac{\cos[(1-m)\phi-\beta]}{1-m} - \frac{\cos[(m-1)(\pi-\alpha-\phi)-\beta]}{m-1} + \frac{\cos[(1-m)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\cos[(m-1)(\pi-\phi)-\beta]}{m-1} - \frac{\cos[(1-m)(\pi-\phi)-\beta]}{1-m}\right]$$

$$b1(\alpha, m) := \frac{Q}{\pi}\left[\frac{\sin[(1-m)(\alpha+\phi)-\beta]}{1-m} - \frac{\sin[(m-1)(\alpha+\phi)-\beta]}{m-1} - \frac{\sin[(1-m)\phi-\beta]}{1-m} + \frac{\sin[(m-1)\phi-\beta]}{1-m} - \frac{\sin[(1-m)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\sin[(m-1)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\sin[(1-m)(\pi-\phi)-\beta]}{1-m} - \frac{\sin[(m-1)(\pi-\phi)-\beta]}{1-m}\right]$$

$$a2(\alpha, m) := \frac{Q}{\pi}\left[\frac{\cos[(m-1)(\alpha+\phi)-\beta]}{m-1} - \frac{\cos[(1-m)(\alpha+\phi)-\beta]}{1-m} - \frac{\cos[(m-1)\phi-\beta]}{m-1} + \frac{\cos[(1-m)\phi-\beta]}{1-m} - \frac{\cos[(m-1)(\pi-\alpha-\phi)-\beta]}{m-1} + \frac{\cos[(1-m)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\cos[(m-1)(\pi-\phi)-\beta]}{m-1} - \frac{\cos[(1-m)(\pi-\phi)-\beta]}{1-m}\right]$$

$$b2(\alpha, m) := \frac{Q}{\pi}\left[\frac{\sin[(1-m)(\alpha+\phi)-\beta]}{1-m} - \frac{\sin[(m-1)(\alpha+\phi)-\beta]}{m-1} - \frac{\sin[(1-m)\phi-\beta]}{1-m} + \frac{\sin[(m-1)\phi-\beta]}{1-m} - \frac{\sin[(1-m)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\sin[(m-1)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\sin[(1-m)(\pi-\phi)-\beta]}{1-m} - \frac{\sin[(m-1)(\pi-\phi)-\beta]}{1-m}\right]$$

$$a3(\alpha, m) := \frac{Q}{\pi}\left[\frac{\cos[(m-1)(\alpha+\phi)-\beta]}{m-1} - \frac{\cos[(1-m)(\alpha+\phi)-\beta]}{1-m} - \frac{\cos[(m-1)\phi-\beta]}{m-1} + \frac{\cos[(1-m)\phi-\beta]}{1-m} - \frac{\cos[(m-1)(\pi-\alpha-\phi)-\beta]}{m-1} + \frac{\cos[(1-m)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\cos[(m-1)(\pi-\phi)-\beta]}{m-1} - \frac{\cos[(1-m)(\pi-\phi)-\beta]}{1-m}\right]$$

$$b3(\alpha, m) := \frac{Q}{\pi}\left[\frac{\sin[(1-m)(\alpha+\phi)-\beta]}{1-m} - \frac{\sin[(m-1)(\alpha+\phi)-\beta]}{m-1} - \frac{\sin[(1-m)\phi-\beta]}{1-m} + \frac{\sin[(m-1)\phi-\beta]}{1-m} - \frac{\sin[(1-m)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\sin[(m-1)(\pi-\alpha-\phi)-\beta]}{1-m} + \frac{\sin[(1-m)(\pi-\phi)-\beta]}{1-m} - \frac{\sin[(m-1)(\pi-\phi)-\beta]}{1-m}\right]$$

To Calculate THD:

$$a11(\alpha) := \frac{Q1}{2\pi}\left[-\cos(2\alpha - \beta(\alpha) + 2\phi) - 2(\phi + \alpha)\cdot\sin(\beta(\alpha)) + \cos(2\phi - \beta(\alpha)) - 2\phi\cdot\sin(\beta(\alpha))\right]$$

$$b11(\alpha) := \frac{Q1}{2\pi}\left[2(\phi + \alpha)\cos(\beta(\alpha)) - \sin(2\alpha + 2\phi - \beta(\alpha)) - 2\phi\cdot\cos(\beta(\alpha)) + \sin(2\phi - \beta(\alpha))\right]$$

$$A1(\alpha) := \frac{\sqrt{2}\cdot V}{Z_{t1}} + \frac{a11(\alpha)}{Z_{s1}(1)} \qquad B1(\alpha) := \frac{b11(\alpha)}{Z_{s1}(1)}$$

$$THD1(\alpha) := \frac{\sqrt{\sum_{m=2}^{50}\left[\left(\frac{a1(\alpha,m)}{Z_{s1}(m)}\right)^2 + \left(\frac{b1(\alpha,m)}{Z_{s1}(m)}\right)^2\right]}}{\sqrt{\left(\frac{\sqrt{2}\cdot V_s}{Z_{t1}} + \frac{a11(\alpha)}{Z_{s1}(1)}\right)^2 + \left(\frac{b11(\alpha)}{Z_{s1}(1)}\right)^2}}$$

$$a12(\alpha) := \frac{Q2}{2\pi}\left[-\cos(2\alpha - \beta(\alpha) + 2\phi) - 2(\phi + \alpha)\cdot\sin(\beta(\alpha)) + \cos(2\phi - \beta(\alpha)) + 2\phi\cdot\sin(\beta(\alpha))\right]$$

$$b12(\alpha) := \frac{Q2}{2\pi}\left[2(\phi + \alpha)\cos(\beta(\alpha)) - \sin(2\alpha + 2\phi - \beta(\alpha)) - 2\phi\cdot\cos(\beta(\alpha)) + \sin(2\phi - \beta(\alpha))\right]$$

$$A2(\alpha) := \frac{\sqrt{2}\cdot V_s}{Z_{t2}} + \frac{a12(\alpha)}{Z_{s2}(1)} \qquad B2(\alpha) := \frac{b12(\alpha)}{Z_{s2}(1)}$$

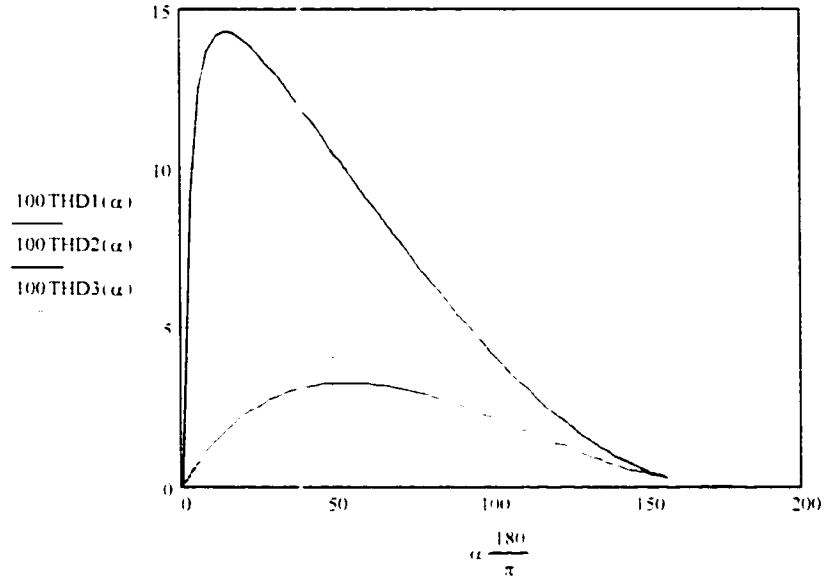
$$THD2(\alpha) := \frac{\sqrt{\sum_{m=2}^{50}\left[\left(\frac{a2(\alpha,m)}{Z_{s2}(m)}\right)^2 + \left(\frac{b2(\alpha,m)}{Z_{s2}(m)}\right)^2\right]}}{\sqrt{\left(\frac{\sqrt{2}\cdot V_s}{Z_{t2}} + \frac{a12(\alpha)}{Z_{s2}(1)}\right)^2 + \left(\frac{b12(\alpha)}{Z_{s2}(1)}\right)^2}}$$

$$a13(\alpha) := \frac{Q3}{2\pi}\left[-\cos(2\alpha - \beta(\alpha) + 2\phi) - 2(\phi + \alpha)\cdot\sin(\beta(\alpha)) + \cos(2\phi - \beta(\alpha)) + 2\phi\cdot\sin(\beta(\alpha))\right]$$

$$b13(\alpha) := \frac{Q3}{2\pi}\left[2(\phi + \alpha)\cos(\beta(\alpha)) - \sin(2\alpha + 2\phi - \beta(\alpha)) - 2\phi\cdot\cos(\beta(\alpha)) + \sin(2\phi - \beta(\alpha))\right]$$

$$A3(\alpha) := \frac{\sqrt{2}\cdot V_s}{Z_{t3}} + \frac{a13(\alpha)}{Z_{s3}(1)} \qquad B3(\alpha) := \frac{b13(\alpha)}{Z_{s3}(1)}$$

$$THD3(\alpha) := \frac{\sqrt{\sum_{m=2}^{50}\left[\left(\frac{a3(\alpha,m)}{Z_{s3}(m)}\right)^2 + \left(\frac{b3(\alpha,m)}{Z_{s3}(m)}\right)^2\right]}}{\sqrt{\left(\frac{\sqrt{2}\cdot V_s}{Z_{t3}} + \frac{a13(\alpha)}{Z_{s3}(1)}\right)^2 + \left(\frac{b13(\alpha)}{Z_{s3}(1)}\right)^2}}$$



$$100THD3\left(144\frac{\pi}{180}\right) = 0.62$$

To Find Out θ and Power Factor:

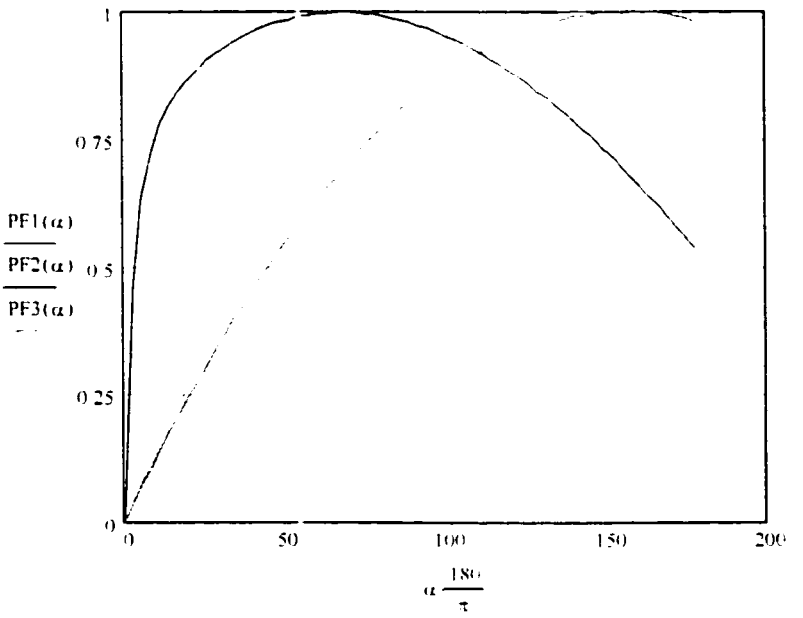
$$\theta 11(\alpha) := \operatorname{atan}\left(\frac{A1(\alpha)}{B1(\alpha)}\right) \qquad \theta 12(\alpha) := \operatorname{atan}\left(\frac{A2(\alpha)}{B2(\alpha)}\right) \qquad \theta 13(\alpha) := \operatorname{atan}\left(\frac{A3(\alpha)}{B3(\alpha)}\right)$$

$$\theta 11\left(144\frac{\pi}{180}\right)\cdot\frac{180}{\pi} = 6.833$$

$$PF1(\alpha) := \frac{\cos(\theta 11(\alpha))}{\sqrt{1 + (THD1(\alpha))^2}}$$

$$PF2(\alpha) := \frac{\cos(\theta 12(\alpha))}{\sqrt{1 + (THD2(\alpha))^2}}$$

$$PF3(\alpha) := \frac{\cos(\theta 13(\alpha))}{\sqrt{1 + (THD3(\alpha))^2}}$$



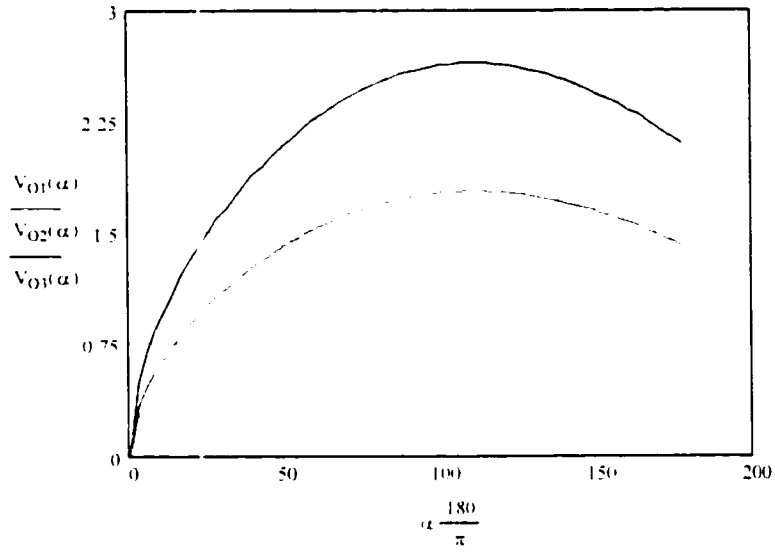
$$PF1\left(144\frac{\pi}{180}\right) = 0.993$$

To Find Out Output Voltage:

$$V_{O1}(\alpha) := \sqrt{\frac{V_s \cdot R_1}{\sqrt{2}} \cdot B1(\alpha)}$$

$$V_{O2}(\alpha) := \sqrt{\frac{V_s \cdot R_2}{\sqrt{2}} \cdot B2(\alpha)}$$

$$V_{O3}(\alpha) := \sqrt{\frac{V_s \cdot R_3}{\sqrt{2}} \cdot B3(\alpha)}$$

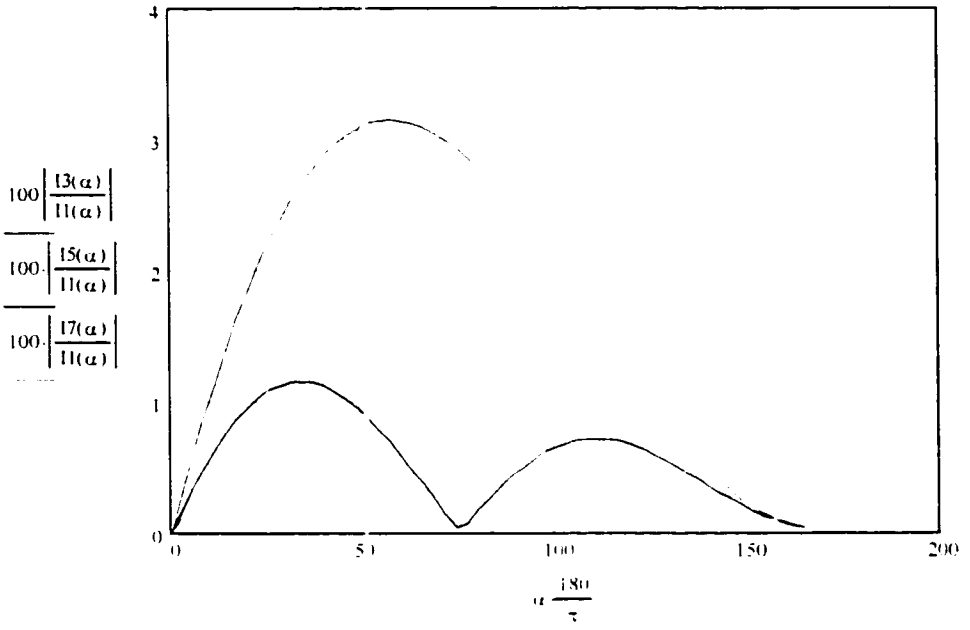


$$V_{O1}\left(144 \cdot \frac{\pi}{180}\right) = 1.68$$

To find Out THD:

$$I1(\alpha) := \sqrt{A1(\alpha)^2 + B1(\alpha)^2} \qquad I3(\alpha) := \sqrt{\left(\frac{a1(\alpha,3)}{Z_{s1}(3)}\right)^2 + \left(\frac{b1(\alpha,3)}{Z_{s1}(3)}\right)^2}$$

$$I5(\alpha) := \sqrt{\left(\frac{a1(\alpha,5)}{Z_{s1}(5)}\right)^2 + \left(\frac{b1(\alpha,5)}{Z_{s1}(5)}\right)^2} \qquad I7(\alpha) := \sqrt{\left(\frac{a1(\alpha,7)}{Z_{s1}(7)}\right)^2 + \left(\frac{b1(\alpha,7)}{Z_{s1}(7)}\right)^2}$$



$$100\left|\frac{I3\left(144\frac{\pi}{180}\right)}{I1\left(144\frac{\pi}{180}\right)}\right| = 0.354$$

$$100\left|\frac{I5\left(144\frac{\pi}{180}\right)}{I1\left(144\frac{\pi}{180}\right)}\right| = 0.282 \qquad 100\left|\frac{I7\left(144\frac{\pi}{180}\right)}{I1\left(144\frac{\pi}{180}\right)}\right| = 0.213$$

APPENDIX 3

Mathematical Analyses carried out in MathCAD for Chapter 4

Defining Some Constant Values:

$C_O := 500 \cdot 10^{-6}$ $V_O := 1.6$ $R_L := 0.032$ $D := 0.$

$j := \sqrt{-1}$ $K_C := 40 \cdot 10^{5}$ $\omega_Z := 360325$ $\omega_P := 4382286$

Defined Transfer Functions:

$$G_{PS}(s) := \frac{1 - 2 \cdot D}{1 - D} \cdot \frac{V_O}{s \cdot R_L \cdot C_O - 2 \cdot D + 1}$$ *Power Stage Transfer Function*

$$G_C(s) := \frac{K_C}{s} \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)}$$ *Controller Transfer Function*

$G_{OL}(s) := G_{PS}(s) \cdot G_C(s)$ *Open Loop Transfer Function*

$$G_{CL}(s) := \frac{G_{OL}(s)}{1 + G_{OL}(s)}$$ *Close Loop Transfer Function*

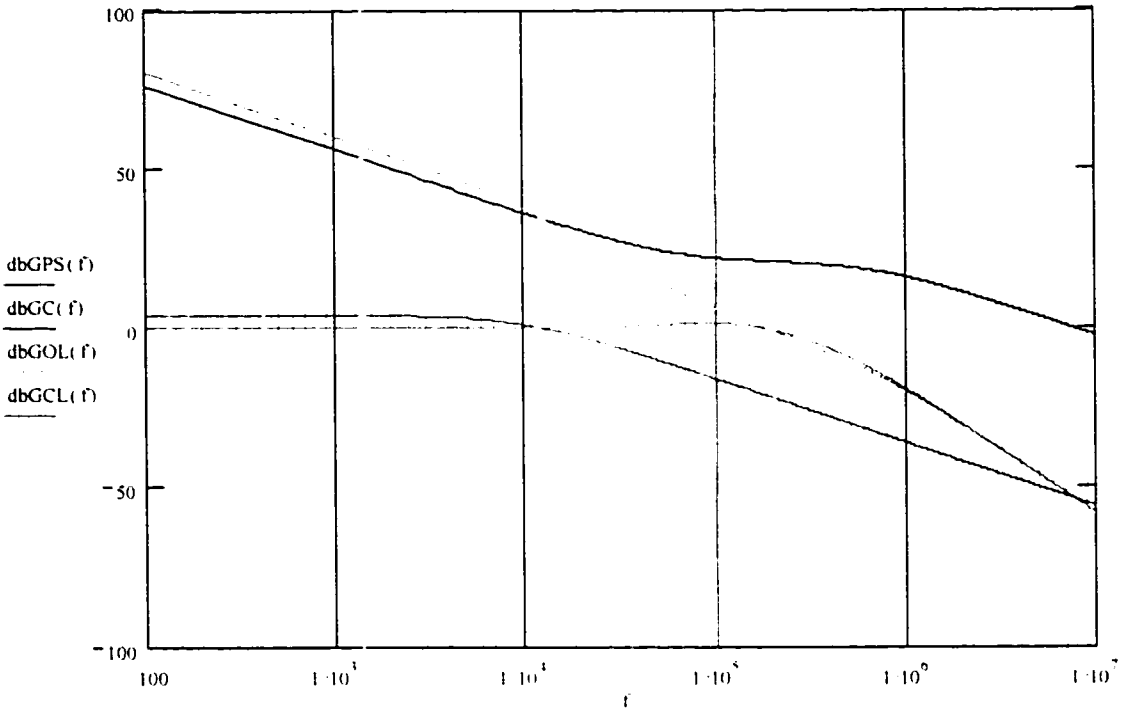
$f := 100, 500 .. 10000000$ $s(f) := 2 \cdot \pi \cdot f \cdot j$

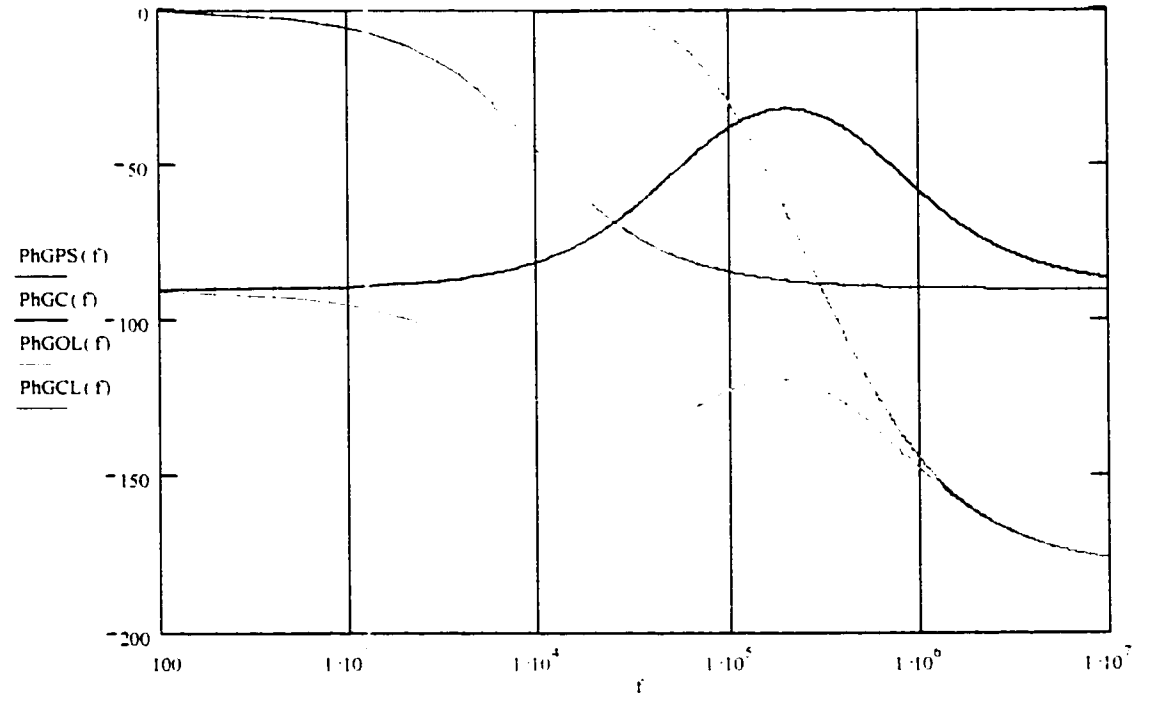
$dbGPS(f) := 20 \cdot \log(|G_{PS}(s(f))|)$ $PhGPS(f) := \frac{\arg(G_{PS}(s(f)))}{2 \cdot \pi} \cdot 360$

$dbGC(f) := 20 \cdot \log(|G_C(s(f))|)$ $PhGC(f) := \frac{\arg(G_C(s(f)))}{2 \cdot \pi} \cdot 360$

$dbGOL(f) := 20 \cdot \log(|G_{OL}(s(f))|)$ $PhGOL(f) := \frac{\arg(G_{OL}(s(f)))}{2 \cdot \pi} \cdot 360$

$dbGCL(f) := 20 \cdot \log(|G_{CL}(s(f))|)$ $PhGCL(f) := \frac{\arg(G_{CL}(s(f)))}{2 \cdot \pi} \cdot 360$


100
50
0
-50
-100
dbGPS(f)
dbGC(f)
dbGOL(f)
dbGCL(f)
100
1·10^3
1·10^4
1·10^5
1·10^6
1·10^7
f


0
-50
-100
-150
-200
PhGPS(f)
PhGC(f)
PhGOL(f)
PhGCL(f)
100
1·10
1·10^4
1·10^5
1·10^6
1·10^7
f