Fast Symbol Synchronization Algorithms for On-Board Processing Satellites

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ABSTRACT

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Satellite communications continue to undergo changes not only from advancing technology, but also from new service and regulatory activities. Therefore, advanced digital satellite communication systems using efficient on-board processing capabilities are required. Signal regeneration on-board the satellite makes it possible to use different multiple access schemes for the uplink and the downlink. The uplink and the downlink can be separately optimized for greater power efficiency and bandwidth utilization. A multiple access scheme using the frequency division multiple access (FDMA) for the uplink and time division multiplex (TDM) for the downlink has been considered for regenerative satellite communications. However, the feasibility of this approach depends on efficient means to directly interface the two multiple access formats on-board the satellite. The conversion from frequency to time division multiplex format requires the uplink signal to be demultiplexed and each individual carrier to be demodulated.

The main objective of this thesis is to present the existing symbol timing recovery structures, analyze them and prove the feasibility of the proposed technique which is less complex and that has fast-acquisition characteristics than the conventional techniques. Firstly, feed-forward symbol timing recovery technique based on the

spectral line estimation is presented, which requires relatively high over-sampling ratio and requires considerable amount of hardware resources for implementation. Secondly, feedback timing estimators are analyzed. These techniques have less complex structures compared to feed-forward structures but require more acquisition time. Feedback structures are well suited for continuous mode communications. Finally, a new algorithm for symbol timing recovery is presented in this thesis, which is based on decision-directed approach. The proposed algorithm has fast acquisition time, it has been shown through computer simulations that it is three times faster than the conventional feedback technique. In terms of VLSI implementation, the proposed symbol timing recovery circuit requires 3 adders for QPSK modulation format, where as Gardner's timing error detector needs 3 adders and 2 multipliers.

Dedicated to my uncle, Late Shri Tarachand Narsinghani.

ACKNOWLEDGEMENTS

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Last but not the least, I would like to thank Leena for her patience and support.

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LIST OF ABBREVIATIONS AND SYMBOLS

AAF	Anti-Aliasing Filter
ADC	Analog to Digital Converter
ARC	Adaptive Rate Conversion
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CR	Carrier Recovery
CRB	Cramer Rao Bound
DA	Data Aided
DAC	Digital to Analog Converter
DD	Decision Directed
DFT	Discrete Fourier Transform
DSP	Digital Signal Processing
FB	Feedback
FDM	Frequency Division Multiplex
FDMA	Frequency Division Multiple Access
FF	Feedforward
FFT	Fast Fourier Transform

FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HPA	High Power Amplifier
IIR	Infinite Impulse Response
IL	Implementation Loss
ISI	Inter Symbol Interference
LPF	Low Pass Filter
LUT	Look-Up Table
M&M	Mueller and Muller
MAP	Maximum A Posteriori Probability
MCD	Multicarrier Demodulation
ML	Maximum Likelihood
MLE	Maximum Likelihood Estimation
NCO	Numerical Controlled Oscillator
NDA	Non-Data Aided
OBP	On-Board Processing
PAM	Pulse Amplitude Modulation
PDF	Probability Density Function
Pe	Probability of BER
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
ROM	Read Only Memory
RRC	Root Raised Cosine

SCPC	Single Channel Per Carrier
SNR	Signal to Noise Ratio
SRRC	Square Root Raised Cosine
STR	Symbol Timing Recovery
TDM	Time Division Multiplex
TDMA	Time Division Multiple Access
TED	Timing Error Detector
TRC	Timing Recovery Circuit
TWTA	Traveling Wave Tube Amplifier
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration

Chapter 1

Introduction

1.1 Background

In this thesis various schemes for estimating the timing offset of a group demodulator, a representative subsystem which simultaneously demultiplexes 8 QPSK channels, each with a complex data rate of 0.772 M-samples per second is considered. Also, a technique which corrects the timing offset using an Adaptive Rate Conversion (ARC) filter is presented.

In an on-board processing (OBP) system, frequency-division multiple access using single channel per carrier (SCPC-FDMA) on the uplink and time-division multiplex (TDM) on the downlink is assumed. With SCPC-FDMA, each earth station in the satellite network transmits a radio frequency (RF) carrier to the satellite transponder. Each uplink carrier occupies a specific frequency band location within the uplink bandwidth. In addition, the data rate is typically constant, for all channels, so that each station has the same bandwidth and the network is uniform. With TDMA systems, each station transmits one data frame at a time which is globally synchronized in time to avoid collision. For both FDMA and TDMA the uplink signal is amplified by the satellite's traveling wave tube amplifier (TWTA) and retransmitted in the downlink beam. As compared to the TDMA method,

the SCPC-FDMA method on the uplink reduces the cost and complexity of the earth terminals considerably, because global synchronization is not needed. However, amplification of the multiple carriers by the TWTA operated at saturation on the downlink produces inter-modulation distortion, which significantly degrades individual channel performance. On the other hand, with TDMA since there is only one carrier at a time, the inter-modulation distortion is eliminated [1].

The SCPC-FDMA/TDM link combines the advantages of SCPC-FDMA on the uplink and benefits of a TDMA on the downlink. Thus, this method reduces the cost and complexity of the earth stations and allows the satellite amplifier to operate at saturation for maximum efficiency. It enables high power amplifier (HPA) power and antenna size at the terminal to be reduced [2]. Also, splitting of the satellite link into two distinct sections prevents noise and other interference to be accumulated and transferred from the uplink to the downlink, which improves performance.

The above discussions indicate the benefit of using FDMA on the uplink and TDMA on the downlink in a satellite communications system. The FDMA/TDMA configuration necessitates on-board signal regeneration in which the FDMA uplinks are frequency demultiplexed and then the individual carriers demodulated, routed and recombined into TDM signals for retransmission.

The digital signal processing (DSP) operation that simultaneously downconverts multiple FDM signals to baseband is referred to as a multicarrier demodulation and the device which accomplishes this is called a multicarrier demodulator (MCD). Multicarrier demodulation includes frequency demultiplexing of the FDM carriers and subsequent demodulation of each carrier to recover the individual channel data. Figure 1.1 depicts the block diagram for a group demodulator. It consists of two main blocks: a digital group demultiplexer and a bank of channel processors. The digital group demultiplexer separates out the individual channels in the received signal. The function of the channel processors is to regenerate each signal by performing timing and carrier recovery and making decisions on the QPSK signals.

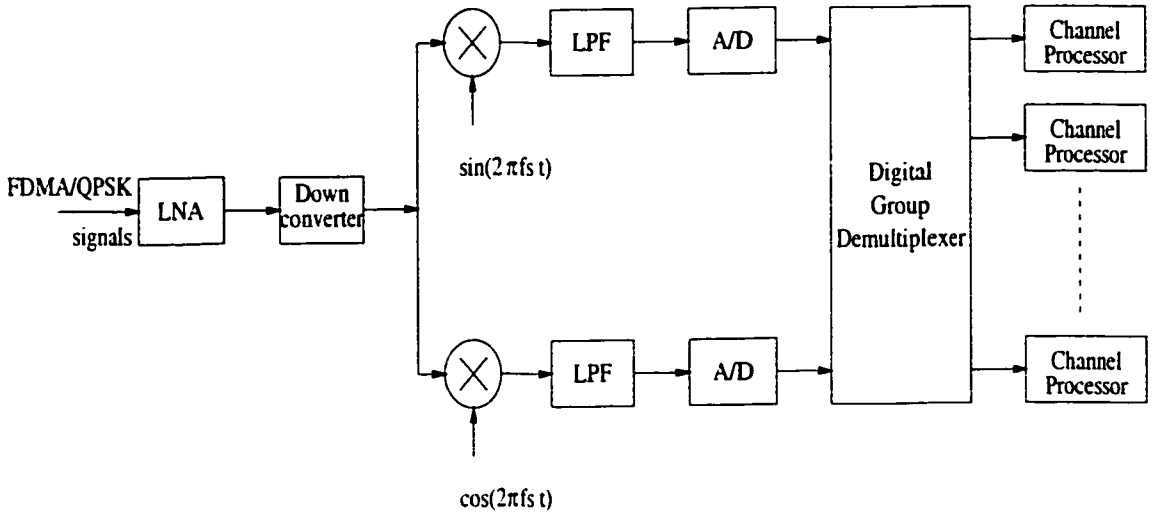

Figure 1.1: **Block diagram of group demodulator**

Several approaches to demodulation (carrier and timing recovery) have been proposed. In this thesis various techniques for estimating the timing offset have been considered. The one most suitable for on-board processing has been studied and further improvement has been proposed to reduce the acquisition time.

1.2 Contribution of Thesis

The main objective of this thesis is to propose new techniques for symbol timing recovery in on-board processing satellites. The key feature of the work is the development of symbol timing recovery methods which provide fast acquisition and considerable amount of jitter for continuous mode based communications systems. The major contributions of this thesis include the following:

- A review of the literature on symbol timing recovery is performed to highlight current areas of interest, namely symbol timing estimation algorithms for continuous mode communication systems.

- Performance evaluation of few timing estimation algorithms. Non-Data Aided - Feed-forward and Non-Decision Directed - Feedback estimators are two schemes

which have been simulated and performance evaluated using computer simulations.

- Proposed two new techniques for symbol timing recovery, which are based on Decision-Directed feedback approach.
- Evaluated the performance of the proposed technique using computer simulations and compared the performance to the existing schemes.
- A new study is made to replace the interpolating filter with matched filter on the receiver side, which reduces the hardware cost of the system.
- Made a comparison of various techniques for symbol timing recovery in feedback configuration in terms of performance and hardware cost.
- Finally, hardware structures are proposed for the implementation of the new algorithms and estimators.

1.3 Organization of Thesis

This thesis is organized in the following manner. Chapter 2 provides an overview of clock synchronization issues in satellite receivers. The effect of imperfect timing recovery on the system performance is presented. Various schemes for estimating and correcting timing offset are surveyed. Non-data aided feed-forward estimator for symbol synchronization is presented in chapter 3. Its performance is also evaluated. In chapter 4, feedback timing recovery circuits are presented. Chapter 5 gives the description of proposed symbol synchronization algorithms. Performance of the proposed scheme in terms of acquisition time, tracking (variance of estimate), bit error rate (BER) etc. are presented. Chapter 6 summarizes the thesis and provides recommendations for further research in this area.

Chapter 2

Clock Synchronization Issues in Satellite Digital Receivers

2.1 Introduction

Satellite communications continue to undergo changes not only from advancing technology, but also from new service and regulatory activities. Therefore, advanced digital satellite communication systems using efficient modulation techniques and satellites with on-board signal processing capabilities are required. In particular, the on-board signal processing offers several advantages to satellite communication systems; an interesting feature is the separation of the uplinks and downlinks which permits their distinct and independent optimization. For mobile communication services, the use of uplink FDMA techniques with the inherent low-cost earth stations, and downlink TDMA techniques that can fully exploit the satellite transponder output power without inter-modulation, is a very interesting and attractive solution. The feasibility of this approach, however, depends on an efficient means of translating between the two formats on board the satellite. The complexity of the on-board system (including the VLSI design) and power consumption are obviously of primary concern. The on-board processing system receives an input FDMA signal and

supplies an output TDM signal; therefore it must be able to separate each radio channel, perform demodulation and correctly switch to the appropriate downlink channel. In this work, the concentration is on demodulation process with emphasis on clock synchronization circuit.

In this chapter, four major topics will be described. In Section 2.2, the importance and need for symbol synchronization will be discussed. Section 2.3 will the deal with effect of timing offset on the probability of error (Pe). It will be shown how the timing offset degrades the bit error rate. Also the effect of various parameters on the system performance will be presented. Section 2.4 deals with various symbol timing estimators which include both feed-forward and feedback estimators. In Section 2.5, various techniques for timing estimation/correction will be explained. This section addresses both types of receivers: synchronous and non-synchronous sampling receivers. In Section 2.6, a comparison is made between Non-Data Aided and Decision Directed schemes.

2.2 Importance and need for Synchronization

Synchronization is a critical function in Digital Communications; its failures may have catastrophic effects on the transmission system performance. In digital communications there is a hierarchy of synchronization problems to be considered. First, assuming a carrier-type system is involved, there is the problem of carrier synchronization which concerns the generation of a reference carrier with a phase closely matching that of the data signal. This reference carrier is used at the data receiver to perform a coherent demodulation operation, creating a baseband signal. Next comes the problem of synchronizing a receiver clock with the baseband data-symbol sequence. This is commonly called symbol synchronization [4].

In synchronous digital transmissions the information is conveyed by uniformly

spaced pulses and the received signal is completely known except for the data symbols and a group of variables referred to as reference parameters. Although the ultimate task of the receiver is to produce an accurate replica of the symbol sequence with no regard to reference parameters, it is only by exploiting knowledge of the latter that the detection process can properly be performed. In a baseband Pulse Amplitude Modulation (PAM) system the received waveform is first passed through a matched filter and then is sampled at the symbol rate. The optimum sampling times correspond to the maximum eye opening and are located at the "peaks" of the signal pulses. Clearly, the locations of the pulse peak must be accurately determined for reliable detection. A circuit that is able to predict such locations is called a timing synchronizer and is a vital part of any synchronous receiver [5].

Coherent demodulation is used with passband digital communications when optimum error performance is of paramount importance. This means the baseband data signal is derived making use of a local reference with same frequency and phase as the incoming carrier. This requires accurate frequency and phase measurements as phase errors introduce crosstalk between the in-phase and quadrature phase channels of the receiver and degrades the detection process. Such circuits are referred to as carrier synchronizers.

Carrier phase information is not always needed. In applications where simplicity and robustness of implementation are of more importance than achieving optimum performance, differential demodulation is an alternative to coherent detection. Differential demodulation of PSK signals is accomplished by the difference between the signal phases at two consecutive sampling times and making a decision on this difference.

From the above discussion it is evident that measuring reference parameters is a vital function in satellite communication systems. This function is called synchronization.

2.2.1 Importance of Timing Estimation

Symbol Timing Recovery (STR) is a very important process in demodulation. Various options exists for the architecture of the STR process. The sampling process may take place using a feedback (FB) scheme where the signal is sampled after the matched filter. Alternatively, it may be sampled prior to, or directly after the frequency translation process. Each option has its own particular merits. Also, a feed-forward (FF) STR method could be used. This range of optional structures is discussed below. After the sample (symbol) timing has been established, phase and frequency correction is made. Again, a range of structures exists for implementation including both FF and FB schemes. If a feed-forward Carrier Recovery (CR) scheme is used, such as that described by Viterbi and Viterbi [6], then symbol timing must be established prior to the CR function. Consequently the STR process must operate on samples which have unknown carrier phase and frequency offset. In this situation the STR scheme chosen must be phase independent. Alternatively, a feedback CR scheme may be employed. If phase lock is achieved prior to the STR function a phase dependent STR scheme may be employed. The final process is that of data detection, where the received, matched filtered, and synchronized signal samples are produced to determine the values of the transmitted data symbols.

Without the STR function the phase and frequency at which the signal is sampled will generally be different to that optimum sampling. This situation will incur more symbol decision errors and potentially lost symbols due to cycle slipping. The task of the STR function is to sample the signal at or near the optimum location for all received symbols. This will ensure that the samples passed to the demodulation processes, including data detection, have the maximum available Signal to Noise Ratio (SNR) and hence a Bit Error Rate (BER) as close as possible to optimum. The increase in SNR above the minimum required to obtain a particular BER, is known as Implementation loss (IL). Considering that modern receivers are generally

required to have an implementation loss less than 1dB, the implementation associated with the symbol timing recovery function is often required to be less than 0.1dB.

2.2.2 Overview of existing schemes and strategies

Digital transmission of a signal can be classified into two basic categories; continuous-time and burst-mode transmission. A continuous time signal may be defined as one in which the signal is continuously transmitted/received i.e., the communication link operates from days to years without interruption. In contrast, burst mode signals are used in schemes designed to use short packets of information. Packet size may range from very short(for e.g., 32 or 64 symbols) to very large(for e.g., several thousands symbols). Typically, burst mode signals are used in TDMA and slow frequency hopping communications systems.

The information (i.e., signal) is transmitted in discrete form. The information coded using binary representation offers many advantages, such as higher bandwidth efficiency. Initially, timing synchronization information was transmitted on a separate channel. Golomb et al [7], in 1963 presented research work showing that optimum efficiency(that is the highest data throughput per used bandwidth) could be attained if all the transmitted energy was denoted to the transmission of the data signals, instead of splitting it between a data and a synchronization channel.

First symbol timing recovery methods extracted timing information from a discrete frequency component at the symbol rate using feed-forward structures. The frequency component is generally produced by feeding the baseband signal through a non-linearity and then filtering the unwanted frequency components using a bandpass filter (BPF) [8]. The output of the bandpass filter is a discrete component, corresponding to a sine wave, at a symbol rate. As the received signal is usually corrupted by the Additive White Gaussian Noise (AWGN), the use of the non-linearity introduces additional noise term due to the interaction of the signal with itself, and

with the input noise. Some constant fractional symbol delay is usually required after zero crossing edge to ensure that it is aligned with the symbol center. The delay is necessary because the previous processing functions introduce a delay which is not usually a multiple of the symbol period. The performance of such systems is highly dependent on the input SNR as the non-linearity produces unwanted signal components which increase the jitter of the timing estimate significantly at low SNRs. Additionally, this method has until recently been confined to analog implementation and hence has problems due to drift in the analog components in filtering, amplification and limiting stages.

In feedback systems, the received signal is processed by a timing phase detector which determines whether the current sample timing phase is advanced or retarded with respect to the symbol center. The output of the timing phase detector, that is the timing error, is then filtered to reduce the variance of the timing error. The filter usually incorporates an integrator which is used in the loop-back mode. The output of the loop-filter controls the frequency and phase of the sampling oscillator which is usually a Voltage Controlled Oscillator (VCO) or Numerically Controlled Oscillator (NCO) [4, 9, 10].

Earlier feedback symbol timing recovery loops were constructed using analog techniques with the familiar loop filter and VCOs. With the introduction of digital semiconductor devices, and the matured digital phase locked loop techniques, these methods are now implemented in a range of forms including hybrid analog/digital or fully digital hardware. Considering the disadvantages of analog implementations, and the increasing power of Digital Signal Processing (DSP) technologies, both feed-forward and feedback methods are increasingly being implemented in fully digital forms.

Synchronization techniques are generally modeled using Maximum Likelihood Estimation (MLE) and Maximum A Posteriori Probability (MAP) [10] models. Techniques for analysis of the performance of STR schemes continued to advance

through the seventies. Many new techniques were published by Franks and Bubrouski [8] and by Mueller and Muller [9]. A good tutorial paper on Carrier and Bit synchronization was presented by Franks [4] in the special issue of IEEE transactions on communications on synchronization (1980).

The 80's saw a dawn of relatively powerful DSP integrated circuits, that allowed the implementation of systems completely digital. Gardner [11] proposed a new timing error detector for sampled data receivers. A technique for digitally implemented data receivers was proposed by Farhang-Boroujeny [12] in 1990. Lee et al [13], proposed a new STR algorithm based on the spectral line method and has better performance in narrowband.

Continuous signal based systems generally tend to use feedback STR methods. This is due to the tracking ability of the timing phase locked loop structure. Feed-forward methods can also be used for STR in continuous systems, however, generally these schemes do not have the tracking ability of feedback methods and have higher jitter when the SNR is poor.

STR schemes using the feed-forward methodology have also been investigated. Basically the techniques available for feed-forward configuration are used for burst-mode transmission. The use of a burst mode transmission scheme increases the complexity of the demodulator relative to continuous mode systems. Such as, the accuracy of timing estimate depends on the burst length (i.e., number of symbols). There is a design constraint on the burst length, which limits the performance of the system. Shorter packets have high jitter, which results in increased BER. Burst-mode systems require fast acquisition so that the preamble length is reduced and hence maximize the user data throughput. Guard times are required at the beginning and at the end of the packet transmission to avoid packets overlapping with adjacent time slots.

The packets are generally constructed with a preamble of defined data. The preamble allows the STR scheme to ensure that the timing phase errors does not

exceed a predefined value with a specific probability. The use of preambles has two major disadvantages, namely: it reduces the available throughput of the system by introducing overheads and a trade-off is required between the acquisition time and steady state performance of the symbol timing and carrier phase.

Various techniques for estimating the timing phase in the burst-mode demodulators have been addressed in the past two decades. Meyr and Oerder [19] presented a technique for estimating the timing phase based on the FFT. It is the digital counterpart of the well-known continuous-time filter and square time recovery [8]. Thus keeping in mind the excessive computation power required by the STR structures in the feed-forward mode. Also the signal transmission has FDMA structure, techniques using feedback structure were preferred. This thesis proposed a number of new methods and solutions for continuous mode timing recovery and determines their performance through computer simulations and is shown that the proposed technique has better performance when compared to existing techniques.

2.3 The Effect of Timing Offset on System Performance

In this section, the effect of timing offset on the system performance is presented. Filtering is an importance aspect in digital transmission, the reason for selecting transmitter and receiver filter is given. And also the effect of Matched filtering is explained. In the next subsection, various parameters effecting the probability of BER are explained.

2.3.1 Effects of Filtering in Digital Transmission

Filtering is an integral part of both, modulating and demodulating function. The obvious purpose of the transmit filter is to limit energy outside of a chosen bandwidth,

hence allowing the signal to be channelized and to provide a means of controlling the bandwidth efficiency. The purpose of the receive filter is to stop unwanted energy, both from adjacent channels and out of band noise, from entering the receiver.

The combination of the transmit and receive filter plays an important role in determining system performance, in terms of bit error rate, by affecting the received signal to noise ratio and the level of Inter-Symbol Interference (ISI).

It is well known [14, 15] that the matched filter receiver is the optimum solution for maximizing the received signal to noise ratio. The received filter is named matched filter, the reason being it is a time reversal and delayed version of the received pulse waveform.

The excess bandwidth factor (i.e., alpha) can be between 0 and 1, but commonly this will be 0.3 to 0.5 for 30% to 50% excess bandwidth. A class of filter called raised cosine filter is discussed in the following section.

2.3.1.1 Raised Cosine Pulse Shaping

In order to obtain the level of performance for the matched filter demodulation, the ISI must be zero. Raised cosine pulses belong to such category [14, 16]. They contribute zero energy at symbol spaced sampling instants outside their own symbol epoch. These class of pulses satisfy the Nyquist pulse shaping criterion.

The frequency domain description of the Raised cosine family of pulses is given below:

$$H(f) = \begin{cases} Ts & for \quad 0 \leq |f| \leq \frac{1-\alpha}{2Ts} \\ \frac{Ts}{2}\left[1+\cos\left(\frac{\pi Ts}{\alpha}\left[|f|-\frac{1-\alpha}{2Ts}\right]\right)\right] & for \quad \frac{1-\alpha}{2Ts} \leq |f| \leq \frac{1+\alpha}{2Ts} \\ 0 & for \quad \frac{1+\alpha}{2Ts} \leq |f| \end{cases} \tag{2.1}$$

where $0 \leq \alpha \leq 1$ is the *roll-off factor* or *excess-bandwidth factor* which shapes the spectrum as illustrated in Figure 2.1. Note that *H(f)* is strictly band-limited.

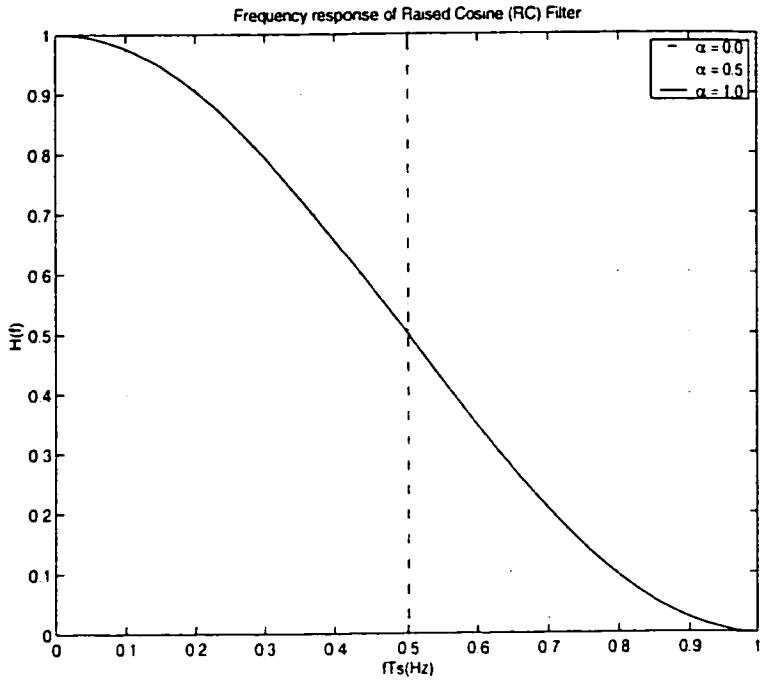

Figure 2.1: **Raised Cosine Filter Frequency Response**

This, of course, implies that the impulse response $h(t)$ is not time limited and extends to $t = \infty$. The impulse response is given by,

$$h(t) = \frac{\left[\frac{\sin\left(\pi \frac{t}{T_s}\right)}{\pi \frac{t}{T_s}}\right] \cos\left(\frac{\pi \alpha t}{T_s}\right)}{1 - \left(2\alpha \frac{t}{T_s}\right)^2} \tag{2.2}$$

It should be noted that these pulses are non-causal i.e.,

$$h(t) \neq 0; t < 0$$

and is plotted in Figure 2.2. Note that the impulse response is exactly zero for integer multiples of T_s. Thus, when $h(t)$ is used as a pulse shape for signaling at a rate $1/T_s$ symbols/sec, intersymbol interference is not a problem. The RC pulse belongs to a general class of signals which satisfy the Nyquist Criterion for no ISI.

The choice of small α corresponds to highest bandwidth efficiency, but makes the filtering function difficult to implement as the pulses decay slowly in time from

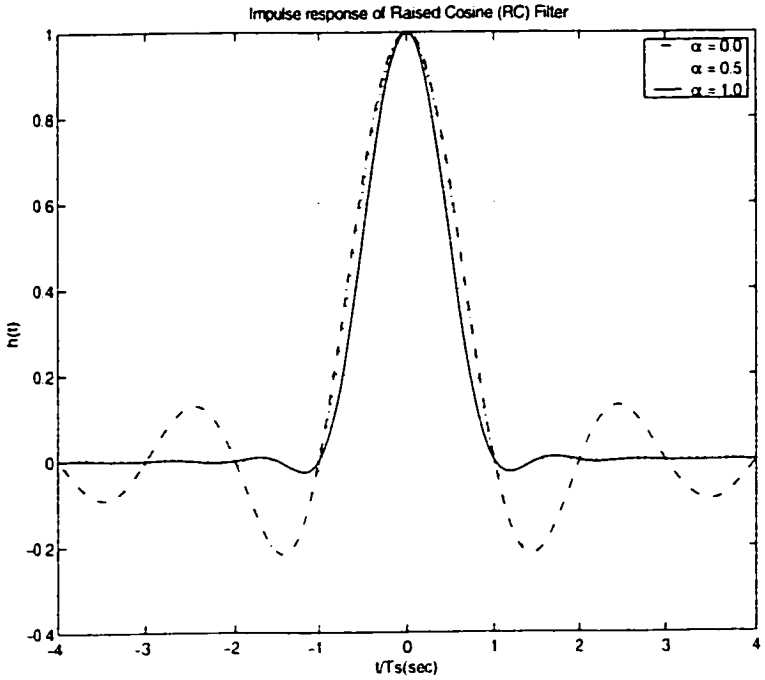

Figure 2.2: **Raised Cosine Filter Impulse Response**

the symbol center, as it is evident from Figure 2.2. It also proves that symbol synchronization is aided by larger value of excess bandwidth factor (this is proved in later chapters). In practise, an α of 0.3 to 0.4 is used for satellite transmission as a compromise between implementation complexity, bandwidth efficiency and synchronization performance.

2.3.1.2 Root Raised Cosine Pulse Shaping

In most communications applications, the RC pulse shape is divided into two parts, one for the transmitter and the other for the receiver. In this case, each side has what is called a *Square Root Raised Cosine Filter* forming a matched filter pair. The frequency response of this filter is the square root of Equation 2.1, while the impulse response is given by

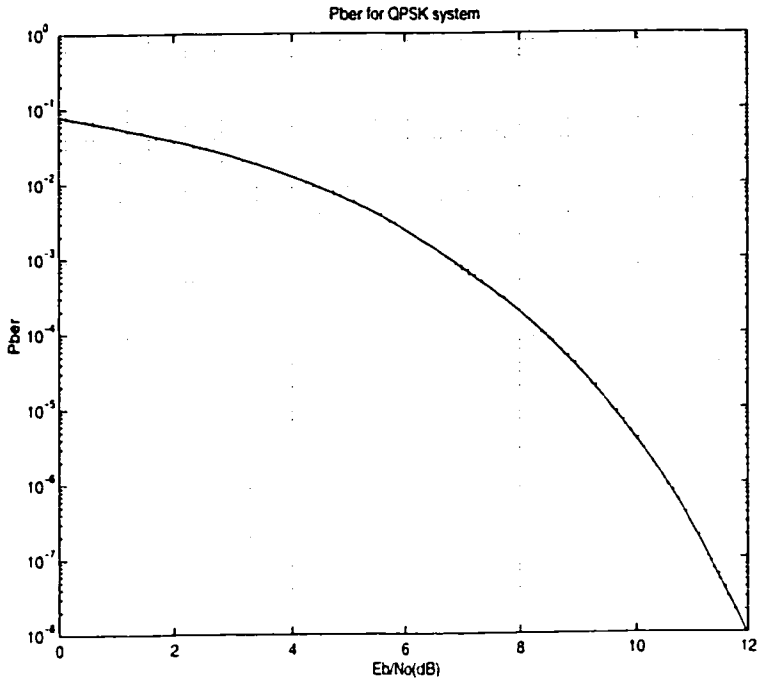

Figure 2.3: **Probability of Bit Error for QPSK System**

$$h(t) = \frac{4\alpha}{\pi\sqrt{T_s}} \frac{\cos\left((1+\alpha)\,\pi\frac{t}{T_s}\right) + \frac{\sin\left((1-\alpha)\pi\frac{t}{T_s}\right)}{4\alpha\frac{t}{T_s}}}{1-\left(4\alpha\frac{t}{T_s}\right)^2} \tag{2.3}$$

2.3.2 Probability of Error

Bit error rate is a measure of number of bits in error over a certain number of transmitted bits at a particular SNR. A typical BER for QPSK modulated system is shown in Figure 2.3.

The probability of bit error of the coherent QPSK receiver [15] is,

$$P_{E,QPSK} = \frac{1}{2} erfc\left(\sqrt{\frac{E_b}{N_o}}\right)$$

where $erfc(y) = \frac{2}{\sqrt{\pi}} \int_y^\infty \exp\left(-z^2\right) dz \qquad for\ y > 0$

Figure 2.3 illustrates the theoretical limit on BER presuming a perfect synchronization. Synchronization mismatch causes this curve to deviate from its theoretical

limit, as will be illustrated.

The fundamental feature of a *practical* Timing Recovery Circuit (TRC) is that the separation between adjacent pulses is not exactly constant but varies slowly in a random manner. The variations are referred to as *timing jitter* and are a consequence of the random nature of the waveform at the TRC input. The average error probability is obtained by averaging $P(e \mid \widehat{\tau})$ over $\widehat{\tau}$.

$$P(e) = \int_{-\infty}^{\infty} P(e \mid \widehat{\tau}) p(\widehat{\tau}) d\widehat{\tau} \tag{2.4}$$

where $P(e \mid \widehat{\tau})$ is the detector error probability on a fixed sampling epoch $\widehat{\tau}$.

The derivation of the probability of error, Pe, of an optimum demodulator is generally derived assuming perfect STR (and CR).

The effect of static timing offset on the probability of error is shown in Figures 2.4 to 2.6 for a range of signal bandwidths. Figure 2.5 shows that for a channel roll-off factor, α, of 0.4 and a BER of 10e-4, timing offsets of 5% and 10% will result in implementation losses of 0.33 and 0.80 dB respectively. A value of 0.4 is used for α throughout this thesis as it provides a good trade off between matched filter implementation complexity and channel bandwidth and as such is commonly used. Where the channel bandwidth has distinct effects, results are given for a range of values of α.

Figure 2.7 may be used to determine the standard deviation required to obtain a specified implementation loss at a nominal value of signal to noise ratio. However, if the signal to noise ratio varies, so will the timing estimate variance, and hence the implementation loss will also change. Consequently this method is only useful for constant SNRs. If a variable SNR is likely, or the effect of the timing offset variance is required over a range of SNRs, the effect of the SNR on the timing estimate variance can be taken into account. Effectively, this requires making the timing estimate *pdf* dependent on the SNR.

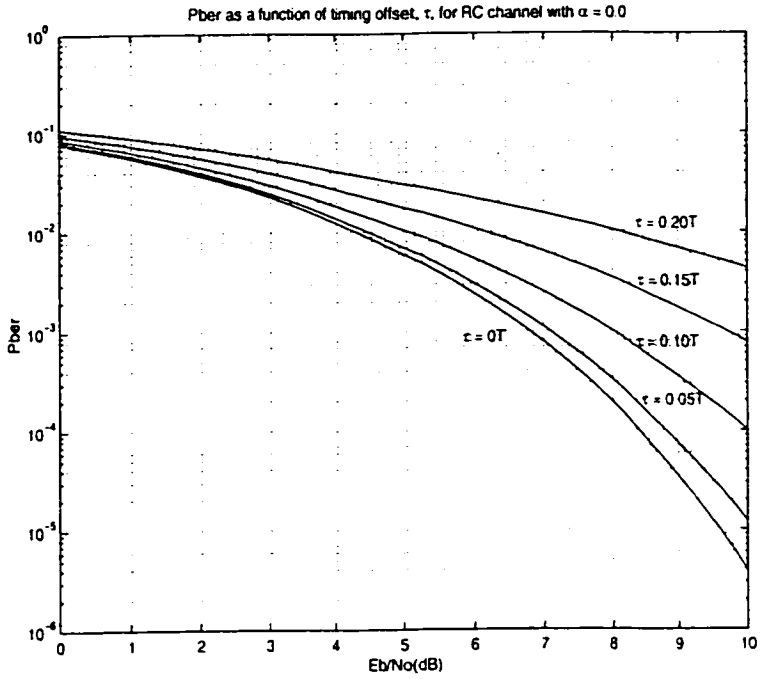

Figure 2.4: **BER as a function of timing offset, τ, for RC channel with α = 0**

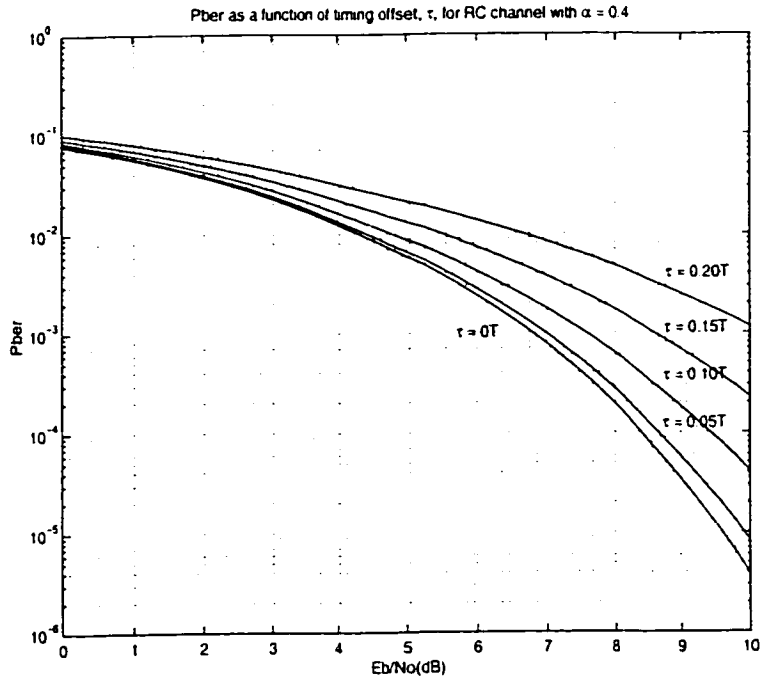

Figure 2.5: **BER as a function of timing offset, τ, for RC channel with α = 0.4**

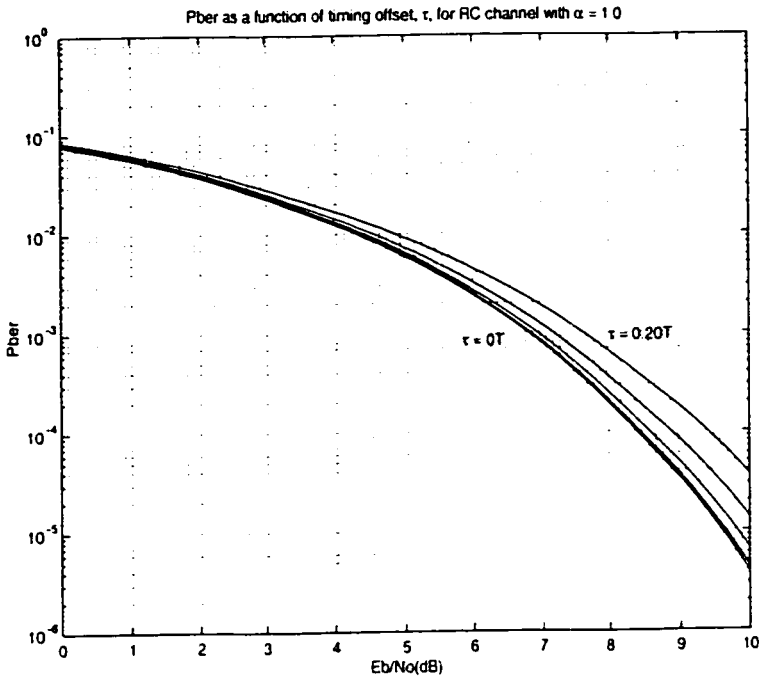

Figure 2.6: **BER as a function of timing offset, τ, for RC channel with α = 1.0**

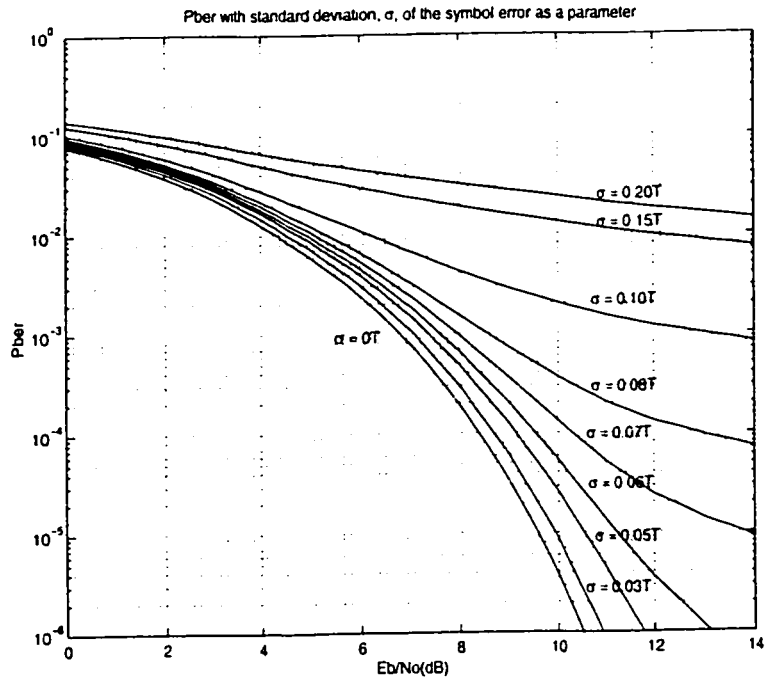

Figure 2.7: **BER as a function of standard deviation of timing offset as parameter**

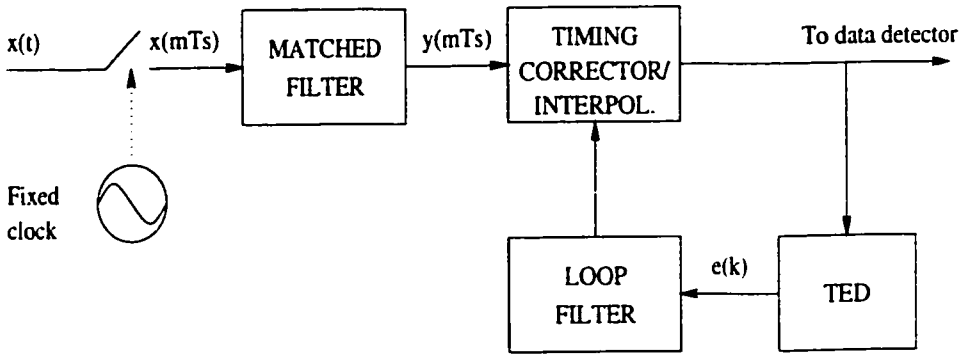

Figure 2.8: **Feedback Configuration**

An interesting feature of the upper curves in Figures 2.4-2.7 is that they exhibit an irreducible error as E_b/N_o increases. The explanation is that timing errors generate intersymbol interference (ISI) which, in turn, produce decision errors even in the absence of noise [5].

2.4 Symbol Timing Estimators

Timing recovery basically consists of two distinct operations: (1) Estimation of the timing phase and (2) Application of the estimate to the sampling process. The former is referred to as timing measurement and the latter as timing correction (or adjustment). Timing correction serves to provide the decision with signal samples with minimum inter symbol interference [5].

Four types of algorithms exists for timing estimation and correction. They are:

- Feedback (FB) or Feed-forward (FF) structures,
  - FB : correction before the detection of the error parameter.
  - FF : correction after the estimation of the error parameter.
- Decision directed (DD) or Non-Data Aided (NDA) structures,

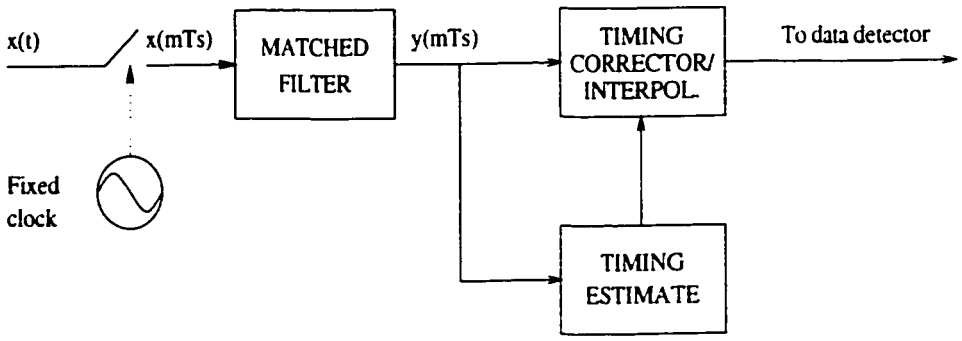

Figure 2.9: **Feed-forward Configuration**

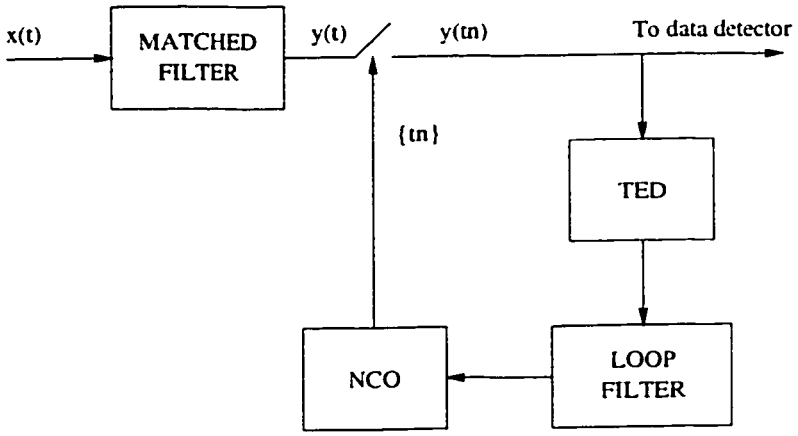

Figure 2.10: **Synchronous Sampling**

- DD : use of data decisions to perform the detection.
- NDA : no use of data decisions to perform the detection.

In full digital implementation, the receiver clock is not synchronized to the transmitter clock. Figure 2.8 and 2.9 illustrate the feedback and feed-forward schemes.

In feedback configuration, the timing corrector feeds a timing error detector (TED), whose purpose is to generate an error signal *e(k)* proportional to the difference between timing phase and it's estimate. The error signal is then used to recursively update the timing estimates. Feed-forward timing recovery configuration is shown in Figure 2.9.

The next prominent issue in synchronization is synchronized and non-synchronized sampling. In a fully digital implementation, sampling is not locked to the incoming

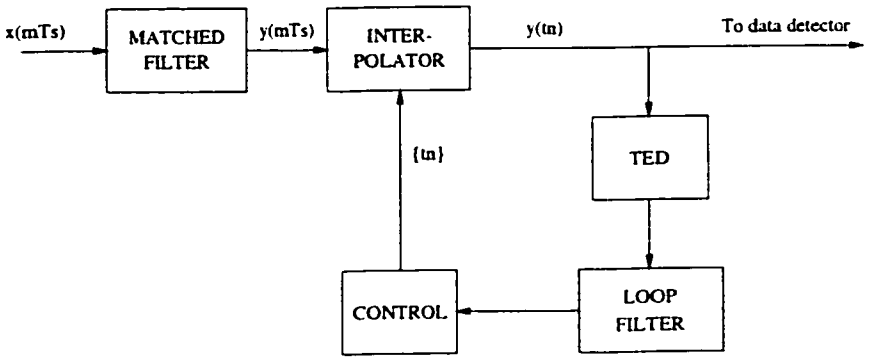

Figure 2.11: **Non-synchronous Sampling**

pulses. This is referred to as a non-synchronous sampling (Figure 2.11). On the other hand, sampling can be made synchronous by exploiting some error signal to adjust the timing phase of a numerically controlled oscillator (NCO) as shown in Figure 2.10.

2.4.1 Feed-Forward Estimators

In this section various methods of estimating the symbol timing using a feed-forward approach are discussed. Traditionally, feed-forward methods have been based on non-linearity and filter schemes which extract the phase of a discrete frequency component, generated by the non-linearity at the symbol rate. The timing estimate obtained is thus used to correct the timing offset. This is done using the interpolation technique, which is addressed in Section 2.5.

In Section 2.4.1.1, a Non-Data Aided (NDA) Maximum Likelihood timing error estimator is explained. In the following Section (2.4.1.2), a scheme based on spectral line estimation is illustrated.

2.4.1.1 NDA-ML based Algorithm

Let the transmitted symbol sequence be $\{a_n\}$, n = 1, 2, ... In general, the a_n's are complex numbers depending on the modulation type used such as QPSK. Then the

transmitted baseband waveform will take the form

$$x(t) = \sum_{n=-\infty}^{\infty} a_n g(t - nT) \tag{2.5}$$

where T and $g(t)$ denote the symbol interval and the pulse shaping waveform, respectively. The received noisy signal can be written as

$$z(t) = x(t;\tau) + n(t) \tag{2.6}$$

where

$$x(t;\tau) = \sum_{n=-\infty}^{\infty} a_n g(t - nt - \tau) \tag{2.7}$$

and n(t) denotes the added white Gaussian noise with a double-sided spectral density of N_o W/Hz. And τ is the timing offset due to propagation delays and other channel distortions.

The Maximum Likelihood (ML) estimate of the timing parameter $\widehat{\tau}$ is obtained by maximizing the apriori likelihood function $L(\tau)$, given by

$$L(\tau) = p\left(z(t)/\widehat{\tau}\right) \quad , \quad z(t) \in T_o \tag{2.8}$$

where T_o is the time interval over which the received signal $z(t)$ is observed and is assumed to be much longer compared to the symbol interval T. The resulting likelihood function, with argument $\widehat{\tau}$ which can be regarded as a trial estimate of the parameter, is given by [8, 17, 18]

$$L(\tau) = \exp\left\{-\frac{1}{2N_o}\int_{T_o}\left[z(t) - x(t,\tau)\right]^2 dt\right\} \tag{2.9}$$

where N_o is used to denote the two-sided power spectral density of the noise (i.e., the variance of each of the quadrature Gaussian noise components with zero mean assumed).

The ML estimate is the value of τ which minimizes the integral in Equation 2.9. This integral expresses the signal space distance between the received signal, $z(t)$

and reference signal $x(t,\tau)$ defined on the interval T_o [8]. Expanding the binomial term in Equation 2.9, we see that

$$\Lambda(\widehat{\tau}) = \ln L(\widehat{\tau}) = \frac{1}{N_o}\int_{T_o} z(t)x(t,\widehat{\tau})dt + constant \tag{2.10}$$

since $z^2(t)$ is independent of $\widehat{\tau}$, and the $x^2(t,\widehat{\tau})$ term is simply the power of the transmitted signal and hence for signals with equal energy symbols its integral is $\widehat{\tau}$. Hence $z^2(t)$ and $x^2(t,\widehat{\tau})$ terms can be considered as constants independent of τ and consequently the most likely timing offset $\widehat{\tau}$ is the value which maximizes Equation 2.10, that is

$$\widehat{\tau} = \arg\max_{\widehat{\tau}} \{\Lambda(\widehat{\tau})\} = \arg\max \left\{ \frac{1}{N_o}\int_{T_o} z(t)x(t,\widehat{\tau})dt \right\} \tag{2.11}$$

Note that the constant term is not included in above equation, as it has no impact on the maximization process.

The dependence of the likelihood function (Equation 2.11) on the data symbol valued may be removed by averaging the likelihood function over the data values [8, 18]. This is referred to as the non-data aided approach. Consider Equation 2.9,

$$L(\tau) \propto \exp\left\{ -\frac{1}{2N_o}\int_{T_o} [z(t) - x(t,\tau)]^2\, dt \right\} \tag{2.12}$$

Since the integral of the $z^2(t)$ and $x^2(t,\widehat{\tau})$ terms is independent of $\widehat{\tau}$, as described previously. Equation 2.12 can be rewritten considering the cross correlation terms only,

$$L(\widehat{\tau}) \propto \exp\left[\frac{1}{N_o}\int_{T_o} z(t)x(t,\widehat{\tau})dt \right] \tag{2.13}$$

Substituting for $z(t)$ from Equations 2.6 and 2.7, this expression is simplified after the necessary complex algebra and discarding constant multiplication factor involving the received signal $z(t)$, is given by

$$L(\widehat{\tau}) \propto \exp\left[\frac{1}{N_o}\sum_{n=0}^{L-1} a_n q_n(\widehat{\tau}) \right] \tag{2.14}$$

$q_n(t)$ is the output of the receiver matched filter and is given by

$$q_n(t) = \int_{-\infty}^{\infty} z(t)g(t - nT - \tau)dt \tag{2.15}$$

and L denotes the number of symbols that span the observation time interval T_o.

Equation 2.14 may be written as the product of L factors where each factor depends only on the random variable a_n, namely;

$$L(\widehat{\tau}) \propto \prod_{n=0}^{L-1} \exp\left(\frac{1}{N_o} a_n q_n(\widehat{\tau})\right) \tag{2.16}$$

In the case of binary PAM, the data terms can have the values +A and -A. If the data values are equally probable then to average (Equation 2.16) over the data values, the sum of the exponential terms is taken with respect to the data values. [8, 15].

$$L(\widehat{\tau}) \propto \prod_{n=0}^{L-1} \left(\frac{1}{2}\exp\left(\frac{A}{N_o} q_n(\widehat{\tau})\right) + \frac{1}{2}\exp\left(\frac{-A}{N_o} q_n(\widehat{\tau})\right)\right) \tag{2.17}$$

Taking natural logarithms, Equation 2.17 is given by

$$\Lambda(\widehat{\tau}) \propto \sum_{n=0}^{L-1} \ln\cosh\left(\frac{A}{N_o} q_n(\widehat{\tau})\right) \tag{2.18}$$

As $\ln\cosh(x)$ function is complex to implement, it is often approximated to x^2 for small values of x and absolute value $|x|$ when the argument x is larger.

2.4.1.2 NDA-FFT (Oerder & Meyer) Algorithm

In the previous section (2.4.1.1), the unknown timing parameter is obtained by a maximum search. It is interesting to know that this maximum search could be circumvent. A commonly used *single shot* symbol timing estimator is the DFT estimator [19]. It is defined as

$$\widehat{\tau} = \frac{T_s}{2\pi} \arctan\left[\frac{\sum_{n=0}^{LK-1} x^2(nT_s - \tau)\sin\left(\frac{2\pi n}{K}\right)}{\sum_{n=0}^{LK-1} x^2(nT_s - \tau)\cos\left(\frac{2\pi n}{K}\right)}\right] \tag{2.19}$$

where *atan(.)* returns a value over $(-\pi, \pi)$. The signal samples are squared to eliminate data dependency and generate a discrete frequency component at the symbol rate. Atleast four samples per symbol are required to generate the discrete frequency component at the symbol rate [19]. The phase of the discrete frequency component at the symbol rate is a measure of the timing offset from optimum and hence an estimate of the timing offset may be obtained by taking the DFT, of the squared signal, at the symbol rate. This results in the estimator (Equation 2.19) which is known as DFT-NDA. Derivation of this estimator and performance will be illustrated in chapter 3.

The tone filtering algorithm is seen to provide excellent overall performance in the estimation of the symbol timing offset as long as the timing offset is within $\pm 45\%$ of the symbol time [18]. Its performance with this range and effectiveness in low signal to noise ratio is seen to be slightly better than the best of the ML-based algorithms. The ML-based techniques break after $\pm 25\%$ of the symbol time. The tone filtering approach would in fact work well even at lower signal to noise ratios due to the processing gain of the DFT, which is a correlation-type computation in which the noise is decorrelated.

2.4.2 Feedback Estimators

In the following sections, symbol timing recovery using feedback estimators is presented. Various techniques suitable for this configuration were studied and the one suitable from performance and implementation complexity point of view were chosen and analyzed.

In Section 2.4.2.1, the algorithm proposed by Mueller and Muller [9] is explained. Block diagram explaining its mode of operation is also presented. Second in the series is the timing error detector proposed by Floyd M. Gardner [11]. The one best suitable for this application is further investigated in chapter 5.

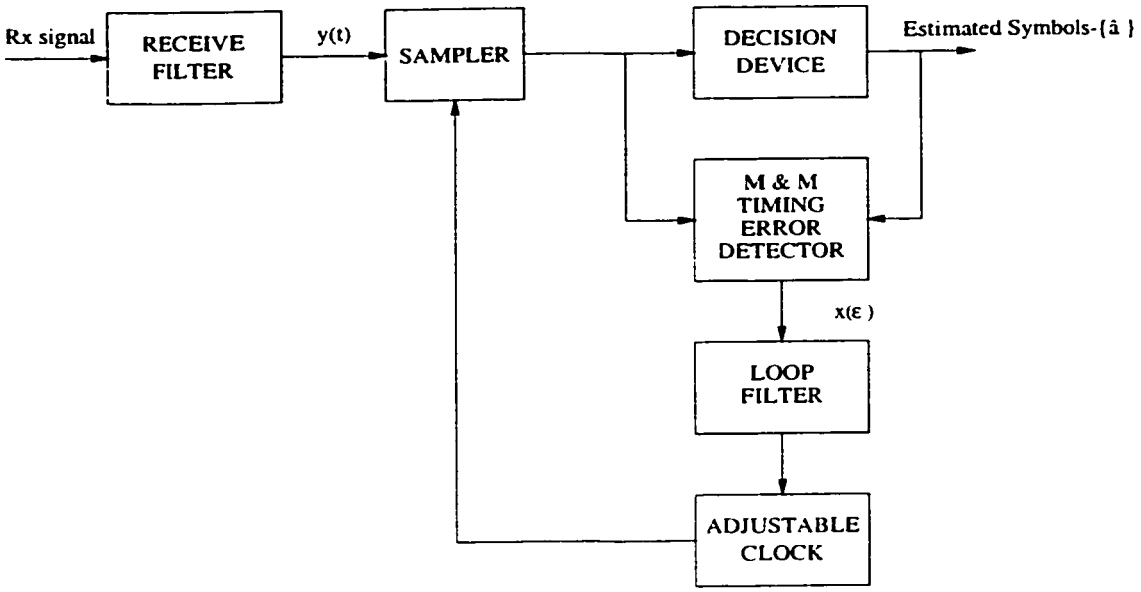

Figure 2.12: **Block diagram of receiver with Mueller and Muller Synchronizer**

2.4.2.1 The Mueller and Muller (M & M) Synchronizer

The Mueller & Muller synchronizer [9] is a discrete-time error tracking synchronizer, which derives an indication about the delay difference between the received signal and the sampling clock from samples of the receive filter output signal $y(t;\varepsilon)$ taken at the channel symbol rate $1/T$. The M & M synchronizer is represented by the block diagram shown in Figure 2.12.

The timing error detector produces a sequence $x_k(\varepsilon,\widehat{\varepsilon})$, which is determined by

$$x_k(\varepsilon,\widehat{\varepsilon}) = \widehat{a}_{k-1}y(kT+\widehat{\varepsilon}T;\varepsilon) - \widehat{a}_k y(kT-T+\widehat{\varepsilon}T;\varepsilon) \tag{2.20}$$

where $\widehat{a}_m$ denotes the receiver's decision about the m^{th} channel symbol a_m. As the timing error detector makes use of the receiver's decision, the M & M synchronizer is *decision-directed.*

The PAM signal $y(t;\varepsilon)$ at the input of the synchronizer is given by

$$y(t;\varepsilon) = \sum_m a_m g(t-mT-\varepsilon T) + n(t) \tag{2.21}$$

where $\{a_m\}$ is a stationary sequence of not necessarily binary data symbols, $g(t)$ is the baseband pulse and $n(t)$ is stationary noise.

The adjustment clock samples the signal $y(t;\varepsilon)$ at the instants t_k, given by

$$t_k = kT + \widehat{\varepsilon}T \tag{2.22}$$

The resulting samples are denoted by $y_k(\varepsilon,\widehat{\varepsilon})$,

$$y_k(\varepsilon,\widehat{\varepsilon}) = y(kT + \widehat{\varepsilon}T;\varepsilon) \tag{2.23}$$

These samples are combined with the receiver's decision $\{\widehat{a}_m\}$. to form the following timing error detector output samples:

$$x_k(\varepsilon,\widehat{\varepsilon}) = \widehat{a}_{k-1}y_k(\varepsilon,\widehat{\varepsilon}) - \widehat{a}_k y_{k-1}(\varepsilon,\widehat{\varepsilon}) \tag{2.24}$$

The Mueller and Muller synchronizer uses decision feedback to produce a timing error detector output. In the absence of data transitions, the useful timing error detector output equals zero; therefore, the transmissions of long strings of identical symbols must be avoided. The loop noise consists of two components: a component due to additive noise and a self-noise component due to the tails of the baseband pulse $g(t)$. Self noise component is eliminated for a zero, steady-state timing error e_s when $g(t)$ is a (time-shifted) Nyquist pulse, satisfying [20]

$$g(mT + \overline{\tau}) = 0 \quad for \quad m \neq 0 \tag{2.25}$$

where $\overline{\tau}$ is defined by

$$g(T + \overline{\tau}) = g(-T + \overline{\tau}) \tag{2.26}$$

when this condition is fulfilled and $e_s = 0$, only additive noise contributes to the timing error detector. When this condition is fulfilled but $e_s \neq 0$, self-noise is present at the timing error detector output, and its contribution to the timing error variance is proportional to the normalized loop bandwidth $(B_L T)$ [20].

2.4.2.2 Non Decision-Directed Timing Error Detector

A second type of algorithm in the feedback systems explored was, the non-decision directed timing error detector by Floyd M. Gardner [11]. Compared to M & M algorithm, this timing error detector requires two samples per symbol to output a timing error signal. Gardner's algorithm is well suited for feedback systems. Gardner's detector needs only two samples of the signal for each data symbol. Moreover, one of the two samples serves as *symbol strobe*, i.e., the sample on which the symbol decision is made, while the other is a *mid-way* sample between two strobe samples. This algorithm is not decision directed, unlike M & M [9].

Gardner's detector is further studied and analyzed in chapter 3. A decision-directed version of this timing error detector proposed by Takahata et al [3] is also presented.

2.5 Techniques for Timing Correction/Adjustment

Timing correction serves to provide the decision device with signal samples (strobes) with minimum intersymbol interference. In synchronous analog or hybrid systems, timing adjustment is accomplished by shifting phase (delay) of a continuous timing wave. In asynchronous sampling systems, some other method of timing correction is needed. In digital receivers, the incoming signal is asynchronously sampled. That is, the sampling is not locked to the incoming pulses. In this section various methods for timing adjustment in synchronous and non-synchronous systems are studied.

2.5.1 NCO Based Hybrid Method for Synchronous Sampling

Figure 2.10 shows the block diagram of a clock recovery circuit using synchronous sampling. In the sequel, first an overview of operation of a hybrid NCO is presented and then how an NCO can be used for timing adjustment in a feedback timing loop is demonstrated.

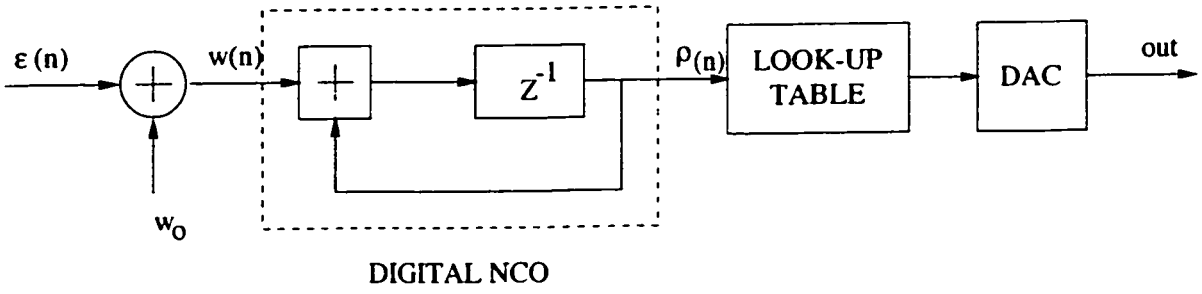

Figure 2.13: **Block diagram of a hybrid NCO**

2.5.1.1 Hybrid NCO

The block diagram of a hybrid NCO [20] is shown in Figure 2.13. It consists of two parts: a digital loop comprising a delay and a *mod*1 adder (*the so-called digital NCO*), plus a look-up table and a digital-to-analog converter (DAC). These, together transform the NCO output into a continuous-time waveform. First let us concentrate on the digital NCO. Let $w(n)$ be its input and $\rho(n)$ its output. In the sequel $w(n)$ and $\rho(n)$ are viewed as numbers between 0 and 1. At each tick of a clock $w(n)$ is added to $\rho(n)$. This results in the following difference equation:

$$\rho(n+1) = \rho(n) + w(n) mod 1 \tag{2.27}$$

As indicated in the Figure 2.13, $w(n)$ is the sum of some constant w_o plus a zero-mean signal $\varepsilon(n)$. The constant establishes the "free running" period of the NCO whereas $\varepsilon(n)$ allows us to change the period. To see how this comes about, suppose first that $\varepsilon(n) = 0$. In these conditions the NCO output will recycle every $1/w_o$ ticks. Thus, calling T_c the clock period, the free running period will be T_c/w_o. If $\varepsilon(n)$ is different from zero (but slowly varying in time), then the recycling period will be,

$$\begin{aligned} T_s(n) &= \frac{T_c}{w_o + \varepsilon(n)} \\ &\simeq \frac{T_c}{w_o}\left[1 - \frac{\varepsilon(n)}{w_o}\right] \end{aligned} \tag{2.28}$$

assuming $|\varepsilon(n)| \ll w_o$.

Returning to the scheme in Figure 2.13, a look-up table maps $\rho(n)$ into some function $f[\rho(n)]$ which in turn, is transformed into a continuous-time function by the action of the DAC and some low-pass filter.

Now, how NCO can be used to do the timing correction is addressed; The hybrid NCO consists of a sine-table ROM, the *up-crossings* of the sine-wave (zero crossings with positive slope) are used to generate command pulses for the sampler. The goal is to steer the NCO so that its actual up-crossings occur at the exact sampling instants. Because of the presence of the hybrid NCO, the overall circuit cannot be implemented in full digital form.

2.5.2 Ideal Sync Function Based Timing Correction

According to the sampling theorem [21], a bandlimited function can be reconstructed perfectly from its samples by means of a sync function, defined by

$$sinc(x) = \frac{sin(x)}{x} \tag{2.29}$$

In other words, if the sampling rate satisfies the relation

$$F_s \geq 2 \star BW(AAF)$$

where, $BW(AAF)$ is the bandwidth of the waveform from the anti-aliasing filter. In these conditions, the output sequel from the matched filter is sufficient to reconstruct the underlying continuous-time waveform through the interpolation formula,

$$y(t) = \sum_{m=-\infty}^{\infty} h_s(t - mT_s)y(mT_s) \tag{2.30}$$

where, $h_s(t) = \frac{\sin(\pi t/T_s)}{\pi t/T_s}$

The representation of the above equation is illustrated in the Figures 2.14 and 2.15,

The Digital timing correction replaces its analog counterpart as shown in Figure 2.14. This type of ideal interpolation requires a transversal filter of infinite

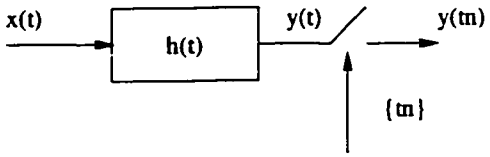

Figure 2.14: **Analog Implementation**

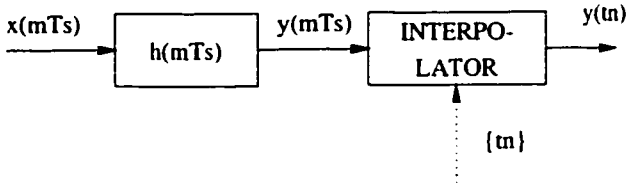

Figure 2.15: **Digital Implementation**

length, whereas only a limited number of terms can be handled in practise. One way to realize such a filter is by truncating the ideal sync function, which will inevitably cause a certain amount of signal distortion.

The direct truncation is not usually used because of the Gibbs phenomenon which can be avoided by weighting the truncated sinc with some window function [22]. Thus instead of reconstructing the continuous-time signal by using DAC and an analog filter, a discrete interpolation filter can be used to achieve the same result.

2.5.3 Polynomial based Interpolators with Non-Sync Sampling

The polynomial based interpolators have achieved a lot of attention in the past decade. The linear and cubic Lagrange interpolation were first applied to the timing adjustment problem by Gardner and Lars Erup [23, 24]. Because these interpolation methods are polynomial-based they can be implemented using the Farrow structure [25].

A polynomial based interpolator calculates the filter coefficients online, given the fraction delay μ. The underlying continuous-time impulse response $h_a(t)$ is

expressed in each interval T_s (Symbol duration) by means of a polynomial as follows,

$$h_a\left((\mu(l)-k)T_s\right)=\sum_{m=0}^{M}c_m(k)(\mu(l))^m \tag{2.31}$$

for $k=-N/2+1,-N/2+2,...,N/2$ and $\mu(l)\in[0,1)$. Here the $c_m(k)'s$ denote the polynomial coefficients for $h_a((\mu(l)-k)T_s)$ and M is the degree of polynomials. Thus, the polynomial-based interpolation filter can be implemented by filtering the input signal with $M+1$ parallel FIR filters of length N having the coefficient values of $c_m(k)$ to obtain the output samples.

The main advantage of the Farrow structure is that the filter coefficients are fixed, and the only changeable parameter is the fractional interval $\mu(l)$. The second advantage to polynomial interpolation is the time resolution is determined by the number of bits used in specifying $\mu(l)$. An arbitrarily fine resolution can be obtained by employing a long-enough word length for $\mu(l)$ and the filter coefficient [26, 27].

Cubic Lagrange or even Linear interpolation may be sufficient for the cases where the oversampling factor is high, e.g. $>>2$. However, if the oversampling factor is small (<2) the linear and cubic Lagrange interpolation are not good enough. The complexity of the Farrow structure can be reduced by increasing the sampling rate before the signal is passed through it.

2.5.4 Coefficient Memory Implementation for Interpolation Filters

Fractional delay FIR filters can also be used to implement the interpolation operation. This is done by using the so called coefficient memory implementation, where K different fractional delay FIR filters are designed having the fractional delay of $\mu_k=\frac{k}{K}$ for $k=0,1,...,K-1$. Fractional delay, μ_k is also referred to as control step size. Here K is a large integer which determines the resolution of $\mu(l)$. The coefficients of these filters are then stored into a memory, and, during the computation,

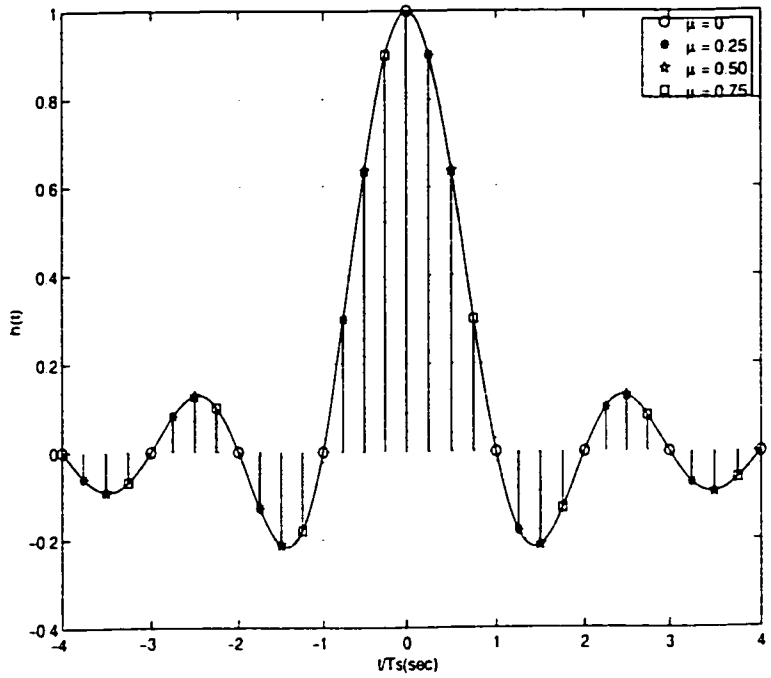

Figure 2.16: **Impulse responses for the Fractional Delay filters and the underlying continuous-time impulse response**

the desired delay can be obtained by choosing the corresponding filter coefficients from the memory [23, 24].

The impulse responses of these fractional delay filters are arranged as over-lapping polyphase components. The resulting polyphase-type impulse response then approaches the continuous-time response $h_a(t)$ when $K \rightarrow \infty$. This is illustrated in Figure 2.16 for K = 4. In this figure, the discrete-time impulse response consists of the over-lapping impulse response of the fractional delay FIR filters having the delay values of μ = *0, 0.25, 0.5 and 0.75.* The solid line illustrates the continuous-time response $h_a(t)$ that is obtained when $K \rightarrow \infty$.

The approach presented in Section 2.5.3 demands multiple computations in exchange for reduced memory requirements and the need for calling coefficients from memory. But with the advent of high speed VLSI technology, the transfer of data (i.e. coefficients) is a trivial issue.

Filter operations include delays (i.e., memory), multiplications and additions.

Reductions in number of adders and multipliers is obtained at the cost of a facility needed for transfer of coefficients values from memory to the coefficient registers. One main drawback of memory based interpolators is that, at high data rates, time is a limiting factor. Only a small number of clock intervals would be available and so a large number of bits would have to be transfered in parallel.

2.6 Comparison of NDA and DD Schemes

- NDA implementation is substantially less complicated than DD implementation in an analog synchronizer since DD estimators require signal and/or data storage, which is usually awkward with analog circuits.
- In Digital synchronizers, NDA methods are slightly more complicated than DD methods.
- DD algorithms require less computation, for binary signals, since the NDA algorithms require multiplication of samples, whereas the DD algorithms only require 1-bit sign reversal.
- NDA can be better than DD only in one characteristic, that it might be superior in acquisition when decisions are unreliable and many are wrong.
- DD estimators give statistically better estimates than an NDA estimator in the range of E_b/N_o values of practical interest.
- NDA estimators have self-noise due to non-linearity used to remove the modulation.
- NDA estimator is very sensitive to frequency errors, thus leading to a systematic bias and to an increase in the mean square error of the reference parameters.

Chapter 3

Non-data Aided Feed-Forward Estimation

3.1 Introduction

In the previous chapter (Section 2.4.1) two techniques for estimating the timing offset based on feed-forward structures were presented. Among the two approaches, NDA-ML and NDA-FFT, the scheme using the discrete Fourier transform has achieved a great deal of attention in the digital receivers. In this chapter analysis of the scheme are considered, performance bounds for such techniques are derived, the algorithm is simulated and compared to Cramer-Rao lower bounds and its implementation issues are discussed and presented.

3.2 DFT Based STR

The DFT approach makes use of signal processing techniques for extracting a symbol rate spectral line from the received signal generated by non-linear operation [19]. Once the symbol rate spectral line is extracted, its phase scaled as will be explained below.

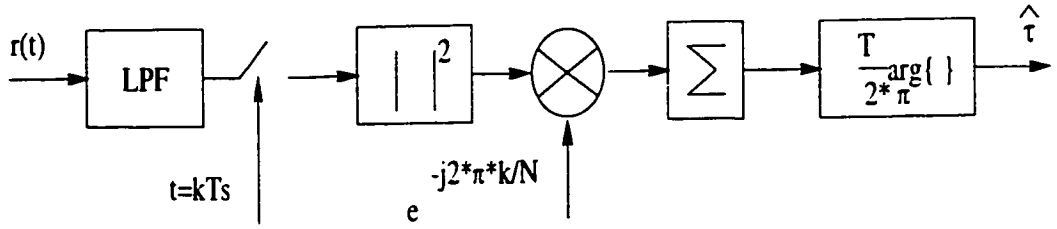

Figure 3.1: **Timing phase estimate using the spectral line method**

Referring back to Section 2.4.1 and rewriting Equation 2.6 and 2.7, we have

$$z(t) = \sum_{n=-\infty}^{\infty} a_n g_T(t - nT - \tau) + n(t) \tag{3.1}$$

where a_n are the symbols with mean power 1. $g_T(t)$ is the transmission signal pulse, T is the symbol duration, $n(t)$ is the channel noise which is assumed to be white and Gaussian with power density N_o and τ is the slowly varying time delay. The timing estimator block diagram is shown in Figure 3.1

The symbol rate spectral line may be generated by a squaring operation on the magnitude of the baseband received signal samples from the matched filter output. The output of the matched filter $g_R(t)$], $r(t) = z(t) * g_R(t)$ is sampled at rate N/T. The sequence,

$$x(k) = \left| \sum_{n=-\infty}^{\infty} a_n g\left(\frac{kT}{N} - nT - \tau\right) + n\left(\frac{kT}{N}\right) \right|^2 \tag{3.2}$$

represents the samples of the filtered and squared input signal and contains a spectral component at $1/T$.

The above statement is asserted by considering a simple baseband BPSK signal. For this demo an alternative stream of ± 1 symbols is chosen. The signal is filtered using $g(t)$, which is convolution of transmitted and received pulse shaping filter and is shown to be a Raised cosine filter. The output of the pulse shaping filter is squared and is illustrated in Figure 3.2. Once this waveform is squared, little dips are created at each rounded corners, which represent a bit transition. Thus, the squared waveform should have a fundamental harmonic at the symbol rate, with

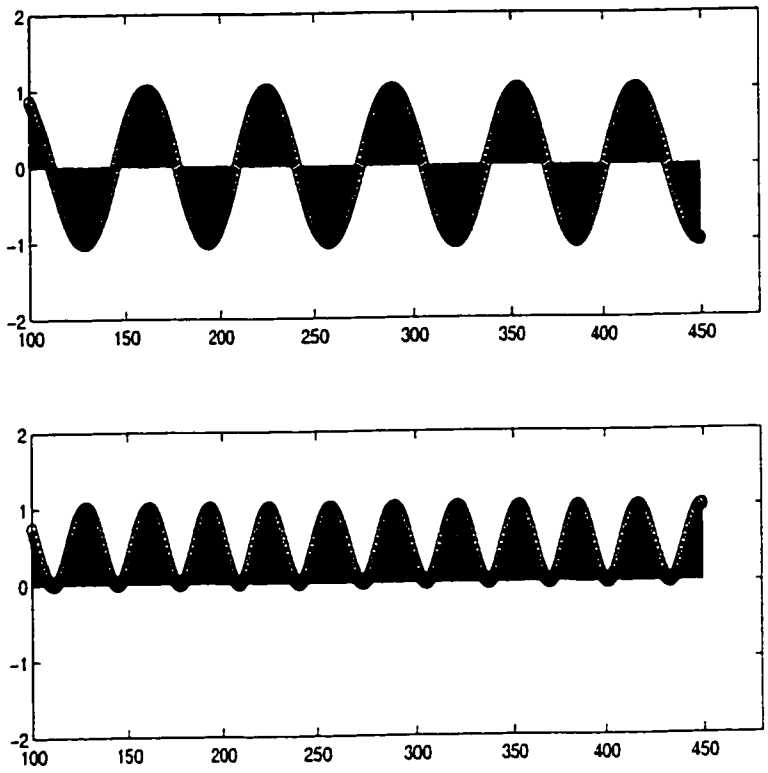

Figure 3.2: **Demonstration of TRC using spectral line**

the maximum points lying in the middle of the bit. This is illustrated in Figure 3.2. In the case of QPSK or $\pi/4$ QPSK type waveforms, each component of the complex baseband samples acts like the BPSK waveform, and when squared individually and added together, will reinforce each other to create a dip at each symbol transition. If the origin of time at the receiver is chosen to be the instant of the first sample taken from the matched filter, the optimum timing phase, relative to this origin, is obtained by computing the phase of the fundamental harmonic in units of time and reversing the sign. This would give the amount of time necessary to move the first sampling point to arrive at a maximum point on the sinusoidal waveform, which would represent the optimum symbol sampling point [18].

The spectral component created by the squaring equation can be extracted by computing DFT of the sampled squared baseband signal at the symbol rate [19]. Assuming that the burst consists of L_o symbols, and N samples of the baseband

matched filtered signal are taken per symbol interval (a minimum of 2 samples per symbol are necessary to satisfy the Nyquist sampling criteria), the DFT of the resulting signal is [18, 19]

$$X(m) = \sum_{K=0}^{L_oN-1} x_k \exp\left(-j\frac{2\pi Km}{L_oN}\right) \tag{3.3}$$

Evaluating the above expression at the symbol rate, that corresponds to $m = L_o$, the result is

$$X(m = L_o) = \sum_{K=0}^{L_oN-1} x_k \exp\left(-j\frac{2\pi K}{N}\right) \tag{3.4}$$

From Equation 3.4 we know that x_k is summation of square of in-phase and quadrature phase component of signal. Thus we have,

$$X(m) = \sum_{K=0}^{L_oN-1} \left[I^2(K) + Q^2(K)\right] \exp\left(-j\frac{2\pi K}{N}\right) \tag{3.5}$$

The optimum timing phase in units of time is then

$$\widehat{\tau} = -\frac{T}{2\pi}\left[angle\, of\, X(m)\right]$$

Evaluating angle of Equation 3.5, we have

$$angle\, of\, X(m) = -\arctan\left[\frac{\sum_{K=0}^{L_oN-1}\left[I^2(K) + Q^2(K)\right]\sin\left(\frac{2\pi K}{N}\right)}{\sum_{K=0}^{L_oN-1}\left[I^2(K) + Q^2(K)\right]\cos\left(\frac{2\pi K}{N}\right)}\right] \tag{3.6}$$

Thus,

$$\widehat{\tau} = \frac{T}{2\pi}\arctan\left[\frac{\sum_{K=0}^{L_oN-1}\left[I^2(K) + Q^2(K)\right]\sin\left(\frac{2\pi K}{N}\right)}{\sum_{K=0}^{L_oN-1}\left[I^2(K) + Q^2(K)\right]\cos\left(\frac{2\pi K}{N}\right)}\right] \tag{3.7}$$

where $arctan(.)$ returns a value over $(-\pi, \pi)$.

If the number of samples per symbol is chosen to be 4, that is N = 4, the complex exponential $\exp\left(-j2\pi\frac{K}{N}\right)$ reduces to $\exp\left(-j\pi\frac{K}{2}\right)$, Equation 3.7 reduces to

$$\widehat{\tau} = \frac{T}{2\pi}\arctan\left[\frac{\sum_{K=0}^{L_oN-1}\left[I^2(K) + Q^2(K)\right]\sin\left(\frac{\pi K}{2}\right)}{\sum_{K=0}^{L_oN-1}\left[I^2(K) + Q^2(K)\right]\cos\left(\frac{\pi K}{2}\right)}\right] \tag{3.8}$$

In cases where a less than 4 samples per symbol are used, the missing samples can be generated by using some kind of interpolation [18].

3.3 Theoretical Bounds on Performance

The output of the STR estimators are timing offset estimates and timing error signals respectively. These signals act as the control signals to other blocks in the STR. Thus, the statistics of the estimators and detectors are the key elements in the determination of the performance of a symbol timing recovery method. For example, if the estimates are biased, the resulting sampling locations selected by an estimator will be biased from the true optimum and performance will suffer. Similarly, if the estimator has a high variance, the variance of the selected location will also be high. Clearly, it is desirable to keep the variance of the estimates as low as possible.

In this section the bounds on the performance of the estimators and detectors are discussed. The performance bound for symbol timing estimation is the Cramer-Rao Lower Bound (CRLB). The CRLB for the block based symbol timing estimation is explained.

3.3.1 The Cramer-Rao Lower Bound for Block Based Estimators

The Cramer-Rao bound is used as a lower bound on the performance of symbol timing recovery systems in demodulators. It provides a benchmark against which the performance of synchronizers could be compressed.

In this section, bounds on the variance of the estimation errors for non-random but unknown parameters are discussed. Such bounds are useful since they allow to compare the variance of a suboptimal (but realizable) estimator to that of an optimal (but non realizable) estimator in order to assess the implementation loss of the suboptimal estimator [5].

Let r be the received signal vector and $\theta = (\theta_1, \theta_2, ...\theta_k)$ be a set of K nonrandom parameters. Let $\widehat{\theta}(r)$ be the corresponding estimate. Note that $\widehat{\theta}(r)$ depends on the observation r. Its expectations may, or may not, coincide with the true value

of θ. If it does, then the estimate is unbiased. Being unbiased is clearly a favorable feature as, on an average, the estimator will yield true value of the unknown parameter. Even an unbiased estimator, however may be unsatisfactory if the errors $\widehat{\theta}(r)$ - θ are widely scattered around zero. To know what is the minimum error desirable, Cramer-Rao bound provides the answer.

The Cramer-Rao bound, which is the lower limit to the variance of any unbiased estimator, is expressed as [5]

$$var\left\{\widehat{\theta}(r) - \theta\right\} \geq CRLB(\theta) \tag{3.9}$$

where

$$CRLB(\theta) \cong \frac{1}{E_\theta\left\{\left[\frac{\partial \ln \Lambda(r/\theta)}{\partial \theta}\right]^2\right\}} \tag{3.10}$$

where E_θ is the expectation of enclosed quantity with respect to θ. No unbiased estimator can provide smaller errors than those indicated by Equations 3.9 and 3.10.

3.3.2 Derivation of CRLB

The CRLB for the parameter estimation is defined above. In this section, the lower bound for symbol timing offset $\widehat{\tau}$ is derived. Rewriting Equation 2.8, we have

$$\Lambda(\widehat{\tau}) = p(z(t)/\widehat{\tau})$$

where

$$z(t) = x(t;\tau) + n(t)$$

and

$$x(t;\tau) = \sum_{n=-\infty}^{\infty} a_n g(t - nt - \tau)$$

and $p(z(t)/\widehat{\tau})$ is the probability density function of the received signal $z(t)$.

The resultant CRLB for symbol timing offset $\widehat{\tau}$ is given by

$$\frac{1}{T^2}CRLB(\tau) = \frac{1}{8\pi^2\xi} \cdot \frac{1}{E_s/N_o}$$

where $\xi = \frac{1}{12} + \alpha^2\left(\frac{1}{4} - \frac{2}{\pi^2}\right)$, which is the normalized mean square bandwidth of $G(f)$, root-raised cosine pulse.

The above was derived assuming a single pulse. When assuming L_o adjacent pulses, the CRLB is given by

$$\frac{1}{T^2}CRLB(\tau) = \frac{1}{8\pi^2\xi L_o} \cdot \frac{1}{E_s/N_o}$$

Detailed derivation of equations is omitted here due to complex nature of equations.

3.4 Performance of FFT based STR

Simulations were carried on by varying various parameters, such as, roll-off value, estimation interval and number of samples per symbol.

Figure 3.3 and 3.4 show the simulation results of Oerder and Meyr scheme [19].

- N = 3 & 4 (T/T_s)
- Alpha = 0.4

Results show that as the estimation range is increased, the variance of the estimate is closer Cramer-Rao lower bound.

Next the symbol estimation interval was fixed and simulations were carried on by varying the roll-off values (Figure 3.5 and Figure 3.6)

- N = 3 (T/T_s)
- Alpha = 0.35, 0.50 and 0.75

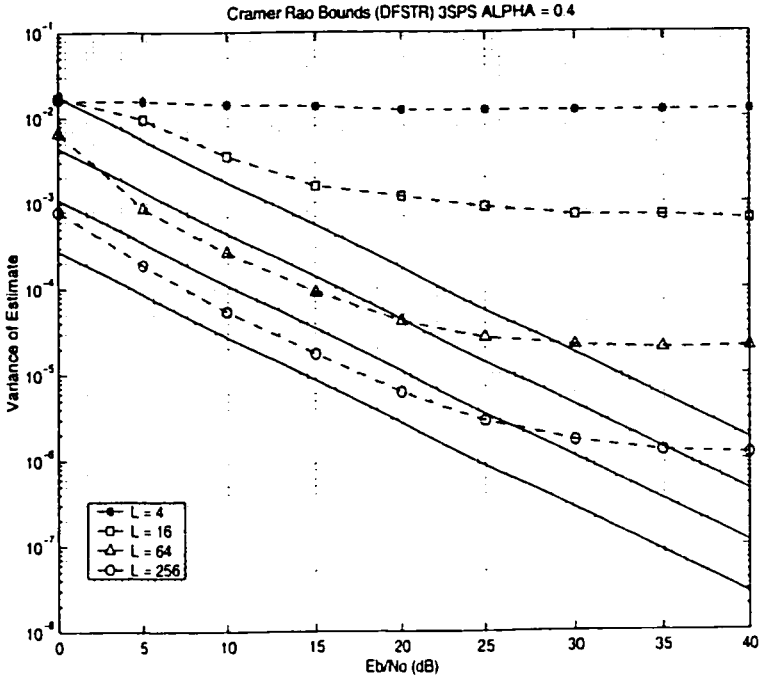

Figure 3.3: **CRLB for Oerder and Meyr scheme (varying L, 3SPS, and ALPHA = 0.4)**

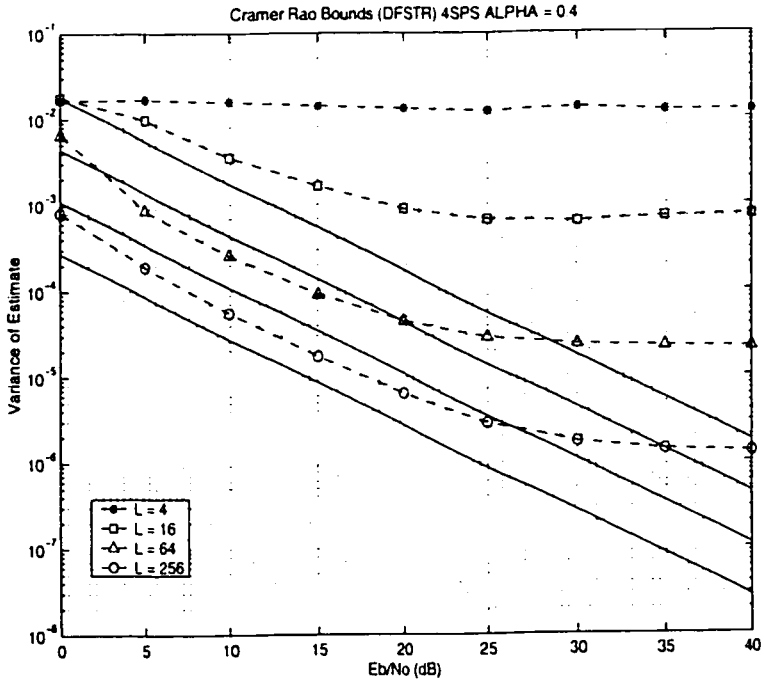

Figure 3.4: **CRLB for Oerder and Meyr scheme (varying L, 4SPS, and ALPHA = 0.4)**

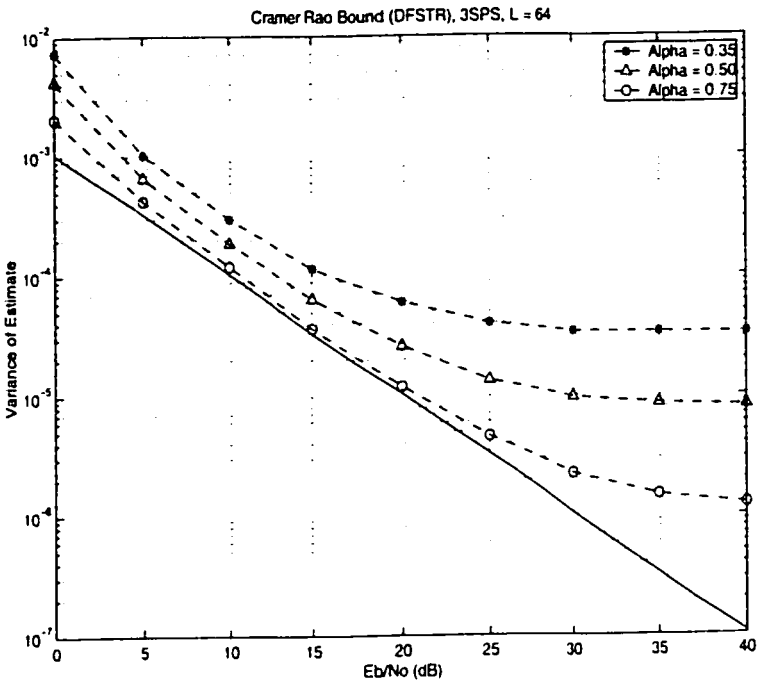

Figure 3.5: **CRLB for Oerder and Meyr scheme (varying roll-off values, 3SPS, and L = 64)**

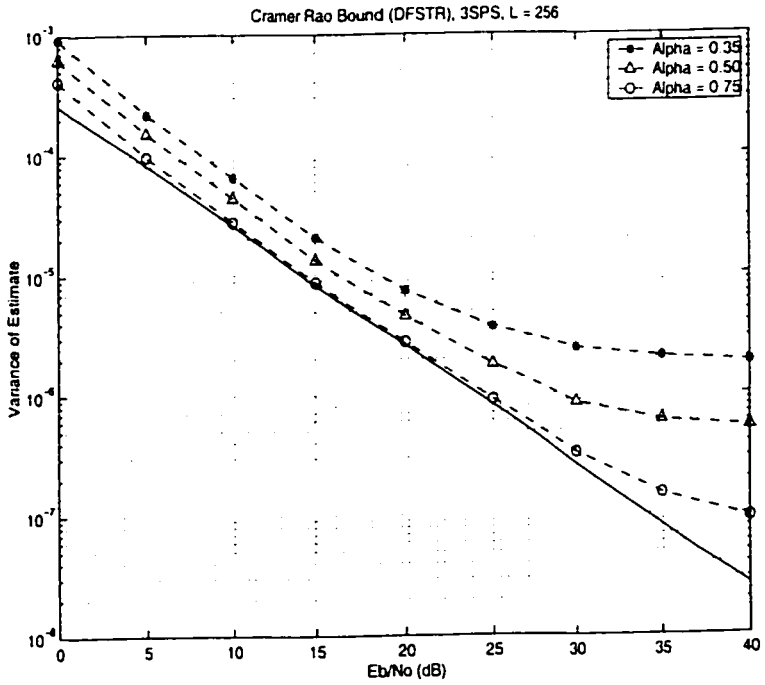

Figure 3.6: **CRLB for Oerder and Meyr scheme (varying roll-off values, 3SPS, and L = 256)**

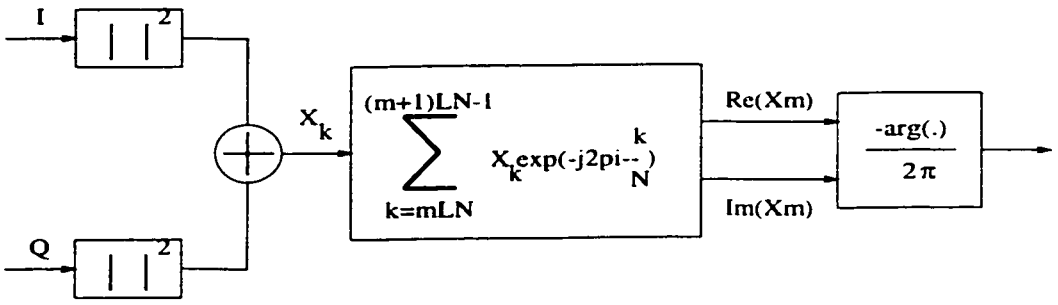

Figure 3.7: **Block Diagram of DFT based Timing Estimator**

Figure 3.5 illustrates the results for L = 64 and Figure 3.6 for L = 256.

It is observed that as the excess bandwidth factor is increased, the accuracy of the variance of estimate is close to the Cramer-Rao lower bound. Also for L = 256, the accuracy and performance are much better than L = 64.

3.5 Implementation Issues and Considerations

A block diagram for the timing estimator using the DFT [19] method is shown in Figure 3.7. The algorithm for the symbol timing recovery is given in Section 3.2, which produces a spectral component at $1/T$. The spectral component is extracted by calculating the complex Fourier coefficient at the symbol rate for each section of length LT (i.e., *LN samples*). The normalized phase of this estimator is then an unbiased estimate of the fractional delay time. For this implementation, N = 4 (i.e. 4 samples per symbol) was chosen, this reduces the operations to the addition and subtraction of squared output samples. Since *sine* and *cosine* functions take only values 0 and ± 1, no multiplications are necessary. Equation 3.8 represents the output of timing phase estimator for N = 4. The samples are processed at the symbol rate $1/T$ rather than at $4/T$ sampling rate.

Realization of the timing estimator is shown in Figure 3.8. The incoming signal in each channel is squared and accumulated for L symbols. Spectral component is determined by taking the argument of accumulated values of samples. The *atan*(.)

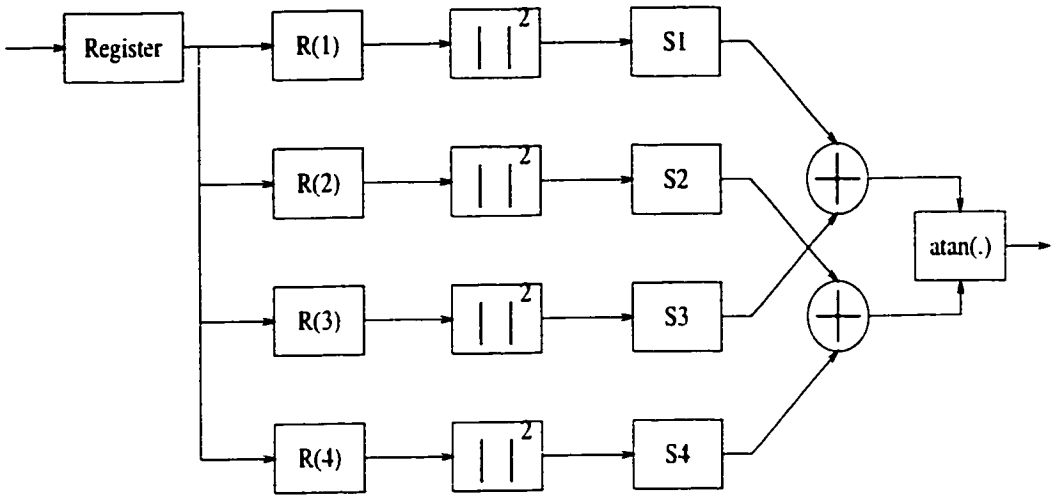

Figure 3.8: **Realization of the DFT based Timing Estimator**

function can be implemented in a LUT and hence requires only a single operation per block.

Chapter 4

Feedback Timing Error Detectors

4.1 Introduction

In this chapter feedback techniques for timing estimation and correction are studied and their performance is evaluated. Feedback implementations use the maximum likelihood estimate to derive a timing phase detector, which is used to indicate the direction of the required timing adjustment and the intensity with which the adjustment is to be applied. A typical symbol timing recovery structure with feedback loop is shown in Figure 4.1.

In Figure 4.1, the incoming signal is sampled with a nominal period T_s, at

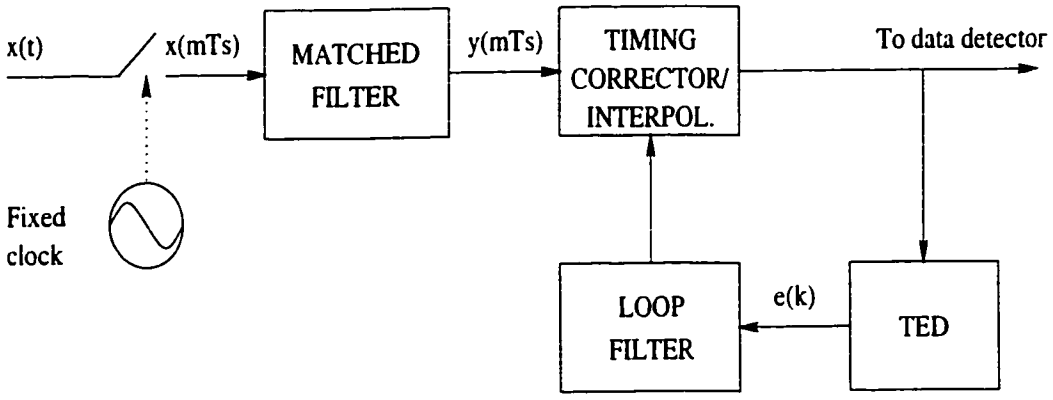

Figure 4.1: **Feedback Configuration**

some timing offset, τ, from optimum. The initial timing offset, τ_o, is random over the range $[-T/2, +T/2]$. The matched filter signal samples are used by the timing error detector to direct the update of the sample location in the succeeding symbol period. The output of the timing error detector is filtered by a loop filter and applied to the timing corrector/interpolator.

Feedback symbol timing recovery loops are phase locked loops and hence as the operation of the loop progresses, the timing offset will gradually decrease until its mean value is zero. A mean value of zero requires the use of an integrating loop filter to remove fixed timing offset. Clearly the performance of the timing phase detector will have a strong influence on the performance of the STR scheme.

In Section 4.2, a Non-Decision directed approach based on Gardner's [11] algorithm is presented. Takahata et al [3] presented a decision directed timing phase estimator, which uses the fundamental equation from Gardner is presented in Section 4.3.

4.2 Non-Decision Directed TED

A non-decision directed timing phase detector originally developed by Gardner [11] is given by,

$$u_t(r) = y_I(r - \frac{1}{2})\,[y_I(r) - y_I(r-1)] + y_Q(r - \frac{1}{2})\,[y_Q(r) - y_Q(r-1)] \qquad (4.1)$$

has resemblances to the Wave Difference Method. It may also be derived from the maximum likelihood principle as shown by Oerder [28].

The Equation 4.1 may be understood physically as follows: The timing error detector samples the quadrature-phase signals between the strobe time. If there is transition between symbols, the average mid-way sample is zero in absence of timing error. An error gives a non-zero mid-way sample, but the slope information necessary for the error correction is missing. If there is no transition between two consecutive symbols, their strobe values are the same, and the mid-way sample is rejected. If

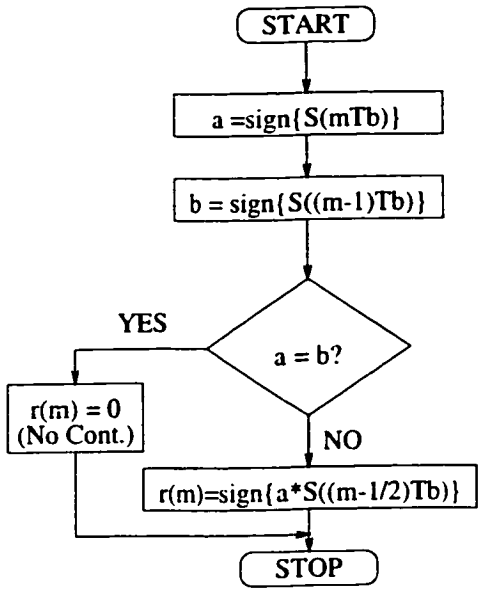

Figure 4.2: **Flow chart for determining the timing error signal**

there is a transition, the strobe values are different, and the difference provides the required slope information. The product of the slope information and the mid-way sample provides the timing error information. The timing error is corrected with the help of a combined interpolation and decimation filter. This timing algorithm is suitable for both tracking and acquisition modes of operation. Furthermore, timing lock can be obtained without depending on prior carrier phase acquisition [11]. The complexity of the timing circuit is relatively low.

4.3 Decision Directed Timing Phase Detector

In 1987 Takahata et al [3] presented a modified timing error detector based on the non-decision directed algorithm [11]. This type of timing detector falls under the Decision-Directed (DD) class of algorithms, since it uses decisions made on the received signal to produce timing error signal. The algorithm requires two samples per symbol for its operation i.e., to estimate an error signal. The flow chart in Figure 4.2 shows a procedure for detecting the clock timing error.

The algorithm examines the two strobes values to either side of the midway sample. If the strobe values are the same, then no timing information is available. The mid sample is thus rejected as no timing information is available in the absence of a transition.

If a transition is present, the strobe values will be different. A control signal ($r(m)$) is generated by taking the product of sign of first strobe and the midway sample. The midway sample $S((m-1/2))$ has the unique feature of having values at zero-crossing points when the value of data changes from -1 to +1 or from +1 to -1. That is, the average value of $S((m-1/2))$ becomes approximately zero so long as the sequence $S(m)$ has values sampled at the best eye opening condition.

4.4 Theoretical Bounds for Performance

In Section 3.3.1 CRLB for estimators such as those used in feed-forward STR structures was defined. In this chapter STR structures pertaining to feedback configuration are studied and analyzed, thus need arises to define theoretical bounds for feedback estimators. Cramer Rao lower bounds are derived for feedback structures in the section to follow.

4.4.1 The CRLB for Feedback STR Structures

Normalized timing error variance [5] is given as,

$$\sigma_\tau^2 = \frac{1}{T^2} \sum_{m=-\infty}^{\infty} R_n(m)\eta(m) \tag{4.2}$$

where $R_n(m) = E[n(k+m)n(k)]$ is the autocorrelation function of the noise and $\eta(m)$ is the convolution of $h(k)$ with $h(-k)$, wher $h(k)$ is the impulse response of the loop filter, i.e.,

$$\eta(m) = \sum_{i=-\infty}^{\infty} h(iT)h[(i-m)T]$$

After some manipulation, it is found that [5]

$$\sigma_\tau^2 = \frac{2B_L T}{A^2} \cdot \frac{1}{T^2} \sum_{m=-\infty}^{\infty} R_n(m)(1-\gamma A)^{|m|} \tag{4.3}$$

where B_L is loop filter bandwidth, A is the slope of the S-curve when the timing error is equal to zero and is given by $A = -q''(0)$ and $q(t) = g(t) \bigotimes g_{MF}(t)$ is the convolution of the root-raised cosine pulse with the matched filter response.

The computation of the timing error variance σ_τ^2 requires a knowledge of the autocorrelation $R_n(m)$ of the noise. The noise variance is given by [5],

$$R_n(m) = \frac{N_o}{2} \cdot 4\pi^2 \int_{-\infty}^{\infty} f^2 |G(f)|^2 \, df \tag{4.4}$$

From Equations 4.3 and 4.4, the timing error variance is given by

$$\sigma_\tau^2 = \frac{N_o B_L}{A^2 T} \cdot 4\pi^2 \int_{-\infty}^{\infty} f^2 |G(f)|^2 \, df \tag{4.5}$$

Then, substituting A, we have

$$\sigma_\tau^2 = \frac{N_o B_L}{q''^2(0) T} \cdot 4\pi^2 \int_{-\infty}^{\infty} f^2 |G(f)|^2 \, df \tag{4.6}$$

and recognizing $q(t) = g(t) \bigotimes g_{MF}(t)$, it can be seen that $-q''(t)$ has the Fourier transform $-4\pi^2 f^2 |G(f)|^2$ and hence, $-q''(0)$ can be written as

$$q''(0) = -4\pi^2 \int_{-\infty}^{\infty} f^2 |G(f)|^2 \, df \tag{4.7}$$

Also the signal energy is given by

$$E_s = \int_{-\infty}^{\infty} |G(f)|^2 \, df \tag{4.8}$$

substituting 4.7 and 4.8 in 4.6 produces

$$\sigma_\tau^2 = \frac{B_L T}{4\pi^2 \xi} \cdot \frac{1}{E_s/N_o} \tag{4.9}$$

where ξ is a coefficient given by

$$\xi = T^2 \frac{\int_{-\infty}^{\infty} f^2 |G(f)|^2 \, df}{\int_{-\infty}^{\infty} |G(f)|^2 \, df} \tag{4.10}$$

It is also given [5]

$$B_L T = \frac{1}{2L_o} \tag{4.11}$$

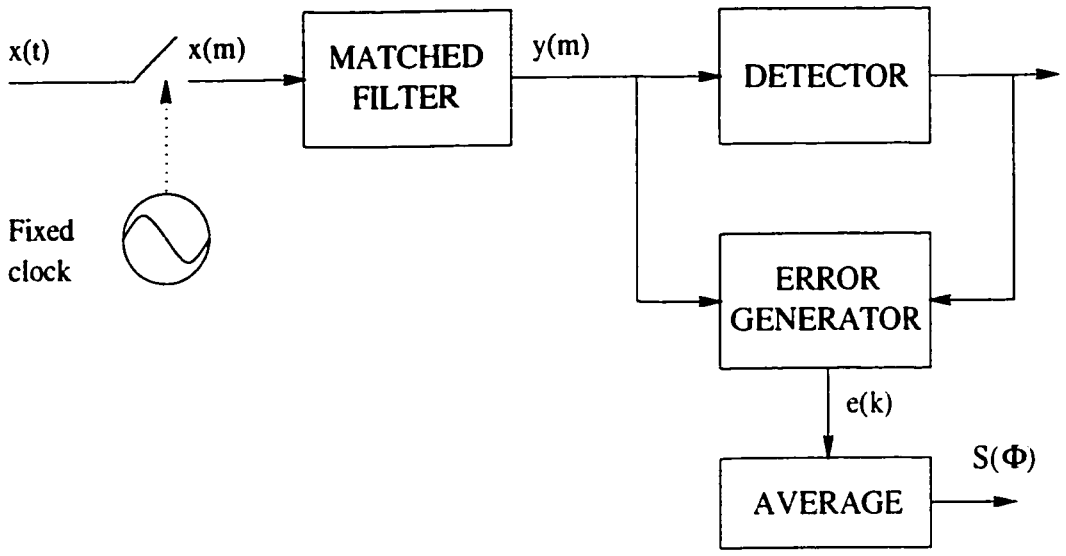

Figure 4.3: **Measuring the S-curve of the detector**

4.5 Performance Analysis

4.5.1 Acquisition Performance

At the start of signal reception the synchronizer has no knowledge about the value of the parameters. During a start-up phase the synchronizer reduces the initial uncertainty to a small steady-state error. This process is called acquisition. To efficiently use the channel, the acquisition time should be short.

A key tool to investigate acquisition is the S-curve of the phase error generator. This is the expectation of the error signal $e(k)$, conditioned on a fixed value of the difference $\phi \cong \tau - \widehat{\tau}$, i.e.,

$$S(\phi) \cong E\left[e(k) \mid \phi\right]$$

Experimentally $S(\phi)$ is obtained by opening the loop and measuring the time average of the error signal as indicated in Figure 4.3.

The S-curve for Gardner's detector is derived in [5]. It is given by,

$$S(\delta) = \frac{4C_2K}{T}\sin\left(\frac{2\pi\delta}{T}\right) \tag{4.12}$$

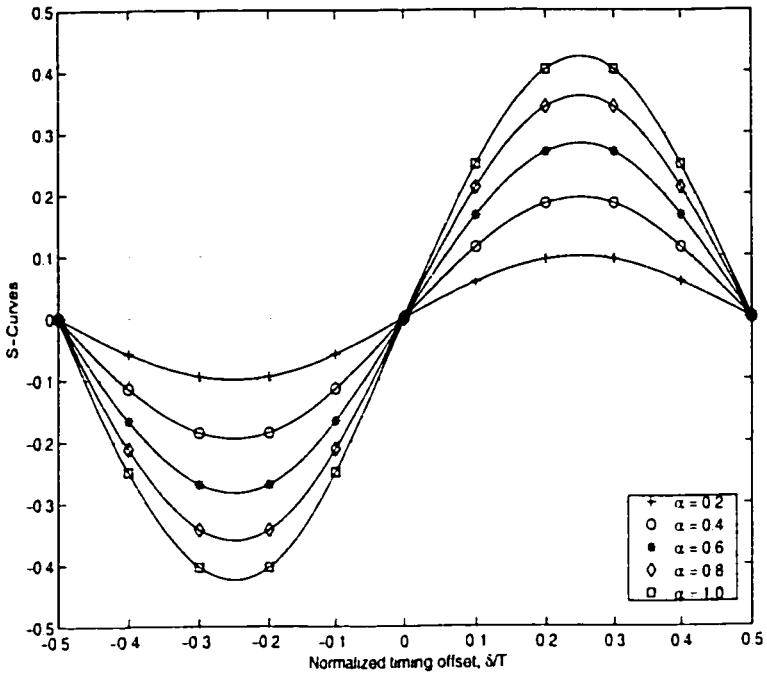

Figure 4.4: **S-Curves for Gardner's Timing Error Detector**

where C_2 is given by $C_2 = \frac{E_s}{\int_{-\infty}^{\infty}|G(f)|^2 df}$, E_s is the signal energy and $G(f)$ is the Fourier transform of $g(t)$, raised cosine pulse.

In particular, with raised cosine roll-off function with roll-off α the constant K is given by

$$K = \frac{1}{4\pi(1-\alpha^2/4)} \sin\left(\frac{\pi\alpha}{2}\right)$$

Equation 4.12 indicates that the S-curve is sinusoidal of period T and passes through the origin at $\delta = 0$. Its amplitude is proportional to K, which depends on the roll-off factor. As α decreases, K gets smaller and smaller and the amplitude of the S-curve becomes inadequate for the tracking operation. Thus, the Gardner detector is ill-suited for narrow-band signaling. Figure 4.4 illustrates the S-curve for Gardner's detector for various values of α.

It can be seen that S-curve depends only on the channel impulse response and is not affected by the signal-to-noise ratio.

The acquisition time taken by Gardner's detector before the data could be

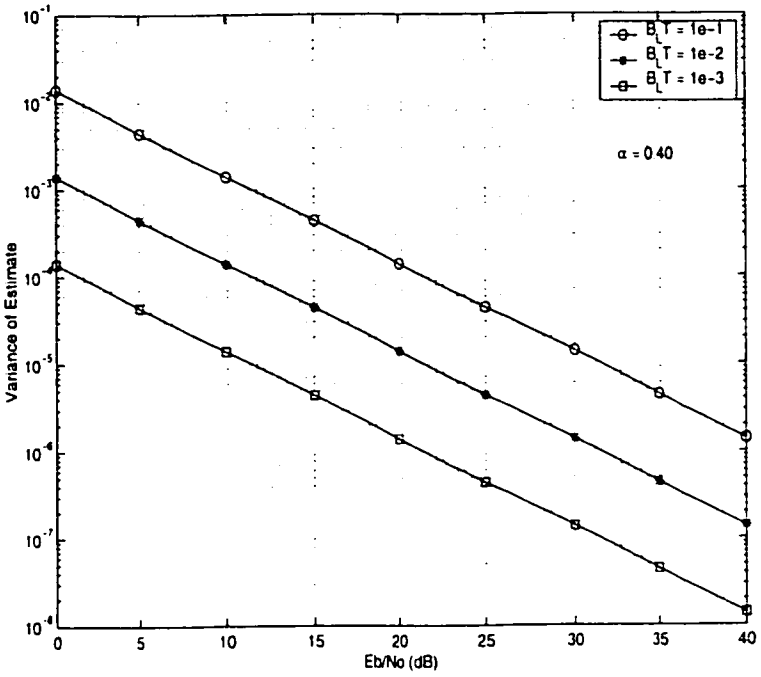

Figure 4.5: **Effect of Loop Bandwidth on Variance of Estimate**

sampled at the best eye opening is 600 symbols [29].

4.5.2 Tracking performance

The synchronizer provides an estimate which most of the time exhibits small fluctuations about the true value. The synchronizer is operating in the tracking mode. The performance measure of this mode is the variance of the estimate.

The tracking performance of Gardner's detector (section 4.2) has been well documented in [5, 30]. The performance of timing error detector is strongly affected by the roll-off factor and degrades significantly as α decreases. This is in contrast with the behavior of decision-directed detectors which are much less sensitive to roll-off factor [5]. Thus, it can be concluded that Gardner's detector is not useful for narrow-band signaling.

Figure 4.5 shows the effect of loop bandwidth on the tracking performance of the timing error detector. It is seen that with increasing loop bandwidth, the

tracking performance detoriates due to increase in self noise. On the other hand, if the loop bandwidth is increased the acquisition of the loop is faster.

Chapter 5

Proposed TED using DD Feedback Technique and a Filter Interpolation Approach

5.1 Introduction

In this chapter a novel timing error detector based on the detector by Gardner using the feedback configuration is introduced. In Section 5.2, the elements of the timing loop are explained. Equations concerning the generation of control signals are given. Section 5.3 explains the proposed timing error detectors. Section 5.4 explains how an RRC filter can be used instead of an interpolating FIR filter for correcting the timing phase error of the signal. Performance of the proposed schemes is presented in Section 5.5. Various simulation results pertaining to acquisition time, tracking performance, S-curve and bit error rate are presented. Finally, in Section 5.6 hardware implementation structures and issues are discussed. Also, implementation structure for Gardner's detector is presented and comparisons are made in terms of hardware resources. Issues concerning the hardware requirements of timing error detector on-board the satellite are also discussed.

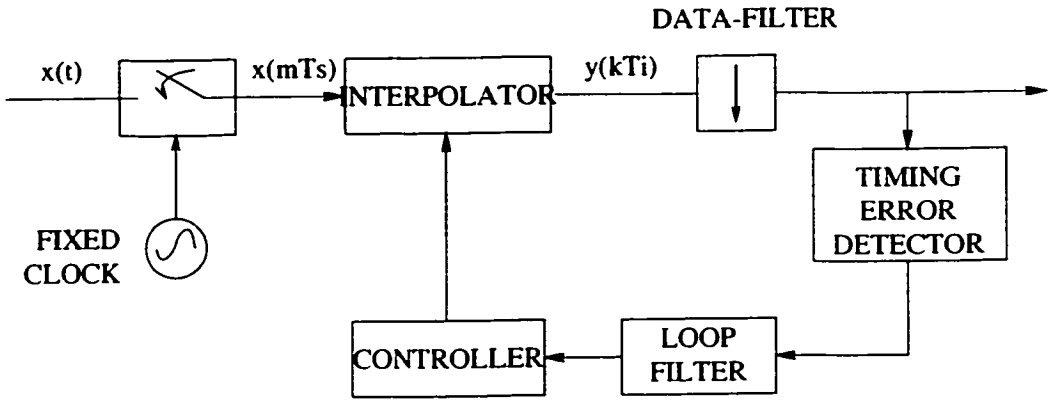

Figure 5.1: **Digital timing recovery feedback loop**

5.2 Feedback Timing Control Loop Model

In this section the elements of the timing loop in a feedback system are revisited. The main emphasis will be on the control block of the loop which generates the fractional delay and base point index. Equations concerning the generation of control signals will be explained.

5.2.1 Feedback Loop

Figure 5.1 illustrates various elements of digital timing recovery loop. A time-continuous, PAM signal $x(t)$ is received. Symbol pulses in $x(t)$ are uniformly spaced at intervals T. Assuming that $x(t)$ is bandlimited so that it can be sampled at a rate $1/T_s$ without aliasing. If $x(t)$ is not adequately bandlimited, aliasing will introduce distortion that causes a performance penalty. Samples $x(mT_s) = x(m)$ are taken at uniform intervals T_s. The ratio T/T_s is assumed to be irrational, as it is the case in all practical situations where the symbol timing is derived from a source that is independent of the sampling clock. These signal samples are applied to the interpolator, which computes interpolants, designated $y(kT_i) = y(k)$ at intervals T_i. Assuming that $T_i = T/K$ where K is a small integer, a downsampler is employed to compute the strobes that are used for data and timing recovery.

The interval T_i between the interpolants is not constant. A modem always adjusts the interval so that the strobes can be brought into synchronism with the data symbols of the signal; thus, the interpolation interval cannot be constant.

All elements within the feedback loop contribute to the synchronization process. Timing error is measured by the timing error detector and filtered in the loop filter, whose output drives the controller. The interpolator obtains instructions for its computations from the controller.

The data filter (or decimator) is placed within the feedback loop. The placement is not essential, it could be placed outside the loop, prior to the interpolator. If the data filter is placed before the interpolator, then the sample rate of the data filter must be maintained high enough to avoid aliasing. Thus, the data filter is placed inside the feedback loop and after the interpolator.

The loop filter is modeled as a simple accumulator or a low order butterworth filter. In this study a simple accumulator is considered. Various timing error detectors estimators have been explained in the preceding chapters. A novel approach based on the Timing error detector of Gardner [11], is proposed in the next section. In the remaining section, the emphasis will be on the digital interpolator control. The generation of control signal will be explained.

5.2.2 Interpolator Equation

The interpolator equations are well defined in paper by Takahata and Gardner [3, 23]. For understanding purpose they have been reproduced here. The same underlines the adaptive rate converter in [3].

Figure 5.2 shows a fictitious, hybrid analog/digital method of rate conversion. The Digital-to-Analog (DAC) converts the samples to a sequence of weighted analog impulses, which are applied to a time-continuous, analog, interpolating filter with

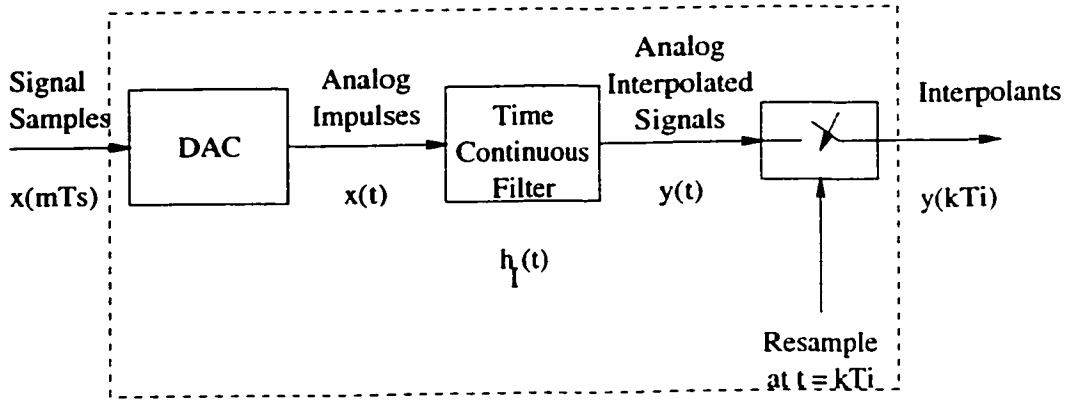

Figure 5.2: **Rate conversion with time-continuous filter**

impulse response $h_I(t)$. The time-continuous output of the filter is

$$y(t) = \sum_m x(mT_s)h_I(t - mT_s) \tag{5.1}$$

Observe that $y(t) \neq x(t)$. There is no attempt and no need to recover the original waveform, contrary to most conventional interpolation. Since a modem is required to perform filtering of signals there is no reason why some of the filtering cannot be included in the interpolator.

The signal $y(t)$ is resampled at time instants $t = kT_i$ where T_i is synchronized with the signal symbols. In general, T_i/T_s is irrational; the sampling and symbol rates are incommensurate. The new samples-the interpolants-are represented by

$$y(kT_i) = \sum_m x(mT_s)h_I(kT_i - mT_s) \tag{5.2}$$

Although the model includes a fictitious DAC and a fictitious analog filter, the interpolants in (Equation 5.2) can be computed entirely digitally from knowledge of: 1) the input sequence $x(m)$, 2) the impulse response $h_I(t)$ of the interpolating filter, and 3) the time instants mT_s and kT_i of the input and output samples. These digitally computed interpolants have identically the same values if the analog operations had been performed.

A more useful format is obtained by rearranging the indexing in (Equation 5.2).

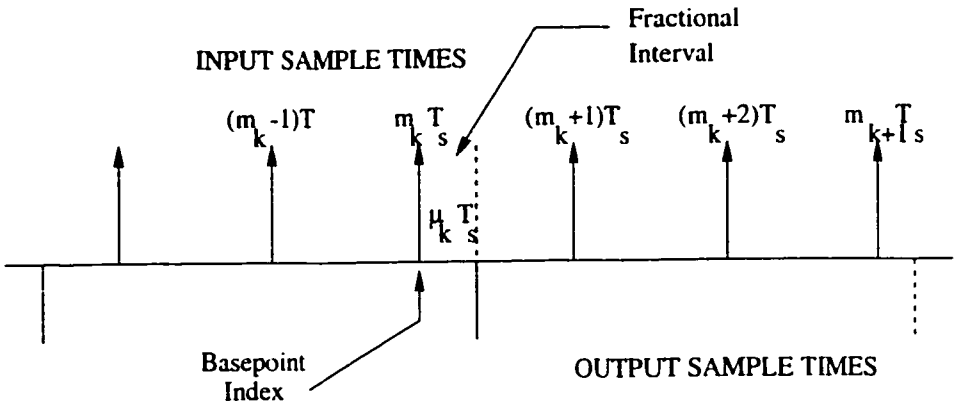

Figure 5.3: **Sample Time relations**

Recognizing that m is a signal index, define a filter index

$$i = int\,[kT_i/T_s] - m \tag{5.3}$$

where $int[z]$ means largest integer not exceeding z. Also, define a basepoint index

$$m_k = int\,[kT_i/T_s] \tag{5.4}$$

and a fractional interval

$$\mu_k = kT_i/T_s - m_k \tag{5.5}$$

where $0 <= \mu_k < 1$. Timing relations are illustrated in Figure 5.3.

Function arguments in (Equation 5.2) become $m = m_k - i$ and $(kT_i - mT_s) = (i + \mu_k)Ts$, and the interpolant is computed at time $kT_i = (m_k + \mu_k)T_s$. Equation (5.2) can be rewritten as

$$\begin{aligned} y(kT_i) &= y\,[(m_k + \mu_k)T_s] \\ &= \textstyle\sum_{i=I_1}^{I_2} x\,[(m_k - i)T_s]\,h_I\,[(i + \mu_k)T_s] \end{aligned} \tag{5.6}$$

Equation (5.6) is the foundation of digital interpolation in modems.

If the interpolating filter has finite impulse response (FIR), then I_1 and I_2 are fixed, finite numbers and the digital filter actually used for computing the interpolants has $I = I_2 - I_1 + 1$ taps.

At this point, most DSP accounts of interpolation assume that the ratio T_i/T_s is rational. No such assumption will be made here; real-world symbol rates are almost never synchronous with independent, fixed-rate sampling clocks. Assuming a commensurate ratio tends to obscure broader issues of control and implementation.

When T_i is incommensurate with T_s, the fractional interval μ_k will be irrational and will change for each interpolant. If determined to infinite precision, μ_k takes on an infinite number of values, which never repeat exactly. This behavior is contrary to that observed if T_i is assumed very nearly equal to T_s - if sampling is nearly synchronized. Then μ_k changes only very slowly; if μ_k is quantized, it might remain constant over many interpolants. If T_s were commensurate with T_i, but not equal, then μ_k would cyclicly repeat a finite set of values, when the timing loop is in equilibrium.

5.3 Proposed Timing Error Detector (TED)

The proposed new digital symbol timing recovery algorithm has a structure based on the Gardner's timing error detector [11]. The algorithm is independent of the carrier recovery and requires only two samples per symbol for its operation. The proposed scheme requires less hardware processing speed when compared to spectral line estimators in the feed-forward configurations(chapter 3). Performance is analyzed by computer simulations in various aspects such as jitter performance, timing detector output characteristics(s-curve), acquisition time and a complete closed loop simulation is performed to evaluate the system performance in terms of probability of bit error rate. In the following section, the proposed algorithm is presented and its operation is explained.

5.3.1 Algorithm

Rewriting the equation of received filtered signal, we have

$$y(kT_i) = \sum_m x(mT_s)h_I(kT_i - mT_s) \tag{5.7}$$

The main function of clock recovery is obtaining the sequence $y(kT_i)$ at the best eye-opening condition, which is accomplished by monitoring the clock timing error and subsequently updating the control signals to the interpolator.

A novel approach for detecting the clock timing error is proposed. The TED algorithms in [3, 11] are based on observing *2 symbols* and using the mid-sample for generating a timing error signal. In the proposed structure, the observation is extended over three symbol durations. The idea behind this technique is to reduce the acquisition time and obtain a better tracking performance as will be demonstrated in the later sections. It is proved through computer simulations that new approach acquires lock faster than the schemes surveyed and has comparable jitter performance.

Figure 5.4 shows the procedure for detecting the clock timing error. The sequence $y((k + 1/2)T_i)$ is also produced in order to check the eye-opening condition. This sequence has a unique feature of having values around at zero-crossing points when the value of data changes from -1 to +1 or from +1 to -1. In other words, the average value of $y((k + 1/2)T_i)$ becomes approximately zero so long as the sequence $y(kT_i)$ has values sampled at the best eye-opening condition. On the other hand, if there exists a lag or lead clock phase, the sequence $y((k + 1/2)T_i)$ has value set apart from zero-crossing point. In the case of the lag clock phase, the sequence $y((k + 1/2)T_i)$ has minus values when the value of data changes from +1 to -1, and a plus value when the value of data changes from -1 to +1. On the other hand, in the case of the lead clock phase, the sequence has plus and minus values when the value of data changes from +1 to -1 and from -1 to +1 respectively. The clock timing error can therefore be detected by adopting to the flowchart shown in Figures 5.5

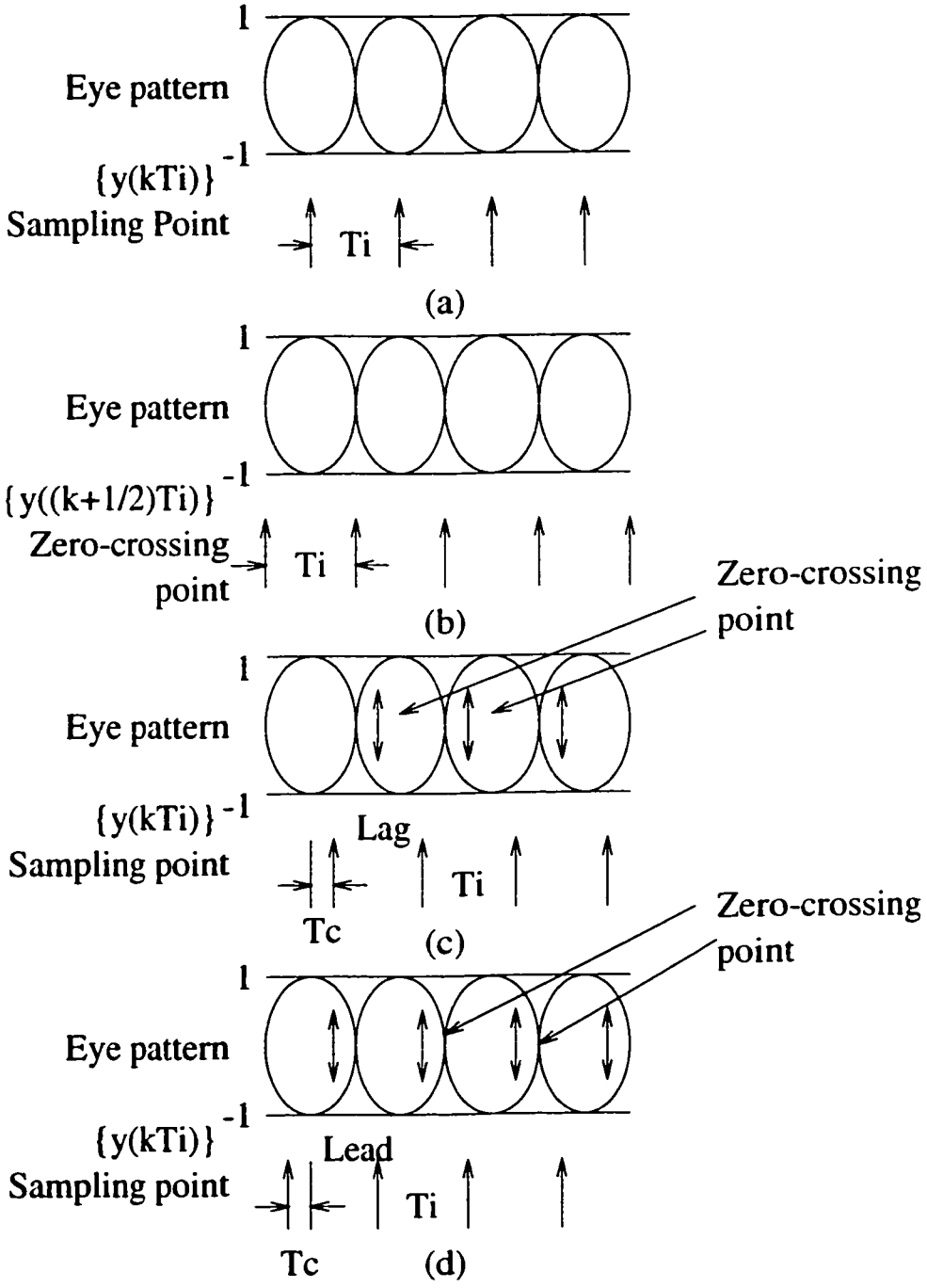

Figure 5.4: **Procedures for detecting clock timing error**

and 5.6.

In general, the symbol clock on the receive side has a different phase and frequency, in both the short and the long term, from the clock on the transmit side. This difference is caused by aspects of the satellite link, such as the Doppler shift resulting from the movement of the satellite and the frequency variation in up/down converters. Let the step size of timing control and the output of the timing error detector circuit (Figure 5.4) be T_c and r respectively; the clock timing is controlled by changing the time delay characteristics of $h_I(t)$ in the rate conversion filter according to the value of $T_c r$.

The output data sample in Equation 5.6 is then given by

$$y(kT_i) = \sum_{i=I_1}^{I_2} x\left[(m_k - i)\,T_s\right] h_I\left[(i + \mu_k)\,T_s + \sum_{j=0}^{k-1} T_c r(j)\right] \tag{5.8}$$

The flowcharts for the proposed timing error detectors are shown in Figures 5.5 and 5.6.

These timing error detectors are suitable for both tracking mode and acquisition mode of symbol timing recovery. The TED operates upon two symbol durations. It requires two samples per symbol, one at the decision instant and the other at the nominal zero-crossing time.

5.4 Using RRC Filter instead of Interpolator FIR Filter for Timing Correction

In the traditional timing recovery loops, the sampled data is passed through a matched filter which is a root raised cosine filter in the system considered here, then it is passed through an interpolator which is a FIR filter. The NCO provides the fractional delay (μ) and basepoint index to the interpolator, which in turn provides the approximate value of sample based on μ. Various structures for interpolating filter are presented in [22, 24]. One approach which requires no computation and

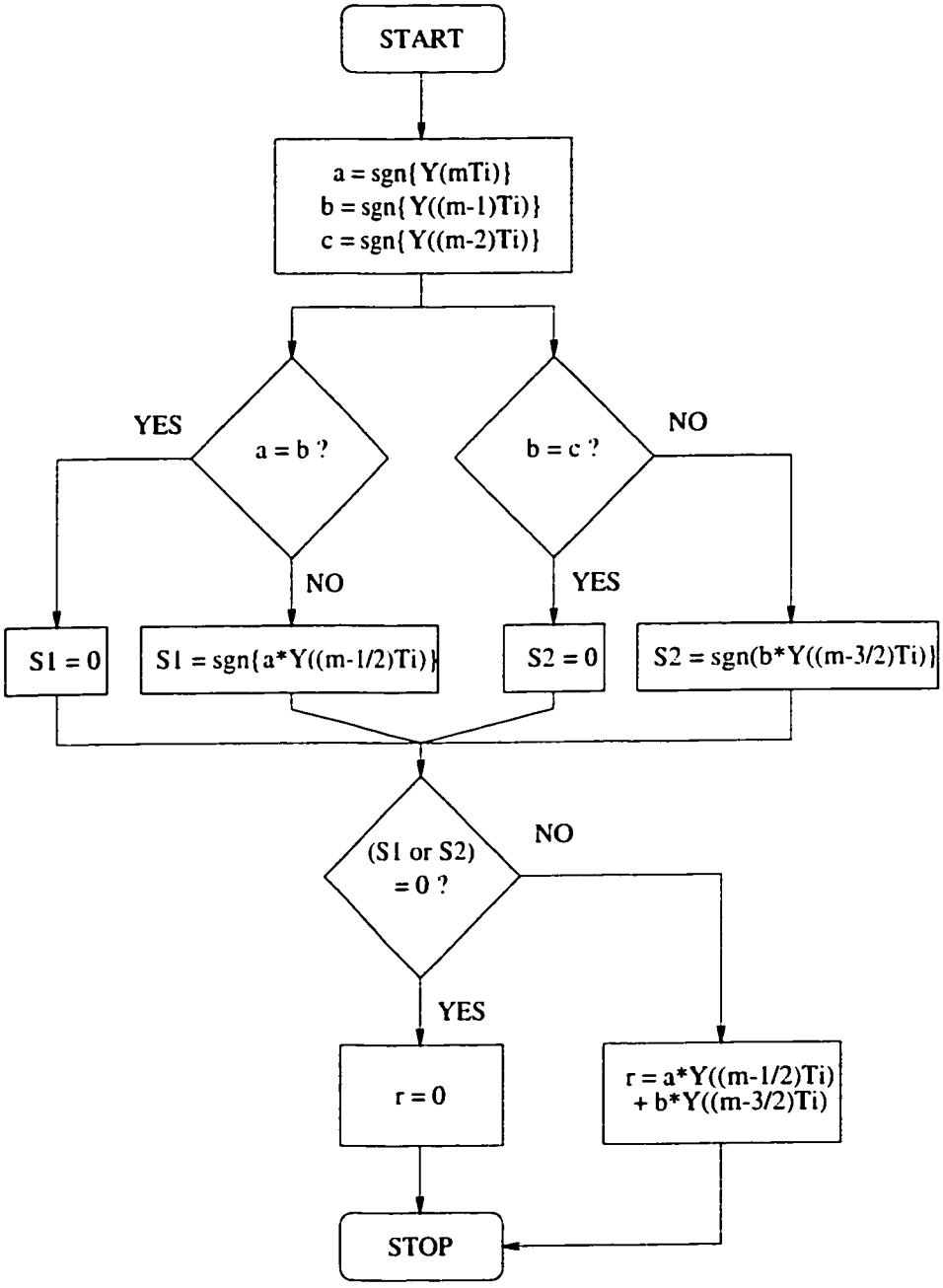

Figure 5.5: **Flow chart GT-MOD-1**

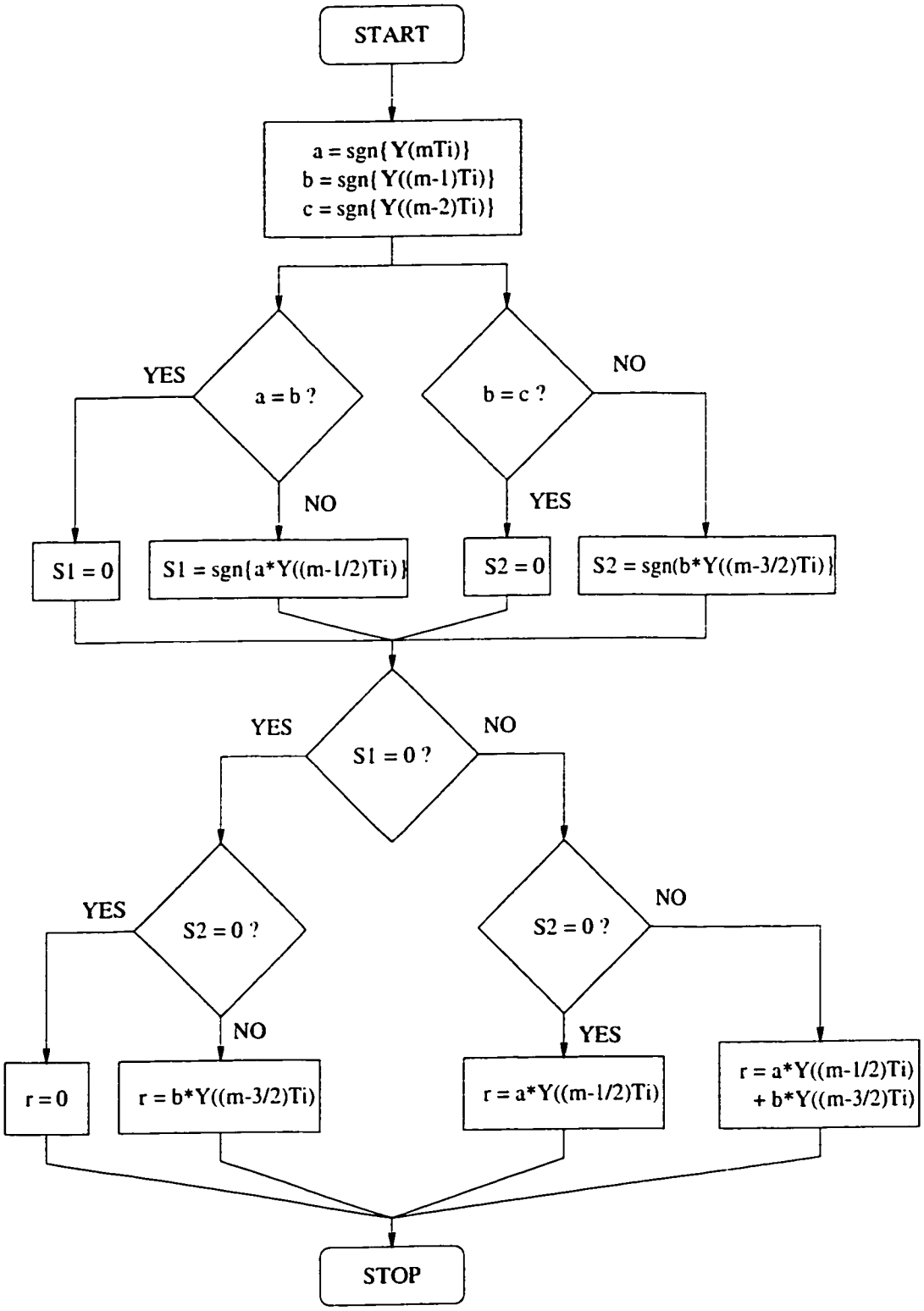

Figure 5.6: **Flow chart GT-MOD-2**

eliminates the need for interpolation is the "stored impulse response" [24]. In [20] it is mentioned that quadratic error of the polynomial interpolator will be larger for the stored FIR filter coefficients. It also states that the error can be made small by increasing the degree of the polynomial. This inturn increases the complexity and computational burden.

A new method is implemented for this research. As discussed, the sampled data is first passed through a matched filter and then through an interpolating FIR filter. To reduce the resources, and to increase the performance of the timing loop, matched filter and interpolator are combined.

5.5 Performance

A series of computer simulation tests have been carried out to study the performance of the proposed symbol timing recovery algorithms in the AWGN channels.

The following parameters were adopted in the simulations:

1. The oversampling factor (N) is 2.
2. The modulation format is QPSK.
3. The filtering impulse response $h(t)$ is a square root raised cosine with excess bandwidth factor *alpha*.

5.5.1 S-Curve : Mean of the Estimated Timing Error

S-Curve is the expectation of error signal (i.e. output of the TED) $e(k)$ for constant timing offset ($\widehat{\tau_k} = \widehat{\tau} = constant$). The curves are plotted for both proposed timing error detectors.

The S-Curve in Figures 5.7 to 5.10 are sinusoidal of period T and pass through the origin at $\delta = 0$. As seen in Figures 5.7 and 5.8, it is evident that its amplitude depends on the roll-off factor. As α decreases, the amplitude of the S-curve becomes

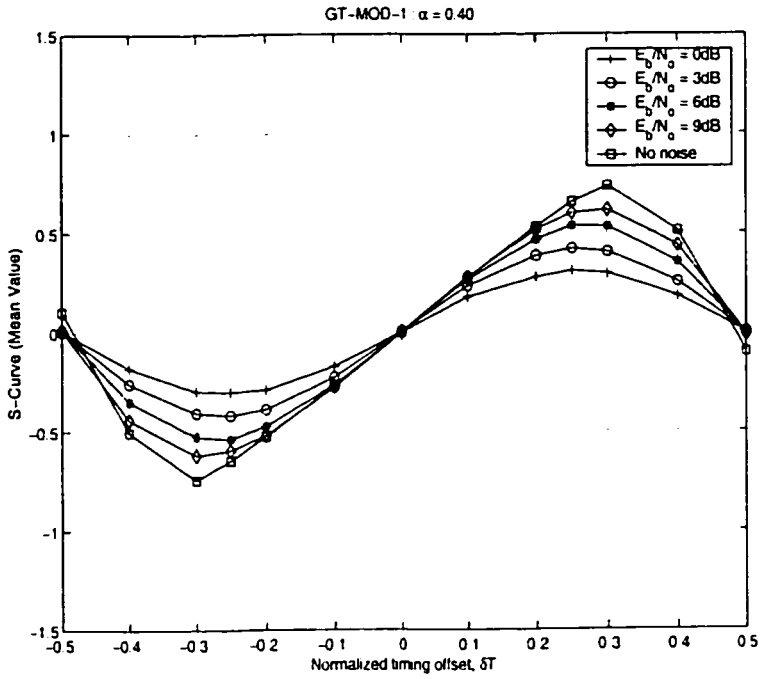

Figure 5.7: **S-Curve for GT-MOD-1 for alpha = 0.40**

smaller and is inadequate for the tracking operation. Thus this may not be suitable for narrowband signaling.

Figures 5.9 and 5.10 illustrate the S-curves for GT-MOD-2 for excess bandwidth of 40% and 70% respectively. It is observed that S-curve for GT-MOD-2 has greater amplitude, in turn the slope of the curves are higher than GT-MOD-1 for same values of α. Thus it can be concluded that GT-MOD-2 is a better choice than GT-MOD-1 for narrowband signaling.

The S-Curve for the Mueller and Mueller Detector [9] with quaternary alphabet (M=4) is of some concern as it exhibits a null for timing errors at about $\pm\frac{T}{3}$ [5]. This null may cause hangup effect if the system starts with errors on that order of magnitude. The situation gets even worse at higher SNR. For E_s/N_o of 23dB, it is seen that the S-Curve with M=4 exhibits spurious lock at about $\pm 0.37T$. A false lock with such large errors could have disabling effects on performance.

The slope of the S-curve is the gain of the detector, the greater the slope

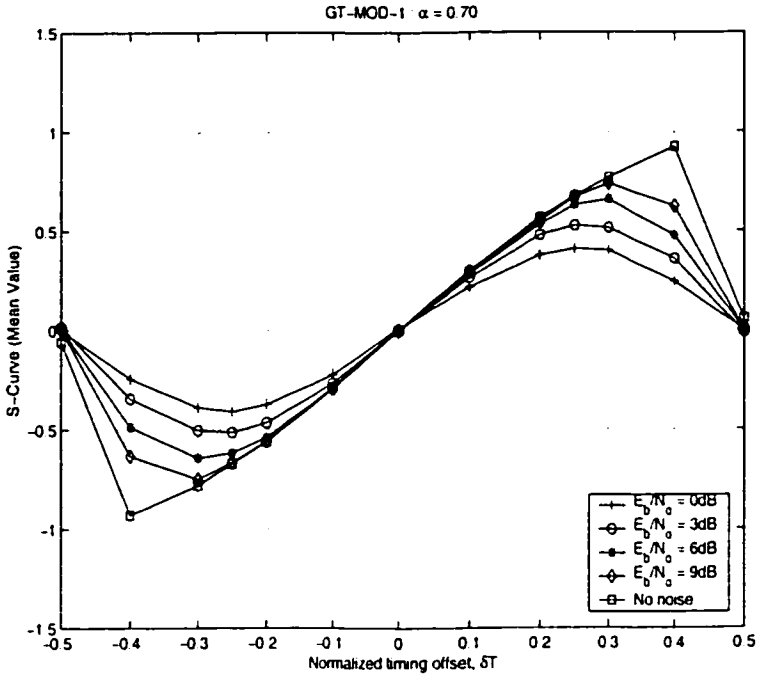

Figure 5.8: **S-Curve for GT-MOD-1 for alpha = 0.70**

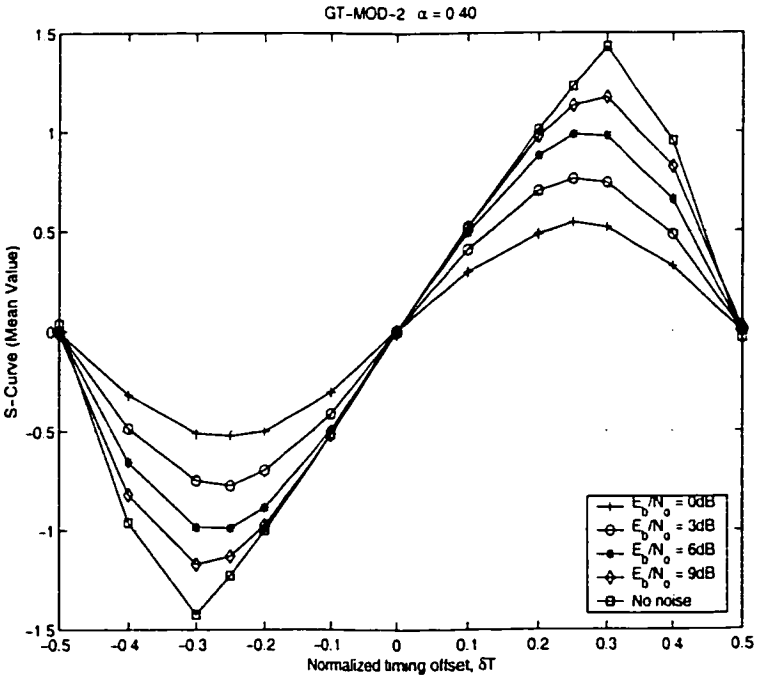

Figure 5.9: **S-Curve for GT-MOD-2 for alpha = 0.40**

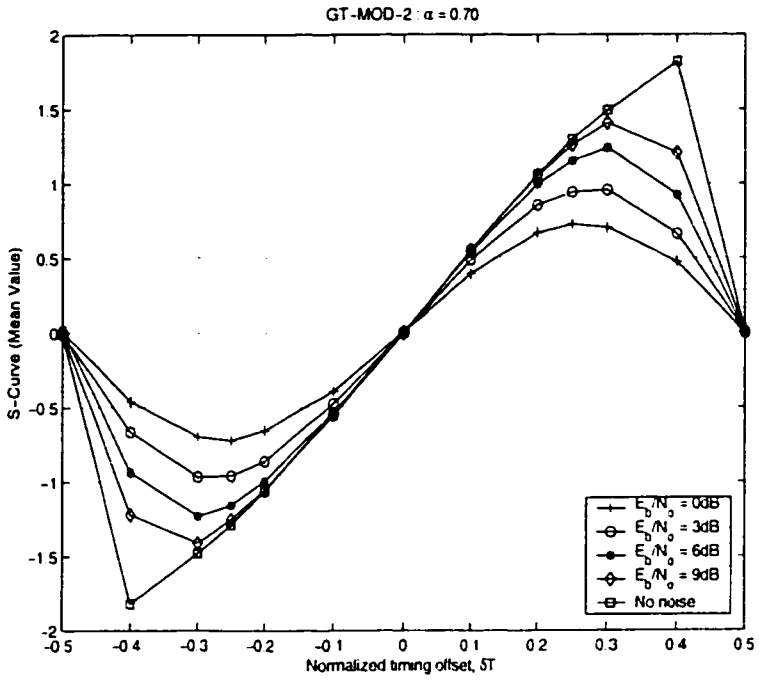

Figure 5.10: **S-Curve for GT-MOD-2 for alpha = 0.70**

the better. The S-curve of Gardner's detector [11] is independent of the SNR, but dependent of the roll-off factor as evident from Figure 4.4. It is observed that with an increase in excess bandwidth value, the detector has a higher slope. In contrast, the slope of Mueller and Muller detector [9] is a function of SNR due to the influence of decision errors [30].

Thus, it is can be seen from Figures 5.7 and 5.8, for a fixed SNR, the slope of the curves varies very slightly. The same holds true for GT-MOD-2 in Figures 5.9 and 5.10. Thus, the proposed techniques are a function of SNR and the slope of S-curve is unaffected by excess bandwidth factor.

5.5.2 Variance of Estimate (or Tracking Performance)

The tracking performance of the proposed synchronizers are assessed in this section. Simulation results are presented for both timing error detectors. Unless otherwise specified, the results for variance of estimate use the following parameters:

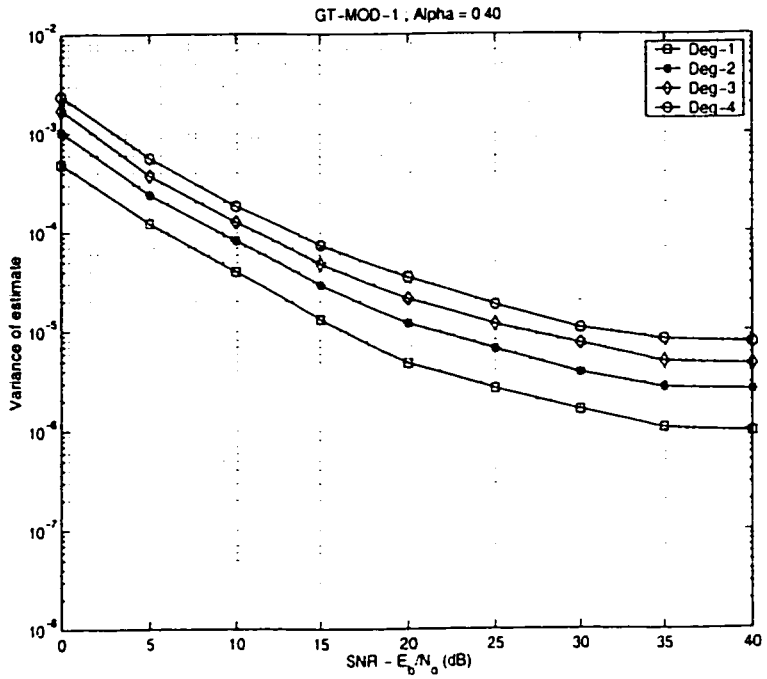

Figure 5.11: **Tracking performance for GT-MOD-1 for alpha = 0.40**

1. Alpha = 0.40 and 0.70

2. Control Step size = 1, 2, 3 and 4 degrees.

Control step size (μ_k) indicates the number of fractional delay filters (Section 2.5.4). If we assume each symbol duration to be 360 degrees, then 4 degree will have 90 fractional delay filters in both directions. Thus for a control step size of 4 degree, a total of 181 filters are stored and used in the simulations. Similarly for a control step size of 2 degree, the number of filters required are 361.

Figure 5.11 and 5.12 illustrate simulation results obtained by using GT-MOD-1. In both figures, control step size is taken as a parameter. In Figure 5.11, the curves exhibit a floor in the estimate, it says that the synchronizer performance cannot be further improved by increasing Eb/No. The floor in the curves is a manifestation of self noise. Figure 5.11 illustrates the result of a small roll-off factor. Infact a small alpha produces a longer channel response and correspondingly, a relatively higher self noise. One more reason for self-noise is basically due to the random nature of

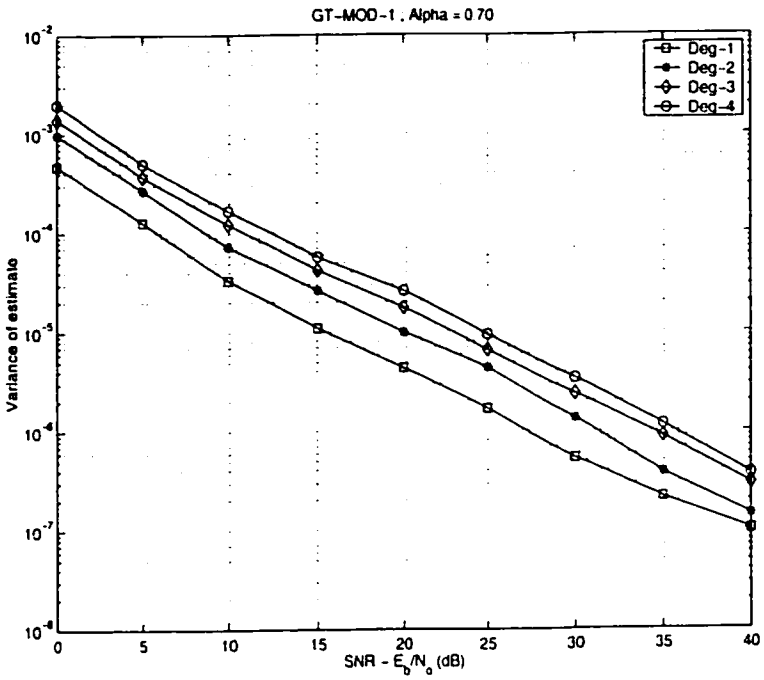

Figure 5.12: **Tracking performance for GT-MOD-1 for alpha = 0.70**

data.

In Figure 5.12, the results are obtained for higher roll-off value. It is observed that the variance of the estimate remains linear even at high SNRs. For large value of alpha, the channel impulse response is smaller and thus relatively smaller self noise.

In Figures 5.11 and 5.12, control step sizes of 1, 2, 3 and 4 degrees are used as a parameter. It is found that as the step size is increased, the synchronizer exhibits more jitter and is much away from the theoretical bound.

In Figure 5.13, a comparison is made by keeping excess bandwidth factor as a parameter for a fixed control step size of degree 1. It is observed that beyond SNR of 35dB, the variance of estimate for low alpha, exhibits a floor.

Figure 5.14 and 5.15 exhibit the performance of GT-MOD-2. Comparing GT-MOD-1 and GT-MOD-2, it can be concluded that the jitter performance of GT-MOD-1 is less when compared to GT-MOD-2. The same explanations are applicable

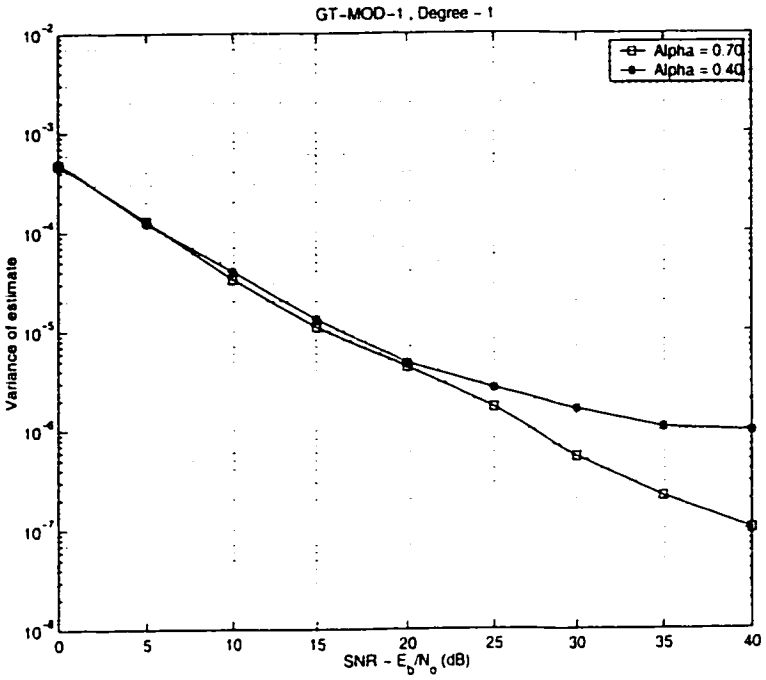

Figure 5.13: **Tracking performance for GT-MOD-1 (Degree = 1)**

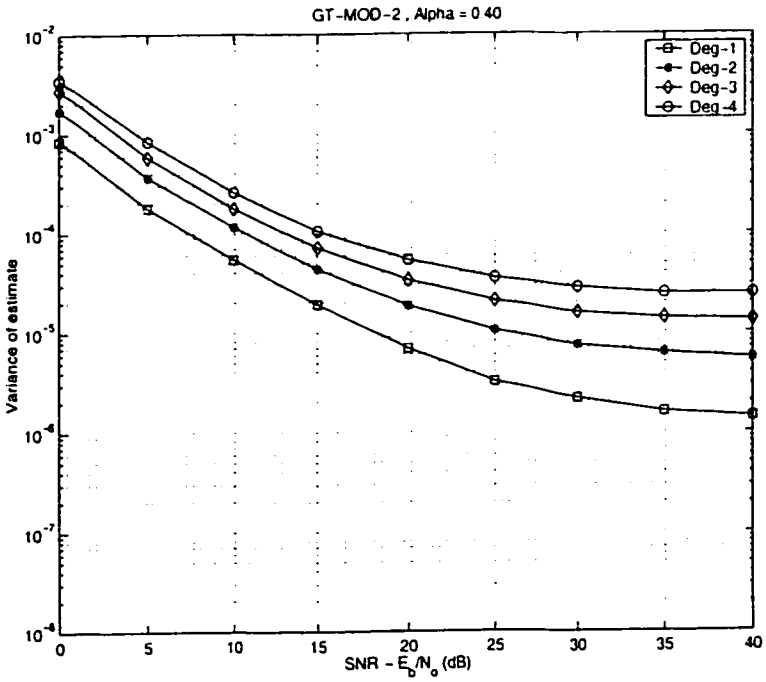

Figure 5.14: **Tracking performance for GT-MOD-2 for alpha = 0.40**

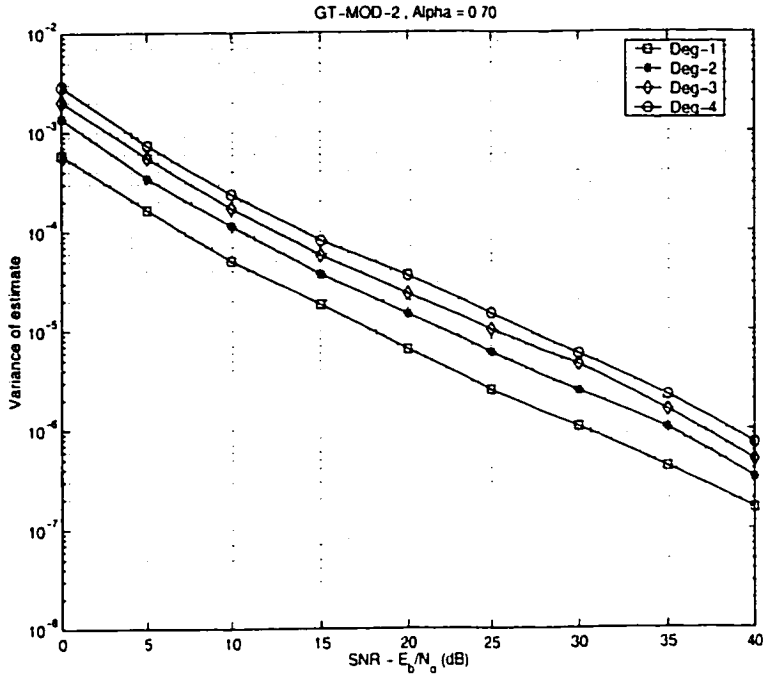

Figure 5.15: **Tracking performance for GT-MOD-2 for alpha = 0.70**

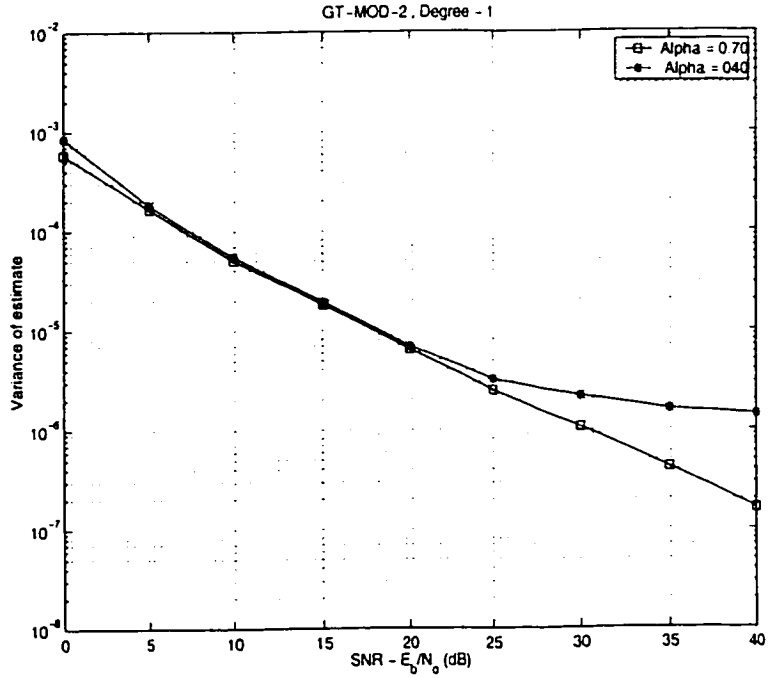

Figure 5.16: **Tracking performance for GT-MOD-2 (Degree = 1)**

to GT-MOD-2.

5.5.3 Acquisition Performance

Acquisition performance or in other words timing error convergence is the time taken by the timing recovery circuit to converge. It is defined as the time required by the loop to sample the signal at the best eye opening. Acquisition performance gives a measurement of time which is taken by the circuit to bring the timing error close to zero. Simulations were conducted by varying the following parameters,

- Alpha - excess bandwidth factor
- Timing offset τ
- Signal to Noise ratio
- Control step size

Figures 5.17 to 5.19 illustrate the timing error convergence for following parameters,

- α - 0.40
- τ - 10% of T (symbol time)
- SNR - 3, 8, 15 dB

Figures 5.17 and 5.18 show the simulation results for control step size of 1 and 4 degree respectively. It is observed that for high SNR, the synchronizer exhibits less jitter. Acquisition time is approximately between 200 and 300 symbols. Secondly, with control step size of degree 4, the synchronizer acquires lock faster but at the cost of tracking performance. In Figure 5.19, the SNR is fixed and control step size is used as the variable. For a control step size of 1 degree, 10% timing offset corresponds to filter number 397 (361 + 10% of 360). Similarly for a step size of 4 degree, 10% offset corresponds to 100 (91 + 10% of 90). It is asserted that for a

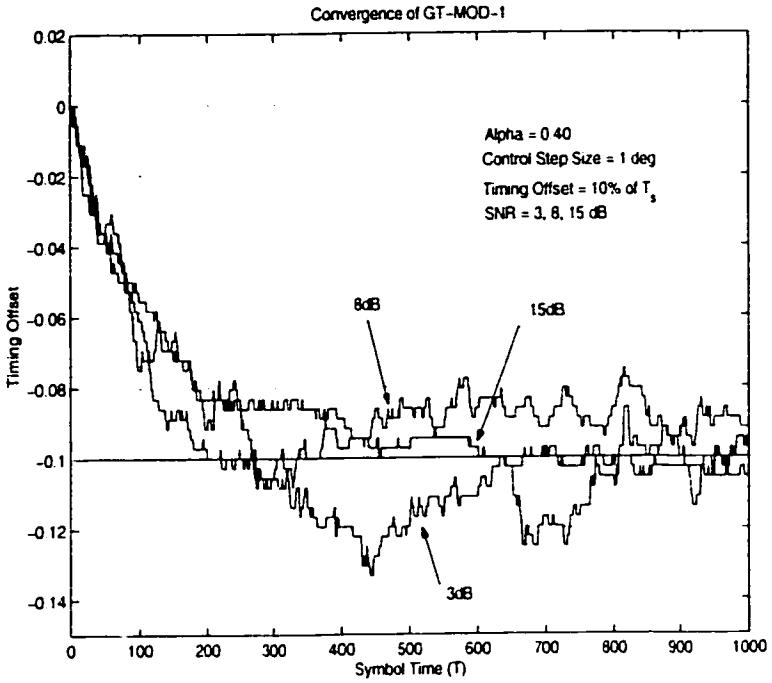

Figure 5.17: **Convergence of GT-MOD-1 for different SNRs (alpha = 0.40 and deg - 1)**

with large control step size, the convergence of loop is faster than a small control step size.

In Figure 5.20, $\alpha = 0.70$ is used and it is noted that due to smaller impulse response, the self-noise is absent which results in faster acquisition even at low SNR.

Figure 5.22 illustrates the acquisition time for random and symmetric data(+1, -1, +1,...). It is seen that the minimum number of symbols required to acquire lock in case of a symmetric data is 100. Similar results for $\alpha = 0.70$ are shown in Figure 5.23

5.5.4 Bit Error Rate

Bit error rate (BER) is defined as the number of bits in errors over the total number of bits transmitted. Figures 5.31 to 5.34 illustrate the BER of the proposed timing error detectors. Simulations were conducted with and without the feedback loop i.e.,

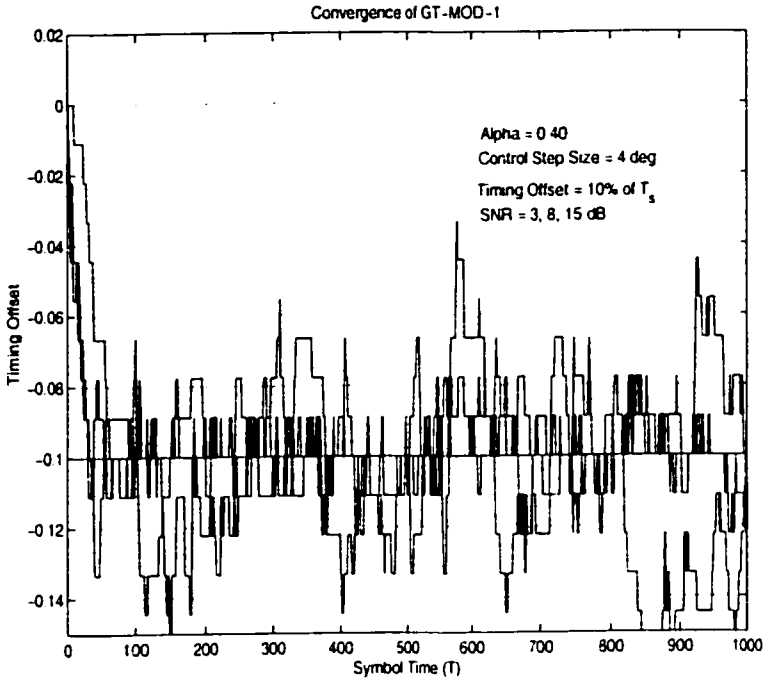

Figure 5.18: **Convergence of GT-MOD-1 for different SNRs (alpha = 0.40 and deg - 4)**

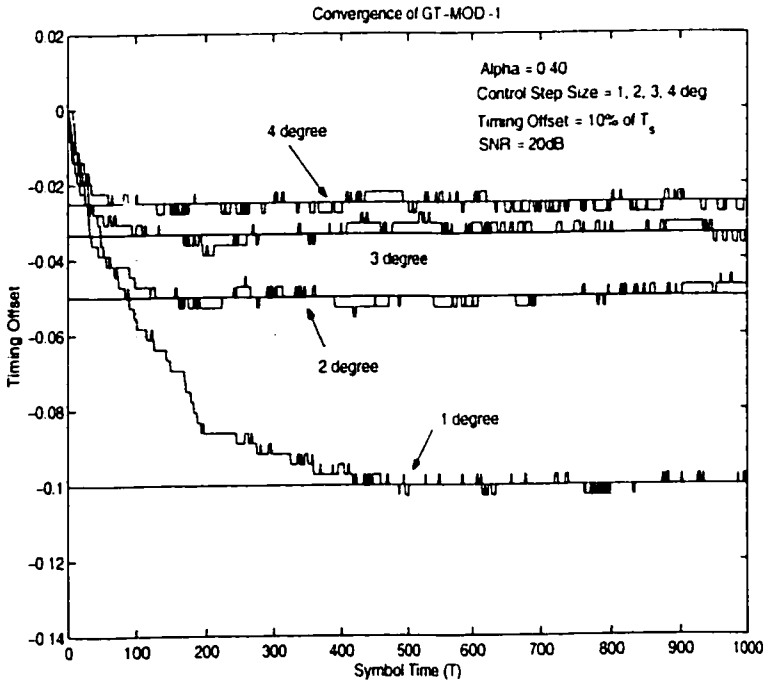

Figure 5.19: **Convergence of GT-MOD-1 for various control step size (alpha = 0.40)**

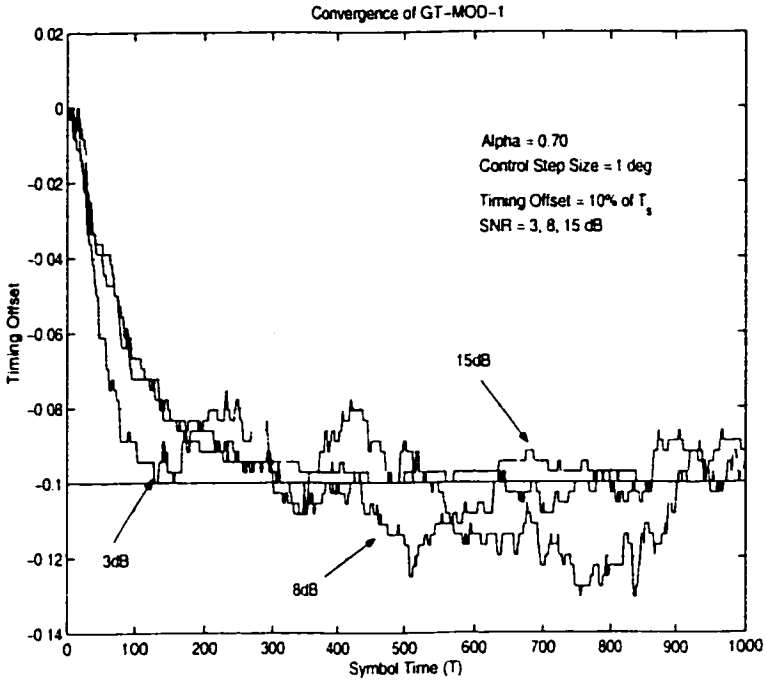

Figure 5.20: **Convergence of GT-MOD-1 for different SNRs (alpha = 0.70 and deg - 1)**

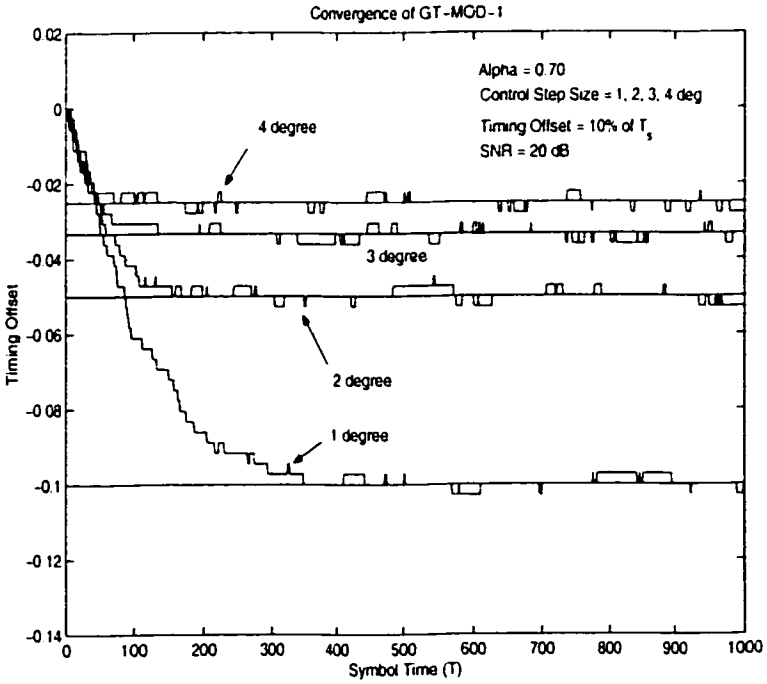

Figure 5.21: **Convergence of GT-MOD-1 for various control step size (alpha = 0.70)**

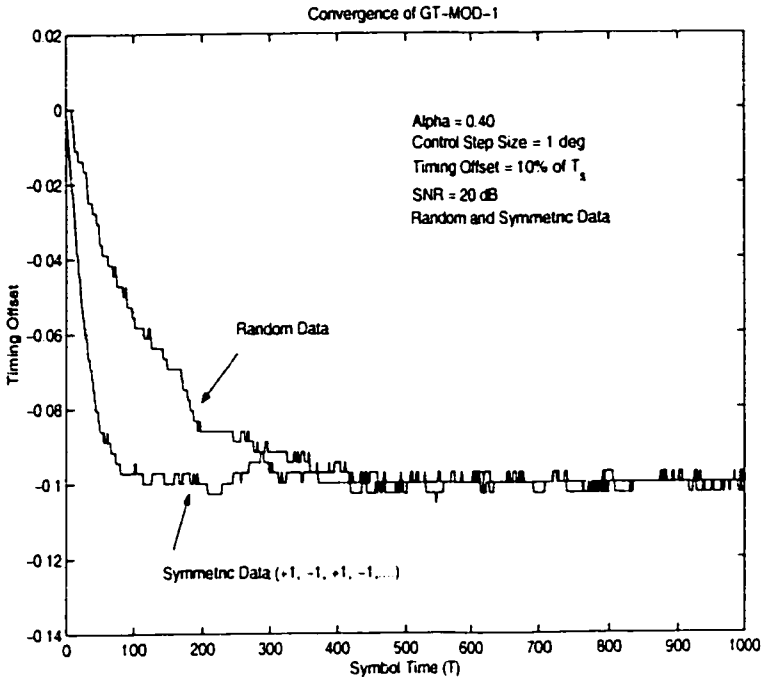

Figure 5.22: **Convergence of GT-MOD-1 for Random and Symmetric data (alpha = 0.40)**

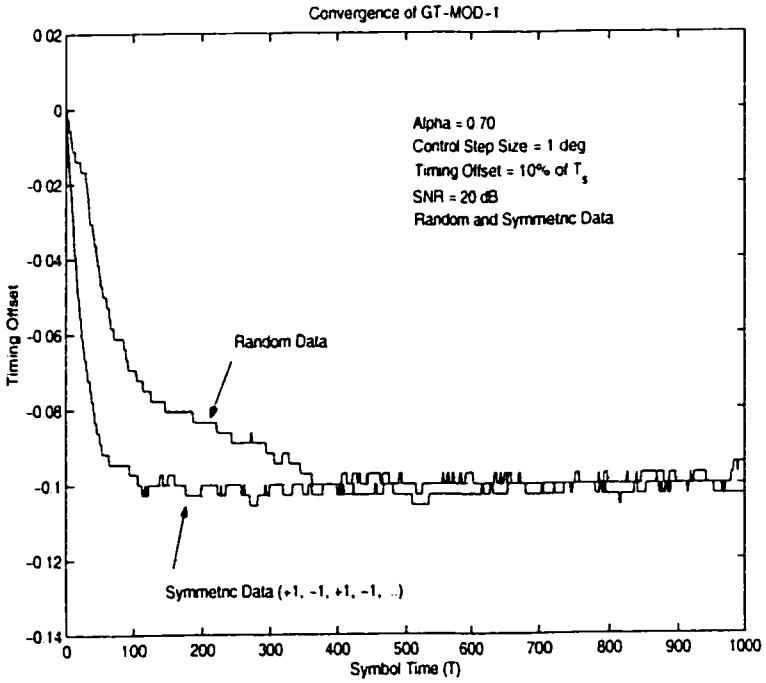

Figure 5.23: **Convergence of GT-MOD-1 for Random and Symmetric data (alpha = 0.70)**

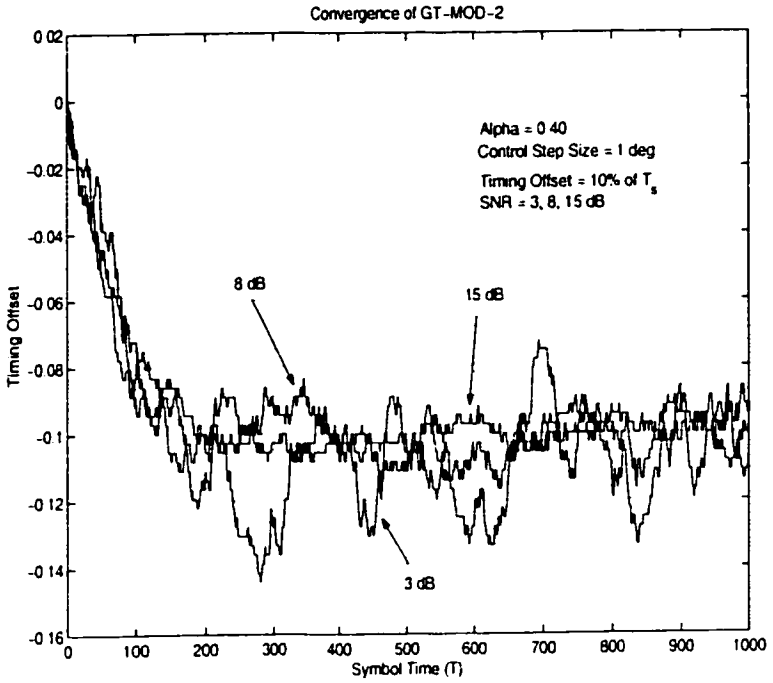

Figure 5.24: **Convergence of GT-MOD-2 for different SNRs (alpha = 0.40 and deg - 1)**

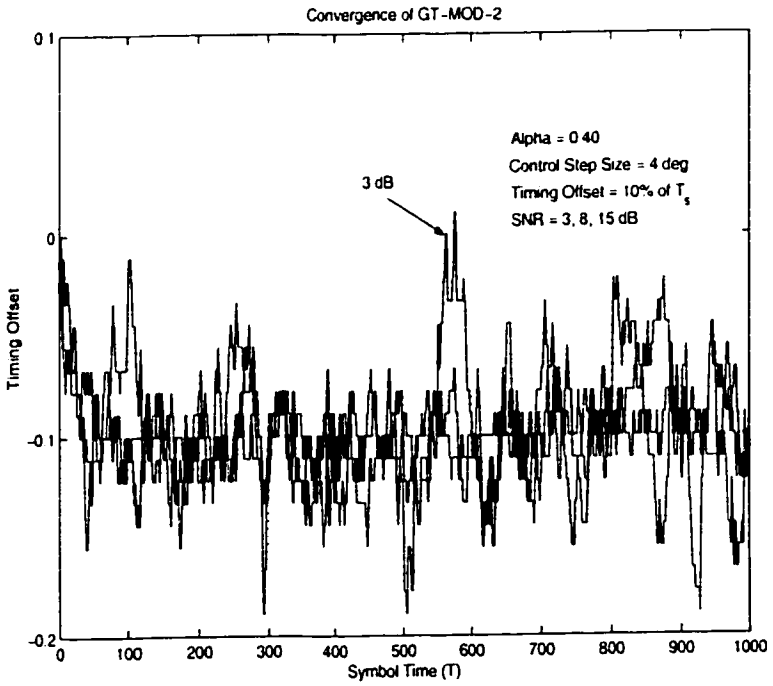

Figure 5.25: **Convergence of GT-MOD-2 for different SNRs (alpha = 0.40 and deg - 4)**

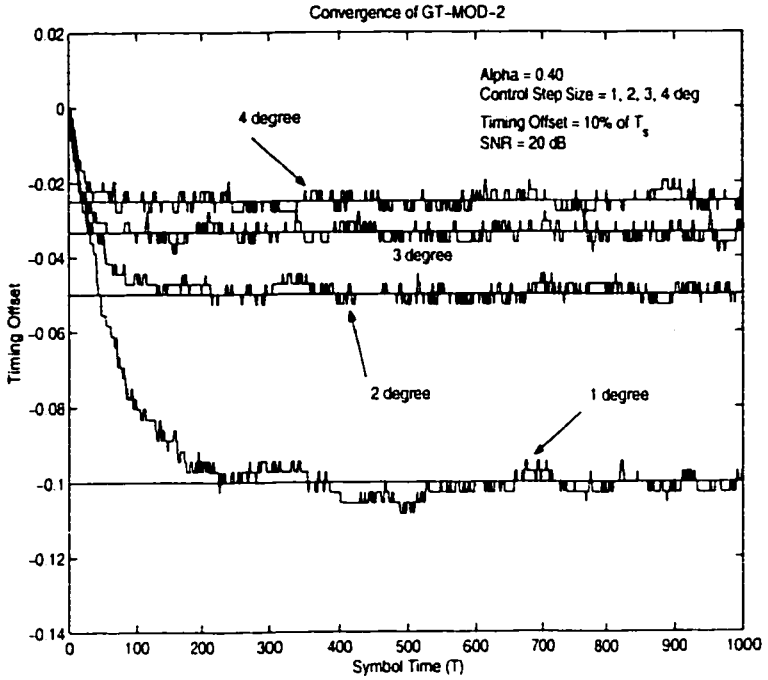

Figure 5.26: **Convergence of GT-MOD-2 for various control step size (alpha = 0.40)**

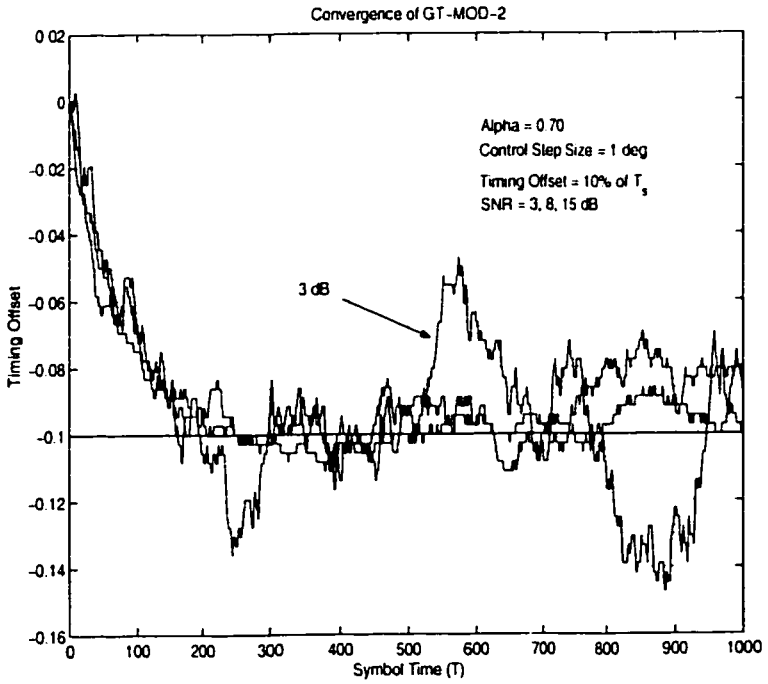

Figure 5.27: **Convergence of GT-MOD-2 for different SNRs (alpha = 0.70 and deg - 1)**

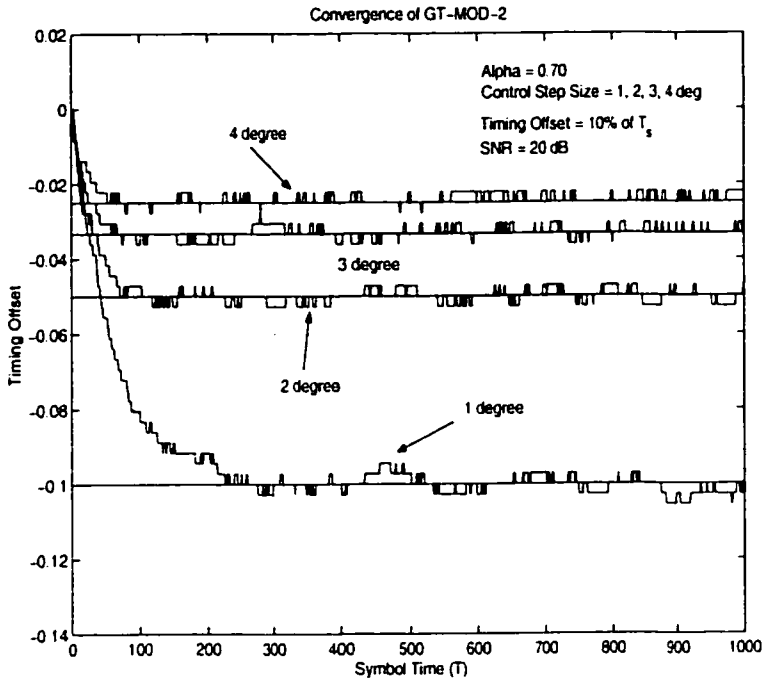

Figure 5.28: **Convergence of GT-MOD-2 for various control step size (alpha = 0.70)**

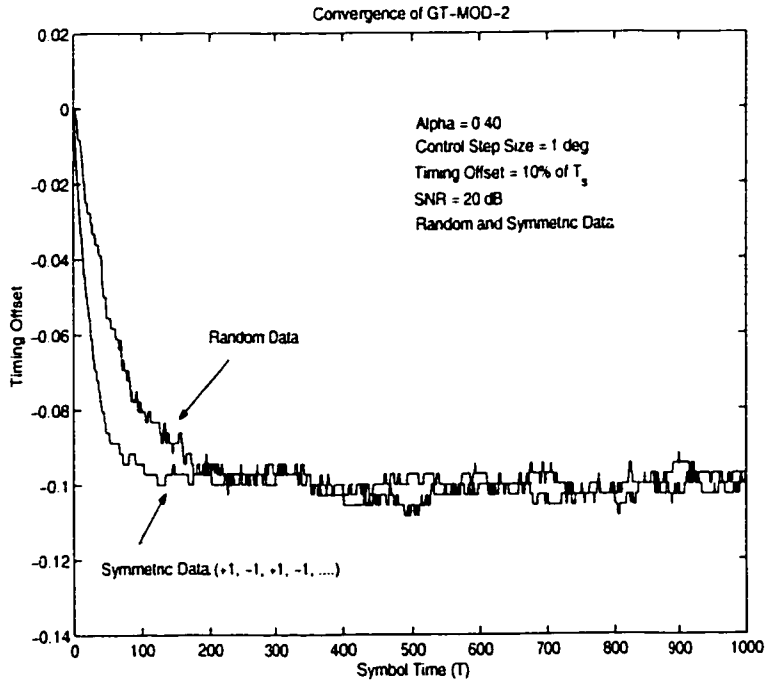

Figure 5.29: **Convergence of GT-MOD-2 for Random and Symmetric data (alpha = 0.40)**

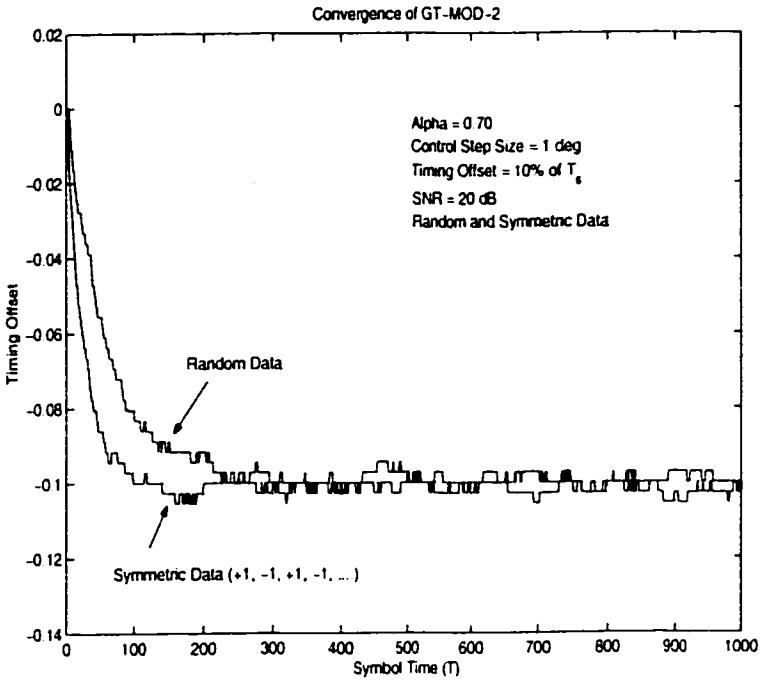

Figure 5.30: **Convergence of GT-MOD-2 for Random and Symmetric data (alpha = 0.70)**

the timing recovery circuit. A timing offset of 10% of symbol duration was used for simulating the system. Figures 5.31 and 5.32 show the performance of GT-MOD-1 for control step size of 1 and 4 degree. It is seen that the BER of the system lies on the theoretical curve. Similar experiments were carried out for GT-MOD-2 for control step size of 1 & 4 degrees and a timing offset of 10%. The results coincide with the theoretical curve. These experiments validate the proposed structures in terms of BER performance.

5.6 Hardware Implementation Structures and Issues

Most DSP algorithms consist of a combination of four types of functions: delay, addition/subtraction, multiplication and data storage. Thus, suitable architectures

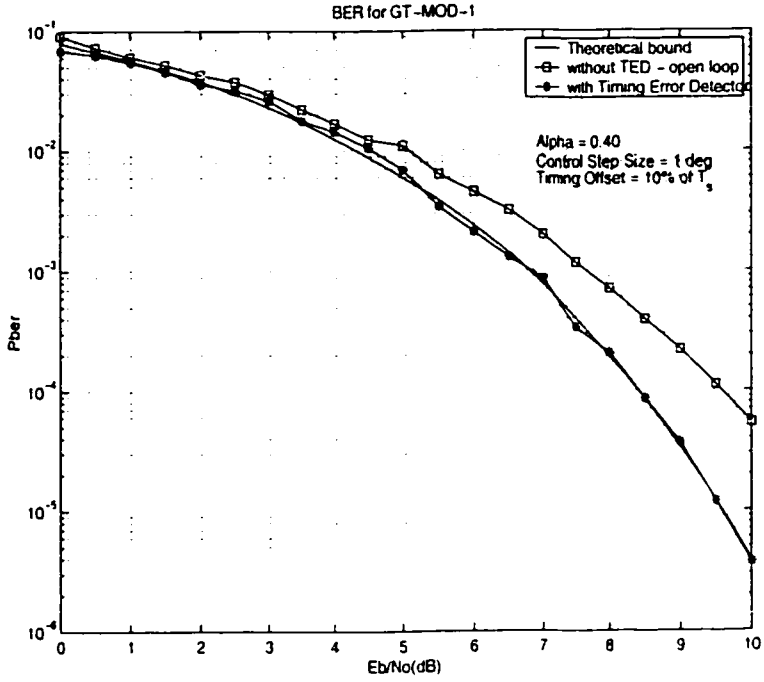

Figure 5.31: **Bit Error Rate for GT-MOD-1 (Degree - 1)**

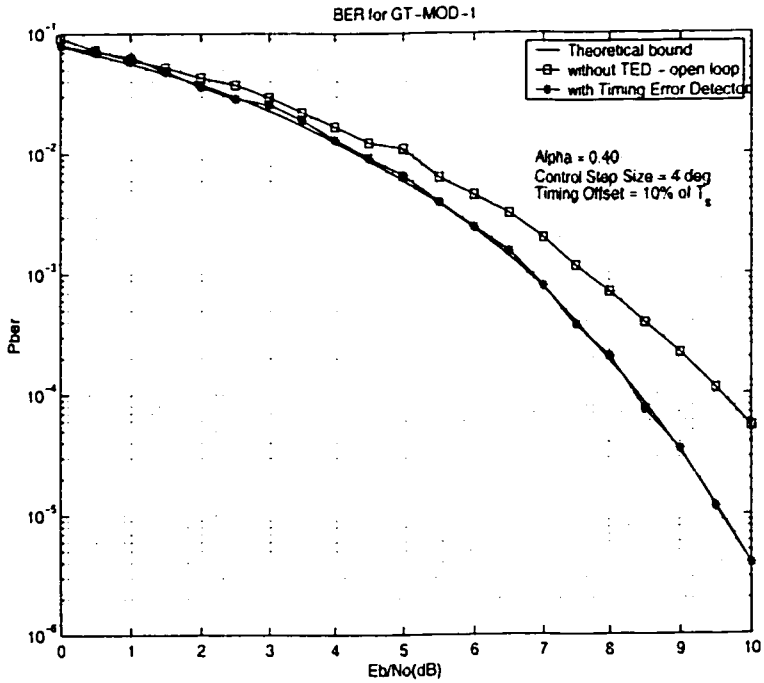

Figure 5.32: **Bit Error Rate for GT-MOD-1 (Degree - 4)**

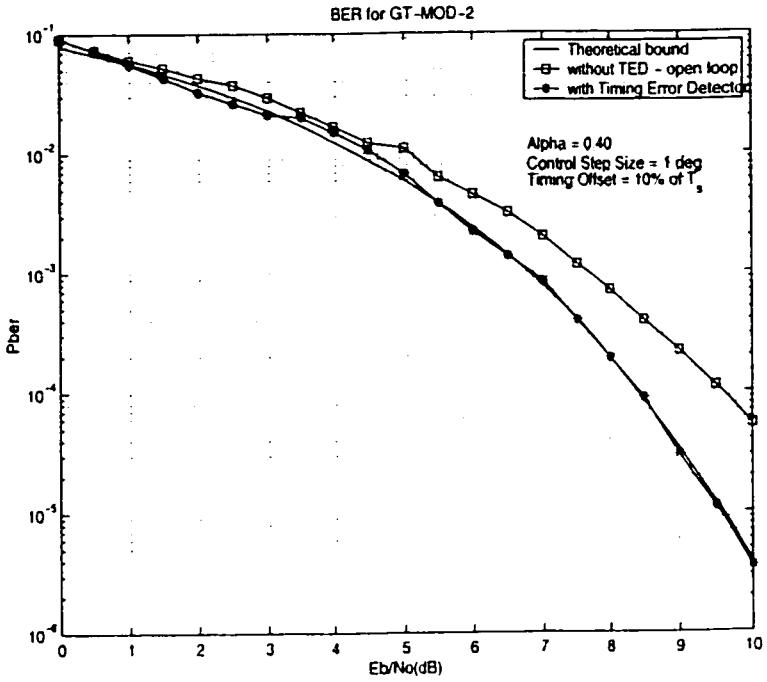

Figure 5.33: **Bit Error Rate for GT-MOD-2 (Degree - 1)**

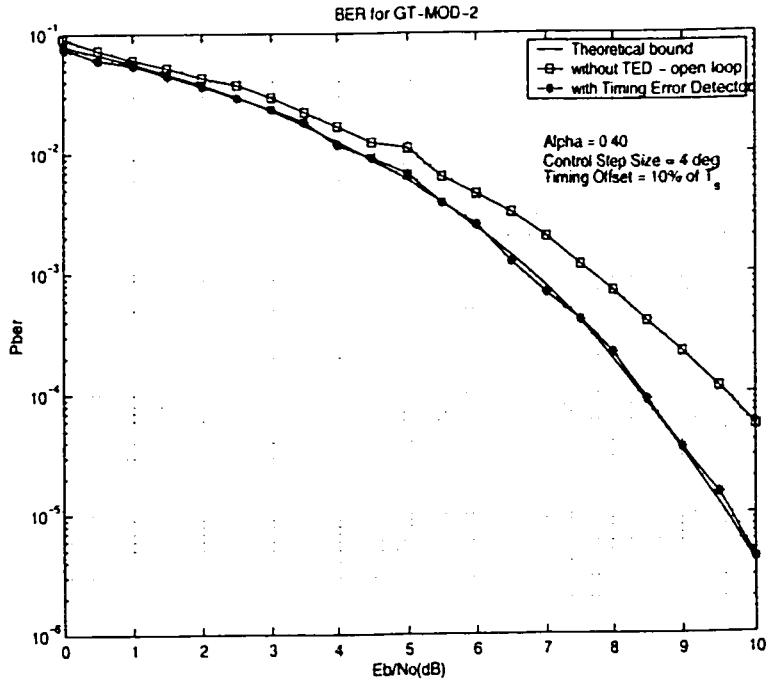

Figure 5.34: **Bit Error Rate for GT-MOD-2 (Degree - 4)**

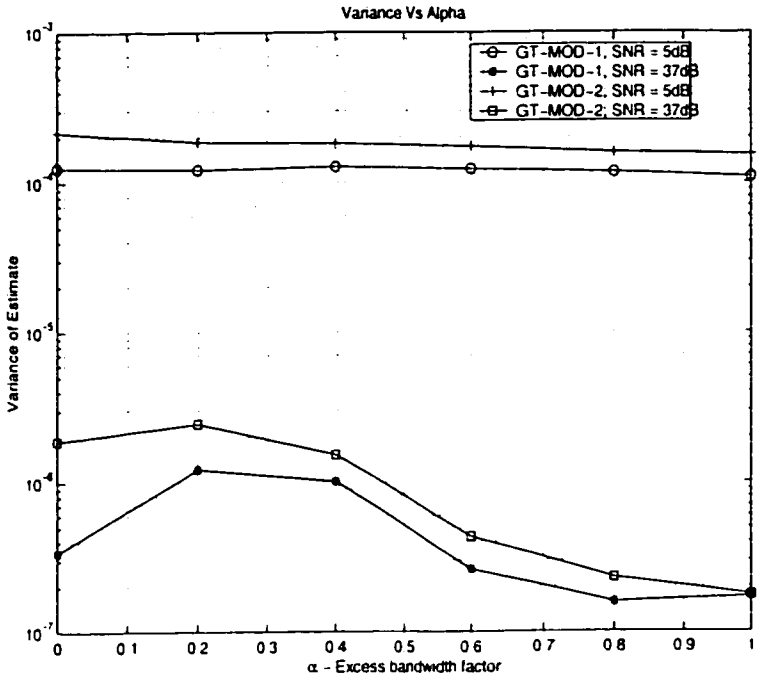

Figure 5.35: **Variance Vs Alpha for GT-MOD-1 and GT-MOD-2**

must be selected to efficiently implement these four operations, as well as delivering the needed capacity and performance required by the application. As multipliers cost more in terms of hardware than adders, the goal of this work is to reduce or eliminate the multipliers and achieve a circuit which is less complex and has comparable performance. Hardware implementation structures for the Gardner's TED are presented. The structures for proposed algorithms are given and it is shown that the proposed structures use less hardware resources when compared to the existing techniques.

5.6.1 Clock Recovery Circuit

5.6.1.1 Gardner's Timing Error Detector

Gardner's TED can be implemented using the structure shown in Figure 5.36. This detector evaluates the error signal based on the real value of the signal.

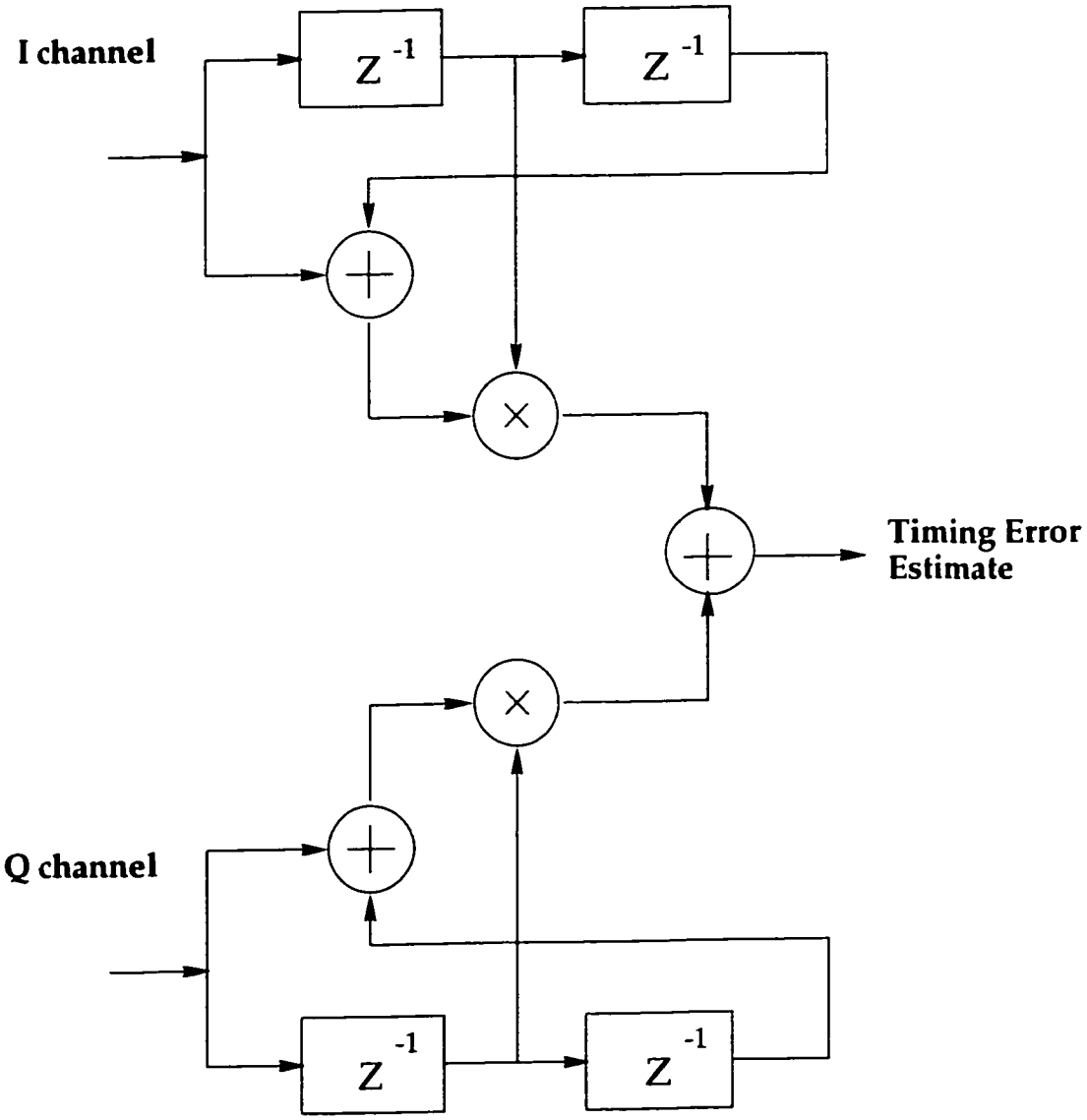

Figure 5.36: **Implementation structure for Gardner's TED**

As seen from the figure, this implementation needs 2 fully functional multipliers(both inputs changing simultaneously), 3 adders and 4 delay elements to evaluate an error signal.

5.6.1.2 Proposed Timing Error Detector

The proposed timing error detector is shown in Figure 5.37. The structure is for GT-MOD-2 and with slight modification can be implemented for GT-MOD-1. It is evident from the figure, that proposed timing error detector requires 3 adders, 8 delay (registers) and couple of logic gates (considering in-phase and quadrature phase channels). Thus the multipliers are eliminated without having any performance degradation.

5.6.2 FIR Filter Implementation

FIR filter is implemented using a pipelined approach (Figure 5.38). FPGA based digital signal processing is based on hardwire logic and allows applications to run in parallel. Pipelined approach does the filtering, correlation and other tasks simultaneously and thus increases the performance. High throughput can be achieved by carrying out operations simultaneously, which can be only done by parallel processing and pipeling. In pipeling, one sub-module accepts and processes the intermediate result of its predecessor which is simultaneously receiving new data to be processed. In order for pipeling to hold, a signal translation from one node to the next must have a delay of atleast one clock cycle. C1, C2, C3 and C4 are the filter coefficients and R(0), R(1), R(2) and R(3) are sequentially stored input data values or taps.

In the case of a fixed coefficient FIR filter, the hardware required for parallelism can be greatly minimized. In such case, multipliers can be replaced by a combination of look-up tables and adders by using the distributed arithmetic technique.

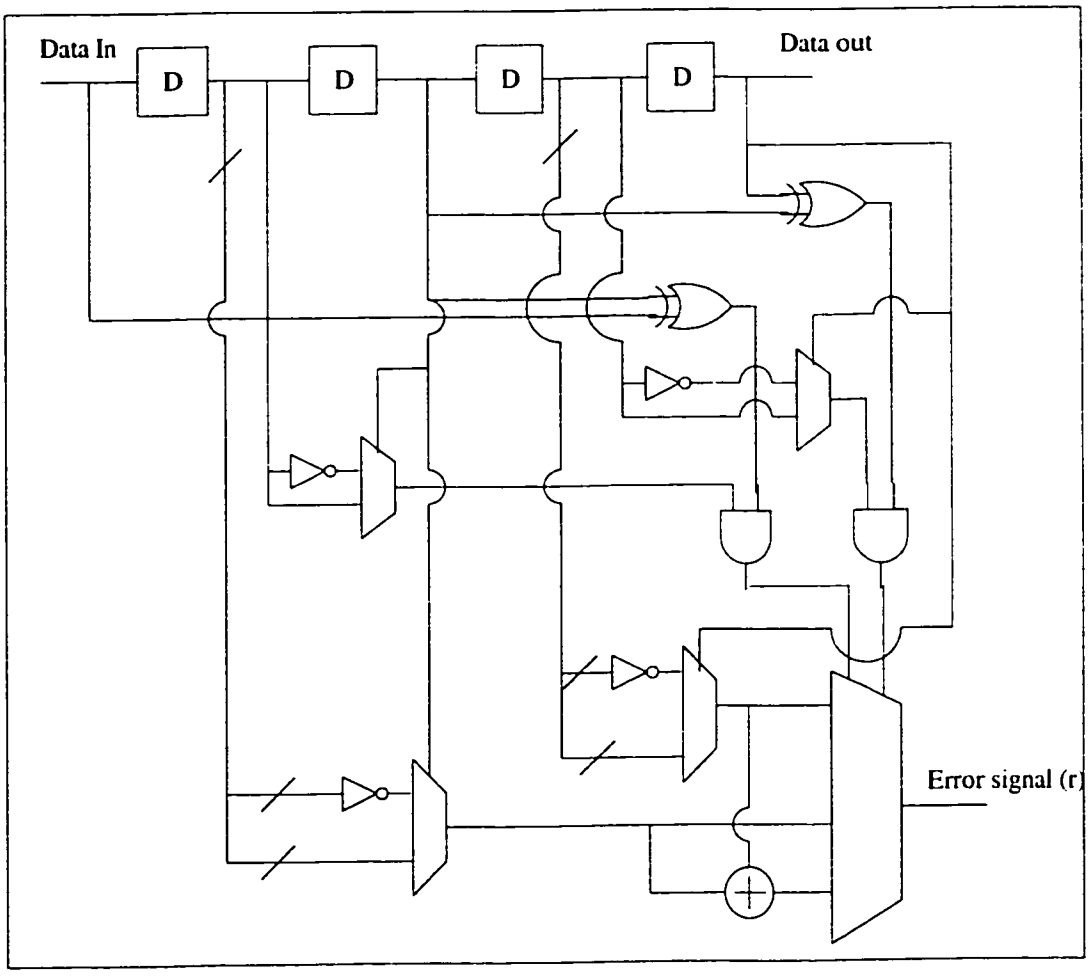

Figure 5.37: **Logic level circuit diagram for GT-MOD-2**

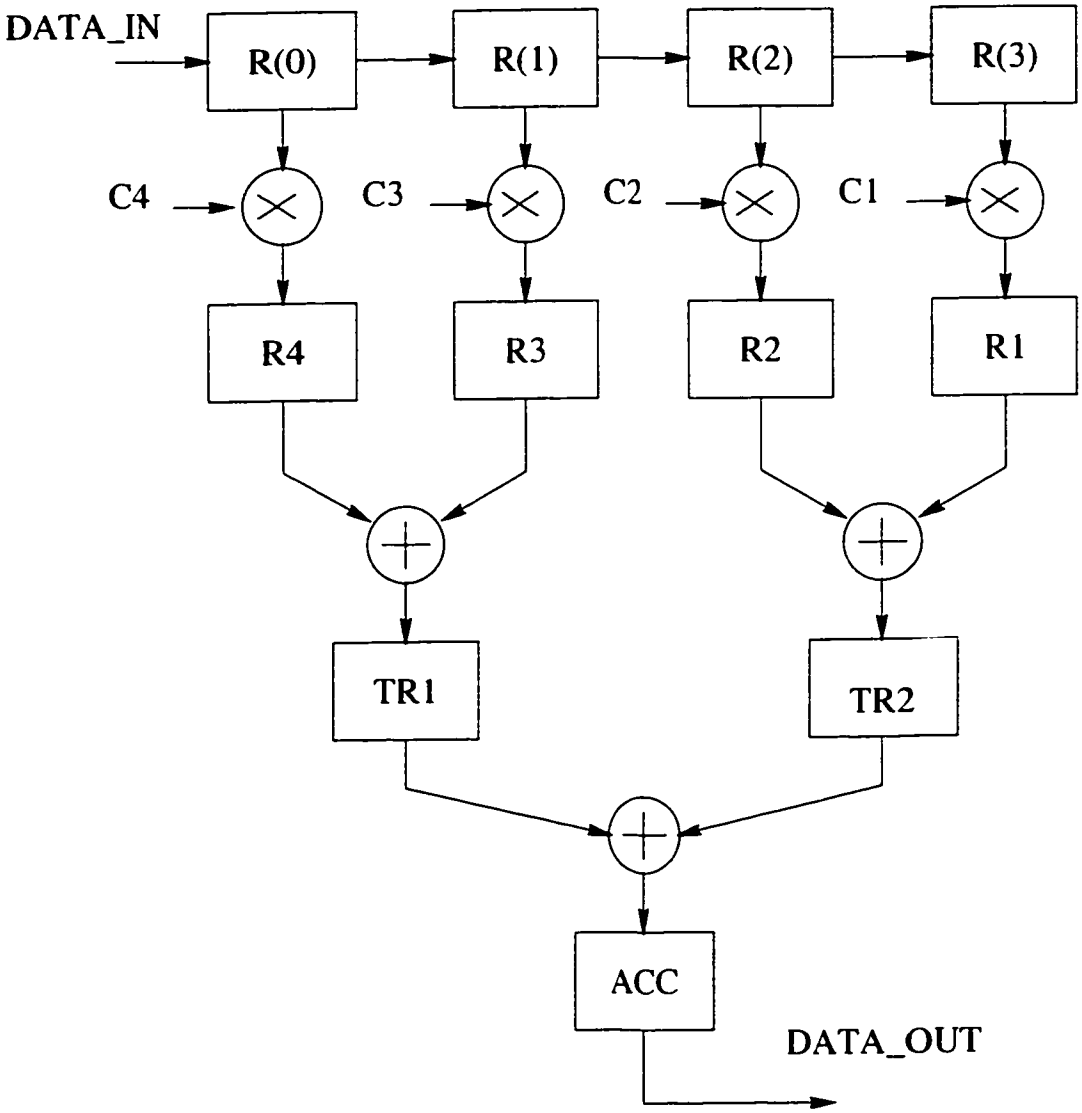

Figure 5.38: **FIR filter implementation using pipelined approach**

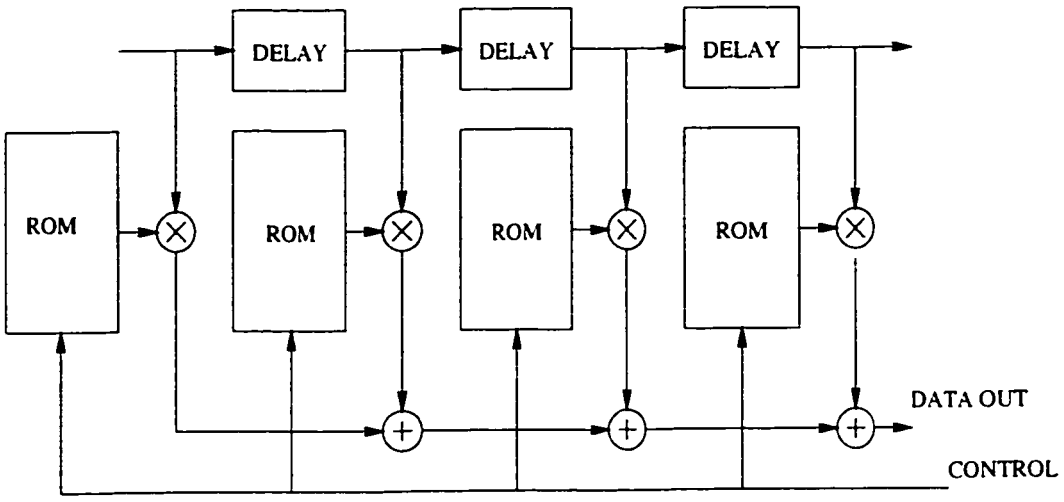

Figure 5.39: **Adaptive FIR filter implementation using ROM**

5.6.2.1 ARC Filter Implementation

Adaptive Rate Conversion(ARC) filter is a digital filter that is capable of self-adjustment in accordance to the input signal. The core of ARC filter is typically a finite impulse response (FIR) filter with coefficients that can be changed on-the-fly. An ARC filter has the ability to update its coefficients. New coefficients are sent to the filter from a coefficient generator. In this design, the coefficient generator is ROM based. Coefficients are precalculated and stored in a ROM. ARC filter updates its coefficients based on the error signal from the timing error detector (TED) and loop filter. This is shown in Figure 5.39.

5.6.3 Loop Filter

The averaging loop filter is a low pass filter, which smoothes out the error signal and produces a control signal. One of the simplest filters from digital implementation point of view, is a first order Infinite Impulse Response (IIR) filter, which is given by,

$$H(z) = \frac{g_2}{1 - g_1 z^{-1}} \tag{5.9}$$

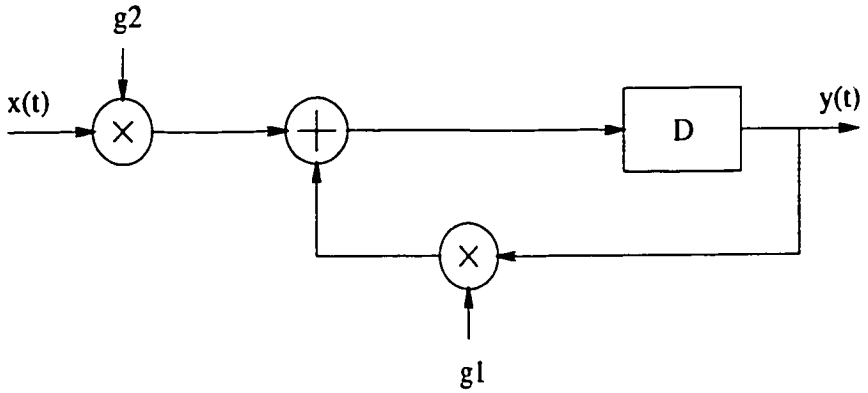

Figure 5.40: **Loop filter**

A discrete time representation of this IIR filter is written as

$$y(t) = g_2 x(t) + g_1 y(t-1) \tag{5.10}$$

Figure 5.40 shows the IIR loop filter structure based on Equation 5.10. This implementation needs only 2 constant multipliers and one adder.

Despite the huge amount of flexibility and functionality that digital signal processing introduces, DSP leads to power consuming implementations. The power resources on-board the satellite are strongly limited and highly expensive. Furthermore, as more functionality is implemented on-board the satellites, the amount of hardware increases. This results in large and expensive satellites. Thus applications of DSP on-board the satellites call for highly cost effective implementations. Cost-efficiency is related to low power consumption and compact hardware designs. This is achievable only through implementations in full custom very large scale integrated (VLSI) circuits. One particular challenge is to make radiation hard VLSI circuits. Other important issues are interconnection and packing of the VLSI circuits. In satellite communication systems it is required that flexibility is implemented in the satellite payloads. This can be provided through configurable hardware designs. But, increased flexibility as well as much functionality drive up the power consumption and the amount of hardware. Hence, there is a trade-off between functionality and flexibility on one side and cost-efficiency on the other.

Chapter 6

Conclusions and Suggestions for Further Research

6.1 Summary and Conclusion

The main objective of this thesis was to investigate the present available symbol timing recovery methods and to propose a new technique having low complexity and fast acquisition features. All techniques are illustrated as an application to the part of on-board processing satellite systems, however, the application of techniques can be easily expanded to other wireless and wireline systems.

In chapter 2, the effect of filtering on the system performance was analyzed. Probability of bit error in satellite receivers due to imperfect symbol timing recovery was studied. Effects of the timing offset on the bit error rate curves was illustrated for the raised cosine channel. The probability of error as a function of the variance of timing estimate was given. Various timing estimators and detectors were also presented. Finally, techniques pertaining to the timing correction were given.

The work in chapter 3 presented symbol timing recovery schemes for feed-forward configuration. Two techniques, one based on the theory of Maximum Likelihood Estimation and the other was non-data aided based on spectral line estimation were presented. These techniques are particularly useful for feed-forward based timing estimators. They are useful when designing burst mode demodulators. The effect of burst length was also studied and it is shown through computer simulations that longer burst have better performance. The variance of timing estimate is close to the Cramer-Rao Lower Bound (CRLB) for large burst lengths. Also it is noted that the timing offset is estimated using FFT structures which require considerable amount of hardware resources in terms of adders, multipliers and delay elements.

In chapter 4 analysis of two existing symbol timing detectors based on feedback structures was performed. The first was the decision-directed technique based on one sample per symbol. This technique is very simple to implement, as the decisions are based on the symbol samples. The main drawback of this scheme is that it exhibits null in the mean of the estimate (s-curve), which is quite dangerous to the system performance. The second technique analyzed was the non-decision directed timing error detector. This technique is based on two samples per symbol. It has a perfect s-curve (mean of the estimate). Both schemes are well suited for the application under consideration.

Chapter 5 develops and analyses a new feedback based symbol timing estimation technique. The technique presented is based on the Gardner's detector [11]. Gardner's timing error detector makes an estimate over two symbols, that is an error signal is given by observing two symbol intervals. In the proposed structures the estimation is increased for 3 symbols. The oversampling factor is maintained at 2. The proposed technique is decision-directed as it takes into account the decision of the symbol rather than the real value. This makes it easier to implement in hardware. Results have been presented in terms of acquisition, tracking performance, s-curve and probability of error. It is observed through simulation that the proposed

algorithms has a fast acquisition, it is three times faster than the non-decision directed timing error estimator and has considerable tracking performance. In terms of VLSI implementation, the proposed structure requires just 3 adders for QPSK modulation format, where as Gardner's detector needs 3 adders and 2 multipliers.

In conclusion, the work presented in this thesis has presented a novel technique for symbol timing recovery in digital modems. An extensive survey of existing techniques for symbol synchronization in digital communications has also been made.

6.2 Suggestions for Further Research

The analysis and results presented in this thesis are restricted to QPSK modulation formats. Considering the use of higher order modulations schemes (for e.g., MPSK and M-QAM) in mobile communications systems, it would be a good idea to evaluate the performance of presented timing error estimators for such systems. This could also lead to new symbol timing recovery structures. Also, the performance analysis of the schemes under mobile channels conditions could lead to more efficient timing recovery schemes for the fading channels.

Timing correction used in this study is based on the ROM based interpolator. Further research could be done to implement efficient interpolation techniques for timing correction.

In order to verify the partial theoretical analysis and the obtained simulation results, the hardware implementation should be pursued and the pratical bit error rate measurements should be made. The effect of quantization of the signal on the performance of the new algorithm has not been investigated. Further work in this area could provide valuable complexity reductions.

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