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SINGLE PHASE TRAPEZOIDAL AC POWER SUPPLIES FOR HYBRID FIBER/COAX NETWORKS

Neeraj Kaushik

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements
for the Degree of Master of Applied Science at
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ABSTRACT

Single Phase Trapezoidal AC Power Supplies for Hybrid Fiber/ Coax Networks

Neeraj Kaushik

Single phase ac power supplies are used to power hybrid fiber/coax (HFC) networks. These power supplies are required to produce a trapezoidal-shaped voltage waveform. Conventional power supplies having a front-end diode bridge rectifier and a large dc bus capacitor are an unacceptable approach for this application as they draw a highly distorted current waveform resulting in a poor power factor. An intermediate boost stage is used to waveshape the input current thus providing power factor correction. Owing to the additional power conversion stage, this topology results in reduced efficiency. In this thesis a novel power supply topology is proposed which eliminates the use of the boost stage and the large dc bus capacitor while maintaining high efficiency and good power factor. Three voltage controlled PWM pattern generators namely, Hysteresis, Triangular-carrier and One-cycle technique are identified and implemented for the power supply based on the proposed topology. Performance comparison of the power supply using the three techniques is done based on criteria such as input power factor, input current total harmonic distortion and efficiency. Experimental results on a laboratory prototype confirm the feasibility of the proposed power supply.

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CATV	cable television
DPF	displacement power factor
EMI	electromagnetic interference
mH	milli Henry
MOSFET	metal-oxide semiconductor field-effect transistor
P	proportional
PF	power factor
PI	proportional integral
PWM	pulse width modulation
rms	root mean square
SW	switch
THD	total harmonic distortion
kW	kilo watts
μF	micro farad
pu	per unit

C	capacitor, capacitance
C_{dc}	dc bus capacitance
C_o	output filter capacitor
C_{S1}, C_{S2}	high frequency capacitor
D	duty cycle
D_1 *to* D_4	diodes of the bridge rectifier
$f_{sw(max)}$	maximum switching frequency
f_r	dominant frequency
i_i	input current drawn by the power supply
I_1	rms value of fundamental frequency current component
I_s	rms value of the total current
I_o	output load current
I_{diode}	diode current
k_S	voltage sensor gain
k_r	measure of harmonic content of the input at dominant frequency
L	inductor, inductance
LC	second-order output filter
L_o	output filter inductor
L_{S1}	input high frequency inductor
L_S	input source inductance
P_o	output power

R_S	input source resistance
S_1, S_2, S_3, S_4	switches of the full-bridge inverter
SW_{rect}	switching function of the rectifier
SW_{inv}	switching function of the inverter
t_{on}	on-time of the switch
T_{sw}	switching time period
T_i	integrator time constant
V_H	hysteresis boundary voltage level
v_{int}	output voltage of the integrator
v_{ref}	reference voltage
v_m	modulated voltage
v_e	error voltage
V_F	feedback voltage
v_{carr}	carrier voltage waveform
v_{inv}	inverter output voltage
$v_{i\text{-}min}$	minimum input voltage
$v_{i\text{-}max}$	maximum input voltage

CHAPTER 1

INTRODUCTION

1.1 General

The cable-TV (CATV), consumer electronics and telecommunication industries are now entering the age of technology and business innovation to achieve new digital infrastructures. These infrastructures currently known as 'Information Superhighway', will be capable of providing a platform for a wide range of broadband, multimedia, entertainment, communication and information services. Power electronics is an integral part of these infrastructures and has been challenged to provide cost effective and reliable end-to-end power solutions.

In recent years, hybrid fiber/coax networks have emerged as a preferred approach for distributing multimedia services to the customer [1-2]. An attractive feature of these networks is in the use of coaxial cable for distributing reliable power to the customer [3].

Fig. 1 shows a simplified diagram of a hybrid fiber/coax network. The headend typically serves a large area or a city. Bringing fiber optic line to home to provide broadband services is not economical. In the current architecture, video, telephony, audio and broadband signals are brought into a coax node over a fiber optic line. The optical signals are converted into electrical signals in the coax node, and are distributed to the homes using coax cable.

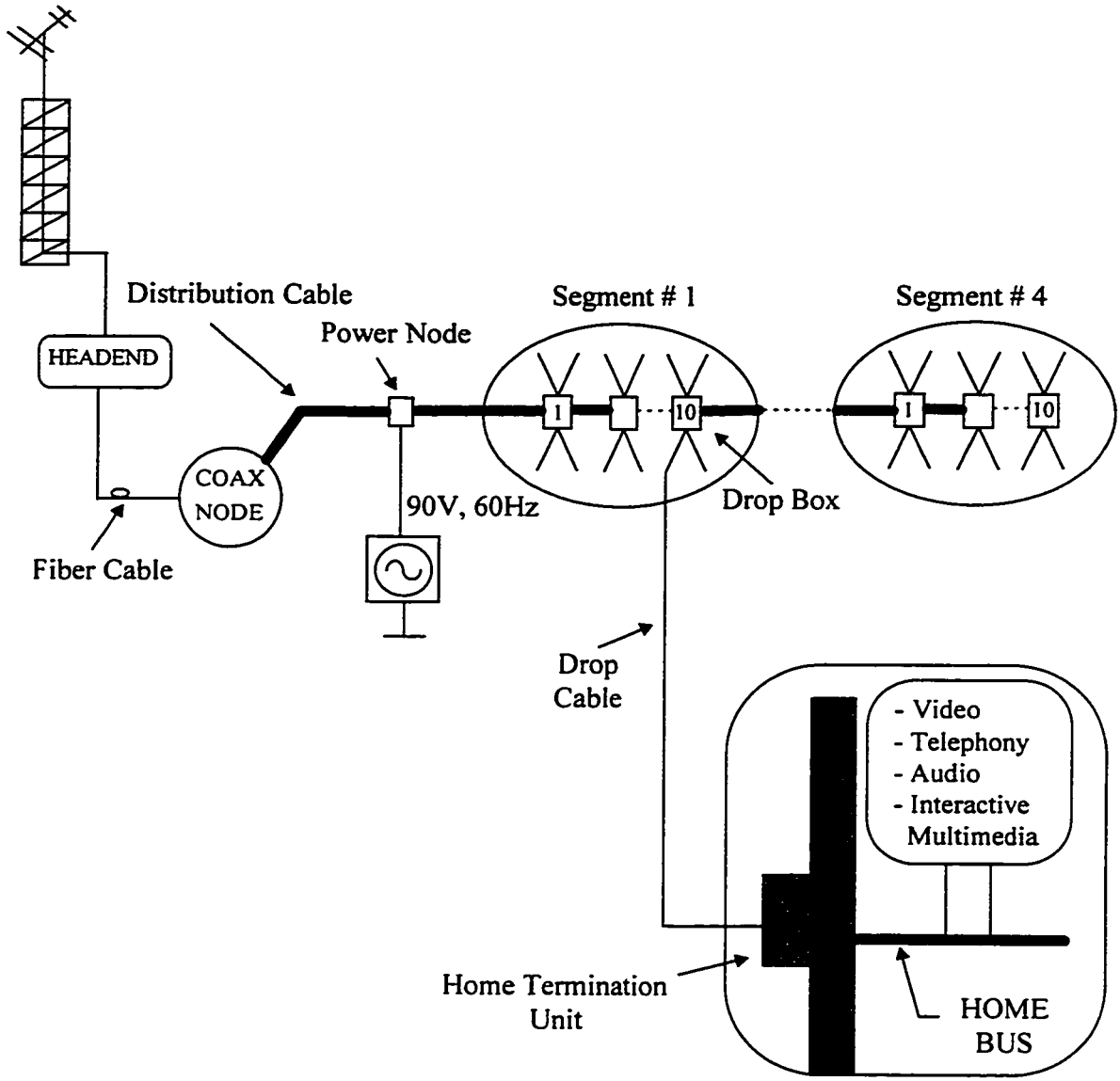


Fig. 1 Hybrid fiber/coax network.

Each headend in the network requires dc power which is obtained locally using ac/dc rectifiers. Powering the residential broadband (hybrid fiber/coax) network requires uninterrupted power to provide reliable telecommunication services [4,5].

Therefore, the requirements imposed for powering the hybrid fiber/coax system are [5]:

(i) Uninterrupted power supply to all network elements

(ii) Safe voltage distribution at the consumer end

(iii) Low installation and maintenance cost

(iv) High efficiency for minimum energy cost

(v) Compatibility with existing network equipments.

Single phase ac power supplies are used to power hybrid fiber/coax networks. Unlike conventional ac/ac power supplies which generate sinusoidal shaped ac output waveform, the power supplies for hybrid fiber/coax networks are required to produce a trapezoidal-shaped waveform. This is based upon the fact that in order to transfer the maximum power to the network equipments at a given peak voltage and to have a low EMI, a trapezoidal waveform is better than a sinusoidal waveform [5].

The voltage level and frequency of network power distribution depends primarily on the following two factors:

(1) Electrical safety of the people, and

(2) Corrosion of distribution cables and connectors.

A good compromise which allows high enough safe voltage and frequency for low distribution power loss and corrosion is 90V at 60Hz [4-7].

Additional requirements of the power supplies include small size, high power factor (ideally 1), low total harmonic distortion (ideally 0) and high efficiency (ideally 100%) [8-10].

1.2 Problem Definition

Conventional single phase ac/ac power supplies distort the utility waveform due to harmonic currents injected into the utility grid and produce electromagnetic interference. Fig. 2 illustrates the problems due to current harmonics in the input current drawn by a power electronic load from the utility source. Due to the finite internal impedance of the utility source, the distortion in the current waveform would result in the distortion of the voltage waveform at the point of common coupling to the other loads. This will cause the other loads to malfunction [8].

The power factor (PF) at which a power electronic load or an equipment such as a power supply operates is the product of the current ratio I_1/I_S and the displacement power factor (DPF):

$$\text{PF} = \frac{\text{real power}}{\text{apparent power}} = \frac{I_1}{I_s} \cdot DPF \tag{1}$$

In (1), the displacement power factor equals the cosine of the angle ϕ_1 by which the fundamental frequency component in the current waveform is displaced with respect to the input voltage waveform. The current ratio I_1/I_S in (1) is the ratio of the rms value of the fundamental frequency current component to the rms value of the total current [9].

It is observed from (1) that the power factor degradation is caused by current waveform distortion and/or phase displacement of the fundamental component of the

current with respect to the voltage. For the case when $I_1/I_S = 1$ (i.e no distortion in the input current), and DPF < 1, only the component of current in phase with the input voltage contributes to the useful power delivered to the load but the total rms current determines the amount of line losses. Also, when the input current waveform is distorted, harmonic currents will be injected in the utility line. These injected harmonics contribute to the total rms current in the line which determines the amount of losses, but do not contribute to the useful power delivered to the load. Thus, both factors causing PF degradation, result in reduced efficiency and poor utilization of the utility source and line capacity [8-9].

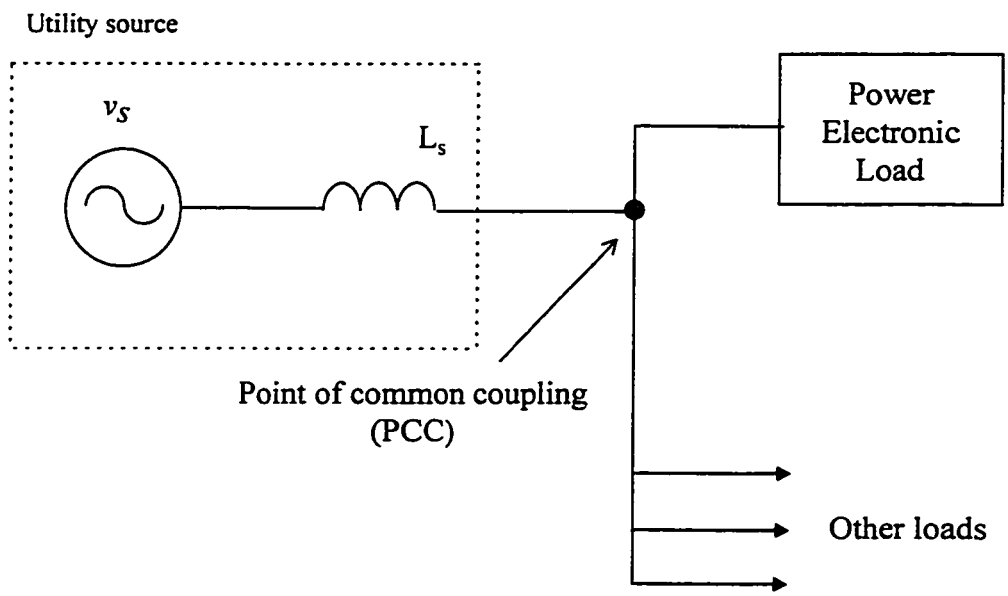


Fig. 2 Utility interface

1.2.1 Conventional regulated ac/ac power supply without power factor correction

A conventional ac power supply structure for such applications, Fig. 3, consists of a front-end diode bridge rectifier, a large dc bus capacitor and a full-bridge PWM inverter. A front end diode bridge rectifier is utilized since it is rugged in nature, requires no external control and thereby reduces the cost in low and medium power applications. In operation, unregulated ripple free dc voltage is applied across the input of the PWM inverter. The PWM inverter converts this unregulated dc voltage into a regulated ac output voltage waveform of the desired shape [12].

In the simplest implementations, conventional open loop feedforward PWM techniques are utilized to control the duty-cycle of the inverter switches and produce the required output voltage [11].

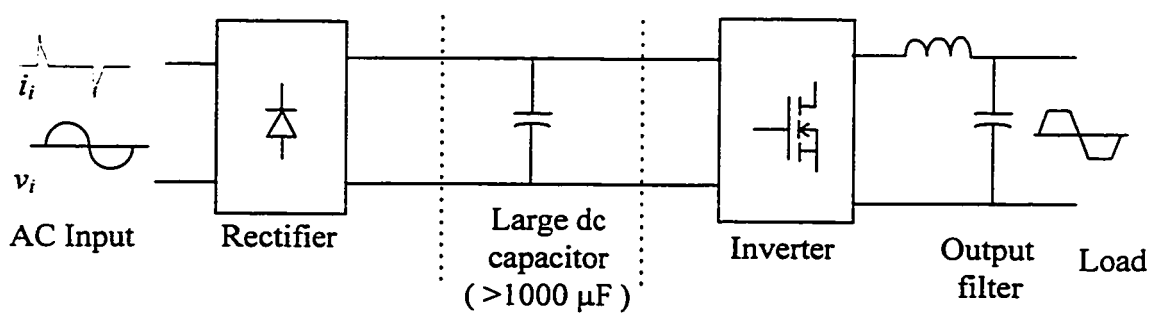


Fig. 3 Conventional regulated ac/ac power supply without power factor correction

Although the conventional topology of Fig. 3 is simple, it has a severe drawback that the current drawn from the utility source is highly distorted and discontinuous, owing to the large capacitor connected at the output of the diode bridge rectifier. This results in very high current harmonics (>100% of the fundamental) in the input current and thus, a poor power factor (typically 0.5-0.6).

High input current distortion results in voltage distortion at the point of common coupling, which may affect other loads. Therefore regulations on power supply distortion have either been introduced, as in the case of IEC 1000-3-2 or recommended, as with the IEEE 519 standard. Power supplies such as the conventional one of Fig. 3 may therefore not meet the new requirements.

Table I shows the relative sizes of the input current harmonics in a typical ac/ac power supply without power factor correction (input voltage = 115 V rms, supply frequency = 60 Hz, having a dc bus capacitor greater than 1500 uF)

TABLE I
Relative sizes of the input current harmonics in a typical ac/ac power supply without power factor correction

Harmonic number	3	5	7	9	11	13	15	17
$\frac{I_h}{I_1}$%	73.2	36.6	8.1	5.7	4.1	2.9	0.8	0.4

There are two different approaches to obtain a high input power factor at the input of these power supplies having a front end diode bridge rectifier [8]. One is by filtering harmonic currents at the interface with the utility. Passive input current waveshaping

methods use this approach. Passive methods have the obvious advantage of simplicity and reliability, but they cannot keep the current waveform independent of the load i.e., the input power factor can be optimized for only a narrow range of operating points [17]. The second approach is by preventing harmonic currents from being generated (or minimizing them). This approach is taken in active input current waveshaping techniques. Active methods provide possibility of using advanced control methods and can make the current waveform independent of the load [18-23].

1.2.2 Conventional regulated ac/ac power supply with power factor correction

The common active method is to place a boost stage between the diode bridge rectifier and the PWM inverter. In this case, Fig. 4, the filtering capacitor is an integral part of the converter and is placed directly across the load.

To make the input power factor equal to unity, the input ac source should see a pure resistance when looking into the input terminals of the diode rectifier. This resistance is emulated by controlling the switch of the boost stage. The converter is so controlled that a sinusoidal current in phase with the input voltage is drawn by the rectifier.

Although power factor correction can be performed by using the buck and buck-boost converter, the most widely used topology for this purpose is the boost converter. A boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the improved input current waveform [9].

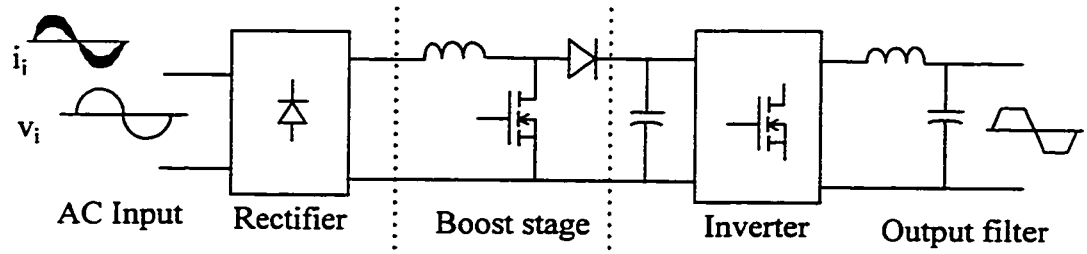


Fig. 4 Conventional regulated ac/ac power supply with power factor correction.

The boost regulator input current must be forced or programmed to be proportional to the input voltage waveform for power factor correction [10].

Fig. 4 shows an acceptable approach to waveshaping the input current. The boost stage forces the dc bus current to follow the waveshape of a full wave rectifier. This results in a sinusoidal input current with low THD (< 3%), with close to unity power factor (> 0.98).

The disadvantages of this type of power factor corrector are: (i) reduced conversion efficiency due to the additional power conversion stage and (ii) increased cost.

1.3 Proposed topology

This thesis presents and analyzes a 60 Hz ac to 60 Hz trapezoidal ac converter topology that requires neither a boost stage nor a large dc capacitor [24-27].

The main features of the proposed topology include: (a) a small dc bus capacitor, the presence of the 120 Hz ripple being exploited in the control scheme; this choice reduces both overall weight and cost; (b) an on-line instantaneous voltage controlled

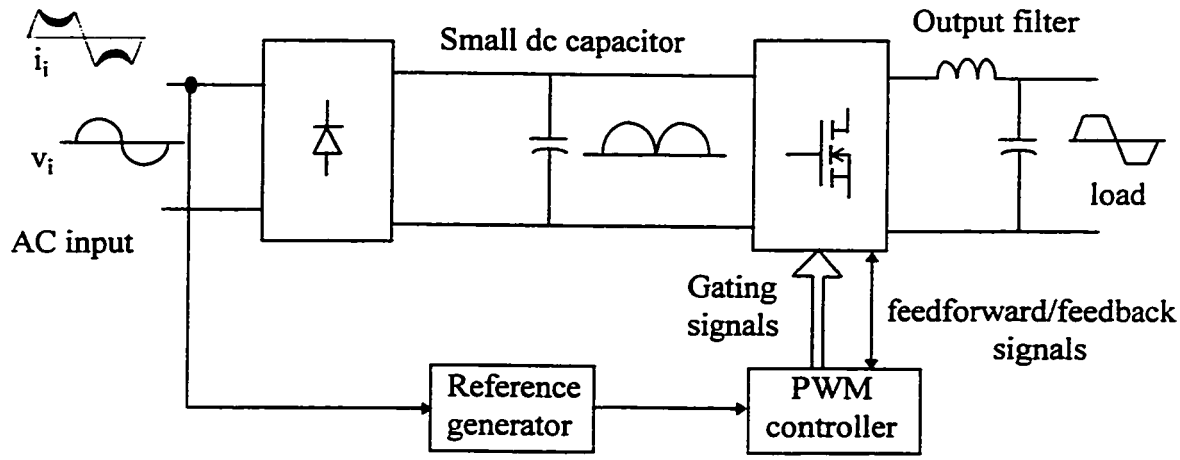


Fig. 5 Proposed power supply topology.

pattern generator synchronized with the dc ripple; this yields an increased dc bus utilization; (c) the input current drawn from the ac source is continuous and the fundamental component is in phase with the voltage; the THD of the input current is low (< 50%) and the resulting power factor is high (>0.9).

1.4 Scope and contribution of this thesis

Single phase sinusoidal ac to trapezoidal ac power supply based on a novel single stage topology is implemented using the three PWM pattern generation and control schemes, namely (a) Hysteresis integral control (b) Triangular-carrier integral control, and (c) One-cycle integral control [25]. The focus of this thesis is on the PWM pattern generation and control schemes required to produce a trapezoidal output voltage for the proposed topology of Fig. 5 and their effect on input power factor and harmonic

distortion. A performance based comparison of these PWM techniques is done on a 900 VA laboratory prototype in terms of power factor (PF), Total Harmonic Distortion (THD) and efficiency (η).

Average switching function analysis [39], which utilizes the concept of transfer function, is used to provide quantitative explanation of power supply waveforms. Furthermore, this analysis also establishes the theoretical limits to power factor and input harmonic distortion of each technique.

Also detailed design procedure for selecting and rating the components of the power supply based on One cycle or Reset integral control technique [38] is described.

The feasibility of the proposed power supply is exhibited and quantified through computer simulation on the PECAN software package [41-42]. Experimental results are obtained on laboratory prototypes comprising of MOSFET-based full bridge PWM inverter topology. The control circuits are designed using state-of-the-art analog and digital devices.

1.5 Outline of the thesis

The contents of the thesis have been organized as follows:

Chapter 2 identifies an output voltage integral duty-cycle control based on which three modified feedforward/ feedback PWM pattern generation and control techniques- Hysteresis integral control, Triangular-carrier integral control and One-cycle integral control are derived. Different modes of the PWM inverter controlled by various techniques are identified.

In Chapter 3 the implementation aspects of the three schemes are discussed. Procedure for selection of parameters is given. A design example illustrates the selection of various power and control circuit components. Key simulation results are shown.

Chapter 4 presents generalized average switching function analysis. It further compares the performance of the three schemes in terms of the effect on input power factor and THD as a function of load, input dc bus capacitor and input line voltage. Experimental results are presented.

Chapter 5 presents design guidelines for the power circuit components of the proposed power supply based on Reset integral PWM control scheme.

Chapter 6 concludes the thesis and identifies some areas for future research work.

CHAPTER 2

PWM PATTERN GENERATOR AND CONTROL TECHNIQUES FOR THE POWER SUPPLY

2.1 Introduction

As discussed in the last chapter, single phase ac power supplies are used to power hybrid/coax cable networks. These power supplies are required to generate 90 V, 60 Hz trapezoidal shaped voltage waveform. An ideal trapezoidal shaped voltage waveform would have sharp rising and falling edges resulting in substantial amount of EMI generation [8]. Alternatively, 60 Hz trapezoidal shaped voltage waveform can be obtained without generating excessive EMI by simply flattening the top and bottom of the curved peaks of a 60 Hz pure sinusoidal waveform. That is, the flatting operation is performed only on the peaks of an otherwise sinusoidal voltage waveform. This type of shaping of the pattern is done using pulse-width-modulation (PWM) [12]. Besides the operation as a voltage controlled PWM pattern generator, these power supplies have to maintain 90 V rms, 60 Hz trapezoidal shaped voltage against all the source voltage and load power variations. Therefore control techniques for these voltage controlled PWM pattern generators have to be developed for the proposed power supply.

The objective of this chapter is to develop the voltage controlled PWM pattern generators and control techniques based on the integral duty cycle control. In this chapter three PWM pattern generators and control techniques- Hysteresis integral PWM control, Triangular-carrier integral PWM control and One-Cycle or Reset integral PWM control are derived and their hardware implementation is presented. Principle of operation of each scheme is explained. Modes of operation of the converter based on the proposed schemes are illustrated. Design details of the control loop and power circuit are discussed in subsequent chapters of the thesis.

2.2 Hysteresis Integral PWM Control Technique

Hysteresis, also known as bang-bang technique, is a widely used control method. This technique is based on the integral duty cycle control. The principle of operation of this PWM generation and control technique is illustrated. The hardware implementation of single phase trapezoidal ac/ac power supply based on this technique is described. Modes of operation of the converter based on this technique are also discussed.

2.2.1 Principle of operation

Hysteresis control is a well known and rugged technique [28-32]. It provides tight regulation of the control variable with a simple comparator circuit. Dynamic response is fast, however switching frequency varies over one cycle as well as with operating conditions [30].

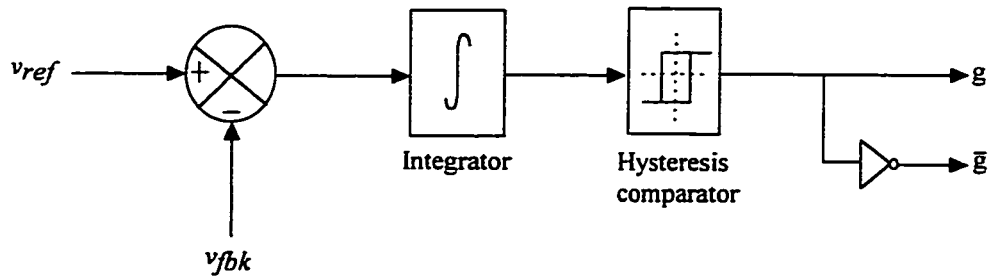


Fig 2.2 Pattern generator based on Hysteresis integral PWM control

In Fig. 2.2, the generalized pattern generator based on hysteresis integral control technique is shown. The output voltage of the converter before the LC filter stage is sensed with a voltage sensor and is fedback. This fedback voltage (v_{fbk}) is compared with the reference voltage signal by an error amplifier. The output of the error amplifier i.e. the error is integrated using a real-time integrator. The integrated error is fed to the comparator circuit which is based on the principle of hysteresis.

2.2.2 Implementation aspects

The implementation of hysteresis control for the proposed topology is illustrated in Fig. 2.3. The purpose of the PWM generator and control circuit is to maintain the average volt-sec of the output voltage over one switching cycle equal to the trapezoidal reference. Therefore the unfiltered instantaneous inverter output voltage pattern is sensed and fedback to be compared to the trapezoidal reference. The error generated due to this comparision is fed to an integrator which improves the tracking of the feedback signal with the reference signal. The controlled voltage (i.e. the average integrated error)

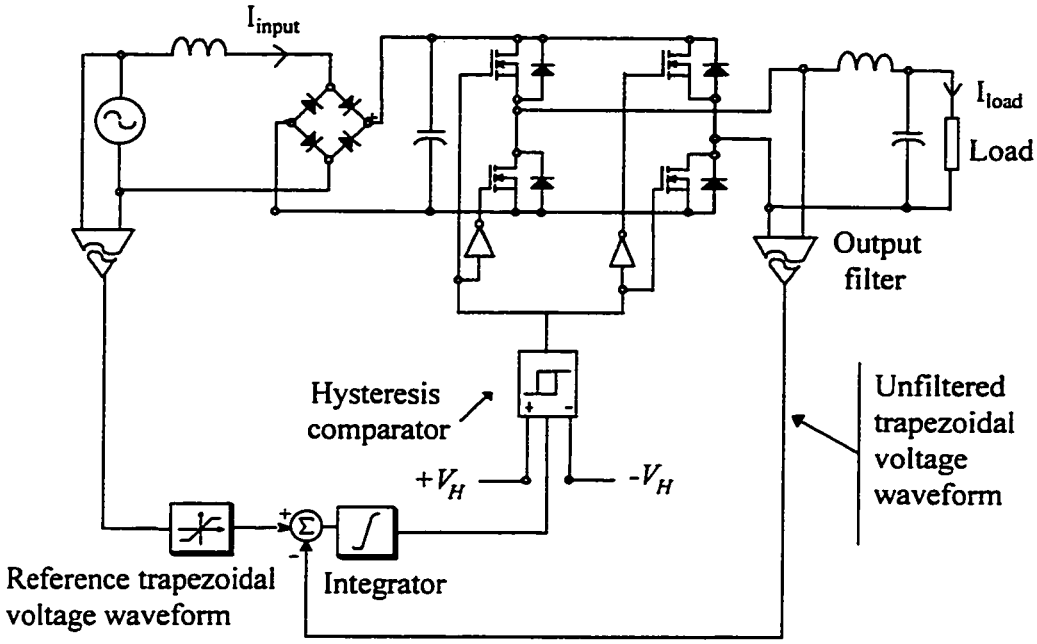


Fig. 2.3 Hysteresis-based PWM controller.

remains within a window, whose size is a design parameter and fixes the maximum ripple of output voltage. Whenever the average error voltage hits one of the top or bottom boundaries, the inverter changes the mode of operation.

2.2.3 Modes of operation

The modes of operation of the PWM inverter illustrated in Fig. 2.4 display the sequence of gating of switches of the inverter controlled by hystersis control. During the positive half of the trapezoidal reference, the switches S_1 and S_3 are gated simultaneously forcing the current to flow in positive direction through the load.

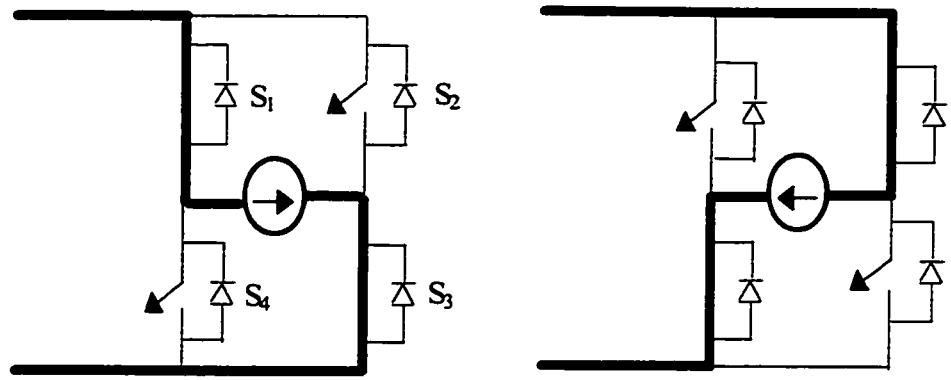


Fig. 2.4 Modes of Operation of the PWM inverter based on the hysteresis integral PWM control. (a) operation of the inverter for positive half-cycle of the trapezoidal reference. (b) operation of the inverter for negative half-cycle of the trapezoidal reference.

During the negative half of the trapezoidal reference, switches S_2 and S_4 are gated simultaneously, forcing the current through the load in opposite direction as shown in Fig. 2.4(b). As it can be observed, all the four switches carry the same rms current.

2.3 Triangular-Carrier Integral Control

This technique [31-35] is also based on the output voltage integral duty cycle control. The principle of operation of this PWM pattern generation and control technique is illustrated. The hardware implementation of single phase trapezoidal ac/ac power supply based on this technique is described. Modes of operation of the converter based on this control technique are also discussed.

2.3.1 Principle of operation

The basic loop is identical to the hysteresis controller, Fig.2.6. However, the switching frequency is stabilized by means of triangular carrier [35]; the integrated error is intersected with the carrier and the intersections define switching instants of the converter. Inverter switching frequency is constant and equal to the carrier frequency. Since this is the case, design is simpler than that of the hysteresis controller.

In Fig. 2.6, the generalized pattern generator based on triangular-carrier integral control technique is shown. The reference voltage is compared with the feedback voltage by an error amplifier. The error generated is integrated using a real-time integrator.

This integrated error or the modulating waveform is superimposed or compared with a triangular carrier waveform. When the modulating waveform is equal to the carrier waveform, switching occurs i.e. the intersections of the two waveforms generates the gating signals. The frequency of the carrier decides the switching frequency of the inverter.

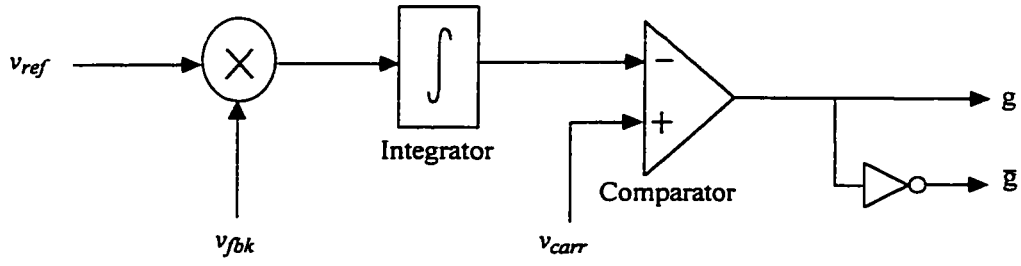


Fig. 2.5 Pattern generator based on Triangular-carrier integral PWM control.

2.3.2 Implementation aspects

The implementation of triangular-carrier integral control for the proposed topology is illustrated in Fig. 2.5. The purpose of the PWM generator and control circuit is to maintain the average volt-sec of the output voltage over one switching cycle to the trapezoidal reference. Therefore the instantaneous inverter output voltage pattern (unfiltered) is sensed and fedback. This fedback signal is compared to the trapezoidal reference. The error generated is fed to an integrator which improves the tracking of the feedback signal with the reference signal. This integrated error or the modulated waveform is further stabilized with a triangular carrier waveform. The output of the comparator i.e. the gating signals are fed to the top and the bottom switches of the left leg of the PWM inverter. The intregrated error is inverted and then compared with the carrier waveform, the gating signals generated in such a way are fed to the top and bottom switches of the right leg of the inverter.

2.3.3 Modes of operation

The modes of operation of the PWM inverter illustrated in Fig. 2.7 display the sequence of gating of switches of the inverter controlled by the proposed control technique. During the positive half of the trapezoidal reference, the switches S_1 and S_3 are gated simultaneously forcing the current to flow in positive direction through the load, Fig. 2.7(a), this is followed in the next interval by turn-off of S_3 and simultaneously turn-on of S_2. During this interval, Fig. 2.7(b), the current follows the same direction through the load but now S_3 and the integral diode of switch S_4 starts to conduct.

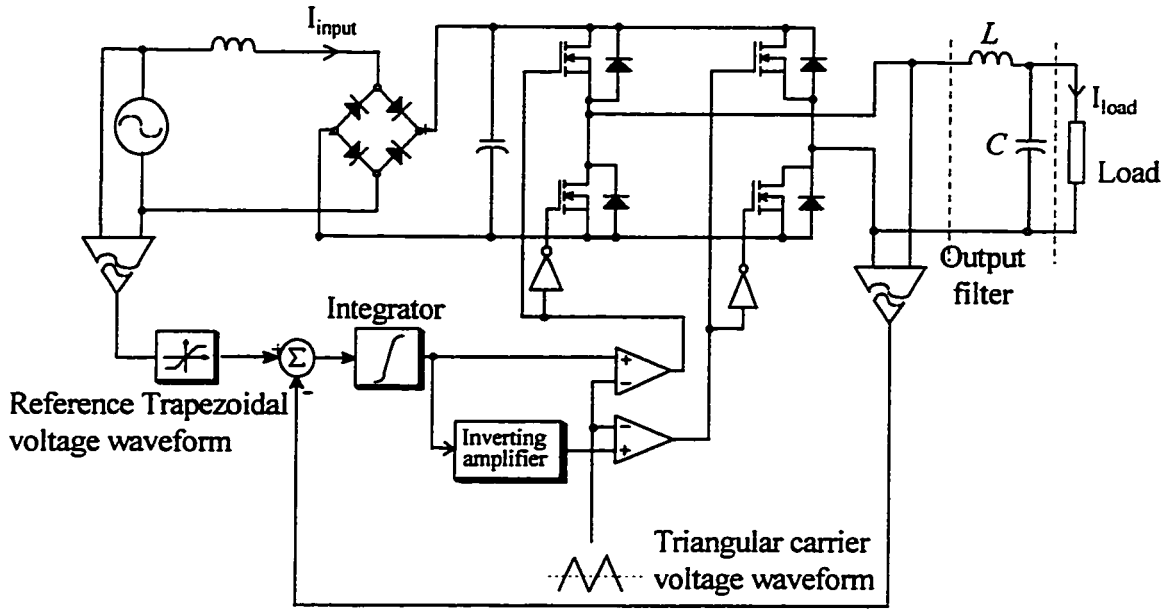


Fig. 2.6 Triangular-carrier based PWM integral control.

These modes of operation are sequentially repeated throughout the positive half cycle of trapezoidal reference.

During the negative half of the trapezoidal reference, switches S_2 and S_4 are gated simultaneously, forcing the current through the load in opposite direction as shown in Fig. 2.7(c) . In the next interval, S_2 turns-off and integral diode of S_3 starts to freewheel to maintain the current in the same direction as displayed in Fig. 2.7(d). These two intervals are repeated throughout the negative half of trapezoidal reference.

As it can be observed, the lower switches S_3 and S_4 carry higher rms current as compared to the upper switches S_1 and S_2 , of the two legs of the PWM inverter.

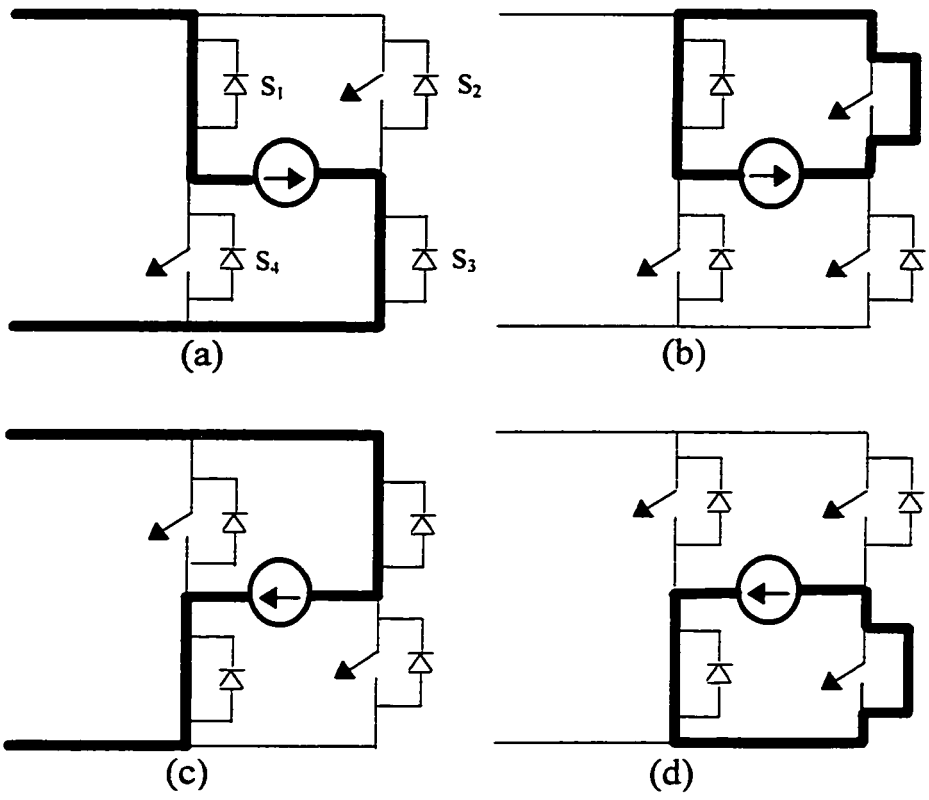


Fig. 2.7 Modes of Operation of the PWM inverter based on the Triangular-carrier integral control . (a) and (b) represent operation of the inverter for positive half-cycle of the trapezoidal reference. (c) and (d) depict the operation of the inverter for negative half-cycle of the trapezoidal reference.

2.4 One Cycle or Reset Integral Control Technique

Reset integral control also known as the one-cycle control [34][35][38], forces the average value of the switched variable to follow a dynamic reference within one cycle. The duty-ratio of the switch is controlled such that in each cycle the average value of the switched variable of the switching circuit is exactly equal to or proportional to the control reference, both in the steady and the transient state. It rejects power source perturbations

and corrects switching errors if the dc bus voltage is measured at the inverter output [38].

2.4.1 Principle of operation

Fig. 2.8 shows the generalized pattern generator based on One-cycle Integral PWM control. The dc bus voltage is sensed across the bottom switch and is integrated by a resettable integrator. The integrated output voltage (v_{int}) is compared with the reference voltage signal (v_{ref}) by the comparator. When integrated voltage v_{int} hits the reference voltage v_{ref}, the integrator is reset (goes low) and the switch across which the voltage is sensed, turns ON hence applying zero voltage across the integrator. When the clock sets the flip-flop (Q goes high), the switch is turned OFF and the sensed voltage is applied to the integrator. The clock fixes the switching frequency of the pattern generator.

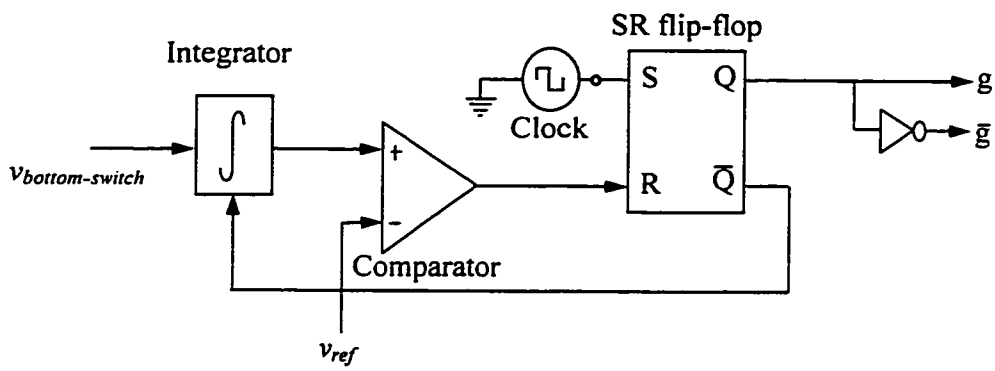


Fig. 2.8 Pattern generator based on One-cycle integral PWM control

2.4.2 Implementation aspects

The implementation of One cycle integral PWM control for the proposed topology is illustrated in Fig. 2.9. The ac mains voltage is directly sensed from the single-phase ac

mains supply and passed through a limiter circuit to generate a trapezoidal-shaped reference signal. By generating the reference signal in such a manner, the trapezoidal-shaped reference is in phase and synchronized with the 120 Hz dc bus ripple. That is the zero-crossing of this reference signal corresponds to the zero-crossing of the dc bus ripple voltage.

The control circuit further consists of two feedforward loops based on One cycle Reset integral control principle. Each consists of a Reset Integral PWM control block which further consists of a real-time resettable integrator, a comparator, a clock, and S-R flip-flop. The output of the clock signal is tied to the SET option of the two flip-flops. The PWM gating signals generated by the upper controller block is complementary fed to the two switches of the left leg of the full-bridge inverter whereas the output of the lower PWM controller is fed to the two switches of the right leg of the full-bridge inverter.

The proposed simple on-line pattern generator based on cycle by cycle control of output voltage has a closed loop structure and requires sensing of the instantaneous value of the voltage across the bottom switches. This voltage is applied to a resettable real-time integrator. The integrated output is compared to a trapezoidal-shaped reference. As it reaches the reference during a cycle, the integrator is reset and the bottom switch is turned on. Similar operation is exhibited by the lower loop, the only difference is that the integrator output is compared with a trapezoidal reference which is inverted (180 degrees phase shift).

With this type of implementation, the upper loop (with a trapezoidal-shaped reference) controls the duty-cycle of the left leg of the full-bridge inverter during the first

half period and the lower loop (with an inverted trapezoidal-shaped reference) controls the duty-cycle of the right leg of the full bridge inverter during the remaining half period of the trapezoidal reference.

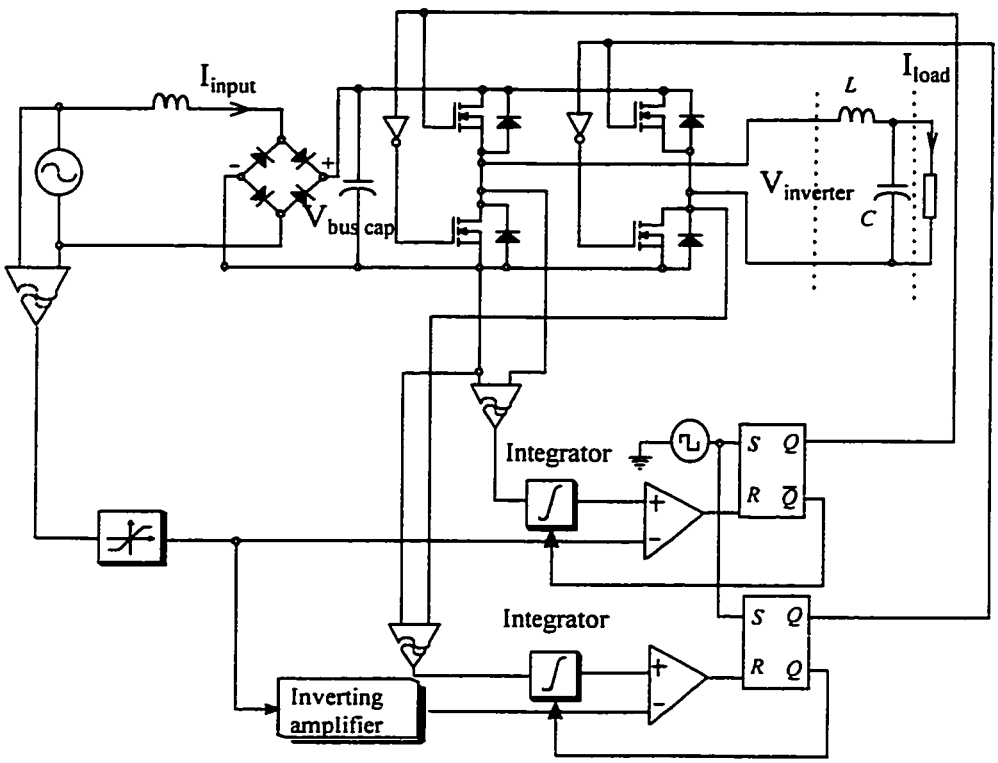


Fig. 2.9 One-cycle Reset Integral PWM controller.

2.4.3 Modes of operation

The modes of operation of the PWM inverter illustrated in Fig. 2.10 displays the sequence of gating of switches of the inverter controlled by the proposed topology. During the positive half of the trapezoidal reference, the switches S_1 and S_3 are gated

simultaneously forcing the current to flow in positive direction through the load, Fig. 2.10(a), this is followed in the next interval by turn-off of S_1 and simultaneously turn-on of S_4. During this interval, Fig. 2.10(b), the current follows the same direction through the load but now S_3 and the integral diode of switch S_4 starts to conduct. These modes of

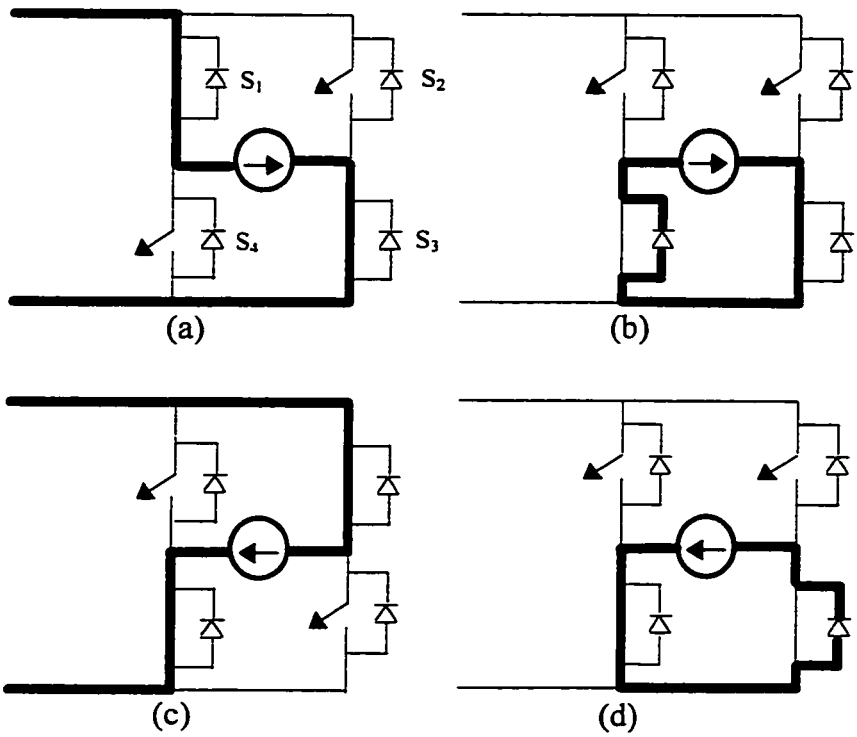


Fig. 2.10 Modes of Operation of the PWM inverter based on the reset integral control. (a) and (b) represent operation of the inverter for positive half-cycle of the trapezoidal reference. (c) and (d) depict the operation of the inverter for negative half-cycle of the trapezoidal reference.

operation are sequentially repeated throughout the positive half cycle of trapezoidal reference.

During the negative half of the trapezoidal reference, switches S_2 and S_4 are gated simultaneously, forcing the current through the load in opposite direction as shown in Fig. 2.10(c) . In the next interval, S_2 turns-off and integral diode of S_3 starts to freewheel maintain the current in the same direction as displayed in Fig. 2.10(d). These two intervals are repeated throughout the negative half of trapezoidal reference. As it can be observed, the lower switches S_3 and S_4 carry higher rms current as compared to the upper switches S_1 and S_2 , of the two legs of the PWM inverter.

2.5 Conclusions

In this chapter three PWM pattern generation and control strategies based on voltage integral control with their block diagram implementation are presented for a single phase trapezoidal ac power supply. The principle of operation of each control scheme is explained. Modes of operation of the PWM inverter based on various PWM pattern generation and control strategies is illustrated.

CHAPTER 3

CONTROL LOOP DESIGN

3.1 Introduction

In the previous Chapter, the principle of operation of the three PWM pattern generation and control techniques have been presented. In hysteresis based control technique, the error generated due to the comparison of reference and feedback voltages is averaged using a real-time integrator and then limited within a boundary by controlling the duty-cycle of the switches of the inverter. In triangular-carrier based control technique, the generated error is averaged using a real-time integrator and then limited within a boundary established by a triangular-carrier waveform. The switching frequency is stabilized by the carrier. In reset control technique, the integrated sensed voltage is compared with the trapezoidal reference in each cycle and error generated controls the gating signals applied to the switch.

Therefore in all three PWM pattern generation and control techniques, the heart of control loop is the real-time integrator as it provides better tracking of output voltage with the reference waveform. Therefore the selection of the proper time constant of the integrator is a crucial design parameter.

In this Chapter, design guidelines for the selection of integrator time constant are presented for all the three control techniques. Further, the key simulation waveforms are also presented.

3.2 Hysteresis PWM integral control technique

Hysteresis control is a well known and rugged technique [29]. It provides tight regulation of the control variable with a simple comparator circuit. Dynamic response is fast, however switching frequency varies over one cycle as well as with operating conditions [30].

The implementation of hysteresis control for the present application had been illustrated in Fig. 2.3. The purpose of the PWM pattern generator and control circuit is to maintain the average volt-sec of the output voltage over one switching cycle equal to the trapezoidal reference. Therefore, the instantaneous inverter output voltage is measured, compared to the trapezoidal reference and the integrated error, or average error is maintained within a hysteresis band by switching upper and lower switches. The two legs of the inverter are operated in a complementary fashion (diagonal switches are gated simultaneously).

3.2.1 Design guidelines for the control loop

Design of the controller involves the choice of hysteresis band and integrator time constant. However, the accuracy of the output voltage tracking is essentially dependent upon the switching frequency. Therefore, hysteresis band and integrator time constant can

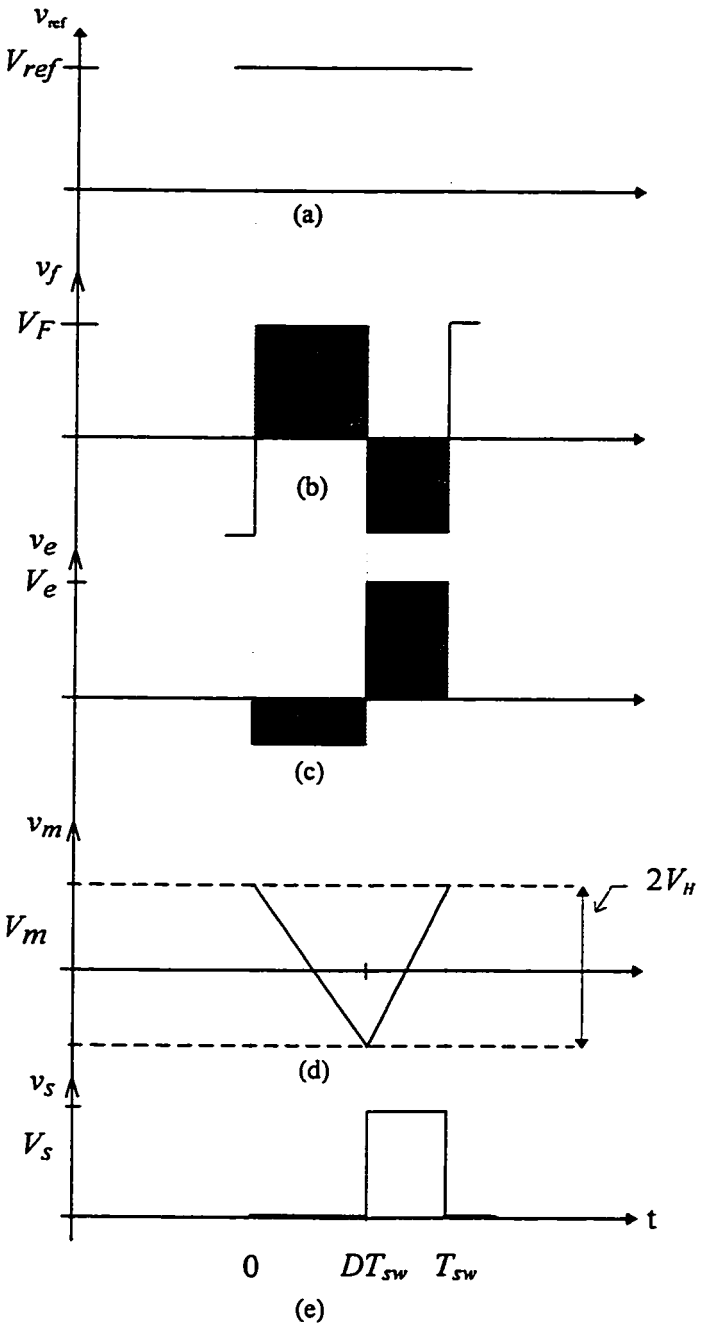


Fig. 3.1 Waveforms representing a specific period of operation of the converter based on hysteresis based controller. (a) reference trapezoidal waveform. (b) feedback voltage signal. (c) error voltage signal. (d) integrated error waveform. (e) gating signal generated at the output of the comparator.

be used to control the switching frequency.

From the Fig. 3.1, it can be observed that,

$$\frac{1}{T_i}\int_0^{DT_{sw}}(V_R - V_F)\,dt = -2V_H \tag{3.1}$$

And,

$$\frac{1}{T_i}(V_R - V_F)\,DT_{sw} = -2V_H \tag{3.2}$$

the duty cycle can be defined as,

$$D = \begin{cases} = \dfrac{V_R}{V_F} & V_F > V_R \\ 1 & V_F < V_R \end{cases} \tag{3.3}$$

Further from the waveform of V_e , it can be observed that when the feedback voltage is less than the reference voltage, the switch is always ON ie. D = 1. When the feedback voltage is greater than the reference voltage, the duty cycle is equal to $\frac{V_R}{V_F}$.

$$\frac{1}{T}(V_R - V_F)\,\frac{V_R}{V_F}\,T_{sw} = -2V_H \tag{3.4}$$

Therefore,

$$T_{sw} = \frac{2V_H T_i V_F}{(-V_R + V_F)\,V_R} \tag{3.5}$$

$$\text{Maximum switching frequency, } f_{sw(max)} = \frac{V_R}{2V_H T_i} \tag{3.6}$$

Maximum switching frequency for V_{fmax} ,

$$\frac{V_R(V_{F\max} - V_R)}{2V_H T_i V_{F\max}} = f_{sw(\max)} \tag{3.7}$$

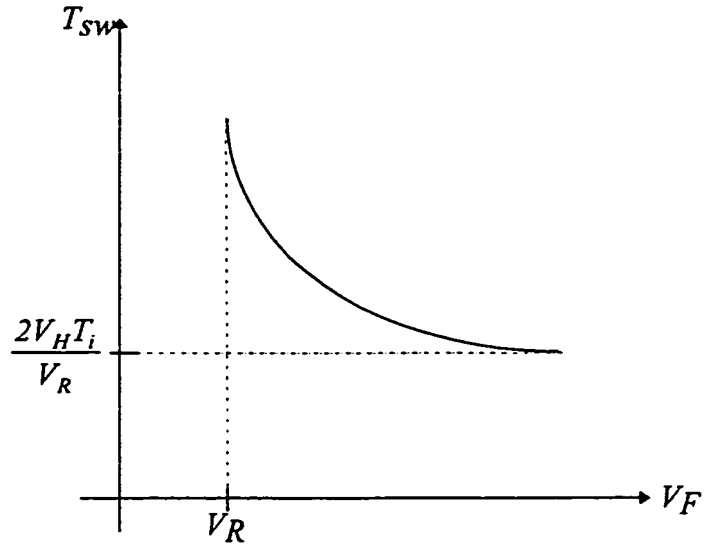


Fig. 3.2 Variation of feedback voltage with the switching period.

It was found that given an average switching frequency, a hysteresis band of 5% of the peak of the trapezoidal waveform, together with an integrator time constant equal to 0.5 of the average switching period, resulted in good tracking.

3.2.2 Simulated results

Simulated waveforms for input line current, load voltage and dc bus voltage for the proposed power supply based on Hysteresis integral PWM control are shown in the Fig. 3.2.

3.3 Triangular-Carrier Integral Control

The basic loop is identical to the hysteresis controller [33]. However, the switching frequency is stabilized by means of triangular carrier; the integrated error is

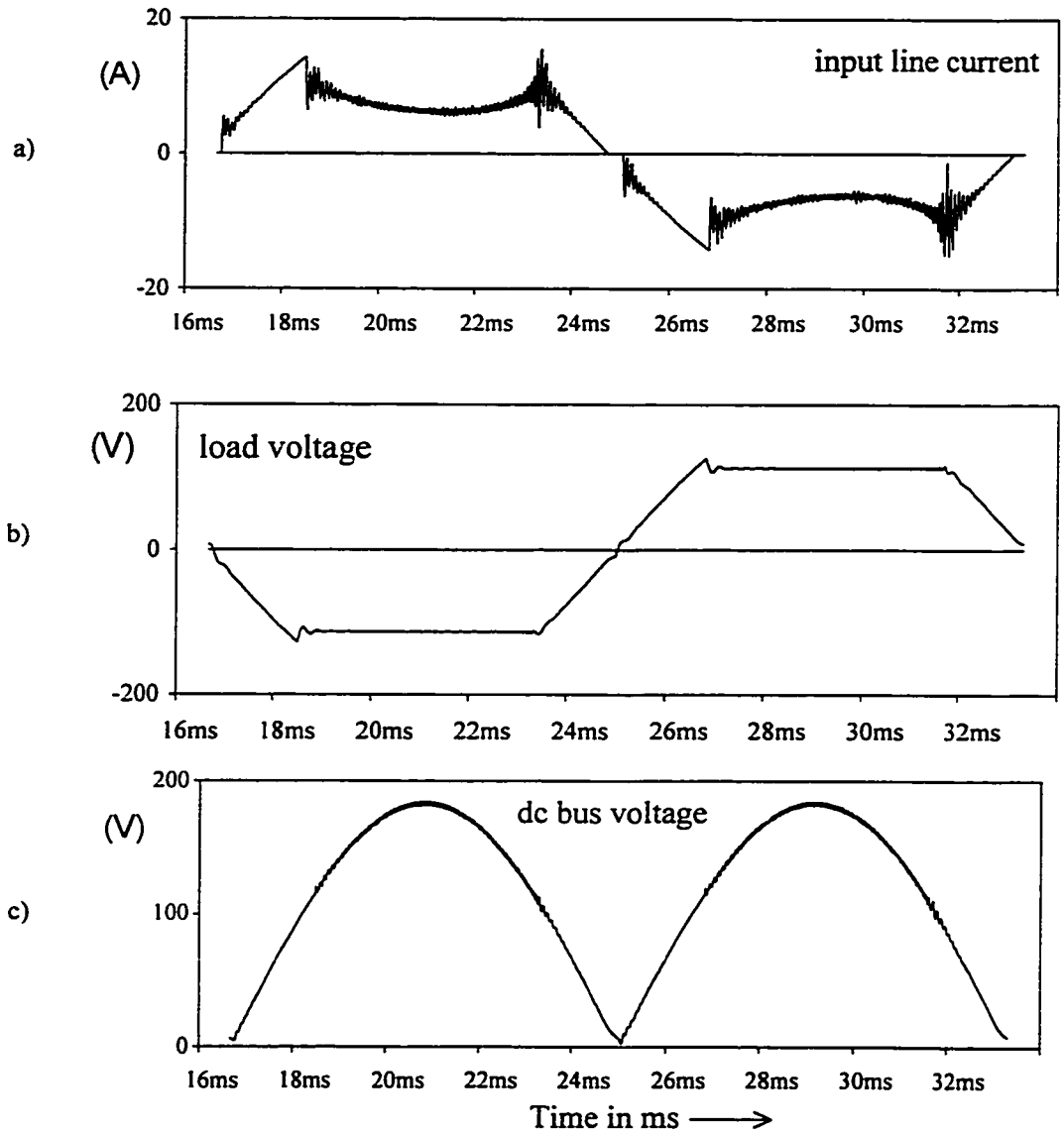


Fig. 3.3 Operation of the hysteresis based PWM controller (simulated results). (a) Input current. (b) Load voltage (filtered). (c) Dc bus voltage. (Hysteresis window $\Delta V_H = 5$ % peak of reference, average switching frequency $f_{SW} = 40$ kHz, input voltage = 120 V, output voltage = 90 V rms, rated output current = 10 A, resistive load).

intersected with the carrier and intersections define switching instants, Fig. 3.4. Inverter switching frequency is constant and equal to the carrier frequency. design is simpler than

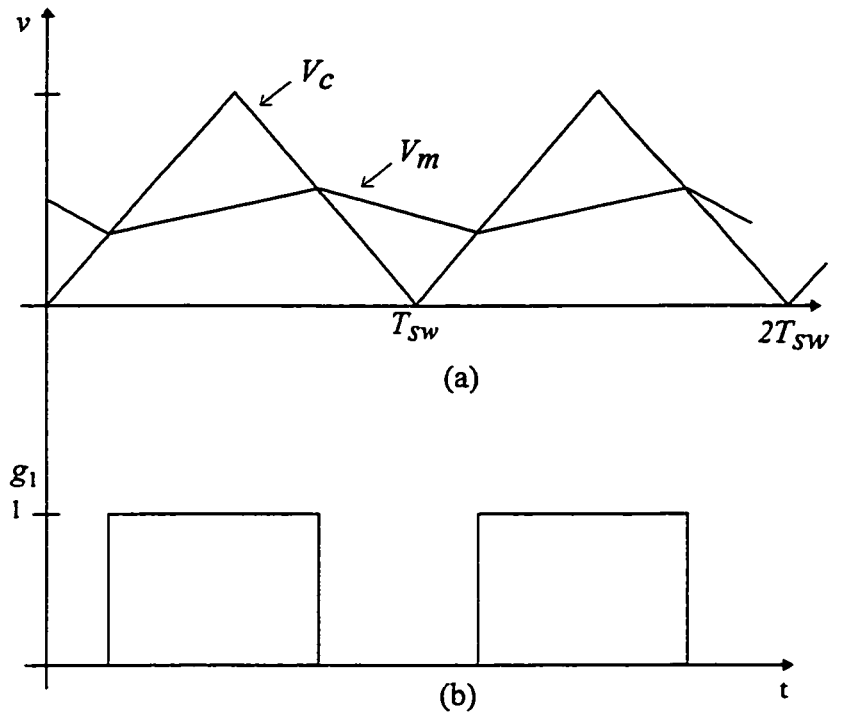


Fig. 3.4 Control waveforms for triangular-carrier integral control technique

that of the hysteresis controller [35].

3.3.1 Design guidelines for the control loop

The key design parameter of the control loop is the integrator time constant T_i. The time constant should be small enough to achieve a fast response, but large enough to maintain proper PWM operation [29]. The constraint is that the slopes of the modulation waveform v_m should be smaller than those of the carrier waveform v_{carr}. The maximum

falling slope of v_m occurs when the reference voltage v_{ref} is at the maximum and the inverter voltage v_{inv} is zero, i.e.

$$S_f = \frac{V_{ref,\max}}{T_i} \tag{3.8}$$

The maximum rising slope of V_m occurs when the difference between v_{int} and v_{ref} at the maximum. This corresponds to the peak of the sine wave, i.e.

$$S_r = \frac{V_{fbk.peak} - V_{ref.max}}{T_i} \tag{3.9}$$

On the other hand, the rising and falling slopes of the carrier waveform are equal to $4V_c / T_{sw}$ where V_c is the peak amplitude of the carrier and T_{sw} is the switching period.

The slope constraints are:

$$\frac{V_{ref.max}}{T_i} < \frac{4\ V_c}{T_{sw}} \tag{3.10}$$

and

$$\frac{V_{fbk.peak} - V_{ref.max}}{T_i} < \frac{4\ V_c}{T_{sw}} \tag{3.11}$$

According to (3.10) and (3.11), and assuming $V_c = 1$ and a voltage sensor gain of 1.0, the integrator time constant is 110 μs. To provide a safety margin, particularly in view of the dc bus fluctuations, a value of 150 μs is chosen for T_i.

3.3.2 Simulated results

Simulated waveforms for input line current, load voltage and dc bus voltage for the proposed power supply based on triangular-carrier integral PWM control are shown in the Fig. 3.5.

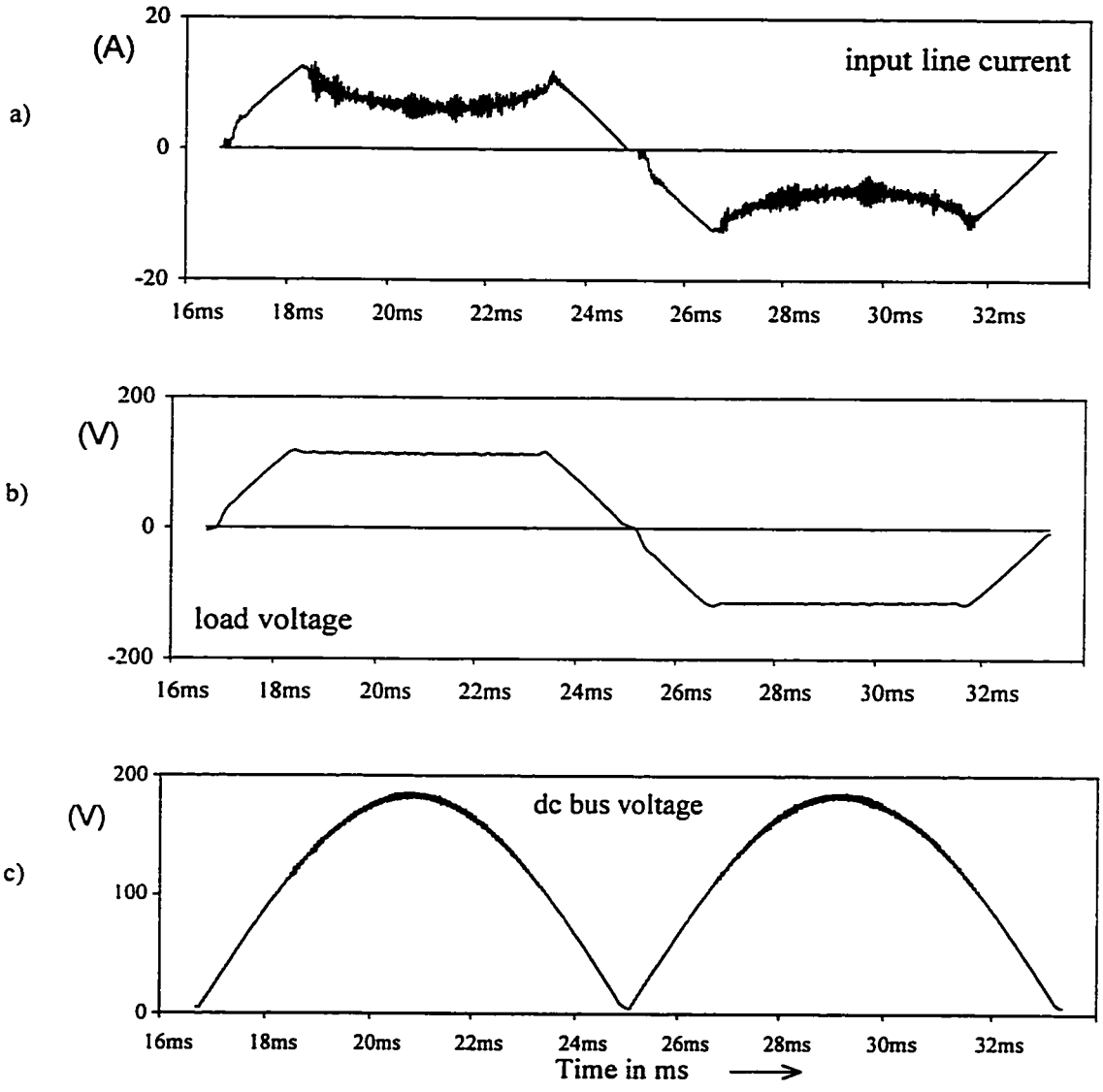


Fig. 3.5 Operation of the Triangular Carrier-based integral PWM controller (simulated results). (a) Input current. (b) Load voltage (filtered) (c) DC bus voltage. (Magnitude of the carrier = 20 V (peak to peak), average switching frequency f_{sw} = 40 kHz, input voltage = 120 V rms, output voltage = 90 V rms rated output current = 10 amps, resistive load).

The error triangulation method provides instantaneous waveshaping resulting in very fast response and has the advantage of constant switching frequency. This simplifies input filter design.

3.4 Reset Integral control

Reset integral control, Fig.2.9, also known as the One-cycle control, forces the average value of the switched variable to follow the reference within one cycle. The technique rejects power source perturbations and corrects switching delays if the dc bus voltage is measured at the inverter output [38].

3.4.1 Design guidelines for the control loop

The on time of the switch is controlled by the rate of integration, dependent on the input voltage and integrator time constant and the control voltage V_{ref}. It can be

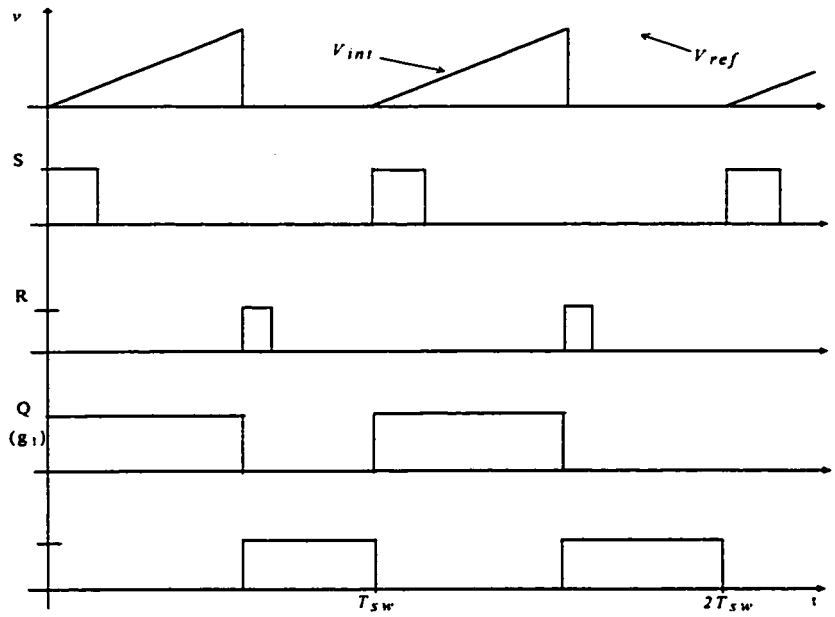


Fig. 3.6 Control waveforms for one-cycle reset PWM integral control technique.

computed from the following equation :

$$\frac{1}{T_i}\int_0^{t_{on}} v_{sw} = v_{ref} \tag{3.12}$$

where, v_{sw} the voltage across the switch, the v_{ref} control reference voltage and T_i the integrator time constant.

The switch voltage v_{sw} can be represented by

$$v_{sw} = v_{dc} + k_r . v_{dc} \ sin(2\pi \ f_r \ t) \tag{3.13}$$

where k_r is the measure of the harmonic content of the input at the dominant frequency f_r.

The integrator output is given by :

$$v_{int} = \frac{k_s v_{sw} t}{T_i} \tag{3.14}$$

where k_s is voltage sensor gain.

The design procedure involves choosing the integrator to integrate the switch voltage to the value of the reference voltage, corresponding to the duty cycle $D = 1$ in one switching period. Constraints are satisfied for a given integrator time constant when :

$$\frac{k_s v_{dc}(1-k_r)T_{sw}}{T_i} = v_{ref} \tag{3.15}$$

Rearranging the above equation, we have

$$(1-k_r)\ v_{ref,max} = v_{ref} \tag{3.16}$$

From the equations above, with v_{sw}= $120\sqrt{2}$ volts, v_{ref} = 90 V rms and switching frequency = 40 kHz, the integrator time constant is derived equal to 20 μs.

3.4.2 Simulated results

Simulated waveforms for input line current, load voltage and dc bus voltage for the proposed power supply based on reset integral PWM control are shown in the Fig. 3.7.

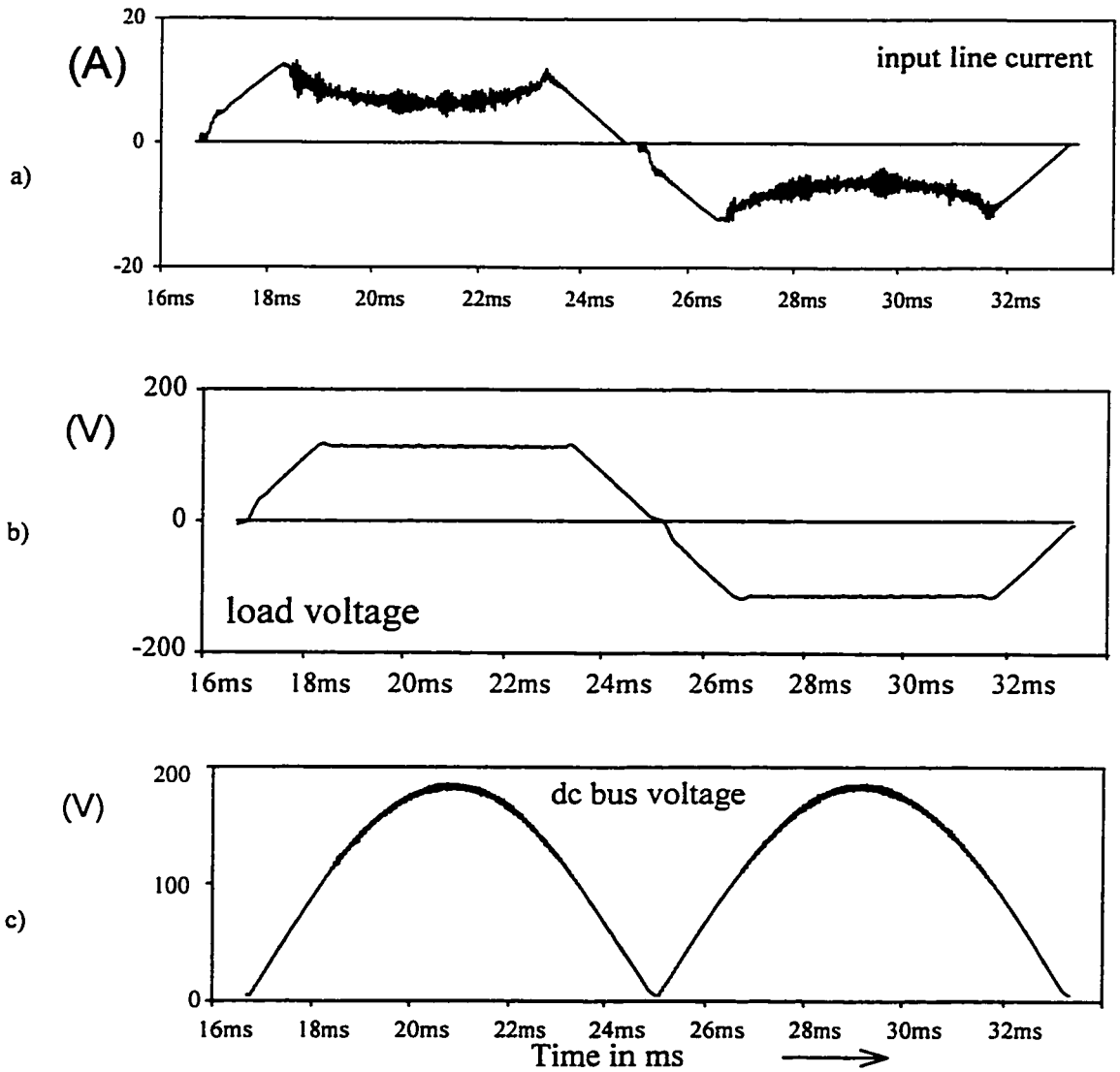


Fig. 3.7 Operation of the Reset Integral PWM Controller (simulated results) (a) Input current (c) output voltage (filtered) (c) DC bus voltage. (Integrator gain = 20 μs, switching (clock) frequency f_{SW} = 40 kHz, input voltage = 120 V, output voltage = 90 V, rated output current = 10 A, resistive load).

3.5 Conclusions

In this chapter, the design of the control loop for all the three control techniques has been illustrated. The design equations have been derived to select a proper time constant of the integrator which is a crucial design parameter of the control loop for the three control techniques. Key simulation waveforms obtained validate the selection of the appropriate value of the integrator time constant.

CHAPTER 4

ANALYSIS AND PERFORMANCE COMPARISON OF THE THREE CONTROL SCHEMES

4.1 Introduction

As discussed, the selection of the size of the dc bus capacitor for the power supply is based on a trade-off between two conflicting requirements. One being the input current distortion as a function of dc bus capacitor value and the other is the filtering provided by this capacitor to the reflected high frequency current harmonics, generated due to the PWM inverter. Since the dc capacitor is small, it does not provide a buffer between ac and dc sides, therefore, the shape of the output voltage and current affect the ac input current drawn by the power supply.

In order to examine this interaction, an analysis based on the average switching function is proposed, the switching frequency components being neglected. The analysis uses the concept of transfer characteristics. In addition to giving a quantitative explanation of the power supply waveforms, the switching function analysis also establishes the theoretical limits to power factor and input harmonic distortion, assuming the inverter switching frequency is high and can be eliminated by means of a small low-pass filter. Further in this chapter, a performance comparison of three PWM pattern

generation and control techniques is presented. The performance features are compared based on the indices such as input current Total Harmonic Distortion and input power factor.

4.2 Average switching function analysis

In this Chapter, the transfer characteristics of the PWM inverter are first established quantitatively by considering the available input and expected output. Next, the analytical expressions (i.e. transfer function) for this transfer characteristics are derived as the ratio of expression representing relevant converter input and output [13].

The waveform to be modulated is considered the independent variable (input voltage/current in the converter). The resulting modulated waveform is the dependent variable (output voltage/current out of the converter). Therefore, the relationship between modulated and unmodulated waveforms can be analytically described by the following transfer function ;

$$\text{TF} = \frac{\text{converter dependent electrical variable}}{\text{converter independent electrical variable}} \tag{4.1}$$

The transfer characteristics of the rectifier and PWM inverter are derived, for example, the rectifier switching function is a bipolar square wave with a frequency equal to the line frequency: the rectified dc bus voltage (Fig. 4.1(a)) is the product of this switching function and the ac voltage:

$$v_{dc} = SW_{rect} \cdot v_{ac} \tag{4.2}$$

Similarly, the trapezoidal output voltage is obtained from the dc bus voltage through the inverter switching function

$$v_o = SW_{inv} \cdot v_{dc} \tag{4.3}$$

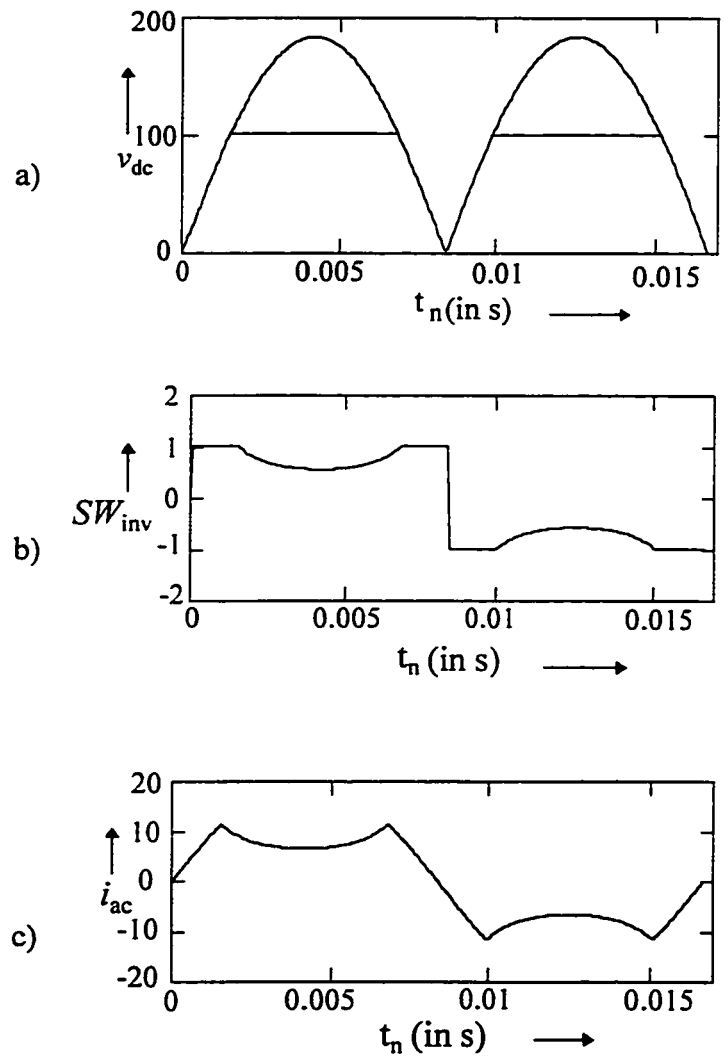


Fig. 4.1 (a) Rectified dc bus voltage and rectified trapezoidal reference. (b) Inverter average switching function. (c) Input line current (rated voltage, 130 V, rated load, 10 A).

The trapezoidal reference voltage is shown in Fig. 4.1(a) and it is assumed the output v_O tracks the reference if a suitable pattern generator is used, as described in Section II. The inverter switching function is shown in Fig. 4.1(b).

Assuming the load is resistive, the load current i_O is also trapezoidal. The dc bus current i_{dc} is given by:

$$i_{dc} = SW_{inv} \cdot i_o \tag{4.4}$$

and the ac input current:

$$i_{ac} = SW_{rect} \cdot i_{dc} \tag{4.5}$$

This current is shown in Fig. 4.1(c).

In addition to giving a quantitative explanation of the power supply waveforms, the switching function analysis also establishes the theoretical limits to power factor and input harmonic distortion, assuming the inverter switching frequency is high and switching frequency is high and switching frequency harmonics are eliminated by means of a small low pass filter.

The maximum input power factor and minimum input THD (caused by low frequency components only) are given in Table I as a function of input voltage. Since the trapezoidal reference is generated by clipping the ac input voltage, input current distortion will increase as the ac line voltage increases, thus lowering power factor to 0.89.

Conversely, for the lowest input voltage, 92 V, the trapezoidal output voltage waveform is nearly sinusoidal, accounting for a higher power factor of 0.99. For rated

input voltage, 120 V, the power factor has a high value of 0.94. Note also that as the input voltage increases, the input current decreases, as expected.

TABLE II

Theoretical limit - Input THD and power factor

(Switching function analysis, Average model, PWM switching neglected, resistive load)

Input voltage	Input rms current	Input THD	Input Power Factor
92 V	9.82 A	5.05 %	0.99
100 V	9.17 A	17.39 %	0.98
110 V	8.52 A	28.03 %	0.96
120 V	8.00 A	36.43 %	0.94
130 V	7.57 A	43.58 %	0.91
138 V	7.28 A	48.67 %	0.89

4.3 Example

The input power factor and input current total harmonic distortion have been calculated for a nominal sinusoidal source voltage of 120 V rms, 60 Hz while generating a trapezoidal shaped output voltage having rms value of 90 V, 60 Hz using average switching function analysis. In this analysis, the higher order switching frequency harmonics have also been neglected.

As already shown, the switching function of the rectifier and inverter are first derived. Then, the load current is reflected using the switching function to obtain the waveshape of the current drawn by the power supply.

Similarly the value of power factor and total harmonic distortion can be derived for various input voltages.

$$V = 120\sqrt{2}\ V \quad \omega = 2 \cdot \pi \cdot 60\ rad/s$$

$$k = 2^8$$

$$n = 0...k-1 \tag{4.6}$$

$$t_n = \frac{1}{60} \cdot \frac{n}{k-1} \text{ in seconds.} \tag{4.7}$$

The output of the full bridge rectifier is given as:

$$V_{dc_n} = |V.\sin(\omega \cdot t_n)| \tag{4.8}$$

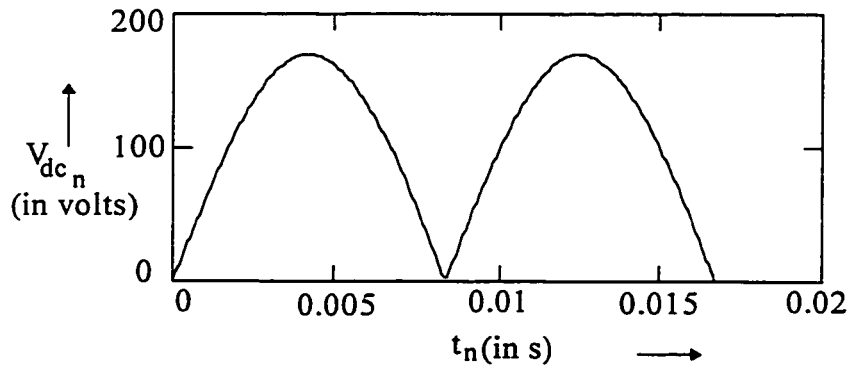


Fig. 4.2 Output rectified waveform of the bridge rectifier.

The Fourier transform of the output rectified waveform of the full- bridge rectifier can be obtained as following:

$$c = \frac{fft(V_{dc})}{\sqrt{k}} \cdot 2; \quad c_o = \frac{c_o}{2} \tag{4.9}$$

N=last(c) N=128 (4.10)

j=0....N (4.11)

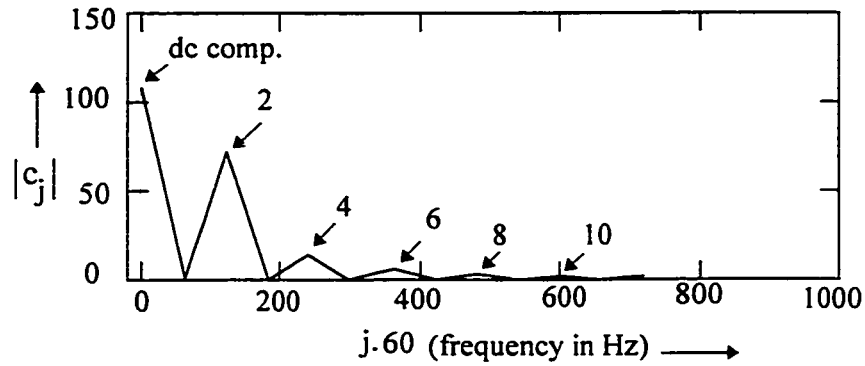


Fig. 4.3 Harmonic spectrum of the output voltage of the bridge rectifier.

TABLE III
Harmonic contents of the output voltage of the bridge rectifier

	dc comp.	2nd	4th	6th	8th	10th
Magnitude of the harmonics	107.6 V	72.5 V	14.4 V	6.2 V	3.4 V	2.2 V

The trapezoidal shaped output voltage waveform across the load as a function of λ is given by ;

$$V_{o_n} = V \sin(\omega t_n) \tag{4.12}$$

$$\lambda = 0.625$$

where λ is the multiplication factor required to make a trapezoidal output voltage equal to 90 V.

$$V_{o_n} = \begin{cases} \lambda.V & \text{if } V_{o_n} > \lambda.V \\ V_{o_n} & \text{if } V_{o_n} < \lambda.V \end{cases} \tag{4.13}$$

$$V_{o_n} = \begin{cases} V_{o_n} & \text{if } V_{o_n} > -\lambda.V \\ -\lambda.V_{o_n} & \text{if } V_{o_n} < -\lambda.V \end{cases} \tag{4.14}$$

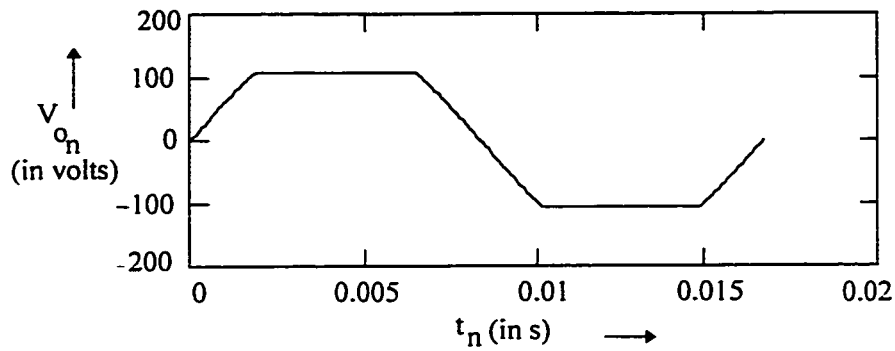


Fig. 4.4 Output trapezoidal waveform of the full-bridge inverter.

Obtaining the Fourier transform of the output voltage waveform of the full bridge inverter, we have:

$$c = \frac{fft(V_o)}{\sqrt{k}} \cdot 2,\ c_o = \frac{c_o}{2} \tag{4.15}$$

$$\text{N=last(c)}\quad \text{N=128} \tag{4.16}$$

$$\text{j=0....N} \tag{4.17}$$

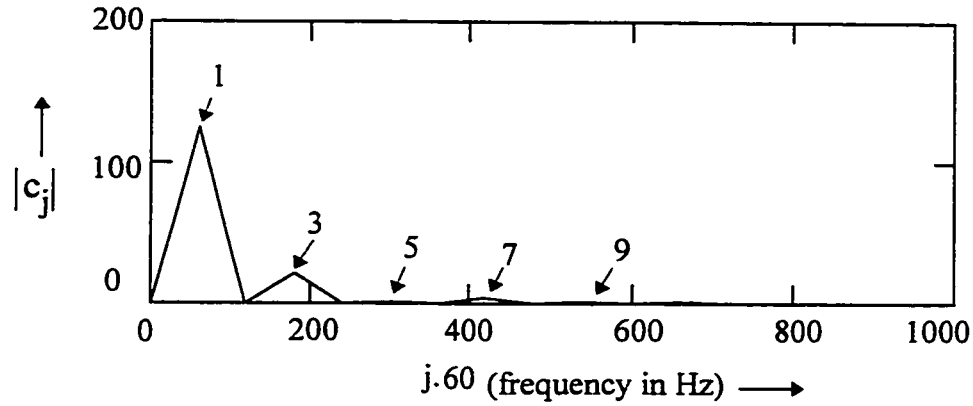


Fig. 4.5 Harmonic spectrum of the output trapezoidal waveform of the full-bridge inverter.

TABLE IV

Harmonic contents of the output trapezoidal waveform of the full-bridge inverter

	fund.	3rd	5th	7th	9th
magnitude of the harmonics	125.5 V	21.0 V	0.96 V	3.73 V	0.69 V

The rms value of the output trapezoidal waveform is given by:

$$\frac{\sqrt{\sum_{j=1}^{N}\left(|c_j|\right)^2}}{\sqrt{2}} = 90 \tag{4.18}$$

The switching function of the full bridge inverter is given as :

$$SW_n = \frac{V_{on}}{V_{dc_n}} \tag{4.19}$$

In Fig. 4.6, the switching fuction for the full-bridge inverter is given as

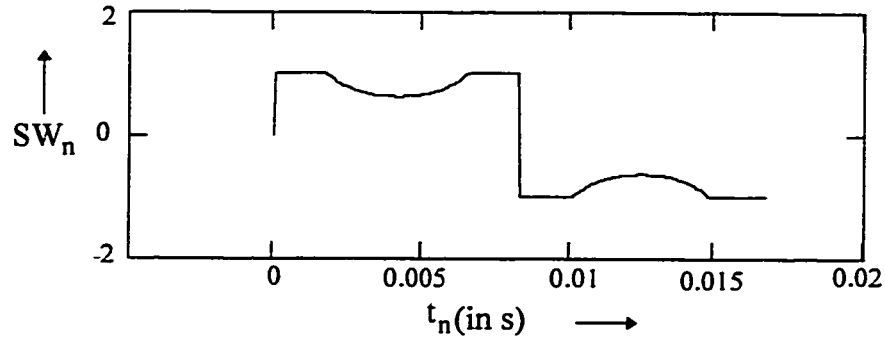


Fig. 4.6 Switching function curve of the full-bridge inverter.

The current through the load is obtained as:

$$i_{L_n} = \frac{V_{o_n}}{R} \tag{4.20}$$

Since the high switching order harmonics are neglected, the output filter can be neglected for low order harmonics. Further the dc bus current can be obtained by reflecting the load current to input of the full bridge inverter.

$$i_{L_n} = i_{L_n}.SW_n \tag{4.21}$$

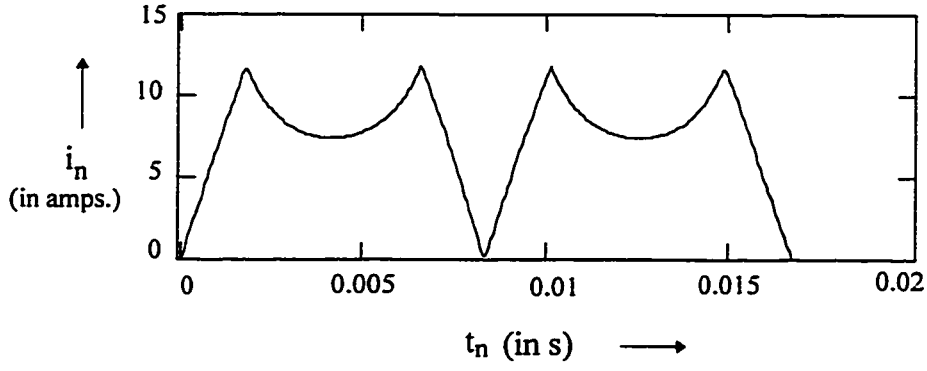


Fig. 4.7 Waveform of the dc bus current.

The input current drawn by the power supply is given by:

$$i_{s_n} = \begin{cases} i_{s_n} & t_n < \dfrac{1}{2.60} \\ -i_{s_n} & t_n > \dfrac{1}{2.60} \end{cases} \qquad (5.22)$$

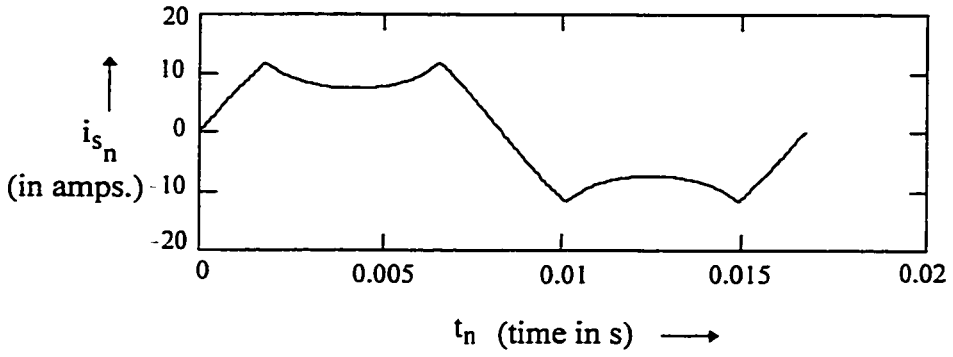


Fig. 4.8 Waveshape of the input current drawn from the utility by the supply.

Obtaining the Fourier transform of the input current drawn by the power supply, we get:

$$c = \frac{fft(i_s)}{\sqrt{k}} \cdot 2, \; c_o = \frac{c_o}{2} \qquad (4.23)$$

$$N=\text{last}(c) \quad N=128 \qquad (4.24)$$

$$j=0....N \qquad (4.25)$$

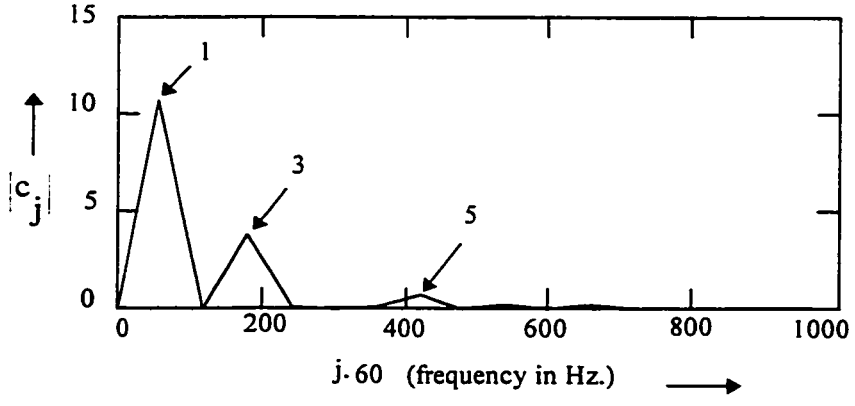


Fig. 4.9 Harmonic spectrum of the input current drawn by the power supply.

TABLE V

Harmonic contents of the input current drawn by the power supply

	fundam -ental	3rd	5th	7th	9th	11th	13th
Magnitude of the harmonics	10.6 A	3.78 A	0.04 A	0.73 A	0.17 A	0.24 A	0.13 A

The rms value of the input current is given by:

$$\frac{\sqrt{\sum_{j=1}^{N}\left(|c_j|\right)^2}}{\sqrt{2}} = 8.01 \tag{4.26}$$

Input harmonic total harmonic distortion is given by:

$$\mathbf{THD} = \frac{\sqrt{\sum_{j=2}^{N}\left(|c_j|\right)^2}}{|c_1|} \cdot 100 \tag{4.27}$$

$$\text{THD} = 36.36\ \%$$

Input power factor of the supply is given by:

$$\mathbf{PF} = \frac{|c_1|}{\sqrt{\sum_{j=1}^{N}\left(|c_j|\right)^2}} \tag{4.28}$$

$$\text{PF} = 0.94$$

4.4 Experimental Results

4.4.1 Conditions

The power supply is implemented with the 3 pattern generators and control circuits.

All the results are measured under the following conditions :

- Input voltage : 120 V rms, 60 Hz.
- Output voltage : 90 V rms, 60 Hz, 10 A rms (9 Ω resistive load).
- System parameters : line resistance R_S = 0.09 Ω, line inductance L_S = 10 μH, dc bus capacitor C_d = 10 μF.
- Switching frequency : 40 Hz.
- Controller design parameters : as calculated in this chapter.

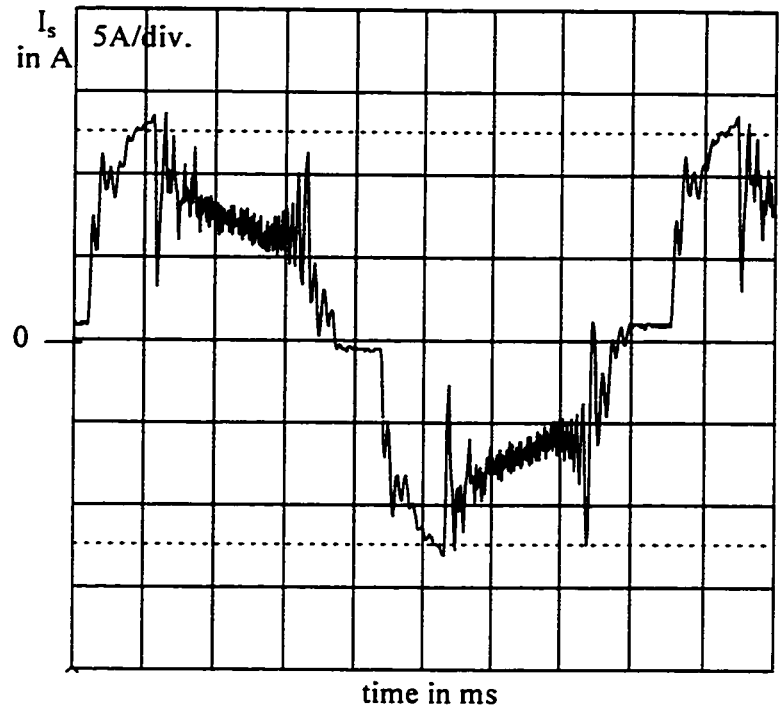
4.4.2 Current and voltage waveforms

Input current, output current (or output voltage), dc bus voltage and PWM (unfiltered) output voltage are given in Figs. 4.5, 4.6 and 4.7 for the hysteresis, triangular-carrier and reset integral techniques respectively.

4.5 Performance evaluation and comparison

To evaluate the performance of the proposed power supply implemented with three PWM pattern generators and control techniques, the following system is designed and studied:

a)



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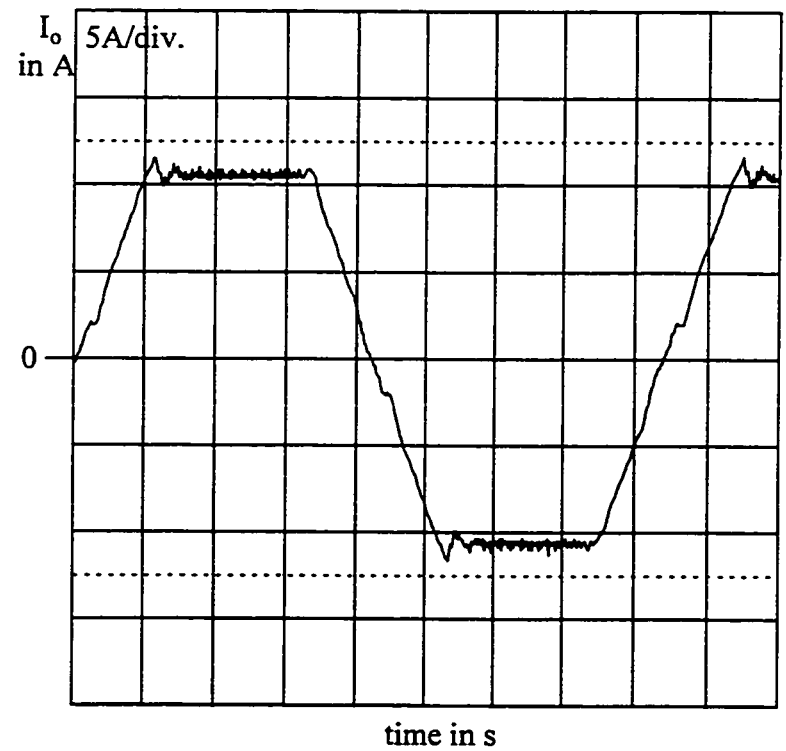
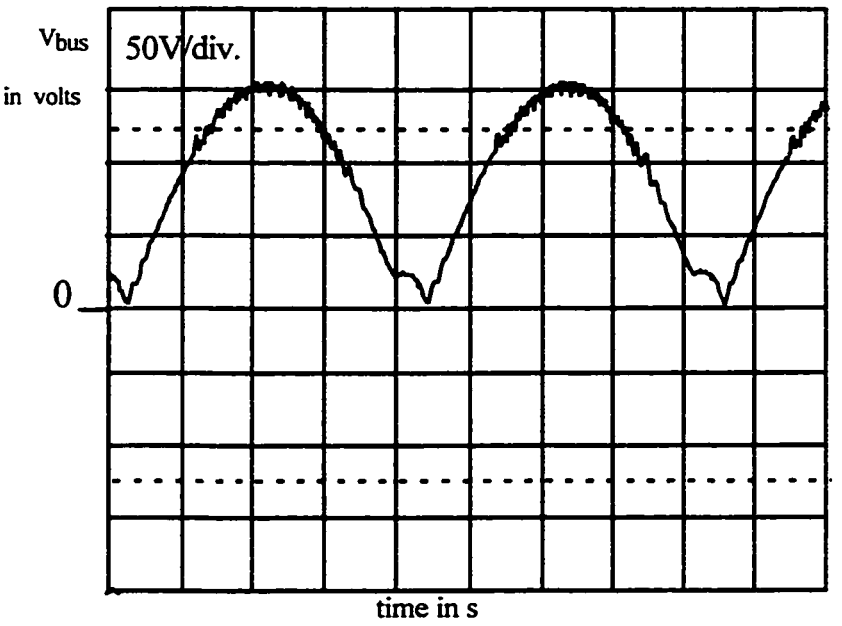
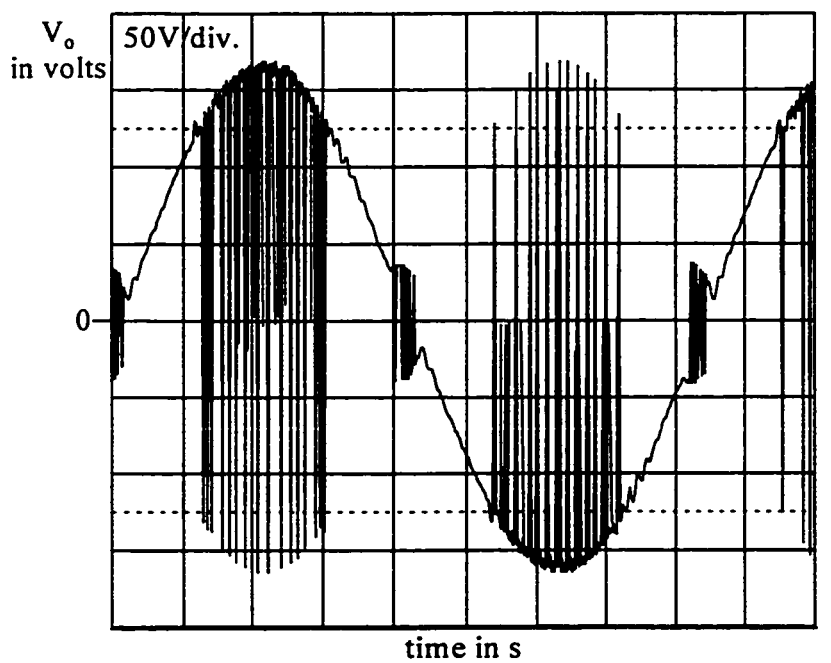




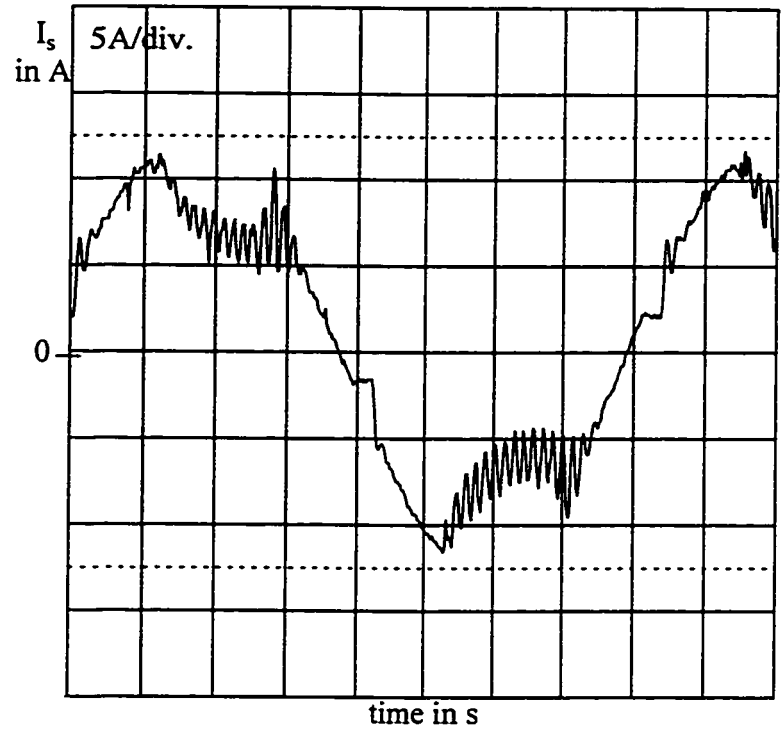
c)



d)

Fig. 4.10 Operation of the hysteresis controller (experimental results). (a) Input current. (b) Load current (filtered). (c) Dc bus voltage. (d) Unfiltered inverter output voltage. (Hysteresis window $\Delta V_H = 5$ % peak of reference, average switching frequency $f_{sw} = 40$ kHz, input voltage = 120 V, output voltage = 90 V rms, rated output current = 10 A, resistive load).

a)



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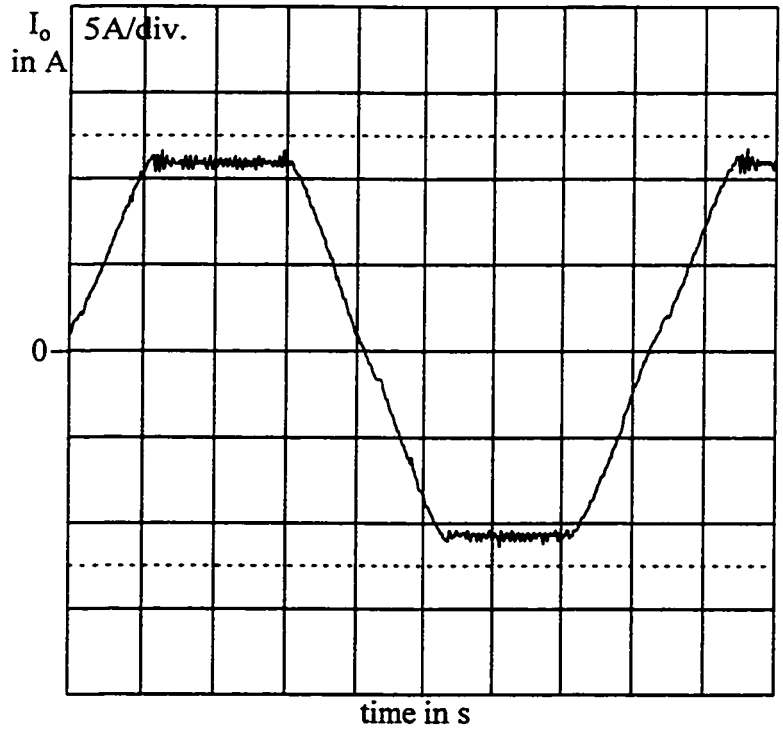

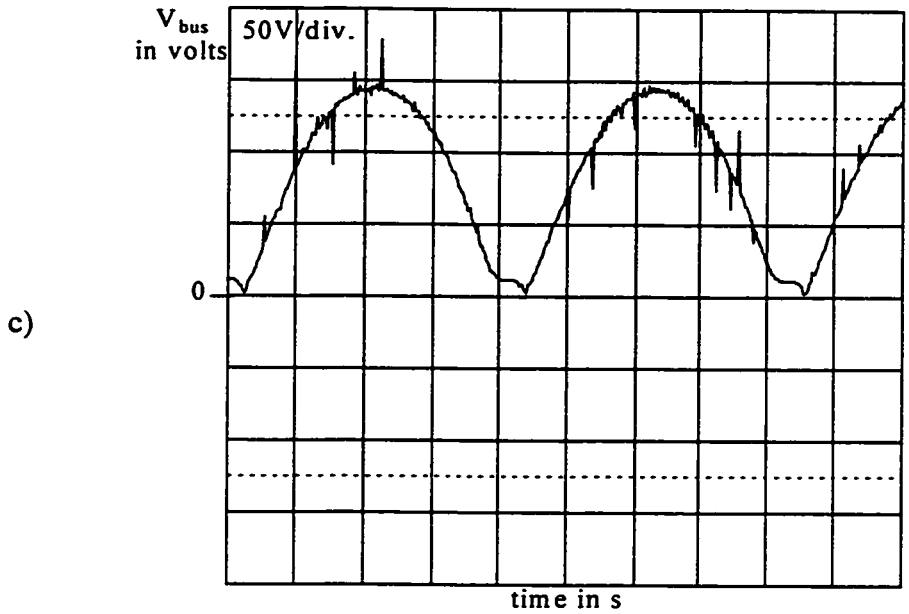

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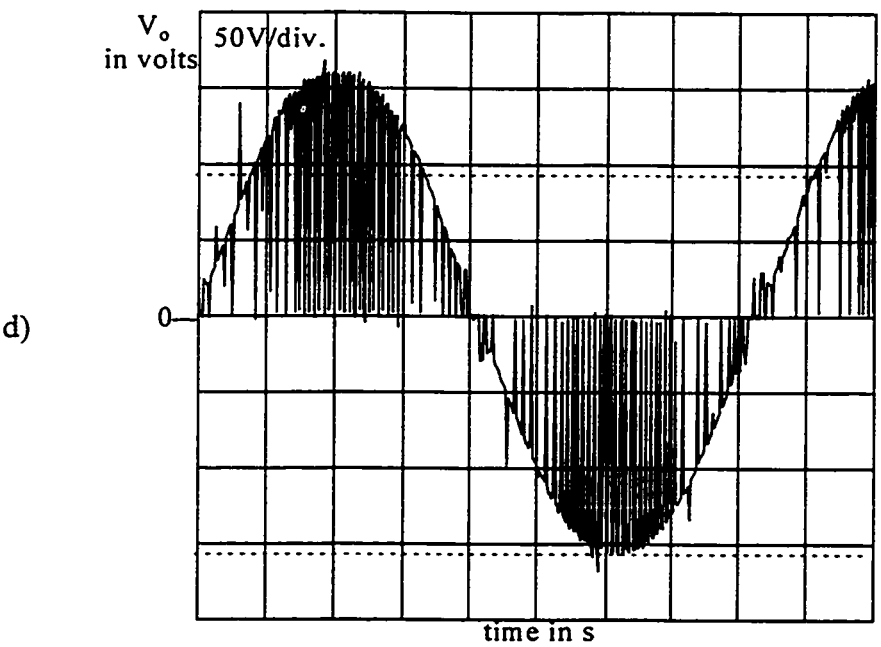
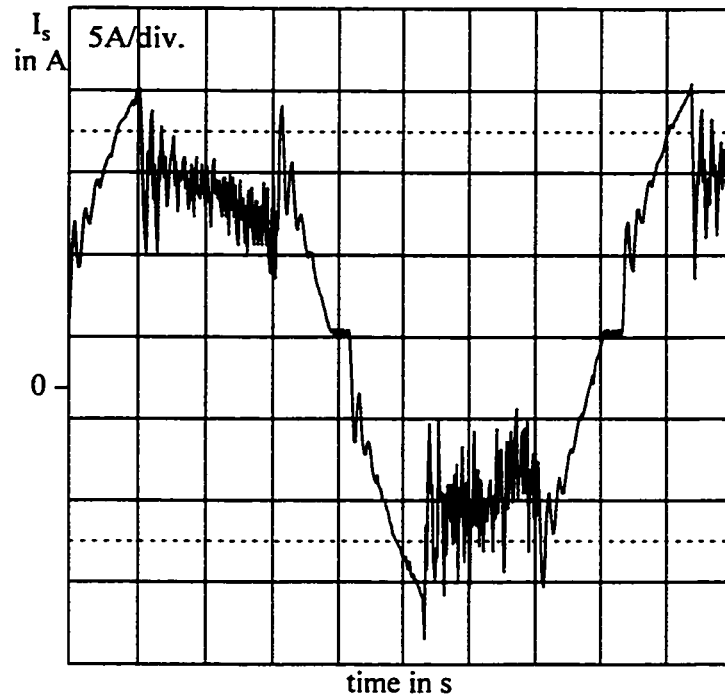


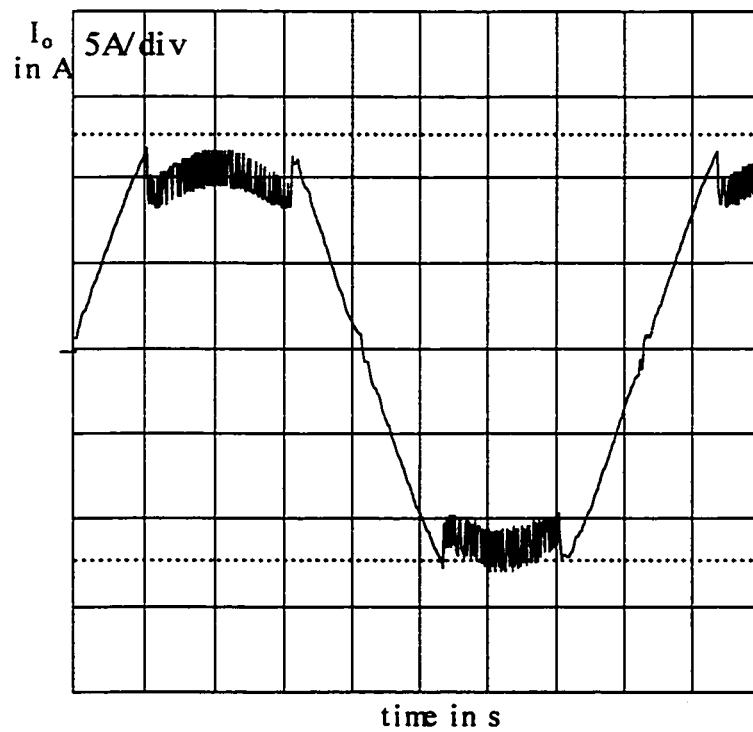
d)

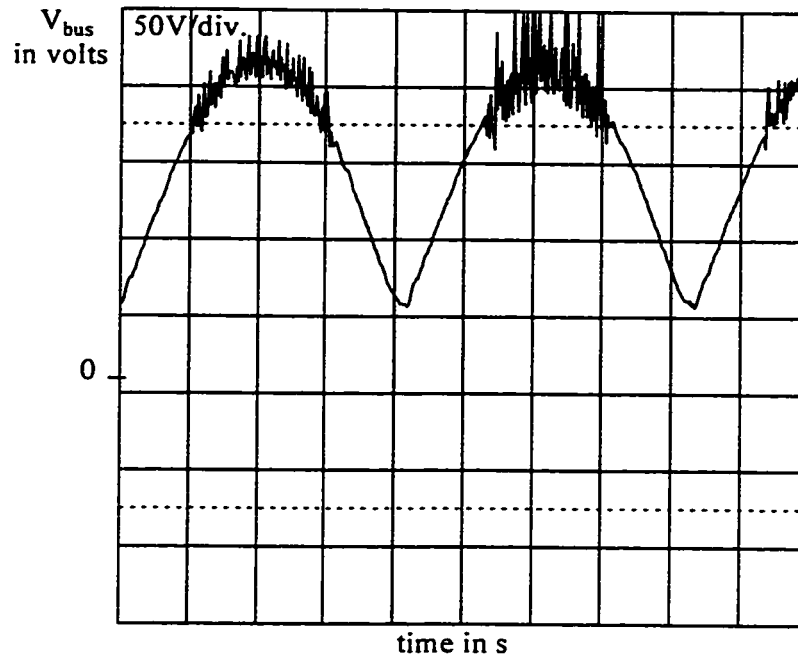
Fig.4.11 Operation of the Triangular Carrier -based integral PWM controller (experimental results). (a) Input current. (b) Load current (filtered). (c) DC bus voltage. (d) Unfiltered inverter output voltage . (Magnitude of the carrier = 20 V(peak to peak), average switching frequency f_{SW} = 40 kHz, input voltage = 120 V rms, output voltage = 90 V rms rated output current = 10 amps, resistive load.

a)

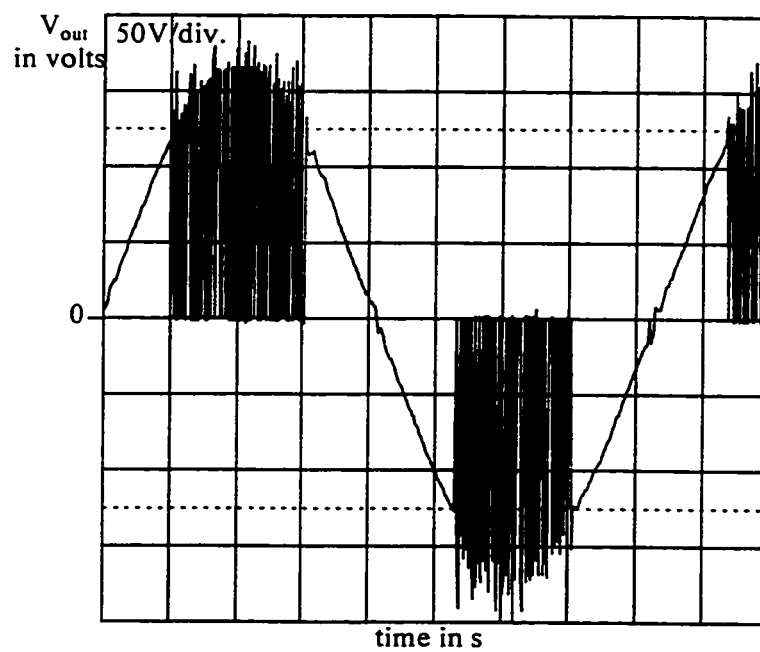


b)





c)



d)

Fig. 4.12 Operation of the Reset Integral PWM Controller (experimental results).(a) Input current. (b) Dc bus voltage. (c) Inverter output voltage (unfiltered). (d) Output voltage (filtered). (Integrator gain = 25 μs, average switching (clock) frequency f_{sw} = 40 kHz, input voltage = 120 V, output voltage = 90 V rated output current = 10 amps, resistive load).

The performance of such a power supply is studied under the following conditions; (i) varying load; (ii) different dc bus capacitor values, and (iii) varying input voltage levels. The power factor and input current THD are used as the criteria for comparative evaluation of the performance features.

4.5.1 Rated Operation

Fig.4.12 shows the rectified output voltage v_s, input current i_s and load current i_L. These figures illustrate that input current has a waveform much closer to the sinusoidal waveshape as compared to the pulse-like waveform of the conventional ac power supplies. In addition the current is in phase with the voltage, which gives a high input power factor. Since the dc link capacitor is small, the dc bus is almost the same as the rectifier waveform of the ac source voltage.

4.5.2 Change of the DC link Capacitor C_{dc}

(i) Effect on input power factor: Fig. 4.13 shows that as the value of the dc link capacitance is increased, the input power factor decreases almost linearly from about 0.9 to 0.6. The value of the pf is maximum i.e. 0.911, 0.903, 0.884 for Reset Integral, Triangular Carrier and Hysteresis Integral control technique respectively, when the dc bus capacitance value is as low as 10 μF.

At a larger value of C_{dc}, the current becomes more distorted, resulting in a faster decline of the power factor. The input power factor reduces to about 0.6 for all the three techniques when the value of the capacitance reaches 400 μF.

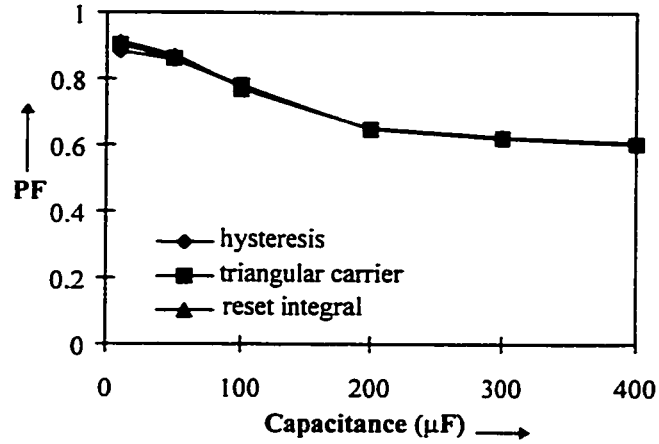


Fig. 4.13 Effect of different capacitor values on input power factor for proposed control techniques.

(ii) Effect on total harmonic distortion: The effect on the input total harmonic distortion is studied for different capacitor values for the three control techniques. Fig. 4.14 depicts the result of the variation of the capacitance values on the input THD for all the three control techniques. The THD increases linearly as the value of the capacitance increases from 10 μF to 400 μF. It varies from about 45 % to about 150 %.

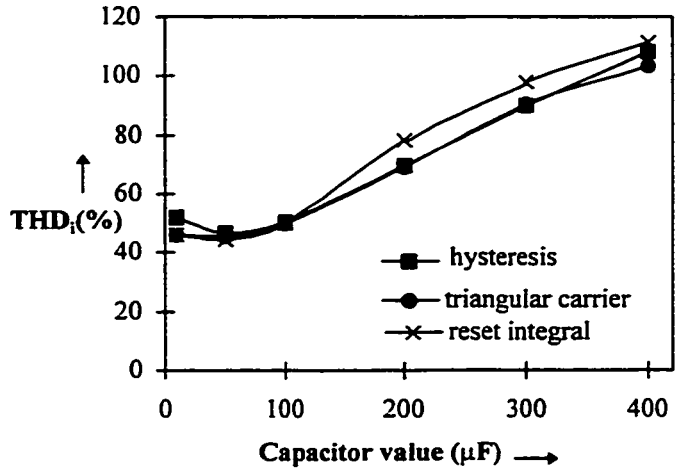


Fig. 4.14 Effect of different capacitor values on total harmonic distortion for proposed control techniques.

4.5.3 Variation of the percentage load

(i) Effect on input power factor: The three control techniques are studied under different load conditions, ranging from 10 % to 100 % load. Fig. 4.15 shows the variation of power factor with varying load. The reset integral control shows the best performance as the pf remains as high as 0.9 for loads varying from 20 % to 100 %. In the case of triangular-carrier control, the input power factor increases almost linearly with load but is quite lower than that of reset integral control especially at lower loads. The variation of pf

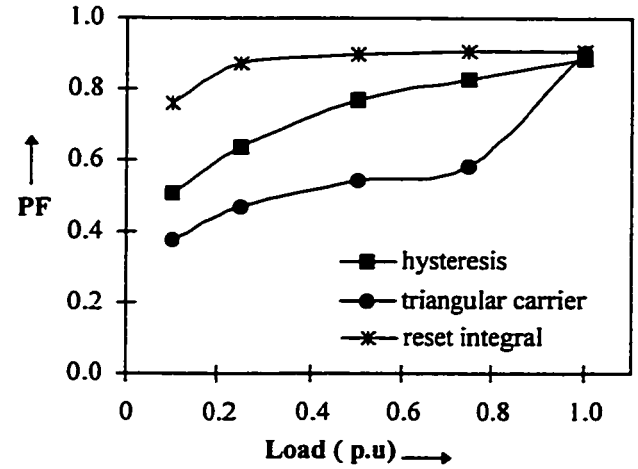


Fig. 4.15 Effect of varying load on input power factor for proposed control techniques.

with hysteresis is better than the triangular carrier control technique but not as good as reset integral control technique.

ii) Effect on total harmonic distortion:

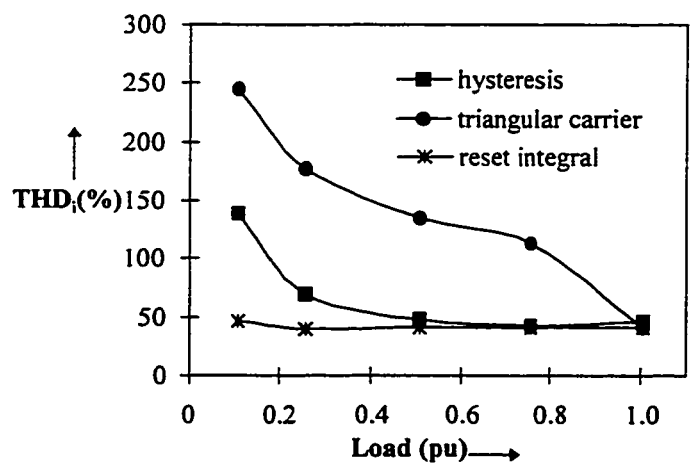


Fig. 4.16 Effect of varying load on input total harmonic distortion for proposed control techniques.

Fig.4.16 shows that the total harmonic distortion for the varying load conditions for reset integral control technique is minimum and remains approximately the same i.e around 50 %. The THD for triangular carrier control is maximum for almost all the load conditions but reduces with increasing load. The hysteresis control has a high THD at low loads which reduces quite considerably as the load increases.

C) Variation of the input voltage

(i)**Effect on Input power factor**: Fig. 4.17 shows that as we increase the value of the input voltage , the input power factor decreases almost linearly. The value of the pf is maximum i.e. 0.97, 0.99, 0.99 for hysteresis, triangular carrier and reset integral control techniques, respectively when the input voltage is as low as 0.75.

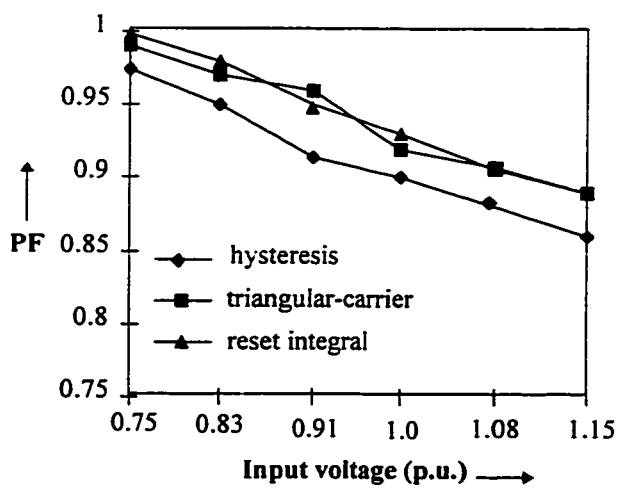


Fig. 4.17 Performance as a function of input voltage variation.

(ii) Effect on input total harmonic distortion:

As the input voltage varies from 90 V rms to 140 V rms, the input total harmonic distortion increases almost linearly for all the proposed techniques. For hysteresis-based controller, the %THD_i varies from 23% to 60%. The variation of THD_i is 5% to 48% for triangular-carrier based controller and from 18% to 48% for reset integral control technique.

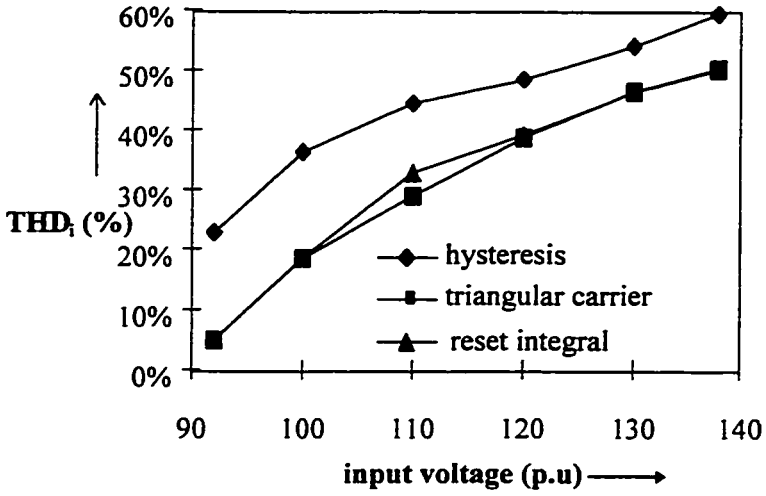


Fig. 4.18 Effect of input voltage variation on the performance of the proposed power supply.

D) Comparative efficiency:

Fig. 4.19 shows the comparative efficiency curve of the three techniques from no-load to full-load. It can be seen that the efficiency for all the three techniques remains high, above 90%, for loads above 50%.

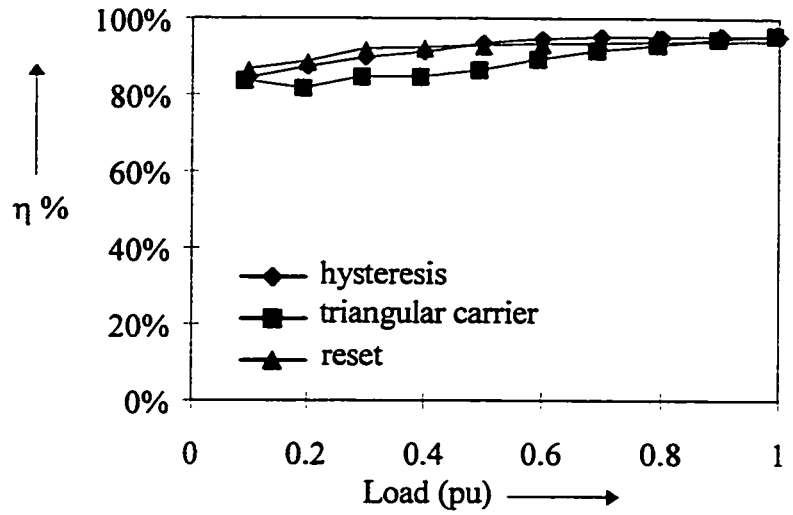


Fig. 4.19 Efficiency as a function of load (experimental results). Average f_{SW} = 40 kHz, input voltage = 120V, output voltage = 90V, resistive load.

4.6 Conclusions

In this chapter, a quantitative analysis based on average switching function is performed. An average model of the power supply waveforms is considered, neglecting the switching frequency harmonics. This provides the explanation for the power supply waveforms. The maximum input power factor and input current total harmonic distortion obtained for a certain level of the input source voltage is calculated. A performance comparison of three PWM pattern generation and control techniques has been done. The performance features are compared based on the indices such as input current Total Harmonic Distortion and input power factor. Of the three proposed PWM techniques, the one-cycle reset integral technique has produced the best overall results, including output voltage tracking.

CHAPTER 5

POWER CIRCUIT DESIGN

5.1 Introduction

A comparison of various PWM pattern generation and control techniques for the proposed power supply topology was performed and it was found that the One-cycle Reset integral control technique produced the best overall results in terms of power factor (PF), Total Harmonic Distortion (THD) and efficiency (η) [25].

This chapter presents detailed analysis and design curves that are required to implement a single phase trapezoidal ac power supply based on One-cycle Reset Integral control technique for hybrid fiber/coax networks. A design procedure to select and rate components of the power circuit is illustrated by means of a design example [26].

A power circuit realization of the proposed power supply based on the One-cycle Reset Integral PWM pattern generator, required to produce a trapezoidal output voltage is illustrated. Detailed circuit description is followed by the design considerations for the power circuit. Finally the design procedure is illustrated using a design example.

5.1.2 Circuit Description

The converter circuit as shown in Fig. 5.1, consists of the following :

1) *Input Filter* : The input filter is comprised of high frequency capacitors C_{S1} and C_{S2} and an inductor L_{S1}. This filter is used to filter out the high frequency harmonic components of the input current and also the conducted EMI.

2) *Diode Rectifier Bridge* : The diode rectifier bridge consisting of the diodes D_1 to D_4 is used to convert the input ac line voltage to an unregulated dc voltage across its output terminals.

3) *DC bus Capacitor* C_{bus} : The dc bus capacitor C_{bus} performs two functions; (a) it partially filters out the high frequency current harmonics being injected to the supply bus due to the operation of the high-frequency inverter; (b) it serves to decouple the high switching frequency PWM inverter stage from low frequency diode-bridge rectifier stage.

4) *Full-bridge PWM Inverter* : The single-phase PWM inverter consists of four power semiconductor MOSFET switches S_1, S_2, S_3 and S_4 connected in a full-bridge configuration. It is pulse-width modulated to convert the unregulated dc voltage into a regulated trapezoidal-shaped ac output voltage waveform.

5) Output Filter : The output filter consists of an inductor, L_o, and capacitor, C_o . Its function is to filter out higher order harmonics generated due to the operation of the high-frequency inverter. The relative values of the filter components is chosen such that only the higher order harmonics are completely attenuated whereas the lower order harmonics are unaffected.

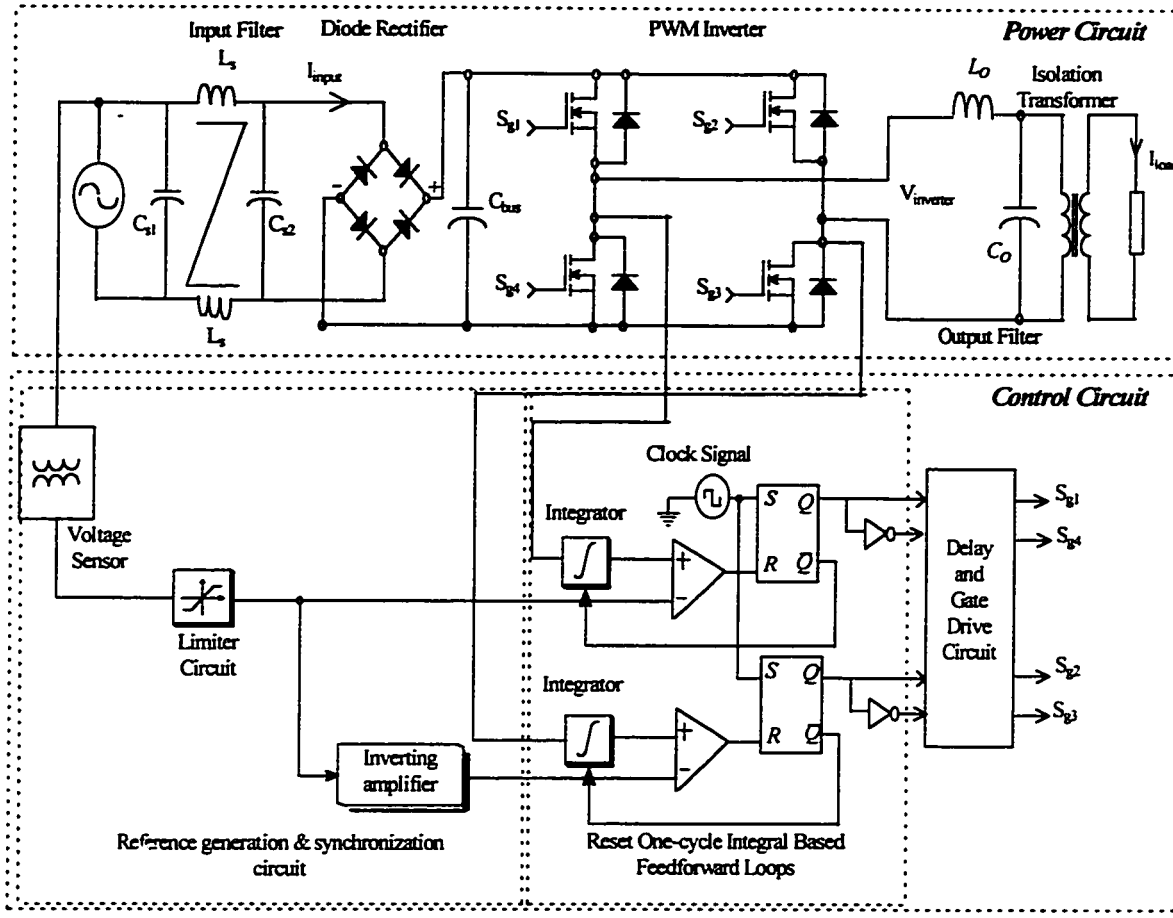


Fig. 5.1 One-cycle Reset Integral PWM Controlled Sine Wave ac to Trapezoidal Wave ac Power Supply.

6) *Isolation Transformer :* As the name implies, this transformer is used to isolate the load from the high frequency inverter and also step-up the voltage to meet the output voltage requirements.

7) *Control Circuit* : The configuration of the control circuit of the proposed topology based on Reset or One-cycle control technique can be classified in two major sub-divisions :

(i) Reference Generation and Synchronization Circuit: The source voltage is directly sensed from the single-phase ac mains supply and passed through a limiter circuit to generate a trapezoidal-shaped reference signal. By generating the reference signal in such a manner, the trapezoidal-shaped reference is in phase and synchronized with the 120 Hz dc bus ripple. That is the zero-crossing of this reference signal corresponds to the zero-crossing of the dc bus ripple voltage.

(ii) Reset Integral based feedforward Loops : There are two such loops - upper loop and lower loop. Each consists of a Reset Integral PWM control block which further consists of a real-time resettable integrator, a comparator, a clock, and S-R flip-flop. The output of the clock signal is tied to the SET option of the two flip-flops. The PWM gating signals generated by the upper controller block is complementary fed to the two switches of the left leg of the full-bridge inverter whereas the output of the lower PWM controller is fed to the two switches of the right leg of the full-bridge inverter.

5.1.3 Design Considerations For Power Circuit

A. *Input Filter*

Fig. 5.2 shows the input current harmonic spectrum of the converter for various operating conditions. It can be observed that the input current has low frequency magnitudes 3^{rd}, 5^{th}, 7^{th}, 9^{th} as well as the higher switching frequency components and this satisfies the IEC-1000-3-2 requirements. The high frequency harmonic contents appearing in the input current are small enough and can be easily filtered out using a high frequency differential mode and common mode input filter, as per FCC Class A or Class

B requirements.

The value of the dc bus capacitance is chosen to be 10 uF. Owing to a small value of this capacitance, the shape of the output voltage waveform generated has significant effect on the shape of the input current waveform. This was substantiated in the Chapter 4 using switching function analysis.

Since a trapezoidal shaped waveform has all the low-order odd harmonics as its characteristic harmonics (such as 3rd, 5th, 7th, 9th etc.,) and the input current is a reflection of this output current waveform, the input current would essentially have all the low-order harmonic contents in addition to the high switching frequency harmonics.

B. *Diode bridge rectifier*

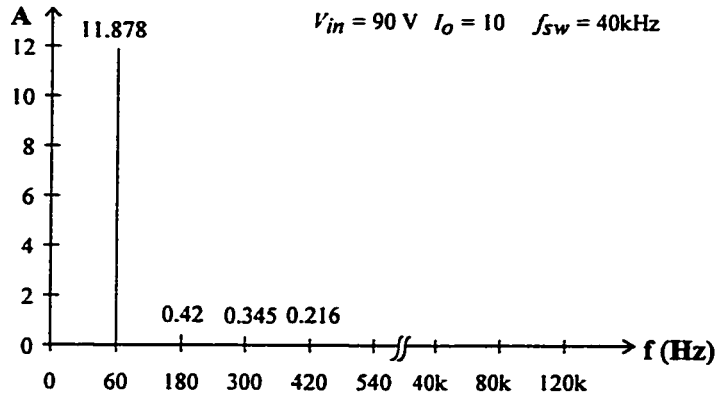
The selection of the diodes of the full bridge rectifier is based on their peak reverse voltage withstand capability and the maximum value of average current through them.

The average current through the diodes as a function of load for minimum and maximum input voltage with a dc bus capacitor of 10uF is illustrated in Fig. 5.3.

The average current through the diode increases proportionally as the load is increased from zero to twice its rated power. Therefore the average current rating of the diodes at rated load corresponds to minimum input voltage range and maximum output power.

The peak value of the voltage applied across each diode of the rectifier is equal to the peak value of the maximum input line voltage.

a)



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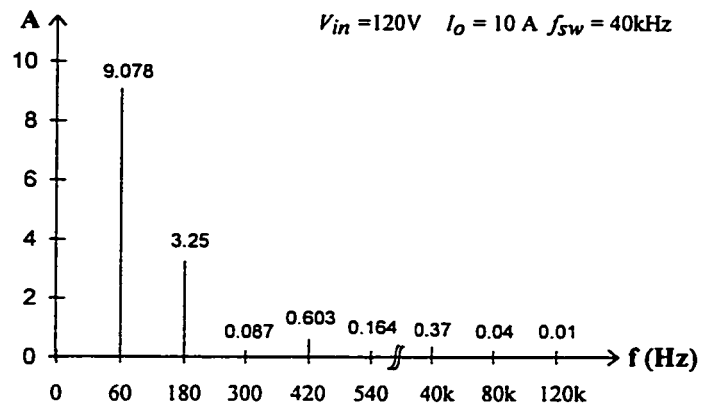

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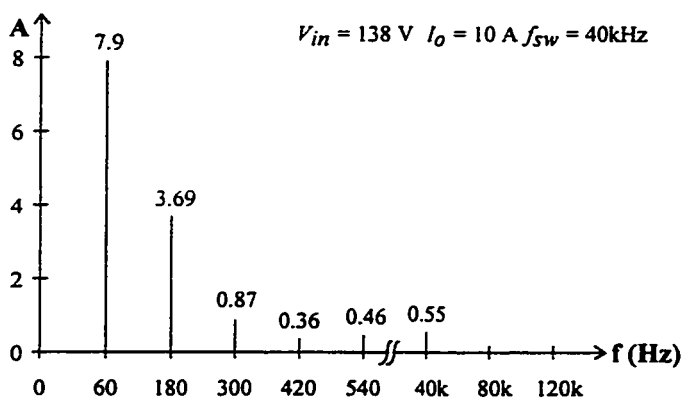


Fig. 5.2 The harmonic spectrum of the input current at rated load for various operating conditions at f_{sw}= 40 kHz, I_o= 10 amps at (a) V_i = 90 V (b) V_i = 120 V (c) V_i = 138 V.

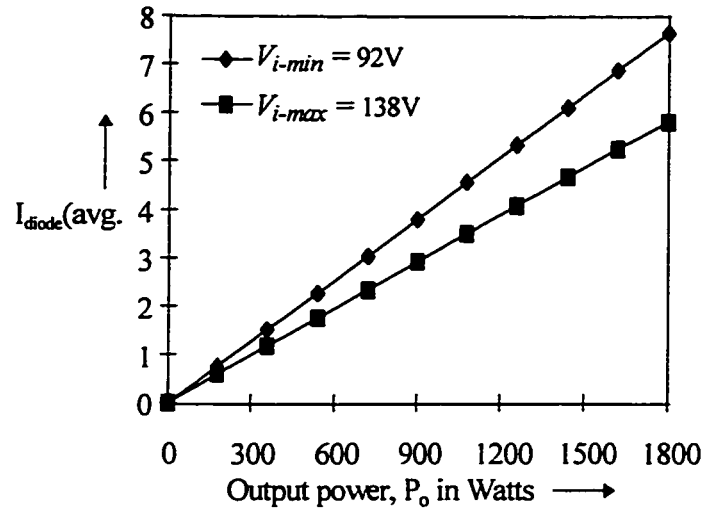


Fig. 5.3 Variation of average current through the rectifier diodes as a function of output power for minimum and maximum operating voltages (f_{SW} = 40 kHz, output voltage = 90 V, resistive load).

C. *DC bus capacitor*

The operation of the proposed power supply depends to a large extent on the dc bus capacitor. With a large dc bus capacitor, the current drawn from the ac source is peaky in nature hence resulting in a poor power factor and high input current total harmonic distortion.

Since the rectifier diodes are selected based on the average current through them, such a peaky current would be harmful.

The influence of the dc bus capacitance value on the power factor and input current THD is displayed in Fig. 5.4. It is clearly observed that as the capacitor value increases,

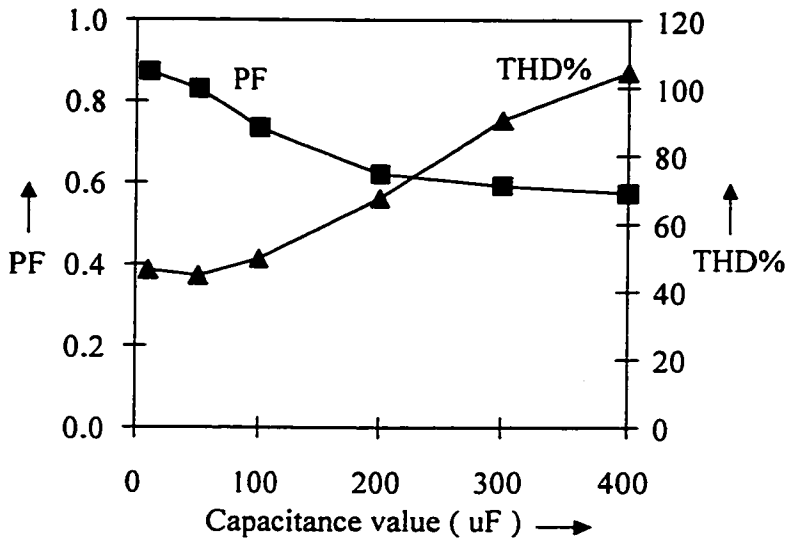


Fig. 5.4 Performance of the proposed power supply as a function of dc capacitor size (experimental results). (a) Power factor and Input current THD. (f_{SW} = 40 kHz, input voltage = 120 V, output voltage = 90 V, output voltage = 90 V, resistive load).

the power factor decreases, from 0.936 at 10 μF to 0.632 at 400 μF whereas the THD increases almost linearly from 36.65% at 10 μF to 90.34% at 400 μF. Therefore a minimum value equal to 10 μF is chosen for the dc link capacitor. Besides providing a buffer between the inverter and rectifier stage, the dc bus capacitor serves to filter out the high frequency ripple current being injected to the ac source as a result of high switching frequency inverter. The rms current rating of the capacitor is plotted as a function of load for minimum and maximum input source voltage (Fig. 5.5).

It can be observed from Fig. 5.5 that with the increase in the output power, the rms current flowing through the dc bus capacitor also increases linearly. The dc bus capacitor of 10 uF is not sufficient to bypass all the high order switching frequency harmonic current through it. Therefore significant amount of switching frequency harmonic components appear in the input current of the power supply.

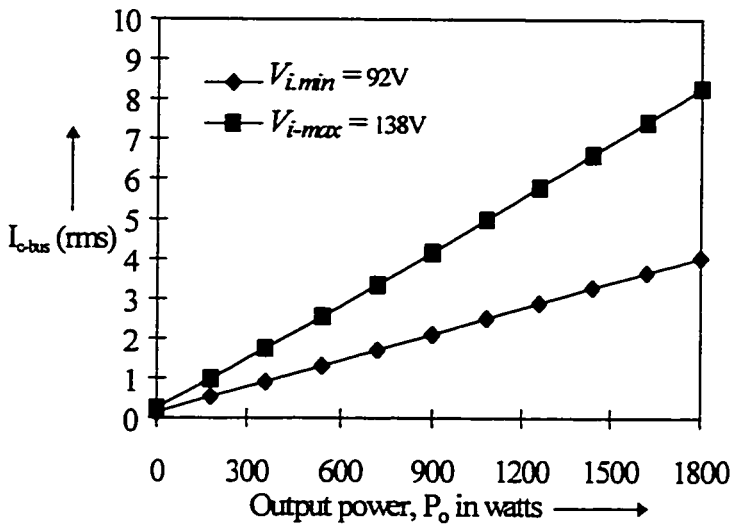


Fig. 5.5 Variation of rms current through the dc bus capacitance as a function of output power for minimum and maximum operating voltages.(f_{SW} = 40 kHz, output voltage = 90V, resistive load).

Larger the value of the dc bus capacitor, lower would be the impedance offered to the higher order harmonics and the input current would have less distortion. But a larger value the capacitor would reduce the pf and worsen the input current THD. Therefore a trade-off has to be achieved in order to select a particular dc bus capacitor value. Based

on this trade-off, the dc bus capacitor having a value of 10 uF was chosen.

D. *Selection of MOSFETs of the full-bridge Inverter*

The modes of operation of the PWM inverter is displayed in Fig. 2.10 in which it can be observed that the rms current flowing through the lower switches is greater as compared to the rms current flowing through the upper switches. Further the Fig. 5.6 shows the variation of rms current flowing through these switches as a function of load for minimum and maximum level of input voltage.

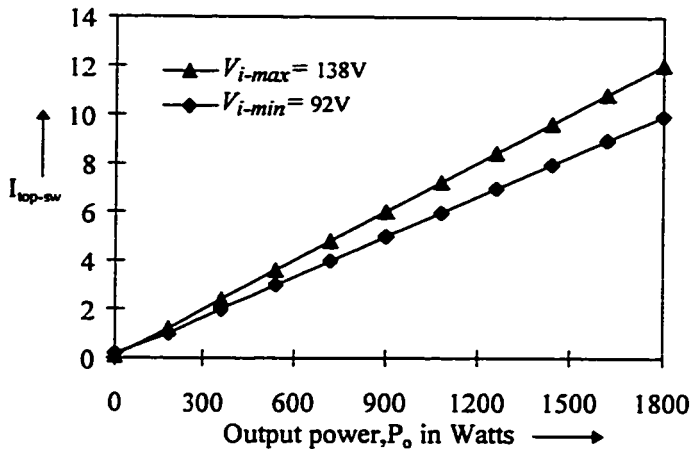
E. *Output Filter*

Fig. 5.7 shows the harmonic spectrum of the unfiltered output voltage for input line voltage of 90 V, 120 V, 138 V, respectively.

The break-frequency of the second-order low-pass output filter is chosen to be one-tenth of the switching frequency. Consequently, the attenuation offered to the higher-order harmonics is high whereas the lower-order characteristic harmonics of a trapezoidal waveform remain unaffected.

The transfer function of the second order filter with resistive load is given by the following equation:

a)



b)

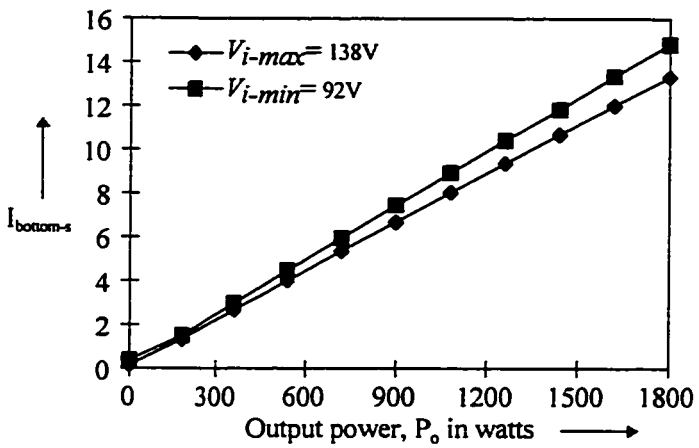


Fig. 5.6 Variation of rms current through the MOSFETs of the full-bridge inverter as a function of output power for minimum and maximum supply voltages.(f_{SW} = 40 kHz, output voltage = 90 V, resistive load). (a) current through the top switches (b) current through the bottom switches.

$$v_o(\omega) = \frac{1}{\sqrt{\left\{\left(1-\omega^2 \cdot L \cdot C\right)^2 + \left(\frac{\omega \cdot L}{R}\right)^2\right\}}} \cdot v_i(\omega) \qquad (5.1)$$

By selecting the appropriate break-frequency and using (5.1), the suitable value of L_o and C_o can be chosen.

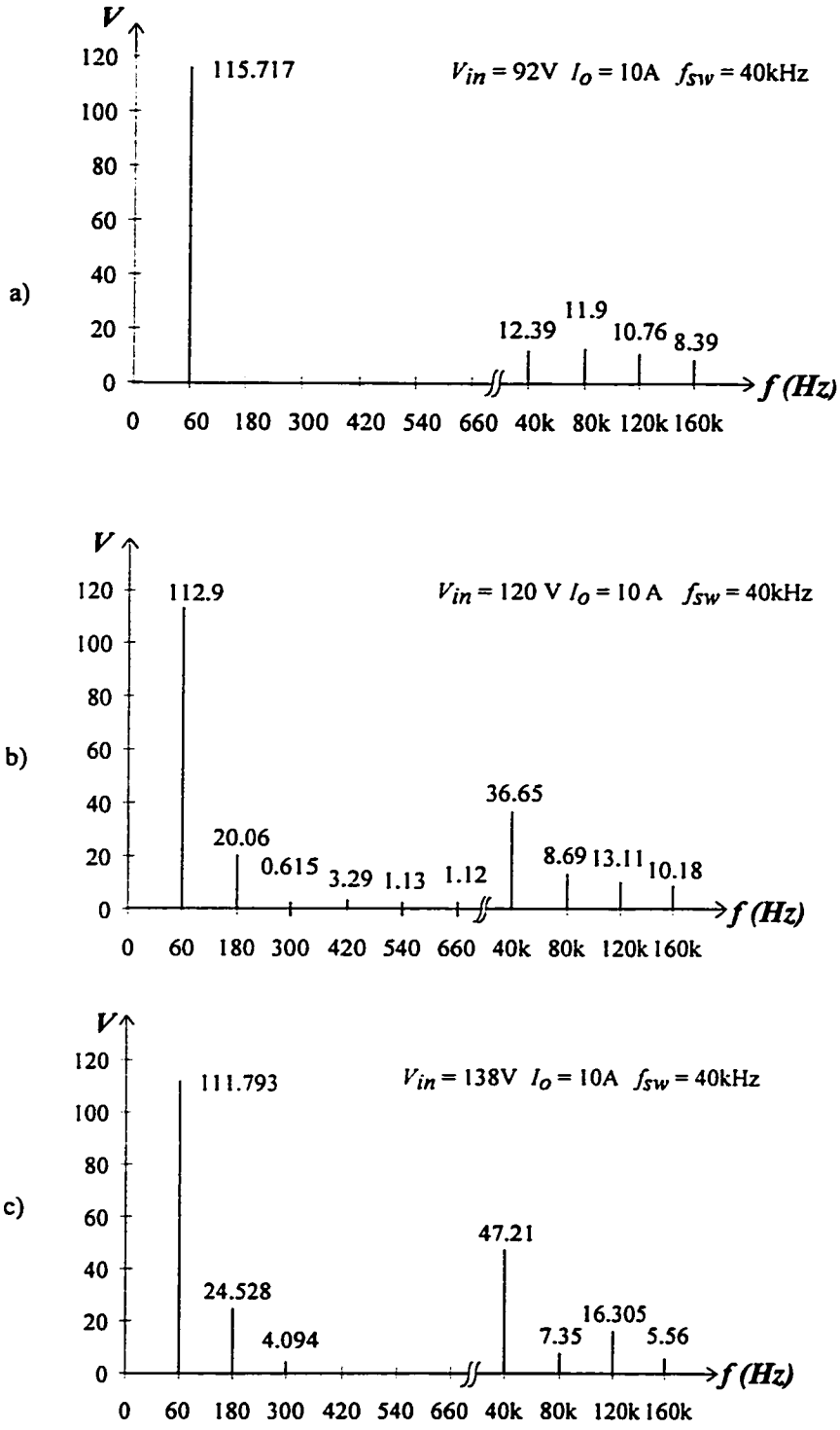


Fig. 5.7 The harmonic spectrum of the output voltage at rated load for various operating conditions at f_{SW}= 40 kHz, I_O= 10 amps at (a) V_i = 90 V (b) V_i = 120 V (c) V_i = 138 V.

F. Isolation Transformer

The transformer at the output of the PWM inverter is a standard 60 Hz, 1:1.5 turns ratio used for stepping up the input voltage. This is essential because if the input line voltage goes below 90 V, the converter would not be able to regulate the output voltage equal to desired level. Further it also provides isolation to the load.

5.1.4 Design Example

A design example with the following specifications is illustrated to select and rate the components.

a) The rated output power (P_O) = 900 W.

b) The rated input voltage range (V_{in}) = 92 V-138 V rms.

c) The rated output voltage (V_O) = 90 V rms (Trapezoidal waveshape).

d) The rated operating frequency (f_{SW}) = 40 kHz.

1) *Selection of input filter components*: During the input filter component selection it is important to make sure that the resonant frequency of the input filter is lower than the working frequency of the power supply.

Based on the above consideration and the input line current harmonic spectrum as shown in Fig. 5.2, a value of C_{S1} = 0.1 μF, C_{S2} = 0.1 μF and L_S = 1mH has been chosen for this filter.

2) *Selection of the rectifier diodes*: According to the Fig. 5.3, the maximum rms current flowing through the rectifier diodes is 3.8 A and the maximum voltage applied across the

diodes is $138\sqrt{2}$ V. Based on the above specification, a rectifier bridge GBPC 25-06 is selected.

3) *Selection of the dc bus capacitor*: As shown in Fig. 5.4, a small capacitor of the order of 10 μF should be chosen. It should be able to carry 4.3 A of rms current through it and able to withstand peak output voltage across the terminals of the full-bridge rectifier.

4) *Selection of the MOSFETs of the full-bridge Inverter*: The power semiconductor switch (IRFP 250) with the following specifications is the most suitable for the design of the inverter system under consideration.

The Drain-to-source Breakdown Voltage = 200 V

The on state resistance of the MOSFET = 0.085 Ω

The continuous Drain current, V_{GS} @ 10 V = 30 A

Rise time = 86 ns.

Fall time = 62 ns.

5) *Selection of the output filter components*: Based on the considerations of the break-frequency and using (5.1), it is observed that if we choose L_O = 200 μH and C_O = 10 μF at 40 kHz of operating frequency, the low frequency components inherent to a trapezoidal are unaffected and the high frequency harmonic components are completely attenuated.

5.1.5 Conclusions

In this chapter, design considerations of a single phase trapezoidal ac power supply for hybrid fiber/coax network based on One-cycle Reset Integral control technique has

been presented. A detailed design procedure to select and rate the components of the inverter system has been illustrated by means of a design example.

CHAPTER 6

CONCLUSIONS

6.1 Conclusions

Conventional ac to ac power supplies with power factor correction use an intermediate stage such as a boost regulator between the rectifier and the inverter. In this thesis a novel power supply topology is proposed which achieves increased efficiency by eliminating the intermediate power factor correction stage while maintaining high power factor. It does not require either a boost stage or a large dc bus capacitor; it uses a voltage-controlled inverter in the output stage, in which the PWM modulating function is synchronized with the dc capacitor voltage ripple.

In this thesis, it has been demonstrated that, with a small dc bus capacitor and an appropriate PWM pattern generator and control technique, high input power factor and high overall efficiency can be achieved for a power supply producing a trapezoidal output waveform.

Three voltage controlled PWM pattern generator and control techniques such as hysteresis integral control, triangular-carrier integral control and one-cycle integral control technique are identified and compared. Of the three proposed PWM techniques, the one-cycle reset integral technique has produced the best overall results, including output voltage tracking. The proposed power supply based on one-cycle reset integral

technique is therefore a viable alternative to systems using a boost intermediate stage for meeting new power factor and harmonic distortion standards and requirements. These schemes can be used as voltage pre-regulators for feedback loop design.

Average switching function analysis is presented which provides the quantitative explanation of the power supply waveforms. A detailed design procedure to select and rate the components of the power supply has been illustrated by means of a design example. Further, the control circuit implementation details have been also highlighted. Finally, the performance of the proposed topology is experimentally evaluated in terms of input power factor, input THD and efficiency.

6.2 Suggestions for further research work

There is a scope of further research in this thesis. In particular:

- to stabilize the switching frequency of the hysteresis control technique, without increasing the complexity of the overall circuit [ ].
- to compare the performance of the conventional power supplies required to power hybrid fiber/coax networks using a ferroresonant transformer [ ] with that of the proposed topology.

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APPENDIX

A.1 Calculation of the rms current drawn by the power supply

The objective of the analysis is to derive the approximate rms values of the input line current drawn by the power supply and the rms current through the dc bus capacitor analytically. This analysis utilizes the concept of switching function analysis and neglects the higher switching frequency harmonics.

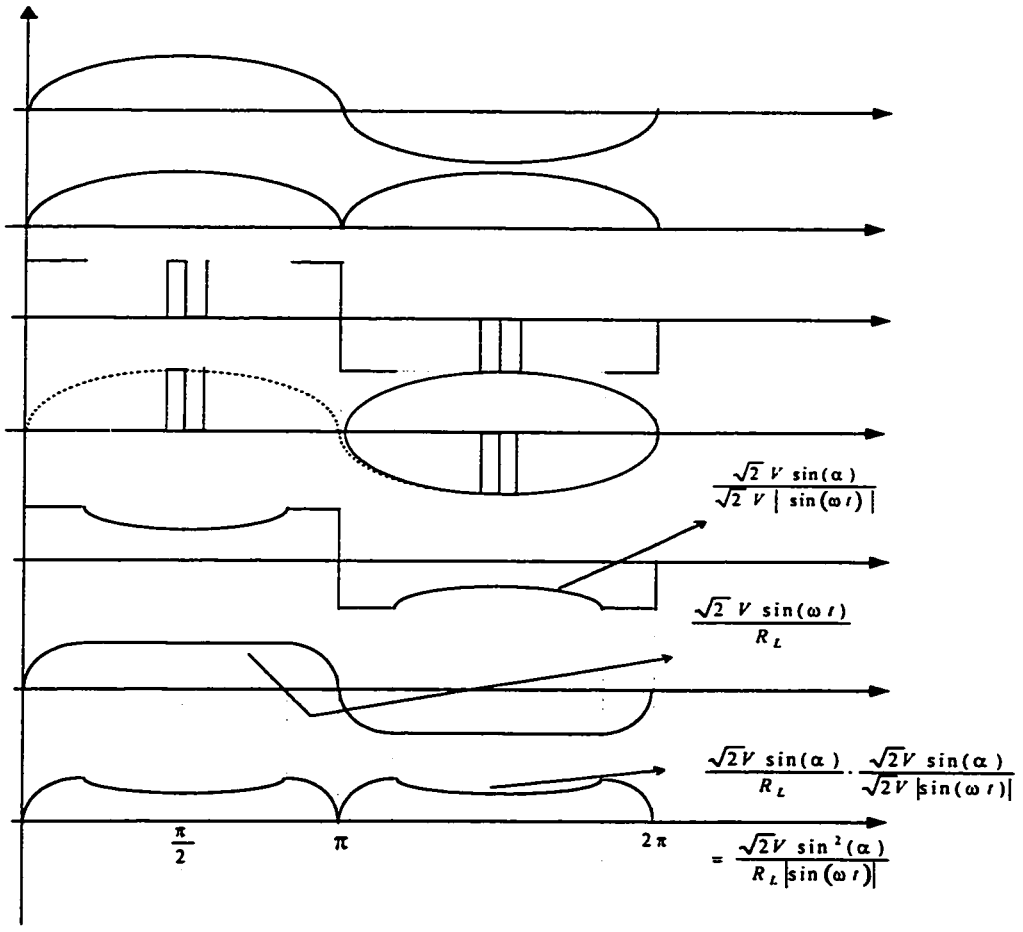


Fig. A.1 Various waveforms of the power supply.

The proceedure is as follows: The expression for the rms value of the voltage generated at the output is expressed as a function of input source voltage and clipping level angle α. For a given nominal input rms source voltage and output rms voltage, α is found out. For the given value of the α, the output rms voltage is calculated.

In the similar way, the rms value of the current through the capacitor is also calculated by inserting this value of α.

The clipping of the sinusoidal waveform takes place at an angle α and the voltage at that instant is represented by v_i where;

$$v_i = A\ sin(\alpha) \tag{A.1}$$

The rms value of the output voltage can be calculated as below;

$$v_{o\_rms} = \sqrt{\frac{1}{T}\int_0^T {v_o}^2\ \mathrm{dt}} \tag{A.2}$$

As can be obtained from the figure

$$v_{o\_rms} = \sqrt{\frac{4}{T}\left\{\int_0^{\alpha_1} A^2\ sin(\omega t) + A^2\left(\frac{\pi}{2}-\alpha\right)\ \sin(\alpha)^2\right\}} \tag{A.3}$$

as,

$$sin(x)^2 = \frac{1}{2}\cdot\left(1-cos(2\cdot x)\right) \tag{A.4}$$

$$\int_0^{\alpha} sin(x)^2 dx = \frac{1}{2}\cdot\int_0^{\alpha}\left(1-cos(2x)\right) = \frac{1}{2}\left(\alpha - \frac{sin(2\alpha)}{2}\right) \tag{A.5}$$

Inserting (A.4) in (A.3), we get

$$v_{o\_rms} = \frac{2A}{\sqrt{2\pi}}\sqrt{\left\{\frac{1}{2}\left(\alpha - \frac{sin(2\alpha)}{2}\right) + \left(\frac{\pi}{2} - \alpha\right)\sin(\alpha)^2\right\}} \quad \text{(A.6)}$$

This is the rms value of trapezoidal output voltage generated by the power supply

Given the nominal rms source voltage,

$$v_i = 120 \text{ V}$$

$$v_O = 90 \text{ V}$$

$$v_{o\_rms} = \frac{2A}{\sqrt{2\pi}}\sqrt{\left\{\frac{1}{2}\left(\alpha - \frac{sin(2\alpha)}{2}\right) + \left(\frac{\pi}{2} - \alpha\right)\sin(\alpha)^2\right\}} \quad \text{(A.7)}$$

$$\alpha = 38.57 \text{ deg.}$$

The rms value of the input current drawn by the power supply is derived as follows:

$$i_{s\_rms} = \sqrt{\left\{\frac{4}{2\pi}\int_0^{\alpha}\left(\frac{\sqrt{2}V_o}{R_L}\right)^2 sin(\omega t)^2 d(\omega t)^2 + \int_{\alpha}^{\frac{\pi}{2}}\left(\frac{\sqrt{2}V_o}{R_L}\right)\left(\frac{sin(\alpha)}{sin(\omega t)}\right)^2 d(\omega t)\right\}} \quad \text{(A.8)}$$

Further simplifying (A.8),

$$i_{s\_rms} = \frac{\sqrt{2}V_o}{R_L}\frac{2}{\sqrt{2}\sqrt{\pi}}\sqrt{\left\{\int_0^{\alpha} sin(\omega t)^2 d(\omega t) + sin(\alpha)^2\int_{\alpha}^{\frac{\pi}{2}}\frac{1}{sin(\omega t)^2}d(\omega t)\right\}} \quad \text{(A.9)}$$

Integrating the first term of (A.9)

$$\int_0^{\alpha} sin(\omega t)^2 d(\omega t) = \frac{\alpha}{2} + \frac{1}{8}\cdot cos(2\alpha) - \frac{1}{8} \quad \text{(A.10)}$$

Integrating the second term of (A.9)

$$\int_{\alpha}^{\frac{\pi}{2}} \frac{1}{sin(\omega t)^2} d(\omega t) = \left[-cot(\omega t)\right] = \frac{cos(\alpha)}{sin(\alpha)} \qquad (A.11)$$

Inserting (A.10) and (A.11) in (A.9)

$$i_{s\_rms} = \frac{2V_o}{\sqrt{\pi}\, R_L} \sqrt{\frac{\alpha}{2} + \frac{1}{8}\cos(2\alpha) - \frac{1}{8} + \frac{1}{2}\, sin(2\alpha)} \qquad (A.12)$$

For,

$$\alpha = 38.571 \text{ deg.}$$

$$R_L = 9 \text{ ohms}$$

$$i_{s\_rms} = \frac{2V_o}{\sqrt{\pi}\, R_L} \sqrt{\frac{\alpha}{2} + \frac{1}{8}\cos(2\alpha) - \frac{1}{8} + \frac{1}{2}\sin(2\alpha)} \qquad (A.13)$$

$$i_{s\_rms} = \frac{2 \cdot 120}{\sqrt{\pi}\, R_L} \sqrt{\frac{\alpha}{2} + \frac{1}{8}\cos(2\alpha) - \frac{1}{8} + \frac{1}{2}\sin(2\alpha)} \qquad (A.14)$$

$$i_{r\_rms} = 12.827 \text{ A}$$

A.2 Calculation of rms current through the bus capacitor

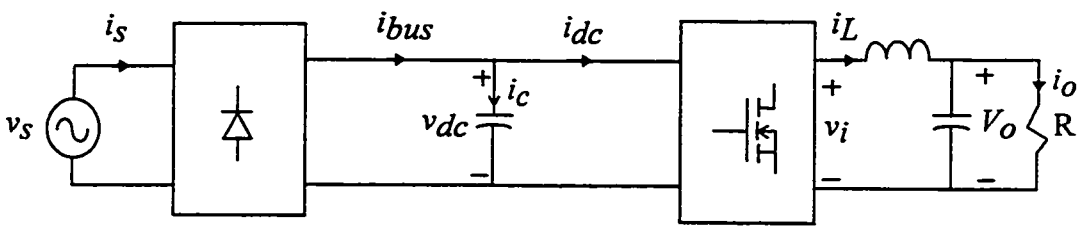
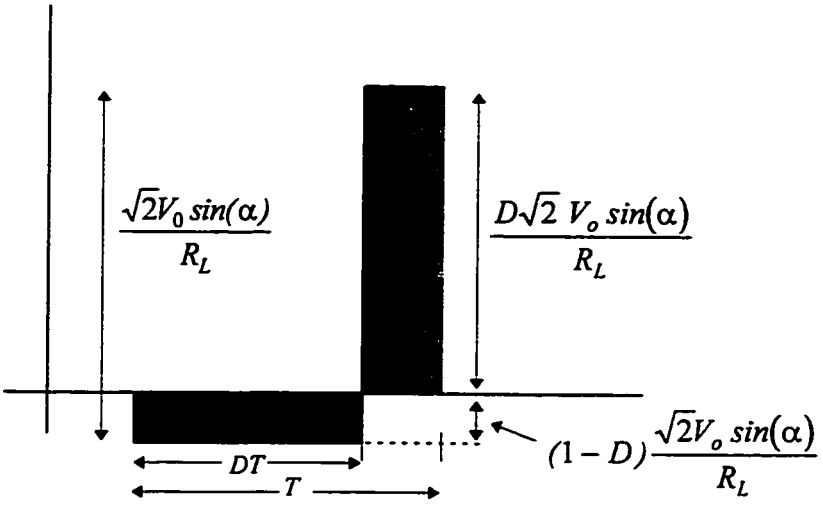


Fig. A.2 Power supply structure showing the various current and voltage waveforms.



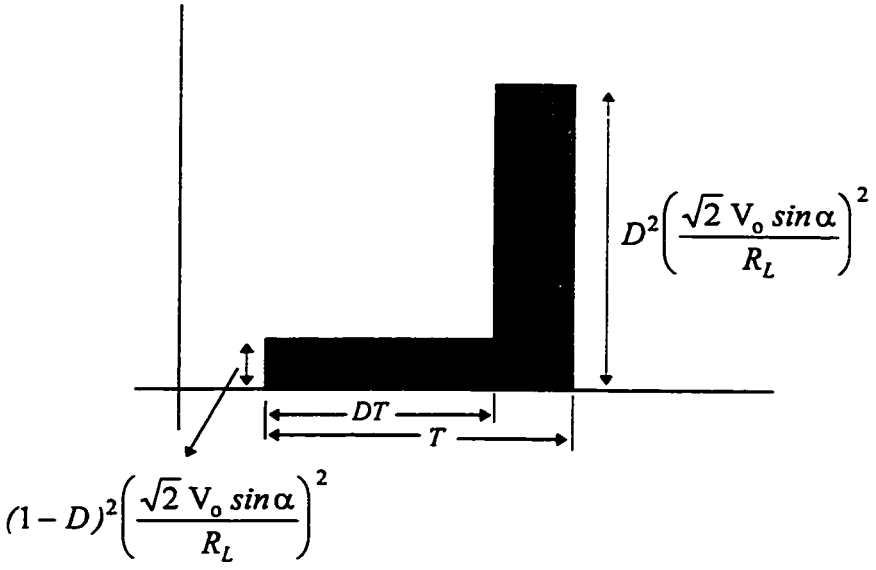
Let

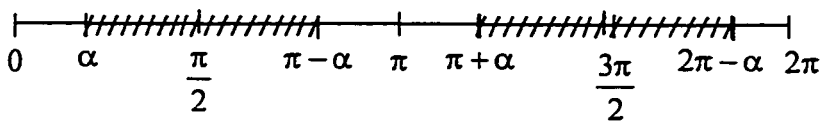
$$k = \frac{\sqrt{2}V_o \sin(\alpha)}{R_L} \tag{A.14}$$

$$(1-D)^2 k^2 DT + D^2 k^2 (1-D)T \tag{A.15}$$

$$= k^2 T\left\{D(1-D)^2 + (1-D)D^2\right\} \tag{A.16}$$

$$= k^2 DT(1-D)$$





The duty cycle is given by:

$$D = \frac{sin\alpha}{sin(\omega t)} \tag{A.17}$$

$$i_c = \sqrt{\frac{1}{T}\left(\text{area under } i_c^2\right)} \tag{A.18}$$

$$i_c = \sqrt{\frac{4}{T}\left(\text{area under } i_c^2\right)_{\alpha}^{\frac{\pi}{2}}} \tag{A.19}$$

$$= \sqrt{\frac{4}{T_s}} \sum_{\alpha,\alpha+\frac{2\pi}{\frac{T_s}{T}},\alpha+2.\frac{2\pi}{\frac{T_s}{T}}} \left(\frac{\sqrt{2}V_o\, sin(\alpha)}{R_L}\right)^2 T\left(1-\frac{sin(\alpha)}{sin(\omega t)}\right)\frac{sin(\alpha)}{sin(\omega t)} \tag{A.20}$$

$$i_{c\_rms} = \sqrt{\frac{1}{T}\int_{\alpha}^{\frac{\pi}{2}} i_c^2\, d(\omega t)} \tag{A.21}$$

$$\frac{1}{T_s} = 60 \text{ Hz};\ T_s = \frac{1}{60} \tag{A.22}$$

$$T = \frac{1}{40\cdot 10^3};\ \frac{1}{T} = 40 \text{ kHz} \tag{A.23}$$

$$R_1 = 9 \tag{A.24}$$

$$N = floor\left[\frac{\frac{\pi}{2}-\alpha}{\left(\frac{2\pi}{\left(\frac{T_s}{T}\right)}\right)}\right]; \text{N=95} \qquad \text{(A.25)}$$

$$i_{c\_rms} = \frac{2\sqrt{2}V_o \sin(\alpha)}{R_1}\sqrt{\frac{T}{T_s}}\sqrt{\left\{\sum_{n=0}^{N}\left(\left(1-\frac{sin(\alpha)}{sin\left(n.2.\frac{\pi}{\left(\frac{T}{T}\right)}\right)}\right)\frac{\sin(\alpha)}{\sin\left(2.n.\frac{\pi}{\left(\frac{T_s}{T}\right)}+\alpha\right)}\right)\right\}} \qquad \text{(A.26)}$$

A.2 Control Circuit Implementation

Figs. A.3 (a),(b) and (c) illustrate the schematic diagram of control circuit implementation for the proposed topology. The complete control circuit has been classified in three major sub-divisions, such as a) Reference generation and synchronization circuit b) Reset One-cycle Integral based feed-forward loops c) Delay unit and gate-drive circuit.

Fig. A.3(a) displays the practical implementation of the reference and synchronization circuit of the proposed power supply topology. The input voltage across

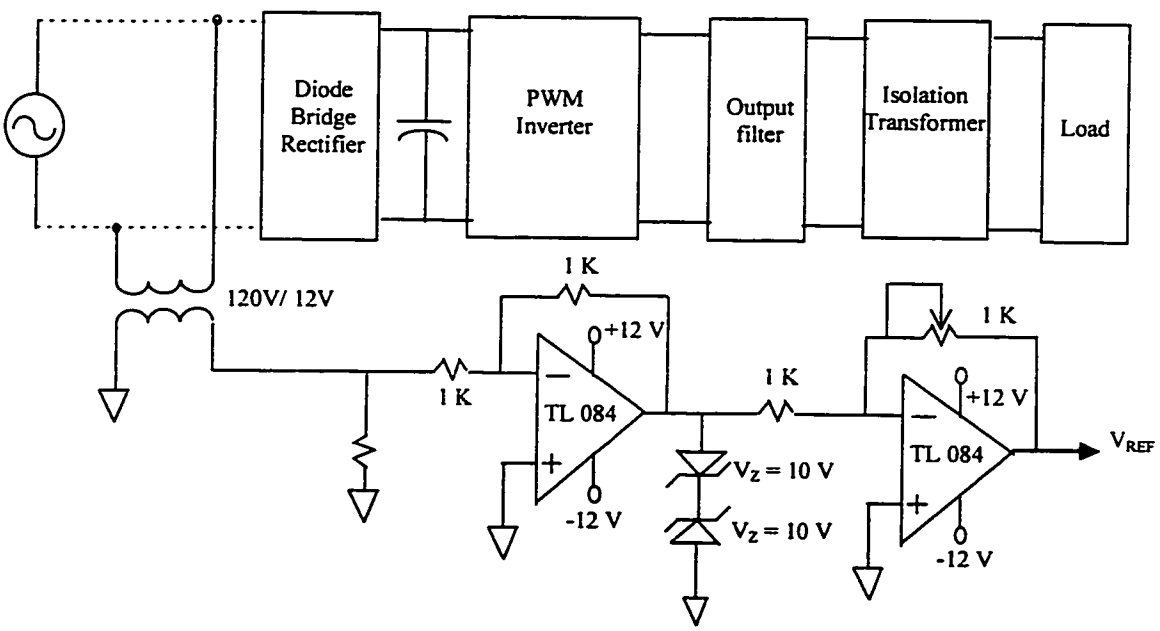


Fig. A.3 Implementation of Reference and Synchronization circuit

the ac source is directly sensed and is step-down using a standard 60 Hz step-down transformer to a voltage level suitable for a logic circuitry. The trapezoidal- shaped reference voltage waveform is then generated by passing the sensed sinusoidal voltage through the limiter circuit which is essentially a bipolar clipper circuit consisting of two back-to-back connected zener diodes. The gain of this trapezoidal-shaped reference waveform can be adjusted using a variable pot across the feedback of the TL 084 op-amp.

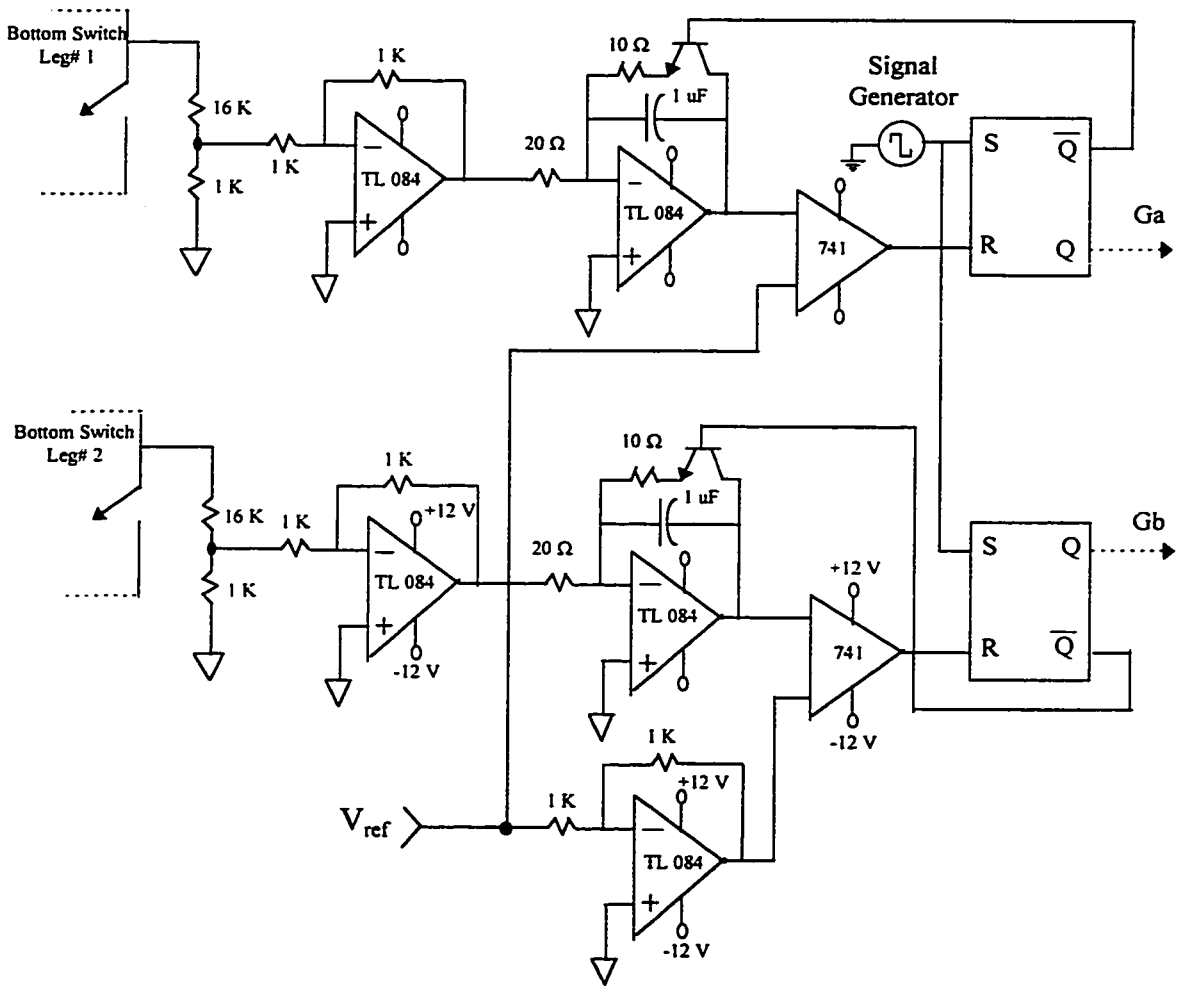


Fig. A.4 Implementation of Reset One-cycle Integral based Feedforward Loops.

The implementation details of the feedforward loops based on an One-cycle Reset Integral control technique are illustrated in Fig. A.3(b). The upper loop consists of a resistive potential divider connected across the lower MOSFET switch of the left leg of the PWM inverter to scale down the voltage to a level acceptable for logic and control circuitry. The voltage across the divider is fed to a real-time resettable integrator formed by connecting a BJT (2N2222) in series with a discharge resistance in the feedback path of the active integrator formed by an op-amp (TL 084). The integrated output is compared with a trapezoidal shaped reference signal by a IC comparator LM 741. The

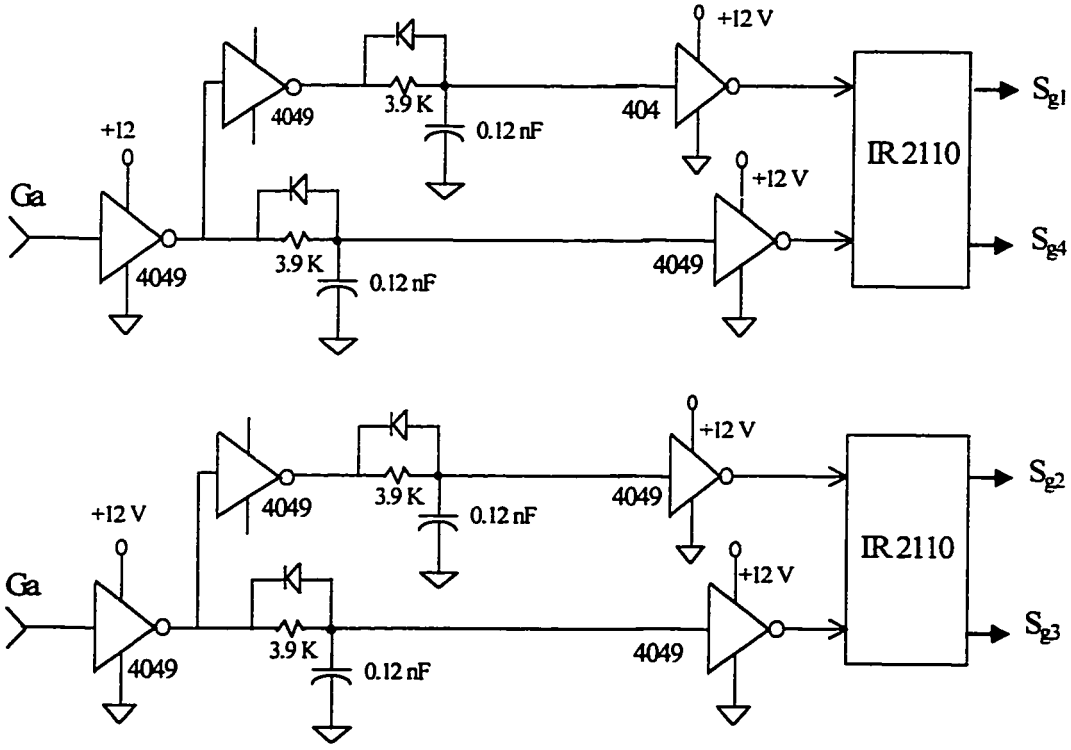
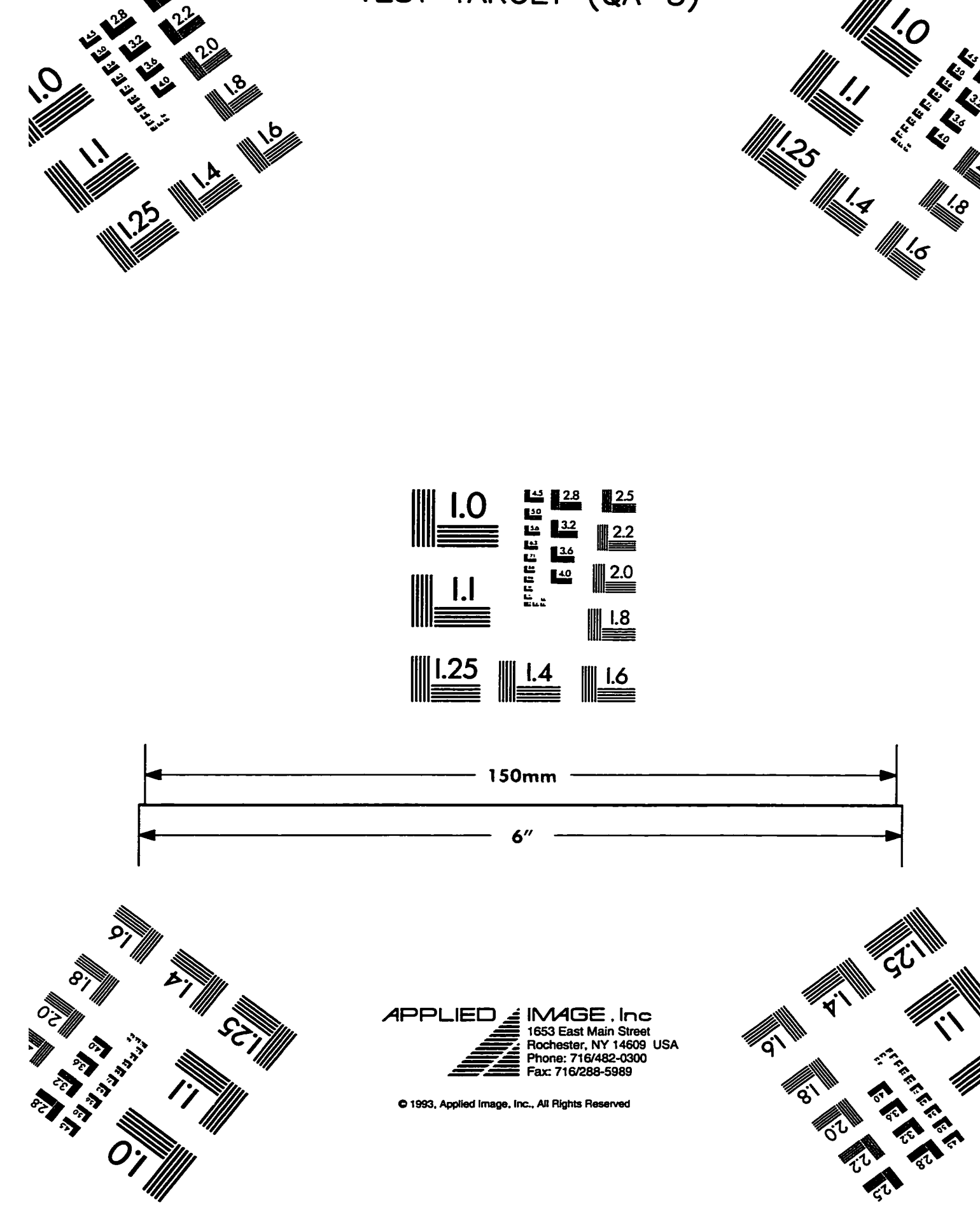


Fig. A.5 Implementation of Delay and Gate-drive Circuitry.

output of the IC comparator is connected to the Reset option of the S-R flip-flop. This flip-flop is set by a function generator or a clock obtained from a monostable multivibrator timer IC 555. The complimentary output is connected to the base of the BJT whereas the actual output goes to the delay unit and gate drive circuitry. The lower loop is similar to the upper one but in the lower loop the voltage is sensed across the bottom switch of the right leg of the inverter and also the integrated output is compared with an inverted trapezoidal-shaped reference signal.

The delay unit Fig. A.3(c) is formed by connecting a reverse diode across the resistor of the simple RC network. The delayed signal is fed to a gate-drive IC 2110 which gates the two MOSFET switches complimentary of one leg of the PWM inverter. The other gate drive IC IR 2110 drives the other two switches complimentary of the other leg of the same inverter.



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