DISTRIBUTED POINT-OF-USE POWER SUPPLY ARCHITECTURES FOR LOW-VOLTAGE SEMICONDUCTOR CIRCUITS

Youhao Xi

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy at
Concordia University
Montréal, Québec, Canada

August 2003

ABSTRACT

Distributed point-of-use power supply architectures for
low-voltage semiconductor circuits

Youhao Xi, Ph.D.
Concordia University, 2003

The low-voltage semiconductor circuit boards in advanced telecom systems require the power supplies to have some key features such as the very low voltage, very high current, very high slew-rate load transients, high power density and low cost. The objective of this thesis is to find solutions to satisfy these requirements without sacrificing the cost, efficiency and usable on-board space. In order to achieve this objective, this thesis proposes two distributed point-of-use power supply architectures (DPUPS) suitable for different configurations of the low-voltage semiconductor circuit boards.

In order to implement the proposed DPUPS architectures, this thesis presents two improved soft switching forward converter topologies (Type 1 and Type 2). These two topologies both employ the simplified power transformers that achieve self-reset without using the conventional resetting winding, and they both guarantee the soft switching under all operating conditions without complicating the control scheme.

Based on the two improved soft-switching converter topologies, two DPUPS architectures are developed. Both architectures have common merits such as the soft switching, single stage power conversion, minimized length of the high current PCB tracks and reduced PCB copper area, independent and tight voltage regulation at the point of load, instantaneous response to the system dc bus variations, elimination of the cross regulation between multiple outputs, inherent protection against overloading or the output

short-circuit condition, capable of high closed-loop bandwidth, and reduced number of power components for multiple output applications. In comparison between these two DPUPS architectures, the one that is implemented with the proposed Type 1 topology is optimal for a circuit board with the heavy current loads collocating, while the other one that is implemented with the Type 2 topology serves better for a circuit board with the heavy current loads distributed at different points.

In this thesis, detailed steady state and small signal analyses are performed, the performance of the proposed architectures are characterized, and the design procedures are generated. Simulation and experimental results obtained from prototype circuits are used to verify the analyses and design and to serve as the proof of concepts. The results indicate that the proposed DPUPS architectures provide promising solutions to satisfy the power requirements of the low-voltage semiconductor circuits.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my supervisor Dr. Praveen K. Jain for his guidance, inspiration, encouragement, friendship and strong support, during the course of this study.

My colleagues in the P. D. Ziogas Power Electronics Lab have always amazed me with their kindness, help and encouragement, with many valuable discussions we have shared as well as with unforgettable group activities. Special thanks to Mr. Joseph Woods for his help with grammatical correction of the thesis text, and also for his technical support over the years.

I would also like to thank Mr. George Spak at Pulse Engineering, Inc., Kanata, Ontario, for providing some optimized magnetics for a prototype converter.

Thanks extend to my employer, EMS Technologies Canada, Ltd., for the permission of my leave-of-absence of six months in 2002, which enabled me to focus on some issues of this work.

The financial support from the Natural Sciences and Engineering Research Council of Canada (NSERC) is gratefully appreciated.

The love and support from my family, and the joy with my two lovely children, both of whom were born during the course of this study, are crucial for me to complete this work.

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LIST OF ACRONYMS

AC	Alternating Current
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DPUPS	Distributed Point-of-Use Power Supply
EMI	Electromagnetic Interference
EA	Error Amplifier
FF	Feed-Forward
FB	Feedback
HVLC	High Voltage Low Current
IC	Integrated Circuit
LVHC	Low Voltage High Curent
Magamp	Magnetic Amplifier
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PUPS	Point-of-Use Power Supply
PWM	Pulse Width Modulation
RMS, rms	Root Mean Square value
SR	Synchronous Rectifier
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

LIST OF PRINCIPAL SYMBOLS

α Intermediate variable, equal to the product of $L_aC_aL_eC_{snb}$, or $L_aC_aL_{R1}C_{snb}$, depending on the referred circuit in this thesis.

β Intermediate variable, equal to the sum of products $L_eC_{snb}+L_eC_a+L_aC_a$, or $L_{R1}C_{snb}+L_{R1}C_a+L_aC_a$, depending on the referred circuit in this thesis.

δ the factor by which the steady state drain-to-source voltage of S_{main} deviates from the input voltage V_d at the beginning of each switching cycle

η_{rect} efficiency of the rectification stage of a converter

ΔI_{mj} net change of the magnetizing current in the arbitrary j^{th} interval

Δ_{j1} reduction of the effective duty ration by L_{sj} or L_{Rj1}

Δ_{j2} transition duration of the secondary current after S_{main} is turned off, in a fraction of a switching cycle

Δ_{j3} transition duration of the current through the coupled inductor L_{Rj2}, in a fraction of a switching cycle

ω_1 resonant angular frequency given by $\sqrt{\beta/\alpha}$

ω_2 angular frequency of a resonance given by $1/\sqrt{\beta}$

ω_3 angular frequency of a resonance given by $1/\sqrt{L_aC_a}$

ω_4 angular frequency of a resonance given by $1/\sqrt{L_mC_{snb}}$

ω_5 angular frequency of a resonance given by $1/\sqrt{k^2L_sC_{snb}}$

ω_6 angular frequency of a resonance given $1/\sqrt{L_{R1}C_{snb}}$

A_e effective cross-section area of T_P magnetic core

B_{sat} flux density saturation point of a magnetic core

$B_{\max}$ the upper boundary of the flux excursion of T_P

$B_{\min}$ the lower boundary of the flux excursion of T_P

C_a capacitor of the resonant tank in the auxiliary circuit

C_{iss} MOSFET inherent gate-to-source capacitor

C_o output filter capacitor

C_{oss} MOSFET inherent drain-to-source capacitor

C_{snb} snubber capacitor of S_{main}

D_{a1} auxiliary rectifier diode in the auxiliary circuit

D_{a2} auxiliary rectifier diode in the auxiliary circuit

D_{o1} rectifier diode in the output stage

D_{o2} freewheeling diode in the output stage

D main switch S_{main}'s duty cycle

D_{aux} duty cycle of the auxiliary switch

D_{eff} effective duty cycle of the main switch in the forward topology

$D_{\max}$ maximum duty cycle of the main switch

$D_{\min}$ minimum duty cycle of the main switch

d simultaneous conduction interval of the pair synchronous rectifiers, in a fraction of a switching cycle

d_m S_{main} duty ration margin, in a fraction of a switching cycle

$\hat{d}$ small signal deviation of d in Laplace transformation

f_{co} cross over frequency of an open loop system

f_p a pole of a transfer function

f_{sw} switching frequency

f_z a zero of a transfer function

I_{aj} steady state current of the auxiliary circuit the end of the arbitrary j^{th} interval

$I_{d\max}$ peak drain current of S_{main}

I_{m0} steady state magnetizing current at the beginning of a switching cycle

I_o maximum output current

$I_{o\max}$ peak drain current of S_{main}

I_{pj} the steady state primary current at the end of the arbitrary j^{th} interval, j=1,2,…

i_a instantaneous current flowing through the auxiliary circuit

i_m instantaneous magnetizing current of T_p

i_p instantaneous primary current of T_p

i_s instantaneous secondary current of T_p

$\hat{i}_L$ small signal deviation of the output inductor current in Laplace transform

$\hat{i}_o$ small signal deviation of the output current in Laplace transform

j ordinal number

k power transformer T_p's turns ratio, namely N_p/N_s

k_a auxiliary transformer T_a's turns ratio

L_a inductor of the resonant tank in the auxiliary circuit

L_e equivalent inductor seen of the paralleled L_m and L_s from the primary side

L_m magnetizing inductor of T_p

L_o output filter inductor

L_{R1} current limiting inductor inserted into the primary circuit

L_{R2} the coupled inductor with L_{R1}

L_s current limiting inductor inserted into the secondary circuit

N_p primary winding of T_p, and also the number of turns of the winding

N_s secondary winding of T_p, and also the number of turns of the winding

N_{SR} number of MOSFETs to be paralleled to fulfill one SR

P_o output power

R_D on resistance of a power MOSFET

R_E Thevenin equivalent resistor

R_{ESR} output capacitor's equivalent series resistor

R_L output inductor's equivalent series resistor

R_M total primary circuit resistance

R_o load resistance

R_{SR} synchronous rectifier on-state resistor

S_{main} main switch MOSFET

S_{aux} auxiliary switch MOSFET

SR_{j1} rectification synchronous rectifier in the arbitrary j^{th} output circuit

SR_{j2} freewheeling synchronous rectifier in the arbitrary j^{th} output circuit

s Laplace transform operator

T_a auxiliary transformer

T_p power transformer

T_s switching cycle (equal to $1/f_{sw}$)

t time

t_0 the beginning of the switching cycle under analysis

t_j the end time of the arbitrary j^{th} interval under analysis, j=1,2,…

u_a instantaneous voltage across C_a

u_{d1} instantaneous drain-to-source voltage of S_{main}

V_{a0} steady state voltage across C_a at the beginning of each switching cycle

V_{aj} steady state voltage across C_a at the end of the arbitrary j^{th} interval

V_{end} steady state drain voltage of S_{main} at the end of a switching cycle

V_d input dc voltage

$V_{d\max}$ the maximum input dc voltage

$V_{d\min}$ the minimum input dc voltage

V_o nominal output voltage

V_{pk} peak of S_{main}'s drain voltage

V_{REF} reference voltage

V_s peak value of the secondary voltage of T_p

V_{sw} peak-to-peak voltage of the saw-tooth signal in the PWM control unit

V_{Th} Thevenin equivalent voltage

v_c instantaneous voltage across C_o excluding ESR

v_o instantaneous output voltage

v_s instantaneous secondary voltage of T_p

$\hat{v}_o$ small signal deviation of V_o in Laplace transform

CHAPTER 1

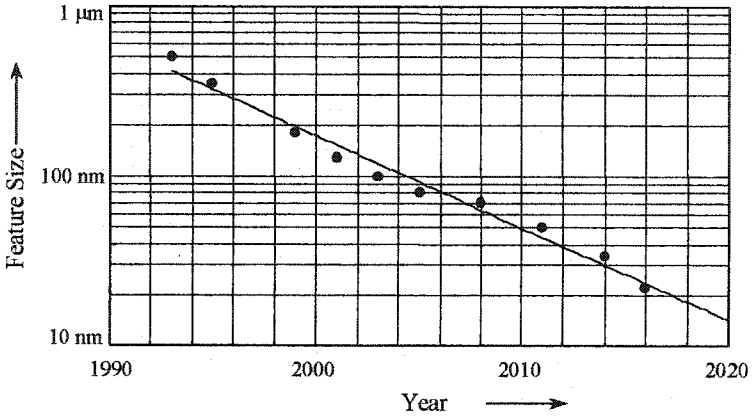
INTRODUCTION

1.1 TRENDS IN SEMICONDUCTOR TECHNOLOGY

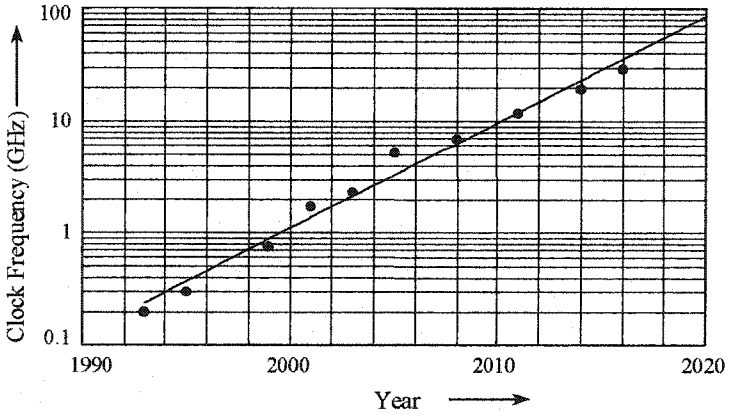
For the last few decades, semiconductor technology has been advancing along the trajectory predicted by Moore's Law, namely the scale of integration of transistors in integrated circuits (ICs) doubles every 18 months. Behind this trajectory is the continual shrinking of the poly-silicon gate's feature-size—the means by which a chip can integrate more gates to perform more complex functions at a higher speed.

According to the International Technology Roadmap for Semiconductors (ITRS) [1], such trends will continue as shown in Fig. 1.1 for at least another 15 years [1-4]. Similar technology roadmaps can be found from the Semiconductor Industry Association (SIA) [2]. According to Fig. 1.1a, in about 10 years, the feature size will be reduced from today's 0.13 μm to 50 nm, leading to a transistor density of up to 1.5 billion/cm^2 in a die. Meanwhile, as shown in Fig. 1.1b, the IC's internal clock frequency f_{CLK} will be raised up to a dozen Giga Hertz.

Following these trends is the continual production of higher performance microprocessors, memories, and application-specific integrated circuits (ASICs). These devices have benefited a wide range of applications. Typical examples are advanced telecommunication and computer systems, both of which are growing rapidly to meet increasing demands in data processing capability and data transfer bandwidth.

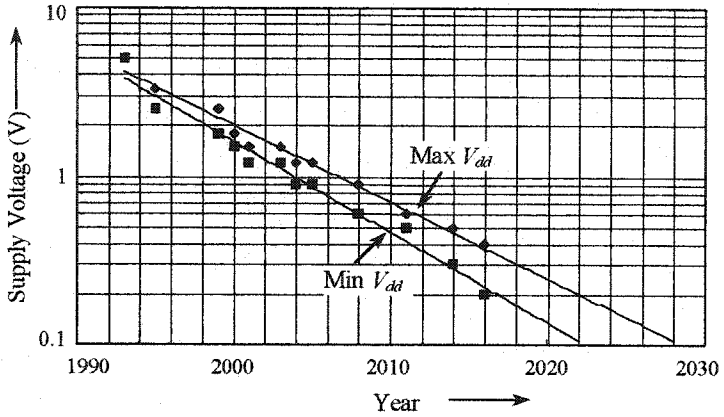


a. Feature size.

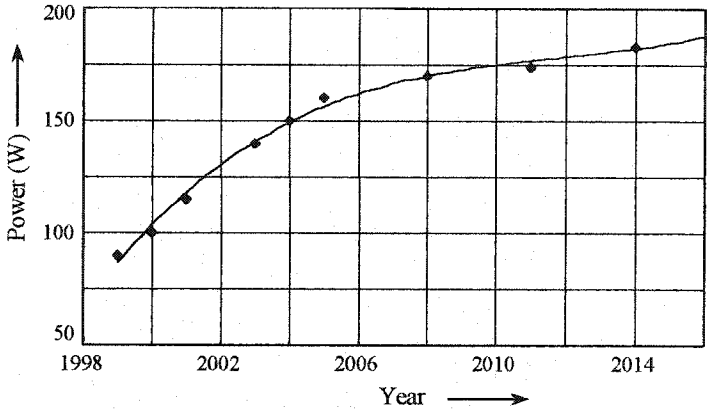


b. Clock frequency.

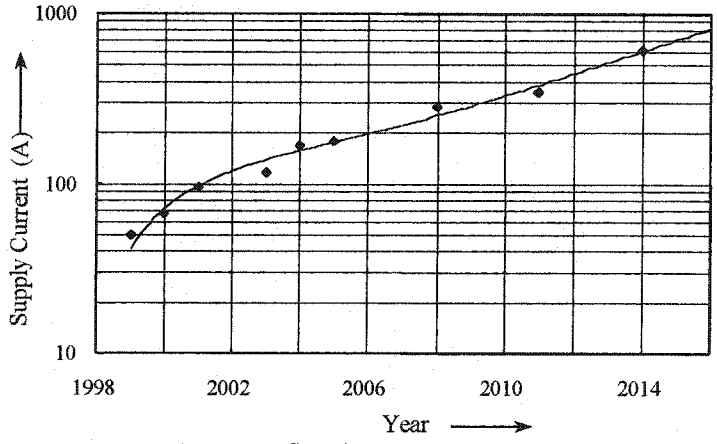
Fig. 1.1 Trends in Semiconductor Technology.



a. Supply voltage



b. Power per chip.



c. Supply current.

Fig. 1.2 Trends in the IC power requirements.

Along with these trends is the requirement for continuous reduction of the power supply voltage (V_{dd}) with which the new generation low-voltage semiconductor circuits can operate safely at very high clock frequencies. Such a requirement is driven by several factors, including the reduced channel length of the transistor, reliability of the gate dielectrics, and especially, the limitation of power consumption of an IC chip. This power limit is proportional to the product of $f_{CLK}V_{dd}^2$.

The ITRS also provides a roadmap for power requirements. This is shown in Fig. 1.2. When the supply voltage decreases, the power consumption of a single poly-silicon gate decreases. However, the total power consumption of an IC chip increases because of the increased number of gates integrated into the chip and the increased clock frequency. At a very low supply voltage, such an IC chip draws a very high current.

Specifically, according to Figs. 1.1 and 1.2, the maximum power per chip will be as high as 174 W when the very large scale integration (VLSI) process enters the generation of 50 nm around the year 2011, and all the power is fed into the chip at a V_{dd} as low as 0.5 V. This will require the power supply to provide about 350 A. Much higher current is required as the VLSI process advances into the 35 nm generation in 2014.

Another power issue arising from recent trends in semiconductor technology is the requirement of multiple supply voltages for most advanced ICs, especially the mixed-signal ASICs. These ICs' digital cores may run at a lower voltage while their I/O and the analog sections operate with a higher supply voltage. On the other hand, a circuit board may use different ICs that require different operating voltages. For instance, a microprocessor may operate at 1.8V while the memory works with 3.3V. Such a diversity of supply voltages on a single circuit board is mainly owing to the device availability and

high clock frequency. The slew-rate may go above 10000 A/μs in a multi-gegahertz circuit. If not treated properly, such high slew-rate transients may cause a power supply to lose output regulation. This in turn may affect the load at normal operation and even damage the load.

The new generation low-voltage semiconductor circuits bring some problems to the system's power distribution architecture. These problems include the power distribution efficiency for delivering the power at LVHC, the effects of PCB track impedance along the low voltage distribution paths, the flexibility in system upgrades with the continually decreasing supply voltage, limitation on costs, and ease of design, installation and maintenance.

Unfortunately, as will be seen in the next section, conventional power supplies and power distribution architectures in telecom systems are not always able to meet these new requirements. They become bulky, costly and inefficient in an attempt to satisfy the more demanding performance requirements. The objective of this thesis is to find solutions at both the level of the power supply topology and at the level of the power distribution architecture.

The rest of this chapter is arranged in the following five sections. A brief review of the existing power distribution architectures in telecom systems is given in Section 1.3 and their limitations are examined. Based on the review, the concepts of the distributed point-of-use power supply (DPUPS) architecture are introduced in Section 1.4. The applicability of existing power converter topologies in DPUPS is discussed in Section 1.5. The scope and objectives of the thesis are defined in Section 1.6, followed by the outline of the remainder of the thesis in Section 1.7.

1.3 CONVENTIONAL POWER DISTRIBUTION ARCHITECTURES

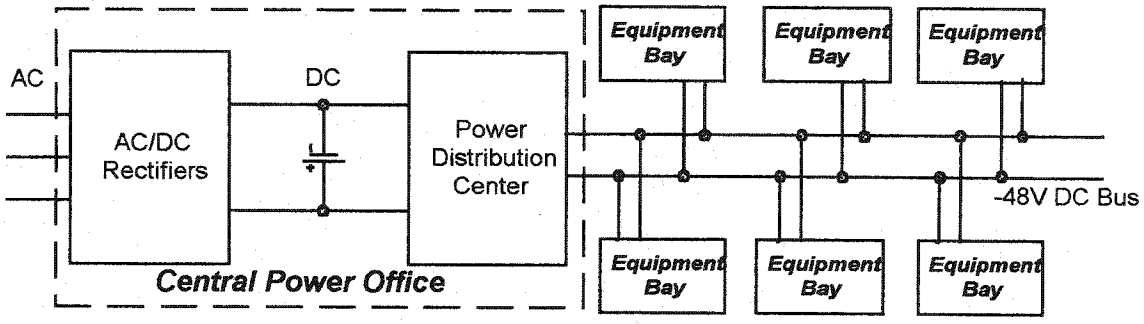
Telecom systems normally consist of equipment bays, if only hardware is mentioned. For instance, a telecom system [5-7] includes the local central offices, access tandem offices, transmission facilities, relay stations, and customer terminal offices. An equipment bay usually harbors many cabinets each holding a group of plug-in electronic circuit boards, or the so-called electronic cards. Fig. 1.3 shows the fundamental frame of power distribution in such a system [7], of which Fig. 1.3a depicts the system block diagram and Fig. 1.3b shows the configuration inside an equipment bay.

Inside the cabinet, there are two types of conventional power distribution architectures [7-23]. The first one uses the centralized power supplies, in which an on-shelf power supply resides in a cabinet to distribute the power to all circuit boards inside the cabinet. The second one is the decentralized power system in which each circuit board uses an on-board power supply, which is usually called the point-of-use power supply (PUPS). The following is a close look of these two architectures.

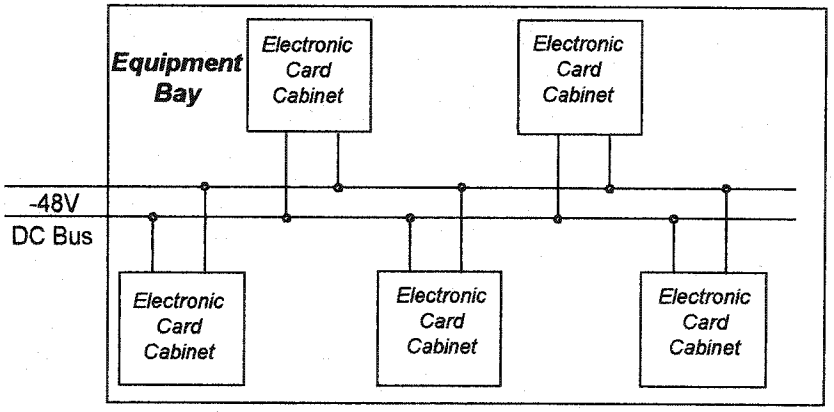
1.3.1 The Centralized Power Distribution Architecture

Fig. 1.4 shows the block diagram of a typical section of the centralized power distribution architecture in an electronic card cabinet. Each cabinet uses an on-shelf power supply [7, 12, 14-16] to convert the system dc bus voltage into the required operating voltages, and distributes these voltages through complex back-plane rails to all circuit boards inside the cabinet. All cabinets are parallel connected to the system dc bus.

The major advantages of the centralized power distribution architecture include the saving of on-board space used by the electronic cards, and cost effectiveness in terms of watts per dollar spent for a fully occupied cabinet.



a. The system block diagram



b. The equipment bay configuration

Fig. 1.3 The basic power distribution frame in the telecom systems.

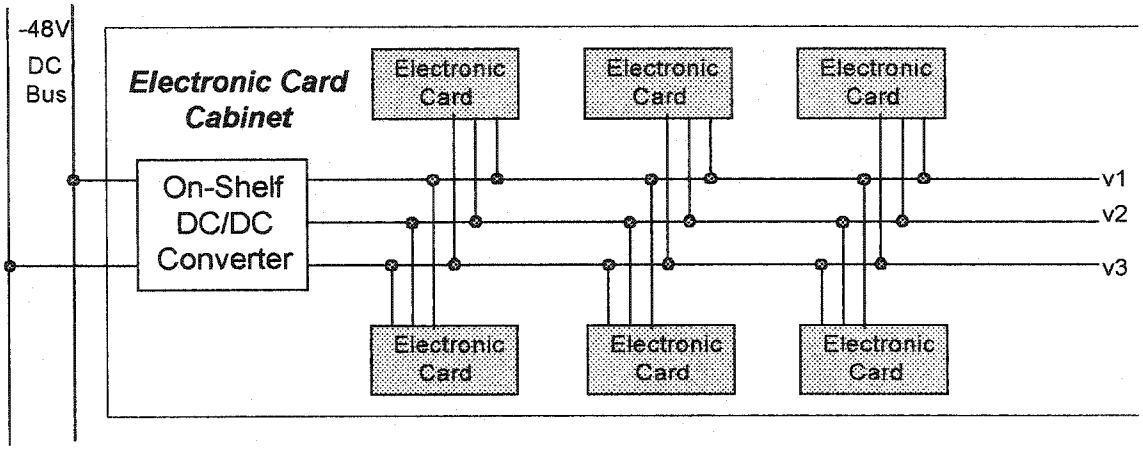


Fig. 1.4 The block diagram of the centralized power distribution architecture.

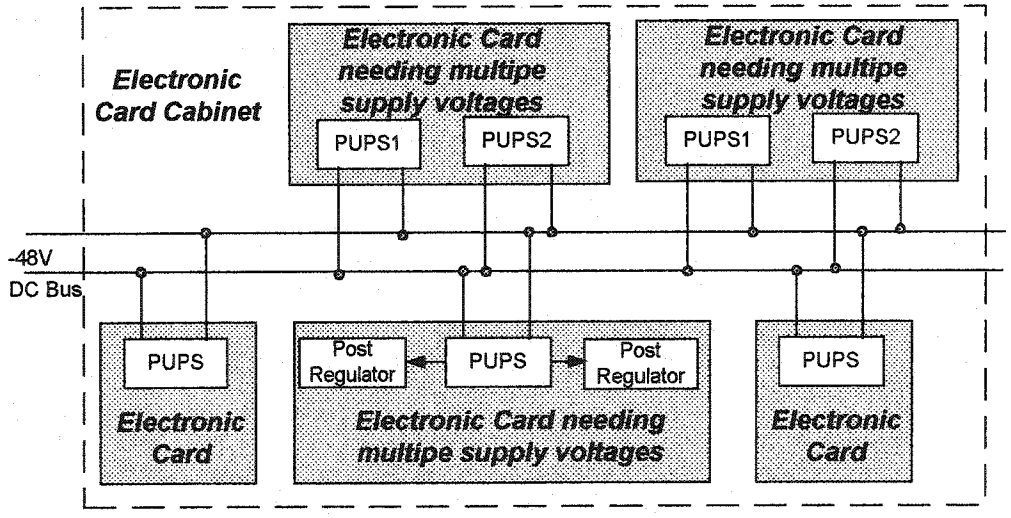


Fig. 1.5 The block diagram of the decentralized power distribution architecture.

However, the centralized architecture has the following significant drawbacks:

(i) It does not permit the direct upgrading of the electronic cards with new generation ICs, otherwise it requires the costly redesign of the centralized power supply and the layout of the back-plane.

(ii) It is not able to achieve tight voltage regulation at the point of use, owing to voltage deterioration caused by the long power distribution rails, and also because of the interaction between the electronic cards.

(iii) It does not allow hot insertion of an electronic card, or a voltage glitch will be produced that may interrupt the normal operation of other cards.

(iv) It is not efficient to power the low-voltage semiconductor circuits owing to the high losses on the long power rails from the supply to the circuit boards.

(v) The power supply has concentrated thermal problems, and forced air cooling is thus required to remove the concentrated heat in the power supply.

(vi) Its large ground or return loops propagate noise throughout the cabinet that may affect the sensitive high speed circuits.

(vii) Its failure group is the entire cabinet, and a failure in the power supply will shut down the entire cabinet.

All these problems disqualify the centralized architecture approach for advanced systems.

1.3.2 The Decentralized Power Distribution Architecture

Fig. 1.5 shows the block diagram of the decentralized architecture inside a cabinet using the distributed power supplies [7, 8-11]. A PUPS [17-23] converts the system dc bus voltage to the required operating voltage for the host board. When multiple voltage regulation is required, the card will employ multi PUPS modules or use a pre-regulator-

post-regulator converter. All circuit boards are parallel connected to the system dc bus.

Major merits of the decentralized distribution architecture include the following :

(i) It is easy to accommodate the upgraded cards with new ICs.

(ii) It provides well regulated supply voltages to the on-board loads, because the PUPS resides directly on the card.

(iii) It is more efficient for the low-voltage semiconductor circuit boards than is the centralized architecture, because the high current only travels short distances.

(iv) It distributes heat throughout the system, hence permitting convection cooling.

(v) The back-plane becomes simple because of the removal of high current rails.

(vi) Hot insertion of the card is feasible.

(vii) There is less noise to disturb sensitive circuits due to the absence of the large ground loop existing in the centralized architecture.

(viii) The failure group is the smallest, as a failed PUPS does not affect the other cards.

However, the distributed power architecture has the following shortcomings.

(i) Multiple PUPS modules or a pre-regulator-post-regulator multiple dc/dc power conversion stage must be used to obtain multiple output regulation.

(ii) The PUPS occupies valuable on-board space. The problem is much worse when multi modules are used to provide multiple supply voltages.

(iii) It is costly, especially when multi modules are used.

(iv) With the PUPS it is difficult to meet the input noise specifications due to the limited input filter allowed inside the compact module case.

Comparing these two architectures, one can easily conclude that the decentralized architecture is advantageous over the centralized one, if the voltage regulation, efficiency

of power distribution, ease in system upgrades with new ICs, size of failure group, and hot insertion are the major concerns. However, when looking deeper at the power distribution on the circuit board level, even the decentralized architecture cannot be applied to advanced telecom systems. This is mainly because of the complex implementation of multiple output regulation, the inefficient on-board power distribution of LVHC, and because of the bulkiness and high cost. These problems are explored further below.

1.3.3 Conventional Architectures to Produce Regulated Multiple Output Voltages

As shown in Fig. 1.6, conventionally there are three basic on-board power distribution architectures to deliver the power in regulated multiple output voltages. The first one (Fig. 1.6a) is to use post-regulators in cascade [24-47]. The second one (Fig. 1.6b) is to parallel additional output circuits to the master one. Typical examples of this approach are the cross-regulated topologies [48-71]. The third approach (Fig. 1.6c) is to use multi PUPS modules to produce finely regulated multiple output voltages [8]. All these approaches have significant drawbacks that must be examined in detail

1.3.3.1 Pre-Regulator-Post-Regulator Approach

The pre-regulator-post-regulator (Fig. 1.6a) is a popular solution. The pre-regulator may be a PUPS, which regulates an intermediate voltage. Regulation of the multiple output voltages is fulfilled by post-regulators. Typical post-regulators include the magnetic amplifiers (Magamps) [24-39], linear regulators [40], buck converter post-regulators [40-43], and the synchronous switch post-regulator (SSPR) [44-47].

A Magamp in each slave output is cost effective when the output voltage is above

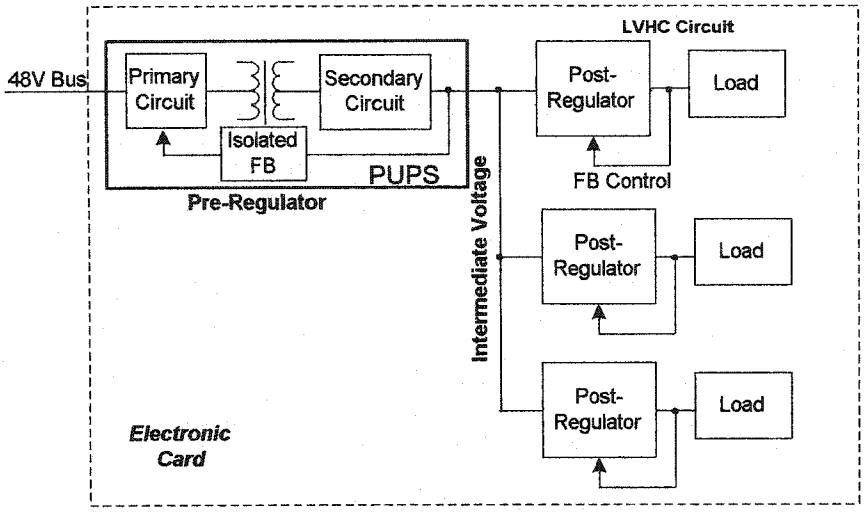
5 V [40]. Unfortunately, it is inefficient for very low voltage applications, because it cannot be used along with synchronous rectifiers (SRs). In addition, the bandwidth of the Magamp loop must be kept lower than the main loop to avoid loop interaction [37], and this limits the speed of its dynamic response.

Other post-regulators have some drawbacks as well. The linear regulator is cheap but lossy, and the output current is limited to be less than 1.5A. The buck converter post-regulator is more efficient than the other two. However, it adds an additional stage of power conversion and thus it cannot expect a high overall efficiency. The SSPR is basically a simplified version of a buck converter in which the buck switch is placed directly in series with the pre-regulator rectifier, and this will reduce the costs. But, such a two-component rectifier, which is normally a MOSFET with a series diode, nevertheless reduces the efficiency.

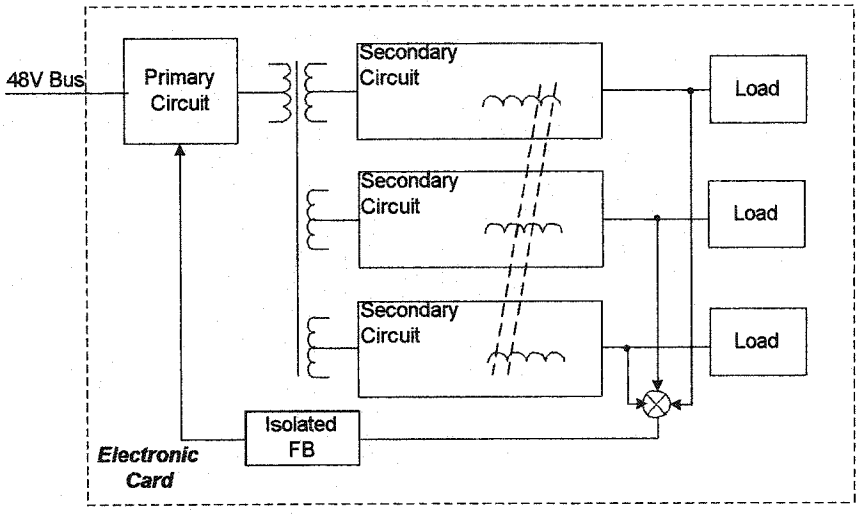
Above all, these post regulators will lose output regulation when the pre-regulator runs into discontinuous conduction mode, and their overall efficiency is sacrificed by the multi-stage conversion. Another drawback is that they all employ additional power components, and this will increase costs and overall physical size of the power supplies.

1.3.3.2 Cross-Regulation Approach

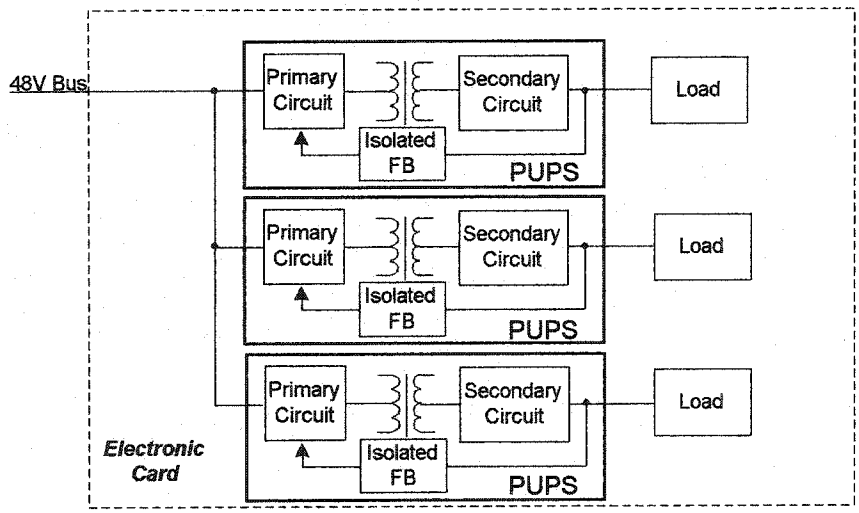
A converter that is cross-regulated for multiple outputs (Fig. 1.6b) is hardly able to produce precise regulation in all of the multiple outputs, owing to the difficulty of exactly matching and coupling of the magnetics [51,59-68]. They are rather complicated in analysis and difficult to design due to the complex cross-regulation. Also, they may not have output isolation [71]. Moreover, the dynamic properties of this type of converter are complicated and make the loop difficult to design [53-58].



a. Using Pre-regulator-post-regulators



b. Using cross-regulated converter



c. Using multi modules

Fig. 1.6 Conventional on-board power architectures.

1.3.3.3 Multi-Module Approach

Fig. 1.6c is a common practice in industry, in which several PUPS modules are used, each independently producing a finely-regulated supply voltage [8]. This approach is nevertheless bulky and costly because of the high costs of the PUPSs and the excessive use of the precious on-board space.

1.3.3.4 Conventional Control Scheme

Generally, in order to achieve output regulation in a switch-mode power supply, the output information is fed back to the pulse-width-modulation (PWM) controller that controls the main switch or switches. Such a control scheme may be perfect for the single output regulation but is surely not flawless for multiple output regulations.

In the pre-regulator-post-regulator approach, the main control loop only uses the pre-regulator output information as the feedback signal. Thus, the pre-regulator can only regulate the main output or the intermediate voltage, and post-regulators must be employed to regulate the slave outputs. In the cross-regulated multiple output converters, the feedback loop combines signals from all outputs for cross-regulation, but it is not dedicated to any single output. Consequently, precise regulation in any output is difficult to obtain.

In order to solve this problem, each output should have a dedicated feedback control loop such that fine regulation can be achieved at all of the outputs. This will be discussed further in Section 1.4.

1.3.4 Performance of Conventional On-Board Power Distribution Architectures

When looking at the performance in power efficiency and board-space

occupancy, there appear more problems in the conventional architectures. The low-voltage semiconductor circuit board, for example, will require a very high current from the power supply. When all heavy loads are not collocated but distributed at multi points on the board, the interaction of the high currents will cause significant losses.

It is obvious that the losses associated with the power distribution are determined by the following four factors: (i) the power level, (ii) the voltage at which the power is distributed, (iii) the length of the PCB tracks for the power delivery, and (iv) the cross-section area of these PCB power tracks. To be optimal in design, there will be a trade-off between the allowable losses and the size of the PCB power tracks, of which the latter is usually referred to as the PCB copper area requirements.

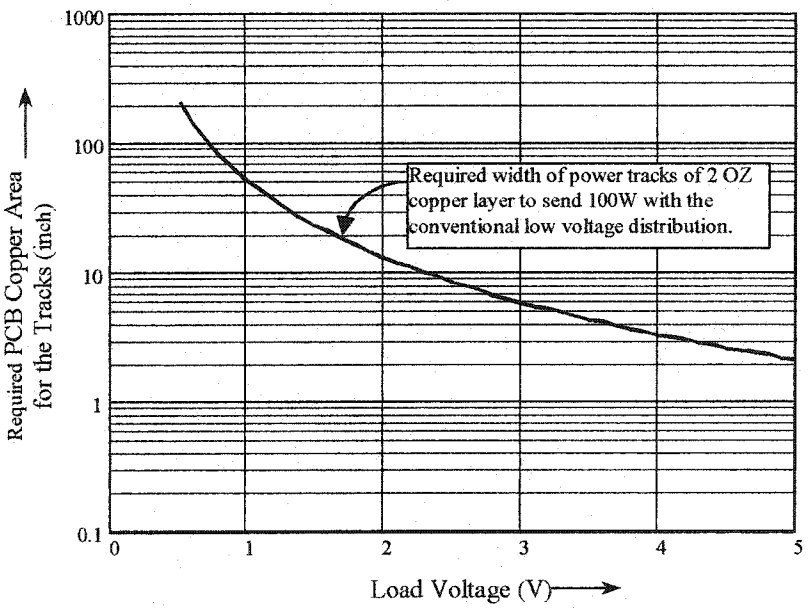


Fig. 1.7 PCB copper requirement for power distribution.

Fig. 1.7 shows the required copper area for the PCB power distribution tracks versus the voltage level at which the power is distributed for a given power loss. The required copper area rises exponentially as the load voltage decreases. For example, to deliver 100W at 1V to a load located 18 inches (46cm) away from the power supply, the PCB power distribution tracks of a 2OZ (or 71μm) thick copper layer will be at least 50 inches (or 127cm) wide, in order to limit the distribution loss to 1W. This is much greater than the dimension of a normal PCB board, indicating the necessary use of many layers of PCB for the power tracks. The following is a close look of the performance of each of the three conventional on-board power distribution architectures shown in Fig. 1.6.

1.3.4.1 On-Board Power Distribution Using Single Power Converter Module

When a single on-board power converter module delivers power to multi-point loads, as may be the case when using the cross-regulated converter, the power is usually distributed to the loads directly at the load operating voltage. Heavy duty tracks of multi layer PCB will be used to deliver the high current. This creates the following three major problems:

(i) Many layers of the PCB are used to carry the heavy currents, which reduces the number of available layers for tracking the high-speed signals.

(ii) There will be higher power losses on the long power tracks.

(iii) The voltage regulation will deteriorate at the point of load.

1.3.4.2 On-Board Power Distribution Using Multi-Modules

When multi PUPS modules are used to produce multi-point voltages [8], the approach seems optimal. Each PUPS module can be put directly beside the pertinent load

to minimize the length of the high current PCB tracks, and each load can obtain precisely regulated supply voltage. In addition, the power drawn by a PUPS from the dc bus is at high voltage (namely the 48V bus voltage) but at low current. Hence, the conduction losses on the PCB tracks are reduced. However, multi modules increase the total cost and take much of the valuable on-board space.

1.3.4.3 On-Board Power Distribution Using Pre-Regulator-Post-Regulators

The pre-regulator-post-regulators can be considered as a compromise between the above two approaches, and actually it is a widely used solution in telecom systems. The pre-regulator usually produces an intermediate voltage (typically in a range of 5 to 12V). The post-regulators can be placed closely to each of the multi-point loads. Now, the power is distributed to multi-point loads at the intermediate voltage level. Thus, this option causes less conduction losses on the power distribution tracks than the first one. However, since the intermediate voltage is much lower than the 48 V bus voltage, it still causes significant losses on the PCB power distribution tracks. This further decreases the already low conversion efficiency of the multiple-stage converters.

In summary, the conventional on-board power distribution architecture cannot be applied to multi-point load applications, because, although the load operating voltage will be very low, the current will be very high and the required copper area will be excessive. Furthermore, the conventional on-board power distribution degrades the voltage regulation at the point of the distant load due to the complex impedance and voltage drops along the long tracks between the power supply output port and the load. All these problems must be solved to meet the power requirements of advanced telecom systems

1.4 INTRODUCTION OF DPUPS ARCHITECTURE

As seen from the review, the major drawbacks of the conventional power distribution architectures are the costly implementation of multiple output regulation and the inefficient on-board power distribution for the low-voltage semiconductor circuit boards. These problems, from the architecture point of view, can be solved by developing a single stage converter topology that produces finely regulated multiple output voltages and distributes the power over the board in an efficient way. This new architecture concept, which has been previously referred to as the DPUPS in Section 1.2, will be elaborated below.

Fig. 1.8 shows the overview of the electronic card cabinet distribution configuration using the proposed DPUPS. Clearly, it is based on the conventional decentralized power systems. Hence, it will retain all the merits stated in Section 1.3.2. In addition, the DPUPS fulfills the functions of multi PUPS modules or the pre-regulator-post-regulator converters, thereby improving the overall efficiency by using single-stage conversion and reducing the costs by using fewer power components.

Table 1.1 summarizes the most desired features of the DPUPS. Unfortunately, none of existing converter topologies and on-board power distribution technologies alone has all these desired features.

The possible solutions for the implementation of these features are also given in Table 1.1. Among these solutions, 4 through 10 will be considered in developing the proposed DPUPS in latter chapters but will not be explained further.

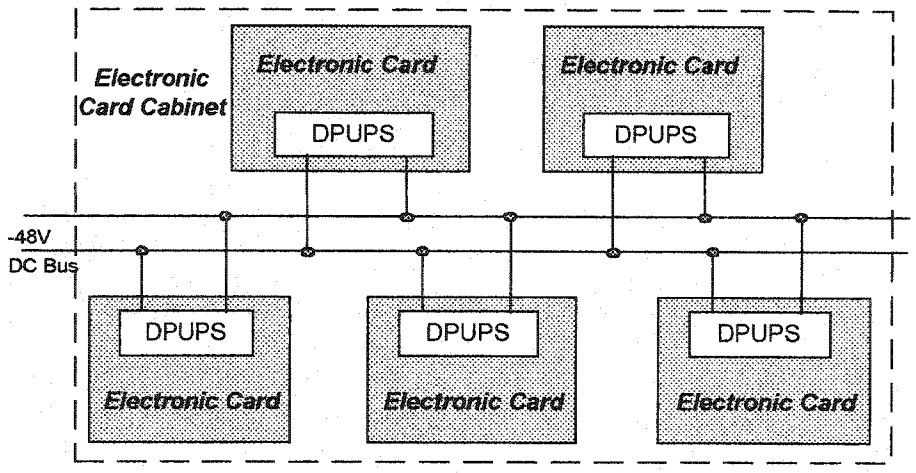
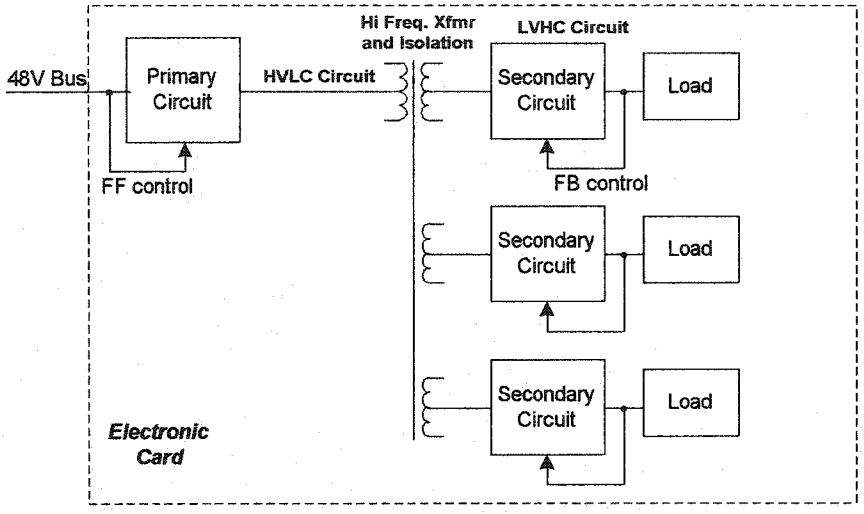


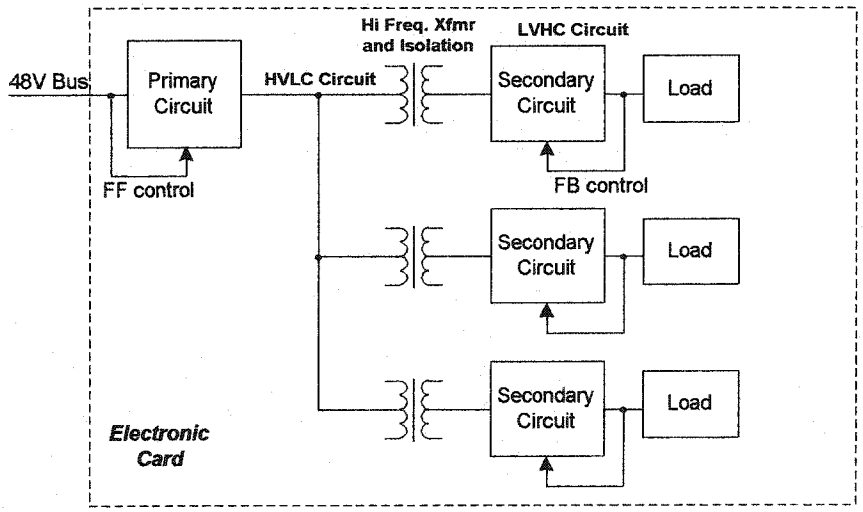
Fig. 1.8 The proposed power distribution architecture using DPUPS

Table 1.1 Desired features of DPUPS and possible solutions for implementation

Desired Features	Possible Solutions
a. Multiple output voltages with cost effective solution	1. Developing new topologies that achieves finely regulated multiple output in single stage;
b. Tight regulation at the point of load	2. Placing the output ports of the power supply directly beside critical loads, thereby to minimize the deterioration of voltage regulation by the LVHC PCB tracks
c. Efficient on-board power distribution to multi-point loads	3. Delivering the power to multi-point loads in the high-voltage-low-current form instead of the conventional LVHC form, thereby to minimize the conduction losses and the PCB copper area requirement to deliver the power to multi-point loads.
d. High power density and high efficiency to minimize the space taken by the power supplies	4. Using high switching frequency to reduce the size of power devices like magnetics and capacitors; 5. Using a simple converter topology with low number of power components, and avoiding multi-stage conversion; 6. Employing synchronous rectifier; 7. Using soft switching technique to improve the efficiency and to limit the cooling requirements;
e. Fast dynamic responses to handle the high slew-rate load transient	8. Also requiring high switching frequency to achieve a wide bandwidth; 9. Avoiding using slow devices like opto-couplers;
f. Low costs	10. Simple topologies, easy to understand, design and manufacture.



a. DPUPS suitable for collocated load applications



b. DPUPS suitable for multi-point load applications

Fig. 1.9 The conceptual block diagrams of the proposed DPUPS architectures.

The solutions 1 through 3 formulate the core concepts of the DPUPS. In order to realize these concepts, the DPUPS shall have the following configurations and features.

(i) All output circuits, namely the output rectification stages, should be arranged in parallel such that only a single dc/dc power conversion stage is involved for all outputs.

(ii) Each output circuit should be regulated by a dedicated and independent feedback control loop. Therefore, fine regulation at each of the output can be achieved, and cross-regulation can be eliminated.

(iii) The LVHC sections (namely the secondary circuits) of the DPUPS should be compact and close to the pertinent loads.

(iv) The employed number of power components/devices should be minimized.

Accordingly, all these lead to the two conceptual configurations of the DPUPS for different on-board power distribution applications, which are shown in Fig. 1.9.

By comparing Fig. 1.6 and Fig. 1.9, one can see clearly that the proposed DPUPS architectures use fewer power components in both the primary and secondary circuits than the conventional architectures do. This becomes very pronounced in terms of saving the circuit board space occupied by the power supply.

In comparison of the two DPUPS configurations, Fig. 1.9a is optimal for the applications where the heavy on-board loads are collocated. Its major advantage over the other configuration is the ability to integrate the power transformer to reduce the costs.

For the multi-point load applications, Fig. 1.9b serves as a better solution. Now, the LVHC sections can be located close to the loads, thereby minimizing the length of high-current PCB tracks and hence reducing the copper area requirement and the

deterioration of the voltage regulation. Therefore, each load can receive a finely regulated supply voltage no matter where it locates on the board. More importantly, the power from the dc bus is now delivered to the multi-point loads in the HVLC form. This greatly reduces the conduction losses and also greatly reduces the PCB copper area requirement. Fig. 1.10 shows the comparison of the PCB copper requirement of the DPUPS HVLC distribution vs. that of the conventional LVHC distribution. For the same amount of conduction losses as mentioned in the previous example, the DPUPS only requires a 0.2 inches wide track of 2OZ copper layer to deliver 100W, in contrast to the use of 50 inches wide track in the previous case.

In the next section, a fundamental power converter topology will be searched as the basis to implement the DPUPS architecture.

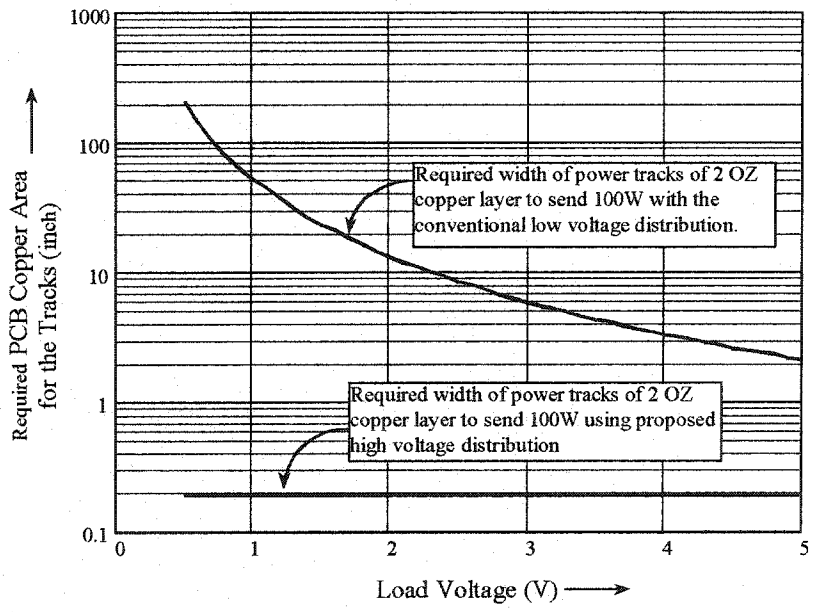


Fig. 1.10 Comparison of the PCB copper requirements of the DPUPS HVLC distribution and the conventional LVHC distribution.

1.5 A CANDIDATE OF BASIC CONVERTER TOPOLOGY FOR THE DPUPS

Normally the power level of most electronic cards in telecom systems is not more than 250 watts. For such a power level, the single switch topologies like the flyback or forward converters can be used due to their simple circuitry and low cost. If the power requirement is higher, the following multi-switch topologies, in an ascending order of power level, can be selected: the push-pull, half-bridge and full-bridge converters.

This thesis will focus on the majority applications, namely, for power levels below 250W. Hence, only flyback and forward type circuits will be considered below. Table 1.2 shows the comparison between these two simple topologies.

Table 1.2 Comparison between the flyback and forward converter topologies

Comparison	Flyback topology	Forward topology
Advantages	1. Single switch topology, 2. Not requiring output inductor in the output stage, 3. Simple transformer structure, 4. Relatively better regulating of slave outputs against the load variations , 5. Well-understood.	1. Single switch topology, 2. Lower rms and peak currents, 3. Lower output ripples, 4. Smaller output capacitor needed, 5. Easy to use self-driven SRs, 6. Well-understood.
Disadvantages	1. Higher rms and peak currents, 2. Larger output voltage ripples, 3. Lager output capacitor needed, 4. Hard to use self-driven SRs, 5. Hard switching.	1. Output inductor and one more diode are needed, 2. Complex power transformer, 3. Poor regulation of slave outputs against load variations, 4. Hard switching.
Applications	1. High input/output voltages, 2. Low output current, 3. Relatively lower power level.	1. Low input/output voltages, 2. High output current, 3. Relatively higher power level.

Because advanced telecom systems require high load currents at low operating voltages, the forward topology is the preferred candidate to implement the DPUPS. The major drawbacks that exclude the flyback are the difficulty in using the self-driven SRs, the high current stress on the power components, and the worst, the large ripple voltage in the output.

1.5.1 Drawbacks of the Forward Converter Topology

Although the forward topology is advantageous over the flyback one, the basic forward topology cannot be readily used to implement the DPUPS. The major problems are the poor regulation in the slave outputs, the hard switching, and the complex power transformer. The multiple output regulation issues have been discussed in Section 1.3.3. In the following, the other two issues will be discussed.

The complex power transformer of a forward converter requires an extra reset winding and thus is more expensive and bulky than that of other single-switch converter topologies. Normally, an additional winding requires two additional pins on the bobbin, and a bobbin having more pins is larger. This forces the use of a larger core even if a smaller one can meet the power requirement. Besides, an extra winding requires extra processes in finishing the bobbin and in installation. Consequently, this increases the transformer size, manufacturing costs and board assembly costs.

A hard switching converter is prohibited from operating at a frequency above 150kHz, otherwise it would suffer from excessive switching losses. Because the switching frequency is low, the converter must employ large power magnetics and capacitors. This makes the converter bulky in size and difficult to achieve high power density. Another drawback of the low switching frequency is the limited bandwidth in the

control loop and thence slow dynamic response, because the maximum achievable bandwidth is usually limited below one tenth of the switching frequency, in order to attenuate the switching noises.

In recent years, several soft switching forward converter topologies have been developed, and the following is a brief review of these topologies.

1.5.2 Existing Soft Switching Forward Topologies

1.5.2.1 Forward with Resistor-Capacitor-Diode Snubber and Non-dissipative Snubber

A simple solution to reduce the switching losses is to use a Resistor-Capacitor-Diode (RCD) snubber [72-74]. It reduces the turn-off losses of the switch, but does not help to reduce the turn-on losses. From the overall efficiency point of view, the RCD snubber itself dissipates the power saved from the switching losses, and hence it does not improve the converter overall efficiency.

An improved version of the RCD snubber is the so-called non-dissipative snubber [40,75-76]. It replaces the lossy resistor with an inductor. This inductor first stores the energy of the removed switching losses during the switching transients, and afterwards it feeds the energy back into the input dc line. Unfortunately, this approach does not work for the switch turn-on losses and it only functions within a very narrow input voltage range.

1.5.2.2 Resonant Reset Forward (RRF)

The RRF [77-79] achieves soft switching at full load, and it employs a simplified power transformer that does not use the tertiary reset winding. Unfortunately, in order to optimize its performance, the RRF generally works with a variable switching frequency.

This is not applicable to telecom systems, because the switching ripples and harmonics varies with the switching frequencies and they becomes difficult to filter out, and these noises may affects some sensitive high speed loads.

The RRF can also operate at a fixed switching frequency at the cost of high voltage stress on the main switch [79]. For a typical input voltage range of 35 V to 75 V, the voltage stress would be close to 200 V, which is about 50 V higher than that of a conventional forward converter. A higher voltage stress requires the main switch to use a MOSFET of a higher voltage rating, which normally has a higher Rds(ON) and thus causes more conduction losses.

In addition, although the RRF usually achieves soft switching at full load, it loses soft switching at light load. The loss of soft switching will cause thermal problems on the main switch due to the so-called $\frac{1}{2}CV^2$ losses, and this leads to a high cooling requirement on the switch.

The most serious problem with the RRF is the difficulty in driving the SR [79]. If the SR MOSFET is self-driven, namely being driven directly from a power transformer winding, its body diode will conduct and may reduce the efficiency of the SR stage. This is resulted from the sinusoidal shape of the voltage waveform during the transformer reset interval, which consequently reducing the gate drive voltage level to be lower than the MOSFET gate threshold and forcing the body diode to conduct. The conduction of the body diode not only causes more losses but also produce voltage spikes due to its slow reverse recovery. Extra circuit can be added to overcome these problems, but the entire circuit will become rather complicated.

1.5.2.3 Active Rest/Clamp Forward (ARF)

The ARF is a very popular topology developed in recent years [80-104]. It overcomes most of the drawbacks of the RRF. However, to achieve ZVS, normally a saturable inductor is added, and it is lossy and brings nonlinear property and makes design complex. Instead of using this additional saturable inductor, ZVS may also be achieved by lowering the magnetizing inductance of the power transformer. But this increases conduction losses due to the increased magnetizing current, and the design of the transformer no longer follows the well-understood design procedure of the conventional forward transformer. The circulating current in the clamp circuit results in additional conduction losses. Besides, the ARF also suffers from the following four problems.

(i) A variable pulse width gating pattern with controllable dead time must be generated for the clamp switch.

(ii) When the clamp switch uses an n-channel MOSFET, it stays on the high side and its gate drive must be isolated from the main switch. When a p-channel MOSFET is used as the clamp switch, it stays on the low side, and theoretically there is no need of the gate drive isolation. However, a negative bias voltage ($-V_{CC}$) is required to turn off the p-channel device.

(iii) ZVS is lost under light load conditions for the same reason as in the RRF.

(iv) The patent related legal issues create difficulties in their applications.

1.5.2.4 A Flyback-Type Auxiliary Circuit Aided ZVS Forward (FBF)

To overcome above mentioned drawbacks of the RRF and ARF, an improved ZVS forward converter topology employing a small flyback-type auxiliary circuit is

developed in [105-108]. With this auxiliary circuit, the main switch can always achieve ZVS independent of the operating conditions. This significantly improves the overall efficiency under all operating conditions. Besides, the gating of the auxiliary switch is in a fixed pulse width, and there is no need of gate drive isolation. All these simplify the design of the gate drive circuits. But the FBF has a hard turn-off switching in its auxiliary switch, and it does not recover the energy associated with the leakage inductance of the auxiliary circuit. Thus, very high switching frequencies cannot be applied. Moreover, the FBF transformer is a complex one.

In conclusion, existing soft-switching forward converter topologies cannot be readily applied to implement the DPUPS. Their major drawbacks like the loss of soft switching at some operating conditions, use of complex power transformer and complicated gate drive and control issues should be overcome.

1.6 OBJECTIVES AND SCOPE OF THE THESIS

The four major objectives of this thesis are as follows:

(i) To develop new on-board power distribution architectures that are suitable for different load configurations on the low-voltage semiconductor circuit board;

(ii) To develop new power converter topologies that can be used to implement the architectures;

(iii) To develop design procedures of the proposed architectures;

(iv) To perform experimental and simulation verifications.

These major objectives involves the following six minor objectives:

(i) To develop improved soft switching forward converter topologies;

(ii) To simplify the forward-type power transformer with self-reset technique;

(iii) To achieves multiple output regulation by single stage power conversion;

(iv) To achieve optimal on-board power distribution for multi-point loads;

(v) To perform detailed steady state and dynamic analyses.

(vi) To build prototype circuits to verify the analysis and provide proof of concepts.

The scope of the thesis will be defined within the circuit descriptions, steady state and small signal analyses, simulation and experimental verification, and design of the proposed DPUPS architectures.

1.7 THESIS OUTLINE

The outline of the rest part of the thesis is as follows.

In Chapter 2, the Type 1 ZVS and self-reset forward converter topology is presented. It employs a resonant auxiliary circuit and a simplified power transformer to overcome the drawbacks in existing soft-switching forward topologies. Steady state operation of ZVS is analyzed, and the flux excursion of the self-reset power transformer is investigated, and its characteristics are summarized. Experimental and simulation results are presented to verify the analysis.

In Chapter 3, the Type 2 ZVS and self-reset forward converter topology is presented. It is similar to the Type-1 topology, but it does not have the same mechanism in achieving the self-reset of the power transformer. It retains all the advantages of the Type 1 topology. In addition, it limits the main switch drain voltage stress at about twice of the input voltage. Steady state operation of ZVS is analyzed, and the flux excursion of the self-reset power transformer is investigated, and its characteristics are summarized. Experimental and simulation results are presented to verify the analysis.

In Chapter 4, the DPUPS architecture is presented using the Type-1 topology. It is

optimal for applications where the critical loads can be collocated closely around the on-board power supply. This DPUPS overcome the drawbacks of conventional on-board power distribution architecture by providing independently and precisely regulated multiple outputs in a single dc-dc power conversion stage with simplified control scheme. Both steady state and small signal analyses are performed, and the characteristics of the DPUPS are summarized. A design procedure is generated based on the analyses of Chapters 2 and 4. The analysis and design are verified with experimental and simulation results.

In Chapter 5, the DPUPS architecture is presented using the Type 2 topology. It is optimal for multi-point load applications. Optimal on-board power distribution is achieved by distributing the power in the high-voltage-low-current form. Both steady state and small signal analyses are performed, and the DPUPS characteristics are summarized. A design procedure is generated based on the analyses of Chapters 3 and 5. The analysis and design are verified with experimental and simulation results.

In Chapter 6, conclusions and contributions of the thesis are summarized. Suggestions for future work are proposed.

CHAPTER 2

ZVS AND SELF-RESET FORWARD CONVERTER TOPOLOGY (TYPE 1)

2.1 INTRODUCTION

As reviewed in last chapter, the forward converter topology is selected to implement the proposed DPUPS concept, mainly because of its capabilities of high output current, low output ripples, and easy use of self-driven synchronous rectifiers. All these advantages are the desired features for very low output voltage and high output current applications like the widely used low-voltage semiconductor circuit boards in advanced telecom systems.

There are several improved forward converter topologies, including the resonant reset forward (RRF) [77-79], the active reset/clamp forward (ARF) [80-104], and the the flyback-type auxiliary circuit aided ZVS forward (FBF) [105-108]. However, as reviewed in last chapter, all these topologies suffer from at least one of the following drawbacks:

(i) The soft switching is lost under some operating conditions (RRF, ARF).

(ii) The control and gate-drive design is complicated (ARF).

(iii) The power transformer is complex that requires a reset winding (FBF).

(iv) The auxiliary switch has hard switching (FBF).

(v) The leakage energy in the auxiliary circuit is not recovered (FBF).

Because of drawbacks, it is difficult to use these existing topologies directly to implement the DPUPS concepts.

This chapter presents an improved ZVS and self-reset forward topology (referred

to as the Type 1 converter topology hereafter) that can overcome the aforementioned drawbacks. In contrast to the FBF's flyback-type auxiliary circuit, this proposed topology employs a resonant auxiliary circuit, such that the auxiliary switch also achieves soft switching at both turn-on and turn-off, and the energy associated with the leakage inductance can be recovered. It also employs a simplified power transformer that can be reset without the use of tertiary reset winding. The self resetting property simplifies the design of the power transformer considerably, and it is undoubtedly a very desirable feature of the DPUPS architectures.

In order to understand its operating principle and performance, detailed steady state analysis of the Type 1 topology is performed in this chapter.

The structure of this chapter is arranged in the following six sections. The description of the Type 1 topology is given in Section 2.2, and the operating principle is presented in Section 2.3. The steady state analysis is performed in Section 2.4, and the flux excursion of the self-reset power transformer is studied in Section 2.5. Simulation and experimental results are presented in Section 2.6 as proof of concept. Finally, in Section 2.7, some conclusions are drawn to summarize the topology's characteristics.

2.2 CIRCUIT DESCRIPTION

Fig. 2.1 shows the generic topology of the Type 1 ZVS and self-reset forward converter. It consists of a forward-type power circuit and a resonant auxiliary circuit that is shown inside the dash-line boundary.

The power circuit consists of (i) the self-rest power transformer T_P with two windings N_p and N_s (turns ratio $k=N_p/N_s$), (ii) the main switch S_{main}, (iii) the synchronous rectifiers (SRs), SR_1 and SR_2, (iv) an output filter comprised of L_o and C_o, and (v) a small

current limiting inductor L_s.

The resonant auxiliary circuit consists of (i) S_{aux}, the auxiliary switch, (ii) C_{snb}, a snubber capacitor for S_{main}, (iii) L_a and C_a, a resonant tank, (iv) T_a, a center-tapped auxiliary transformer with three windings N_{ap}, N_{as1} and N_{as2} (turns ratio k_a=N_{ap}/N_{as1}= N_{ap}/N_{as2}), and (v) D_{a1} and D_{a2}, two blocking diodes.

The auxiliary circuit fulfills the following multifold functions:

(i) To provide ZVS conditions for S_{main} at both turn-on and turn-off, thereby to greatly reduce, or even eliminate S_{main}'s switching losses;

(ii) To achieve zero current switching (ZCS) of S_{aux} at turn-on and ZVS at turn-off, thereby to greatly reduce the switching losses of S_{aux};

(iii) To recover the discharged energy from the snubber capacitor C_{snb} that otherwise would be dissipated somewhere else, hence to improve the overall efficiency;

(iv) To reset the power transformer T_P.

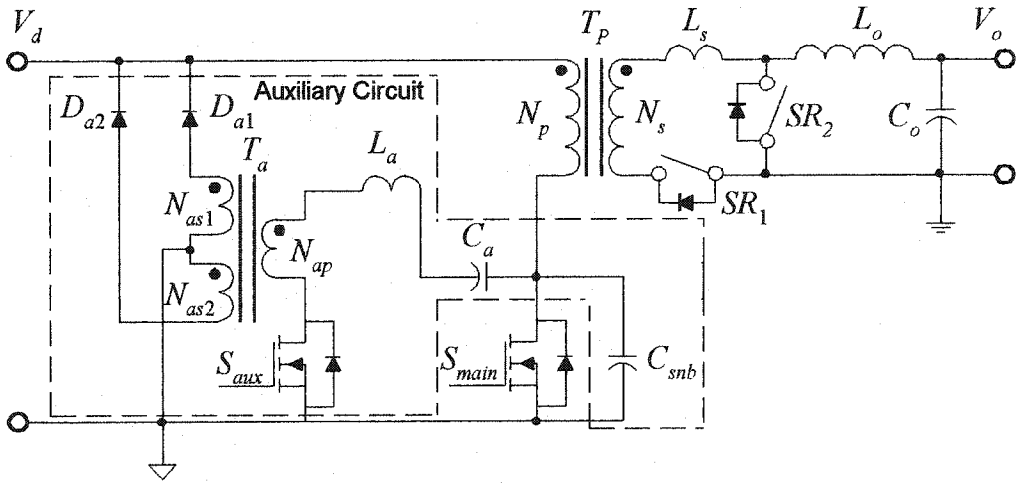


Fig. 2.1 The Type 1 ZVS and self-reset forward converter topology.

2.3 OPERATING PRINCIPLE

The operating principle of the Type 1 converter topology will be described with the assumption that all components are ideal devices, and the timing of controlling the SRs are ideal such that the SRs operate exactly as ideal diodes.

Fig. 2.2 gives the circuit variable designations of the Type 1 converter topology. Fig. 2.3 shows key waveforms of the topology in steady state operation. Each switching cycle (duration T_s) can be divided into eight (8) intervals.

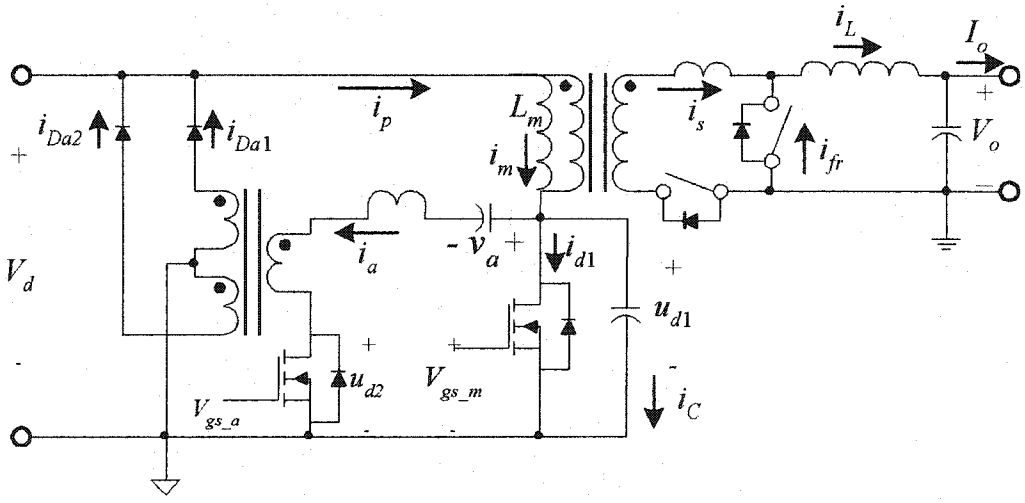


Fig. 2.2 Variable designations.

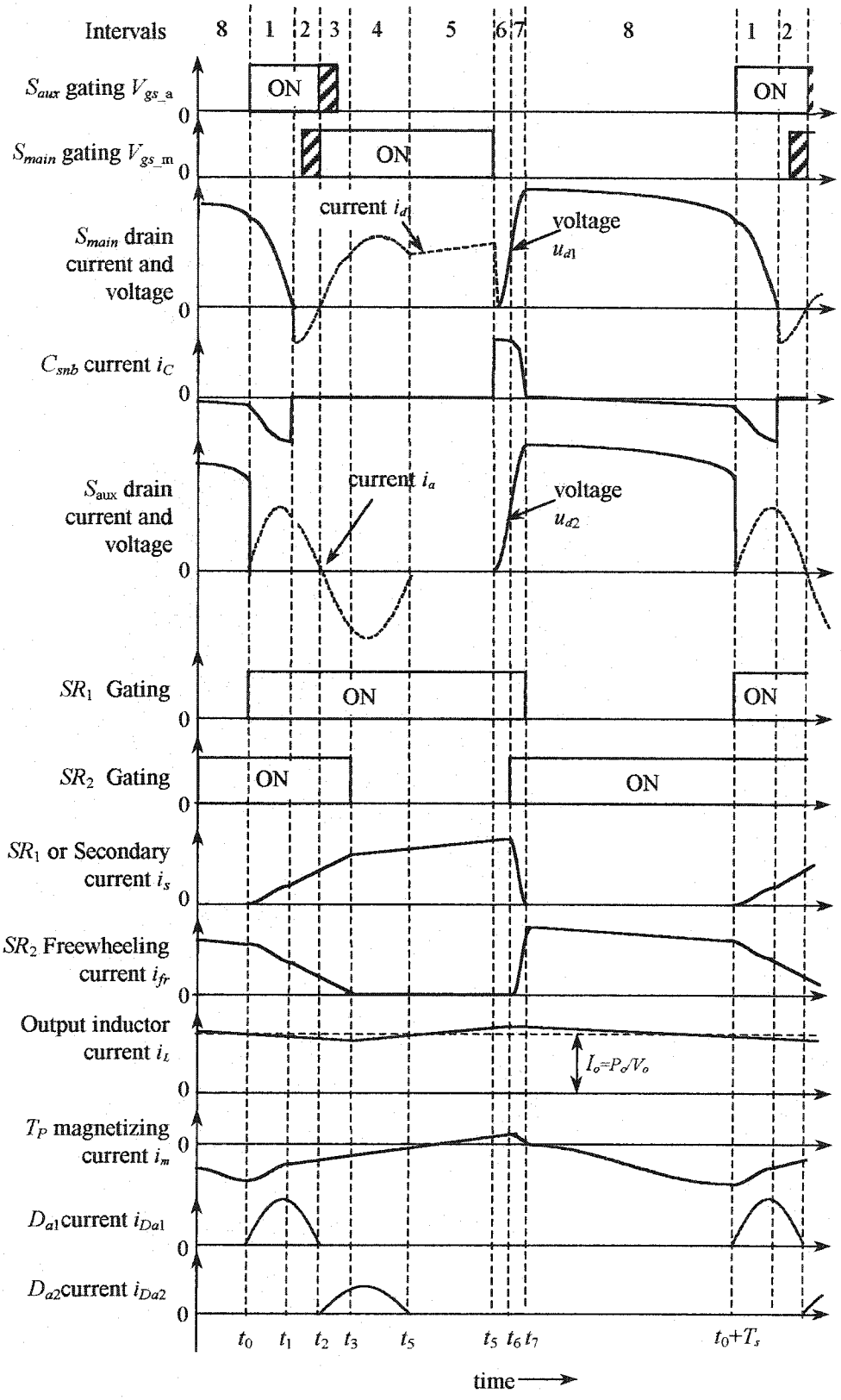


Fig. 2.3 Steady-state operation key waveforms of the Type 1 converter topology.

2.3.1 *Interval 1 ($t_0 \leq t < t_1$): Snubber capacitor discharging and energy recovering*

Fig. 2.4 shows the active current paths during Interval 1. At the beginning of this interval ($t = t_0$), the auxiliary switch S_{aux} is turned on. Since the inductor L_a does not allow the current i_a to rise instantly, the series-connected S_{aux} achieves a ZCS turn-on. This softly switched transient helps S_{aux} to reduce the turn-on switching losses.

Now, C_{snb} starts to discharge by the resonant current i_a that flows along the path of C_a, L_a, T_a and S_{aux}. This prepares the ZVS condition for S_{main} to turn on in the next interval. The resonant current i_a temporarily stores the discharged energy from C_{snb} into C_a and L_a, and it also recovers some of the discharged energy by inducing a current to flow into the input dc bus through N_{as1} and D_{a1}.

The function of L_s in this interval is to slow down the rise of the secondary current i_s such that C_{snb} can be discharged completely. Without L_s, as soon as i_a pulled u_{d1} lower than the input voltage V_d, T_P would see a positive voltage. This positive voltage would cause SR_1, which is an ideal SR, to turn-on, and then, a large primary current would be induced to flow down to refill C_{snb}, which would prevent the C_{snb} from complete discharge. Conclusively, L_s must be employed in order to provide ZVS condition for S_{main} to turn on.

It shall be pointed out that L_o is fairly large and can be considered as a dc current source, namely $i_L \approx I_o$. However, L_s only allows i_s to rise slowly. Hence, both SR_1 and SR_2 conduct to continue the almost constant current i_L.

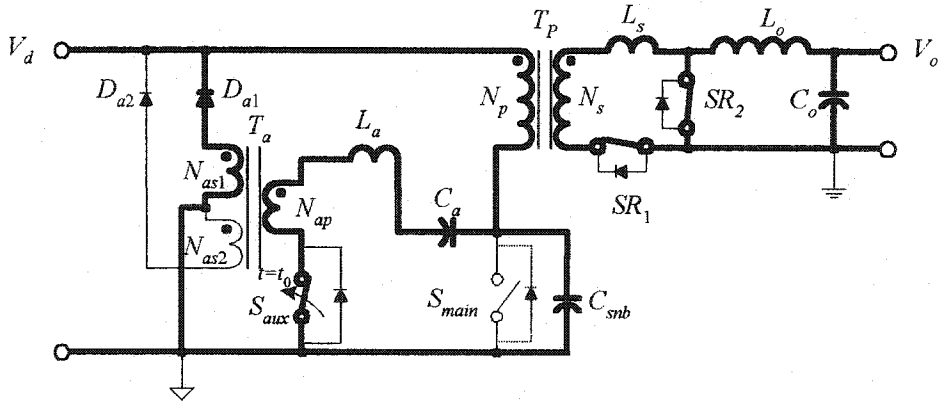


Fig. 2.4 Active current paths in steady state operation during Interval 1.

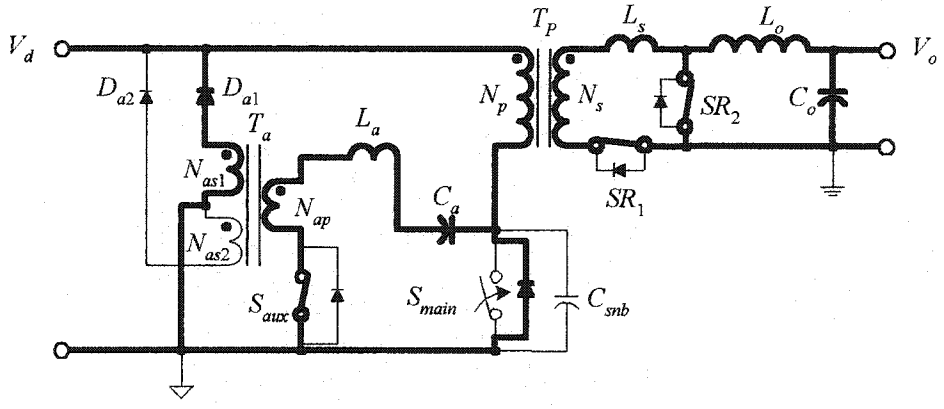


Fig. 2.5 Active current paths in steady state operation during Interval 2.

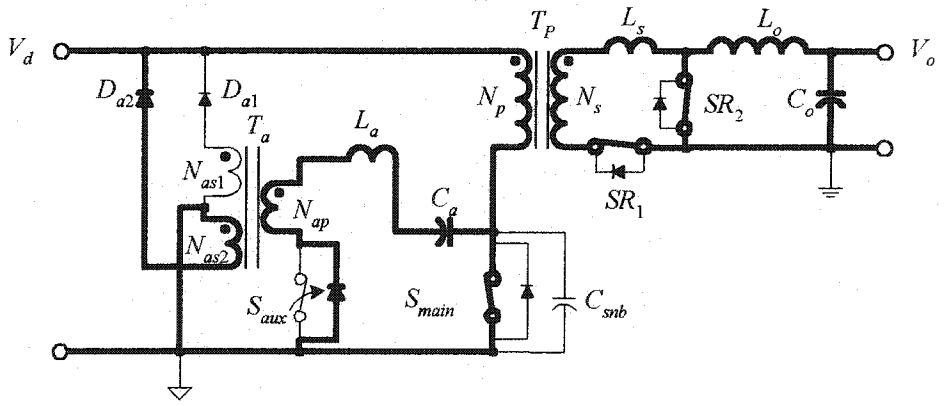


Fig. 2.6 Active current paths in steady state operation during Interval 3.

2.3.2 *Interval 2 ($t_1 \leq t < t_2$): S_{main} drain zero voltage clamping and S_{main} ZVS turn-on*

Fig. 2.5 shows the active current paths in Interval 2. At the beginning of this interval, C_{snb} is just completely discharged. The inductor L_a forces i_a to continue flowing in the auxiliary circuit, but i_a diverts from C_{snb} to the body diode of S_{main}, and this clamps u_{d1} at zero and waits for S_{main} to turn-on. The induced current on the secondary side of T_a continues the recovery of the discharged energy that is temporarily stored in the resonant tank. At anytime in this interval can S_{main} be turned on in ZVS, hence to eliminate the turn-on switching losses.

During this interval, i_s continues rising but it has yet to reach the magnitude of i_L, thus, the simultaneous conduction of both SR_1 and SR_2 continues.

2.3.3 *Interval 3 ($t_2 \leq t < t_3$): Resonant current reversing and S_{aux} ZVS turn-off*

Fig. 2.6 shows the active current paths in Interval 3. At the beginning of this interval, the resonant i_a reaches zero and it starts to reverse its direction. The reversed i_a induces a current flowing through N_{as2} and D_{a2} and recovers the discharged energy that is temporarily stored in C_a in last two intervals.

At any time during this interval can S_{aux} be turned off in ZVS, because the reversed i_a can divert to S_{aux}'s body-diode, and thus clamping its drain voltage at zero to eliminating the turn-off switching losses.

During this interval, i_s continues rising but it has yet to reach the magnitude of i_L, thus, the simultaneous conduction of both SR_1 and SR_2 continues.

2.3.4 *Interval 4 ($t_3 \leq t < t_4$): Power transferring, T_P magnetizing, and discharged energy recovery completing*

Fig. 2.7 shows the current loops in Interval 4. At the beginning of this interval, i_s reaches the magnitude of i_L, then the current through SR_2, namely i_{fr}, becomes zero and afterwards SR_2 is turned off. During this interval, the power is transferred from the input to the load in the same way as in a conventional forward converter.

The auxiliary circuit continues the process described in Interval 3 until the resonant i_a swings back to zero again at the end of Interval 4.

2.3.5 *Interval 5 ($t_4 \leq t < t_5$): Power transfer and T_P magnetizing continuing*

Fig. 2.8 shows the active current paths in Interval 5. At the beginning of this interval, the resonant i_a becomes zero again and the recovery of the discharged energy from C_{snb} is completed. Since S_{aux} is already turned off, the resonance between L_a and C_a is blocked, and i_a stops flowing. During this interval, the secondary circuit behaves the same as in the last interval.

2.3.6 *Interval 6 ($t_5 \leq t < t_6$): C_{snb} charging and S_{main} ZVS turn-off*

Fig. 2.9 shows the active current paths in Interval 6. At the beginning of this interval, S_{main} is turned off to regulate the output voltage. The snubber capacitor C_{snb} only allows S_{main} drain voltage u_{d1} to rise slowly, and thus S_{main} achieves a soft switching turn-off and greatly reduces or even eliminates the turn-off switching losses.

Before u_{d1} reaches the magnitude of V_d, T_P continues to see a positive voltage. Thus, SR_2 stays off, and total output inductor current i_L flows through SR_1.

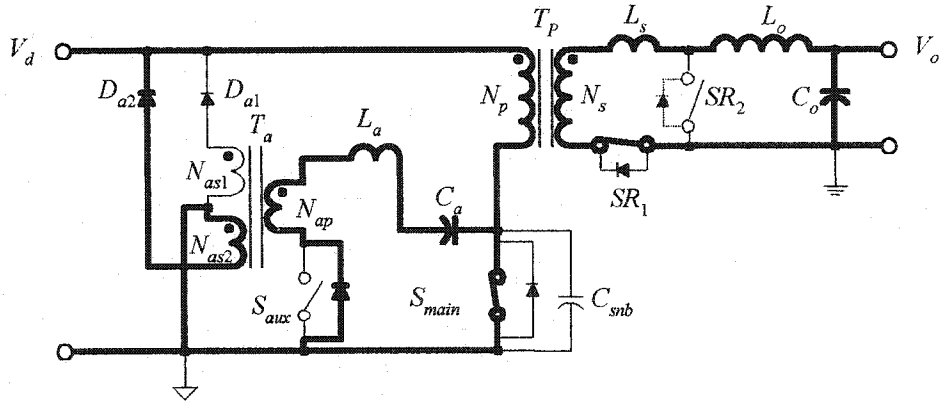


Fig. 2.7 Active current paths in steady state operation during Interval 4.

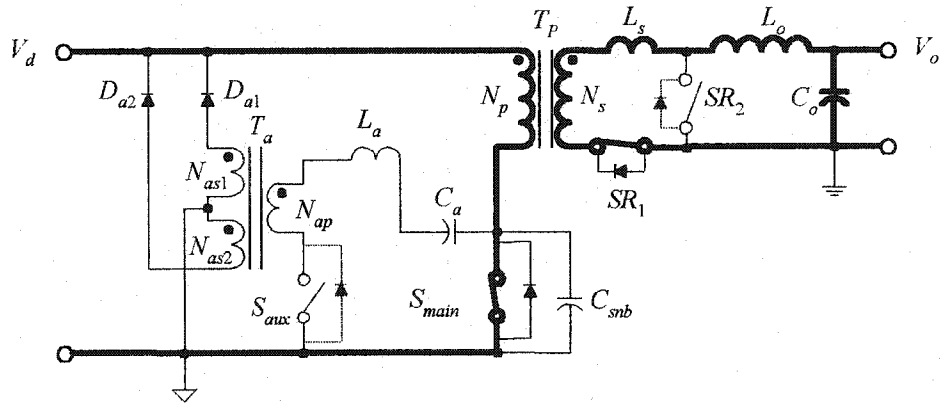


Fig. 2.8 Active current paths in steady state operation during Interval 5.

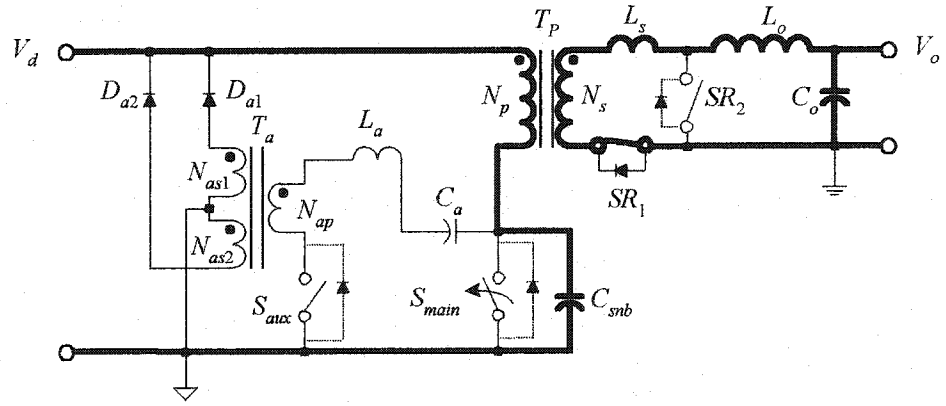


Fig. 2.9 Active current paths in steady state operation during Interval 6.

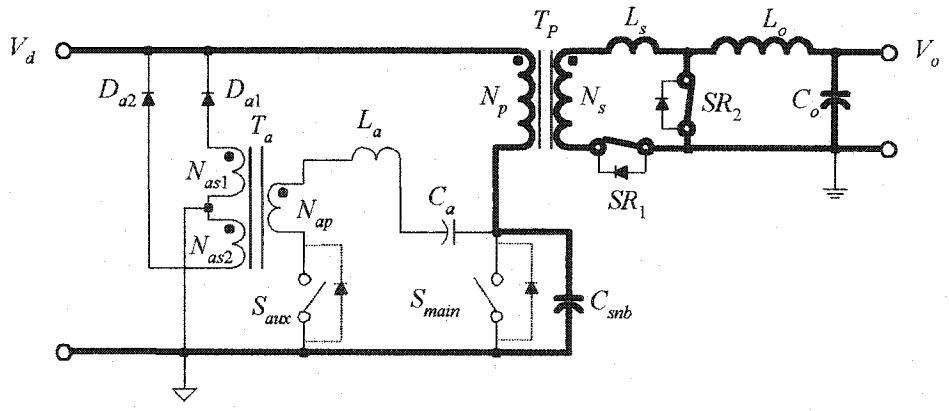


Fig. 2.10 Active current paths in steady state operation during Interval 7.

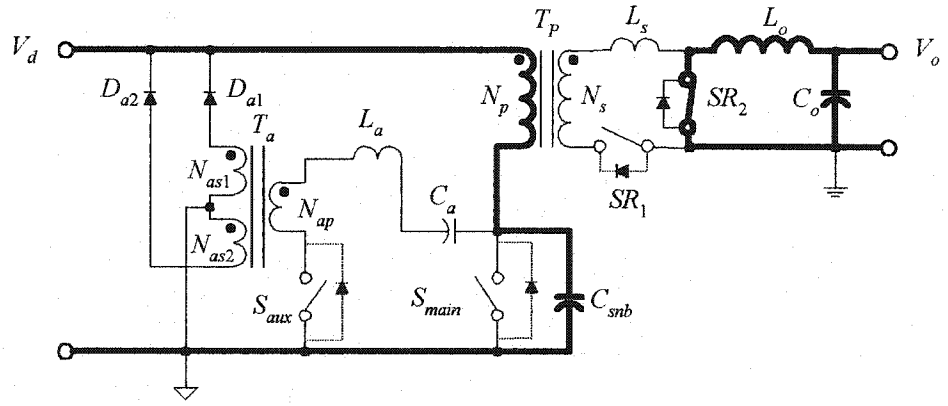


Fig. 2.11 Active current paths in steady state operation during Interval 8.

2.3.7 Interval 7 ($t_6 \leq t < t_7$): L_s transferring energy to C_{snb}

Fig. 2.10 shows the active current paths in Interval 7. At the beginning of this interval, u_{d1} rises above the magnitude of V_d and T_P starts to see a negative voltage. However, L_s does not allow i_s to stop immediately. Then i_s continues flowing but it starts to decreases because L_s also sees the negative voltage. This secondary current reflects

into the primary side and keeps charging C_{snb}, in this way the stored energy in L_s is transferred to C_{snb} instead of being dissipated. Since i_s decreases, SR_2 starts to conduct in order to continue the almost constant current i_L.

2.3.8 Interval 8 ($t_7 \leq t < t_0+T_s$): T_P resetting

Fig. 2.11 shows the active current paths in Interval 8. At the beginning of this interval, i_s decreases to zero and SR_1 is then turned off. In a freewheeling mode, SR_2 now conducts the entire i_L.

On the primary side, the magnetizing inductance L_m and the snubber capacitor C_{snb} now excites a new resonance that finally leads to the reset of the power transformer.

Interval 8 completes at the end of the switching cycle, and the circuit repeats the process from Intervals 1 through 8, cycle after cycle, to continually deliver the power to the load at the regulated voltage.

2.3.9 Summary of the Operating Principle

In summary, major stages of the steady state operation are as follows. C_{snb} is discharged first to pull S_{main} drain voltage down to zero, and this allows S_{main} to have a ZVS turn-on. Then, the converter transfers the power to the load in the same way as the standard forward converter does. When S_{main} is turned off after completing its duty cycle, C_{snb} slows down the rise of S_{main} drain voltage, thus S_{main} achieves a soft switching turn-off. In the rest of the cycle, the resonance between L_s and C_{snb}, and afterwards between L_m and C_{snb}, resets the power transformer. The auxiliary circuit recovers the energy stored in C_{snb}, L_s and the leakage inductances, instead of dissipating the energy. Because of soft switching and energy recovery, the overall efficiency of the topology can be improved.

2.4 STEADY STATE ANALYSIS

In order to understand the performance and characteristics of the topology, the steady state analysis of the Type 1 topology of Fig. 2.1 is given below. In the analysis, the time varying variables such as the principal currents and voltages of the Type 1 converter topology are determined. Based on these variables, the resultant quantities such as the peak, average or rms currents and voltages of the principal components and devices are obtained. These quantities provide guidelines for design of the proposed DPUPS in Chapter 4.

The methodology used in the analysis is as follows. The closed form solution is obtained by solving a set of differential equations in each interval and by matching the boundary conditions at the boundaries of each interval. These boundary conditions are functions of the operating frequency f_{sw}, the input voltage V_d and the output power P_o, and they can be obtained by the iterative process such as the Newton-Raphson method.

2.4.1 Assumptions for the Steady State Analysis

The following assumptions are made for the steady state analysis. The analysis starts with ideal components. The effects of the non-ideal properties of the components and devices in a practical circuit will be discussed in Section 2.4.3.

(i) The circuit is already in steady state, and the operating frequency f_{sw}, input voltage V_d, output voltage V_o, and output current I_o, are all constant.

(ii) Switching of S_{main} and S_{aux} are instant and the transients are negligible.

(iii) S_{aux} output capacitor is negligible.

(iv) T_P magnetizing inductance L_m is much greater than L_s and L_a.

(v) L_o and C_o are fairly large such that L_o can be regarded as a dc current source and

the C_o can be considered a dc voltage source, and the current through L_o is thus equal to the load current.

(vi) The current limiting inductor L_s is much smaller than the output filter inductor L_o.

(vii) T_a has a very small turns-ratio, i.e., k_a<<1, such that the primary winding N_{ap} sees a much lower voltage when the input voltage is applied to N_{as1} or N_{as2}.

(viii) T_a magnetizing current is negligible.

(ix) The forward drops of all diodes are negligible.

(x) The SRs are ideal synchronous rectifiers with accurate timing of control.

(xi) The leakage inductances of T_a and T_P are negligible.

(xii) Losses on each component and device are negligible.

To facilitate the analysis, the following symbols are assigned to some instantaneous variables (see Fig. 2.2):

(i) i_p, the primary current,

(ii) i_a, the current flowing through the resonant inductor L_a,

(iii) u_a, the voltage across the resonant capacitor C_a,

(iv) u_{d1}, S_{main} drain-to-source voltage

(v) i_s, the secondary current , and

(vi) i_m, the magnetizing current of the power transformer T_P.

The following equivalents are worth pointing out for later references:

(i) The currents through C_a, L_a, N_{ap} and S_{aux} are the same i_a,

(ii) The currents through N_s, SR_1 and L_s are the same i_s,

(iii) The drain current of S_{main} when it is ON is the sum of i_p and i_a,

(iv) The voltage across C_{snb} and S_{main} drain-to-source voltage are the same u_{d1}.

2.4.2 Steady State Analysis

According to the operating principle, and referring to Fig. 2.4 through Fig. 2.11, one can obtain the equivalent circuit for each interval as shown in Fig. 2.12. Based on these equivalent circuits and according to Kirchhoff's Laws, one can obtain a group of sets of differential equations, as given in Appendix A, which restrain the instantaneous values of key variables in each interval.

2.4.2.1 Interval 1 ($t_0 \le t < t_1$)

The equivalent circuit in Interval 1 is shown in Fig. 2.12a. At the beginning of Interval 1, the steady state initial values of key variables are as follows:

$$\begin{cases} u_{d1}(t_0) = (1+\delta)V_d \\ u_a(t_0) = V_{a0} \\ i_a(t_0) = 0 \\ i_p(t_0) = i_m(t_0) \\ i_s(t_0) = 0 \\ i_m(t_0) = I_{m0} \end{cases} \tag{2-1}$$

where δ is the factor by which S_{main} drain voltage is greater than V_d at t_0.

From the set of equations given in (A-1), the drain-to-source voltage of S_{main} satisfy the following fourth order differential equation:

$$\alpha \frac{d^4 u_{d1}(t)}{dt^4} + \beta \frac{d^2 u_{d1}(t)}{dt^2} + u_{d1}(t) = V_d \tag{2-2}$$

where

$$\begin{cases} \alpha = L_a C_a L_e C_{snb} \\ \beta = L_e C_{snb} + L_e C_a + L_a C_a \end{cases} \tag{2-3}$$

in which L_e is the equivalent of the paralleled L_m and L_s seen by the primary, namely

$$L_e = \frac{k^2 L_s L_m}{k^2 L_s + L_m} \underset{L_m >> k^2 L_s}{\approx} k^2 L_s \tag{2-4}$$

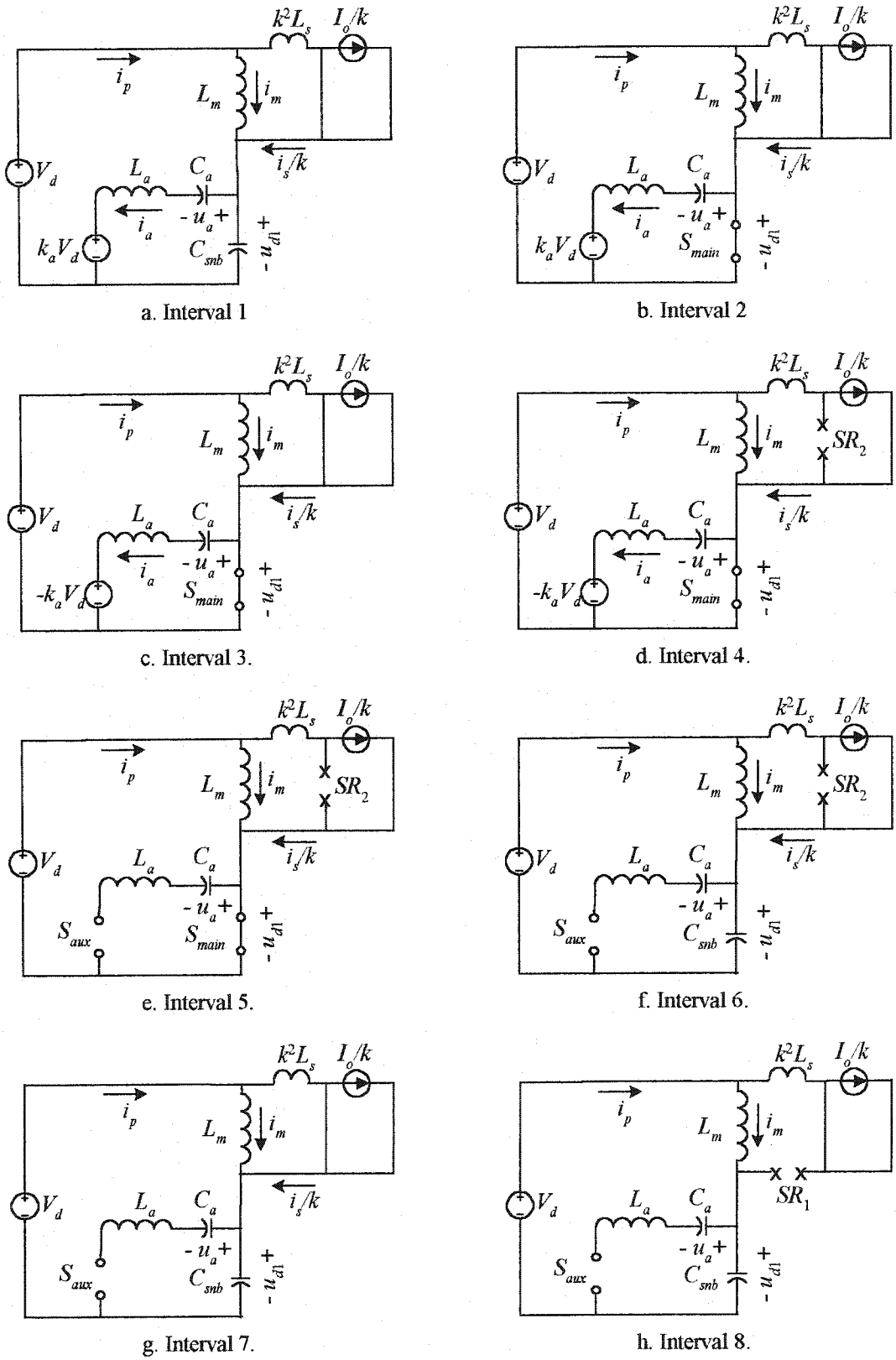


Fig. 2.12 Equivalent circuits seen from the primary side in the eight different intervals.

The solution of (2-2) is found to be as follows:

$$u_{d1}(t) = V_d + a_1 \cos\omega_1(t-t_0) + a_2 \sin\omega_1(t-t_0) + a_3 \cos\omega_2(t-t_0) + a_4 \sin\omega_2(t-t_0) \tag{2-5}$$

where, the resonant frequencies are determined by

$$\omega_1 = \frac{1}{2}\sqrt{\frac{2\beta + 2\sqrt{\beta^2 - 4\alpha}}{\alpha}} \approx \sqrt{\frac{\beta}{\alpha}} \tag{2-6}$$

$$\omega_2 = \frac{1}{2}\sqrt{\frac{2\beta - 2\sqrt{\beta^2 - 4\alpha}}{\alpha}} \approx \frac{1}{\sqrt{\beta}} \tag{2-7}$$

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & \omega_1 & 0 & \omega_2 \\ -\omega_1^2 & 0 & -\omega_2^2 & 0 \\ 0 & -\omega_1^3 & 0 & -\omega_2^3 \end{bmatrix}^{-1} \begin{bmatrix} \delta V_d \\ \dot{u}_{d1}(t_0) \\ \ddot{u}_{d1}(t_0) \\ \dddot{u}_{d1}(t_0) \end{bmatrix} \tag{2-8}$$

in which the initial conditions (δV_d and the three order derivatives of u_{d1} at $t = t_0$) are determined by the operating conditions and also by the four energy storage components C_{snb}, C_a, L_a and L_s. Their expressions are given in Appendix E as the variable "vector".

Similarly, from (A-1), u_a that is the voltage across C_a is governed by

$$\alpha\frac{d^4u_a(t)}{dt^4} + \beta\frac{d^2u_a(t)}{dt^2} + u_a(t) = (1-k_a)V_d \tag{2-9}$$

and its solution is found to be the following:

$$u_a(t) = -k_aV_d + b_1 \cos\omega_1(t-t_0) + b_2 \sin\omega_1(t-t_0) + b_3 \cos\omega_2(t-t_0) + b_4 \sin\omega_2(t-t_0) \tag{2-10}$$

where

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & \omega_1 & 0 & \omega_2 \\ -\omega_1^2 & 0 & -\omega_2^2 & 0 \\ 0 & -\omega_1^3 & 0 & -\omega_2^3 \end{bmatrix}^{-1} \begin{bmatrix} (1-k_a)V_d - V_{a0} \\ \dot{u}_a(t_0) \\ \ddot{u}_a(t_0) \\ \dddot{u}_a(t_0) \end{bmatrix} \tag{2-11}$$

The initial conditions (V_{a0} and u_a's three order derivatives at $t=t_0$) are also determined by the operating conditions and the energy storage components C_{snb}, C_a, L_a and L_s.

The currents i_s, i_m, and i_a are determined respectively by

$$\begin{cases} i_s(t) = \dfrac{1}{kL_s}\int_{t_0}^{t}[V_d - u_{d1}(t)]dt \\ i_m(t) = I_{m0} + \dfrac{1}{L_m}\int_{t_0}^{t}[V_d - u_{d1}(t)]dt \\ i_a(t) = C_a\dfrac{du_a(t)}{dt} \end{cases} \tag{2-12}$$

During this interval, the current through SR_2 is determined by

$$i_{Do2}(t) = I_o - i_s(t) \tag{2-13}$$

And the instantaneous recovery of the discharged power from C_{snb} is governed by

$$p_{rec}(t) = k_a V_d i_a(t) \tag{2-14}$$

Because Interval 1 terminates when u_{d1} reaches zero, namely $u_{d1}(t_1)=0$, the duration of this interval (t_1- t_0) can be determined by substituting the left hand of (2-5) with zero and solving for t_1.

At the end of Interval 1, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_1) = 0 \\ u_a(t_1) = V_{a1} \\ i_a(t_1) = I_{a1} \\ i_p(t_1) = \dfrac{1}{k}i_s(t_1) + i_m(t_1) = I_{p1} \\ i_s(t_1) = I_{s1} \\ i_m(t_1) = I_{m0} + \Delta I_{m1} \end{cases} \tag{2-15}$$

where the net change of the magnetizing current is determined by

$$\Delta I_{m1} = \frac{1}{L_m}\int_{t0}^{t1}[V_d - u_{d1}(t)]dt \tag{2-16}$$

2.4.2.2 Interval 2 ($t_1 \le t < t_2$)

Fig. 2.12b shows the equivalent circuit of Interval 2. The instantaneous values of key variables are restrained by the set of equations given in (A-2). The following are obtained by solving (A-2):

$$\begin{cases} u_a(t) = [V_{a1} + k_a V_d]\cos\omega_3(t-t_1) + I_{a1}\sqrt{\dfrac{L_a}{C_a}}\sin\omega_3(t-t_1) - k_a V_d \\ i_a(t) = -[V_{a1} + k_a V_d]\sqrt{\dfrac{C_a}{L_a}}\sin\omega_3(t-t_1) + I_{a1}\cos\omega_3(t-t_1) \\ i_m(t) = I_{m0} + \Delta I_{m1} + \dfrac{V_d}{L_m}(t-t_1) \\ i_s(t) = I_{s1} + \dfrac{V_d}{kL_s}(t-t_1) \end{cases} \tag{2-17}$$

where the resonant frequency is determined by

$$\omega_3 = 1/\sqrt{L_a C_a} \tag{2-18}$$

The current through SR_2 is still governed by (2-13). For the auxiliary circuit, the instantaneous recovery of the energy discharged from C_{snb} is still governed by (2-14).

Because Interval 2 terminates when i_a reaches zero, from (2-17), the duration of this interval is found to be:

$$(t_2 - t_1) = \frac{1}{\omega_3}\arctan\left(\frac{I_{a1}}{V_{a1} + k_a V_d}\sqrt{\frac{L_a}{C_a}}\right) \tag{2-19}$$

At the end of Interval 2, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_2) = 0 \\ u_a(t_2) = V_{a2} \\ i_a(t_2) = 0 \\ i_p(t_2) = \dfrac{1}{k} i_s(t_2) + i_m(t_2) = I_{p2} \\ i_s(t_2) = I_{s2} \\ i_m(t_2) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} \end{cases} \tag{2-20}$$

where, the net change of the magnetizing current is determined by

$$\Delta I_{m2} = \frac{V_d}{L_m}(t_2 - t_1) \tag{2-21}$$

2.4.2.3 Interval 3 ($t_2 \le t < t_3$)

Fig. 2.12c shows the equivalent circuit of Interval 3. The instantaneous values of key variables are restrained by the set of equations given in (A-3). The following are obtained by solving (A-3):

$$\begin{cases} u_a(t) = [V_{a2} - k_a V_d]\cos\omega_3(t - t_2) + k_a V_d \\ i_a(t) = -[V_{a2} - k_a V_d]\sqrt{\dfrac{C_a}{L_a}}\sin\omega_3(t - t_2) \\ i_m(t) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \dfrac{V_d}{L_m}(t - t_2) \\ i_s(t) = I_{s2} + \dfrac{V_d}{kL_s}(t - t_2) \end{cases} \tag{2-22}$$

The current through SR_2 is still governed by (2-13). For the auxiliary circuit, the instantaneous recovery of the energy discharged from C_{snb} is now governed by

$$p_{rec}(t) = -k_a V_d i_a(t) \tag{2-23}$$

Because Interval 3 terminates when i_s reaches the value of the output inductor current, from (2-22), the duration of this interval can be found to be:

$$(t_3 - t_2) = \frac{kL_s}{V_d}(I_o - I_{s2}) \tag{2-24}$$

At the end of Interval 3, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_3) = 0 \\ u_a(t_3) = V_{a3} \\ i_a(t_3) = I_{a3} \\ i_p(t_3) = \dfrac{1}{k} i_s(t_3) + i_m(t_3) = I_{p3} \\ i_s(t_3) = I_o \\ i_m(t_3) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} \end{cases} \tag{2-25}$$

where, the net change of the magnetizing current is determined by

$$\Delta I_{m3} = \frac{V_d}{L_m}(t_3 - t_2) \tag{2-26}$$

2.4.2.4 Interval 4 ($t_3 \le t < t_4$)

Fig. 2.12d shows the equivalent circuit of Interval 4. The instantaneous values of key variables are restrained by the set of equations given in (A-4). (2-22) is still satisfied except that i_s becomes a constant, namely

$$\begin{cases} u_a(t) = [V_{a2} - k_a V_d]\cos\omega_3(t - t_2) + k_a V_d \\ i_a(t) = -[V_{a2} - k_a V_d]\sqrt{\dfrac{C_a}{L_a}}\sin\omega_3(t - t_2) \\ i_m(t) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \dfrac{V_d}{L_m}(t - t_3) \\ i_s(t) = I_o \end{cases} \tag{2-27}$$

The current through SR_2 is stopped. For the auxiliary circuit, the instantaneous recovery of the energy discharged from C_{snb} is still governed by (2-23).

Because Interval 4 terminates when i_a becomes zero again, the duration of this interval can be found by solving (2-27) and (2-24), and it is determined by:

$$(t_4 - t_3) = (t_4 - t_2) - (t_3 - t_2) = \frac{\pi}{\omega_3} - \frac{kL_s}{V_d}(I_o - I_{s2}) \tag{2-28}$$

At the end of Interval 4, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_4) = 0 \\ u_a(t_4) = V_{a4} \\ i_a(t_4) = 0 \\ i_p(t_4) = I_{p3} + \Delta I_{m4} \\ i_s(t_4) = I_o \\ i_m(t_4) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} \end{cases} \tag{2-29}$$

where, the net change of the magnetizing current is determined by

$$\Delta I_{m4} = \frac{V_d}{L_m}(t_4 - t_3) \tag{2-30}$$

2.4.2.5 Interval 5 ($t_4 \le t < t_5$)

Fig. 2.12e shows the equivalent circuit of Interval 5. The instantaneous values of key variables are restrained by the set of equations given in (A-5).

Because Interval 5 terminates when S_{main} completes its duty ratio in order to regulate the output voltage, the duration, by referring to Fig. 2.3, is given by:

$$(t_5 - t_4) = \frac{D + D_{aux}}{f_{sw}} - t_4 \tag{2-31}$$

At the end of Interval 5, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_5) = 0 \\ u_a(t_5) = V_{a4} \\ i_a(t_5) = 0 \\ i_p(t_5) = I_{p3} + \Delta I_{m4} + \Delta I_{m5} \\ i_s(t_5) = I_o \\ i_m(t_5) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} \end{cases} \tag{2-32}$$

where, the net change of the magnetizing current is determined by

$$\Delta I_{m5} = \frac{V_d}{L_m}(t_5 - t_4) \tag{2-33}$$

2.4.2.6 Interval 6 ($t_5 \le t < t_6$)

Fig. 2.12f shows the equivalent circuit of Interval 6. The instantaneous values of key variables are restrained by the set of equations given in (A-6). The following is obtained by solving (A-6):

$$u_{d1}(t) = V_d - V_d \cos\omega_4(t - t_5) + [\frac{I_o}{k} + i_m(t_5)]\sqrt{\frac{L_m}{C_{snb}}} \sin\omega_4(t - t_5) \tag{2-34}$$

where the resonant frequency is determined by

$$\omega_4 = 1/\sqrt{L_m C_{snb}} \tag{2-35}$$

Because Interval 6 terminates when u_{d1} reaches the value of V_d, the duration of this interval can be obtained by replacing the left hand of (2-34) with V_d and solving for t_6. This yields:

$$(t_6 - t_5) = \sqrt{L_m C_{snb}} \arctan\left[\frac{kV_d}{I_o + ki_m(t_5)}\sqrt{\frac{C_{snb}}{L_m}}\right] \tag{2-36}$$

At the end of Interval 6, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_6) = V_d \\ u_a(t_6) = V_{a4} \\ i_a(t_6) = 0 \\ i_p(t_6) = I_{p3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} \\ i_s(t_6) = I_o \\ i_m(t_6) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} \end{cases} \tag{2-37}$$

where the net change of the magnetizing current is determined by

$$\Delta I_{m6} = \frac{V_d}{\omega_4 L_m}\sin\omega_4(t_6 - t_5) + [\frac{I_o}{k} + i_m(t_5)][1 - \cos\omega_4(t_6 - t_5)] \tag{2-38}$$

2.4.2.7 Interval 7 ($t_6 \le t < t_7$)

Fig. 2.12g shows the equivalent circuit of Interval 7. The instantaneous values of key variables are restrained by the set of equations given in (A-7). The following are obtained by solving (A-7):

$$\begin{cases} u_{d1}(t) = V_d + [\frac{I_o}{k} + i_m(t_6)]\sqrt{\frac{L_e}{C_{snb}}}\sin\omega_5(t - t_6) \\ i_s(t) = I_o - \frac{L_e}{k^2 L_s}[I_o + ki_m(t_6)][1 - \cos\omega_5(t - t_6)] \end{cases} \tag{2-39}$$

where the net change of the magnetizing current is determined by

$$\omega_5 = 1/\sqrt{L_e C_{snb}} \approx 1/\sqrt{k^2 L_s C_{snb}} \tag{2-40}$$

Because Interval 7 terminates when i_s becomes zero, its duration can be obtained

by replacing the left hand of (2-39) with zero and solving for t_7. This yields:

$$(t_7 - t_6) = \sqrt{L_e C_{snb}} \arccos\left(1 - \frac{k^2 L_s I_o}{L_e I_o + k L_e i_m(t_6)}\right) \tag{2-41}$$

S_{main} drain voltage will reach a peak value given by the following:

$$V_{pk} = V_d + [\frac{I_o}{k} + i_m(t_6)]\sqrt{\frac{L_e}{C_{snb}}} \sin \omega_5 (t_7 - t_6) \tag{2-42}$$

At the end of Interval 7, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_7) = V_{pk} \\ u_a(t_7) = V_{a4} \\ i_a(t_7) = 0 \\ i_p(t_7) = i_m(t_7) \\ i_s(t_7) = 0 \\ i_m(t_7) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} + \Delta I_{m7} \end{cases} \tag{2-43}$$

where the net change of the magnetizing current is determined by

$$\Delta I_{m7} = \frac{-1}{\omega_5 L_m}[\frac{I_o}{k} + i_m(t_6)]\sqrt{\frac{L_e}{C_{snb}}}[1 - \cos \omega_5 (t_7 - t_6)] \tag{2-44}$$

2.4.2.8 Interval 8 ($t_7 \leq t < t_0 + 1/f_{sw}$)

Fig. 2.12h shows the equivalent circuit of Interval 8. The instantaneous values of key variables are restrained by the set of equations given in (A-8). The following are obtained by solving (A-8):

$$\begin{cases} u_{d1}(t) = V_d + (V_{pk} - V_d)\cos \omega_4 (t - t_7) + i_m(t_7)\sqrt{\frac{L_m}{C_{snb}}} \sin \omega_4 (t - t_7) \\ i_m(t) = -(V_{pk} - V_d)\sqrt{\frac{C_{snb}}{L_m}} \sin \omega_4 (t - t_7) + i_m(t_7)\cos \omega_4 (t - t_7) \end{cases} \tag{2-45}$$

The current through SR_2 is governed by (2-13).

Interval 8 is the last interval of a complete switching cycle. At the end of this

interval, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_0+1/f_{sw}) = V_{end} \\ u_a(t_0+1/f_{sw}) = V_{a4} \\ i_a(t_0+1/f_{sw}) = 0 \\ i_p(t_0+1/f_{sw}) = i_m(1/f_{sw}) \\ i_s(t_0+1/f_{sw}) = 0 \\ i_m(t_0+1/f_{sw}) = I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} + \Delta I_{m7} + \Delta I_{m8} \end{cases} \tag{2-46}$$

where ΔI_{m8} is the net change of the magnetizing current in Interval 8, and V_{end} is the final value of S_{main} drain voltage at the end of the switching cycle, which are given below:

$$\begin{cases} \Delta I_{m8} = -(V_{pk}-V_d)\sqrt{\dfrac{C_{snb}}{L_m}}\sin\omega_4(\dfrac{1}{f_{sw}}+t_0-t_7) - i_m(t_7)[1-\cos\omega_4(\dfrac{1}{f_{sw}}+t_0-t_7)] \\ V_{end} = V_d + (V_{pk}-V_d)\cos\omega_4(\dfrac{1}{f_{sw}}+t_0-t_7) + i_m(t_7)\sqrt{\dfrac{L_m}{C_{snb}}}\sin\omega_4(\dfrac{1}{f_{sw}}+t_0-t_7) \end{cases} \tag{2-47}$$

2.4.2.9 The Sufficient and Necessary Conditions for Steady State Operation

The sufficient and necessary condition for steady state operation is that all variables have the same values respectively at the end of Interval 8 and beginning of Interval 1. Comparing (2-1) and (2-46), this sufficient and necessary condition yields:

$$\begin{cases} V_{end} = (1+\delta)V_d \\ V_{a4} = V_{a0} \\ \sum_{j=1}^{8} \Delta I_{mj} = 0 \end{cases} \tag{2-48}$$

Equation (2-48) also indicates that the successful reset of the power transformer requires the total change of the magnetizing current to be zero in a complete cycle.

2.4.3 Influences of Non-ideal Properties of Components/Devices on the Analysis

The above analysis has been made under the assumptions of using ideal

components and devices. In fact, each component has some non-ideal properties. For example, the leakage of the transformers, the ON resistance and the inherent capacitance of MOSFET switches, and so on. It is important to determine the validity of the above analysis after these non-ideal properties are taken into account.

The ON resistance of a MOSFET causes the so-called conduction losses, and they can be negligible if a very low Rds(ON) device is chosen. The inherent capacitors indeed have some effects on the performance of the switch. But S_{main} output capacitor can be considered a part of C_{snb}, and the effects of input capacitor of both S_{main} and S_{aux} can be made negligible by employing strong gate drives.

The S_{aux} output capacitor C_{oss} causes the so-called $\frac{1}{2}CV^2$ switching losses. Such losses can be made nearly negligible by employing low output capacitor devices. However, as long as C_{oss} is not absolutely zero, it causes some asymmetrical ringing in the waveform of i_a after S_{aux} is turned off. It is because L_a resonates alternately with C_{oss} and C_a in different half cycles of the resonance. When i_a flowing into the drain of S_{aux} (that has already been turned off), L_a resonates with C_{oss}, and i_a will display a very high frequency dominated by C_{oss} and L_a. When i_a flows out of the drain in its second half of oscillation, i_a bypasses C_{oss} by taking the path of S_{aux} body diode. Then i_a will display a lower frequency determined by C_a and L_a. Due to the damping of the real circuit and also because of the insignificant energy involved, this asymmetrical resonance will die very fast. Furthermore, it does not have any significant influence on the ZVS operation and the self-reset of the power transformer. Thus, the thesis does not discuss this issue any further.

The SRs, which are normally ultra-low Rds(ON) MOSFETs, can be made very

close to ideal rectifiers by employing the self-driven techniques.

The effects of the equivalent series resistance (ESR) of C_{snb} and C_a can be made negligible as long as the low ESR ceramic capacitors is chosen for the C_{snb} and C_a.

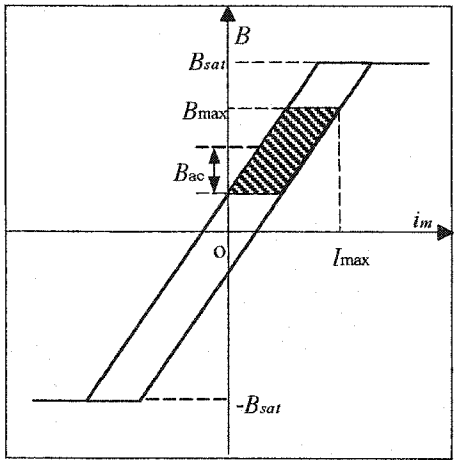
The effects of the forward drops and reverse recovery of the diodes can be made negligible by choosing Schottky diodes or the ultra-fast diodes.

The effect of T_a leakage inductance can considered a part of L_a, and T_p leakage inductance can be considered as a part of L_s.

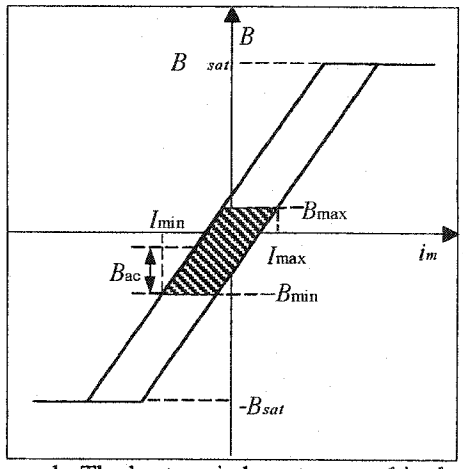
Since the selection of components usually observe common rules, namely using low Rds(ON) MOSFETs, ultra-fast recovery diodes, low ESR capacitors, etc, the above analysis is valid for a practical circuit.

2.5 FLUX EXCURSION IN THE SELF-RESET POWER TRANSFORMER

As seen from the above analysis, the power transformer resetting process is different from the standard forward transformer using the tertiary reset winding. For the latter one, the flux-swing is fixed in the first quadrant of the hysteresis loop, and the magnetizing current always start from the origin. In contrast, the flux swing of the self-reset transformer may shift over the first and third quadrants of the hysteresis loop, in order to satisfy the steady state constrains as given by (2-48). This behavior depends on the circuit parameters (C_{snb}, L_s, L_m, R_E, etc.), the operating conditions (V_d and I_o), and the dc flux bias that is related to I_{m0} and indirectly represented in the instantaneous magnetizing current $i_m(t)$. When the operating condition changes, the dc flux bias may change in accordance. Fig. 2.13 compares the flux excursion and hysteresis loop traversed in the standard and self-reset transformers.



a. The hysteresis loop traversed in the conventional forward transformer



b. The hysteresis loop traversed in the self reset transformer

Fig. 2.13 Comparison of the flux excursion and the hysteresis loop traversed in the conventional forward transformer and the self reset transformer.

The magnetic core of a real transformer creates some core loss, and the loss is determined by the ac flux excursion range. Besides, the core may saturate at certain flux density. It is crucial to investigate the behavior of flux excursion in the self-reset power transformer. Under all operating conditions it should prevent an excessive excursion range as well as the peak flux density that is the sum of the dc flux bias and the magnitude of the ac flux swing.

2.5.1 Self-Reset Transformer Losses

The first important issue is to investigate the core and copper losses caused by the self-reset transformer. The core losses are determined by the area of the hysteresis loop that the flux excursion traverses, and they are approximately proportional to the square of the ac peak flux density. The total flux swing range is determined by the sum of (2-16), (2-21), (2-26), (2-30), (2-33) and (2-38). Thus, increasing L_m will narrow the swing range of magnetizing current, and this reduces the ac peak flux density and the core losses as

well. This can be done by adding more turns in the magnetizing winding. However, it increases the copper losses as well as the transformer size and weight. Hence, a compromise in selecting L_m should be made to minimize the total transformer losses, and it is well treated in conventional design. A question here is whether the conventional design suits for the self reset transformer.

Fortunately, the core losses as well as the copper losses in the self reset transformer do not differ much from those in the conventional forward transformer, if they are designed the same except for the absence of the tertiary reset winding in the former one. The reason is as follows. The ac flux peak is almost half of the upward swinging (or equally the downward swing) excursion of the flux. When the main switch is ON, the flux swings up linearly, and this upward swing is proportional to the input dc voltage and the duty ratio of the main switch. If the operating conditions are the same, the main switch will have almost the same duty ratio, and the ac peak flux in both the self-reset transformer and a conventional one will be the same, although the dc flux bias may differ. Hence, the core losses will be the same in both transformers.

The copper losses are determined by the power that the transformer delivers. Both conventional transformer and the self-reset one will suffer from almost the same copper losses for the same output power. Some negligible difference in copper losses may exist due to their different dc bias in magnetizing current, which is normally much less than the full load current.

In conclusion, the self-reset transformer can achieve self-reset without sacrificing copper and core losses. Therefore, the self-reset transformer can follow the well-developed conventional design procedure, and this saves the development time.

2.5.2 *Flux Excursions*

The other important issue is to maintain the flux excursion well below the saturation point. In the following, detailed examination of the absolute flux swing is performed by solving (2-48) using MathCAD software, and the flux density is discussed directly for convenient evaluation. Since the hysteresis loop is complex, a linear model is used instead. Thus, by applying the following equation to (2-48), one will convert the constrains of magnetizing current i_m into the constrains of the flux density B.

$$B(i_m) = \frac{L_m}{N_p A_e} i_m \tag{2-49}$$

where A_e is the effective cross-sectional area of the transformer magnetic core.

From the above analysis, the flux swing boundaries are defined by the following:

$$\begin{cases} B_{\min} = B(I_{m0}) \\ B_{\max} = B(I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6}) \end{cases} \tag{2-50}$$

The MathCAD spreadsheet that calculates the flux swing range, namely $B_{\max}$ and $B_{\min}$, is provided in Appendix E. The following discussion is made using the example of the prototype converter. Table 2.1 lists the principal parameters and operating conditions of this prototype. The power transformer is designed in a conventional way but the tertiary reset winding is simply eliminated.

2.5.3 *An Insight into the Flux Excursion*

Fig. 2.14 shows the flux excursion as functions of V_d, I_o, L_m, L_s, and C_{snb} in the prototype circuit, which are obtained using the MathCAD spreadsheet. Simulation results using Pspice are presented to verify the analysis. A close look of these curves shows that the flux excursion moves toward the first quadrant from the third quadrant of the

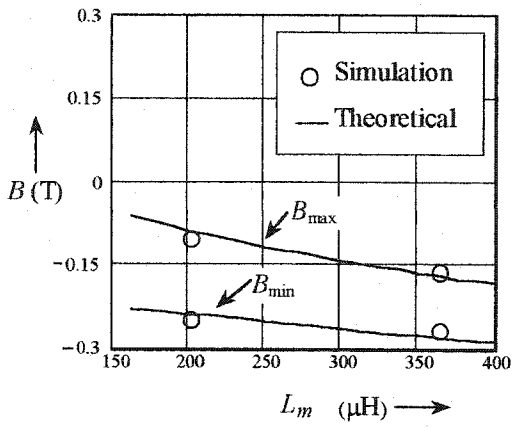
hysteresis loop as the load decreases. The reason can be found in (2-42). S_{main} peak drain voltage V_{pk} is proportional to the load current, and during the reset process it counteracts the input voltage V_d to drive the magnetizing current i_m backward. At light load, V_{pk} is lower, resulting in a weaker driving force to reverse i_m.

It is also seen in these curves that at full load, the excursion traverses only the third quadrant of the hysteresis loop. It means a negative magnetizing current. Benefited from this negative current are the slightly reduced copper losses, since the current stress on the primary winding is likely to reduce. The following are the detail discussions.

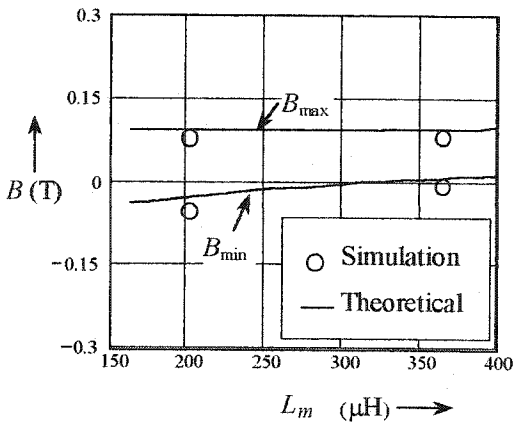
***2.5.3.1** Flux Excursion vs. Magnetizing Inductance L_m*

Fig. 2.14a and b show the flux excursion as a function of the magnetizing inductance L_m. These curves point out that a large L_m reduces the excursion range and hence the core losses. It seems an ungapped core is better in the sense of achieving a higher value of L_m.

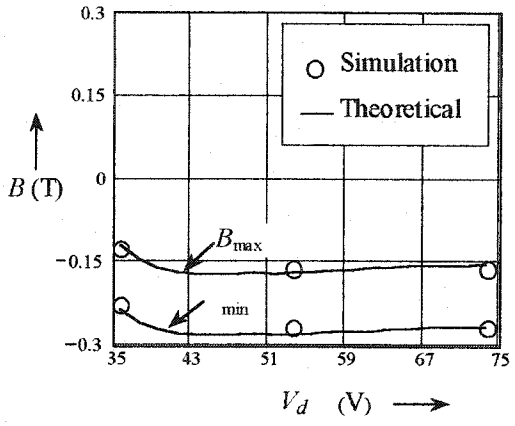
However, at full load, a very large L_m will drive the excursion deeper into the third quadrant of the hysteresis loop and approaches the negative saturation point. This can be explained by observing (2-35) and (2-45). A large L_m results in a slower resonant frequency ω_4, thus C_{snb} can easily hold its voltage without losing much during Interval 8. Consequently the negative voltage pulse with extra voltage-second-product is applied to L_m and this drives the flux to swing back deeper into the third quadrant. This implies that an excessive large L_m by using the un-gapped core or by adding more turns in the magnetizing winding may drive the transformer into saturation.



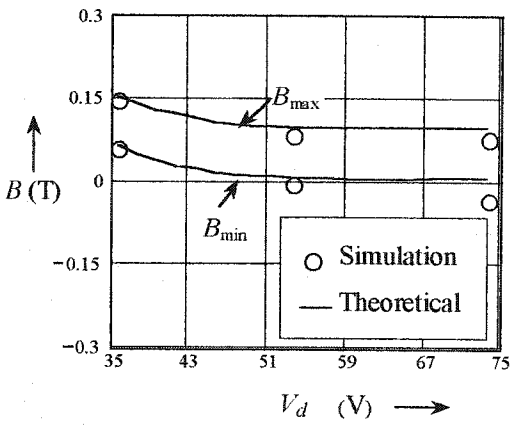
a. Flux density vs. magnetizing inductance at full load. (I_o=20A, L_s=0.3μH, C_{snb}=16nF, V_d=55V).



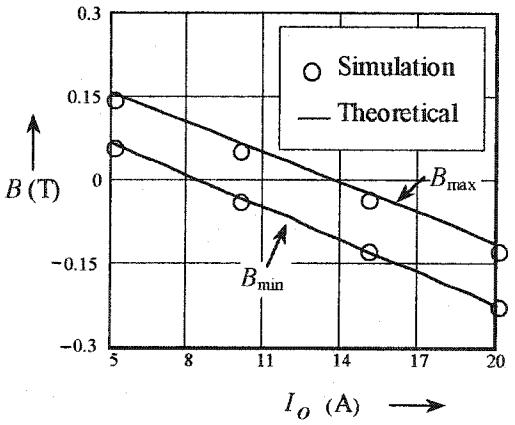
b. Flux density vs. magnetizing inductance at light load. (I_o=5A, L_s=0.3μH, C_{snb}=16nF, V_d=55V).



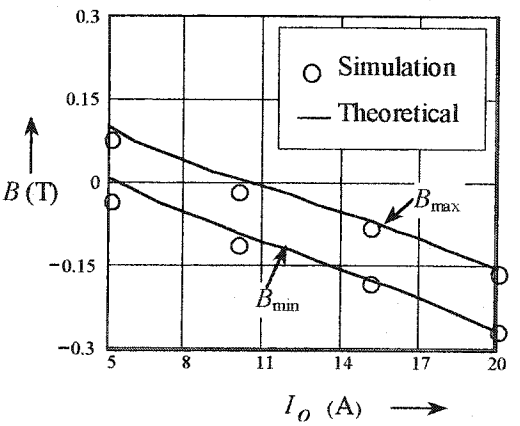
c. Flux density vs. input voltage at full load. (L_m=320μH, L_s=0.3μH, C_{snb}=16nF, I_o=20A).



d. Flux density vs. input voltage at light load. (L_m=320μH, L_s=0.3μH, C_{snb}=16nF, I_o=5A).

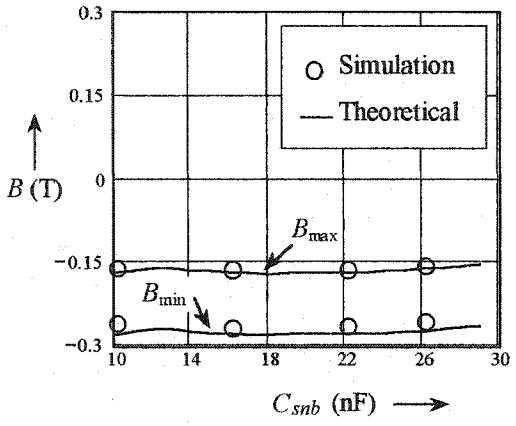


e. Flux density vs. load current at low input voltage. (V_d=35V, L_m=320μH, L_s=0.3μH, C_{snb}=16nF).

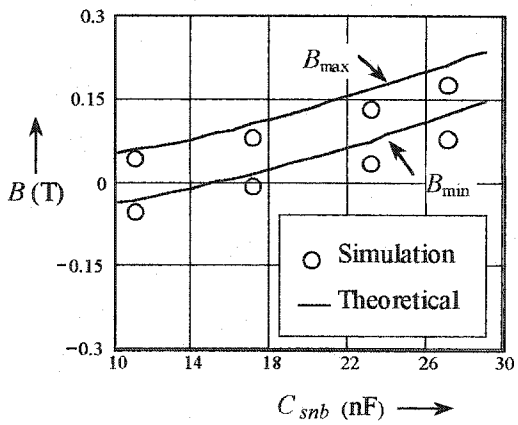


f. Flux density vs. load current at high input voltage. (V_d=75V, L_m=320μH, L_s=0.3μH, C_{snb}=16nF).

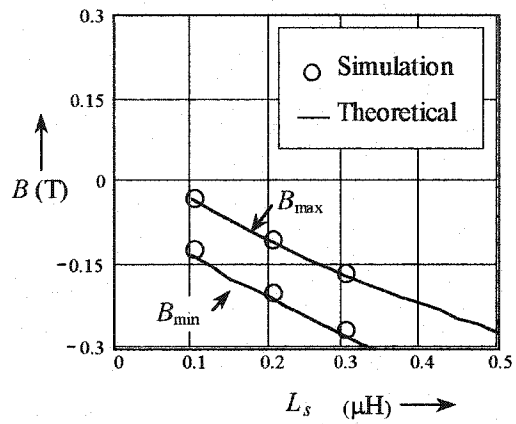
Fig. 2.14 The flux excursion as function of different circuit parameters. The flux density swings back and forth between the two boundaries, B_{max} and B_{min}. The output voltage V_o =5V, switching frequency is 200 kHz.(*To be continued on the next page*).



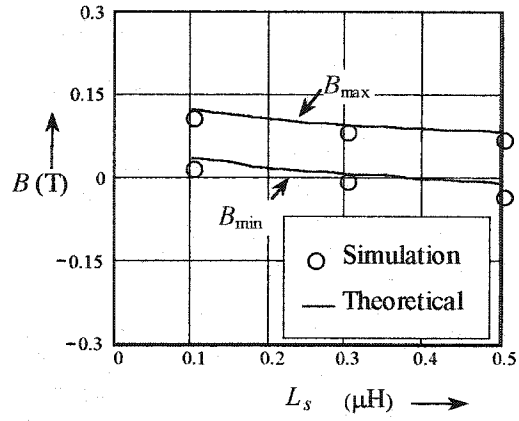
g. Flux density vs. snubber capacitor at full load. (L_m=320μH, L_s=0.3μH, V_d=55V, I_o=20A).



h. Flux density vs. snubber capacitor at light load. (L_m=320μH, L_s=0.3μH, V_d=55V, I_o=5A).



i. Flux density vs. current limiting inductor at full load. (L_m=320μH, C_{snb}=16nF, V_d=55V, I_o=20A).



j. Flux density vs. current limiting inductor at light load. (L_m=320μH, C_{snb}=16nF, V_d=55V, I_o=5A).

Fig. 2.14 (*Continued from last page*) The flux excursion as function of different circuit parameters.

2.5.3.2 Flux Excursion vs. Input Voltage V_d

Fig. 2.14c and d show the flux excursion as a function of the input voltage V_d. Over a wide range of V_d, the excursion remains almost independent of V_d. The reason can also be found in (2-42). The reset driving force is the difference between V_{pk} and V_d, and this voltage difference is almost independent of V_d.

As the input voltage decreases to the lowest point, the flux excursion moves

deeper into the first quadrant. This is mainly because the duty ratio is larger at a lower input voltage, and this leaves shorter time for the magnetizing current to swing backward. If not designed properly, the swing may exceed the saturation point under the conditions of light load and minimum input voltage. Thus, special attention shall be paid to such conditions.

2.5.3.3 Flux Excursion vs. Load Current I_o

Fig. 2.14e and f show the flux excursion as a function of the output current I_o. As the load decreases, the excursion shifts towards the first quadrant. This does not increase the conduction losses at light load, because of the reduced load current.

2.5.3.4 Flux Excursion vs. Snubber Capacitor C_{snb}

Fig. 2.14g and h show the excursion as a function of the snubber capacitor C_{snb}. At full load, the excursion is almost independent of C_{snb} value. Although a large C_{snb} can easily hold its voltage in Interval 8, it will increase the duration of Interval 6, and this reduces the duration of Interval 8, such that the negative voltage pulse applied to L_m does not significantly change the volt-second product, and thus the flux backward swing does not change significantly.

But at light load, the larger the snubber, the higher the excursion moves up into the first quadrant of the hysteresis loop. The reason can still be found in (2-42); the peak voltage of the main switch is in inverse proportion to C_{snb}. A larger C_{snb} results in a lower V_{pk} and hence a weaker force to drive i_m backward during the reset process. Thus, the value of C_{snb} should be limited.

2.5.3.5 Flux Excursion vs. Current Limiting Inductor L_s

Fig. 2.14i and j show the excursion as a function of the current limiting

inductance L_s. A larger L_s will move the excursion deeper into the third quadrant of the hysteresis loop. It is because, as seen in (2-4) and (2-42), a larger L_s results in a higher V_{pk} that produces a stronger force to drive i_m downward during the reset process.

The spreadsheet does not find solutions when L_s is smaller than 0.1 μH, and Pspice simulation confirms this as it does not converge. This indicates that L_s plays a crucial role in the self reset topology, and a too small L_s will not satisfy (2-48), meaning that a successful self-reset cannot be obtained. Consequently, L_s should be limited at both ends so that self-reset is obtainable while the excursion does not reach the saturation point in the third quadrant.

2.6 EXPERIMENTAL AND SIMULATION RESULTS

Experimental and simulation results are presented in the following to verify the steady state analysis made in this chapter, and also to prove the concepts of ZVS and self reset operation.

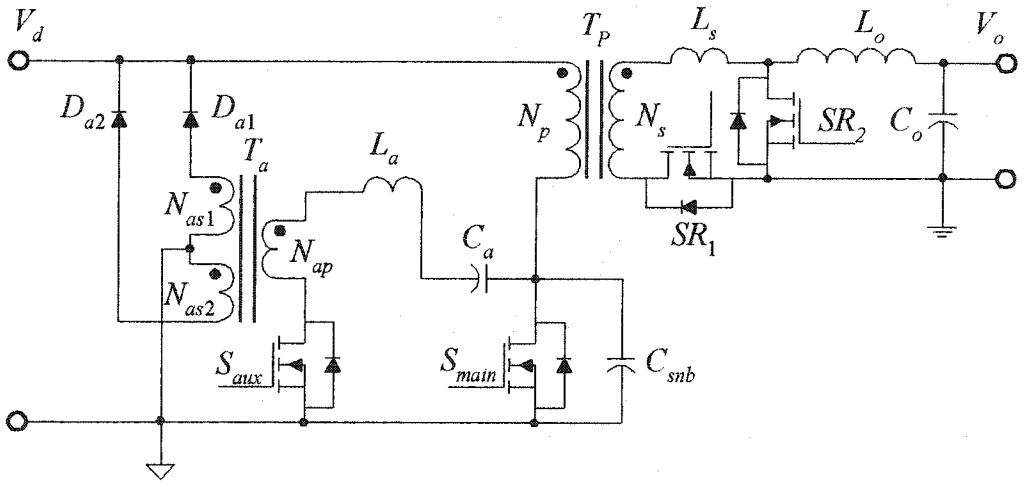


Fig. 2.15 The prototype converter of Type 1 topology using MOSFET SRs.

Table 2. 1 Principal Parameters of the Prototype Converter

Components	Values	Selections
$V_{d\ min}$, V_{in_max}	35, 60V	
P_o	100W (V_o=5V,I_o=20A)	
D_{min}/ D_{max}	0.2 / 0.45	
T_P	L_m=360 μH(k=N_p/N_s=12/4)	ETD29-PC40**
S_{main}	Rds(on)=0.18 Ω	IRF640*
SR_1/SR_2	Rds(on)=0.009 Ω	MTP75N05*
C_{snb}	16 nF	Ceramic
L_s	0.3 μH	Magnetic bead
L_a	2 μH	Gapped RM4-4C6**
C_a	66 nH	Ceramic
S_{aux}	Rds(on)=0.18 Ω	IRF640
L_o	12 μH	MPP Core**
C_o	400 μF	Tantanlum+Electrolyte
D_{a1}, D_{a2}	V_F=0.8V	MUR860
T_a	L_m=50 μH (N_p/N_s=3/18)	RM4/I-3C3**
Controller		UC3855AN***
Q_3		IRF510

*using two paralleled devices.
**Optimized magnetics, courtesy of Pulse Engineering, Inc., Kanata, Ontario, Canada.
***Unitrode samples, courtesy of Texas Instruments Inc.

Fig. 2.15 shows the prototype converter topology employing the MOSFET SRs. It is built to operate at 200 kHz under an input voltage range of 35 to 60 Vdc, and the output voltage is 5 Vdc with a load of 100 W. The principal circuit parameters are given in Table 2.1. The self-driven SR techniques reported in [110] are also employed in this prototype circuit. The Psipce model of this prototype converter is given in Appendix I.

2.6.1 Simulation Results

Previously, some Pspice simulation results have been presented in Fig. 2.14 for the verification of the theoretically predicted flux excursion. The slight differences

between the simulation and the theoretical results arises from the fact that the predicted results are based on ideal circuit parameters, while the Pspice model of the circuits uses more realistic ones. After all, Fig. 2.14 shows a good agreement between the predictions and simulation, indicating the analysis made in Section 2.4 is valid and applicable to a real circuit. In the following, typical waveforms obtained from simulation are presented as the proof-of-concept.

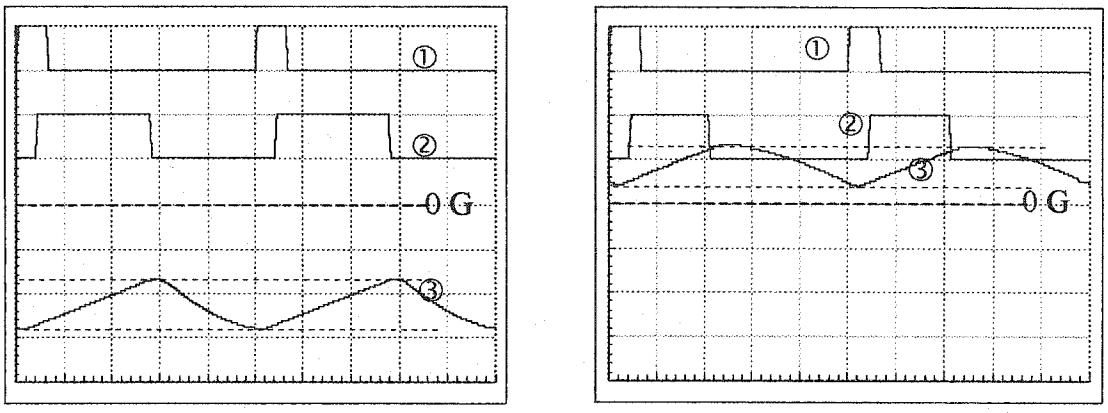
2.6.1.1 Flux Excursion under Different Load Conditions.

Fig. 2.16 shows typical waveforms of the flux excursion vs. gating signal under various load conditions. Self-reset is achieved since the flux returns to the same point after each cycle. Secondly, the flux excursion shifts from the third quadrant into the first quadrant of the hysteresis loop as the load decreases, verifying the analytical results given in Section 2.5.2. The flux excursion range also confirms with the theoretical predictions.

2.6.1.2 Soft Switching

Fig. 2.17 shows typical waveforms of S_{main} ZVS operation under different load conditions. It also shows how S_{main} drain voltage is pulled down to zero by the resonant current in the auxiliary circuit, namely S_{aux} drain current. Under both full and light load conditions, ZVS turn-on and turn-off are always achieved in S_{main}, as indicated by the non-overlapped drain current and voltage in switching transients.

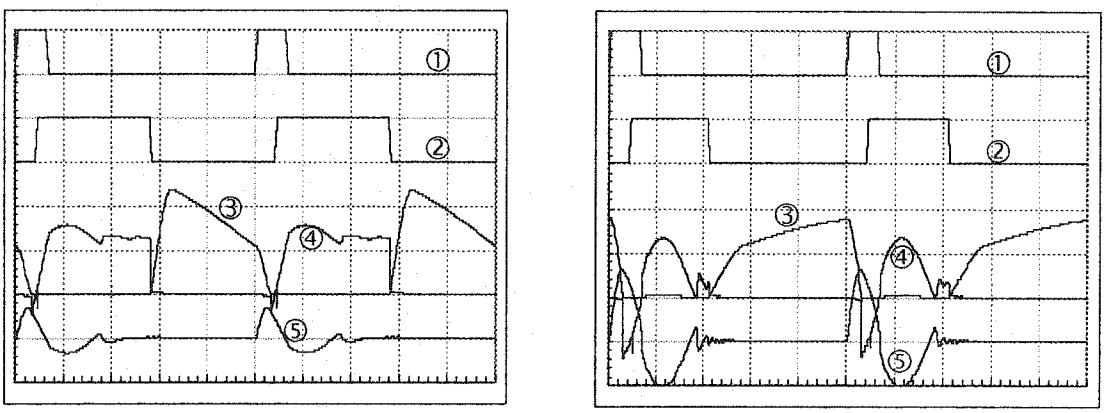
Fig. 2.18 shows typical waveforms of S_{aux} soft switching operation. Due to the resonant current, the auxiliary switch achieves a ZCS turn-on and a ZVS turn-off. The waveforms also prove the discussion of Section 2.3.4 on the effects of C_{oss} on the auxiliary circuit current after S_{aux} is turned off, namely the asymmetrical resonance after the auxiliary circuit current complete the second half cycle.



a. Flux excursion under full load (I_o=20A)

b. Flux excursion under light load (I_o=5A)

Fig. 2.16 Simulation results: flux excursion under different load conditions.
Traces: ①S_{aux} gating (10V/div.), ②S_{main} gating (10V/div.), ③Flux density (1000G/div.). Timing-1μs/div. Operating frequency f_{sw}=200kHz. V_d = 40V



a. ZVS under full load (P_o=100W)

b. ZVS under light load (P_o=25W)

Fig. 2.17 Simulation results: S_{main} ZVS operation under different load conditions.
Traces: ①S_{aux} gating (10V/div), ②S_{main} gating (10V/div), ③S_{main} drain voltage (50V/div), ④S_{main} drain current (5A/div), ⑤S_{aux} drain current (5A/div). Timing-1μs/div. f_{sw}=200kHz.

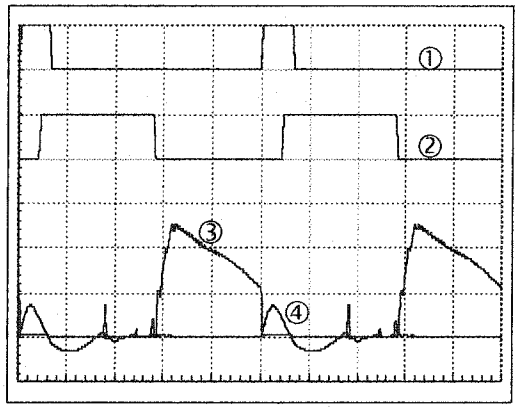


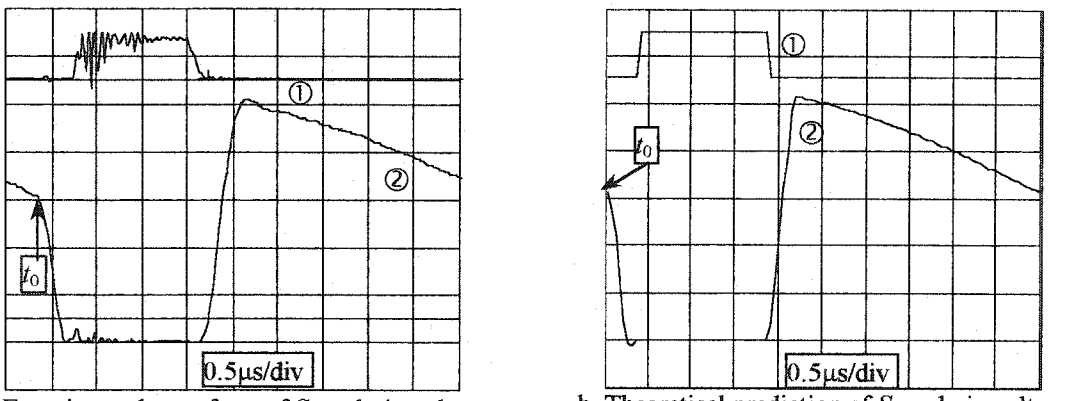
Fig. 2.18 Simulation results: typical waveforms of S_{aux} soft switching.
Traces: ①S_{aux} gating (10V/div), ②S_{main} gating (10V/div), ③ S_{aux} drain voltage (50V/div), ④ S_{aux} drain current (5A/div). Timing-1μs/div. Operating frequency f_{sw}=200kHz.

2.6.2 Experimental Results

Experimental results are obtained on the prototype circuit. The nominal operating frequency is 200kHz, the nominal output voltage is 5V, and the full load current is 18A. Typical experimental results are presented in the following to verify the analysis and to provide proof-of-concepts.

2.6.2.1 Experimental Verification of the Analysis

Fig. 2.19 shows the comparison of S_{main} drain voltage waveform between the experiment and theoretical prediction. Quantitative comparison is given in Table 2.2.



a. Experimental waveform of S_{main} drain voltage

b. Theoretical prediction of S_{main} drain voltage

Fig. 2.19 Experimental verification of the analysis
Traces: ①S_{main} gating (5V/div), ② S_{main} drain voltage (20V/div). Operating conditions: f_{sw}=200kHz, V_d=55V, I_o=18A.

Table 2.2 Comparison of theoretical and experimental drain voltage of S_{main}

Comparison	**S_{main} duty ratio**	**S_{main} Drain Voltage Pulse**				
		0V duration	**Value at t_0**	**Interval 1 Duration**	**Peak value**	**Risr time to reach peak**
Theoretical	28.6%	1.58μs	63.9V	0.26μs	103.5V	0.37μs
Experimental	26.5%	1.52μs	61.7V	0.33μs	101.8V	0.48μs

The small difference between the experimental results and the theoretical predictions in Table 2.2 can be explained as follows. In reality, L_s reduces its inductance when a large current flows through, and this saturation tendency is not considered in the analysis due to the complexity that may involve. Thus, the duration of Interval 3 that is a portion of S_{main} duty ratio is actually shorter than the theoretical prediction by (2-24), and so is the visible duty ratio or the 0V-duration of the drain voltage. The reduced L_s also reduces the peak drain voltage as seen in (2-42).

Above all, the theoretical and experimental wave-shapes shown in Fig. 2.19 and the specific values shown in Table 2.2 indicate good agreements, and this again indicates that the analysis made in this chapter is valid.

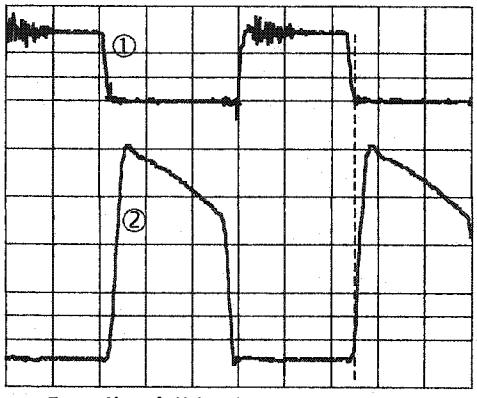
2.6.2.2 Proof-of-Concept Key Waveforms

Fig. 2.20 shows typical experimental waveforms of S_{main} under different operating conditions. The high frequency ringing is mainly the noise picked up by the probe ground leads of the oscilloscope that is used to capture the waveforms.

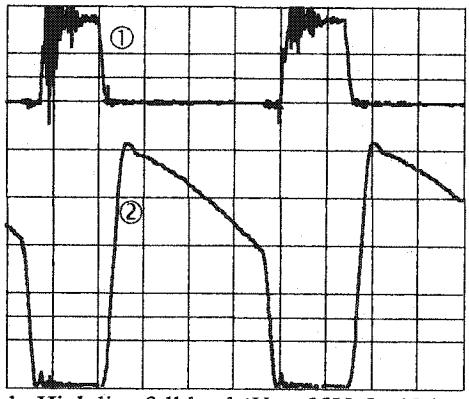
S_{main} drain current waveform is not captured due to the reason that a long wire loop would need to be inserted into the circuit to accommodate the current probe and that would interfere with the normal operation.

However, it can still be concluded from Fig. 2.20 that ZVS is achieved in S_{main}. Because, at turn-on, S_{main} gating signal arrives after the drain voltage has already reached zero, and at turn-off, it is withdrawn completely before the drain voltage starts to rise.

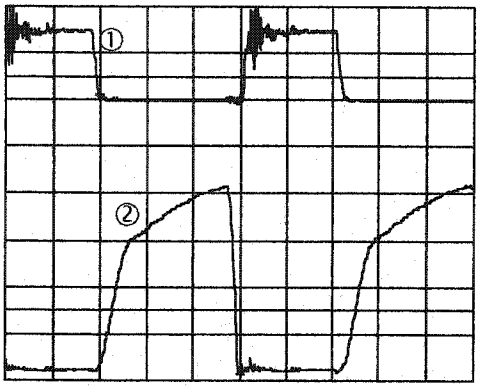
Fig. 2.21 shows typical experimental waveforms of the auxiliary switch S_{aux} under different operating conditions. It is seen that a ZCS turn-on and a ZVS turn-off are always achieved in S_{aux}.



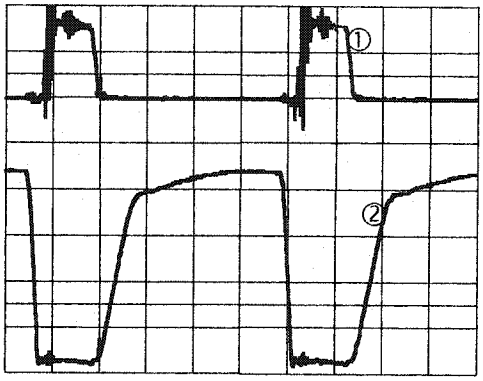
a. Low line full load (V_d = 35V, I_o=18A)



b. High line full load (V_d = 55V, I_o=18A).

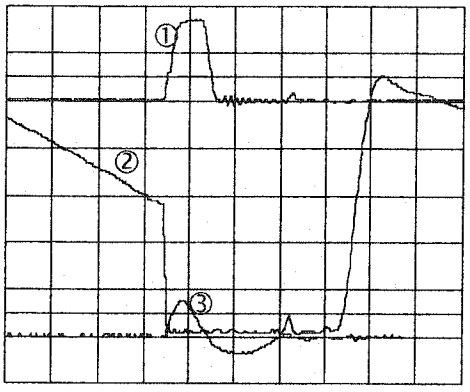


c. Low line light load (V_d = 35V, I_o=5A).

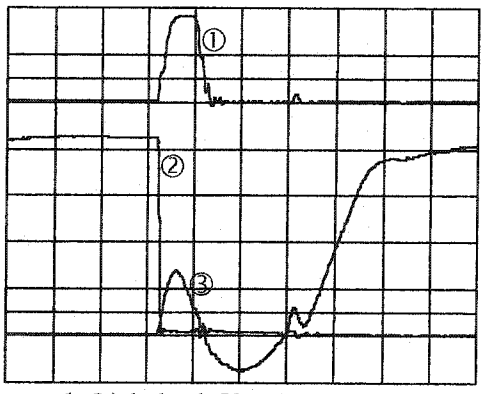


d. High line light load (V_d = 55V, I_o=5A).

Fig. 2.20 Typical experimental waveforms of the main switch.
Traces: ①S_{main} gating (5V/div), ② S_{main} drain voltage (20V/div). Timing-1μs/div. Operating frequency f_{sw}=200kHz.

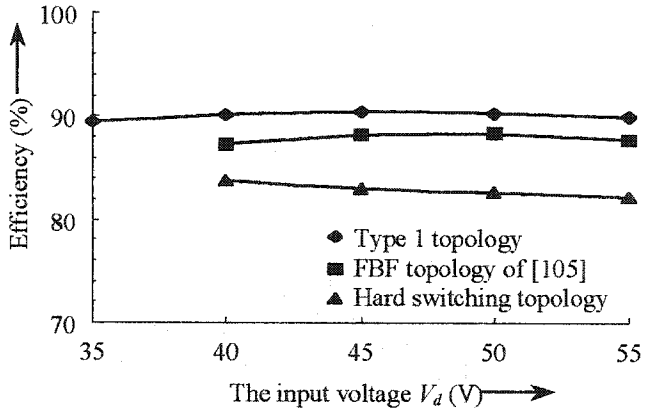


a. Full load (V_d = 55V, I_o=18A).

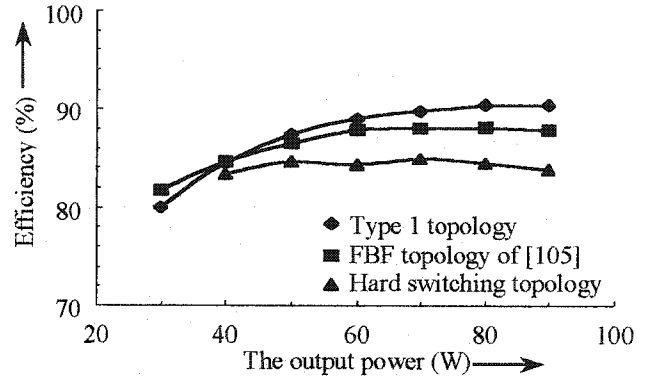


b. Light load (V_d = 55V, I_o=5A).

Fig. 2.21 Typical experimental waveforms of the auxiliary switch.
Traces: ①S_{aux} gating (5V/div), ② S_{aux} drain voltage (20V/div), ③ S_{aux} drain current (5A/div). Timing-0.5μs/div. Operating frequency f_{sw}=200kHz.



a. The efficiency vs. input voltage at full load (90 W).



b. The efficiency vs. output power under fixed input voltage (45 V).

Fig. 2.22 The overall efficiency of the Type 1 converter topology.

2.6.2.3 Efficiency

Fig. 2.22 shows the experimental results of the overall efficiency under different operating conditions. The Type 1 topology has about 90% efficiency at full load over input voltage range from 35 to 55V. Above 55V the prototype converter loses ZVS due the saturation of L_s at high input voltage. The reduced efficiencies in these abnormal input voltage ranges are irrelevant to the comparison here and hence they are not shown in Fig. 2.22.

Seen from Fig. 2.22a, as the function of input voltage, the efficiency at full load is the highest at the middle point of the input voltage range, and it reduces slightly at both

ends of the input voltage range. The reasons are as follows. At a lower input voltage, a higher rms current flows for a given output power, thus the conduction losses are higher. At a higher input voltage, although the conduction losses in the power circuit decrease, the auxiliary circuit will be slightly less efficient. It is because the snubber capacitor stores more energy to discharge at a higher input voltage, and a higher auxiliary current is required, and this increases the conduction losses in the auxiliary circuit.

At middle point of the input voltage range, neither does the conduction losses in the power circuit nor the losses in the auxiliary circuit go excessive, thus the converter has the highest overall efficiency.

As a function of the load, as seen in Fig. 2.22b, the efficiency is almost constant when the load decreases from 100% to about 50% of the full load. Further decreasing the load causes the efficiency to decrease rapidly. This can be explained in the following. Because the circuit achieves soft switching, the major losses are the conduction losses. When the load decrease, the conduction losses also decrease, and this yields an almost constant efficiency. However, when the load decreasing further, the losses in the auxiliary circuit, and the core loss of the power transformer that is independent of load conditions, become significant and causes the efficiency to decrease.

Above all, the Type 1 self reset ZVS topology has about 2-3% better efficiency than the FBF ZVS forward topology that employs a non-resonant auxiliary circuit, and about 8% higher than a hard-switching counterpart.

2.7 CONCLUSIONS

In this chapter the Type 1 ZVS and self-reset forward converter topology has been presented. It employs a resonant auxiliary circuit and a simplified power transformer. The

steady state operation of the topology and the flux excursion in the self-reset transformer have been analyzed and verified with simulation and experimental results.

With the improvement in soft switching, the prototype converter achieves 90% efficiency at full load, and better efficiency is expected on a refined circuit built on PCB. Besides, the Type 1 converter topology has the following advantages as compared to existing soft switching forward topologies:

(i) Guaranteed ZVS of the main switch independent of the operating conditions;

(ii) Soft switching of the auxiliary switch;

(iii) Self resetting of the power transformer without using the tertiary reset winding,

(iv) Simple control and gate-drive design for the auxiliary switching, without the need of gate drive isolation and gating pulse width modulating;

(v) Recovery of the energy related to the leakage inductance in the auxiliary circuit.

Owing to these advantages, the Type 1 topology can be used to implement the proposed DPUPS in Chapter 4.

However, the Type 1 converter topology has the following two major drawbacks:

(i) The current limiting inductor might be difficult to design due to the saturation problems under high load current, and also due to the difficulty in yielding the low but specific inductance value.

(ii) Because of the unclamped drain voltage in the Type 1 topology, the main switch drain voltage stress might be higher than in a conventional forward converter topology.

To solve these problems, another ZVS and self-reset forward topology (Type 2) will be presented in the next chapter.

CHAPTER 3

ZVS AND SELF-RESET FORWARD CONVERTER TOPOLOGY (TYPE 2)

3.1 INTRODUCTION

In the Type 1 converter topology, the secondary side inductor L_s plays an important role to fulfill two key functions. One is to limit the speed of rise of the primary current during Interval 1, such that the snubber capacitor can be completely discharged to provide ZVS condition for the main switch to turn-on. The other function is to resonate with the snubber capacitor after the main switch is turned off, such that a negative voltage pulse with adequate volt-second-product can be produced to reset the power transformer. Such functions can also be fulfilled by placing an inductor in the primary side circuit. In addition to this, the voltage of the main switch can also be clamped if a coupled inductor is used. This leads to the Type 2 converter topology.

The Type 2 converter topology will retain all merits of the Type 1 topology. As it will be shown in Chapter 5, the Type 2 topology is used to implement the proposed DPUPS architecture for multi-point load applications.

However, the analysis made in last chapter does not apply to the Type 2 topology. It is because the primary side inductor is in series with the magnetizing inductor during reset process, not the same as in the Type 1 topology where the secondary side inductor is in parallel with the magnetizing inductor. Therefore, the Type 2 topology has a different mechanism to reset the power transformer, and this requires a new analysis to understand its performance and characteristics.

The structure of this chapter is arranged in the following six sections. The Type 2 converter topology is illustrated in Section 3.2, and the operating principle is described in Section 3.3. The steady state analysis is given in Section 3.4, and the flux excursion of the self-reset power transformer is studied in Section 3.5. Simulation and experimental results are presented in Section 3.6 as proof of concept, followed by the summary of its characteristics in Section 3.7.

3.2 CIRCUIT DESCRIPTION

Fig. 3.1 shows the Type 2 ZVS and self-reset forward converter topology. In this topology, two coupled inductors L_{R1} and L_{R2} replaces the current limiting inductor L_s of the Type 1 topology, and they are inserted in the primary circuit. Also, an additional blocking diode D_R is used. Otherwise, this topology is similar to the Type 1 converter.

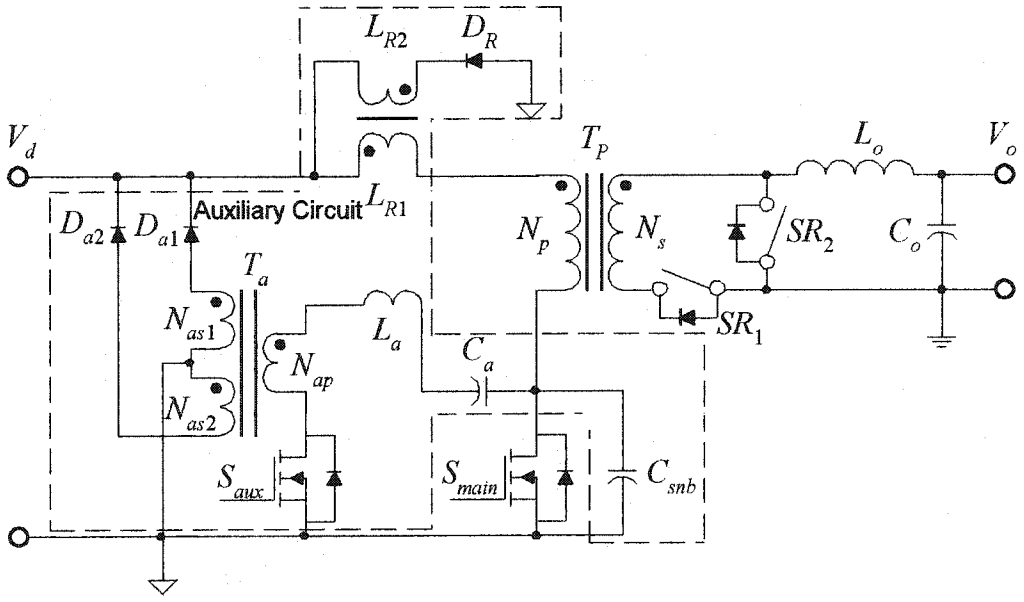


Fig. 3.1 The Type 2 ZVS and self-reset forward converter topology.

3.3 OPERATING PRINCIPLE

The operating principle of the Type 2 converter topology will be described with the assumption that all components are ideal devices, and the timing of controlling the SRs are ideal such that the SRs operate exactly as the ideal diodes.

Fig. 3.2 gives circuit variable designations of the Type 2 converter topology to be referred below. Fig. 3.3 shows the steady state key waveforms of this topology. Each switching cycle can be divided into the following nine (9) intervals.

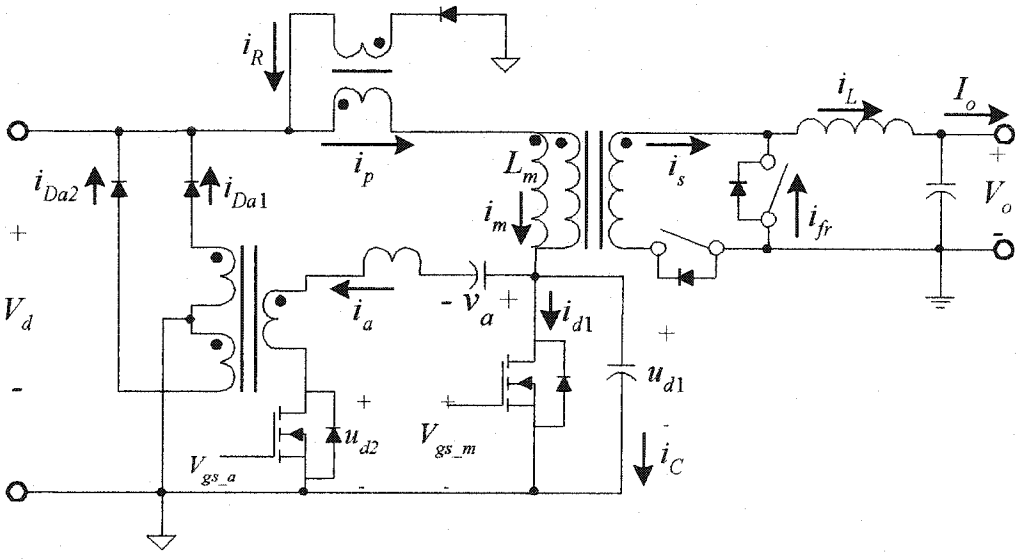


Fig. 3.2 Variable designations of the Type 2 converter topology

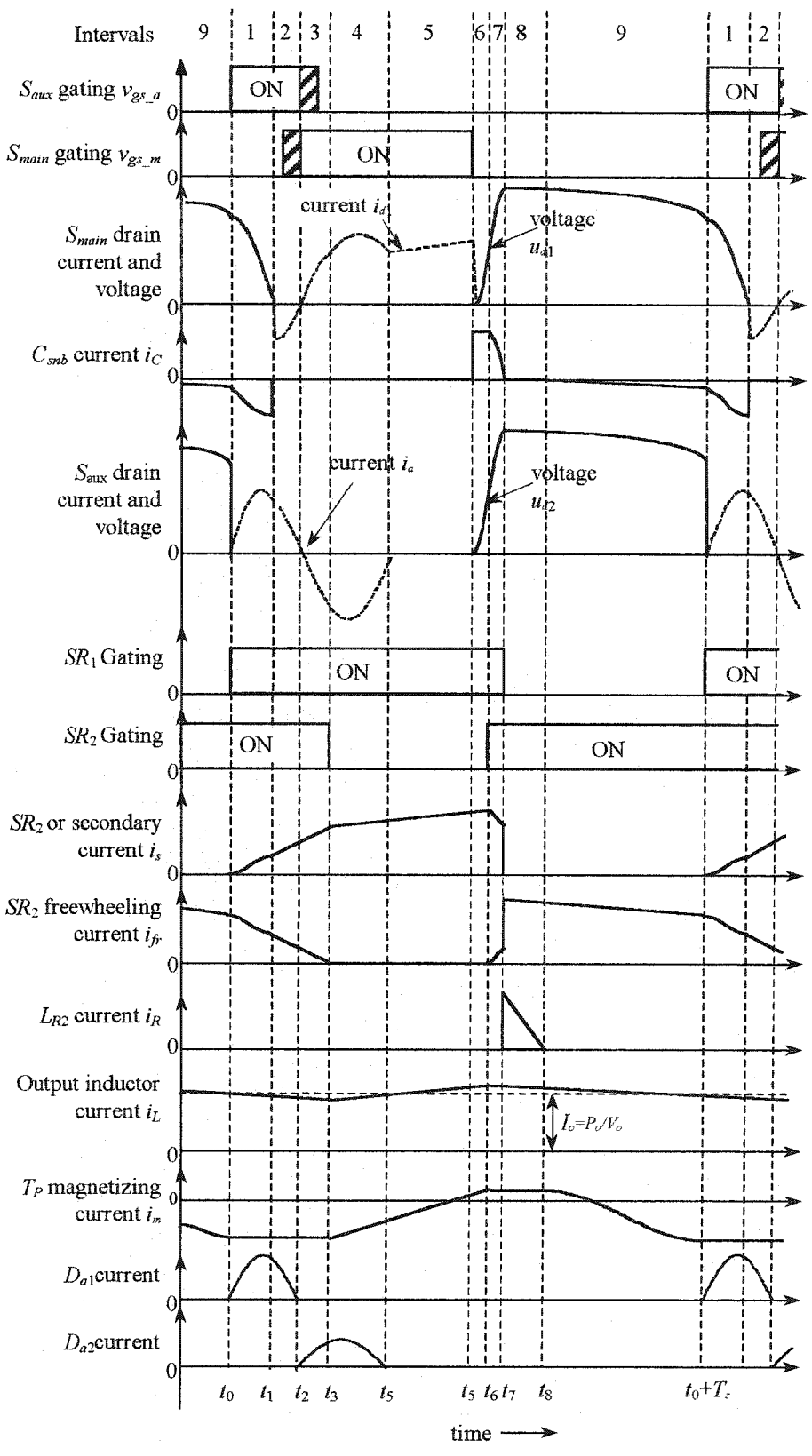


Fig. 3.3 The steady state key waveforms of the Type 2 topology.

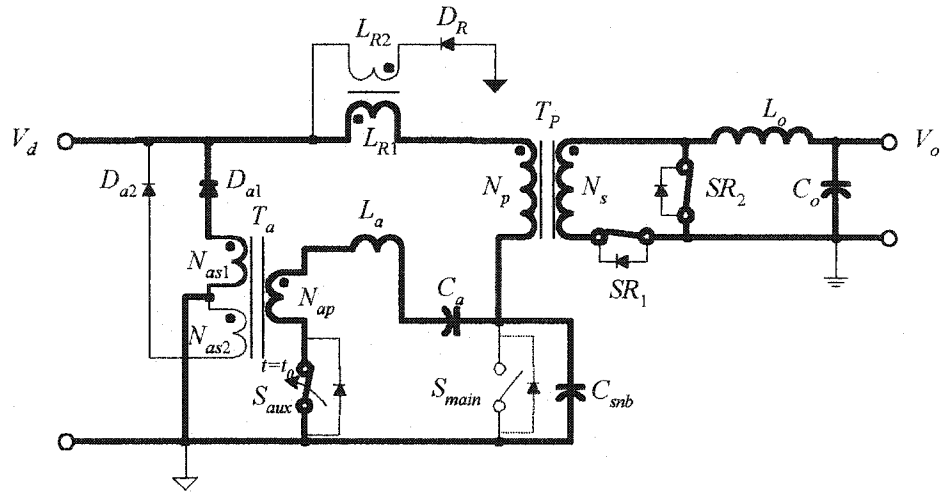


Fig. 3.4 Active current paths in steady state circuit operation during Interval 1.

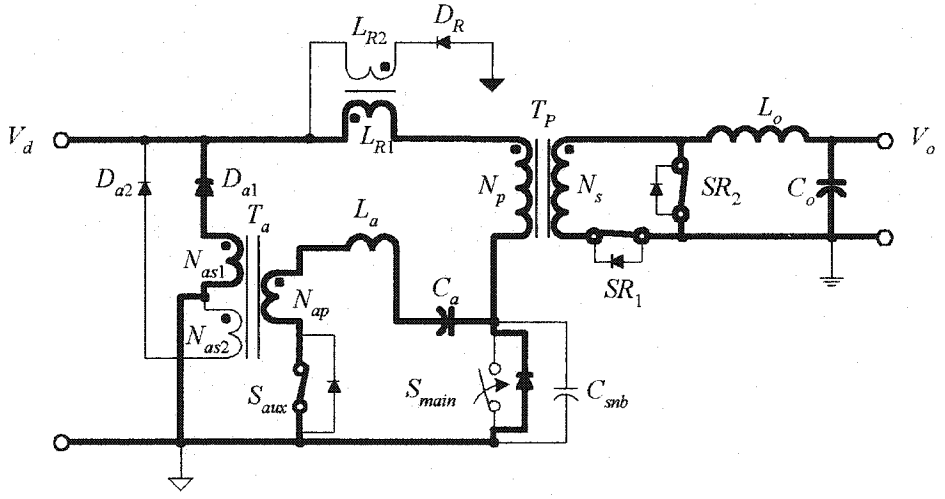


Fig. 3.5 Active current paths in steady state operation during Interval 2.

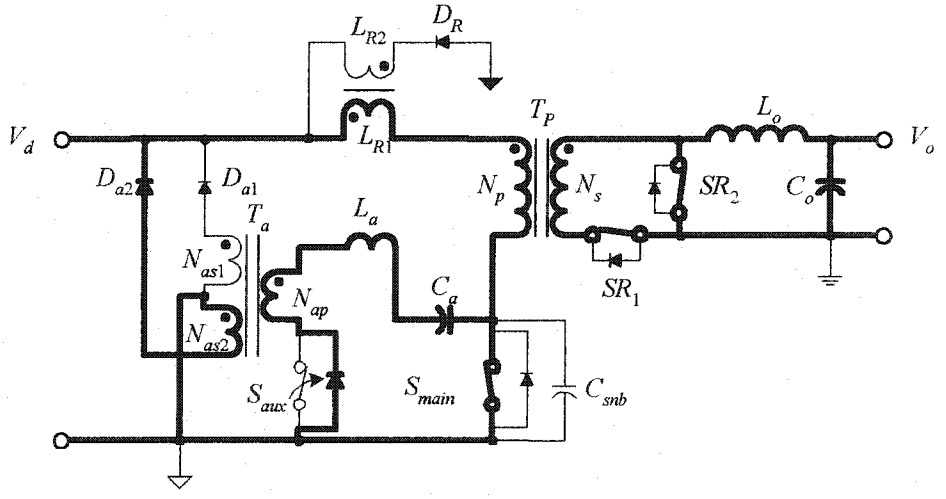


Fig. 3.6 Active current paths in steady state operation during Interval 3.

3.3.1 *Interval 1 ($t_0 \leq t < t_1$): Snubber capacitor discharging and energy recovering*

Fig. 3.4 shows the active current paths in Interval 1. At the beginning of this interval ($t = t_0$), S_{aux} is turned on, and S_{main} snubber capacitor C_{snb} starts to discharge by the resonant current i_a built up along the path C_a, L_a, N_{ap} and S_{aux}. This prepares ZVS condition for S_{main} to turn on in the next interval.

S_{aux} achieves a ZCS turn-on due to the series inductor L_a. i_a temporally stores the discharged energy from C_{snb} into C_a and L_a. Through the coupling of T_a, i_a also induces a current to flow into the input dc line via D_{a1}, thereby to recover some of the discharged energy.

The inductor L_{R1} limits the speed of rise of the primary current i_p, thus to prevent recharging of C_{snb}. Due to the polarity arrangement of the coupled inductors, D_R is reverse-biased and it blocks the L_{R2} branch.

L_{R1} only allows i_p to rise slowly, this also causes the secondary current i_s to rise slowly. Since L_o is fairly large and it can be considered as a dc current source, both SR_1 and SR_2 conduct to continue the almost constant current i_L. The simultaneous conduction of SR_1 and SR_2 in turn causes T_P to see a zero voltage. Therefore, contrary to the Type 1 topology, the magnetizing current of the power transformer in the Type 2 topology does not change in Interval 1.

3.3.2 *Interval 2 ($t_1 \leq t < t_2$): S_{main} drain zero voltage clamping and S_{main} ZVS turn-on*

Fig. 3.5 shows the active current paths in Interval 2. At the beginning of this interval, C_{snb} is completely discharged to pull u_{d1} down to zero volts. i_a diverts to the body diode of S_{main} and thus clamps u_{d1} at zero. This provides the zero voltage condition

for S_{main} to turn on. As in last interval, i_a continues inducing a current to flow into the input dc line via D_{a1}, thereby to recover the energy stored in L_a in last interval. Anytime within this interval can S_{main} be turned on in ZVS to eliminate the turn-on switching losses.

In this interval, L_{R1} sees the constant voltage V_d. Therefore, i_p rises linearly, and so does i_s. However, i_s has yet to reach the magnitude of i_L. Thus, the simultaneous conduction of both SR_1 and SR_2 continues, and T_P still sees zero voltage and the magnetizing current does not change yet.

3.3.3 *Interval 3 ($t_2 \leq t < t_3$): Resonant current reversing and S_{aux} ZVS turn-off*

Fig. 3.6 shows the active current paths in Interval 3. At the beginning of this interval, i_s swings back to zero and it starts to reverse its direction due to the resonance between L_a and C_a. The reversed i_a induces a current to flow into the input dc line via D_{a2} and thus recovers the discharged energy that is temporarily stored in C_a in last two intervals.

At any time in this interval can S_{aux} be turned off in ZVS, because the reversed i_a can divert to S_{aux}'s body-diode and this clamps its drain voltage at zero during the turn-off transient. This eliminates S_{aux} turn-off switching losses.

3.3.4 *Interval 4 ($t_3 \leq t < t_4$):): Power transferring, T_P magnetizing, and discharged energy recovery completing*

Fig. 3.7 shows the active current paths in Interval 4. At the beginning of this interval, i_s reaches the magnitude of i_L. The current through SR_2, namely i_{fr}, becomes zero, and SR_2 is turned off. Thus, SR_1 alone conducts the entire i_L.

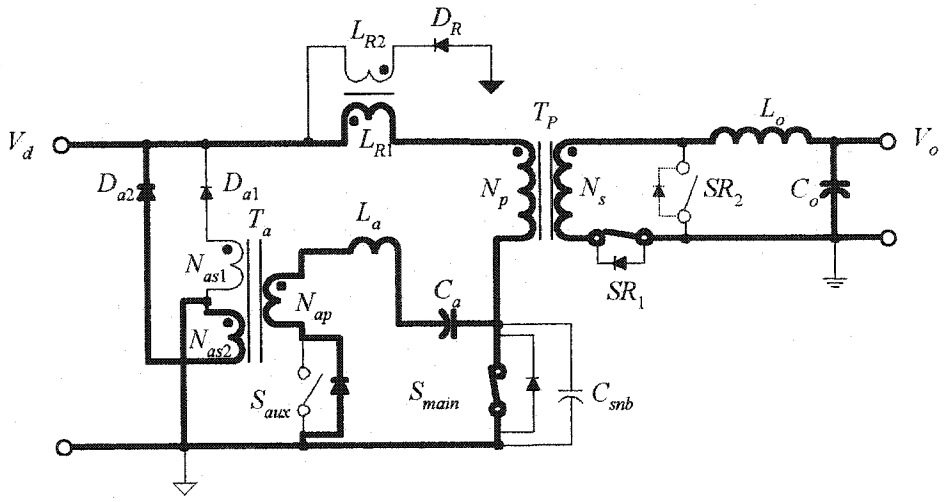


Fig. 3.7 Active current paths in steady state operation during Interval 4.

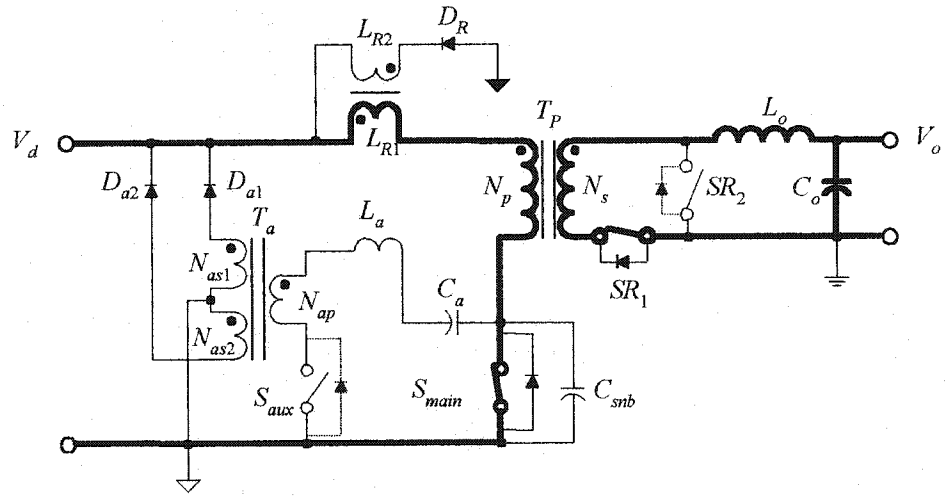


Fig. 3.8 Active current paths in steady state operation during Interval 5.

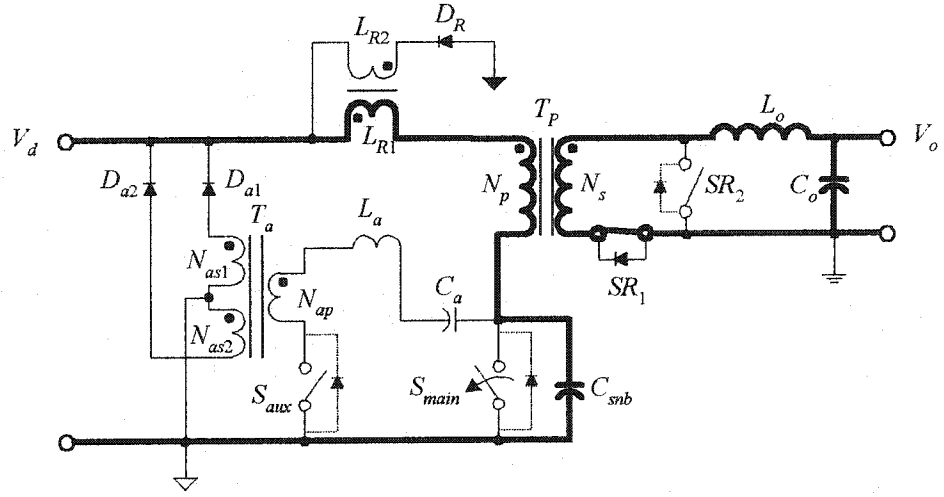


Fig. 3.9 Active current paths in steady state operation during Interval 6.

Since L_o can be regarded as a dc current source, the much smaller L_{R1} becomes negligible in this interval. Therefore, i_p can be considered as constant, the voltage across L_{R1} can be regarded as zero, and T_P starts to see total input voltage. The power is now transferred from the input to the load in the same way as in a conventional forward converter, and T_P magnetizing current starts to rise linearly. The auxiliary circuit continues the process described in Interval 3 until the reversed resonant current swings back to zero again at the end of Interval 4.

3.3.5 Interval 5 ($t_4 \leq t < t_5$): Power transfer and T_P magnetizing continuing

Fig. 3.8 shows the active current paths in Interval 5. At the beginning of this interval, the reversed resonant current in the auxiliary circuit becomes zero again, and the recovery of the discharged energy from C_{snb} is completed. Since S_{aux} is already turned off, the resonance between L_a and C_a is forced to stop. The rest part of the topology behaves the same as in last interval.

3.3.6 Interval 6 ($t_5 \leq t < t_6$): Snubber capacitor charging and S_{main} ZVS turn-off

Fig. 3.9 shows the active current paths in Interval 6. At the beginning of this interval, S_{main} is turned off in order to regulate the output voltage. Due to C_{snb}, S_{main} drain voltage can only rise slowly and this help S_{main} to achieve a soft switching turn-off.

Before S_{main} drain voltage reaches the magntidue of the input voltage V_d, the primary circuit continues to see the output inductor as a dc current source. However, since charging of C_{snb} causes S_{main} drain voltage to increase, T_P starts to see a decreasing voltage that is V_d subtracted by the increasing drain voltage, and this slows down the rise of T_P magnetizing current in this interval.

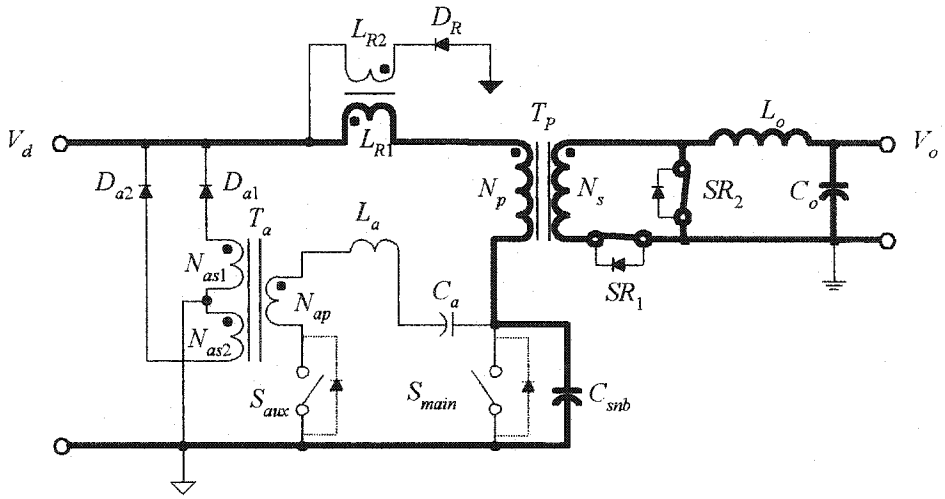


Fig. 3.10 Active current paths in steady state operation during Interval 7.

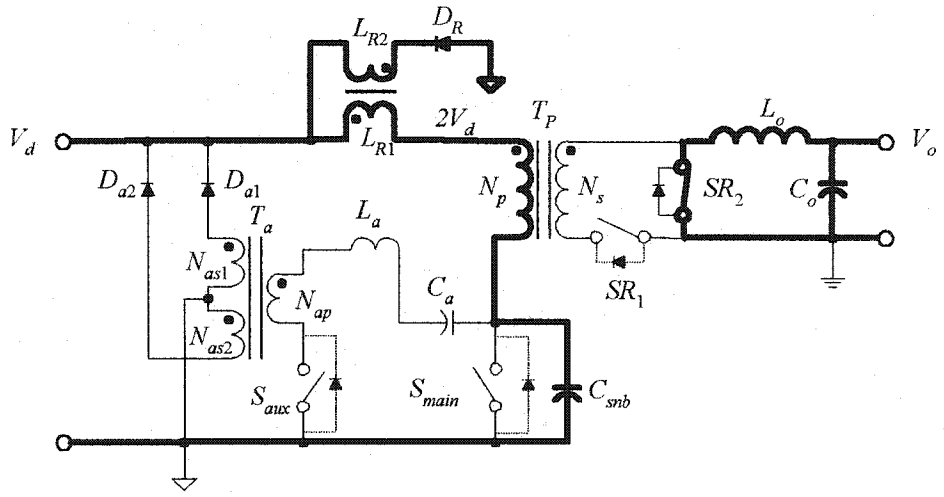


Fig. 3.11 Active current paths in steady state operation during Interval 8.

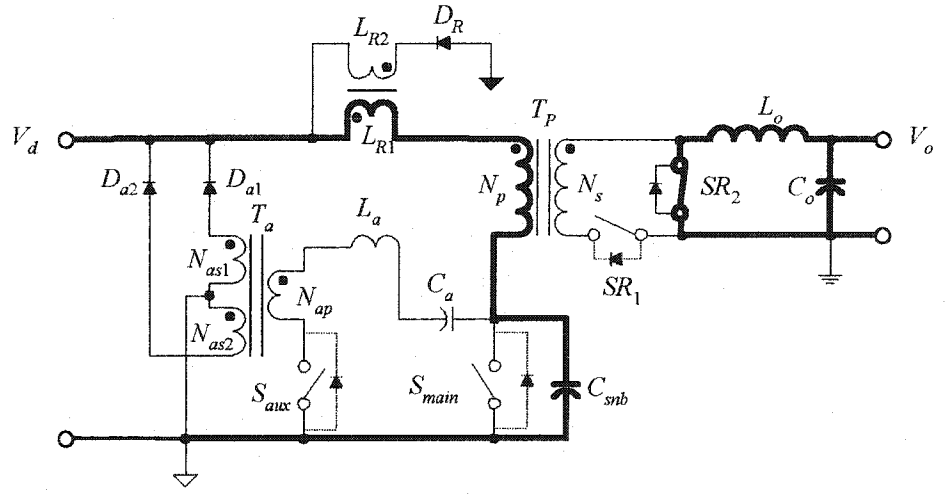


Fig. 3.12 Active current paths in steady state operation during Interval 9.

3.3.7 *Interval 7 ($t_6 \leq t < t_7$): S_{main} drain voltage continuing rising*

Fig. 3.10 shows the active current paths in Interval 7. At the beginning of this interval, C_{snb} is charged to the magnitude of V_d. Continuing charging of C_{snb} causes L_{R1} to see a negative voltage, and in turn, it causes both the primary and secondary currents to decrease. SR_2 is turned on again to conduct the almost constant current through L_o.

The simultaneous conduction of both SR_1 and SR_2 causes T_P to see zero voltage. Again, the magnetizing current stops changing. L_{R1} and C_{snb} start a resonance, and this continues to raise S_{main} drain voltage. This interval is terminated when S_{main} drain voltage reaches the magnitude of $2V_d$ (assuming L_{R1}=L_{R2}).

3.3.8 *Interval 8 ($t_7 \leq t < t_8$): S_{main} drain-voltage clamping and energy recovering*

Fig. 3.11 shows the active current paths in Interval 8. At the beginning of this interval, S_{main} drain voltage reaches the magnitude of $2V_d$. This causes L_{R1} to see a negative voltage, $-V_d$, and induces a voltage across the coupled L_{R2} to forward bias D_R. As soon as D_R is forward biased, the current through L_{R1} is carried over to L_{R2}, and only the magnetizing current now flows through the primary winding.

The current flowing through D_R and L_{R2} release the stored energy in the coupled inductors by sending it back into the input dc bus. The secondary current i_s also stops flowing, and SR_2 conducts the total output inductor current in a freewheeling mode.

Now, the drain voltage of S_{main} is almost clamped at $2V_d$ except for a very small change due to continuous charging of C_{nsb} by the small magnetizing current.

3.3.9 *Interval 9 ($t_8 \leq t < t_0+T_s$): T_P resetting*

Fig. 3.12 shows the active current paths in Interval 9. At the beginning of this

interval, L_{R2} releases all of the stored energy in the coupled inductors. D_R becomes reverse biased again. Therefore, L_{R1} no longer clamps u_{d1} at $2V_d$. C_{snb} and L_m, which are in series with the much smaller L_{R1}, start a new resonance in the primary circuit to reset T_P core. On the secondary side, SR_2 continues the freewheeling mode.

Interval 9 completes at the end of the switching cycle, and the circuit repeats the process from Intervals 1 through 9 and continually delivers the power to the load.

3.3.10 Summary of the Operating Principle

In summary, the steady state operation of the Type 2 topology is similar to the Type 1 topology. Specifically, C_{snb} is discharged first to allow S_{main} to have a ZVS turn-on. Then, the converter transfers the power to the load in the same way as the standard forward converter does. When S_{main} is turned off after completing its duty ratio, the rise of its drain voltage is slowed down by C_{snb}, thus to achieve a soft switching turn-off. In the rest of the cycle, the resonance between L_{R1} and C_{snb}, and afterwards between L_m and C_{snb}, resets the power transformer. Instead of dissipating the energy, the auxiliary circuit recovers the discharged energy from C_{snb}, and L_{R2} recovers the stored energy in L_{R1}. Because of soft switching and energy recovery, the overall efficiency will be improved.

3.4 STEADY STATE ANALYSIS

In order to understand the performance and characteristics of the Type 2 converter topology, the steady state analysis is performed below, and the methodology is the same as mentioned in Section 2.4. The analysis will provide guidelines in generating a design procedure for the DPUPS implementation to be discussed in Chapter 5.

3.4.1 Assumptions for the Steady State Analysis

The following assumptions are made for the steady state analysis. The analysis will start with ideal components. The effects of the non-ideal properties of the components and devices in a practical circuit will be discussed in Section 3.4.3.

(i) The circuit is already in the steady state, and the operating frequency f_{sw}, input voltage V_d, output voltage V_o, and output current I_o, are all constant.

(ii) Switchings of S_{main} and S_{aux} are instant, and the transients are negligible.

(iii) S_{aux} output capacitor is negligible.

(iv) T_P magnetizing inductance L_m is much greater than L_{R1} and L_a.

(v) L_o and C_o are fairly large such that they can be considered as dc current and voltage sources, respectively, and the current through L_o is thus equal to I_o.

(vi) The current limiting inductor L_{R1} is much smaller than L_o.

(vii) T_a has a very small turns-ratio, i.e., $k_a<<1$, such that the primary winding N_{ap} sees a much lower voltage when the input voltage is applied to N_{as1} or N_{as2}.

(viii) T_a magnetizing current is negligible.

(ix) The forward drops of all diodes are negligible.

(x) The SRs are ideal rectifiers.

(xi) The leakage inductances of T_a, T_P and the coupled inductors are negligible.

(xii) Losses on each component and device are negligible.

To facilitate the analysis, the following symbols are assigned:

(i) i_p, the primary current,

(ii) i_a, the current flowing through the resonant inductor L_a,

(iii) u_a, the voltage across the resonant capacitor C_a,

(iv) u_{d1}, S_{main} drain-to-source voltage

(v) i_s, the secondary current , and

(vi) i_m, the magnetizing current of the power transformer T_P.

The following equivalents are worth pointing out for later references:

(i) the currents through L_{R1} and t N_p are the same i_p,

(ii) the currents through C_a, L_a, N_{ap} and S_{aux} are the same i_a,

(iii) the currents through N_s, SR_1 are the same i_s,

(iv) the drain current of S_{main} when it is ON is the sum of i_p and i_a,

(v) the voltage across C_{snb} and S_{main} drain-to-source voltage are the same u_{d1}.

3.4.2 Steady State Analysis

According to the operating principle, and referring to the active current paths shown in Fig. 3.4 through Fig. 3.12, the equivalent circuit for each interval can be obtained as shown in Fig. 3.13. Based on these equivalent circuits and according to Kirchhoff's Laws, one can obtain a group of sets of differential equations, as given in Appendix B that restrain the instantaneous values of key variables in each interval.

3.4.2.1 Interval 1 ($t_0 \leq t < t_1$)

The equivalent circuit in Interval 1 is shown in Fig. 3.13a. The steady state initial values of key variables are as follows:

$$\begin{cases} u_{d1}(t_0) = (1+\delta)V_d \\ u_a(t_0) = V_{a0} \\ i_a(t_0) = 0 \\ i_m(t_0) = I_{m0} \\ i_s(t_0) = 0 \\ i_p(t_0) = i_m(t_0) \end{cases} \tag{3-1}$$

where δ is the factor by which S_{main} drain voltage is greater than V_d at t_0.

From the set of equation given in (B-1), the drain-to-source voltage of S_{main} is found restrained by the following equation, which is the same as (2-2):

$$\alpha\frac{d^4u_{d1}(t)}{dt^4}+\beta\frac{d^2u_{d1}(t)}{dt^2}+u_{d1}(t)=V_d \tag{3-2}$$

However, the coefficients α and β are now defined by the following other than (2-3):

$$\begin{cases} \alpha = L_aC_aL_{R1}C_{snb} \\ \beta = L_{R1}C_{snb}+L_{R1}C_a+L_aC_a \end{cases} \tag{3-3}$$

The solution of (3-2) has the same form as (2-5), namely

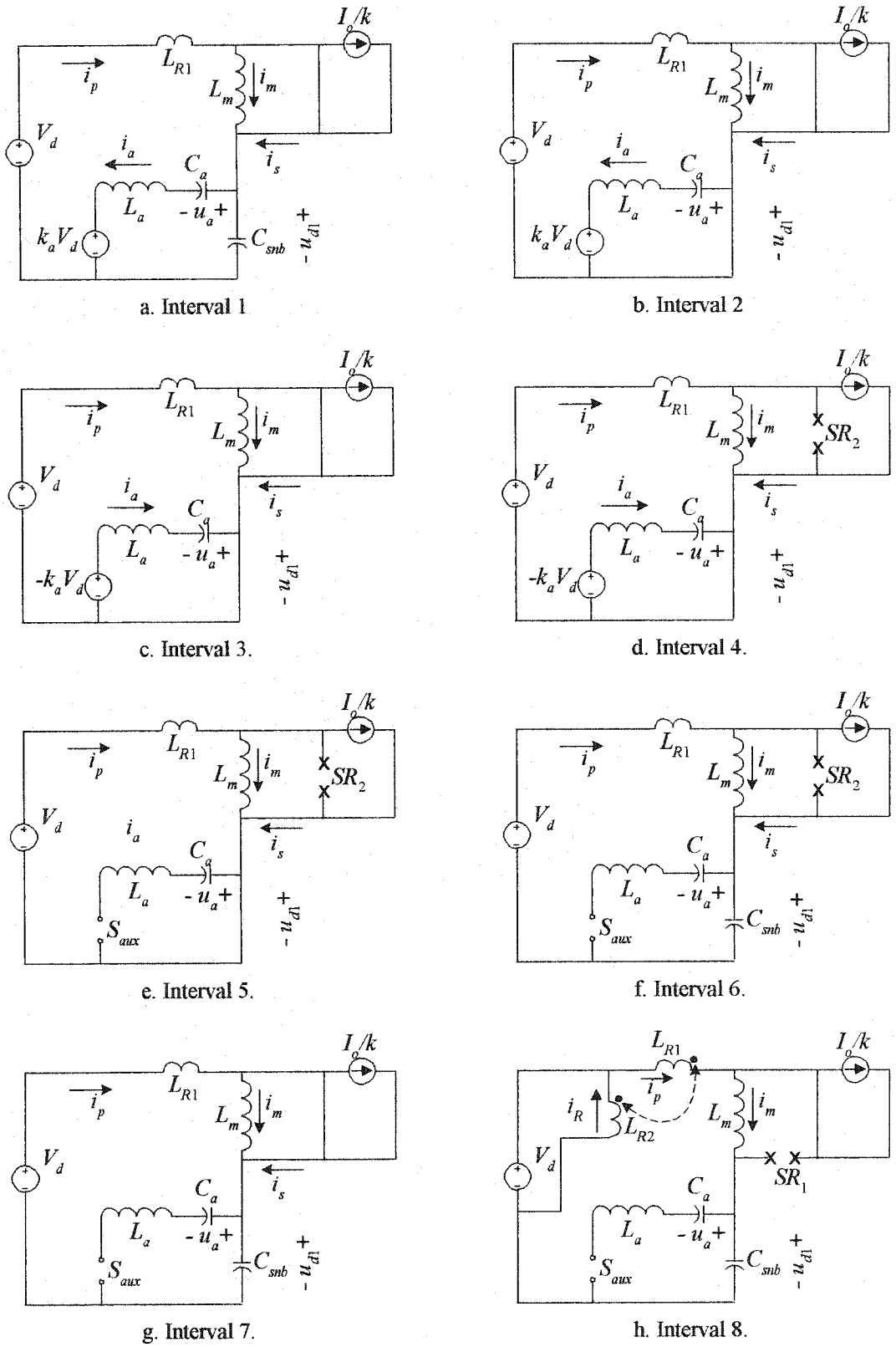
$$u_{d1}(t)=V_d+a_1\cos\omega_1(t-t_0)+a_2\sin\omega_1(t-t_0)+a_3\cos\omega_2(t-t_0)+a_4\sin\omega_2(t-t_0) \tag{3-4}$$

where ω_1 and ω_2 are given in (2-6) and (2-7), respectively, except for the new definitions of α and β, and the four coefficients a_1 through a_4 are given by (2-8) except that the initial conditions (u_{d1} and its three order derivatives at $t = t_0$) are now determined by the operating conditions as well as the four energy storage components C_{snb}, C_a, L_a and L_{R1}. The expressions of the initial conditions are given in the variable "vector" in Appendix F.

Similarly, from (B-1), u_a, namely the voltage across C_a, is governed by (2-10), where the four coefficients b_1 through b_4 are also given by (2-11) except that the initial conditions (V_{a0} and the three order derivatives of u_a at $t = t_0$) are determined by the operating conditions as well as C_{snb}, C_a, L_a and L_{R1}.

The currents i_p, i_s, and i_a are determined respectively by

$$\begin{cases} i_p(t) = I_{m0}+\dfrac{1}{L_{R1}}\displaystyle\int_{t_0}^{t}[V_d-u_{d1}(t)]dt \\ i_s(t) = k[i_p(t)-I_{m0}] \\ i_a(t) = C_a\dfrac{du_a(t)}{dt} \end{cases} \tag{3-5}$$



a. Interval 1

b. Interval 2

c. Interval 3.

d. Interval 4.

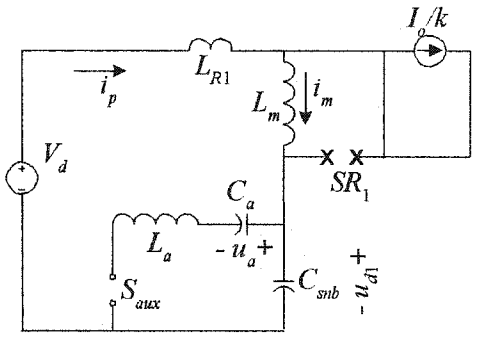
e. Interval 5.

f. Interval 6.

g. Interval 7.

h. Interval 8.

Fig. 3.13 Equivalent circuits seen by the primary in nine different intervals (*To be continued on the next page*).



i. Interval 9.

Fig. 3.13 (*Continued from last page*) Equivalent circuits seen by the primary in nine different intervals

During this interval, the current through SR_2 decreases in the same way as determined by (2-13). The instantaneous recovery of the discharged energy from C_{snb} is governed by (2-14).

Since Interval 1 terminates when u_{d1} reaches zero, namely $u_{d1}(t_1)=0$, the duration of this interval (t_1- t_0) can be determined by substituting the left hand of (3-4) with zero and solving for t_1.

At the end of Interval 1 the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_1) = 0 \\ u_a(t_1) = V_{a1} \\ i_a(t_1) = I_{a1} \\ i_p(t_1) = I_{p1} \\ i_s(t_1) = k(I_{p1} - I_{m0}) \\ i_m(t_1) = I_{m0} + \Delta I_{m1} = I_{m0} \end{cases} \tag{3-6}$$

where ΔI_{m1}, the net change of the magnetizing current in Interval 1, is zero.

3.4.2.2 Interval 2 ($t_1 \leq t < t_2$)

The equivalent circuit in this interval is shown in Fig. 3.13b. The instantaneous values of key variables are restrained by the set of equations given in (B-2). The following are obtained by solving (B-2):

$$\begin{cases} u_a(t) = [V_{a1} + k_a V_d]\cos\omega_3(t-t_1) + I_{a1}\sqrt{\dfrac{L_a}{C_a}}\sin\omega_3(t-t_1) - k_a V_d \\ i_a(t) = -[V_{a1} + k_a V_d]\sqrt{\dfrac{C_a}{L_a}}\sin\omega_3(t-t_1) + I_{a1}\cos\omega_3(t-t_1) \\ i_m(t) = I_{m0} \\ i_p(t) = I_{p1} + \dfrac{V_d}{L_{R1}}(t-t_1) \end{cases} \tag{3-7}$$

where ω_3 is the same as defined in (2-18).

The current through SR_2 is still governed by (2-13), and the instantaneous recovery of the energy discharged from C_{snb} is still governed by (2-14). Since Interval 2 terminates when i_a reaches zero, the duration of this interval is also determined by (2-19).

At the end of Interval 2, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_2) = 0 \\ u_a(t_2) = V_{a2} \\ i_a(t_2) = I_{a2} \\ i_p(t_2) = I_{p2} \\ i_s(t_2) = k(I_{p2} - I_{m0}) \\ i_m(t_2) = i_m(t_1) + \Delta I_{m2} = I_{m0} \end{cases} \tag{3-8}$$

where ΔI_{m2}, the net change of the magnetizing current in Interval 2, is zero.

3.4.2.3 Interval 3 ($t_2 \leq t < t_3$)

The equivalent circuit in this interval is shown in Fig. 3.13c. The instantaneous values of key variables are restrained by the set of equations given in (B-3). The following are obtained by solving (B-3):

$$\begin{cases} u_a(t) = [V_{a2} - k_a V_d]\cos\omega_3(t-t_2) + k_a V_d \\ i_a(t) = -[V_{a2} - k_a V_d]\sqrt{\dfrac{C_a}{L_a}}\sin\omega_3(t-t_2) \\ i_m(t) = I_{m0} \\ i_p(t) = I_{p2} + \dfrac{V_d}{L_{R1}}(t-t_2) \end{cases} \tag{3-9}$$

The current through SR_2 is still governed by (2-13). For the auxiliary circuit, the instantaneous recovery of the energy discharged from C_{snb} is still governed by (2-14).

Since Interval 3 terminates when i_p reaches the magnitude of I_o, from (3-9) the duration of this interval can be found to be:

$$(t_3 - t_2) = \frac{L_{R1}}{V_d}\left[\frac{I_o}{k} - I_{p2} + I_{m0}\right] \tag{3-10}$$

At the end of Interval 3, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_3) = 0 \\ u_a(t_3) = V_{a3} \\ i_a(t_3) = I_{a2} \\ i_p(t_3) = I_{m0} + I_o / k \\ i_s(t_3) = I_o \\ i_m(t_3) = i_m(t_2) + \Delta I_{m3} = I_{m0} \end{cases} \tag{3-11}$$

where ΔI_{m3}, the net change of the magnetizing current in Interval 3, is zero.

3.4.2.4 Interval 4 ($t_3 \leq t < t_4$)

The equivalent circuit in this interval is shown in Fig. 3.13d. The instantaneous values of key variables are restrained by the set of equations given in (B-4). The following are obtained by solving (B-4):

$$\begin{cases} u_a(t) = [V_{a2} - k_a V_d]\cos\omega_3(t - t_2) + k_a V_d \\ i_a(t) = -[V_{a2} - k_a V_d]\sqrt{\dfrac{C_a}{L_a}}\sin\omega_3(t - t_2) \\ i_m(t) = I_{m0} + \dfrac{V_d}{L_m}(t - t_3) \\ i_p(t) = i_m(t) + \dfrac{I_o}{k} \end{cases} \tag{3-12}$$

The current through SR_2 is stopped. For the auxiliary circuit, the instantaneous recovery of the energy discharged from C_{snb} is still governed by (2-13).

Since Interval 4 terminates when i_a becomes zero again, the duration of this interval can be found by solving (3-12) and (3-10). The duration is thus determined by:

$$(t_4 - t_3) = (t_4 - t_2) - (t_3 - t_2) = \frac{\pi}{\omega_3} - \frac{L_{R1}}{V_d}\left(\frac{I_o}{k} - I_{p2} + I_{m0}\right) \tag{3-13}$$

At the end of Interval 4, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_4) = 0 \\ u_a(t_4) = V_{a4} \\ i_a(t_4) = 0 \\ i_p(t_4) = I_o / k + i_m(t_4) \\ i_s(t_4) = I_o \\ i_m(t_4) = i_m(t_3) = I_{m0} + \Delta I_{m4} \end{cases} \tag{3-14}$$

where ΔI_{m4} is the magnetizing current net change in Interval 5, the same as given in (2-30).

3.4.2.5 Interval 5 ($t_4 \leq t < t_5$)

The equivalent circuit in this interval is shown in Fig. 3.13e. The instantaneous values of key variables are restrained by the set of equations given in (B-5).

Since Interval 5 terminates when S_{main} completes its duty ratio in order to regulate the output voltage, by referring to Fig. 3.3 the duration is the same as given by (2-31).

At the end of Interval 5, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_5) = 0 \\ u_a(t_5) = V_{a4} \\ i_a(t_5) = 0 \\ i_p(t_5) = I_o / k + i_m(t_5) \\ i_s(t_5) = I_o \\ i_m(t_5) = i_m(t_4) + \Delta I_{m5} = I_{m0} + \Delta I_{m4} + \Delta I_{m5} \end{cases} \tag{3-15}$$

where ΔI_{m5} is the magnetizing current net change in Interval 5, the same as given in (2-33).

3.4.2.6 Interval 6 ($t_5 \leq t < t_6$)

The equivalent circuit in this interval is shown in Fig. 3.13f. The instantaneous values of key variables are restrained by the set of equations given in (B-6).

Similar to the Type 1 topology, u_{d1} is also governed by (2-34).

Since Interval 6 terminates when u_{d1} reaches the value of V_d, similar to Interval 6 of the Type 1 topology, the duration of this interval is also governed by (2-36).

At the end of Interval 6, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_6) = V_d \\ u_a(t_6) = V_{a4} \\ i_a(t_6) = 0 \\ i_p(t_6) = I_o / k + i_m(t_6) \\ i_s(t_6) = I_o \\ i_m(t_6) = i_m(t_5) + \Delta I_{m6} = I_{m0} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} \end{cases} \tag{3-16}$$

where ΔI_{m6}, the magnetizing current net change in Interval 6, is determined by (2-38).

3.4.2.7 Interval 7 ($t_6 < t < t_7$)

The equivalent circuit in this interval is shown in Fig. 3.13g. The instantaneous values of key variables are restrained by the set of equations given in (B-7). The following are obtained by solving (B-7):

$$\begin{cases} u_{d1}(t) = V_d + [\dfrac{I_o}{k} + i_m(t_6)]\sqrt{\dfrac{L_{R1}}{C_{snb}}} \sin \omega_6 (t - t_6) \\ i_p(t) = [\dfrac{I_o}{k} + i_m(t_6)] \cos \omega_6 (t - t_6) \end{cases} \tag{3-17}$$

where

$$\omega_6 = 1/\sqrt{L_{R1} C_{snb}} \tag{3-18}$$

This interval can end up with two possible cases. The first case is that u_{d1} can reach the magnitude of $(1+\sqrt{L_{R1}/L_{R2}})V_d$. Thus, the duration of this interval can be

obtained from (3-17) as follows:

$$(t_7 - t_6) = \sqrt{L_{R1} C_{snb}} \arcsin\left(\frac{kV_d}{I_o + ki_m(t_6)} \sqrt{\frac{C_{snb}}{L_{R2}}} \right) \tag{3-19}$$

Then, at the end of Interval 7, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_7) = (1 + \sqrt{L_{R1}/L_{R2}})V_d \\ u_a(t_7) = V_{a4} \\ i_a(t_7) = 0 \\ i_p(t_7) = I_{p7} \\ i_s(t_7) = I_{s7} \\ i_m(t_7) = i_m(t_6) + \Delta I_{m7} = I_{m0} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} + \Delta I_{m7} \end{cases} \tag{3-20}$$

where ΔI_{m7}, the net change of the magnetizing current in Interval 7, is zero, and the value of I_{p7} can be obtained by substituting (3-19) into (3-17), which yields:

$$I_{p7} = \sqrt{[\frac{I_o}{k} - i_m(t_6)]^2 - \frac{C_{snb}}{L_{R2}} k^2 V_d^2} \tag{3-21}$$

In the second case that happens most likely at light load, u_{d1} is unable to reach $(1 + \sqrt{L_{R1}/L_{R2}})V_d$, then this interval will terminate when the secondary current decreases to zero. Thus, obtained form (3-17), the duration of this interval is determined by the following, instead:

$$(t_7 - t_6) = \sqrt{L_{R1} C_{snb}} \arccos\left(\frac{ki_m(t_6)}{I_o + ki_m(t_6)} \right) \tag{3-22}$$

and S_{main} drain voltage will reach a peak value given by

$$V_{pk} = V_d + [\frac{I_o}{k} + i_m(t_6)] \sqrt{\frac{L_{R1}}{C_{snb}} \left[1 - \left(\frac{ki_m(t_6)}{I_o + ki_m(t_6)} \right)^2 \right]} \tag{3-23}$$

Note that, in the second case the circuit will skip Interval 8 and directly enters Interval 9. For the continuity in analysis, Interval 8 will be considered existing virtually, its duration

will be zero. Then, at the end of this interval, that is also the end of the virtual Interval 8, the final values of key variables are as follows instead:

$$\begin{cases} u_{d1}(t_7) = u_{d1}(t_8) = V_{pk} \\ u_a(t_7) = u_a(t_8) = V_{a4} \\ i_a(t_7) = i_a(t_8) = 0 \\ i_p(t_7) = i_p(t_8) = i_m(t_6) \\ i_s(t_7) = i_s(t_8) = 0 \\ i_m(t_7) = i_m(t_8) = i_m(t_6) + \Delta I_{m7} = I_{m0} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} + \Delta I_{m7} + \Delta I_{m8} \end{cases} \tag{3-24}$$

In this case, obviously,

$$\Delta I_{m7} = \Delta I_{m8} = 0 \tag{3-25}$$

3.4.2.8 Interval 8 ($t_7 \leq t < t_8$)

When Interval 7 ends up with the second case, this interval will be skipped and the circuit directly enters the next interval.

Otherwise, the equivalent circuit in this interval is shown in Fig. 3.13h. The instantaneous values of key variables are restrained by the set of equations given in (B-8).

Assume I_R to be the initial condition for i_R, namely the current through L_{R2}. According to energy conservation, I_R is determined by the following:

$$I_R = \sqrt{\frac{L_{R1}}{L_{R2}}}[I_{p7} - i_m(t_7)] \tag{3-26}$$

The following solutions are obtained by solving (B-8):

$$\begin{cases} u_{d1}(t) = V_d\left(1 + \sqrt{\frac{L_{R1}}{L_{R2}}}\right) + i_m(t_7)\sqrt{\frac{L_m}{C_{snb}}}\sin\omega_4(t - t_7) \\ i_m(t) = i_m(t_7)\cos\omega_4(t - t_7) \\ i_R(t) = I_R - \frac{V_d}{L_{R2}}(t - t_7) \end{cases} \tag{3-27}$$

where ω_4 is defined by

$$\omega_4 = 1/\sqrt{L_m C_{snb}} \tag{3-28}$$

Because this interval is terminated when the current through L_{R2} exhausts and D_R become reverse biased again, the duration of this interval can be obtained from (3-27) as the following:

$$(t_8 - t_7) = \frac{I_R L_{R2}}{V_d} \tag{3-29}$$

At the end of Interval 8, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_8) = V_{pk} \\ u_a(t_8) = V_{a4} \\ i_a(t_8) = 0 \\ i_p(t_8) = i_m(t_8) \\ i_s(t_8) = 0 \\ i_R(t_8) = 0 \\ i_m(t_8) = i_m(t_7) + \Delta I_{m8} = I_{m0} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6} + \Delta I_{m7} + \Delta I_{m8} \end{cases} \tag{3-30}$$

where ΔI_{m8} is the net change of the magnetizing current in Interval 8, and V_{pk} is the peak value of S_{main} drain voltage, which are given below, respectively:

$$\begin{cases} \Delta I_{m8} = i_m(t_7)\cos\omega_4(t_8 - t_7) \\ V_{pk} = V_d\left(1 + \sqrt{\frac{L_{R1}}{L_{R2}}}\right) + i_m(t_7)\sqrt{\frac{L_m}{C_{snb}}}\sin\omega_4(t_8 - t_7) \end{cases} \tag{3-31}$$

3.4.2.9 Interval 9 ($t_8 \leq t < t_0 + 1/f_{sw}$)

The equivalent circuit in this interval is shown in Fig. 3.13i. The instantaneous values of key variables are restrained by the set of equations given in (B-9). The following are obtained by solving (B-9):

$$\begin{cases} u_{d1}(t) = V_d + (V_{pk} - V_d)\cos\omega_4(t - t_8) + i_m(t_8)\sqrt{\frac{L_m}{C_{snb}}}\sin\omega_4(t - t_8) \\ i_m(t) = -(V_{pk} - V_d)\sqrt{\frac{C_{snb}}{L_m}}\sin\omega_4(t - t_8) + i_m(t_8)\cos\omega_4(t - t_8) \end{cases} \tag{3-32}$$

Interval 9 is the last interval of a complete switching cycle. At the end of this interval, the final values of key variables are as follows:

$$\begin{cases} u_{d1}(t_0+1/f_{sw})=V_{end} \\ u_a(t_0+1/f_{sw})=V_{a4} \\ i_a(t_0+1/f_{sw})=0 \\ i_p(t_0+1/f_{sw})=i_m(1/f_{sw}) \\ i_s(t_0+1/f_{sw})=0 \\ i_m(t_0+1/f_{sw})=I_{m0}+\Delta I_{m1}+\Delta I_{m2}+\Delta I_{m3}+\Delta I_{m4}+\Delta I_{m5}+\Delta I_{m6}+\Delta I_{m7}+\Delta I_{m8}+\Delta I_{m9} \end{cases} \tag{3-33}$$

where ΔI_{m9} is the net change of the magnetizing current in Interval 9, and V_{end} is the final value of S_{main} drain voltage at the end of one switching cycle, which are given below, respectively:

$$\begin{cases} \Delta I_{m9}=-(V_{pk}-V_d)\sqrt{\dfrac{C_{snb}}{L_m}}\sin\omega_4(\dfrac{1}{f_{sw}}+t_0-t_8)-i_m(t_8)[1-\cos\omega_4(\dfrac{1}{f_{sw}}+t_0-t_8)] \\ V_{end}=V_d+(V_{pk}-V_d)\cos\omega_4(\dfrac{1}{f_{sw}}+t_0-t_8)+i_m(t_8)\sqrt{\dfrac{L_m}{C_{snb}}}\sin\omega_4(\dfrac{1}{f_{sw}}+t_0-t_8) \end{cases} \tag{3-34}$$

3.4.2.10 The Sufficient and Necessary Conditions for Steady State Operation

The sufficient and necessary condition for steady state operation is that at the end of Interval 9 all variables returns to the same values respectively as are at the beginning of Interval 1. Comparing (3-1) and (3-33), this sufficient and necessary condition yields:

$$\begin{cases} V_{end}=(1+\delta)V_d \\ V_{a4}=V_{a0} \\ \sum_{j=1}^{9}\Delta I_{mj}=0 \end{cases} \tag{3-35}$$

Equation (3-35) also indicates that the successful reset of the power transformer requires the total change of the magnetizing current is zero in a complete cycle.

3.4.3 *Influences of Non-ideal Properties of Components/Devices on the Analysis*

Similar to the discussion made in Section 2.4.3, the effects of the non-ideal properties of S_{main}, S_{aux}, T_a, the SRs and the diodes can be made negligible by observing the practical rules to select the components, employing strong gate drives and SR self-driven techniques.

In the Type 2 topology, T_p leakage inductance can be treated as part of L_{R1} during Intervals 1, 2, 3, 6 and 7. The effects of the leakage inductances of the coupled inductors can be made very small by using the bifilar winding technique for a close coupling. The leakage of the L_{R1} winding does not affects above analysis except for Interval 8, because L_{R1} just behaves as an inductor in those intervals. In Interval 8, the coupled inductors function as a flyback transformer and the leakage is outside the coupling. However, during Interval 8, the leakage can be considered a part of L_m and is usually negligible as compared to the much greater L_m.

In conclusion, the above analysis is valid and applicable to a practical circuit.

3.5 FLUX EXCURSION

Comparing the steady state analyses of Chapters 2 and 3, the self-reset processes in these two topologies are different. It is because L_s of the Type 1 topology is seen in parallel with L_m while L_{R1} of the Type 2 topology is in series with L_m. This difference will cause the magnetizing and reset process to take a different course. Some examples of the difference can be seen in Intervals 1, 2, 7, etc, in which the net change of magnetizing current is zero in the Type 2 topology but non-zero in the Type 1 topology. Because of these differences, the study of last chapter does not apply to the Type 2 topology, and the self-reset of the power transformer shall be investigated separately.

For convenience in discussion, a 300 kHz, 50 W, and 40-60 Vdc to 5 Vdc prototype converter is used as the example circuit. Table 3.1 lists the principal parameters and operating conditions of this prototype. The power transformer is designed in a conventional way as of the standard forward transformer but the tertiary reset winding is simply eliminated.

3.5.1 Self-Reset Transformer Losses

Like the discussion of Section 2.5.1, similar conclusions can be reached. Namely, the self-reset transformer can achieve self-reset without sacrificing copper and core losses, and the self-reset transformer can follow the conventional design procedure.

3.5.2 Flux Excursions

Seen from the analysis, the boundaries of the flux swing of the self-reset transformer are defined by the following:

$$\begin{cases} B_{\min} = B(I_{m0}) \\ B_{\max} = B(I_{m0} + \Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6}) \end{cases} \tag{3-36}$$

The MathCAD spreadsheet that calculates the flux swing range, namely $B_{\max}$ and $B_{\min}$, is provided in Appendix F.

3.5.2.1 Overlook of the Flux Excursion

Fig. 3.14 shows the flux excursion as a function of V_d, I_o, L_m, L_s, and C_{snb} in the prototype circuit, which are obtained using the MathCAD spreadsheet. Simulation results using Pspice are also given to verify the analysis.

An overall look of these curves indicates that the flux excursion moves toward the first quadrant from the third quadrant of the hysteresis loop when the load decreases. The

reason can be found in (3-23) or (3-31). The peak drain voltage V_{pk} is proportional to the load current, and during the reset process it counteracts the input voltage V_d to drive the magnetizing current i_m to move backward. At light load, V_{pk} is lower, resulting in a weaker driving force to reverse i_m.

It is also seen that at full load, the excursion traverses only the third quadrant of the hysteresis loop. It means a negative magnetizing current. Benefited from this negative current are the slightly reduced copper losses, since the current stress on the primary winding is likely reduced.

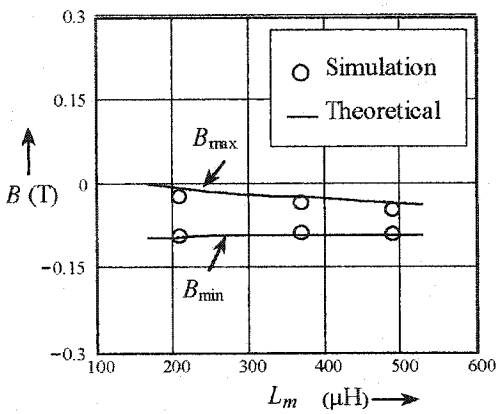
3.5.2.2 Flux Excursion vs. Magnetizing Inductance

In detail, Fig. 3.14a and b show the flux excursion as a function of the magnetizing inductance L_m. It is seen that a larger L_m reduces the excursion range and hence the core losses, and thus an ungapped core seems to serve better in this case due the achievable L_m.

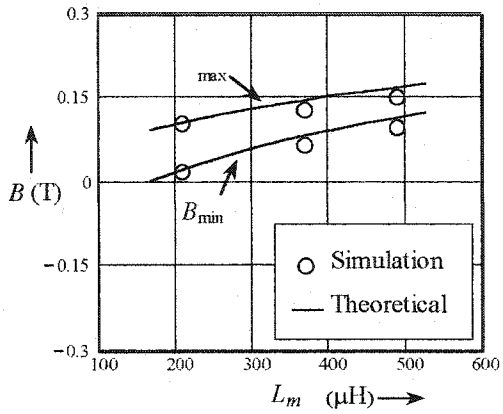
However, at light load, the excursion drifts deeper into the first quadrant of the hysteresis loop as L_m increases. This implies that a very large L_m will increase the conduction losses at light load, and it may drive the transformer into saturation.

3.5.2.3 Flux Excursion vs. Input Voltage

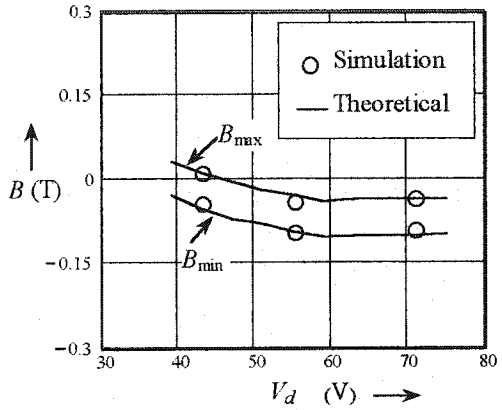
Fig. 3.14c and d show the flux excursion as a function of the input voltage V_d. As V_d varies over a wide range, the excursion remains almost independent of V_d. The reason can also be found in (3-23) or (3-31). The reset driving force is the difference between V_{pk} and V_d, and this voltage difference is almost independent of V_d.



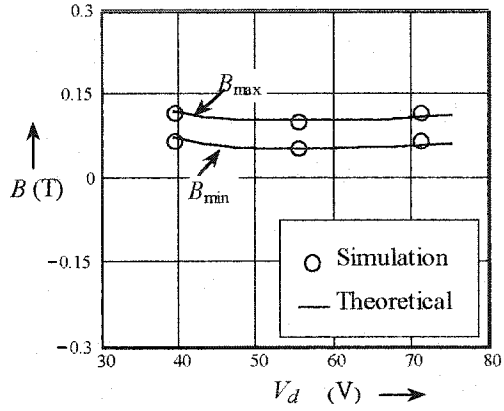
a. Flux density vs. magnetizing inductance at full load. (I_o=10A, L_{R1}=3μH, C_{snb}=6nF, V_d=55V).



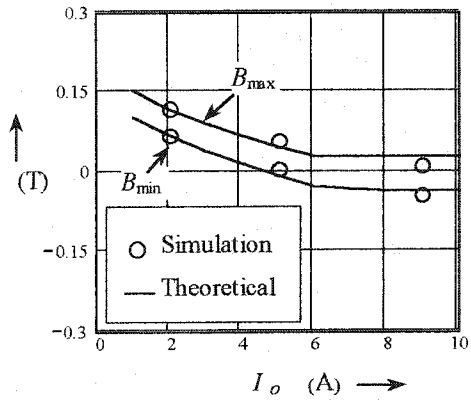
b. Flux density vs. magnetizing inductance at light load. (I_o=1A, L_{R1}=3μH, C_{snb}=6nF, V_d=55V).



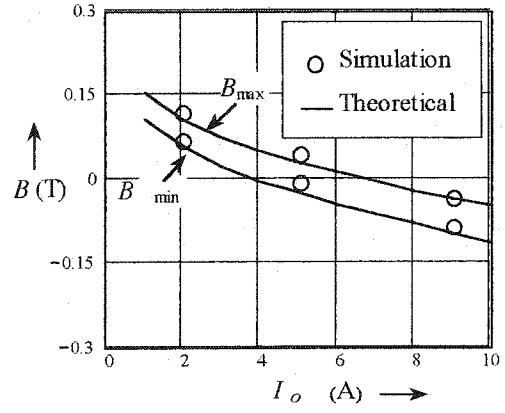
c. Flux density vs. input voltage at full load. (L_m=360μH, L_{R1}=3μH, C_{snb}=6nF, I_o=10A).



d. Flux density vs. input voltage at light load. (L_m=360μH, L_{R1}=3μH, C_{snb}=6nF, I_o=1A).

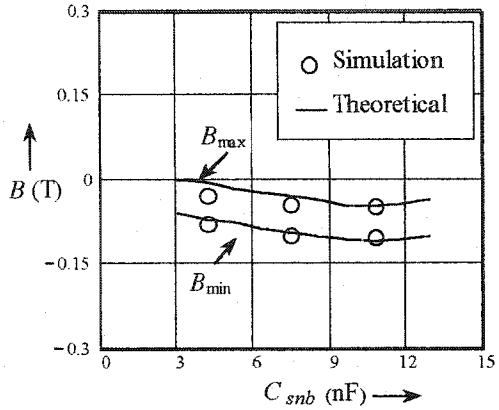


e. Flux density vs. load current at low input voltage. (V_d=40V, L_m=360μH, L_{R1}=3μH, C_{snb}=6nF).

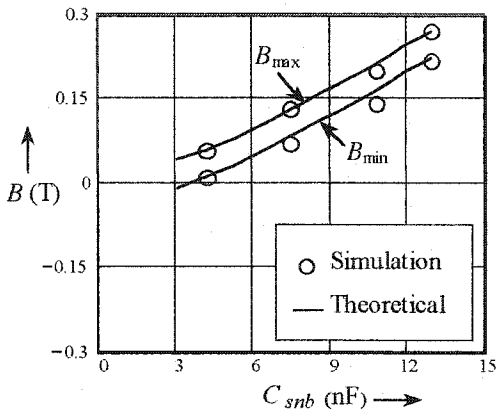


f. Flux density vs. load current at high input voltage. (V_d=70V, L_m=360μH, L_{R1}=3μH, C_{snb}=6nF).

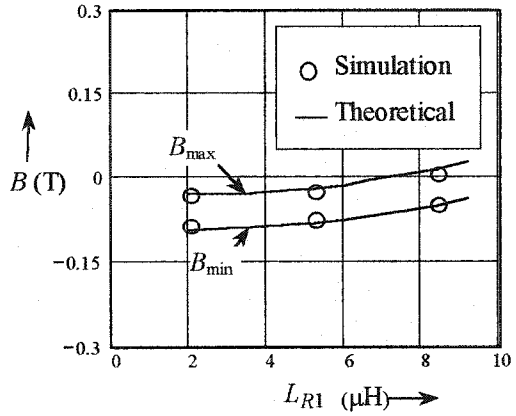
Fig. 3.14 The flux excursion as function of circuit parameters. The flux swings between the two boundaries, B_{max} and B_{min}. The output voltage V_o =5V, switching frequency is 300 kHz. (*To be continued on the next page.*)



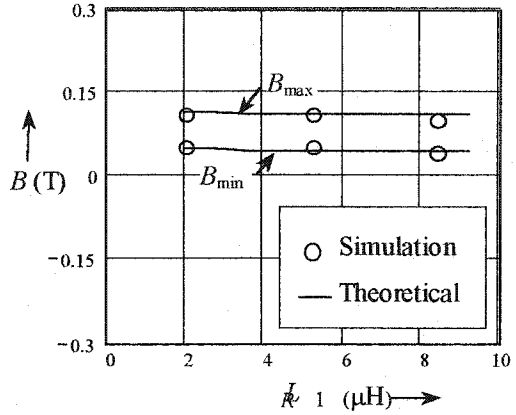
g. Flux density vs. snubber capacitor at full load. (L_m=360μH, L_{R1}=3μH, V_d=55V, I_o=10A).



h. Flux density vs. snubber capacitor at light load. (L_m=360μH, L_{R1}=3μH, V_d=55V, I_o=1A).



i. Flux density vs. current limiting inductor at full load. (L_m=360μH, C_{snb}=6nF, V_d=55V, I_o=10A).



j. Flux density vs. current limiting inductor at light load. (L_m=360μH, C_{snb}=6nF, V_d=55V, I_o=1A).

Fig. 3.14 (*Continued from last page*) The flux excursion as function of circuit parameters. The flux swings between the two boundaries, B_{max} and B_{min}. The output voltage V_o =5V, switching frequency is 300 kHz

As the input voltage decreases further, the flux excursion moves toward the first quadrant of the hysteresis loop. This is mainly because at a lower input voltage, the duty ratio as well as the magnetizing duration is larger, and this leaves shorter time for the magnetizing current to moves back. This indicates that the condition of light load and minimum input voltage is the worst case for the flux excursion of self-reset transformer.

3.5.2.4 Flux Excursion vs. Load Current I_o

Fig. 3.14e and f show the flux excursion as a function of the output current I_o. As the load decreases, the excursion shifts towards the first quadrant. This does not increase the conduction losses at light load, because of the reduced load current. The reasons are similar to those discussed in Section 2.5.2.4.

3.5.2.5 Flux Excursion vs. Snubber Capacitor C_{snb}

Fig. 3.14g and h show the excursion as a function of the snubber capacitor C_{snb}. At full load, the excursion is almost independent of C_{snb} value. But at light load, the larger the snubber, the deeper the excursion moves up into the first quadrant of the hysteresis loop. The reason can still be found (3-23) or (3-31). The peak voltage of the main switch is inverse proportional to C_{snb}. A larger C_{snb} results in a lower V_{pk} and hence a weaker force to drive i_m backward during the reset process. Thus, the value of C_{snb} should be limited again in this sense, although a larger C_{snb} is preferable in removing the turn-off losses of the main switch.

On the other hand, when C_{snb} is lower than 3 nF for the example circuit, the spreadsheet does not find solutions, and the Pspice simulation does not converge. As seen from (3-28) and (3-32), a too small C_{snb} will result in a very fast resonant frequency ω_4 and C_{snb} does not easily hold its voltage through Interval 9. Then the applied negative voltage pulse does not have sufficient volt-second product to reset the core.

In conclusion, neither shall a too small nor a too large C_{snb} be used.

3.5.2.6 Flux Excursion vs. Current Limiting Inductor L_{R1}

Fig. 3.14i and j show the excursion as a function of the current limiting inductance L_{R1}. At light load, the flux excursion is almost independent of L_{R1}. This is

because Interval 7 ends up with the second case and skips Interval 8. Thus, the duration of Interval 9 is almost the same, so is the flux backward swing.

Under full load condition, a larger L_{R1}will move excursion into the first quadrant of the hysteresis loop. This can be explained by (3-29), a larger L_{R1} (equally L_{R2}), results in a longer Interval 8 and that reduces the time for the flux to swing backward.

On the other hand, when L_{R1} is smaller than 2μH for the example circuit, the spreadsheet does not find solutions under full load condition, and the Pspice simulation does not converge. This means that a too small L_{R1} will not reset the transformer successfully.

3.6 EXPERIMENTAL AND SIMULATION RESULTS

Experimental and simulation results are presented in the following to verify the steady state analysis in this chapter. A prototype of 5 V, 50 W circuit operated at 300 kHz has been built, and the circuit parameters are shown in Table 3.1.

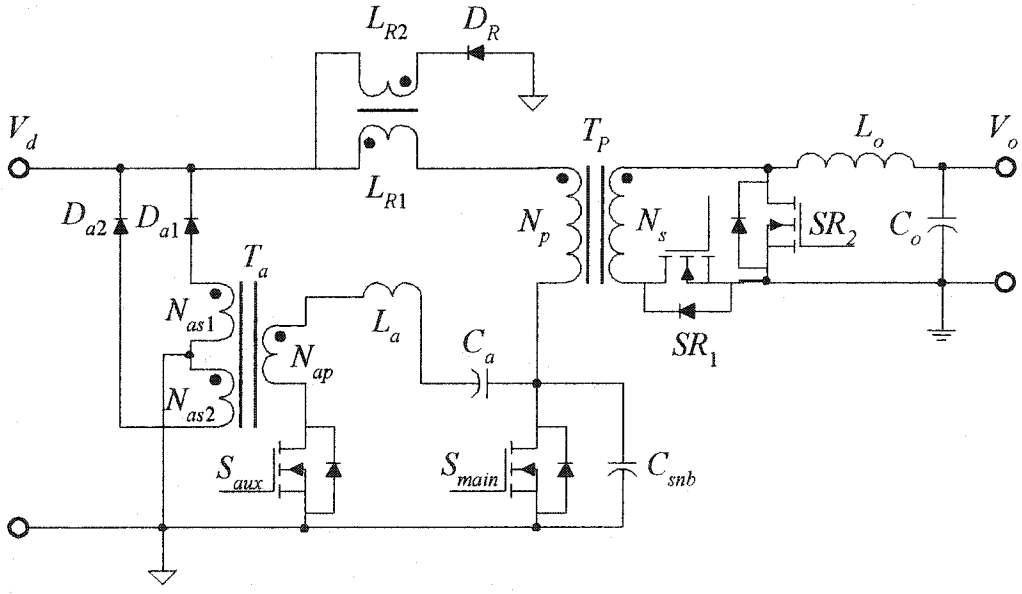


Fig. 3.15 Prototype converter of Type 2 topology using MOSFET SRs.

Table 3.1 Principal Parameters of the Prototype Converter

Components	Values	Selections
$V_{d\,min}$, $V_{d\,max}$	40, 60V	
P_o	50W (V_o=5V,I_o=10A)	
D_{min}/ D_{max}	0.2 / 0.45	
T_P	L_m=350 μH N_p/N_s=12/4	PQ26/20-3F3, custom gap of about 25 μm (1 mil) in each leg.
S_{main}	Rds(on)=0.18 Ω	IRF640, two in parallel
SR_1/SR_2	Rds(on)=0.009 Ω	MTP57N05
C_{snb}	6.6 nF	Ceramic
L_{R1}/ L_{R2}	3 μH/3 μH	RM5/I-3F3-A100
L_a	2 μH	RM4/ILP-3F3, with custom gap
C_a	66 nF	Ceramic
S_{aux}	Rds(on)=0.18 Ω	IRF640
L_o	32 μH	MPP Core
C_o	133 μF	Tantanlum+Electrolyte
D_{a1}, D_{a2}, D_R	V_F=0.8V	MUR860
T_a	L_m=25 μH N_p/N_s=5/30	RM4/I-3F3

Fig. 3.15 shows the prototype converter topology employing the MOSFET SRs. It is built to operate at 300 kHz under an input voltage range of 40 to 60 Vdc, and the output voltage is 5 Vdc with a load of 50 W. The principal circuit parameters are given in Table 3.1. The self-driven SR techniques reported in [110] are also employed in this prototype circuit. The Psipce model of this prototype converter is given in Appendix I.

3.6.1 Simulation Results

Previously, some Pspice simulation results have been presented in Fig. 3.14 for the verification of the theoretically predicted flux excursion. The slight differences between the simulation and the theoretical results arises from the fact that the predicted results are based on ideal circuit parameters, while the Pspice model of the circuits uses

more realistic ones. After all, Fig. 3.14 shows a good agreement between the predictions and simulation, indicating the analysis made in Section 3.4 is valid and applicable to a real circuit. In the following, typical waveforms obtained from simulation are presented as the proof-of-concepts.

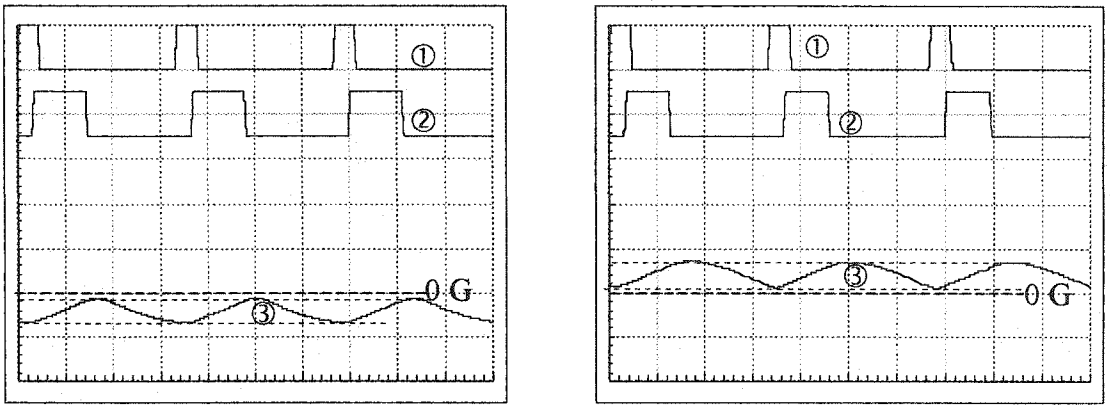
3.6.1.1 Flux Excursion under Different Load Conditions.

Fig. 3.16 shows typical waveforms of the flux density vs. gating signal under different load conditions. First, the flux returns to the same point after each cycle, indicating that T_P achieves self-reset. Second, the flux excursion shifts from the third quadrant into the first quadrant of the hysteresis loop when the load decreases, and thus verifies the analytical results given in Section 3.5.2. The flux excursion range also confirms with the theoretical predictions.

3.6.1.2 Soft Switching

Fig. 3.17 shows typical waveforms of S_{main} ZVS operation under different load conditions. It also shows how S_{main} drain voltage is pulled down to zero by the resonant current in the auxiliary circuit, namely S_{aux} drain current. Under both full and light load conditions, ZVS turn-on and turn-off are always achieved in S_{main}, since the overlap between the drain current and voltage during the switching transient are eliminated.

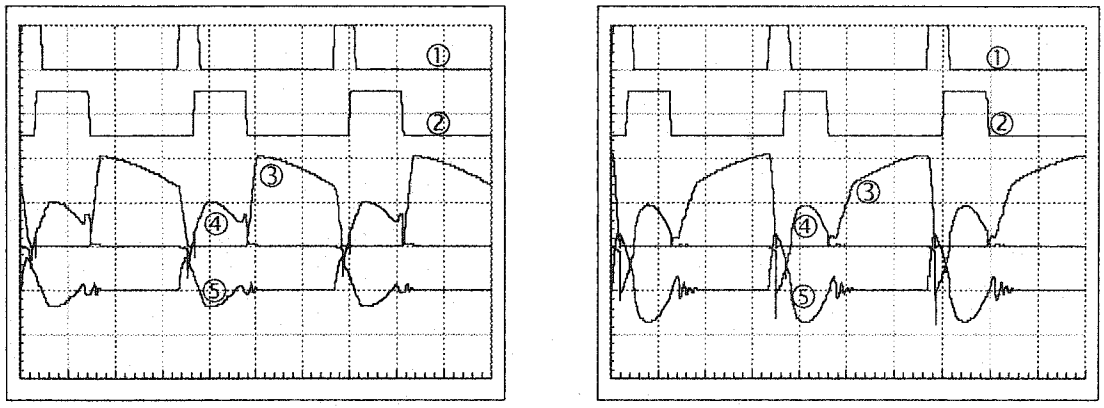
Fig. 3.18 shows typical waveforms of S_{aux} soft switching operation. The auxiliary switch achieves a ZCS turn-on and a ZVS turn-off. The asymmetrical resonant waveform of the auxiliary current is resulted from the different resonant frequencies in its two halves of the resonant cycle, as mentioned in the analysis in Section 2.3.4.



a. Flux excursion under full load (V_d = 50V, I_o=10A)

b. Flux excursion under light load (V_d = 50V, I_o=3A)

Fig. 3.16 Simulation results: flux excursion under different load conditions.
Traces: ①S_{aux} gating (10V/div.), ②S_{main} gating (10V/div.), ③Flux density (1000G/div.). Timing-1μs/div. Operating frequency f_{sw}=300kHz.



a. ZVS under full load (P_o=50W)

b. ZVS under light load (P_o=15W)

Fig. 3.17 Simulation results: S_{main} ZVS operation under different load conditions.
Traces: ①S_{aux} gating (10V/div), ②S_{main} gating (10V/div), ③S_{main} drain voltage (50V/div), ④S_{main} drain current (5A/div), ⑤S_{aux} drain current (5A/div). Timing-1μs/div. Operating frequency f_{sw}=300kHz, V_d=50V.

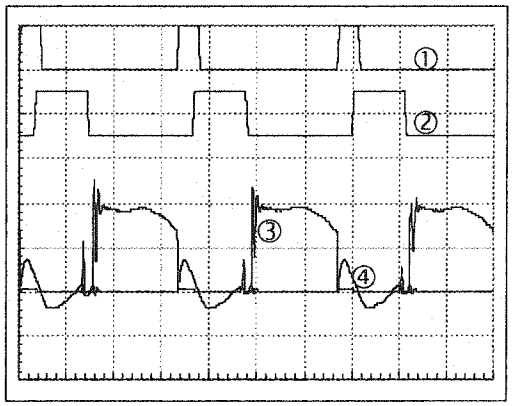
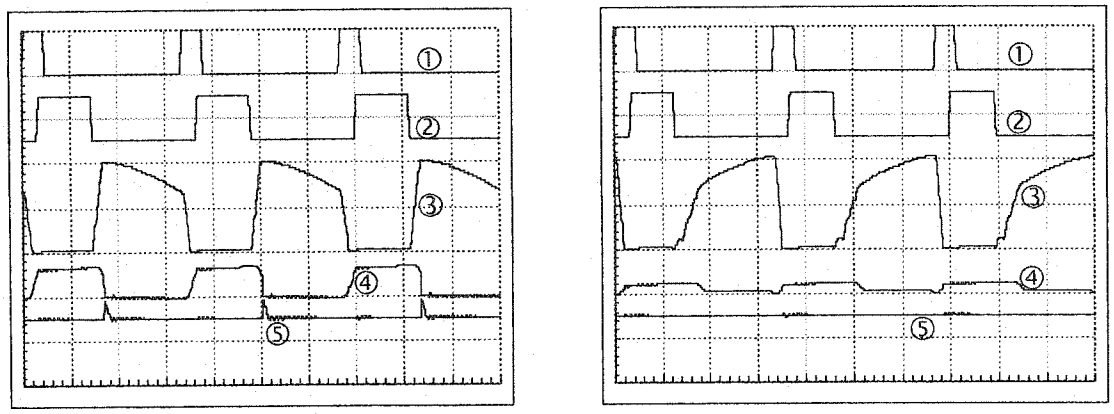


Fig. 3.18 Simulation results: typical waveforms of S_{aux} soft switching.
Traces: ①S_{aux} gating (10V/div), ②S_{main} gating (10V/div), ③ S_{aux} drain voltage (50V/div), ④ S_{aux} drain current (5A/div). Timing-1μs/div. Operating frequency f_{sw}=300kHz, V_d=50V.



a. Current through coupled inductors under full load (V_d = 50V, I_o=10A)

b. Current through coupled inductors under light load (V_d = 50V, I_o=1A)

Fig. 3.19 Simulation results: flux excursion under different load conditions.
Traces: ①S_{aux} gating (10V/div.), ②S_{main} gating (10V/div.), ③ S_{main} drain voltage (50V/div.), ④L_{R1} current (5A/div), ⑤ L_{R2} current (5A/div). Timing-1μs/div. Operating frequency f_{sw}=300kHz.

High frequency ringings are also seen on S_{aux} drain voltage. These ringings are caused by the resonance between L_a and S_{aux}'s inherent drain-to-source capacitor. In a real circuit, the high frequency ringings will be well damped by the significantly increased losses of L_a at such high frequencies. If the ringings are still severe in a real circuit, a small snubber may be required.

3.6.1.3 Behaviors of the Coupled Inductors

Fig. 3.19 shows typical waveforms the currents through the two coupled inductors under different load conditions. The gating signal and S_{main} drain voltage are also presented to provide references. At light load, there is no current flowing through L_{R2}, indicating that Interval 7 ends in the second case and Interval 8 is skipped.

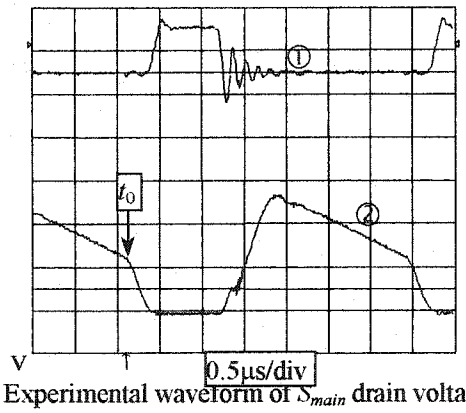
3.6.2 Experimental Results

Experimental results are obtained with the prototype circuit. Typical experimental results are presented in the following to verify the analysis and to provide proof-of-concepts.

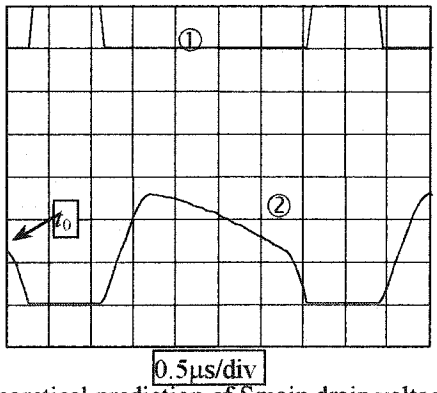
3.6.2.1 Experimental Verification of the Analysis

Fig. 3.20 shows the comparison of S_{main} drain voltage waveform between the experiment and theoretical prediction. Quantitative comparisons are given in Table 3. 2.

The small difference between the experimental results and the theoretical predictions in Table 3. 2 can be explained as follows. In reality, L_{R1} reduces its inductance when a large current flows through, and this saturation tendency is not considered in the analysis due to the complexity that may involve. Thus, the duration of Interval 3 that is a portion of S_{main} duty ratio is actually shorter than the theoretical prediction given by (3-10), and so is the visible duty ratio or the 0V-duration of the drain voltage. The reduced L_{R1} also reduces the peak drain voltage as seen in (3-23).



a. Experimental waveform of S_{main} drain voltage

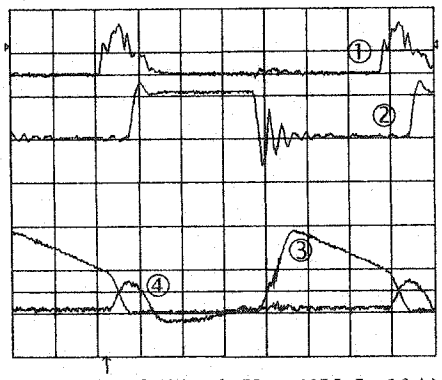


b. Theoretical prediction of Smain drain voltage

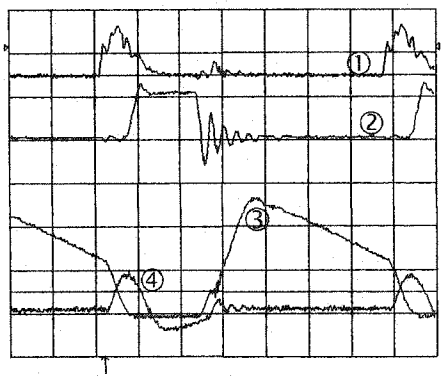
Fig. 3.20 S_{main} drain voltage experimental and theoretical waveforms.
Traces: ①S_{main} gating (10V/div), ② S_{main} drain voltage (50V/div). Operating conditions: f_{sw}=300kHz, V_d=60V, I_o=10A.

Table 3. 2 Comparison of theoretical and experimental drain voltage of S_{main}

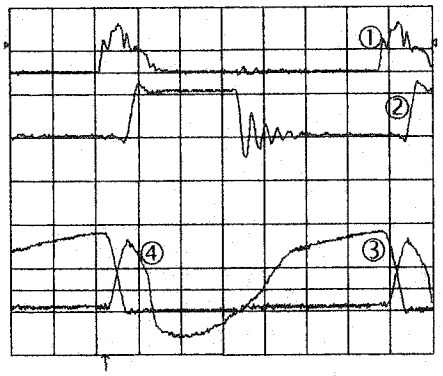
Comparison	S_{main} duty ratio	S_{main} Drain Voltage Pulse				
		0V duration	Value at t_0	Interval 1 Duration	Peak value	Rise time to reach peak
Theoretical	25.8%	0.89μs	61.1V	0.50μs	128.5V	0.57μs
Experimental	24.3%	0.84μs	64.3V	0.54μs	134.7V	0.66μs



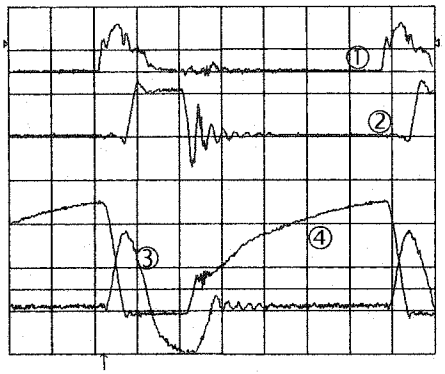
a. Low line full load (V_d = 40V, I_o=10A)



b. High line full load (V_d = 60V, I_o=10A).



c. Low line light load (V_d = 35V, I_o=2A).



d. High line light load (V_d = 60V, I_o=2A).

Fig. 3.21 Typical experimental waveforms of the main switch.
Traces: ①S_{aux} gating (10V/div), ② S_{main} gating (10V/div), ③ S_{main} drain voltage (50V/div), ④ S_{aux} drain current (5A/div.). Timing-1μs/div. Operating frequency f_{sw}=300kHz.

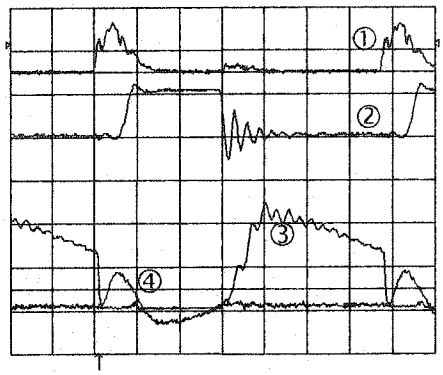


Fig. 3.22 Typical experimental waveforms of the auxiliary switch.
Traces: ①S_{aux} gating (10V/div), ② S_{main} gating (10V/div), ③ S_{aux} drain voltage (20V/div),) ④ S_{aux} drain current (5A/div). Timing-0.5μs/div. f_{sw}=300kHz, I_o=10A.

Above all, the theoretical and experimental wave-shapes shown in Fig. 3.20 and the specific values shown in Table 3. 2 indicate good agreements, and this validates the analysis in this chapter.

3.6.2.2 Proof-of-Concept Key Waveforms

Fig. 3.21 shows typical experimental waveforms of the main switch S_{main} under different operating conditions. The high frequency ringings are caused by noises picked by the scope probes.

S_{main} drain current waveform is not captured due to the reason that a long wire loop needs to be inserted into the circuit to accommodate the current probe and that interferes with the normal operation. However, it still can be concluded from Fig. 3.21 that ZVS is always achieved in S_{main}. Because, at turn-on, S_{main} gating signal arrives after the drain voltage has already dropped to zero and at turn-off it is withdrawn completely before the drain voltage starts to rise.

Fig. 3.22 shows typical experimental waveforms of the auxiliary switch S_{aux}. It is seen that S_{aux} achieves a ZCS turn-on and a ZVS turn-off.

3.6.2.3 Efficiency

Fig. 3.23 shows the experimental results of the overall efficiency under different operating conditions. The Type 2 topology has about 88% maximum efficiency at full load over input voltage range from 40 to 60V. This seemingly low efficiency is mainly because the magnetics used in this prototype are not as efficient as the optimized ones used in the prototype of the type 1 topology.

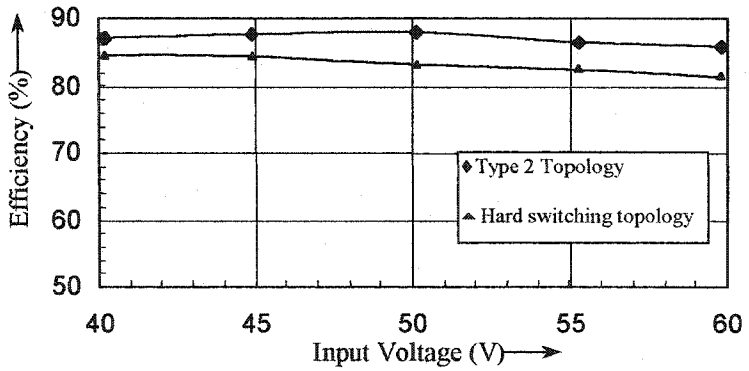
Above 60V the prototype converter loses ZVS due to the saturation of non-optimized L_{R1} at higher input voltages, and below 40V it loses regulation due the

limitation on maximum duty ratio on the prototype. The efficiencies in these abnormal input voltage ranges are irrelevant to the comparison and hence they are not shown in Fig. 3.23.

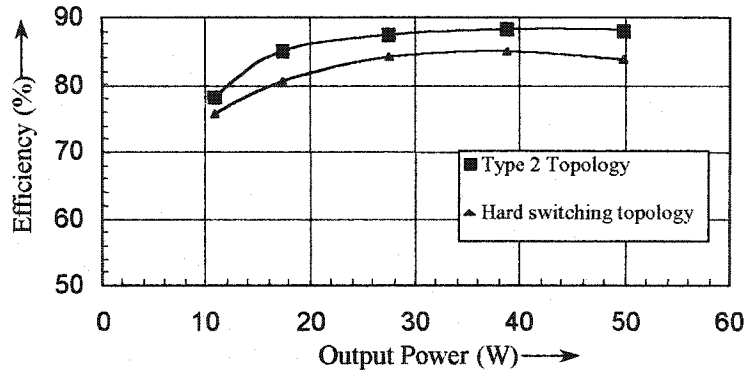
Seen from Fig. 3.23a, as the function of input voltage, the efficiency at full load is the highest at the middle point and it reduces slightly at both ends of the input voltage range. It is because, at a lower input voltage, higher rms current flows for a given output load, thus the conduction losses are higher. At a higher input voltage, although the conduction losses in the power circuit decrease, the auxiliary circuit will be slightly less efficient. It is because the snubber capacitor stores more energy to discharge at a higher input voltage, and a higher auxiliary current is required. This increases the conduction losses in the auxiliary circuit.

At middle point of the input voltage range, neither are the conduction losses in the power circuit nor the losses in the auxiliary circuit excessive, thus the converter has the highest overall efficiency.

As a function of the load, as seen in Fig. 3.23b, the efficiency is almost constant when the load decreases from 100% to about 50% of the full load. Further decreasing the load causes the efficiency to decrease rapidly. This can be explained in the following. Since the circuit achieves soft switching, the major losses are the conduction losses. When the load decrease, the conduction losses also decrease, and this yields an almost constant efficiency. However, when the load decreasing further, the losses in the auxiliary circuit, and the core losses of the power transformer that is almost independent of load conditions, become significant and causes the efficiency to decrease.



a. The efficiency vs. input voltage at full load (50 W).



b. The efficiency vs. output power under fixed input voltage (48 V).

Fig. 3.23 The overall efficiency of the prototype converter of the Type 2 topology.

Above all, the prototype converter of the Type 2 topology shows at least 3% better efficiency than the hard-switching counterpart over the entire input voltage range at full load. This does not sound as great as the 8 % gain of efficiency on the Type 1 topology prototype. The main reason behind this seemingly less efficient performance is the relatively higher losses in the magntices used in the prototype of the Type 2 topology (including both power transformer and coupled inductors) are not optimized. Higher efficiency is expected with optimized magnetics.

3.7 CONCLUSIONS

In this chapter the Type 2 ZVS and self-reset forward converter topology has been presented. The steady state operation of the topology and the flux excursion in the self-reset transformer of the Type 2 topology have been analyzed and verified with experimental and simulation results. The prototype converter shows at least 3% higher efficiency than its hard switching counterpart, and better efficiency is expected by using optimized magnetics and by building the converter on a neat PCB.

The Type 2 topology overcomes the drawbacks of existing soft switching forward topologies and it has the following advantages:

(i) Guaranteed ZVS of the main switch independent of the operating conditions,

(ii) Soft switching auxiliary switches,

(iii) Self resetting of the power transformer without using the tertiary reset winding,

(iv) Simple control and gate-drive design for the auxiliary switching, no need of isolated gate drive or modulating of the auxiliary switching gating pulse width,

(v) Recovery of the energy related to the leakage inductance in the auxiliary circuit.

(vi) Clamped voltage stress on the main switch.

Having these advantages, the Type 2 topology can be used to implement the proposed DPUPS in Chapter 5.

CHAPTER 4

IMPLEMENTATION OF DISTRIBUTED POINT-OF-USE POWER SUPPLY ARCHITECTURE EMPLOYING TYPE 1 CONVERTER

4.1 INTRODUCTION

As discussed previously in Section 1.3, the conventional on-board power distribution architectures are unable to meet the requirements of the low-voltage semiconductor circuit boards. Their major problems include the low efficiency, high count of power components and high costs. Specifically,

(i) The multi-stage power conversion of pre-regulator-post-regulator approaches [24-47] significantly reduces the overall efficiency of the architecture;

(ii) The approach using the cross-regulated multiple-output converters [48-71] is not able to obtain tight regulation of the outputs;

(iii) The architecture using multi PUPS modules [8] not only greatly increases the costs but also occupies too much space of the circuit board.

To solve these problems, Section 1.4 presented the concepts of the DPUPS architectures (shown in Fig. 1.9). In this chapter, the implementation of the architecture shown in Fig. 1.9a will be made with the Type 1 converter topology. Such an architecture will be suitable for a circuit board with its heavy loads collocated.

The DPUPS implementation to be discussed in this chapter is simply to add paralleled secondary circuits to produce multiple outputs, and the primary circuit remains the same as in the Type 1 topology. However, unlike the distinguishable Master/Slave outputs in a conventional multiple output converter, all secondary circuits of the DPUPS

are independently regulated.

Since its primary circuit is the same as that of the Type 1 converter topology, the DPUPS will retain all of Type 1 topology's advantages, including the improved soft switching and self-reset power transformer. Consequently, the steady state analysis of the primary circuit made in Chapter 2 is validly applicable to the DPUPS. Therefore, this chapter only requires focusing on the secondary circuits to understand the DPUPS performance and characteristics.

The additional work to be performed in this chapter includes the following issues: the discussion of the operating principle of multiple output regulation; the small signal analysis of the DPUPS dynamic properties; the development of a generic design procedure of the DPUPS; and the proof-of-concept by simulation and experiments.

The structure of this chapter is arranged in the following six sections. The DPUPS implementation is presented in Section 4.2. Additional steady state analysis for multiple output regulation is performed in Section 4.3. Dynamic analysis of the DPUPS is performed in Section 4.4, in which the small signal model is established. A design procedure for the proposed DPUPS is developed in Section 4.5. Simulation and experimental results are provided in Section 4.6 to verify the analysis and design. In Section 4.7, the characteristics of this DPUPS are summarized.

4.2 THE ARCHITECTURE IMPLEMENTATION AND OPERATING PRINCIPLE

4.2.1 Conceptual Implementation

Fig. 4.1 shows the conceptual implementation of the DPUPS architecture given in Fig. 1.9a for a two-output example. More outputs can be easily added by paralleling additional secondary circuits in the same manner. In contrast to the conventional multiple

output converters, the primary circuit of the proposed DPUPS stays as simple as a single output converter. This reduces the number of the primary components, such as transformers, MOSFETs, soft-switching auxiliary circuits and control circuits. As the number of outputs increases, this component reduction becomes very pronounced on the save of board space occupied by the power supply.

Fig. 4.1 is electrically equivalent to two paralleled converters, with their primary circuits integrated into one. The secondary circuits employs Synchronous Rectifiers (SRs) to improve the efficiency of the rectification stage in addition to achieve the output regulation. A special feature that distinguishes the circuit of Fig. 4.1 from most conventional power converters is that it eliminates the conventional master feedback loop that normally crosses over the primary/secondary isolation boundary. Now, the primary switch is only voltage-feed-forward controlled and the pair SRs of each output circuit are independently controlled. There is no need of opto-coupler and hence much faster dynamic performance can be achieved.

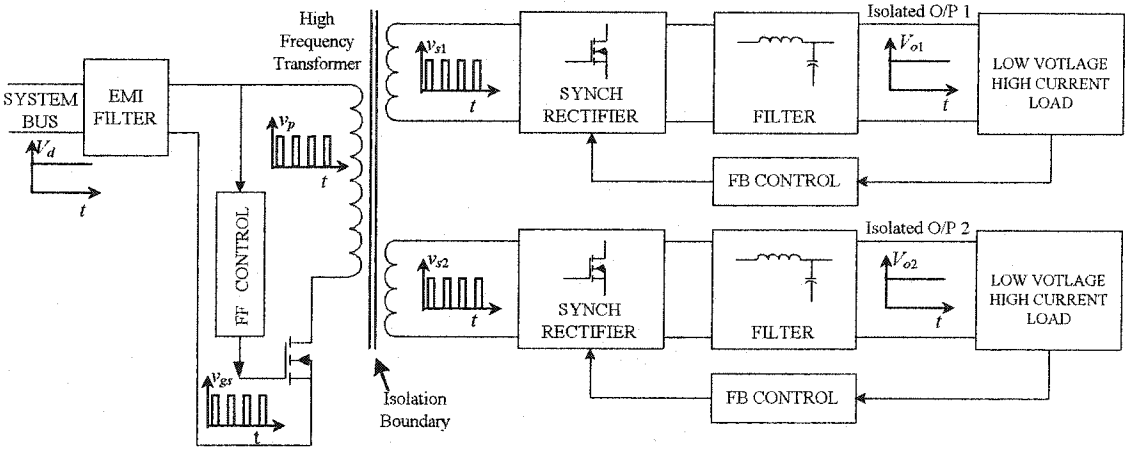


Fig. 4.1 The conceptual block diagram of the first DPUPS Architecture.

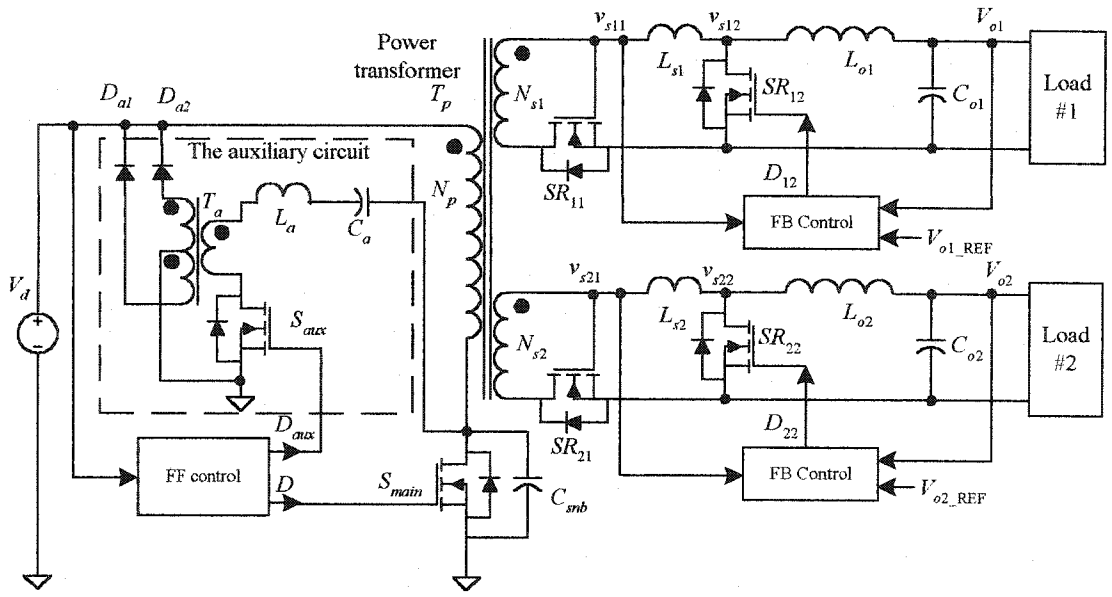


Fig. 4.2 Implementation of the DPUPS of Fig. 4.1 using the Type 1 converter topology.

4.2.2 DPUPS Implementation

Fig. 4.2 shows an implementation of the conceptual architecture of Fig. 4.1 using the Type 1 converter topology. It consists of the following functional blocks: (i) a power transformer, (ii) a main switch MOSFET, (iii) a feed-forward control circuit controlling the main switch S_{main}, (iv) an auxiliary circuit that is described in Chapter 2 to achieve ZVS of the main switch and self-reset of the power transformer, and (v) multiple output sub-circuits on the secondary side of the power transformer.

All the output sub-circuits have identical structures. For the arbitrary j^{th} output circuit, where j =1 or 2 in the case of Fig. 4.2, it consists of (i) an output filter comprised of L_{oj} and C_{oj}, (ii) two SR MOSFET, SR_{j1} and SR_{j2}, (iii) a small current limiting inductor L_{sj} that fulfils the voltage decoupling of the pertinent output circuit from the others, (iv) a dedicated feedback control circuit producing the PWM for SR_{j2}.

4.2.3 Operating principle

The primary circuit operates in almost the same way as described in Chapter 2 to achieve ZVS and self-reset of the power transformer. In addition, the voltage-feed-forward control circuit generates the PWM signal for S_{main} such that unidirectional pulses of constant volt-second-product are produced in the primary circuit. Therefore, the DPUPS can achieve instantaneous output regulation against dc bus voltage variations.

On the secondary side, each pair SRs acts as a chopper to vary the pulse-width of the unidirectional voltage pulses. The pertinent feedback control circuit modulates the pulse-width interval by controlling the simultaneous conduction of the SRs to regulate the output voltage against load variations.

All output circuits are voltage-decoupled from each other by the current-limiting inductors, therefore the cross-regulation between different output is eliminated.

4.2.4 Advantageous Features

Clearly, this proposed DPUPS architecture has the following advantageous features in contrast to the conventional solutions reviewed in Chapter 1:

(i) Single stage power conversion for every output, hence to avoid additional conduction losses in the multi-stage converters.

(ii) Independent feedback control of each output voltage, hence realizing precise regulation of each output voltage.

(iii) Voltage decoupling among the outputs, therefore eliminating cross regulation.

(iv) Isolated multiple outputs, thus to facilitate power distribution.

(v) No need of the feedback loop that crosses over the isolation boundary between the input and output, thereby permitting complete and reliable isolation and also

allowing for high bandwidth design due to the elimination of such slow devices as the opto-coupler in the control loop.

(vi) Voltage feed-forward control of the main switch, thereby enabling instant response in regulation of the output voltages against the input voltage variations.

(vii) Improved soft-switching and power transformer self-reset, which are already discussed in Chapter 2.

(viii) Single power transformer to reduce the number of magnetics.

4.3 STEADY STATE ANALYSIS OF MULTIPLE OUTPUT REGULATION

As mentioned above, this architecture is based on the Type 1 converter topology, and the steady state analysis in Chapter 2 validly applies to the primary circuit of the DPUPS for ZVS and transformer self-reset. This chapter will focus on the secondary circuits to understand the function of multiple output regulation.

The following assumptions are made to perform the analysis for the arbitrary j^{th} output circuit, where j= 1 or 2 in the case of having two outputs.

(i) The input and output dc voltages are at constant values, V_d and V_{oj}, respectively.

(ii) The load draws constant output current, I_{oj}.

(iii) The feed-forward control circuit generates the gating pattern for S_{main} with a duty ratio (pulse-width) of D.

(iv) The switching frequency is f_{sw}.

(v) The output circuit is in CCM.

(vi) The components have linear properties.

(vii) The leakage inductance of T_p is treated as a part of L_{sj}.

(viii) Each pair L_{oj} and C_{oj} makes an ideal output filter.

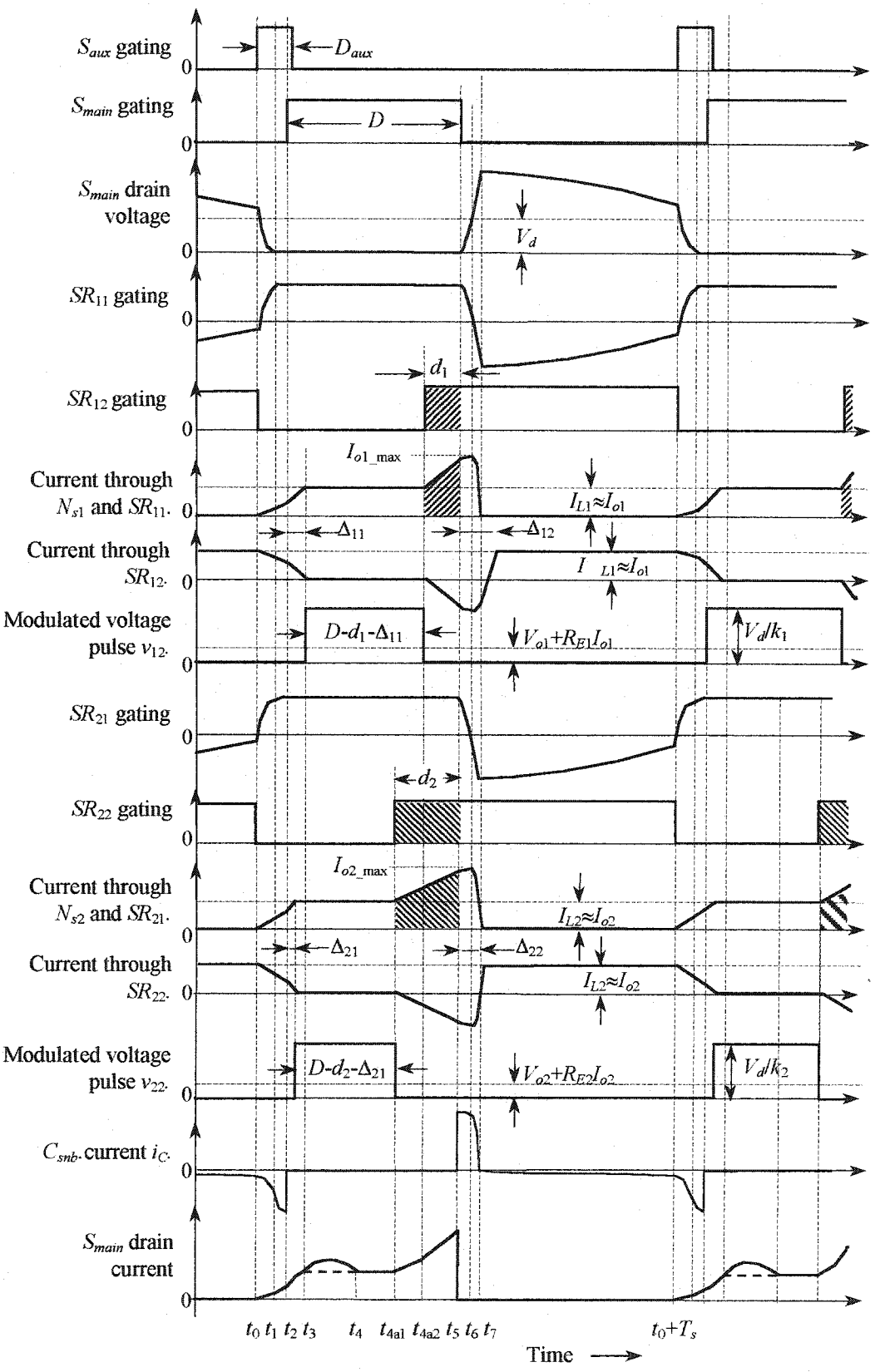
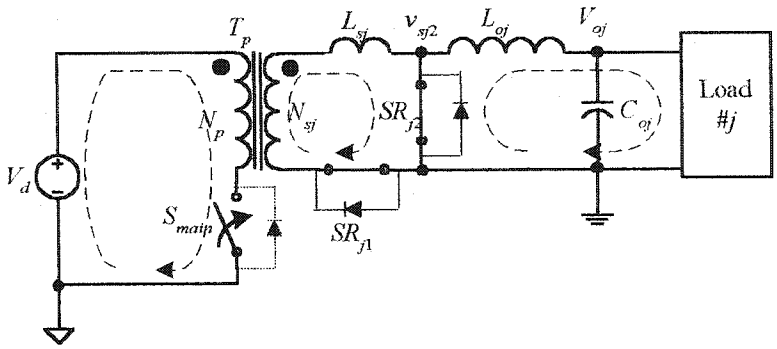
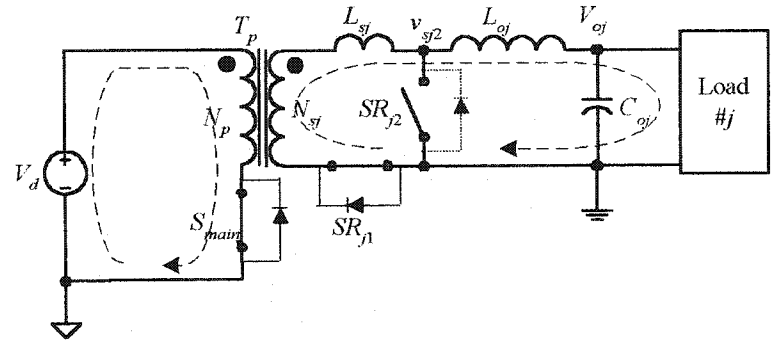


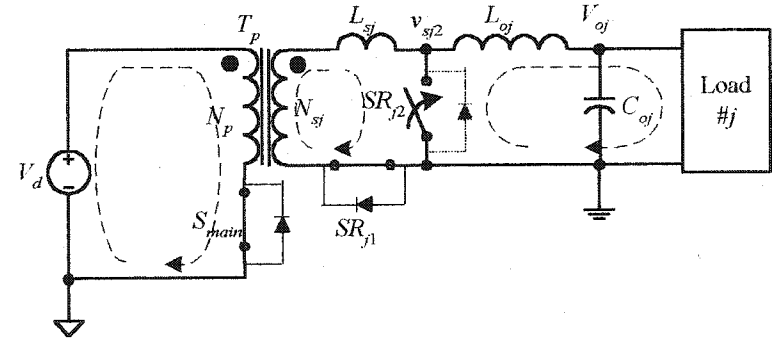
Fig. 4.3 Key waveforms of a two-output DPUPS using Type 1 Topology.



a. Mode 1 (Intervals 1 through 3, total duration approximately Δ_{j1})

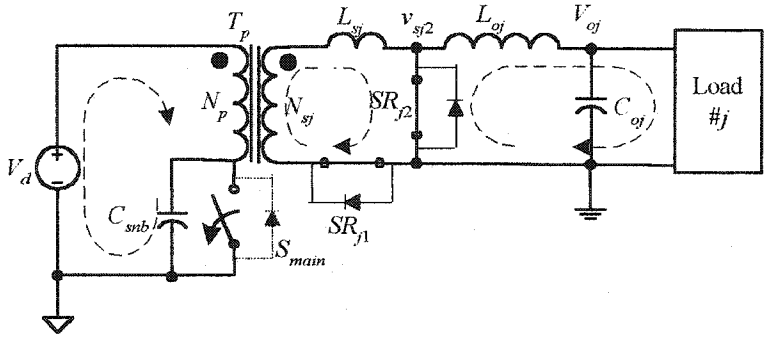


b. Mode 2 (Intervals 4 and 5, total duration D-Δ_{j1}-d_j)

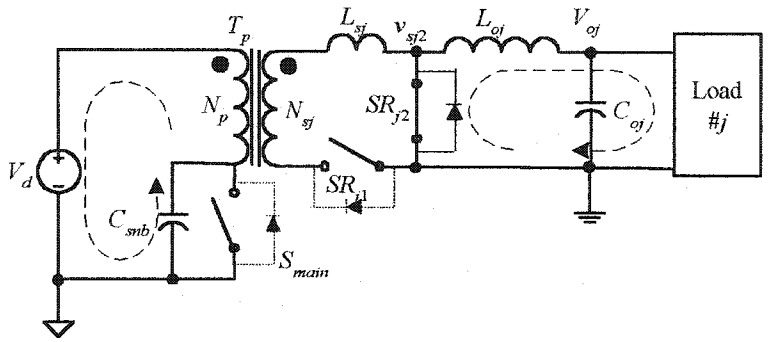


c. Mode 3 (Interval 5a, duration d_j)

Fig. 4.4 Active current paths in the five steady state operation intervals of the arbitrary j^{th} output circuit (*To be continued on the next page*).



d. Mode 4 (Intervals 6 and 7, total duration Δ_{j2})



e. Mode 5 (Interval 8, total duration 1-D-Δ_{j2})

Fig. 4.4 (*Continued from last page*) Active current paths in the five steady state operation intervals of the arbitrary j^{th} output circuit.

Fig. 4.3 shows steady state key waveforms of the two-output circuit of Fig. 4.2. The definition of the intervals are similar to that of Chapter 2. An additional interval 5aj (between t_{4a1} to t_5 for the 1st output, or between t_{4a2} and t_5 for the 2nd output circuit) is introduced, which is the interval during which the pair SRs conduct simultaneously. However, each output circuit only sees five modes, because it cannot distinguish among Intervals 1 through 3, and between Intervals 4 and 5.

Seen from the secondary side, S_{main} and S_{aux} are logically OR-ed to let the primary current flow. For the convenience in performing the analysis on the secondary circuit, S_{aux} is assumed to be a part of S_{main}.

S_{main} has only two states, ON and OFF. The first three modes happen during S_{main}

is ON, and the rest two during S_{main} is OFF. Fig. 4.4 shows the active current paths in the five distinguishable modes for the arbitrary j^{th} output circuit. The duration of each mode is expressed as a fraction of a switching period.

4.3.1 Main Switch ON (Duty-ratio D)

As soon as S_{main} is ON, the front SR, namely SR_{j1}, is also turned on because it is driven by a transformer winding. The circuit goes through the following three Modes.

4.3.1.1 Mode 1 (Intervals 1 through 3: both SR_{j1} and SR_{j2} conduct.)

In this mode, S_{main}, SR_{j1} and SR_{j2} are all ON. Fig. 4.4a shows the active current paths in this mode. Since L_{sj} sees a constant voltage, thus i_{sj} is governed by

$$i_{sj}(t) = \int \frac{V_d - u_{d1}(t)}{k_j L_{sj}} dt \tag{4-1}$$

where u_{d1} is determined by (2-5), or V_d, depending on the actual interval, and k_j is the turn ratio of T_P's primary winding to the j^{th} secondary winding, namely

$$k_j = N_p / N_{sj} \tag{4-2}$$

The duration of this mode, namely (t_3-t_0), can be found in the analysis made in Chapter 2. Since Interval 1 is usually very short, a linear approximation of the total duration of Mode 1, expressed in a fraction of a switching cycle, can be obtained by the following equation,

$$\Delta_{1j} = (t_3 - t_0) f_{sw} \approx \frac{k_j f_{sw} L_{sj}}{V_d} I_{oj} \tag{4-3}$$

4.3.1.2 Mode 2 (Intervals 4 and 4aj: SR_{j1} conducts but SR_{j2} does not.)

In this mode, the total output inductor current now flows through SR_{j1}, and the power is transferred from the input to the load in the same way as in a conventional forward converter. Fig. 4.4b shows the active current paths in this mode

Since L_{oj} is so great that it can be considered as a dc current source, i_s is constant now as governed by

$$i_{sj}(t) = I_{oj} \tag{4-4}$$

Consequently, the voltage v_{sj2} is constant as given by

$$v_{sj2}(t) = \frac{1}{k_j} V_d \tag{4-5}$$

This mode terminates when SR_{j2} is turned ON by the feedback circuit at some time ahead of the end of the ON state of S_{main} in order to regulate the output voltage. The duration of this mode is determine by

$$f_{sw}(t_{4a} - t_3) = D - d_j - \Delta_{1j} \tag{4-6}$$

where d_j is the duration of the next mode expressed in a fraction of a switching cycle.

4.3.1.3 Mode 3 (Interval 5: both SR_{j1} and SR_{j2} conduct.)

In this mode, SR_{j2} is turned ON ahead of the end of D by an interval of duration d_j. Because SR_{j1} is still ON, both SRs now conducts simultaneously, and this creates a short-circuit. Fig. 4.4c shows the active current paths in this mode.

This short-circuit condition chops off the excessive portion the voltage pulses produced by the primary circuit, and by modulating this interval the output voltage is regulated. The effective pulse width, or effective duty-ratio, is determined by the following equation:

$$D_{eff\_j} = D - d_j - \Delta_{1j} \tag{4-7}$$

Thanks to the inductor L_{sj}, this short-circuit condition is voltage-decoupled from T_p. Consequently, the voltages cross all T_p windings do not collapse, and cross-regulation between different outputs is eliminated.

This short-circuit condition also equivalently places L_{sj} across the pertinent T_p secondary winding, and the secondary current rises again as governed by

$$i_{sj}(t) = \frac{V_d}{k_j L_{sj}}(t - t_{4aj}) + I_{oj} \tag{4-8}$$

This mode is terminated by turning off the main switch. The duration of this mode is d_j that will be determined below in Section 4.3.4. At the end of this mode, i_{sj} reaches a peak value given by

$$I_{sj\_pk} = I_{oj} + \frac{V_d}{k_j L_{sj}} \frac{d_j}{f_{sw}} \tag{4-9}$$

4.3.2 Main Switch OFF

4.3.2.1 Mode 4 (Intervals 6 and 7: both SR_{j1} and SR_{j2} conduct.)

In this mode, S_{main} is turned OFF, but both SR_{j1} and SR_{j2} conduct. Fig. 4.4d shows the active current paths in this mode.

The secondary current i_s is determined by (2-37) and (2-39). Because the secondary current decreased to zero at the end of this mode, a linear approximation of i_s can be obtained by the following equation,

$$i_{sj}(t) = I_{sj\_pk} - \frac{V_d}{k_j L_{sj}}(t - \frac{D}{f_{sw}}) \tag{4-10}$$

Thus, the linear approximate duration of this mode can be easily found to be

$$\Delta_{2j} = (t_7 - t_5) f_{sw} \approx \Delta_{1j} + d_j \tag{4-11}$$

4.3.2.2 Mode 5 (Interval 8: SR_{j2} conducts but SR_{j1} does not.)

In this mode, SR_{j2} is freewheeling of the total output inductor current. Fig. 4.4e shows the active current paths in this mode. The duration of this mode is simply (1-D-Δ_{2j}).

4.3.3 Validity of the Linear Approximations

Linear approximation of the duration of Modes 1 and 4 in the above analysis is made to facilitate the small signal analysis in Section 4.4.1 by using averaged state space method. However, it is important to justify these approximations.

4.3.3.1 Validation of the Linear Approximation of Δ_{1j}

Fig. 4.5 shows the comparison between the linear approximation of Δ_{1j} given in (4-3), and the accurate value of Δ_{1j}, namely (t_3-t_0), which is obtained by solving numerically the equations given in Section 2.4.1.

Over the entire load range of the prototype circuit of Section 4.7, the curve of the accurate value is always smaller. It is because the accurate value takes into account the small rise of the secondary current during Interval 1, which was neglected by the approximation. However, (4-3) introduces only a little deviation of less than 1% of a switching cycle. Thus, it can be used as a satisfactory approximation.

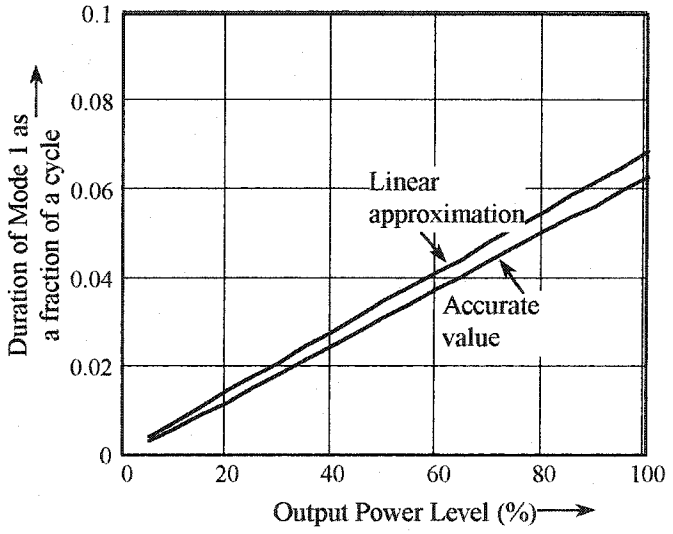


Fig. 4.5 Comparison of the approximation and accurate duration of Mode 1.

4.3.3.2 Validation of the Linear Approximation of Δ_{2j}

Fig. 4.6 shows comparison of the linear approximation of Δ_{2j} given in (4-11), and the accurate value of Δ_{2j} obtained by solving numerically the equations given in Section 2.4.1.

It shows that the linear approximation of Δ_{2j} is very close to its accurate value, although there are little deviations smaller than 1% of a cycle over the entire load range of the prototype circuit of Section 4.7. Therefore, in order to simplify the dynamic analysis made below in Section 4.5, (4-11) can be used as a satisfactory approximation.

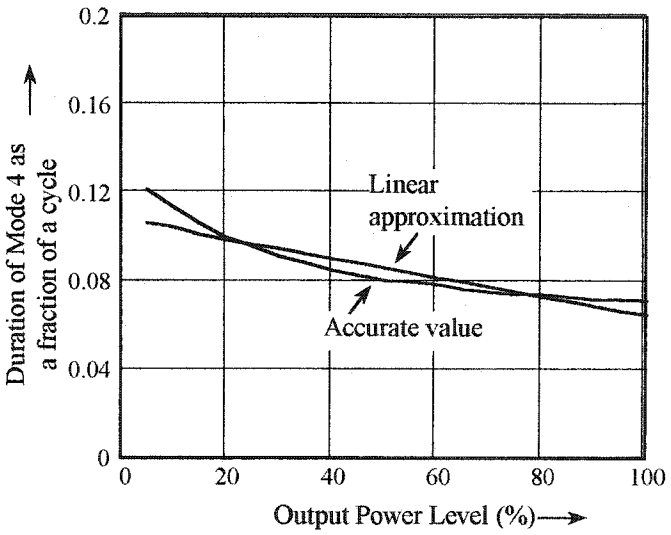


Fig. 4.6 Comparison the approximation and accurate duration of Mode 4.

4.3.4 Steady State Characteristics

4.3.4.1 Modulation of SR Simultaneous Conduction Interval

Each output circuit can be represented by a Thevenin equivalent circuit, and the output voltage as the function of the load current can be expressed as

$$V_{oj} = V_{Thj} - R_{Ej} I_{oj} \tag{4-12}$$

where V_{Thj} and R_{Ej} are the Thevenin equivalent voltage and resistance, respectively, of the the arbitrary j^{th} output circuit. The values of these two equivalents will be found below in Section 4.4.

In fact, V_{Thj} is the average voltage of v_{sj2}. Obviously, it is given by:

$$V_{Thj} = (D - d_j - \Delta_{1j}) \frac{V_d}{k_j} \tag{4-13}$$

Equations (4-12) and (4-13) explain a fundamental concept of the DPUPS to fulfil independent voltage regulation of the multiple outputs against load current. By modulating d_j, or the simultaneous conduction interval of the pair SRs, V_{Thj} can be adjusted to regulate V_{oj}.

Solving from (4-3), (4-12) and (4-13), d_j must satisfy the following equation to obtain the output regulation.

$$d_j = D - \frac{k_j V_{oj}}{V_d} - \frac{k_j (f_{sw} L_{sj} + R_{Ej})}{V_d} I_{oj} \tag{4-14}$$

Specifically, when the load current increases, the internal voltage drops across R_{Ej} and L_{sj} also increase, but this can be compensated by decreasing d_j, which will leads to increase V_{Thj}. And vice versa.

Because d_j represents the duration of the short-circuit condition and a large current may be produced in this condition, it is important to minimize the maximum d_j in

design so as to limit the conduction losses. Ideally, if S_{main} duty ratio is programmed to satisfy the following equation, d_j shall be set to zero under full load condition.

$$D = k_j \frac{V_{oj} + (R_{Ej} + f_{sw}L_{sj})I_{oj\_max}}{V_d} \tag{4-15}$$

where I_{oj_max} is the maximum load current of the j^{th} output. Thus, under reduced load conditions, (4-14) turns out to be

$$d_j = \frac{k_j(f_{sw}L_{sj} + R_{Ej})}{V_d}(I_{oj\_max} - I_{oj}) \tag{4-16}$$

In a practical design, (4-15) can not be exactly satisfied, because k_j is the a ratio of two integer numbers, and the values of L_{sj} and R_{Ej} can not be known with 100% accuracy. To count for this, a practical S_{main} duty ratio usually has a reasonable margin, namely,

$$\begin{aligned} D &\geq \max_{j=1,2}(k_j \frac{V_{oj} + (R_{Ej} + f_{sw}L_{sj})I_{oj\_max}}{V_d}) \\ &= k_j \frac{V_{oj} + (R_{Ej} + f_{sw}L_{sj})I_{oj\_max}}{V_d} + d_{mj} \end{aligned} \tag{4-17}$$

where d_{mj} is S_{main} duty ratio margin seen by the arbitrary j^{th} output circuit. Then, substituting (4-18) into (4-14), it yields:

$$d_j = d_{mj} + \frac{k_j(f_{sw}L_{sj} + R_{Ej})}{V_d}(I_{oj\_max} - I_{oj}) \tag{4-18}$$

Equation (4-18) determines d_j in a practical design. It increases with R_{Ej}. Because R_{Ej} is mainly determined by the Rds(ON) of the SR MOSFETs, the SRs requires low Rds(ON) MOSFETs to minimize d_j.

Fig. 4.7 shows d_j as a function of the circuit parameters of the prototype circuit. The duty ratio margin d_{mj} is assumed zero for the 2V output circuit, and 0.02 for the 5V output circuit. The maximum d_j, which occurs at no load, can be kept smaller than 5% of a switching cycle, when R_{Ej} can be lower than 5mΩ.

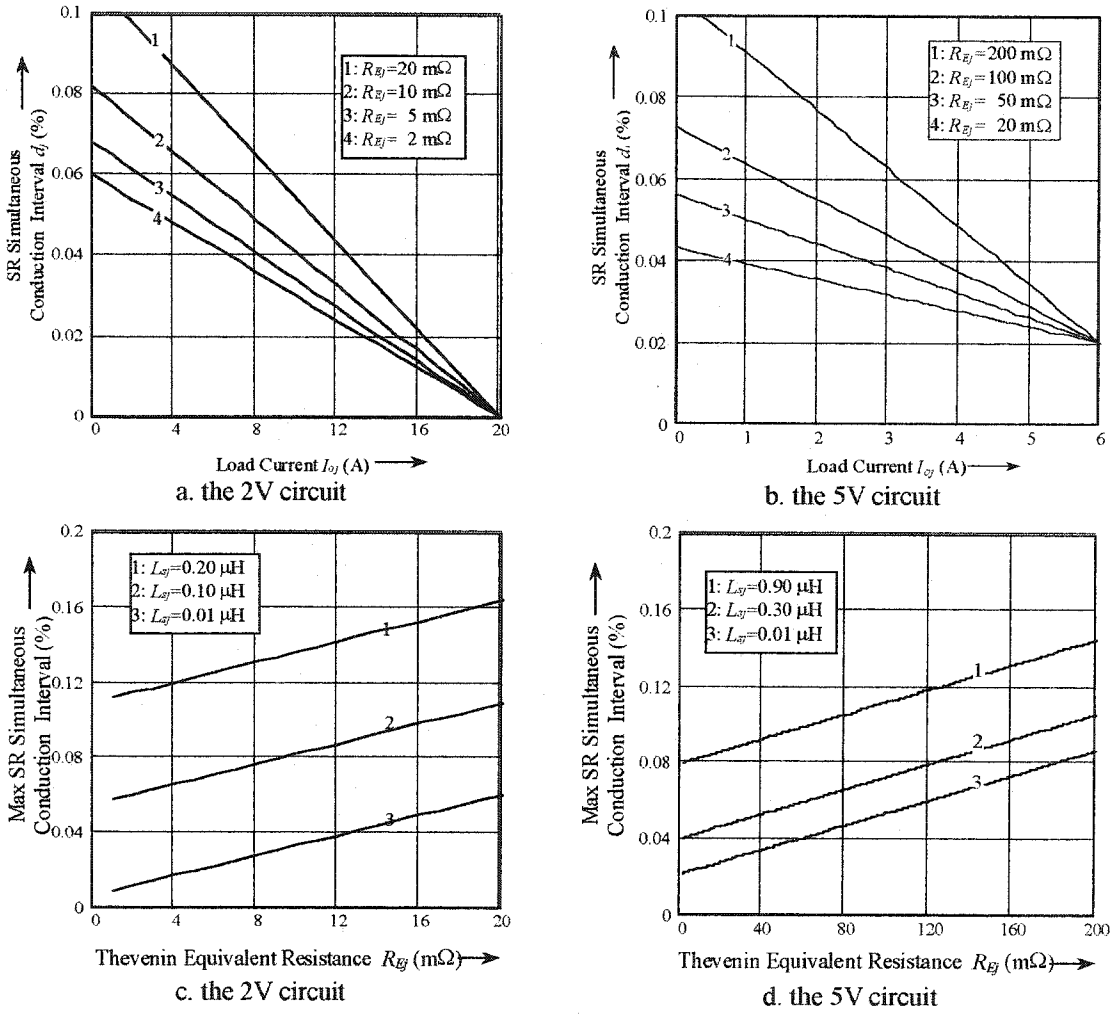
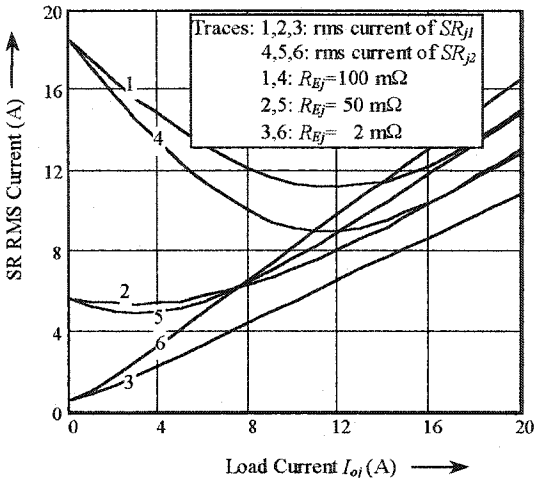
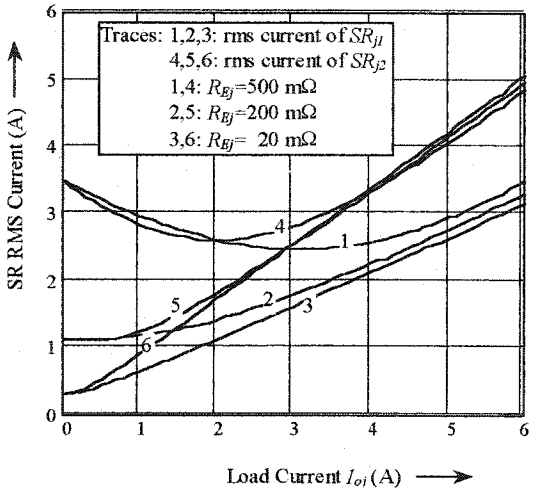


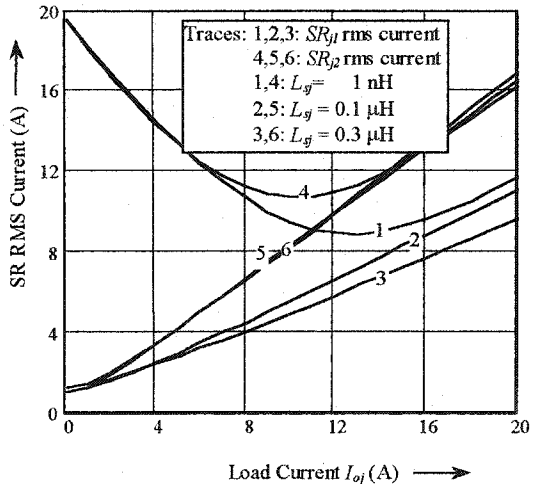
Fig. 4.7 The maximum simultaneous conduction interval d_j of the pair SRs in the 2 V 24W output circuit vs. the Thevenin equivalent source resistance R_{Ej} and the decoupling inductor L_{sj}. I_{oj}=0A, V_d=55V, f_{sw}=200kHz.



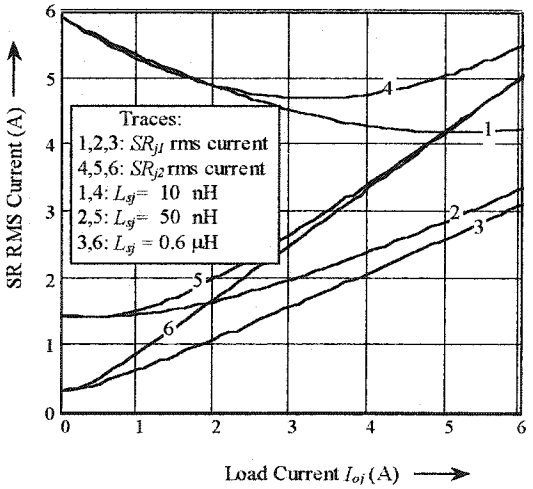
a. SR rms current of the 2V output circuit. (L_{sj}=0.1μH)



b. SR rms current of the 5V output circuit. (L_{sj}=0.3μH)



c. SR rms current of the 2V output circuit. (R_{Ej}= 10mΩ)



d. SR rms current of the 5V output circuit. (R_{Ej}= 50mΩ)

Fig. 4.8 The rms current through the pair SRs as a function of R_{Ej}, L_{sj} and I_{oj}. V_d=55V, f_{sw}=200kHz.

4.3.4.2 RMS Current through the SRs

Seen from (4-9) and (4-14), the circuit parameters L_{sj} and R_{Ej} determine the SR's peak current arising from the simultaneous conduction interval. However, to evaluate the resultant conduction losses, the rms current through the SRs should be investigated.

Fig. 4.8 shows the rms current in the SRs as a function of L_{sj}, R_{Ej} and I_{oj}. The rms current through SR_{f2} is always higher than that of SR_{f1}, because the duty ratio of SR_{f2} is always greater (>50%) than that of the SR_{f1} in a forward type converter. The curves 3 and 6 in Fig. 4.8a and b indicate that a smaller R_{Ej} always results in lower conduction losses, because a small R_{Ej} reduces the duration of the simultaneous conduction interval and thus the peak current. The curves 3 and 6 in Fig. 4.8c and d indicate that a smaller L_{sj} always results in higher conduction losses, because a small L_{sj} does not have sufficient current limiting capability during the simultaneous conduction interval. When the circuit is designed properly, the short circuit interval can be limited, and excessive rms current or conduction losses can be prevented.

4.3.4.3 Effects of SR Simultaneous Conduction on Primary Circuit

The simultaneous conduction interval of the SRs has an effect on the current stress of S_{main} in the primary circuit. During the power transfer, namely Mode 2 of Section 4.3.1.2, the total primary current is simply given by the following,

$$i_d(t) = i_m(t) + \sum_j \frac{I_{oj}}{k_j} \tag{4-19}$$

The drain current during the SR simultaneous conduction intervals are determined by the following:

$$i_d(t) = i_m(t) + \sum_j \left(\frac{V_d}{k_j^2 L_{sj}} (t - \frac{D - d_j}{f_{sw}}) + \frac{I_{oj}}{k_j} \right) \tag{4-20}$$

From (4-9) the peak drain current of S_{main} is approximately determined by

$$I_{d\_pk} = \sum_j \frac{I_{sj}}{k_j} = \sum_j \left(\frac{V_d}{k_j^2 L_{sj}} \frac{d_j}{f_{sw}} + \frac{I_{oj}}{k_j} \right) \tag{4-21}$$

Substituting (4-18) into (4-21), the maximum drain current of S_{main} is determined by:

$$I_{d\_\max} = \sum_j \left(\frac{R_{Ej} + f_{sw} L_{sj}}{k f_{sw} L_{sj}} I_{oj\max} + \frac{V_{d\max}}{k_j^2 f_{sw} L_{sj}} d_{mj} \right) \tag{4-22}$$

It is seen that the maximum drain current of S_{main} will always reach the same magnitude as given by (4-22) under all load conditions. The total rms current through S_{main} is mainly determined by (4-19), (4-21) and $i_a(t)$ discussed in Section 2.4.1, which will not be discussed further.

4.3.4.4 Effects of SR Simultaneous Conduction on the Self-Reset Power Transformer

Comparing the DPUPS and the Type 1 converter, a basic difference is that there is an SR simultaneous conduction interval (Interval 5aj) in the DPUPS, namely the interval between t_{4aj} and t_5.

Owing to this simultaneous conduction interval, as indicated in (5-22), the peak drain current of S_{main} will not change in the DPUPS, regardless the load condition. This constant current stress will always charge the snubber capacitor to the same peak drain voltage of S_{main}, which represents the magnitude of the driving force to reset the power transformer in the rest of the switching cycle. Consequently, contrary to the Type 1 topology, the flux swing range will not vary with load in the DPUPS, although it still varies with other parameters. This brings another advantage, namely the worry that the self reset transformer might saturate under light or no load conditions is no longer an issue for the DPUPS.

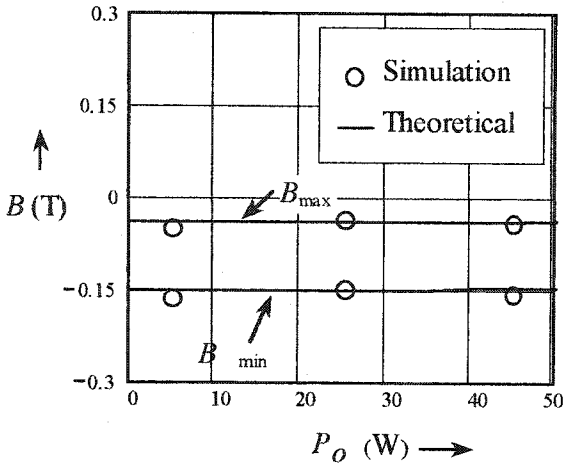


Fig. 4.9 Power transformer flux excursion vs. load in the DPUPS. The two output loads vary at the same scale from zero to full load.

The calculation of the flux excursion in the DPUPS is provided in the second part of spreadsheet of Appendix E. Fig. 4.9 shows a typical curves of the flux excursion under variable load conditions. The simulation results are also shown to verify the theoretical analysis. Because the flux excursion is independent of the load conditions, only the flux excursion curves at full load like the ones in Fig. 2.13a,c,g,i need to be referred in design.

4.3.4.5 Soft Switching of the SRs

The pair SRs can achieve soft switching at both turn-on and turn-off. SR_{f1} can achieve ZVS turn-off by withdrawing the gate drive signal a little bit ahead of the end of Mode 4 (Fig. 4.4d), because the secondary current will divert from its main channel to its body-diode and thus clamping the drain-to-source voltage at zero. It can achieve ZVS turn-on by giving a little delay in its gate drive, since the delay time permits the increasing secondary current to discharge SR_{f1} inherent drain-to-source capacitor at the beginning of Mode 1 (Fig. 4.4a).

SR_{f2} can achieves ZVS turn-off by withdrawing the gate drive signal a little bit

ahead of the beginning of Mode 2 (Fig. 4.4b), because continuing flowing current through SR_{f2} branch will divert from its main channel to its body-diode, thus clamping its drain-to-source voltage at zero. SR_{f2} can automatically achieve a ZCS turn-on at the beginning of Mode 3 (Fig. 4.4c), because the current that can flow into SR_{f2} branch can only rise slowly due to the current limit by L_{sj}.

In conclusion, soft switching can be achieved in the pair SRs. This will enhance the rectification efficiency of the SR stage.

4.4 SMALL SIGNAL ANALYSIS

4.4.1 Small Signal Model

Observe Fig. 4.4, one can find that the active current paths are the same for both Modes 1 and 3. Thus, the five modes can be represented with four equivalent circuits, which are shown in Fig. 4.10.

In these equivalent circuits, the following parasite parameters are also included in order to obtain an accurate dc model:

(i) R_M: the total effective resistance of the primary circuit including S_{main} Rds(ON), dc resistance of T_p, dc resistance of the PCB tracks of the power flow, etc.

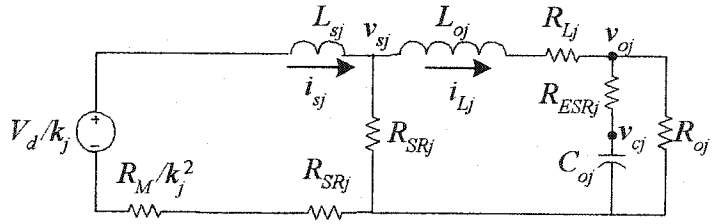
(ii) R_{Lj}: the equivalent resistance of the output inductor.

(iii) R_{SRj}: the Rds(ON) of the SRs.

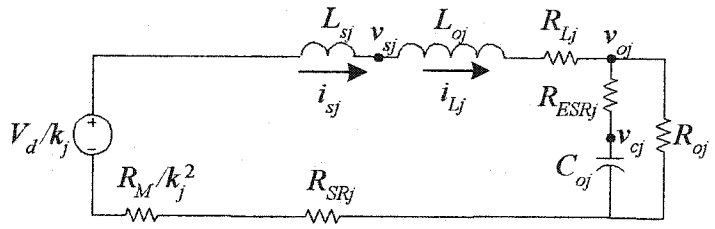
(iv) R_{ESRj}, the ESR of the output capacitor bank.

(v) L_{sj}: the current limiting inductor also including the leakage of T_p.

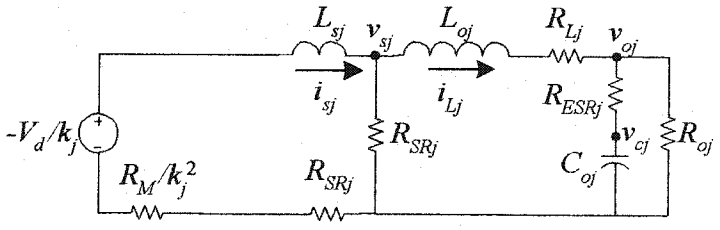
Based on the equivalent circuits, one can obtain the averaged state space model of the j^{th} output circuit as follows (See Appendix C):



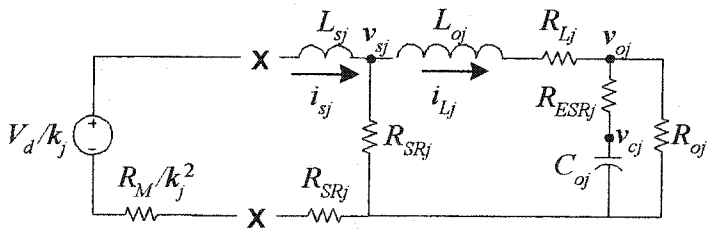
a. Modes 1 and 3. Duration: $\Delta_{j1}+ d_j$



b. Mode 2. Duration: D-Δ_{j1}-d_j



c. Mode 4. Duration: Δ_{j2}



d. Mode 5. Duration: 1-D-Δ_{j2}

Fig. 4.10 Four equivalent circuits of the five modes in the j^{th} output circuit (j=1 or 2 in a two-output example).

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = v_{sj} - R_{Lj}i_{Lj} - v_{oj} \\ L_{sj}\dfrac{di_{sj}}{dt} = (D-\Delta_{1j}-d_j)\dfrac{V_d}{k_j} - (D+\Delta_{1j}+d_j)v_{sj} - (D+\Delta_{1j}+d_j)(\dfrac{R_M}{k_j^2}+R_{SRj})i_{sj} \\ 0 = v_{sj} - (D-\Delta_{1j}-d_j)\dfrac{V_d}{k_j} + [R_{SRj} + (D-\Delta_{1j}-d_j)\dfrac{R_M}{k_j^2}]i_{Lj} - 2(\Delta_{1j}+d_j)R_{SRj}i_{sj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \quad (4\text{-}23)$$

Note that the average current of i_{Lj}, namely the dc component, is the output current I_o. From (4-23), one can obtain the following dc model of the j^{th} output circuit:

$$\begin{cases} (D-d_j-\Delta_{j1})\dfrac{V_d}{k_j} = -[R_{SRj} + R_{Lj} + (D-d_j-\Delta_{1j})\dfrac{R_M}{k_j^2}]I_o + V_o \\ V_o = V_c \\ V_o = R_{oj}I_o \end{cases} \quad (4\text{-}24)$$

Compare (4-12) and (4-24), one can easily define the Thevenin equivalents of the j^{th} output circuit as the following:

$$R_{Ej} = R_{SRj} + R_{Lj} + (D-d_j-\Delta_{1j})\frac{R_M}{k_j^2} \quad (4\text{-}25)$$

$$V_{Thj} = (D-d_j-\Delta_{1j})\frac{V_d}{k_j} \quad (4\text{-}26)$$

Equation (4-26) confirms with (4-13).

For convenience in deriving the small signal model, the internal resistances, including R_{SRj}, R_{Lj} and R_M, are assumed negligible. Thus, from (4-23), the transfer function of the j^{th} output circuit (in Laplace transform) from the control of SR_{j2} to the output is found to be as follows (Also see Appendix B):

$$\frac{\hat{v}_{oj}(s)}{\hat{d}_j(s)} = \frac{-\left(\frac{V_d}{k_j} - sL_{sj}\frac{(1-D-d_j-\Delta_{1j})V_{oj}}{(D-d_j-\Delta_{1j})R_{oj}}\right)(1+sR_{jESR}C_{oj})}{s^2L_{oj}C_{oj}(1+\frac{R_{jESR}}{R_{oj}})+s[\frac{L_{oj}}{R_{oj}}+R_{jESR}C_{oj}(1+\frac{f_{sw}L_{sj}}{R_{oj}})]+(1+\frac{f_{sw}L_{sj}}{R_{oj}})} \quad (4\text{-}27)$$

It is seen that the power circuit has a Right-Half-Plane (RHP) zero, which is caused by L_s. However, since L_s is usually very small in contrast to the boost inductor, this RHP zero is usually located in a much higher frequency range, thus the phase lag that it brings in becomes less concerned in closing the DPUPS loop. In a poor design with this RHP zero close to the intended crossover frequency, a Type-III Error Amplifier can be used to compensate the phase lag by the RHP zero. Since such issues have been well discussed in the literature [24, 72-73, 111], it will not be addressed further herein.

4.4.2 Small Signal Model Verification

To verify the model, the breadboard prototype DPUPS is used. Details of this prototype are given below Table 4.2 in the section of experimental results.

Fig. 4.11 shows the theoretical Bode Plot of the 5V output circuit of the prototype DPUPS from the output of the error amplifier to the output terminal. Fig. 4.12 shows the measured results.

Table 4.1 compares the predicted and tested control-to-output power circuit transfer function. They have a good agreement. Over the frequency range up to 60 kHz, the maximum gain error is less than 3dB. The maximum phase error is not more than 10 degree over the wide frequency range. The differences are caused by the approximation in the model, and they are also caused by test errors including the instrument calibration tolerance and reading errors.

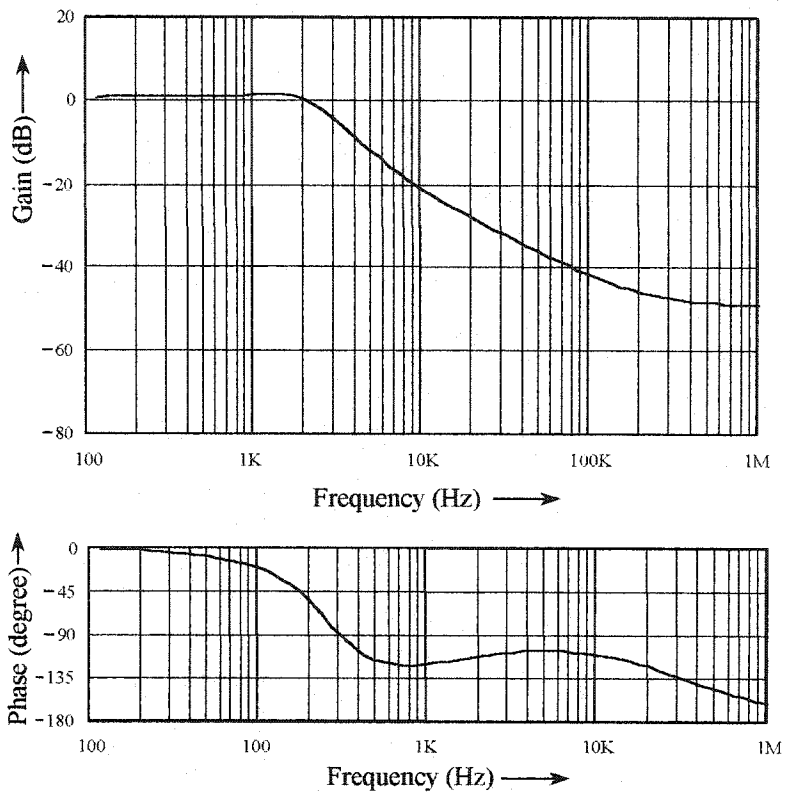


Fig. 4.11 Theoretical predicted Bode Plot of the power circuit.

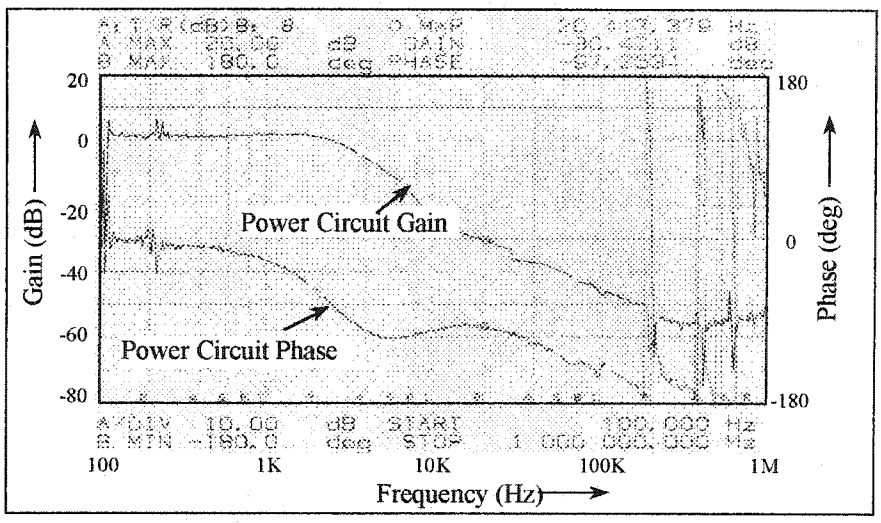


Fig. 4.12 Experimental measurement of the transfer functions of the power circuit and total open loop. V_d=50V. f_{sw}=200kHz. I_o =6A.

Table 4.1 Power Circuit Transfer Function Verification

Frequency	Gain (dB)			Phase (degree)		
	Predicted	Tested	Error	Predicted	Tested	Error
1 kHz	0.76	1.1	+0.4	-27	-25	-2
2 kHz	0.30	0.4	-0.1	-68	-59	-9
4 kHz	-8.5	-6.3	-2.2	-109	-102	-7
10 kHz	-21.0	-23.7	+2.7	-111	-101	-10
20 kHz	-28.1	-30.1	+1.5	-106	-97	-9
60 kHz	-37.8	-40.2	+2.4	-109	-125	+16
100 kHz	-41.7	-45.1	+3.4	-116	-137	+21

4.5 DESIGN PROCEDURE AND CONTROL IMPLEMENTATION

Based on the steady state analysis made in Chapters 2 and 4, a design procedure can be generated for the DPUPS of this chapter. The design shall also refer to the flux excursion range using the spreadsheet of Appendix E, in order to guarantee the successful self-reset of the power transformer.

Assume that the following principal parameters are already determined for a particular application:

(i) f_{sw}—switching frequency,

(ii) L_m—magnetizing inductance of T_p,

(iii) V_{oj}—output voltage,

(iv) I_{oj}—full load current, and

(v) $V_{d\min}$ and $V_{d\max}$—the minimum and maximum input voltage, respectively.

(vi) η_{rect}—the target efficiency in the rectification stage at full load.

4.5.1 Selection of Principal Components and Parameters

4.5.1.1 D_{max}, Maximum Duty Ratio

In steady state, the magnetizing and demagnetizing intervals of the transformer must maintain volt-second balance. The main switch duty-ratio determines the magnetizing of the power transformer, thus the maximum D should be limited below 0.5, otherwise the main switch would suffer from excessive voltage stress owing to a short demagnetizing interval.

On the other hand, D shall not be too small, or larger output filter may be required to meet the output voltage ripple specifications. It is a good practice to set the maximum D at about 0.45.

4.5.1.2 D_{aux}, Auxiliary Switch Duty Ratio

D_{aux} is fixed under all operating conditions such that the control and design of the gate drive circuit for S_{aux} can be simplified. As the auxiliary duty ratio steals some time from the permitted resetting duration, as seen from the analysis in Section 2.4.1, a large D_{aux} will narrow the reset duration. To guarantee the least reset time not to be less than the maximum magnetizing time, the fixed duty ratio of the auxiliary switch shall be limited by the following equation,

$$D_{aux} < (1 - 2D_{\max}) \tag{4-28}$$

However, D_{aux} shall not be too small, otherwise the allowable discharging time would be too narrow and it would require an excessive peak resonant current to complete the discharging of C_{snb}. A good trade-off is to select D_{aux} between 5% to 10% of a switching cycle.

4.5.1.3 Transformer Turns Ratio k_j for the j^{th} Outpout circuit

The target rectification efficiency requires the allowable maximum voltage drop across the SRs to be limited by the following:

$$V_{drop\_j} \le (1-\eta_{rect})V_{oj} \tag{4-29}$$

From (4-12) and (4-13), and limiting the total duty ratio reduction at full load not to be more than 0.05, thus,

$$\frac{V_{d\min}}{k_j}(D_{\max}-0.05) \ge V_{oj}+V_{drop} \tag{4-30}$$

$$k_j = \frac{N_p}{N_{sj}} =\le \frac{V_{d\min}}{V_{oj}+V_{drop\_j}}(D_{\max}-0.05) \tag{4-31}$$

Selection of the power transformer core and magnetizing inductance can follow the conventional design procedure.

4.5.1.4 The Synchronous Rectifiers SRs:

Allowable maximum voltage drop on the SRs shall satisfy the following:

$$V_{drop\_j} \le (1-\eta_{rect})V_{oj} \tag{4-32}$$

Thus, the total resistance of the SRs shall be limited by

$$R_{SRj} < \frac{V_{drop}}{2.8I_{oj}} \tag{4-33}$$

where the factor 2.8 takes into account the thermal effects of Rds(ON) (1.8 times at hot junction temperature) and also the PCB track impedance and L_o dc resistance.

The number of MOSFETs to be paralleled to fulfill one SR is thus given by

$$N_{SR\,j} \ge \frac{R_{D\_RS}}{R_{SRj}} \tag{4-34}$$

where R_{D_RS} is the Rds(ON) of the candidate MOSFETs to be employed. However,

excessively large number of N_{SRj} should be avoided. Otherwise, the costs and circuit size would be unnecessarily increased, in addition to the increased gate-drive power for larger number of paralleled SRs.

On the other hand, the candidate SR MOSFET shall meet the current and voltage ratings. The RMS current shall refer to the curve given in Fig. 4.8, and the voltage rating for both SRs can be determine by the following equations, respectively.

$$V_{R\_SRj1} = \frac{2V_{d\max}}{k_j} \tag{4-35}$$

$$V_{R\_SRj2} = \frac{2V_{d\max}}{k_j} \tag{4-36}$$

The factor of 2 in (4-35) takes into account the voltage overshoot due to the effects of the leakage inductance.

4.5.1.5 Snubber Capacitor C_{snb}

When S_{main} is turned off, C_{snb} must handle the maximum drain current given by (4-22). Seen from (2-34), the drain voltage rises approximately by the following,

$$\Delta u_{d1}(t) \approx \frac{I_{d\_\max}}{C_{snb}}(t - t_3) \tag{4-37}$$

To achieve a soft switching turn-off, C_{snb} should be so chosen to limit u_{d1} below V_d within an expected rise time t_r. This rise time is usually about a few hundred nanoseconds. Then, by (4-37), the capacitor should satisfy the following equation:

$$C_{snb} > \frac{I_{d\_\max}}{V_{d\min}} t_r \tag{4-38}$$

On the other hand, as seen from (2-41), C_{snb} determines the duration of Interval 7 in which L_s transfers its energy to C_{snb}. The worst case duration that happens under no load condition must be limited within the permitted margin left by balanced

magnetizing/demagnetizing time, which is approximately ($1-D_{aux}-2D_{max}-t_r/f_{sw}$), in order not to exert an excessive voltage stress on S_{main}. Therefore, the maximum value of C_{snb} shall be limited by.

$$C_{snb} \le \frac{1}{f_{sw}^2 k^2 L_s}(1 - D_{aux} - 2D_{\max} - \frac{t_r}{f_{sw}})^2 \tag{4-39}$$

4.5.1.6 Current Limiting Inductor L_{sj}

In a practical circuit, L_{sj} can just be T_r's leakage inductance if it is large enough. The stray inductance of the circuit can also contribute to the total effective value of L_{sj}, although it is normally negligible. When these parasites are not large enough, an additional inductor shall be added.

Seen from (4-3) and (4-26), L_{sj} reduces the effective duty-ratio by Δ_{j1}. Thus, L_{sj} shall not be too big in order to avoid excessive duty-ratio reduction, otherwise a larger output inductor must be employed to meet the output ripples specifications. On the other hand, as seen from (4-9) and (4-22), L_{sj} should not be too small, or excessive current would be resulted during the SR simultaneous conduction interval.

Therefore, a reasonable tradeoff is to set Δ_{j1} between 0.05 and 0.1. On the other hand, the peak current arising from the SR simultaneous conduction interval should not be more than two times of the maximum load current. Thus, from (4-9) and (4-22), the following condition shall be satisfied in the selection of L_{sj}.

$$L_{sj} < \frac{V_{d\min}}{k_j f_{sw} I_{oj\max}} \Delta_{1j} \tag{4-40}$$

$$L_{sj} > \frac{R_{Ej}}{f_{sw}} \approx \frac{2R_{SRj}}{f_{sw}} \tag{4-41}$$

Assuming L_{ljk} is T_p leakage inductance seen by the pair SRs in the j^{th} output, then the

required additional inductor is given by

$$L_{sj\_external} = L_{sj} - L_{lkj} \tag{4-42}$$

It is important to point out that L_{sj} must be prevented from saturation, otherwise it would lose the voltage decoupling function and failure of whole circuit could happen.

4.5.1.7 Resonant Tank L_a-C_a

The inductor L_a controls the speed of discharging of C_{snb}. It shall be selected such that C_{snb} can be completely discharged before S_{main} is turned on. Since the maximal allowable time for the discharging process is limited by S_{aux} duty ratio D_{aux}, the discharging duration $(t_1\text{-}t_0)$ in a fraction of D_{aux} shall be lower than 1. On the other hand, $(t_1\text{-}t_0)$ shall not be too short, otherwise the resonant discharging current would have a very high peak.

The longest discharging duration corresponds to maximum input voltage and full load condition. Obtained numerically from (2-5), Fig. 4.13 shows the relationship between the discharging interval $(t_1\text{-}t_0)$, D_{aux}, L_a and the total equivalent inductance of all L_{sj} seen by the primary circuit that is given by

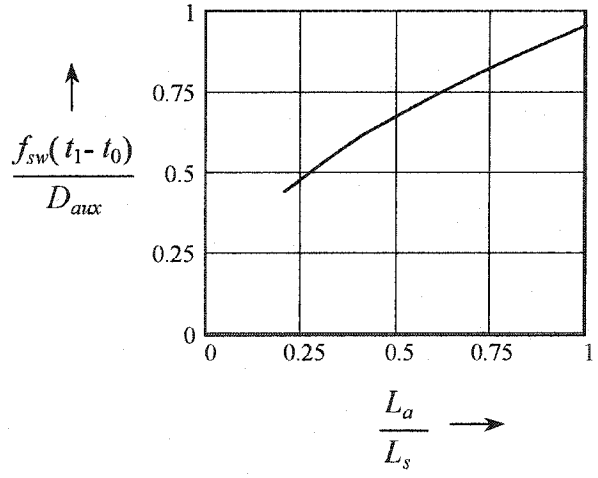


Fig. 4.13 Relationship between L_a, L_s, D_{aux} and C_{snb} discharging time.

$$L_s = \frac{1}{\sum_j \frac{1}{k_j^2 L_{sj}}} \tag{4-43}$$

Seen from Fig. 4.13, in order to limit the discharging interval in between 70 to 90% of D_{aux}, L_a shall be selected according to the following criterion,

$$L_a = 0.5 \sim 0.9 L_s \tag{4-44}$$

C_a shall be much greater than C_{snb} such that its voltage rise during the discharging of C_{snb} does not counteract the discharging process. The following condition shall be satisfied:

$$C_a > 5C_{snb} \tag{4-45}$$

However, in order to complete the energy recovery before S_{main} is turned off, the reversed resonant current shall complete its second half cycle within the minimum duty ratio of S_{main}. Referring to (2-28), C_a shall be limited by,

$$C_a \le \frac{D_{\min}^2}{\pi^2 f_{sw}^2 L_a} \tag{4-46}$$

4.5.1.8 Main Switch S_{main}

It should be low Rds(ON) MOSFEF and meet the power rating requirements. Several MOSFETs can be used in parallel to achieve an equivalently low Rds(ON) S_{main}. The equivalent Rds(ON) shall be smaller than total R_{RSj} when reflected into the primary side. Assume R_{D_main} is the Rds(ON) of individual MOSFET of a selected product, then the suggested number of parts to be paralleled for S_{main} shall satisfy:

$$N_{main} \ge 1.8 R_{D\_main} \sum_j \frac{1}{k_j^2 R_{SRj}} \tag{4-47}$$

where N_{main} is the number of MOSFETs to be paralleled, and the factor of 1.8 takes into

account the thermal effects on the MOSFET Rds(ON). However, excessively large number of N_{main} shall be avoided. Otherwise, the costs and circuit size would be unnecessarily increased, in addition to the increased gate-drive power for larger number of paralleled S_{main}.

The ratings of individual device of S_{main} shall satisfy the following:

$$I_D > \frac{1.5}{N_{main} V_{d\min} \sqrt{D_{\max}}} \sum_j V_{oj} I_{oj\max} \tag{4-48}$$

$$V_{ds} > 1.2 V_{pk} \tag{4-49}$$

where V_{pk} is determined by (2-42), and the factor of 1.5 takes into account an minimal efficiency of 70%, the square root of D_{max} convert the current into rms values, and the factor of 1.2 takes into account the voltage overshoot caused by the leakage inductance.

4.5.1.9 Auxiliary Transformer

The auxiliary transformer shall handle the power discharged from C_{snb}, and the maximum of this power is about $2f_{sw}C_{snb}V_{d\max}^2$. The center-tapped secondary windings shall have the same number of turns to facilitate the design, manufacturing and installing onto the circuit board.

T_a turns ratio k_a (k_a=N_{ap}/N_{as}) shall be low to limit the reflected V_d through the coupling of T_a, otherwise the reflected voltage would be significant to counteract the discharging of C_{snb}. However, k_a shall not be excessive to avoid the use of an unnecessary large magnetic core. The following conditions can be used to select k_a:

$$\frac{1}{10} < k_a < \frac{1}{5} \tag{4-50}$$

4.5.1.10 Auxiliary Switch S_{aux}

Although S_{aux} is soft switched both at turn-on and turn-off, it still suffer from the

so-called $\frac{1}{2}CV^2$ losses at turn-on caused by its inherent drain-source capacitance. In order to limit the total losses in S_{aux}, a trade-off in its selection should be made between the least inherent capacitance and the least on-resistance. Its current rating should be able to handle the discharging current given by (2-17) and (2-18), and since it is actually in parallel with S_{main} during the OFF state, its voltage rating is determined by (4-49).

4.5.1.11 Auxiliary Rectifier Diodes D_{a1}, D_{a2}

They shall use ultra-fast diodes, or high voltage Schottky diodes if available. Refer to the analysis in Section 2.4.1, one can find that their voltage ratings shall meet the following requirement:

$$V_{R\_Da} = 2V_{d\max} \tag{4-51}$$

Since each of the diode handles half of the discharged energy, the diode forward current rating shall meet the following requirement

$$I_{F\_Da} = f_{sw}C_{snb}V_{d\max} \tag{4-52}$$

and the peak current rating shall satisfy the values related to (2-17) and (2-18).

4.5.1.12 Others

The selection of the output filters can follow the conventional criteria to achieve the specified output ripple voltage and ripple current requirement for a particular application, which will not be repeated herein.

ZVS of SR_{j1} can be achieved by delaying its gate drive signal. Assume SR_{j1} inherent drain-to-source capacitance is C_{oss_SRj}, gate to source capacitance is C_{iss_SRj}, the gate threshold voltage is V_{th}, the maximum voltage level of the self-driven gate drive is V_{gmax}, and the gate drive resistor is R_{gj1}. When SR_{j1} is OFF, its drain-to-source inherent capacitor C_{oss_SRj} stores an amount of charge that is approximately determined by

$$Q_{j1} = \frac{C_{oss\_SRj} V_d}{k_j} \tag{4-53}$$

Be delaying the gate signal at turn-on, C_{oss_SRj} stores will be discharged by the secondary current. Thus, from (4-1) and (4-53), the required time to completely discharge the stored charge is approximately determined by

$$t_d = \sqrt{2 L_{sj} C_{oss\_SRj}} \tag{4-54}$$

This delay time can be achieved if R_g is selected according to the following condition:

$$R_g \geq \frac{t_d}{C_{iss\_SRj} \ln\left(\frac{V_{g\max}}{V_{g\max} - V_{th}}\right)} \tag{4-55}$$

4.5.2 Implementation of the Voltage Feed-Forward Control

Simple implementation for the voltage feed-forward control circuit is given below. Other implementations are possible but will not be discussed further herein.

4.5.2.1 Generating of the Gating Pattern for S_{aux}

The voltage feed-forward control circuit will generate a single PWM signal, and this single signal can be split into the two gating signals for S_{aux} and S_{main}, respectiavely. Appendix G shows a simple implementation of such a splitter that is originally reported in [106].

4.5.2.2 Voltage Feed-Forward Control Circuit

As mentioned above, the feed-forward control circuit shall produce a PWM signal with a pulse width of D_{aux}+D, of which the duty ratio D for S_{main} shall satisfy (4-17).

Fig. 4.14 shows a simple implementation of the feed-forward control circuit, and Fig. 4.15 shows key waveforms of this circuit.

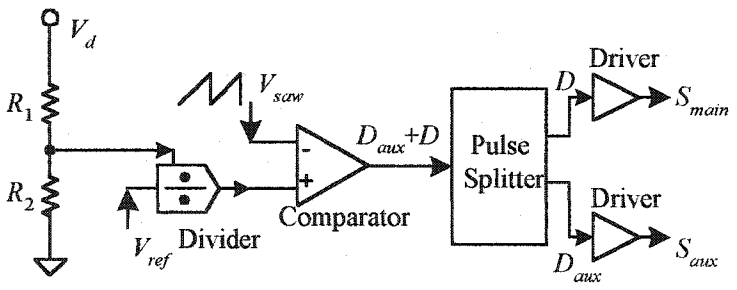


Fig. 4.14 Control implementation of the feed-forward control circuit.

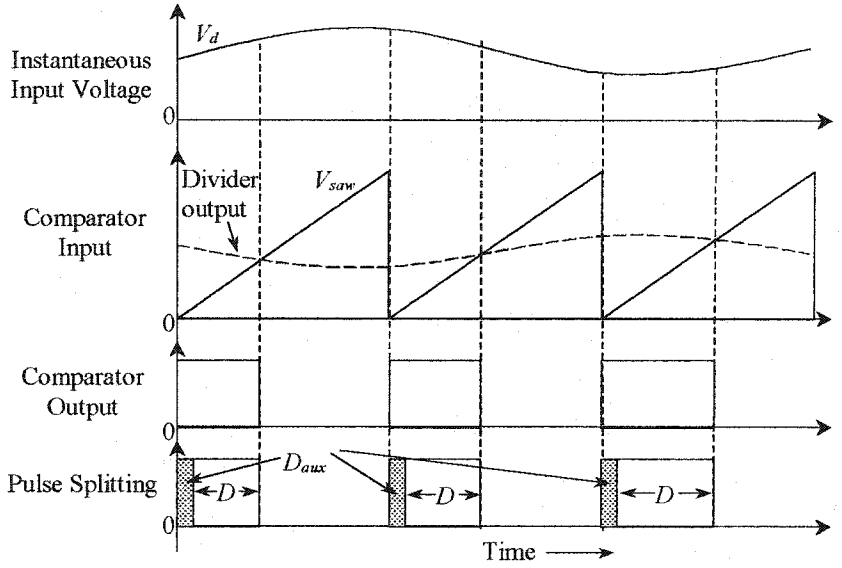


Fig. 4.15 Key waveforms of the feed-forward control circuit.

In the prototype DPUPS, an multiplier/divider AD734 (courtesy of Analog Device Inc.) is used to perform the inverse function of the input voltage. A 5V reference voltage V_{ref} is use for the divider. The output voltage of the divider compares with a 200kHz, 5V pk-pk saw-tooth signal to generate the PWM signal. CMOS logic circuits of MC74HC-- series are uses for the splitter to split the pulse into two parts, of which a smaller pulse with fixed pulse-width for the auxiliary switch, and a larger pulse with modulated pulse-width for the main switch. Drivers of IR2110s are used to drive the switches.

4.5.3 Implementation of Controls of the SRs.

4.5.3.1 Control of SR_{j1}

SR_{j1} can be directly driven by the secondary winding as shown in Fig. 4.2, or be driven by a separate winding if the secondary winding does not produce proper voltage level. It can also be driven by S_{main} gating signal, however, a pulse transform is thus required for the isolation purpose, and a buffer circuit may also be required in order not to overload S_{main} gate driver.

4.5.3.2 Feedback Control Circuit to Control SR_{j2}

The modulation of the pulse width for SR_{j2} must satisfy (4-18). The timing of the generated PWM must be synchronized to the main switch frequency, and this can be obtained by sensing the secondary voltage pulse and this does not break the primary/secondary isolation boundary.

Fig. 4.16 shows a simple implementation of the feedback control circuit for the arbitrary j^{th} output circuit, and Fig. 4.17 shows key waveforms of this control circuit.

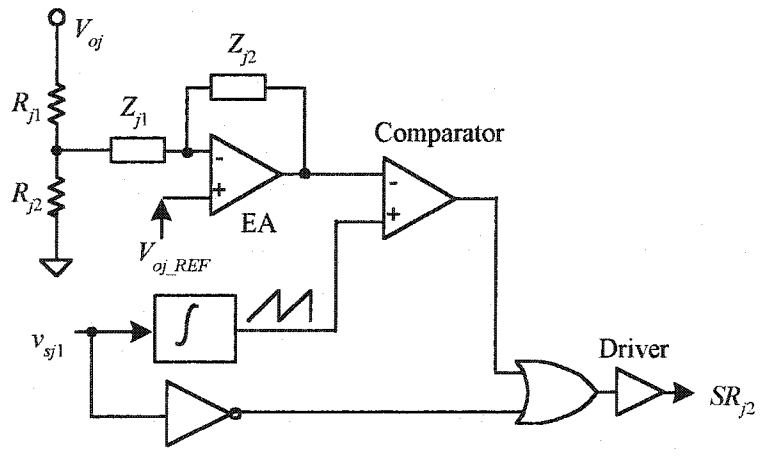


Fig. 4.16 Feedback control circuit implementation.

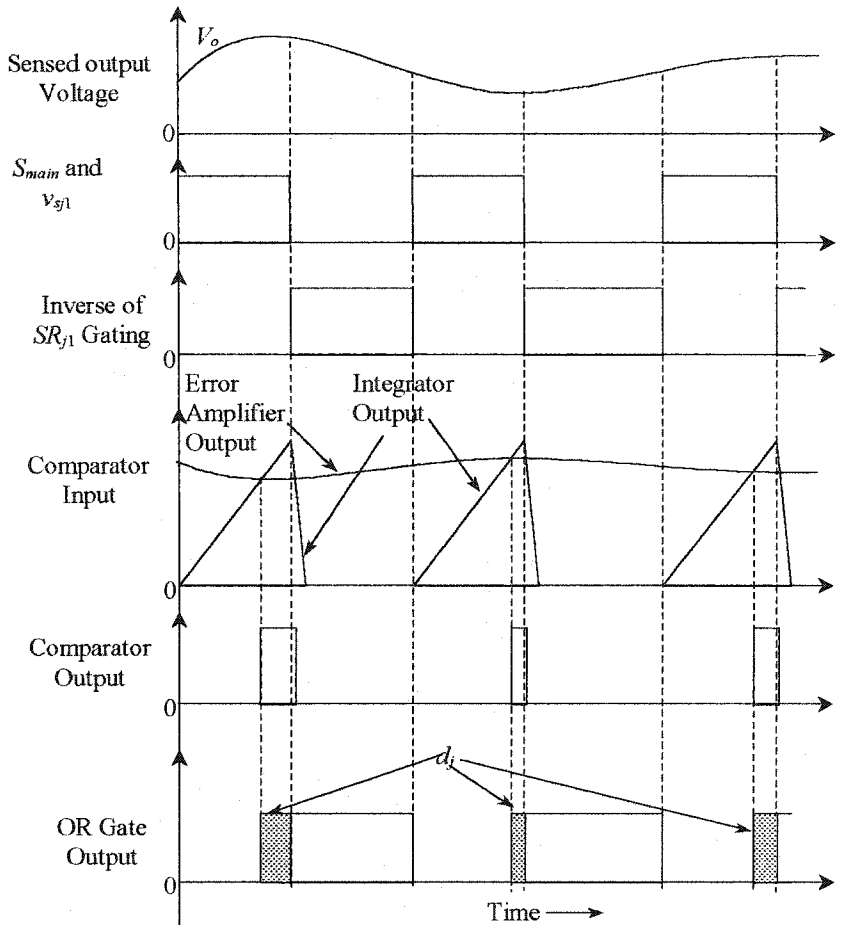


Fig. 4.17 Key waveforms of the feedback control circuit.

The integrator converts the sensed secondary voltage pulses into a saw-tooth waveform to be used by the comparator, and this synchronizes the clock of the feedback control circuit to the main switch frequency

In the prototype DPUPS, the voltage error amplifier uses AD844, the comparator uses AD790. The Integrator also uses AD844, and a IRF510 is employed to reset the integrator output each cycle. The logic circuits employs MC74HC-- series CMOS devices, and the MOSFET drivers are implemented with IR2110.

4.5.4 A Design Example

As a design example, the prototype DPUPS is designed by using above design criteria. The principle parameters and components of the prototype are given in Table 4.2.

Table 4.2 Principal Components of the Prototype DPUPS

Components	**Values/Selections**	
	2V circuit	**5V circuit**
S_{main}	IRF640, two in parallel	
L_{sj}	0.15 μH	0.9 μH
k_j	15:2	15:5
SR_{j1}, SR_{j2}	MTP75N05	IRFZ44
L_{oj}	3.6μH	24μH
C_{oj} Bank	64μF Tantanlum +482.2μF Electrolytes	47μF Tantanlum +102.2 μF Electrolytes
Maximum Load	15 A	6A
T_p	PQ2625-3F3, L_m=360μH	
T_a	Gapped SP41408	
L_a/C_a	2 μH/66 nF	
C_{snb}	10 nF	
S_{aux}	IFR634	

4.6 EXPERIMENTAL AND SIMULATION RESULTS

To prove the concept of the proposed DPUPS, simulation and experiment are carried out. A two-output prototype DPUPS mentioned in Section 4.5.5 is built on the breadboard. Its two outputs are 2 V 30 W and 5 V 30 W, respectively, and the operating frequency is 200 kHz. The input voltage range is from 35 to 60 Vdc.

4.6.1 Experimental Results

4.6.1.1 Key Waveforms

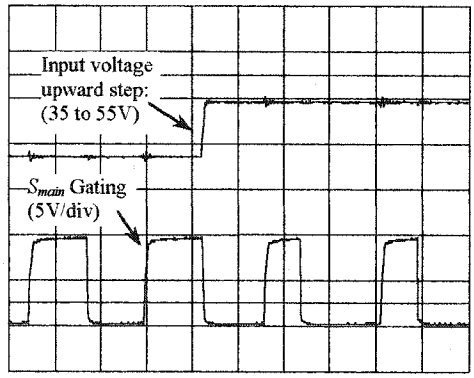
Fig. 4.18 shows the gating signals under step line and load conditions. The high frequency noises in Fig. 4.18b is due to the ground noise on the scope probes.

As seen in Fig. 4.18a, main switch gating reacts instantaneously against the input voltage step. This verifies the implementation of the feed-forward control circuit.

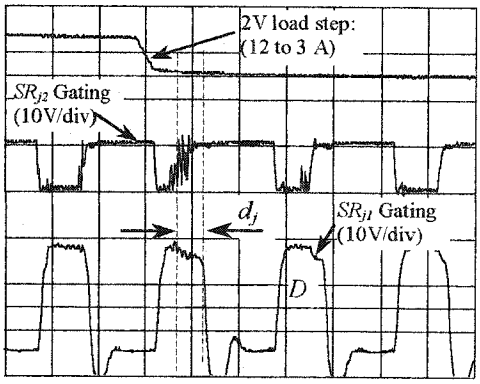
It is seen from Fig. 4.18b that the gating signal of the shunt SR, namely SR_{f2}, also reacts within one cycle, and the pair SR simultaneous conduction interval increases immediately as the load decreases. This proves the feed-back control circuit design.

Fig. 4.19 shows a detailed look of the gating signals of the pair SRs under different load conditions in the 2V output circuit. Again, the simultaneous conduction interval of the pair SRs increases as the load decreases, proving the analysis.

Fig. 4.20 shows the current through the front SR (namely SR_{f1}) in the 2V output circuit under different load conditions. Although the simultaneous conduction interval is increased at no load, the peak current is almost constant, and this verifies (4-22). Moreover, the rms current is seemingly lower under no load than that under full load conditions. This indicates that even at open circuit, the conduction losses are well limited.

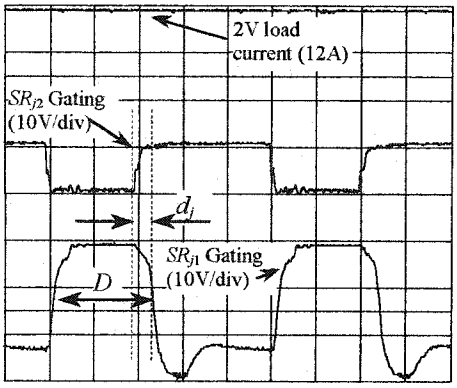


a. The feed-forward controlled gating signal response to input step. f_{sw}=200kHz. Timing-2μs/div.

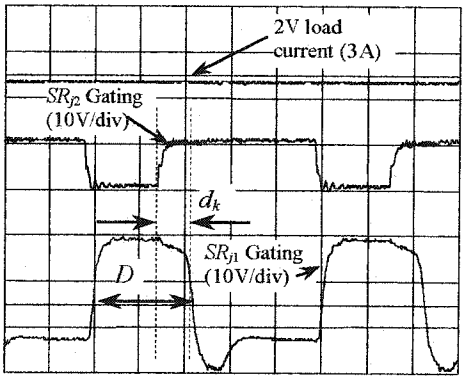


b. The gating signal in response to step load conditions for the 2V output circuit. V_d=55V, f_{sw}=200kHz, Timing-2μs/div.

Fig. 4.18 The gating signal under dynamic conditions.

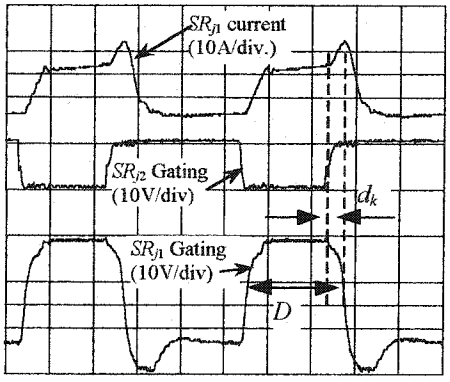


a. The gating of the SRs at full load for the 2 V output. I_o=12 A.

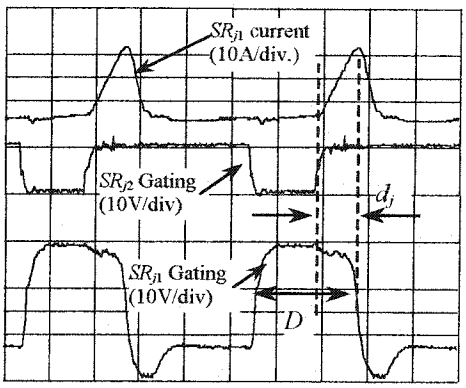


b. The gating of the SRs at no load for the 2 V output. I_o=0 A.

Fig. 4.19 The gating of the SRs under different load conditions for the 2V output. V_d=55V, f_s=200kHz. Timimg-1μs/div.



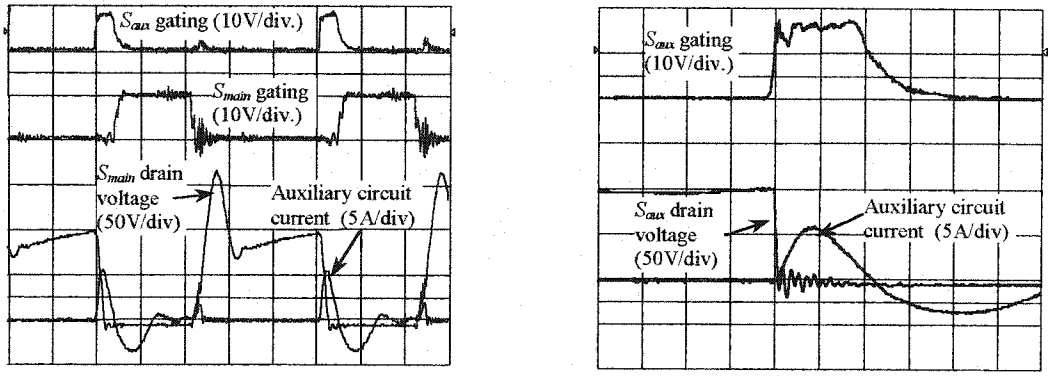
a. Gating and drain current of the front SR of the 2V output at full load (12A)



b. Gating and drain current of the front SR of the 2V output no load (0A)

Fig. 4.20 The front SR Current waveform in the 2 V output circuit under different load conditions. V_d=55V, f_s=200kHz. Timimg-1μs/div.

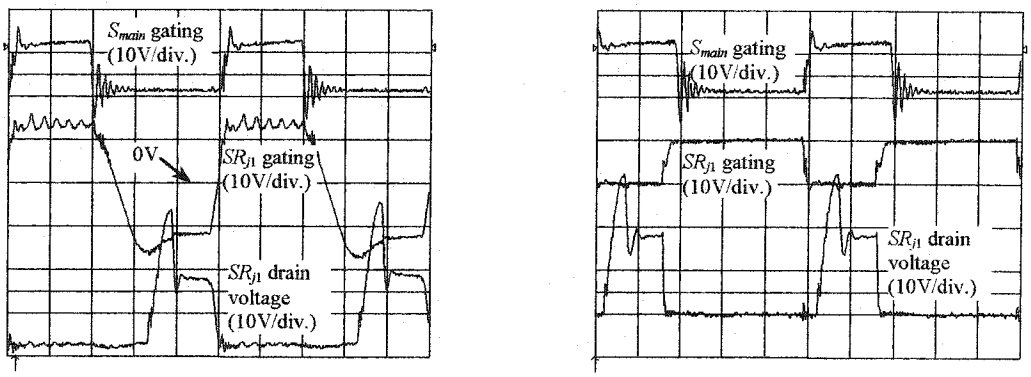
Fig. 4.21 shows the soft switching being achieved in the main and auxiliary switches. In Fig. 4.21a, the current of the auxiliary circuit discharges S_{main} snubber capacitor before S_{main} is turned on, and S_{main} gating comes after the drain voltage drops to zero, indicating a ZVS turn-on. At turn-off, due to the snubber capacitor, the drain voltage rise after the gating has already tripped to low level, indicating a ZVS turn-off. S_{main} drain current waveform is not recorded, because a long wire loop must be added to admit the current probe and this long wire loop will interfere with the nominal operation.



a. S_{main} ZVS turn-on and turn-off. Timing: 1μs/div.

b. S_{aux} ZCS turn-on and ZVS turn-off. Timing: 0.2μs/div.

Fig. 4.21 Soft switching of the main and auxiliary switches.



a. The front SR (SR_{f1}) soft switching.

b. The shunt SR (SR_{f2}) switching.

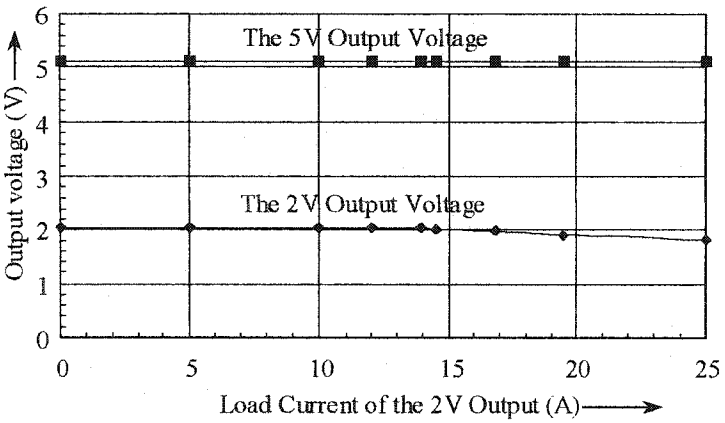
Fig. 4.22 Soft switching of the 5V output circuit synchronous rectifiers.
Timing: 1μs/div. Vertical scale for all traces: 10V/div.

Seen in Fig. 4.21b, S_{aux} achieves a zero current switching (ZCS) turn on. At turn-off, S_{aux} drain voltage is clamped at zero, hence it achieves a ZVS turn-off. In summary, the prototype DPUPS achieves soft switching.

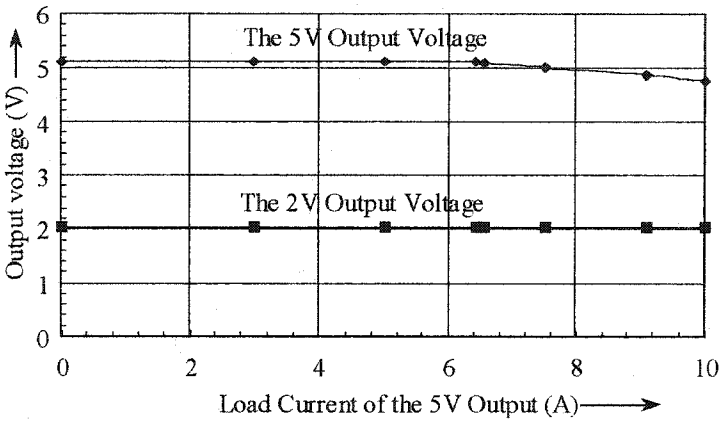
Fig. 4.22 shows soft switching of the 5V output circuit SRs. Similar waveforms are observed on the 2V circuit SRs. The spike on the front edge of the drain voltage pulses is caused by the resonance between the transformer leakage and the SR MOSFET inherent drain-to-source capacitor. The main switch gating signal is also shown as a timing reference. For the said reason, the drain current is not shown. However, it is obvious that the front SR (namely SR_{f1}) achieves ZVS at both turn-on and turn-off. Because the self-driven gating signal always comes after the SR drain voltage has already decreased to zero and withdraws before the SR drain voltage start to rise. The shunt SR (namely SR_{f2}) achieves a ZVS turn-off, because its drain voltage rises from zero after its gate drive has already withdrawn. Although hardly seen from Fig. 4.22b, the shunt SR achieves a ZCS turn-on, due to the current limitation by L_{sf}.

4.6.1.2 Regulation and Cross-Regulation

Fig. 4.23 shows the output voltage regulation against the load currents. The voltage regulation of one output is totally independent of the load condition of the other output, indicating the elimination of cross regulation in the DPUPS. However, when an output provides an excessive load current, it will lose regulation, and the voltage will decrease in almost a linear way vs. the load current. The loss of regulation in the pertinent output can be explained as follows.

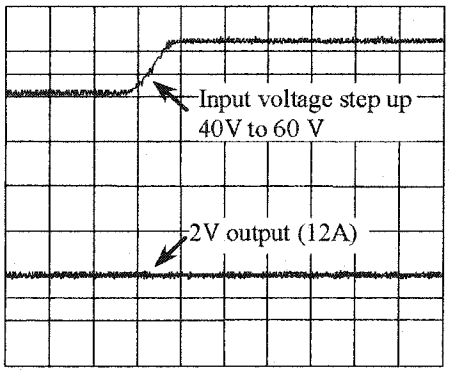


a. Output voltages vs. the 2V output current. The 5V output current is at 6A constant.

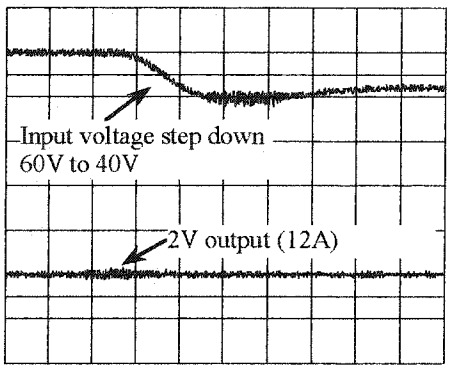


b. Output voltages vs. the 5V output current. The 2V output current is at 12A constant.

Fig. 4.23 Experimental results of output regulation and cross regulation vs. load. The cross-regulation is eliminated between the two outputs.

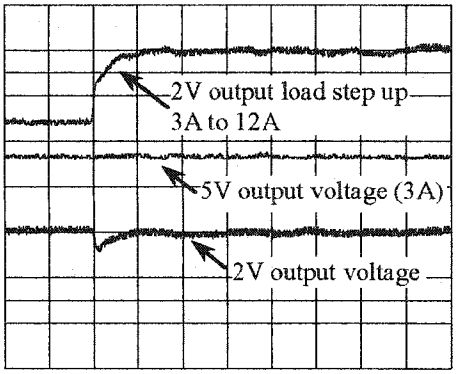


a. Regulation vs. input voltage upward step

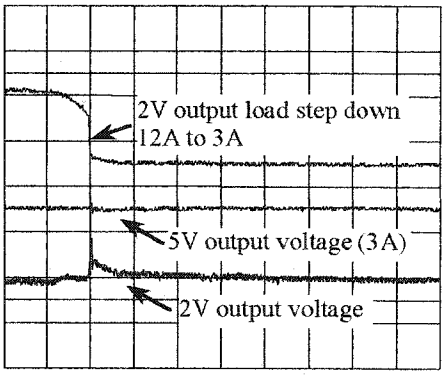


b. Regulation vs. input voltage downward step

Fig. 4.24 Step input voltage response in the 2V output circuit.
Time scale: 10 ms/div. Vertical scales: 20V/div. for the input voltage, 1V/div. for the 2V output voltage.



a. Regulation against load upward step and elimination of cross-regulation



b. Regulation against load downward step and elimination of cross-regulation

Fig. 4.25 Step load response in the 2V output circuit.
Time scale: 0.1 ms/div. Vertical scales: 5A/div for the load current, 1V/div. for the 2V output voltage.

Refer to (4-12) and (4-26), and note that S_{main} duty ratio D is only feed-forward controlled and does not react to the load changes. When the load current increases, the output regulation is achieved by decreasing d_k to compensate the internal voltage drops. However, when the load current keeps increasing, d_k will decreases to zero and cannot further compensate the internal voltage drops at these excessive load currents. Thus, the output voltage will lose regulation and starts to decrease as the load current increases, providing an inherent overload protection.

Also obtainable from Fig. 4.23 is the output resistor of each output circuit, which yields 23.4mΩ for the 2V output and 99.6mΩ for the 5V output, and it reflects the losses on all parts along the secondary current paths, including the SRs, output filters, decoupling inductors, transformer windings, and the circuit tracks. These output resistors are much higher than the SRs Rds(ON) (see Table 4.2). The reasons for these large internal resistances include the poor layout of the breadboard circuit, lack-of copper on the power tracks, and non-optimized magnetics. This also explains the lower-than-expected efficiency shown below.

4.6.1.3 Step Responses

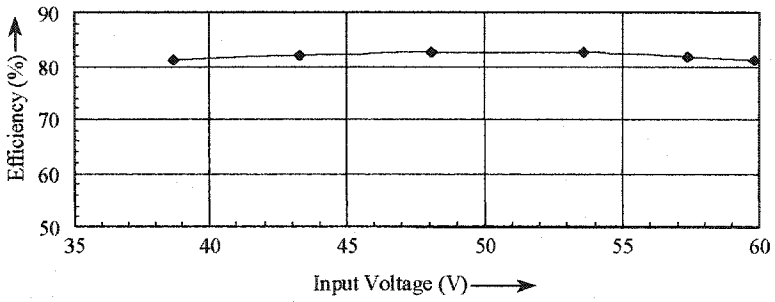
Fig. 4.24 shows the prototype DPUPS responses to input voltage step changes. It is seen from Fig. 4.24a and b that the output voltage is nearly immune to the disturbance in the input voltage, and this verifies the instantaneous regulation against the input with the feed-forward control.

Fig. 4.25 shows the prototype DPUPS responses to load step changes. The load step changes in one output circuit hardly affects the other output voltage, experimentally proving the independent regulation of each output and the elimination of cross-regulation. The large spike in the output voltage response is caused by the large ESR in the output capacitor bank made of low quality parts. Using high quality capacitors will significantly reduce the voltage spike.

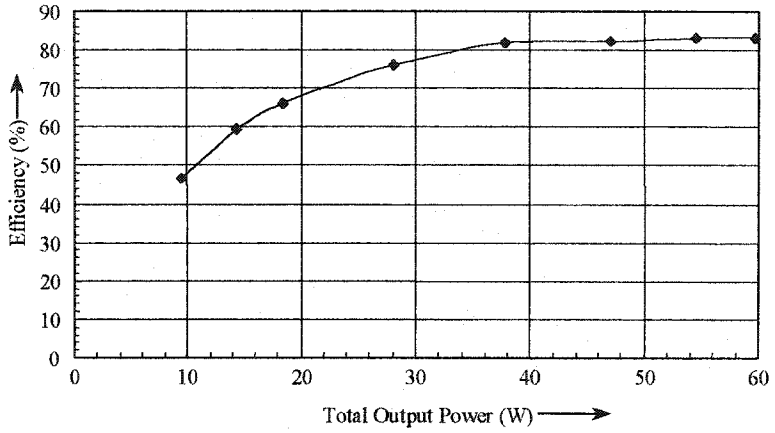
4.6.1.4 Efficiency

Fig. 4.26 shows the overall efficiency of the prototype DPUPS. Seen from Fig. 4.26a, as the function of input voltage, the overall efficiency under full load condition is almost constant over the input voltage range, with a slight drop at both ends.

At the minimum input voltage, the conduction losses are higher due to the increased rms current for a given output power. At the higher end of the input voltage, the snubber capacitor will be charged to a higher level and this need a higher current to discharge for the ZVS operation, and this increased discharging current and thus increases the conduction losses. In addition, since SR_{f1} is self-driven by a transformer winding, the gate-drive losses will increase with the input voltage owing to a higher gate drive voltage applied to the SR gate. At medium input voltage, each type of losses is not excessive, and thus the efficiency is the highest.



a. Efficiency vs. input voltage at full load



b. Efficiency vs. load at input voltage of 48V.

Fig. 4.26 Overall efficiency of the prototype DPUPS. Each output has 50% of the total output power.

As a function of load, as seen in Fig. 4.26b, the efficiency stays almost constant over the range from 100% to 70% of the full power, and it drops as the output power decreases further. This is because when the loads decrease from the full power, the conduction losses also decreases, therefore the overall efficiency can be kept almost constant. However, as the power decreases further, the simultaneous conduction interval d_j of the pair SRs in each output circuit becomes greater, as indicated by (4-14). Then, the conduction losses arising from the increased d_j become more significant, and hence the overall efficiency drops more and more rapidly as the output power decreases.

The prototype DPUPS only yields a maximum efficiency of about 83% at full load. This lower than expected efficiency confirms with the excessive output resistance implied in Fig. 4.23. However, this efficiency can be improved significantly when the

following are satisfied: (i) better MOSFETs like future products can be used for the switches and SRs, (ii) the magnetics are optimized, and (iii) the circuit can be built on a neat PCB.

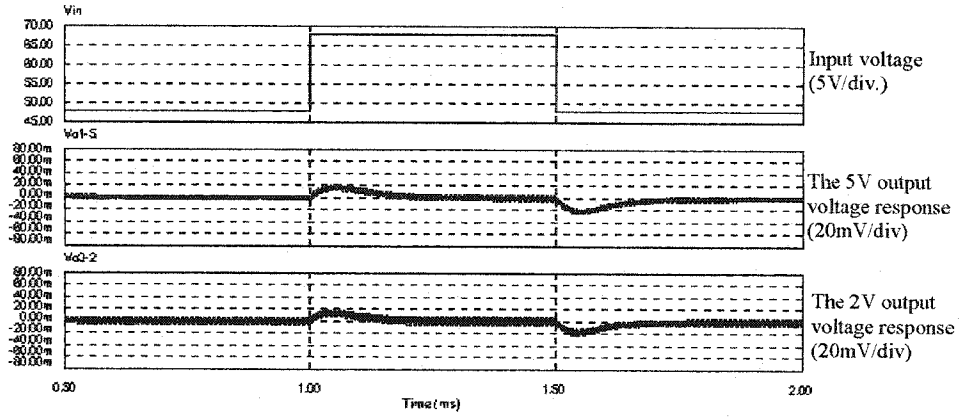
4.6.2 Simulation Results

Due to the limitation of the available test facility, simulation is used instead to investigate the DPUPS dynamic properties under high-slew rate large signal transients in both input voltage and load current. Such transients in the input dc bus may be caused by the hot insertion of an adjacent board, or the noise picked up by the bus from other sources. The high slew rate transients in the load are normally created by the high speed electronic loads like the microprocessor.

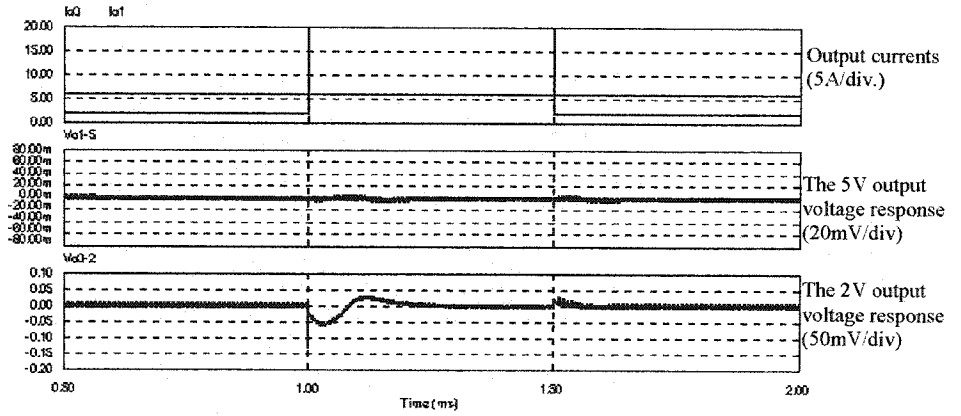
The Psim software is used to carry out the simulations. The Psim models of the DPUPSs are presented in Appendix H. The circuit parameters of Table 4.2 are used, with the exception that the poor output capacitor bank is now replaced with very low ESR capacitors in simulation. Specifically, the 2V output capacitor bank will consist of the following components in parallel: (i) 24 high frequency ceramic capacitors of 10 μF each with a ESR of 3.97 mΩ and an Equivalent Series Inductance (ESL) of 0.9 nH; and (ii) 10 Oscon capacitors of 560 μF each having an ESR of 14 mΩ, and an ESL of 4nH. The 5V output capacitor will use 2 Oscon capacitors of 220 μF each having an ESR of about 20 mΩ. The loop for each output circuit will be tailored to crossover around 20 kHz, with a phase margin around 60 degree.

4.6.2.1 High Slew-Rate Large Signal Response

Fig. 4.27 shows the DPUPS response to very high slew-rate large step transients. In Fig. 4.27a, the input voltage changes between 40 and 60V in 10 ns.



a. Regulation against input voltage variations (20V step with a slew-rate of 2000V/μs).



b. Regulation against the load variations (18A step with a slew-rate of 10000A/μs)

Fig. 4.27 Simulation results: responses to high slew-rate large-signal transients. Timing: 0.5 ms/div.

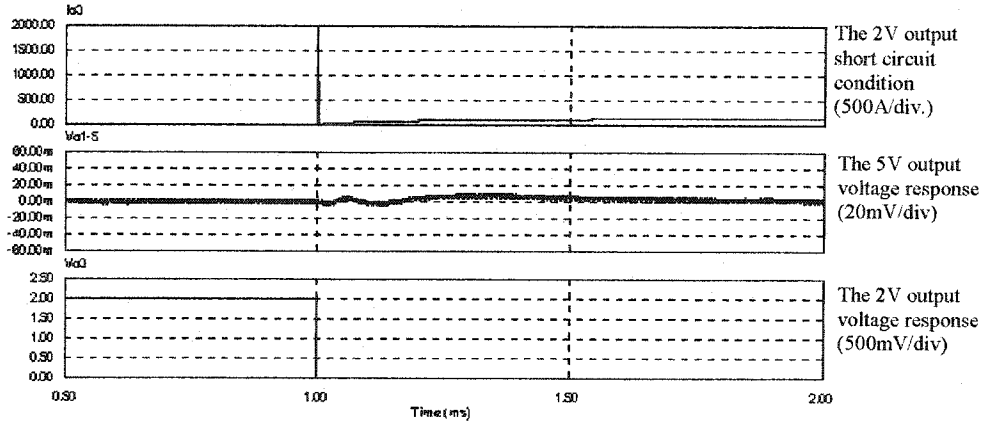


Fig. 4.28 Simulation results: responses to short circuit condition in the 2V output circuit. The time scale: 0.5 ms/div.

As seen in Fig. 4.27a, the two output voltages are hardly affected by this high slew-rate large signal input voltage transients, thanks to the voltage feed-forward control in the DPUPS.

Fig. 4.27b shows the output voltage responses to large step load transients of a slew rate of 10000 A/μs in the 2V output circuit. Large undershoot of the pertinent output voltage in response to upward step load is seen (namely the 2V output voltage). The large undershoot spike of about 120 mV is caused by the ESRs and ESLs of the output capacitor banks. The slower undershoot portion following the spike is because the output inductor becomes virtually an open circuit at such high slew-rate di/dt, and only the output capacitor provides total load current. Increasing the output capacitor seems able to improve such responses. However, when a fast start-up is required by the application, an excessively large output capacitor will result in a much slower startup, due to the longer charging of a bigger output capacitor. In such cases, increasing the switching frequency may be the solution to improve the DPUPS dynamic response.

Besides, the output response to a large downward step load is much faster than the response to the upward step load, and it just experience a little overshoot. This asymmetry in step load response shows the special dynamic property of the DPUPS.

The phenomena of the asymmetrical step load response is caused by the control scheme employed in the DPUPS. Contrary to a conventional power converter, the DPUPS main switch duty ratio is fixed for a given input voltage, and it does not react to load variations. The output regulation is achieved by modulating the simultaneous conduction interval of the SRs. The modulation is asymmetrical in the two opposite directions, namely it can reduce the effective duty ratio to zero, but not able to increase it

to the maximum due the limitation of the fixed duty ratio of S_{main}.

Consequently, in an event of a downward load step, the controlled SRs are able to reduce the effective duty ratio to the minimum such that the regulation will be recovered quickly. But when an upward load step comes, the SR stage cannot provide a large effective duty ratio to recover the regulation at the same speed as it does at the downward load step. Then undershoot voltage recovery will take a longer time, resulting asymmetrical response, as shown in Fig. 4.27b.

Above all, the DPUPS is stable under high slew-rate large signal transients.

Also seen from Fig. 4.27b is the hardly affected voltage in the other output, namely the 5V output voltage, thanks to the elimination of cross-regulation. Absolute elimination of the cross-regulation under dynamic conditions is not achievable, mainly because of the limited value of the voltage decoupling inductors that does not perform as a pure current source to achieve an ideal voltage decoupling between different outputs.

Fig. 4.28 shows the output responses to the short circuit condition in the 2V output. The short circuit of the 2V output happens instantly, and this creates a very high slew-rate large current spike. The other output (namely the 5V output) is hardly affected by this short circuit condition, thanks to the elimination of the cross-regulation.

4.7 CONCLUSIONS

The first DPUPS has been presented in this chapter. It is suitable for applications where all critical loads on-board can be collocated closely around the power supply. Steady state and small signal analyses of the proposed DPUPS architecture reveal its characteristics and properties, and a design procedure is generated. The concepts and design are verified experimentally and by simulation.

Major advantages of the proposed DPUPS architecture include the following:

(i) Single stage power conversion, hence to avoid additional conduction losses in the multi-stage converters.

(ii) Independent feedback control of each output voltage, hence realizing precise regulation of each output voltage.

(iii) Voltage decoupling among the outputs, therefore eliminating cross regulation.

(iv) Isolated multiple outputs, thus to facilitate power distribution.

(v) Dynamically stable under high slew-rate large signal transients.

(vi) Voltage feed-forward control of the main switch, thereby enabling instantaneous response in regulation of the output voltages against the input voltage variations.

(vii) Improved soft-switching and power transformer self-reset, which are already discussed in Chapter 2.

(viii) Soft switching of the synchronous rectifier, hence further improving the rectification efficiency.

(ix) Integrated power transformer to reduce the number of power magnetics.

However, as mentioned in Section 1.4, the DPUPS presented in this chapter is optimal for co-located on-board load applications. When several heavy loads are distributed at different places over the circuit board, this DPUPS is not an efficient solution to delivery the power to these multi-point loads. To cope with this problem, the other DPUPS shown in Fig. 1.9b must be implemented, and this leads to the study of the next chapter.

CHAPTER 5

IMPLEMENTATION OF DISTRIBUTED POINT-OF-USE POWER SUPPLY ARCHITECTURE EMPLOYING TYPE 2 CONVERTER

5.1 INTRODUCTION

The DPUPS architecture presented in last chapter has many advantages over the conventional ones, including the single-stage power conversion, independent and fine regulation of multiple outputs, reduced number of power components, etc. Therefore, it provides a promising solution to the circuit boards with critical loads collocated. However, it is not suitable for multi-point load applications in which several heavy and critical loads are distributed at different points of the circuit board.

As discussed previously in Section 1.3.4.1, there exist three approaches to distribute power to multi-point loads, which are (i) the use of single power supply module having master/slave multiple outputs, (ii) the use of multi-PUPS modules, and (iii) the use of pre-regulator-post-regulators. All these approaches have some major drawbacks.

Obviously, the DPUPS presented in the last chapter is similar to the first of the aforementioned approaches, namely the single power supply module approach. Thus, it will not overcome the following drawbacks when being applied to multi-point loads.

(i) Many layers of the PCB are used to carry the heavy currents, which reduces the number of available layers for tracking the high-speed signals.

(ii) Higher power losses on the long power tracks.

(iii) Deteriorated voltage regulation at the multi-point-of-use due to the stray impedance of long tracks.

The second DPUPS architecture presented in Fig.1.9b can be used to solve these problems. It distributes the power in the form of High Voltage and Low Current (HVLC), thus, it can greatly reduce the PCB copper requirements and conduction losses. Besides, it will greatly improve the supply voltage regulation at multi-points of use. This chapter discusses the implementation of such a DPUPS architecture using the Type 2 converter topology presented in Chapter 3.

The primary circuit of the second DPUPS will be the same as that of the Type 2 converter topology. Thus, the second DPUPS will retain such advantages as the improved soft switching and power transformer self-reset. Consequently, the steady state analysis of the primary circuit made in Chapter 3 is validly applicable to the second DPUPS. Therefore, this chapter only requires focusing on the secondary circuits to understand the second DPUPS performance and characteristics.

Similar to last chapter, the additional work to be performed on the second DPUPS include the discussion of the operating principle of multiple output regulation, the small signal analysis of dynamic properties, the development of a generic design procedure, and the proof-of-concepts by simulation and experiments.

The structure of this chapter is arranged in the following six sections. Section 5.2 presents the DPUPS implementation using the Type 2 converter topology. Steady state analysis of multiple output regulation is made in Section 5.3. Small signal analysis of this DPUPS is made in Section 5.4. A design procedure for this DPUPS is presented in Section 5.5. Simulation and experimental results are provided in Section 5.6 to verify the analysis and design. In Section 5.7, characteristics of this DPUPS architecture are summarized.

5.2 THE ARCHITECTURE IMPLEMENTATION AND OPERATING PRINCIPLE

5.2.1 Concepts of On-Board Power Distribution to Multi-Points Loads

Fig. 5.1 shows the conceptual implementation of DPUPS of Fig.1.9b for an example of two distantly located loads on a circuit board. It can be easily extended to power more points of loads just by paralleling additional secondary circuits in the same manner. The primary circuit of the second DPUPS is as simple as a single output Type 2 converter topology, hence it save many primary power component that otherwise could have to be employed in conventional power solutions.

Fig. 5.1 is electrically equivalent to two paralleled forward-type converters with their primary circuits integrated as one. It delivers the power from the dc bus to multi-point transformers in the form of HVLC pulses. The transformers and pertinent secondary circuits convert these pulses to the required low dc voltages. Since the secondary circuits are closely located to each of the multi-point load, the high current at regulated low dc voltage only travels a very short distance to reach the load. Therefore, the overall conduction losses along the PCB power distribution tracks are greatly reduced, and each load receives precisely regulated supply voltage.

5.2.2 DPUPS Implementation

Fig. 5.2 shows an implementation of Fig. 5.1 using the Type 2 topology. This DPUPS architecture consists of the following functional blocks: (i) the main switch S_{main}, (ii) a feed-forward control circuit controlling S_{main}, (iii) an auxiliary circuit that is described in Chapter 3 to achieve ZVS of S_{main} and self-reset of the power transformers, and (iv) multiple output sub-circuits.

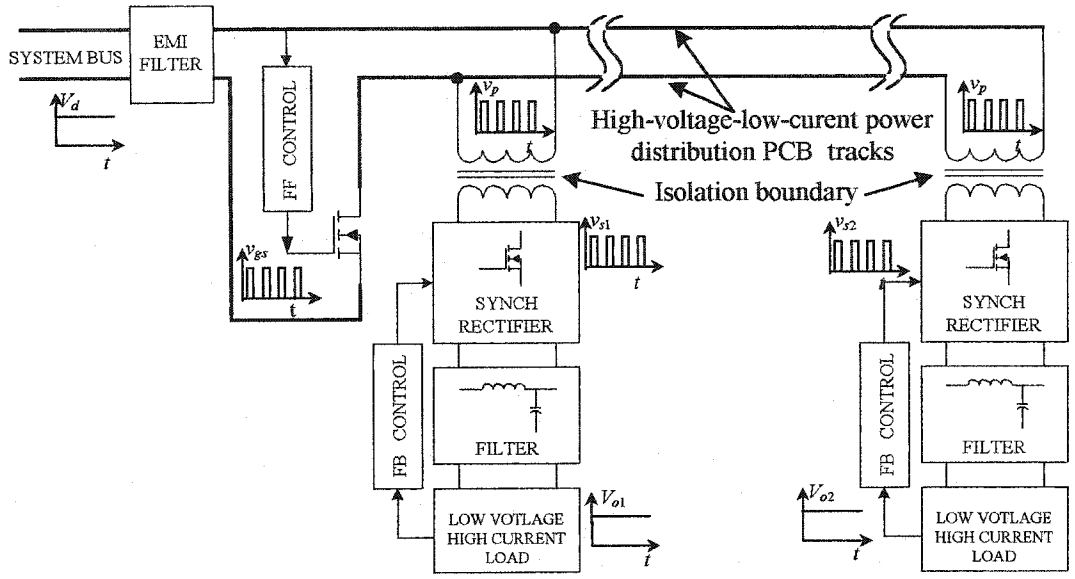


Fig. 5.1 Conceptual implementation of the DPUPS suitable for multi-point load applications.

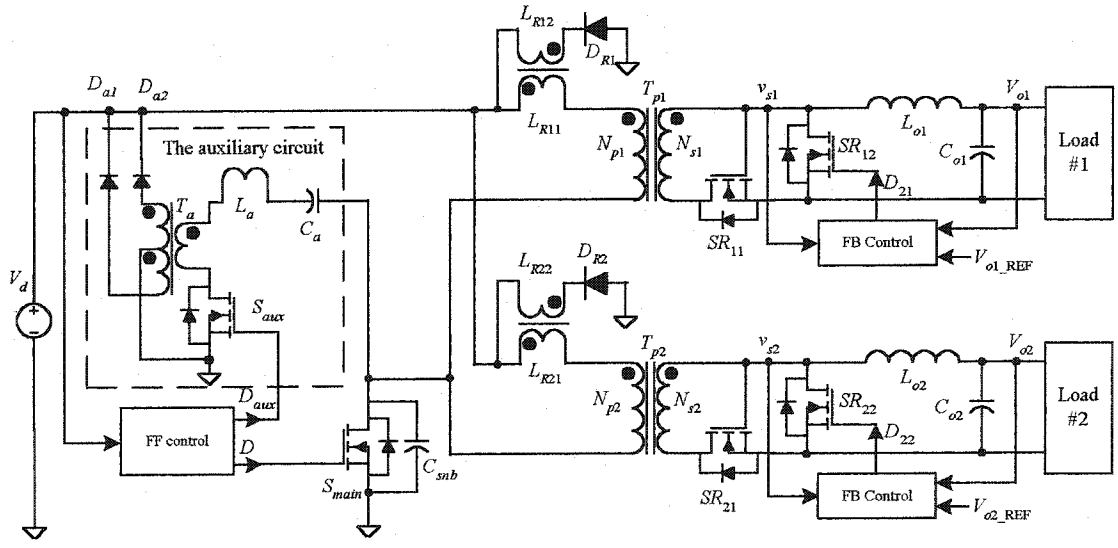


Fig. 5.2 A two-output DPUPS implementation using the Type 2 converter topology.

All output sub-circuits have identical structures. For the arbitrary j^{th} output, where j =1 or 2 in the case of Fig. 5.2, it consists of (i) a dedicated power transformer T_{pj} exclusive for the j^{th} output, (ii) two SR MOSFETs, SR_{j1} and SR_{j2}, (iii) an output filter comprised of L_{oj} and C_{oj}, (iv) two coupled inductors L_{Rj1} and L_{Rj2}, (v) a blocking diode D_{Rj}, and (iv) a dedicated feedback control circuit producing PWM signal to control the shunt SR, namely SR_{j2}.

The coupled inductors L_{Rj1} and L_{Rj2} limit the current during SR simultaneous conduction interval, decouple the short circuit conditions of the pertinent output circuit from the other one, and recover the stored energy in their core.

5.2.3 Operating Principle

The primary circuit operates in almost the same way as described in Chapter 3 to achieve ZVS and self-reset of the power transformers. In addition, the voltage-feed-forward control circuit generates the PWM signal for S_{main} in such a way that unidirectional pulses of constant volt-second-product are produced in the primary circuit. Therefore, the DPUPS can achieve instantaneous output voltage regulation against variations of the dc bus voltage.

The unidirectional voltage pulse train has a high level of the dc bus voltage V_d. It carries the power in the HVLC form, and travels along HVLC PCB tracks to individual power transformers that can be closely located to each of the critical multi-point loads. Thus, the conduction losses along the distribution paths will be greatly reduced, and precise and tight voltage regulation at the points of load can be obtained.

The individual power transformer converts the power to LVHC pulses. On its secondary side, each pair SRs acts as a chopper that chops these voltage pulses. The

pertinent feedback circuit modulates the chopping interval, or the pair SRs simultaneous conduction interval, to obtain the output regulation against load variations.

The simultaneous conduction interval of SRs creates a short-circuit condition. However, the current limiting inductor L_{Rj1} limits the current rise, and this also decouples this short-circuit condition from the other output circuit. Therefore, the cross-regulation between different outputs is eliminated. When the main switch is turned OFF, the coupled inductors in each output circuit returns the stored energy to the input dc bus via D_{Rj} and L_{Rj2}.

5.2.4 Advantageous Features

Clearly, this DPUPS has the following advantageous features in contrast to the conventional approaches:

(i) Efficient on-board power distribution to multi-point loads.

(ii) Precise voltage regulation at multi-point loads.

(iii) Single stage power conversion, hence to avoid additional conduction losses in the multi-stage converters.

(iv) Independent feedback control of each output voltage, hence realizing precise regulation of each output voltage.

(v) Voltage decoupling among the outputs, therefore eliminating cross regulation.

(vi) Isolated multiple outputs, thus to facilitate power distribution.

(vii) No need of the feedback loop crossing the isolation boundary between the input and output, thereby permitting complete and reliable isolation and also allowing for high bandwidth design due to the elimination of such slow devices as the opto-coupler in the control loop of the conventional topologies.

(viii) Voltage feed-forward control of the main switch, thereby enabling instantaneous regulation of the output voltages against the input voltage variations.

(ix) Improved soft-switching and power transformer self-reset that are already discussed in Chapter 3.

(x) Above all, the most significant advantage is its HVLC onboard power distribution to multi-point loads.

5.3 STEADY STATE ANALYSIS

This architecture is based on the Type 2 converter topology, and the steady state analysis in Chapter 3 validly applies to the primary circuit of the DPUPS for ZVS and transformer self-reset. This chapter will focus on the secondary circuits to understand the function of multiple output regulation.

The following assumptions are made to perform the analysis for the arbitrary j^{th} output circuit, where j= 1 or 2 in the case of having two outputs.

(i) The input and output dc voltages are at constant values, V_d and V_{oj}, respectively.

(ii) The load draws constant output current, I_{oj}.

(iii) The feed-forward control circuit generates the gating pattern for S_{main} with a duty ratio (pulse-width) of D.

(iv) The switching frequency is f_{sw}.

(v) The output circuit is in CCM.

(vi) The components have linear properties.

(vii) The leakage inductance of T_{pj} is treated as a part of L_{Rj1}.

(viii) L_{Rj1} and L_{Rj2} have equal inductance, and they are ideally coupled.

(ix) Each pair L_{oj} and C_{oj} makes an ideal output filter.

Fig. 5.3 shows steady state key waveforms of a two-output DPUPS as shown in Fig. 5.2. The definition of the intervals are similar to that of Chapter 3. An additional interval 5aj (between t_{4a1} to t_5 for the 1st output, or between t_{4a2} and t_5 for the 2nd output circuit) is introduced, which is the interval during which the pair SRs conduct simultaneously. However, each output circuit only sees six modes, because it cannot distinguish among Intervals 1 through 3, and between Intervals 4 and 5.

Seen from the secondary side, S_{main} and S_{aux} are logically OR-ed to let the primary current flow. For the convenience of performing the analysis on the secondary circuit, S_{aux} is assumed to be a part of S_{main}.

S_{main} has only two states, ON and OFF. The first three modes happen during S_{main} is ON, and the rest three during S_{main} is OFF. Fig. 5.4 shows the active current paths in the five distinguishable modes for the arbitrary j^{th} output circuit. The duration of each mode is expressed as a fraction of a switching period.

5.3.1 Main Switch ON (Duty-ratio D)

When S_{main} is ON, the circuit goes through the following three Modes.

5.3.1.1 Mode 1 (Intervals 1 through 3, both SR_{j1} and SR_{j2} conduct.)

In this Interval, S_{main} is on, and both SR_{j1} and SR_{j2} conduct. Fig. 5.4a shows the active current paths in this mode. L_{Rj1} starts to see the input dc voltage V_d. Thus, the primary and secondary currents are determined by:

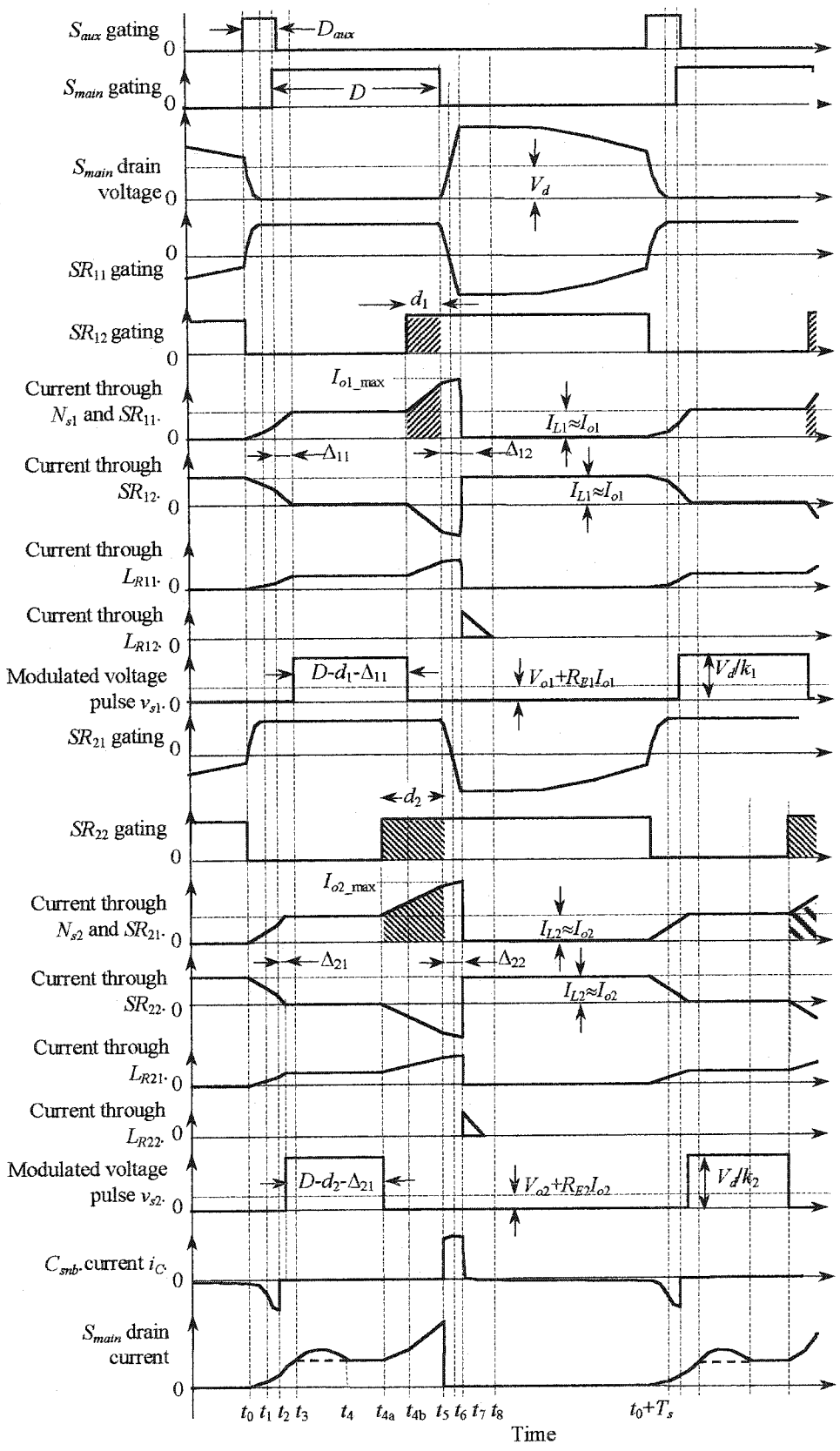
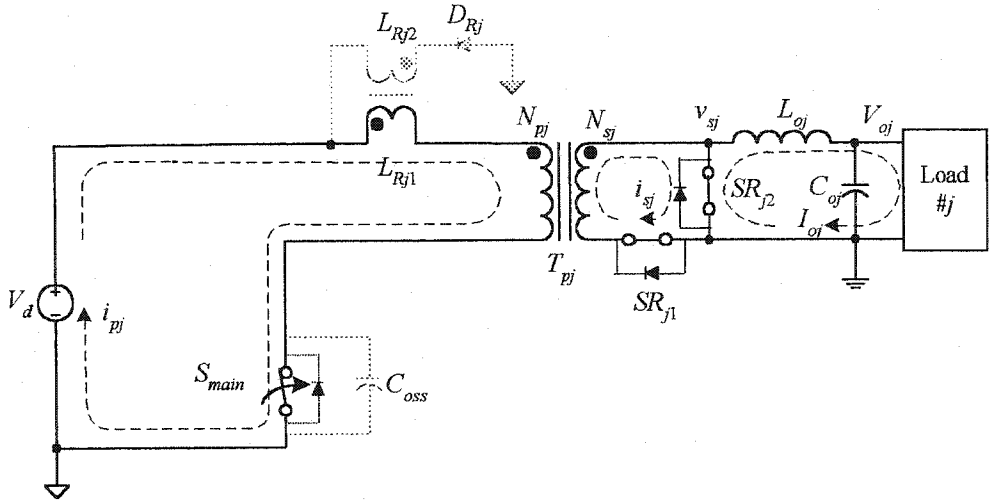
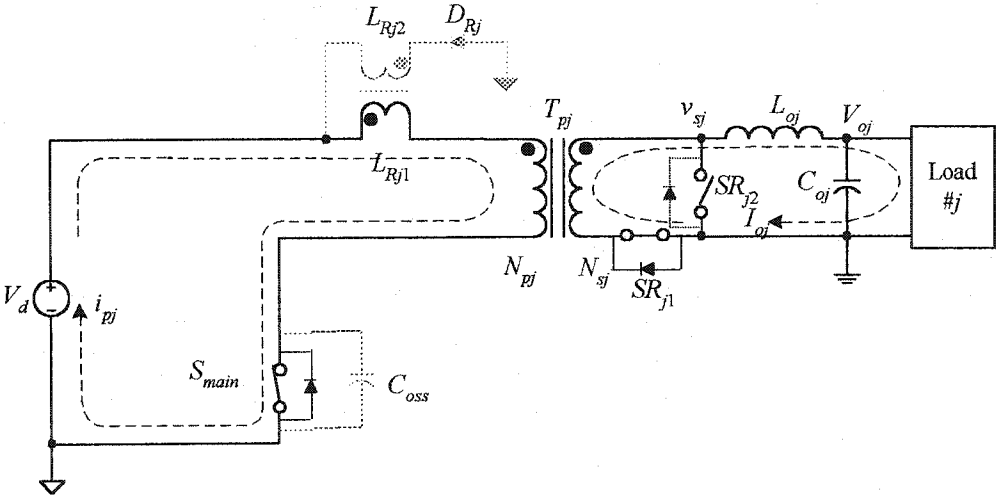


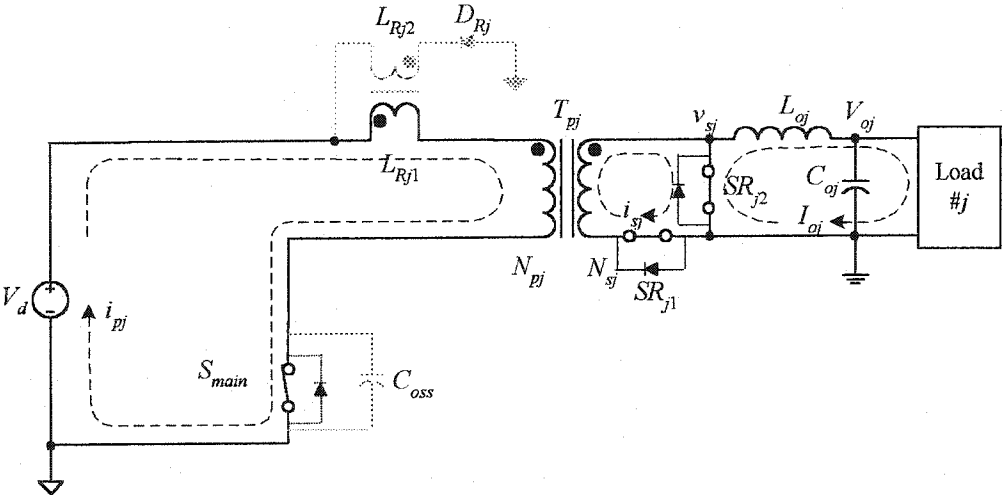
Fig. 5.3 Key waveforms of a two output DPUPS of Fig. 5.2.



a. Mode 1 (Intervals 1 through 3, total duration approximately $\Delta_{1j}=f_s L_{Rj1} I_{oj}/k_j V_d$).

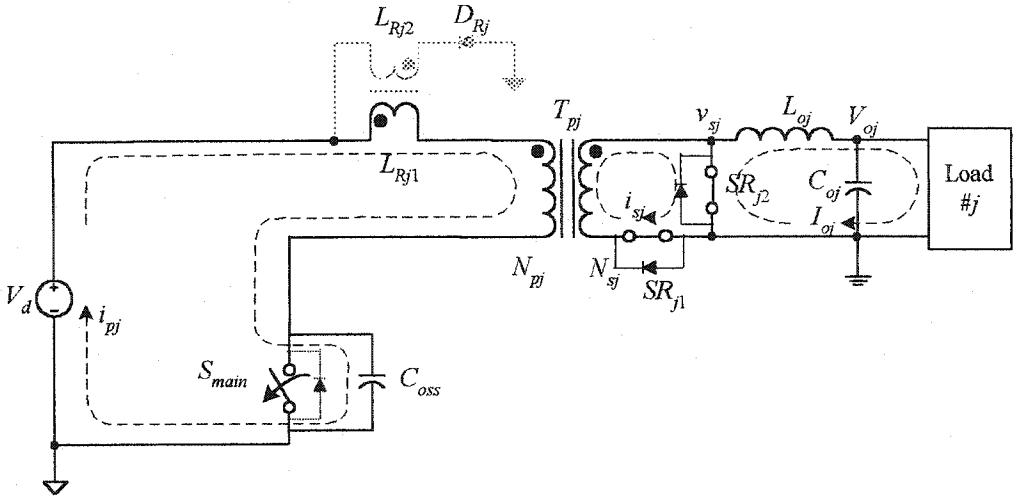


b. Mode 2 (Intervals 4 and 5, total duration $D-\Delta_{1j}-d_j$).

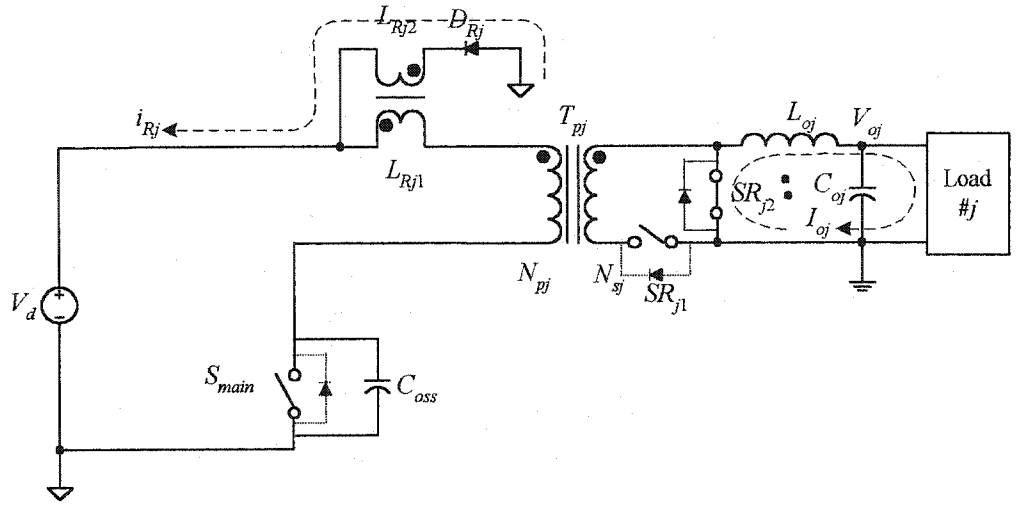


c. Mode 3 (Interval 5a, duration d_j).

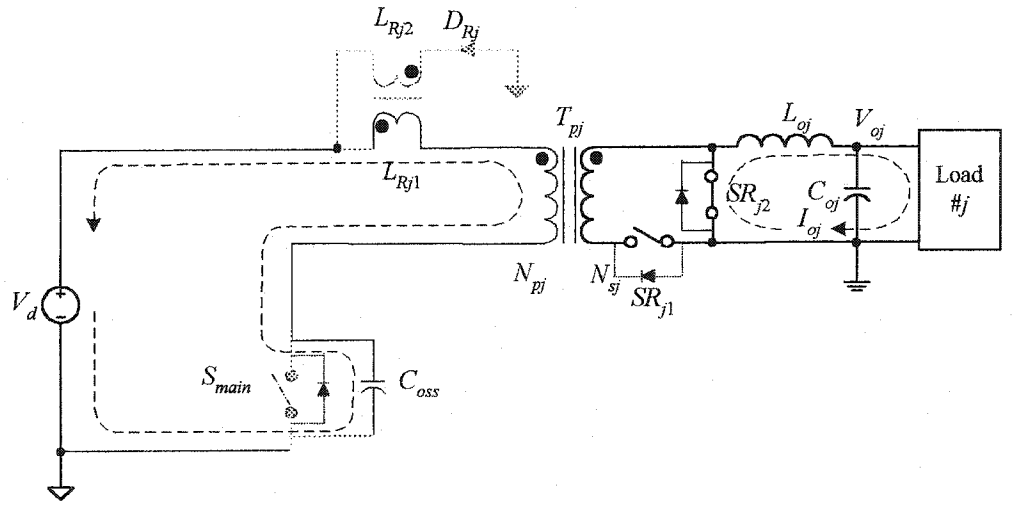
Fig. 5.4 Active current paths in the six modes of the arbitrary j^{th} output circuit (*To be continued on the next page*).



d. Mode 4 (Interval 6 and 7, total duration: Δ_{2j}).



e. Mode 5 (Interval 8, duration: Δ_{3j}).



f. Mode 6 (Interval 9, duration 1-D-Δ_{2j}-Δ_{3j}).

Fig. 5.4 (*Continued from last page*) Active current paths in the six steady state intervals of the arbitrary j^{th} output circuit.

$$i_{sj}(t) = k_j \int \frac{V_d - u_{d1}(t)}{L_{Rj1}} dt \tag{5-1}$$

where u_{d1} is determined by (3-4), or V_d, depending on the actual interval, and k_j is the turns ratio of T_{Pj}'s primary winding to the secondary winding, namely

$$k_j = N_{pj} / N_{sj} \tag{5-2}$$

Because the current through the output inductor L_{oj} is almost constant, the body diodes of both SR_{j1} and SR_{j2} are forced to conduct before i_{sj} reaches the magnitude of I_{oj}. Therefore, the secondary voltage v_{sj} is simply zero.

The duration of this mode, namely (t_3-t_0), can be found in the analysis made in Chapter 3. Since Interval 1 is usually very short, a linear approximation of the total duration of Mode 1, expressed in a fraction of a switching cycle, can be obtained by the following equation,

$$\Delta_{1j} = (t_3 - t_0) f_{sw} \approx \frac{f_{sw} L_{Rj1}}{k_j V_d} I_{oj} \tag{5-3}$$

5.3.1.2 Mode 2 (Intervals 4 and 5, SR_{j1} conducts but SR_{j2} does not.)

In this mode, the total output inductor current now flows through SR_{j1}, and the power is transferred from the input to the load in the same way as in a conventional forward converter. Fig. 5.4b shows the active current paths in this mode.

Since L_{oj} is so great that it can be considered as a dc current source, i_s constant now as governed by

$$i_{sj}(t) = I_{oj} \tag{5-4}$$

Consequently, the voltage v_{sj2} is constant as given by

$$v_{sj2}(t) = \frac{1}{k_j} V_d \tag{5-5}$$

This mode terminates when SR_{j2} is turned ON by the feedback circuit at some time ahead of the end of the ON state of S_{main} in order to regulate the output voltage. The duration of this mode is determine by

$$f_{sw}(t_{4a} - t_3) = D - d_j - \Delta_{1j} \tag{5-6}$$

5.3.1.3 Mode 3 (Interval 5aj, both SR_{j1} and SR_{j2} conduct.)

In this mode, SR_{j2} is turned ON ahead of the end of D by an interval of duration d_j. Because SR_{j1} is still ON, both SRs now conducts simultaneously, and this creates a short-circuit. Modulating the duration of this mode will regulate the output voltage. Fig. 5.4c shows the active current paths in this mode.

This short-circuit condition chops off the excessive portion the voltage pulses produced by the primary circuit, and in this way the output voltage is regulated. Hence, the effective pulse width, or effective duty-ratio, is determined by the following equation:

$$D_{eff\_j} = D - d_j - \Delta_{1j} \tag{5-7}$$

Thanks to the inductor L_{Rj1}, this short-circuit condition is voltage-decoupled from the input dc bus. Consequently, the voltages cross the other power transformer do not collapse, and cross-regulation between different outputs is eliminated.

Now, the total input voltage again falls across L_{Rj1}, and the secondary current starts to rise again as governed by

$$i_{sj}(t) = \frac{k_j V_d}{L_{Rj1}}(t - t_{4aj}) + I_{oj} \tag{5-8}$$

This mode is terminated by turning off the main switch. The duration of this mode is d_j that will be determined below in Section 5.3.4. At the end of this mode, i_{sj} reaches a value given by

$$I_{sj} = \frac{d_j k_j V_d}{f_s L_{Rj1}} + I_{oj} \tag{5-9}$$

5.3.2 Main Switch OFF

5.3.2.1 Mode 4 (Intervals 6 and 7, both SR_{j1} and SR_{j2} conduct.)

In this mode, S_{main} is turned OFF, but both SR_{j1} and SR_{j2} conduct. Fig. 5.4d shows the active current paths in this mode.

The duration of this mode is the total duration of Intervals 6 and 7, which are given in (2-36) and (3-19).

5.3.2.2 Mode 5 (Interval 8, SR_{j2} conducts but SR_{j1} does not.)

In this mode, D_{Rj} is forced to conduct to release the stored energy in the couppled inductors. SR_{j2} is in freewheeling of the total output inductor current. Fig. 5.4e shows the active current paths in this mode. The duration of this mode is determined by (3-29).

5.3.2.3 Mode 6 (Interval 9, SR_{j2} conducts but SR_{j1} does not.)

In this mode, SR_{j2} is in freewheeling of the total output inductor current. Fig. 5.4f shows the active current paths in this mode. The duration of this mode is $(1\text{-}D\text{-}\Delta_{2j}\text{-}\Delta_{3j})$.

5.3.3 Validity of the Linear Approximations

5.3.3.1 Validation of the linear approximation of Δ_{1j}

Linear approximation of the duration of the Mode 1 in the above analysis is made to facilitate the small signal analysis in Section 5.4.1 by using averaged state space method. However, it is important to justify these approximations.

Fig. 5.5 shows the comparison between the linear approximation of Δ_{1j} given in (5-3), and the accurate value of Δ_{1j}, namely $(t_3\text{-}t_0)$, which is obtained by solving numerically the equations given in Section 3.4.1

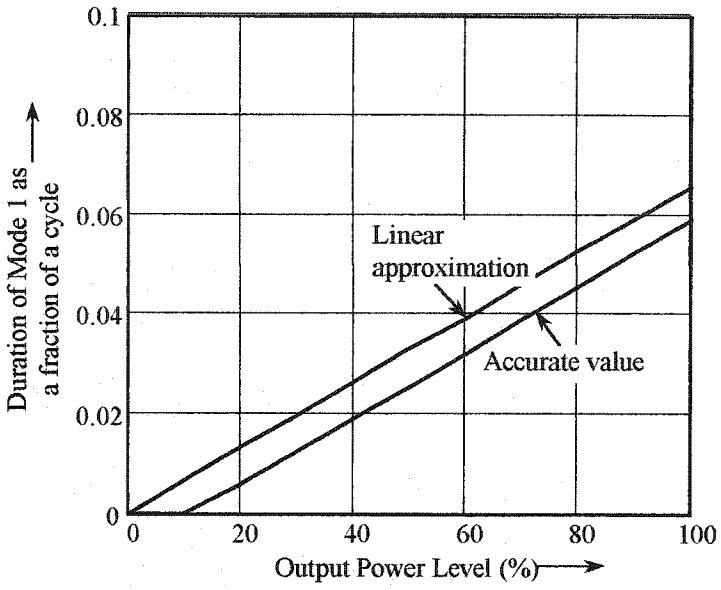


Fig. 5.5 Comparison of the approximation and accurate duration Δ_{1j}.

Over the entire load range of the prototype circuit of Section 4.7, the curve of the accurate value is always smaller. It is because the accurate value takes into account the small rise of the secondary current during Interval 1, which was neglected by the approximation. However, (5-3) introduces only a little deviation of less than 1% of a switching cycle. Thus, it can be used as a satisfactory approximation.

5.3.4 Steady State Characteristics

5.3.4.1 Modulation of SR Simultaneous Conduction Interval

Similar to Section 4.3.4, the arbitrary j^{th} output circuit can be represented by

$$V_{oj} = V_{Thj} - R_{Ej} I_{oj} \tag{5-10}$$

where V_j and R_{Ej} are the Thevenin equivalent source voltage and resistance, respectively. V_{Thj} is the averaged voltage of v_{sj}, and it is easily found to be

$$V_{Thj} = \frac{V_d}{k_j}(D - d_j - \Delta_{1j}) \tag{5-11}$$

where S_{main} duty ratio D is found to be as follows

$$D \geq \max_{j=1,2}\left(\frac{k_j}{V_d}[V_{oj}+(R_{Ej}+f_{sw}\frac{L_{Rj1}}{k_j^2})I_{oj\_\max}]\right)$$
$$=\frac{k_j}{V_d}[V_{oj}+(R_{Ej}+f_{sw}\frac{L_{Rj1}}{k_j^2})I_{oj\_\max}]+d_{mj} \quad (5\text{-}12)$$

where d_{mj} is the margin of S_{main} duty ratio seen by the j^{th} output circuit at full load. Then, solving from (5-3), (5-10), (5-11) and (5-12), the modulation of the simultaneous conduction interval d_j can be found as follows.

$$d_j = d_{mj}+\frac{k_j}{V_d}[V_{oj}+(R_{Ej}+f_{sw}\frac{L_{Rj1}}{k_j^2})](I_{oj\_\max}-I_{oj}) \quad (5\text{-}13)$$

An optimal design in practice is to make d_{mj} be zero or very close to zero. Thus, all d_j will be minimized to reduce the conduction losses arising from the SR simultaneous conduction interval.

Fig. 5.6 shows d_j as a function of the circuit parameters in the two-output prototype DPUPS. Assume d_{mj} for the 2V-20A output circuit is zero, while it is about 0.02 for the 5V-5A output circuit.

It indicates that the short-circuit interval can be limited below 6% of a switching cycle, when R_{Ej} is kept below 5 mΩ for the 2V output circuit and 20 mΩ for the 5V output circuit. This can be achieved by using very low $R_{ds(ON)}$ MOSFET devices for S_{main} and SRs and by optimizing the magnetics and the circuit layout.

5.3.4.2 RMS Current through the SRs

Fig. 5.7 shows the rms current in the SRs as a function of the circuit parameters in the 2V output circuit of the prototype DPUPS. These curves show that the rms current, or the conduction losses, can be limited by reducing R_{Ej} and increasing the current limiting inductor. However, L_{Rj} shall not be too large to limit the reduction of effective duty ratio.

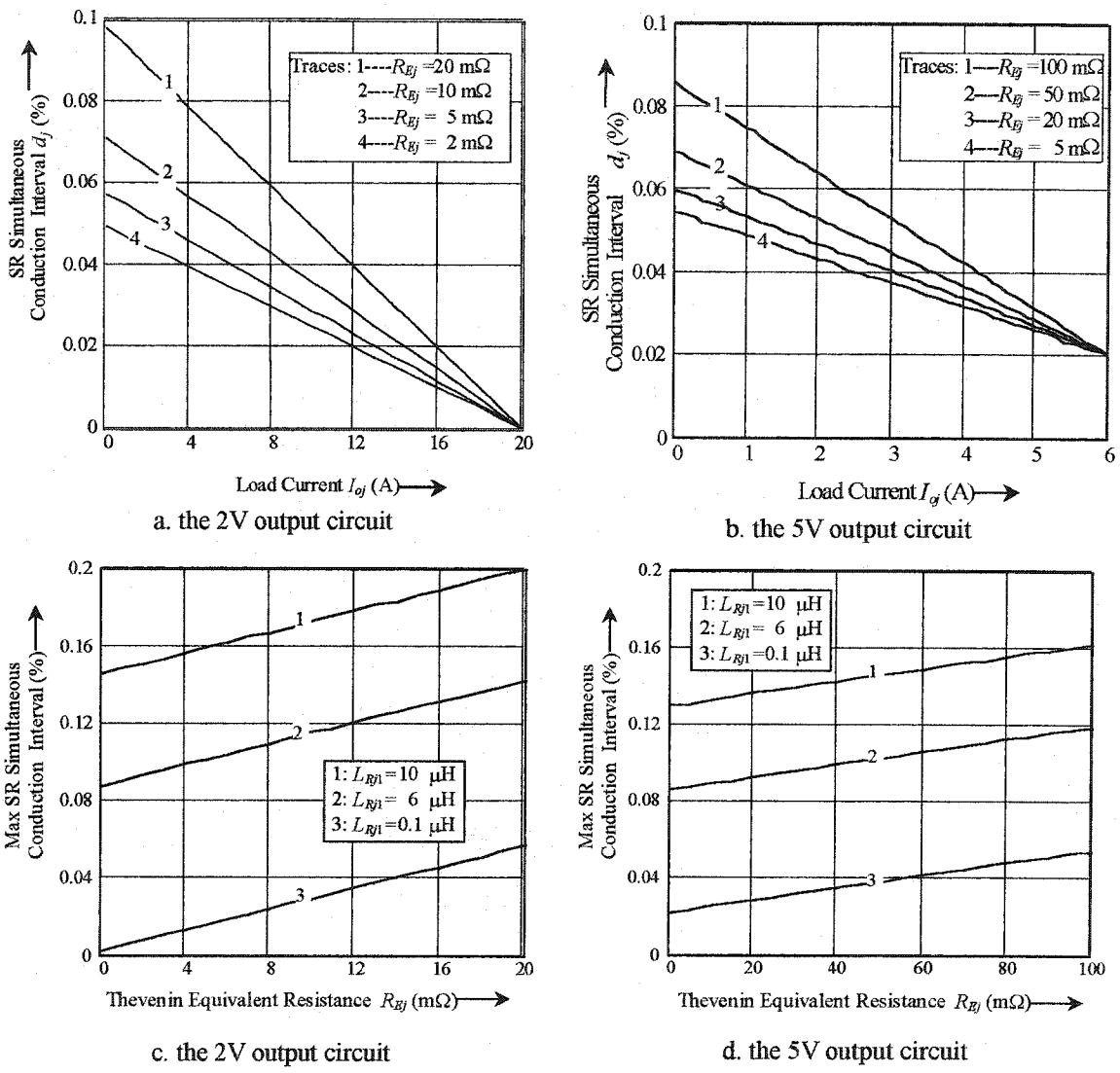
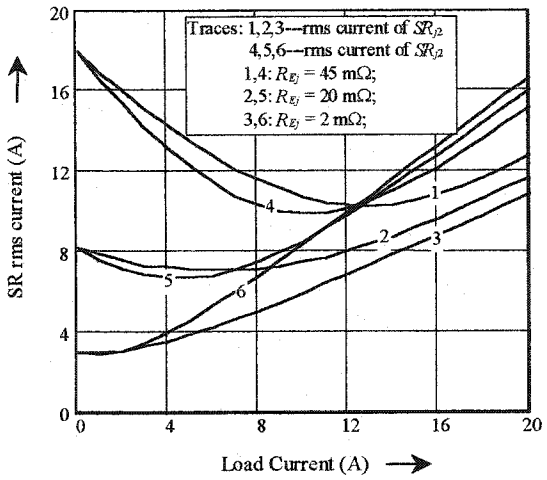
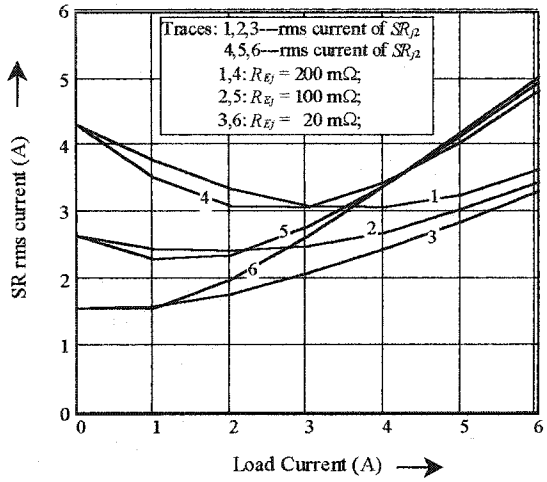


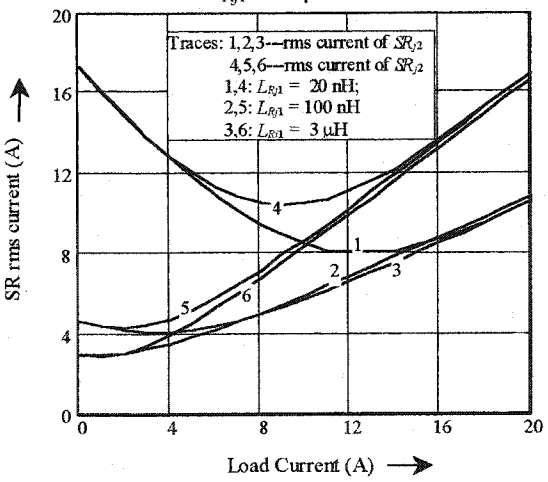
Fig. 5.6 The simultaneous conduction interval of the pair SRs vs. the load condition and Thevenin equivalent source resistance in the 2V output of the prototype circuit. P_o=0 to 40 W, f_{sw}=300kHz.



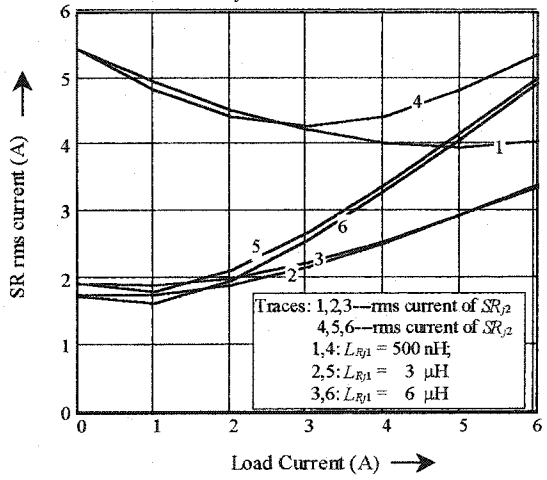
a. The SR rms currents of the 2V output circuit. L_{Rj1}=3.0 μH.



b. The SR rms currents of the 5V output circuit. L_{Rj1}=3.0 μH.



c. RMS current vs. load current and the current limiting inductor. R_{Ej}=2 mΩ.



d. RMS current vs. load current and the current limiting inductor. R_{Ej}=50 mΩ.

Fig. 5.7 The rms currents through the SRs of the prototype circuit as functions of circuit parameters. V_d=55V, f_{sw}=300kHz.

5.3.4.3 Effects of the Multiple Output Circuit on Primary Circuit

The total current of the main switch is the sum of the primary currents of all output circuits plus the auxiliary circuit current. The peak value of S_{main}'s drain current is determined by

$$I_{d\max} = \sum_j \left(\frac{d_j V_d}{f_{sw} L_{Rj1}} + \frac{I_{oj}}{k_j}\right) \tag{5-14}$$

Substituting (5-12) into (5-14), the maximum drain current of S_{main} is determined by:

$$I_{d\max} = \sum_j \left(\frac{R_{Ej} + f_{sw}\dfrac{L_{R1j}}{k_j^2}}{f_{sw}\dfrac{L_{R1j}}{k_j^2}} \cdot \frac{I_{oj\max}}{k_j} + \frac{V_{d\max}}{f_{sw} L_{R1j}} d_{mj} \right) \tag{5-15}$$

5.3.4.4 Effects of the Multiple Output Circuit on the Self-Rreset Power Transformer

Comparing the DPUPS of this chapter and the Type 2 topology of Chapter 3, a basic difference is that there is an SR simultaneous conduction interval (Interval 5aj) in the DPUPS. Owing to this simultaneous conduction interval, as indicated in (5-15), the peak drain current of S_{main} will not change in the DPUPS, regardless the load condition. This peak current determines the peak drain voltage of S_{main}, and will always cause the Interval 7 to end up with the first case, whatever the load is at the maximum, minimum, or intermediate. This also makes the duration of Intervals 7, 8 and 9 constant, which means the constant magnitude in the flux backward swing to reset the power transformer. Consequently, contrary to the Type 2 topology, the flux swing range will not vary with load in the DPUPS, although it still varies with other parameters. This brings another advantage, namely the worry that the self reset transformer might saturate under light or no load conditions is no longer an issue for the DPUPS.

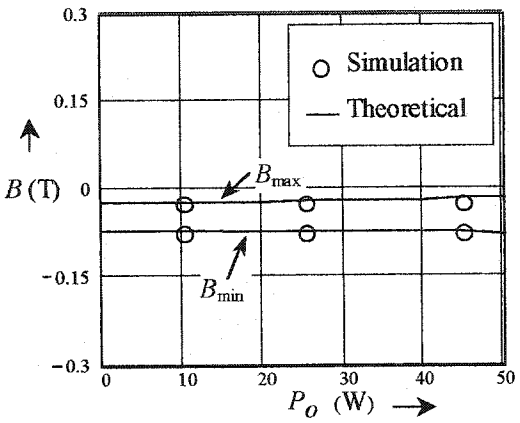


Fig. 5.8 Power transformer flux excursion vs. load in the DPUPS. The two- output load varies at the same scale from zero to full load.

The calculation of the flux excursion in the DPUPS is provided in Part II of the spreadsheet of Appendix F. Fig. 5.8 shows a typical curves of the flux excursion under variable load conditions. The simulation results are also presented to verify the theoretical analysis. Because the flux excursion is independent of the load conditions, the flux excursion curves at full load like the ones in Fig. 3.13a,c,g,i need to be referred only in design.

***5.3.4.5** Soft Switching of the SRs*

Referring to Fig. 5.3 and Fig. 5.4, it can be confirmed that the pair SRs automatically achieves soft switching. For the front SR, namely SR_{f1}, its inherent drain-to-source capacitor has already been discharged by the secondary current in Interval 1. Thus, when the self-driven gating signal goes to high at the beginning of Interval 2, SR_{f1} achieves a ZVS turn-on.

For the same reasons as mentioned in Section 4.3.4.5, SR_{f1} automatically achieves a ZVS turn-off, and SR_{f2} automatically achieves a ZCS turn-on and ZVS turn-off.

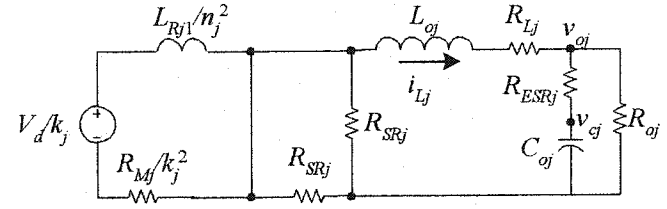
5.4 SMALL SIGNAL ANALYSIS

5.4.1 Small Signal Model

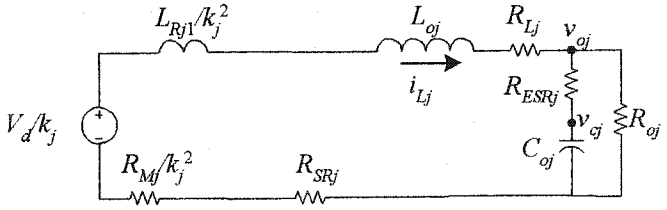
Observe Fig. 5.4, one can find that the active current paths are the same for Modes 1,3 and 4, and the same for both Modes 5 and 6. Thus, the six modes can be represented with three equivalent circuits, which are shown in Fig. 5.9.

In these equivalent circuits, the following parasite parameters are also included in order to obtain a more accurate model:

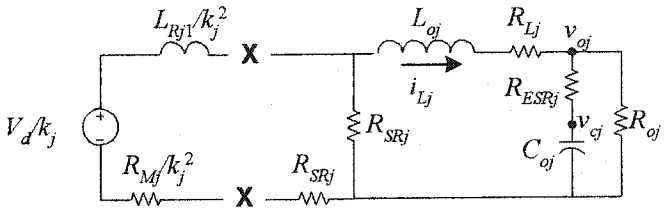
(i) R_{Lj}: the equivalent resistance of the output inductor.



a. Modes 1, 3 and 4. Total duration: $\Delta_{1j}+ d_j +\Delta_{2j}$.



b. Mode 2. Duration: D-Δ_{1j} -d_j.



c. Modes 5 and 6. Duration: 1-D-Δ_{2j}

Fig. 5.9 Three equivalent circuits of the six modes in the j^{th} output circuit (j=1 or 2 in the two-output example).

(ii) R_M: the total effective resistance of the primary circuit including S_{main} Rds(ON), dc resistance of T_{pj}, dc resistance of the PCB tracks that the power flow takes, etc.

(iii) R_{SRj}: the Rds(ON) of the SRs.

(iv) R_{ESRj}, the ESR of the output capacitor bank.

(v) L_{Rj1}: the current limiting inductor also including the leakage of T_p.

Based on the equivalent circuits, one can obtain the averaged state space model of the j^{th} output circuit as follows (See Appendix D):

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = -[R_{SRj} + R_{Lj} + (D - d_j - \Delta_{1j})\dfrac{R_M}{k_j^2}]i_{Lj} + (D - d_j - \Delta_{j1})\dfrac{V_d}{k_j} - v_{oj} \\ R_{ESRj}C_{oj}\dfrac{dv_{oj}}{dt} = -v_{cj} + v_{oj} \\ R_{oj}C_{oj}\dfrac{dv_{cj}}{dt} = R_{oj}i_{Lj} - v_{oj} \end{cases} \tag{5-16}$$

Similarly, the dc model of the j^{th} output circuit is

$$\begin{cases} V_{oj} = (D - d_j - \Delta_{j1})\dfrac{V_d}{k_j} - \left[R_{SRj} + R_{Lj} + (D - d_j - \Delta_{1j})\dfrac{R_M}{k_j^2}\right]I_{oj} \\ V_{cj} = V_{oj} \\ V_{oj} = R_{oj}I_{oj} \end{cases} \tag{5-17}$$

Comparing (5-17) with (5-10), it is obvious that Thevenin equivalents of the j^{th} output circuit are determined by

$$R_{Ej} = R_{SRj} + R_{Lj} + (D - d_j - \Delta_{1j})\frac{R_{Mj}}{k_j^2} \tag{5-18}$$

$$V_j = \frac{V_d}{k_j}(D - d_j - \Delta_{1j}) \tag{5-19}$$

Equation (5-19) confirms with (5-11).

Considering small perturbations and ignoring higher order terms, one can obtain from (5-16) the j^{th} output circuit transfer function from the control signal (namely d_j, or the simultaneous conduction interval of the pair SRs) to the output voltage as the following:

$$\frac{\hat{v}_{oj}(s)}{\hat{d}_j(s)} = \frac{-(\frac{V_d}{k_j} - \frac{R_M V_{oj}}{k_j^2 R_{oj}})(1+sR_{jESR}C_{oj})}{s^2 L_{oj}C_{oj}(1+\frac{R_{jESR}}{R_{oj}}) + s\left\{\frac{L_{oj}}{R_{oj}} + C_{oj}\left[R_{jESR}(1+\frac{f_{sw}L_{Rj1}}{k_j^2 R_{oj}}) + R_{Ej}(1+\frac{R_M}{k_j^2 R_{oj}})\right]\right\} + (1+\frac{R_M + f_{sw}L_{Rj1}}{k_j^2 R_{oj}})} \tag{5-20}$$

Comparing (4-27) and (5-20), one can easily find the intrinsic difference between the two DPUPSs. In the DPUPS of this chapter, there is no RHP zero in the power circuit transfer function, and this makes the power circuit an ordinary buck-type circuit. According to [72-74,111], the compensation to such a system is straightforward, and the Type-II Error Amplifier can be applied to close the loop.

Usually, all internal resistances are much smaller than the load resistance, thus, (5-20) can be simplified to the following transfer function:

$$\frac{\hat{v}_{oj}}{\hat{d}_j} = -\frac{(\frac{V_d}{k_j} - \frac{R_M V_{oj}}{k_j^2 R_{oj}})(sR_{ESRj}C_{oj}+1)}{s^2 L_{oj}C_{oj} + s\left[\frac{L_{oj}}{R_{oj}} + (R_{Ej}+R_{ESRj})C_{oj}\right] + 1} \tag{5-21}$$

5.4.2 Model Verification

To verify the model, the breadboard prototype DPUPS is used. Details of this prototype are given in Table 5.2 in Section 5.6. Fig. 5.10 shows the theoretical Bode Plot of the 2V output circuit of the prototype DPUPS from the output of the error amplifier to the 2V output terminal. Fig. 5.11 shows the measured results.

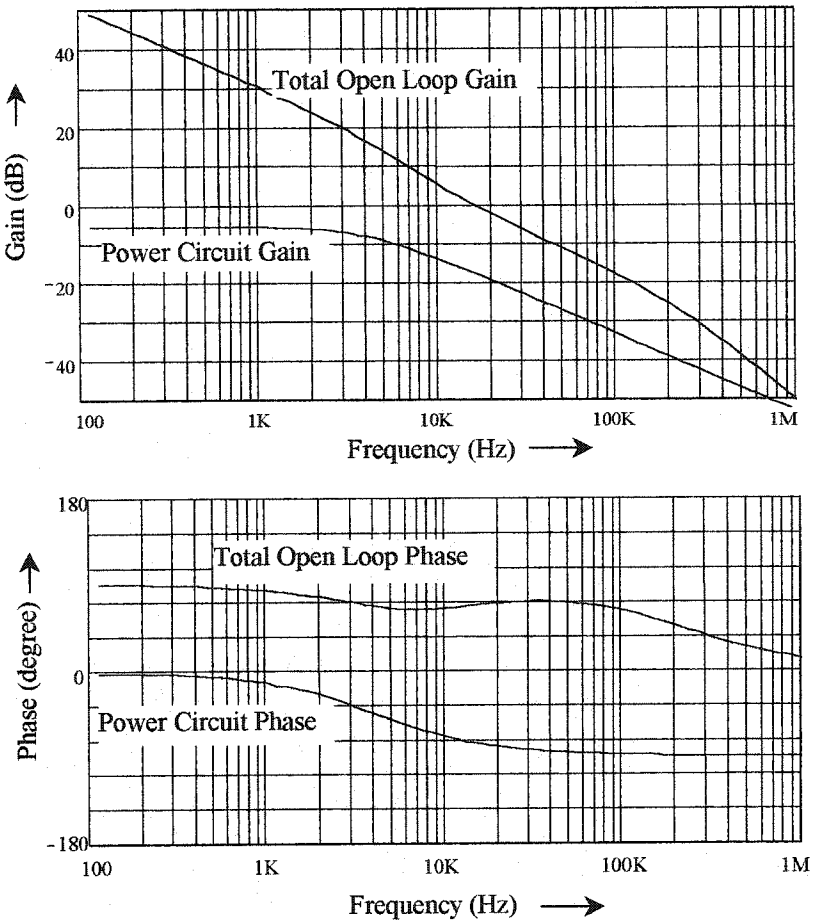


Fig. 5.10 Theoretical predicted Bode Plot of the power circuit and total open loop.

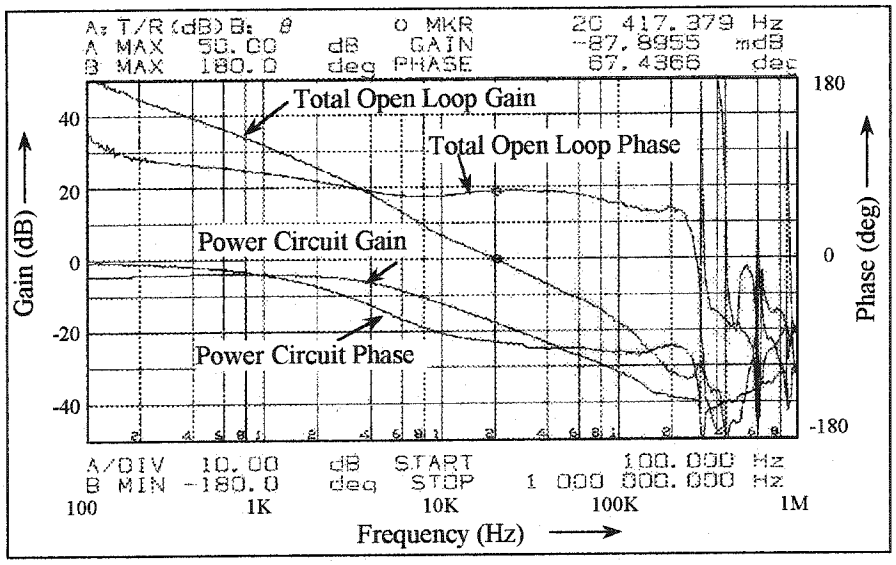


Fig. 5.11 Measured transfer functions of the power circuit and total open loop. V_d=50V. f_{sw}=300kHz. Output Current=12A.

Table 5.1 compares the predicted and tested power circuit gain and phase at different frequencies. They have a good agreement, both in the gain and phase over the frequency range up to 100kHz (maximum gain error less than 3dB and maximum phase error less than 10^{o}). The little differences are caused by the approximation in the model that ignores some insignificant and negligible factors, and they are also caused by test errors including the instrument calibration tolerance and reading errors.

Table 5.1 Power Circuit Transfer Function Verification

Frequency	Gain (dB)			Phase (degree)		
	Predicted	Tested	Error	Predicted	Tested	Error
1k	-6.3	-4.1	-2.2	-13	-14	+1
2 kHz	-6.8	-4.3	-2.5	-24	-28	+4
4 kHz	-8.6	-6.1	-2.5	-43	-44	+1
10 kHz	-14.2	-12.3	-1.9	-78	-73	-5
20 kHz	-19.8	-18.0	-1.8	-84	-82	-2
60 kHz	-29.3	-27.5	-1.8	-86	-90	+4
100 kHz	-33.7	-31.8	-1.9	-87	-95	+8

5.5 DESIGN PROCEDURE AND CONTROL IMPLEMENTATION

The analyses show that the Types 1 and 2 topologies have many similarities in circuitry, performance and characteristics, and so do the two DPUPS topologies. Therefore, the some design criteria of the first DPUPS in last chapter can be applied to design the second DPUPS of this chapter. Above all, the design shall also refer to the flux excursion range using the spreadsheet of Appendix F, to guarantee the successful self-reset of the power transformer.

Assume that the following principal parameters are already determined for a particular application:

(i) f_{sw}—switching frequency,

(ii) L_m—magnetizing inductance of T_p,

(iii) V_{oj}—output voltage,

(iv) I_{oj}—full load current, and

(v) $V_{d\min}$ and $V_{d\max}$—the minimum and maximum input voltage, respectively.

(vi) η_{rect}—the target efficiency in the rectification stage at full load.

5.5.1 Selection of Principal Components and Parameters

Selections of the following components and parameters are the same as discussed in Chapter 4, and they are not repeated here:

(i) Selection of D_{max}, the maximum duty ratio: see Section 4.5.1.1.

(ii) Selection of D_{aux}, the auxiliary switch duty ratio: see Section 4.5.1.2.

(iii) Selection of the synchronous rectifiers SRs: see Section 4.5.1.4.

(iv) Selection of of the snubber capacitor C_{snb}: see Section 4.5.1.5. However, the peak

drain current to be handled by C_{snb} is now determined by (5-15), instead.

(v) Selection of the resonant tank L_a-C_a: See Section 4.5.1.7. However, the total equivalent current limiting inductance L_s is now determined by the following, instead:

$$L_s = \frac{1}{\sum_j \frac{1}{L_{Rj1}}} \tag{5-22}$$

(vi) Selection of the main switch S_{main} is the same as given in Section 4.5.1.8.

(vii) Selection of the auxiliary transformer T_a: see Section 4.5.1.9.

(viii) Selection of the auxiliary switch S_{aux}: see Section 4.5.1.10. However, the voltage rating is now given by $2V_d$ and peak current to be handled by S_{aux} is now determined by (3-7).

(ix) Selection of the auxiliary rectifier diodes D_{a1}, D_{a2}: see Section 4.5.1.11.

(x) Design of the output filter can follow the conventional design to meet the specified requirements of output ripples for a particular application.

Selection of other power components shall observe the following criteria.

5.5.1.1 The j^{th} Transformer Turns Ratio k_j:

The approach of Section 4.5.1.3 can be used herein to determine the turns ratio of the j^{th} power transformer:

$$k_j = \frac{N_{pj}}{N_{sj}} =\leq \frac{V_{d\min}}{V_{oj} + (1-\eta_{rect})V_{oj}}(D_{\max} - 0.05) \tag{5-23}$$

Similarly, selection of the power transformer core and magnetizing inductance can follow the conventional design procedure.

5.5.1.2 Current Limiting Inductor L_{Rj1}

Seen from (5-3) and (5-11), L_{Rj1} reduces S_{main} effective duty-ratio by the amount of Δ_{j1}. Thus, L_{Rj1} shall not be too big in order to avoid excessive duty-ratio reduction, otherwise a larger output inductor must be employed to meet the output ripples specifications. On the other hand, as seen from (5-9), (5-15) and Fig. 5.7c and d, L_{Rj1} should not be too small, or excessive current would be resulted during the SR simultaneous conduction interval. Therefore, a reasonable tradeoff is to set Δ_{j1} between 0.05 and 0.1 and also to limit the peak current in the SR simultaneous conduction interval such that it is not more than two times of the maximum load current. Thus, from (5-9) and (5-15), the following condition shall be satisfied in the selection of L_{Rj1}.

$$L_{Rj1} \le \frac{k_j V_{d\min}}{f_{sw} I_{oj\max}} \Delta_{1j} \tag{5-24}$$

$$L_{Rj1} > \frac{k_j^2 R_{Ej}}{f_{sw}} \approx \frac{2k_j^2 R_{SRj}}{f_{sw}} \tag{5-25}$$

It is important to point out that L_{Rj1} must be prevented from saturation, otherwise it would lose the voltage decoupling function and failure of whole circuit could happen.

5.5.1.3 Coupled Inductor L_{Rj2}

For the coupled inductor L_{Rj2}, it is recommended to be equal to L_{Rj1}. When it is greater, S_{main} will suffer from voltage stress higher than $2V_d$, as given in (3-21). This will bring two problems. First, C_{snb} will be charged to a higher voltage, and this requires a higher current to discharge it at the beginning of the next cycle, and thus causes more conduction losses in the auxiliary circuit. Second, a higher voltage rating MOSFET may have to be used. Because a higher voltage MOSFET usually also has a higher Rds(ON), this will increase the conduction losses in the main switch.

On the other hand, when L_{Rf2} is selected smaller than L_{Rf1}, C_{snb} will be charged to a lower voltage. This applies a lower negative voltage pulse to the power transformer during the resetting process. One possible consequence is that it may not be sufficient to achieve the volt-second balance to reset the transformer, owing to the limited resetting time by large duty-ratio of S_{main} at low input voltage. Another possibility is that the transformer can be reset but at the sacrifice of using a smaller duty-ratio, and the drawback is that a larger output filter must be used to achieve the output ripple specifications.

In conclusion, L_{Rf2}, shall be selected equal to L_{Rf1}. The coupled inductors shall be wound with bifilar technique to obtain a better coupling. However, the winding of L_{Rf2} can use a much thinner wire due to the smaller current involved as given in (3-27).

5.5.1.4 Blocking Diodes D_{Rj}

It shall be a fast recovery diode. As seen in the Section 5.3.1, its voltage rating shall be $2V_d$, and its peak current rating is determined by (5-9).

5.5.2 Implementations of Control

The feed-forward and feedback control circuits are the same as discussed in Section 4.5.2 and Section 4.5.3.

5.6 EXPERIMENTAL AND SIMULATION RESULTS

A two-outputs prototype DPUPS has been built to prove the concept of the second proposed DPUPS. Its two outputs are 2V 12A, and 5V 5A and the switching frequency is 300kHz. The principal parameters and operating conditions are listed in Table 5.2.

5.6.1 Experimental Results

5.6.1.1 Key Waveforms

Fig. 5.12 shows the main switch gating signal in response to the input voltage step change. The pulse-width of the main switch gating signal is adjusted immediately by the feed-forward circuit to react against the input step change. This verifies the concept and design of the feed-forward control circuit.

Table 5.2 Principal Components of the Prototype DPUPS

Components	**Values/Selections**	
	2V circuit	**5V circuit**
S_{main}	IRF640, two in parallel	
L_{R1j}/L_{R2j}	6μH/6μH	6μH/6μH
k_j	15:2	12:4
$T_{pj\ Core}$	PQ26/20-3F3, Custom gap	PQ26/20-3F3, Custom gap
SR_{j1}, SR_{j2}	MTP75N05	IRFZ44
L_{oj}	3.6μH	24μH
C_{oj} Bank	68μF Tantanlum +482.2μF Electrolytes	68μF Tantanlum +102.2μF Electrolytes
Maximum Load	15 A	5A
L_a/C_a	2μH/66nF (Ceramic)	
S_{aux}	IRF634	
C_{snb}	12nF (Ceramic)	
D_{a1}, D_{a2}	HFA08TB	
D_{Ri},	HFA08TB	HFA08TB

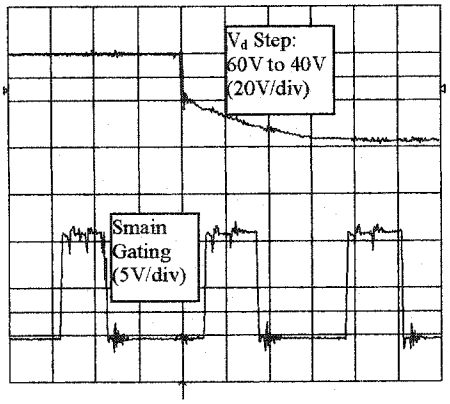


Fig. 5.12 Main switch duty ratio in response to input voltage change. (Timing: 1μs/div).

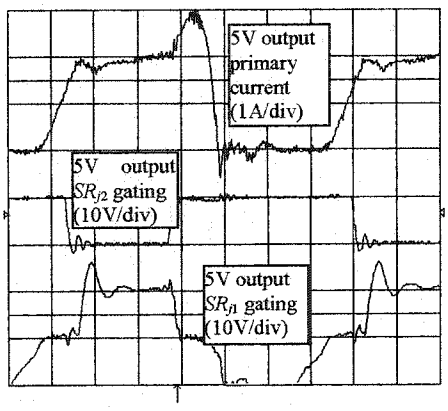


Fig. 5.13 The primary current in the 5V output circuit and the gating of the SRs. V_d=55V, I_o=5A. (Timing 0.5μs/div)

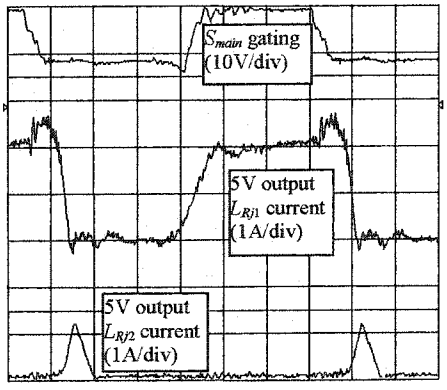


Fig. 5.14 Current through the current limiting coupled inductors. (Timing: 0.5μs/div.)

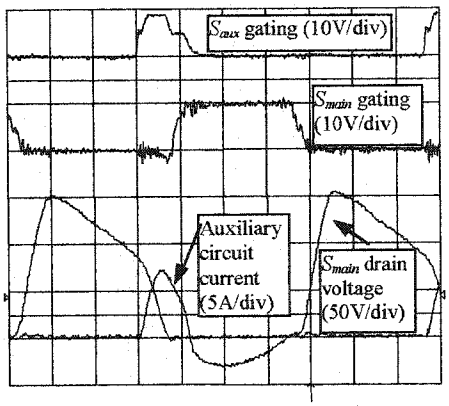


Fig. 5.15 Soft switching of the main switch. Operating conditions: V_d=50V and the loads are 5A @ 5V and 12A @ 2V. (Timing: 0.5μs/div.)

Fig. 5.13 shows the primary current of the 5V output and the gating of the pair SRs. The simultaneous conduction of the pair SRs is not apparent. It is because the front SR (namely SR_{f1}) of the prototype DPUPS is self-driven by a power transformer winding. As soon as the shunt SR (namely SR_{f2}) is turned on, the short circuit condition will cause the gate signal for the front SR to become zero. The body diode then conducts instead. However, the short circuit condition is implied on the current trace. The bump at the end the current pulse indicates the simultaneous conduction interval. The current waveform verifies the concept and analysis made in this chapter.

Fig. 5.14 shows the waveforms of the current through the coupled current limiting inductors. The flowing of the current through coupled inductor (L_{Rf2}) indicates the recovery of the stored energy in the coupled inductors after S_{main} is turned off. This verifies the concept and design of the DPUPS.

Fig. 5.15 shows the soft switching of the main switch by employing the resonant auxiliary circuit. The drain current of the main switch is not shown here mainly due to the difficulty of inserting a long wire loop to accommodate the current probe. However, it is

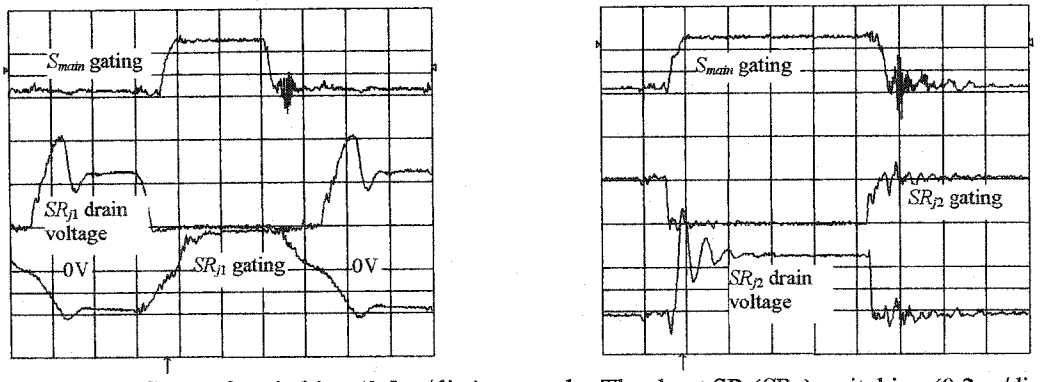
seen clearly that zero voltage switching is achieved in S_{main} at both turn-on and turn-off, because S_{main} drain voltage has already decreased to zero before the gate signal comes and it starts to rise only after the gate signal has already dropped below the 4V threshold. The auxiliary switch achieves soft switch at both turn-on and turn-off. It is because the auxiliary current starts gradually from zero after S_{aux} is turned on, and before the auxiliary switch is turned off while the drain voltage stays at zero. Main switch drain voltage is higher than $2V_d$ is due to the leakage inductance of the non-optimized power transformers used in the prototype.

Fig. 5.16 shows soft switching of the 5V output circuit SRs. Similar waveforms are observed on the 2V circuit SRs. The spike on the front edge of the drain voltage pulses is caused by the resonance between the transformer leakage and the SR MOSFET inherent drain-to-source capacitor.

By observing the timing of SR gating signals and drain voltage waveforms, one can easily confirm that the front SR (namely SR_{f1}) achieves ZVS at both turn-on and turn-off, and the shunt SR (namely SR_{f2}) achieves a ZVS turn-off. Although hardly seen from Fig. 5.16b, the shunt SR achieves a ZCS turn-on, due to the current limitation by L_{sf}. This verifies the discussion made in Section 5.3.4.4.

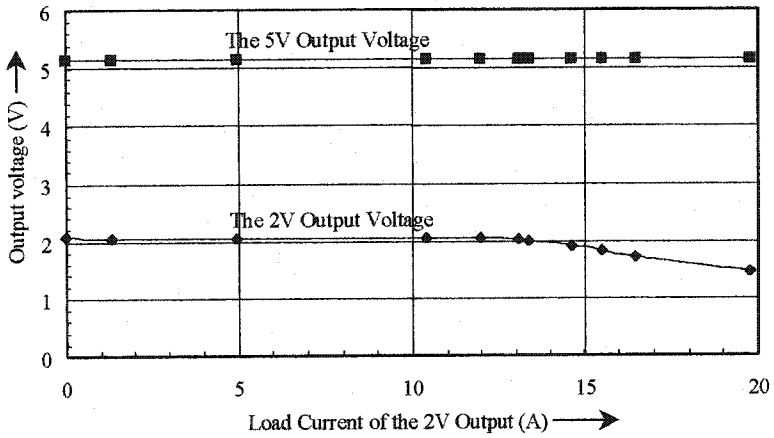
5.6.1.2 Regulation and Cross-Regulation

Fig. 5.17 shows the output voltage regulation against the load currents. The voltage regulation of one output is totally independent of the load condition of the other output, indicating the elimination of cross-regulation in the second DPUPS. Similar reasons as mentioned in Section 4.6.1.2 can explain the loss of regulation of the relevant output at very large load current.

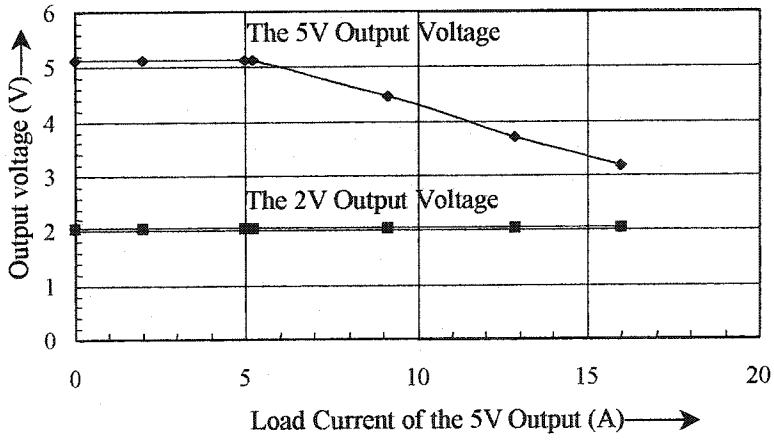


a. The front SR (SR_{f1}) soft switching (0.5μs/div.). b. The shunt SR (SR_{f2}) switching (0.2μs/div.).

Fig. 5.16 Soft switching of the 5V output circuit synchronous rectifiers. Vertical scale for all traces: 10V/div.



a. Output voltages vs. the 2V output current. The 5V output current is at 5A constant.



b. Output voltages vs. the 5V output current. The 2V output current is at 10A constant.

Fig. 5.17 Experimental results of output regulation and cross regulation vs. load. The cross-regulation is eliminated between the two outputs.

Also obtainable from Fig. 5.17 is the output resistor of each output circuit, which gives 83.4mΩ for the 2V output and 168mΩ for the 5V output, and it reflects the losses on all parts along the secondary current paths, including the SRs, output filters, decoupling inductors, transformer windings, and the circuit tracks. These output resistors are much higher than the SRs Rds(ON) (see Table 5.2). The reasons are the poor layout of the breadboard circuit, lack-of copper on the power tracks, and non-optimized magnetics. This also explains the lower-than-expected efficiency shown below.

5.6.1.3 Step Responses

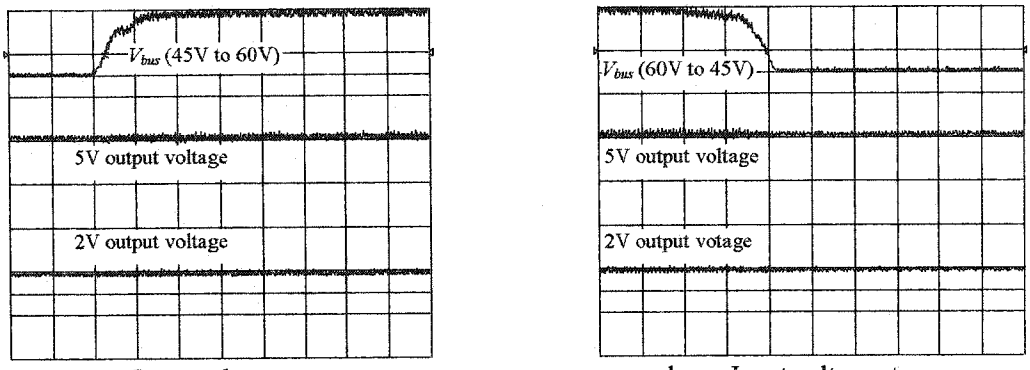
Fig. 5.18 shows the prototype DPUPS responses to the input dc voltage step changes. The output voltage is nearly immune to the disturbance in the input voltage, and this verifies the instantaneous regulation against the input with the feed-forward control.

Fig. 5.19 show the prototype DPUPS responses to load step changes. The load step changes in one output circuit hardly affects the other output voltage, experimentally proving the independent regulation of each output and the elimination of cross-regulation.

5.6.1.4 Efficiency

Fig. 5.20 shows the overall efficiency of the prototype DPUPS. Seen from Fig. 5.20a, as the function of input voltage, the overall efficiency under full load condition is almost constant over the input voltage range, with a slight drop at both ends. It is because at the minimum input voltage, the conduction losses are higher due to the increased rms current for a given output power.

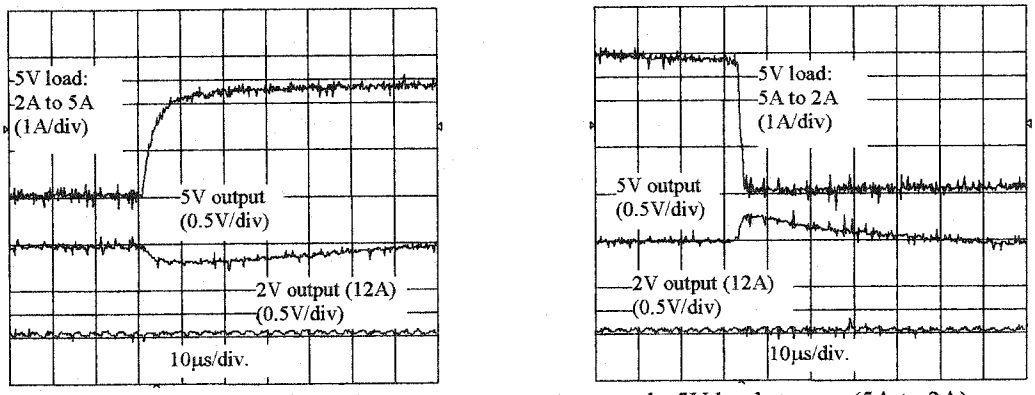
At the higher end of the input voltage, the snubber capacitor will be charged to a higher level and this needs a higher current to discharge for the ZVS operation, and the high discharging current increases the conduction losses.



a. Input voltage step up

b. . Input voltage step up

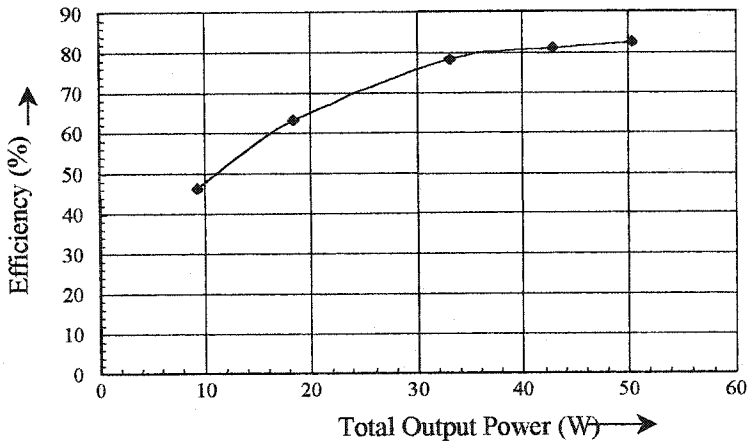
Fig. 5.18 Output voltages versus input step changes. (Timing: 0.1ms/div.)



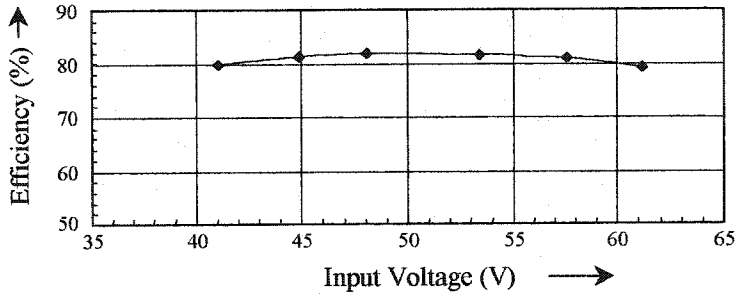
a. 5V load step up (2A to 5A).

b. 5V load step up (5A to 2A).

Fig. 5.19 Output regulation versus step load.



a. Efficiency vs. load at input voltage of 48V



b. Efficiency vs. input voltage at full load

Fig. 5.20 Overall efficiency of the prototype DPUPS.

In addition, since SR_{j1} is self-driven by a transformer winding, the gate-drive losses will increase with the input voltage owing to a higher gate drive voltage applied to the SR gate. At medium input voltage, each type of losses is not excessive, and thus the efficiency is the highest.

As a function of load, as seen in Fig. 5.20b, the efficiency stays almost constant over the range from 100% to 70% of the full power, and it drops as the output power decreases further. This is because when the loads decrease from the full power, the conduction losses also decrease, therefore the overall efficiency can be kept almost constant. However, as the power decreases further, the simultaneous conduction interval d_j of the pair SRs in each output circuit becomes greater, as indicated by (5-13). Then, the conduction losses arising from the increased d_j become more significant, and hence the

overall efficiency falls more and more rapidly as the output power decreases.

The prototype DPUPS only yields a maximum efficiency of about 82% at full load. The lower than expected efficiency confirms with the excessive output resistance implied in Fig. 5.17. However, this efficiency can be improved if better MOSFETs such as future products can be used for the switches and SRs, if optimized magnetics are employed, and if the circuit can be built on a neat PCB.

5.6.2 Simulation Results

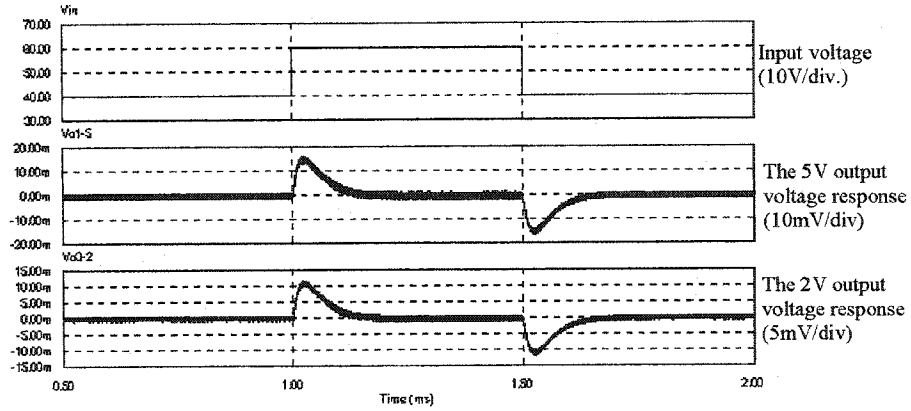
For the same reasons as mentioned in Section 4.6.2, simulation is used to investigate the second DPUPS dynamic properties under high slew-rate and large signal transients. The Psim models to simulation the DPUPSs are presented in Appendix H.

5.6.2.1 Regulation and Cross-Rregulation under Dynamic Conditions

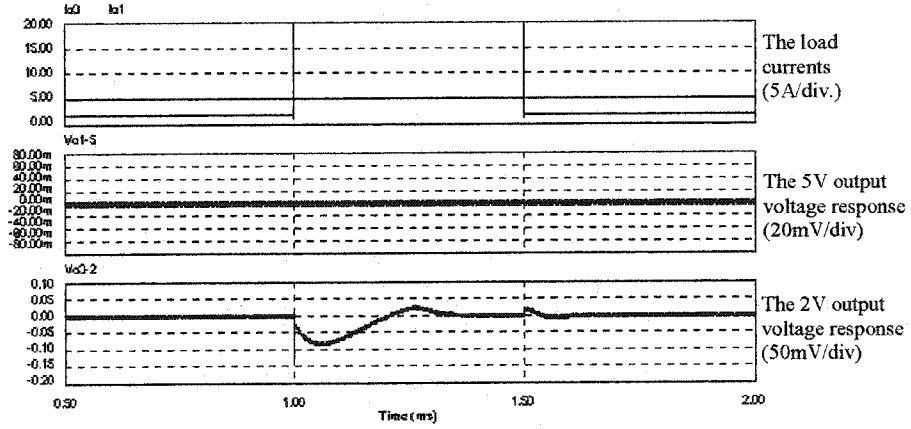
Fig. 5.21 shows the DPUPS response to very high slew-rate step transients. In Fig. 5.21a, the input voltage changes between 40 and 60V in steps of zero rise and fall times of 10ns. Due to the feed-forward control of the main switch, the overshoot and under shoot of the two output voltages are well limited under these high slew-rate transients.

Fig. 5.21b shows the output voltage responses to high slew-rate (10000A/μs) large signal step load transients in the 2V output circuit. It is seen that the step load transients in the 2V output circuit hardly affect the output regulation of the 5V output, thanks to the elimination of the cross-regulation between different outputs.

Fig. 5.21b also shows that the PDUPS has asymmetrical responses to the step load transients. The reasons for this asymmetrical step-load response can also be explained as previously discussed in Section 4.6.2.1.



a. Regulation against input voltage variations (20V step with a slew-rate of 1000V/μs)



b. Regulation against the load variations (2V output load step with a slew-rate of 10000A/μs)

Fig. 5.21 Simulation results: output regulation against input and load variations. Only the voltage deviations are shown. Timing: 0.5 ms/div.

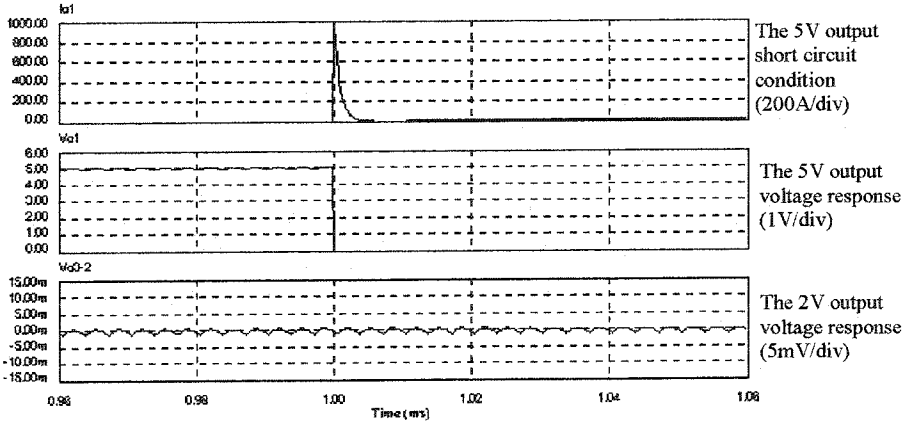


Fig. 5.22 Simulation results: responses to short circuit condition in the 2V output circuit. The time scale: 20 μs/div.

Fig. 5.22 shows the output responses to the short circuit condition in one of the two outputs. The short circuit of the 5V output happens instantly, and this creates a very high slew-rate large current spike. The other output (namely the 2V output) is hardly affected by this short circuit condition in the 5V output, thanks to the elimination of the cross-regulation.

Above all, the second DPUPS is stable under high slew-rate large signal transients both in the input and load.

5.7 CONCLUSIONS

The second DPUPS has been presented in this chapter. It is suitable for multi-point load applications where a few critical loads are distributed at different locations of the PCB board. Steady state and small signal analyses of the proposed architecture reveal its characteristics and properties, and a design procedure is generated. The concepts and design are verified experimentally and by simulation.

Major advantages of the proposed DPUPS include the following:

(i) HVLC efficient on-board power distribution to multi-point loads.

(ii) Precise voltage regulation at multi-point loads.

(iii) Single stage power conversion, hence to avoid additional conduction losses in the multi-stage converters.

(iv) Voltage decoupling among the outputs, therefore eliminating cross regulation.

(v) Isolated multiple outputs, thus to facilitate power distribution.

(vi) No need of the feedback loop crossing the isolation boundary between the input and output, thereby permitting complete and reliable isolation and also allowing for high bandwidth design due to the elimination of such slow devices as the opto-

coupler in the control loop of the conventional topologies.

(vii) Voltage feed-forward control of the main switch, thereby enabling instant response in regulation of the output voltages against the input voltage variations.

(viii) Improved soft-switching and power transformer self-reset.

(ix) The DPUPS is dynamically stable under very high slew-rate large signal transients.

Therefore, the second DPUPS complements the first one such that these two DPUPSs together provide optimal power solutions to different types of on-board power distribution of advanced telecom systems.

CHAPTER 6

CONCLUSIONS

6.1 SUMMARY

The objective of this thesis is to find cost-effective and efficient solutions to meet the power requirements of new generation low-voltage semiconductor circuits in advanced telecom systems. For this purpose, two distributed point-of-use power supply (DPUPS) architectures are presented in this thesis. These two DPUPS architectures are basically soft switched single-stage converters with independently regulated multiple outputs, and they can overcome the drawbacks of conventional on-board power distribution architectures.

This thesis can be summarized as follows. Chapter 1 performs the background study and defines the topic of the thesis work. The power requirements of new generation low-voltage semiconductor circuit boards in advanced telecom systems include very low operating voltage and high load current, tight regulation of multiple voltages, multi-point loads on-board, high efficiency, high power density, and low costs. The conventional power distribution architectures, both centralized and decentralized ones, become costly, inefficient and bulky in attempts to meet these requirements.

In order to solve these problems, this thesis derives two DPUPSs architectures suitable for different board layout configurations. Of the two, one DPUPS is optimal for the circuit boards with collocating loads, and the other is a better solution for the circuit boards with the loads distributed at different points on the board.

To implement the proposed DPUPS architectures for majority applications (power

level <250W), the forward converter topology is selected for its capability of high output current and low output ripples. However, no existing soft-switching forward converter topologies can be readily applied, because they suffer from some major drawbacks including the loss of soft switching at light load, the use of complex power transformer, the complicated gate drive and control design, and the poor regulation in the slave outputs. Thus, to overcome these drawbacks and to implement the proposed DPUPS are the main objectives of this thesis. To achieve the goal, the thesis is planned to develop improved soft switching forward topology in the first step. Then, based on the improved forward topologies, the DPUPSs are developed.

Chapter 2 presents the first improved ZVS and self-reset forward converter topology (Type 1). The Type 1 topology employs a resonant auxiliary circuit and a simplified power transformer, and ZVS operation is always guaranteed independent of the operating conditions. Therefore, it overcomes the said major drawbacks of existing soft-switching forward topologies. Steady state operation of the topology is analyzed, the flux excursion of the self-reset power transformer is investigated, and its characteristics are summarized. Simulation and experimental verifications of the analysis are presented. On the 200kHz 100W breadboard prototype converter, about 8% better efficiency is obtained in contrast to its hard switching counterpart.

Chapter 3 presents the second ZVS and self-reset forward converter topology (Type 2). The Type 2 topology retains all the advantages of Type 1 topology. Besides, the main switch drain voltage stress is limited at about two-times of the input voltage. Similar to Chapter 2, the Type 2 topology is analyzed and characterized, and the flux excursion of the self-reset power transformer is investigated. Simulation and

experimental verifications of the analysis are presented. On the 300kHz 50W breadboard prototype converter, about 3% better efficiency is obtained in contrast to its hard switching counterpart.

Chapter 4 presents the first DPUPS architecture based on the Type 1 converter topology. It is suitable for applications where all critical loads can be located closely around the power supply. It produces independently and precisely regulated multiple outputs in a single-stage power conversion. Thus, the number of employed power components is low. Each output circuit is regulated by controlling the synchronous rectifiers with a dedicated feedback circuit, and cross-regulation between different outputs is eliminated. Both steady state and small signal analyses are performed, and the performance and characteristics of the DPUPS architecture are summarized. A design procedure is generated based on the analyses in both Chapters 2 and 4. A breadboard prototype converter with two outputs has been built to prove the concepts. The steady state and dynamic analyses and design are verified with simulation and experimental results.

Chapter 5 presented the second DPUPS architecture based on the Type 2 converter topology. It is suitable for multi-point load applications with optimal on-board power distribution by distributing the power in the high-voltage-low-current form. The low-voltage-high-current section of each output circuit is closely located to each of the multi-point load. Hence, each of the multi-point loads can obtain finely regulated voltage and the conduction losses on the PCB tracks as well as the PCB copper requirements are greatly reduced. Both steady state and small signal analyses are performed. A design procedure is generated based on the analyses of Chapters 3 and 5. A breadboard

prototype converter of two outputs has been built to prove the concepts. The steady state and dynamic analyses and design are verified with simulation and experimental results.

6.2 CONCLUSIONS AND CONTRIBUTIONS

The following conclusions can be obtained:

(i) Soft switching of all power MOSFETs, including the main and auxiliary switches, and the SRs, can be achieved in the proposed DPUPSs independent of the operating conditions. This enables to achieve high switching frequency, high efficiency and high power density.

(ii) The power transformers are simplified with self-reset techniques, and the design of the power transformers can follow the conventional procedure but just eliminating the tertiary reset winding. This reduces the costs in design, manufacturing and board assembly of the power transformers. The core losses of the self-reset transformers are not increased. In contrary, the conduction losses may be reduced by having the flux excursion defined in the third quadrant of the hysteresis loop.

(iii) The proposed DPUPS architecture only involves a single dc/dc power conversion stage to process the power for all of the multiple outputs. This reduces the number of power components and devices, and also reduces the conduction losses that are increased otherwise in a multi-stage converters like the pre-regulator-post-regulators.

(iv) The proposed DPUPS architectures can achieve independently regulated multiple output voltages, and they eliminate the cross-regulation between outputs.

(v) The DPUPS architecture that is implemented with the Type 1 converter topology

is advantageous for applications where critical loads can be located closely, due to the integration of the power transformers and the reduction of the number of power magnetics.

(vi) The DPUPS architecture that is implemented with the Type 2 converter topology is advantageous for multi-point load applications, because it provides efficient on-board power distribution, offers finely regulated supply voltages for multi-point loads, and minimizes the PCB copper requirement.

(vii) The DPUPS implemented with the Type 1 converter topology has a RHP zero in its power circuit transfer function, and this zero is normally in the high frequency range beyond the switching frequency.

(viii) The DPUPS implemented with the Type 2 converter topology has a power circuit transfer function similar to an ordinary buck converter.

(ix) The DPUPS response to very high slew-rate large signal step loads is asymmetrical, with a much slower response to the upward step load. However, the step load in one output virtually does not affect other outputs, due to the elimination of cross-regulation.

(x) The resonant auxiliary circuit employed by the DPUPS only involves simple control and gate drive design, because the auxiliary switch does not require isolated gate drive and does not need modulation of its gating pulse width.

(xi) A major drawback of the DPUPS architectures is that the main switch is only feed-forward controlled and it does not react to the load changes, therefore, the dynamic response to a high slew-rate, large upward load transient is relatively slower than to a downward load transient.

(xii) Another drawback of the DPUPS architectures, like most existing power supplies, is the non-resonant and lossy gate drive circuits for the synchronous rectifiers. Such losses may become significant for very high switching operation.

Major contributions of this thesis include the following

(i) The DPUPS concepts are derived, and two DPUPS architectures optimal for different types of on-board power distribution are developed.

(ii) Dynamic properties of the two DPUPS architecture are investigated, and the small signal transfer functions of the power circuits are obtained.

(iii) Soft switching in the forward converter topology is improved, with two different schemes (Type 1 and Type 2).

(iv) Self reset of the power transfer is achieved.

(v) Systemically analyses are performed.

(vi) Design procedures for the proposed DPUPSs are generated.

(vii) Prototype converters are built and experiments and simulation verification are performed.

6.3 SUGGESTIONS FOR FUTURE WORK

In the proposed circuits in this thesis, all power MOSFET switches, including S_{main}, S_{aux} and SRs, are soft switched. However, there is still a type of losses related to switching of the MOSFETS that is not yet coped with in the thesis. This type of losses is the gate drive loss, that is equal to $C_{iss}V_g^2f_{sw}$, of which C_{iss} is the MOSFET inherent gate-to-source capacitor, V_g is gate drive voltage, and f_{sw} is the switching frequency.

For low switching frequency and high output voltage applications, this type of losses are usually negligible, because C_{iss} of a high voltage MOSFET is normally less

than 1nF. For instance, when the switching frequency is 200kHz, and V_g=10V, the gate drive losses for such a MOSFET is not more than 20mW.

However, for very low voltage high output current applications, an SR is normally achieved by paralleling several low Rds(ON) MOSFETs. Such a MOSFET normally has a very large gate capacitance. For example, the IRF57640 of 4mΩ Rds(ON) has a C_{iss}=6nF. In an 1V 100A (100W) application, four MOSFETs of IRF57640 should be used in parallel to fulfill one SR in order to limit its conduction losses below 1W. The total C_{iss} of such a multi-MOSFET SR is about 25nF. Thus, when the circuit is switched at 1 MHz, the SR gate drive loss will be about 2.5 W if it is externally driven, or about 10 W if it is self-driven by a transformer winding. It clearly indicates that the gate drive loss must be reduced for switching frequencies above 1 MHz, if it is not able to be eliminated completely.

The solution is the resonant gate drive. There are some reports on the resonant gate drives [113-115], however, they suffer from at least one of the following drawbacks:

(i) The implementation is rather complex and adds too many components [113],

(ii) They involve isolated gate drive from the SR it drives [113],

(iii) They employ a large coupled inductor [114],

(iv) They only recover less than 50% of the gate drive energy [114],

(v) The SR MOSFETs operate in the linear range for a significant period of time due to the resonant gate drive voltage waveform [115],

(vi) The patent related legal issues make their application difficult [113,114].

All this indicates that the resonant gate drive circuit shall be improved in the future research to further improve the proposed DPUPS performance.

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APPENDIX A

STEADY STATE DIFFERENTIAL EQUATIONS OF THE TYPE 1 CONVERTER TOPOLOGY

According to the equivalent circuits in Fig. 2.12, the steady state operation of the Type 1 converter topology satisfies the following equations, in the eight intervals:

A.1. Interval 1 ($t_0 \leq t < t_1$)

$$\begin{cases} kL_s \dfrac{di_s(t)}{dt} + u_{d1}(t) = V_d \\ L_m \dfrac{di_m(t)}{dt} + u_{d1}(t) = V_d \\ L_a \dfrac{di_a(t)}{dt} + u_a(t) - u_{d1}(t) = -k_a V_d \\ i_p(t) - i_a(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ i_a(t) - C_a \dfrac{du_a(t)}{dt} = 0 \\ i_p(t) - \dfrac{1}{k} i_s(t) - i_m(t) = 0 \end{cases} \tag{A-1}$$

A.2. Interval 2 ($t_1 \leq t < t_2$)

$$\begin{cases} kL_s \dfrac{di_s(t)}{dt} = V_d \\ L_m \dfrac{di_m(t)}{dt} = V_d \\ L_a \dfrac{di_a(t)}{dt} + u_a(t) = -k_a V_d \\ u_{d1}(t) = 0 \\ i_a(t) - C_a \dfrac{du_a(t)}{dt} = 0 \\ i_p(t) - \dfrac{1}{k} i_s(t) - i_m(t) = 0 \end{cases} \tag{A-2}$$

A.3. Interval 3 ($t_2 \leq t < t_3$)

$$\begin{cases} kL_s \dfrac{di_s(t)}{dt} = V_d \\ L_m \dfrac{di_m(t)}{dt} = V_d \\ L_a \dfrac{di_a(t)}{dt} + u_a(t) = k_a V_d \\ u_{d1}(t) = 0 \\ i_a(t) - C_a \dfrac{du_a(t)}{dt} = 0 \\ i_p(t) - \dfrac{1}{k} i_s(t) - i_m(t) = 0 \end{cases} \tag{A-3}$$

A.4. Interval 4 ($t_3 \leq t < t_4$)

$$\begin{cases} i_s(t) = I_o \\ L_m \dfrac{di_m(t)}{dt} = V_d \\ L_a \dfrac{di_a(t)}{dt} + u_a(t) = k_a V_d \\ u_{d1}(t) = 0 \\ i_a(t) - C_a \dfrac{du_a(t)}{dt} = 0 \\ i_p(t) - \dfrac{1}{k} I_o - i_m(t) = 0 \end{cases} \tag{A-4}$$

A.5. Interval 5 ($t_4 \leq t < t_5$)

$$\begin{cases} i_s(t) = I_o \\ L_m \dfrac{di_m(t)}{dt} = V_d \\ u_{d1}(t) = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_p(t) - \dfrac{1}{k} I_o - i_m(t) = 0 \end{cases} \tag{A-5}$$

A.6. Interval 6 ($t_5 \leq t < t_6$)

$$\begin{cases} i_s(t) = I_o \\ L_m \dfrac{di_m(t)}{dt} + u_{d1}(t) = V_d \\ i_p(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_p(t) - \dfrac{1}{k} I_o - i_m(t) = 0 \end{cases} \tag{A-6}$$

A.7. Interval 7 ($t_6 \leq t < t_7$)

$$\begin{cases} kL_s \dfrac{di_s(t)}{dt} + u_{d1}(t) = V_d \\ L_m \dfrac{di_m(t)}{dt} + u_{d1}(t) = V_d \\ i_p(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_p(t) - \dfrac{1}{k} i_s(t) - i_m(t) = 0 \end{cases} \tag{A-7}$$

A.8. Interval 8 ($t_7 \leq t < t_0+T_{sw}$)

$$\begin{cases} i_s(t) = 0 \\ L_m \dfrac{di_m(t)}{dt} + u_{d1}(t) = V_d \\ i_p(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_p(t) - i_m(t) = 0 \end{cases} \tag{A-8}$$

Solving these closed form equations by matching the boundary conditions, one can obtain the solutions of the principal variables, as referred to in Section 2.4.

APPENDIX B

STEADY STATE DIFFERENTIAL EQUATIONS OF THE TYPE 2 CONVERTER TOPOLOGY

According to the equivalent circuits in Fig. 3.13, the steady state operation of the Type 2 converter topology satisfies the following equations, in the nine intervals:

B.1. Interval 1 ($t_0 \leq t < t_1$)

$$\begin{cases} L_{R1}\dfrac{di_p(t)}{dt} + u_{d1}(t) = V_d \\ L_m\dfrac{di_m(t)}{dt} = 0 \\ L_a\dfrac{di_a(t)}{dt} + u_a(t) - u_{d1}(t) = -k_a V_d \\ i_p(t) - i_a(t) - C_{snb}\dfrac{du_{d1}(t)}{dt} = 0 \\ i_a(t) - C_a\dfrac{du_a(t)}{dt} = 0 \\ i_p(t) - \dfrac{1}{k}i_s(t) - i_m(t) = 0 \end{cases} \tag{B-1}$$

B.2. Interval 2 ($t_1 \leq t < t_2$)

$$\begin{cases} L_{R1}\dfrac{di_p(t)}{dt} = V_d \\ L_m\dfrac{di_m(t)}{dt} = 0 \\ L_a\dfrac{di_a(t)}{dt} + u_a(t) = -k_a V_d \\ u_{d1}(t) = 0 \\ i_a(t) - C_a\dfrac{du_a(t)}{dt} = 0 \\ i_p(t) - \dfrac{1}{k}i_s(t) - i_m(t) = 0 \end{cases} \tag{B-2}$$

B.3. Interval 3 ($t_2 \leq t < t_3$)

$$\begin{cases} L_{R1}\dfrac{di_p(t)}{dt} = V_d \\ L_m\dfrac{di_m(t)}{dt} = 0 \\ L_a\dfrac{di_a(t)}{dt} + u_a(t) = k_a V_d \\ u_{d1}(t) = 0 \\ i_a(t) - C_a\dfrac{du_a(t)}{dt} = 0 \\ i_p(t) - \dfrac{1}{k}i_s(t) - i_m(t) = 0 \end{cases} \tag{B-3}$$

B.4. Interval 4 ($t_3 \leq t < t_4$)

$$\begin{cases} i_p(t) = \dfrac{I_o}{k} + i_m(t) \\ L_m\dfrac{di_m(t)}{dt} = V_d \\ L_a\dfrac{di_a(t)}{dt} + u_a(t) = k_a V_d \\ u_{d1}(t) = 0 \\ i_a(t) - C_a\dfrac{du_a(t)}{dt} = 0 \\ i_s(t) = I_o \end{cases} \tag{B-4}$$

B.5. Interval 5 ($t_4 \leq t < t_5$)

$$\begin{cases} i_p(t) = \dfrac{I_o}{k} + i_m(t) \\ L_m\dfrac{di_m(t)}{dt} = V_d \\ i_a(t) = 0 \\ u_{d1}(t) = 0 \\ u_a(t) = V_{a4} \\ i_s(t) = I_o \end{cases} \tag{B-5}$$

B.6. Interval 6 ($t_5 \leq t < t_6$)

$$\begin{cases} i_s(t) = I_o \\ L_m \dfrac{di_m(t)}{dt} + u_{d1}(t) = V_d \\ i_p(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_p(t) - \dfrac{1}{k} I_o - i_m(t) = 0 \end{cases} \tag{B-6}$$

B.7. Interval 7 ($t_6 \leq t < t_7$)

$$\begin{cases} L_{R1} \dfrac{di_p(t)}{dt} + u_{d1}(t) = V_d \\ L_m \dfrac{di_m(t)}{dt} = 0 \\ i_p(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_p(t) - \dfrac{1}{k} i_s(t) - i_m(t) = 0 \end{cases} \tag{B-7}$$

B.8. Interval 8 ($t_7 \leq t < t_8$)

$$\begin{cases} L_{R1} \dfrac{di_R(t)}{dt} + u_{d1}(t) = V_d \\ L_m \dfrac{di_m(t)}{dt} + u_{d1}(t) = (1 + \sqrt{\dfrac{L_{R1}}{L_{R2}}}) V_d \\ i_m(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_s(t) = 0 \\ i_p(t) = i_m(t) \end{cases} \tag{B-8}$$

B.9. Interval 9 ($t_8 \le t < T_{sw} + t_0$)

$$\begin{cases} i_p(t) = i_m(t) \\ L_m \dfrac{di_m(t)}{dt} + u_{d1}(t) = V_d \\ i_m(t) - C_{snb} \dfrac{du_{d1}(t)}{dt} = 0 \\ u_a(t) = V_{a4} \\ i_a(t) = 0 \\ i_s(t) = 0 \end{cases} \tag{B-9}$$

Solving these closed form equations by matching the boundary conditions, one can obtain the solutions of the principal variables, as referred to in Section 3.4.

APPENDIX C

SMALL SIGNAL ANALYSIS OF THE DPUPS IMPLEMENTED WITH THE TYPE 1 CONVERTER TOPOLOGY

In the following, the arbitrary j^{th} output circuit small signal model is derived, according to the equivalent circuits of Fig. 4.10.

D.1. State-space equation of Mode 1

For the equivalent circuit of Fig. 4.10a, the state space equations are:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = v_{sj} - v_{oj} - R_{Lj}i_{Lj} \\ L_{sj}\dfrac{di_{sj}}{dt} = \dfrac{V_d}{k_j^2} - v_{sj} - (\dfrac{R_M}{k_j^2} + R_{SRj})i_{sj} \\ 0 = v_{sj} - R_{SRj}i_{sj} + R_{SRj}i_{Lj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \tag{C-1}$$

The duration of this mode is $\Delta_{1j}+d_j$.

D.2. State-space equation of Mode 2

For the equivalent circuit of Fig. 4.10b, the state space equations are:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = v_{sj} - v_{oj} - R_{Lj}i_{Lj} \\ L_{sj}\dfrac{di_{sj}}{dt} = \dfrac{V_d}{k_j} - v_{sj} - (\dfrac{R_M}{k_j^2} + R_{SRj})i_{sj} \\ 0 \approx v_{sj} - \dfrac{V_d}{k_j} + (\dfrac{R_M}{k_j^2} + R_{SRj})i_{Lj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \tag{C-2}$$

The duration of this mode is D-Δ_{1j}-d_j.

D.3. State-space equation of Mode 3

For the equivalent circuit of Fig. 4.10c, the state space equations are:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = v_{sj} - v_{oj} - R_{Lj}i_{Lj} \\ L_{sj}\dfrac{di_{sj}}{dt} = -\dfrac{V_d}{k_j^2} - v_{sj} - (\dfrac{R_M}{k_j^2} + R_{SRj})i_{sj} \\ 0 = v_{sj} - R_{SRj}i_{sj} + R_{SRj}i_{Lj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \tag{C-3}$$

The duration of this mode is Δ_{1j}+d_j.

D.4. State-space equation of Mode 4

For the equivalent circuit of Fig. 4.10d, the state space equations are:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = v_{sj} - v_{oj} - R_{Lj}i_{Lj} \\ L_{sj}\dfrac{di_{Lj}}{dt} = 0 \\ 0 = v_{sj} + R_{SRj}i_{Lj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \tag{C-4}$$

The duration of this mode is 1-D-Δ_{1j}-d_j.

D.5. Averaged state-space equation in one switching cycle

The averaged state-space equations can be obtained by performing the following, (C-1)·(Δ_{1j}+d_j)+(C-2)·(D-Δ_{1j}-d_j) +(C-3)·(Δ_{1j}+d_j)+(C-4)·(1-D-Δ_{1j}-d_j), which yields:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = v_{sj} - R_{Lj}i_{Lj} - v_{oj} \\ L_{sj}\dfrac{di_{sj}}{dt} = (D-\Delta_{1j}-d_j)\dfrac{V_d}{k_j} - (D+\Delta_{1j}+d_j)v_{sj} - (D+\Delta_{1j}+d_j)(\dfrac{R_M}{k_j^2}+R_{SRj})i_{sj} \\ 0 = v_{sj} - (D-\Delta_{1j}-d_j)\dfrac{V_d}{k_j} + [R_{SRj} + (D-\Delta_{1j}-d_j)\dfrac{R_M}{k_j^2}]i_{Lj} - 2(\Delta_{1j}+d_j)R_{SRj}i_{sj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \quad \text{(C-5)}$$

D.6. DC and AC model of the circuit

Assume that there are small signal perturbations in the circuit, namely

$$\begin{cases} i_{Lj} = I_{oj} + \tilde{i}_{Lj} \\ i_{sj} = I_{sj} + \tilde{i}_{sj} \\ v_{oj} = V_{oj} + \tilde{v}_{oj} \\ v_{sj} = V_{sj} + \tilde{v}_{oj} \\ v_{cj} = V_{oj} + \tilde{v}_{cj} \\ d_j = d_j + \tilde{d}_j \end{cases} \quad \text{(C-6)}$$

and substituting (C-6) into (C-5), one will obtain the dc model of the circuit as written in (4-24). For the small signal model, substituting (4-3) and (4-25) into (C-5), and neglecting higher order terms and small terms, one can obtain the transfer function from control (the simultaneous conduction interval d_j) to the output (v_{oj}) as written in (4-28).

APPENDIX D

SMALL SIGNAL ANALYSIS OF THE DPUPS IMPLEMENTED WITH THE TYPE 2 CONVERTER TOPOLOGY

In the following, the arbitrary j^{th} output circuit small signal model is derived, according to the equivalent circuits of Fig. 5.9.

D.1. State-space equation of Mode 1

For the equivalent circuit of Fig. 5.9a, the state space equations are:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = -(R_{SRj}+R_{Lj})i_{Lj} - v_{oj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \tag{D-1}$$

The duration of this mode is $\Delta_{1j}+d_j+\Delta_{2j}$.

D.2. State-space equation of Mode 2

For the equivalent circuit of Fig. 5.9b, the state space equations are:

$$\begin{cases} (\dfrac{L_{Rj1}}{k_j^2}+L_{oj})\dfrac{di_{Lj}}{dt} = \dfrac{V_d}{k_j} - (\dfrac{R_M}{k_j^2}+R_{SRj}+R_{Lj})i_{Lj} - v_{oj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \tag{D-2}$$

The duration of this mode is $D-\Delta_{1j}-d_j$.

D.3. State-space equation of Mode 3

For the equivalent circuit of Fig. 5.9c, the state space equations are:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = -(R_{SRj}+R_{Lj})i_{Lj} - v_{oj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ C_{oj}\dfrac{dv_{cj}}{dt} = i_{Lj} - \dfrac{1}{R_{oj}}v_{oj} \end{cases} \tag{D-3}$$

The duration of this mode is 1-D-Δ_{2j}.

D.4. Averaged state-space equation in one switching cycle

The averaged state-space equations can be obtained by performing the following: (D-1)·(Δ_{1j}+d_j)+(D-2)·(D-Δ_{1j}-d_j) +(D-3)·(1-D-Δ_{2j}), which yields:

$$\begin{cases} L_{oj}\dfrac{di_{Lj}}{dt} = (D-\Delta_{1j}-d_j)\dfrac{V_d}{k_j} - [(D-\Delta_{1j}-d_j)\dfrac{R_M}{k_j^2} + R_{SRj} + R_{Lj}]i_{Lj} - v_{oj} \\ C_{oj}R_{ESRj}\dfrac{dv_{cj}}{dt} = v_{oj} - v_{cj} \\ R_{oj}C_{oj}\dfrac{dv_{cj}}{dt} = R_{oj}i_{Lj} - v_{oj} \end{cases} \tag{D-4}$$

D.5. DC and AC model of the circuit

Assume that there are small signal perturbations in the circuit, namely:

$$\begin{cases} i_{Lj} = \dfrac{1}{R_{oj}}V_{oj} + \tilde{i}_{Lj} \\ v_{oj} = V_{oj} + \tilde{v}_{oj} \\ v_{cj} = V_{oj} + \tilde{v}_{cj} \\ d_j = d_j + \tilde{d}_j \end{cases} \tag{D-5}$$

and substituting (D-5) into (D-4), one will obtain the dc model of the circuit as written in (5-17). For the small signal model, substituting (5-3) and (5-18) into (D-4), and

neglecting higher order terms and small terms, one can obtain the following:

$$\begin{cases} L_{oj}\dfrac{d\tilde{i}_{Lj}}{dt} = -(\dfrac{V_d}{k_j} - \dfrac{R_M V_{oj}}{k_j^2 R_{oj}})\tilde{d}_j - (1+\dfrac{f_{sw}L_{Rj1}}{k_j^2 R_{oj}})\tilde{v}_{oj} - R_{Ej}\tilde{i}_{Lj} \\ C_{oj}R_{ESRj}\dfrac{d\tilde{v}_{cj}}{dt} = \tilde{v}_{oj} - \tilde{v}_{cj} \\ C_{oj}\dfrac{d\tilde{v}_{cj}}{dt} = \tilde{i}_{Lj} - \dfrac{1}{R_{oj}}\tilde{v}_{oj} \end{cases} \quad \text{(D-6)}$$

Applying Laplace transform to (D-6), one will obtain the following:

$$\begin{cases} sL_{oj}\hat{i}_{Lj} = -(\dfrac{V_d}{k_j} - \dfrac{R_M V_{oj}}{k_j^2 R_{oj}})\hat{d}_j - (1+\dfrac{f_{sw}L_{sj}}{R_{oj}})\hat{v}_{oj} - R_{Ej}\hat{i}_{Lj} \\ sC_{oj}R_{ESRj}\hat{v}_{cj} = \hat{v}_{oj} - \hat{v}_{cj} \\ sC_{oj}\hat{v}_{cj} = \hat{i}_{Lj} - \dfrac{1}{R_{oj}}\hat{v}_{oj} \end{cases} \quad \text{(D-7)}$$

Solving from (D-7), one can obtain the small signal transfer function from control (the simultaneous conduction interval d_j) to the output (v_{oj}) as written in (5-20).

APPENDIX E

SPREADSHEET TO CALCULATE THE FLUX EXCURSION IN TYPE 1 CONVERTER TOPOLOGY AND THE DPUPS EMPLOYING THE TYPE 1 CONVERTER

This mathcad spreadsheet is created to calculate the self-reset power transformer flux excursion in the Type 1 converter topology and in the DPUPS that is implemented with the Type 1 topology, which are discussed below in Parts I and II, respectively.

Part I Type 1 Converter Topology

To perform the analysis, the following input data are required. Refer to Chapters 2 and 4 for the difinitions of these variables.

$V_o := 5\ V$ $k := 3$ $L_s := 0.3 \cdot \mu H$ $C_{snb} := 16 \cdot nF$ $I_o := 0\ A .. 20\ A$ $I_{omax} := 20\ A$

$C_a := 66\ nF$ $L_a := 2 \cdot \mu H$ $f_s := 200\ kHz$ $L_m := 360 \cdot \mu H$

$D_{aux} := 0.08$ $R_e := 0.03 \cdot \Omega$ $Gauss := \frac{1}{76 \cdot 12 \cdot 10^{-6} \cdot m^2}$ * $T_s := \frac{1}{f_s}$

Nominal Values: $C_{snbnm} := 7 \cdot nF$ $L_{mnm} := 353 \cdot \mu H$ $L_{snm} := 0.3 \cdot \mu H$

For convenience, Intervals 3,4,5,are combined as a single interval, since they are the same in the sense of magnetizing. Thus, the following is relationship between the intervals:

Analysis	Spreadsheet	Duration
Interval 1	Interval 1	Δt1
Interval 2	Interval 2	Daux/fsw-Δt1
Intervals 3,4,5	Interval 3	D/fsw
Interval 6	Interval 4	Δt4
Interval 7	Interval 5	Δt5
Interval 8	Interval 6	Δt6

Let us start with the definition of a few functions:

$\Delta t_4(D, I_o, I_{m2}, L_m, L_s, C_{snb}) := \arccos\left(\frac{k \cdot I_{m2}}{k \cdot I_{m2} + I_o}\right) \cdot \left(k \cdot \sqrt{L_s \cdot C_{snb}}\right)$ *

$$u_0(t,D,I_o,I_{m2},L_s,L_m,C_{snb},\omega_2,\omega_3,V_d,\Delta_4) := \left| \begin{array}{l} \xi \leftarrow \omega_2 \cdot \Delta_4 \\ V_{d1} \leftarrow V_d + \dfrac{\dfrac{I_o}{k} + I_{m2}}{\omega_2 \cdot C_{snb}} \cdot \sin(\xi) \\ I_{m4} \leftarrow \dfrac{\left[\begin{array}{l} \cos(\omega_2 \cdot \Delta_4) \cdot k \cdot L_s \cdot (I_o + I_{m2} \cdot k) \ \ldots \\ + I_{m2} \cdot L_m - I_{m2} \cdot k^2 \cdot L_s - I_o \cdot k \cdot L_s \end{array} \right]}{L_m} \\ V_d + (V_{d1} - V_d) \cdot \cos(\omega_3 \cdot t) + \dfrac{I_{m4}}{(C_{snb} \cdot \omega_3)} \cdot \sin(\omega_3 \cdot t) \end{array} \right.$$

$$\delta(D,I_o,I_{m2},L_s,L_m,C_{snb},\omega_2,\omega_3,V_d,\Delta_4) := \left| \begin{array}{l} t_3 \leftarrow \dfrac{1}{\omega_3} \cdot \operatorname{atan}\left(\dfrac{V_d \cdot \omega_3 \cdot C_{snb}}{I_{m2} + \dfrac{I_o}{k}} \right) \\ t_5 \leftarrow \dfrac{1 - D - D_{aux} - \Delta_4 \cdot f_s - t_3 \cdot f_s}{f_s} \\ \dfrac{u_0(t_5,D,I_o,I_{m2},L_s,L_m,C_{snb},\omega_2,\omega_3,V_d,\Delta_4) - V_d}{V_d} \end{array} \right.$$

$$u_{d11}(t,D,I_o,I_{m0},I_{m2},L_s,L_m,C_{snb},C_a,L_a,\delta,V_d) := \left| \begin{array}{l} \alpha \leftarrow L_a \cdot C_a \cdot k^2 \cdot L_s \cdot C_{snb} \\ \beta \leftarrow k^2 \cdot L_s \cdot (C_{snb} + C_a) + L_a \cdot C_a \\ \omega_{11} \leftarrow \dfrac{1}{2} \cdot \sqrt{\dfrac{2 \cdot \beta + 2\sqrt{\beta^2 - 4 \cdot \alpha}}{\alpha}} \\ \omega_{12} \leftarrow \dfrac{1}{2} \cdot \sqrt{\dfrac{2 \cdot \beta - 2\sqrt{\beta^2 - 4 \cdot \alpha}}{\alpha}} \\ M \leftarrow \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & \omega_{11} \cdot s & 0 & \omega_{12} \cdot s \\ -(\omega_{11} \cdot s)^2 & 0 & -(\omega_{12} \cdot s)^2 & 0 \\ 0 & -(\omega_{11} \cdot s)^3 & 0 & -(\omega_{12} \cdot s)^3 \end{bmatrix}^{-1} \\ \text{Vector} \leftarrow \begin{bmatrix} \dfrac{\delta \cdot V_d}{V} \\ \dfrac{I_{m0} \cdot F}{C_{snb} \cdot A} \\ \dfrac{1 \cdot F}{C_{snb}} \cdot \left[\dfrac{(-\delta \cdot V_d) \cdot H}{k^2 \cdot L_s \cdot V} - \dfrac{(1+\delta) \cdot V_d \cdot H}{L_a \cdot V} \right] \\ \dfrac{1 \cdot F}{C_{snb}} \cdot \left(\dfrac{-I_{m0} \cdot F \cdot H}{C_{snb} \cdot k^2 \cdot L_s \cdot A} - \dfrac{I_{m0} \cdot F \cdot H}{C_{snb} \cdot L_a \cdot A} \right) \end{bmatrix} \\ a \leftarrow M \cdot \text{Vector} \\ V_d + a_1 \cdot V \cdot \cos(\omega_{11} \cdot t) + a_2 \cdot V \cdot \sin(\omega_{11} \cdot t) \ \ldots \\ + a_3 \cdot V \cdot \cos(\omega_{12} \cdot t) + a_4 \cdot V \cdot \sin(\omega_{12} \cdot t) \end{array} \right.$$

$$t_6(D, I_o, I_{m2}, L_s, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_4) :=$$

$$\xi \leftarrow \omega_2 \cdot \Delta_4$$

$$I_{m4} \leftarrow \frac{\left[\cos(\xi)\cdot k \cdot L_s \cdot (I_o + I_{m2}\cdot k) + I_{m2}\cdot L_m - I_{m2}\cdot k^2 \cdot L_s - I_o \cdot k \cdot L_s\right]}{L_m}$$

$$\text{alpha} \leftarrow \operatorname{atan}\left[\frac{\frac{I_o}{k} + I_{m2}}{\omega_2 \cdot C_{snb}}\cdot \sin(\xi) \Big/ \frac{-I_{m4}}{\omega_3 \cdot C_{snb}}\right]$$

$$\text{if}\left[\text{alpha} > 0\ \text{deg}, \frac{1}{\omega_3}\cdot(\text{alpha}), \frac{1}{\omega_3}\cdot(\text{alpha}+\pi)\right]\cdot 1$$

$$\Delta I_{m1}(t_1, D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, L_a, \delta, V_d) :=$$

$$\alpha \leftarrow L_a \cdot C_a \cdot k^2 \cdot L_s \cdot C_{snb}$$

$$\beta \leftarrow k^2 \cdot L_s \cdot (C_{snb} + C_a) + L_a \cdot C_a$$

$$\omega_{11} \leftarrow \frac{1}{2}\cdot\sqrt{\frac{2\cdot\beta + 2\sqrt{\beta^2 - 4\cdot\alpha}}{\alpha}}$$

$$\omega_{12} \leftarrow \frac{1}{2}\cdot\sqrt{\frac{2\cdot\beta - 2\sqrt{\beta^2 - 4\cdot\alpha}}{\alpha}}$$

$$V_d \leftarrow \frac{k\cdot V_o + k\cdot(R_e + f_s \cdot L_s)\cdot(I_o)}{D}$$

$$M \leftarrow \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & \omega_{11}\cdot s & 0 & \omega_{12}\cdot s \\ -(\omega_{11}\cdot s)^2 & 0 & -(\omega_{12}\cdot s)^2 & 0 \\ 0 & -(\omega_{11}\cdot s)^3 & 0 & -(\omega_{12}\cdot s)^3 \end{bmatrix}^{-1}$$

$$\text{Vector} \leftarrow \begin{bmatrix} \frac{\delta \cdot V_d}{V} \\ \frac{I_{m0}\cdot F}{C_{snb}\cdot A} \\ \frac{1\cdot F}{C_{snb}}\cdot\left[\frac{(-\delta\cdot V_d)\cdot H}{k^2\cdot L_s \cdot V} - \frac{(1+\delta)\cdot V_d \cdot H}{L_a \cdot V}\right] \\ \frac{1\cdot F}{C_{snb}}\cdot\left(\frac{-I_{m0}\cdot F\cdot H}{C_{snb}\cdot k^2 \cdot L_s \cdot A} - \frac{I_{m0}\cdot F\cdot H}{C_{snb}\cdot L_a \cdot A}\right) \end{bmatrix}$$

$$a \leftarrow M \cdot \text{Vector}$$

$$\theta 1 \leftarrow t_1 \cdot \omega_{11}$$

$$\theta 2 \leftarrow t_1 \cdot \omega_{12}$$

$$\frac{V}{L_m}\cdot\left[\frac{-\left(\begin{matrix}\sin(\theta 1)\cdot a_1 \cdot \omega_{12} - \cos(\theta 1)\cdot a_2 \cdot \omega_{12} \cdots \\ + \sin(\theta 2)\cdot a_3 \cdot \omega_{11} - \cos(\theta 2)\cdot a_4 \cdot \omega_{11}\end{matrix}\right)}{(\omega_{11}\cdot\omega_{12})} \cdots + \frac{(a_4\cdot\omega_{11} + a_2\cdot\omega_{12})}{(\omega_{12}\cdot\omega_{11})}\right]$$

Gauess $t_{11} := \frac{0.05}{f_s}$ $t_{11} = 2.5 \cdot 10^{-7}\ s$

Given $u_{d11}(t_{11}, D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, L_a, \delta, V_d) = 0 \cdot V$ $t_{11} < \frac{D_{aux}}{f_s}$

$t_{x1}(D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, L_a, \delta, V_d) := \text{Find}(t_{11})$

$$f1(\rho, \omega_3) := \text{if}\left[\rho > 0, \left[\frac{1}{\omega_3} \cdot (\rho)\right], \left[\frac{1}{\omega_3} \cdot (\rho + \pi)\right]\right]$$

$$f2(\Delta t_6, \omega_3, D_x, \Delta t_4, f_s, D_{aux}, \Delta t_3, \tau) := \text{if}\left[\Delta t_6 > 0 \cdot s, (\tau \cdot \omega_3), \left[\omega_3 \cdot \frac{(1 - D_x - \Delta t_4 \cdot f_s - D_{aux} - \Delta t_3 \cdot f_s)}{f_s}\right]\right]$$

$$f3(\omega_2, \Delta t_6, L_m, C_{snb}, I_{m4}, \Delta I_{m5}) := \text{if}\left(\Delta t_6 > 0 \cdot s, \frac{\cos(\omega_2 \cdot \Delta t_6)}{\omega_2^2 \cdot L_m} \cdot \frac{I_{m4} + \Delta I_{m5}}{C_{snb}}, 0\ A\right)$$

$$f4(D, I_o, I_{m2}, L_s, L_m, C_{snb}, V_{d0}, Vd, \omega 2, \omega 3, \Delta 4, \Delta 6) := \text{if}\left(\Delta 6 > 0 \cdot s, \frac{V_{d0} - Vd}{Vd}, \delta(D, I_o, I_{m2}, L_s, L_m, C_{snb}, \omega 2, \omega 3, Vd, \Delta 4)\right)$$

$$f5(D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, La, \delta, fs, Daux, Vd) := \text{if}\left(\delta > 0, t_{x1}(D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, La, \delta, Vd), \frac{Daux}{fs}\right)$$

Guess $I_{max} := 0 \cdot A$ *

Given

$$0 \le \omega_2 \leftarrow \frac{1}{k\cdot\sqrt{L_s\cdot C_{snb}}}$$

$$\omega_1 \leftarrow \frac{\omega_2}{\sqrt{2}}$$

$$V_d \leftarrow \frac{k\cdot V_o + k\cdot\left(R_e + f_s\cdot L_s\right)\cdot\left(I_o\right)}{D}$$

$$\omega_3 \leftarrow \frac{1}{\sqrt{L_m\cdot C_{snb}}}$$

$$t_3 \leftarrow \frac{1}{\omega_3}\cdot\operatorname{atan}\left(\frac{k\cdot V_d\cdot\omega_3\cdot C_{snb}}{k\cdot I_{max} + I_o}\right)$$

$$\Delta I_{m3} \leftarrow \sin\left(\omega_3\cdot t_3\right)\cdot\omega_3\cdot V_d\cdot C_{snb} + \left(I_{max} + \frac{I_o}{k}\right)\cdot\left(\cos\left(\omega_3\cdot t_3\right) - 1\right)$$

$$I_{m2} \leftarrow I_{max} + \Delta I_{m3}$$

$$tt_4 \leftarrow \frac{1}{\omega_2}\cdot\operatorname{acos}\left(\frac{k\cdot I_{m2}}{k\cdot I_{m2} + I_o}\right)$$

$$\theta \leftarrow \omega_2\cdot tt_4$$

$$V_{d1} \leftarrow V_d + \frac{I_o + k\cdot I_{m2}}{k\cdot\omega_2\cdot C_{snb}}\cdot\sin(\theta)$$

$$I_{m4} \leftarrow \frac{\left[\cos(\theta)\cdot k\cdot L_s\cdot\left(I_o + I_{m2}\cdot k\right) + I_{m2}\cdot L_m - I_{m2}\cdot k^2\cdot L_s - I_o\cdot k\cdot L_s\right]}{L_m}$$

$$\Delta I_{m4} \leftarrow \frac{\left(\cos(\theta)\cdot I_o + \cos(\theta)\cdot I_{m2}\cdot k - I_o - I_{m2}\cdot k\right)}{L_m}\cdot k\cdot L_s$$

$$\rho \leftarrow \operatorname{atan}\left[\frac{\left(V_{d1} - V_d\right)\cdot\left(\omega_3\cdot C_{snb}\right)}{-I_{m4}}\right]$$

$$\tau \leftarrow \left(f1\left(\rho, \omega_3\right)\right)\cdot 1$$

$$\Delta t_6 \leftarrow -\tau + \left(1 - D - tt_4\cdot f_s - D_{aux} - t_3\cdot f_s\right)\cdot\frac{1}{f_s}$$

$$\beta \leftarrow \left(f2\left(\Delta t_6, \omega_3, D, tt_4, f_s, D_{aux}, t_3, \tau\right)\right)\cdot 1$$

$$\Delta I_{m5} \leftarrow \left(-\sin(\beta)\cdot\omega_3\cdot C_{snb}\cdot V_{d1} + \sin(\beta)\cdot\omega_3\cdot C_{snb}\cdot V_d + \cos(\beta)\cdot I_{m4}\right) - I_{m4}$$

$$\Delta I_{m6} \leftarrow \left(f3\left(\omega_2, \Delta t_6, L_m, C_{snb}, I_{m4}, \Delta I_{m5}\right)\right)\cdot 1$$

$$V_{d0} \leftarrow V_d + \frac{I_{m4} + \Delta I_{m5}}{\omega_2\cdot C_{snb}}\cdot\sin\left(\omega_2\cdot\Delta t_6\right)$$

$$I_{m0} \leftarrow I_{m2} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6}$$

$$\delta \leftarrow \left(f4\left(D, I_o, I_{m2}, L_s, L_m, C_{snb}, V_{d0}, V_d, \omega_2, \omega_3, tt_4, \Delta t_6\right)\right)\cdot 1$$

$$t_1 \leftarrow f5\left(D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, L_a, \delta, f_s, D_{aux}, V_d\right)$$

$$\Delta I_{m2} \leftarrow \frac{V_d}{L_m}\cdot\left[\frac{D + \left(D_{aux}\right)}{f_s} - t_1\right]$$

$$\Delta I_{m11} \leftarrow \Delta I_{m1}\left(t_1, D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, L_a, \delta, V_d\right)$$

$$\Delta I_{m11} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6}$$

$$I_{mmax}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) := \text{Find}(I_{max})$$

$$I_{m\_mmax}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) := \left[\begin{array}{l} V_d \leftarrow \frac{k \cdot V_o + k \cdot (R_e + f_s \cdot L_s) \cdot (I_o)}{D} \\ \omega_3 \leftarrow \frac{1}{\sqrt{L_m \cdot C_{snb}}} \\ I_{max} \leftarrow I_{mmax}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) \\ t_3 \leftarrow \frac{1}{\omega_3} \cdot \operatorname{atan}\left(\frac{V_d \cdot \omega_3 \cdot C_{snb}}{I_{max} + \frac{I_o}{k}} \right) \\ I_{max} + \left[\frac{V_d \cdot \sin(\omega_3 \cdot t_3)}{\omega_3 \cdot L_m} + \left(I_{max} + \frac{I_o}{k} \right) \cdot (\cos(\omega_3 \cdot t_3) - 1) \right] \end{array} \right]$$

The maximum flux density of the excursion:

$$B_{m\_max}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) := I_{m\_mmax}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) \cdot L_m \cdot \text{Gauss} \cdot \sqrt{\frac{L_{mnm}}{L_m}}$$

The ac excursion range:

$$\Delta B_m(D, L_m, I_o, L_s) := \frac{\frac{k \cdot V_o + k \cdot (R_e + f_s \cdot L_s) \cdot (I_o)}{D}}{L_m} \cdot D \cdot \frac{L_m}{f_s} \cdot \text{Gauss} \cdot \sqrt{\frac{L_{mnm}}{L_m}}$$

Part II The first DPUPS

$L_s := 0.3 \cdot \mu H$ $C_{snb} := 10 \cdot nF$ $I_{omax} := 10\ A$ $I_o := 1\ A .. I_{omax}$

$R_e := 0.002\ \Omega$ $I_{m2} := -0.2\ A$ $n := 1 .. 10$ $L_{snm} := 0.6 \cdot \mu H$

$$Iin\_pk(I_o, I_{max}, L_s, L_m, V_d) := \left| \begin{array}{l} d \leftarrow \dfrac{k \cdot (R_e + f_s \cdot L_s) \cdot (I_{omax} - I_o)}{V_d} \\ I_{max} + \dfrac{I_o}{k} + \dfrac{V_d}{k^2 \cdot L_s} \cdot \dfrac{d}{f_s} \end{array} \right.$$

$$Ispk(I_o, I_{max}, L_s, L_m, V_d) := \left| \begin{array}{l} d \leftarrow \dfrac{k \cdot (R_e + f_s \cdot L_s) \cdot (I_{omax} - I_o)}{V_d} \\ I_o + \dfrac{V_d}{k \cdot L_s} \cdot \dfrac{d}{f_s} \end{array} \right.$$

$$i_s(t, \omega_2, V_d, I_{pk}, Is_{pk}) := \cos(\omega_2 \cdot t) \cdot I_{pk} \cdot k + Is_{pk} - I_{pk} \ *$$

$$\Delta t_4(D, \omega_2, V_d, I_{pk}, Is_{pk}) := \frac{\operatorname{acos}\left[\dfrac{(-Is_{pk} + I_{pk} \cdot k)}{(I_{pk} \cdot k)}\right]}{\omega_2}$$

$$u_0(t, D, I_o, I_{max}, L_s, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_4, I_{pk}) := \left| \begin{array}{l} \xi \leftarrow \omega_2 \cdot \Delta_4 \\ V_{d1} \leftarrow V_d + \dfrac{I_{pk}}{\omega_2 \cdot C_{snb}} \cdot \sin(\xi) \\ I_{m4} \leftarrow I_{max} + \dfrac{\left(\cos(\omega_2 \cdot \Delta_4) \cdot k^2 \cdot L_s \cdot I_{pk} - I_{pk} \cdot k^2 \cdot L_s\right)}{L_m} \\ V_d + (V_{d1} - V_d) \cdot \cos(\omega_3 \cdot t) + \dfrac{I_{m4}}{(C_{snb} \cdot \omega_3)} \cdot \sin(\omega_3 \cdot t) \end{array} \right.$$

$$t_6(D, I_o, I_{max}, L_s, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_4, I_{pk}) := \left| \begin{array}{l} \xi \leftarrow \omega_2 \cdot \Delta_4 \\ I_{m4} \leftarrow I_{max} + \dfrac{\left(\cos(\omega_2 \cdot \Delta_4) \cdot k^2 \cdot L_s \cdot I_{pk} - I_{pk} \cdot k^2 \cdot L_s\right)}{L_m} \\ alpha \leftarrow \operatorname{atan}\left[\dfrac{\dfrac{I_{pk}}{\omega_2 \cdot C_{snb}} \cdot \sin(\xi)}{\dfrac{-I_{m4}}{\omega_3 \cdot C_{snb}}}\right] \\ if\left[alpha > 0\ deg, \dfrac{1}{\omega_3} \cdot (alpha), \dfrac{1}{\omega_3} \cdot (alpha + \pi)\right] \cdot 1 \end{array} \right.$$

$$\delta(D, I_o, I_{max}, L_s, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_4, I_{pk}) := \left| \begin{array}{l} t_5 \leftarrow \dfrac{1 - D - D_{aux} - \Delta_4 \cdot f_s}{f_s} \\ \dfrac{u_0(t_5, D, I_o, I_{max}, L_s, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_4, I_{pk}) - V_d}{V_d} \end{array} \right.$$

$$f4(D, Io, Im2, Ls, Lm, Csnb, \Delta 6, Vd0, Vd, \omega 2, \omega 3, \Delta 4, I_{pk}) := if\left(\Delta 6 > 0 \cdot s, \frac{Vd0 - Vd}{Vd}, \delta(D, Io, Im2, Ls, Lm, Csnb, \omega 2, \omega 3, Vd, \Delta 4, I_{pk})\right)$$

$I_{max} := .25 \cdot A$ $R_e := 0.050\ \Omega$ $D_{aux} = 0.08$

Given

$$0 \le \omega_2 \leftarrow \frac{1}{k\cdot\sqrt{L_s\cdot C_{snb}}}$$

$$\omega_1 \leftarrow \frac{\omega_2}{\sqrt{2}}$$

$$V_d \leftarrow k\cdot\frac{\left(f_s\cdot L_s\cdot I_{omax}+V_o+R_e\cdot I_{omax}\right)}{D}$$

$$D_x \leftarrow D$$

$$\omega_3 \leftarrow \frac{1}{\sqrt{L_m\cdot C_{snb}}}$$

$$I_{in\_pk} \leftarrow Iin\_pk\left(I_o, I_{max}, L_s, L_m, V_d\right)$$

$$Is_{pk} \leftarrow Ispk\left(I_o, I_{max}, L_s, L_m, V_d\right)$$

$$tt_4 \leftarrow \frac{\operatorname{acos}\left[\frac{\left(-Is_{pk}+I_{in\_pk}\cdot k\right)}{\left(I_{in\_pk}\cdot k\right)}\right]}{\omega_2}$$

$$\theta \leftarrow \omega_2\cdot tt_4$$

$$V_{d1} \leftarrow V_d+\frac{I_{in\_pk}}{\omega_2\cdot C_{snb}}\cdot\sin(\theta)$$

$$I_{m4} \leftarrow I_{max}+\frac{\left(\cos(\theta)\cdot k^2\cdot L_s\cdot I_{in\_pk}-I_{in\_pk}\cdot k^2\cdot L_s\right)}{L_m}$$

$$\Delta I_{m4} \leftarrow \frac{\left(\cos(\theta)\cdot k^2\cdot L_s\cdot I_{in\_pk}-I_{in\_pk}\cdot k^2\cdot L_s\right)}{L_m}$$

$$\rho \leftarrow \operatorname{atan}\left(\frac{V_{d1}-V_d}{\frac{-I_{m4}}{\omega_3\cdot C_{snb}}}\right)$$

$$\tau \leftarrow \left(f1\left(\rho, \omega_3\right)\right)\cdot 1$$

$$\Delta t_6 \leftarrow -\tau+\left(1-D_x-tt_4\cdot f_s-\frac{D_{aux}}{2}\right)\frac{1}{f_s}$$

$$\beta \leftarrow \left(f2\left(\Delta t_6, \omega_3, D_x, tt_4, f_s, D_{aux}, \tau\right)\right)\cdot 1$$

$$\Delta I_{m5} \leftarrow \left(-\sin(\beta)\cdot\omega_3\cdot C_{snb}\cdot V_{d1}+\sin(\beta)\cdot\omega_3\cdot C_{snb}\cdot V_d+\cos(\beta)\cdot I_{m4}\right)-I_{m4}$$

$$\Delta I_{m6} \leftarrow \left(f3\left(\omega_2, \Delta t_6, L_m, C_{snb}, I_{m4}, \Delta I_{m5}\right)\right)\cdot 1$$

$$V_{d0} \leftarrow V_d+\frac{I_{m4}+\Delta I_{m5}}{\omega_2\cdot C_{snb}}\cdot\sin\left(\omega_2\cdot\Delta t_6\right)$$

$$I_{m0} \leftarrow I_{max}+\Delta I_{m4}+\Delta I_{m5}+\Delta I_{m6}$$

$$\delta \leftarrow \left(f4\left(D, I_o, I_{max}, L_s, L_m, C_{snb}, \Delta t_6, V_{d0}, V_d, \omega_2, \omega_3, tt_4, I_{in\_pk}\right)\right)\cdot 1$$

$$t_1 \leftarrow f5\left(D, I_o, I_{m0}, I_{max}, L_s, L_m, C_{snb}, C_a, L_a, \delta, f_s, D_{aux}, V_d\right)$$

$$\Delta I_{m2} \leftarrow \frac{V_d}{L_m}\cdot\left(\frac{D_x+D_{aux}}{f_s}-t_1\right)$$

$$\Delta I_{m11} \leftarrow \Delta I_{m1}\left(t_1, D, I_o, I_{m0}, I_{m2}, L_s, L_m, C_{snb}, C_a, L_a, \delta, V_d\right)$$

$$\Delta I_{m11}+\Delta I_{m2}+\Delta I_{m4}+\Delta I_{m5}+\Delta I_{m6}$$

$$I_{mmax}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) := \text{Find}(I_{max})$$

The maximum flux density of the excursion:

$$B_{m\_max}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) := I_{m\_mmax}(I_o, D, C_{snb}, L_m, L_s, C_a, L_a) \cdot L_m \cdot \text{Gauss} \cdot \sqrt{\frac{L_{mnm}}{L_m}}$$

The ac flux excursion range

$$\Delta B_m(D, L_m, I_o, L_s) := \left| \begin{array}{l} Dx \leftarrow D \\ k \cdot \dfrac{\left(f_s \cdot L_s \cdot I_{omax} + V_o + R_e \cdot I_{omax}\right)}{D} \cdot (Dx) \cdot \dfrac{L_m}{f_s} \cdot \text{Gauss} \cdot \sqrt{\dfrac{L_{mnm}}{L_m}} \end{array} \right.$$

APPENDIX F

SPREADSHEET TO CALCULATE THE FLUX EXCURSION IN TYPE 2 CONVERTER TOPOLOGY AND THE DPUPS EMPLOYING THE TYPE 2 CONVERTER

This mathcad spreadsheet is created to calculate the self-reset power transformer flux excursion in the Type 2 converter topology and in the DPUPS that is implemented with the Type 2 topology, in Part I and Part II, respectively.

Part I Type 2 Converter Topology

To perform the analysis, the following input data are required. Refer to Chapters 3 and 5 for the difinitions of these variables.

$V_o := 5\ V$ $k := 3$ $L_{R1} := 6 \cdot \mu H$ $C_{snb} := 10 \cdot nF$ $I_o := 0\ A, 0.1\ A .. 10\ A$ $I_{omax} := 10\ A$

$C_a := 66\ nF$ $L_a := 2 \cdot \mu H$ $L_{R2} := L_{R1}$ $f_s := 300\ kHz$ $L_m := 360 \cdot \mu H + 983 \cdot \mu H \cdot 0$ $D_{aux} := 0.08$

$I_{max} := 0 \cdot A$ $D_{aux} := 0.08$ $R_e := 0.03 \cdot \Omega$ $Gauss := \frac{1}{(76 \cdot 12 \cdot 10^{-6})} \cdot 0 + \frac{1}{121 \cdot 9 \cdot 10^{-6}}$ $Gauss = 918.27365$

$R_e := 0.03\ \Omega$ $T_s := \frac{1}{f_s}$

For convenience , Intervals 3,4,5,are combined as a single interval, since they are the same in the sense of magnetizing. Thus, the following is the relationship between the intervals:

Analysis	Spread Sheet	Duration
Interval 1	Interval 1	Daux (intervals 1 and 2 total duation)
Interval 2	Interval 2	
Intervals 3,4,5	Interval 3	D
Interval 6	Interval 4a	$\Delta t4a$
Interval 7	Interval 4b	$\Delta t4b$
Interval 8	Interval 5	$\Delta t5$
Interval 9	Interval 6	$\Delta t6$

Let us start with the definition of a few functions:

$$\Delta t_{4a}(I_o, I_{in2}, \omega_2, \omega_3, V_d) := \frac{\operatorname{atan}\left(V_d \cdot \omega_3 \cdot \frac{C_{snb}}{I_{in2}}\right)}{\omega_3}$$

$$\Delta t_{4b}(I_o, I_{in\_pk}, I_{max2}, \omega_2, A) := \begin{cases} \dfrac{\operatorname{asin}(A)}{\omega_2} & \text{if } A \le 1 \\ \dfrac{\operatorname{acos}\left(\dfrac{I_{max2}}{I_{in\_pk}}\right)}{\omega_2} & \text{otherwise} \end{cases}$$

$$\delta(D, I_{max2}, I_{m5}, \omega_2, \omega_3, V_d, \Delta_5, \Delta_6, V_{ds\_5}) := \begin{cases} V_0 \leftarrow (V_{ds\_5} - V_d)\cdot\cos(\omega_3\cdot\Delta_6) + \dfrac{I_{m5}}{(C_{snb}\cdot\omega_3)}\cdot\sin(\omega_3\cdot\Delta_6) + V_d \\ \dfrac{V_0 - V_d}{V_d} \end{cases}$$

$$u_{d1}(t, D, I_{m0}, I_m, I_5, L_{R1}, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_5, \Delta_6, V_5) := \begin{cases} \alpha 1 \leftarrow L_a\cdot C_a\cdot L_{R1}\cdot C_{snb} \\ \beta \leftarrow L_{R1}\cdot(C_{snb} + C_a) + L_a\cdot C_a \\ \omega_{12} \leftarrow \sqrt{\dfrac{\beta + \sqrt{\beta^2 - 4\cdot\alpha 1}}{2\cdot\alpha 1}} \\ \omega_{11} \leftarrow \sqrt{\dfrac{\beta - \sqrt{\beta^2 - 4\cdot\alpha 1}}{2\cdot\alpha 1}} \\ \delta\delta \leftarrow \delta(D, I_m, I_5, \omega_2, \omega_3, V_d, \Delta_5, \Delta_6, V_5) \\ M \leftarrow \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & \dfrac{\omega_{11}}{Hz} & 0 & \dfrac{\omega_{12}}{Hz} \\ -\dfrac{\omega_{11}^2}{Hz^2} & 0 & -\dfrac{\omega_{12}^2}{Hz^2} & 0 \\ 0 & -\dfrac{\omega_{11}^3}{Hz^3} & 0 & -\dfrac{\omega_{12}^3}{Hz^3} \end{bmatrix}^{-1} \\ Vector \leftarrow \begin{bmatrix} \delta\delta\cdot\dfrac{V_d}{V} \\ \dfrac{I_{m0}\cdot F}{C_{snb}\cdot A} \\ -(1+\delta\delta)\cdot\dfrac{(L_a + L_{R1})\cdot V_d}{V\cdot H} \ldots \\ \quad + \dfrac{V_d\cdot L_a}{V\cdot H} \\ \dfrac{L_{R1}\cdot L_a\cdot C_{snb}}{H\cdot H\cdot F} \\ -\dfrac{I_{m0}\cdot F}{C_{snb}\cdot A}\cdot\dfrac{\dfrac{(L_a + L_{R1})}{H}}{\dfrac{L_{R1}\cdot L_a\cdot C_{snb}}{H\cdot H\cdot F}} \end{bmatrix} \\ a \leftarrow M\cdot Vector \\ V_d + \begin{pmatrix} a_1\cdot\cos(\omega_{11}\cdot t) + a_2\cdot\sin(\omega_{11}\cdot t) \ldots \\ + a_3\cdot\cos(\omega_{12}\cdot t) + a_4\cdot\sin(\omega_{12}\cdot t) \end{pmatrix}\cdot V \end{cases}$$

$t1 := 0.1 \cdot 10^{-6}\,s$ *

Given

$t1 > 0\,s \qquad t1 < 0.3 \cdot 10^{-6}\,s$

$u_{d1}(t1, D, I_{m0}, I_{max2}, I_{m5}, L_{R1}, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta t_5, \Delta t_6, V_{ds\_5}) = 0 \cdot V$

$\Delta t_1(D, I_{m0}, I_{max2}, I_{m5}, L_{R1}, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta t_5, \Delta t_6, V_{ds\_5}) := \text{Find}(t1)$

$$\Delta t_2(D, I_o, I_{m0}, L_{R1}, V_d, Iin) := \frac{\frac{I_o}{k} - Iin + I_{m0}}{V_d} \cdot L_{R1}$$

Given

$$0\,A \le \omega_2 \leftarrow \frac{1}{\sqrt{L_{R1} \cdot C_{snb}}}$$

$$\omega_3 \leftarrow \frac{1}{\sqrt{L_m \cdot C_{snb}}}$$

$$V_d \leftarrow \frac{1}{D}\cdot\left[k\cdot\left[V_o + R_e\cdot\left(I_o\right)\right] + \frac{f_s \cdot L_{R1}\cdot\left(I_o\right)}{k}\right]$$

$$I_{in2} \leftarrow I_{max} + \frac{I_o}{k}$$

$$\Delta_{4a} \leftarrow \frac{1}{\omega_3}\cdot\operatorname{atan}\left(V_d \cdot \omega_3 \cdot \frac{C_{snb}}{I_{in2}}\right)$$

$$\Delta I_{m4a} \leftarrow \left(\sin\left(\Delta_{4a}\cdot\omega_3\right)\cdot V_d\cdot\omega_3\cdot C_{snb} + \cos\left(\Delta_{4a}\cdot\omega_3\right)\cdot I_{in2}\right) - I_{in2}$$

$$I_{in\_pk} \leftarrow I_{in2} + \Delta I_{m4a}$$

$$I_{max2} \leftarrow I_{max} + \Delta I_{m4a}$$

$$Aid\_A \leftarrow V_d \cdot C_{snb} \cdot \frac{\omega_2}{I_{in\_pk}}$$

$$\Delta_{4b} \leftarrow \Delta t_{4b}\left(I_o, I_{in\_pk}, I_{max2}, \omega_2, Aid\_A\right)$$

$$I_{LR1\_end} \leftarrow I_{in\_pk}\cdot\cos\left(\omega_2\cdot\Delta_{4b}\right)$$

$$\Delta_5 \leftarrow \begin{cases} (0\,s) & \text{if } Aid\_A > 1 \\ \left[\frac{L_{R1}}{V_d}\cdot\left(I_{LR1\_end} - I_{max2}\right)\right] & \text{otherwise} \end{cases}$$

$$\Delta I_{m5} \leftarrow I_{max2}\cdot\left(\cos\left(\omega_3\cdot\Delta_5\right) - 1\right)$$

$$\Delta_6 \leftarrow \left(1 - D - D_{aux}\right)\cdot T_s - \Delta_{4a} - \Delta_5 - \Delta_{4b}$$

$$I_{m5} \leftarrow I_{max2} + \Delta I_{m5}$$

$$V_{ds\_5} \leftarrow \begin{cases} \left(V_d + \frac{I_{in\_pk}}{C_{snb}\cdot\omega_2}\cdot\sin\left(\omega_2\cdot\Delta_{4b}\right)\right) & \text{if } Aid\_A > 1 \\ \left[\frac{I_{max2}}{\left(C_{snb}\cdot\omega_3\right)}\cdot\sin\left(\omega_3\cdot\Delta_5\right) + 2\cdot V_d\right] & \text{otherwise} \end{cases}$$

$$\Delta I_{m6} \leftarrow \sin\left(\Delta_6\cdot\omega_3\right)\cdot\omega_3\cdot C_{snb}\cdot\left(V_d - V_{ds\_5}\right) + I_{m5}\cdot\left(\cos\left(\Delta_6\cdot\omega_3\right) - 1\right)$$

$$I_{m0} \leftarrow I_{max2} + \Delta I_{m5} + \Delta I_{m6}$$

$$\Delta_1 \leftarrow \Delta t_1\left(D, I_{m0}, I_{max2}, I_{m5}, L_{R1}, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_5, \Delta_6, V_{ds\_5}\right)$$

$$Iin \leftarrow \frac{\int_0^{\Delta_1}\left(V_d - u_{d1}\left(t, D, I_{m0}, I_{max2}, I_{m5}, L_{R1}, L_m, C_{snb}, \omega_2, \omega_3, V_d, \Delta_5, \Delta_6, V_{ds\_5}\right)\right)dt}{L_{R1}} + I_{m0}$$

$$Iin \leftarrow \begin{cases} Iin & \text{if } Iin > 0\,A \\ I_{m0} & \text{otherwise} \end{cases}$$

$$\Delta_2 \leftarrow \Delta t_2\left(D, I_o, I_{m0}, L_{R1}, V_d, Iin\right)$$

$$\Delta I_{m2} \leftarrow \frac{V_d}{L_m}\cdot\left[\left(D + D_{aux}\right)\cdot T_s - \Delta_1 - \Delta_2\right]$$

$$\left(\Delta I_{m2} + \Delta I_{m4a} + \Delta I_{m5} + \Delta I_{m6}\right)$$

$$I_{m\_pk}(D, I_o, L_{R1}, L_{R2}, L_m, C_{snb}, R_e) := \text{Find}(I_{max})$$

The maximum flux density of the excursion:

$$B_{m\_max}(I_o, D, C_{snb}, L_m, L_{R1}, L_{R2}, C_a, L_a, R_e) := \left| \begin{array}{l} I_{m1} \leftarrow I_{m\_pk}(D, I_o, L_{R1}, L_{R2}, L_m, C_{snb}, R_e) \\ V_d \leftarrow \dfrac{k \cdot \left[V_o + R_e \cdot (I_o)\right] + \dfrac{f_s \cdot L_{R1} \cdot (I_o)}{k}}{D} \\ \omega_3 \leftarrow \dfrac{1}{\sqrt{L_m \cdot C_{snb}}} \\ I_{in2} \leftarrow I_{m1} + \dfrac{I_o}{k} \\ \Delta_{4a} \leftarrow \dfrac{\operatorname{atan}\left(V_d \cdot \omega_3 \cdot \dfrac{C_{snb}}{I_{in2}}\right)}{\omega_3} \\ \Delta I_{m4a} \leftarrow \sin(\Delta_{4a} \cdot \omega_3) \cdot V_d \cdot \omega_3 \cdot C_{snb} \cdots \\ \qquad + \cos(\Delta_{4a} \cdot \omega_3) \cdot I_{in2} - I_{in2} \\ (I_{m1} + \Delta I_{m4a}) \cdot L_m \cdot \dfrac{\text{Gauss}}{m^2} \cdot \sqrt{\dfrac{L_{mnm}}{L_m}} \end{array} \right.$$

The ac flux swing range:

$$\Delta B_{m2}(D, L_m, I_o, R_e) := \frac{\dfrac{k \cdot \left[V_o + R_e \cdot (I_o)\right] + \dfrac{f_s \cdot L_{R1} \cdot (I_o)}{k}}{D}}{L_m} \cdot (D) \cdot \frac{L_m}{f_s} \cdot \text{Gauss} \cdot \sqrt{\frac{L_{mnm}}{L_m}}$$

Part II The Second DPUPS

$L_{R1} := 3 \cdot \mu H$ $C_{snb} := 11 \cdot nF$ $I_o := 0\,A, 0.1\,A .. 10\,A$ $I_{max} := 0.16\,A$

$L_m := 360 \cdot \mu H$ $R_e := 0.1 \cdot \Omega$

Guess $t_4 := 0.1 \cdot 10^{-6}\,s$

Given

$t_4 < 1 \cdot \left(10^{-6}\,s\right)$ $t_4 > 0 \cdot s$

$$\left(1 + \sqrt{\frac{L_{R1}}{L_{R2}}}\right) \cdot V_d = V_d - V_d \cdot \cos\left(\omega_2 \cdot t_4\right) + \frac{I_{max} + \frac{I_o}{k} + \frac{k \cdot R_e \cdot \left(I_{omax} - I_o\right) + \frac{f_s \cdot L_{R1} \cdot \left(I_{omax} - I_o\right)}{k}}{L_{R1} \cdot f_s}}{\omega_2 \cdot C_{snb}} \cdot \sin\left(\omega_2 \cdot t_4\right)$$

$\Delta t_4\left(I_o, I_{max}, L_{R1}, L_{R2}, L_m, C_{snb}, R_e, \omega_2, \omega_3, V_d\right) := \text{Find}\left(t_4\right)$

$$\delta\left(D, I_o, I_{max}, LR1, LR2, L_m, C_{snb}, R_e, \omega 2, \omega 3, Vd, \Delta 4, \Delta 6\right) := \left| \begin{array}{l} I_{in\_pk} \leftarrow I_{max} + \frac{I_o}{k} + \frac{D \cdot Vd - V_o \cdot k - R_e \cdot I_o \cdot k - \frac{f_s \cdot LR1 \cdot I_o}{k}}{LR1 \cdot f_s} \\ I_{LR1\_end} \leftarrow C_{snb} \cdot \left(Vd \cdot \sin(\omega 2 \cdot \Delta 4) \cdot \omega 2 + \frac{I_{in\_pk}}{C_{snb}} \cdot \cos(\omega 2 \cdot \Delta 4)\right) \\ \Delta t_5 \leftarrow \frac{LR2}{Vd} \cdot \sqrt{\frac{LR1}{LR2}} \cdot \left(I_{LR1\_end} - I_{max}\right) \\ I_{m5} \leftarrow I_{max} \cdot \cos\left(\Delta t_5 \cdot \omega 3\right) \\ V5 \leftarrow \frac{I_{max}}{\left(C_{snb} \cdot \omega 3\right)} \cdot \sin\left(\omega 3 \cdot \Delta t_5\right) + \left(1 + \sqrt{\frac{LR1}{LR2}}\right) \cdot Vd \\ V_0 \leftarrow (V5 - Vd) \cdot \cos(\omega 3 \cdot \Delta 6) + \frac{I_{m5}}{\left(C_{snb} \cdot \omega 3\right)} \cdot \sin(\omega 3 \cdot \Delta 6) + Vd \\ \frac{V_0 - Vd}{Vd} \end{array} \right.$$

$$u_{d1}(t, D, Io, I_{m0}, Imax, LR1, LR2, Lm, C, Re, \omega 2, \omega 3, Vd, \Delta 4, \Delta 6) :=$$

$$\alpha 1 \leftarrow L_a \cdot C_a \cdot LR1 \cdot C$$

$$\beta \leftarrow LR1 \cdot (C + C_a) + L_a \cdot C_a$$

$$\omega 12 \leftarrow \sqrt{\frac{\beta + \sqrt{\beta^2 - 4 \cdot \alpha 1}}{2 \cdot \alpha 1}}$$

$$\omega 11 \leftarrow \sqrt{\frac{\beta - \sqrt{\beta^2 - 4 \cdot \alpha 1}}{2 \cdot \alpha 1}}$$

$$\delta\delta \leftarrow \delta(D, Io, Imax, LR1, LR2, Lm, C, Re, \omega 2, \omega 3, Vd, \Delta 4, \Delta 6)$$

$$M \leftarrow \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & \omega 11 \cdot s & 0 & \omega 12 \cdot s \\ -(\omega 11 \cdot s)^2 & 0 & -(\omega 12 \cdot s)^2 & 0 \\ 0 & -(\omega 11 \cdot s)^3 & 0 & -(\omega 12 \cdot s)^3 \end{bmatrix}^{-1}$$

$$Vector \leftarrow \begin{bmatrix} \delta\delta \cdot \frac{Vd}{V} \\ \frac{I_{m0} \cdot F}{C \cdot A} \\ \frac{-(1 + \delta\delta) \cdot \frac{(L_a + LR1) \cdot Vd}{V \cdot H} + \frac{Vd \cdot L_a}{V \cdot H}}{\frac{LR1 \cdot L_a \cdot C}{H \cdot H \cdot F}} \\ -\frac{I_{m0} \cdot F}{C \cdot A} \cdot \frac{\frac{(L_a + LR1)}{H}}{\frac{LR1 \cdot L_a \cdot C}{H \cdot H \cdot F}} \end{bmatrix}$$

$$a \leftarrow M \cdot Vector$$

$$Vd + \left(\begin{matrix} a_1 \cdot \cos(\omega 11 \cdot t) + a_2 \cdot \sin(\omega 11 \cdot t) \ \ldots \\ + a_3 \cdot \cos(\omega 12 \cdot t) + a_4 \cdot \sin(\omega 12 \cdot t) \end{matrix} \right) \cdot V$$

$t_1 := 0\,s$ *

Given

$t1 > 0\,s \qquad t1 < 0.5 \cdot 10^{-6}\,s$

$u_{d1}(t1, D, I_o, I_{m0}, I_{max}, L_{R1}, L_{R2}, L_m, C_{snb}, R_e, \omega_2, \omega_3, V_d, \Delta tt_4, \Delta t_6) = 0 \cdot V$

$\Delta t_1(D, I_o, I_{m0}, I_{max}, L_{R1}, L_{R2}, L_m, C_{snb}, R_e, \omega_2, \omega_3, V_d, \Delta tt_4, \Delta t_6) := \text{Find}(t1)$

$$i_{in}(D,a,b,c,d,e,f,g,h,i,j,k,l,m) := \left| \begin{array}{l} \Delta t \leftarrow \Delta t_1(D,a,b,c,d,e,f,g,h,i,j,k,l,m) \\ \dfrac{1}{L_{R1}} \cdot \displaystyle\int_0^{\Delta t} \left(k - u_{d1}(tt,D,a,b,c,d,e,f,g,h,i,j,k,l,m)\right) d\,tt + b \end{array} \right.$$

$$\Delta t_2(D, I_o, I_{m0}, Imax, L1, L2, L, C, R, \omega 2, \omega 3, Vd, \Delta 4, \Delta 6) := \left| \begin{array}{l} Iin \leftarrow i_{in}(D, I_o, I_{m0}, Imax, L1, L2, L, C, R, \omega 2, \omega 3, Vd, \Delta 4, \Delta 6) \\ \dfrac{\frac{I_o}{k} - Iin + I_{m0}}{Vd} \cdot L1 \end{array} \right.$$

Guess $I_{max} = 0.16\ A$

Given

$\Delta I_{m1} \leftarrow 0\ A$ $= 0 \cdot A$

$\Delta I_{m3} \leftarrow 0\ A$

$\Delta I_{m4} \leftarrow 0\ A$

$\omega_2 \leftarrow \frac{1}{\sqrt{L_{R1} \cdot C_{snb}}}$

$\omega_3 \leftarrow \frac{1}{\sqrt{L_m \cdot C_{snb}}}$

$V_d \leftarrow \frac{k \cdot \left(V_o + R_e \cdot I_{omax} + \frac{f_s \cdot L_{R1} \cdot I_{omax}}{k \cdot k}\right)}{D}$

$\Delta_4 \leftarrow \Delta t_4\left(I_o, I_{max}, L_{R1}, L_{R2}, L_m, C_{snb}, R_e, \omega_2, \omega_3, V_d\right)$

$d \leftarrow \frac{R_e \cdot k + \frac{f_s \cdot L_{R1}}{k}}{V_d} \cdot \left(I_{omax} - I_o\right)$

$I_{in\_pk} \leftarrow I_{max} + \frac{I_o}{k} + \frac{d \cdot V_d}{L_{R1} \cdot f_s}$

$I_{LR1\_end} \leftarrow C_{snb} \cdot \left(V_d \cdot \sin\left(\omega_2 \cdot \Delta_4\right) \cdot \omega_2 + \frac{I_{in\_pk}}{C_{snb}} \cdot \cos\left(\omega_2 \cdot \Delta_4\right)\right)$

$\Delta_5 \leftarrow \frac{L_{R1}}{V_d} \cdot \left(I_{LR1\_end} - I_{max}\right)$

$\Delta I_{m5} \leftarrow I_{max} \cdot \left(\cos\left(\omega_3 \cdot \Delta_5\right) - 1\right)$

$\Delta_6 \leftarrow \left(1 - D - D_{aux}\right) \cdot T_s - \Delta_4 - \Delta_5$

$I_{m5} \leftarrow I_{max} + \Delta I_{m5}$

$V_{ds\_5} \leftarrow \frac{I_{max}}{\left(C_{snb} \cdot \omega_3\right)} \cdot \sin\left(\omega_3 \cdot \Delta_5\right) + 2 \cdot V_d$

$\Delta I_{m6} \leftarrow \sin\left(\Delta_6 \cdot \omega_3\right) \cdot \omega_3 \cdot C_{snb} \cdot \left(V_d - V_{ds\_5}\right) + I_{m5} \cdot \left(\cos\left(\Delta_6 \cdot \omega_3\right) - 1\right)$

$I_{m0} \leftarrow I_{max} + \Delta I_{m5} + \Delta I_{m6}$

$\Delta_2 \leftarrow \Delta t_2\left(D, I_o, I_{m0}, I_{max}, L_{R1}, L_{R2}, L_m, C_{snb}, R_e, \omega_2, \omega_3, V_d, \Delta_4, \Delta_6\right)$

$\Delta_1 \leftarrow \Delta t_1\left(D, I_o, I_{m0}, I_{max}, L_{R1}, L_{R2}, L_m, C_{snb}, R_e, \omega_2, \omega_3, V_d, \Delta_4, \Delta_6\right)$

$\Delta I_{m2} \leftarrow \frac{V_d}{L_m} \cdot \left[\left(D + D_{aux} - d\right) \cdot T_s - \Delta_1 - \Delta_2\right]$

$\left(\Delta I_{m1} + \Delta I_{m2} + \Delta I_{m3} + \Delta I_{m4} + \Delta I_{m5} + \Delta I_{m6}\right)$

$I_{m\_pk}\left(D, I_o, L_{R1}, L_{R2}, L_m, C_{snb}, R_e\right) := \text{Find}\left(I_{max}\right)$

The maximum flux density of the excursion:

$$B_{m\_max}(I_o, D, C_{snb}, L_m, L_{R1}, L_{R2}, C_a, L_a, R_e) := I_{m\_pk}(D, I_o, L_{R1}, L_{R2}, L_m, C_{snb}, R_e) \cdot L_m \cdot \frac{Gauss}{m^2} \cdot \sqrt{\frac{L_{mnm}}{L_m}}$$

The ac flux excursion range:

$$\Delta B_m(D, L_m, I_o, R_e) := \frac{k \cdot \left(V_o + R_e \cdot I_{omax} + \frac{f_s \cdot L_{R1} \cdot I_{omax}}{k \cdot k}\right)}{\frac{D}{L_m}} \cdot \left[D - \frac{\left(V_o + R_e \cdot I_o + \frac{f_s \cdot L_{R1} \cdot I_o}{k \cdot k}\right)}{\left(V_o + R_e \cdot I_{omax} + \frac{f_s \cdot L_{R1} \cdot I_{omax}}{k \cdot k}\right)} \right] \cdot \frac{L_m}{f_s} \cdot \frac{Gauss}{m^2} \cdot \sqrt{\frac{L_{mnm}}{L_m}}$$

APPENDIX G

IMPLEMENTATION OF THE PULSE SPLITTER

A pulse splitter is originally developed in [106], and it is used in the prototype DPUPSs to generate the fixed pulse-width gating pattern for the auxiliary switch.

Fig. G.1 shows an implementation of the pulse splitter circuit, and Fig. G.2 shows key waveforms at the different points of the circuit.

The splitter consists of a Schmitt trigger, an Opamp, two inverters and two AND gates. The fixed duty cycle for the auxiliary switch can be adjusted by the time constant of the R_B-C_B network.

In Fig. G.2, V_F and V_E appear to have the same wave shape. Thus, the AND gate between point E and F seems unnecessary. However, this gate is to match the delay times in the two branches such that the two signals at the outputs of the splitter have accurate timing sequence.

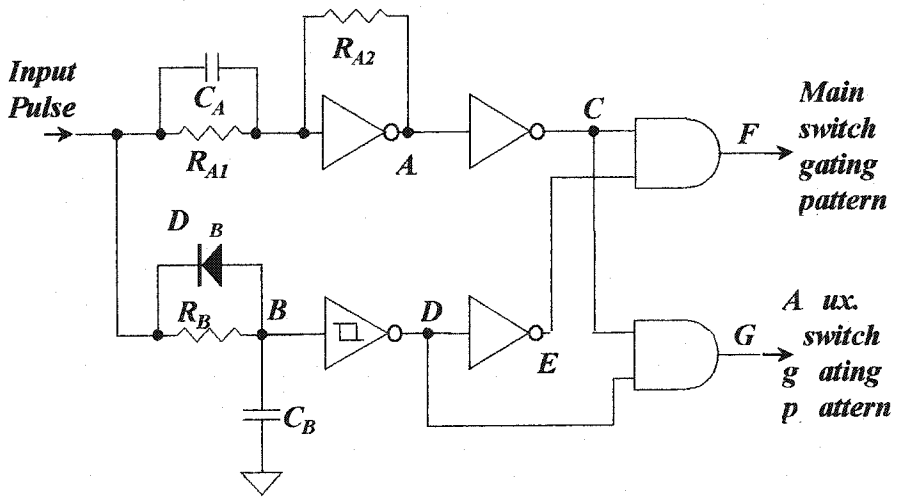


Fig. G.1 The pulse splitter circuit.

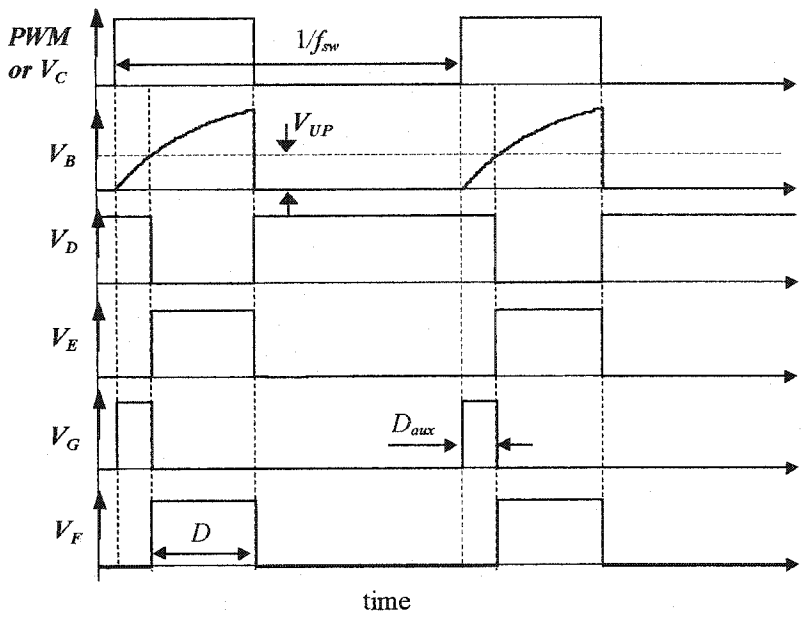


Fig. G.2 Key waveforms in the splitter.

The design guideline of the splitter is given below.

A. Selection of R_B, C_B and D_B

The duty cycle of the auxiliary switch can be set by R_B and C_B. The following equation should be satisfied

$$V_{UP} = V_{PWM}[1 - \exp(-\frac{D_{aux}}{f_{sw} R_B C_B})] \tag{G-1}$$

where V_{PWM} is the high level voltage of the input PWM pulses generated by the Comparator in Fig. 4.14.

From (G-1), the selection of R_B and C_B shall satisfy the following equation:

$$R_B C_B = -\frac{D_{aux}}{f_{sw} \ln(1 - \frac{V_{UP}}{V_{PWM}})} \tag{G-2}$$

The diode D_B is introduced to follow the fast drop of PWM signals. It should be a small current rated Schottky or fast diode.

B The voltage divider, R_{A1} and R_{A2}

Assume the high output voltage level of the logic circuit is V_{OH}. The input PWM with a higher level of V_{PWM} should be converted to the logic circuit voltage level through an interface buffer circuit. The gain of the buffer shall observe the following equation:

$$\frac{R_{A2}}{R_{A1}} = \frac{V_{OH}}{V_{PWM}} \tag{G-3}$$

An additional capacitor C_A is introduced to match the stray impedance of the circuit to reduce distortion of the waveform. C_A value can be selected experimentally.

C. The selection of the logic gates and the driver

All the logic gates should be capable of high speed response. The example splitter given below uses CMOS logic circuits of 74HC00 series, and it performs satisfactorily for switching frequencies up to a few MHz.

D. A design example

Table G.1 shows the parameters of an example splitter for switching frequency of 200kHz. The desired D_{aux} is about 8% of the switching cycle.

Table G.1 The parameters of the example splitter

Component/Device	Selection	Component/Device	Selection
R_{A1}	180 kΩ	D_B	IN4148
R_{A2}	91 kΩ	Inverters*	TC74HC04P
C_A	0.22 μF	AND gate	MC74HC08A
R_B	2.2 kΩ	C_B	500 nF

* The Schmitt trigger and Opamp are substituted with inverters in the example.

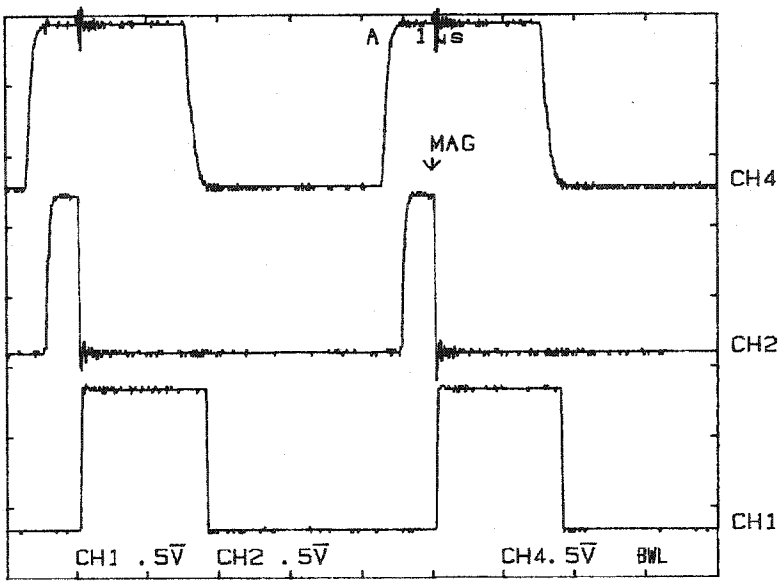


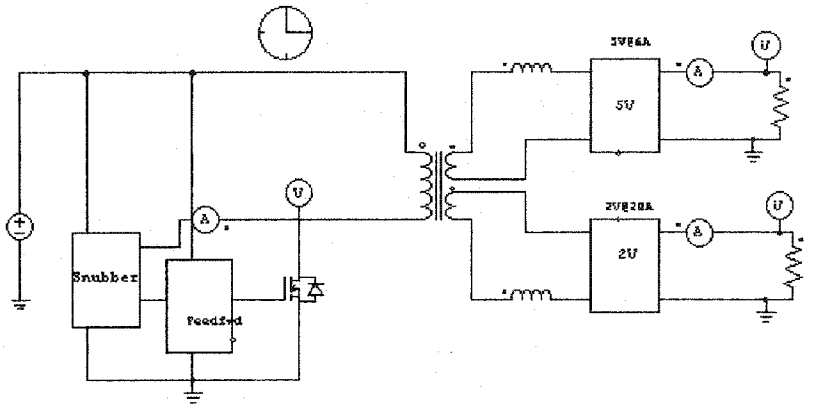
Fig. G.3 The experimental results of the gating patterns generated by the splitter.. Traces: CH1- gate drive for main switch S_{main}; CH2-gate drive for auxiliary switch S_{aux}; CH4-input pulse

Fig. G.3 shows the experimental results of the gating signals to verify the design. The output of the drivers are displayed herein instead of showing the split logic signal. IR2110s are used to drive both S_{main} and S_{aux}. However, the 200ns delay of IR2110 limits the applicable switching frequency to be lower than 400kHz. For a higher switching frequency, the MOSFET type push-pull gate-drive buffer circuits shall be used to drive the switches.

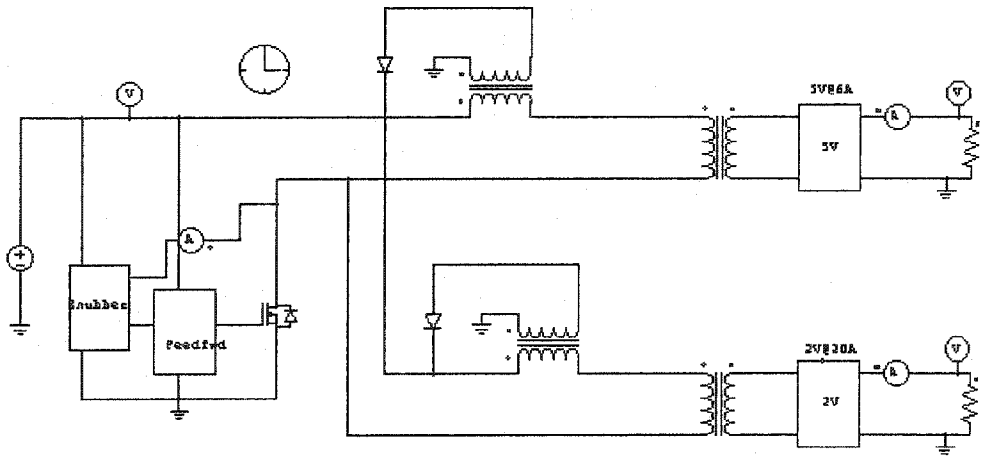
APPENDIX H

PSIM MODELS OF THE DPUPS ARCHITECTURES

Fig. H1a shows the Psim model of the DPUPS implemented with the Type 1 converter topology, and Fig. H1b shows the model of the DPUPS implemented with the Type 2 topology. The sub-circuits are shown in the Fig. H2.

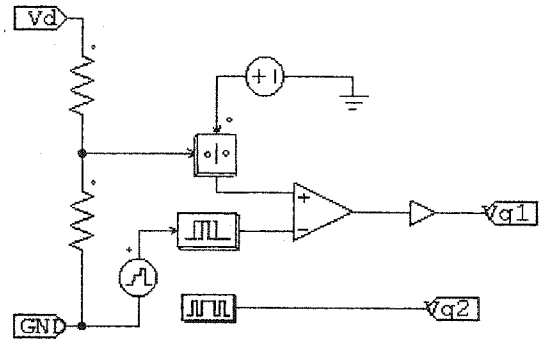


a. The DPUPS architecture implemented with the Type 1 converter topology.

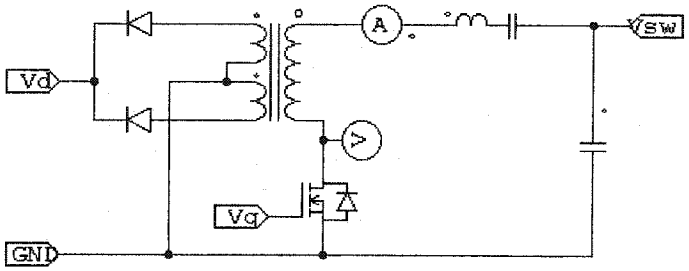


b. The DPUPS architecture implemented with the Type 2 converter topology.

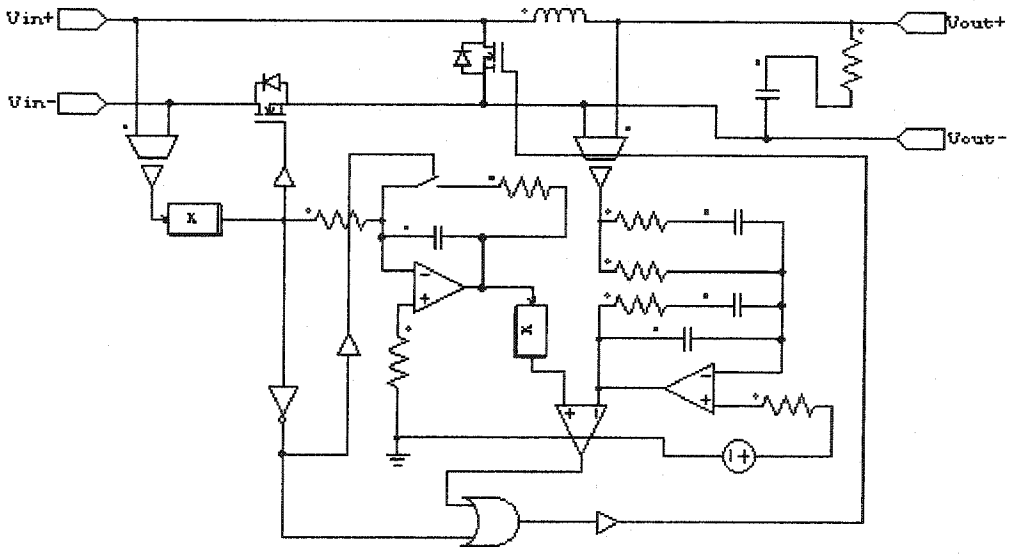
Fig. H1 The Psim model of the DPUPS architectures.



a. The voltage feed-forward controller.



b. The resonant auxiliary circuit.



c. The output circuit with feedback control.

Fig. H1 The Psim models of the sub-circuits.

APPENDIX I

PSPICE MODELS OF THE PROPOSED ZVS CONVERTER TOPOLOGIES

I.1 THE PSPICE MODEL OF THE TYPE 1 CONVERTER TOPOLOGY

```
.PARAM        fsw=200kHz
.PARAM        Lo={(Vo-2)/3*30uH+(5-Vo)/3*3.8uH}    Co={(Vo-2)/3*160uF+(5-
Vo)/3*500uF} Ls={Lm/(k*k)}
.PARAM        d={(k*Rs*(Iomax-Io)/Vin+fsw*Lss*k/(Vin)*(Iomax-Io)*0+0.0)}
.PARAM        k={(Vo-2)/3*3+(5-Vo)/3*7.5}  Lm=360uH  Rs={(Vo-2)/3*20m+(5-
Vo)/3*4.8m*2}
.PARAM         Vin=40V    Iomax={(Vo-2)/3*20A+(5-Vo)/3*12A}    Lss={(Vo-
2)/3*0.3uH+(5-Vo)/3*0.1uH}
.PARAM        DUTY={(k*(Vo+Rs*Io)+fsw*Lss*k*Io)/Vin-0.08} Daux=0.12
.PARAM        Vo=5V Io=5A Ro={Vo/Io}
*
** Analysis setup **
.tran 50ns 400u 390u SKIPBP
.OP
*
*     From     [PSPICE     NETLIST]     section     of     C:\Program
Files\Orcad\PSpice\PSpice.ini:
.lib "C:\My Documents\simulation\Spice_models\Mosfet_additional.lib"
.lib "nom.lib"
.INC "flux_1st_fwd_single_op_SR.net"
**** INCLUDING flux_1st_fwd_single_op_SR.net ****
* Schematics Netlist *
D_D5          $N_0001 $N_0002 MUR860
D_D4          $N_0003 $N_0002 MUR860
Kn_K3          L_Lap L_Las1
+ L_Las2    1
R_R3          $N_0002 $N_0004  10m
R_R5          $N_0006 $N_0005  10
R_R6          $N_0007 0  1k
V_V3          $N_0007 0
+PULSE   0   10   {DUTY/fsw+0.85*Daux/fsw+50ns-d/fsw}   50n   50n   {(1-
DUTY+d)/fsw-100ns}
+  {1/fsw}
Kn_K4          L_Lo L_Lg4     1
L_Lg4         $N_0008 $N_0009  {4*Lo}
R_R7          $N_0010 $N_0009  10
R_R8          $N_0012 $N_0011  10
V_V1          $N_0002 0 {Vin}
D_D8           0 $N_0013 MUR860
V_V6          $N_0014 0
+PULSE 0 10 0 50n 50n {Daux/fsw} {1/fsw}
L_Las1        $N_0001 0  250uH
L_Las2         0 $N_0003  250uH
```

```
L_Lap          $N_0015 $N_0013  5uH
C_C3           $N_0016 $N_0017  66nF
R_R9           $N_0017 $N_0018  1m
L_Lp           $N_0004 $N_0017  {Lm}
D_D9           $N_0013 $N_0019 MBD701
M_Saux         $N_0019 $N_0014 0 0 IRF634
Kn_K1          L_Lp L_Ls
+ L_Lg1 L_Lg3   0.9999
M_Smain        $N_0018 $N_0020 0 0 IRF640
C_C2           $N_0017 0  16nF
L_Lo           $N_0021 $N_0022  {Lo}
L_Lss          $N_0023 0  {Lss}
C_Co           $N_0022 0  {Co}
R_Rload        $N_0022 0  {Ro}
D_D6            0 $N_0008 MBD701
M_M8           $N_0010 $N_0011 0 0 IRF510
L_Lg3          $N_0012 0  {Lm/25}
M_M6           $N_0024 $N_0005 $N_0024 $N_0024 IRFZ44
L_Lg1          $N_0006 $N_0024  {Lm/25}
L_Ls           $N_0024 $N_0023  {Ls}
X_D2           $N_0024 0 $N_0021 MBR2045CT
M_M7            0 $N_0010 0 0 IRFZ44
V_V2           $N_0020 0
+PULSE 0 10 {0.085/fsw} 50n 50n {DUTY/fsw} {1/fsw}
L_L7           $N_0015 $N_0016  2uH
*
**** RESUMING flux_1st_fwd_single_op_SR.cir ****
.PROBE V(*) I(*) D(*) NOISE(*)
.END
```

I.2 THE PSPICE MODEL OF THE TYPE 2 CONVERTER TOPOLOGY

```
.PARAM        Lo={(Vo-2)/3*30uH+(5-Vo)/3*3.8uH}    Co={(Vo-2)/3*160uF+(5-
Vo)/3*500uF} Ls={Lm/(k*k)}
.PARAM        DUTY={(k*(Vo+Rs*Iomax)+fsw*LR1/k*Iomax)/Vin} Daux=0.1
.PARAM        d={k*Rs*(Iomax-Io)/Vin+fsw*LR1/(k*Vin)*(Iomax-Io)*1}
.PARAM        fsw=300kHz
.PARAM        k={(Vo-2)/3*3+(5-Vo)/3*7.5}  Lm=353uH  Rs={(Vo-2)/3*50m+(5-
Vo)/3*4.8m*2}
.PARAM        Vin=55V Iomax={(Vo-2)/3*10A+(5-Vo)/3*20A} LR1=6uH
.PARAM        Vo=5V Io=0 Ro={Vo/Io}
*
** Analysis setup **
.tran 200ns 300u 290u SKIPBP
.OP
*
*
*     From     [PSPICE     NETLIST]     section     of     C:\Program
Files\Orcad\PSpice\PSpice.ini:
.lib "C:\My Documents\simulation\Spice_models\Mosfet_additional.lib"
.lib "nom.lib"
*
.INC "2nd_fwd_c.net"
*
```

```
**** INCLUDING 2nd_fwd_c.net ****
* Schematics Netlist *
*
X_D2          $N_0001 0 $N_0002 MBR2045CT
D_D3          $N_0003 $N_0004 MBR320
D_D1           0 $N_0003 MUR860
M_Smain       $N_0006 $N_0005 0 0 IRF640
L_Lg1         $N_0007 $N_0001  {Lm/25}
R_R5          $N_0007 $N_0008  10
L_Lp          $N_0009 $N_0010  {Lm}
R_Rload       $N_0011 0  {Ro}
L_LR1         $N_0012 $N_0013  {LR1}
L_LR2         $N_0004 $N_0014  {LR1}
Kn_K2          L_LR1 L_LR2     1
R_R3          $N_0013 $N_0009  10m
L_Ls          $N_0001 0  {Ls}
V_V1          $N_0012 0 {Vin}
R_R4          $N_0014 $N_0012  10m
D_D5          $N_0015 $N_0012 MUR860
L_L7          $N_0016 $N_0017  2uH
R_R2          $N_0010 $N_0006  10m
C_C3          $N_0017 $N_0010  66nF
D_D4          $N_0018 $N_0012 MUR860
L_Las1        $N_0015 0  100uH
L_Las2         0 $N_0018  100uH
M_M7          $N_0002 $N_0019 0 0 IRFZ44
M_M6          $N_0002 $N_0008 $N_0001 $N_0001 IRFZ44
V_V2          $N_0005 0
+PULSE 0 10 {0.85*Daux/fsw} 50n 50n {DUTY/fsw} {1/fsw}
V_V3          $N_0019 0
+PULSE   0   10   {DUTY/fsw+0.85*Daux/fsw+50ns-d/fsw}   50n   50n   {(1-
DUTY+d)/fsw-100ns}
+  {1/fsw}
L_Lo          $N_0002 $N_0011  {Lo} IC={Io}
C_Co          $N_0011 0  {Co} IC={Vo}
Kn_K1          L_Lp L_Ls
+ L_Lg1    1
Kn_K3          L_Lap L_Las1
+ L_Las2    1
V_V6          $N_0020 0
+PULSE 0 10 0 50n 50n {Daux/fsw} {1/fsw}
L_Lap          $N_0016 $N_0021  5uH
D_D6          $N_0021 $N_0022 MBR320
M_Saux          $N_0022 $N_0020 0 0 IRF634
D_D7          0 $N_0022 MUR860
C_C2          $N_0006 0  5nF
**** RESUMING 2nd_fwd_c.cir ****
.PROBE V(*) I(*) D(*) NOISE(*)
.END
```