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**DESIGN AND IMPLEMENTATION OF THREE-PHASE  
FOUR-WIRE ACTIVE FILTERS**

**Kévork Haddad**

**A Thesis  
in  
The Department  
of  
Electrical and Computer Engineering**

**Presented in Partial Fulfillment of the requirements  
for the Degree of Master of Applied Science at  
Concordia University  
Montreal, Quebec, Canada.**

**November 1996**

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## **ABSTRACT**

# **DESIGN AND IMPLEMENTATION OF THREE-PHASE FOUR-WIRE ACTIVE FILTERS**

Kévork Haddad

Concordia University, 1996.

The widespread use of power electronics in all types of industrial, commercial and even residential electrical equipment is causing the deterioration of the quality of the electric supply through distortion of the supply voltage. This has led to the development of more stringent requirements regarding harmonic current generation, as are found in standards such as IEEE-519. Passive filters have been used to limit the flow of harmonic currents in distribution systems. However, these tend to be bulky and the design is complex, particularly if the number of harmonic components to be reduced increases. With improvements in power electronic devices and conversion techniques, an innovative concept, the active power filter, has recently been proposed and investigated. Voltage source structures in particular present excellent performance characteristics in three phase configurations. However, in a number of installations, four-wire systems are used. Furthermore, if the three phase load is unbalanced, neutral currents flow and the three phase three-wire active filter cannot adequately eliminate harmonics. This thesis deals with active filters for the general case of three phase four-wire systems. The proposed filter uses three independent current controllers acting on half-bridge inverters. The PWM pattern is generated using a constant frequency ramp comparison technique. A detailed analytical study is presented to design the power circuit in order to ensure operation in single phase and unbalanced load conditions. The quality of the supply current, the magnitude and components of the neutral current and the filter bandwidth are investigated. The theoretical considerations are verified by simulation and by experiments on a industrial prototype. Results demonstrate that the active filter is a viable and a potentially economical solution to mitigating harmonics in distribution power systems.

## **ACKNOWLEDGMENTS**

I wish to express my sincere gratitude to my supervisor, Dr. Géza Jóos, for his valuable support, advice and guidance throughout the course of my research.

I am also grateful to Professor Alain Jaafari and Mr. Thierry Thomas, from the Laboratoire d'Electronique Industrielle, E.I.V.L., Blois, France, for sharing their practical experience.

Thanks are extended to my friends in the Power Electronics Lab, who made the period of my research more pleasant and fruitful. Special thanks to Mr. José Espinoza and Mr. Ali Reza Bakhshai for many helpful discussions we shared.

Financial support from Québec Ministry of Education (FCAR) is gratefully acknowledged, particularly for financing a three month stay at the Laboratoire d'Electronique Industrielle (summer 1995) and the National Sciences and Engineering Research Council (NSERC).

To my father, Hagop.



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## LIST OF PRINCIPAL SYMBOLS

$A_r$	Amplitude of the ripple component
$BW$	Current loop bandwidth
$C$	Active filter capacitor
$C_i$	Current controller transfer function
$d$	Ratio of rate of rise currents
$E$	Energy stored in the capacitor
$f$	Fundamental frequency
$f_b$	Frequency width of the filter passing band
$f_c$	Cut-off frequency
$f_{jn}$	High order frequency
$f_h$	Low order frequency
$f_{sw}$	Switching frequency
$F$	Extraction circuit transfer function
$F_b$	Band pass filter transfer function
$G_c$	Modulator transfer function
$h$	Harmonic order
$H$	Harmonic or distorting power

$HD_v$	Individual harmonic voltage distortion
$H_v$	Voltage open loop transfer function
$I_1$	Fundamental load current
$I_1'$	Active filter fundamental current
$i_j$	Load current in line j (j = a, b and c )
$i_{j,1}$	Load fundamental current in line j (j = a, b and c)
$i_{j,h}$	Load distorting current in line j (j = a, b and c)
$i_{af}$	Active filter current
$i_{af,j}$	Active filter current in line j (j = a, b and c)
$i_{af,N}$	Active filter current in the fourth wire
$i_{dc1}$	Upper capacitor dc current
$i_{dc2}$	Lower capacitor dc current
$i_{load}$	Load current
$i_N$	Load side neutral current
$i_s$	Supply current
$i_{s,j}$	Supply current in line j (j = a, b, and c)
$I_{sc}$	Short circuit current at PCC
$i_{s,N}$	Supply side neutral current
$k$	Current controller proportional term
$k_v$	Voltage controller proportional term
$L_{af}$	Active filter inductor
$L_s$	Supply impedance

$m_0$	No load modulation index
$m$	Modulation index at full load
$P$	Real power
$Q$	Reactive power
$R_{losses}$	Losses of the active filter
$r_v$	Dc voltage regulation ratio
$s$	Laplace operator
$S$	Apparent Power
$t_{off}$	Off time of a switch
$t_{on}$	On time of a switch
$T_{sw}$	switching period
$v_{af}$	Active filter output voltage
$v_{cont}$	Modulating signal
$V_{dc}$	Dc bus voltage
$\tilde{V}_{dc}$	Dc bus fluctuating voltage
$V_{dc1}$	Upper capacitor dc voltage
$V_{dc2}$	Lower capacitor dc voltage
$\tilde{V}_{dc1}$	Upper capacitor fluctuating voltage
$\tilde{V}_{dc2}$	Lower capacitor fluctuating voltage
$V_s$	Supply voltage (line to neutral)
$V_{tri}$	Triangular wave amplitude

$\omega$	Fundamental angular frequency
$\omega_0$	Natural undamped frequency
$\omega_r$	Angular frequency of the ripple component
$\Delta E$	Energy variation across the capacitor
$\Delta i$	Peak to peak ripple current
$\Delta V_{dc}$	Peak to peak dc bus ripple voltage
$\psi_{jn}$	Active filter current phase angle at high frequencies
$\phi_h$	Load current phase angle at low frequencies
$\varphi_r$	Ripple component phase angle
$\tau$	Current controller time constant
$\tau_f$	Low pass filter time constant
$\tau_v$	Voltage controller time constant
$\zeta$	Damping ratio
$\varepsilon_v$	Dc voltage error

## **LIST OF ACRONYMS**

BJT	Bipolar Junction Transistor
EPRI	Electric Power Research Institute
GTO	Gate Turn-Off Thyristor
IEEE	Institute of Electrical and Electronic Engineers
IEC	International Electrical Commission
IGBT	Insulated Gate Bipolar Transistor
PCC	Point of Common Coupling
PI	Proportional-Integral
PWM	Pulse Width Modulated
PSIM	Power Electronic Circuit Simulator
rms	Root Mean Square
THD	Total harmonic distortion
VSI	Voltage Source Inverter

# **Chapter 1**

## **INTRODUCTION**

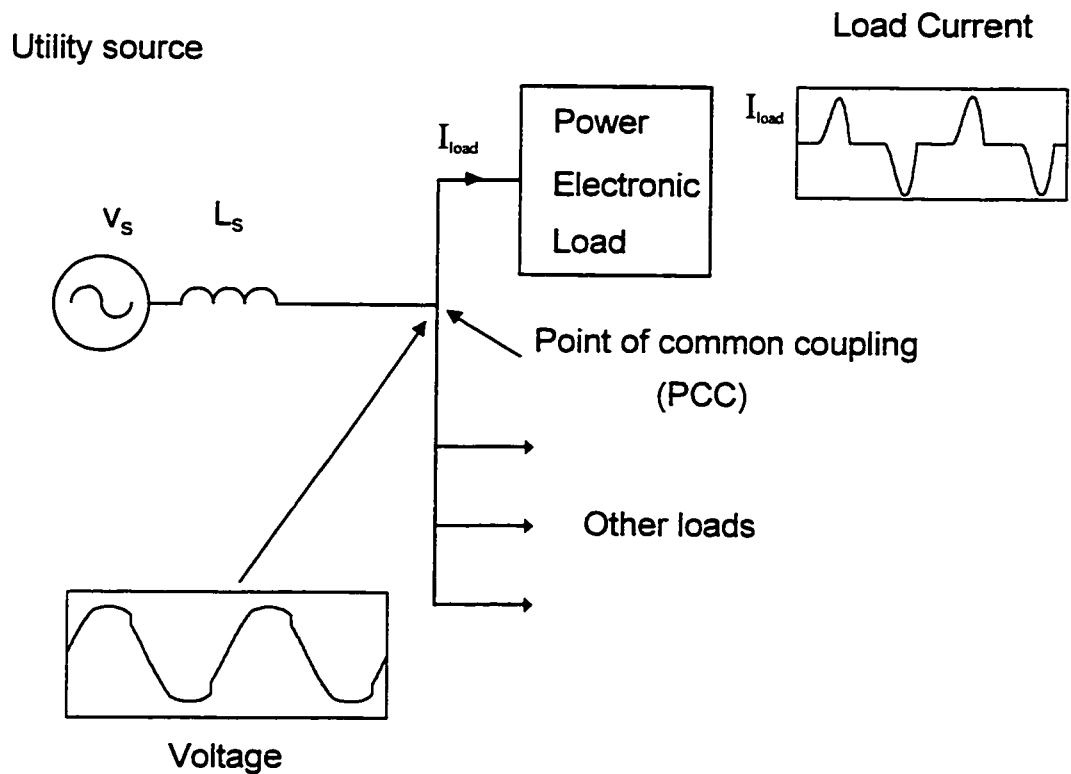
### **1.1 General**

Electric power generated by the utilities is distributed to the consumer in the form of 60 Hz ac voltage. The utilities have a tight control on the design and operation of the equipment used for transmission and distribution, and can therefore keep frequency and voltage delivered to their customers within close limits. Unfortunately, an increasing portion of loads connected to the power system are comprised of power electronic converters. These loads are non linear and inject distorted currents in the network and consequently, through line drops, they generate harmonic voltage waveforms. Power converters such as rectifiers, power supplies and at a higher power level, arc furnaces are all sources of distortion. According to the Electric Power Research Institute (EPRI), in 1995, 35-40% of all electric power flows through electronic converters. This is expected to increase to 60% by the year 2000 [1].

The distortion, whether it is produced by a large single source or by the cumulative effect of many small loads, often propagates for miles along distribution feeders.

As the use of non linear power equipment is spreading, the degradation of the power quality in the utility networks is increasing and is becoming a major problem. Limiting the voltage distortion is therefore a concern for both utilities and consumers. For these reasons international agencies like IEEE and IEC are proposing or enforcing distortion limits [2] [3].

The simple block diagram of Fig. 1.1 illustrates the distortion problem due to harmonic at low and medium power levels.



**Fig. 1.1** Harmonic distortion at PCC.



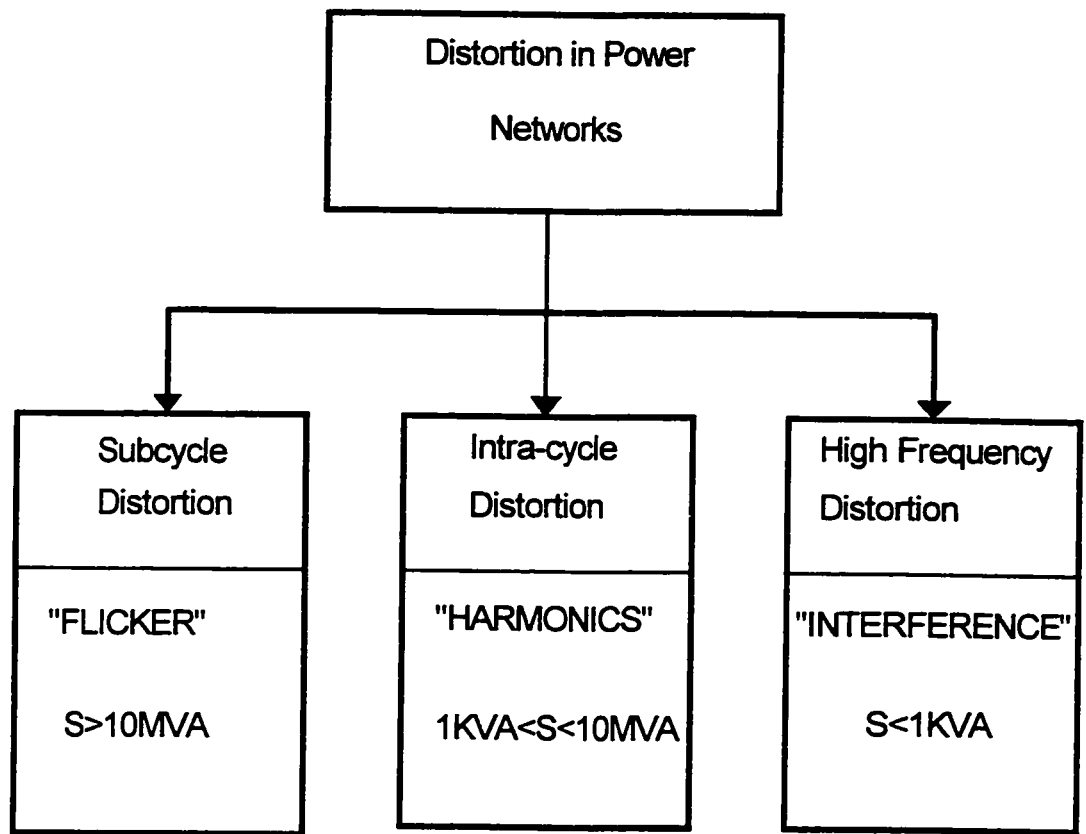
The utility is represented by an ideal ac voltage source in series with a lumped impedance representing lines and transformers. The voltage waveform at the point of common coupling is distorted due to harmonic current generated by the power electronic load or the non-linear load. This results in the following effects on the power system components :

- (i) Malfunction of harmonic sensitive loads;
- (ii) Increased losses in parallel connected capacitors, transformers, and motors;
- (iii) Improper operation of protection relays and circuit breakers.

## **1.2 Distortions in Power Networks**

As shown in Fig. 1.2, the different sources of distortion in power networks conveniently can be divided into three classes according to the power level of the equipment and frequency range [4]: (a) sub-cycle distortion give rise to flicker and occur generally at the highest power level, they are caused by dynamic loads, such as arc furnaces, mill drives, mine winders, (b) high frequency distortion is caused by modern power electronic equipment, due to high rate of rise of current and voltage, and (c) intra-cycle distortion which covers a very wide range of power, and results from the power processing technique. The distortion generated by these last sources is usually termed “harmonics”.

This work focuses on distortion caused by harmonics.



**Fig. 1.2** Classification of distortion types in power networks.

### **1.3 Harmonic Standards and Recommended Practices.**

In view of the proliferation of the power electronic equipment connected to the utility distribution system, various international agencies have proposed limits on the magnitude of harmonic current injected into the supply to maintain acceptable power quality. The resulting guidelines and standards specify limits on the magnitudes of harmonic currents and harmonic voltage distortion at various harmonic frequencies. The most widely known are the IEEE-519 guidelines [2] in North America and the IEC-1000

Standard (formerly IEC 555) [3] prepared by the International Electrical Commission (in effect since 1996). However, the approach taken in these documents is drastically different. The IEC Standard imposes limits on individual equipment (up to 15 A, 220 V) connected to the supply, whereas the IEEE Recommended Practice addresses the issue of harmonic distortion at the point of common of coupling (PCC). Complying with the IEC Standard usually requires special design of the equipment itself [5] [6] [7]. However, meeting the IEEE guidelines can be achieved by means of filters, particularly active filters. Therefore, reference in this work will only be made to the IEEE guideline.

IEEE 519 proposes to designers of industrial plants harmonic limits as given in Table 1.1 and 1.2. For existing installations, harmonic mitigation techniques may have to be used to reduce distortion to the specified limits.

**Table 1.1 IEEE-519 Maximum odd-harmonic current distortion.**

**% Limits of Harmonic Currents ( Bus voltage @ PCC<69 KV)**

$I_{SC}/I_1$	$h<11$	$11<h<17$	$17<h<23$	$23<h<35$	$35<h$	THD
<20	4.0	2.0	1.5	0.3	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Notes: 1  $I_{SC}$  is the maximum short-circuit current @PCC.

2  $I_1$  is the maximum fundamental frequency load current@PCC.

**Table 1.2 IEEE-519 Voltage distortions limits**

Bus Voltage @PCC	HDv(%)	THDv(%)
69 KV and below	3.0	5.0

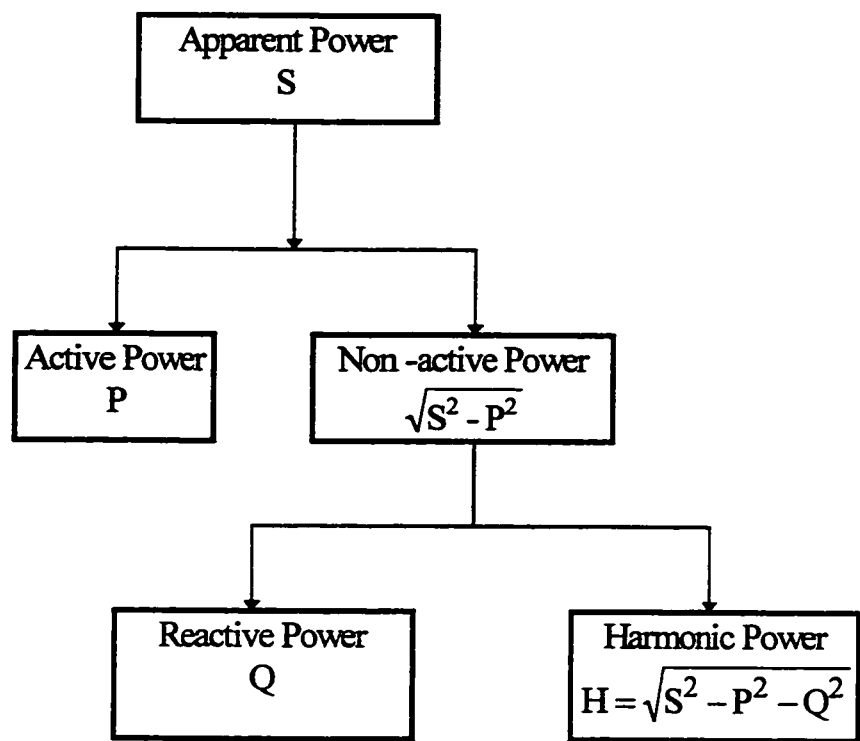
HDv=Individual harmonic voltage distortion.

#### **1.4 Power in Distorted AC Networks.**

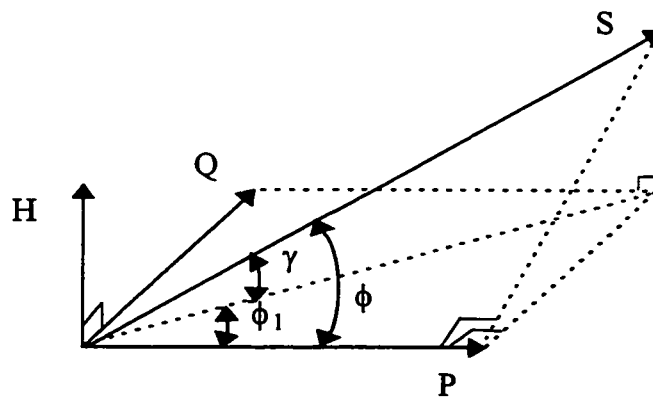
The active and reactive power components for electric circuits with sinusoidal and linear loads are well established. In the case of non-linear loads, however the use of the reactive and the harmonic power is an actual necessity for accomplishing reactive power compensation and/or harmonic filtering. The components of the electric power are shown in Fig. 1.3 assuming a sinusoidal voltage supply and a non-linear load [8]. In this case, the power factor ( $\cos\phi$ ) is the product of the distortion factor ( $I_1/I = \cos\gamma$ ) by displacement factor ( $\cos\phi_1$ ) :

$$\text{Power Factor} = \text{Distortion factor} \times \text{Displacement Factor}$$

The displacement factor corresponds to the power factor of systems without harmonics. This factor may be called fundamental power factor, as it depends only on the current fundamental component. On the other hand, the power factor, as defined above, may be called total power factor, as it depends on fundamental and all harmonic components. Hence, harmonics cause lower power factor. The power components in distorted networks are represented in power tetrahedron, instead of the triangle as in the linear case, is shown in Fig. 1.4.



**Fig. 1.3** Components of electric power



**Fig. 1.4** Power tetrahedron.

From Fig. 1.3 and 1.4, various important factors are determined on the use of reactive power and harmonic compensation :

(i) The reactive component is dependent only on the current component at fundamental frequency. The reactive component can be eliminated by using a conveniently chosen capacitor or inductor. The connection of an inductor or a capacitor component in parallel with load allows the generation of a current at fundamental frequency that absorbs or generates the reactive power required by the load;

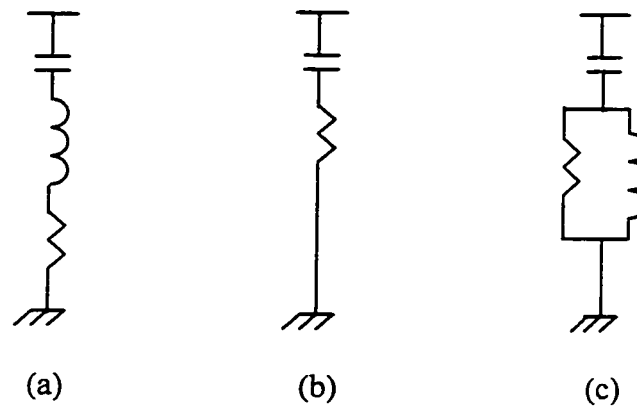
(ii) The distorting power is dependent on the current components with frequencies different from fundamental frequency (harmonics) and can not be eliminated by a single capacitor or inductor. The elimination of harmonic power depends on filters that work as a short-circuit for the harmonic current generated by the load.

### **1.5 Methods of Dealing with Harmonics.**

As an alternative to harmonic reduction, it has been suggested to derate transformers and oversize cables [9]. This could be an adequate solution in some cases. but since system configurations change, and thereby the harmonic profile of the system, the required amount of derating or oversizing could be difficult to predict. Also, this option does not prevent harmonics from entering the supply system. Therefore, a more appropriate method for harmonic mitigation is the use of filters.

### 1.5.1 Passive Filters

Passive filters in power systems as shown in Fig. 1.5, are usually shunt connected, the accepted practice being to connect a number of separate shunt branches across the terminals of the load or the plant. Each of these branches is tuned to one of the dominant harmonics, with a low pass branch added that exhibits low impedance for the remaining higher order harmonics [10].



**Fig. 1.5** Passive filters. (a) single tuned filter (b) first order high-pass filter (c) second order high-pass filter.

Passive filters can prevent harmonics from entering a supply system, and are also useful in increasing power factor, but there are a number of considerations that are critical in this approach [10] [11]. For instance parallel and series resonance with ac line impedance may produce amplification in the harmonic current and voltage of the line at certain frequencies. Also, the effectiveness in attenuating harmonics are not dictated only by the passive filter itself, but depend on the source impedance. Moreover, it is difficult to decouple the effects of one load from those of other loads connected to the line and

compensate only for harmonic currents produced by this one load. Thus, it is often necessary to oversize passive filters in order to avoid overheating.

The classic solution of tuned passive filters therefore has serious limitations. Furthermore, with the widespread use of variable distorting electronic loads, harmonic tracking is not adequately achieved. Also the probability of encountering resonant conditions increases with the number of installed filtering units.

Active filtering techniques have therefore been proposed to overcome the problems associated with passive filters.

### **1.5.2 Active Filtering**

The first attempts to reduce harmonics without the use of conventional passive filters, were made by B. Bird, et al. [12]. Their design proposed changing the waveform of the current drawn by the load by injecting a third harmonic current, displaced in phase, into the converter itself. With this method however it is impossible to fully eliminate more than one harmonic.

It was Ametani's idea to expand the current injection method by proposing a technique to eliminate multiple harmonics [13] [14]. According to this theory, an active control circuit could be used to precisely shape the injected current. Ideally, this current would contain harmonic components of opposing phase, thus the harmonics would be neutralized, and only the fundamental component would remain. Despite the promising theoretical concept, Ametani was not successful in producing a practical circuit capable



of creating a precise current. The total harmonic distortion was reduced, but single harmonics were not completely eliminated.

On the other hand, Sasaki and Machida theorized that harmonics could be eliminated by using the principle of magnetic flux compensation [15]. This in principle, is the use of current to produce a flux to counteract the flux produced by the harmonics. Once again, theoretically, any number of harmonics could be directly eliminated. The current that would be required to eliminate waveform distortion caused by harmonics was calculated mathematically, but again, a practical control circuit was not realized.

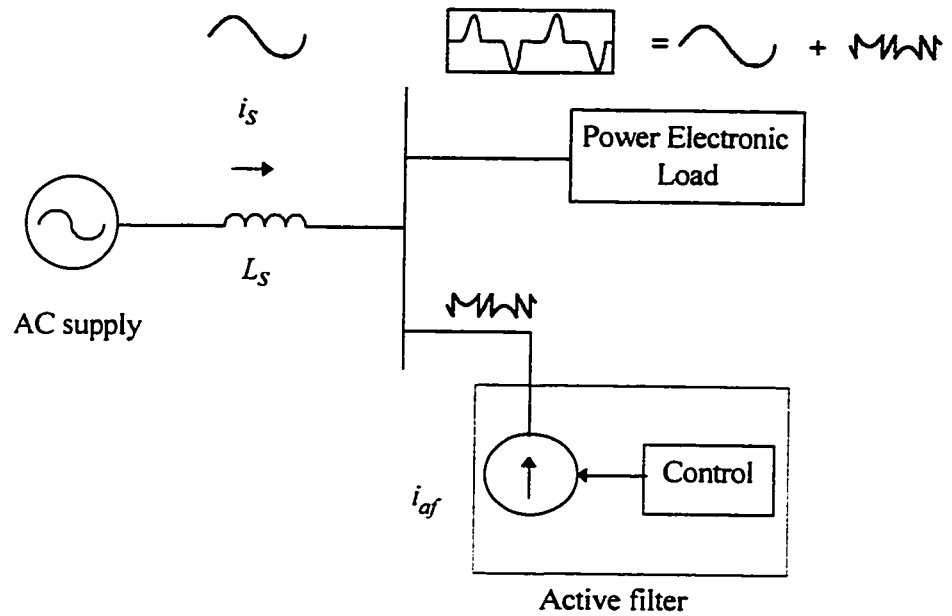
Over the last ten to twelve years the remarkable progress in capacity and switching performance of devices such as bipolar transistors (BJT), gate turn-off thyristors (GTO) and insulated gate bipolar transistors (IGBT), has spurred in the study of active power filters for harmonic compensation. In addition, advances in topologies and controls schemes for static PWM converters have enabled active power filter using these converters to generate specified harmonic currents, such as created by non linear loads.

## **1.6 Literature Review**

### **1.6.1 Shunt Active Filters.**

The shunt active filter approach [16] [17] [18] is based on the principle of injection of harmonic currents into the ac system, of the same amplitude but opposite in phase to that of the load harmonic currents. Fig. 1.5 shows the active power filter

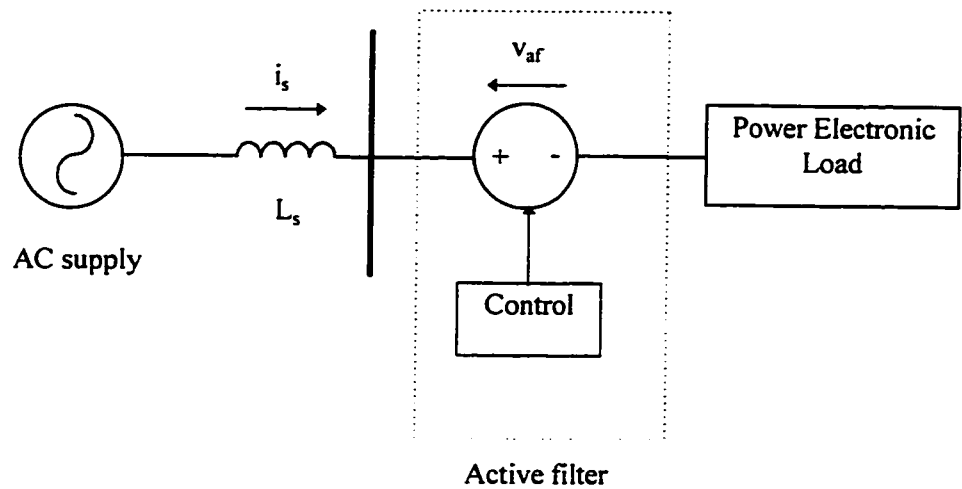
compensation principle, which is controlled in a closed loop manner to actively shape the source current into sinusoid.



**Fig. 1.6** Principle of shunt connected active filters.

### 1.6.2 Series Active Filters

In series active filter configuration [10], a voltage source,  $v_{af}$ , is constructed in such a way that when its voltage is added to the load voltage, the distorted voltage is canceled, thus resulting of a sinusoidal voltage at the PCC. Fig. 1.7 shows the series active filter compensation principle.



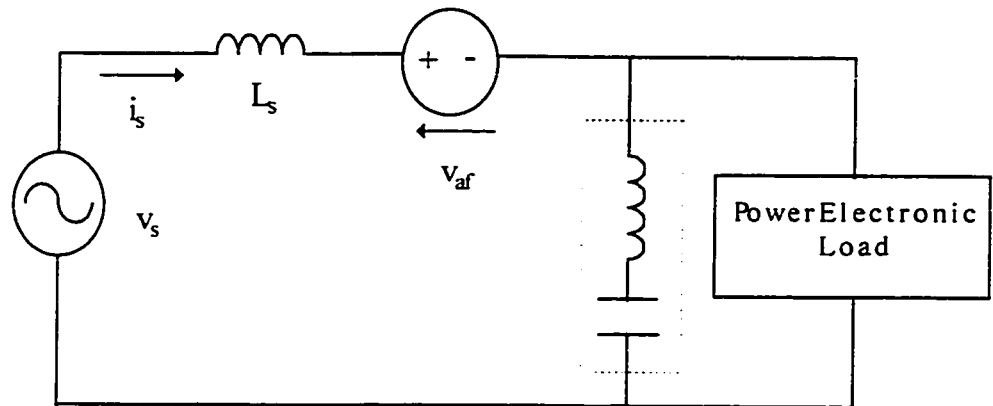
**Fig. 1.7** Series connected active filter.

For harmonic compensation, both shunt and series active filter have much smaller ratings than the apparent power of the load. The shunt active filter is rated for supply voltage, but a reduced current. In the case of series dynamic filters, the rated load current passes through the filter but the rated voltage is again lower. Therefore, harmonic minimization can be implemented with converters having a reduced power rating.

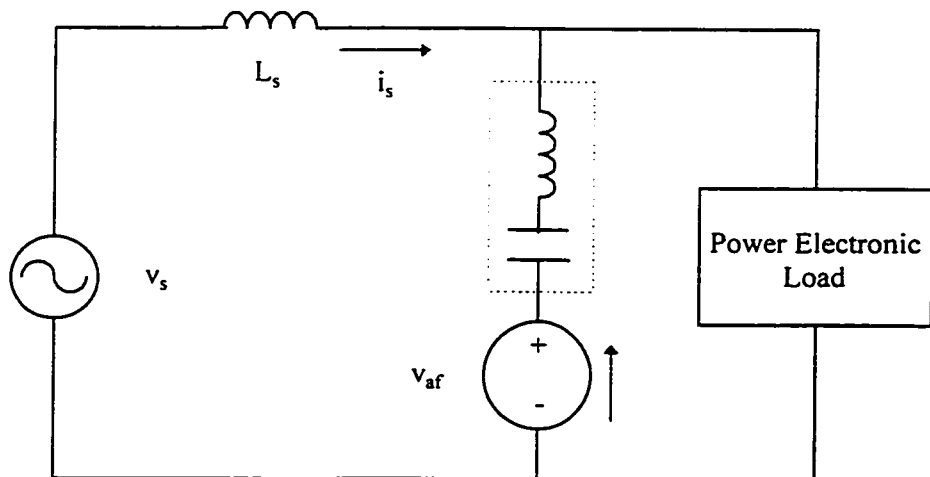
### 1.6.3 Hybrid Active Filters.

Hybrid structures were proposed for harmonic compensation of large rated loads in high voltage networks. Hybrid active filters configurations, combines passive and active filters [20]. These filters improve the compensation characteristics of the passive filters and thus realize a reduction in the rating of the active filter. They are particularly suited in installations where L-C tuned passive filters already exist.

In the hybrid series configuration, the series voltage injection is to be regarded as an isolator, either determining the harmonic currents to be supplied to the non-linear load or the harmonic currents that will be absorbed by the tuned LC-filters. Fig. 1.7 and Fig. 1.8 show two hybrid active filter configurations, series [21] [22] [23] [24] and shunt [25] [26] [27] [28] [29] [30]. In the first case, the injected voltage is in series, Fig. 1.7, and in the second case it is in series with the shunt passive filter Fig. 1.8.



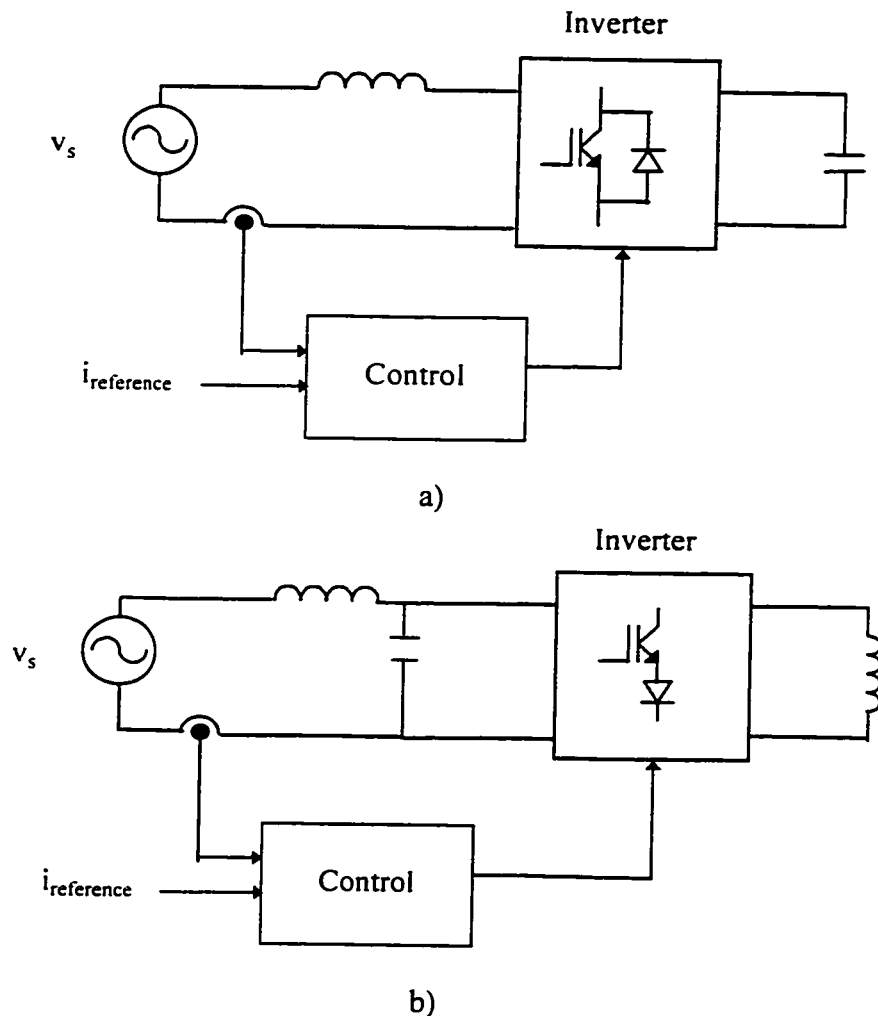
**Fig. 1.8** Hybrid series active filter.



**Fig. 1.9** Hybrid shunt active filter.

#### 1.6.4 Active Filter Topologies.

There are two types of power circuits [31] for the active filters as shown in Fig. 1.9, current and voltage source types. The voltage-type inverter uses a capacitor with a regulated dc voltage [32] [33], Fig. 1.9 (a), while the current-type approach uses a reactor supplied with a regulated dc current [34] [35] [36], Fig. 1.9 (b). One of the main advantage of voltage type converters is that they are easily expandable and are less expensive than current-type converters.



**Fig. 1.10** Main topologies of active filters. (a) voltage-type  
(b) current-type.

### **1.6.6 Control Aspects.**

Compensation of harmonics can be accomplished in time-domain or frequency domain [17]. First approach is based upon “on line” computation of an instantaneous error function, while the second case uses the principle of Fourier analysis and periodicity of the distorted waveform to be corrected. The error-function in time-domain could be computed in the following ways: a) extraction of the fundamental component from the distorted waveform through a notch filter [17], b) instantaneous reactive power compensation, which uses an instantaneous orthogonal power transformation on both the actual and the fundamental components of voltage and current to produce a power function [37][38]. The difference between these two transformations is the error, and c) synchronous reference frame approach [21] [39]. Many PWM strategies exist (for compensation in the time-domain) to generate the gating signals to the switches and thereby to reconstruct the distorted current. The most widely used PWM strategies are [17] [40] : a) triangular wave or ramp comparison , b) hysteresis, and c) deadbeat.

### **1.7 Problem Statement.**

The conventional three phase active filter, in a bridge configuration is well suited for three phase balanced loads, supplied from a three wire ac mains [31] [35] [36] [41] [42] [43] [37]. Nevertheless, in a number of industrial and commercial applications, power is distributed through three phase, four wire systems. Furthermore, if non-linear single-phase loads are present, or the three phase load is unbalanced, the line currents,

both in terms of fundamental and harmonic components, are unbalanced and neutral currents flow. In unbalanced load condition, the sum of the instantaneous harmonic currents is not equal to zero. As a result, phase interactions between the lines appear and the three-phase three-wire active filter cannot adequately reduce or eliminate line harmonics in this situation. The problem points to the necessity of having per phase based current controllers and converters so that:

- i) independent harmonic reduction is achieved in each phase;
- ii) reduction of the neutral current is achieved without disturbing the operation of the active filter.

To eliminate the neutral current in three phase four wire systems, [44] has proposed an additional active filter, while [45] [46] [47] [48] [49] proposed an eight switch active filter topology, which is complicated to implement. Also [45] [46] reported a three phase half-bridge topology, which uses variable hysteresis current mode controller. Other suggested methods include the use of complicated zigzag transformer connections as reported in [50].

## **1.8 Scope and Contribution of This Thesis**

This thesis is a contribution to the design and implementation of a three phase four wire active filter. An industrial-type experimental unit rated 208V/15A, was developed and used for testing and validation purposes. Features of the system include:

- (i) The power circuit is a force-commutated pulse-width modulated voltage source

inverter (PWM-VSI), based on half-bridge configuration, using three single phase modules with a center tap capacitor, (ii) Per phase based current controllers and power converters are implemented to allow control of individual phase currents. The proposed implementation uses the ramp comparison technique that allows operation under constant switching frequency achieving better switching pattern than hysteresis control [51].

Specific contributions include :

(i) A detailed analytical treatment and a systematic approach to design the power circuit for various modes of operation is presented [52] [53]. The treatment is general and valid for other type of voltage source configurations;

(ii) The residual currents and individual harmonic distortion factors after compensation are determined theoretically [54]. The feasibility is tested through computer simulation on PSIM [55] software package;

(iii) Thorough testing and validation is carried out on the experimental unit to verify the theoretical results.

## **1.9 Outline of This Thesis**

The thesis is organized as follows:

**Chapter 2** analyzes the three phase three wire and three phase four wire voltage source active filters. Working constraints are derived. Design guidelines showing the selection of various power components such as the synchronous link reactor, dc bus voltage and the switching frequency are included.



**Chapter 3** quantifies the required harmonic power and discusses rating issues of the active filter and power components. A design procedure is presented to select the dc bus capacitor that covers all modes of operation. The effect of dc bus ripple on the compensation capacity is analyzed. A typical example is included to illustrate the design approach followed by simulation results showing the static performance of the active filter.

**Chapter 4** covers modeling of the voltage and current blocks, and control system design, quantifies the residual harmonic components, and gives simulation results showing the dynamic performance of the active filter.

**Chapter 5** validates the theoretical concepts by simulation and experimentally. Performance of the active filter is investigated under different modes of operation: (a) single phase load, (b) balanced load (c) unbalanced load, and (d) mains voltage unbalance. The active filter in the three phase full bridge configuration is tested under the same modes and its performance is compared to the proposed topology.

**Chapter 6** concludes the thesis and identifies some areas for future research work.

## **Chapter 2**

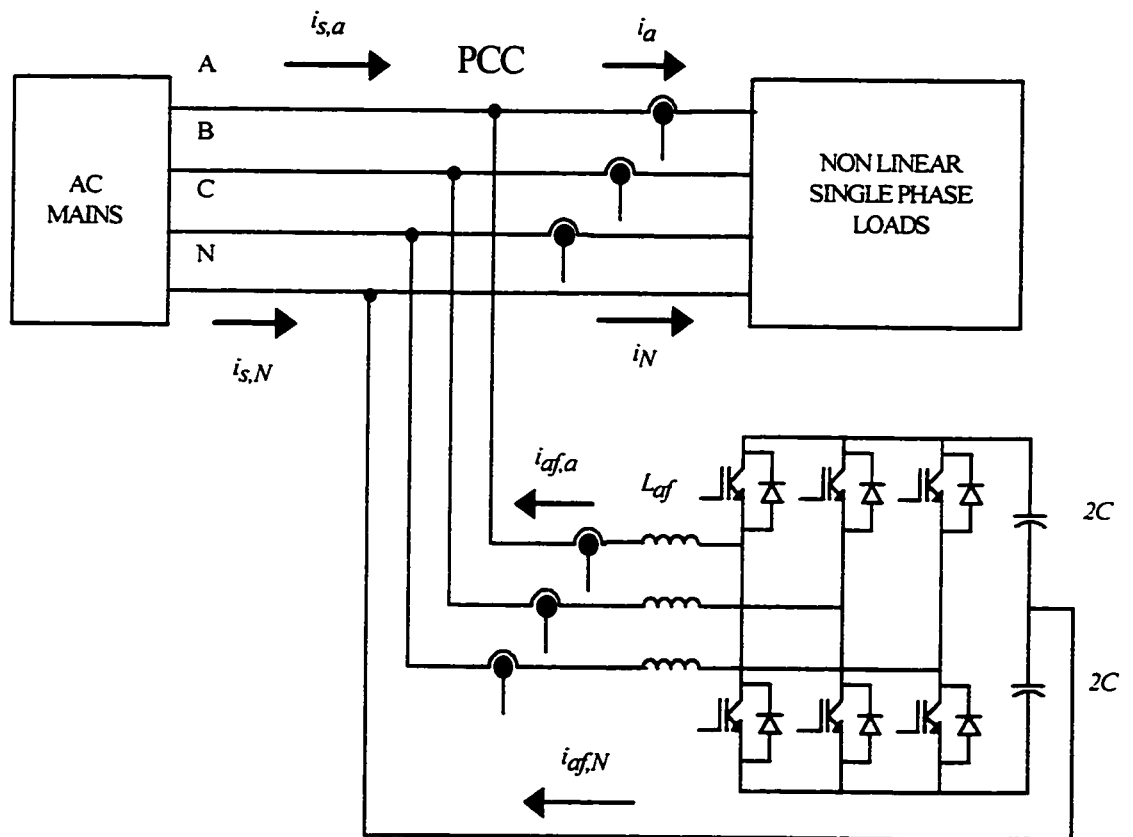
### **THREE PHASE SHUNT CONNECTED VOLTAGE SOURCE ACTIVE FILTERS**

#### **2.1 Introduction**

With improvements in power and control circuits, active filters are becoming a viable alternative to passive filters for meeting harmonic distortion limits. The superior performance of active filters as compared to conventional passive L-C filters, is in fact due to their filtering characteristics which is independent of the source impedance [10]. This chapter describes the operation of three-phase four wire active filters for the general case. The active filter under study is connected in shunt with the load and its structure is based on a self commutated pulse-width modulated voltage source inverter connected to a self controlled dc bus. The chapter also investigated the neutral current for unbalanced load conditions when the half-bridge topology is used. Design issues such as switching frequency, dc bus voltage and line inductor values are detailed. The quality of the supply current, the magnitude and components of the neutral currents are also investigated.

## 2.2 Active Filter Configuration

The general topology for the four wire active filter is given in Fig. 2.1. The dc bus uses a common capacitor, with the center-tap connected to the line neutral, thus providing a return path for the neutral current. The PWM pattern is generated using a constant frequency ramp comparison technique [40] [56]. The ac side of the converter is connected to the mains via a synchronous link reactor,  $L_{af}$ , Fig. 2.1, which also serves as a first order low-pass filter.



**Fig. 2.1** Four wire half-bridge active filter.

### 2.3 Three Phase Active Filter

The operation of the conventional three phase active filter, Fig. 2.2, is investigated for the general case. It is assumed that the supply feeds three different single phase non-linear loads, connected between the lines and the neutral. The currents drawn by the loads are non sinusoidal and have all the odd harmonics including the triplen.

The load currents are expressed as :

$$i_j = i_{j,1} + i_{j,h} \quad (2.1)$$

Where  $j$  = phase  $a$ ,  $b$  and  $c$ .  $i_{j,1}$  is the fundamental component of the load current, and  $i_{j,h}$  is the distorting current for phase  $j$ .

Neutral current before compensation is the sum of phase currents :

$$i_N = - \sum_{j=a,b,c} i_j \quad (2.2)$$

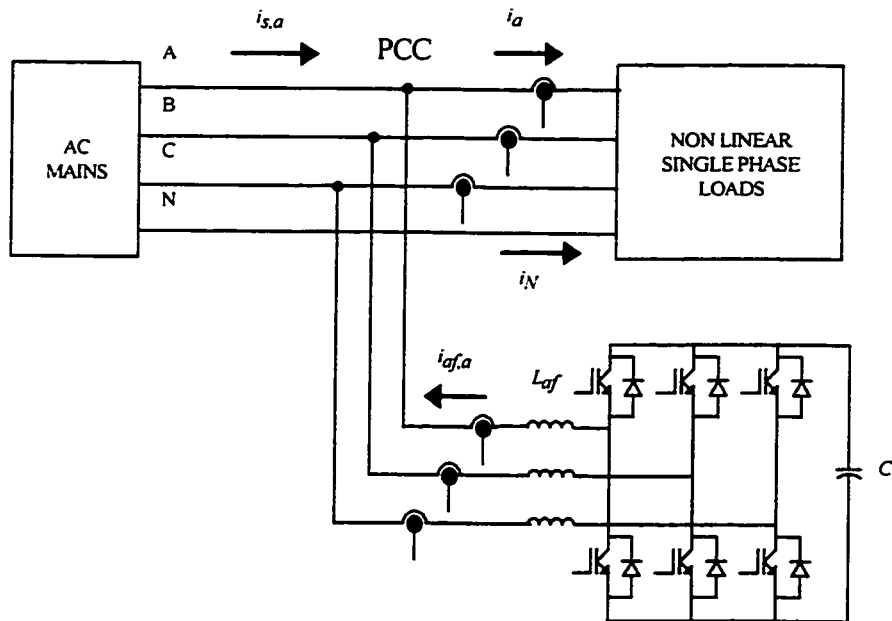


Fig. 2.2 Three phase active filter.

For the general case, each three phase system of harmonic order  $h$ , is an unbalanced system. By the symmetrical components theory each unbalanced system can be decomposed in several balanced harmonic systems of the same harmonic order and of positive,  $i_{j,h}^+$ , negative,  $i_{j,h}^-$ , and zero sequence,  $i_{j,h}^0$ .

$$i_{j,h} = i_{j,h}^+ + i_{j,h}^- + i_{j,h}^0 \quad (2.3)$$

The absence of fourth wire in the active filter makes the zero sequence current nil.

$$i_{af}^0 = 0 \quad (2.4)$$

The active filter currents are given by :

$$i_{af,j} = i_{j,h}^+ + i_{j,h}^- \quad (2.5)$$

Supply side currents are given by :

$$i_{s,j} = i_j - i_{af,j} \quad (2.6)$$

Combining (2.1), (2.5) and (2.6) gives :

$$i_{s,j} = i_{j,1} + i_{j,h}^0 \quad (2.7)$$

The neutral current is given by :

$$i_N = -\{i_{a,1}^0 + i_{a,h}^0\} = -i_a^0 \quad (2.8)$$

The theoretical analysis shows that with a three wire three phase active filter :

- i) the line current harmonics remain partially uncompensated, (2.7).
- ii) the amplitude of the harmonic currents in the neutral wire is not reduced.

Moreover, the equations (2.7) and (2.8) show that the active filter cannot compensate the line currents even when balanced non linear single phase loads are present, since triplen components cannot be supplied.

## **2.4 Four Wire Half-Bridge Topology**

### *A. Operation*

The connection of the capacitor midpoint to the neutral wire allows implementation of per-phase based current regulators, hence the phases are totally decoupled.

The currents generated by the active filter are given by :

$$i_{af,j} = i_{j,h} \quad (2.9)$$

Supply side currents are obtained from (2.7) and (2.9) :

$$i_{s,j} = i_{j,l} \quad (2.10)$$

Current in the neutral wire at the supply side is given by :

$$i_{s,N} = - \sum_{j=a,b,c} i_{s,j} \quad (2.11)$$

Combining (2.10) and (2.11) yields :

$$i_{s,N} = - \sum_{j=a,b,c} i_{j,1} \quad (2.12)$$

Comparing equations (2.2) and (2.12) one see that only the fundamental component remains in the neutral wire. Comparing the magnitude of the neutral current before and after compensation yields :

$$\frac{I_{s,N}}{I_N} < 1 \quad (2.13)$$

The theoretical analysis shows that in the general case :

- i) the line currents are compensated, equation (2.10);
- ii) the amplitude of the neutral current is reduced for unbalanced loads, equation (2.13).

### B. Neutral Current

The current in the neutral wire before compensation contains all the odd harmonics including the triplen, its expression is given by :

$$i_N = \sum_{h=1}^{\infty} I_{N,2h-1} \cdot \sqrt{2} \cdot \sin[(2h-1)\omega t + \phi_h] \quad (2.14)$$

The rms value of  $i_N$  is given by :

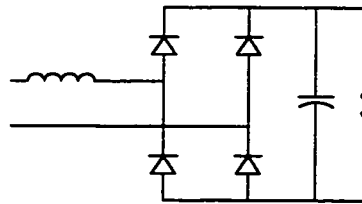
$$I_N = \sqrt{\sum_{h=1}^{\infty} I_{N,2h-1}^2} \quad (2.15)$$

The current in the fourth wire of the active filter supplies all the odd harmonics including the triplen, but excluding the fundamental component. After compensation the current in the neutral wire has a 60 Hz component which is the contribution of unbalanced line currents. The rms value of the current in the neutral wire at the supply side is given by [9] :

$$I_{s,N} = \sqrt{I_{a,l}^2 + I_{b,l}^2 + I_{c,l}^2 - (I_{a,l} \cdot I_{b,l}) - (I_{a,l} \cdot I_{c,l}) - (I_{b,l} \cdot I_{c,l})} \quad (2.16)$$

Usually, when the loads are balanced, the neutral current contains only triplen harmonics. It follows that after compensation, the neutral wire is exempt of low frequency components. On the other hand, the return wire of the active filter carries the current present in the neutral wire of the load. To illustrate the problems associated with typical single phase non-linear loads, diode rectifiers with capacitive output are considered, as shown in Fig. 2.3.

With rectifier conduction angles of  $60^\circ$ , the magnitude of the neutral current could reach 1.73 times the phase current for balanced loads [9]. Table 2.1 gives the magnitude of the neutral current for two cases. The magnitude of the neutral current is 127 % of the line current when the loads are unbalanced. The worst case occurs when the load are balanced, since its magnitude reaches a value of 165 % of the line current.



**Fig. 2.3** Single phase diode rectifier.



**Table 2.1 Typical neutral current amplitudes.**

<b>Harmonic h</b>	<b>Single Phase load</b>	<b>Balanced Loads (3×1φ) Neutral Current</b>	<b>Typical Unbalanced Loads Neutral Current</b>
1	1.0	--	0.57
3	0.68	2.04	1.46
5	0.287	--	0.11
7	0.083	--	0.11
9	0.073	0.0219	0.127
11	0.036	--	0.032
<b>I<sub>a</sub></b>	<b>1.25</b>	--	--
<b>I<sub>N</sub></b>	--	<b>2.06</b>	<b>1.58</b>
<b>I<sub>N</sub>/I<sub>a</sub></b>	--	<b>1.65</b>	<b>1.264</b>

## **2.5 Power Circuit Design**

The selection of the ac link reactor and the dc capacitor value affects directly the performance of the active filter. The design criteria is based upon specifying the filter inductor such that it keeps the high frequency ripple of the inverter ac output current small, and at the same time ensuring sufficient driving voltage to generate the rate of rise of the distorting current.

The following assumptions are made when the power circuit is analyzed:

- i) the converter switching elements are ideal;
- ii) the passive elements are ideal;
- iii) the dc bus voltage is ripple free.

### 2.5.1 Current Ripple Generated by the Half-Bridge Active Filter

The switches of one leg of the inverter are gated in a complementary fashion, yielding a bipolar output voltage as shown in Fig 2.4 a). The output current and voltage of the inverter are shown in Fig. 2.4 b).

When upper switch is gated.

$$\frac{di_{af}^+}{dt} = \frac{0.5 \cdot V_{dc} - v_s(t)}{L_{af}} \quad (2.17)$$

When lower switch is gated

$$\frac{di_{af}^-}{dt} = \frac{-0.5 \cdot V_{dc} - v_s(t)}{L_{af}} \quad (2.18)$$

From Fig. 2.4 we have :

$$\frac{d}{dt}(i_{af}^+ - i_{ref}) = \frac{\Delta i}{t_{on}} \quad (2.19)$$

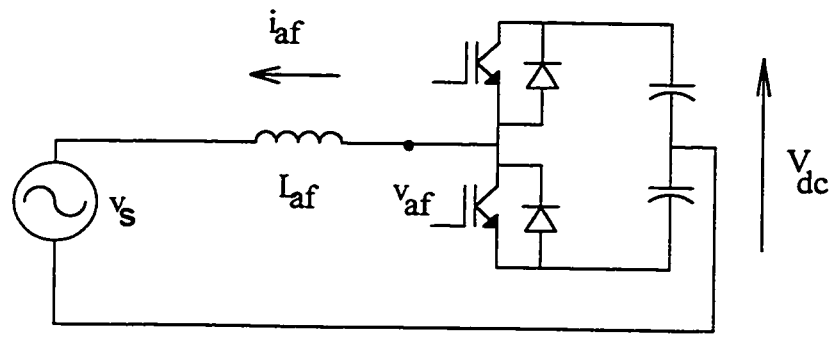
$$\frac{d}{dt}(i_{af}^- - i_{ref}) = \frac{\Delta i}{t_{off}} \quad (2.20)$$

Using the fact that :

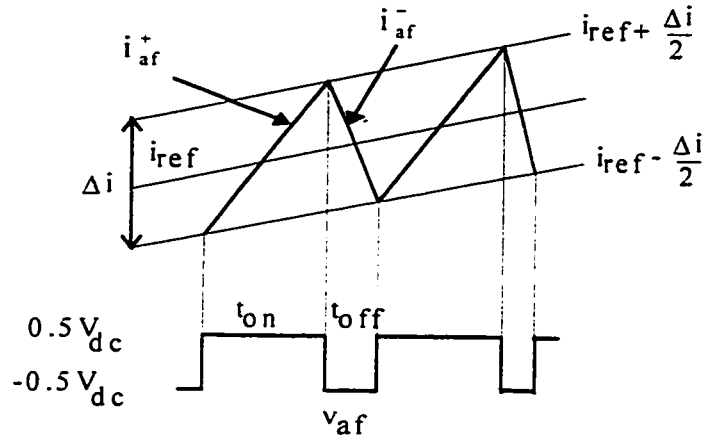
$$f_{sw} = \frac{1}{T_{sw}} = \frac{1}{t_{on} + t_{off}} \quad (2.21)$$

Combining equations (2.14), (2.15), (2.16) and (2.17) gives:

$$\Delta i = \frac{V_{dc}}{4 \cdot f_{sw} \cdot L_{af}} \left[ 1 - \frac{4}{V_{dc}^2} (v_s + L_{af} \cdot \frac{di_{ref}}{dt})^2 \right] \quad (2.22)$$



a)



b)

**Fig. 2.4** (a) half-bridge active filter (b) output voltage and current.

Maximum ripple is expressed as:

$$\Delta i_{\max} = \frac{V_{dc}}{4 \cdot L_{af} \cdot f_{sw}} \quad (2.23)$$

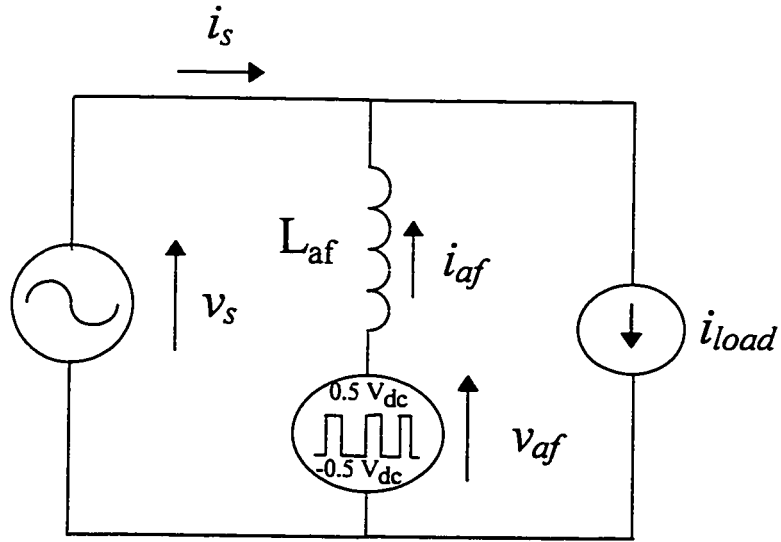
The above expression shows that the current ripple increases when the switching frequency and/or the reactor value decreases. Also, the current ripple increases when the dc bus voltage increases.

### 2.5.3 Reactor and DC Bus Voltage Selection

The ripple generated by the converter must be limited to an acceptable level in order to achieve a low total harmonic distortion current in the mains. With the ramp comparison technique, the spectrum of the output current is well defined, hence its rms value may be obtained by simply calculating the value of the individual harmonic at specified frequencies. The equivalent circuit of the system is shown in Fig. 2.5.

The output voltage generated by the converter is the sum of the voltage,  $G_c \cdot V_{cont}$ , that produces the required injected current and the high frequency components. The output voltage,  $v_{af}$  can be written as :

$$v_{af}(t) = G_c \cdot v_{con}(t) + \sum_{j \rightarrow n=odd} V_{af, f_j} \cdot \sqrt{2} \cdot \sin(2 \cdot \pi \cdot f_j \cdot t + \psi_{j_n}) \quad (2.24)$$



**Fig. 2.5** Per phase equivalent circuit of the system.

Where  $G_c$  is the gain of the converter and is defined as the ratio of half the dc bus voltage to the amplitude of the triangular waveform,  $v_{cont}$  is the control voltage or the modulating signal,  $V_{af.f_n}$  is the rms value of the active filter output voltage at high frequencies,  $f_{jn}$ . The high frequency harmonics are generated as a consequence of switching action of the converter.

The high frequency harmonic orders  $f_{jn}$  are given by :

$$f_{jn} = j \cdot f_{sw} \pm n \cdot f \quad (2.25)$$

It is assumed that the active filter cancels the harmonic component of the load completely, hence the high frequency harmonic currents are reflected back to the supply side.

The supply side current is given :

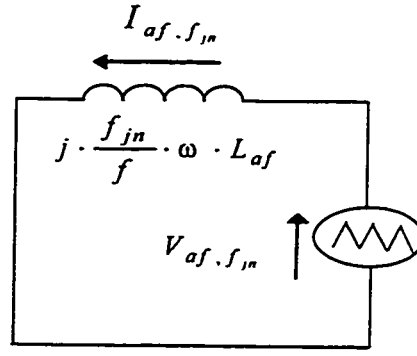
$$i_s(t) = I_1 \cdot \sqrt{2} \cdot \sin(\omega t + \phi_1) + \sum_{j+n=odd} I_{af.f_n} \cdot \sqrt{2} \cdot \sin(2 \cdot \pi \cdot f_{jn} \cdot t + \psi_{jn}) \quad (2.26)$$

Using the equivalent circuit of the active filter as shown in Fig. 2.6. The rms value of individual harmonic currents at frequencies  $f_{jn}$  is expressed as :

$$I_{af.f_n} = \frac{V_{af.f_n}}{2 \cdot \pi \cdot f_{jn} \cdot L_{af}} \quad (2.27)$$

Rearranging equation (2.27) gives :

$$\frac{I_{af.f_n}}{I_1} = \frac{1}{m_0} \cdot \frac{V_{af.f_n}}{V_{dc}/2} \cdot \frac{f}{f_{jn}} \cdot \sqrt{2} \cdot \frac{1}{\frac{\omega \cdot L_{af}}{V_s/I_1}} \quad (2.28)$$



**Fig. 2.6** Equivalent circuit of the system at high frequencies.

$m_0$  is the modulation index at no load, and is defined as the ratio of peak output voltage to half the dc bus voltage.

$$m_0 = \frac{2 \cdot V_s \cdot \sqrt{2}}{V_{dc}} < 1 \quad (2.29)$$

The value of the synchronous link reactor in pu in function of the ripple current becomes :

$$\frac{\omega L_{af}}{V_s / I_1} = \frac{1}{m_0} \cdot \frac{\sqrt{\sum_{j+n=odd} \left[ \frac{f}{f_{jn}} \cdot \left( \frac{\hat{V}_{af, f_{jn}}}{V_{dc} / 2} \right) \right]^2}}{(I_{af, ripple})_{rms} / I_1} \quad (2.30)$$

Where  $(I_{af, ripple})_{rms}$  is defined as :

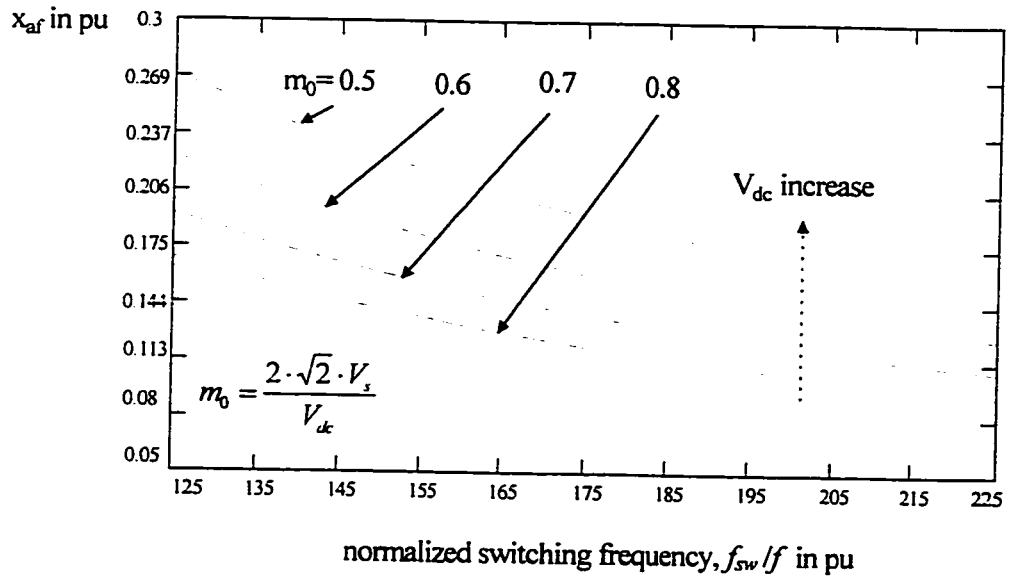
$$(I_{af, ripple})_{rms} = \sqrt{\sum_{j+n=odd}^{\infty} I_{af, f_{jn}}^2} \quad (2.31)$$

Equation (2.30), shows that the value of the reactor depends on the dc bus voltage and the harmonic content of the converter voltage which in turn depends on the modulation index. Table 2.2 gives the value of these harmonics for a modulation index 0.9. The largest component of the ripple current in the active filter is contributed by the harmonic at the switching frequency,  $f_{sw}$ , as shown in Table 2.2.

**Table 2.2 High frequency components of the inverter voltage for modulation index 0.9**

$f_{jn} = j f_{sw} \pm n \cdot f$	$\hat{V}_{af, f_n} / V_{dc} / 2$
$f_{sw}$	0.71
$f_{sw} \pm 2 \cdot f$	0.269
$2 \cdot f_{sw} \pm f$	0.248
$2 \cdot f_{sw} \pm 3 \cdot f$	0.176
$2 \cdot f_{sw} \pm 5 \cdot f$	0.023
$3 \cdot f_{sw}$	0.142
$3 \cdot f_{sw} \pm 2 \cdot f$	0.119
$3 \cdot f_{sw} \pm 4 \cdot f$	0.13
$3 \cdot f_{sw} \pm 6 \cdot f$	0.03
$4 \cdot f_{sw} \pm 1 \cdot f$	0.173
$4 \cdot f_{sw} \pm 3 \cdot f$	0.062
$4 \cdot f_{sw} \pm 5 \cdot f$	0.101
$4 \cdot f_{sw} \pm 7 \cdot f$	0.033

The minimum value of the synchronous link reactor can be found by forcing the ripple,  $(I_{af,ripple})_{rms} / I_1$ , to less than 5% for the maximum load current,  $I_1$ , and by choosing a modulation index equal to 0.9 for the same load condition. For a given modulation frequency, increasing the dc bus voltage, will result in a higher value for the reactor. On the other hand, for a given dc bus voltage, increasing the modulation frequency, decreases the value of the inductor, as shown in Fig. 2.7. Equation (2.30) gave the first relation between the dc bus voltage and the reactor. An additional equation is required to compute both  $L_{af}$  and  $V_{dc}$  values. The second relation is obtained by using the fact that the modulation is less than one at maximum load condition (in our case 0.9).



**Fig. 2.7** Minimum active filter inductance in function of normalized switching frequency and dc bus voltage as parameter.



The modulation index is defined as the ratio between the inverter voltage and half the dc bus voltage.

$$m = \frac{(v_{af}(t))_{\max}}{V_{dc}/2} = \frac{\left( V_s \cdot \sqrt{2} \cdot \sin \omega t + L_{af} \cdot \frac{di_{load,h}}{dt} \right)_{\max}}{V_{dc}/2} \quad (2.32)$$

In the general case if the instant at which the maximum occurs in (2.32) is not known, then the worst case occurs when the reactor introduces a voltage drop that equals the supply voltage, hence the slope of the distorting current is at its maximum and has positive sign :

$$\left( \frac{di}{dt} \right)_{load,h} = \frac{0.5 \cdot V_{dc} \cdot m - V_s \cdot \sqrt{2}}{L_{af}} \quad (2.33)$$

In other words, (2.33) shows that the  $di/dt$  generated by the inverter is finite and is greater than the  $di/dt$  generated by the harmonic component of the load current.

$$\left( \frac{di}{dt} \right)_{load,h} < \left( \frac{di}{dt} \right)_{active\ filter} \quad (2.34)$$

The design equations show that there are a compromise to make when choosing the reactor and the dc voltage values. Small reactor,  $L_{af}$ , is required to generate high  $di/dt$ , however decreasing the reactor increases the ripple current, which in turn is reflected to the mains. As a consequence the supply side exhibits higher total harmonic distortion. Also, a similar effect is observed with  $V_{dc}$ . A high dc voltage is required to obtain a sufficient driving voltage capable of producing a high  $di/dt$ , which has two immediate effects: i) the ripple current of the converter is increased, ii) the switches must be selected with higher blocking capability in terms of voltage.

The flowchart of Fig. 2.8 shows the selection procedure of the switching frequency, the synchronous link reactor and the dc bus voltage values. These three parameters are determined knowing the supply voltage, the harmonic content of the load, and the rate of rise of the distorting current. On the other hand, the flowchart shows that an iteration is required to extract these values, and the dc voltage is not permitted to exceed the practical limit. The practical limit is the maximum blocking capability of the switches and is dependent on the technology available. For example, IGBT type switches have maximum blocking capability of twelve hundred volts, and if a fifty percent of safety margin is taken, then the practical limit as referred to flowchart becomes eight hundred volts.

The design procedure as presented in Fig. 2.8 requires an initial guess of the switching frequency, which is dependent from the highest harmonic to eliminate [16]. From Table 2.2, the high frequency components of the active filter current are mainly at.

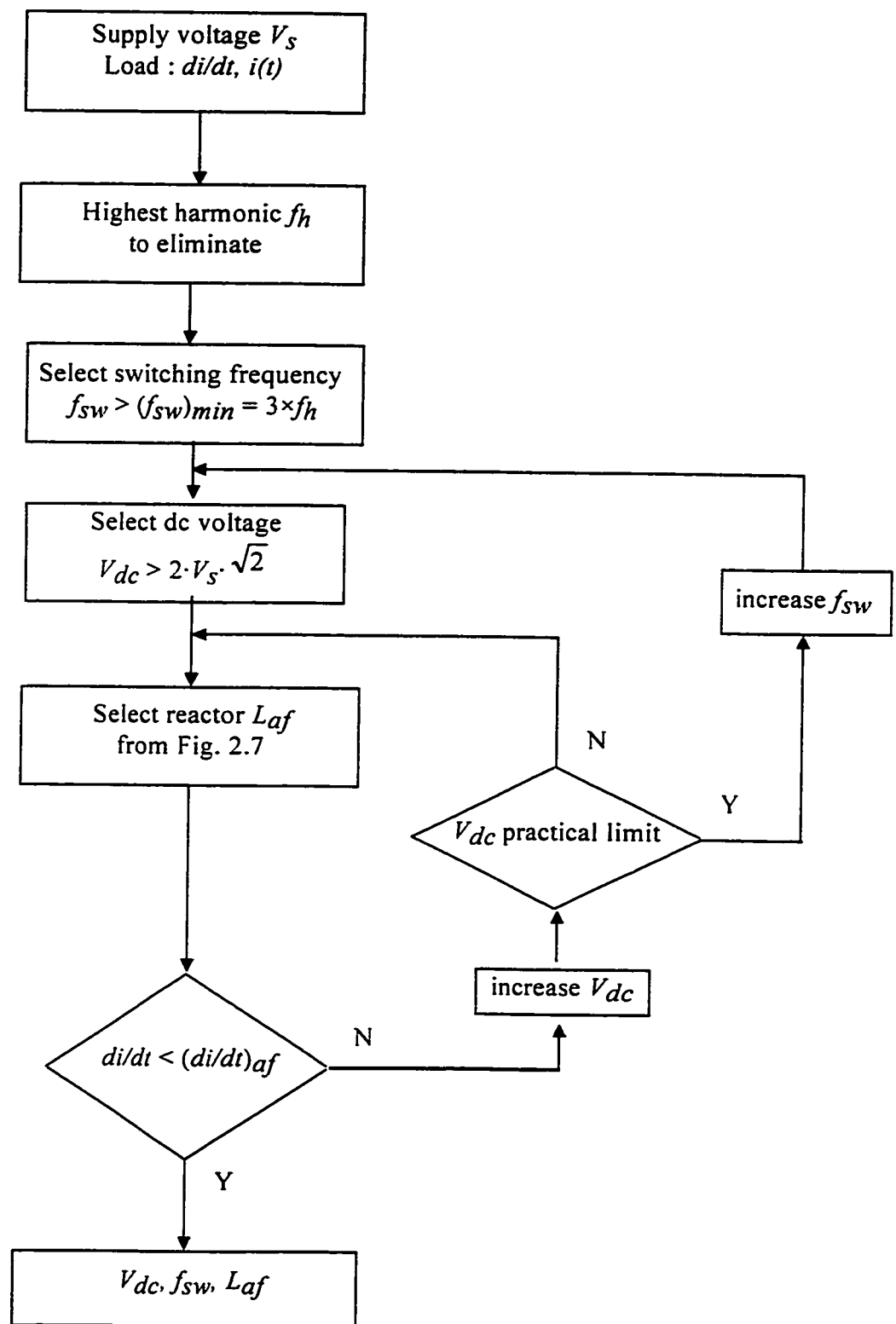
$$f_{sw}, f_{sw} \pm 2f, 2f_{sw} \pm f, 2f_{sw} \pm 3f, 2f_{sw} \pm 5f, \dots$$

The lowest frequency is  $f_{sw} - 2f$ , and  $f_{sw}$  must be chosen so that this frequency becomes higher than the highest frequency of harmonics to be eliminated. Thus

$$f < f_{sw} - 2 \cdot f \quad (2.35)$$

Hence,  $f_{sw}$  should be chosen at least three times the highest frequency of harmonics to be suppressed. For example, if the highest frequency of harmonics is 1260 Hz (21<sup>st</sup> harmonic), the frequency of the triangular wave should be 3780 Hz or higher.

The design equations are general and are valid for any type of non-linear load and regardless of the combination, such as balanced and unbalanced loads.



**Fig. 2.8** Flowchart showing selection procedure of the power circuit parameters.

## **2.6 Conclusions**

The chapter has presented the power circuit configuration and the working principles for different modes of operation. Design equations for the power circuit were derived in the general case and for any type of load. The analysis demonstrates that with the proposed configuration the current in the neutral wire is substantially decreased. Moreover, the chapter shows that the switching frequency, the synchronous link reactor and the dc voltage are related to each other and that they depended upon the parameters of the load. Accordingly a systematic design procedure is presented to select the power circuit parameters in order to obtain the appropriate parameters of the active filter.

## **Chapter 3**

### **RATING ISSUES AND DC BUS CAPACITOR SELECTION**

#### **3.1 Introduction**

The previous chapter has presented a general design procedure to select the power components. A constant dc bus voltage has been assumed. However, the force commutated voltage source inverter consists of a self controlled dc bus, and capacitors are used as a reservoir of energy to maintain constant the dc voltage and to reduce the voltage fluctuation under load variation. This chapter presents a design procedure to select the capacitor value in such a way as to ensure the proper operation of the harmonic compensator for various load environments. The impact of the ripple voltage on the active filter compensation capability is also investigated. Rating issues of the active filter and the power components are discussed in detail as a function of various system parameters. An example is detailed to illustrate the complete design process for the power circuit. Finally, simulation results are presented to show the static performance of the active filter and to confirm theoretical calculations.

### **3.2 Design of the Capacitors**

Under steady state operating conditions the dc voltage control loop keeps the dc voltage constant. However, transient changes in the instantaneous power absorbed by the load generate voltage fluctuations across the dc capacitor. The amplitude of these voltage fluctuations can be controlled effectively with an appropriate dc capacitor value [57] :

When designing the capacitor the following assumptions are made:

- ii) in steady state, the fluctuating voltage of the capacitor is very small compared to the average voltage.
- ii) the converter is lossless.

The voltage fluctuation in the dc capacitor under steady state is due to the variation of the harmonic power flow [58] [57] and the energy stored in the inductor. The current in the inductor has two components, the distorted current and the ripple current superimposed on the reference due to the switching action of the converter. The first current is a periodic ac waveform, hence the energy variation is null. The second part consist of the energy that the inductor discharges in the capacitor within one switching period. During the on state, energy is accumulated across the inductor and this energy is absorbed by the capacitor during the off state. Because the switching frequency is high, the effect of this energy variation on the dc bus is neglected.

For the single phase case, by equalizing the instantaneous input power to the instantaneous output power we obtain.

$$v_s \cdot i_{of} = i_{dc1} \cdot v_{dc1} + i_{dc2} \cdot v_{dc2} \quad (3.1)$$

$$v_{dc1} = V_{dc1} + \tilde{V}_{dc1} \quad \text{and} \quad v_{dc2} = V_{dc2} + \tilde{V}_{dc2} \quad (3.2)$$

$$i_{dc1} = 2 \cdot C \cdot \frac{d\tilde{V}_{dc1}}{dt} \quad \text{and} \quad i_{dc2} = 2 \cdot C \cdot \frac{d\tilde{V}_{dc2}}{dt} \quad (3.3)$$

Using the fact that the average dc voltage of each capacitor are approximately equal, then (3.1) could be written as :

$$v_s \cdot i_{af} = C \cdot V_{dc} \cdot \frac{d\tilde{V}_{dc}}{dt} \quad (3.4)$$

$$v_s = V_s \cdot \sqrt{2} \cdot \sin \omega t \quad (3.5)$$

$$i_{af} = \sum_{h=3,5}^{\infty} I_{af,h} \cdot \sqrt{2} \cdot \sin(h \cdot \omega \cdot t - \phi_h) \quad (3.6)$$

The voltage fluctuation,  $\Delta V_{dc}$  across the capacitor is :

$$\Delta V_{dc} = (\tilde{V}_{dc})_{\max} - (\tilde{V}_{dc})_{\min} \quad (3.7)$$

The energy variation,  $\Delta E$ , across the capacitor is :

$$\Delta E = E_{\max} - E_{\min} \quad (3.8)$$

Where

$$E = \int_0^t v_s \cdot i_{af} \cdot dt \quad (3.9)$$

$$\Delta V_{dc} = \frac{\Delta E}{C \cdot V_{dc}} \quad (3.10)$$

It can be shown that using reasonably high switching frequency the instantaneous energy can be written as:

$$E = \int_0^t v_s \cdot i_{load,h} \cdot dt \quad (3.11)$$

Equation (3.10) shows that the voltage fluctuation across the capacitor is a function of the converter instantaneous energy fluctuation, the dc bus voltage and the size of the capacitor.

The dc voltage regulation ratio is defined as :

$$r_v = \frac{\Delta V_{dc}}{V_{dc}} \quad (3.12)$$

Finally the minimum capacitor value to meet the required voltage regulation is given by :

$$C_{\min} = \frac{1}{V_{dc}^2 \cdot r_v} \Delta E \quad (3.13)$$

For three phase case equation (3.13) is replaced by :

$$E = \int_0^t \left( \sum_{j=a,b,c} v_{s,j} \cdot i_{j,h} \right) \cdot dt \quad (3.14)$$

The capacitors are designed to limit the dc voltage ripple to a specified value, typically 1 to 2 %. In our case the capacitor should be designed for the worst case, since the active filter will operate in several modes (single phase or unbalanced load). It follows that the capacitor value is load dependent and simulation is one way of evaluating the worst possible case. It will be shown in section 3.6, that the worst case occurs when the active filter is compensating a single phase load. The harmonic frequencies of the dc bus voltage in the case of a single phase load, can be found by expanding (3.13) .

$$E = \int_0^t \sum_{h=2,4}^{\infty} (V_s \cdot \sqrt{2} \cdot I_h \cdot \sqrt{2} \cdot \sin(\omega \cdot t) \cdot \sin(h \cdot \omega \cdot t - \phi_h)) dt \quad (3.15)$$



Transforming the product into summation yields :

$$E = \int_0^t \sum_{h=2,4}^{\infty} \left\{ 2 \cdot V_s \cdot I_h \left( \cos[(h-1)\omega t - \phi_h] - \cos(h+1)\omega t - \phi_h \right) \right\} \quad (3.16)$$

Integrating (3.18) one obtains :

$$E = \sum_{h=2,4}^{\infty} \left\{ V_s \cdot I_h \left( \frac{1}{(h-1)\omega} \sin[(h-1)\omega t - \phi_h] - \frac{1}{(h+1)\omega} \sin[(h+1)\omega t - \phi_h] \right) \right\} + cte \quad (3.17)$$

The above expression shows that the dc bus voltage has harmonic components at twice the mains frequency, resulting from the third harmonic of the load, a harmonic component at four times the mains frequency, which is the contribution of the third and fifth harmonic of the load, hence all the even harmonics are present in the spectrum of the dc bus voltage. A similar reasoning show that, under unbalanced load condition, the spectrum of the dc bus has similar harmonic distribution. However, under balanced load condition, the dc bus ripple components are located at multiples of six times the mains frequency.

### **3.3 Dc Capacitor Voltage for Step Changing Load**

In some cases, a load has a sudden change, such as disconnection from the ac line or sudden connection to the ac line. When the load current is dropped, the active filter current has not yet changed until the next cycle. Hence this extra current,  $\Delta I_{af}$ , will charge the capacitor [38] [58]. Where  $\Delta I_{af}$  is the step drop of the peak value of the active

filter accompanied with the drop of the fundamental load current. From (3.1) we have :

$$\frac{C}{2} \cdot \left( \frac{dv_{dc}^2}{dt} \right) = v_s \cdot i_{af} \quad (3.18)$$

Let  $V_{dc}(\infty) = V_{dc} + \Delta V_{dc}$ , then equation (3.18) becomes :

$$\Delta V_{dc}^2 + 2 \cdot V_{dc} \cdot \Delta V_{dc} - \frac{4 \cdot V_s \cdot \sqrt{2} \cdot \Delta I_{af}}{C \cdot \omega} = 0 \quad (3.19)$$

The previous equation shows that the voltage rises when the load steps down. For the calculated value  $C$ , the voltage rise is obtained by solving the second order equation. If the voltage rise is not permissible, then the new value of the capacitor is obtained by imposing a permissible voltage range. It is found that the new value of the capacitor is greater than the first value obtained in Section 3.2.

Similarly, when the load current has a step increase, the energy stored in the capacitor must be released immediately to support the step increase of the power consumed by the load. In this case the  $\Delta I_{af}$  is replaced by  $-\Delta I_{af}$  and the voltage drop  $\Delta V_{dc}$  is replaced by  $-\Delta V_{dc}$  in (3.19), hence obtaining the voltage drop. Equation (3.19) will be validated by simulation results in chapter 4.

### **3.4 Active Filter Current Compensation Capacity**

The maximum current that the active filter can compensate is calculated in function of the frequency of the current to track. The information is obtained using the maximum rate of rise of the current to compensate as equal to the maximum rate of rise generated by the active filter.

The current to compensate is given by :

$$i_h = \hat{I}_h \cdot \sin(\omega_h t - \varphi_h) \quad (3.20)$$

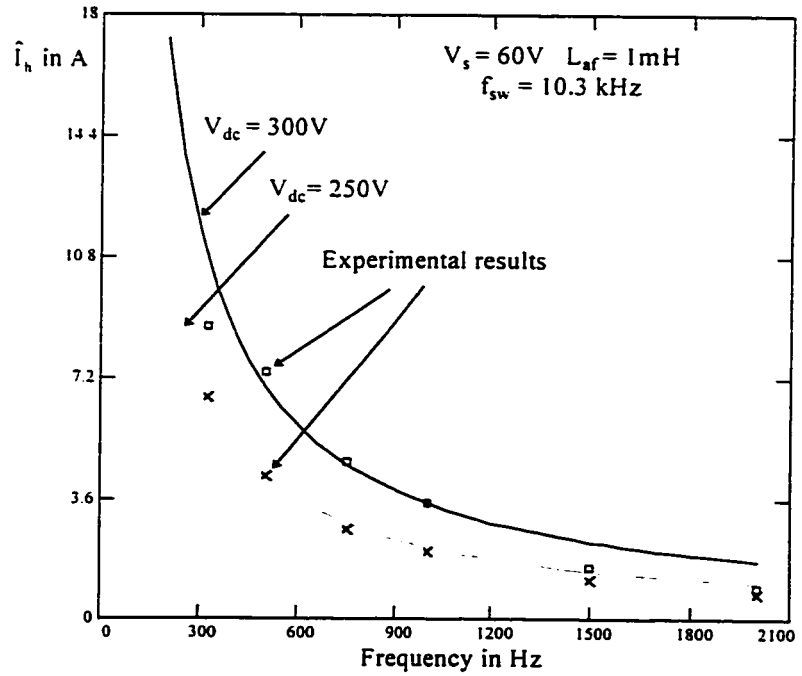
Since the  $di/dt$  capability of the active filter is dictated by :

$$\frac{di_{af}}{dt} = \frac{0.5 \cdot V_{dc} - V_s \cdot \sqrt{2}}{L_{af}} \quad (3.21)$$

The compensation capability is calculated by combining (3.20) and (3.21) :

$$\hat{I}_h = \frac{0.5 \cdot V_{dc} - V_s \cdot \sqrt{2}}{2 \cdot \pi \cdot f_h \cdot L_{af}} \quad (3.22)$$

The curves in Fig 3.1 show that the compensation capability of the active filter increases if the dc bus voltage is increased.



**Fig. 3.1** Peak current compensation capability of the active filter in function of the frequency with dc bus voltage as parameter.

### **3.5 Effect of the Dc Bus Ripple on the Compensation Capability**

Up to now the dc bus voltage was assumed flat and exempt of ripple. To study the effect of the capacitor, a ripple component at twice the mains frequency is considered in the dc bus voltage. The instantaneous dc bus voltage is expressed as :

$$v_{dc} = V_{dc} + A_r \cdot \sin(2 \cdot \omega \cdot t - \varphi_r) \quad (3.23)$$

Where  $A_r$  is the amplitude of the ripple component. Relating the amplitude of the ripple to the voltage regulation ratio one obtains :

$$v_{dc} = V_{dc} + \frac{V_{dc}}{2} \cdot r_v \sin(\omega_r t - \varphi_r) \quad (3.24)$$

The compensation capability of the active filter is given by :

$$\left( \frac{di}{dt} \right)_{af} = \frac{0.5 \cdot v_{dc} - v_s}{L_{af}} \quad (3.25)$$

Within a switching period of the converter, the worst case occurs when the ripple component is at its minimum value, thus reducing the driving voltage necessary to generate the  $di/dt$  :

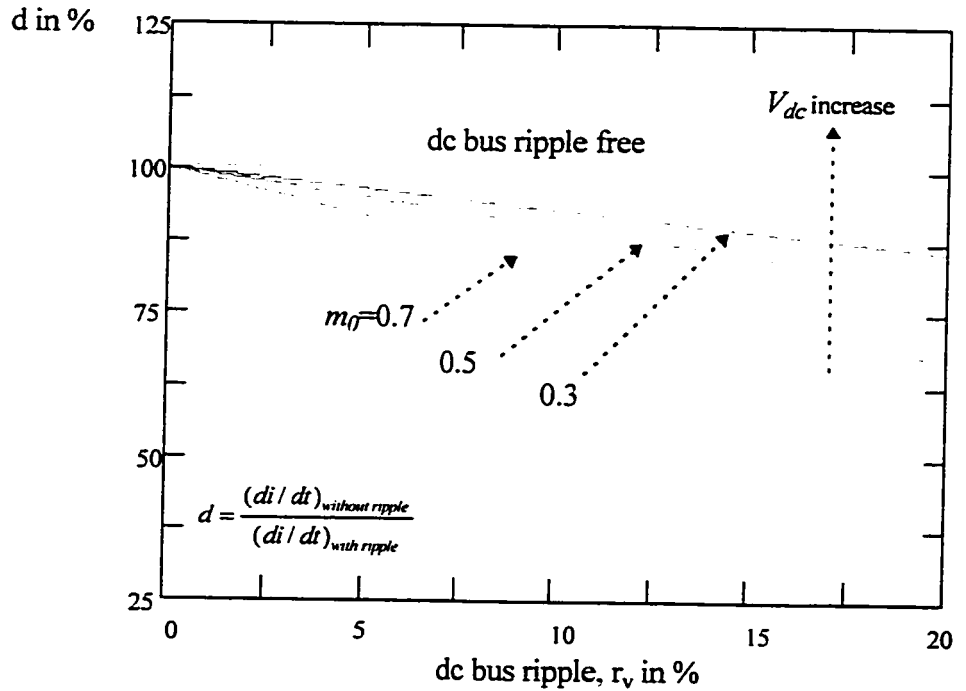
$$\left( \frac{di}{dt} \right)_{af} = \frac{0.5 \cdot V_{dc} - r_v \cdot V_{dc} / 4 - V_s \cdot \sqrt{2}}{L_{af}} \quad (3.26)$$

Let  $d$  represents the ratio of the  $di/dt$  of the active filter with ripple over the  $di/dt$  of the active filter without ripple. Moreover, this ratio represents also the ratio by which the peak current is reduced in the presence of ripple in the dc bus voltage.

$$d = \frac{(di / dt)_{with\ ripple}}{(di / dt)_{without\ ripple}} \quad (3.27)$$

$$d = \frac{1 - 0.5 \cdot r_v - m_0}{1 - m_0} \quad (3.28)$$

The ripple in the dc bus introduces a voltage drop at the output of the active filter, thus reducing the driving voltage across the inductor. The effect of the ripple is presented in Fig. 3.2. The curves show that the compensation capability of the active filter decreases when the ripple in the dc bus voltage increases. A smaller capacitor value is allowed, provided that the  $di/dt$  of the active filter remains higher than the  $di/dt$  of the distorting current.



**Fig. 3.2** Effect of the dc bus ripple on the  $di/dt$  capability of the active filter with dc bus voltage as parameter.

### **3.6 Required Harmonic Power by the Active Filter**

To obtain sinusoidal current at the mains, harmonic power is injected into the system, thus canceling the distorting power of the load. In the general case, if reactive power and harmonic power is injected,  $H+Q$ , then from appendix A1 we have :

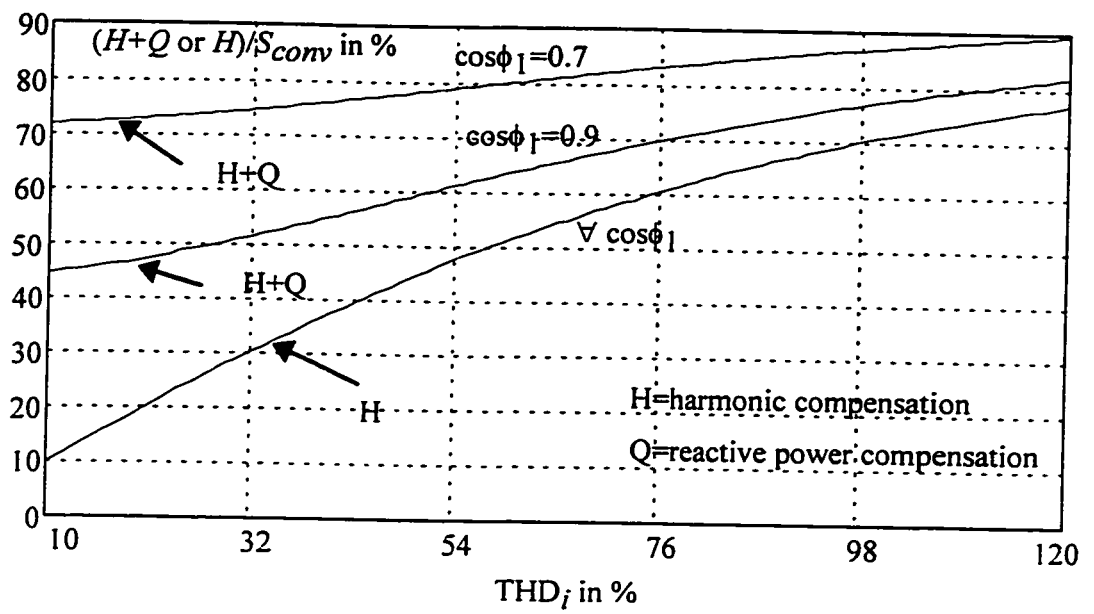
$$\frac{H+Q}{S_{conv}} = \sqrt{\frac{(\sin \phi_1)^2 + THD_i^2}{1 + THD_i^2}} \quad (3.29)$$

Fig. 3.3 gives the required reactive and harmonic power from the active filter relative to the rating of the load converter, as a function of the total harmonic distortion of load current,  $THD_i$ , for several displacement power factors. The curves show that if reactive power is combined with harmonic compensation, the required rating is substantially increased. Also, the curves in Fig. 3.3 show that the required rating increases with a faster rate as the load  $THD_i$  increases. For harmonic compensation, the expressions given below are used :

$$H = V_s \cdot I_1 \cdot THD_i \quad (3.30)$$

$$\frac{H}{S_{conv}} = \frac{THD_i}{\sqrt{1 + THD_i^2}} \quad (3.31)$$

The main difference between combined harmonic and reactive compensation,  $H+Q$ , and harmonic injection,  $H$ , is power factor correction. In the first case the current in the mains has a unity power factor and a sinusoidal waveform, in the latter case, the supply is harmonic free, however the supply voltage and current are not in phase.



**Fig. 3.3** Required harmonic and reactive power from the active filter in function of load  $THD_i$ .

### **3.7 Rating of the Synchronous Link Reactor**

The rating of the synchronous link reactor is specified in terms of an inductor equivalent rating at 60 Hz, giving an indication of inductor cost/size.

$$S_{Laf} = \omega \cdot L_{af} \cdot (i_{af})_{rms}^2 \quad (3.32)$$

The dominant components in the expression of the active filter current are the low frequency harmonics, therefore we obtain :

$$\frac{S_{Laf}}{S_{load}} = \frac{L_{af} \cdot \omega \cdot I_1}{V_s} \cdot THD_i \quad (3.33)$$

### 3.8 Capacitor and Inverter Rating

The total VA rating of the dc side capacitors is the product of the rms current and rms voltage :

$$S_{cap} = v_{dc1,rms} \cdot i_{dc1,rms} + v_{dc2,rms} \cdot i_{dc2,rms} \quad (3.33)$$

The rating of the inverter is the same as the rating of the inverter, and is given by the product of rms voltage at its terminal and the rms current of the distorting current:

$$S_{af} = V_{af,rms} \cdot I_{af,rms} \quad (3.34)$$

The rating of the inverter is different from the injected harmonic power, since the voltage at the point of common coupling is smaller than the terminal voltage of the inverter due to the voltage drop across the inductor.

$$\frac{S_{af}}{S_{load}} = \frac{S_{cap}}{S_{load}} = THD_i \cdot \sqrt{1 + (x_{af})^2 \cdot \sum_{h=2}^{\infty} (h \cdot \frac{I_h}{I_1})^2} \quad (3.35)$$

Where  $x_{af}$ , is the synchronous link reactor value in pu. The rms value of dc current for each capacitor is half the active filter current.

$$i_{dc1,rms} = i_{dc2,rms} = \frac{I_1 \cdot THD_i}{2} \quad (3.36)$$

The rated peak terminal voltage of the active filter is given by the product of the modulation index and half the dc bus voltage,

$$\frac{V_{af,pk}}{V_s} = \frac{m}{m_0} \quad (3.37)$$



### 3.9 Design Example

Apparent power of the load and the supply voltage are selected as base values

$$S_{base} = S_{load} = 3 \cdot V_s \cdot I_1$$

$$V_{base} = V_s \text{ and } I_{base} = \frac{S_{base}}{V_{base}}$$

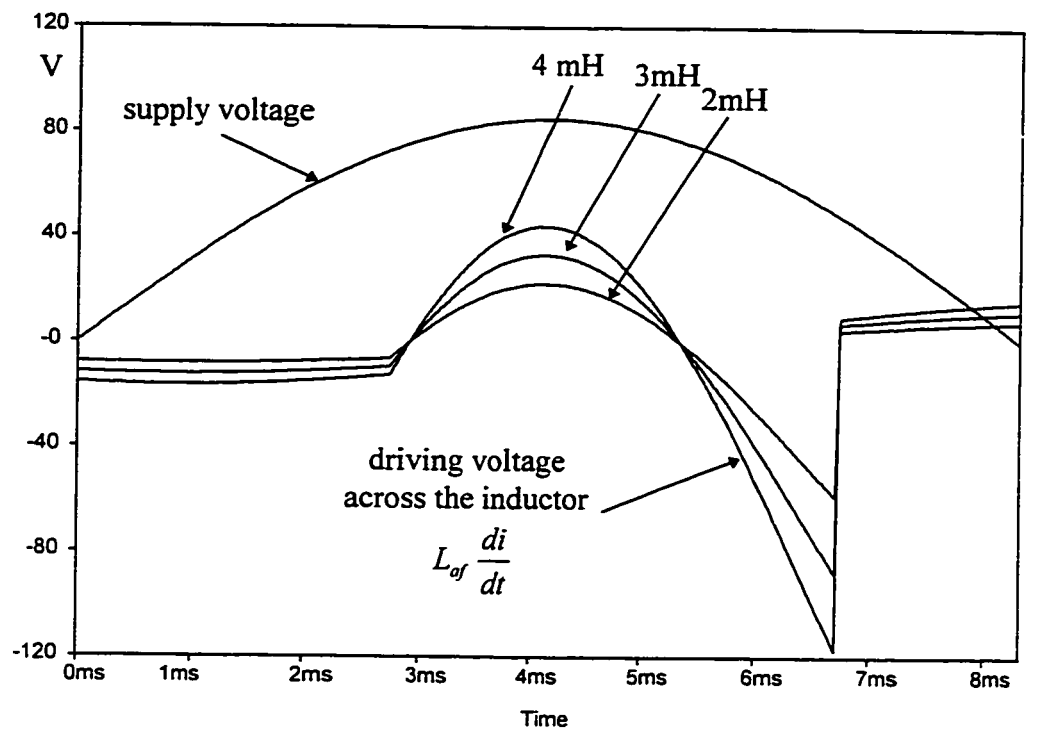
1) *Load specification* : In this example the mains is supplying three unbalanced single phase loads, connected between the lines and the neutral. Each load consists of a diode rectifier with a capacitive output in parallel with the load resistor. The data for the single phase load is :

$$V_s = 60 \text{ V } I_1 = 7.8 \text{ A}$$

$$I_{h,peak} = 11 \text{ A, } THDi = 70 \%,$$

$$(di/dt)_{max} @ \text{positive slope} = 11 \text{ kA/s.}$$

2) *Active Filter* : The switching frequency is chosen equal to 10.3 kHz. The modulation index must be close as possible to 1.0, so that inverter output exhibits low harmonic content, in our case, the modulation index is chosen equal to 0.9. The dc bus voltage value  $V_{dc}$  and the reactor value  $L_{af}$ , are extracted by iteration using the flowchart of Chapter 2, Fig. 2.7. Choosing  $V_{dc} = 265\text{V}$ , ( $m_0 = 0.65$ ), the minimum required inductance becomes 2.2 mH.



**Fig. 3.4** Supply voltage and the driving voltage across the inductor in function of time.

Fig. 3.4 shows that the maximum positive slope of the distorting current represents the worst condition. In order to meet the modulation index requirement, the inductor is chosen equal to 3 mH.

For single phase operation, the capacitor value is selected according to equation

(3.15). Simulation results show that the voltage fluctuation is  $\Delta V_{dc} = \frac{1.17}{C \cdot V_{dc}}$ , for

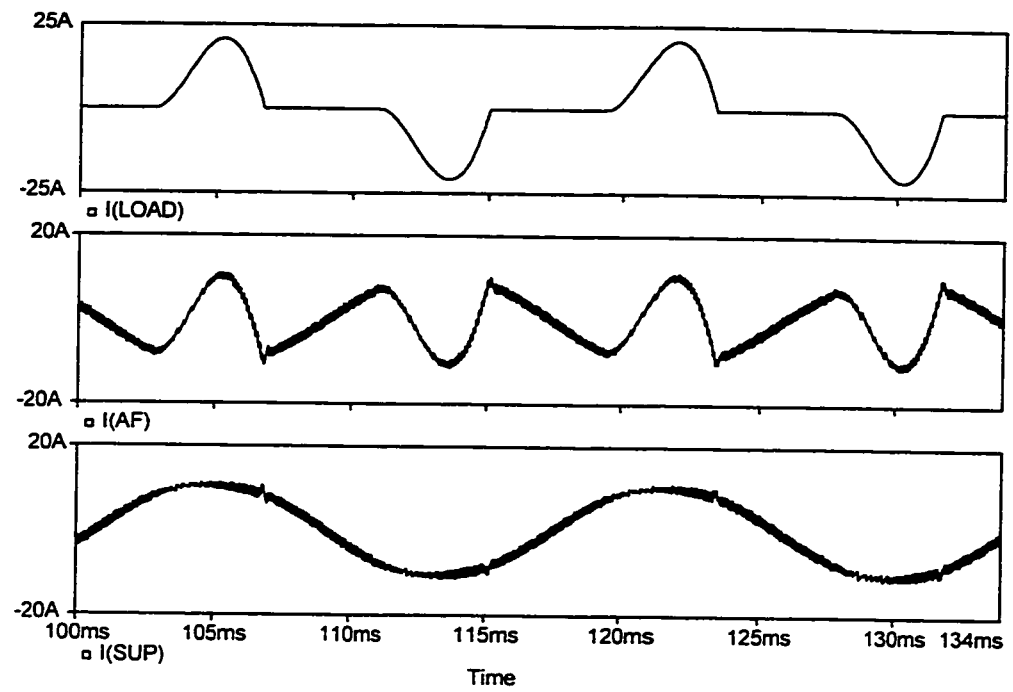
balanced three phase operation  $\Delta V_{dc} = \frac{0.32}{C \cdot V_{dc}}$ , and for unbalanced three phase operation

$\Delta V_{dc} = \frac{0.776}{C \cdot V_{dc}}$ . Choosing a voltage regulation ratio of  $r_v < 2\%$  ( $\Delta V_{dc} < 5V$ ), for single

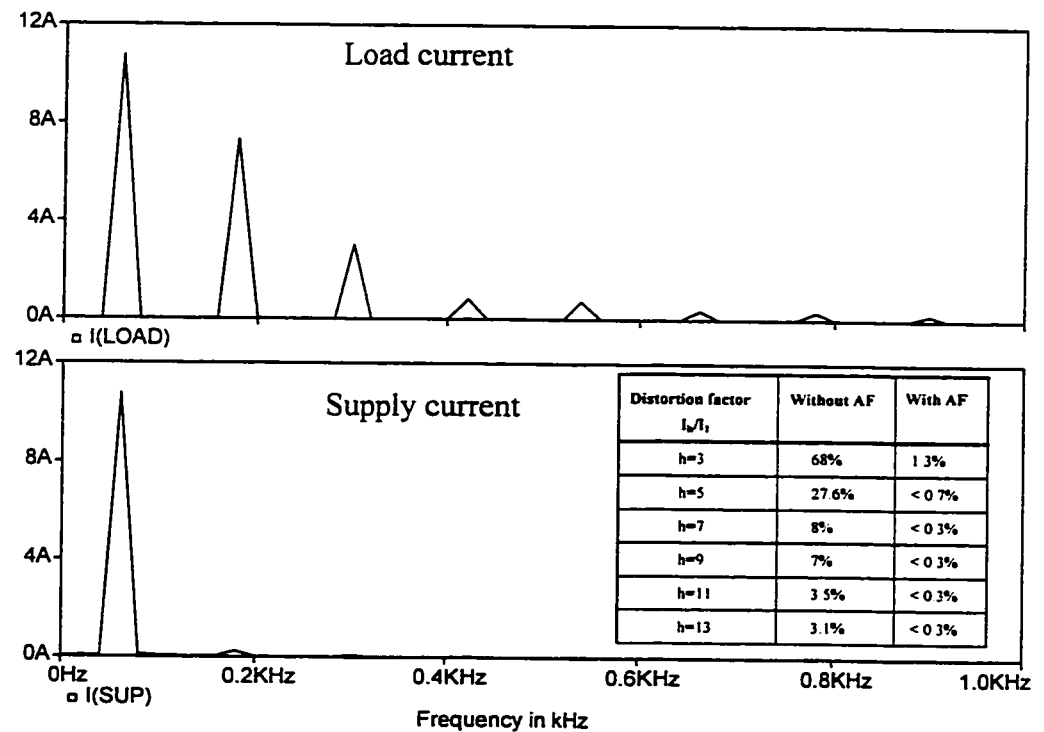
phase operation the minimum required capacitor is 800  $\mu\text{F}$ , for the same percentage of ripple, calculations show that for a typical unbalanced load case  $C_{min} = 500\mu\text{F}$  and for the balanced three single phase loads case  $C_{min} = 200\mu\text{F}$ . It is obvious that the single phase operation represents the worst case, thus the capacitor will be designed for this mode of operation. For this example a capacitor of 900  $\mu\text{F}$  is chosen. Table 3.1 summarizes the design data of the active filter valid for balanced, unbalanced and single phase load operation. The designed system is simulated and results are presented in Fig. 3.6 and Fig. 3.7 respectively. Simulated results show that after compensation, the supply current, Fig. 3.6 (c) is perfectly sinusoidal and the distorted current is eliminated. The spectrum of the supply current in Fig. 3.7 (b), show that the remaining dominant low harmonic current is at the fundamental frequency.

**Table 3.1 Active filter design values**

$S_{base} = S_{load}$	1.4 kVA = 1 pu
$V_{base}$	60 V = 1 pu
$I_{base}$	7.8 A = 1 pu
$f_{sw} / f$	170 pu
$x_{af}$	0.146 pu
$x_c$	0.38 pu
$S_{Laf}$	0.11 pu
$S_{cap} = S_{af}$	0.75 pu
$V_{af,pk}$	1.65 pu



**Fig. 3.5** Simulation results. a) load current b) injected current c) supply current after compensation.



**Fig. 3.6** Simulation results. Load and supply currents spectrum.

### **3.10 Conclusions**

The chapter presented a detailed analysis to design the dc capacitors of voltage source inverter based active filter. The effect of the ripple in the dc bus on the compensation capacity of the active filter was also studied. It was shown that the ripple reduces the rate of rise of current, and the compensation capability of the active filter. Moreover, it was shown that the worst possible case for the four wire active filter occurs when it is compensating a single phase load. On the other hand, rating issues such as rating of the reactor, rating of the capacitors and rating of the active filter were evaluated in function of the parameters, thus giving an insight to the size and cost of the converter. An example was added to illustrate the complete design of the power circuit which is valid for balanced, unbalanced and single phase load conditions. Finally theoretical results and design values have been validated by simulation.

## **Chapter 4**

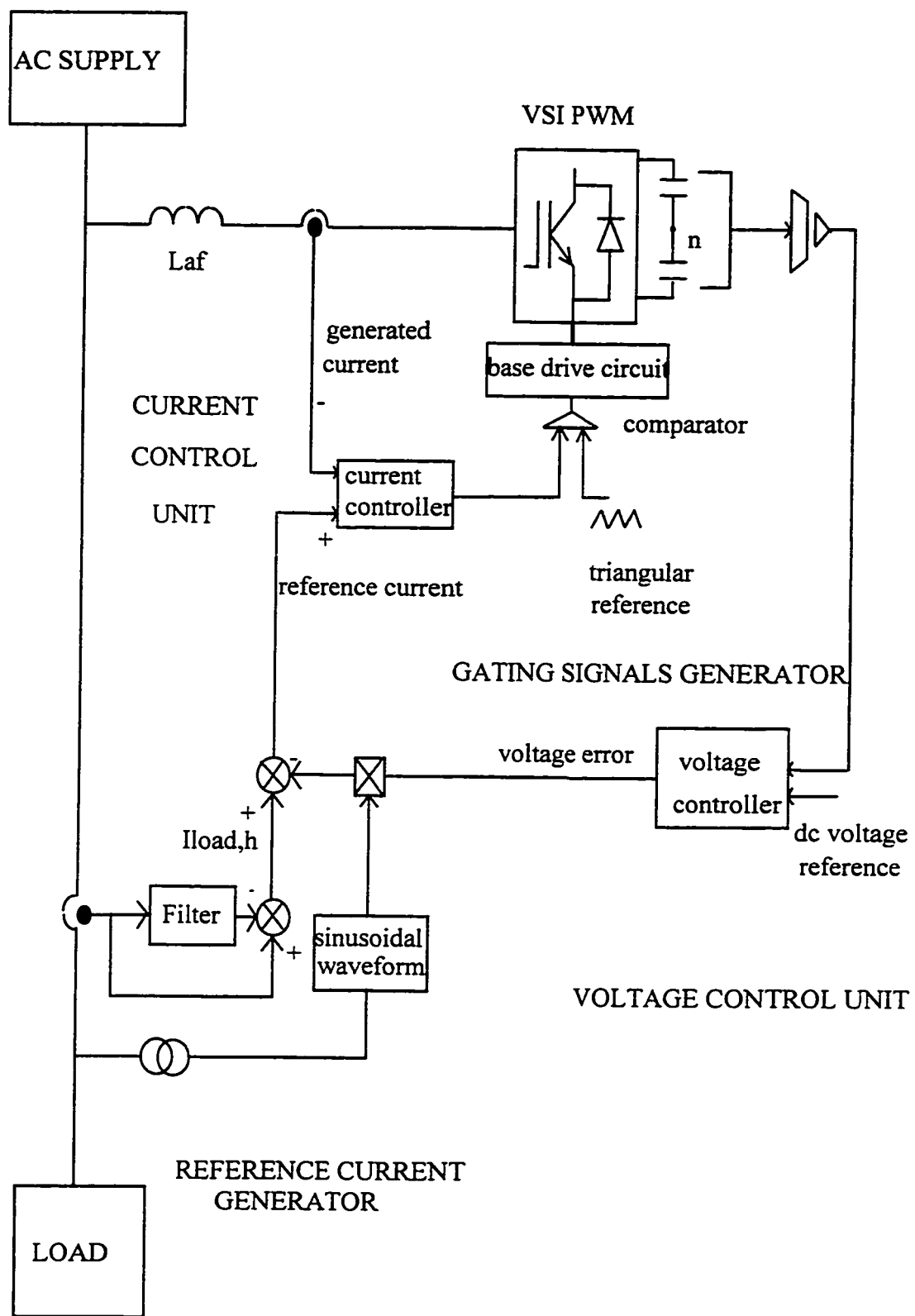
### **CONTROL SYSTEM DESIGN**

#### **4.1 Introduction**

This chapter deals with the control circuits of the active filter. The fundamental component is extracted from the load current to obtain a reference signal for the control circuit. This reference signal is synthesized by the means of a voltage source inverter. The gating signals are obtained from a carrier-based PWM modulator. The control system consist of : a) a reference current generator unit, b) a current control unit, c) a voltage control unit, and d) a gating signals generator. Design guidelines for the current and voltage loops are included to facilitate the selection of controllers parameters. The dynamic performance of the filter is evaluated through quantified residual currents and simulation results.

#### **4.2 Control Circuits Description**

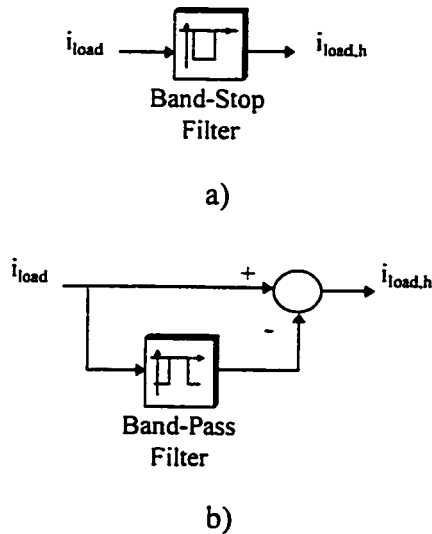
A brief functional description of the building blocks of the control system as shown in Fig. 4.1 are given in the following subsections.



**Fig. 4.1** Active filter control block diagram

### 4.2.1 Reference Current Generator

This unit generates the harmonic component of the load current that the inverter is forced to follow. The distorted load current could be obtained in a number of ways, among which: i) band stop filter centered around the fundamental frequency and rejecting this component, Fig. 4.2(a), ii) band-pass filter centered around the fundamental frequency and isolating this component which is then subtracted from the total current Fig. 4.2(b). Phase shift and gain attenuation introduced in the filter output must be as small as possible in order to accomplish cancellation of load harmonics. Option b) has superior residual characteristics compared to a) [38], therefore it is chosen in the actual implementation.



**Fig. 4.2** Harmonic current extraction options.

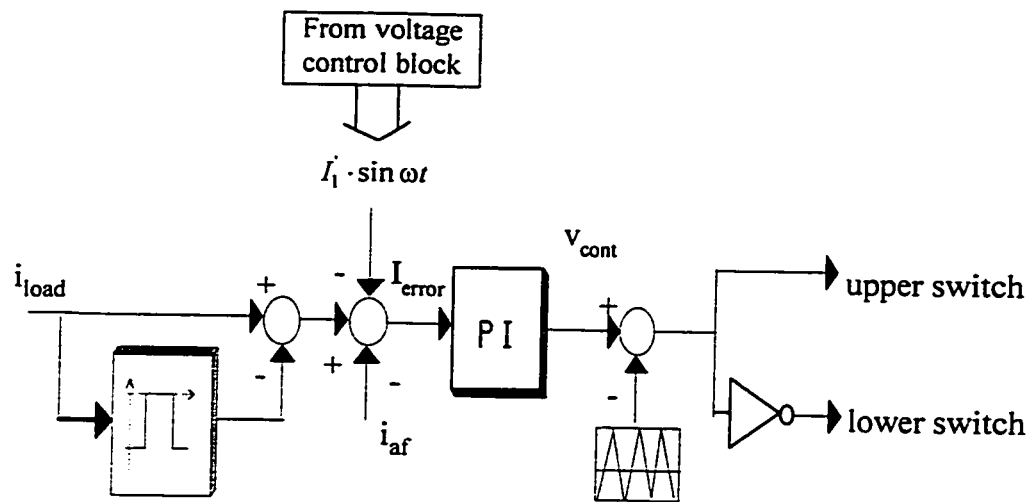


### 4.2.2 Current Control Unit

The function of the current control unit is to generate the error signal by subtracting the measured current from the actual current. Then the error is processed through the current controller to produce the modulating or the control signal. The PI structure is chosen for the controller implementation since it contributes to zero steady state error.

### 4.2.3 Gating Signals Generator

A constant switching frequency is achieved by comparing the current error signal with a triangular reference waveform. By introducing the triangular waveform the inverter switching frequency is stabilized by forcing it to be constant and equal to the frequency of the triangular reference. The proposed method can be explained by considering the hysteresis technique plus the addition of a fixed frequency triangular waveform inside the imaginary window [59]. If the reference current,  $i_{load,h}$  is higher than the generated current,  $i_{af}$ , the error waveform is positive and when compared with the triangular waveform it results in a positive pulse. This pulse will then turn on the appropriate inverter bottom switch that will increase the corresponding output line current. In the same way if the reference current is smaller than  $i_{af}$ , the error waveform is negative, the gating signals are adjusted so that the line current decreases (a top switch is turned). These gating signals are generated from the intersection of a triangular waveform superimposed on the reference wave as shown in Fig 4.3.



**Fig. 4.3** Per phase current control.

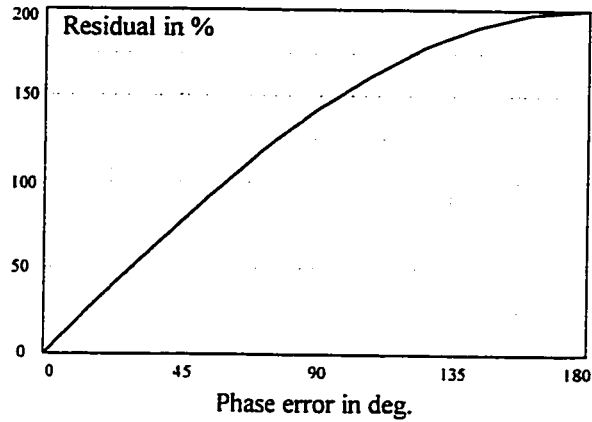
#### 4.2.4 Voltage Control Unit

The dc voltage control unit keeps the voltage across the dc capacitor to its preset value. The voltage across the dc capacitor is controlled by adjusting the small amount of real power absorbed by the inverter. By controlling the amplitude of the fundamental current, the PWM inverter absorbs the real power required to cover the inverter switching losses and to maintain the steady state dc capacitor voltage constant.

### 4.3 Design of the Extraction Circuit

In order to obtain the distorting component of the current, the extraction circuit must isolate the fundamental without altering the magnitude of the harmonics and keeping the phase shift to zero. This will achieve perfect cancellation of harmonics. The

effect of phase shift by  $\Delta\phi$ , between the injected and reference current on the residual current is shown in Fig. 4.4.



**Fig. 4.4** The effect of phase error on residual current.

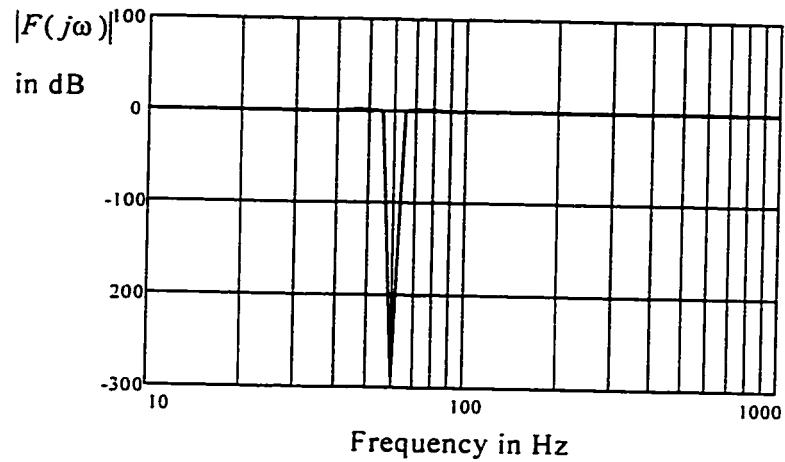
Fig. 4.4 shows that the residual current is a strong function of phase error. For example, a  $6^\circ$  phase error results in 10 % of that harmonic remaining, rather than complete cancellation. Moreover, phase errors larger than  $60^\circ$  will result in harmonic amplification rather than cancellation. In order to reduce the effect of phase shift, two second order cascaded band pass filters are used to isolate the fundamental. The transfer function of the band pass filter is given by :

$$F_b(s) = \frac{s/\omega_c \cdot q}{1 + s/\omega_c \cdot q + s^2/\omega_c^2} \quad (4.1)$$

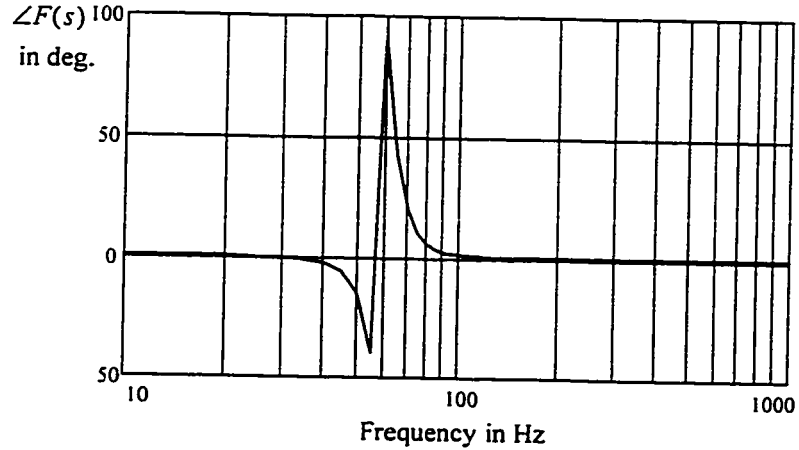
Where  $f_c = 1/2 \cdot \pi \cdot \omega_c$  is the cut-off frequency and  $q$  is the quality factor defined as the ratio of cut-off frequency to the frequency width of the filter,  $q = f_c/f_b$ . In our case  $f_b=15$  Hz and  $f_c=60$  Hz.

The complete transfer function of the extraction circuit is given as :

$$\frac{I_{load,h}(s)}{I_{load}(s)} = F(s) = 1 - F_b(s) \cdot F_b(s) \quad (4.2)$$



**Fig. 4.5** Gain of the extraction circuit in function of frequency.



**Fig. 4.6** Phase angle of the extraction circuit in function of frequency.

Fig. 4.5 and Fig. 4.6 show that a narrow band filter was achieved, and that the extraction process does not attenuate the harmonic components above the fundamental, and phase shift introduced is nearly zero.

#### **4.4 Design of Control Loops**

The design procedure for the current and voltage loop is based on the respective time response requirements, since the transient response of the active power filter is determined by the current control loop, its time response has to be fast enough to follow the current reference waveform closely. On the other hand, the time response of the dc voltage control loop need not to be fast but much slower than the current loop time response of the inverter. Thus, these two control systems can be regarded as decoupled and designed independently.

##### **4.4.1 Design of the Current Loop**

The transfer function of the extraction circuit is assumed equal to one at frequencies different than the fundamental, and equal to zero at fundamental frequency. Hence, it is not taken into account when designing the loop. The active power filter is implemented with voltage-source inverters, it follows that the ac output current is defined by the inverter ac output voltage. A PI controller is selected for the current loop since it

contributes to zero steady state error. The transfer function of the modulator is taken constant within the current loop bandwidth which is one third of the switching frequency. To ease the analyzes, the gain of the current transducers are lumped into the gain of the PI controller.

Where

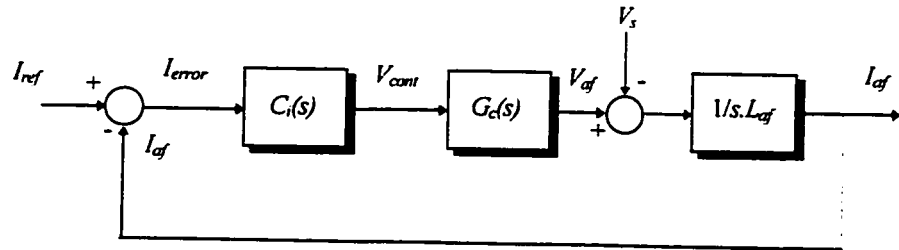
$V_s$  is the phase to neutral voltage;

$C_i(s) = k \cdot \left( \frac{1 + \tau \cdot s}{\tau \cdot s} \right)$  is the transfer function of the PI controller,

$G_c(s) = \frac{V_{dc}}{2 \cdot V_{tri}}$  is the transfer function of the converter,

$$I_{ref} = I_{load,h}$$

The design of the current loop is a two step operation. First the PWM part of the inverter is dealt, by forcing the slope of the error less than the triangular wave [60] [61], in this way linear operation of the modulator is ensured, and multiple crossing is avoided. Then the parameters of the PI controller are selected to satisfy time requirements of the current loop.



**Fig. 4.7** Current loop model.

The condition on the slope gives :

$$\left| \frac{d}{dt}(v_{cont}) \right| < \left| \frac{d}{dt}(v_{iri}) \right| \quad (4.3)$$

From Fig. 4.5 we have :

$$V_{cont}(s) = I_{error}(s) \cdot k \cdot \left( \frac{1 + \tau \cdot s}{\tau \cdot s} \right) \quad (4.4)$$

The time constant of the PI controller,  $\tau$ , is in the range of the switching period,  $T_{sw}$ , for this purpose the time constant can be written :

$$\tau = \alpha \cdot T_{sw} \quad (4.5)$$

In practice the slope of the control signal is set 75 % of the slope of the triangular wave, it follows that the gain of the PI controller for the worst case is :

$$k = \frac{3 \cdot f_{sw} \cdot L_{af}}{G_c \cdot \left( \frac{1}{4 \cdot \alpha} + 1 + m_0 \right)} \quad (4.6)$$

The last equation shows that the constraint on the slope relates the gain and time constant of the PI controller.

Since the supply voltage acts as disturbance, the closed loop transfer function is obtained as :

$$\frac{I_{af}}{I_{ref}} = \frac{2 \cdot \zeta \cdot \omega_0 \cdot s + \omega_0^2}{s^2 + 2 \cdot \zeta \cdot \omega_0 \cdot s + \omega_0^2} \quad (4.7)$$

Where

$$\omega_0 = \sqrt{k \cdot \frac{V_{dc}}{2 \cdot V_{iri}} \cdot \frac{1}{\tau \cdot L_{af}}} \quad (4.8)$$

and

$$\zeta = \frac{1}{2} \cdot \sqrt{k \cdot \frac{V_{dc}}{2 \cdot V_{tri}} \cdot \frac{\tau}{L_{af}}} \quad (4.9)$$

Replacing the expression of the gain in (4.9) we obtain

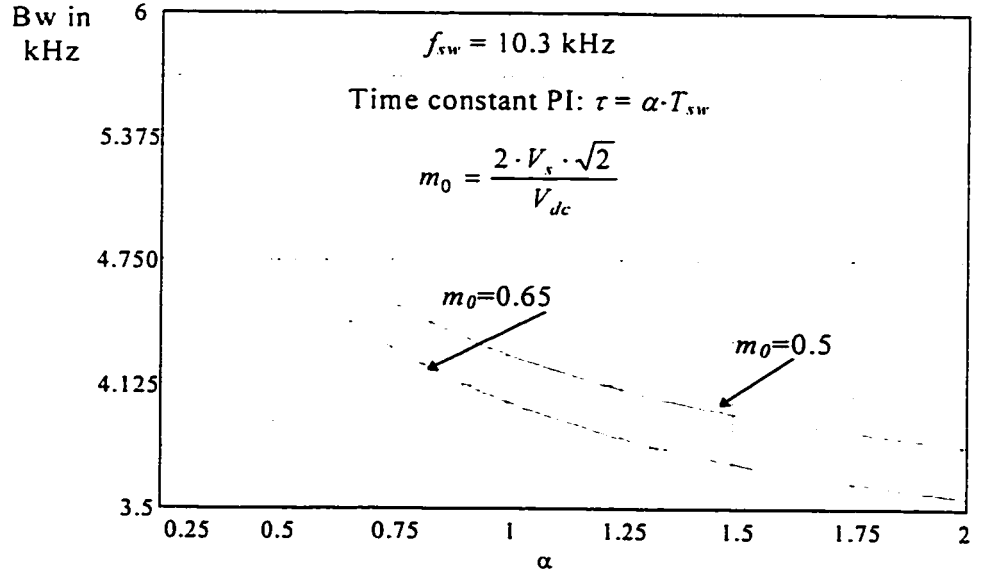
$$\zeta = \frac{1}{2} \sqrt{\frac{3 \cdot \alpha}{\left[ \frac{1}{4 \cdot \alpha} + 1 + m_0 \right]}} \quad (4.10)$$

$$\omega_0 = 2 \cdot \frac{f_{sw}}{\alpha} \cdot \zeta \quad (4.11)$$

The bandwidth of the active filter is determined by setting the module of the closed loop transfer function to 0.707.

$$BW = \frac{\omega_0}{2 \cdot \pi} \cdot \sqrt{(2 \cdot \zeta^2 + 1) + \sqrt{(2 \cdot \zeta^2 + 1)^2 + 1}} \quad (4.12)$$

Where  $BW$  is the bandwidth of the current loop in Hz.



**Fig. 4.8** Bandwidth of the active filter in function of time constant of the PI controller.

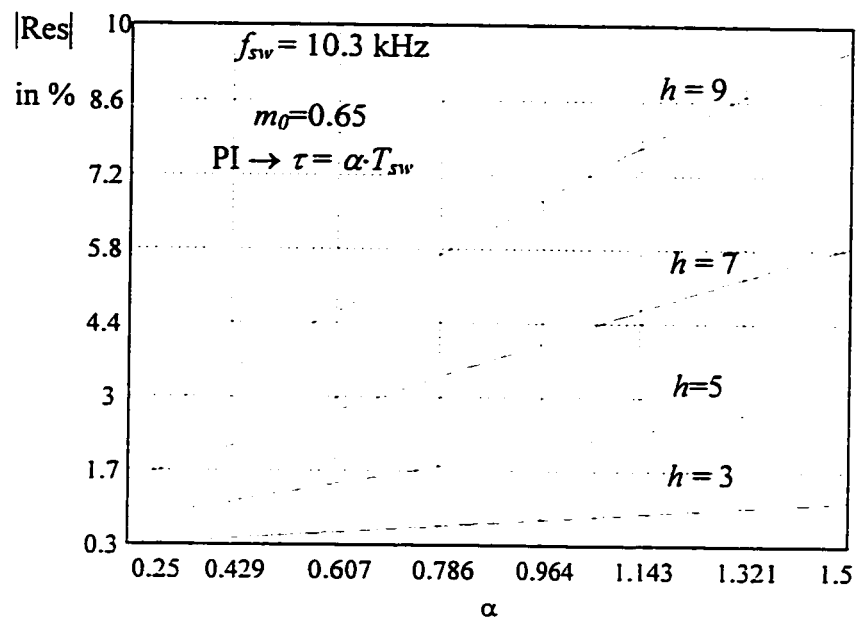


The curves in Fig. 4.8 show that the power components does not intervene in the bandwidth of the current loop. Also, the curves show, the dc bus voltage have negligible effect on the bandwidth. The intervening parameters are the switching frequency and the time constant of the PI controller.

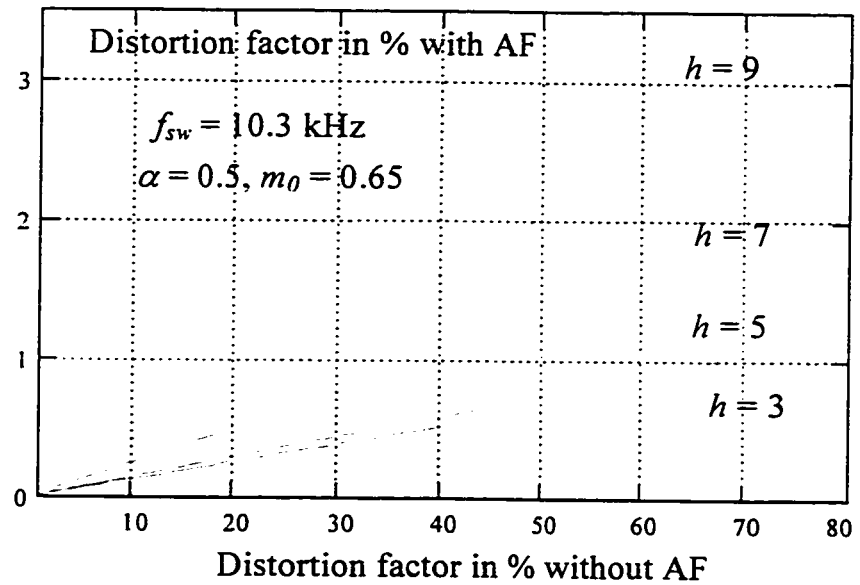
The residual currents are defined as the ratio between the magnitude of  $h^{th}$  harmonic after compensation to the magnitude of  $h^{th}$  harmonic before compensation.

$$|Res(j \cdot h \cdot \omega)| = \left| 1 - \frac{I_{af}(j \cdot h \cdot \omega)}{I_{ref}(j \cdot h \cdot \omega)} \right| \quad (4.13)$$

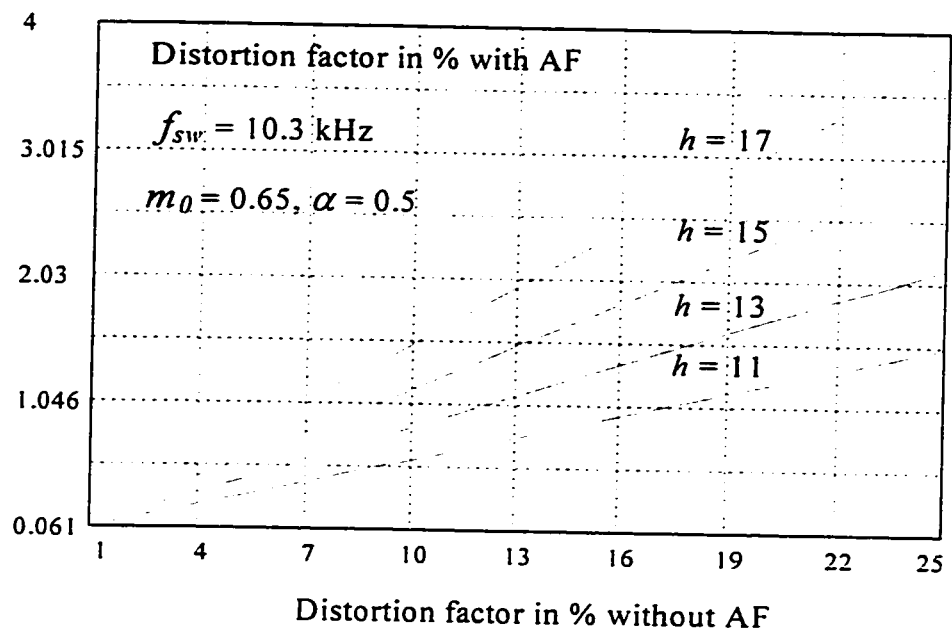
Equation (42) takes into account the combined effect of magnitude and phase angle of the injected current on the supply current, because the perfect cancellation of supply harmonics requires from active filter to inject a current of the same magnitude and phase angle of the distorted current. The curves of Fig. 4.9 show that the residual currents decreases when the time constant of the PI controller decreases. To obtain the individual harmonic distortion after compensation, the residual current at a specific frequency is multiplied by the corresponding harmonic distortion before compensation. Fig. 4.10 and Fig. 4.11 show the individual harmonic distortion after compensation taking into account the combined effect of the extraction circuit and the current loop. For example, the individual harmonic distortion of harmonic order 9, is 3.5 % compared to a value of 80 % before compensation.



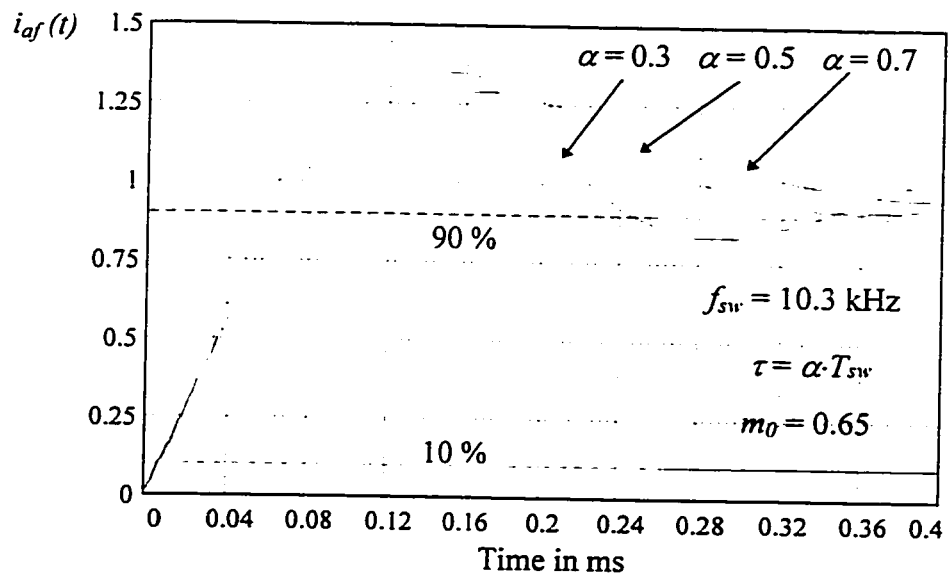
**Fig. 4.9** Residual current introduced by the current loop in function of the PI controller time constant.



**Fig. 4.10** Individual distortion factor after compensation in function of distortion factor before compensation.



**Fig. 4.11** Individual distortion factor after compensation in function of distortion factor before compensation for high order harmonics.

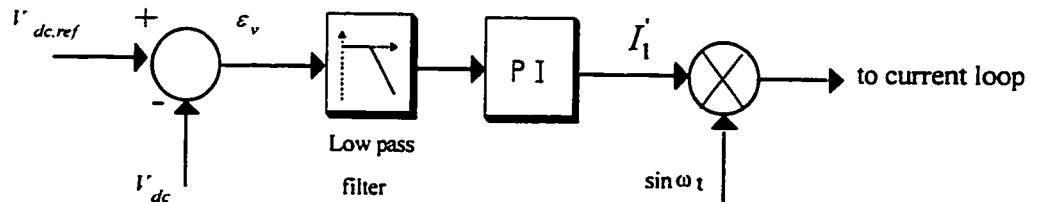


**Fig. 4.12** Response of the current loop for a step change in load.

The response time of the current loop is faster as the time constant of the PI controller is decreased, however the current exhibits higher overshoots. The time constant is chosen to half the switching period, thus giving an overshoot of 40 % and a response time of 0.625ms.

#### 4.4.2 Voltage Loop Design

If the converter is lossless, the mains supplies the demanded real power of the load, and the power converter supplies the harmonic power of the load in the steady state. Hence the dc capacitor is a buffer for the harmonic flow. Therefore no real power is supplied from the dc capacitor. The average voltage of the dc capacitor is maintained at a constant value, but the voltage of the dc capacitor is maintained at a constant value, and the voltage fluctuation cannot be avoided due to the harmonic power flow. Also the transient caused by the load change will result in the fluctuation of the capacitor voltage. To cover the switching losses and to keep the dc voltage constant, the real power absorbed by the inverter is controlled by adjusting the amplitude of the fundamental current reference,  $I_1'$ , as shown in Fig. 4.13.



**Fig. 4.13** Voltage control block.

Since the active filter will operate in single and unbalanced load conditions, the dc bus voltage has a ripple component at twice the mains frequency, hence the voltage ripple is reflected back to the voltage loop, passed through the PI controller and then forms part of the current reference along with the dc error, this current is then multiplied by a sine wave template, thus generating a third harmonic component. Assuming the inverter can follow exactly the reference, then the supply current will contain a third harmonic component. For this purpose a low pass filter is cascaded with a PI controller, Fig. 4.12. The analysis of the capacitor voltage regulation is carried out by assuming the load current to be zero.

For the low pass filter, the cut off frequency is chosen equal to 15 Hz .

$$\tau_f = 10 \text{ ms}$$

The power flow into the capacitor is expressed as :

$$\frac{\hat{V}_s}{2} \cdot I_1'(t) = v_{dc} \cdot idc + \frac{V_{dc}^2}{R_{losses}} \quad (4.14)$$

Equation (4.14) can be written as:

$$\frac{\hat{V}_s}{2} \cdot I_1'(t) = \frac{C}{2} \cdot \frac{dv_{dc}^2}{dt} + \frac{V_{dc}^2}{R_{losses}} \quad (4.15)$$

Considering variation around the operating point we have :

$$v_{dc} = V_{dc} + \Delta V_{dc} \quad (4.16)$$

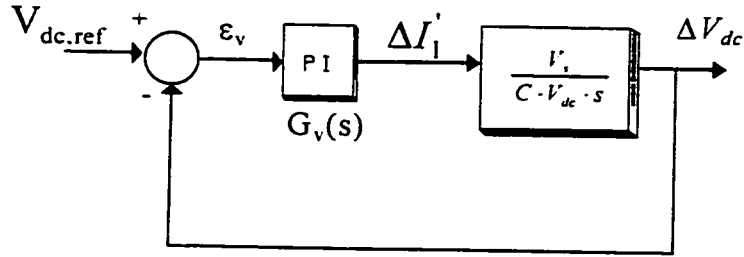
$$I_1' = I_{1,0}' + \Delta I_1' \quad (4.17)$$

In steady state, the mains supply the losses of the converter, therefore replacing the expressions of  $v_{dc}$  and  $I_1'$  in (4.15) we obtain :

$$\frac{\hat{V}_s}{2} \cdot \Delta I_1' = \frac{C}{2} \cdot \frac{d}{dt} (V_{dc} + \Delta V_{dc})^2 \quad (4.18)$$

Neglecting the second order terms and taking the Laplace transform of (4.18) we obtain :

$$\frac{\Delta V_{dc}(s)}{\Delta I_1'(s)} = \frac{\hat{V}_s}{2 \cdot C \cdot V_{dc} \cdot s} \quad (4.19)$$



**Fig. 4. 14** Model of the voltage loop at no load.

The transfer function of the controller is given by :

$$G_v(s) = k_v \frac{(1 + \tau_{vl} \cdot s)}{\tau_{vl} \cdot s} \cdot \frac{1}{1 + \tau_f \cdot s} \quad (4.20)$$

From Fig. 4.14, the open loop transfer function of the voltage loop is given by :

$$H_v(s) = \frac{k_v \cdot \hat{V}_s}{2 \cdot \tau_{vl} \cdot C \cdot V_{dc}} \cdot \frac{(1 + \tau_{vl} \cdot s)}{s \cdot (1 + \tau_f \cdot s)} \quad (4.21)$$

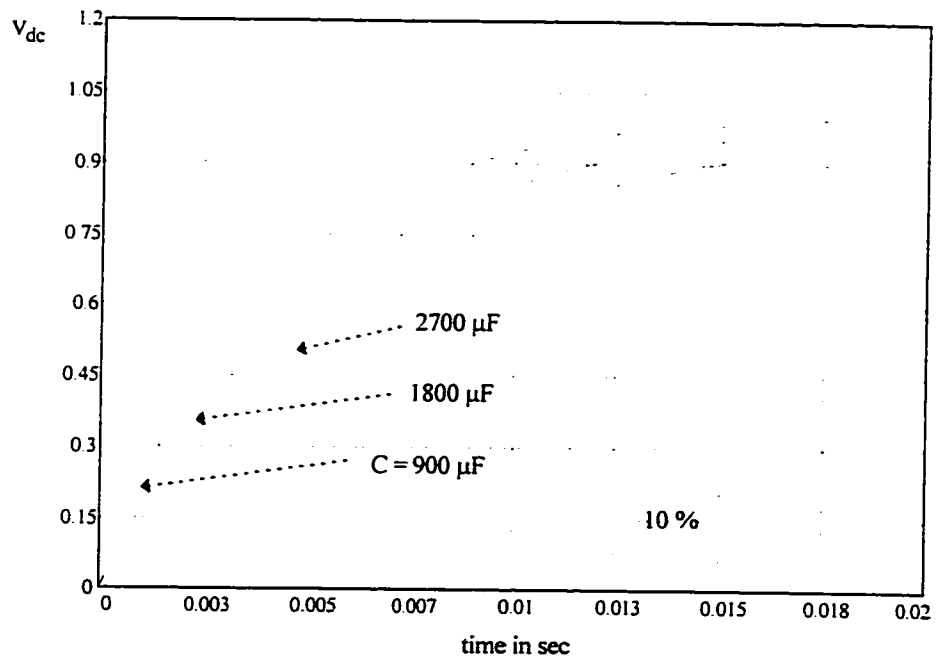
The closed loop transfer function of the voltage loop is given by :

$$\frac{V_{dc}(s)}{V_{dc,ref}(s)} = \frac{H_v(s)}{1 + H_v(s)} \quad (4.22)$$

For the example of Chapter 3, Section 3.10, the parameters of the PI controller are chosen as follows :

$$k_v = 1 \text{ and } \tau_{v1} = 0.5s$$

Finally, the response of the voltage loop for a step change in function of the dc bus capacitor value is shown in Fig. 4.15.



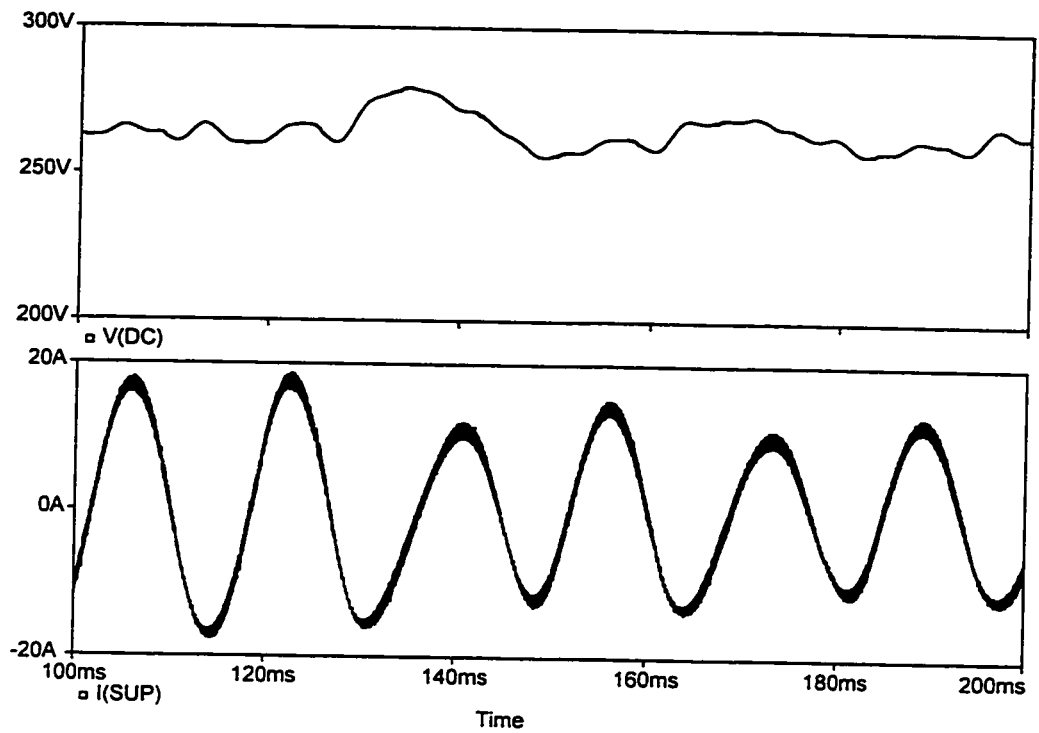
**Fig. 4.15** Dc bus behavior for a step change in reference.

The above curves show that increasing the capacitor value gives slower response. For the selected example, design values for the current loop and voltage loop are summarized in Table 4.1, simulation results showing dynamic performance of the active filter compensating a single phase load are shown in Fig. 4.16, and Fig. 4.17.

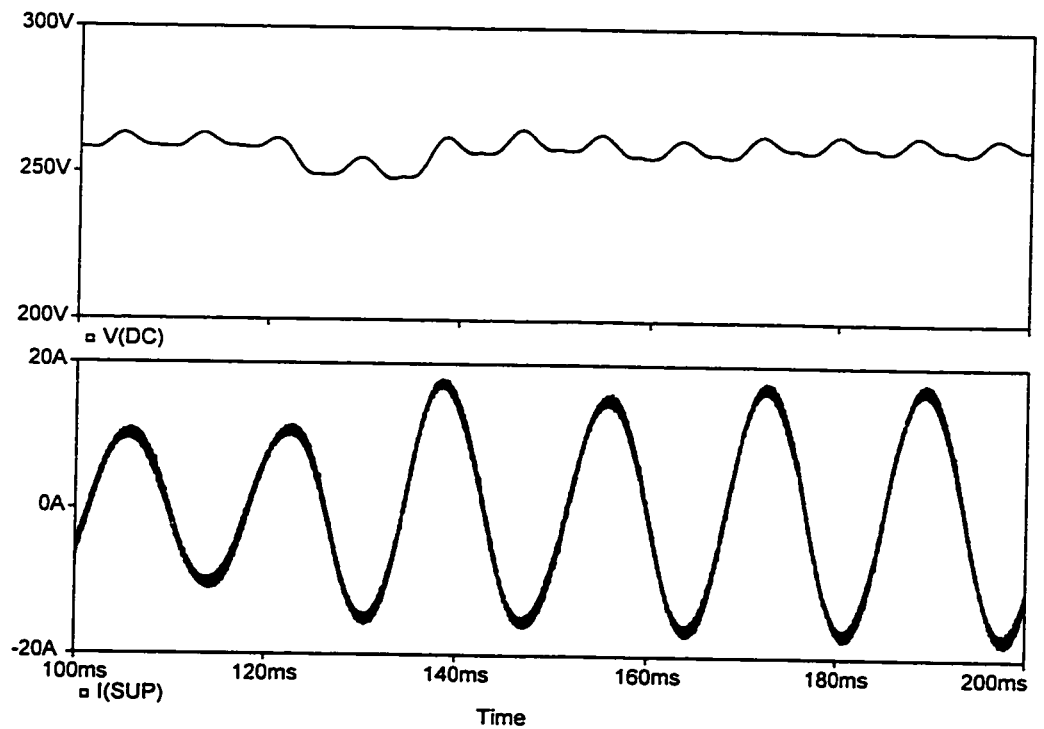
**Table 4.1 Power circuit and control system design values**

<b>Power Circuit</b>	
$f_{sw}$	10 kHz
$L_{af}$	3mH
$C$	900 $\mu$ F
$V_{dc}/2\sqrt{2}V_s$	1.56
<b>Current Loop</b>	
$k$	4
$\tau$	0.05 ms
<b>Voltage Loop</b>	
$k_v$	1
$\tau_v$	0.5 s
$\tau_f$	0.01s





**Fig. 4.16** Dynamic performance of the active filter for a sudden decrease in load a) dc bus voltage b) supply current.



**Fig. 4.17** Dynamic performance of the active filter for a sudden increase of load a) dc voltage b) supply current.

Under steady state condition, simulation results showed that the low frequency harmonics of the distorted current are canceled and the supply is a sinusoidal wave. When sudden changes occur at the load side, the dc bus reaches its preset value after the transient time has elapsed. If the load is decreased, the voltage across the capacitor is increased during the transient, and the worst case happens from no load to full transition. This overvoltage across the dc bus occurs as a consequence of the energy that has to be released by the capacitor during the transient. The opposite effect is observed during the transient if the load is increased from no load to full load.

#### **4.5 Conclusions**

The control aspects of the active filter based upon on-line current error extraction in the time domain is presented, and a description of control system is given. The active filter is presented by a simple model which is adequate enough for the purpose of designing the current and voltage controllers. A low pass filter is inserted in the voltage loop to make possible the single phase operation of the active filter. Simulation results given, justifies the validity of the control system and its designed parameters. Also the dynamic performance of the active filter under transient conditions are examined by simulation.

## **Chapter 5**

### **SIMULATION AND EXPERIMENTAL RESULTS**

#### **5.1 Introduction**

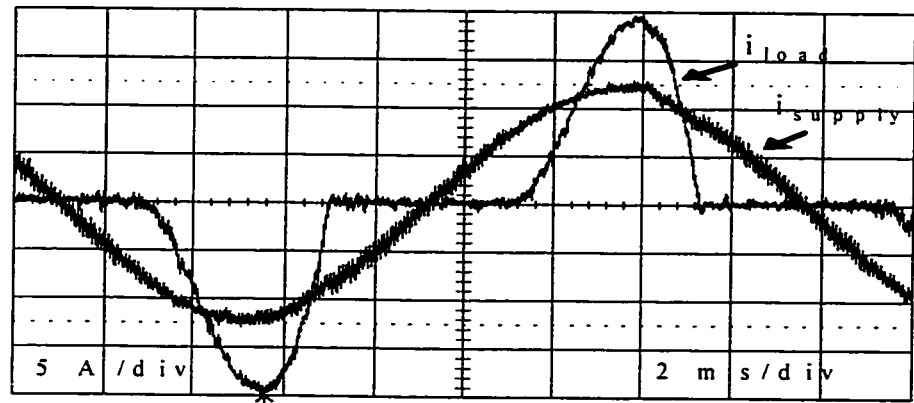
In previous chapters operating principles and design aspects of the active filter have been covered. This chapter presents experimental and simulation results validating the theoretical analysis. An industrial prototype fully assembled using PCBs was implemented in the laboratory. The following modes of operation were investigated: i) single phase load, ii) three-wire and four-wire connections, iii) unbalanced loads, and iv) unbalanced line voltages. It is experimentally demonstrated that with four active filter structure the neutral current is considerably reduced without the need of an additional active filter or a four leg converter. Also the reduction of the neutral current is achieved without affecting the operation of the active filter.

#### **5.2 Single Phase Operation-Experimental Results**

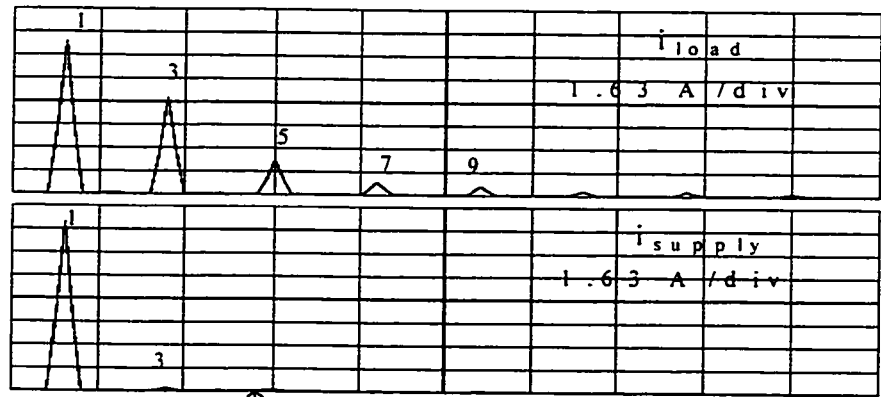
For single phase operation, the load data specifications are summarized in Table 5.1. The active filter design characteristics are shown in Table 5.4.

**Table 5.1 Single phase diode bridge data**

Power Circuit	Value
L-ac side	1 mH
C-dc side	3300 $\mu$ F
R-dc side	13.3 $\Omega$



a)



b)

**Fig. 5.1** Load and supply currents b) Spectrum of line and load currents.

Experimental results (Fig. 5.1) show that the low frequency components of the load current are nearly canceled (less than 1% residual) and the remaining dominant harmonics are at around the switching frequency with amplitudes limited to 5%.

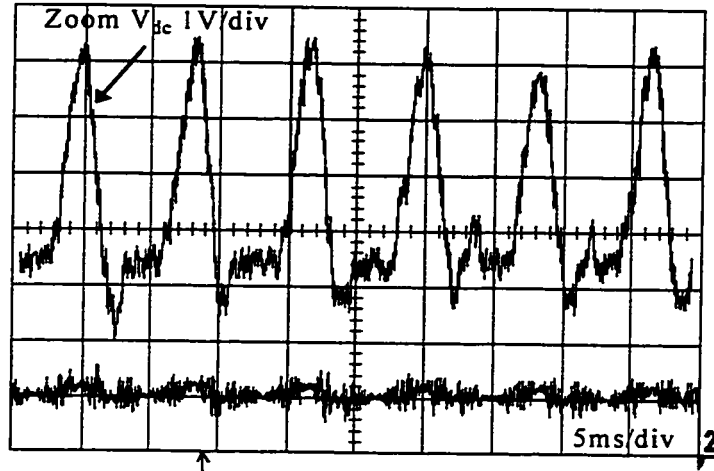


Fig. 5.2 Dc bus voltage

The dc bus voltage as shown in Fig. 5.2 is constant and is equal to its preset value, 265 V. The zoomed part of the voltage shows a ripple at twice the mains frequency, and the maximum fluctuation observed is 4.5 V, which is in good agreement with the design value, where a voltage regulation ratio of 2 % was imposed.

Table 5.2 summarizes different test results for single phase operation. The load line inductance is varied from 1mH to 5mH. The value of the active filter inductance,  $L_{af}$ , is kept constant to 3mH in all cases. The experiment showed that, the dc bus voltage could be decreased when the load reactor is increased and still achieve the same  $THD_i$  in the line current.

**Table 5.2 Active filter performance for different load conditions.**

		Load side		
$L_{load}$	(mH)	1	3	5
$di/dt$	(kA/s)	25	12	10
$I_{load,l}$	(A)	11.5	10.7	8.8
$THD_i$		59.4 %	45.5 %	32 %
		Active filter dc bus voltage		
$V_{dc}$	(V)	265	210	200
		Supply side		
$I_{s,h} @ f_{sw} / I_{load,l}$		4.7 %	4.2 %	4.5 %
$THD_i$		4.86 %	4.38 %	4.67 %

### **5.3 Unbalanced Load Operation**

Three single phase diode bridge rectifiers are connected between the line and the neutral to form an unbalanced load. Load data is presented in Table 5.3.

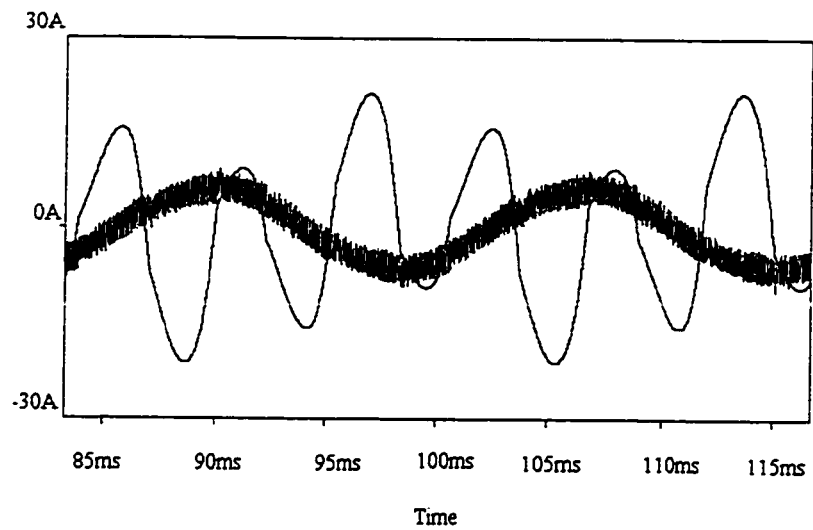
**Table 5.3 Three single phase diode bridges.**

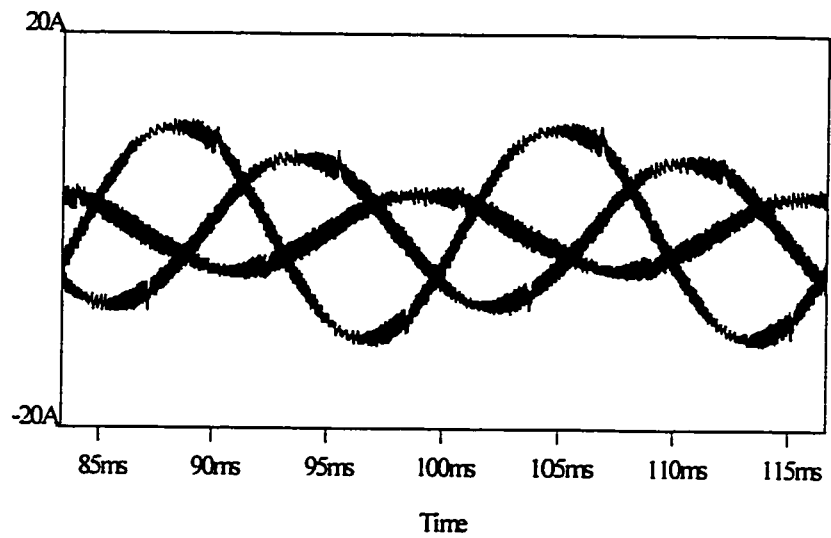
Power Circuit	Value
L-ac side	1 mH
C-dc side	3300 $\mu$ F
R-dc side	13.3 $\Omega$ , 20 $\Omega$ , 41 $\Omega$

**Table 5.4 Four wire active filter ( $f_{sw} = 10.3 \text{ kHz}$ )**

Power Circuit	Value
$L_{af}$	3 mH
$C_{af}$	900 $\mu\text{F}$
$V_s$	60 V
$V_{dc}$	260 V

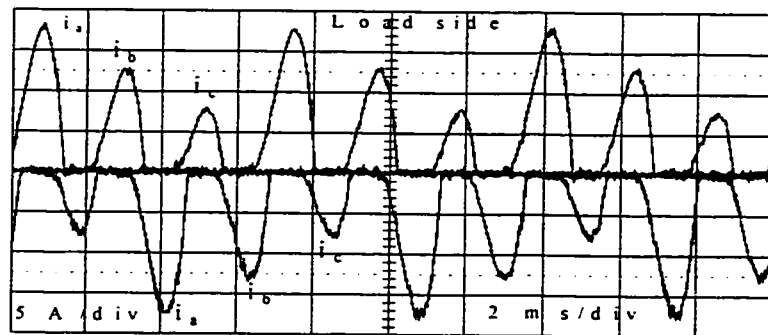
### 5.3.1 Simulation Results-Four Wire Active Filter.

**Fig. 5.3** Neutral current before and after compensation.

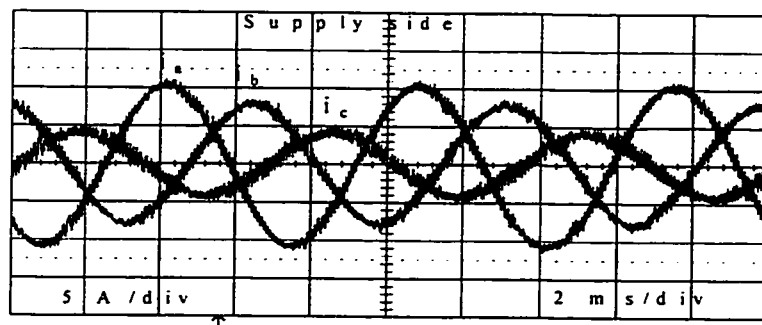


**Fig. 5.4** Supply currents after compensation.

### 5.3.2 Experimental Results-Four Wire Active Filter



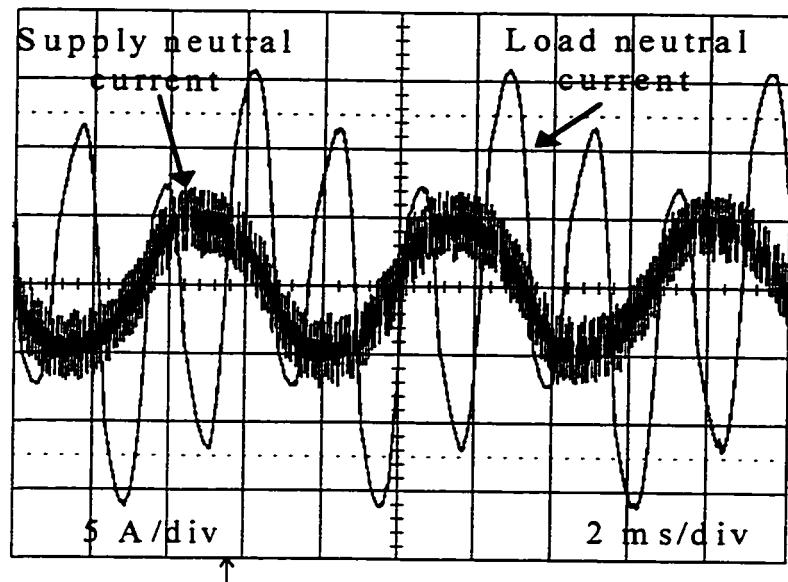
a)



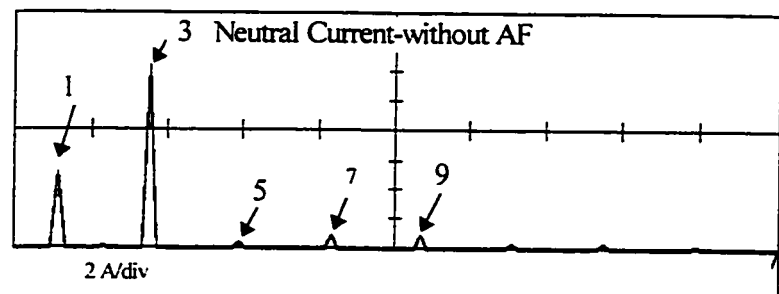
b)

**Fig. 5.5** a) Load currents b) supply currents.

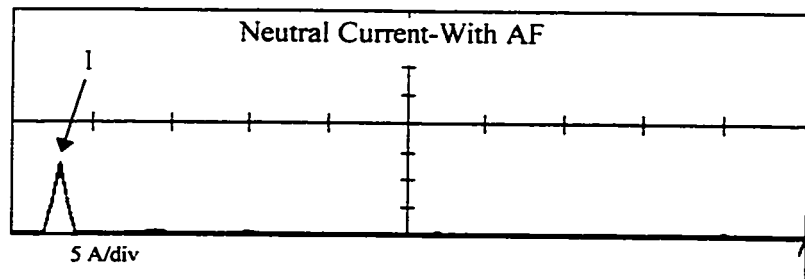




**Fig. 5.6** Neutral current with and without active filter.

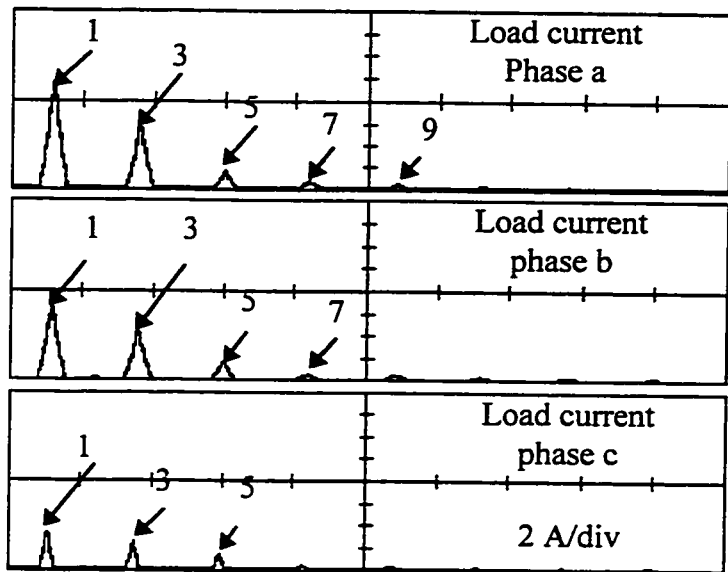


a)

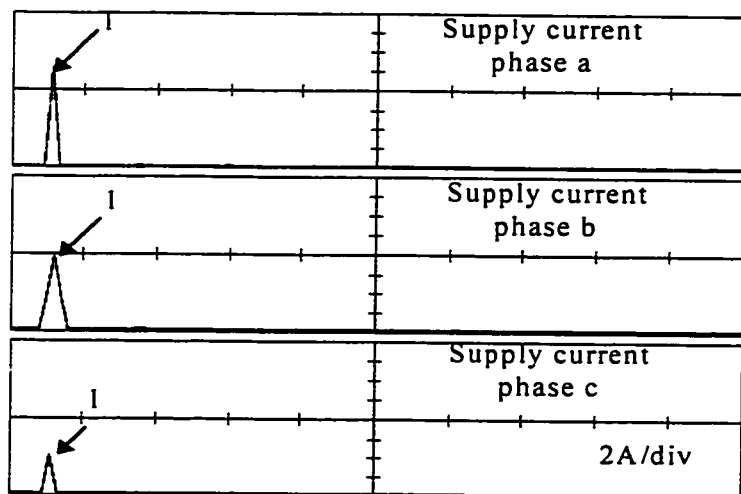


b)

**Fig. 5.7** Spectrum of the neutral current. a) load side b) supply side.



**Fig. 5.8** Spectrum of load currents.



**Fig. 5.9** Spectrum of supply side currents after compensation.

Experimental results show that (a) the active filter is able to operate under load unbalance, and (b) compensation of the line currents is accompanied with a reduction of neutral current, Fig. 5.6 and Fig. 5.7. Before compensation, the peak current in the neutral wire is 14 A (140 % of the peak line current). After compensation, the peak current has dropped to 5.36 A (50 % of the peak line current), thus a reduction of 60 % was achieved. The spectrum of the neutral wire contains 60 Hz and 10.3 kHz (switching frequency) components. The fundamental component exists because the currents are unbalanced. In all three lines, the residual currents are reduced to less than 1%. Also the rms current at the switching frequency in all three lines have the same value. As a result each line has a different THD, relative to the phase current and since the fundamental currents in lines *b* and *c* are less than the line *a*, they exhibit higher  $THD_i$  as shown in Table 5.5. The harmonic at the switching frequency can be reduced easily, using a small passive filter at the output of the converter.

**Table 5.5 Active filter performance under unbalanced operation**

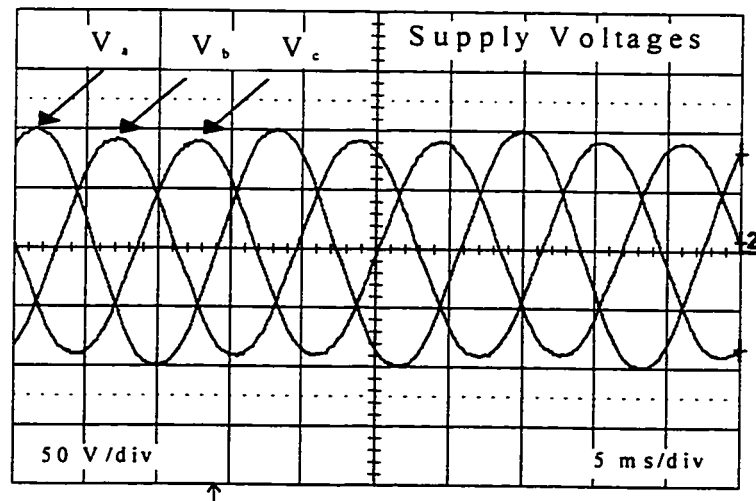
Line	1	2	3
Load side			
$I_{load,i}$ (A)	10.5	7.8	4.1
$THD_i$	62.6 %	70.5 %	84 %
Supply side			
$I_{s,h} @ f_{sw}/I_{load,i}$	5.2 %	7.2 %	14 %
$THD_i$	5.38 %	7.36 %	14.27 %

#### 5.4 Unbalanced Mains-Experimental Results.

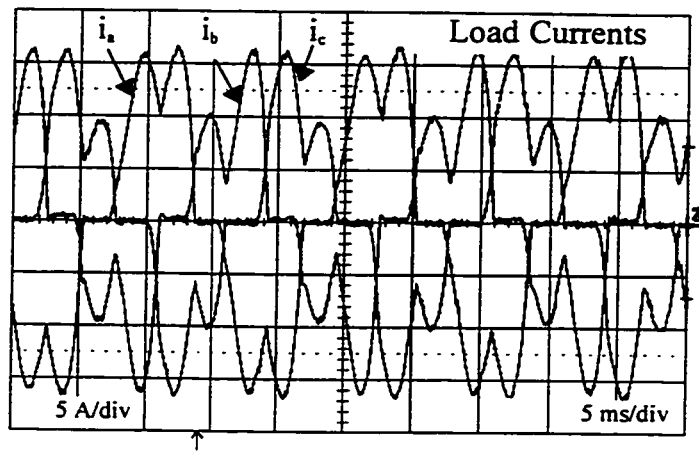
In this section the active filter is tested under unbalanced mains voltage ( $\pm 10\%$ ). The supply feeds a three phase diode bridge rectifier with capacitive output. Test conditions are summarized in Table 5.6 and the active filter design characteristics are given in Table 5.4.

**Table 5.6 Three single phase diode bridges**

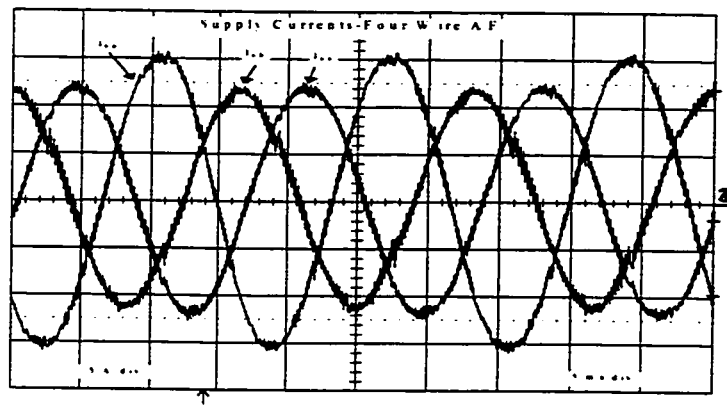
Power Circuit	Value
L-ac side	1 mH
C-dc side	3300 $\mu$ F
R-dc side	20 $\Omega$



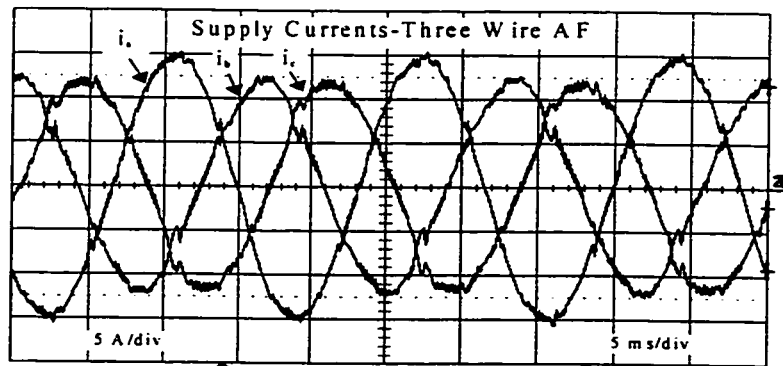
**Fig. 5.10** Unbalanced ac mains (+10%). Line to neutral voltages.



**Fig. 5.11** Load currents before compensation.

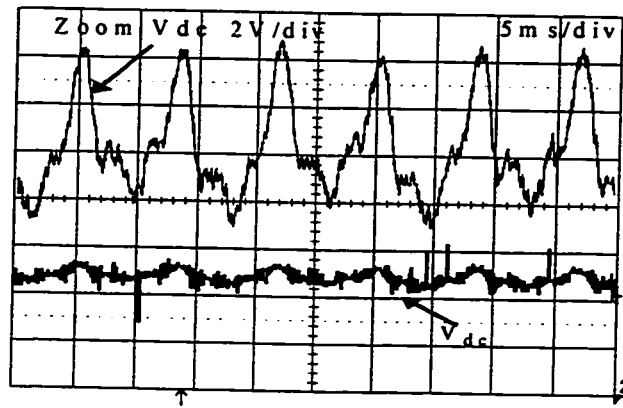


a)



b)

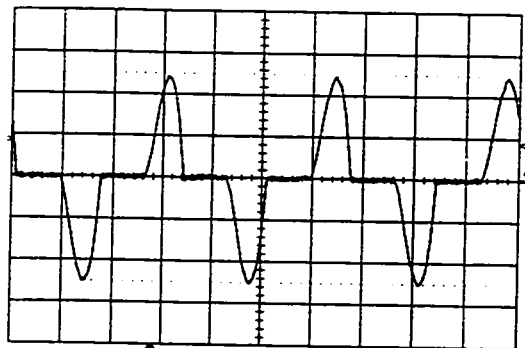
**Fig. 5.12** Supply currents for three phase diode rectifier load under unbalanced mains (+10%). a) Four wire active filter b) Three wire active filter.



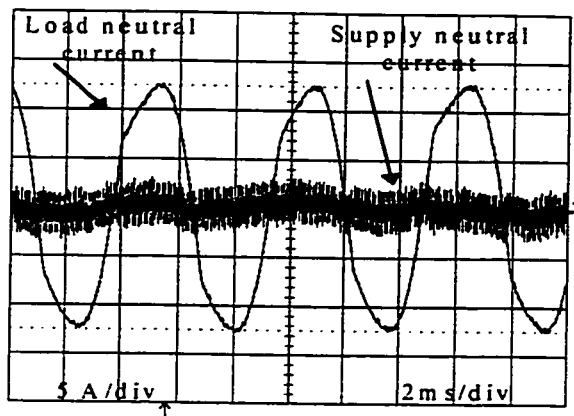
**Fig. 5.13** Dc bus voltage in four wire active filter.

#### **5.4 Balanced Single Phase Loads Operation-Experimental Investigation.**

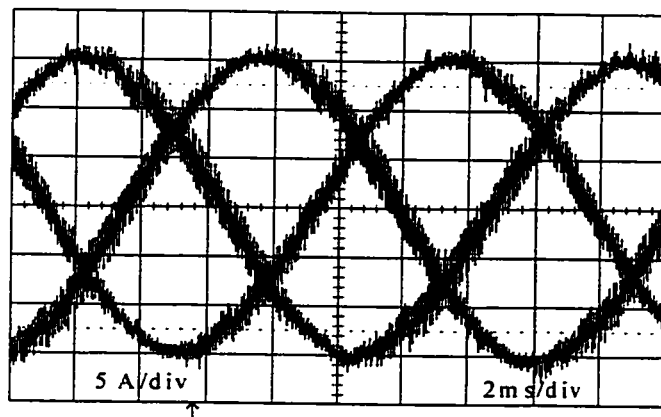
The four wire active filter is tested when compensating three balanced single phase diode rectifiers. Although the lines are balanced, the presence of single phase loads causes the sum of the three lines currents to flow in the neutral wire. Hence, the neutral current contains the sum of the triplen harmonics present in each line. Load and active filter data are summarized in Table 5.6 and Table 5.4, respectively. Also, the conventional active filter in a bridge configuration is tested under the same condition.



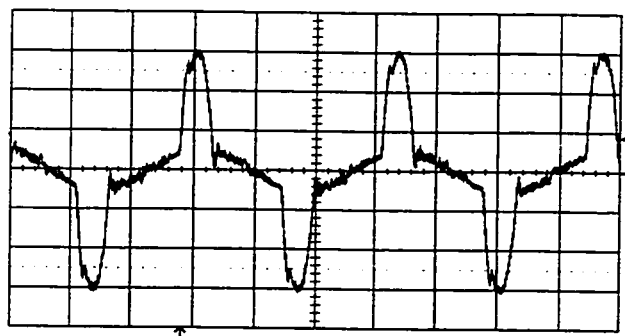
**Fig. 5.14** Load current.



**Fig. 5.15** Supply and load neutral currents with four wire active filter.



**Fig. 5.16** Supply currents after compensation with four wire active filter.



**Fig. 5.17** Supply current after compensation with three wire active filter.

Experimental results show that in the case of balanced single phase loads, the four active filter cancels the distorted current as well as eliminates the triplen harmonics from the neutral wire, and the only remaining harmonic is the component at the switching frequency. However, results with three wire active filter operated under the same conditions show that the line currents remains uncompensated.

### **5.5 Performance Comparisons.**

Experimental results show that in all modes of operation the proposed active filter was able to compensate effectively the harmonic component of the load. The performance of the four wire and three wire active filters are summarized in Table 5.7.

**Table 5.7 Performance of half bridge and three phase active filters.**

<b>NON-LINEAR LOAD</b>	<b>HALF-BRIDGE</b>	<b>CONVENTIONAL</b>
$1 \times 3\phi$	$THD_i < 5 \%$	$THD_i < 1 \%$
$3 \times 1\phi$ (balanced)	- $THD_i < 5\%$ -neutral current reduced	-triplen harmonics amplified -poor harmonic correction
$3 \times 1\phi$ (unbal.)	-line current harmonics eliminated -neutral current reduced	-line currents and neutral current remain unchanged
Unbal.mains	$THD_i < 5 \%$	$THD_i \approx 6 \%$



## **5.5 Conclusions**

This chapter has demonstrated the feasibility of a three phase active filter based on half-bridge topology. Experimental results show that the filter is able to reduce harmonics under various modes of operation. The high frequency harmonic currents generated by the inverter remains within the specified range of the design value. Moreover, the neutral current is reduced significantly under unbalanced conditions, and effectively compensated for balanced loads. Dc bus voltage fluctuation is effectively controlled by appropriate selection of the dc bus capacitor.

## Chapter 6

### SUMMARY AND CONCLUSIONS

#### **6.1 Summary**

The thesis has investigated harmonic compensation for typical low voltage distribution systems where power is fed through four wire systems using force commutated inverters, based on voltage type structures connected in parallel with the load. The following aspects have been covered :

(a) Harmonic compensation using a conventional three wire active filter and a four wire active filter, compensating single phase, balanced and unbalanced loads is investigated, as is the harmonic content of the neutral wire before and after compensation by means of both topologies. Moreover, the concept of half-bridge single phase active filter is extended to three half-bridge active filters in parallel with a common dc bus, and the operation of the proposed configuration was described.

(b) A thorough analysis of the power circuit, and a systematic design approach to the selection of power components is presented. Dc bus capacitor design and its effect on the compensation capability of the active filter. Rating issues of various components.

(c) A control scheme using the ramp comparison technique is implemented on a per phase basis for each leg of the inverter. The effect of the controller parameters on the residual currents are quantified. Simplified models for the current and voltage loops were included to design the controllers.

(d) Simulation of the presented configuration in various modes of operation to confirm theoretical results. Experimental investigation based on an industrial prototype to verify the concepts.

## **6.2 Conclusions**

Experimental investigation of the proposed configuration on an industrial prototype has confirmed the theoretical concepts and the feasibility of a shunt active filter on a laboratory scale. The unit has shown that the quality of supply current can be significantly improved under various load conditions. The following conclusions are reached regarding the problem of harmonic contamination in four wire distribution systems :

(a) Conventional three phase bridge type active filters are not able to reduce harmonics in the presence of single phase balanced and unbalanced non linear loads. Triplen harmonics are amplified, and harmonic compensation is poor.

(b) The three half-bridge topology can compensate harmonics generated by single phase non linear loads. Moreover, harmonic cancellation is achieved for three balanced single phase loads as well as unbalanced loads. In all three lines, the residual currents are

reduced to less than 1% and the remaining dominant harmonic is at the switching frequency. Its value is limited to 5 % under maximum load conditions .

(c) The neutral current is effectively canceled for operation with three single phase balanced loads, and substantially reduced if the load consists of three unbalanced single phase units. Typically, the rms harmonic current of the neutral wire is reduced by a factor of seven after compensation.

### **6.3 Suggestions for Future Work.**

As an extension of this study of three half-bridge active filter applied in four wire distribution supplies, the following topics are suggested :

(a) An investigation of the effect of adding a high frequency attenuation filter formed by a small L-C filter on the static and dynamic performance of the active filter.

(b) A study of the d-q-n reference frame control scheme applied to the three half-bridge active filter and performance comparison with the average current-mode control scheme in four wire environments.

(c) An analysis of the instantaneous reactive power control scheme applied to the three half-bridge active filter and performance comparison with the average current-mode control scheme in four wire environments.

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## ACTIVE AND REACTIVE POWERS IN ELECTRICAL SYSTEMS WITH GENERIC LOADS

### A.1 Sinusoidal voltage source and linear loads

#### a) Single phase case

The voltage source and load current are given by:

$$v_a(t) = V \cdot \sqrt{2} \cdot \sin(\omega t) \quad i_a(t) = I_s \cdot \sqrt{2} \cdot \sin(\omega t) \quad (\text{A.1})$$

Instantaneous power can be calculated by:

$$p_a(t) = v_a(t) \cdot i_a(t) = V \cdot I \cdot \cos \phi \cdot (1 - \cos 2\omega t) - V \cdot I \cdot \sin 2\omega t \quad (\text{A.2})$$

Average or active power is given as

$$P = V \cdot I \cdot \cos \phi \quad (\text{A.3})$$

Reactive power is defined as

$$Q = V \cdot I \cdot \sin \phi \quad (\text{A.4})$$

#### b) Three Phase Case

The system is balanced with phases a,b and c. Average or active power is given as

$$P = 3 \cdot V \cdot I \cdot \cos \phi \quad (\text{A.5})$$

Reactive power is given as :

$$Q = 3 \cdot V \cdot I \cdot \sin \phi \quad (\text{A.6})$$

## A.2 Sinusoidal voltage and non-Linear loads

In this section the voltage source is the same as in equation (A.1), but current contains harmonics at frequencies multiples of fundamental frequency.

$$i_a(t) = \sum_{h=1}^{\infty} I_h \cdot \sqrt{2} \cdot \sin(h \cdot \omega \cdot t - \phi_h) \quad (\text{A.7})$$

Instantaneous power

$$p_a(t) = V \cdot I_1 \cdot \cos \phi_1 (1 - \cos 2\omega t) - V \cdot I_1 \cdot \sin \phi_1 \cdot \sin 2\omega t \\ + \sum_{h=2}^{\infty} \sin(\omega \cdot t) \cdot \sin(h \cdot \omega \cdot t - \phi_j) \quad (\text{A.8})$$

Average or active power

$$P = V \cdot I_1 \cdot \cos \phi_1 \quad (\text{A.9})$$

Reactive power

$$Q = V \cdot I_1 \cdot \sin \phi_1 \quad (\text{A.10})$$

Current rms value

$$I = \sqrt{\sum_{h=1}^{\infty} I_h^2} = \sqrt{\frac{1}{T} \int_0^T i^2 \cdot dt} \quad (\text{A.11})$$

Apparent power is given as :

$$S = V \cdot I \quad (\text{A.12})$$

The above equation squared gives

$$S^2 = V^2 \cdot I^2 = V^2 \cdot (I_1^2 + I_2^2 + I_3^2 + \dots) \quad (\text{A.13})$$

Harmonic power is defined as

$$H = V \cdot \sqrt{I_2^2 + I_3^2 + \dots} = V \cdot I_1 \cdot THD_i \quad (\text{A.14})$$

Finally equation (A.13) can be written as

$$S^2 = P^2 + Q^2 + H^2 \quad (\text{A.15})$$

Displacement factor or fundamental power factor =  $\cos \phi_i$

$$\text{Distortion factor} = \frac{\sqrt{P^2 + Q^2}}{S} = \frac{I_1}{I} = \cos \gamma$$

$$\text{Power factor or total power factor} = \frac{P}{S} = \frac{I_1}{I} = \cos \phi_1 \cos \gamma = \cos \phi$$

For a three phase balanced system all quantities in equations (A.9), (A.10), (A.12), and (A.14) are multiplied by 3.

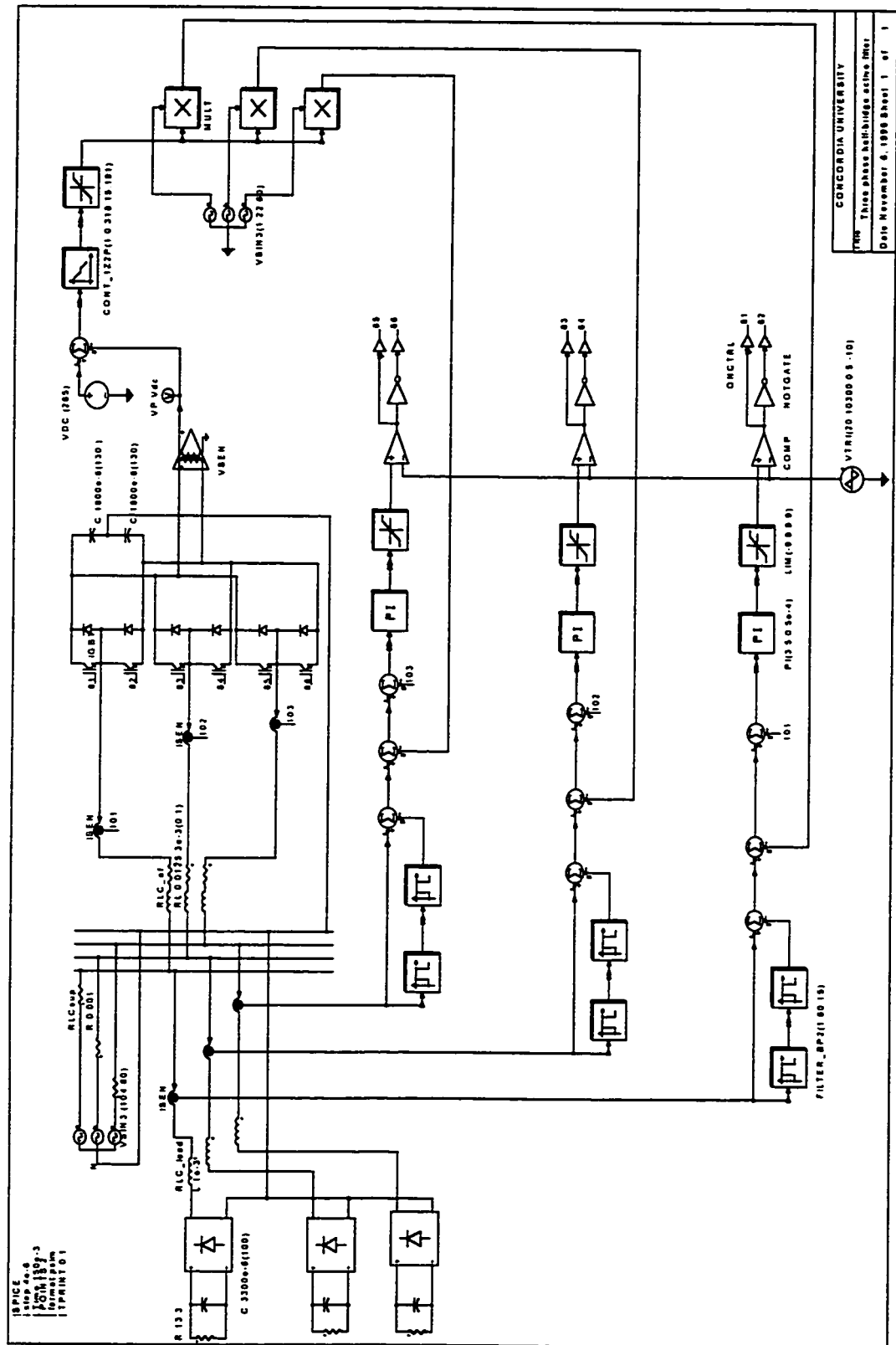
## **APPENDIX B**

### **SIMULATION AND MATHEMATICAL PACKAGES**

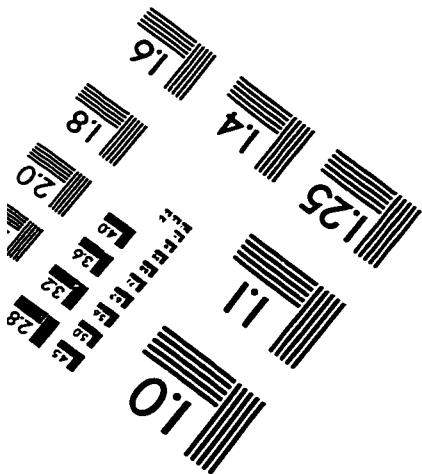
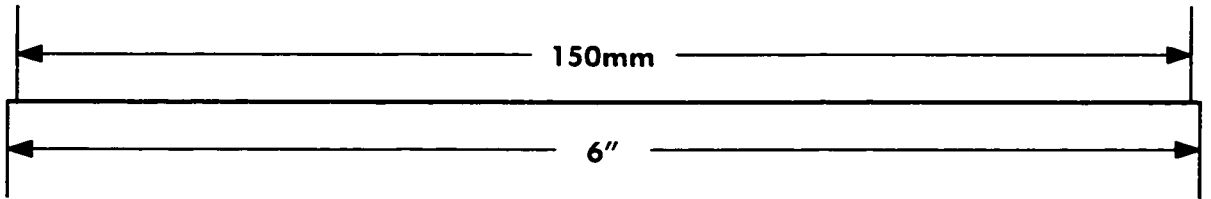
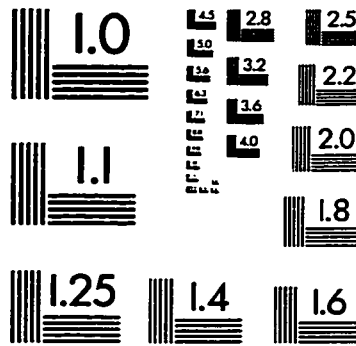
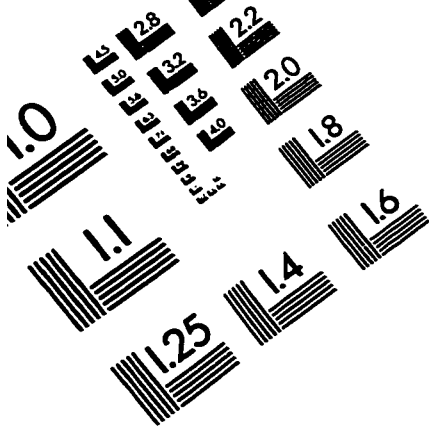
In this thesis, the PC based PSIM simulation package, developed by Dr. Hua Jin was used and PROBE for PSPICE as the graphic interface. To overcome the limitations due to number of points in PROBE, PSIM is forced to generate a fixed length data in an ASCII format, after which a custom program, developed by Mr. José Espinoza converts the ASCII file to a BINARY file formatted for PROBE. The complete simulation file is presented in Fig. B.1.

Two mathematical packages were used in this thesis. PC based Mathcad 5.0 plus by MathSoft Inc. and SUN based Matlab by The Mathworks Inc.





**Fig. B.1 Complete simulation file.**



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