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LA THÈSE A ÉTÉ
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DESIGN AND BUILDING
OF A DIGITALLY CONTROLLED
THYRISTOR CURRENT SOURCE

Mohammad Akhtar Jamil

A Dissertation

in

The Department

of

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ABSTRACT

DESIGN AND BUILDING OF A DIGITALLY CONTROLLED THYRISTOR CURRENT SOURCE

Mohammad Akhtar Jamil

A complete design and implementation of digital firing circuit with a digital current controller for a constant current source is described. The controller accepts an 8 bit binary number, representing the delay angle. The achieved resolution of the converter delay angle is 0.4 degrees.

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CHAPTER 1

INTRODUCTION

With the development of thyristor technology there has been a spectacular rise in converter application. The main factors contributed to this are efficiency, compactness, reliability and relatively high switching speeds at high power levels of thyristor converters.. One of the most widely used type of converter is a six-pulse thyristor bridge, Fig. (1.1). Due to its transient characteristics, this converter is often used in closed feedback loop configuration. One such configuration is a regulated current source which is the subject of this dissertation. The regulated current source consists of thyristor bridge with firing control circuit, d.c. link filter, current feedback loop and a current controller, Fig. (1.2).

Without any feedback loop the three phase full-wave converter rectifies three phase a.c. to unregulated d.c. voltage. The d.c. link filter is used to smooth the d.c. current and also acts as an energy reservoir by supplying large but short term current to the load. Current feedback loop and controller adjust the converter delay angle to produce the adequate d.c. voltage in order to meet a load current demand.

Existing analog systems for control of six pulse thyristor converters are well known and extensively used in the industry. The development of I.C. chips gives an alternative to analog systems and it was felt that a digitally controlled current source may offer some advantages over the designs currently used. Finally, the development of Power

Electronics Laboratory requires several current sources, all to be used as building blocks in various motor drives. Since these drives will be ultimately microprocessor controlled, a digital current source becomes a much easier block to interface.

The salient feature of this report is digital firing control which enhances:

a) Immunity against drift;

b) Accuracy of control; and

c) Compatibility with possible digital (microprocessor) controller of the total system.

Chapter 2 describes the application of a current source. Chapter 3 explains the operation, dynamic characteristics and pulse gating. Chapter 4 describes the design, implementation of current feedback loop and the digital current controller in regulated current source. In Chapter 5, experimental results are discussed.

CHAPTER 2

CURRENT SOURCE APPLICATIONS

2.1 Introduction

Various applications of a current source are discussed briefly. These applications are used to formulate the required steady state and transient characteristics of current sources used in industry. While a current source can be built around any power amplifier by implementing a current feedback loop, it is understood in this report that such an amplifier consists of a six-pulse thyristor bridge, Fig. (1.1). At the present, only thyristor based current source can supply sufficiently high power while offering the desirable transient characteristics. The bridge from Fig. (1.1) has the additional advantage of operating from an industrial 3-phase network.

2.2 DC Motor Drives

For long time d.c. motor drives were the only choice for variable speed and traction applications. Although the availability of thyristor inverters has led to the development of variable frequency supplied induction motor drives, the d.c. drive still remains as the most widely used one in variable speed applications. This means that the drive transient characteristics are of greatest concern. These characteristics are considerably improved by implementing as an inner current feedback loop in addition to a speed feedback loop, Fig. (2.1). The speed error then becomes the input reference for the motor current [1]. In this way, one controls directly the armature current and thus the motor output

torque, thereby eliminating the electrical time constant of the armature circuit. The current loop gives additional advantage of short circuit protection.

2.3 Induction Motor Drives

The speed of an induction motor can be regulated by varying the frequency of the stator voltages. In industrial drives, this is normally achieved by using thyristor inverters with adjustable frequency [2]. While there is a number of inverter schemes, the one consisting of a d.c. current source and an auto-sequentially commutation inverter is very often used in industry, Fig. (2.2). This scheme offers advantages of relatively simple inverter configuration, to be gradient operation and automatic protection against excessive short circuit currents. The current source described in this dissertation is directly applicable to such induction motor drive.

2.4 Synchronous Motor Drives

Due to their ability to provide reactive power and thus operate from phase commutated inverters, synchronous motor dirves are becoming an attractive alternative in variable speed, high power (1000 hp and more) applications [3] . In order to obtain desirable drive performance, the phase commutated inverter is supplied from a current source of the same type as the one described in this report.

2.5 Summary

Three most common industrial applications of a high power current source were briefly described in this chapter. The current

source described in this report is directly suitable to any of these applications and has been indeed designed by having them all in mind. Based on these applications, the following appear to be the desirable characteristics of a current source:

(1) it provides sufficiently wide bandwith for short circuit protection;

(2) it gives good transient performance in terms of stability, overshoot, etc; and

(3) it has the ability to regulate precisely the current, thus achieving zero steady state error.

CHAPTER 3

CONVERTER OPERATION, PULSE GATING AND CONVERTER CHARACTERISTIC

3.1 Introduction

The three phase fullwave thyristor bridge used in the current source is shown in Fig. (1.1). This is the most commonly used bridge configuration in industry [4], since it provides two quadrant operations (rectification, with both output voltage and current positive and inversion with output current positive and voltage negative).

For low power requirements of 1 or 2 KW, a single phase bridge is adequate, but for higher powers a three phase bridge is normally used. The six thyristor bridge configuration results in full wave rectification and elimination of the d.c. component from the source current.

3.2 Thyristor Bridge Operation

A complete description of three phase bridge is provided by Dewan [5]. For the present purpose, a brief description is given. The bridge operates when two thyristors are triggered at the same instant, thus connecting the load to appropriate a.c. lines. By controlling the triggering, one controls the converter output d.c. voltage. The voltage and current waveforms are illustrated in Fig. (3.1). The thyristor switches on when it is forward biased by the input a.c. supply and when a triggering pulse is applied to its gate terminal.

3.3 Pulse Gating

The three types of gating signal for thyristor bridge are illustrated in Fig. (3.2). They are: (a) pulse gating; (b) continuous gating; and (c) high frequency carrier gating (burst firing). The first type is not used in the present application. The reason is that it not only requires large amplitude of the pulse but also due to low frequency the size of the pulse transformer is sufficiently large. The second type (b) is not suitable because of the resulting large gate power dissipation and the required size of the pulse transformer for this application. Type (c) is prefered for the present application since it provides less gate power dissipation and due to high frequency (burst) the size of the pulse transformer is considerably reduced. These pulses normally have a frequency of the order of 30 KHz. The minimum pulse width is 5μsec. In our case it is about 10μsec. The burst lasts for 5.5 msec, thus consisting of 275 pulses.

The thyristor bridge has two modes of operation continuous and discontinuous conduction. In continuous conduction the load current is never zero. In the discontinuous conduction, there are periods during which the load current is zero. For any given set of load circuit parameters (R, L and V_c), it may be broadly said that when α is large, the load current is discontinuous, being made of a series of pulses, each lasting less than 60°. The range of α over which this mode of operation takes place depends on the values of the load parameters.

3.4 Converter Characteristic

3.4.1 Transfer Characteristic

The transfer characteristic of a converter under continuous load current and assuming zero interval impedance is given by

$$E_{do} = 1.35\, V_L \tag{3.1}$$

$$E_d = g(\alpha) = E_{do}\cos\alpha \tag{3.2}$$

where

α = phase delay angle

E_d = average no-load output voltage for a delay angle

E_{do} = average output voltage for $\alpha = 0^{\circ}$.

V_L = rms line to line voltage

When the bridge is used as a power amplifier in a control system, a linear transfer characteristic between a control voltage V_c and the output voltage E_d is desirable. This can be achieved by a bias shift technique [6] assuming equation 3.2 holds: a firing pulse is produced at the intersection between a properly phased and scaled cosine wave and the reference voltage V_c. The relationship between firing angle α, and control voltage V_c, i.e.,

the transfer function is

$$\alpha = f(V_c) = \cos^{-1}\frac{V_c}{V_m} \qquad (3.3)$$

substituting in (2.2), we obtain

$$E_d = \frac{E_{do}}{V_m} . V_c. \qquad (3.4)$$

This technique not only gives a linear transfer function to the converter, but also compensates for fluctuations in the main voltage. If the a.c. mains voltage drops, Fig. (3.3), the delay angle is advanced in rectifier operation, thus maintaining the output voltage constant. The converter gain is therefore, independent of mains fluctuation, so long as the rectifier limits ($\alpha = 0^o$-90^o) are not reached. The maximum output voltage, however, decreases.

Discontinuous Conduction:

The discussion, so far, has assumed that converter load is capable of maintaining continuous conduction throughout the whole range of delay angles. However, current flowing in the converter cannot reverse, and the output voltage contains a high amount of ripple, current, in most practical loads, may become discontinuous at some operating points.

Disadvantages:

Under discontinuous current condition, the output voltage, for a given angle, is larger than in continuous conduction [6]. Since

the relationship between control voltage and firing angle remains unchanged, the converter transfer characteristic ceases to be linear. This is illustrated in Fig. (3.4) for a passive load.

For example, in the case of a d.c. machine, which generates an emf, discontinuous conduction can occur for any delay angle, the amount of discontinuity depends mainly upon the load imposed on the machine. If the armature current is zero (ideal no-load operation), the motor emf rests on the peak of the converter output. Thus,

$$E_d = E_a = 2\,V_L = \frac{\pi}{3} E_{do} \quad 0° \leq \alpha \leq 30° \tag{3.5}$$

$$E_d = 2\,V_L \cos(\alpha - 30^o) \quad 30° \leq \alpha \leq 180°$$

$$= \frac{\pi}{3} E_{do} \cos\left(\cos^{-1} \frac{V_c}{V_{vm}} - 30^o\right)$$

where the symbols used have been defined previously. This no load curve is drawn in Fig. (3.5): it is the locus of the operating points at which discontinuous current just starts to flow. These curves also point out the sharp decrease in converter gain as the operating point moves into discontinuous conduction.

The regulation curves of the d.c. machine supplied by the converter are shown in Fig. (3.6). Regulation is very poor in the discontinuous region.

The dynamic performance of the converter system is also affected by discontinuous current, since the gain of the amplifier is reduced during a discontinuous conduction.

CHAPTER 4

DESIGN AND IMPLEMENTATION OF REGULATED CURRENT SOURCE

4.1 Introduction

This chapter describes the regulated current source, the general guide lines for design of controller and the advantages of employing a digital scheme. It also presents the digital controller together with the description of each functional block.

4.2 Regulated Current Source

The regulated current source, consisting of thyristor bridge, feedback loop, a current controller and a firing circuit is shown in Fig. (1.2). The thyristor bridge is described in Chapter 3. The feedback loop which comprises of current sensing element and an amplifier, is explained in later sections. The current controller designed is of integral type which means that the output of the controller varies in accordance with both magnitude and duration of the input.

The current source involves the following:

a) Measurement of the average input current (I_{av}).

b) Comparison of the I_{av} with the reference value I_{as} thus defining the current error:

$$I_{as} - I_{av} = I_E \text{ (Error)}$$

c) Application of the error signal to a phase shift circuit which reduces the error. The phase shift circuit consists of a current controller and firing circuit.

4.3 Guidelines for Controller Design

In order to achieve the above mentioned functions, the controller has to be designed to provide:

a) fast response of the output current

b) zero steady state current error

c) stability in the converter output

A controller which satisfies these requirements can be realized by analog or digital scheme. The analog technique is, however, more conventional and is well documented in past technical literature [1]. Therefore, it was decided to adopt the digital scheme in order to acquire first hand knowledge in the design.

The advantages of using a digital scheme are:

a) immunity against drift

b) accuracy of control

c) no tuning required

d) high reliability

The disadvantage is that a large number of components (i.e., I.C. chips) is needed to realize the controller.

It may be pointed out that the design of most of the functional blocks, which form the controller, is quite standard and straight forward, except for the error processor which requires numerical manipulation to realize a desired function. During the design, the following criterion was always kept in mind:

a) The logic circuitry should be simple

b) The circuit should provide greatest reliability

c) The controller should be realized by using low cost standard I.C. chips.

4.4 Overview of System Concept

The block diagram of the digitally regulated current source and feedback loop is shown in Fig. (4.1). The proposed system can be used either as a regulated voltage source in open loop mode or as a regulated current source in the close loop mode. The system does not require any circuit modification for selecting either one of the two modes. A simple switch is provided for mode selection which automatically connects the different functional blocks to achieve this feature. Due to this additional advantage, it is well suited for the Power Electronics Laboratory.

4.4.1 Open Loop Operation

In open loop operation, the converter behaves as a regulated voltage source, Fig. (4.1). An 8 bit binary word (0-255 in decimal corresponding to a delay angle of 0-116°) is fed through manual switches to the memory. At the same time a zero crossover pulse is fed to an 8 bit counter and a sequencer. The two outputs, one from the memory and the other from the counter, are fed to a magnitude comparator, which gives it an output when the magnitude of the two inputs is equal. Comparator output is fed to the sequencer which performs the steering process, i.e., it guides the firing pulse to the right thyristor. The sequencer gives a pulse of 5,4 msec; the phase shift in this pulse depends on the

delay angle. The sequencer also contains gating circuits which under a control signal (on/off switch), stop or allow the firing pulses (burst) to pass on to thyristor gates. The outgoing pulses, from the sequencer, are fed through a pptocoupler to the pulse amplifier.

The need for pulse amplification arises from the fact that since these are TTL (5V logic) pulses, they do not have sufficient power to drive the thyristor gate.

After pulse amplification, the pulses are fed through a pulse transformer, whose secondary winding is connected to the gate and cathode of the thyristor. The purpose of this pulse transformer is to provide electrical isolation between the power circuit and the controller.

The control range of the delay angle is $0\text{-}116^{o}$, corresponding to the memory content of 0-255 binary. The delay angle resolution is 0.4^{o}.

4.4.2 Close Loop Operation

The a.c. line current is sensed by using three current transducers , Fig. (4.1). The output is rectified to obtain a pulsating (360 Hz) d.c. voltage. This d.c. voltage is fed to an analog to digital converder (ADC1) to obtain an 8 bit binary word which is passed on to an error processor.

The reference signal is obtained from a potentiometer fed from +5V and - 5V corresponding to a delay angle of $0\text{-}116^{o}$. The output is converted in ADC2 into an 8 bit binary

word and is fed to the error processor.

In this block the difference in magnitude (error) between current feedback signal and the reference signal is computed by using arithmetic logic units (ALU's). The error is conditioned to obtain the absolute value. The absolute value is then added to or substracted from the memory content depending whether the error is negative or positive. In this way, after every 2.7 msec, a new word is stored in the memory. This word is then fed to the comparator. The other input to the comparator comes from the counter which initiates counting upon the arrival of the first zero crossover pulse. When the count becomes equal to the memory word, the comparator gives an output which triggers the sequencer which releases the firing pulse. The memory is updated at every 2.7 msec.

The sampling time of the error is 110μsec. The firing pulse is amplified and applied to the thyristor.

4.5 Description and Realization of Each Functional Block

4.5.1 Zero Crossing Detector

The function of this circuit is to detect the zero crossover voltage of the three phase input supply to the thyristor bridge. The circuit is realized by employing 6-optocoupler devices, and three resistors. They are connected in delta configuration and protected by fuses as shown in Fig. (4.2).

The salient features of this block are:

a) no tuning is required

b) the design is simple

c) the realization is inexpensive

d) the circuit has high reliability

In order to understand the circuit operation, consider a single phase supply connected to the optocouplers, as shown in Fig. (4.2a). Fig. (4.2b) shows an optocoupler device. The devide works in the following fashion:
When an a.c. voltage is applied to the input diode of the optocoupler, the diode conducts and, through the optical coupling, triggers the associated transistor, which goes immediately into saturation.

Therefore, the collector (point c), goes from the supply to the ground potential. Thus, the optocoupler acts as a switch giving a high or low voltage depending whether the diode is in the conducting or non-conducting state. The input and output voltage wave forms are shwon in Fig. (4.3). The other optocouplers connected in delta configuration conduct during the other half cycle, Fig. (4.3).

The two outputs are inverted and fed to an NOR gate with Schmitt trigger to obtain a TTL compatible signal. As shown in the wave form, the mid point of the pulse, coming from the NOR gate corresponds to the voltage zero crossover. The duration of this pulse is 1 msec. Since the actual zero crossover occurs at the midpoint of this pulse, i.e., after 500 μ sec from the leading edge.

In order to detect this point, a single shot multivibrator is used which is triggered by the leading edge of 1 msec pulse Fig. (4.3). The pulse width of the single shot is adjusted to 500 μ sec. Thus, the trailing edge of the output pulse corresponds to the actual zero crossover point, Fig. (4.3).

4.5.2 Current Transducer

For operation of a current loop, a current transducer that senses the d.c. value of the output current is required. This transducer has also to provide the isolation of the control from the power circuit. A Hall effect current probe, an optically isolated sheet or a current transformer can be used as a current transducer. An inexpensive current transducer was selected for this design, Fig. (4.4).

Anticipating the possibility of unsymmetrical input voltages, the current is measured in each of three phases. The voltage signals, obtained across the burden resistors of each current transformer are rectified by a three phase, full wave diode bridge. Since the current transformer along with the burden resistor acts as a current source which reduces the dead zone encountered due to the voltage drop across the diode. The bridge output voltage is then proportional to the d.c. output current of the main thyristor converter.

Note that the current measurement on the a.c. side provides automatic isolation of the control circuit.

The gain of this feedback loop is $\frac{\Delta Vi}{\Delta_{ia}}$ and is found experimentally to be 1.15, Fig. (5.10)

4.5.3 Current Signal Amplifier.

After rectification, the output of the current transformer is fed to the d.c. amplifier. The design of this amplifier is well documented [7] . The gain of the amplifier is adjusted to have the maximum range of the ADC converter for a maximum input signal of -5V to +5V, (i.e., 255), Fig. (4.5). The output is fed to an RC circuit to filter the ripple in the current feedback signal. Since the filter introduces the phase lag it is undesirable. But from stability point of view, it is necessary. The effect of the filter is shown in Chapter 5. A 100K ohm resistor is used to limit the current into the analog to digital converter. The zener diodes clamp the ADC input voltage to a safe value, Fig. (4.5).

4.5.4 Reference Signal

The reference signal is obtained by using a potentiometer connected to +5V and -5V. The output is fed to a standard buffer stage as shwon in Fig. (4.6). Zener diodes are used to limit the input voltage to 10V. The 100K ohm resistor serves to limit the current to the analog to digital converter.

4.5.5 Interface Unit

Since the proposed scheme is digital and accepts only an 8 bit binary word , there is a need for an interface which converts the analog (current and reference signals) into a digital (8 bit word) signal.

Thus, the interface unit consists of two analog to digital (A/D) converters (5357), for current feedback and current reference signals.

The A/D converter, Fig. (4.7) employs a successive approximation technique to give an 8 bit complementing binary work corresponding to the input voltage, (Appendix(I)).

The sampling rate of ADC is 110μ secs where 80 μ sec is the ADC conversion time and 475 KHz is the clock frequency. The ADC requires a clock frequency of 475 KHz for its operation. The precision of ADC is ± 1 LSB (least significant bit), corresponding to 39mV of the full scale input. The starting pulse is fed from a 9.2 KHz clock through a single shot multivibrator which reduces the pulse width so that it becomes acceptable to ADC, Fig. (4.7).

4.5.6 Error Processor

The error processor is the vital part of the feedback loop, performing two basic operations:

a) error computation (by substracting the current feedback signal from the input reference)

b) error correction (by adding or substracting the error to the memory)

The operation of this block can be better understood by considering Fig. (4.8). Let A and B be two 8 bit binary words fed to ALU 1, which give the difference of the two words along with a sign bit corresponding to A > B.

The output from ALU1 is conditioned to obtain an absolute error. This error becomes the input to ALU2, which adds it to or substracts it from the word in the memory which represents the last calculated firing angle. In this way, the value of the firing angle, residing in the memory is updated at each firing pulse. The ALU circuit performs 16 binary arithmetic operations on two 4 bit words. These are selected by four function select-lines (S_0, S_1, S_2, S_3), Fig (4.9), and include addition, substraction and straight transfer. For operation on two 8 bit words, two such units are used as shown in Fig. (4.9).

The question arises as to why an absolute error is necessary. Suppose that the reference word is greater than the current word. This difference has to be substracted from the memory word so that the firing angle may be reduced. However, in a case where the reference is less than the current, the difference has to be added to increase the firing angle.

Since the ALU can handle only 8 bit word and if two 8 bit words are added, the resultant will have a carry which cannot be handled by 8 bit ALU's. Therefore, in order to prevent such condition, a command signal is given which loads the memory with the number 255 thus preventing it from malfunctioning.

The error conditioning circuit is realized by 8 OR gates and 5 inverters, Fig. (4.10). When A > B, the outputs of the OR gates are passed on without inversion while for the other case it is inverted.

When the command word (A<B) is applied to function select lines (S_0, S_1, S_2, S_3) of ALU 2A and 2B it switches from adder to substracter, (Appendix (II)).

4.5.7 Multiplexer

The multiplexer performs two important functions:

a) Selection (i.e., it selects the open loop or close loop operation)

b) Loading the memory with the maximum firing angle in overload condition.

By using the multiplexer [8] open loop or close loop operation can easily be selected by a switch (S1A and S1B) as shown in Fig. (4.9). However, in close loop operation, all the 8 manual switches are open, thus feeding the multiplexer with 255. When the load current demand exceed the maximum reference value (i.e., 255) from ALU1B and ALU2B is applied to the multiplexer select pin which immediately selects the open loop condition of 255, thus loading the memory with the maximum firing angle. When the condition stabilizes, the multiplexer again switches back to normal close loop operation as explained earlier.

The multiplexer output is passed through "zero limiting" circuit before feeding it to the memory. The purpose of this circuit is to prevent zero memory load. The reason being that zero input blocks the memory and the controller fails to perform the normal operation.

4.5.8 Comparator and Counter

The basic function of the digital comparator [9] is to compare the magnitudes of the two input words and to give an output when they are equal, Fig. (4.11).

The two 8 bit binary words, one from the memory and the other from the counter, are fed to the comparator. A synchronous counter, which starts counting from 0-255 (in binary) on receiving the first zero crossover pulse, is used. When the input from the count becomes equal to the other input from the memory, the comparator gives an output which resets the counter, fires one thyristor through the sequencer and loads the new value of the delay angle into the memory.

4 Comparators (7485) along with four J-K flip flops are used to achieve this function. Fig. (4.11) shows the complete circuit diagram. Each counter can handle 4 bits. For an 8 bit word, two parallel counters are needed. Another two counters have to be used if the delay angle exceeds 60^{o}. The reason is as follows:
The counting starts at each zero crossover which occurs every 60^{o}. When the delay angle is less than 60^{o}, the counter pair is cleared before the next crossover occurs. However, when the delay angle is more than 60^{o}, the next crossover starts a new counter pair, while the first pair has to keep going. Thus, when the delay angle is more than 60^{o}, the condition of all the four counters is very important in distinguishing which thyristor is to be fired next. (The sequencer is always looking at the counter conditions in selecting the right thyristor for firing).

4.5.9 Sequencer

This circuit basically performs a steering process, i.e., it guides the firing pulse to the correct thyristor.

The steering process is realized by using one counter (74193) which counts from 0-5 in binary numbers, a BCD to decimal converter (7442) and two single shot multivibrators. The circuit diagram is shown in Fig. (4.12). When the counter (74193) received the pulse $\bar{G}$, Fig. (4.12) from the comparator circuit, it triggers and releases a pulse which is fed to BCD to decimal counter (7442) to obtain the firing pulse. The duration of this pulse is 11.1 msec (corresponds to 116^{o}). When the delay angle is changed, this pulse is shifted corresponding to the delay angle but the duration of the pulse remains constant.

Single shot multivibrators are used, Fig. (4.12) for loading and synchronizing the counter (74193). The output of the sequencer is gated with on/off switch and then with a clock of 47.5 KHz. The clock frequency of 47.5 KHz is the carrier frequency (for burst) of the firing pulse. The circuit employs standard TTL logic gates [9] as shown in Fig. (4.14). The firing sequence is shown in Fig. (4.13).

4.5.10 Opto Coupler

Six opto couplers are used to isolate the pulse amplifier from the controller, Fig. (4.1). The reason is that the supply voltage required for pulse amplier is 15 volts where as the controller is supplied by 5V and 12 volts supplies with common ground. Application

of opto couplers also reduces the noise propagation problem.

4.5.11 Master Clock

For any digital system to operate in synchronizm, various clock frequencies are required. Therefore, a fundamental frequency generator and a frequency dividing network is called for to meet this requirement.

A crystal oscillator of 4.75 MHz is employed to generate the fundamental frequency. A frequency dividing network performs a division of 2 and 5 to obtain the various clock frequencies for the digital circuit. Fig. (4.15), (4.16) show the circuit diagram

4.5.12 Pulse Amplifier (Gate Amplifier)

The need for power amplification arises from the fact that since the output of the firing circuit is TTL (5V logic) pulses, they do not have sufficient power to drive the thyristor gate. Therefore, pulse amplification is very important.

The circuit shown in Fig. (4.17) uses a direct amplification to achieve gate drive [10]. The problem with transistor circuitry for high drive is the change in collector and the gate current required and the transfer problem of supplying sufficient volt second capability in a core to carry this signal.

This problem is solved in this circuit by driving the transformer as a current transformer and changing collector and gate drive by various primary collector impedances. In this fashion, the transistor base drive is kept constant and the R-C circuit generates the

sharp leading edge. Then, when the capacitor is fully charged, the 120 ohm resistor takes over to supply the needed sustaining current. The output of the pulse amplifier is applied to the thyristor gate.

Conclusion

The experimental evaluation of the current source prototype described in this section and actually built in the lab showed good results. These results are presented and discussed in the next chapter.

CHAPTER 5

REGULATED CURRENT SOURCE

PERFORMANCE AND EXPERIMENTAL RESULTS

5.1 Introduction

The performance of the regulated current source, calculated experimentally, is documented in this chapter. The experiments were performed for open loop steady state and close loop transient response of the current source with passive load (R and R-L). The effect of load on the dynamic behaviour of the current source is also presented.

The results obtained from these experiments showed that the steady state and dynamic behaviour were satisfactory.

5.2 Steady State Response

5.2.1 Transfer Characteristics

In the open loop operation, the converter transfer function between d.c. output voltage and the delay angle are plotted in Fig. (5.1). The curve follows a cosine law as mentioned in Chapter 2. It may be seen from Fig. (5.1) that for large values of the output voltage for inductive load is reduced. The maximum range of delay angle is 0°-116° (or 0-255 in binary) which gives output voltage range of 274V. to 5V d.c. for 208 volts a.c. input voltage.

5.2.2 Regulation Characteristics

The output voltage plotted as a function of output current I_d for two values of α (0^o and 60^o) is given in Fig. (5.2). For continuous conduction and with zero output impedance of the a.c. voltage source, the slope of these curves gives the thevenin equivalent resistor of the thyristor bridge. Both experiments showed that the equivalent resistance is $R_{th} = 0.83$.

5.3 Dynamic Response

5.3.1 Square Wave Response

The experimental setup used to evaluate the source closed loop performance in shown in Fig. (5.3). A square wave current input reference (6 Hz) was used. The current signal was measured at point x, Fig. (5.3). The reason for this was that voltage levels are conveniently small while the waveforms are the exact duplicate of the output current. A passive RL load (250 ohm and 200 mH), with the time constant of 0.8 msec was used.

The purpose of this test was to evaluate the speed by which the controller will respond to a sudden change in the load current demand. In order to respond to this demand the controller has to change the delay angle in minimum period of time. For this particular amplitude of the input reference square wave, the delay angle was changed from 35.3^o to 71.5^o which represents a

large variation in the load current. The output voltage changes from 223.62V to 86.94V in order to maintain the load current constant. The time taken in this transition is 8 msec, Fig. (5.4). The sampling period is 2.7 msec, therefore, in three sampling periods, this transition is completed.

It may be mentioned that even for such a large variation in the load current, the controller response was relatively fast. In Fig. (5.4), the time constant of the filter in the feedback loop was set to zero. This means that there is no phase lag introduced by the feedback loop. The rise time is 8 msec and the output faithfully follows the square wave input, Fig. (5.4).

When the time constant of the filter feedback loop is increased to 6.2 msec, the output, Fig. (5.5) showed an overshoot and an increase in the rise time. Since the filter time constant introduces a phase lag which means that the rise time will obviously be slow and the overshoot signifies that the system is underdamped. When the maximum filter time constant was set, the response was not only poor but the system started to oscillate, Fig. (5.6).

5.3.2 Frequency Response

A sinosoidal signal of 10 Hz, 50 Hz, and 100 Hz respectively, was applied to the system as reference signals. The response given in Fig. (5.7) and (5.8). With an increase in the frequency of the reference signal, the phase difference between the input and output increases, Fig. (5.7) and (5.8).

For 100 Hz signal, it was difficult to obtain clear waveform, because the sampling rate was 2.7 msec while the input signal time period was 10 msec, giving 4 samples per period. The resulting wave form is shown in Fig. (5.9) which is not very clear.

5.3.3 Summary

The results obtained from these experiments showed that filter time constant in the feed back loop has marked effect on the system performance. The band width of the system was found to be 100 Hz with a purely resistive load.

With RL load the band width is decreased. The band width also depends upon the load parameter.

CHAPTER 6

CONCLUSION AND RECOMMENDATION

6.1 - Conclusion

The regulated current source described in this report is suitable for d.c. motor dirve, current source inverter induction motor drive or a variable speed synchronous motor drive. All desirable characteristics of a current source such as short circuit protection, good transient performance in terms of stability and ability to accurately regulate the current have been incorporated in this prototype. An additional advantage of this design is that the source can also be used as a regulated voltage source (open loop operation) without any additional hardward modification.

The salient features of this design are:

- digital firing and digital current control which gives immunity against drift, accuracy of control and compatibility with possible microprocessor drive control.
- an economical and reliable zero crossing circuit, designed by employing the optocoupler devices.
- the burst firing technique which gives low gate power dissipation and decreased size of the pulse transformer.
- an integral controller with a fast response and zero steady state error.

It has already been explained that the dynamic performance of the current source greatly depends on the load time constants. Since this source is intended for a multitude of differend loads, its dynamic

performance was evaluated experimentally for a simple R-L passive circuit. The results were satisfactory.

6.2 Recommendation

In the future, the source can be further improved by implementing the arc cosine function for linearizing the controller transfer function and PI (proportional-integral) controller.

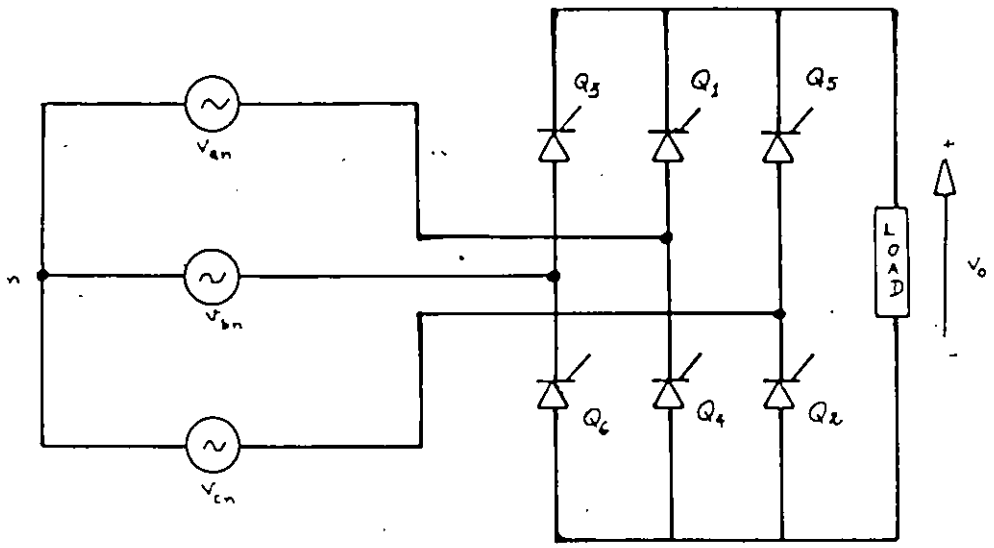


FIG. 1.1 SIX PULSE THYRISTOR BRIDGE

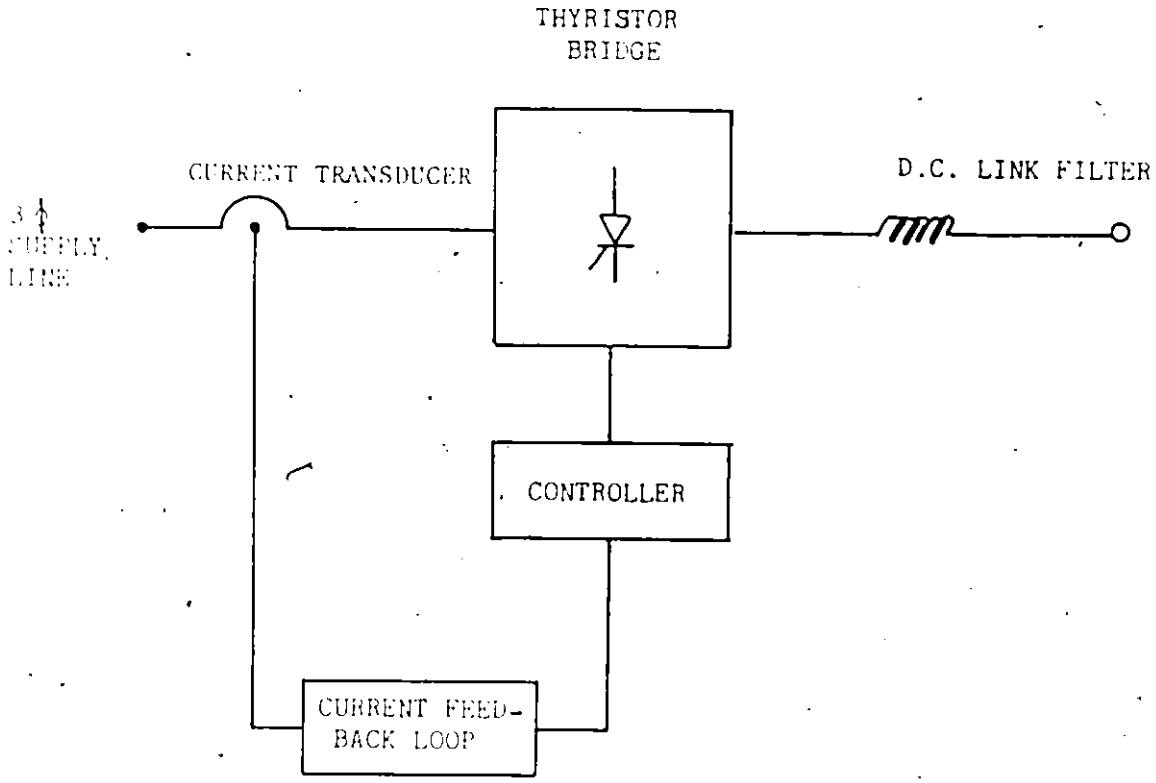
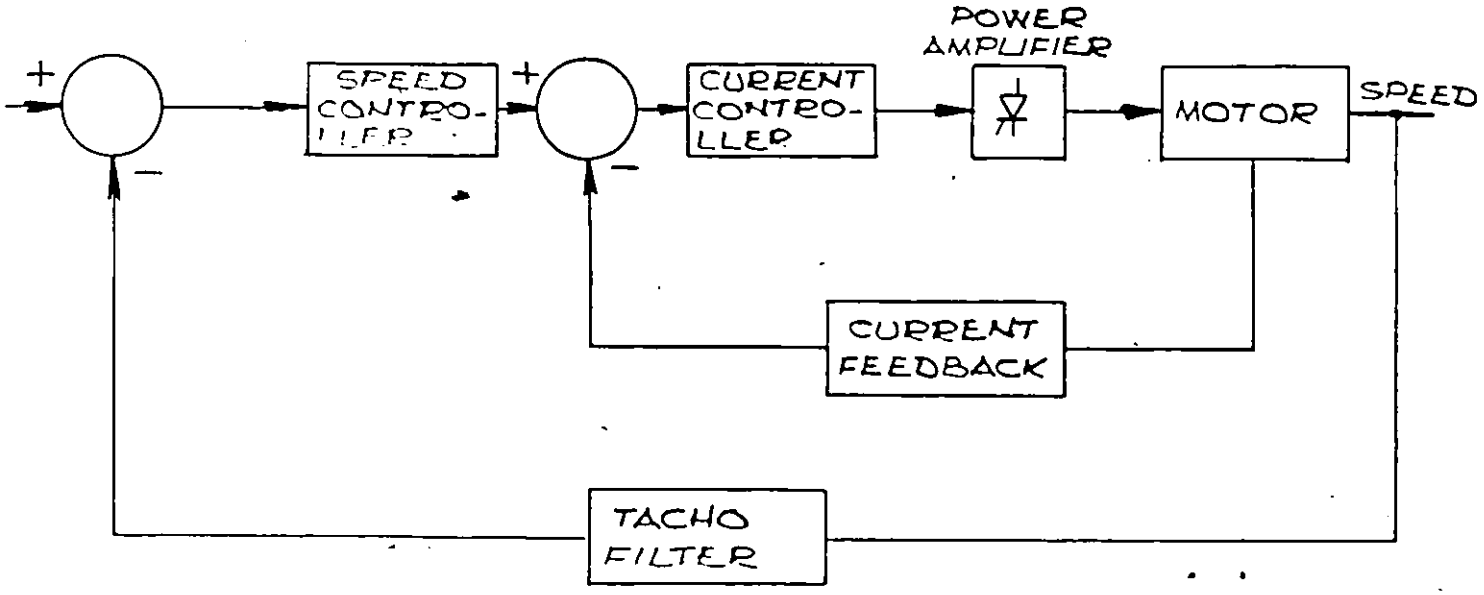


FIG. 1.2 REGULATED CURRENT SOURCE



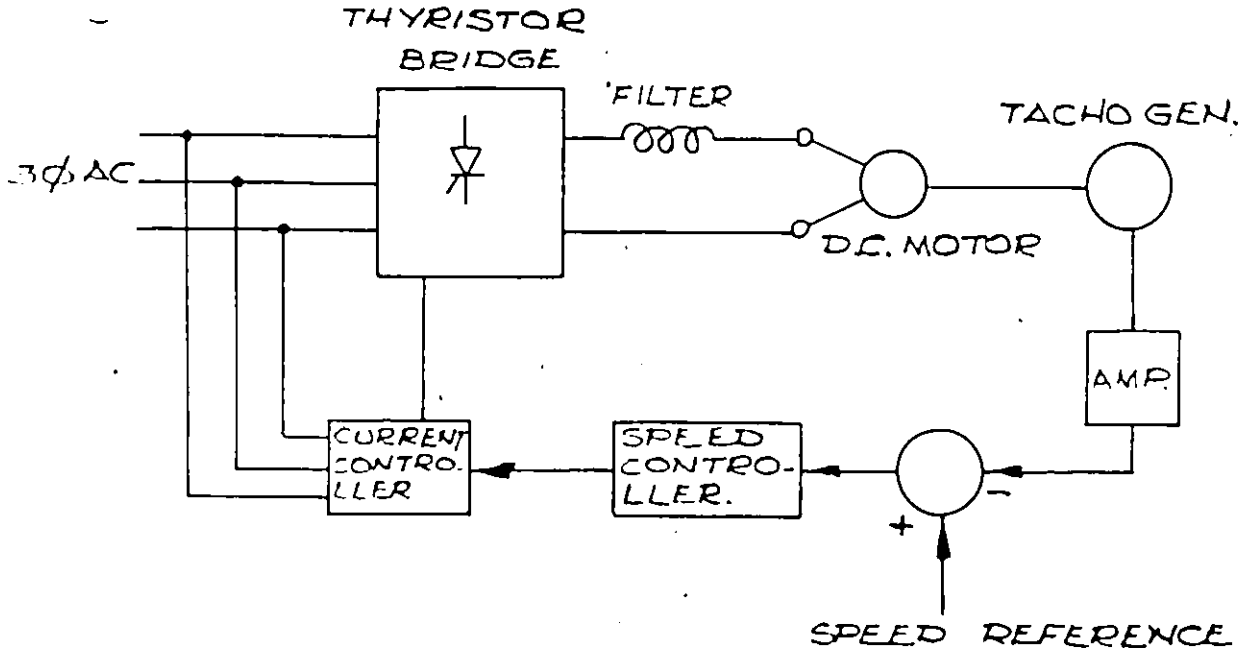
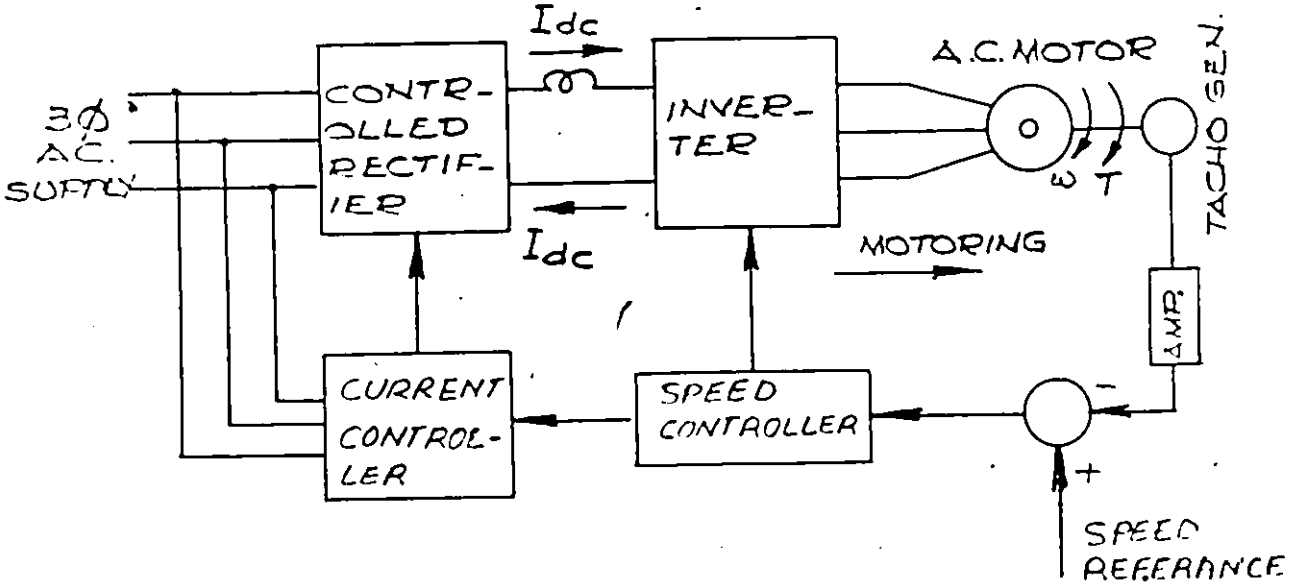


FIG. 2.1 DC MOTOR DRIVE



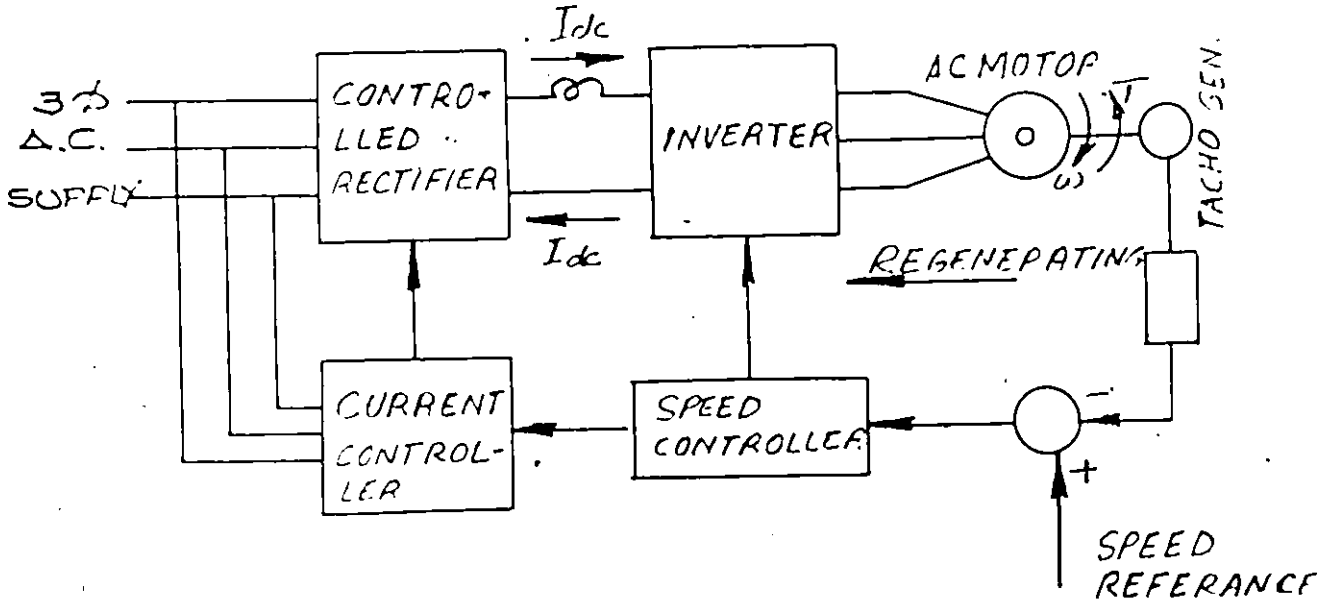


FIG. 2.2 AC MOTOR DRIVE

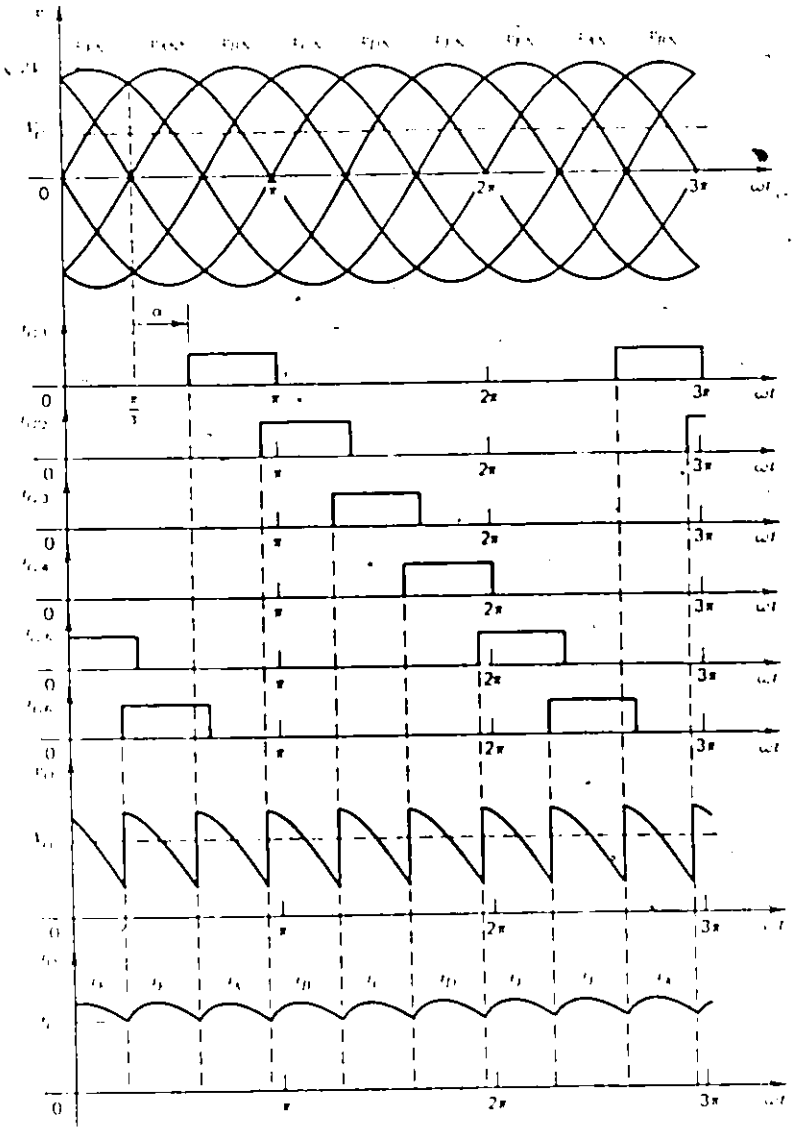


FIG. 3.1 TIME VARIATIONS OF VOLTAGES AND CURRENTS OF CONVERTER 5

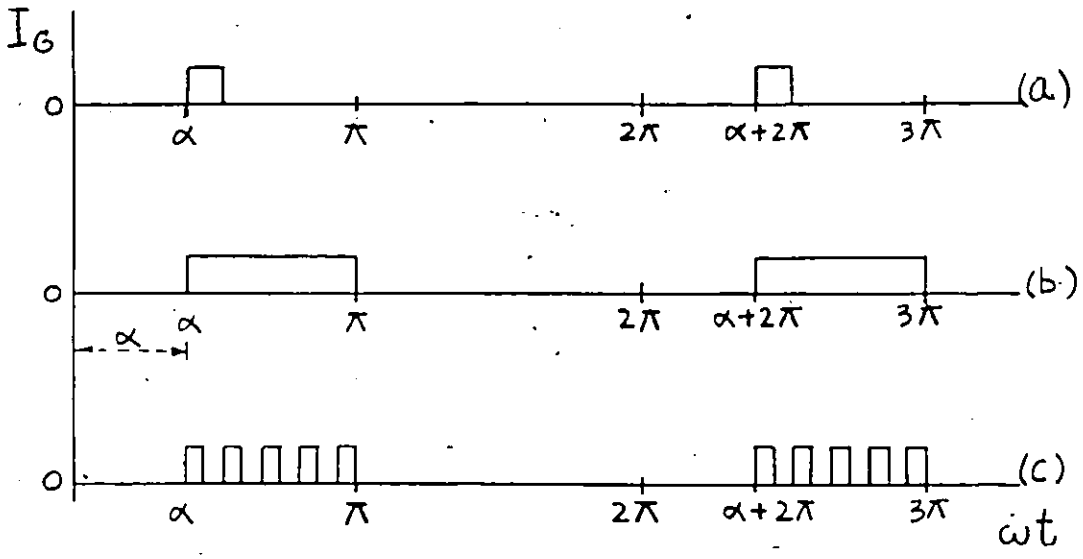
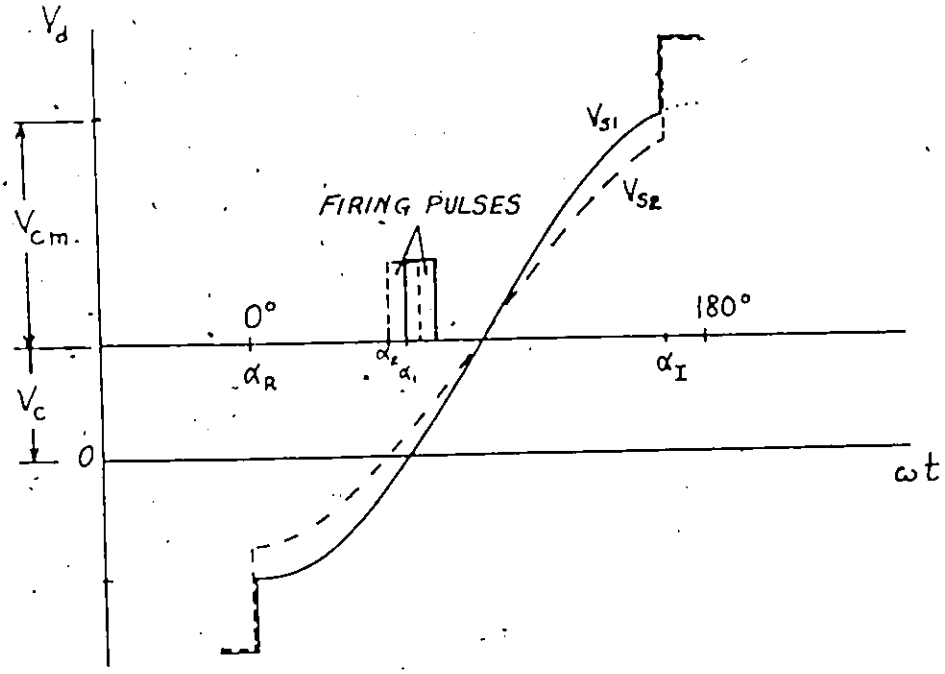


FIG. 3.2 TYPES OF GATING SIGNAL



V_c : Control Voltage, Regulated, Maximum V_{cm}

V_s : Sinusoidal Control Voltage, Derived from Mains

α : Delay Angle

α_R : Rectifier Limit

α_I : Inverter Limit

ω : Line Frequency

t : Time

V_d : Input to Zero Crossing Detector

FIG. 3.3 BIAS SHIFT TECHNIQUE AND COMPENSATION FOR MAINS FLUCTUATIONS

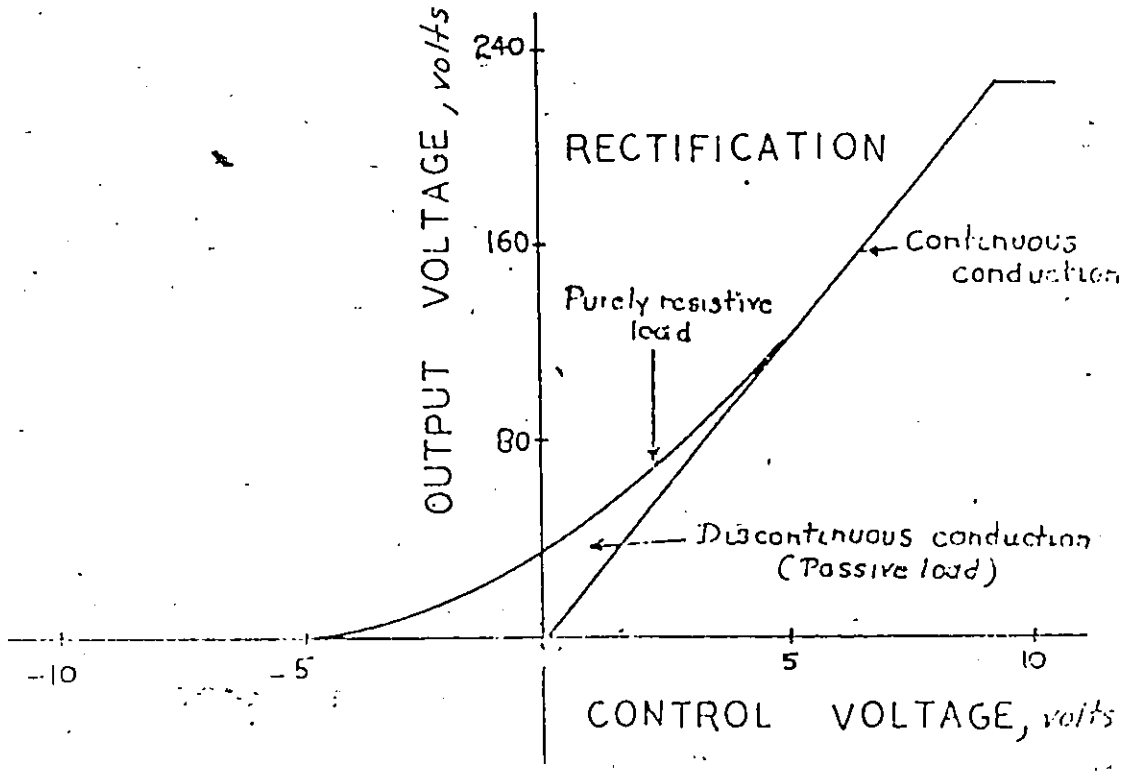


FIG. 3.4 EFFECT OF DISCONTINUOUS CONDUCTION ON CONVERTER CHARACTERISTICS

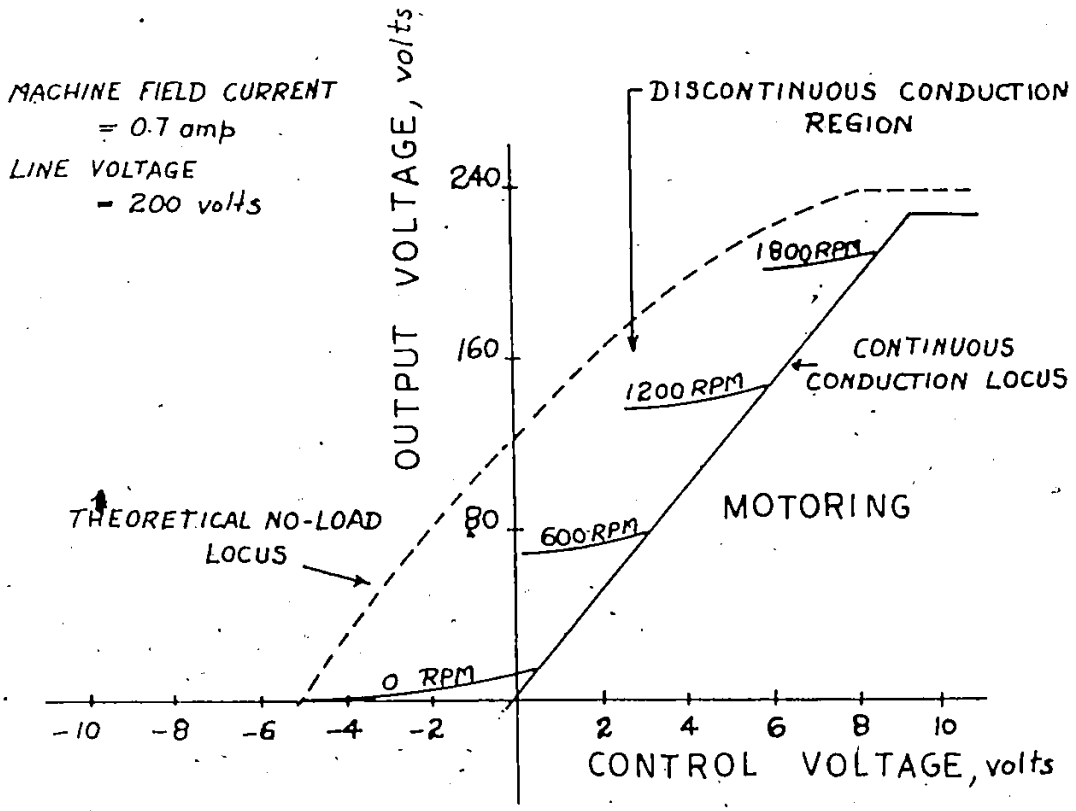


FIG. 3.5 CONVERTER VOLTAGE CHARACTERISTICS WITH D.C. MACHINE LOAD

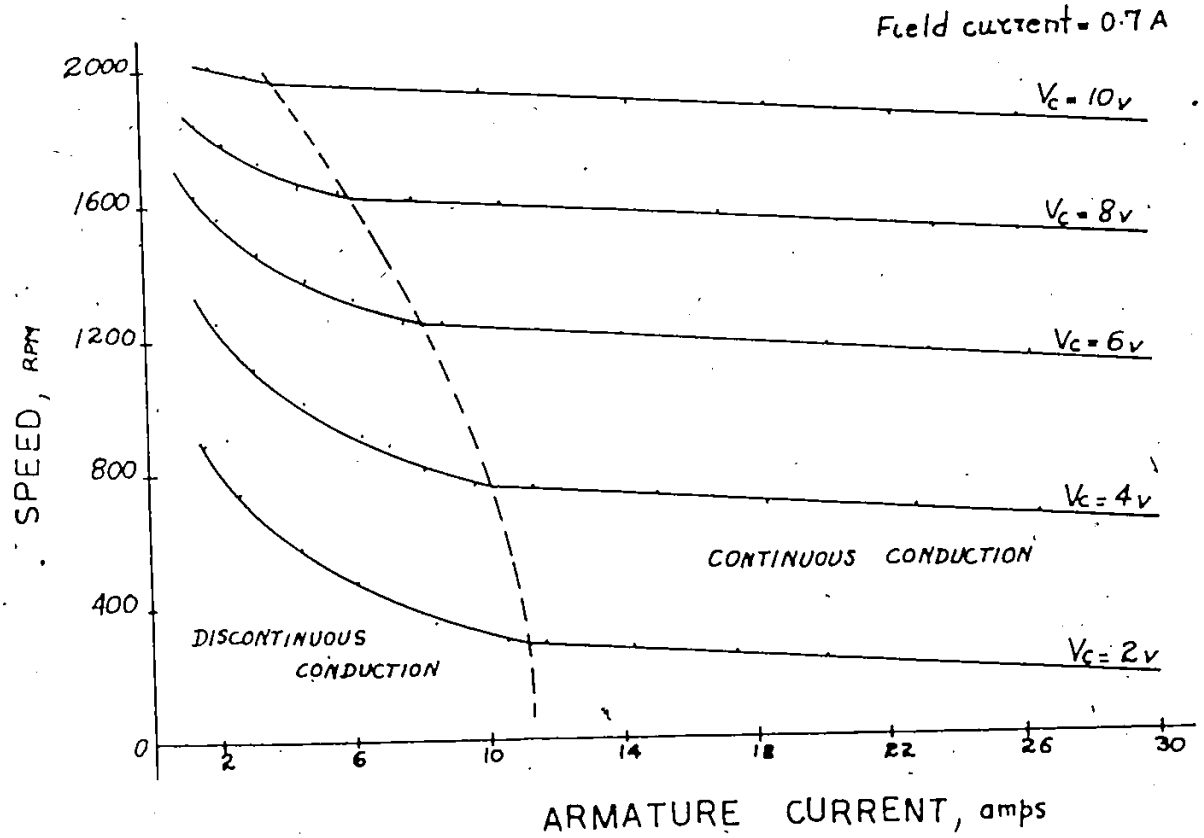


FIG. 3.6 REGULATION CURVES OF THE CONVERTER FED D.C. MACHINE 6

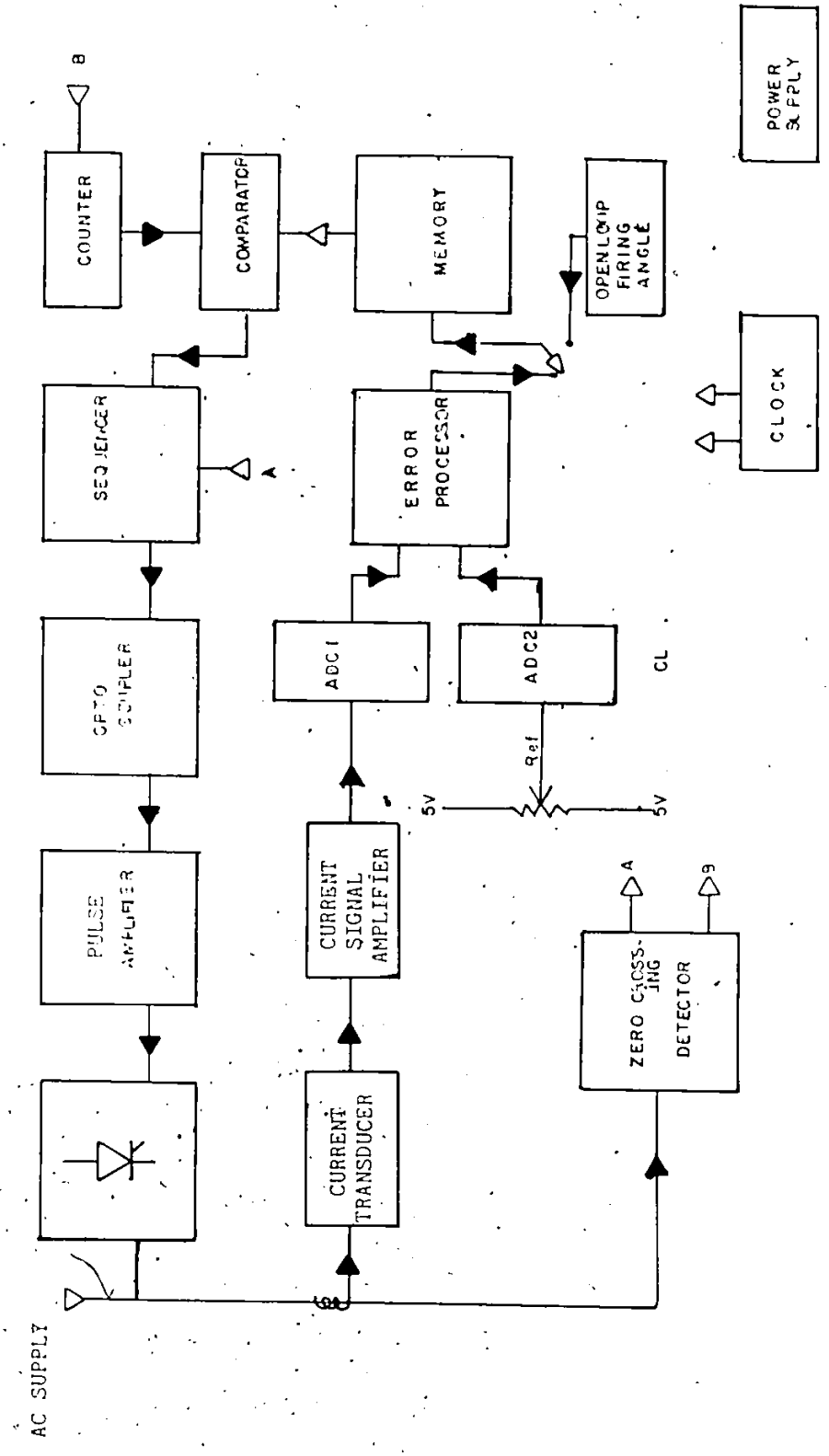


FIG. 4.1 THE FUNCTIONAL BLOCK DIAGRAM OF REGULATED CURRENT CONTROL SYSTEM

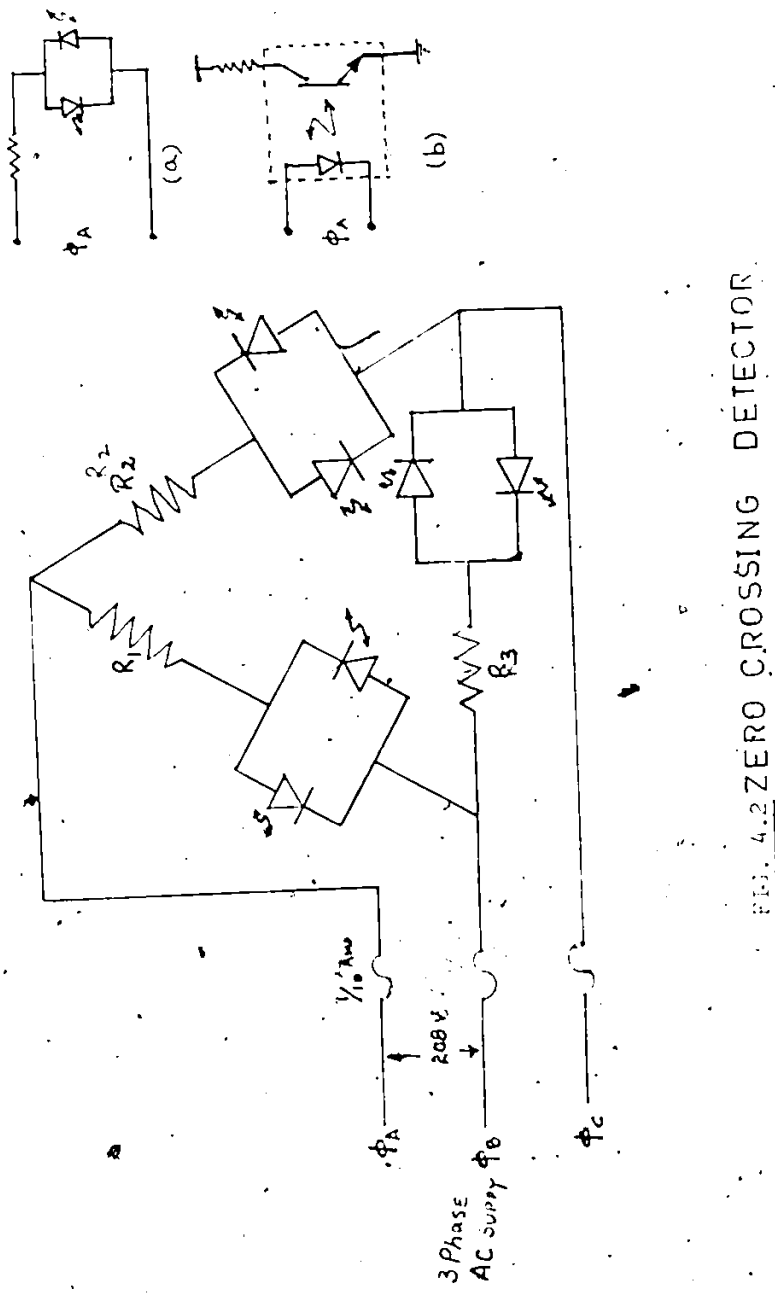


FIG. 4.2 ZERO CROSSING DETECTOR

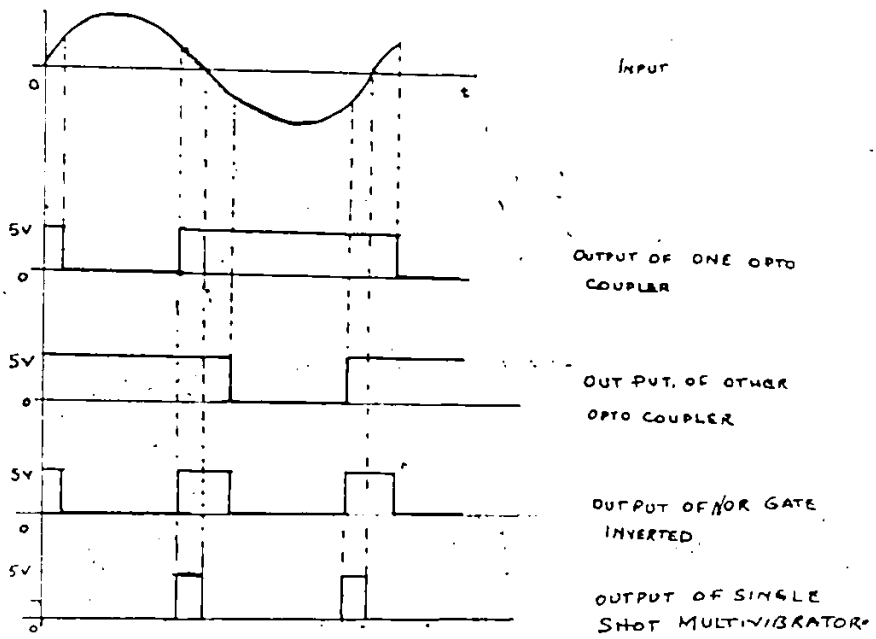


FIG. 4.3 ZERO CROSSING DETECTION CIRCUIT WAVE FORM

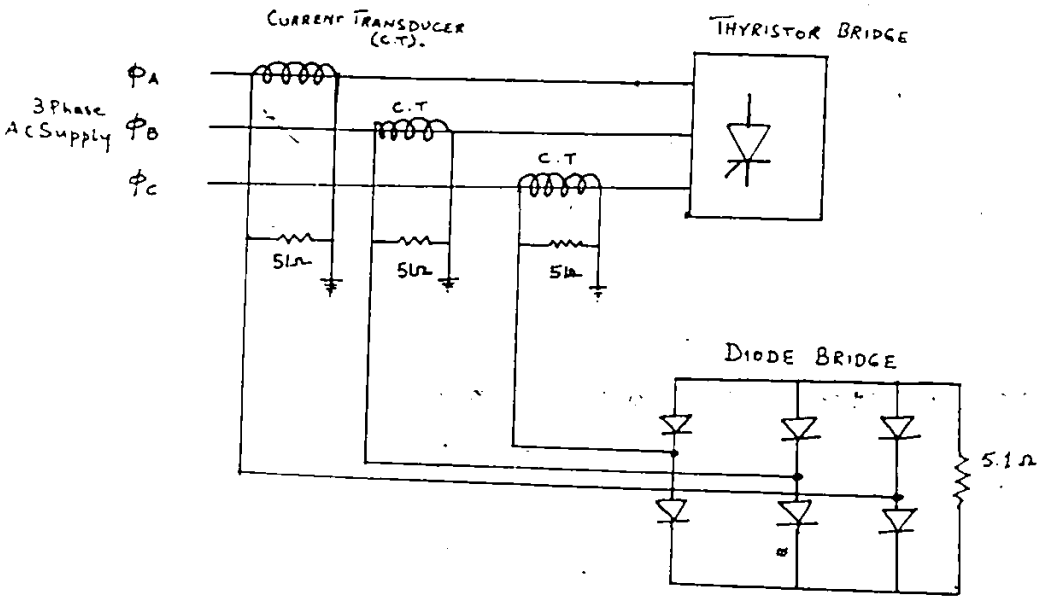


FIG. 4.4 CURRENT TRANSDUCER AND FULL WAVE RECTIFIER

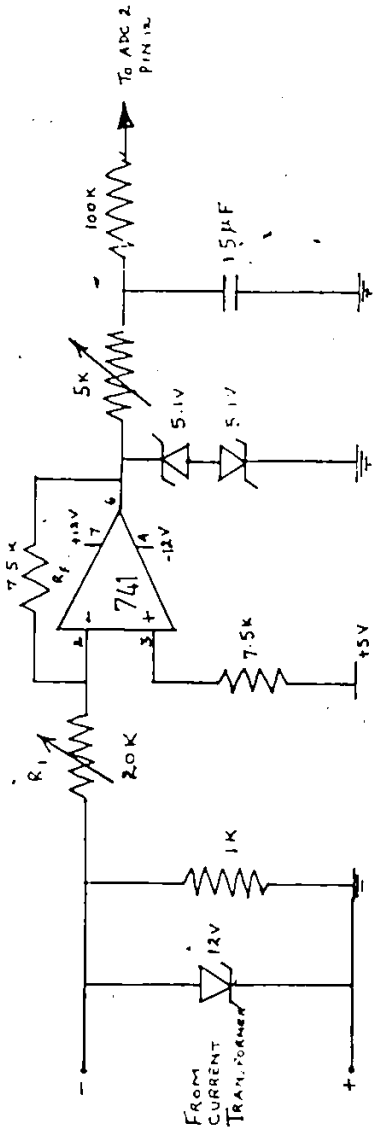


FIG. 4.5 CURRENT FEEDBACK SIGNAL AMPLIFIER

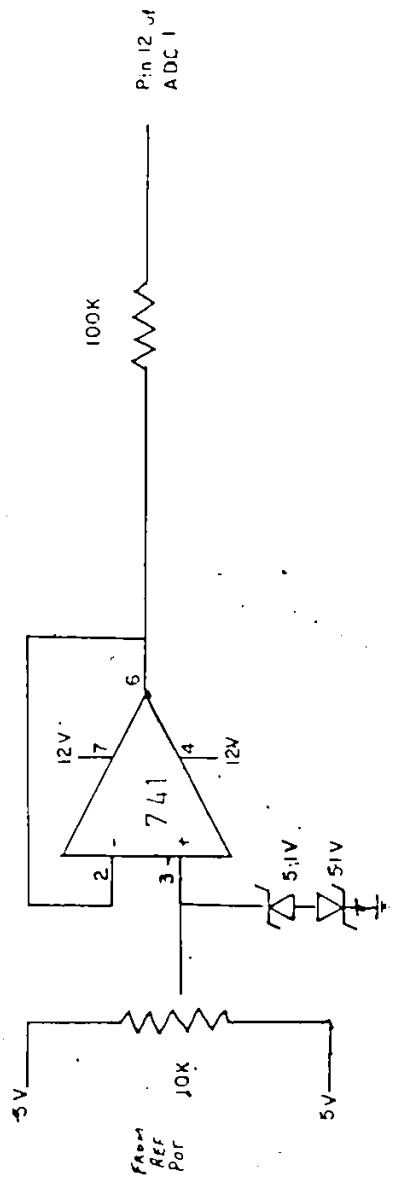


FIG. 4.6 REFERENCE SIGNAL BUFFER STAGE

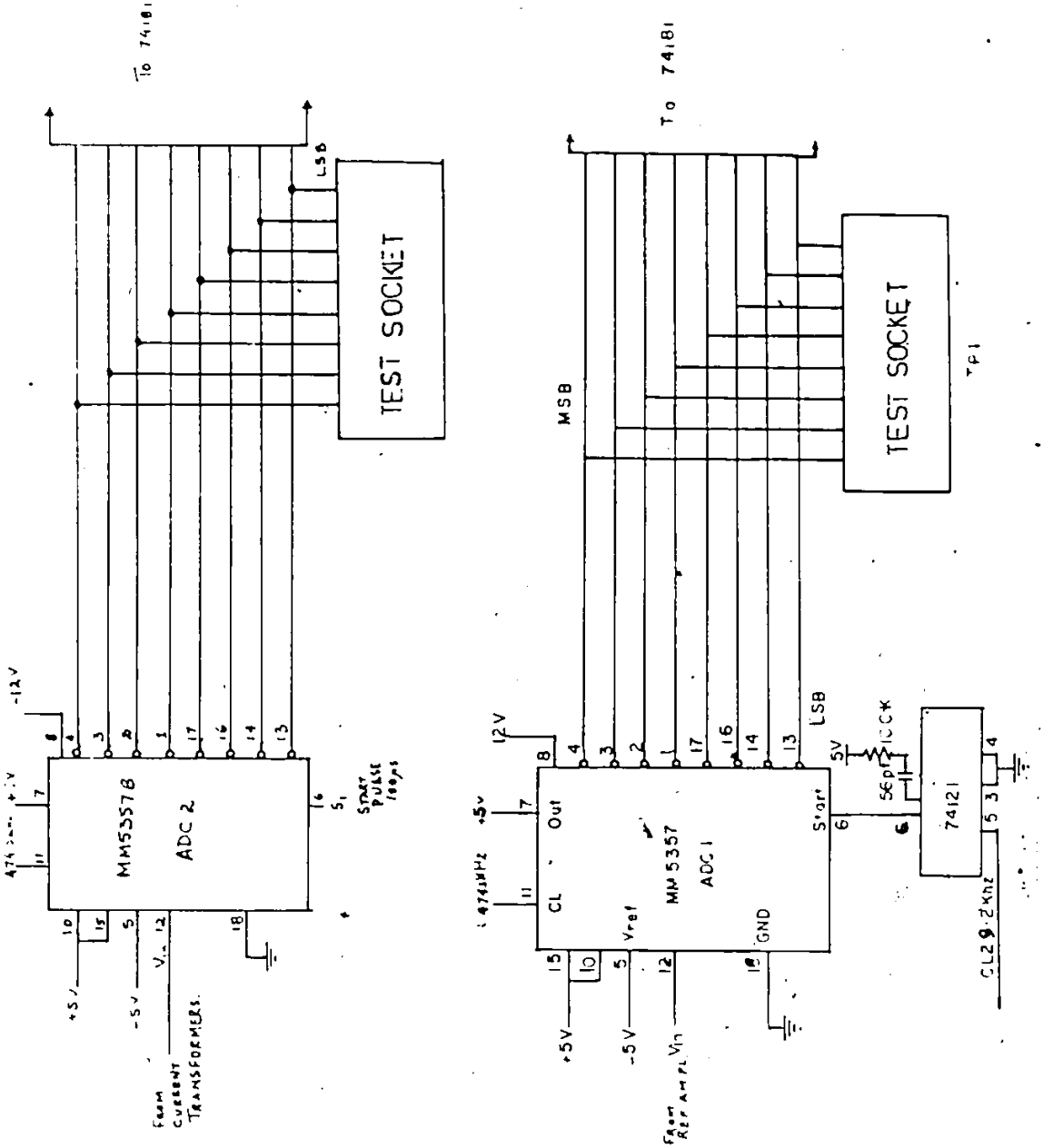


FIG. 4.7 ANALOG TO DIGITAL CONVERTER

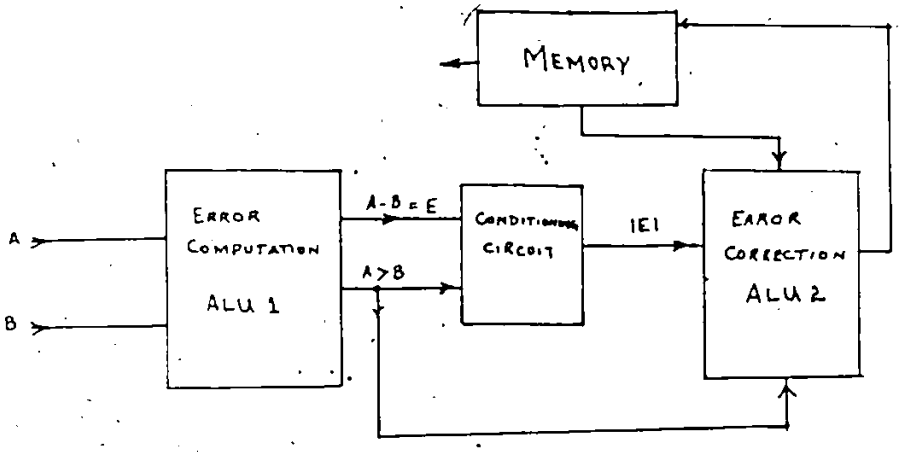


FIG. 4.8 BLOCK DIAGRAM OF ERROR PROCESSOR

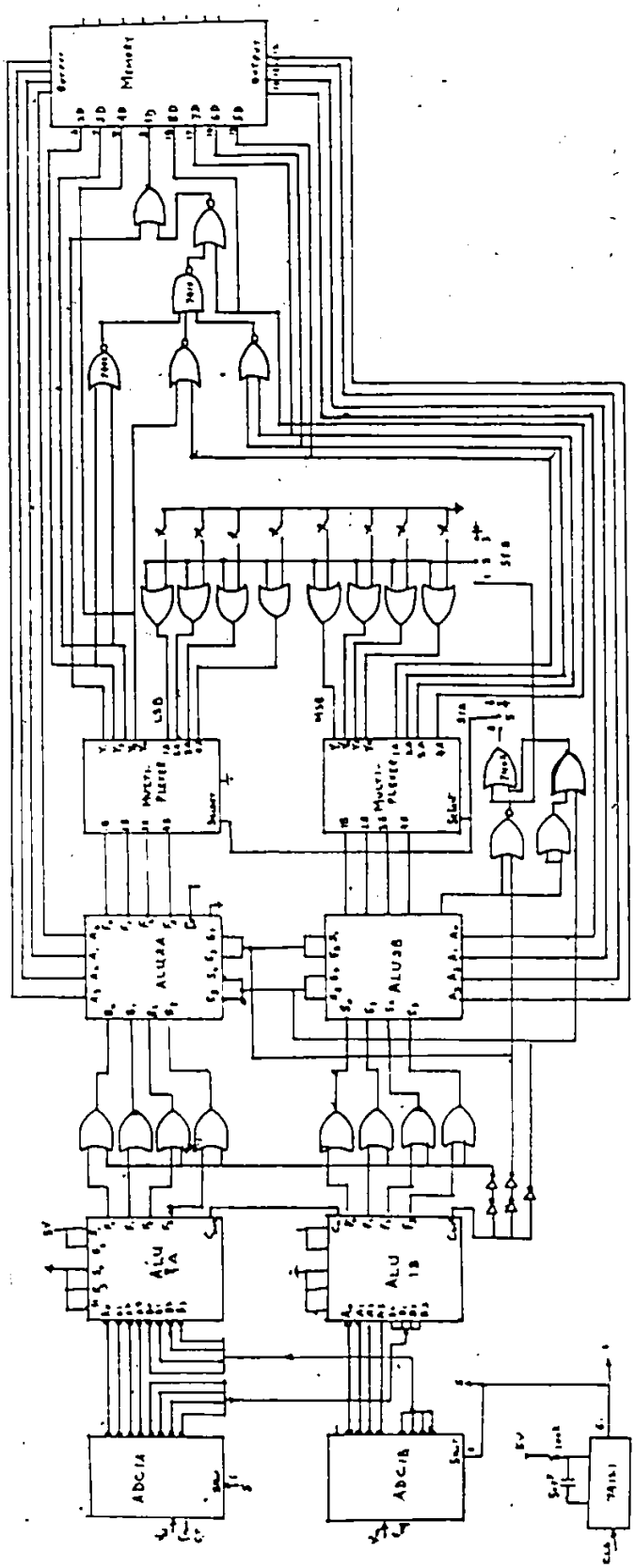


FIG. 4.9 CIRCUIT DIAGRAM OF ERROR PROCESSOR

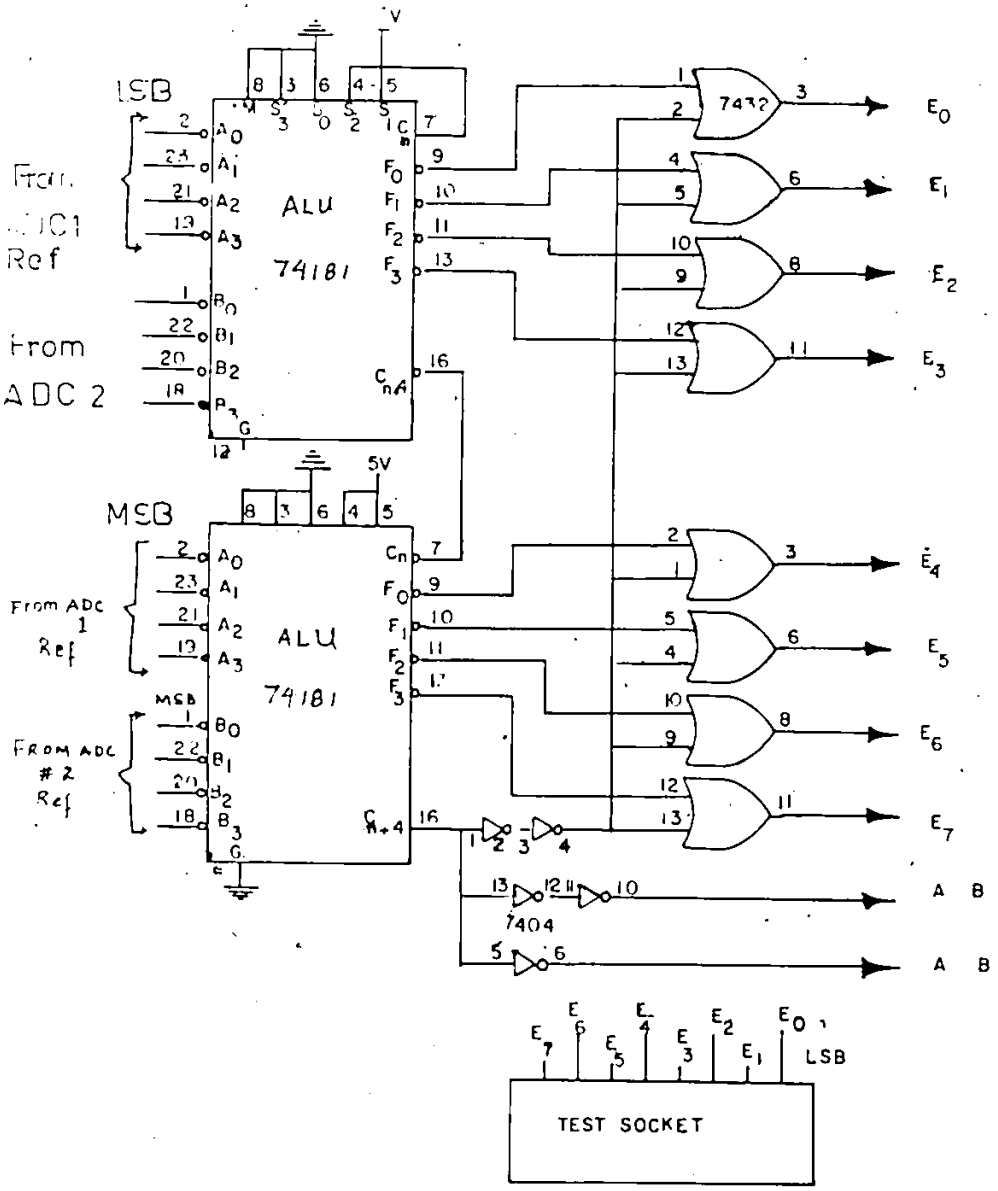


FIG. 4.10 ERROR COMPUTATION CIRCUIT AND ERROR CONDITIONING CIRCUIT

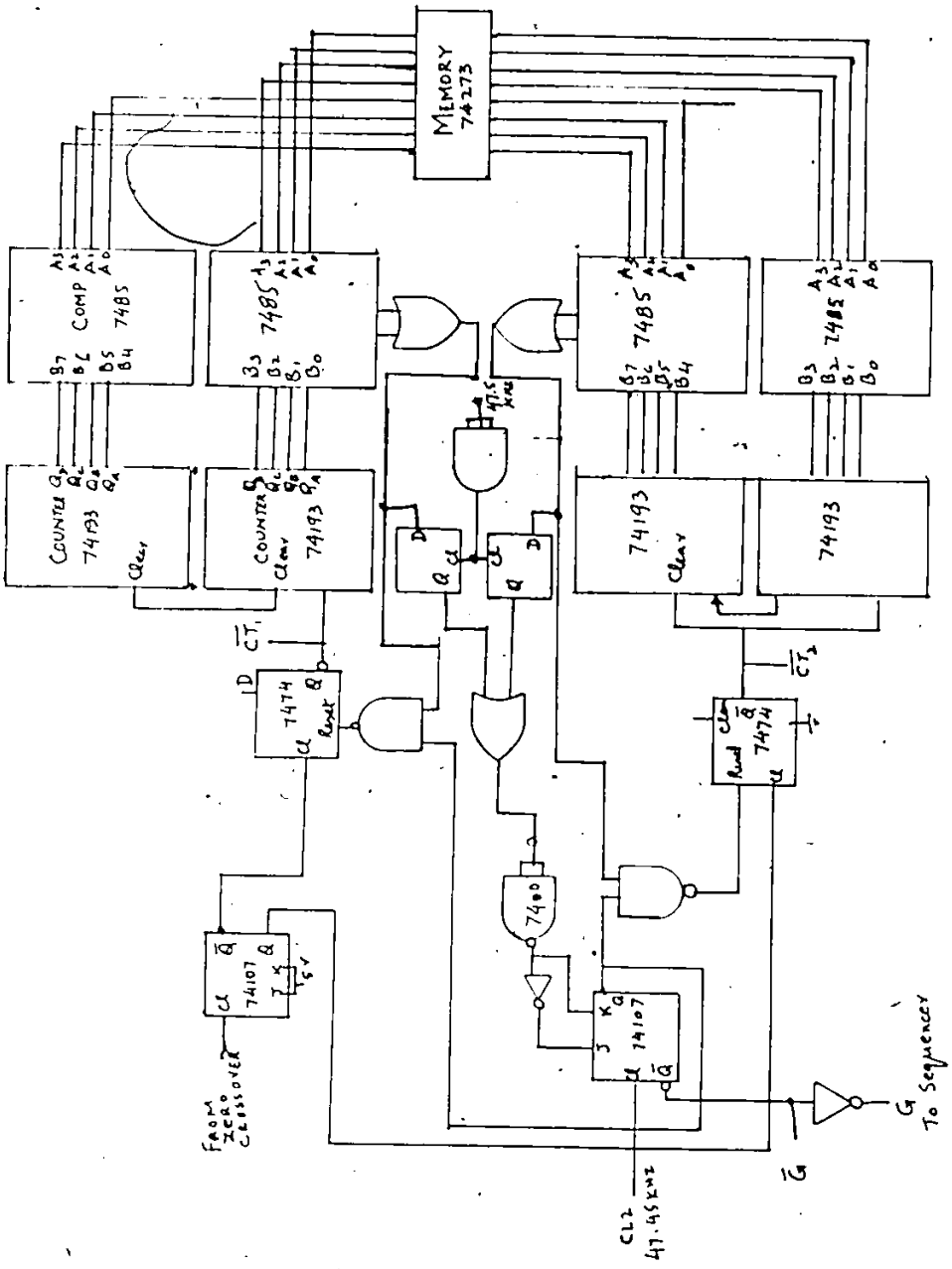


FIG. 4.11 COMPARATOR AND COUNTER CIRCUIT

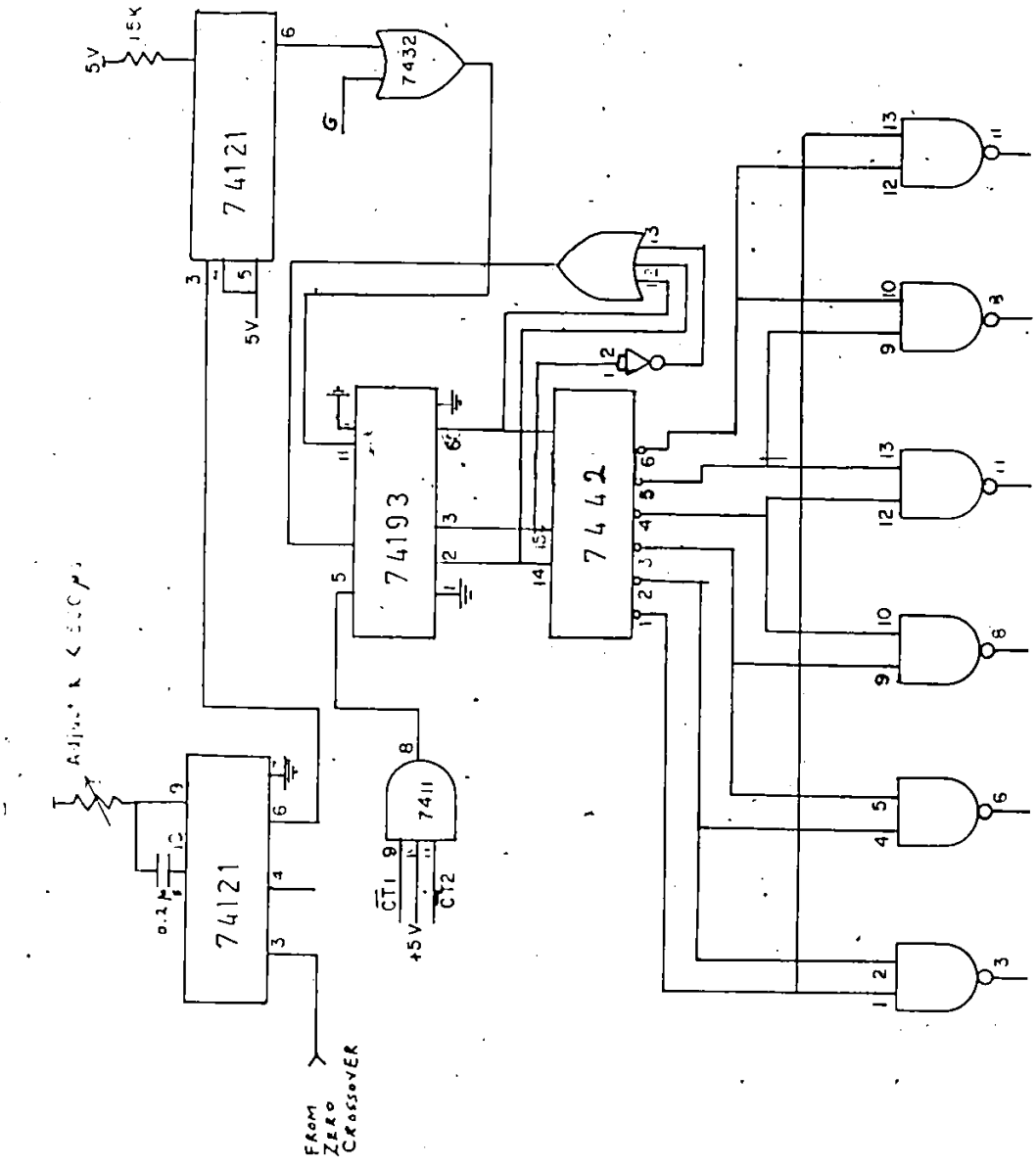


FIG. 4.12 SEQUENCER

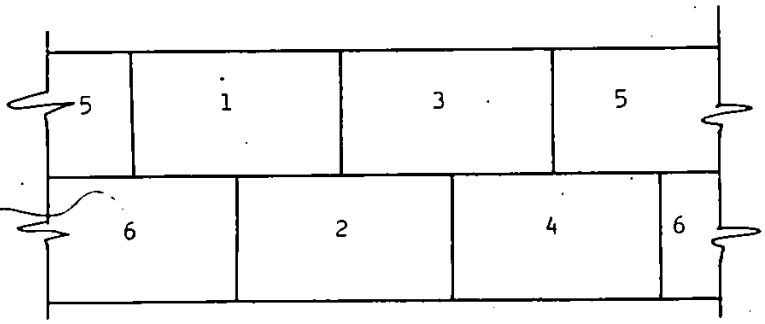


FIG. 4.13 FIRING SEQUENCE

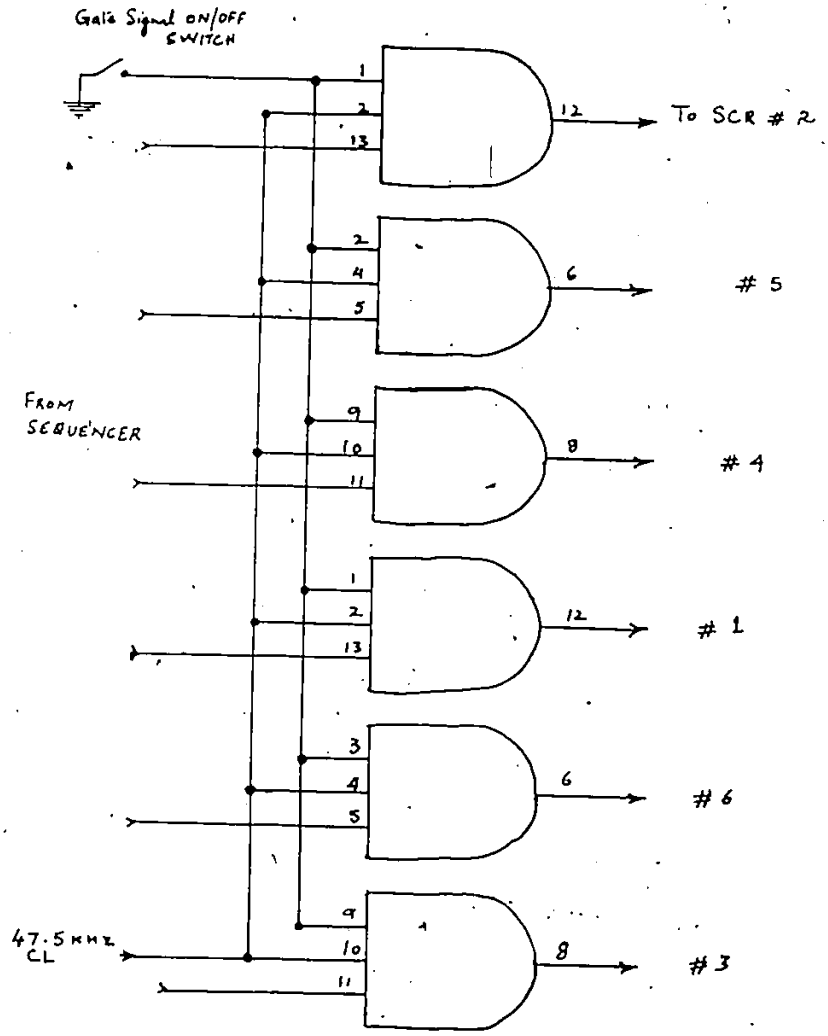


FIG. 4.14 GATING CIRCUIT

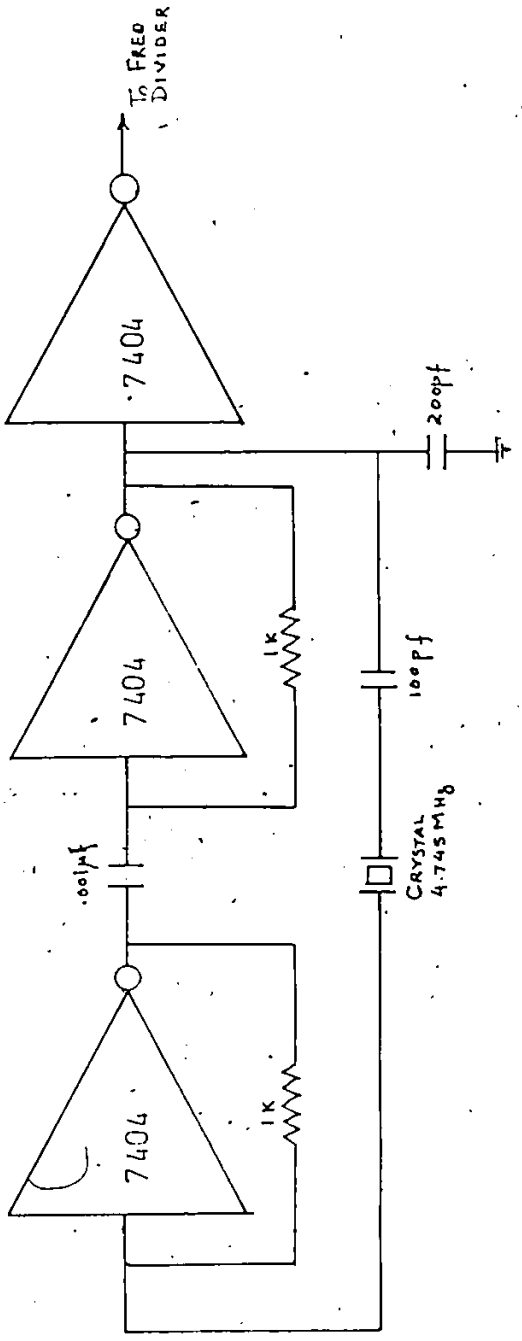


FIG. 4.15 MASTER CLOCK

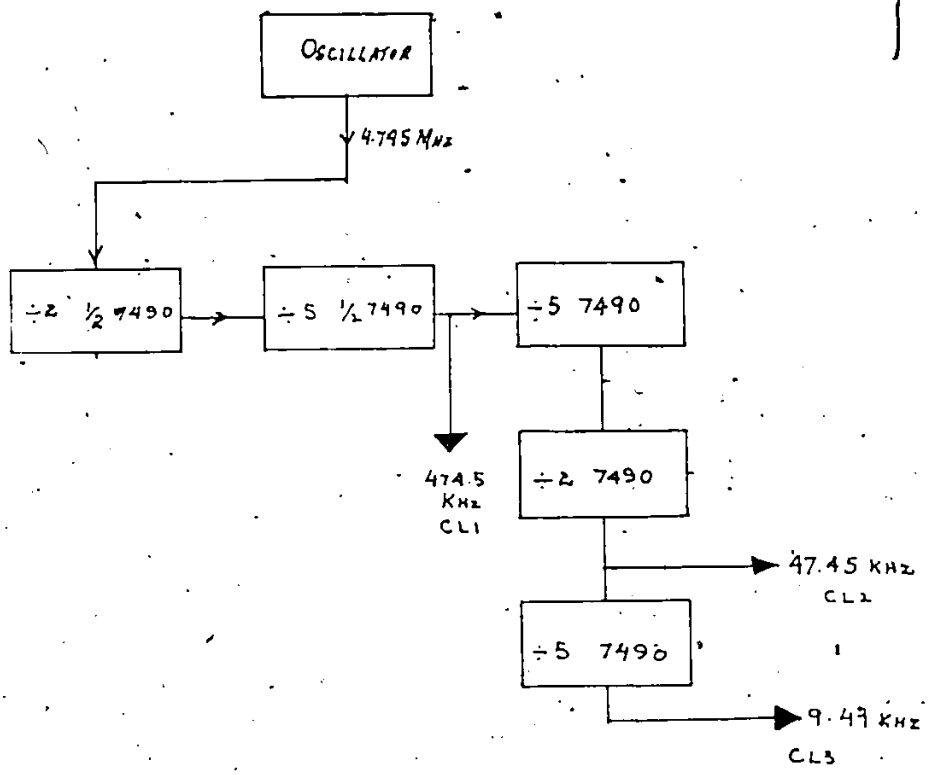


FIG. 4.16 FREQUENCY DIVIDING CIRCUID

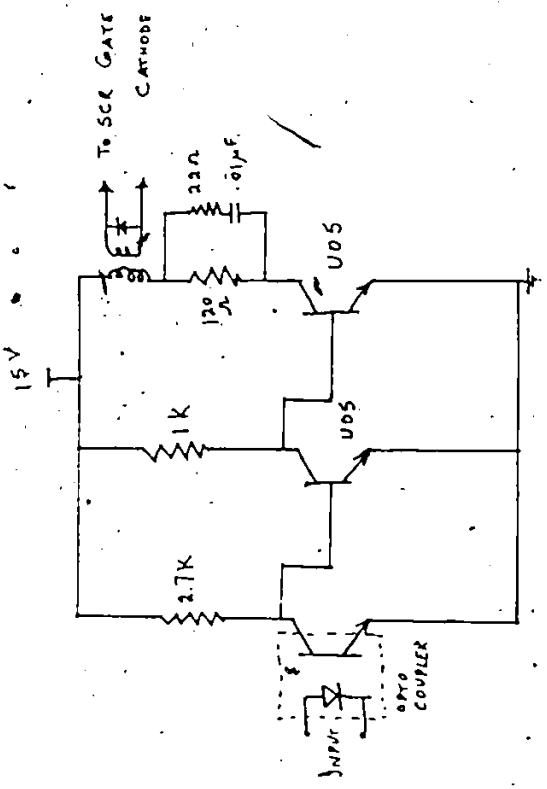


FIG. 4.17 PULSE AMPLIFIER

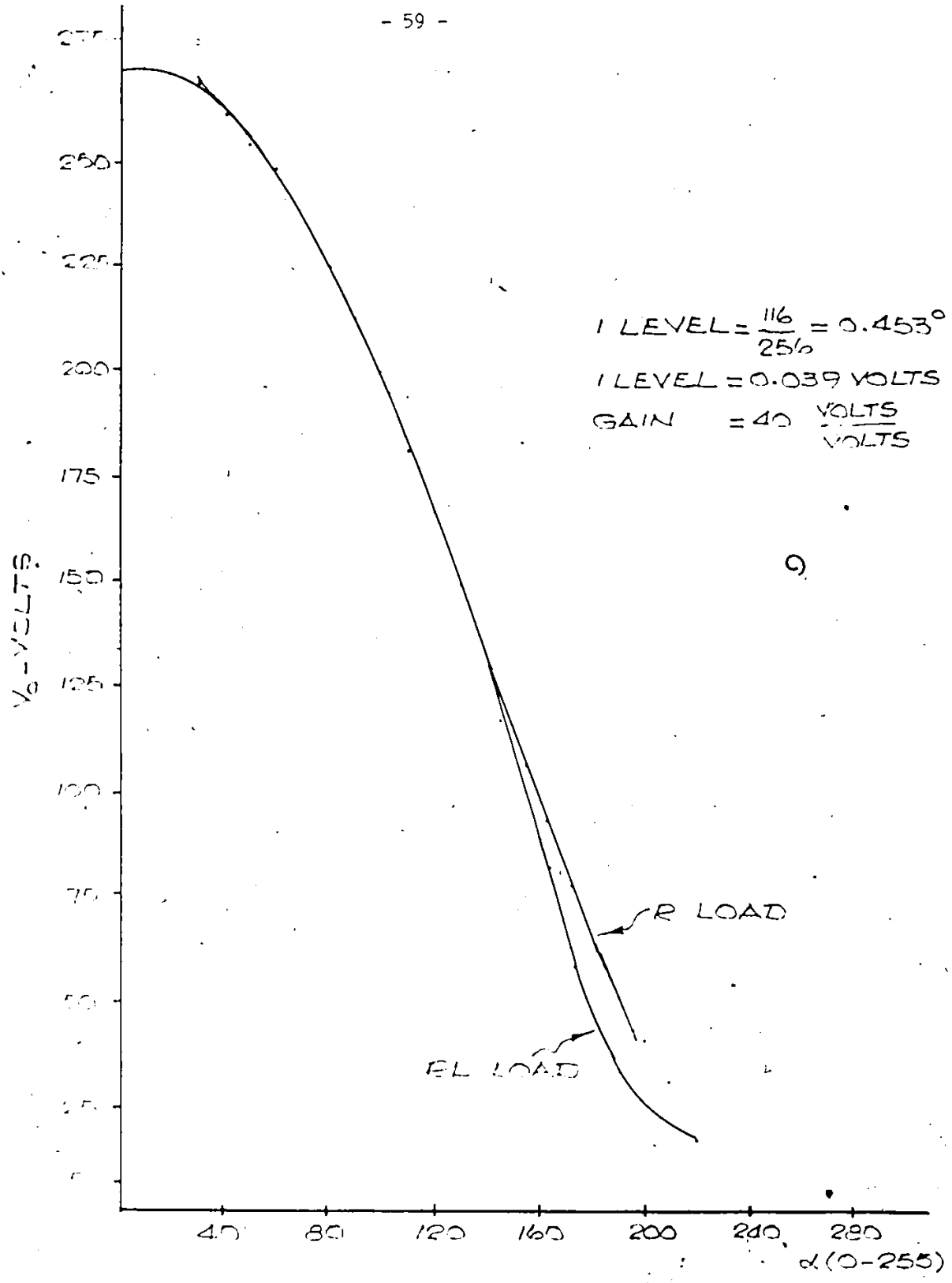
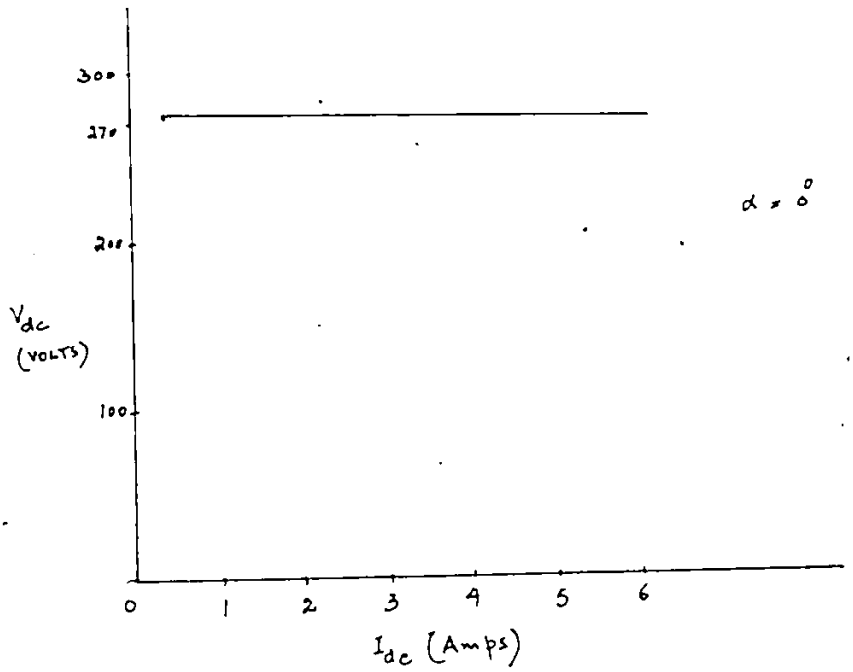


FIG. 5.1 TRANSFER CHARACTERISTICS OF THE CONVERTER



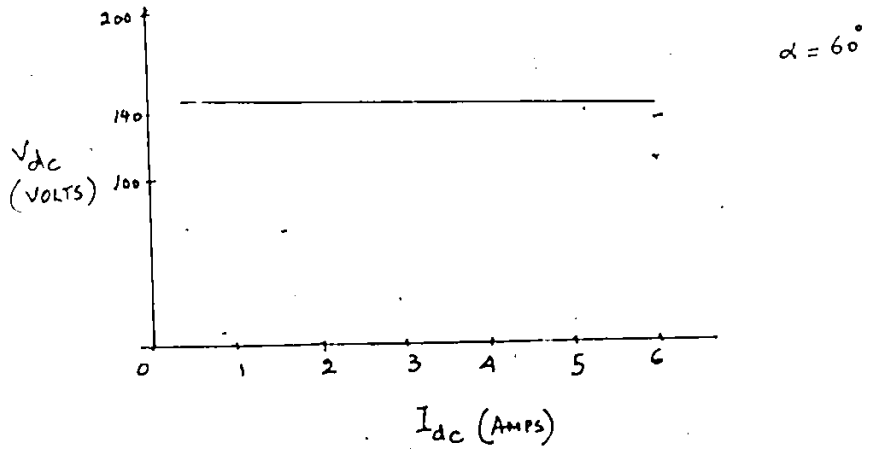


FIG. 5.2 REGULATION CHARACTERISTICS OF THE CONVERTER

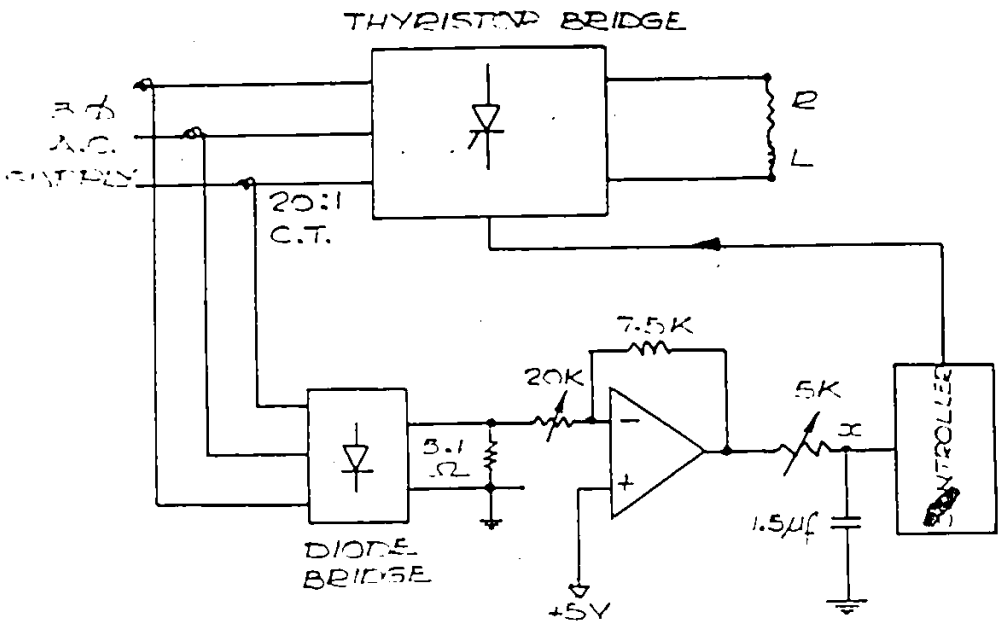


FIG. 5.3 EXPERIMENTAL SETUP

[POOR COPY]

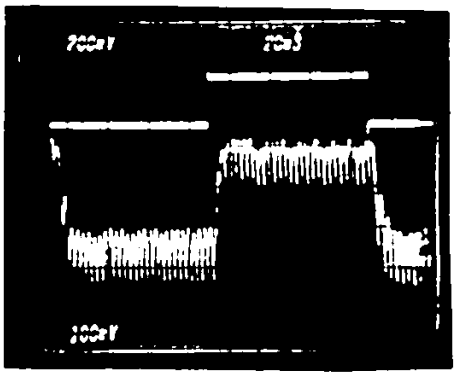


FIG. 5.4 SQUARE WAVE CURRENT SIGNAL RESPONSE OF THE CURRENT SOURCE WITHOUT FEEDBACK FILTER TIME CONSTANT

[POOR COPY]

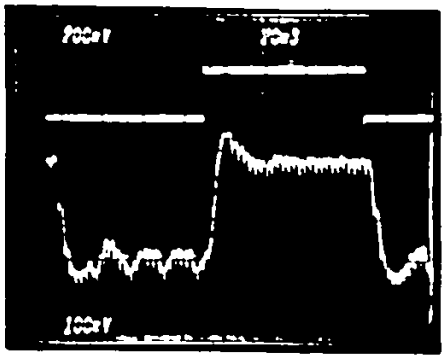


FIG. 5.5 CURRENT SIGNAL RESPONSE WITH 6.2 msec FILTER TIME CONSTANT OF FEEDBACK LOOP

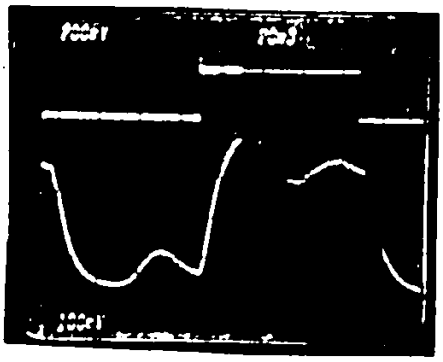


FIG. 5.6 CURRENT SIGNAL RESPONSE WITH MAXIMUM FILTER TIME CONSTANT OF FEEDBACK LOOP

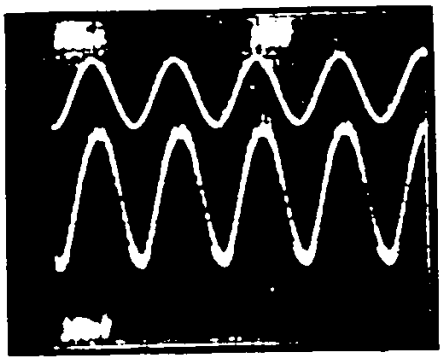


FIG. 5.7 FREQUENCY RESPONSE WITH
10 HZ INPUT CURRENT SIGNAL

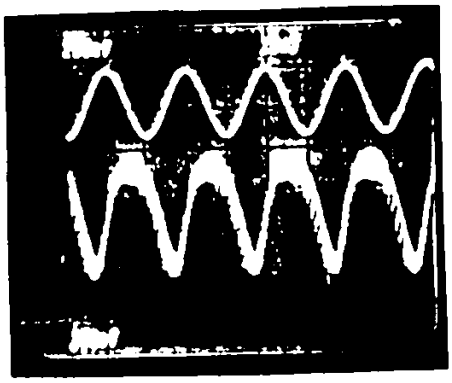


FIG. 5.8 FREQUENCY RESPONSE WITH
50 HZ INPUT CURRENT SIGNAL

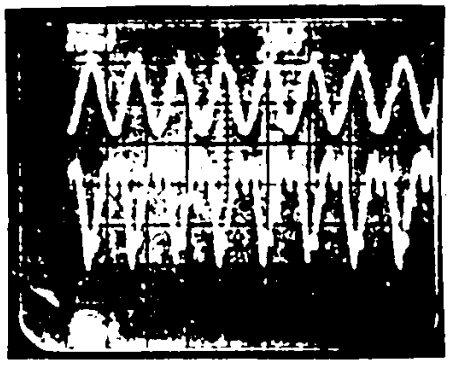


FIG. 5.9 FREQUENCY RESPONSE WITH
100 HZ INPUT CURRENT SIGNAL

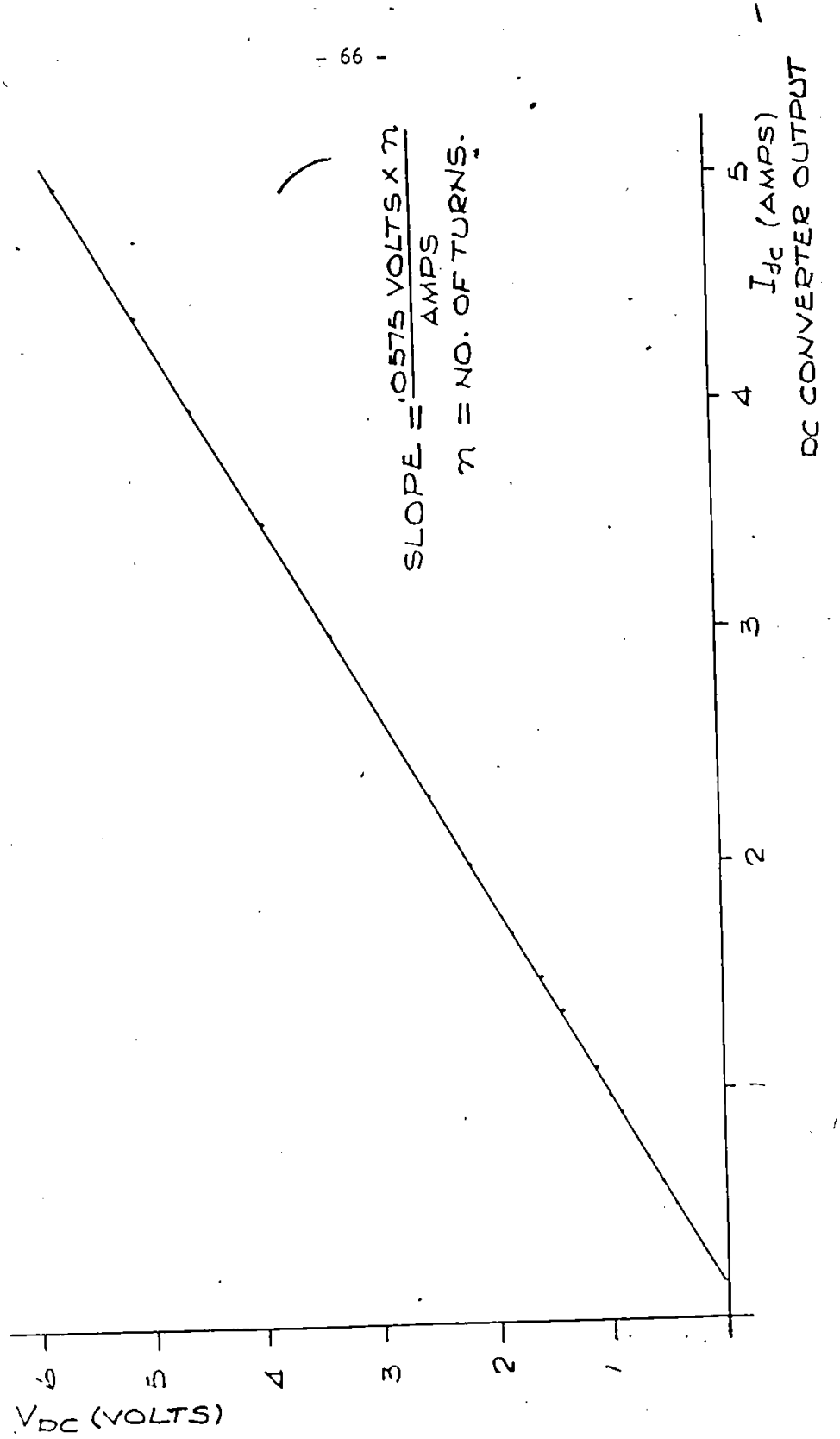


FIG. 5.10 CURRENT FEEDBACK CHARACTERISTIC CURVE

[POOR COPY]

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APPENDIX I

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