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Design of Polyphase Networks For High Selectivity, High Frequency Filtering

Mumtaz B. Gawargy

A Thesis

in

The Department

of

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Presented in Partial Fulfillment of the Requirements

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A B S T R A C T

Design of Polyphase Networks For High Selectivity, High Frequency Filtering

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Concordia University, 1986

A novel design approach in high selectivity single sideband modulation and demodulation using a polyphase network sequence discriminator is presented. The special case of a four phase network sequence discriminator is required for 90° phase shift circuits.

The tolerance requirements on capacitors to manufacture the circuits have been relaxed to a practical value of ±1% from the existing state of the art of ±0.2% through the invention of a new trimming procedure. The new ideas in trimming can be used for other circuit designs.

New circuits using buffered polyphase network sequence discrminators were invented. The circuits use capacitors of the same nominal value which simplifies the manufacture of the filter. These circuits allow high image band rejection to be achieved.

The filters were manufactured on a 1" x 2.5" substrate using thick film technology. The overall yield of the manufactured network is close to 100%.

For we know in part, and we prophesy in part. But when that which is perfect is come, then that which is in part shall be done away .

1 Corinthians 13: 9,10

To: Suzan, Maryam, Michael, Manar and Mark

With Love.

ACKNOWLEDGEMENT

I am most grateful to my doctoral thesis supervisors, Professor M.N.S. Swamy, Dean of Engineering and Computer Science, Concordia University and Professor W.B. Mikhael, Chairman of Communications and Signal Processing, West Virginia University, for their contribution in the field of the research which forms the basic background of the present work, and for their continuous advice and guidance throughout the whole program.

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List of Abbreviations and Symbols

A	= Loss in dB
AR	= Reference level of loss in dB
A,B,C,D	= Transmission matrix parameters of an electrical network
C	= Capacitance value in Farads
f	= Frequency in Hz
fc	= Carrier frequency
G	= Conductance value in Mhos
I	= Current in Amperes
j	= $\sqrt{-1}$
Li	= Loss in dB at frequency point of index i
R	= Resistance value in Ohms
SD	= Sequence discriminator
G	= Conductance value in Mhos
	= Polyphase network
s = jw	= Laplace's variable
Si	= Sequence of vectors of index i
Tij (s)	= Voltage transfer functions between nodes i,j
V	= Voltage in Volts
w = 2 π f	= Angular frequency in rad/sec
δ	= Magnitude error of a signal
Δφ	= Phase error of a signal

Chapter 1

INTRODUCTION

CHAPTER 1

INTRODUCTION

For more than fifty years, single-sideband (SSB) modulation has prevailed over other modulation schemes in analog multiplex communication systems. The applications are quite large in number. To quote a few, they are wireless communication systems like HF radio for military telephony, Radio hams, Carrier Communications etc. Particular mention has to be made of the Carrier Communication system. In this system, SSB is dominant. The public telephone which basically employs the SSB is expanding at a global rate of about one million SSB channels per year. There is no further need to emphasize the advantage gained by employing SSB for such systems. In fact, consistent and continuous efforts are being made all over the world in order to further improve the state of the art and the economics of SSB technology in frequency-division multiplex (FDM) communication systems. FDM systems are usually built in the form of a hierarchy of modulation steps. Each modulation step combines a number of channels from the previous modulation steps. For example, the basic group consists of 60 - 108 KHz consisting of twelve voice channels, each having a bandwidth of 4 KHz. In the next modulation step, five such basic groups are modulated into the next basic super-group 312 - 552 KHz. This system is common

irrespective of the transmission medium, whether it is a radio, or a cable or a satellite link. In fact, modern FDM systems carry several thousands of SSB channels over one link. This dense packing of channels into the available spectrum of a transmission medium requires sharp filtering in order to separate the individual channels and for the suppression of unwanted modulation products in each SSB modulation step. The channel bandpass filters (CBF) shall be designed to meet the required specifications, while keeping in mind the cost factor.

1.1 State of the Art of Channel Bank Filters (CBF's)

The following types of filters are generally employed in order to achieve the required high selectivity:

(a) Inductor-Capacitor (LC) filters

(b) Crystal Filters

(c) Mechanical Filters

(d) Resistor-Capacitor Active Filters

(e) Recently proposed Polyphase Filters (1)

In all the above filters, it is to be noted that the higher the frequency band the more complex the filter will be.

LC filters are bulky, require large space and have to be manually tuned. In addition, each frequency band of interest requires a different filter design. These factors limit the use of LC filters.

Crystal filters have the advantage of exhibiting selective characteristics, but suffer from the following disadvantages, namely:

i) The filter characteristics vary considerably with temperature, unless expensive crystals are used.

ii) The filter requires manual adjustment after manufacturing which adds to the cost, unless complex monolithic approaches are used.

iii) Each frequency band of interest requires a different filter design.

Mechanical filters can be used. However, they also suffer from certain disadvantages, which are:

i) Manufacturing facilities are difficult to set up and require large capital investment.

ii) They require tuning as a part of fabrication.

iii) Each frequency band requires a different filter design.

Active RC-filters have been used during the last twenty years to design CBFs (2,3,4,5). The best contribution in this direction is due to Saraga in 1978 (3). He was able to design two of the twelve filters required for the 60-108 KHz channel bank. He developed a trimming algorithm and a very accurate simulation of the filters which allowed

the use of ±10% tolerance capacitors in order to achieve the required performance. However Saraga's design has the following disadvantages:

i) The filters were not designed to meet system requirements with out-of-band signalling facilities, where frequencies up to about 3850 Hz in each channel may have to be transmitted.

ii) The filters entail extremely tight resistor tolerance requirements (±0.1%), which are very difficult to achieve unless very slow and expensive trimming procedures are followed.

iii) The two filters that were designed did not meet a temperature variation of 10-40 degrees centigrade. (Normal temperature requirements in North America are 0-70 degrees centigrade).

iv) A different design is required for each of the twelve channels.

In all the above CBF's, it is seen that a different design is required whenever different channels are used. This disadvantage alone could be the determining factor, even if all other problems could somehow be resolved with new technologies or techniques.

During the past decade, different attempts have been made to introduce the polyphase technique to single sideband modems (1,6,7). None of the attempts could be used in manufacturing. One of the discouraging factors was the tight tolerances required for the capacitors, which is of the

order of ±0.2 % . However, there are some important advantages of the polyphase technique which can be summarized as follows:

1. The single sideband modem can be operated at different frequency bands by changing the system clock.
2. The phase shift network can be miniaturized using thick or thin film technology.

In addition to the disadvantage of tight tolerance of the capacitors, the other disadvantages are:

1. Sensitivity is a big factor, because of very low component tolerances required.
2. Even with expensive components, the highest image rejection achieved was only 57 dB.
3. The existing design by E. Daoud (6) does not meet the power consumption requirements and it was not designed for wideband applications.
4. Timing is a problem in both modulation and demodulation.

1.2 Scope of the thesis:

From the previous discussion, it is easily seen that the polyphase concept is very promising for designing CBF's. This thesis advances the state of the art of the above concept so as to produce highly selective

filters using components having reasonable tolerances. The following points are highlighted:

1. An accurate trimming procedure is given which permits the use of capacitors having a tolerance of ±1 % .

2. Optimization of the tolerance procedure through the derivation of the sensitivity of the structure is formulated. This allows further simplification of the trimming of the wideband polyphase filters.

3. The buffered polyphase concept is introduced, which allows the cascading of polyphase networks , which permits us to achieve higher out-of-band rejection.

4. The exact timing requirements for the modem are derived so as to achieve out-of-band requirements.

5. The designed polyphase network is implemented using thick film technology.

6. The polyphase network is used in FDM channel banks.

Chapter Two outlines the polyphase concept, followed by single polyphase network and wideband polyphase network designs, with the application to the new buffered polyphase network. Chapter three will deal with the

sensitivity analysis. Because of the complexity of the network under investigation , a closed form analysis is extremely difficult, and the way to handle more than sixty R,C components and other stray components was overcome through computer simulation. Chapter four explains the trimming procedure for the single stage polyphase networks and extends the concepts to the wideband polyphase network. Chapter five describes the factors which should be considered in the design of SSB modem , with emphasis on the effect of the on-resistance of the switches and the timing errors on the performance of the polyphase network. Chapter six shows the temperature and humidity effects. Chapter seven describes the different statistical simulations from the quick simplified component tolerance simulation, to the exact statistical simulation which includes the trimming procedure. Chapter eight gives sample test results while Chapter nine summarizes the conclusions and discusses possible future developments related to the polyphase network design concept. The reader is encouraged to read chapters in the order he wishes to, except for the first two chapters. The introduction is important, as is the second chapter which includes basic information on the polyphase concept.

Chapter 2

DESIGN OF POLYPHASE NETWORKS

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DESIGN OF POLYPHASE NETWORKS

2.1 Definition of Positive and Negative Symmetric Sequences

Let us define a symmetric sequence (1) as a set of vectors containing more than two vectors that are equal in magnitude and equally spaced in phase. For present applications we will consider only the special case of four vectors. Each vector represents an alternating voltage and can be represented by Ve^{jwt} i.e. the magnitude of the vector (= V) and its frequency (= w rad/sec).

We will define the positive sequence as the sequence of vectors 1,2,3,4 (Figure 1a) in the clockwise direction and the negative sequence as the sequence of vectors 1,2,3,4 (Figure 1b) in the anticlockwise direction. In Figure 1, S1 is the positive sequence, S2 is the negative sequence, and S3 = S1 ± S2 is their vector sum.

It is to be noted that the sequence whether positive or negative is composed of vectors rotating anticlockwise with angular velocity = w rad/sec.

2.1.1 Design Objectives for Single-Sideband Applications

In practice we do not have a symmetric sequence of four signals but this is actually what we want to achieve in the ideal case as an output sequence. To find a suitable input, the opposite procedure is performed. Since the possible input signals are of unsymmetric form, they can be formed only by adding at least two symmetric sequences of different polarity like S3 in Figure 1C. Figure 1D shows a circuit to generate a sequence like S3, which is composed of both the positive and the negative sequences S1, S2. It is desired that only one sequence survive over the wanted frequency band such that our desired signals from the network are equal in amplitude and 90° apart in phase.

2.2 Single-Frequency Notch Sequence Discriminators

Consider the sequence discriminator shown in Figure 2a. It is easy to show that the chain matrix for one path, for example 1 to ground as an input and 5 to ground as an output is as follows:

a) for the positive sequence:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \frac{1}{1 - wCR} \begin{bmatrix} 1 + jwCR & R \\ 2jwC & 1 + jwCR \end{bmatrix} \begin{bmatrix} V_5 \\ -I_5 \end{bmatrix}$$

The open-circuit transfer function is:

$$T_{51+} = \frac{V_5}{V_1}\bigg|_{I_5=0} = \frac{1 - f/f_1}{1 + jf/f_1}$$

$$\text{where } f_1 = \frac{1}{2\pi RC}$$

b) for the negative sequence:

$$\begin{bmatrix} V_1 \\ \end{bmatrix} = \frac{1}{1+wCR} \begin{bmatrix} 1+jwCR & R \\ 2jwC & 1+jwCR \end{bmatrix} \begin{bmatrix} V_5 \\ -I_5 \end{bmatrix}$$

and

$$T_{51-} = \frac{V_5}{V_1}\bigg|_{I_5=0} = \frac{1 + f/f_1}{1 + jf/f_1}$$

Figure 2b shows both the positive and negative sequence frequency responses. The loss in dB for a positive sequence varies with frequency according to the equation:

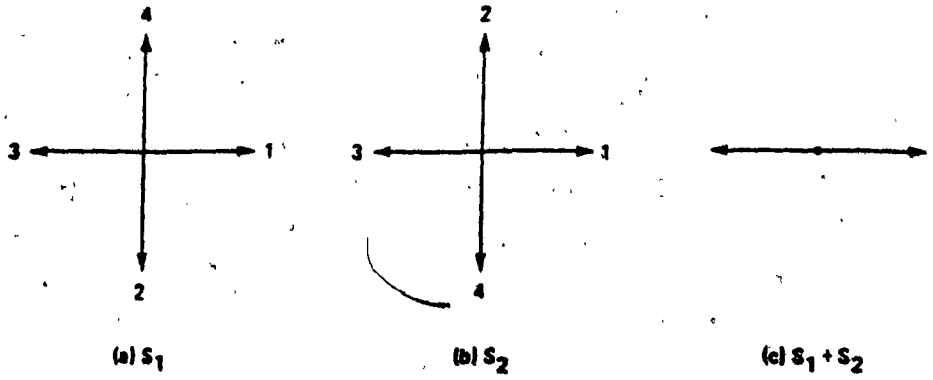
$$\text{Loss} = 20 \log_{10} \left| \sqrt{1 + (f/f_1)^2} / (1 - f/f_1) \right|$$

Figure 3 shows the 30 dB bandwidth Δf where Δf can be derived from the above equation to be:

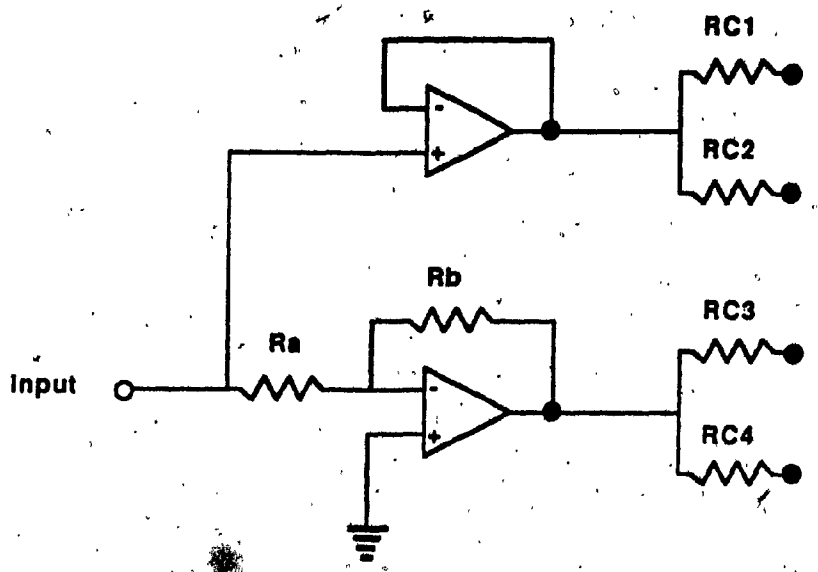
$$\Delta f \cong 0.08933 \times f_1$$

where f_1 is the centre frequency.

Higher rejection is possible at the expense of reducing the bandwidth for a single-stage sequence discriminator, however, if both wide-band and high rejection are required, then a cascade of these single frequency notches will help in achieving the requirements as will be shown in the next section.



(a) S_1 (b) S_2 (c) $S_1 + S_2$



(d)

Figure 1. (a) Positive Sequence
(b) Negative Sequence
(c) Sum of Positive and Negative Sequences
(d) Generation of S1 + S2

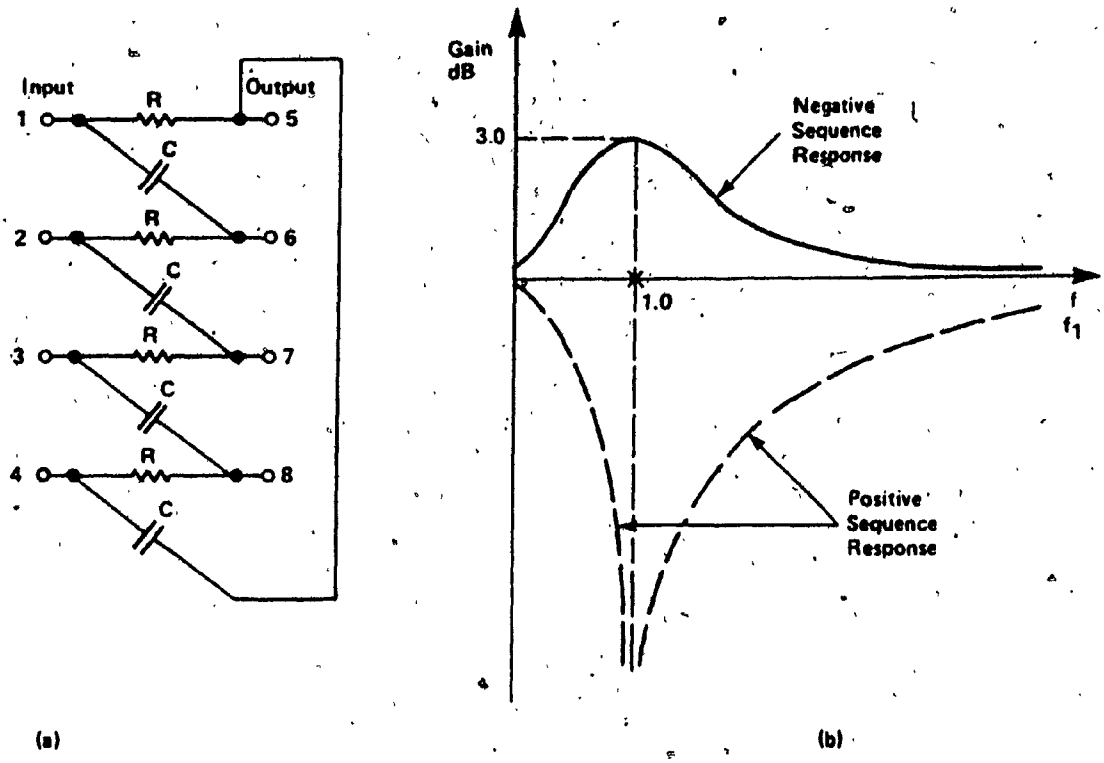


Figure 2 (a) Four Phase Sequence Discriminator
(b) Frequency Response

2.3 Wide-Band Sequence Discriminators

To design wide-band sequence discriminators, Gingell (5) suggested cascading a number of sections whose notch frequencies are well distributed in the band of interest.

Although different techniques can be used to get the optimum response, none of these solutions leads to an acceptable in-band ripple. Figure 4 shows a solution to the ripple problem suggested by Mikhael (1,3). The addition of the four resistors to ground will result in a modified chain matrix such that:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \frac{1}{1+jwCR} \begin{bmatrix} 1 + \frac{R}{RG} + jwCR & R \\ 2jwC\ (1 + \frac{R}{2RG}) + \frac{1}{RG} & 1 + jwCR \end{bmatrix} \begin{bmatrix} V_5 \\ -I_5 \end{bmatrix}$$

The modification can be shown to improve the in-band ripple without noticeable change in the image-band.

It is to be noted that these resistors to ground need not necessarily be added to all the stages, it may be only necessary to add them to a few stages.

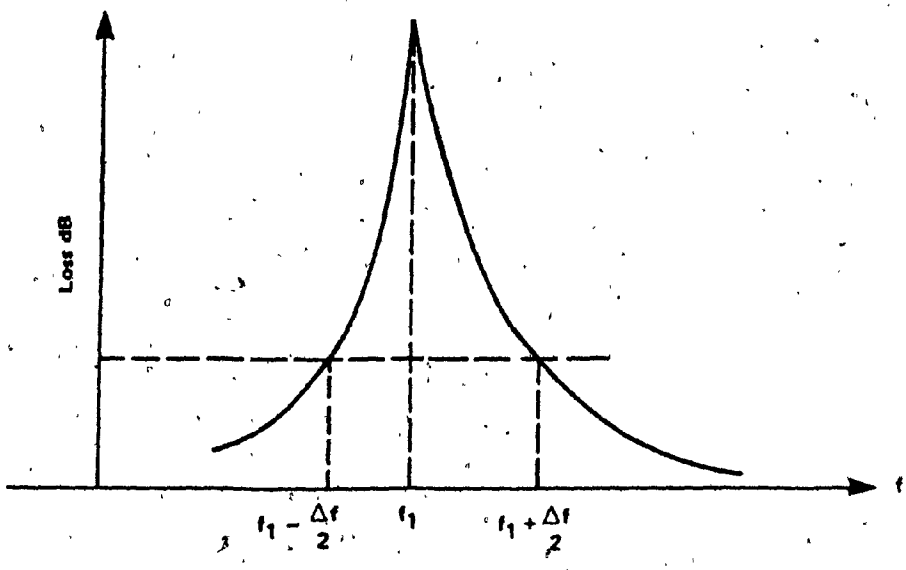


Figure 3 The 30 dB Bandwidth for the Single Frequency Notch Sequence Discriminator

$$\Delta f \approx 0.08933 \ f_1$$

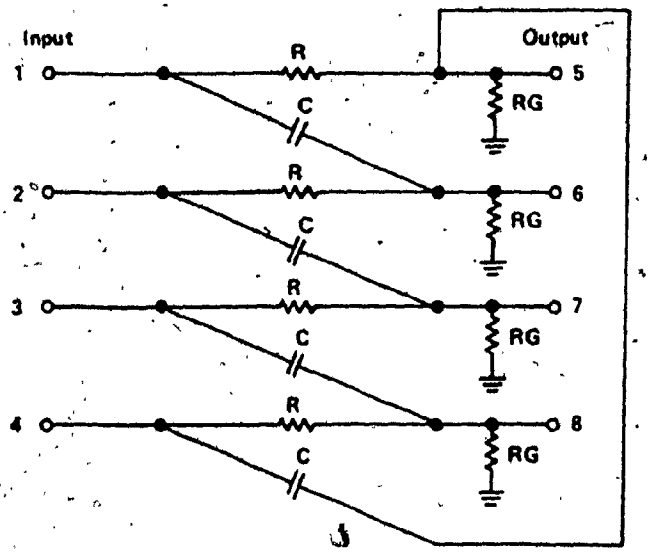


Figure 4. Additional Resistors to Ground to Minimize in-Band Ripple

The position of these added resistors can be found through a number of optimization runs. In these runs it is recommended to start with the addition of these resistors in one stage and find out which stage will give the optimum results. If the result is not acceptable, more than one stage should be tried to get the optimum location of these two stages.

Mikhael's design (1) used six stages with resistors to ground in some stages. Using ±0.2% capacitors, 57 dB image rejection could be achieved.

Attempts were made to increase the image rejection by increasing the number of stages, but these attempts did not show improvement. The theoretical improvement in image rejection was taken away by component tolerances added to the network. It was concluded that six stages is optimum for the passive design. The active design by Daoud et Al [6] was for notch frequency applications; it was not designed to fit into wide-band applications.

2.4 The New Design

It was found through simulation that the novel idea of designing two separate sequence discriminator networks with a unity gain buffer in between is the best solution to achieve higher out-of-band rejection.

The theoretical explanation is simple; losses are added for buffered networks, while in a cascade of networks, the chain matrix of the resulting network equals the product of the chain matrices of the individual networks, which is not equivalent to the addition of the individual losses because of the interaction of the other chain matrix parameters.

In our approach of buffered polyphase networks we start with the design of n stages, then we optimize the location of the buffer (buffers) and finally we optimize the location of the stage (stages) where we need to add grounded resistors.

The network requirements could be achieved with a seven-stage polyphase filter, a buffer after the sixth stage giving optimum results in the transmit direction. The additional resistors to ground were needed only at the fourth stage, which resulted in a big saving in the substrate area.

Figure 5 shows the circuit diagram of the seven-stage buffered polyphase filter. For clarity of the figure, cross connections for the nodes X1, X2, ... X7 are not shown.

Figure 6 shows the nominal response of the polyphase filter with peaks corresponding to the notch frequencies of the sections.

The present design can be used for the transmit or the receive directions. We call it the compromise design to differentiate between it and the alternative of having two different designs, one for the transmit and one for the receive directions.

It is possible to design two different sequence discriminators with different topologies one for the transmit path and another for the receive path; instead, a compromise design was done for either transmit or receive. One design is not optimum for both; the optimum location of the buffer and/or the added resistor to ground is different for the receive path.

The main advantages of having only one design are:

1. Development cost is reduced to about 70%.
2. Reduced manufacturing costs.
3. All sequence discriminators failing in one path have a high probability of passing in the other path, such that the overall yield is higher than for individual designs.

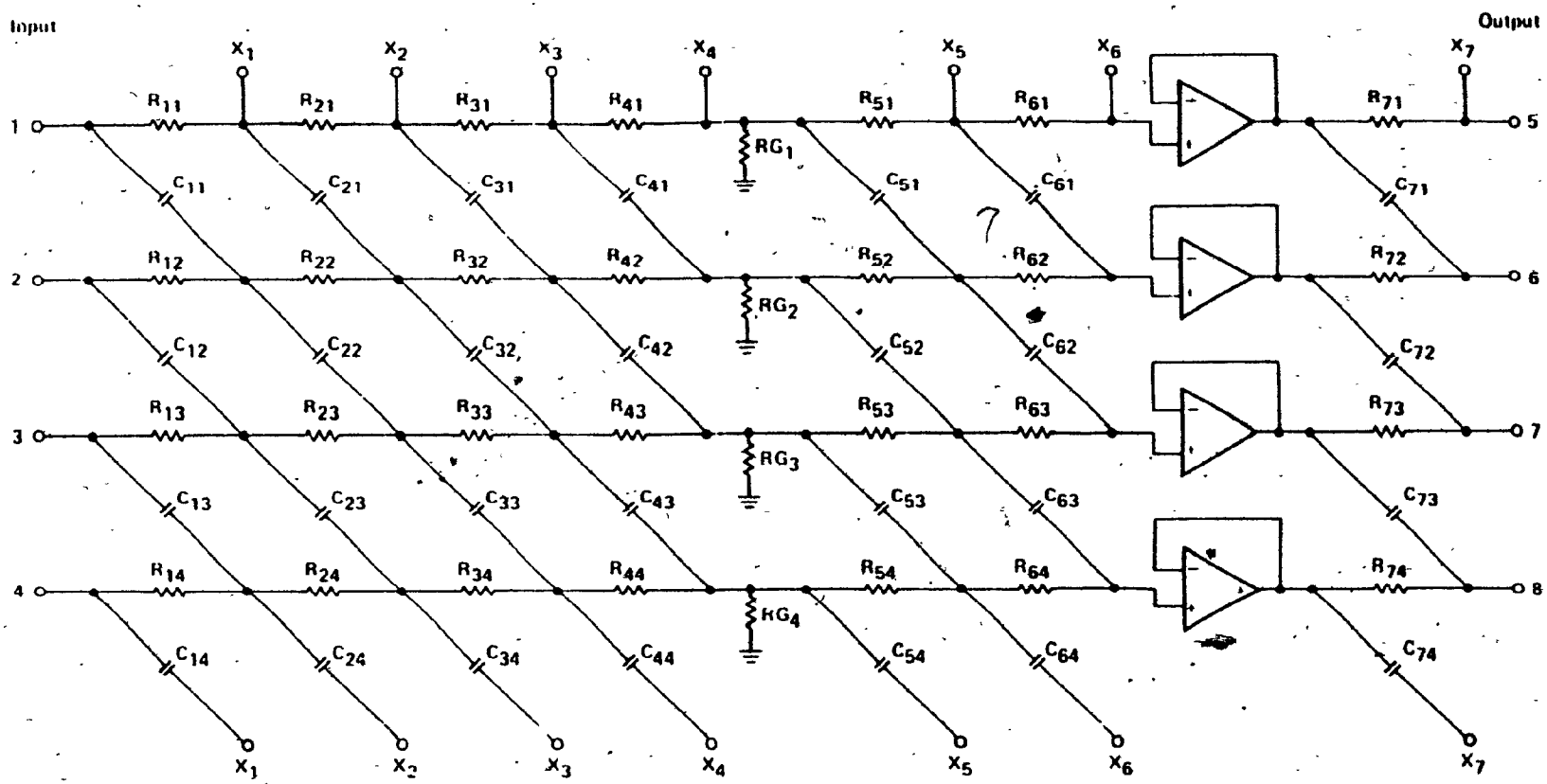
Different strategies were involved in the design and different optimization techniques were used to determine the number of sections required, the location of buffer/buffers and the value and location of the additional resistors to ground.

One of the important strategies was the use of the same capacitor value in all the stages which ensures high yield in the assembly of the sequence discriminator and a lower parts cost. In this way, the resistor ratio of the sequence discriminator was reduced from 24.8 (1) to 11.3 which reduces the number of different inks for thick-film design.

The compromise design has close to 100% yield in the transmit path and approximately 60% yield in the receive path, which means that the overall yield is 100%.

The sequence discriminator was first built using discrete components in the development stage. Now it is in production using thick-film technology on a 1" x 2.5" substrate.

Figure 7 shows the discrete SD as well as the thick-film SD.



All Capacitors are 2 2 nf

Resistors (in Kilo-Ohms)

R_1	114 2238	R_5 =	20 1095
R_2	78 5707	R_6 =	226 3894
R_3	24 7573	R_7 =	42 4017
R_4	36 8923	RG =	35 5035

Figure 5 Seven Stage Buffered Sequence Discriminator (S D)

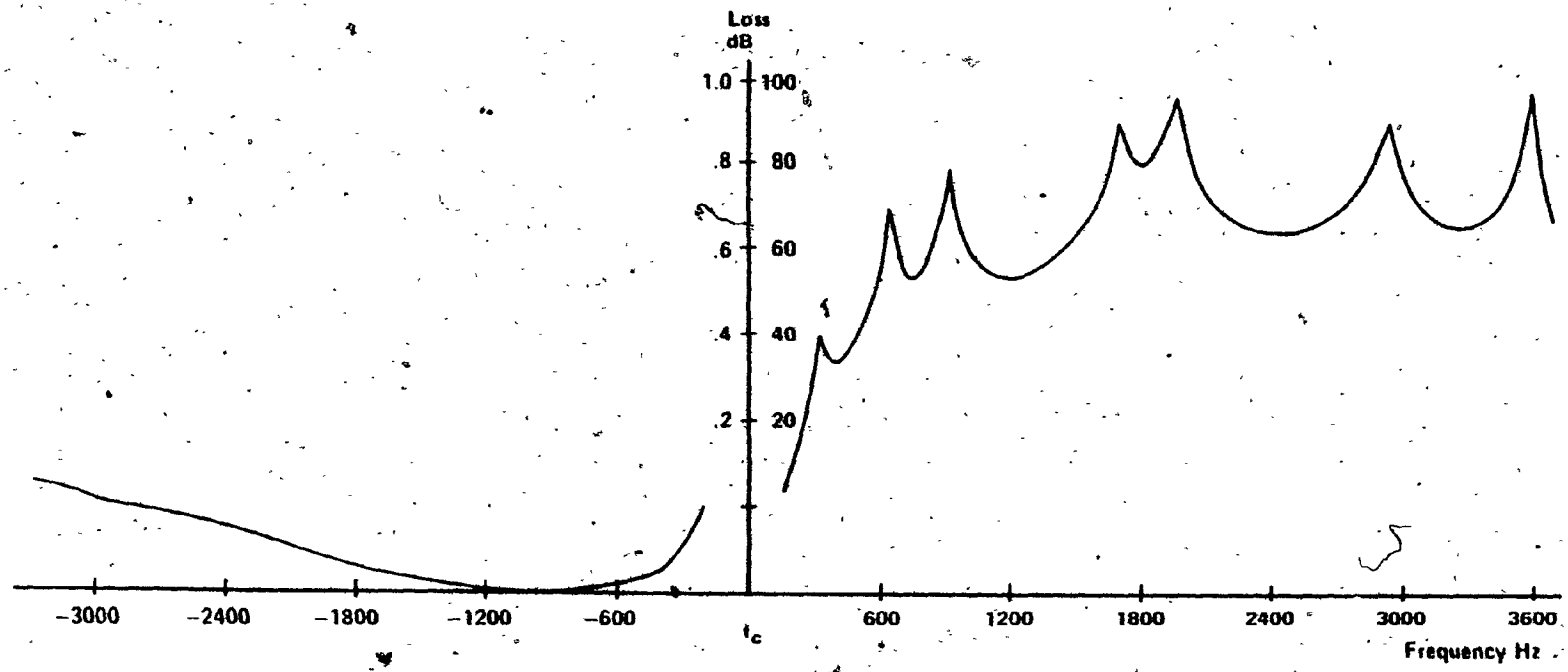


Figure 6 Nominal Response of the Seven Stage Buffered Sequency Discriminator

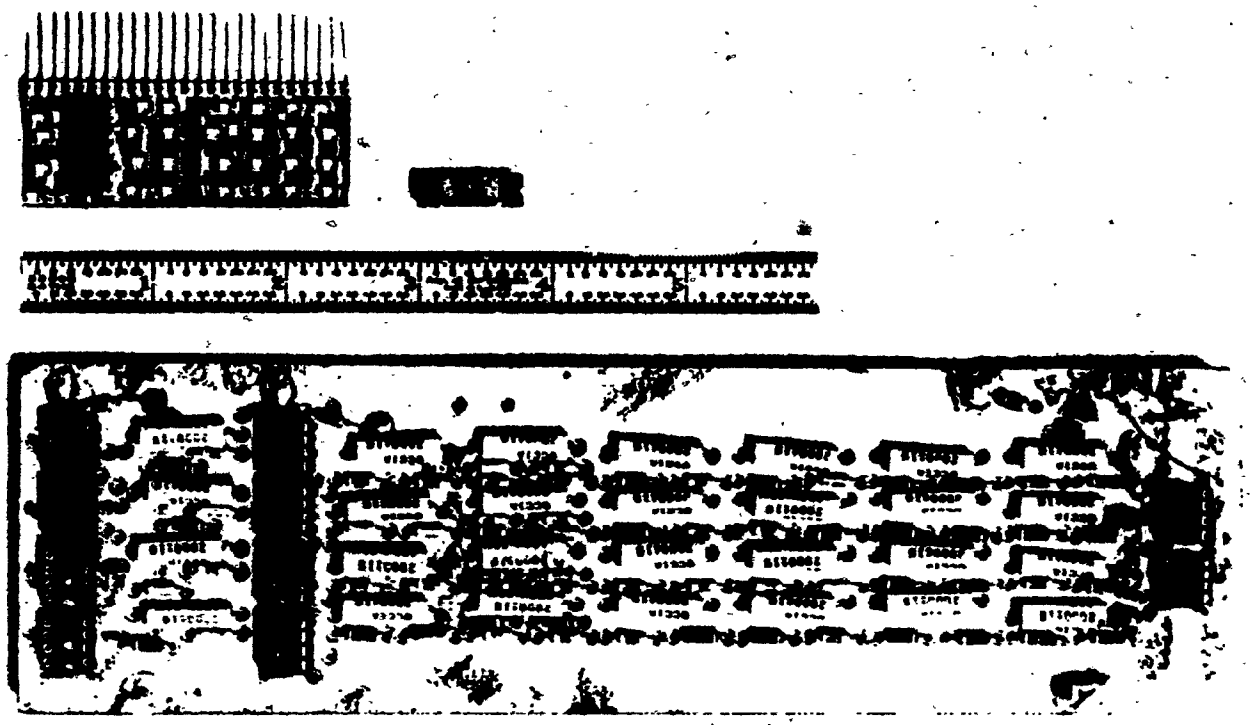


Figure 7: Seven Stage Buffered Poly-Phase Network
Thick Film S–D and Modem (top)
Discrete S–D (bottom)

Chapter 3

SENSITIVITY* ANALYSIS

CHAPTER 3

SENSITIVITY ANALYSIS

Consider a sequence discriminator (SD) used as a transmit phase shift network, where the modulator is connected to the output of the SD .

Disturbance signals occurring at the input of the SD will be highly attenuated, since they pass through all the sections of the SD. Disturbance signals occuring at later stages will have less attenuation since they pass through fewer sections of the SD. If the tolerances in the components were treated as disturbance signals, we can conclude that the response is more sensitive to the components, which are close to the output.

If two buffered sequence discriminator sections were used as a transmit phase shift network, the sensitivity of the last two stages of the first SD section may differ from the rule in some frequency bands. Figures 8 and 9 show the effect of ±10% variation in the resistors and capacitors for the seven-stage buffered design, in which only components for stages 7, 6, 5 and 4 are shown, while components for stages 3, 2 and 1 are not shown because they did not show significant variation from the nominal response.

The foregoing result is very important; it can be used in simplifying the trimming procedure. For those stages with low sensitivity we do not need to use tighter tolerance capacitors and do not need to accurately trim the resistors.

Figures 10 and 11 show the effect of 10% variation in the resistors and capacitors if the same SD is used as a receive SD.

Note in this case that the first stages are the most sensitive ones (the stages close to the demodulator). In these curves only components for stages 1, 2, 3 and 4 are shown while components for stages 5, 6 and 7 are not shown because they did not show significant variation from the nominal response.

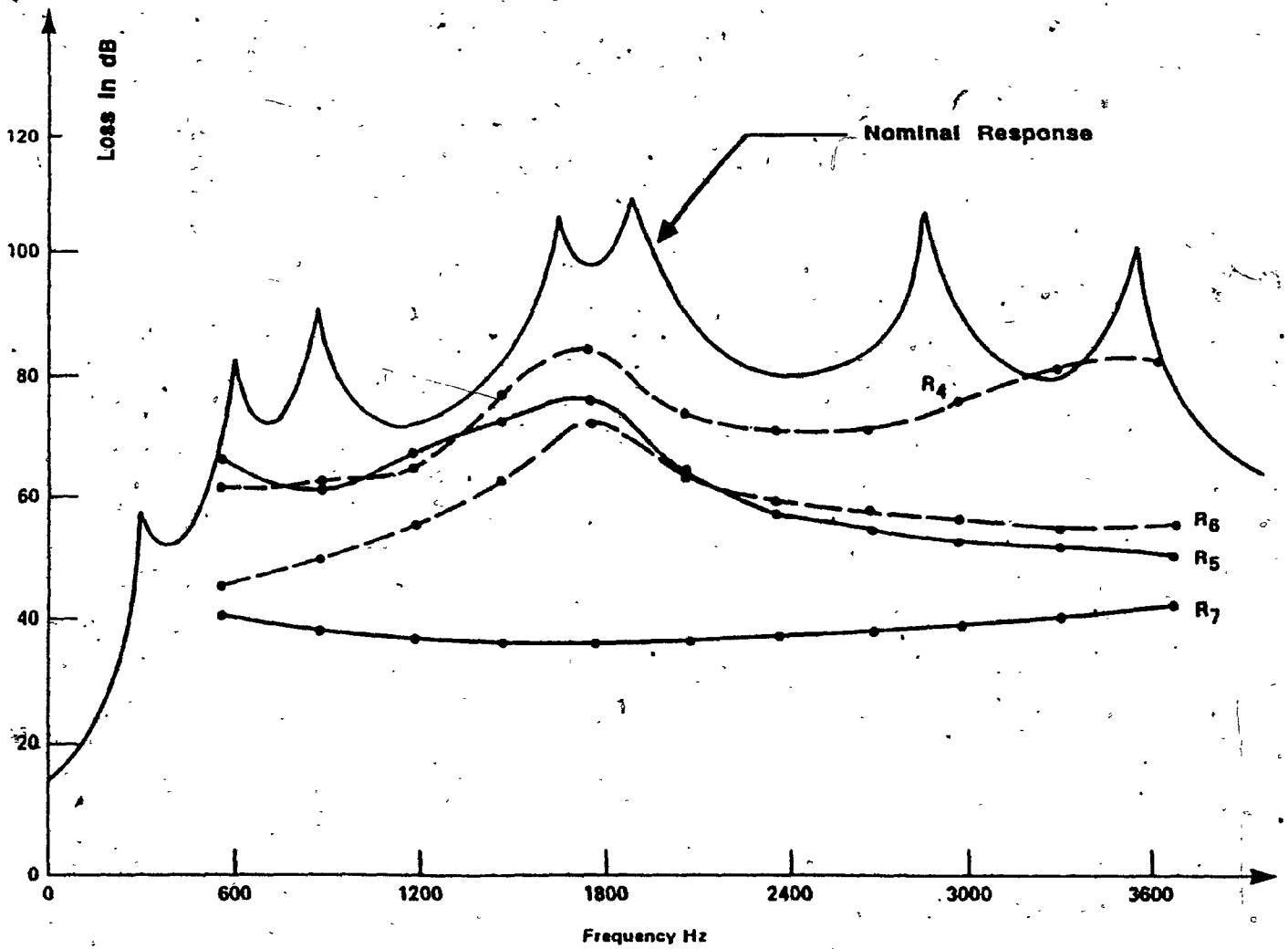


Figure 8. Effect of ±10% Variation in the Resistors on the response of the Seven Stage Buffered Polyphase Network

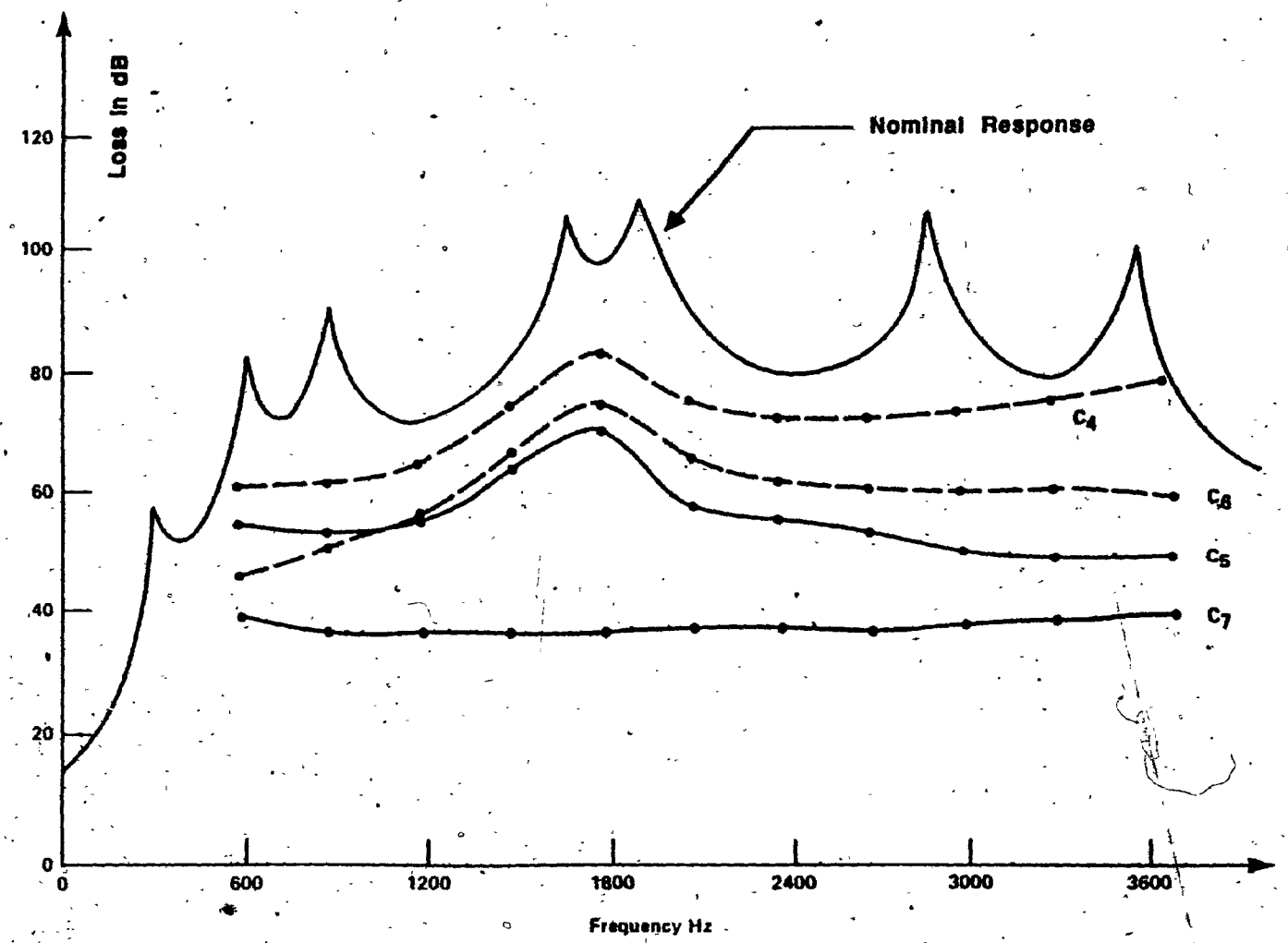


Figure 9. Effect of ±10% Variation in the Capacitors on the response of the Seven Stage Buffered Polyphase Network

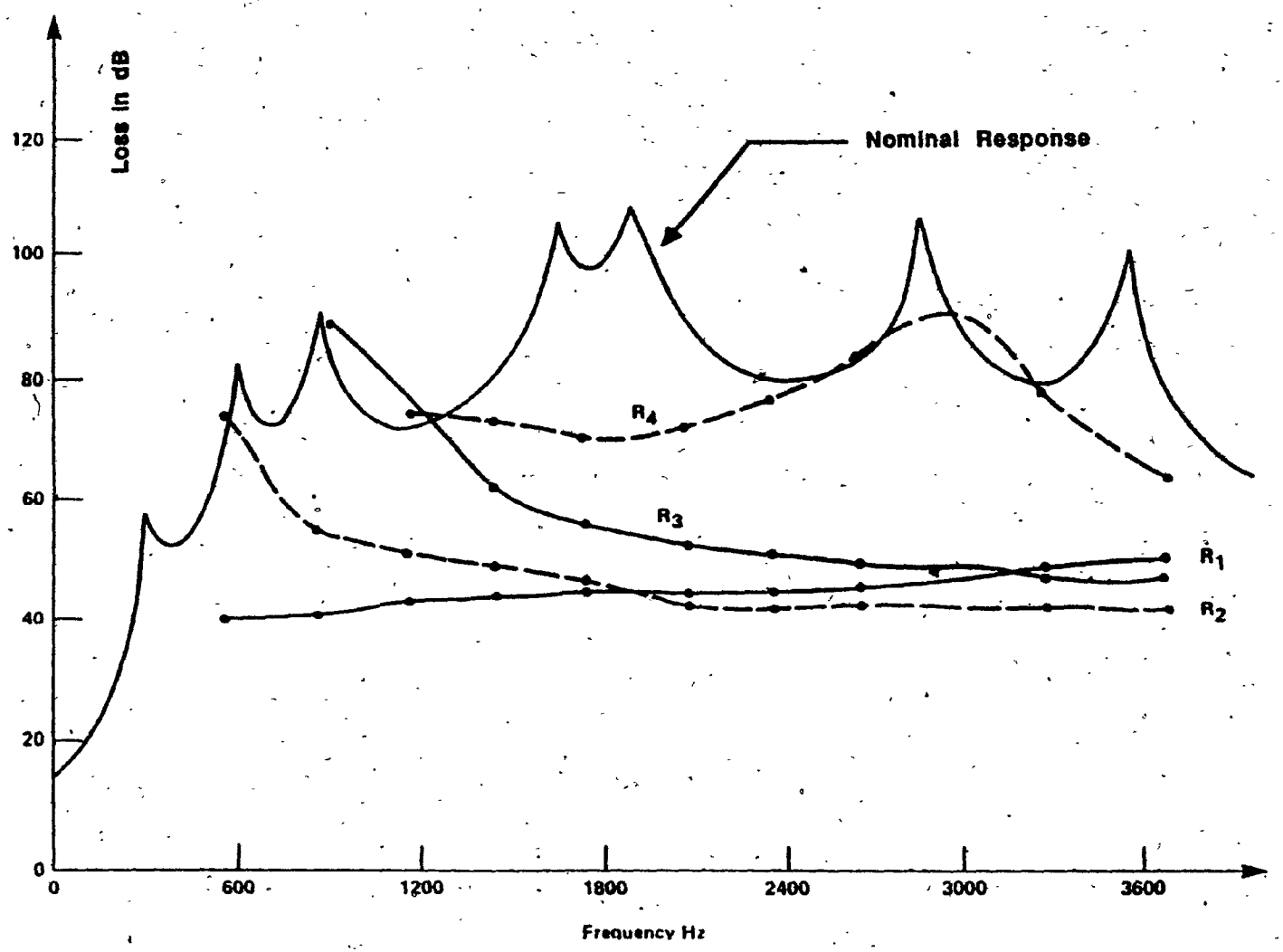


Figure 10. Effect of ±10% Variation in the Resistors on the response of the Seven Stage Buffered Polyphase Network Used in the Receive Path

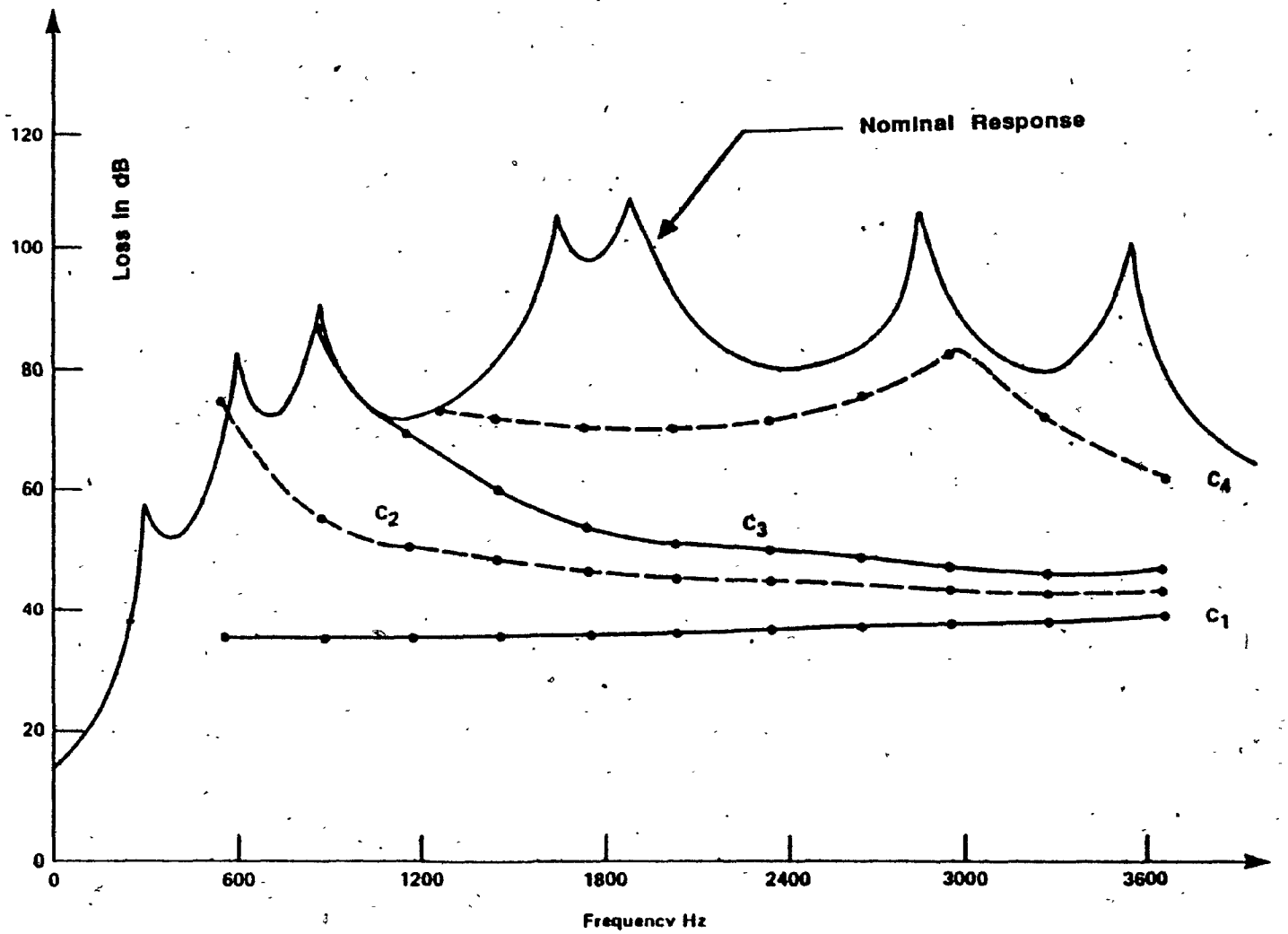


Figure 11. Effect of ±10% Variation in the Capacitors on the response of the Seven Stage Buffered Polyphase Network Used in the Receive Path

CHAPTER 4

TRIMMING PROCEDURE

In the thick-film design, capacitors with certain tolerances are used and the resistors are trimmed to compensate for the effect of these capacitor tolerances. The larger the allowable tolerances in the capacitors, the more accurate the trimming procedure must be. The opposite is also true, i.e., if an accurate trimming procedure is developed, it will allow wider tolerance capacitors to be used.

In any polyphase design, each stage consists of a number of capacitors and a number of resistors (in our case four capacitors and four resistors). The known method of trimming such an arrangement (1) is to measure the capacitors, find their average value, calculate the corresponding resistor value from the resonant frequency of the stage, and then trim all the resistors in that stage to the calculated value. This is repeated in all the stages.

This method of trimming can be applied where the rejection required is not very high, it will limit the capacitor tolerances to ±0.2% (1) for a 57 dB out-of-band rejection.

Chapter 4

TRIMMING PROCEDURE

4.1 Trimming Single-Stage Polyphase Networks

The invented method of trimming is based on the chain matrix, also known as the ABCD matrix of a single-stage polyphase network. The derivation of the ABCD matrix for both the positive and the negative sequence in terms of resistor and capacitor values is carried out.

All capacitors of the single-stage polyphase network have the same nominal value. However, the ABCD matrix is derived assuming non-equal values for both the capacitors and the resistors. This will help us to understand the interaction of each component and it will simulate the real world, since components are always associated with tolerances. In our case of four phases, assume that the resistors are R1, R2, R3 and R4 and the capacitors are C1, C2, C3 and C4 as shown in Figure 12. Appendix 3 shows the derivation of the ABCD matrix for both the positive and the negative sequences with input node 1 and output node 5, as an example. Other matrices can be derived in a similar manner. If nodes 1, 2, 3 and 4 are the input nodes, while nodes 5, 6, 7 and 8 are the output nodes, four ABCD matrices for the positive sequence and four ABCD matrices for the negative sequence can be written as follows:

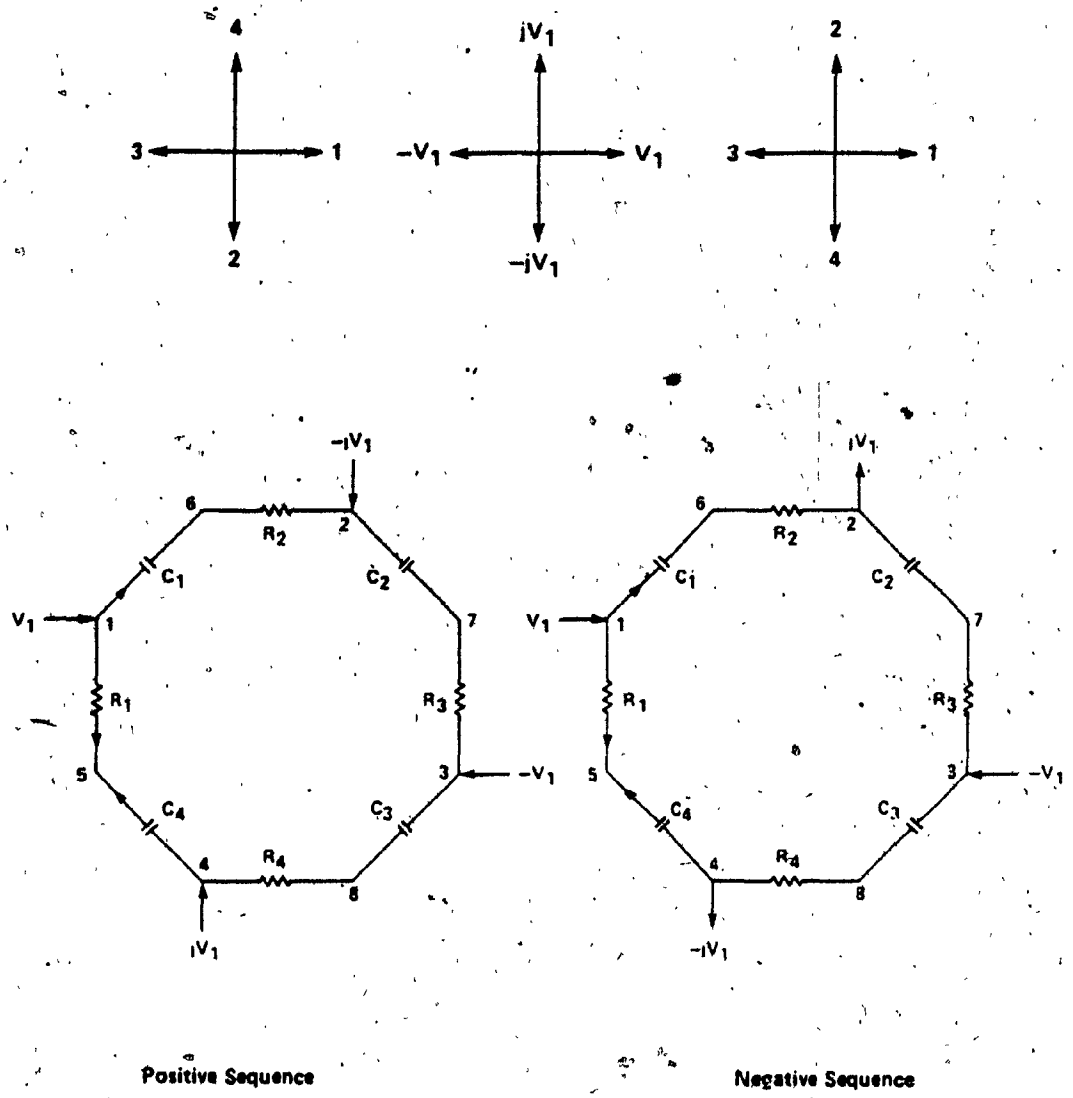


Figure 12: Derivation of the ABCD Matrices For the Single Stage Four-Phase S.D.

$$\begin{bmatrix} A_{51} & B_{51} \\ C_{51} & D_{51} \end{bmatrix}_{Pos} = \frac{1}{(1-wC_4R_1)} \begin{bmatrix} 1+jwC_4R_1 & R_1 \\ wC_4(j+1)+wC_1(j-1) & 1+j\,wC_1R_1 \end{bmatrix} \qquad (4-1)$$

$$\begin{bmatrix} A_{62} & B_{62} \\ C_{62} & D_{62} \end{bmatrix}_{Pos} = \frac{1}{(1-wC_1R_2)} \begin{bmatrix} 1+jwC_1R_2 & R_2 \\ wC_1(j+1)+wC_2(j-1) & 1+jwC_1R_1 \end{bmatrix} \qquad (4-2)$$

$$\begin{bmatrix} A_{73} & B_{73} \\ C_{73} & D_{73} \end{bmatrix}_{Pos} = \frac{1}{(1-wC_2R_3)} \begin{bmatrix} 1+jwC_2R_3 & R_3 \\ wC_2(j+1)+wC_3(j-1) & 1+jwC_1R_1 \end{bmatrix} \qquad (4-3)$$

$$\begin{bmatrix} A_{84} & B_{84} \\ C_{84} & D_{84} \end{bmatrix}_{Pos} = \frac{1}{(1-wC_3R_4)} \begin{bmatrix} 1+jwC_3R_4 & R_4 \\ wC_3(j+1)+wC_4(j-1) & 1+jwC_1R_1 \end{bmatrix} \qquad (4-4)$$

$$\begin{bmatrix} A_{51} & B_{51} \\ C_{51} & D_{51} \end{bmatrix}_{Neg} = \frac{1}{(1+wC_4R_1)} \begin{bmatrix} 1+jwC_4R_1 & R_1 \\ wC_4(j+1)+wC_1(j-1) & 1+jwC_1R_1 \end{bmatrix} \qquad (4-5)$$

$$\begin{bmatrix} A_{62} & B_{62} \\ C_{62} & D_{62} \end{bmatrix}_{Neg} = \frac{1}{(1+wC_1R_2)} \begin{bmatrix} 1+jwC_1R_2 & R_2 \\ wC_1(j+1)+wC_2(j-1) & 1+jwC_1R_1 \end{bmatrix} \qquad (4-6)$$

$$\begin{bmatrix} A_{73} & B_{73} \\ C_{73} & D_{73} \end{bmatrix}_{Neg} = \frac{1}{(1+wC_2R_3)} \begin{bmatrix} 1+jwC_2R_3 & R_3 \\ wC_2(j+1)+wC_3(j-1) & 1+jwC_1R_1 \end{bmatrix} \qquad (4-7)$$

$$\begin{bmatrix} A_{84} & B_{84} \\ C_{84} & D_{84} \end{bmatrix}_{Neg} = \frac{1}{(1+wC_3R_4)} \begin{bmatrix} 1+jwC_3R_4 & R_4 \\ wC_3(j+1)+wC_4(j-1) & 1+jwC_1R_1 \end{bmatrix} \qquad (4-8)$$

If R4 = R3 = R2 = R1

and C4 = C3 = C2 = C1

we have

$$\begin{bmatrix} A_{51} & B_{51} \\ C_{51} & D_{51} \end{bmatrix} = \begin{bmatrix} A_{62} & B_{62} \\ C_{62} & D_{62} \end{bmatrix} = \begin{bmatrix} A_{73} & B_{73} \\ C_{73} & D_{73} \end{bmatrix} = \begin{bmatrix} A_{84} & B_{84} \\ C_{84} & D_{84} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \qquad (4-9)$$

for both the positive and negative sequences where

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Pos} = \frac{1}{(1-wC_1R_1)} \begin{bmatrix} 1+jwC_1R_1 & R_1 \\ 2jwC_1 & 1+jwC_1R_1 \end{bmatrix} \qquad (4-10)$$

and

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Neg} = \frac{1}{(1+wC_1R_1)} \begin{bmatrix} 1+jwC_1R_1 & R_1 \\ 2jwC_1 & 1+jwC_1R_1 \end{bmatrix} \qquad (4-11)$$

Equations (4-10) and (4-11) agree with those derived for the equal components case (1). Equations (4-1) to (4-8) show that the best way to control the pole location is to fix the products R1 C4, R2 C1, R3 C2 and R4 C3 i.e., if R1, R2, R3, R4 and C1, C2, C3, C4 are as shown in Figure 12 which is clockwise numbering, then according to this result the trimming should be in a counterclockwise direction. If the numbering goes from top to bottom as in Figure 5, the trimming should be carried out from bottom to top.

The previous statement does not in any way restrict the sequence of trimming (which resistor to be trimmed first), but it does restrict each resistor to an associated capacitor such that the RC product is fixed.

The foregoing method of trimming resulted in widening the capacitor tolerances to ±1%, from the state of the art of ±0.2%.

4.2 Trimming Wide-Band Polyphase Networks

The previous section shows the method of trimming single-stage polyphase networks. In wide-band polyphase networks, each stage is trimmed in a similar manner to the single-stage case. To optimize the trimming procedure the following steps should be carried out.

a) Sensitivity analysis to find out which stages need to be trimmed and which stages can be left without trimming.

From our previous discussion on sensitivity analysis we can conclude that if the filter is used in the transmit mode, stages 4, 5, 6 and 7 need to be trimmed; if it is used in the receive mode, stages 1, 2, 3 and 4 need to be trimmed; however, if it is used for both transmit and receive modes, all the stages must be trimmed.

Note that the exclusion of some of the stages from trimming cannot be applied to the compromise design, since it is not an optimum design for both transmit and receive modes. If two different designs were developed, we would be able to trim fewer sections in each design. The foregoing procedures have been successfully applied to our design, resulting in the use of ±1% capacitor tolerances.

The advantages of changing capacitor tolerance in each stage were studied. The cost reduction was not enough to compensate for the extra cost associated with more codes and lower quantities for components.

The measuring and trimming inaccuracies, temperature, humidity effects and aging have all contributed to the limitation of the capacitor tolerances to ±1%. It is to be noted that even with a successful functional trimming procedure, which could be investigated, some of these effects such as the temperature, humidity and aging effects, will still be there.

There is still a possibility in the future to relax the capacitor tolerances, if we can have more control or improve the effect of the other factors. It is of some importance to mention that, with relaxed out-of-band rejection, there is always room for relaxed capacitor tolerances.

b) Few runs have to be performed using the laser trimming process to determine the optimum value of the grounded resistors, so that the in-band ripple is minimized. The modified value can be slightly different from the design value due to parasitic effects not included in the simulation.

c) The sequence in which the stages are trimmed can be optimized based on their sensitivity as well as their relative position on the layout. It is important to trim the resistors on a stage by stage basis; row by row trimming may result in an intolerable drift in some of the stages.

d) One possible way to partially offset trimming inaccuracies in each stage is to trim the first resistor, measure it and find out the percentage deviation from its calculated value, then use this percentage to modify the calculated value of the other resistors in the stage and trim these resistors to their modified value.

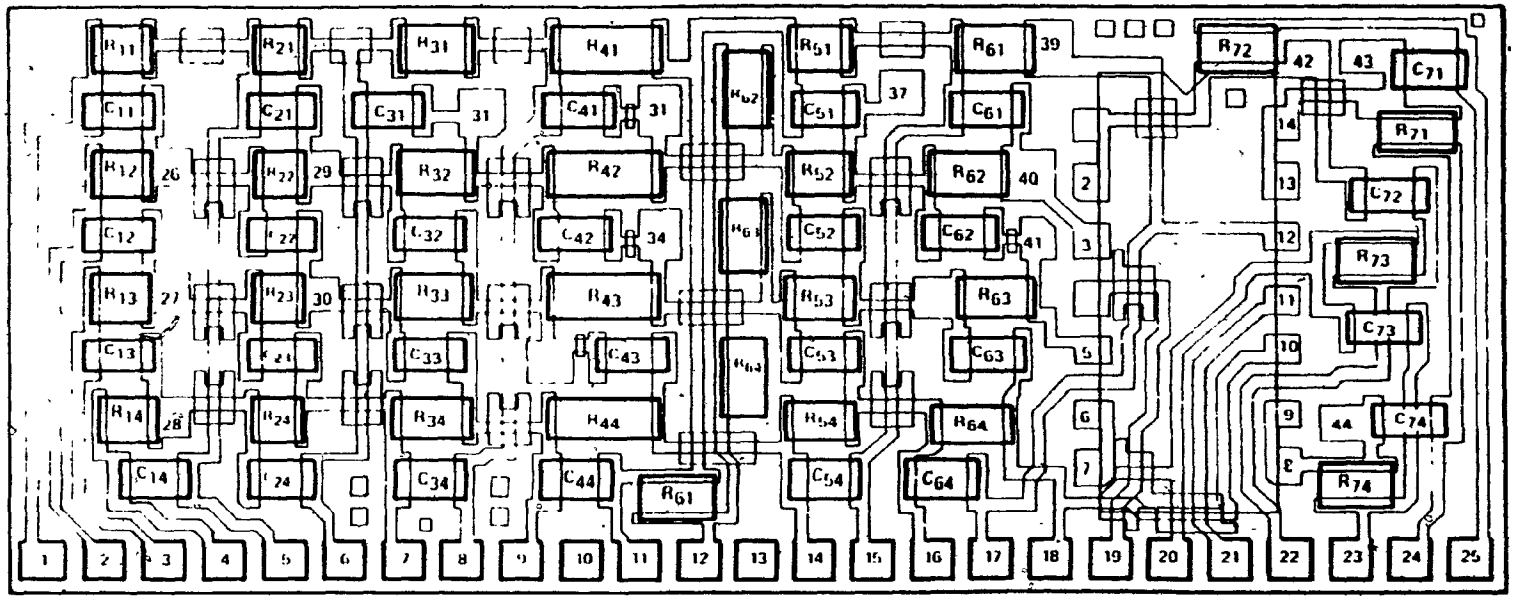


Figure 13. Layout of Seven Stage Buffered Polyphase Network

Chapter 5

SINGLE SIDE BAND MODEM DESIGN

CHAPTER 5

SINGLE SIDE-BAND MODEM DESIGN

The sequence discriminator technique in image rejection modulation and demodulation depends on the existence of a precise four-phase modem.

Figure 14 shows the circuit diagram of the whole scheme. At the input of the transmit SD, an inverted signal is derived from the input signal and both the input signal and the derived signal are fed to the transmit SD, the output of which is connected to the modulator through a buffer arrangement.

In the receive direction, the demodulator is connected to the receive SD either directly or through a buffering arrangement, two of the receive SD outputs are fed to the output through another buffer arrangement.

In our design a four phase modem was implemented in a 16 pin dual-in-line ceramic package using a metal gate MC-Series gate array, this package includes the four phase carrier generator, the four phase switched modulator and the four phase switched demodulator.

Figure 15 shows the G39 Modem Circuit diagram. Figure 16 shows the Block diagram and Pin configuration. Table 1 shows the pin description. Two important factors have been taken into account in the design of the modem:

a) The Switch On resistance.

b) The timing of the pulses.

5.1 Effect of On Resistance of the Switches

The On resistance of the series switches is not critical for the transmit side since the SD is buffered from the modulator.

In the receive direction the main concern is to present the receive SD with four equal signals which are equally spaced in phase, if the On resistance tolerance causes these four signals to be disturbed, it will cause the out-of-band rejection of the receive SD to drop. These resistors are in series with holding capacitors CR1 to CR4, Figure 14.

The existence of resistors at the input of the receive SD is another reason for concern because in the receive direction, the first stages are the most sensitive.

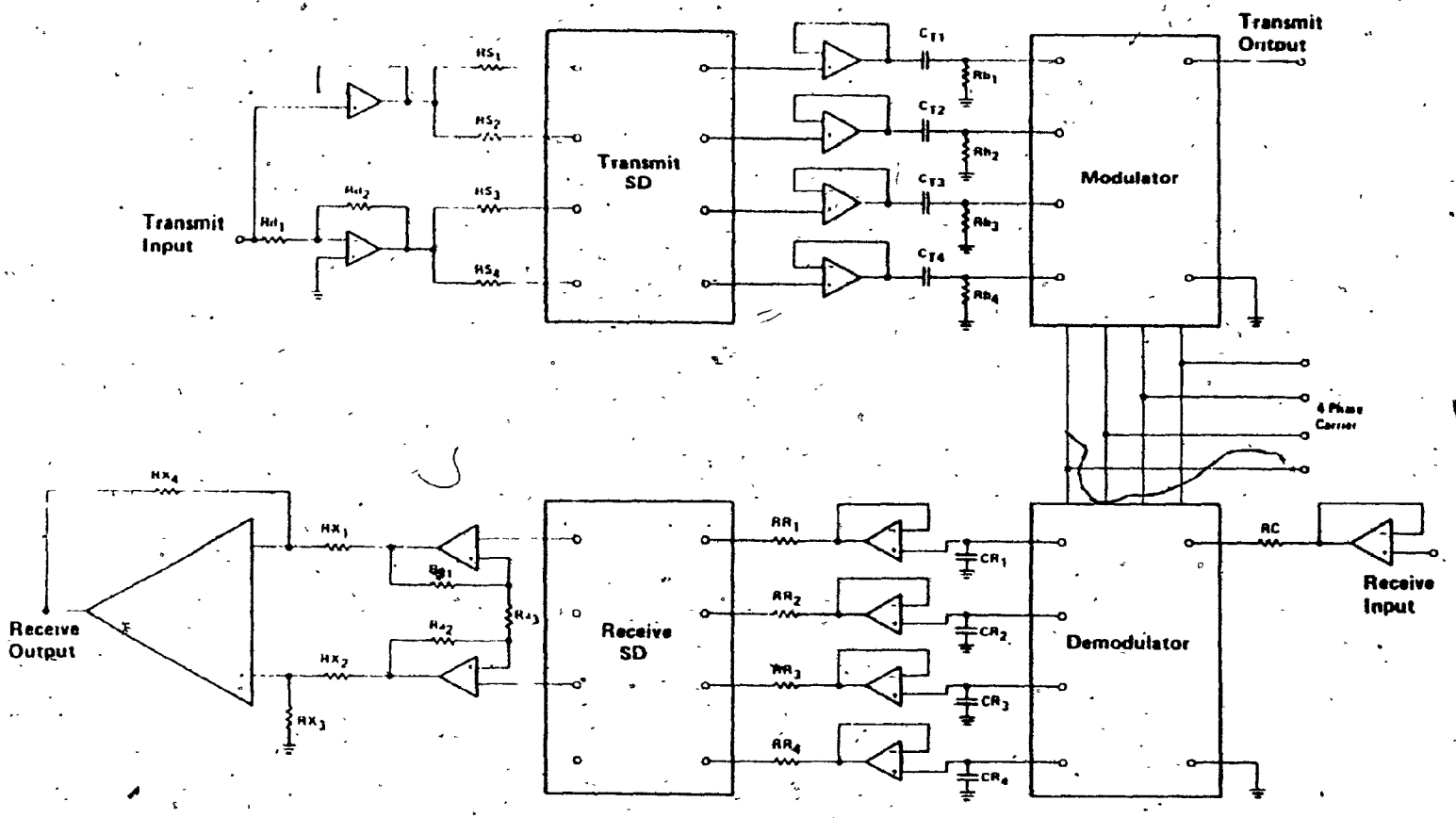


Figure 14 Schematic Diagram of the Poly Phase Network Technique Showing the Connection of the Modem

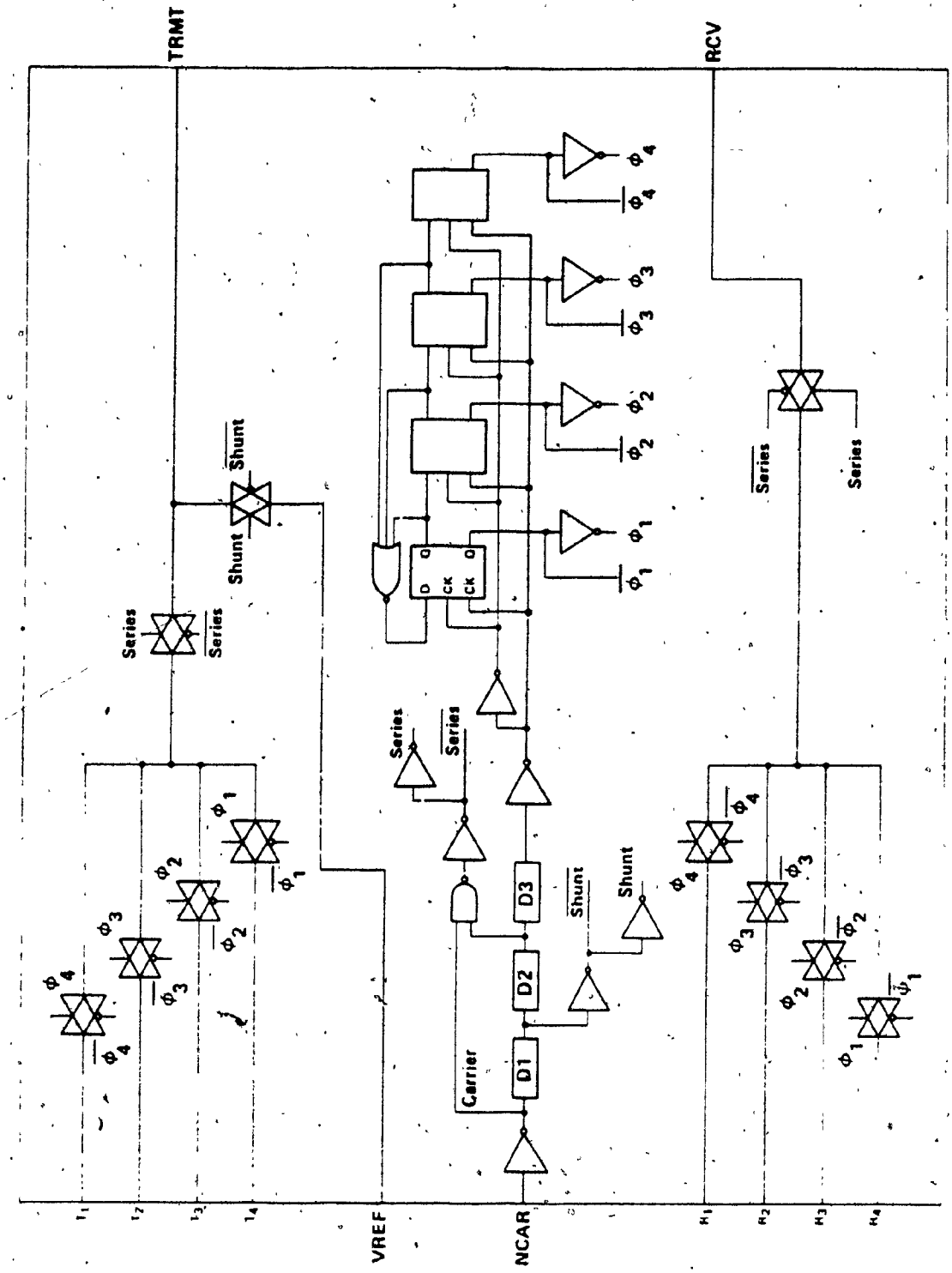


Figure 15 The G39 Modem Circuit Diagram

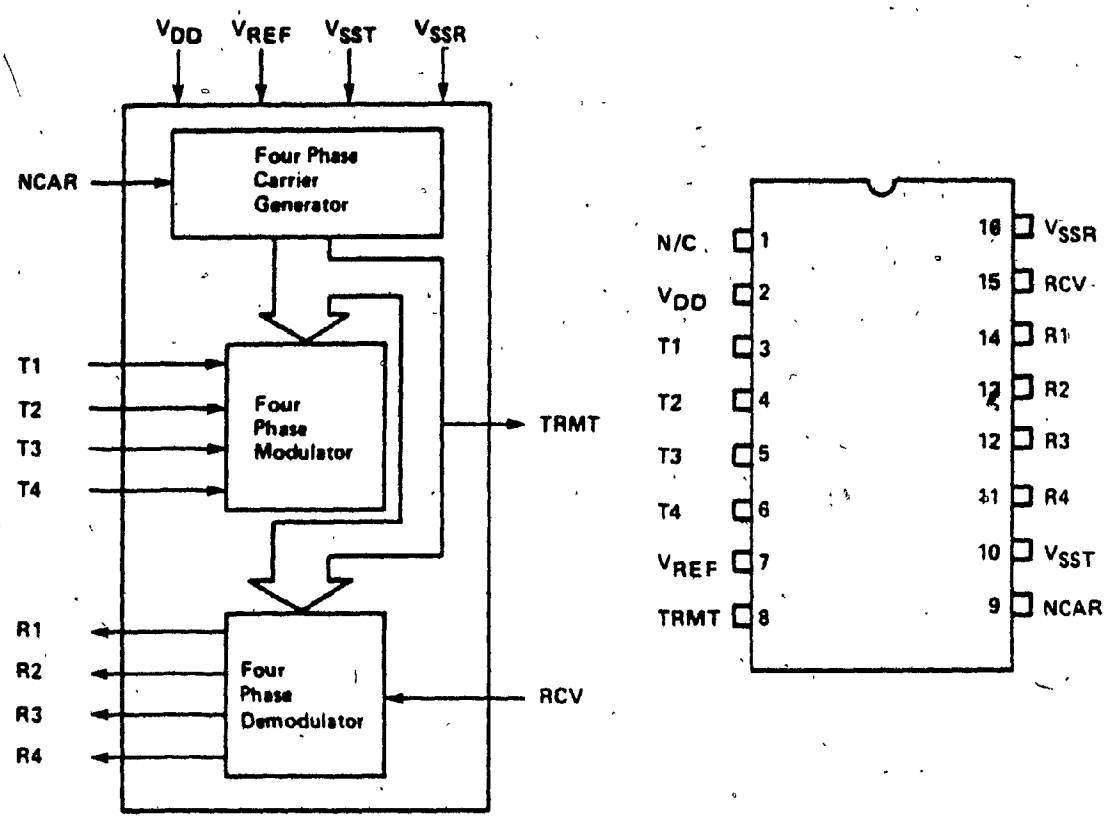


Figure 16 The G39 Modem Block Diagram and Pin Configuration

Table 1 Pin Description of G39 Modem

Number	Symbol	Type	Function
1	n.c.	ns	No connection
2	VDD	I	Positive supply (reference to VSSR or VSST)
3	T1	I	Transmit audio input (limited to = 3.4 KHz) Other transmit inputs have phase referred to T1.
4	T2	I	Transmit audio input. Amplitude same as T1. Phase leads T1 by 90°.
5	T3	I	Transmit audio input. Amplitude same as T1, Phase leads T1 by 180°.
6	T4	I	Transmit audio input. Amplitude same as T1. Phase leads T1 by 270°.
7	VREF	I	Analog ground for analog inputs and outputs. When used with a single supply, this pin must be connected externally to (VSS–VDD)/2.
8	TRMT	0	Transmit modulated output. This is the SSB–SC signal.
9	NCAR	I	Four times carrier frequency input. This signal is divided by four internally to produce the actual carrier frequency about which TRMT is modulated.
10	VSST	I	Transmit channel negative supply. It is separated from VSSR externally only to provide additional transmit to receive channel isolation and decoupling.
11	R4	0	Receive audio output. This signal is derived by "sampling" the RCV input at the carrier frequency and for a duration approximately equal to 1/8 of the carrier period. Phase leads R1 by 270°.
12	R3	0	Receive audio output. Derived same as R4. Phase leads R1 by 180°.
13	R2	0	Receive audio output. Derived same as R4. Phase leads R1 by 90°.
14	R1	0	Receive audio output. Derived same as R4. Phase of other receive outputs referred to R1.
15	RCV	I	Receive SSB–SC input signal. Signal is demodulated to produce the four receive audio outputs.
16	VSSR	I	Receive channel negative supply. See VSST signal description.

Note that absolute tolerances are not as critical as relative tolerances.

To reduce the effect of the on resistance of the series switches, 2 Kohm resistors (RC Figure 14) were added.

5.2 Effect of Modem Timing Error

The high selectivity in the sequence discriminator approach is based on image cancellation. In the ideal modulator where all the modulator inputs are equal in magnitude and equally spaced in phase, the out-of-band rejection will be infinite. In practice there will be a magnitude error and a phase error in these outputs, in addition to phase error resulting from the modulation timing error. All these errors will result in a finite image band rejection.

In the region of high image rejection, the image response can be considered as a small residue vector resulting from the cancellation of two vectors.

Let us examine the relationship of magnitude error δ , and total phase error $\Delta\phi$ to the cancellation factor D; note that image rejection $= -20 \log_{10} D$. The cancellation factor D is the difference

between the error-free unit vector and the vector $(1+\delta)e^{j\Delta\phi}$ and is given by

$$D = |(1+\delta)e^{j\Delta\phi} - 1|$$

$$\therefore D^2 = \left[(1+\delta)\,\mathrm{Cos}\,\Delta\phi - 1\right]^2 + \left[(1+\delta)\,\mathrm{Sin}\,\Delta\phi\right]^2$$

From which we can derive $\Delta\phi$ to be

$$\Delta\phi = 2\,\mathrm{Arc\,Sin}\;0.5\left(\frac{D^2-\delta^2}{1+\delta}\right)^{0.5}$$

Note that $\Delta\phi$ is the total phase error due to both modulator and SD.

The maximum allowable time error ΔT_{max}, which is the total time error including the time error resulting from the SD phase errors, can be found from the equation

$$\Delta T_{max} = \frac{\Delta\phi}{2\pi f_c}$$

where fc is the carrier frequency.

If the filter is to be used for different carrier frequencies, fc should correspond to the highest carrier, since the results should be as good, if not better, for lower carrier frequencies.

In our case the filter will be used in any of the 12 channels with carrier frequencies 64, 68, ..., 108 kHz respectively.

Use 5-5, 5-6 and fc = 108 kHz to yield:

$$\Delta T_{max} = (2.9473E-6)\left[\text{Arc Sin } 0.5\left(\frac{D^2-\delta^2}{1+\delta}\right)^{0.5}\right] \qquad (5-6)$$

In the special case where $\delta = 0$ equations 5-4, 5-6 will reduce to

$$\Delta\phi = 2 \text{ Arc Sin } 0.5\,D \cong D \qquad (5-7)$$

$$\Delta T_{max} = (1.4737E-6)\,D \qquad (5-8)$$

Equation 5-7 shows that the cancellation is mainly determined from the phase error.

Equation 5-8 shows that the maximum allowable time error is ~ 1.47 nanoseconds to achieve 60 dB of cancellation.

Note that ΔT_{max} derived here includes only the polyphase newtwork phase errors, and must be further reduced to allow for magnitude errors and SD phase errors. If the modem is designed with lower value for ΔT_{max}, the performance of the whole system will be improved.

Figure 17 shows the relation between the cancellation factor D and the maximum allowable time error ΔT_{max} for three values of magnitude

errors corresponding to -55, -60, -65, $-\infty$ dB respectively, other curves can be drawn in between.

From these curves, we note that D is always greater than δ, and the smaller the magnitude error δ, the more relaxed ΔT_{max} will be.

5.3 Magnitude and Phase Error Simulation

Table 3 shows the simulation results for the seven-stage polyphase network. The Actual magnitude and phase is compared with the nominal magnitude and phase. The magnitude error is shown to be less than .06 dB. and the phase error is less than 0.1 degrees.

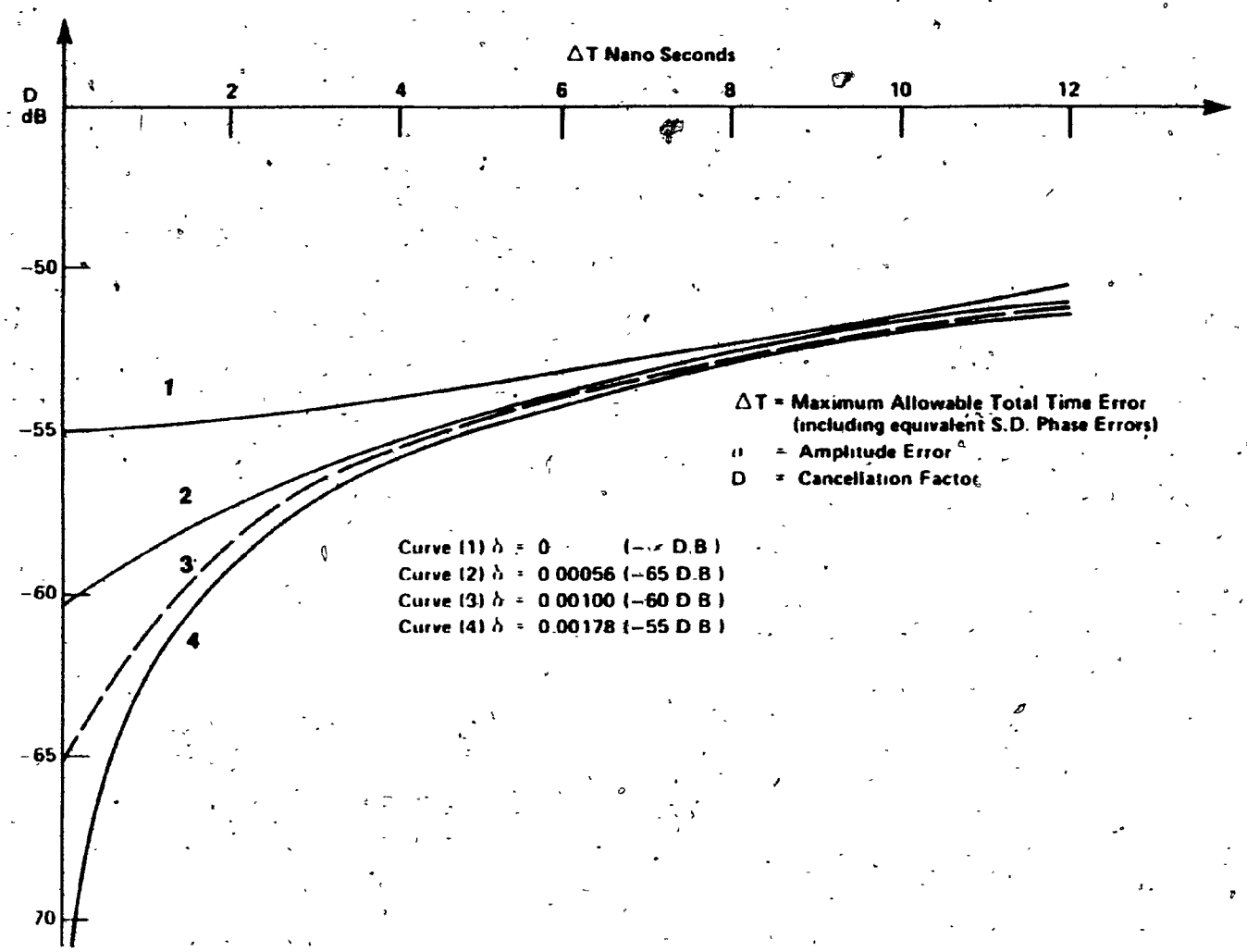


Figure 17 Relation Between Maximum Allowable Time Error and Cancellation Factor for Different Amplitude Errors

Table 2: Magnitude and Phase Error for Seven Stage Polyphase Network

Freq. Hz	Nominal Mag dB	Nominal Phase Degree	Actual Mag dB	Actual Phase Degree	Mag Error dB	Phase Error Degree
-1004.	-2.386	33.507	-2.359	33.745	0.0268	0.2380
0.	0.0	0.0	0.0	0.0	0.0	0.0
160.	-1.787	138.270	-1.781	138.100	0.0061	-.1700
175.	-1.887	146.360	-1.880	146.170	0.0062	-.1900
200.	-2.013	158.640	-2.007	158.140	0.0060	-.2300
400.	-2.272	-134.300	-2.262	-134.670	0.0097	-.3700
600.	-2.303	-91.809	-2.284	-92.184	0.0185	-.3750
800.	-2.348	-59.756	-2.323	-60.073	0.0249	-.3170
1000.	-2.385	-33.974	-2.359	-34.213	0.0268	-.2390
1200.	-2.404	-12.523	-2.379	-12.686	0.0249	-.1630
1400.	-2.403	5.728	-2.383	5.633	0.0203	-.0947
1600.	-2.389	21.514	-2.374	21.476	0.0143	-.0380
1800.	-2.365	35.344	-2.358	35.348	0.0072	-.0040
2000.	-2.336	47.584	-2.337	47.621	-.0001	0.0370
2200.	-2.307	58.512	-2.314	58.572	-.0074	0.0600
2400.	-2.278	68.343	-2.292	68.418	-.0144	0.0750
2600.	-2.251	77.246	-2.272	77.330	-.0209	0.0840
2800.	-2.227	85.359	-2.254	85.445	-.0271	0.0860
3000.	-2.207	92.791	-2.240	92.877	-.0327	0.0860
3200.	-2.190	99.636	-2.228	99.718	-.0378	0.0820
3400.	-2.177	105.970	-2.219	106.040	-.0425	0.0700
3600.	-2.166	111.850	-2.213	111.920	-.0467	0.0700
3800.	-2.158	117.350	-2.209	117.400	-.0505	0.0500
4000.	-2.153	122.490	-2.207	122.540	-.0538	0.0500

Chapter 6

TEMPERATURE AND HUMIDITY EFFECTS

CHAPTER 6

TEMPERATURE AND HUMIDITY EFFECTS

6.1 Temperature Effects

The existing design of the polyphase network should meet 60 dB image band rejection at any temperature between zero and 50°C.

The effect of temperature has been simulated based on the following assumptions:

a) Capacitors of the type COG-NPO Chip Ceramic which have a temperature coefficient of ±30 ppm/°C.

b) Thick film resistors using the DuPont 1600 series type ink with temperature coefficient of ±50 ppm/°C.

c) The analysis is based on the fact that the circuit is trimmed according to the proper trimming algorithm to compensate for the component tolerances and part of the manufacturing measuring and trimming inaccuracies.

The results of the simulation were as follows:

1) If all the capacitors change in one direction, or if all the resistors change in one direction, the effect is insignificant both in the in-band and in the image band of the network.

2) If the capacitors in each stage change in one direction or if the resistor in each stage change in one direction, the effect will still be insignificant both in the pass-band and in the image band of the network.

3) If the capacitors and the resistors vary in a random fashion within the given temperature coefficient, a degradation of approximately 1 dB will result in the image band.

4) If, in addition to the effect of temperature variation, a drift component is added to the capacitors and the resistors with a relative value of ±0.1%, the degradation in the image band will be approximately 2 dB.

The above results suggest a manufacturing specification of 62 dB to accommodate the temperature and drift effects, and meet 60 dB image rejection specification.

6.2 Humidity Effects

Humidity is simulated by a resistor across each capacitor (RC), the higher the humidity, the lower the value of this resistor.

Table 4 shows the effect of humidity on the pass-band of the filter, while Table 5 shows the effect of humidity on the stop-band of the filter. Both tables were derived for different values of RC from 1 Mohm to 10 Mohms. It is clear from these tables that humidity will have a significant effect for values of RC less than 10 Mohms. Thick-film manufacturing believe that they can meet higher RC values.

Statistical analysis (shown in next chapter) confirmed that RC of as low as 8 Mohms ±50% across the capacitors of the filter will meet the requirements.

Table 3 Effect of Humidity on the In–Band of the Poly Phase Network

Frequency Hz	No Moisture	RC = 1MΩ	2MΩ	3MΩ	4MΩ	6MΩ	10MΩ
−1.000D+00	−7.41066	−8.63812	−8.02515	−7.82042	−7.71801	−7.61557	−7.53361
−500000.	−10.0499	−11.2772	−10.6643	−10.4596	−10.3572	−10.2548	−10.1728
−100000.	−10.3425	−11.5662	−10.9551	−10.7510	−10.6489	−10.5468	−10.4650
−4000.00	−.127430	−1.11397	−.621502	−.456922	−.374581	−.292214	−.226306
−3850.00	−9.317D-02	−1.06685	−.580819	−.418382	−.337111	−.255814	−.190763
−3800.00	−8.226D-02	−1.05140	−.567642	−.405961	−.325069	−.244150	−.179401
−3650.00	−5.121D-02	−1.00588	−.529359	−.370090	−.290402	−.210689	−.146903
−3600.00	−4.145D-02	−.990992	−.517038	−.358623	−.279362	−.200076	−.136631
−3600.00	−5.642D-03	−.932992	−.470142	−.315426	−.238014	−.160575	−9.861D-02
−3200.00	2.448D-02	−.877582	−.427385	−.276883	−.201578	−.126246	−6.596D-02
−3000.00	4.823D-02	−.824821	−.389131	−.243464	−.170575	−9.766D-02	−3.931D-02
−2800.00	6.501D-02	−.774557	−.355614	−.215529	−.145431	−7.530D-02	−1.919D-02
−2600.00	7.431D-02	−.726301	−.326830	−.193238	−.126387	−5.951D-02	−5.966D-03
−2400.00	7.591D-02	−.679045	−.302392	−.176412	−.113368	−5.030D-02	1.800D-04
−2200.00	6.998D-02	−.631004	−.281316	−.164336	−.105793	−4.722D-02	−3.496D-04
−2000.00	5.733D-02	−.579249	−.261722	−.155483	−.102314	−4.912D-02	−6.546D-03
−1800.00	3.971D-02	−.519199	−.240442	−.147159	−.100472	−5.376D-02	−1.638D-02
−1600.00	2.011D-02	−.443928	−.212510	−.135055	−9.629D-02	−5.750D-02	−2.646D-02
−1400.00	3.009D-03	−.343236	−.170574	−.112775	−8.385D-02	−5.490D-02	−3.174D-02
−1200.00	−5.725D-03	−.202359	−.104310	−7.148D-02	−5.505D-02	−3.861D-02	−2.546D-02
−1000.00	.0	.0	.0	.0	.0	.0	.0
−800.000	2.267D-02	.295843	.159708	.114069	9.123D-02	6.838D-02	5.009D-02
−600.000	5.206D-02	.742163	.398932	.283492	.225670	.167809	.121506
−400.000	5.924D-02	1.49306	.785802	.545048	.424025	.302666	.205387
−300.000	6.714D-02	2.14111	1.12958	.779855	.603136	.425350	.282446
−250.000	9.980D-02	2.61221	1.39859	.973594	.757858	.540186	.364780
−200.000	.193006	3.25000	1.79400	1.27481	1.00948	.740574	.523035
−175.000	.284222	3.65775	2.06592	1.49168	1.19688	.897211	.654122
−170.000	.307857	3.74819	2.12821	1.54233	1.24125	.934988	.686394
−160.000	.361807	3.93903	2.26198	1.65223	1.33820	1.01831	.758304
−100.000	.974419	5.43037	3.40877	2.64539	2.24589	1.83430	1.49623
−80.0000	1.35539	6.09473	3.97177	3.15888	2.73082	2.28780	1.92236
−30.0000	3.00761	8.24425	5.96645	5.06659	4.58606	4.08359	3.66497
.0	4.66498	9.92747	7.66405	6.75847	6.27251	5.76265	5.33654
Reference	5.06204	6.28955	5.67656	5.47182	5.36940	5.26696	5.78500

RC = Resistance across each capacitor in the S D

Table 4. Effort of Humidity on the Image-Band of the Polyphase Network

F Hz	No Moisture	1MΩ	2MΩ	3MΩ	4MΩ	6MΩ	10MΩ
0	4 66498	9 92747	7 66405	6 75847	6 27251	5 76265	5.33654
1 00000	4 73028	9 98912	7 72787	6.82286	6 33715	5 82752	5.40159
100 000	14 1980	17 8995	16 3507	15 7048	15 3554	14 9880	14 6808
175 000	24 4362	26 1173	25 6255	25 3166	25 1303	24 9217	24.7386
200 000	28 4501	29 2514	29 2711	29 1100	28 9892	28 8396	28.6985
300 000	55 8561	42 3823	47 7735	50 4966	52 1048	53.8003	55.0241
400 000	51 0838	47 0371	49 6323	50 3214	50 6008	50 8261	50.9621
500 000	56 6659	50 3125	53 4018	54 5678	55 1527	55 7170	56 1359
600 000	73 2710	54 6347	59 7067	62 5296	64.3997	66 7587	69.1339
700 000	71 8047	58 7989	64 9979	68 5855	70 7977	72.8497	73 4802
800 000	72 1537	62 2378	68 8404	72 2751	73 8765	74 5767	74.0861
1000 00	79 7655	64 8984	69 7121	72 1074	73 5785	75 3052	76.9184
1200 00	73 2734	66 9957	69 8699	70 9508	71 5145	72 0918	72.5615
1400 00	78 9541	73 5550	76 3415	77 2485	77 6920	78.1259	78.4645
1600 00	95 0622	82 7306	89 2475	91 6233	92 7450	93 7423	94.3982
1800 00	82 6651	76 3614	79 5235	80 6119	81 1505	81.6780	82 0865
2000 00	86 6460	75 8851	80 4467	82 3829	83 4380	84.5338	85 4140
2200 00	91 0271	77 6442	84 4014	87 8752	89 8142	91 4572	92 0021
2400 00	79 3563	77 6422	79 9446	80 1139	80.0475	79 8898	79 7069
2600 00	75 8904	76 0135	76 5076	76 4037	76 3090	76 1898	76.0789
2800 00	75 3365	75 8581	75 8696	75 3090	75 6540	75 5577	75.4734
3000 00	77 1201	77 9838	77 7293	77.5547	77 4553	77.3491	77.2599
3200 00	82 2569	84 2338	83 4084	83 0413	82 8494	82 6539	82.4958
3300 00	87 8221	91 9171	90 1950	89 3965	88 9944	88.5963	88.2826
3400 00	106 981	93 9124	102 206	108.091	112.788	115.624	112 118
3600 00	85 3670	82 3185	83 7854	84 2977	84 5590	84.8241	85.0391
3700 00	83 1705	80 7771	81 9832	82 3807	82 3807	82.5788	82.9341
3800 00	82 9388	80 7202	81 9010	82 2638	82 4389	82.6098	82.7434
4000 00	93 6154	85 9071	90 3195	91 7955	92 4476	92.9932	93.3261
5000 00	53 7047	52 5085	53 1137	53 3124	53 4111	53 5094	53 5878
6000 00	41 2741	40 1231	40 7005	40 8922	40.9879	41 0834	41.1598
7000 00	33 7650	32 6137	33 1900	33 3819	33 4777	33.5736	33.6502
8000 00	28 5113	27 3531	27 9323	28 1254	28 2220	28 3185	28.3956
9000 00	24 5543	23 3885	23 9712	24.1656	24 2628	24 3600	24 4377
10000 0	21 4313	20 2587	20 8446	21 0402	21 1379	21.2357	21.3139
11000 0	18 8838	17 7054	18 2941	18 4907	18 5889	18.6872	18.7659
12000 0	16 7536	15 5702	16 1614	16 3587	16 4574	16 5561	16.6351
19999 0	7 77317	6 57063	7 17120	7 37177	7 47209	7 57244	7 65273
20000 0	6 95144	5 74741	6 34871	6 54953	6 64999	6 75046	6 83085
30000 0	1 36160	149020	754560	956814	1 05798	1 15918	1.24014

RC = Resistance Across Each Capacitor in the S D

Chapter 7

STATISTICAL SIMULATION

CHAPTER 7

STATISTICAL SIMULATION

An in-house computer program "SCAMPER" (a) is used in the analysis of the polyphase network. SCAMPER can be used to do statistical simulation on the circuits if the nominal component values and the tolerances were defined. Our problems in the case of polyphase networks will not allow us to use SCAMPER as it is, since the trimming simulation requires us to randomly generate Capacitor values and use trimming equations to derive the trimmed resistor values, add measuring and trimming inaccuracies, and finally simulate the circuit. Similarly, the simulation results from SCAMPER has to be compiled, this can be done manually if the number of circuits are small. In our case we increase the number of circuits until the statistical yield is stable. To do all this work within SCAMPER, the author has to develop custom Fortran programs and the associated interfaces, shown in Appendix 1.

Because of the large amount of work that is involved in the design and optimization, the statistical analysis is done at three levels depending on the importance. At the early design stages, the analysis is carried out around the nominal component values until a reasonable design is obtained. In the intermediate stage of the design, trimming simulation

is added, and when the design is finalized, the most accurate statistical simulation is used.

7.1 Statistical Analysis Around Nominal Component Values

This is the quickest statistical analysis, mainly used for broad comparisons between different designs, or for checking the effect of varying some components on the response.

The SCAMPER Program is used to vary the components randomly within specified tolerances, analyze the generated circuits and then perform statistical analysis to calculate the minimum, maximum, average and standard deviation of the response. The statistical analysis can be done on a specified number of circuits, SCAMPER will show the summary of the results, the detailed response of each circuit is lost.

A sample data file "SD7K9 Data File" is shown in Appendix 2. Table 5 shows a sample SCAMPER output file.

To get the detailed responses from each circuit, we can use SD7J4, SD7R9 data files shown in Appendix 2. These files use the subroutine XTOL which returns a random value of the element, given its nominal value and its tolerance.

7.2 Statistical Analysis Including Humidity and Temperature Effects

As shown in Chapter 6, the effect of humidity is simulated by adding a resistor across each capacitor (these resistors can vary widely), we will assume in our analysis a ±50% tolerance on these resistors.

Table 6 summarizes the statistical simulation including the effect of moisture for different values of moisture resistances RC, from which as indicated in Chapter 6 the value of RC has to be greater than 8 Mohms, which was found to be possible.

Table 5. Sample SCAMPER Output File

***** STATISTICS FOR *OUT *****

FREQ(HZ)	IDEAL	AVERAGE	SIGMA	MAXIMUM	MINIMUM	FAIL AVG	FAIL SIGMA	NFAIL
-1 00000+06	4.7655	4.8420	51481	5.8281	4 0622	.0	.0	0/ 0
-5 00000+05	2.6247	2 6630	21108	3.0850	2 3495	.0	.0	0/ 0
-1 00000+05	1 0175	1.0201	1 67490-02	1.0604	.98421	.0	0	0/ 0
-4000 0	.20825	.20847	3 9657D-03	.21777	.19841	.0	0	0/ 0
-3850 0	20540	20562	3.8652D-03	.21455	.19580	.0	.0	0/ 0
-3800 0	.20416	.20438	3.8309D-03	.21318	19464	.0	0	0/ 0
-3650 0	.19951	19972	3.7250D-03	20814	19025	0	0	0/ 0
-3600.0	.19764	.19785	3.6888D-03	20614	18847	.0	0	0/ 0
-3400 0	18842	.18862	3.5382D-03	19639	17963	.0	0	0/ 0
-3200.0	.17627	.17646	3 3775D-03	18369	.16790	.0	.0	0/ 0
-3000 0	.16098	.16116	3.2046D-03	.16798	.15307	.0	0	0/ 0
-2800 0	.14246	14263	3 0170D-03	.14907	13506	.0	.0	0/ 0
-2600 0	.12078	.12093	2.8114D-03	.12694	.11393	0	.0	0/ 0
-2400.0	9 6253D-02	9 6386D-02	2.5842D-03	.10192	9.00388-02	.0	.0	0/ 0
-2200.0	6.9624D-02	6.9737D-02	2.3308D-03	7.4732D-02	6.4085D-02	.0	.0	0/ 0
-2000 0	4.2202D-02	4.2300D-02	2 0462D-03	4.6685D-02	3.7430D-02	.0	0	0/ 0
-1800.0	1.6117D-02	1.6194D-02	1.7252D-03	1.9891D-02	1.2187D-02	.0	.0	0/ 0
-1600 0	-5.5119D-03	-5.4550D-03	1 3627D-03	-2.5355D-03	-8 5210D-03	.0	.0	0/ 0
-1400 0	-1.8484D-02	-1.8447D-02	9.5444D-04	-1.6403D-02	-2.0505D-02	.0	0	0/ 0
-1200 0	-1.7874D-02	-1.7857D-02	4 9741D-04	-1.6792D-02	-1.8867D-02	.0	.0	0/ 0
-1004 0	.0	.0	0	.0	.0	.0	.0	0/ 0
-1000.0	5.5524D-04	5 5493D-04	1.0686D-05	5 7593D-04	5 3207D-04	.0	.0	0/ 0
-800 00	3.6570D-02	3.6556D-02	5 7575D-04	3.7740D-02	3 5328D-02	.0	.0	0/ 0
-600 00	7.7866D-02	7.7847D-02	1.2223D-03	8.0483D-02	7.5256D-02	.0	.0	0/ 0
-400 00	.10381	10381	2 0597D-03	.10825	9.9453D-02	.0	0	0/ 0
-300.00	.14330	.14333	2 6903D-03	.14949	.13720	.0	0	0/ 0
-250 00	.21094	.21101	3.1344D-03	.21820	.20369	.0	.0	0/ 0
-200 00	.36580	.36591	3.7237D-03	.37424	.35708	.0	.0	0/ 0
-175.00	50300	.50315	4.0900D-03	51206	49339	.0	.0	0/ 0
-170.00	53735	53750	4 1697D-03	.54653	52755	.0	0	0/ 0
-160.00	61437	.61455	4.3359D-03	.62412	.60417	.0	.0	0/ 0
-100.00	1.4140	1 4143	5 5115D-03	1.4275	1 4008	.0	.0	0/ 0
-80 000	1 8718	1.8722	5 9527D-03	1.8865	1 8573	0	0	0/ 0
-30 000	3 6957	3.6962	7.0576D-03	3.7127	3 6775	.0	.0	0/ 0
0	5.3954	5 3960	7.7468D-03	5.4147	5.3747	.0	0	0/ 0
1.0000	5.4609	5.4615	7 7722D-03	5 4804	5.4402	.0	0	0/ 0
100 00	14 683	14 684	1.3520D-02	14.719	14 649	.0	.0	0/ 0
175.00	24 687	24 689	2.6230D-02	24.743	24.632	.0	0	0/ 0
200 00	28 623	28.625	3 4713D-02	28.712	28 546	.0	0	0/ 0
300 00	53 986	53.865	48684	55.274	52 639	.0	.0	0/ 0
400 00	52.220	52.145	.48288	53.751	50 745	.0	.0	0/ 0
500 00	57.601	57.385	1 0159	60.526	54.567	.0	.0	0/ 0
600 00	73.687	69 169	4 2616	81 441	59.304	59.304	.0	1/ 1
700 00	73 687	69 661	5 2502	95.550	59 682	59.743	6.1526D-02	2/ 2
800 00	74.323	69 691	4.9725	83.359	58 932	59.075	.14353	2/ 2
900 00	89.307	71 799	6 8239	89 190	58 153	58.733	.57963	2/ 2
1000 0	79 016	70.392	5 6986	91.752	57 473	58.323	.85025	2/ 2

Table 5. Sample SCAMPER Output File (continued)

1100 0	74.317	68 844	4.1540	80.730	57.008	58.469	1 0813	3/ 3
1200 0	73.687	68 471	3 8665	77 862	56.745	58.132	1 0350	3/ 3
1300 0	75 073	69 943	4 2465	77.767	56 606	57.930	1.0173	3/ 3
1400 0	78 070	69.883	5.1083	80.387	56 519	57.798	1.0159	3/ 3
1500 0	82.906	71.013	6.4048	84 985	56 444	57.698	1.0170	3/ 3
1600 0	90.914	72.127	8.1094	93.492	56 373	57.613	1.0150	3/ 3
1700 0	118.94	73 294	11:032	119.11	56 312	57.552	1.0117	3/ 3
1800 0	100.18	72.812	9 5477	104 17	56 269	57.516	1.0104	3/ 3
1900 0	103.30	72.860	9 6464	109.91	56 248	57.504	1.0129	3/ 3
2000 0	104.76	72 789	9.3353	109.04	56 249	57.515	1.0185	3/ 3
2100.0	92.634	72 391	8.2326	101.63	56.269	57.542	1.0295	3/ 3
2200 0	87.654	71 987	7 2338	91.942	56 305	57.583	1.0421	3/ 3
2300 0	84 985	71 731	6 6371	88 996	56 352	57.635	1.0566	3/ 3
2400 0	83.687	71.625	6 3081	89 575	56.405	57.697	1 0721	3/ 3
2500.0	83.462	71 680	6 2143	91.084	56 463	57.766	1.0871	3/ 3
2600.0	84 291	71.886	6 3357	94.111	56.521	57.841	1.1006	3/ 3
2700 0	86.442	72 156	6 4781	94 761	56 575	57.920	1.1115	3/ 3
2800 0	90.943	72 368	6.4600	90.477	56.625	57.998	1.1197	3/ 3
2900 0	105.45	72.556	6 7467	103.83	56.669	58.074	1.1255	3/ 3
3000 0	94.524	72.390	6 0491	94 669	56.708	58.148	1.1305	3/ 3
3100 0	87.765	72.192	5 5359	87.692	56.746	58.220	1.1359	3/ 3
3200 0	84.787	72.053	5 2294	86.476	56.791	58.294	1.1428	3/ 3
3300 0	83.687	72.038	5.0801	86.604	56 850	58.375	1.1517	3/ 3
3400 0	84.352	72.223	5 1337	87.053	56.933	58 469	1.1632	3/ 3
3500.0	88 059	72.629	5 4148	87.307	57.048	58.579	1.1798	3/ 3
3600.0	117 65	73 142	6 7427	109.90	57.201	57.978	77681	2/ 2
3700.0	83 686	72.851	5.9486	97.228	57.391	58.022	.63085	2/ 2
3800 0	76 134	71.124	5 1154	88.863	57.608	.0	.0	0/ 0
3900 0	71 171	68.730	3.5855	79 770	57 819	.0	.0	0/ 0
4000 0	67.348	66 121	2 5583	71 832	57 500	.0	.0	0/ 0
5000.0	47 508	47.518	.29756	48.314	46.540	.0	.0	0/ 0
6000 0	37.866	37.876	9.9336D-02	38.178	37 611	.0	.0	0/ 0
7000.0	31.696	31.703	4.9416D-02	31.857	31.596	.0	0	0/ 0
8000.0	27.318	27 323	3 0981D-02	27.418	27 261	0	.0	0/ 0
9000 0	24 021	24.025	2.2555D-02	24.090	23.979	.0	0	0/ 0
10000.	21.438	21.442	1 8136D-02	21.489	21.406	.0	0	0/ 0
11000	19 356	19 359	1 5584D-02	19.398	19.327	.0	0	0/ 0
12000	17.641	17 644	1 4007D-02	17.681	17.613	.0	.0	0/ 0
19000	10.901	10.903	1.1086D-02	10.936	10.877	.0	.0	0/ 0
20000	10.346	10.347	1.1037D-02	10.380	10.321	.0	.0	0/ 0
30000	6 9810	6 9822	1.1332D-02	7 0161	6 9565	.0	.0	0/ 0
40000.	5.4470	5.4483	1.1854D-02	5.4834	5.4217	.0	0	0/ 0
50000	4.5965	4 5978	1 2360D-02	4.6341	4.5701	.0	.0	0/ 0
60000	4.0654	4.0669	1 2918D-02	4.1040	4 0377	0	0	0/ 0
63000.	3 9437	3 9452	1.3107D-02	3 9826	3.9156	.0	.0	0/ 0
1.00000+05	3.1131	3 1159	1 6890D-02	3.1575	3.0780	.0	.0	0/ 0
5 00000+05	3.0437	3.0821	21111	3 5040	2.7688	.0	0	0/ 0
1.00000+06	4.9750	5.0516	51483	6.0375	4.2718	.0	0	0/ 0
REFERENCE	7 2635	7 2632	5 1401D-03	7.2757	7 2504	.0	.0	0/ 0

IN 100 SAMPLES THERE WERE 3 CIRCUITS WHICH FAILED TO MEET SPECS. SO THE YIELD IS 97 0000%

Table 6 Statistical Simulation Including Effect of Moisture

f, Hz		Minimum Losses dB				
		No Moisture	RC = 2MΩ	RC = 4MΩ	RC = 6MΩ	RC = 8MΩ
In-Band	300	0.08	1.43	.76	.54	.41
	3000	0.03	-.50	-.23	-.14	-.10
	Ripple	0.08	1.93	.99	.67	.51
Image-Band	175	24.3	21.94	22.85	23.31	23.57
	300	53.9	33.83	38.24	40.94	42.82
	400	49.8	36.05	40.45	42.74	44.19
	600	59.5	40.16	45.63	48.74	50.84
	3400	57.4	52.61	57.12	57.27	57.33
	3700	57.4	53.62	57.18	57.29	57.33

RC = Moisture Resistance Across Each Capacitor
RC is Assumed to Vary Within ± 50% of its Nominal Value

The effect of temperature can be studied using the same data file SD7K9 shown in Appendix 2 after deleting the $TERM line on the third page. Note that the specifications following that line are 2 dB lower; as explained before, the 2 dB margin is used for manufacturing specification. Different temperature runs can be generated, normally for the lowest and highest temperatures.

7.3 Statistical Analysis Including Trimming Simulation

A subroutine F51 shown in Appendix 1 is used to simulate the trimming of the resistors in a polyphase network given the notch frequency and the capacitor values, this routine is called from the SCAMPER data file, and it has to be in specific format compatible with the SCAMPER program.

A sample Data file SD7J is shown in Appendix 2; it can be used to study the trimming procedure and the effect of different tolerances on the performance of the polyphase network.

7.4 Generalized Statistical Simulation

This is the most powerful and most accurate simulation, but it is custom made for a finalized design, i.e., any change in the design requires a modified package to be written.

Two Fortran programs, POLTX, POLRX developed by the author are shown in Appendix 1. POLTX is used to generate SCAMPER data files for the transmit polyphase network; POLRX is used to generate SCAMPER data files for the receive polyphase network.

These programs allow the generation of a specified number of SCAMPER data files, in which the elements vary randomly and in which the trimming algorithm is simulated. Tolerances for operational amplifier gain-bandwidth products are also included in the simulation. The resulting SCAMPER output is processed using a series of programs shown in Appendix 1 (RSD7, RSD7B, RSD7C, RSD7E); the most important is RSD7E. RSD7E calculates the power average of the response between 600 to 3300 Hz and arranges the results in descending order so that the yield can be estimated for a given specification of power averaging.

Table 7 shows a sample output for 200 data files generated from POLTX Fortran; the output is generated by the program RSD7E.

The following assumptions were used in the analysis:

1 - Capacitors of ±1% tolerance and trimming, and measuring inaccuracies of ±0.25%.

2 - Trimming and measuring inaccuracies for the resistors = ±.25%.

3 - Gain-bandwidth tolerance of the operational amplifiers = ±20%.

4 - Only resistors for Sections 5, 7 are trimmed.

From Table 7 it is clear that the yield corresponding to 60 dB is 95% while the yield corresponding to 62 dB is 88%. Note that in this sample run only stages 5, 7 are trimmed. In our compromise design, the yield is higher because we trim all the stages since the same design is used for both the transmit and receive directions.

Table 7 Sample Output for 200 Data Files Generated from POLTX FORTRAN

AVERAGE LOSS BETWEEN 600 , 3300 HZ									
71.92	65.46	73.24	65.67	68.29	62.60	66.50	77.39	62.55	58.48
70.46	69.43	66.34	67.32	77.81	63.94	71.89	65.15	62.05	73.54
69.65	61.75	76.36	66.96	61.06	75.80	76.60	64.03	73.29	65.80
69.92	68.29	61.80	65.35	60.78	73.27	73.51	69.02	68.16	64.72
69.26	65.35	67.21	65.35	58.62	76.49	67.09	65.53	57.67	69.00
70.56	68.37	61.30	65.05	73.28	66.87	69.95	71.30	66.50	63.67
60.64	63.82	68.40	58.30	58.99	77.70	65.48	64.78	64.70	70.87
70.64	66.29	65.42	68.27	64.75	76.74	73.67	66.62	62.18	68.85
70.99	80.25	66.76	80.11	71.93	75.75	59.04	64.31	62.80	65.26
68.90	61.75	76.90	75.82	68.90	62.65	59.81	62.48	69.33	68.94
65.09	62.38	63.46	75.31	67.41	73.94	60.69	67.66	63.86	66.43
73.90	72.44	60.56	60.02	69.77	71.54	69.32	68.98	72.18	63.45
62.52	65.54	76.31	63.33	70.35	65.37	66.82	77.91	72.03	68.73
78.04	60.08	72.06	64.23	76.61	61.54	69.59	64.60	73.38	68.16
69.84	74.79	62.67	71.12	71.48	59.04	72.66	73.43	65.85	66.27
64.74	59.35	69.27	63.88	64.47	67.14	60.56	63.10	67.73	70.24
69.18	62.42	75.95	77.32	63.67	79.58	66.70	71.07	69.30	72.00
62.42	72.80	72.93	68.95	67.29	69.88	59.29	79.93	61.00	71.21
69.91	63.89	70.17	68.55	71.40	71.82	66.14	69.21	63.44	66.37
64.30	68.60	66.16	68.63	73.58	63.24	73.59	69.35	65.93	65.15
AVERAGE = 67.95 SIG = 5.1159									
80.25	80.11	79.93	79.58	78.04	77.91	77.81	77.70	77.39	77.32
76.90	76.74	76.61	76.60	76.49	76.36	76.31	75.95	75.82	75.80
75.75	75.31	74.79	73.94	73.90	73.67	73.59	73.58	73.54	73.51
73.43	73.38	73.29	73.28	73.27	73.24	72.93	72.80	72.66	72.44
72.18	72.06	72.03	72.00	71.93	71.92	71.89	71.82	71.54	71.48
71.40	71.30	71.21	71.12	71.07	70.99	70.87	70.64	70.56	70.46
70.35	70.24	70.17	69.95	69.92	69.91	69.88	69.84	69.77	69.65
69.59	69.43	69.35	69.33	69.32	69.30	69.27	69.26	69.21	69.18
69.02	69.00	68.98	68.95	68.94	68.90	68.90	68.85	68.73	68.63
68.60	68.55	68.40	68.37	68.29	68.29	68.27	68.16	68.16	67.73
67.66	67.41	67.32	67.29	67.21	67.14	67.09	66.96	66.87	66.82
66.76	66.70	66.62	66.50	66.50	66.43	66.37	66.34	66.29	66.27
66.16	66.14	65.93	65.85	65.80	65.67	65.54	65.53	65.48	65.46
65.42	65.37	65.35	65.35	65.35	65.26	65.15	65.15	65.09	65.05
64.78	64.75	64.74	64.72	64.70	64.60	64.47	64.31	64.30	64.23
64.03	63.94	63.89	63.88	63.86	63.82	63.67	63.67	63.46	63.45
63.44	63.33	63.24	63.10	62.80	62.67	62.65	62.60	62.55	62.52
62.48	62.42	62.42	62.38	62.18	62.05	61.80	61.75	61.75	61.54
61.30	61.06	61.00	60.78	60.69	60.64	60.56	60.56	60.08	60.02
59.81	59.35	59.29	59.04	59.04	58.99	58.62	58.48	58.30	57.67

Chapter 8

TESTING POLYPHASE NETWORKS

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TESTING POLYPHASE NETWORKS

Testing polyphase networks should be done with care because of the interference that may be caused from the test environment, test equipment or from the modem. The contribution of any of these factors can easily degrade the performance of the polyphase filter and cause the false rejection of the good samples. The test environment should have the lowest possible noise, the common power supply should have a clean ground with no currents flowing through the neutral phase, the test equipment should be of high dynamic range, otherwise it would be impractical to use it for high rejection measurements. Finally, the modem used should be a master piece that was previously tested with a standard polyphase filter to ensure that the modem introduces the minimum degradation on the performance of the polyphase filter. Appendix 4 shows the test jig schematic and the block diagram of the test equipment. When placing the thick-film filter (hybrid) into the test jig, the zero insertion force connector can be used to ensure that the pins of the hybrid are well connected to the external test circuitry, the hybrid must be supported so that it sits at least half an inch from the unprinted substrate side to any surrounding metallic surface. The

test jig has a switch to allow the filter to be tested in the transmit or in the receive modes.

8.1 Test Results

A large number of hybrids have been tested in the transmit and receive modes. In the transmit mode all the samples passed the test, while in the receive mode approximately 60% of the samples passed the test. Since these samples failing in the receive modes can be used in the transmit mode, the overall yield of the filter is very close to 100%.

Table 8 shows a sample test result for a transmit polyphase filter; Table 9 shows a sample test result for a receive polyphase filter.

Table 8 - A Sample Test Result for a Transmit Polyphase Filter

TX SUBSTRATE NO. .2
REF. LEVEL dB = -7.656

PASS-BAND MEASUREMENT

I/P FREQ Hz	O/P FREQ kHz	NORMALIZED LOSS dB
300	63.70	.244
400	63.60	.163
3000	61.00	.155
3400	60.60	.182

STOP-BAND MEASUREMENT
POWER SERIES CALCULATION IN dB = 66.032

I/P FREQ Hz	O/P FREQ kHz	NORMALIZED LOSS dB
175	64.175	24.79
300	64.300	51.98
600	64.600	82.09
900	64.900	69.83
1200	65.200	70.98
1500	65.500	67.59
1800	65.800	65.52
2100	66.100	64.67
2400	66.400	64.03
2700	66.700	63.34
3000	67.000	62.55
3300	67.300	61.95

Table 9 - A Sample Test Result for a Receiver Polyphase Filter

TX SUBSTRATE NO. IS 2
REF. LEVEL IN dB = 2.243
REF. LEVEL CORRECTION IN dB = 11.297
CORRECTED REFERENCE IN dB = 13.54

PASS-BAND MEASUREMENT

I/P FREQ Hz	O/P FREQ kHz	NORMALIZED LOSS dB
63.70	300	.165
63.60	400	.120
61.00	3000	.179
60.60	3400	.211

STOP-BAND MEASUREMENT

I/P FREQ Hz	O/P FREQ kHz	NORMALIZED LOSS dB
64.175	175	24.01
64.300	300	49.77
64.600	600	77.99
64.900	900	67.92
65.200	1200	73.01
65.500	1500	67.80
65.800	1800	65.16
66.100	2100	64.82
66.400	2400	64.98
66.700	2700	64.43
67.000	3000	63.21
67.300	3300	62.36

POWER SERIES CALCULATION IN dB = 67.043

Chapter 9

CONCLUSIONS AND FUTURE DEVELOPMENTS

CHAPTER 9

CONCLUSIONS AND FUTURE DEVELOPMENTS

Novel design approaches in a high selectivity, high frequency filtering using the polyphase network were examined. The special case of the 90° polyphase network was found to be of most practical value.

The polyphase network was designed to meet the channel bank specifications of 60 dB out-of-band rejection while maintaining a low in-band ripple of ±0.25 dB, through the invention of buffered polyphase networks. The high out-of-band rejection of 60 dB, cannot be achieved by the conventional way of increasing the number of polyphase network stages.

In previous channel bank filtering using crystal or mechanical filters, a separate filter design is needed for each of the twelve channels. In our technique using the polyphase network, only one design can be used for any of the twelve channels by changing the clock frequency applied to the modem. In addition, the same design can be used for both the transmit and the receive direction.

The capacitors of the polyphase network stages can be chosen to be of different value; in the existing design all the stages use the same capacitor value, which simplifies the manufacturing of the network. The resultant resistor ratio of the network (ratio of maximum resistor value to minimum resistor value) was far smaller than in previous designs which use unequal capacitor values. This resulted in a further simplification in manufacturing since all the resistors were printed on the substrate using one ink only.

The tolerance requirements on capacitors to manufacture the circuits have been relaxed to a practical value of ±1%, from the existing state of the art of ±0.2%, through the invention of a new trimming procedure. The new ideas in the trimming can be used for other circuit designs.

Sensitivity analysis was carried out with the result of further simplification of trimming polyphase sections. It was concluded that if the polyphase network is used in the transmit direction, the last sections of the polyphase network need to be trimmed, while if it is used in the receive direction, only the first sections need to be trimmed.

The timing requirements for the modem circuits have been derived. The relationship between the maximum allowable time error and the achieveable out-of-band rejection is shown in graph form to help future designs.

The filters are being manufactured on a 1" x 2.5" substrate using thick-film technology. The overall yield of the manufactured network is close to 100%. Future implementation could result in a smaller substrate, or the incorporation of both the transmit and receive filters on one substrate.

The successful approaches used in the design have resulted in new routes to be investigated which may result in more optimized strategies for specific applications and/or external circuitry. These are:

a. Development of a stand-alone test procedure, i.e., to test the polyphase network without any modems. The existing test procedure involves the testing of the polyphase network with a standard modem. If the modem were not extremely good, there could be good polyphase networks which fail the test. The stand-alone test procedure will remove the uncertainty of failing good networks.

b. Development of a functional trimming procedure, which will eliminate the measurements of all the capacitors and will reduce the number of resistors to be trimmed.

c. If the functional trimming procedure in (b) is combined with the stand-alone test procedure in (a), we may be able to eliminate the need for testing the polyphase network completely.

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Appendix 1

FORTRAN PROGRAM LISTINGS

APPENDIX 1

FORTRAN PROGRAMS AND ASSOCIATED SUBROUTINES

1 - POLTX Program

Generates any specified number of data files to analyze the polyphase network in the transmit direction, by the analysis package "SCAMPER". The data files are generated at random using the nominal values and component tolerances.

2 - POLRX Program

Generates any specified number of data files to analyze the polyphase network in the receive direction, by the analysis package "SCAMPER". The data files are genrated at random using the nominal values and component tolerances.

3 - Function XT02

Used for both POLTX, POLRX programs to return a random value for a component, given its nominal value and the percentage tolerance.

4 - Subroutine F51

Formatted to be called from a SCAMPER data file to return the trimmed resistor value given the notch frequency and the capacitor value.

5 - Function F51B

Used for both POLTX, POLRX programs to calcualte the trimmed value of a resistor, given the associated capacitor value, the angular frequency and the trimming inaccuracy.

6 - Subroutine XTOL

Same as function XT02, but formatted to be called from a SCAMPER data file.

7 - Subroutine C10

Formatted to be called from a SCAMPER data file to cause a given voltage to be phase shifted with a specified angle, in radians.

8 - Subroutine C12

Same as C10, but the phase shift have a random value for a given tolerance.

9 - RSD7 Program

To process the output file generated by SCAMPER, for each circuit, it calculates the average loss in dB between 600 to 3300 Hz, list these averages, find their average, standard deviation, minimum, maximum value and arrange these values in descending order to calculate the yield corresponding to a given specification.

10 - RSD7B Program

To process the output file generated by the SCAMPER program, to look at statistics at a specified frequency.

11 - RSD7C Program

To process the output file generated by the SCAMPER program and reformat the output so that the frequency response of each randomly generated circuit in a given frequency range is shown. The new format make the output more readable as it shows one or two lines per circuit.

12 - RSD7E Program

Same as RSD7, but the average is calculated on power basis, instead of the arithmetic average.

13 - Power Program

To calculate the power average, given the losses between 600 to 3300 Hz in dB.

14 - AB1X, AB2X Programs

To analyze a single section polyphase network, given the values of R, C for the section. AB1X used for the positive sequence analysis. AB2X used for the negative sequence anlaysis.

15 - Subroutines AB1, AB2, AB3 "AB3 File"

Used with the programs AB1X, AB2X to evaluate the ABCD matrix for the positive and negative sequence analysis.

16 - AB3X Program

To analyze a single section polyphase network with grounded resistors, given R, C and RG. The analysis can be done for both the positive and the negative sequences.

17 - AB4X Program

Same as AB3X program, but used to optimize the value of RG such that the pass-band ripple is minimized.

18 - Subroutines AB4, AB5, AB6 "AB6 File"

Used with programs AB3X, AB4X to evaluate the ABCD matrix for the positive and negative sequence analysis.

19 - RR1 Exec

To process the SCAMPER output file with any of the Fortran programs RSD7, RSD7B, RSD7C or RSD7E.

```
C-------      POLTX  FORTRAN      -------
C
      IMPLICIT REAL*8(A-H,O-Z)
      PI=4.DO*DATAN2(1.DO,1.DO)
      F1=633.34573DO
      F2=920.73961DO
      F3=2922.0927DO
      F4=1960.9299DO
      F5=3597.4707DO
      F6=319.55187DO
      F7=1706.1400DO
      RGNOM=35.50351D3
      CNOM=2.2D-9
      W1=2.DO*PI*F1
      W2=2.DO*PI*F2
      W3=2.DO*PI*F3
      W4=2.DO*PI*F4
      W5=2.DO*PI*F5
      W6=2.DO*PI*F6
      W7=2.DO*PI*F7
      R1NOM=F51B(W1,CNOM,0.)
      R2NOM=F51B(W2,CNOM,0.)
      R3NOM=F51B(W3,CNOM,0.)
      R4NOM=F51B(W4,CNOM,0.)
      R5NOM=F51B(W5,CNOM,0.)
      R6NOM=F51B(W6,CNOM,0.)
      R7NOM=F51B(W7,CNOM,0.)
      WRITE(5,3)
3     FORMAT(' ENTER NO. OF CIRCUITS ')
      READ(5,*,END=500) NCKT
      WRITE(5,6)
6     FORMAT(' ENTER TOLERANCES    TCC,TC,TR,TRS,TEE,TG  ')
      READ(5,*,END=500) TCC,TC,TR,TRS,TEE,TG
      DO 200 J=1,NCKT
      WRITE(2,5) J
5     FORMAT('$H     POLYPHASE  TX NO. ' ,I5,'( CASE XD6247 ) ')
      RS1=XTO2(15.E3,TR)
      RS2=XTO2(15.E3,TR)
      RS3=XTO2(15.E3,TR)
      RS4=XTO2(15.E3,TR)
      C11=XTO2(CNOM,TCC)
      C12=XTO2(CNOM,TCC)
      C13=XTO2(CNOM,TCC)
      C14=XTO2(CNOM,TCC)
      R11=XTO2(R1NOM,TR)
      R12=XTO2(R1NOM,TR)
      R13=XTO2(R1NOM,TR)
      R14=XTO2(R1NOM,TR)
      C21=XTO2(CNOM,TCC)
      C22=XTO2(CNOM,TCC)
      C23=XTO2(CNOM,TCC)
      C24=XTO2(CNOM,TCC)
```

```
      R21=XTO2(R2NOM,TR)
      R22=XTO2(R2NOM,TR)
      R23=XTO2(R2NOM,TR)
      R24=XTO2(R2NOM,TR)
      C31=XTO2(CNOM,TCC)
      C32=XTO2(CNOM,TCC)
      C33=XTO2(CNOM,TCC)
      C34=XTO2(CNOM,TCC)
      R31=XTO2(R3NOM,TR)
      R32=XTO2(R3NOM,TR)
      R33=XTO2(R3NOM,TR)
      R34=XTO2(R3NOM,TR)
      C41=XTO2(CNOM,TCC)
      C42=XTO2(CNOM,TCC)
      C43=XTO2(CNOM,TCC)
      C44=XTO2(CNOM,TCC)
      R41=XTO2(R4NOM,TR)
      R42=XTO2(R4NOM,TR)
      R43=XTO2(R4NOM,TR)
      R44=XTO2(R4NOM,TR)
      C51=XTO2(CNOM,TCC)
      C52=XTO2(CNOM,TCC)
      C53=XTO2(CNOM,TCC)
      C54=XTO2(CNOM,TCC)
      R51=F51B(W5,C54,TR)
      R52=F51B(W5,C51,TR)
      R53=F51B(W5,C52,TR)
      R54=F51B(W5,C53,TR)
      C51=XTO2(C51,TC)
      C52=XTO2(C52,TC)
      C53=XTO2(C53,TC)
      C54=XTO2(C54,TC)
      C61=XTO2(CNOM,TCC)
      C62=XTO2(CNOM,TCC)
      C63=XTO2(CNOM,TCC)
      C64=XTO2(CNOM,TCC)
      R61=XTO2(R6NOM,TR)
      R62=XTO2(R6NOM,TR)
      R63=XTO2(R6NOM,TR)
      R64=XTO2(R6NOM,TR)
C     C61=XTO2(C61,TC)
C     C62=XTO2(C62,TC)
C     C63=XTO2(C63,TC)
C     C64=XTO2(C64,TC)
      C71=XTO2(CNOM,TCC)
      C72=XTO2(CNOM,TCC)
      C73=XTO2(CNOM,TCC)
      C74=XTO2(CNOM,TCC)
      R71=F51B(W7,C74,TR)
      R72=F51B(W7,C71,TR)
      R73=F51B(W7,C72,TR)
      R74=F51B(W7,C73,TR)
```

```
      C71=XTO2(C71,TC)
      C72=XTO2(C72,TC)
      C73=XTO2(C73,TC)
      C74=XTO2(C74,TC)
      RG1=XTO2(RGNOM,TR)
      RG2=XTO2(RGNOM,TR)
      RG3=XTO2(RGNOM,TR)
      RG4=XTO2(RGNOM,TR)
      GG1=XTO2(1.E6,TG)
      GG2=XTO2(1.E6,TG)
      GG3=XTO2(1.E6,TG)
      GG4=XTO2(1.E6,TG)
      AB=XTO2(-1.,TEE)
      IF(J.NE.1) GO TO 100
      WRITE(2,8) TCC,TC,TR,TG
8     FORMAT('$*  CAPACITOR TOLERANCES = ',F7.3,' %'/
     +   '$* TC= ',F7.3,' %',9X,'TR= ',F7.3,' %',9X,'TG= ',F7.3)
      WRITE(2,9)
9     FORMAT('$P C11,C12,C13,C14,C21,C22,C23,C24',
     +  ',C31,C32,C33,C34'/'$P C41,C42,C43,C44,C51,C52,C53,C54'/
     +  ',C61,C62,C63,C64'/'$P C71,C72,C73,C74'/
     +  '$P R11,R12,R12,R14,R21,R22,R23,R24,R31,R32,R33,R34'/
     +  '$P R41,R42,R43,R44,R51,R52,R53,R54,R61,R62,R63,R64'/
     +  '$P R71,R72,R73,R74'/
     +        '$P RS1,RS2,RS3,RS4,RG1,RG2,RG3,RG4')
      WRITE(2,10) RS1,RS2,RS3,RS4
10    FORMAT('RS1  1  5  ',F7.0/'RS2  2  6 ',F7.0/'RS3  3  7 ',
     + F7.0/'RS4  4  8 ',F7.0)
      WRITE(2,11) C11,C12,C13,C14
11    FORMAT('C11  5 10 ',E12.6/'C12  6 11 ',E12.6/'C13  7 12 ',
     +  E12.6/'C14  8  9 ',E12.6)
      WRITE(2,12) R11,R12,R13,R14
12    FORMAT('R11  5  9 ',F7.0/'R12  6 10 ',F7.0/'R13  7 11 ',
     +  F7.0/'R14  8 12 ',F7.0)
      WRITE(2,13) C21,C22,C23,C24
13    FORMAT('C21  9 14 ',E12.6/'C22 10 15 ',E12.6/'C23 11 16 ',
     +  E12.6/'C24 12 13 ',E12.4)
      WRITE(2,14) R21,R22,R23,R24
14    FORMAT('R21  9 13 ',F7.0/'R22 10 14 ',F7.0/'R23 11 15 ',
     +  F7.0/'R24 12 16 ',F7.0)
      WRITE(2,15) C31,C32,C33,C34
15    FORMAT('C31 13 18 ',E12.6/'C32 14 19 ',E12.6/'C33 15 20 ',
     +  E12.6/'C34 16 17 ',E12.6)
      WRITE(2,16) R31,R32,R33,R34
16    FORMAT('R31 13 17 ',F7.0/'R32 14 18 ',F7.0/'R33 15 19 ',
     +   F7.0/'R34 16 20 ',F7.0)
      WRITE(2,17) C41,C42,C43,C44
17    FORMAT('C41 17 22 ',E12.6/'C42 18 23 ',E12.6/'C43 19 24 ',
     +   E12.6/'C44 20 21 ',E12.6)
      WRITE(2,18) R41,R42,R43,R44
18    FORMAT('R41 17 21 ',F7.0/'R42 18 22 ',F7.0/'R43 19 23 ',
     +   F7.0/'R44 20 24 ',F7.0)
```

```
      WRITE(2,19) C51,C52,C53,C54
   19 FORMAT('C51 21 26 ',E12.6/'C52 22 27 ',E12.6/'C53 23 28 ',
     +  E12.6/'C54 24 25 ',E12.6)
      WRITE(2,20) R51,R52,R53,R54
   20 FORMAT('R51 21 25 ',F7.0/'R52 22 26 ',F7.0/'R53 23 27 ',
     +  F7.0/'R54 24 28 ',F7.0)
      WRITE(2,21) C61,C62,C63,C64
   21 FORMAT('C61 25 80 ',E12.6/'C62 26 81 ',E12.6/'C63 27 82 ',
     +  E12.6/'C64 28 79 ',E12.6)
      WRITE(2,22) R61,R62,R63,R64
   22 FORMAT('R61 25 79 ',F7.0/'R62 26 80 ',F7.0/'R63 27 81 ',
     +  F7.0/'R64 28 82 ',F7.0)
      WRITE(2,23) GG1,GG2,GG3,GG4
   23 FORMAT('$P RR,GA,GG1,GG2,GG3,GG4'/'*RR=1.E10'/'*GA=2.E4'/
     + '*GG1= ',E12.6/'*GG2= ',E12.6/'*GG3= ',E12.6/'*GG4= ',E12.6)
      WRITE(2,24)
   24 FORMAT(
     +  'M1 OPAMP 79 29 29 GND / RIN=*RR , GAIN=*GA , GBW=*GG1'/
     +  'M2 OPAMP 80 30 30 GND / RIN=*RR , GAIN=*GA , GBW=*GG2'/
     +  'M3 OPAMP 81 31 31 GND / RIN=*RR , GAIN=*GA , GBW=*GG3'/
     +  'M4 OPAMP 82 32 32 GND / RIN=*RR , GAIN=*GA , GBW=*GG4')
      WRITE(2,25) C71,C72,C73,C74
   25 FORMAT('C71 29 34 ',E12.6/'C72 30 35 ',E12.6/'C73 31 36 ',
     +       E12.6/'C74 32 33 ',E12.6)
      WRITE(2,26) R71,R72,R73,R74
   26 FORMAT('R71 29 33 ',F7.0/'R72 30 34 ',F7.0/'R73 31 35 ',
     +       F7.0/'R74 32 36 ',F7.0)
      WRITE(2,27) RG1,RG2,RG3,RG4
   27 FORMAT('RG1 21 GND ',F7.0/'RG2 22 GND ',F7.0/'RG3 23 GND ',
     +       F7.0/'RG4 24 GND ',F7.0)
      WRITE(2,28) AB,AB
   28 FORMAT('E1 N1 GND 0'/'VL 1 GND V(E1) 1.'/'V1 3 GND V(VL) ',
     +       F9.4/'V2 2 GND V(VL) 1.'/'V4 4 GND V(VL) ',F9.4/
     + 'VV1 A33 GND V(01) C10(0.)'/'VV2 A34 GND V(02) C10(',
     +  '1.5707963)'/'VV3 A35 GND V(03) C10(3.1415927)'/
     +  'VV4 A36 GND V(04) C10(4.712389)'/
     +  'VV5 100 GND V(05) V(06) 1. 1.'/'VV6 200 GND V(07) V(08)',
     +  ' 1. 1.'/'VV7 300 GND V(09) V(010) 1. 1.'/'01 33 GND '/
     +  '02 34 GND'/'03 35 GND'/'04 36 GND'/'05 A33 GND'/
     +  '06 A34 GND '/'07 A35 GND'/'08 A36 GND'/'09 100 GND'/
     +  '010 200 GND')
      WRITE(2,29)
   29 FORMAT('$PORT *OUT = NV(300)/E1 DBL AREF(-1004.,-1004.) S'/
C    +  '$DELAY *DEL = NV(33)/E1 DBL DREF(2200.,2200.)'/
     +  '$FREQ SP  175. 300. 600. 900. 1200. 1500. 1800. 2100.'/
     +  '$FREQ SP 2400. 2700. 3000. 3300.  3700.'/
C    +  '$FREQ SP -300. -400. -2000. -3000. -3200. -3300. -3400.'/
C    +  '$FREQ SP -1004. 2200.'/'$ANAL')
     +  '$FREQ SP -1004.'/'$ANAL')
      GO TO 200
  100 WRITE(2,31) RS1,RS2,RS3,RS4
   31 FORMAT('*RS1= ',F7.0/'*RS2= ',F7.0/'*RS3= ',F7.0/'*RS4= ',
```

```
     +       F7.0 )
             WRITE(2,32) C11,C12,C13,C14
  32         FORMAT('*C11= ',E12.6/'*C12= ',E12.6/'*C13= ',E12.6/
     +       '*C14= ',E12.6)
             WRITE(2,33) R11,R12,R13,R14
  33         FORMAT('*R11= ',F7.0/'*R12= ',F7.0/'*R13= ',F7.0/'*R14= ',
     +         F7.0 )
             WRITE(2,34) C21,C22,C23,C24
  34         FORMAT('*C21= ',E12.6/'*C22= ',E12.6/'*C23= ',E12.6/
     +         '*C24= ',E12.6)
             WRITE(2,35) R21,R22,R23,R24
  35         FORMAT('*R21= ',F7.0/'*R22= ',F7.0/'*R23= ',F7.0/'*R24= ',
     +         F7.0 )
             WRITE(2,36) C31,C32,C33,C34
  36         FORMAT('*C31= ',E12.6/'*C32= ',E12.6/'*C33= ',E12.6/
     +         '*C34= ',E12.6)
             WRITE(2,37) R31,R32,R33,R34
  37         FORMAT('*R31= ',F7.0/'*R32= ',F7.0/'*R33= ',F7.0/'*R34= ',
     +         F7.0 )
             WRITE(2,38) C41,C42,C43,C44
  38         FORMAT('*C41= ',E12.6/'*C42= ',E12.6/'*C43= ',E12.6/
     +         '*C44= ',E12.6)
             WRITE(2,39) R41,R42,R43,R44
  39         FORMAT('*R41= ',F7.0/'*R42= ',F7.0/'*R43= ',F7.0/'*R44= ',
     +         F7.0 )
             WRITE(2,40) C51,C52,C53,C54
  40         FORMAT('*C51= ',E12.6/'*C52= ',E12.6/'*C53= ',E12.6/
     +         '*C54= ',E12.6)
             WRITE(2,41) R51,R52,R53,R54
  41         FORMAT('*R51= ',F7.0/'*R52= ',F7.0/'*R53= ',F7.0/'*R54= ',
     +         F7.0 )
             WRITE(2,42) C61,C62,C63,C64
  42         FORMAT('*C61= ',E12.6/'*C62= ',E12.6/'*C63= ',E12.6/
     +         '*C64= ',E12.6)
             WRITE(2,43) R61,R62,R63,R64
  43         FORMAT('*R61= ',F7.0/'*R62= ',F7.0/'*R63= ',F7.0/'*R64= ',
     +         F7.0 )
             WRITE(2,44) C71,C72,C73,C74
  44         FORMAT('*C71= ',E12.6/'*C72= ',E12.6/'*C73= ',E12.6/
     +         '*C74= ',E12.6)
             WRITE(2,45) R71,R72,R73,R74
  45         FORMAT('*R71= ',F7.0/'*R72= ',F7.0/'*R73= ',F7.0/'*R74= ',
     +         F7.0 )
             WRITE(2,46) RG1,RG2,RG3,RG4
  46         FORMAT('*RG1= ',F7.0/'*RG2= ',F7.0/'*RG3= ',F7.0/'*RG4= ',
     +         F7.0 )
             WRITE(2,47) GG1,GG2,GG3,GG4
  47         FORMAT('*GG1= ',E12.6/'*GG2= ',E12.6/'*GG3= ',E12.6/
     +         '*GG4= ',E12.6)
             WRITE(2,48)
  48         FORMAT('$ANAL')
  200        CONTINUE
```

```
500   STOP
      END
```

```
C-------      POLRX  FORTRAN      -------
C
C
      IMPLICIT REAL*8(A-H,O-Z)
      PI=4.D0*DATAN2(1.D0,1.D0)
      F1=633.34573D0
      F2=920.73961D0
      F3=2922.0927D0
      F4=1960.9299D0
      F5=3597.4707D0
      F6=319.55187D0
      F7=1706.1400D0
      RGNOM=35.50351D3
      CNOM=2.2D-9
      W1=2.D0*PI*F1
      W2=2.D0*PI*F2
      W3=2.D0*PI*F3
      W4=2.D0*PI*F4
      W5=2.D0*PI*F5
      W6=2.D0*PI*F6
      W7=2.D0*PI*F7
      R1NOM=F51B(W1,CNOM,0.)
      R2NOM=F51B(W2,CNOM,0.)
      R3NOM=F51B(W3,CNOM,0.)
      R4NOM=F51B(W4,CNOM,0.)
      R5NOM=F51B(W5,CNOM,0.)
      R6NOM=F51B(W6,CNOM,0.)
      R7NOM=F51B(W7,CNOM,0.)
      WRITE(5,3)
3     FORMAT(' ENTER NO. OF CIRCUITS ')
      READ(5,*,END=500) NCKT
      WRITE(5,6)
6     FORMAT(' ENTER TCC,TC,TR,TRS,TR1,TG'/
     +       ' AND RA,RB,RC,RD,TRA,TRB,TRC,TRD ')
      READ(5,*,END=500)TCC,TC,TR,TRS,TR1,TG,RA1,RB1,RC1,RD1,
     +     TRA,TRB,TRC,TRD
      DO 200 J=1,NCKT
      WRITE(2,5) J
5     FORMAT('$H     POLYPHASE  RX NO. ',I5,' ( CASE XD6247 ) ')
      RS1=XTO2(15.D3,TRS)
      RS2=XTO2(15.D3,TRS)
      RS3=XTO2(15.D3,TRS)
      RS4=XTO2(15.D3,TRS)
      C11=XTO2(CNOM,TCC)
      C12=XTO2(CNOM,TCC)
      C13=XTO2(CNOM,TCC)
      C14=XTO2(CNOM,TCC)
      R11=F51B(W1,C14,TR)
      R12=F51B(W1,C11,TR)
      R13=F51B(W1,C12,TR)
      R14=F51B(W1,C13,TR)
      C11=XTO2(C11,TC)
```

```
C12=XTO2(C12,TC)
C13=XTO2(C13,TC)
C14=XTO2(C14,TC)
C21=XTO2(CNOM,TCC)
C22=XTO2(CNOM,TCC)
C23=XTO2(CNOM,TCC)
C24=XTO2(CNOM,TCC)
R21=F51B(W2,C24,TR)
R22=F51B(W2,C21,TR)
R23=F51B(W2,C22,TR)
R24=F51B(W2,C23,TR)
C21=XTO2(C21,TC)
C22=XTO2(C22,TC)
C23=XTO2(C23,TC)
C24=XTO2(C24,TC)
C31=XTO2(CNOM,TCC)
C32=XTO2(CNOM,TCC)
C33=XTO2(CNOM,TCC)
C34=XTO2(CNOM,TCC)
R31=F51B(W3,C34,TR)
R32=F51B(W3,C31,TR)
R33=F51B(W3,C32,TR)
R34=F51B(W3,C33,TR)
C31=XTO2(C31,TC)
C32=XTO2(C32,TC)
C33=XTO2(C33,TC)
C34=XTO2(C34,TC)
C41=XTO2(CNOM,TCC)
C42=XTO2(CNOM,TCC)
C43=XTO2(CNOM,TCC)
C44=XTO2(CNOM,TCC)
R41=F51B(W4,C44,TR)
R42=F51B(W4,C41,TR)
R43=F51B(W4,C42,TR)
R44=F51B(W4,C43,TR)
C41=XTO2(C41,TC)
C42=XTO2(C42,TC)
C43=XTO2(C43,TC)
C44=XTO2(C44,TC)
C51=XTO2(CNOM,TCC)
C52=XTO2(CNOM,TCC)
C53=XTO2(CNOM,TCC)
C54=XTO2(CNOM,TCC)
R51=F51B(W5,C54,TR)
R52=F51B(W5,C51,TR)
R53=F51B(W5,C52,TR)
R54=F51B(W5,C53,TR)
C51=XTO2(C51,TC)
C52=XTO2(C52,TC)
C53=XTO2(C53,TC)
C54=XTO2(C54,TC)
C61=XTO2(CNOM,TCC)
```

```
      C62=XTO2(CNOM,TCC)
      C63=XTO2(CNOM,TCC)
      C64=XTO2(CNOM,TCC)
      R61=F51B(W6,C64,TR)
      R62=F51B(W6,C61,TR)
      R63=F51B(W6,C62,TR)
      R64=F51B(W6,C63,TR)
      C61=XTO2(C61,TC)
      C62=XTO2(C62,TC)
      C63=XTO2(C63,TC)
      C64=XTO2(C64,TC)
      C71=XTO2(CNOM,TCC)
      C72=XTO2(CNOM,TCC)
      C73=XTO2(CNOM,TCC)
      C74=XTO2(CNOM,TCC)
      R71=F51B(W7,C74,TR)
      R72=F51B(W7,C71,TR)
      R73=F51B(W7,C72,TR)
      R74=F51B(W7,C73,TR)
      C71=XTO2(C71,TC)
      C72=XTO2(C72,TC)
      C73=XTO2(C73,TC)
      C74=XTO2(C74,TC)
      RG1=XTO2(RGNOM,TR)
      RG2=XTO2(RGNOM,TR)
      RG3=XTO2(RGNOM,TR)
      RG4=XTO2(RGNOM,TR)
      GG1=XTO2(1.E6,TG)
      GG2=XTO2(1.E6,TG)
      GG3=XTO2(1.E6,TG)
      GG4=XTO2(1.E6,TG)
      GG5=XTO2(1.E6,TG)
      GG6=XTO2(1.E6,TG)
      GG7=XTO2(2.E6,TG)
      RA=XTO2(RA1,TRA)
      RB=XTO2(RB1,TRB)
      RC=XTO2(RC1,TRC)
      RD=XTO2(RD1,TRD)
      RYY1=XTO2(100.D3,TR1)
      RYY2=XTO2(100.D3,TR1)
      RX3=XTO2(100.D3,TR1)
      RX4=XTO2(100.D3,TR1)
      IF(J.NE.1) GO TO 100
      WRITE(2,8) TCC,TC,TR,TG
8     FORMAT('$*  CAPACITOR TOLERANCES = ',F7.3,' % '/'$* TC= ',
     +  F7.3,' %',8X,' TR= ',F7.3,' %',8X,' TG= ',F7.3,' % ')
      WRITE(2,9)
9     FORMAT(
     +    '$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34'/
     +   '$P C41,C42,C43,C44,C51,C52,C53,C54,C61,C62,C63,C64'/
     +   '$P C71,C72,C73,C74'/
     +   '$P R11,R12,R13,R14,R21,R22,R23,R24,R31,R32,R33,R34'/
```

```
     +    '$P R41,R42,R43,R44,R51,R52,R53,R54,R61,R62,R63,R64'/
     +    '$P R71,R72,R73,R74'/
     +   '$P RA,RB,RC,RD,RYY1,RYY2,RX3,RX4'/
     +         '$P RS1,RS2,RS3,RS4,RG1,RG2,RG3,RG4')
          WRITE(2,10) RS1,RS2,RS3,RS4
 10       FORMAT('RS1  1  5  ',F7.0/'RS2  2  6 ',F7.0/'RS3  3  7 ',
     +   F7.0/'RS4  4  8 ',F7.0)
          WRITE(2,11) C11,C12,C13,C14
 11       FORMAT('C11  5 10 ',E12.6/'C12  6 11 ',E12.6/'C13  7 12 ',
     +   E12.6/'C14  8  9 ',E12.6)
          WRITE(2,12) R11,R12,R13,R14
 12       FORMAT('R11  5  9 ',F7.0/'R12  6 10 ',F7.0/'R13  7 11 ',
     +   F7.0/'R14  8 12 ',F7.0)
          WRITE(2,13) C21,C22,C23,C24
 13       FORMAT('C21  9 14 ',E12.6/'C22 10 15 ',E12.6/'C23 11 16 ',
     +   E12.6/'C24 12 13 ',E12.4)
          WRITE(2,14) R21,R22,R23,R24
 14       FORMAT('R21  9 13 ',F7.0/'R22 10 14 ',F7.0/'R23 11 15 ',
     +   F7.0/'R24 12 16 ',F7.0)
          WRITE(2,15) C31,C32,C33,C34
 15       FORMAT('C31 13 18 ',E12.6/'C32 14 19 ',E12.6/'C33 15 20 ',
     +   E12.6/'C34 16 17 ',E12.6)
          WRITE(2,16) R31,R32,R33,R34
 16       FORMAT('R31 13 17 ',F7.0/'R32 14 18 ',F7.0/'R33 15 19 ',
     +    F7.0/'R34 16 20 ',F7.0)
          WRITE(2,17) C41,C42,C43,C44
 17       FORMAT('C41 17 22 ',E12.6/'C42 18 23 ',E12.6/'C43 19 $24 ',/
     +    E12.6/'C44 20 21 ',E12.6)
          WRITE(2,18) R41,R42,R43,R44
 18       FORMAT('R41 17 21 ',F7.0/'R42 18 22 ',F7.0/'R43 19 23 ',
     +    F7.0/'R44 20 24 ',F7.0)
          WRITE(2,19) C51,C52,C53,C54
 19       FORMAT('C51 21 26 ',E12.6/'C52 22 27 ',E12.6/'C53 23 28 ',
     +    E12.6/'C54 24 25 ',E12.6)
          WRITE(2,20) R51,R52,R53,R54
 20       FORMAT('R51 21 25 ',F7.0/'R52 22 26 ',F7.0/'R53 23 27 ',
     +    F7.0/'R54 24 28 ',F7.0)
          WRITE(2,21) C61,C62,C63,C64
 21       FORMAT('C61 25 80 ',E12.6/'C62 26 81 ',E12.6/'C63 27 82 ',
     +    E12.6/'C64 28 79 ',E12.6)
          WRITE(2,22) R61,R62,R63,R64
 22       FORMAT('R61 25 79 ',F7.0/'R62 26 80 ',F7.0/'R63 27 81 ',
     +    F7.0/'R64 28 82 ',F7.0)
          WRITE(2,23) GG1,GG2,GG3,GG4,GG5,GG6,GG7
 23       FORMAT('$P RR,GA,GG1,GG2,GG3,GG4,GG5,GG6,GG7'/'*RR=1.E10'/
     +    '*GA=2.E4'/'*GG1= ',E12.6/'*GG2= ',E12.6/'*GG3= ',E12.6/
     +    '*GG4= ',E12.6/'*GG5= ',E12.6/'*GG6= ',E12.6/
     +    '*GG7= ',E12.6)
          WRITE(2,24)
 24       FORMAT(
     +    'M1 OPAMP 79 29 29 GND / RIN=*RR , GAIN=*GA , GBW=*GG1'/
     +    'M2 OPAMP 80 30 30 GND / RIN=*RR , GAIN=*GA , GBW=*GG2'/
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     +   'M3 OPAMP 81 31 31 GND / RIN=*RR , GAIN=*GA , GBW=*GG3'/
     +   'M4 OPAMP 82 32 32 GND / RIN=*RR , GAIN=*GA , GBW=*GG4')
         WRITE(2,25) C71,C72,C73,C74
 25      FORMAT('C71 29 34 ',E12.6/'C72 30 35 ',E12.6/'C73 31 36 ',
     +        E12.6/'C74 32 33 ',E12.6)
         WRITE(2,26) R71,R72,R73,R74
 26      FORMAT('R71 29 33 ',F7.0/'R72 30 34 ',F7.0/'R73 31 35 ',
     +        F7.0/'R74 32 36 ',F7.0)
         WRITE(2,27) RG1,RG2,RG3,RG4
 27      FORMAT('RG1 21 GND ',F7.0/'RG2 22 GND ',F7.0/'RG3 23 GND ',
     +        F7.0/'RG4 24 GND ',F7.0)
         WRITE(2,28) RA,RB,RC,RD,RYY1,RYY2,RX3,RX4
 28      FORMAT('E1 N1 GND 0'/'OX1 N1 GND'/
     +   'VV1 4 GND V(OX1) C10(0.)'/
     +   'VV2 3 GND V(OX1) C10(1.5707963)'/
     +   'VV3 2 GND V(OX1) C10(3.1415927)'/
     +   'VV4 1 GND V(OX1) C10(4.712389)'/
     +   'O1 33 GND'/'O2 34 GND'/'O3 35 GND'/'O4 36 GND'/
     +   'RA 33 57 ',F7.0/'RB 34 57 ',F7.0/
     +   'RC 35 59 ',F7.0/'RD 36 59 ',F7.0/
     +  'MXX1 OPAMP 57 B200 B200 GND / RIN=*RR , GAIN=*GA , GBW=*GG5'/
     +  'MXX2 OPAMP 59 B100 B100 GND / RIN=*RR , GAIN=*GA , GBW=*GG6'/
     +   'RYY1 B200 200 ',F7.0/
     +   'RYY2 B100 100 ',F7.0/
     +   'RX3 100 GND ',F7.0/
     +   'RX4 200 300 ',F7.0/
     +  'MXX3 OPAMP 200 100 300 GND / RIN=*RR , GAIN=*GA , GBW=*GG7')
         WRITE(2,29)
 29      FORMAT('$PORT *OUT = NV(300)/E1 DBL AREF(-1004.,-1004.) S'/
C    +   '$DELAY *DEL = NV(33)/E1 DBL DREF(2200.,2200.)'/
     +   '$FREQ SP  175. 300. 600. 900. 1200. 1500. 1800. 2100.'/
     +   '$FREQ SP 2400. 2700. 3000. 3300. 3700.'/
C    +   '$FREQ SP -300. -400. -2000. -3000. -3200. -3300. -3400.'/
C    +   '$FREQ SP -1004. 2200.'/'$ANAL')
     +   '$FREQ SP -1004.'/'$ANAL')
         GO TO 200
 100     WRITE(2,31) RS1,RS2,RS3,RS4
 31      FORMAT('*RS1= ',F7.0/'*RS2= ',F7.0/'*RS3= ',F7.0/'*RS4= ',
     +    F7.0 )
         WRITE(2,32) C11,C12,C13,C14
 32      FORMAT('*C11= ',E12.6/'*C12= ',E12.6/'*C13= ',E12.6/
     +   '*C14= ',E12.6)
         WRITE(2,33) R11,R12,R13,R14
 33      FORMAT('*R11= ',F7.0/'*R12= ',F7.0/'*R13= ',F7.0/'*R14= ',
     +    F7.0 )
         WRITE(2,34) C21,C22,C23,C24
 34      FORMAT('*C21= ',E12.6/'*C22= ',E12.6/'*C23= ',E12.6/
     +        '*C24= ',E12.6)
         WRITE(2,35) R21,R22,R23,R24
 35      FORMAT('*R21= ',F7.0/'*R22= ',F7.0/'*R23= ',F7.0/'*R24= ',
     +    F7.0 )
         WRITE(2,36) C31,C32,C33,C34
```

```
36    FORMAT('*C31= ',E12.6/'*C32= ',E12.6/'*C33= ',E12.6/
     +       '*C34= ',E12.6)
      WRITE(2,37) R31,R32,R33,R34
37    FORMAT('*R31= ',F7.0/'*R32= ',F7.0/'*R33= ',F7.0/'*R34= ',
     +   F7.0 )
      WRITE(2,38) C41,C42,C43,C44
38    FORMAT('*C41= ',E12.6/'*C42= ',E12.6/'*C43= ',E12.6/
     +       '*C44= ',E12.6)
      WRITE(2,39) R41,R42,R43,R44
39    FORMAT('*R41= ',F7.0/'*R42= ',F7.0/'*R43= ',F7.0/'*R44= ',
     +   F7.0 )
      WRITE(2,40) C51,C52,C53,C54
40    FORMAT('*C51= ',E12.6/'*C52= ',E12.6/'*C53= ',E12.6/
     +       '*C54= ',E12.6)
      WRITE(2,41) R51,R52,R53,R54
41    FORMAT('*R51= ',F7.0/'*R52= ',F7.0/'*R53= ',F7.0/'*R54= ',
     +   F7.0 )
      WRITE(2,42) C61,C62,C63,C64
42    FORMAT('*C61= ',E12.6/'*C62= ',E12.6/'*C63= ',E12.6/
     +       '*C64= ',E12.6)
      WRITE(2,43) R61,R62,R63,R64
43    FORMAT('*R61= ',F7.0/'*R62= ',F7.0/'*R63= ',F7.0/'*R64= ',
     +   F7.0 )
      WRITE(2,44) C71,C72,C73,C74
44    FORMAT('*C71= ',E12.6/'*C72= ',E12.6/'*C73= ',E12.6/
     +       '*C74= ',E12.6)
      WRITE(2,45) R71,R72,R73,R74
45    FORMAT('*R71= ',F7.0/'*R72= ',F7.0/'*R73= ',F7.0/'*R74= ',
     +   F7.0 )
      WRITE(2,46) RG1,RG2,RG3,RG4
46    FORMAT('*RG1= ',F7.0/'*RG2= ',F7.0/'*RG3= ',F7.0/'*RG4= ',
     +   F7.0 )
      WRITE(2,47) GG1,GG2,GG3,GG4,GG5,GG6,GG7
47    FORMAT('*GG1= ',E12.6/'*GG2= ',E12.6/'*GG3= ',E12.6/
     +  '*GG4= ',E12.6/'*GG5= ',E12.6/'*GG6= ',E12.6/'*GG7= ',
     +  E12.6 )
      WRITE(2,48) RA,RB,RC,RD,RYY1,RYY2,RX3,RX4
48    FORMAT('*RA= ',F7.0/'*RB= ',F7.0/'*RC= ',F7.0/
     +  '*RD= ',F7.0/'*RYY1= ',F7.0/'*RYY2= ',F7.0/
     +  '*RX3= ',F7.0/'*RX4= ',F7.0 )
      WRITE(2,49)
49    FORMAT('$ANAL')
200     CONTINUE
500    STOP
       END
```

```
      FUNCTION XTO2(X1,X2)
      IMPLICIT REAL*8(A-H,O-Z)
      LOGICAL FRSTW/.TRUE./
      IF(FRSTW) CALL RAND(-700)
      IF(FRSTW) WRITE(5,111)
      IF(FRSTW) WRITE(8,111)
  111 FORMAT(' -----   MUMTAZ',4H'S  ,' STATISTICS METHOD ( XTO2 )',
     +     '  ------ ')
      FRSTW=.FALSE.
      ANOM=X1
      TOL=X2
      XX=RAND(2)
C     WRITE(5,11)XX
   11 FORMAT('  XX = ',F12.4)
      XA=TOL/100.D0
      XB=1.D0+XA*(XX-1.D0)
      XTO2=ANOM*XB
      RETURN
      END
```

```
      SUBROUTINE F51(N,X,Y)
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION X(3) ,Y(2)
      LOGICAL FRSTW/.TRUE./
      IF(FRSTW) CALL RAND(-700)
      FRSTW=.FALSE.
      IF(N.NE.0) GO TO 10
      AAA=X(1)*X(2)
      TOLP=X(3)/100.D0
      IF(AAA.LE.1.D-20)  AAA=1.D-20
      Y(1)=(1.D0+TOLP*(RAND(2)-1.D0))/AAA
      Y(2)=0.D0
      RETURN
10    AAA=X(1)*X(2)
      IF(AAA.LE.1.D-20)  AAA=1.D-20
      Y(1)=(1.D0+TOLP*(RAND(2)-1.D0))/AAA
      Y(2)=0.D0
      IF(N.EQ.-1) GO TO 100
      IF(N.EQ.-2) GO TO 200
      RETURN
100   Y(1)=-Y(1)/X(1)
      Y(2)=0.D0
      RETURN
200   Y(1)=-Y(1)/X(2)
      Y(2)=0.D0
      RETURN
      END
```

```
FUNCTION F51B(X1,X2,X3)
IMPLICIT REAL*8(A-H,O-Z)
LOGICAL FRSTW/.TRUE./
IF(FRSTW) CALL RAND(-700)
FRSTW=.FALSE.
AAA=X1*X2
TOLP=X3/100.D0
IF(AAA.LE.1.D-20)  AAA=1.D-20
F51B=(1.D0+TOLP*(RAND(2)-1.D0))/AAA
RETURN
END
```

```
      SUBROUTINE XTOL(N,X,Y)
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION X(2),Y(2)
      LOGICAL FRSTW/.TRUE./
      IF(FRSTW) CALL RAND(-200)
      IF(FRSTW) WRITE(5,111)
      IF(FRSTW) WRITE(8,111)
  111 FORMAT(' -----   MUMTAZ',4H'S  ,' STATISTICS METHOD  ------ ')
      FRSTW=.FALSE.
      ANOM=X(1)
      TOL=X(2)
      XX=RAND(2)
C     WRITE(5,11)XX
   11 FORMAT('  XX = ',F12.4)
      XA=TOL/100.D0
      XB=1.D0+XA*(XX-1.D0)
      Y(1)=ANOM*XB
      Y(2)=0.D0
      RETURN
      END
```

```
      SUBROUTINE C10(N,X,Y)
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION Y(2)
      IF(N.NE.0) GO TO 111
      Y(1)=DCOS(X)
      Y(2)=DSIN(X)
C     WRITE(5,20) N,X,Y
      N=2
      RETURN
111   Y(1)=DCOS(X)
      Y(2)=DSIN(X)
C     WRITE(5,20) N,X,Y
 20   FORMAT(2X,I5,2X,F12.4,2X,2(F12.4,2X))
      RETURN
      END
```

```
      SUBROUTINE C12(N,X,Y)
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION X(2),Y(2)
      LOGICAL FRSTW/.TRUE./
      IF(FRSTW) CALL RAND(-200)
      FRSTW=.FALSE.
      ANOM=X(1)
      TOL=X(2)
      XX=RAND(2)
      XA=TOL/100.D0
      XB=1.D0+XA*(XX-1.D0)
      Y11=ANOM*XB
      IF(N.NE.0) GO TO 111
      Y(1)=DCOS(Y11)
      Y(2)=DSIN(Y11)
C     WRITE(5,20) N,Y11,X,Y
      N=2
      RETURN
 111  IF(N.EQ.-1) GO TO 112
      Y(1)=DCOS(Y11)
      Y(2)=DSIN(Y11)
C     WRITE(5,20) N,Y11,X,Y
 20   FORMAT(2X,I5,1X,F9.4,4(1X,F9.4))
      RETURN
 112  Y(1)=-DSIN(Y11)
      Y(2)=DCOS(Y11)
      RETURN
      END
```

```
C-------      RSD7  FORTRAN  FILE      -------
C
C
      IMPLICIT REAL*8 (A-H,O-Z)
      DIMENSION A1(999),B1(999),ALOS1(999),ALOS2(999),ALOS(999)
      REAL*4 TEXT(3),A(20)
      LOGICAL FLAG
      DATA X/'X'/,   BLANK/' '/
C
      DATA  TEXT(1)/'-100'/
      DATA  TEXT(2)/'4.00'/
      DATA  TEXT(3)/'    '/
C
      WRITE(5,117)
  117 FORMAT(' ENTER NO. OF RUNS ')
      READ(5,*,END=500) NMAX
      DO 999 KKK=1,NMAX
      DO 30 K=1,1000
      READ(1,12,END=500) (A(I),I=1,20)
   12 FORMAT(20A4)
      FLAG=.TRUE.
      DO 60 I=1,3
      IF(A(I).NE.TEXT(I)) FLAG=.FALSE.
   60 CONTINUE
      IF(FLAG) GOTO 20
   30 CONTINUE
   20 DO 21 K=1,12
      READ(1,*) A1(K),B1(K)
   21 CONTINUE
      SUM=DABS(B1(3))
      DO 40 K=4,12
      SUM=SUM+DABS(B1(K))
   40 CONTINUE
      AVER1=SUM/10.0
      ALOS(KKK)=AVER1
   50 FORMAT(' AVERAGE LOSS BETWEEN 600 , 3300 HZ ' )
  999 CONTINUE
      WRITE(2,103)
  103 FORMAT('      POLY-PHASE FILTER '//)
      WRITE(5,50)
      WRITE(2,50)
      WRITE(5,102) (ALOS(I),I=1,NMAX)
      WRITE(2,102) (ALOS(I),I=1,NMAX)
      CALL STAT1(NMAX,ALOS,AVER,SIG,ALOS1,ALOS2)
      WRITE(5,101) AVER,SIG
      WRITE(2,101) AVER,SIG
  101 FORMAT(/'   AVERAGE = ',F6.2,'  SIG = ',F8.4//)
      WRITE(5,102) (ALOS1(I),I=1,NMAX)
      WRITE(2,102) (ALOS1(I),I=1,NMAX)
  102 FORMAT(10(1X,F6.2))
  500 STOP
      END
```

```
C--------      RSD7B  FORTRAN  FILE      -------
C
C
      IMPLICIT REAL*8 (A-H,O-Z)
      DIMENSION ALOS1(999),ALOS2(999),ALOS(999)
      DIMENSION FA(99),CCC(999,99)
      REAL*4 TEXT(3),A(20)
      LOGICAL FLAG
      DATA X/'X'/,   BLANK/' '/
C
      DATA  TEXT(1)/'    '/
      DATA  TEXT(2)/'  HZ'/
      DATA  TEXT(3)/'    '/
      WRITE(5,117)
 117  FORMAT(' ENTER NO. OF RUNS , NO. OF FREQ. POINTS ')
      READ(5,*,END=500) NMAX,NF
      DO 999 KKK=1,NMAX
      DO 30 K=1,1000
      READ(1,12,END=500) (A(I),I=1,20)
 12   FORMAT(20A4)
      FLAG=.TRUE.
      DO 60 I=1,3
      IF(A(I).NE.TEXT(I)) FLAG=.FALSE.
 60   CONTINUE
      IF(FLAG) GOTO 20
 30   CONTINUE
 20   DO 21 K1=1,NF
      READ(1,*) FA(K1),CCC(KKK,K1)
 21   CONTINUE
 999  CONTINUE
      DO 118 K1=1,NF
      DO 120 KKK=1,NMAX
      ALOS(KKK)=CCC(KKK,K1)
 120  CONTINUE
 50   FORMAT('  LOSS  AT '  ,F9.1,' HZ'/)
      IF(DABS(FA(K1)+1004.).LE.1.) GO TO 118
      WRITE(2,103)
 103  FORMAT(1H1/'      POLY-PHASE FILTER '//)
      WRITE(5,50)  FA(K1)
      WRITE(2,50)  FA(K1)
      WRITE(5,102)  (ALOS(I),I=1,NMAX)
      WRITE(2,102)  (ALOS(I),I=1,NMAX)
      CALL STAT1(NMAX,ALOS,AVER,SIG,ALOS1,ALOS2)
      WRITE(5,101) AVER,SIG
      WRITE(2,101) AVER,SIG
 101  FORMAT(/'   AVERAGE = ',F6.2,'  SIG = ',F8.4//)
      WRITE(5,102)  (ALOS1(I),I=1,NMAX)
      WRITE(2,102)  (ALOS1(I),I=1,NMAX)
 102  FORMAT(10(1X,F6.2))
 118  CONTINUE
 500  STOP
      END
```

```
C-------      RSD7C  FORTRAN  FILE      -------
C
      IMPLICIT REAL*8 (A-H,O-Z)
      DIMENSION ALOS1(999),ALOS2(999),ALOS(999)
      DIMENSION FA(99),CCC(999,99)
      REAL*4 TEXT(3),A(20)
      LOGICAL FLAG
      DATA X/'X'/,   BLANK/' '/
      DATA  TEXT(1)/'    '/
      DATA  TEXT(2)/'  HZ'/
      DATA  TEXT(3)/'    '/
      WRITE(5,117)
 117  FORMAT(' ENTER NO. OF RUNS , NO. OF FREQ. POINTS ')
      READ(5,*,END=500) NMAX,NF
      NF1=NF-1
      NF2=(NF-2)/10+1
      NF3=50/NF2
      DO 999 KKK=1,NMAX
      DO 30 K=1,1000
      READ(1,12,END=500) (A(I),I=1,20)
 12   FORMAT(20A4)
      FLAG=.TRUE.
      DO 60 I=1,3
      IF(A(I).NE.TEXT(I)) FLAG=.FALSE.
 60   CONTINUE
      IF(FLAG) GOTO 20
 30   CONTINUE
 20   DO 21 K1=1,NF1
 777  READ(1,*) FA(K1),CCC(KKK,K1)
      IF(DABS(FA(K1)+1004.).LE.1.) GO TO 777
 21   CONTINUE
 999  CONTINUE
 105  FORMAT('    CKT',10(1X,F6.0),(/7X,10(1X,F6.0)))
      DO 120 KKK=1,NMAX
      IF(MOD(KKK,NF3).EQ.1) WRITE(2,103)
      IF(MOD(KKK,NF3).EQ.1) WRITE(5,103)
      IF(MOD(KKK,NF3).EQ.1) WRITE(2,105) (FA(I1),I1=1,NF1)
      IF(MOD(KKK,NF3).EQ.1) WRITE(5,105) (FA(I1),I1=1,NF1)
      IF(MOD(KKK,NF3).EQ.1.AND.NF3.NE.50) WRITE(2,106)
      IF(MOD(KKK,NF3).EQ.1.AND.NF3.NE.50) WRITE(5,106)
 106  FORMAT( .)
      IF(NF3.EQ.50) WRITE(2,151) KKK,(CCC(KKK,K2),K2=1,NF1)
      IF(NF3.EQ.50) WRITE(5,151) KKK,(CCC(KKK,K2),K2=1,NF1)
      IF(NF3.NE.50) WRITE(5,150) KKK,(CCC(KKK,K2),K2=1,NF1)
      IF(NF3.NE.50) WRITE(2,150) KKK,(CCC(KKK,K2),K2=1,NF1)
 150  FORMAT(1X,I5,10(1X,F6.2),(/6X,10(1X,F6.2)))
 151  FORMAT(1X,I5,10(1X,F6.2))
 120  CONTINUE
 103  FORMAT('1    POLY-PHASE FILTER '/)
 118  CONTINUE
 500  STOP
      END
```

```
C--------      RSD7E  FORTRAN  FILE      -------
C
C
      IMPLICIT REAL*8 (A-H,O-Z)
      DIMENSION A1(999),B1(999),ALOS1(999),ALOS2(999),ALOS(999)
      REAL*4 TEXT(3),A(20)
      LOGICAL FLAG
      DATA X/'X'/,   BLANK/' '/
C
      DATA  TEXT(1)/'-100'/
      DATA  TEXT(2)/'4.00'/
      DATA  TEXT(3)/'    '/
      WRITE(5,117)
  117 FORMAT(' ENTER NO. OF RUNS ')
      READ(5,*,END=500) NMAX
      DO 999 KKK=1,NMAX
      DO 30 K=1,1000
      READ(1,12,END=500)  (A(I),I=1,20)
   12 FORMAT(20A4)
      FLAG=.TRUE.
      DO 60 I=1,3
      IF(A(I).NE.TEXT(I)) FLAG=.FALSE.
   60 CONTINUE
      IF(FLAG) GOTO 20
   30 CONTINUE
   20 DO 21 K=1,12
      READ(1,*) A1(K),B1(K)
      B1(K)=DEXP(-.23025851D0*B1(K))
   21 CONTINUE
      SUM=DABS(B1(3))
      DO 40 K=4,12
      SUM=SUM+DABS(B1(K))
   40 CONTINUE
      AVER1=SUM/10.D0
      ALOS(KKK)=-10.D0*DLOG10(AVER1)
   50 FORMAT(' AVERAGE LOSS BETWEEN 600 , 3300 HZ '/  )
  999 CONTINUE
      WRITE(2,103)
  103 FORMAT('       POLY-PHASE FILTER '//)
      WRITE(5,50)
      WRITE(2,50)
      WRITE(5,102)  (ALOS(I),I=1,NMAX)
      WRITE(2,102)  (ALOS(I),I=1,NMAX)
      CALL STAT1(NMAX,ALOS,AVER,SIG,ALOS1,ALOS2)
      WRITE(5,101)  AVER,SIG
      WRITE(2,101)  AVER,SIG
  101 FORMAT(/'   AVERAGE = ',F6.2,'  SIG = ',F8.4//)
      WRITE(5,102)  (ALOS1(I),I=1,NMAX)
      WRITE(2,102)  (ALOS1(I),I=1,NMAX)
  102 FORMAT(10(1X,F6.2))
  500 STOP
      END
```

```
C-------      POWER  FORTRAN      -------
C
C
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION A(10),B(10)
 1    WRITE(5,10)
 10   FORMAT(' ENTER  LOSSES AT 600 TO 3300 HZ ')
      READ(5,*,END=500) ( A(I),I=1,10)
      SUM=0.D0
      DO 20 K=1,10
      A(K)=DEXP(-.23025851D0*A(K))
      SUM=SUM+A(K)
 20   CONTINUE
      ALOSS=-10.D0*DLOG10(SUM/10.D0)
      WRITE(5,30) ALOSS
 30   FORMAT(' LOSS BASED ON AVERAGE POWER = ',F12.2)
      GO TO 1
 500  STOP
      END
```

```
C-------      AB1X  FORTRAN  FILE      -------
C
C
      IMPLICIT REAL*8(A-H,O-Z)
      EXTERNAL AB3
      COMPLEX*16 AA,BB,CC,DD
      PI=4.D0*DATAN(1.D0)
 1    WRITE(5,10)
 10   FORMAT(' ENTER R,C, HIT RETURN TO STOP ')
      READ(5,*,END=500) R,C
      FF1=.0000001+1.D0/(2.D0*PI*R*C)
CCC 2      WRITE(5,17)
CCC 17     FORMAT(' ENTER F , TO CHANGE R,C ENTER 0')
CCC        READ(5,*,END=500) F.
CCC        IF(F.EQ.0) GO TO 1
       DO 20 I=1,165
       F=-8100.+(I-1)*100.D0
       IF(I.EQ.1) F=-1.D8
       IF(I.EQ.163) F=FF1
       IF(I.EQ.164) F=-FF1
       IF(I.EQ.165) F=1.D8
C      DO 20 I=1,37
CC      F=-8000.+(I-5)*500.D0
CC      IF(I.EQ.1)  F=-1.D8
CC      IF(I.EQ.2)  F=FF1
CC      IF(I.EQ.3)  F=-FF1
CC      IF(I.EQ.4)  F=1.D8
      IF(F.LT.0.) CALL AB1(R,C,F,AA,BB,CC,DD)
      IF(F.GE.0.) CALL AB2(R,C,F,AA,BB,CC,DD)
      ALOS=20.D0*DLOG10(CDABS(AA))
      APHASE=180.D0*DATAN2(DIMAG(AA),DREAL(AA))/PI
      BB1=DREAL(BB)
      BB2=DIMAG(BB)
      CC1=DREAL(CC)
      CC2=DIMAG(CC)
      WRITE(5,40) F,ALOS,APHASE
      WRITE(8,40) F,ALOS,APHASE,CC1,CC2
 40   FORMAT(1X,F14.2,3X,F8.2,2(3X,E10.3),3X,E10.3,1X,E10.3)
 20   CONTINUE
CCC      GO TO 2
 500  STOP
      END
```

```
C-------      AB2X  FORTRAN  FILE      -------
C
C
      IMPLICIT REAL*8(A-H,O-Z)
      EXTERNAL AB6
      COMPLEX*16 AA,BB,CC,DD
      PI=4.D0*DATAN(1.D0)
 1    WRITE(5,10)
 10   FORMAT(' ENTER R,R7,C , HIT RETURN TO STOP ')
      READ(5,*,END=500) R,R7,C
      FF1=.0000001+1.D0/(2.D0*PI*R*C)
      IDEL=FF1/300.
      IF(FF1.LE.300.) IDEL=1
      IF1=FF1
      DO 20 I=1,55
      F=IF1+(I-26)*IDEL
      IF(I.EQ.52) F=FF1-1.
      IF(I.EQ.53)  F=FF1
      IF(I.EQ.54) F=FF1+1.
      IF(I.EQ.55) F=1.D8
      CALL AB5(R,R7,C,F,AA,BB,CC,DD)
      ALOS=20.D0*DLOG10(CDABS(AA))
      APHASE=180.D0*DATAN2(DIMAG(AA),DREAL(AA))/PI
      BB1=DREAL(BB)
      BB2=DIMAG(BB)
      CC1=DREAL(CC)
      CC2=DIMAG(CC)
      WRITE(8,40) F,ALOS,APHASE
C40   FORMAT(1X,F14.2,3X,F8.2,2(3X,E10.3),3X,E10.3,1X,E10.3)
 40   FORMAT(5X,F14.2,2X,F8.2,8X,F12.2)
 20   CONTINUE
      GO TO 1
 500  STOP
      END
```

```
      SUBROUTINE AB3(R,C,F,AA,BB,CC,DD)
      IMPLICIT REAL*8(A-H,O-Z)
      COMPLEX*16 AA,BB,CC,DD
      IF(F.LT.0.) CALL AB1(R,C,F,AA,BB,CC,DD)
      IF(F.GE.0.) CALL AB2(R,C,F,AA,BB,CC,DD)
      ALOS=20.D0*DLOG10(CDABS(AA))
      RETURN
      END
       SUBROUTINE AB1(R,C,F,A1,B1,C1,D1)
       IMPLICIT REAL*8(A-H,O-Z)
       COMPLEX*16 A1,B1,C1,D1
       PI=4.D0*DATAN(1.D0)
       W=2.D0*PI*F
       G1=1.D0/R
       DEN1=G1-W*C
       A1=DCMPLX(G1,W*C)/DEN1
       B1=DCMPLX(1.D0,0.D0)/DEN1
       C1=DCMPLX(0.D0,2.D0*W*C*G1)/DEN1
       D1=DCMPLX(G1,W*C)/DEN1
      RETURN
      END
       SUBROUTINE AB2(R,C,F,A2,B2,C2,D2)
       IMPLICIT REAL*8(A-H,O-Z)
       COMPLEX*16 A2,B2,C2,D2
       PI=4.D0*DATAN(1.D0)
       W=2.D0*PI*F
       G1=1.D0/R
       DEN2=G1-W*C
      A2=DCMPLX(G1,W*C)/DEN2
      B2=DCMPLX(1.D0,0.D0)/DEN2
      C2=DCMPLX(0.D0,2.D0*W*C*G1)/DEN2
      D2=DCMPLX(G1,W*C)/DEN2
      RETURN
      END
```

```
C-------     AB3X  FORTRAN  FILE     -------
C
C
      IMPLICIT REAL*8(A-H,O-Z)
      EXTERNAL AB6
      COMPLEX*16 AA1,AA2,AA,BB,CC,DD
      DIMENSION AAA(34)
      PI=4.D0*DATAN(1.D0)
 1    WRITE(5,10)
 10   FORMAT(' ENTER R,RG,C,FR , HIT RETURN TO STOP ')
      READ(5,*,END=500) R,RG,C,FR
      FF1=.0000001+1.D0/(2.D0*PI*R*C)
      CALL AB4(R,RG,C,FR,AA,BB,CC,DD)
      IF(FR.GT.0) CALL AB5(R,RG,C,FR,AA,BB,CC,DD)
      ALOS1=20.D0*DLOG10(CDABS(AA))
      WRITE(8,17) R,RG,C,FR,ALOS1
 17   FORMAT('1','   R = ',E12.4,5X,' RG = ',E12.4,5X,' C = ',E12.4//
     + 3X,' REF. FREQUENCY = ',F12.4,7X,' LOSS = ',F12.4,' D.B.'//,
     +  8X,' FRQ. HZ',9X,'LOSS DB',8X,'DEGREES'/)
      DO 20 I=1,37
      F=-3400.+(I-3)*100.
      IF(I.EQ.1)  F=-FF1
      IF(I.EQ.2)  F=-250.
      CALL AB4(R,RG,C,F,AA,BB,CC,DD)
      ALOS=20.D0*DLOG10(CDABS(AA))-ALOS1
      IF(I.LE.34) AAA(I)=ALOS
      APHASE=180.D0*DATAN2(DIMAG(AA),DREAL(AA))/PI
      BB1=DREAL(BB)
      BB2=DIMAG(BB)
      CC1=DREAL(CC)
      CC2=DIMAG(CC)
      IF(MOD(I,4).EQ.0.AND.F.GE.-3400..AND.F.LE.0.) WRITE(5,40) F,ALO
      WRITE(8,40) F,ALOS,APHASE
 40   FORMAT(2X,F14.2,2(3X,F12.2))
 20   CONTINUE
      CALL MAX(34,AAA,AMAX)
      CALL MIN(34,AAA,AMIN)
      DIFF=AMAX-AMIN
      WRITE(5,18) AMAX,AMIN,DIFF
      WRITE(8,18) AMAX,AMIN,DIFF
 18   FORMAT(2X,' AMAX ',F12.3,3X,' AMIN ',F12.3,3X,' DIFF. = ',F12.3
      GO TO 1
 500  STOP
      END
```

```
C-------      AB4X  FORTRAN  FILE      -------
C
C
C
      IMPLICIT REAL*8(A-H,O-Z)
      EXTERNAL AB6
      COMPLEX*16 AA1,AA2,AA,BB,CC,DD
      PI=4.D0*DATAN(1.D0)
1     WRITE(5,10)
10    FORMAT(' ENTER R,RG,C,FR , HIT RETURN TO STOP ')
      READ(5,*,END=500) R,RG,C,FR
      FF1=.0000001+1.D0/(2.D0*PI*R*C)
      CALL AB4(R,RG,C,FR,AA,BB,CC,DD)
      IF(FR.GT.0)  CALL AB5(R,RG,C,FR,AA,BB,CC,DD)
      ALOS1=20.D0*DLOG10(CDABS(AA))
      WRITE(8,17) R,RG,C,FR,ALOS1
17    FORMAT('1','   R = ',E12.4,5X,' RG = ',E12.4,5X,' C = ',E12.4//
     + 3X,' REF. FREQUENCY = ',F12.4,7X,' LOSS = ',F12.4,' D.B.'//,
     +  8X,' FRQ. HZ',9X,'LOSS DB',8X,'DEGREES'/)
      DO 20 I=1,43
      F=(I-1)*100.
      IF(I.EQ.42)  F=FF1
      IF(I.EQ.43)  F=1.D8
      CALL AB5(R,RG,C,F,AA,BB,CC,DD)
      ALOS=20.D0*DLOG10(CDABS(AA))-ALOS1
      APHASE=180.D0*DATAN2(DIMAG(AA),DREAL(AA))/PI
      BB1=DREAL(BB)
      BB2=DIMAG(BB)
      CC1=DREAL(CC)
      CC2=DIMAG(CC)
      WRITE(8,40) F,ALOS,APHASE
40    FORMAT(2X,F14.2,2(3X,F12.2))
20    CONTINUE
      GO TO 1
500   STOP
      END
```

```
      SUBROUTINE AB6(R,R7,C,F,AA,BB,CC,DD)
      IMPLICIT REAL*8(A-H,O-Z)
      COMPLEX*16 AA,BB,CC,DD
      IF(F.LT.0.) CALL AB4(R,R7,C,F,AA,BB,CC,DD)
      IF(F.GE.0.) CALL AB5(R,R7,C,F,AA,BB,CC,DD)
      ALOS=20.D0*DLOG10(CDABS(AA))
      RETURN
      END
       SUBROUTINE AB4(R,R7,C,F,A1,B1,C1,D1)
       IMPLICIT REAL*8(A-H,O-Z)
       COMPLEX*16 A1,B1,C1,D1
       PI=4.D0*DATAN(1.D0)
       W=2.D0*PI*F
       G1=1.D0/R
       G7=1.D0/R7
       DEN1=G1-W*C
       A1=DCMPLX((G1+G7),W*C)/DEN1
       B1=DCMPLX(1.D0,0.D0)/DEN1
       C1=DCMPLX(G1*G7,2.D0*W*C*(G1+G7))/DEN1
       D1=DCMPLX(G1,W*C)/DEN1
      RETURN
      END
       SUBROUTINE AB5(R,R7,C,F,A2,B2,C2,D2)
       IMPLICIT REAL*8(A-H,O-Z)
       COMPLEX*16 A2,B2,C2,D2
       PI=4.D0*DATAN(1.D0)
       W=2.D0*PI*F
       G1=1.D0/R
       G7=1.D0/R7
       DEN2=G1-W*C
      A2=DCMPLX((G1+G7),W*C)/DEN2
      B2=DCMPLX(1.D0,0.D0)/DEN2
      C2=DCMPLX(G1*G7,2.D0*W*C*(G1+G7))/DEN2
      D2=DCMPLX(G1,W*C)/DEN2
      RETURN
      END
```

```
**--------      RR1 EXEC      -------
**
**
&CONTROL OFF
COPY &1 OUT A (LRECL 130 RECFM F
**FI 1 CLEAR
FI 1 DISK &1 OUT A (LRECL 130 RECFM F BLKSIZE 130
LOAD &2
START
&EXIT
```

Appendix 2

SAMPLE DATA FILES

APPENDIX 2

SAMPLE DATA FILES

1 - SD7KM

Data file for analysis of the seven-stage buffered polyphase network in the transmit direction. Nominal component values.

2 - SD7RM

Data file for analysis of the seven-stage buffered polyphase network in the receive direction. Nominal component values.

3 - SD7KN

A sample data file generated from POLTX program, which contains a randomly generated circuit for the analysis of the seven-stage buffered polyphase network in the transmit direction.

4 - SD7RN

A sample data file generated for POLRX program, which contains a randomly generated circuit for the anlaysis of the seven-stage buffered polyphase network in the receive direction.

5 - SD7J4

A SCAMPER data file, in which the component values are randomly generated for specified tolerances in the components. The file is used to simulate the seven-stage buffered polyphase network in the transmit direction.

6 - SD7R9

A SCAMPER data file, in which the component values are randomly generated for specified tolerances in the components. The file is used to simulate the seven-stage buffered polyphase network in the receive direction.

7 - SD7K9

A SCAMPER data file to statistically analyze the seven-stage buffered polyphase network both in the pass-band and the stop-band.

8 - SD7J

A SCAMPER data file to simulate the trimming of the seven-stage buffered polyphase network in the transmit direction.

```
$*--------      SD7KM  DATA  FILE  (- TRANSMIT  SIDE  )      -------

$H  POLYPHASE FILTER TX   ( CASE XD6247 )
$P R11,R12,R13,R14,R21,R22,R23,R24,R31,R32,R33,R34,R41,R42,R43,R44
$P R51,R52,R53,R54,R61,R62,R63,R64,R71,R72,R73,R74
$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34,C41,C42,C43,C44
$P C51,C52,C53,C54,C61,C62,C63,C64,C71,C72,C73,C74
$P RG1,RG2,RG3,RG4,RS1,RS2,RS3,RS4
RS1  1  5 15.E3
RS2  2  6 15.E3
RS3  3  7 15.E3
RS4  4  8 15.E3
C11  5 10 2.2E-9
C12  6 11 2.2E-9
C13  7 12 2.2E-9
C14  8  9 2.2E-9
RI1  5  9 114.2238E3
R12  6 10 114.2238E3
R13  7 11 114.2238E3
R14  8 12 114.2238E3
SS1  9 13
SS2 10 14
SS3 11 15
SS4 12 16
C21 13 18 2.2E-9
C22 14 19 2.2E-9
C23 15 20 2.2E-9
C24 16 17 2.2E-9
R21 13 17 78.5707E3
R22 14 18 78.5707E3
R23 15 19 78.5707E3
R24 16 20 78.5707E3
SS5 17 21
SS6 18 22
SS7 19 23
SS8 20 24
C31 21 26 2.2E-9
C32 22 27 2.2E-9
C33 23 28 2.2E-9
C34 24 25 2.2E-9
R31 21 25 24.7573E3
R32 22 26 24.7573E3
R33 23 27 24.7573E3
R34 24 28 24.7573E3
SS9  25 29
SS10 26 30
SS11 27 31
SS12 28 32
C41 29 34 2.2E-9
C42 30 35 2.2E-9
C43 31 36 2.2E-9
```

```
C44 32 33 2.2E-9
R41 29 33 36.8923E3
R42 30 34 36.8923E3
R43 31 35 36.8923E3
R44 32 36 36.8923E3
SS13 33 37
SS14 34 38
SS15 35 39
SS16 36 40
C51 37 42 2.2E-9
C52 38 43 2.2E-9
C53 39 44 2.2E-9
C54 40 41 2.2E-9
R51 37 41 20.1095E3
R52 38 42 20.1095E3
R53 39 43 20.1095E3
R54 40 44 20.1095E3
SS17 41 45
SS18 42 46
SS19 43 47
SS20 44 48
C61 45 50 2.2E-9
C62 46 51 2.2E-9
C63 47 52 2.2E-9
C64 48 49 2.2E-9
R61 45 49 226.3894E3
R62 46 50 226.3894E3
R63 47 51 226.3894E3
R64 48 52 226.3894E3
C71 53 S58 2.2E-9
C72 54 S59 2.2E-9
C73 55 S60 2.2E-9
C74 56 S57 2.2E-9
R71 53 S57 42.4017E3
R72 54 S58 42.4017E3
R73 55 S59 42.4017E3
R74 56 S60 42.4017E3
RA S57 57 0.
RB S58 58 0.
RC S59 59 0.
RD S60 60 0.
$P RA,RB,RC,RD
MX1 OPAMP 49 53 53 GND / RIN=*RR , GAIN=*GA , GBW=*GG1
MX2 OPAMP 50 54 54 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
MX3 OPAMP 51 55 55 GND / RIN=*RR , GAIN=*GA , GBW=*GG3
MX4 OPAMP 52 56 56 GND / RIN=*RR , GAIN=*GA , GBW=*GG4
$P RR,GA,GG1,GG2,GG3,GG4
*RR=1.E12
*GA=2.E4
*GG1=1.E6
*GG2=1.E6
*GG3=1.E6
```

```
*GG4=1.E6
RG1 33 GND 35.5035E3
RG2 34 GND 35.5035E3
RG3 35 GND 35.5035E3
RG4 36 GND 35.5035E3
E1 N1 GND 0
VL 1 GND V(E1) 1.
V1 3 GND V(VL) -1.
V2 2 GND V(VL) 1.
V4 4 GND V(VL) -1.
VV1 A57 GND V(01) C10(0.)
VV2 A58 GND V(02) C10(1.5707963)
VV3 A59 GND V(03) C10(3.1415927)
VV4 A60 GND V(04) C10(4.712389)
VV5 100 GND V(05) V(06)  1. 1.
VV6 200 GND V(07) V(08)  1. 1.
VV7 300 GND V(09) V(010) 1. 1.
01 57 GND
02 58 GND
03 59 GND
04 60 GND
05 A57 GND
06 A58 GND
07 A59 GND
08 A60 GND
09 100 GND
010 200 GND
$PORT     *ONE=NV(57)/E1 DBL AREF (-1004.,-1004.)
$*DELAY *DEL1=NV(57)/E1 DBL DREF(2200.,2200.)
$*DELAY *DEL2=NV(58)/E1 DBL DREF(2200.,2200.)
$PORT     *TWO=NV(58)/E1 DBL AREF (-1004.,-1004.)
$PORT *OUT=NV(300)/E1 DBL AREF(-1004.,-1004.)    S
$FREQ SP -1004. 175. 300. 600. 900. 1200. 1500. 1800. 2100. 2200. 2400
$FREQ SP 2700. 3000. 3300. 3600. 3700.
$FREQ SP -250. -300. -400. -2000. -3000. -3100. -3200. -3300. -3400.
$SPEC(9)=-1
$ANAL
$TERM
```

```
$*-------     SD7RM  DATA  FILE  (  RECEIVE  SIDE  )     -------

$H  POLYPHASE FILTER RX          ( CAE XD6247 )
$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34
$P C41,C42,C43,C44,C51,C52,C53,C54,C61,C62,C63,C64,C71,C72,C73,C74
$P R11,R12,R13,R14,R21,R22,R23,R24,R31,R32,R33,R34
$P R41,R42,R43,R44,R51,R52,R53,R54,R61,R62,R63,R64,R71,R72,R73,R74
$P RG1,RG2,RG3,RG4
$P RX1,RX2,RX3,RX4
$P RZ1,RZ2,RZ3,RZ4
$P RS1,RS2,RS3,RS4
RS1  1  5 15.E3
RS2  2  6 15.E3
RS3  3  7 15.E3
RS4  4  8 15.E3
C11  5 10 2.2D-9
C12  6 11 2.2D-9
C13  7 12 2.2D-9
C14  8  9 2.2D-9
R11  5  9 114.2238D3
R12  6 10 114.2238D3
R13  7 11 114.2238D3
R14  8 12 114.2238D3
SS1  9 13
SS2 10 14
SS3 11 15
SS4 12 16
C21 13 18 2.2D-9
C22 14 19 2.2D-9
C23 15 20 2.2D-9
C24 16 17 2.2D-9
R21 13 17 78.5707D3
R22 14 18 78.5707D3
R23 15 19 78.5707D3
R24 16 20 78.5707D3
SS5 17 21
SS6 18 22
SS7 19 23
SS8 20 24
C31 21 26 2.2D-9
C32 22 27 2.2D-9
C33 23 28 2.2D-9
C34 24 25 2.2D-9
R31 21 25 24.7573D3
R32 22 26 24.7573D3
R33 23 27 24.7573D3
R34 24 28 24.7573D3
SS9  25 29
SS10 26 30
SS11 27 31
SS12 28 32
```

```
C41 29 34 2.2D-9
C42 30 35 2.2D-9
C43 31 36 2.2D-9
C44 32 33 2.2D-9
R41 29 33 36.8923D3
R42 30 34 36.8923D3
R43 31 35 36.8923D3
R44 32 36 36.8923D3
SS13 33 37
SS14 34 38
SS15 35 39
SS16 36 40
C51 37 42 2.2D-9
C52 38 43 2.2D-9
C53 39 44 2.2D-9
C54 40 41 2.2D-9
R51 37 41 20.1095D3
R52 38 42 20.1095D3
R53 39 43 20.1095D3
R54 40 44 20.1095D3
SS17 41 45
SS18 42 46
SS19 43 47
SS20 44 48
C61 45 50 2.2D-9
C62 46 51 2.2D-9
C63 47 52 2.2D-9
C64 48 49 2.2D-9
R61 45 49 226.3894D3
R62 46 50 226.3894D3
R63 47 51 226.3894D3
R64 48 52 226.3894D3
C71 53 58 2.2D-9
C72 54 59 2.2D-9
C73 55 60 2.2D-9
C74 56 57 2.2D-9
R71 53 57 42.4017D3
R72 54 58 42.4017D3
R73 55 59 42.4017D3
R74 56 60 42.4017D3
RA 57 61 0.
RB 58 61 0.
RC 59 62 0.
RD 60 62 0.
$P RA,RB,RC,RD
$P GG1,GG2,GA,RR
*RR=1.E12
*GA=2.E4
*GG1=2.E6
*GG2=1.D6
M1 OPAMP 49 53 53 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M2 OPAMP 50 54 54 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
```

```
M3 OPAMP 51 55 55 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M4 OPAMP 52 56 56 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
RG1 33 GND 35.5035D3
RG2 34 GND 35.5035D3
RG3 35 GND 35.5035D3
RG4 36 GND 35.5035D3
E1 N1 GND 0
OX1 N1 GND
VV1 4 GND V(OX1) C10(0.)
VV2 3 GND V(OX1) C10(1.5707963)
VV3 2 GND V(OX1) C10(3.1415927)
VV4 1 GND V(OX1) C10(4.712389)
O1 57 GND
O2 58 GND
O3 59 GND
O4 60 GND
MXX1 OPAMP 61 63 63 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
MXX2 OPAMP 62 64 64 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
RX1 63 100 50.E3
RX2 64 200 50.E3
RX3 200 GND 100.E3
RX4 100 300 100.E3
MXX3 OPAMP 100 200 300 GND / RIN=*RR , GAIN=*GA , GBW=*GG1
$PORT    *ONE=NV(57)/E1 DBL AREF (-1004.,-1004.)
$PORT    *TWO=NV(58)/E1 DBL AREF (-1004.,-1004.)
$*PORT   *THREE=NV(59)/E1 DBL AREF (-1004.,-1004.)
$*PORT   *FOUR=NV(60)/E1 DBL AREF (-1004.,-1004.)
$PORT *OUT=NV(300)/E1 DBL AREF(-1004.,-1004.)    S
$*DELAY *DELA=NV(300)/E1 DBL DREF(-2200.,-2200.) S
$FREQ SP   175. 300. 600. 900. 1200. 1500. 1800. 2100. 2400. 2700.
$FREQ SP 3000. 3300. 3700.
$FREQ SP   -300. -1004. -2200.  -2800. -3000.  -3400.
$SPEC(9)=-1
$ANAL
$TERM
```

```
$*-------     SD7KN  DATA  FILE  -------
$*-------     GENERATED FROM POLTX FORTRAN     -------


$H     POLYPHASE  TX NO.     1   ( CASE XD6247 )
$*   CAPACITOR TOLERANCES =   1.000 %
$* TC=    0.250 %          TR=   0.250 %          TG=  20.000
$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34
$P C41,C42,C43,C44,C51,C52,C53,C54,C61,C62,C63,C64
$P C71,C72,C73,C74
$P R11,R12,R13,R14,R21,R22,R23,R24,R31,R32,R33,R34
$P R41,R42,R43,R44,R51,R52,R53,R54,R61,R62,R63,R64
$P R71,R72,R73,R74
$P RS1,RS2,RS3,RS4,RG1,RG2,RG3,RG4
RS1   1   5   14972.
RS2   2   6   15006.
RS3   3   7   14986.
RS4   4   8   15011.
C11   5  10 0.218445D-08
C12   6  11 0.217855D-08
C13   7  12 0.221131D-08
C14   8   9 0.219688D-08
R11   5   9  114373.
R12   6  10  114342.
R13   7  11  114162.
R14   8  12  114497.
C21   9  14 0.219344D-08
C22  10  15 0.219092D-08
C23  11  16 0.220457D-08
C24  12  13   0.2221D-08
R21   9  13   78553.
R22  10  14   78724.
R23  11  15   78474.
R24  12  16   78577.
C31  13  18 0.221368D-08
C32  14  19 0.218755D-08
C33  15  20 0.217814D-08
C34  16  17 0.218091D-08
R31  13  17   24741.
R32  14  18   24771.
R33  15  19   24741.
R34  16  20   24779.
C41  17  22 0.221108D-08
C42  18  23 0.219812D-08
C43  19  24 0.222104D-08
C44  20  21 0.221111D-08
R41  17  21   36931.
R42  18  22   36893.
R43  19  23   36910.
R44  20  24   36813.
C51  21  26 0.218348D-08
C52  22  27 0.220163D-08
```

```
C53 23 28 0.219311D-08
C54 24 25 0.219898D-08
R51 21 25  20161.
R52 22 26  20285.
R53 23 27  20059.
R54 24 28  20150.
C61 25 80 0.221646D-08
C62 26 81 0.219219D-08
C63 27 82 0.218097D-08
C64 28 79 0.220013D-08
R61 25 79 226288.
R62 26 80 226886.
R63 27 81 226880.
R64 28 82 225997.
$P RR,GA,GG1,GG2,GG3,GG4
*RR=1.E10
*GA=2.E4
*GG1= 0.117726D+07
*GG2= 0.103838D+07
*GG3= 0.834918D+06
*GG4= 0.864079D+06
M1 OPAMP 79 29 29 GND / RIN=*RR , GAIN=*GA , GBW=*GG1
M2 OPAMP 80 30 30 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M3 OPAMP 81 31 31 GND / RIN=*RR , GAIN=*GA , GBW=*GG3
M4 OPAMP 82 32 32 GND / RIN=*RR , GAIN=*GA , GBW=*GG4
C71 29 34 0.220228D-08
C72 30 35 0.220968D-08
C73 31 36 0.221558D-08
C74 32 33 0.221723D-08
R71 29 33  42079.
R72 30 34  42374.
R73 31 35  42139.
R74 32 36  42130.
RG1 21 GND  35546.
RG2 22 GND  35528.
RG3 23 GND  35443.
RG4 24 GND  35455.
E1 N1 GND 0
VL 1 GND V(E1) 1.
V1 3 GND V(VL)   -0.9984
V2 2 GND V(VL) 1.
V4 4 GND V(VL)   -0.9984
VV1 A33 GND V(01) C10(0.)
VV2 A34 GND V(02) C10(1.5707963)
VV3 A35 GND V(03) C10(3.1415927)
VV4 A36 GND V(04) C10(4.712389)
VV5 100 GND V(05) V(06) 1. 1.
VV6 200 GND V(07) V(08) 1. 1.
VV7 300 GND V(09) V(010) 1. 1.
O1 33 GND
O2 34/GND
O3 35 GND
```

```
04 36 GND
05 A33 GND
06 A34 GND
07 A35 GND
08 A36 GND
09 100 GND
010 200 GND
$PORT *OUT = NV(300)/E1 DBL AREF(-1004.,-1004.)  S
$FREQ SP  175. 300. 600. 900. 1200. 1500. 1800. 2100.
$FREQ SP 2400. 2700. 3000. 3300.  3700.
$FREQ SP -1004.
$ANAL
```

```
$*-------      SD7RN  DATA  FILE      -------
$*-------      GENERATED FROM POLRX FORTRAN      -------

$H      POLYPHASE  RX NO.      1    ( CASE XD6247 )
$*    CAPACITOR TOLERANCES =    1.000 %
$* TC=    0.250 %          TR=    0.250 %          TG=   20.000 %
$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34
$P C41,C42,C43,C44,C51,C52,C53,C54,C61,C62,C63,C64
$P C71,C72,C73,C74
$P R11,R12,R13,R14,R21,R22,R23,R24,R31,R32,R33,R34
$P R41,R42,R43,R44,R51,R52,R53,R54,R61,R62,R63,R64
$P R71,R72,R73,R74
$P RA,RB,RC,RD,RYY1,RYY2,RX3,RX4
$P RS1,RS2,RS3,RS4,RG1,RG2,RG3,RG4
RS1   1  5    14972.
RS2   2  6   15006.
RS3   3  7   14986.
RS4   4  8   15011.
C11   5 10 0.218282D-08
C12   6 11 0.217630D-08
C13   7 12 0.221246D-08
C14   8  9 0.220217D-08
R11   5  9 114536.
R12   6 10 115157.
R13   7 11 115286.
R14   8 12 113912.
C21   9 14 0.219652D-08
C22  10 15 0.221841D-08
C23  11 16 0.218771D-08
C24  12 13   0.2203D-08
R21   9 13   78667.
R22  10 14   78532.
R23  11 15   77769.
R24  12 16   78788.
C31  13 18 0.220596D-08
C32  14 19 0.219928D-08
C33  15 20 0.221881D-08
C34  16 17 0.220950D-08
R31  13 17   24659.
R32  14 18   24633.
R33  15 19   24790.
R34  16 20   24470.
C41  17 22 0.220092D-08
C42  18 23 0.219266D-08
C43  19 24 0.219157D-08
C44  20 21 0.218245D-08
R41  17 21   37256.
R42  18 22   36896.
R43  19 23   37015.
R44  20 24   37045.
C51  21 26 0.219726D-08
```

```
C52 22 27 0.221871D-08
C53 23 28 0.221590D-08
C54 24 25 0.218213D-08
R51 21 25  20252.
R52 22 26  20170.
R53 23 27  19961.
R54 24 28  19978.
C61 25 80 0.221051D-08
C62 26 81 0.219751D-08
C63 27 82 0.221154D-08
C64 28 79 0.219286D-08
R61 25 79 227013.
R62 26 80 225966.
R63 27 81 226369.
R64 28 82 224439.
$P RR,GA,GG1,GG2,GG3,GG4,GG5,GG6,GG7
*RR=1.E10
*GA=2.E4
*GG1= 0.117687D+07
*GG2= 0.114893D+07
*GG3= 0.110173D+07
*GG4= 0.106998D+07
*GG5= 0.904338D+06
*GG6= 0.996168D+06
*GG7= 0.207593D+07
M1 OPAMP 79 29 29 GND / RIN=*RR , GAIN=*GA , GBW=*GG1
M2 OPAMP 80 30 30 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M3 OPAMP 81 31 31 GND / RIN=*RR , GAIN=*GA , GBW=*GG3
M4 OPAMP 82 32 32 GND / RIN=*RR , GAIN=*GA , GBW=*GG4
C71 29 34 0.218079D-08
C72 30 35 0.220791D-08
C73 31 36 0.217865D-08
C74 32 33 0.217665D-08
R71 29 33  42778.
R72 30 34  42575.
R73 31 35  42342.
R74 32 36  42825.
RG1 21 GND  35542.
RG2 22 GND  35592.
RG3 23 GND  35512.
RG4 24 GND  35470.
E1 N1 GND 0
OX1 N1 GND
VV1 4 GND V(OX1) C10(0.)
VV2 3 GND V(OX1) C10(1.5707963)
VV3 2 GND V(OX1) C10(3.1415927)
VV4 1 GND V(OX1) C10(4.712389)
O1 33 GND
O2 34 GND
O3 35 GND
O4 36 GND
RA 33 57      0.
```

```
RB 34 57  50000.
RC 35 59  50000.
RD 36 59      0.
MXX1 OPAMP 57 B200 B200 GND / RIN=*RR , GAIN=*GA , GBW=*GG5
MXX2 OPAMP 59 B100 B100 GND / RIN=*RR , GAIN=*GA , GBW=*GG6
RYY1 B200 200 100154.
RYY2 B100 100 100035.
RX3 100 GND  99824.
RX4 200 300 100130.
MXX3 OPAMP 200 100 300 GND / RIN=*RR , GAIN=*GA , GBW=*GG7
$PORT *OUT = NV(300)/E1 DBL AREF(-1004.,-1004.)  S
$FREQ SP  175. 300. 600. 900. 1200. 1500. 1800. 2100.
$FREQ SP 2400. 2700. 3000. 3300.  3700.
$FREQ SP -1004.
$ANAL
```

```
$*-------     SD7J4  DATA  FILE  (  TRANSMIT  SIDE  )      -------

$H   POLYPHASE NETWORK     ( CASE XD6247 )
$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34,C41,C42,C43,C44
$P C51,C52,C53,C54,C61,C62,C63,C64,C71,C72,C73,C74
$TOL (0,1.) TEMP(0,30.)  *C11,*C12,*C13,*C14,*C21,*C22,*C23,*C24
$TOL (0,1.) TEMP(0,30.)  *C31,*C32,*C33,*C34,*C41,*C42,*C43,*C44
$TOL (0,1.) TEMP(0,30.)  *C51,*C52,*C53,*C54,*C61,*C62,*C63,*C64
$TOL (0,1.) TEMP(0,30.)  *C71,*C72,*C73,*C74
R11  1  5 XTOL(15.E3,.250D0)
R12  2  6 XTOL(15.E3,.250D0)
R13  3  7 XTOL(15.E3,.250D0)
R14  4  8 XTOL(15.E3,.250D0)
$P R11,R12,R13,R14
$TOL (0,.25) *R11,*R12,*R13,*R14
C11  5 10 XTOL(2.2E-9,.250D0)
C12  6 11 XTOL(2.2E-9,.250D0)
C13  7 12 XTOL(2.2E-9,.250D0)
C14  8  9 XTOL(2.2E-9,.250D0)
R21  5  9 XTOL(114.2238E3 ,.250D0)
R22  6 10 XTOL(114.2238E3 ,.250D0)
R23  7 11 XTOL(114.2238E3 ,.250D0)
R24  8 12 XTOL(114.2238E3 ,.250D0)
C21  9 14 XTOL(2.2E-9,.2500)
C22 10 15 XTOL(2.2E-9,.2500)
C23 11 16 XTOL(2.2E-9,.2500)
C24 12 13 XTOL(2.2E-9,.2500)
R31  9 13 XTOL(78.5707E3 ,.250D0)
R32 10 14 XTOL(78.5707E3 ,.250D0)
R33 11 15 XTOL(78.5707E3 ,.250D0)
R34 12 16 XTOL(78.5707E3 ,.250D0)
C31 13 18 XTOL(2.2E-9,1.00)
C32 14 19 XTOL(2.2E-9,1.00)
C33 15 20 XTOL(2.2E-9,1.00)
C34 16 17 XTOL(2.2E-9,1.00)
R41 13 17 XTOL(24.7573E3 ,.250D0)
R42 14 18 XTOL(24.7573E3 ,.250D0)
R43 15 19 XTOL(24.7573E3 ,.250D0)
R44 16 20 XTOL(24.7573E3 ,.250D0)
C41 17 22 XTOL(2.2E-9,1.00)
C42 18 23 XTOL(2.2E-9,1.00)
C43 19 24 XTOL(2.2E-9,1.00)
C44 20 21 XTOL(2.2E-9,1.00)
R51 17 21 XTOL(36.8923E3 ,.250D0)
R52 18 22 XTOL(36.8923E3 ,.250D0)
R53 19 23 XTOL(36.8923E3 ,.250D0)
R54 20 24 XTOL(36.8923E3 ,.250D0)
C51 21 26 XTOL(2.2E-9,1.00)
C52 22 27 XTOL(2.2E-9,1.00)
C53 23 28 XTOL(2.2E-9,1.00)
C54 24 25 XTOL(2.2E-9,1.00)
R61 21 25 XTOL(20.1095E3 ,.250D0)
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R62 22 26 XTOL(20.1095E3 ,.250D0)
R63 23 27 XTOL(20.1095E3 ,.250D0)
R64 24 28 XTOL(20.1095E3 ,.250D0)
C61 25 80 XTOL(2.2E-9,.500)
C62 26 81 XTOL(2.2E-9,.500)
C63 27 82 XTOL(2.2E-9,.500)
C64 28 79 XTOL(2.2E-9,.500)
R71 25 79 XTOL(226.3894E3 ,.250D0)
R72 26 80 XTOL(226.3894E3 ,.250D0)
R73 27 81 XTOL(226.3894E3 ,.250D0)
R74 28 82 XTOL(226.3894E3 ,.250D0)
M1 OPAMP 79 29 29 GND / RIN=*RR , GAIN=*GA , GBW=*GG1
M2 OPAMP 80 30 30 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M3 OPAMP 81 31 31 GND / RIN=*RR , GAIN=*GA , GBW=*GG3
M4 OPAMP 82 32 32 GND / RIN=*RR , GAIN=*GA , GBW=*GG4
$P RR,GA,GG1,GG2,GG3,GG4
*RR=1.E10
*GA=2.E4
*GG1=1.0E6
*GG2=1.0E6
*GG3=1.0E6
*GG4=1.0E6
$TOL (0.,20.) *GG1,*GG2,*GG3,*GG4
C71 29 34 XTOL(2.2E-9,.250)
C72 30 35 XTOL(2.2E-9,.250)
C73 31 36 XTOL(2.2E-9,.250)
C74 32 33 XTOL(2.2E-9,.250)
R81 29 33 XTOL(42.4017E3 ,.250D0)
R82 30 34 XTOL(42.4017E3 ,.250D0)
R83 31 35 XTOL(42.4017E3 ,.250D0)
R84 32 36 XTOL(42.4017E3 ,.250D0)
$*R91 21 GND F60(*C74,51.5249E3,.2)
R91 21 GND XTOL(35.5035E3,.25)
R92 22 GND XTOL(35.5035E3,.25)
R93 23 GND XTOL(35.5035E3,.25)
R94 24 GND XTOL(35.5035E3,.25)
$P R91,R92,R93,R94
$TOL (0,.25) *R91,*R92,*R93,*R94
E1 N1 GND 0
VL 1 GND V(E1) 1.
V1 3 GND V(VL) -1.
$*SS1 2 GND
$*SS2 4 GND
V2 2 GND V(VL) 1.
V4 4 GND V(VL) -1.
VV1 A33 GND V(01) C10(0.)
VV2 A34 GND V(02) C10(1.5707963)
VV3 A35 GND V(03) C10(3.1415927)
VV4 A36 GND V(04) C10(4.712389)
VV5 100 GND V(05) V(06)  1. 1.
VV6 200 GND V(07) V(08)  1. 1.
VV7 300 GND V(09) V(010) 1. 1.
```

```
01 33 GND
02 34 GND
03 35 GND
04 36 GND
05 A33 GND
06 A34 GND
07 A35 GND
08 A36 GND
09 100 GND
010 200 GND
$*PORT    *ONE=NV(33)/E1 DBL AREF (-1004.,,-1004.)
$PORT *OUT=NV(300)/E1 DBL AREF(-1004.,-1004.)    S
$*FREQ SP -1004. 175. 300. 600. 900. 1200. 1500. 1800. 2100. 2400.
$*FREQ SP 2700. 3000. 3300. 3700.
$FREQ SP -1004. -250. -300. -400. -2000. -3000. -3200. -3300. -3400.
$SPFN *OUT (-3000.,-300.) (-.15,.15)   10
$SPFN *OUT (-3400.,-3000.)    (-.2,.2)    10
$SPFN *OUT (-300.,-250.) (-.2,.2)    10
$SPFN *OUT (300.,600.)        (43.,PINF)
$SPFN *OUT (600.,2000.)       (70.,PINF)
$SPFN *OUT (2000.,3700.)      (77.,PINF)
$SPFN *OUT (175.,175.)        (24.,PINF)
$*SPFN *OUT (0.,0.) (5.,PINF)
$SPEC(9)=-1
$ANAL
$ANAL
$ANAL
$ANAL
$ANAL
$ANAL
$*      $ANAL CAN BE REPEATED
```

```
$*-------     SD7R9  DATA  FILE  (  RECEIVE  SIDE  )     -------

$H  POLYPHASE NETWORK     ( CASE XD6247 )
RS1   1   5 XTOL(15.E3,.25)
RS2   2   6 XTOL(15.E3,.25)
RS3   3   7 XTOL(15.E3,.25)
RS4   4   8 XTOL(15.E3,.25)
C11   5  10 XTOL(2.2D-9,.25D00)
C12   6  11 XTOL(2.2D-9,.25D00)
C13   7  12 XTOL(2.2D-9,.25D00)
C14   8   9 XTOL(2.2D-9,.25D00)
R11   5   9 XTOL(114.2238D3,.250D0)
R12   6  10 XTOL(114.2238D3,.250D0)
R13   7  11 XTOL(114.2238D3,.250D0)
R14   8  12 XTOL(114.2238D3,.250D0)
SS1   9  13
SS2  10  14
SS3  11  15
SS4  12  16
C21  13  18 XTOL(2.2D-9,.25D00)
C22  14  19 XTOL(2.2D-9,.25D00)
C23  15  20 XTOL(2.2D-9,.25D00)
C24  16  17 XTOL(2.2D-9,.25D00)
R21  13  17 XTOL(78.5707D3,.250D0)
R22  14  18 XTOL(78.5707D3,.250D0)
R23  15  19 XTOL(78.5707D3,.250D0)
R24  16  20 XTOL(78.5707D3,.250D0)
SS5  17  21
SS6  18  22
SS7  19  23
SS8  20  24
C31  21  26 XTOL(2.2D-9,1.D00)
C32  22  27 XTOL(2.2D-9,1.D00)
C33  23  28 XTOL(2.2D-9,1.D00)
C34  24  25 XTOL(2.2D-9,1.D00)
R31  21  25 XTOL(24.7573D3,.250D0)
R32  22  26 XTOL(24.7573D3,.250D0)
R33  23  27 XTOL(24.7573D3,.250D0)
R34  24  28 XTOL(24.7573D3,.250D0)
SS9   25  29
SS10 26  30
SS11 27  31
SS12 28  32
C41  29  34 XTOL(2.2D-9,1.D00)
C42  30  35 XTOL(2.2D-9,1.D00)
C43  31  36 XTOL(2.2D-9,1.D00)
C44  32  33 XTOL(2.2D-9,1.D00)
R41  29  33 XTOL(36.8923D3,.250D0)
R42  30  34 XTOL(36.8923D3,.250D0)
R43  31  35 XTOL(36.8923D3,.250D0)
R44  32  36 XTOL(36.8923D3,.250D0)
SS13 33  37
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SS14 34 38
SS15 35 39
SS16 36 40
C51 37 42 XTOL(2.2D-9,1.D00)
C52 38 43 XTOL(2.2D-9,1.D00)
C53 39 44 XTOL(2.2D-9,1.D00)
C54 40 41 XTOL(2.2D-9,1.D00)
R51 37 41 XTOL(20.1095D3,.250D0)
R52 38 42 XTOL(20.1095D3,.250D0)
R53 39 43 XTOL(20.1095D3,.250D0)
R54 40 44 XTOL(20.1095D3,.250D0)
SS17 41 45
SS18 42 46
SS19 43 47
SS20 44 48
C61 45 50 XTOL(2.2D-9,.25D00)
C62 46 51 XTOL(2.2D-9,.25D00)
C63 47 52 XTOL(2.2D-9,.25D00)
C64 48 49 XTOL(2.2D-9,.25D00)
R61 45 49 XTOL(226.3894D3,.250D0)
R62 46 50 XTOL(226.3894D3,.250D0)
R63 47 51 XTOL(226.3894D3,.250D0)
R64 48 52 XTOL(226.3894D3,.250D0)
C71 53 58 XTOL(2.2D-9,.25D00)
C72 54 59 XTOL(2.2D-9,.25D00)
C73 55 60 XTOL(2.2D-9,.25D00)
C74 56 57 XTOL(2.2D-9,.25D00)
R71 53 57 XTOL(42.4017D3,.250D0)
R72 54 58 XTOL(42.4017D3,.250D0)
R73 55 59 XTOL(42.4017D3,.250D0)
R74 56 60 XTOL(42.4017D3,.250D0)
$P GG1,GG2,GA,RR
*RR=1.E12
*GA=2.E4
*GG1=2.E6
*GG2=1.D6
M1 OPAMP 49 53 53 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M2 OPAMP 50 54 54 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M3 OPAMP 51 55 55 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M4 OPAMP 52 56 56 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
RG1 33 GND XTOL(35.5035D3,.250D0)
RG2 34 GND XTOL(35.5035D3,.250D0)
RG3 35 GND XTOL(35.5035D3,.250D0)
RG4 36 GND XTOL(35.5035D3,.250D0)
E1 N1 GND 0
OX1 N1 GND
VV1 4 GND V(OX1) C12(0.,*DD)
VV2 3 GND V(OX1) C12(1.5707963,*DD)
VV3 2 GND V(OX1) C12(3.1415927,*DD)
VV4 1 GND V(OX1) C12(4.712389,*DD)
*DD=0.
O1 57 GND
```

```
O2 58 GND
O3 59 GND
O4 60 GND
RA 57 N57 XTOL(200.,1.)
RB 58 N57 XTOL(50.2E3,1.)
RC 59 N59 XTOL(50.2E3,1.)
RD 60 N59 XTOL(200.,1.)
RYY1 B200 200 XTOL(100.E3,.25)
RYY2 B100 100 XTOL(100.E3,.25)
MXX1 OPAMP N57 B200 B200 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
MXX2 OPAMP N59 B100 B100 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
RX3 100 GND XTOL(100.E3,.25)
RX4 200 300 XTOL(100.E3,.25)
MXX3 OPAMP 100 200 300 GND / RIN=*RR , GAIN=*GA ,GBW=*GG1
$*PORT    *ONE=NV(57)/E1 DBL AREF (-1004.,-1004.)
$PORT *OUT=NV(300)/E1 DBL AREF(-1004.,-1004.)     S
$FREQ SP -300. -400. -3000. -3400.
$FREQ SP -1004. 175. 300. 600. 900. 1200. 1500. 1800. 2100. 2400.
$FREQ SP  2700. 3000. 3300. 3700.
$SPFN *OUT (-3000.,-300.)   (-.15,.15)   10
$SPFN *OUT (-3400.,-3000.) (-.2,.2)   10
$SPFN *OUT (-300.,-250.)     (-.2,.2)   10
$*SPFN *OUT (0.,0.)            (5.,PINF)
$SPFN *OUT (300.,600.)         (43.,PINF)
$SPFN *OUT (600.,2000.)        (70.,PINF)
$SPFN *OUT (2000.,3700.)       (77.,PINF)
$SPFN *OUT (175.,175.)         (24.,PINF)
$SPEC(9)=-1
$ANAL
$ANAL
$ANAL
$ANAL
$ANAL
$ANAL
$*   $ANAL CAN BE REPEATED
$TERM
```

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$*-------     SD7K9  DATA  FILE  (  TRANSMIT  SIDE  )      -------

$H  POLYPHASE NETWORK     ( CASE XD6247 )
$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34
$P C41,C42,C43,C44,C51,C52,C53,C54,C61,C62,C63,C64,C71,C72,C73,C74
$P R11,R12,R13,R14,R21,R22,R23,R24,R31,R32,R33,R34
$P R41,R42,R43,R44,R51,R52,R53,R54,R61,R62,R63,R64,R71,R72,R73,R74
$P RG1,RG2,RG3,RG4
$TOL (0,.2) TEMP (0,30.) *C11,*C12,*C13,*C14,*C21,*C22,*C23,*C24
$TOL (0,.2) TEMP (0,30.) *C31,*C32,*C33,*C34,*C41,*C42,*C43,*C44
$TOL (0,.2) TEMP (0,30.) *C51,*C52,*C53,*C54,*C61,*C62,*C63,*C64
$TOL (0,.2) TEMP (0,30.) *C71,*C72,*C73,*C74
$TOL (0,.250) TEMP (0,50.) *R11,*R12,*R13,*R14,*R21,*R22,*R23,*R24
$TOL (0,.250) TEMP (0,50.) *R31,*R32,*R33,*R34,*R41,*R42,*R43,*R44
$TOL (0,.250) TEMP (0,50.) *R51,*R52,*R53,*R54,*R61,*R62,*R63,*R64
$TOL (0,.250) TEMP (0,50.) *RG1,*RG2,*RG3,*RG4
$TOL (0,.25) TEMP (0,50.) *R71,*R72,*R73,*R74
$TOL (0,20.) *GG2
$P RZ1,RZ2,RZ3,RZ4
RI1  1  5 15.E3
RI2 2  6 15.E3
RI3  3  7 15.E3
RI4 4  8 15.E3
$P RI1,RI2,RI3,RI4
$TOL (0,.5) *RI1,*RI2,*RI3,*RI4
C11  5 10 2.2D-9
C12  6 11 2.2D-9
C13  7 12 2.2D-9
C14  8  9 2.2D-9
R11  5  9 114.2238D3
R12  6 10 114.2238D3
R13  7 11 114.2238D3
R14  8 12 114.2238D3
SS1  9 13
SS2 10 14
SS3 11 15
SS4 12 16
C21 13 18 2.2D-9
C22 14 19 2.2D-9
C23 15 20 2.2D-9
C24 16 17 2.2D-9
R21 13 17 78.5707D3
R22 14 18 78.5707D3
R23 15 19 78.5707D3
R24 16 20 78.5707D3
SS5 17 21
SS6 18 22
SS7 19 23
SS8 20 24
C31 21 26 2.2D-9
C32 22 27 2.2D-9
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C33 23 28 2.2D-9
C34 24 25 2.2D-9
R31 21 25 24.7573D3
R32 22 26 24.7573D3
R33 23 27 24.7573D3
R34 24 28 24.7573D3
SS9  25 29
SS10 26 30
SS11 27 31
SS12 28 32
C41 29 34 2.2D-9
C42 30 35 2.2D-9
C43 31 36 2.2D-9
C44 32 33 2.2D-9
R41 29 33 36.8923D3
R42 30 34 36.8923D3
R43 31 35 36.8923D3
R44 32 36 36.8923D3
SS13 33 37
SS14 34 38
SS15 35 39
SS16 36 40
C51 37 42 2.2D-9
C52 38 43 2.2D-9
C53 39 44 2.2D-9
C54 40 41 2.2D-9
R51 37 41 20.1095D3
R52 38 42 20.1095D3
R53 39 43 20.1095D3
R54 40 44 20.1095D3
SS17 41 45
SS18 42 46
SS19 43 47
SS20 44 48
C61 45 50 2.2D-9
C62 46 51 2.2D-9
C63 47 52 2.2D-9
C64 48 49 2.2D-9
R61 45 49 226.3894D3
R62 46 50 226.3894D3
R63 47 51 226.3894D3
R64 48 52 226.3894D3
C71 53 58 2.2D-9
C72 54 59 2.2D-9
C73 55 60 2.2D-9
C74 56 57 2.2D-9
R71 53 57 42.4017D3
R72 54 58 42.4017D3
R73 55 59 42.4017D3
R74 56 60 42.4017D3
$P GG2,GA,RR
*RR=1.E12
```

```
*GA=2.E4
*GG2=1.D6
M1 OPAMP 49 53 53 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M2 OPAMP 50 54 54 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M3 OPAMP 51 55 55 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
M4 OPAMP 52 56 56 GND / RIN=*RR , GAIN=*GA , GBW=*GG2
RG1 33 GND 35.5035D3
RG2 34 GND 35.5035D3
RG3 35 GND 35.5035D3
RG4 36 GND 35.5035D3
E1 N1 GND 0
VL 1 GND V(E1) 1.
V1 3 GND V(VL) -1.
SSS1 2 GND
SSS2 4 GND
VV1 A57 GND V(01) C12(0.,*DD)
VV2 A58 GND V(02) C12(1.5707963,*DD)
VV3 A59 GND V(03) C12(3.1415927,*DD)
VV4 A60 GND V(04) C12(4.712389,*DD)
*DD=0.
VV5 100 GND V(05) V(06)  1. 1.
VV6 200 GND V(07) V(08)  1. 1.
VV7 300 GND V(09) V(010) 1. 1.
01 57 GND
02 58 GND
03 59 GND
04 60 GND
05 A57 GND
06 A58 GND
07 A59 GND
08 A60 GND
09 100 GND
010 200 GND
$PORT     *ONE=NV(57)/E1 DBL AREF (-1004.,-1004.)
$*PORT     *TWO=NV(58)/E1 DBL AREF (-1004.,-1004.)
$*PORT     *THREE=NV(59)/E1 DBL AREF (-1004.,-1004.)
$*PORT     *FOUR=NV(60)/E1 DBL AREF (-1004.,-1004.)
$*PORT *VV1=NV(100)/E1 DBL AREF(-3400.,-250.)
$PORT *OUT=NV(300)/E1 DBL AREF(-1004.,-1004.)     S
$*DELAY *DELA=NV(300)/E1 DBL DREF(-2200.,-2200.) S
$FREQ LIN 4 5.E3 8.E3
$FREQ LIN 5 8.E3 12.E3
$FREQ LIN 40 100. 4000.
$FREQ SP  -1004. -2200. 1. 100. 175. 300. 500. 700. 3300. 3700.
$FREQ SP -30. -80. -100. -175. -160. -170. -250. -300. -3650. -3800.
$FREQ SP 19.D3 20.D3 30.D3 40.D3 50.D3 60.D3 63.D3
$FREQ LIN 21 -4000. 0.
$FREQ SP -1.E6 -5.E5 -1000. -1.E5 1.E5 5.E5 1.E6
$SPFN *OUT (-3000.,-300.)   (-.15,.15)   10
$SPFN *OUT (-3400.,-3000.) (-.2,.2)    10
$SPFN *OUT (-300.,-250.)     (-.2,.2)   10
$*SPFN *OUT (0.,0.)            (5.,PINF)
```

```
$SPFN *OUT (300.,600.)        (43.,PINF)
$SPFN *OUT (600.,2000.)       (70.,PINF)
$SPFN *OUT (2000.,3700.)      (83.,PINF)
$SPFN *OUT (175.,175.)        (24.,PINF)
$SPEC(9)=-1
$ANAL
$STATS 100
$TEST *OUT (-3400.,-3000.) (-.3,.3)
$TEST *OUT (-3000.,-300.) (-.2,.3)
$TEST *OUT (-300.,-300.)  (-.2,.3)
$TEST *OUT (-250.,-250.) (-.2,.7)
$TEST *OUT (175.,175.)    (22.,PINF)
$TEST *OUT (300.,600.)    (42.,PINF)
$TEST *OUT (600.,3700.)   (60.,PINF)
$FIN 20
$TERM
$STATS 100,-25
$TEST *OUT (-3400.,-3000.) (-.3,.3)
$TEST *OUT (-3000.,-300.) (-.2,.3)
$TEST *OUT (-300.,-250.)  (-.2,.7)
$TEST *OUT (175.,175.)    (20.,PINF)
$TEST *OUT (300.,600.)    (40.,PINF)
$TEST *OUT (600.,3700.)   (60.,PINF)
$FIN 20
$STATS 100,25
$TEST *OUT (-3400.,-3000.) (-.3,.3)
$TEST *OUT (-3000.,-300.) (-.2,.3)
$TEST *OUT (-300.,-250.)  (-.2,.7)
$TEST *OUT (175.,175.)    (20.,PINF)
$TEST *OUT (300.,600.)    (40.,PINF)
$TEST *OUT (600.,3700.)   (60.,PINF)
$FIN 20
$TERM
```

```
$*-------     SD7J  DATA  FILE  (  TRANSMIT  SIDE  )     -------

$H   POLYPHASE NETWORK    ( CASE XD6247 )   CLOCKWISE TRIMMING
$P C11,C12,C13,C14,C21,C22,C23,C24,C31,C32,C33,C34,C41,C42,C43,C44
$P C51,C52,C53,C54,C61,C62,C63,C64,C71,C72,C73,C74
$TOL (0,1.) TEMP(0,30.)  *C11,*C12,*C13,*C14,*C21,*C22,*C23,*C24
$TOL (0,1.) TEMP(0,30.)  *C31,*C32,*C33,*C34,*C41,*C42,*C43,*C44
$TOL (0,1.) TEMP(0,30.)  *C51,*C52,*C53,*C54,*C61,*C62,*C63,*C64
$TOL (0,1.) TEMP(0,30.)  *C71,*C72,*C73,*C74
R11  1  5 15.E3
R12  2  6 15.E3
R13  3  7 15.E3
R14  4  8 15.E3
$P R11,R12,R13,R14
$TOL (0,.25) *R11,*R12,*R13,*R14
C11  5 10 2.2E-9
C12  6 11 2.2E-9
C13  7 12 2.2E-9
C14  8  9 2.2E-9
R21  5  9 F51(*W1,*C14,.350D0)
R22  6 10 F51(*W1,*C11,.350D0)
R23  7 11 F51(*W1,*C12,.350D0)
R24  8 12 F51(*W1,*C13,.350D0)
C21  9 14 2.2E-9
C22 10 15 2.2E-9
C23 11 16 2.2E-9
C24 12 13 2.2E-9
R31  9 13 F51(*W2,*C24,.350D0)
R32 10 14 F51(*W2,*C21,.350D0)
R33 11 15 F51(*W2,*C22,.350D0)
R34 12 16 F51(*W2,*C23,.350D0)
C31 13 18 2.2E-9
C32 14 19 2.2E-9
C33 15 20 2.2E-9
C34 16 17 2.2E-9
R41 13 17 F51(*W3,*C34,.350D0)
R42 14 18 F51(*W3,*C31,.350D0)
R43 15 19 F51(*W3,*C32,.350D0)
R44 16 20 F51(*W3,*C33,.350D0)
C41 17 22 2.2E-9
C42 18 23 2.2E-9
C43 19 24 2.2E-9
C44 20 21 2.2E-9
R51 17 21 F51(*W4,*C44,.350D0)
R52 18 22 F51(*W4,*C41,.350D0)
R53 19 23 F51(*W4,*C42,.350D0)
R54 20 24 F51(*W4,*C43,.350D0)
C51 21 26 2.2E-9
C52 22 27 2.2E-9
C53 23 28 2.2E-9
C54 24 25 2.2E-9
R61 21 25 F51(*W5,*C54,.350D0)
```

```
R62 22 26 F51(*W5,*C51,.350D0)
R63 23 27 F51(*W5,*C52,.350D0)
R64 24 28 F51(*W5,*C53,.350D0)
C61 25 80 2.2E-9
C62 26 81 2.2E-9
C63 27 82 2.2E-9
C64 28 79 2.2E-9
R71 25 79 F51(*W6,*C64,.350D0)
R72 26 80 F51(*W6,*C61,.350D0)
R73 27 81 F51(*W6,*C62,.350D0)
R74 28 82 F51(*W6,*C63,.350D0)
OS1 79 GND
OS2 80 GND
OS3 81 GND
OS4 82 GND
VS1 29 GND V(OS1) 1.
VS2 30 GND V(OS2) 1.
VS3 31 GND V(OS3) 1.
VS4 32 GND V(OS4) 1.
C71 29 34 2.2E-9
C72 30 35 2.2E-9
C73 31 36 2.2E-9
C74 32 33 2.2E-9
R81 29 33 F51(*W7,*C74,.350D0)
R82 30 34 F51(*W7,*C71,.350D0)
R83 31 35 F51(*W7,*C72,.350D0)
R84 32 36 F51(*W7,*C73,.350D0)
$*R91 21 GND F60(*C74,51.5249E3,.2)
R91 21 GND 35.50351E3
R92 22 GND 35.50351E3
R93 23 GND 35.50351E3
R94 24 GND 35.50351E3
$P R91,R92,R93,R94
$TOL (0,.25) *R91,*R92,*R93,*R94
*W1=3.9794286E3
*W2=5.7851776E3
*W3=18.36005E3
*W4=12.320886E3
*W5=22.603575E3
*W6=2.0078036E3
*W7=10.719994E3
E1 N1 GND 0
VL 1 GND V(E1) 1.
V1 3 GND V(VL) -1.
$*SS1 2 GND
$*SS2 4 GND
V2 2 GND V(VL) 1.
V4 4 GND V(VL) -1.
VV1 A33 GND V(01) C10(0.)
VV2 A34 GND V(02) C10(1.5707963)
VV3 A35 GND V(03) C10(3.1415927)
VV4 A36 GND V(04) C10(4.712389)
```

```
VV5 100 GND V(05) V(06)  1. 1.
VV6 200 GND V(07) V(08)  1. 1.
VV7 300 GND V(09) V(010) 1. 1.
01 33 GND
02 34 GND
03 35 GND
04 36 GND
05 A33 GND
06 A34 GND
07 A35 GND
08 A36 GND
09 100 GND
010 200 GND
$PORT    *ONE=NV(33)/E1 DBL AREF (-1004.,-1004.)
$PORT    *TWO=NV(34)/E1 DBL AREF (-1004.,-1004.)
$*PORT   *THREE=NV(35)/E1 DBL AREF (-1004.,-1004.)
$*PORT   *FOUR=NV(36)/E1 DBL AREF (-1004.,-1004.)
$*PORT *VV1=NV(100)/E1 DBL AREF(-1004.,-1004.)
$*PORT *VV2=NV(200)/E1 DBL AREF(-1004.,-1004.)
$PORT *OUT=NV(300)/E1 DBL AREF(-1004.,-1004.)    S
$FREQ LIN 4 5.E3 8.E3
$FREQ LIN 5 8.E3 12.E3
$FREQ LIN 41  0. 4000.
$FREQ SP 1. 30. 80. 100. 175.
$FREQ SP -175 -160. -170. -250. -300. -3650. -3000. -3400. -3800. -385
$FREQ LIN 21 -4000. 0.
$SPFN *OUT (-3000.,-300.) (-.15,.15)   10
$SPFN *OUT (-3400.,-3000.)    (-.2,.2)    10
$SPFN *OUT (-300.,-250.) (-.2,.2)    10
$SPFN *OUT (300.,600.)        (43.,PINF)
$SPFN *OUT (600.,2000.)       (70.,PINF)
$SPFN *OUT (2000.,3700.)      (77.,PINF)
$SPFN *OUT (175.,175.)        (24.,PINF)
$*SPFN *OUT (0.,0.) (5.,PINF)
$SPEC(9)=-1
$ANAL
$STATS 100
$*TEST *OUT (-3400.,-3000.) (-.2,.7)
$*TEST *OUT (-3000.,-300.) (-.2,.3)
$*TEST *OUT (-300.,-250.)  (-.2,1.)
$TEST *OUT (175.,175.)    (20.,PINF)
$TEST *OUT (300.,600.)    (40.,PINF)
$TEST *OUT (600.,2000.)   (60.,PINF)
$TEST *OUT (2000.,3700.)  (60.,PINF)
$FIN 20
$TERM
$STATS 100,-25
$TEST *OUT (-3400.,-3000.) (-.2,.7)
$TEST *OUT (-3000.,-300.) (-.2,.2)
$TEST *OUT (-300.,-250.)  (-.2,.7)
$TEST *OUT (175.,175.)    (20.,PINF)
$TEST *OUT (300.,600.)    (40.,PINF)
```

```
$TEST *OUT (600.,2000.)    (60.,PINF)
$TEST *OUT (2000.,3700.)   (60.,PINF)
$FIN 20
$STATS 100,25
$TEST *OUT (-3400.,-3000.) (-.2,.7)
$TEST *OUT (-3000.,-300.)  (-.2,.2)
$TEST *OUT (-300.,-250.)   (-.2,1.)
$TEST *OUT (175.,175.)     (20.,PINF)
$TEST *OUT (300.,600.)     (40.,PINF)
$TEST *OUT (600.,2000.)    (60.,PINF)
$TEST *OUT (2000.,3700.)   (60.,PINF)
$FIN 20
$END
$TERM
```

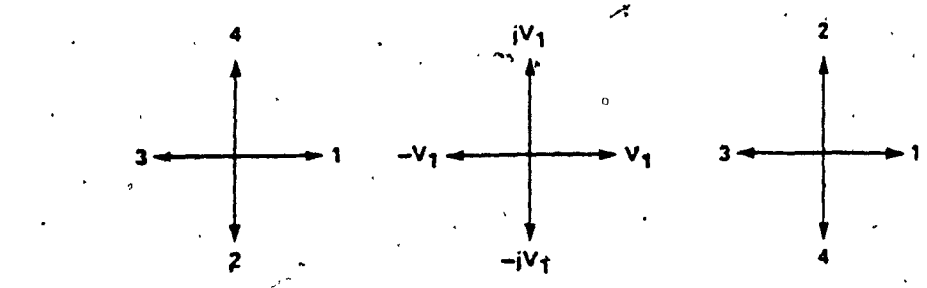
Appendix 3

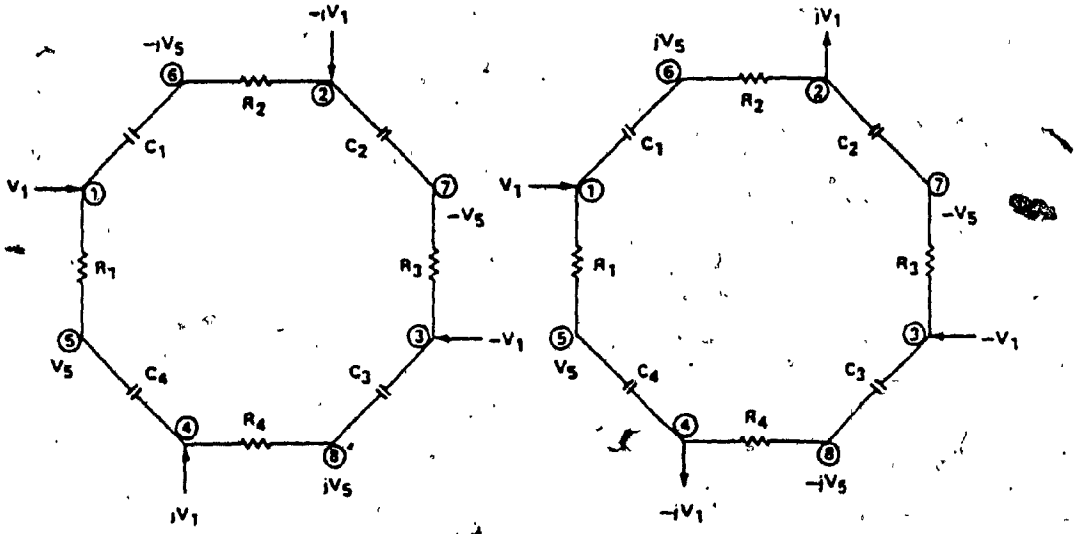
THE ABCD MATRIX FOR THE SINGLE STAGE POLYPHASE NETWORK

Appendix 3

The ABCD Matrix for the Single Stage Four Phase S.D.

(1) The A Parameter





Positive Sequence

$$(V_5 - V_1)\, G_1 = (jV_1 - V_5)\, jwC_4$$

$$V_5 (G_1 + jwC_4) = V_1 (G_1 - wC_4)$$

$$\left(\frac{V_1}{V_5}\right)_+ = \frac{G_1 + jwC_4}{G_1 - wC_4}$$

$$\therefore A_{15+} = \frac{1 + jwC_4R_1}{1 - wC_4R_1}$$

For equal R's, C's

$$A_{15+} = \frac{1 + jwCR}{1 - wCR}$$

Negative Sequence

$$(V_5 - V_1)\, G_1 = (jV_1 - V_5)\, jwC_4$$

$$V_5 (G_1 + jwC_4) = V_1 (G_1 + wC_4)$$

$$\left(\frac{V_1}{V_5}\right)_- = \frac{G_1 + jwC_4}{G_1 + wC_4}$$

$$\therefore A_{15-} = \frac{1 + jwC_4R_1}{1 + wC_4R_1}$$

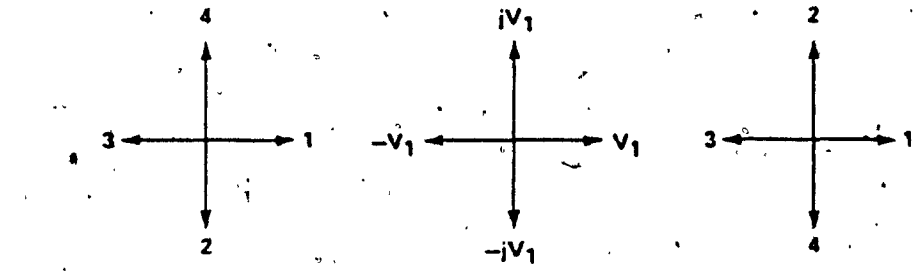
For equal R's, C's

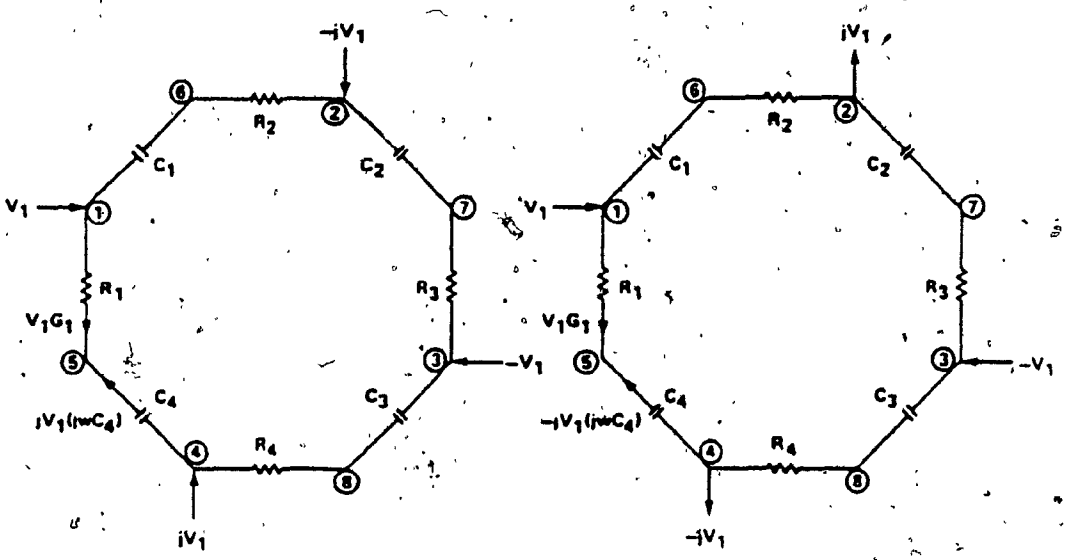
$$A_{15-} = \frac{1 + jwCR}{1 + wCR}$$

Appendix 3

The ABCD Matrix for the Single Stage Four Phase S.D.

(2) The B Parameter





Positive Sequence

$$i_5 = V_1 (G_1 - wC_4)$$

$$\left(\frac{V_1}{i_5}\right)_+ = \frac{1}{G_1 - wC_4}$$

$$\therefore B15+ = \frac{R_1}{1 - WC_4R_1}$$

For equal R's, C's

$$B15+ = \frac{R}{1 - wCR}$$

Negative Sequence

$$i_5 = V_1 (G_1 + wC_4)$$

$$\left(\frac{V_1}{i_5}\right)_- = \frac{1}{G_1 + wC_4}$$

$$B15- = \frac{R_1}{1 + WC_4R_1}$$

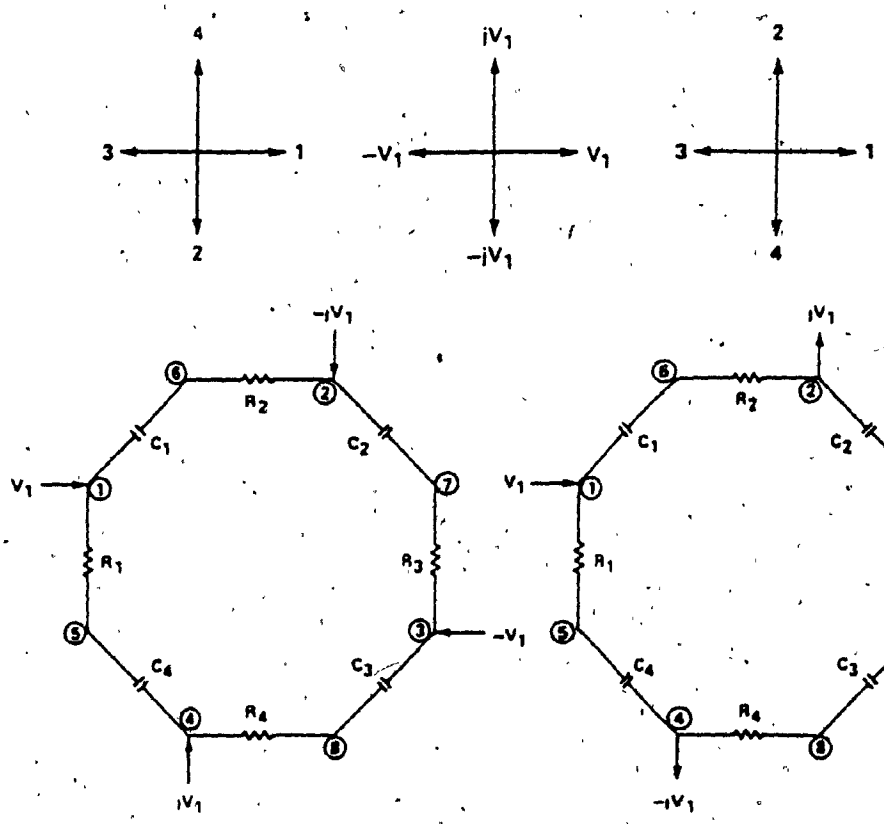
For equal R's, C's

$$B15+ = \frac{R}{1 + wCR}$$

Appendix 3

The ABCD Matrix for the Single Stage Four Phase S.D.

(3) The C Parameter



Positive Sequence

$$i_1 = (V_1 - V_5)\,G_1 + (V_1 + jV_5)\,jwC_1$$

$$\left.\frac{i_1}{V_5}\right)_+ = \left(\frac{V_1}{V_5} - 1\right) G_1 + \left(\frac{V_1}{V_5} + j\right) SC_1$$

Substitute

$$\frac{V_1}{V_5} = \frac{1 + jwC_4R_1}{1 - wC_4R_1}$$

$$\therefore C15+ = \frac{wC_4(j+1) + wC_1(j-1)}{1 - wC_4R_1}$$

For equal R's, C's

$$C15+ = \frac{2jwC}{1 - wCR}$$

Negative Sequence

$$i_1 = (V_1 - V_5)\,G_1 + (V_1 + jV_5)\,jwC_1$$

$$\left.\frac{i_1}{V_5}\right)_- = \left(\frac{V_1}{V_5} - 1\right) G_1 + \left(\frac{V_1}{V_5} - j\right) jwC_1$$

Substitute

$$\frac{V_1}{V_5} = \frac{1 + jwC_4R_1}{1 + wC_4R_1}$$

$$C15- = \frac{wC_4(j-1) + wC_1(j+1)}{1 + wC_4R_1}$$

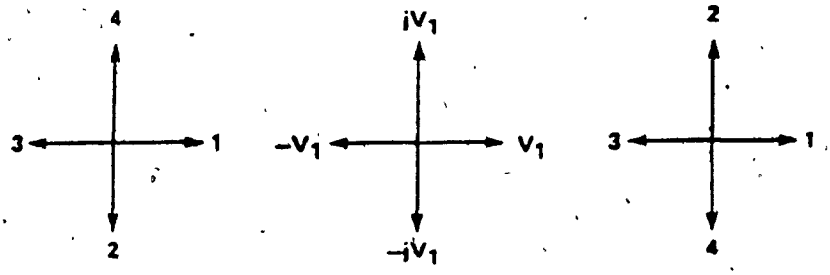
For equal R's, C's

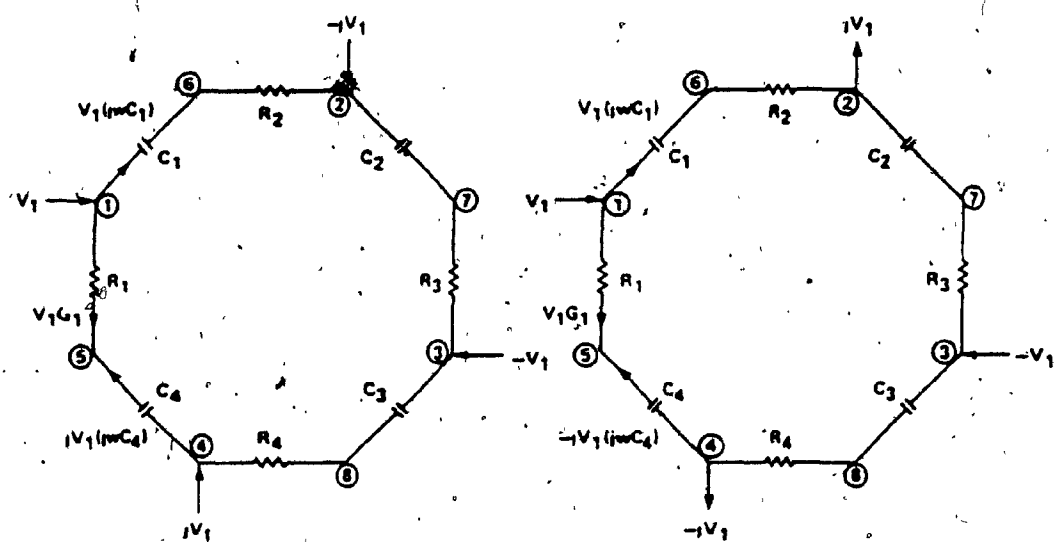
$$C15- = \frac{2jwC}{1 + wCR}$$

Appendix 3

The ABCD Matrix for the Single Stage Four Phase S.D.

(4). The D Parameter





Positive Sequence

$$i_1 = V_1 (G_1 + jwC_1)$$

$$i_5 = V_1 (G_1 - wC_4)$$

$$\left(\frac{i_1}{i_5}\right)_+ = \frac{G_1 + jwC_1}{G_1 - wC_4}$$

$$\therefore D15+ = \frac{1 + jwC_1R_1}{1 - wC_4R_1}$$

For equal R's, C's

$$D15+ = \frac{1 + jwCR}{1 - wCR}$$

Negative Sequence

$$i_1 = \overline{V_1}(G_1 + jwC_1)$$

$$i_5 = V_1 (G_1 + wC_4)$$

$$\left(\frac{i_1}{i_5}\right)_- = \frac{G_1 + jwC_1}{G_1 + wC_4}$$

$$\therefore D15- = \frac{1 + jwC_1R_1}{1 + wC_4R_1}$$

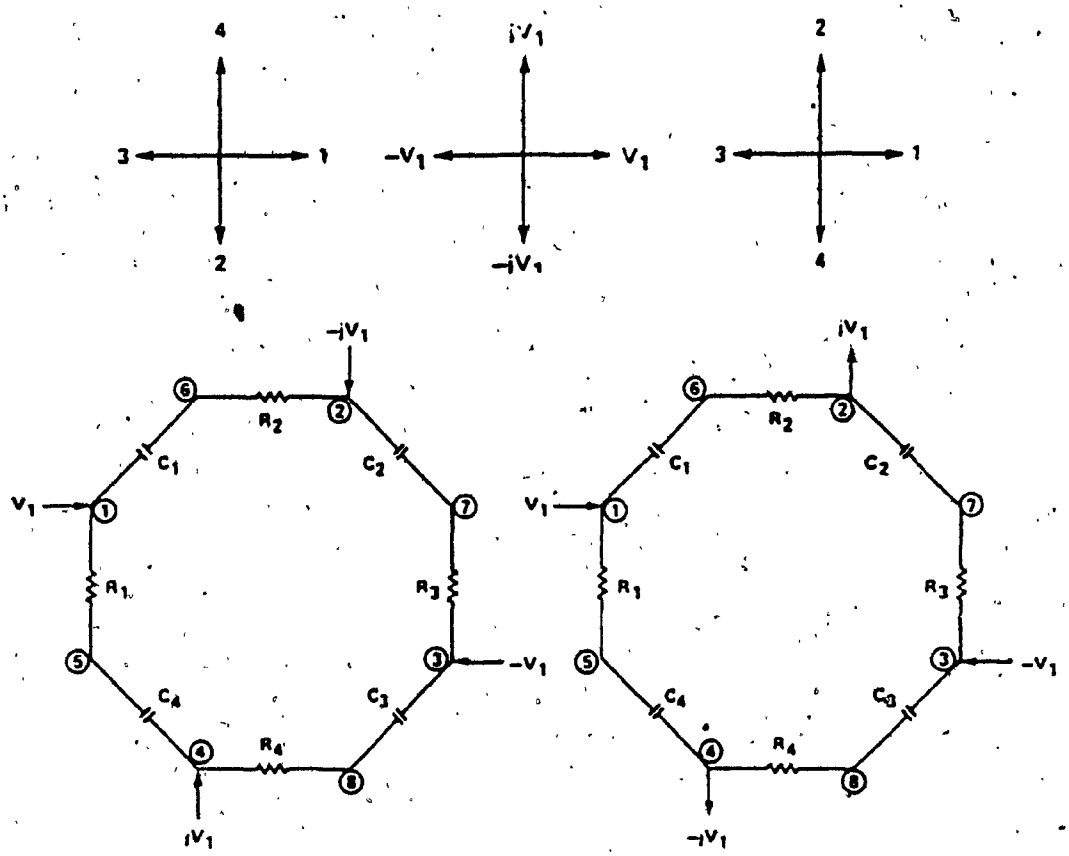
For equal R's, C's

$$D15- = \frac{1 + jwCR}{1 + wCR}$$

Appendix 3

The ABCD Matrix for the Single Stage Four Phase S.D.

(5) The Whole Matrix



Positive Sequence

$$\begin{bmatrix} A51 & B51 \\ C51 & D51 \end{bmatrix} = \frac{1}{(1 - wC_4R_1)} \begin{bmatrix} A1 & B1 \\ C1 & D1 \end{bmatrix}$$

Where

$$\begin{bmatrix} A1 & B1 \\ C1 & D1 \end{bmatrix} = \begin{bmatrix} 1 + jwC_4R_1 & R_1 \\ wC_4(j+1) + wC_1(j-1) & 1 + jwC_1R_1 \end{bmatrix}$$

For equal R's, C's

$$\begin{bmatrix} A51 & B51 \\ C51 & D51 \end{bmatrix} = \frac{1}{(1 - wCR)} \begin{bmatrix} 1 + jwCR & R \\ 2jwC & 1 + jwCR \end{bmatrix}$$

Negative Sequence

$$\begin{bmatrix} A51 & B51 \\ C51 & D51 \end{bmatrix} = \frac{1}{(1 + wC_4R_1)} \begin{bmatrix} A2 & B2 \\ C2 & D2 \end{bmatrix}$$

Where

$$\begin{bmatrix} A2 & B2 \\ C2 & D2 \end{bmatrix} = \begin{bmatrix} 1 + jwC_4R_1 & R_1 \\ wC_4(j-1) + wC_1(j+1) & 1 + jwC_1R_1 \end{bmatrix}$$

For equal R's, C's

$$\begin{bmatrix} A51 & B51 \\ C51 & D51 \end{bmatrix} = \frac{1}{(1 + wCR)} \begin{bmatrix} 1 + jwCR & R \\ 2jwC & 1 + jwCR \end{bmatrix}$$

Appendix 4

TESTING OF POLYPHASE NETWORKS

APPENDIX 4

TESTING THE POLYPHASE NETWORK IN THE TRANSMIT MODE

(A) Testing the Polyphase Network in the Transmit Mode

1 - Install the hybrid in the test jig.

2 - Turn the power supply on.

3 - Obtain a reference level reading

Generator frequency = 1004 Hz

Output level = 5.0 dBm

Selective voltmeter frequency = 62.996 (20 Hz bandwidth)

Measure reference level = AR dBm.

4 - Repeat measurements for the input frequencies

Pass-band 300, 400, 3000 and 3400

Stop-band 175, 300, 600, 900, 1200, 1500, 1800, 2100, 2400, 2700, 3000 and 3300.

Ensure that the selective voltmeter frequency is 64000 - f in the pass-band and 64000 + f in the stop-band.

Assume the readings in dBm at these frequencies to be A1, A2, ... ,A16.

5 - Calculate the referenced loss at each frequency from the equation

$L_i = AR - A_i$

6 - The following specifications have to be met.

(i) $-0.2 \leq L1 \leq 0.5$

(ii) $-0.2 \leq L2 \leq 0.3$

(iii) $-0.2 \leq L3 \leq 0.3$

(iv) $-0.2 \leq L4 \leq 0.3$

All hybrids falling outside the specified range fail in the pass-band.

7 - Calculate the power average between 600 and 3300 Hz in the stop-band from the equation

$$\text{Power Average} = -10 \log_{10} (0.1) \sum_{i=7}^{i=16} 10^{(-0.1) L_i}$$

8 - The following specifications have to be checked.

(i) $L5 \geq 22$

(ii) $L6 \geq 42$

(iii) Any value of L7, L8, ... , L16 ≥ 50

(iv) Power average ≥ 61.9

All hybrids falling outside the specified range fail in the stop-band.

The foregoing procedure was programmed using an HP85 minicomputer to allow fast automatic testing of hybrids.

(B) Testing the Polyphase Network in the Receive Mode

1 - Install the shorting bar in the test jig.

2 - Turn the power supply on.

3 - Obtain a reference level reading.

Generator frequency = 62.996 kHz

Output level = -10 dBm

Selective voltmeter frequency = 1004 Hz (20 Hz bandwidth)

Measure reference label = BR dB

4 - Repeat measurements for input frequencies 63700, 63600, 61000 and 60600 Hz (pass-band), 64175, 64300, 64600, 64900, 65200, 65500, 65800, 66100, 66400, 66700, 67000 and 67300 Hz (stop-band).

Ensure that the selective voltmeter frequency is 64000 - f in the pass-band and f - 64000 in the stop-band.

Assume the readings in dBm at these frequencies to be BL1, BL2, ... ,BL16.

5 - Turn the power supply off, insert the hybrid and turn the power on again.

6 - Obtain a reference reading as in Step 3; assume the reference level to be R dBm.

7 - Repeat the measurements as in Step 4. Assume the readings in dBm to be A1, A2, ... ,A16.

8 - Calculate the referenced losses L1, L2, ... ,L16 from the equation

$$L_i = BL_i - A_i - (BR - R)$$

9 - The following specifications have to be met.

(i) $-0.2 \leq L1 \leq 0.5$

(ii) $-0.2 \leq L2 \leq 0.3$

(iii) $-0.2 \leq L3 \leq 0.3$

(iv) $-0.2 \leq L4 \leq 0.3$

All hybrids falling outside the specified range fail in the pass-band.

10 - Calculate the power average in the stop-band from the equation

$$\text{Power Average} = -10 \log_{10} (0.1) \sum_{i=7}^{i=16} 10^{(-0.1) L_i}$$

11 - The following specifications have to be checked.

(i) $L5 \geq 22$

(ii) $L6 \geq 42$

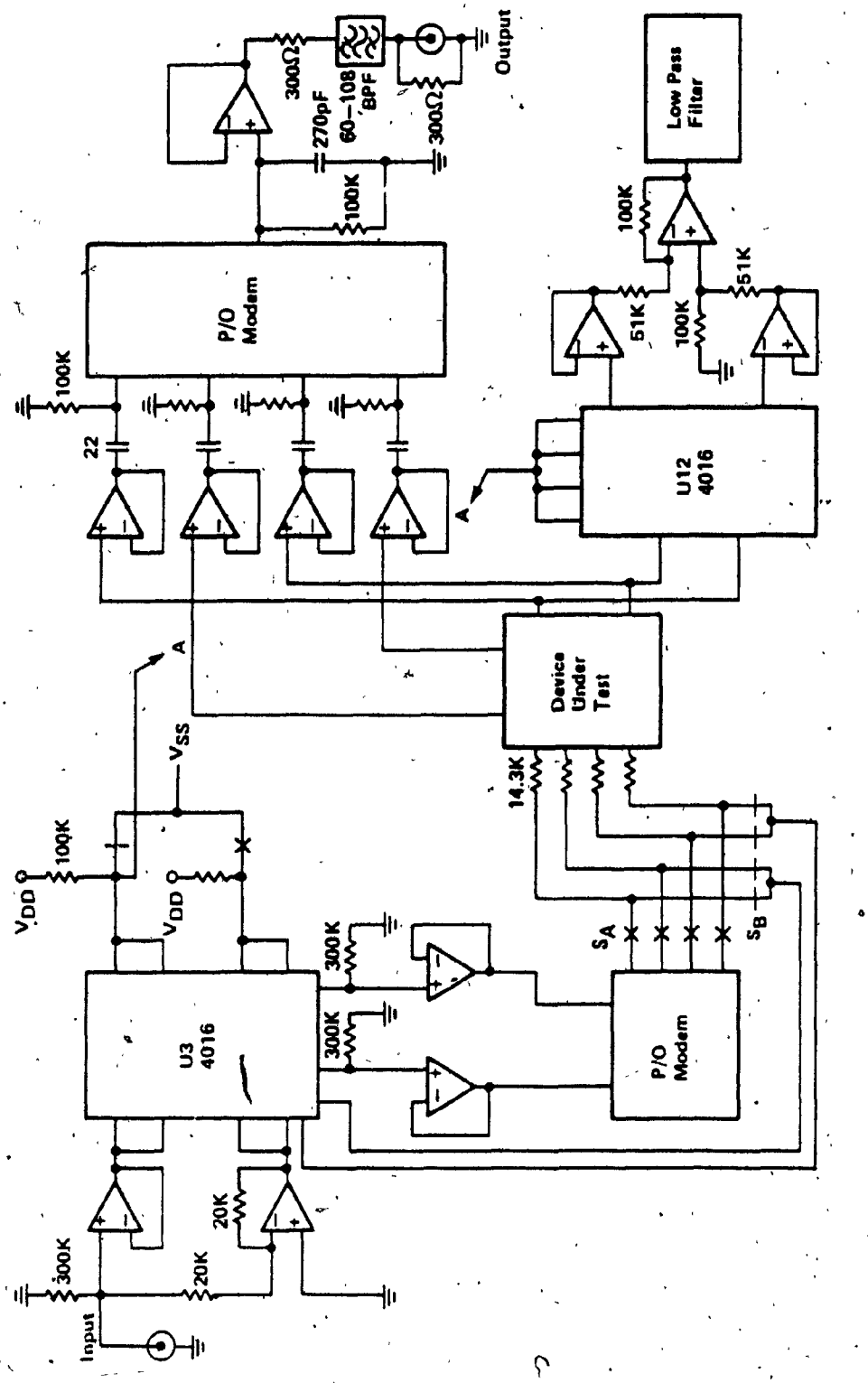
(iii) Any value of L7, L8, ... ,L16 ≥ 50

(iv) Power average ≥ 61.9

All hybrids falling outside the specified range fail in the stop-band.

The procedure was programmed using an HP85 minicomputer to allow fast automatic testing of hybrids.

(C) Test Jig 'Schematic'



(D) Block Diagram of the Polyphase Test Equipment