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NOVEL CMOS CURRENT MIRRORS DESIGN AND THEIR APPLICATIONS

NOURI SABIH DAOUD

A Thesis
in
The Department
of
Electrical and Computer Engineering

Presented in Partial Fulfillment of the requirements
for the degree of Master of Applied Science at
Concordia University
Montreal, Quebec, CANADA

June 1992

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ABSTRACT

NOVEL CMOS CURRENT MIRRORS DESIGN AND THEIR APPLICATIONS

NOURI SABIH DAUD

Current mirror is one of the basic circuits which is widely used in linear analog integrated circuits as a building block. The efficient implementation of these circuits is, therefore, a major concern in the VLSI technology. In addition to *speed*, two other factors are generally considered in the VLSI design of a chip; the *area of the chip* and its *power consumption*. Consequently, minimization of these parameters can be regarded as a design goal in the VLSI implementation of current mirrors.

In this thesis some novel current mirror designs for VLSI MOS technology are presented. Specifically we consider twelve different current mirrors (sinks & sources) with two fixed current ratios; one current ratio which is greater than unity and the other one which is less than unity. Our approach is to eliminate the mask misalignment effect and to reduce the required area for the current mirror on the chip at the same time. The proposed technique is technology independent in the sense that it can be applied for any VLSI technology of any size.

The operation of the current mirrors, presented in this thesis is discussed, and their different parameters are evaluated by both analysis and simulation. The results represent the characteristics of different structures of these current mirror circuits. In addition, this study establishes a methodology for using the MOS transconductance (K) factor in designing a novel current mirror with consequent reduction of the area. This method provides an idea of possible extension of this design technique for industrial applications.

A statistical study of the output current errors caused by time independent random difference in the parameters of the MOSFET devices, is also presented. The two most important time-independent parameters, namely, *transconductance* and *threshold voltage* are selected for this study. It shows that for the same gain and minimum required area, the percentage error in the output current for the new current mirrors is 20% less than the ones in regular NMOS or PMOS current mirrors.

A method of increasing the current gain of the new current mirrors by cascading them is presented. A voltage control technique for the DC current ratio is also described. The effectiveness of this technique in controlling the output current is verified by analysis and simulation.

Finally, an application of the novel current mirror circuit is considered in the design of an *Operational Transconductance Amplifier* (OTA) circuit. A selected structure for an OTA which has the advantage of using the new current mirror will result in a remarkable increase in the transconductance value of the OTA. Different techniques for increasing the OTA transconductance are discussed, showing the advantage of using the new current mirrors over the regular current mirror in the OTA circuit from the point of view of chip area and power consumption.

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To my Mother and Father.

To my Wife and Daughter.

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LIST OF ACRONYMS AND SYMBOLS

CMOS	Complementary metal oxide semiconductor
FET	Field Effect Transistor
IC	Integrated Circuit
LSI	Large-Scale Integration
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NCMOS	New CMOS
NMOS	N-channel Metal Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	P-channel Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
C_{ox}	the gate oxide capacitance per unit area
f_{co}	cutoff frequency
g_m	transconductance
i_O	instantaneous output current
i_o	AC output current
I_o	DC output current
K	transconductance parameters ratio
K_n	NMOS transconductance parameter
K_p	PMOS transconductance parameter
L	length of the gate
Q_f	the fixed charge in the gate oxide
Q_B	the depletion region charge in the substrate
t_{ox}	thickness of the gate insulator (oxide)
V_T	device threshold voltage
W	width of the gate
β	MOS device gain factor
ϵ	permittivity of the gate insulator
λ	empirical channel length modulation factor
σ_I	the standard deviation of I
$\sigma^2 I$	the variance of I
Φ_{MS}	the gate-semiconductor work function difference
Ψ_B	the substrate fermi potential

CHAPTER 1

INTRODUCTION

1.0. GENERAL

Metal oxide semiconductor (MOS) field effect transistor (FET) integrated circuit (IC) technology has seen widespread application first in digital circuitry, which was more tolerant of variations in device gains and device thresholds. Since the late 1970s, interest in using MOS technology for analog circuits has been increasing rapidly. As circuits have advanced to higher levels of integration, there has been a need to interface these integrated circuits directly with signals from the external world which are primarily analog in nature. MOS processing has improved to the appropriate level of consistency and uniformity such that IC analog circuit design with MOS has become practical.

MOS analog circuits can be more dense than corresponding bipolar circuits. A MOS operational amplifier (op. amp.) takes 100 to 200 mil^2 , which is one-third to one-half of the die area of the equivalent in characteristics to bipolar version and consumes 1 to 10 mW as compared to 100mW in the bipolar version. With such small size and low power, use of 20 to 30 op. amps in a single chip is not at all uncommon. MOS circuits also have a unique ability to store charge on a node for periods of several milliseconds. A high-input impedance MOS transistor can be used to sense this charge nondestructively.

Bipolar transistors have higher transconductance, higher output drive capability and lower noise. In terms of absolute performance, bipolars will therefore prevail in the foreseeable future.

For example, there are few single MOS op. amps packaged for sale as off-the-shelf components. However, the ability to realize digital and analog circuits on the same large-scale integration (LSI) technology has pushed MOS technology into the realm of linear circuit design[1]. IC manufacturing has already become a more accurate and automated technique in the past decade. Now analog MOS circuit design can be implemented accurately by using very large scale integration (VLSI) technology.

1.1. MOSFET TRANSISTOR STRUCTURE

Figures 1.1a and 1.1b show the basic structure of the MOSFET transistor. It basically consists of a silicon substrate which is part of a silicon wafer on which the circuit is fabricated. The wafer is a cut from a single crystal which has been lightly doped with N or P type impurities during the crystal growth [2].

There are also two heavily diffused regions of opposite polarity from the substrate called the source and the drain [3], and a metal or polysilicon gate which sits above a thin layer of insulator (silicon dioxide) and lies between the drain and the source. There are metal connections on the drain and the source which make the wiring with the other MOS transistors on the chip (wafer) possible. The creation of the heavily doped areas, the insulating material film in some regions, the polysilicon gates on some specific areas, and the metal connections and wiring in some selected areas is done by a fabrication process which is called “The Masking Process”[4] will be discussed more in sec. 1.3.2.

1.2. MOS DEVICE EQUATIONS

The MOS transistor is a voltage controlled device. The current passing from the drain to source is controlled by the voltage applied between the gate and source of the MOS transistor. It has three regions of operation depending on the V - I characteristics of that region.

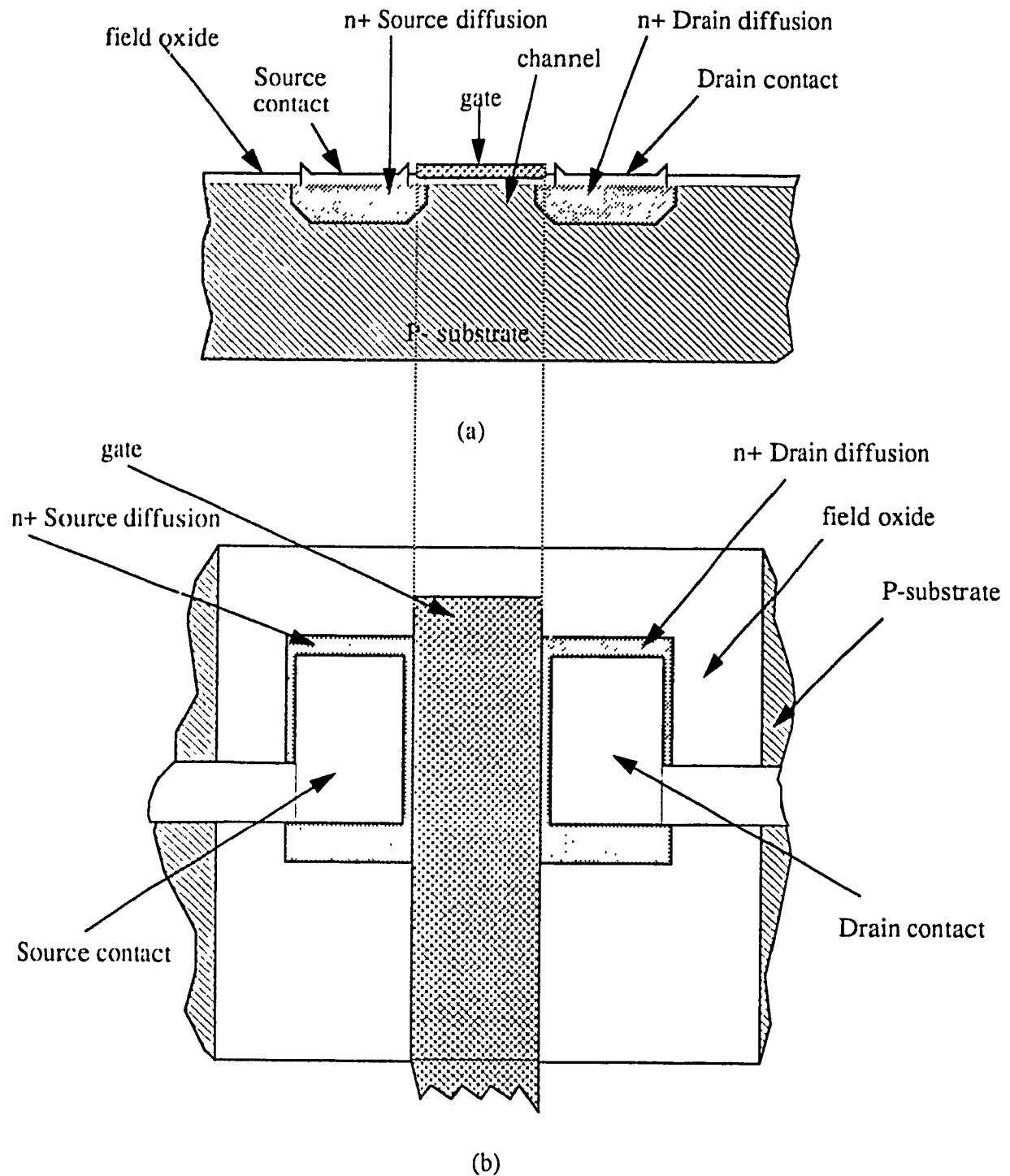


Fig. 1.1
Basic structure of the n-channel MOSFET transistor (a) Side cut. (b) Top view

These regions are:

1. Cutoff region.
2. Linear region.
3. Saturation region.

The general equations for the MOS transistor which describe its behavior in the three regions are:

$$i_{DS} = 0 \quad v_{GS} - V_T \leq 0 \quad \text{cutoff} \quad (1.1a)$$

$$i_{DS} = \beta (v_{GS} - V_T) \cdot v_{DS} - 0.5 (v_{DS})^2 \quad 0 < v_{DS} < v_{GS} - V_T \quad \text{linear} \quad (1.1b)$$

$$i_{DS} = 0.5 \beta (v_{GS} - V_T)^2 \quad 0 < v_{GS} - V_T < v_{DS} \quad \text{saturation} \quad (1.1c)$$

where

i_{DS} is the drain-source current,

v_{GS} is the gate to source voltage,

V_T is the device threshold voltage,

β is the MOS device gain factor.

The factor β depends on both the process parameters and the device geometry and it is given by:

$$\beta = \frac{\mu \cdot \epsilon}{t_{ox}} \cdot \frac{W}{L} \quad (1.2)$$

where μ is the effective surface mobility,

ϵ is the permittivity of the gate insulator,

t_{ox} is the thickness of the gate insulator (oxide),

W is the width of the gate,

L is the length of the gate.

The factor $(\mu \epsilon / t_{ox})$ depends on the process technology and contains all the process terms [4]. It is called the K factor. Because of the difference between the mobility of electrons (in NMOS device) and the mobility of the holes (in PMOS device), we will label the K as K_n for the NMOS device and as K_p for the PMOS device.

The value of K_n is $40 \times 10^{-6} \text{ A/V}^2$ and the value of K_p is $12 \times 10^{-6} \text{ A/V}^2$. Their values are fixed because of certain doping and masking processes. The gain factor of the NMOS transistor is:

$$\beta_n = K_n \cdot \frac{W}{L} \quad (1.3)$$

and the gain factor of the PMOS transistor is:

$$\beta_p = K_p \cdot \frac{W}{L} \quad (1.4)$$

The current i_{DS} for the NMOS transistor in the saturation region will be:

$$i_{DS} = \frac{K_n}{2} \cdot \frac{W}{L} \cdot (v_{GS} - V_{Tn})^2 \quad (1.5)$$

and the current i_{SD} for the PMOS transistor in the saturation region will be:

$$i_{SD} = \frac{K_p}{2} \cdot \frac{W}{L} \cdot (v_{SG} - V_{Tp})^2 \quad (1.6)$$

where $V_{Tn} = 0.7$ volt for the NMOS transistor when the source to bulk voltage is equal to zero volt and $V_{Tp} = 0.8$ volt for the PMOS transistor under the same condition.

Eqn. (1.1c) assumes that the current i_{DS} in the transistor channel is saturated and is independent of the applied drain to source voltage, while in practice the drain current increases slightly with the increase of drain to source voltage v_{DS} .

A more accurate model that takes this behavior into account is represented by the following equation:

$$i_{DS} = \frac{\beta}{2} \cdot (v_{GS} - V_{Tn})^2 \cdot (1 + \lambda v_{DS}) \quad (1.7)$$

where λ is the empirical channel length modulation factor [4] having the value of 0.01 V^{-1} for NMOS transistor and 0.03 V^{-1} for PMOS device [5].

1.3. MOSFET FABRICATION PROCESS

In this section we will present a brief explanation of the fabrication process of the MOSFET transistor in steps and give an example of the fabrication of the CMOS inverter to make the steps more clear. This will help us visualize where the main fabrication problems are located to enable us to attempt minimizing the effect of these problems on the circuits fabricated.

1.3.1. OXIDATION

Before the Masking process it is important to select the size of the lightly doped silicon wafer and pass it through the oxidation process to create an insulating layer of silicon dioxide (SiO_2).

Oxidation of silicon is achieved by heating the silicon wafer in an oxidizing atmosphere such as oxygen or water vapor [4]. It creates an insulating layer of SiO_2 on the silicon wafer, and it consumes silicon because of this creation. The importance of oxidation process is due to the fact that different structures and manufacturing techniques used to make the MOS integrated circuits rely heavily on the properties of the silicon dioxide.

It is important to select properly the size of a lightly doped wafer for oxidation before the masking process. Since SiO_2 has approximately twice the volume of the silicon, the silicon dioxide layer grows almost in both vertical directions. This effect is shown in Fig. 1.2 for an n-channel MOS device in which SiO_2 (field oxide) projects above and below the unoxidized silicon surface[4].

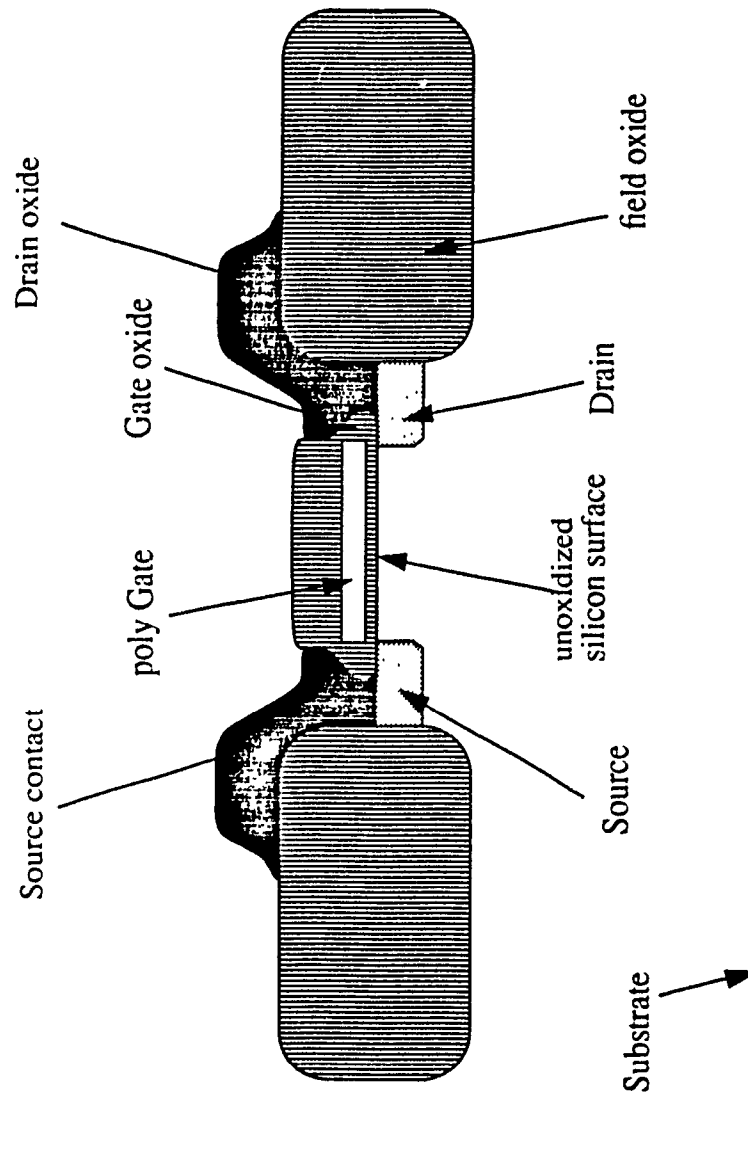


Fig. 1.2

NMOS cut through showing the growth of field oxide in both vertical directions

1.3.2. MASKING PROCESS

Masking is the process of applying a series of photo masks over a wafer that has passed through the oxidation process. A photomasking is done by placing over the wafer a square glass plate with a patterned emulsion or metal film on one side. Each mask following the first must be carefully aligned to the previous pattern on the wafer. Much of the alignment equipment has traditionally involved manual operation of alignment.

With manual alignment equipment, the wafer is held on a vacuum chuck and carefully moved into position below the mask using an adjustable x - y stage.

VLSI designs with minimum-size geometrical features measuring $1.25\ \mu\text{m}$ (minimum line width or space) require an alignment tolerance of better than $\pm 0.25\ \mu\text{m}$. Computer-controlled alignment equipment has been developed to achieve this level of alignment precision[6].

To get a clear idea about the masking process, we discuss the P-well process for a CMOS inverter implementation. This process uses the N-type substrate (wafer) and it creates the P-type well for the N-channel transistor, and builds the P-channel transistor in the *native* N-substrate. Fig. 1.3 shows the major steps involved in a typical CMOS process. The masks that are used in each process step are shown, in addition to a sample cross section on the N and P transistors. Fig. 1.3, shows that the mask levels are not organized by component function, rather they reflect the processing steps[4].

The masking processes are as follows:

- (1) The first mask defines the P-well; the N-channel transistor will be fabricated in this well. The field oxide is etched away to allow a deep diffusion, Fig. 1.3a.
- (2) The second mask defines where thin oxide areas are needed to implement the transistor gates and allow implantation of P or N-type diffusions for transistor source/drain regions, Fig. 1.3b.

(3) Polysilicon gate is implemented by covering the surface with the polysilicon material and etching the required pattern, Fig. 1.3c.

(4) A P-plus (P^+) mask is then used to delineate those thin-oxide areas that are to be implanted as P^+ diffusions. Hence a thin oxide area exposed by a P-plus mask will become a P^+ diffusion area. If the P-plus area is in the N-substrate, then a P-channel transistor or a P-type wire or ohmic contact will be constructed, Fig. 1.3d.

(5) This masking step usually uses the complement of the P-plus mask, although an extra mask is normally not needed. The absence of a P-plus region over a thin-oxide area indicate that the area will be an N^+ diffusion, Fig. 1.3e. The N^+ diffusion in the N-substrate allows an ohmic contact to be made. Following this step, the surface of the chip will be covered with a layer of SiO_2 .

(6) This mask will define the contact cuts. This involves etching the SiO_2 down to the contacted surface, Fig. 1.3f.

(7) Metallization is applied to allow metal to contact diffusion regions or polysilicon regions and cover the surface. After that the etching of the metal will be done by another mask, Fig. 1.3g.

After completing the masking steps, the wafer is passivated and openings to the bond pads are etched to allow for wire bonding. Passivation protects the silicon surface against the contaminants that can modify the circuit behavior in deleterious ways[4]. Fig. 1.3h shows the whole masks of Fig. 1.3a to g one over the other sequentially. Only the P-plus two masks are not shown to give a clear view for the masks underneath it.

1.4. CURRENT SOURCES AND CURRENT MIRRORS

Current sources are used extensively in MOS analog circuits, both as biasing elements and as active loads to obtain a high ac voltage gain. MOS current sources are current mirrors constructed by passing a reference current through a diode-connected (gate tied to drain) MOSFET. The voltage developed across it is applied to the gate and the source of a second MOSFET which provides the output current as shown in Fig. 1.4. To

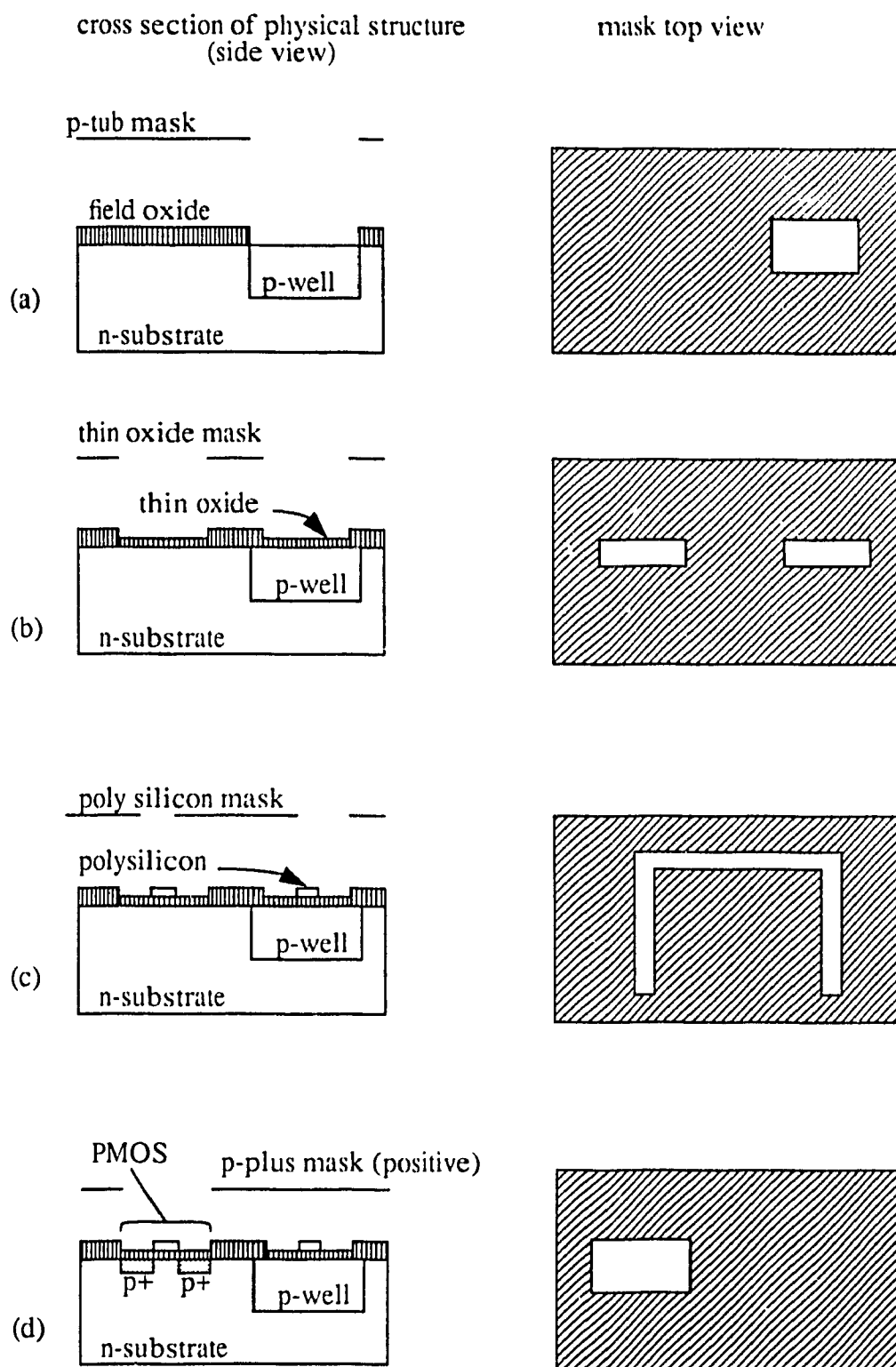
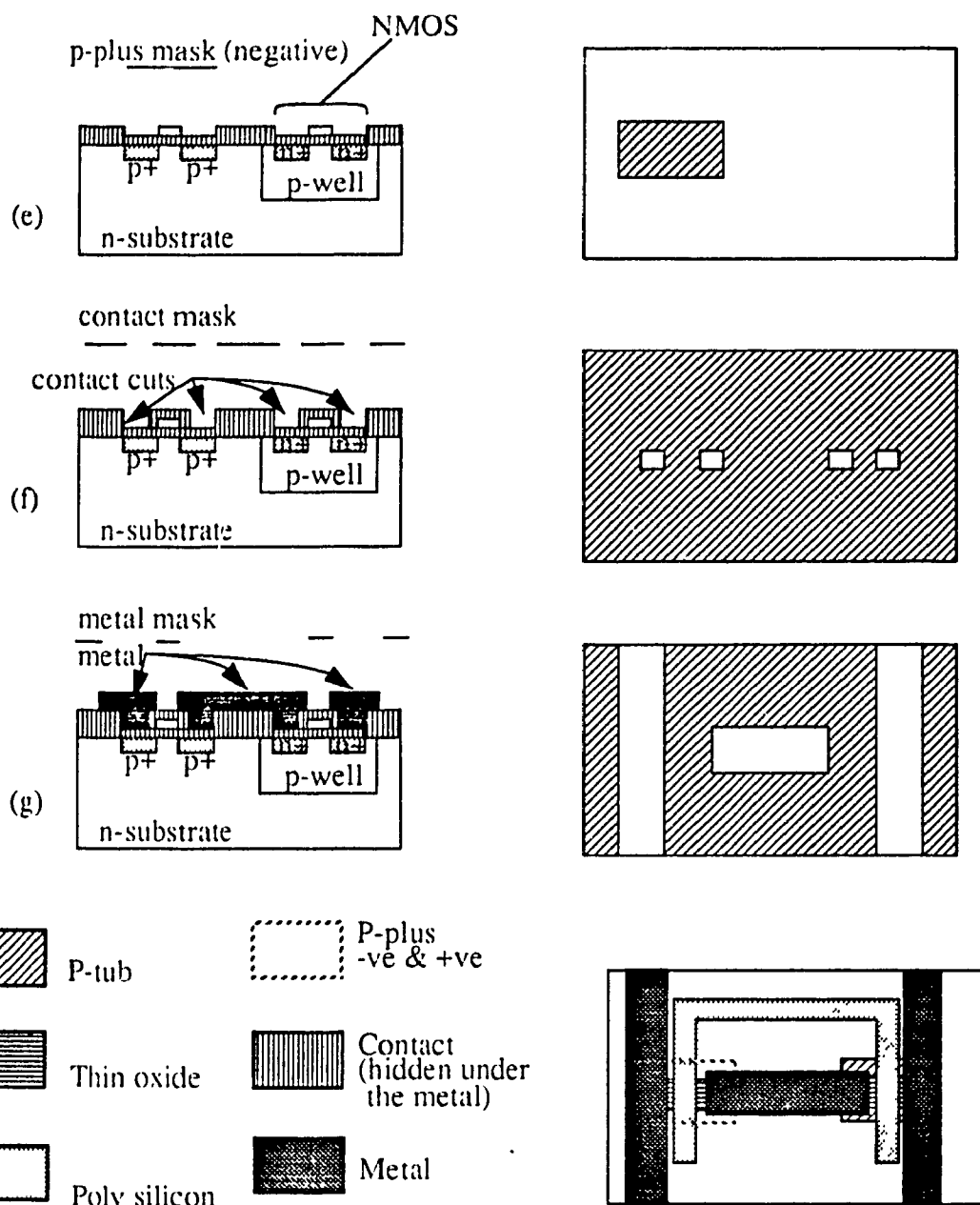


Fig. 1.3
Typical P-well CMOS process steps with corresponding masks required[4]



(h)

The whole masks shown one over the other sequentially.

(Note: for clear view the P-plus masks positive and negative are not shown completely)

Fig. 1.3
(continued)

increase the output impedance of the current source, the channel length of transistor Q_2 should be large.

The W/L ratio of transistor Q_2 can be scaled up or down to make I_O either larger or smaller than I_R . It is also possible, and in fact quite common, to have several current source outputs by placing other devices in parallel with Q_2 as the Fig. 1.4 shows. All output currents will scale up or down together if I_R changes, such as from power supply or temperature fluctuations. The use of current sources for biasing (to the extent that they are ideal current sources) makes the circuit performances insensitive to such fluctuations[1].

A single MOSFET also behaves like a current source because the channel current stays almost steady with the variation of drain-to-source voltage. Further, it has a high output impedance in the saturation region.

Any current mirror is either a current sink to current source converter or a current source to current sink converter. The current mirror needs two basic things, a reference current and a reference voltage.

1.4.1. REVIEW OF CURRENT MIRRORS

Current mirror is universally employed to generate a DC output current from a constant current of reference source. To get a good idea about the current mirrors we discuss the basic structure as illustrated in Fig. 1.5a.

The current mirror in Fig. 1.5a consists of two enhancement MOSFET's, Q_1 & Q_2 having the same threshold voltage V_T , but possibly different W/L ratios. Transistor Q_1 is fed with the reference current I_R from a current source, and the output current I_O is taken at the drain of transistor Q_2 which must be operated in the saturation (pinch-off) region.

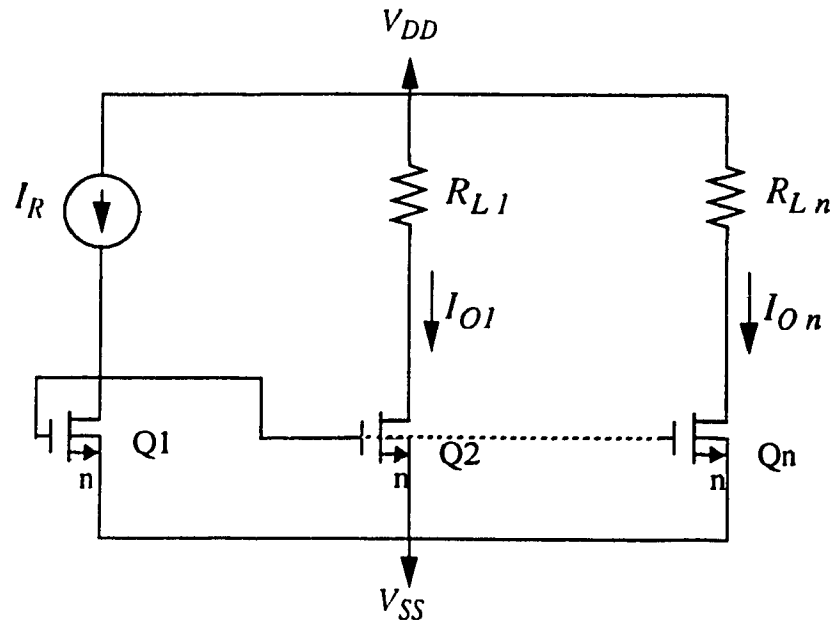


Fig. 1.4

Basic structure of multiple output current mirror

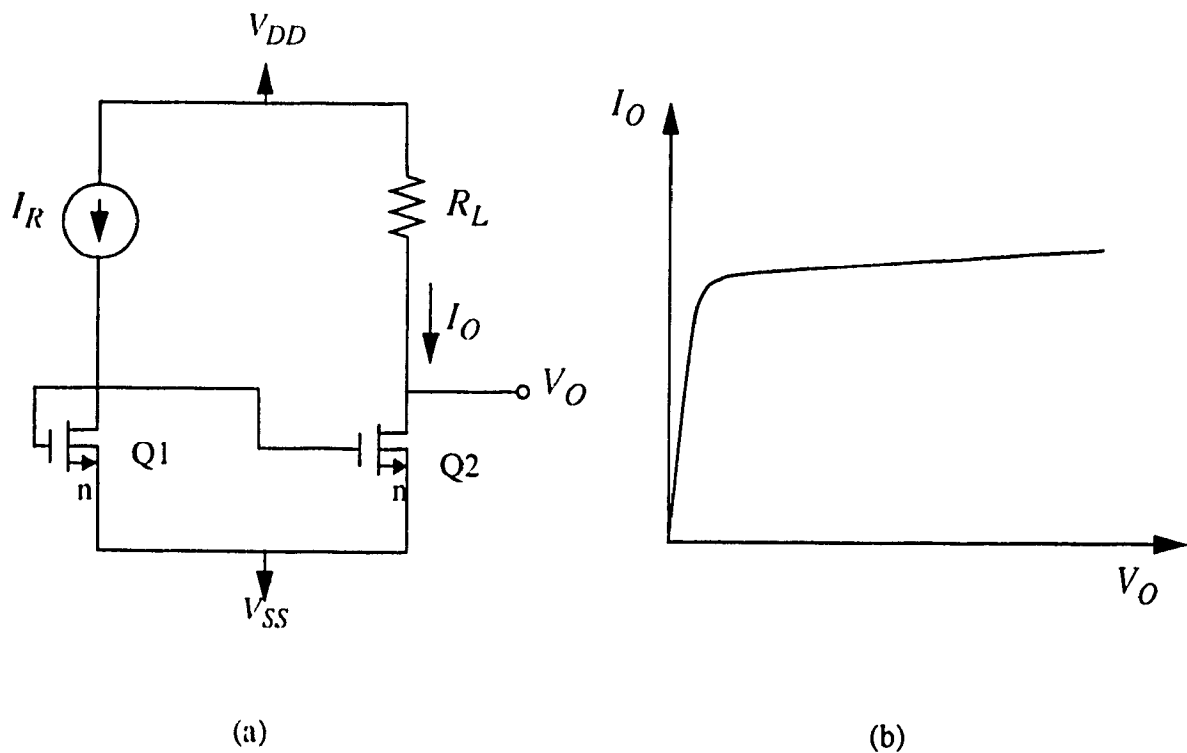


Fig. 1.5

Current mirror with two enhancement MOSFETs

(a) circuit diagram (b) $I_O - V_O$ characteristics

For Q_1 , the instantaneous current equation can be written as:

$$i_R = \beta_1 \cdot (v_{GS} - v_T)^2 \quad (1.8)$$

where v_{GS} is the instantaneous gate-to-source voltage corresponding to a drain current of i_R . Since the gate of Q_2 is connected to the gate of Q_1 , it will have the same v_{GS} .

The instantaneous output current equation for Q_2 is:

$$i_O = \beta_2 \cdot (v_{GS} - v_T)^2 \quad (1.9)$$

For simplicity the effect of the finite output resistance in eqn. (1.8) and eqn. (1.9) are neglected.

Dividing eqn. (1.9) by eqn. (1.8) we obtain:

$$\frac{i_O}{i_R} = \frac{\beta_2}{\beta_1} \quad (1.10)$$

Since the devices parameters are identical for both Q_1 and Q_2 then:

$$\frac{i_O}{i_R} = \frac{W_2/L_2}{W_1/L_1} \quad (1.11)$$

Ideally i_O will be a multiple of i_R whose value is determined by the device geometry. In practice, the value of i_O will be multiplied by a certain factor which depend on the value of v_{DS} , because of the finite output impedance of the output transistor Q_2 . Fig. 1.5b shows i_O as a function of v_O . This is simply the $i_D - v_{DS}$ characteristic curve for Q_2 corresponding to the value of v_{GS} established by passing i_R through the transistor Q_1 [7].

The current mirror structure has been well developed to stabilize the current over a range of variable loads. This has been done by keeping the voltage v_{DS} of the output transistor constant, or by increasing the output impedance of the current mirror. Different circuits have been discussed such as Wilson, Modified Wilson, and Cascode current mirrors in sink and source versions. The operation of all the circuits is based on eqn. (1.11), which is basically a geometrical ratio that increases with the area of the output MOSFET.

1.5. MOS VLSI ANALOG CIRCUITS - PROBLEMS OF IMPLEMENTATION

Analog MOSFET circuits differ from digital circuits in their operating condition. MOSFETs in analog circuits always operate in a saturation region with a constant DC drain current required to stabilize the operating point voltage of the circuit.

The sources of mismatches between the current mirrors are (1) the threshold voltage, (2) the channel length modulation and (3) the mask misalignment. The threshold voltage and channel length modulation as a source of mismatch and the suggested solutions for this problem are given in detail in sec. 2.5. The mask misalignment problem will be discussed in the following paragraphs.

Since the drain current and the operating point voltage are functions of the MOSFET size. Hence, any variation in the size due to the misalignment of the masks will cause a change in both of the drain current and the operating point voltage at the same time.

Fixing both the drain current and the operating point voltage at the same time by making exact alignment is a difficult task. It will produce more defective products in the fabrication process, decreasing yield. Thus it is necessary to fix one variable, usually the drain current, in order to make the mask alignment easier and to reduce the percentage of defective products. Exact mask alignment is extremely difficult. A deviation of each mask position by 20 to 30% of the minimum line width is usually expected [8]. Thus as more masks are used, we will have an increasing number of faulty chips. Since this thesis is mainly concerned with current mirrors, we shall consider now the alignment problem in more detail for the current mirrors.

The current mirror circuit is mostly used to give an output current related to a given reference current. Normally the value of the output current will be decided by the designer, depending on the requirement of the circuit to be driven by the current mirror. Thus the

output current value will be a certain ratio of the reference current, and this ratio is achieved by fixing the ratio of the size of the two transistors Q_1 and Q_2 in Fig. 1.5a. It is clear, in eqn. (1.11) that the current ratio can be controlled by changing either (W) or (L) or both of them.

In order to minimize the chip area, minimum dimensions within bounds for both Q_1 and Q_2 transistors should be chosen to obtain the i_O / i_R ratio as desired. Theoretically this can be achieved, but problem arises in implementation, particularly in the masking process. In fact, the major problem is due to the misalignment of the masks.

The misalignment of the masks affects analog circuits more than the digital circuits because any change in the transistor size will disrupt the DC level of the circuit which will disturb the operating point, affecting finally the AC operation. For simplicity, if it is assumed that Q_1 and Q_2 transistors have the same length (L), eqn. (1.11) becomes:

$$\frac{i_O}{i_R} = \frac{W_O}{W_R} \quad (1.12)$$

where W_O and W_R are the widths of Q_2 and Q_1 , respectively. As an example, let the misalignment factor in the masking process be $\pm 0.25 \mu\text{m}$ in the $1.2 \mu\text{m}$ technology[6], $W_R = 1.25 \mu\text{m}$ and $W_O = 6.25 \mu\text{m}$ for a current ratio of 5. Then the error in the current ratio becomes:

$$\frac{i_O}{i_R} = \frac{6.25 \pm 0.25}{1.25 \pm 0.25} = 5 \pm 0.67$$

We observe that a misalignment in mask position of 20% of the minimum size ($1.2\mu\text{m}$), gives a variation of 13.4% in the desired current ratio. One solution to this problem is to use a proper layout. The exact one-to-five ratio can be implemented by using five duplicates of the transistor Q_1 . In this way, the tolerance on W_O is simply multiplied by the nominal current gain, assuming that ΔW is the same for all transistors i.e.,

$$\frac{i_O}{i_R} = \frac{5 \times (1.25 \pm 0.25)}{1.25 \pm 0.25} = 5$$

The layout technique is shown in Fig. 1.6. This technique has some limitations, i.e., the current ratio has to be an integer number for minimum area, and it needs a larger area than the previous technique. Further ΔW may not be the same for all the transistors. However ΔW matching errors are small compared to the other error contributions. Usually one does not try to scale the length because length tolerances are greater than width tolerances, due to diffusions under the polysilicon gate[9]. As an example if the under diffusion part tolerance is 5% of the gate length and the length is scaled down by 50% then the tolerance will increase to 10%. Under the same condition of under diffusion part tolerance of 5% if the gate length stay unchanged and gate width is doubled the percentage error will not increase.

The other solution is to increase the area of both transistors (reference and output) which makes the percentage errors smaller. As an example, we take the previous current mirror with the same ratio and error but with different areas. Thus, assume $W_R = 12.5 \mu\text{m}$ and $W_O = 62.5 \mu\text{m}$ then:

$$\frac{i_O}{i_R} = \frac{62.5 \pm 0.25}{12.5 \pm 0.25} = 5 \pm 0.08$$

In this case the percentage error has been reduced from 13.4% to 1.6%. Thus we can conclude that if we are seeking to achieve one advantage i.e, reducing the misalignment effect, we will have to accept the disadvantage of increased area.

The problem can also be solved by maintaining the size of both transistors Q_1 and Q_2 equal, or by using a more advanced manufacturing technology. For example, if the misalignment error in previous example can be reduced from 20% to 10%, then the effect on current ratio will be:

$$\frac{i_O}{i_R} = \frac{6.25 \pm 0.12}{1.25 \pm 0.12} = 5 \pm 0.36$$

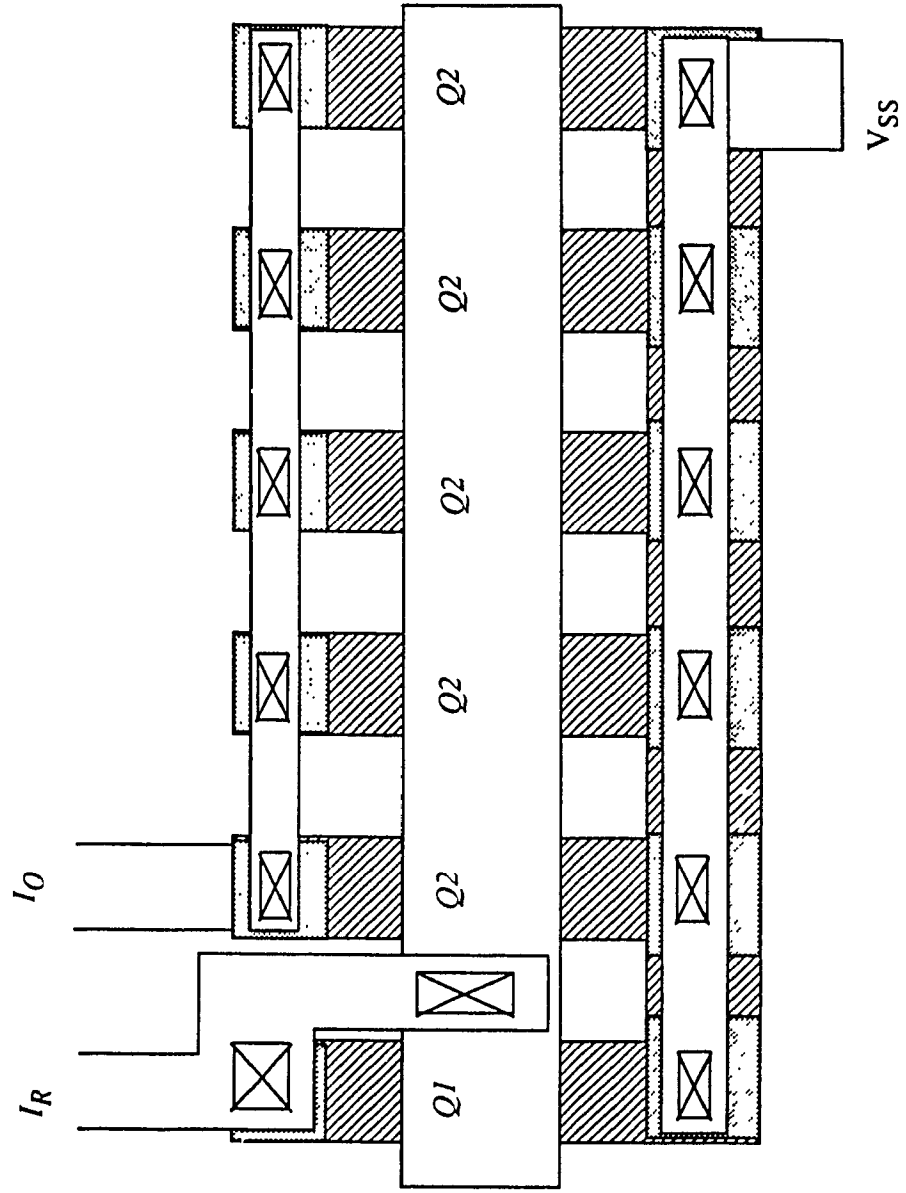


Fig. 1.6
Layout technique to eliminate the misalignment problem

From the previous discussion it can be concluded that an efficient way to solve the misalignment problem is by making use of equal size transistors. In which case the current gain should be achieved from another parameter in the drain current equation, eqn.(1.5) or eqn. (1.6), rather than from the device geometries.

1.6. SCOPE OF THE THESIS

The purpose of this thesis is to present novel current mirror designs for efficient implementation in VLSI MOS technology. In VLSI design of a chip, two principal factors are generally considered, i.e., the area of the chip and the anticipated power consumption of the chip. Consequently, we will consider the minimizations of the above two parameters in the VLSI design of CMOS current mirrors.

In this thesis, we present twelve new current mirror circuits. They are classified into eight types. First four types are available in both the sink and source versions. Four of these current mirrors have gains greater than unity while the other four have gains less than unity. The last four types realize a current mirror only in a source or sink version, both with a gain greater than unity or less than unity.

This is done by taking an approach, that simultaneously eliminates the mask misalignment effects and reduces the area of the current mirror. The design technique presented in this thesis is applied to 3 μm technology. This technique is technology independent in the sense that it can be use with any present or future size (1.2 μm , 0.8 μm etc.) VLSI technology.

A control technique using the idea of current multiplication by cascading current mirrors and sharing the input current by a control block is presented to give the advantage in saving area.

1.6.1. DESCRIPTION OF THE DIFFERENT CHAPTERS

In chapter II, analyses of twelve novel current mirror circuits that make use of the (K) factor to realize gains greater than or less than unity for the output current are given. The inherent negative feedback in the network that is used to stabilize the current gain is discussed. AC analyses for the output impedances of these circuits are given. A comparison between the output impedances of these current mirrors is given. A statistical study for these circuits is discussed to identify the percentage error that comes from the various parameters of the MOSFET as given by the equation for the operation in saturation region. A comparison of these errors with the conventional design is also given.

Chapter III describes a way of increasing the current gain. It also discusses a technique for controlling this gain electronically. The control circuit for each of the twelve DC current mirrors is analyzed.

An application of the new current mirrors in the design of an operational transconductance amplifier (OTA) is considered in Chapter IV. The same OTA is also designed using the conventional current mirrors. Performance comparisons between the two designs demonstrate the desirability of using the new current mirrors.

Appendix (A) contains FORTRAN77 and HSPICE simulation programs for the different designed circuits. HSPICE simulator is using the 3 micron process technology parameters of the Canadian Microelectronics Corporation (C.M.C.). The results are used to check the accuracy and compare with the analyses done in the thesis.

Appendix (B) consists an analysis for the circuits used with the control unit described in Chapter 3. This analysis gives a help in analyzing these selected controlled current mirrors.

CHAPTER 2

NEW CMOS CURRENT MIRRORS

2.0 INTRODUCTION

It is observed in chapter 1 that an efficient solution for the misalignment problem in current mirrors may be obtained through the use of equal size MOSFETs. This chapter develops techniques to implement the above philosophy and suggests methods of achieving a stable DC current gain greater than or less than unity. The equal size technique uses MOSFETs in both reference and output sides of a current mirror (Fig. 2.1) with equal dimensions i.e.:

$$W_R = W_O$$

$$L_R = L_O$$

where W is the channel width and L is the channel length, R and O refer to the reference and output MOSFETs, respectively. The basic current mirror shown in Fig.2.1 has a current ratio equation as follows:

$$\frac{i_O}{i_R} = \frac{K_O}{K_R} \cdot \frac{(v_{GS_O} - v_{T_O})^2}{(v_{GS_R} - v_{T_R})^2} \cdot \frac{(1 + \lambda_O v_{DS_O})}{(1 + \lambda_R v_{DS_R})} \quad (2.1)$$

The voltages v_{GS_O} and v_{GS_R} are equal. Since λ_O and λ_R are small factors (0.01 to 0.03)[5], the ratio $(1 + \lambda_O v_{DS_O}) / (1 + \lambda_R v_{DS_R})$ will stay close to unity for $v_{DS_O} \ll \lambda_O^{-1}$ and $v_{DS_R} \ll \lambda_R^{-1}$.

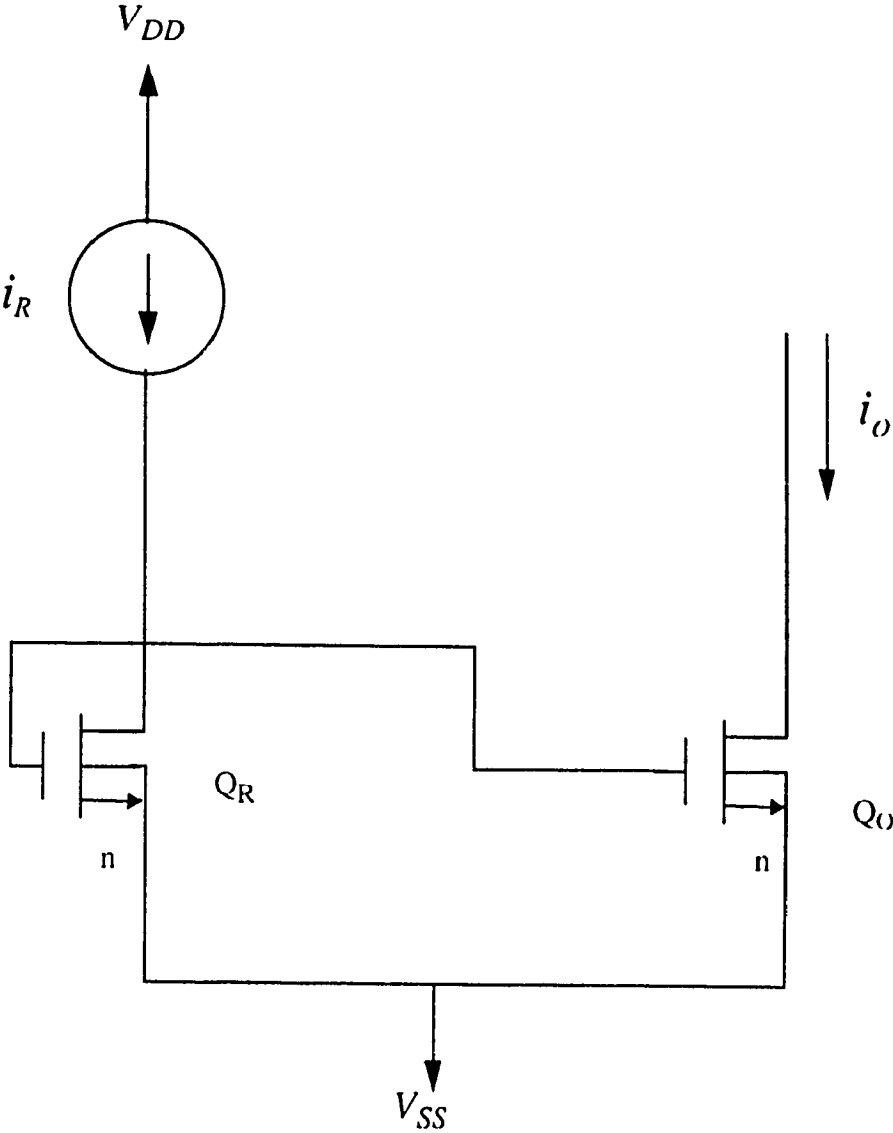


Fig.2.1
Simple current mirror

By examining eqn. (2.1), it is observed that a current gain can be achieved by utilizing the K factor, K_O / K_R . This is possible because one may use K_n (NMOS transconductance parameter) for K_O and K_p (PMOS transconductance parameter) for K_R or vice versa. K_n and K_p are fabrication process parameters. The values of K_n and K_p are $40 \times 10^{-6} \frac{A}{V^2}$ and $2 \times 10^{-6} \frac{A}{V^2}$, respectively [5]. This implies that it is possible to get a current gain without increasing the size (width) of the output transistor Q_O . By making both Q_R and Q_O transistors of equal sizes, an approximate current ratio equation can be written as follows:

1. For current ratio greater than unity, the equation is:

$$\frac{i_O}{i_R} \cong \frac{K_n}{K_p} \cdot \frac{(v_{GSO} - V_{Tn})^2}{(v_{SGR} - V_{Tp})^2} \quad (2.2)$$

2. For current ratio less than unity, the equation is:

$$\frac{i_O}{i_R} \cong \frac{K_p}{K_n} \cdot \frac{(v_{SGO} - V_{Tp})^2}{(v_{GSR} - V_{Tn})^2} \quad (2.3)$$

Fig. 2.2a and Fig. 2.2b shows the block diagrams which indicate the above two current mirror operations in both current sink and current source versions, respectively.

In this chapter, new current mirrors are designed utilizing the K -factor to obtain a current gain, to minimize the area and to eliminate the effect of misalignment on the output current. These current mirrors will be called "New CMOS (NCMOS) current mirrors". These can be used in any analog circuit such as a difference amplifier or an inverting amplifier etc.

There are two main types of NCMOS current mirrors, the first one sinks the output current while the second one sources the output current. Each type has two categories, one gives a DC current gain greater than unity, and the other gives a DC current gain less than

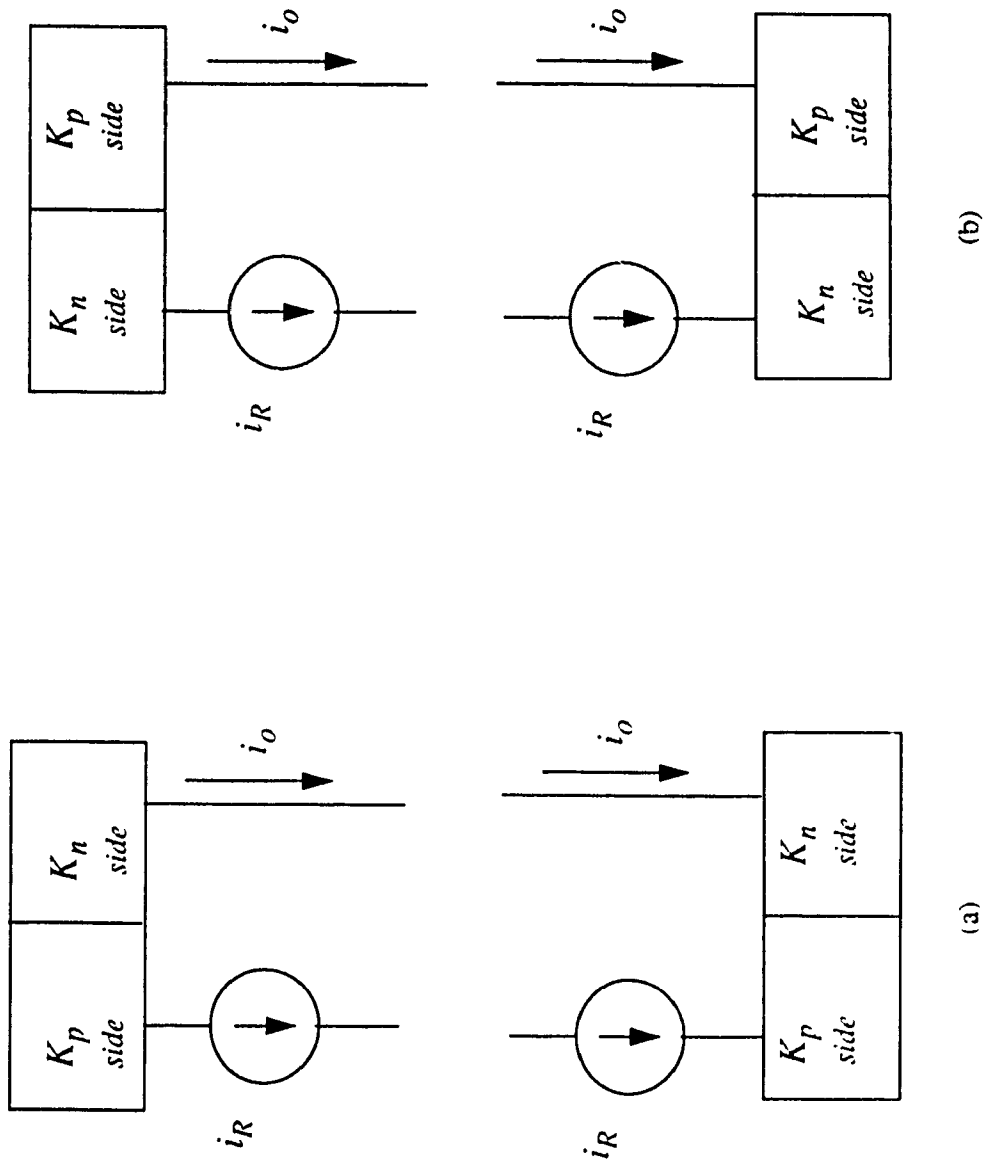


Fig.2.2
Block diagrams for current mirrors which satisfies eqn. (2.2) and eqn. (2.3)

unity. The stabilization of the output current in each case is achieved by increasing the output impedance by using negative feedback.

Twelve different NCMOS current mirror circuits are proposed which can be designed with equal size MOSFETs as suggested in this thesis. These NCMOS current mirrors are as follows:

- (a) Type Ia (sink with $K > 1$, Fig2.3) and Type Ib (source with $K < 1$, Fig.2.4).
- (b) Type IIa (sink with $K < 1$, Fig2.5) and Type IIb (source with $K > 1$, Fig.2.6).
- (c) Type IIIa (sink with $K < 1$, Fig2.7) and Type IIIb (source with $K > 1$, Fig.2.8).
- (d) Type IVa (sink with $K > 1$, Fig2.9) and Type IVb (source with $K < 1$, Fig.2.10).
- (e) Type V (sink with $K > 1$, Fig2.11).
- (f) Type VI (sink with $K < 1$, Fig2.12).
- (g) Type VII (source with $K > 1$, Fig2.13).
- (h) Type VIII (source with $K < 1$, Fig2.14).

Each of the first four NCMOS current mirrors is available in both sink and source versions, while the last four types are available only either in a sink or a source version. The DC analysis has been carried out for all these circuits. However, to conserve space, detailed analyses of only four circuits are presented in the next four sections. These circuits were selected because of their superior performances relative to the rest of the circuits. They are as follows:

- 1- Type IIa (sink with $K < 1$, Fig2.5).
- 2-Type IVb (source with $K < 1$, Fig.2.10).
- 3- Type V (sink with $K > 1$, Fig2.11).
- 4- Type IIIb (source with $K > 1$, Fig.2.8).

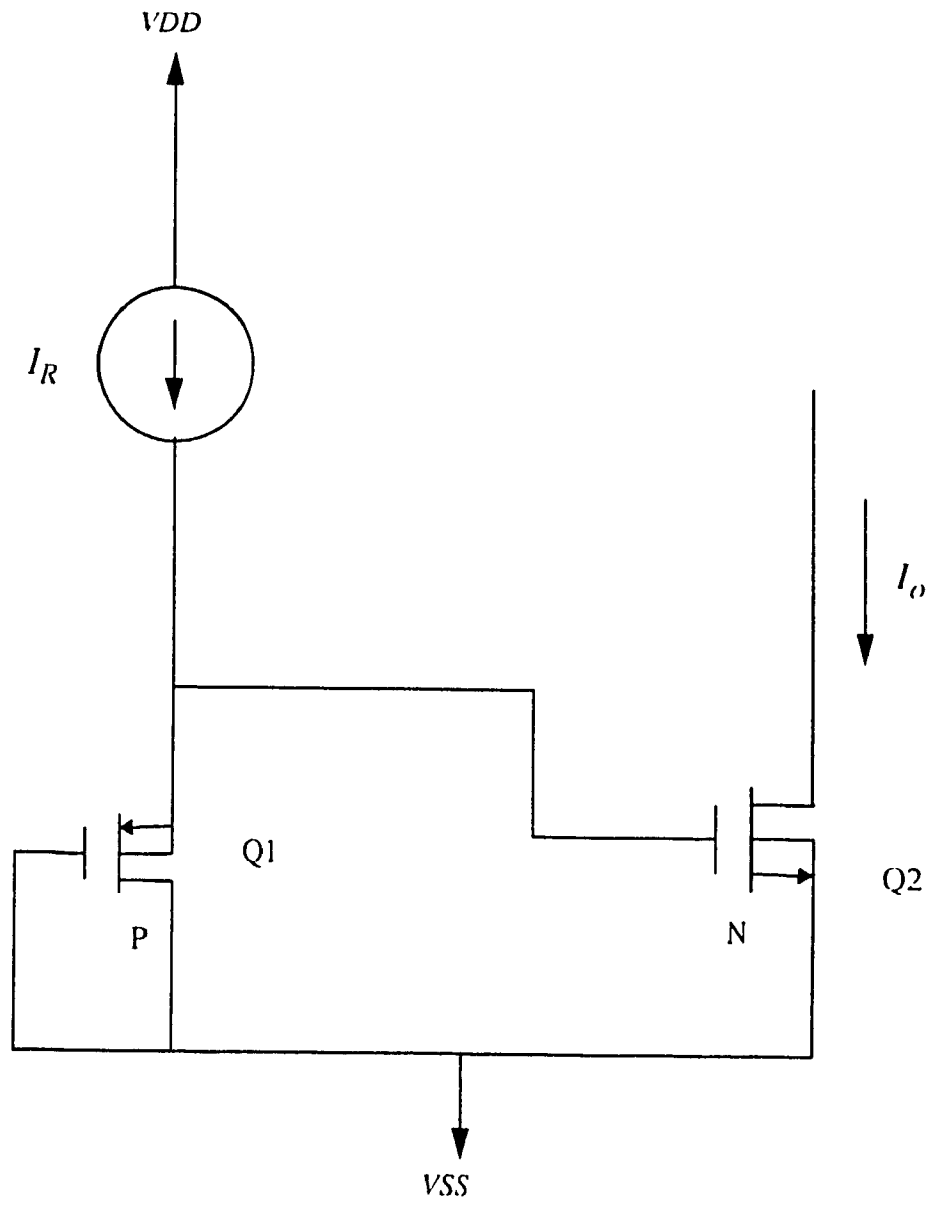


Fig.2.3
Circuit diagram for Type Ia NCMOS current mirror, (sink version) with $K > 1$

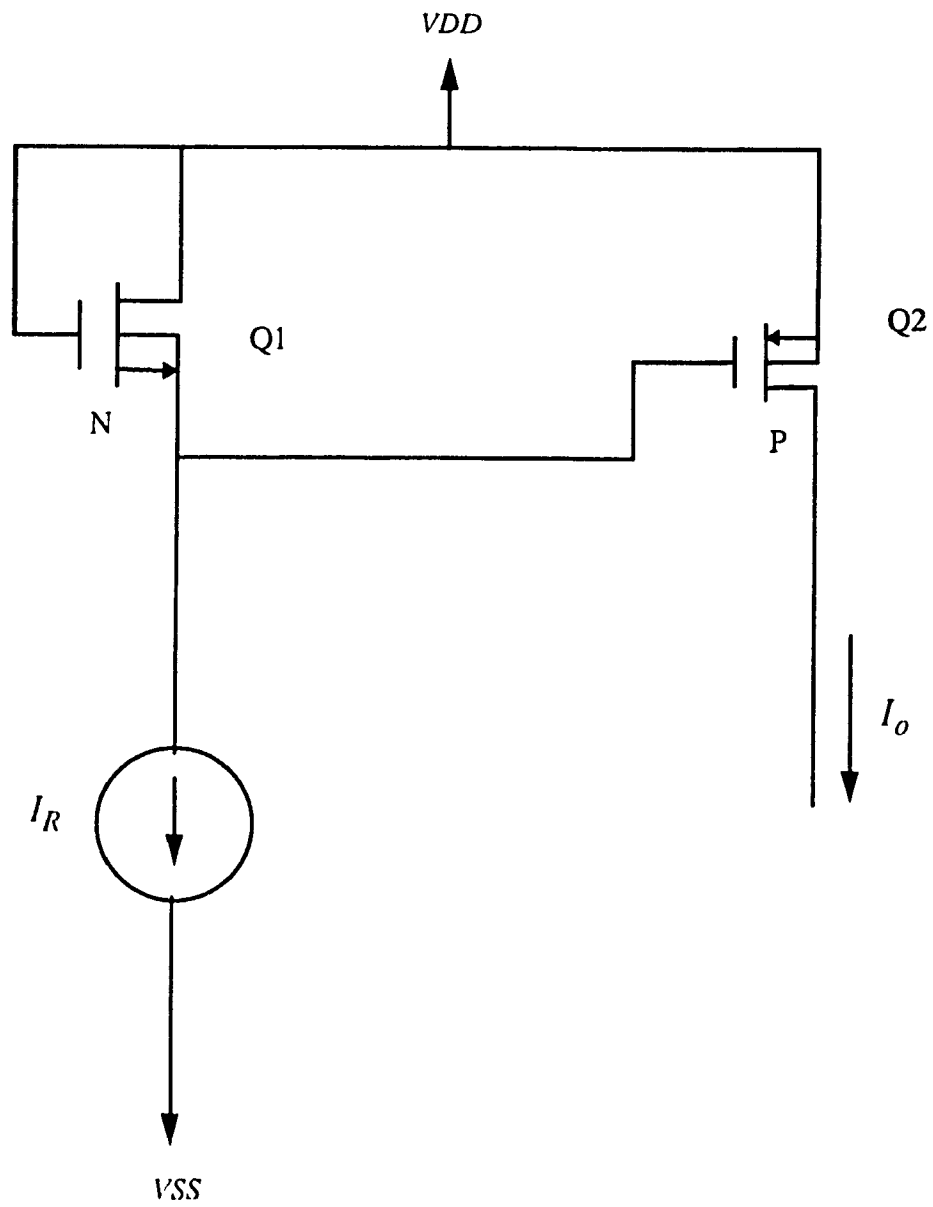


Fig. 2.4

Circuit diagram for Type Ib NCMOS current mirror, (source version) with $K < 1$

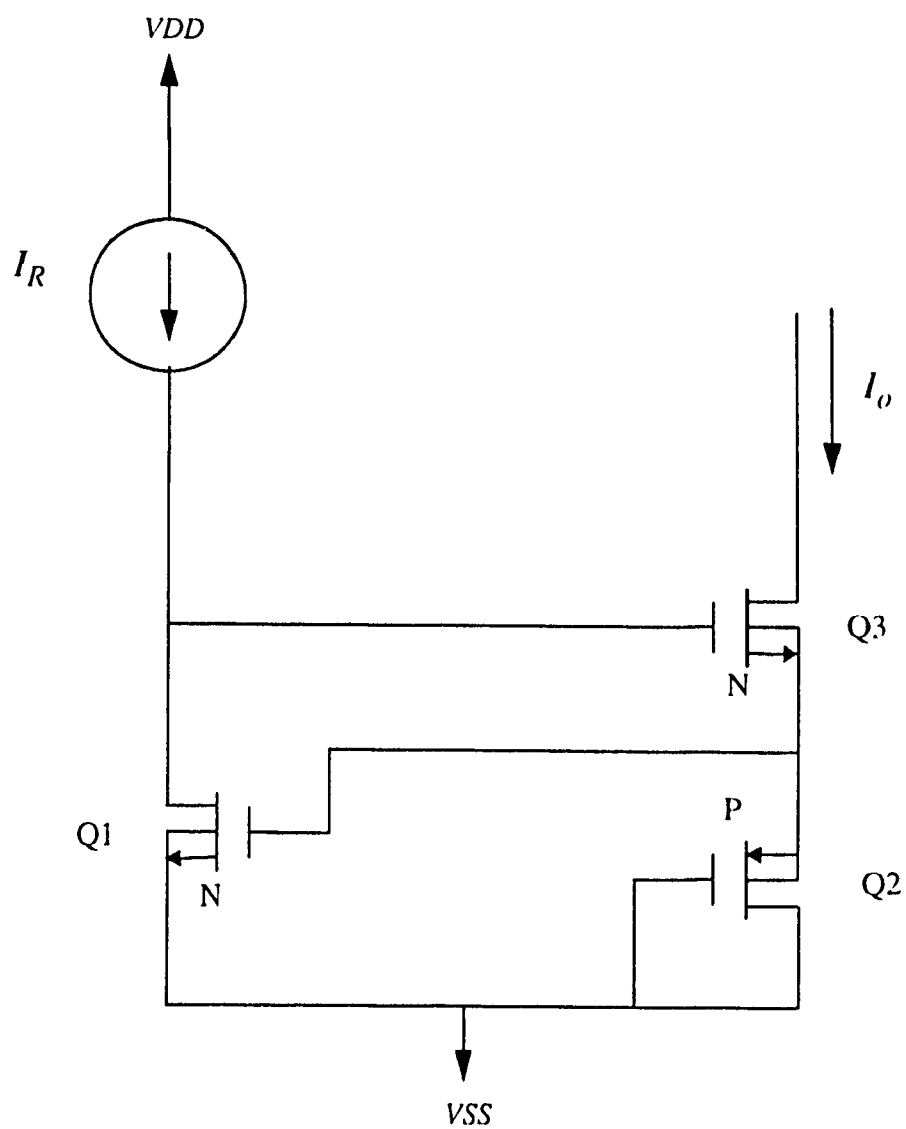


Fig. 2.5
Circuit diagram for Type IIa NCMOS current mirror, (sink version) with $K < 1$

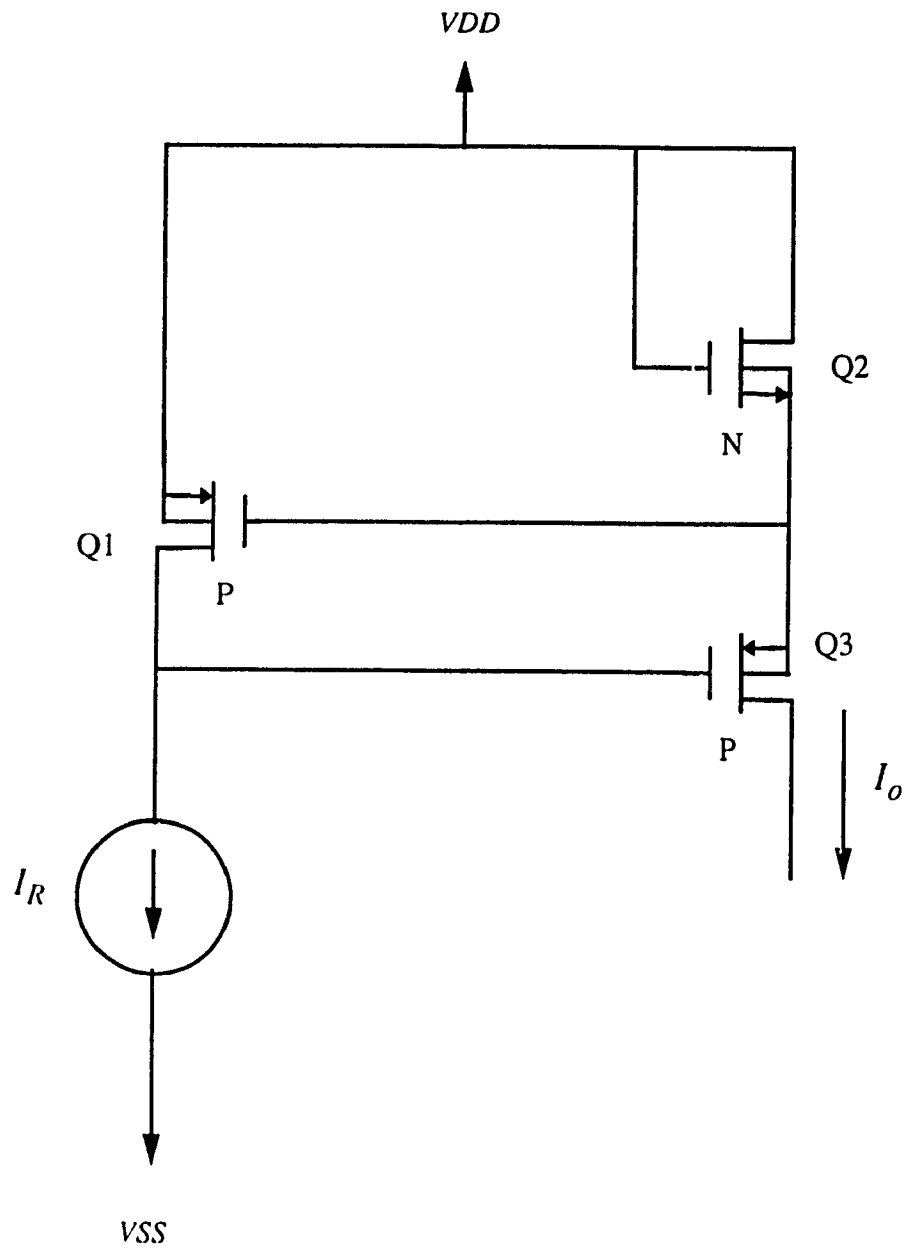


Fig. 2.6
Circuit diagram for Type IIb NCMOS current mirror, (source version) with $K > 1$

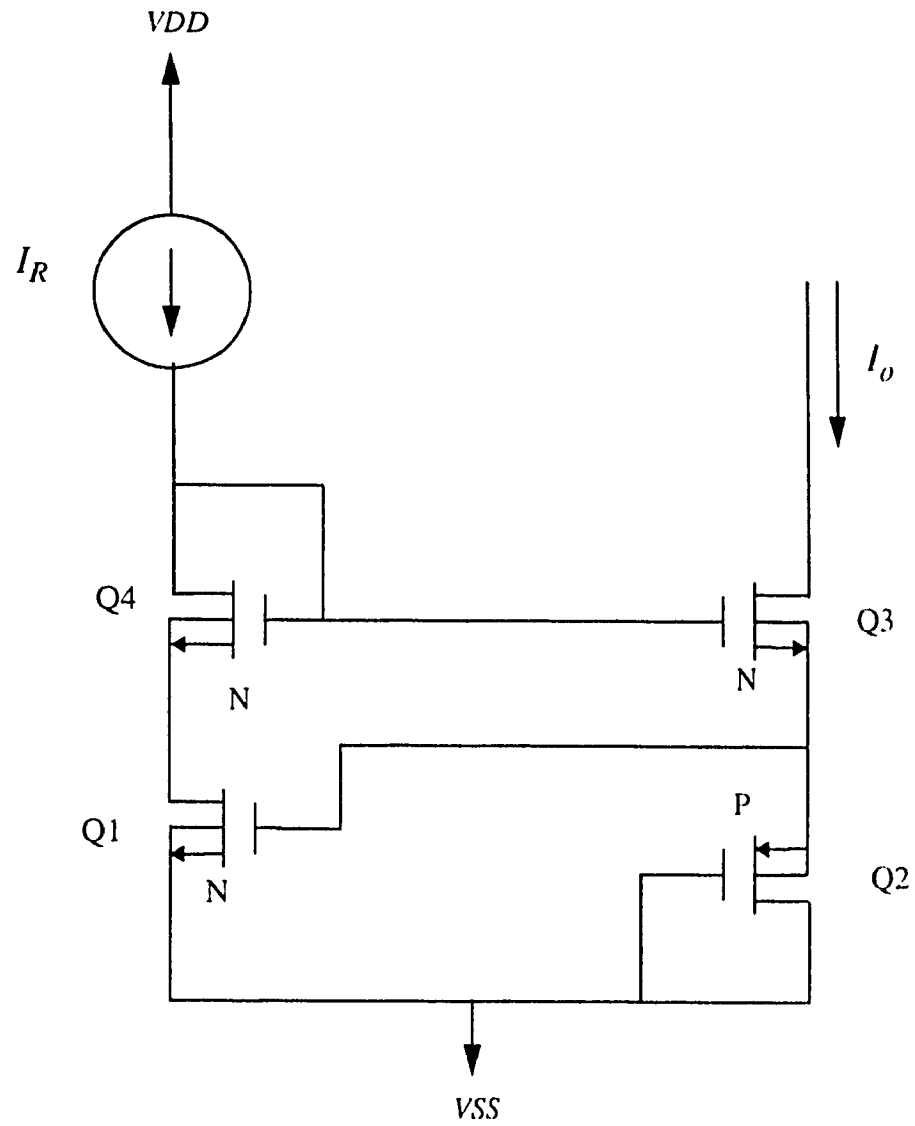


Fig. 2.7

Circuit diagram for Type IIIa NCMOS current mirror, (sink version) with $K < 1$

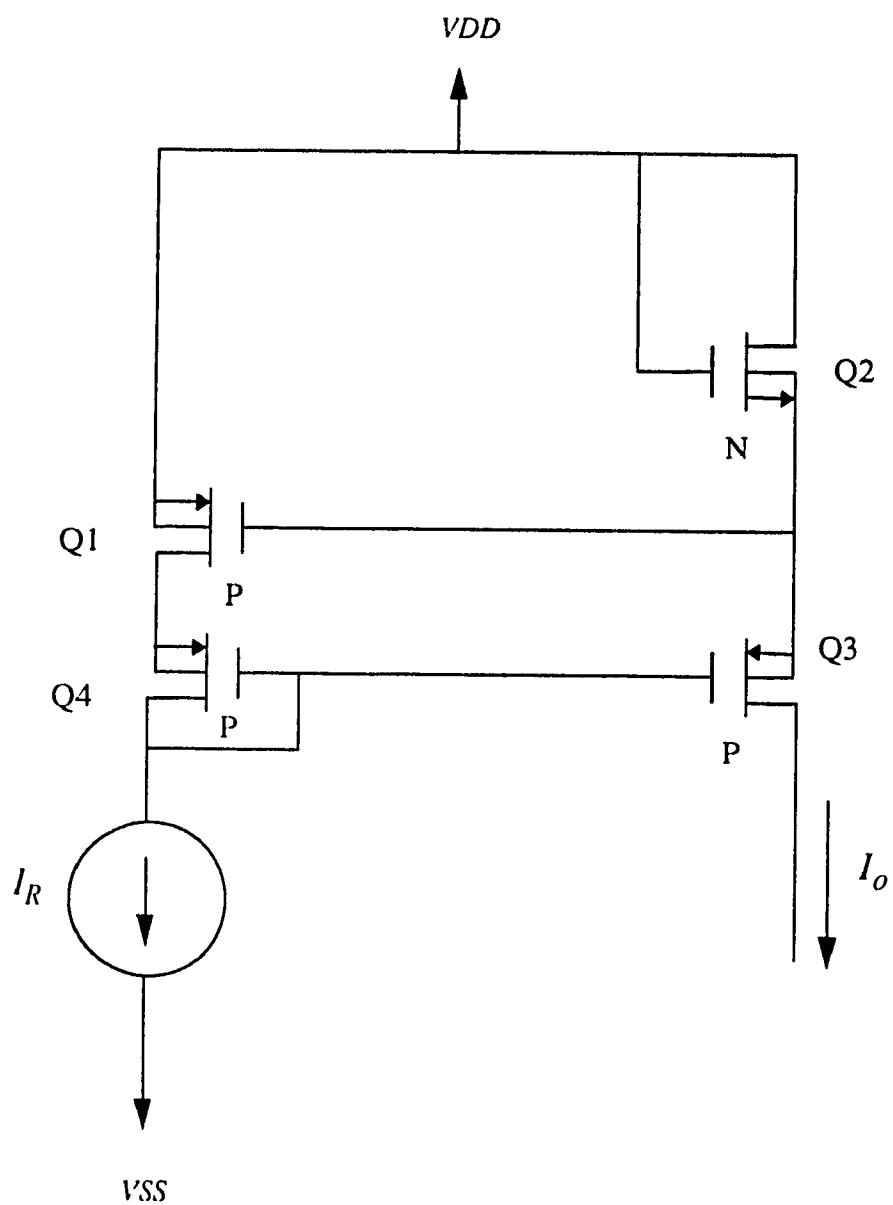


Fig. 2.8
Circuit diagram for Type IIIb NCMOS current mirror, (source version) with $K > 1$

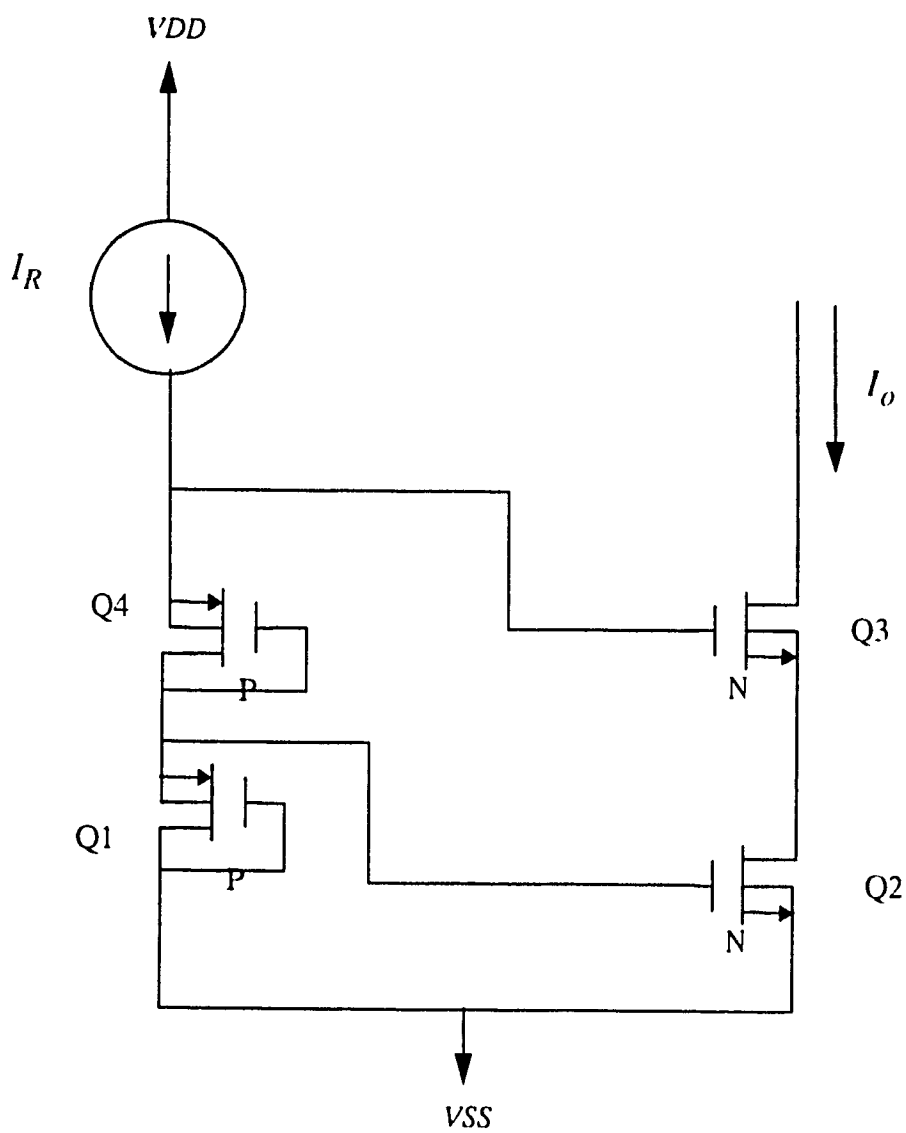


Fig. 2.9

Circuit diagram for Type IVa NCMOS current mirror, (sink version) with $K > 1$

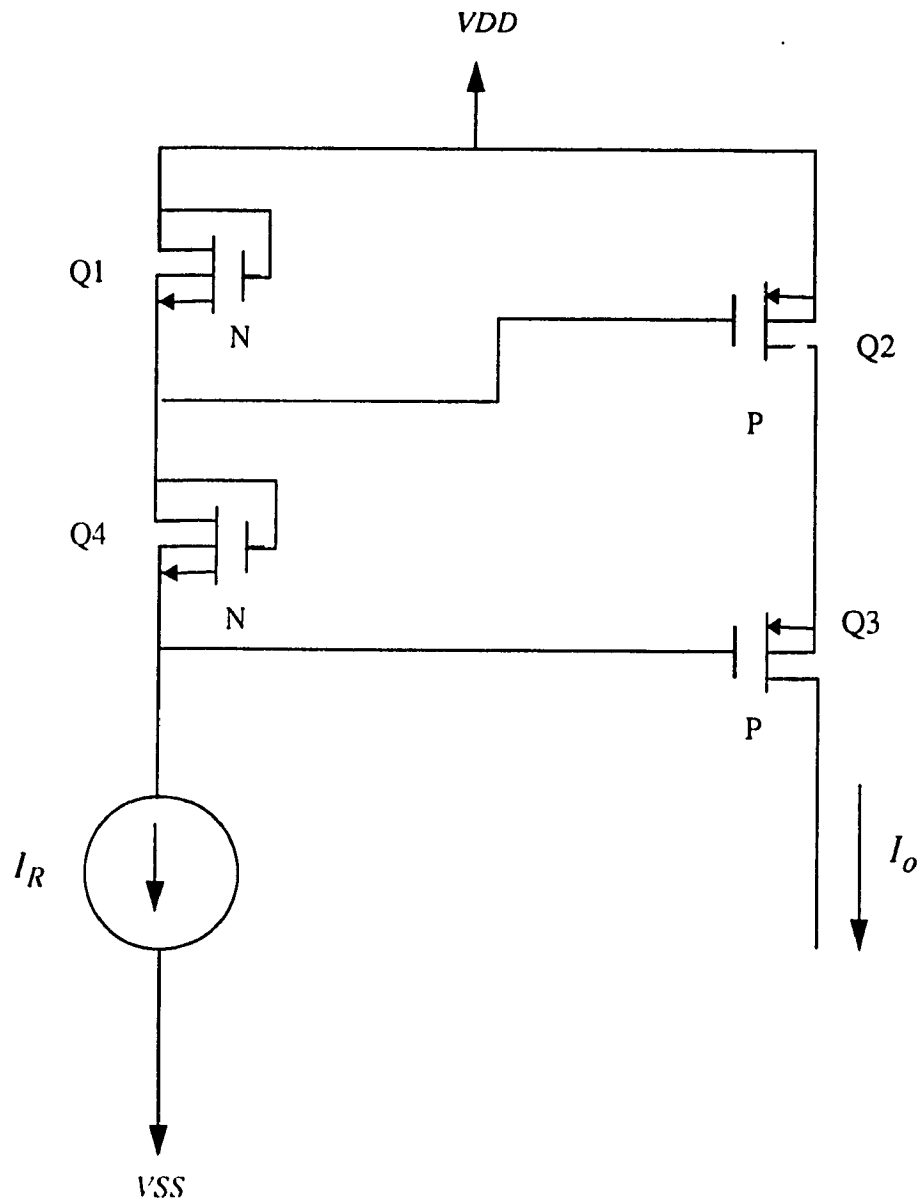


Fig. 2.10
Circuit diagram for Type IVb NCMOS current mirror, (source version) with $K < 1$

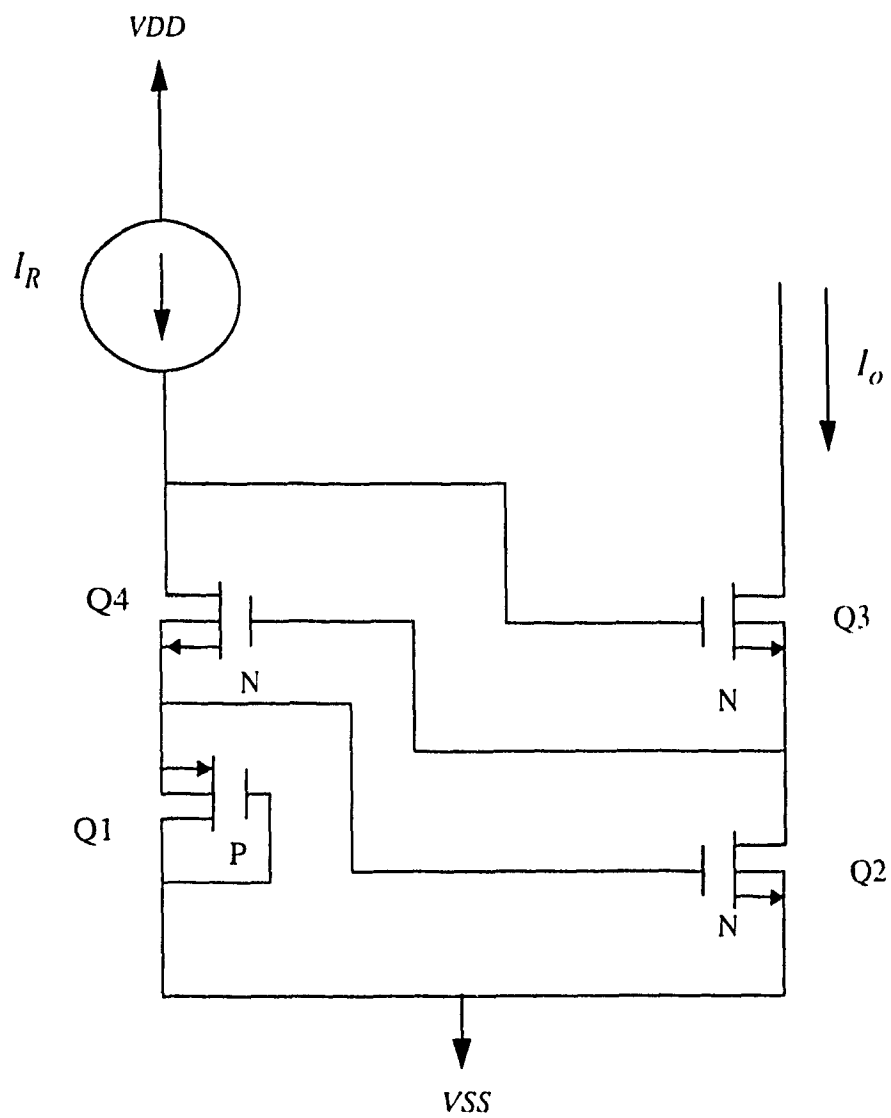


Fig. 2.11

Circuit diagram for Type V NCMOS current mirror, (sink version) with $K > 1$

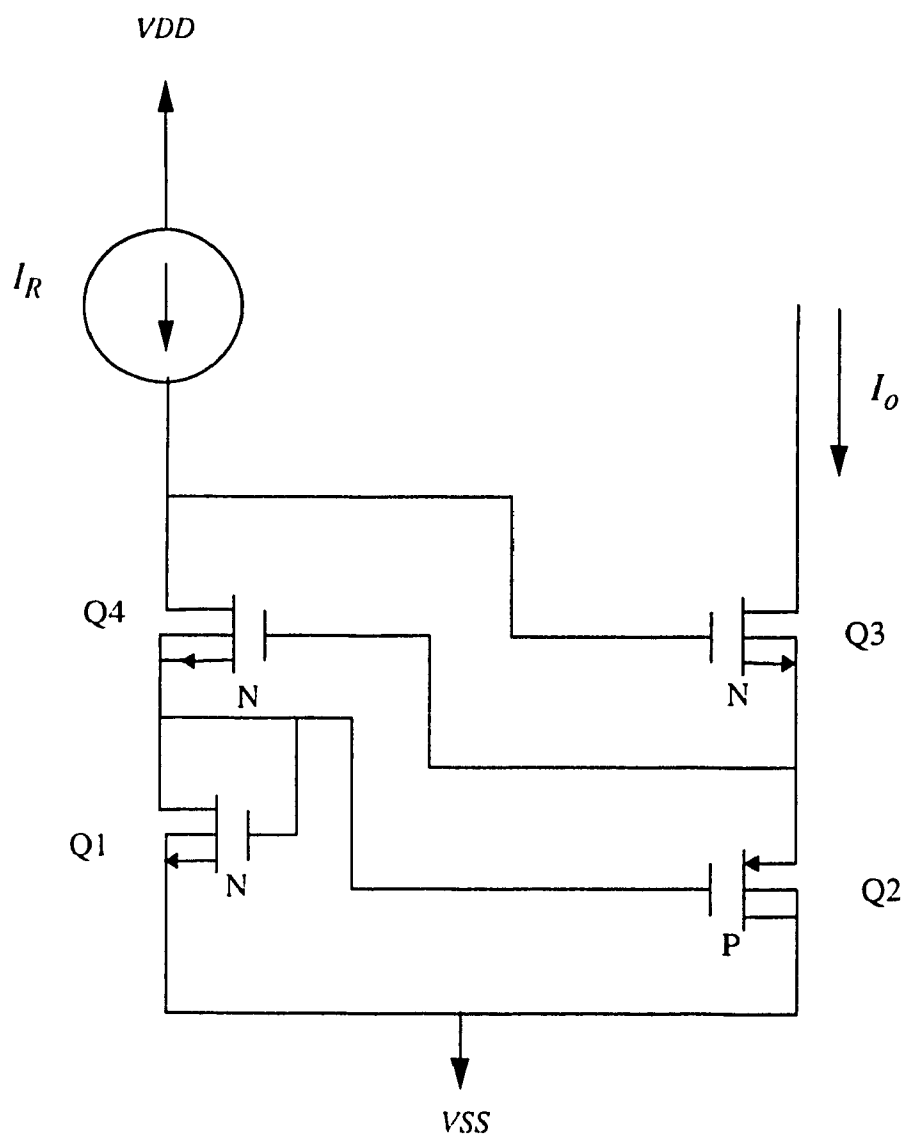


Fig. 2.12

Circuit diagram for Type VI NCMOS current mirror, (sink version) with $K < 1$

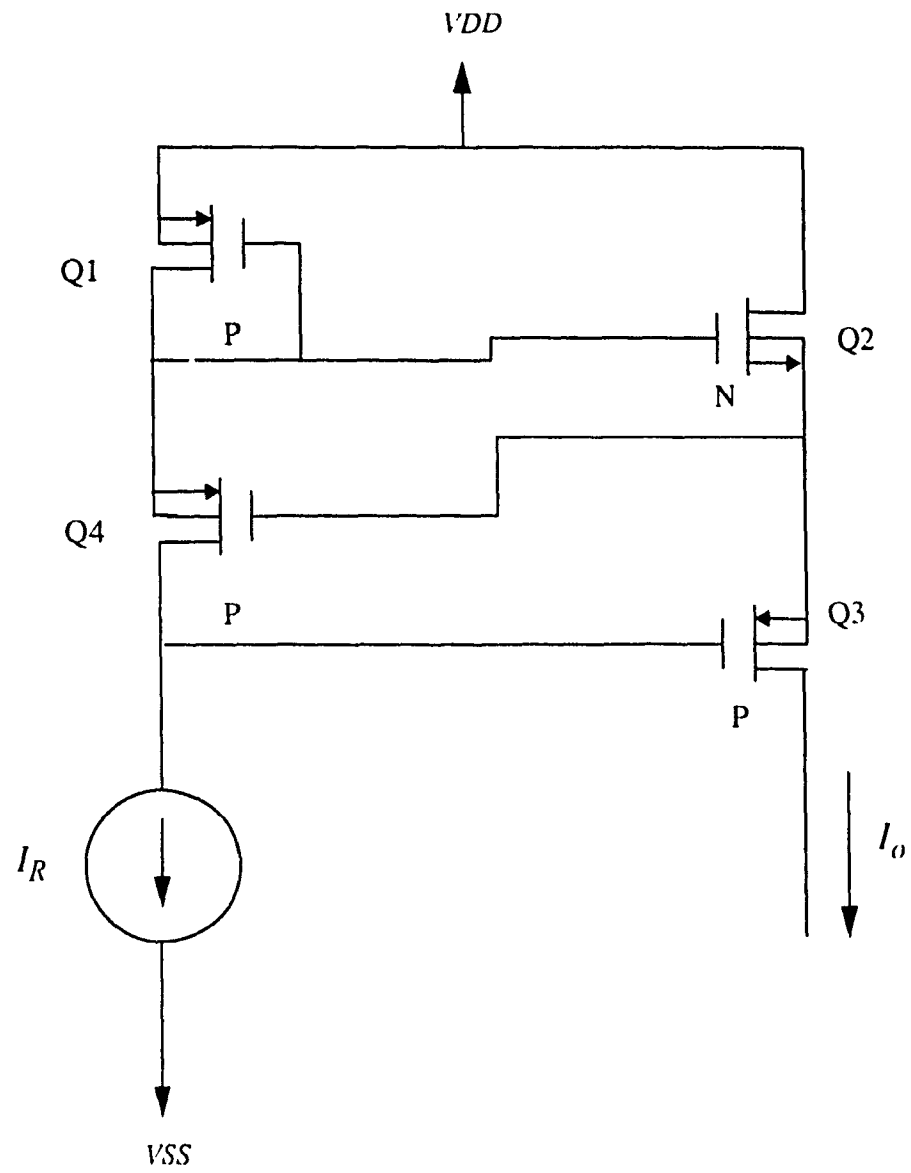


Fig. 2.13
Circuit diagram for Type VII NCMOS current mirror, (source version) with $K > 1$

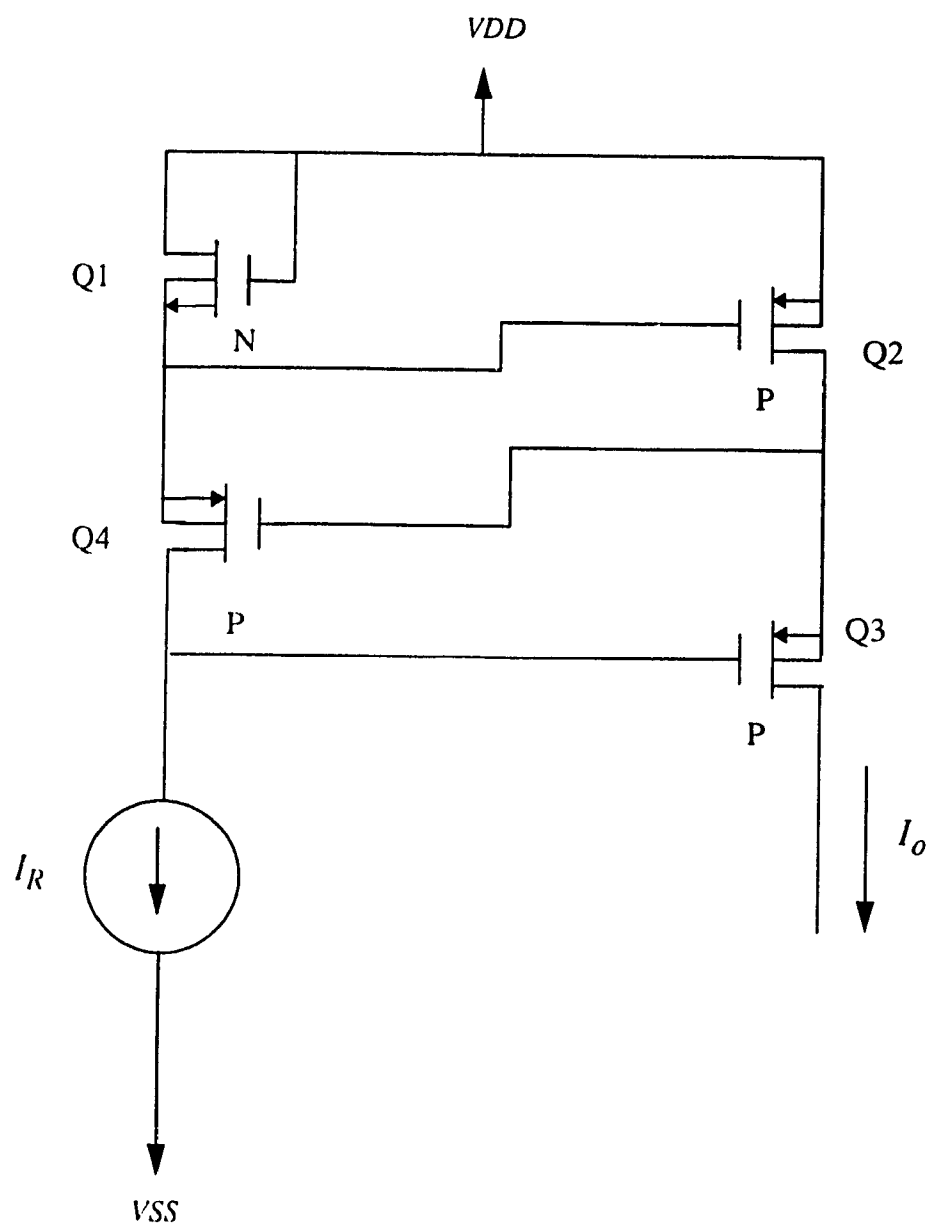


Fig. 2.14
Circuit diagram for Type VIII NCMOS current mirror, (source version) with $K < 1$

Tables and graphs showing current ratio stability of the twelve circuits are given¹. The HSPICE software has also been used to simulate these NCMOS current mirrors and a comparison between the analysis and simulation results are supplied in a graphical form.

Modifications are suggested to further improve the current ratio stability of these NCMOS current mirrors. AC analyses have been done to calculate the output impedances of the NCMOS current mirrors, and the final expressions are tabulated. A statistical study is carried out to show the maximum percentage error in the current ratio which might take place due to variation of the various process parameters. Finally, a twin-tub implementation technique for implementing these NCMOS current mirrors has been discussed towards the end of this chapter.

2.1 TYPE IIa NCMOS CURRENT MIRROR (SINK) WITH $K < 1$:

Based on simulation and analysis results, this circuit was selected as the best NCMOS current mirror in the sink version with a current gain less than unity. Fig.2.5 shows the circuit diagram. This circuit has a negative feedback which gives a more stable current gain during the load variation, because the drain-to-source voltage V_{DS1} of transistor Q_1 will be limited by the sum of the voltages V_{SG2} of transistor Q_2 and V_{GS3} of transistor Q_3 . The load is separated from the basic NCMOS current mirror structure Q_1 and Q_2 by transistor Q_3 , which keeps the current gain almost constant and independent of the load value.

Since I_R has a constant value, then it will develop a corresponding voltage V_{GS1} between the gate and source of transistor Q_1 , and this voltage will also be impressed across

1. By the term "current ratio stability" is meant the degree of the constancy of the current ratio with respect to variation in any parameter that may be of interest.

the source and gate of transistor Q_2 . The output current I_o is pulled by Q_2 depending on the values of the voltage V_{SG2} and the transconductance K_2 .

Assume transistors Q_1 , Q_2 and Q_3 are all operating in the saturation region.

For transistor Q_1 :

$$I_R = \beta_1 \cdot (V_{GS1} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS1}) \quad (2.4)$$

For transistor Q_2 :

$$I_o = \beta_2 \cdot (V_{SG2} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD2}) \quad (2.5)$$

For transistor Q_3 :

$$I_o = \beta_3 \cdot (V_{GS3} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS3}) \quad (2.6)$$

Our approach uses equal size transistors with ratio $W/L = 1$, in order to minimize the area. Hence:

$$\beta_1 = \frac{K_n}{2}, \beta_2 = \frac{K_p}{2}, \text{ and } \beta_3 = \frac{K_n}{2}.$$

Since the voltage $V_{SG2} = V_{SD2} = V_{GS1} = V_R$, and the drain to source voltage of transistor Q_1 is $V_{DS1} = V_{SG2} + V_{GS3}$.

From eqn. (2.5) and eqn. (2.6) the voltage V_{GS3} will be, assuming $\lambda_n V_{DS3} \ll 1$:

$$V_{GS3} \approx \sqrt{\frac{K_p}{K_n}} \cdot (V_{SG2} - V_{Tp}) + V_{Tn}$$

The assumption $\lambda_n V_{DS3} \ll 1$ should hold over a large range of R_L because of the negative feedback employed in the circuit. This negative feedback is easily demonstrated as follows. Let I_o increase, for a constant I_R , for any reason. Then $V_{SG2} = V_{SD2}$ increases. This leads to an increase in V_{GS1} . Since I_R is constant V_{DS1} has to decrease. Thus, V_{GS3} tends to decrease tending to bring down I_o . Consequently, increase of I_o will be less than its value in the absence of this negative feedback.

Thus the voltage V_{DS1} will be approximately constant and equal to:

$$V_{DS1} = V_{SG2} \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn} \quad (2.7)$$

From eqn. (2.4) and eqn. (2.7), the reference current can be written as:

$$I_R = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot \left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right) \quad (2.8)$$

Substituting the values of β_2 , V_{SG2} and V_{SD2} , the output current becomes:

$$I_o = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R) \quad (2.9)$$

The current ratio can be derived from dividing eqn. (2.9) by eqn. (2.8) in the following form:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_p V_R)}{\left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)} \quad (2.10)$$

It is clear in eqn. (2.10) that the current ratio I_o / I_R is approximately a function of only one variable, V_R , and is thus relatively independent of the value of the load R_L and the output voltage V_o , as long as Q_1 , Q_2 and Q_3 operate in the saturation region.

2.2 TYPE IVb NCMOS CURRENT MIRROR (SOURCE) WITH $K < 1$:

This circuit was selected, according to simulation and analysis results, because of its superior current ratio stability compared to the other NCMOS current mirrors in source versions with a current gain less than unity. This is attributed to the fact that the four MOSFET transistors shown in Fig.2.10 utilize again a negative feedback loop. Further, each current branch has the same type of MOSFET transistors which leads to a simpler current ratio form.

The other advantage of this circuit is its higher output impedance because none of the two output transistors are connected as a two terminal MOSFET. This will keep them away

from the boundary region (between the triode and saturation regions), as will be shown later in the AC analysis of the output impedance.

Assuming all the transistors are saturated,

For transistor Q_1 :

$$I_R = \beta_1 \cdot (V_{GS1} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS1}), \quad V_{DS1} = V_{GS1} \quad (2.11)$$

For transistor Q_4 :

$$I_R = \beta_4 \cdot (V_{GS4} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS4}), \quad V_{DS4} = V_{GS4} \quad (2.12)$$

For transistor Q_2 :

$$I_o = \beta_2 \cdot (V_{SG2} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD2}) \quad (2.13)$$

For transistor Q_3 :

$$I_o = \beta_3 \cdot (V_{SG3} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD3}) \quad (2.14)$$

Since the ratio W/L for the four transistors is equal to unity:

$$\beta_1 = \frac{K_n}{2}, \beta_2 = \frac{K_p}{2}, \beta_3 = \frac{K_p}{2}, \text{ and } \beta_4 = \frac{K_n}{2}.$$

From eqn. (2.11) and eqn. (2.12), we have:

$V_{GS1} = V_{GS4} = V_{DS1} = V_R$, where V_R is the reference voltage. Now eqn. (2.11) can be written as:

$$I_R = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (2.15)$$

From the circuit diagram of Fig.2.10, it is clear that the voltage V_{SD2} will be:

$$V_{SD2} = 2V_R - V_{SG3} \quad (2.16)$$

Combining both eqn. (2.13) and eqn. (2.14) we will get, assuming $\lambda_p V_{SD2} \ll 1$ and $\lambda_p V_{SD3} \ll 1$.

$$V_{SG2} \approx V_{SG3} \quad (2.17)$$

The assumption $\lambda_p V_{SD2} \ll 1$ and $\lambda_p V_{SD3} \ll 1$ are reasonable in view of the negative feedback loop among Q_1 through Q_4 . The negative feedback action arises in this case as follows. As long as I_R is held constant, $V_{GS1} = V_{SG2} = V_R$ remains constant. If for any reason I_o tends to increase, V_{SD2} has to increase. Since $V_{SD2} + V_{SG3} = 2V_R$, this makes V_{SG3} tends to decrease. Consequently, increase of I_o will be less than its value in the absence of this negative feedback.

The last two equations (2.16) and (2.17) along with $V_{GS1} = V_{SG2} = V_R$, will imply:

$$V_{SD2} = V_R \quad (2.18)$$

Equation (2.2.8) shows that the drain-to-source voltage of transistor Q_2 is held constant. This will keep the output current constant with different load values since the reference current is fixed. The output current can therefore, be written in terms of the reference voltage as follows:

$$I_o = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R) \quad (2.19)$$

Dividing eqn. (2.19) by eqn. (2.15), will give the following current ratio

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_p V_R)}{(1 + \lambda_n V_R)} \quad (2.20)$$

The current ratio in eqn. (2.20) is a function of only one variable which is V_R . Thus if the voltage V_R stays constant then the current ratio will also stay constant. This condition is, however, only true when all transistors are in the saturation region.

2.3 TYPE V NCMOS CURRENT MIRROR (SINK) WITH $K > 1$:

Fig.2.11 shows the best NCMOS current mirror in a sink version with a current gain greater than unity. This circuit is the best in its group because of its high current ratio stability. The voltage V_{DS2} of the output transistor Q_2 is stabilized by adding transistor Q_4 .

A separation between the output voltage and the voltage V_{DS2} is provided through transistor Q_3 , which will also give a negative feedback to the reference side transistor Q_4 , to keep the I_o stable whenever there is a variation in the output voltage due to load variation.

Let all transistors be in the saturation region, Q_1 and Q_4 carry the same reference current, while Q_2 and Q_3 carry the same output current.

For transistor Q_1 :

$$I_R = \beta_1 \cdot (V_{SG1} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD1}) \quad (2.21)$$

For transistor Q_4 :

$$I_R = \beta_4 \cdot (V_{GS4} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS4}) \quad (2.22)$$

For transistor Q_2 :

$$I_o = \beta_2 \cdot (V_{GS2} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS2}) \quad (2.23)$$

For transistor Q_3 :

$$I_o = \beta_3 \cdot (V_{GS3} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS3}) \quad (2.24)$$

Since all the MOSFETs used are the same size, then the values of β will be as follows:

$$\beta_1 = \frac{K_p}{2}, \beta_2 = \frac{K_n}{2}, \beta_3 = \frac{K_n}{2} \text{ and } \beta_4 = \frac{K_n}{2}.$$

Because I_o is common for Q_2 and Q_3 then:

$$V_{GS3} = V_{GS2} = V_{SG1}, \text{ assuming } \lambda_n V_{DS2} \ll 1 \text{ and } \lambda_n V_{DS3} \ll 1.$$

This is reasonable since there is a negative feedback action which keeps I_o constant as long as I_R constant. It works as follows. As long as I_R is held constant, $V_{GS2} = V_{SG1}$ is held constant. Thus, if for any reason, I_o tends to increase, the voltage V_{DS2} has to decrease. Thus, $V_{GS3} = V_{DS4} + V_{SG1} - V_{DS2}$ decreases tending to keep I_o constant.

This will give: $V_{DS4} = V_{GS4} + V_{SG1}$

Let $V_{GS1} = V_R$. Combining eqn. (2.21) with eqn. (2.22) will results:

$$K_p \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R) = K_n \cdot (V_{GS4} - V_{Tn})^2 \cdot (1 + \lambda_n (V_R + V_{GS4})) \quad (2.25)$$

Since V_{GS4} and V_R are both limited and constant in values, it is possible to approximate eqn. (2.25) to:

$$K_p \cdot (V_R - V_{Tp})^2 = K_n \cdot (V_{GS4} - V_{Tn})^2$$

The value of V_{GS4} can thus be written as:

$$V_{GS4} \approx \sqrt{\frac{K_p}{K_n}} \cdot (V_R - V_{Tp}) + V_{Tn} \quad (2.26)$$

Because the voltage $V_{DS2} = V_R + V_{GS4}$, we have,

$$V_{DS2} = V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - \left(V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}}\right) + V_{Tn} \quad (2.27)$$

Solving eqn. (2.27) and eqn. (2.23) will give for the output current I_o :

$$I_o = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot \left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right) \quad (2.28)$$

The reference current can be written in terms of the reference voltage V_R as follows:

$$I_R = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R) \quad (2.29)$$

Dividing eqn. (2.28) by eqn. (2.29) will give a current ratio as shown below:

$$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{\left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)}{(1 + \lambda_p V_R)} \quad (2.30)$$

It is clear from eqn. (2.30) that the current ratio is a function of only one voltage V_R . Thus when the reference voltage V_R stays constant the current ratio will stay constant, independent of the load, as long as all the transistors stay in the saturation region.

2.4 TYPE IIIb NCMOS CURRENT MIRROR (SOURCE) WITH $K > 1$:

This NCMOS current mirror was selected as the best source version with a gain greater than unity based on the analysis and simulation results. It consist of four MOSFETs connected as shown in Fig.2.8. To stabilize the gain, the PMOS transistor Q_4 was added in series with the reference side transistor Q_1 , to reduce the value of V_{SD1} and bring it closer to the voltage V_{SG1} .

Since Q_2 is an NMOS transistor and Q_3 is a PMOS transistors and they have the same drain current, then the voltage V_{SG3} will have a value greater than voltage V_{GS2} , so that transistor Q_3 will be able to hold the output current I_o through its channel. This means that the value of the voltage V_{SD1} will be around $\sqrt{\frac{K_n}{K_p}} \cdot V_{SG1}$, and the ratio I_o / I_R will be held steady for the designed range of R_L that keeps Q_3 transistor in the saturation region.

Assuming all transistors saturated, the drain currents of the four MOSFETs shown in Fig.2.8. will be as follows:

For transistor Q_1 :

$$I_R = \beta_1 \cdot (V_{SG1} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD1}) \quad (2.31)$$

For transistor Q_4 :

$$I_R = \beta_4 \cdot (V_{SG4} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD4}) \quad (2.32)$$

For transistor Q_2 :

$$I_o = \beta_2 \cdot (V_{GS2} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS2}) \quad (2.33)$$

For transistor Q_3 :

$$I_o = \beta_3 \cdot (V_{SG3} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD3}) \quad (2.34)$$

The ratio W/L for these MOSFETs transistors is equal to unity, then the β factor will be equal to one half the transconductance factor (K) i.e.:

$$\beta_1 = \frac{K_p}{2}, \beta_2 = \frac{K_n}{2}, \beta_3 = \frac{K_p}{2} \text{ and } \beta_4 = \frac{K_p}{2}$$

Since the voltage $V_{GS2} = V_{DS2} = V_{SG1} = V_R$, we have:

$$V_{SD1} = V_{SG1} + V_{SG3} - V_{SG4} \quad (2.35)$$

This means that the voltage V_{SD1} is limited to a value which is less than the sum of the gate-source voltages of the other two transistors in the output side. Since the value of the output current is higher than the value of the reference current, this means that the voltage V_{SG4} is less than the voltage V_{SG3} . Hence, the value of the voltage V_{SD1} will not be less than the value of the voltage V_{SG1} . Because the transistors Q_1 and Q_4 have the same channel current then, the voltage $V_{SG1} \cong V_{SG4}$. Thus, $V_{SD1} \cong V_{SG3}$. Hence $V_{GD1} > 0$ and the transistor Q_1 will always stay in the saturation region. From eqn. (2.33) and eqn. (2.34), the source to drain voltage of transistor Q_1 can be written as follows:

$$V_{SD1} \cong (V_{GS2} - V_{Tn}) \cdot \sqrt{\frac{K_n}{K_p}} + V_{Tp} \quad (2.36)$$

This assumes $\lambda_n V_{DS2} \ll 1$ and $\lambda_p V_{SD3} \ll 1$ which is justified by the stability action of the negative feedback on I_o with respect to load variations. The negative feedback action in this case occurs as follows. If, for any reason, I_o increases, $V_{GS2} = V_{SG1}$ increases. Since V_{SG4} remains constant as long as I_R is kept constant, V_{SD1} has to decrease. This of course leads to a decrease of V_{SG3} . Hence increase of I_o will be less than its value in the absence of this negative feedback.

Letting now $V_{GS2} = V_R$ and solving eqn. (2.31) and eqn. (2.36) will give the reference current as a function of the single variable V_R as follows:

$$I_R = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot \left(1 + \lambda_p \left((V_R - V_{Tn}) \cdot \sqrt{\frac{K_n}{K_p}} + V_{Tp} \right) \right) \quad (2.37)$$

The output current in eqn. (2.33) can be written in terms of K_n and V_R by substituting the values of β_2 , V_{GS2} and V_{DS2} as shown below:

$$I_o = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (2.38)$$

Table 2.1: Current ratio for the different NCMOS current mirrors

NCMOS C.M. type	Current Ratio Equations
Type Ia K > 1 Sink	$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{(1 + \lambda_n V_{ds2})}{(1 + \lambda_p V_R)}$
Type Ib K < 1 Source	$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_p V_{ds2})}{(1 + \lambda_n V_R)}$
Type IIa K < 1 Sink	$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_p V_R)}{\left(1 + \lambda_n \left(V_R \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)}$
Type IIb K > 1 Source	$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_n V_R)}{\left(1 + \lambda_p \left(V_R \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{Tn} \sqrt{\frac{K_n}{K_p}} + V_{Tp}\right)\right)}$
Type IIIa K < 1 Sink	$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_p V_R)}{\left(1 + \lambda_n \left((V_R - V_{Tp}) \times \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)}$
Type IIIb K > 1 Source	$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{(1 + \lambda_n V_R)}{\left(1 + \lambda_p \left((V_R - V_{Tn}) \sqrt{\frac{K_n}{K_p}} + V_{Tp}\right)\right)}$

NCMOS C.M. type	Current Ratio Equations
Type IVa K > 1 Sink	$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{(1 + \lambda_n V_R)}{(1 + \lambda_p V_R)}$
Type IVb K < 1 Source	$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_p V_R)}{(1 + \lambda_n V_R)}$
Type V K > 1 Sink	$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{\left(1 + \lambda_n \left(V_R \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)}{(1 + \lambda_p V_R)}$
Type VI K < 1 Sink	$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + 2\lambda_p V_R)}{\left(1 + \lambda_n \left(V_R \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)}$
Type VII K > 1 Source	$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{(1 + 2\lambda_n V_R)}{\left(1 + \lambda_p \left(V_R \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{Tn} \sqrt{\frac{K_n}{K_p}} + V_{Tp}\right)\right)}$
Type VIII K < 1 Sink	$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{\left(1 + \lambda_p \left(V_R \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{Tn} \sqrt{\frac{K_n}{K_p}} + V_{Tp}\right)\right)}{(1 + \lambda_n V_R)}$

Dividing eqn.(2.38) by eqn.(2.37), gives the current ratio as follows:

$$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{(1 + \lambda_n V_R)}{\left(1 + \lambda_p \left((V_R - V_{Tn}) \cdot \sqrt{\frac{K_n}{K_p}} + V_{Tp} \right)\right)} \quad (2.39)$$

The expressions for the current ratios of all the NCMOS current mirrors are summarized in Table 2.1, when we consider a constant value for the current I_R .

The characteristics curves (current gain versus reference current) of the twelve NCMOS current mirrors listed in Table 2.1, as obtained from analysis, are shown in Fig.2.15 and Fig.2.16. The HSPICE simulation, using the CMOS3 DLM model, shows similar characteristics curves in Fig.2.17 and Fig.2.18. These curves indicate that the DC current gain has a functional dependence on the reference current, even though it is a function of a single variable V_R . They are nonlinear at low level reference current because of the low value of voltage V_R and the affect of λ factor. This non-linearity will cause instability in output current. To get the output current be more stable and linear the following improvement suggested to be done.

2.5 PERFORMANCE IMPROVEMENT POSSIBILITIES

If the NCMOS current mirror needs to be more stable, it is necessary to eliminate the square term from the numerator and the denominator of each current ratio equation. This can be obtained by ensuring that the threshold voltages of both PMOS and NMOS transistors are equal. This can achieved through special manufacturing processes. Two common techniques for the adjustment of the threshold voltage are available; by varying the doping concentration at the silicon insulator interface through ion implantation, or by using different insulating material for the gate [4].

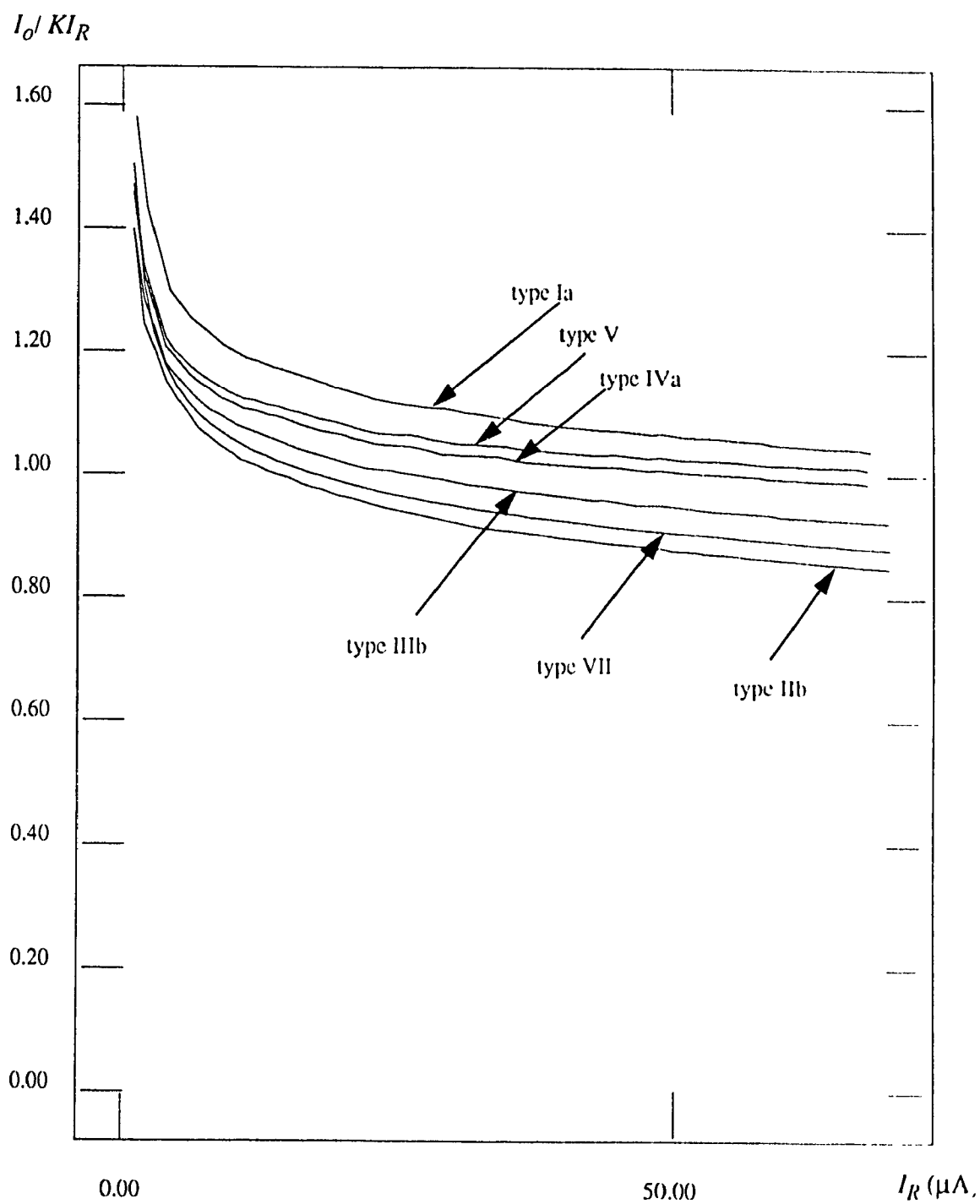


Fig.2.15
 Current ratio variation with reference current for NCMOS current mirrors
 with a current gain greater than unity (from analysis)

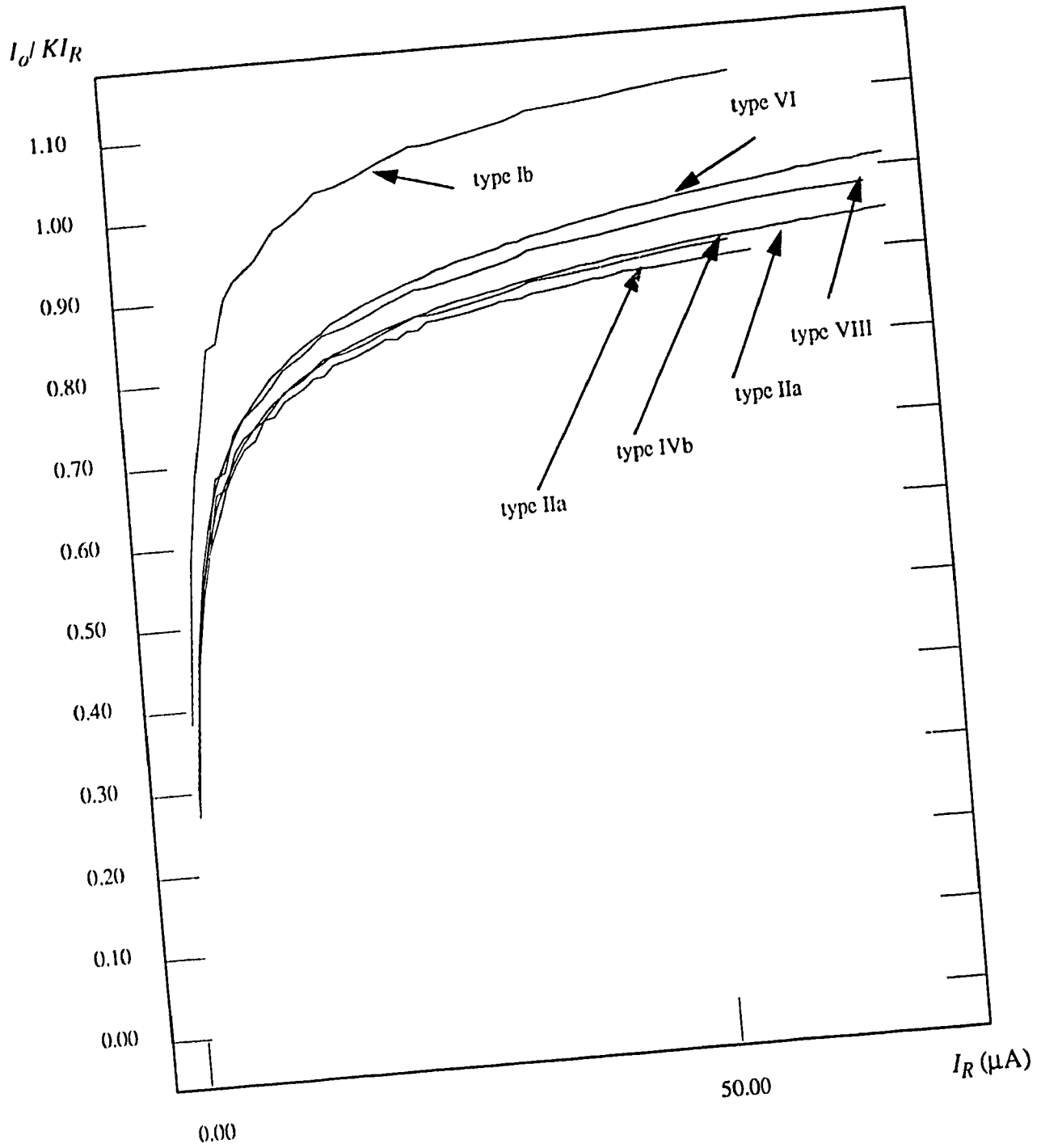
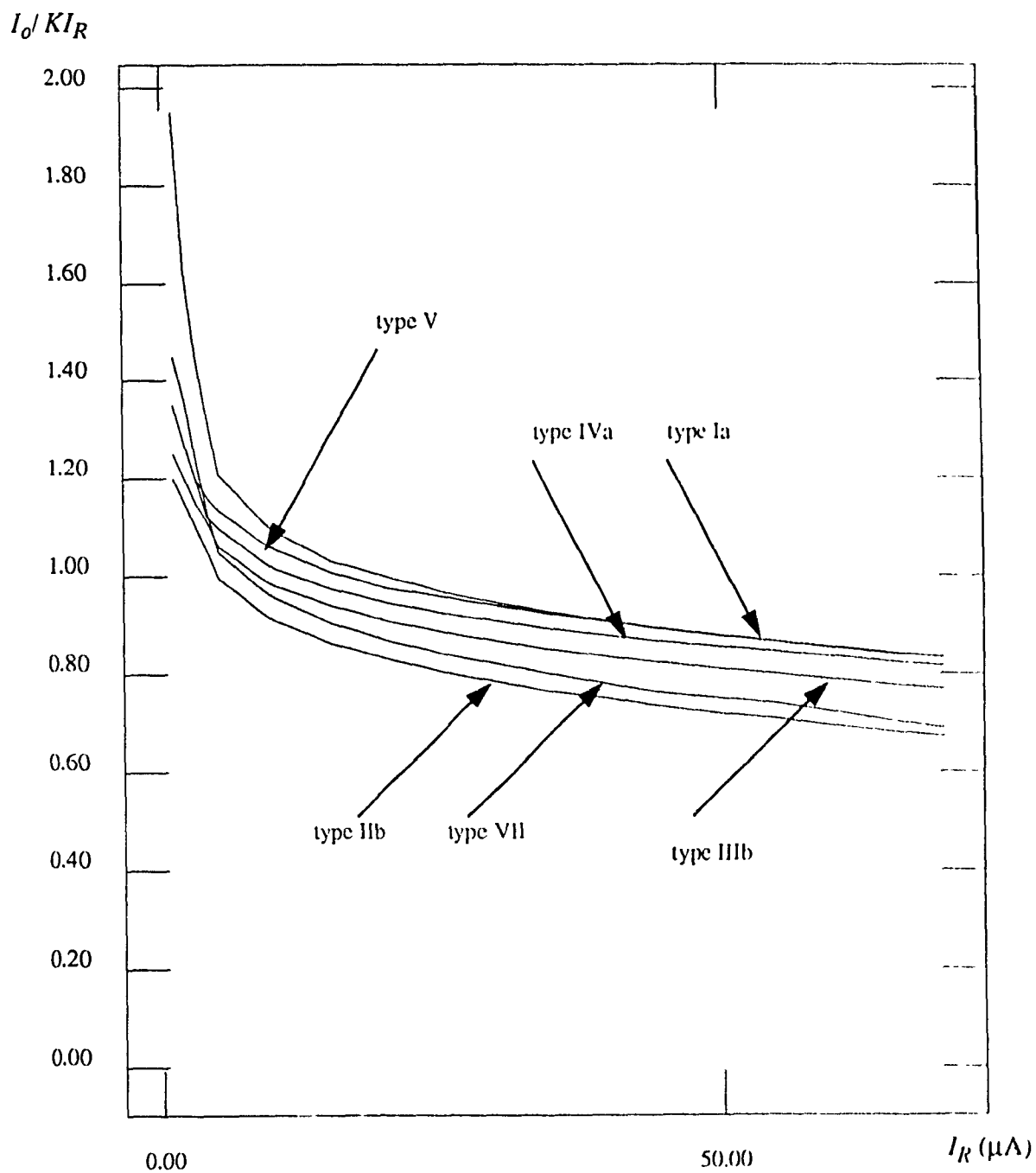


Fig.2.16
 Current ratio variation with reference current for NCMOS current mirrors.
 with a current gain less than unity (from analysis)



2.17

Current ratio variation with reference current for NCMOS current mirrors
with a current gain greater than unity (from HSPICE simulation)

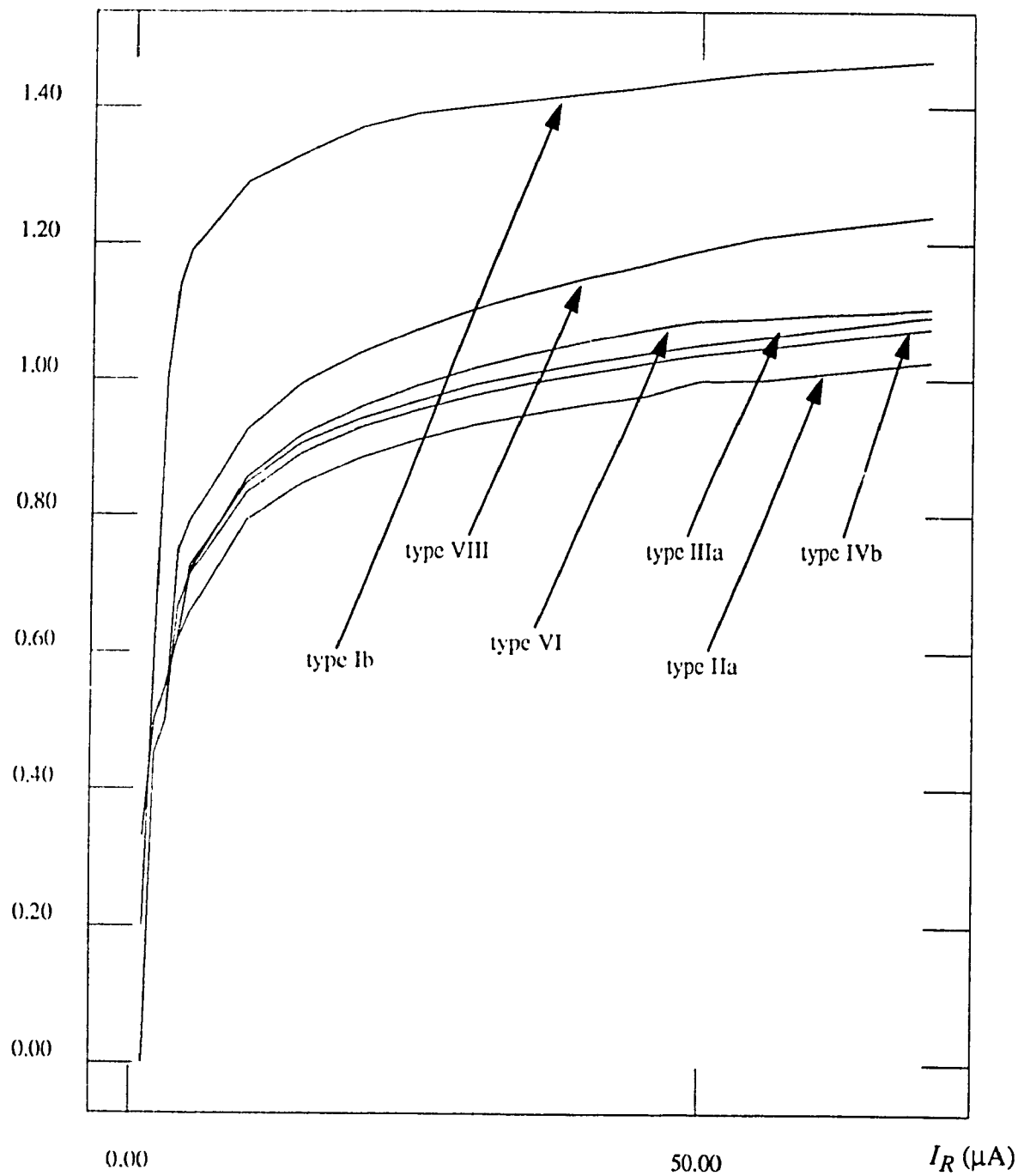
I_O / KI_R


Fig.2.18

Current ratio variation with reference current for NCMOS current mirrors
with a current gain less than unity (from HSPICE simulation)

If the threshold voltages can be made equal, as suggested above, the curves in Fig.2.15 and Fig.2.16 will be more flat, and their starting points will be closer to the unity value, as shown in Fig.2.19 and Fig.2.20. This means that current ratios become more stable with respect to the reference current variations.

Another modification is also possible by using the new (1.2 μm) technology where the λ factor can be made equal to zero[4]. This means that the current gain equation for NCMOS current mirrors with a gain greater than unity, will be:

$$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \quad (2.40)$$

The corresponding current gain equation for NCMOS current mirrors with a gain less than unity will be:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \quad (2.41)$$

Fig.2.21 shows two curves (curve 1 and curve 2) for the above two types of NCMOS current mirrors which specify the current gain as a function of the reference current. If both modification are used, then eqn. (2.40) will be:

$$\frac{I_o}{I_R} = \frac{K_n}{K_p} \quad (2.42a)$$

And eqn. (2.41) becomes:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \quad (2.42b)$$

The two previous equations show that with such modifications the current gain will be fixed by the values K_n/K_p or K_p/K_n , depending on the model used, even if there is a variation in the reference voltage V_R or the output voltage. The curves of current gain variation with the reference current shown in Fig.2.19 and Fig.2.20 will change to straight horizontal line, at two constant levels for all NCMOS current mirrors as shown in Fig.2.22 (curve 3). Finally, Fig. 2.23 to Fig. 2.34 compare the analysis and HSPICE simulation

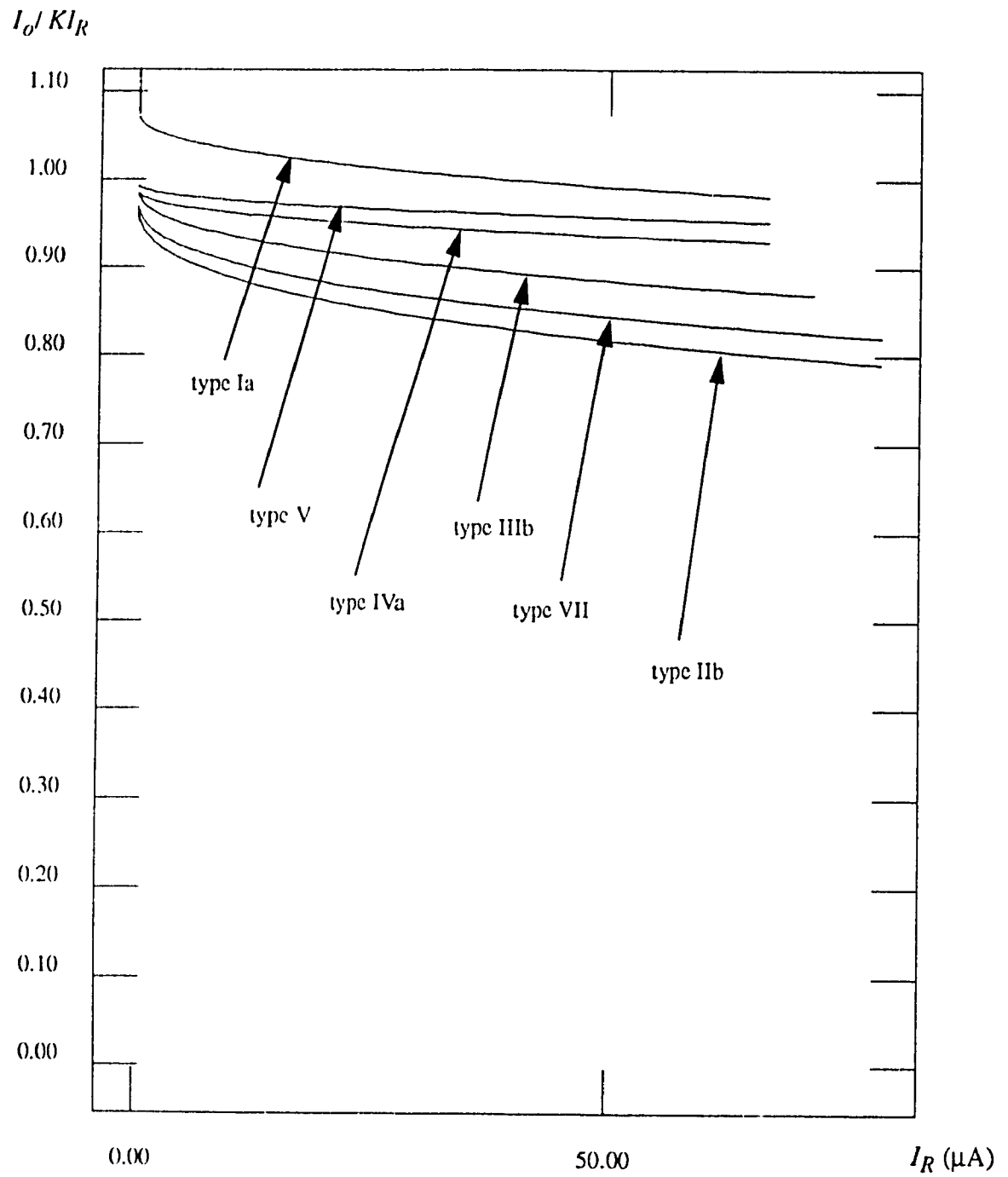


Fig.2.19
Current ratio variation with reference current for NCMOS current mirrors
with equal threshold voltages and a current gain greater than unity.

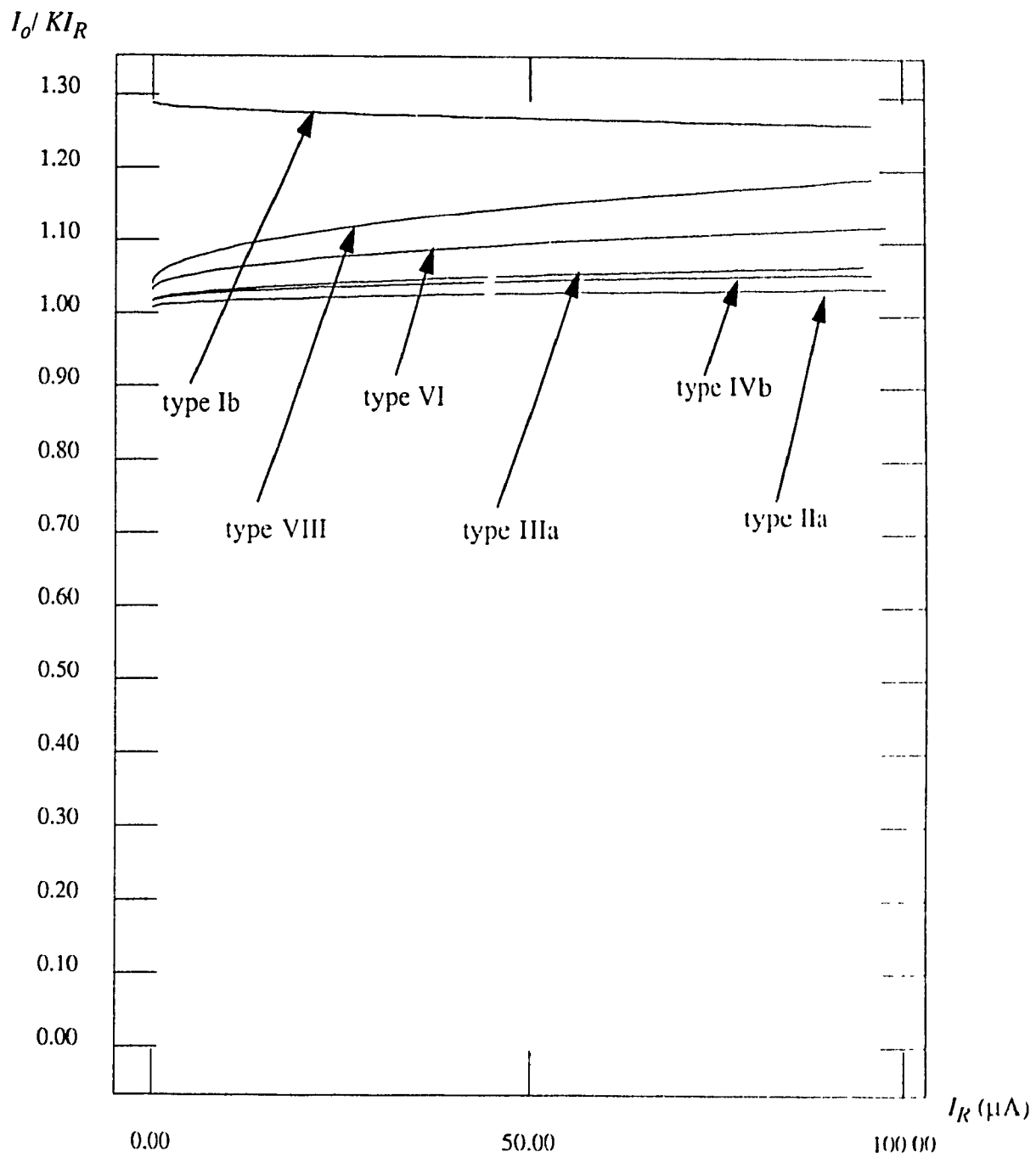


Fig.2.20

Current ratio variation with reference current for NCMOS current mirrors with equal threshold voltages and a current gain less than unity.

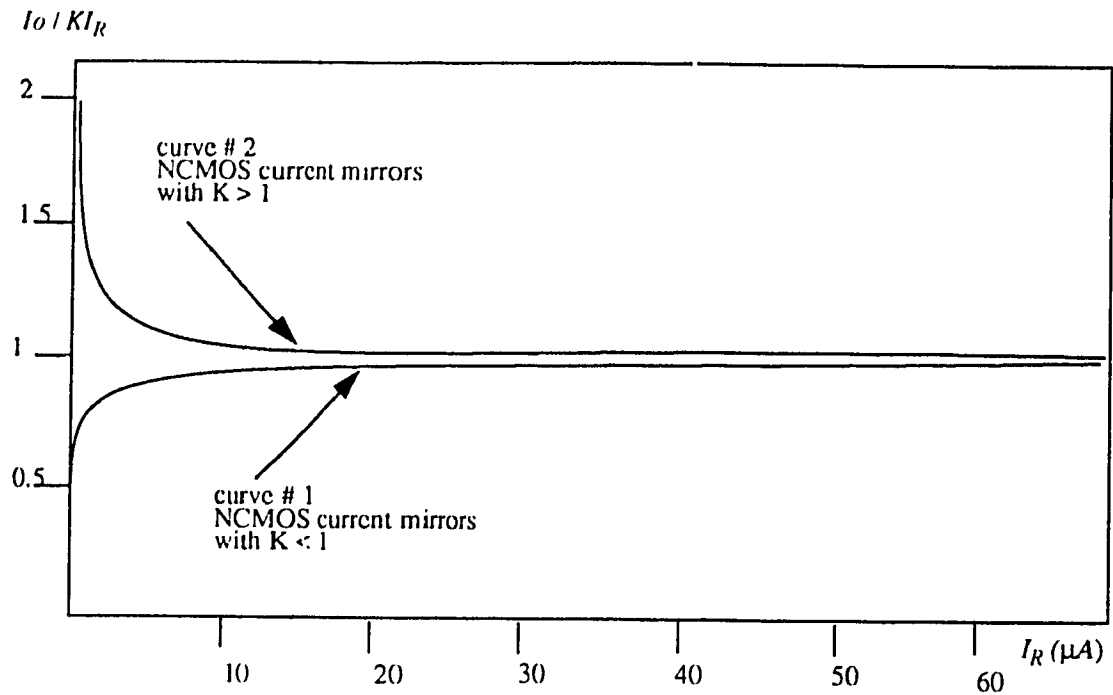


Fig. 2.21

Current ratio variation with reference current for NCMOS current mirrors with λ factor equal to zero. (1.2 micron model)

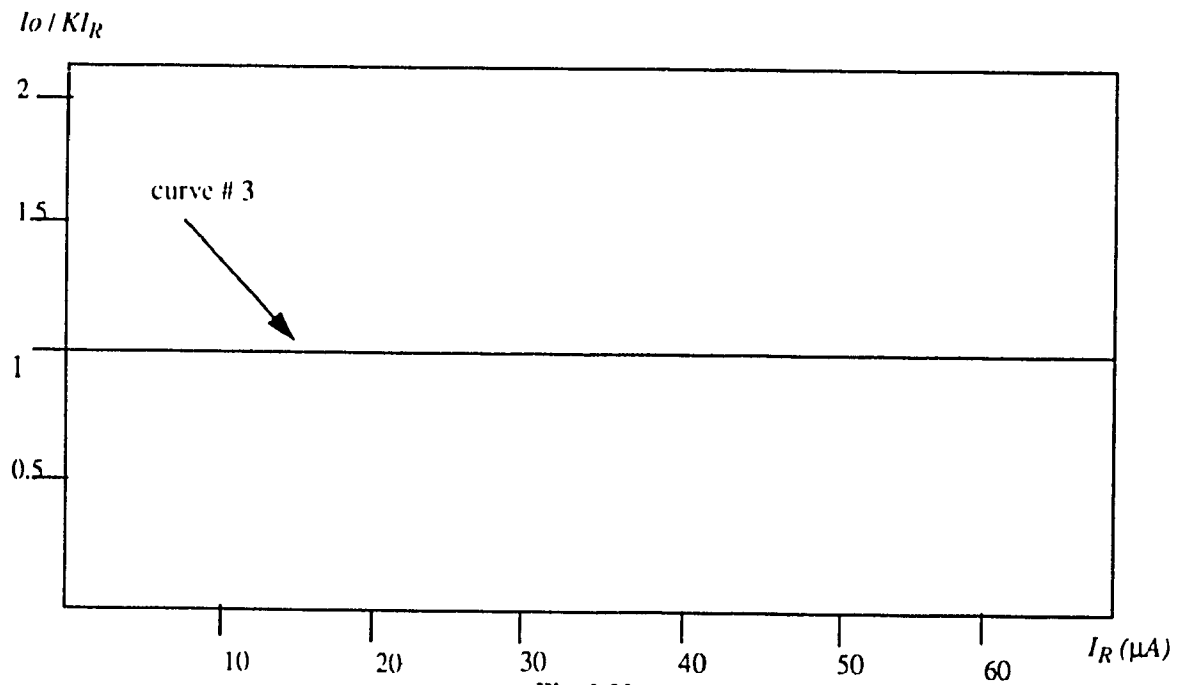


Fig. 2.22

Current ratio variation with reference current for NCMOS current mirrors with equal threshold voltages and λ factor equal to zero. (1.2 micron model)

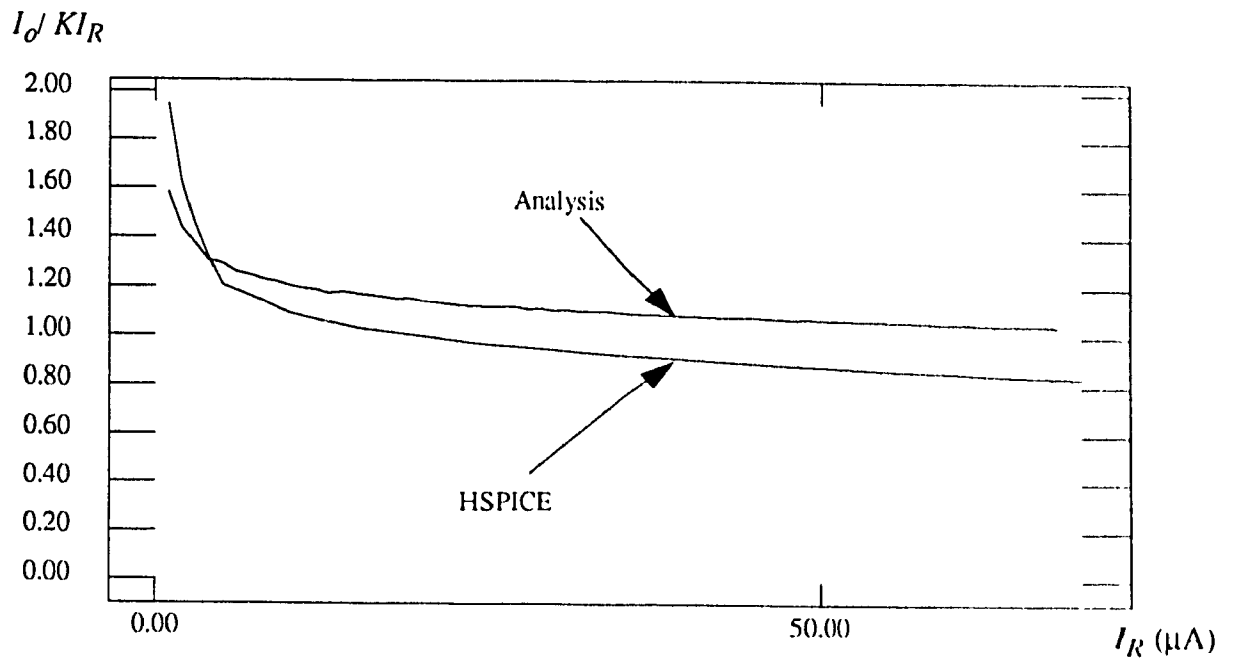


Fig.2.23

Current ratio variation with reference current for Type Ia current mirror according to both analysis and HSPICE results.

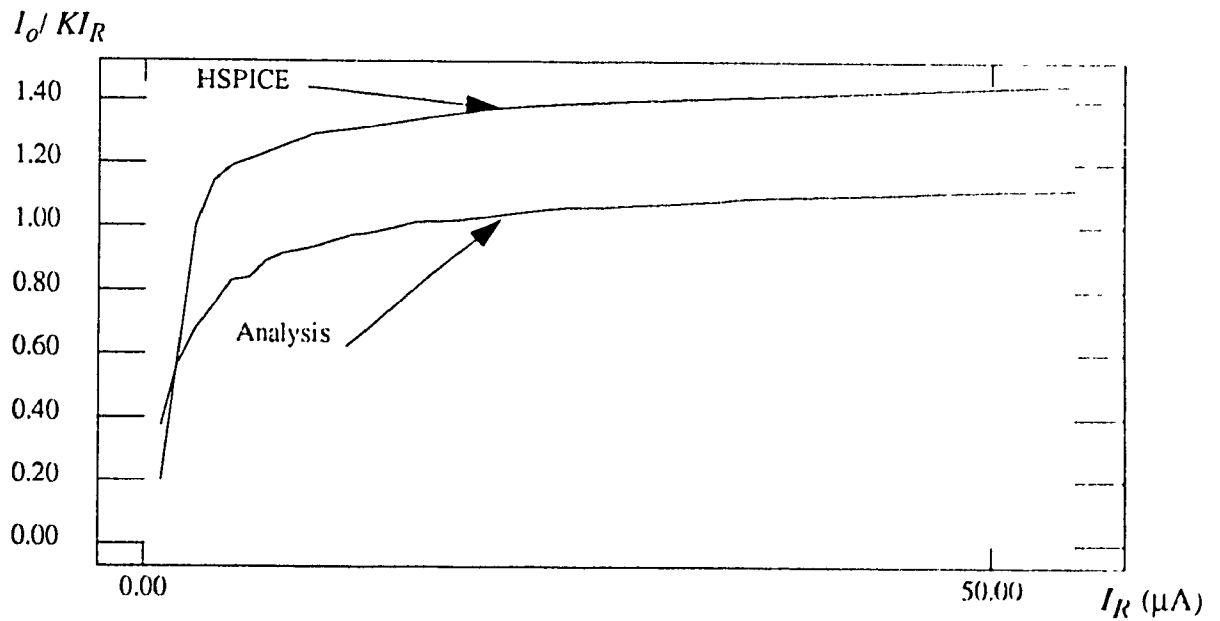


Fig. 2.24

Current ratio variation with reference current for Type Ib current mirror according to both analysis and HSPICE results.

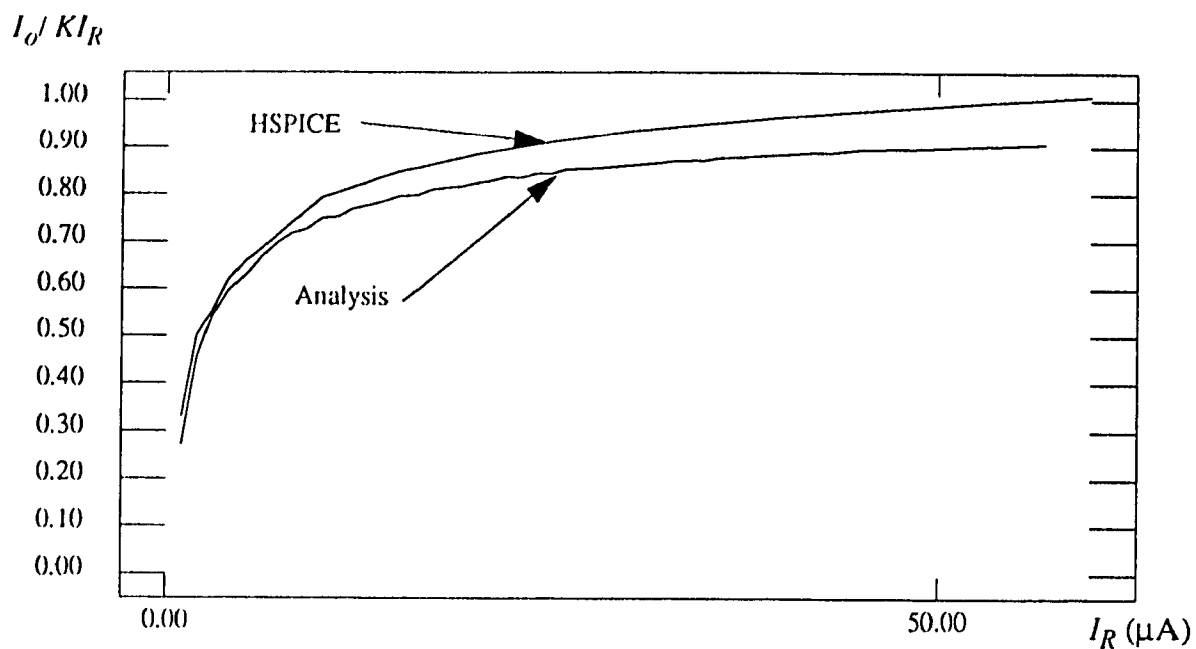


Fig. 2.25

Current ratio variation with reference current for Type IIa
NCMOS current mirror according to both analysis and HSPICE results.

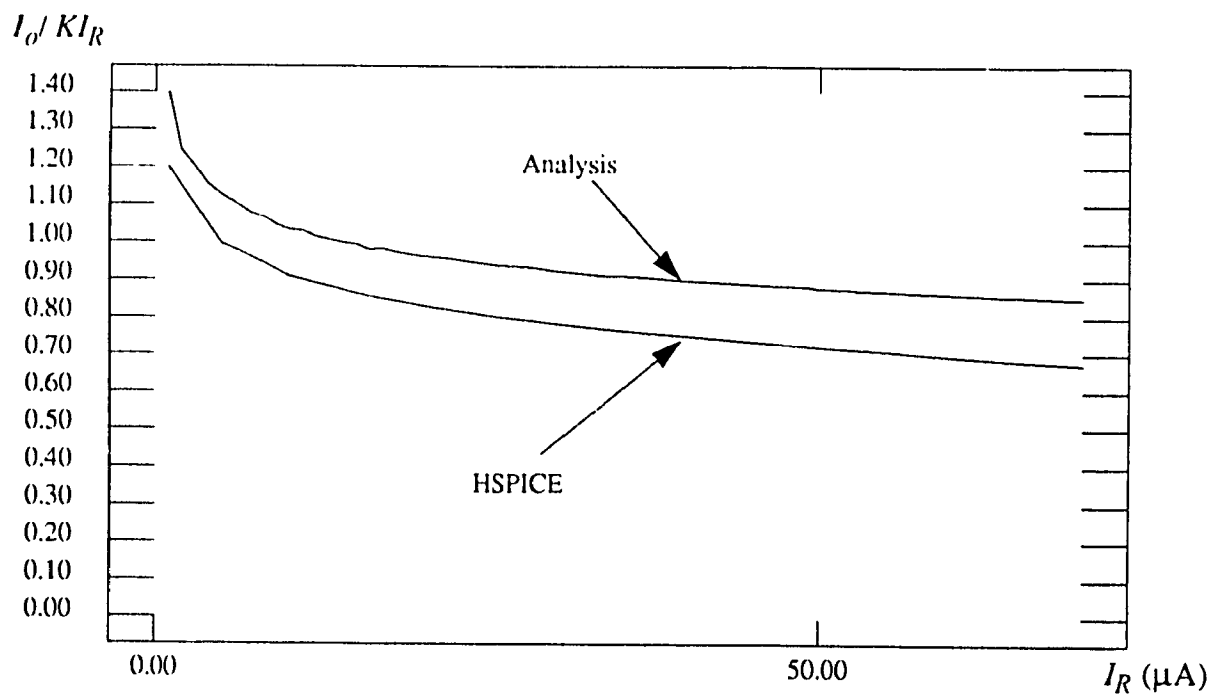


Fig. 2.26

Current ratio variation with reference current for Type IIb
NCMOS current mirror according to both analysis and HSPICE results.

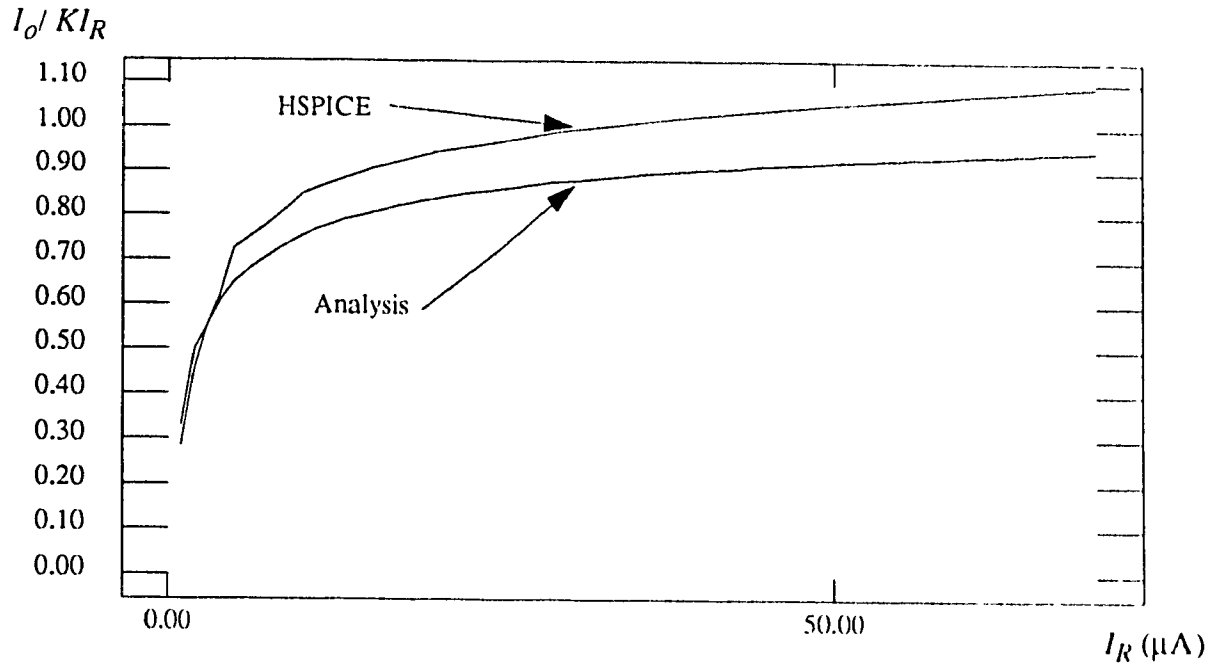


Fig. 2.27

Current ratio variation with reference current for Type IIIa
NCMOS current mirror according to both analysis and HSPICE results.

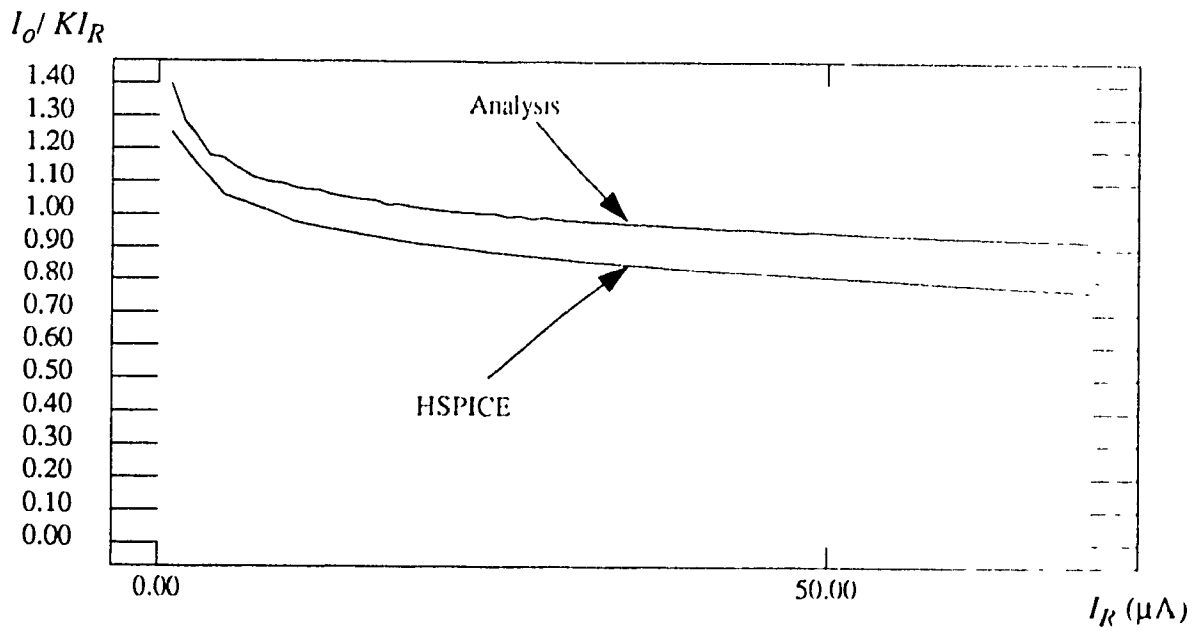


Fig. 2.28

Current ratio variation with reference current for Type IIIb
NCMOS current mirror according to both analysis and HSPICE results

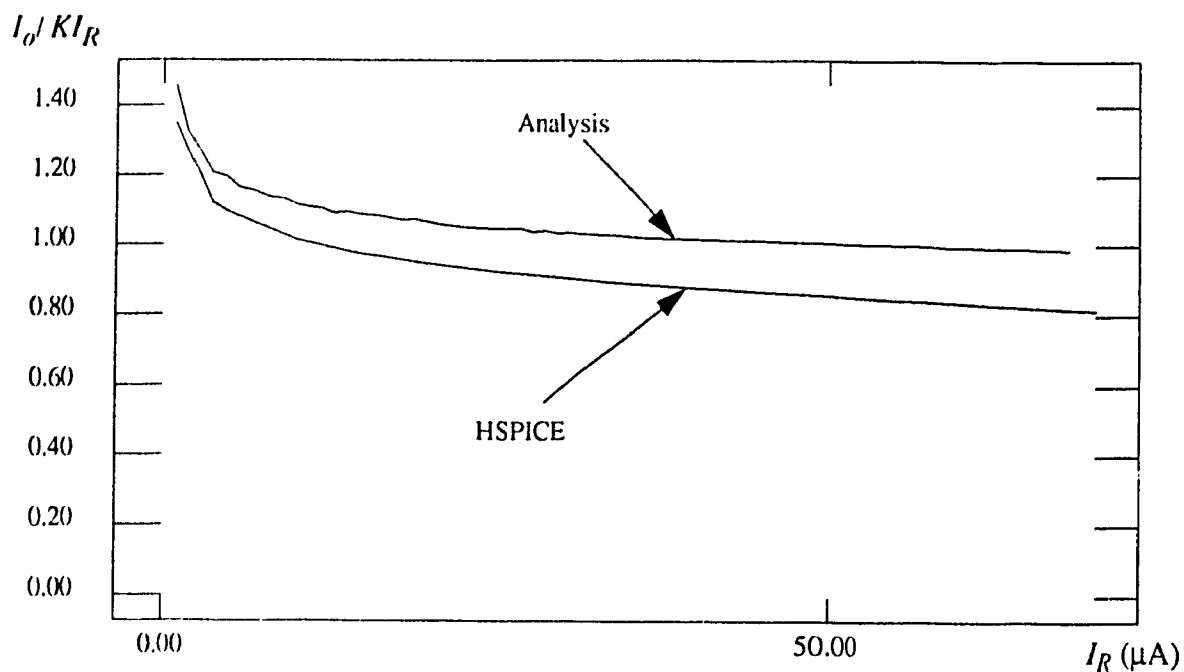


Fig. 2.29

Current ratio variation with reference current for Type IVa
NCMOS current mirror according to both analysis and HSPICE results.

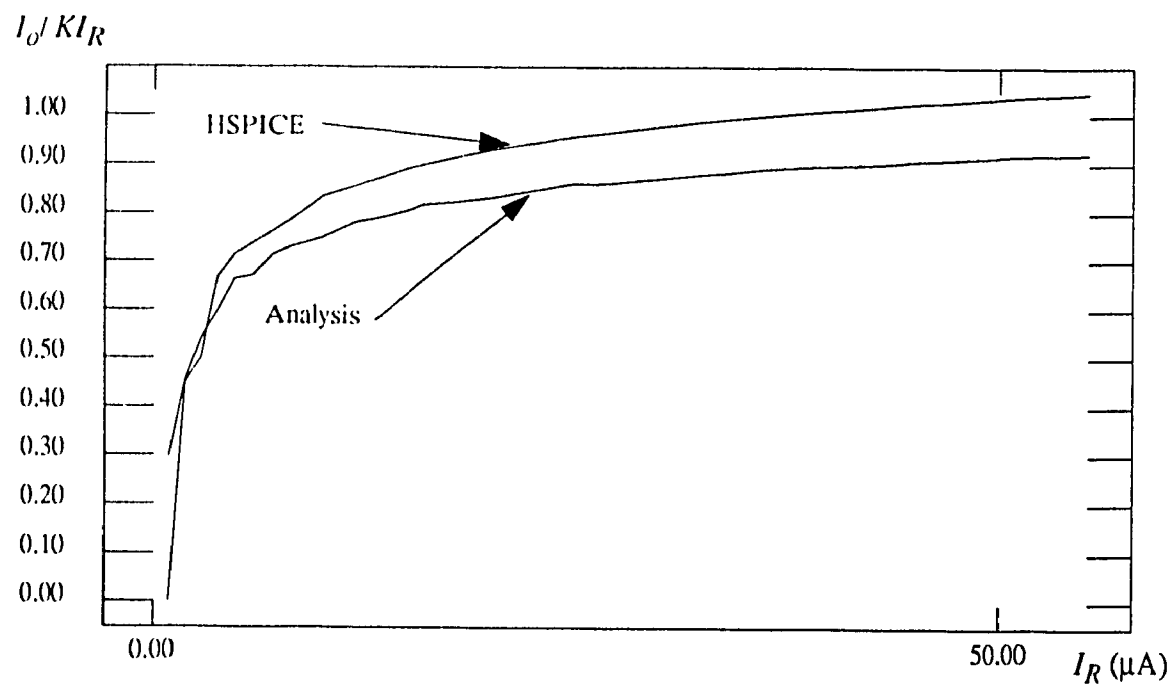


Fig. 2.30

Current ratio variation with reference current for Type IVb
NCMOS current mirror according to both analysis and HSPICE results

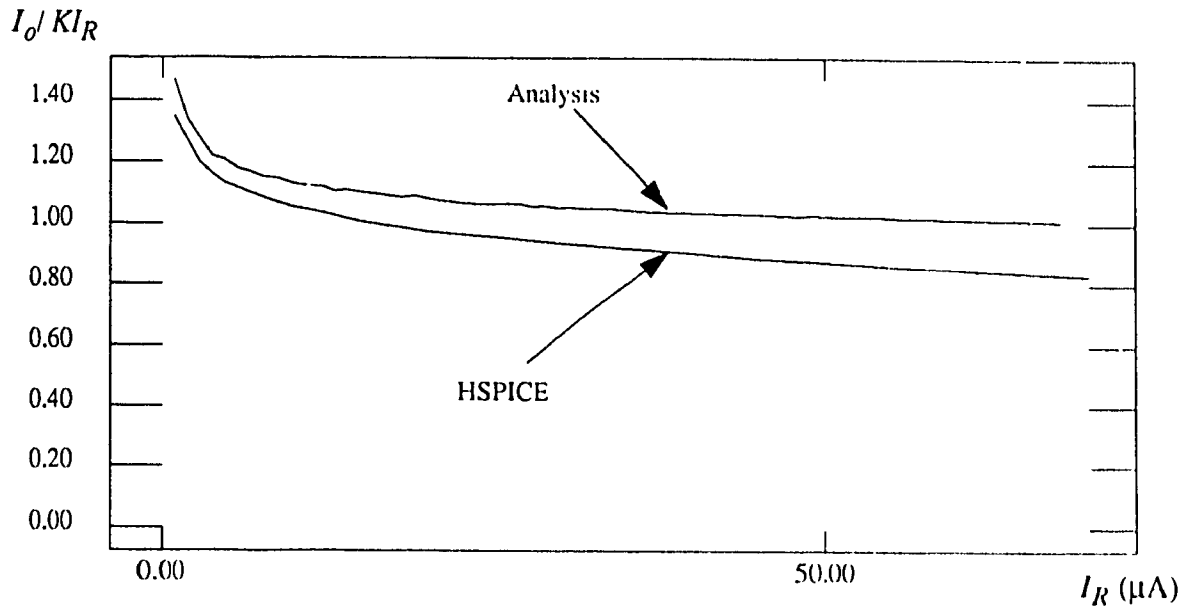


Fig. 2.31

Current ratio variation with reference current for Type V
NCMOS current mirror according to both analysis and HSPICE results.

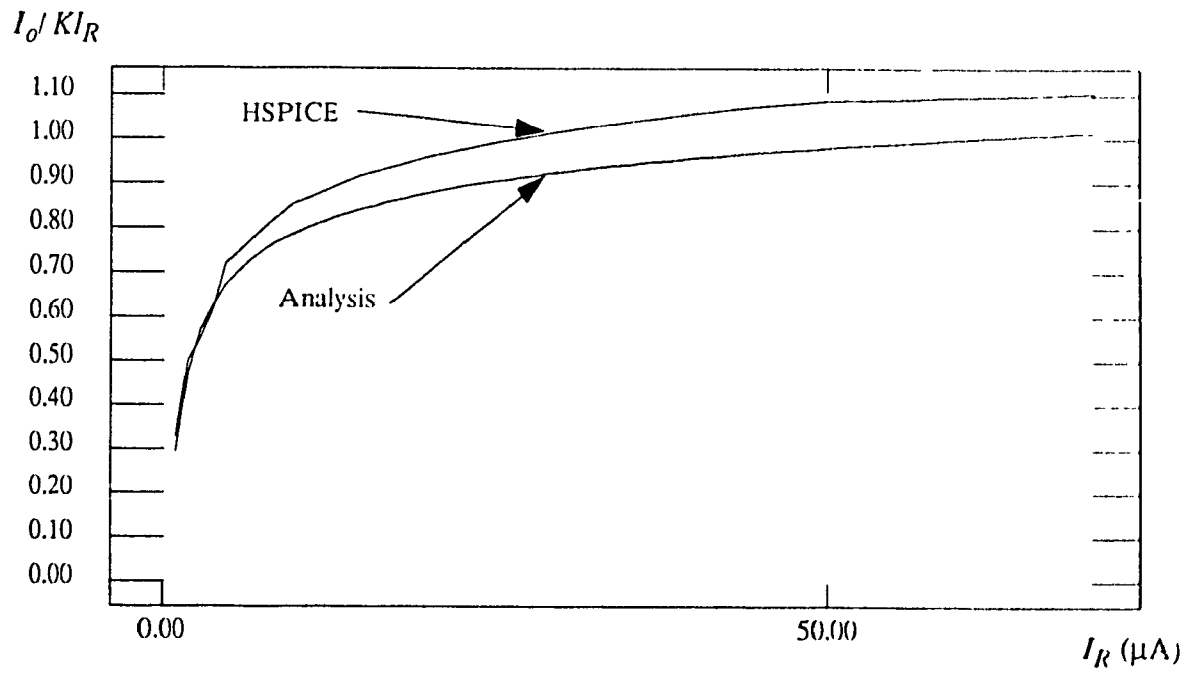


Fig. 2.32

Current ratio variation with reference current for Type VI
NCMOS current mirror according to both analysis and HSPICE results

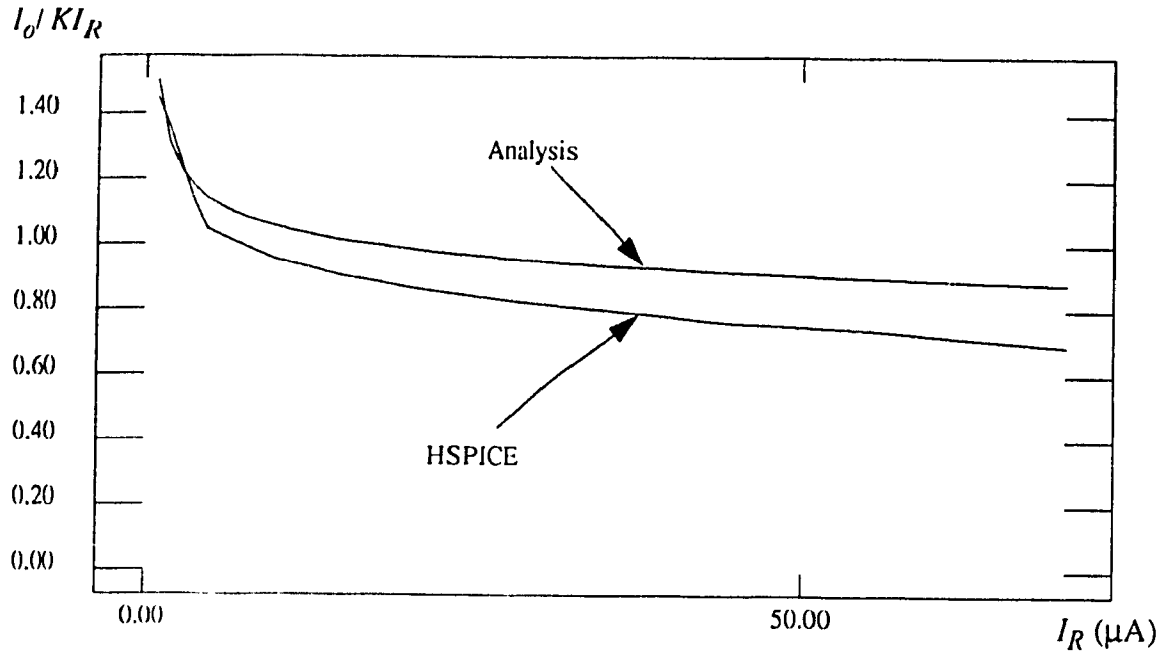


Fig. 2.33
Current ratio variation with reference current for Type VII
NCMOS current mirror according to both analysis and HSPICE results

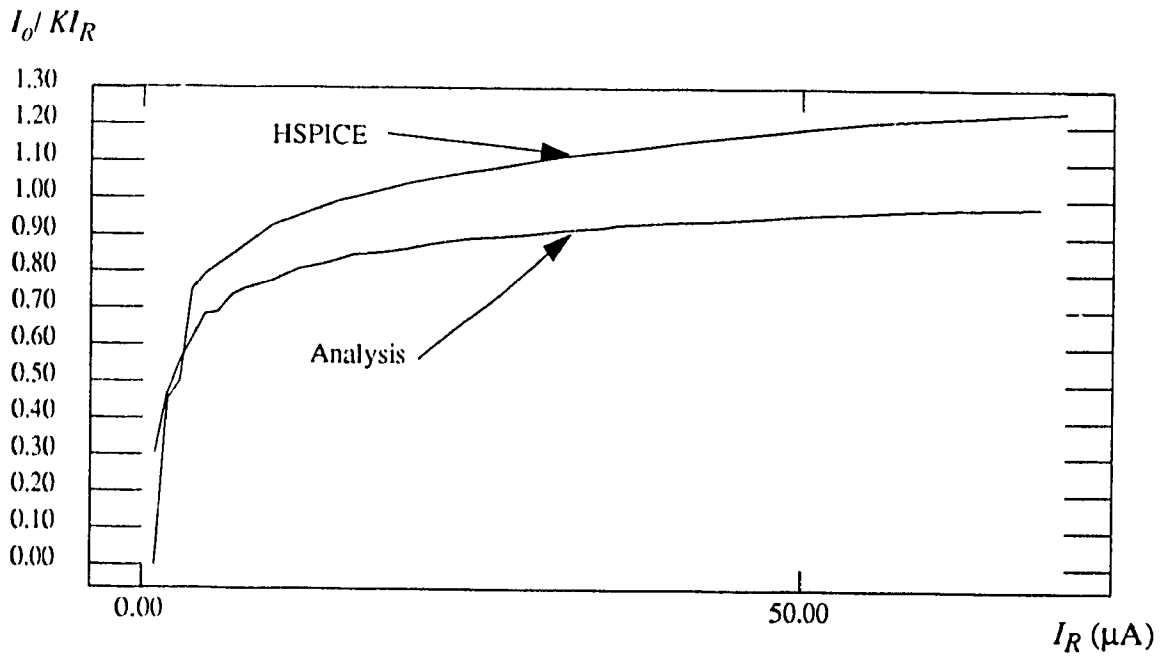


Fig. 2.34
Current ratio variation with reference current for Type VIII
NCMOS current mirror according to both analysis and HSPICE results.

(CMOS3 DLM, level3) results. The slight difference between the analysis and HSPICE simulation results are due to the difference between the MOSFET models used in both of them.

2.6 OUTPUT IMPEDANCE ANALYSIS

The output impedance of a current mirror should be high, as it is supposed to behave as a current source. In this section the small signal analysis of the output impedance for the NCMOS current mirrors is carried out. These NCMOS current mirrors are classified according to their output circuit configuration. A table for the final formulae of output impedance of the NCMOS current mirrors is also provided.

2.6.1 TYPE Ia NCMOS CURRENT MIRROR (SINK)

Referring to Fig.2.35, which shows the connections required for output impedance measurement and the small signal equivalent circuit, the value of r_{out} will be:

$$r_{out} = v_x / i_x = r_{o2} \quad (2.43)$$

where r_{o2} is the equivalent output impedance of transistor Q_2 at its operating point (Q), in the $(v_{DS} - i_D)$ characteristics shown in Fig.2.37, and it is equal to the inverse of the slope of the curve where the operating point (Q) is located. This output impedance will vary slightly when the output voltage changes according to load variation, but it will stay at the high value range as long as the operating point stays away from the active region.

2.6.2 TYPE Ib NCMOS CURRENT MIRROR (SOURCE):

Fig.2.36 shows both the connections required for output impedance measurements and its small signal equivalent circuit. Eqn. (2.43) will also define the output impedance (r_{out}) of this current mirror.

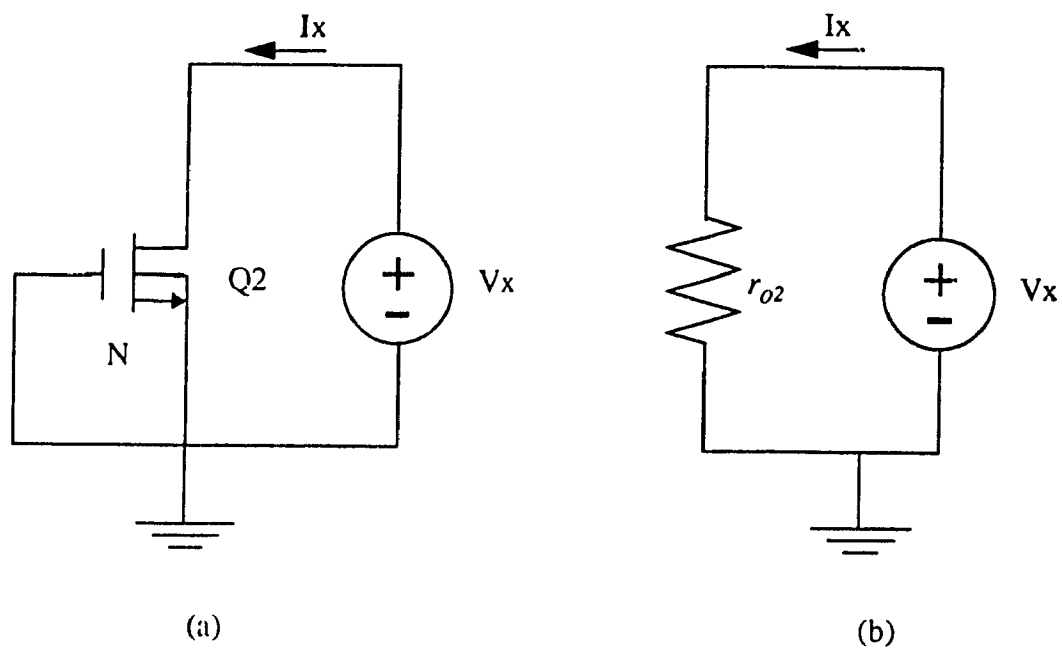


Fig.2.35

(a) Connection required for output impedance measurements of Type Ia current mirror. (b) small signal equivalent circuit

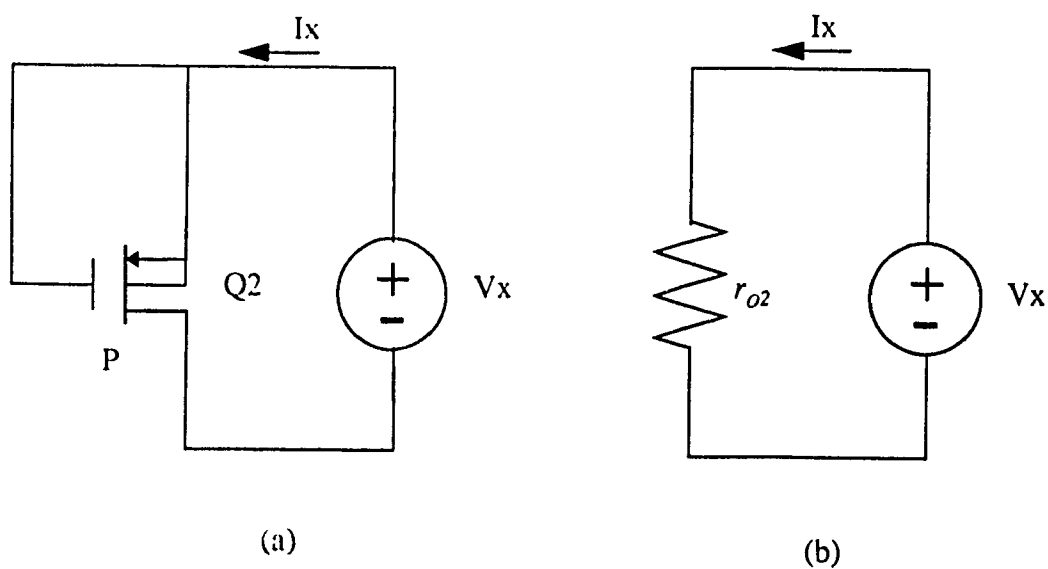


Fig.2.36

(a) Connection required for output impedance measurements of Type Ib current mirror. (b) small signal equivalent circuit.

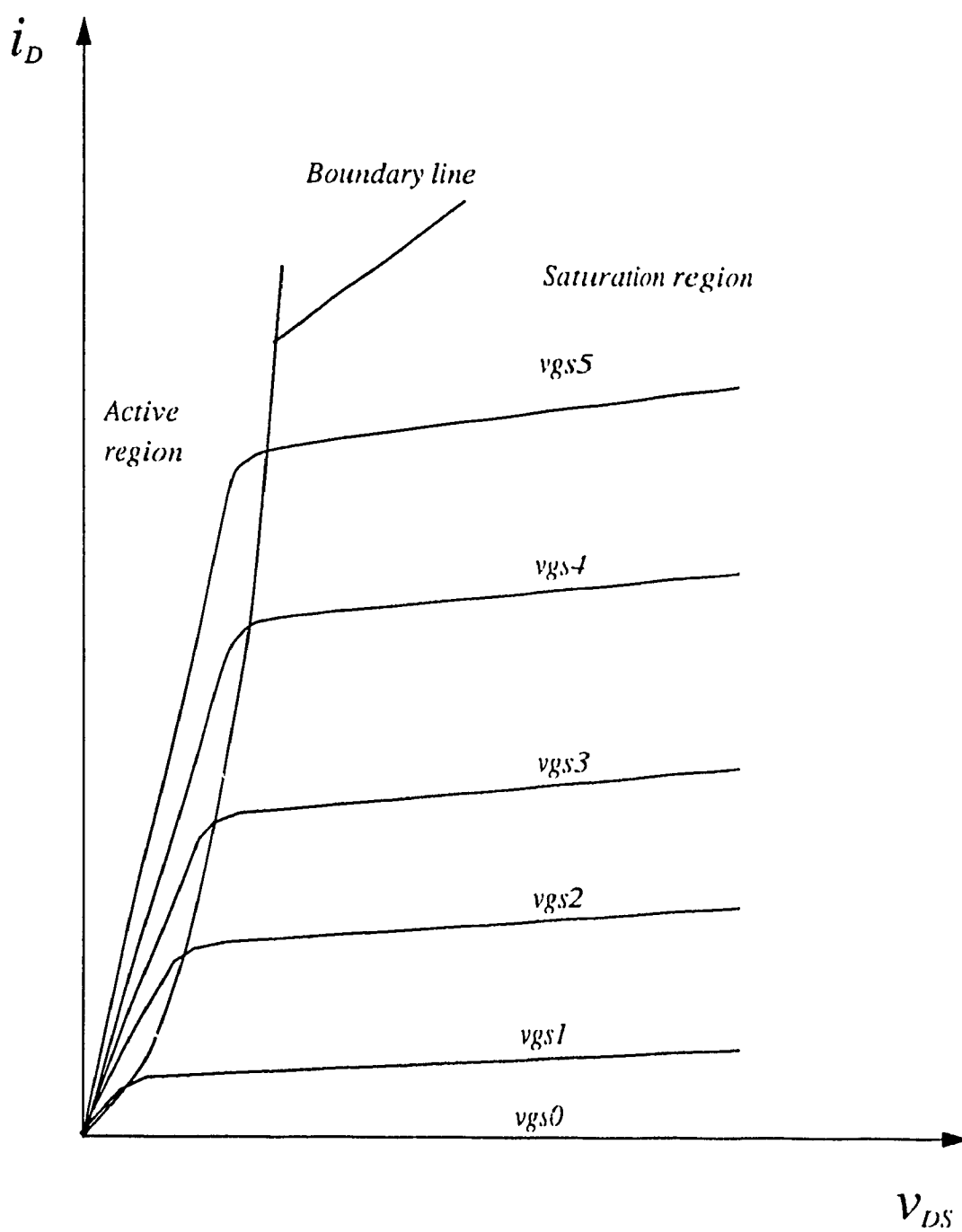


Fig. 2.37
 $i_D - V_{DS}$ characteristics of a MOSFET transistor.

Normally, this current mirror has lower output impedance, because the leakage current between the drain and the source of the output PMOS transistor of this circuit is higher than the leakage current of the NMOS output transistor in the previous circuit. This is under the assumption that these MOSFETs have the same size. This (r_o) value will also depend on the operating point location, or in other words it depends on the value of the load driven by the current mirror circuit.

2.6.3 TYPE II AND III NCMOS CURRENT MIRROR (SINK & SOURCE):

Type II and III NCMOS current mirrors has the same output circuit MOS connections, as shown in Fig.2.38a, which means that they will have the same small signal output impedance circuit representation.

Since transistor Q_2 is connected as an active load, then its output impedance will be:

$$r_{o2} = \frac{1}{g_{m2}} \quad (2.44)$$

The small signal equivalent circuit for the output impedance is shown in Fig.2.38b.

The output impedance can be shown to be:

$$r_{out} = r_{o3} + \frac{1}{g_{m2}} + \frac{g_{m3}}{g_{m2}} \cdot r_{o3} \quad (2.45)$$

Or it can be written as follows:

$$r_{out} = \frac{1}{g_{m2}} + \left(\frac{g_{m3}}{g_{m2}} + 1 \right) \cdot r_{o3} \quad (2.46)$$

The sink version of these NCMOS current mirrors have the transistor Q_2 as a PMOS device, which will increase the output impedance of those sinks slightly because the lower mobility of the holes i.e. it has lower g_m .

The source version will follow the same analysis and the output impedance will have the same formula.

2.6.4. TYPE IV, V, VI, VII AND VIII NCMOS CURRENT MIRRORS:

The output impedance of these circuits follow the same analysis, thus only one circuit is going to be analyzed for the small signal output impedance. Type IV NCMOS current mirror, sink version has been selected for this analysis. The equivalent circuit for the output impedance of this current mirror is obtained by replacing transistors Q_2 and Q_3 by their equivalent small signal model, and their gates are connected to the ground[7], as shown in Fig.2.27.

We have:

$$r_{out} = \frac{v_x}{i_x},$$

From Fig.2.39b, we get:

$$v_x = i_x \cdot r_{o2} + i_3 \cdot r_{o3} \quad (2.47)$$

Since: $i_3 = i_x - i_2$, then the value of v_x will be equal to:

$$v_x = i_x \cdot r_{o2} + (i_x - i_2) \cdot r_{o3} \quad (2.48)$$

We observe that:

$$i_2 = v_{gs3} \cdot g_{m3} \quad (2.49)$$

From Fig. 2.39b:

$$v_{gs3} = -i_x \cdot r_{o2} \quad (2.50)$$

Substituting eqn. (2.49) and eqn. (2.50) into eqn. (2.48) will give:

$$v_x = i_x \cdot (r_{o2} + r_{o3}) + i_x \cdot r_{o2} \cdot r_{o3} \cdot g_{m3} \quad (2.51)$$

Dividing (v_x) by (i_x) gives r_{out} as shown below:

$$r_{out} = \frac{v_x}{i_x} = (r_{o2} + r_{o3}) + r_{o2} \cdot r_{o3} \cdot g_{m3} \quad (2.52)$$

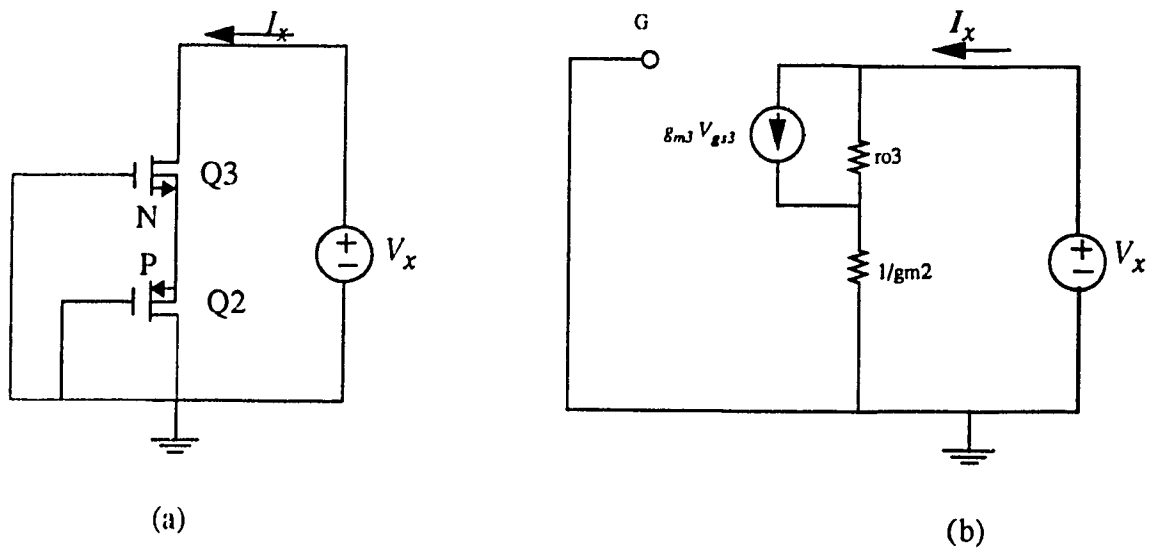


Fig.2.38

(a) Connection required for output impedance measurements of Type II and III NCMOS current mirrors. (b) small signal equivalent circuit

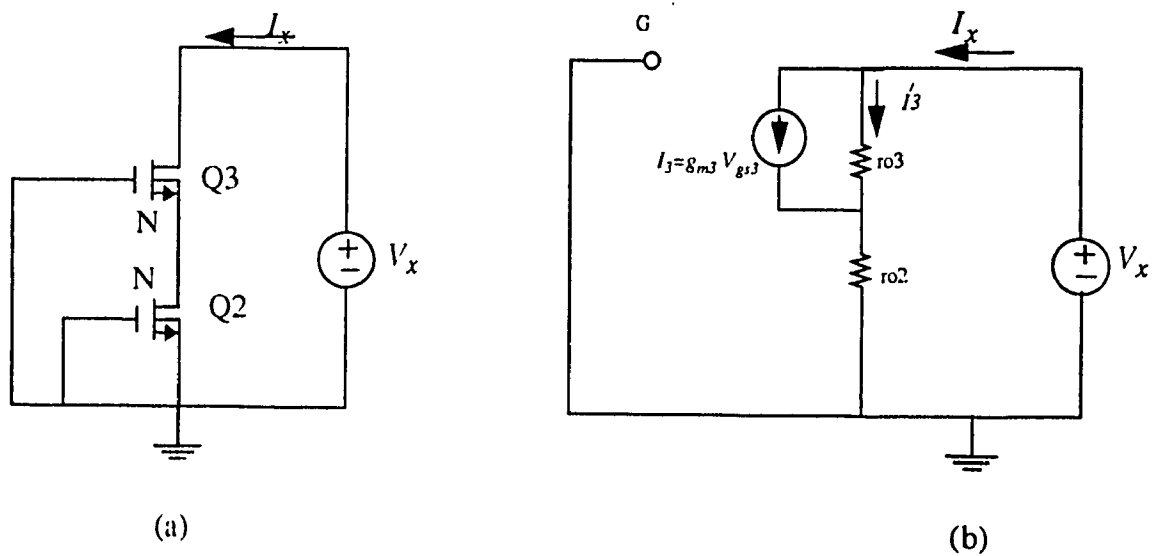


Fig.2.39

(a) Connection required for output impedance measurements of Type IV, V, VI, VII and VIII NCMOS current mirrors. (b) small signal equivalent circuit

Eqn. (2.52) shows that the value of r_{out} is higher than the output impedance of first six NCMOS current mirrors given in sec.2.6.1, sec.2.6.2 and sec.2.6.3. The output impedance of the NCMOS current mirrors with K factor less than unity is higher than the one with K greater than unity, because of lower mobility of holes in the PMOS device at the output stage. The source version of type IV NCMOS current mirror will follow the same previous analysis for its output impedance.

The last four types of NCMOS current mirrors circuits will also follow the same small signal output impedance analysis of type IV NCMOS current mirror, because none of these circuits have MOSFET transistor in output branch connected as an active load. This means that eqn. (2.52) is valid for output impedance representation for the four types of NCMOS current mirrors, as it is shown in Table 2.2. The results of the output impedance analyses for all the current mirrors are given in Table 2.2.

Table 2.2: Output impedance formulas for different NCMOS current mirrors

C.M type	Output Impedance formulas
Ia and Ib	$r_{out} = r_{o2}$
IIa, IIb, IIIa and IIIb	$r_{out} = \frac{1}{g_{m2}} + \left(1 + \frac{g_{m3}}{g_{m2}}\right) \cdot r_{o3}$
IVa, IVb, V, VI, VII and VIII	$r_{out} = r_{o2} + r_{o3} + g_{m3} \cdot r_{o2} \cdot r_{o3}$

A good current mirror should have the following properties.

- Stable output current for a wide range of load variation.
- High output impedance.

- c. Minimum output offset voltage.
- d. Minimum number of transistors.

The output offset voltage is defined as the lowest voltage across the output stage of a current mirror for which it still behaves as a current mirror. For an ideal current mirror, this voltage should be zero. The minimum output voltage formulas of the NCMOS current mirror are given in Table (2.3). Other relevant properties are also listed in this Table. A comparison between different NCMOS current mirror properties shown in this Table leads to following conclusions:

1. Type IVa (sink with $K=3.34$): highest output impedance group, fair current regulation, low output offset voltage and two additional transistors compared to the simplest versions.
2. Type VI (sink with $K=0.3$): highest output impedance group, low current regulation, fair output offset voltage. The price paid is two additional transistors compared to the simplest versions.
3. Type VIII (source with $K=3.34$): highest output impedance group, low current regulation, fair output offset voltage and two additional transistors.
4. Type IVb (source with $K=0.3$): highest output impedance group, fair current regulation, low output offset voltage and two additional transistors.

The selection of a NCMOS current mirror circuit will depend mainly on the required output impedance and the current regulation. For any specific design a suitable one can be selected from Table 2.3.

Table 2.3: Properties of the different NCMOS current mirrors.

C.M. type	output impedance	minimum output offset voltage	K factor ratio	$\left 1 - \frac{I_o}{K \cdot I_R}\right _{\max} \times 100\%$	No. of transistors
Type Ia Sink, $K > 1$	r_{o2}	$V_R - V_{Tn}$	3.34	30%	2
Type Ib Source, $K < 1$	r_{o2}	$V_R - V_{Tp}$	0.3	0%	2
Type IIa Sink, $K < 1$	$\frac{1}{g_{m2}} + \left(1 + \frac{g_{m3}}{g_{m2}}\right) \cdot r_{o3}$	$V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_f}{K_n}}$	0.3	21%	3
Type IIb Source, $K > 1$	$\frac{1}{g_{m2}} + \left(1 + \frac{g_{m3}}{g_{m2}}\right) \cdot r_{o3}$	$V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}}$	3.34	13%	3
Type IIIa Sink, $K < 1$	$\frac{1}{g_{m2}} + \left(1 + \frac{g_{m3}}{g_{m2}}\right) \cdot r_{o3}$	$V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_f}{K_n}}$	0.3	19%	4
Type IIIb Source, $K > 1$	$\frac{1}{g_{m2}} + \left(1 + \frac{g_{m3}}{g_{m2}}\right) \cdot r_{o3}$	$V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}}$	3.34	18%	4
Type IVa Sink, $K > 1$	$r_{o2} + r_{o3} + g_{m3} \cdot r_{o2} \cdot r_{o3}$	$2V_R - 2V_{Tn}$	3.34	19%	4
Type IVb Source, $K < 1$	$r_{o2} + r_{o3} + g_{m3} \cdot r_{o2} \cdot r_{o3}$	$2V_R - 2V_{Tp}$	0.3	19%	4
Type V Sink, $K > 1$	$r_{o2} + r_{o3} + g_{m3} \cdot r_{o2} \cdot r_{o3}$	$V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_f}{K_n}}$	3.34	21%	4

C.M. type	output impedance	minimum output offset voltage	K factor ratio	$\left 1 - \frac{I_o}{K \cdot I_R}\right _{max} \times 100\%$	No.of transistors
Type VI Sink, $K < 1$	$r_{o2} + r_{o3} + g_{m3} \cdot r_{o2} \cdot r_{o3}$	$V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}}\right) - V_{TP} \cdot \sqrt{\frac{K_p}{K_n}}$	0.3	16%	4
Type VII Source, $K > 1$	$r_{o2} + r_{o3} + g_{m3} \cdot r_{o2} \cdot r_{o3}$	$V_R + \sqrt{\frac{K_n}{K_p}} \cdot (V_R - V_{TN}) \times \sqrt{\frac{1 + \lambda_n V_R}{1 + 2\lambda_p V_R}}$	0.3	16%	4
Type VIII Source, $K < 1$	$r_{o2} + r_{o3} + g_{m3} \cdot r_{o2} \cdot r_{o3}$	$V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{TN} \cdot \sqrt{\frac{K_n}{K_p}}$	3.34	14%	4

2.7 STATISTICAL STUDY OF PARAMETER MISMATCH EFFECT ON OUTPUT CURRENT.

2.7.0 INTRODUCTION

A statistical model is proposed in this section to study the random errors in the output current due to the mismatch between two presumably similar MOS elements. This mismatch will cause a time-independent random difference in the parameters of identically designed devices[10]. Unlike the case for digital integrated circuits, the performance of the analog MOS integrated circuits depends heavily upon the element matching accuracy. This required accuracy depends on the application. For instance, the matching accuracy of MOS transistors used in a current mirror is a critical one[11]. Mismatch that can be observed between the parameters of a group of equally designed devices (MOS transistors) is the result of several random processes which occur during the fabrication steps of the devices[10]. In the fabrication of an integrated circuit pattern, the edges of interconnecting

wires and devices cannot be exactly located due to uncertainty in the locations of the particle beams and mask dimensions. The position of an edge is thus affected by a certain amount of noise so that an ideally straight line appears wavy[11]. The elements of MOS I.C.s are inherently subject to errors from two sources. One is the systematic error, which affect adjacent elements with identical geometries similarly. It can thus be reduced by proper matching techniques. The other is the random error, which differs from element to element, and therefore cannot be corrected by improved matching techniques. It hence presents the ultimate limitation of 0.1% on the achievable accuracy, with minor variations around this value depending on the MOSFET size[11]. The MOS transistors for analog circuits, will generally operate in the saturation region. The measured mismatches in V_T and K should be related to their saturation region values. Since the drain current for this region is given by:

$$I \cong \frac{K}{2} \cdot (V_{GS} - V_T)^2 \quad (2.53)$$

where I is the drain current, K is the conductance constant, and V_T is the threshold voltage. The statistically significant parameters of this model are V_T and K . The mismatch in V_T accounts for variations in the different charges quantities, and in the gate oxide capacitance per unit area. The variations in the dimensions, channel mobility and the gate oxide capacitance per unit area are measured as the mismatch in K .

The variance in the drain current may be written as[12]:

$$\frac{\sigma_I^2}{\bar{I}^2} = \frac{\sigma_K^2}{\bar{K}^2} + 4 \cdot \frac{\sigma_{V_T}^2}{(V_{GS} - \bar{V}_T)^2} - 4r \cdot \frac{\sigma_{V_T}}{(V_{GS} - \bar{V}_T)} \cdot \frac{\sigma_K}{\bar{K}} \quad (2.54)$$

This equation concerns the variance of a function of two variables (V_T and K). Here r is correlation coefficient between the mismatches in V_T and K , \bar{I} is the expected value of the random variable I , σ_I is the standard deviation of I , and so on for the rest of the variables.

Thus the mismatch in drain current at any operating point may be estimated if σ_K , σ_{V_T} and r are known.

The threshold voltage V_T and the conductance constant K can be determined experimentally by measuring the drain current versus the gate voltage for a small value of V_{DS} . The maximum slope of the I versus V_{GS} curve provides the value of K , while V_T is obtained from the intercept of maximum slope on the V_{GS} axis.

The correlation factor (r) between mismatches in V_T and K comes from the variation in oxide capacitance. Hence, a dependence between the mismatches in V_T and K can be expected. A theoretical expression for the correlation coefficient is derived in [13]. Also, the value has been experimentally measured[12]. For n-channel devices the agreement between theoretical and experimental values is excellent, while it is fair for the p-channel ones. However, both the theoretical and experimental values are close to zero, indicating that the mismatch in V_T and K are almost independent. From the above discussion, since the correlation factor (r) almost equal to zero then the variance in drain current which was given in eqn. (2.54) can be written as follows:

$$\frac{\sigma_I^2}{\bar{I}^2} = \frac{\sigma_K^2}{\bar{K}^2} + 4 \cdot \frac{\sigma_{V_T}^2}{(V_{GS} - \bar{V}_T)^2} \quad (2.55)$$

At low values of V_{GS} the dominant factor causing the drain current mismatch is the threshold voltage variation, while for higher values of V_{GS} (mid-rail) the conductance constant and the threshold voltage mismatch have almost equal contributions to the drain current mismatch[12]. A note to take care of it, the square shaped MOSFET ($W=L$) will have the lowest variance of the drain current[14].

2.7.1. CONDUCTANCE CONSTANT MISMATCH

The conductance constant for any MOSFET transistor is given by:

$$K = \mu \cdot C \cdot \frac{W}{L} \quad (2.56)$$

where μ is the channel mobility, C is the gate oxide capacitance, W and L are the width and length dimensions of the gate, respectively[12]. The variance of the conductance constant can be expressed in terms of the variances of the mutually independent components, i.e., W , L , μ , and C :

$$\frac{\sigma_K^2}{\bar{K}^2} = \frac{\sigma_W^2}{\bar{W}^2} + \frac{\sigma_L^2}{\bar{L}^2} + \frac{\sigma_C^2}{\bar{C}^2} + \frac{\sigma_\mu^2}{\bar{\mu}^2} \quad (2.57)$$

The mismatch-generating processes for the gate oxide capacitance and the mobility[10] lead to a standard deviation in both quantities as:

$$\frac{\sigma_C^2}{\bar{C}^2} = \frac{1}{\bar{L} \cdot \bar{W}} \cdot A_{ox} \quad (2.58)$$

where A_{ox} is the parameter to be determined from measurements, and is equal to

$6.46 \times 10^{-14} \text{ cm}^2$ for n-channel device and $3.003 \times 10^{-12} \text{ cm}^2$ for p-channel device. Also,

$$\frac{\sigma_\mu^2}{\bar{\mu}^2} = \left(\frac{A_\mu}{\bar{L} \cdot \bar{W}} \right)^{0.5} \quad (2.59)$$

where $(A_\mu)^{0.5} = 4.95 \times 10^{-7} \text{ cm}$ for n-channel device, and it is not known for p-channel device. Substituting eqn.(2.58) and eqn.(2.59) into eqn.(2.57) the standard deviation of the K factor will be:

$$\frac{\sigma_K^2}{\bar{K}^2} = \frac{1}{\bar{L} \cdot \bar{W}} \cdot (A_{ox} + A_\mu) + \frac{\sigma_W^2}{\bar{W}^2} + \frac{\sigma_L^2}{\bar{L}^2} \quad (2.60)$$

Due to raggedness it is found that σ_L and σ_W are approximately the same and in the range of 0.01 to 0.03 μm . An average value 0.02 μm can be used for σ_L and σ_W [12]. The value of A_μ and A_{ox} are $2.64 \times 10^{-13} \text{ cm}^2$ and $0.646 \times 10^{-13} \text{ cm}^2$, respectively, for an n-channel device. The value of A_{ox} for the p-channel device is $3.0369 \times 10^{-12} \text{ cm}^2$. The value of A_μ for p-channel device can be found as follows:

Since $\bar{L} = \bar{W} = 3 \mu\text{m}$ for the 3 micron technology, then: $\sqrt{\frac{1}{\bar{L}^2} + \frac{1}{\bar{W}^2}} = 4717 \text{ cm}^{-1}$.

The value of $\frac{\sigma_K}{\bar{K}}$ is plotted in Fig.2.40 for an n-channel device[12]. Using this figure for the above values of \bar{W} and \bar{L} , $\frac{\sigma_K}{\bar{K}}$ is approximately equal 1.15%, which gives $\frac{\sigma_K^2}{\bar{K}^2} = 1.31$.

Substituting these values into eqn.(2.60), the value of A_μ for p-channel will approximately be equal to $8.725 \times 10^{-13} \text{ cm}^2$.

Using eqn.(2.60) and its parameters values, the variance in the K conductance factor for the n-channel MOSFET is:

$$\frac{\sigma_K^2}{\bar{K}^2} = \frac{1}{9 \times 10^{-8}} \times (2.64 \times 10^{-13} + 0.646 \times 10^{-13}) + \frac{(0.02)^2 \times 10^{-12}}{9 \times 10^{-12}} + \frac{(0.02)^2 \times 10^{-12}}{9 \times 10^{-12}}$$

$$\frac{\sigma_K^2}{\bar{K}^2} = 9.2345 \times 10^{-5}$$

while for the p-channel MOSFET the value of the variance is:

$$\frac{\sigma_K^2}{\bar{K}^2} = 1.3234 \times 10^{-4}$$

The percent variation in the standard deviation of the K conductance factor for the n-channel MOSFET is $\frac{\sigma_K}{\bar{K}} \%$ will be 9.609%, and for the p-channel it is 1.15%

2.7.2. THRESHOLD VOLTAGE MISMATCH

Gate material choice and channel doping level will determine the threshold voltage for the MOSFET. To maximize the performance of the devices, the threshold voltages of the n-channel and p-channel MOSFETs should be comparable, and ideally of equal magnitudes[15]. The threshold voltage can be expressed as:

$$V_T = \Phi_{MS} + 2\Psi_B - \frac{Q_f}{C_{ox}} + \frac{Q_B}{C_{ox}} \quad (2.61)$$

where Φ_{MS} is the gate-semiconductor work function difference, Ψ_B is the substrate Fermi potential, Q_f is the fixed charge in the gate oxide, Q_B is the depletion region charge in the substrate and C_{ox} is the gate oxide capacitance per unit area.

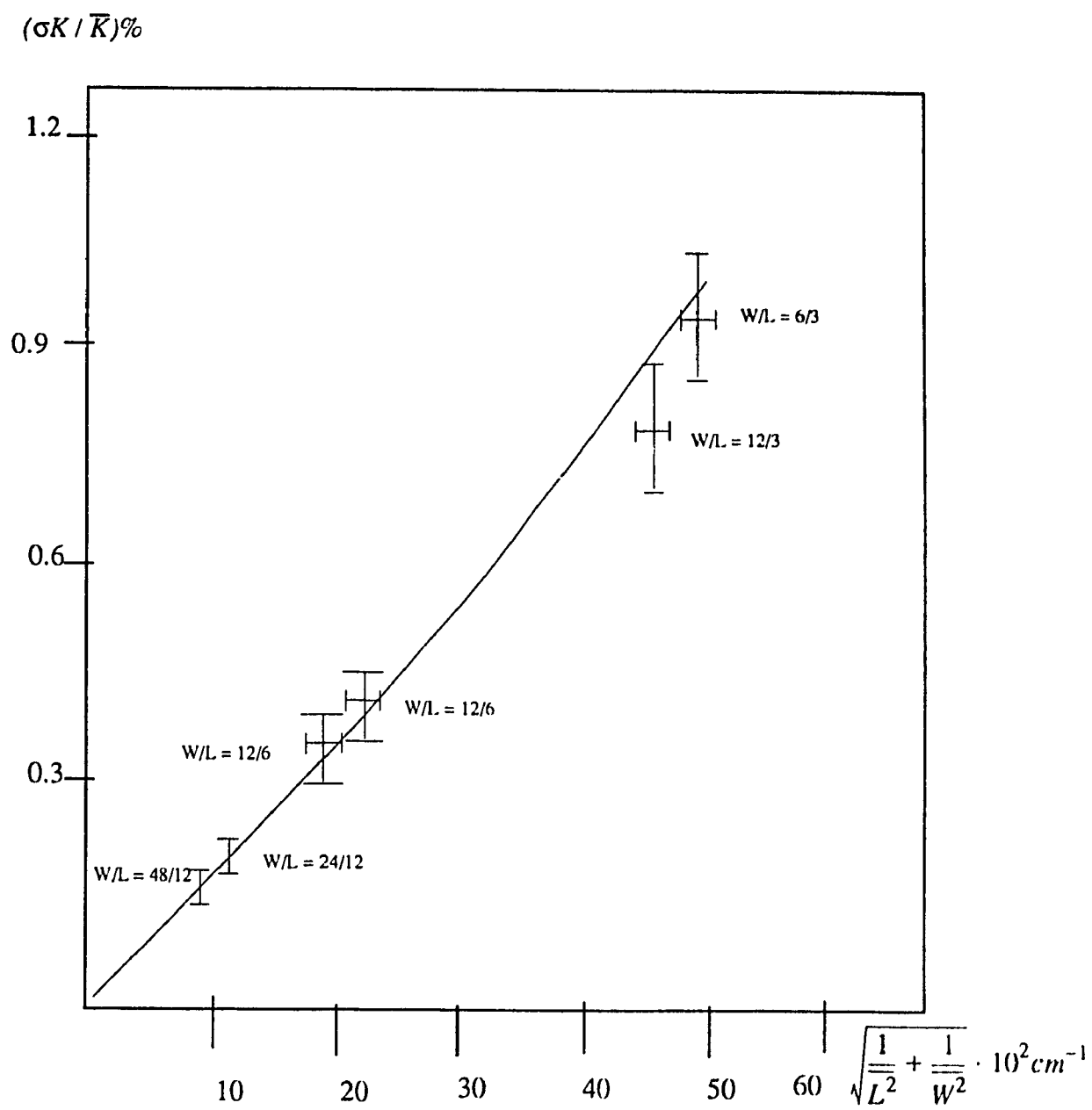


Fig.2.40

Conductance constant mismatch versus dimension for P-channel device[12].

The standard deviation of the threshold voltage in eqn.(2.61) can be determined through the determination of the standard deviation of the parameters in the right hand side of eqn.(2.61). Both Ψ_B and Φ_{MS} have a logarithmic dependence on the substrate doping while Φ_{MS} depends on another parameter which is the polysilicon gate doping. The previous two terms are regarded as constants, not affected by any mismatch[12].

The gate oxide fixed charge (Q_f) has a poisson distribution. Its variation can be written as:

$$\sigma_{Q_f}^2 = q \cdot \frac{\bar{Q}_f}{L \cdot \bar{W}} \quad (2.62)$$

where L is the effective length, W is the effective width of the channel and q is the electron charge.

The depletion region charge in the substrate Q_B is randomly depending on the distribution of the dopant atoms[12]. The variance in Q_B is:

$$\frac{\sigma_{Q_B}^2}{\bar{Q}_B^2} = \frac{1}{4\bar{L} \cdot \bar{W} \cdot \bar{W}_d \cdot \bar{N}_A} \quad (2.63)$$

where W_d is the width of depletion layer and N_A is the substrate doping.

The variance in gate oxide capacitance C_{ox} depends on the variance in oxide thickness and the permittivity. It can be written as:

$$\frac{\sigma_C^2}{\bar{C}^2} = \frac{1}{L \cdot \bar{W}} \cdot A_{ox} \quad (2.64)$$

where A_{ox} is a constant parameter determined from measurements.

Since the random variables Q_f , Q_B and C are all independent, then the variance in the threshold voltage can be written as:

$$\sigma_{V_t}^2 = \frac{1}{\bar{C}^2} \cdot (\sigma_{Q_B}^2 + \sigma_{Q_f}^2) + \frac{\sigma_C^2}{\bar{C}^2} + \frac{\bar{Q}_B^2}{\bar{C}^2} + \frac{\bar{Q}_f^2}{\bar{C}^2} \quad (2.65)$$

Substituting eqn. (2.62) and eqn. (2.64) into eqn. (2.65) and by assuming Q_B has the same variance approximately as Q_f , the variance in threshold voltage will be:

$$\sigma_{V_T}^2 = \frac{1}{\bar{L} \cdot \bar{W} \cdot \bar{C}^2} \cdot (q \cdot (\bar{Q}_B + \bar{Q}_f) + A_{ox} \cdot (\bar{Q}_B^2 + \bar{Q}_f^2)) \quad (2.66)$$

First for n-channel MOSFET device the values of $Q_B = 7.7 \times 10^{-8} \text{ C/cm}^2$, $Q_f = 3.2 \times 10^{-9} \text{ C/cm}^2$, $A_{ox} = 6.4631 \times 10^{-14} \text{ cm}^2$ and $q = 16.019 \times 10^{-10} \text{ Coulombs}$, then the standard deviation of the n-channel threshold voltage will be equal to:

$$\frac{\sigma_{V_T}}{\bar{V}_T} = \frac{1}{\sqrt{\bar{L} \cdot \bar{W}}} \cdot \frac{(2.59 \times 10^{-12})^{0.5}}{\bar{V}_T} \quad (2.67)$$

For the p-channel MOSFET device $Q_B = 4.810 \times 10^{-8} \text{ C / cm}^2$, Q_f is negligible, $A_{ox} = 6.4631 \times 10^{-14} \text{ cm}^2$ and $q = 16.019 \times 10^{-10} \text{ Coulombs}$, therefor, the standard deviation of the p-channel threshold voltage will be equal to:

$$\frac{\sigma_{V_T}}{\bar{V}_T} = \frac{1}{\sqrt{\bar{L} \cdot \bar{W}}} \cdot \frac{(9.89 \times 10^{-12})^{0.5}}{\bar{V}_T} \quad (2.68)$$

The numerical coefficient in eqn.(2.68) is greater than the unity in eqn.(2.67), which indicates larger threshold voltage mismatch in p-channel device. The physical explanation is that, there is larger variation in surface charge concentration due to the differential doping occurrence at the MOSFET channel surface.

For the MOSFET p and n-channel models given in this research that has the minimum dimension of $3 \mu\text{m}$ of both L and W , the variance in threshold voltage (σ_{V_T}) will be around 5.3 mV for n-channel MOSFET, while for the p-channel MOSFET it is 10.4 mV . The percent variation in the threshold voltage is 0.75% for the n-channel device and 1.3% for the p-channel device. The mismatch in threshold voltage can be summarized as follows:

- (a) The standard deviation of mismatch in threshold voltage is inversely proportional to the square root of the effective channel area.

- (b) The fixed oxide charge Q_f has negligible effect on the threshold voltage mismatch because the number of fixed oxide charges in well-controlled process can be reduced to about $2 \times 10^{10}/\text{cm}^2$. Then when we compare the value of Q_f and Q_B we may interfere the contribution of the variability of the fixed oxide charges to threshold voltage mismatch in eqn. (2.66) may be neglected
- (c) A major effect on threshold voltage mismatch comes from the nonuniform distribution of the dopant atom in the depletion charge at the bulk Q_B .
- (d) There is little influence on the threshold voltage mismatch due to gate oxide capacitance because it is quite uniform.

The drain current mismatch can be evaluated for the model given in this research depending on the drain current variance given in eqn. (2.55).

For the NMOS device, the variance in the drain current can be found by plugging the values of the transconductance parameters which was found before equal to 9.2345×10^{-5} and the threshold voltage variance which defined in eqn. (2.67) will be equal to 5.873×10^{-5}

The MOSFET size used in this design has $W = L = 3 \mu\text{m}$, the corresponding gate-to-source voltage is 1.25 volts and the average threshold voltage is assumed to be 0.7 volts. Substituting these values and the variance of the threshold voltage and transconductance into eqn. (2.55), the variance in drain current will be 46.52×10^{-5} and the standard deviation will be 2.16×10^{-3} , i.e. it is 0.216%. For the p-channel device, the variance in drain current will be found by the same way under the assumption of the threshold voltage equal to 0.8 volts. Then the variance will be 23.04×10^{-4} and the standard deviation become 48×10^{-3} or it can be defined as 4.8%.

For NCMOS type Ia current mirrors the worst case variation in output current is

$$\frac{\sigma_{I_o}^2}{I_o^2} = \frac{\sigma_{K_n}^2}{K_n^2} + \frac{\sigma_{K_p}^2}{K_p^2} + 4 \cdot \frac{\sigma_{(V_{GSn}-V_{Tn})}^2}{(V_{GSn}-V_{Tn})^2} + 4 \cdot \frac{\sigma_{(V_{GSp}-V_{Tp})}^2}{(V_{GSp}-V_{Tp})^2}$$

Substituting the values of each variable variation in the equation above for a reference current of 6 μ A and current gain grater than unity, will give a percent variation in output current of 1.36%. The NCMOS type Ib current mirror with reference current of 15 μ A, will give a percent variation in output current of 6.03% Table 2.4 shows the previous values tabulated.

Table 2.4: Statistical numbers showing the variations in currents of NCMOS current mirrors

parameter	max. value	comments
NMOS drain current variance $\sigma^2 I / \bar{I}^2$	46.52×10^{-5}	single NMOS 3 μ m drain current variance with $V_T=0.7$ and $V_{GS}=1.25$ volts
NMOS drain current standard deviation $\sigma I / \bar{I}$	2.16×10^{-3}	single NMOS 3 μ m drain current standard deviation with $V_T=0.7$ and $V_{GS}=1.25$ volts
PMOS drain current variance $\sigma^2 I / \bar{I}^2$	23.04×10^{-4}	single PMOS 3 μ m drain current variance with $V_T=0.8$ and $V_{GS}=1.25$ volts
PMOS drain current standard deviation $\sigma I / \bar{I}$	48×10^{-3}	single PMOS 3 μ m drain current standard deviation with $V_T=0.8$ and $V_{GS}=1.25$ volts
percent variation in threshold voltage V_{Tn} $\sigma V_{Tn} / V_{Tn} \%$	0.76%	single NMOS 3 μ m
percent variation in output current $\sigma I_o / \bar{I}_o \%$	1.36%	NCMOS current mirror with current gain greater than unity
percent variation in threshold voltage V_{Tp} $\sigma V_{Tp} / V_{Tp} \%$	1.31%	single PMOS 3 μ m
percent variation in output current $\sigma I_o / \bar{I}_o \%$	6.03%	NCMOS current mirror with current gain less than unity

As an example of comparison, the minimum masking error for the $1.2\ \mu\text{m}$ is 20%. If we need to design a current mirror with a current gain opportunity of 3.34 using the size factor and minimum size MOSFETs, then the error will be:

$$\frac{i_O}{i_R} = \frac{4 \pm 0.24}{1.2 \pm 0.24} = 3.34 \pm 0.73$$

This shows that the best case in the output current error of the conventional current mirror is 22% of the designed value. We conclude that for a minimum dimensions Type Ia NCMOS current mirror still better than the conventional current mirror by 20.5%. Fig. 2.41 shows the amount of area reduction in the NCMOS current mirror (a) in comparison with conventional current mirror (b) giving the same current gain of 3.34.

2.7.3 MONTE CARLO SIMULATION RESULTS

Simulations for worst case analysis was carried out using Monte Carlo package in HSPICE simulator for both NCMOS and conventional CM. The model for NCMOS CM was defined to skip the typical 20% maximum mask misalignment while it is applied to the conventional CM. A Monte Carlo program sample was shown in Appendix A, and the results for two NCMOS CM, controllable and noncontrollable compared with two conventional CM are given in Table 2.5. These results shows that the NCMOS CM, type Ia for input current level of $5\ \mu\text{A}$ has an output current standard deviation σ_{I_O}/\bar{I}_O percentage error equal to 1% of the simple conventional CM. Also the controllable type IVa has 15% of the conventional cascode with the same gain of 2.

Table 2.5: Monte Carlo Statistical results of the output current for a selected types of CM.

CM circuit	Type	σ_{I_O}	$VAR(I_O)$
Novel NCMOS CM	Ia	0.243×10^{-7}	5.93×10^{-14}
	IVa (cont.)	1.95×10^{-7}	3.806×10^{-14}
Conventional CM	simple	2.272×10^{-6}	5.160×10^{-12}
	cascode	1.283×10^{-6}	1.647×10^{-12}

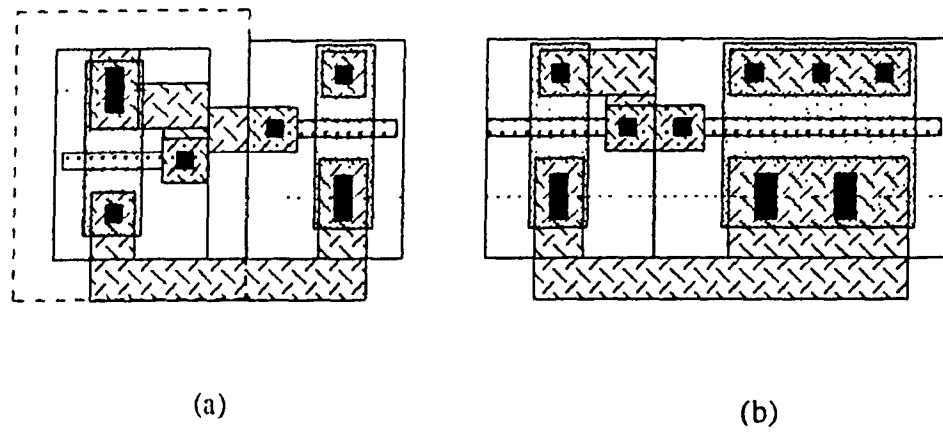


Fig 2.41
layout of (a) Type Ia NCMOS current mirror (b) conventional current mirror (for $K=3.34$)

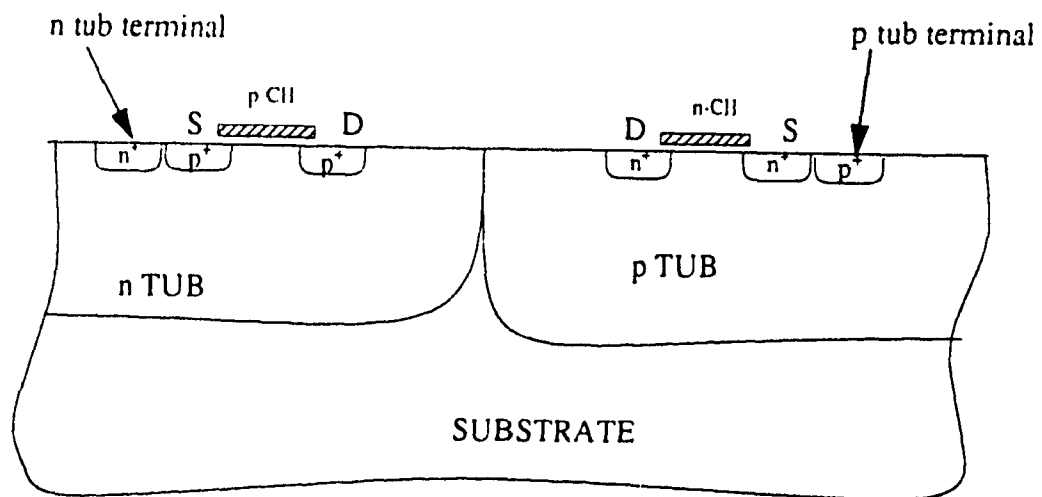


Fig. 2.42
Twin-tub CMOS structure[16].

2.8 IMPLEMENTATION TECHNIQUE

In all the current mirror configurations suggested in this chapter, the body of the MOSFET is always connected to its source terminal. Thus it is necessary to form a separate well for each MOSFET. The twin-tub technique allows separate wells for NMOS and PMOS transistors in a lightly doped substrate. The corresponding device structure for the two different MOSFETs is shown in Fig. 2.42 in which the substrate can be either n - or p -type. The original claim for this structure was that doping profiles in each well could be set independently; hence both device types would be optimized. The major advantage of the twin-tub approach is the flexibility of selecting substrate type (n or p) with no effect on transistor performance; the latch-up behavior however, will not be identical. This flexibility may be important in implementing design with different applications. Consequently, spacing between NMOS and PMOS devices can be reduced for high density circuits. As CMOS technology advances to submicron dimensions, the twin-tub approach may become more attractive. This is because the two device types perform similarly in the half micron regime. Thus it makes sense to provide symmetric NMOS and PMOS devices. Because the doping concentration will be scaled up at these dimensions anyway, whether devices are made in the well or in the substrate makes only a marginal difference[4, 16].

2.9 SUMMARY

The analysis and simulation of the twelve new current mirror circuits proposed circuits in this chapter have established a methodology of using the K - factor in designing a NCMOS current mirror. This methodology allows design of these NCMOS current mirrors with equal size MOSFETs and, consequently, with a minimum area. The area saving is 25% when compared to the regular current mirror with the same current gain. Further, the designs are portable for any VLSI implementation technology, present or

future i.e., they are valid for any VLSI technology. The designs also employ negative feedback profitably to improve the current ratio stability of the current mirror circuits.

Negative feedback was applied to most of the circuits to eliminate the effect of the output voltage variation on the current ratio, which makes it more stable with respect to the load variations. A quick review of the final current ratio equations of the twelve current mirrors is given in Table 2.1.

Results of analysis and simulation have shown that these circuits also provide a good stability with respect to the variation of the reference current. However, modifications have been proposed to further improve the performance of these circuits.

(1) The current ratio variations with respect to the reference current derived from the equations in Table 2.1 are given in two sets of graphs as shown in Fig.2.15 and Fig.2.16.

(2) The current ratio variation with the reference current, according to the HSPICE simulator results are given in two sets of graphs, Fig. 2.17 and Fig. 2.18. HSPICE simulation curves for the twelve current mirrors and the corresponding analytically evaluated curves are almost the same at small reference currents, while the difference starts to increase at higher levels of reference current because the MOSFET model used in the HSPICE simulator differs slightly from the one used in this thesis. The HSPICE programs along with the tables of results for each circuit are given in Appendix A.

(3) Finally the graphs from Fig.2.29 to Fig.2.40 show the stability curves of each NCMOS current mirror derived from both the analysis and the HSPICE simulator, to facilitate an improved visual comparison.

The output impedance analysis and calculations show that the last six NCMOS current mirrors are superior to the first six NCMOS current mirrors because of their output

stage designs. These output stages do not have any MOSFET connected in a diode form. A set of numerical results given in Table 2.6 shows the last six NCMOS current mirrors have output impedances in the range of 43.84 M Ω to 297.16 M Ω , while for the first six NCMOS current mirrors, the range of output impedances lies between 2 M Ω and 18.79 M Ω , for the reference current range of 5 μ A to 15 μ A as a worst case situation.

A statistical study has been done to calculate the errors in output current of the NCMOS current mirrors caused by a time independent random difference in the parameters of the MOSFET devices. The two most important time independent parameters (transconductance and threshold voltage) have been selected for this study. This study shows that the percentage error in the output current of the NCMOS current mirrors with a current gain greater than unity is higher than the one with a current gain less than unity, due to device type and the K factor ratio of the NCMOS current mirrors. The maximum percentage error in the output current due to device mismatch is approximately 6.03% and

Table2.6: Numerical comparison of the current mirrors for a typical case.

C.M. type	reference current level	output impedance	output offset voltage	K factor ratio	$\left 1 - \frac{I_o}{K I_{ref}}\right _{max}$; 100%	No.of transistors
Type Ia	5 μ A	2 M Ω	1.01 V	3.34	30%	2
Type Ib	15 μ A	5.33 M Ω	0.51 V	0.3	0%	2
Type IIa	15 μ A	18.79 M Ω	1.99 V	0.3	20%	3
Type IIb	5 μ A	5.67 M Ω	3.1 V	3.34	13%	3
Type IIIa	15 μ A	18.79 M Ω	1.99 V	0.3	19%	4
Type IIIb	5 μ A	5.67 M Ω	3.1 V	3.34	18%	4

C.M. type	reference current level	output impedance	output offset voltage	K factor ratio	$\left 1 - \frac{I_o}{K I_{ref}}\right _{max}$ 100%	No.of transis tors
Type IVa	5 μ A	106.7 M Ω	2.0 V	3.34	19%	4
Type IVb	15 μ A	157.6 M Ω	1.56 V	0.3	19%	4
Type V	5 μ A	106.7 M Ω	3.89 V	3.34	21%	4
Type VI	15 μ A	297.2 M Ω	3.61 V	0.3	16%	4
Type VII	15 μ A	159.7 M Ω	3.13 V	0.3	16%	4
Type VIII	5 μ A	43.84 M Ω	3.46 V	3.34	14%	4

1.36% for NCMOS current mirrors with gains less than unity and greater than unity, respectively. The worst case variation due to device mismatch (i.e. 6.03%) is still 16% less than the error caused by the only misalignment of a conventional current mirror giving the same gain and minimum required area. A Monte Carlo simulation shows that the NCMOS CM, type Ia for input current level of 5 μ A has an output current standard deviation $\sigma I_o / \bar{I}_o$ percentage error equal to 1% of the simple conventional CM. Also the controllable type IVa has 15% of the conventional cascode with the same gain of 2.

VLSI implementation technique suggested for this NCMOS current mirror circuits design is the twin tub technique. This technique illustrated in Fig. 2.43, has been used by the AT&T Bell Laboratories[4].

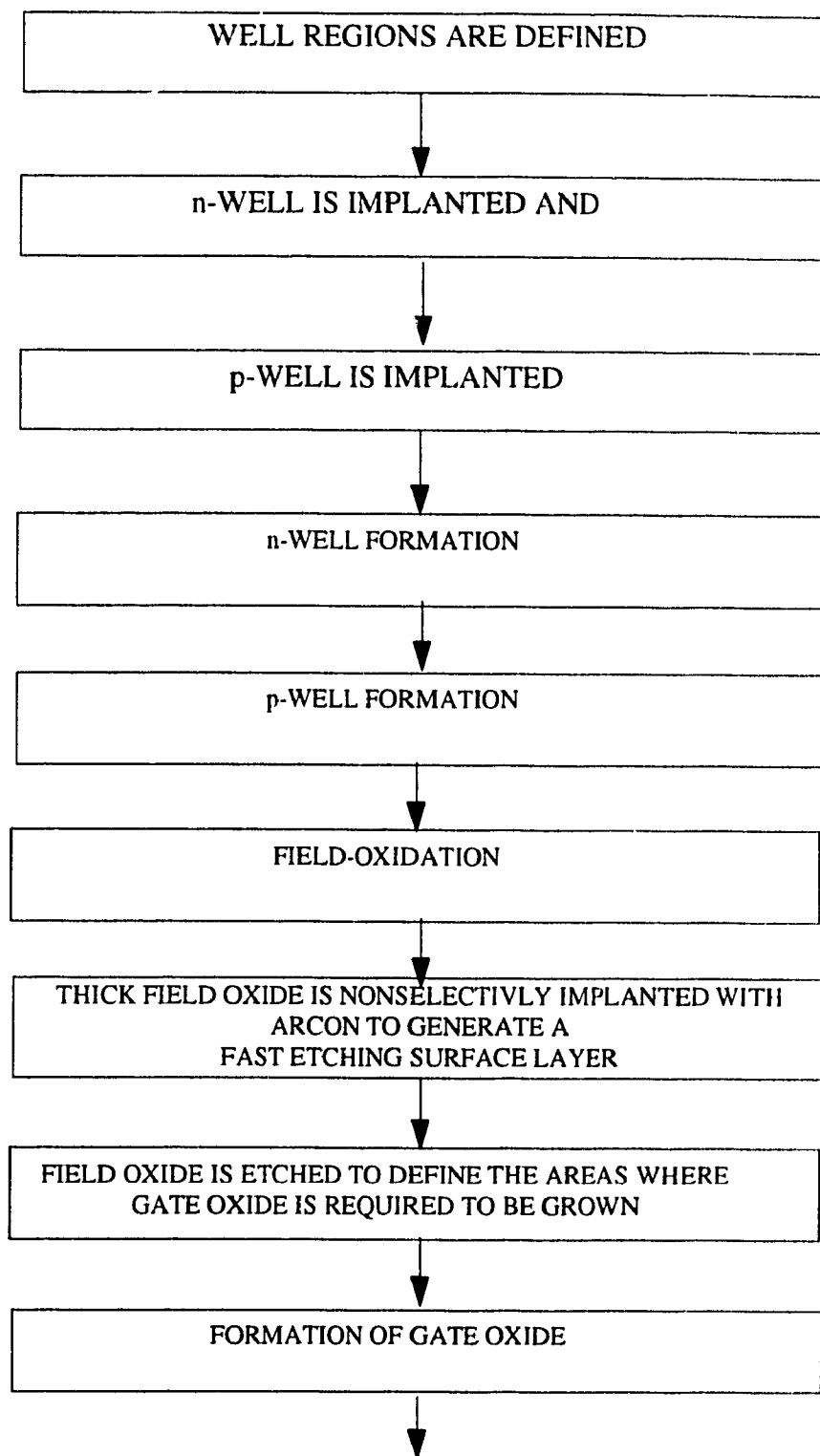


Fig. 2.43

AT&T Bell Laboratories twin-tub CMOS process steps[4]

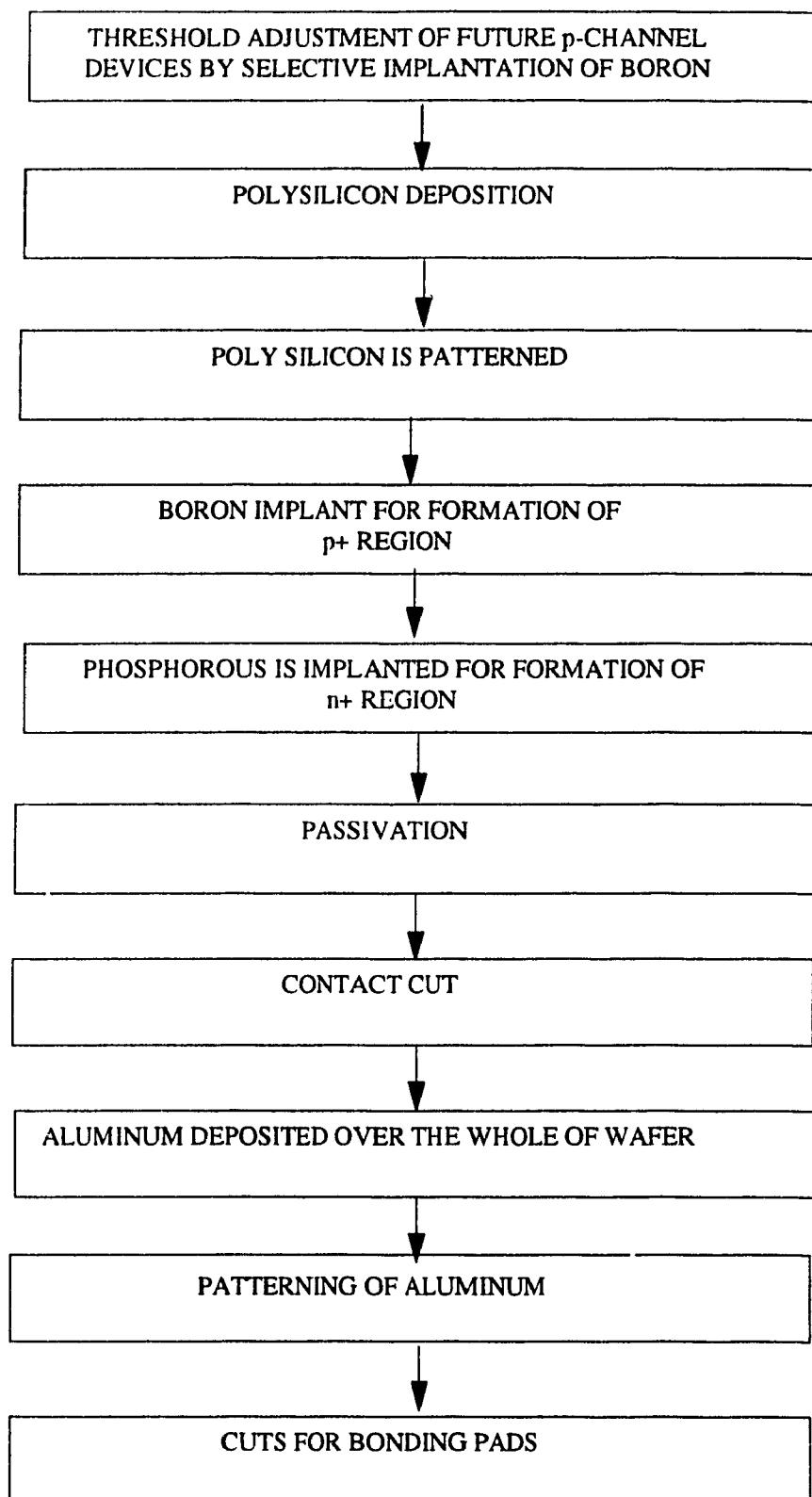


Fig. 2.43 (continued)

CHAPTER 3

VOLTAGE CONTROL OF CURRENT TRANSFER RATIO

3.0 GENERAL

The NCMOS current mirrors developed in Chapter 2 realize a fixed current ratio of K or $1/K$. By cascading n such current mirrors, a ratio of K^n or K^{-n} can be obtained, as shown in Fig.3.1. For an area comparison if $n=2$ and $K=3.34$ then the current ratio will be 10. If we use type Ia and type IIb to get this gain the total MOSFETs are 5. Rough area estimation, depending on the MOSFET gate size, the total area will be $5 \times 3^2 = 45 \mu\text{m}^2$. The conventional size technique using regular current mirror will cost an area of $11 \times 3^2 = 99 \mu\text{m}^2$. This rough estimation shows that an area reduction of 55% has been achieved. The parallel combination of output MOSFETs can give a current ratio increase of nK . It is desirable, however, to have a technique of continuous voltage control of the current ratio. In this chapter such a technique will be investigated in detail.

3.1 VOLTAGE CONTROL OF CURRENT TRANSFER RATIO

We have observed in Chapter 2 that for any current mirror the output current can be expressed as a function of the reference voltage across one of the reference side transistors. Let us call this transistor Q_R . The value of the reference voltage depends on the amount of the current that flows through the Q_R transistor. Thus, if we can control this current through the transistor Q_R , which develops the reference voltage V_R , while keeping I_R at a constant level, the output current can be correspondingly controlled without changing I_R . The block diagram on Fig.3.2 shows how this control circuit can be effected by a voltage. Clearly, I_c can be controlled by V_c and since:

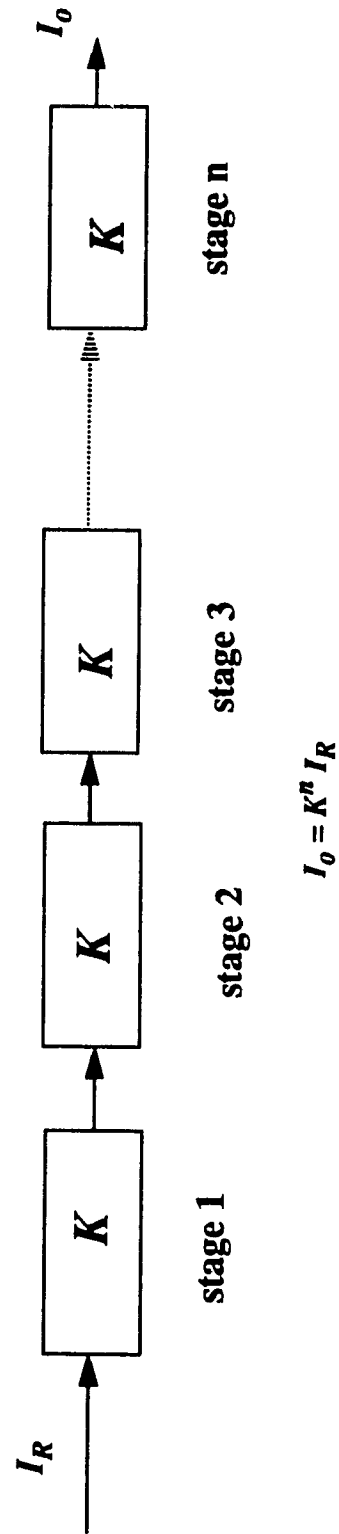


Fig. 3.1
current mirror coupling technique

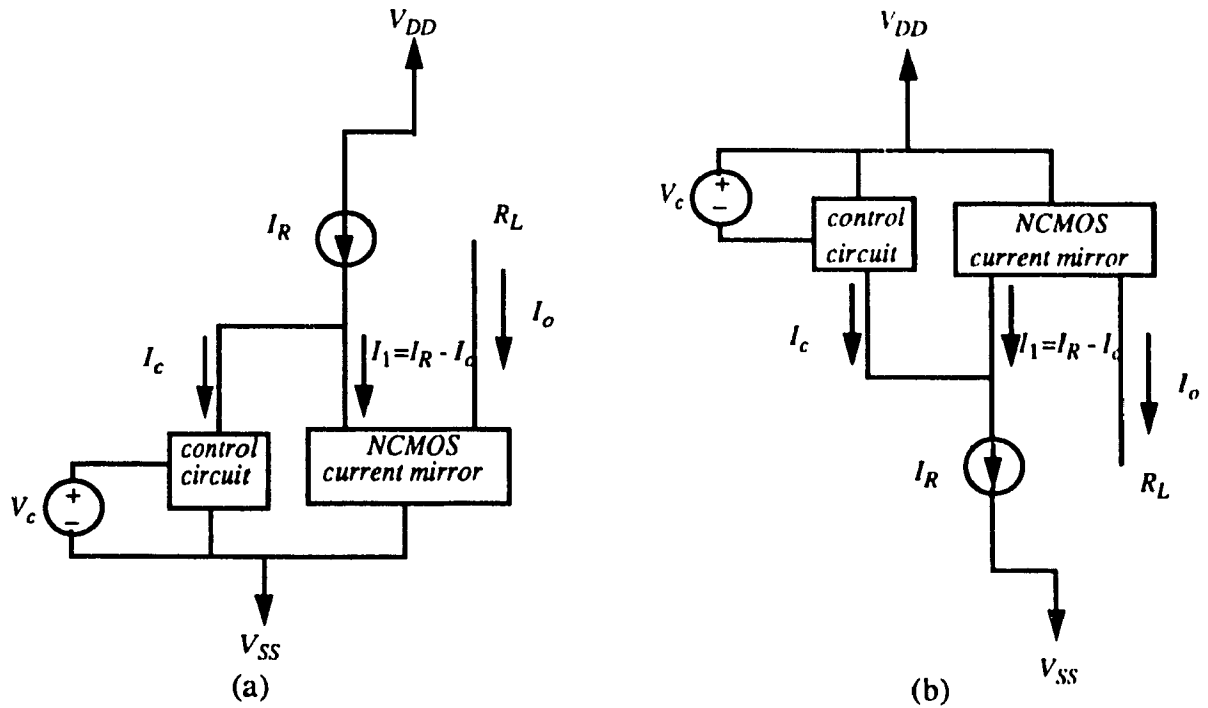


Fig.3.2

Voltage control of the current ratio.

(a) current sink (b) current source

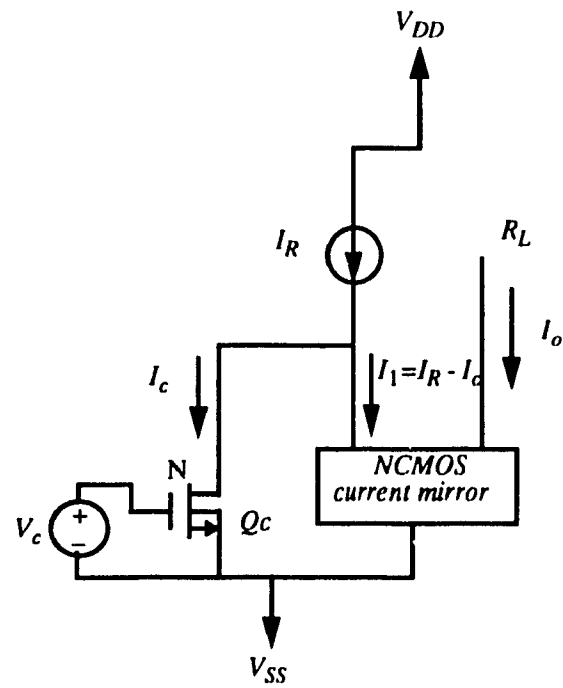


Fig.3.3

The voltage controlled current mirror sink with the control circuit shown.

$$I_c = I_R - I_1$$

Since the current I_R is a DC constant current, then it is true to say:

$$\Delta I_c = -\Delta I_1$$

Because the basic gain of a NCMOS current mirror equal to K , then

$$\frac{\Delta I_o}{\Delta I_c} = -K$$

This means that the output current is linearly (inversely) dependent on the control current I_c [17], or I_o can be made dependent on the control voltage V_c .

Fig.3.3 shows a simple control circuit for any of the sink model of the NCMOS current mirrors developed in Chapter 2. Assume this NCMOS current mirror has a current gain greater than unity. Obviously, the transistor Q_R in this case is an NMOS transistor. The voltage across its gate-source terminals is equal to V_R .

The analysis for this voltage controlled NCMOS current mirror will be as follows:

For control transistor Q_c the current is:

$$I_c = \beta_c \cdot (V_c - V_{Tn})^2 \cdot (1 + \lambda_n V_{DSC}) \quad (3.1)$$

The reference side MOSFET transistor of the NCMOS current mirror has a current equal to:

$$I_R - I_c = \beta_R \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (3.2)$$

Summing equations (3.1) and (3.2) and assuming $\beta_c = \beta_R$, the reference current becomes:

$$I_R = \beta_R \cdot ((V_c - V_{Tn})^2 \cdot (1 + \lambda_n V_{DSC}) + (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R)) \quad (3.3)$$

Assuming $\lambda_n V_{DSC} \ll 1$ and $\lambda_n V_R \ll 1$, we have from eqn. (3.3)

$$(V_R - V_{Tn})^2 = \frac{I_R}{\beta_R} - (V_c - V_{Tn})^2 \quad (3.4)$$

From equation (3.4) it is clear that the voltage V_R is a decreasing function of the voltage V_c . Thus, the value of V_R can be controlled by the voltage V_c . The output current I_o is developed by impressing V_R across a transistor, say, Q_o , on the output side of the current mirror. Hence, we have for I_o ,

$$I_o = \beta_o \cdot (V_R - V_{To})^2 \cdot (1 + \lambda_o V_{DSO}) \quad (3.5)$$

where β_o , V_{To} , λ_o and V_{DSO} refer to appropriate quantities for Q_o .

Dividing eqn. (3.5) by eqn. (3.3) will give a current ratio:

$$\frac{I_o}{I_R} = \frac{\beta_o}{\beta_R} \cdot \frac{(V_R - V_{To})^2}{(V_c - V_{Tn})^2 + (V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_o V_{DSO})}{(1 + \lambda_n V_R)} \quad (3.6)$$

Even eqn. (3.6) is a nonlinear equation, it shows that the current ratio is a decreasing function of the DC control voltage V_c . A similar equation can be developed for the source version of the NCMOS current mirror. This non-linearity is not important because the control voltage is an external DC voltage.

3.2 VOLTAGE CONTROLLED NCMOS CURRENT MIRRORS.

The above voltage control technique has been applied to all the NCMOS current mirrors. The DC analyses have been done for all of these circuits. The appropriate expressions are given in Table 3.1 and Table 3.2. Corresponding control curves for all the current mirrors are given in Fig. 3.4 and Fig. 3.5. However only, four circuits have been selected for presentation of the detailed analysis. Analysis and simulation results shows that these four circuits offer superior control characteristics relative to the other types. These circuits are:

Table 3.1: Summary of the analysis results for the controlled current mirrors.

NCMOS current mirror type	Current gain (I_O / I_R)	Comments
Ia	$\frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_{ds2})}{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R) + \frac{K_n}{K_p} \cdot (V_c - V_{Tn})^2 \cdot (1 + \lambda_n V_R)}$	i) For a given I_R and V_c , the voltage V_R can be obtained from Table 3.2. ii) V_{cmax} can be obtained from Table 3.2 using computer programming.
Ib	$\frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_{sd2})}{(V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) + \frac{K_p}{K_n} \cdot (V_c - V_{Tp})^2 \cdot (1 + \lambda_p V_R)}$	i) For a given I_R and V_c , the voltage V_R can be obtained from Table 3.2. ii) V_{cmax} can be obtained from Table 3.2 using computer programming.
IIa	$\frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R)}{((V_R - V_{Tn})^2 + (V_c - V_{Tn})^2) \cdot \left(1 + \lambda_n \left(V_R \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)}$	i) For a given I_R and V_c , the voltage V_R can be obtained from Table 3.2. ii) V_{cmax} can be obtained from Table 3.2 using computer programming.
IIb	$\frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R)}{((V_R - V_{Tp})^2 + (V_c - V_{Tp})^2) \cdot \left(1 + \lambda_p \left(V_R \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{Tp} \sqrt{\frac{K_n}{K_p}} + V_{Tn}\right)\right)}$	i) For a given I_R and V_c , the voltage V_R can be obtained from Table 3.2. ii) V_{cmax} can be obtained from Table 3.2 using computer programming.
IIIa	$\frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R)}{((V_R - V_{Tn})^2 + (V_c - V_{Tn})^2) \cdot \left(1 + \lambda_n \left((V_R - V_{Tp}) \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right)}$	i) For a given I_R and V_c , the voltage V_R can be obtained from Table 3.2. ii) V_{cmax} can be obtained from Table 3.2 using computer programming.

NCMOS current mirror type	Current gain (I_O / I_R)	Comments
IIIb	$\frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R)}{(V_R - V_{Tn})^2 + (V_c - V_{Tp})^2 \cdot (1 + \lambda_p ((V_R - V_{Tp}) \sqrt{\frac{K_n}{K_p}} + V_{Tn}))}$	<p>i) For a given I_R and V_c, the voltage V_R can be obtained from Table 3.2.</p> <p>ii) V_{cmax} can be obtained from Table 3.2 using computer programing.</p>
IVa	$\frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R)}{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R) + \frac{K_n}{K_p} (V_c - V_{Tn})^2 \cdot (1 + 2\lambda_n V_R)}$	<p>i) For a given I_R and V_c, the voltage V_R can be obtained from Table 3.2.</p> <p>ii) V_{cmax} can be obtained from Table 3.2 using computer programing.</p>
IVb	$\frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R)}{(V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) + \frac{K_p}{K_n} (V_c - V_{Tn})^2 \cdot (1 + 2\lambda_p V_R)}$	<p>i) For a given I_R and V_c, the voltage V_R can be obtained from Table 3.2.</p> <p>ii) V_{cmax} can be obtained from Table 3.2 using computer programing.</p>
V	$\frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2 + \frac{K_n}{K_p} (V_c - V_{Tn})^2} \cdot \frac{(1 + \lambda_n (V_R (1 + \sqrt{\frac{K_p}{K_n}}) - V_{Tp} \sqrt{\frac{K_p}{K_n}} + V_{Tn}))}{(1 + \lambda_p V_R)}$	<p>i) For a given I_R and V_c, the voltage V_R can be obtained from Table 3.2.</p> <p>ii) V_{cmax} can be obtained from Table 3.2 using computer programing.</p>
VI	$\frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p 2V_R)}{(V_c - V_{Tn})^2 \left(1 + \lambda_n \left(V_R \left(2 + \sqrt{\frac{K_p}{K_n}} \right) - V_{Tp} \sqrt{\frac{K_p}{K_n}} + V_{Tn} \right) \right) + (V_R - V_{Tn})^2 (1 + \lambda_n V_R)}$	<p>i) For a given I_R and V_c, the voltage V_R can be obtained from Table 3.2.</p> <p>ii) V_{cmax} can be obtained from Table 3.2 using computer programing.</p>

NCMOS current mirror type	Current gain (I_O / I_R)	Comments
VII	$\frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2 \cdot (1 + 2\lambda_n V_R)}{(V_R - V_{Tp})^2 (1 + \lambda_p V_R) + \frac{(V_c - V_{Tp})^2 (1 + \lambda_p (V_R (2 + \sqrt{\frac{K_n}{K_p}}) - V_{Tn} \sqrt{\frac{K_n}{K_p}} + V_{Tp}))}{(V_R - V_{Tn})^2 (1 + \lambda_n V_R)}}$	<p>i) For a given I_R and V_c, the voltage V_R can be obtained from Table 3.2.</p> <p>ii) V_{cmax} can be obtained from Table 3.2 using computer programing.</p>
VIII	$\frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p (V_R + (\sqrt{\frac{K_n}{K_p}} \cdot (V_R - V_{Tn}) \cdot \alpha) + V_{Tp}))}{\frac{K_p}{K_n} (V_c - V_{Tn})^2 (1 + \lambda_p (2V_R + (\sqrt{\frac{K_n}{K_p}} (V_R - V_{Tn}) \alpha) + V_{Tp})) + \frac{(V_R - V_{Tn})^2 (1 + \lambda_n V_R)}{(V_R - V_{Tn})^2 (1 + \lambda_n V_R)}}$ $\alpha = \sqrt{(1 + \lambda_n V_R) / (1 + \lambda_p 2V_R)}$	<p>i) For a given I_R and V_c, the voltage V_R can be obtained from Table 3.2.</p> <p>ii) V_{cmax} can be obtained from Table 3.2 using computer programing.</p>

Table 3.2: Design equations for determination of V_R and V_{cmax}

NCMOS current mirror Type		(a) Equation to obtain V_R from a given I_R and V_c . (b) Equation to obtain V_{cmax} for a given I_R .
Type Ia	(a)	$V_R = \sqrt{\frac{2I_R}{K_p} - \frac{K_n}{K_p} (V_c - V_{Tn})^2} + V_{Tp}$
	(b)	$I_R = \frac{K_n}{2} (V_{Cmax} - V_{Tn})^2 + \frac{K_p}{2} \cdot (V_{Cmax} - V_{Tn} - V_{Tp})^2$
Type Ib	(a)	$V_R = \sqrt{\frac{2I_R}{K_n} - \frac{K_p}{K_n} (V_c - V_{Tp})^2} + V_{Tn}$
	(b)	$I_R = \frac{K_p}{2} \cdot (V_{Cmax} - V_{Tp})^2 + \frac{K_n}{2} \cdot (V_{Cmax} - V_{Tn} - V_{Tp})^2$
Type IIa	(a)	$V_R = \sqrt{\frac{2I_R}{K_n} - (V_c - V_{Tn})^2} + V_{Tn}$
	(b)	$I_R = \frac{K_n}{2} \cdot \left((V_{Cmax} - V_{Tn})^2 + \left(\frac{V_{Cmax} + V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} - V_{Tn} \right)^2 \right)$
Type IIb	(a)	$V_R = \sqrt{\frac{2I_R}{K_p} - (V_c - V_{Tp})^2} + V_{Tp}$
	(b)	$I_R = \frac{K_p}{2} \cdot \left((V_{Cmax} - V_{Tp})^2 + \left(\frac{V_{Cmax} + V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} - 2V_{Tp}}{2 + \sqrt{\frac{K_n}{K_p}}} - V_{Tp} \right)^2 \right)$

NCMOS current mirror Type		(a) Equation to obtain V_R from a given I_R and V_c . (b) Equation to obtain V_{cmax} for a given I_R .
Type IVb	(a) (b)	$V_R = \sqrt{\frac{2I_R}{K_n} - \frac{K_p}{K_n} (V_c - V_{Tp})^2} + V_{Tn}$ $I_R = \frac{K_p}{2} \cdot (V_{Cmax} - V_{Tp})^2 + \frac{K_n}{2} \cdot \left(\frac{V_{Cmax} - V_{Tp}}{2} - V_{Tn} \right)^2$
Type V	(a) (b)	$V_R = \sqrt{\frac{2I_R}{K_p} - \frac{K_n}{K_p} (V_c - V_{Tn})^2} + V_{Tp}$ $I_R = \frac{K_n}{2} \cdot (V_{Cmax} - V_{Tn})^2 + \frac{K_p}{2} \cdot \left(\frac{V_{Cmax} + V_{Tp} \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} - V_{Tp} \right)^2$
Type VI	(a) (b)	$V_R = \sqrt{\frac{2I_R}{K_n} - (V_c - V_{Tn})^2} + V_{Tn}$ $I_R = \frac{K_n}{2} \cdot (V_{Cmax} - V_{Tn})^2 + \frac{K_n}{2} \cdot \left(\frac{V_{Cmax} + V_{Tp} \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} - V_{Tn} \right)^2$

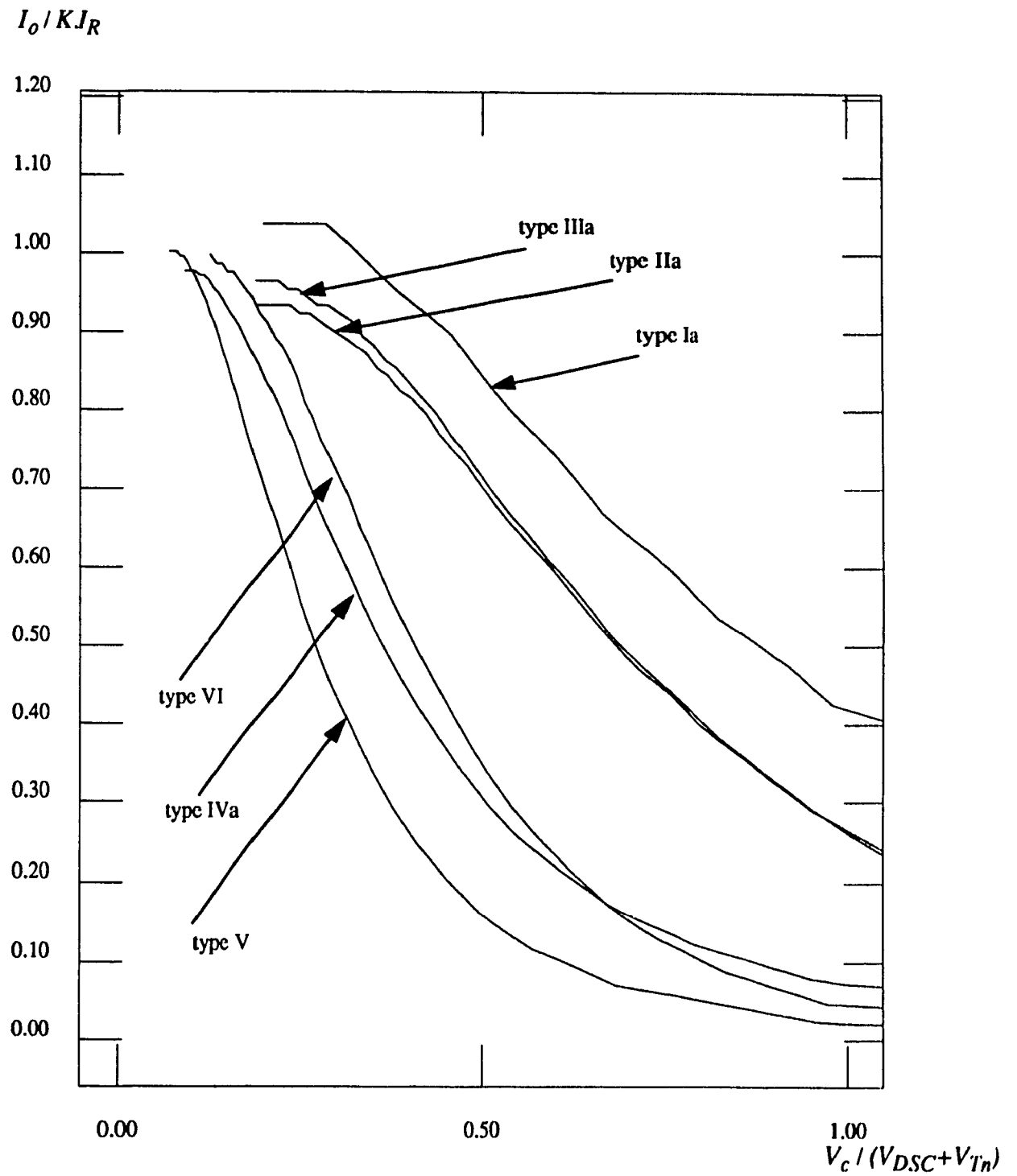


Fig. 3.4

Current ratio with control voltage variation for sink versions of the NCMOS current mirrors.

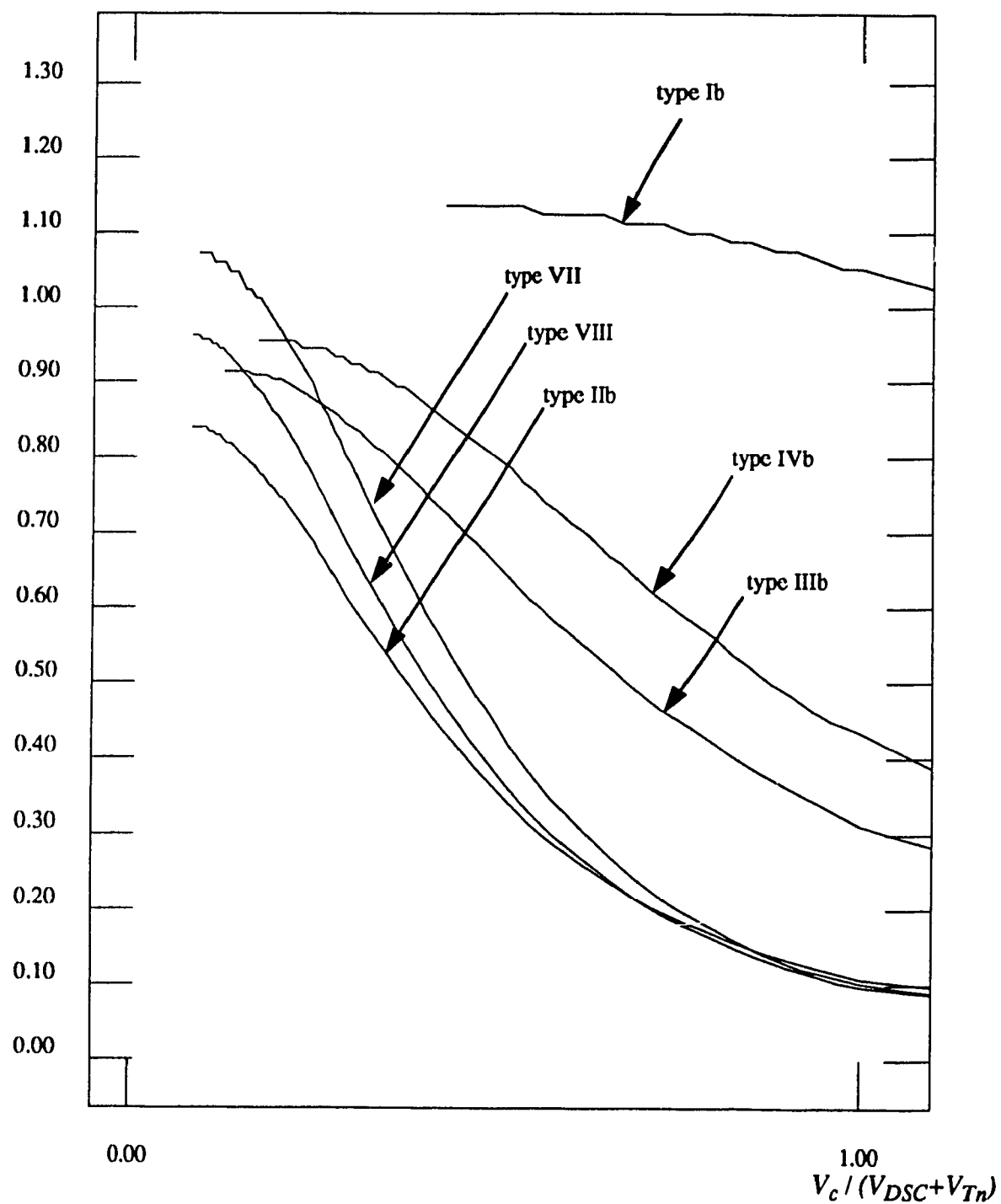
$I_o / K I_R$


Fig. 3.5

Current ratio with control voltage variation for source versions of the NCMOS current mirrors.

- (a) Type V sink with $K > 1$.
- (b) Type VI sink with $K < 1$.
- (c) Type IIb source with $K > 1$.
- (d) Type VIII source with $K < 1$.

3.2.1 VOLTAGE CONTROLLED TYPE V NCMOS CURRENT MIRROR

To control the output current of this type of NCMOS current mirror, an NMOS control transistor Q_c is connected across both Q_1 and Q_4 MOSFET transistors (which are located in the reference side of the current mirror) in order that Q_1 and Q_4 carry the same current through them as shown in the circuit diagram of Fig.3.6. The current I_c is the control current, while the current I_I is the adjustable current that flows through Q_1 and Q_4 . I_I is equal to the difference between the main reference current and the control current.

Referring to the circuit diagram of Fig.3.6, the V_{DSC} voltage of Q_c transistor is equal to the sum of V_{SD1} of the Q_1 transistor and V_{DS4} of the Q_4 transistor.

Referring to the analysis in Chapter 2, section 2.3, the voltage between the drain and the source of transistor Q_4 can be written as follows:

$$V_{DS4} = V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}} \right) - \left(V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} \right) + V_{Tn} \quad (3.7)$$

Since the voltage V_{SG1} was assumed to be the reference voltage V_R , then the drain to source voltage V_{DSC} of the control transistor Q_c will be:

$$V_{DSC} = V_{DS4} + V_{SG1} = V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}} \right) - \left(V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} \right) + V_{Tn} \quad (3.8)$$

The drain current I_c of the NMOS control transistor Q_c is:

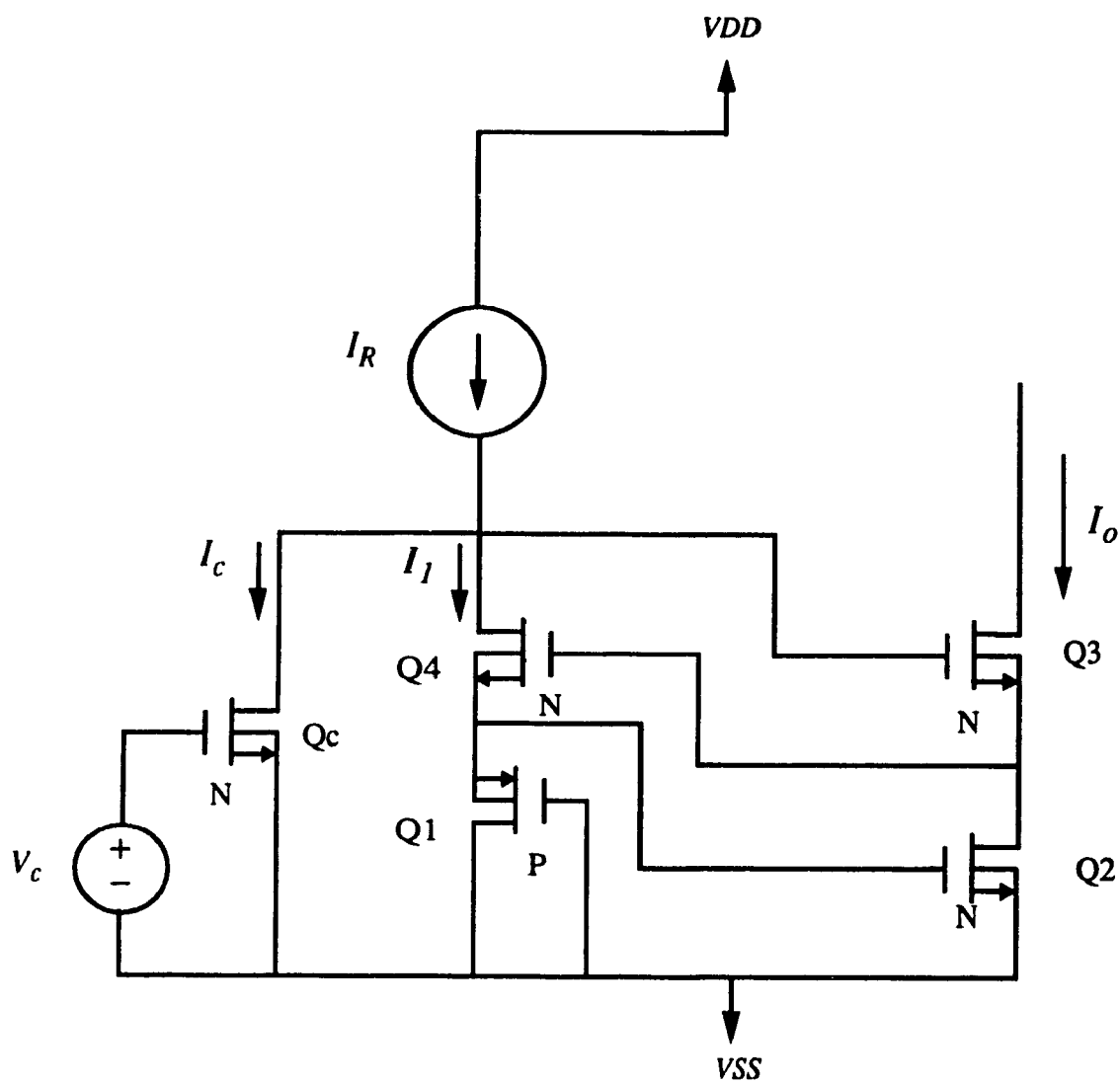


Fig. 3.6
Circuit diagram for Type V NCMOS current mirror, (sink version) with $K > 1$

$$I_c = \frac{K_n}{2} \cdot (V_c - V_{Tn})^2 \cdot \left(1 + \lambda_n \left(V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}} \right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn} \right) \right) \quad (3.9)$$

The source current I_1 of transistors Q_1 will be:

$$I_1 = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_R) \quad (3.10)$$

Because the factor $\left(2 + \sqrt{\frac{K_p}{K_n}} \right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn} \cong 2.81$ and $\lambda_p \cong 3\lambda_n$ one may assume,

$$\lambda_n \left(V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}} \right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn} \right) \approx \lambda_p V_R$$

Thus we have,

$$I_R = I_1 + I_c = \frac{K_p}{2} \cdot \left((V_R - V_{Tp})^2 + \frac{K_n}{K_p} \cdot (V_c - V_{Tn})^2 \right) \cdot (1 + \lambda_p V_R) \quad (3.11)$$

The previous equation shows that the reference current can be expressed in terms of two variables V_R and V_c , which means that, for a given I_R , V_R can be controlled by the voltage V_c . Equation(2.28) in Chapter 2 gives the output current as:

$$I_o = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot \left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}} \right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn} \right) \right) \quad (3.12)$$

Dividing equation (3.12) by equation (3.11) the following current ratio equation is obtained:

$$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2 + \frac{K_n}{K_p} \cdot (V_c - V_{Tn})^2} \cdot \frac{\left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}} \right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn} \right) \right)}{(1 + \lambda_p V_R)} \quad (3.13)$$

Assuming $\lambda_p V_R \ll 1$, we have from equation (3.11):

$$I_R = \frac{K_p}{2} \cdot \left((V_R - V_{Tp})^2 + \frac{K_n}{K_p} \cdot (V_c - V_{Tn})^2 \right) \quad (3.14)$$

The above equation shows that the voltage V_R is a decreasing function of the voltage V_c when the current I_R is held constant.

Rearranging equation (3.14), the reference voltage V_R can be written in terms of the reference current and the control voltage as shown below:

$$V_R = \sqrt{\frac{2I_R}{K_p} - \frac{K_n}{K_p} (V_c - V_{Tn})^2} + V_{Tp} \quad (3.15)$$

The above equation is valid when the control transistor Q_c stays in the saturation region, and this condition is valid when the voltage V_c is less or equal the sum of the drain-to-source voltage and the threshold voltage of the control transistor Q_c , i.e.:

$$\frac{V_c}{V_{DSC} + V_{Tn}} \leq 1 \quad (3.16)$$

Consequently, the maximum control voltage is:

$$V_{Cmax} = V_{DSC} + V_{Tn} = V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}} \right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + 2V_{Tn} \quad (3.17)$$

The value of reference voltage in terms of the maximum control voltage becomes:

$$V_R = \frac{V_{Cmax} + V_{Tp} \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} \quad (3.18)$$

The maximum control current that can be sunk through Q_c transistor while it is in saturation region is:

$$I_{Cmax} = \frac{K_n}{2} \cdot (V_{Cmax} - V_{Tn})^2 \quad (3.19)$$

Thus, the minimum value of the current I_1 through transistor Q_1 becomes:

$$I_1 = \frac{K_p}{2} \cdot \left(\frac{V_{Cmax} + V_{Tp} \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} - V_{Tp} \right)^2 \quad (3.20)$$

The reference current can also be written in terms of the maximum control voltage as follows:

$$I_R = \frac{K_n}{2} \cdot (V_{Cmax} - V_{Tn})^2 + \frac{K_p}{2} \cdot \left(\frac{V_{Cmax} + V_{Tp} \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} - V_{Tp} \right)^2 \quad (3.21)$$

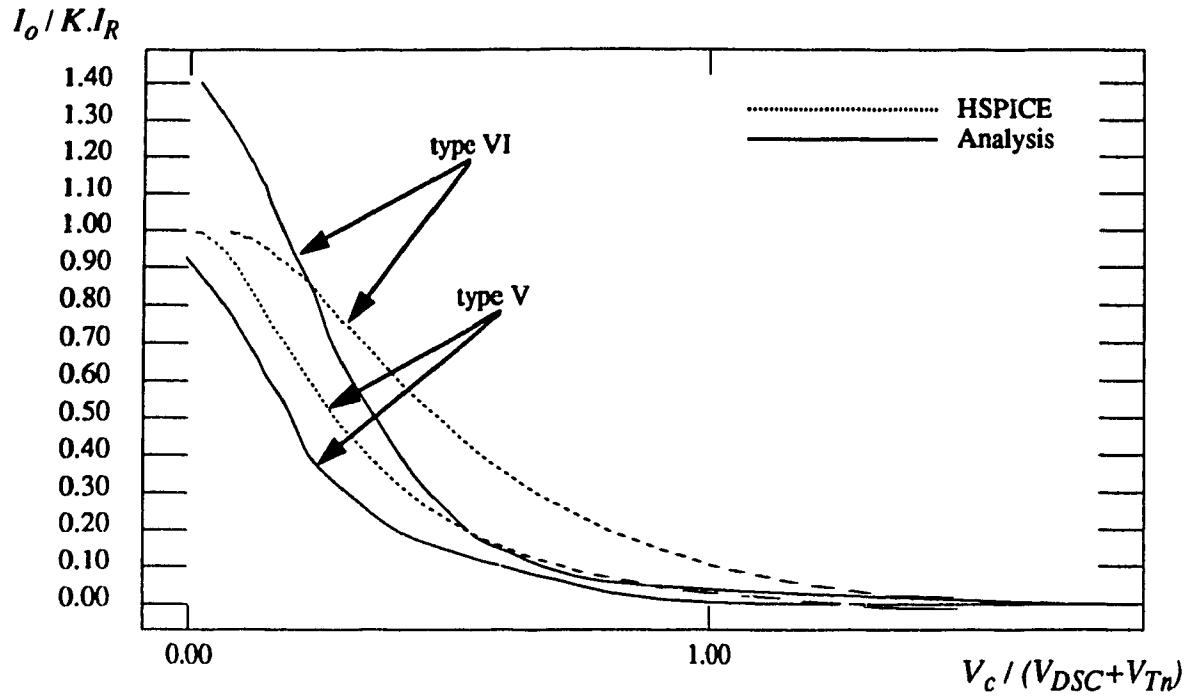
Solving eqn. (3.21), we can obtain V_{Cmax} for a given I_R . The above equation can be solved through the use of programming technique. The programs and simulations for this circuit are given in Appendix A. Relevant expressions are listed in Table 3.1 and Table 3.2. Fig.3.7 compares the analysis and HSPICE simulation results for two levels of reference current 40 μ A and 120 μ A.

3.2.2 VOLTAGE CONTROLLED TYPE VI NCMOS CURRENT MIRROR

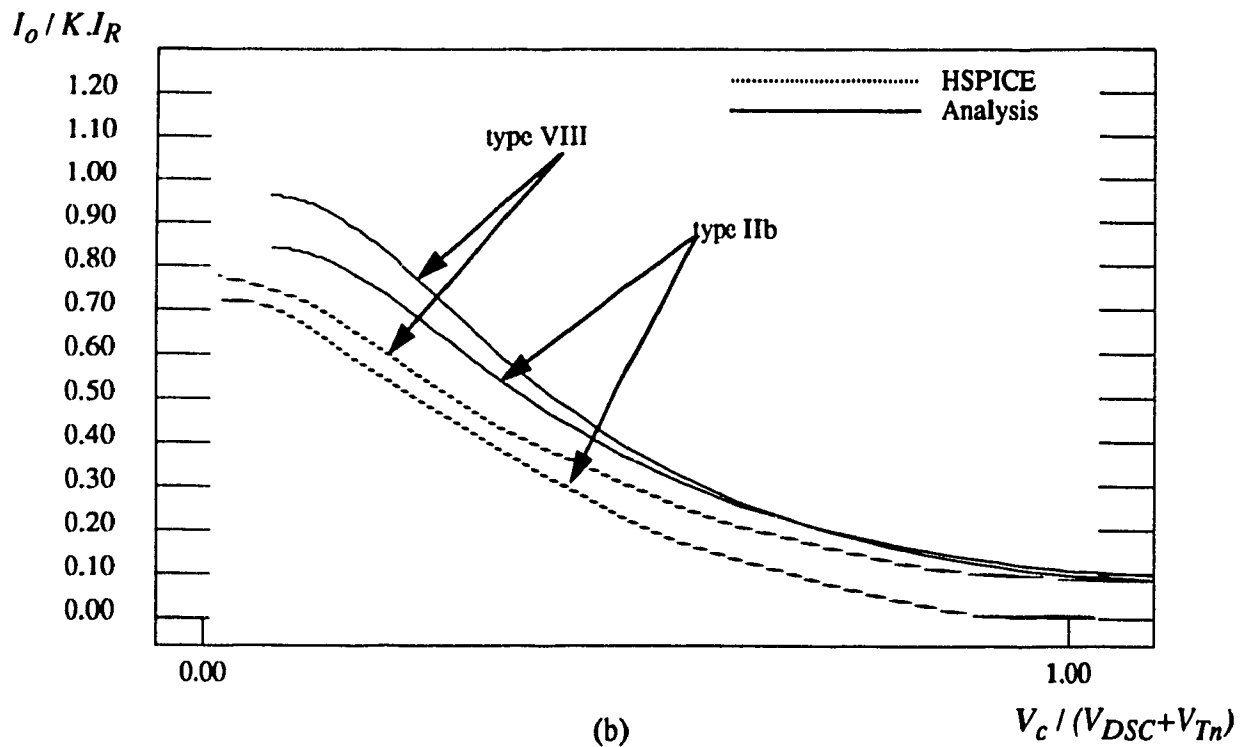
Fig.3.8 shows the complete circuit diagram for type VI voltage controlled NCMOS current mirror. From the circuit diagram of Fig.3.8 it is clear that the voltage V_{DSC} can be written as:

$$V_{DSC} = V_{DS4} + V_{SG1}$$

Referring to the analysis of type VI NCMOS current mirror in Appendix B, eqn.(B.15), the voltage V_{DSC} can be written in terms of the reference voltage V_R , which is the gate-to-source voltage of Q_4 transistor, as follows:



(a)



(b)

Fig. 3.7: Comparison between the HSPICE and Analysis (Table 3.1 & 3.2) results for (a) best NCMOS sink current mirrors (b) best NCMOS source current mirrors for the values of I_R given in page 159 and 161.

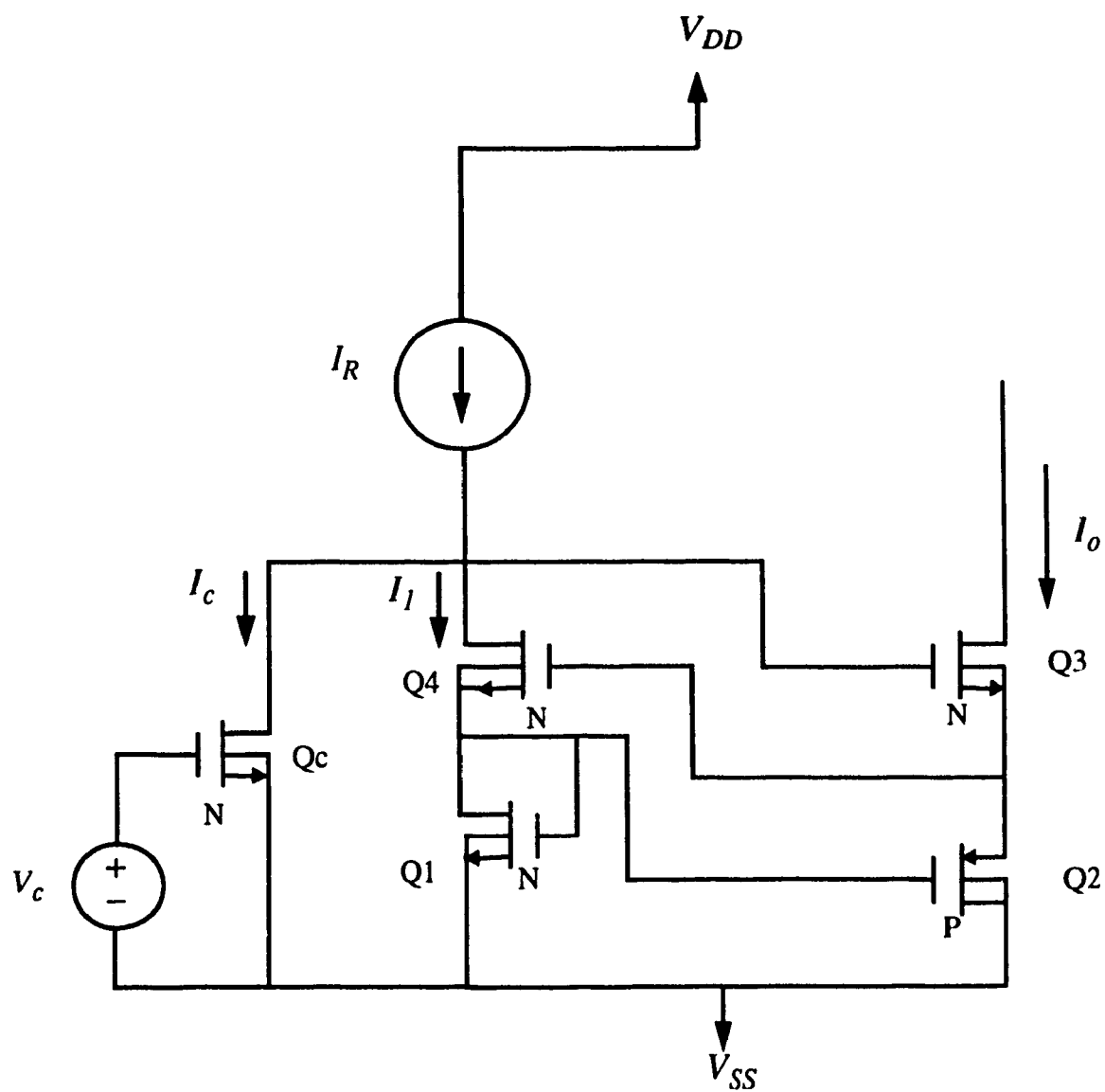


Fig. 3.8

Circuit diagram shows the control circuit connected to Type VI NCMOS current mirror.

$$V_{DSC} = V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}}\right) - \left(V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}}\right) + V_{Tn} \quad (3.22)$$

The amount of control current I_c that is going to pass through the control transistor Q_c can now be written as:

$$I_c = \frac{K_n}{2} \cdot (V_c - V_{Tn})^2 \cdot \left(1 + \lambda_n \left(V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right) \quad (3.23)$$

The current which passes through reference side of this NCMOS current mirror, I_1 , can be written in terms of transistor Q_1 parameter as follows:

$$I_1 = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (3.24)$$

Since the reference current I_R is the sum of both currents I_c and I_1 , it can be written in the following form:

$$I_R = \frac{K_n}{2} \cdot (V_c - V_{Tn})^2 \cdot \left(1 + \lambda_n \left(V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn}\right)\right) + \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (3.25)$$

The output current of this NCMOS current mirror was given in Appendix B, eqn. (B.17) as follows:

$$I_o = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p 2V_R) \quad (3.26)$$

Dividing eqn. (3.26) by eqn. (3.25), will result in a current ratio for the controlled NCMOS current mirror as in the following equation:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2 \cdot (1 + \lambda_p 2V_R)}{(V_c - V_{Tn})^2 \cdot (1 + \lambda_n (V_R \cdot (2 + \sqrt{\frac{K_p}{K_n}}) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn})) + (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R)} \quad (3.27)$$

Rearranging eqn. (3.25), it is possible to put the reference voltage as a function of the reference current and the control voltage, which will be valid only when the control transistor is in the saturation region, i.e.,

$$V_R = \sqrt{\frac{2I_R}{K_n} - (V_c - V_{Tn})^2} + V_{Tn} \quad (3.28)$$

The control MOSFET Q_c will be in the saturation region if the following equation is valid:

$$\frac{V_c}{V_{DSC} + V_{Tn}} \leq 1 \quad (3.29)$$

This means that the maximum control voltage will be:

$$V_{Cmax} = V_{DSC} + V_{Tn} = V_R \cdot \left(2 + \sqrt{\frac{K_p}{K_n}}\right) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + 2V_{Tn} \quad (3.30)$$

By arranging the previous equation, the reference voltage can be written in terms of the maximum control voltage as follows:

$$V_R = \frac{V_{Cmax} + V_{Tp} \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} \quad (3.31)$$

For each value of reference current there is a maximum control voltage, above which the control MOSFET will start working in the active region i.e. the previous derivations will not be valid. The following equation specifies the required maximum control voltage.

$$I_R = \frac{K_n}{2} \cdot (V_{Cmax} - V_{Tn})^2 + \frac{K_n}{2} \cdot \left(\frac{V_{Cmax} + V_{Tp} \sqrt{\frac{K_p}{K_n}} - 2V_{Tn}}{2 + \sqrt{\frac{K_p}{K_n}}} - V_{Tn} \right)^2 \quad (3.32)$$

To find the value of the maximum control voltage that is required for any reference current level, it is possible to solve eqn. (3.32) through a nonlinear computer programming. The solution programs are given in the Appendix A. Relevant expressions are listed in Table 3.1 and Table 3.2. Fig.3.7 compares the analysis and simulation results.

3.2.3 VOLTAGE CONTROLLED TYPE IIb NCMOS CURRENT MIRROR

Type IIb NCMOS current mirror (source version) can be controlled through the connection of a control PMOS transistor Q_c in parallel with the reference PMOS transistor Q_I of this NCMOS current mirror as shown in Fig.3.9.

The PMOS transistor Q_c will inject an amount of current that depends on the value of the control voltage V_c , and because the reference current is constant, it is going to be shared between the I_c of the Q_c transistor and I_I of the Q_I transistor. Thus any increase in the control current I_c will cause a reduction in the current I_I and this will reflect as a reduction in the output current I_O .

Since the source-to-drain voltage V_{SDC} of Q_c transistor is equal to the source-to-drain voltage V_{SDI} of Q_I transistor and by referring to eqn. (B.5) in Appendix B, the control current can be written as follows:

$$I_c = \frac{K_p}{2} \cdot (V_c - V_{Tp})^2 \cdot (1 + \lambda_p V_{SDI}) \quad (3.33)$$

The voltage $V_{sdc} = V_{sdl}$ can be written as follows:

$$V_{SDC} = V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - \left(V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}}\right) + V_{Tp}$$

The current I_I through transistor Q_I is:

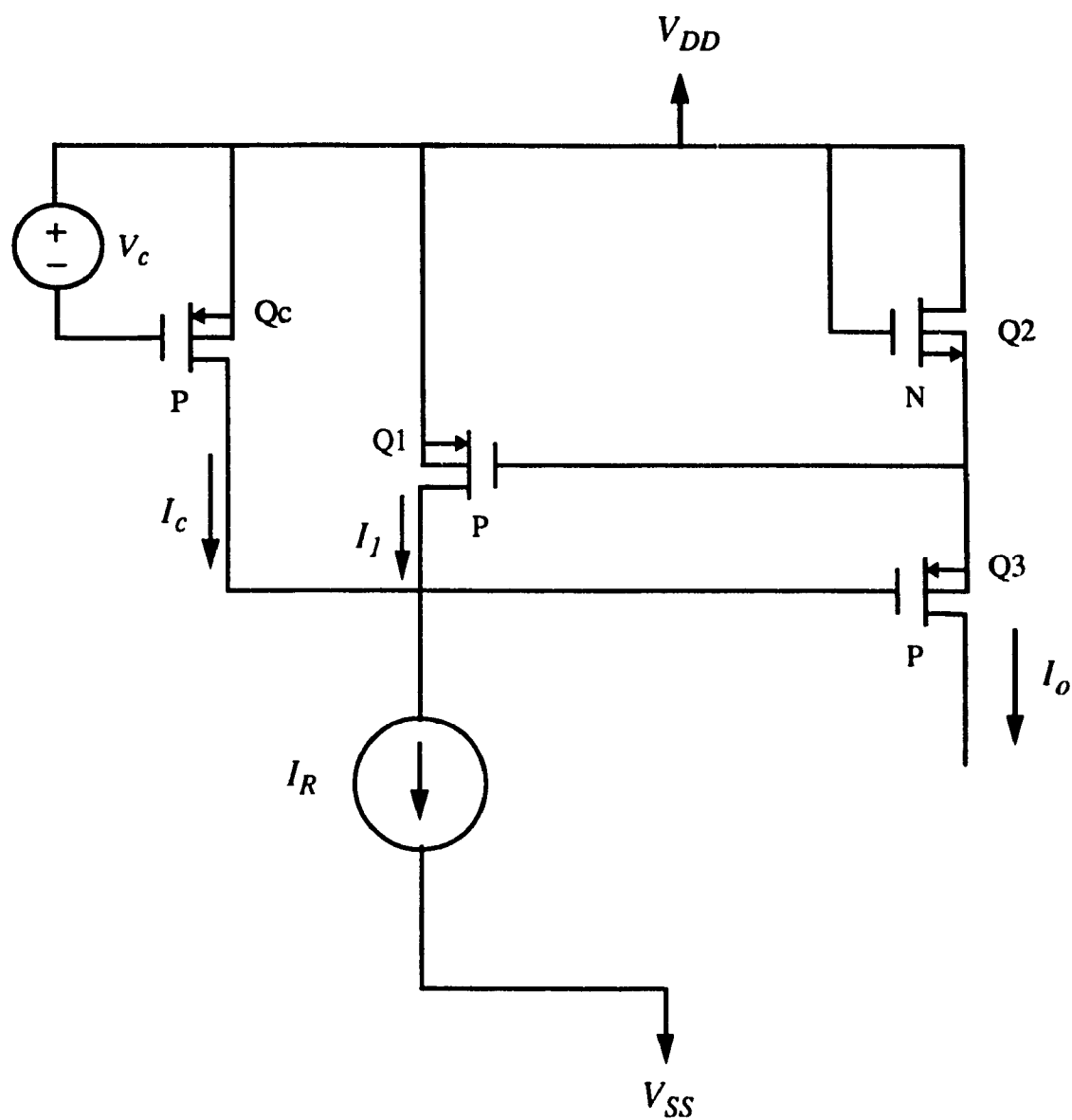


Fig. 3.9

Circuit diagram shows the control circuit connected to Type II-b NCMOS current mirror.

$$I_1 = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD1}) \quad (3.34)$$

Since the reference current I_R is the sum of I_I and I_c and $V_{SD1} = V_{SDC}$ then:

$$I_R = \frac{K_p}{2} \cdot ((V_R - V_{Tp})^2 + (V_c - V_{Tp})^2) \cdot (1 + \lambda_p V_{SD1}) \quad (3.35)$$

Referring to eqn. (B.7) in Appendix B, the output current I_o is:

$$I_o = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (3.36)$$

Dividing eqn.(3.36) by eqn.(3.35) the following current ratio is obtained:

$$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2 + (V_c - V_{Tp})^2} \cdot \frac{(1 + \lambda_n (V_R \cdot (1 + \sqrt{\frac{K_p}{K_n}}) - V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}} + V_{Tn}))}{(1 + \lambda_p V_R)} \quad (3.37)$$

Assuming $\lambda_p V_{SD1} \ll 1$, we have, from eqn. (3.35),

$$I_R = \frac{K_p}{2} \cdot ((V_R - V_{Tp})^2 + (V_c - V_{Tp})^2) \quad (3.38)$$

Thus, when both Q_c and Q_I transistors are in saturation region,

$$V_R = \sqrt{\frac{2I_R}{K_p} - (V_c - V_{Tp})^2} + V_{Tp} \quad (3.39)$$

The control transistor Q_c will stay in saturation region as long as the control voltage V_c is not going to exceed the source-to-drain voltage by more than the threshold voltage V_{Tp} i.e.:

$$\frac{V_c}{V_{SDC} + V_{Tp}} \leq 1 \quad (3.40)$$

The maximum limit for the control voltage V_c will then be:

$$V_{Cmax} = V_{SDC} + V_{Tp} \quad (3.41)$$

It can be written in terms of the reference voltage and the threshold voltage as follows:

$$V_{Cmax} = V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}}\right) - V_{Tn} \sqrt{\frac{K_n}{K_p}} + 2V_{Tp} \quad (3.42)$$

It is possible now to write the reference voltage V_R in terms of the maximum control voltage as shown below:

$$V_R = \frac{V_{Cmax} + V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} - 2V_{Tp}}{2 + \sqrt{\frac{K_n}{K_p}}} \quad (3.43)$$

The reference current can also be written in terms of the voltage V_{Cmax} as follows:

$$I_R = \frac{K_p}{2} \cdot (V_{Cmax} - V_{Tp})^2 + \left(\frac{V_{Cmax} + V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} - 2V_{Tp}}{2 + \sqrt{\frac{K_n}{K_p}}} - V_{Tp} \right)^2 \quad (3.44)$$

Equation (3.44) will be solved by a nonlinear computer programming to find the value of V_{Cmax} for each reference current level I_R . The solution programs for this circuit are supplied in Appendix A. Relevant expressions are listed in Table 3.1 and Table 3.2. Fig.3.7 compares the analysis and HSPICE simulation results.

3.2.4 VOLTAGE CONTROLLED TYPE VIII NCMOS CURRENT MIRROR

The connection of the control PMOS Q_c to this current mirror is shown in Fig.3.10. The control PMOS transistor Q_c is going to share with both of Q_1 and Q_4 MOS transistors the current sunk to the reference current source I_R . The value of the current I_c will depend mainly on the control voltage V_c .

If the reference current is held constant, any increase in the injecting current from transistor Q_c will cause a decrease by the same amount in the current I_1 that passes through

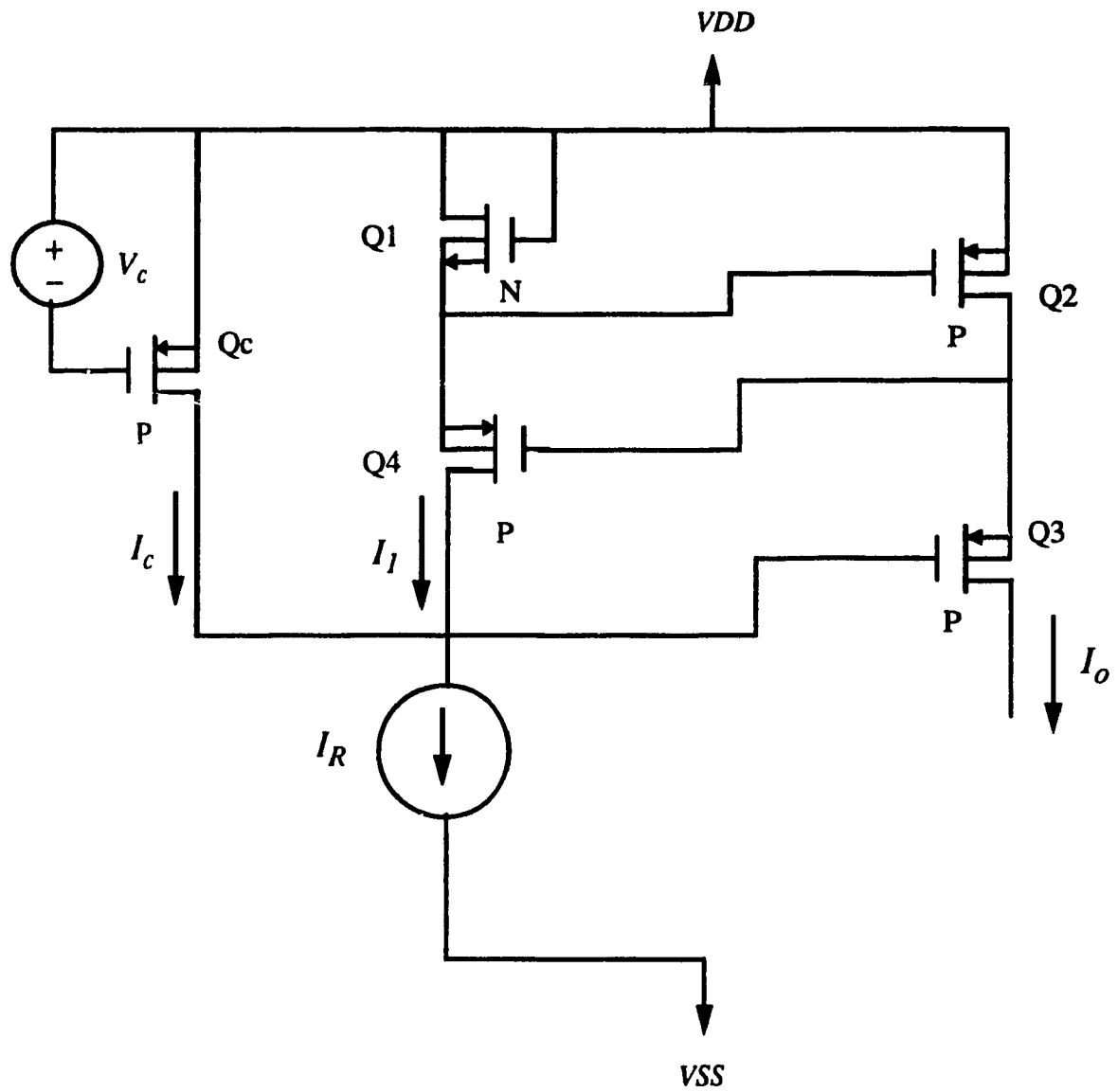


Fig. 3.10

Circuit diagram shows the control circuit connected to Type VIII NCMOS current mirror.

Q_1 and Q_4 transistors, and this will lead to a reduction in the gate-to-source voltage of both MOSFETs Q_1 and Q_4 , causing a reduction in the output current I_o . The control current I_c can be written as follows:

$$I_c = \frac{K_p}{2} \cdot (V_c - V_{Tp})^2 \cdot (1 + \lambda_p V_{SDC}) \quad (3.45)$$

The current I_1 can be written in terms of Q_1 NMOS transistor parameters as:

$$I_1 = \frac{K_n}{2} \cdot (V_{GS1} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS1}) \quad (3.46)$$

where: $V_{DS1} = V_{GS1} = V_R$

Because the reference current I_R is equal to the sum of the previous two currents I_c and I_1 , we get:

$$I_R = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) + \frac{K_p}{2} \cdot (V_c - V_{Tp})^2 \cdot (1 + \lambda_p V_{SDC}) \quad (3.47)$$

Since the voltage $V_{SDC} = V_{DS1} + V_{SD4}$, while the voltage $V_{SD4} = V_{SG4} + V_{SG3}$.

Because the voltage $V_{DS1} = V_{GS1} = V_R$. Thus, by using eqn. (B.24), Appendix B, we get:

$$V_{SDC} = 2V_R + \left(\sqrt{\frac{K_n}{K_p}} \cdot (V_R - V_{Tn}) \cdot \sqrt{\frac{(1 + \lambda_n V_R)}{(1 + \lambda_p 2V_R)}} \right) + V_{Tp} \quad (3.48)$$

Consequently, the reference current I_r becomes:

$$I_R = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) + \frac{K_p}{2} \cdot (V_c - V_{Tp})^2 \cdot \left(1 + \lambda_p \left(2V_R + \sqrt{\frac{K_n}{K_p}} \cdot (V_R - V_{Tn}) \cdot \sqrt{\frac{(1 + \lambda_n V_R)}{(1 + \lambda_p 2V_R)}} + V_{Tp} \right) \right) \quad (3.49)$$

Also from Appendix B, eqn. (B.26), the output current is:

$$I_o = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot \left(1 + \lambda_p \left(V_R + \left(\sqrt{\frac{K_n}{K_p}} \cdot (V_R - V_{Tn}) \cdot \sqrt{\frac{(1 + \lambda_n V_R)}{(1 + \lambda_p 2V_R)}} \right) + V_{Tp} \right) \right) \quad (3.50)$$

Dividing eqn. (3.50) by eqn. (3.49), the current ratio can be written as follows:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \frac{(V_R - V_{Tp})^2 \cdot \left(1 + \lambda_p \left(V_R + \left(\sqrt{\frac{K_n}{K_p}} \cdot (V_R - V_{Tn}) \cdot \sqrt{\frac{(1 + \lambda_n V_R)}{(1 + \lambda_p 2V_R)}} \right) + V_{Tp} \right) \right)}{\frac{K_p}{K_n} (V_c - V_{Tp})^2 \left(1 + \lambda_p \left(2V_R + \left(\sqrt{\frac{K_n}{K_p}} (V_R - V_{Tn}) \sqrt{\frac{(1 + \lambda_n V_R)}{(1 + \lambda_p 2V_R)}} \right) + V_{Tp} \right) \right) + (V_R - V_{Tn})^2 (1 + \lambda_n V_R)} \quad (3.51)$$

The current ratio equation is complicated because of the λ factors. Ignoring the λ factors, the current ratio equation becomes:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \frac{(V_R - V_{Tp})^2}{\frac{K_p}{K_n} (V_c - V_{Tp})^2 + (V_R - V_{Tn})^2} \quad (3.52)$$

It has been verified that this approximation will not affect the value of the control voltage V_c and the reference voltage V_R by more than 3%.

Assuming $\lambda_p V_{SDC} \ll 1$, we get, from eqn. (3.47),

$$I_R = \frac{K_n}{2} \cdot ((V_R - V_{Tn})^2 + \frac{K_p}{K_n} \cdot (V_c - V_{Tp})^2) \quad (3.53)$$

Rearranging eqn. (3.53) by putting the voltage V_R in terms of the current I_R and the control voltage V_c , it becomes:

$$V_R = \sqrt{\frac{2I_R}{K_n} - \frac{K_p}{K_n} (V_c - V_{Tp})^2} + V_{Tn} \quad (3.54)$$

The previous equation will not be satisfied if the control transistor moves out of the saturation region, which means it is necessary to restrict the functional range of the control voltage i.e.,

$$\frac{V_c}{V_{SDC} + V_{Tp}} \leq 1 \quad (3.55)$$

Using eqn. (3.48) with the previous equation, we can define the maximum control voltage approximately in terms of the reference voltage as shown below:

$$V_{Cmax} \approx V_R \cdot \left(2 + \sqrt{\frac{K_n}{K_p}} \right) - V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} + 2V_{Tp} \quad (3.56)$$

The value of the reference voltage in terms of the maximum control voltage becomes:

$$V_R = \frac{V_{Cmax} + V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} - 2V_{Tp}}{2 + \sqrt{\frac{K_n}{K_p}}} \quad (3.57)$$

The maximum control current that can be derived from Q_c transistor to the reference current source, while staying in the saturation region of Q_c transistor, is:

$$I_{Cmax} = \frac{K_p}{2} \cdot (V_{Cmax} - V_{Tp})^2 \quad (3.58)$$

The corresponding minimum current that passes through the reference side of transistor Q_l can also be written in terms of the maximum control voltage as:

$$I_{lmin} = \frac{K_n}{2} \cdot \left(\frac{V_{Cmax} + V_{Tn} \sqrt{\frac{K_n}{K_p}} - 2V_{Tp}}{2 + \sqrt{\frac{K_n}{K_p}}} - V_{Tn} \right)^2 \quad (3.59)$$

Taking the sum of eqn. (3.58) and eqn. (3.59), the reference current can now be written as a function of one variable which is the V_{Cmax} .

$$I_R = \frac{K_p}{2} \cdot (V_{Cmax} - V_{Tp})^2 + \frac{K_n}{2} \cdot \left(\frac{V_{Cmax} + V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} - 2V_{Tp}}{2 + \sqrt{\frac{K_n}{K_p}}} - V_{Tn} \right)^2 \quad (3.60)$$

The solution of this equation can be achieved by using nonlinear computer programming. The solution programs are given in Appendix A. Relevant expressions of this analysis are listed in Table 3.1 and Table 3.2. Fig. 3.7 compares the analysis and HSPICE simulation results.

3.3 SUMMARY

A method of increasing the current gain of the NCMOS current mirrors considered in Chapter 2 by cascading and/or parallel them has been presented in this chapter. A technique for the voltage control of the current ratio is also discussed. The analysis and simulation results of the current mirrors with their control circuits are also presented. Only four circuits have been selected to show the analysis in details. The selections are based on their performance superiority as controllable NCMOS current mirrors. Depending on NCMOS current mirror type, the range of control can be from the full value to about 2% (for type V NCMOS current mirror) and 10% (for type IIb current mirror) of the full value while maintaining the control MOSFET in the saturation region. Final current ratio equations for all the circuits are however given in Tables 3.1 & 3.2. Results of analysis and HSPICE simulation show that most of these NCMOS current mirrors have a good control response. These results are given in Fig.3.4 and Fig.3.5 which show the current ratio variations with control voltage (from analysis) for both sink and source NCMOS current mirrors. The response of each controlled current mirror derived from both analysis and HSPICE simulator are compared in Fig.3.7 for the four selected circuits. Since this design depends on an external control voltage to adjust the required output current, Table 3.1 also shows how the required control voltage can be determined for a given reference current.

The non-linearity of the output current with the control voltage make its application limited to certain circuits such as an automatic gain control circuits or a symmetrical structure circuits such as an OTA circuit shown in the next chapter.

An application of the NCMOS current mirrors is considered in next chapter that shows the advantage of using the proposed NCMOS current mirrors over the regular one from the point of view of area minimization and reduction of power consumption.

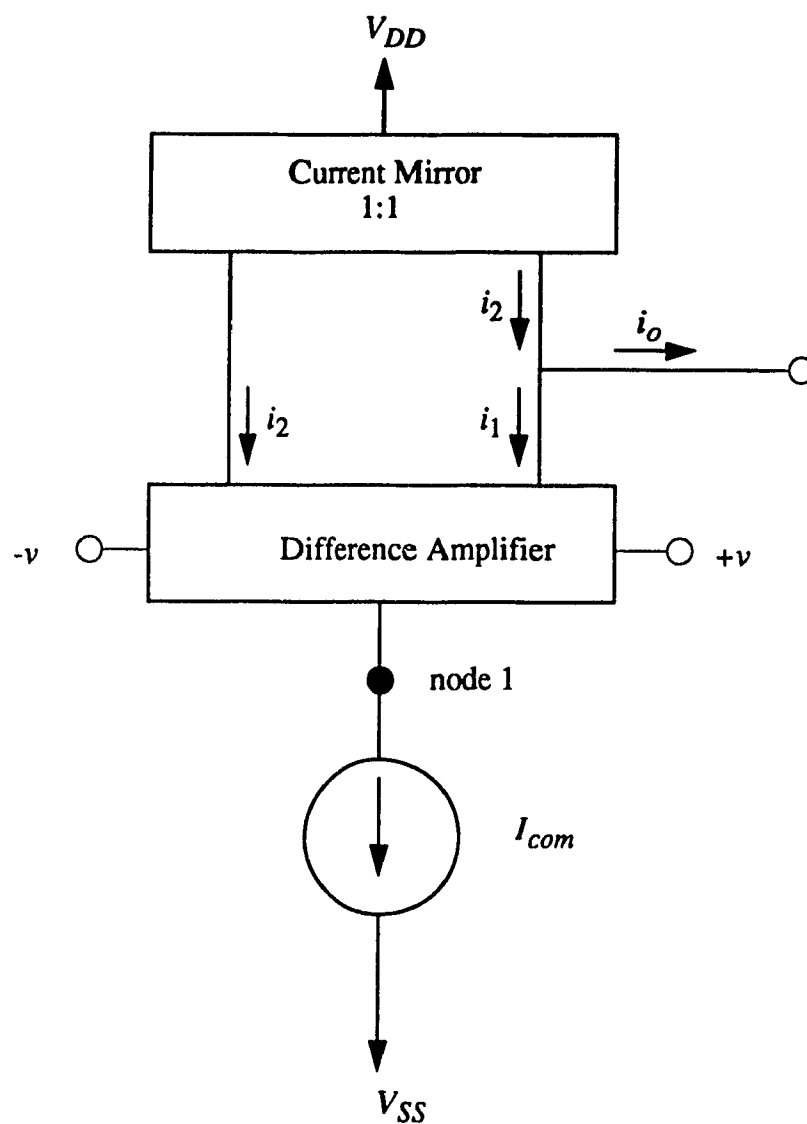
CHAPTER 4

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER - AN APPLICATION OF THE NCMOS CURRENT MIRRORS

4.0 GENERAL

One of the most important elements in continuous-time circuit design is the Operational Transconductance Amplifier (OTA). It is also a useful building block in analog signal-processing systems[18] and continuous time filters. It is a programmable device and has only a single high impedance node, in contrast to conventional op amps. This makes the OTA an excellent device candidate for high-frequency and voltage (or current) programmable analog basic building block[19]. Different techniques have been used in designing the OTA seeking optimization of various performance characteristics i.e. better linearity, wider dynamic range, etc[20]. In addition to these circuit design objectives, a low power consumption and minimum chip area are desirable. An OTA design is proposed in this chapter using an NCMOS current mirror developed in this thesis. It is superior in area and power consumption when comparing to those using a conventional current mirror in certain respects. The dynamic current control technique used in [21-25] is not useful for the continuous time OTA designed in this chapter because of the large phase shift between the input and output signals at high frequencies.

Two basic building blocks are used in any OTA circuit design. These blocks are a difference amplifier and a current mirror. A simple structure of an OTA is shown in Fig.4.1. Consider a difference amplifier with a matched NMOS pair of MOSFETs (Q_1 , Q_2) with an input voltage v applied to the positive input (gate) terminal and $-v$ to negative input (gate) terminal.

**Fig. 4.1**

Block diagram for a basic operational transconductance amplifier.

The drain current of the MOSFET $Q1$ can be defined as follows:

$$i_1 = \beta \cdot (v - V_1 - V_{Tn})^2 \quad (4.1)$$

and the drain current of the MOSFET $Q2$ will be written as:

$$i_2 = \beta \cdot (-v - V_1 - V_{Tn})^2 \quad (4.2)$$

where the voltage V_1 represents the DC potential at node 1 in Fig. 4.1. If the difference amplifier shown in Fig. 4.1 is truly symmetric with respect to the positive and negative input terminals, the ac voltage at node 1 is zero.

The AC output current is defined as the difference between both drain currents i_1 and i_2 :

$$i_o = i_2 - i_1 = 4\beta \cdot v (V_1 + V_{Tn}) \quad (4.3)$$

The transconductance of this circuit is defined as:

$$g_m = \frac{\Delta i_o}{\Delta v} = 4\beta (V_1 + V_{Tn}) = 2K_n \frac{W}{L} (V_1 + V_{Tn}) \quad (4.4)$$

Eqn.(4.4) shows that the transconductance of this circuit is perfectly linear and its value can be varied by the variables W/L (size of the MOSFET) and V_1 (i.e. DC voltage level at node 1 which depends on the DC common current level). Any changes in the common current will cause a related change in the DC operating point of the difference pair which will limit the linear range of operation of the OTA. This is because the MOSFET pair of the difference amplifier will approach the linear region or the cutoff region of operation instead of staying in the saturation region as I_{com} is increased or decreased. As an example, the characteristic curves¹ given in Fig.4.2 show if the current I_{com} is increased from $10\mu A$ to $20\mu A$, the operating point of the difference amplifier will move from point A to point B

1. For the sake of illustration, it is assumed that the drain loads of the matched MOSFETs are identical resistors fed by supply voltage of 10 volts.

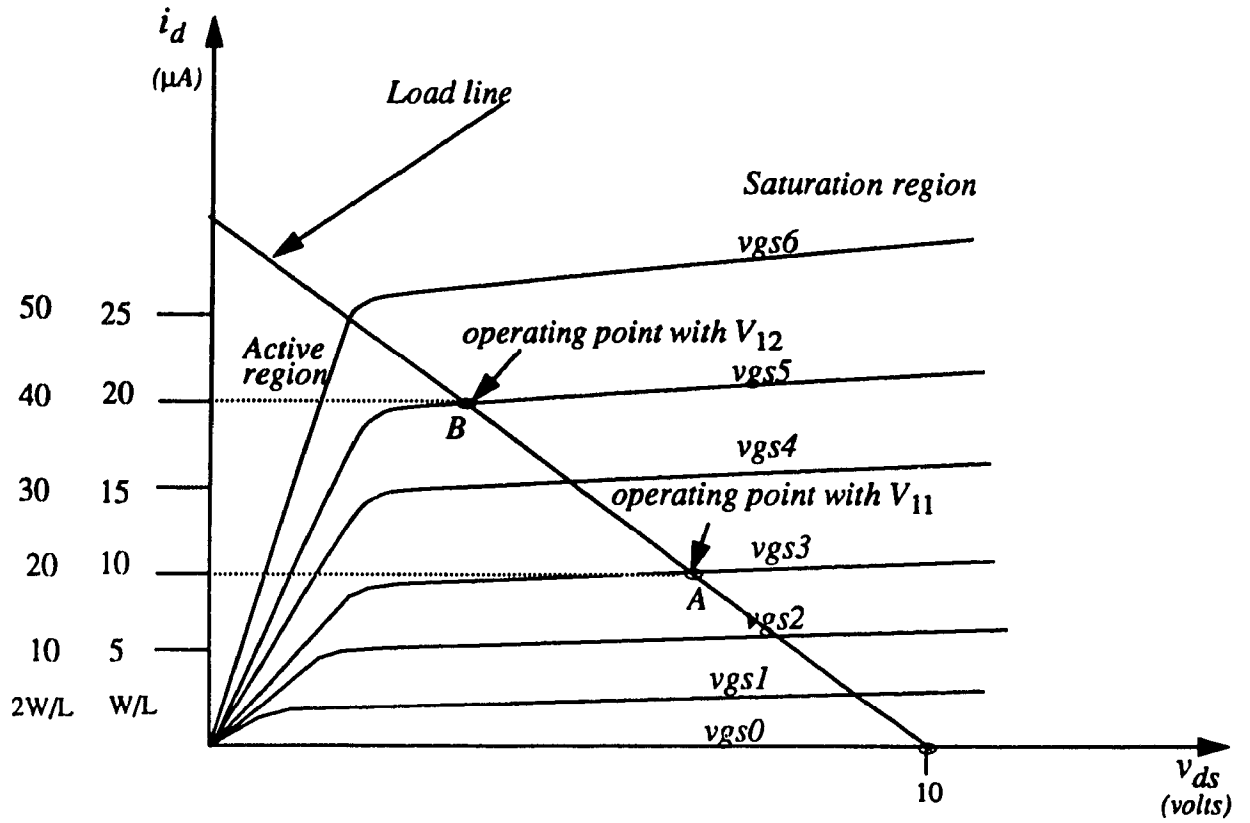


Fig.4.2

Operating points locations with two different values of control voltage V_1 . at node 1 of Fig. 4.1.

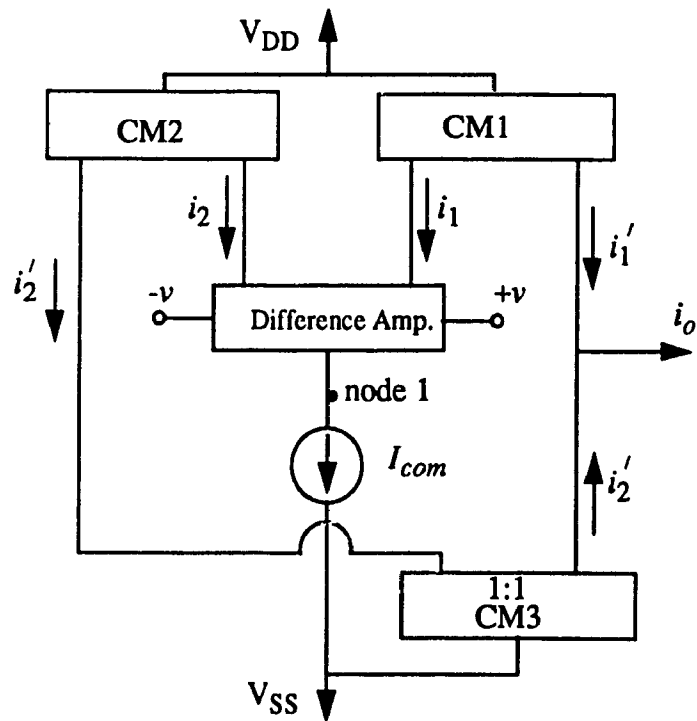


Fig.4.3

Block diagram for the proposed model of the OTA.

which is very near to the linear region and this will cause the circuit to work improperly. To keep the operating point close to A, the W/L ratio may be doubled i.e. doubling the gate width of both $Q1$ and $Q2$ MOSFETs. Fig.4.2 shows that it is possible to increase the value of the common current I_{com} to $20\mu A$ while the DC operating point stays at point A using this method. However this method will lead to more power consumption and more chip area in VLSI implementation.

The block diagram of the proposed OTA model suitable for employing the NCMOS current mirrors developed in this thesis is shown in Fig.4.3. The differential amplifier in this OTA model has two independent loads, current mirrors CM1 and CM2. The unity gain current mirror CM3 is used to convert the current source i'_2 from a source version to a sink version, to allow subtraction from the current i'_1 . The output current can be written as:

$$i_o = 4G\beta \cdot v(V_1 + V_{Tn}) \quad (4.5)$$

where G is the current gain for each of current mirrors CM1 and CM2.

The value of g_m can be written as:

$$g_m = \frac{\Delta i_o}{\Delta v} = 4G\beta V_1 = 2GK_n \frac{W}{L} (V_1 + V_{Tn}) \quad (4.6)$$

The advantage of this circuit is that the operating point of the difference amplifier will remain unaffected when the range of g_m is varied, by say, variation of G . The value of G can be increased either by increasing the sizes of the output MOSFETs of both current mirrors CM1 and CM2, or by using the NCMOS current mirrors developed in this thesis. The first approach has the disadvantage of the MOSFET area increasing. It is also sensitive to the implementation problems, such as misalignment, discussed in chapter 1. Further this will create an offset output current without any signal being applied depending on the angle

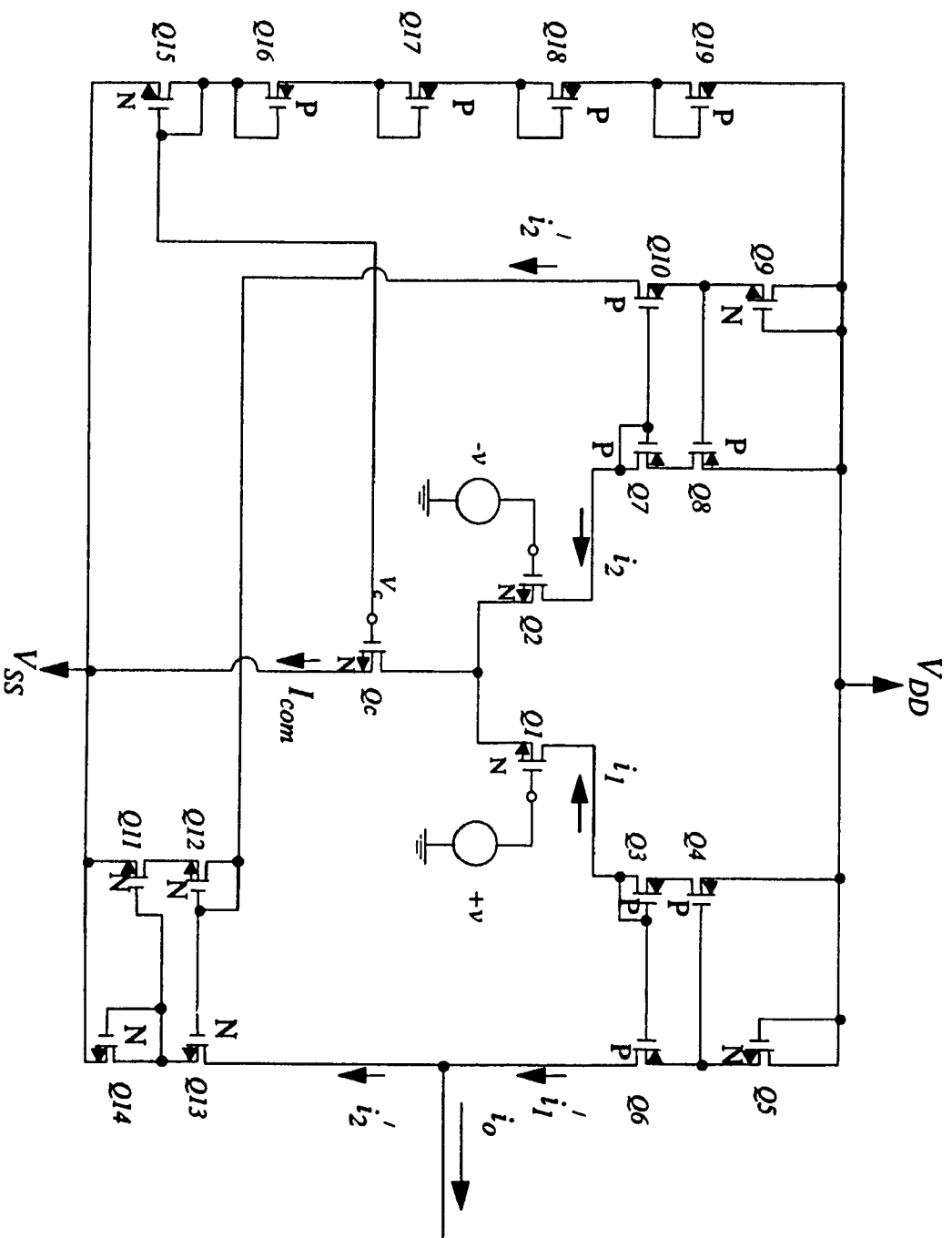


Fig. 4.4
Circuit Diagram for an OTA using the NCMOS current mirror

of implementation for each current mirror and inequality in ΔX and ΔY of the masks misalignment. The transconductance will be affected by this current and its range of linearity will be shifted by this amount. The second approach is attractive as it does not suffer from these disadvantages because of using equal size MOSFETs. The circuits using this approach have a disadvantage of the well capacitance which needs to be considered during the design. This capacitance will appear connected to the source of each MOSFET.

The NCMOS current mirror circuit which is used for CM1 and CM2 is the best source version with a gain greater than unity. Referring to chapter 2, this NCMOS current mirror is type IIIb because of its superior performance with respect to the other current mirrors of the same type. The current mirror CM3 is a regular NMOS current mirror with a unity current gain and the type “modified wilson current mirror” is selected. The complete circuit diagram is shown in Fig.4.4.

4.1 DESIGN OF THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The electronic circuit design consists of two main steps. The first one is the D.C. analysis while the next one will be the A.C. analysis. The OTA circuit shown in Fig.4.4 has to be analyzed in D.C. and A.C. The D.C. analysis will show the steady state operating condition of this circuit i.e. it gives the operating point of the difference amplifier and the D.C. operating currents of the current mirrors and current source according to the designed values. The A.C. analysis will give the maximum A.C. operating range of the output current of this circuit depending on the small signal circuit parameters of the MOSFET models used. It also gives the 3dB and the maximum operating (cutoff) frequencies of the OTA circuit.

4.2 D.C. ANALYSIS

The D.C. analysis treats the operational transconductance amplifiers as consisting of two main circuits, a difference amplifier in the input stage and the current mirror(s) in the

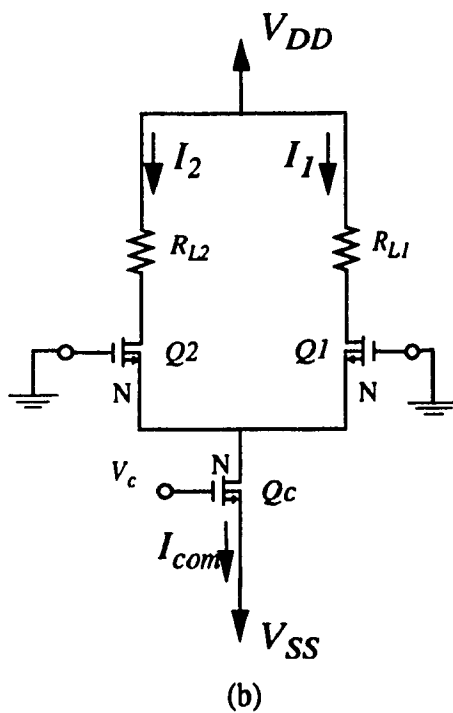
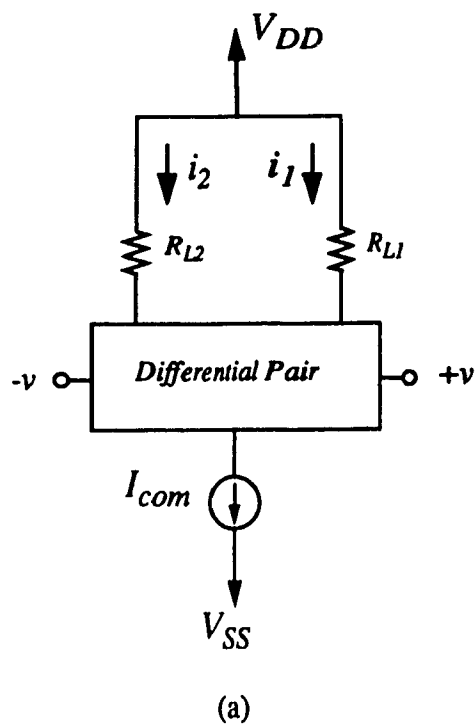


Fig.4.5

Difference amplifier circuit (a) Basic structure (b) MOSFET implementation.

output stage. Its biasing comes through an active load voltage divider and a current mirror to create the required current source for the difference amplifier.

4.2.1 D.C. ANALYSIS OF THE DIFFERENCE AMPLIFIER

The basic structure of a difference amplifier is shown in Fig 4.5a. The current source I_{com} can be implemented by using a single MOSFET (Q_c) with a D.C. control voltage applied to its gate as shown in Fig.4.5b. The two MOSFETs Q_1 and Q_2 are identical and their source terminals are connected together. This arrangement make drain currents I_1 and I_2 equals, provided Q_1 and Q_2 are in DC saturation.

Assume that the MOSFET Q_c works in the saturation region acting as a current source to obtain the common current I_{com} with a value equal to $10\mu A$. Assume also that the NMOS transistor Q_c has a W/L ratio equal to 1. The control voltage $V_{GSC} = V_C - V_{SS}$ will be equal to:

$$V_{GSC} = \sqrt{\frac{2I}{K_n}} + V_{Tn} = \sqrt{\frac{20}{40}} + 0.7 = 1.4V \quad (4.7)$$

Since both Q_1 and Q_2 MOSFETs are identical, they will share equally the common current I_{com} and their drain currents I_1 and I_2 will be $5\mu A$. These two transistors are also supposed to work in the saturation region. Consequently, their gate to source voltages V_{GS1} and V_{GS2} are equal to each other and their value are given by:

$$V_{GS1} = \sqrt{\frac{2I_1}{K_n}} + V_{Tn} = \sqrt{\frac{10}{40}} + 0.7 = 1.2V = V_{GS2} \quad (4.8)$$

The previous voltages are the D.C. levels of the circuit when the A.C. input signal is supposed to be equal to zero. If the circuit of Fig.4.1 is used to get an output current, then the maximum positive output current will occur when the current I_1 is equal to zero. Hence,

$$I_{omax} = I_{2max} - 0 = I_{com} = 10\mu A \quad (4.9)$$

This limit of D.C. output current can be considered roughly the same as the limit for the A.C. signal. The transconductance for this circuit at this level of common current source ($I_{com} = 10\mu A$) will be:

$$g_m = \frac{\partial i_O}{\partial v_{GS2}} = \frac{2 \times \partial i_2}{\partial v_{GS2}} = 4 \cdot \beta \cdot (v_{GS2} - V_T) = 56\mu S \quad (4.10)$$

The transconductance g_m can be increased by increasing the common reference current. This can be done even by increasing the D.C. control voltage V_c of the current source I_{com} or through increasing the size of the MOSFET Q_c , i.e. the ratio W/L is selected to be greater than unity. These techniques will lead to an increase in the voltage v_{GS2} and consequently, to an increase in the transconductance g_m .

For the previous values of difference amplifier, if the structure of Fig.4.3 is used, the maximum D.C. output current will also be equal to $10\mu A$ and the same g_m will be achieved. In addition to the previous two ways of increasing the transconductance g_m , we now have a third way of increasing g_m . This is accomplished by increasing the current gain of both current mirrors CM1 and CM2 from unity to G which can be achieved by using the NCMOS current mirrors without increasing the size of the current mirror MOSFETs. If the value of the current gain G is set to K^n then the transconductance value will be:

$$g'_m = 4G \cdot \beta \cdot (v_{GS2} - V_T) = K^n \cdot 4 \cdot \beta \cdot (v_{GS2} - V_T) = K^n g_m \quad (4.11)$$

where K is the MOSFET transconductance ratio which is equal to $\frac{K_n}{K_p} = 3.34$ and n is the number of the NCMOS current mirrors cascaded. The number n for circuit of Fig.4.3 is equal to 1 then:

$$g'_m = \frac{K_n}{K_p} \cdot g_m = 3.34 \times 56\mu S = 187\mu S \quad (4.12)$$

This is a remarkable increase in g_m , achieved without increasing the current mirror size or the control voltage V_c .

4.2.2 CURRENT MIRRORS AND CURRENT SOURCES

In section 4.0 it is mentioned that the current mirror circuit to be selected for CM1 and CM2 is the Type IIIb NCMOS current mirror. The D.C. analysis for them is given in Chapter 2 and the final current ratio expressions are given in Table 2.1. CM3 current mirror is a regular unity gain current mirror. The modified Wilson current mirror is selected for this element. The current source connected to the source terminals of both $Q1$ and $Q2$ MOSFETS is represented by a single MOSFET Q_c as shown in Fig.4.5b. The voltage V_c for a certain designed value can be delivered from a voltage divider consisting of MOSFETs in series. The combination of the divider with Q_c MOSFET acts as a simple current mirror of Type Ia NCMOS current mirror.

4.3 AC ANALYSIS OF THE OTA

An important parameter in MOSFET devices is the transconductance. It is derived in saturation region by differentiating the MOSFET drain current equation with respect to the gate voltage v_{GS} , which leads to:

$$g_m = 2\beta(v_{GS} - V_T) = \frac{\mu_n C_{ox} W}{L} (v_{GS} - V_T) \quad (4.13)$$

According to the idealized theory, the drain current remains constant for any drain voltage beyond pinchoff. This means that the drain resistance is infinite in the saturation region. However, all experimental MOSFETs shows a finite slope in their drain current-voltage characteristics in this region, (Fig. 4.2). Therefore, we define the drain resistance in the saturation region as:

$$r_{ds} = r_d(sat) \equiv \left. \frac{\partial v_{DS}}{\partial i_D} \right|_{v_{GS} = \text{constant}} \quad (4.14)$$

The drain resistance in the saturation region can be obtained graphically from the drain characteristics shown in Fig. 4.2.

An equivalent small signal circuit of the MOSFET is shown in Fig.4.6. The gate to drain capacitance C_{gd} usually dominates the high frequency response because of the Miller effect[26]. The gate to source capacitance C_{gs} also has an effect on the cutoff frequency. The Maximum operating frequency or cutoff frequency f_{co} is defined as the frequency beyond which the transistor no longer amplifies the input signal.

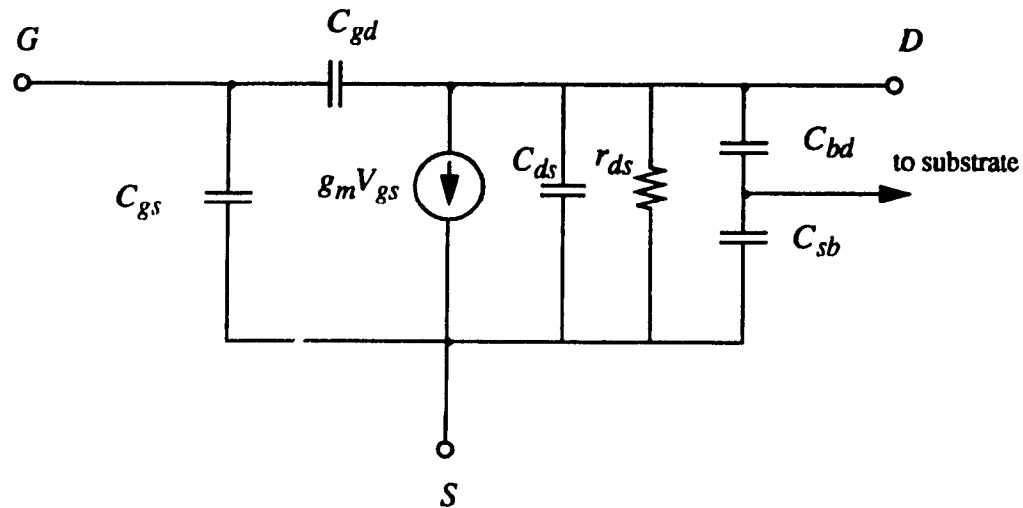


Fig.4.6
Small signal model of a MOSFET[26].

It is noted that a large mobility and a short channel length are required to achieve a high cutoff frequency[26].

The gate capacitance outside the saturation region¹ defined as:

$$C_{gs} + C_{gd} = C_G = WLC_{ox} = \text{the gate capacitance} \quad (4.15)$$

while in the saturation region the dominant capacitive effect is that of the gate-source capacitance, and its value is given by:

$$C_{gs} = 0.67 \times C_G = 0.67 \times C_{ox} \times W \times L \quad (4.16)$$

1. $C_{gs} + C_{gd} \neq WLC_{ox}$ in the saturation region[20].

The gate-drain capacitance starts to affect in the linear region and its value is equal to gate-source capacitance in this region,[4]. It is given by:

$$C_{gs} = 0.5C_G = 0.5 \times C_{ox} \times W \times L = C_{ds} \quad (4.17)$$

Assuming all MOSFETs have the same gate capacitance (C), the small signal circuit model of the OTA is shown in Fig. 4.7. The cutoff frequency of this circuit can be derived as follows.

The small signal high frequency input current to the MOSFET Q_2 in difference amplifier is:

$$i_{ind} = \frac{v_{gs2}}{\left(\frac{2}{sC} + r_o\right)} \quad (4.18)$$

where r_o is the output resistance of the MOSFET Q_c . The output current of this stage is equal to:

$$i_d = g_{m2} \times v_{gs2} \quad (4.19)$$

The current ratio of this stage becomes:

$$\frac{i_d}{i_{ind}} = g_{m2} \times \left(\frac{2}{sC} + r_o\right) \quad (4.20)$$

where i_{ind} is the input current and i_d is the output current of difference amplifier.

The AC current to voltage ratio equals the transconductance of the input MOSFET,

$$\frac{i_2}{v_{gs2}} = g_{m2}$$

The transfer function of this NCMOS current mirror can be written as follows:

$$\frac{i_2'}{i_2} = \frac{g_{m7}}{g_{m7} + 3.7sC + 1/(r_{ds7})} \quad (4.21)$$

where g_{m7} is the transconductance at drain current of $5\mu A$.

The NMOS current mirror transfer function can be defined as follows:

$$\frac{i_2''}{i_2'} = \frac{g_{m12}}{g_{m12} + 4sC + 1/(r_{ds12})} \quad (4.22)$$

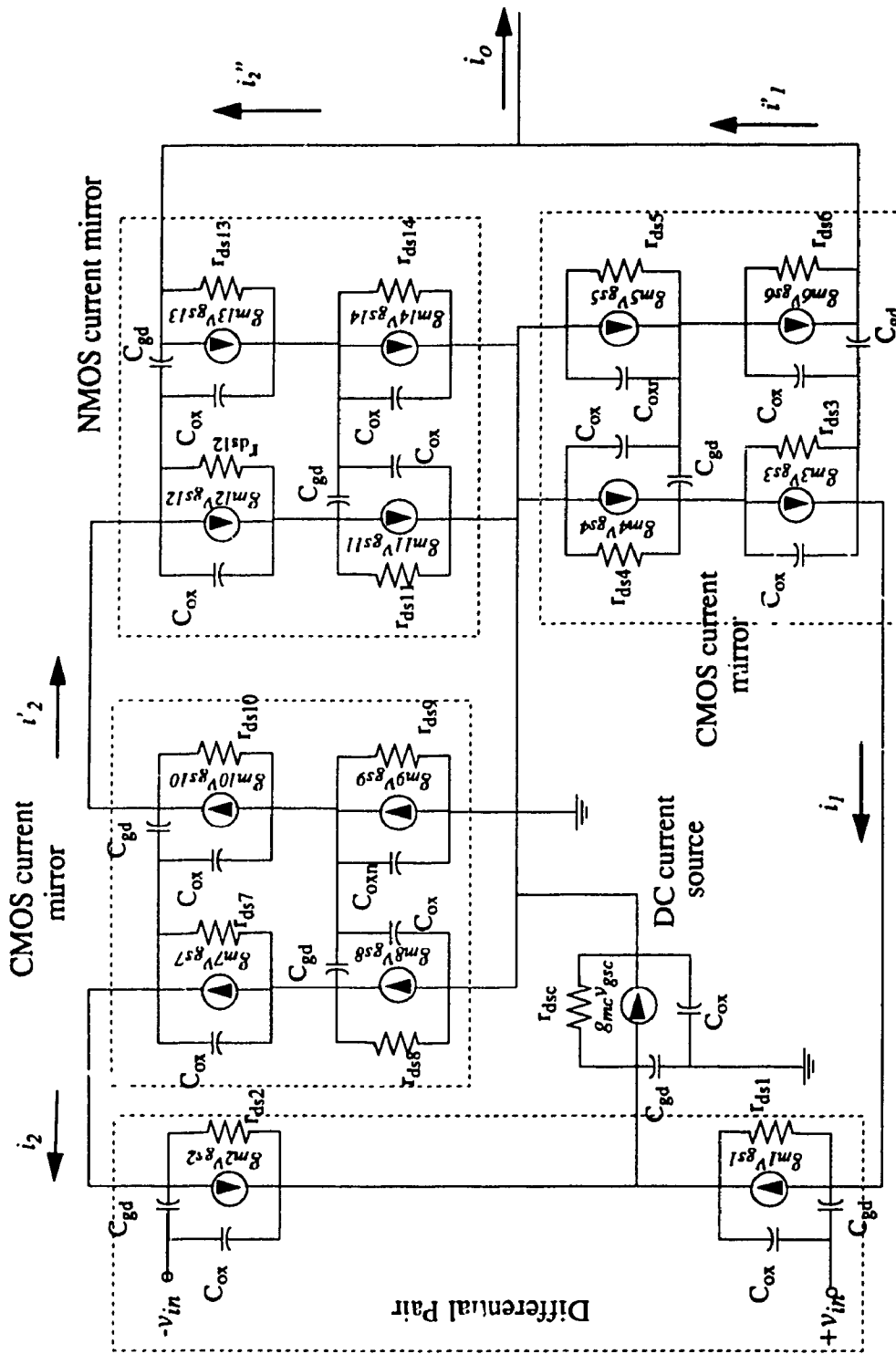


Fig. 4.7

Small signal equivalent circuit of the operational transconductance amplifier.

The OTA small signal high frequency transfer function will be the multiplication of the previous three transfer functions i.e.:

$$\frac{i_{out}}{v_{in}} = g_{m2} \cdot \frac{g_{m12}}{g_{m12} + 4sc + 1/(r_{ds12})} \cdot \frac{g_{m7}}{g_{m7} + 3.7sc + 1/(r_{ds7})} \quad (4.23)$$

The denominator of this transconductance is a second order equation and the 3 dB frequency, defined as the frequency at which the output current is reduced to 0.707 of its low frequency value. The variables given in eqn. (4.23) has the following values:

$r_{ds7} = 4.17 \text{ M}\Omega$ (from the HSPICE MOSEFT model, at the operating current value).

$r_{ds12} = 3.4 \text{ M}\Omega$ (from the HSPICE MOSEFT model, at the operating current value).

$C = 0.6 C_{ox} = 0.005 \text{ pF}$ for minimum gate size in the 3 micron technology.

$g_{m7} = g_{m2} = 10 \mu\text{S}$ for differential pair and input stage of NCMOS current mirror.

$g_{m12} = 22 \mu\text{S}$ for NMOSFET in NCMOS current mirror and NMOS regular current mirror.

Substituting these values in eqn. (4.23), the 3dB frequency has a value of 45 MHz. The advantages of the NCMOS current mirrors used in this OTA circuit lie in minimum area usage and reduced power consumption (by 37%) while keeping the same output current level. A comparison between the following three cases is given in Table 4.1, where the following definitions are used with the 3 μm CMOS3 DLM model.

1. model #1: OTA circuit with NCMOS current mirrors (gain greater than unity) and reduced current level in differential amplifier than in model #2 ($I_{com} = 10 \mu\text{A}$), $V_{DD} = -V_{SS} = 5\text{V}$.
2. model #2: OTA circuit with regular current mirrors (unity current gain) and differential amplifier bias current level of ($I_{com} = 20 \mu\text{A}$), $V_{DD} = -V_{SS} = 5\text{V}$.
3. model #3: OTA circuit with regular current mirror (gain greater than unity) and same differential amplifier bias current level.

The percent difference in power, area and maximum output current between the three models under the same current mirror DC output current condition are given in Table 4.2. It shows the superiority in area saving and power consumption reduction of the OTA circuit when using the NCMOS current mirror.

A comparison between the frequency response of the three models of OTA is given in Table 4.3. It shows that model #1 OTA has better range of linearity and good 3 dB frequency in comparison with the other two models.

Fig. 4.8 shows the VLSI layout of the OTA circuit using the NCMOS current mirrors given in Fig.4.9. The difference between the OTA circuits shown in Fig. 4.4 and Fig. 4.9 is the grounded substrate that appears in Fig. 4.9 while a separate substrate for each MOSFET are used in Fig. 4.4. The complete single-well layout requires $(110 \times 100 \mu\text{m}^2)$ chip area in the 1.2 micron technology. The development of the VLSI layout for this circuit is facilitated by the fact that all the MOSFETs are of the same size.

Thus once a single MOSFET file is created, the same file can be recalled repeatedly to complete the layout procedure efficiently. The node capacitance needs to take care of when using the twin-tub technology because of the tub capacitance. It is not included here because of invalidity of this technology at concordia university VLSI lab.

4.4 SUMMARY

An application of the NCMOS current mirrors developed in this thesis in the design of an OTA circuit is described in this chapter. The special structure of an OTA proposed in Fig. 4.3 has been discussed with regard to its advantages over the conventional structure particularly from the point of view of increasing the transconductance value. Three techniques have been discussed in increasing the value of the transconductance (g_m). The advantages of using the NCMOS current mirror over the regular current mirrors in minimization of area and DC power consumption are established. A detailed analysis of the OTA has been given. The small signal transfer function of the proposed OTA circuit has been derived to determine the 3dB frequency of this circuit. Finally comparison tables

between three designs of OTA, for different performance, characteristics, are given to provide a good idea of the advantages of using the NCMOS current mirrors in analog VLSI circuits. The values given in tables 4.1 to 4.3 have been derived from the HSPICE, H9007 simulator for the 3 micron technology.

Table 4.1
Comparison between the area, DC power consumption and transconductance
under the same maximum DC output current.

OTA CIRCUIT MODEL	MOSFETs TOTAL AREA (no. of min. size transistors)	MAXIMUM DC OUTPUT CURRENT (μ A)	POWER CONSUMPTION (mW)	OTA Transconductance μ S
model #1 (NCMOS)	20	36	0.46	53.7
model #2	22	36	0.73	48
model #3	34	36	0.46	55

Table 4.2
Percent increase in total chip area and power consumption when using
the regular current mirror models over the NCMOS models (from HSPICE simulator).

OTA CIRCUIT MODEL	PERCENT INCREASE IN TOTAL AREA (no. of minimum size transistors) compare to model #1	PERCENT INCREASE IN MAXIMUM OUTPUT CURRENT (μ A)	PERCENT INCREASE IN POWER CONSUMPTION (mW)
model #2	+10%	0%	+49%
model #3	+70%	0%	0%

Table 4.3
A comparison in frequency response and input voltage range of
the three models of current mirrors (from HSPICE simulator).

OTA CIRCUIT MODEL	3dB frequency (MHz)	Cut off frequency (MHz)	input voltage range (V)
model #1 (NCMOS)	71.3	326	0.8
model #2	161	405	0.5
model #3	36	264	0.65

91x100um

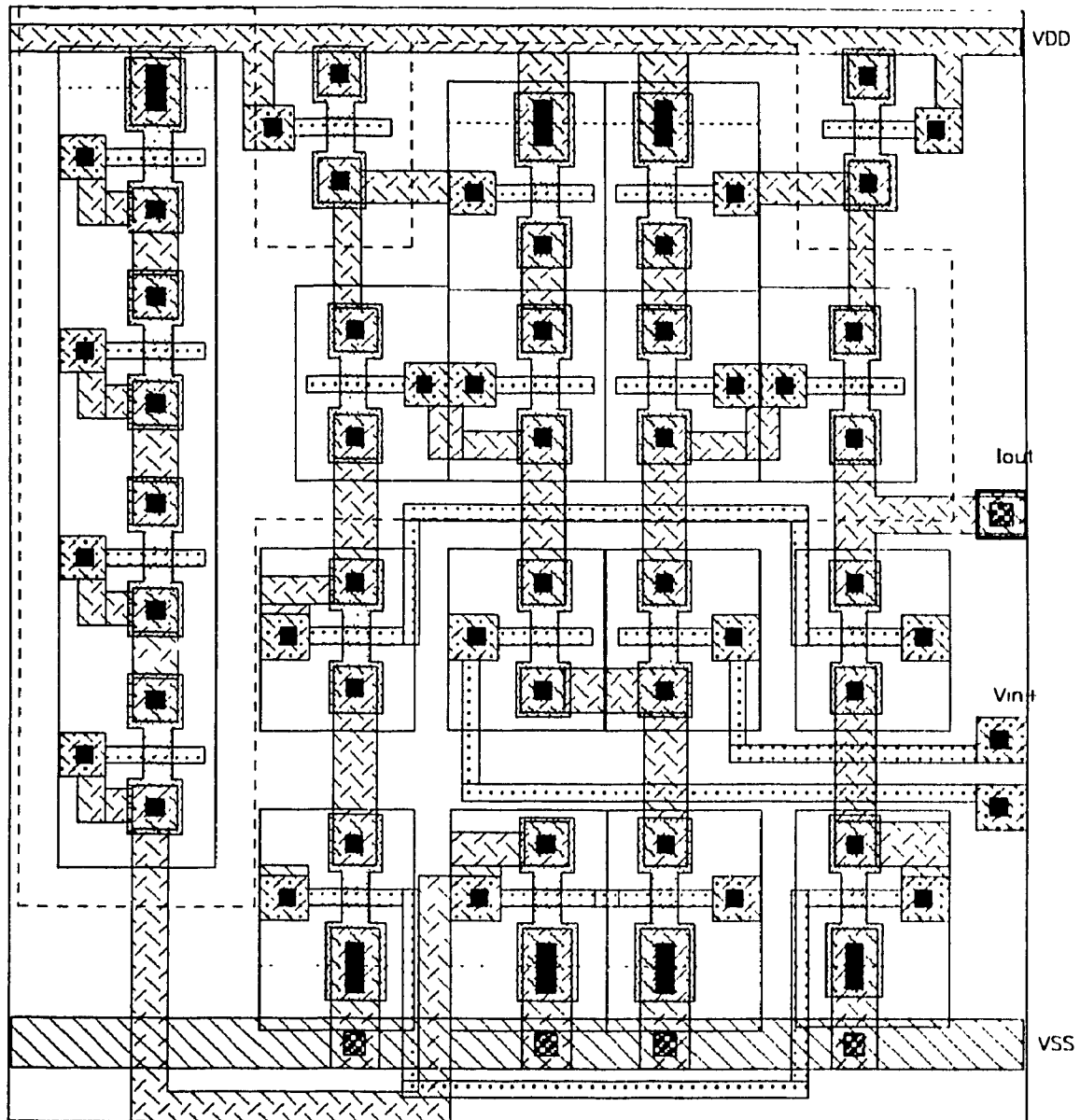


Fig. 4.8

A VLSI Layout for the OTA Using NCMOS current mirrors with grounded substrate.

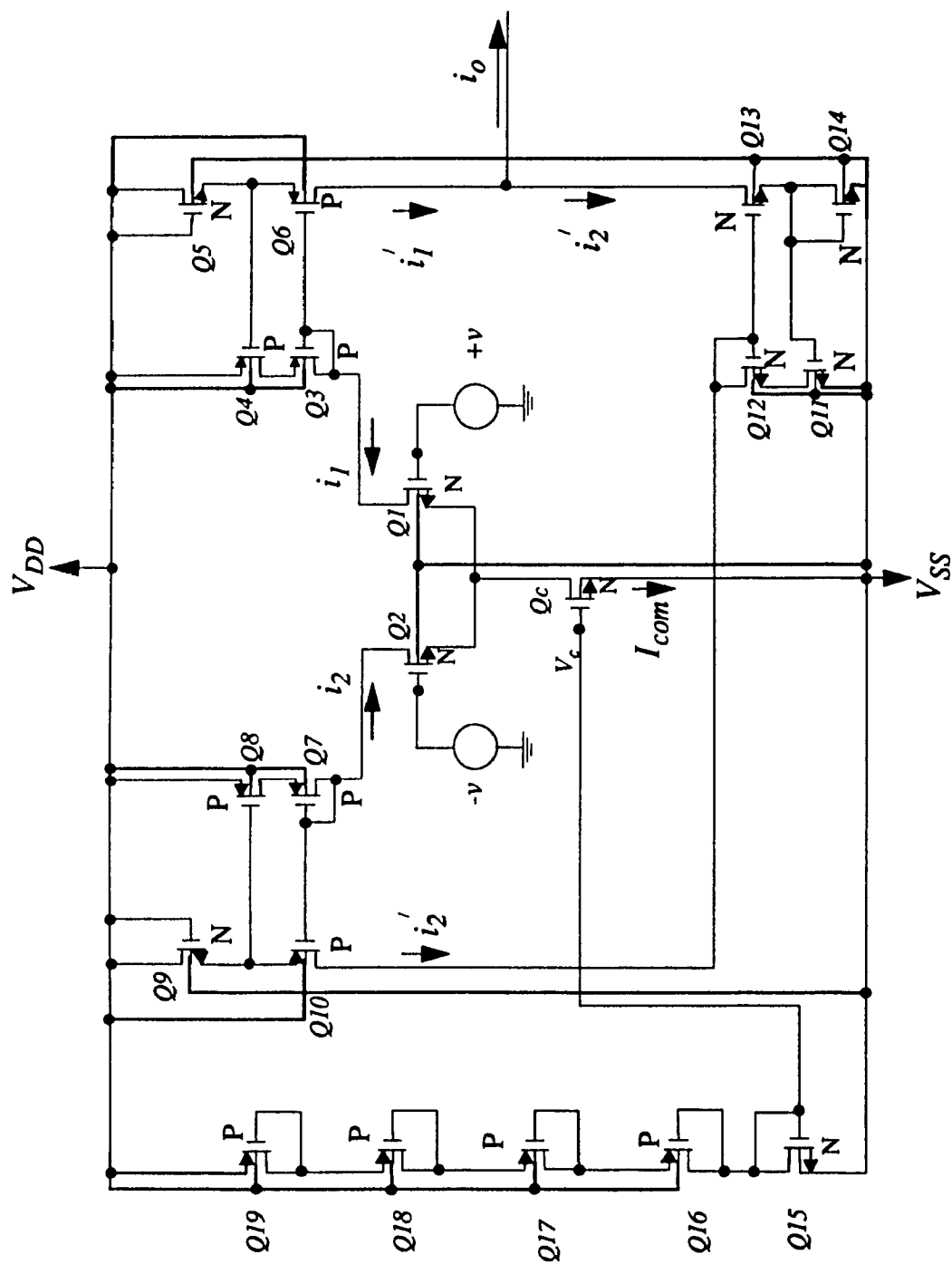


Fig. 4.9
Circuit Diagram for OTA layout of Fig 4.8 using the grounded substrate

CHAPTER 5

CONCLUSION AND FUTURE WORK

This thesis presents novel current mirror designs for efficient implementation in VLSI MOS technology. Two main factors are generally considered in VLSI design of a chip, i.e., the area and the anticipated power consumption of the chip. Consequently, the minimization of the above two parameters in the VLSI design of NCMOS current mirrors has been considered.

In this thesis, twelve different current mirrors (sinks & sources) with current ratio greater than as well as less than unity, have been presented. The process of obtaining these structures follows an approach that eliminates the mask misalignment effects and reduces the area of the current mirror simultaneously. The design technique is portable in the sense that it can be applied to any present or future VLSI technology of any size.

The analysis and simulation of the twelve different current mirror circuits considered in chapter 2 have established a methodology of using the K - factor in designing an “NCMOS current mirror” with minimum area. The stability of NCMOS current mirror circuit designs has been improved by 10% to 20% when employing negative feedback profitably. Further modifications in the design have been proposed to improve the performance of these circuits.

Analysis of the output impedance shows that the last six NCMOS current mirrors are superior to the first six because of their output stage designs. These output stages do not have any diode-connected MOSFET. A set of numerical results as given in Table 2.5 shows that the last six NCMOS current mirrors have output impedances in the range of 43.84 M Ω to 297.16 M Ω , while for the first six their range lies between 2 M Ω and 18.79 M Ω .

A statistical study of the errors in the output current, caused by time-independent random differences in the parameters of the MOSFET device, has been carried out. The two most important time-independent parameters, the transconductance and threshold voltage, are selected for this study. This study shows that, due to device type and the K factor ratio of the NCMOS current mirror, the percentage error in output current of the NCMOS current mirrors with a current gain greater than unity is higher than the one with current gain less than unity. The maximum percentage error in output current due to device mismatch is approximately 4.8% and 16.2% for current mirrors with gains less than unity and greater than unity, respectively.

An implementation technique suggesting an industrial fabrication of these NCMOS current mirror circuits has been discussed.

A method of increasing the current gain of the NCMOS current mirrors by cascading them has been presented. A voltage control technique has also been described for varying the current ratio of the NCMOS current mirror circuits. The analysis and simulation of these NCMOS current mirrors with their control circuits show the effectiveness of the technique in controlling the output current. Four circuits are selected, based on their superior performance, to show the analysis in details. However, tabular analysis results have been provided in tabular form for all the circuits. Analysis and HSPICE simulation results show that most of these NCMOS current mirrors have good response to the control technique. The output current can be reduced to 2% of its maximum value as a best case while the control MOSFET stays in saturation region.

An application of the NCMOS current mirrors has been considered in the design of an OTA circuit. The special structure of an OTA, shown in Fig. 4.3 has been discussed with regard to its advantages over the old structure from the point of view of increasing the transconductance without affecting the dynamic range of operation. Three techniques have been shown to increase the value of the transconductance (g_m). The advantages of using the

NCMOS current mirror instead of the conventional current mirrors in reducing area and DC power consumption have been shown clearly. An AC analysis with the small signal model has been used to derive the transfer function of the OTA circuit and then to determine the 3-dB frequency of this circuit. Finally, a table comparing the three models has been given that shows the advantages in saving area and power when using the NCMOS current mirrors in analog VLSI circuit design.

A layout of the OTA circuit using a single-well, 1.2 μm technology has been developed to show the suggested MOSFET cells structure and its advantage over the conventional cells. The single-well technology has been used instead of the twin-tub because the latter technology is not supported by the facilities provided by the CMC (Canadian Microelectronic Corporation). The limitations of the proposed NCMOS current mirrors comes through the nonlinearity at low current level, the fixed current gain and the well capacitance of the MOSFETs used.

FUTURE WORK

The current mirror models proposed in this thesis can be used to enhance the performance of various circuit designs. In this thesis we have considered an application, namely for a *continuous-time* OTA circuit design.

A *discrete-time*[27] control technique is suggested for future investigation in order to perform a linear controllable g_m from the OTA.

Another challenging area in VLSI technology is neural network based analog implementation [28-33]. The study of the design of a *current mode neuron* can be done based on using the NCMOS current mirrors. This will improve the structure of the neural network. Still there are a few problems related to the minimization of chip area and power consumption, which has to be tackled if the current mirror design is to be optimized. This, however, will require a further investigation and research.

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APPENDICES

APPENDIX A

HSPICE AND FORTRAN-77 PROGRAMS

A.0 INTRODUCTION

This Appendix consists of two parts. The first part will cover the programs used as an aid to analysis in getting data of current mirrors parameters. These programs are written in FORTRAN77 language. It translates the equations given in Tables 2.1 and 3.1 into data to for the seek of obtaining the transfer functions graphs using the X-graph software. It is also used to find a numerical values for the control voltage bounds for each of these CMOS current mirrors.

The second part consist the HSPICE simulating programs for these CMOS current mirrors and their control circuits to get there response according to the MOSFETs models implemented inside the HSPICE simulator. It also include the ac simulating program for the OTA model given in Chapter 4.

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type Ia CMOS current mirror.

```

* vgs1=vgs2=vds1=vr
  read(5,7) Ir
7   format (f6.2 )
  write (6,*) ' Ir1 Ratio '
  write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .81 , 4.26 , .001
      x1 = 6* ((vr - .8)**2)*(1 + .03* vr)
      if (abs(aIr-x1).gt.0.01) goto 21
*assume the voltage Vds=10 volts. which is nearest to the spice simulation
      y1 = 20* ((vr - .7)**2)*(1 + .01* 10)
      a1 = y1 / aIr
      Ratio = 0.3 * a1
    write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
    goto 20
21   continue
20  continue
    stop
    end

```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type Ib CMOS current mirror.

```

* vgs1=vgs2=vds1=vr
  read(5,7) aIr
7   format (f6.2 )
  write (6,*) ' Ir2 Ratio '
  write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .71 , 2.36 , .01
      x2 = 20* ((vr - .7)**2)*(1 + .01* vr)
      if (abs(aIr-x2).gt.0.1) goto 21
*Assuming Vsd2=10 volts, which is the nearest value to spice simulation.
      y2 = 6* ((vr - .8)**2)*(1 + .03* 10)
      a2 = y2 / aIr
      Ratio = 3.33 * a2
    write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
    goto 20
21   continue
20  continue
    stop
    end

```


*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type IIa CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) aIr
7   format (f6.2 )
write (6,*) ' Ir3 Ratio '
  write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
  do 21 vr = .71 , 2.36 , .005
    x3 = 20*((vr - .7)**2)*(1 + .01*(1.55*vr - .44 + .7))
    if (abs(aIr-x3).gt.0.1) goto 21
    y3 = 6* ((vr - .8)**2)*(1 + .03* vr)
    a3 = y3 / aIr
    Ratio = 3.33 * a3
  write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
    goto 20
21   continue
20   continue
    stop
    end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type IIb CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) Ir
7   format (f6.2 )
write (6,*) ' Ir Ratio '
  write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
  do 21 vr = .81 , 4.26 , .01
    x4 = 6* ((vr - .8)**2)*(1 + .03*(2.82* vr - 0.48))
    if (abs(aIr-x4).gt.0.1) goto 21
    y4 = 20* ((vr - .7)**2)*(1 + .01* vr)
    a4 = y4 / aIr
    Ratio = 0.3 * a4
  write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
    goto 20
21   continue
20   continue
    stop
    end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type IIIa CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) aIr
7   format (f6.2 )
    write (6,*) ' Ir5 Ratio '
    write (6,*) ' --- ----- '
    do 20 aIr = 1 , 70 , 1
      do 21 vr = .71 , 2.96 , .001
        x5 = 20*((vr - .7)**2)*(1 + .01*(.55*vr - .44 + .7))
        if (abs(aIr-x5).gt.0.05) goto 21
        y5 = 6* ((vr - .8)**2)*(1 + .03* vr)
        a5 = y5 / aIr
        Ratio = 3.33 * a5
        write (6,25) aIr , Ratio
25    format ( f8.4, 4x, f6.3)
      goto 20
21    continue
20    continue
    stop
  end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type IIIb CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) Ir
7   format (f6.2 )
  write (6,*) ' Ir Ratio '
  write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .81 , 4.26 , .01
      x6 = 6* ((vr - .8)**2)*(1 + .03*(1.82*(vr-.7) + .8))
      if (abs(aIr-x6).gt.0.1) goto 21
      y6 = 20* ((vr - .7)**2)*(1 + .01* vr)
      a6 = y6 / aIr
      Ratio = 0.3 * a6
      write (6,25) aIr , Ratio
25    format ( f8.4, 4x, f6.3)
    goto 20
21    continue
20    continue
  stop
  end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type IVa CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) Ir
7   format (f6.2 )
   write (6,*) ' Ir Ratio '
   write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .81 , 4.26 , .01
      x7 = 6* ((vr - .8)**2)*(1 + .03* vr)
      if (abs(aIr-x7).gt.0.1) goto 21
      y7 = 20* ((vr - .7)**2)*(1 + .01* vr)
      a7 = y7 / aIr
      Ratio = 0.3 * a7
      write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
      goto 20
21   continue
20  continue
    stop
  end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type IVb CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) aIr
7   format (f6.2 )
   write (6,*) ' Ir8 Ratio '
   write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .71 , 2.36 , .01
      x8 = 20* ((vr - .7)**2)*(1 + .01* vr)
      if (abs(aIr-x8).gt.0.1) goto 21
      y8 = 6* ((vr - .8)**2)*(1 + .03* vr)
      a8 = y8 / aIr
      Ratio = 3.33 * a8
      write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
      goto 20
21   continue
20  continue
    stop
  end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type V CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) Ir
7   format (f6.2 )
   write (6,*) ' Ir9 Ratio'
   write (6,*) ' --- -----'
  do 20 aIr = 1 , 70 , 1
  do 21 vr = .81 , 4.26 , .01
    x9 = 6* ((vr - .8)**2)*(1 + .03* vr)
    if (abs(aIr-x9).gt.0.1) goto 21
    y9 = 20* ((vr - .7)**2)*(1 + .01*(vr + .55*(vr-.8) +.7))
    a9 = y9 / aIr
    Ratio = 0.3 * a9
    write (6,25) aIr , Ratio
25   format ( f8.4 , 4x , f8.4)
    goto 20
21  continue
20  continue
    stop
    end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type VI CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) aIr
7   format (f6.2 )
   write (6,*) ' Ir10 Ratio '
   write (6,*) ' --- -----'
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .71 , 2.96 , .001
      x10 = 20*((vr - .7)**2)*(1 + .01*(.55*vr - .44 + .7))
      if (abs(aIr-x10).gt.0.05) goto 21
      y10 = 6* ((vr - .8)**2)*(1 + .03*2* vr)
      a10 = y10 / aIr
      Ratio = 3.33 * a10
      write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
      goto 20
21  continue
20  continue
    stop
    end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type VII CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) Ir
7   format (f6.2 )
  write (6,*) ' Ir Ratio '
  write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .81 , 4.26 , .01
      x11 = 20* ((vr - .7)**2)*(1 + .01* vr)
      if (abs(aIr-x11).gt.0.1) goto 21
      z11 = sqrt((1+ .01*vr)/(1 + .03*2*vr))
      y11 = 6* ((vr - .8)**2)*(1 + .03*(vr + .55*(vr-.7)*z11 +.8))
      a11 = y11 / aIr
      Ratio = 3.33 * a11
      write (6,25) aIr , Ratio
25   format ( f8.4, 4x, f6.3)
      goto 20
21   continue
20  continue
  stop
end
```

*Program to find the Ratio = I_o/I_r for current range 1 to 70uA for Type VIII CMOS current mirror.

```
* vgs1=vgs2=vds1=vr
  read(5,7) Ir
7   format (f6.2 )
  write (6,*) ' Ir Ratio Ratio2'
  write (6,*) ' --- ----- '
  do 20 aIr = 1 , 70 , 1
    do 21 vr = .81 , 4.26 , .01
      x12 = 6* ((vr - .8)**2)*(1 + .03*(2.82* vr - 0.48))
      if (abs(aIr-x12).gt.0.1) goto 21
      y12 = 20* ((vr - .7)**2)*(1 + .01 * 2 * vr)
      a12 = y12 / aIr
      b12 = y12 / x12
      Ratio = 0.3 * a12
      Ratio2 = 0.3 * b12
      write (6,25) aIr , Ratio , Ratio2
25   format ( f8.4, 4x, f6.3, 4x, f6.3)
      goto 20
21   continue
20  continue
  stop
end
```

```

* THIS PROGRAM TEST THE C.M. UNDER THE ASSUMPTION OF EQUAL THRESHOLD
VOLTAGES *
* THIS IS FOR CIRCUITS WITH GAIN GRATER THAN UNITY ***
* THE SQUARE FACTORS WILL BE CANCELLED FROM THE RATIO FACTORS
*** Program to find the Io/ K.Ir current ratio with Ir for ccts with cur-
rent gain grater than unity.
    read (5,1) vr
1    format(f8.4)
*    vr=1
    vt=.8
*Type Ia CMOS current mirror.
    do 18 vr1 = 0.81 , 4 , .05
        a1=(vr1-vt)**2
            oI1=20*a1*(1+.01*10)
            rI1=6*a1*(1+.03*vr1)
            b1=oI1/(rI1*3.34)
    write(6,12) rI1,b1
12    format(2(f8.3,3x))
18    continue
    write(6,*)' Type Ia '
    write(6,*)' Ir      ratio '
* Type IIb CMOS current mirror.
    do 48 vr4 = 0.81 , 4 , .05
        a4=(vr4-vt)**2
            oI4=20*a4*(1+.01*vr4)
            rI4=6*a4*(1+.03*(2.82*vr4-.82*vt))
            b4=oI4/(rI4*3.33)
    write(6,42) rI4,b4
42    format(2(f8.3,3x))
48    continue
    write(6,*)' Type IIb '
    write(6,*)' Ir      ratio '
* Type IIIb CMOS current mirror.
    do 68 vr6 = 0.81 , 4 , .05
        a6=(vr6-vt)**2
            oI6=20*a6*(1+.01*vr6)
            rI6=6*a6*(1+.03*(1.82*vr6-.82*vt))
            b6=oI6/(rI6*3.33)
    write(6,62) rI6,b6
62    format(2(f8.3,3x))
68    continue
    write(6,*)' Type IIIb '
    write(6,*)' Ir      ratio '
* Type IVa CMOS current mirror.
    do 78 vr7 = 0.81 , 4 , .05
        a7=(vr7-vt)**2
            oI7=20*a7*(1+.01*vr7)
            rI7=6*a7*(1+.03*vr7)
            b7=oI7/(rI7*3.33)
    write(6,72) rI7,b7
72    format(2(f8.3,3x))
78    continue
    write(6,*)' Type IVa '
    write(6,*)' Ir      ratio '

```

```

* Type V CMOS current mirror.
do 98 vr9 = 0.81 , 4 , .05
  a9=(vr9-vt)**2
    oI9=20*a9*(1+.01*(1.55*vr9+.45*vt))
    rI9=6*a9*(1+.03*vr9)
    b9= oI9/(rI9*3.33)
  write(6,92) rI9,b9
92  format(2(f8.3,3x))
98  continue
  write(6,*)' Type V '
  write(6,*)' Ir   ratio '

* Type VII CMOS current mirror.
do 128 vrl2 = 0.81 , 4 , .05
  a12=(vrl2-vt)**2
    oI12=20*a12*(1+.01*2*vrl2)
    rI12=6*a12*(1+.03*(vrl2+1.82*(vrl2-vt)+vt))
    b12=oI12/(rI12*3.33)
  write(6,122) rI12,b12
122 format(2(f8.3,3x))
128 continue
  write(6,*)' Type VII '
  write(6,*)' Ir   ratio '
  stop
end

```

```

* THIS PROGRAM TEST C.M. UNDER THE ASSUMPTION OF EQUAL THRESHOLD VOLTAGES
*
* THIS PROGRAM FOR CIRCUITS WITH GAIN LESS THAN UNITY *
* THE SQUARE FACTORS WILL BE CANCELLED FROM THE RATIO FACTORS
*** Program to find the following relations :
*** 1-  $I_o/I_r$  ratio with  $I_r$  for ccts 3 to 12
*** 2-  $f_1(v_r)$  with  $I_r$  for ccts 3 to 12
    read (5,1) vr
1    format(f8.4)
*    vr=1
    vt=.8
* Type IbCMOS current mirror.
    do 28 vr2 = 0.81 , 3 , .05
        a2=(vr2-vt)**2
        oI2=6*a2*(1+.03*10)
        rI2=20*a2*(1+.01*vr2)
        b2=oI2/(rI2*0.3)
        write(6,22) rI2,b2
22    format(2(f8.3,3x))
28    continue
    write(6,*)' Type Ib `
    write(6,*)' Ir   ratio `
*Type IIa CMOS current mirror.
    do 38 vr3 = 0.81 , 3 , .05
        a3=(vr3-vt)**2
        oI3=6*a3*(1+.03*vr3)
        rI3=20*a3*(1+.01*(1.55*vr3+.45*vt))
        b3=oI3/(rI3*.3)
        write(6,32) rI3,b3
32    format(2(f8.3,3x))
38    continue
    write(6,*)' Type IIa `
    write(6,*)' Ir   ratio `
* Type IIIa CMOS current mirror.
    do 58 vr5 = 0.81 , 3 , .05
        a5=(vr5-vt)**2
        oI5=6*a5*(1+.03*vr5)
        rI5=20*a5*(1+.01*(.55*vr5+.45*vt))
        b5=oI5/(rI5*.3)
        write(6,52) rI5,b5
52    format(2(f8.3,3x))
58    continue
    write(6,*)' Type IIIa `
    write(6,*)' Ir   ratio `
* Type IVb CMOS current mirror.
    do 88 vr8 = 0.81 , 3 , .05
        a8=(vr8-vt)**2
        oI8=6*a8*(1+.03*vr8)
        rI8=20*a8*(1+.01*vr8)
        b8=oI8/(rI8*.3)
        write(6,82) rI8,b8
82    format(2(f8.3,3x))
88    continue

```



```

        write(6,*)' Type IVb '
        write(6,*)' Ir ratio '
* Type VI CMOS current mirror.
        do 108 vr10 = 0.81 , 3 , .05
            a10=(vr10-vt)**2
            oI10=6*a10*(1+.03*2*vr10)
            rI10=20*a10*(1+.01*(1.55*vr10+.45*vt))
            b10=oI10/(rI10*.3)
        write(6,102) rI10,b10
102    format(2(f8.3,3x))
108    continue
        write(6,*)' Type VI '
        write(6,*)' Ir ratio '
* Type VIII CMOS current mirror.
        do 118 vr11 = 0.81 , 3 , .05
            a11=(vr11-vt)**2
            f=((1+.01*vr11)/(1+.06*vr11))**.5
            oI11=6*a11*(1+.03*(vr11+1.82*f*(vr11-vt)+vt))
            rI11=20*a11*(1+.01*vr11)
            b11=oI11/(rI11*.3)
        write(6,112) rI11,b11
112    format(2(f8.3,3x))
118    continue
        write(6,*)' Type VIII '
        write(6,*)' Ir ratio '
        stop
        end

```

```

* HSPICE program to test the variation of Io wrt Ir variation for differ-
ent CMOS current mirror (sink) *
*
** HSPICE model for Type Ia CMOS current mirror **
m1 4 4 2 2 p l=3u w=3u
m2 5 2 4 4 n l=3u w=3u
*
** HSPICE model for Type IIa CMOS current mirror **
m31 32 33 4 4 n l=3u w=3u
m32 4 4 33 33 p l=3u w=3u
m33 35 32 33 33 n l=3u w=3u
*
** HSPICE model for Type IIIa CMOS current mirror **
m21 26 23 4 4 n l=3u w=3u
m22 4 4 23 23 p l=3u w=3u
m23 25 22 23 23 n l=3u w=3u
m24 22 22 26 26 n l=3u w=3u
*
** HSPICE model for Type IVa CMOS current mirror **
m11 4 4 16 16 p l=3u w=3u
m12 13 16 4 4 n l=3u w=3u
m13 15 12 13 13 n l=3u w=3u
m14 16 16 12 12 p l=3u w=3u
*mc1 12 7 1 1 p l=3u w=3u
*
** HSPICE model for Type V CMOS current mirror **
m41 4 4 46 46 p l=3u w=3u
m42 43 46 4 4 n l=3u w=3u
m43 45 42 43 43 n l=3u w=3u
m44 42 43 46 46 n l=3u w=3u
*
** HSPICE model for Type VI CMOS current mirror **
m51 56 56 4 4 n l=3u w=3u
m52 4 56 53 53 p l=3u w=3u
m53 55 52 53 53 n l=3u w=3u
m54 52 53 56 56 n l=3u w=3u
*
.MODEL p PMOS (LEVEL=2 VTO=-0.8 KP=12E-6 GAMMA=0.6 PHI=0.6 LAMBDA=0.03
+ RD=100 RS=100 PB=0.6 CGSO=2.5E-10 CGDO=2.5E-10 CGBO=5.0E-10 RSH=80
+ CJ=1.5E-4 MJ=0.6 CJSW=4.0E-10 MJSW=0.6 JS=1.0E-5 TOX=5.0E-8 NSUB=5.0E15
+ NSS=0 NFS=0 TPG=1 XJ=5.0E-7 LD=2.5E-7 UO=250 VMAX=0.7E5)
*
.MODEL n NMOS (LEVEL=2 VTO=0.7 KP=40E-6 GAMMA=1.1 PHI=0.6 LAMBDA=0.01
+ RD=40 RS=40 PB=0.7 CGSO=3.0E-10 CGDO=3.0E-10 CGBO=5.0E-10 RSH=25
+ CJ=4.4E-4 MJ=0.5 CJSW=4.0E-10 MJSW=0.3 JS=1.0E-5 TOX=5.0E-8
+ NSUB=1.7E16 NSS=0 NFS=0 TPG=1 XJ=6.0E-7 LD=3.5E-7 UO=775 VMAX=1.0E5)
*
vdd 1 0 dc 5
vss 4 0 dc -5
*
vio1 1 5
vio3 1 35
vio5 1 25
vio7 1 15
vio9 1 45
violf 1 55
*
vic0 7 2
vic1 17 12
vic2 27 22
vic3 37 32
vic4 47 42
vic5 57 52
*

```

```
irc0 1 7 pwl(0 0 10us 10u 300us 300u)
irc1 1 17 pwl(0 0 10us 10u 300us 300u)
irc2 1 27 pwl(0 0 10us 10u 300us 300u)
irc3 1 37 pwl(0 0 10us 10u 300us 300u)
irc4 1 47 pwl(0 0 10us 10u 300us 300u)
irc5 1 57 pwl(0 0 10us 10u 300us 300u)
.tran 1us 300us
.option nomod limpts=4000
.option post dcon=2
.end
```

```

* HSPICE program to test the variation of Io wrt Ir variation for differ-
ent CMOS current mirrors (source) *
** HSPICE model for Type Ib CMOS current mirror **
m1 4 4 2 2 n l=3u w=3u
m2 5 2 4 4 p l=3u w=3u
**
** HSPICE model for Type IIb CMOS current mirror **
m31 32 33 4 4 p l=3u w=3u
m32 4 4 33 33 n l=3u w=3u
m33 35 32 33 33 p l=3u w=3u
**
** HSPICE model for Type IIIb CMOS current mirror **
m21 26 23 4 4 p l=3u w=3u
m22 4 4 23 23 n l=3u w=3u
m23 25 22 23 23 p l=3u w=3u
m24 22 22 26 26 p l=3u w=3u
**
** HSPICE model for Type IVb CMOS current mirror **
m11 4 4 16 16 n l=3u w=3u
m12 13 16 4 4 p l=3u w=3u
m13 15 12 13 13 p l=3u w=3u
m14 16 16 12 12 n l=3u w=3u
**
** HSPICE model for Type VII CMOS current mirror **
m41 4 4 46 46 n l=3u w=3u
m42 43 46 4 4 p l=3u w=3u
m43 45 42 43 43 p l=3u w=3u
m44 42 43 46 46 p l=3u w=3u
**
** HSPICE model for Type VIII CMOS current mirror **
m51 56 56 4 4 p l=3u w=3u
m52 4 56 53 53 n l=3u w=3u
m53 55 52 53 53 p l=3u w=3u
m54 52 53 56 56 p l=3u w=3u
*
.MODEL p PMOS ( LEVEL=2 VTO=-0.8 KP=12E-6 GAMMA=0.6 PHI=0.6 LAMBDA=0.03
+ RD=100 RS=100 PB=0.6 CGSO=2.5E-10 CGDO=2.5E-10 CGBO=5.0E-10 RSH=80
+ CJ=1.5E-4 MJ=0.6 CJSW=4.0E-10 MJSW=0.6 JS=1.0E-5 TOX=5.0E-8 NSUB=5.0E15
+ NSS=0 NFS=0 TPG=1 XJ=5.0E-7 LD=2.5E-7 UO=250 VMAX=0.7E5 )
*
.MODEL n NMOS (LEVEL=2 VTO=0.7 KP=40E-6 GAMMA=1.1 PHI=0.6 LAMBDA=0.01
+ RD=40 RS=40 PB=0.7 CGSO=3.0E-10 CGDO=3.0E-10 CGBO=5.0E-10 RSH=25
+ CJ=4.4E-4 MJ=0.5 CJSW=4.0E-10 MJSW=0.3 JS=1.0E-5 TOX=5.0E-8
+ NSUB=1.7E16 NSS=0 NFS=0 TPG=1 XJ=6.0E-7 LD=3.5E-7 UO=775 VMAX=1.0E5)
vdd 4 0 dc 5
vss 1 0 dc -5
*
vio2 5 1
vio4 35 1
vio6 25 1
vio8 15 1
vio11 45 1
vio12 55 1
*
vic0 2 7
vic1 12 17
vic2 22 27
vic3 32 37
vic4 42 47
vic5 52 57
*
irc0 7 1 pwl(0 0 10us 10u 300us 300u)
irc1 17 1 pwl(0 0 10us 10u 300us 300u)
irc2 27 1 pwl(0 0 10us 10u 300us 300u)

```

```
irc3 37 1 pwl(0 0 10us 10u 300us 300u)
irc4 47 1 pwl(0 0 10us 10u 300us 300u)
irc5 57 1 pwl(0 0 10us 10u 300us 300u)
*
.tran 1us 300us
.option nomod limpts=4000
.option post dcon=2
.end
```

```

* HSPICE program to test the variation of Io wrt Vc variation for differ-
ent CMOS current mirror (sink)*
* This program for the controllable CMOS current mirror.
*
** HSPICE model for Type Ia CMOS current mirror **
m1 4 4 2 2 p l=3u w=3u
m2 5 2 4 4 n l=3u w=3u
mc 2 7 4 4 n l=3u w=3u
*
** HSPICE model for Type IIa CMOS current mirror **
m31 32 33 4 4 n l=3u w=3u
m32 4 4 33 33 p l=3u w=3u
m33 35 32 33 33 n l=3u w=3u
mc3 32 37 4 4 n l=3u w=3u
*
** HSPICE model for Type IIIa CMOS current mirror **
m21 26 23 4 4 n l=3u w=3u
m22 4 4 23 23 p l=3u w=3u
m23 25 22 23 23 n l=3u w=3u
m24 22 22 26 26 n l=3u w=3u
mc2 22 27 4 4 n l=3u w=3u
*
** HSPICE model for Type IVa CMOS current mirror **
m11 4 4 16 16 p l=3u w=3u
m12 13 16 4 4 n l=3u w=3u
m13 15 12 13 13 n l=3u w=3u
m14 16 16 12 12 p l=3u w=3u
mc1 12 17 4 4 n l=3u w=3u
*
** HSPICE model for Type V CMOS current mirror **
m41 4 4 46 46 p l=3u w=3u
m42 43 46 4 4 n l=3u w=3u
m43 45 42 43 43 n l=3u w=3u
m44 42 43 46 46 n l=3u w=3u
mc4 42 47 4 4 n l=3u w=3u
*
** HSPICE model for Type VI CMOS current mirror **
m51 56 56 4 4 n l=3u w=3u
m52 4 56 53 53 p l=3u w=3u
m53 55 52 53 53 n l=3u w=3u
m54 52 53 56 56 n l=3u w=3u
mc5 52 57 4 4 n l=3u w=3u
*
.MODEL p PMOS ( LEVEL=2 VTO=-0.8 KP=12E-6 GAMMA=0.6 PHI=0.6 LAMBDA=0.03
+ RD=100 RS=100 PB=0.6 CGSO=2.5E-10 CGDO=2.5E-10 CGBO=5.0E-10 RSH=80
+ CJ=1.5E-4 MJ=0.6 CJSW=4.0E-10 MJSW=0.6 JS=1.0E-5 TOX=5.0E-8 NSUB=5.0E15
+ NSS=0 NFS=0 TPG=1 XJ=5.0E-7 LD=2.5E-7 UO=250 VMAX=0.7E5 )
*
.MODEL n NMOS (LEVEL=2 VTO=0.7 KP=40E-6 GAMMA=1.1 PHI=0.6 LAMBDA=0.01
+ RD=40 RS=40 PB=0.7 CGSO=3.0E-10 CGDO=3.0E-10 CGBO=5.0E-10 RSH=25
+ CJ=4.4E-4 MJ=0.5 CJSW=4.0E-10 MJSW=0.3 JS=1.0E-5 TOX=5.0E-8
+ NSUB=1.7E16 NSS=0 NFS=0 TPG=1 XJ=6.0E-7 LD=3.5E-7 UO=775 VMAX=1.0E5)
vdd 1 0 dc 5
vss 4 0 dc -5
*
vio1 1 5
vio3 1 35
vio5 1 25
vio7 1 15
vio9 1 45
vio10 1 55
*
vic0 8 2
vic1 18 12

```

```
vic2 28 22
vic3 38 32
vic4 48 42
vic5 58 52
*
irc0 1 8 dc 40u
irc1 1 18 dc 40u
irc2 1 28 dc 120u
irc3 1 38 dc 120u
irc4 1 48 dc 40u
irc5 1 58 dc 120u
*
vc0 7 4 pwl(0 0 10us 1v 500us 5v)
vc1 17 4 pwl(0 0 10us 1v 500us 5v)
vc2 27 4 pwl(0 0 10us 1v 500us 5v)
vc3 37 4 pwl(0 0 10us 1v 500us 5v)
vc4 47 4 pwl(0 0 10us 1v 500us 5v)
vc5 57 4 pwl(0 0 10us 1v 500us 5v)
*
.tran 5us 500us
.option nomod limpts=4000
.option post dcon=2
.end
```

```

* HSPICE program to test the variation of Io wrt Vc variation for differ-
ent CMOS current mirror (source)*
* This program for the controllable CMOS current mirror.
*****
*
** HSPICE model for Type Ib CMOS current mirror **
m1 4 4 2 2 n l=3u w=3u
m2 5 2 4 4 p l=3u w=3u
mc0 2 7 4 4 p l=3u w=3u
*
** HSPICE model for Type IIb CMOS current mirror **
m31 32 33 4 4 p l=3u w=3u
m32 4 4 33 33 n l=3u w=3u
m33 35 32 33 33 p l=3u w=3u
mc3 32 37 4 4 p l=3u w=3u
*
** HSPICE model for Type IIIb CMOS current mirror **
m21 26 23 4 4 p l=3u w=3u
m22 4 4 23 23 n l=3u w=3u
m23 25 22 23 23 p l=3u w=3u
m24 22 22 26 26 p l=3u w=3u
mc2 22 27 4 4 p l=3u w=3u
*
** HSPICE model for Type IVb CMOS current mirror **
m11 4 4 16 16 n l=3u w=3u
m12 13 16 4 4 p l=3u w=3u
m13 15 12 13 13 p l=3u w=3u
m14 16 16 12 12 n l=3u w=3u
mc1 12 17 4 4 p l=3u w=3u
*
*** HSPICE model for Type VII CMOS current mirror **
m41 4 4 46 46 n l=3u w=3u
m42 43 46 4 4 p l=3u w=3u
m43 45 42 43 43 p l=3u w=3u
m44 42 43 46 46 p l=3u w=3u
mc4 42 47 4 4 p l=3u w=3u
*
** HSPICE model for Type VIII CMOS current mirror **
m51 56 56 4 4 p l=3u w=3u
m52 4 56 53 53 n l=3u w=3u
m53 55 52 53 53 p l=3u w=3u
m54 52 53 56 56 p l=3u w=3u
mc5 52 57 4 4 p l=3u w=3u
vio12 55 1
*
*
.MODEL p PMOS ( LEVEL=2 VTO=-0.8 KP=12E-6 GAMMA=0.6 PHI=0.6 LAMBDA=0.03
+ RD=100 RS=100 PB=0.6 CGSO=2.5E-10 CGDO=2.5E-10 CGBO=5.0E-10 RSH=80
+ CJ=1.5E-4 MJ=0.6 CJSW=4.0E-10 MJSW=0.6 JS=1.0E-5 TOX=5.0E-8 NSUB=5.0E15
+ NSS=0 NFS=0 TPG=1 XJ=5.0E-7 LD=2.5E-7 UO=250 VMAX=0.7E5 )
*
.MODEL n NMOS (LEVEL=2 VTO=0.7 KP=40E-6 GAMMA=1.1 PHI=0.6 LAMBDA=0.01
+ RD=40 RS=40 PB=0.7 CGSO=3.0E-10 CGDO=3.0E-10 CGBO=5.0E-10 RSH=25
+ CJ=4.4E-4 MJ=0.5 CJSW=4.0E-10 MJSW=0.3 JS=1.0E-5 TOX=5.0E-8
+ NSUB=1.7E16 NSS=0 NFS=0 TPG=1 XJ=6.0E-7 LD=3.5E-7 UO=7/5 VMAX=1.0E5)
*
vdd 4 0 dc 5
vss 1 0 dc -5
*
vio2 5 1
vio4 35 1
vio6 25 1
vio8 15 1
vio11 45 1

```



```
viol2 55 1
*
vic0 2 8
vic1 12 18
vic2 22 28
vic3 32 38
vic4 42 48
vic5 52 58
irc0 8 1 dc 120u
irc1 18 1 dc 120u
irc2 28 1 dc 40u
irc3 38 1 dc 40u
irc4 48 1 dc 120u
irc5 58 1 dc 40u
vc0 7 4 pwl(0 0 10us -1v 700us -7v)
vc1 17 4 pwl(0 0 10us -1v 700us -7v)
vc2 27 4 pwl(0 0 10us -1v 700us -7v)
vc3 37 4 pwl(0 0 10us -1v 700us -7v)
vc4 47 4 pwl(0 0 10us -1v 700us -7v)
vc5 57 4 pwl(0 0 10us -1v 700us -7v)
.tran 5us 700us
.option nomod limpts=4000
.option post dcon=2
.end
```

```

**** operational transconductance amplifier model #1 (CMOS)**
** program to test the ac analysis ****
** designed power; designed gm (output current); designed area ****
** differential pair ****
m1 14 26 8 8 n l=3u w=3u
m2 48 27 8 8 n l=3u w=3u
** current source ****
m10 8 6 25 25 n l=3u w=3u
*** current mirror 1 ***
m20 15 16 1 1 p l=3u w=3u
m21 14 14 15 1 p l=3u w=3u
m22 1 1 16 16 n l=3u w=3u
m23 17 14 16 1 p l=3u w=3u
*** current mirror 2 ***
m24 19 20 1 1 p l=3u w=3u
m25 18 18 19 1 p l=3u w=3u
m26 1 1 20 20 n l=3u w=3u
m27 41 18 20 1 p l=3u w=3u
*** current mirror 3 ***
m28 23 23 25 25 n l=3u w=3u
m29 17 17 23 25 n l=3u w=3u
m30 22 23 25 25 n l=3u w=3u
m31 51 17 22 25 n l=3u w=3u
*****
***
.model p pmos (level=2 vto=-0.8 kp=12e-6 gamma=0.6 phi=0.6 lambda=0.03
+ rd=100 rs=100 pb=0.6 cgso=2.5e-10 cgdo=2.5e-10 cgbo=5.0e-10 rsh=80
+ cj=1.5e-4 mj=0.6 cjsw=4.0e-10 mjsw=0.6 js=1.0e-5 tox=5.0e-8 nsub=5.0e15
+ nss=0 nfs=0 tpg=1 xj=5.0e-7 ld=2.5e-7 uo=250 vmax=0.7e5)
*
.model n nmos (level=2 vto=0.7 kp=40e-6 gamma=1.1 phi=0.6 lambda=0.01
+ rd=40 rs=40 pb=0.7 cgso=3.0e-10 cgdo=3.0e-10 cgbo=5.0e-10 rsh=25
+ cj=4.4e-4 mj=0.5 cjsw=4.0e-10 mjsw=0.3 js=1.0e-5 tox=5.0e-8
+ nsub=1.7e16 nss=0 nfs=0 tpg=1 xj=6.0e-7 ld=3.5e-7 uo=775 vmax=1.0e5)
*****
**
vdd 101 0 dc 5
vss 125 0 dc -5
vc1 6 25 dc 1.35
vn 126 0 ac 1
vp 27 0 dc 0
.ac dec 5 1khz 300meghz
.print i(vio)
.print i(viin)
vidd 101 1
viss 25 125
vip 18 48
vil 41 21
vi2 21 51
vio 21 61
viin 126 26
ro 61 0 100k
*****
.option nomod limpts=4000
.option post dcon=1
.end

```

```

**** operational transconductance amplifier model # 2 **
** program to test the ac analysis ****
** more power; same gm (output current); same area ****
** differential pair ****
m1 14 26 8 8 n l=3u w=3u
m2 48 27 8 8 n l=3u w=3u
** current source ****
m10 8 6 25 25 n l=3u w=3u
*** current mirror 1 ***
m20 15 16 1 1 p l=3u w=3u
m21 14 14 15 1 p l=3u w=3u
m22 16 16 1 1 p l=3u w=3u
m23 17 14 16 1 p l=3u w=3u
*** current mirror 2 ***
m24 19 20 1 1 p l=3u w=3u
m25 18 18 19 1 p l=3u w=3u
m26 20 20 1 1 p l=3u w=3u
m27 41 18 20 1 p l=3u w=3u
*** current mirror 3 ***
m28 23 23 25 25 n l=3u w=3u
m29 17 17 23 25 n l=3u w=3u
m30 22 23 25 25 n l=3u w=3u
m31 51 17 22 25 n l=3u w=3u
*****
***
.model p pmos (level=2 vto=-0.8 kp=12e-6 gamma=0.6 phi=0.6 lambda=0.03
+ rd=100 rs=100 pb=0.6 cgso=2.5e-10 cgdo=2.5e-10 cgbo=5.0e-10 rsh=80
+ cj=1.5e-4 mj=0.6 cjsw=4.0e-10 mjsw=0.6 js=1.0e-5 tox=5.0e-8 nsub=5.0e15
+ nss=0 nfs=0 tpg=1 xj=5.0e-7 ld=2.5e-7 uo=250 vmax=0.7e5)
*
.model n nmos (level=2 vto=0.7 kp=40e-6 gamma=1.1 phi=0.6 lambda=0.01
+ rd=40 rs=40 pb=0.7 cgso=3.0e-10 cgdo=3.0e-10 cgbo=5.0e-10 rsh=25
+ cj=4.4e-4 mj=0.5 cjsw=4.0e-10 mjsw=0.3 js=1.0e-5 tox=5.0e-8
+ nsub=1.7e16 nss=0 nfs=0 tpg=1 xj=6.0e-7 ld=3.5e-7 uo=775 vmax=1.0e5)
*****
**
vdd 101 0 dc 5
vss 125 0 dc -5
vc1 6 25 dc 2.04
vn 126 0 ac 1
vp 27 0 dc 0
.ac dec 5 1khz 300meghz
.print i(vio)
.print i(viin)
vidd 101 1
viss 25 125
vip 18 48
vil 41 21
vi2 21 51
vio 21 61
viin 126 26
ro 61 0 100k
*****
.option nomod limpts=4000
.option post dcon=1
.end

```

```

**** operational transconductance amplifier model # 3**
** program to test the ac analysis ****
** same power; same gm (output current); more area ****
** differential pair ****
m1 14 26 8 8 n l=3u w=3u
m2 48 27 8 8 n l=3u w=3u
** current source ****
m10 8 6 25 25 n l=3u w=3u
*** current mirror 1 ***
m20 15 16 1 1 p l=3u w=3u
m21 14 14 15 1 p l=3u w=3u
m22 16 16 1 1 p l=3u w=10.8u
m23 17 14 16 1 p l=3u w=10.8u
*** current mirror 2 ***
m24 19 20 1 1 p l=3u w=3u
m25 18 18 19 1 p l=3u w=3u
m26 20 20 1 1 p l=3u w=10.8u
m27 41 18 20 1 p l=3u w=10.8u
*** current mirror 3 ***
m28 23 23 25 25 n l=3u w=3u
m29 17 17 23 25 n l=3u w=3u
m30 22 23 25 25 n l=3u w=3u
m31 51 17 22 25 n l=3u w=3u
*****
***
.model p pmos (level=2 vto=-0.8 kp=12e-6 gamma=0.6 phi=0.6 lambda=0.03
+ rd=100 rs=100 pb=0.6 cgso=2.5e-10 cgdo=2.5e-10 cgbo=5.0e-10 rsh=80
+ cj=1.5e-4 mj=0.6 cjsw=4.0e-10 mjsw=0.6 js=1.0e-5 tox=5.0e-8 nsub=5.0e15
+ nss=0 nfs=0 tpg=1 xj=5.0e-7 ld=2.5e-7 uo=250 vmax=0.7e5)
*
.model n nmos (level=2 vto=0.7 kp=40e-6 gamma=1.1 phi=0.6 lambda=0.01
+ rd=40 rs=40 pb=0.7 cgso=3.0e-10 cgdo=3.0e-10 cgbo=5.0e-10 rsh=25
+ cj=4.4e-4 mj=0.5 cjsw=4.0e-10 mjsw=0.3 js=1.0e-5 tox=5.0e-8
+ nsub=1.7e16 nss=0 nfs=0 tpg=1 xj=6.0e-7 ld=3.5e-7 uo=775 vmax=1.0e5)
*****
**
vdd 101 0 dc 5
vss 125 0 dc -5
vc1 6 25 dc 1.35
vn 126 0 ac 1
vp 27 0 dc 0
.ac dec 5 1khz 300meghz
.print i(vio)
.print i(viin)
vidd 101 1
viss 25 125
vip 18 48
vil 41 21
vi2 21 51
vio 21 61
viin 126 26
ro 61 0 100k
*****
.option nomod limpts=4000
.option post dcon=1
.end

```

```

* file to check the random error in output current of conventional
sink CM.
* for the current gain of 3)
*set parameters
.param nk=gauss(40u,0.024,3)
.param pk=gauss(12u,0.03,3)
.param nvt=gauss(0.7,0.018,3)
.param pvt=gauss(-0.8,0.033,3)
*
*** Mask implementing error (litho)
.param l1=3u lphoto=.1u xphotol=gauss (lphoto, .3, 3)
.param w1=3u wphoto1=.1u xphotow1=gauss (wphoto1, .3, 3)
.param w2=9u wphoto2=.1u xphotow2=xphotow1
.param photol=xphotol
.param photow=xphotow1
*
* Edge raggedness effect **
.param leff =agauss (l1, .02u, 3)
.param weffr=agauss (w1, .02u, 3)
.param weffo=agauss (w2, .02u, 3)
*
*** Mask misalignment error (20%) effect / CH1/page 8 ***
.param leff1=gauss (leff, .2, 3)
.param weff1=gauss (weffr, .2, 3)
.param weff2=gauss (weffo, .2, 3)
*
m1 2 2 0 0 n l=leff1 w=weff1
m2 5 2 0 0 n l=leff1 w=weff2
.model n nmos level=1 vto=nvt kn=nk lambda=0.000 xl=photol xw=pho-
tow
.model p pmos level=1 vto=pvt kp=pk lambda=0.000 xl=photol xw=pho-
tow
vdd 1 0 dc 5
vic0 7 2
viol 1 5
irc0 1 7
.dc irc0 4.95u 5.05u 0.02u sweep monte=25
.print dc i(vic0) i(viol) v(2) v(5)
* measurment statements
.meas dc maxval max i(viol)
.meas dc minval min i(viol)
.meas dc avgval avg i(viol)
.meas dc ppval pp i(viol)
.option spice nomod autostop
.option post dcon=2
.end

```

```

* file to check the random error in output current of
*conventional cascode sink CM. for the same current gain
*set parameters
.param nk=gauss(40u,0.024,3)
.param pk=gauss(12u,0.03,3)
.param nvt=gauss(0.7,0.018,3)
.param pvt=gauss(-0.8,0.033,3)
*
*** Mask implementing error (litho)
.param l1=3u lphoto=.1u xphotol=gauss (lphoto, .3, 3)
.param w1=3u wphoto1=.1u xphotow1=gauss (wphoto1, .3, 3)
.param w2=6u wphoto2=.1u xphotow2=xphotow1
.param photol=xphotol
.param photow=xphotow1
*
* Edge raggedness effect **
.param leff =agauss (l1, .02u, 3)
.param weffr=agauss (w1, .02u, 3)
.param weffo=agauss (w2, .02u, 3)
*
*** Mask misalignment error typical (20%). / CH1/page 8 ***
.param leff1=gauss (leff, .2, 3)
.param weff1=gauss (weffr, .2, 3)
.param weff2=gauss (weffo, .2, 3)
*
m1 3 3 0 0 n l=leff1 w=weff1
m2 4 3 0 0 n l=leff1 w=weff2
m3 2 2 3 3 n l=leff1 w=weff1
m4 5 2 4 4 n l=leff1 w=weff2
.model n nmos level=1 vto=nvt kn=nk lambda=0.000 xl=photol xw=photo-
tow
.model p pmos level=1 vto=pvt kp=pk lambda=0.000 xl=photol xw=photo-
tow
vdd 1 0 dc 5
vic0 7 2
viol 1 5
irc0 1 7
.dc irc0 4.95u 5.05u 0.02u sweep monte=25
.print dc i(vic0) i(viol) v(2)
* measurment statements
.meas dc maxval max i(viol)
.meas dc minval min i(viol)
.meas dc avgval avg i(viol)
.meas dc ppval pp i(viol)
.option spice nomod autostop
.option post dcon=2
.end

```

```

* file to check the random error in output current of
* type 1.a CM.
*set parameters
.param nk=gauss(40u,0.024,3)
.param pk=gauss(12u,0.03,3)
.param nvt=gauss(0.7,0.018,3)
.param pvt=gauss(-0.8,0.033,3)
*
*** Mask implementing error (litho)/ montc. manual ***
.param l1=3u lphoto=.1u xphotol=gauss (lphoto, .3, 3)
.param w1=3u wphoto1=.1u xphotow1=gauss (wphoto1, .3, 3)
.param photol=xphotol
.param photow=xphotow1
*
*Edge raggedness effect /sigma L&W=.01 to .03 um [12],pp140**
.param leff=agauss (l1, .02u, 3)
.param weff=agauss (w1, .02u, 3)
*
**Mask misalignment error (20%) /CH1/page 8 [NO EFFECT ON THIS CM]
*
m1 0 0 2 2 p l=leff w=weff
m2 5 2 0 0 n l=leff w=weff
.model n nmos level=1 vto=nvt kn=nk lambda=0.000 xl=photol xw=photo-
tow
.model p pmos level=1 vto=pvt kp=pk lambda=0.000 xl=photol xw=photo-
tow
vdd 1 0 dc 5
vic0 7 2
viol 1 5
irc0 1 7
.dc irc0 4.95u 5.05u 0.02u sweep monte=25
.print dc i(vic0) i(viol) v(2) v(5)
* measurment statements
.meas dc maxval max i(viol)
.meas dc minval min i(viol)
.meas dc avgval avg i(viol)
.meas dc ppval pp i(viol)
.option spice nomod autostop
.option post dcon=2
.end

```

```

* file to check the random error in output current of
* type IV.a CM sink.
*set parameters
.param nk=gauss(40u,0.024,3)
.param pk=gauss(12u,0.03,3)
.param nvt=gauss(0.7,0.018,3)
.param pvt=gauss(-0.8,0.033,3)
*
*** Mask implementing error (litho)/ montc. manual ***
.param l1=3u lphoto=.1u xphotol=gauss (lphoto, .3, 3)
.param w1=3u wphoto1=.1u xphotow1=gauss (wphoto1, .3, 3)
.param photol=xphotol
.param photow=xphotow1
*
*Edge raggedness effect /sigma L&W=.01 to .03 um [12],pp140**
.param leff=agauss (l1, .02u, 3)
.param weff=agauss (w1, .02u, 3)
*
**Mask misalignment error (20%) /CH1/page 8 [NO EFFECT ON THIS CM]
*
m1 0 0 3 3 p l=leff w=weff
m2 4 3 0 0 n l=leff w=weff
m3 3 3 2 2 p l=leff w=weff
m4 5 2 4 4 n l=leff w=weff
mc 2 8 0 0 n l=leff w=weff
.model n nmos level=1 vto=nvt kn=nk lambda=0.000 xl=photol xw=photo-
tow
.model p pmos level=1 vto=pvt kp=pk lambda=0.000 xl=photol xw=photo-
tow
vdd 1 0 dc 5
vc 8 0 dc 1.407
vic0 7 2
viol 1 5
irc0 1 7
.dc irc0 24.95u 25.05u 0.02u sweep monte=25
.print dc i(vic0) i(viol) v(2)
* measurment statements
.meas dc maxval max i(viol)
.meas dc minval min i(viol)
.meas dc avgval avg i(viol)
.meas dc ppval pp i(viol)
.option spice nomod autostop
.option post dcon=2
.end

```


APPENDIX B

DERIVATION OF THE CURRENT RATIO FOR SELECTED NCMOS CURRENT MIRRORS

B.0 INTRODUCTION

In this appendix the current ratio formulas for the NCMOS current mirrors described in Chapter 3 will be derived. This will help us to get much clear idea for sec. 3.2.2 to sec. 3.2.4. Since the analysis of Type V NCMOS current mirror was already discussed in Chapter 2, it will not be discussed in this Appendix. Only the three remaining NCMOS current mirrors namely (Type IIb, Type VI and Type VIII) will be analyzed here.

B.1 TYPE IIb NCMOS CURRENT MIRROR (SOURCE) WITH $K > 1$

This NCMOS current mirror, shown in Fig. B.1, is the source version of Type IIa discussed in Chapter 2. Since the reference current I_R is constant, then it will develop a corresponding voltage V_{SG1} between the source and the gate of the PMOS transistor Q_1 , and this voltage will also be impressed across the gate and source of the NMOS transistor Q_2 . The output current I_o is pulled by Q_2 , depending on the values of voltage V_{SG2} and transconductance K_2 .

Assume that MOSFETs Q_1 , Q_2 and Q_3 are all operating in the saturation region, then.

For transistor Q_1 :

$$I_R = \beta_1 \cdot (V_{SG1} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD1}) \quad (\text{B.1})$$

For transistor Q_2 :

$$I_o = \beta_2 \cdot (V_{GS2} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS2}) \quad (\text{B.2})$$

For transistor Q_3 :

$$I_o = \beta_3 \cdot (V_{SG3} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD3}) \quad (\text{B.3})$$

Further to minimize the NCMOS current mirror area used in this design, assume equal size transistors with ratio $W/L = 1$. Hence:

$$\beta_1 = \beta_3 = \frac{K_p}{2}, \text{ and } \beta_2 = \frac{K_n}{2}.$$

The voltage $V_{DG2} = V_{DS2} = V_{SG1} = V_R$, and the drain to source voltage of transistor Q_1 is

$$V_{SD1} = V_{GS2} + V_{SG3}.$$

Combining eqn (B.2) and (B.3) and assuming $\lambda_p V_{SD1} \ll 1$, the voltage V_{SG3} can be written as:

$$V_{SG3} \approx \sqrt{\frac{K_n}{K_p}} \cdot (V_{GS2} - V_{Tn}) + V_{Tp} \quad (\text{B.4})$$

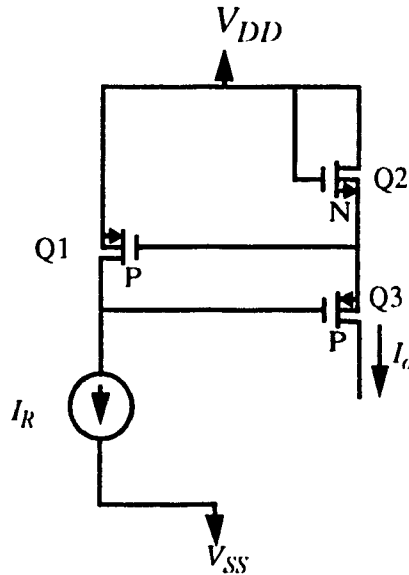


Fig. B.1

Circuit diagram for Type IIb NCMOS current mirror, (source version) with $K > 1$

The assumption $\lambda_p V_{SD1} \ll 1$ should hold over a large range of R_L values because of the negative feedback employed in the circuit. The reason behind the use of this -ve feedback is similar to the one described in Chapter 2, in conjunction with Type IIa NCMOS current mirror.

The voltage V_{SD1} will be approximately constant and equal to:

$$V_{SD1} = V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}} \right) - V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} + V_{Tp} \quad (\text{B.5})$$

Substituting eqn. (B.5) into eqn. (B.1), the reference current can be written as:

$$I_R = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot \left(1 + \lambda_p \left(V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}} \right) - V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} + V_{Tp} \right) \right) \quad (\text{B.6})$$

Substituting the values of β_2 , V_{SG2} and V_{SD2} into eqn. (B.3), the output current becomes:

$$I_o = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (\text{B.7})$$

From eqn. (B.7) by eqn. (B.6) the current ratio is easily derived and is equal to:

$$\frac{I_o}{I_R} = \frac{K_n}{K_p} \cdot \frac{(V_R - V_{Tn})^2}{(V_R - V_{Tp})^2} \cdot \frac{(1 + \lambda_p V_R)}{\left(1 + \lambda_p \left(V_R \cdot \left(1 + \sqrt{\frac{K_n}{K_p}} \right) - V_{Tn} \cdot \sqrt{\frac{K_n}{K_p}} + V_{Tp} \right) \right)} \quad (\text{B.8})$$

The current ratio I_o/I_R in eqn (B.8) is greater than unity and is a function of only one variable V_R , and it is therefore completely independent of load resistance R_L and the output voltage V_o , as long as Q_1 , Q_2 and Q_3 operate in the saturation region.

B.2 TYPE VI NCMOS CURRENT MIRROR (SINK) WITH $K < 1$

This circuit shown in Fig. B.2, is one of the best four circuits in its response to control circuit given in Chapter 3. A separation between the output voltage V_o and the voltage V_{SD2} is provided through transistor Q_3 , which will also give a negative feedback to the reference

side transistor Q_4 . This will keep output current I_o stable whenever there is a variation in the output voltage due to a load variation.

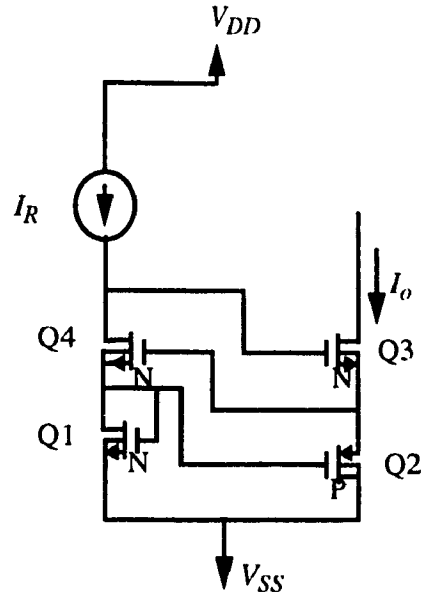


Fig. B.2

Circuit diagram for Type VI NCMOS current mirror, (sink version) with $K < 1$

Let all transistors be in the saturation region. Further assume that transistors Q_1 and Q_4 carry the same reference current, while Q_2 and Q_3 carry the same output current, then:

For transistor Q_1 :

$$I_R = \beta_1 \cdot (V_{GS1} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS1}) \quad (\text{B.9})$$

For transistor Q_4 :

$$I_R = \beta_4 \cdot (V_{GS4} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS4}) \quad (\text{B.10})$$

For transistor Q_2 :

$$I_o = \beta_2 \cdot (V_{SG2} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD2}) \quad (\text{B.11})$$

For transistor Q_3 :

$$I_o = \beta_3 \cdot (V_{GS3} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS3}) \quad (\text{B.12})$$

Since all the MOSFETs used are of the same size, then the values of β 's will be as follows:

$$\beta_2 = \frac{K_p}{2} \text{ and } \beta_1 = \beta_3 = \beta_4 = \frac{K_n}{2}.$$

Because I_R is common for both MOSFETs Q_1 and Q_4 then assuming $\lambda_n V_{DS1} \ll 1$ and $\lambda_n V_{DS4} \ll 1$ we have:

$$V_{GS1} \equiv V_{SG2} = V_{GS4} = V_R$$

This is reasonable since there is the negative feedback will keep current I_o constant as long as I_R remains constant. The feedback operations is similar to the one discussed in sec. 2.3 in conjunction with type V NCMOS current mirror.

Now since:

$$V_{SD2} = V_{GS4} + V_{GS1}.$$

Then by letting $V_{GS1} = V_R$, and Combining eqn. (B.11) with eqn. (B.12) we get:

$$K_p \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p 2 V_R) = K_n \cdot (V_{GS3} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS3}) \quad (\text{B.13})$$

Assuming $\lambda_n V_{DS3} \ll 1$ then the voltage V_{GS3} can be written in terms of the reference voltage as follows:

$$V_{GS3} \approx \sqrt{\frac{K_p}{K_n}} \cdot (V_R - V_{Tp}) + V_{Tn} \quad (\text{B.14})$$

voltage $V_{DS4} = V_{GS4} + V_{GS3}$ or equivalently:

$$V_{DS4} = V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - \left(V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}}\right) + V_{Tn} \quad (\text{B.15})$$

Substituting the values of V_{GS4} and V_{DS4} into eqn. (B.10), the current I_R will be equal to:

$$I_R = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot \left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - \left(V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}}\right) + V_{Tn}\right)\right) \quad (\text{B.16})$$

Because voltage $V_{SD2} = 2V_R$ then the output current I_o in eqn. (B.11) can be written as follows:

$$I_o = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot (1 + \lambda_p 2 V_R) \quad (\text{B.17})$$

Dividing eqn. (B.17) by eqn. (B.16) the current ratio of Type VI NCMOS current mirror will be:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{(1 + \lambda_p 2V_R)}{\left(1 + \lambda_n \left(V_R \cdot \left(1 + \sqrt{\frac{K_p}{K_n}}\right) - \left(V_{Tp} \cdot \sqrt{\frac{K_p}{K_n}}\right) + V_{Tn}\right)\right)} \quad (\text{B.18})$$

The current ratio in eqn. (B.18) is clearly a function of only one variable namely is V_R . This means that this NCMOS current mirror is regulated and its current ratio is independent of the load value.

B.3 TYPE VIII NCMOS CURRENT MIRROR (SOURCE) WITH $K < 1$

This NCMOS current mirror shown in Fig. B.3, was also selected in Chapter 3 as one of the best four current mirror circuits that has a good response to the control circuit. This current mirror is a source model with current ratio less than unity. This circuit also implements a feedback loop to keep the circuit stable and independent of load variation.

Assuming that all transistors are saturated, the drain currents will be as follows:

For transistor Q_1 :

$$I_R = \beta_1 \cdot (V_{GS1} - V_{Tn})^2 \cdot (1 + \lambda_n V_{DS1}) \quad (\text{B.19})$$

For transistor Q_4 :

$$I_R = \beta_4 \cdot (V_{SG4} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD4}) \quad (\text{B.20})$$

For transistor Q_2 :

$$I_o = \beta_2 \cdot (V_{SG2} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD2}) \quad (\text{B.21})$$

For transistor Q_3 :

$$I_o = \beta_3 \cdot (V_{SG3} - V_{Tp})^2 \cdot (1 + \lambda_p V_{SD3}) \quad (\text{B.22})$$

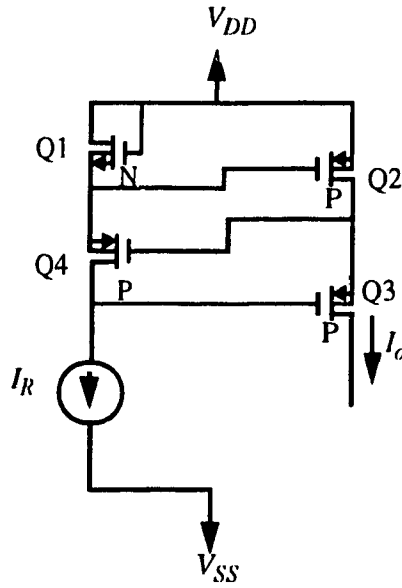


Fig. B.3

Circuit diagram for Type VIII NCMOS current mirror, (source version) with $K < 1$

Further let the ratio W/L for these MOSFETs transistors equal to unity, then the β 's factors will be equal to one half the transconductance factor (K) i.e.:

$$\beta_1 = \frac{K_n}{2}, \text{ and } \beta_2 = \beta_3 = \beta_4 = \frac{K_p}{2}$$

Provided that $\lambda_p V_{SD3} \ll 1$ and $\lambda_p V_{SD2} \ll 1$.

Since transistors Q_2 & Q_3 hold the same current I_o , then voltage $V_{SG2} = V_R = V_{SG3}$, because voltage $V_{SD4} = V_{SG4} + V_{SG3}$.

Also since MOSFETs Q_1 & Q_4 hold the same current I_R , then:

$$\frac{K_n}{2} \cdot (V_R - V_{Tn})^2 (1 + \lambda_n V_R) = \frac{K_p}{2} \cdot (V_{SG4} - V_{Tp})^2 (1 + \lambda_p (V_{SG4} + V_{SG3})) \quad (\text{B.23})$$

For simplicity and because $\lambda_p \ll 1$, then making the following reasonable approximation:

$$\lambda_p (V_{SG4} + V_{SG3}) = \lambda_p 2V_R$$

we get:

$$V_{SG4} \approx \sqrt{\frac{K_n}{K_p}} \cdot (V_R - V_{Tp}) \cdot \sqrt{\frac{1 + \lambda_n V_R}{1 + \lambda_p 2 V_R}} + V_{Tp} \quad (\text{B.24})$$

Since the source-to-drain voltage of transistor Q_2 equal to:

$$V_{SD2} \equiv V_{SG2} + V_{SG4} = V_R + V_{SG4} \quad (\text{B.25})$$

Then the output current can be written by using eqn. (B.21), eqn. (B.24) and eqn. (B.25) as follows:

$$I_o = \frac{K_p}{2} \cdot (V_R - V_{Tp})^2 \cdot \left(1 + \lambda_p \left(\alpha V_R \left(1 + \sqrt{\frac{K_n}{K_p}} \right) - \left(\alpha V_{Tp} \cdot \sqrt{\frac{K_n}{K_p}} \right) + V_{Tp} \right) \right) \quad (\text{B.26})$$

where the factor α equals to:

$$\alpha = \sqrt{\frac{1 + \lambda_n V_R}{1 + \lambda_p 2 V_R}} \quad (\text{B.27})$$

The reference current can be written in terms of Q_1 MOSFET parameters as follows:

$$I_R = \frac{K_n}{2} \cdot (V_R - V_{Tn})^2 \cdot (1 + \lambda_n V_R) \quad (\text{B.28})$$

Dividing eqn. (B.26) by eqn. (B.28) gives us the current ratio formula:

$$\frac{I_o}{I_R} = \frac{K_p}{K_n} \cdot \frac{(V_R - V_{Tp})^2}{(V_R - V_{Tn})^2} \cdot \frac{\left(1 + \lambda_p \left(\alpha V_R \left(1 + \sqrt{\frac{K_n}{K_p}} \right) - \left(\alpha V_{Tp} \cdot \sqrt{\frac{K_n}{K_p}} \right) + V_{Tp} \right) \right)}{(1 + \lambda_n V_R)} \quad (\text{B.29})$$

Since the factor α is a function of one variable V_R , then the current ratio in eqn. (B.29) will be defined as a function of the same single variable (V_R). This means the proposed NCMOS current mirror model is independent of the load value.