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Solid State Series Tapping of HVDC Transmission

Md.Anisur Rahman

A Thesis

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The Department

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ABSTRACT

Solid State Series Tapping of HVDC Transmission

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There are two ways of tapping power from a HVDC transmission link, i.e, a series tap or a parallel tap. It has already been shown [7] that the series tap is more economical, when it is small. The feasibility of using a solid state forced commutated series tap, when feeding a weak ac system, is reported in technical literature [9, 10, 16, 22]. In this thesis, a forced commutated technique for series tapping named short circuit method is proposed and analyzed. Different series tapping techniques are also investigated and compared. A harmonic analysis of the output ac current and of the voltage on the dc side using short circuit method has been done. The harmonic reduction possibility using sinusoidal pulse width modulation (SPWM) technique and symmetric pulse width modulation technique with more than two pulses per half cycle are also investigated. Although these techniques reduce the harmonic levels, SPWM technique is found to be more effective in harmonic reduction capability than symmetric pulse width modulation. A series tap that uses the proposed short circuit method is investigated under small disturbance conditions and control strategy for the successful operation of the tap is evaluated.

ACKNOWLEDGEMENTS

The author wishes to express his heartfelt gratitude to Professor M. H. Rashid and to Dr. V. K. Sood for suggesting the problem and for their guidance and assistance during the entire preparation of this thesis. The author also expresses his gratitude to Dr. Saeed Arabi for his constructive suggestions.

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SYMBOLS

Symbols	Description
Δ	Small change / Difference
δ	Power angle
δ_o	Power Angle at Initial Condition
Φ_i	Power Factor Angle of Inverter Tap
Φ_m	Maximum System Impedence Angle
μ	Over lap Angle
ω_s	Angular Frequency
ω_o	Angular Frequency at Initial Conditions
g	Conductance per unit Length of Line
H	Feed back Transfer Function / Inertia Constant.
I_d	Current Magnitude Direct (dc)
I_i	" " of Inverter
I_l	" " " Load
$I_{(n)}$	Current Magnitude of the nth Harmonic
I_t	Current Magnitude of the Tap
I_0	Current Magnitude at Initial Conditions
i	Instantaneous Current
i_d	Instantaneous Current(pu) of d-Axis of Machine
i_q	Instantaneous Current(pu) of q-Axis of the Machine
i_i	Instantaneous Current of Inverter
i_l	Instantaneous Current of Load
i_o	Instantaneous Current at Initial Conditions
K_e	Controller Gain of Exciter
s	Over lap Angle in Degrees
$S_{(HP)}$	Size of High pass Filter

Symbols	Description
S_n	Size of Minimum Filter
$S_{(n)}$	Size of the nth Harmonic Filter
s	Laplace Transform Variable
T_ω	Time Constant of Speed Transducer
T_e	Time Constant of the Exciter
T_i	Time Constant of the Current Transducer
T_v	Time Constant of the Voltage Transducer
T_{do}	Open Circuit Field time Constant
U_c	Unit Cost of Capacitor
U_l	Unit Cost of Inductor
V_d	Voltage Magnitude Direct (dc)
Z_F	Impedence of Filter
A	System Matrix / Constant
B_c	Susceptance of Capacitance
B_F	Susceptance of Filter
B_t	Susceptance of Line
B	Constant
$C_{(HP)}$	Cap. of High Pass Filter
$C_{(n)}$	Cap. of nth Harmonic Filter
c	Capacitance per Unit Length
D	Self Damping Coefficient
D_{max}	Maximum Short Circuit Angle
D_{min}	Minimum Short Circuit Angle
d	$\frac{1}{2}$ Short circuit Angle
e_q	Internal Voltage of q- axis
V_f	Voltage Magnitude of Field

Symbols	Description
$V_{(n)}$	Voltage Magnitude of nth Harmonic
V_0	Voltage Magnitude at Rated Conditions
v	Instantaneous Voltage
v_d	Inst. Voltage(pu) of d- Axis
v_f	Inst. voltage(pu) of q- Axis
v_q	Inst. voltage(pu) of Field
v_t	Inst. voltage(pu) of Machine Terminal
v_0	Inst. voltage(pu) at Initial Conditions
X_t	Reactance of the Line
X	Reactance of the Transformer
x_d	d- Axis Syn. Reactance(pu) of the Machine
x_q	q- Axis Syn. Reactance(pu) of the Machine
x_0	Zero Seq. Reactance(pu) of Machine
$L_{(H.P)}$	Induct. of High Pass Filter
$L_{(n)}$	Induct. of nth Harm. Filter
L_t	Inductance of Line
l	Inductance per Unit Length
M	Moment of Inertia
P_d	DC Power
p_e	Electrical Power
p_m	Mechanical Power
p	Number of Pulses
$R_{(HP)}$	Resistance of High Pass Filter
$R_{(n)}$	Resist. of nth Harm. Filter
x_d'	d- Axis Trans. React.(pu) of Machine
x_q'	Q- Axis Trans. React.(pu) of Machine
x_d''	D- Axis Sub-Tran. React.(pu) of Machine
x_q''	Q- Axis Sub-Tran. React.(pu) of Machine

ABBREVIATIONS

ac	Alternating Current
BPS	By Pass Switch
Cap.	Capacitance
C.B.	Circuit Breaker
Comm'd	Commutated
Cont'd	Continued
Conv.	Converter
Ckt.	Circuit
Diff.	Differential
dc	Direct Current
d-q	Direct and Quadrature (axes)
e.g.	For Example
Eqn.	Equation
FC	Forced Commutated
FL	Full Load
Gen.	Generator
HP	High-Pass
HVDC	High Voltage Direct Current
i.e.	That is
Inv.	Inverter
IS	Isolation Switch
Max.	Maximum
Min.	Minimum
PF	Power Factor
PI	Proportional Integral (Controller)

pu	Per Unit
PWM	Pulse Width Modulated
Rect.	Rectifier / Rectification
ref.	Reference
r.m.s.	Root mean Square
S.R	Smoothing Reactor
SPWM	Sinusoidal Pulse Width Modulation
Syn.C	Synchronous Condenser
Sym. PWM	Symmetrical Pulse Width Modulation
VAr	Reactive Volt Ampere
12p	Twelve Pulse

LIST OF FIGURES.

CHAPTER 1

INTRODUCTION

1.1 REVIEW.

Since the beginning of high voltage direct current transmission, there has been a considerable interest to interconnect more than two terminal stations with a dc network. The introduction of thyristor valves has increased interest in multiterminal HVDC systems. Multiterminal HVDC system can basically be divided into two categories namely, parallel and series arrangements. Series and parallel arrangements of a three terminal system are shown in Fig. 1.1, and 1.2. respectively. Kingsnorth HVDC system and Nelson river HVDC system include control characteristics which are virtually multiterminal [3]. Work on a few other multiterminal projects is going on around the world [23]. There has been a considerable interest in series tapping in recent years and it can be considered as a potential candidate for future multiterminal operations.

A comparison between parallel and series arrangements, shows that series arrangement is more economical for small taps of rating less than 20% of the dc system capability [7]. Moreover, since the cost of a high-voltage low-current valve is higher than the cost of a low-voltage high-current valve, it is likely that series tap may be cheaper than a comparably rated parallel tap. There are two drawbacks of a HVDC converter, namely, production of harmonics and consumption of reactive power. Two conventional methods i.e filtering and increasing the number of pulses exist for reducing the harmonics. Increasing the pulse number beyond 12pulse using phase shifting transformer windings, is considered to be uneconomic.

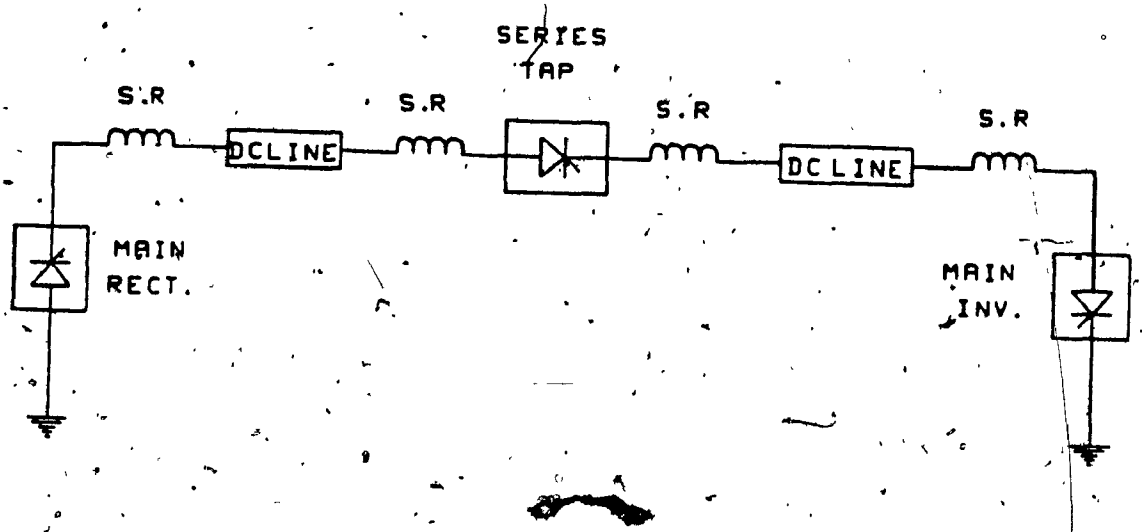

Figure 1.1 Series Arrangement of a Three Terminal HVDC System.

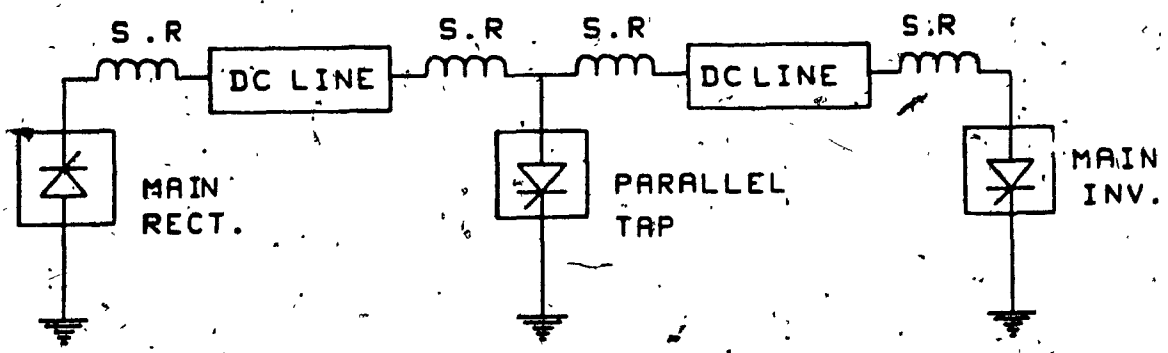

Figure 1.2 Parallel Arrangement of a Three Terminal HVDC System.

The reactive power is normally provided by static VAr systems, synchronous condensers, capacitor banks, and partially by filter banks. Forced commutated inverters have been proposed in recent years as an alternative to line commutated inverters. In many cases, these forced commutated inverters are capable of providing their own reactive power requirements and do not need an external source of reactive power, rather they can deliver reactive power to the ac systems. Moreover, it can feed an ac system without its own generator or synchronous condensers. Overvoltages due to load changes and electromechanical transients are no problem for these inverters and a quick restart is possible after a fault [18].

Forced commutated inverters have some shortcomings mainly due to increased cost in station equipment especially for the valves and commutation circuits. In this thesis, a novel series tapping technique is proposed which is easier to implement, and can feed a system without any ac generation. This method is designated as short circuit method [9]. This forced commutated scheme is really pulse width modulation technique with 2-symmetric pulse per half cycle.

In power electronics, modern techniques such as pulse width modulation and sinusoidal pulse width modulation are available to reduce low order harmonics, with or without output control of converters. With the development of high power gate turn off thyristor's (GTO's), such techniques can also be applied to forced commutated HVDC inverters.

1.2 OBJECTIVES

There are two inherent drawbacks of an HVDC converter, namely, reactive power consumption and harmonic production, and these become more intense when the converter operates as a series tap i.e; operating at constant dc line current, rather than constant dc voltage. The short circuit method is free from one drawback namely, reactive power consumption, provided there is no overlap [9]. However, harmonic generation is still a problem of this method. The methods of harmonic reduction by the application of various modern techniques are studied.

The objectives of this thesis are as follows :

1. Comparing series tap with parallel tap
2. Development of the idea of short circuit method. Its principle of operation and comparison with differential firing method.
3. Study of harmonic reduction possibilities.
4. Dynamic study of the tapping station and control of the tapping station.

1.3 COMPARISON BETWEEN SERIES AND PARALLEL TAPPING

Depending upon the application, series and parallel arrangements each offers some advantage over the other. But the series connected tapping has been found to be more advantageous than the parallel connected tapping when the tap is small.

A parallel tap has to be rated at system voltage (with current rating less than system current). A series tap has to be rated at system current, not system voltage. The cost of a high-voltage low-current valve is usually higher than the cost of a low voltage high-current valve. As such, series arrangement for small taps will be less costly than a parallel arrangement.

The parallel arrangement is not economical for small taps (less than 20% of system rating) because the small parallel tap is susceptible to system faults, especially to disturbances on its own ac bus. This might cause commutation failure; recovery from such failure may be difficult and may require a momentary shutdown of the whole system. A series tap however, is less subject to commutation failure [7, 6].

Other general advantages of series arrangement are indicated in rows 4, 5, 6, 7, 8, 9 of Table 1.1. But a series tap may also have some drawbacks as indicated in rows 3, 11, 12 and 13, of Table 1.1.

TABLE 1.1

	DESCRIPTION	PARALLEL ARRANGEMENT	SERIES ARRANGEMENT
1	Current rating of tap	Less than system current	At system current
2	Voltage rating of tap	At system voltage	Less than system voltage
3	Insulation level Tap Equipment Line	 At low voltage The same along the line	 At high voltage Different at each section
4	Blocking of a single bridge in series connection	Either all stations work at reduced voltage or that station be disconnected	No reduction in other stations voltage
5	Central control	More flexible if used	Not needed
6	D C Circuit Breaker	More flexible if used	Not needed
7.	Dependance on fast communication	Higher than point to point system	More or less similar to point to point system
8.	Reversal of power at any station.	Requires mechanical switch operation	No mechanical switch operation
9.	Commutation failure in one station	May draw excessive current from other station	Is handled by main rectifier α control similar to point to point system
10.	Effect of system fault	Probability of commutation failure high	Probability of commutation failure low

		(recovery may be difficult)	with easy recovery
11.	Transmission losses	Minimized by keeping the system voltage at rated value	Minimized by letting the inverter with the highest $\frac{P_{do}}{P_{dn}}$ set the current
12	Harmonic magnitude (p.u) ac	Some what higher than comparable converter in a point to point system	Much higher than comparable converter in a point to point system
13.	VAr requirement of the tap	Some what higher than comparable converter in a point to point system	Much higher than comparable converter in a point to point system
14.	Harmonic magnitude of dc in the range of operation	Slightly higher than those of point to point system	Much higher than those of point to point converters usually less on line base

CHAPTER 2

SURVEY OF SERIES TAPPING TECHNIQUES AND PRINCIPLE OF OPERATION OF SHORT CIRCUIT METHOD

2.1 INTRODUCTION

Series tapping employing natural commutation requires a large amount of reactive power compensation and needs a suitable source of ac for commutation. Forced commutation can solve many problems connected with weak receiving end ac system. FC inverters do not require any reactive power compensation and they can feed a system without its own generation capability. Hybrid converters consisting of naturally commutated converter and forced commutated converter inherit the advantages and disadvantages of both. Diode rectifier stations have been proposed to transfer electrical energy of isolated station to an HVDC system.

In this thesis, different series tapping techniques employing natural commutation, forced commutation or hybrid of these two are discussed.

A comparison of series tapping between short circuit method and differential firing method is also presented.

2.2 SCHEME PROPOSED BY BOWLES, NAKRA AND TURNER

The schematic diagram of the proposed station is shown in Fig.2.1. There are two main parts in the station, the first is the unit to extract power from the line consisting of converter bridges. The second part of the station is the ac machine. One problem of this method is that it will require an auxiliary drive for starting the machine from rest. Without the commutation voltage the bridge cannot provide the accelerating torque [7].

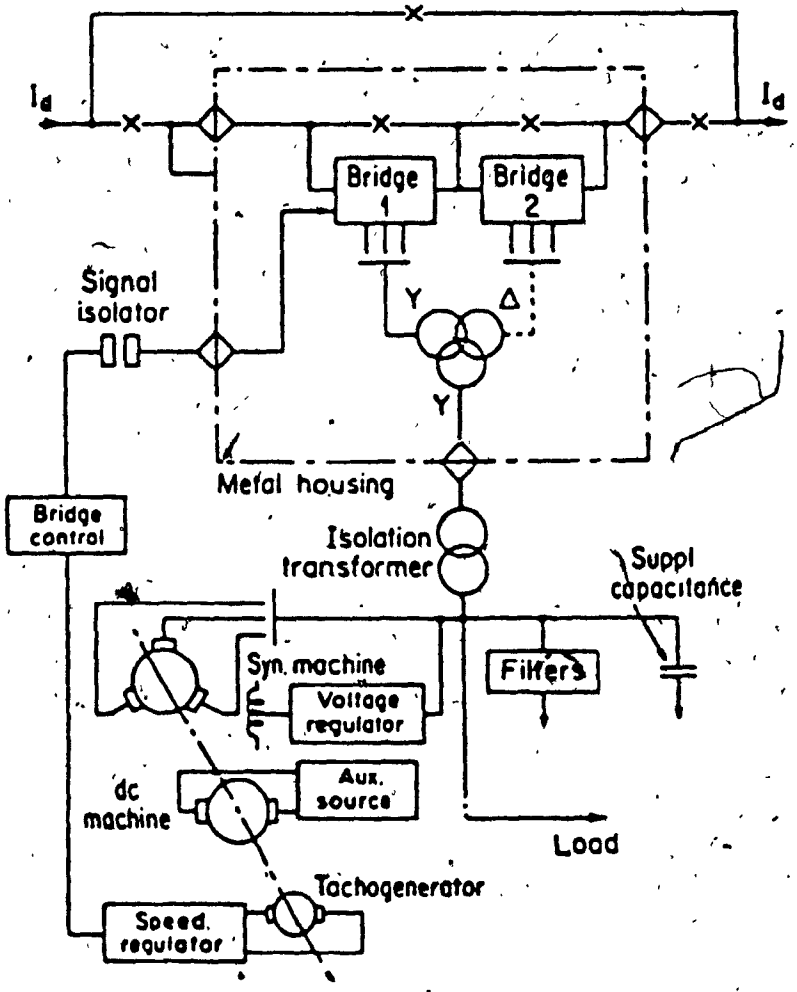

Fig. 2.1 Block Diagram of a Series Tapping Station Auxiliary Source required for Start-up.

2.3 DIFFERENTIAL FIRING METHOD

When two or more sets of bridges in series have different firing angles we call the system a differential firing system Fig.2.2. For explaining, approximating the ac current waveform as a square wave Fig.2.3, if the zero axis is moved to the right by the firing angle plus 60 degrees, the waveform will be symmetrical about the zero axis and the phase angle of all harmonics will be zero. Therefore with the zero axis as indicated in Fig.2.3.

$$\theta_{(n)}=n\,(\alpha+60^0)$$

For differential firing with two bridges with firing angles $\alpha_{(1)}$ and $\alpha_{(2)}$.

$$\theta_{1(n)}=n\,(\alpha_1+60^o)$$

$$\theta_{2(n)}=n\,(\alpha_2+60^0)$$

The approximate relative phase angle between the nth harmonic currents produced by the two bridges is

$$\delta\theta_{(n)}=\theta_{2(n)}-\theta_{1(n)}=n\,(\alpha_2-\alpha_1)=n\,\delta\alpha$$

which holds for small dc line current.

That means by maintaining a proper phase difference between two firing angles a desired phase shift between the two components of the nth harmonic currents can be achieved. This phase shifting property can be utilized in reducing harmonic magnitudes similar to phase shifting transformer, although no characteristic harmonics can be completely eliminated [6].

Alternatively, by adjusting the firing angle of both bridges reactive power flow can be controlled and would thus regulate the taps ac voltage to some extent. Higher voltage regulation can be obtained by using more bridge sets in

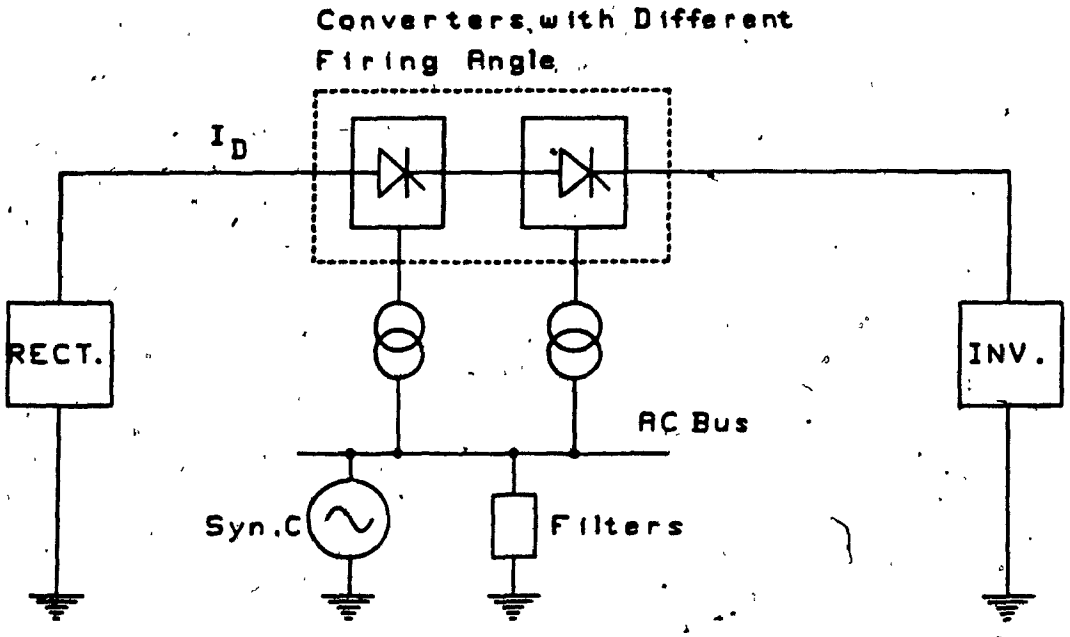

Fig. 2.2 Differential Firing Method Schematic.

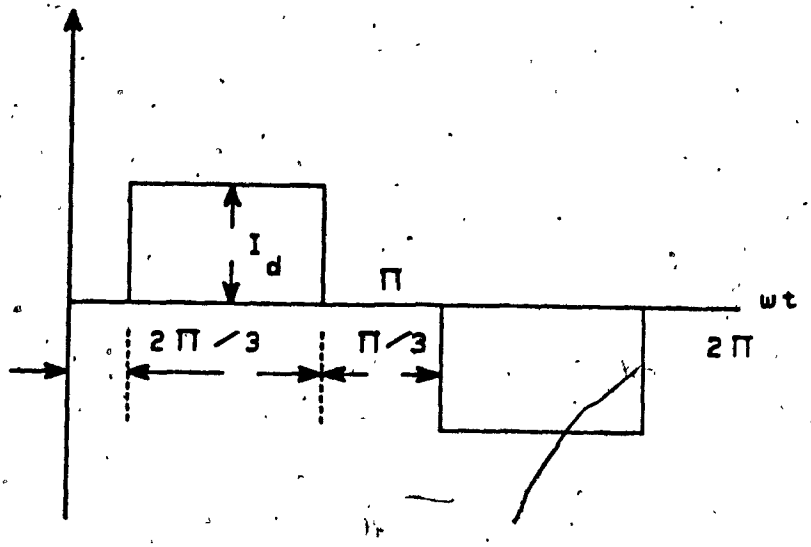

Fig. 2.3 Square Current Waveforms.

series.

2.4 SERIES CAPACITOR COMMUTATED TAPPING

The series capacitor commutated bridge is one of the most suitable alternatives amongst various possible forced commutation techniques. Assuming that a constant DC current is flowing and the system is operating in the steady state with thyristors T_1 and T_2 conducting, the capacitors in phase a and c charge with opposite polarity as shown in Fig.2.4. When T_3 is fired to take over from T_1 the voltages on C_a and C_b are of the correct polarity for commutation. After the commutation is completed T_3 and T_2 conduct with voltage on C_b decreasing and on C_c decreasing with constant current flowing through them [21].

Capacitors provide the commutation voltage, and firing angles beyond 180^0 are possible. The valve stresses are higher. There are some limitations on the rate of change of firing angle. The dc harmonics are considerable. The 12th and 24th could be as high as 15% which is quite substantial. This makes the series capacitor commutated converter unsuitable as a major converter. However it can be used as a series tap on an HVDC line with a small voltage drop (say, less than 10%) so that from the dc lines point of view, the resulting harmonics are small [22].

2.5 HYBRID CONVERTER

It has been shown (Fig. 2.5) that a connection of advance firing converter with a delay firing converter results in a high performance HVDC converter called a hybrid converter [16].

This arrangement requires no reactive power compensation. Within a certain range real and reactive power can be independently controlled and the ac

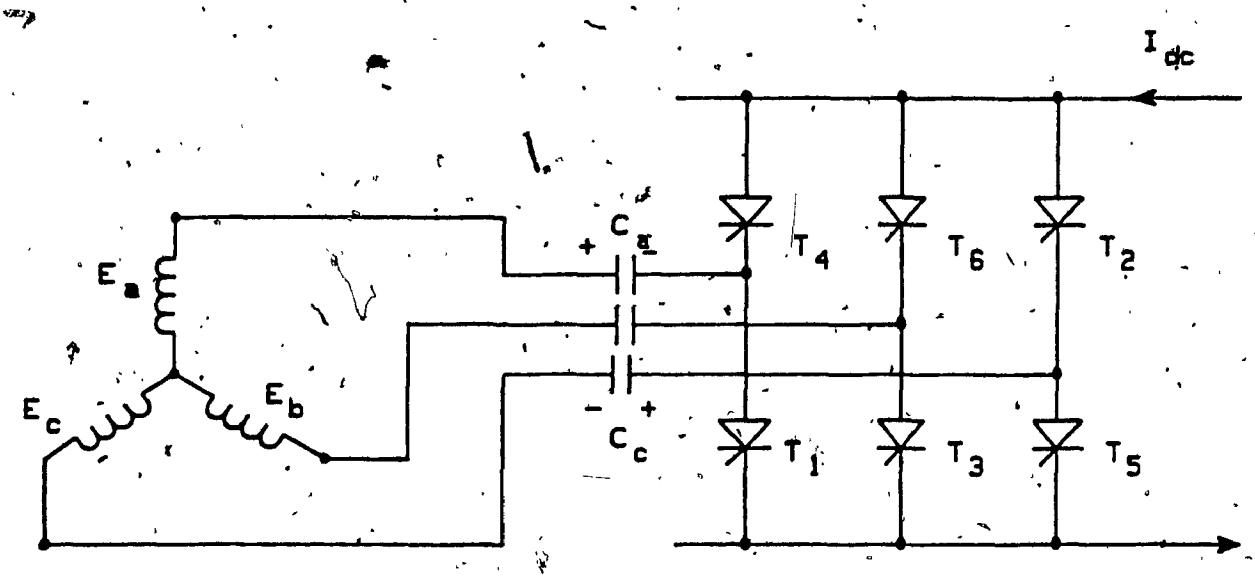

Fig. 2.4 Series Capacitor Commutated Inverter.

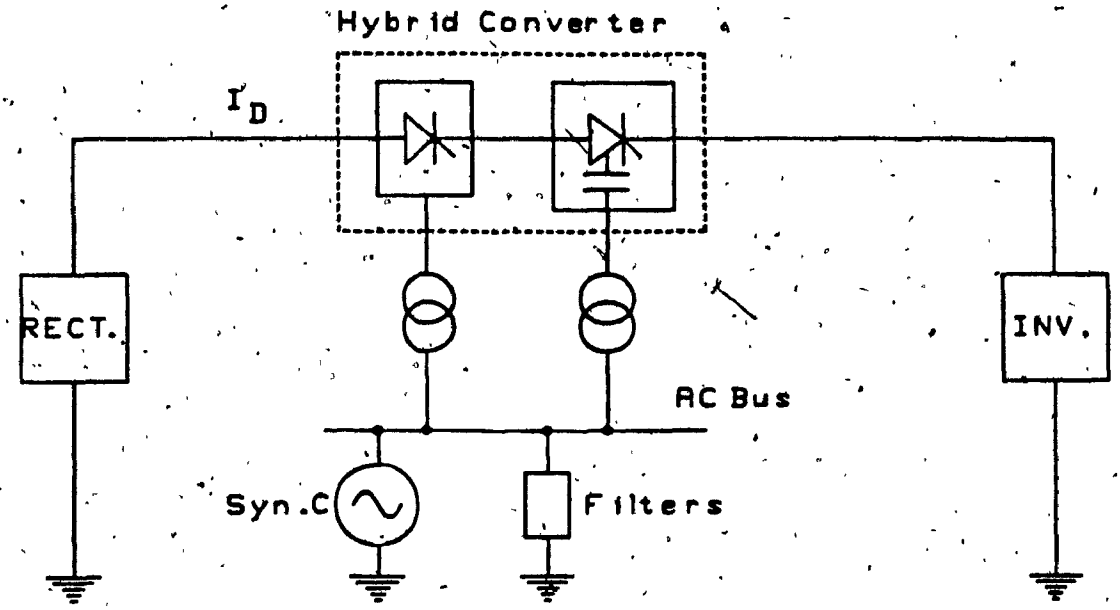

Fig. 2.5 Hybrid Converter Method.

bus voltage can also be controlled. It can feed a weak ac system without sophisticated control.

The hybrid converter, being a combination of naturally commutated converter and artificially commutated converter, inherits both the advantages and disadvantages of both converters.

2.6 DIODE RECTIFIER TECHNIQUE

Diode rectifier stations have been proposed for HVDC series tapping (Fig. 2.6.). A likely application of a series tapping station is where the electrical energy of rather small isolated source i.e, hydro electric generator, wind generator etc. is to be transferred to an otherwise point to point HVDC system. Such a tap will operate in rectification mode only [4, 6].

2.7.1. PRINCIPLE OF OPERATION OF SHORT CIRCUIT METHOD

A series inverter tap is inserted between nodes X and Y in a dc line as shown in Fig.2.7. Assuming that a shorting switch S is placed and it is desirable to turn on and turn off this switch S by means of a commutating circuit. By controlling the conducting to non conducting duration ratio of switch S it is possible to control the average voltage across the tap [9].

$$V_{dc} = [\frac{t_{off}}{(t_{on} + t_{off})}] * I_d * Z_L$$

where,

$t_{ON} = ON\text{-}time\ of\ switches.$

$t_{OFF} = OFF\text{-}time\ of\ switches$

$I_d = dc\ line\ current\ assumed\ constant.$

$Z_L = Equivalent\ load\ impedence$

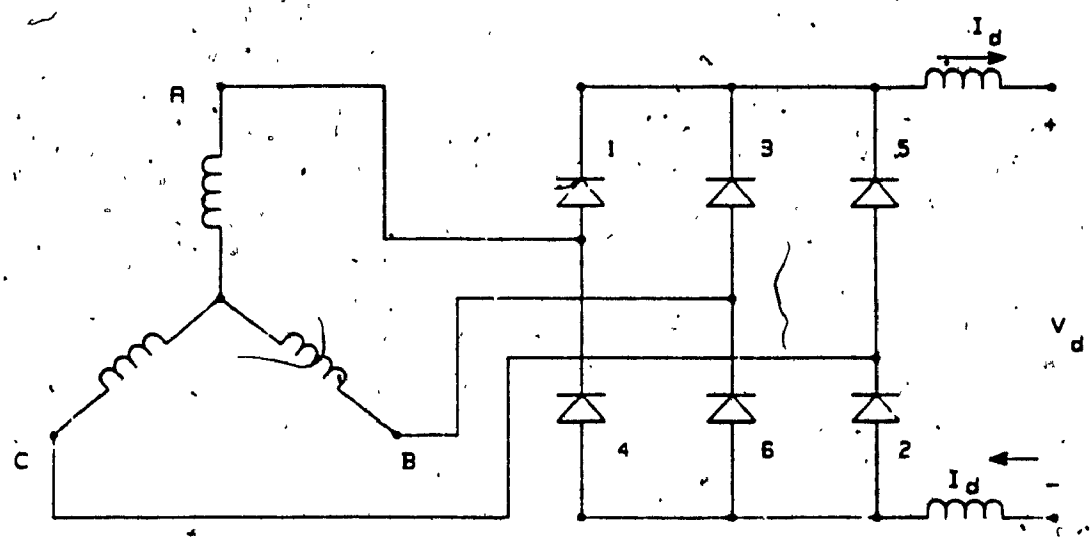

Fig. 2.6 Typical Diode Rectifier Series Tapping . Station Arrangements.

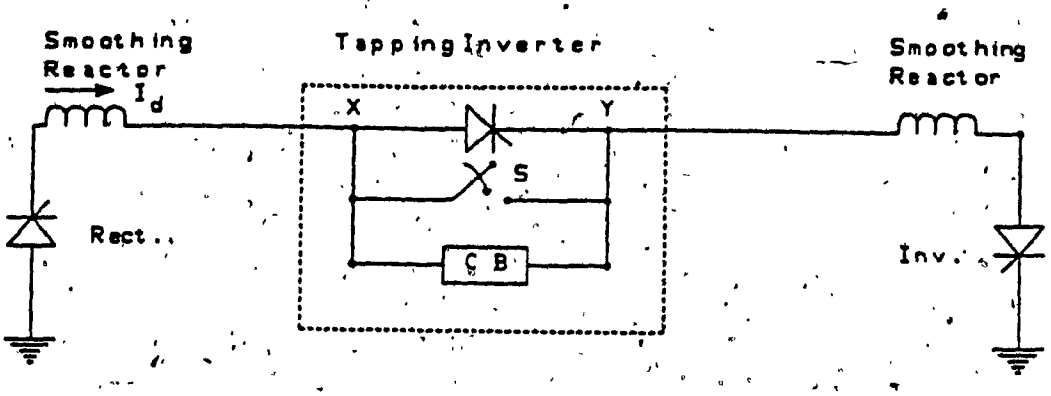

Fig. 2.7 Principle of Operation of Short Circuit Method

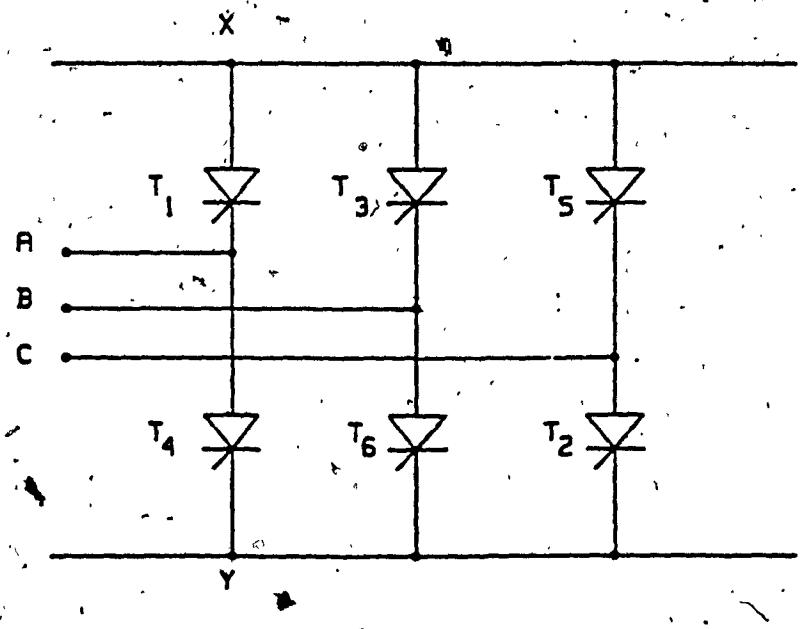

Fig. 2.8 Six Pulse Inverter

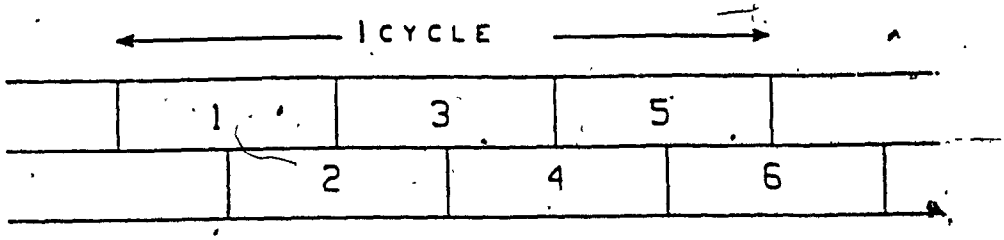

Fig. 2.9 Normal Six Pulse Bridge Valve Firing Periods.

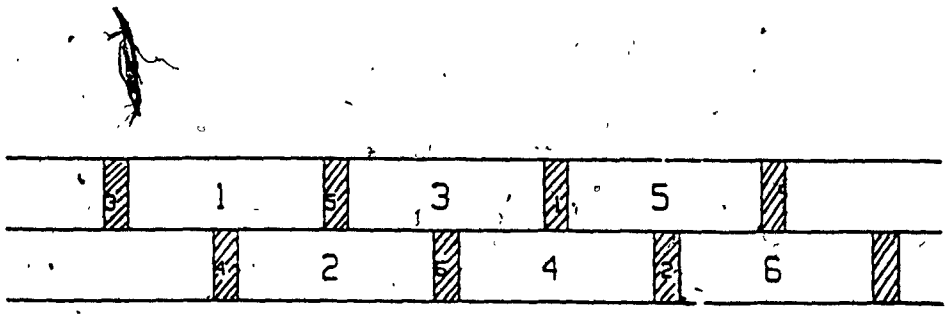

Fig. 2.10 Modified 6- Pulse Bridge Valve Firing Periods.

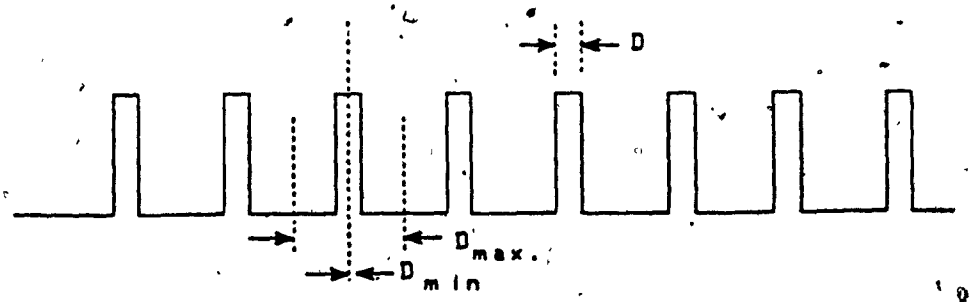

Fig. 2.11 Duration of by Pass Period.

The mean power (P_{tap}) fed into the tap load is

$$P_{dc} = V_{dc} * I_d$$

This method will be termed the short circuit method. The shorting function of the switch can be incorporated into the inverter itself, as shown in Fig.2.8. Since valves T_1 and T_4 or T_3 and T_6 or T_5 and T_2 together at the same time will cause a short circuit across the tap. The by pass function must be rotated between the three inverter arms comprising of valves T_1 and T_4 or T_3 and T_6, T_5 and T_2.

The normal firing periods of a 6-pulse inverter (neglecting overlap) are shown in Fig.2.9. These are modified as shown in Fig.2.10, to incorporate the by-pass function, where the cross hatched periods indicate when the tap is by passed. The maximum and minimums and the duration of the by pass periods are shown in Fig.2.11. Theoretically $D_{max}=60^0$ and $D_{min}=0^0$. But practically due to effects of overlap these ranges will be smaller. When the short circuit duration is $D = D_{max}$ the tap output will be zero and when $D = D_{min}$ the tap output will be maximum.

2.7.2 SHORT CIRCUIT METHOD INVERTER COMMUTATOR CIRCUIT

A commutation circuit has been proposed for the short circuit method consisting of a bridge comprising four valves CT1, CT2, CT3 and CT4, a commutation capacitor C and a $\frac{di}{dt}$ limiting inductor L. This is shown in Fig. 2.12. The valves CT1 and CT2 are fired simultaneously similarly CT3 and CT4. The capacitor C is pre-charged via a commutating circuit (not shown) in the polarity indicated [9].

Commutation is initiated by firing valves CT1 and CT2, with the polarity of the capacitor as shown. It will connect the charged capacitor across XY,

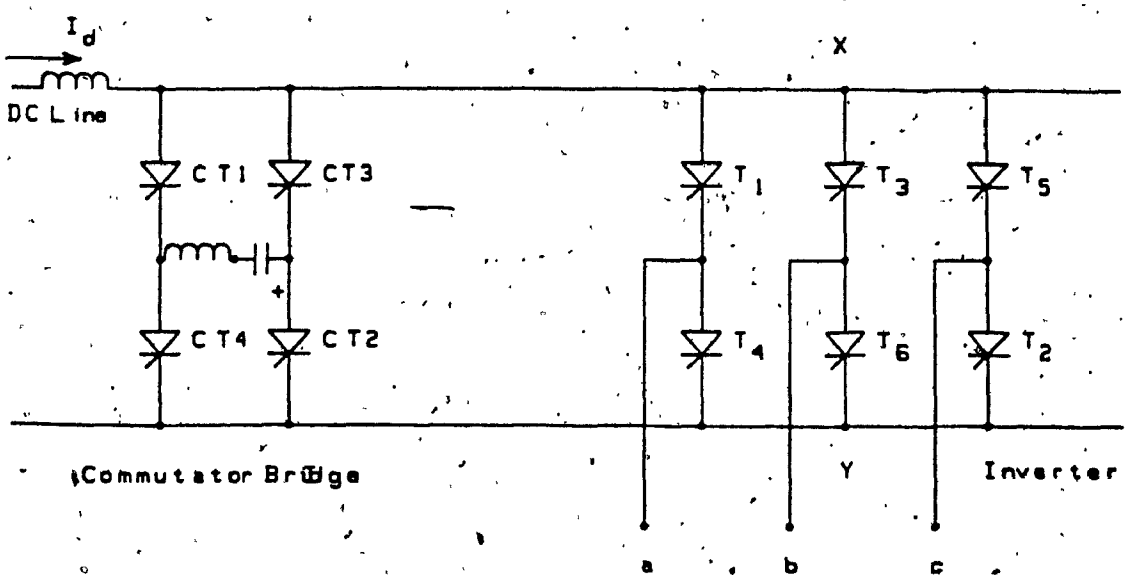

Fig. 2.12 Combined Commutator Inverter Circuit.

with terminal Y more positive than X. The dc line current flows into the capacitor rather than the inverter valves and turns the inverter valves off.

The capacitor will now be charged and its polarity will be reversed until the dc line current is transferred back to the inverter valves at the firing of the next incoming valves. For the next commutation, valves CT3 and CT4 will be fired, since the polarity of the capacitor charge will be of the opposite polarity to that shown in Fig. 2.12. The firing pulses to the commutator bridge valves are derived from the trailing edges of the by pass period. Alternate pulses from this train of pulses fire CT1 and CT2 , CT3 and CT4.

2.8 COMPARISON BETWEEN SHORT CIRCUIT METHOD AND DIFFERENTIAL FIRING METHOD

The series tap with short circuit method has no need for reactive power compensation provided there is no overlap. Since no reactive power compensation is necessary low cost high impedance filters are possible [9], this inverter can feed a dead load with no generation capability. A feature of this inverter is its ability to recover rapidly from most system faults. One major problem of this method is the harmonics. The short circuit method uses the pulse width modulation technique. By increasing the number of pulses per half cycle , harmonics can be reduced. Other disadvantages of this method are increased number of components, requirement for a start up circuit, increased valve stresses and increased complexity.

By the differential firing method the harmonics can be controlled and the reactive power of the bridges can also be controlled [4, 6]. Some voltage regulation on the tap's ac bus can be exercised by differential firing method. Voltage regulation capability can be increased by increasing the number of bridges in series. This method can not feed into a system which has no generation capability.

CHAPTER 3

ANALYSIS OF HARMONICS GENERATED BY A SERIES TAP

3.1 INTRODUCTION

Harmonics will be generated by a series tap. These harmonics will be generated into the output ac current, voltage in the dc side and some harmonics will also be injected into the dc line current.

The ac current harmonics generated by a forced commutated inverter are usually higher than those of a line commutated inverter. There is always some overlap in a practical converter, which also has an effect on the harmonics.

In order to determine the order and magnitudes of the harmonics generated by the system, an analysis has been done in this chapter.

3.2 HARMONICS

3.2.1 AC HARMONICS

In HVDC books the magnitudes of the characteristic harmonics are usually plotted against the overlap angle with firing angle as a parameter. However, in our case the harmonic magnitude is plotted against the short circuit angle with overlap angle as a parameter.

The theoretical waveform of the transformer current in one phase for a line commutated converter is shown in Fig.3.1. The corresponding waveform for a 6-pulse short circuit method FC converter is shown in Fig.3.2. The effects of overlap have been neglected. The mean value of the current for the FC converter can be varied by controlling the period d. As d approaches zero the two current waveforms become identical. Fourier analysis of the FC converter

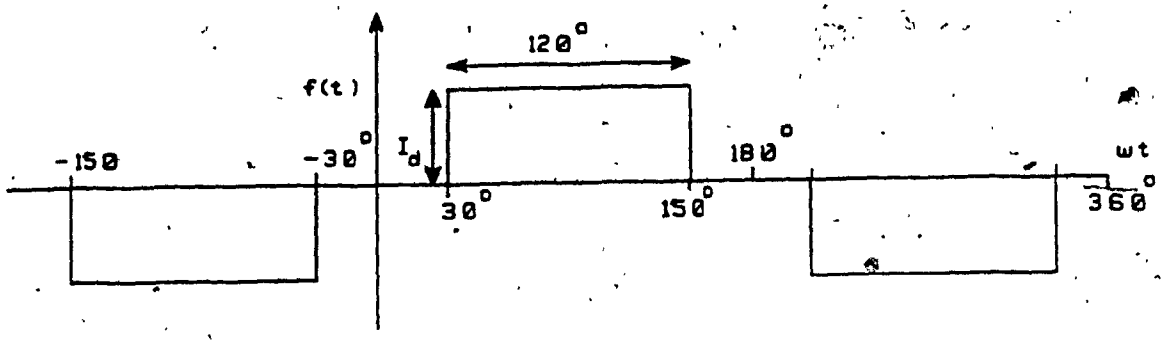

Fig. 3.1 Normal 6-Pulse Current Wave Shape

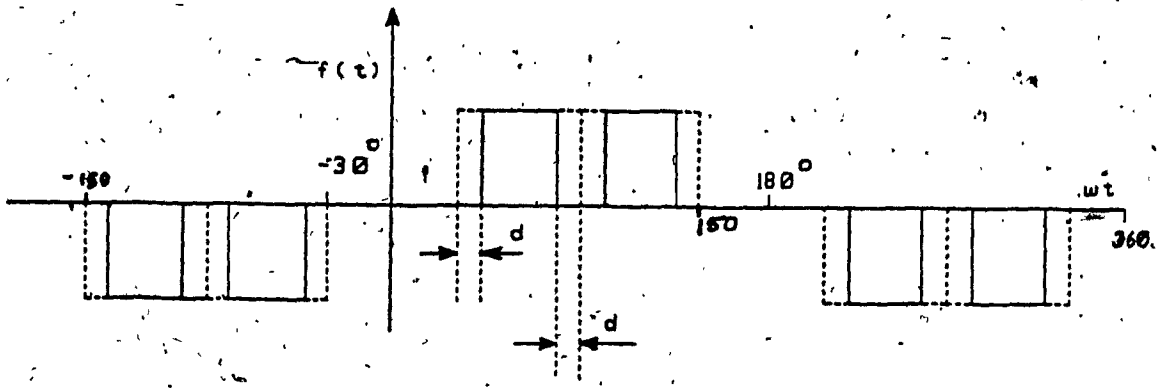

Fig. 3.2 Approximate Waveform of Transformer Current with no Overlap for Short Circuit Method.

current wave (neglecting overlap) reveals the following components [23].

$$f(t) = \sum_{n=1,5,7}^{n=inf} \frac{4I_d}{n\pi}\left\{ -\cos n(\frac{\pi}{2} - d) + \cos n(\frac{\pi}{6} + d)\right\}\sin n\omega t \quad (3.1.)$$

where,

n= order of harmonic.

$d = \frac{1}{2}$ short circuit period.

$I_d =$ dc line current (assumed constant).

3.2.2 EFFECT OF OVERLAP

Equation 3.1 describes the harmonics present in the transformer current assuming that there is no leakage reactance and the dc line current is constant. But in reality converter transformer has some leakage inductance (18-20%). This leakage inductance causes rounding of the edges of the current block. The rounding of the edges has different shapes for the leading and trailing edges since different parts of the sine wave are involved when the current is increasing and decreasing. A secondary effect of this is to shift the center axis of the current block as shown in Fig. 3.3. This phase shift is a reflection of the reactive power being consumed by the converter transformer leakage.

In order to simplify the analysis the effect of the overlap angle is linearly approximated by a trapezoidal shape as shown in Fig.3.4, the primary effect of the overlap is to modify the harmonic content of the waveforms [23].

The trapezoidal waveform f(t) shown in Fig.3.4, is comprised of three components.

$$f(t) = f_1(t) + f_2(t) + f_3(t) \quad (3.2)$$

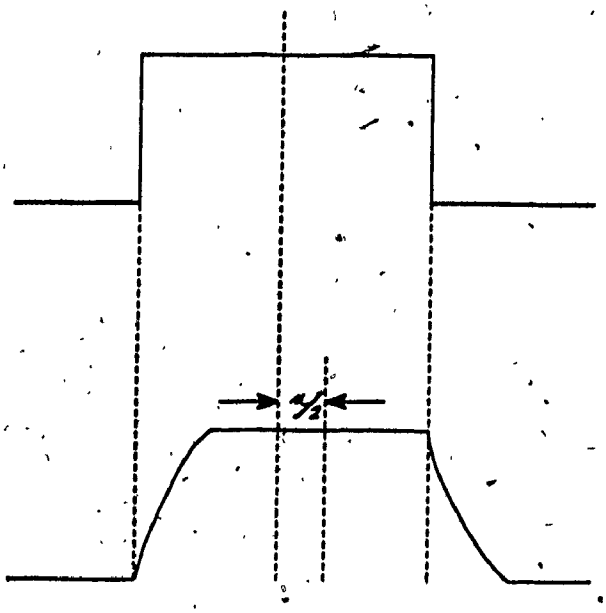

Fig. 3.3 Current Block with Overlap and no Overlap

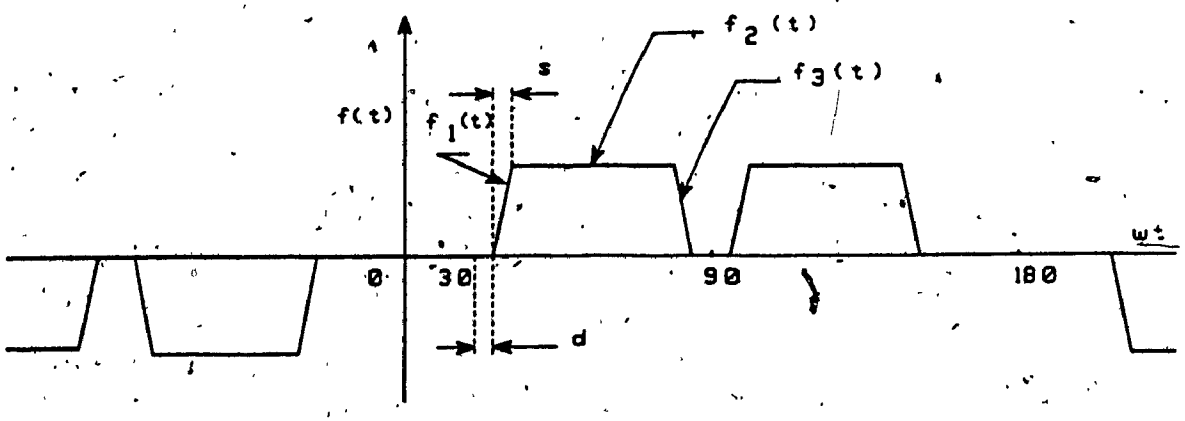

Fig. 3.4 Approximated Waveform of Transformer Current.

where,

$$f_1(t) = \frac{[t-(\frac{\pi}{6})-d]}{s} \quad , \quad [\frac{\pi}{6}+d] \leq t \leq [\frac{\pi}{6}+d+s] \tag{3.3.}$$
$$= 0 \quad , \quad \text{for } \textit{the rest of period}$$

$$f_2(t) = 1 \quad , \quad [(\frac{\pi}{6}) + d + s] \leq t \leq [\frac{\pi}{6} + d + s + p] \tag{3.4.}$$
$$= 0 \quad , \quad \text{for } \textit{the rest of period}$$

$$f_3(t) = [1 - \frac{(t-(\frac{\pi}{6})-d-s-p)}{s}] \quad , \quad [(\frac{\pi}{6})+d+s+p] \leq t \leq [(\frac{\pi}{6})+d+2s+p]$$
$$= 0 \quad , \quad \text{for } \textit{the rest of period} \tag{3.5.}$$

It is assumed that the magnitude of the dc current I_d is constant.

The final expression for the Fourier analysis of the wave is.

$$f(t) = \frac{4}{\pi} \sum_{n=6k\pm1}^{n=inf} \frac{1}{n^2 s} \Big\{ \sin n(\frac{\pi}{6} + d + s) - \sin n(\frac{\pi}{6} + d) + \sin n(\frac{\pi}{6} + d + s + p) - \sin n(\frac{\pi}{6} + d + 2s + p) \Big\} \sin n\omega t \tag{3.6.}$$

where, $p = \frac{\pi}{3} - 2d - 2s$

when s=0 Eqn. [3.6] becomes indeterminate and it is necessary to utilize L-hospitals rule. This enables equation [3.1] to be derived from Eqn. [3.6].

Plots of harmonic content versus d for different values of overlap s equal to 0^0, 5^0 and 10^0 are shown in Fig. 3.5, 3.6, and 3.7. The harmonic magnitudes has been normalized by the maximum fundamental current magnitude ($I_{1max} = \frac{4}{\pi} * cos\frac{\pi}{6}$) of the 6-pulse line commutated inverter.

It is evident from the figures that as the overlap is increased;

(a) The fundamental peaks are reduced.

(b) The range of operation for d=D/2 is reduced.

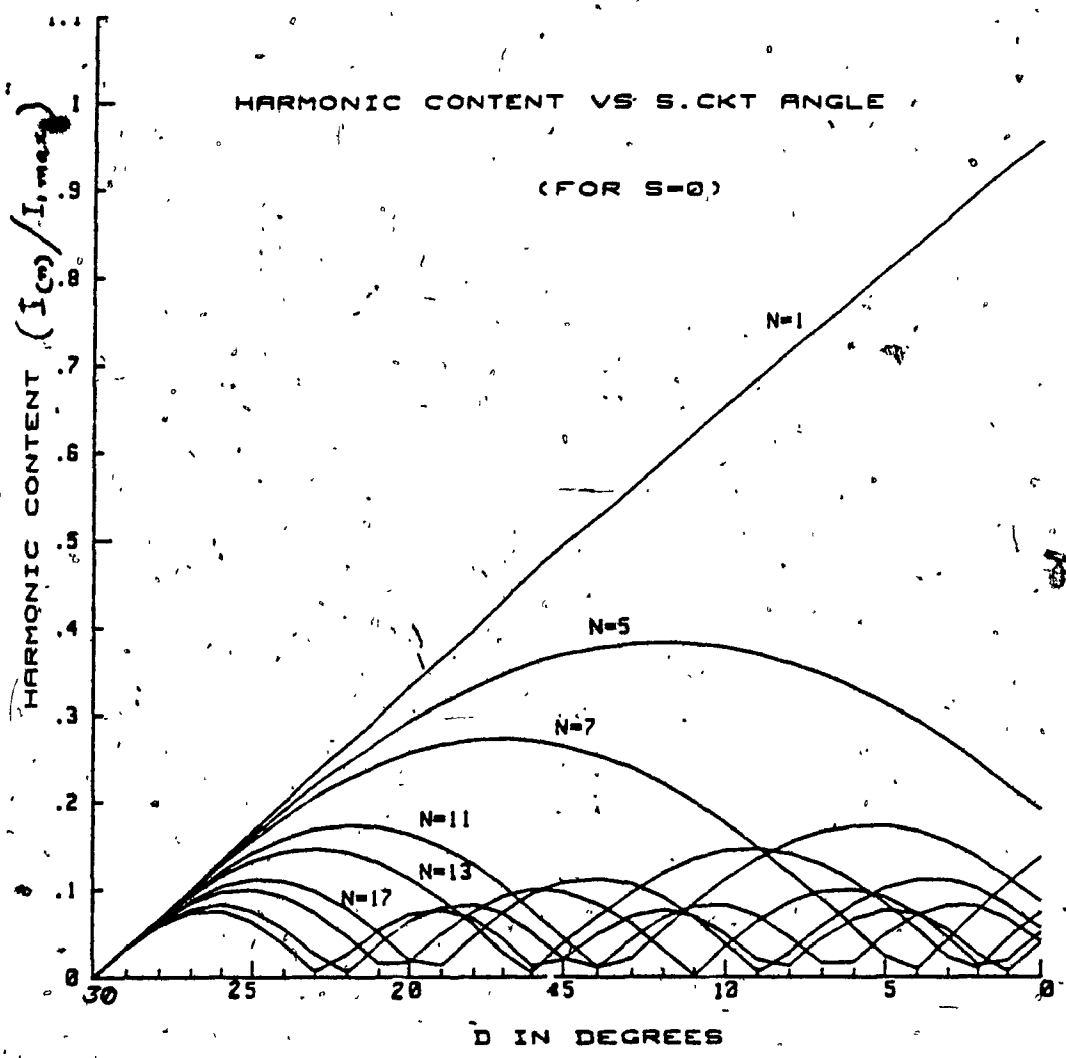

Fig. 3.5 Plot of AC Harmonic Content vs Short Circuit Angle for no Overlap.

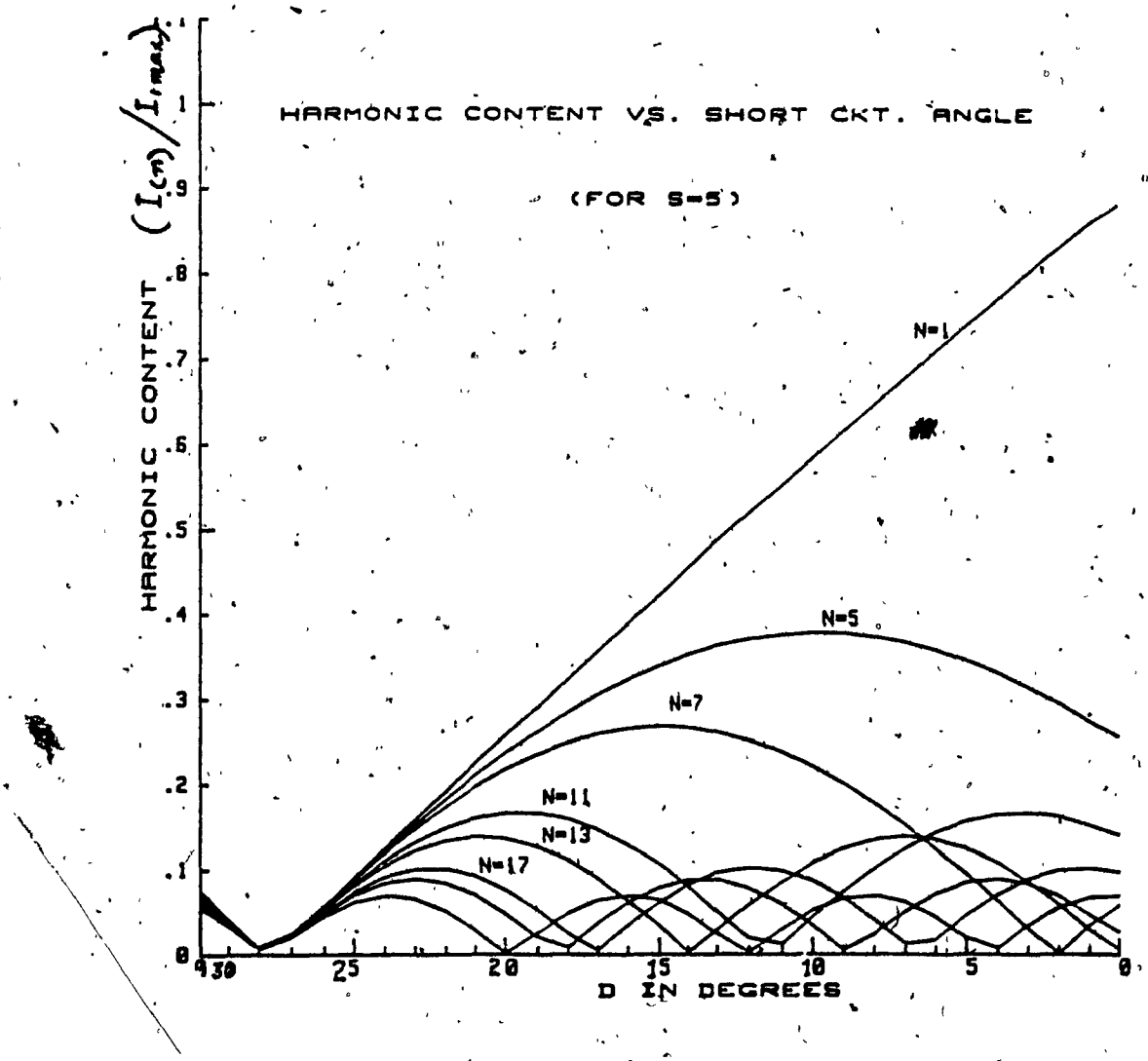

Fig. 3.6 Plot of AC Harmonic Content vs Short Circuit Angle for Overlap Angle of 5 deg.

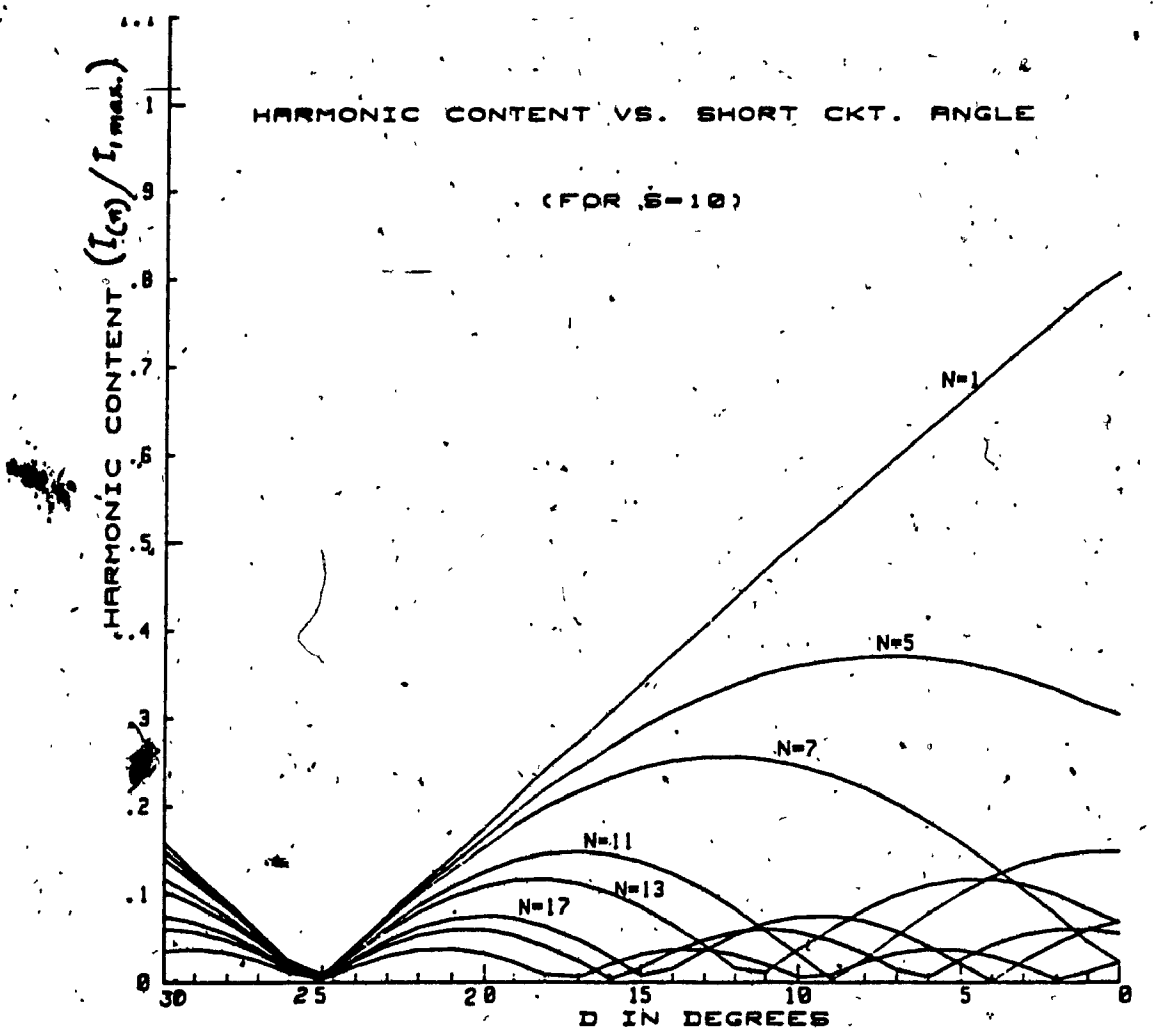

Fig. 3.7 Plot of AC Harmonic Content vs Short Circuit Angle for Overlap Angle of 10 deg.

3. DC VOLTAGE HARMONICS

For determining dc voltage harmonics the following analysis will be necessary.

The transfer function of a converter can be expressed in terms of its Fourier series.

$$S(\theta) = \sum H_n \sin(n\theta + \psi_n) \tag{3.6}$$

Considering the converter as a set of modulating switches and assuming $S_1(\theta)$, $S_2(\theta)$, $S_3(\theta)$ as the transfer functions of the switches with respect to the input port of the converter and assuming the supply voltages as

$$V_1 = E\sin(\theta)$$
$$V_2 = E\sin(\theta - 120^\circ)$$
$$V_3 = E\sin(\theta - 240^\circ)$$

Output voltage expression becomes

$$V_0(\theta) = V_i(\theta)S(\theta) \tag{3.8.}$$
$$V_0(\theta) = F_1(\theta) + F_2(\theta) + F_3(\theta)$$

where,

$$F_1(\theta) = S_1(\theta)E\sin(\theta) \tag{3.9.}$$
$$F_2(\theta) = S_2(\theta)E\sin(\theta - 120^\circ) \tag{3.10.}$$
$$F_3(\theta) = S_3(\theta)E\sin(\theta - 240^0) \tag{3.11.}$$

By using simple trigonometrical relations the average output voltage becomes

$$V_{dc} = \frac{3}{2}EH_1 \tag{3.12.}$$

Following the same procedure the m^{th} harmonic component of the output voltage can be expressed as

$$V_{om} = E\frac{H_{m+1}}{2}\cos m\theta - E\frac{H_{m-1}}{2}\cos m\theta \tag{3.13.}$$
$$+ \frac{EH_{m+1}}{2}\cos(m\theta - m*120^\circ) - \frac{EH_{m-1}}{2}\cos(m\theta - m*120^\circ)$$
$$+ \frac{EH_{m+1}}{2}\cos(m\theta - m*240^\circ) - \frac{EH_{m-1}}{2}\cos(m\theta - m*240^\circ) -$$

where,

$$H_n = \frac{4}{\pi n}\left\{-\cos n\left(\frac{\pi}{2} - d\right) + \cos n\left(\frac{\pi}{6} + d\right)\right\} \qquad (3.14.)$$

Details of the derivation are given in Appendix B.

Plot of dc voltage harmonic content versus d, is shown in Fig. 3.8 [23]. The harmonic magnitudes have been normalized by the no-load dc voltage of the tap.

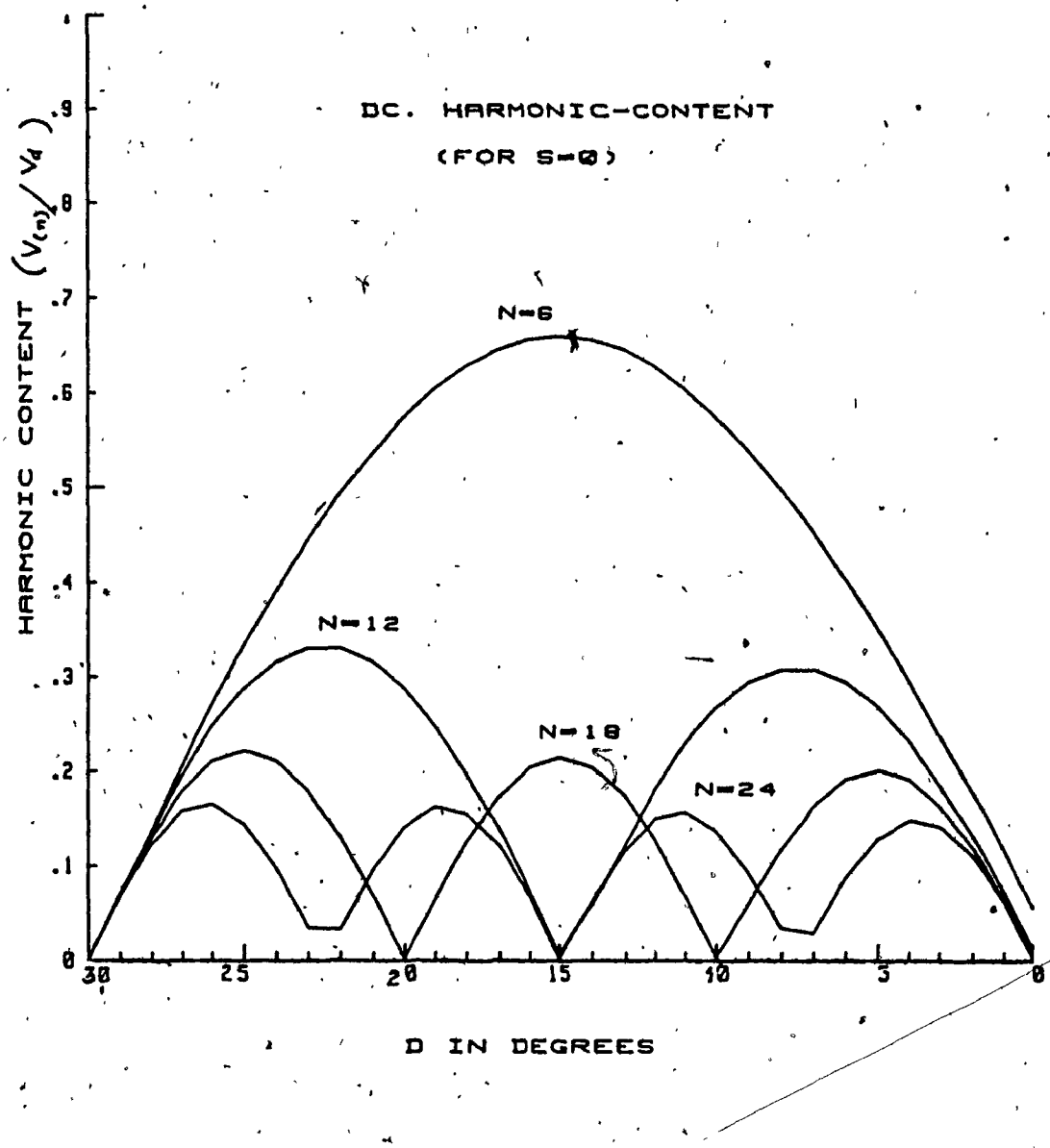

Fig. 3.8 Plot of DC Voltage Harmonic Content vs Short Circuit Angle for Overlap Angle s=0

3.4 HARMONIC REDUCTION

The harmonic spectrum of the current wave for the short circuit method are shown in Fig. 3.5, 3.6, and 3.7. The harmonic contents are quite high for the low order harmonic frequencies compared to the fundamental. Because of this high harmonic content the filtering requirement will be severe and it would be expensive. The conventional method of harmonic reduction is to increase the pulse number. But increasing the pulse number has limitations in that it increases the number of transformers in service and associated complexity of connection. For a HVDC scheme only simple transformer connections are used. A pulse number of twelve is obtained with star/star and star/delta transformer connections as shown in Fig.3.9. For more than twelve pulse operation, this method has been found to be uneconomic.

3.4.1 SYMMETRIC PULSE WIDTH MODULATION

Many techniques have been developed to reduce low order harmonics in the inverter output. The short circuit method is actually a 2-pulse per half cycle symmetric pulse width modulation technique. The harmonics in the output waveform of the inverter can be limited by varying the widths of the pulses symmetrically. In this arrangement the maximum conduction interval for each half cycle is 120^{o}. To vary the output from this maximum value, the output wave shape is divided into a number of symmetrical pulses whose widths are to be varied to achieve the desired control [20].

A computer program has been developed to plot the harmonic content vs relative pulse width for different numbers of pulses per half cycle. Figs. 3.12, 3.13, and 3.14 show respectively the harmonic spectra for 4-pulse per half cycle, 8-pulse per half cycle and 16-pulse per half cycle operation. From Fig,3.12 it is evident 4pulse per half cycle operation there is

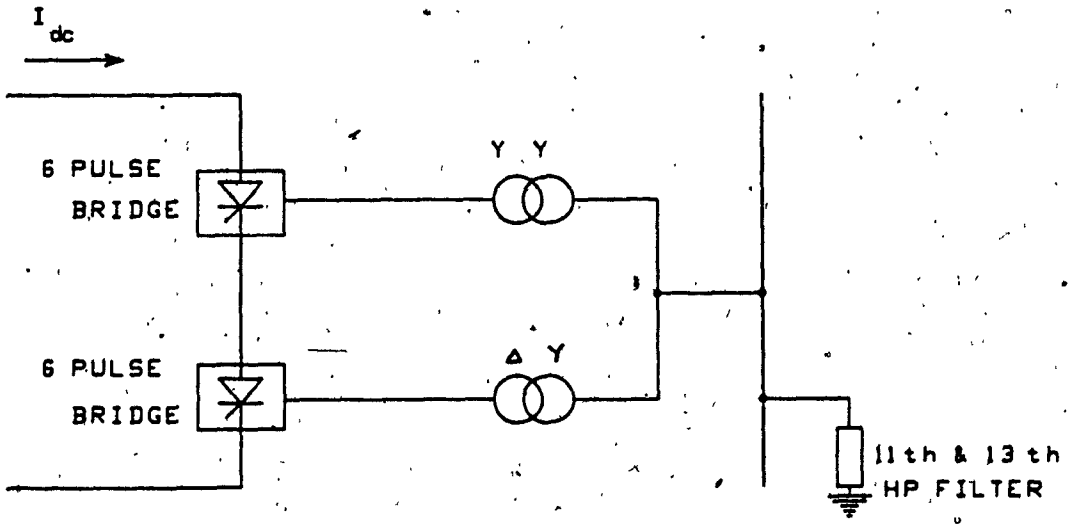

Fig. 3.9 12- Pulse Operation of Converter by Using Two Six Pulse Bridges and Transformer.

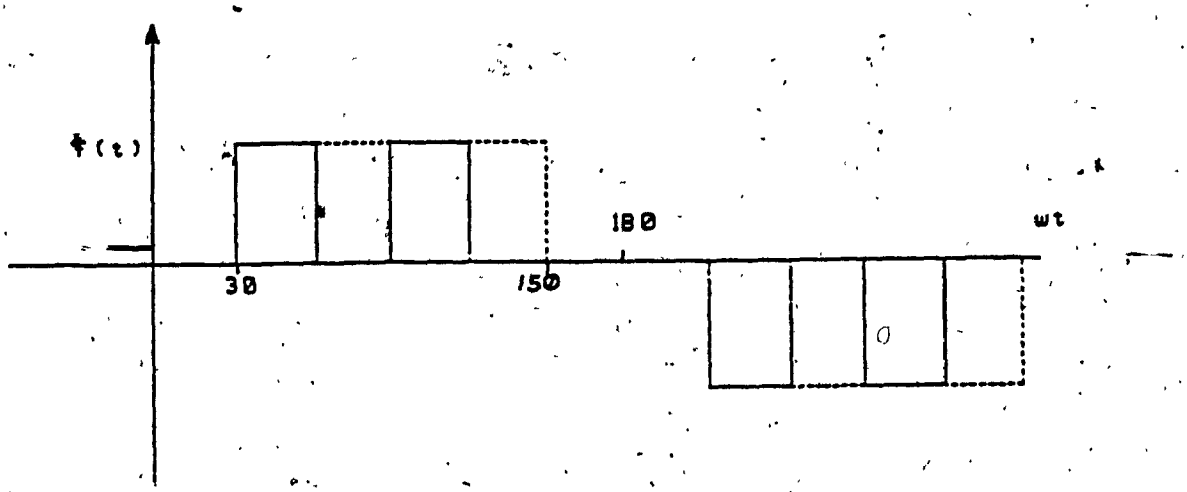

Fig. 3.10 2-Symmetric Pulse Per Half Cycle.

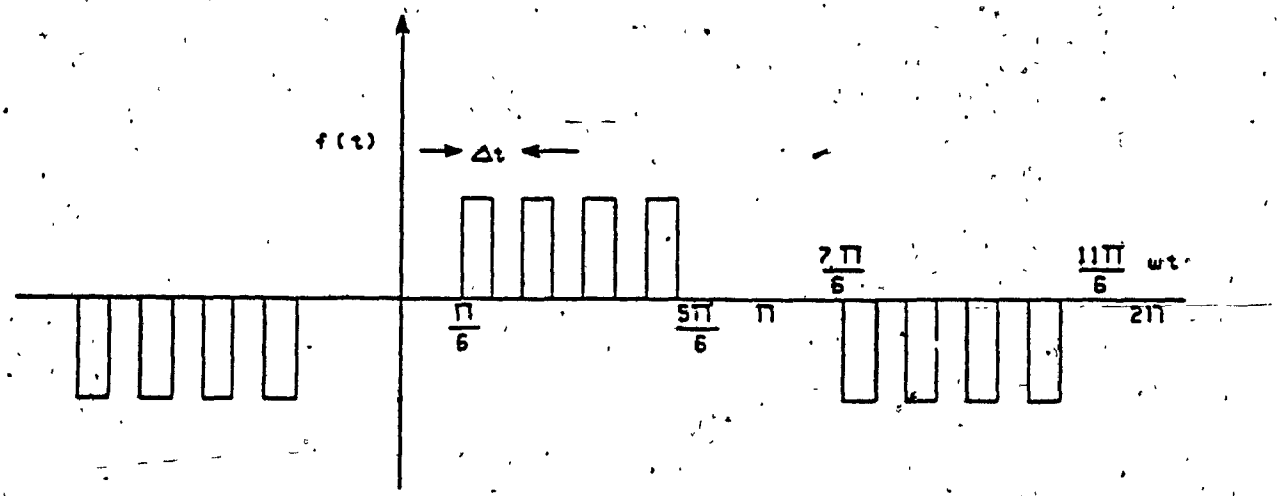

Fig. 3.11 4-Symmetric Pulse Per Half Cycle.

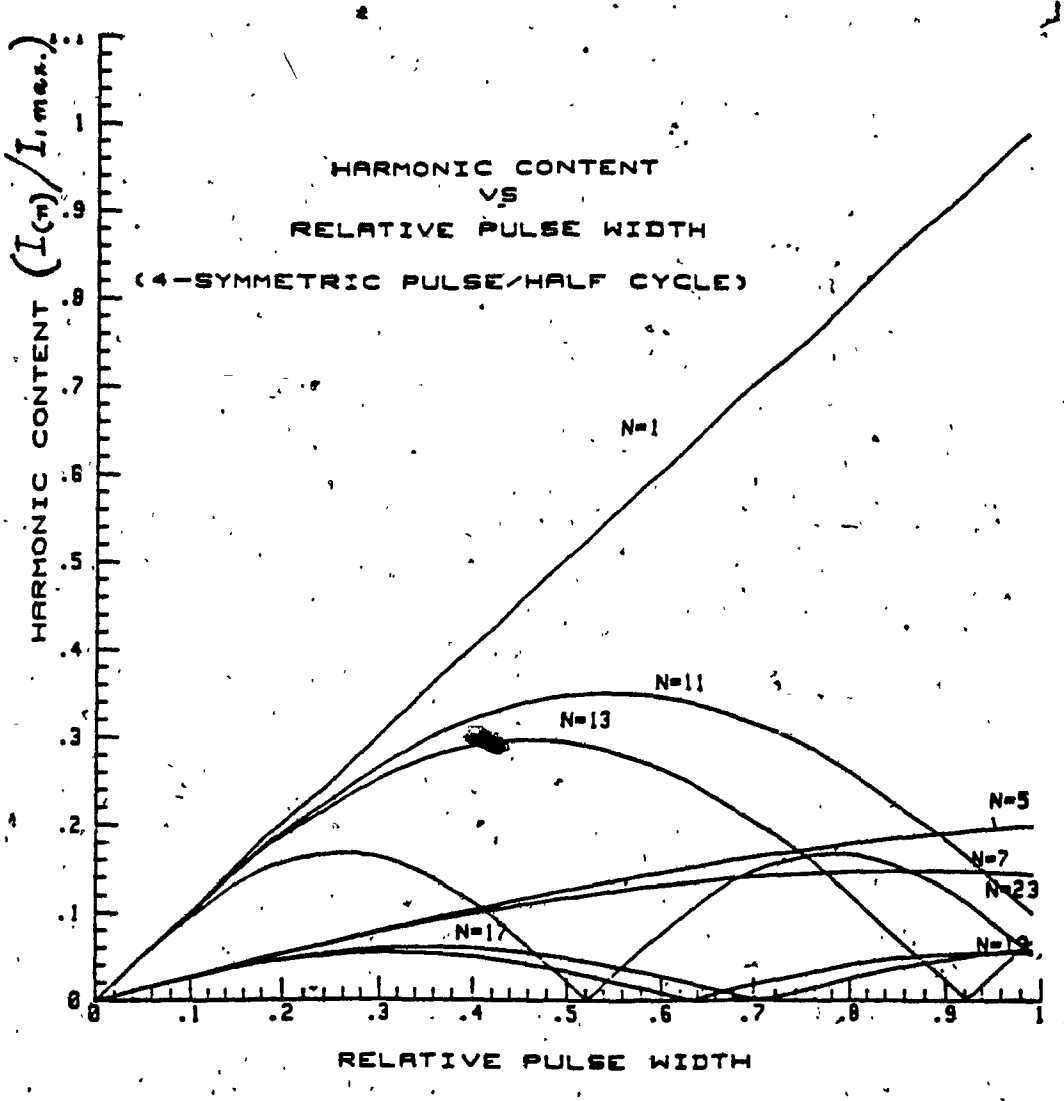

Fig. 3.12 Plot of AC Harmonic Content vs Relative Pulse Width for 4-Symmetric Pulse Per Half Cycle.

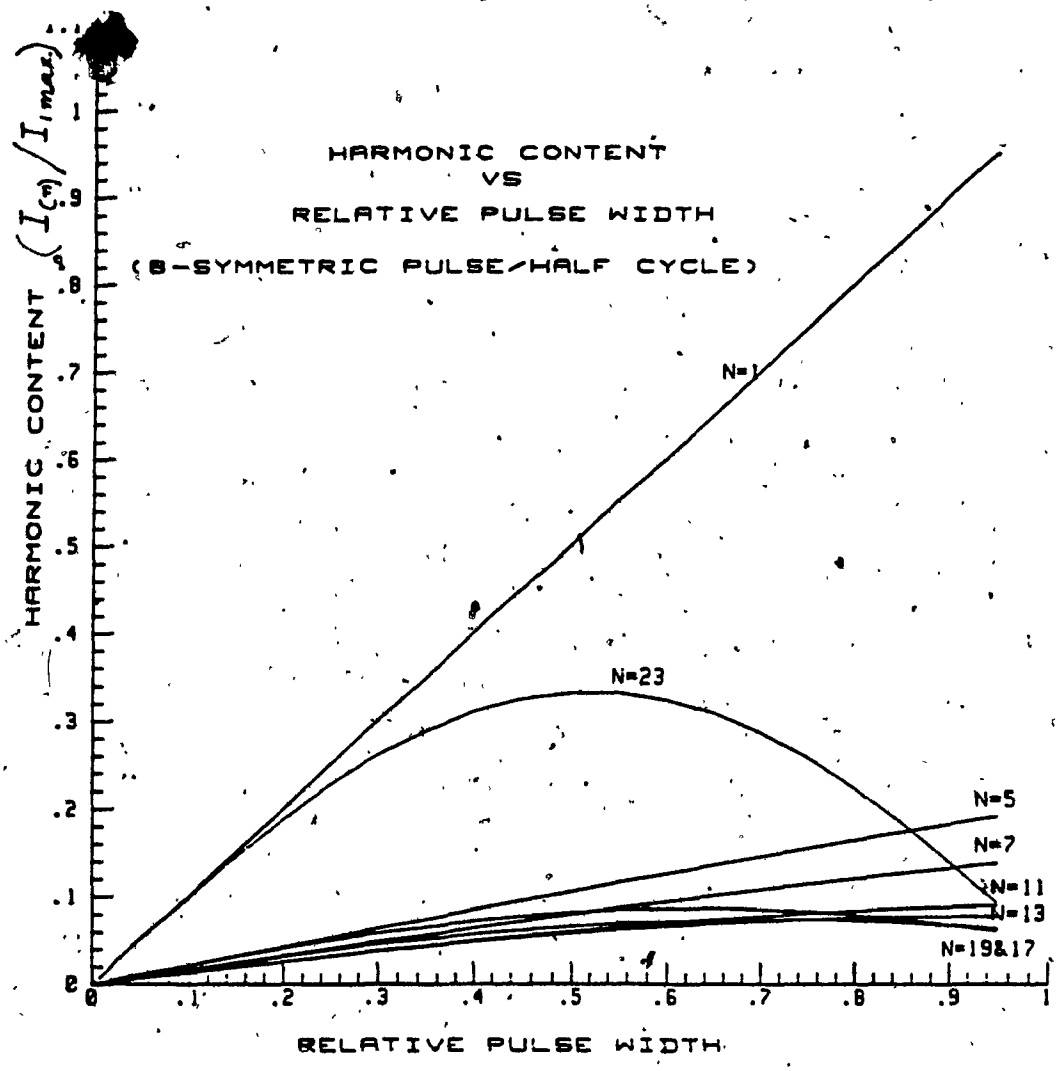

Fig. 3.13 Plot of AC Harmonic Content vs Relative Pulse Width for 8-Symmetric Pulse Per Half Cycle.

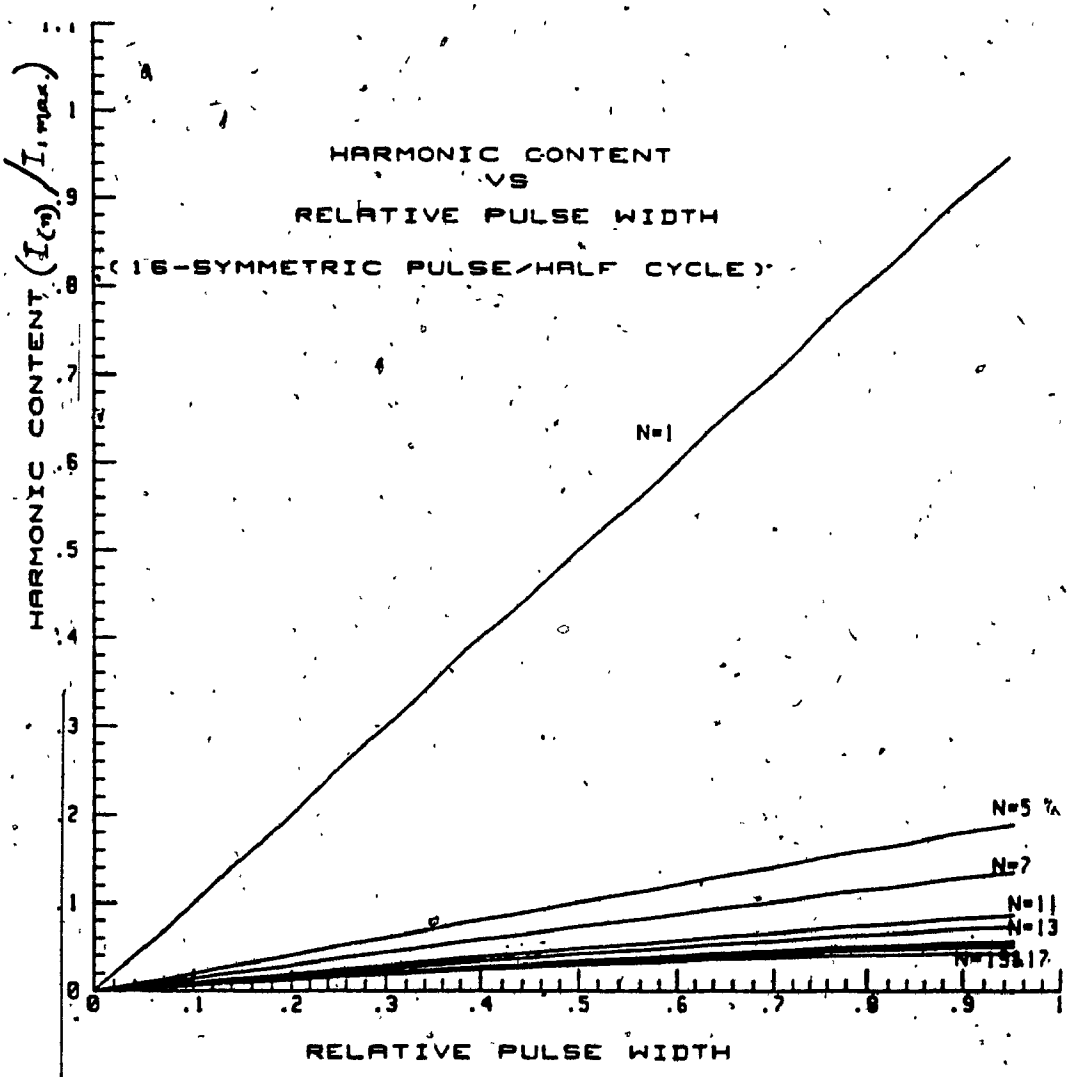

Fig. 3.14 Plot of AC Harmonic Content vs Relative Pulse Width for 16-Symmetric Pulse Per Half Cycle.

no significant changes in the harmonic content of the lower order harmonics. The 5th and 7th harmonics decrease but the 11th and the 13th harmonics increase from that of 2-pulse per half cycle operation. From Figs. 3.13 and 3.14 it is evident that for 8-pulse per half cycle 16pulse per half cycle operation the lower order harmonics decrease significantly.

3.4.2 SINUSOIDAL PULSE WIDTH MODULATION

For harmonic control the sinusoidal pulse width modulation technique is presently the most popular and effective. Fig. 3.15 shows the scheme for the SPWM technique [21].

The outputs in this scheme can be controlled by controlling the modulation index, i.e the controller will control the modulation index according to the desired output.

A computer program has been developed to plot the harmonic content vs modulation index for different numbers of pulses. Figs. 3.16, 3.17 and 3.18 show the harmonic spectra for 4-pulse per half cycle, 8-pulse per half cycle and 16-pulse per half cycle operation respectively. Fig. 3.16 shows that the lower order harmonics in 4-pulse per half cycle operation are quite high. In the 8-pulse per half cycle operation (Fig.3.17) and 16-pulse per half cycle operation the lower order harmonics are almost eliminated. The harmonic content for the same number of pulses per half cycle operation in this method is lower than that of symmetric pulse width modulation technique; i.e this method is more effective in harmonic reduction. But there is one limitation of this method; i.e the maximum achievable output rating is lower than that can be achieved with symmetric pulse width modulation, and the output rating of the tap will decrease.

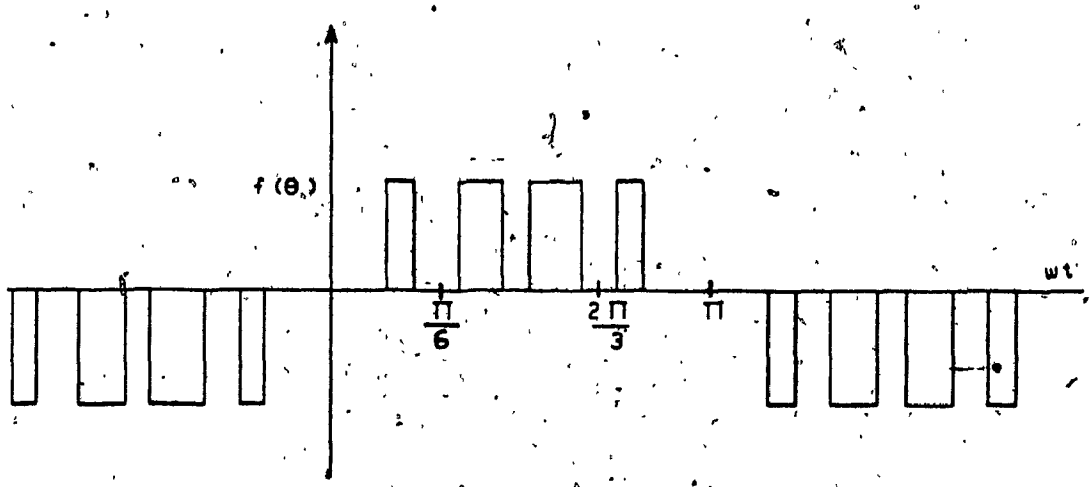

Fig. 3.15 Sinusoidal Pulse Width Modulation.

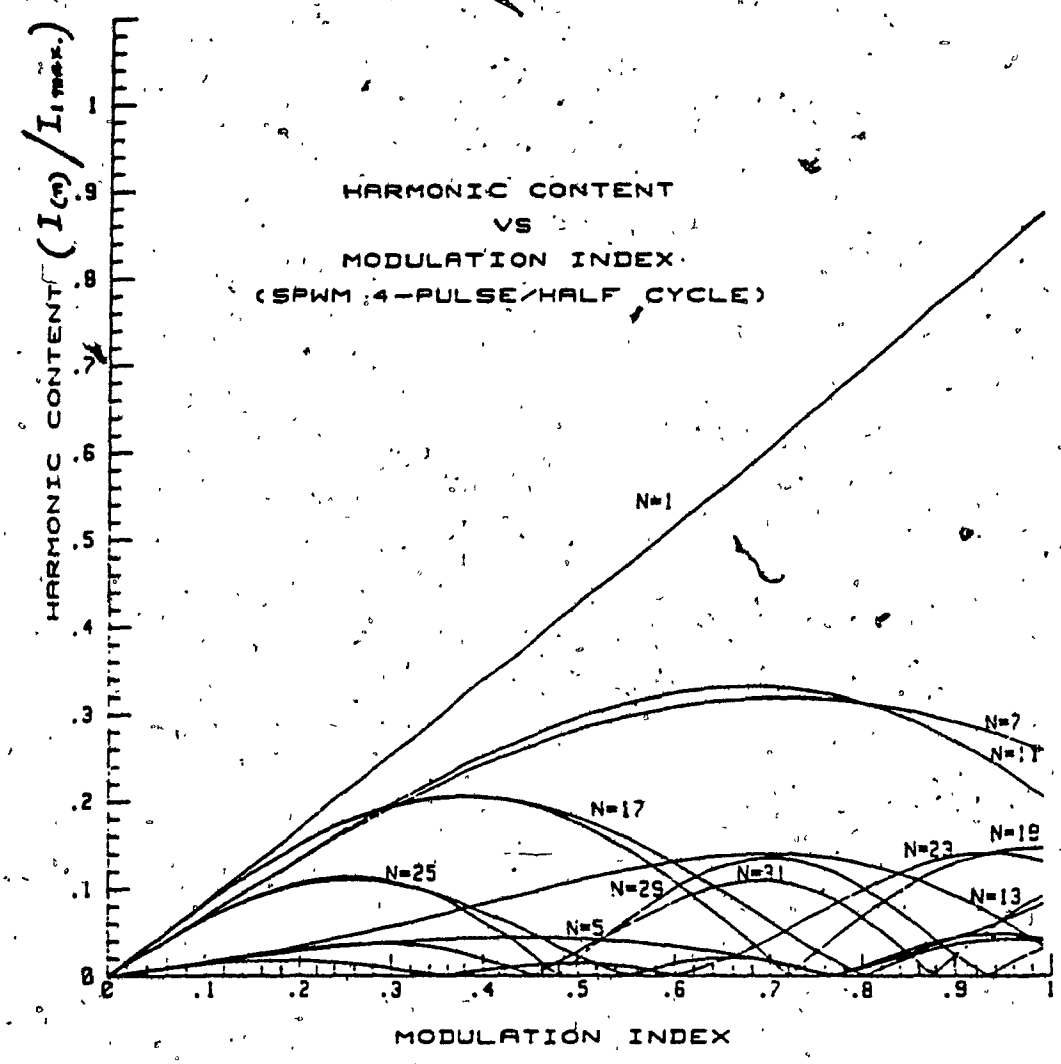

Fig. 3.16 Plot of AC Harmonic Content vs Modulation Index for SPWM 4- Pulse Per Half Cycle.

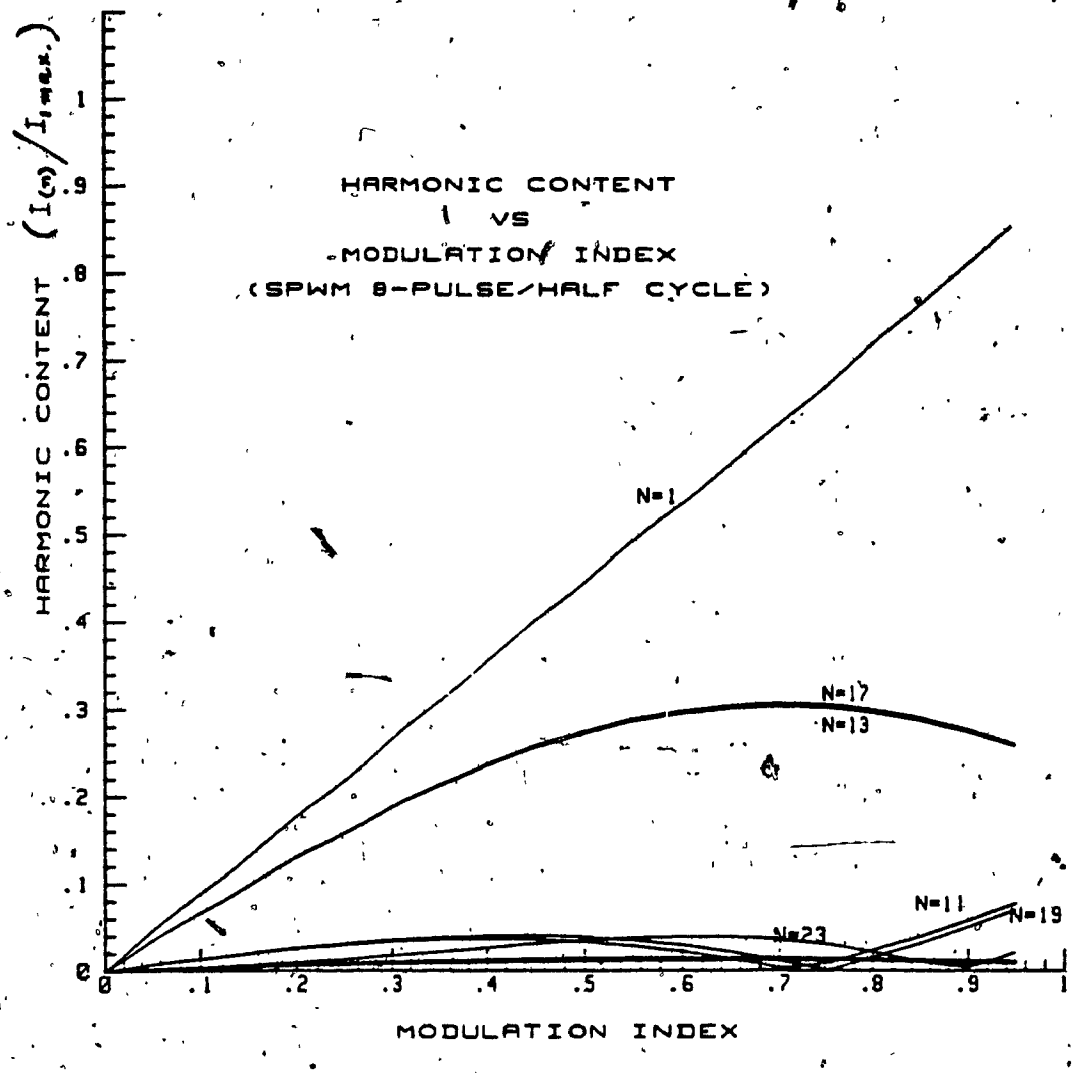

Fig. 3.17 Plot of AC Harmonic Content vs Modulation Index for SPWM 8-Pulse Per Half Cycle.

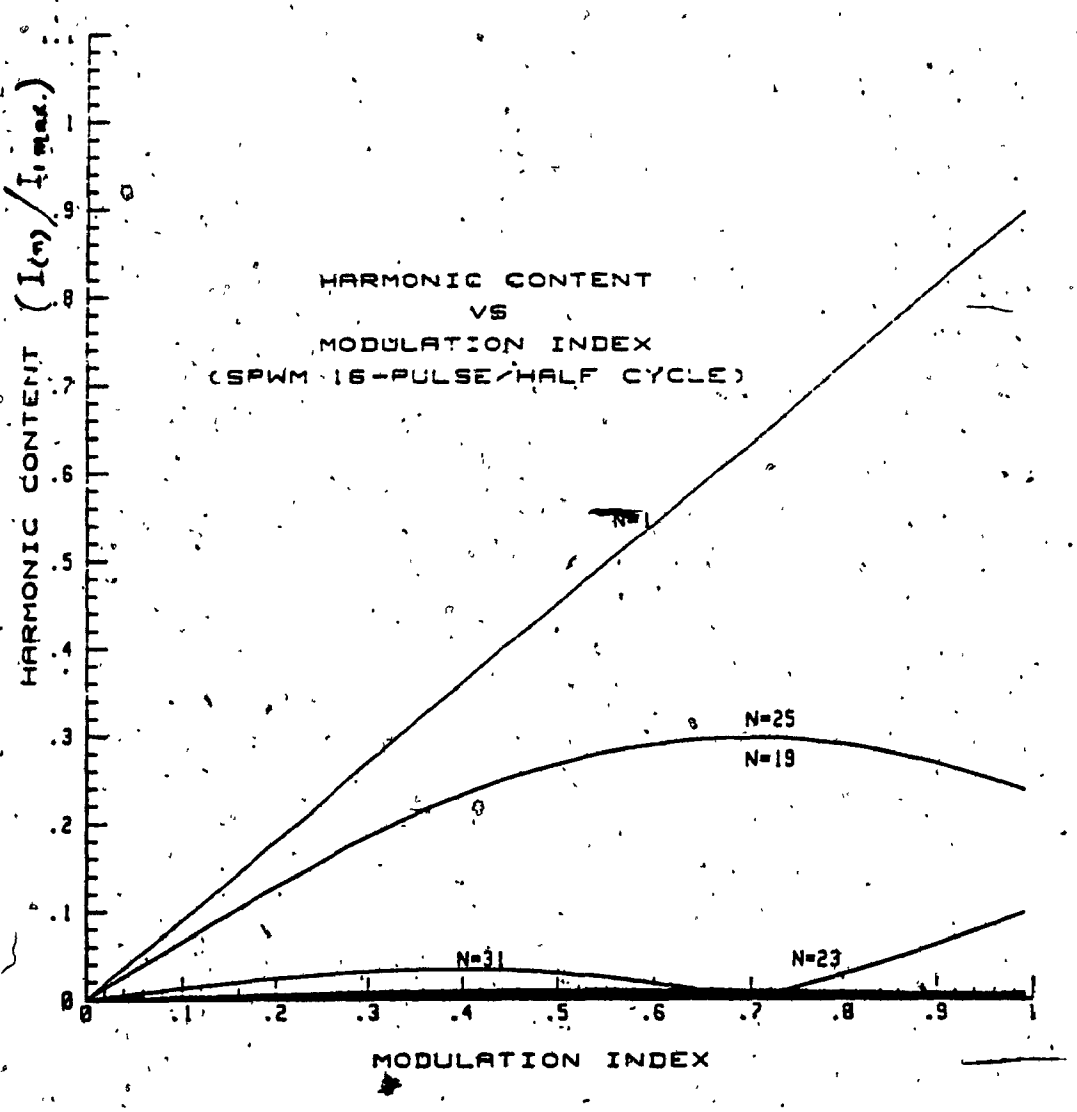

Fig.3.18 Plot of AC Harmonic Content vs Modulation Index for SPWM 16- Pulse per Half Cycle.

3.4.3 HARMONIC ELIMINATION

The undesirable harmonics content of the square wave can be eliminated and the fundamental component of the output can be controlled as well by the harmonic elimination method. In this method notches will be created on the square wave at predetermined angles.

The harmonic elimination method can be conveniently implemented to eliminate and control the inverter output current with a microcomputer using a look-up table of notch angles. At a certain command current or output, the angles will be retrieved from a look-up table and corresponding pulse widths will be generated. For successful operation minimum pulse widths and notch angles will be maintained for commutation.

A computer program was developed to calculate the switching angles for specific harmonic elimination (Fig. 3.19.).

3.4.4 DRAW BACKS OF UNCONVENTIONAL METHODS

There are practical problems associated with all these methods, particularly their application in HVDC. A self commutating valve of high rating suitable for HVDC application has yet to be developed. The main problem is due to the increased number of commutations per half cycle. The number of pulses per half cycle will be limited by turn off requirement of the devices and due to their application in HVDC. A compromise will be necessary for an economical and efficient system. 8-pulse per half cycle will be a reasonable choice considering harmonic reduction capability and due to their application in HVDC.

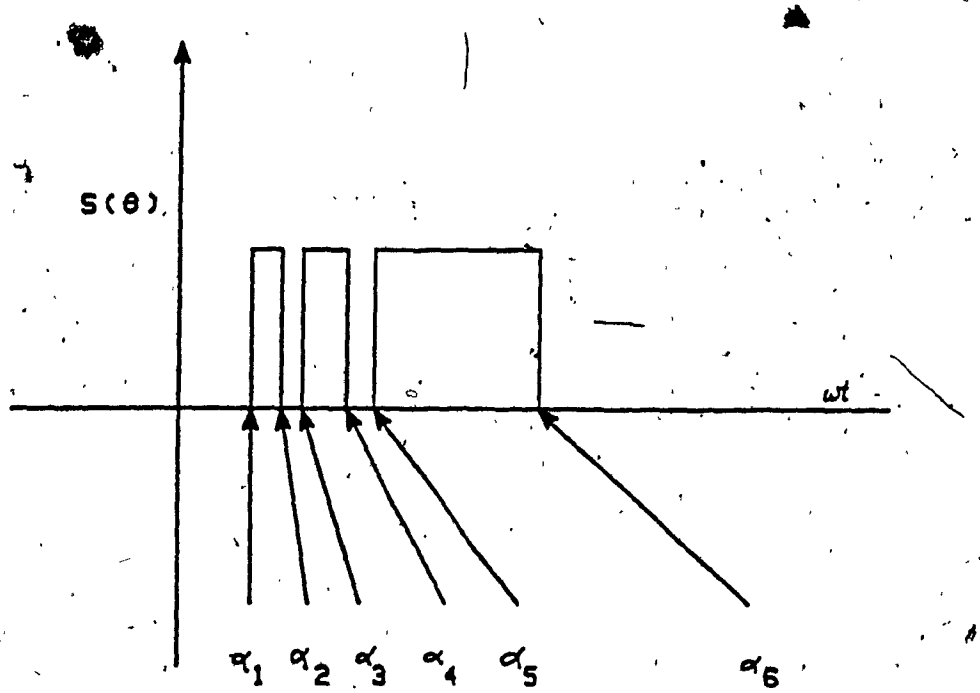

Fig. 3.19 Specific Harmonic Elimination and Switching Angles. Solutions for eliminating 5th, 7th, 11th, 13th, 17th, and 19th harmonics

$\alpha_1 = 10.072^\circ$, $\alpha_2 = 14.306^\circ$,

$\alpha_3 = 20.653^\circ$, $\alpha_4 = 41.796^\circ$,

$\alpha_5 = 42.817^\circ$, $\alpha_6 = 88.410^\circ$,

CHAPTER 4

DYNAMIC STUDY AND CONTROL OF THE TAPPING STATION

4.1 INTRODUCTION

There will always be some disturbance in the tapping station due to faults in the station or due to load changes. There may also be some disturbance in the main dc system. All of these load changes or faults will affect the operation of the tapping station. Moreover, the control of the tapping station is also very important. The control and behavior of the tap due to disturbances or load changes can be studied by digital or analog simulation. But before the system (i.e tapping station and associated dc line) is to be simulated a small disturbance analysis of the tap is important for evaluation of the controls. With a view to these the network for dynamic study is presented, control strategy discussed and a small disturbance analysis made in this chapter.

4.2 NETWORK FOR DYNAMIC STUDY AND CONTROLS

Fig. 4.1, illustrates a constant current dc system in which is inserted a series tap that will be considered for disturbance analysis.

The tap consists of two bridges acting as one twelve pulse bridge set and the tap acts into an ac system which has no other source of power. That means the tap will act as an inverter. A synchronous condenser is used at the taps ac bus. The tap does not draw any reactive power so the synchronous condenser can be of low reactive power capacity. The rated reactive power supplied by the synchronous condenser is 50% of the real power of the tap. The filters (11th, 13th tuned & high-pass) supply part of the reactive power. (Details of Filter are given in Appendix-C).

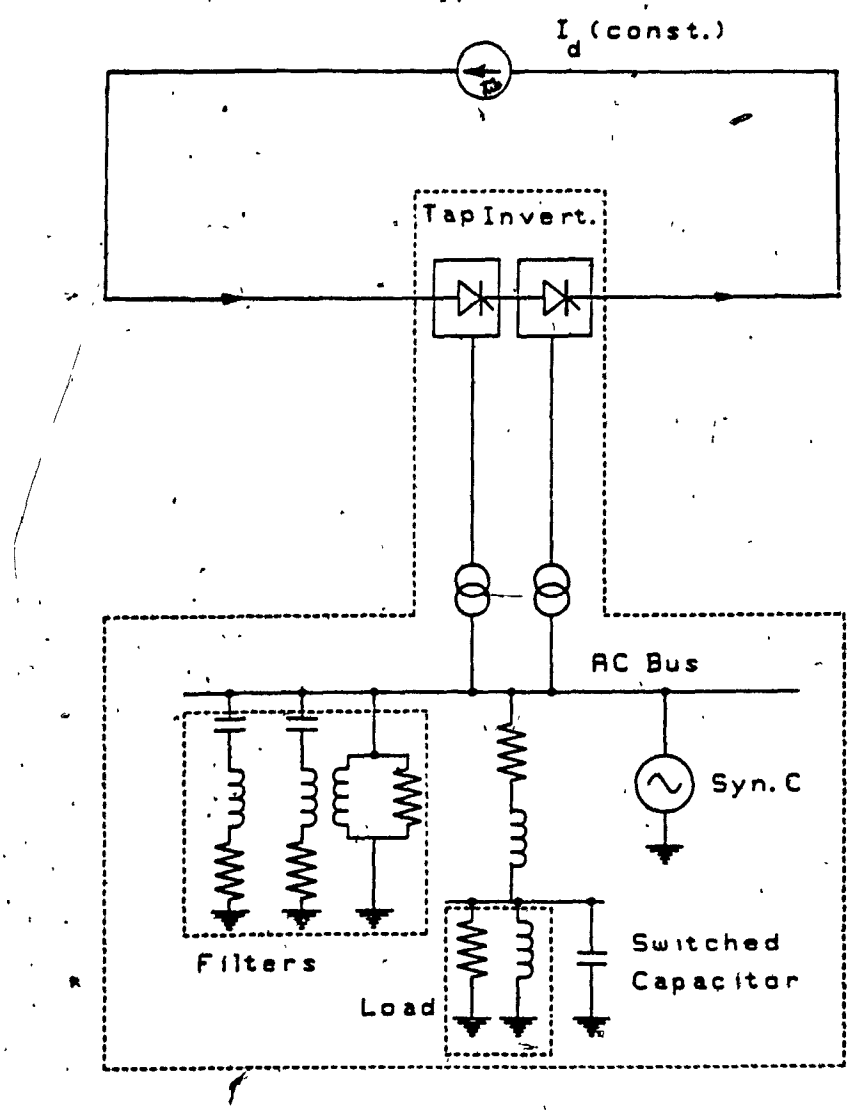

Fig. 4.1 Network for Dynamic Study

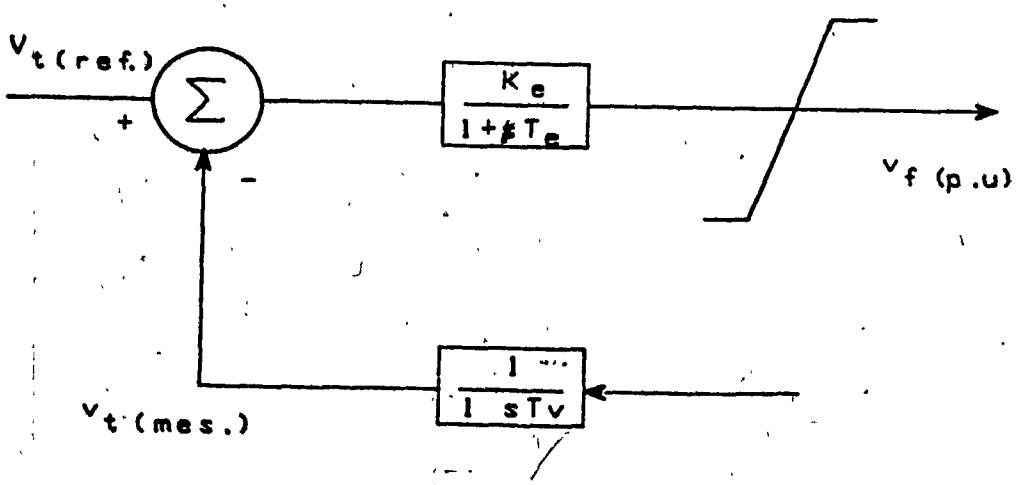

Fig. 4.2 AC Voltage Regulator of the Tap.

The tap's ac bus is connected to the load bus by a short line which is represented by its series impedance. The load is represented by a resistance in parallel with an inductance. The power factor of the circuit is assumed to be .85 lagging as seen from the taps ac bus excluding the power factor correcting capacitors. Details data of the tapping station are given in Appendix-D.

4.3 CONTROLS OF THE TAPPING STATION AND DISTURBANCE ANALYSIS

The voltage at the tap's ac bus i.e, the terminal voltage of the synchronous condenser is to be regulated by the excitation control of the synchronous condenser. A typical static exciter is used. The voltage regulator of the tap is as shown in Fig.4.2. The time constant of the voltage transducer is assumed .01 sec.

The speed of the synchronous condenser will be regulated by controlling the short circuit angle of the tap, with speed deviation as the error signal.

The mechanical power applied to the shaft of the synchronous condenser p_e and its power angle δ should be zero. The short circuit angle should have a specific value at any steady state situation.

Assuming that due to some small disturbance the speed has changed by $\Delta\omega$. The change in short circuit angle, Δd , should finally settle at a constant value (usually non zero) [6]; i.e, the short circuit angle is derived by integrating the speed deviation twice. The following equations can be written.

$$\Delta\dot{\delta} = -2\pi f_s \Delta\omega \quad (\Delta\omega \text{ in per unit}) \tag{4.1.}$$

$$\Delta\dot{d} = K\,\Delta\delta \quad (\text{where, } K \text{ is the gain}) \tag{4.2.}$$

where, ω is in p u. and δ and d are in radians. The dot represents

differentiation with respect to time.

The following equations can be written for the mechanical part of the machine

$$\Delta\dot{\omega} = \frac{\Delta p_e}{M} \qquad (\Delta p_m = 0) \tag{4.3}$$

where, M is the inertia constant and D, the self damping coefficient, is neglected. The power is assumed positive when absorbed by the machine.

For reducing the order of the transfer function the time constant of the voltage transducer is combined with the time constant of the exciter which results in Fig.4.2.

$$\Delta V_f \cong -\frac{K_e \Delta V_t}{\left[1+s(T_e+T_v)\right]}$$

$$\Delta\dot{V}_f = -\frac{\Delta V_f}{(T_e+T_v)} - \frac{K_e \Delta V_t}{(T_e+T_v)} \tag{4.5.}$$

where, V_t and V_f are the terminal and field voltage of the machine respectively (in pu.).

Using a basic machine model (neglecting the dampers and the armature resistance) the following equations can be written (in d-q axes) for the electrical part of the machine [13].

$$\Delta e'_q = \frac{\left\{\Delta V_f + (x_d - x'_d)\Delta i_d\right\}}{(1+sT'_{do})} \tag{4.6.}$$

$$\Delta\dot{e}'_q = \frac{\left\{-\Delta e'_q + \Delta V_f + (x_d - x'_d)\Delta i_d\right\}}{T'_{do}} \tag{4.7.}$$

where, e'_q, x_d, x'_d, i_d and T'_{do} are the internal quadrature axis voltage, the direct axis synchronous reactance, the direct axis transient reactance, the

direct axis current, and the open circuit field time constant of the machine.

The following machine equations will also be needed.

$$p_e = i_d v_d + i_q v_q \tag{4.8.}$$
$$v_d = -x_q i_q \tag{4.9.}$$
$$v_q = e'_q + x'_d i_d \tag{4.10.}$$
$$v_t^2 = v_d^2 + v_q^2 \tag{4.11}$$

where, v_d, v_q, i_q, and x_q are the direct axis voltage, the quadrature axis voltage, the quadrature axis current, the quadrature axis synchronous reactance of the machine. The direction of the machine current is assumed from terminal bus into the machine.

At any operating point the following initial conditions denoted by the additional subscript o may be assumed for the synchronous condenser.

$$v_{to} = 1.0\ pu$$
$$v_{do} = 0.0\ pu$$
$$v_{qo} = 1.0\ pu$$
$$v_{fo} = 1.0\ pu$$
$$i_{qo} = 0.0\ pu$$
$$\omega_o = 1.0\ pu$$
$$\delta_o = 0.0\ pu$$

Using these initial conditions, equations (4.8) through (4.11) can be linearized about any operating point for a small disturbance as,

$$\Delta p_e = i_{do} \Delta v_d + \Delta i_q \tag{4.12.}$$
$$\Delta v_d = -x_q \Delta i_q \tag{4.13.}$$
$$\Delta v_q = \Delta e'_q + x_d \ \Delta i_d \tag{4.14.}$$
$$\Delta v_t = \Delta v_q \tag{4.15.}$$

Putting for Δp_e in Eqn.(4.12) and then substituting for Δv_d from Eqn.(4.13)

$$\Delta \dot{\omega} = \frac{(1 - i_{do} x_q) \Delta i_q}{M} \tag{4.16.}$$

Putting for Δv_t in Eqn.(4.15) and then substituting for Δv_q from Eqn.(4.14) result in

$$\Delta \dot{v}_f = -\frac{\Delta v_f + K_e \Delta e'_q + K_e x'_d \Delta i_d}{(T_e + T_v)} \tag{4.17.}$$

In Fig.4.3, a simplified representation of the tapping station is shown where it is assumed that all harmonic currents produced by the tap are perfectly absorbed by the filters. The current and the voltages are represented by their fundamental components and the filters by their capacitors at fundamental frequency only.

Figs.4.3, and 4.4, illustrate the relationship between the machine current I with the tapping inverter current i_i and the load current i_l.

Fig.4.4, represents the situation in d-q axes after a small disturbance.

The dc power of the tap $= V_d I_d$

$$I_i = \frac{V_d I_D}{V_t}$$

where, V_t is the terminal voltage of the machine (in pu.).

$$V_d = - V_{co} 2\sin(\frac{\pi}{6} - \frac{d}{2}) \tag{4.18}$$

where, $V_{co} = \frac{3}{\pi}\sqrt{2} V_c$ is the rated no load voltage of the tap $= 1.p.u = V_{on}$

$$I_i = \frac{V_d I_d}{V_t}$$

$$= - I_d \left[V_{on} 2\sin(\frac{\pi}{6} - \frac{d}{2}) \right] \tag{4.19}$$

Examining the geometrical relationship of Fig 4.4, the following equations can be written.

$$i_d + i_i \sin(\phi_i + \delta) + i_l \sin(\phi_l + \delta) = 0 \tag{4.20}$$

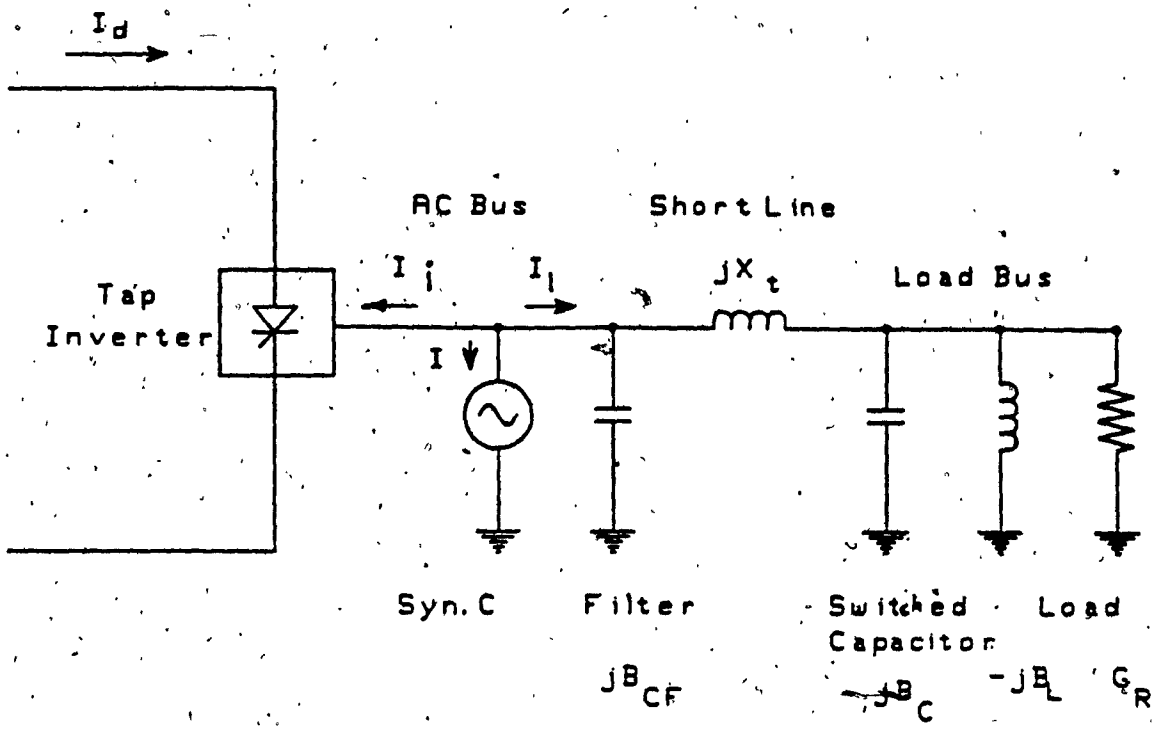

Fig. 4.3 Simplified Representation of the Tap.

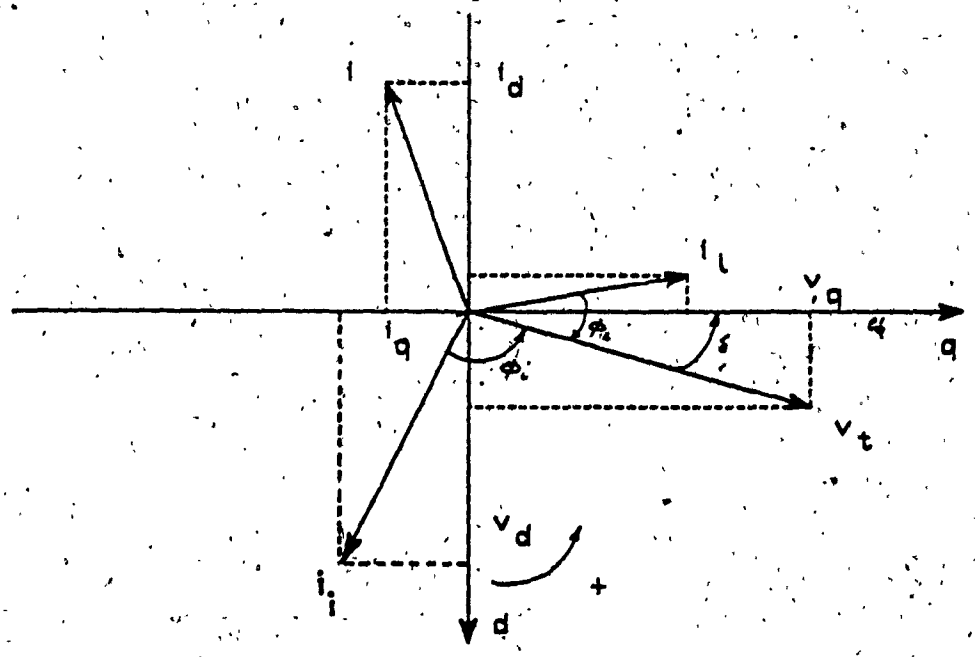

Fig. 4.4 Geometrical Representation.

$$i_q + i_i \cos(\phi_i + \delta) + i_l \cos(\phi_l + \delta) = 0 \tag{4.21}$$

where, ϕ_i, and ϕ_l are the power factor angles of the tap and the load respectively.

$$i_d + i_i \sin(180 + \delta) + i_l \sin(\phi_l + \delta) = 0$$

$$i_d - i_i \sin\delta + i_l \sin(\phi_l + \delta) = 0$$

$$i_d = i_i \sin\delta - i_l \sin\phi_l \cos\delta - i_l \cos\phi l \sin\delta = 0 \tag{4.22}$$

Similarly,

$$i_q = i_i \cos\delta - i_l \cos\phi_l \cos\delta - i_l \cos\phi_l \sin\delta \tag{4.23}$$

$$i_d = i_i \sin\delta + I_{lq} \cos\delta - I_{lp} \sin\delta \tag{4.24}$$

$$i_q = i_i \cos\delta - I_{lp} \cos\delta + I_{lq} \sin\delta \tag{4.25}$$

where,

$$I_{lp} = I_l \cos\phi_l = V_t G(\omega) \tag{4.26}$$

$$I_{lq} = -I_l \sin\phi_l = V_t B(\omega) \tag{4.27}$$

A transfer function of unity is assumed for the tapping converter (assuming that there is no delay).

$G + jB$ is the equivalent admittance of the load, the capacitors and the line as seen from the taps ac bus (Fig.4.3.).

$$G = \frac{G_R B_t^2}{(B_c - B_L - B_t)^2 + G_R^2} \tag{4.29}$$

$$B = B_{CF} - B_t - \frac{(B_c - B_t - B_l) B_t^2}{(B_c - B_t - B_l)^2 + G_R^2} \tag{4.30}$$

In per unit ω.

$$G(\omega) = \frac{G_R \frac{B_t^2}{\omega^2}}{(B_c \omega - \frac{B_L}{\omega} - \frac{B_t}{\omega}) + G_R^2} \tag{4.31.}$$

$$B(\omega) = B_{CF}\omega - \frac{B_t}{\omega} - \frac{(B_c\omega - \frac{B_t}{\omega} - \frac{B_L}{\omega})\frac{B_t^2}{\omega^2}}{(B_c\omega - \frac{B_t}{\omega} - B_L\omega)^2 + G_R^2} \qquad (4.32)$$

The operating point about which the Eqns. (4.19), (4.24), (4.25), (4.26) and (4.27) will be linearized for a small disturbance is assumed to be $P_d = -.8pu$ and $I_d = 1.0pu$

Thus the analysis will be presented for the above mentioned operating point only. This operating point leads to the following initial conditions.

$$I_{do} = 1.0 \ pu$$
$$G_o = .8 \ pu$$
$$B_{CF\,o} = \ pu$$
$$B_{co} = .43 \ pu$$
$$x_{t\,o} = .3 \ pu$$
$$B_{lo} = .311 \ pu$$
$$G_{RO} = .8 \ pu$$
$$B_o = .129 \ pu$$
$$G_o' = \frac{dG(\omega)}{d\omega}\Big|_0 = .317 pu$$
$$B_o' = \frac{dB(\omega)}{d\omega}\Big|_0 = .68 pu$$
$$d_o = 12.843^o \ deg.$$
$$I_{lpo} = .8 \ pu$$
$$I_{lqo} = .12867129 \ pu$$
$$i_{do} = .12867219 \ pu$$

After linearization we get the following equations

$$\Delta i_d = \Delta I_i + \Delta I_{lq}$$
$$\Delta i_q = \Delta I_i - \Delta I_{lp} - \Delta\delta i_{do} \qquad (4.34)$$
$$\Delta I_{lp} = G_o'\Delta\omega + G_o\Delta e_q' + G_o x_d'\Delta i_d \qquad (4.35.)$$
$$\Delta I_{lq} = B_o'\Delta\omega + B_o\Delta e_q' + B_o x_d'\Delta i_d \qquad (4.36.)$$
$$\Delta I_i = I_{do}\left[V_{on}\cos(\frac{\pi}{6} - \frac{d}{2})\right]\Delta d \qquad (4.37)$$

where, the main system is treated as a constant direct current source.

The synchronous condenser used has the following data.

$$x_d = 1 \quad (2)\ pu$$
$$x_q = .92 \quad (1.84)\ pu$$
$$x'_d = .2 \quad (.4)\ pu$$
$$T'_{do} = 11$$
$$M = 2.H = 2.2 = 1.1\ pu$$

H is the inertia constant of the machine.

Substituting Eqns. (4.35), (4.36) and (4.37) in Eqns. (4.33) and (4.34) and solving for Δi_d and Δi_q and then substituting for Δi_d and Δi_q in Eqns. (4.7.), (4.16.) and (4.17.) results in three differential equations in terms of the space variables. These three differentials along with Eqns. (4.1) and (4.2.) are one set of the state space equations of the system which can be written in matrix form as.

$$\dot{x} = Ax \tag{4.38.}$$

$$x = \begin{bmatrix} \delta \\ \omega \\ e'_q \\ V_f \\ d \end{bmatrix} \tag{4.38.}$$

$$\dot{x} = \begin{bmatrix} \dot{\delta} \\ \dot{\omega} \\ \dot{e}'_q \\ \dot{V}_f \\ \dot{d} \end{bmatrix}$$

And

$$A = \begin{bmatrix} 0 & -377 & 0 & 0 & 0 \\ .158 & -.76 & -1.03 & 0 & 1.124 \\ 0 & .114 & -0.78 & .1 & 0 \\ 0 & -477 & -1757.3 & -16.67 & 0 \\ K & 0 & 0 & 0 & 0 \end{bmatrix}$$

From matrix the characteristic equation of the system can be derived as .

$$S^5 + 17.4S^4 + 247.96S^3 + 1071.4S^2 + 10466.47S + 423.748K\,[S^2 + 16.74S + 177.13] \quad (4.40.)$$

As K increases from zero one complex conjugate pair of the roots of the characteristics equation enters the right half of s-plane.

Adding two zeros to the open loop transfer function (i.e proportional signals in parallel with the integrators) may cause a stable situation. These zeros should be close to the $j\omega$ axis. They have been set after several iterations at $S = -1.0$ which results in $T_1 = T_2 = 1\ s$. A pole at $S = -50$ is also added to the open loop transfer function. (i.e $T_\omega = .02s$)

Therefore the poles of the closed loop transfer function are the roots of the following equation.

$$(S+50)(S^5 + 17.4S^4 + 274.96S^3 + 1071.4S^2 + 50*423.748K\,(S+1)^2(S^2 + 16.74S + 177.13) = 0 \quad (4.41.)$$

The root locus plot of Eqn.(4.41) is given in Fig.4.5. Requiring $\rho = \cos\theta \geq .5$ for the dominant complex cojugate roots. The loop sensitivity turns out to be $k \geq .034$. For $k = .034$ the settling time constant of these oscillatory roots is 0.166 s with an oscillation frequency of 1 Hz.

The modified speed regulator of the tap is shown in Fig.4.6.

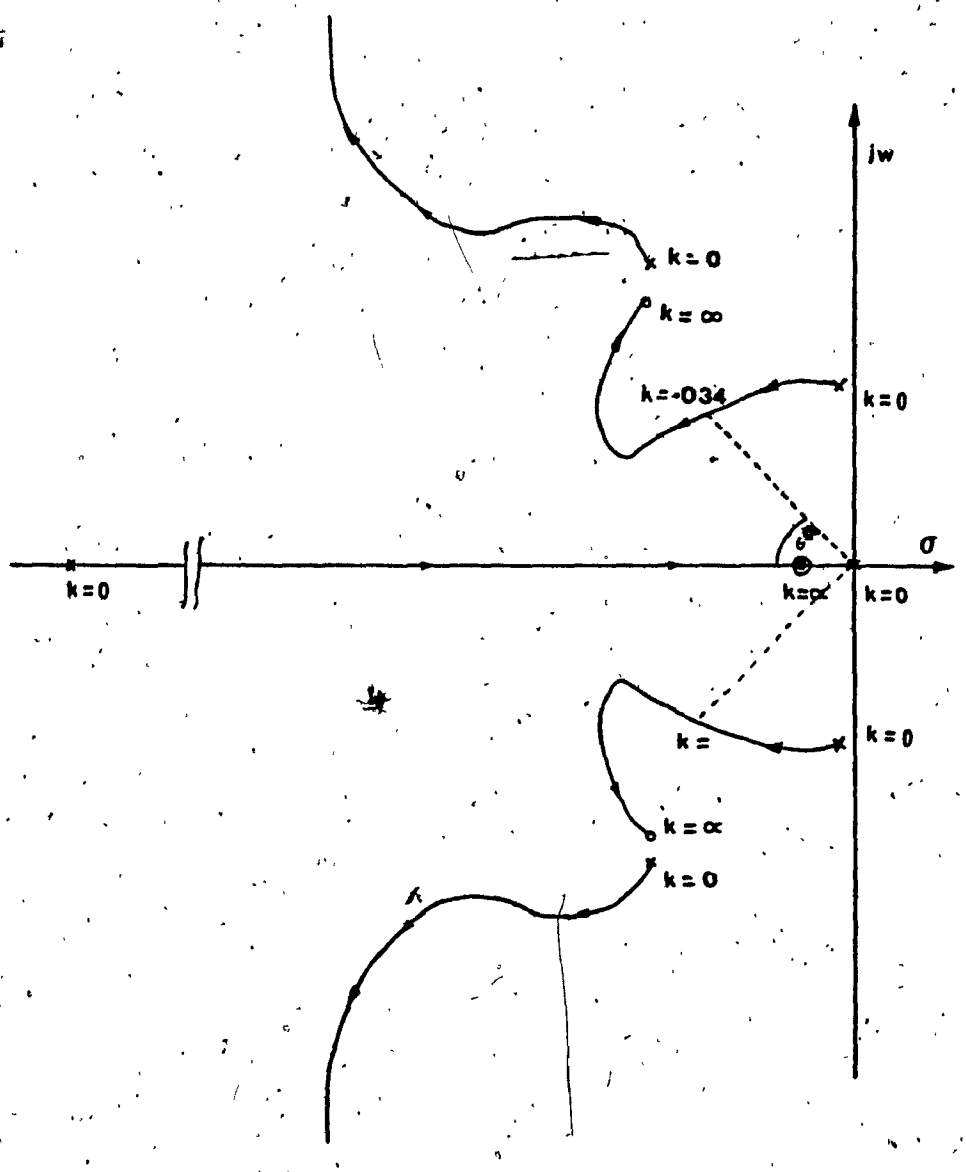

Fig. 4.5 Root locus Plot of the Closed Loop System.

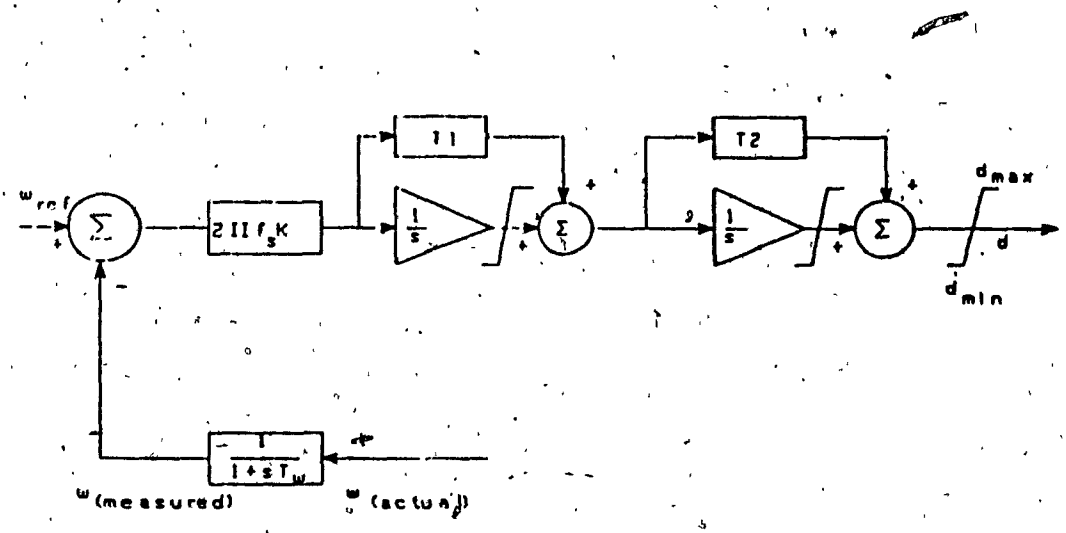

Fig. 4.6 Speed Regulator of the Tap

CHAPTER 5

CONCLUSIONS

5.1 CONCLUSIONS

The objective of this thesis has been to investigate the series tapping of power from a HVDC transmission line. A series tap is compared with a parallel tap. A series tap is more advantageous than a parallel one when the tap is small.

A forced commutated technique for series tapping [9, 10], which is called short circuit method, is analysed. Harmonic analysis of the output ac current and the dc voltage on the input side for the short circuit method is presented. It has been observed that the increase in the amount of overlap decreases the harmonic current magnitudes. These harmonics are found to be greater than that of the line commutated converters. The possibility of harmonic reduction by the application of sinusoidal pulse width modulation (SPWM) and symmetric pulse width modulation techniques with more than two pulses per half cycle is also investgated in detail. The lower order harmonics are seen to be considerably reduced by the application of symmetric pulse width modulation and sinusoidal pulse width modulation techniques which is evident from Figs. 3.12, 3.13, 3.14, 3.16, 3.17, and 3.18.

SPWM technique is more effective in harmonic reduction capability than symmetrical pulse width modulation which is shown in Figs.3.17, and 3.18. Considering the complexity of HVDC application and harmonic reduction capability, sinusoidal pulse width modulation (SPWM) technique with 8-pulse per half cycle is a suitable choice.

In the SPWM scheme the output fundamental current magnitude is less than that could be obtained by the proposed short circuit method. As the output voltage magnitudes are the same in both the schemes, the power output of the SPWM tap will be reduced.

In practical systems with overlap certain amount of reactive power compensation will be necessary in order to control the system voltage. In the proposed short circuit method the inverters do not generate or consume any reactive power, when there is no overlap.

A small disturbance analysis of the system has been carried out and control of the system studied. From the root locus plot of the closed loop system, the loop sensitivity turns out to be $k \geq .034$. For $k = .034$ the settling time constant of the dominant complex conjugate roots is 0.166 s with an oscillation frequency of 1 Hz.

The Short Circuit method has some limitations; i.e, it requires some special start up sequence which makes it complex and expensive. Delays in recovery from a dc line fault may leave the commutation capacitor in a discharged state.

5.2 FURTHER STUDIES

The following work needs to be done for evaluating the series tap in a HVDC line.

1. System studies using either a digital or an analog simulator of a HVDC system incorporating a prototype Short circuit method series tap, and study of the effects of faults on the system.
2. Dynamic study of the system using Static VAr sources (SVS) for reactive power control. Evaluating in terms of merits, demerits and costs.
3. Hybrid converter applications for series tapping, in order to reduce the harmonics and provide voltage regulation.
4. Development of the control strategies for short circuit method series tapping and implementation of these strategies.
5. A typical design and implementation of a prototype experimental setup, to establish the practical limitations of series tap.

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APPENDIX

A. FOURIER ANALYSIS OF TRAPEZOIDAL WAVE

The trapezoidal wave shown in Fig [3.3.] is comprised of three components.

$$f(t) = f_1(t1) + f_2(t) + f_3(t) \tag{A-1}$$

where,

$$f_1(t) = \frac{1}{s}(t - \frac{\pi}{6} - d - s) \ , \ (\frac{\pi}{6} + d) \leq t \leq (\frac{\pi}{6} + d + s) \tag{A-2}$$

$$f_2(t) = 1 \ , \ (\frac{\pi}{6} + d + s) \leq t \leq (\frac{\pi}{6} + d + s + p)$$

$$f_3(t) = [1 - \frac{(t - \frac{\pi}{6} - d - s - p)}{s}] \ , (\frac{\pi}{6} + d + s + p) \leq t \leq (\frac{\pi}{6} + d + 2s + p)$$

The wave shape satisfies quarter wave symmetry. It means $f(t)$ consists of sine terms with odd harmonics only. So the Fourier coefficient

$$A_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f_1(t)\sin nt dt = X + Y + Z \tag{A-3}$$

Where,

$$X = (\frac{4}{\pi}) \int_{\frac{\pi}{6}+d}^{\frac{\pi}{6}+d+s} \frac{1}{s}(t - \frac{\pi}{6} - d - s)\sin nt \ dt \tag{A-4}$$

$$Y = \frac{\pi}{4} \int_{\frac{\pi}{6}+d+s}^{\frac{\pi}{6}+d+s} \sin nt \ dt \tag{A-5}$$

$$Z = \frac{4}{\pi} \int_{\frac{\pi}{6}+d+s+p}^{\frac{\pi}{6}+d+2s+p} [1 - \frac{1}{s}(t - \frac{\pi}{6} - d - s - p)]\sin nt \ dt \tag{A-6}$$

From Eqn.(A-3)

$$= \frac{\pi}{4} \int_{\frac{\pi}{6}+d}^{\frac{\pi}{6}+d+s} \frac{1}{s}(t - \frac{\pi}{6} - d)\sin nt \; dt$$

Integrating and evaluating,

$$X = \frac{4}{\pi}[- \frac{1}{ns}(\frac{\pi}{6}+d+s)\cos n(\frac{\pi}{6}+d+s) + \frac{1}{n^2 s}\sin n(\frac{\pi}{6}+d+s) \quad \text{(A-7)}$$
$$+ \frac{1}{ns}\cos(\frac{\pi}{6}+d) - \frac{1}{n^2 s}\sin n(\frac{\pi}{6}+d)$$
$$+ \frac{1}{ns}(\frac{\pi}{6}+d)\cos n(\frac{\pi}{6}+d+s) - \frac{1}{ns}(\frac{\pi}{6}+d)\cos n(\frac{\pi}{6}+d)]$$

From Eqn.(A-4).

$$= \frac{4}{\pi} \int_{\frac{\pi}{6}+d+s}^{\frac{\pi}{6}+d+s+p} \sin nt \; dt \quad \text{(A-8)}$$

Integrating and evaluating

$$Y = \frac{4}{\pi}[- \frac{1}{n}\cos n(\frac{\pi}{6}+d+s+p) + \frac{1}{n}\cos n(\frac{\pi}{6}+d+s)]$$

From Eqn.(A-5)

$$\frac{4}{\pi} \int_{\frac{\pi}{6}+d+s+p}^{\frac{\pi}{6}+d+2s+p} [1 - \frac{1}{s}(t - \frac{\pi}{6} - d - s - p)]\sin nt \; dt$$

Integrating and evaluating

$$Z = \frac{4}{\pi}[\frac{1}{n}\cos n(\frac{\pi}{6}+d+s+p) + [\frac{1}{n^2}s\sin n(\frac{\pi}{6}+d+s+p) - \sin n(\frac{\pi}{6}+d+2s+p)]]$$

From relation (A-7),(A-8) and (A-9)

$$A_n = X + Y + Z$$

$$A_n = \frac{4}{\pi}[\frac{1}{n^2 s}[\sin n(\frac{\pi}{6}+d+s) - \sin n(\frac{\pi}{6}+d)$$

$$+ \sin n(\frac{\pi}{6}+d+s+p) - \sin n(\frac{\pi}{6}+d+2s+p)]]$$

So the fourier series,

$$f(t) = \sum_{n=1,3,5}^{n=\infty} A_n \sin n\omega t$$

$$f(t) = \sum_{n=1,3,5}^{n=\infty} \frac{4}{\pi}[\frac{1}{n^2 s}[\sin n(\frac{\pi}{6}+d+s) - \sin n(\frac{\pi}{6}+d) + \sin n(\frac{\pi}{6}+d+s+p)$$

$$- \sin n(\frac{\pi}{6}+d+2s+p)]]\sin n\omega t$$

APPENDIX B

B. DETERMINATION OF DC VOLTAGE HARMONICS

The transfer function of a converter S_θ can be expressed in terms of its Fourier series component as:

$$S_i(\theta) = \sum H_n \sin n(\theta+\psi_i)$$

Considering the converter as a set of modulating switches and assuming $S_1(\theta)$, $S_2(\theta)$, $S_3(\theta)$ as the transfer function of the switches with respect to the input port of the converter

Assuming the supply voltage as,

$$V_1 = E\sin(\theta)$$
$$V_2 = E\sin(\theta - 120^0)$$
$$V_3 = E\sin(\theta - 240^0)$$

The output voltage expression becomes

$$V_0(\theta) = \sum V_i(\theta) S_i(\theta)$$
$$V_0(\theta) = F_1(\theta) + F_2(\theta) + F_3(\theta)$$

where,

$$F_1(\theta) = S_1(\theta) E\sin\theta$$
$$F_2(\theta) = S_2(\theta) E\sin(\theta - 120^0)$$
$$F_3(\theta) = S_3(\theta) E\sin(\theta - 240^0)$$

Using respective Fourier series for the terms for the function, $F_1(\theta)$, $F_2(\theta)$, and $F_3(\theta)$, can be expressed as.

$$F_1(\theta) = E\sin\theta \sum_{n=1}^{n=\infty} H_n \sin(n\theta) \qquad \text{(B.4)}$$

$$F_2(\theta) = E\sin(\theta - 120^0) \sum_{n=1}^{n=\infty} H_n \sin(n\theta - n*120^0) \qquad \text{(B-5)}$$

$$F_3(\theta) = E\sin(\theta - 240^0) \sum_{n=1}^{n=\infty} H_n \sin(n\theta - n*240^0) \qquad \text{(B-6)}$$

The output voltage components can be rewritten by using simple trigonometrical identity.

$$F_1(\theta) = \sum_{n=1}^{n=\infty} \frac{EH_n}{2}[\cos(n-1)\theta - \cos(n+1)\theta] \quad \text{(B-7)}$$

$$F_2(\theta) = \sum_{n=1}^{n=\infty} \frac{EH_n}{2}[\cos((n-1)\theta-(n-1)*120^o) - \cos((n+1)\theta - (n+1)*120^o)] \quad \text{(B-8)}$$

$$F_3(\theta) = \sum_{n=1}^{n=\infty} E\frac{H_n}{2}[\cos((n-1)\theta - (n-1)*240^o) - \cos((n+1)\theta - (n+1)*240^o)] \quad \text{(B-9)}$$

Using Eqns.(B-7), (B-8), (B-9) for $n=1$

$$\textit{Output dc voltage } V_{dc} = \frac{3}{2}EH_1$$

Substituting n=1, 2, 3, 4 in the Eqns.(B-7), (B-8), (B-9)

First harmonic component. $V_{o1} = 0$

2nd harmonic component

$$V_{o2} = E\frac{H_3}{2}\cos2\theta - \frac{EH_1}{2}\cos2\theta + \frac{EH_3}{2}\cos(2\theta-2*120^o) - E\frac{H_1}{2}\cos(2\theta - 2*120^o) + E\frac{H_3}{2}\cos(2\theta - 2*240^o) - E\frac{H_1}{2}\cos(2\theta - 2*240^o)$$

3rd harmonic component

$$V_{o3} = \frac{EH_4}{2}\cos3\theta - E\frac{H_2}{2}\cos(3\theta) + E\frac{H_4}{2}\cos(3\theta - 3*120^o) - E\frac{H_2}{2}\cos(3\theta - 3*120^o) + E\frac{H_4}{2}\cos(3\theta - 3*240^o) - E\frac{H_2}{2}\cos(3\theta - 3*240^o)$$

Similarly the m^{th} harmonic component of the output voltage can be expressed as

$$V_{om} = E\frac{H_{m+1}}{2}\cos m\,\theta - E\frac{H_{m-1}}{2}\cos m\,\theta \qquad \text{(B-11)}$$

$$+ E\frac{H_{m+1}}{2}Cos\,(m\,\theta - m*120^{o}) - E\frac{H_{m-1}}{2}\cos(m\,\theta - m*120^{o})$$

$$+ E\frac{H_{m+1}}{2}\cos(m\,\theta - m*240^{o}) - E\frac{H_{m-1}}{2}\cos(m\,\theta - m*240^{o})$$

APPENDIX

C. AC FILTERS WITH SHORT CIRCUIT METHOD

The cost of a filter tuned for a particular harmonic varies as [1]

$$K = AS + BS^{-1} \tag{C-1}$$

where,

$K = Cost\ (\$)$
$S = Size\ (MVAr)$
$A = Constant\ (\$/MVAr)$
$B = Constant\ (\$/MVAr)$

Neglecting the total cost of the resistor the total cost of the filter is

$$K = P_{rc} + P_{rl} \tag{C-2}$$

where,

$U_c = Unit\ cost\ of\ Capacitor\ (\$/MVAr)$
$U_l = Unit\ cost\ of\ Inductor\ (\$/MVAr)$

The above constants can be derived as

$$A = U_c + \frac{U_l}{n^2} \tag{C-3}$$

$$B = \frac{V_1^2 I_{hf}^2 (U_c + U_l)}{n} = \frac{2.8 V_1^2 I_{hf}^2 U_c}{n}$$

where,

$V_1 = Fundamental\ Voltage\ (kV/Phase)$
$I_{nf} = nth\ harmonic\ current\ through\ the\ filter.$

The size for minimum cost is found by equating the derivative $\frac{dK}{dS}$ to zero.

$$\frac{dk}{dS} = A - BS^2 = 0$$

Whence, $S_{(min)} = (\frac{B}{A})^{\frac{1}{2}}$ and substitution of this value of S into the

equation for cost gives the minimum cost as,

$$K_{\min} = 2\sqrt{AB} \tag{C-7}$$

Assuming,

$$\Phi_m = \textit{Maximum Network Impedence Angle} = 75^0$$
$$\delta_m = \textit{Maximum perunit deviation of frequency from tuned frequency} = .02$$

The optimum quality factor of the filter [1] $Q = \frac{.65}{\delta_m} = 32.5$ and the nth ac harmonic voltage in per unit of fundamental voltage is

$$V_{(n)} = 3.17\delta_m (n^2+2)^{\frac{1}{2}} \frac{\cos(\frac{\Phi_m}{2})}{(3n^3)^{\frac{1}{2}}}$$

Thus,

$$V_{(11)} = 0.88\% < 1.0\%$$
$$V_{(13)} = 0.809\% < 1.0\%$$

As the voltage is less than one percent there is no need to increase the size of the tuned filter beyond $S_{\min}$.

For the series tap in dynamic studies.

$$V_{(1)} = 9.815\ kV$$
$$I_{(1)} = 1.698\ kA$$
$$I_{(11)F} = (\frac{.2}{1.1}) * 1.698\sec(\frac{\Phi_m}{2}) = .389\ kA$$
$$I_{(13)F} = (\frac{.17}{1.1}) * 1.698\sec(\frac{\Phi_m}{2}) = .3306\ kA$$

$(\frac{.2}{1.1})$ and $(\frac{.17}{1.1})$ are the maximum per unit 11th and 13th harmonic current of the tap.

$$S_{(11)} = 1.912\ MVAr/phase \cong 12\%$$
$$C_{(11)} = \frac{S_{(11)}}{(\omega V_1^2)} = 52.64 * 10^{-6}\ F$$

$$L_{(11)} = \frac{1}{C_{(11)}\omega^2 n^2} = 1.104\ mH$$

$$R_{(11)} = \frac{X_o}{Q_o} = \frac{1}{Q_o}\left(\frac{L}{C}\right)^{\frac{1}{2}} = .1409\ ohm$$

$$Loss_{(11)} = (\omega C_{(11)} V_{(1)})^2 R_{(11)} = 5.345 kW/phase$$

$$S_{(13)} = 1.4979\ MVAR \cong 9\%$$

$$C_{(13)} = \frac{S_{(13)}}{(\omega V_1^2)} = 41.24 * 10^{-6}\ F$$

$$L_{(13)} = \frac{1}{C_{(11)}\omega^2 n^2} = 1.0\ mH$$

$$R_{(13)} = \frac{X_o}{Q_o} = \frac{1}{Q_o}\frac{L}{C}^{\frac{1}{2}} = .152\ ohm$$

$$Loss_{(13)} = (\omega C_{(13)} V_{(1)})^2 R_{(13)} = 3.539\ kW/phase.$$

For decreasing the arithmetic sum of the voltage harmonics up to the 25th inclusive to 2.5% the arithmetic sum of the 23rd and and 25th should be [1],

$$2.5 - (.88 + .809) = .82\%$$

The arithmetic sum of the 23rd and 25th harmonic current through the high pass filter is,

$$I_{(H.P)} = \left(\frac{.1}{1.1} + \frac{.09}{1.1}\right) I_{(1)} \sec\left(\frac{\Phi}{2}\right) = .3695\ kA$$

The magnitude of the impedance of the high pass filter at the resonance frequency (i.e at n=24) is,

$$Z = \frac{R_{(H.P)}}{[Q(Q+1)^2]}$$

where,

$$Q = \omega n R_{(H.P)} C_{(H.P)}$$

Assuming that the total reactive power supplied by the filters should be 24% of the real power of the tap.

$$S_{(H.P)} = (4 - 3.409) = .5901\ MVAr\ /Phase.$$

$$C_{(H.P)} = \frac{S_{(H.P)}}{\omega(V_1)^2} = 16.248\ uF$$

$$L_{(H.P)} = .75\ mH$$

$$R = 6.625 ohms.$$

D. DATA OF TAPPING STATION

TAPPING STATION

Ratings : 25 kV/pole = 1.0 pu

2000 A = 1.0 p.u

50 MW/pole = 1.0 pu

FILTER OF TAPPING STATION

AC High pass Filter : 16.248 uF, .75 mH, 6.625 ohms

AC 11th tuned Filter : 52.64 uF, 1.104 mH, .1409 ohms.

AC 13th tuned Filter : 41.24 uF, 1.00 mH, .152 ohms

CONVERTER TRANSFORMERS

Three phase MVA = 29.18

AC side voltage kV = 17.0 (LL) kV = 1.0 pu

Valve side = 10.316 (LL) kV

SYNCHRONOUS CONDENSER

MVA = 25 kV = 17.0 $f_b = 60H$

$x_o = .015$

$x'_d = .2$

$x_q = .92$

$T'_{do} = 11s$

$x_d = 1$

$x'_d = .12$

$H = 1.1 M.W.s/MVA$

SPEED REGULATOR

$K = .09$

$T_1 = T_2 = 1\ s$

$T_\omega = .02\ s$

VOLTAGE REGULATOR

$K_e = 100$

$T_e = .05s$

$T_v = .01s$

SHORT AC LINE

$R_t = .1 ohm\ ,\ L_t = 2.3\ mH$

SWITCHABLE CAPACITOR

$C = 200\ uF \cong 0.44 pu$