ACKNOWLEDGEMENT

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V. ANANDU

TABLE OF CONTENTS

CHAPTER I

INTRODUCTION

One of the most interesting and fascinating devices which are discussed and coming up in recent years is charge coupled devices. In the case of charge coupled device, the signal can be injected to the device either electrically or optically. The signal is injected in the form of an electrical charge rather than electrical voltage or Current. The charge injected at one end can be clocked from electrode to electrode, so that an output is formed after a delay. Therefore one of the most powerful applications of a charge coupled device is as a delay line. Further signals can be processed in the analog form. This eliminates A/D Conversion in signal processing applications. The charge coupled devices are simple to manufacture, consumes less power, has high reliability and has essentially a low-noise figure.

It was in 1970, that Boyle and Smith[1] of Bell Laboratories demonstrated the principle of a charge coupled device. It was shown that by clocking the gate voltage of a metal oxide semi conductor, the electrical charge injected under the first electrode could be moved from electrode to electrode. Therefore one of the applications of a charge coupled device is as a shift register., Amelio[2], who first experimented this

charge coupled device convinced the engineers and scientists all over the world of the reliability of Boyle and Smith principle.

The concept of a charge coupled device was well received by engineers and scientists. By 1972, large scaled integrated circuits were built and were used as imaging devices in Television systems.

As the signal charge introduced at the first electrode could be transferred from electrode to electrode by means of the clocking pulses, one of the powerful applications of the charge coupled device, is as a delay line; used in Transversal filtering. The CCD Transversal filters offers cost advantage, size, weight and simpler manufacturing process. The signals could be processed without any A/D conversion.

In Chapter 2 of this report, the principle, input/output circuits, weighting and frequency of a charge coupled device are described. Transversal filter principle as envisaged by Kallmann is also described[3]. In chapter 3, two methods of implementing the charge coupled device transversal filters are described. Performance of a low-pass filter implemented using the two techniques are given. The transversal filters were implemented using linear phase design. Linear phase filters have constant time delay over the entire filter frequency band. This is very useful in data communication. However, the

long time delays are undesirable in voice communication, as their long time delays are likely to introduce echo and singing on voice channels. Further the group delay increases, as the number of stages are increased in a transversal filter. In order to decrease the group delay for voice communication purposes, the CCD transversal filter can be designed with a minimum-phase. Therefore a minimum phase CCD transversal filter is described and the advantages of a minimum phase filter compared to a linear phase filter are given with the help of a 32 tap low-pass CCD transversal filter.

Any input frequency f_i close to the clock frequency f_o gives rise to $(f_o + f_i)$ and $(f_o - f_i)$ due to aliasing. In this case if the CCD transversal filter designed is a low pass filter, then the spurious component $(f_o - f_i)$ may fall within the pass band of the filter. As a result, if this spurious frequency component is not removed, it may also appear in the output. In order to eliminate these spurious frequencies from the output, the band width of the input signal is limited by a prefilter, which rejects all frequencies above $(f_o - f_i)$. The prefilter can be implimented by an RC network. In this case the prefilter implementation offsets the cost advantage of a CCD transversal filter. The prefilter is implemented as a transversal filter of only few taps and is included on the main chip of the CCD transversal filter. Therefore the

prefiltering requirements of a CCD transversal filter are also given. There is no doubt whatsoever that much work appears to be done in these two fields.

In the chapter 4, errors and cures in implementing CCD transversal filters are covered. Choice of clock frequency number of taps, chip size and tap weight tolerance are highlighted with examples wherever possible. Experimental results conducted on two low-pass CCD transversal filters are also included.

During the charge transfer from electrode to electrode in a charge coupled device, some charge is invariably left behind at each transfer. Therefore there is a loss in charge transfer from electrode to electrode. Transfer efficiency, which is the fraction of the charge packet correctly transferred per stage. This is usually in the range of 99,9 to 99.99% for a three phase device. Therefore it is rather convenient to define a term called transfer inefficiency. The transfer inefficiency is cumulative, as a large number of electrodes are used. The effect of imperfect charge transfer put a limit on the performance of a CCD transversal filter. Therefore in the chapter 5, limitations of CCD transversal filter are covered.

CHAPTER II

BASIC PRINCIPLES OF CCD AND TRANSVERSAL FILTER

2-1 Principle Of Transversal Filter

Passive filters constructed using inductances and capacitors produce phase distortion. Hence these filters can be used, where phase distortion can be tolerated. However, in certain cases, phase distortion has to be avoided throughout the range of the filter.

The transversal filters described in here show no phase distortion at all or a phase distortion which varies slowly and steadily irrespective of the amplitude response. As such the error introduced due to phase distortion can easily be corrected. Transversal filters are constructed from pieces of cable, contrary to RLC filters. The input impedance of the transversal filter is matched to the impedance of the generator and the output impedance is terminated with a proper resistance. The cable is tapped at different points equidistant from the centre. The tapped outputs are added by a summing amplifier.

Consider a lossless cable of impedance Z, which is matched to a generator 'G' at one end and terminated with a resistance 'R' at the other end. The lossless cable is shown in Fig.2.1. The cable is tapped at two points A and B, such that an electric wave takes a time 'T' to travel from A to B. The tapped points are connected to an voltmeter as shown in

Fig. 2.1 in order to measure the difference in voltage between A and B. The voltmeter has an infinite input impedance, so that even small differences in voltage between the points A and B can be measured. Sine waves at different frequencies were fed from the generator 'G' to the cable and the difference in voltage between the tapped points A and B were observed on the voltmeter. At frequencies, wherein 'f' was equal to 1/T; 2/T; 3/T; etc, the observed difference in voltage was zero. But at other intervals, a voltage difference was observed. Assuming Eo to be the voltage applied by the generator and 'E' to be the difference in voltage between the tapped points A and B,

$$E = 2Eo \sin \pi fT. \qquad \ldots\ldots\ldots (2\text{-}1)$$

At frequencies $f = 1/T$,

$$E = 2Eo \sin \pi = 0 \quad \text{as } \sin \pi = 0$$

But at frequencies $f = \frac{1}{2T}$;

$$E = 2Eo \sin \pi \frac{1}{2T} T = 2E_o \sin \frac{\pi}{2}$$

$$= 2E_0 \quad \text{as } \sin \frac{\pi}{2} = 1$$

In other words the tapped points A and B reproduce the amplitude response of a Sine wave, without introducing any phase error. The amplitude response of the tapped points A and B are shown in Fig.2.2. The response is of sinusoidal shape and continues to oscillate unattenuated. The function

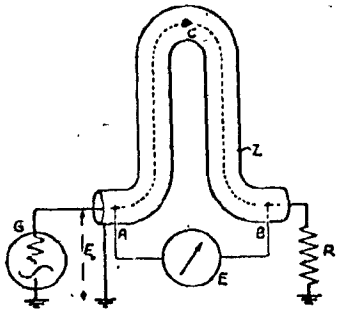


Figure 2.1 Showing a lossless cable.
(Courtesy:Reference 3)

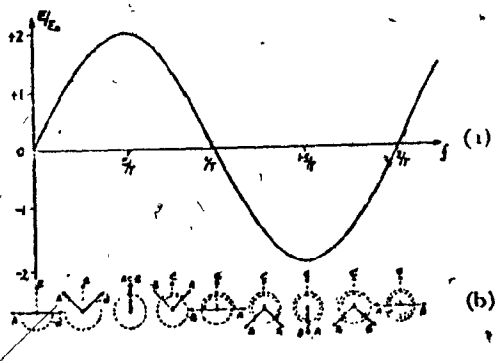


Figure 2.2 Showing the amplitude response of a sine wave.
(Courtesy:Reference 3)

is periodic and the voltage E assumes alternatively positive and negative values. In other words, the magnitude of the response varies continuously and periodically reverses in polarity.

Assuming the centre point of the cable 'C' as reference phase, the resultant victor 'E' which is the sum of A and B, has the same phase as 'C' vector at f = 0.5/T; 2.5/T; etc. But at f = $\frac{1.5}{T}$; $\frac{3.5}{T}$; etc, the resultant vector 'E' has opposite phase.

Figure 2.3. shows the phase angle 'Q' between E and C is plotted against frequency 'f'.

The phase angle 'Q' lags $\pi/2$ for zero frequency and the phase linearly rises with frequency. The phase lag can be ignored when 'f' is very large. But if 'f' is small, $\Delta f/f$, becomes considerable. Hence at low frequencies, phase correcting circuits are required in order to provide slow but steady phase change.

This can be offset, if the circuit in Fig.2.1 modified so that instead of the difference in the potential between the points A and B, their sum is used. The sum of the voltages between the points A and B, will result in an amplitude response of $E = 2Eo \cos \pi fT$.

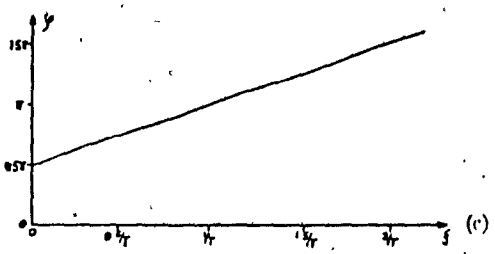


Figure 2.3 Phase angle plotted against frequency. (Courtesy:Reference 3)

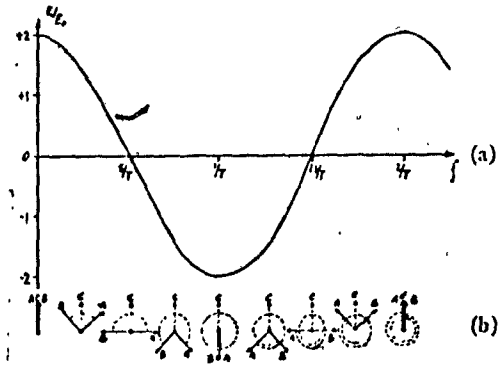


Figure 2.4 Cosine response of the filter. (Courtesy:Reference 3)

This amplitude response is shown in Fig.2.4.

Now $E = 2Eo \cos \pi fT$ ..... (2-2)

At $f = 0.5/T$;

$$E = 2Eo \cos \pi \frac{0.5}{T} T$$

$$= 2E_o \cos \frac{\pi}{2} = 0 \text{ as } \cos \frac{\pi}{2} = 0.$$

This means, that at frequencies, $f = \frac{0.5}{T}; \frac{1.5}{T}; \frac{2.5}{T}$ etc., the sum of the voltages E is zero.

At $f = 0, 1/T$;

$$E = 2Eo \cos \pi fT$$

$$= 2Eo \quad \because \cos 0 = 1$$

Hence at frequencies $f = 0, 1/T; 2/T;$ etc. the sum of the voltage is maximum.

The phase angle 'Q' between E and C plotted against frequency is shown in Fig. 2.5. The initial lag in zero, but the phase angle 'Q' increases linearly with frequency.

It is clear, that in both of the above cases of Sine and Cosine waves, the amplitude response varies inversely as the delay between the points A and B. This concept can be extended to a number of cable pieces. This has been shown in Fig.2.6

In Fig. 2.6, the cable is tapped at different points

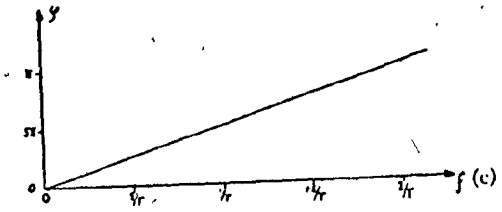


Figure 2.5 Phase angle versus frequency.
(Courtesy:Reference 3)

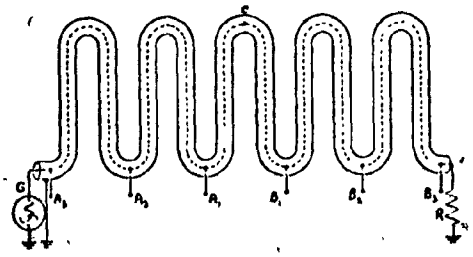


Figure 2.6 Multisection filters.
(Courtesy:Reference 3)

A_1, A_2 ..... An and B_1, B_2 ..... Bn, so that A_1 B_1, A_2 B_2..... AnBn are equidistant from the center 'C', the reference point. This means that all the tappings are equidistant from the center. In other words, each tap effectively multiplies the amplitudes by either + 1 or by -1.

Hence by using a combination of pairs of tappings, any desired amplitude response and phase characteristics can be realized. Therefore a transversal filter consists of a pieces of cable, capable of reproducing any amplitude response, without introducing phase distortion. This is the basic concept of a transversal filter as envisaged by H.E. Kalmann in his original paper.(3)

This basic concept of delaying the input signal and sampling can best be achieved by using charge-coupled devices. In charge coupled devices, the information is stored as an electric charge and not as an current or voltage in conventional circuits. A charge-coupled device is basically a shift register, wherein the signal charge is shifted from electrode to electrode by means of clock pulses. A unique feature of the device is that the signal can be injected either electrically or optically. In order to perform transversal filtering with a charge-coupled device, it is required to nondestructively sample the analog signal as it shifts from electrode to electrode. Therefore in the following chapters, the basic principle

of a CCD, CCD transversal filters, its implementation and its limitations for analog signal processing are fully covered.

2.2. Principle of a Charge-Coupled device

A metal-oxide semi conductor cell is shown in Fig. 2.7. The metal electrode is made of Aluminum. The substrate is silicon, which can be either P-type or N-type semi Conductor. In the Fig. 2.7, P-type semiconductor is used. In P-type semiconductors, electrons are the minority carriers and holes being majority carriers.

When a positive voltage is applied to the silicon electrode, holes are repelled back from the electrode. Thus the area under the electrode become depleted of the holes or forms a potential well to store electrons Hence the extent of the depletion region is a function of gate voltage. Information can be stored in the depletion region in the form of minority carriers.

Consider four closely spaced metal electrodes as shown in Fig. 2.8.[1,4] . Initially the electrodes 1, 3, and 4 are biased with 2 volts, whereas the bias on the electrode 2, is kept at 10 volts. The bias of 2 volts is assumed to be sufficient in order to maintain depletion, under all of the electrodes. The charge is assumed to be stored under the electrode 2. Now increasing the bias Voltage on the electrode

3 to 10 volts, makes the potential on the electrodes 2 and 3 to be the same. As a result, the depletion layers of electrodes 2 and 3, will merge, as shown in Fig. 2.9. Now reducing the voltage, on electrode 2 to 2 volts, the charge which was assumed to be under electrode 2, will not shift to electrode 3. This is shown in Fig.2.10. In other words, moving the bias voltage from electrode to electrode, the charge packet can be made to propogate beneath the surface of the semiconductor. This is the basic principle of a charge coupled device.

The bias voltage on the electrode can be made to move by means of a clock mechanism. This is because, the bias voltage on the electrodes has to be changed in a time shorter than the storage time, say 't'. The storage time 't_s' is given by

$$t_s = \frac{Q}{I_d}, \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2\text{-}3)$$

when Q = Charge density,

I_d = Thermally generated Current.

Generally, the storage time is of the order of seconds. The magnitude of the charge that can be stored under a given electrode depends on the size and the bias voltage of the electrode.

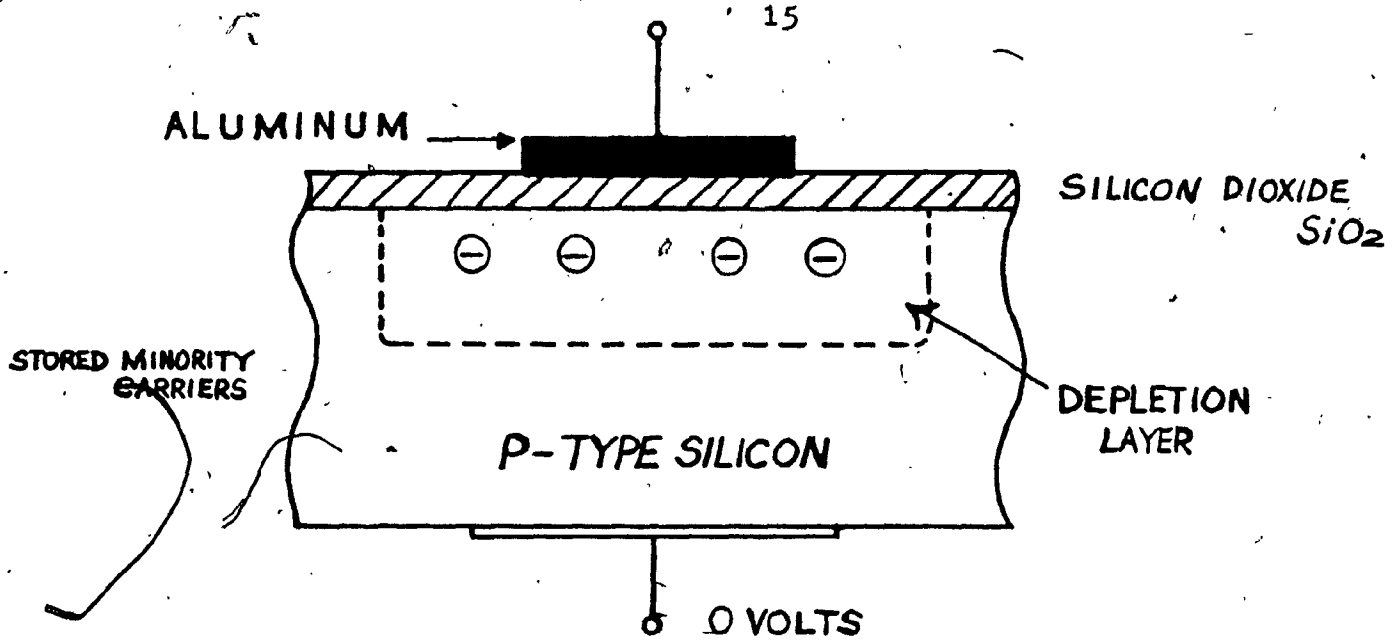


Figure 2.7

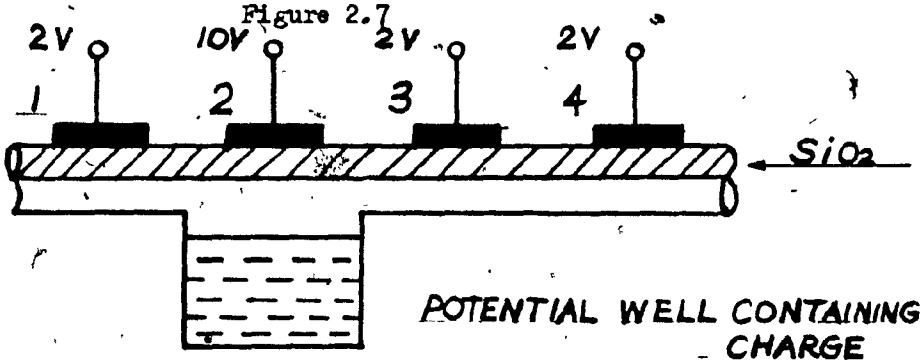


Figure 2.8

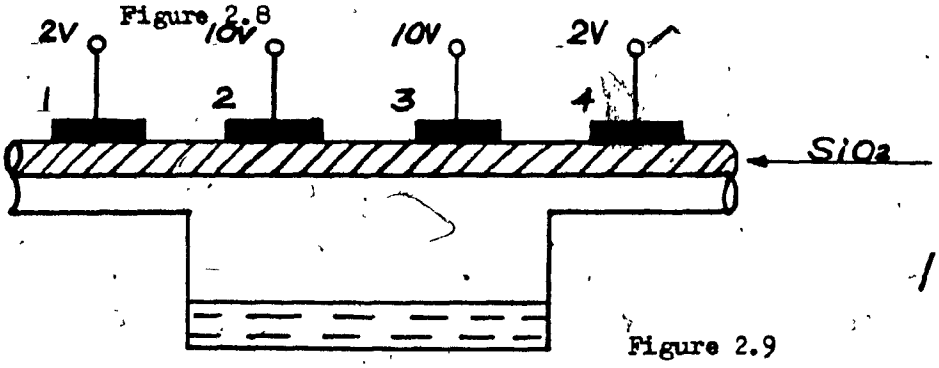


Figure 2.9

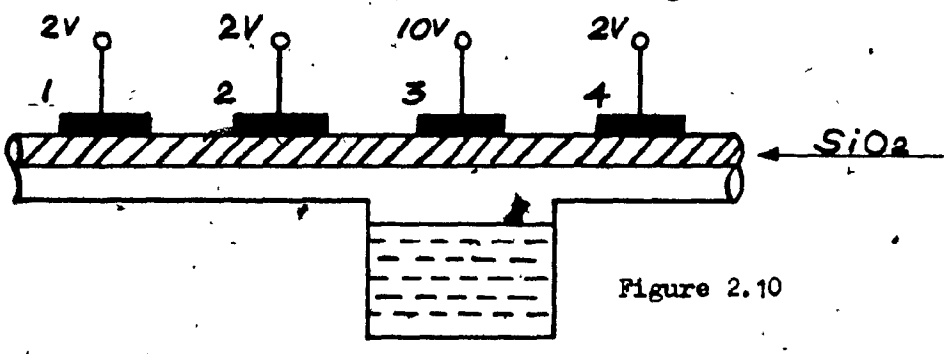


Figure 2.10

The potential wells are used to store and transfer minority carriers, also repels majority carriers. The minority carriers for example, can be analog signals. As a result of interaction, a minority carriers are lost from the original charge packet and are left behind at each transfer. In most of the applications of CCD's require more than 1000 transfers. Therefore the charge left behind namely 'ε' has to be extremely small, in order to avoid signal degradation. Generally speaking, 'ε' is in the range of 10^{-4} to 10^{-5}. In order to accomplish this, no potential barrier should exist between any two potential wells, so that all the charge can be transferred.[5] When a barrier does exists, a small amount of charge is left behind as already stated. In this case the barrier height shown in Fig.2.11 determines the amount of charge transferred at low frequencies.

The barrier height is determined by the amount of charge in the receiving well. Large signals results in charge repulsion and so increases the barrier height. This results in less charge being transferred for large charge packets than for small charge packets. This barrier height results in a transfer loss of 10^{-3} at gate lengths of 10μm. The transfer loss increases, as gate length increases. Therefore whenever higher transfer efficiencies are required, the potential barriers are to be avoided. Suppose, even if this is accomplished, the transfer efficiency is limited by fat zeros caused

by trapping effects. The fat zero is only effective in the deepest parts of the potential wells but not the edges. This is shown in Fig. 2.12. This trapping effect is severe with surface channle CCD (SCCD) than barried channel CCD. It will not be out of the place to mention, that in the SCCD, the Mos Capacitor has a uniform doped substrate. In the case of buried channel CCD, the Mos capacitor has a substrate with a thin depleted layer of opposite conductivity at the surface. In the case of surface channel CCD, the potential minimum for the minority carriers is at the interface of si/sio_2. The potential minimum can be moved away from the surface to a point within the impurity. This can be accomplished by doping the surface with opposite polarity than the substrate. This means that for a p-type substrate, an n-type layer is made use of. This is the basic concept of a buried-channel CCD.[6] The SCCD and BCCD are shown in Fig. 2.13 and 2.14 respectively. The BCCD prevents contact of the signal with the interface and as such eliminates surface state trapping on account of this transfer inefficiencies of the order of 10^{-4} to 10^{-5} can easily be accomplished.

2-3. Charge Injection

Two methods of charge injection are described[7] namely:

(a) Linear current method

(b) Measured charge method.

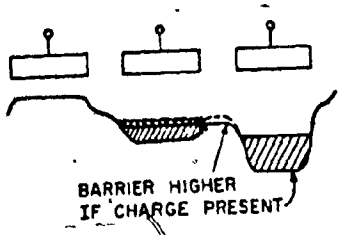


Figure 2.11 Showing barrier height in charge coupled devices. (Courtesy:Reference 5)

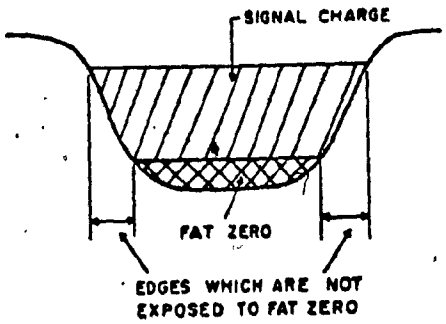


Figure 2.12 Shows the effects of fat-zero charge on potential wells.(Courtesy:Reference 5)

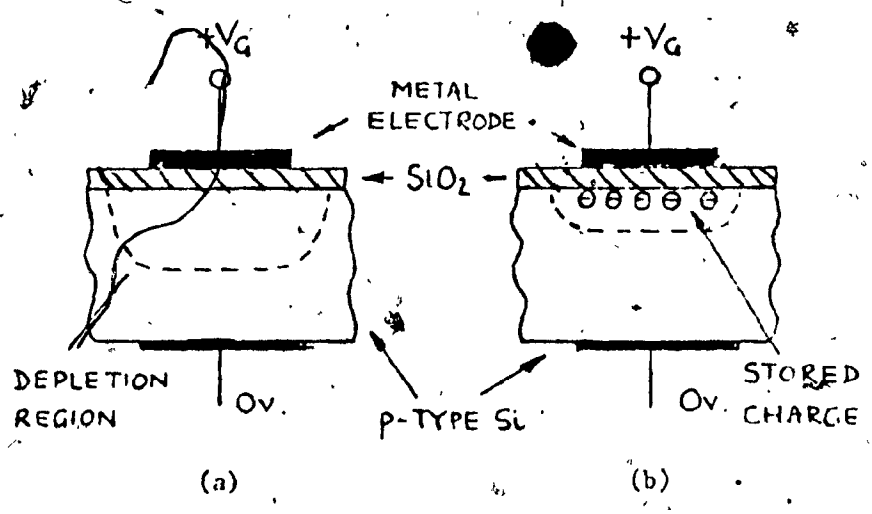


Figure 2.13 Surface channel charge coupled device.
(Courtesy: Reference 6)

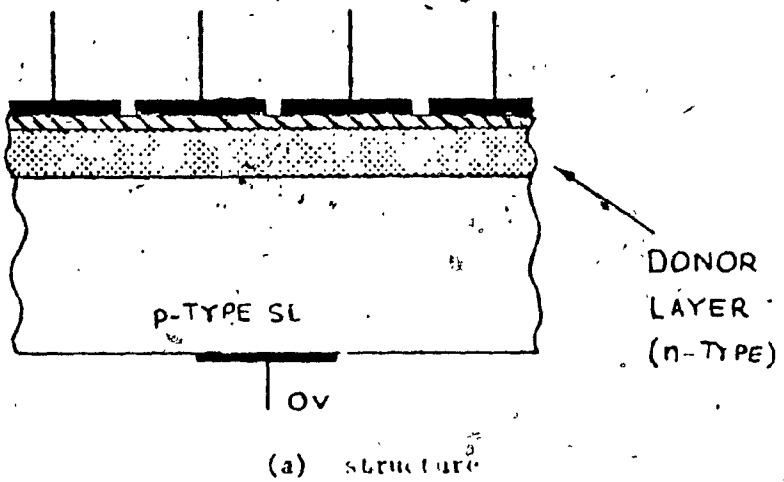


Figure 2.14 Burried channel charge coupled device.
(Courtesy: Reference 6)

Figure 2.15 shows the basic circuit required to inject a charge linearly to a CCD element. The circuit consists of an input diode - input gate and a first stage of a CCD. The first stage of the CCD is a low-input bias current amplifier and one resistor. This is similar to a current regulator and so produces a constant current at the input of the CCD.

Assuming the input V_{in} to be positive signal voltage, causes the output of the amplifier to swing negative and this negative voltage is applied to the input gate of the CCD. This in turn causes the input FET to be turned on and allows current flow to the CCD. The current injected into the CCD is proportional to the input signal and hence can be expressed as

$$i_{injected} = \frac{V_{in}}{R} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2\text{-}4)$$

Therefore the charge injected to the CCD is given by

$$Q = \int \frac{V_{in}}{R}\, dt \quad \ldots\ldots\ldots\ldots \quad (2\text{-}5).$$

The magnitude of the current injected is very small and is of the order of nanoamperes. Therefore care must be taken to see that all the signal current enters the first stage of the CCD, without any loss. The P^+ diffusion shown in Fig. 2.16 forms a junction diode with the substrate. If a bias voltage is present across this junction, a current will

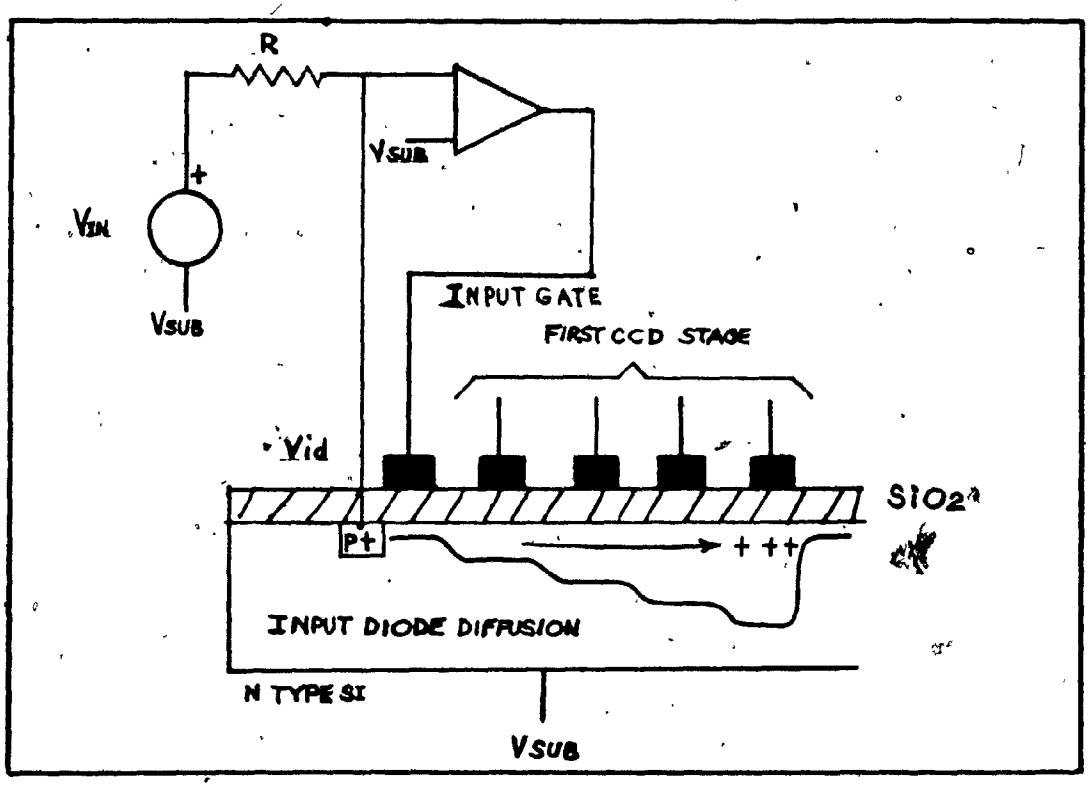


Figure 2.15 Linear current method of injecting the input.
(Courtesy: Reference 7)

flow. This current will add or subtract from the current injected into the CCD. This is likely to cause an error. But this circuit eliminates this error, as the bias voltage across the junction is zero. The circuit also has enough compensation for threshold voltage, oxide thickness and needs no critical adjustments.

Figure 2.16 shows a linearly injecting signal to a CCD by measured charge method. The circuit consist of a charge detector, which senses the amount of charge injected to the first stage of a CCD, a comparator, which controls the FET input to the CCD.

Initially the first stage of the CCD is empty as the FET is turned off. The charge detector is set in order to measure a new charge. Now applying the signal Vin, will cause the comparator to turn on the FET, causing current flow to the CCD. Therefore a corresponding charge accumulate in the first stage. The charge detector, detects this charge, as the first stage is filled up. The comparator compares the output with the input and turn off the FET. This method eliminates the nonlinearity caused due to the depletion region capacitance. This circuit is shown in Fig. 2.17. Non destructive sensing is used at the output to detect the charge in the CCD. The Fig. 2.17 uses two detectors, one at the input and one at the output, having same electrical characteristics.

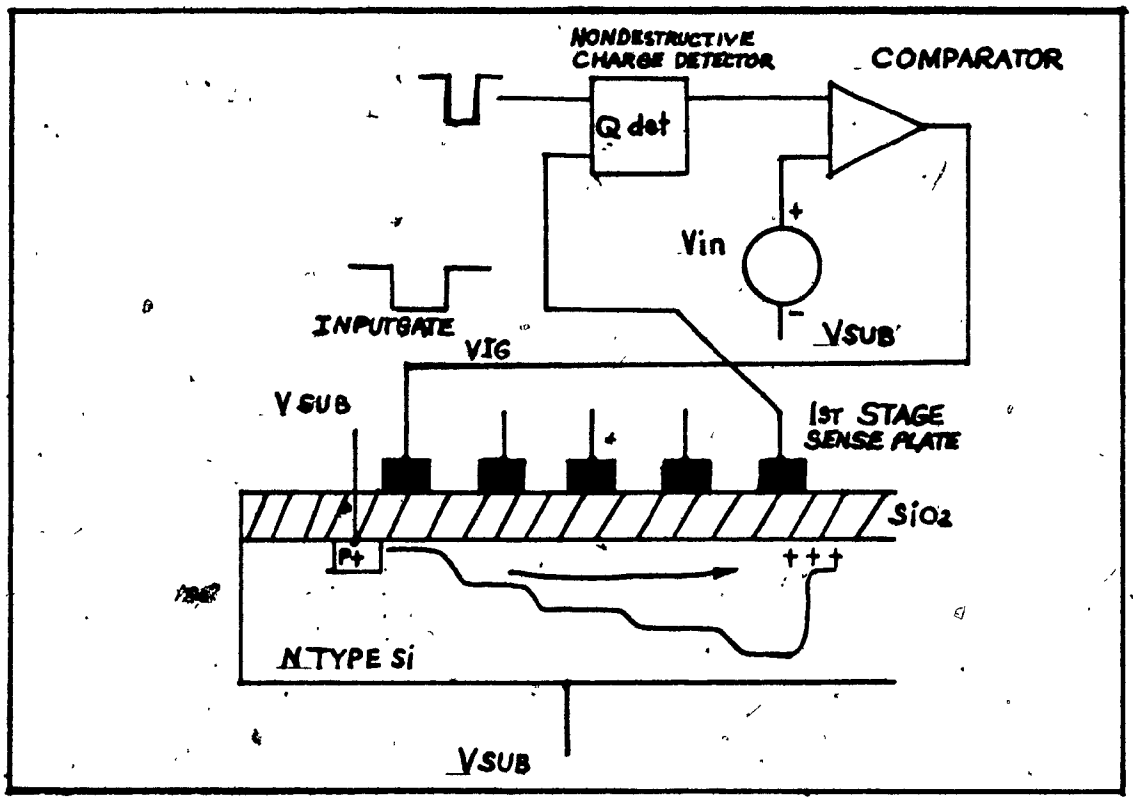


Figure 2.16 Measured charge method of injecting the input. (Courtesy: Reference 7)

In charge coupled devices, there are two types of charges namely, the free electronic charge Q_n, which is propagated through the CCD and the bulk charge Q_b, which resides in the depletion region. These two charges Q_n and Q_b, causes a corresponding signal charge Q_s to accumulate outside the semiconductor on the sense plate of the CCD. Hence Q_s can be written as follows:-

$$|\delta Q_s| = |\delta Q_n| - |\delta Q_b| \quad \ldots\ldots(2\text{-}6)$$

In linear Current method, the free electronic charge δQ_n is proportional to the input signal on account of this the signal current is a nonlinear function of δQ_n, as δQ_n is related to δQ_b, the depletion region capacitance. This nonlinearity can be reduced in many of the CCD applications by using a high resistivity substrate, keeping the sense plate voltage constant and limiting the range of δQ_n.

However, in the measured charge method δQ_s, measured signal charge is proportional to the input signal, on account of this, if nonlinearity exists in the input current or if leakage currents are present, the circuit completely eliminates these sources of non-linearities due to depletion region capacitance. In Fig.2.17, it does not really matter how much charge is stored in the depletion region capacitance, as both the input and the output circuits are strictly functions of the

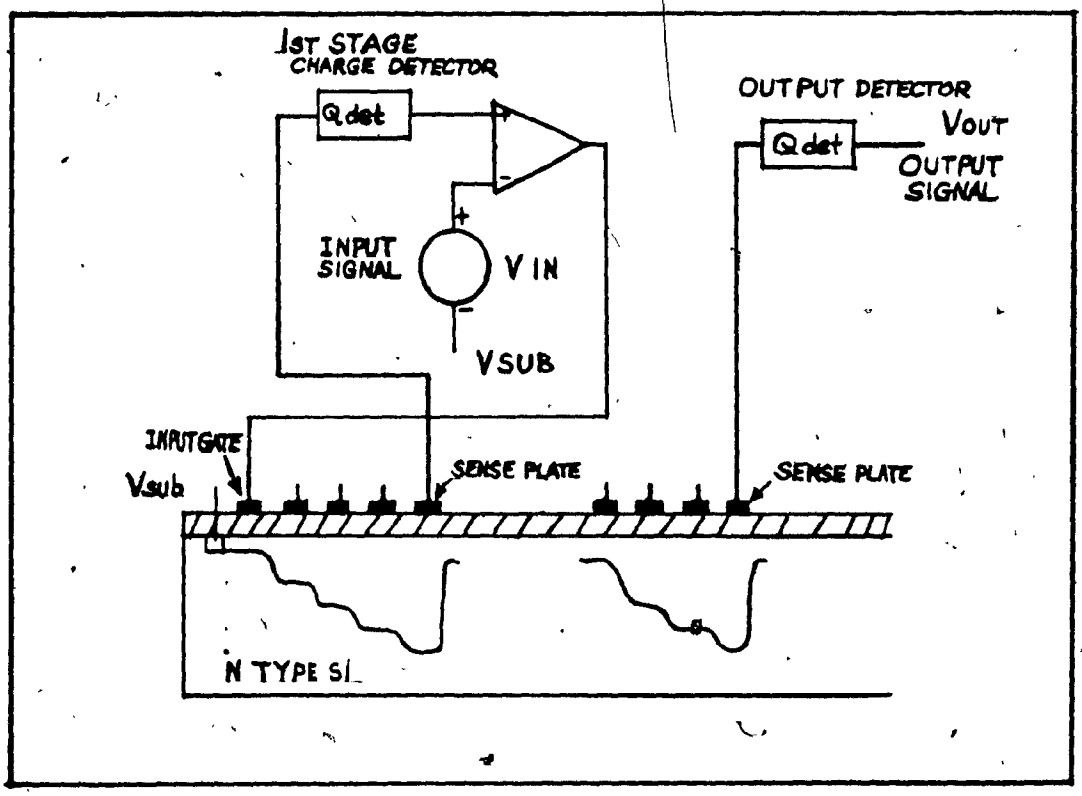


Figure 2.17 Circuit for eliminating the nonlinear effects of depletion region capacitance.(Courtesy:Reference 7)

signal charge SQs. It does not matter, even if the detectors are nonlinear. The only requirement for the detectors being they should be non-destructive and have identical electrical characteristics.

2.4. Weighting

In order to process the analog signal successfully by a charge coupled device, requires accurate weighting of each CCD tap. Figure 2.18, shows split conductance weighting concept used in a single stage CCD. The weighting network consists of R_1 and R_2. The network is placed between the CCD sense plate and the charge detector $Q_{det.}$

The weighting factors depends upon the values of resistance R1 and R2. Hence the weighting factor can be expressed as follows:

$$\text{Weighting factor} = \frac{R_2}{R_1+R_2} \quad \ldots\ldots\ldots\ldots (2.7)$$

The output voltage of the charge detector is given by

$$V_{out} = \frac{1}{C} \frac{R_2}{R_1+R_2} \int i_p dt \quad \ldots\ldots\ldots\ldots\ldots (2.8)$$

The only disadvantage of the circuit is that the dynamic range is limited to the ratio of two resistors. To increase the dynamic range, the ratio has to be increased.

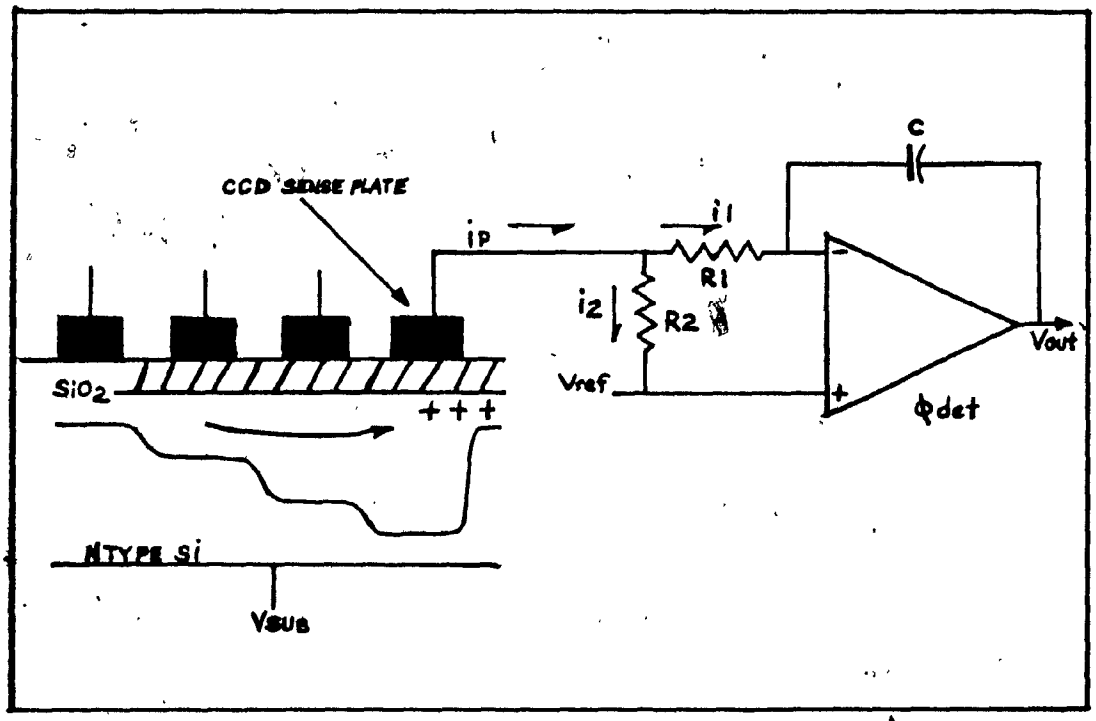


Figure 2.18 Split conductance weighing.
(Courtesy: Reference 7)

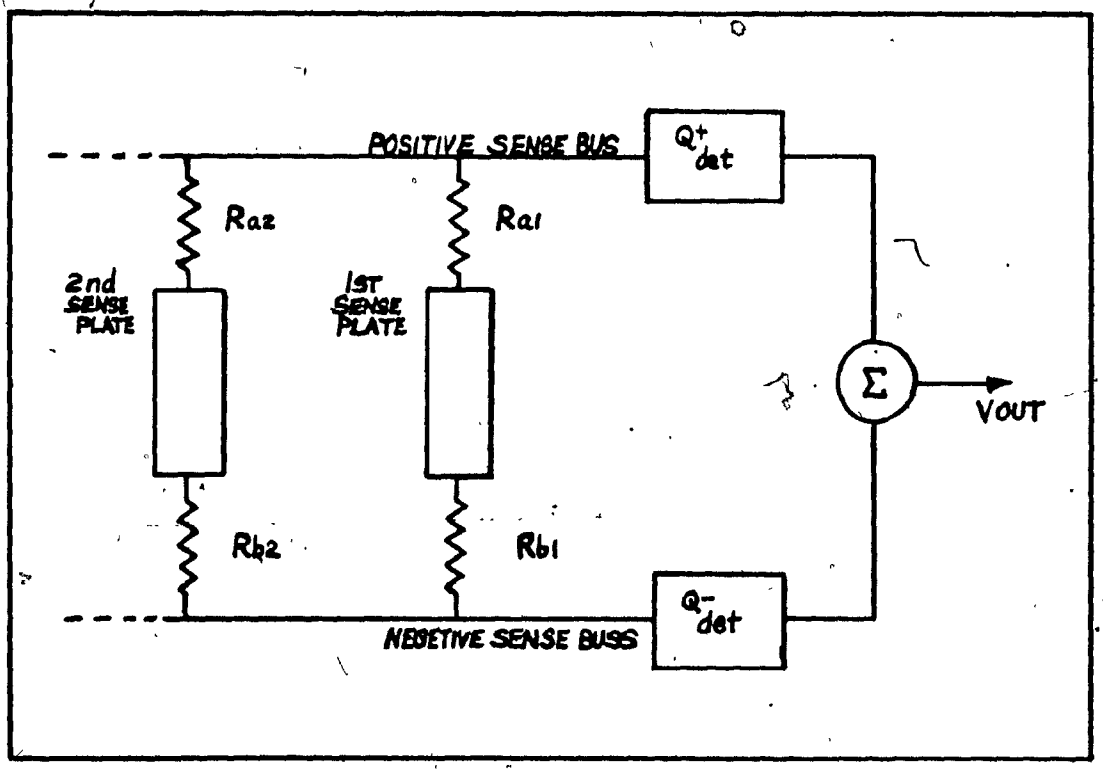


Figure 2-19 Split conductance weighing technique.
(Courtesy: Reference 7)

This in turn calls for large values of resistance which is difficult to achieve in integrated circuits. In order to overcome this problem, two detectors as shown in figure 2.19 are used.

The ouput of the positive and negative detectors are summed up to give the output, V_{out}. In this case the magnitude and sign of the weighting coefficients are uniquely determined by the conductance net work for each plate. The weighting coefficient h_i, for the i^{th} sense plate is given by

$$h_{(i)} = \frac{R_{b(i)} - R_{a(i)}}{R_{b(i)} + R_{a(i)}} \qquad \text{.....(2.9)}$$

As the weighting coefficients are determined by the difference of two resistors, a large dynamic range is possible, without increasing the values of R_1 and R_2.

2.5. Frequency

At present charge coupled devices can be operated upto 10 MHZ without any difficulty. Above 10 MHZ, it is preferable to use surface acoustic wave devices. However Buried channel CCD can be operated at a much higher frequency than surface channel CCD[8]. This is shown in Fig. 2.20.

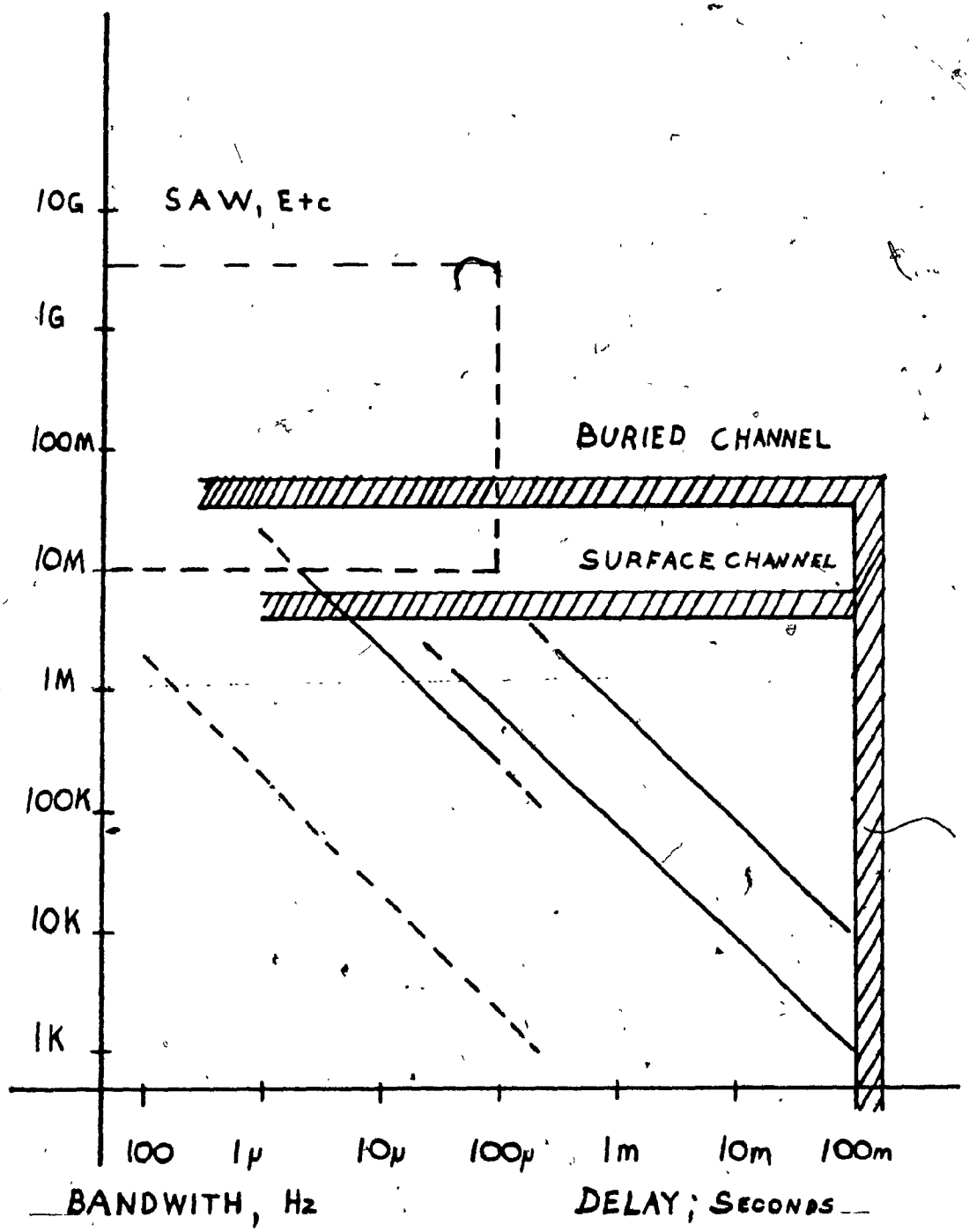


Figure 2-20 Frequency limits of charge coupled devices. (Courtesy: Reference 8)

CHAPTER III

FILTER IMPLEMENTATION

There are two methods of implementing CCD transversal filters namely,

1. Split-electrode technique;
2. Biased-gate tapping technique.

3 - 1 SPLIT-ELECTRODE TECHNIQUE.

In this technique, it is assumed that the capacitance formed by the depetion layer namely, Cd, is lower than the capacitance of the oxide layer, C_{ox} and C_d is constant. Cd, depends on the width of the layer and the width depends upon the gate voltage.[10] The depletion layer is devoid of electrical charges and as such it has high resistivity. The depletion layer Capacitance, Cd is in versely proportional to the width of the layer. If the silicon-di-oxide layer formed by exppsing silicon to oxygen at very high temperature, is thinner than the width of the depletion layer, than the oxide layer capacitance C_{ox}, is greater than depletion layer capacitance C_d. This improves the linearity of the transversal filter.

In split-electrode technique[11], the electrode is split either in the middle or at the top or at the bottom. The charge on each side is measured, and given to a difference amplifier. The difference in the charge on the two sides of the electrode gives the weighted sample. Hence in order to implement a CCD

transversal filter, it is required to sample the delay line and perform a weighted summation. The basic principle used is to measure, the charge under the CCD electrode and to integrate the current that flows in the clock-line during the charge transfer. Figure 3.1 shows the schematic diagram of a split electrode weighting and summing.

Assuming the substrate has high resistivity, the integral of the clock line current can be written as follows:-

$$Q_K^C = V_c C_d + Q_k^t \qquad \text{.....(3-1.)}$$

In order to weigh each sampled charge, the electrode Q_3 is split into two parts namely $Q_3^{(+)}, Q_3^{(-)}$. Identical inputs are given to both $Q_3^{(+)}$ and $Q_3^{(-)}$ and the difference between the charges in the two electrodes are measured by a difference amplifier.

Let the two inputs applied to $Q_3^{(+)}$ and $Q_3^{(-)}$ be as follows:-

$$Q_3^{(+)} = \frac{1}{2} (1+hk) \qquad \text{.....(3-2)}$$

$$Q_3^{(-)} = \frac{1}{2} (1-hk) \qquad \text{.....(3-3)}$$

The output of the difference amplifier is given by

$$V_{OUT} \propto \sum_{k=1}^{M} \frac{1}{2} (1+hk) Q_k^c - \sum_{K=1}^{M} \frac{1}{2} (1-hk) Q_K^C \qquad \text{..... 3-4.}$$

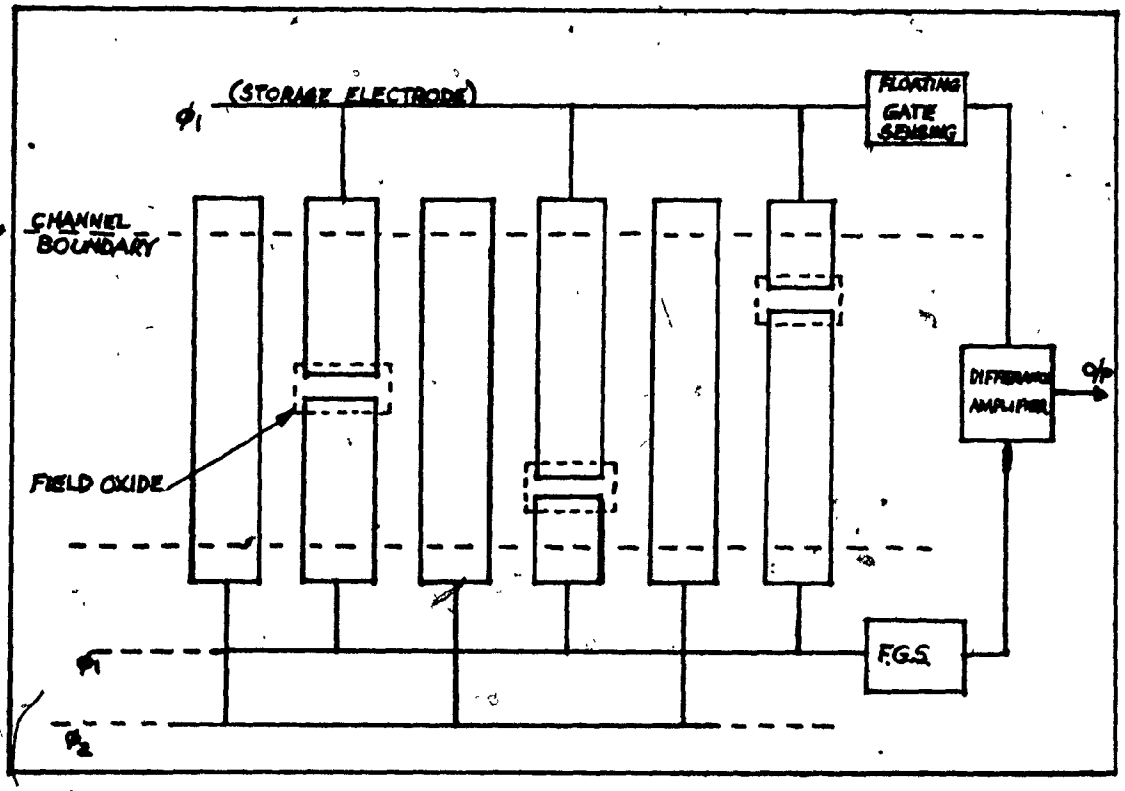


Figure 3-1 Split electrode weighing and summing technique. (Courtesy: Reference11)

$$\simeq \sum_{K=1}^{M} h_k Q_k^C \quad \text{.....(3-5)}$$

As already stated, the electrode can be split either in the centre or at the top or at the bottom. If the device is operated, splitting the electrode at the center, then the device is subject constant background charge or fat zero[6] and maximum charge. The split at the top corresponds to positive signal charge and the split at the bottom corresponds to negative signal charge. The signal charge in this case can be written as follows:-

$$Q_K^S = Q_K^t - \frac{1}{2} (Q_{max} - Q_{fz}) \quad \text{.....(3-6)}$$

Q_{fz} or the fat zero charge ensures that the interface remains permanently filled and so minimum distrubance with the the desired signal. The disadvantage of the fat zero is that, it brings down the dynamic range of the device considerably. Fat zero charge are in practice 10-25% of the full well capacity.

The charge transferred under the k^{th} electrode can be written as

$$Q_k^t = Q_k^s + \frac{1}{2} (Q_{max} - Q_{fz}) \quad \text{.....(3-7)}$$

Substituting equation (3-7) to equation (3-1), we have that,

$$Q_k^C \simeq V_c C_d + Q_k^S + \frac{1}{2} (Q_{max} - Q_{fz}) \quad \text{.....(3-8)}$$

Substituting this value of Q_k^C in equation (3-5), we have that,

$$V_{out} \propto \left[V_c\ C_d + \frac{1}{2}\ (Q_{Max} - Q_{fz})\right] \sum_{K=1}^{M} h_k + \sum_{K=1}^{M} h_k\ Q_k^S \qquad \ldots\ldots\ldots(3\text{-}9)$$

The first part of the equation (3-9) consists of a d.c. component which can be eliminated by a capacitor. Hence 'V_{out}' can be written as follows:-

$$V_{out} \propto \sum_{K=1}^{M} h_k\ Q_k^S \qquad \ldots\ldots\ldots\ldots\ldots(3\text{-}10)$$

Hence the output of the device is given by convolution of the impulse response bk by the input signal charge.

The floating gate sensing circuit is shown in Fig.3.2. The sensing circuit transforms nondestructively, the Signal charge to an output voltage at each tap position, along the CCD delay line. The tapped voltage may be weighted by a conductance. It is the basic property of a CCD, that the Signal charge can be passed under a sensing electrode and this does not in anyway result in any signal degradation.[12] On the other hand, by repeatedly sensing the signal charge, improves the signal-to-noise ratio of the signal.

Figure 3.2, shows a block diagram of a charge sensing amplifier.[13] The charge sensing amplifier nondestructively detects or senses the presence or absence of a signal charge at one end and transmits the signal charge to the other end. The sensing amplifier is sensitive to signal charge variations but insensitive to parasitic charges likely to be introduced during manufacturing or atmospheric charges deposited on the surface.

Charge sensing amplifier consists of two electrodes connected to the master and the slave ends. The two electrodes are separated by a distance, on which is mounted an field-effect transistor.

When a voltage is appliced to 'VG' in Fig. 3.2 , V_G, turns on the FET, allowing the signal charge to be applied to the charge sensing amplifier. After a short time, the gate voltage is removed and this turns off the FET. Hence the signal charge is floating and the charge is distributed as surface potentials under the master and slave electrodes. Therefore as the signal is dumped under the master electrode, it detects the presence or absence of signal charge.

Fig. 3.3 , shows the hamonic distortion produced by a CCD transversal filter sensing circuit. For an input signal of IKHZ, sampling frequency being 30 KHZ, the peak to peak

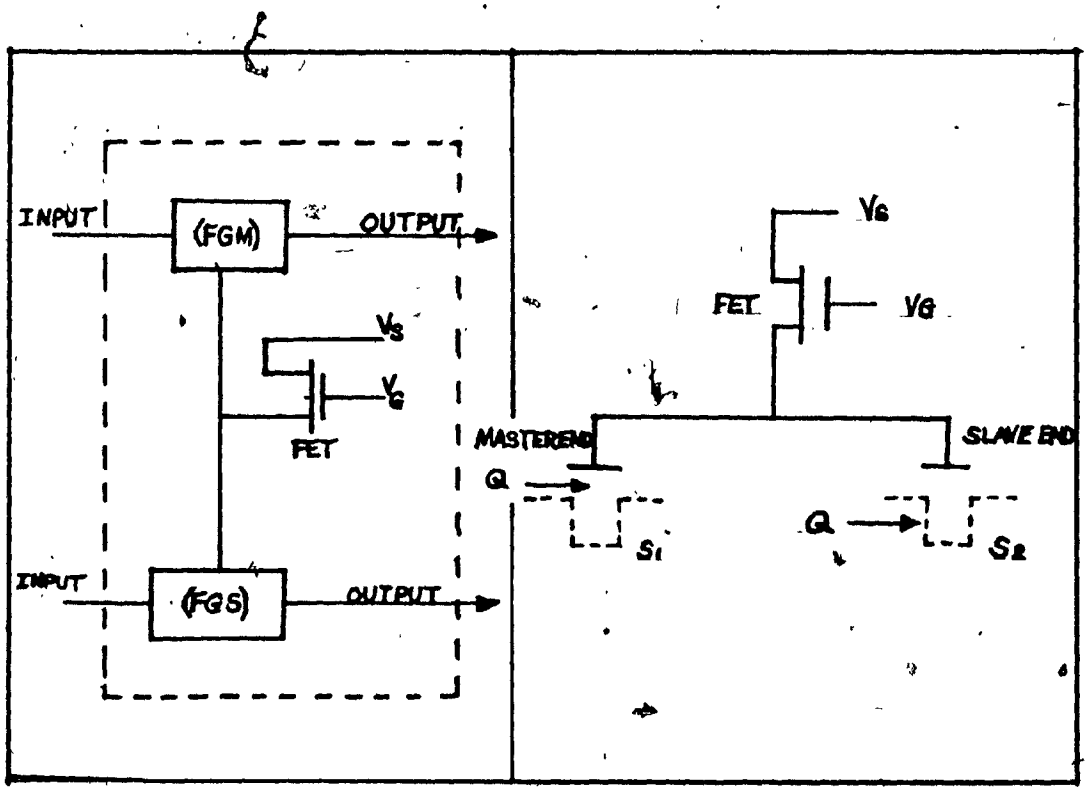


Figure 3-2 Block and circuit diagram of a charge sensing amplifier with FET. (Courtesy: Reference 13)

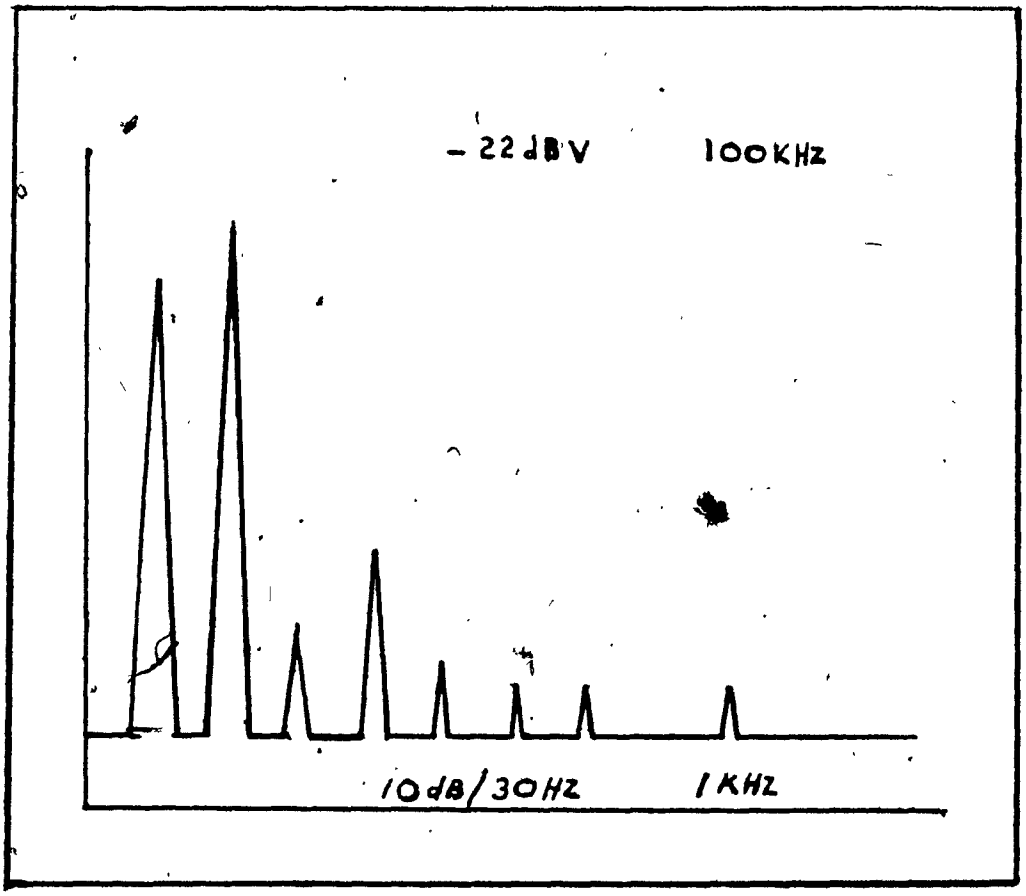


Figure 3.3 Harmonic distortion of a CCD transversal filter sensor circuit.(Courtesy:Reference 15)

voltage being 0.5 volts, the harmonic distortion was less than 0.3%, which can be tolerated.

3-2. Biased-Gate Tapping Technique

In the split-electrode technique, the weighting co-efficients of the transversal filter are fixed and as such cannot be varied. In the biased-gate tapping technique, the weighting coefficients are variable. Therefore, in biased-gate tapping technique,[14] one set of clocking electrodes are charged to a d.c. potential. When a charge is clocked on the electrode, the electrode potential alters and remains at a new value, until the charge is removed. The change in potential well on the electrodes are sensed by a M.O.S. transistor.[15] amplifier. Therefore, the biased-gate tapping technique is also referred to variable coefficient filter.

Figure 3.4 shows a CCD shift register, with three electrodes namely ϕ_1 ϕ_2 and ϕ_3. The electrode ϕ_2 is charged with an initial d.c. voltage. When a signal charge is introduced, the d.c. potential will vary in order to maintain equilibrium. In the absence of the signal charge, the electrode ϕ_2 will revert back to its original value. The potential charges can be sensed by an amplifier. The electrode ϕ_2 is referred to as the biased gate, as ϕ_2 is biased by a d.c. voltage. As the output is also tapped from electrode ϕ_2, this technique

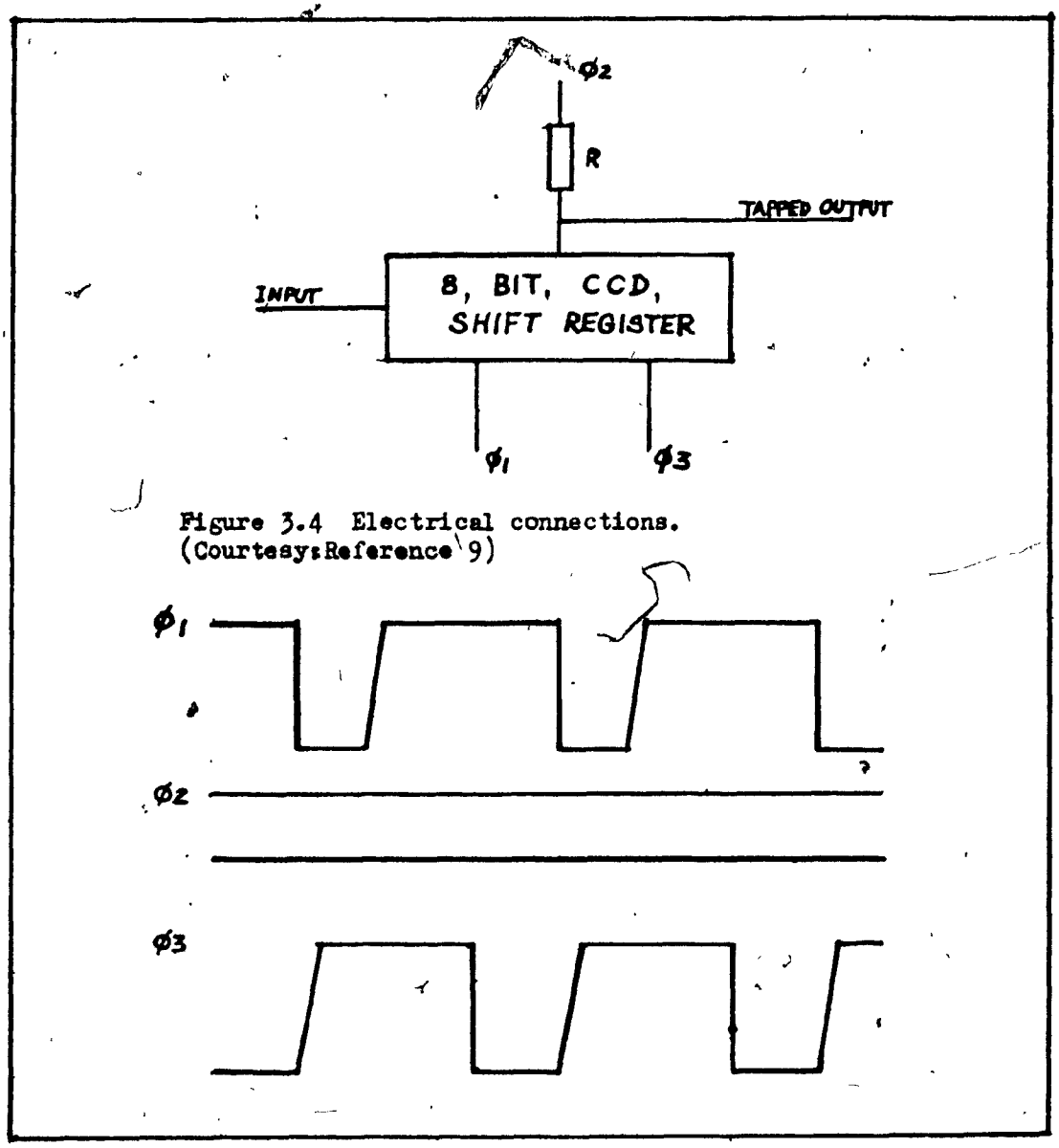


Figure 3.4 Electrical connections.
(Courtesy:Reference 9)

Figure 3.5 Clock waveforms.
(Courtesy:Reference 14)

is called "Biased-gate tapping technique."

Figure 3.5 shows, the clock wave forms, of the three electrodes. As the clock voltages are changing with respect to the bias on the gate, the effective voltage is the difference between the peak clock voltage and the d.c. bias. on account of this, the effective peak signal voltage is reduced, reducing the efficiency of the device. The reduced efficiency can be overcome by increasing the clock voltage. The charge handling capacity can be increased, by increasing the area of the biased electrode.

The maximum charge that a gate can handle is given by

$$Q_{max} \propto \frac{A_b \cdot A_c}{A_b + A_c} \qquad \text{.....(3-11)}$$

where A_b, is the area of the biased-gate and

A_c, is the area of the clocked-gate.

In order to compute, the response of the biased-gate to Signal charge, an equivalent circuit to Fig. 3.4 can be drawn. The equivalent circuit is shown in Fig. 3.6a

Assuming the depletion capacitance per unit area 'C_d' to be constant, Vs, the gate voltage change due to the Signal charge Q_s is given by,

$$V_S = \frac{Q_s A_b}{C_g} \qquad \text{.....(3-12)}$$

where Cg is total capacitance external to CCD channel and $C_g \gg C_d A_b$ and C_d

$$C_d \leq C_{ox}.$$

The transfer characteristics namely the output voltage against signal charge is shown in Fig. 3.6b . As long as the signal excursions are kept and maintained in the linear region of the curve, a linear output voltage can be developed.

Figure 3.7 shows the circuit of Fig. 3.4 with sensing, external weighting and summing. Q_1 is CCD storage electrode, T_1 is emitter follower and T_2, the M.O.S. transistor sensing circuit. The signal is sensed during the time, the charge is stored in storage electrode Q_1. In order to prevent loading and charge losses, $C_{ox}/C_d \simeq 100$. The 32 delay outputs were externally weighted and summed up. The filter coefficients can be easily varied, by changing the resistor values in the summing circuit.

The K^{th} coefficient is given by,

$$h_k = \frac{R_{f1}}{R_k} \frac{R_{f2}}{R_S} \qquad \text{.....(3-13)}$$

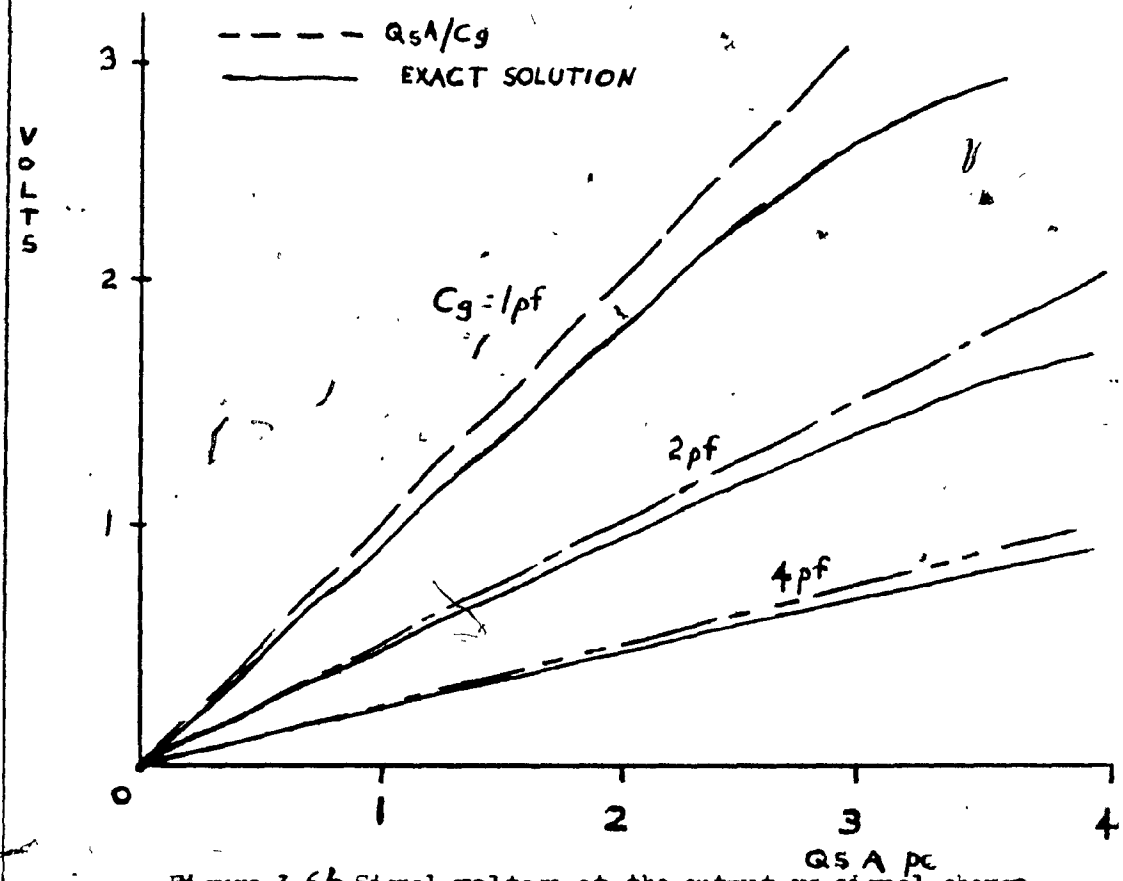


Figure 3-6b Signal voltage at the output vs signal charge. (Courtesy: Reference 14)

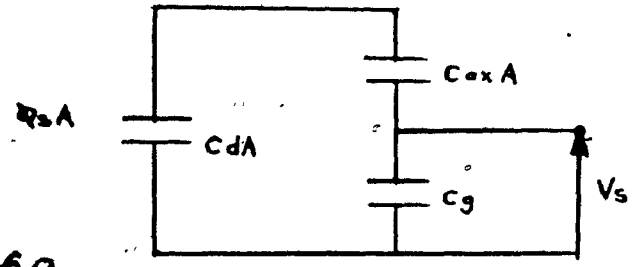


Figure 3-6a
Equivalent circuit for biased gate. (Courtesy: Reference 14)

Where R_{f1} and R_{f2} are feedback resistances and R_s is coupling resistance in the output circuit.

A 32-stage band pass filter was implemented using this technique. The filter was designed to give 55 dB attenuation in the stop band.

Figure 3.8 shows, the frequency characteristics of the filter. Each curve in the figure was plotted again and again, after adjusting the resistors in order to get an accurate agreement with the calculated response. The measured curves showed good agreement in the passband but had deviations in the stop band. These deviations are due to mainly inaccuracies in the setting of filter coefficients. A tap error of 1% will raise the stop band magnitude by about 6dB. But if random error is present in all of the taps, the response will vary in unpredictable manner. This is seen in Fig. 3.8 . Hence there is a practical limit to output attenuation, when a single transversal filter is used.

In order to make full utilization of CCD bandwidth, the CCD shift registers of Fig. 3.4 , can be operated in parallel as shown in Fig. 3.9 .

A sample from each of the clock phases are passed down separate shift registers. After an equal number of transfers, the signal is detected. This increases the bandwidth of the

data by three for a three phase device shown in Fig. 3.9 . Table 3-1 gives comparison between normal design and parallel operation. The table speaks for itself of the advantages of parallel operation.

PARAMETER	NORMAL DESIGN	PARALLEL DESIGN	UNIT
ACTIVE LENGTH	2.286	0.762	mm
ACTIVE WIDTH	0.1	0.3	mm
RESIDUAL LEVEL	-28.4	-37.9	dB
CLOCK FREQ	1	0.333	MHZ

Table 3-1 comparison is for 127 Bit, 1 MHZ data rate, linear CCD array.

Transfer inefficiency puts a limit on the maximum number of elements that can be used.[8] This transfer inefficiency in certain applications gives rise to dispersion, which attenuate high frequencies compared to low frequencies. This dispersion can be minimized by operating the device in parallel. But the parallel operation reduces transfer rate and also the total number of transfers made by the signal. Observation prove parallel operation improves high frequency response considerably at the cost of noise. More research appears to be carried out in this direction, in order to make

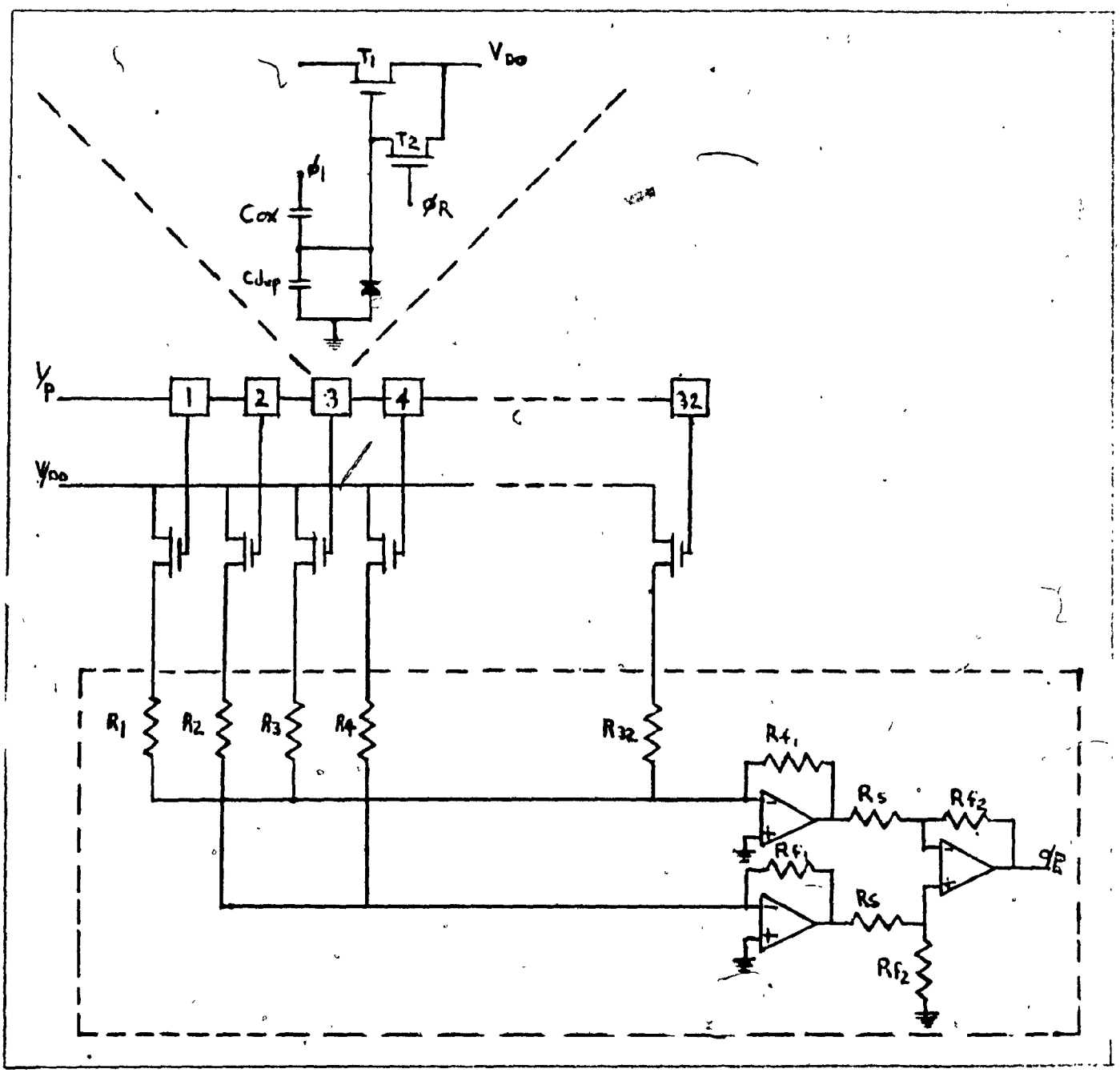


Figure 3-7 Circuit showing voltage sensing diffusion technique. (Courtesy: Reference 15)

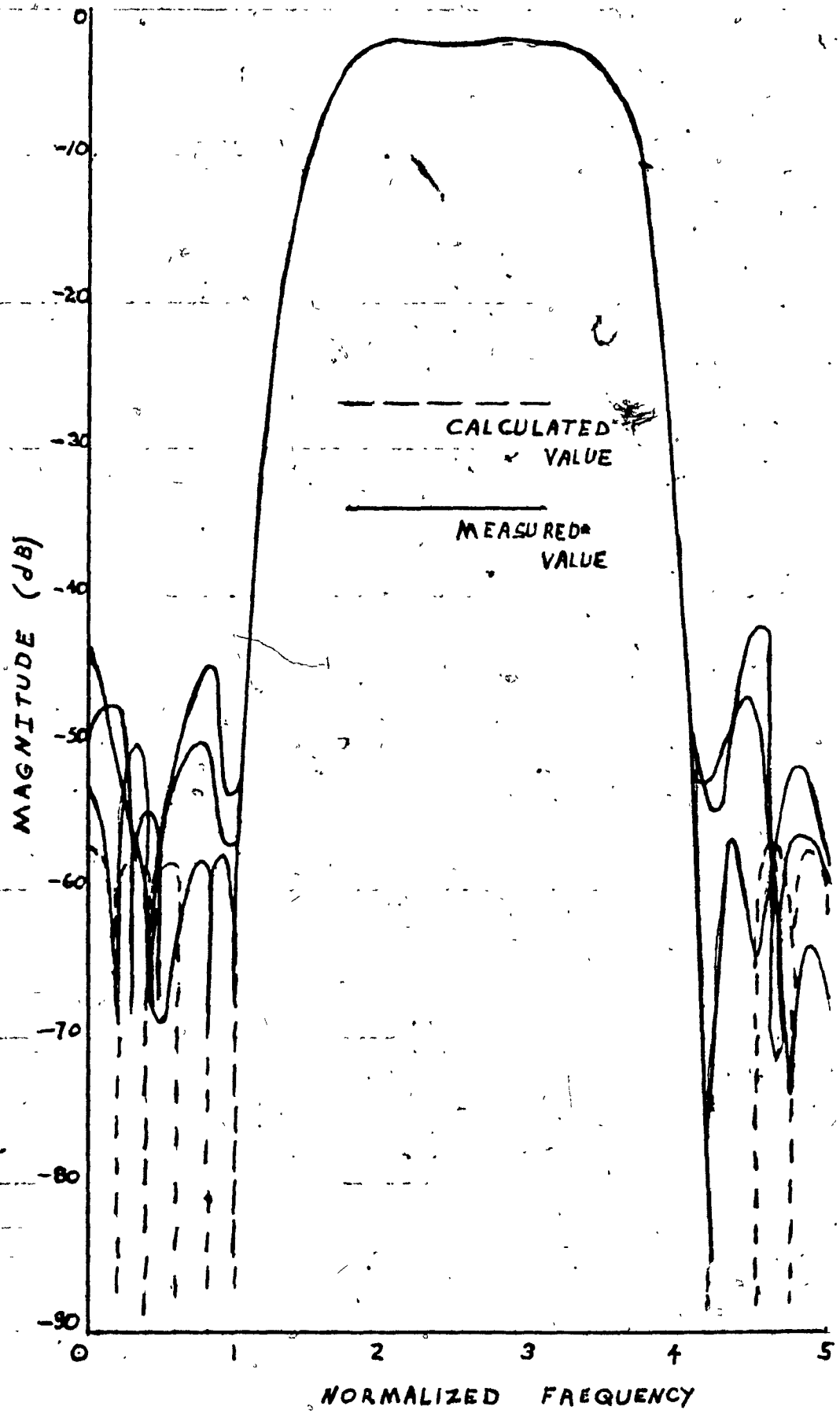


Figure 3-8 Frequency response of 32-tap bandpass filter, showing several measured responses. (Courtesy: Reference 15)

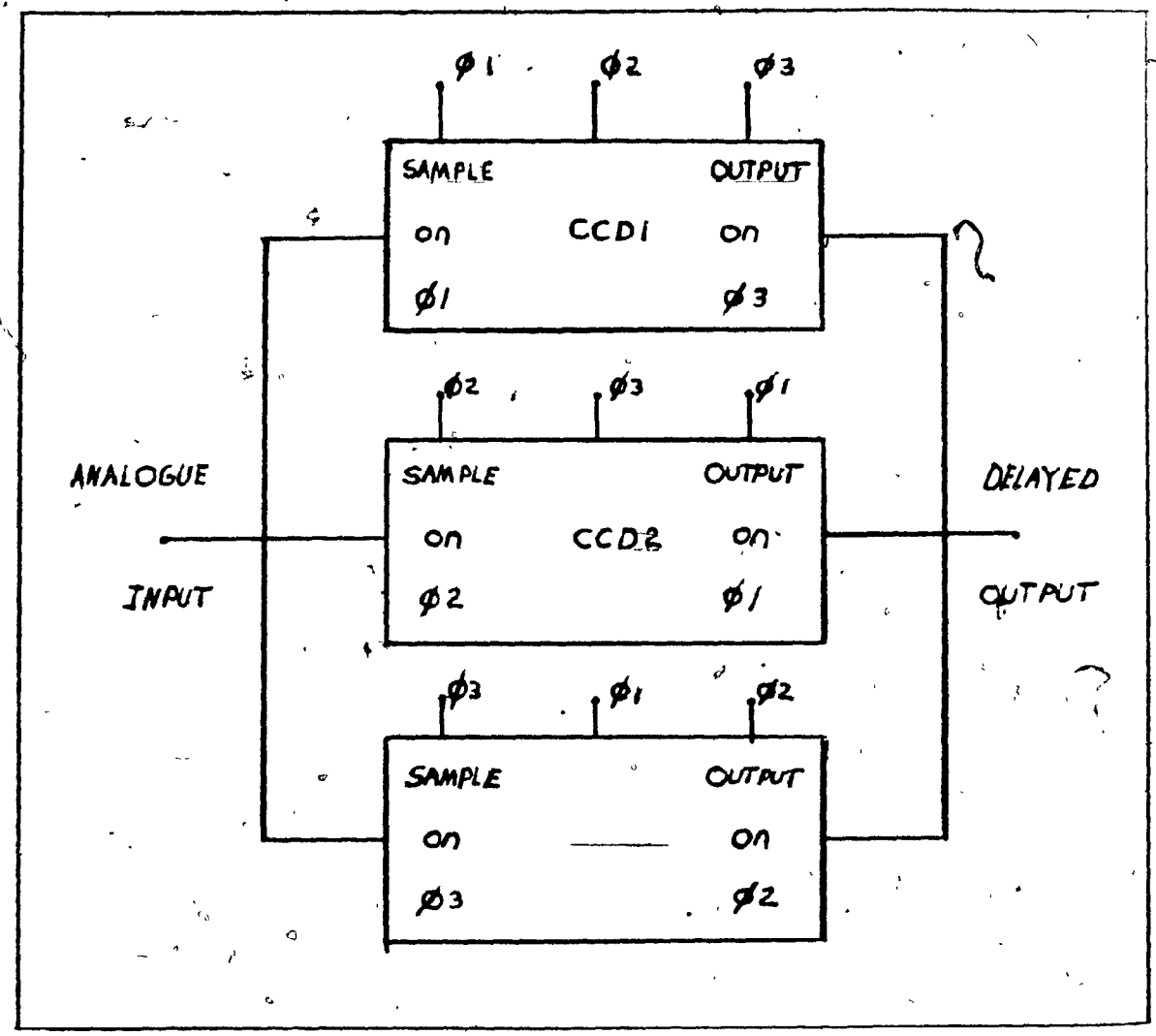


Figure 3-9 Parallel operation of a three phase charge coupled device. (Courtesy: Reference 4.)

Biased-gate tapping technique as popular as split-electrode technique.

Figures 3.10 and 3.11 show frequency response of a 24 tap low-pass filter implemented using split-electrode and voltage sensing diffusion.

It will not be out of the place to mention that the transversal filters implemented using biased-gate tapping technique have a number of uses in communication engineering. Transversal filters with variable weighting coefficients are used in matched filtering on a wave form which changes intermittently.[16] Secondly it can also be used in adoptive equalization. However, it is not clear whether the variable weighting coefficients filter has any definite advantage at all over the conventional digital filters.

3.3. Minimum - Phase CCD Transversal Filters.[17]

In all of the discussions carried out, the transversal filters were implemented using linear phase design only. Linear phase filters have constant time delay over the entire filter frequency band. This is extremely useful in data communication. The long time delays are undesirable in speech communication, as the time delays are going to introduce echo and singing on voice channels.

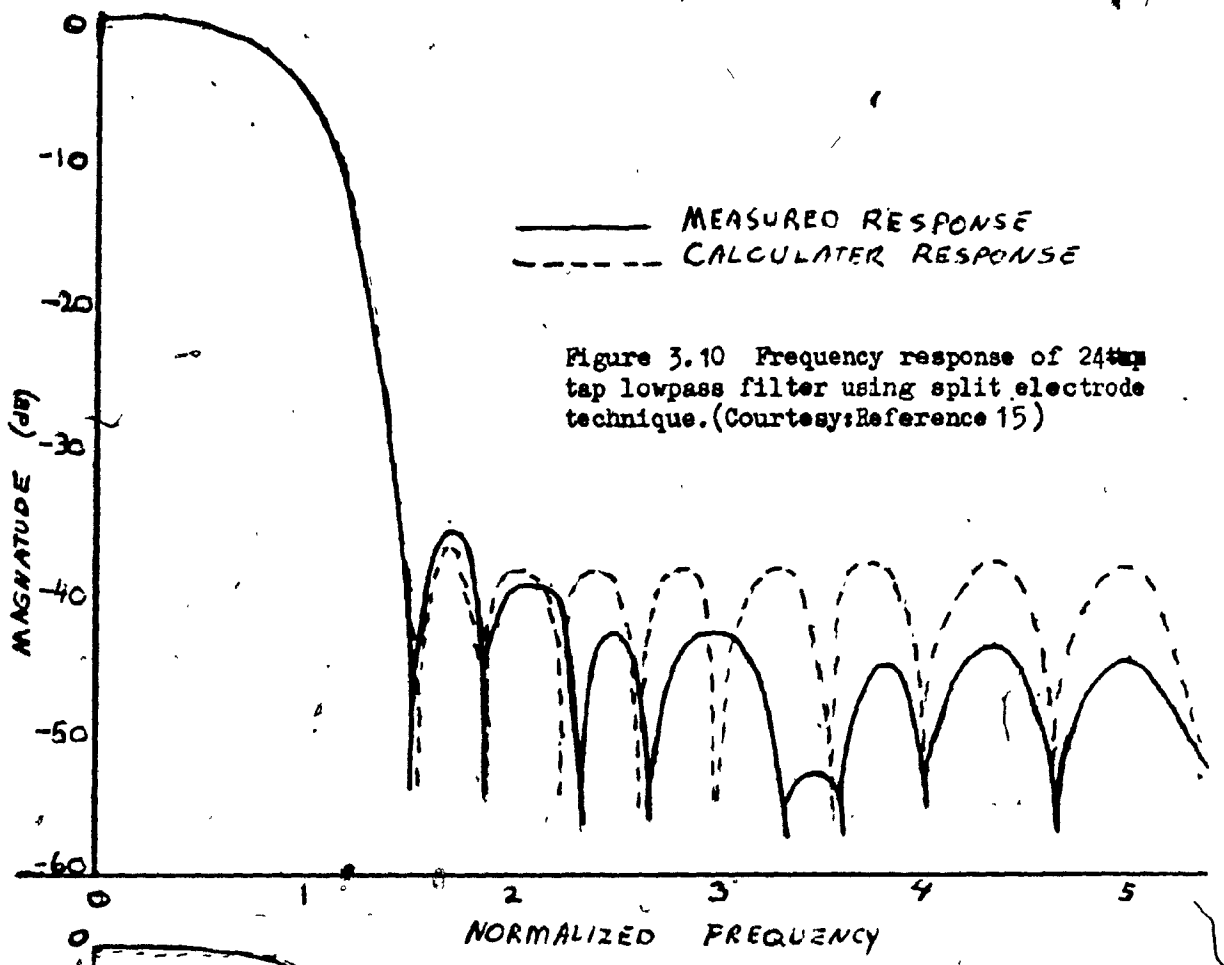


Figure 3.10 Frequency response of 24 tap lowpass filter using split electrode technique. (Courtesy: Reference 15)

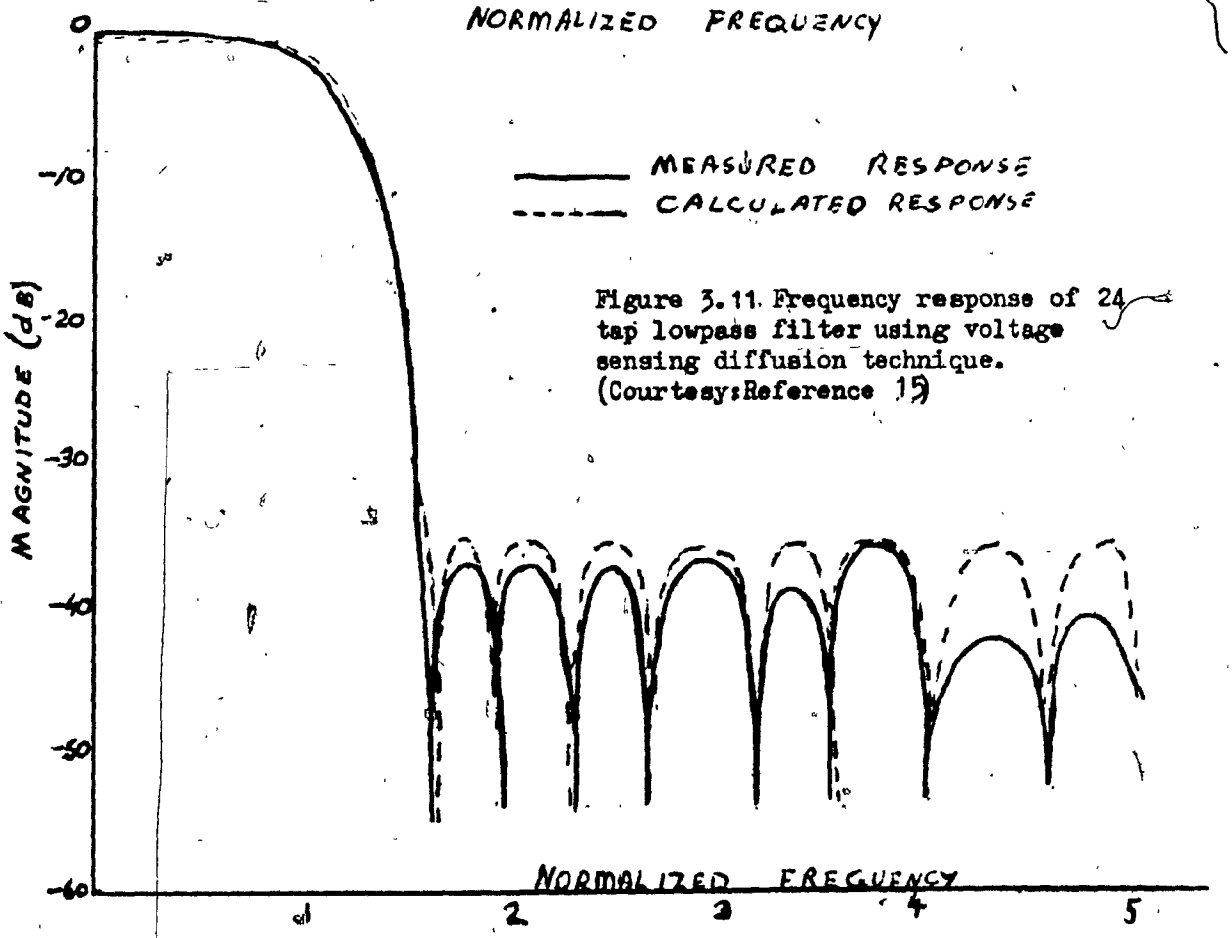


Figure 3.11 Frequency response of 24 tap lowpass filter using voltage sensing diffusion technique. (Courtesy: Reference 15)

For an N-Stage transversal filter, the group delay is given by

$$TG = \frac{(N-1)T}{2} \qquad \ldots\ldots\ldots\ldots (3\text{-}14)$$

where T = time delay per stage;

N = Number of stages.

Hence the group delay increases as the number of stages increase. In order to decrease the time delay, for voice communication, the transversal filters may be designed with minimum phase instead of linear phase. The basis for minimum phase design of transversal filters is based on the article written by McClellan et al.[18]

In the case of linear-phase design, the zeros of the polynominal occur on the unit circle, $|Z| = 1$ or as conjugate reciprocal pairs namely r, θ and $1/r, \theta$ respectively. The pole-zero plot for a 32-tap linear-phase transversal filter is shown in Fig. 3.12.

A minimum-phase transfer function on the otherhand has all zeros located on or inside the unit circle in the Z-plane. This suggest that if all the zeros of Fig. 3.12 could be moved inside the unit circle by some means without effecting the magnitude response, the filter will have minimum-phase. The pole-zero plot for a filter having minimum-phase is shown in Fig. 3.13.

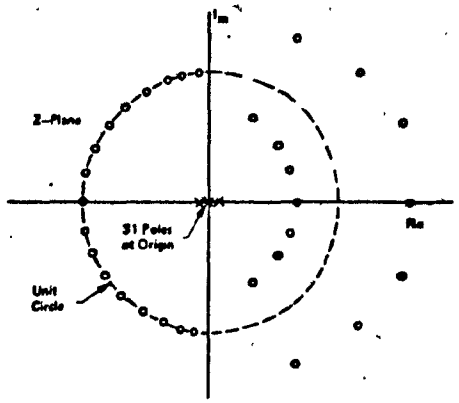


Figure 3.12 Pole-zero configuration for a linear-phase 32 tap ccd low-pass filter.(Courtesy:Reference 17)

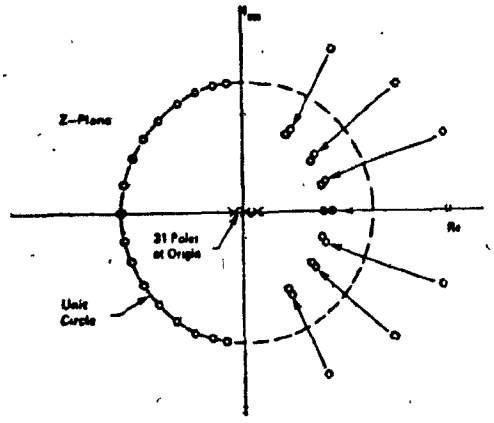


Figure 3.13 Pole-zero configuration for a minimum-phase 32 tap low-pass filter.(Courtesy:Reference 17)

In moving the complex conjugates to conjugate reciprocal locations in the z-plane has the effect of adding or removing all-pass sections from the filter.[19] This is nothing other than changing the phase of the filter without affecting the magnitude.

A comparison of the group delay between the linear-phase and minimum-phase design is shown in Fig. 3.14. It can be seen from the curve, that in the case of minimum-phase low-frequencies suffer 90% less delay than the corresponding linear-phase design.

Fig. 3.15 shows a comparison between the linear and minimum-phase in as far as the magnitude error is concerned. The peak error is about 35% less for minimum-phase design. Hence the minimum-phase transversal filter is less sensitive to transfer inefficiency than a linear phase transversal filter. The phase error due to transfer inefficiency is also reduced for a minimum-phase filter. This shown in Fig. 3.16.

In figures 3.17 and 3.18, the coefficient values for the 32-tap low-pass filter for linear and minimum-phase are compared. The absolute maximum tap value, maximum/hi/is about 7% less for minimum-phase. The means that a minimum-phase transversal filter has 7% more coefficient tolerance than linear-phase filter. This result was verified by Monte carlo

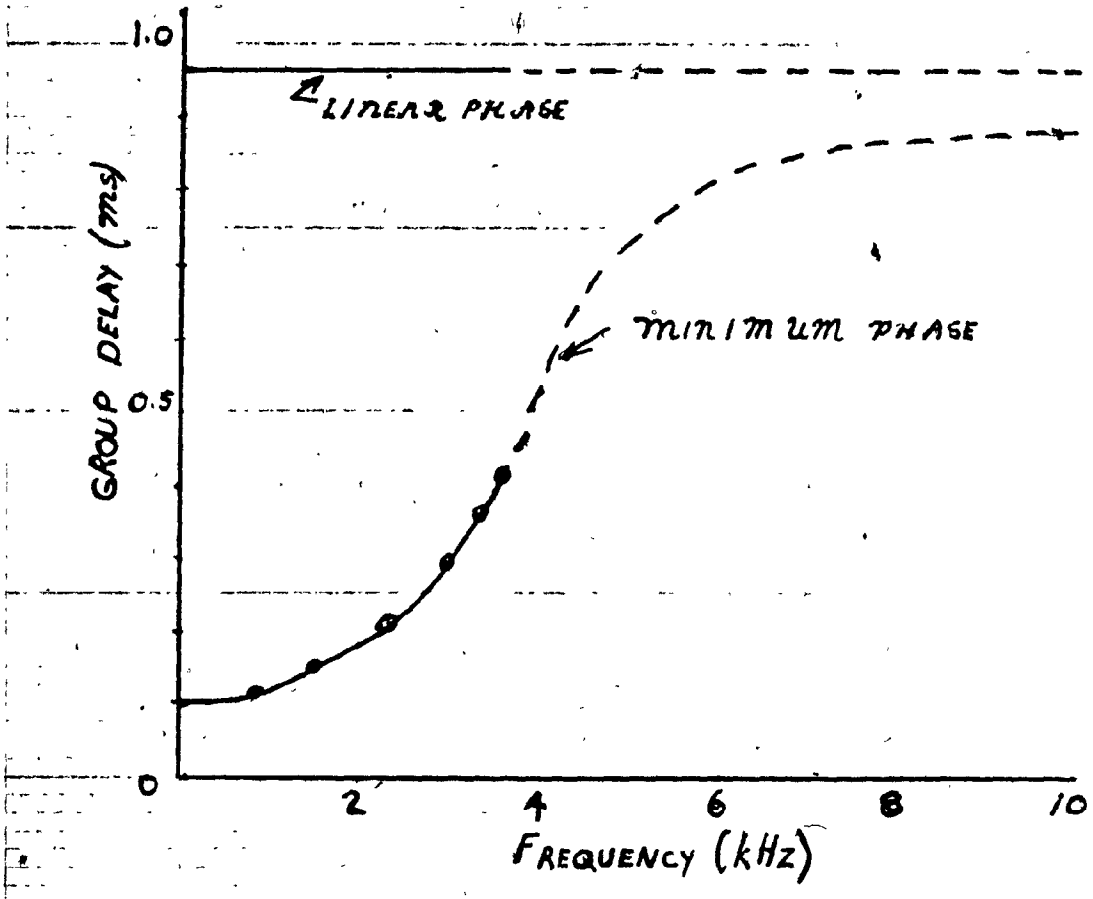


Figure 3.14 Comparison of group delay between linear and minimum phase CCD transversal filters. (Courtesy: Reference 17)

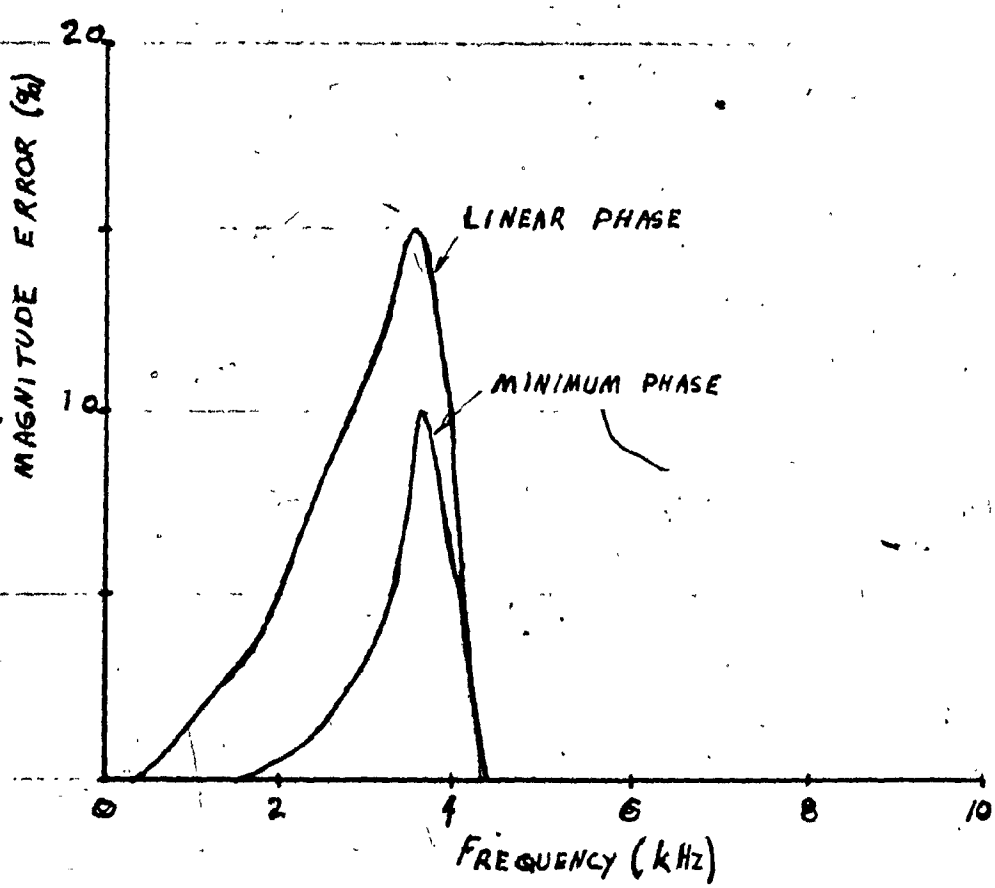


Figure 3.15 Comparison of magnitude error due to transfer inefficiency for a 32 tap low pass filter.(Courtesy:Reference 17)

simulation. This is shown in Fig. 3.19.

3.4. Prefilter requirements in CCD transversal filters.

Any input frequency f_i close to the clock frequency f_o, will give rise to (f_o-f_i) and (f_o+f_i) by aliasing.[20] Suppose the CCD transversal filter designed is a low-pass filter, then the spurious component (Fc-Fi) may fall inside the passband of the filter. In this case, the spurious component will appear in the output. In order to cancel these spurious frequencies from the output, the bandwidth of the input signal is limited by a prefilter, which rejects all frequencies above (f_o-f_i). This prefilter must have a large N/f_o ratio, where N is the number of taps and f_o, is the clock frequency. It is already mentioned that large value of N is undesirable, instead lowest clock frequency is used, in order to make the ratio N/f_o as large as possible. This gives a fairly low value for f_o/Fb where Fb is the passband frequency. Hence the prefilter has a sharp cutoff.

The prefilter can be implemented either by a passive Lc filter or by an active Rc network.[20] Implementing the prefilter in this case may exceed the cost of the main CCD filter and the attenuation obtained by a simple Rc filter would not be sufficient in many applications. Hence it is preferable to implement the prefilter compatible with CCD technology.

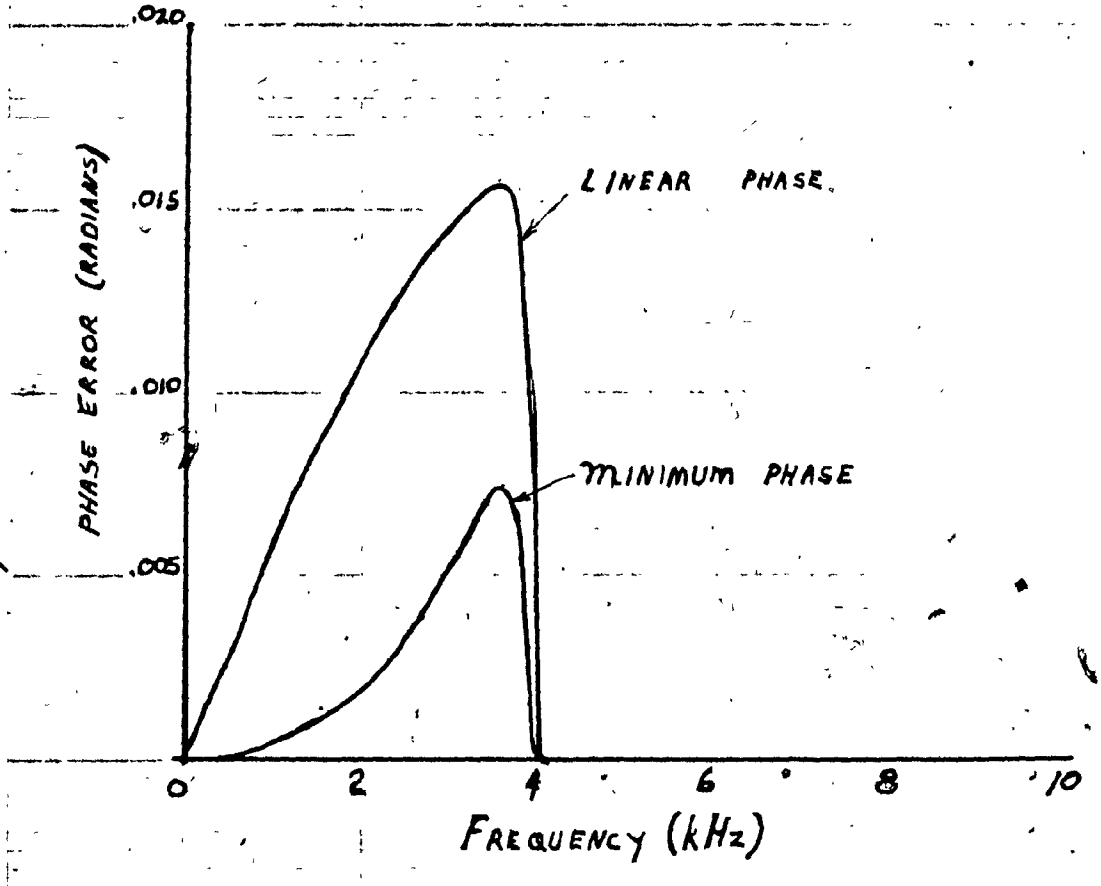


Figure 3.16 Comparison of phase error between linear and minimum phase 32 tap low pass filter. (Courtesy: Reference 17)

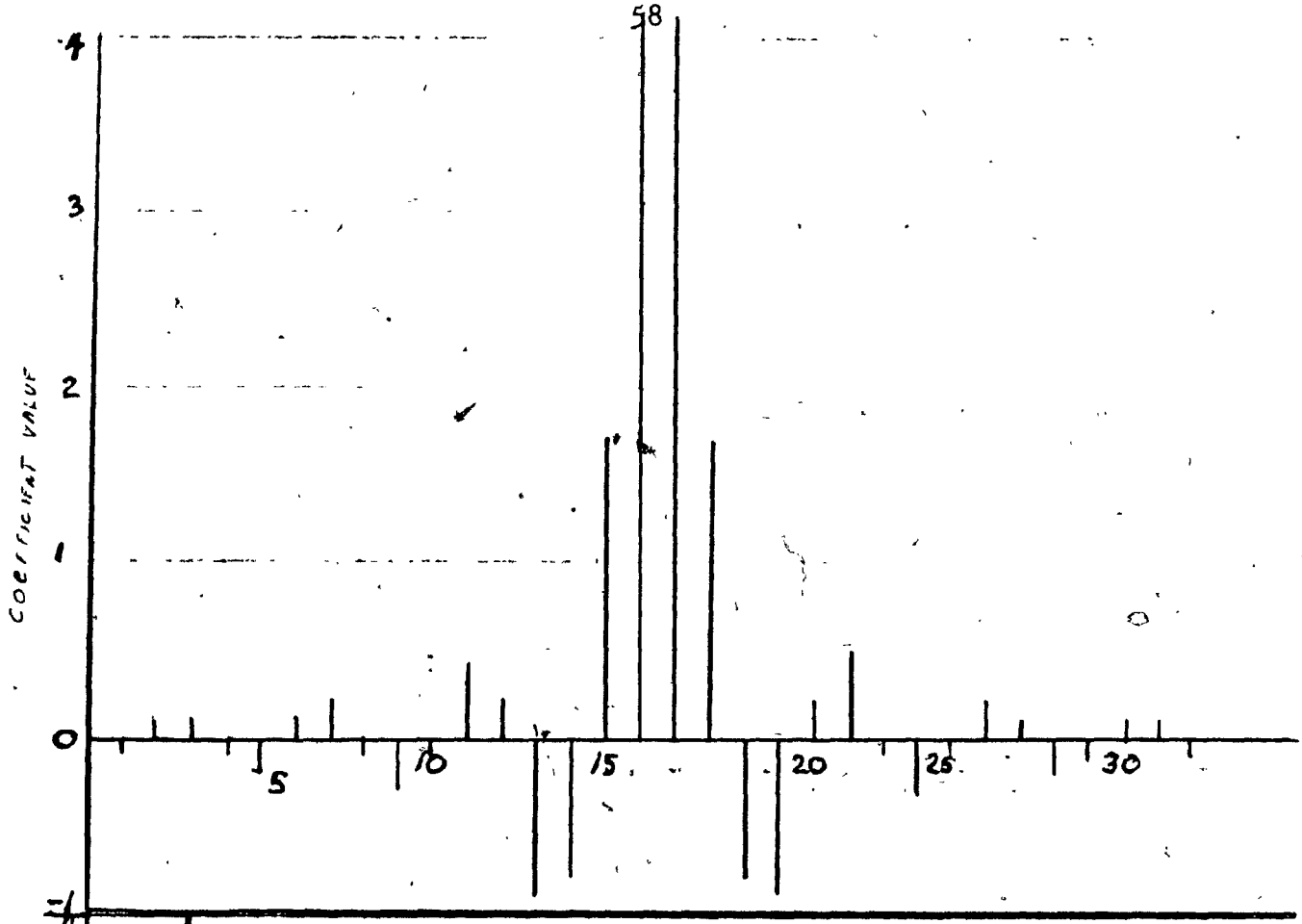


Figure 3.17 Coefficient values of 32 tap linear phase low pass filter. (Courtesy: Reference 17)

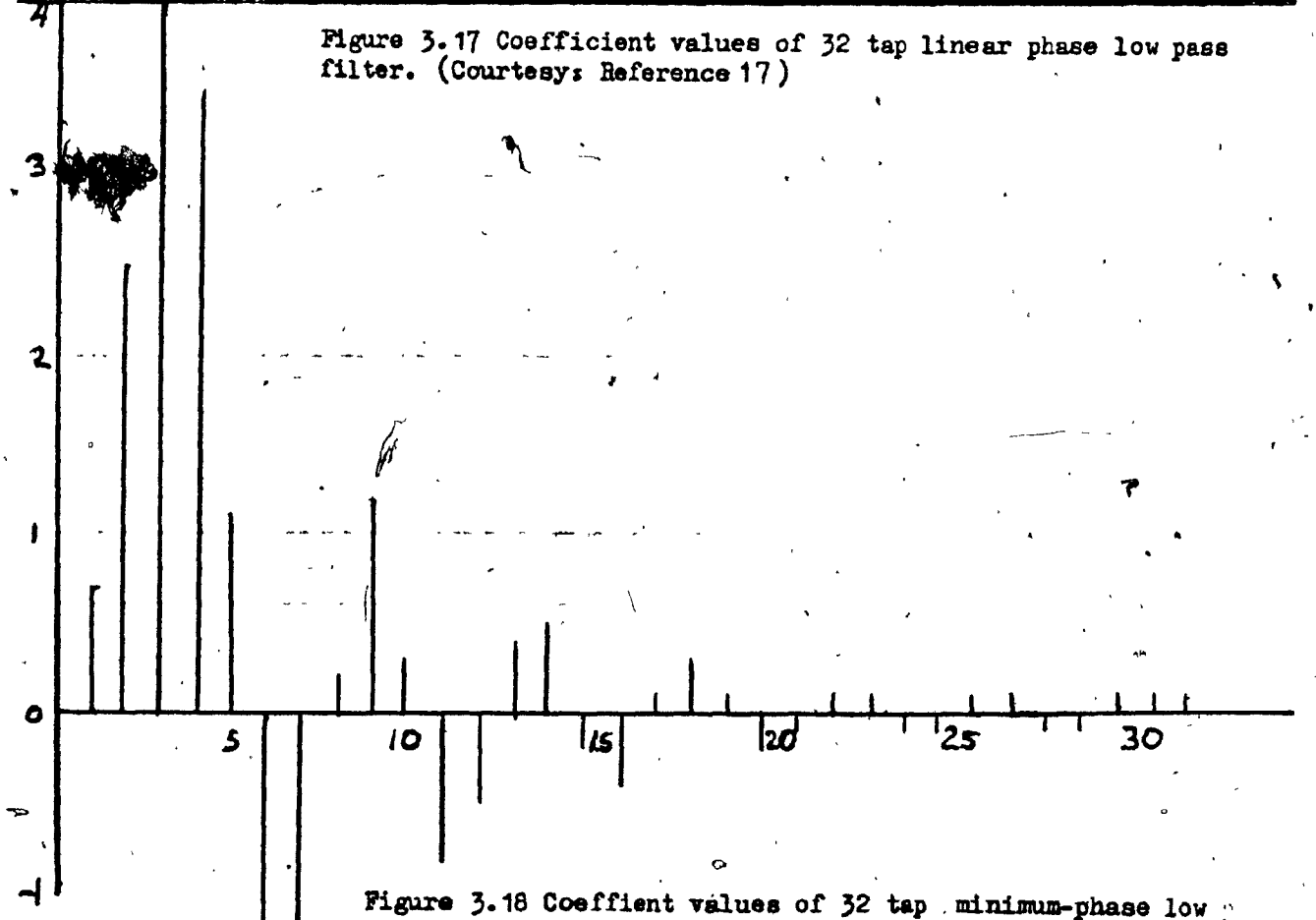


Figure 3.18 Coeffient values of 32 tap minimum-phase low pass filter.(Courtesy:Reference 17).

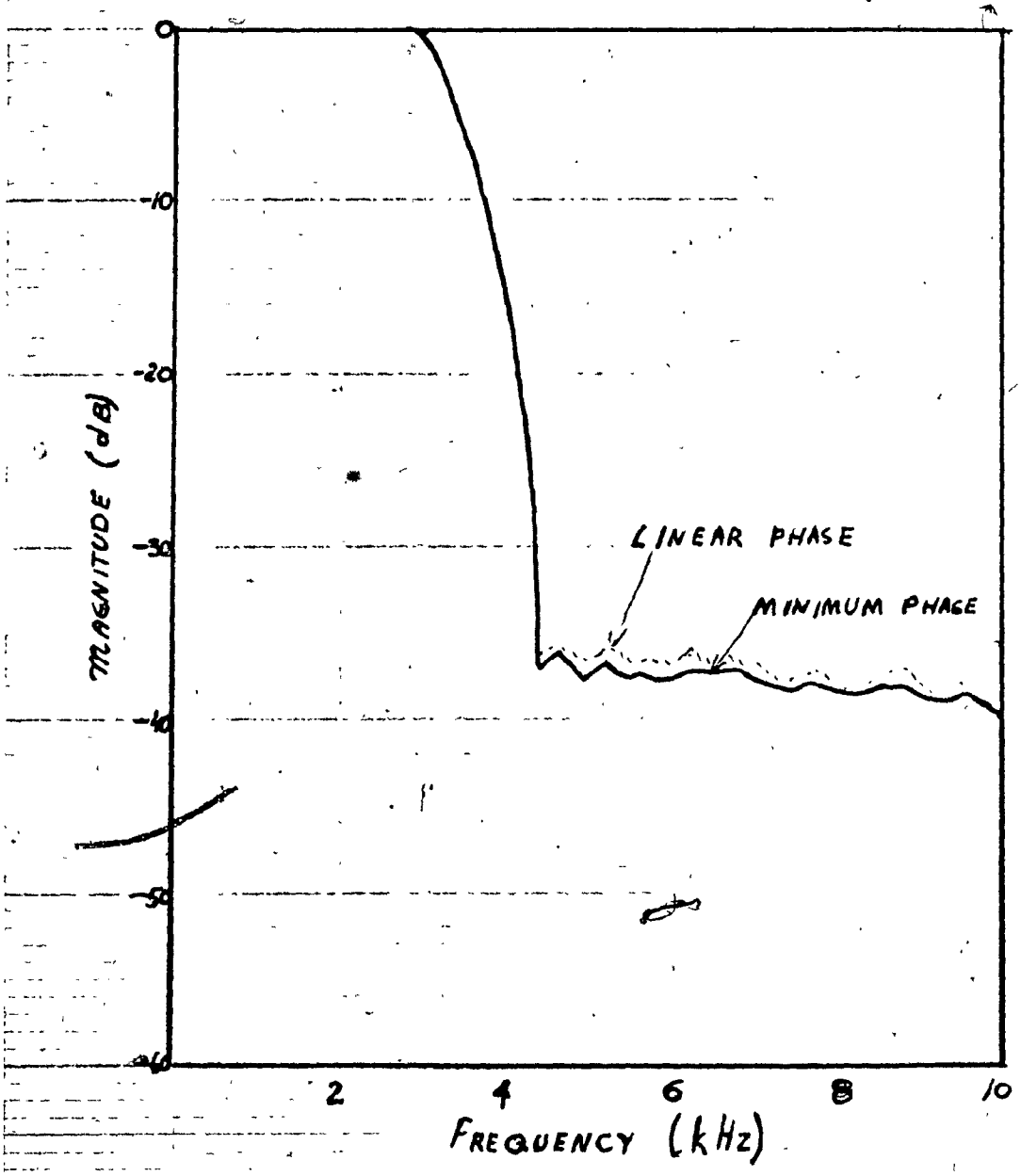


Figure 3.19 Weighting coefficient error on response of a 32 tap low pass filter. (Courtesy: Reference 17)

Therefore, the prefilter is included on the same chip and it is also a transversal filter of a relatively low order. For example, a prefilter required to roll-off between 4 and 28KHZ, for the main filter operating at 32KHZ, can be implemented by a transversal filter of only 6 taps, operating at 64 KHZ. This is shown in Fig. 3.20.

The basic prefilter is a Cosine filter, realized by delaying the input signal and then adding it, to a nondelayed input.[20] The delay used is Tc/2, where Tc = $1/f_o$, clock period. In practice, the signal input is sampled twice with a difference of π-phase between two sampling signals, one sampled signal is delayed by half sampling period and then it is added in phase to other signals.[21]

Let $V_{in}(t)$ be the input signal.

$$V_{1_{in}}(t) = V_{in}(t) \sum_{k=-\infty}^{\infty} \delta(t-kTc) \quad \ldots\ldots\ldots(3.15)$$

$$V_{2_{in}}(t) = V_{in}(t) \sum_{k=-\infty}^{\infty} \delta(t-kTc-\frac{Tc}{2}) \quad \ldots\ldots\ldots(3-16)$$

The output signal is given by

$$V_{out} = V_{1_{in}}(t-\frac{Tc}{2}) + V_{2_{in}}(t) \quad \ldots\ldots\ldots\ldots\ldots(3-17)$$

The spectrum of the output signal is given by,

$$/S(f)/ = \left[2 \sum_{k=-\infty}^{+\infty} E(f-k F_c) \cos\left(\frac{\pi Tcf}{2} - k \frac{\pi}{2}\right)\right] \quad \ldots\ldots(3-18)$$

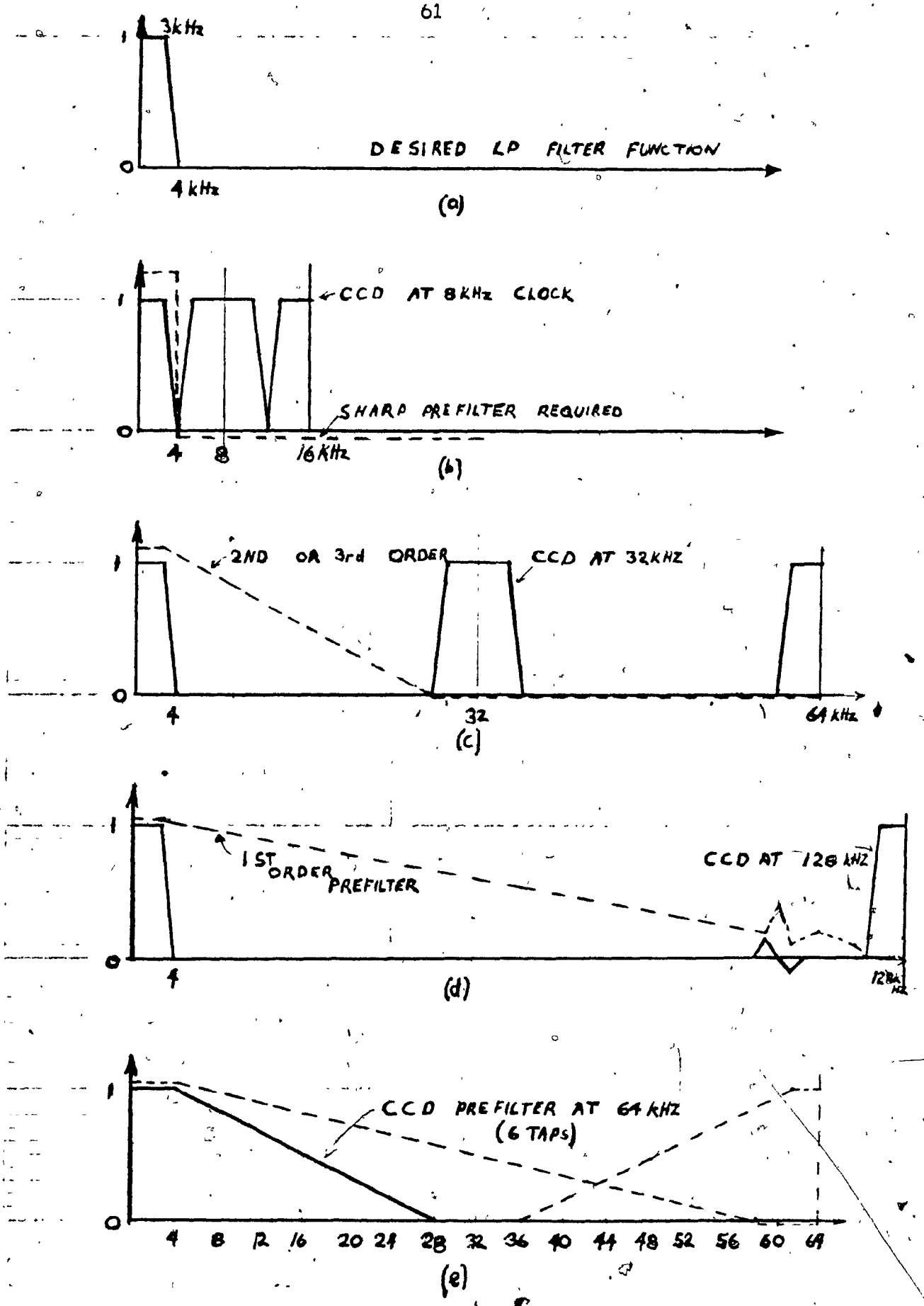


Figure 3.20 Comparison of the prefilter requirements for various operating clock rates of the CCD low pass filter. (Courtesy: Ref. 19)

where E(f) is the spectrum of the input signal.

From the equation (3-18), it is clear that the input spectrum is rendered periodic by the sampling and the different parts of the spectrum can overlap, which is referred to as aliasing. But each alias spectrums for each value of k is multiplied by either a sine or a Cosine function centered at the clock frequency. This being the effect of filtering. This is shown in Fig. 3.21.

Figure 3.22, shows the attenuation obtained with one, two and three stages of prefilt ering. For a two stage prefilter using passband frequency F_b and the clock frequency equal to $8F_b$, the attenuation for the spurious frequencies is more than 28 db and the attenuation for the passband is around 0.3db, which can be tolerated. Increasing the clock frequency to 16 F_b, the attenuation is more than 40 db for the alias components and the passband attenuation decreased to 0.08 db.[20] But as already stated earlier, the clock frequency cannot be increased but must be as low as possible. In this case, the passband attenuation is compensated for in the design of main low-pass filter.

The frequency response of the prefilter and the low-pass filter taken is shown in Fig. 3.23, 3.24 and 3.25.

Magnified view of frequency response of low-pass filter with antialiasing input on these different scales are shown in Fig. 3.26(a), (b) and (c).

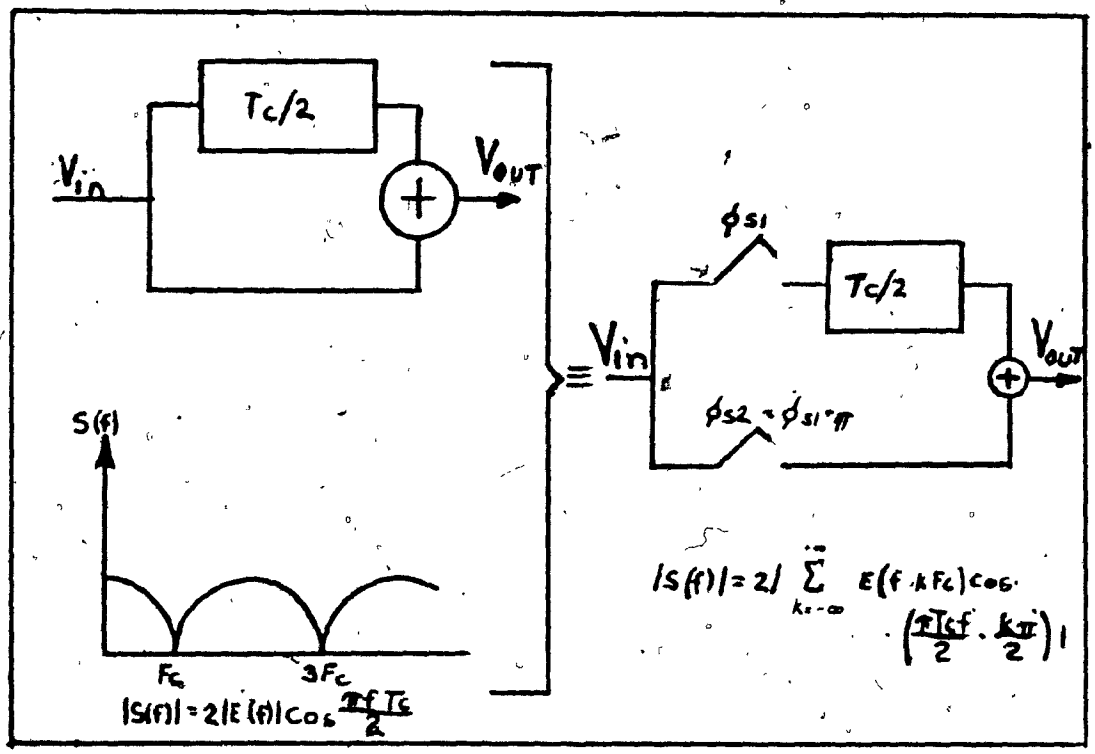


Figure 3-21 Cosinesoidalias prefilter.
(Courtesy: Reference 20)

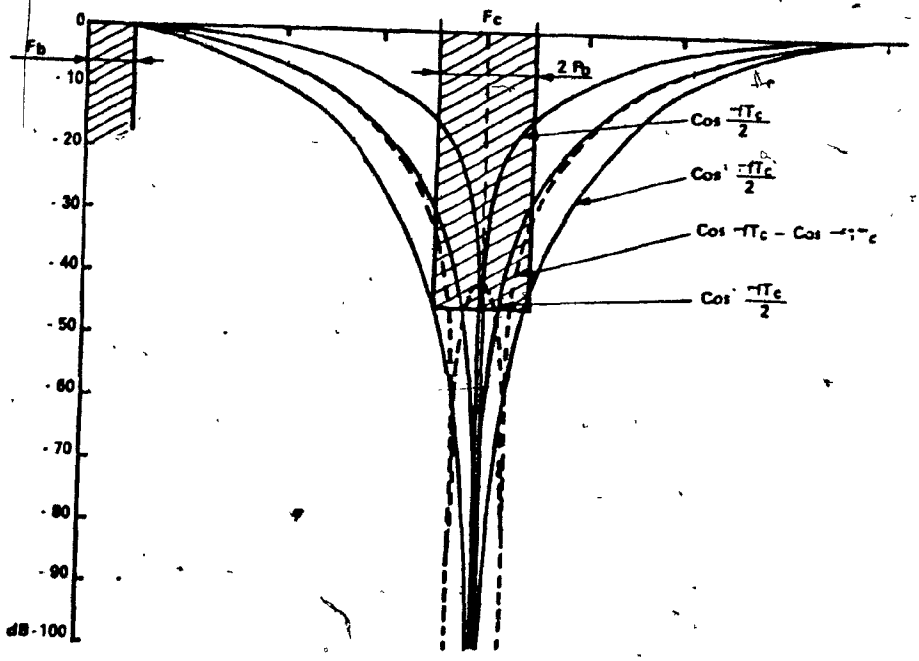


Figure 3.22 Frequency response of cosine prefilter. (Courtesy:Reference 20)

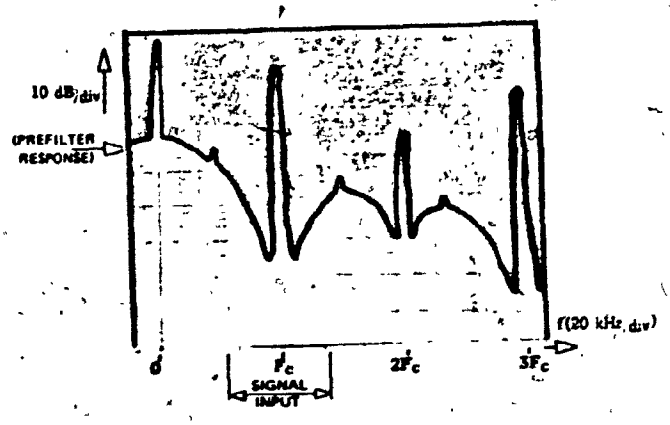
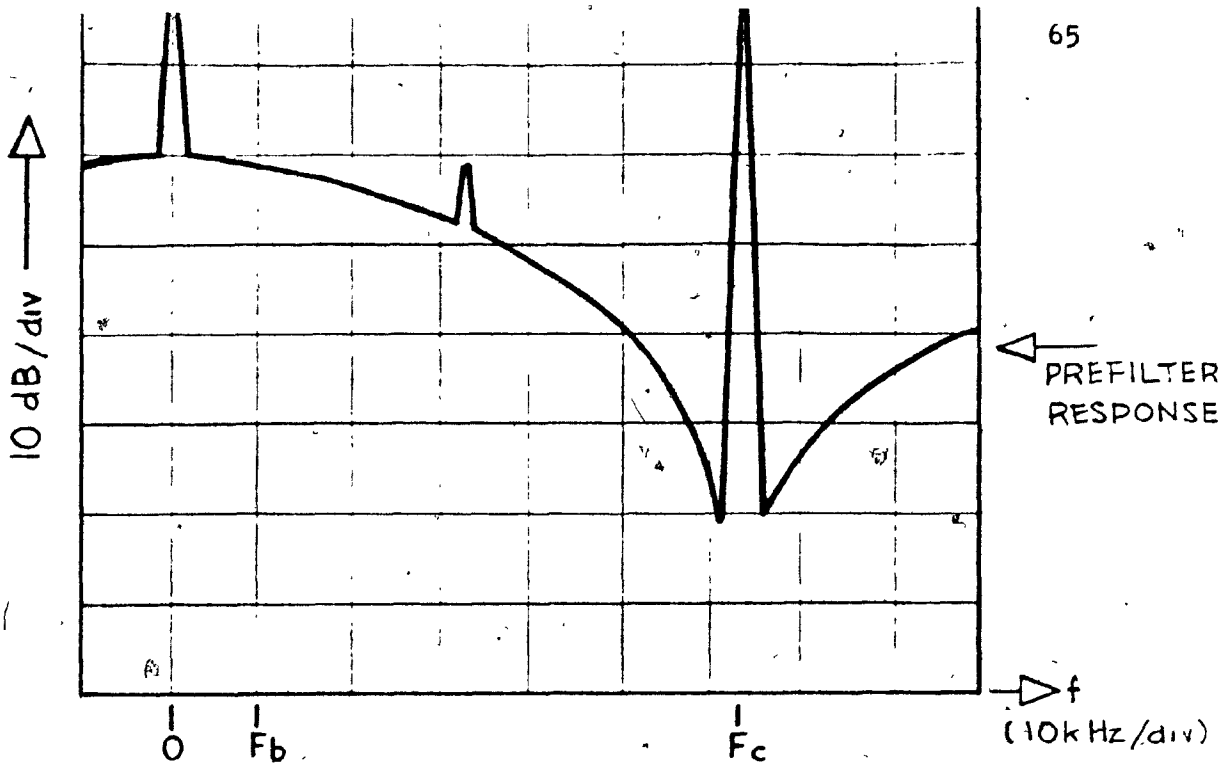
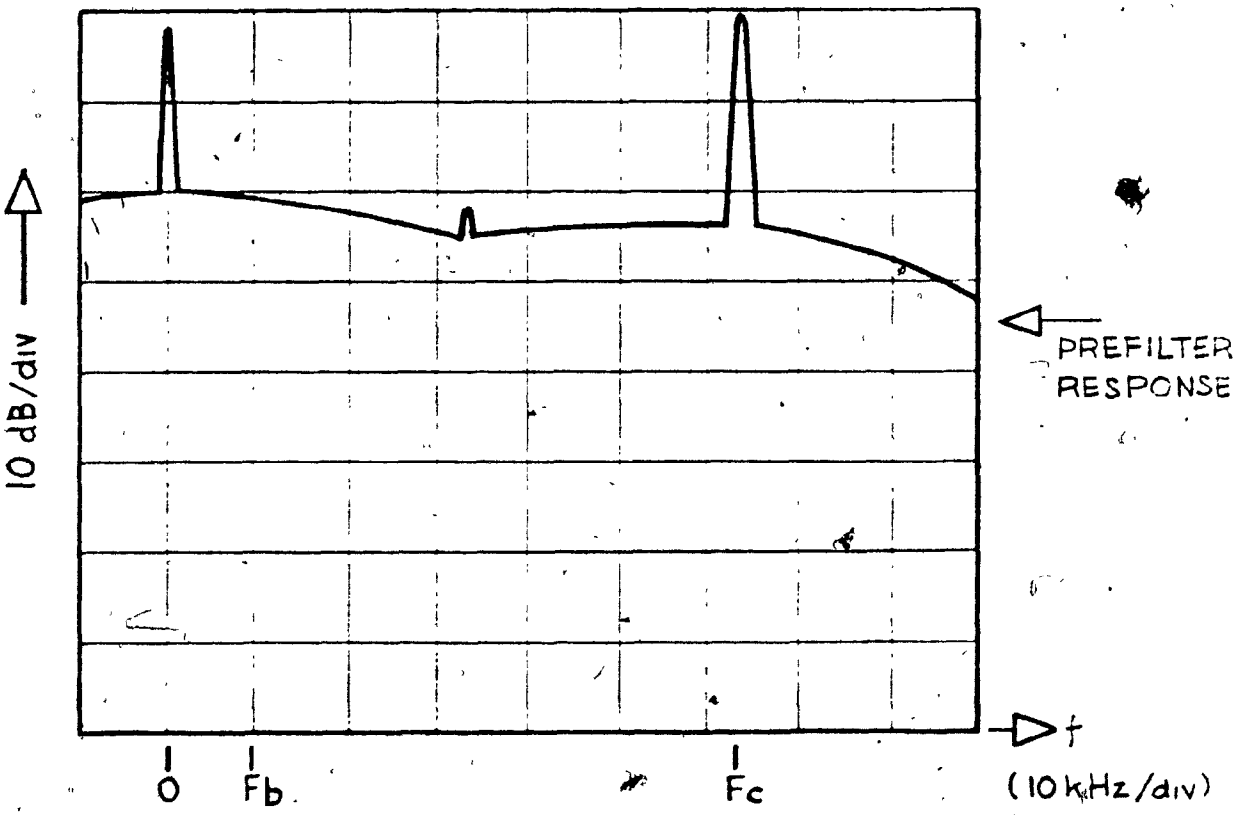


Figure 3.23 Response for an input signal having a bandwidth of 50khz,using a clock frequency of 60khz. (Courtesy:Reference 20)



PREFILTER + LOW PASS CCD FILTER

Figure 3.24



MIDDLE CHANNEL ALONE THE PREFILTER

Figure 3.25 (Courtesy: reference 20)

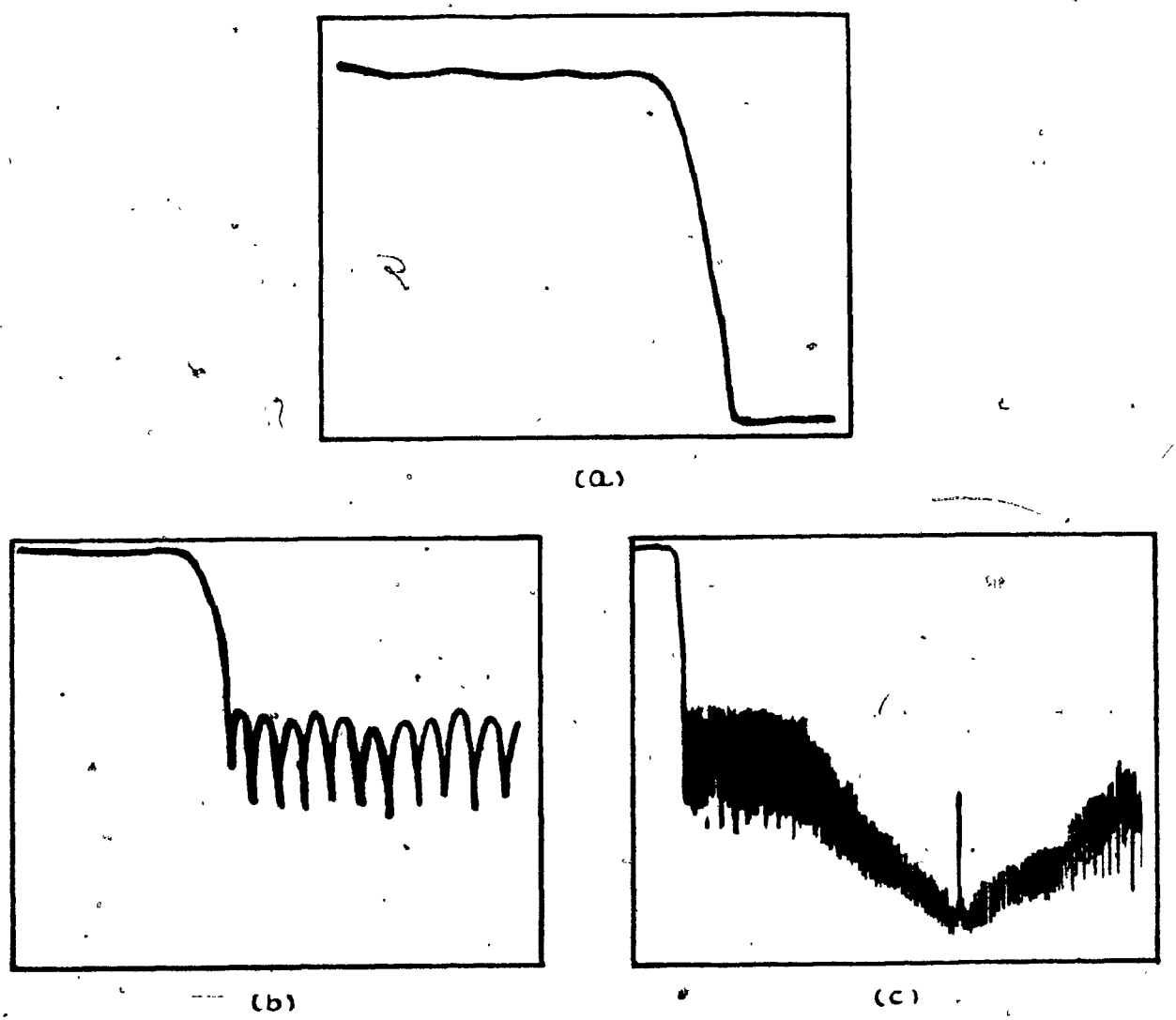


Figure 3.26 Frequency response of the low-pass filter with antialiasing input for different scales.
a) 500 HZ/division. b) 1 KHZ/division c) 5 KHZ/division.
(Courtesy:Reference 19)

CHAPTER IV

TYPES OF ERRORS AND CURES

4-1. Clock Frequency.

Figure (4.1) shows the frequency response of two low-pass transversal filters. The passband and the transition band characteristics are the same, but the stop-band attenuation differs by about 17 dBs. Both the filters have the same number of taps but the clock frequencies are in the ratio of 5:4. Figure (4.2) shows, the calculated impulse response of the two filters. It is evident that the filter having lower clock frequency, has better response. Therefore for good response consideration, a lower clock frequency is preferred.

But the choice of the clock frequency is determined by the analog filter, which preceeds the transversal filter. The analog filter is necessary to prevent assumed signals near the clock frequency into the passband of the transversal filter. Hence if a sharp out-off is used in analog filter, a lower clock frequency for the transversal filter can be used. This implies greater number of components or tolerance for the analog filter and so ends up in higher cost. For example, if a 3-Pole analog filter is used, using one operational amplifier, the usable frequency region extends up to about 1/6th of the clock frequency of the transversal filter. On the other hand, if a 5-Pole

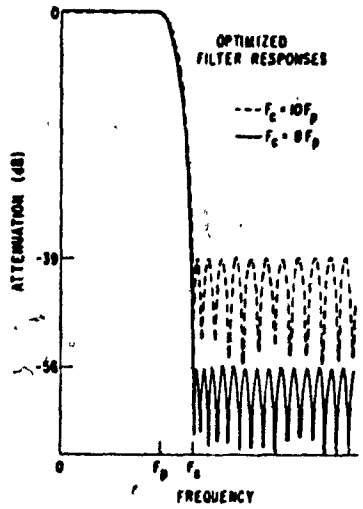


Figure 4.1 Frequency response of two low-pass filters. (Courtesy:Reference 22) 2v

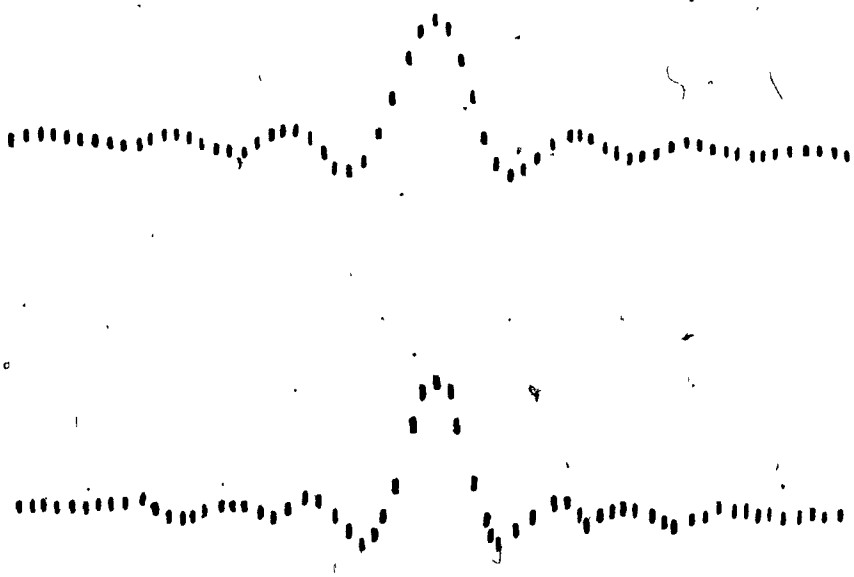


Figure 4.2 Impulse response of the two filters. (Courtesy:Reference 22).

filter is used with an operational amplifier, the usable frequency can be extended up to 1/3 rd the clock frequency.

4-2 Number of Taps.[22]

The duration of the impulse response can be increased and hence the performance of the filter by increasing the number of taps of the transversal filter. The tap-weights of an ideal low-pass transversal filter is given by

$$W_n = \frac{\sin 2\pi n \, Fp/Fc}{2\pi n \, Fp/Fc} \qquad \text{.....(4-1)}$$

$$-\infty < n < \infty \ .$$

when n = number of taps;

F_p = Passband frequency;

F_c = Cut-off frequency;

W_n = Tap weights.

In practice, two aspects of the CCD device limit, the smallest tap weight that can be realized and hence the length of the transversal filter. First of all, tap weights less than one half has to be rounded off to zero. This means that if the tap weight calculated by using equation (4-1) is $4\frac{1}{2}$, the tap weight in practice has to be rounded off to 4. Secondly, the device fabrication process variations, result in random tap weight errors and this puts a limition on tap size. For example,

the process variation can be nonuniform etching.

4-3. CHIP AREA

The tap errors can also be reduced, by suitably increasing the chip area of a single CCD element. By increasing the chip area, increases the cost of the device, decreases the yield and increases the capacitance of the electrode. The capacitance of the electrode increases, as the area is directly proportional to the area of the chip. [23]

Increasing the chip size, produces nonuniformity in the charge density. As a result, the charge will not be split into correct proportions, when it is transferred to the next stage. Transversal filters using thick oxide at the electrode split will be limited by this error. The error is also severe, when the impulse response changes from one stage to the next stage or in high frequency operation. The error is shown in Fig. 4.3 .

The time constant for lateral equilibrium is given by

$$T = (W^2/\mu)\ (V_{app} - V_t) \qquad \text{.....(4-2)}$$

where μ is the mobility factor;

V_{app} is the electrode voltage;

V_t is the threshold voltage;

W is the longest distance over which lateral

equilibrium occurs.

For example, if W = 10 MILS;

$T = 3 \times 10^{-7}$ seconds for P-type and

$T = 1 \times 10^{-7}$ seconds for N-type Semi Conductor.

4-4. TAP WEIGHT TOLERANCE.[24]

The tap weight precision is limited by the tap weight quantization and device process parameters. Generally, one designs a transversal filter with a given set of parameters and scales the maximum value of tap weight by the mask construction and truncation. When this is completed, the impulse response obtained may not meet the stop band specification, even though it is an ideal design.

The tap weight accuracy can be improved by using the dynamic range of tap weights. For example, a high pass filter can be realized as a low-pass filter in parallel with a unity gain paths. The two outputs are subtracted to yield the high pass filter output. The advantage of this scheme is that a low-pass filter with a correct tap weight is used as a high pass filter, when the clock frequency is short. As large tap weights are used for a given filter, fewer levels of quantization are available for tap weights. Figure (4.4), shows the effect of quantization to 1 part in 600 of two optimum low-pass filters. Figure (4.5) shows the effect of quantization

on the high pass analog to the low-pass filter with Fc= 8Fp. The stopband attenuation of low-pass filter degrades from 56 to 47 dB. The quantization reduces the stopband rejection of the high pass filter to 36 dBs.

The effect of random tap weight errors have been analyzed using Monte Carlo technique.[14] This technique was used on a low-pass transversal filter designed as per the optimization procedure described by Parks and McClellan.[25]

Monte Carlo technique gave the equation for the random error as follows:-

$$\Delta_n = T_{OL} * MAX\ W_n * RN \quad \ldots\ldots\ldots \quad (4\text{-}3)$$

where

Max Wn = maximum Tap weight;

T_{OL} = Tolerance;

RN = Random number uniformly distributed from +1 to -1.

This error was added to each tap weight. The curve in Fig. 4.6 , gives the stop band attenuation against Tap weight tolerance. The transversal filters with more than 31 taps fail to improve, the out-of-band rejection, if their tolerance is more than 1%.

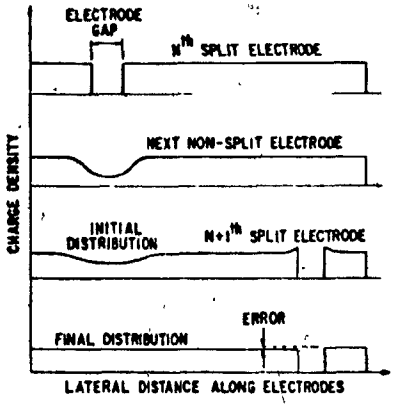


Figure 4.3 Error due to increasing chip size. (Courtesy:Reference 22)

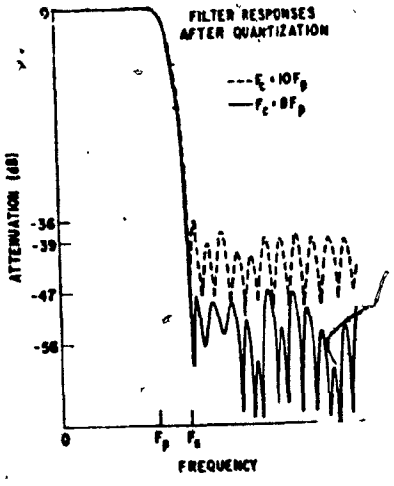


Figure 4.4 Filter response after quantization. (Courtesy:Reference 22)

Increasing the number of taps to about 63, improves the performance, and a tap tolerance of about 0.1% can be tolerated.

Transversal filters with taps 31, 47 and 63 were selected with normalized passband cutoff equal to 0.125. The stop band cut-off was set at 0.175 and the ratio of passband to stopband ripple was set at 5. By adding random errors to each of the filters, responses were calculated. This gave that increased tap weight accuracy was required in the case of longer filters, which meant smaller random errors.

The combined effects of quantization and random errors are shown in figures (4.7) and (4.8) respectively.

Figure (4.7) shows the expected values of peak pass band ripples against random tap weight error tolerance, with and without tap weight quantization. Figure (4.8) shows minimum stopband attenuation together with its variance against tap weight tolerance. Results show that for a transversal filter designed for 63 tap, a random tap weight error of 0.1 to 0.3% can be tolerated.

In addition to random tap weight errors, correlated errors may also appear.[26] For example, a mask misalignment can reproduce constant errors being added to all the taps.

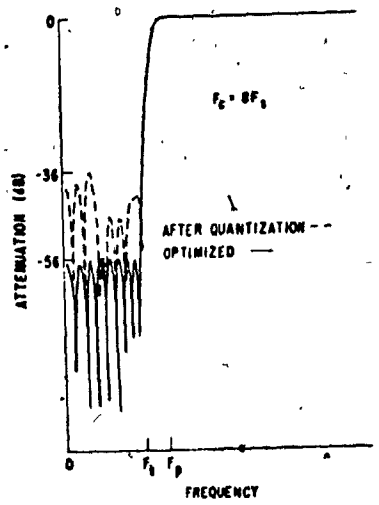


Figure 4.5 Response of high-pass analog of low-pass filter. (Courtesy: Reference 22)

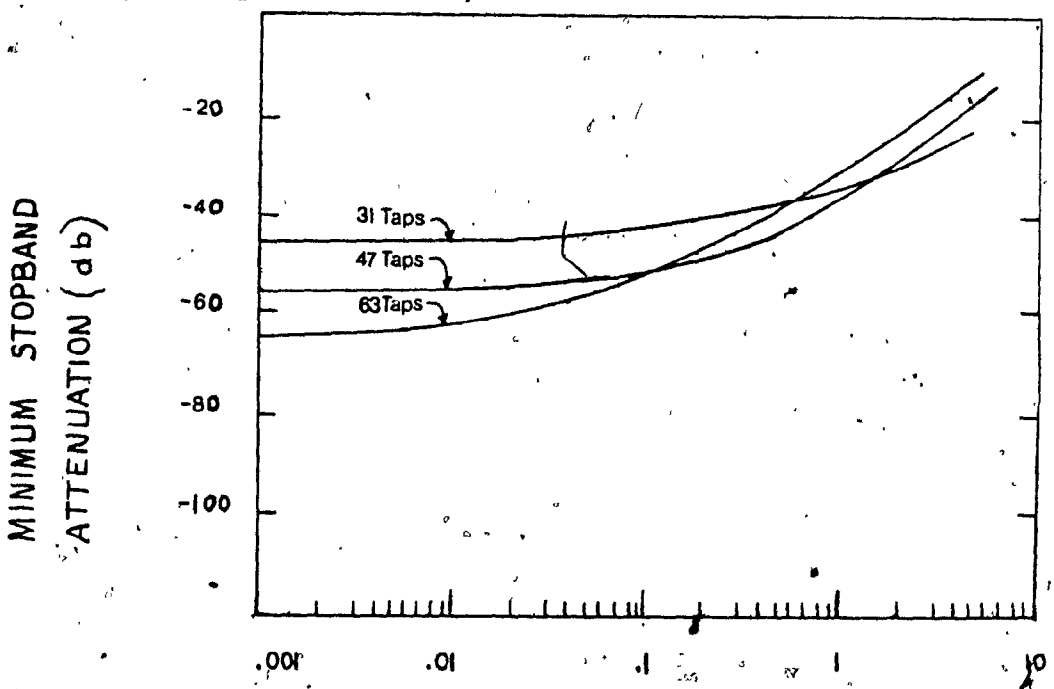


Figure 4.6 Stopband attenuation versus tap weight tolerance. (Courtesy: Reference 26)

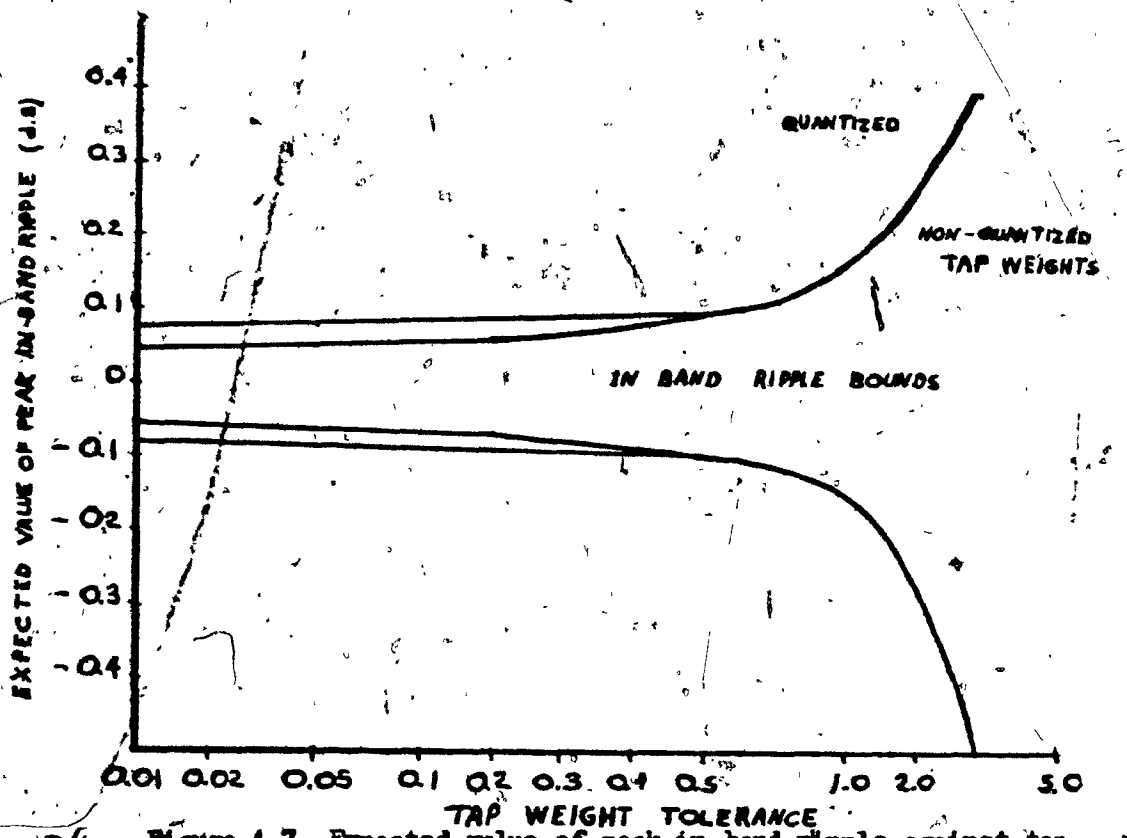


Figure 4-7 Expected value of peak in-band ripple against tap weight tolerance. (Courtesy Reference 22)

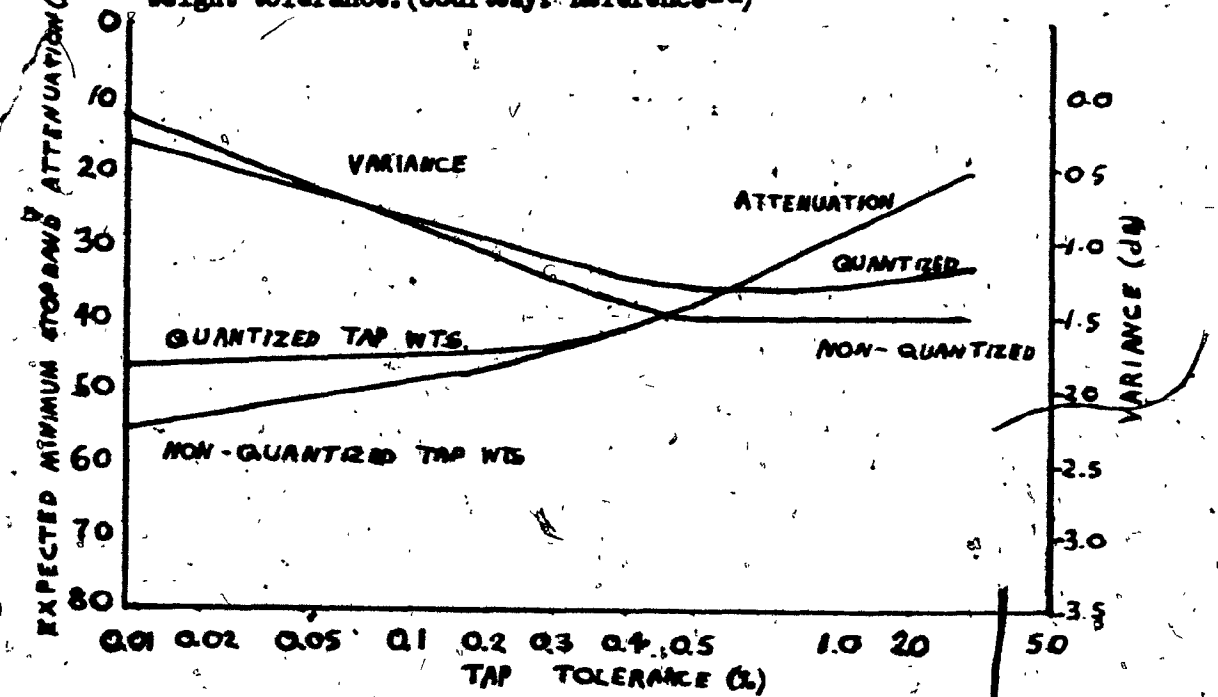


Figure 4-8 Expected minimum stopband attenuation against tap weight tolerance. (Courtesy Reference 22)

Consider the frequency response of an N-tap transversal filter, which is given by,

$$W_N(f) = \sum_{n=\frac{N-1}{2}}^{\frac{N-1}{2}} W_n \exp(-2\pi jnf\,T) \quad \ldots\ldots\ldots(4-4)$$

When T is the delay between taps.

Adding a constant error say "δ" to all of the taps, the frequency response of the equation (4-4) can be written as follows:-

$$W_N'(f) = W_N(f) + \delta \sum_{n=\frac{N-1}{2}}^{\frac{N-1}{2}} \exp(-2\pi njfT) \quad \ldots\ldots\ldots(4-5)$$

In order to evaluate the d.c. error, put f = 0 in equation (4-5).

$$W_N'(0) - W_N(0) = N\delta \quad \ldots\ldots\ldots\ldots\ldots(4-6)$$

This equation (4-6) clearly shows, that as the number of taps are increased, the size of the error component, also increases in proportion. Slow changes in tap weight affect low frequency response and rapid changes in tap weight affect high frequency response.

Tap weight errors can effect phase characteristics as well as amplitude characteristics. Consider an ideal transversal filter, wherein tap weight are symmetric with respect to center tap. This means that $W_N = W_{-N}$. The tap weight errors added are divided into two sets namely symmetric set δ_n^S, and asymmetric set δ_n^a, wherein $\delta_n^S = \delta_{-n}^a$.

The equation (4-4), the frequency response of the transversal filter can be written as follows:-

$$W_N^1(f) = \sum_{n=-\frac{N-1}{2}}^{\frac{N-1}{2}} W_n \cos 2\pi n fT + \sum_{n=-\frac{N-1}{2}}^{\frac{N-1}{2}} \delta_n^S \cos 2\pi nfT$$

$$- j \sum_{n=-N-1/2}^{\frac{N-1}{2}} \delta_n^a \sin 2\pi nfT \qquad \ldots\ldots(4-7)$$

The response can be considered in two ways, namely the real part of equation (4-7) are symmetric errors which affect amplitude only, whereas the imaginary part of equation (4-7), containing asymmetric errors affects phase characteristics.

4 - 5. Experimental Results

Two low-pass filters were fabricated. In both of the filters, 63 taps were used.

Filter A:- $F_p/Fc = 0.1$;

$F_s/F_c = 0.131$;

$\delta_1/\delta_2 = 1$;

Filter B:- $Fp/Fc = 0.1238$;

$Fs/Fc = 0.165$;

$\delta_1/\delta_2 = 5$;

where F_p = Passband frequency;

F_s = Stop band frequency;

F_c = Cut off frequency;

δ_1 = amplitude of passband ripple;

δ_2 = amplitude of stopband ripple;

The filters were designed to meet the following specifications:-

Passband ripple from 0 to 3KHZ to be less than $\pm$ 0.1dB.

Attenuation beyond 4.6 KHZ 32 dB.

A photomicrograph of filter A is shown in Fig. (4-9).

Making use of equation (4-4), the frequency response of the filter was evaluated. Figures (4.10) and (4.11) show the calculated and observed filter response. Figures (4.12) and (4.13) show the calculated and observed response of stopband and passband attenuation.

Figure 4.9 Photomicrograph of low pass transversal filter. (Courtesy:Reference 22)

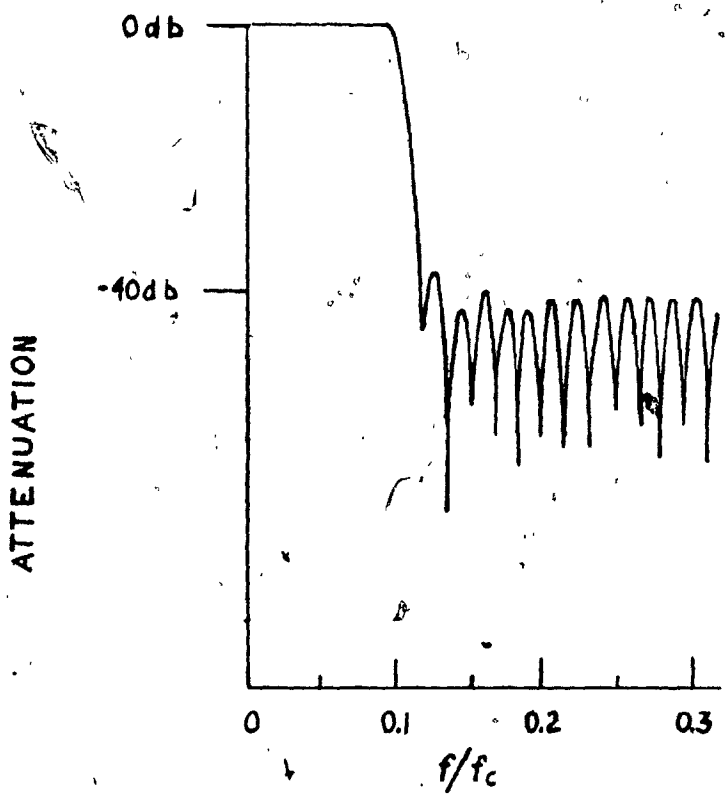


Figure 4.10 CALCULATED FILTER RESPONSE

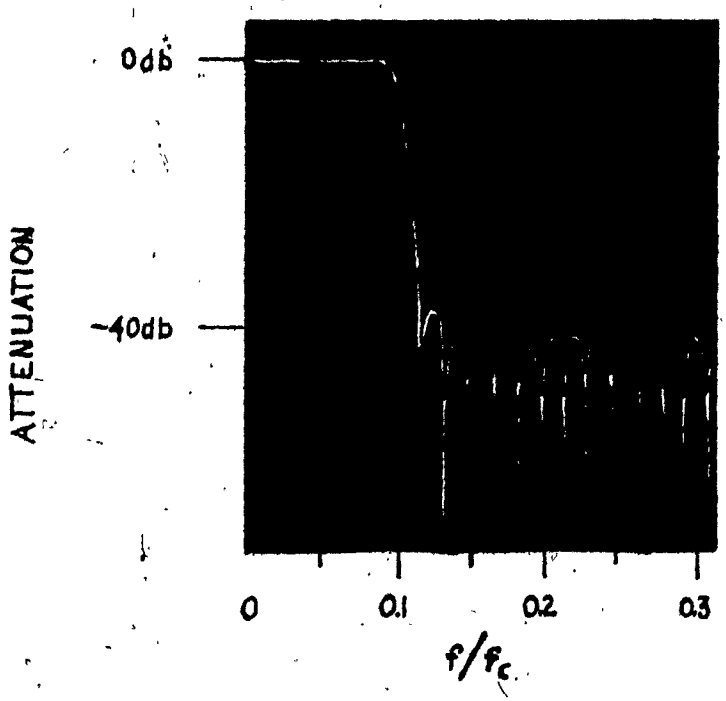


Figure 4.11 OBSERVED FILTER RESPONSE

(Figure courtesy of reference 22)

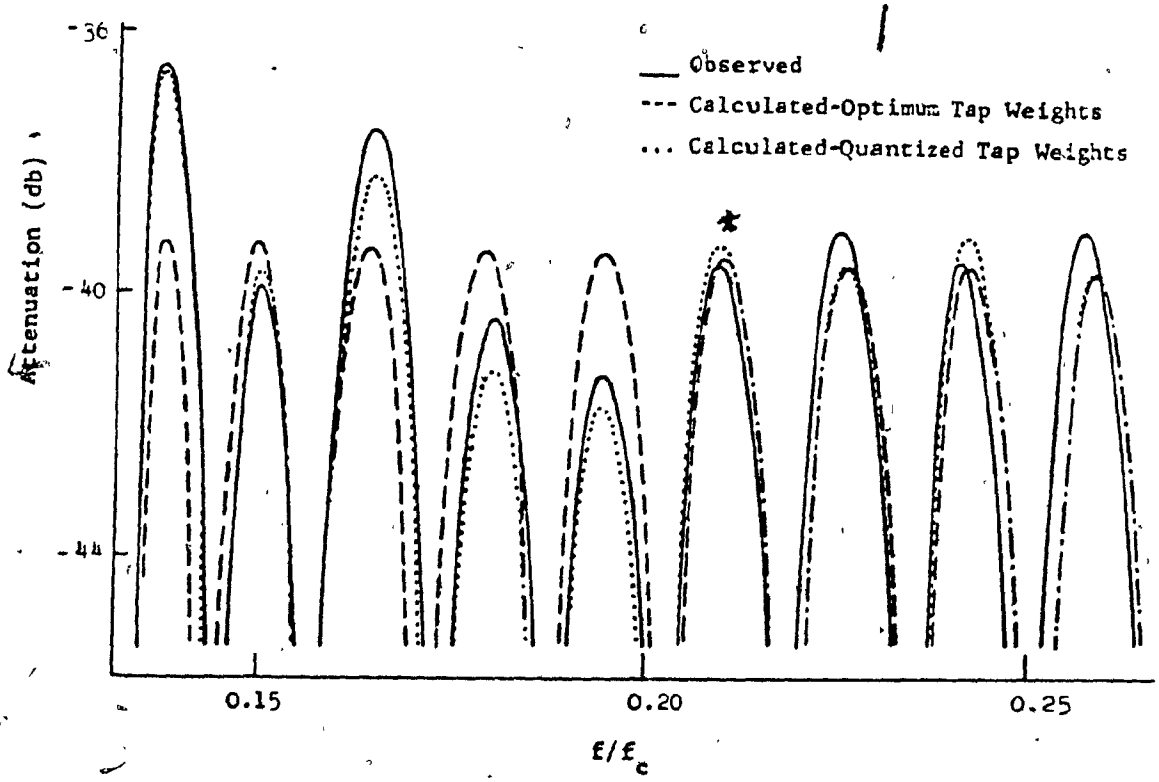


Figure 4.12 Stopband Frequency Response

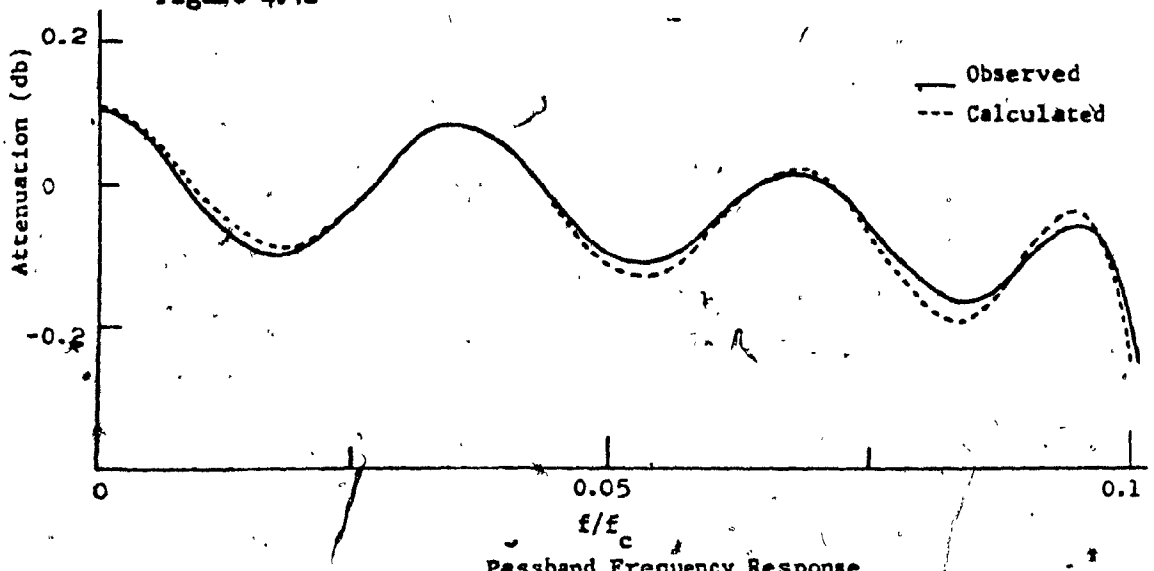


Figure 4.13 Passband Frequency Response

(Figures, courtesy of reference 22)

In Fig. 4.12 when the responses are close between the calculated and observed values, the tap weight error can be 1 part in 1000. In Fig. (4.13), the close proximity between the calculated and observed values of passband attenuation show a tap weight accuracy of 0.1%.

Figure (4.14) shows calculated and observed passband frequency response due to mask misalignment. The close proximity indicates, a 0.3% mask misalignment.

Figure 4.15 shows the low frequency filter response for filter B. The stopband attenuation is in the range - 42 to - 45 dB. The tap weight tolerance was in the range of 0.1 to 0.3%, which was the same for the filter A.

4-6 Clock frequency and Signal recovery.[22]

The primary considerations in signal recovery are linearity and signal to noise ratio. The output signal of a transversal filter is small. The output signal is the difference between the two split electrodes. As the depletion capacitance depends on the output voltage, an error occurs. This error is known as "Cross-talk error". The error can be offset by clamping the electrode potentials to operational amplifier as shown in Fig. 4.16. This eliminates cross-talk errors but imposes severe restrictions on operational

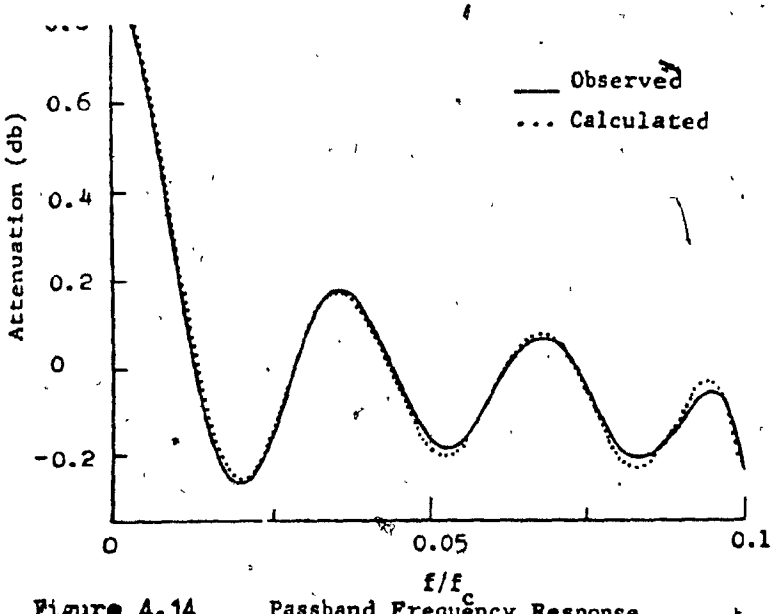


Figure 4.14 Passband Frequency Response —Mask Misalignment (Courtesy:Ref. 22)

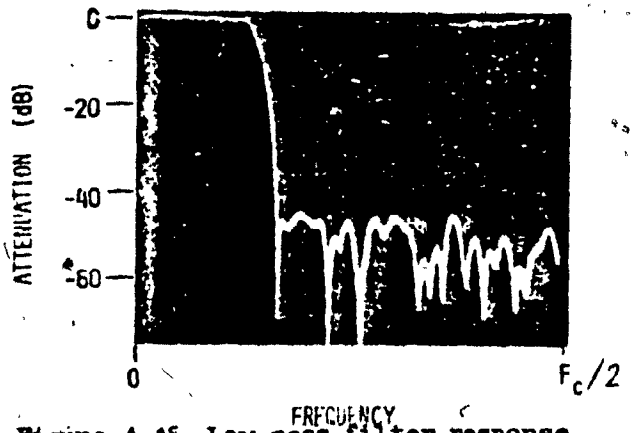


Figure 4.15 Low pass filter response. (Courtesy:Reference 22)

amplifier. The operational amplifier must be a low noise amplifier and must be able to handle dynamic range of full electrode voltage and not difference voltage.

It is preferable to permit a change in electrode potential. In this case a difference operational amplifier is used. The common-mode signal is eliminated and the difference signal is selected.

Figure (4.17) shows an output circuitry that can be used in split-electrode technique. In operation, the reset is closed, discharging the capacitor C_{FB}. After the reset, the transistor opens, thereby the split-electrodes are floating. Hence when signal charge moves under them, their potentials change. As the circuit is symmetrical, two output is equal to the difference between the charges on the split-electrodes. The resistor R is selected so that RC_T = 1/10 of the clock frequency, when C_T is total capacity to ground at the input terminals. As the split-electrodes return to the same voltage after each clock cycle, the circuit is free from cross-talk error.

An alternative circuit to Fig. 4.17 is shown in Fig. 4.18. In this case, the split electrodes are reset by two FET'S. An essential feature of both the circuits is that the feedback around the operational amplifier maintains the electrode voltages at the same potential.

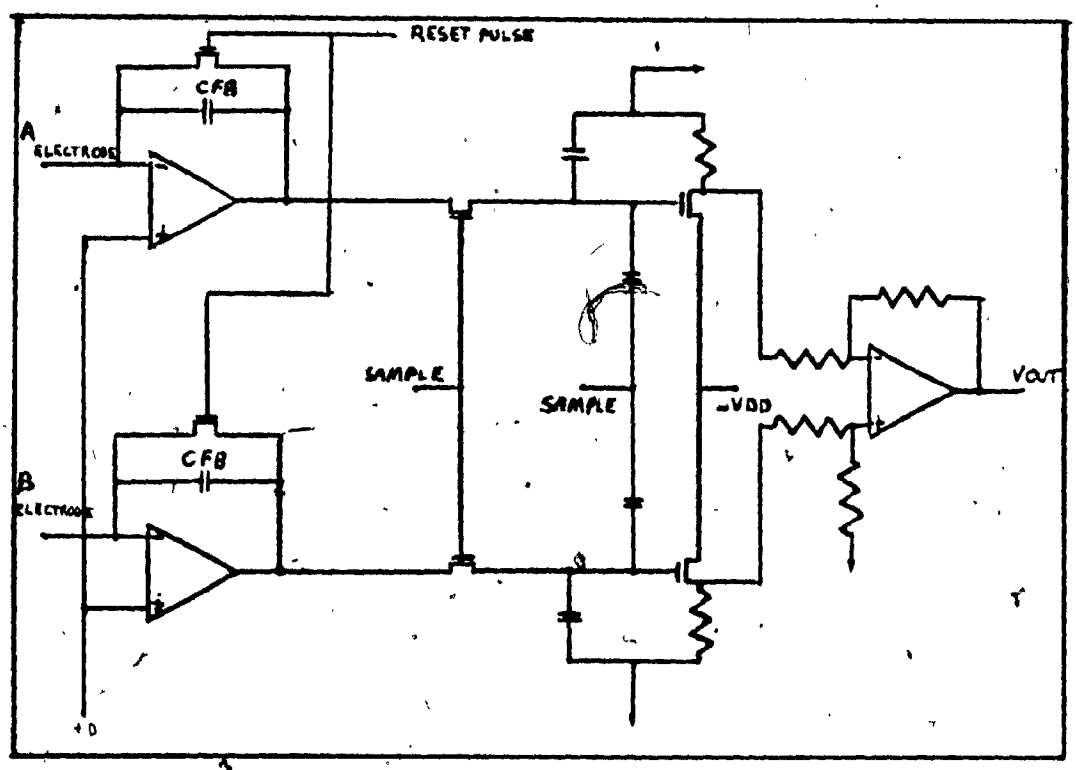


Figure 4-16 Split-electrodes clamped at fixed voltages in order to eliminate cross-talk error.
(Courtesy: Reference 22)

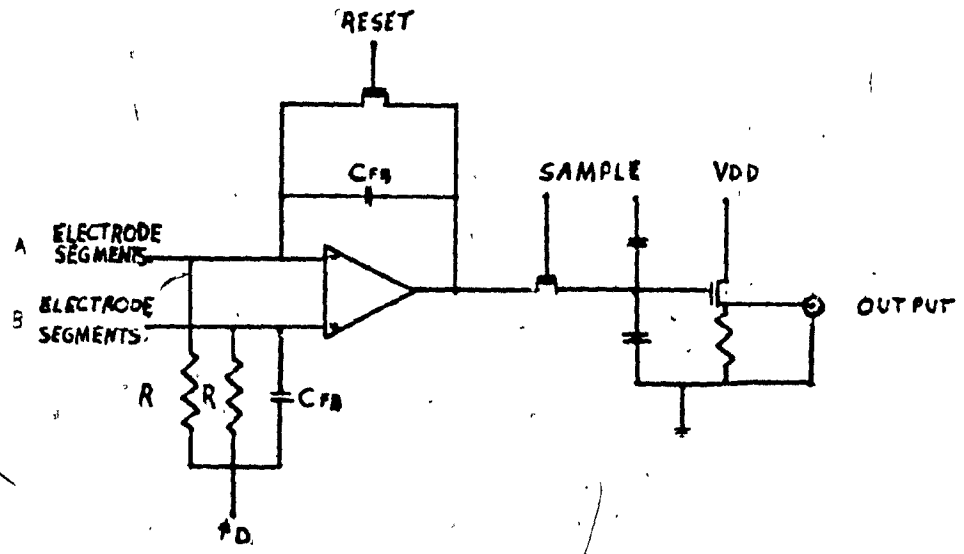


Figure 4-17 Charge-sensitive amplifier, wherein the electrode voltages are reset by the resistors. (Courtesy; Reference 22)

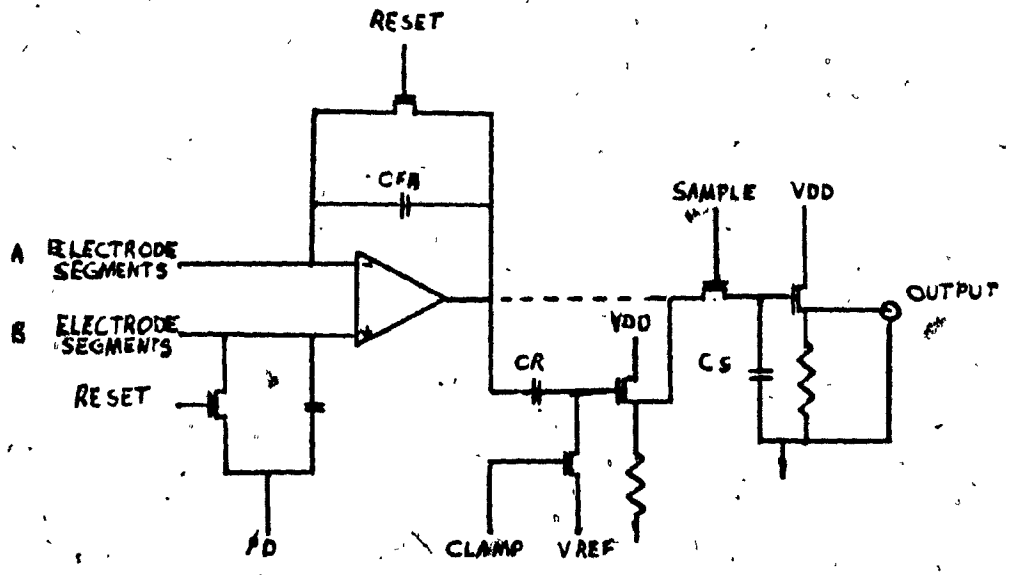


Figure 4-18 Charge-sensitive amplifier, wherein the electrodes are reset by FET. (Courtesy: Reference 22)

equation.

$$Q_R = (1-\alpha)^n \sum_{N=1}^{\infty} \binom{n+N}{N} \alpha^N Q_N \quad \ldots\ldots\ldots(5\text{-}8)$$

when Q_N = Size of the N^{th} charge packed at the input by N clock cycles;

n = Total number of transfers;

α = Coefficient of incomplete charge transfer.

The transfer inefficiency 'ε' can also be compensated.[31] Let h_k be the impulse response of an ideal filter with desired weighting coefficients. Thus the impulse response h_k' required to invert charge transfer loss is given by

$$h_k' = \frac{h_k - \sum_{j=1}^{k-1} h_{k-J}' \binom{K-1}{J} \varepsilon^J (1-\varepsilon)^{K-J}}{(1-\varepsilon)^k} \quad \ldots\ldots\ldots(5\text{-}9)$$

If 'ε', transfer inefficiency of the CCD is known, the weighting coefficients 'h_k'' can be selected to invert the dispersion.[32] This technique for compensating charge transfer loss has been shown.[11] However, this technique cannot always be implemented as the value of 'ε' cannot be predicted accurately. But as CCD processing is standarized, ε can be predicted and compensation is possible in practice.

During the charge transfer as already stated, some charge is invariably left over. This charge left behind joins

the charge in the subsequent packet leading to a delay in charge transfer. For a single stage CCD delay is given by[33]

$$X_{i+1}(1+t1) = \eta\, x_i(t_1) + \varepsilon X_{i+1}(t_1) \quad \ldots\ldots(5\text{-}10)$$

when $X_i(t_1)$ is the charge sample in the i^{th} delay stage at time $t = t_1 T$, when T is the clock period. $\eta = 1-\varepsilon$. The values of ε lie in the range 10^{-3} to 10^{-4}.

Taking the Z - transform of equation (5-10) gives

$$\frac{X_{i+1}\, Z^{-1}}{X_i\, Z^{-1}} = \frac{\eta\, Z^{-1}}{1-\varepsilon Z^{-1}} \quad \ldots\ldots(5\text{-}11)$$

which is CCD transfer function per stage.

The charge transfer ineefficiency in certain applications gives rise to dispersion, which attenuates high frequencies compared to low frequencies. This dispersion can be minimized. by operating the device in parallel. This reduces the transfer rate and also the total number of transfers made by any signal charge.

The Z-transform of a single element delay is given by[34]

$$H(z) = \frac{(1-\varepsilon)\, Z^{-1}}{1-\varepsilon Z^{-1}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5\text{-}12)$$

when $Z = \exp(-2\pi i\, f/fs)$ when fs is sampling frequency.

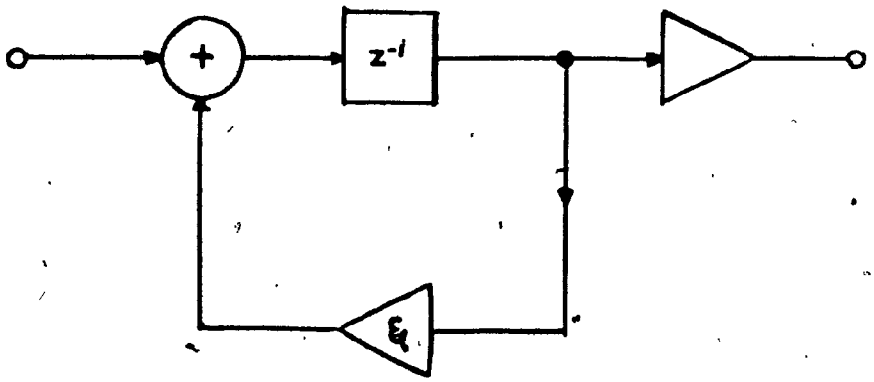


Figure 5.3 Equivalent model for the unit transfer element. (Courtesy: Reference 37)

If 'M' elements are used in parallel and "q' is the clock phase, the transfen function H(Z) in equation (5-12) can be written as follows:-

$$H^M(Z) = \frac{(1-\epsilon)^{M/q} Z^{-M}}{1-\epsilon Z^{-q}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (5\text{-}13)$$

Substituting for $Z = \exp(2\pi i f/f_s)$ and taking the magnitude gives

$$\left| H^M(f) \right| = \exp\left[\frac{M\epsilon}{q} (1-\cos 2\pi q f/fs) \right] \ldots\ldots (5\text{-}14)$$

Observations prove, that parallel operation yields much less dispersion and hence the high frequency response is improved. But this gives rise to fixed pattern noise, which can be eliminated by filtering.

In split-electrode technique,[24] the weighting coefficients h_k are coded into the mask as gaps in electrode structure. For higher accuracy, the channel diffusion can be placed under the gaps making the coefficients insensitive to small photo mask misalignments. The desired electrode length is rounded off to the nearest value. On account of this the actual weight implemented differs from desired weight/ 'h_k' by a random error component 'd_k' which is uniformly distributed over interval $(-\delta, +\delta)$. The value of δ is in the range of 0.002 to 0.01.[14]

5-2 CLOCK RATE

Although CCD transversal filters are operated at clock frequencies in excess of 100 MHZ, practically CCD transveral filters can be operated up to 10 MHZ only. This limitation comes from lack of clock drivers and analog circuits associated with filter output.

The lowest clock frequency depends on the thermal leakage.[35] For an N-Stage CCD operating at a clock frequency 'f_o' should hold charge for a period $T_d = N/f_o$, when T_d is total time delay. Due to thermal leakage, the CCD gradually loses the capacity to hold charge. The potential wells are filled in a storage time 't_s' = 50 seconds at room temperature. The minimum clock rate therefore depends on $T_d \ll t_s$. Delay times $T_d \leq 1$ second is possible at room temperature. The leakage current however increases by a factor of two for each 8°C increase in temperature. Typical value obtained for a 500-stage CCD filter is 25HZ.

Storage time ts:- A heavily conducting transistor has many excess charge carriers moving in the collector region. When the transistor is turned off by the base signal, the collector current does not stop instantaneously, but continues for some time, until all of the excess carriers has been removed by the collector region. The time taken by the transistor in order to remove the excess of carriers at room temperature is called the storage time 't_s' the semi conductor.

5-3. LINEARITY

The major source of nonlinearity arises at the input, when the charge is initially injected.[36] The linearity of charge injection has been studied and the harmonic contents of the input signal measured. Various injection methods have been described in literature elsewhere. using potential equilibrium method with surface channel devices, the signal is applied at the second input gate, whereas the first input gate is held at a constant d.c. bias, all the harmonic components were 40dB below fundamental.

Figure (5.4) and (5.5) show the harmonic components of the potential equilibrium injection method and dynamic injection method.

The linearity can be improved, if the electrodes are allowed to return to the same voltage every clock period after the charge transfer. This can be achieved by turning off one of the electrodes. In this case, the charge below the electrode is independent of the signal charge.[9]

5-4. NOISE

It is difficult to give a detailed account and cures for all types of noises appearing in charge transfer devices. Noise in CCD transversal filters can be divided into two parts

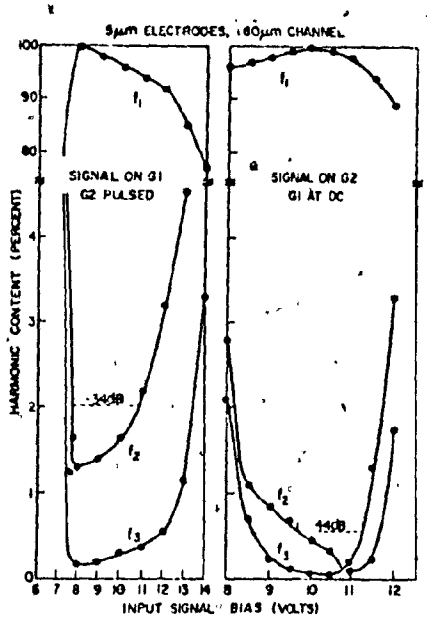


Figure 5.4 Distortion in potential equalibrium method. (Courtesy:Reference 27)

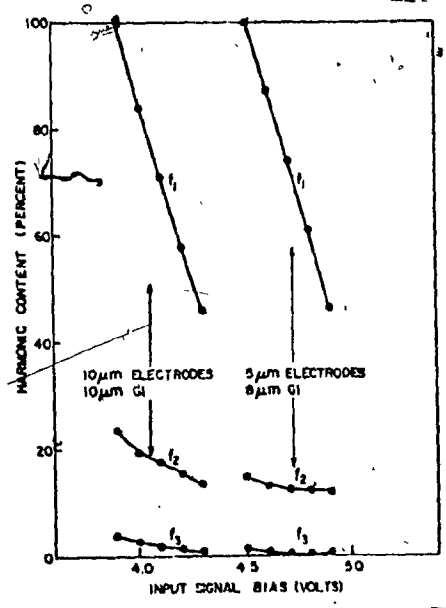


Figure 5.5 Distortion in dynamic injection method. (Courtesy:Reference 27)

namely, noise inherently present with the CCD and noise present in the differential amplifier. Strictly speaking CCD's are low noise devices and as such noise introduced by a CCD is low compared to noise introduced by the differential amplifier. The differential amplifier noise invariably dominates the noise of the CCD, because the differential amplifier noise is introduced after the weighted summation. The split-electrode transversal filter has an insertion loss of 20dBs. Hence the differential amplifier works at a low-input. At low-inputs, the noise itself appears as distortion in the output. This brings down the performance of the transversal filter, unless good design of the differential amplifier is used.

A charge transfer device stores and transfers electrical charges. Noise will be introduced on both of the occasions. Thermal noise will be added during charge transfer and leakage current noise during the storage process. Combined with charge transfer is $X_i(t_i)$, a zero-mean Gaussian noise[37], independent of the process $X_J(t_1)$, when $J \neq i$. As the noise is white, having uniform spectral density, $X_i(t_1)$ is independent from $X_i(t_2)$, for any time periods, t_1 and t_2, when $t_1 \neq t_2$. (White noise is a term applied to a random process, for which the spectral density is uniform for all W[38]). The transfer noise has a spectral density of shape $(1-\cos \pi f/f_o)$, when 'fo' is the clock frequency.

Figure (5.6) shows, the noise spectral densities of transfer and storage processes indicated by 'S_{TP}' and 'S_{SP}'.[39] For a single transfer, for all frequencies, less than the clock frequency, the transfer noise can be neglected. Therefore in signal processing, the signal to noise ratio of signals can greatly be improved by increasing the clock frequency. However, at low frequencies, noise due to charge transfer can be neglected, whereas noise due to storage processes predominates. This proves that for good reproduction of low frequencies, storage process noise has to be kept to a minimum. The lowest frequency that a CCD can faithfully reproduce depends on the delay time being smaller than the storage time. Delay time at present at room temperature is of the order of a second. This puts a limit on the lowest frequency of operation of a CCD and the noise that can be accepted. It can also be noted that the noise due to charge transfer is twice as much as the noise made by charge storage in a CCD. This is because, charge transfer is contributed by two charge packets as opposed to one charge packet in charge storage process.

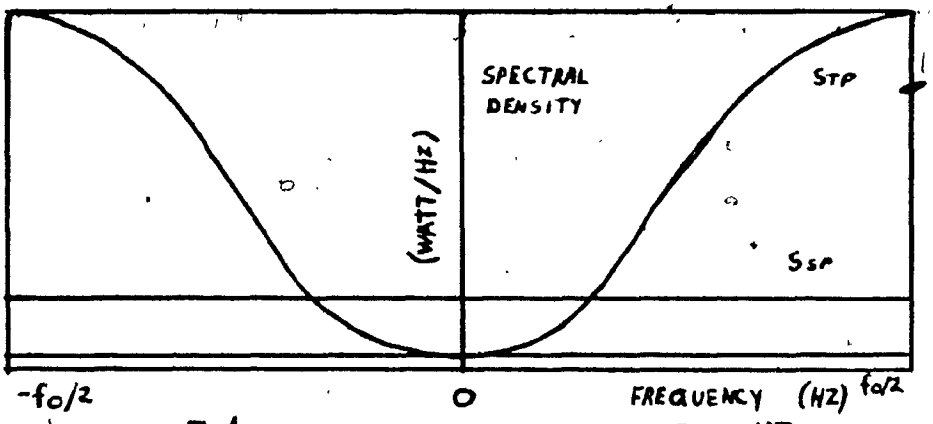


Figure 5.6 - Noise Spectral densities S_{SP} AND S_{TP} plotted against frequency. (Reference 39)

CHAPTER VI

C O N C L U S I O N

The basic concept of a transversal filter and a charge coupled device are explained. Two techniques in implementing CCD transversal filter are covered in detail. Minimum-phase CCD transversal filters used in voice communication as opposed to linear phase design is explained with the help of a low-pass filter. In order to offset the aliasing effect due to clock frequency on the signal frequency, prefiltering requirements of a ~~CCD~~ transversal filter are explained. The errors in implementing CCD transversal filters are covered and cures are suggested whenever possible. Finally, the limitations of the CCD transversal filters are given in detail.

In conclusion, a charge coupled device offers cost advantage compared to any of the existing analogue or digital signal processing due to the following reasons.

(a) No necessity for conversion either from A to D or from D to A, as the signals can be processed in an analogue form.

(b) A single CCD chip performs the function of many digital filters.

(c) Manufacturing process is simple.

(d) CCD's offer temperature stability compared to surface acoustic wave devices.

(e) Can be used at low signal levels and the noise level can be tolerated.

(f) Lower in cost, smaller in size, lighter in weight, lower power and improved reliability over D.F.

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ABBREVIATIONS

$V_{in}(t)$	Input Signal
$V_{out}(t)$	Output Signal
T.	Time delay between taps.
W_n	Tap weight
$X_i(k)$	Charge Sample in the i th delay stage.
$X_i(S)$	Charge sample in the i^{th} delay stage.
t_1, t_2	Time instants.
f_S	Sampling frequency
P	Clock phases
M.N.	Total delay elements
F	Frequency
C_d	Depletion layer Capacitance
C_{ox}	Oxide layer Capacitance
Q_{MAX}	Maximum charge
Q_{fZ}	Fat zero charge
h_K	Impulse response
Q_K^C	Charge under k^{th} electrode at instant 'C'
Q_K^S	Signal charge under K^{th} electrode
Q_K^t	Charge under k^{th} electrode at instant "t"
FET	Field-Effect Transistor
V_G	Gate Voltage