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CHAPTER I

INTRODUCTION

The low-noise satellite communications receiver has evolved as the essential element in defining the performance level of a variety of microwave and millimeter wave systems applications. Generally, the low-noise receiver "front-end" consists of one or more stages of low-noise microwave or millimeter-wave amplification, followed by a hetrodyne frequency converter, the latter translating the received signals to the appropriate frequency range for signal processing. In the last two decades a variety of "building blocks" for low-noise front ends have evolved in the direction of lower noise performance, solid state implementation, smaller size, lighter weight and longer life maintenance-free operation. Some of these, such as the maser, the low-noise travelling-wave tube, and the tunnel diode amplifier are diminishing in importance and currently experience, at best, limited useage, whereas others such as the Gallium Arsenide field-effect transistor (GaAs MESFET) devices are the primary constituents of current and future front ends.[(1)-(4)]. This report concerns the use of GaAs MESFET as a microwave mixer*, suitable for incorporation and improvement of a satellite down converter. And the

* Note 1: In this report we shall only consider the Gallium Arsenide Schottky-barrier gate field effect transistor, the terms GaAs MESFET, GaAs FET and FET are used interchangeably.

possibility of simultaneous low-noise figure, high dynamic range and power gain from a FET mixer, offers an attractive alternative to the conventional tunnel diode amplifier – resistive mixer; as an integrated front-end at microwave frequencies. (Fig 1.1)

The material Gallium Arsenide (GaAs) has been under considerable study by many companies around the world as a practical semi-conductor for many years. Its higher electron mobility (four to five times that of Si) and saturated carrier velocity, offers significant advantages over silicon, especially at microwave frequencies. This intrinsic characteristics result in lower transmit times and resistances, which permit higher gains, lower noise figures and extremely high cutoff frequencies – the ideal material for a microwave MESFET.

This report will briefly discuss some basic semi-conductor physics necessary to understand the operation of the Schottky-barrier FET as a mixer. In Chapter 2, the report discusses the Schottky-barrier (diode) physics. That is to say, the explanation of the potential barrier between a metal and a semiconductor, and the Schottky theory of rectification. Unlike the p-n junction diode, the rectifying contact is based on majority carrier concentration and in high frequency (due to no minority carrier storage) results in more efficient rectification.[5]

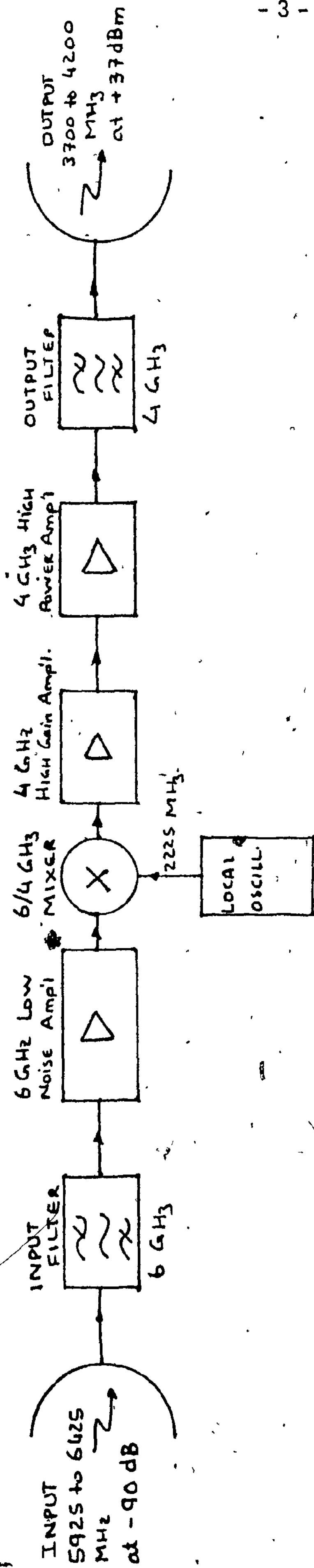


Figure 1.1: Satellite Transponder Block Diagram

This property is then exploited, via various theories like the thermal-field emission, to physically represent an ideal switch needed for mixer diodes. Thus the chapter further develops the diode theories into a Schottky-barrier gate field effect transistor.

The discussion first deals with the choice of GaAs over Si. Then develops the fundamental equation for the FET characteristics from the Poisson's equation, incorporating the effect of the carrier velocity saturation in the channel. A small signal model is developed, which is appropriate for devices where the gate length, Lg, is of the order of a micron, and the field can exceed 3KV/cm, even at low-drain voltages of 3V.

With this discussion of device physics, Chapter 2 concentrates on mixer theory. The basic operation and definition of the 'mixer' and the various terms used, are stated. The theory of resistive mixing acts as the building block to explain fundamental mixer concepts. The theory treats the non-linear mixing device as an ideal switch, and goes on to compare (analytically and mathematically), the similarities between a GaAs Schottky-barrier junction (diode), and an ideal switch. This briefly concerns itself with parasitics and frequency limitation in real devices. Starting from this, the mixing process in a FET is discussed. This adapts the small signal amplifier models, developed in most

of the references [6], and produces a small signal FET mixer model with L.O. pumped into the Gate. Again the effects of device and packaging parasitics is discussed in terms of their frequency limitation. The report goes on to develop the small signal mixer conversion gain equation from the [Y] matrix representation of the device model.

Chapter 3 discusses Design and Construction technics to realize an actual Gate FET mixer. To do this, a basic understanding of microstrip line theory is necessary. Here a planer transmission line consisting of a strip of conductor, separated from a ground plane by a dielectric layer, is defined as the microstrip transmission line. To design a circuit using this, some basic impedance, wavelength and loss equation for a microstrip integrated circuit (MIC) line, are presented.

Also presented are equations for parasitics and edge corrections. The report then presents details of the actual circuit design of a gate injected local oscillator FET mixer.

The actual mixer chosen has

F_{signal} = 6 GHz (5925 MHz to 6425 MHz)

F_{pump} = 2225 MHz = Local Oscillator

F_{output} = 4 GHz (3700 to 4200 MHz)

Again starting from device mixing properties, this section explains exactly how transconductance modulation results from gate pumped local oscillator, and leads to mixing and conversion gain. An actual circuit, results of which are presented in Chapter 4, is described in terms of design details for input diplexing, input and output impedance matches, and bias feed circuits.

Chapter 4, presents the experimental techniques and the test results of a gate injected local oscillator mixer developed by the author, for use in a satellite down-converting receiver. Fundamental motivation in developing a FET mixer was to describe a circuit which had improved performance, compared to the old designs of mixers based on the resistive (Schottky-barrier) diode. The performance is measured in terms of three main parameters. These are the Mixer conversion gain, the Noise figure and the Carrier-to-Intermodulation ratio. The FET conversion gain theory was developed in Chapter 2, and this chapter develops a noise model of the GaAs FET, based on Pucel's work. The references are given at the end of each chapter. However, here the development is complicated and the detailed mixer equations are only briefly presented. The attempt was to concentrate more on physical understanding of the sources of noise and the means to reduce them. The experimental setups for Noise Figure and Gain are presented and

the critical areas of microwave performance measurement are highlighted. The actual test results, based on a 6/4 GHz gate injected L.O. mixer, are from the author's own work, and reflect a state-of-the-art realization of a microwave FET mixer for use in a satellite receiver.

This chapter also presents ideas for further research, including improvements in performance due to (i) reduced gate length for higher frequency of operation; (ii) lower temperature operation, for improvements in noise figure and gain; (iii) variation in circuit-realization, like a drain injected local oscillator, for better conversion gain and spurious performance, and (iv) the use of new materials like InP for its higher efficiency and velocity-field characteristics.

The final chapter presents the conclusion and a comparison of the FET mixer versus the diode mixer.

The Appendices contain information which is relevant to this report, but could not easily be blended into the main text of the other chapters.

Appendix A, presents a brief pictorial essay on photolithographic, micron length gate, MESFET fabrication. Appendix B, presents the NE 244 FET data sheet. This is the device used in the results of Chapter 4. Appendix C presents background information on S-parameter computer aided design techniques. Appendix D is a detailed derivation of the FET mixer noise figure equation,

omitted from Chapter 3. Finally, Appendix E gives the circuit design details for the particular solution of the FET mixer, as presented in Chapter 3.

CHAPTER 2

GALLIUM ARSENIDE METAL - SEMICONDUCTOR FIELD-EFFECT TRANSISTOR (GaAs MESFET)

2.1 Introduction

The intention of this chapter is to discuss the device physics and the FET mixer concept. Field-effect transistor technology is a very dynamic field in microwaves today. This report is a comprehensive review of the literature to discuss the device physics and the starting block is to present the theory of the Schottky barrier itself. This means to discuss the diode, as a non linear mixer device, and then to develop this theory into the MESFET. The GaAs semiconductor material, with majority carrier transport properties, superior to silicon, is the obvious material choice. The minority-carrier lifetime and mobility are of no concern in unipolar transistor. Therefore, materials with optimized transport properties for electron but poor performance for holes can be chosen. Basically current transport in GaAs MESFETs, based on the non-equilibrium velocity-field characteristics, can be summarized as - slow electrons in a constant field region, with energy below the threshold field, remain in equilibrium condition, and as the electrons enter a high-field region, they are accelerated to a higher velocity before relaxing to equilibrium velocity. This overshoot shortens electron transit time through the high-field region. Using this concept, equivalent circuit of the FET, as an amplifier are developed. With the addition of parasitic elements, and the block diagram of a gate pumped mixer, a FET model as a mixer is presented. The fundamentals of resistive mixing are included to help explain the notation used in

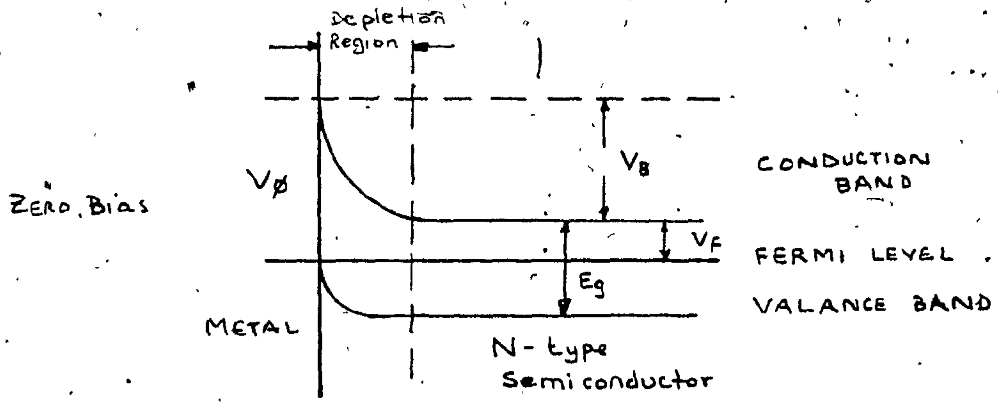
a mixer, and to develop the theory of transconductance modulation by strong LO pumping at the gate Schottky-barrier diode. In summary, mixing occurs in a FET when the small signal elements representing the FET are varied at a periodic rate by a large local oscillator signal impressed between a pair of device terminals, in our case the gate-source terminals. The mixing is a result of the strong gate bias dependence of the transconductance, g_m.

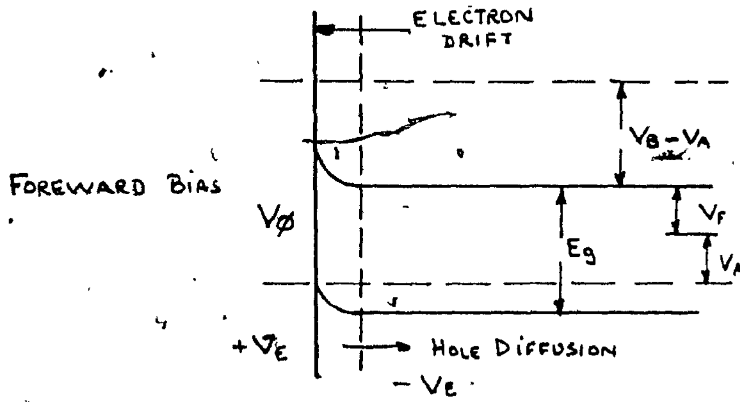
2.2 The Schottky-Barrier (diode) Physics

A mixer is a circuit containing a non-linear element known as the mixer diode, which enables a signal frequency to be converted to another frequency, known as the intermediate frequency (IF). This is achieved by extracting the difference between the signal frequency and that of another oscillator known as the local oscillator (LO). The mixer can be cascaded with an IF amplifier and the complete system is referred to as a hetrodyne receiver.

Semiconductor diodes for microwave applications are based on the phenomena of majority carrier injection across a Schottky type barrier between a metal and semiconductor. The origin of the barrier is due mainly to a combination of the effects of surface states and the metal work function. Such a device is called a Schottky-barrier diode.

The metal semiconductor contact is defined by the Schottky theory of rectification.[1] Unlike the p-n junction diode, the rectifying contact is based on majority carrier conduction and in normal operation exhibits virtually no storage of minority carriers. This results in more efficient rectification at high frequencies. The operation of a metal semiconductor diode can best be understood by referring to its appropriate electron energy diagrams, as shown in Figure 2.1[2]. These show the energies of free electrons in the metal in for example, an n-type semiconductor under various conditions of bias.





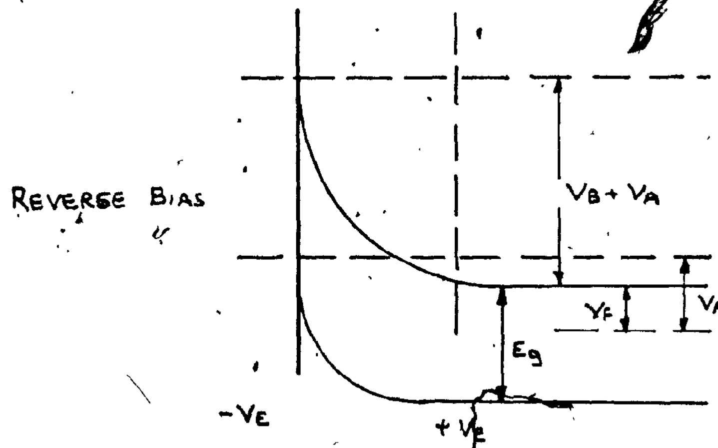


Figure 2.1: Metal – Semiconductor Junction Electron Energy Diagram

Both diffusion and diode theories predict an ideal I-V characteristic of the form: [1]

$$I = I_s (e^{\alpha V} - 1) \quad (2.1)$$

where $\alpha = q / nkT$ (2.2)

Thus, $I = I_s (e^{qV/nkT} - 1)$ (2.3)

where I_s is the saturation current,

q is the electron charge $= 1.6 \times 10^{-19}$ (coulomb.),

T is the absolute temperature (^oK),

k is the Boltzman's constant = 1.38×10^{-23} (joules/^oK)

V is the voltage across the diode junction (volts)

n is termed the ideality factor and should be equal to 1.0 for ideal characteristics.

That is, $\frac{q}{kT} = 40 \text{ (volts)}^{-1}$ (2.4)

This result by Schottky together with Bethe's [3] thermionic emission theory, is combined in a detailed thermionic emission-diffusion theory. The approach is derived from the boundary condition of a thermionic recombination velocity, v_R, near the metal-semiconductor interface. In addition, effects of electron optical-phonon scattering and quantum-mechanical reflection at the metal-semiconductor interface are incorporated. The electron optical-phonon

scattering between the barrier energy maximum and the metal predicts a low-field limit for assuming [4] that the metal acts as a perfect sink for carriers which cross the potential maximum in the direction of the metal, i.e. the thermionic emission theory. The effect of quantum-mechanical reflection and quantum tunneling on the recombination velocity predicts the high-field limit of validity of the thermionic emission theory and the onset of thermionic-field emission. Thus, the Schottky-barrier diode is a majority carrier device under loss-injection conditions, and at sufficiently large foreward bias, the minority-carrier injection ratio (the ratio of minority carrier current to total current) increases with current due to the enhancement of the drift-field component which becomes much larger than the diffusion current. Thus, [1]

$$J = \frac{q N_C v_R}{1 + \frac{v_R}{v_D}} \exp\left[\frac{-q\phi_{Bn}}{kT}\right]\left[\exp\frac{-qV}{kT} - 1\right] \quad (2.5)$$

where q is the electron charge,

N_C is the effective density of states in the conduction band,

v_R is the effective diffusion velocity associated with the transport of electrons from the edge of a depletion layer at W to the potential energy maximum,

$q\phi_{Bn}$ is the barrier height (for Au-GaAs = 0.9 eV).

With this brief introduction to Schottky-barrier contact theory a discussion of parameters sensitive for mixer diodes is possible.

To obtain high performance in terms of low conversion loss and noise figure, it is required to use a diode with a very high cutoff frequency f_{LO}, (to simulate an ideal switch), and to be able to properly terminate the modulation products in the mixer circuit.[5] A criteria involving diode area, material parameters, and temperature, must be considered to extend Schottky-barrier mixer diode range into high frequencies, while keeping low the conversion loss or noise figure of the device. To reduce the parasitic loss as the frequency is increased, the diode area must be reduced.[6] However, this reduction in diode area will increase the intrinsic conversion loss rapidly due to the non-linear contact resistance. Also, a large Richardson Constant extends the usefulness to smaller diameters (higher frequencies), and cooling a thermionic emitting diode will degrade the conversion loss.

The principal factors limiting performance are the barrier capacitance (C_o) and the spreading resistance (R_S) [5]. The former is merely the capacitance of the space charge limited region, and effectively shunts the non-linear diode resistance (R_j). The spreading resistance (R_S) mainly consists of the undepleated portion of the epitaxial layer lying below the junction, and it is thus in series with the parallel combination of C_o and R_j. The deleterious effect of these two

parasitic elements on the conversion efficiency of a Schottky barrier diode are immediately apparent: C_o allows current to bypass R_j, while R_S is a source of power dissipation, heat production, and, consequently, excess diode noise.

A cutoff frequency at which dI/dP, detected current versus incident power is one-half its maximum value is defined as: (1)

$$f_C = \frac{1}{2\pi C_o (R_j R_S)^{\frac{1}{2}}} \tag{2.6}$$

This shows how the high frequency performance of a Schottky-barrier diode can be limited by the presence of the parasitics, such as an increase in diode noise temperature due to I^2R heating of R_S, which is present at all frequencies.

To reduce C_o and R_S certain fundamentals in device fabrication are possible. (6), (7)

(i) Since $C_o \sim r^2$ and $R_S \sim 1/r^2$

where r is the radius of the diode contact area, a reduction of the spreading resistance is possible by choosing a pattern with larger periphery to area ratio compared to that of a dot.

(ii) A very highly doped n^{++} layer to serve as a buffer layer, but more importantly to help minimize the parasitic series resistance in the most critical region, namely in close proximity to the small area Schottky contact where the spreading resistance is located and on the surface of

the back contact where the ohmic contact resistance dominates. Of course, non-epitaxial or bulk GaAs if used could be used so that this effect would not occur. This, however, would cause an increased Co as well as a reduction in the back breakdown voltage. This latter effect could lead to an increase in diode noise due to reverse current flow during negative half of the local oscillator cycle.

2.3 The MESFET Physics

With the introductory information on Schottky barrier physics of the previous section we can now consider the MESFET. The FET (Field Effect Transistor), as the name implies, is a device whose current through it can be varied by an electric field applied to a terminal Basically, there are three types of FETs (see Figure 2.2). These are the Insulated Gate (IGFET), Junction (JFET), and metal semiconductor (MESFET). The main difference is depending on whether the controlling field is applied to a semiconductor reverse biased junction or at an insulating layer. In this report, only the GaAs Metal to Semiconductor field effect transistor (GaAs MESFET) will be analyzed.

The choice for GaAs [8] was based on an ideal semiconductor for a Microwave FET which has simultaneously a large mobility, large maximum drift velocity, and large avalanche breakdown field. Consequently, a small electron effective mass, a large intervalley separation and a large energy gap were required. Devices fabricated on GaAs have performance improvement over Si, because -

(i) In GaAs the conduction electrons have a six times larger mobility and a two times larger peak drift velocity than in Silicon [9]. Therefore, parasitic resistances are smaller, the transconductance is larger, and the transit time of electrons in the high field region is shorter.

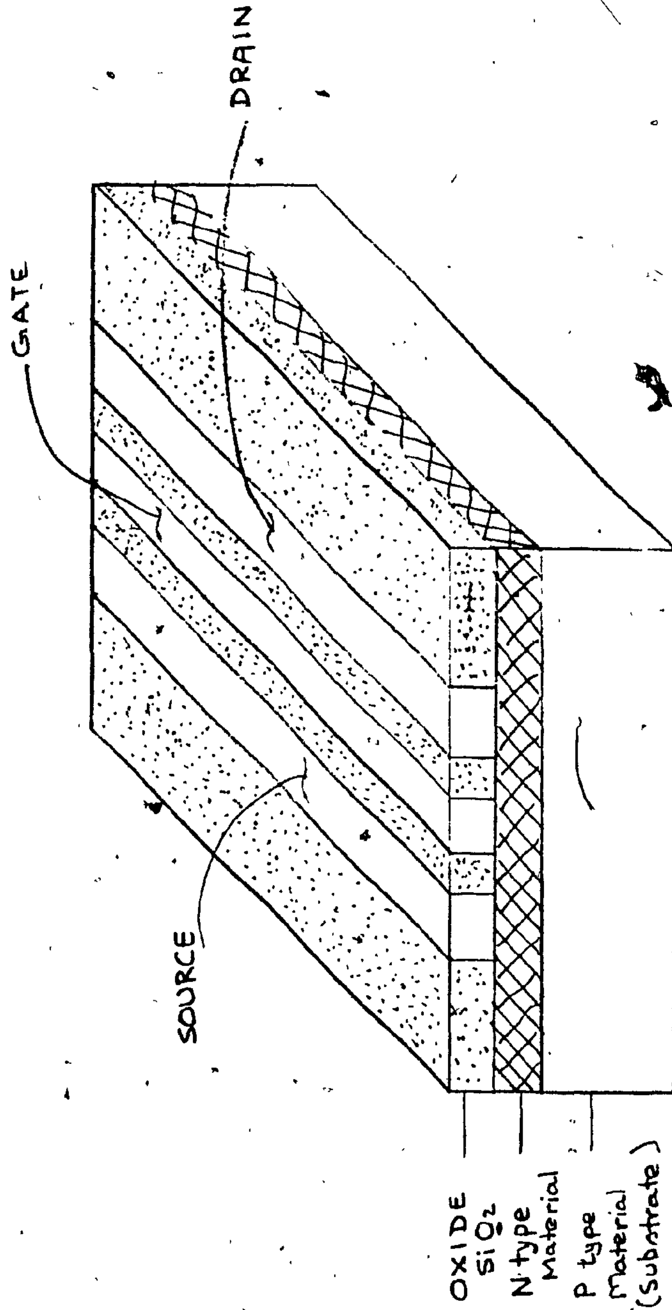


Figure 2.2(a): Junction FET

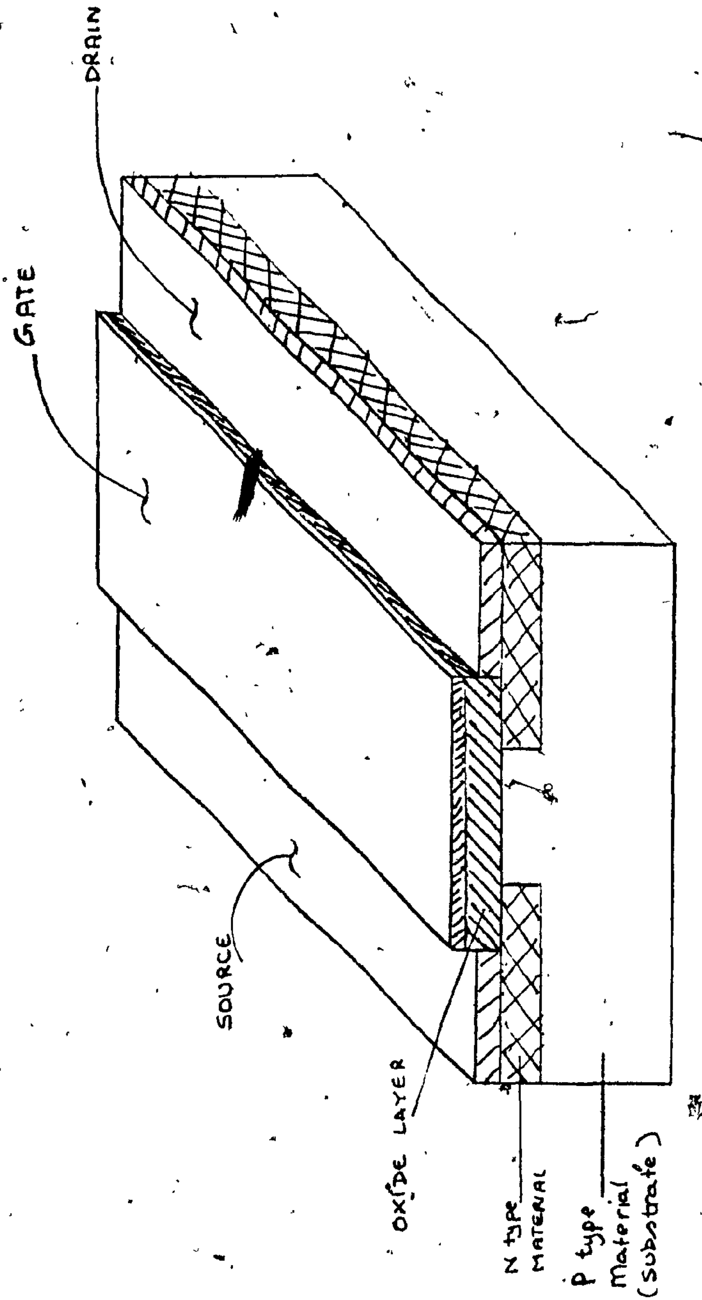


Figure 2.2 (b): Metal Oxide Semiconductor FET

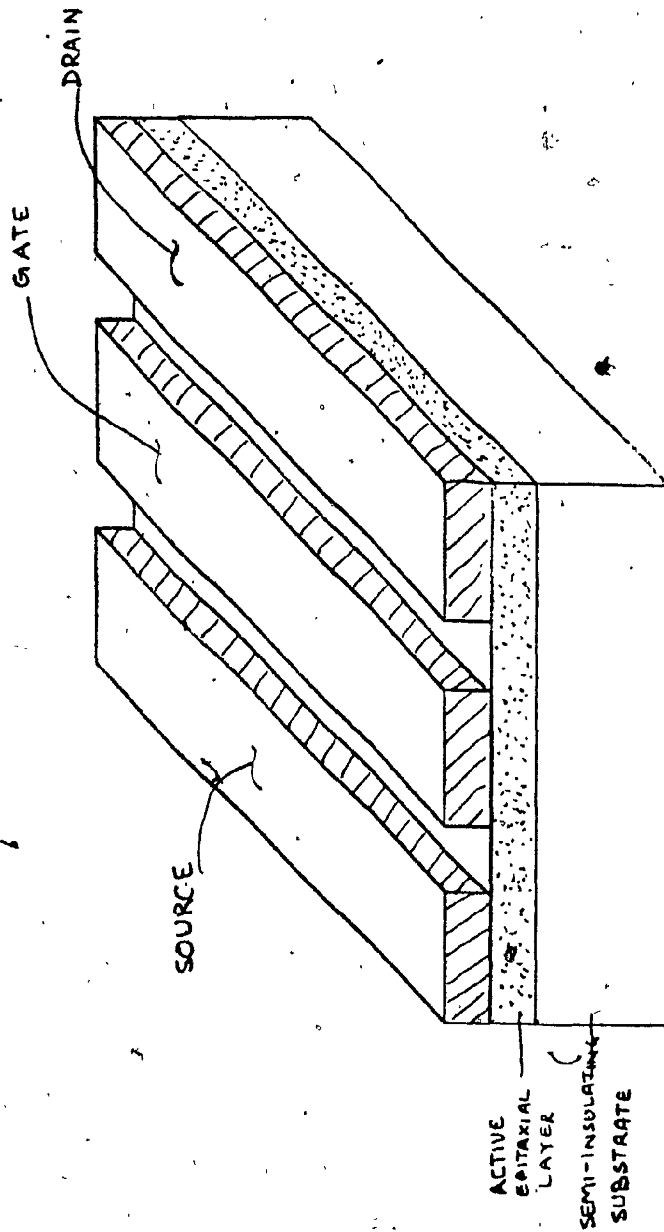


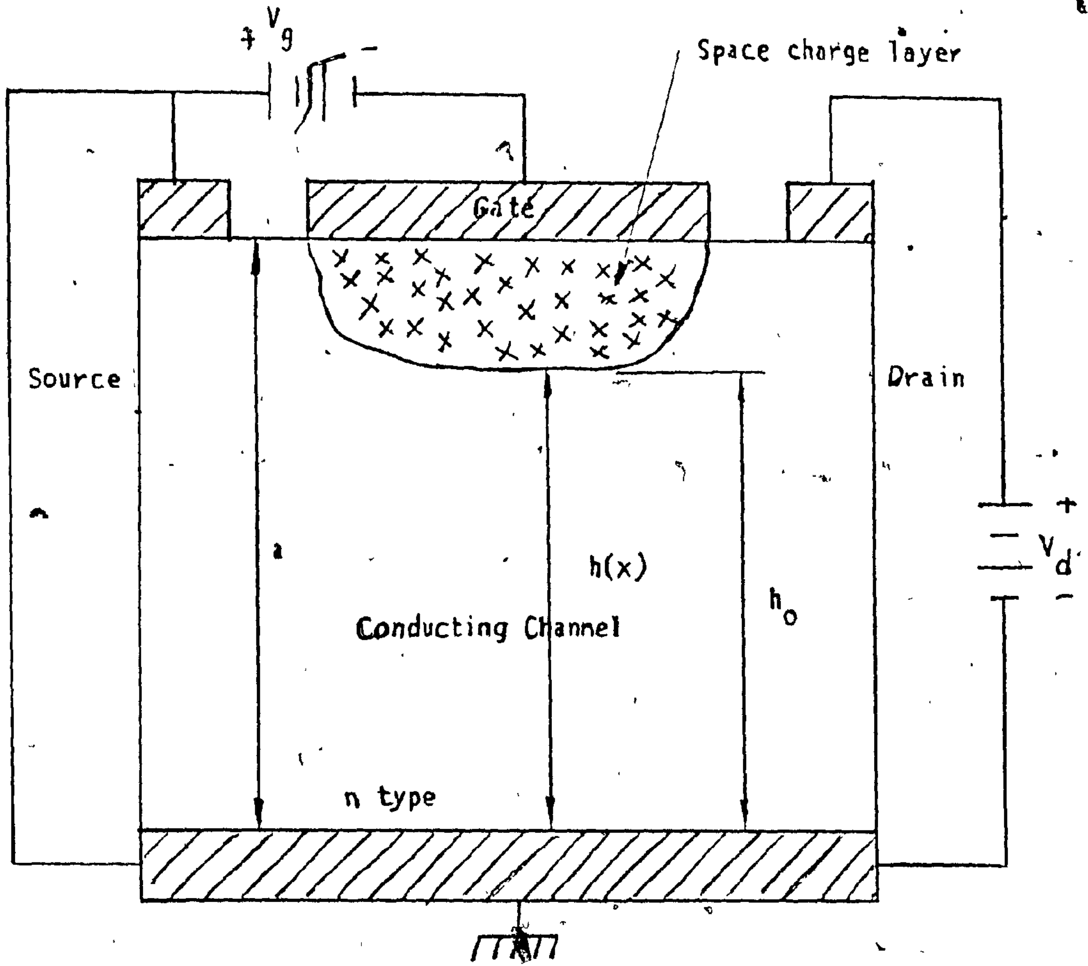
Figure 2.2 (c): Metal Semiconductor FET

(ii) The large parasitic capacitance of the gate bonding pad of Si, can be eliminated [10] by positioning the pad on the substrate with an active layer grown on the semi-insulating GaAs with resistivity larger than 10^{17} ohm-cm.

(iii) Noise figure improvements [11] due to a high purity buffer layer between the substrate and the active layer, a high doping level in the active n-layer (2.5×10^{17} cm^{-3}), a short gate length (less than one micron), and smallest possible source and gate-metal resistance.

The general theory of JFETs [12] has developed as a result of Shockley's analysis [13] using the gradual channel approximation. This analysis has proved useful for long gate devices. It has not been so successful for short gate devices, where the gradual channel approximation does not apply. Thus, along the lines of Yamaguchi et al [14], we adapt Schockley's analysis to short gate devices, and incorporate the carrier velocity saturation in the channel.

To start, usually GaAs FETs are constructed on a semi-insulating or n-substrate with a finite resistivity. However, assume an infinitely high resistivity for the substrate in order to simplify the problem. Consider a Schottky-barrier gate FET structure (without substrate) as shown in Figure 2.3. In a majority carrier device like a FET, fundamental equations describing the operations are Poisson's equation and the current continuity equation.



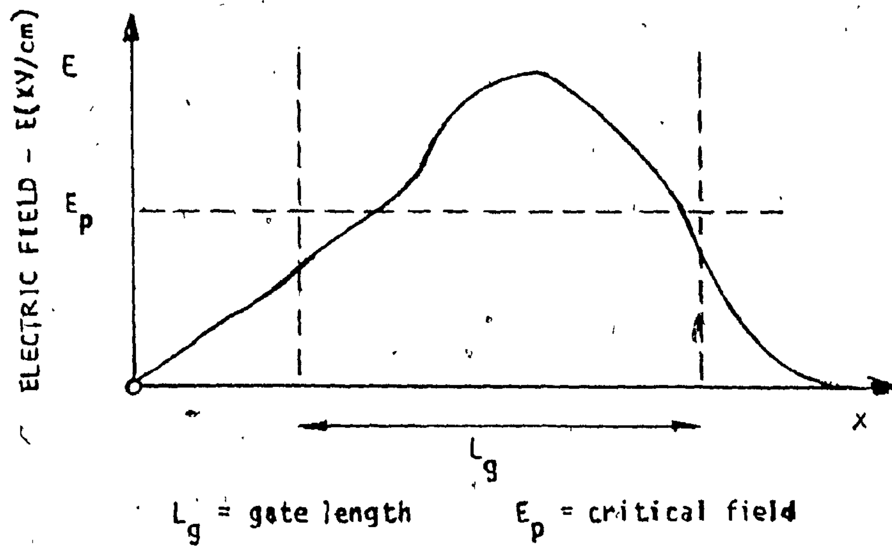


Figure 2.3: Schematic of a MESFET, Detail

They are given by:[15]:

$$\nabla^2 V = -\frac{q}{\epsilon}(N_D - n) \qquad (2.7)$$

$$\frac{\partial \rho}{\partial t} = \nabla \cdot J \qquad (2.8)$$

Current density and terminal current are expressed as follows[15]:

$$J = \rho v + D \nabla \rho \qquad (2.9)$$

$$J_{total} = qJ + \epsilon \frac{\partial E}{\partial t} \qquad (2.10)$$

$$I = \int_S J_{total} \cdot dS \qquad (2.11)$$

where S is an integration plane surrounding each electrode. The bulk negative differential conductivity effect is used in the velocity-field relation as [16]:

$$v(E) = \frac{\mu E + v_s (E/E_o)^4}{1 + (E/E_o)^4} \qquad (2.12)$$

where v_s and E_o are the saturation velocity and the characteristic field respectively (Figure 2.4). The diffusion coefficient D is given by [14]

$$D(E) = \frac{kT}{q}\frac{v(E)}{E} + \frac{3}{2}\tau v(E)^2 \qquad (2.13)$$

where τ is the relaxation time in the energy space (approximately 10^{-13} s for GaAs).

Boundary conditions imposed are [14]:

i) Ohmic contacts for source and drain electrodes,

$$\rho = N_D \qquad (2.14)$$

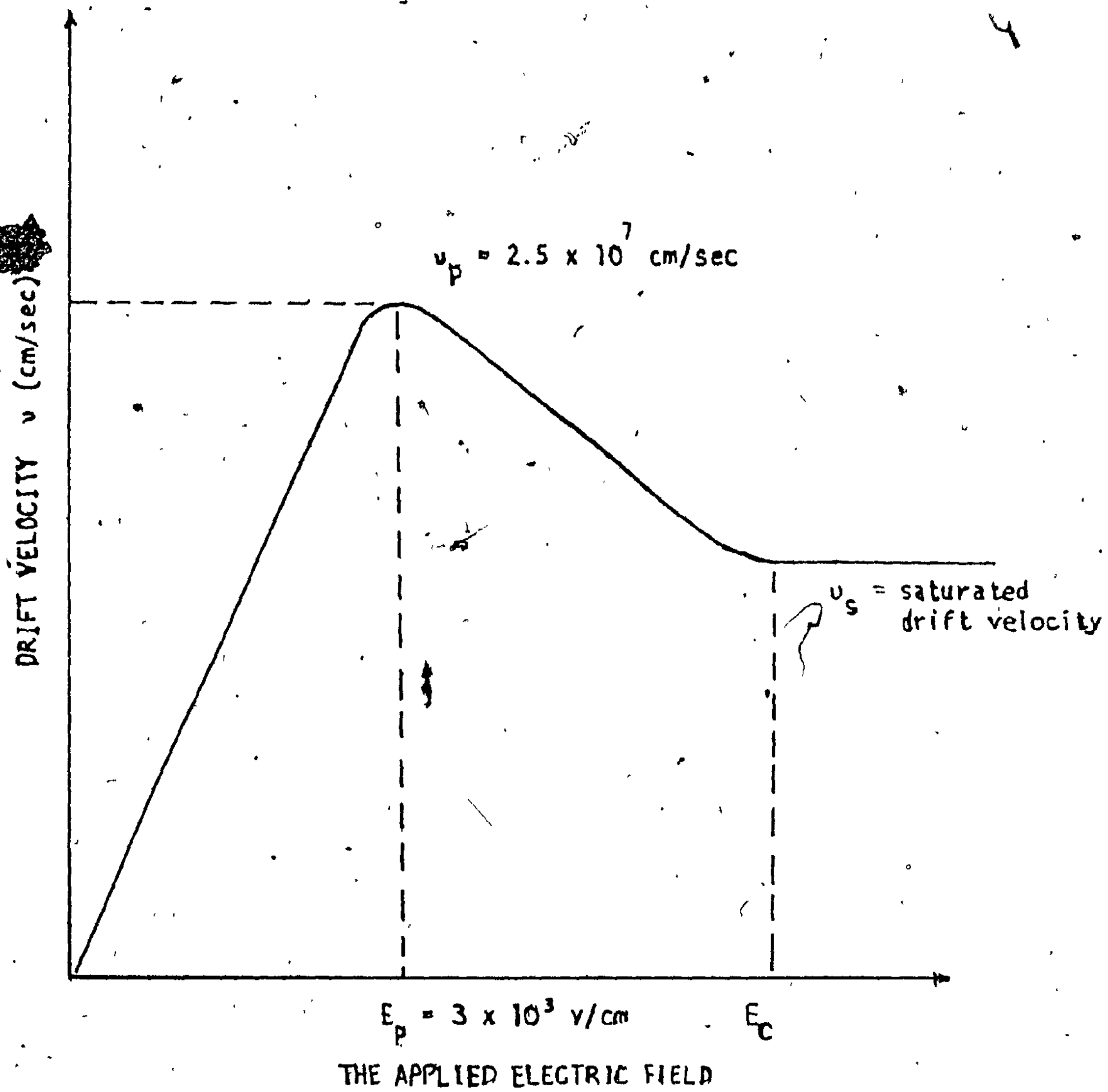


Figure 2.4: Electron Drift Velocity vs Electric Field for GaAs

ii) a rectifying contact for the gate electrode,

$$\rho = N_D \exp\left[\frac{-q}{kT} \quad (V_{bi} + V_G)\right] \quad (2.15)$$

$$V = V_{bi} + V_G \quad (2.16)$$

where V_{bi} is the built-in potential, and,

iii) free surface except for the electrodes,

$$\frac{\partial \rho}{\partial y} = \frac{\partial V}{\partial y} = 0, \text{ at } y = 0 \text{ and } d \quad (2.17)$$

In the region below the gate where the stream of carriers continue with constant density and uniform cross-section. We have to solve Poisson's equation assuming a uniform acceptor density and including the space charge of the flowing carriers. A particular solution[7] of Poisson's equation is

$$-\frac{\rho a^2}{2\epsilon}\left(\frac{(V_g + V_{dif} - V_p)}{\left(\frac{2\epsilon}{\rho a^2}\right)} - \frac{(V_g + V_{dif})}{\frac{2\epsilon}{\rho a^2}}\right) = V_p \quad (2.18)$$

(where $\frac{\rho a^2}{2\epsilon}$ is the gate-to-channel potential required to deplete the channel of carriers, and V_{dif} is the built-in diffusion potential due to the doping difference between channel and gate), everywhere in the stream (V_p = potential at pinch off and V_s = potential at saturation), and outside of the stream a potential increasing parabolically toward the gate electrode. Along with the homogeneous solution we have [17]

$$V = \sum_{n=-\infty}^{\infty} A_n \cos(2n+1)\frac{\pi y}{2a} \exp(2n+1)\frac{\pi x}{2a} \quad (2.19)$$

where x starts at the pinch off point.

$$V_{sd} = V_p - \frac{2a}{\pi} E_{sat} \sinh\left(\frac{\pi}{2a} L_g\right) \quad (2.20)$$

The transconductance g_m, is defined as the change in drain current dI_d divided by the change in gate voltage dV_g, holding the potential difference between source and drain V_{sd} constant, and under velocity saturation conditions we have [18][19]

$$g_m = -\frac{dI_d}{dV_g} = \frac{g_o E_{sat}}{2V_s\left(\frac{2\epsilon}{\rho a}\right)} L_g \frac{dV_p}{dV_g} \qquad (2.21)$$

This is further modified by Lehovec [12] and we end up with

$$I_d = \frac{I_p\left[3(U_m^2 - t^2) - 2(U_m^3 - t^3)\right]}{1 + Z(U_m^3 - t^2)} \qquad (2.22)$$

where I_p = the saturation current in the Schockley case where saturation effects are ignored ($Z=0, U_m=1$) [20]

$$Z = \mu V_p / L_g v_s \qquad (2.23)$$

μ = the low field mobility

V_p = the pinch-off voltage

v_s = the saturation velocity

$$t^2 = -(V_g + \emptyset) / (V_p + \emptyset) \qquad (2.24)$$

V_g = applied gate voltage

$\emptyset$ = the junction contact potential, and U_m is the normalized reduced drain potential given by:

$$U_m^3 + 3U_m(1/Z - t^2) + 2t^3 - 3/Z = 0 \qquad (2.25)$$

The device transconductance g_m and the drain resistance R_{ds} are given by [21]

$$g_m = \frac{\partial I_d}{\partial V_g} = g_{mo} (U_m - t) / (1 + Z (U_m^2 - t^2)) \qquad (2.26)$$

$$R_{ds} = E_c L_g \ (1 + Z (U_m^2 - t^2)) / I_d \qquad (2.27)$$

and, $$E_c = \cdot 13 \ v_s / \ \mu \qquad (2.28)$$

This model is appropriate for devices where the gate length L_g is of the order of a micron and the field can exceed 3 kV/cm even at low drain volts (3V) [22].

2.4 Theory of Resistive Mixing

The mixer, can be thought of as an ideal switch [23]. "Frequency converters" are used in communications receivers and transmitters, radars, radio and radar astronomy, control systems and many other applications. The frequency converter consists of a "local oscillator" or "pump" and a network containing one or more non-linear devices and means to couple the local oscillator and the input and output signals. This network is called a mixer. Inside the mixer the input signal, which is simply called the "signal", and the local oscillator are "mixed" together in the non-linear device to produce, among other frequencies, the required output frequency which is separated by filtering. The object is to achieve this with the least possible conversion loss, noise and non linear distortion. In hetrodyne receivers, and many other applications, the output signal is called the "intermediate frequency" (IF). This frequency is the difference between the signal and local oscillator frequencies.

Traditionally, the basic mixing process is accomplished by a non-linear positive resistance device [24]. Today's semiconductor technology is capable of producing mixer diodes, such as Schottky-barrier diodes, which exhibit almost purely resistive characteristics even at microwave frequencies. And in this respect GaAs has an advantage over Si [25] for high frequency devices in that the electron mobility for n-type GaAs is high, thus leading to higher frequency operation and reduced series resistance losses.

What follows below is the theory of resistive mixers. The mixer is treated as a linear periodically time-varying resistance inserted in a passive linear time-invarient network. The results emphasize the importance of the method of pumping and the proper termination of the out-of-band frequencies on the performance of the mixer. The analysis is limited to deducing the matrix equation relating the input and output frequency voltage and currents from the resistance waveform.

The schematic representation of a mixer is shown in Figure 2.5 . This is an ideal microwave mixer. The input signal is mixed with the pump and the output signal extracted. Typically however, many more frequencies are involved.

For linear mixers pumped with a frequency ω_p, the voltage and current can be written from Figure 2.6. This shows the basic electrical mixer circuit, and the equations are: (26)

$$V(t) = \sum_{n=-\infty}^{\infty} V_n e^{j(n\omega_p+\omega_o)t} \tag{2.29}$$

$$I(t) = \sum_{n=-\infty}^{\infty} I_n e^{j(n\omega_p+\omega_o)t} \tag{2.30}$$

where ω_o is the desired output frequency,

ω_p is the pump signal frequency,

ω_{in} is the input signal frequency.

The rest of the frequency components are undesirable harmonic mixer products. Figure 2.7 shows, on the frequency scale, the mixer frequencies involved. The circuit shown in Figure 2.6 has all out-of-band frequencies open circuited. The series circuit is tuned to the input signal and is a short circuit to it, and open

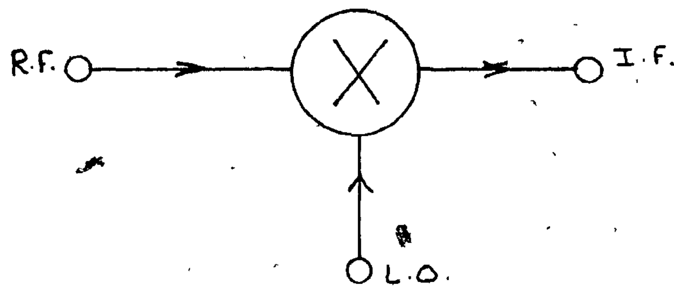


Figure 2.5 (a): Schematic Representation of a Mixer

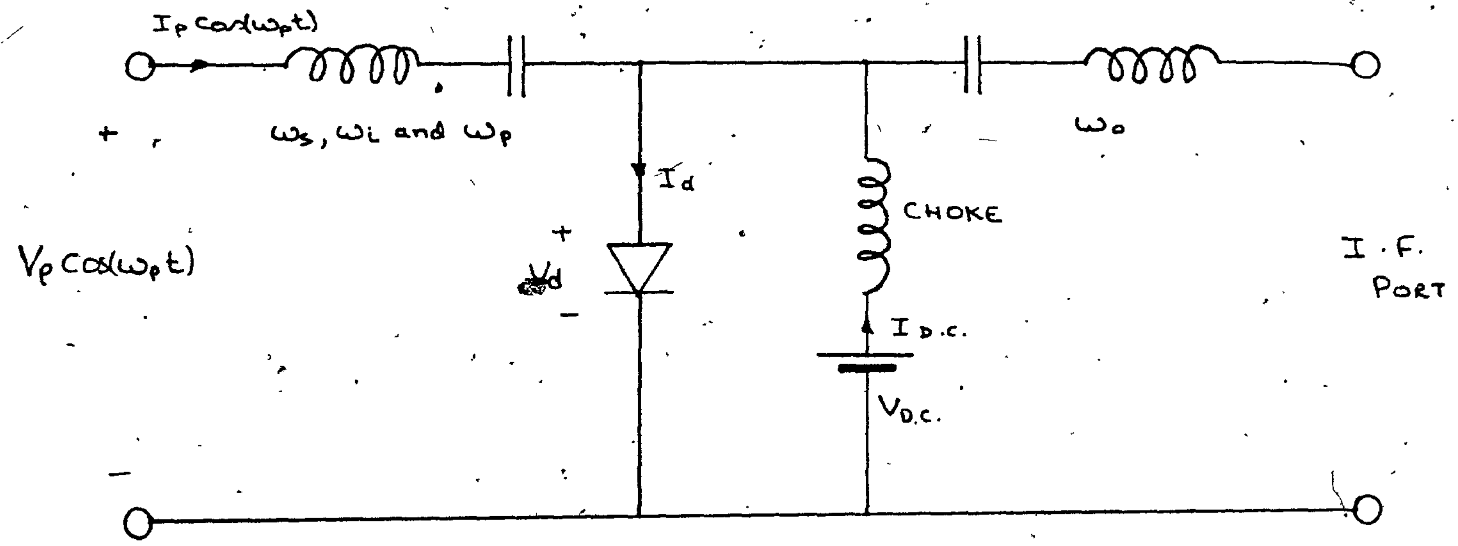


Figure 2.5 (b): Pumping a Single Diode Mixer

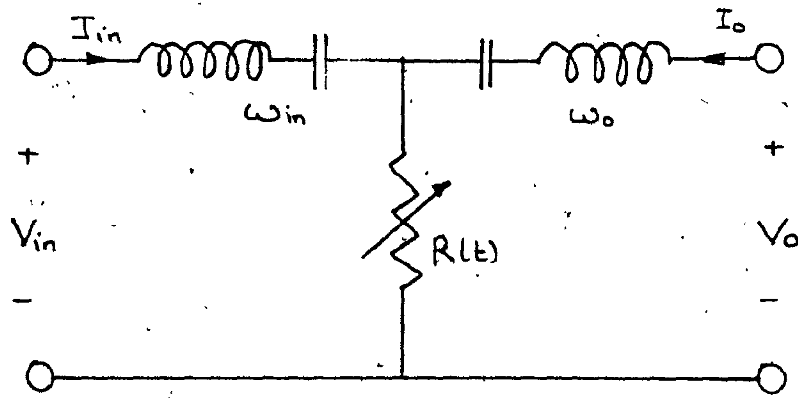


Figure 2.6: The Diode Resistive Mixer Circuit

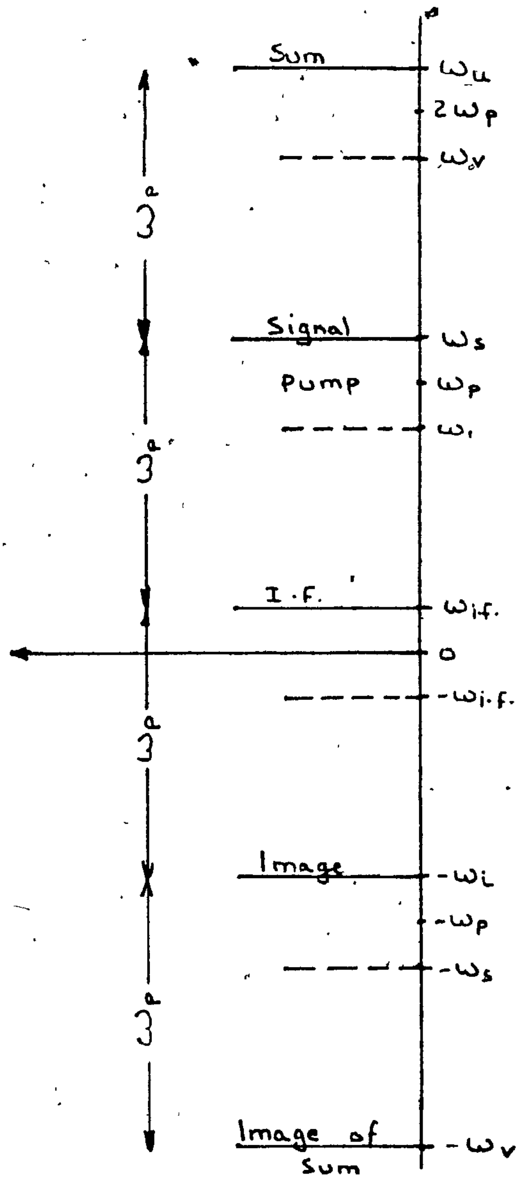


Figure 2.7: Frequency Separation and Notation

circuit at all other frequencies. This type of circuit is referred to as an infinite Q circuit; or to be more precise, the series circuit tuned to ω_{in} should be defined as a series L and C in the limit when $L \rightarrow \infty$ with $C = \frac{1}{\omega_{in}^2 L}$.

This implies $I_n = 0$ for all n, $n \neq in, 0$, because the circuit is short circuit for these frequencies only.

Thus, only $I_{in}\, e^{\,j\omega_{in}t}$ and $I_o\, e^{\,j\omega_o t}$ pass through $R(t)$.

The mixer equation becomes

$$\begin{bmatrix} V_{in} \\ V_o \end{bmatrix} = \begin{bmatrix} R_0 & R_1 \\ R_1^* & R_0 \end{bmatrix} \begin{bmatrix} I_{in} \\ I_0 \end{bmatrix} \qquad (2.31)$$

An important frequency is the image, and the inclusion of this component changes the above system to a three-port equation. Various other mixer analysis techniques are available. These can be with either all out-of-band frequencies are open circuited while all the even-order out-of-band frequencies are short circuited, etc. These each representations give different mixer equations, suited for the particular diode imbedding circuits. Essentially however, the circuits are duals of each other.

The separation of the frequencies for the mixer in different ports can be achieved by appropriate transmission line filters if $\omega_o << \omega_p$. However, the use of symmetry (in a balanced mixer arrangement), and more than one resistance (diode) for the frequency separation is only possible if constant, or generally linear, phase-shifting networks [27] can be built to operate at <u>all</u> the frequencies are

only required to be reactive, or generally to have large reflection coefficients.

Speaking generally still, in practice, a capacitance exists across the time-varying resistance and a fixed resistance exists in series with the combination. For example, these can be the diode junction capacitance and series resistance. In the literature many authors have dealt with this problem having[25],[26],[27] assumed that the junction capacitance short-circuits all the higher order out-of-band frequencies; ω_n, $|n| > 1$; across the time-varying resistance. Thus, only the signal, IF and image frequency voltages were considered. The result is a complex 3 X3 Z-matrix based on the model of the diode parameters. The analysis yields good results if the junction capacitance is large and the series resistance small. Figure 2.8 shows the diode model, valid for devices (GaAs) with negligible charge storage in the foreward region.

The result for optimum conversion loss is,[23]

$$L_{opt} \approx 1 + 2\,\omega_s/\omega_c \qquad (2.32)$$

where, $\omega_c << \omega_s$

and $\omega_c = \dfrac{1}{R_s C}$

This assumes an optimum resistance waveform of a rectangular pulse switching between R_{max} and R_{min} with the appropriate pulse duty ratio (typically 1/2). Also assumed is the fact that the level of the local oscillator is much higher than that of the signal; however, this result is only approximate and the signal will see some small non-linear distortion instead of a linear, periodically time-varying resistance.

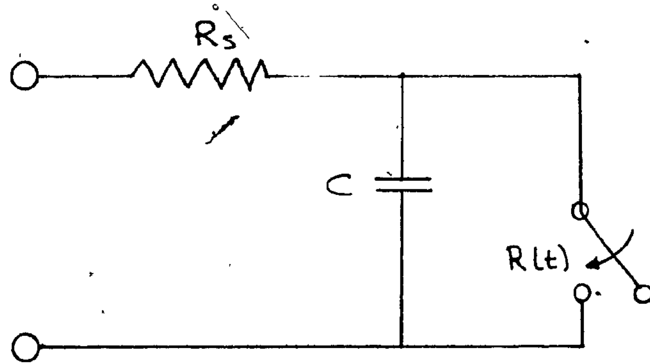


Fig. Figure 2.8 (a): Strongly Pumped Diode

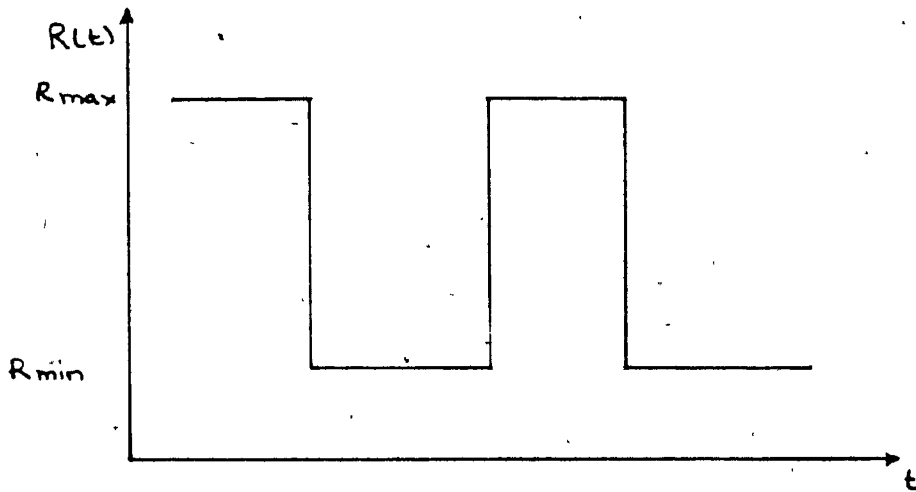


Figure 2.8 (b): Diode Resistance Waveform

The non-linear device is an exponential diode, and the V-I characteristics are:[1]

$$I = I_s \quad (e^{\alpha V} - 1) \tag{2.33}$$

where, I_s is the diode saturation current. A Schottky-barrier diode is the best known device to exhibit this characteristic over several current decades even at microwave frequencies. However, we have neglected the effects of the diode series resistance, reverse breakdown region and junction capacitance.

Another parameter, equally important as the conversion loss is noise figure[28]. In an ideal Schottky-barrier diode at microwave frequencies, the only relevant source of noise is shot noise. This can be accurately described by an emission model,[29] which produces a full shot noise effect identical to that of a temperature limited vacuum diode carrying the same current and neglecting the transit time. The thermal noise is generated due to the diode series resistance. And in a strongly pumped diode with square wave voltage, this will be the only considerable noise source in the mixer. (This is true since in the foreward direction where the shot noise is large, the junction is nearly short circuited, and in the reverse direction the shot noise is negligible). In this case the mixer acts as a passive network at room temperature and the noise figure should be equal to the conversion loss.

2.5 FET Mixer Theory

This section begins with yet another look at the basic meaning of mixing. Microwave Mixing, is defined as the conversion of a low power signal, called the RF signal at a frequency, f_s, to another signal called the IF at a frequency f_o, by combining the RF signal with a higher power signal, called the local oscillator LO, or pump signal at a frequency f_p, by means of non-linear devices such as varactors, transistors, vacuum tubes and so on. The nonlinear device output comprises of the following signals:

(i) the original input signals, the LO and the RF signals,

(ii) all harmonics of the LO, mf_p and the RF signal nf_s, (m and n are integers),

(iii) two primary sidebands, the upper sideband signal, called the sum, at the frequency $f_p + f_s$ and the lower sideband signal, called the difference at the frequency $|f_p - f_s|$.

(iv) a dc level,

(v) all higher products at the frequencies $m f_p \pm n f_s$

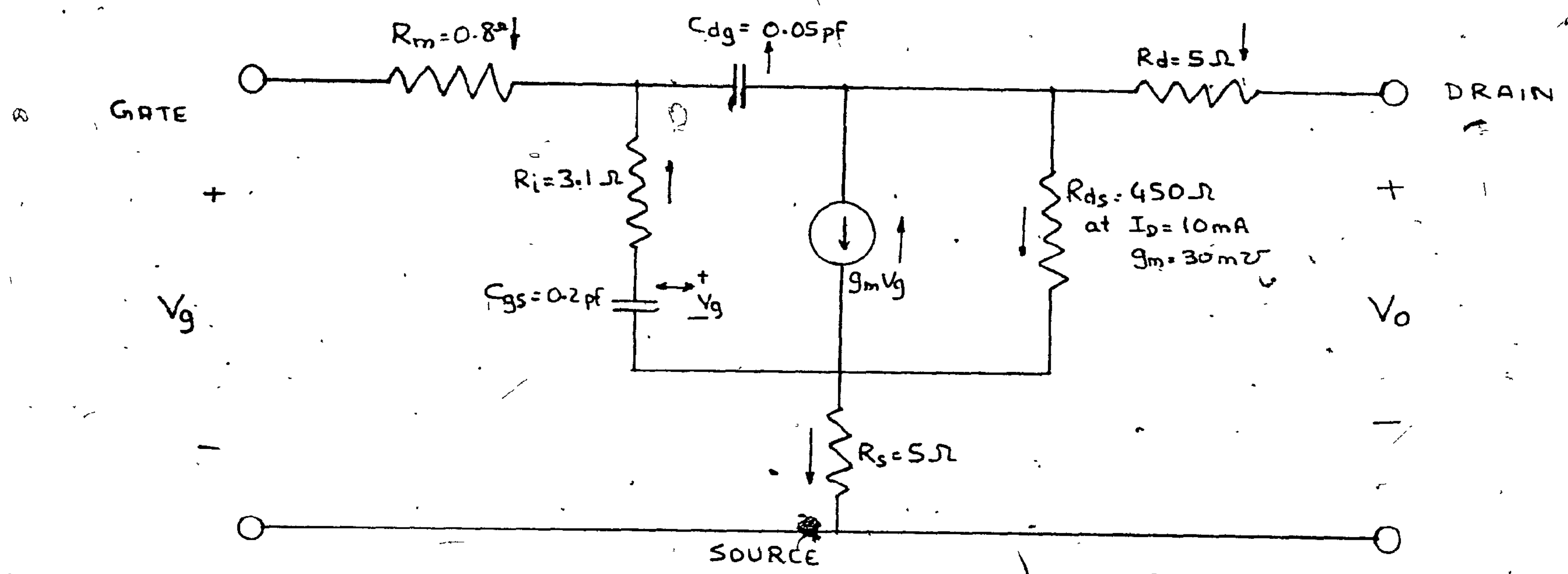
The desired output, commonly known as the intermediate frequency (IF) can either be the lower or the upper sideband. In our case we will discuss the lower sideband as the IF frequency. To present some mixer theory we need to consider the GaAs FET device.

It has widely been recognized [30] that GaAs Field Effect Transistors (FET) have very low noise figures of about 3 to 4 dB at X-band. The Schottky-barrier contact, together with the high mobility of the GaAs materials have made it

possible to attain high cut-off frequencies, as high as 50-80 GHz; that is, several times higher than that of silicon bipolar transistors.

Most of the work today on GaAs FETs have been concentrated on the application of FETs as small signal amplifiers [31], oscillators [32], and as power amplifiers [33]. The application of GaAs FET as mixers has been lightly treated in the literature [34], [35], [36]. So necessarily our buiding blocks will be the amplifier theory.

The small signal behaviour of a GaAs FET canbe described by the equivalent circuit [37] shown in Fgiure 2.9. In the diagram, the input gate circuit is represented by the gate metallization resistance R_m, a gate-to-source capacitance C_{gs} and the channel resistance R_i. The capacitance C_{dg} represents the gate-to-drain capacitance and R_{ds} represents the small signal relationship between the drain current and the gate voltage. R_d and R_s are the metallization resistances of the drain and source respectively. Typical element values for NEC V244 FET are shown in Figure 2.9. Not shown in Figure 2.9 is the package parasitics which have effect on the performance of the device at high frequencies. Figure 2.10 shows the packaged FET parasitics which have an effect on the performance of the device at high frequencies. Figure 2.10 shows the packaged FET parasitics (see Appendix C). The most important parasitic element is the gate lead inductance. At high frequencies Lg, Cgs, and Ls form a resonant circuit. Above the resonance frequency the gate inductance dominates the input impedance and the device stops to behave as a voltage controlled device,



Arrow indicates change for smaller gate lengths.

Figure 2.9 (a): The Intrinsic MESFET Model

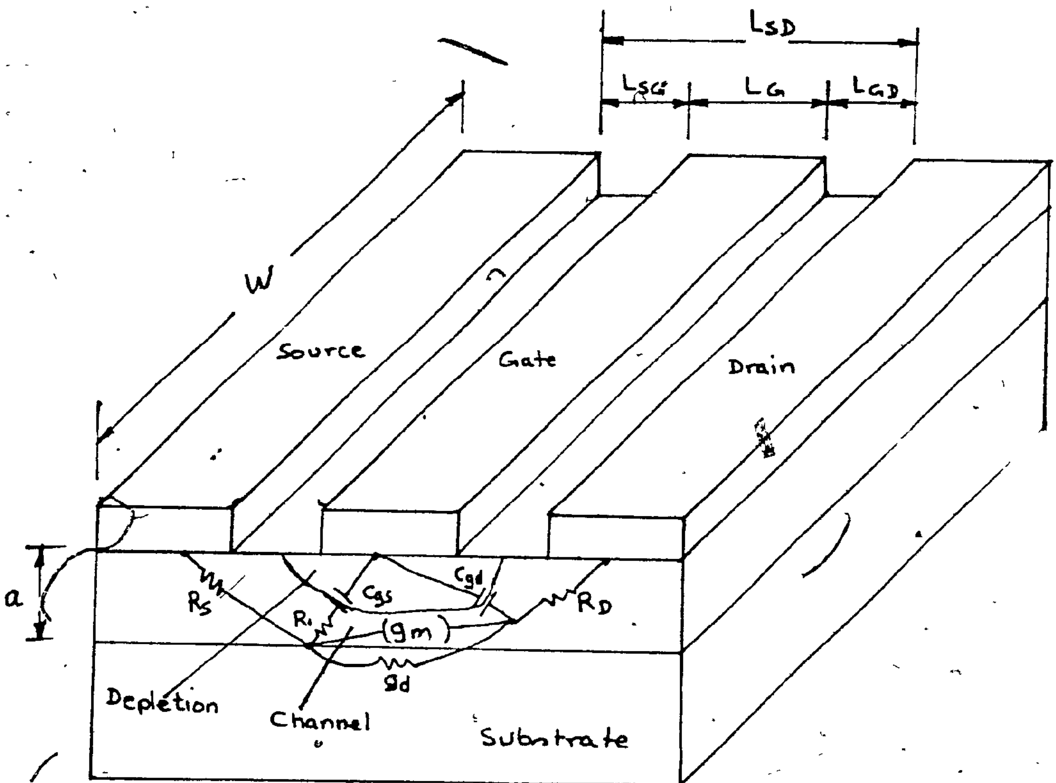


Figure 2.9 (b): Conceptual Cross-Section of a GaAs Schottky-Barrier Gate FET

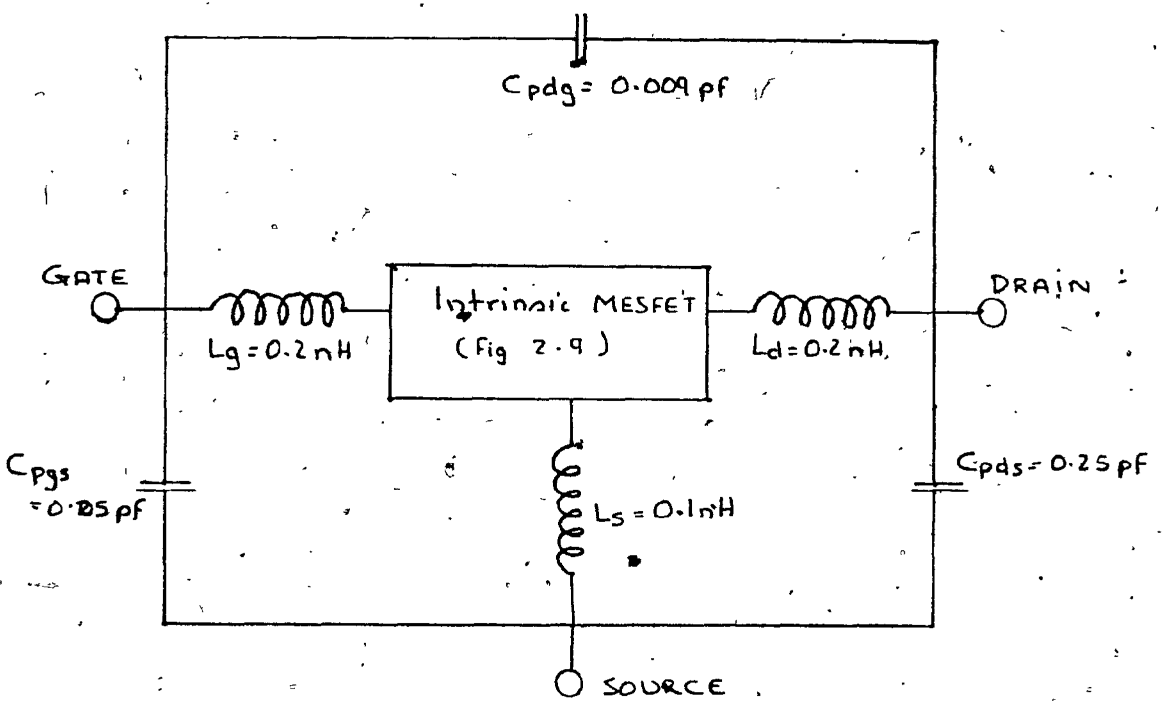


Figure 2.10: The Packaged MESFET

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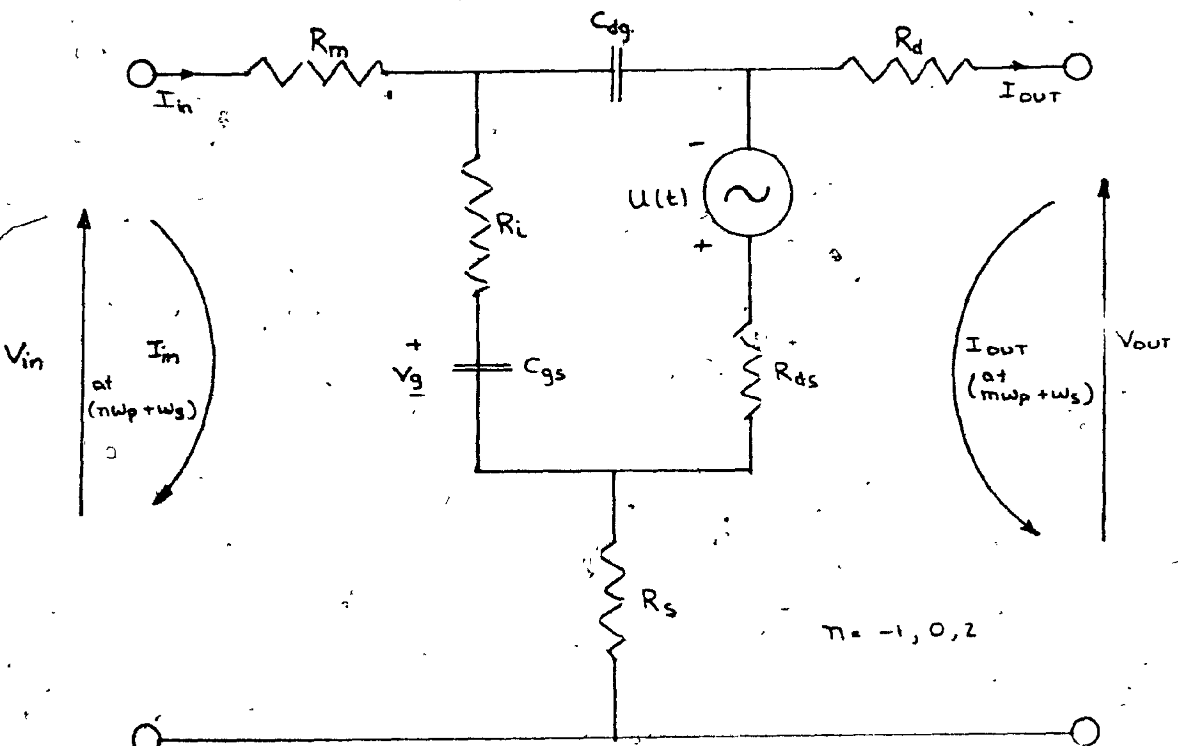


Figure 2.11: The FET Mixer Model

The time varying transconductance g_m can be expressed in a Fourier series as [34]

$$g_m = \sum_{k=-\infty}^{\infty} g_k \exp(j k\omega_p t) \tag{2.37}$$

where $\omega_p = 2\pi f_p$ = the pump signal frequency in radians,

g_k = the kth harmonic Fourier coefficient, given by

$$g_k = \frac{1}{2\pi} \int_{t_o}^{2\pi + t_o} g_m \exp(-j k \omega_p t)\, d(\omega_p t) \tag{2.38}$$

where t_o = an arbitrary time origin. This time origin can always be chosen such that -

$$g_k = g^*_{-k} \tag{2.39}$$

The input current I_{in} and the input voltage V_{in} are related by the following equation: (see Figure 2.11)

$$V_{in} = I_{in}(R_i + R_s + R_m - j/\omega_{in} C_{gs}) + I_{out} R_s \tag{2.40}$$

And similarly, the output voltage is related to the output current by (see Figure 2.11) -

$$V_{out} = I_{out}(R_{ds} + R_d + R_s) + I_{in} R_s - U(t) \tag{2.41}$$

where I_{in}, I_{out}, V_{in}, V_{out}, ω_{in} and ω_{out} represent any of the possible currents and voltages at the frequency $n\omega_p + \omega_s$ ($n = -\infty$ to $+\infty$)

To simplify the analysis, only three signals will be allowed to exist at both the input and the output terminals. These signals are:

i) RF signal at the frequency f_s,

ii) IF signal at the output frequency $f_o = |f_s - f_p|$ and,

iii) LO signal at the frequency f_p

iv). See note below.[38]

Now a set of equations relating the input RF currents and voltage to the output IF voltages and currents can be written down as:[34]

$$V_{is} = (R_{dt} - j/\omega_s C_{gs})\ I_{is} + R_s I_{os} \tag{2.42}$$

$$V^*_{io} = (R_{gt} - j/\omega_o C_{gs})^*\ I^*_{io} + R_s I^*_{od} \tag{2.43}$$

Note: The effect of the Image Signal (at $2\omega_p - \omega_s$)

The image signal at the frequency $2\,\omega_p - \omega_s$ generated by the nonlinear transconductance g_m will flow through the drain external circuits. In order to recover this power and convert it to the required IF signal, some means of feeding back the image signal to the gate capacitance must be devised. This feedback is necessary because, we assume, that the output drain current depends only on the gate voltage. The FET model of Figure 2.11 shows source contact resistance R_s (for voltage) and drain gate capacitance C_{dg} (for current) as possible feedback paths. The conversion process of the image signal to the IF involves the second harmonic Fourier coefficient g_2 of the non-linear transconductance g_m. If it is assumed that g_m varies between 0 and a fixed value, over the LO cycle, then g_2 is equal to zero. Thus, the effect of the image signal was considered to be negligible.

$$V_{os} = (R_s + jR_{ds}\, g_o/\omega_s C_{gs})\, I_{is} + R_{dt}\, I_{os} + jR_{ds}\, g_1\, I^*_{id}/\omega_o C_{gs} \quad (2.44)$$

$$V^*_{od} = (R_s + jR_{ds}\, g_o/\omega_o C_{gs})\, I^*_{od} + jR_{ds}\, g_1\, I^*_{id}/\omega_s C_{gs} + R_{dt}\, I^*_{od} \quad (2.45)$$

where g_o, g_1 = the average and the fundamental Fourier coefficients of g_m

$$R_{gt} = R_m + R_i + R_s \quad (2.46)$$

$$R_{dt} = R_s + R_d + R_{ds} \quad (2.47)$$

I_{is} = the input current at the RF frequency (ω_s)

I_{os} = the output current at the RF frequency

I_{id} = the input current at the IF frequency (ω_o)

I_{od} = the output current at the IF frequency.

V_{is}, V_{os}, V_{id}, and V_{od} are similarly defined as

$$\omega_o = 2\pi\left|(f_s - f_p)\right| \quad (2.48)$$

Let the impedances seen by the signals at the two ports be designated by Z_{id}, Z_{od}, Z_{is} and Z_{os}

where Z_{id} = the IF signal impedance at the input port (gate)

Z_{is} = the RF signal impedance at the input port (gate)

Z_{os} = the RF signal impedance at the output port (drain)

Z_{od} = the IF signal impedance at the output port (drain).

The impedance matrix Z describing the relationship between the RF and the IF currents is obtained from the above equations as: [39]

$$\begin{bmatrix} V_{is} \\ V^*_{od} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z^*_{22} \end{bmatrix} \begin{bmatrix} I_{is} \\ I^*_{od} \end{bmatrix} \tag{2.49}$$

where $$Z_{11} = R_m + R_i + R_s - jX_s - \frac{R_s(R_s + j g_o X_s R_{ds})}{(Z_{os} + R_{dt})} \tag{2.50}$$

$$Z_{12} = \frac{-jX_s\, g_1 R_s}{(Z_{os} + R_d + R_s + R_{ds})\,(R_{gt} + Z_{id} - jX_d)^*} \tag{2.51}$$

$$Z_{21} = jX\, g_1 \tag{2.52}$$

$$Z_{22} = R_{dt} - \frac{R_s(R_s + jR_{ds} g_o X_s)}{(R_{gt} + Z_{id} - jX_d)} \tag{2.53}$$

$$X_s = 1/\omega_s C_{gs} \tag{2.54}$$

$$X_d = 1/\omega_o C_{gs} \tag{2.55}$$

The conversion gain G_c can be written as [34]

$$G_c = \frac{4R_g}{R_L} \frac{|V_{od}|^2}{|V_{gs}|^2} = \frac{\text{The power IF delivered to load } R_L}{\text{The available RF power}} \tag{2.56}$$

where V_{gs} is the RF signal source voltage.

Assuming that the external circuit presents impedances Z_g and Z_L to the RF and the IF signals, respectively, then we can get the conversion gain as[34]:

$$G_c = \frac{4 R_g R_L |Z_{21}|^2}{|(Z_{22} + Z_L)^* (Z_{11} + Z_g) - Z_{12} Z_{21}|^2} \tag{2.57}$$

where R_g = Real (Z_g) = the real part of the impedance seen by the RF in the gate external circuit,

R_L = the real part of the impedance seen by the IF signal in the drain external circuit. = Real(Z_L)

The feedback capacitance C_{dg} increases the input admittance and the reverse transfer admittance, Y_{12}. The result is a reduced conversion gain. This can be seen by analyzing Figure 2.11[34]

$$I_{in} = Y'_{11} V_{in} + Y'_{12} V_{out} \quad (2.58)$$

$$I_{out} = Y'_{21} V_{in} + Y'_{22} V_{out} \quad (2.59)$$

where $$Y'_{11} = Y_c \left((F_\beta + 1/(R_s g_m + 1)) \right) \left(1 + R_s/R_{ds} \right) \quad (2.60)$$

$$Y'_{12} = -Y_c (F_\beta + R_s/R_{ds}) (1/R_s g_m + 1) \quad (2.61)$$

$$Y'_{21} = -Y_c (F_\beta + R_s/R_{ds}) (1/R_s g_m + 1) g_m \quad (2.62)$$

$$Y'_{22} = Y_c \left(F_\beta + (R_s + R_i)/(R_{ds}(R_s g_m + 1)) + 1/(R_{ds}(g_m R_s + 1)\right) \quad (2.63)$$

$$Y_c = j\omega C_{gs} = \text{gate capacitance admittance at } \omega \quad (2.64)$$

$$f_\beta = C_{dg}/C_{gs} \quad (2.65)$$

Thus,
$$\begin{bmatrix} I_{is} \\ I^*_{od} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y^*_{22} \end{bmatrix} \begin{bmatrix} V_{is} \\ V^*_{od} \end{bmatrix} \quad (2.66)$$

where $$Y_{11} = \frac{Y_{cs} K_1 - (Y_{cs} K_2 + g_0) K_2}{(Y_{os} + K_3 + Y_{cs} F_\beta)} \quad (2.67)$$

$$Y_{12} = \left[\frac{K_2 Y_{cd} g_1}{K_1 Y_{cd} + Y_{id}} \right]^* \left[\frac{Y_{cs} K_2}{(Y_{os} + K_3 + Y_{cs} f'_\beta)} \right] \quad (2.68)$$

$$Y_{21} = g_1 \quad (2.69)$$

$$Y_{22} = K_3 + Y_{cd}\, F'_\beta - \frac{Y_{cd}\, K_2\, (g_o + K_2\, Y_{cd})}{Y_{cd}\, K_1 + Y_{id}} \qquad (2.70)$$

$$K_1 = F_\beta + 1/(R_s g_o + 1) \qquad (2.71)$$

$$K_2 = -R_s/R_{ds}(1 + R_s g_o + 1) - F_\beta \qquad (2.72)$$

$$K_3 = 1/R_{ds}(1 + R_s g_o) \qquad (2.73)$$

$$Y_{cd} = j\,|\omega_p - \omega_s|\, C_{gs} \qquad (2.74)$$

$$F'_\beta = F_\beta \pm (R_i + R_s)/R_{ds}(R_s g_o + 1) \qquad (2.75)$$

Y_{id} = Input circuit - gate admittance at IF

Y_{os} = Output circuit - drain admittance at RF

$$Y_{cs} = j\,\omega_s\, C_{gs} \qquad (2.76)$$

For the NE244, $F_\beta = C_{dg}/C_{sg} = 0.25$, whereas the R_s feedback contribution to K_2 is of the order of 10^{-2}. K_2 is a multiplication factor in Y_{12}.

CHAPTER 3

DESIGN AND CONSTRUCTION

3.1 Introduction

The intention of this chapter is to describe the circuit design and construction. The discussion starts with a brief theoretical and technological background involved in the design and production of microwave integrated circuits. However, the main intent here is to provide a set of equations relating impedance, wavelength and loss in terms of the width, thickness and length of the printed track. These are state of current MIC theory and technology, and detailed derivation is often based on numerical techniques and experimental analysis. This detail is left to the references listed at the end of the report, and Appendix E.

The actual mixer circuit is, of course, constructed on a MIC realization. This section presents a block diagram of the gate injected local oscillator type mixer. The basic frequencies are -

F_{signal} = 6 GHz (5925 to 6425 MHz) injected at the gate terminal. Typical signal level of −40 dBm. Thus, for all intents a small-signal model of the non-linear mixing device is adequate for the design of matching networks.

F_{pump} = 2225 MHz. This is the local oscillator, and is also injected at the gate via a printed circuit diplexer combing the 6 GHz input signal with this 2 GHz pump signal. This pump is typically at +10 dBm, and presents to the gate a

switching signal which is responsible for the transconductance modulation and subsequent frequency translation.

F_{out} = 4 GHz (3700 to 4200 MHz). This is the IF difference signal, resulting from (Input-Pump) combination. There are several other mixer outputs, however in this example, we have chosen to select this as the desired Intermediate frequency.

The rest of this chapter discusses the details of the mixer circuit realization, and the references for the diplexer design.

3.2 The Microstrip Transmission Line

A planer transmission line consisting of a strip conductor separated from a ground plane by a dielectric layer is known as a microstrip transmission line. The Schematic diagram of a microstrip transmission line, shown in Figure 3.1 (a),[1] defines the dimensional parameters of the structure. The characterization of this structure is of great importance because of their increasing use as a guiding structure in microwave circuits.[2],[3] . This section summarizes only some important and useful relations for computing the characteristics of a MIC circuit.

The ceramic substrate is generally a polished (better than 2 micro-inch surface finish) alumina (99.5% alumina - Al_2O_3) and the vacuum evaporated metallization[4] (thin film) is as listed below in Figure 3.1 (b).

The initial metal is Cr to provide adhesion of Cu to the alumina. The next metal is Cu. This is the main microwave conductor and is several skin depths thick at these frequencies of operation. The Ni layer acts as a buffer between Cu and Au. The final Au layer is to protect the Cu from tarnishing and to facilitate thermo-compression bonding and conventional soldering of components onto the circuit.

Proximity of the air-dielectric interface with the strip conductor causes a discontinuity in the electric and magnetic fields (see Figure 3.2 at the interface.[2] In fact, there are components of both electrical and

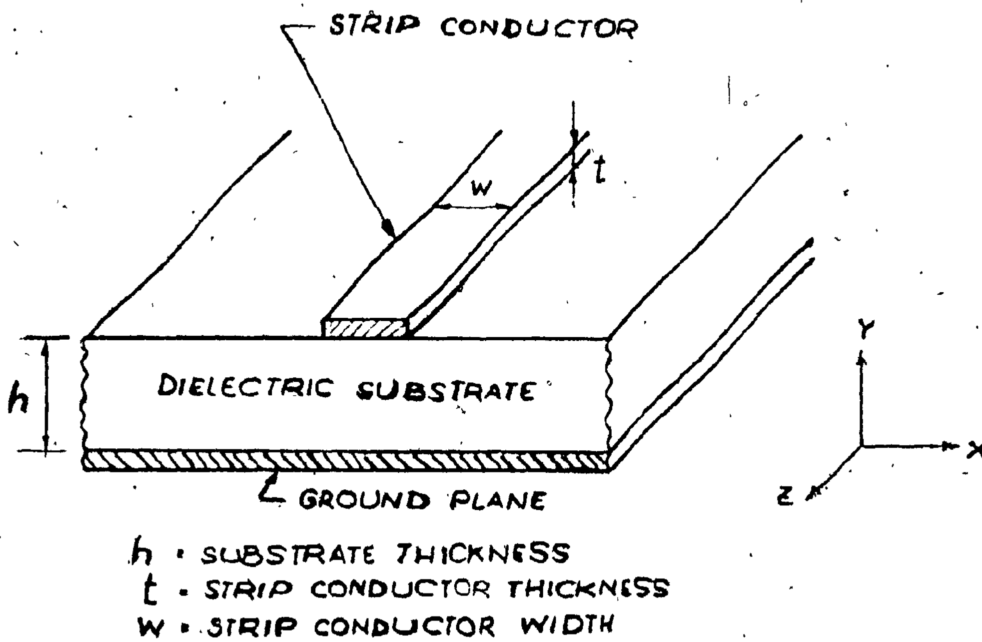


Figure 3.1 (a): Microstrip Transmission Line

		Metallization	Thickness
1.	Top Side RF Conductor track	Cr	200Å
		Cu	4 micron
		Ni	2000Å
		Au	1 micron
2.	Bottom Side Ground Plane	Cr	200Å
		Cu	4 micron
		Ni	2000Å

Figure 3.1 (b): Metallization Scheme

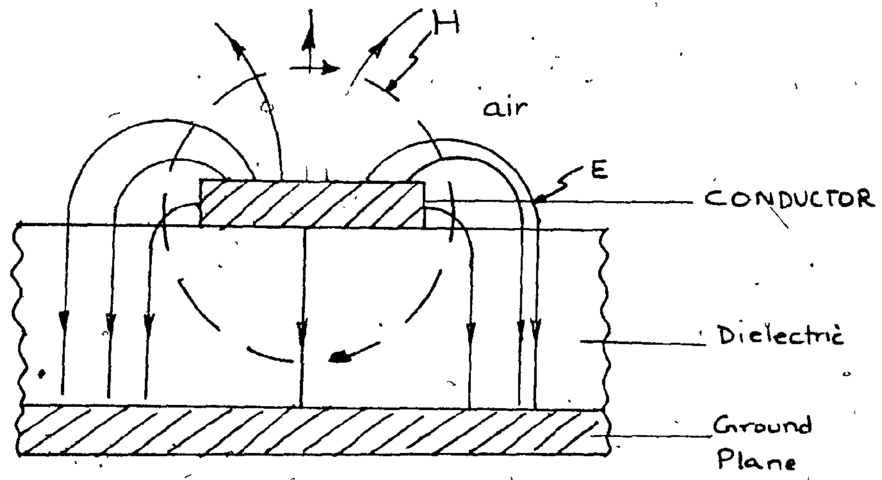


Figure 3.2: Electric and Magnetic Fields in the Vicinity of a Microstrip

magnetic fields in the direction of propagation. The propagation mode is thus not a pure TEM mode. At the present time, one of the most convenient and useful techniques for determining the wave impedance, the phase velocity and the wavelength is that reported by Wheeler.[5] Wheeler derived the following expressions for the wave impedance of wide ($W/h > 1$) and narrow ($W/h < 1$) lines:

$$Z_o = 0.5 \frac{\sqrt{\epsilon_r}\ R_c}{\frac{W}{2h} + C + \frac{\epsilon_r+1}{2\pi\epsilon_r} \ln \frac{\pi e}{2}\left(\frac{W}{2h} + 0.94\right) + \frac{\epsilon_r-1}{2\pi\epsilon_r^2} \ln\left(\frac{\pi e^2}{16}\right)} \qquad \left(\frac{W}{h} < 1\right) \qquad (3.1)$$

and,

$$Z_o = \frac{R_c}{2\pi}\sqrt{\frac{2}{\epsilon_r+1}}\left[\ln\frac{8h}{W} + \frac{1}{32}\left(\frac{W}{h}\right)^2 - \frac{1}{2}\,\frac{\epsilon_r-1}{\epsilon_r+1}\left(\ln\frac{\pi}{2} + \frac{1}{\epsilon_r}\ln\frac{4}{\pi}\right)\right] \qquad \left(\frac{W}{h} > 1\right) \qquad (3.2)$$

where, R_c = wave impedance of free space

$e = 2.72$

$c = \frac{1}{\pi}\ln 4$, edge correction for an infinitely wide microstrip line.

ϵ_r = relative dielectric constant.

The wavelength in the microstrip may be calculated using

$$\lambda_g = \frac{\lambda_o}{\sqrt{\epsilon_{eff}}} \tag{3.3}$$

where λ_o is the free space wavelength and ϵ_{eff} is the effective dielectric constant defined as

$$\epsilon_{eff} = \left[\frac{Z_{oa}}{Z_o}\right]^2 \tag{3.4}$$

where, Z_o and Z_{oa} are the wave impedances of a microstrip line with and without the dielectric substrate respectively. The phase velocity in the microstrip is given by:

$$\nu_p = \frac{\nu_{pa}}{\sqrt{\epsilon_{eff}}} \tag{3.5}$$

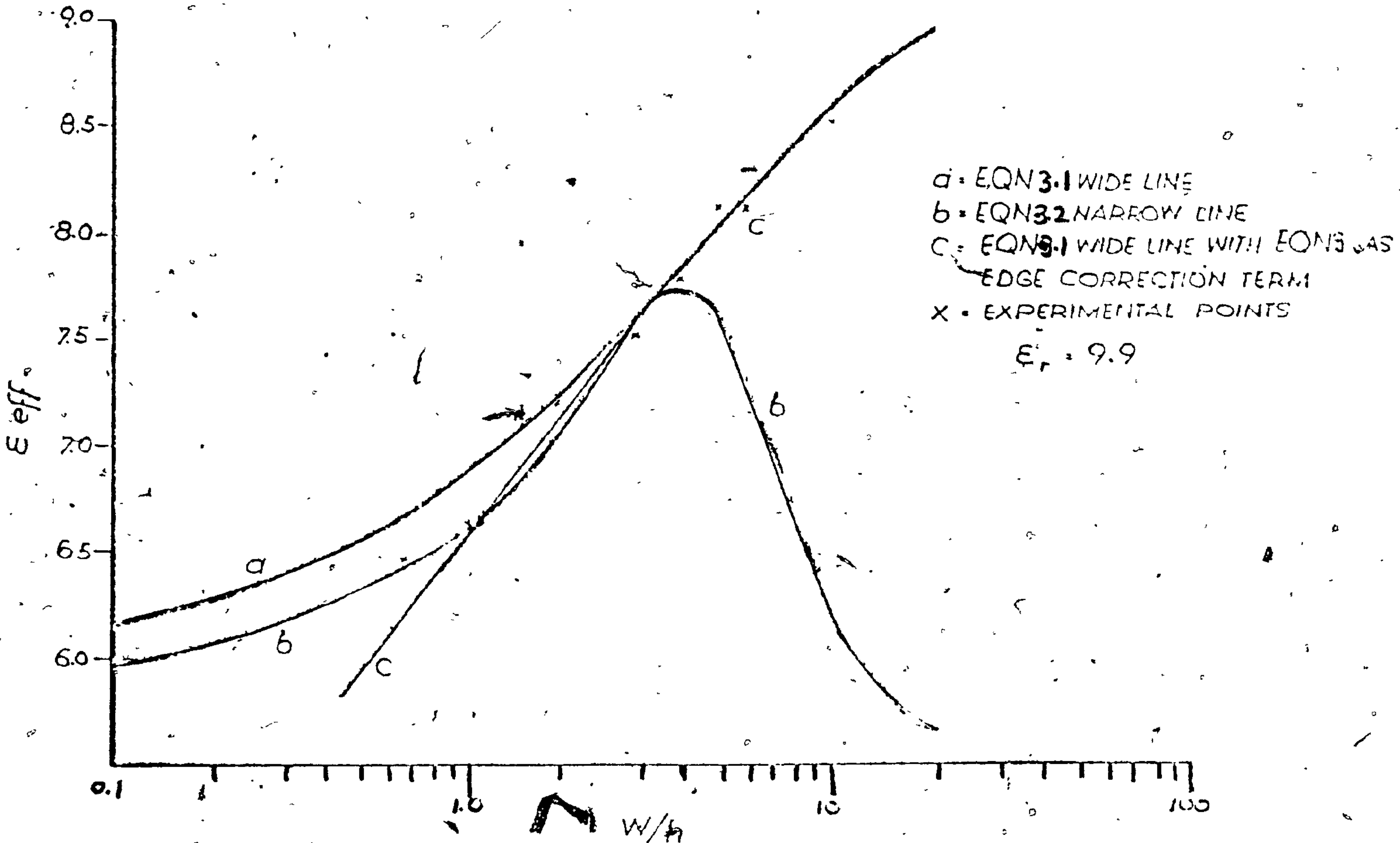
where ν_{pa} is the velocity of light in vacuum.

A plot of the wide line approximation ($W/h > 1$) and the narrow line approximation ($W/h < 1$) as a function of W/h, Figure 3.3, does not yield a cross-over at $W/h = 1$ as might be desired or expected. This is because the expression $h \, [\text{illegible}] \left(\frac{4}{\pi}\right)$ is used to account for edge correction for $W/h > 1$. However, [6] the open end effect in microstrip lines is described by the following relationship:

$$\Delta l = \frac{1}{k} \text{ arc cot}\left[\frac{4C + 2W}{C + 2W} \cot (kC)\right] \tag{3.6}$$

where Δl = apparent increase in length of the centre conductor due to fringe field at open end.

$k = 2\pi/\lambda$



MICROSTRIP TRANSMISSION-LINE EFFECTIVE DIELECTRIC CONSTANT AS A FUNCTION OF THE W/h RATIO

Figure 3.3

and for $kC < 0.3$; $$\Delta l = \left[\frac{C + 2W}{4C + 2W}\right] \quad (3.7)$$

Figure 3.3 shows curve C, incorporating this correction and a definite crossover occurs at $W/h = 1$. This same edge correction is useful in correcting the lengths of the $\lambda/2$ resonators used in the design of a coupled line bandpass filters.

A relation to predict the frequency dependence of the effective dielectric constant of the microstrip transmission lines is [7]

$$\epsilon_{eff} = \epsilon_r \left(1 - \frac{B}{1+\omega^2 T^2} \right) \quad (3.8)$$

where ω is the angular frequency, and,

$$B = 1 - \frac{\epsilon_{ffo}}{\epsilon_r} \quad (3.9)$$

where $\epsilon_{effo} = \lim_{\omega \to 0} \epsilon_{eff}$ and $\lim_{\omega \to \infty} \epsilon_r$

and $$T = 0.11\,(W)^{0.6} \sqrt{\epsilon_r - 1} \quad (3.10)$$

The frequency dependence of coupled microstrip lines is determined from:

$$T = 0.11 \left(\omega \frac{s}{h}\right)^{0.6} Z^2 \sqrt{\epsilon_r - 1} \quad (3.11)$$

where s = distance between two coupled lines,

h = substrate thickness,

Z = Even mode impedance/50 for even mode

and Odd mode impedance/50 for odd mode.

For calculation of incremental inductance in microstrip lines[8], the recession in the width of the strip conductor and the recession in the thickness of the strip conductor are used. Also, using the internal impedance formulae for a semi-infinite plane solid conductor with a round conductor at high frequencies (at which the thickness of the conductor is at least twice the skin depth), yields

$$\alpha_c = \frac{8.68}{2Z_o} R_s \left[\frac{1}{W} + \frac{1}{\pi h} \right] \left[1 - \left(\frac{W}{4h}\right)^2 \right] \quad W/h < 2 \qquad (3.12)$$

and

$$\alpha_c = \frac{8.68\, R_s}{2\, Z_o} \left[\frac{\pi}{W} + \frac{1}{h} \right] \frac{\frac{W}{2h} + \frac{W/2\pi h}{W/2h + 0.94}}{\left[\frac{W}{2h} + \frac{1}{\pi} \ln\left(\pi\, 2\, e \left(\frac{W}{2h} + 0.94 \right) \right) \right]^2} \qquad (3.13)$$

$$\frac{W}{h} > 2$$

where Z_o is the characteristic impedance of the microstrip line and R_s is the surface resistivity of the strip conductor (for copper $R_s = .00826 \sqrt{f} \left[1 + \Delta (\rho/s) \sqrt{f}\right]$, where f is the frequency and $\Delta(\rho/S)$ is the surface roughness correction factor.

We can thus get[8] for calculating MIC conductor loss:

$$\alpha_c \cong \left[.072 \sqrt{f} (1 + 0.13 \sqrt{f}) \right] f\left(\frac{W}{h}\right) / [Z_o W] \qquad (3.14)$$

where $\lim_{\frac{W}{h} \to \infty} f\left(\frac{W}{h}\right) = 1$

The parasitics associated with impedance discontinuities (such as quarter-wave transformers) are most pronounced as an excessive phase shift[9]. The series reactance is described by:

$$\omega L = 2\, \frac{Z_{01} W_1^*}{\lambda} \ln \left[\operatorname{cosec} \left(\frac{\pi}{2} \cdot \frac{W_2^*}{W_1^*} \right) \right] \qquad (3.15)$$

where ωL = Impedance discontinuity series reactance

Z_{01} = characteristic impedance of the transformer section

λ = wavelength

$W_{1,2}$ = equivalent strip width, where

$$W_n^* = \frac{h \; R_c}{Z_{on}} \sqrt{\frac{1}{\epsilon_{eff}}} \; , \quad n = 1,2 \qquad (3.16)$$

The short reactance may be found by approximating the step discontinuity by an open circuit. Thus electrically, the quarter wave transformer will appear as $\lambda/4 + 2\Delta\ell$, where $\Delta\ell$ is the extension at the open end of the transformer or step and is converted into an equivalent shunt capacitance.

However, thankfully, most CAD programs like COMPACT[12], incorporate all these MIC features, and the user merely needs to specify, frequency, impedance, length and loss constant to accurately generate the microwave performance properties.

3.3 The Circuit Design

The design follows the theory developed earlier in this chapter and in chapter 2. The 2225 MHz local oscillator and the swept 5925 to 6425 MHz input signal are diplexed and injected at the gate of the FET. The 3700 to 4200 MHz output signal is taken from the drain. Figure 3.4 shows the FET D.C. operating characteristics. The nonlinear mixing regions are indicated. Approximately (and ideally);

$$I_D = I_{DSS}\left(1 - \frac{V_{gs}}{V_P}\right)^2 \tag{3.17}$$

neglecting the DC component, we get

$$V_{gs} = \text{L.O.} + 6 \text{ GHz input} \tag{3.18}$$

resulting in $I_D = \text{L.O.} + 6\text{ GHz} + 2 \times \text{L.O.} + 2 \times 6\text{ GHz}$

$$+ \underbrace{(6\text{GHz} - \text{L.O.})}_{\text{desired 4GHz output}} + (6\text{GHz} + \text{L.O.}) \tag{3.19}$$

The undesired mixing products must necessarily be filtered out and terminated reactively. Figure 3.5 shows a block diagram and Figure 3.6 shows the design layout.

Basically when a sufficiently strong local oscillator signal is applied to the gate of an FET biased close to pinch-off, the drain current will be modulated between zero and the saturation value I_{DSS}. Simultaneously FET transconductance, g_m, will also vary between zero and its peak value. Figure 3.7. Since g_m remains fairly constant down to small values of the

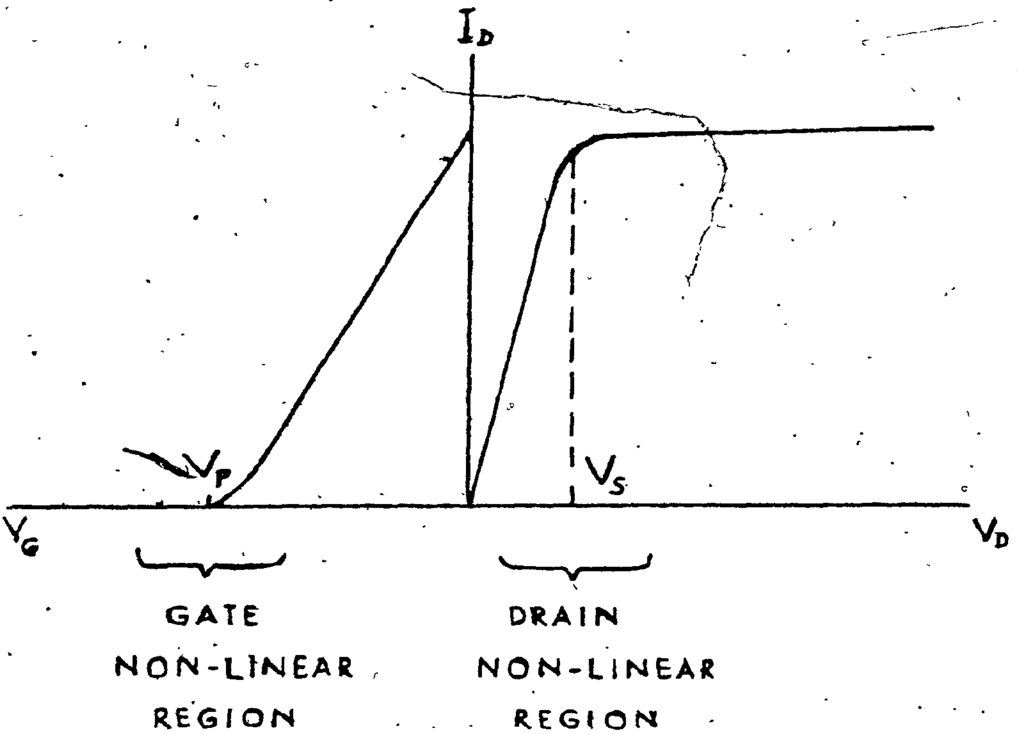


Figure 3.4: FET D.C. Characteristics

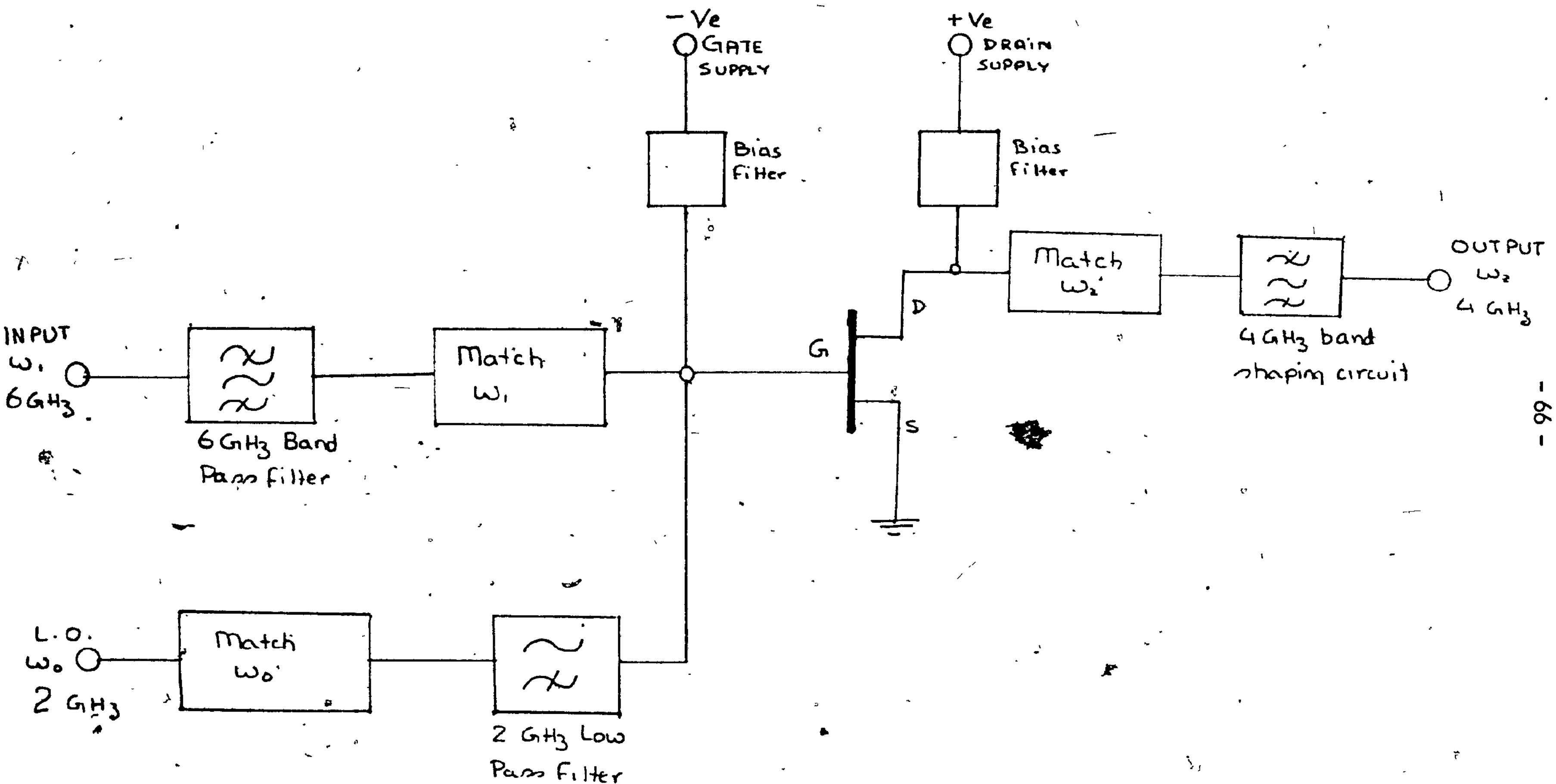
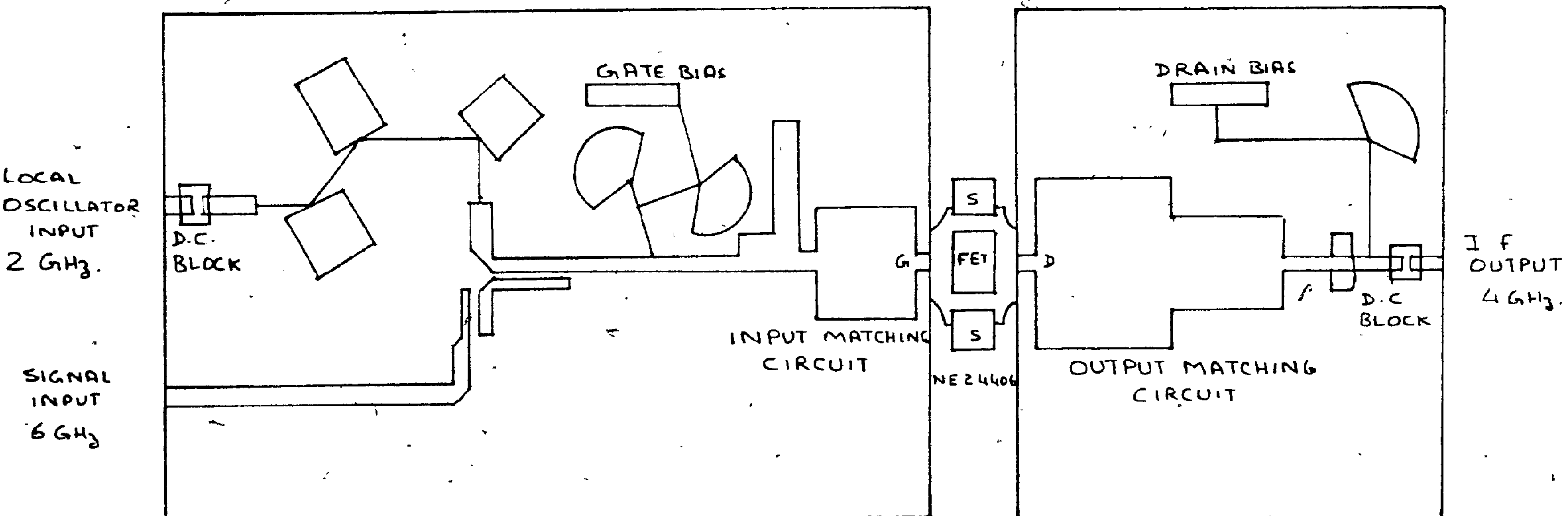


Figure 3.5: Block Diagram for a Gate Injected Local Oscillator, Mixer



$V_{GS} = 3.9v$

$V_{DS} = 4.1v$

$I_{DS} = 3.7\ mA$

L.O. = +7 dBm

Figure 3.6: Design Layout for the Gate Mixer

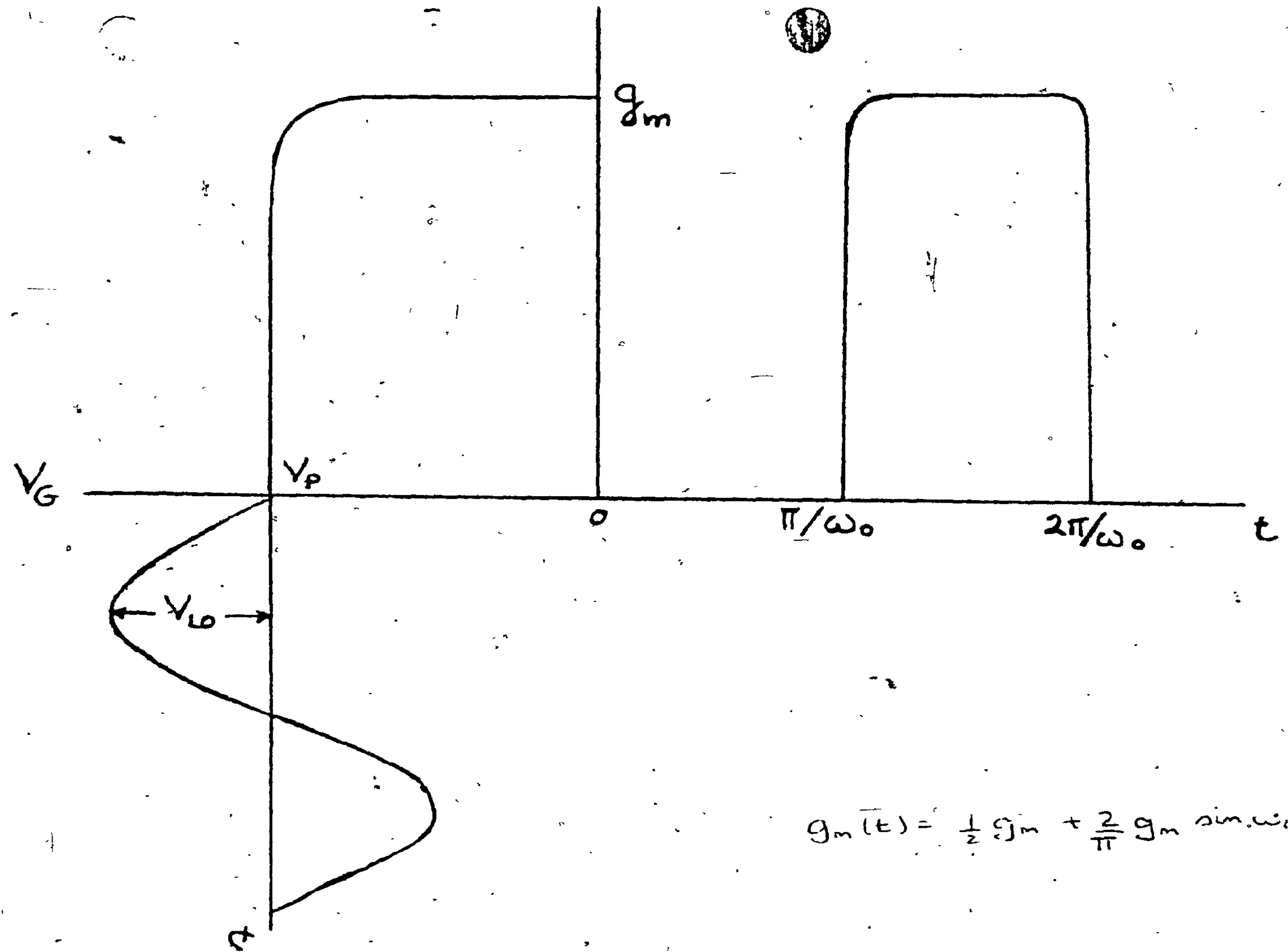


Figure 3.7: Process of Generating Time-Varying Transconductance $g_m(t)$ in the Gate Mixer

the drain current, the g_m waveform can be regarded as approximating a square wave. For this limiting condition the intrinsic mixer conversion gain is given by [10]

$$G_C = \frac{1}{4}\left(\frac{g_m}{\pi\omega\overline{C}_g}\right)^2 \frac{R_D}{R_g} \tag{3.20}$$

where $\overline{C}_g$ is the time average of the gate-to-source capacitance and R_D and R_g are the drain and gate resistances. For the one micron gate (NEC) FET, this yields a conversion gain of 7 dB at 6 GHz. The block diagram of Figure 3.5, shows a 2 GHz low pass filter, and a 6 GHz bandpass filter, diplexer and a matching circuit for the gate. The output at the drain is removed by a matching network.

All experimental results quoted were performed with the mixer circuit in integrated form on 0.025 inch thick alumina substrate. All conductors were gold plated. The RF input frequency was 6 GHz, the L.O. signal was at 2225 MHz and the output IF was in the vicinity of 4 GHz. As can be seen from the schematic Figure 3.6, the alumina substrate consists of two parts which lie on common metal base containing a ridge. The two alumina wafers butt against the ridge and connect to the gate and drain terminals of the beam-leaded FET package which is mounted, grounded source, on the ridge.[12] One of the wafers contains the input or R.F. circuitry which appears to the "left" of the FET in the schematic (Figure 3.6). The other wafer contains the 4 GHz I.F. circuitry.

The 'cheese-slice' bias feed DC circuits, use a high and low impedance transmission line sections in shunt with the principle R.F. circuitry.

The idea here is to reflect, through the $\lambda/4$ radial section and the $\lambda/4$ high impedance lines, an open circuit for the main R.F. lines. In actuality this circuit provides a broadband ($\Delta f = 2$ GHz) open at the main R.F. line, yet is an effective bias feed for the gate and drain voltages.

The d.c. lines are isolated from the outside by use of d.c. blocking capacitors. In this instance they are MIS beam lead 22 pf capacitors. The beam leads make for easy assembly using thermocompression bonding of these devices onto the substrate track. And at our frequencies of interest these blocks represent less than 1 ohm series impedance to the RF signal, yet are an effective D.C. block. The other end of the bias network is isolated by the use of 'filter-con' type connectors. Essentially they are a π type network, with capacitors shunting to ground. They provide a satisfactory low pass filter and allow for bias stability in the circuit.

The 2 GHz low pass filter has a cutoff frequency of $f_c = 2.6$ GHz, and is constructed using techniques detailed in H. Howe.[11] This is a Chebyshev type low pass with N = 7. The isolation at 2 LO (4450) and at 6 GHz is 20 and 30 dB respectively. This filter is used to inject the local oscillator into the gate, and by the isolation, also directs the 6 GHz signal into the gate.

The other half of the diplexer is the 6 GHz band pass filter,[11] using half wave side coupled resonators. The centre frequency is 6200 MHz with Δf = 1000 MHz. The design is a three-section Chebyshev with isolation of 25 dB at the LO (2225 MHz), and 45 dB at 2 LO (4450 MHz).

The gate matching circuit is then designed such that the 50 ohm output of the diplexer is a practical interface

Due to the extreme difficulty in S-parameter characterization (see Appendix C) of the FET under mixer operating condition, the initial gate matching circuit was chosen similar to that for a single stage 6 GHz amplifier input matching circuit. The design for the partially matching circuits for the input and output, were based on the manufacturer supplied data. See Appendix B. As indicated elsewhere, this approach was intended, at best, to provide a first iteration, and no significant data on 'mixer-bias' FET parameters were available. The manufacturer has, of course, provided small signal FET S-parameters in an amplifier operation. This design was then optimized, empirically, for lowest noise figure, consistent with good gain flatness.

The drain matching circuit was similarily difficult to calculate analytically. The problems of S-parameter characterization led to an initial design of the drain matching circuit which was similar to the 4 GHz single-stage amplifier output match circuit. This design was then optimized, empirically, for good gain and gain flatness.

The matter of providing proper reactive termination to the other mixer products, as discussed earlier is the next design constraint. Usually the 25 dB isolation of S_{12} isolates the gate from the mixer products present at the drain. And these are uncontrollably terminated in the reverse direction. The output circuit has to have some filtering to suppress the L.O. signal from straight forward amplification. A quarter wavelength long stub (at 2225 MHz) at the output placed $\lambda/4$ (at 2225 MHz) away from the drain terminal of the FET, acts as a short circuit when rotated back to the drain. This reflects the L.O. and its odd order harmonics back into the transistor for some form of L.O. recovery. The mixer also produces the 6 GHz output signal which is amplified and outputted. Also produced are the sum and image frequencies and 2xL.O. signal (4450 MHz) frequencies. For optimum conversion gain, a reactive termination equal to the broadband complex conjugate impedance at these spurious frequencies is needed. To analytically design this is too major a task, and the design is generally empirically tuned for maximum gain. It is assumed that some signal energy reconversion takes place, however (see Appendix C), as the gain achieved is less than calculated, it is also assumed that significant signal energies are lost in these spurious signals. The mixer does need external filtering in the form of a 2xL.O. (4450 MHz) notch filter and a 4 GHz bandpass filter. This testing detail is discussed in the next chapter.

CHAPTER 4

EXPERIMENTAL TECHNIQUES AND RESULTS

4.1 Introduction

The intention of this Chapter is to describe the techniques used to measure the mixer of Chapter 3.3 and to present the results. The performance of a microwave mixer is measured in terms of its three major parameters. These are the conversion gain (and the gain-flatness, defining the bandwidth), noise figure, and carrier-to-intermodulation ratio. The conversion gain equation developed in Chapter 2, has a band pass, frequency dependent shape factor, and the results presented show a marked band pass response. For this measurement of gain, the LO and signal power were carefully calibrated, and with all necessary filtering the 'true' response was measured. Obviously, the circuit had conversion gain!

The noise figure theoretical analysis in a GaAs MESFET mixer is complicated, because the correlation between the intrinsic drain noise and the induced gate noise cannot be neglected, and is also a time-varying function. Thus the analysis, based mainly on Pucel's[1] work, is briefly developed. Appendix D, presents the detailed equation derivation. The actual measurement technique and set up are shown, and a discussion of the microwave measurements is presented.

The results presented, consider the sensitivity of the mixer to gate and drain bias and to the local oscillator pump level. The mixer tuning is empirical, and optimized for a particular set of conditions. The constraints on the set of bias and pump levels are either minimum noise figure or maximum gain. In all case, gain flatness is a co-requirement, as ripple degrades the carrier to intermodulation performance. Finally, results versus temperature are presented, and hold promise for dramatic performance improvements or new systems applications of the FET mixer.

4.2 Noise Figure Measurements

Noise in a microwave FET is produced by sources intrinsic to the device;[2] [3] by thermal sources associated with the parasitic resistances, i.e., the gate metallization and source and drain contact resistances, and by extraneous sources arising from defects in the semiconductor material such as traps. The spectrum of the intrinsic noise is flat, i.e. white noise, extending well beyond the microwave band. The trap noise, generally, shows a rapid drop with frequency, often exhibiting 1/f - character. As such it is more pronounced in the IF (below 100 MHz) frequency band than in the signal band.

The basic principle of operation of the field-effect transistor was first described by Shockley,[13, Ch.2] who assumed a constant mobility throughout the conducting channel regions. Var der Ziel, in a series of classic papers; used Shockley's model to derive the small-signal parameters and intrinsic noise properties of the FET.[4] Van der Ziel showed that the intrinsic noise is thermal in origin, and can be represented by two white noise generators, one in the drain circuit, and one in the gate circuit. The gate noise generator, which represents the noise induced on the gate electrode by the passing fluctuations in the drain current, is partly correlated with the drain noise generator.

The constant mobility model of Shockley and Van der Ziel, though applicable to long-gate devices, does not apply to microwave devices whose

gate lengths are in the micron range. For these devices, when biased in the current saturation regine, the average value of the longitudinal dc field in the channel is in the range where the mobility is a decreasing function of the field, and indeed, where the carrier velocity is approaching a constant ("saturated") value. Consider, for example, a typical case of a GaAs FET with a one micron gate operating with a drain voltage of 3V. The average longitudinal channel field is 30KV/cm, approximately ten times the threshold value at which the velocity begins to saturate. Thus, the effects of velocity saturation must be included in any model of a GaAs FET designed for micro-wave operations.

Velocity saturation within the channel not only modifies the small-signal parameters, but the noise performance as well. Many workers have introduced some aspects of velocity saturation into their FET models, though none of these models include the diffusion noise introduced by electrons experiencing velocity saturation, or the effect due to the intervalley scattering of the electrons from the low mobility to the high mobility valleys.[7] Statz[6] has derived the small signal noise behaviour of the FETs, taking into account the saturation velocity behaviour and the high field diffusion noise (this is the dominant intrinsic noise of microwave GaAs FETs).

Based on the above introduction, a brief development of the noise figure model will be given. This is based on Statz's[6] and Pucel's [1],[10] work.

Thus we have:

(i) Thermal noise, caused by the random motion of the carriers in a conduction medium. The noise voltage or current generated by a conducting medium with a resistance Rg at a temperature T and in a small bandwidth B is given by

$$\bar{v}^2 = 4kTBRg \text{ (Nyquist's theorem)} \quad (4.1)$$

$$\bar{i}^2 = 4kTB/Rg \quad (4.2)$$

where k = Boltzman's constant and

$\bar{v}^2$ and $\bar{i}^2$ are the mean square noise voltage and current respectively.

(ii) The shot noise is caused by the discreteness of the charge carriers and the random fluctuations in the number available for conduction at any given time. The shot noise current resulting from a dc current I flowing is given by

$$\bar{i}^2 = 2q\bar{I}B \quad (4.3)$$

where q = the electronic charge.

(iii) The 1/f noise can be attributable to

(a) carrier trapping at crystal dislocations,

(b) formation of an additional depletion region on the channel surfaces resulting from surface contamination, and,

(c) the generation and recombination of the carriers in the space charge region.[8]

1/f noise can be minimized by passivation of the FET surface and by having a buffer layer between the active epitaxial layer and the semiconductor substrate. In our case, the NE244 device has both a SiO_2 passivation as well as an intrinsic buffer layer. And more over, as can be seen from Figure 4.1, showing data from three separate studies on 1/f noise, at our frequencies of interest 1/f noise is not a significant factor in contributing to the overall mixer noise figure.

Following Pucel,[10] Figure 4.2, shows the equivalent circuit noise model of a GaAs MESFET, for the frequency range beyond 1/f noise. The average noise current, i_{nd}, represents the thermal channel noise, and is expressed (based on transmission line properties) as:

$$\overline{i_{nd}^2} = 4\,kTB\,g_m \left[P(V_{gs}, V_{gd}) + S(\omega C_{in})^2 / g_m \right] \tag{4-4}$$

where P is a factor dependent on the gate to source, V_{gs} and gate to drain, V_{gd} voltages

S is a constant also dependent on V_{gs} and V_{gd}

C_{in} is the input gate circuit capacitance, and,

g_m is the saturation transconductance.

For mixer applications, the FET is usually operated in the saturation region. The limiting values for P and S, as given by Pucel is:[10]

$$P(V_{gs}, V_{gd}) = 2/3 \tag{4-5}$$

and $S(V_{gs}, V_{gd}) = 0.15$ for $V_{gd} = V_p$ = the pinch off voltage (4-6)

Thus the mean squared drain noise current $\overline{i_{nd}^2}$ at the IF frequency is then expressed as:

$$\overline{i_{nd}^2(\omega_o)} = 4\,kTBg_m\,(2/3 + (\omega_o C_{in})^2\, S/g_m) \tag{4-7}$$

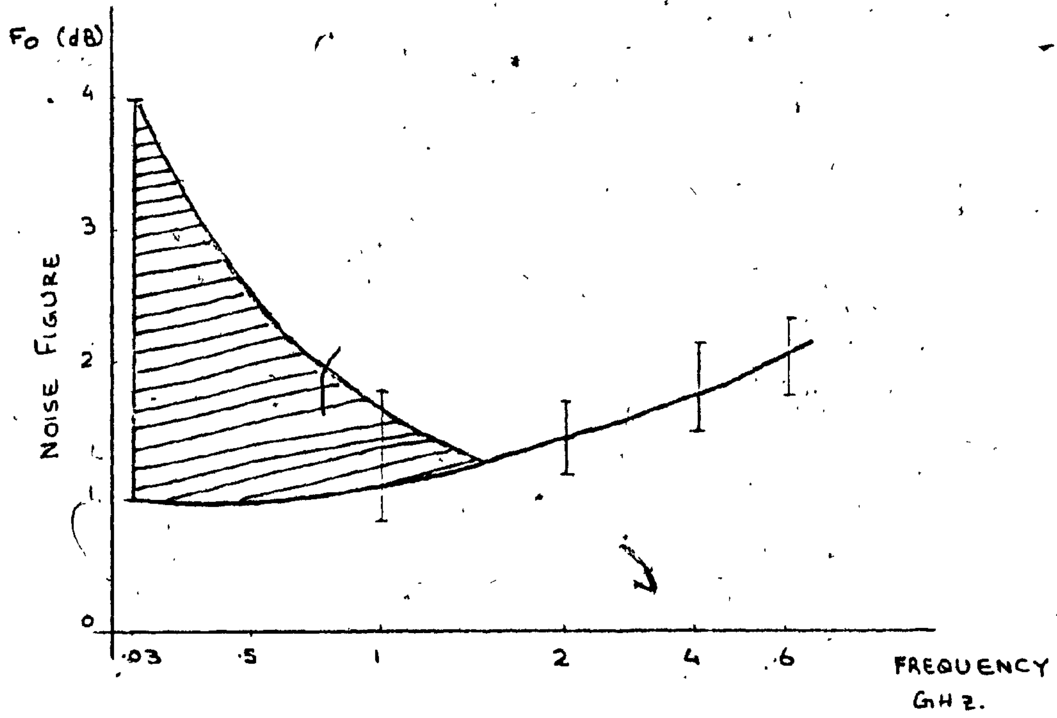


Figure 4.1: MESFET 1/f Noise

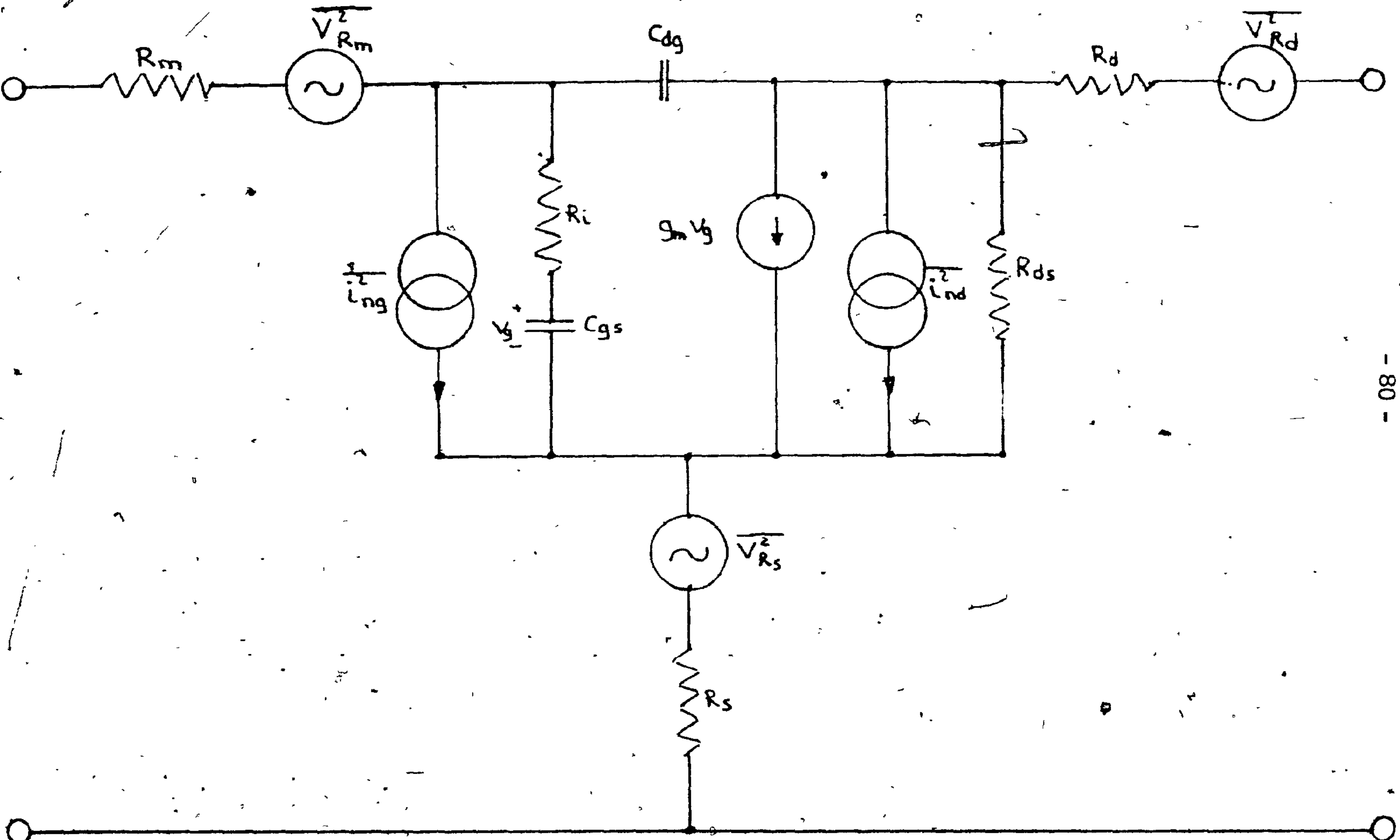


Fig. 4.2 Noise Figure Model of the FET

And the gate mean square induced noise, from Pucel,[10] is given by:

$$\overline{i_{ng}^{2}} \; (\omega_s) = 4kTB \; (\omega_s C_{in})^2 / g_m R \qquad (4\text{-}8)$$

Where ω_s is the RF signal frequency, and ignores the LO signal noise contribution, also ignored are the noise sources at the spurious mixer frequencies. The lengthy calculations are duplicated in Appendix D, and the result is presented here for the minimum noise figure

$$F_{min} = 1 + 2G_n \; (\text{real} \; (Z_{cor}) + R_g \; (\text{opt}) \;) \qquad (4\text{-}9)$$

$$\text{where } G_n = \frac{gd \; R_{ds}^{2}}{Z_{21}^{\;2}} \qquad (4\text{-}10)$$

Z_{cor} = the FET mixer correlation impedance

$$= \frac{Z_{11} - j\,C\,(R_i - jX_s)\,Z_{21}\,(g_n/g_{dn})^{\frac{1}{2}}}{R_{ds}} \qquad (4\text{-}11)$$

$R_g(\text{opt})$ = optimum source impedance

$$= (\text{Real} \; (Z_{cor}) + R_n/G_n)^{\frac{1}{2}} \qquad (4\text{-}12)$$

The experimental setup for the FET mixer with drain injected local oscillator is shown in Figure 4-3 with Table 4.1 giving the list of equipment used.[11]

Some of the equipment and terms used are defined below:

(1) Clean and stable RF signal generator, implies that the microwave signal source should have sufficient filtering such that the signal being injected into the FET drain is essentially a single frequency signal. There are no measurable sidebands or harmonics. The signal generator should also be stable with respect to time, and drift in frequency of the applied local oscillator signal should be

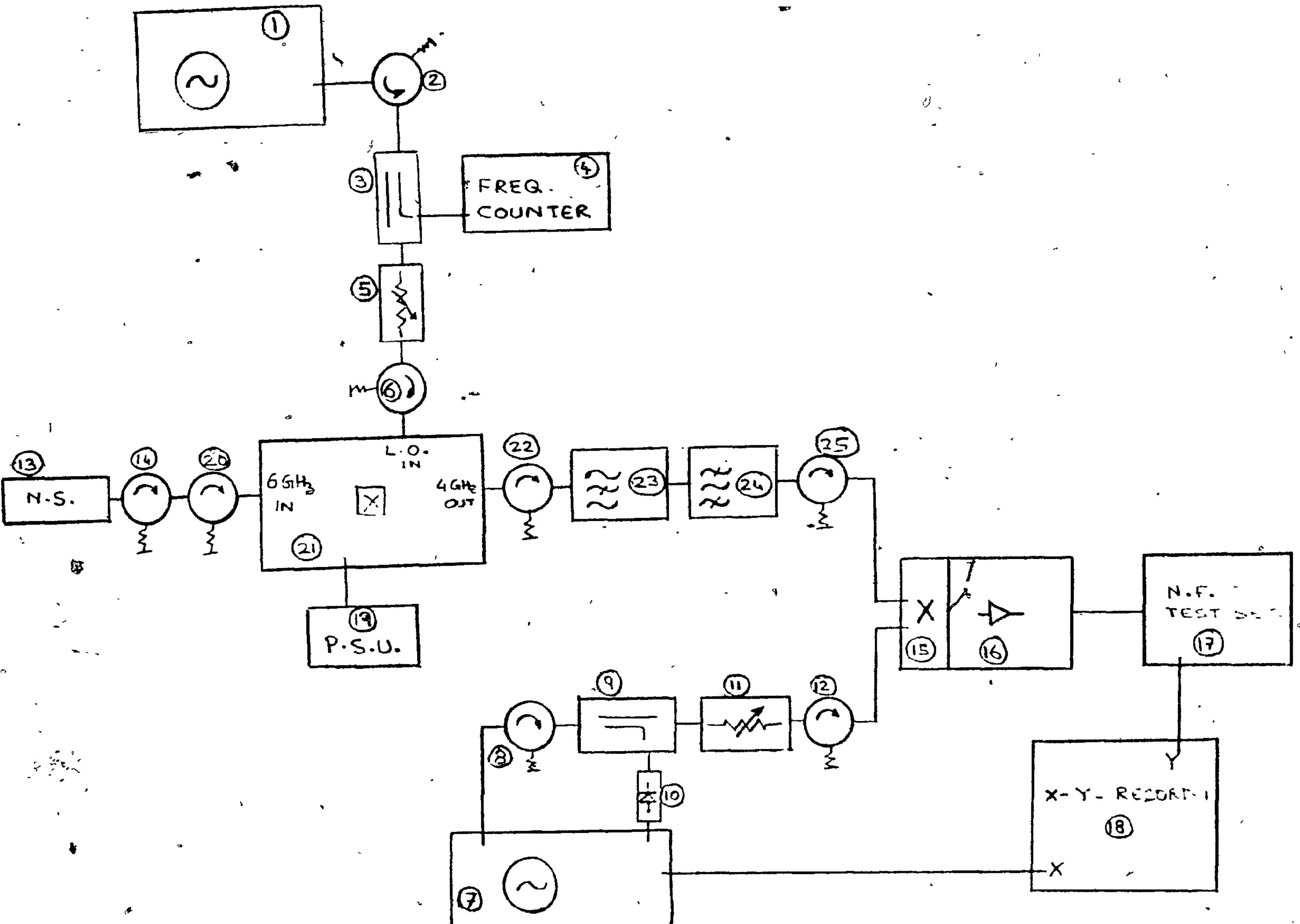


Figure 4.3 Noise Figure Setup

TABLE 4.1: LIST OF EQUIPMENT FOR FIGURE 4.3

#	Description	
1	Clean and stable RF signal generator (+16 dBm O/P power) 2 to 3 GHz frequency range	FET mixer local oscillator power circuit
2	2 GHz Coax isolator	
3	10 dB 2GHz Coax directional coupler	
4	Frequency counter, 2 to 3 GHz range	
5	2 GHz variable microwave attenuator	
6	2 GHz coax isolator	
7	Clean and stable RF sweep generator (+10dBm O/P power) 3 to 5 GHz frequency range	Noise figure test set load oscillator power circuit
8	4 GHz coax isolator	
9	10 dB 4 GHz coax directional coupler	
10	Detector diode for automatic sweep levelling of generator	
11	4 GHz variable microwave attenuator	
12	4 GHz coax isolator	
13.	Solid state noise source - calibrated	Noise figure test set
14	6 GHz coax isolator - calibrated	
15	4 GHz noise figure test set mixer	
16	Noise figure test set preamplifier	
17	Noise figure test set control box	

Table 4.3 Mixer Operating Conditions

	V_{DS}(v)	V_{GS}(v)	I_{DS}(mA)	L.O.(dBm)
- Absolute Maximum Ratings	5.0	-10.0	100	-
- Operating point for best Gain Frequency response	4.0	-4.0	6	+11

Note: The L.O. injection filter has 1.0 dB loss, thus actual Local Oscillator drive required at the gate is +10 dBm.

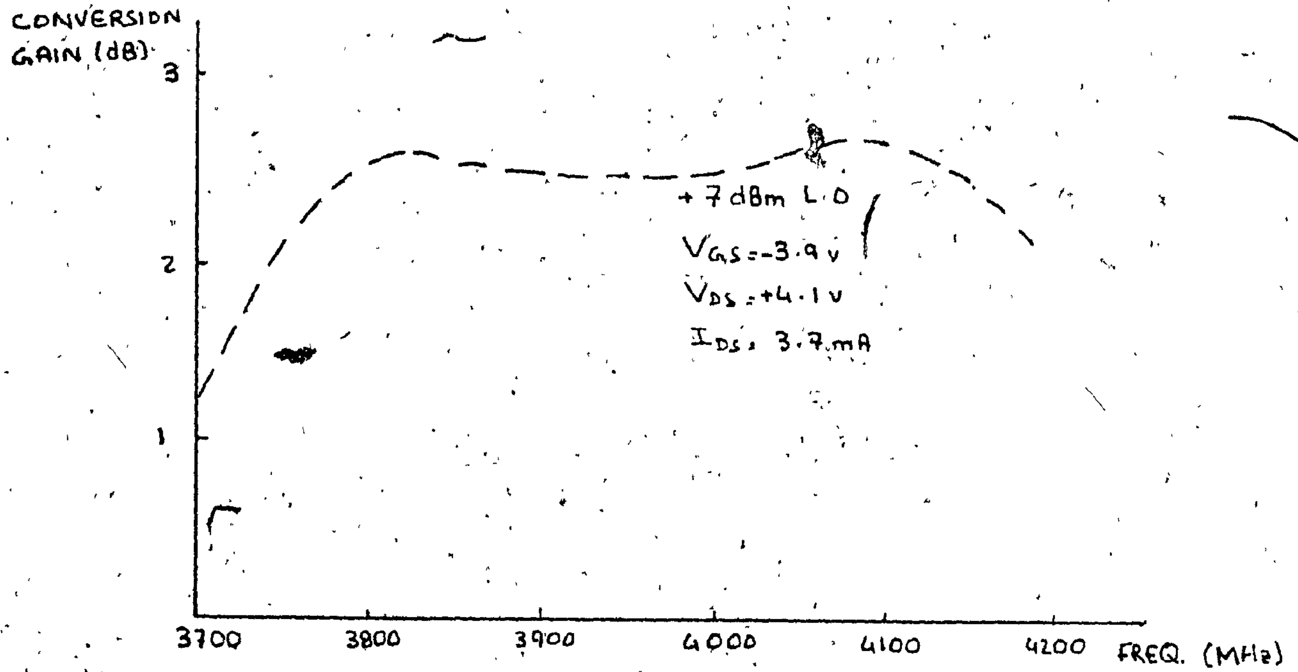


Figure 4.5: Gate Mixer Gain Frequency Response.

Figures 4.6, 4.7 and 4.8 show the sensitivity of the Gain frequency response to the Gate Bias, and local oscillator drive level.[15] Figure 4.9 shows the $2 f_s - 4 f_{LO}$ level compared to the output signal level. Note, this is done with the input signal equal to -25 dBm, and in a satellite receiver the expected operating level is -40 dBm. This should result in 15 dB better carrier to spurious (intermod) ratio. As can be seen, the spurious is completely suppressable by minor bias adjustment. The Gain, and gain flatness are minimally affected.

Figure 4.10 shows mixer response over temperature, and as can be seen, gain improves linearly with temperature. This can have a useful application in automatic receiver gain temperature compensation schemes, or in general lower noise receiver applications. These ideas are discussed further in the next section. Figure 4.11 and 4.12 show the noise figure measurement results and the actual corrected data is presented in Figure 4.13. This graph was calculated using the formula detailed in the text above, (4.14) to correct for the reference noise figure and input circuit losses. The operating bias for best gain and best noise figure, are, as usual, not the same.[16]

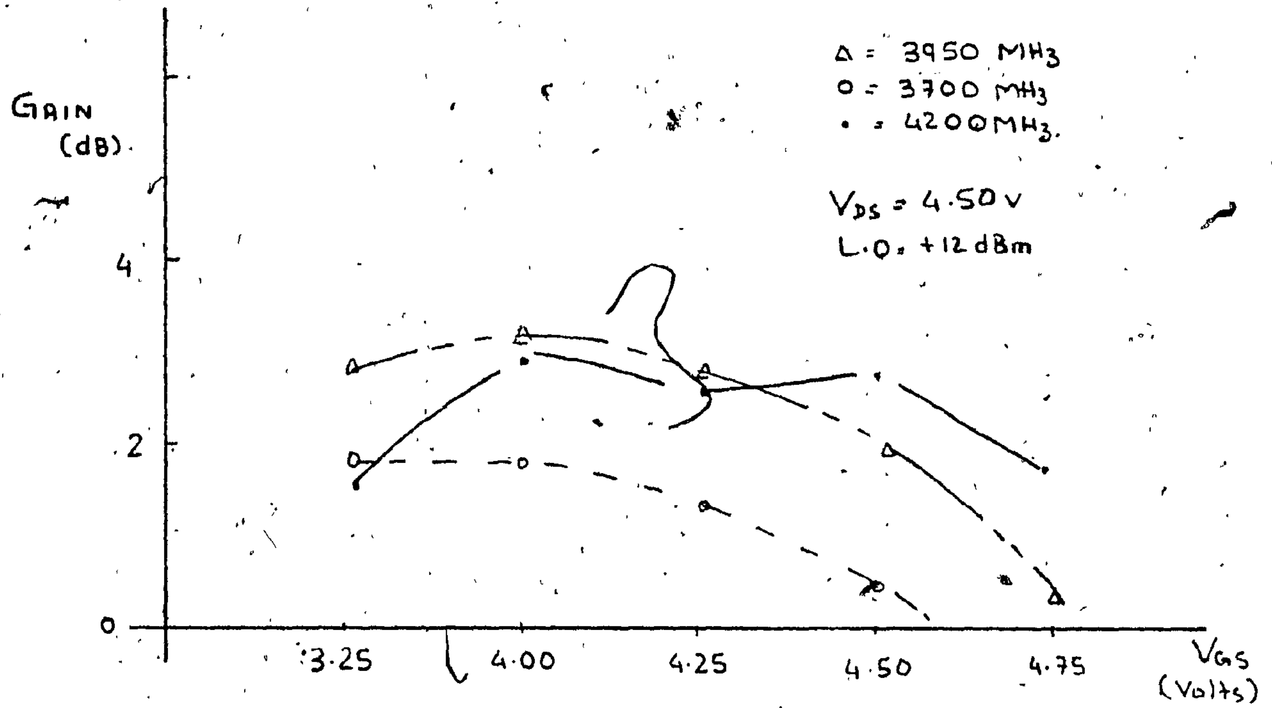


Figure 4.6: Sensitivity of Gain Frequency Response to Gate Bias

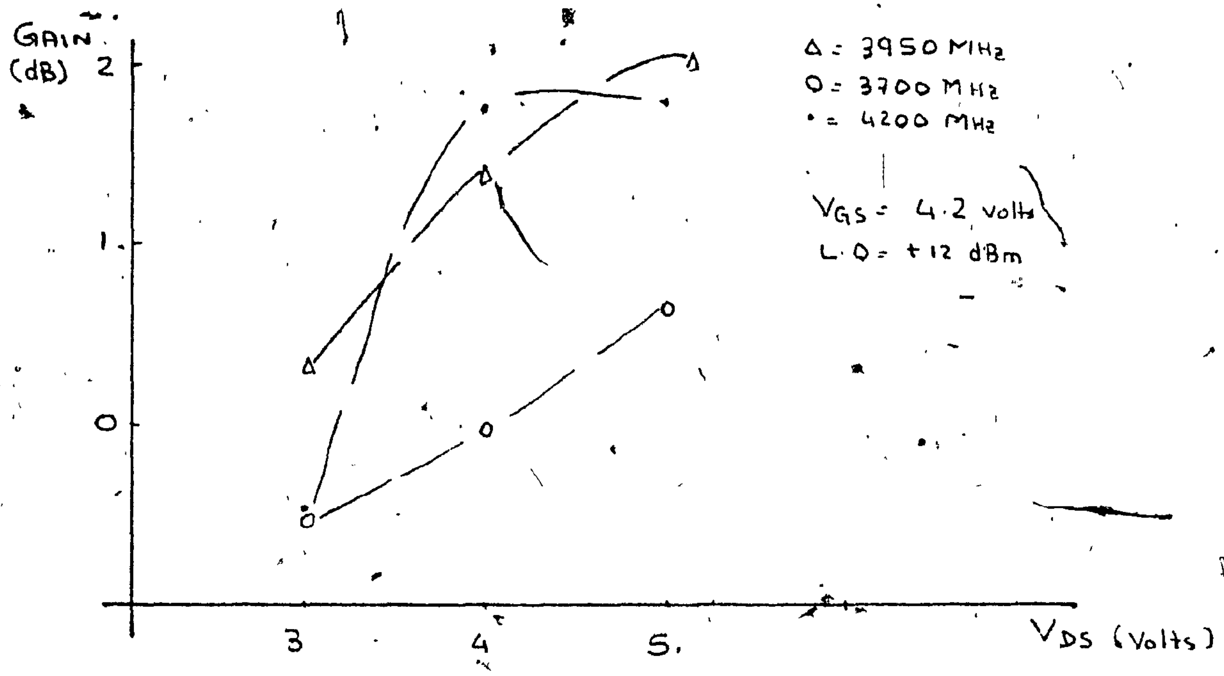


Figure 4.7: Sensitivity of Gain Frequency Response to Drain Bias

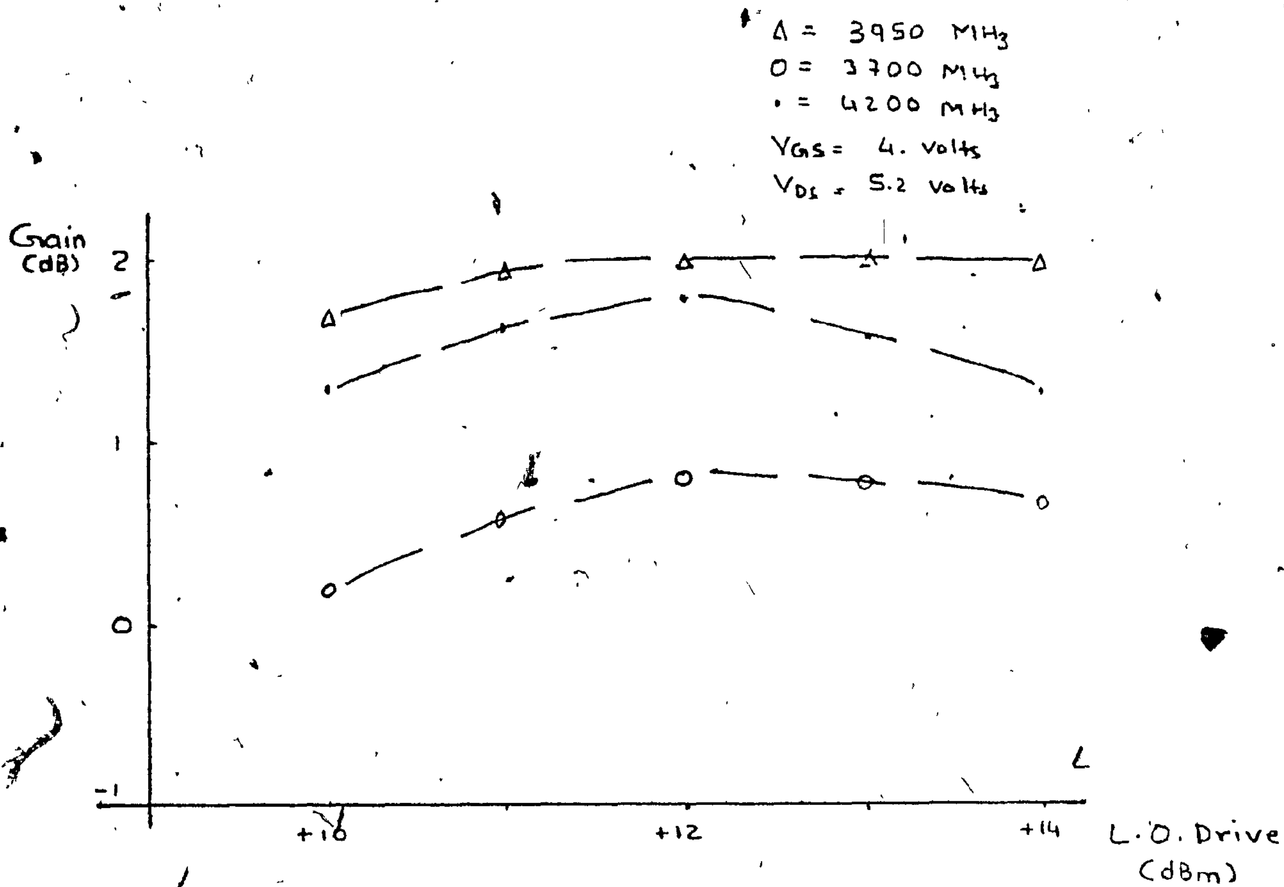


Figure 4.8: Sensitivity of Gain Frequency Response to Local Oscillator Drive

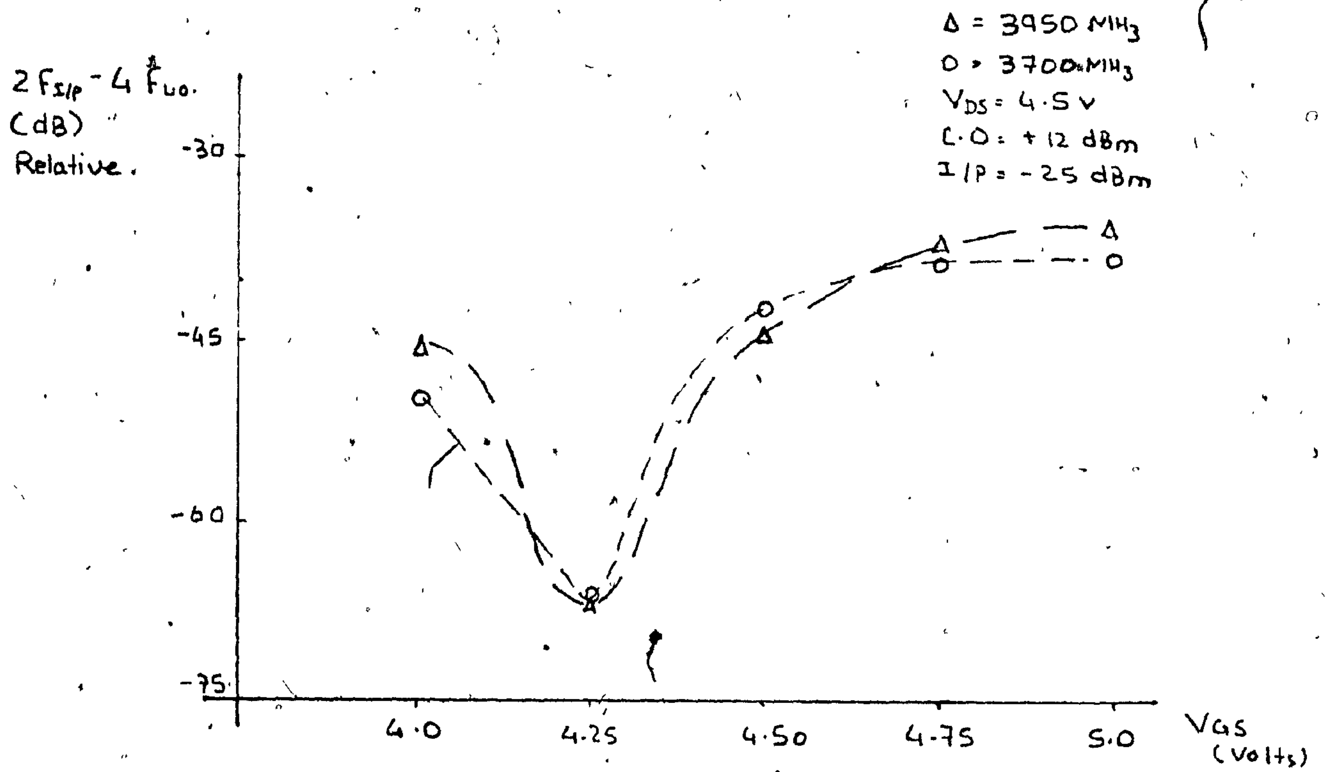


Figure 4.9: Sensitivity of the $(2 f_s - 4 f_{LO})$ Spurious to the Gate Bias

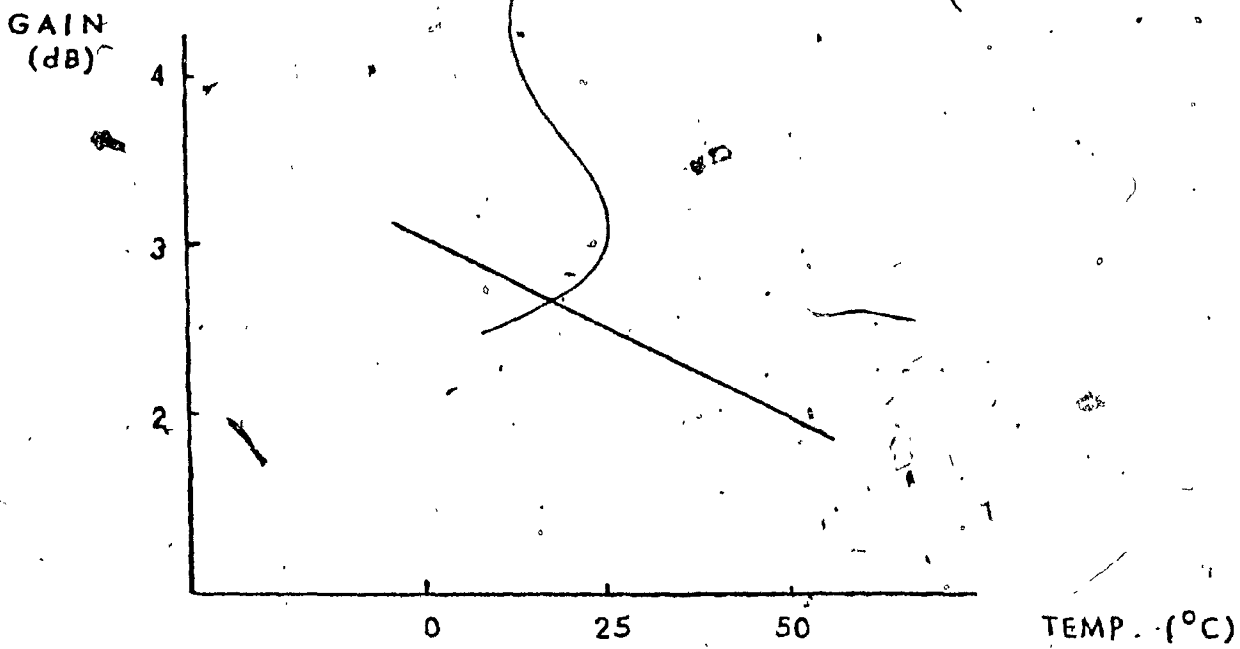


Figure 4.10: Mixer Gain versus Temperature

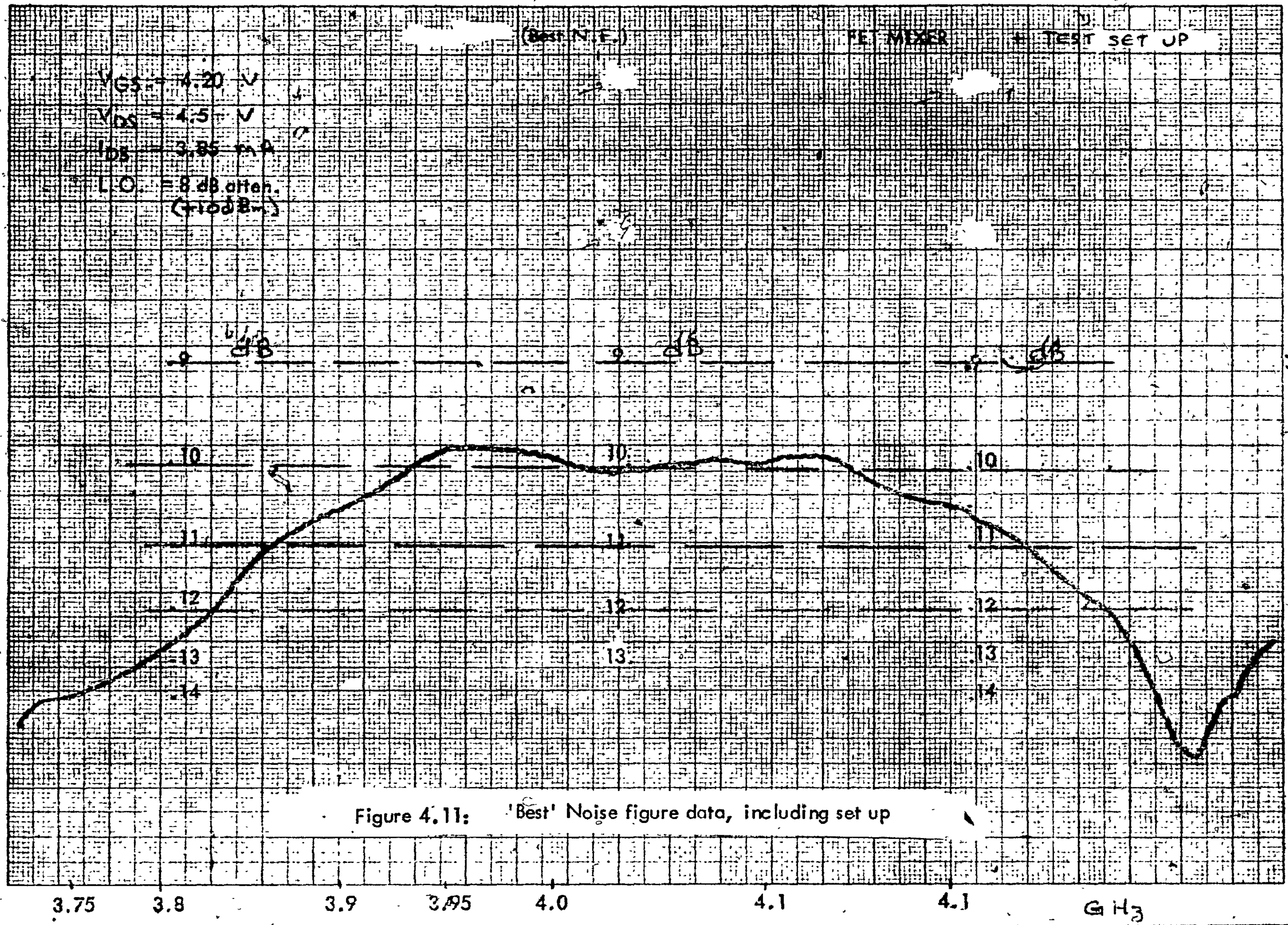


Figure 4.11: 'Best' Noise figure data, including set up

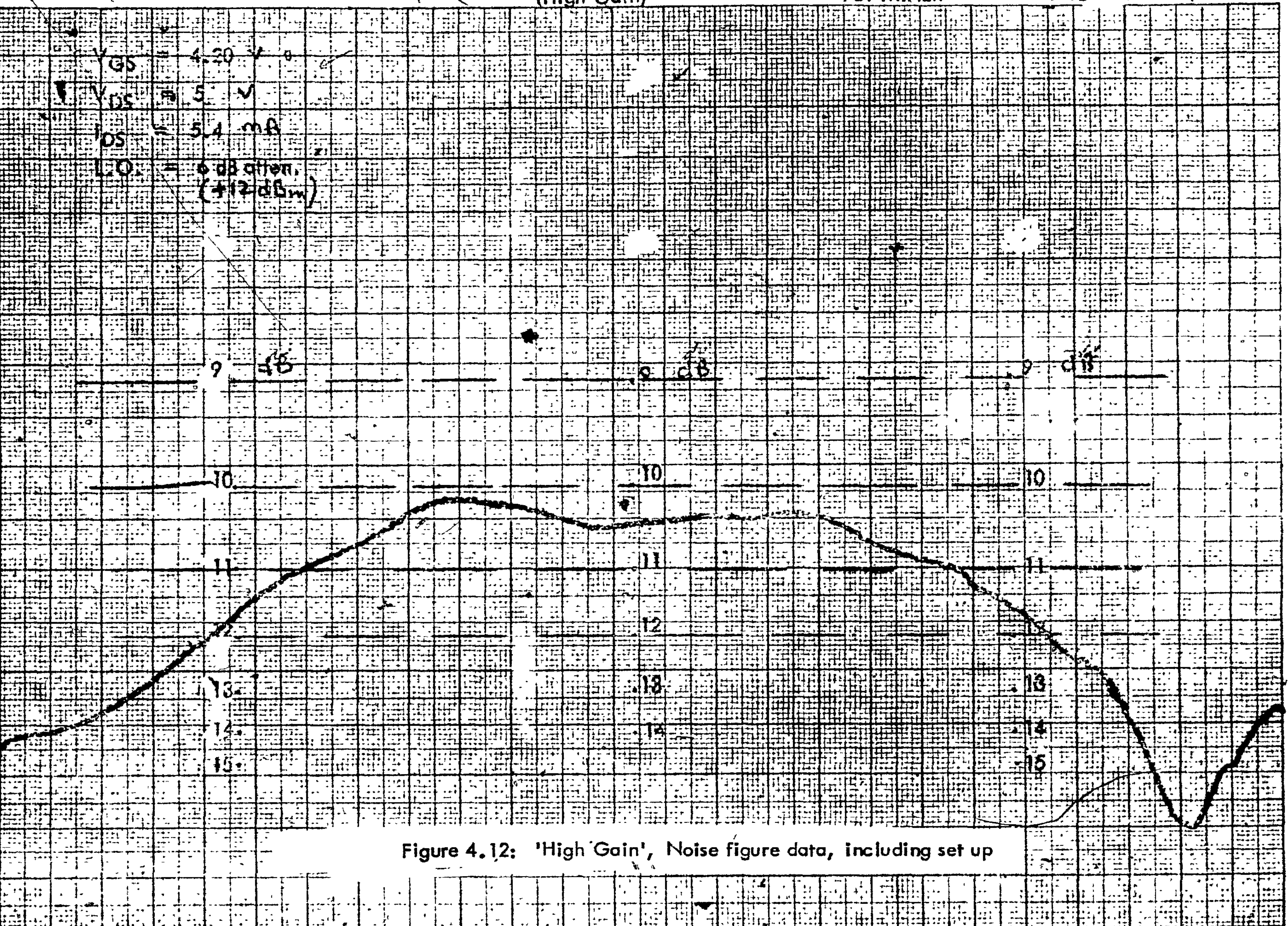


Figure 4.12: 'High Gain', Noise figure data, including set up

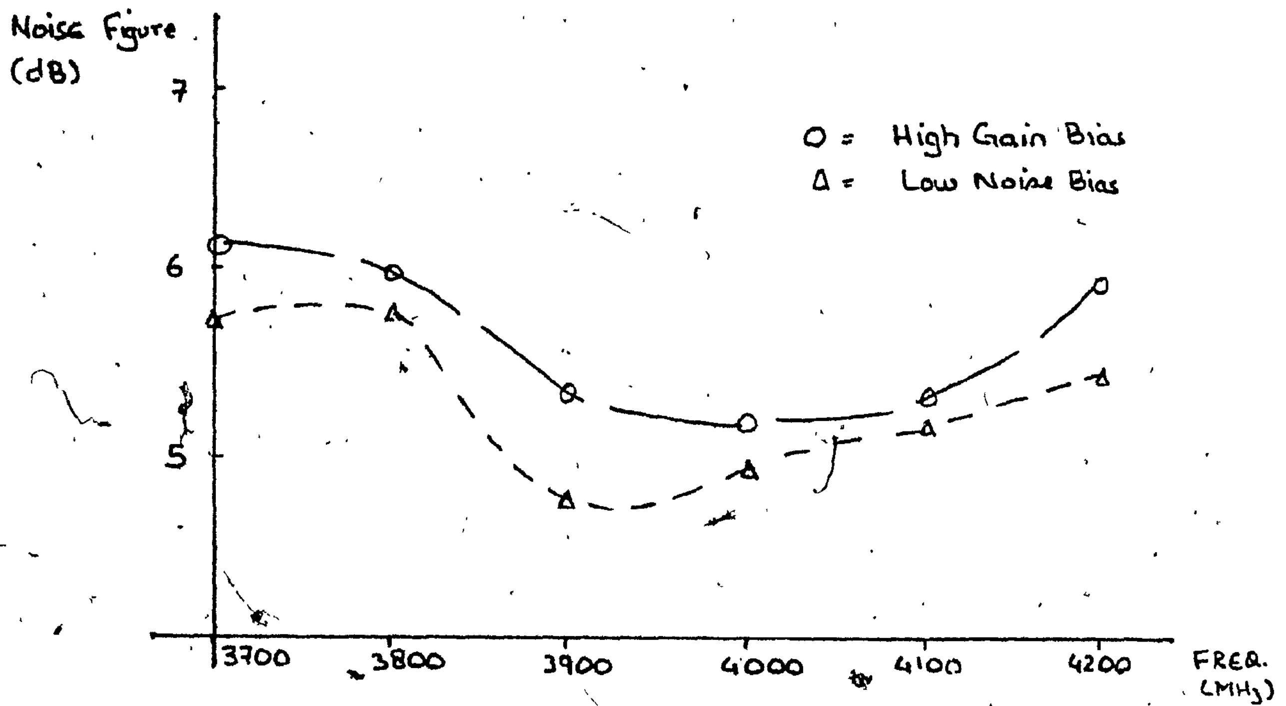


Figure 4.13: Noise Figure versus Frequency

4.5 Topics for Further Research

This section is a synopsis of new ideas regarding FETs and their circuit application as mixers for microwave communications. These new trends in device fabrication, and satellite configuration have promises of still further performance improvements. Thus the ideal FET mixer will contain the latest of these ideas.

Some of these are discussed below:

i) The results presented were based on a NE24406 packaged MESFET. This has a 1 μm long and 300 μm wide aluminum gate, with 1 μm gate-to-drain and gate-to-source spacing. Epilayer is 0.4 μm thick with 1.5×10^{17} cm^{-3} doping density and a buffer layer is used between the epilayer and the substrate. The ohmic contacts use Au-Ge/Pt metallization and Ti/Pt/Au metallization is used for the bonding pad. The latest state-of-the-art devices (17) have a 0.2 μm long gate. And although the gate metallization is still aluminum, a high reliability intermetal structure is used before the gold bond wire. This device, fabricated using ion implementation has an active layer doping of 5×10^{18} cm^{-3}. The overall effect is higher frequency of operation (for use in the 14/12 GHz satellite system) and at low frequencies results in lower noise figure and higher associated gain. Figures 4.14[18], 4.15[18] and 4.16[18] show the variation of Gain and Noise Figure versus gate length, doping density, N_D, and channel thickness. This shows that at each frequency of operation it is possible to optimize the device

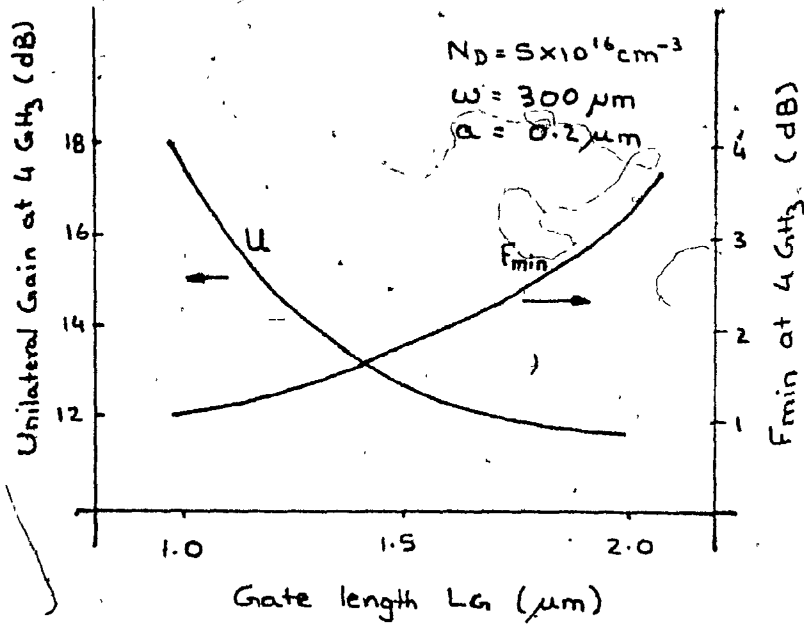


Figure 4.14: Calculated Gate-Length dependance on the Unilateral Power Gain and minimum Noise Figure at 4 GHz

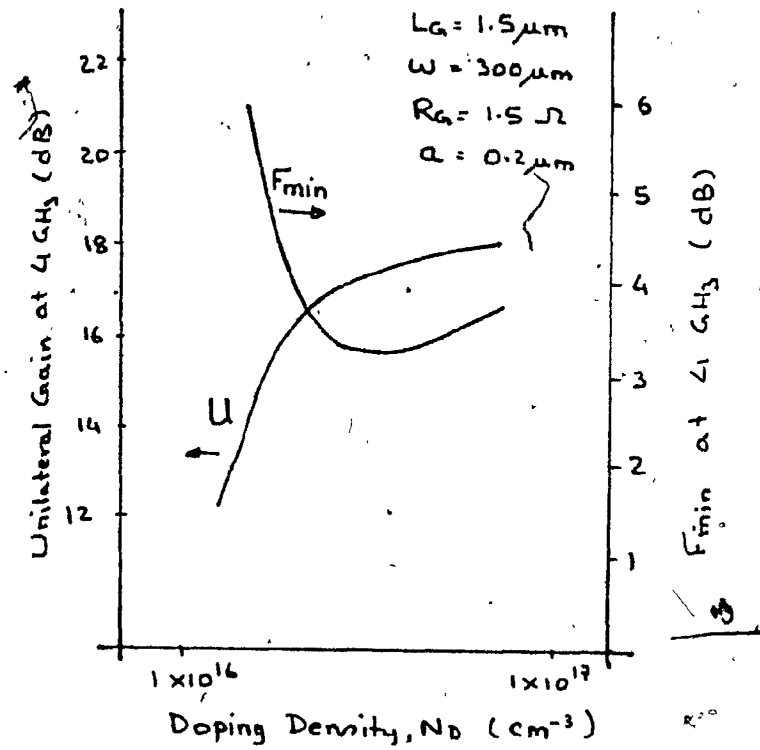


Figure 4.15: Calculated Doping Density dependance of the Unilateral Power Gain and minimum Noise Figure at 4 GHz

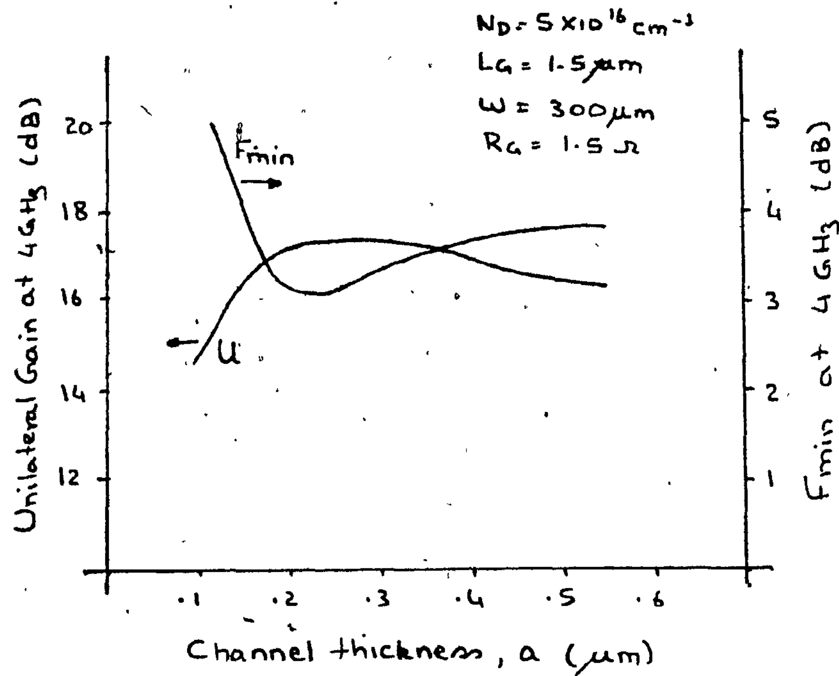


Figure 4.16: Calculated Channel-Thickness dependance of the Unilateral Power Gain and minimum Noise Figure at 4 GHz

parameters, such that improved performances are possible.

ii) The mixer was designed and tested for room temperature operation. The results showing performance versus temperature in Figure 4.10 show that gain improved with cooling. This trend is also true for noise figure, that is, noise figure improves with cooling. This is especially important at higher frequencies when package parasitics reduce performance limits. Recent results on amplifiers[19] have shown over 1.5 dB noise figure and 0.8 dB associated gain improvement with cooling from +25°C to -100°C. See Figure 4.17.[20] Of course, the problems of achieving (via radiation coolers) or designing (S-parameter data) for these temperatures are not trivial; the promise of such significant performance make it an important area of research. The published results show that for an amplifier, cooling below 150°K becomes rapidly ineffective and that operation in the 175 to 200°K area yields the biggest improvements in terms of noise figure versus cooling difficulty.

iii) As mentioned above, package parasitics contribute to performance limitations at the higher frequencies,[21] and especially for mixers certainly other configurations are desirable. These are, a self bias realizability, and a self oscillating configuration[22] for the FET mixer. Also possible is to inject the L-O into the drain.[20] Thus in the case of a 'drain-mixer', the L.O. is injected into the drain circuit with resultant modulation of the drain resistances between a low and high value corresponding to the saturated electron flow in the channel. (Figure 4-18).

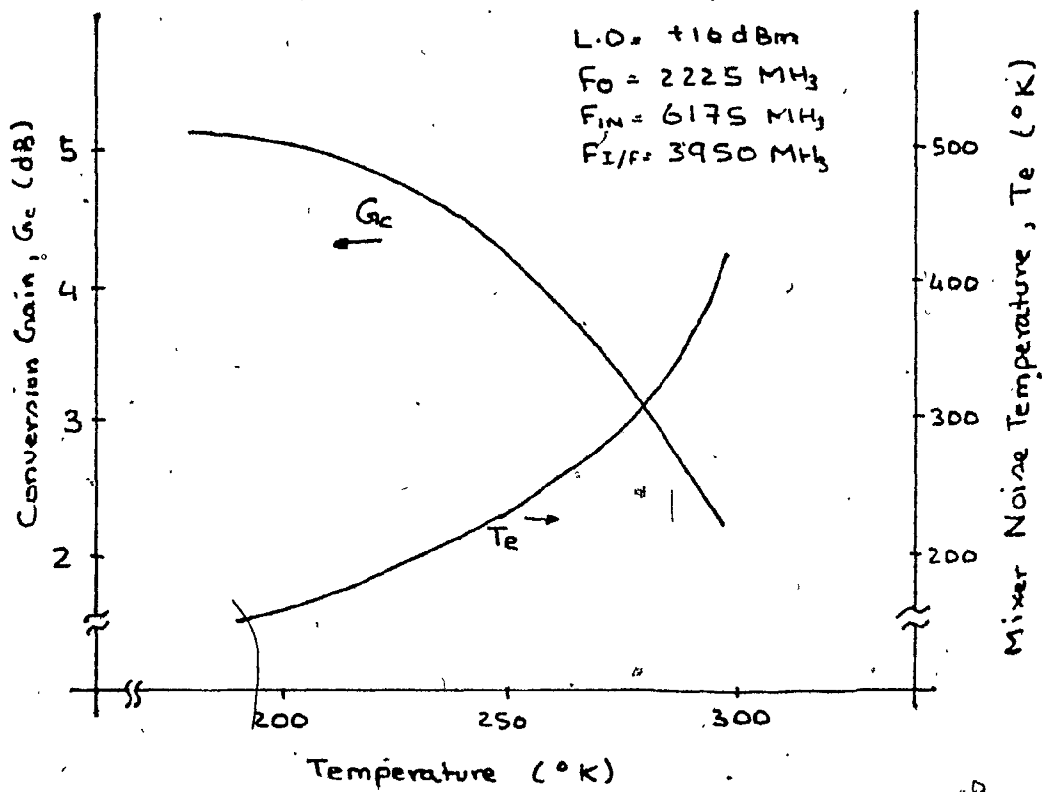


Figure 4.17: Variation of Conversion Gain and Noise Figure with Ambient Temperature

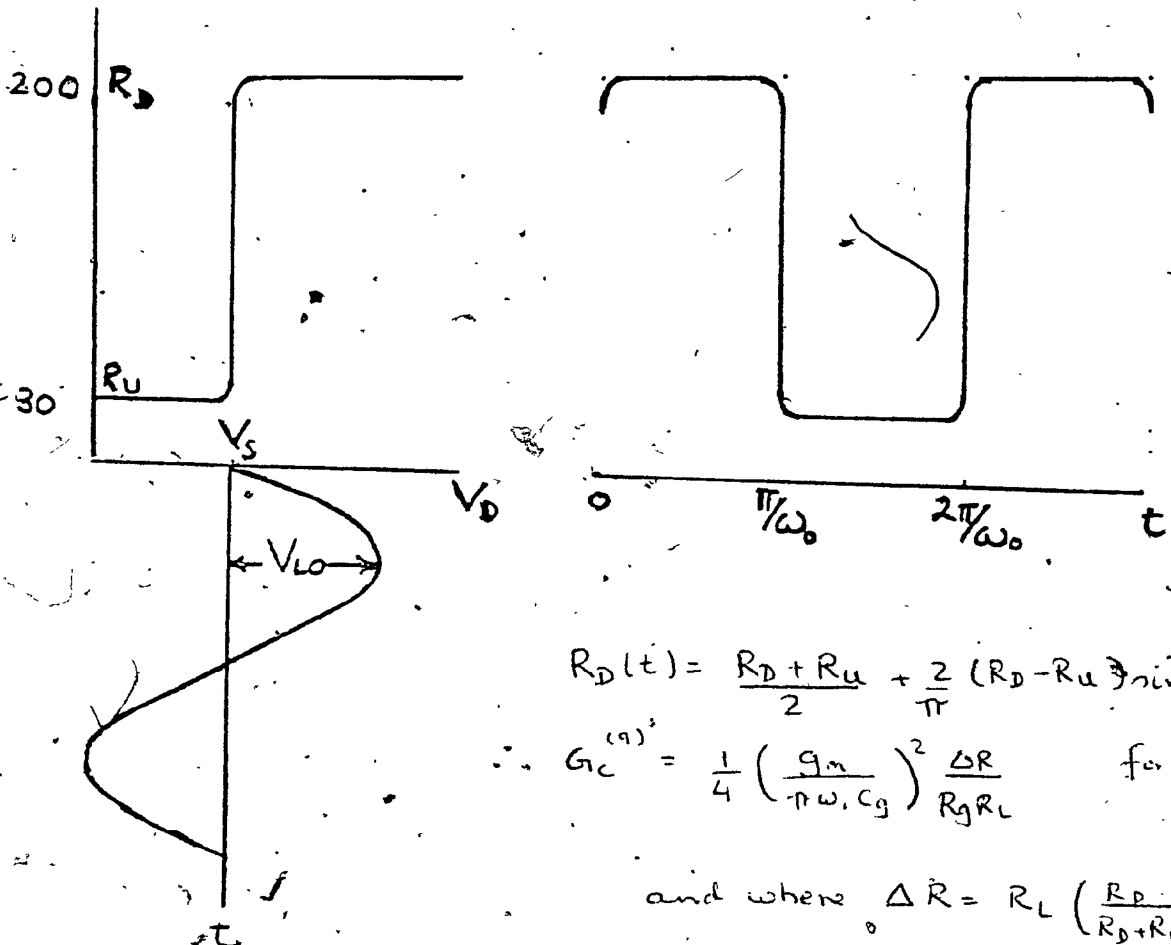


Figure 4.18 Generation of Time Varying Resistance in the Drain Circuit

An accurate estimate of the intrinsic conversion gain is more difficult to this case as both the resistance and the transconductance are modulated. However, it can be reasoned that the drain mixer will yield a considerably lower noise figure, probably due to the parametric upconversion of the low frequency noise in the FET to the output frequency, in the case of the gate mixer. With the gate Schottky-barrier remaining in the reverse bias condition over the whole of the L.O. cycle, the variation of the depletion layer width results in the corresponding capacitance modulation. In the drain mixer, very little gate capacitance modulation takes place.

Figure 4.19 shows a block diagram of the drain mixer. A low pass filter in the drain circuit are used to separate the L.O. and the output signal. Figure 4.20. This circuit is very suitable for low I.F. applications. Figure 4.21 and 4.22 show test results. However, the most significant new design is a dual gate FET. Until recently, most FET mixers were realized using devices designed for amplifier use; the design of the dual gate FET, is an indication that semiconductor engineers are catering to mixer designer demands. This type of FET is ideally suited for use as a gate mixer, where the input and L.O. are fed in at the separate gates. Perhaps a similar, multiple-drain, power FET is necessary for drain mixer realizations. It is clear that more investigation is necessary both in the device technology and the circuit techniques to realize more optimum mixer performance.

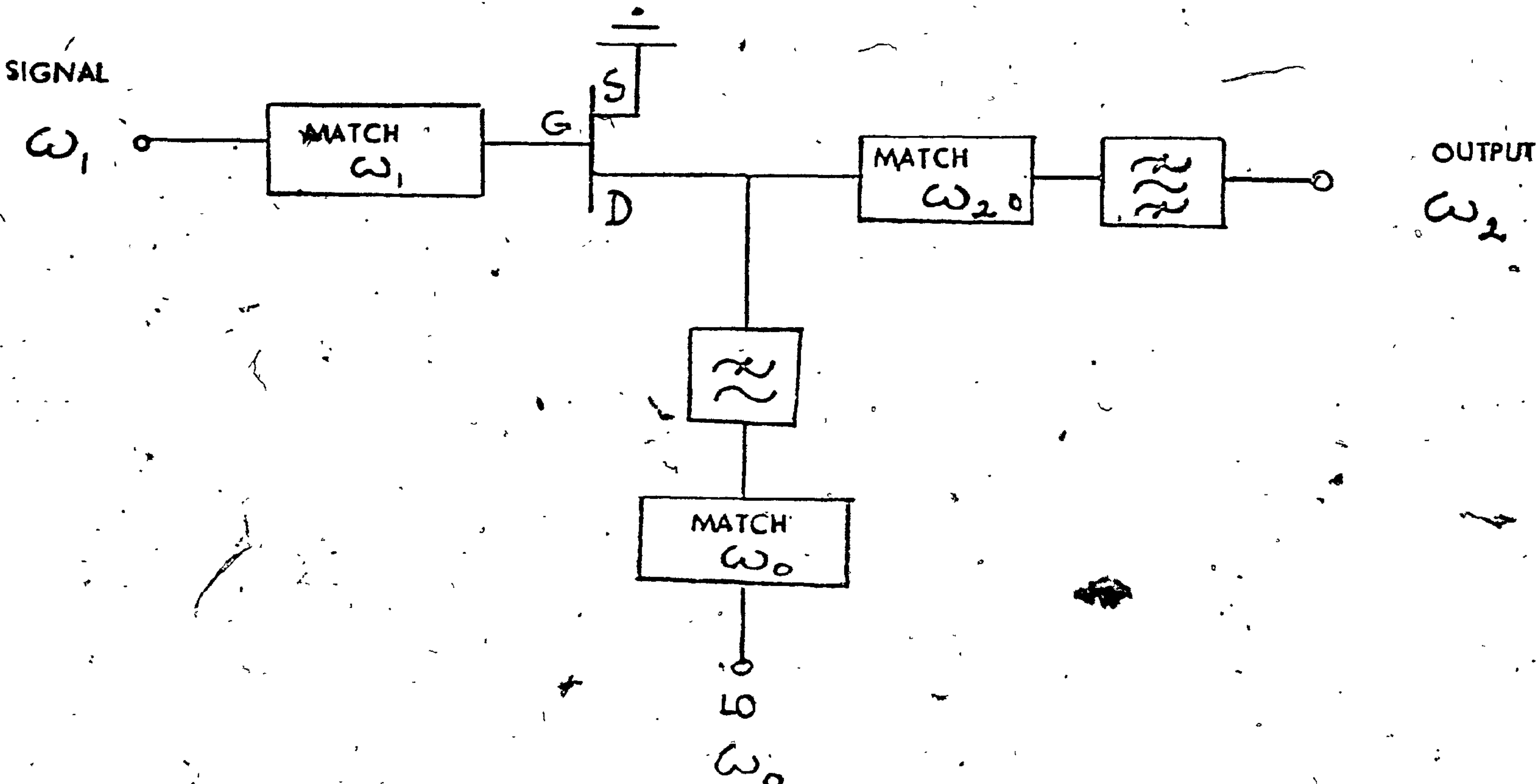


Figure 4.19 Block Diagram for a Drain Mixer

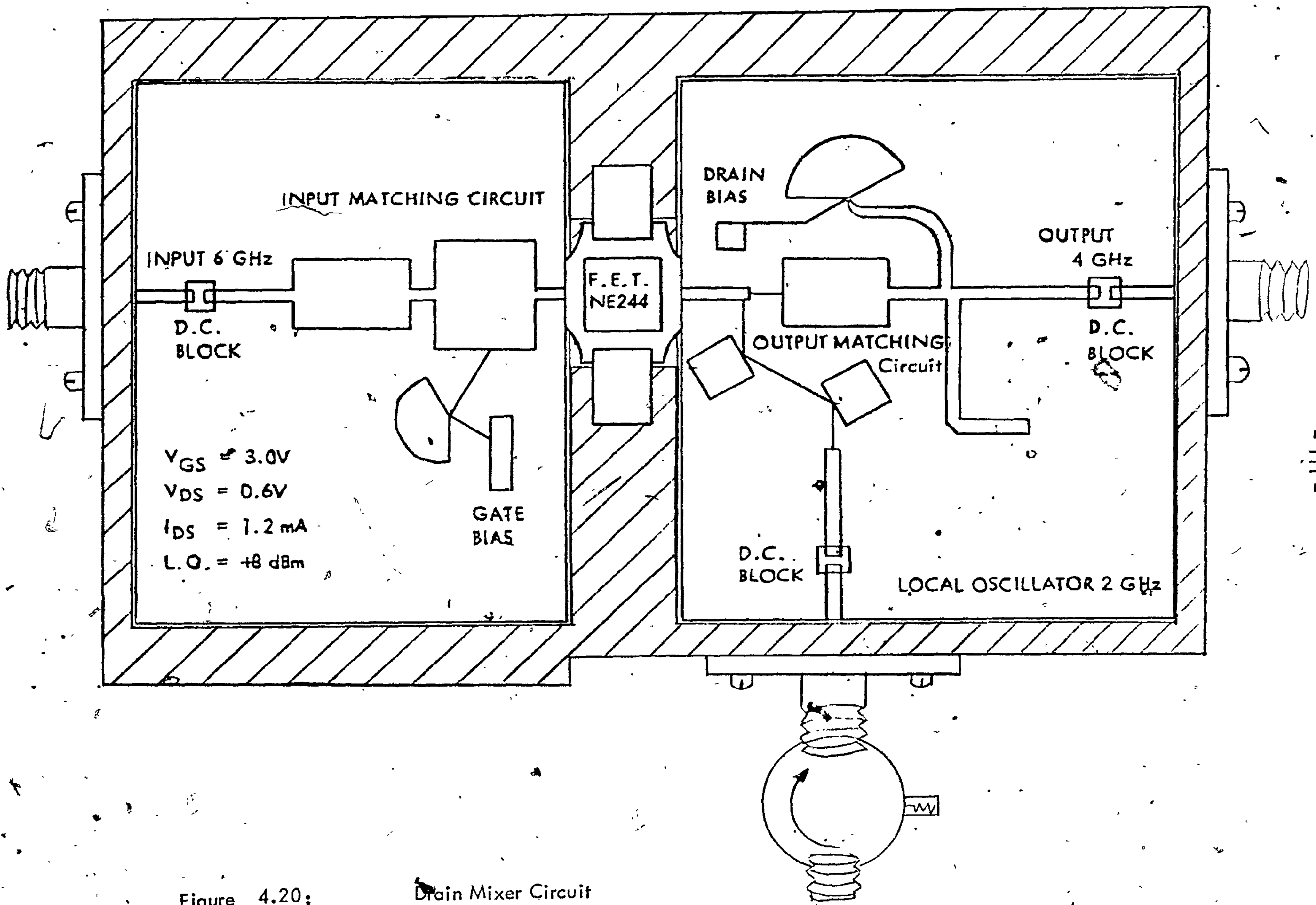


Figure 4.20: Drain Mixer Circuit

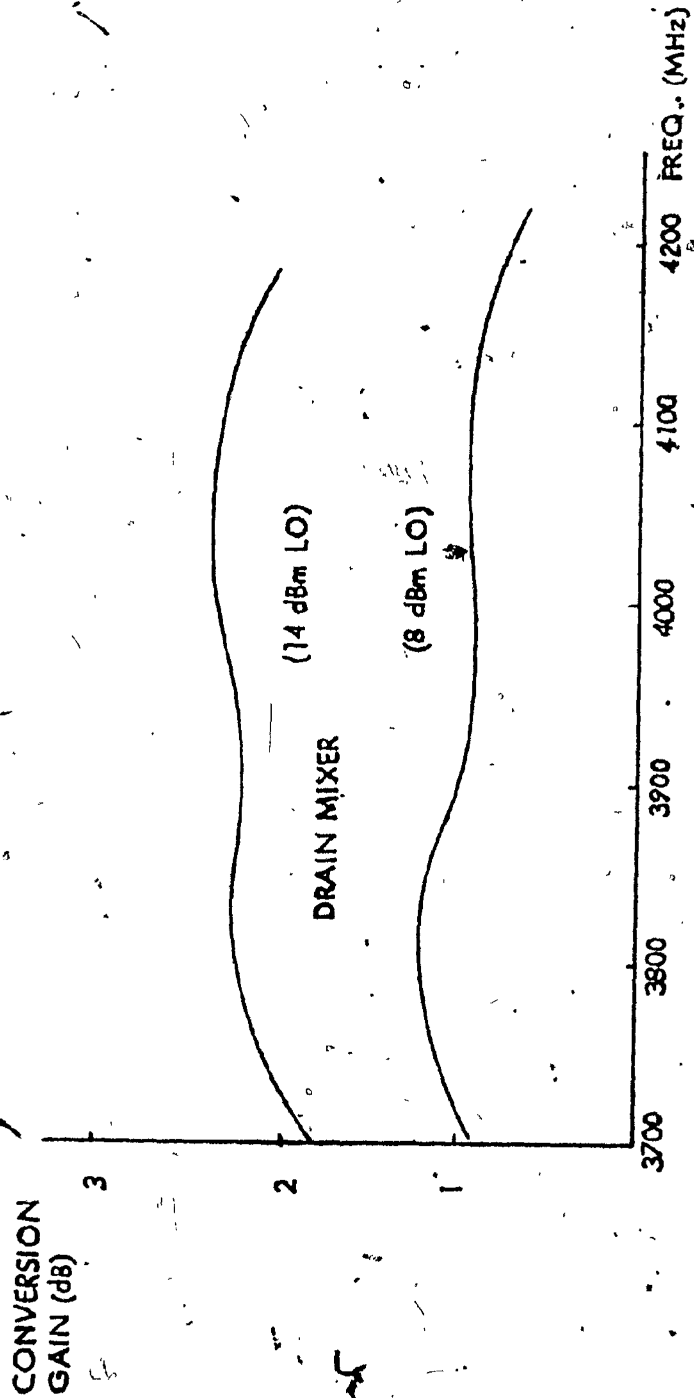


Figure 4.21: Drain Mixer Conversion Gain results

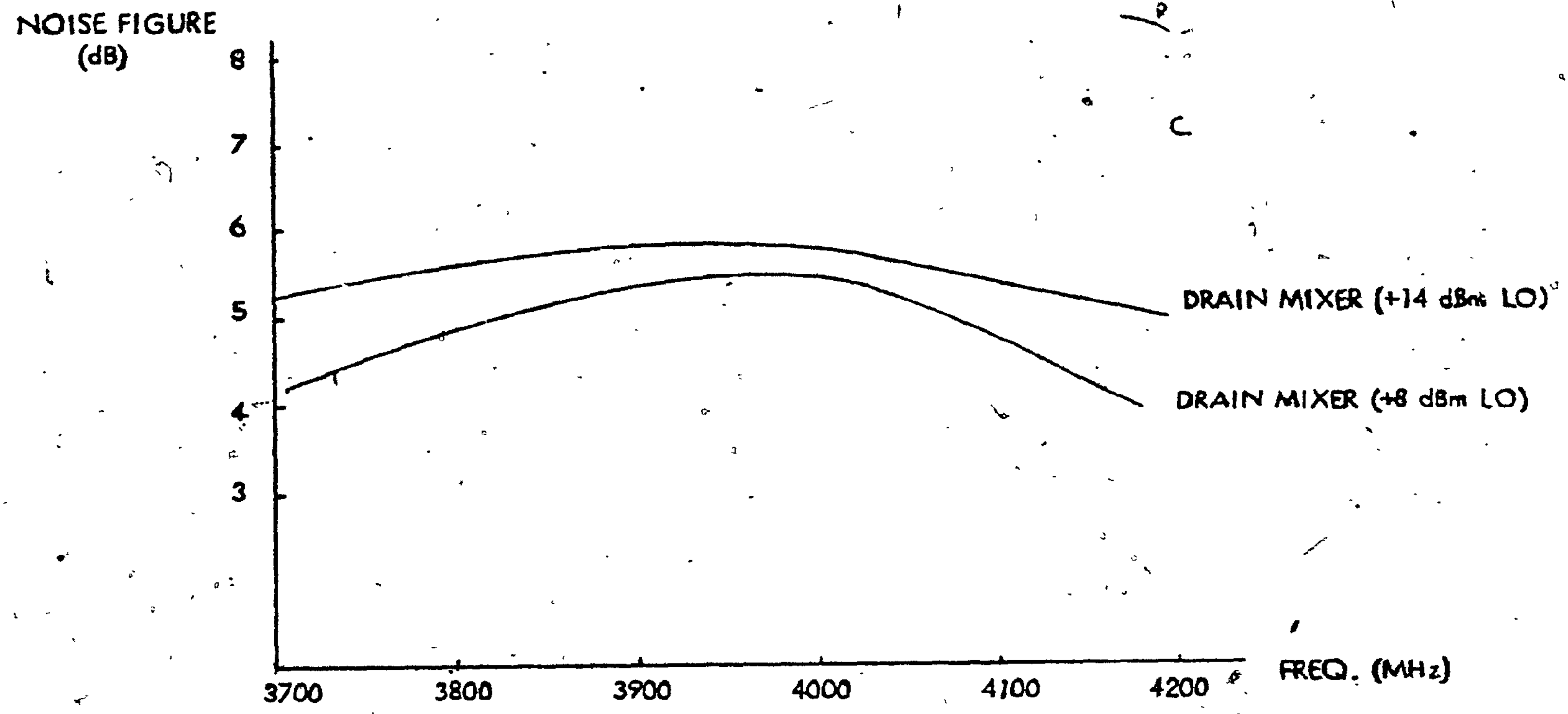


Figure 4.22 Drain Mixer Noise figure results

iv) Another new area of investigation is the use of InP (Indium Phosphide).[23] It has long been established that the electron velocity-field characteristics on the basis of higher peak-to-valley ratio (3.5 in InP and 2.2 in GaAs) leads to an efficiency improvement by a factor of 2 for InP over GaAs (Figure 4.23). This offers higher frequency operation with lower noise figure than current GaAs devices using the same geometries.[21] And as sub-half-micron gate length technology becomes commercially feasible, in the noise and bandwidth trade-off, the compromise favours InP at higher frequencies. The devices await further development of the InP technology, particularly in the growth of high quality buffer layers and the fabrication of improved Schottky barrier gates.

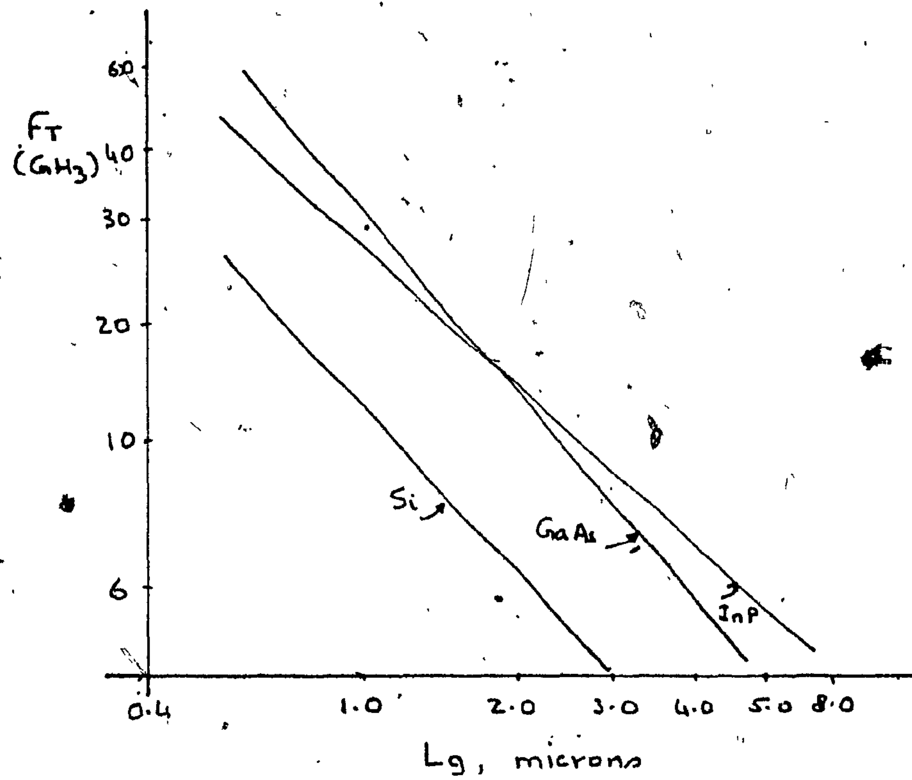


Figure 4.23: Unity Gain Frequency versus Gate Length, compared for Si, GaAs, and InP.

CHAPTER 5

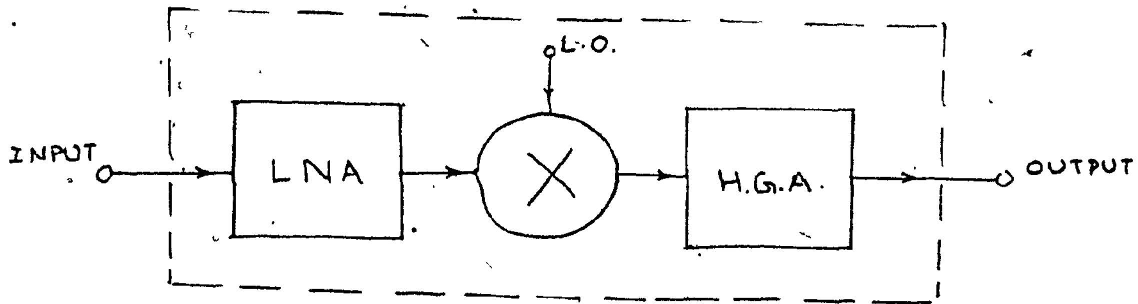
CONCLUSION

The theoretical analysis and experiments on FET mixers presented in this literature review, refer to the FET mixer in which the RF and the LO signals are fed into the gate. Frequency conversion is possible through the non-linear modulation characteristic of the transconductance, g_m. The motivation behind this study was because it is no longer possible to meet the growing demands on the transmission capacity of intercontinental communications network with submerged cable alone. Developments in the field of satellite engineering were needed to create additional high-quality communications links to cover great distances.

The use of the FET mixer, with both low noise figure and conversion gain offer a dramatic improvement over the resistive mixer type integrated front ends. Figure 5.1 compares receiver noise figures for the two cases. The benefits of conversion gain are further useful in reducing post-down-conversion amplification. This improves the carrier-to-intermod performance of the entire receiver.

Perhaps, it is appropriate to review the major topics of this report before commenting on the main ideas. The paragraph below summarizes the operation of a MESFET.

The device consists of a semiconductor substrate, usually GaAs, two contacts at both ends called the drain and the source. The substrate



The low noise amplifier characteristics

NF = 4 dB

G = 10 dB

The FET mixer

NF = 3 dB

G_C = +3 dB

Diode Mixer

NF = 4.5 dB

G_C = -4.5 dB

The High Gain Amplifier characteristics

NF = 8 dB

G = 50 dB

Overall Receiver Gain and Noise Figure characteristics

FET Mixer Case

NF = 4.56 dB

G = +63 dB

Diode Mixer Case

NF = 7.54 dB

G = 55.5 dB

Figure 5.1: System Calculations for a Satellite Receiver

material is mostly n-type because of the large electron mobility. The current flow from the drain to the source is by the majority carriers and can be controlled by voltage applied to a third terminal called the gate. The applied gate voltage causes the metal to semiconductor space charge layer to either widen or shorten (Figure 2.1). The widening and shortening of this layer has a modulating effect on the current through the device.

When the large signal local oscillator voltage pumps the Schottky-barrier gate, the result is a modulated (switched) transconductance which leads to frequency conversion, and amplification. Thus the fundamental mixer is realized. To optimize this circuit for best conversion gain and lowest noise figure, exhaustive, iterative circuit analysis is necessary. All published results, are based on empirical tuning of the FET mixer circuit to achieve, at best, local optimas in the performance. Aside from reactively terminating a few important spurious mixer products, it is not possible to control terminations for the rest. Especially true for microwave frequencies, it is simply not within the current state-of-the-art to analytically design a FET mixer circuit for optimum performance.

It is for this reason that there exists a significant gap between theory and results as presented in this review. The use of FET as microwave mixer in satellite communications is fairly novel, and most authors (except Bura/Dikshit) discuss IF in the order of 70 MHz. For use in a satellite downconverter, the realities of 500 MHz bandwidth of 0.1 dB flatness, at 6/4 GHz, virtually force

an empirical, rather than analytical, design approach.

The circuit construction and realization were on MIC, and here, it was not intended to present a detailed expose of MIC design data, but merely to review some important circuit parameters. Like everything at microwave frequencies (above 2 GHz), experimental and numerical techniques are in close corelation, and analytic approaches are approximate or unwieldly. The circuit for the 6/4 GHz gate injected local oscillator mixer circuit design was calculated to a first iteration, but significant bench tuning was needed to meet performance specification. The status of acceptable 'mixer-bias' S-parameters has been adequately discussed elsewhere in the main text and appendix. The results quoted are based on the author's own work and necessarily some of the design details are proprietory to the company.

These results are the best to-date performance data on FET mixers for communications satellites.[1] However, a conversion gain in excess of 18 dB, (but with IF of 70 MHz), and noise figure less than 6 dB, using a dual gate, half-micron FET has been reported.[2] This, along with Chapter 4.5, points the path for future development and studies, and holds the promise for true optimum mixer design.

LIST OF REFERENCES

CHAPTER 1

1. R. Dikshit, P. Bura, P. Mercer "6/4 GHz FET Receiver", Technical Report, RCA Report # MNLD-76-TR-015.

2. J. Sitch and P. Robson, "The Performance of GaAs FET As Microwave Mixers", Proc. IEEE, Vol. 61, pp. 399-400, March 1973.

3. R. Pucel, D. Masse and R. Bera, "Integrated GaAs FET Mixer Performance at X-Band", Electronics Letters, Vol. 11, pp. 199-200, May 1975.

4. P. Bura and R. Dikshit, "FET Mixers with the Drain LO Injection", Electronics Letters, Vol. 12, pp. 536-537, Sept. 1976.

5. C. Liechti, "Microwave Field-Effect Transistor - 1976", IEEETrans. on Microwave Theory and Techniques, Vol. MTT-24, No. 6, pp. 279-300, June 1976.

6. H. Cooke, "Microwave FET - A Status Report", International Solid-State Circuits Conference, Digest of Technical Papers, pp. 116-118, San Francisco, Feb. 1978.

CHAPTER 2

1. S. Sze, "Physics of Semiconductor Devices", Wiley, 1969.

2. P. Ludguist, "A Model Relating Electrical Properties and Impurity Concentrations in Semi-Insulating GaAs", Journal of Applied Physics, Vol. 48, pp. 1262-1267, March 1977.

3. R. Dikshit, "GaAs Schottky-Barrier Mixer Diode", Term Paper, Elec-N-722, Concordia University, May 1977.

4. W. Tantraporn, "On the Study of Metal-Semiconductor Contacts", IEE Trans. Electron Devices, pp. 331-338, March 1972.

5. M. McColl, "Conversion Loss Limitation on Schottky-Barrier Mixers", IEEE Trans Microwave Theory and Techniques, pp. 54-59, Jan. 1977.

6. E. Denlinger, "High Performance Mixer Diodes", International Electron Devices Meeting, Technical Digest, pp. 87-89, Washington, Dec. 1976.

7. G. Wrixon, "Low-Noise Diodes and Mixers for the 1-2 mm Wavelength Region", IEEE Trans. Microwave Theory and Techniques, pp. 1159-1165, Dec. 1974.

8. C. Liechti, "Microwave Field Effect Transistors - 1976", IEEE Trans on Microwave Theory and Techniques, Vol. MTT-24, No. 6, pp. 279-300, June 1976.

9. J. Ruch and W. Fawcett, "Temperature Dependence of the Transport Properties of Gallium Amenide Determined by a Monte Carlo Method", J. Appl. Physics, Vol. 41, August 1970.

10. R. Dawson, "Equivalent Circuit of the Schottky-Barrier Field-Effect Transistor at Microwave Frequencies", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-23, No. 6, pp. 499-501, June 1975.

11. B. Hewitt, H. Cox, J. Dilarenzo, W. Schlosser and D. Iglesias, "Low-Noise GaAs MES FETs", Electronics Letters, Vol. 12, No. 12, pp. 309-310, 10th June 1976.

12. K. Lehovac, "Voltage-Current Characteristics of GaAs JFET in the Hot Electron Range", Solid State Electronics, Vol. 13, pp. 1415-1426, Oct. 1970.

13. W. Shockley, "A Unipolar FET", Proc. IRE, Vol. 40, pp. 1365-1376, Nov. 1952.

14. K. Yamaguchi, S. Asai and H. Kodera, "Two-Dimensional Numerical Analysis of Stability Criteria of GaAs FETs", IEEE Trans. on Electron Devices, Vol. ED-23, No. 12, pp. 1283-1289, Dec. 1976.

15. W. Hwang, "Lecture Notes" - Elec-N-722, Concordia University, Jan. 1977.

16. J. Cooper and M. Gupta, "Microwave Characterization of GaAs MES FET and the Verification of Device Model", IEEE Journal of Solid-State Circuits, pp. 325-329, June 1977.

17. R. Pucel, D. Masse and C. Knumm, "Noise Performance of a GaAs FET", Proc. 1975, Cornell Conference on Active Semi-Conductor Devices for Microwave and Integrated Optics, pp. 265-276.

18. C. Liechti, E. Gowen and J. Cohen, "GaAs Microwave Shottky-Gate FET", 1972 Int'l. Solid State Circuits Conference, Digest of Technical Papers, pp. 158-159.

19. R. Zuleeg, "Solid State Electronics", Vol. 10, pp. 599, 1967.

20. D. Surana and J. Gardiner, "Gain and Distortion Properties of FET Mixers and Modulators", IEEE Trans. on Electromagnetic Compatibility, Vol. EMC-16, No. 1, pp. 29-38, Feb. 1974.

21. P. Bura and R. Dikshit, "FET Mixers for Communications Satellite Transponders", 1976 MTTS, International Microwave Symposium, pp. 90-92, June 1976.

22. S. Asai, S. Okazaki and H. Kodera, "Optimized Design of GaAs FETs for Low-Noise Microwave Amplifiers", Solid State Electronics, Vol. 19, pp. 463-470, 1976.

23. A. Saleh, "Theory of Resistive Mixers", Phd Thesis, M.I.T., Jan. 1970.

24. I. Docherty, "Some Solid State Devices for Frequency Converters", Proc. IEEE, Australia, Dec. 1964.

25. R. Pound, "Microwave Mixers", MIT Radiation Laboratory Series, Vol. 16, McGraw Hill, 1948.

26. E. Herold, "Frequency Mixing in Diodes", Proc. IRE, Oct. 1963.

27. D. Tucker, "Circuits with Periodically-Varying Parameters", Van Nostrand, 1964.

28. M. Barber, "Noise Figure and Conversion Loss of the Schottky-Barrier Mixer Diode", IEEE Trans. on Microwave Thoery and Techniques, Nov. 1967.

29. A. Van der Ziel, "On the Shot Effect of p-n Junction", IRE, Trans. on Electron Devices, Nov. 1952.

30. H. Cooke, "Microwave FETS - A Status Report", International Solid-State Circuits Conference, Digest of Technical Papers, pp. 116-118, San Francisco, Feb. 1978.

31. N. Slaymaker, R. Soares and J. Turner, "GaAs MES FET Small Signal X-Band Amplifiers", IEEE Trans-on Microwave Theory and Techniques, Vol. MTT-24, No. 6, pp. 329-337, June 1976.

32. M. Maeda, S. Takahashi and H. Kodera, "CW Oscillations Characteristics of GaAs Schottky-Barrier Gate Field Effect Transistor", Proc. IEEE, Vol. 63, pp. 320-321, Feb. 1975.

33. H. Tserng, H. Macksey, F. Doerbeck and W. Wisseman, "X-Band MIC GaAs Power FET Amplifier Module", International Solid-State Circuits Conference, Digest of Technical Papers, pp. 122-124, San Francisco, Feb. 1978.

34. R. Pucel, D. Masse and R. Bera, "Integrated GaAs FET Mixer Performance at X-Band", Electronics Letters, Vol. II, No. 9, 1st May 1975.

35. R. Pucel, "Performance of GaAs MES FET Mixers at X-Band", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-24, No. 6, pp. 351-360, June 1976.

36. O. Kunita and K. Morita, "Microwave MES FET Mixer", IEEE Trans. Microwave Theory and Techniques, Vol. MTT-24, No. 6, pp. 361-366, June 1976.

37. G. Vendelin and M. Oman, "Circuit Model for the GaAs MES FET Valid up to 12 GHz", Electronics Letters, Vol. II, pp. 60-61, Feb. 1975.

38. B. Lariou and J. Leost, "GaAs FET Mixer Operation with High Intermediate Frequency", Electronics Letters, Vol. 12, No. 15, pp. 373-375, July 1976.

39. B. Himsworth, "A Two-Dimensional Analysis of Gallium Arsenide Junction Field-Effect Transistor with Long and Short Channel", Solid-State Electronics, Vol. 15, No. 12, Dec. 1972.

40. M. Ogawa, K. Ohata, T. Furutsaka and N. Kawamura, "Submicron Single-Gate and Dual-Gate GaAs MES FETs with Improved Low Noise and High Gain Performance", IEEE Trans. on Microwave Theory and Techniques, Vol. 24, No. 6, pp. 300 to 305, June 1976.

CHAPTER 3

1. M.A.R. Gunsten and J.R. Weale, "The Transmission Line Characteristics of Microstrip", The Marconi Review, Third Quarter, pp. 226-243, 1969.

2. E. Yamashita and R. Mitra, "Variational Method for Analysis of Microstrip Lines", IEEE Trans. Microwave Theory and Techniques, Vol. MTT-16, pp. 251-256, April 1969.

3. C.P. Hartwig, D. Masse and R.A. Pucel, "Frequency Dependent Behaviour of Microstrip", G-MTT International Microwave Symposium, Detroit, Michigan, pp. 110-116, May 1968.

4. P. Troughton, "The Evaluation of Alumina Substrates for Use in Microstrip Microwave Integrated Circuits", 1969 European Microwave Conference, IEEE Conference Publication 58, pp. 49-52, 1970.

5. H.A. Wheeler, "Transmission Line Properties of Parallel Strips Separated by a Dielectric Sheet", IEEE Trans. Microwave Theory and Techniques, Vol. MTT-13, pp. 172-185, March 1965.

6. O. Jain, V. Makios and W. Chudobiak, "Open-End Edge Effects in Microstrip Transmission Lines", IEEE Trans. Microwave Theory and Tech. Vol. MTT-20, Sept. 1972, pp. 626-628.

7. K. Mehmet, M. McPhun and D. Michie, "Simple Resonator Method for Measuring Dispersion of Microstrip", Electron Lett. Vol. 8, No. 6, pp. 165-166, March 23, 1972.

8. O. Jain, "Conductor Losses in Microstrip Transmission Lines", IEEE Trans. on MTT, Vol. MTT-21, Sept. 73.

9. O. Jain, J. Wight, W. Chudobiak, and W. Maikos, "Equivalant Circuits of Microstrip Impedance Discontinuties and Launchens", IEEE Trans. on Microwave Tehory and Tech. Vol. MTT-22, Jan. 1974.

10. R. Dikshit, P. Bura, P. Mercer, "An all-FET 6/4 GHz Receiver, IEEE, International Solid State Circuits Conference, Feb. 1977, Philadelphia.

11. H. Howe Jr., "Stripline Circuit Design", Aertech House, 1976.

12. J. Frey, "Microwave Integrated Circuits", Aertech House 1975.

CHAPTER 4

1. R. Pucel, D. Masse and C. Knumm, "Noise Performance of Gallium Arsenide Field Effect Transistors", IEEE Journal of Solid State Circuits, Vol. SC-11, No. 2, April 1976, pp. 243-254.

2. A. Van der Ziel, "Noise, Sources, Characterization, Measurement", Prentice-Hall Inc., Englewood Cliffs, N.J., 1970.

3. H.F. Cooke, "Microwave FETs - A Status Report", 1978, IEEE International Solid State Circuits Conference, Digest of Technical Papers, Feb. 1978, San Francisco pp. 116-118.

4. A. Van der Ziel, "Thermal Noise in FETs", Proc. IRE, Vol. 50, Aug. 1962.

5. W. Beachtold, "Noise Behaviour of GaAs FETs with Short Gate Length", IEEE Trans. on Electron Devices, Vol. ED-19, May 1972.

6. H. Statz et al, "Signal and Noise Properties of GaAs Microwave FETS", in Advances in Electronics and Electron Physics, Vol. 38, New York Academic Press, 1975.

7. J. Frey, "Effects of Intervalley Scattering on Noise in GaAs and InP Field-Effect Transistor", IEEE Trans on Electron Devices, Vol. ED-23, No. 12, Dec. 76, pp. 1298-1303.

8. D. Sodini, A. Touboul, G. Lecoy and M. Savelli, "Generation - Recombination Noise in the Channel of GaAs Schottky-Gate FETs", Electronic Letters, Vol. 12, 22 Jan. 1976.

9. H. Statz, H. Haus and R. Pucel, "Noise Characteristics of Gallium Arsenide Field-Effect Transiston", IEEE Trans. on Electron Devices, Vol. ED-21, No. 9, Sept. 1976.

10. M. Sucher and J. Fox, "Handbook of Microwave Measurements - Vol III", John Wiley and Sons, Inc. 1963.

11. "Microwave Power Measurement", Applications Note Sixty-four Hwelett-Packard.

12. O. Kurita and K. Morita, "Microwave MES FET Mixer", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-29, No. 6, June 1976 pp. 361-366.

13. P. Bura and R. Dikshit, "FET Mixers for Communication Satellite Transponders", 1976 MTTS, International Microwave Symposium, June 1976, pp. 90-92.

14. R. Englemann and C. Liechti, "Bias Dependence of GaAs and InP MES FET Parameters", IEEE Trans. on Electron Devices, Vol. ED-26, No. 11, Nov. 1977 pp. 1288-1296.

15. D. Sodini, G. Lecoy, D. Rigaud and M. Rolland, "Impedance and Noise in the Channel of a GaAs Schottky-Gate FET", Solid State Electronics, July 1977, Vol. 20.

16. Plessey Co. Limited, - 1978 ISSCC - discussion with J. Turner.

17. S. Asai, S. Okazaki and H. Kodera, "Optimized Design of GaAs FETs for Low-Noise Microwave Amplifiers", Solid State Electronics, 1976, Vol. 19, pp. 463-470.

18. R.E. Miller, T.G. Phillips and D.E. Iglesias, "Noise Performance of Microwave GaAs FET Amplifiers at Low Temperatures", Electronic Letters, 6 January 1977, Vol. 13, No. 1, pp. 10-11.

19. R. Dikshit, P. Bura, "FET Mixer With the Drain LO Injection", Electronics Letters, Vol. 12, pp. 536-537, Sept. 1976.

20. T. Maloney, J. Frey, "Frequency Limits of GaAs and InP Field-Effect Transistors", IEEE Trans. on Electron Devices, June 1975, pp. 357-358.

21. I.D. Higgins, "Performance of Self-oscillating GaAs MESFET Mixers at X-Band", Electronic Letters, 11 November 1976, Vol. 12, pp. 605-606.

22. G. Gibbons, "InP Devices; Promising but Challenging", Microwave Systems News, Vol. 8, No. 2, February 1978.

CHAPTER 5

1. P. Bura and R. Dikshit, "FET Mixers for Communications Satellite Transponders", IEEE - MTTS, International Microwave Symposium, pp. 90-92, June 1976.

2. J. Turner, et al, "Dual Gate FET Mixer", To be presented, IEEE - MTTS, International Microwave Symposium, June 1978.

APPENDIX A:

1. E.Gordan, D.Herriott, "Pathways in Device Lithography", IEEE Trans. on Electron Devices, July 1975.

2. D.Markle, "A new projection printer", Solid State Technology, June 1974.

3. T.W.O'Keefe, et. al., "An electron imaging system for the fabrication of semiconductor devices", IEEE Trans. on Electron Devices, Vol.12, 1969

4. F.H.Dill, "Optical Lithography," IEEE Trans. on Electron Devices, July 1975.

5. C.Shank, R.Schmidt, "Optical technique for producing 0.1 um surface structures" Appl. Phys. Letter, Vol.23, Aug. 1973.

6. A.Neureuther, F.Dill, "Photo resist modelling and device fabrication applications", Proc. Microwave Research Institute Symposium, XVIII, April 1974.

7. P.Baudet, "Submicron Self-Alignment GaAs MESFET" IEEE Trans. Microwave Theory Tech., Vol. MTT-24, No.6, June 1976.

8. M.C. Driver, H.B.Kim, "GaAs self-aligned gate field effect transistors", Proc. IEEE, pp.1244, 1245, August 1971.

9. S.Middelhoek, "Metallization processes in fabrication of Schottky barrier FETs", IBM J.Res.Dev., Vol.14, March 1970, pp. 148-151.

APPENDIX B

1. NEC Data Sheet for NE244 Gallium Arsenide Field Effect Transistor.

APPENDIX C

1. J. Cooper and M. Gupta, "Microwave Characterization of GaAs MES FET and the Device Model", IEEE Journal of Solid State Circuits, June 1977.
2. S. Aihara and H. Katoh, "11 and 14 GHz - Band Low-Noise GaAs FET Amplifier", Technical Application Note, Nippon Electric Company.
3. P. Bura and R. Dikshit, "FET Mixers for Communication Satellite Transponder", 1976 MTTS, International Microwave Symposium, June 1976, pp. 90-92.
4. J. Trudel, "CAD and the Network Analyser", Technical Applications Note, Tektronix, Inc.

APPENDIX D

1. H. Statz, H. Haus and R. Pucel, "Noise Characteristics of Gallium Arsenide Field - Effect Transistor", IEEE Trans. on Electron Devices, Vol. ED-21, No. 9, Sept. 1974.
2. R. Pucel, D. Masse and R. Bera, "Integrated GaAs MES FET Mixer Performance at X-Band", Electronics Letters, Vol. II, May 1975.
3. R. Pucel, D. Masse and C. Krumm, "Noise Performance of Gallium Arsenide Field Effect Transistors", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 2, April 1976.

APPENDIX D - continued

4. R. Pucel, D. Masse and R. Bera, "Performance of GaAs MES FET Mixers at X-Band", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-24, No. 6, June 1976

APPENDIX E

E-1 M. O'Donovan and C. Kudsia, "microwave Filters for Communications Networks", Aertech House, 1975.

E-2 J. Frey, "Microwave Integrated Circuits", Aertech House, 1975.

APPENDIX A

DEVICE FABRICATION

A.1 Introduction

In recent years it has been hard to find articles more relevant to the practicing engineer, to those people whose job it is to convert a concept into a demonstrably prodicible market product. A large number of engineers are anxious to devour papers which provide a detailed exposition of "how to", there are only few engineers willing to write such papers in the technical depth appropriate to a professional journal and even fewer companies willing to permit their publication, for obvious proprietary reasons.

There can be little doubt that, in the fabrication of modern solid-state electron devices, the processes by which the device and circuit geometries are defined in the active medium are central to the production of useful state-of-the-art components. But, precisely because this is an intensely competitive area, where art, science, and not a small amount of witchcraft seem inextricably linked, it has been proven difficult to put together a complete picture of the field which will please everyone.

Of particular interest to engineers interested in the fabrication of integrated circuits is the problem of registration of successive pattern levels.

There is some duplication of the background materials, but although the various authors start with the same basic laws of physics, they do not always come to the same conclusion as to the practical consequences.

A.2 Lithography Review

Many technologies have been used or proposed for exposing substrates with finer features. Beyond ubiguitous contact printing, one finds proximity, step-and-repeat, and stationary and scanning projection optical systems being used. Electron beam and X-ray systems are being developed to meet more demanding requirements. (1) All of these will be reviewed briefly in what follows.

Contact Printing:

Contact printing from step-and-repeated masks is used for the vast majority of wafer exposures. Resolution is satisfactory for features as small as $2\mu m$. Uniformity Uniformity of both exposure and photosensitive material can be maintained so that line width control is within acceptable tolerances.

Runout and mask defects accumulated during successive mask uses are the major limitations of contact printing. Flatness errors in the substrates of the master, working copy mask, and wafer cause distortions in the patterns when they are contacted to make the mask and wafer exposures. To the extent that the distortions are not consistent from one level to the next, misalignment of features will occur. These runouts are especially significant when required alignment tolerances are below one micron.

The tight contact during printing damages the mask and substrate. The accrued damage and particles of resist adhering to the mask are printed on the following exposures causing a rapid buildup of defects.

Soft contact, proximity, and projecting printing offer longer mask life at the expense of distortion, resolution, or line width control. The use of conformable masks in a contact mode is another alternative.

Proximity Printing:

Spacing the mask away from the substrate minimizes the contact and eliminates most of the defects that result from contact. Diffraction of the transmitted light causes a reduction in resolution and distortion of the individual photoresist features.[6] The degree to which this occurs depends on the actual mask-to-wafer spacing which is variable across the wafer.

The smallest features that are practical for proximity exposure are approximately 7 um. The cost of equipment for contact or proximity printing is relatively low. The throughput is high. In fact, the cost of masks tends to dominate the cost of operation. It is not likely that contact or proximity printers will soon become obsolete.

Stationary Projection Printing[2]:

The promised performance of projection printing in combination with long mask life has lured many groups into developing 1:1 projection systems. These have been used for features greater than 5.0 um with some success.

Scanning Projection Printing [5]:

A scanning projection system is connercially available that uses an unique optical system to form a 1:1 image of an arc-shaped area of the mask onto the corresponding part of the wafer. This strip of imaged pattern is scanned over the field to expose the entire area in one pass

Step-and-Repeat Projection Systems:

A step-and-repeat reduction camera such as is used for exposing masters can be used to expose wafers with high quality images and uniform intensity. A high aperture lens can be used to expose the small field of a single large chip or an array of smaller chips if the wafer is realigned and refocused for every exposure.

Limitations of Projection Optical Systems [4]:

Diffraction of light limits the resolution that can be achieved with practical systems. A perfect f/2.0 optical system can image the fundamental frequencies of periodic 2.0 u-m lines and spaces with 70% contrast. However, the same lens would have a depth of focus of less than the flatness variations of practical GaAs wafers. This fundamental characteristic limits the practical line width to roughly 5.0 um for exposure over large areas and 2.0 um where focus can be corrected for small image areas. Better results can be obtained, but extreme control is required.

One attractive way to avoid these limitation is to expose using electrons that have an equivalent wavelength of a fraction of an angstrom rather than the fraction of a micron associated with visible light. Another altenative is the use of soft X-rays with wavelengths in the 4 to 10 Å region.

Electron Lithography [3]:

Electrons are a suitable radiation for lithography for reasons other than their short wavelength. Electrons can be imaged to form either a pattern or a small point, and deflected and modulated by electrostatic or magnetic fields with speed and precision. Their energy and dose can be controlled precisely. Special electron-sensitive resists have been developed which have suitable processing characteristics and which can be effectively exposed at the level of radiation that can be conveniently generated in practical electron beam machines. As a consequence, electrons can be used in a number of different ways involving either beam scanning to generate patterns directly from software or electron imaging from special masks.

Beam Scanning Systems:

Electrons from a source can be formed into a pencil-like beam that can be deflected over an electron resist – coated substrate and modulated to draw a desired pattern. The beam can be imaged to a submicron spot with different current to locally expose the resist in less than 10^{-7} sec. Since up to 10^{11} spots are typically required, this high speed is important. Positioning 10^{11} spots accurately place inordinate demands on the electron deflection system.

Two approaches are possible. In both the electron column is used as a scanning electron microscope to locate registration features on the substrate for realignment process. In one approach, realignment on separate registration masks is accomplished for each table position. In the other, laser interferometers are used to control the precision of table motion.

It has been demonstrated that an electron beam pattern generator can make for better accuracy, linewidth control and edge quality, lower defect density, and at a lower cost and faster turn-around then a very high-quality optical system (when both are under the same management).

Electron Imaging (ELIPS) [3]:

Electrons can be imaged to form a complete pattern at one time. An electron image projection system (ELIPS) is available, in which a photocathode is deposited on the patterned surface of an optical mask. Ultra violet light illuminates the photocathode layer through the substrate in the transparent regions of the mask causing a patterned emission of electrons from the photocathode. These electrons are imaged by uniform coaxial electrostatic and magnetic fields onto the facing resist coated substrate. The system is fundamentally capable of submicron resolution over the full wafer area. However, non-uniform fields, imperfect substrate flatness and its effect on the electrostatic fields, and field alignment errors can cause poor resolution and non-reproducible distortion.

Step and Repeat Electron Projection Systems:

Analogous to the optical step-and-repeat projection system, an electron projection can image the electrons transmitted by a special mask or reticle at a 10X reduction onto the device substrate. The substrate can be moved on a mechanical stage and repeated exposures made to cover its area. The 10X reticle could be made of a fine grid as the transparent portion, with opaque metal islands for the electron opaque regions. The images should have submicron resolution over a 5 mm square field, but they may have significant distortion. As in ELIPS, the image current is sufficiently large that actual exposure time is not limiting. The practicality of step-and-repeat electron systems will depend upon

their cost, resolution, stability of distortion, and the durability and practicality of the electron transparent mask. No completed systems are known to be in use at this time.

X-rays (4):

X-rays in the 3 to 10 Å region produced by the bombardment of suitable targets by 20 kV electrons are also essentially free of diffraction. Scattering and reflection effects are also negligible. It is not practical to focus or deflect the X-rays, so a proximity printing arrangement is used with the radiation diverging from a small source at a distance of a half meter or more. An X-ray transparent substrate such as thin silicon supports a pattern of heavy metal such as gold or platinum in the X-ray opaque regions of the mask. The X-ray systems will find commercial use if a stable, durable, and reasonably inexpensive mask can be made and if the source and resist efficiencies can be improved so that exposure times become economically practical.

A.3 Self-alignment of GaAs MESFET

Since 1968 the improvement of the GaAs MESFET has required the use of smaller and more refined geometries. Thus alignment rapidly became one of the major problems in the process. To solve this difficulty, several laboratories have proposed various alignment methods. Baudet [7] describes a new and simple method of selfalignment which does not necessitate the use of electron beam technology.

Whereas the other methods generally use self-alignment from source and drain contacts by using the undercutting or over flowing of ohmic contacts, this method uses the engraving of the gate itself to self-align the source and drain contacts, eliminating in that way the main difficulties of the self-alignment.

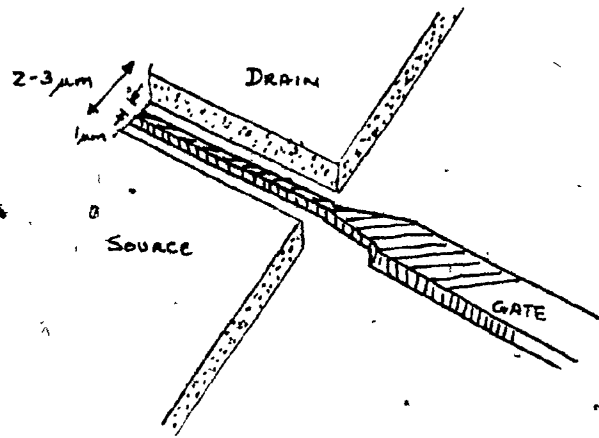
Such difficulties include:

1) Inhomogeneaties of the thickness of the layer which gives a poor processing yield after making the layer thin under the gate,
2) Control of the current flowing through the channel during the etching,
3) Quality of the Schottky diode.

The actual Device Fabrication (not for the NE244 used in the mixer) process is carried out in the following way: [8] [9]

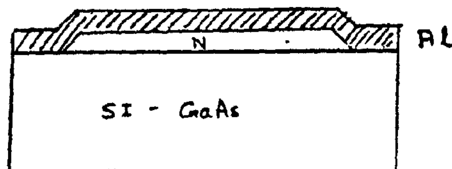
1) The starting material is a chromium-doped semi-insulating substrate on which is grown ($AsCl_3/Ga/H_2$ system) a layer of n-type material of thickness 0.15 um - 0.2 um and doping between 8 and 10×10^{16} cm^{-3}. The surface of the material is a [0,0,1] plane, 3° off towards the [1,1,0] direction. The active zones of transistors are insulated by

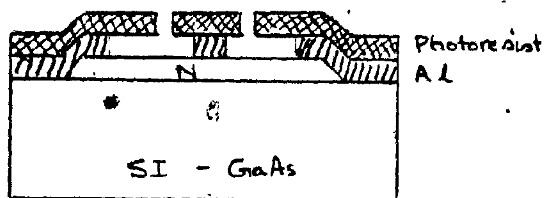
0.4 um deep chemical etching. During this step the wafer is oriented so that the gate passes over a sloping mesa edge.



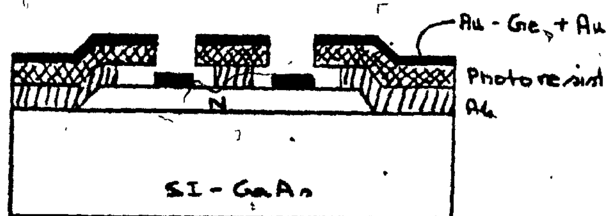
2) In order to obtain a good diode, it is necessary to minimize the thickness of the interfacial layer between the aluminum and the n-layer, thus producing an ideality factor which approaches unity. This is effected by using a classical desoxydizing treatment of the GaAs surface, after which aluminum is deposited under high vacuum.

3) The wafer is then covered with photoresist which is subsequently removed from the source and drain areas, thus defining the channel length. The source and drain areas are opened by etching the aluminum. This etching is continued until the undercutting of the aluminum is one-third of the channel length.

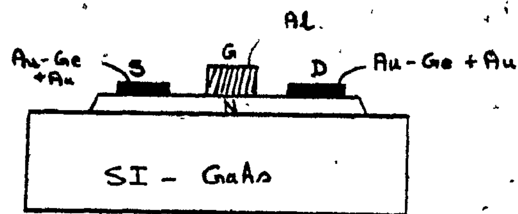




4) After an adequate cleaning of the GaAs surface, an AuGe layer and an Au layer are evaporated on the wafer. The over hanging of the photo resist ensures the automatic alignment of the contacts. The photoresist is removed by a lifting process.



5) A final engraving of the aluminum defines a gate pad at one end of the channel. Annealing at 450°C under H_2 flow makes the drain and source contacts ohmic.



APPENDIX B

NE244 DATA SHEET

APPENDIX B

Fabrication Technology

The device patterns for (NEC) FETs employ a complex metallization system fabricated on a thin (.17 to .20 μ) n-type epitaxial layer which is formed on the Cr-doped semi-insulating GaAs substrate. The use of a semi-insulating substrate reduces the input and output parastics. Beneath the active epitaxial layer, is an intrinsic "buffer" layer which is essential in preventing carrier trapping. Trapping can produce a variety of short- and long-term failure modes, such as I_{DSS} instability (sometimes called "I_{DSS} looping" or "stepping") and gain-temperature hysterisis.

Conventional contact masking, etching and metal-lifting techniques are utilized. The source and drain metallization is shown in Figure B -1(a) and consists of platinum, titanium, platinum and gold films sequentially deposited on a gold-germanium (Au-Ge) contact metal. A subsequent heat treatment is employed to ensure proper alloying and low resistance ohmic contacts. If the deposition of the metallization system is performed incorrectly, it will result in drift of the contact resistance, increasing the leakage current of the gate, and degrading the g_m of the device. This resistance drift is the result of forming a complex Au-Ge intermetallic compound, which increases the bulk resistance. This phenomenon was one of the primary failure mechanisms of the first-generation GaAs FETs.

The Schottky-barrier gate is formed by evaporation of a pure aluminum film and later defined by a similar photomasking technique. An aluminum Schottky-barrier gate has the advantage of low sheet resistance and the elimination of any high temperature gate diffusion process. The epitaxial film has been removed outside the active area by a shallow mesa etch, so that the gate-bonding pad may be formed directly on the semi-insulating substrate. This technique minimizes parasitic gate capacitance to the substrate.

The gate-pad metallization consists of (Figure B -1(b)) evaporated gold on layers of platinum and titanium which overlap an extension of the V-pattern aluminium gate. This system is designed to prevent the formation of any intermetallic compounds ("white" and "purple plaque") during production or assembly. This is of special concern because of the use of gold-bonding wires (and the high temperatures required to conduct accelerated life tests at 300°C).

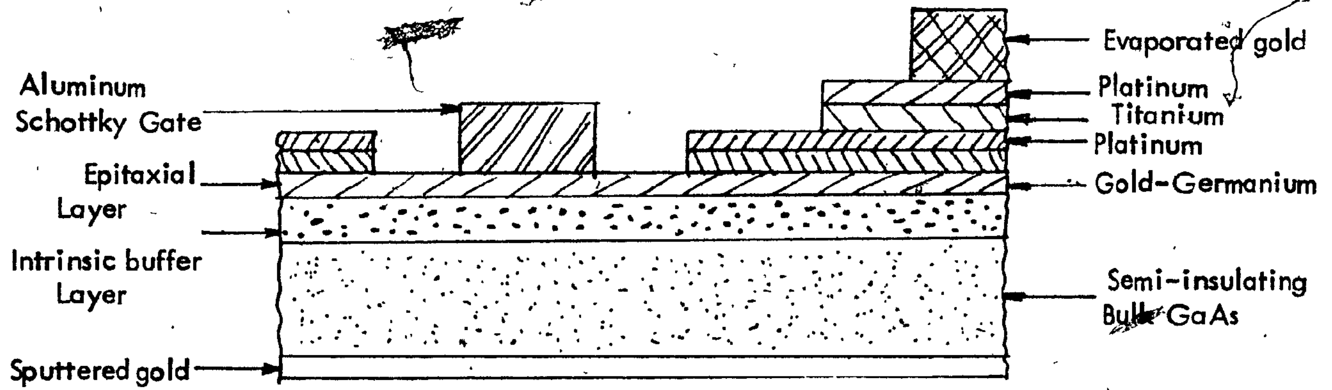


Figure B-1(a): Cross-section Showing Drain and Source and Metallization

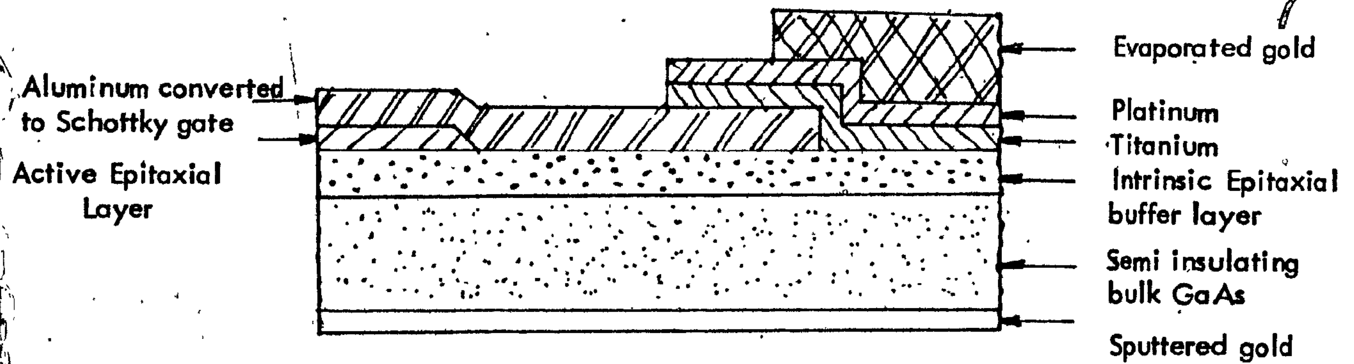


Figure B-1(b): Cross-section Showing Gate Pad Metallization

NEC

MICROWAVE TRANSISTOR SERIES

NE244

PRELIMINARY DATA SHEET

GALLIUM ARSENIDE LOW NOISE MESFET

FEATURES:

- Very High f_{MAX} 55GHz (Packaged Device)
- High Gain 12dB at 8GHz
- Low Noise Figure 2.3dB at 8GHz
- New Stripline Package

DESCRIPTION:

The NE244 is a gallium arsenide field-effect transistor (GaAs FET) designed for low noise amplifier and oscillator applications up to X-Band. Besides chip form (NE24400), the device is available in two rugged, metal-ceramic packages. The NE24406 is in a low parasitic package designed for use up to 12GHz and all hi-rel applications. The NE24483 is a low-cost industrial grade package for applications up to 8GHz. The NE244 Series utilizes the latest design and production techniques, and NEC's quality control procedures assure the utmost in performance reliability. Long term performance stability is assured by NEC proprietary wafer processing. The extraordinarily high gain associated with optimum noise figure, long term stability, and low cost, has made the NE244 the most widely used GaAs FET presently available.

PERFORMANCE SPECIFICATION (T_A=25°C)

		"NE" PART NUMBER	NE24400			NE24406			NE24483		
		OTHER PART NUMBER				2SK85					
		PACKAGE STYLE	Chip			#682			#662K		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
f_{MAX}	Maximum Frequency of Oscillation at V_{DS}=3v, I_{DS}=30mA	GHz		55			55			55	
MAG	Maximum Available Power Gain at V_{DS}=3v, I_{DS}=50% I_{DSS} (Typ. 30mA)										
	f=4GHz	dB		17			17			17	
	f=8GHz	dB		12		9	12			11	
	f=12GHz	dB		10			9			7	
NF	Noise Figure at V_{DS}=3v, I_{DS}=15% I_{DSS} (Typ. 10mA)										
	f=4GHz	dB		1.5			1.5			1.5	
	f=8GHz	dB		2.3			2.7	1.5		3.0	
	f=12GHz	dB		3.3			3.[illegible]			4.5	
GNF	Associated Gain at NF at V_{DS}=3v, I_{DS}=15% I_{DSS} (Typ. 10mA)										
	f=4GHz	dB		14.0			14			13	
	f=8GHz	dB		10.5			10			9	
	f=12GHz	dB		6.5			6			4	
P_{out}	Output Power (1dB Compression) at V_{DS}=3v, I_{DS}=50% I_{DSS} (Typ. 30mA)										
	f=4GHz	dBm		10.0			10.0			10.0	
	f=8GHz	dBm		8.5			8.5			8.5	

25 Sept 76

ELECTRICAL CHARACTERISTICS (T_a=25°C)

	"NE" PART NUMBER		NE24400			NE24406			NE24483		
	OTHER PART NUMBER					2SK85					
	PACKAGE STYLE		Chip			#682			#662K		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
I_{DSS}	Drain Current at V_{DS}=3V, V_{GS}=0V	mA	30	60	100	30	60	100	30	60	100
V_p	Pinch-off Voltage at V_{DS}=3V, I_{DS}=0.1mA	V	-1.5	-4.0		-1.5	-4.0		-1.5	-4.0	
g_m	Transconductance at V_{DS}=3V, I_{DS}=30mA	mmho		20	100	15	20	100	15	20	100
I_{GS}	Gate to Source Leakage Current at V_{GS}=-5V	µA		0.1	1.0		0.1	1.0		0.1	1.0
R_{th}	Thermal Resistance (c-c)	°C/W			170			200			200
P_t	Total Device Dissipation	mW			500			500			300

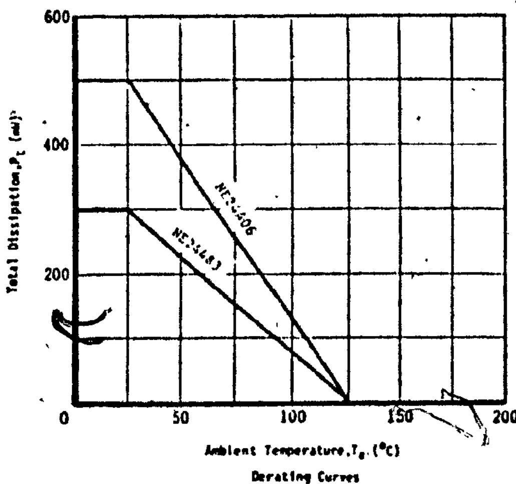
NOTE: All DC tests performed per MIL-STD-750

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

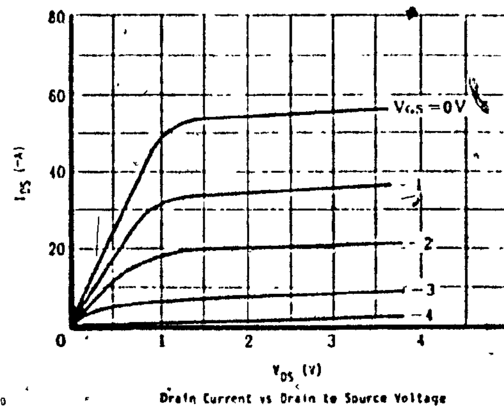
PARAMETER	SYMBOL	RATINGS	UNITS
Drain to Source Voltage	V_{DS}	5.0	V
Gate to Source Voltage	V_{GS}	-10.0	V
Drain Current	I_{DS}	100	mA
Channel Temperature	T_{ch}	125	°C
Storage Temperature	T_{stg}	-65 to 125	°C

RELIABILITY SCREENING

GRADE D (Industrial)	GRADE C (Military)
(200-1200 Failures in 10^9 Device Hours)	(50-300 Failures in 10^9 Device Hours)
•100% DC Wafer Probe •Pre-cap Inspection (sample basis) •100% High Temperature Storage (125°C-24 Hrs.) •100% Gross Leak Tests •100% Mechanical Shock Tests •100% Group A Tests (Tests may vary depending upon package style.)	•100% DC Wafer Probe •100% Pre-cap Inspection •100% High Temperature Storage (125°C-24 Hrs.) •100% Environmental Tests-Heat Cycle, Gross and Fine Leak, Centrifuge Shock •100% 168 Hour Power Burn-in at P_{cmax} and T_a=25°C or T_{jmax}



Derating Curves



Drain Current vs Drain to Source Voltage

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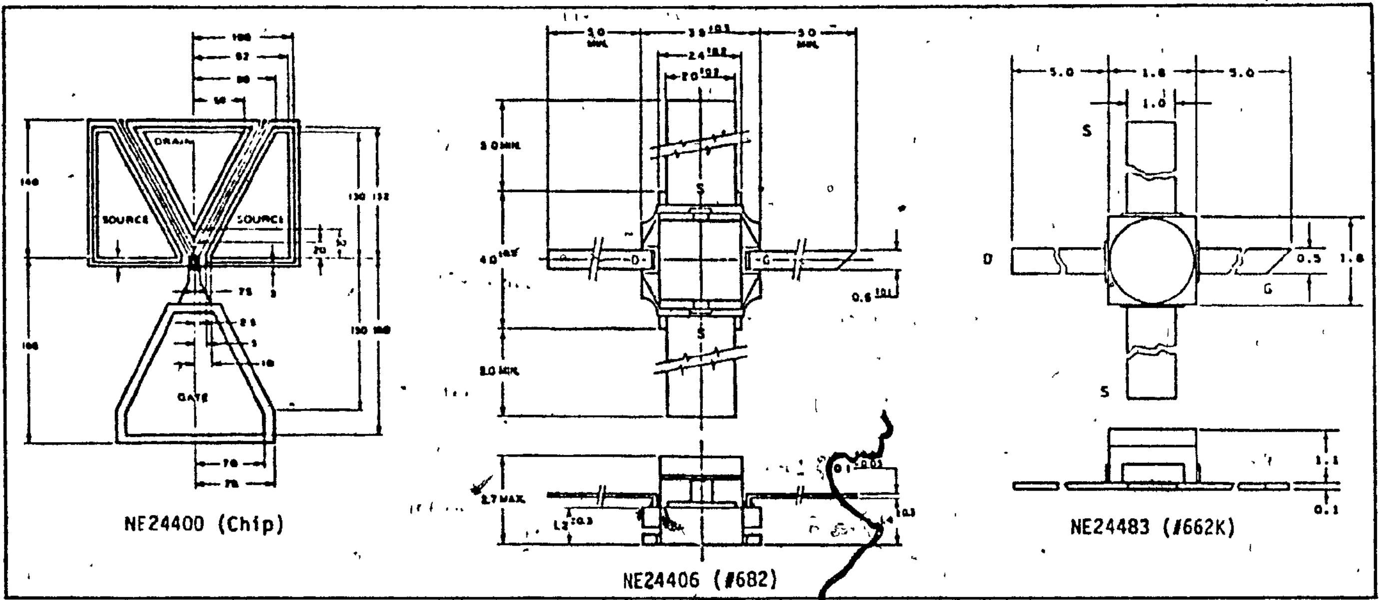
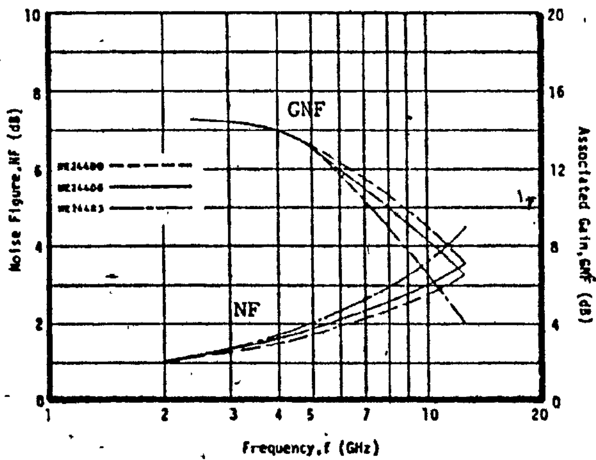
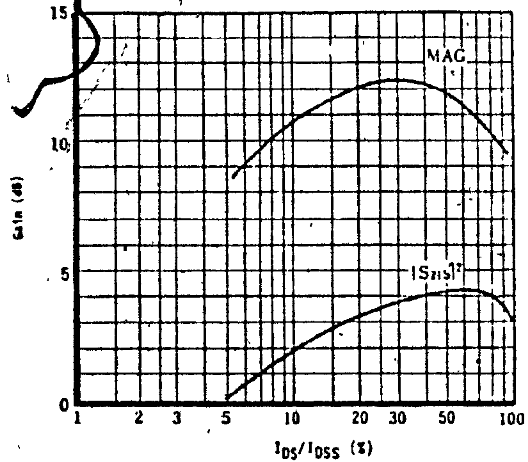
NE244 GaAs FET SERIES CHARACTERISTICS

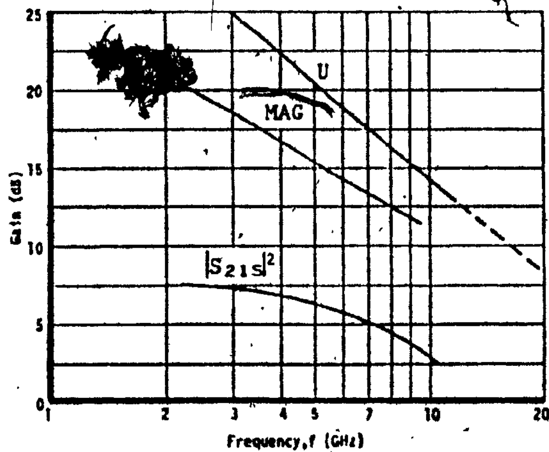




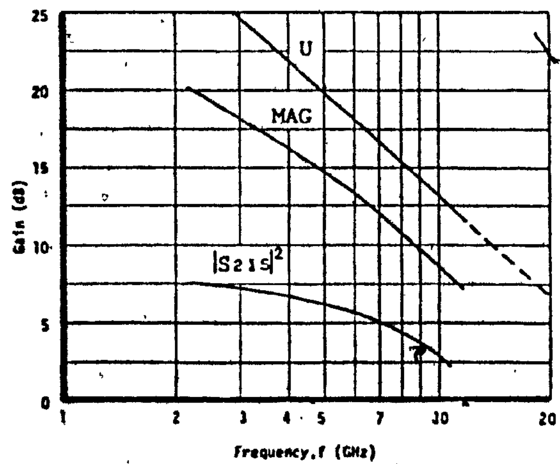
Typical Noise Figure And Associated Gain vs Frequency (V_{DS}=3V, I_{DS}=10mA)



Typical Gain vs Drain Current Ratio For the NE24406 (V_{DS}=3V, f=8GHz)

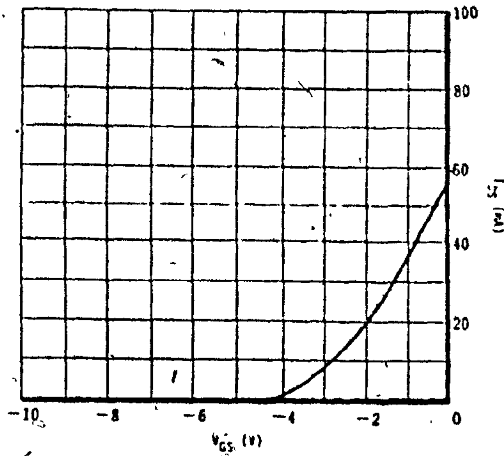


Gain vs Frequency Charateristics For The NE24406 (V_{DS}=3v, I_{DS}=50% I_{DSS})

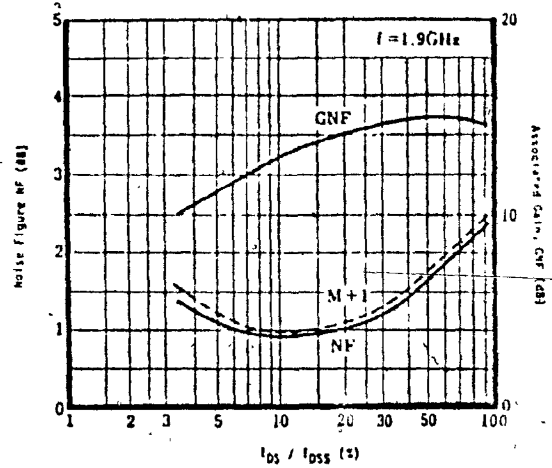


Gain vs Frequency Charateristics For The NE24483 (V_{DS}=3V, I_{DS}=50% I_{DSS})

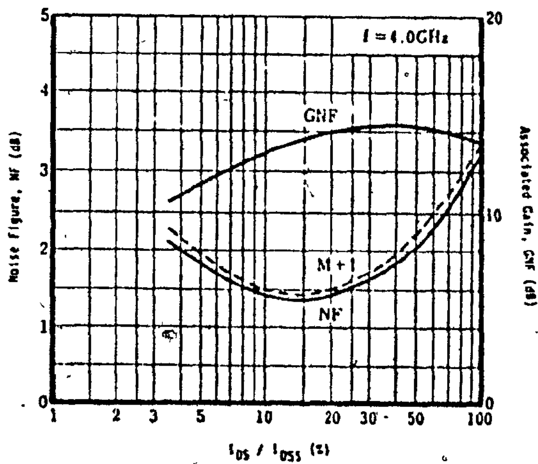
NE244 GaAs FET SERIES PERFORMANCE



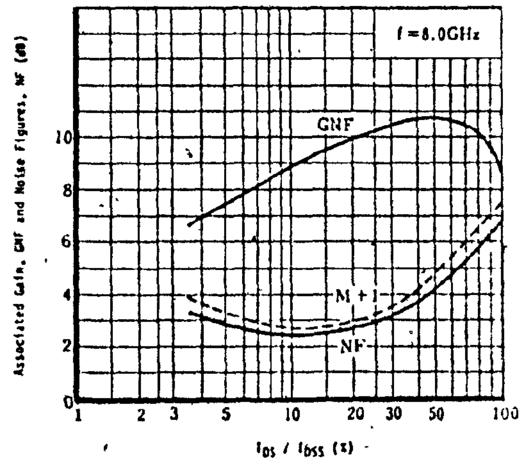
Drain Current vs Gate to Source Voltage



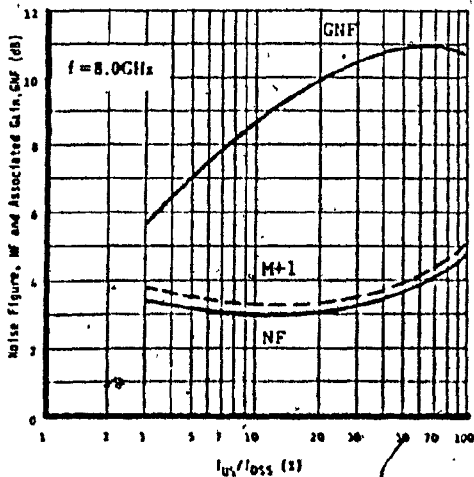
Typical Associated Gain at Optimized Noise Figure vs Drain Current Ratio For the NE24406 and NE24483 (V_{DS}=3V, f=1.9 GHz)



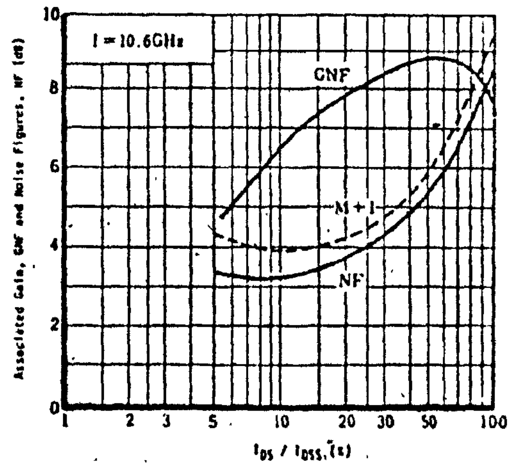
Typical Associated Gain at Optimized Noise Figure vs Drain Current Ratio For the NE24406 and NE24483 (V_{DS}=3V, f=4.0 GHz)



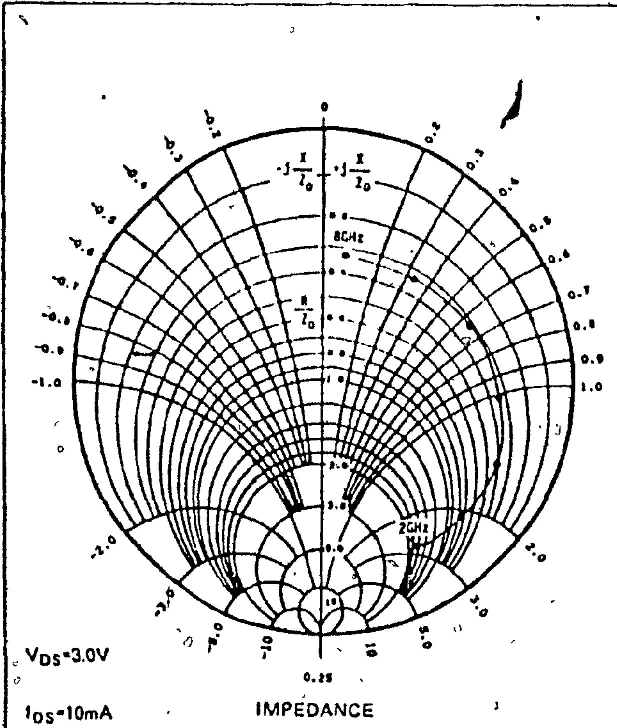
Typical Associated Gain at Optimized Noise Figure vs Drain Current Ratio For the NE24406 (V_{DS}=3V, f=8.0 GHz)

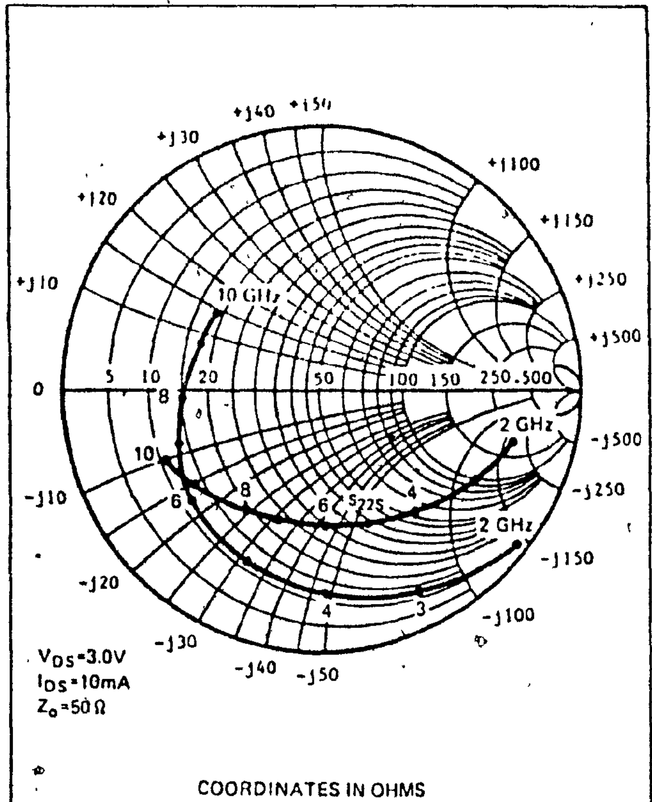


Typical Noise Figure And Associated Gain vs Drain Current Ratio for the NE24483 (V_{DS}=3V, f=8.0GHz)



Typical Associated Gain at Optimized Noise Figure vs Drain Current Ratio For the NE24406 (V_{DS}=3V, f=10.6 GHz)





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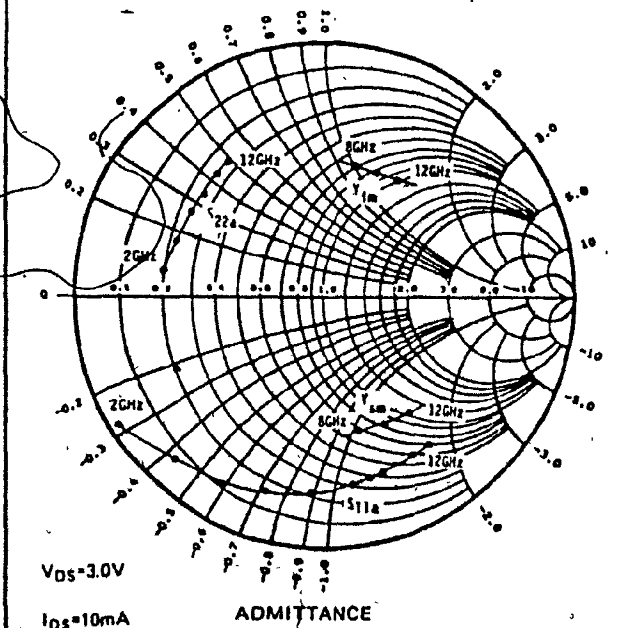
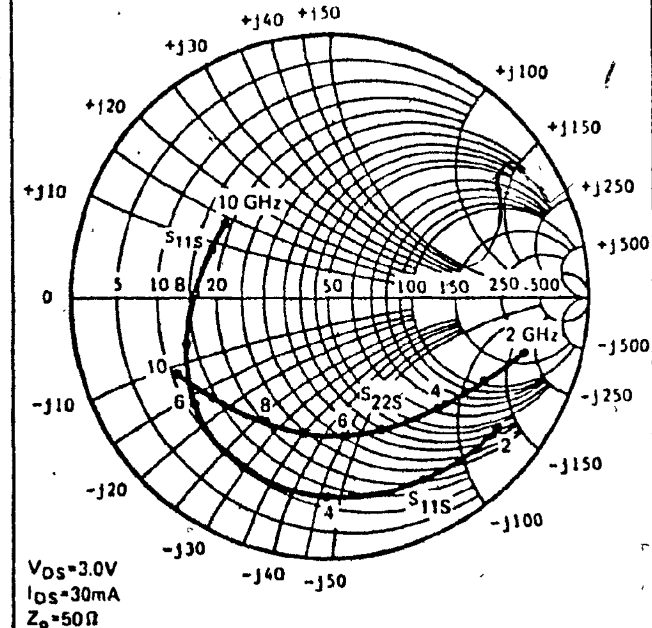




$S_{11a} = \frac{1-S_{11}}{1+S_{11}}$, $S_{22a} = \frac{1-S_{22}}{1+S_{22}}$

Y_{sm} = source admittance for minimum noise measure

Y_{im} = Y_{sm}^* (the termination of the filter which transforms 50Ω to Y_{sm})

Typical Source Admittance and Impedance Data for Optimum Noise Figure (NE24406)

Typical Common Source S-Parameters (NE24406)

NE244 GaAs FET CHIP (NE24400) COMMON SOURCE S-PARAMETERS

NE 24400 (Chip on #74124A Carrier)

VDS 3.0V, ID 10mA
S MAGN AND ANGLES

FREQ	11		21		12		22	
2000	979	−13	1 629	[illegible]	020	89	824	−2
3000	898	−25	1 578	[illegible]	027	83	774	−11
4000	895	−28	1 404	[illegible]	027	93	781	−14
5000	911	−32	1 314	[illegible]	028	103	808	−18
6000	906	−36	1 355	151	030	117	814	−22
7000	826	−45	1 528	144	042	116	734	−9
8000	749	−57	1 423	134	041	107	803	−15
9000	709	−69	1 340	126	042	106	779	−15
10000	647	−82	1 493	118	051	103	756	−16
11000	561	−89	1 208	108	058	106	701	−22
12000	590	−110	1 428	103	088	89	609	−38
13000	684	−127	1 290	83	073	86	591	−48
14000	604	−139	1 109	73	083	82	709	−75
14999	578	−146	998	75	098	81	737	−80

VDS=3.0V, ID=20mA
S MAGN AND ANGLES

FREQ	11		21		12		22	
2000	969	−16	1 866	164	018	90	810	−2
3000	892	−29	1 782	154	023	83	759	−11
4000	884	−33	1 614	153	021	97	765	−14
5000	894	−37	1 535	151	024	108	788	−17
6000	873	−43	1 549	146	026	119	771	−18
7000	784	−54	1 699	139	032	121	780	−12
8000	705	−68	1 574	129	033	121	703	−15
9000	666	−81	1 476	120	.036	123	761	−14
10000	596	−95	1 683	112	044	118	752	−15
11000	499	−101	1 260	104	.051	119	704	−20
12000	576	−123	1 481	100	065	102	632	−34
13000	593	−148	1 333	80	069	99	641	−55
14000	586	−151	1 168	69	078	97	725	−77
14999	550	−158	1 036	72	088	93	756	−89

VDS=3.0V, ID=30mA
S MAGN AND ANGLES

FREQ	11		21		12		22	
2000	973	−17	1 865	163	016	90	811	−1
3000	874	−31	1 768	152	021	87	768	−10
4000	872	−34	1 578	151	020	99	764	−13
5000	889	−40	1 486	149	022	112	788	−15
6000	863	−47	1 457	144	024	123	811	−16
7000	766	−59	1 638	139	028	128	808	−16
8000	687	−74	1 547	128	031	139	.783	−15
9000	650	−87	1 435	118	032	130	.765	−14
10000	.579	−102	1 549	109	041	128	757	−14
11000	502	−106	1 187	102	049	128	.712	−20
12000	573	−130	1 422	98	062	109	639	−33
13000	597	−146	1 274	79	067	107	649	−54
14000	589	−157	1 117	66	076	105	735	−76
14999	556	−165	.979	69	090	100	765	−88

VDS=3.0V, ID=40mA
S ... MAGN AND ANGLES.

FREQ.	11		21		12		22	
2000	956	−19	1 689	161	016	90	819	−1
3000	882	−32	1 635	151	.020	84	772	−10
4000	878	−37	1 464	149	019	99	777	−13
5000	886	−43	1 360	145	019	117	887	−16
6000	854	−50	1 359	144	025	139	817	−20
7000	754	−63	1 550	134	.032	137	668	−14
8000	675	−80	1 423	123	.032	136	805	−12
9000	638	−93	1.308	113	033	131	.786	−13
10000	565	−110	1 387	104	039	129	.776	−14
11000	489	−112	1 069	98	048	131	.726	−20
12000	580	−135	1 288	93	062	115	648	−34
13000	608	−152	1 146	74	.066	106	560	−57
14000	589	−163	1 014	61	074	106	.730	−70
14909	555	−170	.899	63	088	104	.768	−85

NE244 GaAs FET (NE24406) COMMON SOURCE S-PARAMETERS

NE24406

VDS=3.0V, ID=10mA
S -- MAGN AND ANGLES

FREQ	11		21		12		22	
2000	.966	-39	1.916	139	.031	64	.812	-26
2500	.916	-50	1.840	127	.027	52	.784	-33
3000	.910	-64	2.016	114	.034	43	.818	-42
3500	.882	-78	[illegible]	107	.036	33	.756	-51
4000	.893	-91	1.947	89	.043	26	.767	-61
4500	.860	-104	1.892	77	.044	12	.744	-70
5000	.808	-115	1.671	60	.020	35	.718	-77
5500	.835	-127	1.742	62	.032	15	.743	-86
6000	.799	-141	1.758	48	.033	3	.725	-97
6500	.793	-152	1.592	41	.033	5	.729	-106
7000	.761	-161	1.534	33	.032	3	.717	-114
7500	.760	-169	1.519	28	.025	5	.729	-129
8000	.743	-178	1.478	21	.028	20	.732	-126
8500	.743	175	1.434	14	.029	28	.732	-135
9000	.717	161	1.307	-9	.034	17	.755	-148
9500	.726	158	1.339	-15	.036	8	.783	-153
10000	.720	151	1.230	-24	.030	18	.809	-158

VDS=3.0V, ID=20mA
S -- MAGN AND ANGLES:

FREQ.	11		21		12		22	
2000	.922	-40	2.090	138	.018	64	.768	-25
2500	.857	-51	1.954	126	.020	61	.714	-32
3000	.869	-65	2.031	113	.027	43	.721	-40
3500	.830	-79	2.058	100	.028	35	.708	-49
4000	.888	-94	2.183	88	.034	28	.753	-60
4500	.850	-108	2.123	76	.033	12	.726	-68
5000	.797	-119	1.861	64	.018	-4	.716	-76
5500	.815	-129	1.948	61	.024	24	.728	-84
6000	.789	-144	1.909	45	.025	16	.710	-94
6500	.780	-154	1.767	40	.026	20	.721	-103
7000	.753	-164	1.683	31	.024	21	.701	-112
7500	.757	-171	1.676	27	.023	35	.727	-117
8000	.731	179	1.648	18	.020	43	.720	-126
8500	.735	174	1.541	12	.031	48	.730	-132
9000	.702	159	1.452	-11	.040	28	.739	-146
9500	.721	156	1.468	-16	.038	38	.788	-150
10000	.702	149	1.362	-26	.037	34	.799	-156

VDS=3.0V, ID=30mA
S -- MAGN AND ANGLES:

FREQ.	11		21		12		22	
2000	.921	-40	2.123	138	.014	64	.771	-25
2500	.848	-51	1.969	127	.016	58	.719	-31
3000	.874	-65	2.058	114	.023	45	.727	-39
3500	.824	-79	2.057	101	.022	39	.716	-49
4000	.890	-94	2.203	89	.028	38	.759	-59
4500	.848	-107	2.148	76	.031	27	.742	-67
5000	.809	-118	1.917	70	.025	23	.727	-77
5500	.820	-130	1.981	62	.020	18	.723	-83
6000	.794	-144	1.951	46	.018	16	.707	-93
6500	.784	-150	1.782	41	.017	30	.718	-101
7000	.752	-165	1.707	32	.018	48	.706	-109
7500	.753	-171	1.703	28	.027	57	.739	-116
8000	.736	179	1.675	20	.033	52	.727	-124
8500	.737	173	1.578	13	.033	53	.735	-130
9000	.708	158	1.473	-10	.038	36	.754	-144
9500	.722	156	1.485	-14	.041	39	.799	-149
10000	.704	149	1.392	-24	.041	42	.810	-155

VDS=3.0V, ID=40mA
S -- MAGN AND ANGLES:

FREQ.	11		21		12		22	
2000	.921	-41	2.006	138	.013	68	.781	-24
2500	.846	-52	1.856	126	.017	58	.741	-32
3000	.873	-66	1.947	113	.019	48	.731	-40
3500	.834	-79	1.948	101	.021	43	.722	-50
4000	.891	-95	2.085	88	.028	36	.767	-59
4500	.847	-107	2.022	76	.038	21	.749	-68
5000	.817	-120	1.841	67	.014	-60	.727	-76
5500	.824	-131	1.870	61	.016	45	.748	-83
6000	.794	-145	1.836	46	.017	41	.732	-91
6500	.783	-158	1.693	41	.020	50	.745	-103
7000	.753	-166	1.611	32	.023	57	.729	-112
7500	.755	-172	1.615	29	.023	66	.752	-118
8000	.735	178	1.590	20	.033	66	.745	-126
8500	.735	172	1.499	13	.037	67	.756	-132
9000	.702	157	1.407	-9	.045	47	.771	-148
9500	.722	165	1.410	-15	.047	43	.843	-151
10000	.701	148	1.327	-24	.040	47	.826	-156

NE244 GaAs FET (NE24483) COMMON SOURCE S-PARAMETERS

NE24483

VDS=3.0V, ID=10mA

S — MAGN AND ANGLES:

FREQ.	11		21		12		22	
2000	.965	-31	1.976	143	.027	69	.926	-16
2500	.894	-44	1.925	[illegible]	.033	63	.929	-26
3000	.820	-57	1.879	[illegible]	.037	60	.817	-37
3500	.737	-66	1.817	[illegible]	.044	60	.843	-42
4000	.906	-68	1.929	[illegible]	.036	65	.791	-41
4500	.857	-79	2.013	[illegible]	.038	63	.789	-47
5000	.818	-91	2.051	[illegible]	.038	60	.788	-54
5500	.769	-103	2.046	77	.037	60	.740	-63
6000	.742	-113	1.981	65	.038	67	.741	-72
6500	.712	-121	1.868	55	.041	71	.732	-79
7000	.663	-126	1.816	[illegible]	.046	82	.728	-84
7500	.648	-131	1.697		.053	89	.737	-87
8000	.644	-141	1.785		.066	87	.761	-90
8500	.611	-151	1.856	[illegible]	.083	83	.758	-96
9000	.610	-165	1.634	6	.087	80	.729	-101
9500	.575	179	1.595	-11	.088	79	.715	-105
10000	.537	161	1.473	-12	.112	79	.723	-115

VDS=3.0V, ID=20mA

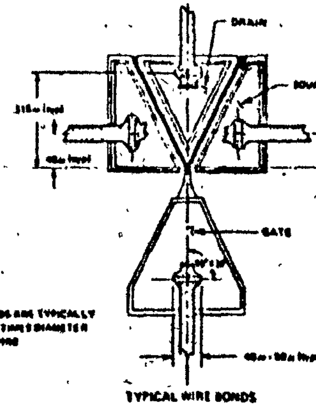
S — MAGN AND ANGLES:

FREQ.	11		21		12		22	
2000	.971	-30	2.087	144	.022	72	.802	-15
2500	.891	-42	2.028	135	.026	67	.753	-24
3000	.819	-56	2.001	123	.029	65	.707	-33
3500	.735	-65	1.928	118	.030	64	.647	-40
4000	.902	-67	2.037	116	.032	70	.759	-38
4500	.858	-79	2.120	105	.034	71	.758	-45
5000	.825	-91	2.147	93	.036	72	.757	-51
5500	.755	-103	2.103	78	.050	79	.713	-60
6000	.748	-113	2.034	67	.038	63	.714	-68
6500	.719	-120	1.913	58	.041	72	.706	-75
7000	.676	-125	1.847	51	.046	83	.706	-80
7500	.670	-129	1.713	46	.052	89	.717	-82
8000	.670	-137	1.793	35	.065	87	.739	-85
8500	.641	-145	1.870	28	.080	84	.742	-90
9000	.649	-156	1.677	14	.080	84	.726	-94
9500	.609	-167	1.589	-2	.081	83	.695	-99
10000	.579	-179	1.547	-4	.112	84	.701	-108

HANDLING PRECAUTIONS

To summarize, the NEC GaAs FET will provide the user with a good low noise, high-gain microwave amplifier with good yields, if the user adheres to the following:

1. Operate in a clean, dry environment.
2. Remember, the slashed lead on the package is the gate.
3. Ferret out and eliminate all sources of transients by properly grounding die-attach and bonding machines, and all test and assembly equipment.
4. Die-attach by hand (with qualified personnel) using any of these methods:
   a. 0.5 mil Au Ge preforms at 400° C±20° C for 3 seconds max.
   b. 0.5 mil Au Sn preforms at 300° C±20° C for 5 minutes max.
   c. Low temperature epoxy.
   d. Attaching Directly onto the gold substrate metallization.
5. Bond with a sapphire or SiC wedge probe and a thermal compression bonding machine using 0.7 mil (20μ) pure gold, half-hard wire. (User should perform incoming inspection on gold wire also. It may have striations which can produce "whiskers".) Gold mesh may also be used.
   a. If an Au-Ge preform is used, the chip face should be 300° C±5° C with the wedge at room temperature and force of 22±2 grams.
   b. If an Au Sn preform is used, the chip face should be 200° C with the wedge at sufficient temperature to bond at 22±2 grams of force.



GAIN CALCULATIONS

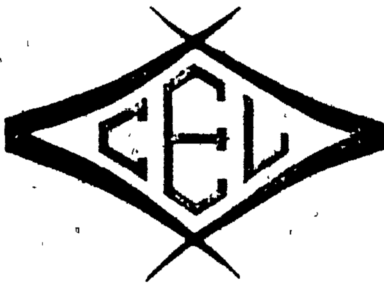
The gains for the NE244 GaAs FETs are calculated from the device S-parameters using the following equations:

$$U = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)}$$

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|\left(k \pm \sqrt{k^2-1}\right)$$

$$k = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$



CALIFORNIA EASTERN LABORATORIES, INC.

SORRY!

In our rush to get the V244-V388 Application Note published, we overlooked the following errors:

Page 2, right column, 15th line, word is "platinum" not "plantium".

Page 4, left column. Tests conducted after the printing of the Application Note show good results with very thin films of SiO_2. Therefore, NEC will put glassivation films on all V244 chips starting in October 1976.

Page 8, right column, equations should include:

$$M = \frac{F-1}{1-1/Ga}$$

Page 15, right column, line 37, change "collect" to "collet".

Page 17, Figure 22, change "Return Loss (dbm)" to "Return Loss (dB)".

Page 10, Figure 12, Admittance chart, change S_{11} and S_{22} to S_{11a} and S_{22a} where:

$$S_{11a} = \frac{1-S_{11}}{1+S_{11}}, \qquad S_{22a} = \frac{1-S_{22}}{1+S_{22}}$$

Y_{sm} = source admittance for minimum noise measure

Y_{im} = Y_{sm}^* (the termination of the filter which transforms 50Ω to Y_{sm})

APPENDIX C

S-PARAMETER, THEORY AND DESIGN

APPENDIX C

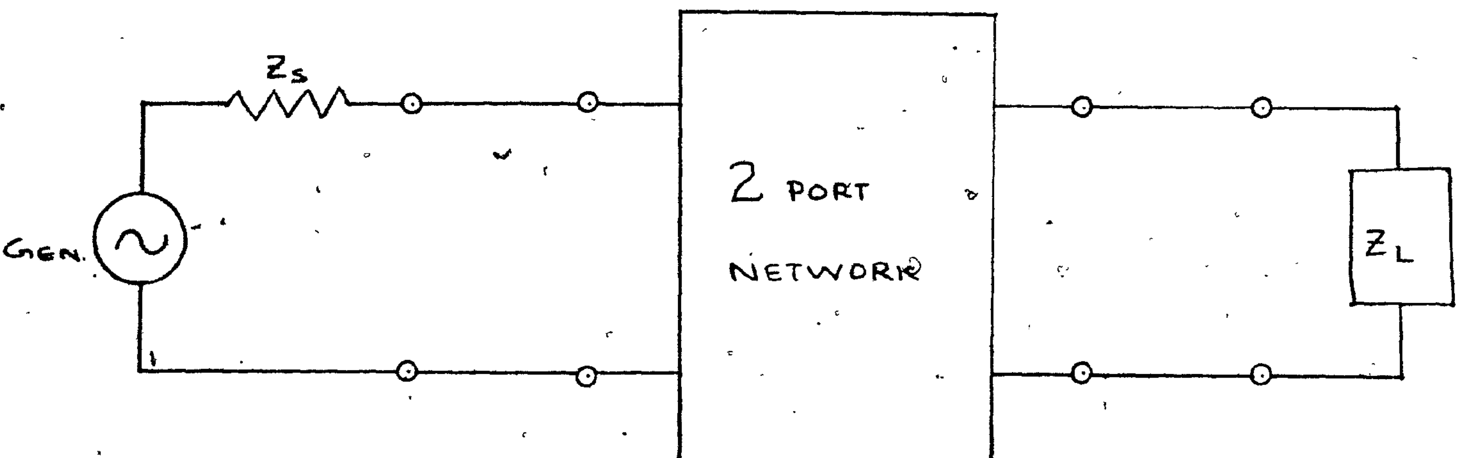
S-Parameters

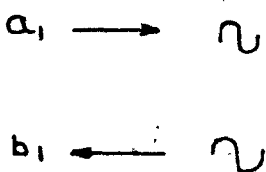
Introduction

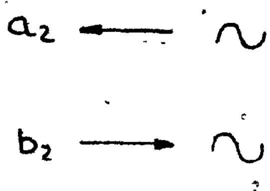
Appendix B presents the manufacturers data sheet on NE244 transistor (and as the packaged versus is called, NE24406). The configuration often used, is with the source terminal common to input and output and is ofter called the grounded source or common source connection. This section will present a S-parameter review, and then discuss the practical realities in S-parameter measurement and design at these microwave frequencies.

S-Parameter Review

Before introducing the design concepts, let us briefly review S-parameters. As opposed to the more conventional parameter sets which relate total voltages and total currents at the network ports, S-parameters relate travelling waves. (Figure C-1). The incident waves, a_1 and a_2, are the independent variables and the reflected waves, b_1 and b_2, are the dependent variables. The network is assumed to be embedded in a transmission line system of known characteristic impedance which shall be designated Z_o. The S-parameters are then measured with Z_o termination on each of the ports of the network. Under these conditions, S11 and S22, the input and output reflection coefficients, and S21 and S12, the foreward and reverse transmission coefficients







if $Z_L = Z_o$, $a_2 = 0$

Figure C-1: S-Parameter Notation

can be measured, as below:

$$S_{11} = \frac{b_1}{a_1}\bigg|_{a_2=0} \qquad S_{21} = \frac{b_2}{a_1}\bigg|_{a_2=0}$$

$$S_{12} = \frac{b_1}{a_2}\bigg|_{a_1=0} \qquad S_{22} = \frac{b_2}{a_2}\bigg|_{a_1=0} \qquad (C-1)$$

This is easy to see, since the transmission line is terminated in the characteristic impedance of the line, the network port does not have to be matched to that impedance as well. If the load impedance is equal to the characteristic impedance of the line, any wave travelling toward the load would be totally absorbed by the load. It would not reflect back to the network. This sets $a_2=0$. This condition is completely independent from the network's output impedance.

These S-matrices can be multiplied together, to give overall cascade network characterization. Let us now shift our attention to the actual S-parameters of a transistor. For an amplifier, the entire circuit is modelled as shown in Figure C-2.

The intrinsic elements,[1] (Ref. J.Cooper, M.Gupta and M.W.Chan of "GaAs MESFET and the device model", IEEE Journal of S.S. Circuits, June 1977) shown in Figure C-3(a) are similar to those presented in the text and used by many authors. The transconductance of the device g_m, the output resistance R_d, the gate-to-source capacitance C_{gs}, and the gate-to-drain capacitances C_{dg} are shown. Also shown is

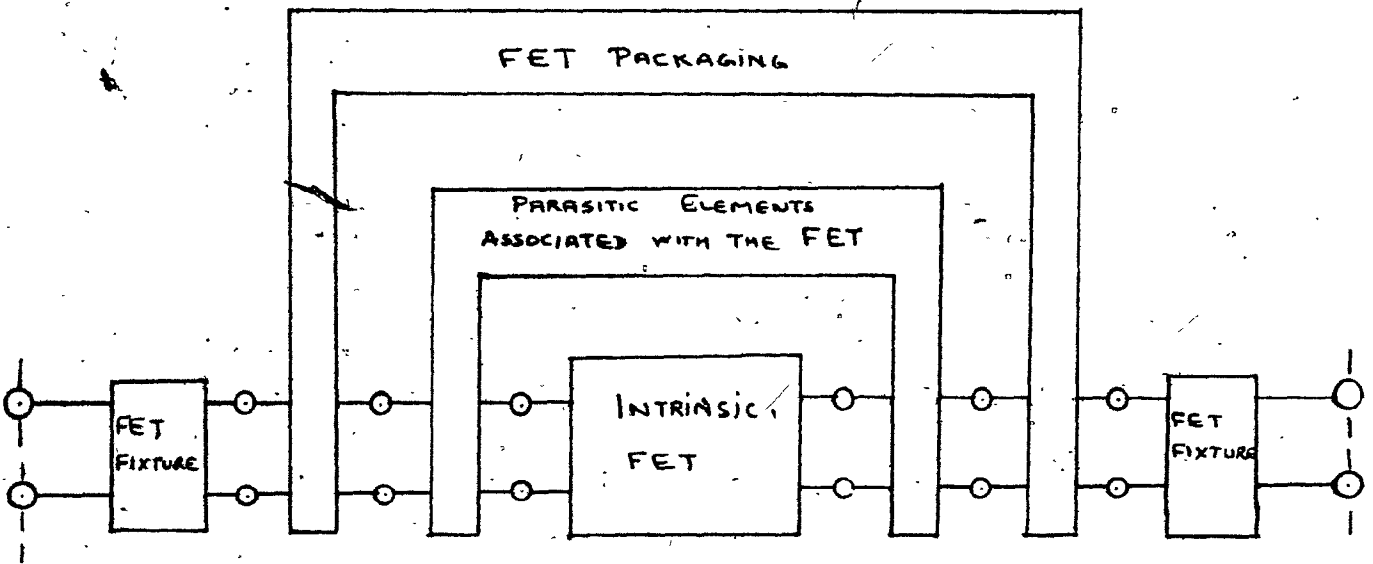


Figure C-2: Port-wise Models for the Intrinsic FET, Device Parasitics, Package, and Fixture Circuit.

the undepleated channel resistance R_i.

The expression for the intrinsic elements, g_m, R_d, C_{gs} and C_{gd} are not reproduced here. However, they relate the four elements to the semiconductor material properties (namely, low-field mobility, epitaxial layer, dielectric constant, and built-in potential), device structural dimensions (device width, gate length, source-to-gate and gate-to-drain interelectrode spacings, and epitaxial layer thickness), and device d.c. bias (V_{DD} and V_{GG}). The other six device parasitic elements, have three electrostatic capacitances, estimatable from a knowledge of the geometry of metallizations on the chip, with correction applied for fringing. The three extrinsic resistances are measurable by dc current and voltage measurements, treating the intrinsic FET as two p-n junctions across a conductive channel. The general expressions are:

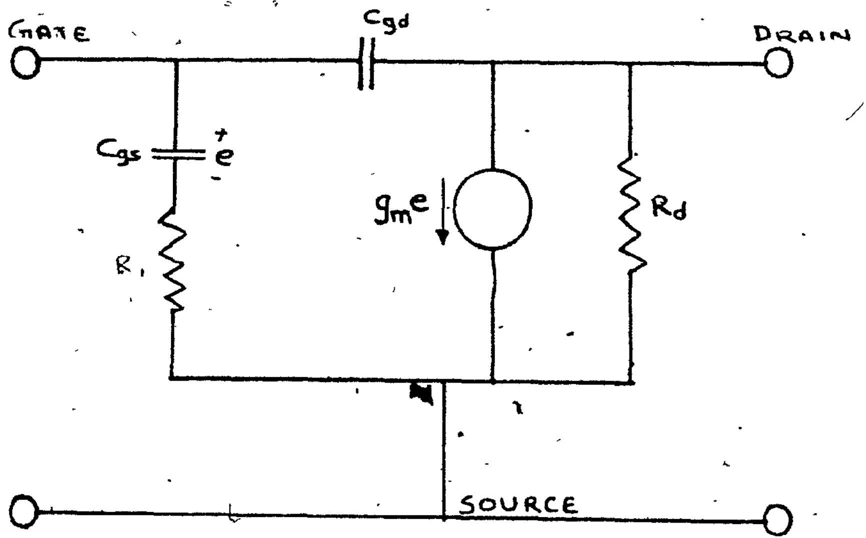
$$R_F = \frac{\Delta V_{ds}}{\Delta I_{gs}} \quad ; \quad R_m = \frac{\Delta V_{gd}}{\Delta I_{gs}} \quad ; \quad dr = \frac{\Delta V_{sd}}{\Delta I_{gd}} \qquad (C-2)$$

The extrinsic elements, and parasitic elements associated with the FET chip are shown in Figure C-3(b). The three resistances R_m, R_{dr} and R_f, in series with the gate, drain, and source terminals, respectively, are due in part to the contact resistance at the metallization and in part to the bulk resistance of the semiconductor. The capacitors C_{gd1}, C_{gs1} and C_{ds1} arise due to the capacitances between the various metallizations on the chip.

The package parasitic elements, add three sets of parasitics which are shown in Figure C-3(c). They include the inductors L_1, L_2 and L_3 representing package leads and bonding pad inductances, the capacitors C_1, C_2, C_3 representing capacitances between the three bonding pads, and inductors L_4, L_5 and L_6 representing bonding wire inductances.

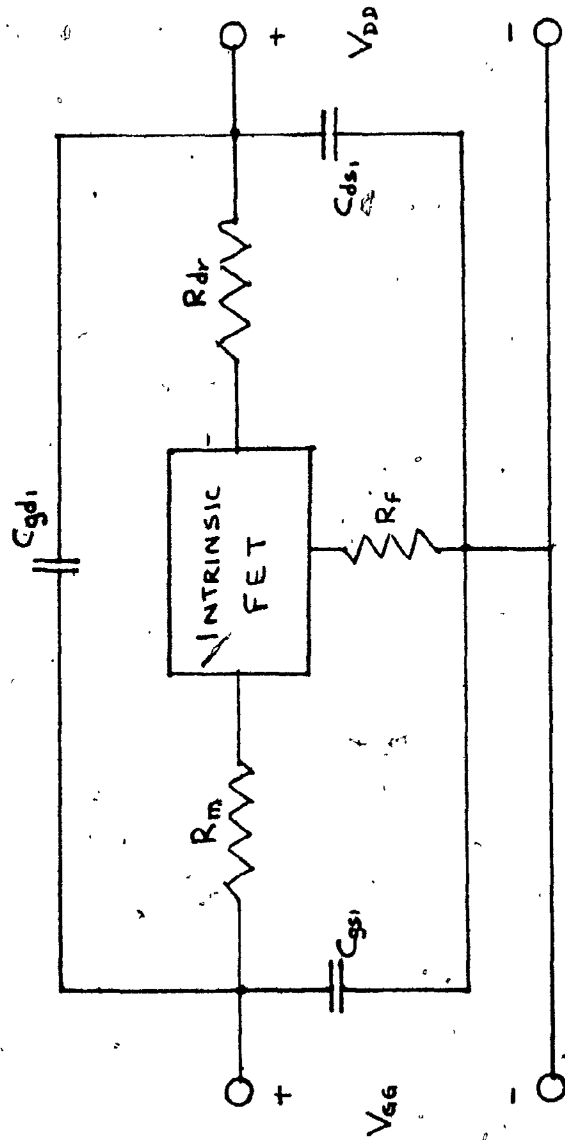
The Test fixture parasitics, model of Figure C-3(d), for an amplifier or characterization circuit would consist of; on one side of the packaged device, two transmission lines of length l_3 and l_1, representing the connector and the microstrip, respectively, and an inductor L_{f5} representing the interconnection of the two lines. The attenuator A_{s1} accounts for the line loss. A similar model is used on the other side of the packaged device. The bias feed network, as was explained in the text, are transparent at the R.F. frequencies of interest, and for simplicity have been neglected. However, their inclusion would only require a more detailed model for l_1 and l_2.

For our discussion we will restrict ourselves to Figure C-3(d). The manufacturer supplies the packaged FET S-parameters, for amplifier application. It is important to re-emphasize this point because now we will discuss the reality of mixer design using CAD (Computer Aided Design) techniques.

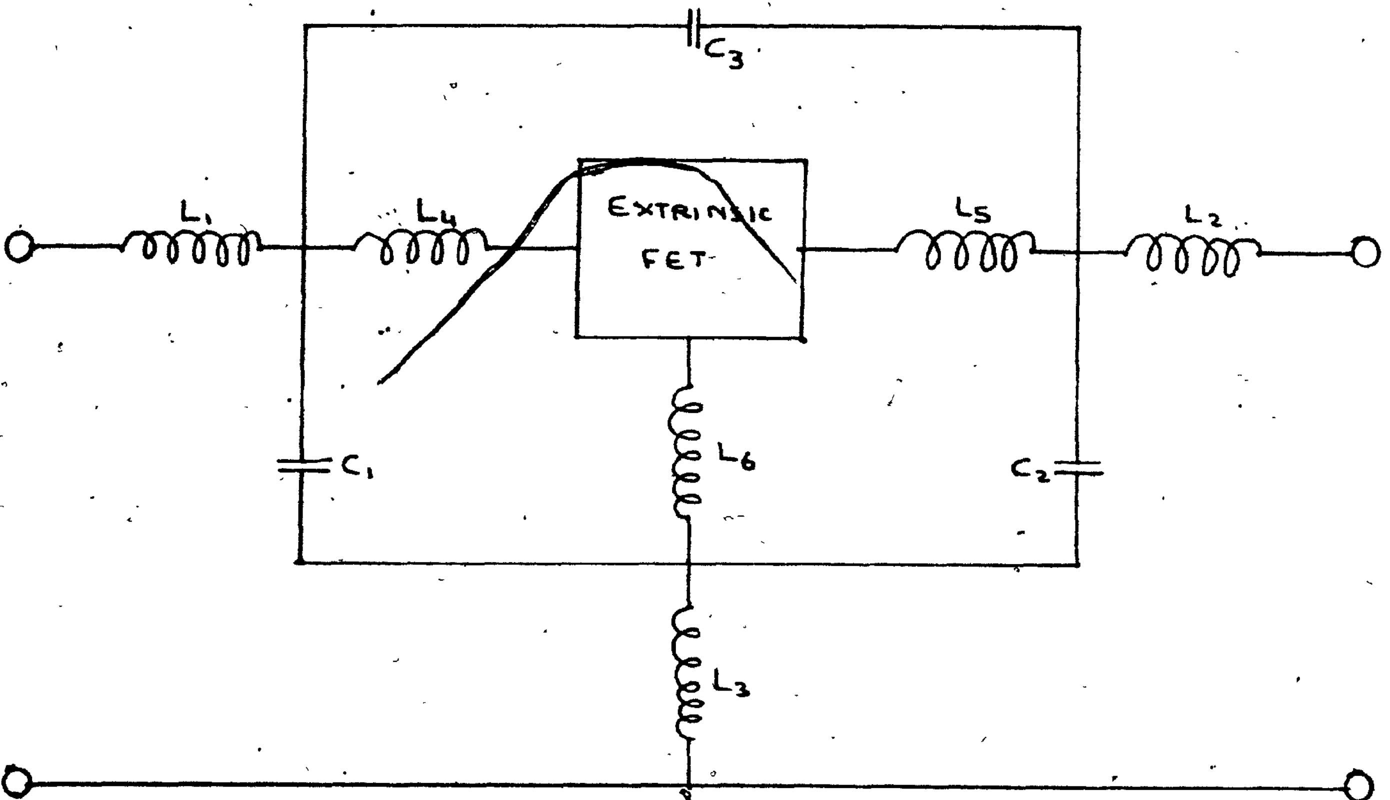


C-3 (a): Intrinsic FET

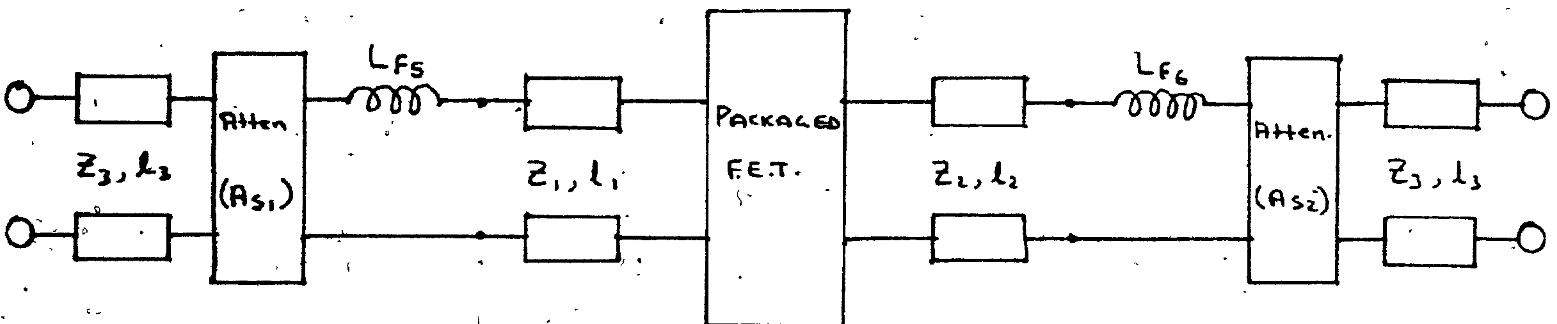
Figure C-3: Detailed circuit models for (a) the intrinsic FET, (b) the extrinsic FET which includes the device parasitics, (c) the packaged FET, and, (d) the packaged FET mounted in an amplifier or characterization test fixture.



C-3 (b): Extrinsic FFT



C-3 (c): Packaged FET



C-3 (d): Mounted FET

S-parameter measurements, are made using a network analyzer. At present, most test instruments are restricted to single frequency analysis. That is to say, the device under test must not translate the frequency. Therefore, a device (FET) may be biased in the non-linear mixing region, but no measurements with the L.O. pumping can be made. This necessarily limits our raw S-parameter data for two reasons:

(i) Operating in the non-linear region, the validity of S-parameter measurements, using network analyzer techniques, is in doubt. Due to the nature of the non-linearity, the signals reflected to the test analyzer are only a fraction of the actual reflected signals, as self mixing ($y \approx x^2$) shifts signals out of measuring range;

(ii) The L.O. pump, which of course translates the signals, also modulates g_m and other FET parameters. The effect of these changes, especially under large signal R.F. condition (typically input signal is -40 dBm, while the L.O. signal is +10 dBm) is not measurable.

The manufacturer supplied S-parameters are at best only a first iteration starting point for the required matching network, and tuning, or optimizing must be done empirically.[2] Without a satisfactory means of S-parameter measurement for mixer condition, an optimum analytic design is at present not possible. *(Note 1).

Still as indicated in the text, first cut designs for matching circuits are possible if we design the input circuit for a 6 GHz low noise amplifier, and the output circuit for a high gain amplifier. The references on FET mixers are particularly shallow

on this point, and in fact all ignore this problem. The majority of mixers presented deal with very low I.F. (about 70 MHz) with negligible bandwidths. The only significant results on mixer using FETs and considering the bandwidths/flatness problem was Burg et al.[3]

The CAD process itself can be shown in block diagram form in Figure C-4.[4] The story is not all roses. The value of using computerized techniques when designing competitive microwave circuit is clear. However, every once in a while Murphy's law strikes, and the end result of a computer assisted design does not work. And especially in the case of a mixer, the solution often lies on the bench rather than at the computer terminal.

Note 1: The author has tried several schemes of evaluating and directly measuring FET S-parameters under mixer bias and L.O. pumping. Most of these were not feasible due to significant measurement uncertainties. However, an amplitude modulation scheme shows promise. But, as this is a patentable process, it is not possible to give details herein.

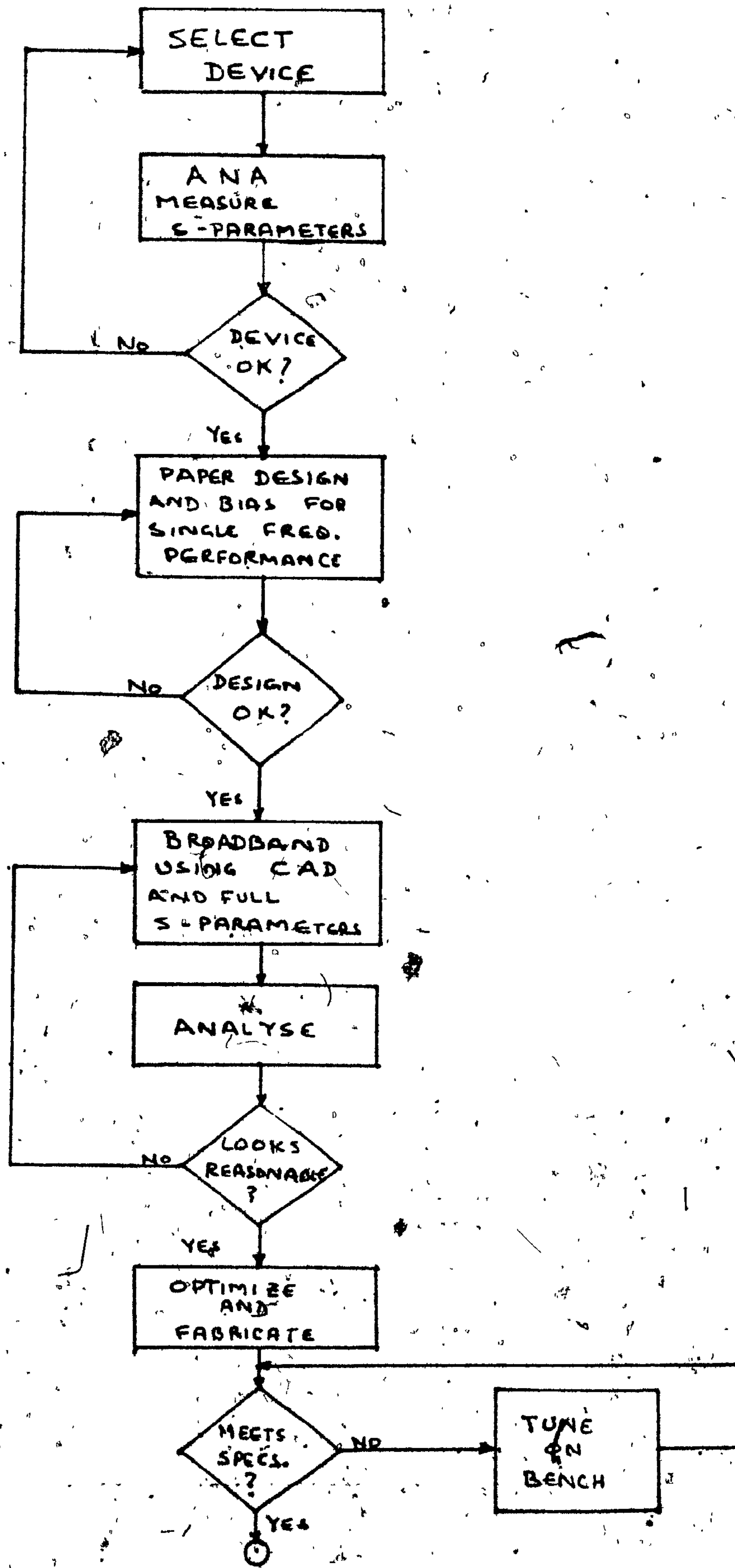


Figure C-4: The CAD Process

APPENDIX D

FET MIXER NOISE FIGURE EQUATION DERIVATION

APPENDIX D

The FET Mixer Noise Figure Equation Derivation

(Ref. Pucel et al) [1]-[4]

To calculate the FET mixer noise figure the total output short circuit noise current $\overline{i^2_{out}}$ must be evaluated. Figuer D-1 is a schematic for calculating the total output short-circuit noise current. Let the mixer be represented by the Y matrix and the total output short-circuit is given by:

$$i_{out} = (V_4 + V_{ng})\,Y_{21} + (V_{nd} + V_i)\,Y_{22} \qquad (D-1)$$

where V_i = the thermal noise voltage generated by R_d and R_s at the IF frequency,

V_4 = the thermal noise voltage generated by R_m, R_s, and R_g at the RF frequency ω_s,

V_{ng} and V_{nd} are the equivalent induced gate noise voltage and the channel noise voltage, respectively.

Rewriting the above equation, we have -

$$i_{out} = (Y_{21} V_4 + Y_{22} V_1) + (Y_{21} V_{ng} + Y_{22} V_{nd}) \qquad (D-2)$$

The mean square noise current $\overline{i^2_{out}}$ is given by:

$$\left|\overline{i^2_{out}}\right| = \left|\overline{\left[(Y_{21} V_4 + Y_{22} V_1) + (Y_{21} V_{ng} + Y_{22} V_{nd})\right]^2}\right| \qquad (D-3)$$

rewriting and neglecting the uncorrelated terms, we get

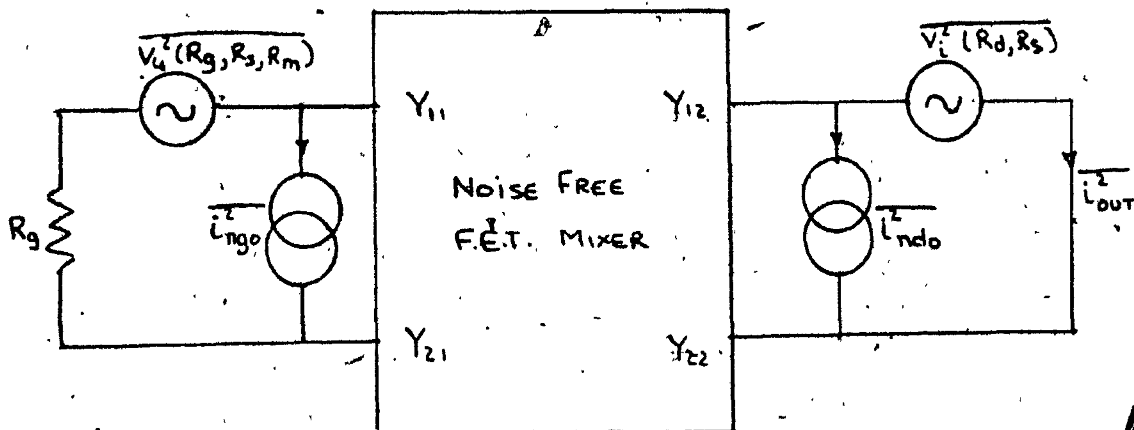


Figure D-1: Model for Calculating the FET Mixer Noise Figure

$$\left|\overline{i^2_{out}}\right| = \left|Y_{21}\right|^2 \overline{V_4^2} + \left|Y_{22}\right|^2 \overline{V_1^2} + \left|\overline{(Y21\ V_{ng} + Y_{22}\ V_{nd})}\right|^2 \quad (D-4)$$

where the noise voltages are:

$$\overline{V_4^2} = 4\,kTB\ (R_s + R_m + R_g) \quad (D-5)$$

$$\overline{V_1^2} = 4\,kTB\ (R_s + R_d) \quad (D-6)$$

$$V_{nd} = R_{ds}\ i_{nd} \quad (D-7)$$

$$V_{ng} = (R_i - J/W_s\ C_{gs})\ i_{ng} \quad (D-8)$$

Let us define $i_{ngo} = Y_{21}\ V_{ng} = Y_{21}(R_i - J/W_s C_{gs})\ i_{ng}$ (D-9)

and $i_{ngo} = Y_{22}\ R_{ds}\ i_{nd} = i_c + i_n$ (D-10)

thus

$$\left|\overline{(Y21\ V_{ng} + Y22\ V_{nd})}\right|^2 = \left|\overline{i_{ngo} + i_{ndo}}\right|^2 = \left|\overline{i^2_n}\right| + \left|i^2_{ndo}\right|^2 \left|\overline{1 + \frac{i_c}{i_{ndo}}}\right|^2 \quad (D-11)$$

$$\left[\overline{\frac{i_c}{i_{ndo}}}\right] = \left[\frac{i_c}{i_{ndo}}\ \frac{i^*_{ndo}}{i^*_{ndo}}\right] = \left[\frac{\overline{(i_{ngo} - i_n)\ i^*_{ndo}}}{\overline{i^2_{ndo}}}\right] = \left[\frac{\overline{i_{ngo}\quad i^*_{ndo}}}{\overline{i^2_{ndo}}}\right] \quad (D-12)$$

and $i\,C_{nd} = \dfrac{\overline{i^2_{ngo}\ \ i^*_{ndo}}}{(\overline{i^2_{ndo}}\ \overline{i^2_{ngo}})^{\frac{1}{2}}}$; where C_{nd} = the correlation coefficient between i_{ngo} and i_{ndo} (D-13)

$$\left[\overline{\frac{ic}{i_{ndo}}}\right] = i\,C_{nd}\left[\frac{(i^2_{ngo}\ i^2_{ndo})}{i^2_{ndo}}\right]^{\frac{1}{2}} \quad (D-14)$$

and

$$\overline{\left|(Y_{21} V_{ng} + Y_{22} V_{nd})\right|^2} = \left|\overline{i_n^2}\right| + \left|\overline{i^2_{ndo}}\right| + \left|1 + j \frac{C_{nd} (\overline{i^2_{ngo}}\ \overline{i^2_{ndo}})^{\frac{1}{2}}}{i^2_{ndo}}\right|^2 \qquad (D-15)$$

where $$i_n^2 = i^2_{ngo} - i_c^2 = i^2_{ngo} (1 - C^2_{nd}) \qquad (D-16)$$

The available mean square short-circuit current noise at the mixer outputs due to the R.F. source termination is $\overline{i^2_{R_g}} = |Y_{21}|^2 \overline{V^2_{Rg}}$ (D-17)

where $$\overline{V^2_{Rg}} = 4\, kTBR_g \qquad (D-18)$$

The mixer noise figure is defined as -

$$F = \frac{\left|\overline{i^2_{out}}\right|^2}{\left|i^2_{Rg}\right|^2} \qquad (D-19)$$

$$= 1 + \frac{R_m + R_s}{R_g} + \frac{|R_i + j X_s|^2 (1 - |K_{nd}|^2) g_{gn}}{R_g} + \frac{R_s + R_d}{R_g} \left|\frac{Z_{11} + Z_g}{Z_{21}}\right|^2$$

$$+ \frac{g_{dn} R^2_{ds}}{R_g |Z_{21}|^2} \left| Z_g + Z_{11} - \frac{jC\ (R_i - j X_s) Z_{21} (g_{gn}/g_{dn})^{\frac{1}{2}}}{R_{ds}} \right|^2 \qquad (D-20)$$

where $g_n = (\omega_s C_{in})^2 / g_o R$ (D-21)

$d_n = 2/3 g_o + (\omega_o C_{in})^2 S$ (D-22)

g_o is the fundamental fourier coefficient of transconductance g_m

C_{in} is the input capacitance $= I_m (Y_{11} - Y_{12} Y_{21} / (Y_{os} + Y_{22})) / \omega_s$, (D-23)

R is a factor dependent on bias ($\simeq 0.3$),

S is a factor dependent on pinch off voltage ($\simeq 0.15$),

Z_g is the RF signal impedance in the gate circuit,

Z_{ij} is the inverse of the [Y] matrix,

$X_s = 1/\omega_s C_{gs}$ (D-24)

C_{gs} = gate to source capacitance

ω_s and ω_o are the RF and IF radian frequencies

Thus, $F = 1 + \frac{R_n}{R_g} + \frac{G_n}{R_g} | Z_g + Z_{cor} |^2$ (D-25)

where $R_n = R_s + R_m + | (R_i - jX_s) |^2 (1 - |C_{nd}|^2) g_{gn}$ (D-26)

$G_n = \frac{g_d R_{ds}^2}{|Z_{21}|^2}$ (D-27)

and $Z_{cor} = Z_{11} - \frac{j^C (R_i - jX_s) Z_{21} (g_{gn}/g_{dn})^{\frac{1}{2}}}{R_{ds}}$ (D-28)

APPENDIX E

CIRCUIT DESIGN DETAILS

APPENDIX E

CIRCUIT DESIGN DETAILS

This appendix will describe the detailed calculation for the circuit of the FET mixer. It was felt that since this is a very particular solution for the FET mixer problem, detailed calculations were out of place in the main text. The design described herein is based on the author's own work, and details an actual 6/4 GHz gate injected local oscillator FET mixer.

Figure E-1 shows the block diagram of the gate mixer. This figures shows the detailed filtering requirements of the circuit, as well as the expected filter responses. The filter design is such that we have optimum amplitude/phase in the pass/stop band and all undesired frequencies are reactively (or with large reflection coefficients) terminated. However, mixer filters must provide specific terminations to different out-of-band frequencies. The optimum imbedding network must present either a short-circuit or an open circuit to each of the out-of-band frequencies. The isolation requirement is an attempt to achieve this. There are five sections to be considered, and these are the:

(i) L.O. filter,

(ii) Input band pass filter,

(iii) Input matching circuit,

(iv) Output matching circuit,

(v) MIC computer program

EFFECTIVE LOW IMPEDANCE PLANE @ 2225 MHz

λ/4 @ 2225 MHz

5925 to 6425 MHz

R.F. INPUT FILTER

TRANSISTOR

OUTPUT FILTER

3700 to 4200 MHz

λ/4 @ 6175 MHz

L.O. INPUT FILTER

EFFECTIVE LOW IMPEDANCE PLANE @ 6175 MHz

2225 MHz

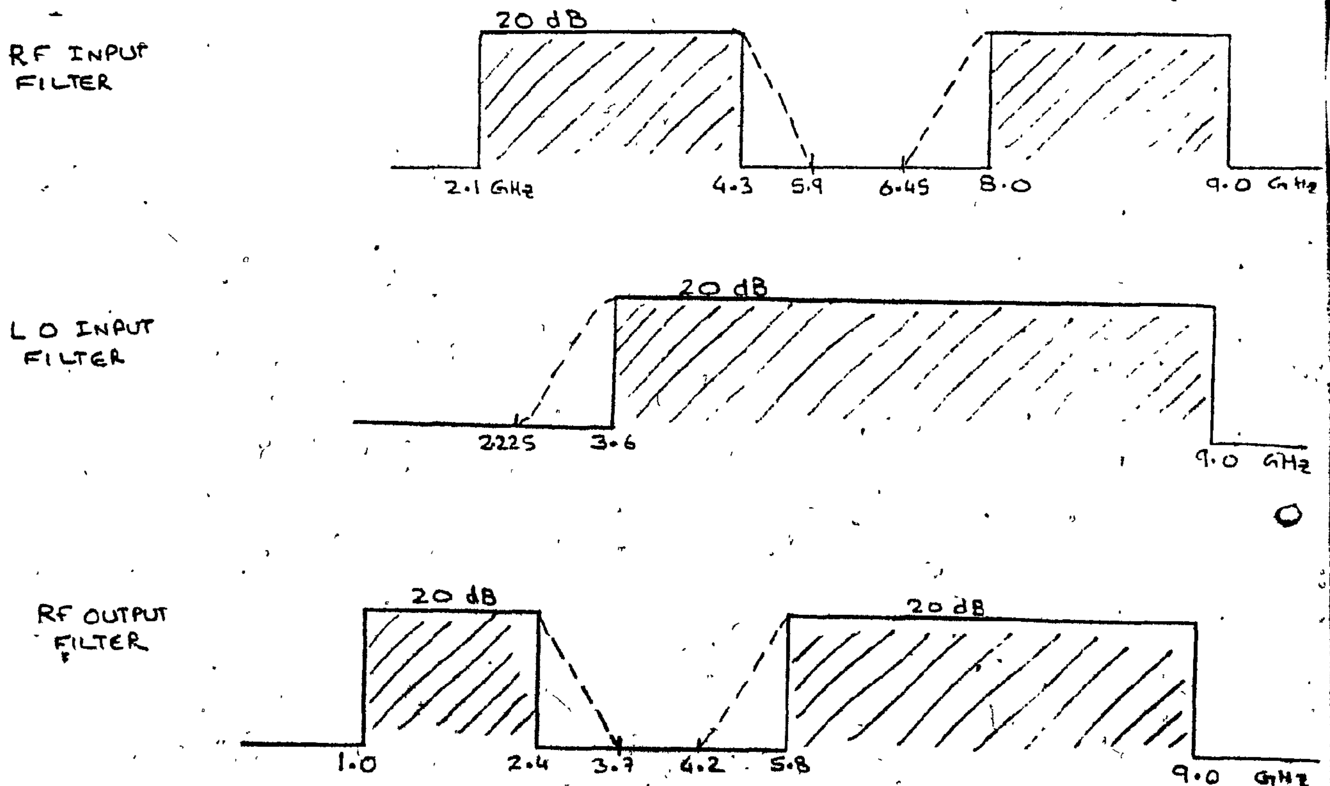


Figure E-1: Mixer Filters

NAME

Figure E-6: 6 and 4 GHz Match

IMPEDANCE OR ADMITTANCE COORDINATES

CANADIAN CHARTS & SUPPLIES
OAKVILLE MONTREAL
G9-756N82BSPR (Smith)

RESISTANCE COMPONENT $\left(\frac{R}{Z_0}\right)$, OR CONDUCTANCE COMPONENT $\left(\frac{G}{Y_0}\right)$

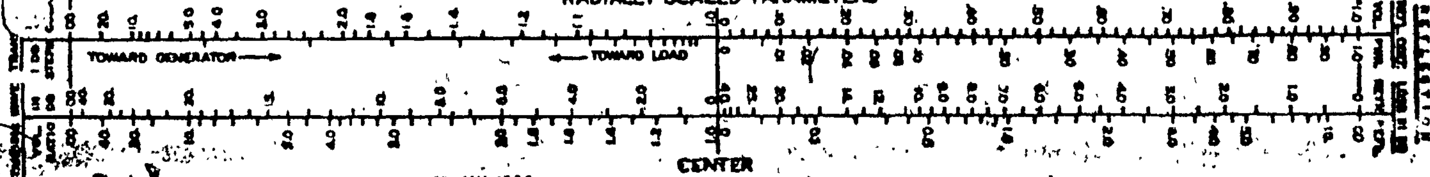
INDUCTIVE REACTANCE COMPONENT $\left(\frac{+jX}{Z_0}\right)$, OR CAPACITIVE SUSCEPTANCE COMPONENT $\left(\frac{+jB}{Y_0}\right)$

CAPACITIVE REACTANCE COMPONENT $\left(\frac{-jX}{Z_0}\right)$, OR INDUCTIVE SUSCEPTANCE COMPONENT $\left(\frac{-jB}{Y_0}\right)$

WAVELENGTHS TOWARD GENERATOR

WAVELENGTHS TOWARD LOAD

ANGLE OF REFLECTION COEFFICIENT IN DEGREES



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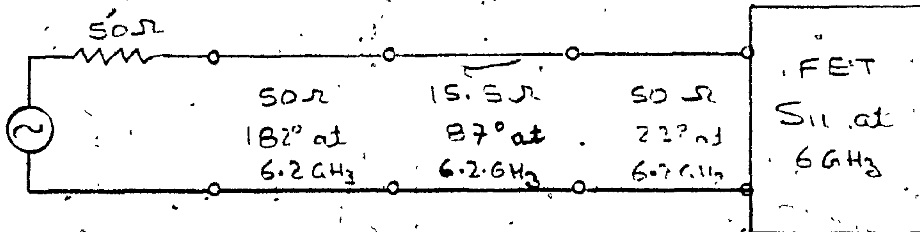

Figure E-7: Input Match Circuit

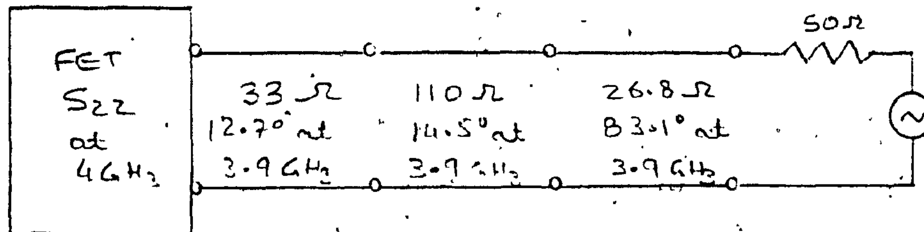

Figure E-8: Output Match Circuit

(v) This section lists the I/O of the calculator based program used in this micro-strip circuit design. The program calculates W/H, given Z_0, and the operating frequency. The formulae used are given in the text, Chapter 3.1, and the input and output format is presented below along with the program listing.

Input data

(1) The desired impedance (ohms)

(2) The operating frequency (GHz)

(3) The dielectric constant

(4) The thickness of the substrate (cms)

(5) The loss tangent

(6) The track thickness (cms)

Output data

(1) The ratio W/H

(2) The guide wavelength (cm)

(3) The attenuation in $dB/\lambda g$