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A NOVEL HIGH PERFORMANCE CURRENT REGULATED DC/AC CONVERTER FOR SINGLE PHASE AND THREE PHASE SYSTEMS

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ABSTRACT

A NOVEL HIGH PERFORMANCE CURRENT REGULATED DC/AC CONVERTER FOR SINGLE PHASE AND THREE PHASE SYSTEMS

Navid Reza Zargari

Standard single phase dc/ac converters use four high frequency switches. Reduction in the number of high frequency switches can reduce the cost, weight and size of the inverter and result in a better overall system reliability. This thesis proposes a novel power circuit configuration. It uses a two-switch topology which eliminates the shoot-through paths across the dc bus. Furthermore, in order to obtain a sinusoidal output waveform, this waveform must be directly or indirectly controlled by using a suitable waveshaping technique. The two-switch topology is therefore associated with an active current control waveshaping technique to obtain a high quality sinusoidal output voltage. Unlike other techniques this one controls the filter capacitor current, which produces sinusoidal output voltages whatever the type of load. The main features of the overall system include low and constant switching frequency, no added distortion with non-linear load, and fast voltage transient response to load changes. Furthermore, the three phase implementation is simple. The thesis presents design considerations and guidelines for the power and control circuits for single and three phase

configurations. Simulation and experimental results confirm the feasibility and attractive features of the proposed system.

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LIST OF ACRONYMS

BBH	bang-bang hysteresis
mH	mili Henry
PI	proportional integral
P	proportional
pu	per unit
PWM	pulse width modulation
PRM	pulse ratio modulation
rms	root mean square
SW	switch
SMC	sliding mode control
VSS	variable system structure
kVA	kilo Volt Amperes
μF	micro Farad

LIST OF PRINCIPAL SYMBOLS

C_1	output filter capacitor
D_1, D_2	diodes
d, d'	switching function
D	average on-time of the top switch
D'	average off-time of the top switch
f_o	fundamental frequency of the output voltage
f_{sw}	switching frequency
$f_{sw,ave}$	average switching frequency
f_m	frequency of the triangular carrier
f_p	frequency of the triangular carrier in the predictive controller
G_v	voltage gain of the inverter
i_{C1}	capacitor current
i_{L1}, i_{L2}	inductor current
i_o	output current
$I_{o,ac,rms}$	rms value of output ac current
$I_{o,ac,peak}$	peak value of output ac current
i_{D1}, i_{D2}	diode current
i_{sw1}, i_{sw2}	switch current
$I_{pri,rms}$	rms value of current in the primary of transformer
$I_{sec,rms}$	rms value of current in the secondary of transformer
I_f	error signal
I_r	steady state ripple in the capacitor current
i_{ref}	reference current

$i_{C1,ref}$	reference current
k_{int}	integral gain of PI
k_{pro}	proportional gain of PI
k_{1i}	proportional gain of PI in the current loop
k_{1v}	proportional gain of PI in the voltage loop
k_{2i}	integral gain of PI in the current loop
k_{2v}	integral gain of PI in the current loop
L	inductance
L_1, L_2	filter inductors
n%	percentage of ripple in the capacitor current
P_o	output power
R, R_{Load}	load resistance
S_1, S_2	controlled switch
$S_{o,ac}$	output ac apparent power
t	time
t_{on}	on-time of the switch
t_{off}	off-time of the switch
T	switching period
V_o	output voltage
v_o	output voltage
$V_{o,ac,rms}$	rms value of the ac component of output voltage
$V_{o,ac,peak}$	peak value of the ac component of output voltage
$V_{o,p-p}$	peak to peak value of output voltage
V_{dc}	dc component of the output voltage
V_{in}	dc input voltage
v_{C1}	capacitor voltage
V_t	triangular carrier

V_m	peak value of the triangular carrier
$V_{D1,rev}$	reverse voltage across diode D_1
$V_{D2,rev}$	reverse voltage across diode D_2
$V_{sw1,rev}$	reverse voltage across switch S_1
$V_{sw2,rev}$	reverse voltage across switch S_2
v_{ph}	phase to neutral voltage
ω	angular frequency in radians per second (rad/s)
X_{C1}	capacitor impedance
X_L	inductor impedance
Z_{base}	base impedance
$\tau_{cur,loop}$	time constant of PI in the current loop
$\tau_{vol,loop}$	time constant of PI in the voltage loop

CHAPTER 1

INTRODUCTION

1.1 Power Processors

When a power electronic circuit is used to interface a dc system to an ac system, the circuit must perform two functions:

- inversion, and
- waveshaping.

Inversion is obtained by using the proper power circuit configuration and number of switching devices, while waveshaping is achieved by implementing an appropriate control technique. The problem of power conversion can therefore be divided into two main considerations:

(1) power circuit configurations,

(2) waveshaping techniques.

1.2 Power Circuit Configurations

The standard bridge topology used in dc to ac converters requires four switches, each capable of interrupting the entire load current (Fig. 1.1). This involves significant complexity in the control circuit and special care in gating the switches, particularly in the case of PWM operation, where several and simultaneous commutations of switches are required in each period. Other problems arise from interactions between the protection and/or commutation associated with the switches. From these points of view, significant benefits may result from the reduction of the number of switches, an approach which has been discussed in several papers [1], [2].

There are a number of power circuit topologies for dc/ac interfaces that use PWM techniques. Differences in these designs are due to topology choices and as well as system requirements. Among these are questions such as whether the power must flow in one or both directions and whether the ac and dc system have the characteristics of voltage or current source.

If only dc to ac power flow is required, the number of high frequency switches can be halved by using the topology shown in Fig. 1.2. In this topology, the waveshaping and inversion functions have been separated. As a result, four bridge switches, instead of two, are now needed. As it can be seen from Fig. 1.2, there is a possibility of shoot-through across the dc bus if the two switches on the same leg turn on.

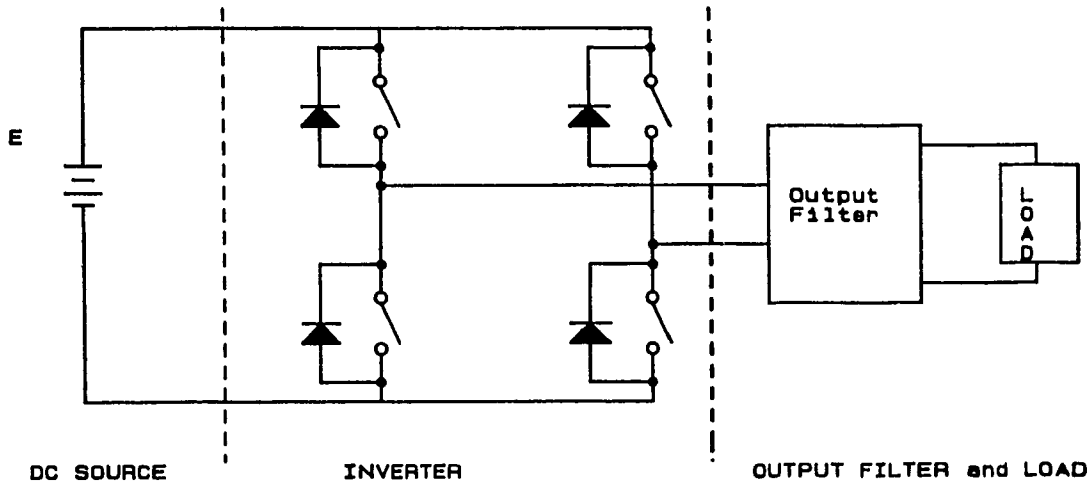

Fig. 1.1 Standard dc/ac converter

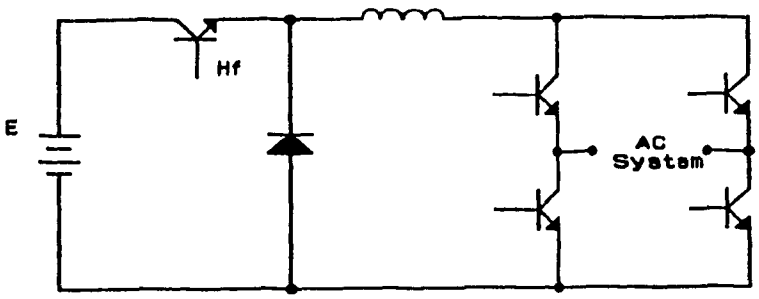

Fig. 1.2 Dc/ac converter with power flow from dc to ac.

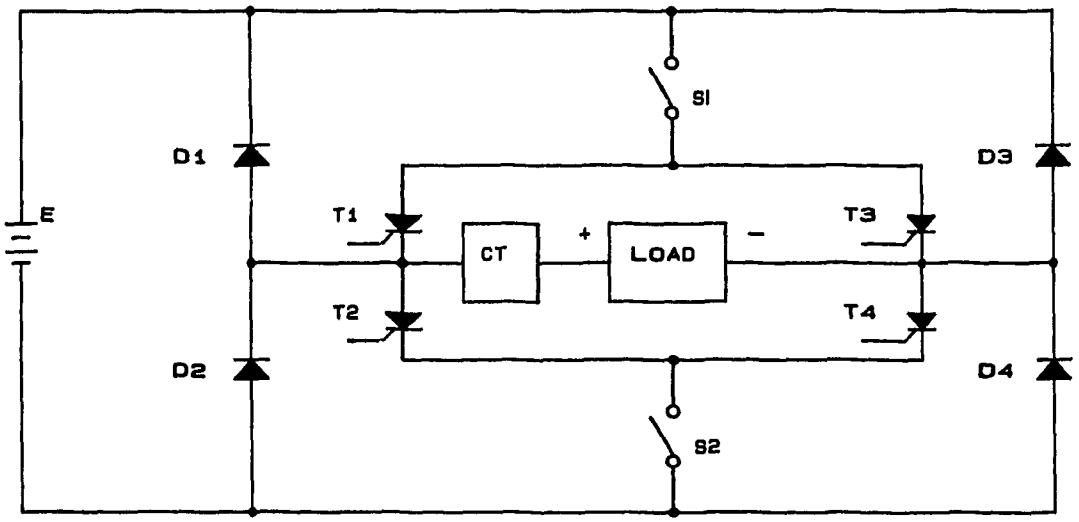

Fig. 1.3 Dc/ac converter with auxiliary switches.

A full bridge single-phase inverter scheme is proposed in [1] which employs two main switches and requires operation of only one of them at high frequency, while the other commutates twice in the period, to turn off the bridge thyristors and reverse the load voltage (Fig. 1.3). As S_1 must switch twice in the period, it must be rated for a moderate repetition frequency. On the contrary, S_2 must switch at the maximum operating frequency of the PWM and must be rated accordingly. Switch S_1 may be designed so as to ensure short circuit protection. It should be noted that there is a penalty associated with the advantages gained by reducing the number of high-frequency switches. In [1], for example extra bridge switches, are needed to determine the polarity of load voltage. Also the control algorithm is more complicated.

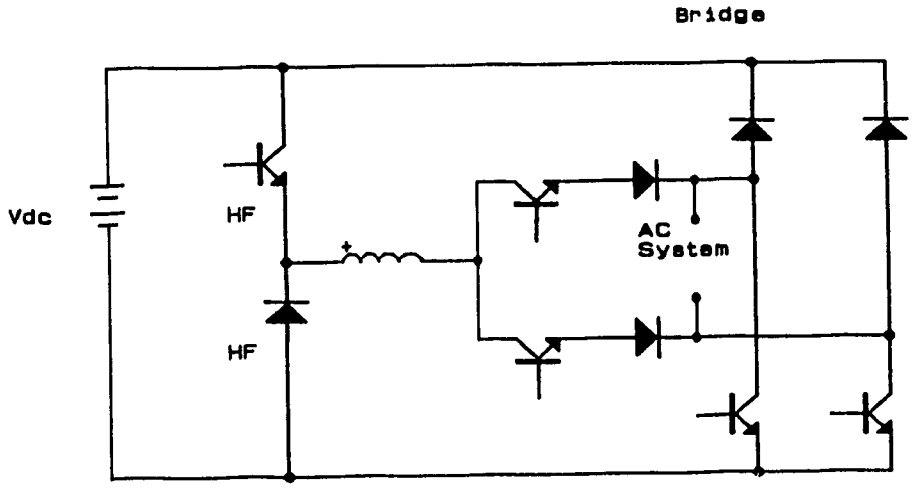

Fig. 1.4 Dc/ac converter with only one high frequency switch pair (labeled as HF).

A new converter topology for bipolar power flow is presented in [2]. In this topology only one high frequency switch pair is used but it has the disadvantage of having four bridge switches (these switches operate only twice in the period and there are always three of them in the conductive path), (Fig. 1.4). Also, a chance of shoot-through across the dc bus exists.

1.3 Waveshaping Techniques

In order to obtain the desired sinusoidal output voltage, waveshaping is usually required. While inversion is obtained by using an appropriate number of semiconductor devices, waveshaping is a more complex operation. Two basic approaches can be used separately or in conjunction:

- passive waveshaping techniques,
- active waveshaping techniques.

1.3.1 Passive waveshaping techniques

The output waveform of an inverter can be shaped by means of passive components such as capacitors and inductors. For high quality output waveforms these methods may require complicated passive filters. They generally need more energy storage capacity and hence larger reactive components than active methods [3]. These methods have the following advantages:

- They are easy to understand, therefore easy to design and service.
- They are typically more reliable than active waveshaping methods.

However, they have several disadvantages including the following:

- They are bulky and heavy.
- They provide a narrow range of operating points.
- Their cost is relatively high.

These disadvantages can be overcome by using active waveshaping methods.

1.3.2 Active waveshaping techniques

Active waveshaping is usually the preferred solution over the passive filtering approach. Several techniques have been implemented to obtain a high quality sinusoidal output waveform. These can be divided into forward Pulse Width Modulation (PWM) techniques and real time waveform feedback control techniques.

1.3.2.1 PWM techniques

Pulse Width Modulation (PWM) is an operation performed on "raw" voltage and current waveforms to shape their spectra so as to obtain the waveform required for the application under consideration. Waveform spectra shaping can be defined as the creation of a "dead band" between wanted and unwanted spectral components. Available PWM schemes can be classified as carrier modulated sine PWM and precalculated programmed PWM schemes. The Modulating Function (MF) methods are usually based on the principle of a comparison between a triangular carrier and a sinusoidal reference waveform reflecting the desired fundamental of the inverter output voltage. This concept can be traced back to the early sixties when the first PWM inverters were developed [4]. PWM allows static converters to generate close to ideal output waveforms while providing variable voltage and frequency. A considerable research effort has gone into improving the output waveforms and minimizing the disadvantages of PWM including generation of unwanted harmonics and reduced voltage gain [5]-[8]. The sinusoidal reference waveform has for example been replaced with trapezoidal, stepped or triangular waveforms. Optimal modulating functions have been investigated as well as an approach to maximize the inverter output voltage [9]. Linearity of the amplitude control characteristics, and simplicity of implementation have also been examined [9].

A critical evaluation of common carrier modulated PWM techniques on the basis of the application is provided in [10]. Techniques for harmonic elimination are studied in [11] and generalized methods are developed for eliminating a fixed number of harmonics in the half bridge and full bridge inverter output waveforms. Programmed PWM techniques have been investigated in [12] and distinct advantages in comparison to the conventional carrier modulated sine PWM schemes are brought out. Inverters utilizing forward PWM techniques have the following drawbacks:

- The output voltage can be significantly distorted by nonlinear loads (if a filter is used).
- The response time to sudden changes in input/output conditions can be slow, up to one cycle of the output waveform, since a feedback loop is required to regulate the output and modify the pattern.
- The phase displacement between the inverter output and the filter output varies with the load.

In the above mentioned methods, the shape of the output voltage is determined on an open-loop basis, while the closed-loop only acts on the amplitude or rms values of the output voltage/current. A different approach to the problem consists of controlling the output waveform by means of a closed-loop or feedback technique. To this end, the reference and the output waveforms are compared, and the resulting error signal, eventually frequency compensated, is used as the input of the modulator. In this case the modulation techniques are based on the comparison between the modulator input signal and a carrier waveform. The main disadvantage of this approach in some cases is the necessity of using an inverter supply voltage much higher than that used in the case of the open loop control, especially if the period of the carrier waveform is not much higher than the minimum

duration of the conduction intervals of the inverter. Therefore, to reduce the over-sizing required it is necessary to limit the maximum modulation frequency. By using a different method known as Pulse Ratio Modulation (PRM) [13], this limitation can be attenuated. In PRM technique both the duration and the frequency of the pulses given by the modulator vary, so the minimum duration of the conduction intervals is ensured. This technique has the obvious disadvantage of varying switching frequency. Also, the type of the load, and the output filter affect the performance of this technique.

1.3.2.2 Real Time Waveform Feedback Techniques

High performance converters rely on feedback control techniques in the form of active current and voltage waveshaping to overcome component and load non-linearities and to minimize response times to sudden changes in operating conditions. In practice many solutions for waveshaping the output voltage of dc/ac converters are known. An excellent description of different current control methods suitable for active waveshaping is presented in detail in [14]. The advantages of current-mode control methods over conventional PWM control techniques are then explained. These advantages can be summarized as follows:

- essentially no phase lag from control reference to filter inductor current;
- inherent pulse-by-pulse current limiting, making the power converter nearly immune to damage from overloads;
- ease of paralleling power stages, to provide increased output-current capability, with equal current-sharing among the paralleled stages;
- ease of applying output-current feed-forward, to obtain fast correction for load transients, minimizing the deviations of the output voltage;

- inherent insensitivity to static and dynamic variations of input voltage, for the buck and other forward-type converters.

The different types of current-mode controllers control the peak current, the valley current, or both (in the case of the hysteresis controller). All types of current-mode controllers usually command directly the current in a filter inductor of the power converter. Hence the inductor current follows instantaneously the control input. An alternate method of obtaining the information about the load voltage and the load current is using the output filter capacitor current. It is based on the idea that the load current (i_{load}) is equal to the inductor current (i_L) minus the capacitor current (i_c) as shown in Fig. 1.5. G. Schoneman and D. Mitchell have used this method in [15] to reduce the output impedance of switching regulators.

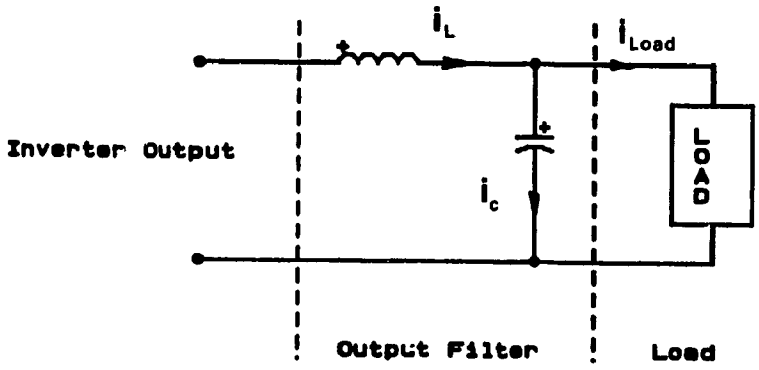

Fig. 1.5 Inverter output filter.

Disregarding the controlled variable, the current waveshaping techniques can be divided into four main categories which are explained below:

A. Hysteresis control.

B. Error triangulation technique.

C. Sliding mode control.

D. Predictive control.

A. Hysteresis control

The simplest and most straight forward technique is the hysteresis control. The control scheme for one inverter leg is shown in (Fig. 1.6). Here, when the line current becomes greater (less) than the current reference by the hysteresis band, the inverter leg is switched in the negative (positive) direction, which provides an instantaneous current limit if the neutral is connected to the dc bus midpoint. Therefore, the hysteresis band specifies the maximum current ripple assuming neither controller nor inverter delays. This technique has the obvious advantage of instantaneous current control which results in very fast response. Fig. 1.7 shows the hysteresis window and the shaped output waveform. The basic disadvantage with the hysteresis is the varying switching frequency. The switching frequency is also sensitive to circuit component values and design parameters. There are modified versions of the hysteresis technique with constant frequency operation [16]. A compensating waveform is needed to obtain stable operation for all duty ratios in the above versions.

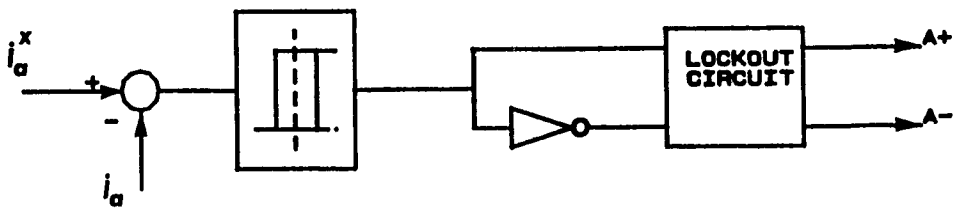

Fig. 1.6 Hysteresis controller.

Attempts to eliminate or reduce the inherent drawbacks with the hysteresis technique, result in added complexity of the control circuit, compromising the elegance and simplicity of the hysteresis technique [16], [17].

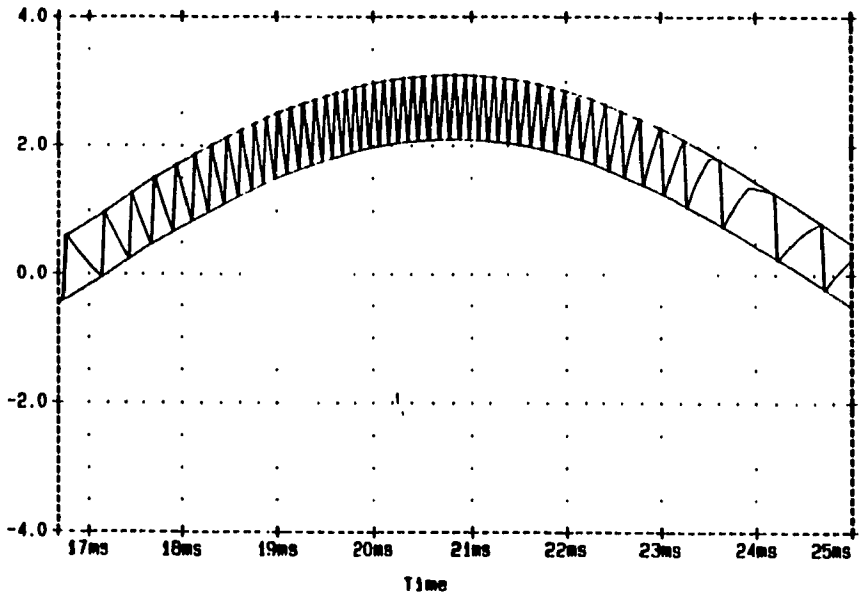

Fig. 1.7 Hysteresis window and the controlled current.

B. Ramp comparison control

A ramp comparison control for one inverter leg is shown in Fig. 1.8. The controller can be thought of as producing synchronous sine-triangle PWM with the current error considered to be the modulating function. The current error is compared to a triangular waveform and if the current error is greater (less) than the triangular waveform, the inverter leg is switched in the positive (negative) direction. The inverter switches at the frequency of the triangular waveform and produces well-defined harmonic frequencies [18]. This method yields a very good spectrum of the sinusoidal output voltage,

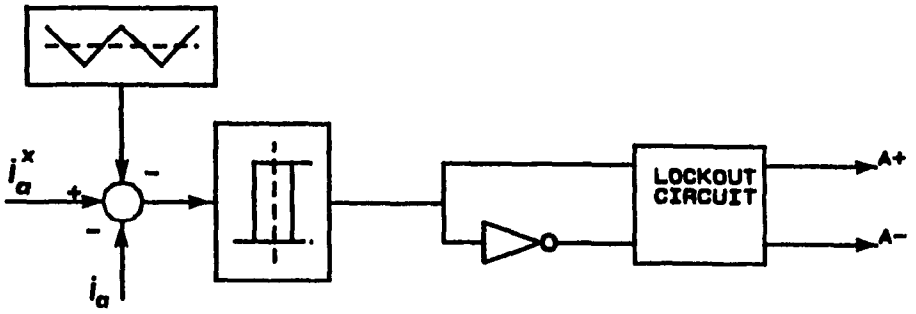

Fig. 1.8 Ramp controller.

since constant switching frequency is achieved. Multiple crossing of the ramp by the current error may become a problem when the slope of the current error becomes greater than that of the ramp.

C. Sliding mode control

The application of the theory of Variable Structure Systems (VSS) and Sliding Mode Control (SMC) to power converter has been recently explored. The control in the variable structure system represents the change of the system structure according to the predetermined rule described with control law u [19]. In the phase plane, the dynamics of the plant is described with a family of the phase trajectories, one for each substructure. The minimum number of the independent substructures represents the number of states of the control function u. The variable structure systems allow such selection of the substructures so that the unstable plant can be stabilized by means of the selected controller (this applies also to the systems with eigenvalues with positive real part). In [20] attempts have been made to outline a controller for the inverter so that the dynamics of the control

will not depend on the variable load. An application of a variable structure system theory, and the associated sliding mode, to a full bridge buck converter is presented in [21]. By using the pole assignment method, a sliding mode controller is designed and the Sliding Mode Control (SMC) and PWM techniques are compared. It should be noted that to generate the PWM pattern, sliding mode controller uses a comparator which operates based on ramp comparison technique principles.

D. Predictive control

Among current-mode control techniques, there are computational or predictive methods. The predictive controller with constant switching frequency calculates an inverter voltage vector, once every sample period, that will force the current to track the current command. The controller is shown in Fig. 1.9 and is described in [22],[23]. When the predictive controller is designed for a single phase system the calculation of the inverter voltage vector is not necessary.

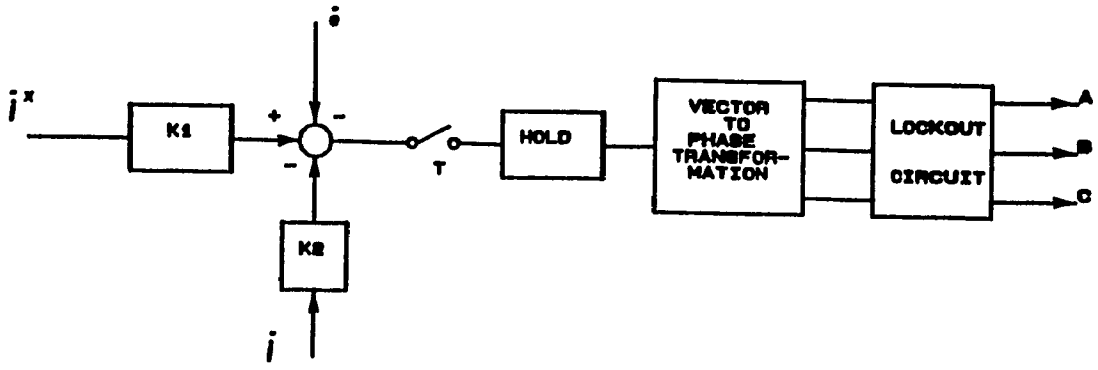

Fig. 1.9 Predictive controller.

The actual current lags the current reference by as much as one sample period. Longer lags probably will be realized due to calculation delays. The current ripple cannot be explicitly specified as with a hysteresis controller but the inverter switching frequency is constant. A predictive controller is presented in [24] and is implemented to control an ac to dc converter. Knowledge of the load and operating conditions can be used to minimize the inverter switching frequency. When the current error magnitude exceeds a specified value, the controller predicts the current trajectory for each possible inverter state and determines the length of the time that the current error will remain within the specified value. This type of controller is described in details in [25].

Some predictive control techniques use dead beat control theory to obtain a nearly sinusoidal output voltage. In [26]-[28] the microprocessor dead beat control is implemented with voltage and current sensors [26], and only with a voltage sensor [27],[28]. In these publications a finite computation time is required for determination of the pulse pattern. An improved version of inverter which uses a state estimator to synthesize three phase sinusoidal voltages of the PWM inverter is introduced in [29]. The main disadvantages of the predictive techniques are:

- The extent of the unknown load is a parameter in the control algorithm.
- Sensitivity to parameter variations.
- Complex implementation.

These features considerably reduce the robustness of the controller and consequently the robustness of the entire system.

1.4 Description of the proposed converter and Contributions

In order to achieve further improvements in terms of reliability, simplicity and the quality of the output waveforms, a new inverter configuration with an appropriate waveshaping scheme is proposed. The thesis contributes to both the power circuit configuration and waveshaping concept of the inverter.

1.4.1 Power circuit configuration

In order to achieve a more reliable inverter, the number of controlled elements could be reduced and shoot-through paths eliminated. Therefore, a new power circuit topology is proposed which uses only two main high frequency switches. By implementing one switch and one diode in each leg of the inverter, shoot-through paths are thus eliminated. This feature will result in significant benefits in terms of cost, weight and size of the converter and also in improved reliability.

1.4.2. Waveshaping technique

A high quality sinusoidal output voltage for nonlinear loads can be obtained by using an active waveshaping technique with constant switching frequency. Waveshaping involves two main aspects:

- The control parameter.
- The control technique.

1.4.2.1 The control parameter

The active waveshaping approach uses the output filter capacitor current to maintain the output voltage sinusoidal and of constant magnitude. The output voltage is therefore controlled indirectly by forcing a sinusoidal filter capacitor current. Current control provides a fast response to input/output transients. Moreover, even large ripple in the capacitor current only result in low ripple in the output voltage, since the voltage is the integral of the controlled capacitor current. This provides

almost ripple-free output voltage.

1.4.2.2 The control technique

The current regulation technique adopted combines constant switching frequency based on triangulation carrier comparison, and excellent response times in tracking variations in the current control reference waveform. By forcing sinusoidal capacitor voltage, the converter can supply loads that are of linear or non-linear type with a minimum of distortion in the output voltage waveform. Also, high output/input voltage gain can be obtained with this technique.

1.4.3 Three phase implementation

The proposed power module topology and control technique can be easily implemented in a three phase system. In this case, three single phase power modules are used and the current references are shifted by 120° degrees. Also, by injecting the third harmonic currents to the current references the voltage gain of the system is further increased.

1.5 Summary of the Thesis

The contents of the thesis have been organized as follows:

Chapter 2 presents the proposed circuit configuration and current control technique. The main power circuit and its advantages over the standard dc/ac bridge configurations are explained. Also, the general structure of the control scheme is presented. The analysis and design aspects of a single phase inverter are presented and component ratings are calculated.

Chapter 3 discusses the choices of current control techniques. First, the hysteresis controller is analyzed and its advantages and disadvantages are studied. Then, the proposed control technique which operates based on

error triangulation technique is analyzed and a design example is provided to indicate the correctness of the design procedure presented. Finally, a predictive controller is discussed and its advantages and drawbacks are brought out. Chapter 3 also includes a comparison among the studied current control techniques.

In chapter 4 the predicted results for the proposed inverter with three different current controllers are presented. The simulation results are used to exhibit the aforementioned drawbacks of each of the control techniques and confirm the advantages of the proposed control technique over the two other methods.

Experimental verification of the predicted results for the proposed current module is provided in chapter 5.

A three phase implementation of the proposed technique is discussed in chapter 6. High output/input voltage gain is achieved by injecting the third harmonic current in the reference waveforms. The change in the device ratings due to this injection are discussed and simulation results are presented.

Finally, chapter 7 contains a summary and conclusions of the thesis.

CHAPTER 2

PROPOSED CONFIGURATION AND CURRENT CONTROL TECHNIQUE

2.1 Introduction

In order to achieve further improvement in terms of reliability, simplicity and the quality of the output waveforms, a new power module topology and an associated control technique for a dc/ac converter are proposed. The novel features of this module include:

- a two switch topology with no shoot-through paths,
- providing high quality sinusoidal output voltage,
- capability of supplying nonlinear loads, and
- practically instantaneous recovery from input or output transients.

By utilizing an inner filter capacitor current control loop the proposed module can maintain nearly perfect sinusoidal output voltage even with highly non-linear loads. Using the capacitor current as the control parameter provides high quality output voltage due to the fact that the output voltage is the integral of the capacitor current.

In the following sections, the circuit configuration and the principles of operation of the control scheme are studied without considering the current control technique. Power circuit analysis and design are provided. The type of the current controller will be discussed in chapter three.

2.2 Circuit Description and Principles of Operation

The proposed converter power circuit, shown in Fig. 2.1, consists of the following components :

- Two high frequency switches S_1, S_2

- An output filter L_1, L_2, C_1
- Two free-wheeling diodes D_1, D_2
- The load which can be passive or active nonlinear type (Fig. 2.1).

As can be seen from Fig. 2.1, each leg of the inverter consists of one diode and one switch, so that dc bus short circuits can not occur.

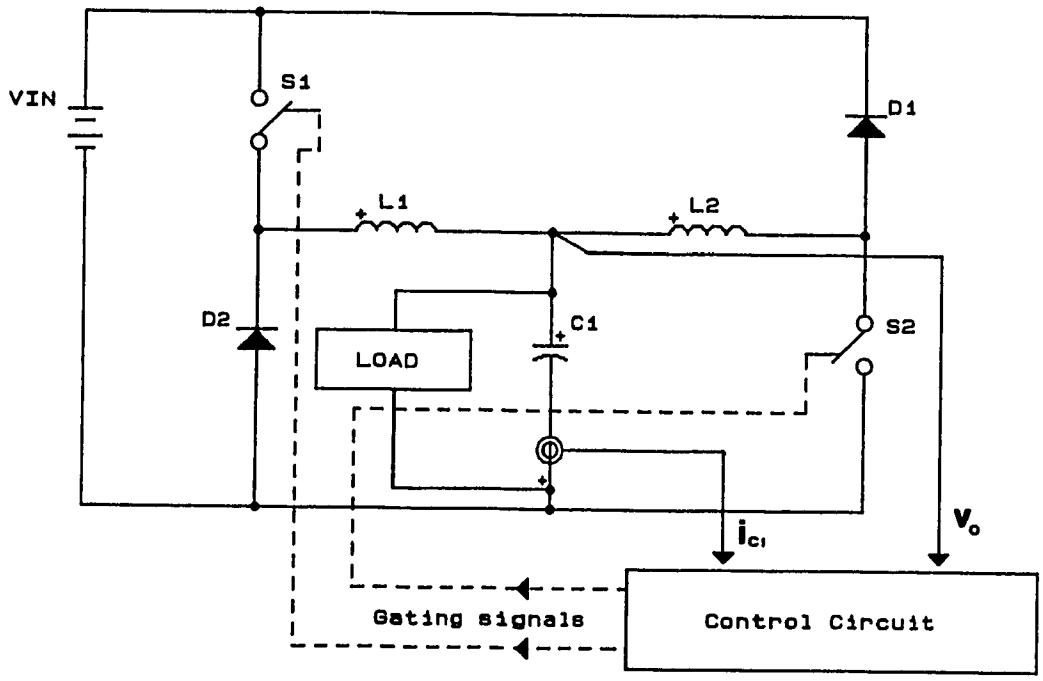

Fig. 2.1 Power circuit configuration and control technique

As Fig. 2.1 shows the current in the output filter capacitor i_{C1} is chosen as the control parameter. The control technique will provide the necessary PWM pattern to waveshape the output voltage indirectly by controlling the capacitor current. The capacitor current can be controlled by using different types of current controller which will be discussed in chapter three. However, the modes of operation can be explained independently of the control technique.

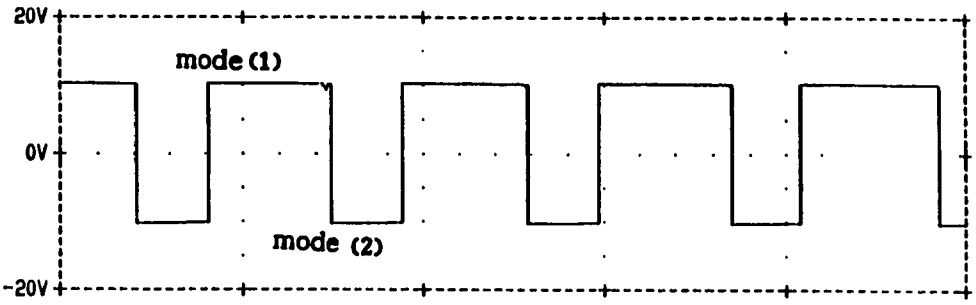

Fig. 2.2 Generated PWM pattern.

If the suitable PWM pattern is generated (Fig. 2.2), two modes of operation are recognized which are shown in Fig. 2.3(a,b).

mode (1) - S_1, D_1 are conducting.

- i_{C1} is increasing.

mode (2) - S_2, D_2 are conducting.

- i_{C1} is decreasing.

It is noted that in order to maintain the controllability of the system, a positive slope of the current must always be obtainable. From Fig. 2.3(a) it is obvious that the capacitor voltage (v_{C1}) must be always less than the dc bus voltage (V_{in}) since turning the top switch (S_1) on increases the capacitor current (i_{C1}). The maximum output voltage is then limited to

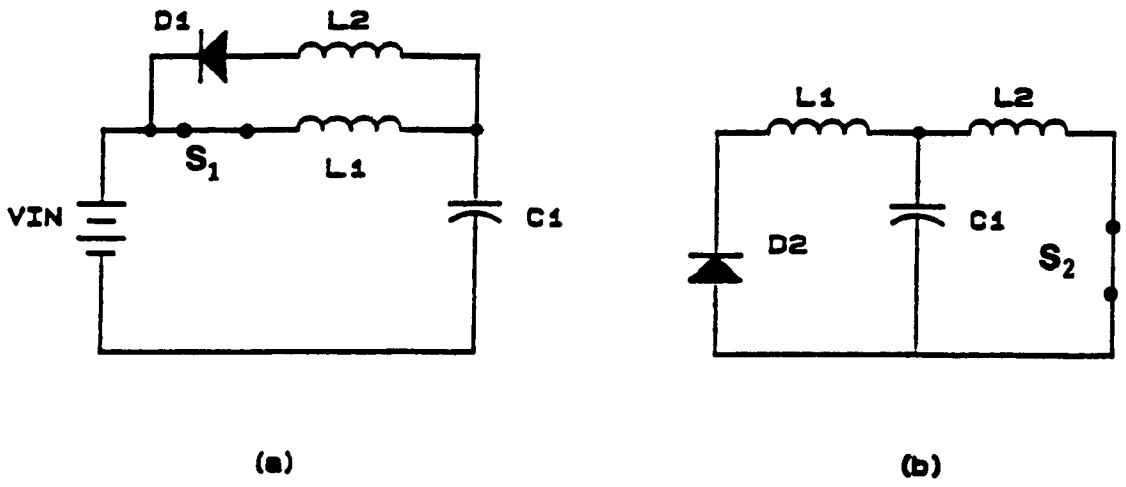

Fig. 2.3 Modes of operation.

a) The capacitor current is increasing.

b) The capacitor current is decreasing.

the dc bus voltage (V_{in}) and the maximum voltage gain of the system (G_v) can theoretically be equal to one.

2.3 Power Circuit Analysis and Design

The behavior of the inverter can be explained by analyzing the two modes of operation as shown in Fig. 2.3(a,b). For simplification, the load is assumed to be resistive (R). In mode (1), neglecting the forward voltage drop of the diode D_1, the following equations are obtained:

$$L_1 \frac{di_{L1}}{dt} + L_2 \frac{di_{L2}}{dt} = 0 \tag{2.1}$$

$$V_{in} = L_1 \frac{di_{L1}}{dt} + v_{C1}(t) \tag{2.2}$$

$$i_{L1}(t) = i_{L2}(t) + i_{C1}(t) + \frac{v_{C1}(t)}{R} \tag{2.3}$$

Substituting the capacitor voltage into the eq. 2.3 yields:

$$i_{L1}(t) - i_{L2}(t) = C_1 \frac{dv_{C1}}{dt} + \frac{v_{C1}(t)}{R} \qquad (2.4)$$

Taking the derivative of the Eqn. (2.4) and substituting di_{L2}/dt from Eqn. (2.1) results in:

$$\left(1 + \frac{L_1}{L_2}\right) \frac{di_{L1}}{dt} = C_1 \frac{dv_{C1}^2}{dt^2} + \frac{1}{R} \frac{dv_{C1}}{dt} \qquad (2.5)$$

Eqn. (2.5) can be solved for di_{L1}/dt and finally the change in the capacitor voltage in mode (1) will be described by the following equation:

$$V_{in} = \frac{L_1 L_2 C_1}{L_1 + L_2} \frac{d^2 v_{C1}}{dt^2} + \frac{L_1 L_2}{R(L_1 + L_2)} \frac{dv_{C1}}{dt} + v_{C1}(t) \qquad (2.6)$$

By using the same procedure, operation in mode (2) is described by:

$$0 = \frac{L_2 L_2 C_1}{L_1 + L_2} \frac{d^2 v_{C1}}{dt^2} + \frac{L_1 L_2}{R(L_1 + L_2)} \frac{dv_{C1}}{dt} + v_{C1}(t) \qquad (2.7)$$

In mode (1) when S_1 is on and S_2 is off, the switching function (d) is defined to be:

$$d = \begin{cases} 1 & \text{when } S_1 \text{ is on} \\ 0 & \text{when } S_1 \text{ is off} \end{cases}$$

The on-time of the bottom switch S_2 is defined as d'.

$$d' = \begin{cases} 1 & \text{when } S_2 \text{ is on} \\ 0 & \text{when } S_2 \text{ is off} \end{cases}$$

Since the two switches operate complimentarily:

$$d + d' = 1$$

In the frequency range of much lower than the switching frequency, the switching function "d" can be replaced by its average value (D) and the

system behavior can be represented by the following equation:

$$DV_{in} = \frac{L_1 L_2 C_1}{L_1 + L_2} \frac{d^2 v_{C1}}{dt^2} + \frac{L_1 L_2}{R(L_1 + L_2)} \frac{dv_{C1}}{dt} + v_{C1}(t) \qquad (2.8)$$

It would be useful to find the average on-time of the top switch (S_1) as:

$$D = \frac{AC_1 \frac{d^2 v_{C1}}{dt^2} + \frac{A}{R} \frac{dv_{C1}}{dt} + v_{C1}(t)}{V_{in}} \qquad (2.9)$$

where $$A = \frac{L_1 L_2}{L_1 + L_2}$$

It is useful to derive another equation for the average off-time of the switch S_1. Since:

$$D' = 1 - D$$

then:

$$D' = \frac{V_{in} - (AC_1 \frac{d^2 v_{C1}}{dt^2} + \frac{A}{R} \frac{dv_{C1}}{dt} + v_{C1}(t))}{V_{in}} \qquad (2.10)$$

The current reference is calculated by using the desired output voltage. Neglecting the voltage drop across the filter inductor, the maximum peak to peak value of the output voltage is:

$$V_{o,p-p} = V_{in}$$

The magnitude of the reference current can be calculated as:

$$I_p = \frac{V_{in}}{2 X_{C1}}$$

$$= \frac{V_{in} \omega C_1}{2} \qquad (2.11)$$

and $$\omega = 2\pi f_o$$

where f_o is the fundamental frequency of the output voltage and X_{C1} is the capacitor impedance.

The dc offset of the output voltage is:

$$V_{dc} = \frac{V_{in}}{2} \tag{2.12}$$

If the converter module is to be used for ac loads, this dc offset should be eliminated by using a transformer in the output of the inverter.

2.4 Component Ratings

For a resistive load (R), assuming the rated values for the output of the inverter, the capacitor current (i_{C1}) will be equal to the capacitor reference current, provided that the capacitor current ripple is neglected:

$$i_{C1}(t) = i_{ref}(t) = I_p \sin \omega t \tag{2.13}$$

$$v_{C1}(t) = \frac{1}{C_1} \int i_{C1}\, dt + v(0)$$

$$v_{C1}(t) = -\frac{I_p}{C_1 \omega} \cos \omega t + v(0) \tag{2.14}$$

at $t = 0$, $v_{C1} = 0$

$$0 = -\frac{I_p}{C_1 \omega} + v(0) \Rightarrow v(0) = \frac{I_p}{C_1 \omega}$$

$$v_{C1}(t) = -\frac{I_p}{C_1 \omega} \cos \omega t + \frac{I_p}{C_1 \omega} \tag{2.15}$$

The capacitor reference current is designed to obtain the maximum rated output voltage. Substituting I_p from Eqn. (2.11) into Eqn. (2.13), yields:

$$i_{C1}(t) = \frac{V_{in} C_1 \omega}{2} \sin \omega t \qquad (2.16)$$

And also the output voltage and the load current will be:

$$v_o(t) = v_{C1}(t) = - \frac{V_{in}}{2} \cos \omega t + \frac{V_{in}}{2} \qquad (2.17)$$

$$i_o(t) = - \frac{V_{in}}{2R} \cos \omega t + \frac{V_{in}}{2R} \qquad (2.18)$$

from Eqn. (2.3):

$$i_{L1}(t) - i_{L2}(t) = \frac{- V_{in}}{2R} \cos \omega t + \frac{V_{in}}{2R} + \frac{V_{in} C_1 \omega}{2} \sin \omega t \qquad (2.19)$$

If $L_1 = L_2$, from Eqn. (2.1) we have:

$$\frac{di_{L1}}{dt} = - \frac{di_{L2}}{dt} \qquad (2.20)$$

Integration of the above equation results in:

$$i_{L1}(t) + i_{L2}(t) = B \qquad (2.21)$$

Where B is the constant of the integration and can be calculated by substituting the initial values of the inductor currents:

since at $t = 0$: $\quad i_{L1}(0) = i_{L2}(0) = \frac{V_{in}}{2R}$

then:

$$B = \frac{V_{in}}{R}$$

Substituting the value of B in Eqn. (2.21) yields:

$$i_{L1}(t) + i_{L2}(t) = \frac{V_{in}}{R} \qquad (2.22)$$

Using Eqns. (2.19), (2.22) and solving for the inductor currents

yields:

$$i_{L1}(t) = \frac{-V_{in}}{4R} \cos \omega t + \frac{V_{in} C_1 \omega}{4} \sin \omega t + \frac{3V_{in}}{4R} \qquad (2.23)$$

$$i_{L2}(t) = \frac{V_{in}}{4R} \cos \omega t - \frac{V_{in} C_1 \omega}{4} \sin \omega t + \frac{V_{in}}{4R} \qquad (2.24)$$

The inductor currents (i_{L1}, i_{L2}), the capacitor current (i_{C1}), and the load current (i_o) are shown in Fig. 2.4.

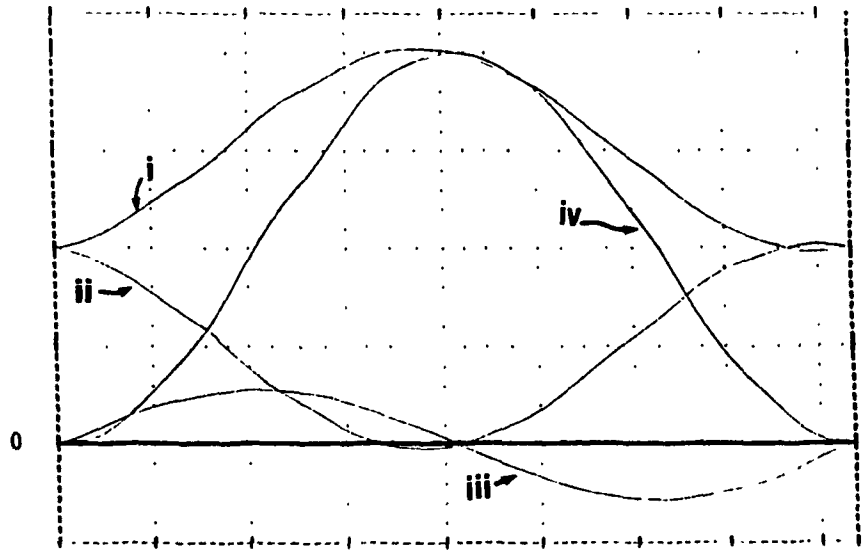

Fig. 2.4 The component currents.

(i) Inductor current i_{L1}.

(ii) Inductor current i_{L2}.

(iii) Capacitor current i_{C1}.

(iv) Load current i_o.

The rating of the inverter components will be found in per unit of the rated values:

$$\text{Base VA} = S_{rated} = S_{o,ac}$$

Base V = $V_{o,ac,rms}$

Base current can be calculated from the above equations:

$$\text{Base A} = \frac{S_{o,ac}}{V_{o,ac,rms}} = I_{o,ac,rms}$$

Assuming 1 pu ac current in the load, the load resistance must be:

$$\text{Base R} = \frac{V_{o,ac,rms}}{I_{o,ac,rms}}$$

The peak of the ac load current is:

$$i_{o,ac,peak} = 1.414 \text{ pu}$$

The peak of the ac load voltage is:

$$V_{o,ac,peak} = 1.414 \text{ pu}$$

Since tne output ac voltage is assumed to be 1 pu, the input dc voltage is:

$$V_{in} = V_{o,p-p} = 2 \times 1.414 = 2.828 \text{ pu}$$

The average on-time of the switch S_1 is defined as D in equation (2.9). Assuming $L_1 = L_2 = L$, and substituting the steady state value of v_{C1} from Eqn. (2.15) into Eqn. (2.9) yields:

$$D = \frac{L\omega}{4R} \sin \omega t + \left(\frac{LC_1\omega^2}{4} - \frac{1}{2}\right) \cos \omega t + \frac{1}{2} \qquad (2.25)$$

The currents passing through the diodes (i_{D1}, i_{D2}) and the switches (i_{sw1}, i_{sw2}) have the following relations with the inductor currents (i_{L1}, i_{L2}):

$$i_{D1} = \begin{cases} iL_2 & \text{when } D = 1,\ D' = 0 \\ 0 & \text{when } D = 0,\ D' = 1 \end{cases}$$

$$i_{D2} = \begin{cases} iL_1 & \text{when } D = 0,\ D' = 1 \\ 0 & \text{when } D = 1,\ D' = 0 \end{cases} \qquad (2.26)$$

$$i_{sw1} = \begin{cases} iL_1 & \text{when } D = 1,\ D' = 0 \\ 0 & \text{when } D = 0,\ D' = 1 \end{cases}$$

$$i_{sw2} = \begin{cases} iL_2 & \text{when } D = 0,\ D' = 1 \\ 0 & \text{when } D = 1,\ D' = 0 \end{cases} \qquad (2.27)$$

Based on the above relations, the average and rms values of the diodes and switches currents can be calculated.

2.4.1 Capacitor ratings

The capacitor current is given by Eqn. (2.16). The peak and the rms value of the capacitor current are calculated. The value of the capacitor will be calculated in the next chapter, but for now it is assumed to be:

$$X_{C1} = 3.54 \text{ pu.}$$

$$i_{C1,peak} = \frac{V_{o,ac,peak}}{X_{C1}} = 0.4 \text{ pu}$$

$$i_{C1,rms} = 0.707 \times 0.4 = 0.283 \text{ pu}$$

$$v_{C1,peak} = V_{in} = 2.828 \text{ pu}$$

$$v_{C1,rms} = 1.732 \text{ pu}$$

2.4.2 Inductor ratings

The inductor peak current is calculated using Eqns. (2.23) and (2.24). For the inductor L_1 substituting the per unit values of the input voltage and the capacitor current yields:

$$i_{L1,peak} = \sqrt{\left(\frac{1.414}{2}\right)^2 + \left(\frac{2.828 \times 0.283}{4}\right)^2} + \frac{3 \times 2.828}{4}$$

$$= 2.856 \text{ pu}$$

The inductor (L_1) rms current is:

$$i_{L1,rms} = \sqrt{\frac{1}{T}\int_0^t i_{L1}^2\, dt} = 2.184 \text{ pu}$$

Also:

$$V_{L1,peak} = V_{in} = 2.828 \text{ pu}$$

Following a similar procedure the following results are obtained for inductor L_2:

$$i_{L2,peak} = 1.442 \text{ pu}$$

$$i_{L2,rms} = \sqrt{\frac{1}{T}\int_0^t i_{L2}^2\, dt} = 0.878 \text{ pu}$$

$$V_{L2,peak} = V_{in} = 2.828 \text{ pu}$$

2.4.3 Diode ratings

The peak current in the diode D_1 is as high as the inductor (L_2) peak current:

$$i_{D1,peak} = i_{L2,peak} = 1.442 \text{ pu}$$

Also the peak current in D_2 is:

$$i_{D2,peak} = i_{L1,peak} = 2.856 \text{ pu}$$

The average and rms values of (i_{D1} ,i_{D2}) are found using Eqns. (2.26), (2.27):

$$i_{D1,ave} = \frac{1}{T}\int_0^T D\, i_{L2}\, dt$$

$$i_{D1,rms} = \sqrt{\frac{1}{T}\int_0^T (D\, i_{L2})^2\, dt} \qquad (2.28)$$

$$i_{D2,ave} = \frac{1}{T}\int_0^T D' iL_1 dt$$

$$i_{D2,rms} = \sqrt{\frac{1}{T}\int_0^T (D' i_{L1})^2 dt} \qquad (2.29)$$

Using the above equations the ratings of the diodes (D_1, D_2) are calculated as:

$$i_{D1,ave} = 0.177 \text{ pu}$$

$$i_{D1,rms} = 0.219 \text{ pu}$$

$$i_{D2,ave} = 0.884 \text{ pu}$$

$$i_{D2,rms} = 1.006 \text{ pu}$$

The maximum reverse voltage across the diodes D_1 and D_2 will be:

$$V_{D1,rev} = V_{in} = 2 \times 1.414 = 2.828 \text{ pu}$$

$$V_{D2,rev} = V_{in} = 2 \times 1.414 = 2.828 \text{ pu}$$

2.4.4 Switch ratings

Switch ratings are found by following the same procedure as diodes. Switch S_1 experiences the same peak current as diode D_2 while switch S_2 experiences the peak current of diode D_1.

$$i_{sw1,peak} = i_{D2,peak} = 2.856 \text{ pu}$$

$$i_{sw2,peak} = i_{D2,peak} = 1.442 \text{ pu}$$

$$i_{sw1,ave} = \frac{1}{T}\int_0^T D\, i_{L1}\, dt$$

$$i_{sw1,rms} = \sqrt{\frac{1}{T}\int_0^T (D\, i_{L1})^2 dt}$$

$$i_{sw2,ave} = \frac{1}{T}\int_0^T D' i_{L2}\, dt$$

$$i_{sw2,rms} = \sqrt{\frac{1}{T}\int_0^T (D' i_{L2})^2\, dt}$$

Substituting the equations for i_{L1}, D, i_{L2}, D', the average and the rms values for both switches are found:

$$i_{sw1,ave} = 1.237 \text{ pu}$$

$$i_{sw1,rms} = 1.585 \text{ pu}$$

$$i_{sw2,ave} = 0.53 \text{ pu}$$

$$i_{sw2,rms} = 0.739 \text{ pu}$$

The maximum reverse voltage across the switches will be:

$$V_{sw1,rev} = V_{in} = 2 \times 1.414 = 2.828 \text{ pu}$$

$$V_{sw2,rev} = V_{in} = 2 \times 1.414 = 2.828 \text{ pu}$$

2.4.5 Transformer design

In order to eliminate the dc offset in the output voltage, use of a 1:1 transformer becomes necessary. The current and voltage rating of this transformer differ from primary to secondary because the primary winding must carry the dc current. In order to avoid saturation of the transformer, the power rating of the primary winding should be higher than the secondary winding.

$$i_{sec,rms} = 1 \text{ pu}$$

$$i_{pri,rms} = 1.731 \text{ pu}$$

$$v_{sec,rms} = 1 \text{ pu}$$

$$v_{pri,rms} = 1.731 \text{ pu}$$

2.5 Conclusions

A novel two-switch dc to ac converter module with no shoot-through paths has been proposed. The general structure of the control scheme has been described. Also, power circuit configuration has been analyzed and component ratings calculated. The output filter capacitor current is selected as the control parameter to provide indirect control over the output voltage. The advantages of this converter module can be summarized as:

- High reliability, since the number of high frequency switches are reduced and shoot-through paths are eliminated.

- High quality output voltage, since high ripple in the capacitor current will only result in very low ripple in the output voltage.

Different current control techniques can be used to achieve sinusoidal output voltage. These techniques will be studied in the following chapter.

CHAPTER 3

IMPLEMENTATION OF THE PROPOSED CONTROL SCHEME

3.1 Introduction

The structure of the control scheme has been described in the previous chapter. The capacitor current has been selected as the control parameter to provide a high quality output voltage, but the current control technique has not been specified.

The error triangulation technique is chosen to provide the proper output waveshaping. In order to justify this selection and to provide an adequate view over different types of current controllers, three different types of current control techniques are studied and evaluated in this chapter. For the proposed converter module, these controllers are implemented and the complete system is analyzed. First by investigating the bang-bang hysteresis, a well known current control method, a base of comparison is provided. Then the error triangulation technique is studied in more details and a design example is presented. Finally, a more complicated technique, the predictive control is discussed. The advantages and drawbacks of the three control techniques are brought out and compared.

3.2 Bang-Bang Hysteresis (BBH) Technique

The bang-bang hysteresis technique is a very widely used current control method. It provides a very tight current regulation using a simple control circuit. This method is simple and rugged but it has the well known drawback of variable switching frequency f_{sw} within a cycle of the output

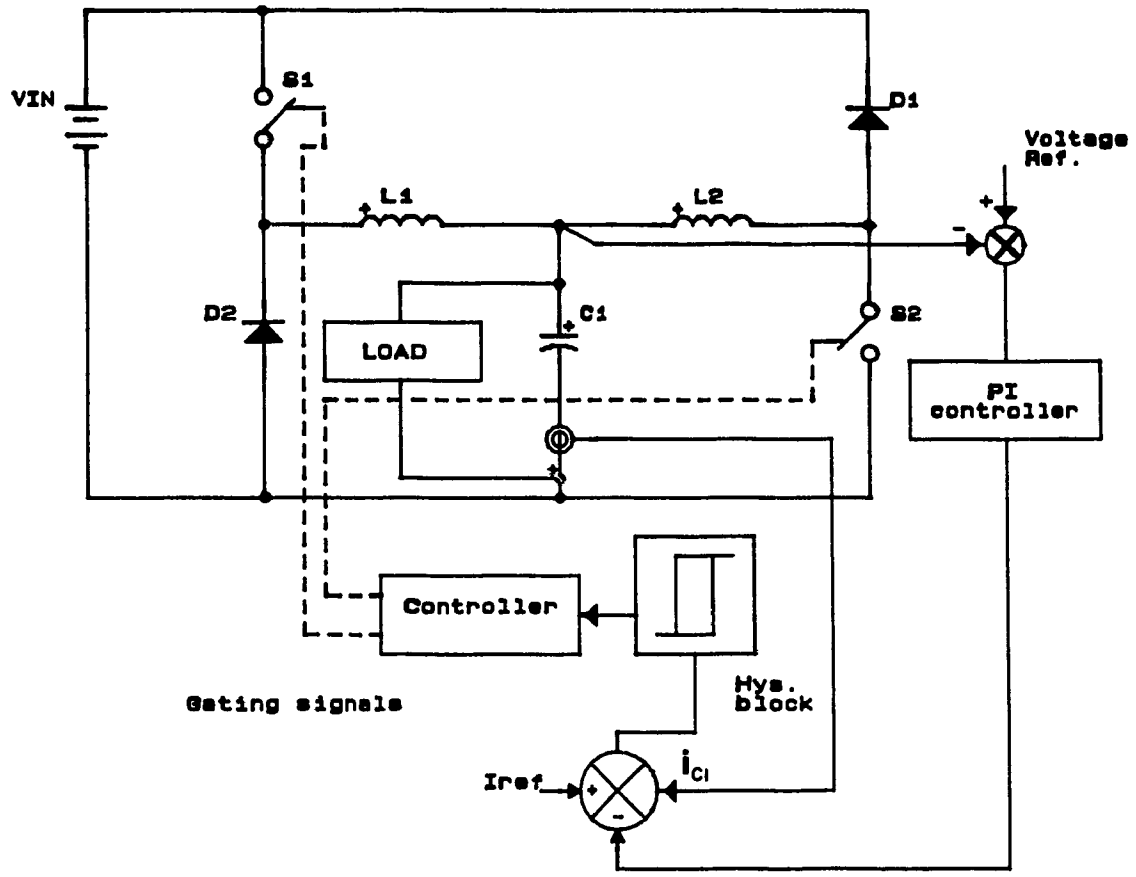

Fig. 3.1 The proposed inverter with hysteresis control.

voltage and as the reference amplitude (I_p) changes.

3.2.1 Principles of operation

The control scheme is shown in Fig. 3.1 and Fig. 3.2 shows the principles of operation. The controlled current always remains within a window, whose size is a design parameter and fixes the maximum ripple of current. Every time the actual current hits one of the top or bottom boundaries, the inverter changes its mode of operation. Since the maximum current ripple is fixed, the on time and the off time for the top and the bottom switches can be calculated [30]. When the top switch is on, the capacitor current increases till the error signal I_f reaches $\Delta I/2$. At this time , the top switch turns off and the bottom switch turns on till the error signal reaches $-\Delta I/2$.

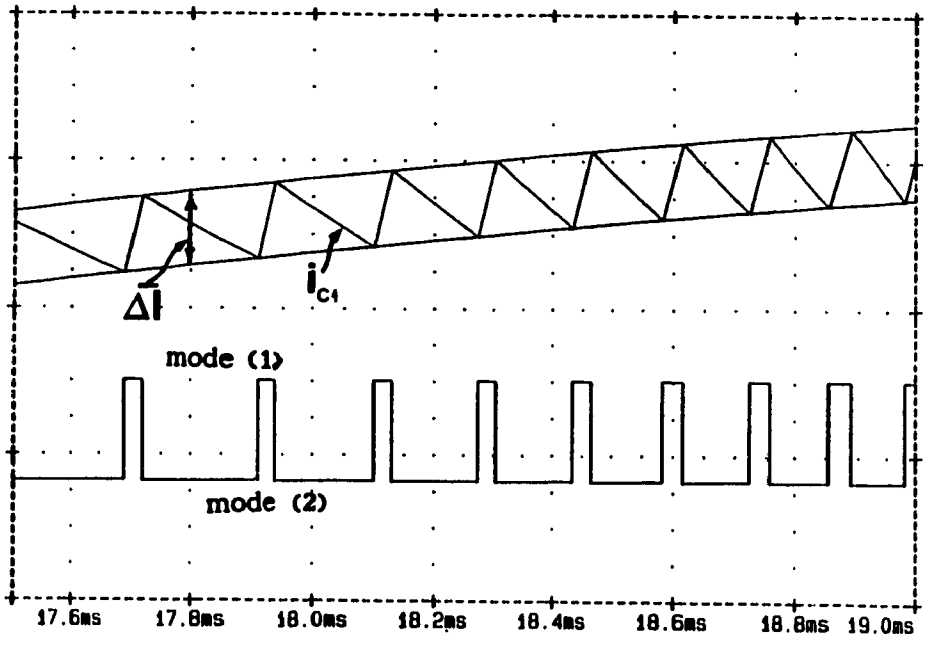

Fig. 3.2 Principles of operation of hysteresis control.

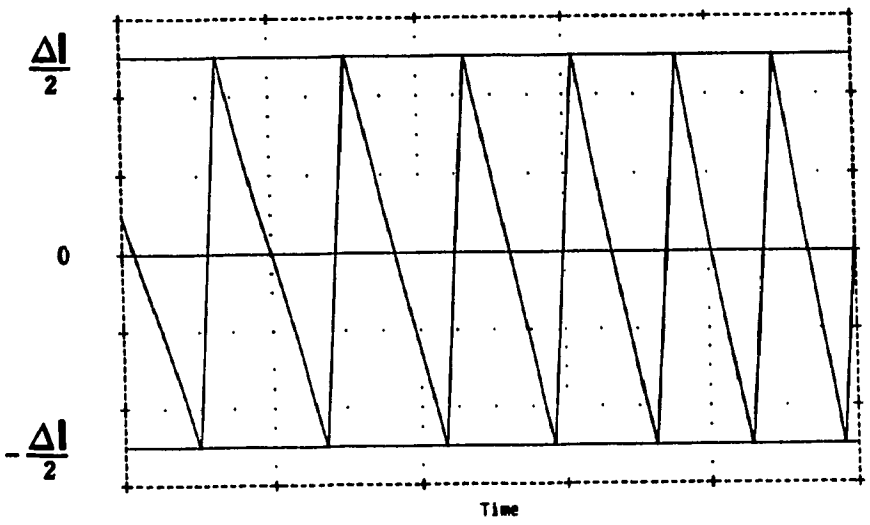

Fig. 3.3 The error signal in hysteresis control.

3.2.2 Analysis

The average switching frequency can be found by calculating the on-time and the off-time of the top switch (S_1). Again for the sake of simplification the noload condition is being considered. If the load is disconnected, from Eqn. (2.3):

$$i_{C1}(t) = i_{L1}(t) - i_{L2}(t) \tag{3.1}$$

Taking the derivative of the above equation yields:

$$\frac{di_{C1}}{dt} = \frac{di_{L1}}{dt} - \frac{di_{L2}}{dt} \tag{3.2}$$

Using Eqn. (2.1) and assuming $L_1 = L_2 = L$, results in:

$$\frac{di_{L1}}{dt} = \frac{-di_{L2}}{dt} \tag{3.3}$$

also Eqn. (2.2) can be rewritten as:

$$\frac{di_{L1}}{dt} = \frac{V_{in} - v_{C1}(t)}{L} \tag{3.4}$$

Using Eqns. (3.2)-(3.4), the slope of the capacitor current can be found:

$$\frac{di_{C1}}{dt} = \frac{2(V_{in} - v_{C1}(t))}{L} \tag{3.5}$$

In order to simplify the equations, it is assumed that the inverter provides the rated output voltage, i.e.:

$$I_P = \frac{V_{in}\,\omega\,C_1}{2}$$

where I_P is the amplitude of the current reference. By substituting the steady state value of the rated output voltage from Eqn. (2.15), the slope of the capacitor current during the on-time of S_1 is obtained:

$$\frac{di_{C1}}{dt}_{on} = \frac{V_{in}}{L}(1 + \cos \omega t) \tag{3.6}$$

The average slope of the capacitor current during the on-time is:

$$\frac{di_{C1}}{dt}_{on,ave} = \frac{1}{(t_1 - t)} \int_{t_1}^{t} \frac{V_{in}}{L}(1 + \cos \omega t)\, dt$$

$$= \frac{V_{in}}{L}\left[1 + \frac{1}{\omega(t - t_1)}(\sin \omega t - \sin \omega t_1)\right] \tag{3.7}$$

The capacitor current can be expressed as:

$$i_{C1}(t) = i_{C1}(t_1) + (t - t_1)\frac{di_{C1}}{dt}_{on,ave}$$

Substituting from Eqn. (3.7):

$$i_{C1}(t) = i_{C1}(t_1) + \frac{V_{in}}{L}(t - t_1) + \frac{V_{in}}{\omega L}(\sin \omega t - \sin \omega t_1) \tag{3.8}$$

The on-time of the top switch t_{on} can be derived from Eqn. (3.8) by putting $t = t_2$ and substituting $i_{C1}(t_1)$ and $i_{C1}(t_2)$ by their value at these times i.e., $I_p \sin \omega t - \frac{\Delta I}{2}$ and $I_p \sin \omega t + \frac{\Delta I}{2}$, respectively.

$$I_p \sin \omega t_2 + \frac{\Delta I}{2} = I_p \sin \omega t_1 - \frac{\Delta I}{2} + \frac{V_{in}}{L}(t_2 - t_1) + \frac{V_{in}}{\omega L}(\sin \omega t_2 - \sin \omega t_1) \tag{3.9}$$

This equation can be changed to:

$$\Delta I = 2(-I_p + \frac{V_{in}}{\omega L}) \cos \frac{\omega(t_1 + t_2)}{2} \sin \frac{\omega(t_1 - t_2)}{2} + \frac{V_{in}}{L}(t_2 - t_1) \tag{3.10}$$

Remembering that the value of t_{on} is very small, the sine term in Eqn. (3.10) can be replaced by the value of its angle in radians. Replacing $\frac{t_1 + t_2}{2}$ by t, and $t_2 - t_1$ by t_{on} and solving for t_{on} will result in:

$$t_{on} = \frac{L \Delta I}{(\omega L I_p - V_{in}) \cos \omega t + V_{in}} \tag{3.11}$$

Same procedure can be followed to obtain the off-time of the top switch t_{off}. Using Fig. 2.3(b), when the top switch (S_1) is off:

$$L \frac{di_{L2}}{dt} = v_{C1}(t) \tag{3.12}$$

Eqn. (3.12) can be changed to:

$$\frac{di_{L2}}{dt} = \frac{v_o(t)}{L} \tag{3.13}$$

The slope of the capacitor during the off-time of the top switch (S_1) is obtained from Eqns. (3.2), (3.3) and (3.13):

$$\frac{di_{C1}}{dt}_{off} = - \frac{2\, di_{L2}}{dt} = - \frac{2\, v_o(t)}{L} \tag{3.14}$$

Using Eqn. (2.17):

$$\frac{di_{C1}}{dt}_{off} = \frac{V_{in}\cos\,\omega t - V_{in}}{L} \tag{3.15}$$

The average slope of the capacitor current during the off-time is found to be:

$$\frac{di_{C1}}{dt}_{off,ave} = \frac{1}{(t_2 - t)} \int_{t_2}^{t} \frac{(V_{in}\cos\,\omega t - V_{in})}{L}\, dt$$

$$= \frac{V_{in}}{L} \left[\frac{1}{\omega(t - t_2)} (\sin\,\omega t - \sin\,\omega t_2) - 1\right] \tag{3.16}$$

The capacitor current is expressed as follows:

$$i_{C1}(t) = i_{C1}(t_2) + (t - t_2) \frac{di_{C1}}{dt}_{off,ave}$$

$$i_{C1}(t) = i_{C1}(t_2) - \frac{V_{in}}{L} (t - t_2) + \frac{V_{in}}{\omega L} (\sin\,\omega t - \sin\,\omega t_2) \tag{3.17}$$

Taking $t=t_3$ and substituting $i_{c1}(t_3)$ and $i_{C1}(t_2)$ by their equivalents, i.e., $I_p \sin\,\omega t - \frac{\Delta I}{2}$ and $I_p \sin\,\omega t + \frac{\Delta I}{2}$, respectively.

$$I_p \sin\,\omega t_3 - \frac{\Delta I}{2} = I_p \sin\,\omega t_2 + \frac{\Delta I}{2} - \frac{V_{in}}{L} (t_3 - t_2)$$

$$+ \frac{V_{in}}{\omega L} (\sin\,\omega t_3 - \sin\,\omega t_2) \tag{3.18}$$

Replacing $\frac{t_3 + t_2}{2}$ by t, and $t_3 - t_2$ by t_{off} and solving for t_{off} will

result in:

$$t_{off} = \frac{L\,\Delta I}{(-\omega L I_p + V_{in})\cos\,\omega t + V_{in}} \qquad (3.19)$$

Using Eqns. (3.11), (3.19) the switching frequency can be found as a function of time:

$$T_{sw} = t_{on} + t_{off}$$

$$f_{sw} = \frac{1}{T_{sw}}$$

Therefore,

$$f_{sw} = \frac{(V_{in})^2 - (L\omega I_p - V_{in})^2 \cos^2\omega t}{2\,LV_{in}\,\Delta I}$$

$$= \frac{V_{in}}{2L\,\Delta I}\left(1 - \left(\frac{L\,\omega^2\,C_1}{2} - 1\right)^2 \cos^2\omega t\right) \qquad (3.20)$$

Eqn. (3.20) shows that switching frequency is dependent of inductor (L) and capacitor (C_1) value, input voltage (V_{in}) and the hysteresis window (ΔI). The variations of switching frequency as a function of time is shown in Fig. 3.4. It can be seen that switching frequency varies within a half cycle of the inverter output voltage, from 20 to 170 pu.

The average value of the switching frequency over a half cycle of the ac output voltage will be derived as:

$$f_{sw,ave} = \frac{1}{\pi}\int_0^{\pi} f_{sw}\,d\omega t$$

$$= \frac{V_{in}}{16L\,\Delta I}\left[8 - (L\omega^2\,C_1 - 2)^2\right] \qquad (3.21)$$

As it can be seen from Eqn. (3.21), the average switching frequency varies with respect to values of (L), (C_1), input voltage (V_{in}) and the

hysteresis window size (ΔI). Fig. 3.5 shows that how average switching frequency is affected by the variations in the inductor value (L). Variations in the average switching frequency due to the change in the hysteresis window size (ΔI) and also due to the change in the capacitor value are illustrated in Figs. 3.6, 3.7 respectively. Fig. 3.7 shows that the average switching frequency does not change dramatically with variation in the capacitor value. The average switching frequency also depends on the level of the output voltage. Eqn. (3.21) was obtained, assuming that the inverter provides the rated output voltage. In order to illustrate the effect of the amplitude of the output voltage on the switching frequency, Eqn. (3.20) can be changed to:

$$f_{sw} = \frac{-(L\omega I_P - 2I_P X_{C1})^2 \cos^2\omega t + (4I_P X_{C1} - 2V_{in})(L\omega I_P - I_P X_{C1}) \cos \omega t}{2L\Delta I V_{in}}$$

$$+ \frac{4V_{in} I_P X_{C1} - 4(I_P X_{C1})^2}{2L \Delta I V_{in}} \qquad (3.22)$$

where $$I_P X_{C1} = V_o$$

The average switching frequency is:

$$f_{sw,ave} = \frac{1}{2L \Delta I V_{in}} \left[\frac{-(L\omega^2 C_1 V_o - V_o)^2}{2} + 4V_{in} V_o - 4V_o^2 \right] \qquad (3.23)$$

The variation in the average switching frequency due to the changes in the output voltage (V_o) is illustrated in Fig. 3.8.

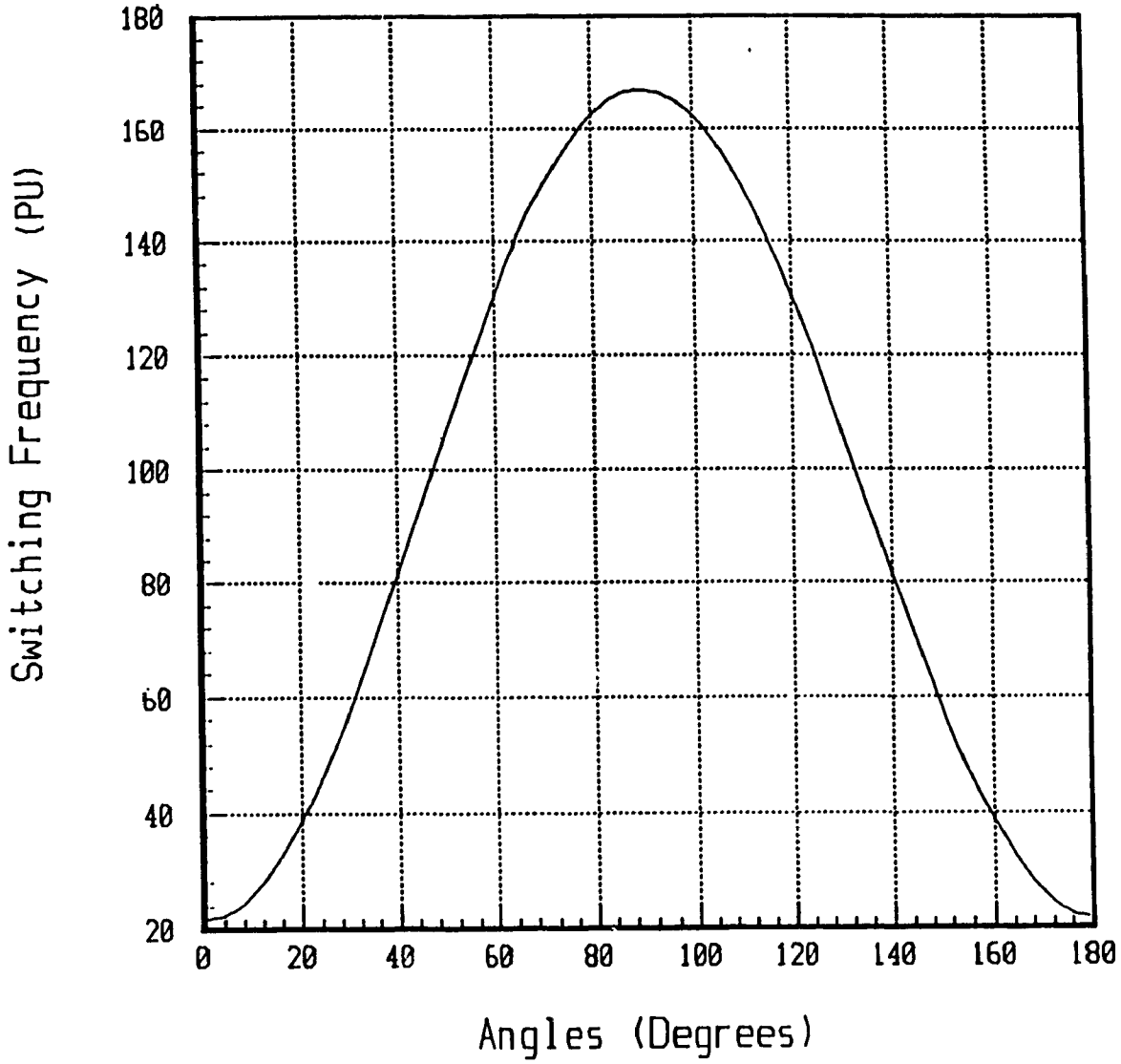

Fig. 3.4 The variation of switching frequency vs. time.

(V_{in} = 2.828 pu, X_{C1} = 3.54 pu, X_L = 0.37 pu, ΔI = 0.141 pu).

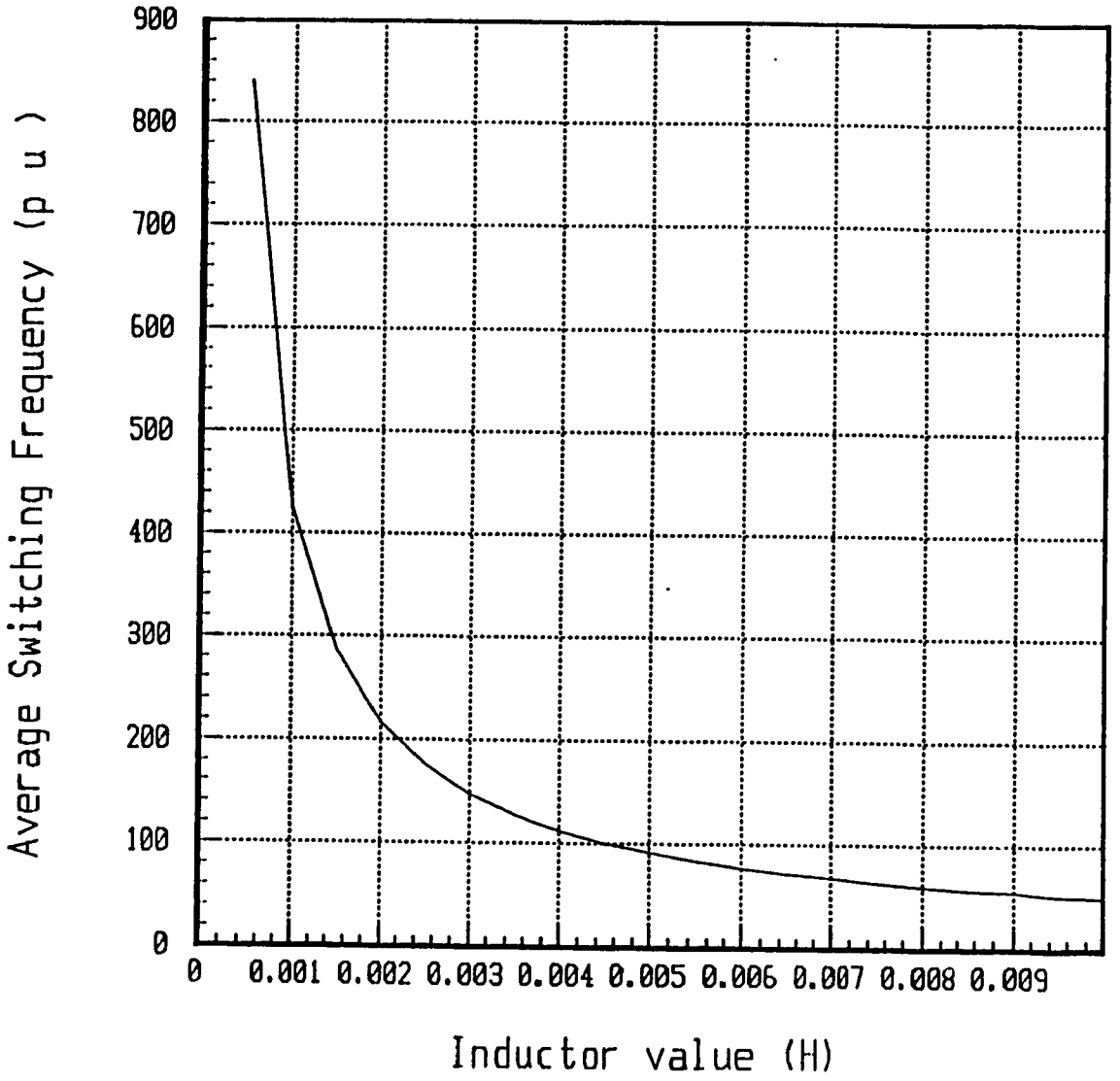

Fig. 3.5 The variation of average switching frequency vs. inductor value. (V_{in} = 2.828 pu, X_{C1} = 3.54 pu, ΔI = 0.141 pu).

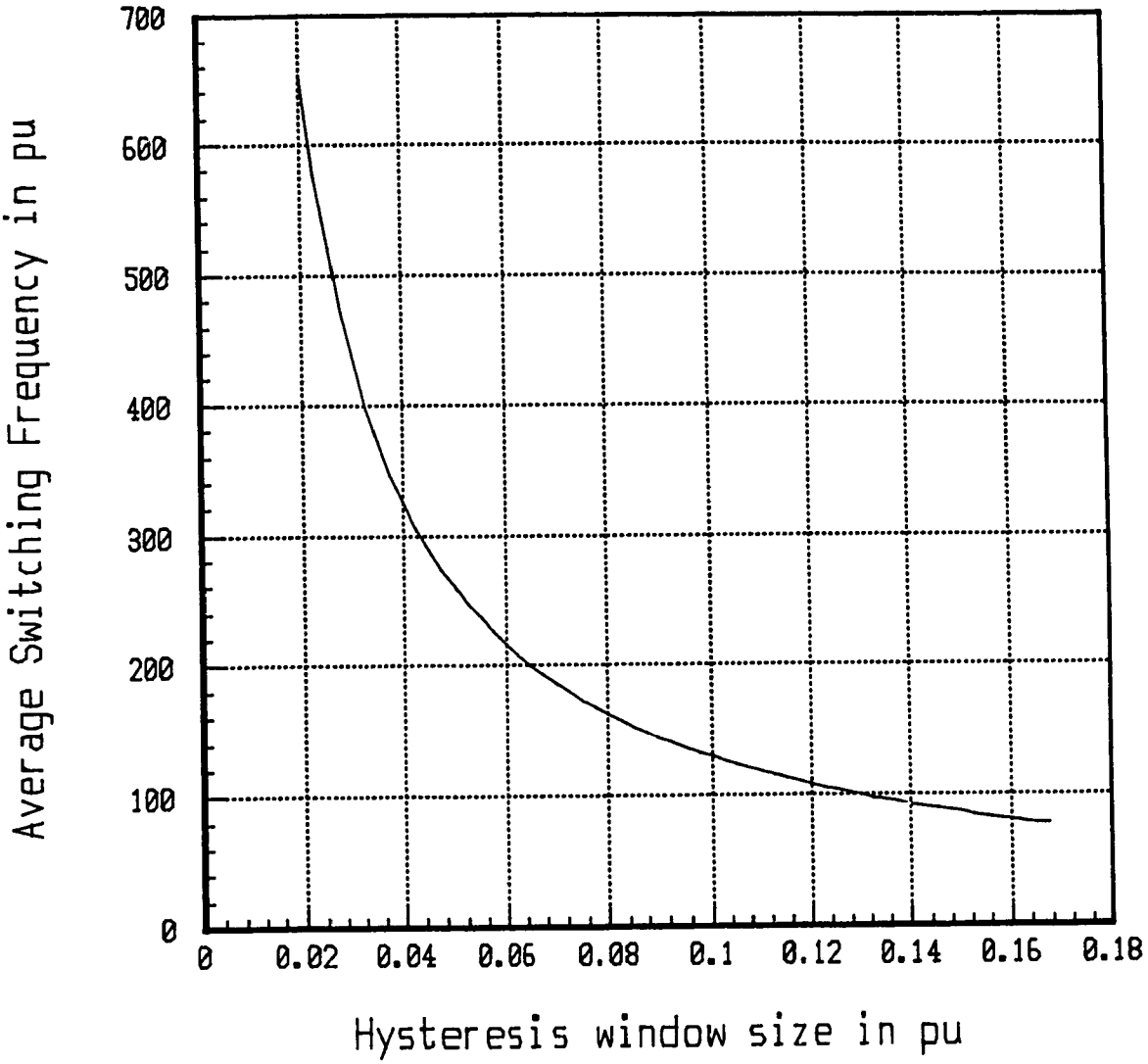

Fig. 3.6 The variation of average switching frequency vs. hysteresis window size (ΔI). (V_{in} = 2.828 pu, X_{C1} = 3.54 pu, X_L = 0.37 pu).

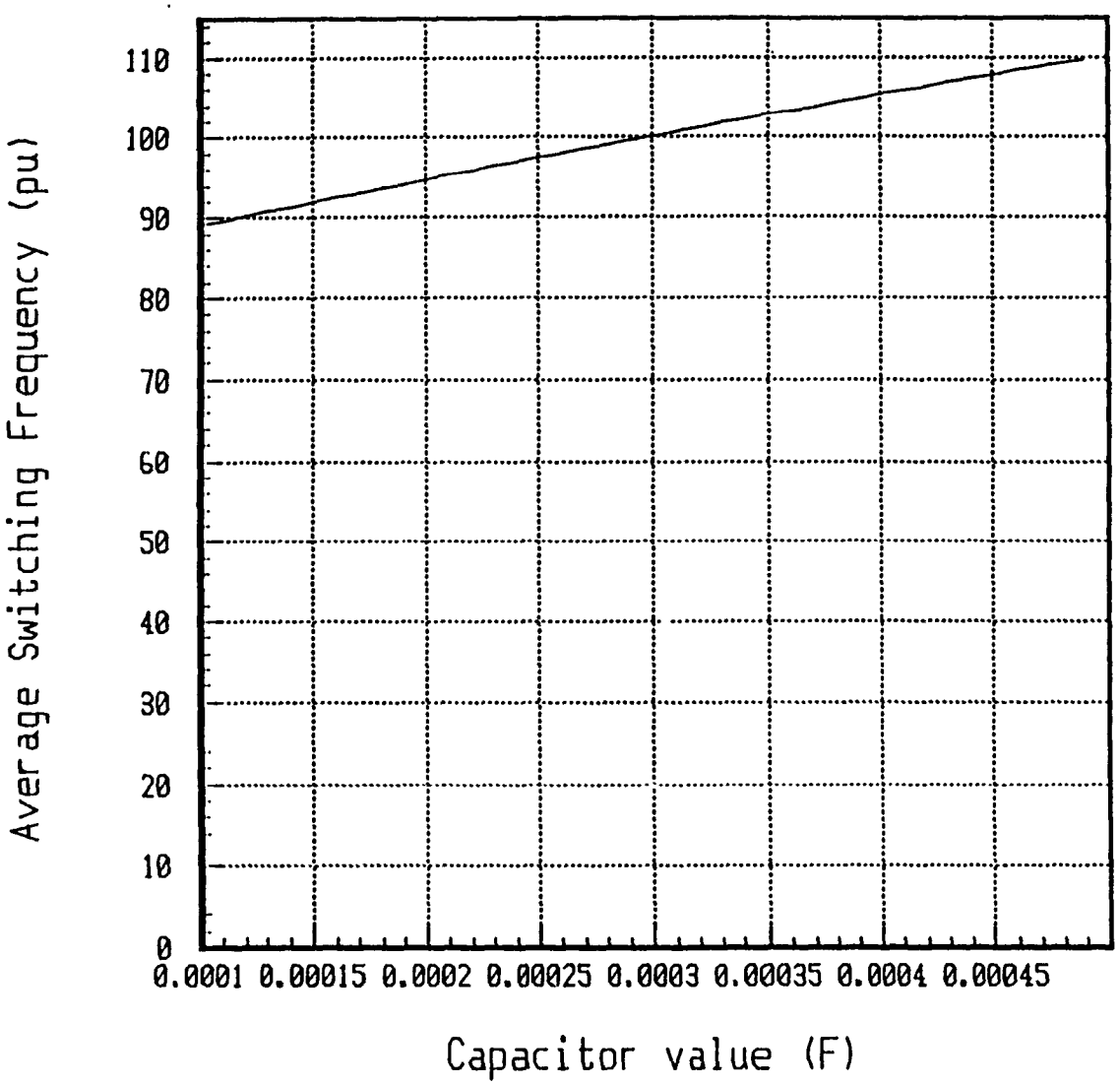

Fig. 3.7 The variation of average switching frequency vs. capacitor value. (V_{in} = 2.828 pu, X_{C1} = 3.54 pu, X_L = 0.37 pu, ΔI = 0.141 pu)

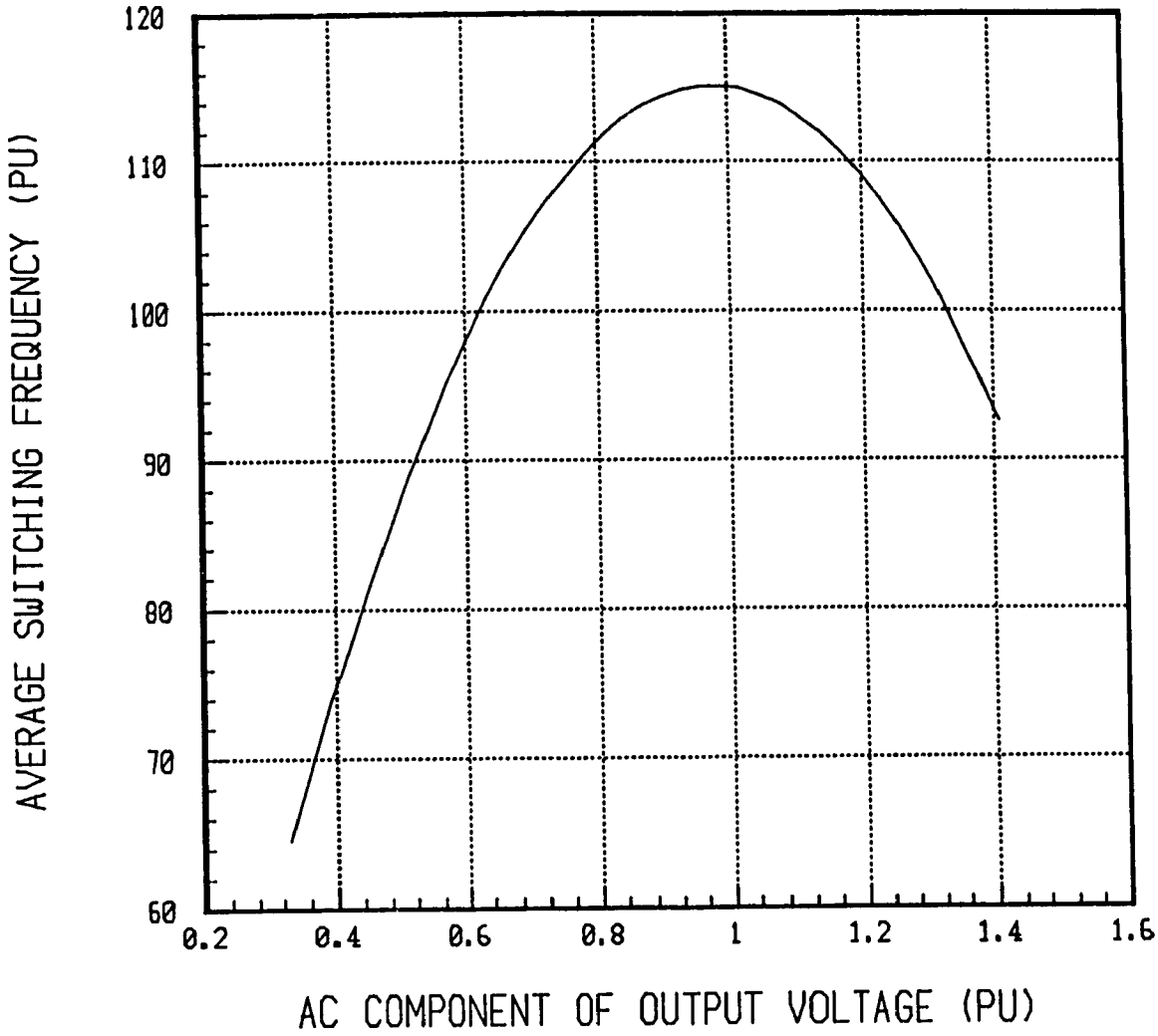

Fig. 3.8 The variation of average switching frequency vs. the ac component of the output voltage.

(V_{in} = 2.828 pu, X_{C1} = 3.54 pu, X_L = 0.37 pu, ΔI = 0.141 pu)

3.2.3 Components ratings

Since the ripple in the capacitor current is neglected, the steady state currents and voltages in the inverter are independent of the applied control technique. Therefore, the component ratings in the power circuit remain unchanged. These ratings are calculated in chapter two.

3.3 The Error triangulation Technique

The main drawback of hysteresis controller is varying switching frequency which results in a wide spread harmonic spectra. To overcome this problem, a control technique is needed which provides constant switching frequency and also does not involve complicated circuitry. The best solution to this matter is the error triangulation technique. Implementing this technique with the proposed converter combines the following advantages:

- low and constant switching frequency,
- simple implementation, and
- fast transient response.

In the following sub-sections, the error triangulation technique is studied and the complete analysis and design guidelines are provided. A design example is given to complete the analysis.

3.3.1 Principles of operation

The complete converter circuit and control scheme of the error triangulation technique are shown in Fig. 3.8. Switching points are obtained by comparison of the error with a triangular waveform. The inverter switches at the frequency of the triangular waveform and produces well-defined harmonic frequencies (basically at switching frequency). A simple proportional controller can be used to obtain near sinusoidal output voltage. The slope of the filter capacitor current (i_{C1}) is well defined

ensuring intersections. An integral term is added to the proportional term (Fig. 3.9) to improve the tracking between the reference and the feedback and thus the quality of the current waveform. The control circuit consists of two loops:

- A fast internal current loop, and
- a slow voltage loop which provides output voltage regulation.

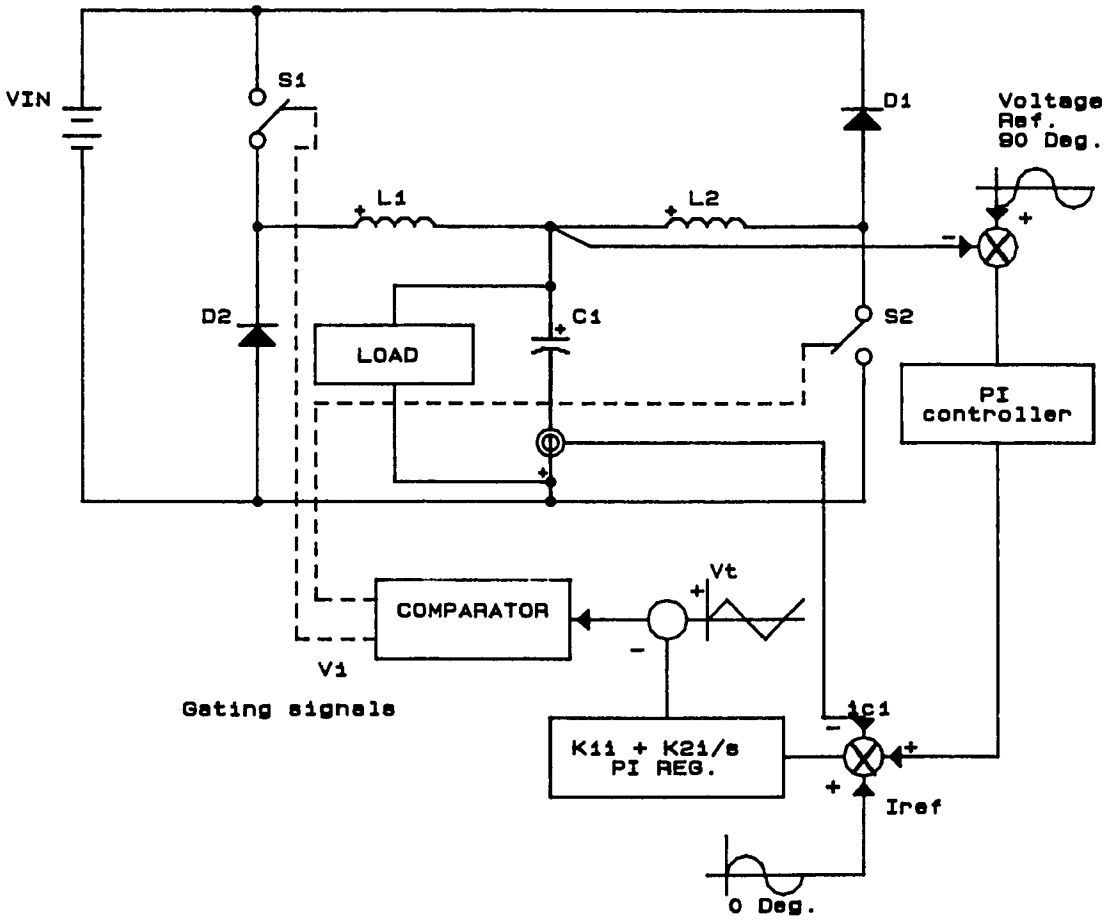

Fig. 3.9 The proposed converter module and control scheme.

3.3.1.1 Capacitor current loop

In order to obtain a sinusoidal output voltage independently of the load, it is sufficient to ensure that the capacitor current (i_{c1}) is sinusoidal (Fig. 3.9). This is done by comparing the actual current passing through the capacitor (i_{c1}) with a sinusoidal current reference whose magnitude is dictated by the desired output voltage magnitude (I_p). The error (I_f) is fed to a proportional-integral regulator and compared with a triangular waveform (V_t) to obtain the necessary gating signals to control the switches (Fig. 3.10). When the amplitude of the error (I_f) is larger than that of the triangular waveform, the output of the comparator (V_1) is positive and the top switch (S_1) turns on, hence increasing the capacitor current and reducing the error. Fig. 3.10 shows the principles of operation and the respective output of the comparator.

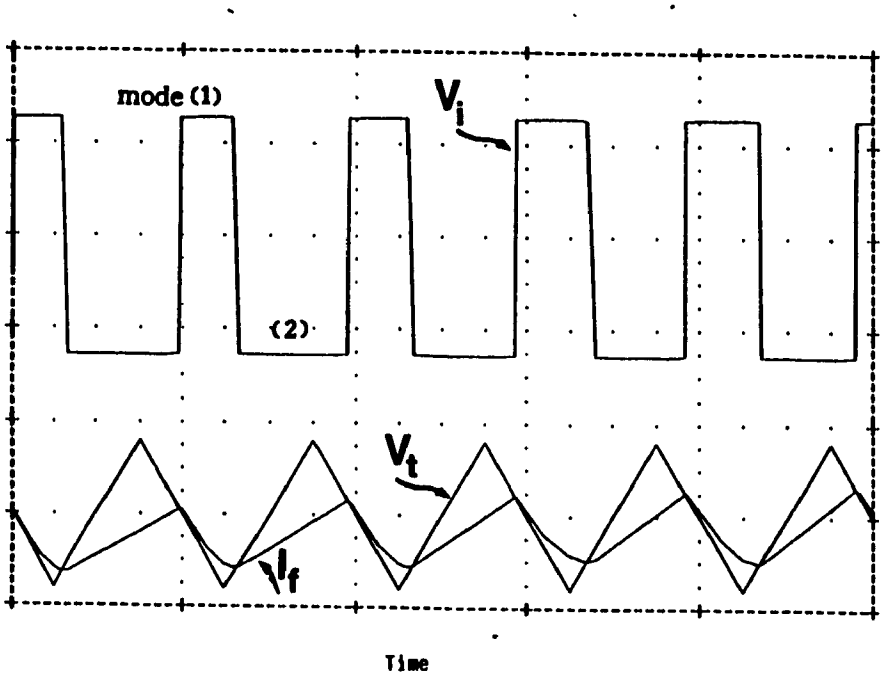

Fig. 3.10 The principles of operation of the proposed current control technique

3.3.1.2 Voltage loop

Ideally, the output voltage can be controlled by controlling the capacitor current. However, if a dc offset exists in the current reference, it will charge up the capacitor voltage. If the capacitor voltage exceeds the input dc voltage, the control over the capacitor current is lost, since turning on the top switch will no more increase the capacitor current and will not compensate for the current error. In order to ensure that the capacitor voltage never exceeds the dc bus voltage, and to compensate for the possible existing dc offset in the capacitor current reference, use of the voltage loop becomes necessary. This voltage loop also maintains the proper voltage regulation, improves the voltage gain of the proposed module, and compensates for the imperfections of implementation. The output voltage (Fig. 3.9) is compared with a sinusoidal reference and the error is fed to a PI regulator. The output of the voltage regulator is then subtracted from the current reference, so the current reference can be changed due to the output voltage requirements as shown in Fig. 3.9.

3.3.2 Analysis

In the following sections the proposed control method which consists of two control loops is explained. The design guidelines are derived and a general design procedure is given.

3.3.2.1 Capacitor Current Loop

In order to ensure that the feedback signal tracks the reference, a condition on the slope of the error must be satisfied. This requires calculation of the maximum slope of the capacitor current. It is obvious that the maximum slope of the capacitor current should be calculated under noload conditions, i.e., $i_o = 0$. In section 3.2.3 the slope of the capacitor current in mode (1) was found to be:

$$\frac{di_{C1}}{dt} = \frac{2(V_{in} - v_{C1}(t))}{L}$$

The maximum slope is obtained when $v_{C1} = 0$:

$$\frac{di_{C1}}{dt}_{max} = \frac{2\ V_{in}}{L} \qquad (3.24)$$

Similar results can be obtained for mode (2). To maintain proper control over the capacitor current, multiple crossing between the error signal I_f and the triangular waveform must be avoided. So the maximum slope of the error (I_f) should be less than the slope of the triangular waveform. This means that the following condition applies in terms of magnitudes:

$$\text{slope of } I_f < \text{slope of } V_t$$

Assuming the gain of the proportional controller is K_{11}:

$$K_{11} \times (\text{slope of } i_{ref} - \text{slope of } i_{C1}) < \text{slope of } V_t$$

The reference current is a sinusoidal waveform:

$$i_{ref}(t) = I_p \sin \omega t$$

$$\text{slope of } i_{ref}(t) = I_p\ \omega \cos \omega t$$

The maximum slope of the error signal (V_f) is obtained when $\omega t = 180^\circ$:

$$\text{max slope } (i_{ref}) = I_p\ \omega = 2\pi\ f_o\ I_p$$

where f_o is the fundamental frequency of the current reference. From Fig. 3.11 the slope of the triangular pulse is calculated as:

$$\text{slope of } V_t = 4\ V_m f_m$$

where V_m and f_m are the magnitude and the frequency of the triangular carrier. From the above and Eqn. (3.24):

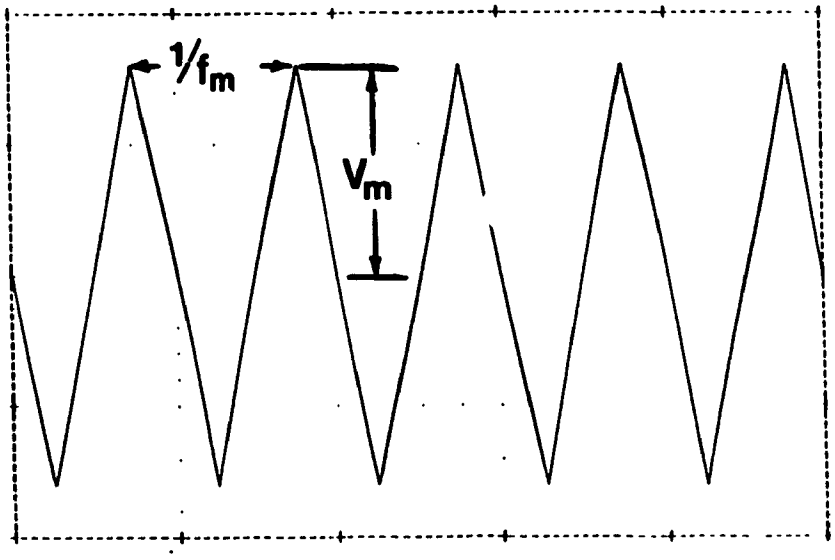

Fig 3.11 Triangular carrier.

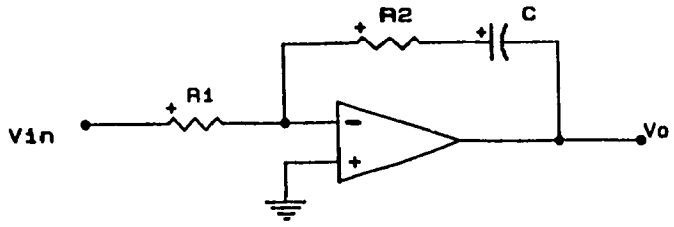

Fig. 3.12 A simple PI controller.

$$K_{ii}\left(\frac{2\,V_{in}}{L} + 2\pi f_{op} I\right) < 4V_m f_m \qquad (3.25)$$

The design of the power and control circuit is based on Eqn. (3.25), depending on the maximum capacitor current ripple (ΔI_m).

To achieve high quality output voltage, a fast integrator is needed for the current loop, although using only a proportional (P) controller, results in a fairly good sinusoidal output voltage. A simple proportional integral

(PI) controller is shown in Fig. 3.12. The output voltage of this controller block is given by:

$$V_{o,PI} = -\left[\frac{R_2}{R_1} V_{in} + \frac{1}{R_1 C} \int V_{in}\right]$$

The integral and proportional gain of a typical PI controller are defined to be:

$$K_{int} = \frac{1}{R_1 C}$$

$$K_{pro} = \frac{R_2}{R_1}$$

At least one switching is needed to correct the error in the actual capacitor current. This means that the error signal I_f, can not be corrected in time less than one switching period, in other words, the integral gain of the PI controller must be less than the switching frequency. A fairly fast response can be obtained by choosing the integral gain of the regulator (K_{21}) in the range of (0.5-1) switching frequency, while the proportional gain is assumed to be equal to one:

$$K_{21} = (0.5 - 1)f_m$$

$$K_{11} = 1$$

where: k_{11} = the proportional gain

k_{21} = the integral gain

3.3.2.2 Triangular Carrier

The actual capacitor current and the reference current are shown in Fig. 3.13. If intersections are present, the maximum current error does not exceed the amplitude of the triangular waveform. This can be shown as an imaginary hysteresis window, Fig. 3.13.

$$\Delta I_{tri} = 2 V_m$$

where V_m is the magnitude of the triangular carrier.

The error in the actual capacitor current (I_f) is limited to the magnitude of the triangular waveform V_m (Fig. 3.10). The desired percentage of the capacitor current ripple (n%) limits the value of V_m. Since the output voltage of the inverter is the integral of the capacitor current, the magnitude of the triangular carrier (V_m) can be high without resulting in a large output voltage distortion. By increasing the magnitude of the triangular carrier, the switching frequency or the component values are decreased and the implementation of the method is facilitated. However, the voltage gain of the inverter is decreased. It should be noted that high values of capacitor current ripple reduce the capability of the control technique for handling nonlinear loads and load transients.

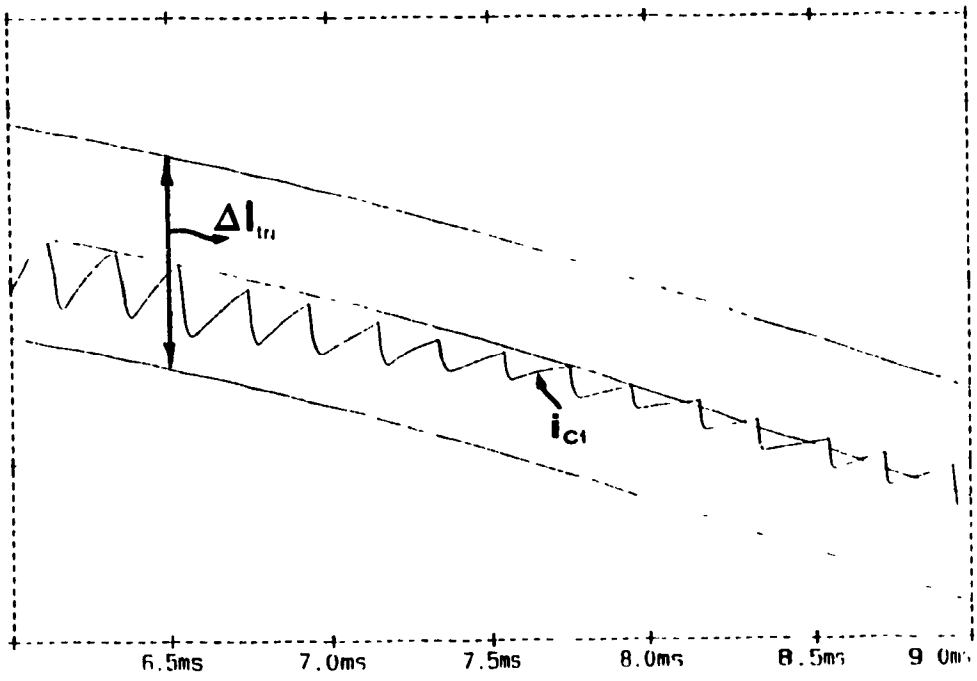

Fig. 3.13 The actual capacitor current (i_{C1}) and the imaginary hysteresis window (ΔI_{tri}).

Synchronization of the triangular carrier and the reference current is not needed, since the switching frequency is usually much higher than the line frequency. The frequency and the magnitude of the triangular waveform are designed considering the condition described in Eqn. (3.25).

3.3.2.3 Voltage loop

Since the triangular carrier and the current reference are not synchronized, a dc offset always exists in the output voltage, which is associated with the current control technique. This dc offset reduces the voltage gain of the inverter in a single phase system. If the current reference is shifted (which is the case in a three phase system), the value of this dc offset changes.

In order to compensate for the imperfections in the implementation , to eliminate the undesired dc offset in the capacitor current, and to improve the voltage gain of the system, the voltage loop becomes necessary. To avoid interference between the current loop and the voltage loop, the time constant of the PI controller in the voltage loop must be much larger than that of the current loop. The time constant of a PI regulator is defined as:

$$\tau = \frac{k_{pro}}{k_{int}}$$

So for a slower voltage loop:

$$\tau_{cur,loop} = 0.1\ \tau_{vol,loop}$$

or:

$$\frac{k_{1i}}{k_{2i}} = 0.1 \times \frac{k_{1v}}{k_{2v}}$$

If the proportional gain is normalized on the same base as the current loop, i.e.:

$$k_{1v} = k_{1i} = 1$$

The integral gain of the PI regulator in the voltage loop can be:

$$k_{2v} = 0.1\ k_{2i}$$

The reference waveform for the voltage loop is the desired sinusoidal output voltage which is known both in amplitude and phase.

3.3.3. General design procedure

The capacitor value is chosen to obtain a relatively high impedance at fundamental frequency. To ensure a minimum current passing through the capacitor and not affecting the load, this impedance can be ranged from 3 pu to 10 pu. The current reference for the maximum output voltage is calculated as:

$$I_p = \frac{V_{in}}{2\ X_{C1}}$$

Assuming that only a P regulator with a gain of one is used, the maximum capacitor current ripple is limited by the peak value of triangular waveform, the value of V_m is then fixed:

$$\frac{V_m}{I_p} = n\ \%$$

Substituting I_p from Eqn. (2.11) and solving for V_m results in:

$$V_m = \frac{2X_{C1}\ n}{V_{in}} \qquad (3.26)$$

Now, from Eqn. 3.25 the values of f_m, L are calculated.

3.3.4 Design example

The following specifications will be considered for the design example:

$$V_{in} = 100\ V$$

$$V_{o,ac,peak} = 50\ V$$

$$S_{o,ac} = 250\ VA$$

$$f_o = 60\ Hz$$

To provide rated output KVA the output current must be:

$$i_{o,ac,rms} = \frac{250}{50 \times 0.707} = 7.07 \text{ A}$$

$$i_{o,ac,peak} = 10 \text{ A}$$

Taking the rated values as the base parameters, the base impedance can be calculated:

$$Z_{base} = \frac{V_{o,ac,rms}}{i_{o,ac,rms}} = 5 \ \Omega$$

To provide the rated output power for a resistive load, the load impedance must be one per unit:

$$P_{o,ac} = 1 \text{ pu}$$

$$V_{o,ac,rms} = 1 \text{ pu}$$

$$R_{load} = 1 \text{ pu}$$

The switching frequency and the maximum ripple percentage of the capacitor current are chosen to be:

$$f_{sw} = 10 \text{ kHz}$$

$$n = 35\%$$

3.3.4.1 Component values

First the capacitor value is chosen:

$$C_1 = 150 \ \mu F$$

$$X_{C1} = 3.537 \text{ pu}$$

Then, the capacitor current is calculated. Next from Eqns. (3.26) and (3.25) the values of V_m, L are chosen:

$$I_p = 2.827 \text{ A}$$

$$V_m = 0.35 \times 2.827 = 1 \text{ V}$$

Using Eqn. (3.25), the inductor value is calculated:

$$L = 5 \text{ mH}$$

$$X_L = 0.377 \text{ pu}$$

3.3.4.2 Component ratings

Substituting the base values in the device ratings obtained in chapter two, the following will result:

$$i_{C1,rms} = 2.0 \text{ A} \qquad v_{C1,rms} = 61.2 \text{ V}$$

$$i_{L1,rms} = 15.44 \text{ A} \qquad v_{L1,peak} = 100 \text{ V}$$

$$i_{L2,rms} = 6.21 \text{ A} \qquad v_{L2,peak} = 100 \text{ V}$$

$$i_{D1,rms} = 1.55 \text{ A} \qquad v_{D1,rev} = 100 \text{ V}$$

$$i_{D2,rms} = 7.11 \text{ A} \qquad v_{D2,rev} = 100 \text{ V}$$

$$i_{sw1,rms} = 8.75 \text{ A} \qquad v_{sw1,rev} = 100 \text{ V}$$

$$i_{sw2,rms} = 5.22 \text{ A} \qquad v_{sw2,rev} = 100 \text{ V}$$

3.4. Predictive Method

To provide a good view over different types of current control techniques, it will be usefull to analyze and discuss a predictive controller for the proposed inverter with capacitor current control.

A predictive current control with constant switching frequency is discussed below. This technique provides an instantaneous control over the current and a fast response to the output transients. Its main drawbacks include: complicated circuitry and parameter sensitivity because of which the use of an input voltage sensor becomes necessary.

3.4.1. Principles of operation

The main circuit of the inverter (Fig. 3.14) is being considered. A switching function for the top switch (S_1) is required which forces the capacitor current to follow a reference current. Assuming that the capacitor current i_{C1} will follow the reference current with only one switching period

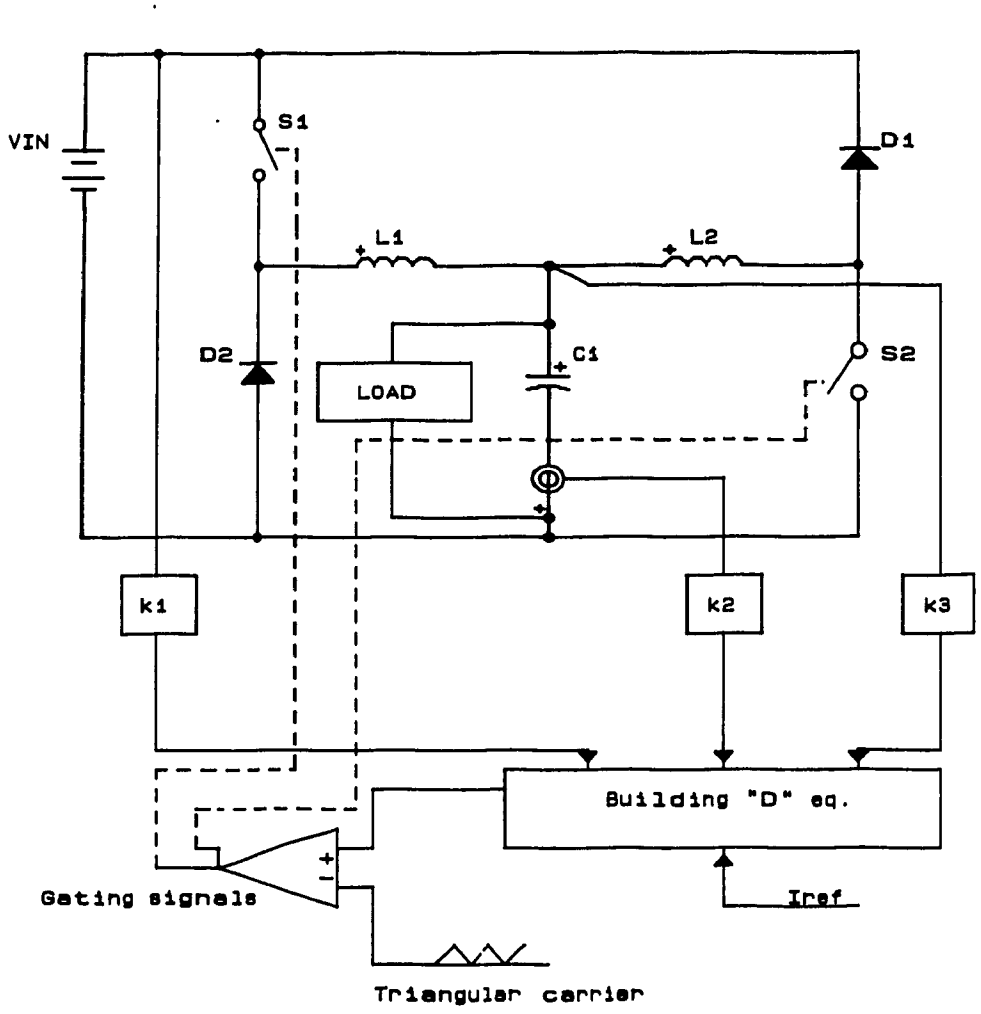

Fig. 3.14 The proposed converter with the predictive controller.

(T) delay, the equation below is obtained:

$$i_{C1}(t) + T\frac{di_{C1}}{dt} = i_{C1,ref}(t) \tag{3.27}$$

Where T is the switching period. From Eqn. (2.9) the average switching function is :

$$D = \frac{AC_1\frac{d^2v_{C1}}{dt^2} + \frac{A}{R}\frac{dv_{C1}}{dt} + v_{C1}(t)}{V_{in}} \tag{3.28}$$

The relation between the current and the voltage of a capacitor is:

$$i_c(t) = C\frac{dv_c}{dt}$$

Rewriting Eqn. (2.9) by substituting the capacitor current i_{C1} and considering A = L/2, results in:

$$D = \frac{\frac{L}{2}\frac{di_{C1}}{dt} + \frac{L}{2RC_1}i_{C1}(t) + v_{C1}(t)}{V_{in}} \tag{3.29}$$

Eqn. (3.27) can be changed to:

$$\frac{di_{C1}}{dt} = \frac{1}{T}\left(i_{C1,ref}(t) - i_{C1}(t)\right) \tag{3.30}$$

Substituting Eqn. (3.30) into Eqn. (3.29) yields:

$$D = \frac{L}{2V_{in}T}\left(i_{C1,ref}(t) - i_{C1}(t)\right) + \frac{L}{2R\,C_1V_{in}}i_{C1}(t) + V_{C1}(t) \tag{3.31}$$

The capacitor current can be controlled by the on-time of the top switch (D). Since the average switching function (D) always varies between 0 and 1, the gating signals can be obtained by comparing the "D" equation with

a triangular carrier of magnitude of one, whose frequency is the same as desired switching frequency.

$$f_p = f_{sw} = 1/T$$

where f_p is the frequency of the triangular carrier. The principles of operation of the predictive controller are shown in Fig. 3.15. This method provides constant switching frequency and instantaneous current control but it uses a complicated circuit. Also, since the "D" equation is dependent of input dc voltage V_{in}, use of an input voltage sensor becomes necessary which in turn adds to the complexity of the control technique.

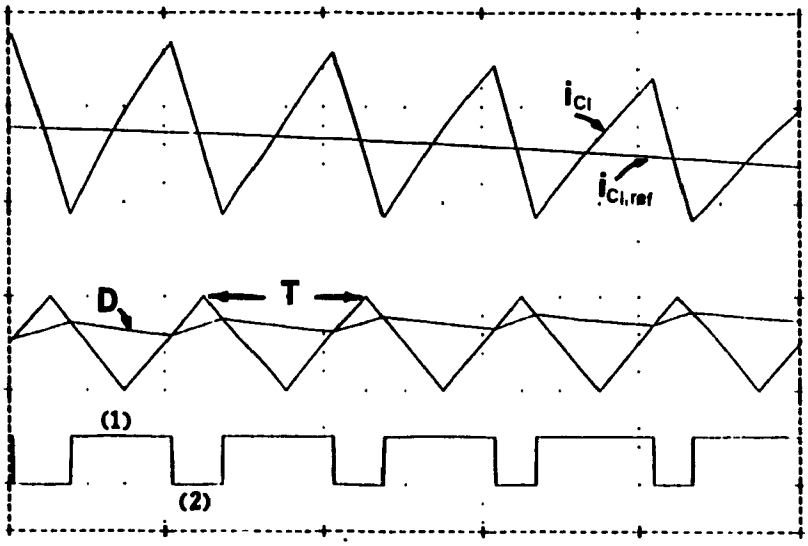

Fig. 3.15 Principles of operation of the predictive controller.

3.5 Comparison of the Current Control Techniques

The three discussed techniques are compared in the following aspects.

- Switching frequency;
- Implementation considerations;
- Component ratings.

3.5.1 Switching frequency

Switching frequency is a very important issue in switched mode converters. In BBH method, the maximum ripple in the capacitor current is constant (ΔI) and the switching frequency varies within a cycle of the output voltage. Varying switching frequency increases the stresses on the switches and decreases the system reliability as well as increasing the size of passive filters required in the system. With the proposed technique, constant switching frequency is achieved, but the amplitude of the error in the capacitor current changes, although its maximum value is limited to the amplitude of the triangular carrier. The predictive method also operates at constant switching frequency. The actual error changes within a cycle of the output voltage but it is also centered around zero.

3.5.2 Implementation considerations

Since only the ac component of the capacitor current is controlled by the control technique, an external voltage loop is needed to eliminate the undesired dc offset in the current reference and to compensate for the implementation imperfections. Also, to maintain control over the capacitor current, the following equation must hold true for the full cycle of the output voltage:

$$2X_{C1}\ (I_p + I_r) < V_{in} \tag{3.32}$$

where I_r is the steady state ripple in the capacitor current. According to Eqn. (3.32), the BBH technique can not operate with large values of the hysteresis window size (ΔI), unless the peak value of the current reference is reduced (I_p). A lower value of current reference results in a lower level for the output voltage and thus a reduced voltage gain. Decreasing the size of the hysteresis window, increases the switching frequency which is not

desirable. Adding the voltage loop, allows the BBH technique to operate with larger ripple in the capacitor current. But, the simplicity of the method will be compromised.

The error triangulation method needs the external voltage loop to eliminate the dc offset in the capacitor current and to provide the desired output voltage regulation. However, eliminating the voltage loop will only result in a small reduction in the voltage gain and does not affect the control of the capacitor current.

As it can be seen from Eqn. (3.31), the predictive method requires an output voltage sensor. Also, since the input voltage V_{in} appears in the "D" equation, the method is sensitive to the variations in the input voltage. Therefore, use of an input voltage sensor becomes necessary.

Both error triangulation technique and BBH technique are implementable by analog circuitry. The BBH technique needs a less complicated circuit than the two other techniques. For the predictive controller, building the "D" equation needs a complicated circuit. The predictive controller also suffers from parameter sensitivity which makes it difficult to implement.

3.5.3 Component ratings

As it was mentioned earlier, the component ratings for the discussed methods are similar. The type of the control method used does not affect the component ratings and the power circuit design.

3.6 Conclusions

Different types of current controllers have been studied in this chapter. Implementation of each of these controllers for the novel two switch current regulated inverter module has been discussed and the following conclusions obtained:

- Hysteresis controller provides a tight and rugged control over the current but it has the obvious disadvantage of varying switching frequency. In order to maintain the control over the capacitor current, this technique must operate with small values of ΔI. According to Eqn. (3.21), small values of ΔI result in increased switching frequency and consequently produce extra stresses on the switches.

- Predictive controller yields a fast response to load transients but it needs a complicated circuitry. Also, parameter sensitivity is a main disadvantage of this method which makes it hard to implement.

- Error triangulation technique with an added PI regulator provides a good control over the capacitor current. Implementing this technique for the proposed converter module exhibits the following advantages:

- Low and constant switching frequency,

- fast response to input and output transients,

- excellent response time in tracking load non-linearities, and

- simple implementation.

A design example for the combined power circuit and control technique has been given.

CHAPTER 4

SIMULATION RESULTS

4.1 Introduction

In order to verify the derived equations and study the transient behavior of the inverter, the proposed current regulated converter module is simulated by SPICE [31]. In the following sections the simulation results are provided for the proposed current control technique, the BBH method and the predictive method. The aforementioned drawbacks of the predictive and hysteresis method are confirmed by simulation. The simulation results of the proposed converter and control technique for load transients and nonlinear loads are also provided.

4.2 Single Phase Converter

The design example discussed in the previous chapter is simulated and steady and transient analysis are performed on the circuit. A lower ratio of switching frequency to line frequency is chosen to clearly bringing out the main features of the techniques. The switching frequency is chosen as:

$$f_{sw} = 5000 \text{ Hz}$$

The remaining design values remain unchanged:

$$V_{in} = 100 \text{ V dc}$$

$$S_{o,ac} = 250 \text{ VA}$$

$$I_{o,ac,peak} = 10 \text{ A}$$

$$V_{o,ac,peak} = 50 \text{ V}$$

$$f_o = 60 \text{ Hz}$$

$$X_L = 0.37 \text{ pu}$$

$$X_{C1} = 3.54 \text{ pu}$$

The reference current and output dc offset were calculated as:

$$I_p = 2.83 \text{ A}$$

$$\text{output dc offset} = 50 \text{ V}$$

4.2.1 Linear load

The proposed inverter with a 1 pu resistive load is controlled by the three discussed current control techniques and the output waveforms are plotted to confirm the advantages of the error triangulation method. The results are described in the following sub-sections.

4.2.1.1. Hysteresis technique

The BBH method is used to control the capacitor current in the previously designed power circuit. In order to maintain the control over the capacitor current the size of the hysteresis window (ΔI) had to be changed to a small value.

$$\Delta I = 0.141 \text{ pu}$$

Fig. 4.1 shows the inverter output voltage and the respective gating signals. The frequency spectrum of the capacitor current in Fig. 4.2(a) clearly shows that the harmonics are spread over a wide frequency range. Fig. 4.2(b) again proves that the frequency spectrum of the output voltage is almost clean and ideal. The voltage gain of the inverter can be calculated from Fig. 4.2(b) which is almost equal to one. The capacitor current and the hysteresis window are shown in Fig. 4.3(a). In order to clarify the effect of ΔI on the performance of the converter, simulation results are also obtained for a larger hysteresis window size. In this case the hysteresis window size is chosen to be equal to the size of imaginary

window in error triangulation technique:

$$\Delta I = \Delta I_{trl} = 0.45 \text{ pu}$$

The capacitor current, the reference current, and the hysteresis window are shown in Fig. 4.3(b). Fig. 4.3(b) indicates that with increasing ΔI, the control over the capacitor current can be lost. Large value of hysteresis window will dramatically distort the inverter output voltage as can be seen from Fig. 4.4.

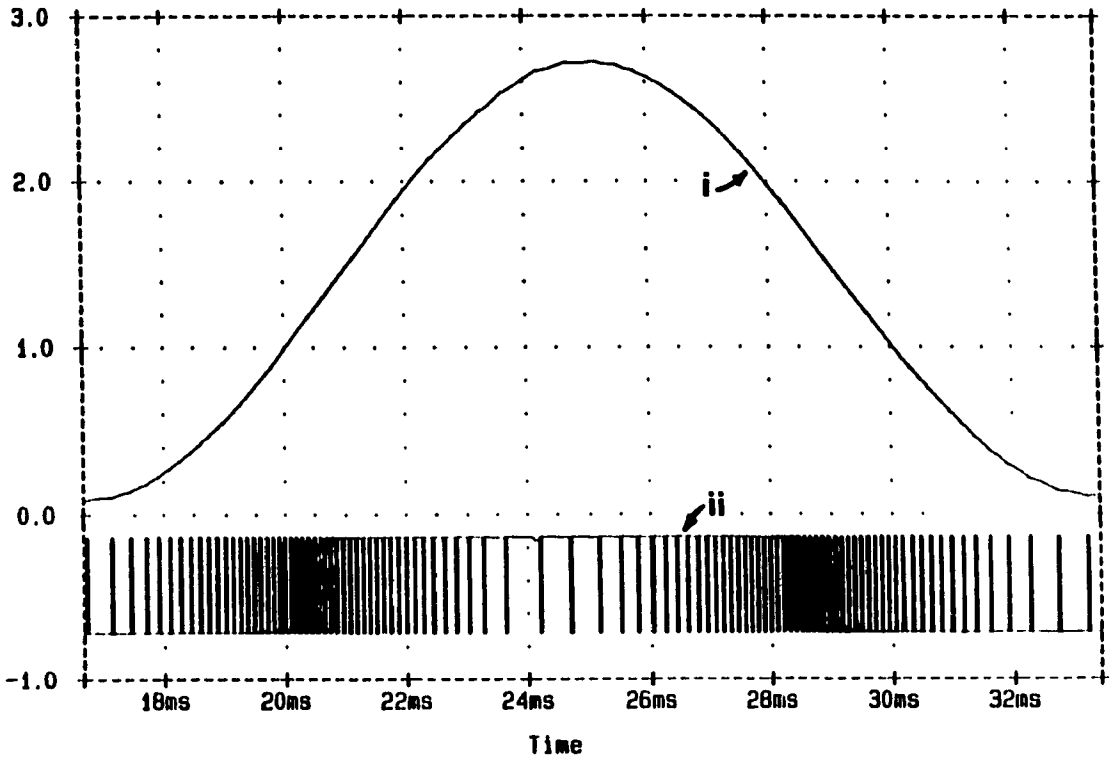

Fig. 4.1 Output voltage for the inverter with hysteresis controller.

(i) Output voltage.

(ii) Gating signals.

(V_{in} = 2.828 pu, ΔI = 0.141 pu, R_{Load} = 1 pu).

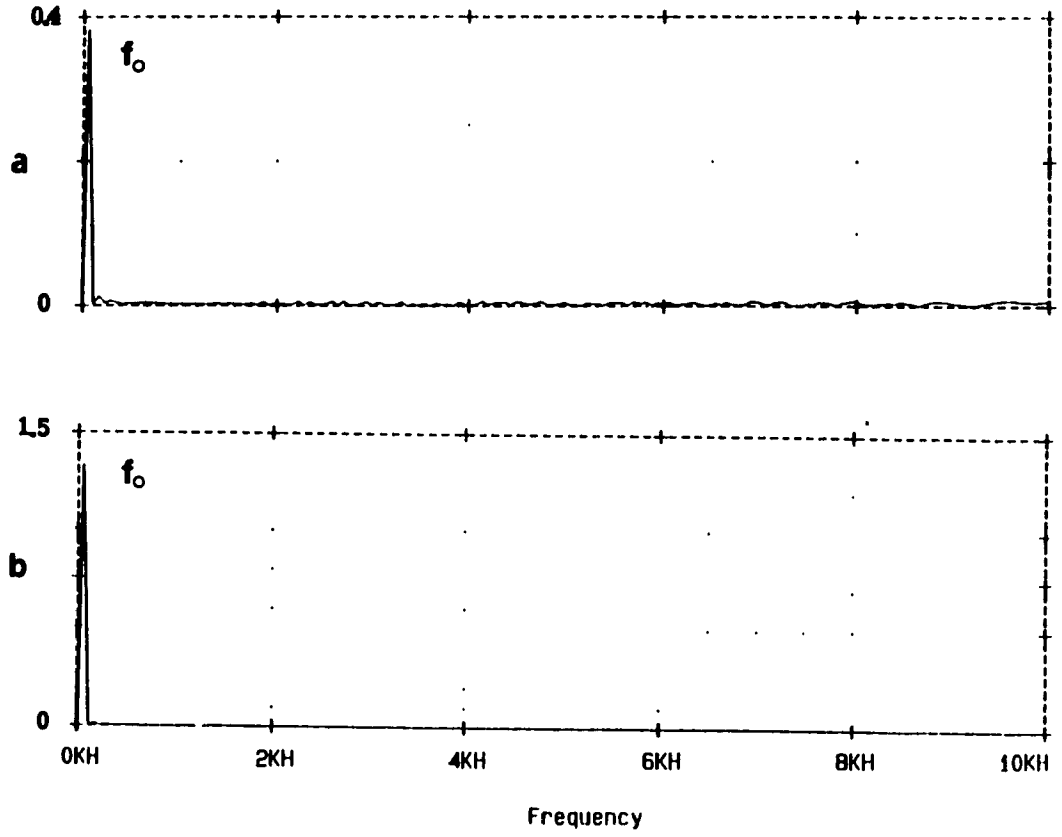

Fig. 4.2 a) Frequency spectrum of the capacitor current.

b) Frequency spectrum of the output voltage.

(f_o = fundamental component, V_{in} = 2.828 pu, ΔI = 1.414 pu).

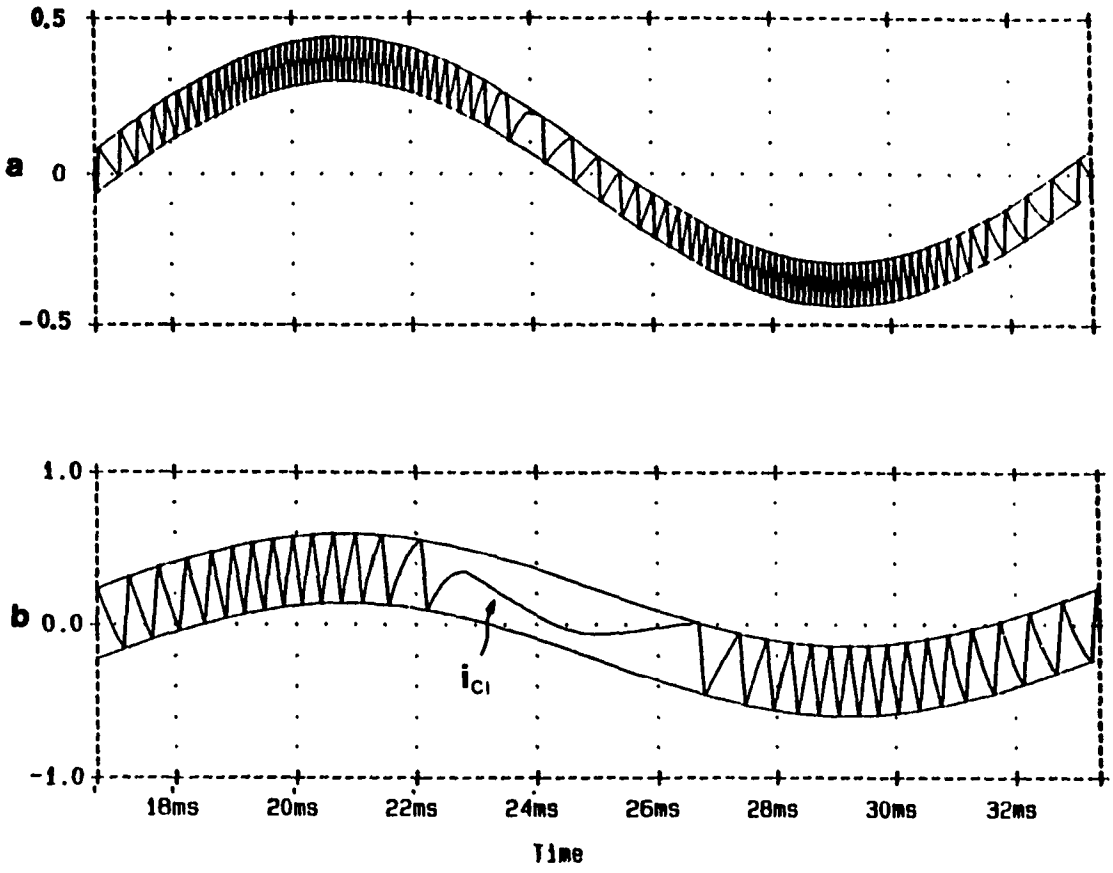

Fig. 4.3 a) The capacitor current and hysteresis window. (ΔI = 0.141 pu)

b) The capacitor current and hysteresis window. (ΔI = 0.45 pu).

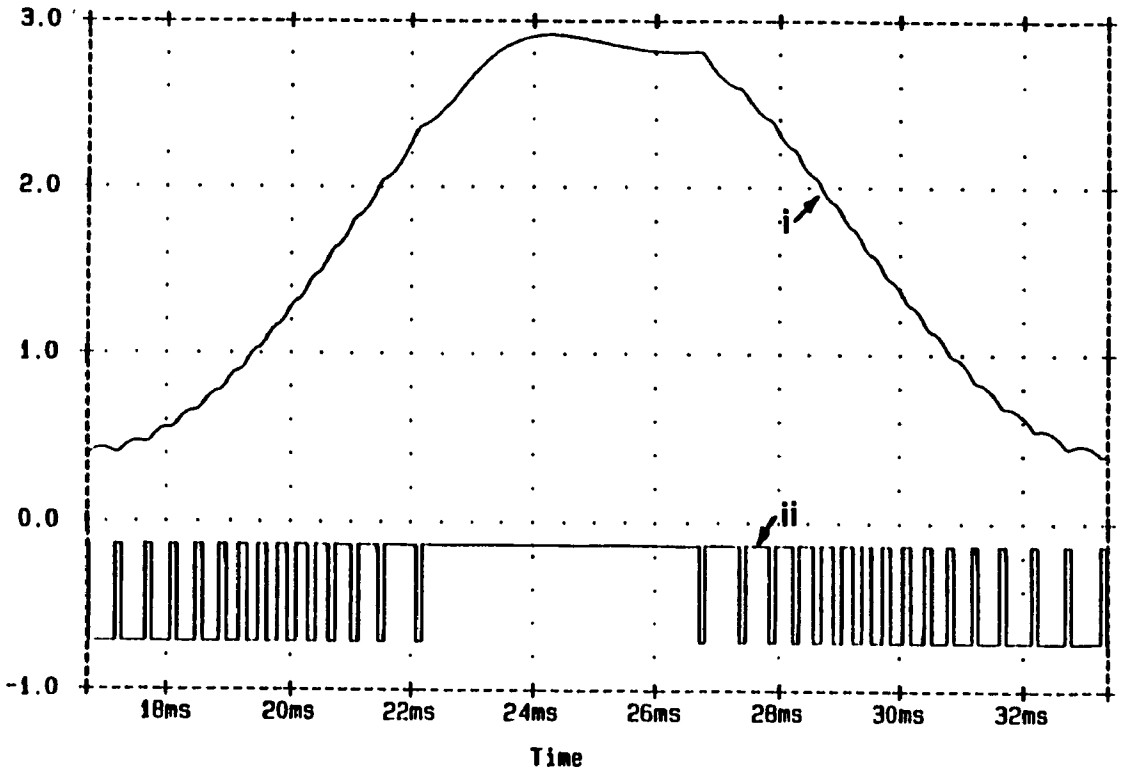

Fig. 4.4 Output voltage for the inverter with hysteresis controller.

(i) Output voltage.

(ii) Gating signals.

(V_{ln} = 2.828 pu, ΔI = 0.45 pu, R_{Load} = 1 pu).

4.2.1.2 Error triangulation technique

For the proposed current control technique, since the switching frequency is changed, the amplitude of the triangular carrier must also change to:

$$V_m = 0.22 \text{ pu}$$

For a 1 pu resistive load, output voltage, capacitor current and gating signals during a full cycle of the output voltage are shown in Figures 4.5, 4.6, 4.7. Figure 4.5(a) indicates that the output voltage has very low distortion and is almost ideal sinusoidal waveform. Fig. 4.5(b) indicates the effect of the voltage loop on the operation of the proposed control technique. This figure proves that a sinusoidal output voltage is obtained even without the external voltage loop. However, the voltage gain of the inverter is decreased and the dc offset of the output voltage is changed. The capacitor current and the imaginary hysteresis window (ΔI_{trl}) are shown in Fig. 4.6.

$$\Delta I_{trl} = 2 \times V_m = 0.45 \text{ pu}$$

Figure 4.6 proves that although capacitor current has a large ripple, the output voltage remains ideally sinusoidal. From Figs 4.5 and 4.6, it can be seen that the minimum error in the capacitor current corresponds to maximum output voltage, which provides more flexibility in handling large current errors (ΔI_{trl}). The harmonic content of the capacitor current (Fig. 4.7(a)), includes mainly multiples of the switching frequency since constant switching frequency is achieved. The frequency spectra of the output voltage is shown in Fig. 4.7(b), which indicates the maximum voltage gain achieved.

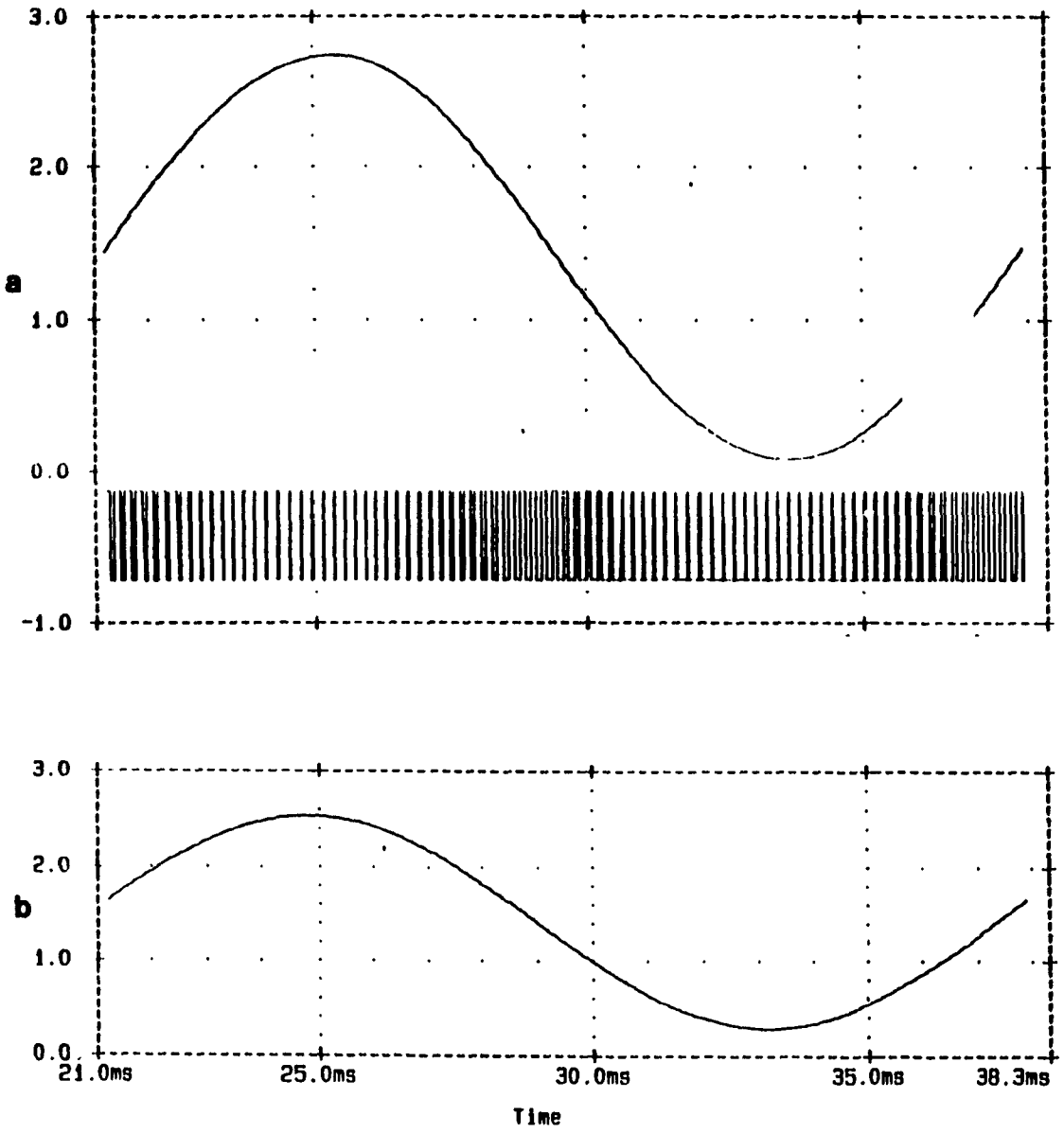

Fig. 4.5 Output voltage for the inverter with the proposed control technique.

a) With voltage loop.

b) Without voltage loop.

(V_{in} = 2.828 pu, X_L = 0.37 pu, X_{C1} = 3.54 pu, R_{Load} = 1 pu).

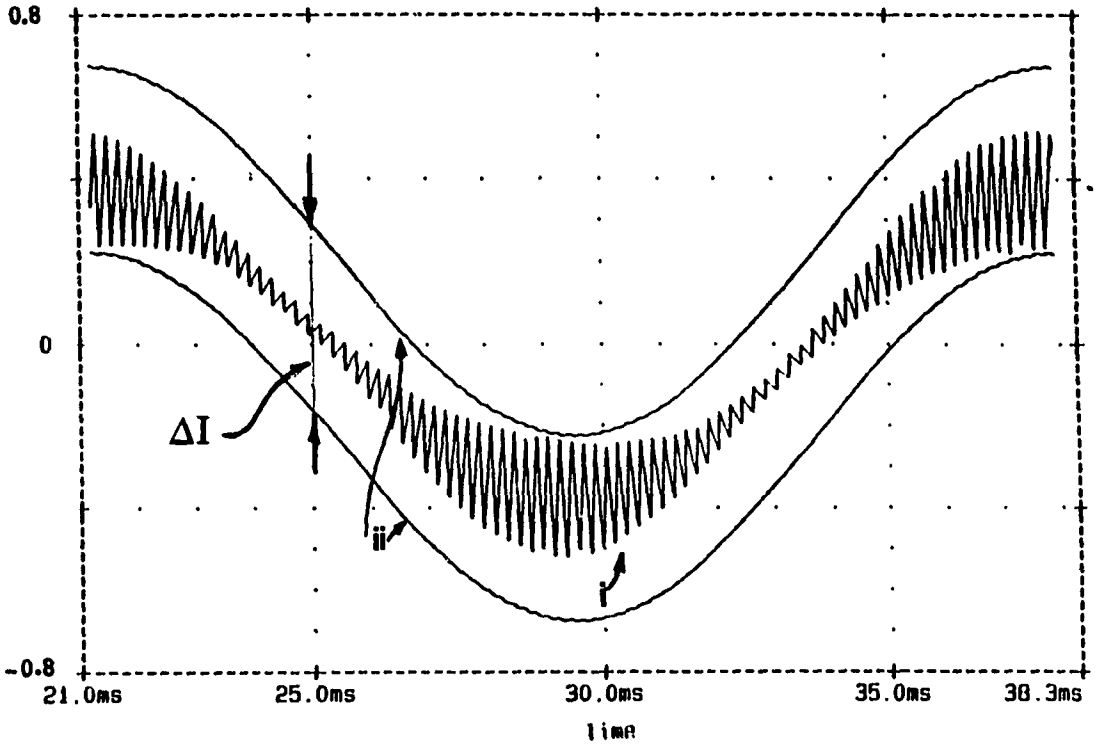

Fig. 4.6 (i) Capacitor current.

(ii) Imaginary hysteresis window.

(ΔI = 0.45 pu)

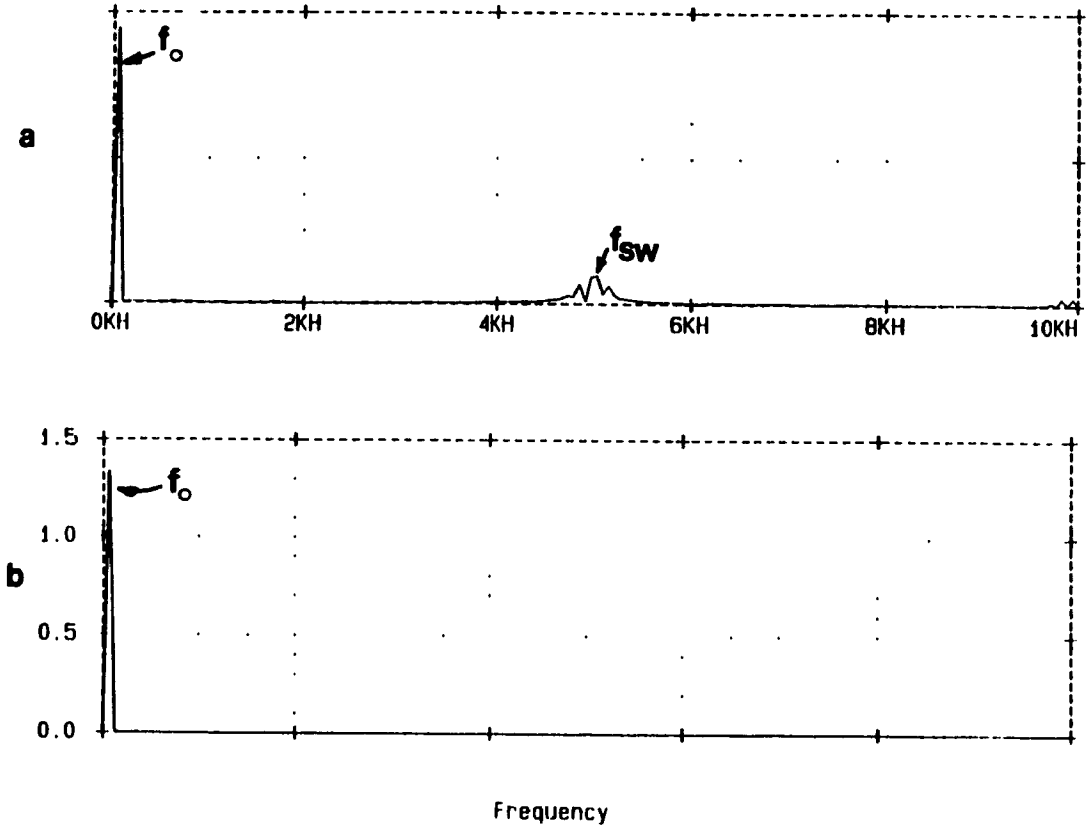

Fig. 4.7 a) Frequency spectrum of the capacitor current.

b) Frequency spectrum of the output voltage.

(f_o = fundamental component, f_{sw} = switching frequency)

4.2.1.3. Predictive method

The previously designed inverter is controlled by the predictive method and the following results are obtained. The reference current and the capacitor actual current are shown in Fig. 4.8. Fig. 4.8 indicates that the reference current always remains at the center of the actual current since the necessary switching instants are calculated. The predictive method shows great sensitivity to the changes in the component values and also to the variations of dc input voltage. One solution to this problem can be the use of the external voltage loop which in turn will add to the complexity of the control scheme. The output voltage for a 1 pu resistive load is shown in Fig. 4.9. Fig. 4.10 illustrates the change in the shape of the output voltage due to 2 percent variation in the input dc voltage. As it can be seen, by increasing the input dc voltage to 2.848 pu the output voltage is significantly distorted.

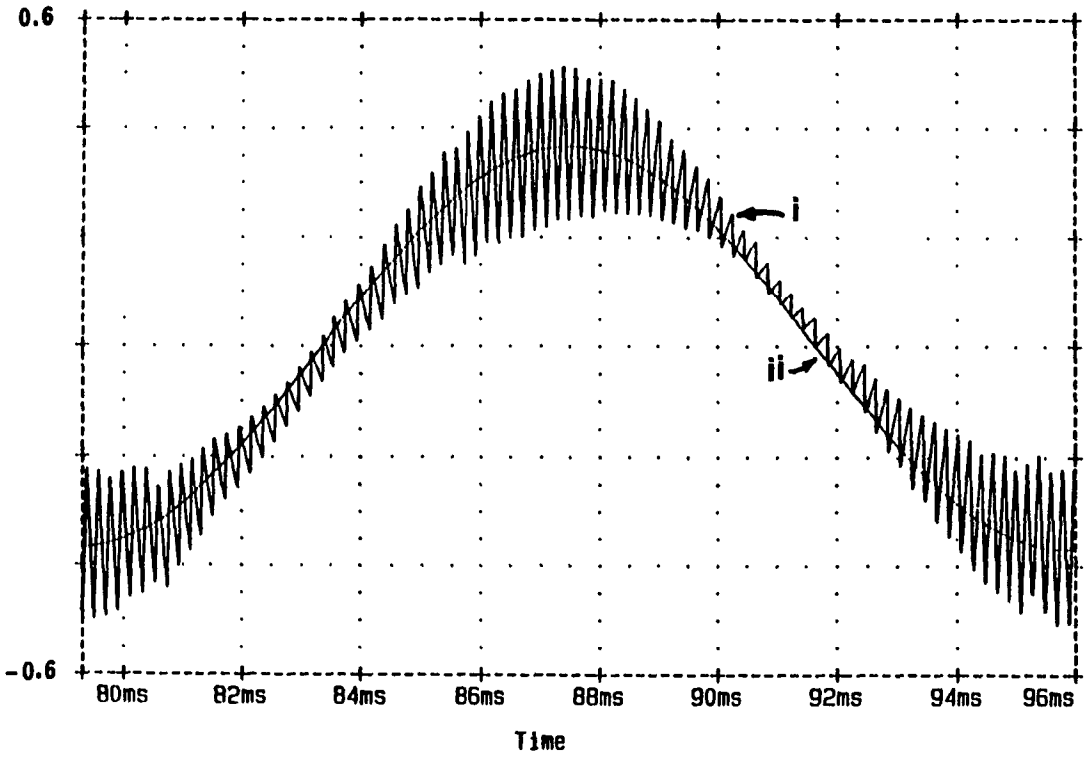

Fig. 4.8 Proposed inverter with the predictive controller.

(i) Capacitor current.

(ii) Reference current waveform.

(V_{In} = 2.828 pu, R_{Load} = 1 pu).

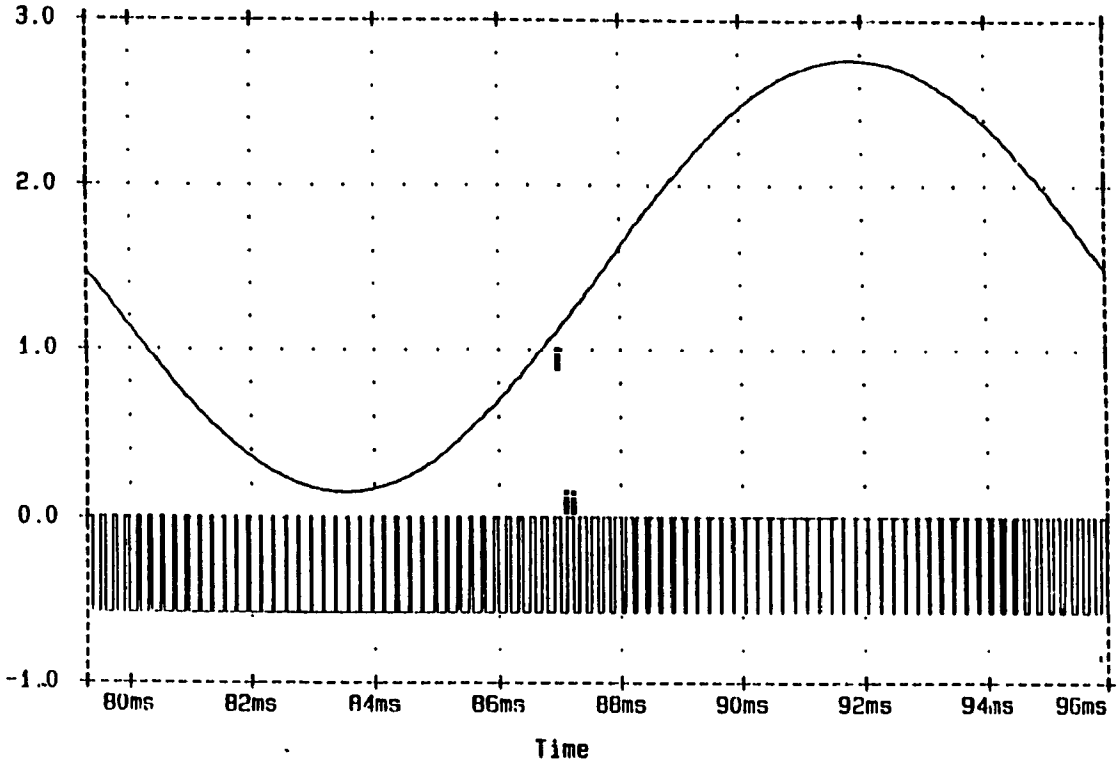

Fig. 4.9 Predictive controller.

(i) Output voltage.

(ii) Gating signals.

(V_{in} = 2.828 pu, R_{Load} = 1 pu).

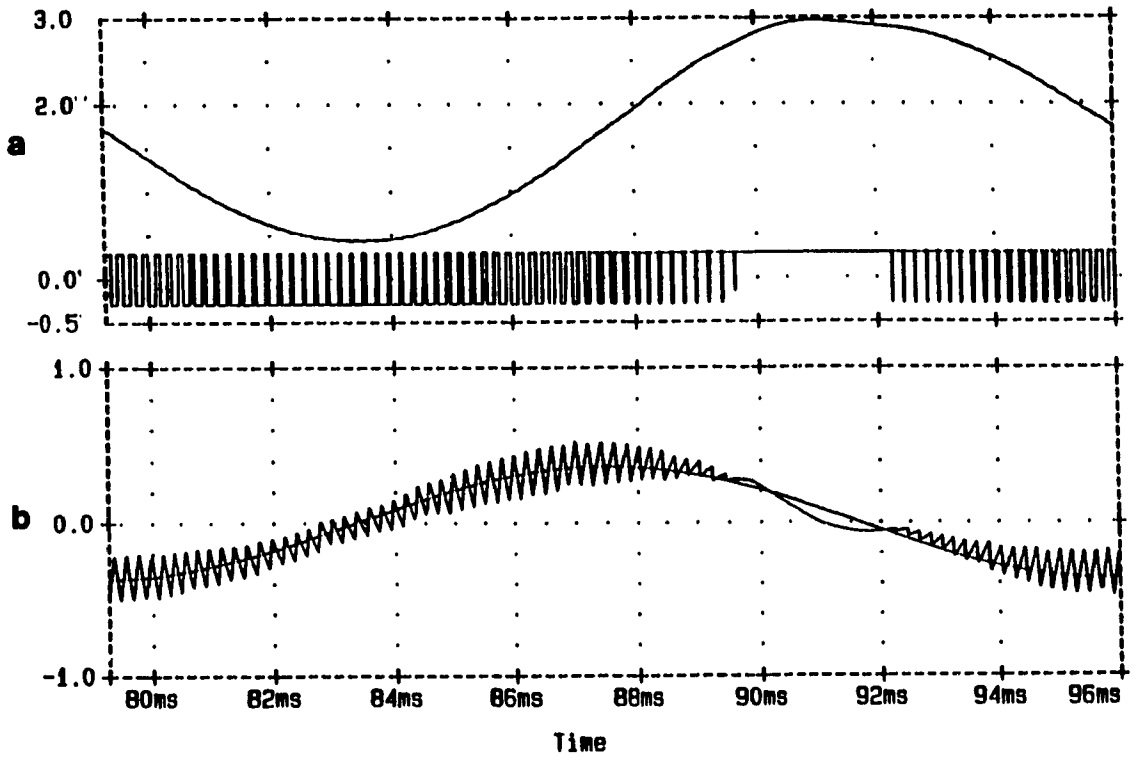

Fig. 4.10 Predictive controller.

a) Output voltage.

b) Actual capacitor current.

(V_{in} = 2.884 pu, R_{Load} = 1 pu).

4.2.2 Nonlinear load

An LC filter fed through a bridge rectifier (Fig. 4.11) is used as a nonlinear load. The following specification are chosen for the nonlinear load:

$$C = 2000\ \mu F,\ X_C = 0.265\ pu$$

$$R = 50\ \Omega,\ R = 10\ pu$$

$$L = 0.005\ H,\ X_L = 0.37\ pu$$

Figure 4.12 shows that excellent output voltage waveform is obtained even with a nonlinear load. This is confirmed by the frequency spectrum of the output voltage, which is almost identical to the linear case, (Fig. 4.13).

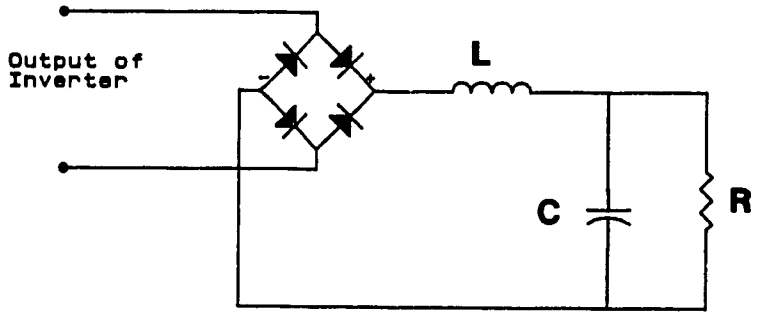

Fig. 4.11 Nonlinear load. (X_L = 0.37 pu, X_C = 0.265 pu, R = 10 pu)

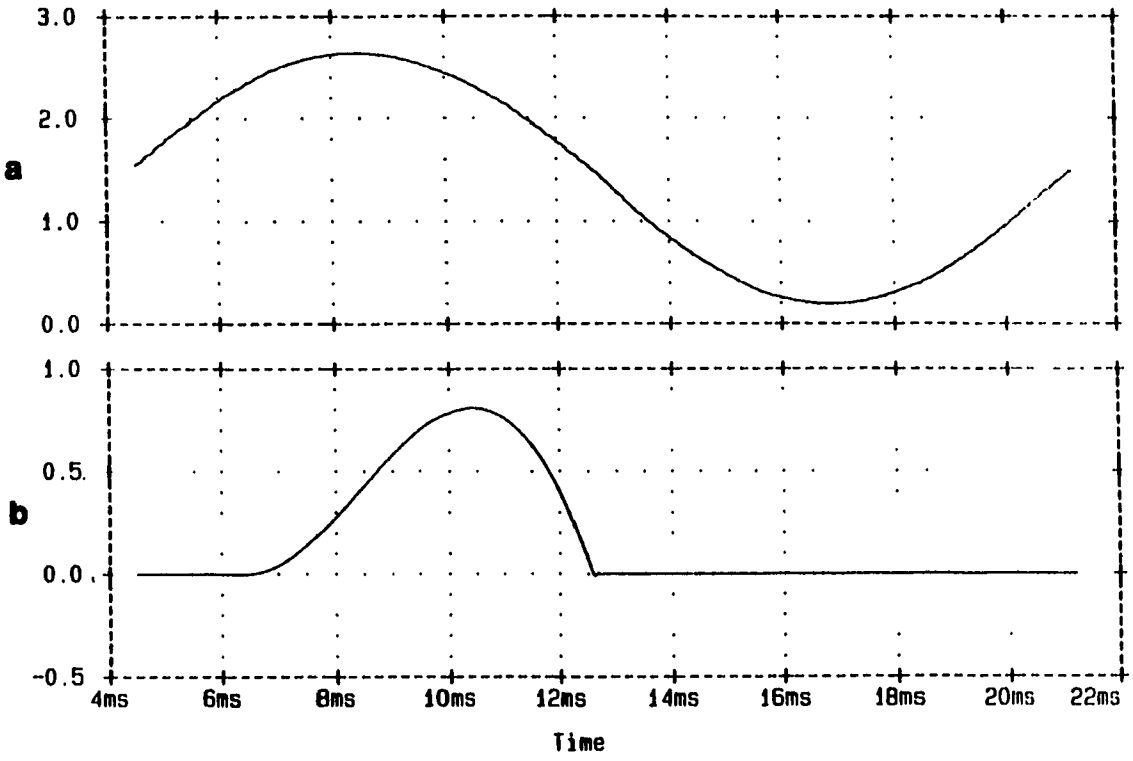

Fig. 4.12 Nonlinear load.

(a) Output voltage.

(b) Load current.

(V_{in} = 2.828 pu).

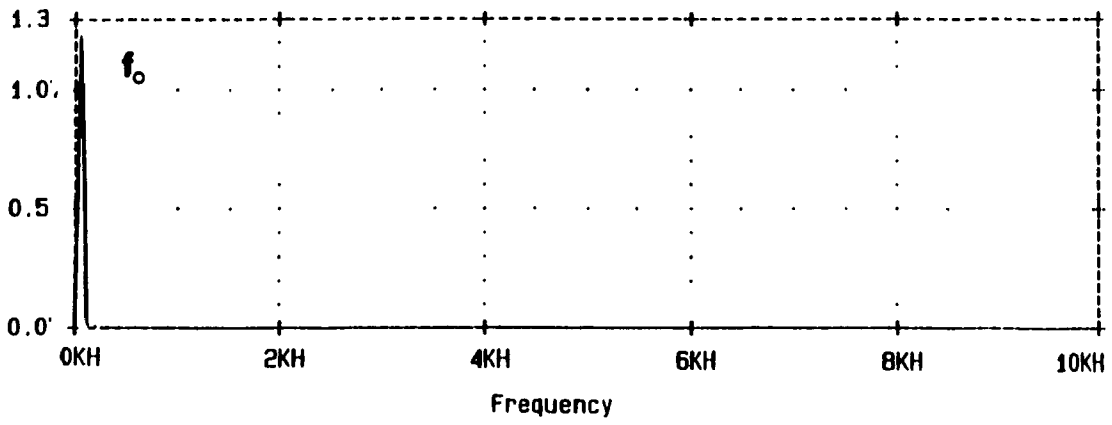

Fig. 4.13 Frequency spectrum of the output voltage.

(f_o = fundamental component, f_{sw} = switching frequency).

4.2.3 Load transients

A step change in the load impedance from 2 pu to 1 pu has been considered to illustrate the speed of the response of the proposed technique to the load transients. The response to sudden change in the load is very fast with only a small voltage dip as shown in Fig. 4.14. The switching pattern returns to normal after 2 switching periods (0.4 ms).

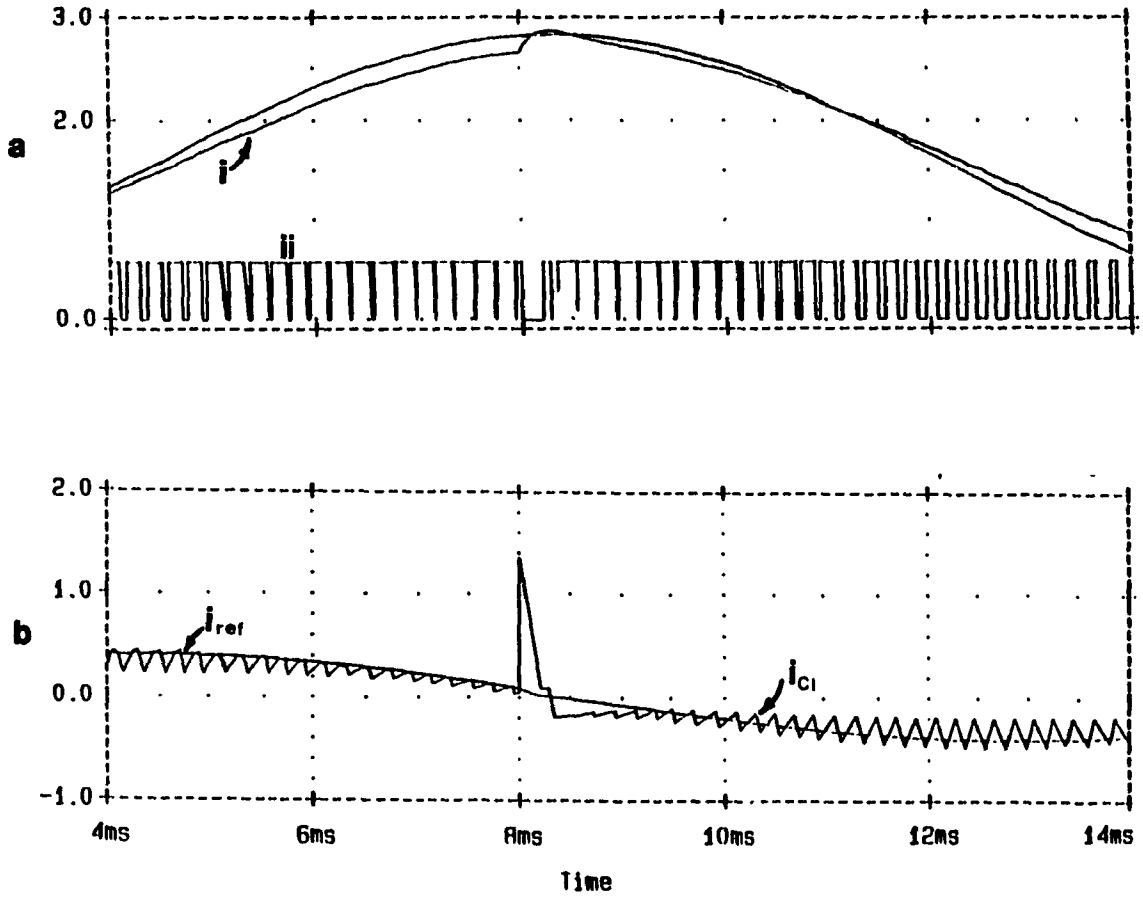

Fig. 4.14 Step change in the load.

a) (i) Output voltage. (ii) Gating signals.

b) Capacitor current.

(resistive load changes from 2 pu to 1 pu, V_{ln} = 2.828 pu)

4.3 Conclusions

The dc/ac current regulated converter module has been simulated by SPICE program and the transient and steady state responses have been presented. Three different types of current control methods have been implemented with the proposed inverter to supply a resistive load and the output results compared. From this comparison the following results are obtained:

- The hysteresis controller suffers from varying switching frequency. Also, the average and the maximum switching frequency are very high. By increasing the size of the hysteresis window, the average switching frequency can be decreased but the output voltage will be distorted.

- The proposed current control technique exhibits a simple control with constant switching frequency. The use of the voltage loop is not necessary, however, implementing this loop will increase the voltage gain of the inverter to a value close to one. The error triangulation technique provides a fast response to load transients. The simulation results also confirm the capability of the proposed converter module of supplying nonlinear loads without any distortion in the inverter output voltage.

- The predictive controller requires a complicated circuitry. This technique suffers from high parameter sensitivity which makes it very hard to implement.

CHAPTER 5

EXPERIMENTAL RESULTS

5.1 Introduction

The design procedure and the simulation results are experimentally verified in this section. Only the error triangulation technique is implemented in a single phase system and the results are presented next. Two types of load are considered: resistive and nonlinear loads.

5.2 Experimental set up

A 250 VA converter using the specifications given in the design example was set up in the laboratory. A hall effect sensor was used to sense the capacitor current. The external voltage loop has not been implemented since for the single phase inverter it is not necessary. The layout of the inverter set up is given in the appendix of the thesis. Since only the ac component of the capacitor current is controlled, the existing dc offset of the current reference produces a drift in the output voltage. This voltage drift will be removed if the voltage loop is used.

5.3 Experimental Results

An ideal sinusoidal output voltage is obtained for a 1 pu resistive load which is shown in Fig. 5.1. Comparison of experimental (Fig. 5.1) and predicted (Fig. 4.1) results shows that hey are in close agreement. In order to examine the effect of nonlinear loads, an LC filter fed by a bridge rectifier is used as a typical nonlinear load. The output voltage and the load current are shown in Fig. 5.2, which also confirm the simulation

results. This figure indicates that the output voltage distortion is minimized by controlling the capacitor current with the error triangulation technique.

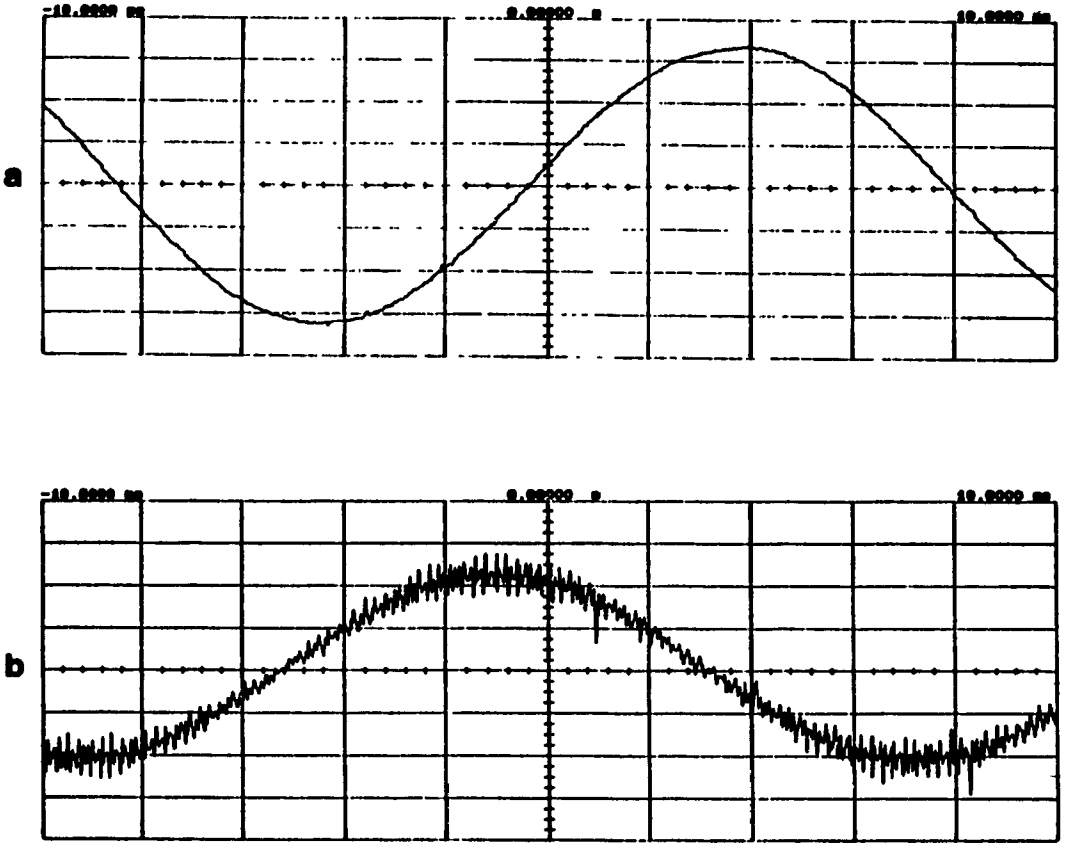

Fig. 5.1 Experimental results for linear load.

a) Output voltage (10 V/div).

b) Capacitor current (1 A/div).

(R_{Load} = 1 pu, V_{in} = 2.828 pu, X_L = 0.37 pu, X_{C1} = 3.54 pu).

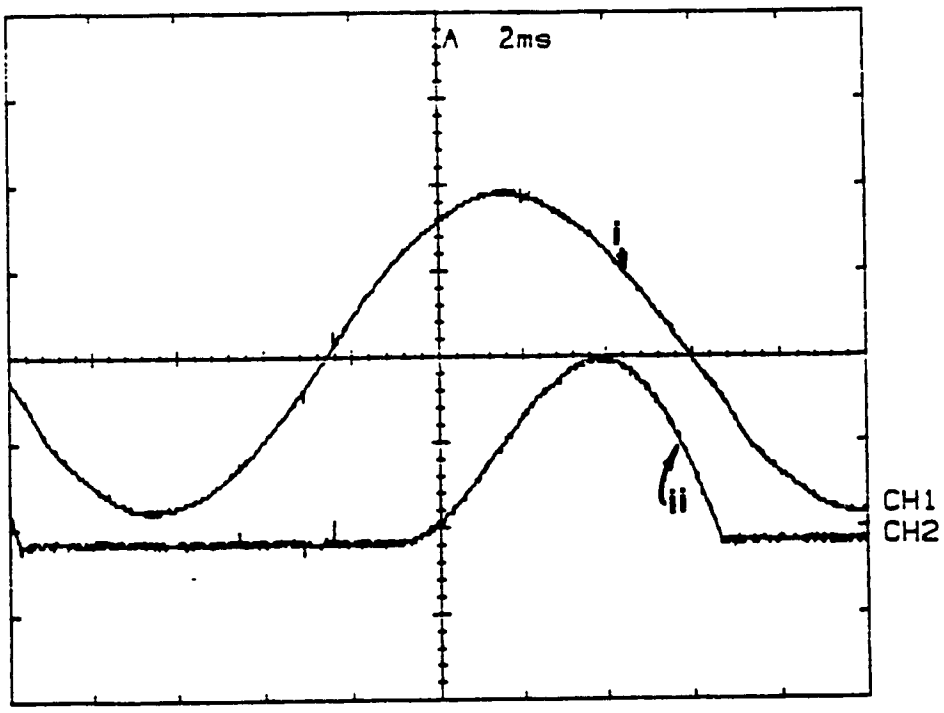

Fig. 5.2 Experimental results for nonlinear load.

(i) Output voltage (20 V/div).

(ii) Load current (2 A/div).

(R_{Load} = 10 pu, X_L = 0.37 pu, V_{in} = 2.828 pu, X_C = 0.265 pu)

5.4 Conclusions

The simulation results and feasibility of the proposed converter module are verified by experimental results.

- The proposed converter module provides high quality sinusoidal output voltage even without using the voltage loop. However, adding the voltage loop will eliminate the existing drift of the output voltage and will improve the voltage gain of the inverter.

- A high quality sinusoidal voltage is obtained while a typical nonlinear load is supplied.

CHAPTER 6

THREE PHASE SYSTEM IMPLEMENTATION

6.1 Introduction

The three phase implementation of the proposed inverter and control technique is easily obtainable. Three blocks of the proposed current module are connected together to build a three phase system (Fig. 6.1).

In order to obtain the three phase balanced output voltages, the current and voltage reference waveforms should be properly phase shifted. These current and voltage references are calculated in the following sections. The voltage gain of the three phase system is further increased by subtracting the third harmonic currents from the phase current references. The analysis and design procedure for the three phase system is the same as single phase module. However, component ratings are calculated to indicate the effect of the injected third harmonic currents.

6.2 Reference Waveforms

In order to implement the proposed method in a three phase system, the three current references should be phase shifted by 120 degrees with respect to each other (Fig. 6.1). The reference waveforms for the external voltage loop should be also phase shifted. By injecting the 3rd harmonics into the current references, the gain of the system can be further increased. Using the optimum values for 3rd harmonic voltage injection, the optimum values of the injected currents are obtained.

With a typical sinusoidal reference current:

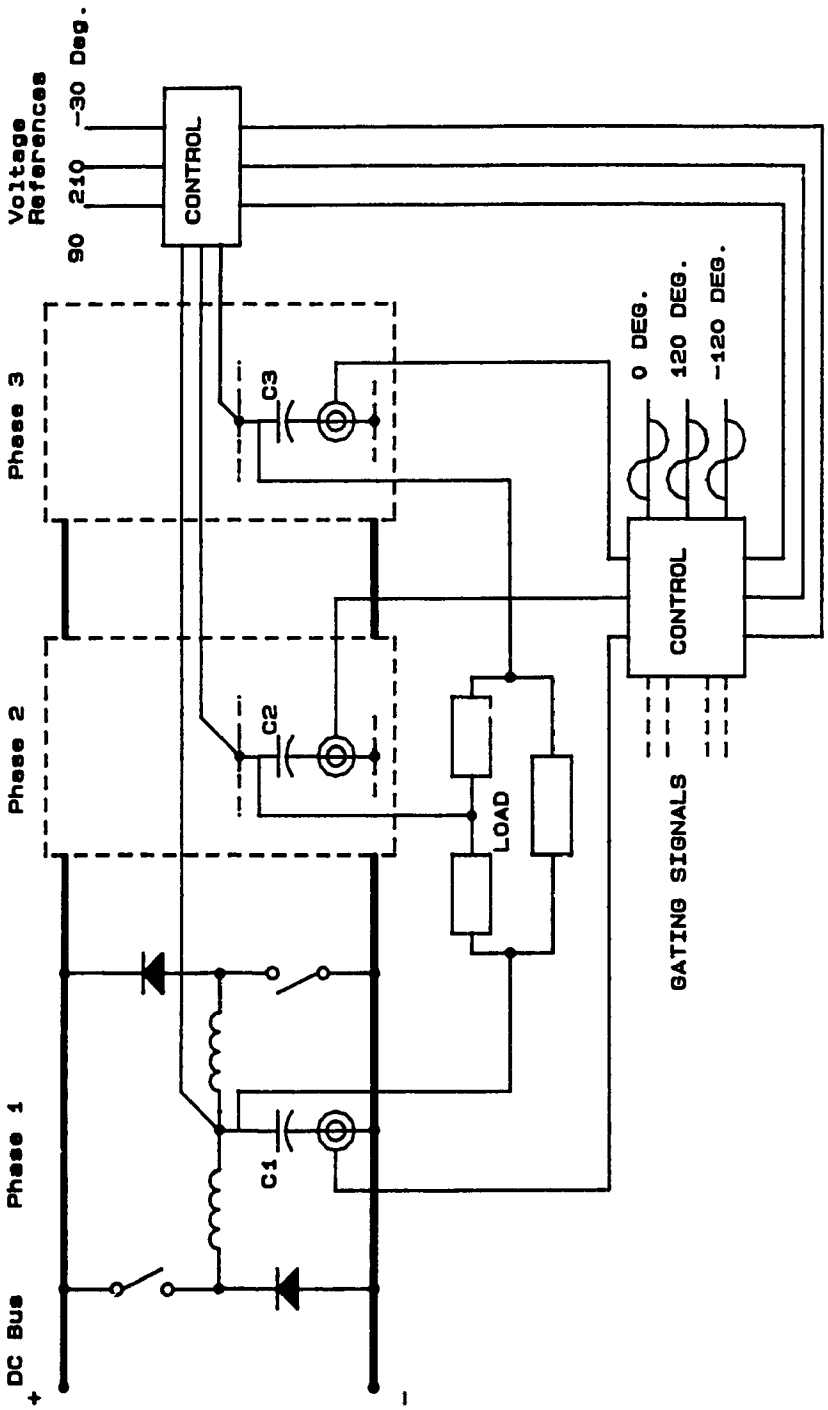

Fig. 6.1 Three phase implementation of the proposed current regulated inverter.

$$i(t) = I_p \sin \omega t$$

Neglecting the dc offset of the output voltage, the capacitor voltage will be:

$$v(t) = V_p \sin (\omega t + \frac{\pi}{2})$$

where:

$$V_p = X_{C1} I_p$$

Injecting the optimized 3rd harmonic voltages into the phase voltage gives:

$$v_{ph}(t) = 1.17V_p \sin (\omega t + \frac{\pi}{2}) + 0.19V_p \sin 3(\omega t + \frac{\pi}{2})$$

$$= -1.17V_p \cos (\omega t) + 0.19V_p \cos (3\omega t) \qquad (6.1)$$

Taking the derivative of the voltage to obtain the reference current yields:

$$i_{ref}(t) = 1.17I_p \sin (\omega t) - 0.57I_p \sin (3\omega t) \qquad (6.2)$$

The reference current and the reference voltage for phase one are shown in Fig. 6.2. Frequency spectrum of the reference voltage is also shown in Fig. 6.3 which illustrates the added third harmonic voltage.

Now, by using Eqn. (6.2) as the reference current, replacing I_p by its equivalent $(V_{in}\omega C_1)/2$, and adding the dc offset $V_{in}/2$, the reference current, the actual output voltage and the load current are calculated:

$$i_{ref}(t) = \frac{1.17\ V_{in}\omega\ C_1}{2} \sin \omega t - \frac{0.57\ V_{in}\omega\ C_1}{2} \sin (3\omega t) \qquad (6.3)$$

$$V_o(t) = V_{ref}(t) = -\frac{1.17\ V_{in}}{2}\cos\omega t + \frac{0.19\ V_{in}}{2}\cos(3\omega t) + \frac{V_{in}}{2} \tag{6.4}$$

$$i_o(t) = -\frac{1.17\ V_{in}}{2R}\cos\omega t + \frac{0.19\ V_{in}}{2R}\cos(3\omega t) + \frac{V_{in}}{2R} \tag{6.5}$$

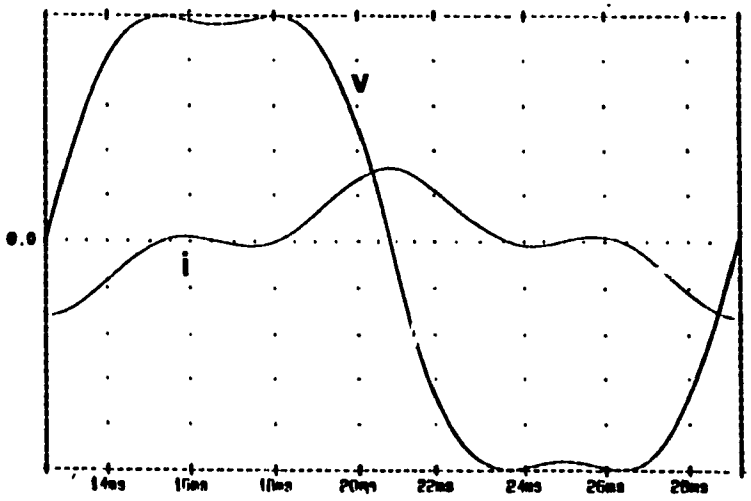

Fig. 6.2 Current and voltage waveform references.

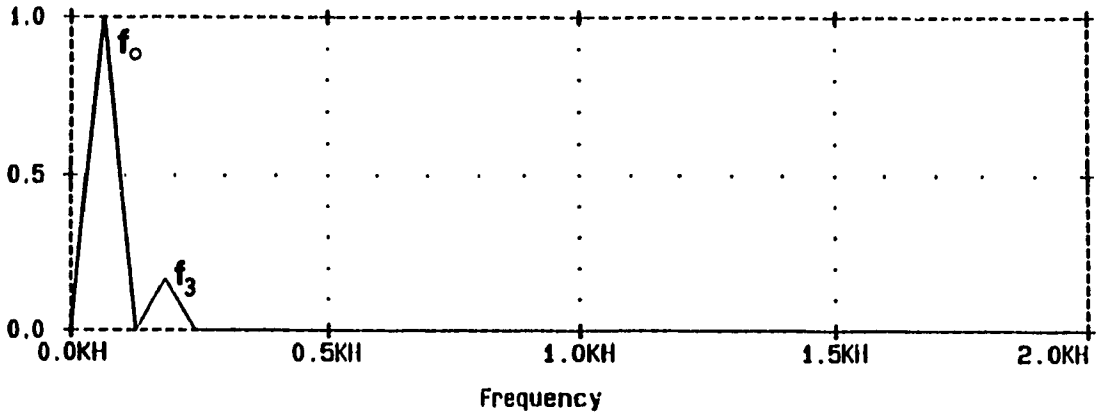

Fig. 6.3 The frequency spectrum of the phase voltage reference. (f_o = the fundamental component, f_3 = the injected third harmonic component).

6.3 Analysis and Design

The analysis and design procedure for the three phase system are similar to those of the single phase inverter. Only the current and voltage reference waveforms are phase shifted. The magnitude of the dc offset produced in the three phases depends on the phase shift of the output voltage. Therefore, in order to obtain the three balanced output voltage, use of an external voltage becomes necessary.

The inductor currents can be calculated using the equations derived in chapter two. From Eqn. (2.3):

$$i_{L1}(t) - i_{L2}(t) = i_{C1}(t) + i_{load}(t)$$

which will yield:

$$i_{L1}(t) - i_{L2}(t) = -\frac{1.17\ V_{in}}{2R}\cos\omega t + \frac{0.19\ V_{in}}{2R}\cos(3\omega t) + \frac{V_{in}}{2R} + \frac{1.17\ V_{in}\omega\ C_1}{2}\sin\omega t - \frac{0.57\ V_{in}\ \omega\ C_1}{2}\sin(3\omega t) \tag{6.6}$$

Also by using the same initial value as in Eqn. (2.22) for the inductor currents:

$$i_{L1}(t) + i_{L2}(t) = \frac{V_{in}}{R} \tag{6.7}$$

Solving Eqns. (6.6) and (6.7), the inductor currents are found to be:

$$i_{L1}(t) = -\frac{1.17\ V_{in}}{4R}\cos\omega t + \frac{0.19\ V_{in}}{4R}\cos(3\omega t) + \frac{3\ V_{in}}{4R} + \frac{1.17\ V_{in}\omega\ C_1}{4}\sin\omega t - \frac{0.57\ V_{in}\ \omega\ C_1}{4}\sin(3\omega t) \tag{6.8}$$

$$i_{L2}(t) = \frac{1.17\ V_{in}}{4R} \cos \omega t - \frac{0.19\ V_{in}}{4R} \cos (3\omega t) + \frac{V_{in}}{4R} - \frac{1.17\ V_{in}\ \omega\ C_1}{4} \sin \omega t + \frac{0.57\ V_{in}\ \omega\ C_1}{4} \sin (3\omega t) \quad (6.9)$$

The inductor currents are shown in Fig. 6.4.

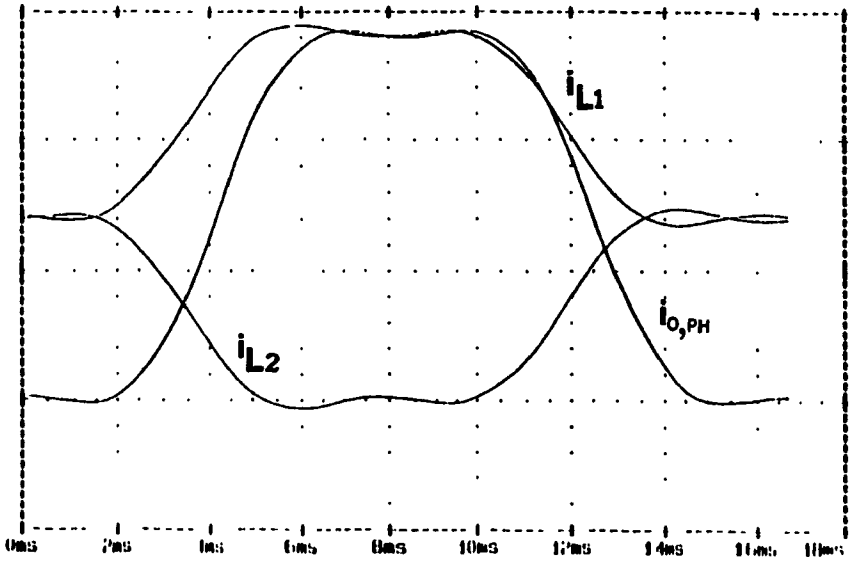

Fig. 6.4 Inductor currents.

Injecting the third harmonic into the current reference will change the switching function (d) of the inverter. By substituting the steady state output voltage, Eqn. (6.4) and its first and second derivative in Eqns. (2.9), (2.10), the new average on-time and off-time of the top switch (S_1) can be calculated. Assuming ($L_1 = L_2 = L$, $A = L/2$):

$$V_{in}D = \frac{1.17\ V_{in}\ LC_1\omega^2}{4} \cos \omega t - \frac{1.71\ V_{in}\ LC_1\omega^2}{4} \cos (3\omega t) + \frac{1.17\ V_{in}\ L\omega}{4R} \sin \omega t + \frac{0.57\ V_{in}\ L\omega}{4R} \sin (3\omega t) - \frac{1.17\ V_{in}}{2} \cos\omega t + \frac{0.19\ V_{in}}{2} \cos (3\omega t) + \frac{V_{in}}{2} \quad (6.10)$$

The above equation can be rewritten as:

$$D = (0.2925\ LC_1\omega^2 - 0.585)\cos\omega t + (0.095 - 0.4275\ LC_1\omega^2)\cos(3\omega t) + \frac{0.2925\ L\omega}{R}\sin\omega t + \frac{0.1425\ L\omega}{R} + 0.5 \qquad (6.11)$$

Also $$D' = 1 - D$$

6.4 Component Ratings

The device ratings are changed due to the injection of the third harmonic current. In order to obtain 1 pu line current, the load resistor should be changed to:

$$R_{ph,Load} = 1 \times 3 = 3 \text{ pu}$$

The other per unit values are equal to those chosen for the single phase inverter:

$$I_{o,ph} = 0.333 \text{ pu}$$

$$V_{o,ph} = 1 \text{ pu}$$

$$S_{o,3ph} = 3 \times 0.333 \times 1 = 1 \text{ pu}$$

$$V_{in} = 2.828 \text{ pu}$$

$$X_{C1} = 3.54 \text{ pu}$$

$$X_L = 0.377 \text{ pu}$$

In the following sub-sections, the device ratings are calculated first for sinusoidal reference waveform and then considering the effect of third harmonic current injection.

6.4.1 Capacitor ratings

The capacitor current is given by Eqn. (6.3). The peak and rms value of the capacitor current are calculated as follows.

$$I_{C1,3ph,peak} = \frac{1.17 \times 2.828 \times 0.283}{2} + \frac{0.57 \times 2.828 \times 0.283}{2} = 0.696 \text{ pu}$$

$$I_{C1,3ph,rms} = \sqrt{\frac{1}{T}\int_0^t i_{C1}^2 \, dt} = 0.368 \text{ pu}$$

$$V_{C1,3ph,peak} = \frac{1.17 - 0.19 + 1}{2} \times 2.828 = 2.8 \text{ pu}$$

$$V_{C1,3ph,rms} = \sqrt{\frac{1}{T}\int_0^t v_{C1}^2 \, dt} = 1.845 \text{ pu}$$

If the third harmonic currents are not injected, the current ratings of the capacitor will be:

$$I_{C1,3ph,peak} = 0.4 \text{ pu}$$

$$I_{C1,3ph,rms} = 0.283 \text{ pu}$$

6.4.2 Inductor ratings

The inductor peak current is calculated using Eqns. (6.8) and (6.9). For inductor L_1 substituting the per unit values of the input voltage and the capacitor current yeilds:

$$I_{L1,3ph,peak} = \sqrt{\left(\frac{0.98 \times 2.828}{12}\right)^2 + \left(\frac{1.74 \times 2.828 \times 0.283}{4}\right)^2} + \frac{3 \times 2.828}{12} = 1.125 \text{ pu}$$

The inductor (L_1) rms current is:

$$I_{L1,3ph,rms} = \sqrt{\frac{1}{T}\int_0^t i_{L1}^2 \, dt} = 0.757 \text{ pu}$$

Also:

$$V_{L1,3ph,peak} = V_{o,3ph,peak} = 2.8 \text{ pu}$$

Following a similar procedure the following results are obtained for inductor L_2:

$$I_{L2,3ph,peak} = 0.654 \text{ pu}$$

$$I_{L2,3ph,rms} = \sqrt{\frac{1}{T}\int_0^T i_{L2}^2 \, dt} = 0.359 \text{ pu}$$

$$V_{L2,3ph,peak} = V_{o,3ph,peak} = 2.8 \text{ pu}$$

Without injecting the third harmonic currents, the current ratings are:

$$I_{L1,3ph,peak} = 1.016 \text{ pu}$$

$$I_{L1,3ph,rms} = 0.735 \text{ pu}$$

$$I_{L2,3ph,peak} = 0.545 \text{ pu}$$

$$I_{L2,3ph,rms} = 0.321 \text{ pu}$$

6.4.3 Diodes ratings

The peak current in the diode D_1 is as high as the inductor (L_2) peak current:

$$I_{D1,3ph,peak} = I_{L2,3ph,peak} = 0.654 \text{ pu}$$

Also the peak current in D_2 is:

$$I_{D2,3ph,peak} = I_{L1,3ph,peak} = 1.125 \text{ p.u}$$

The average and rms values of (i_{D1} ,i_{D2}) are found using Eqns. (2.30):

$$I_{D1,3ph,ave} = \frac{1}{T}\int_0^T D\, i_{L2} \, dt$$

$$I_{D1,3ph,rms} = \sqrt{\frac{1}{T}\int_0^T (D\, i_{L2})^2 \, dt}$$

$$I_{D2,3ph,ave} = \frac{1}{T}\int_0^T D' i_{L1}\, dt$$

$$I_{D2,3ph,rms} = \sqrt{\frac{1}{T}\int_0^T (D' i_{L1})^2\, dt}$$

Using the above equations, the diodes ratings are:

$$I_{D1,3ph,ave} = 0.037 \text{ pu}$$

$$I_{D1,3ph,rms} = 0.112 \text{ pu}$$

$$I_{D2,3ph,ave} = 0.273 \text{ pu}$$

$$I_{D2,3ph,rms} = 0.341 \text{ pu}$$

The maximum reverse voltage across the diodes will be:

$$V_{D1,3ph,rev} = V_{ln} = 2 \times 1.414 = 2.828 \text{ pu}$$

$$V_{D2,3ph,rev} = V_{ln} = 2 \times 1.414 = 2.828 \text{ pu}$$

The diodes current ratings for a sinusoidal reference waveform are:

$$I_{D1,3ph,peak} = I_{L2,3ph,peak} = 0.545 \text{ pu}$$

$$I_{D2,3ph,peak} = I_{L1,3ph,peak} = 1.016 \text{ pu}$$

$$I_{D1,3ph,ave} = 0.059 \text{ pu}$$

$$I_{D1,3ph,rms} = 0.1 \text{ pu}$$

$$I_{D2,3ph,ave} = 0.295 \text{ pu}$$

$$I_{D2,3ph,rms} = 0.340 \text{ pu}$$

6.4.4 Switch ratings

Switch ratings are found by following the same procedure as diodes. Switch S_1 experiences the same peak current as diode D_2 while switch S_2 experiences the peak current of diode D_1.

$$I_{sw1,3ph,peak} = I_{D2,3ph,peak} = 1.125 \text{ pu}$$

$$I_{sw2,3ph,peak} = I_{D1,3ph,peak} = 0.654 \text{ pu}$$

Writing equations similar to those obtained for the diodes and substituting i_{L1}, D, i_{L2}, D', the average and rms values for both switches are found:

$$I_{sw1,3ph,ave} = 0.434 \text{ pu}$$

$$I_{sw1,3ph,rms} = 0.587 \text{ pu}$$

$$I_{sw2,3ph,ave} = 0.199 \text{ pu}$$

$$I_{sw2,3ph,rms} = 0.298 \text{ pu}$$

The maximum reverse voltage across the switches will be:

$$V_{sw1,3ph,rev} = V_{in} = 2 \times 1.414 = 2.828 \text{ pu}$$

$$V_{sw2,3ph,rev} = V_{in} = 2 \times 1.414 = 2.828 \text{ pu}$$

For a sinusoidal reference waveform these ratings will be changed to:

$$I_{sw1,3ph,peak} = I_{D2,3ph,peak} = 1.016 \text{ pu}$$

$$I_{sw2,3ph,peak} = I_{D1,3ph,peak} = 0.545 \text{ pu}$$

$$I_{sw1,3ph,ave} = 0.412 \text{ pu}$$

$$I_{sw1,3ph,rms} = 0.531 \text{ pu}$$

$$I_{sw2,3ph,ave} = 0.177 \text{ pu}$$

$$I_{sw2,3ph,rms} = 0.257 \text{ pu}$$

6.5 Simulation Results

A three phase system using three single phase dc/ac converter module is simulated by SPICE program. The component values and the input dc voltage remain unchanged. In order to obtain the same output ac kVA, the resistive load has to be changed to:

$$R_{ph,Load} = 3 \text{ pu}$$

The line to line output voltages for the three phase circuit are shown in Fig. 6.5. Increased voltage gain is achieved by injecting the 3rd harmonic currents to the 3-phase current references. Fig. 6.6(a) shows the output phase voltages. From the harmonic spectrum of the voltage of phase one (Fig. 6.6(b)), it can be seen that there is a 15% increase in the fundamental component. If the external voltage loop is not used, the dc offset produced in the output phase voltages will be different, which will result in unbalanced output voltages. So, in the case of a three phase system, use of the voltage loop becomes a must.

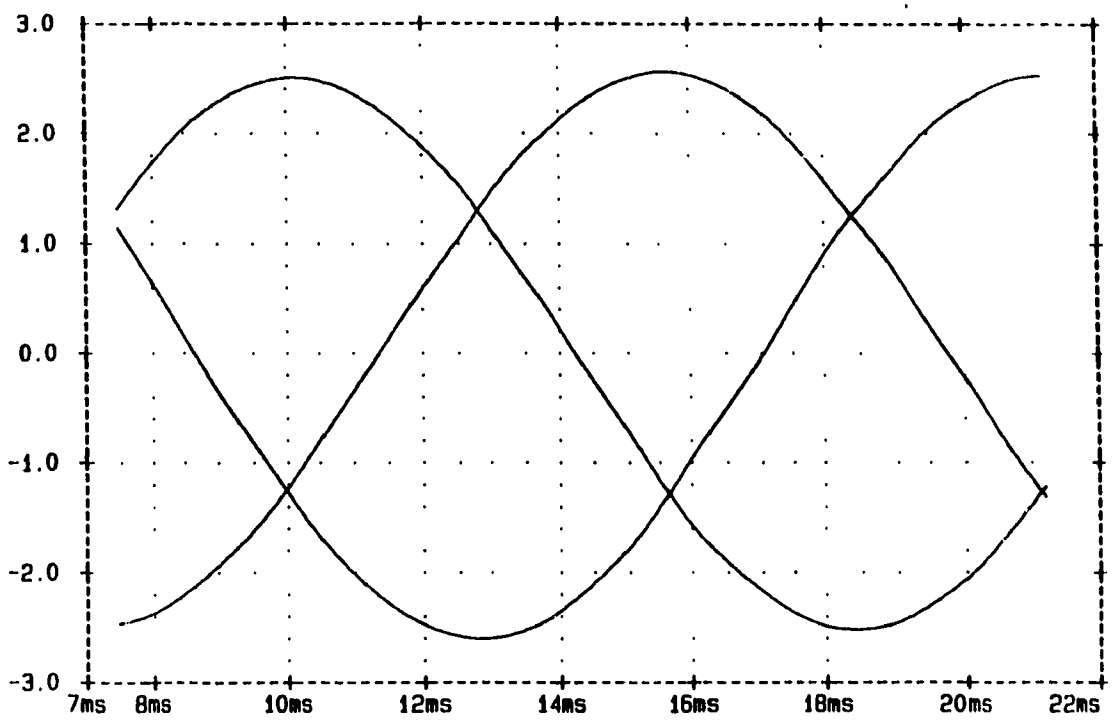

Fig. 6.5 Line to line output voltages in a three phase system.

(V_{in} = 2.828 pu, $R_{ph,Load}$ = 3 pu).

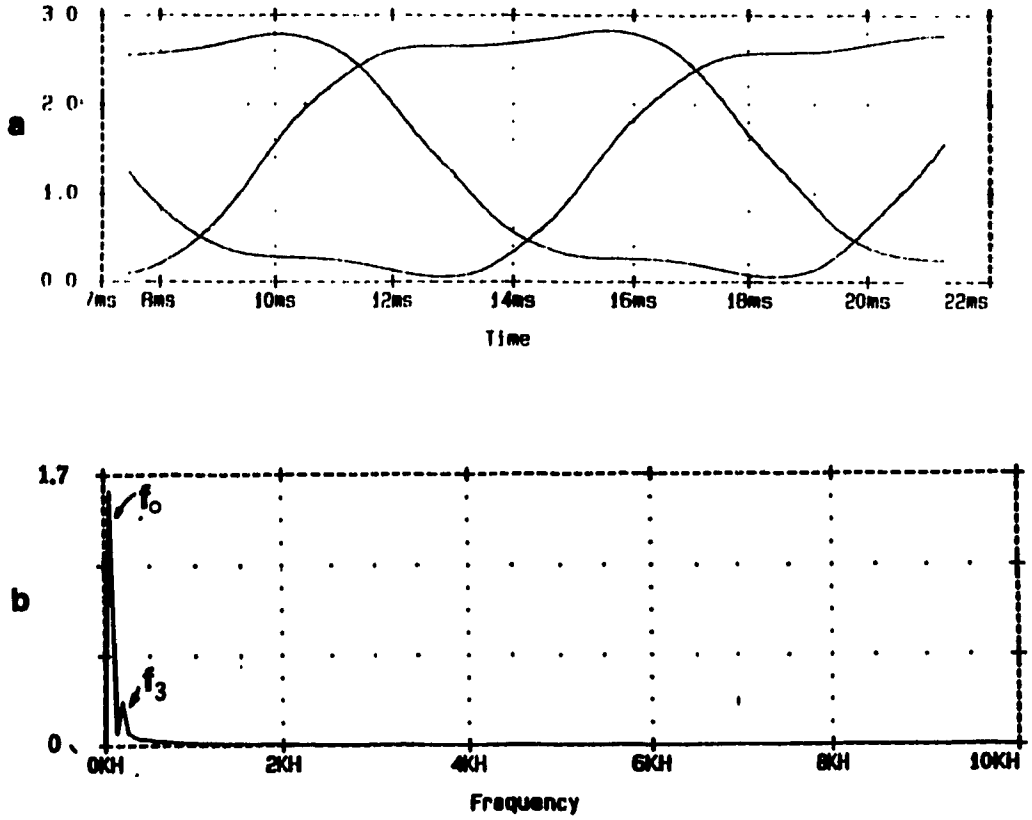

Fig. 6.6 a) Phase output voltages. b) Frequency spectrum of phase voltage. (f_o = fundamental component, f_3 = third harmonic component, f_{sw} = switching frequency)

6.6 Conclusions

Three current regulated dc/ac converter modules are used to provide a three phase system. By analyzing the three phase system, the following results are concluded:

The three phase implementation of the proposed converter module and control technique is easily obtainable.

- The three phase implementation does not require any added circuitry and complexity, but use of the external voltage loop becomes necessary.

- The injection of third harmonic currents to the reference waveforms increases the output/input voltage gain of the inverter up to 15 percent.

- The third harmonic current injection results in device current deratings of almost 10 percent.

- Since the line to line output voltages do not have any dc offset the need of using a transformer in the output of the inverter is eliminated.

CHAPTER 7

SUMMARY AND CONCLUSIONS

7.1 Summary of the Thesis

The existing power circuit configurations of dc/ac converters were reviewed. Different waveshaping techniques and various dc/ac power circuit configurations were also presented in Chapter One. The chapter discussed the advantages of current control techniques over forward PWM techniques. Four main types of current controllers were presented and a brief evaluation was provided. Finally, a novel dc/ac converter with the associated current control technique was proposed.

In Chapter Two the proposed power circuit configuration was analyzed in details and the general scheme of current control technique was introduced. Device ratings for design purposes were provided.

Chapter Three contained the study and analysis of three different types of current controllers. A hysteresis controller, the error triangulation technique and a predictive controller were considered to provide the necessary output voltage waveshaping of the proposed inverter. The techniques were evaluated and the main advantages and disadvantages of each of the current controllers were brought out. The error triangulation technique proved to be the more suitable overall technique for the proposed converter configuration. This technique was studied in details and a design example was provided to complete the design of the combined converter and control technique.

The simulation results of the proposed converter with the different current control techniques were presented in Chapter Four and the theoretical results for the current controllers were confirmed. A typical nonlinear load was also simulated and the operation of the proposed converter and current control were obtained.

The single phase experimental evaluation of the propcsed method was presented in Chapter Five.

The three phase implementation of the proposed technique was discussed in Chapter Six and a method to increase the voltage gain of the inverter was explained. Component rating changes due to this increase of the voltage gain were also calculated. The three phase system was simulated and the output results were provided.

7.2 Conclusions

Dc/ac converter topologies together with the active waveshaping techniques have been investigated in the thesis and a novel power circuit topology presented. Different types of current control techniques have been discussed and three current controller studied in details. A comprehensive comparison between the proposed error triangulation technique, the predictive method and the well known hysteresis control method has been presented in chapter three and the advantages of triangulation method over the two other techniques have been brought out. The advantages of the proposed power circuit topology and current control technique confirmed by design, simulation and experimental results can be summarized as follows:

- The new power circuit configuration achieves high reliability through the use of one "diode-switch" combination on each leg of the inverter, which

eliminates shoot-through paths.

- Controlling the filter capacitor current has the advantage of maintaining high quality output voltage even with large ripple in the controlled current. The natural integration of the capacitor current which yields the output voltage, eliminates this current ripple and provides almost ideal sinusoidal output voltage.

- Low and constant switching frequency is achieved by means of using the error triangulation technique. This technique is robust and simple to implement.

- Nonlinear loads can be supplied from the proposed inverter without resulting in any distortion in the inverter output voltage. Since the capacitor voltage is not affected by the current drawn by the load.

- The method is easily applicable to a three phase system. Furthermore, the fundamental component of the line to line voltage can be increased by injection of third harmonic currents in the current references.

7.3 Suggestions for Future Work

- The use of the proposed converter topology can be extended to other applications such as uninterruptible power supplies.

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APPENDIX

The layout of the single phase inverter set up is shown in Fig. A.1. Three current reference waveforms and the triangular carrier are stored in a 16k EPROM. Only one sinusoidal output of the D/A is used as the reference current. This set up is readily applicable in a three phase system, since the same triangular waveform can be used for three different phases and the three reference currents are properly phase shifted. Fig. A.2 shows the EPROM and the associated logic circuit.

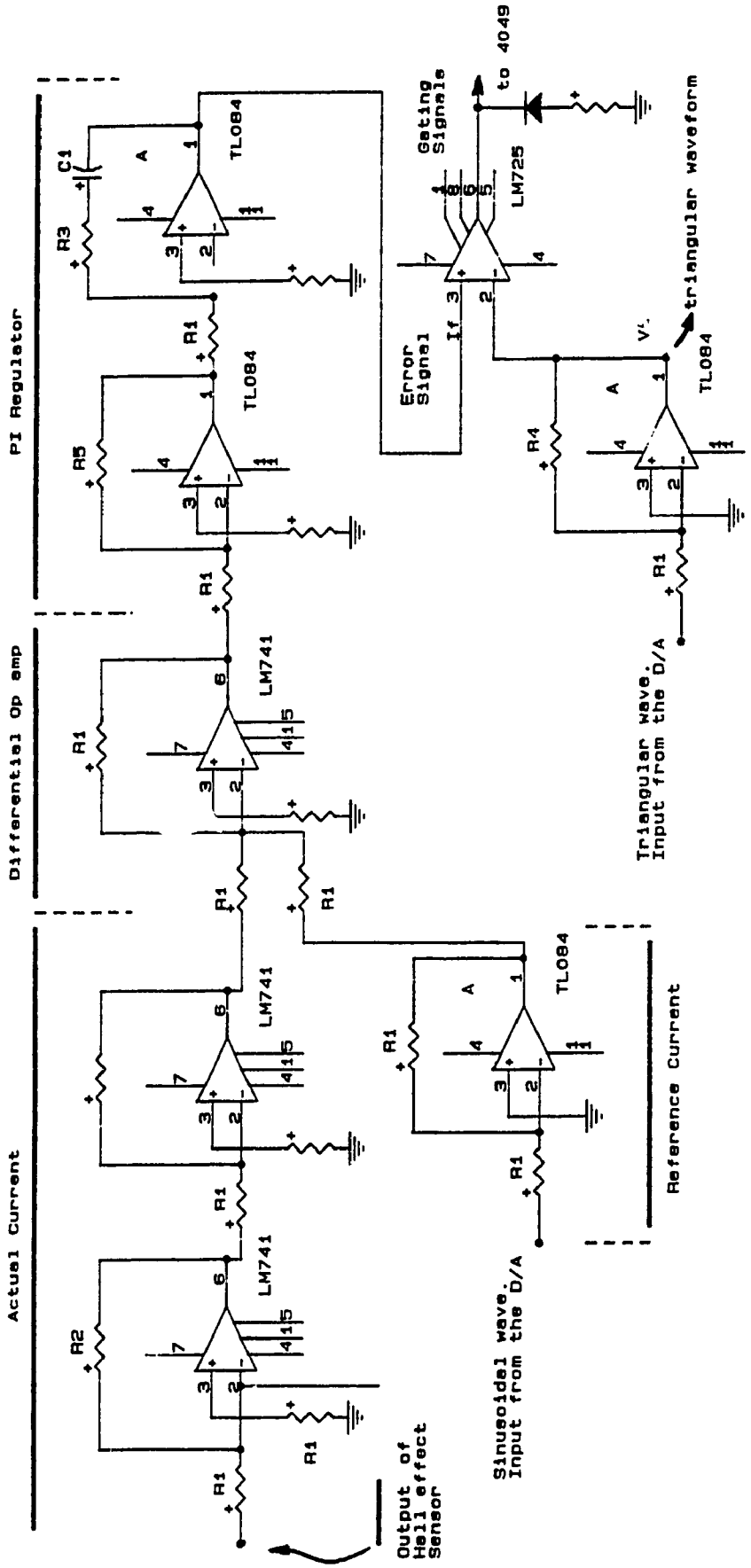
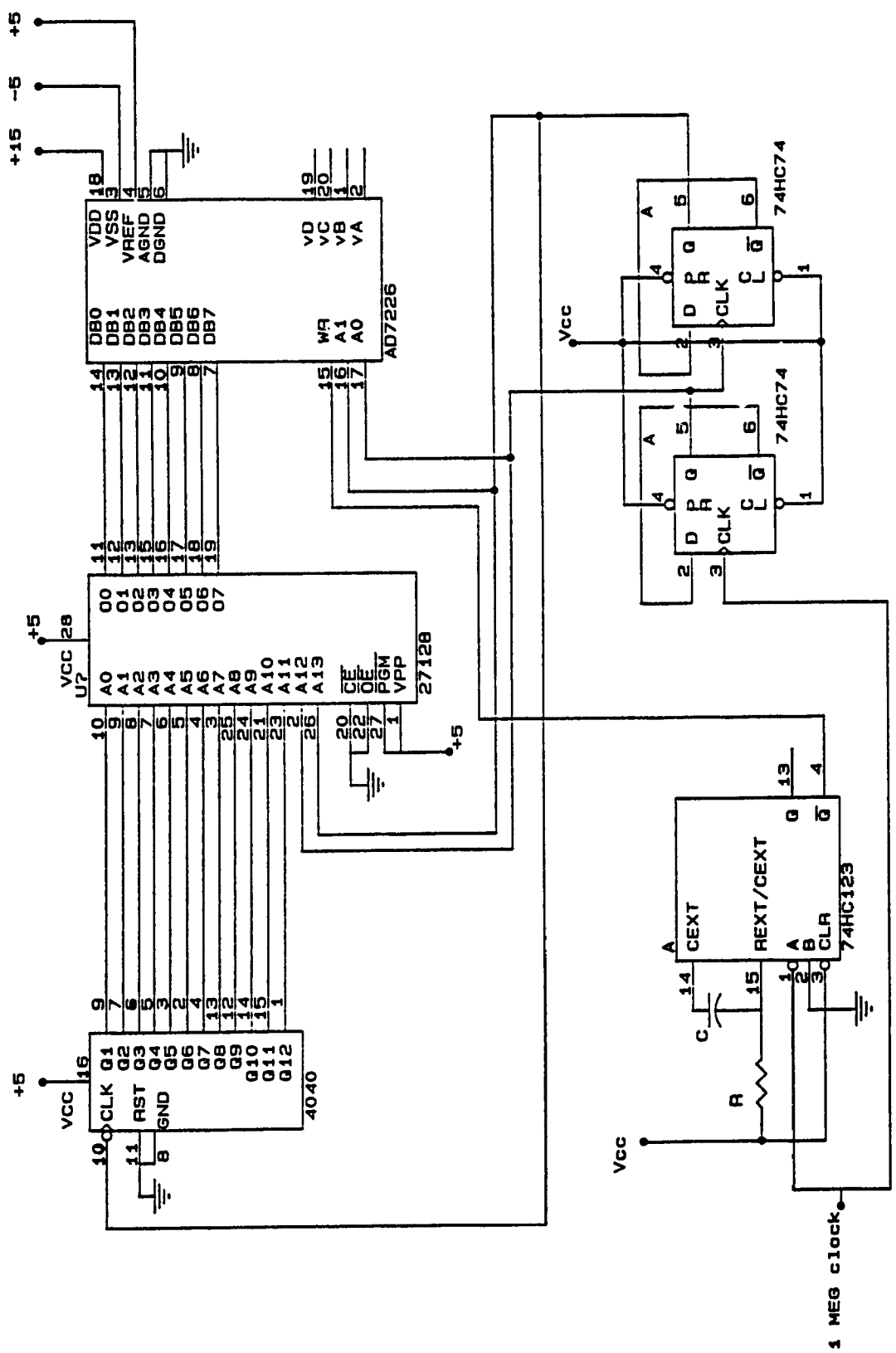


Fig. A.1 Layout of the proposed error triangulation technique.



C = 50pF

R= 1.2 k ohms

Fig. A.2 Layout of EPROM and logic circuitry.