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Using a Single Chip Microcomputer as a Remote Interface Device in Fire Detection Systems

Mostafa Safwat Kassem

A Major Technical Report

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ABSTRACT

Using a Single Chip Microcomputer as a Remote Interface Device in Fire Detection Systems

Mostafa Safwat Kassem

The objective of this report is to study the feasability of using a single chip microcomputer as a remote interface device between heat and smoke detectors and a centralized microcomputer system. The reason for this approach, besides the cost cutting benefit that the micro processor technology provides, is the improved system intelligence.

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ACKNOWLEDGEMENT

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CHAPTER 1

INTRODUCTION

Most of us are aware of the need for fire protection, especially in high risk applications prevelant in the chemical, petroleum, power generation, and offshore industries. Expressions like "life safety", "property loss", "business interruption" are well understood, to say nothing about the codes and standards that dictate the minimum levels of protection.

A fire detection and alarm system is a combination of devices designed to signal an alarm in case of a fire. The system may also accomplish fan control, fire door hold or release, elevator recall, emergency lighting control and other emergency functions. These additional functions supplement the basic system which consists of detection and alarm devices and central control unit.[1]

The fire protection industry has benefitted from the spectacular sophistication offered by the electronics technology in general and the micrbprocessor technology in particular. The introduction of microprocessors in automatic fire detection systems is very recent and is limited to the central control unit. As more and more computing power gets packed into ever shrinking bits of silicon, perhaps nothing demonstrates this silicon power better than today's single chip microcomputers. These new arrivals come very close to

becoming a system on a chip. Features like large ROM size a whole page of RAM, timer, UART, I/O resources are nothing new.

In this thesis we will address the usage of such a single chip microcomputer in the fire potection system , not in the central control panel where they usually belong , but as an interface circuit between field devices and the central micorprocessor.

In the first part of the report we will introduce the elements of fire protection systems as to familiarize the reader with them. In the second part we will deal with the requirements for the single chip microcomputer to be used in this project and compare the merits of 4 single chip microcomputers considered for this project . Following that we will show how the selected microcomputer will be used to remotely interface the detectors and alarm devices with the central microcomputer.

Subsequent chapters will address the transmission line drivers and receivers with particular emphasis on calculating the transmission line parameters .. Finally the last part of the report discusses the communications protocol and the central / remote message definition and the software flow chart used with the single chip microcomputer.

CHAPTER 2

DETECTION AND ALARM DEVICES

2.1 Introduction

The basic fire protection system consists of two parts, detection and annunciation . The detection is accomplished by using different kinds of detectors .They convert the fire products into an electrical signal that can be easly processed . The annunciation is accmoplished by using alarm devices like flashing beacons , bells , buzzers and horns . In this chapter we will discuss the characteristics of the forementioned devices and their usage.

2.2 Detection Devices

Fire is the process of combustion, a chemical reaction producing heat, flame, light, water vapor, gases and other products. An automatic detection device, such as a heat, smoke or flame detector, will sense the presence of one or more of the above products and generate an alarm signal. There can be also human discovery of a fire, resulting in a manual activation of an alarm device . The fire alarm box , "manual pull station", is nothing but a manual switch designed to close or open a circuit when operated . Once

operated, however, the switch can not be externally reset to the normal position. This feature prevents the actuated alarm from being silenced by unauthoized personnel.

2.2.1 Smoke Detectors

There are two types of smoke detectors , the ionization type and the optical type. The ionization type contains two radioactive sources (the amount of radiation is very small and not hazardous to human beings). One of these radio active sources ionises the air in an outer chamber which is exposed to the atmosphere while the other ionises the air in a virtually sealed inner chamber which acts as a reference to the other chamber by compensating for atmospheric changes.[3] Particles of smoke entering the outer chamber reduce the small current which is flowing, resulting in an imbalance between the outer and the inner chambers causing an SCR to be turned on indicating an alarm condition. The SCR stays latched in this state until it is reset , after the smoke has been cleared , by temporary interruption of the power. When a typical detector enters the alarm state its current consumption increases from a mere 15 microampere to 60 milliampere.

The optical smoke detector (fig. 1) consists of a light source (L.E.D) with its associated lens system . Together they produce a circular beam of light. A silicon photocell is positioned so that it is not directly receiving the light

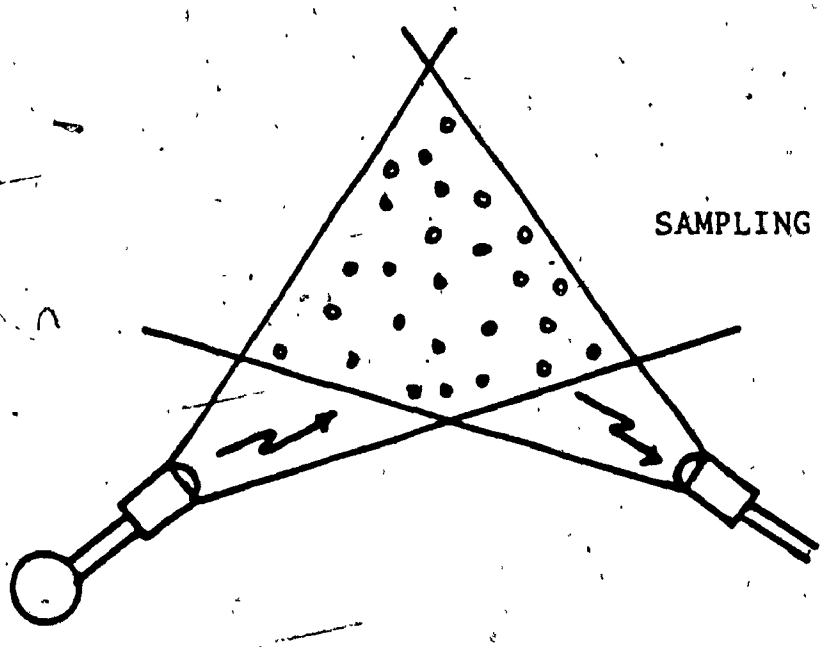


FIGURE (1) OPTICAL SMOKE DETECTOR

source signal. The light source is pulsed once every 8 seconds. Under no smoke conditions light cannot be scattared and therefore the photocell will have no output signal . When smoke enters the sampling area, pulsating light from the light source is scattered by the smoke particles . The photocell catches this scattered light and converts it to an electrical signal which causes the light pulse generator's duty cycle to increase from one pulse per 8 seconds to one pulse per second. After a few seconds an SCR is turned on indicating an alarm condition and stays latched until temporary interruption of the power (provided that the smoke has been cleared).

The major difference between the optical and the ionisation type smoke detector is that the latter is sensitive to very small invisible particles of smoke while the former is sensitive to large visible particles of smoke .This is an advantage in places where smoking is permitted.

2.2.2 Heat Detectors

The function of a heat detector is to sense either an abnormal rate of rise in temperature or the reaching of a preset temperature. Heat detectors normally give a slower response time than smoke detectors. However they are mainly used in areas where smoke detectors are unsuitable or are not required. Most heat detectors are based on the fact that heat changes the physical properties of materials .It

expands metals , liquids or gases and it changes the characteristics of material like the melting of solids , for example .

One method of manufacturing heat detectors is by utilizing two thermistors. One is exposed to the hot gases and a second one is contained in such a way that with an increasing ambient temperature , its temperature and therefore its resistance change lags behind the exposed one, resulting in an electrical imbalance. This in turn causes an alarm state by increasing the typical detector's current consumption from 60 microampere to 60 milliampere and latching into this alarm state until a temporary interruption of the power, provided that the cause of heat has been cleared .

Another method of manufacturing heat detectors is based on the expansion of air within a sensing chamber which has a calibrated bleeding hole. A steep temperature gradient will cause rapid expansion of air inside the chamber, which the bleed hole cannot accomodate , causing the chamber to expand. This in turn causes an electrical contact to be made causing an alarm condition. Also a fixed temperature detector operates by the expansion of an encapsulated bi-metallic element. The advantage of this type of heat detector is that it is self-resetting and does not require a temporary interruption of the power.

2.2.3 Flame Detectors

Flame is the visible or invisible burning gases or vapor produced by fire. Flame detectors are line of sight devices that will generate an alarm signal when exposed to the radiant energy from a flame. Since this radiant energy travels at the speed of light, flame detectors have the potential for being fast acting. Flame detectors, because of their fast detection capabilities (their reaction time is in the millisecond range) are, in general, used where a serious hazard exists, such as fuel storage, industrial process areas and situatons in which explosions or very rapid fire may occur.

2.2.4 Ultraviolet Detectors

One type of flame detector is the ultraviolet (UV) detector that responds to invisible radient energy in the ultraviolet region (below 4000 angstroms). Normally, UV detectors are designed to be reponsive only in the range of approximately 1800 to 2500 angstroms . This narrow band eliminates false alarms from electric discharge , lighting and solar radiation.

One disadvantage of UV detectors is that they may also respond to radiant energy from X-ray machines , arc welders and lightning.

Smoke is another problem because it filters UV radiant energy. Consequently , UV detectors should not be used in areas where large amounts of smoke are likely to occur before the appearance of a flame.

2.2.5 Infrared Detectors

The infrared (IR) detector utilizes a photovolaitic or a photoresistive cell with a filter and lens system and responds to invisible radiant energy, above 7700 angstroms. The IR detector responds to many heat sources and is, therefore, susceptible to false alarms, even when they are equipped with sophisticated discrimination schemes. These detctors are also affected by high humidity. For these reasons IR detectors have very limited applications.

2.2.6 Flame Flicker and Photoelectric Flame Detectors

These detectors respond to visible radiant light energy, which is in the range of 4000 to 7700 angstroms. The photoelectric device consists of a light sensetive photocell that will generate an alarm signal when exposed to the radiant energy of a flame.

The flame flicker device , which also operates on the photoelectric principle , contains a filter that permits detection operation only in reponse to the radiant energy modulated at a frequency characteristic of the flicker of a

flame , making the latter device more accurate in responding to the visible radiant energy from fire. Flame detectors are more expensive than smoke or heat detectors.

2.3 Alarm Devices

Alarm devices signal an alarm either fire or system trouble when activated. They can be audible or visual. Audible alarms include bell, horns, chimes, buzzers and sirens , while visual alarms include annunciators , strobes and flashing lights . Alarm systems may incorporate solid state sound reproduction and emergency voice communicates using prerecorded or live voice instructions. Printers that record time, date, location and other information are normally installed at large facilities where a record of all alarms is required.

Figure 2 illustrates how the previously discussed devices can be intergrated into a typical automatic fire detection system. Depending on the application, systems can vary in size from the very small (just one smoke detector in an apartment or a big house) to the very big industrial complex system containing thousands of detectors .

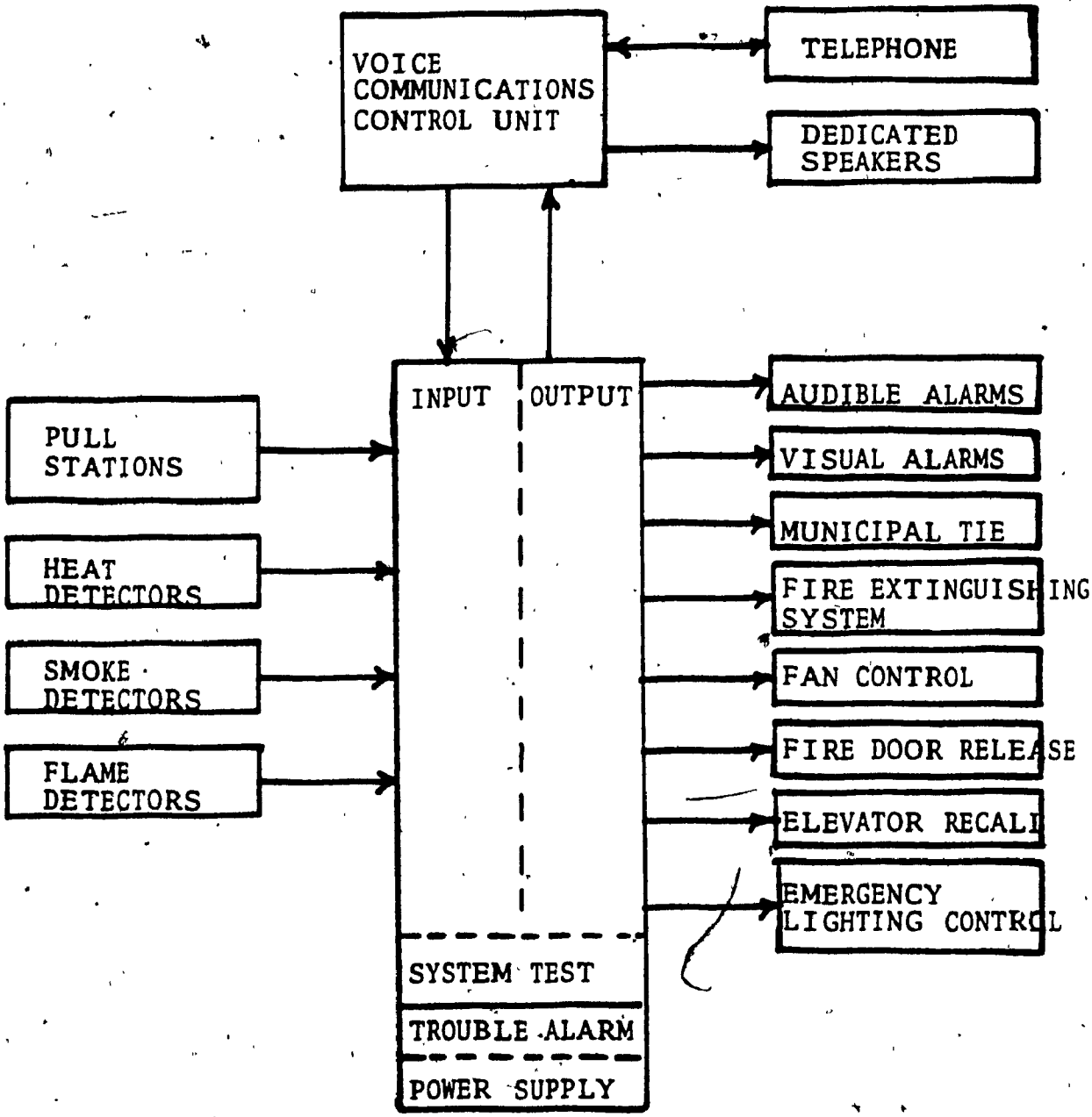


FIGURE (2) ELEMENTS OF A FIRE DETECTION SYSTEM

CHAPTER 3

CONTROL UNITS

3.1 Introduction

Any fire protection system contains different types of detectors and alarm devices . One can not rely on their local indications and outputs for fire detection . A control unit provides a centralized point to monitor and control the system activities.

3.2 Importance of the control unit

The central control unit serves a five fold purpose.[2]

(1) It receives signals from the detection devices, and operates the alarms and other output devices.

(2) It provides a trouble signal in case of systems malfunction.

(3) It provides a point of system control.

(4) It provides a system test point.

(5) It supplies electrical power to the system.

If we look at the fire protection industry as a whole, we would have to admit that the most significant developments are being made in the field of electronics control systems. That should come as no surprise, as this is also the case in many other industries where the large scale integration of electronics - including the microprocessor technology - has

increased system performance, improved reliability and at the same time reduced cost.

It is difficult to find another fire protection related product where such dramatic developments are taking place and so many new capabilities are being made available to the fire protection system designer.

3.3 The Historical Approaches

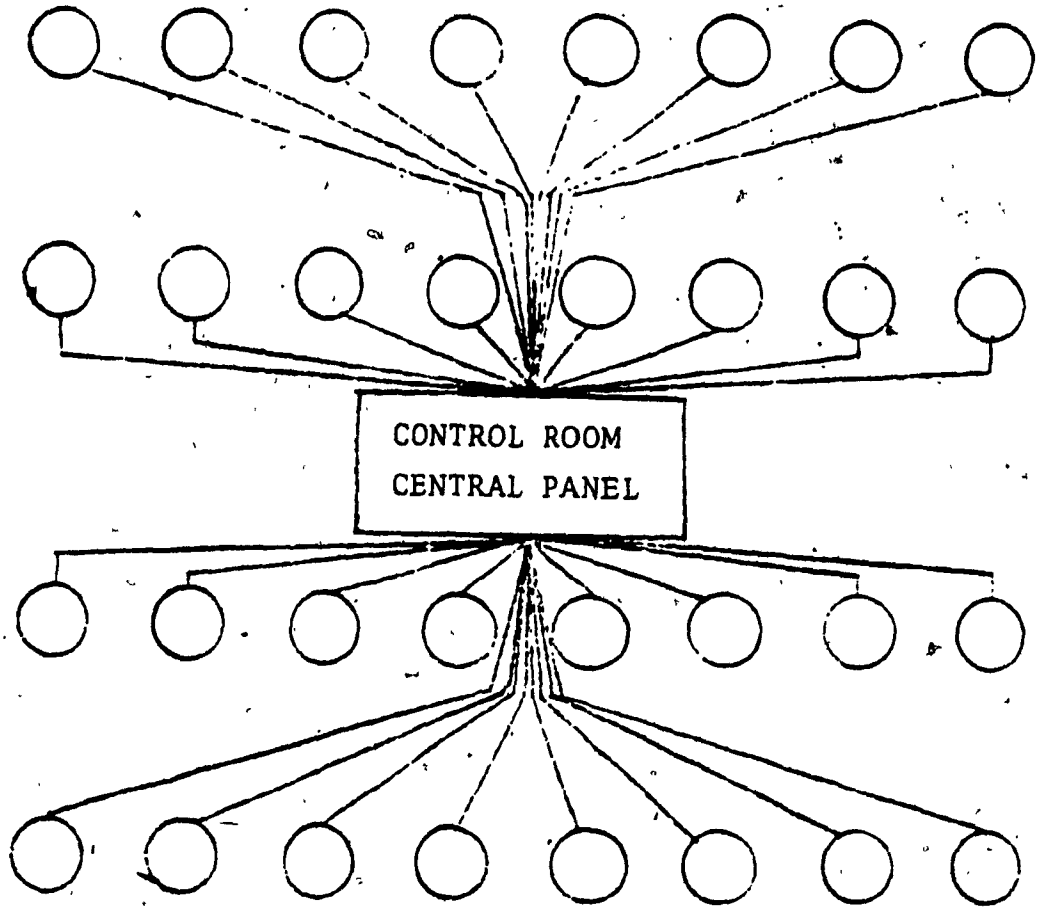
Let us take a look at some historical approaches, the first invovling a hardwired central master control panel and the second covering a scheme of distributed hardwired panels, while the third shows a microprocessor system.

3.3.1 The Central Master Fire Control Panel

Figure 3 illustrates the configuration of a centralized fire detection system. There are several items worth mentioning;

- -The control panel is usually located in a central control room.
- -The circles depict input and output devices (including detectors, bells, horns, release, pump starters, ect.) with which the control interfaces.

All of these devices are hardwired to and from the central panel.



= A DETECTOR OR AN ALARM DEVICE

FIGURE (3) THE HARDWIRE APPROACH

The major disadvantages of this approach are :

-The control system takes up a lot of valuable space in the control room.

-The cable and cable installation costs are very high.

-The central panel does not lend itself to changes without extensive addition or modifications to the cables once the project is completed .

-The more cables there are in a system the more likely they will become damaged due to fire or mechanical damage.[2]

3.3.2 The Hardwired Distributed System

Figure 4 illustrates a typical distributed system which has more than one identical satellite panel distributed through the system, so as to minimize wiring to and from the input and output devices. These satellite panels are usually self contained and not interdependant. They are usually connected back, via hard wiring , to a simple annunciator in the control room . With this approach the major objections to the centralized approach are eliminated.

-Since the panels are distributed throughout the system, the wiring to and from the field devices is minimized thus reducing cabling costs and complexity.

-Since a simple annuciation panel is used in the control room, less space is consumed.

-Also, any changes or modifications to the system are much easier, since they are done on a regional basis. However, two objections still remain. One of them is aggravated by the distributed panels approach .

The first objection is that the annunciation to the control room using this technique is very inadequate from a fire protection stand point. Since the primary objective of the distributed system designer provides only for general alarm and general trouble signals to be hardwired from the satellite panels to the central annunciator panel in the control room .The second objection is that it requires the operator to pay a visit to the satellite panel to investigate the cause of the alarm or trouble.[2]

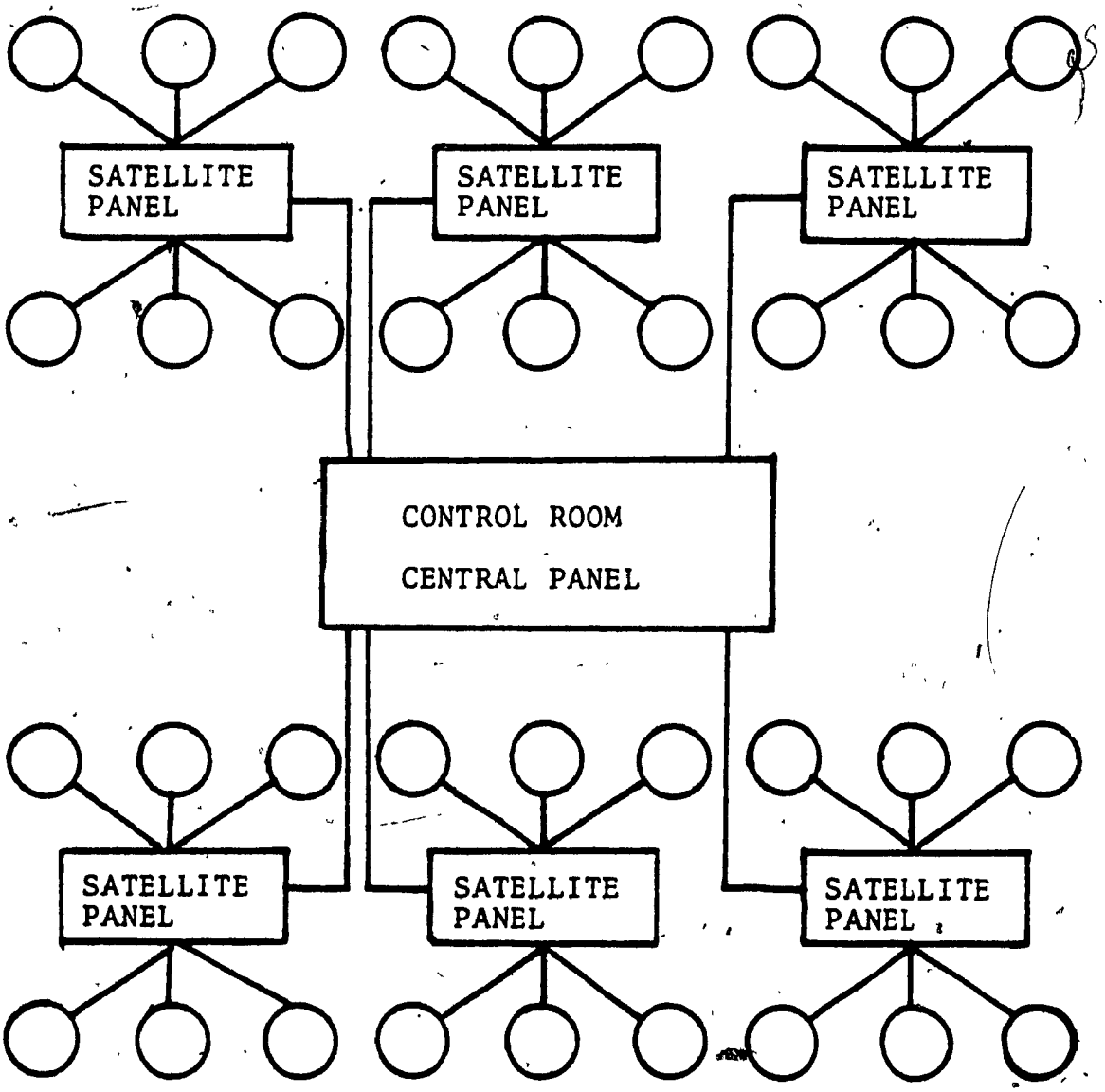


FIGURE (4) THE DISTRIBUTED APPROACH

3.3.3 The New Approach

Now that we have examined two of the historical approaches, we can use them as a reference when we discuss the new system operation and list some of its benefits to the two earlier approaches. Also it adds several important features that are not possible with the hardwired system. With the proliferation of microprocessors , more and more manufacturers are replacing their discrete digital IC's central control units with a microprocessor based one. This new aproach is the result of;[2]

- -The developments in the microprocessor technology that incorporate a sophisticated control system into small and versatile packages.
- -Developments in high security communicatons systems enabling the electronics to be placed remotely from the central facility.
- -Developments in hardware and software permitting the cost effective employment of a microprocessor based system in the control room.

Figure 5 depicts the new system approach in the simplest of forms. This new approach has an altogether different technique for communicating back to the control room. Instead of using dedicated cabling between each remote device (be it a detector or an alarm device) and the central control panel, with a pair of conductors for each signal transmitted or received , now all that is required is a four

conductor cable going in a loop shared by all the remote devices and the control panel.

The saving in cable is obvious, but the most important feature is the amount of information that can be communicated over this simple arrangement utilising digital signaling.

One disadvantage of this approach is the dependency on a single cable for power and signaling . In cases where reliability is of extreme importance , two or even three cables taking different routes throughout the system can be connected in parallel.

As was stated before , the microprocessor technology has been recently used in the central control units . The interface between the central control unit and the field devices (detectors , alarm devices , etc) remains committed to discrete components . This project takes advantage of the recent advances in the single chip microcomputer technology in order to use a single chip microcomputer as an interface device between central control units and field devices.

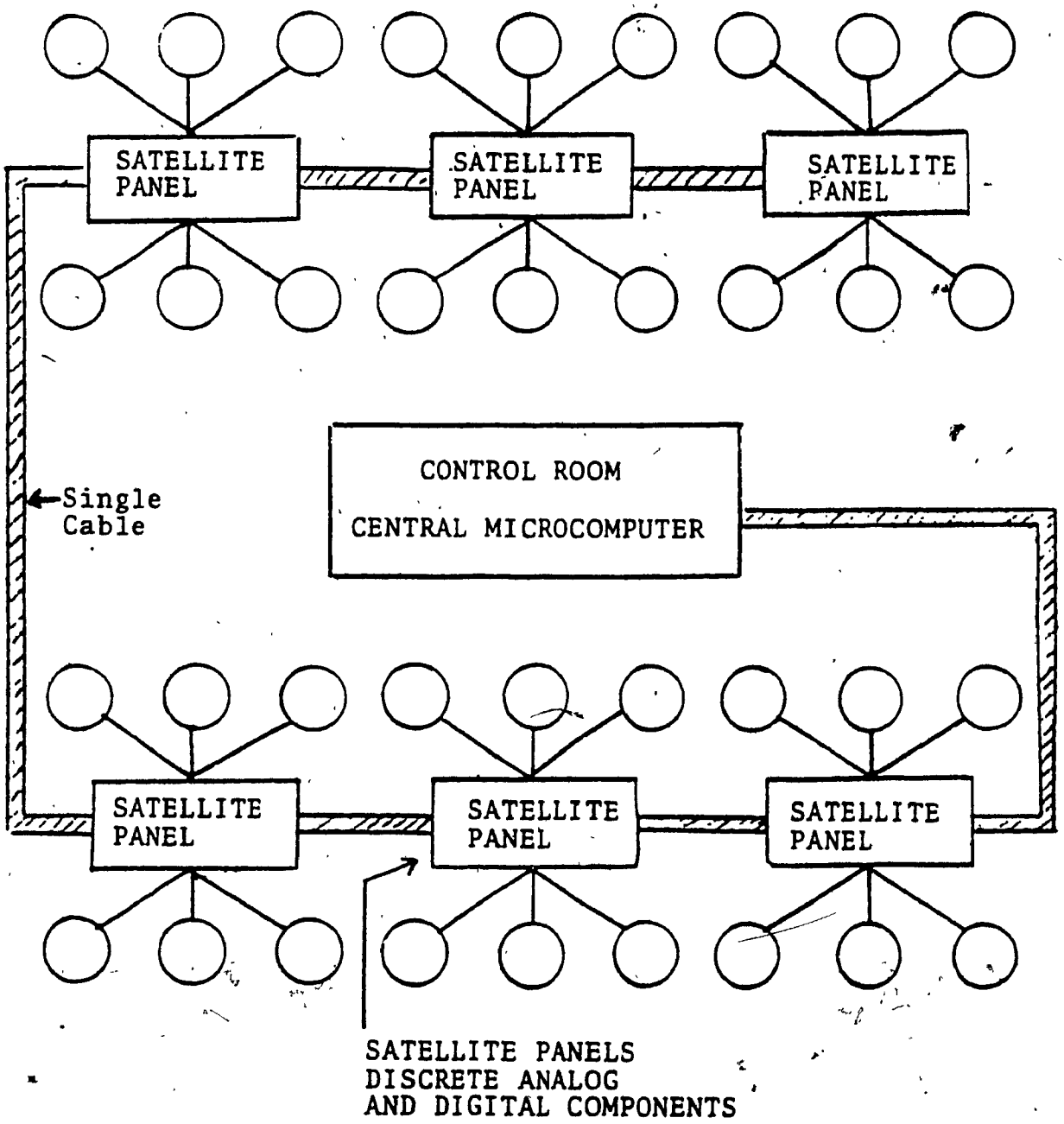


FIGURE (5) MICROPROCESSOR APPROACH

CHAPTER 4

THE SINGLE CHIP MICROCOMPUTER

4.1 Introduction

Now that the basic elements of a fire protection system have been reviewed we can turn to the second part of this report which deals with the single chip microcomputer that was chosen for this project. A single chip microcomputer was chosen over discrete digital and analog devices (due to its extreme flexibility, size, cost effectiveness and its input/output resources) to interface the field devices with the central microcomputer.

4.2 Requirements for Choosing a Single Chip

When choosing a microcomputer for this project, there are certain requirements that one must adhere to. The first of these requirements is the utilization of the CMOS technology throughout this project for high noise immunity and reduced power consumption, resulting in cooler operation, and a smaller, more efficient power supply. The second requirement is the availability of an on board UART (Universal Asyncronous Receiver Transmitter) to facilitate serial communications between the central microprocessor and the single chip field computers. The third requirement is

the availability of analog to digital converters on board, for the simple reason that the field devices must be monitored not only for their normal and alarm conditions, but also for open and short circuit conditions, which means we must monitor four states on one line, a task that can not be done without the help of a simple A/D converter. Actually these four states correspond to four voltage levels . Table 1 shows these four voltage levels as exhibited by a typical detector when it is connected to a 24 V power supply via a 1 KΩ short circuit protection resistor.

TABLE 1

Typical Detector Voltage Output Levels

voltage level	detector condition
> 22 volt	detector is in open circuit condition
>13 v - 22 v	detector is normal
1 v - 13 v	detecor is in an alarm state
<1v	detector is in short circuit condition

While it is true that this task can be accomplished by using two comparators per detector , the saving in board space and the overhead associated with extra components makes having the A/D converters on board a desirable feature.

Several single chip microcomputers were considered for this project. They were ; the TEXAS INSTRUMENTS 70C40, the NATIONAL SEMICONDUCTORS COPS (for "control oriented processor"), the INTEL 80C51 and the MOTOROLA 68HC11A4. Table 2 summerizes their main features. It becomes very clear from the table that the MOTOROLA 68HC11A4 stands out as the best choice as far as the hardware attributes point of view. This processor also has an excellent software instruction set.

Table 2

Comparison Between 4 Single Chip Microcomputers [5,6,7,8]

	68HC11A4	Cops	70C40	80C51
ROM	4K	2K	4K	4K
RAM	256 Byte	128 Byte	128 Byte	128 Byte
EEPROM	512 Byte	N/A	N/A	N/A
I/O Lines	40	20	32	32
Timers	1/16 Bit	--	2/13 Bit	2/16 Bit
UART	Yes	No	No	Yes
A/D	8 ch.	N/A	N/A	N/A
CMOS	Yes	Yes	Yes	Yes

4.3 The Motorola 68HC11A4

The MOTOROLA 68HC11A4 , as shown in block diagram in figure 6 , is a very advanced single chip microcomputer that lends itself well to various control applications. It boasts an impressive array of hardware and software features, built with a CMOS process which offers the highest noise immunity of all logic families and, because of its low power dissipation , it reduces the power supply rating and in turn keeps the system cooling requirements down to a minimum.[9]

4.3.1 Memory Resources

The 68HC11A4 could run in the single chip mode or the expanded mode which is capable of addressing up to 64k of external memory. Since this project will use the single chip mode , the expanded mode will be totally ignored.
The 68HC11A4 has on board 4k byte of ROM, big enough for a large control program. It also has 256 bytes of RAM to hold temporary data, flags, status of different prephirals. However the most impressive feature of this processor's memory resources is the 512 byte of EEPROM which permits the software programmer to write small modules or tasks that could be ROMable, but the final program could be designed by programming the EEPROM to call up these small tasks. This feature is also very attractive to those designers who have more than one product or one product with different models

that has the same progam core but differ slightly from each other. This large EEPROM could also hold last minute data or program changes. In fact , the EEPROM is large enough to hold an entire control program without having to use the on board ROM, or replace some ROM based software routines found to have bugs.[11]

4.3.2 Input/Output Resources

The 68HC11A4 has 5, 8 bit I/O ports. Some of these ports are dedicated to one function only (port B is always an output port, while port C could only be programmed to be either an output or an input port) while the other ports can serve a dual purpose which is software selectable (port E could either be programmed to be a general input port of an 8 channel A/D converter). Pins PD0 and PD1 of I/O port D are used either as general purpose I/O or as the receive and transmit lines of a full duplex UART with an internally programmable baud rate generator.

Pins, PD2, PD3, PD4 and PD5 can serve as general purpose input/output or form the basis of a multi-processor syncronous communications enviroment, PD2 acts as the master-out-slave-in line, PD3 as master-slave-out line, PD4 as the syncronous clock shift line (sck), PD5 as the slave select line (ss). Refer to the 68HC11A4 data sheets for illustration on how to connect these lines in a multi-processor system configuration.

When port E is not used as a digital input port , it could be used as an 8 channel successive approximation analog to digital converter with multiplexed inputs. An 8 bit dual mode counter is part of the silicon real estate. In the first mode the counter works as a simple event counter which must be clocked externally. In the second mode, the gated accumulation mode, the internal clock is divided by 64 to drive the counter while an external input serves as a gate.[9] Port A can be configured as a general purpose I/O port or can be connected to the internal timer section. A programmable prescaler sets the timer clock, which can be set to divide the processor clock by 1,4,8 or 16. Also connected to the timer are 3 input capture registers and five compare registers.

An input capture pin associated with each input capture register can be programmed to detect signals on the positive or negative edges or both, a feature that is useful in applications in which the current state of the input is either unknown or unimportant and the next change of state should be registered.[12] The appropriate transition causes the value of the counter to be latched into the selected input capture register. The input capture signal can be disabled via software and there is also a separate interrupt for each input line.

The five outputs compare registers indicate whether their values match the contents of the counter. When a successful comparison is detected by any output compare register its

corresponding line can be toggled, set high or cleared . As in the input capture function the output comparison function can be disabled via software.

4.3.3 Watch Dog Timer

Although new software design techniques like structured programming and top-down design minimize errors, routines are bound to have errors. Therefore the 68HC11A4 has a watch dog timer called the cop (for "computer operating properly"). When the cop watch dog timer is used, a special software routine must be executed periodically or the timer will initiate a reset to bring the system under control. The cop time out period can range from 10 ms to 1 second and unlike conventional watch dog timers which depend on the system clock for their own operation, the 68HC11A4 has a clock monitoring system, a retriggable monostable multivibrator that is triggered continuously by the internal clock. If the clock stops operating, the clock monitoring system will detect the event within 100 microseconds. If , due to power consumption constraints , the 68HC11A4 had to run on very low speed to save power, the clock monioring system could be disabled by setting a bit in the cop control register. If a failure is detected in either the watch dog timer or the clock monitor system, the reset terminal becomes an output with a logic 0 level, forcing the rest of the system to reset.[11]

These protective hardware and software features are very essential to ensure system integrity and functionality.

4.3.4 Software Considerations

The 68HC11A4 is part of the Motorola 6800 family but unlike the original microprocessor it has more on board registers. Beside the 16 bit program counter and stack pointer, it has two 8 bit accumulators that can be concatanated to form a 16 bit accumulator, and two 16 bit index registers (X and Y registers).
Single chip microcomputers usually have a subset of the instruction repretoire of the family they represent. Not so in the case of the 68HC11A4. It has signed and unsigned multiply and divide instructions, bit manipulation instructions and new instructions to take advantage of the index registers and the enhanced accumulators.

4.3.5 Interrupt Structure

Table 3 illustrates the 68HC11A4 interrupt priority scheme. Generally there are three interrupt groups, the nonmaskable interrupt group which has the highest priority, the XIRQ which is masked by the X bit and the third group which is masked by the I bit lowest priority level. Even within each group there are priority levels.[11] The function of the X bit must be clarified further. Coming out

of power on reset , the X bit is set thus preventing unplanned interrupts on the XIRQ line from occuring during the initialization phase. This X bit can be cleared by software. However once cleared, enabling interrrupts on the XIRQ line, it can not be set again, which is why the XIRQ is called pseudo-nonmaskable interrupt.

By providing a Vector for each interrupt source , the 68HC11A4 eliminates the need for polling to determine the source of interrupt. All the software designer has to do is simply place the address of the interrupt service routine in the Vector associated with a particaular interrupt . When the interrupt occurs, program control immediately transfers to the address specified in that Vector without software polling , thus greatly enhancing execution speed. Notice that the timer section has ten different interrupts associated with it.

Table 3

68HC11A4 Interrupt Vector Table [5]

Vector address	interrupt source	Masked By
FFFG,F7 Lowest	Software interrupt	none
FFD6,D7	UART	I bit
FFD8,D9	Syncronous serial transfer	I bit
FFDA,DB	Pulse Accumulator input edge	I bit
FFDC,DD	Pulse Accumulator overflow	I bit
FFDE,DF	Timer overflow	I bit
FFE0,E1	Timer output compare 5	I bit
FFE2,E3	Timer output compare 4	I bit
FFE4,E5	Timer output compare 3	I bit
FFE6,E7	Timer output compare 2	I bit
FFE8,E9	Timer output compare 1	I Bit
FFEA,EB	Timer output capture 3	I bit
FFEC,ED	Timer output capture 2	I. bit
FFEE,EF	Timer output capture 1	I bit
FFF0,F1	Real time interrupt	I bit
FFF2,F3	Ext. interrupt or parallel I/O	I bit
FFF4,F5	Pseudo non-maskable interrupt	X bit
FFF8,F9	Illegal op-code trap	None
FFFA,FB	Cop failure (reset)	None
FFFC,FD	Cop clock monitor (reset)	None
FFFE,FF Highest	Power on reset	None

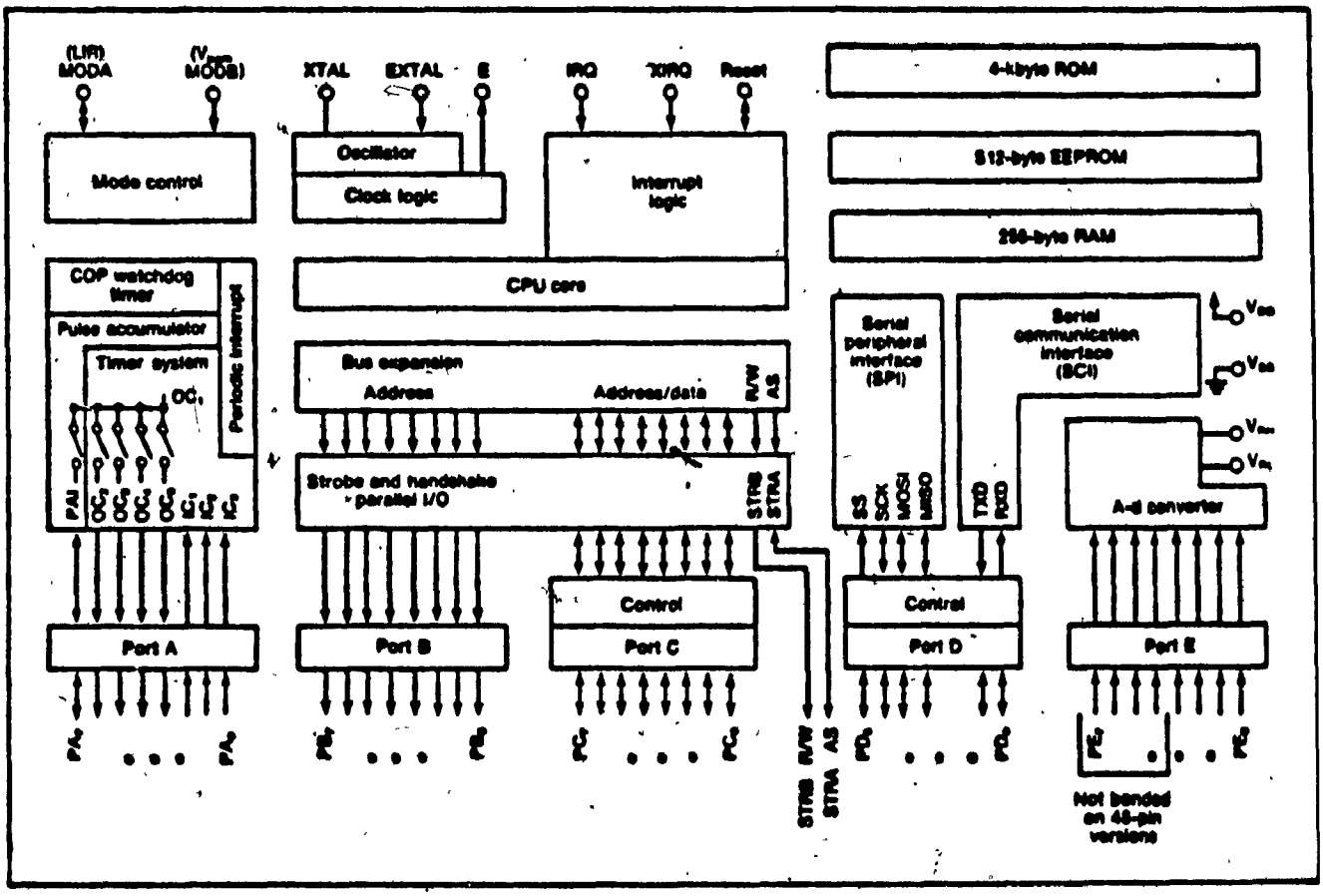


FIGURE 6 THE 68HC11A4 BLOCK DIAGRAM

CHAPTER 5

SYSTEM IMPLEMENTATION

5.1 Introduction

Now that the remote microcontroller has been chosen , let us see how to use such an advanced single chip microcomputer as a fire detection remote sensing device.

5.2 Remote Station Circuit Diagram

Figure (7A) illustrates the circuit used to utilize the MC68HC11A4 as a remote fire detecting circuit while figure (7) illustrates the same circuit in block diagram form . Notice that a single microcontroller can be used to monitor more than one detector, thus reducing system cost.
The loop power supply which is usually between 28v and 26v D.C is further regulated by a 5V 100 mA monolithic low power voltage regulator to supply power to the microcontroller. The on board oscillator , coupled with an external crystal of 2.4576 MHZ , supply the microcontroller with its timing signal which is divided internally by four to yield a processor frequency of 614.4 KHZ which is an even multiple of the RS232 baud rate generator .

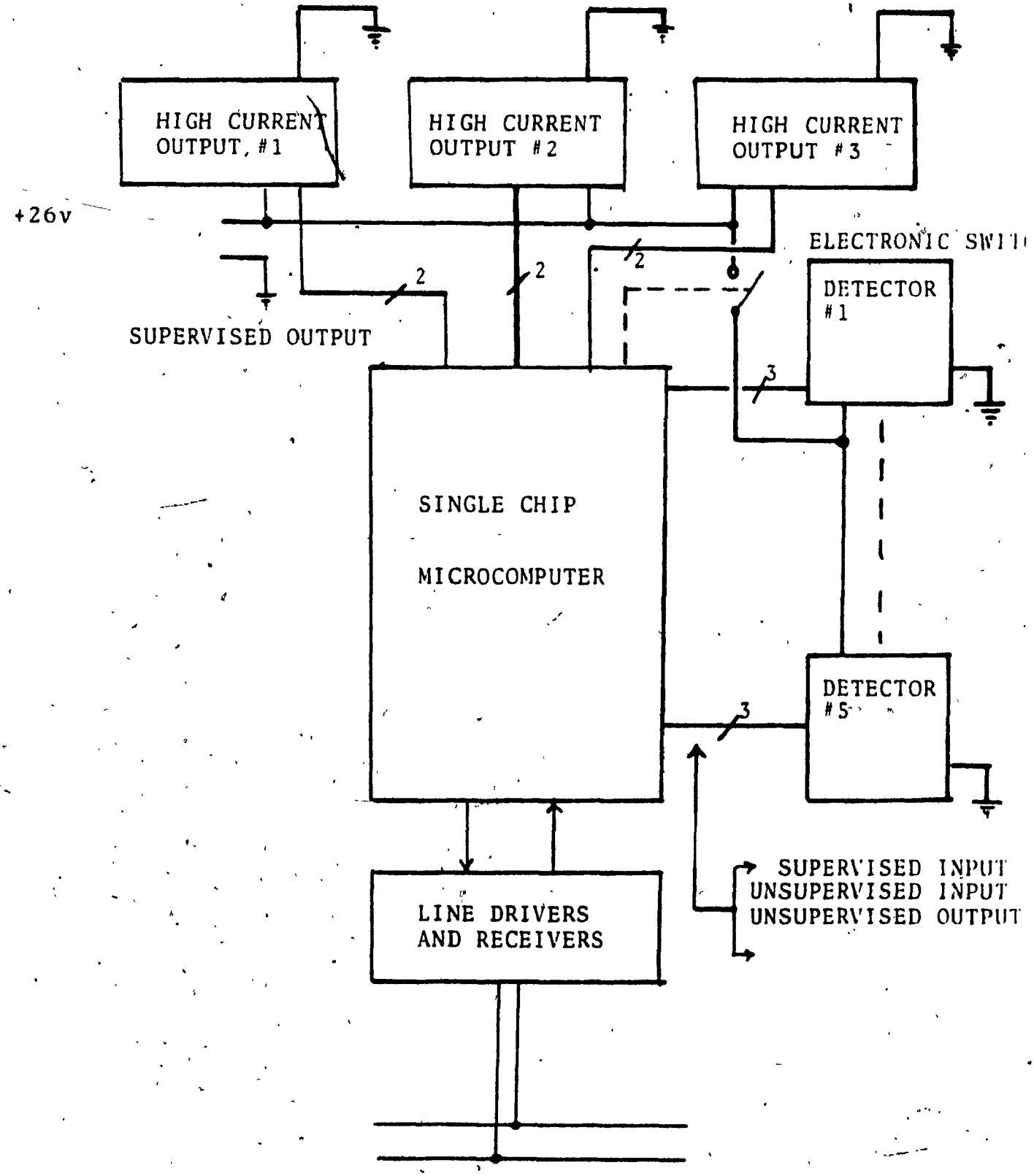


FIGURE (7) REMOTE STATION BLOCK DIAGRAM

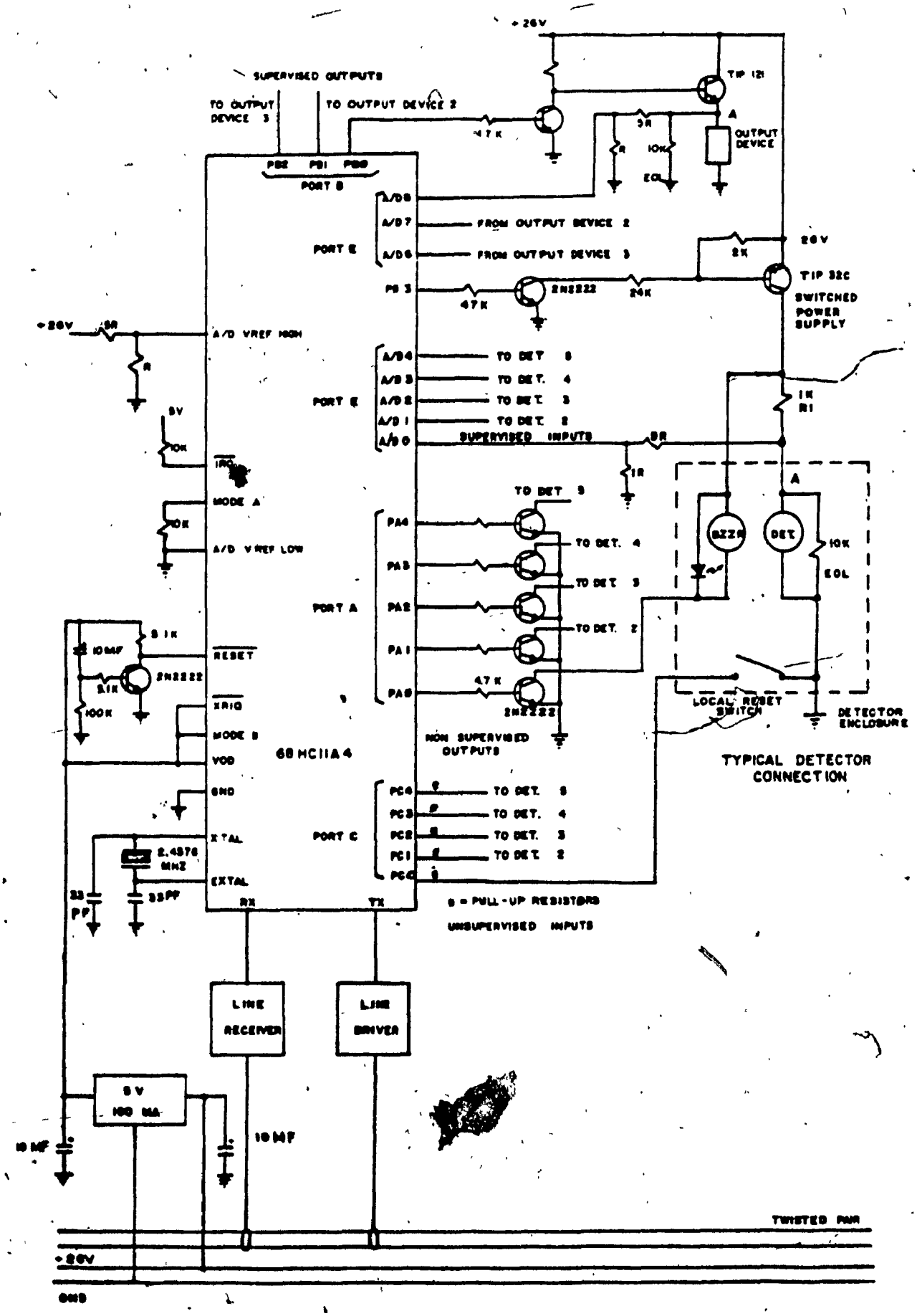


FIGURE (7A) REMOTE STATION CIRCUIT DIAGRAM

During the following paragraphs the term " supervised input or output " will be used to mean that the function in question is monitored for open and short circuit conditions in addition to its other normal functions.

5.2.1 Supervised Detector Connections

Power is applied to five detectors via a series pass transistor , the function of which is to interrupt the flow of power to the detectors upon command from the microcontroller in order to unlatch the output SCR from its alarm condition. The maximum detector current consumption is 65 mA , so the transistor should be chosen to handle approximately 650 mA without any degradation of its performance (5 Detectors * 65 MA each * 2 (factor of safety)) . R1 serves as a short circuit current limiting device in case of a short circuited detector . The 10K end of line resistor (E.O.L) helps the supervising circuit detect the presence of the detector since its normal state input impedance is very high , making it very difficult to distinguish between an open circuit condition and a normal condition without the E.O.L resistor.

The positive detector terminal (A) is connected to the microcontroller A/D converter circuit via an R / 5R divider circuit , the function of which is to reduce the detector output voltage from very close to the loop power supply (26V) to a safe value compatible with the maximum allowable

input voltage of the A/D converter which is 5V. Notice that the detector can exhibit four states , short circuit , open circuit , normal and alarm condition on a single line .

5.2.2 Supervised High Current Output Devices

There is a provision for three high current output devices . Each output is driven by a Darlington power transistor which is controlled by a bit from output port B . The output devices are terminated again like their detector counterparts by the end of line resistors . The output Darligton transistors are used in an emitter follower configuration to allow the grounding of one side of the output devices . Terminal (A) of the output device is connected to the microcontroller A/D converter via an R / 5R divider resistor network . When the A/D channel is read, it relays to the processor the state of the output device, a feature useful in protecting the Darlington transistor beside detecting output faults .

5.2.3 Unsupervised Inputs

There is provision for five unsupervised inputs , which could be the detectors local reset inputs. These inputs are connected to an input port via pull-up resistors .

5.2.4 Unsupervised Outputs

These outputs are low current output devices (buzzers and LED's) . These are of the open collector type which requires a low power driver transistor like the popular " 2N2222 . Also , like the unsupervised inputs there is provision for five unsupervised outputs which can serve as local alarm indicators at the base of each detector.
Now that the hardware part of the circuit has been reviewed, it is time to discuss the software part , mainly the communication protocol between the central station and the remote stations .

5.3 Communications Channels

The MC68HC11A4 has on board a programmable serial communications channel (SCI) with its own programmable baud rate generator that can support transmission speeds as low as 75 bauds and as high as 38400 bauds . Also the word length can be set via software to 5,6,7 or 8 bits with parity and one or two stop bits . This flexible scheme simplifies the serial data transmission since it covers a large number of variations. There is another serial communication channel within the MC68HC11A4 but it is of the syncronous type (it is useful in multiprocessor environment where more than one microcontroller exist on the same printed circuit board). This syncronous channel can be used

in this project but it was not adapted in favour of the asyncronous communication channel.

In cases where two serial communications channels are required , another serial communication channel could be synthesized by software using the on board timer and the interrupt request line to detect the start bit in case of receiving .Of course the processor has full control of the timing in case of transmitting.

This arrangement dictates that the central station has also at least two serial communications channels (UART) , a very easy task in light of todays LSI sophistication .

5.4 Communications Protocol

The communications link between the central station and the remote field microcomputers has to be very reliable and fast on the one hand and also simple on the other hand . It has to be noise tolerant which can be achieved by employing error detection techniques like the cyclic redundancy check or the check-sum method plus the usual hardware parity checking . This two way error detection scheme reduces to a bare minimum the possibility of erroneous message transmission between computers.

Basically to establish a reliable communications link between each of the field microcomputers and the central microcomputer there are two ways of connecting the field microcomputers with the central microcomputer. Figure (8).

illustrates the first way , called the open line method and figure (9) illustrates the second method , called the closed loop method . These two approaches will be discussed in detail.

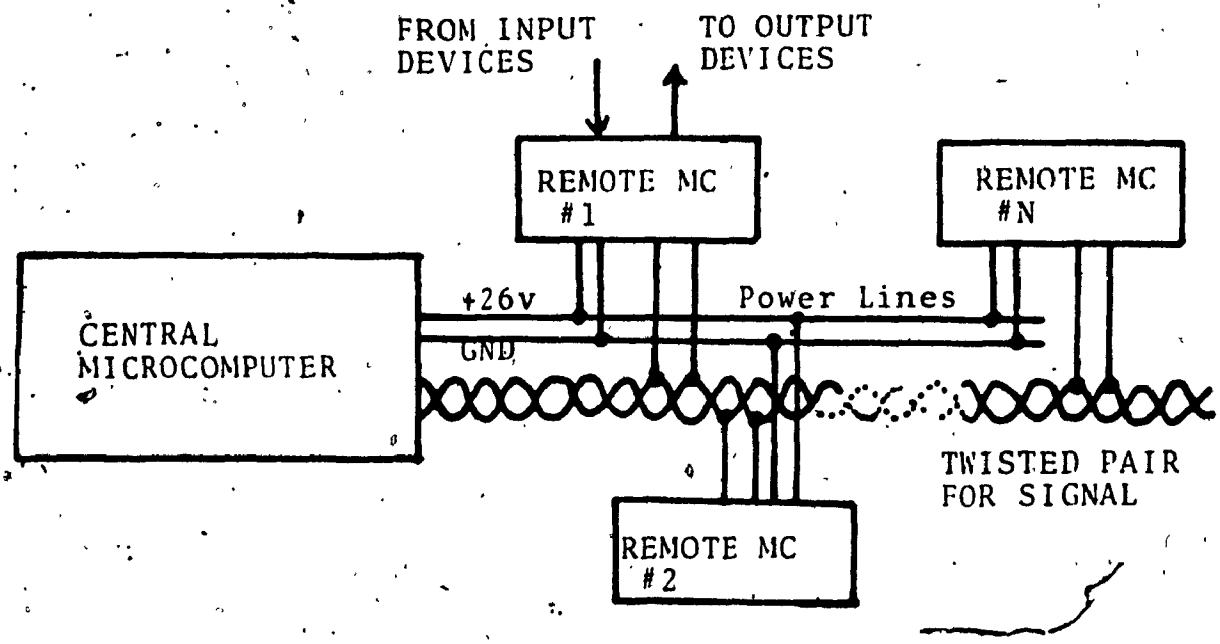


FIGURE (8) OPEN LINE (PARTY LINE) CONNECTIONS

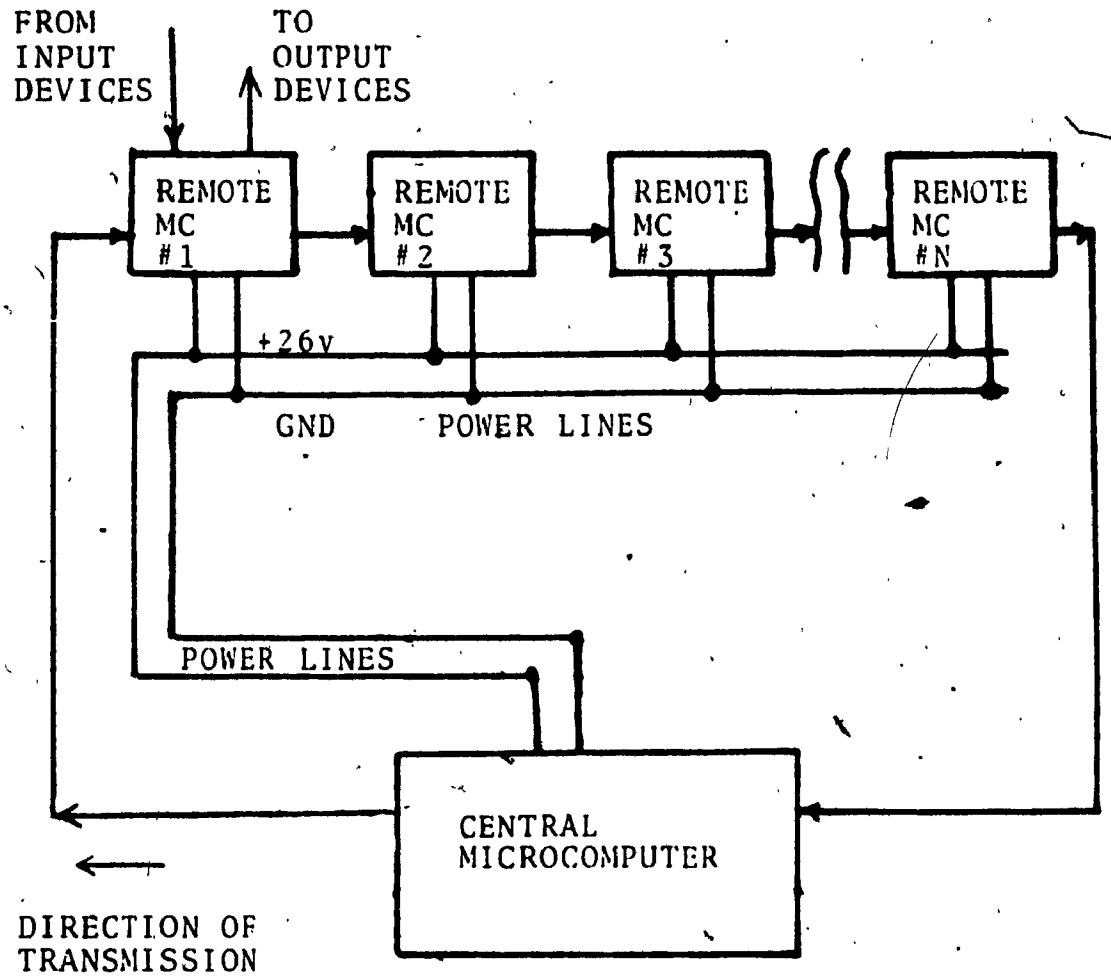


FIGURE (9) CLOSED LOOP CONNECTIONS

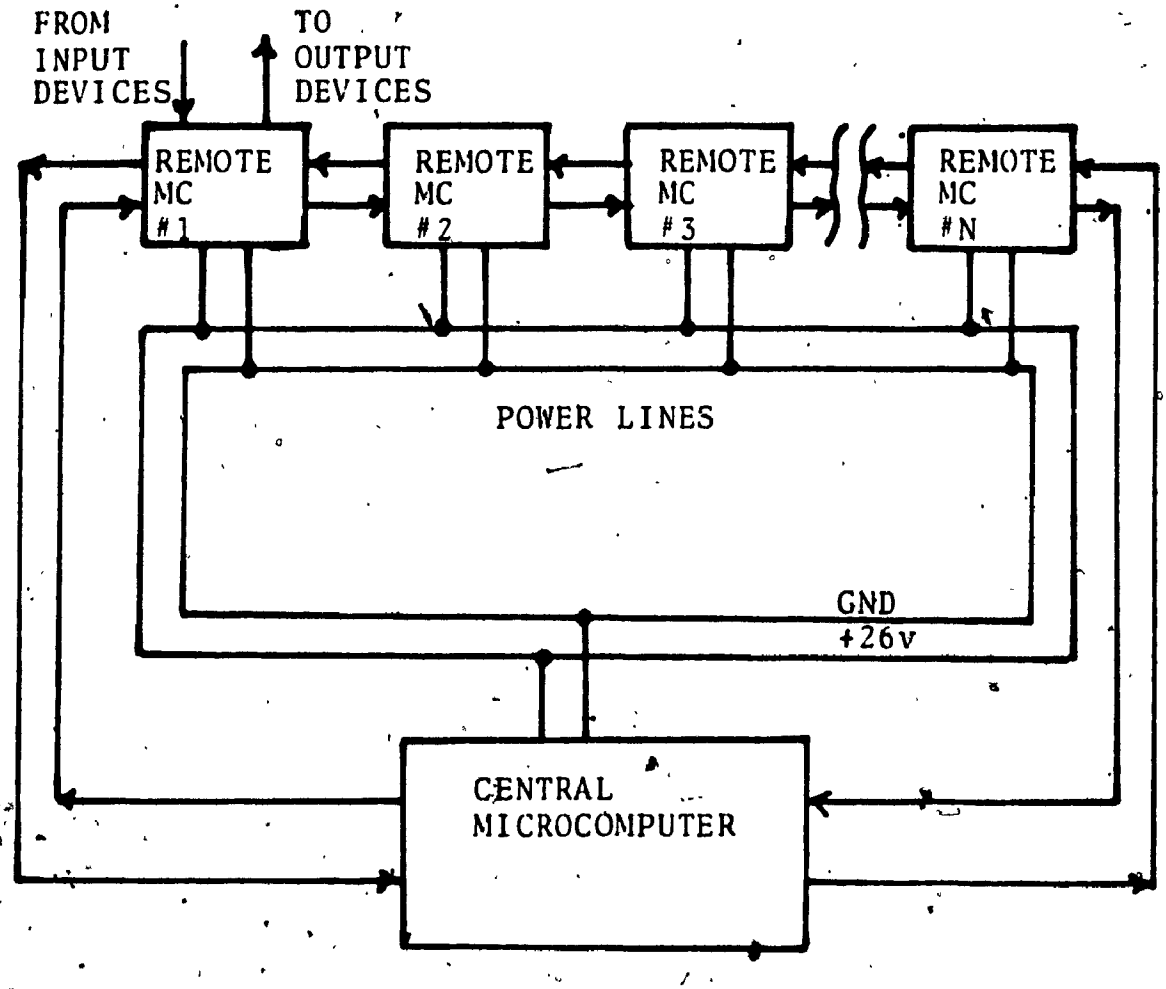


FIGURE (10). AN IMPROVED VERSION OF THE CLOSED LOOP APPROACH.

5.4.1 The Closed Loop Method

In this approach the transmitting output of one device is connected to the receiving input of the next device until the last device transmitting output is connected to the first device receiving input (which happens to be the central station). Figure (9) illustrates such an approach . Figure (10) shows a more reliable adaptation of this approach. Instead of having one transmitting and one receiving channel per station , each device has two communications channels so data transmission can flow clockwise and counter clockwise to facilitate loop communications even with a cable break between two adjacent stations.

In this approach , every remote station has an 8 bits ID code (yielding 256 remote devices per loop) . However, practically speaking the maximum number of remote computers will be less than 256 to give way to special one byte global commands from the central station.

5.4.1.1 Communications Protocol

Status Request:

The central station sends a one byte command requesting field devices status to the first remote station which responds by sending the requested information and at the -

same time , relays the command to the next remote station which relays the command to the next microcomputer while sending its status to the first remote station which again relays the information to the central station and so on until the last remote station receives its command. The central station receives and stores the status information from all remote stations in a RAM block then repeats the whole procedure again from the opposite direction this time saving the status information in another RAM block . Then from the two readings it can process the received data . Now that the received data has been processed , it is time for the central microcomputer to act upon it and starts sending commands to a specific remote station . For example, if a fire was detected , then the central station could sound a horn or shut ventillation or release gas by sending a command to the remote stations to turn certain output on (or off if it is normally on like a door holder). The central microcomputer starts the command message by sending the ID code , followed by the message itself ; the length of which is contained in the first three bits of the byte following the ID code . The last byte in the message is the check-sum byte.

Upon receiving the first message byte the first remote station checks if it is an ID code (between 1 and 240) or a global one byte command (between 241 and 255). If it is a global command it saves in its memory for later processing and then relays the command unchanged to the next remote

station which repeats the same operation until the last remote station receives the command and relays it to the central station as a way of acknowledging that the entire loop has received the command . If this acknowledgement was not received within a pre-calculated time delay that is dependant on the number of remote computers in the loop , the central station will assume that not all the loop devices have received its command either due to a cable break or due to a faulty device in the middle of the loop and then proceeds to send the same command from the other direction and repeats the same operation again in hopes of reaching those remote stations that could not be reached from the other direction.

Now if the first byte was actually an ID code (between 1 and 240) then the remote station decrements the ID code value . If the result was zero then the message was meant for this particular remote station and the message is saved for later processing . However , if the decremented ID code is not zero it is sent to the next remote along with the rest of the message which inturn repeats the entire procedure again.

Having sent a message to the remote station from one side the central station sends the same message again from the opposite side . Only then, when the remote station receives the second message and is compared with the first message and found equal that the remote excutes or processes the message.

From the previous discussion there are always two bytes of overhead associated with each message, the first ID byte and the last check-sum byte . The ID code byte can be eliminated by utilizing a different communications protocol that depends on the time delay between messages to determine the receiving remote station. This method is called store and forward . Here is an example on how it works .

Assume that the central station wants to send a message to remote station # 5 . It starts by sending messages 5,4,3,2 and 1 to remote #1 . Remote #1 stores the last message received (message 1) and forwards messages 5,4,3 and 2 to remote #2 . Remote #2 stores the last message received (message 2) and forwards messages 5,4 and 3 to remote #3. Remote #3 stores the last message received (message 3) and forwards messages 5 and 4 to remote #4 . Remote #4 stores the last message received (message 4) and forwards message 5 to remote #5 which stores that message and does not forward anything .

One disadvantage of this appraoch is that in order to send a message to remote # N , the central station has to send messages to all remote microcomputers before it , which may or may not be a bad idea . Another disadvantage is that a corrupt remote device in the middle of the loop will corrupt the data received and transmitted through this corrupt remote . Its advantage is beside reducing the message length by one byte , that we have saved an input port that was going to be used to set the ID code . Another important

advantage is the uniformity of all remote microcomputer and hence , it will be easier to replace a remote station in case of a fault . Another advantage is the less likelihood of errors due to mistakes in setting the ID code for each remote station.

5.4.2 The Open Line Method (The Party Line)

In this method all field devices share the same twisted pair coming out of the central station serial communications channel . Naturally there has to be an orderly way of communication so that each remote station is only allowed to send data on the line during a specific time . The software communications is based on the very popular RS-232C running half duplex . Each remote device is assigned an ID code or address between 0 to 127 (for a total of 128 remote devices).[13]

The central station sends a message to a remote station (whether it is a command or a status request) which consists of a few bytes (usually 3 or 4) . The first transmitted bit is always a zero indicating that the flow of data is from the central station to the remote station whose ID code is contained in the next seven bits of the first byte . The first three bits of the second byte indicate the number of bytes in the message excluding the first byte which has the transmission indicator bit and the seven bit ID code , including the last check-sum byte .

If,however , the first transmitted bit in a message was 1 , that means that the remote station whose ID code is contained in the following seven bits is responding to a central station message which has an ultimate control of the system party line . A remote microcomputer can not initiate a message . It can only respond to a query from the central station. As is the case with the message originating from the central microcomputer , the first three bits of the second byte originating from the remote station indicates the length of the message in bytes excluding the first byte but including the last check-sum byte.

5.4.3 Error Detection

In a normal communications cycle , the central station starts by sending a message to the first remote station requesting the status of its detectors and other devices connected to it . The addressed remote field computer responds immediately by sending a message containing the requested information which is received and verified by the central station . Then a message is sent to the next remote station via the central station UART . In the mean time the central microcomputer is processing the information received from the previous remote station.

If the central station does not receive the response expected to its message within 1 millisecond it re-transmits the message . If no response is received again then the

central station assumes a faulty remote station and shows a fault on a mimic display board or via a printer and then continues sending messages to the following remote stations, repeating the same procedure again.

5.4.4 Advantages and Disadvantages of The Open Line

The main advantage of this method is that remote stations can be added or removed from the circuit without interfering with the other remote stations . In fact, all that is required in this case is to change the value of a software counter . The other advantage is that the remote station could be far away from the central station without compromising the communications link integrity . Another advantage is the simplicity and the ease of maintenance. A major draw back of this approach is that a short circuit on the party line will paralyze the entire system until such a time when the short circuit is removed. Another disadvantage of this approach is that a cable cut can isolate part of system rendering it useless as long as the cable cut exists.

The advantages and disadvantages of the open line and the closed loop approaches have been discussed . The open line approach has been chosen for this project and the transmission line analysis will be based on that approach.

CHAPTER 6

TRANSMISSION LINE

6.1 Introduction

Because of the long distances involved in industrial and marine fire detection system (several hundred yards) a well designed transmission line is a very important link in a fire detection system , otherwise , the system will be plagued with an unbearable rate of transmission errors rendering the system useless.

Although the RS-232-C is used for communications in this project , the line transmitters and the line receivers do not adhere to the standard for the following reasons :

1- Standard RS-232-C line transmitters and receivers are guaranteed over a distance of only 50 feet .

2- They require additional voltage regulators and circuitry to generate the negative supply from the +26 v supply ,thus adding to cost and complexity of the circuit.

3- These standard devices are power hungry , consuming on the average about 40 mA per remote .That is not bad if we have only one remote .But at 100 remote devices that translates to 4000 mA . This is obviously a very high current consumption .

6.2 Transmission Line Connections for The Open Line Approach

Figure (11) shows the typical connections of the central station and the remote stations transmission line drivers and receivers . The transmission occurs by turning the transmitter line driver transistor on and off according to the bit pattern of the message which in turn modifies the current flowing through the transmission line which is monitored by the line receiver transistors of the receiving channels to form the bit pattern of the message being transmitted.[13]

6.3 Calculations of The Transmission Line Parameters

The line current IL is limited by the twisted pair resistance and the transmitter driver saturation voltage (Vsat). Figure (12) shows the equivalent circuit used to calculate the maximum value of line current of the current source.

Before calculating IL , let us calculate the minimum voltage required to cause a zero reading at the central microcomputer serial channel receiver input (figure 13).

Vmlz = minimum line voltage for a zero reading .

= (Vz + Vbe) - Vnm where

Vz = zener diode voltage = 6.3V

Vbe = receiving transistor saturation voltage = 0.7 V

Vnm = maximum noise voltage margin = 2 V .

In a noisy environment, the noise margin can be increased by increasing the zener diode voltage for the same value of Vmlz . .

Vmlz = (6.3 + 0.7) - 2 = 5 V

IL is set at the receive / transmit current source to ensure a minimum Vmlz (figure 13) at a wire resistance of 257 OHM which correspondes to the resistance of one mile of twisted pair.

IL = (Vmlz - Vsat) / RW

= (5 - 1.8) / 257 = 12.5 milliampere

IL is set at 12.5 mA with the current source limiting resistor RI .

RI = VRI / IL (figure 14) . where

VRI = voltage accross RI

= (Vx + Vbe -Vy) = 1.2 + 0.7 - 0.7 = 1.2 V

RI = current source current setting resistance .

IL = line current

RI = 1.2 V / 12.5 MA = 96 OHM

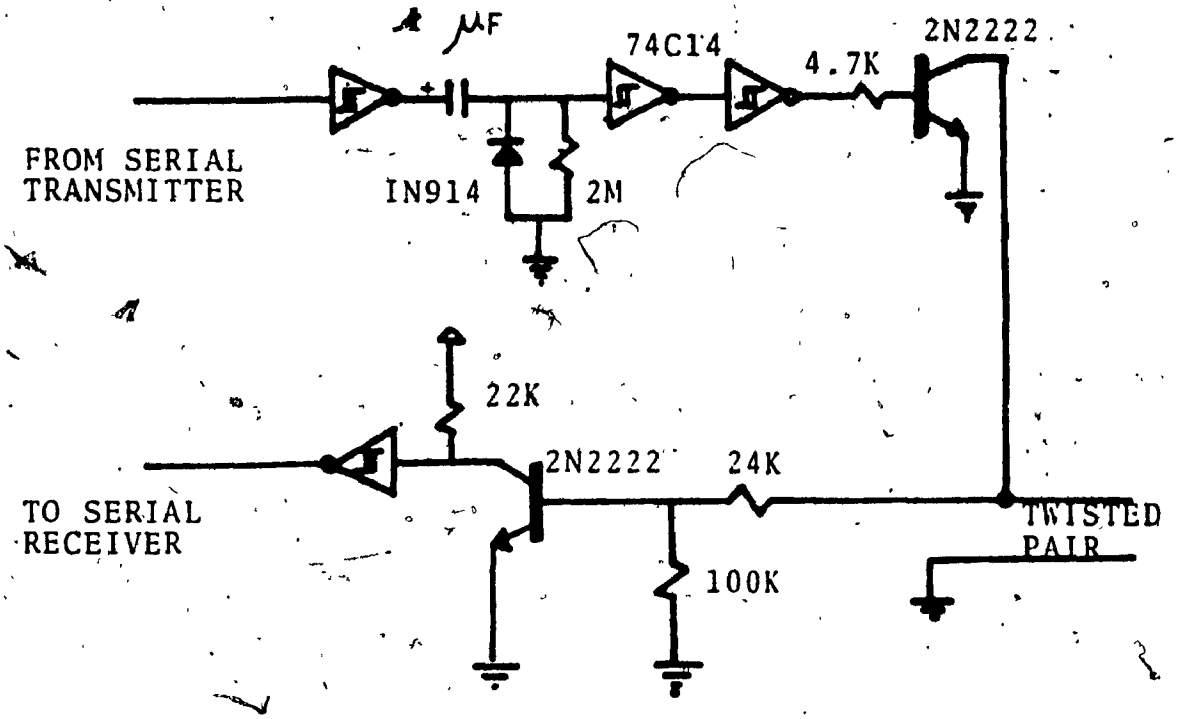


FIGURE (11) OPEN LINE TRANSMISSION
LINE DRIVERS
REMOTE MICROCOMPUTER SIDE

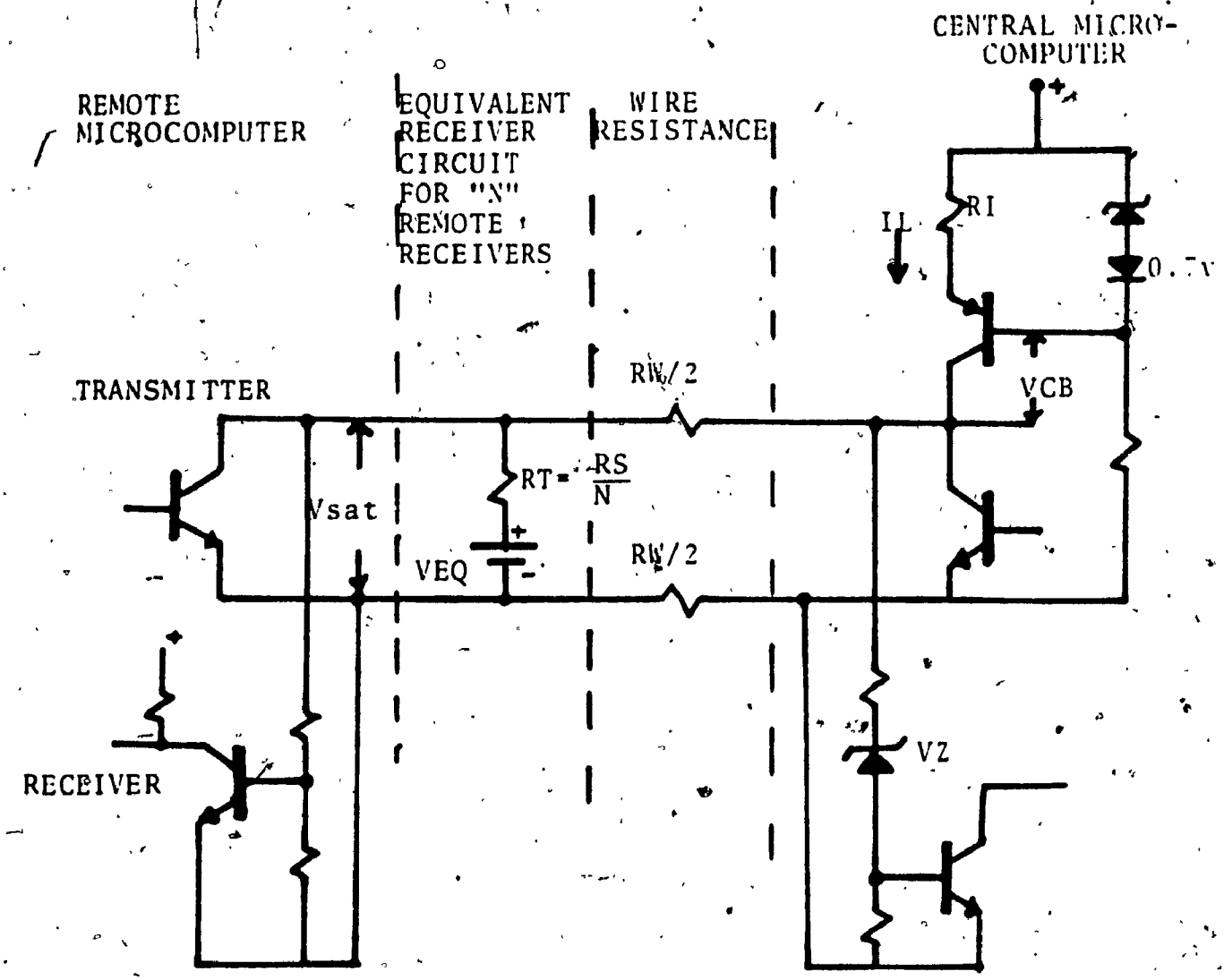


FIGURE (12) RECEIVER/TRANSMITTER TRANSMISSION LINE EQUIVALENT CIRCUIT.

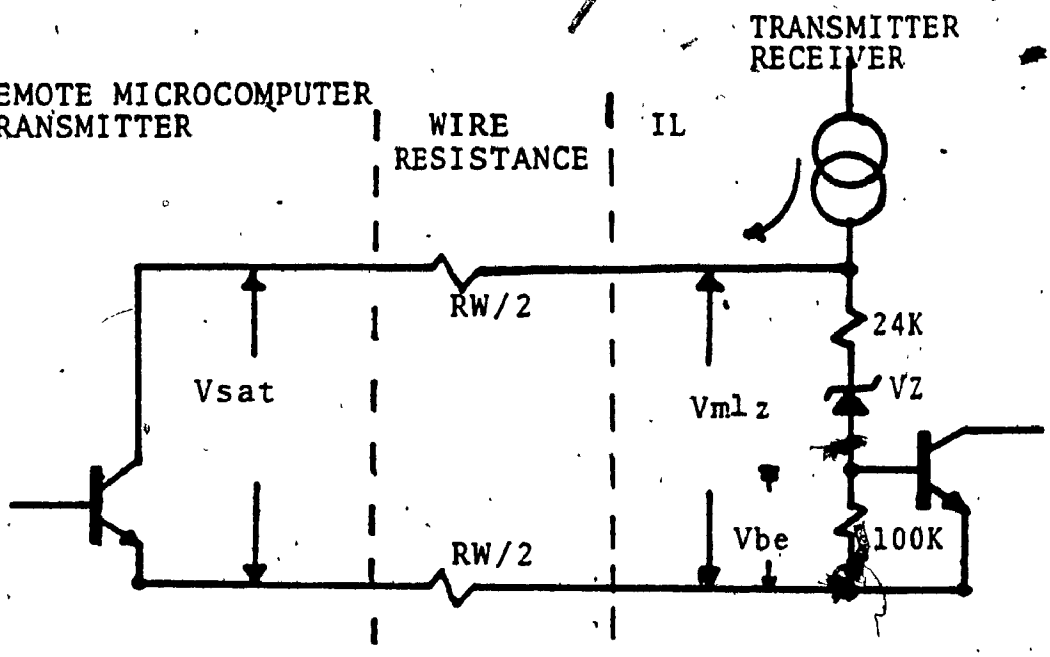


FIGURE (13) CURRENT LOOP EQUIVALENT CIRCUIT

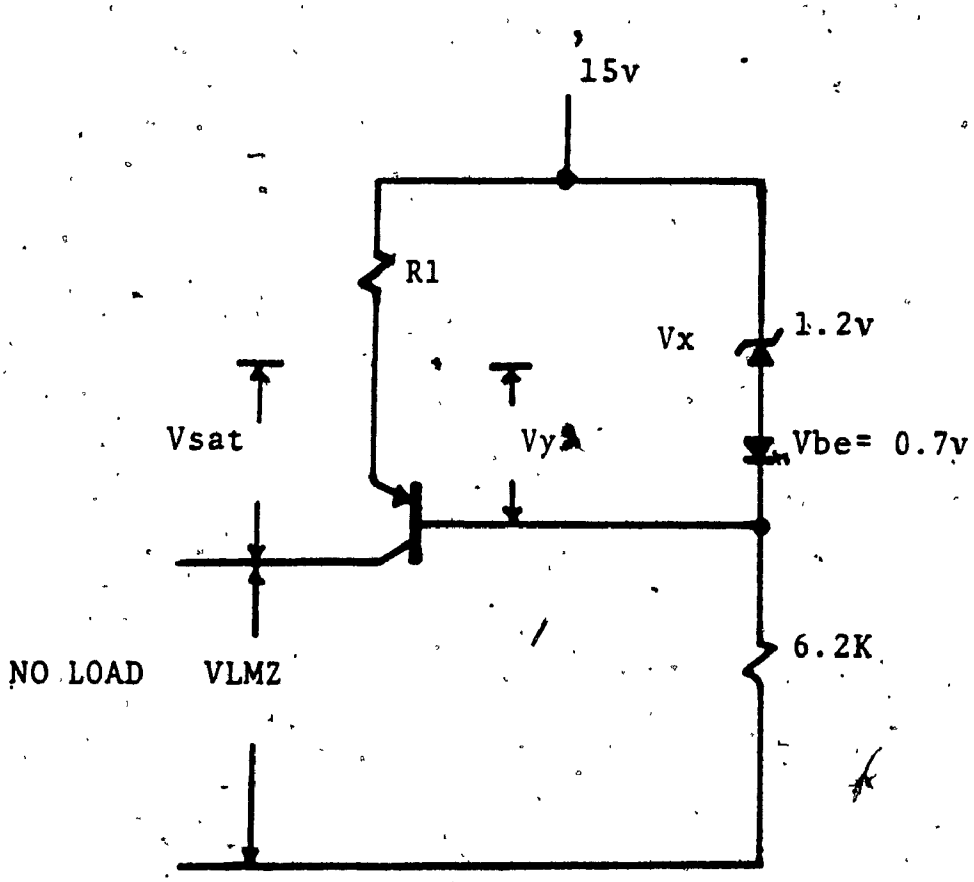


FIGURE (14) NO LOAD LINE VOLTAGE EQUIVALENT CIRCUIT

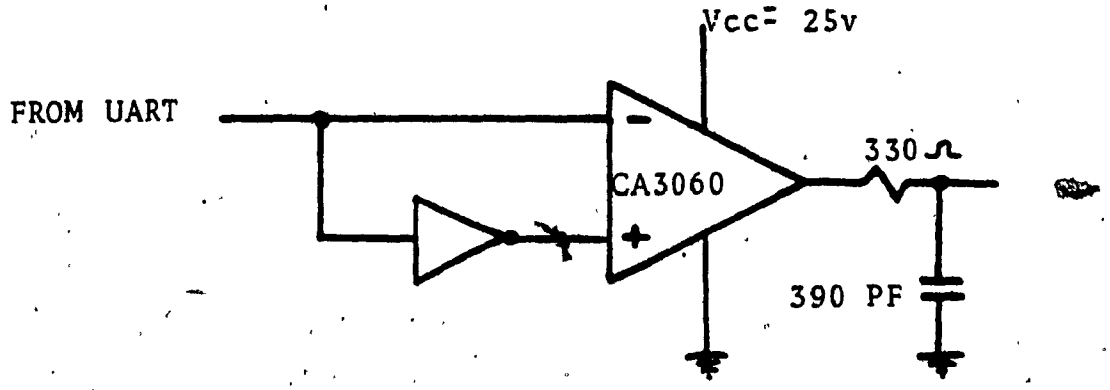
6.4 Maximum Number of Remote Stations

There are two factors which determine the maximum number of remote station , Nmax, the total line current , IL and the receive transistor base current which is usually very small . As stated before in the open loop approach , the maximum number of remote stations is limited to 128 which yields a base transistor current of about 80 microampere , enough to switch a medium gain transistor of the type 2N2222.

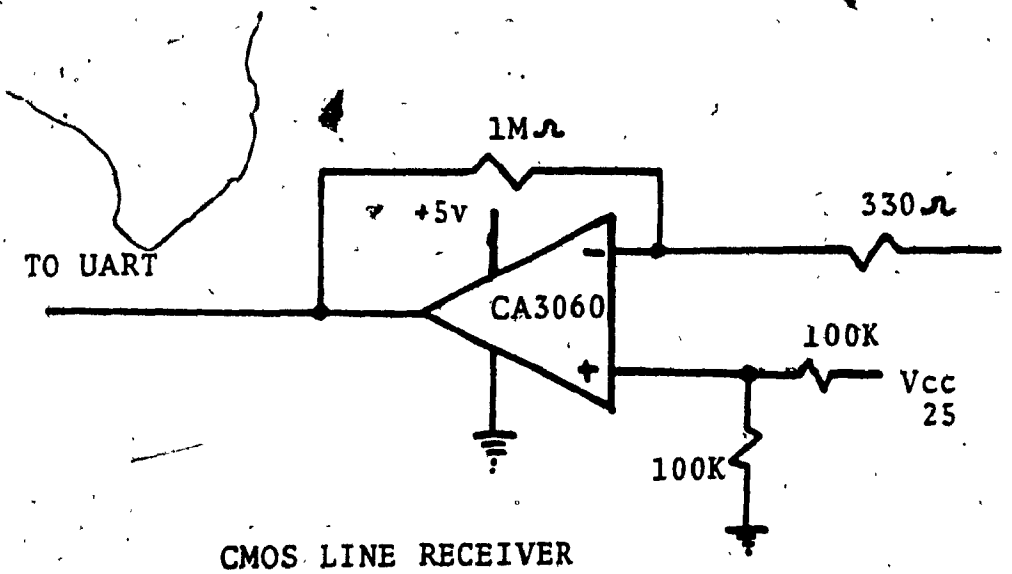
6.5 Closed Loop Line Drivers

In the case of the closed loop, the problem of the long distance between stations is less severe because the loop length is divided amongest several remote stations which means that the individual transmission lines between stations are very short , thus reducing their capacitance, hence allowing a high rate of transmission. Due to this relaxation of environment demand , the line driver will be a CMOS line driver which will utilize a CMOS operational amplifier acting as a comparator switching from power supply rail to rail (between 25 V and ground) which should give a high noise immunity . The line receiver will be a CMOS comparator biased to one half the power supply (25 V / 2 = 12.5 V) with a small amount of hystrises for better noise

immunity . Figure (15) showes a typical circuit for the line driver and the line receiver .



CMOS LINE DRIVER



CMOS LINE RECEIVER

FIGURE (15) CLOSED LOOP LINE DRIVERS AND RECEIVERS

CHAPTER 7

MESSAGE DEFINITION

7.1 Introduction

In this chapter we will define the messages exchanged between the central microcomputer and the remote microcontroller . The messages defined below will be based on the open line approach and can be easily adapted to the closed loop approach. Figure (16) illustrates the message structure in the time domain.

7.2 Central station to remote station

Table 4 illustrates the message structure . Bit 1 of byte 1 is zero indicating that the flow of data is from the central station to a remote station whose I.D code is contained in the following 7 bits (bit 2 to bit 8). The first 3 bits of the second byte contain the message length which in this case will be 2 except for turn output on command which will be 3 . The next 5 bits of the second byte are the command code , yielding 32 available commands . However only 6 commands are utilized for the time being . Except for turn output on command ,the third byte will be the check sum byte .The fourth byte will be the check sum byte in case of turn output on command.

7.2.1 Command Code

The Central station sends to the remote stations six different commands summerized as follows :

1- Reset and reinitialize

This command is issued after power up or if the central station detected bus errors and syncronization is required .

2- Go to sleep mode

This command is issued if the A.C supply failed and the whole system is running on batteries . The effect of this command is to reduce the power consumption of the remote station in order to increase battery life.

3- Wake up

This command is issued either when the A.C supply is restored or during sleep mode when the central station requires the occasional detection of loop activity . After the central station receives the information it needs, it commands the remote station to go back to sleep mode again if the system is still running on batteries.

4- Send status

This command is issued to get the staus of the detectors and also the alarm devices , so the central station can process the loop information .

5- Cut detector power

This command is used to cut power to the detector to unlatch its SCR and return to normal condition. The detector SCR latches into alarm condition when it detects a fire and stays in this alarm condition even after the fire conditions have been cleared until its power is interrupted for a short period of time .

6- Turn output on

This command is issued after detecting a fire or after clearing a fire and the central station processed the loop data and decided that one or more of the outputs associated with this remote station must be turned on or off . These outputs can be buzzers , horns , flashing beacons or magnetic door release . This command is followed by another byte . Each bit in this byte controls one output (a 1 means output should be turned on while a 0 means output should be turned off).

Bit # 1 : Controls supervised output # 1 .

Bit # 2 : Controls supervised output # 2 .

Bit # 3 : Controls supervised output # 3 .

Bit # 4 : Controls unsupervised output # 1 .

Bit # 5 : Controls unsupervised output # 2 .

Bit # 6 : Controls unsupervised output # 3 .

Bit # 7 : Controls unsupervised output # 4 .

Bit # 8 : Controls unsupervised output # 5 .

7.3 Remote station to central station

The remote station transmits to central station only when it is instructed to send status . Otherwise it just executes the command sent by the central station . Table 5 illustrates the message structure .

Bit 1 byte 1 is one indicating that the direction of transmission is from the remote station , whose I.D number is contained in the following 7 bits , to the central station .

The first 3 bits of the second byte has the message length which is 6. The next 5 bits indicate the status of the 5 unsupervised inputs (bit 3 has input 1 status , bit 4 has input 2 status ,etc) . A 1 reading indicates that the input switch is not active (an open switch) while a 0 reading indicates an active switch (a closed switch).

Bits one and two of byte 3 indicate detector # 1 status, bits 3 and 4 indicate detector 2 status , bits 5 and 6 indicate detector 3 status , bits 7 and 8 indicate detector 4 status , while bits one and two of byte 4 indicate detector # 5 status . The status code is shown below .

ODD BIT	EVEN BIT	STATUS
0	0	detector is in short circuit
1	0	detector is in alarm condition
0	1	detector is normal condition
1	1	detector is in open circuit

Bits 3 and 4 of byte 4 indicate supervised output # 1 status ,bits 5 and 6 indicate supervised output # 2 status , bits 7 and 8 indicate supervised output # 3 status . The status code is shown below .

ODD BIT	EVEN BIT	STATUS
0	0	output is in short circuit
1	0	output is on .
0	1	output is off
1	1	output is open circuit

TABLE 4

CENTRAL STATION MESSAGE STRUCTURE

Bit 1	Bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8
Direc	----------	I.D	Number	----------			
--Message Length--		----------		Command Code		----------	
-- Second Command Byte Required only for output turn on --							
Check Sum Byte							

TABLE 5

REMOTE STATION MESSAGE STRUCTURE

Bit 1	Bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8
Direc	----------	I.D Number					
-- Message Length --		-- U.S.I # 1 - U.S.I # 5 status --					
Det. 1 status		Det. 2 status		Det. 3 status		Det. 4 st.	
Det. 5 status		S.O 1 status		S.O 2 status		S.O 3 st.	
-- not used --		-- U.S.I # 1 - U.S.I # 5 status --					
Check Sum Byte							

S.O = Supervised output

U.S.O = Unsupervised output

U.S.I = Unsupervised input

For a definition of supervised and unsupervised inputs and outputs refer to 5.2

7.4 Message Timing

From the previous discussion it is clear that the longest message between the central station and the remote station is when status is requested , which is 3 bytes for the command and 6 bytes for the response , a total of 9 bytes and since each byte consists of 11 bits (8 data , 1 parity , 2 stop bits) the total message length is 99 bit long and assuming that the transmission speed is 9600 BAUD then we can calculate the message time as follows :

MESSAGE TIME = (99 * 1000) / 9600 Millisecond per remote

= 10.3 Millisecond per remote

so if we have the maximum number of remote stations (128) the central station will detect a fire in as fast as 10 Milliseconds if the fire was reported by the first remote or as slow as 1320 Milliseconds if the fire was reported by the last remote .

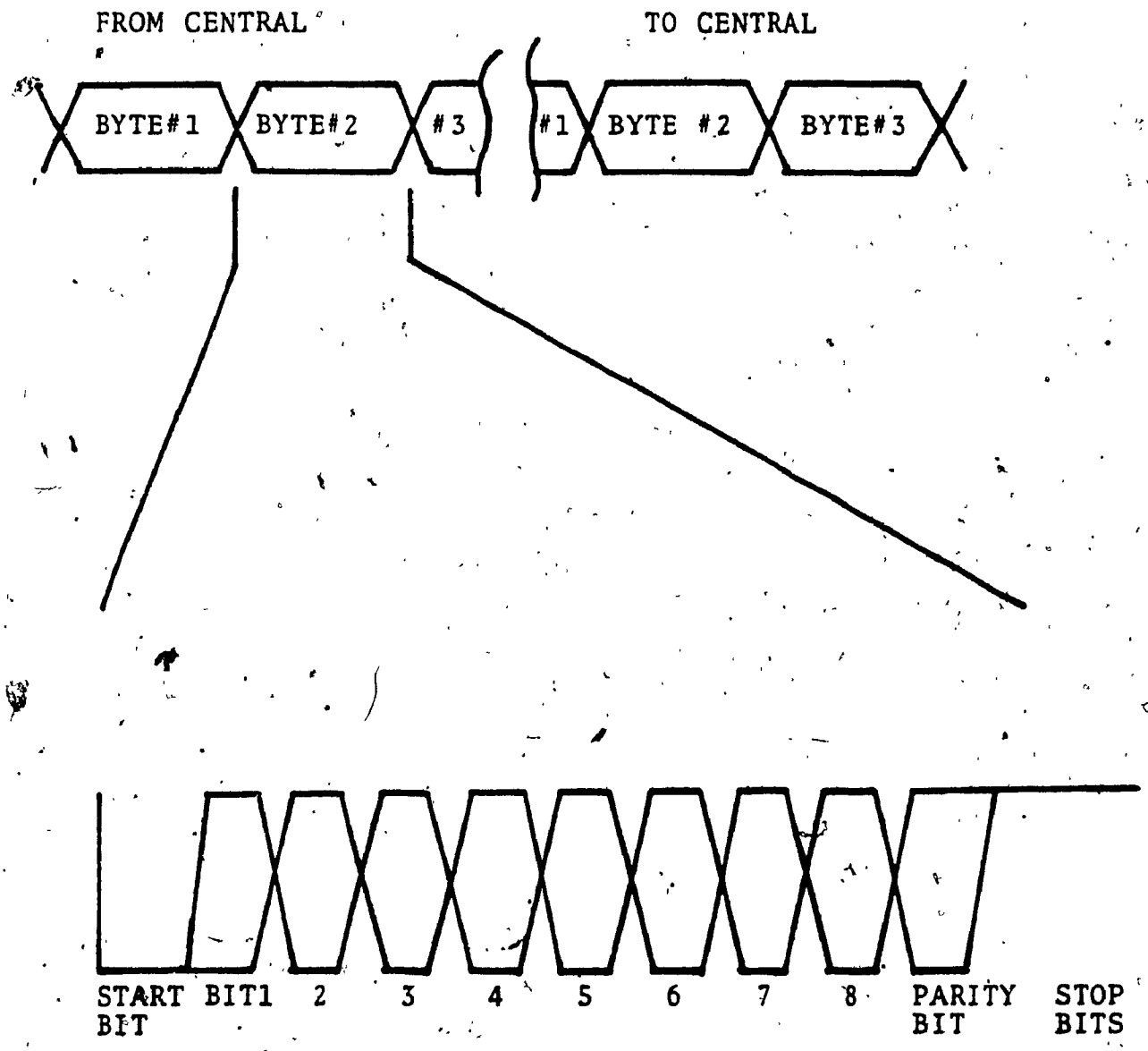


FIGURE (16) MESSAGE TIMING

CHAPTER 8

SOFTWARE CONSIDERATIONS

8.1 Introduction

Almost every project involving programming a computer starts with a flow chart to define steps that have to be taken to solve the problem at hand and this project is no exception . In this chapter we will look at the flow charts used with this project.

8.2 The main loop

Figure (17) illustrates the software used with the remote microcontroller .After power-up the initialization phase starts by disabling all interrupts , loading the stack pointer , initializing the I/O ports , clearing the RAM thus clearing all software counters and setting all flags to the normal condition . For example the wake / sleep mode flag should be set to the wake up mode and the detector power flag should be set to " on " in order to supply power to the detectors.

After the initialization phase the processor executes a continuos loop . First it reads the status of the detectors and stores it in a special RAM area that is reserved for device status . It then reads the output devices status and

saves in RAM then it reads the status of the unsupervised inputs and saves the reading again in RAM .
After reading the status of all the devices connected to the microcontroller , it reads the supervised output command flags from RAM and turns the supervised outputs on or off and then repeats the same procedure for the unsupervised outputs .
The processor then checks the wake / sleep mode flag and if it was set to the wake up mode it executes the same loop again . If , however , the sleep mode flag was set , the processor executes a WAIT instruction which in effect places the processor in a low power mode until it is interrupted by the UART .

8.3 Interrupt Handler Routines

8.3.1 The UART Interrupt

The UART is the main source of interrupt . The flow chart (fig. 18) illustrates how the processor reacts upon being interrupted by the UART . If it was interrupted by the transmitter , the processor loads the transmitter holding register of the UART with a byte from the transmit buffer (provided that the buffer is not empty) and decrements the buffer counter.
If the processor was interrupted by the receiver , then the processor reads the receiver shift register byte and stores

it in the receiver buffer and increments the message counter. If the received byte was the second byte in the message , the message length will be extracted from the first 3 bits . If the received byte was the last byte , then the message counter is cleared to get ready for the next message and the message checked for errors . If the message was error free , then the command will be executed , or else the message is ignored .

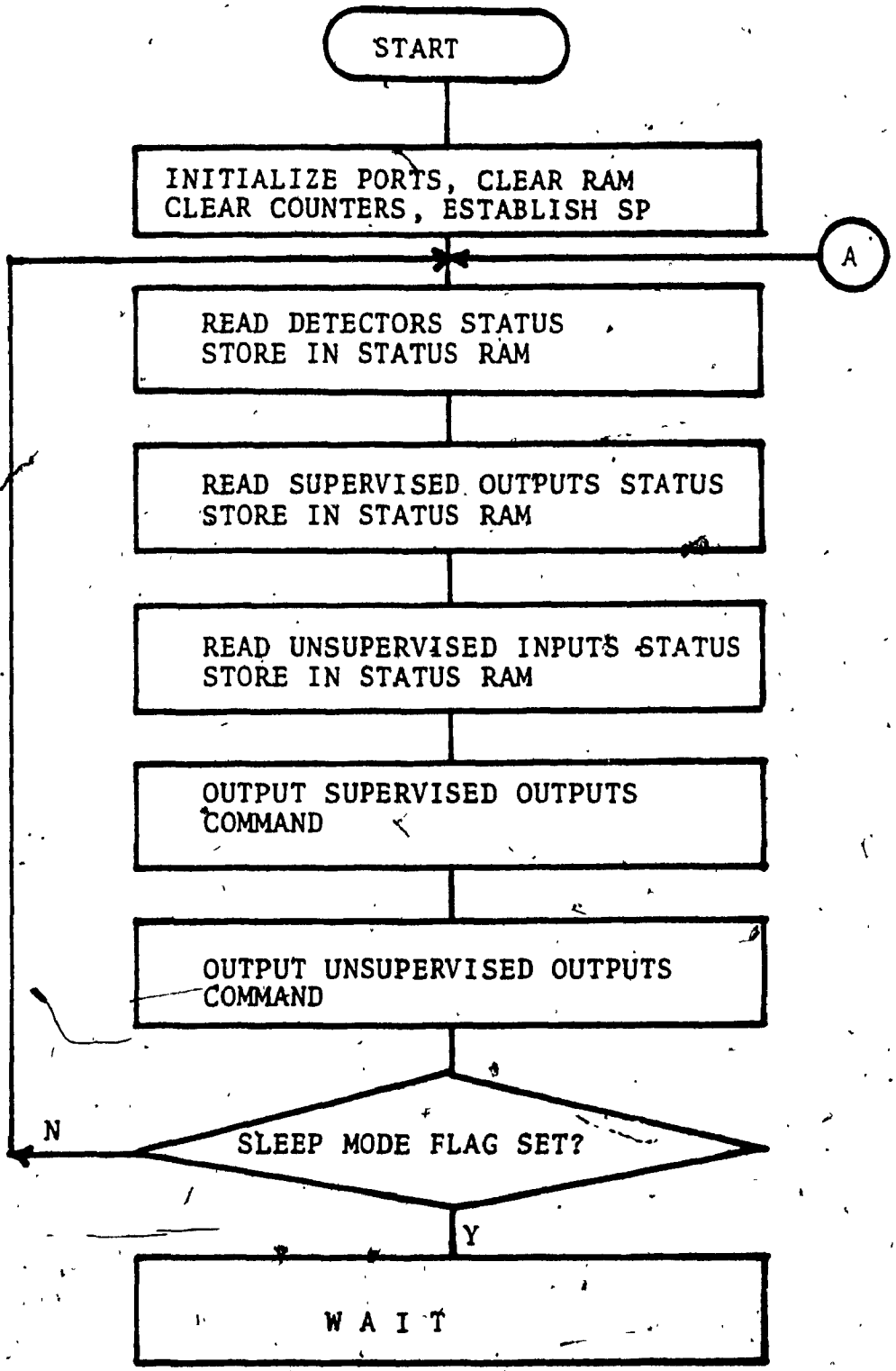


FIGURE (17) MAIN LOOP FLOWCHART

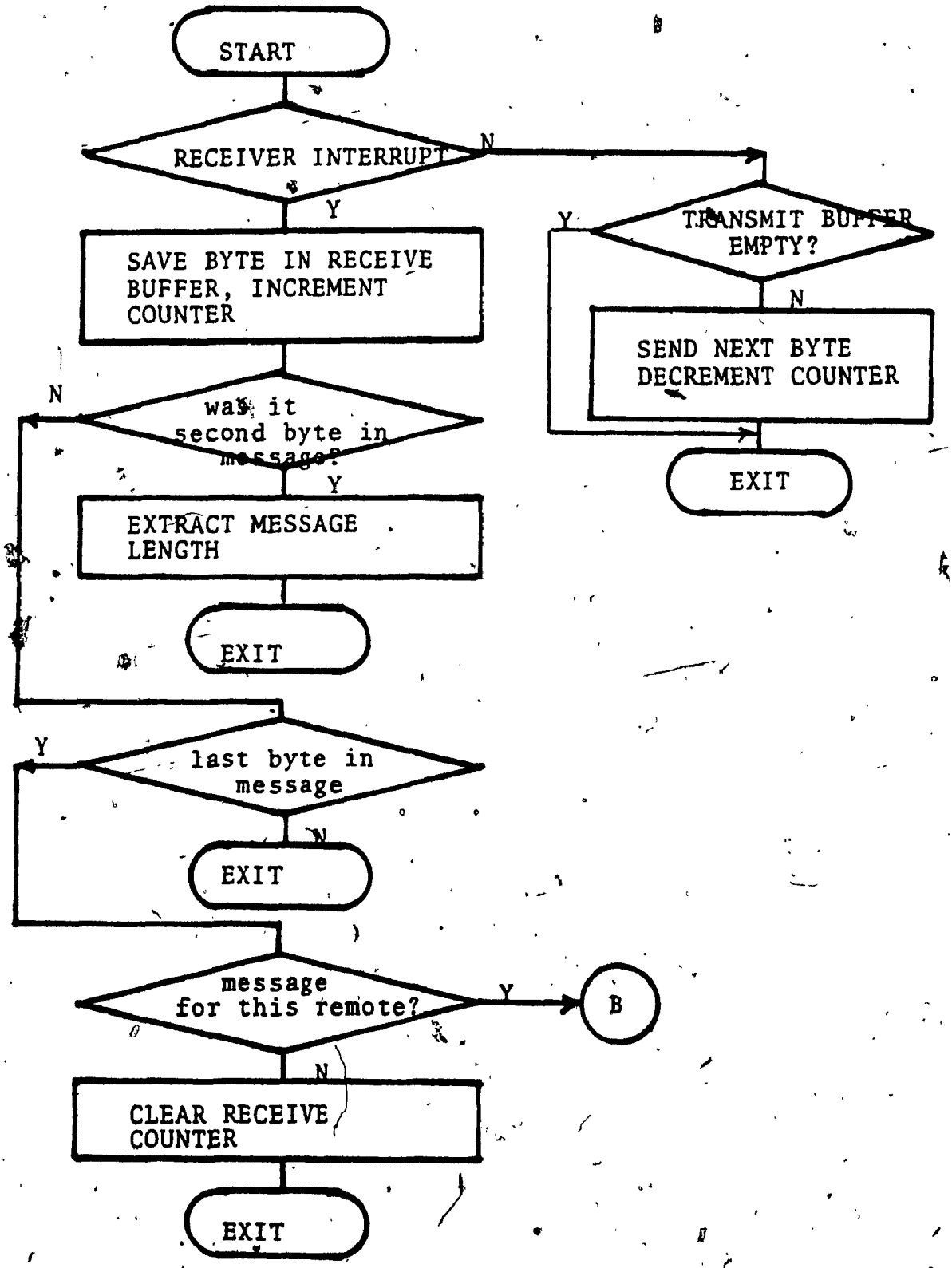


FIGURE (18) UART INTERRUPT PROCESSING

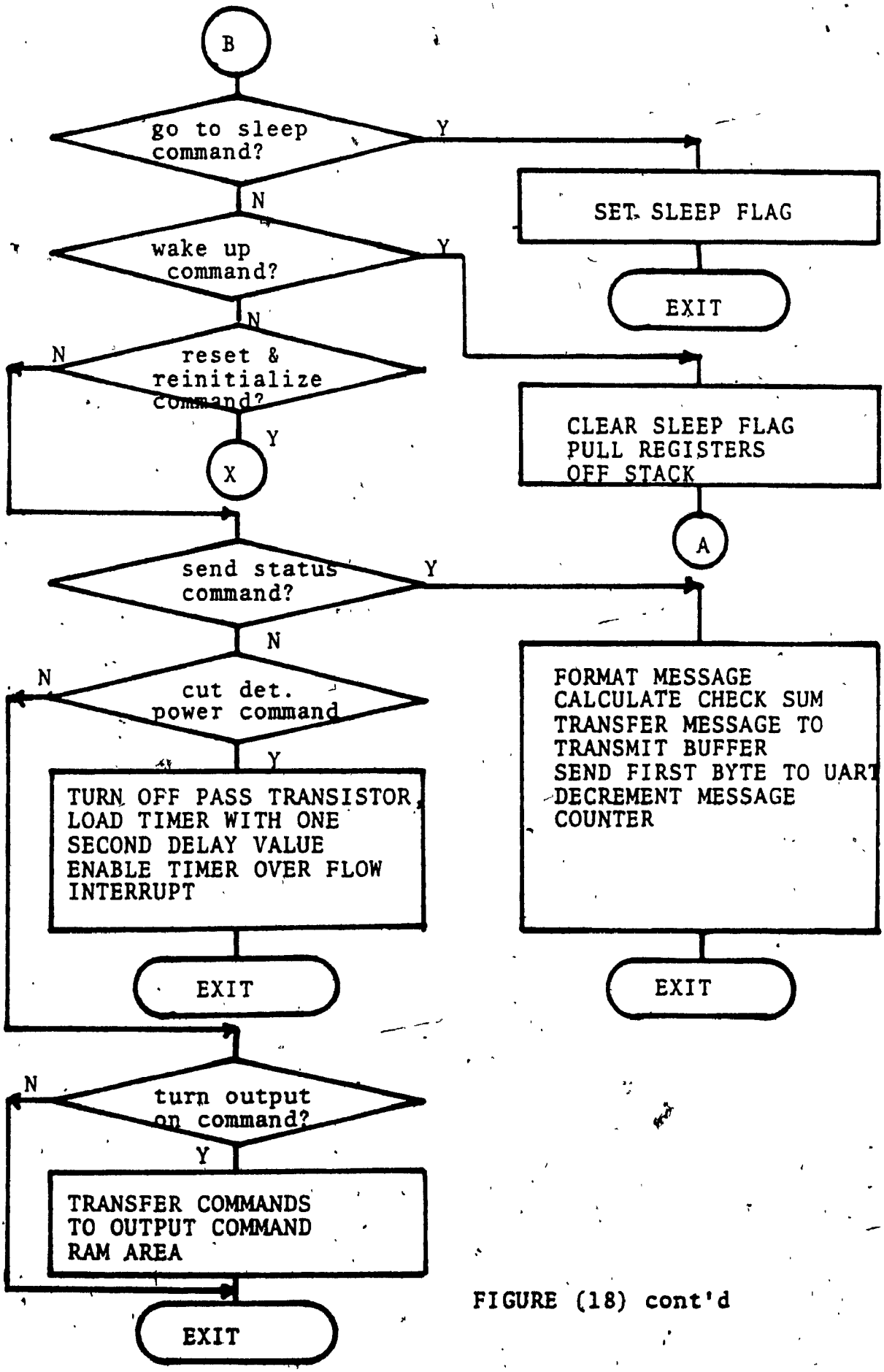


FIGURE (18) cont'd

8.3.2 Command Execution

1- Go to Sleep Mode

The wake / sleep flag bit is set indicating that the processor is in sleep mode .

2- Wake up

The wake / sleep flag bit is cleared indicating that the processor is awake.

3- Reset and Reinitialize

The program jumps to the initialization phase .

4- Send Status

The program takes the status information from the status area and formats the message , calculates the check sum byte then transfers the message to the transmitter buffer area . It then loads the transmitter holding register of the UART with the first byte of the message and decrements the buffer counter.

5- Transfer Output Command

The program transfers the commands from the receiver buffer to the RAM area reserved for output flags .

6- Cut Detector Power

The program turns off the pass transistor thus cutting off power to the detectors and loads the timer with a one second delay value , then enables the timer overflow interrupt. See timer overflow interrupt for more details.

8.3.3 Timer Overflow Interrupt Handler

The timer overflow interrupt flow chart is shown in figure 19. The timer over flow interrupt handler turns on the pass transistor thus supplying power to the detectors and ending the one second interruption of detectors power . It also disables the timer overflow interrupt .

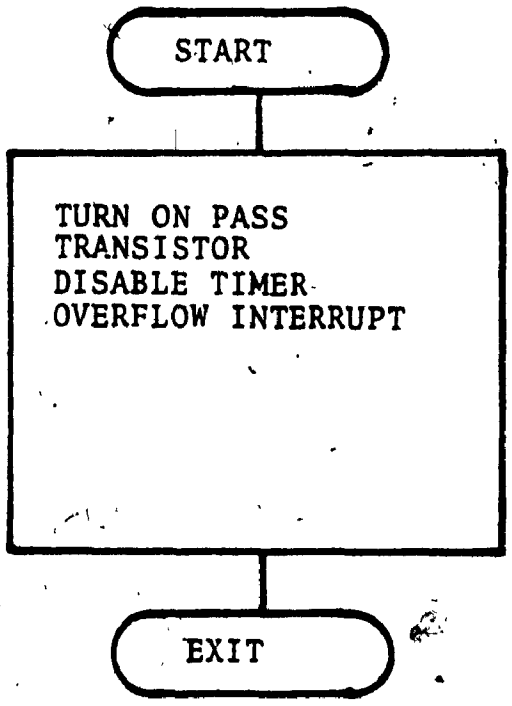


FIGURE (19) TIMER OVERFLOW INTERRUPT PROCESSING

CHAPTER 9

A PRACTICAL EXAMPLE

9.1 Introduction

Now that we have discussed the hardware and software aspects of using a single chip microcontroller as an interface device between detectors and other field devices and the central station , let us see how to apply this idea to a real life situation.

9.2 An Example for a Fire Detection System

Let us assume that this system is going to be installed in a 400 room building like the Concordia campus . Let us also assume for the sake of simplicity that there are 10 floors of 40 rooms each and that the 10 floor plans are identical . Figure (20) shows the floor plan (which may not be architecturally attractive or even feasible) and the detectors distribution . Notice that beside the detectors there also are manual pull down stations . These are activated through a human discovery of a fire or imminent danger . The bells serve as the alarm devices in this case . There can be also other alarm devices like flashing beacons or horns but they are not used here.

Figure (21) shows the electronic system which consists of the central microcomputer station , several mimic boards distributed along key locations in the building - like the superintendants office - , a CRT terminal for system fault diagnostics if required and finally the remote stations connected to each other and the central station via a single cable .

9.2.1 The Central Microcomputer

The central microcomputer has the ever popular Z80 microprocessor running at 4 MHZ with sockets for 16 Kbyte of EPROMS to hold the program ,loop and system data and tables. It also has sockets for 8 Kbyte of static RAM to hold flags, intermediate calculations , data received from loop and data to be transmitted to the loop . The memory requirement varies from one system to another depending on the system specifications and complexity . The circuit also has 3 SIO's (Serial Input / Output) for a total of 6 serial communications channels . The first 4 serial communications channels are dedicated to the four mimic boards while the fifth serial channel communicates with the diagnostics terminal and the sixth serial channel is reserved for communication with the remote stations .

9.2.2 The Mimic Board

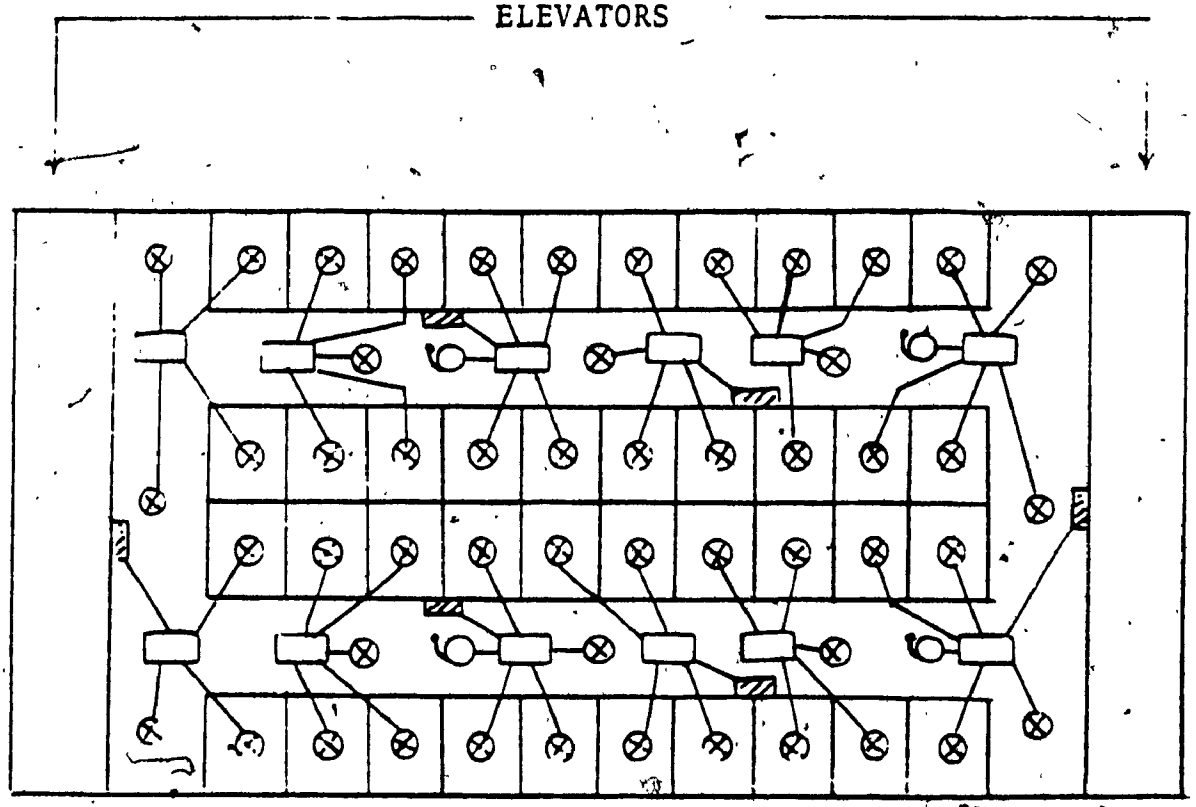
The mimic board is a simple yet very effective way of pin pointing the location of a fire or a fault.Figure (22) is such a mimic board . Each floor plan is silk screened on a black panel . LED 's indicate the location of the detectors and the pull down stations . If a detector goes into an alarm condition which is detected by the central station , the central station sends a command to the mimic boards to flash a common fire LED , turn the buzzer on and flash the LED corresponding to that detector. This action persists until the fire is acknowledeged via the accept switch of the mimic board indicating that the fire has been detected by the people in charge . When the accept switch is activated , all flashing lights turn steady and the buzzer is turned off.

From figure (21) notice that the mimic board has its own Z80 microprocessor since it can be located far away from the central station .

9.2.3 The Remote Stations

By counting the detectors and pull down stations in figure (20) We find 58 of these devices, requiring 12 remote stations (5 detectors per remote station) yielding a total of 120 remote stations well within the 128 maximum remote station per loop . If , however , more than 128

remotes are required in any system an additional loop can be added provided that the central station software was written to accomodate more than one loop .



DETECTOR

BELL

MANUAL PULL DOWN STATION.

REMOTE STATION

FIGURE (20) FLOOR PLAN AND DETECTORS DISTRIBUTION

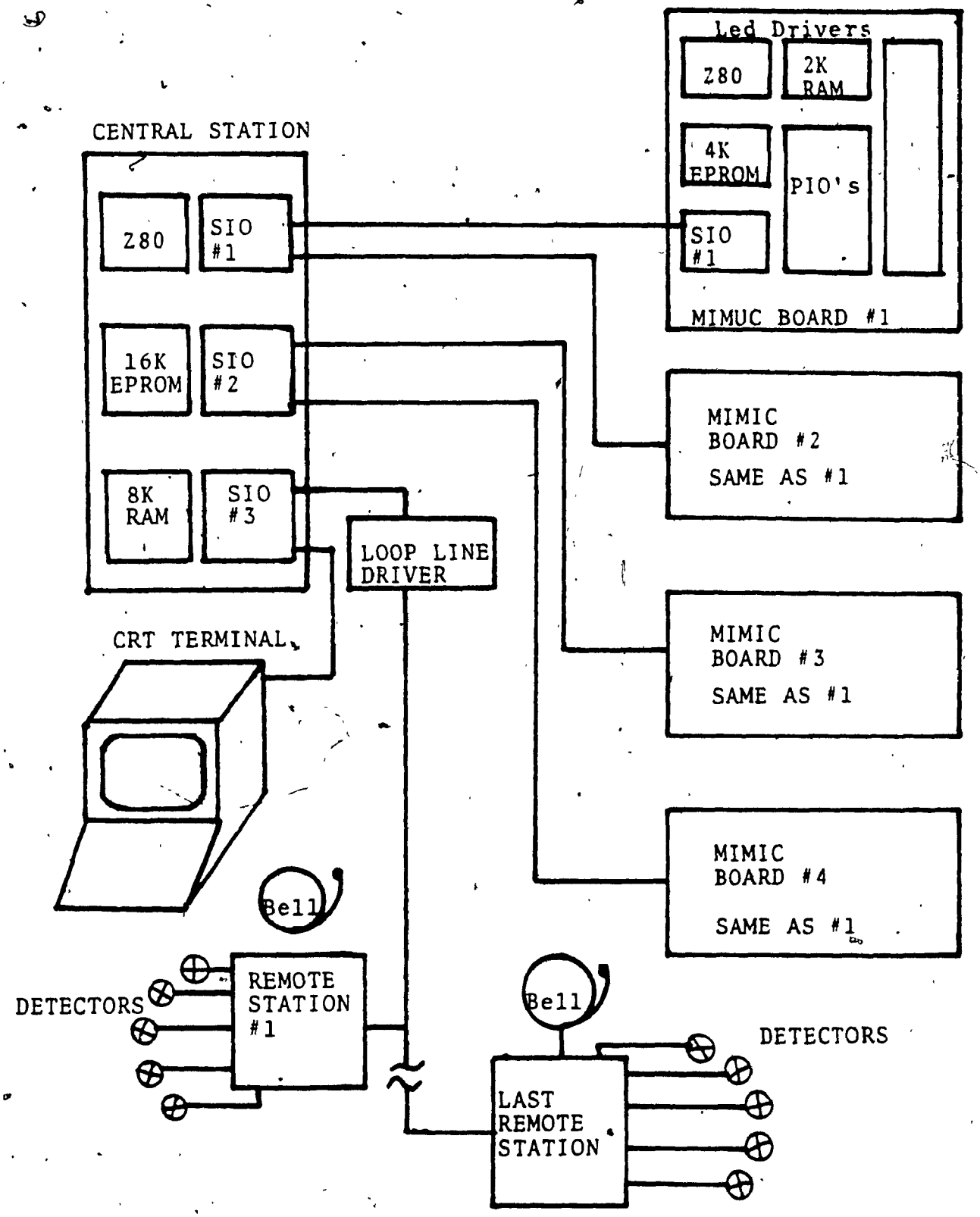


FIGURE (21) SYSTEM ARCHITECTURE

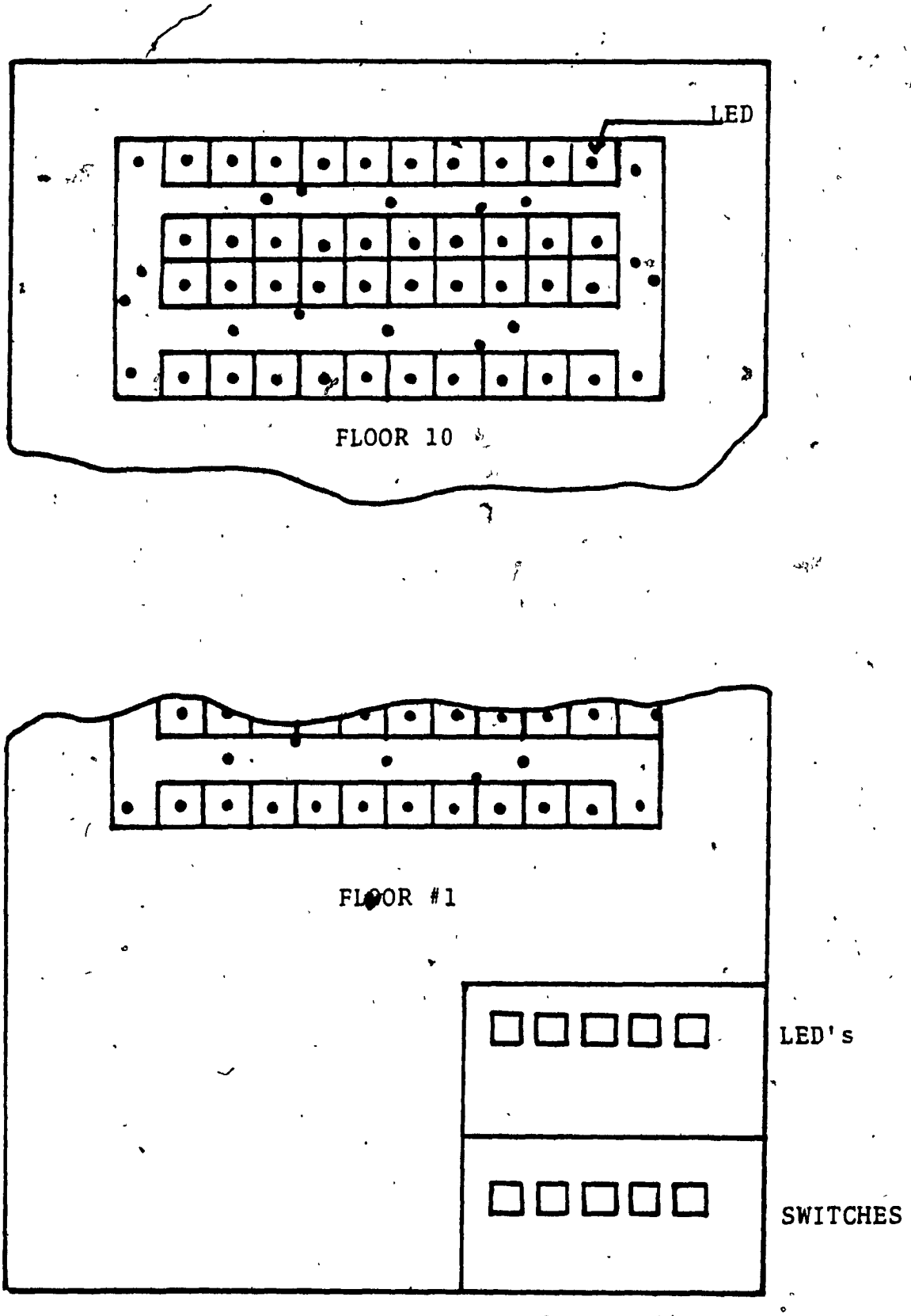


FIGURE (22) MIMIC BOARD

CHAPTER 10

CONCLUSION

In this report the idea of using a single chip microcomputer to interface remote fire detectors with a centralized microcomputer has been investigated and a circuit based on this idea was designed . There was no attempt to build the actual system due to the prohibitive cost involved . The idea is very sound and not only cost effective but it contributes to the system intelligence , a requirement that is demanded more and more from customers in this field . For the sake of simplicity , this report touched only on the very basic idea . What the system designer can do with this approach is only limited by his or her imagination . The very same idea can also be applied to a multitude of remote data acquisition systems that involve analog signal processing .

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5. The Motorola 68HC11A4 microprocessor data sheets .
6. The Intel 80C51 microprocessor data sheets .
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13. The INTERSIL COMPANY DEMDACS Evaluation Kit Technical Manual

APPENDIX 1

THE 68HC11A4 DATA SHEETS

MOTOROLA

SEMICONDUCTORS

MC68HC11A4

Product Preview

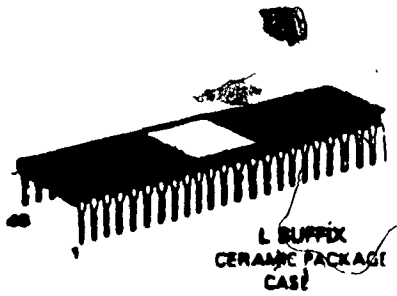
HCMOS
(HIGH-DENSITY HIGH-PERFORMANCE SILICON GATE)

MICROCOMPUTER

MC68HC11A4 8-BIT MICROCOMPUTER

The HCMOS MC68HC11A4 is an advanced microcomputer (MCU) containing highly sophisticated on-chip peripheral functions. An improved instruction set provides additional capability while maintaining compatibility with the other members of the M6801 Family. The fully static design allows operation at frequencies down to dc, further reducing its already low power consumption. Features available in addition to the normal M6801 features include

- 4K Bytes of ROM
- 512 Bytes of EEPROM
- 256 Bytes of RAM (All Saved During Standby)
- Enhanced 16-Bit Timer System
  - Four Stage Programmable Prescaler
  - Three Input Capture Functions
  - Five Output Compare Functions
- An 8-Bit Pulse Accumulator Circuit
- An Enhanced Non-Return-To-Zero Serial Communications Interface (SCI)
- A New Serial Peripheral Interface
- Eight Channel 8-Bit A/D Converter
- A Real Time Interrupt Circuit
- A Computer Operating Properly (COP) Watchdog System



L SUFFIX
CERAMIC PACKAGE
CASE

Also Available in
52-Pin Quad Pack

PIN ASSIGNMENT

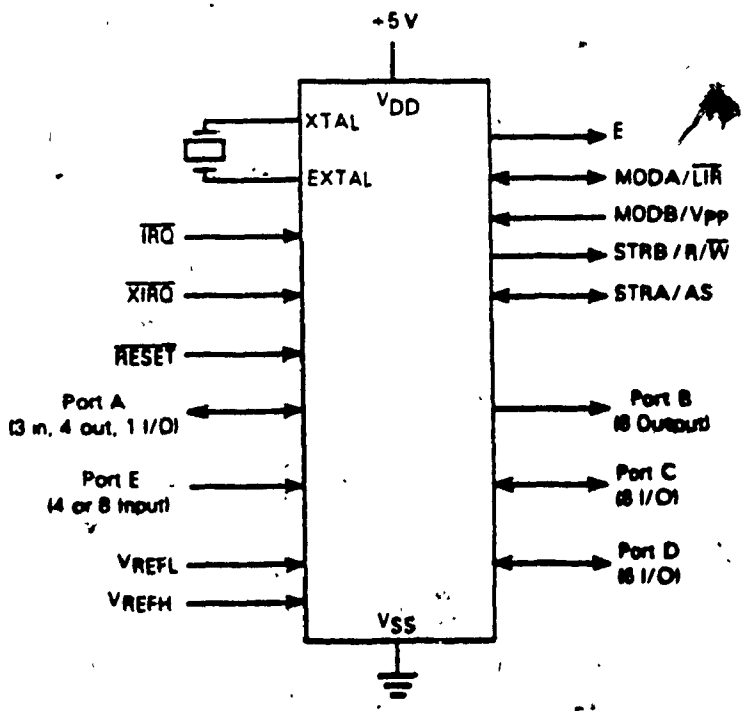
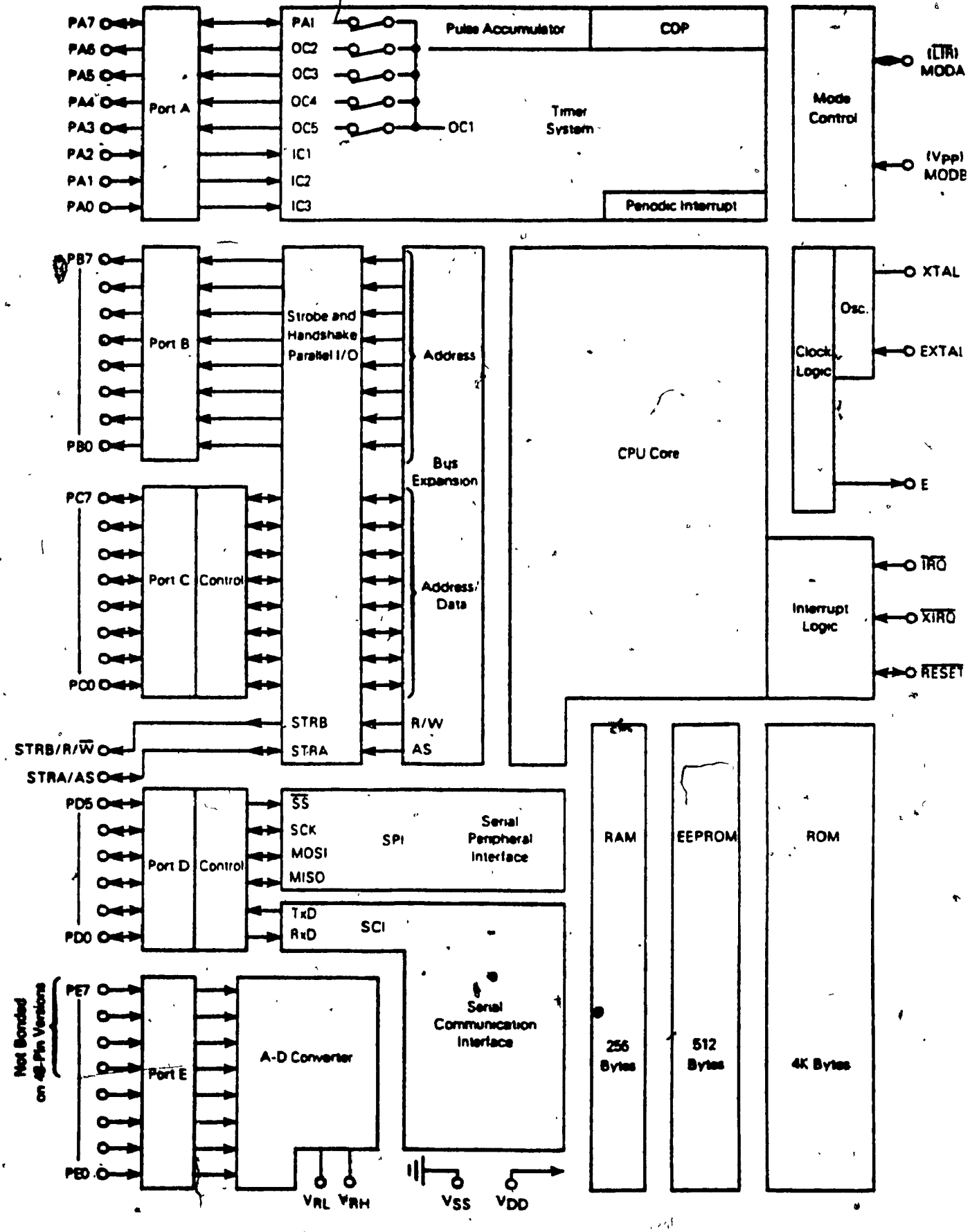


FIGURE 1 – MC68HC11A4 BLOCK DIAGRAM



GENERAL DESCRIPTION

The MC68HC11A4 is a single-chip microcomputer that utilizes HCMOS techniques to provide the low-power characteristics and high noise immunity of CMOS plus the high-speed operation of HMOS. On chip memory systems include a 4K byte ROM, 512 bytes of electrically erasable programmable ROM (EEPROM), and 256 bytes of static RAM. The MC68HC11A4 microcomputer also provides highly sophisticated, on-chip peripheral functions including an 8-channel analog-to-digital converter, a serial communications interface (SCI) subsystem, and a serial peripheral interface (SPI) subsystem.

New design techniques are used to provide a 2 MHz nominal bus rate. The timer system is expanded to provide three input capture lines, five output compare lines, and a real time interrupt circuit. This gives the MC68HC11A4 one of the most comprehensive timer systems found on a single-chip microcomputer. Other features of the MC68HC11A4 include: a pulse accumulator which can be used to count external events (event counting mode) or measure an external period (input gates accumulation of internal clock – E/64), a computer operating properly (COP) watchdog system which helps protect against software failures, a programmable clock monitor system which causes generation of a system reset in case the clock is lost or running too slow; and an illegal opcode detection circuit which provides an unmaskable interrupt if an illegal opcode fetch is detected.

OPERATING MODES

The MC68HC11A4 MCU uses two dedicated pins (MODA and MODB) to select one of two basic operating modes or one of two special operating modes. The basic operating modes are single-chip (mode 0) and expanded multiplexed (mode 1), and the special operating modes are bootstrap and special test. The levels required on the MODA and MODB pins for mode selection are discussed in **FUNCTIONAL PIN DESCRIPTION**. The characteristics of the operating modes are discussed below.

SINGLE-CHIP MODE (MODE 0)

In the single-chip mode the MCU functions as a self-contained microcomputer and has no external address or data bus. In this mode the MCU provides maximum use of its pins for on-chip peripheral functions, and all address and data activity occurs within the MCU. As discussed in **FUNCTIONAL PIN DESCRIPTION**, when MODA = 0 and MODB = V_{DD} the single chip mode is selected during reset.

EXPANDED MULTIPLEXED MODE (MODE 1)

In this mode, two I/O ports plus two additional I/O lines become address, data, and control (AS and R/$\overline{W}$) to allow the MCU to address up to 64K bytes of address space. High order address bits are output on the port B pins. Low order address bits and the data bus are time multiplexed on the eight port C pins, port D bit 6 becomes the address strobe (AS) control output which is used in demultiplexing the low order address from the data at port C. The R/$\overline{W}$ control pin (port D, pin 7) is used to control the direction of data transfers on the port C bus. Refer to **FUNCTIONAL PIN DESCRIPTION** and **INPUT/OUTPUT PORTS** for additional information regarding address strobe, read/write, port B, and port C.

BOOTSTRAP MODE

The bootstrap mode is considered a special mode as distinguished from the normal operating single-chip mode. In the bootstrap mode, all vectors are fetched from the 128 byte on-chip boot loader ROM. This is a very versatile mode since there are essentially no limitations on the special purpose program that is boot loaded into the internal RAM. The boot loader is contained in 128 bytes of ROM which is enabled as internal memory space at $BF80-$BFFF. The boot loader contains a small program which reads a 256 byte program into on-chip RAM ($0000-$00FF). After the character for address $00FF is received, control is automatically passed to that program at memory address $0000 and the MCU operates in the single-chip mode.

In the bootstrap mode, the serial receive logic is initialized by software in the boot loader ROM. This allows the program control of the serial communications interface (SCI) baud and word format.

During initialization of the special bootstrap mode, a special control bit is configured to permit access to a number of special test control bits which allows for self testing of the MCU in the bootstrap mode. Also, since the mode control bits can be written to, the operating mode of the MCU may be changed from the special bootstrap mode (which is a single chip mode by default) to expanded multiplexed mode under program control.

TEST MODE

The test mode is considered a special mode as distinguished from the normal operating expanded multiplexed mode, however, it is considered as operating in the expanded multiplexed mode since external memory may be addressed. The reset vector is fetched from external memory space $BFFE-$BFFF; therefore, program control may be vectored to an external test program.

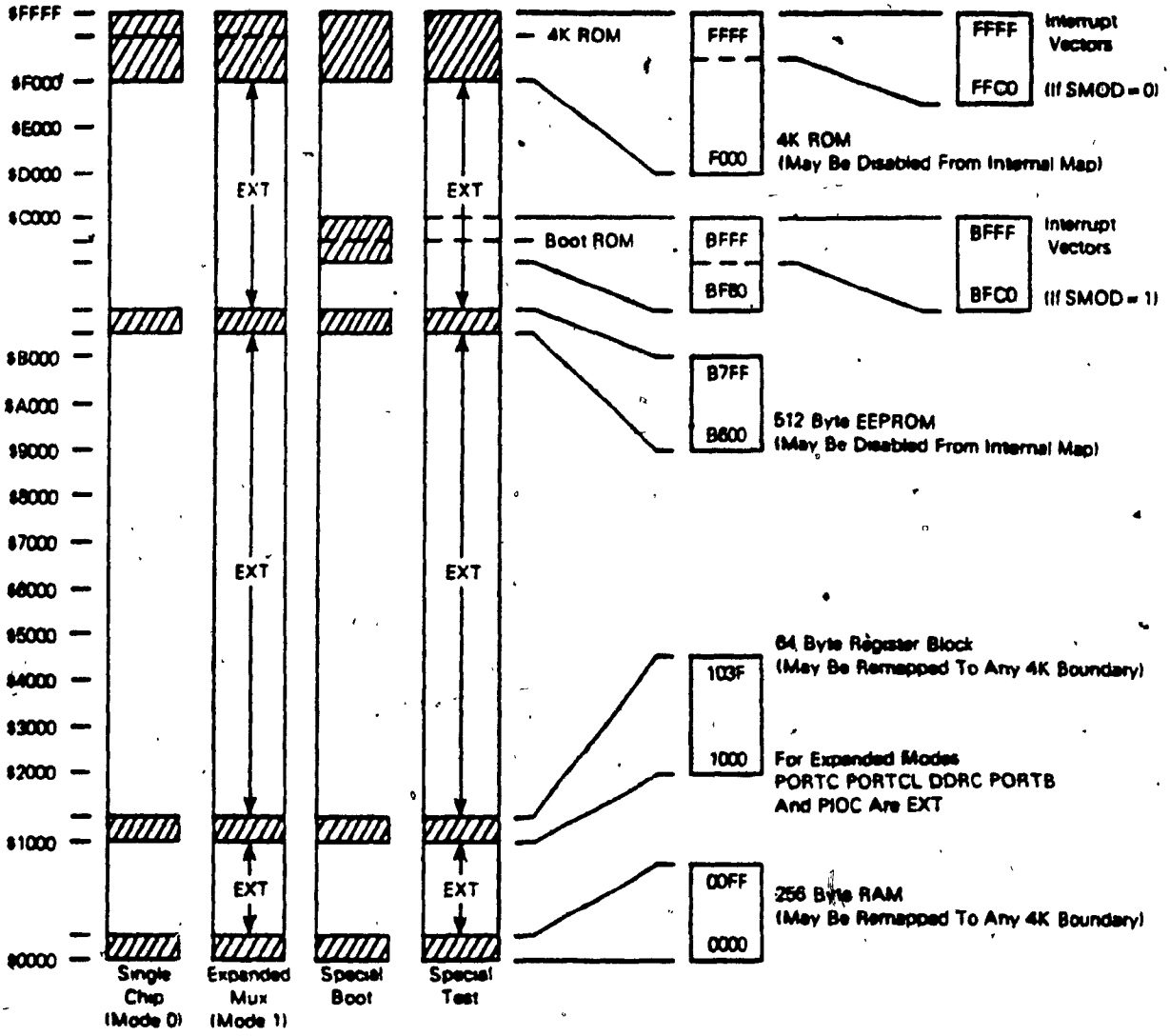
The test mode is primarily intended as the main production test mode at the time of manufacture, however, it may also be used to program calibration or personality data into the internal EEPROM (electrically erasable programmable read only memory) of the MC68HC11A4. During initialization of the test mode, a special control bit is configured to permit access to a number of special test control bits. Also, since the mode control bits can be written to in the test mode, the operating mode of the MCU may be changed from the special test mode (which is an expanded multiplexed mode by default) to the single chip mode under program control.

MEMORY

Composite memory maps for each MC68HC11A4 mode of operation are shown in Figure 2. These modes include single-chip, expanded multiplexed, special boot, and special test.

In the single-chip mode (mode 0) of Figure 2, the MC68HC11A4 does not generate external addresses. The actual internal memory locations are shown in the shaded areas of Figure 2 and the contents of these shaded areas are

FIGURE 2 — MC68HC11A4 MEMORY MAPS



shown on the right side of the diagram. For example, memory locations $0000 through $00FF contain the 256 bytes allocated to RAM, memory locations $1000 through $103F are allocated for a 64-byte register block; memory locations $B600 through $B7FF are allocated for a 512-byte EEPROM (electrically eraseable programmable read only memory); and memory locations $F000 through $FFFF are allocated for 4K bytes of ROM (memory locations $FFC0 through $FFFF are reserved for the interrupt and reset vectors).

The expanded multiplexed mode (mode 1) memory locations shown in Figure 2 are basically the same as for the single-chip mode; however, the memory locations between the shaded areas (designated EXT) are for externally addressed memory and I/O.

The special bootstrap mode memory locations are similar to the single-chip memory locations except that a special bootstrap program is addressed at memory locations $BF80 through $BFFF. The special bootstrap program controls the process of boot loading a 256 byte program through a serial port into internal RAM.

The special test mode memory locations are similar to the expanded multiplex mode except the interrupt vectors are at external memory locations.

CENTRAL PROCESSING UNIT

The central processing unit (CPU) of the MC68HC11A4 is basically an extension of the MC6801 CPU. In addition to being able to execute all MC6800 and MC6801 instructions, the MC68HC11A4 uses a 4-page opcode map to allow execution of 91 new opcodes. As in the MC6801, the CPU of the MC68HC11A4 is implemented independently from the I/O,

memory, or on-chip peripheral configurations. Consequently, this CPU can be treated as an independent processor communicating with these internal subsystems when operating in the single-chip mode. However, when the MC68HC11A4 is operating in the extended multiplexed mode, it is capable of addressing external memory and peripherals in addition to communicating with the on-chip subsystems.

The MC68HC11A4 CPU has seven registers available to the programmer as shown in Figure 3. The interrupt stacking order is shown in Figure 4. The seven registers are discussed below.

FIGURE 3 — MC68HC11A4 PROGRAMMING MODEL

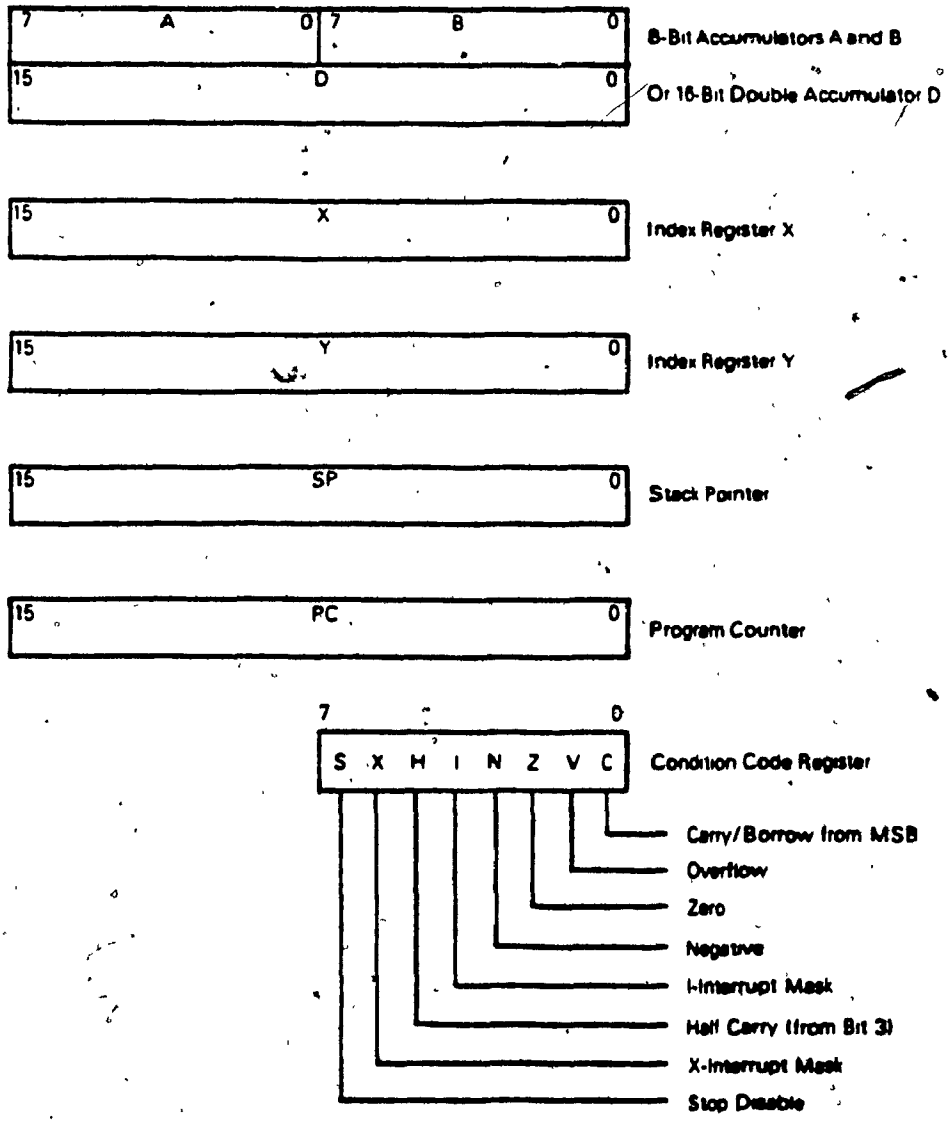
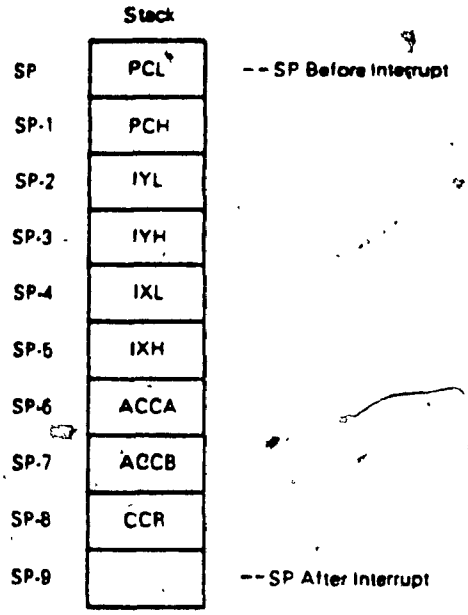


FIGURE 4 — INTERRUPT STACKING ORDER



ACCUMULATOR A AND B

Accumulator A and accumulator B are general purpose 8-bit registers used to hold operands and results of arithmetic calculations or data manipulations. As in the MC6801, these two accumulators can be concatenated into a single double-byte accumulator called the D accumulator.

INDEX REGISTER X (IX)

The 16-bit IX register is used during indexed modes of addressing. It provides a 16-bit indexing value which may be added to an 8-bit offset provided in an instruction to create an effective address. The IX register can also be used as a counter or as a temporary storage area.

INDEX REGISTER Y (IY)

The 16-bit IY register is also used during indexed modes of addressing similar to the IX register, however, most instructions using the IY register require an extra byte of machine code and a cycle of execution time since they are two byte opcodes. The IY register can also be used as a counter or as a temporary storage in the same manner as the IX register.

STACK POINTER (SP)

The stack pointer (SP) is a 16-bit register that contains the address of the next free location on the stack. The stack is configured as a sequence of last-in-first-out read/write registers which allow important data to be stored during interrupts and subroutine calls. Each time a new byte is added to the stack (a push), the SP is decremented; whereas, each time a byte is removed from the stack (a pull) the SP is incremented. The address contained in the SP also indicates the location at which the accumulators (A and B), IX, and IY can be stored during certain instructions.

PROGRAM COUNTER (PC)

The program counter is a 16-bit register that contains the address of the next instruction to be executed.

CONDITION CODE REGISTER (CCR)

The condition code register is an 8-bit register in which each bit signifies the results of the instruction just executed. These bits can be individually tested by a program and a specific action can be taken as a result of the test. Each individual condition code register bit is explained below.

Carry/Borrow (C)

The C bit is set if there was a carry or borrow out of the arithmetic logic unit (ALU) during the last arithmetic operation. The C bit is also affected during shift and rotate instructions.

Overflow (V)

The overflow bit is set if there was an arithmetic overflow as a result of the operation; otherwise, the V bit is cleared.

Zero (Z)

The zero bit is set if the result of the last arithmetic, logic, or data manipulation was zero; otherwise, the Z bit is cleared.

Negative (N)

The negative bit is set if the result of the last arithmetic, logic, or data manipulation was negative (b7 of result equal to a logic one); otherwise, the N bit is cleared.

I Interrupt Mask (I)

The I interrupt mask bit is set either by hardware or program instruction to disable (mask) all maskable interrupt sources (both external and internal).

Half Carry (H)

The half carry bit is set to a logic one when a carry occurs between bits 3 and 4 of the arithmetic logic unit during an ADD, ABA, or ADC instruction; otherwise, the H bit is cleared.

X Interrupt Mask (X)

The X interrupt mask bit is set only by hardware (Reset or $\overline{XIRQ}$), and it is cleared only by program instruction (TAP or RTI).

Stop Disable (S)

The stop disable bit is set to disable the STOP instruction, and cleared to enable the STOP instruction. The S bit is program controlled. The STOP instruction is treated as no operation (NOP) if the S bit is set.

FUNCTIONAL PIN DESCRIPTION

The below pin descriptions do not include the I/O ports. They are discussed separately under INPUT/OUTPUT PORTS.

V_{DD} AND V_{SS}

Power is supplied to the MC68HC11A4 using these two pins. V_{DD} is power input (+5 V) and V_{SS} is the power return path.

RESET

This active low bi-directional control pin is used as an input to initialize the MC68HC11A4 to a known start-up state, and as an open-drain output to indicate an internal failure has been detected in either the clock monitor or computer operating properly (COP) circuit.

XTAL, EXTAL

These two inputs provide for an interface with either a crystal input or a CMOS compatible clock to control the MC68HC11A4 internal clock generator circuitry. The frequency applied to these pins should be four times the desired internal clock rate since an internal divide-by-four circuit determines the actual E-clock rate. When a crystal is used, a 25 picofarad capacitor should be connected between V_{SS} and each of these two pins (XTAL and EXTAL), however, if a CMOS compatible external clock is used, the signal should be connected to the EXTAL pin and the XTAL pin should be left disconnected.

E

The E pin provides an output for the internally generated E-clock which can be used as a timing reference. The frequency of the E output is actually one fourth that of the input frequency at the XTAL and EXTAL pins. In general when the E pin is low, an internal process is taking place and, when high, data is being accessed. This output becomes inactive during the power-saving wait mode if the MC68HC11A4 is operating in the single-chip or bootstrap modes (see MODA/$\overline{LIR}$, MODB/Vpp description below).

$\overline{IRQ}$

The $\overline{IRQ}$ pin provides a means for requesting asynchronous interrupts to the MC68HC11A4. The $\overline{IRQ}$ interrupt input is program selectable with a choice of either negative edge-sensitive or level-sensitive triggering. The $\overline{IRQ}$ interrupt input is always configured to level-sensitive triggering during reset. The $\overline{IRQ}$ pin requires an external resistor to V_{DD}. The MCU completes the current instruction before responding to an interrupt request on the $\overline{IRQ}$ pin.

If $\overline{IRQ}$ is low and the interrupt mask bit (I bit) in the condition code register is clear, the MCU begins an interrupt sequence at the end of the current instruction.

$\overline{XIRQ}$

The $\overline{XIRQ}$ pin provides a means for requesting asynchronous non-maskable interrupts to the MC68HC11A4, after a power-on reset. During reset (including power-on reset), the X bit in the condition code register is set and the $\overline{XIRQ}$ interrupt is masked to preclude interrupts on this line until MCU operation is stabilized. The X bit may then be cleared by program control (using the transfer accumulator A instruction, TAP); however, the X bit can only be set again by reset or by recognition of a hardware $\overline{XIRQ}$ interrupt. Once the X bit in the condition code register is cleared, an interrupt on the $\overline{XIRQ}$ pin will be serviced as soon as the MCU completes the current instruction. When an $\overline{XIRQ}$ interrupt is recognized, on-chip hardware automatically sets the X bit. The X bit can be cleared either as part of interrupt routine by the TAP instruction (nested interrupt) or by the return from interrupt instruction. The $\overline{XIRQ}$ pin requires an external resistor to V_{DD}.

The $\overline{XIRQ}$ input may also be used to return the MCU to normal operation from the low-power stop mode by applying a low level to the $\overline{XIRQ}$ pin. If the X bit in the condition code register is cleared and the MCU is in the stop mode, a low input on the $\overline{XIRQ}$ brings the MCU out of the stop mode and operation resumes with the stacking operation leading to service of the $\overline{XIRQ}$ request. If the X bit is set and the MCU is in the stop mode, a low input on the $\overline{XIRQ}$ brings the MCU out of the stop mode and operation resumes with the program instruction following the STOP instruction.

MODA/$\overline{LIR}$, MODB/Vpp

These pins have alternate functions, MODA and MODB controlling one function, Vpp controlling an alternate function, and $\overline{LIR}$ used for an alternate function.

MODA, MODB

During reset these two pins are used to control the two basic operating modes of the MC68HC11A4 plus two special operating modes. The modes versus MODA and MODB inputs are shown in the table below.

MODB	MODA	Mode Selected
V_{DD}	0	Single-Chip (Mode 0)
V_{DD}	1	Expanded Multiplexed (Mode 1)
/	0	Special Bootstrap
/	1	Special Test

1 = Logic High
0 = Logic Low
/ = 1.4 Times V_{DD} (or Higher)

Vpp

In addition to the MODA function, the MODA/Vpp pin is also used to supply the programming voltage for programming the internal EEPROM. Changing the voltage applied to this pin after reset has no affect on mode selection.

$\overline{LIR}$

In addition to the MODA function, the MODA/$\overline{LIR}$ pin provides an output as an aid in debugging once reset is completed. The $\overline{LIR}$ pin goes to an active-low during the first E-clock cycle of each instruction and remains low for the duration of that cycle (opcode fetch). Some MC68HC11A4 opcodes are two consecutive bytes long including a page 2 (PG2), page 3 (PG3), or page 4 (PG4) prebyte. For these instructions $\overline{LIR}$ goes low for only the first (prebyte) opcode byte fetch.

NOTE

The $\overline{LIR}$ output will not go low for at least two E-clock cycles after reset because of the reset vector fetch.

V_{REFL}, V_{REFH}

These two pins provide the reference voltage for the analog-to-digital converter.

R/$\overline{W}$/STRB

This pin provides two different functions depending on the operating mode. In single-chip mode the pin provides the STRB (output strobe) function and in the expanded multiplexed mode it provides the R/$\overline{W}$ (read-write) function.

In the single-chip mode the STRB pin acts as a programmable strobe. This strobe can also be used to provide a data acknowledge (handshake) to a parallel I/O device.

In the expanded multiplexed mode the R/$\overline{W}$ (read/write) is used to control the direction of transfers on the external data bus. A low level (write) on the R/$\overline{W}$ pin enables the data bus output drivers to the external data bus. A high level (read) on this pin forces the output drivers to a high-impedance state and data is read from the external bus.

AS/STRA

This pin provides two different functions depending on the operating mode. In single-chip mode, the pin provides the STRA (input strobe) function and in the expanded multiplexed mode it provides the AS (address strobe) function.

In the single-chip mode, the STRA pin acts as a programmable input strobe. This input is also used with STRB and port C for full handshake modes of parallel I/O.

In the expanded multiplexed mode the AS (address strobe) output may be used to demultiplex the address and data signals at port C.

INPUT/OUTPUT PORTS

There are five 8-bit ports on the MC68HC11A4 MCU. All of these ports serve more than one purpose depending on the mode configuration of the MCU. A summary of the pins versus function and mode is provided in Table 1 and discussed in the following paragraphs. Because the port functions are controlled by the particular mode selected, each port is discussed for its function(s) during the mode of operation.

SINGLE-CHIP MODE

In the single-chip mode the MC68HC11A4 functions as a monolithic microcomputer without external address or data buses. In this mode, four of these ports (A, B, C, D) are configured as parallel I/O data ports. Port E can be used for general purpose static inputs and/or analog-to-digital converter channel inputs.

Port A

In all operating modes (including the single-chip mode) port A may be configured for: three input capture functions (IC1, IC2, IC3), four output compare functions (OC2, OC3, OC4, OC5), and a pulse accumulator input (PAI) or a fifth output compare function (OC1).

Each of the input capture pins provide for a transitional input which is used to latch a timer value into a 16-bit read-only register (input capture register). The value latched by an input capture corresponds to the value of the free running counter which is part of the timer system. External devices provide the transitional inputs and internal decoders determine which input transition edge (rising, falling, or either) is sensed.

Each of the output compare pins provide for an output whenever a match is made between the value in the free-running counter (in the timer system) and a value loaded into the particular 16-bit output compare register. The outputs can be used externally to indicate that a certain period of time has elapsed.

When port A pin 7 (PA7) is configured as a pulse accumulator input (PAI), the external input pulses are applied to a pulse accumulator register within the MC68HC11A4.

Each port A pin that is not used for its alternate timer function, as described above, may be used as a general purpose input or output line.

Port B

In the single-chip mode, all of the port B pins are general purpose output pins. During MCU read cycles the levels sensed at the input side of the port B output drivers is read. Port B may also be used in a simple strobed output mode where the STRB (port D bit 7) pulses each time port B is written.

Port C

In the single-chip mode, all port C pins are general purpose input/output pins. Port C inputs can be latched by the STRA input (at port D bit 6). Port C may also be used in full handshake modes of parallel I/O where the STRA input and STRB output act as handshake control lines.

Port D

In the single-chip mode port D bits 0-5 may be used for general I/O or with the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems. Bits 6 and 7 are used as handshake control signals for ports B and C.

Bit 0 is the receive data input (RxD) for the serial communication interface (SCI).

Bit 1 is the transmit data output (TxD) for the SCI.

Bits 2 through 5 are dedicated to the serial peripheral interface (SPI). Bit 2 is the master-in-slave-out (MISO) line; this pin is an input when the SPI is configured as a master device and an output when configured as a slave device. Bit 3 is the master-out-slave-in (MOSI) line; this pin is an output when the SPI is configured as a master device and an input when configured as a slave device. Bit 4 is the serial clock (SCK) and is an output when the SPI is configured as a master and an input when configured as a slave device. Bit 5 is the slave select ($\overline{SS}$) input which receives an active low signal to enable a slave device to accept SPI data.

Bit 6 (STRA) and 7 (STRB) are discussed in FUNCTIONAL PIN DESCRIPTION.

TABLE 1 – PORT SIGNAL SUMMARY

Port-Bit	Single-Chip Modes 0 and Bootstrap Mode	Expanded Multiplexed Mode 1 and Special Test Mode
A-0	PA0/IC3	PA0/IC3
A-1	PA1/IC2	PA1/IC2
A-2	PA2/IC1	PA2/IC1
A-3	PA3/OC5/and-or OC1	PA3/OC5/and-or OC1
A-4	PA4/OC4/and-or OC1	PA4/OC4/and-or OC1
A-5	PA5/OC3/and-or OC1	PA5/OC3/and-or OC1
A-6	PA6/OC2/and-or OC1	PA6/OC2/and-or OC1
A-7	PA7/PAI/and-or OC1	PA7/PAI/and-or OC1
B-0	PB0	A8
B-1	PB1	A9
B-2	PB2	A10
B-3	PB3	A11
B-4	PB4	A12
B-5	PB5	A13
B-6	PB6	A14
B-7	PB7	A15
C-0	PC0	A0/D0
C-1	PC1	A1/D1
C-2	PC2	A2/D2
C-3	PC3	A3/D3
C-4	PC4	A4/D4
C-5	PC5	A5/D5
C-6	PC6	A6/D6
C-7	PC7	A7/D7
D-0	PD0/RxD	PD0/RxD
D-1	PD1/TxD	PD1/TxD
D-2	PD2/MISO	PD2/MISO
D-3	PD3/MOSI	PD3/MOSI
D-4	PD4/SCK	PD4/SCK
D-5	PD5/SS	PD5/SS
D-6	STRA	AS
D-7	STRB	R/$\overline{W}$
E-0	PE0/AN0	PE0/AN0
E-1	PE1/AN1	PE1/AN1
E-2	PE2/AN2	PE2/AN2
E-3	PE3/AN3	PE3/AN3
E-4	PE4/AN4 ##	PE4/AN4 ##
E-5	PE5/AN5 ##	PE5/AN5 ##
E-6	PE6/AN6 ##	PE6/AN6 ##
E-7	PE7/AN7 ##	PE7/AN7 ##

- not bonded in 48-pin versions

Port E

In all operating modes (including the single-chip mode), port E is used for general purpose static inputs and/or analog-to-digital (A/D) channel inputs. Port E should not be read as static inputs while an A/D conversion is actually taking place.

NOTE

On 48-pin packaged versions of the MC68HC11A4, the four most significant bits of port E are not connected to pins.

EXPANDED MULTIPLEXED MODE

In the expanded multiplexed mode, the MC68HC11A4 has the capability of accessing a 64K byte address space. The total address space includes the same on-chip memory address as for single-chip mode plus external peripheral devices. In this mode ports B, C, and bits 6 and 7 of port D are configured as a memory expansion bus.

Port A

In all operating modes (including the expanded multiplexed mode), port A may be configured for three input capture functions (IC1, IC2, IC3), four output compare functions (OC2, OC3, OC4, OC5), and a pulse accumulator input (PAI) or a fifth output compare function (OC1).

Each of the input capture pins provide for a transitional input which is used to latch a timer value into a 16-bit read-only register (input capture register). The value latched by an input capture corresponds to the value of a free running

counter which is part of the timer system. External devices provide the transitional inputs and internal decoders determine which input transition edge (rising, falling, or either) is sensed.

Each of the output compare pins provide for an output whenever a match is made between the value in the free running counter (in the timer system) and a value loaded into the particular 16-bit output compare register. The outputs can be used externally to indicate that a certain period of time has elapsed.

When port A pin 7 (PA7) is configured as a pulse accumulator input (PAI), the external input pulses are applied to a pulse accumulator register within the MC68HC11A4

Each port A pin that is not used for its alternate timer function as described above, may be used as a general purpose input or output line

Port B

In the expanded multiplexed mode, all of the port B pins act as high order address output pins. During each MCU cycle, bits 8 through 15 of the address are output on the PB0-PB7 lines respectively.

Port C

In the expanded multiplexed mode, all port C pins are configured as multiplexed address/data pins. During the address portion of each MCU cycle, bits 0 through 7 of the address are output on the PC0-PC7 lines During the data portion of each MCU cycle (E high), bits 0 through 7 (D0-D7) are bidirectional data pins controlled by the R/$\overline{W}$ signal.

Port D

In the expanded multiplexed mode port D bits 0-5 may be used for general I/O or with the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems. Bits 6 and 7 act as expansion bus control lines AS and R/W respectively.

Bit 0 is the receive data input (RxD) for the serial communications interface (SCI).

Bit 1 is the transmit data output (TxD) for the SCI.

Bits 2 through 5 are dedicated to the serial peripheral interface (SPI). Bit 2 is the master-in-slave-out (MISO) line; this pin is an input when the SPI is configured as a master device and an output when configured as a slave device Bit 3 is the master-out-slave-in (MOSI) line, this pin is an output when the SPI is configured as a master device and an input when configured as a slave device Bit 4 is the serial clock (SCK) and is an output when the SPI is configured as a master and an input when configured as a slave device. Bit 5 is the slave select ($\overline{SS}$) input which receives an active low signal to enable a slave device to accept SPI data.

Bit 6 (AS) and 7 (R/$\overline{W}$) are discussed in FUNCTIONAL PIN DESCRIPTION.

Port E

In all operating modes (including the expanded multiplexed mode), port E is used for general purpose static inputs and/or analog-to-digital (A/D) channel inputs. Port E should not be read as static inputs while an A/D conversion is actually taking place.

NOTE

On 48-pin packaged versions of the MC68HC11A4, the four most significant bits of port E are not connected to pins.

BOOTSTRAP MODE

In the bootstrap mode all I/O port pins function the same as in the single-chip mode. Operational differences are discussed in OPERATING MODES.

TEST MODE

In the test mode all I/O port pins function the same as in the expanded multiplexed mode. Operational differences are discussed in OPERATING MODES.

INTERRUPTS

The MC68HC11A4 MCU interrupts can be generated by any of four different basic methods: (1) by presenting the appropriate external signal; (2) by enabling interrupts from the programmable timer output compare or input capture, serial communication interface, serial peripheral interface timer overflow, pulse accumulator, or parallel I/O; (3) by executing a software interrupt (SWI) instruction; or (4) by detection of an illegal opcode.

The program may also be interrupted by: (1) detection of a timeout in the computer operating properly (COP) circuit, (2) clock monitor detects loss of the E-clock or a low frequency E-clock, or (3) by a reset. The above three methods of interrupting the program result in fetching a reset vector rather than an interrupt vector; however, they do interrupt the program.

When an external or internal (hardware) interrupt occurs, the interrupt is not serviced until the current instruction being executed is completed. Until the current instruction is complete, the interrupt is considered pending. After completion of current instruction execution, unmasked interrupts may be serviced in accordance with an established fixed hardware priority circuit; however, one I bit related interrupt source may be elevated to the highest I bit priority position in the circuit

Seventeen hardware interrupts and one software interrupt (excluding reset type interrupts) can be generated from all of the possible sources. The interrupts can be divided into two basic categories, maskable and non-maskable. In the MC68HC11A4 fifteen of the interrupts can be masked using the condition code register I bit. In addition to being maskable by the I bit in the condition code register, all of the on-chip interrupt sources are individually maskable by control bits. The software interrupt (SWI instruction) is a non-maskable instruction rather than a maskable interrupt source. The last interrupt (external input to the $\overline{XIRQ}$ pin) is considered as a non-maskable interrupt because once enabled, it cannot be masked by software; however it is masked during reset and upon receipt of an interrupt at the $\overline{XIRQ}$ pin. Table 2 provides a list of each interrupt, its vector location in ROM, and the actual condition code register bit that masks it. A discussion of the various interrupts is provided below.

TABLE 2 — INTERRUPT VECTOR ASSIGNMENTS

Vector Address	Interrupt Source	Masked By
FFC0, C1	Reserved	—
FFD4, D5	Reserved	—
FFD6, D7	SCI Serial System	I Bit
FFD8, D9	SPI Serial Transfer Complete	I Bit
FFDA, DB	Pulse Accumulator Input Edge	I Bit
FFDC, DD	Pulse Accumulator Overflow	I Bit
FFDE, DF	Timer Overflow	I Bit
FFE0, E1	Timer Output Compare 5	I Bit
FFE2, E3	Timer Output Compare 4	I Bit
FFE4, E5	Timer Output Compare 3	I Bit
FFE6, E7	Timer Output Compare 2	I Bit
FFE8, E9	Timer Output Compare 1	I Bit
FFEA, EB	Timer Input Capture 3	I Bit
FFEC, ED	Timer Input Capture 2	I Bit
FFEE, EF	Timer Input Capture 1	I Bit
FFF0, F1	Real Time Interrupt	I Bit
FFF2, F3	$\overline{IRQ}$ (External Pin or Parallel I/O)	I Bit
FFF4, F5	$\overline{XIRQ}$ Pin (Pseudo Non-maskable Interrupt)	X Bit
FFF6, F7	SWI	None
FFF8, F9	Illegal Op-Code Trap	None
FFFA, FB	COP Failure (Reset)	None
FFFC, FD	COP Clock Monitor Fail (Reset)	None
FFFE, FF	$\overline{RESET}$	None

TIMER INTERRUPTS

The timer system provides nine of the fifteen interrupt possibilities: five output compare interrupts, three input capture interrupts, and a timer overflow interrupt.

The timer contains five 16-bit output compare registers which are program controlled and may be loaded with a number between $0000-$FFFF. The value in each output compare register is then compared to a 16-bit comparator, which is loaded from the timer free running counter, during each clock cycle. If a match is found between the 16-bit comparator value and the output compare register value, the corresponding output compare flag is set. When the output compare flag is set, a corresponding output compare interrupt may be generated and/or an external output may be generated at the corresponding port A pin(s). Port A outputs PA3 through PA7 are used as output pins for output compare functions OC1 through OC5.

In addition to the five output compare interrupts, the timer also provides for three input capture interrupts. The timer contains three 16-bit latch registers which are used to latch the value of the free running counter (in the timer) when an input capture edge is applied to the corresponding PA0-PA2 pin. The value of the free running counter is latched into the corresponding input capture register and an internal interrupt may be generated. The interrupt routine can then read the storage register and determine the time at which the input capture was detected.

The timer may also provide an interrupt when the free running counter changes value from $FFFF to $0000 (overflow). The 16-bit free running counter repeats this change once fo every 65,536 inputs from a prescaler circuit. The prescaler i programmable for either divide-by-1, divide-by-4, divide by-8, or divide-by-16 of the MCU E-clock. Thus, th prescaler extends the actual range of the free runnin counter and the time between timer overflow interrupts fron 2^{16} to 2^{256} E-clock inputs to the prescaler

REAL TIME INTERRUPTS

The real time interrupt is a maskable interrupt that occur periodically at a rate of $E/2^{13}$, $E/2^{14}$, $E/2^{15}$, or $E/2^{16}$.

EXTERNAL INTERRUPTS

Two external interrupts are accessable using the $\overline{IRQ}$ an the $\overline{XIRQ}$ pins. The $\overline{IRQ}$ interrupt is a maskable interrup while the $\overline{XIRQ}$ interrupt is considered a non-maskable inter rupt; however, the $\overline{XIRQ}$ interrupt is masked during rese and immediately following receipt of an $\overline{XIRQ}$ interrup signal. These interrupts are controlled by the I and X bits i the condition code register as discussed in CENTRAL PRO CESSING UNIT.

SOFTWARE INTERRUPT (SWI)

The software interrupt is executed the same as any othe instruction and will take precedence over interrupts only the other interrupts are masked (I and X bits in the conditior code register set). The SWI instruction is executed similar to other maskable interrupts in that it sets the I bit, CPU registers are stacked, etc.

NOTE

The SWI instruction cannot be fetched as long as another interrupt is pending execution. However, once it is fetched no other interrupt can be honored until the first instruction in the SWI service routine is completed.

SERIAL PERIPHERAL INTERFACE (SPI) INTERRUPT

A serial peripheral interface (SPI) interrupt is generated when a serial data transfer between the MC68HC11A4 and an external device has been completed. This interrupt is masked if the condition code register I bit is set.

SERIAL COMMUNICATIONS INTERFACE (SCI) INTERRUPT

A serial communications interface (SCI) interrupt is generated if any one of the following occurs in the SCI:

1. Transmit data register is empty
2. Transmission of data is complete
3. Receive data register is full or an overflow occurred in the receive data register
4. Idle line detected by receiver

The SCI interrupt is masked if the condition code register I bit is set.

PULSE ACCUMULATOR INTERRUPT

The pulse accumulator contains an 8-bit counter which is program controlled to either count input pulses (event counting) at PA7 or to count internal E/64 clocks subject to an enable signal at PA7 (gated time accumulation). When the counter has an overflow from $FF to $00 a pulse accumulator overflow interrupt is generated provided the I bit in the condition code register is clear.

When the input to the pulse accumulator is a gate input at PA7 for counting internal E/64 clocks, the trailing edge of the gate signal (end of counting cycle) can generate an interrupt. This pulse accumulator input edge interrupt is generated provided the I bit in the condition code register is clear. Refer to PULSE ACCUMULATOR for more information.

PARALLEL I/O INTERRUPT

The parallel I/O subsystem can generate an interrupt which uses the same vector as the $\overline{IRQ}$ interrupt. The purpose of sharing the $\overline{IRQ}$ vector is to allow external emulation of the parallel I/O subsystem in expanded multiplexed modes.

RESETS

The MC68HC11A4 MCU has four possible types of reset: an active low external reset pin ($\overline{RESET}$), a power-on reset function, a computer operating properly (COP) watchdog timer reset, and a clock monitor reset.

$\overline{RESET}$ PIN

The $\overline{RESET}$ pin is used to reset the MCU to provide an orderly software startup procedure. To request an external reset, the $\overline{RESET}$ pin must be held low for eight E_{cyc} (two E_{cyc} if internal resets are not used).

POWER-ON RESET

The power-on reset occurs when a positive transition i detected on V_{DD}. The power-on reset is used strictly fo power turn-on conditions and should not be used to detec any drops in power supply voltage. There is no provision fo power-down reset. If the external $\overline{RESET}$ pin is low at th end of the power-on delay time, the processor remains in th reset condition until $\overline{RESET}$ goes high.

COMPUTER OPERATING PROPERLY (COP) RESET

The MC68HC11A4 MCU contains a watchdog timer whic will time itself out if not reset within a specific time by a pro gram reset sequence. If for any reason the COP watchdo timer is allowed to timeout, it generates an MCU reset whic is functionally similar to pulling the $\overline{RESET}$ pin low.

A control bit, which is implemented in an EEPROM cell o the system configuration register, is used to enable (o disable) the COP reset function. When this bit is clear, th COP reset function is disabled; if set, the COP reset i enabled.

CLOCK MONITOR RESET

The MC68HC11A4 MCU contains a clock monitor circui which measures the E-clock input frequency. If the E clock input rate is high enough, then the clock monitor does no time out. However, if the E clock signal is lost, or its fre quency falls below 200 kHz, then an MCU reset is generated which is functionally similar to pulling the $\overline{RESET}$ pin low.

A read-write control bit, which is implemented in th system configuration options register, is used to enable (o disable) the clock monitor reset. When this bit is clear, th clock monitor reset function is disabled; when set, the clock monitor reset is enabled.

STOP AND WAIT

The MC68HC11A4 MCU contains two programmable low power operating modes; stop and wait. In the wait mode the on-chip oscillator remains active together with othe functions discussed below. In the stop mode, all clocks in cluding the crystal oscillator are stopped.

WAI (WAIT) INSTRUCTION

The WAI instruction places the MC68HC11A4 MCU in a low power consumption (wait) mode. In the wait mode, th internal clock remains active, and the MCU enters one of four different variations of the wait mode. These variations, which depend upon the I bit in the condition register and whether or not the COP circuit is required in the system, in clude: (1) only the CPU turned off; (2) CPU and the E clock output buffer turned off; (3) CPU and timer system turned off; or (4) CPU, E output, and timer system all off.

During the wait mode, the CPU registers are stacked and processing is suspended until a qualified interrupt is detected. The actual qualified interrupt type is dependen upon which of the wait mode variations is selected. Th qualified interrupt(s) required to bring the MCU out of th wait mode for each of the wait mode variations is shown below. In all cases, reset brings the MCU out of the wait mode; however, as in all resets, the system is reset and the start of MCU operation is determined by the reset vector.

Wait Mode Variation	Qualified Interrupt
Only CPU Turned Off	$\overline{IRQ}$, $\overline{XIRQ}$, Any Internal Interrupt
CPU and E Clock Output Buffers Turned Off	$\overline{IRQ}$, $\overline{XIRQ}$, Any Internal Interrupt
CPU and Timer System Turned Off	$\overline{IRQ}$, $\overline{XIRQ}$
CPU, E Clock Output Buffers, and Timer System Turned Off	$\overline{IRQ}$, $\overline{XIRQ}$

STOP INSTRUCTION

The STOP instruction places the MC68HC11A4 MCU in its lowest power consumption mode provided the S bit in the condition code register is clear. In the stop mode all clocks including the internal oscillator are stopped, causing all internal processing to be halted. To exit the stop mode and resume normal processing, a low level must be applied to one of the external interrupt pins ($\overline{IRQ}$ or $\overline{XIRQ}$) or to the $\overline{RESET}$ pin. If an external interrupt is used at the $\overline{IRQ}$ input, it is only effective if the I bit in the condition code register is clear. If an external interrupt is applied at the $\overline{XIRQ}$ input, the MCU exits from the stop mode regardless of the state of the X bit in condition code register; however, the actual recovery sequence differs depending on the X bit. If the X bit is clear, the MCU starts up with the stacking sequence leading to normal service of the XIRQ request. If the X bit is set, then processing will continue with the instruction immediately following the STOP instruction and no $\overline{XIRQ}$ interrupt service routine is requested. As in the wait mode, a low input to the $\overline{RESET}$ pin will always result in an exit from the stop mode and the start of MCU operation is determined by the reset vector.

Since the oscillator is stopped in the stop mode, a restart delay may be required to allow for oscillator stabilization when exiting from the stop mode. If the internal oscillator is being used, this delay is required; however, if a stable external oscillator is being used, a control bit within the MCU may be used (cleared) to bypass the delay. If the delay bypass control bit is clear then the $\overline{RESET}$ pin would not normally be used for exiting the stop mode. In this case, the reset sequence sets the delay control bit and the restart delay will be imposed.

PROGRAMMABLE TIMER SYSTEM

The timer system in the MC68HC11A4 uses a "time-of-day" approach in that all timing functions are related to a single 16-bit free running counter. The free running counter is clocked by the output of a programmable prescaler (divide-by-1, 4, 8, or 16) which is in turn clocked by the MCU E clock. Functions available within the MC68HC11A4 timer include: three input capture functions and five output compare functions.

The capabilities of the programmable timer are obtained using the following registers:

1. Prescaler (divide-by-1, 4, 8, or 16)
2. Free Running Counter (16-bit)
3. Input Capture (three 16-bit registers)
4. Output Compare (five 16-bit registers)
5. Main Timer Control and Status Registers

PRESCALER AND FREE RUNNING COUNTER

The key element in the timer system is a 16-bit free running counter with its associated programmable prescaler (divide-by-1, 4, 8, or 16). The free running counter is clocked by the output of the prescaler which is in turn clocked by the E clock. The free running counter can be read by software at any time without affecting its value since it is clocked and read on opposite half cycles of the MPU E clock. The free running counter is cleared to $0000 during reset and is a read-only register (except in the test or bootstrap mode where this feature is used in factory testing).

The 16-bit free running counter repeats every 65,536 counts (prescaler output) and when the count changes from $FFFF to $0000 a timer overflow flag bit is set. Setting the timer overflow flag bit also generates an internal interrupt if the overflow interrupt enable bit is set.

Input Capture Functions

There are three separate 16-bit read-only input capture registers which are not affected by reset. Each of these registers is used to latch the value of the free running counter when a selected transition at an external pin is detected. External devices provide the inputs on the PA0, PA1, PA2 pins, and an interrupt can be generated when an input capture edge is detected. The time of detection can be read from the appropriate register as part of the interrupt routine.

Output Compare Functions

There are five separate 16-bit read/write output compare registers which are initialized to $FFFF at reset. The value written into the output compare register is compared to the free running counter value during each MCU E clock cycle. If a match is found between the two values, the particular output compare flag bit is set and an interrupt is generated provided that particular interrupt is enabled.

In addition to the interrupt, a specified action may be initiated at a timer output pin(s). For OC1, the output action to be taken, when a match is found, is controlled by a 5-bit mask register and a 5-bit data register. The 5-bit mask register specifies which timer port outputs are to be affected and the 5-bit data register specifies the data to be placed on the affected output pins. For OC2 through OC5, one specific timer output is affected as controlled by four 2-bit fields in a timer control register. Specific actions include (1) timer disconnect from output pin logic, (2) toggle output compare line, (3) clear output compare line to zero, or (4) set output compare line to one.

PULSE ACCUMULATOR

The pulse accumulator is an 8-bit counter that can operate in either of two modes depending on the state of a control bit. These include the event counting mode or the gated time accumulation mode.

The pulse accumulator control register contains four bits which enable and configure the pulse accumulator system. One bit enables the counter. One bit determines whether the

PA7/PAI pin will be an input or an output. A third bit specifies the event counting mode or the gated time accumulation mode, and the fourth bit determines which edge of the PAI input is the active one. The 8-bit counter counts from $00 to $FF and when it overflows from $FF to $00 a flag bit is set. This results in a hardware interrupt provided the pulse accumulator overflow interrupt enable bit is set.

In the event counting mode, the 8-bit counter is clocked to increasing values by an external (PAI) pin input (PA7). In the gated time accumulation mode, the 8-bit counter is clocked to increasing values by the MCU E clock (divided-by-64) provided the proper gating signal is applied to an external (PAI) pin input (PA7).

SERIAL COMMUNICATIONS INTERFACE (SCI)

The serial communications interface (SCI) allows the MC68HC11A4 to be efficiently interfaced with peripheral devices that require an asynchronous serial data format. The SCI in the MC68HC11A4 is provided with a standard NRZ format with a variety of baud rates. The baud rate is derived from the crystal clock circuit and interface with peripheral devices is accomplished using port D pins PD0 for receive data (RxD) and PD1 for transmit data (TxD).

BAUD RATE GENERATION

The actual baud rate generation circuit contains a programmable prescaler and divider which is clocked by the MCU E clock. A programmable baud rate register is used to provide the various divide ratios used in the baud rate generator prescaler and divider. This scheme of baud rate generation allows for selection of many different standard baud rates, all of which are controlled by the crystal oscillator.

DATA FORMAT

Receive data (RxD) in or transmit data (TxD) out is the serial data which is presented between the input pin (PD0) and the internal data bus, and between the internal data bus and the output pin (PD1). The data format requires:

1. An idle line which is in the high state (logic one) prior to transmission/reception of a message.
2. A start bit (logic zero) which is transmitted/received indicating the start of a message.
3. Data is transmitted and received least-significant bit first.
4. A stop bit (logic one in the tenth or eleventh bit position) indicates the byte is complete.
5. A break is defined as the transmission or reception of a logic zero for some multiple of the data format.

The data format word length may consist of either ten or eleven bits. Selection of the word length is controlled by a single bit in a control register within the SCI. If this control bit is clear, the data contains a start bit, eight data bits, and a stop bit. If this control bit is set, there is a start bit, nine data bits, and a stop bit.

TRANSMIT OPERATION

The SCI transmitter includes a parallel data register and a serial shift register. This is referred to as a double buffered system in that besides the character being shifted out serially, another character is already waiting to be loaded into the serial shift register. The output of the transmit serial shift-register is applied to the TxD output pin (PD1) as long as a transmit enable bit is set.

RECEIVE OPERATION

Receive data in (RxD) is serial data which is presented to the input pin (PD0). An advanced data recovery scheme is used to distinguish valid data from noise in the serial data stream. In this manner the data input can be selectively sampled to detect receive data and then verify that the data is valid. Data is received in a serial shift register and is transferred to a parallel register as a complete byte. This is referred to as a double buffered system in that besides the character already in the parallel register, another is being shifted in serially.

WAKE-UP FEATURE

The wake-up feature allows a receiver(s) to "sleep" until a specific action takes place. In a typical multiprocessor configuration, the software protocol will usually identify the addressee(s) at the beginning of a message. This wake-up feature allows uninterested MPUs to ignore incoming messages. The MC68HC11A4 SCI permits this wake-up feature by either of two methods: idle line wake-up or address mark wake-up.

In idle line wake-up, all receivers wake up whenever an idle line is detected, however, if a receiver does not recognize its address in the first frame of a message it may ignore the rest of the message by invoking the wake-up feature. In this wake-up method, transmitter software must provide for the required idle string between consecutive messages and prevent it from occurring within messages.

In the address mark wake-up, all serial frames consist of seven (or eight) information bits plus a most-significant bit (MSB) which is used to indicate an address frame if the MSB is a logic one. The first frame of each message is an address frame which wakes up all receivers in the system. All receivers evaluate this marked address frame to determine which receiver(s) the message is intended for. If a receiver determines that a message is not intended for it, it invokes the receiver wake-up function so that no additional program overhead is required for the rest of the message.

INTERRUPT FLAGS

The serial communications interface (SCI) generates a hardware interrupt (SCI interrupt) whenever any one of several flags is set and its corresponding interrupt enable bit is also set. These flags which are discussed below include:

1. Transmit Data register empty
2. Transmission complete
3. Idle line detected
4. Receive data register full or overrun error detected.

The transmit data register empty (TDRE) bit is set to indicate that the transmit parallel data register contents have been transferred to the transmit serial shift register. If the corresponding interrupt enable bit (transmit interrupt enable) is set then an SCI interrupt is generated.

The transmission complete (TC) bit is set when the transmitter no longer has any meaningful information to transmit; i.e., no data in the serial shifter, no queued preamble, and no queued break. If the transmitter is enabled when TC is set, the serial line will go idle (continuous mark).

The idle line detected (IDLE) bit is set whenever a receiver detects a receiver idle line. This could indicate the end of a message, the preamble of a new message, or resynchronization with the transmitter. If the corresponding interrupt enable bit (idle line interrupt enable) is set then an SCI interrupt is generated.

The receiver data register full (RDRF) bit is set whenever the receiver serial shift register contents are transferred to the serial communications data register. If the corresponding interrupt enable bit (receive interrupt enable) is set then an SCI interrupt is generated.

The overrun error bit is set to indicate that the next byte is ready for transfer from the receive shift register to the receive data register but that register is already full (RDRF bit set). Data transfer is then inhibited until the OR (overrun) bit is cleared. As with the RDRF bit, an SCI interrupt is generated if the corresponding interrupt enable bit is set.

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) allows several MC68HC11A4 MCUs, or MC68HC11A4 MCUs plus peripheral devices, to be interconnected within a single "black box", on the same printed circuit board. In a serial peripheral interface, the MC68HC11A4 provides such features as:

- Full Duplex, Two, Three, or Four Wire Synchronous Transfers
- Master or Slave Operation
- Interface With Low Cost "Dumb" Peripherals
- Interface With Intelligent Peripherals on Master/Slave Basis
- Four Programmable Master Bit Rates
- Programmable Clock Polarity and Phase
- End of Transmission Interrupt Flag
- Write Collision Error Detection
- Master-Master Mode Fault Error Detection

Four basic signal lines are associated with the SPI system. These include a master-out-slave-in (MOSI) line; a master-in-slave-out (MISO) line; a serial clock (SCK) line; and a slave select ($\overline{SS}$) line. Two master-slave system configurations are shown in Figure 5 and the basic signals (MOSI, MISO, SCK, and $\overline{SS}$) are described below.

MASTER OUT SLAVE IN (MOSI)

The MOSI pin is configured as a data output in a master (mode) device and as a data input in a slave (mode) device. In this manner data is transferred serially from a master to a slave on this line, most significant bit first, least significant last

MASTER IN SLAVE OUT (MISO)

The MISO pin is configured as an input in a master (mode) device and as an output in a slave (mode) device. In this manner data is transferred serially from a slave to a master on this line; most significant bit first, least significant last

SLAVE SELECT ($\overline{SS}$)

The slave select ($\overline{SS}$) is a fixed input which receives an active low signal that is generated by a master device to enable slave devices to accept data

SERIAL CLOCK (SCK)

The serial clock is used to synchronize the movement of data both in and out of the device through its MOSI or MISO pins. The master and slave devices can exchange a byte of information during a sequence of eight clock pulses. The SCK is generated by the controlling master device and becomes an input on all slave devices to synchronize slave data transfer

ANALOG-TO-DIGITAL (A/D) CONVERTER

The MC68HC11A4 contains an 8-channel, multiplexed input, successive approximation analog-to-digital converter with sample and hold. Two dedicated pins (V_{REFL}, V_{REFH}) are provided for the reference supply voltage input. These dedicated pins are used instead of the device power pins to increase accuracy of the A/D conversion.

The 8-bit A/D conversions of the MC68HC11A4 are accurate to within ± one LSB (± ½ LSB quantizing error and ± ½ LSB non-linearity error). Each conversion is accomplished in 50 MCU E clock cycles or less. An internal control bit allows selection of an internal conversion clock oscillator which allows the A/D to be used with very low MCU clock rates. A typical conversion cycle requires 25 to 50 microseconds to complete.

NOTE

In the 48-pin dual in-line package, four conversion channels are not implemented. These include channels four through seven

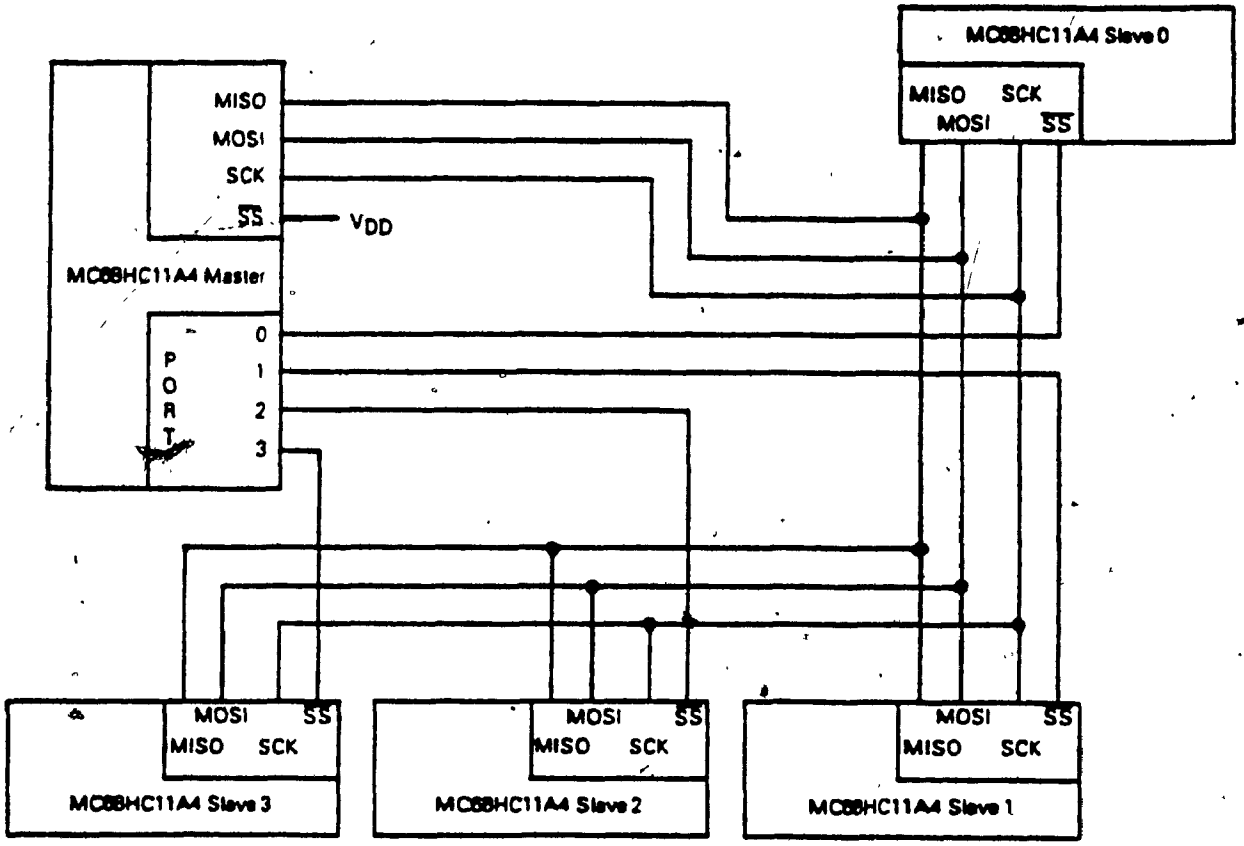
ADDRESSING MODES

Six addressing modes can be used to reference memory they include: immediate, direct, extended, indexed (with either of two 16-bit index registers and an 8-bit offset) inherent, and relative. Some instructions require an additional byte before the opcode to accommodate a multi-page opcode map; this byte is called a prebyte.

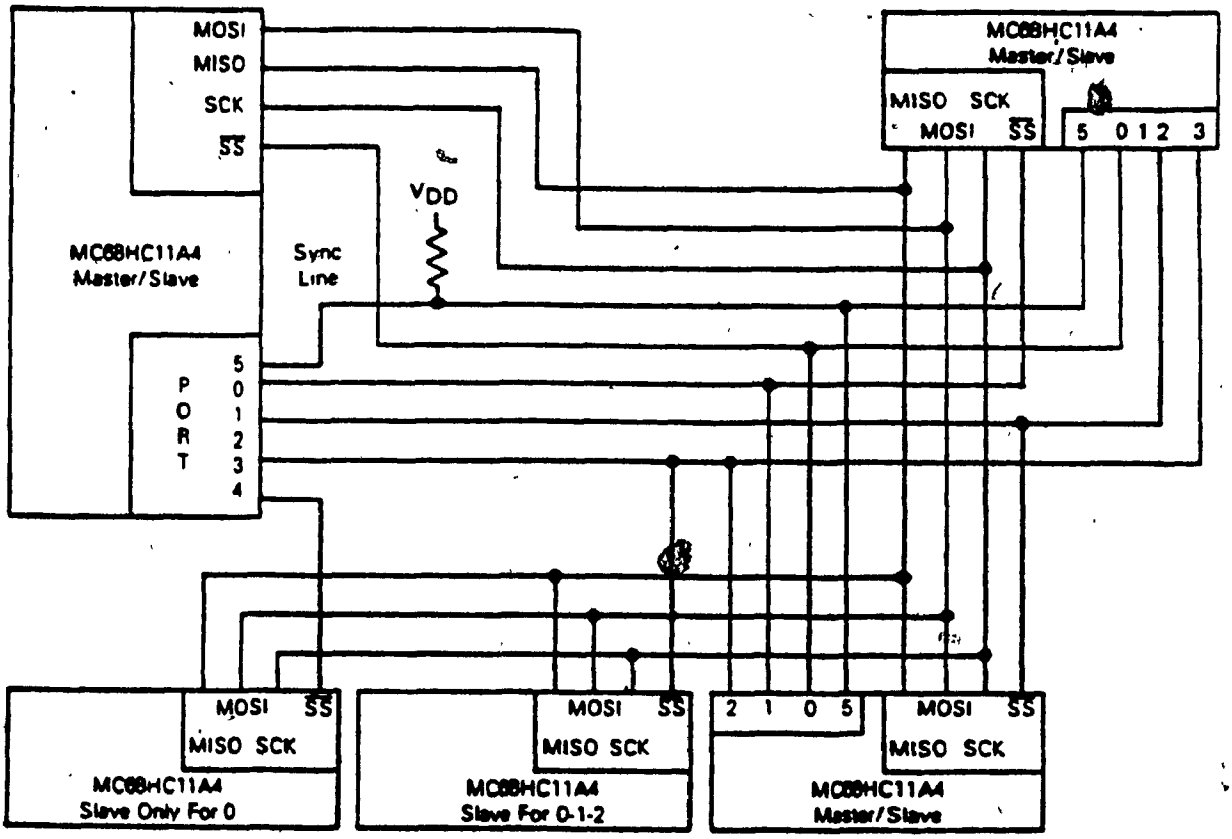
The following paragraphs provide a description of each addressing mode plus a discussion of the prebyte. In these descriptions the term effective address is used to indicate the address in memory from which the argument is fetched or stored, or from which execution is to proceed.

FIGURE 5 — MASTER-SLAVE SYSTEM CONFIGURATION

a. Single Master, Four Slaves



b. Three Master/Slave, Two Slaves



IMMEDIATE ADDRESSING

In the immediate addressing mode, the actual argument is contained in the byte(s) immediately following the instruction where the number of bytes matches the size of the register. These are two, three, or four (if prebyte is required) byte instructions

DIRECT ADDRESSING

In the direct addressing mode, the least significant byte of the operand address is contained in a single byte following the opcode and the most significant byte is assumed to be $00. Direct addressing allows the user to access addresses $0000 through $00FF using two byte instructions and execution time is reduced by eliminating the additional memory access. In most applications, this 256-byte area is reserved for frequently referenced data. These are usually two or three (if prebyte is required) byte instructions

EXTENDED ADDRESSING

In the extended addressing mode, the second and third bytes following the opcode contain the absolute address of the operand. These are three or four (if prebyte is required) byte instructions: one or two for the opcode and two for the effective address

INDEXED ADDRESSING

In the indexed addressing mode, one of the index registers (X or Y) is used in calculating the effective address. In this case the effective address is variable and depends on two factors: (1) the current contents of the index register (X or Y) being used, and (2) the 8-bit unsigned offset contained in the instruction. This addressing mode allows referencing any memory location in the 64K byte address space. These are usually two or three (if prebyte is required) byte instructions, the opcode plus the 8-bit offset

INHERENT ADDRESSING

In the inherent addressing mode, all of the information to execute the instruction is contained in the opcode. The operands (if any) are registers and no memory reference is required. These are usually one or two byte instructions.

RELATIVE ADDRESSING

The relative addressing mode is used for branch instructions. If the branch condition is true and contents of the 8-bit signed byte following the opcode (the offset) is added to the contents of the program counter to form the effective branch address; otherwise, control proceeds to the next instruction. These are usually two byte instructions.

PREBYTE

In order to expand the number of instructions used in the MC68HC11A4, a prebyte instruction has been added to certain instructions. The instructions affected are usually associated with index register Y. The opcode instructions which do not require a prebyte could be considred as page 1 of the overall opcode map. The remaining opcodes could be considered as pages 2, 3, and 4 of the opcode map and would require a prebyte, $18 for page 2, $1A for page 3, and $CD for page 4. Refer to **INSTRUCTION SUMMARY** for more detail.

INSTRUCTION SET

The central processing unit (CPU) in the MC68HC11A4 is basically a proper extension of the MC6801 CPU. In addition to its ability to execute all M6800 and M6801 instructions, the MC68HC11A4 CPU has a paged operation code (opcode) map with a total of 91 new opcodes. Major functional additions include a second 16-bit index register (Y register), two types of 16-by-16 divide instructions, a STOP instruction, and bit manipulation instructions.

Table 3 shows all MC68HC11A4 instructions in all possible addressing modes. For each instruction the operand construction is shown as well as the total number of machine code bytes and execution time in CPU E-clock cycles. Notes are provided at the end of Table 3 which explain the letters in the Operand and Execution Time columns of some instructions.

TABLE 3 – MC68HC11A4 INSTRUCTIONS, ADDRESSING MODES, AND EXECUTION TIMES

Source Form(s)	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Machine Code Bytes (Total)	Execution Time (Cycles)
ABA	INH	1B		1	2
ABX	INH	3A		1	3
ABY	INH	18 3A		2	4
ADCA (opr)	A IMM	89	ii	2	2
	A DIR	99	dd	2	3
	A EXT	B9	hh ll	3	4
	A IND, X	A9	ff	2	4
	A IND, Y	18 A9	ff	3	5
ADCB (opr)	B IMM	C9	ii	2	2
	B DIR	D9	dd	2	3
	B EXT	F9	hh ll	3	4
	B IND, X	E9	ff	2	4
	B IND, Y	18 E9	ff	3	5
ADDA (opr)	A IMM	8B	ii	2	2
	A DIR	9B	dd	2	3
	A EXT	BB	hh ll	3	4
	A IND, X	AB	ff	2	4
	A IND, Y	18 AB	ff	3	5
ADDB (opr)	B IMM	CB	ii	2	2
	B DIR	DB	dd	2	3
	B EXT	FB	hh ll	3	4
	B IND, X	EB	ff	2	4
	B IND, Y	18 EB	ff	3	5
ADDD (opr)	IMM	C3	jj kk	3	4
	DIR	D3	dd	2	5
	EXT	F3	hh ll	3	6
	IND, X	E3	ff	2	6
	IND, Y	18 E3	ff	3	7
ANDA (opr)	A IMM	84	ii	2	2
	A DIR	94	dd	2	3
	A EXT	B4	hh ll	3	4
	A IND, X	A4	ff	2	4
	A IND, Y	18 A4	ff	3	5
ANDB (opr)	B IMM	C4	ii	2	2
	B DIR	D4	dd	2	3
	B EXT	F4	hh ll	3	4
	B IND, X	E4	ff	2	4
	B IND, Y	18 E4	ff	3	5
ASL (opr)	EXT	78	hh ll	3	6
	IND, X	68	ff	2	6
	IND, Y	18 68	ff	3	7
ASLA	A INH	48		1	2
ASLB	B INH	58		1	2
ASLD	INH	05		1	3
ASR (opr)	EXT	77	hh ll	3	6
	IND, X	67	ff	2	6
	IND, Y	18 67	ff	3	7
ASRA	A INH	47		1	2
ASRB	B INH	57		1	2
BCC (rel)	REL	24	rr	2	3
BCLR (opr) (msk)	DIR	15	dd mm	3	6
	IND, X	1D	ff mm	3	7
	IND, Y	18 1D	ff mm	4	8
BCS (rel)	REL	25	rr	2	3
BEQ (rel)	REL	27	rr	2	3
BGE (rel)	REL	2C	rr	2	3
BGT (rel)	REL	2E	rr	2	3

TABLE 3 – MC68HC11A4 INSTRUCTIONS, ADDRESSING MODES, AND EXECUTION TIMES (CONTINUED)

Source Form(s)	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Machine Code Bytes (Total)	Execution Time (Cycles)
BHI (rel)	REL	22	rr	2	3
BHS (rel)	REL	24	rr	2	3
BITA (opr)	A IMM	85	ii	2	2
	A DIR	95	dd	2	3
	A EXT	B5	hh ll	3	4
	A IND, X	A5	ff	2	4
	A IND, Y	18 A5	ff	3	5
BITB (opr)	B IMM	C5	ii	2	2
	B DIR	D5	dd	2	3
	B EXT	F5	hh ll	3	4
	B IND, X	E5	ff	2	4
	B IND, Y	18 E5	ff	3	5
BLE (rel)	REL	2F	rr	2	3
BLO (rel)	REL	25	rr	2	3
BLS (rel)	REL	23	rr	2	3
BLT (rel)	REL	2D	rr	2	3
BMI (rel)	REL	2B	rr	2	3
BNE (rel)	REL	26	rr	2	3
BPL (rel)	REL	2A	rr	2	3
BRA (rel)	REL	20	rr	2	3
BRN (rel)	REL	21	rr	2	3
BRCLR (opr)	DIR	13	dd mm rr	4	6
(msk)	IND, X	1F	ff mm rr	4	7
(rel)	IND, Y	18 1F	ff mm rr	5	8
BRSET (opr)	DIR	12	dd mm rr	4	6
(msk)	IND, X	1E	ff mm rr	4	7
(rel)	IND, Y	18 1E	ff mm rr	5	8
BSET (opr) (msk)	DIR	14	dd mm	3	6
	IND, X	1C	ff mm	3	7
	IND, Y	18 1C	ff mm	4	8
BSR (rel)	REL	8D	rr	2	6
BVC (rel)	REL	28	rr	2	3
BVS (rel)	REL	29	rr	2	3
CBA	INH	11		1	2
CLC	INH	0C		1	2
CLI	INH	0E		1	2
CLR (opr)	EXT	7F	hh ll	3	6
	IND, X	6F	ff	2	6
	IND, Y	18 6F	ff	3	7
CLRA	A INH	4F		1	2
CLRB	B INH	5F		1	2
CLV	INH	0A		1	2
CMPA (opr)	A IMM	81	ii	2	2
	A DIR	91	dd	2	3
	A EXT	B1	hh ll	3	4
	A IND, X	A1	ff	2	4
	A IND, Y	18 A1	ff	3	5
CMPB (opr)	B IMM	C1	ii	2	2
	B DIR	D1	dd	2	3
	B EXT	F1	hh ll	3	4
	B IND, X	E1	ff	2	4
	B IND, Y	18 E1	ff	3	5

TABLE 3 – MC68HC11A4 INSTRUCTIONS, ADDRESSING MODES, AND EXECUTION TIMES (CONTINUED)

Source Form(s)	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Machine Code Bytes (Total)	Execution Time (Cycles)
COM (opr)	EXT	73	hh ll	3	6
	IND, X	63	ff	2	6
	IND, Y	18 63	ff	3	7
COMA	A INH	43		1	2
COMB	B INH	53		1	2
CPD (opr)	IMM	1A 83	jj kk	4	5
	DIR	1A 93	dd	3	6
	EXT	1A B3	hh ll	4	7
	IND, X	1A A3	ff	3	7
	IND, Y	CD A3	ff	3	7
CPX (opr)	IMM	8C	jj kk	3	4
	DIR	9C	dd	2	5
	EXT	BC	hh ll	3	6
	IND, X	AC	ff	2	6
	IND, Y	CD AC	ff	3	7
CPY (opr)	IMM	18 8C	jj kk	4	5
	DIR	18 9C	dd	3	6
	EXT	18 BC	hh ll	4	7
	IND, X	1A AC	ff	3	7
	IND, Y	18 AC	ff	3	7
DAA	INH	19		1	2
DEC (opr)	EXT	7A	hh ll	3	6
	IND, X	6A	ff	2	6
	IND, Y	18 6A	ff	3	7
DECA	A INH	4A		1	2
DECB	B INH	5A		1	2
DES	INH	34		1	3
DEX	INH	09		1	3
DEY	INH	18 09		2	4
EORA (opr)	A IMM	88	ii	2	2
	A DIR	98	dd	2	3
	A EXT	B8	hh ll	3	4
	A IND, X	A8	ff	2	4
	A IND, Y	18 A8	ff	3	5
EORB (opr)	B IMM	C8	ii	2	2
	B DIR	D8	dd	2	3
	B EXT	F8	hh ll	3	4
	B IND, X	E8	ff	2	4
	B IND, Y	18 E8	ff	3	5
FDIV	INH	03		1	41
IDIV	INH	02		1	41
INC (opr)	EXT	7C	hh ll	3	6
	IND, X	6C	ff	2	6
	IND, Y	18 6C	ff	3	7
INCA	A INH	4C		1	2
INCB	B INH	5C		1	2
INS	INH	31		1	3
INX	INH	08		1	3
INY	INH	18 08		2	4
JMP (opr)	EXT	7E	hh ll	3	3
	IND, X	6E	ff	2	3
	IND, Y	18 6E	ff	3	4
JSR (opr)	DIR	9D	dd	2	5
	EXT	BD	hh ll	3	6
	IND, X	AD	ff	2	6
	IND, Y	18 AD	ff	3	7

TABLE 3 — MC68HC11A4 INSTRUCTIONS, ADDRESSING MODES, AND EXECUTION TIMES (CONTINUED)

Source Form(s)	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Machine Code Bytes (Total)	Execution Time (Cycles)
LDAA (opr)	A IMM	86	ii	2	2
	A DIR	96	dd	2	3
	A EXT	B6	hh ll	3	4
	A IND, X	A6	ff	2	4
	A IND, Y	18 A6	ff	3	5
LDAB (opr)	B IMM	C6	ii	2	2
	B DIR	D6	dd	2	3
	B EXT	F6	hh ll	3	4
	B IND, X	E6	ff	2	4
	B IND, Y	18 E6	ff	3	5
LDD (opr)	IMM	CC	jj kk	3	3
	DIR	DC	dd	2	4
	EXT	FC	hh ll	3	5
	IND, X	EC	ff	2	5
	IND, Y	18 EC	ff	3	6
LDS (opr)	IMM	8E	jj kk	3	3
	DIR	9E	dd	2	4
	EXT	BE	hh ll	3	5
	IND, X	AE	ff	2	5
	IND, Y	18 AE	ff	3	6
LDX (opr)	IMM	CE	jj kk	3	3
	DIR	DE	dd	2	4
	EXT	FE	hh ll	3	5
	IND, X	EE	ff	2	5
	IND, Y	CD EE	ff	3	6
LDY (opr)	IMM	18 CE	jj kk	4	4
	DIR	18 DE	dd	3	5
	EXT	18 FE	hh ll	4	6
	IND, X	1A EE	ff	3	6
	IND, Y	18 EE	ff	3	6
LSL (opr)	EXT	78	hh ll	3	6
	IND, X	68	ff	2	6
	IND, Y	18 68	ff	3	7
LSLA	A INH	48		1	2
LSLB	B INH	58		1	2
LSLD	INH	05		1	3
LSR (opr)	EXT	74	hh ll	3	6
	IND, X	64	ff	2	6
	IND, Y	18 64	ff	3	7
LSRA	A INH	44		1	2
LSRB	B INH	54		1	2
LSRD	INH	04		1	3
MUL	INH	3D		1	10
NEG (opr)	EXT	70	hh ll	3	6
	IND, X	60	ff	2	6
	IND, Y	18 60	ff	3	7
NEGA	A INH	40		1	2
NEGB	B INH	50		1	2
NOP	INH	01		1	2
ORAA (opr)	A IMM	8A	ii	2	2
	A DIR	9A	dd	2	3
	A EXT	BA	hh ll	3	4
	A IND, X	AA	ff	2	4
	A IND, Y	18 AA	ff	3	5
ORAB (opr)	B IMM	CA	ii	2	2
	B DIR	DA	dd	2	3
	B EXT	FA	hh ll	3	4
	B IND, X	EA	ff	2	4
	B IND, Y	18 EA	ff	3	5

TABLE 3 — MC68HC11A4 INSTRUCTIONS, ADDRESSING MODES, AND EXECUTION TIMES (CONTINUED)

Source Form(s)	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Machine Code Bytes (Total)	Execution Time (Cycles)
PSHA	A INH	36		1	3
PSHB	B INH	37		1	3
PSHX	INH	3C		1	4
PSHY	INH	18 3C		2	5
PULA	A INH	32		1	4
PULB	B INH	33		1	4
PULX	INH	38		1	5
PULY	INH	18 38		2	6
ROL (opr)	EXT	78	hh ll	3	6
	IND, X	69	ff	2	6
	IND, Y	18 69	ff	3	7
ROLA	A INH	49		1	2
ROLB	B INH	59		1	2
ROR (opr)	EXT	76	hh ll	3	6
	IND, X	66	ff	2	6
	IND, Y	18 66	ff	3	7
RORA	A INH	46		1	2
RORB	B INH	56		1	2
RTI	INH	3B		1	12
RTS	INH	39		1	5
SBA	INH	10		1	2
SBCA (opr)	A IMM	82	ii	2	2
	A DIR	92	dd	2	3
	A EXT	B2	hh ll	3	4
	A IND, X	A2	ff	2	4
	A IND, Y	18 A2	ff	3	5
SBCB (opr)	B IMM	C2	ii	2	2
	B DIR	D2	dd	2	3
	B EXT	F2	hh ll	3	4
	B IND, X	E2	ff	2	4
	B IND, Y	18 E2	ff	3	5
SEC	INH	0D		1	2
SEI	INH	0F		1	2
SEV	INH	0B		1	2
STAA (opr)	A DIR	97	dd	2	3
	A EXT	B7	hh ll	3	4
	A IND, X	A7	ff	2	4
	A IND, Y	18 A7	ff	3	5
STAB (opr)	B DIR	D7	dd	2	3
	B EXT	F7	hh ll	3	4
	B IND, X	E7	ff	2	4
	B IND, Y	18 E7	ff	3	5
STD (opr)	DIR	DD	dd	2	4
	EXT	FD	hh ll	3	5
	IND, X	ED	ff	2	5
	IND, Y	18 ED	ff	3	6

TABLE 3 — MC68HC11A4 INSTRUCTIONS, ADDRESSING MODES, AND EXECUTION TIMES (CONTINUED)

Source Form(s)	Addressing Mode for Operand	Machine Coding (Hexadecimal) Opcode	Operand(s)	Machine Code Bytes (Total)	Execution Time (Cycles)
STOP	INH	CF		1	2
STS (opr)	DIR	9F	dd	2	4
	EXT	BF	hh ll	3	5
	IND, X	AF	ff	2	5
	IND, Y	18 AF	ff	3	6
STX (opr)	DIR	DF	dd	2	4
	EXT	FF	hh ll	3	5
	IND, X	EF	ff	2	5
	IND, Y	CD EF	ff	3	6
STY (opr)	DIR	18 DF	dd	3	5
	EXT	18 FF	hh ll	4	6
	IND, X	1A EF	ff	3	6
	IND, Y	18 EF	ff	3	6
SUBA (opr)	A IMM	80	ii	2	2
	A DIR	90	dd	2	3
	A EXT	B0	hh ll	3	4
	A IND, X	A0	ff	2	4
	A IND, Y	18 A0	ff	3	5
SUBB (opr)	B IMM	C0	ii	2	2
	B DIR	D0	dd	2	3
	B EXT	F0	hh ll	3	4
	B IND, X	E0	ff	2	4
	B IND, Y	18 E0	ff	3	5
SUBD (opr)	IMM	83	jj kk	3	4
	DIR	93	dd	2	5
	EXT	B3	hh ll	3	6
	IND, X	A3	ff	2	6
	IND, Y	18 A3	ff	3	7
SWI	INH	3F		1	14
TAB	INH	16		1	2
TAP	INH	06		1	2
TBA	INH	17		1	2
TEST	INH	00		1	*
TPA	INH	07		1	2
TST (opr)	EXT	7D	hh ll	3	6
	IND, X	6D	ff	2	6
	IND, Y	18 6D	ff	3	7
TSTA	A INH	4D		1	2
TSTB	B INH	5D		1	2
TSX	INH	30		1	3
TSY	INH	18 30		2	4
TXS	INH	35		1	3
TYS	INH	18 35		2	4
WAI	INH	3E		2	14 + n**
XGDX	INH	8F		1	3
XGDY	INH	18 8F		2	4

* - infinity or until reset occurs.

** - 12 cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MPU E-clock cycles (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector.

dd = 8-bit direct address ($0000-$00FF) (high byte assumed to be $00)

ff = 8-bit positive offset $00 (0) to $FF (255) is added to index)

hh = high order byte of 16-bit extended address

ii = one byte of immediate data

jj = high order byte of 16-bit immediate data

kk = low order byte of 16-bit immediate data

ll = low order byte of 16-bit extended address

mm = 1-byte bit mask (set bits to be affected)

rr = signed relative offset $80 (– 128) to $7F (+ 127) (offset relative to the address following the machine code offset byte)

APPENDIX 2

THE OPTICAL SMOKE DETECTOR DATA SHEETS

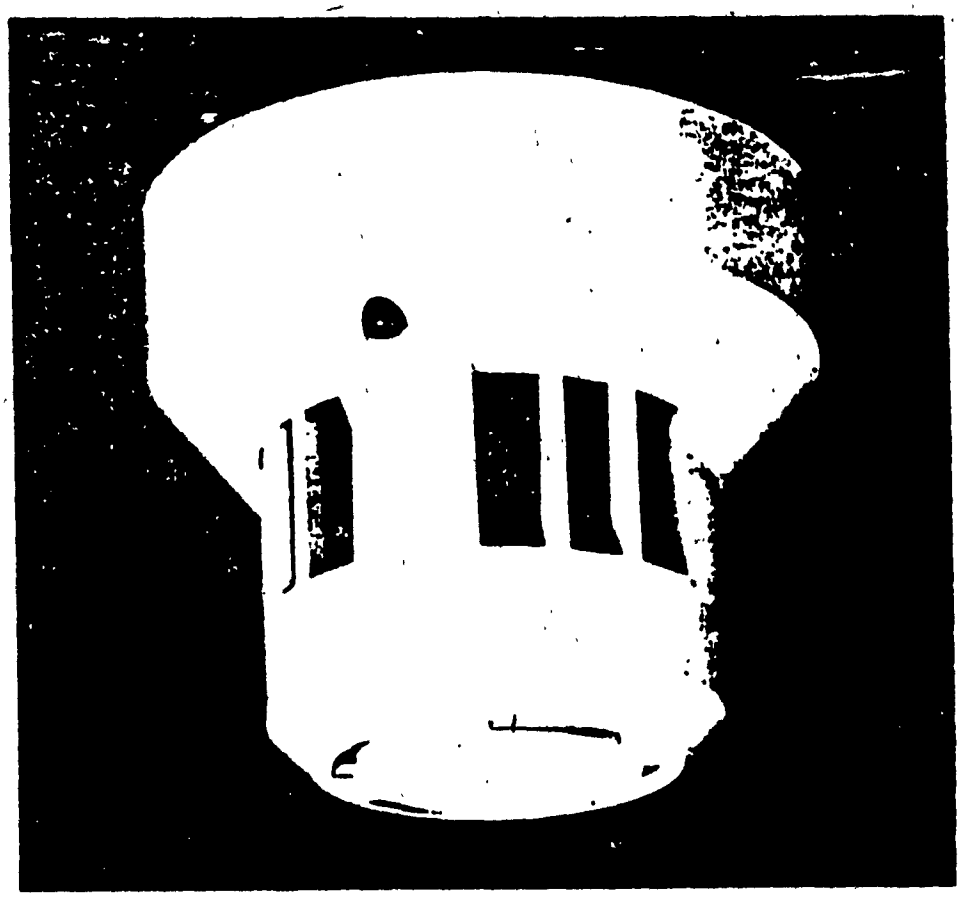


Figure 1. Apollo Optical Smoke Detector 53551-101

Introduction

The Apollo smoke detector Model 53551-101, figure 1, is sensitive to visible smoke particles produced at the early stages of a fire and is particularly useful in detecting smoke from slow burning or smouldering fires. The detector is suitable for use as an early warning fire detector in a wide range of industrial, commercial and residential environments. This guide describes the operating principle, construction specification and methods of installation and use of the detector.

Operating Principle

The detector contains an emitter, a solid state light emitting diode (LED) which, with its associated lens system, produces a hollow circular beam of light. A silicon photocell is positioned in the central dark area of the hollow beam so that in the absence of smoke no light is received, see figure 2. When smoke enters the chamber a combination of reflection and diffraction from smoke particles causes light from the beam to impinge on the photocell. Maximum reliability is obtained by driving the emitter LED to provide short, intense pulses of light and accepting data from the silicon photocell only during these pulses. When smoke is detected during one pulse, a further pulse is immediately produced, and only when smoke is also detected during the second pulse is an alarm initiated. The detector sensitivi is factory pre-set to meet internationc standards. The optical system is contained within a chamber which restricts the access of light from external sources and minimises internal reflections.

Electrical Description

The detector is designed to be connected to a central control unit providing a two wire monitored suppl of between 17 volts and 28 volts d.c. Terminals 1 and 6 are provided for the connection of the incoming positive and negative supplies respectively, see figure 3. Terminals 2 and 5 are connected to terminals 1 and 6 respectively by tracks on the detector printed circuit board. They provide supply outputs for the connection of additional detectors or an end of line monitoring device. This method of connection permits continuity monitoring of both positive and negative supplies through the detector including detector to mounting base supply connections.

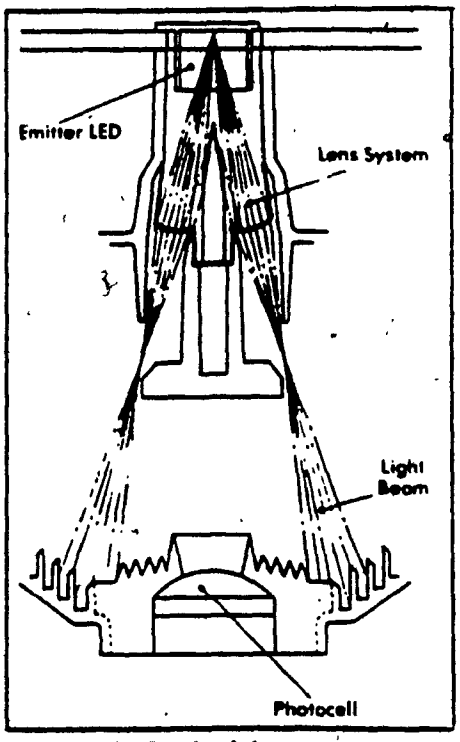


Figure 2. Optical Arrangement.

When power is supplied to the detector electrical interference is suppressed, see figure 3. A constant current is provided to a power supply circuit that after 30 seconds drives the detection electronics. A factory pre-set oscillator is used to control the frequency with which pulses are generated by the emitter drive circuit. The emitter drive output causes the emitter LED to flash at 8 second intervals. In the absence of smoke the photocell receives no light. When smoke enters the detector, light from the emitter LED is scattered on to the photocell. Only signals from the photocell that are received during a pulse of the emitter are recognised.

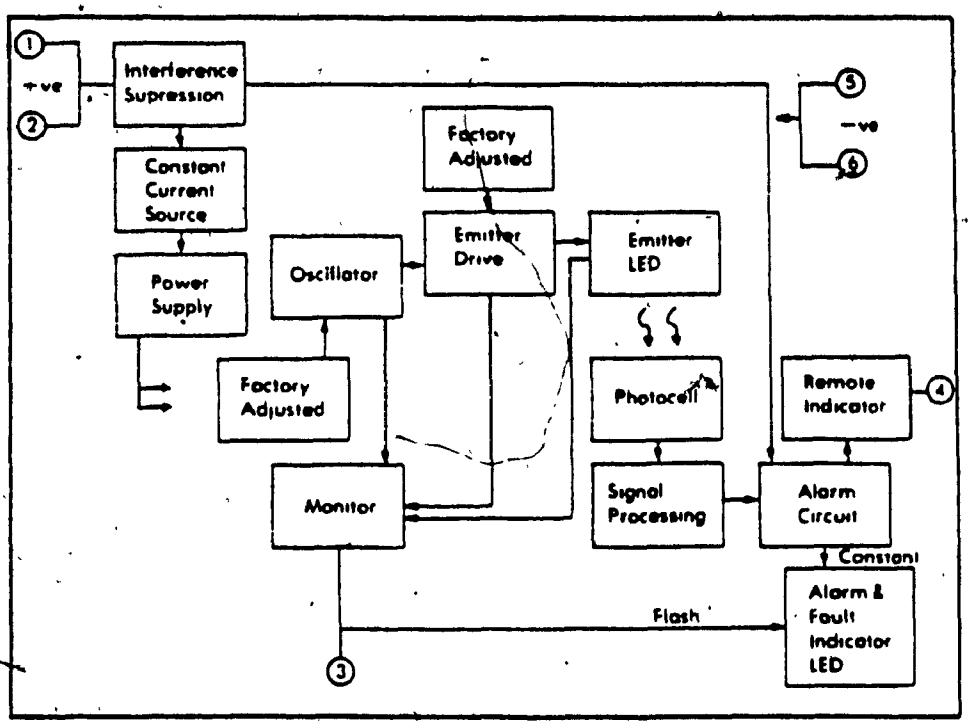


Figure 3. Optical Detector Schematic Circuit Diagram.

If smoke is detected during a pulse the oscillator is accelerated and the emitter LED flashes at one second intervals. It requires smoke to be detected during two consecutive pulses for the alarm circuit to be energised.

The alarm circuit is shown in figure 4. A positive going pulse turns on the silicon controlled rectifier (SCR). The red indicator LED is then turned on continuously and the detector changes state from its stand-by condition of 50 μA constant current to typically 60 mA, see table 1.

An external remote alarm indicator may be connected across terminals 2 and 4, terminal 4 being driven negative with respect to terminal 2 when the detector registers a smoke alarm. The output current terminal 4 should be externally limited to less than 80 mA either by the choice of remote indicator or by a series resistor in the case of an LED. Diode D3 permits the connection of more than one detector to a single remote indicator.

In the alarm state the control unit zone supply circuit voltage should not exceed 28 V and should have a minimum current capacity of 10 mA. The former level is set by power dissipation factors, and latter by the minimum holding current of the SCR. The supply to the detector in the alarm state should normally be held in excess of 12 volts (27 mA) to ensure effective illumination of the indicator LED.

To restore the detector to a stand-by condition it is necessary to expel the smoke and momentarily interrupt the supply to the detector. This resets the SCR and the detector electronics. The sensitivity of the detector is factory pre-set. The emitter LED, see figure 3, is continuously monitored for open and short circuits. Similarly failure of the emitter LED drive circuit, the internal oscillator and the presence of power is monitored. Successful monitoring results in a short pulse at nominally 32-second intervals being generated to flash the indicator LED, and provide a signal used for test purposes at pin 3.

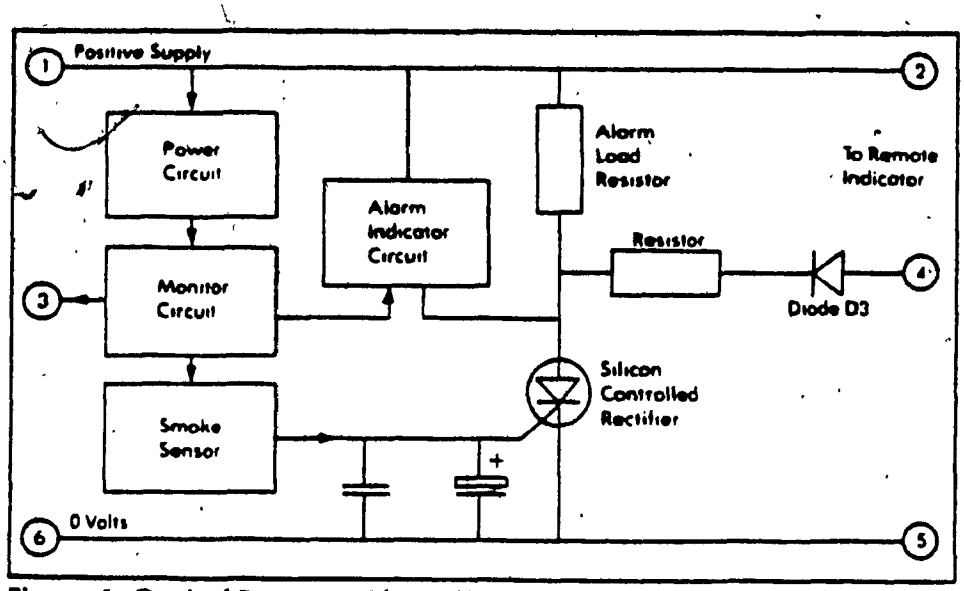


Figure 4. Optical Detector Alarm Circuit Schematic.

A press to test plunger is fitted which, when depressed using the longer probe of calibration test tool Part No. 38531-743 should result in an alarm, and when the shorter probe is inserted should not produce an alarm, see figure 6.

Control Unit Interface

Before a fire alarm system is engineered it is essential that compatibility between detector and control unit be fully investigated and proven under both normal and abnormal operating conditions. System design parameters embodying safety factors should be established

In establishing compatibility, full consideration should be given to supply and battery voltage variations, control unit impedance, line resistance and disconnection of end of line devices. It is recommended that the detector be considered to be a 40 to 60 μA constant current drain in standby conditions and in alarm be considered as 510 ohms in series with a 1.5 volt drop due to the SCR. This condition assumes that the detector's indicator LED is open circuit and represents a realistic minimum detector alarm load. Maximum alarm load conditions should assume that the detector is in full working order and connected to a remote indicating device. Typical current against voltage characteristics for stand-by and alarm states are shown in figure 5 and table 1.

with industry standards, of six per cent grey smoke obscuration per metre.

Independent test results to CEA standards and BS5446: Part 1 will be available in due course.

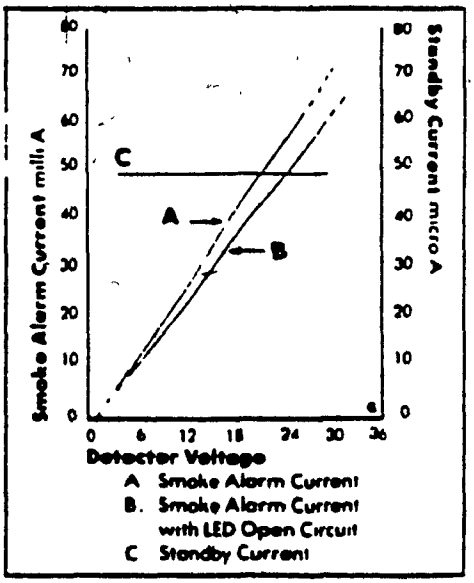


Figure 5. Typical Standby and Alarm Currents.

Detector Status			
Supply Voltage Volts	Standby Current μA	Smoke Alarm Current mA	Smoke Alarm Current (Indicator LED Fault) mA
28	50	68	57
24	50	58	49
18	50	43	36
12	Not Applicable	27	24
6	Not Applicable	12	11

Table 1.

Specification

Operating principle:
Photoelectric detection of light scattered in a forward direction by smoke particles.

Emitter:
Ga/As Infra Red LED.

Sensor:
Silicon photovoltaic cell.

Sampling frequency:
Once every 8 seconds — nominal.

Confirmation frequency:
Once per second — nominal.

Number of confirmations:
1.

Configuration:
Axially disposed light source lens system and light sensor.

Supply voltage:
17 — 28 volts d.c.

Ripple voltage:
2 volt peak to peak maximum.

Supply current:
50 micro amps nominal constant over full voltage range.

Switch-on surge:
Zero.

Alarm current:
68 mA at 28 volts d.c.
27 mA at 12 volts d.c.

Remote alarm output:
Rated 80 mA maximum, diode gated with 47 ohms series resistor.

Alarm voltage required:
10 - 28 volts d.c.

Design alarm load:
510 ohms in series with 1.5 volt drop across SCR (indicator LED open circuit).

SCR Holding voltage:
5 volts.

SCR Holding current:
10 mA.

Alarm Indicator:
Light emitting diode (red LED).

Indication:

a) Normal operation
Red LED flashes once every 30 seconds typical.

b) Fault
The absence of a flash at 30 second typical intervals indicates either:
i) Supply disconnected.
ii) Internal oscillator failure.
iii) Open circuit of infra red emitter LED.
iv) Short circuit of infra red emitter LED.
v) Failure of infra red emitter LED drive circuit.

c) Smoke alarm
LED on continuously.

Sensitivity:
6% grey smoke obscuration per metre.

Temperature range:
Maximum continuous operating 50°C.
Minimum continuous operating 0°C.
Short term minimum (24 hours) -20°C.
Storage -30°C to +70°C

Humidity:
0 — 95% RH.

Wind:
Insensitive to wind interference.

Vibration:
To BS5446 : Part 1. 1977 and EN54 : Part 5 : 1977.

Impact:
To BS5446 : Part 1 : 1977 and EN54 : Part 5 : 1977.

Shock:
To EN54 : Part 5 : 1977.

Electrical Transients:
To UL268.

Atmospheric Pressure:
Insensitive to variations in atmospheric pressure.

Supply Wiring:
Two wire monitored supply.

Terminal size:
2 cores, maximum 1.5 mm^2 per terminal.

Weight:
Detector — 135 grams.
Base — 65 grams.

Dimensions:
Detector —
Height — 72 mm
Diameter — 75 mm
Base —
Height — 23 mm
Diameter — 86 mm
Detector in Base assembly —
Height — 81 mm
Diameter — 86 mm

Materials:
Case and light trap — self extinguishing ABS to UL94 V-0 standard.
Lens — acrylic.
Printed circuit board — 1 ounce copper on glass fibre board with epoxy solder resist on non soldered areas.

Types of Smoke

The Apollo optical detector is suitable for detecting a large variety of fires. It is particularly useful in detecting smoke from slow burning or smouldering fires and is sensitive to the large particles of smoke produced at less than 250°C by some overheating plastics such as PVC. The detector may be slow to respond to free burning fires producing little or no smoke. This is not usually a serious problem because such fires normally involve other materials at an early stage. However, if this is unlikely, the detector should be supplemented by an ionisation smoke, a heat or flame detector.

Application

The application of the Apollo optical smoke detector must only be undertaken by engineers experienced in this field of fire detection.

Design Guides

Detectors should be sited, spaced and zoned in accordance with the recommendations of a generally recognized local standard or code of practice, such as BS 5839: Part 1; the Fire Offices' Committee Rules, the Comite Europeen Des Assurances Guidelines for Automatic Alarm Installations, or the National Fire Protection Association Standard (NFPA) 72E, standard for Automatic Fire Detectors.

Spacing

Unless the following circumstances are specifically covered by the above design guides, spacings substantially less than the maximum permissible recommended should be used where detectors protect main escape routes; where the escape of occupants may be delayed through illness, age, handicap or unfamiliarity with the building; in dormitories and computer suites where the fastest possible detection of smouldering fires is required; and in rooms where air changes exceed four per hour. Apollo Manufacturing Ltd. recommend that the area covered by a single smoke detector should not normally exceed 100 m^2, even if a greater area coverage is permitted by local regulation.

Siting

The detector's mounting base should normally be mounted directly onto the surface of the room, ceiling or roof. This places the sensing element of the detector approximately 50 mm below the surface. This distance may be increased by the presence of a wiring box. However, the distance between the smoke sensing chamber and the roof or ceiling should not normally exceed 150 mm in rooms up to 6 metres high, 300 mm in rooms up to 12 metres high, and 600 mm on steeply pitched roofs, except as may be indicated by fire tests.

The recessing of the detector, or its base, into a ceiling, or the mounting of the detector on a wall or vertical surface is not recommended. Detectors should never be mounted in an inverted position.

Detectors should not be mounted less than 500 mm away from any wall or partition, or in any position where there is an obstruction to the flow of smoke towards the detector within a distance of 600 mm.

Height

A height of 12 metres should not be exceeded except as may be indicated

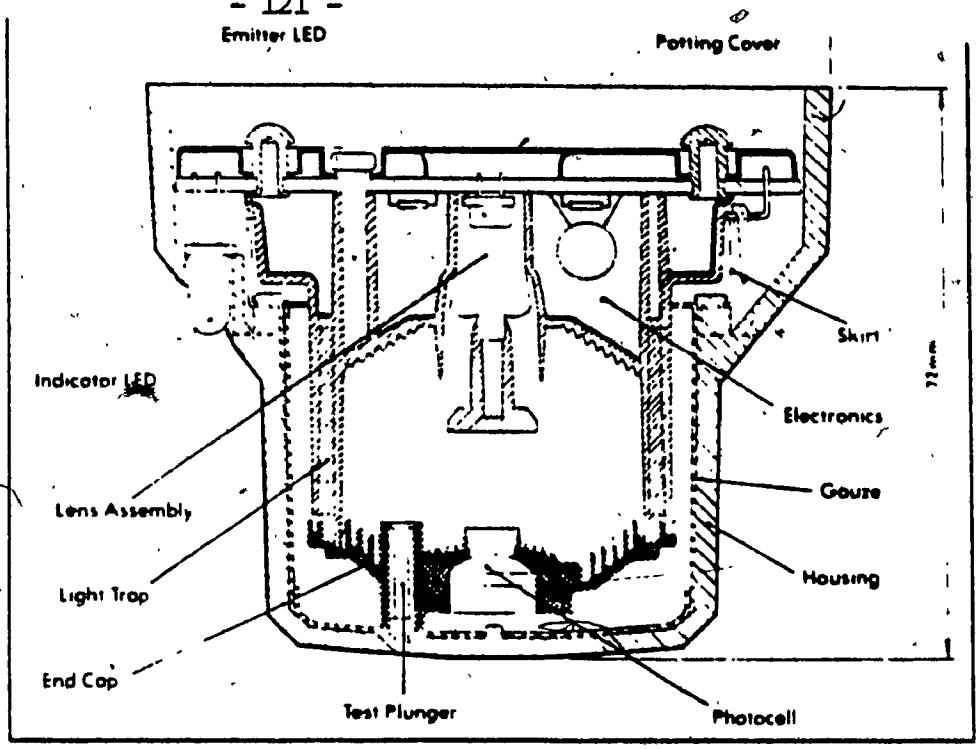


Figure 6. Simplified Construction Schematic.

Mechanical Construction

A sectional drawing of the detector is shown in figure 6. The white plastic housing of the detector is moulded in UL-94 V-0 grade of self extinguishing ABS and plugs into the Apollo Mounting Base Model 45681-007. Correct alignment of the leaf spring electrical contacts in the base with the six domed terminal pins in the detector is ensured by the detector's three volt free polarising bayonet studs. These studs key with three slots in the base through a 20 degree clockwise twist action. The wiping action between the nickel plated beryllium copper springs and the nickel plated brass pins ensures good electrical contact, see figure 7.

Apertures in the detector's housing allow smoke to ingress freely through the stainless steel gauze and into the smoke sensing chamber via the black ABS light trap. The emitter LED with its lens assembly are mounted directly on to the printed circuit board within the smoke sensing chamber.

The photocell is potted into the end cap of the light trap in alignment with the emitter LED, lens and light trap. The leads from this cell are taken via an integral clip on the light trap to the printed circuit board. The light trap and the printed circuit board form an enclosure around the principal electronic components. The track side of the printed circuit board is enclosed by the potting cover. These enclosures are filled with a resilient potting medium, and a label is fitted which covers the potting access holes. The stainless steel gauzes and the stainless steel skirt, which are connected to zero volts through a spring on the printed circuit board, screen the detector from

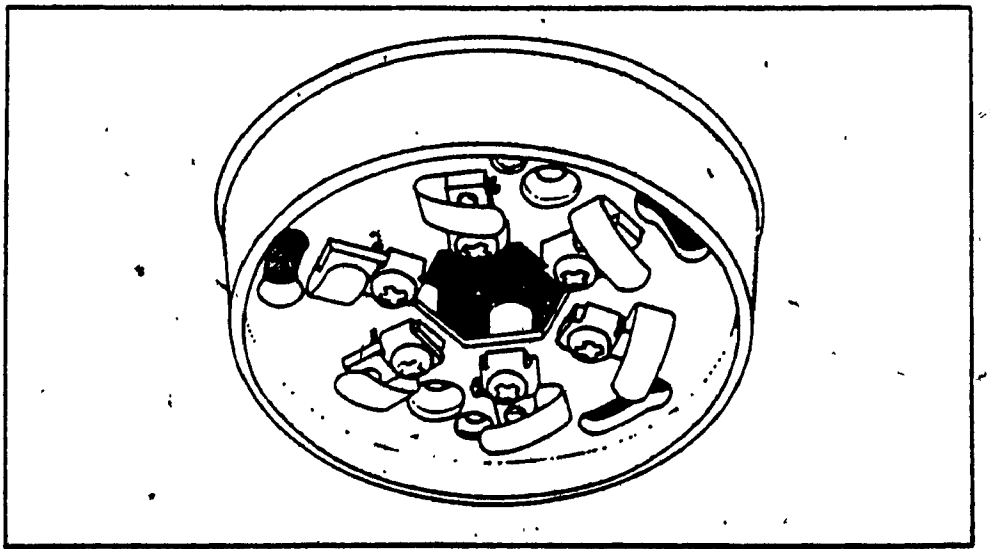


Figure 7. Apollo Mounting Base 45681-007.

electrostatic interference. The gauze also acts as a barrier to insects. The indicator LED is mounted directly on t the printed circuit board and protrud through the detector housing.

Mounting Base

The interface between the smo detector and the fire alarm system wiring is made with an Apollo Mounting Base Model 45681-007, see figure 7. The detector plugs into the base with a 'twist lock' action that causes the detector's terminal spring to engage with the spring contacts in the base with a wiping action. The springs are connected to terminals fitted with a non-rotating clamp for positively securing one or two cable conductors with cross-sectional area up to a maximum of 1.5 mm². Each terminal is identified by a raised number in the plastic moulding. Acce to the terminals is available from the front of the base upon removal of the detector, cables from the terminals being routed to the rear of the base through a central hole. To facilitate th entry of the surface wired cables one more of three thin plastic sections ca be cut away from the base skirt.

Two countersunk 5.0 mm diameter holes on 50.8 mm fixing centres are provided for directly attaching the mounting base to a wiring box to BS4568: Part 2:1970. Two M4 X 25 mm countersunk cadmiu plated steel screws are suitable for th purpose. Additionally, two countersu 3.2 mm diameter holes on 60 mm fixir centres are provided for attaching the base to certain European wiring boxe Either pair of fixing holes may be used to secure the base directly to a structural member of a building.

Every mounting base is supplied with a plastic cover which should be clipped on the back of the base before securing it to a wiring box or structure member. The use of this cover improves the dust, water and insect resistance of the detector.

When it is necessary to orientat a detector so that the indicator LED is visible from a particular viewpoint the mounting base should be installed with terminal number 5 closest to that viewpoint. If a detector is to be installed in a confined space, such as a ventilation duct, a minimum clearance of 100 mm is required beneath the bas fixing surface to enable the detector to be easily inserted and removed.

Smoke Performance

The response time of detectors is dependent on many factors including the type of fuel, the rate of burning, the size and shape of room, ventilatio rates, and the distance of the detecto from the fire. Unless these and other factors are carefully controlled reproducible results cannot be expected. Controlled tests have been conducted in recirculating smoke tunnels to demonstrate that the detector has a sensitivity, consistent by satisfactory fire tests on site. Where ceiling heights in excess of 15 metres are encountered consideration should be given to the use of supplementary ultra-violet or infra-red flame detectors, or to the suspending of smoke detectors from the roof or ceiling to a level below 12 metres, in addition to mounting detectors on or close to the ceiling.

In rooms with ceilings less than 3 metres high, careful siting of detectors is necessary to avoid nuisance operations by tobacco smoke.

Air Flow

The detector is not sensitive to air flow and thus may be used in ducts provided that satisfactory tests have shown that the smoke in the duct is evenly distributed throughout the air flow.

If the detector is installed within a ventilation duct it should be sited in the centre of a straight section of duction having a length of at least six times its width. All cable outlets and air paths between the base of the detector and the outside of the duct should be sealed. As the effectiveness of extract duct mounted detectors may be reduced by the extraction of clean air together with smoke, it may be necessary to install a detector near each extract point.

Humidity

The detector may be operated at humidity levels up to 95% RH. Prolonged operation at humidity levels in excess of 95% or in circumstances where condensation can occur may result in unwanted fire alarms. The detector should not be subject to rain, fog, steam or water spray.

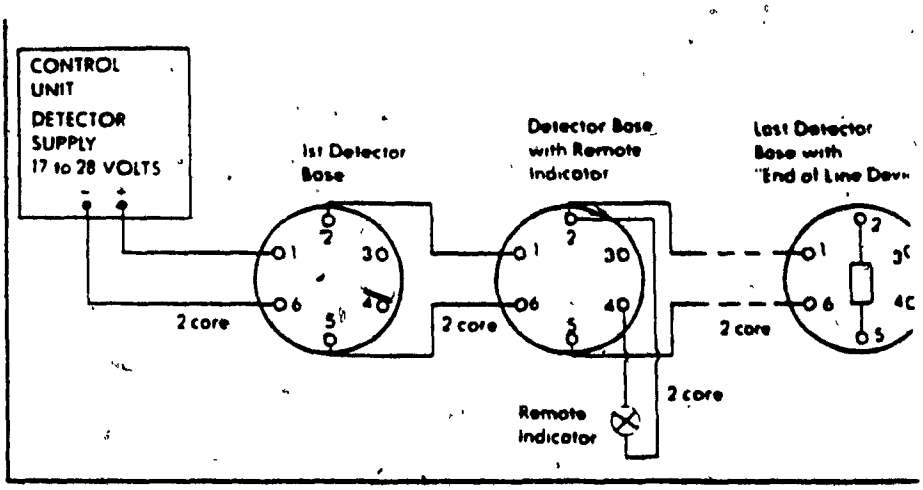


Figure 8. Schematic Wiring Diagram of Monitored 2 wire Zone Circuit.

Vibration

The performance of the detector is unaffected by exposure to levels of vibration and shock normally encountered on structural parts of buildings, but care should be taken not to mount the detector where it would be subject to continuous or frequent perceptible shocks or vibration.

Temperature

The detector may be used at normal ambient temperatures in the range 0°C to 50°C. It may also be used between 0°C and −20°C in circumstances where there is no possibility of detectors freezing up. Continuous operation in refrigerated rooms at less than 0°C is not permissible.

Zone Circuit

Figure 8 is a typical schematic wiring diagram showing the preferred method of connecting Apollo detectors to a control unit featuring a monitored two wire detector circuit. The end of line device is usually a diode or resistor of a type and value to suit the control unit.

If the control unit monitors only for open circuit faults in wiring between it and the end of line device, a short circuit or an open circuit in the unmonitored wiring to a remote indicator will not prevent a detector signalling a fire alarm, although the detector's LED may not illuminate in the event of a short circuit.

If the control unit also monitors for short-circuits it may be necessary to connect a current limiting device directly to terminal 4, in series with remote indicator, in order to prevent an alarm from a detector with a short circuit remote indicator being mistaken for a short circuit in the wiring to the end of line device. The detector's internal remote indicator circuit does include a 47 ohm resistor in series with the remote output. This may be sufficient to provide the required impedance to the control unit, depending on the circuit design of the control unit.

Where detectors are installed in a normally locked room it may be necessary to link all the detectors to a common remote indicator lamp sited outside the room. In such circumstances the method of wiring shown in figure 9 is recommended. If it is more practical to route cables from each detector directly to the remote indicator, all wires from terminals marked 4 should be connected to the return side of the indicator. If all wires originating from terminals marked 2 were connected together at the remote indicator, the wiring between detectors would be bypassed and consequently not fault monitored.

Figure 10 is a typical schematic wiring diagram showing a method of connecting detectors to a control unit which does not monitor the wiring for faults, and where local regulations require that the removal of a detector shall not result in the disconnection of other detectors. When this circuit arrangement is used it is essential to terminate the wiring with a manual callpoint or similar device so that the circuit can be regularly and frequently tested.

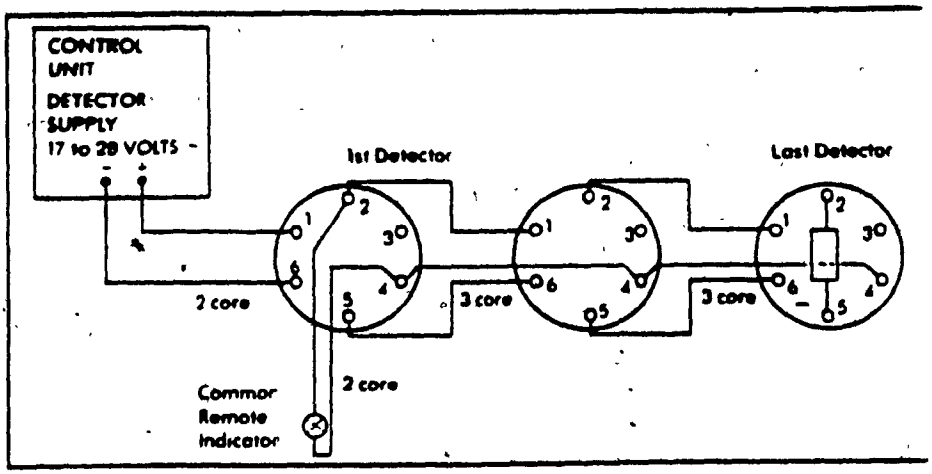


Figure 9. Schematic Wiring Diagram of Monitored Detector Circuit with a Common Remote Indicator.

Installation Wiring

In the United Kingdom the cables and wiring used to interconnect detectors and other components of a fire alarm system should normally be in accordance with the code of practice set out in BS5839: Part 1: 1980. Apollo recommend the use of either mineral insulated copper sheathed cable complying with BS6207: Part 1, or PVC insulated and sheathed cable complying with BS6004. The latter cable should be protected by conduit or trunking except in the special circumstances specified in BS5839.

Although the Apollo smoke detector is fitted with transient protection devices, electrical interference from adjacent cables and conductors supplying other services should be minimised by physical separation of the cables.

Typical methods of installing the detector are shown in figures 11, 12, and 13.

In other countries detectors should be installed and wired in accordance with appropriate national regulations and codes of practice, except where these conflict in principle with recommendations made in this document. Apollo Manufacturing Ltd. should be consulted if such a conflict arises.

When a zone of mounting bases has been installed the wiring should be tested for continuity and insulation resistance before installing the detectors. The time taken to accomplish this task can be minimised by using an Apollo Tristate Polarity Test Head part number 53541-003 and the necessary number of Apollo Link Heads part number 53541-001. The following testing sequence is recommended.

1) Connect the zone wiring to a current limited supply of between 15 and 30 volts or to a detector input of the control unit as appropriate.
2) Plug a polarity test head into the first detector base and note the colour of the LED: green indicates continuity and correct polarity; red indicates continuity and reversed polarity; and no illumination indicates an absence of continuity. When the correct polarity is indicated replace the polarity tester with a link head.
3) Repeat the sequence in 2) above at each successive mounting base until a link head is installed in every base.
4) Disconnect the wiring from the supply and use a high voltage insulation meter (250 volts to 1,000 volts) to measure the insulation resistance between each conductor and earth. The value should not normally be less than 1 Megohm.
5) Separately check the insulation resistance of any wiring to remote indicators.
6) Remove the link head from the last base in the zone, install any necessary end of line monitoring device and replace the link head. Use an appropriate instrument at the control unit end of the wiring to check that the device is correctly installed.
7) Connect the zone circuit to the control unit.
8) Replace every link head with a smoke detector which has been checked to be within calibration using test tool part number 38531-743. Provide the detector with a satisfactory power supply. Allow 60 seconds before testing. Insertion of the shorter probe on the calibration test tool should not result in an alarm. Upon insertion of the longer probe on the calibration test tool an alarm state should be generated within 20 seconds.

devices and any communication link to the fire brigade.

Where detectors are installed in a clean non-corrosive environment an annual service of the detectors in accordance with the schedule set out below is recommended. Detectors installed in less favourable conditions should be checked more frequently. The annual service should be in addition to the more frequently required routine visual inspection and selective smoke testing of detectors necessary to prove the continuing state of readiness of the fire protection system.

Service Schedule

1) Check that the detector is still the most suitable type for the area protected.
2) Check that the ingress of smoke into the detector has not been obstructed by surrounding objects.
3) Check that cables to and from the detector are undamaged and secure.
4) Remove the detector from its mounting base using Apollo extract tool, part number 41186-061, and extension pole, part number 41181-154, and immediately replace with a fully serviceable detector.
5) Check the age of the detector by reference to its serial number. Automatic replacement of detectors more than 10 years old with a new detector is recommended.
6) Clean detector in accordance with the instructions set out in the following section.
7) Test detector as described in Installation Wiring 8) above.
8) After satisfactory cleaning and testing either return detector to its original site in the system or use it as a serviceable replacement for the next detector in the system to be serviced.
9) Test the detector in situ by using either a hot wire/oil smoke generator or other smoke source. Corrosive chemical smoke should not be used. In some circumstances, and where appropriate safety precautions can be taken, test fires may be used. Under no circumstances should any attempt be made to operate the detector using a naked flame from a match or lighter. Check that appropriate alarm signals are produced and that the detector's indicator LED illuminates.
10) Clear smoke and reset detector and control and indicating equipment.
11) Note the results in log book.
12) Ensure that the fire protection system is returned to a fully operational status after servicing.

Storage

Detectors should be stored in a clean, dry environment and used in manufacturing date order.

Although the Apollo Ionisation Smoke Detector Portable Test Set Model 53832-013 does not test the Optical Smoke Detector it is a convenient portable power supply that can be used to facilitate this test. Conduct an in situ smoke test on every detector and check that the detector, the control unit, and any remote indicators respond correctly.

Maintenance

Apollo Manufacturing Ltd., recommend that users of Apollo smoke detectors enter into an agreement with the original supplier of the detectors for regular servicing. Ideally the control and indicating equipment should be serviced at the same time as the detectors as it may be necessary to temporarily inhibit one or more alarm

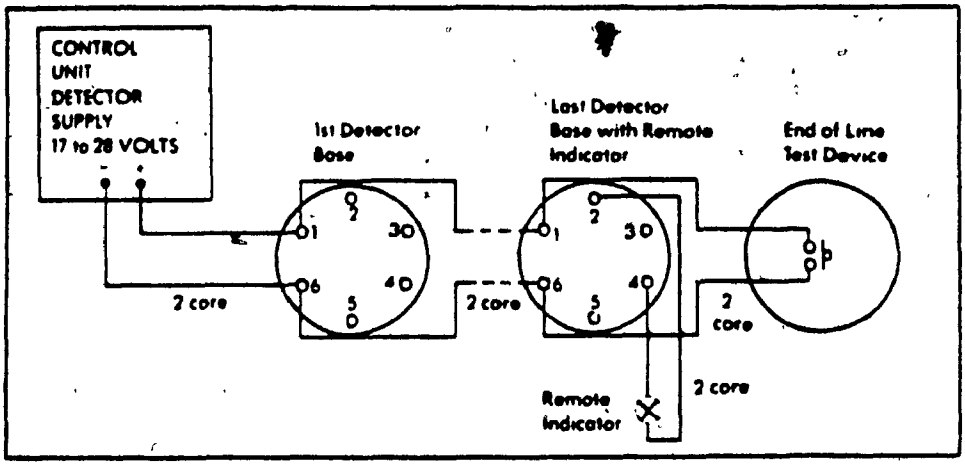


Figure 10. Schematic Wiring Diagram of Unmonitored 2 wire Zone Circuit.

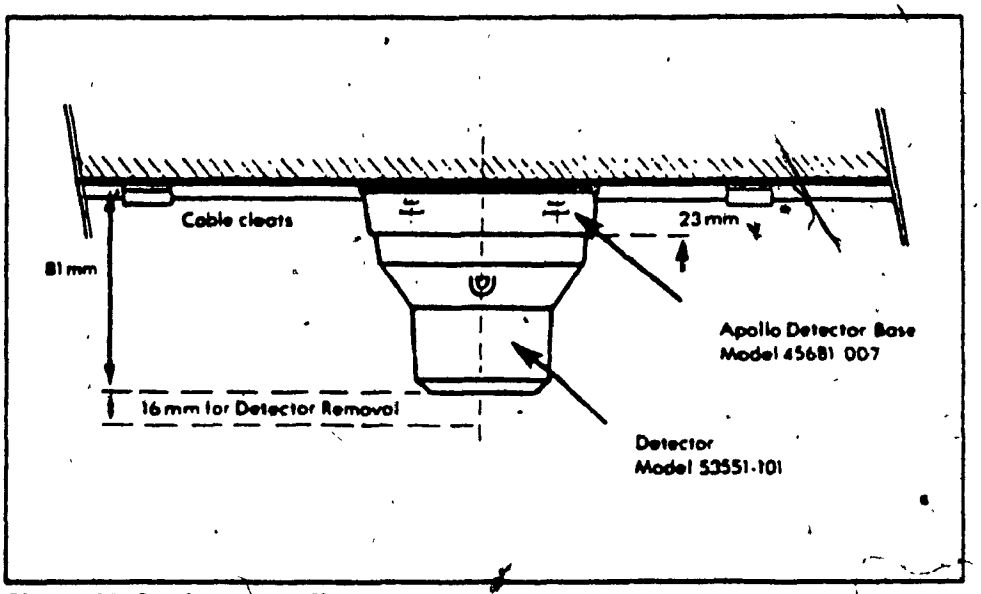


Figure 11. Surface Installation (PVC).

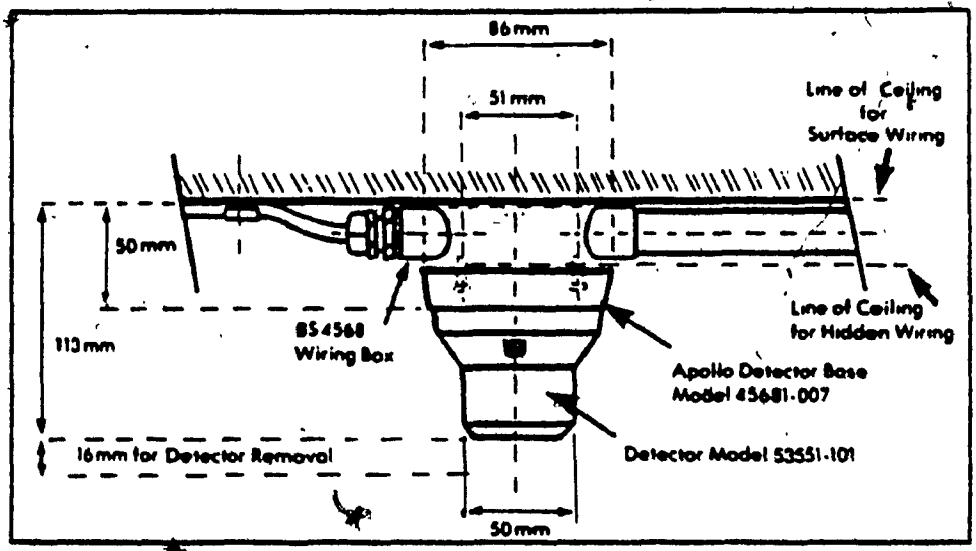


Figure 12. Surface or Finish Installation (M.I.C.C. or Conduit).

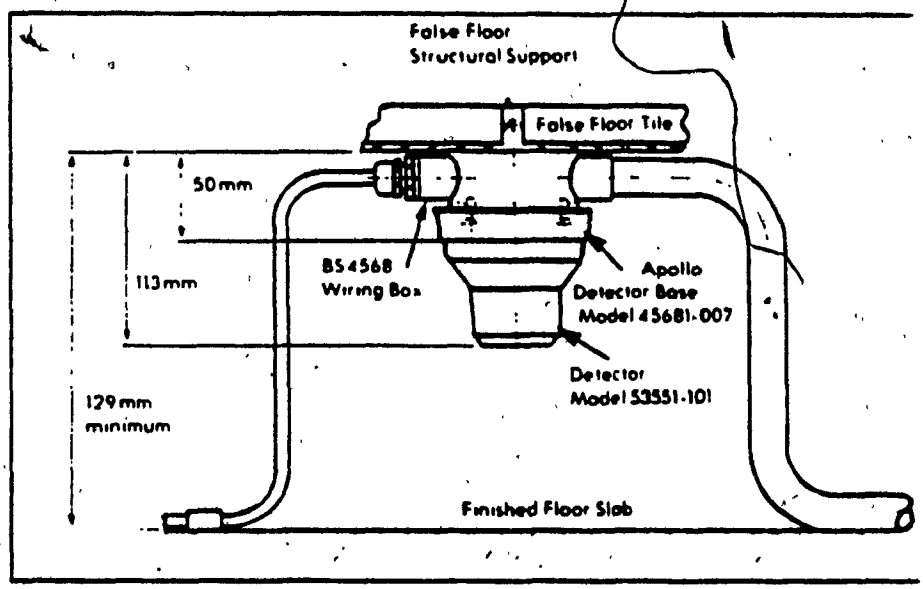


Figure 13. False Floor Installation (M.I.C.C. or Conduit).

Transport

Detectors are packed individually in cardboard cartons and then into a sleeve containing 10 units. The packaging is suitable for most inland transport and handling conditions. Packaging for offshore and export shipments should reflect the appropriate handling and storage conditions.

Cleaning Procedure

A detector which has been installed for a year in a reasonably clean and non-corrosive atmosphere can normally be cleaned without dismantling it. Use a vacuum cleaner with a brush attachment to remove any dust that has accumulated on exposed areas of gauze. A significant deposit in this area will indicate that dust needs to be removed from the internal structure of the detector, in which case remove the two screws visible on the circumference of the potting cover, see figure 6. Remove the detector assembly from the case. Carefully lift off the end cover from the light trap and brush out the light trap, end cover and lens assembly areas using a soft brush.

Reassemble the end cover on to the light trap. The assembly is polarised and will fit in only one position. Refit the assembly into the case so that the calibration plunger is located opposite its access point in the case. Attach the assembly to the case re-using the two screws earlier removed. Do not use excessive force to tighten these self-tapping screws. The white plastic case of the detector may be cleaned with a cloth made damp with diluted washing up liquid. If the case is severely stained a cloth made damp with industrial methylate spirit (ethyl alcohol) may prove more efficient. Do not use any other cleaning fluid or solvent.

Check that the terminal pins on the printed circuit board are clean. Tarnished pins may be cleaned with a quality metal polish. If the pins are badly tarnished or corroded the spring contacts and cable connections in the mounting base should be closely inspected. These should be cleaned or the base replaced as necessary.

Test that the detector is working and within calibration as described in Installation Wiring Section 8) above, prior to its being returned to use.

Detectors which cannot be adequately cleaned by the above procedure and detectors which do not perform satisfactorily when checked as described, should be factory cleaned and recalibrated either by Apollo or an Apollo approved company.

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