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A HIGHLY EFFICIENT LOW OUTPUT VOLTAGE DC TO DC CONVERTER

Edoardo O. L. Gotti

A Thesis

in

The Department

of

Electrical And Computer Engineering

Presented in Partial Fulfillment of the Requirements
for the degree of Master of Applied Science at
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ABSTRACT

A Highly Efficient Low Output Voltage DC to DC Converter

Edoardo O. L. Gotti

The purpose of this work is to develop a 100 V to 3.3 V, 50 W DC to DC converter which achieves the best compromise between low mass and high efficiency. A particular emphasis is put on using components qualified for the aerospace environment. The work was carried out through the following steps:

1. Explore all possible topologies which lend themselves to efficiently convert a raw 100 V input bus to a tightly regulated 3.3 V output, galvanically isolated from the input.
2. Among all these topologies, select the one which leads to the highest efficiency and the lowest mass.
3. Optimize the chosen topology.
4. Develop a small signal moded of the selected topology.

In order to validate the calculations and the mathematical models developed, a prototype of a 100 V to 3.3 V, 50 W converter was built with Space qualified components and tested. With this prototype, conversion efficiencies in excess of 87 % (including control circuit consumption) were measured.

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List of Symbols and Abbreviations

C_o	Output Capacitor
C1, C2	Complementary Half Bridge Converter input capacitors
$Coss(V)$	Parasitic output capacitance of a MOSFET as a function of the voltage V applied across it.
C_{GS}	Parasitic Gate to Source capacitance of a MOSFET
$C_{GD}(V)$	Parasitic Gate to Drain capacitance of a MOSFET as a function of the voltage V applied across it.
$C_{DS}(V)$	Parasitic Drain to Source capacitance of a MOSFET as a function of the voltage V applied across it.
C_{tfo}	Main Power Transformer Primary to Secondary parasitic capacitance
C_{pri}	Overall parasitic capacitance connected to the primary side of the main power transformer
C_{sec}	Overall parasitic capacitance connected to the secondary side of the main power transformer
$Coss_{OFF}$	Parasitic output capacitance of a MOSFET in its non-conducting state
$Ciss_{ON}$	Parasitic input capacitance of a MOSFET in its conducting state
CHBC	Complementary Half Bridge Converter
$C(s)$	Small signal control loop compensation transfer function
D	Power Converter Duty Cycle
$E_{Coss}(V)$	Energy stored in a MOSFET output parasitic capacitance as a function of the voltage V applied across it.
E_{Vin}	Energy supplied by voltage source V_{in} during a soft transition
E_{Vc}	Energy supplied by voltage source V_c during a soft transition
E1	Energy stored in the reactive elements at the end of soft transition Phase I

$E2$	Energy stored in the reactive elements at the end of soft transition Phase II
Fs	Switching Frequency
$F(s)$	Small signal open loop input voltage to output voltage transfer function
$F_{cl}(s)$	Small signal closed loop input voltage to output voltage transfer function
$G(s)$	Small signal duty cycle to output voltage transfer function
I_{pk}	Current through the main transformer primary winding at the beginning of the first soft transition (end of Q1's conduction period)
I_{neg_pk}	Current through the main transformer primary winding at the beginning of the second soft transition (end of Q2's conduction period)
I_{Lpri}	Main power transformer primary magnetizing current
$I1$	Current through main power transformer leakage inductance at the end of soft transition Phase I.
$I2$	Current through main power transformer leakage inductance at the end of soft transition Phase II.
I_o	Output current
ΔI_o	Peak to peak variation of output current
ΔI	Peak to peak variation of main power transformer primary magnetizing current
ΔI_{L1}	Peak to peak ripple current in CHBC output inductor L1
ΔI_{L2}	Peak to peak ripple current in CHBC output inductor L2
L_{pri}	Main power transformer primary magnetizing inductance
L_{sec}	Main power transformer secondary magnetizing inductance
L_{lk}	Main power transformer leakage inductance including secondary side stray inductance.
L_{out}	Output filter inductor
$L1, L2$	Complementary pair of output inductors in CHBC current doubler configuration
L_{eff}	CHBC effective output inductance
N	Main power transformer primary to secondary turns ratio
n	Main power transformer secondary to primary turns ratio (= 1/N)
Q1, Q2	Primary MOSFETs
Q3, Q4	Secondary synchronous rectifier MOSFETs
Ts	Switching period
$T(s)$	CHBC small signal loop transfer function

$t1$	Duration of soft transition Phase I
$t2$	Duration of soft transition Phase II
t_{ov1}	Duration of secondary synchronous rectifiers first overlap period
t_{ov2}	Duration of secondary synchronous rectifiers second overlap period
t_{ov}	Total overlap duration ($= t_{ov1} + t_{ov2}$)
V_{in}	Input voltage
V_{out}	Output voltage
V_c	Voltage across clamping capacitor in ZVT Forward Converter
V_{GS}	Gate to Source voltage of a power MOSFET
V_{DG}	Drain to Gate voltage of a power MOSFET
V_{DS}	Drain to Source voltage of a power MOSFET
$V1$	Voltage variation across the main transformer primary winding during the soft transition Phase I.
$V2$	Voltage variation across the main transformer primary winding during the soft transition Phase II.
V_{on}	Voltage drop across one secondary synchronous rectifier in its conducting state
V_{C1}	Voltage across CHBC primary capacitive divider top capacitor
V_{C2}	Voltage across CHBC primary capacitive divider bottom capacitor
$Zo(s)$	CHBC small signal open loop output impedance
$Zo_{cl}(s)$	CHBC small signal closed loop output impedance
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

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Chapter 1
Introduction

1.1 General Introduction

The last decade has seen significant advances in the area of digital microcircuits; our quest for more speed, more performance with even less electrical power consumption has prompted the development of digital microcircuits working off supply voltages as low as 1.5 V. This downwards trend of supply voltages has posed numerous interesting challenges to the power supply designers as they must now cope with new difficulties which are described below.

1. At a given output power, the output current is inversely proportional to the output voltage; this means that currents delivered by low voltage converters are high; as an example, the nominal output current of a 3.3 V, 50 W converter is equal to 15 A. These high output currents, in turn, create substantial voltage drops in their output rectifier and filter stage which are a significant fraction of the (low) output voltage and therefore cause a significant efficiency degradation.

2. The high output currents combined with the low output voltages have a negative impact on the size of the output filters: assuming that the maximum allowed output voltage ripple is a fixed percentage of the output voltage, the allowed output voltage ripple is much lower in a low voltage converter than in a voltage converter of same output

power supplying a higher output voltage. This means that the filter corner frequency must decrease, and therefore the capacitance and/or inductance values of the filter must increase. If we choose not to increase the filter inductance, we must increase the filter capacitance (and therefore its size) in order to comply with the lower output voltage ripple. However, the size of the inductor will increase too, even though its inductance value remained unchanged, because it must now handle a higher DC current.

3. One of the most important advances achieved in the area of digital microcircuits is certainly the high degree of miniaturization; as a result, complex digital functions can now be implemented on a single printed circuit board, which can now operate independently from the neighbouring printed circuit boards. This has created the possibility of building modular digital systems where each module corresponds to a printed circuit board. For high reliability systems such as those found in Aerospace applications, a certain degree of redundancy can be implemented in the system by simply adding more modules to those strictly required by the application; those additional modules remain in a standby mode until failure of one of the working modules forces one of the spare modules to take over operation from the failed module. Such a system can be quite large (30 modules) and its consumption can easily exceed 1.5 kW (50W per module x 30 modules = 1.5kW). For a 3.3 V power converter, an output power of 1.5 kW would correspond to an output current of 450 A. Not only is it quite difficult to design a converter having such a high output current, but also this high current level will create significant distribution losses as the 3.3 V power is conveyed from the converter output to the many modules which compose the whole system. A viable alternative to this situation is to design several lower power converters, each of which would be providing power to a subset of the system modules, in a decentralized manner; the question is to define how many modules each converter should be providing power to. It was pointed out above that in order for the whole system to have a certain degree of redundancy, each module should operate in an independent fashion; therefore a logical

choice is to provide each module with its own dedicated power supply; since a module corresponds to a printed circuit board, the power converter must be located on the board itself or in its immediate neighbourhood. An additional advantage of having the converter residing on the functional board and therefore co-located with its load is that the dynamic voltage drops due to the load current variations are minimized.

1.2 Problem Statement

The requirement of making the converter on-board resident raises the need to miniaturize the converter since only a given percentage (usually small) of the board area is allocated to it. Unfortunately, as is widely known in the power engineering community, the miniaturization requirement is in conflict both with the high efficiency requirement and also with the low output ripple requirement as explained the previous paragraph.

In many cases, the response of the power supply designers to this need of having a on-board resident converter has been to design a simple non isolated buck converter which steps down the +5 V rail to the required lower voltage rail. This approach is justified by the coexistence, on the same PC board, of circuits requiring +5 V and circuits requiring +3.3 V or lower supply voltages. Although simple, this approach is ineffective for the following reasons:

1. If the +5 V rail is supplied by a centralized converter, then the failure of this converter causes the loss of the whole system, which defeats the redundancy requirement. Moreover, a centralized converter supplying the +5 V rail to the whole system leaves the systems engineer faced with the high distribution losses as explained in (3) above. If the +5 V rail is supplied by a localized converter, then the overall size of this converter and the low voltage converter will be significantly higher than the size of a single low voltage converter operating from the input line.

2. Although a non isolated buck converter which takes its input from the +5 V can be designed with efficiencies in the order of 95 %, the overall efficiency of providing the low voltage rail (+3.3 V or lower) is equal to the product of the +5 V converter efficiency and the buck converter efficiency, which makes the double stage conversion inefficient.

From the above discussion, the only viable alternative lies in a single stage converter which turns the input voltage directly into +3.3 V and provides galvanic insulation between input and output.

1.3 Literature Review

Several topologies have been proposed to convert a medium to high input voltage source into a low output voltage ; a common viewpoint expressed in most of the literature reviewed is the need for secondary synchronous rectifiers, as opposed to Schottky diodes ; in addition, these synchronous rectifiers should be self driven, i.e. their driving signals should be derived from the waveforms appearing on the power transformer secondary winding in order to avoid the added complexity of dedicated gate drive circuitry. Therefore, the problem is to apply a suitable waveform to the gates of the synchronous rectifiers, such that those will remain in full conduction during their conduction interval ; this waveform is shown to be very much dependent on the topology. Comparative studies carried out in [7], [8] and [9] conclude that high frequency resonant topologies are inadequate because the waveforms applied to the gates of the synchronous rectifiers are sinusoidal and hence, they fail to maintain the MOSFETs in full conduction throughout the conduction period. For the same reason, classical Pulse Width Modulation symmetrical topologies are unanimously rejected because inherent to their operation is a dead time during which zero volt is applied to the gates of the secondary synchronous rectifiers; this results in the conduction of the associated antiparallel diode of the MOSFET rather than of the MOSFET itself ; as these

diodes typically have a forward voltage drop much higher than that of the MOSFET, this has a negative impact on efficiency.

As a result, most of the recent research on low output voltage converters focuses on asymmetrical topologies where typically two switching MOSFETs operate in a complementary fashion [1 – 9], [13 – 16] ; this results in no dead time and consequently no zero voltage gap on the gates of the synchronous rectifiers ; in turn, this maximizes their utilization and hence, improves overall efficiency. Furthermore, the complementary operation is taken one step further by introducing a small delay between the turn-off of one of the complementary MOSFETs and the turn-on of the other. It is shown that if sufficient magnetizing energy is stored in the power transformer at the moment the first MOSFETs is turned off, then a natural or "soft" commutation takes places which eventually results in the second MOSFET being turned on under zero voltage. This has the effect of dramatically reducing the switching losses and therefore, paves the way for higher switching frequencies at little penalty in terms of efficiency.

The proposed topologies which take advantage of the complementary operation as well as the Zero Voltage Transition (ZVT) phenomenon are basically derived from classical topologies. The ZVT Forward Converter is described in [1 – 3], [7] and [8]. The ZVT Complementary Half Bridge Converter is described in [4 – 6] and [9]. In [13 – 16], a variant of the above topologies is proposed which utilizes the concept of output current doubling, based on earlier work described in [11] and [12]. In [17] and [19], a modification of conventional Forward and Flyback topologies is described whereby an auxiliary circuit is employed to achieve the desired Zero Voltage Switching. Finally, the phase shift modulated Dual Active Bridge is described in [10].

The choice of one topology versus another is complex and depends on parameters such as input voltage, output power, variations of input voltage and output current, total number of semiconductors and hence cost. One contribution of this thesis is an attempt to

develop objective criteria which lead to the choice of one topology given a set of operating conditions.

1.4 Scope and Contributions of this Thesis

The purpose of this thesis is two-fold:

1. Explore different topologies which make use of the soft commutation phenomenon and determine which topology will lead to the highest conversion efficiency under a given set of operating conditions. In order for this comparative study to be successful, it is necessary to analyze in detail the mechanisms which govern the phenomenon of Zero Voltage Transition (ZVT).

2. Build a prototype based on the selected topology. The small size requirement for this type of on-board resident converter can only be satisfied if the converter is miniaturized by such techniques as "Chip on Board"; this miniaturization effort is beyond the scope of this work; therefore, only a prototype with conventional, packaged components will be developed; however, as a step towards miniaturization, low profile transformers where the windings lie on a printed circuit board will be experimented.

The main contributions of this thesis are the following:

1. The development of a mathematical model which, for a given topology precisely calculates the amount of reactive energy which must be stored in the transformer magnetizing inductance in order to achieve a full ZVT. This mathematical model takes into account the non-linear nature of the switching MOSFET parasitic capacitances. Once the magnetizing current required for a full ZVT has been determined, the RMS values of the currents through the transformer windings and through the primary and secondary MOSFETs can be calculated which in turn enables a precise calculation of the conduction losses. These conduction losses are then compared to those incurred in

other topologies ; the topology retained is the one which exhibits the lowest conduction losses.

2. Based on the results of the above model, a more general mathematical model is developed which, for a given topology and a given switching frequency precisely calculates the size of the converter power stage and the converter overall efficiency. The results obtained from this model allow a quick determination of the optimum switching frequency.

3. The development of dynamic large signal and small signal models for the selected topology in an output current doubler configuration.

1.5 Thesis Outline

The contents of this thesis are organized as follows:

In Chapter 2, a comparative study is carried out between three topologies using the concept of ZVT, in terms of their conduction losses. This comparative study is based on a mathematical model which, for a given topology, precisely calculates the amount of primary magnetizing inductance required for ZVT to occur. For each topology, a PSPICE model of the converter which includes the MOSFET non-linear capacitances is developed in order to validate the results obtained from the mathematical model. The topology selected is the one exhibiting the lowest conduction losses.

Chapter 3 is devoted to the design and construction of a prototype based on the selected topology. The waveforms measured on the prototype are compared to those predicted by the PSPICE model corresponding to the selected topology. A more general mathematical model is developed which, for any switching frequency precisely calculates the overall efficiency. The efficiencies obtained from this mathematical model are then compared to those measured on the prototype operating under the same conditions. The same mathematical model also calculates the size of the converter power stage for a given

set of constraints and operating conditions, and for different switching frequencies. This in turn allows a quick determination of the optimum switching frequency, i.e. the frequency corresponding to the minimum size.

Chapter 4 is devoted to the large signal and small signal modelling of the converter. Analytical expressions and PSPICE models are developed to predict the main transfer functions as well as the transient responses of the converter. The predicted frequency and transient responses obtained from the models are then compared to those measured on the real prototype.

Chapter 5 summarizes the work carried out in this project, the results obtained, the conclusions and the areas requiring future research and development.

Chapter 2
A Comparative Study of Several Topologies

2.1 Introduction

The purpose of the low voltage DC to DC converter we are to develop is to provide power to many identical digital boards located side by side. In such configurations, system redundancy requirements dictate that each individual board be powered by its own dedicated converter. This results in a large number of identical converters each of which typically resides on the functional board it is providing power to or in the immediate neighborhood of it (for example on a backplane to which the functional board is connected).

This situation results on one hand in a tight volume constraint because each local converter occupies a portion of the functional board where it resides and on the other hand, it imposes a severe efficiency requirement; the high efficiency demand which is put on the converter is the direct result of the high power typically consumed by modern digital On Board processing systems.

It will be shown in this chapter that the two conflicting requirements of low volume and high efficiency can only be met with a class of topologies which allow a high frequency of operation while avoiding the high switching losses normally associated with a high switching frequency. These topologies make use of soft commutations and complementary operation between the different power switches.

2.2 Choice of a Topology

The choice of a topology is dictated by several factors which are:

- Input voltage and its variations
- Input to output isolation requirement
- Total output power
- Voltage and current ratings of the power semiconductors
- Number of output rails
- Input current ripple requirement
- Output voltage ripple requirement
- Volume constraints
- Efficiency requirement

The requirements of the converter we are to develop are summarized in Table 2.1 below.

Table 2.1 Low Output Voltage Converter Specifications

Input voltage	90 V DC to 110 V DC
Output voltage	3.3 V, electrically isolated from the input
Output voltage ripple	10 mV peak to peak
Load and Line regulation	± 1 %
Output power	30 W to 60 W
Efficiency	87 % at an output power of 50 W
Size	2.5" × 4" × 0.75"
Frequency of operation	350 kHz to 500 kHz

The output power of 50 W corresponds to the maximum predicted consumption of a digital printed circuit board.

The input voltage of 100 V corresponds to one of the three bus voltages which are becoming standard in the Aerospace world, the other two being the 70 V bus and the 50V bus. The 100 V bus was deliberately chosen for this work since it corresponds to the worst case in terms of efficiency.

The small envelope specified in Table 2.1 imposes a high switching frequency in order to reduce the size of the switching transformer and filtering magnetics. Early estimates suggest that the optimum frequency of operation may lie between 200 kHz and 500 kHz.

It should be noted that the frequency of operation is determined by the minimum efficiency and maximum volume goals.

The low output voltage, in conjunction with the high efficiency goal dictates the use of synchronous rectifiers at the output in order to reduce the conduction losses. Unfortunately, synchronous rectifiers may increase the switching losses if proper caution is not exercised in the timing of their gate drive signals.

The conflicting requirements of high switching frequency and high efficiency (which means low conduction and switching losses) can only be met with a topology which meets the following conditions:

1. Complementary operation among the following pairs of switches:
    a) Primary switch No. 1 vs. Primary switch No. 2
    b) Sync. Rectifier No. 1 vs. Sync. Rectifier No. 2
2. Primary Switch vs. Sync. Rectifier for topologies like the Flyback which only have one switch on the primary and one switch on the secondary.
3. Zero voltage turn-on (ZVT) for all the semiconductor switches, be they located on the primary or on the secondary side.

Complementary operation between two transistors Q1 and Q2 means that Q1 conducts during one portion of the switching period, and that Q2 conducts during the remainder of the period. Q1's conduction time is usually called $D \times Ts$, where D designates the duty cycle and Ts the switching period. Then, Q2's conduction time equals $(1\text{-}D) \times Ts$.

Ideally, the complementary operation should be a true one, i.e. there should be no conduction overlap and no dead time.

This complementary operation is desirable for the following reasons:

1. Any conduction overlap means that Q1 and Q2 are simultaneously conducting; this situation, if not well controlled, leads to momentary current spikes which in turn cause an increase of conduction and switching losses.

2. Any significant dead time between the conduction of Q1 and Q2 always results in no synchronous rectifier being ON, whether Q1 and Q2 represent the sync. rectifiers themselves or the primary transistors. This means that during this dead time, the output current is being carried by the internal antiparallel diodes inherent to the sync. rectifiers MOSFETs; since these diodes have a forward drop significantly higher than the MOSFET, conduction of these diodes causes a significant increase of conduction losses.

3. Complementary conduction is the only mode of operation which allows zero voltage turn-on of the transistors.

Zero voltage turn-on for a MOSFET (also called "soft" transition) means that when a voltage is applied between its Gate and Source terminals to turn it ON, the voltage between its Drain and Source terminals must already be zero. In practice, this means that the internal Body-Drain diode is already conducting reverse current when the ON command is applied to the gate of the MOSFET. This mode of operation is desirable because it avoids the dissipation in the MOSFET of the energy stored in its parasitic capacitance, which normally occurs during a "hard" turn-on. At high switching frequencies, this dissipated energy represents a significant amount of power, which is calculated as follows:

It is shown in Appendix B that the output capacitance of a MOSFET can be expressed as

$$Coss(V) := \frac{Cdso}{\sqrt{1 + \frac{V}{0.8}}} + \frac{Cgdo}{(A + V)^{\gamma}} \qquad (2.2.1)$$

The first term of (2.2.1) represents the drain to source capacitance, whereas the second term represents the drain to gate capacitance. The coefficients of (2.2.1) have been calculated in Appendix B for several MOSFETs. In order to calculate the energy wasted during a hard turn-on, we must consider that the MOSFET which is being turned on must not only discharge its own output parasitic capacitance, but it must also charge the parasitic capacitance of the MOSFET connected in series with it (see Figure 2.10); in addition, it must also charge the transformer parasitic capacitance. With reference to Figure 2.10, (which represents the best case in terms of turn-on losses), we shall assume that the voltage at the connection point of the two MOSFETs equals $0.5 \times V_{in}$ or 50 V at the moment the lower transistor Q1 is being turned on; we also assume that the transformer parasitic capacitance equals 250 pF (measured on a real PCB transformer); the elemental energy being dissipated when the capacitances are being discharged from V to $V - dV$ is equal to

$$dE = V \cdot dQ = V \cdot C_{eq}(V) \cdot dV = \left(Coss(V) + Coss\left(V_{in} - V\right) + C_{tfo}\right) \cdot V \cdot dV \qquad (2.2.2)$$

In the above expression, $Coss(V)$ represents the output capacitance of MOSFET Q1 which is being turned on and whose drain to source voltage equals V. On the other hand, $Coss(V_{in} - V)$ represents the output capacitance of the upper transistor Q2 whose drain to source voltage equals $V_{in} - V$. The equivalent capacitance C_{eq} must be discharged from 50 V to zero; we choose the MOSFETs as IRFM250 (whose capacitance coefficients are calculated in Appendix B) and we take a switching frequency of 300 kHz. Therefore, the turn-on losses are equal to

$$P_{ON} := \left[\int_{0}^{\frac{V_{in}}{2}} \left(Coss(V) + Coss\left(V_{in} - V\right) + C_{tfo} \right) \cdot V \, dV \right] \cdot 2 \cdot Fs \qquad (2.2.3)$$

$$P_{ON} = 1.105 \quad \text{W}$$

In the above equation, the coefficient 2 accounts for two hard turn-ons per period. As can be seen, the power dissipated due to hard turn-on equals 1.1 W at 300 kHz and will increase proportionally to the switching frequency. This dissipation of 1.1 W represents an efficiency loss of 2 % at an output power of 50 W and is considered unacceptably high. Again, it must be stressed that the above calculation corresponds to the best case. Therefore, if we are to operate at frequencies equal to or higher than 300 kHz, the only viable alternative is Zero Voltage turn-on.

Zero voltage turn-on is achieved in the following way. If Q1 and Q2 represent two primary MOSFETs connected such as in Figure 2.2 below, turning off Q1 causes the magnetic energy stored in the transformer during the conduction time of Q1 (either in the leakage inductance or in the magnetizing inductance) to charge Q1's parasitic capacitance and to discharge Q2's parasitic capacitance.

If the magnetic energy is high enough, then the two parasitic capacitances are fully discharged and Q2 starts conducting reverse current through its antiparallel diode.

If an ON command is then applied to the gate of Q2, the latter is being turned on under zero Drain-Source voltage. Subsequently, circuit operation causes the current through Q2 to become positive and the same phenomenon occurs when Q2 is turned off.

It should be noted however that the soft transition just described is only possible in topologies where Q1 and Q2 are driven in a complementary fashion.

If a significant dead time existed between Q1 and Q2 conduction, not only would Q1 and Q2 experience a "hard" turn-on but also all the magnetic energy which could have otherwise been utilized to turn on the complementary transistor under zero voltage is now totally wasted, which creates additional losses.

Four topologies so far have been found to meet the above requirements:

1. The dual active bridge converter (Figure 2.1).
2. The active clamp single ended forward converter with high magnetizing primary current (Figure 2.2).
3. The complementary half bridge converter (Figure 2.10).
4. The continuous mode flyback converter (Figure 2.18).

It should be noted that all classical Pulse Width Modulation topologies were rejected because inherent to them is a dead time in the conduction of the primary transitors which leads to the undesirable effects described above.

The first three topologies are derived from classical PWM topologies. The dual active bridge is a topology where the primary and secondary switches are externally driven and where the power throughput is a function of the phase shift between the primary and secondary bridges.

As mentioned above, the two conditions which must be met in order to achieve ZVT are:

1. Complementary operation.
2. Enough magnetic energy must be stored in the transformer on the primary side in order to fully charge/discharge the MOSFET parasitic capacitances.

The maximum output power of the +3.3 V EPC is equal to 50 W. At that power level, it was found that insufficient energy was being stored in the leakage inductance of the transformer in order to guarantee ZVT; therefore, these topologies were modified in order to increase the magnetizing current of the transformer so as to increase the energy stored in the magnetizing inductance.

Referring to the diagrams at the bottom of Figure 2.2, Figure 2.10 and Figure 2.18, the solid line waveform represents the primary current of the modified circuit whereas the dotted line represents the primary current of the original circuit.

As can be seen from the diagrams, the solid lines have a much steeper slope than the corresponding dotted lines, which causes the minimum current I_{min} to be negative. This negative value of I_{min} guarantees ZVT of Q1 because it represents the current going initially through its antiparallel diode. It should be noted that ZVT operation of the Flyback converter (Figure 2.18) is impossible without this modification.

The modification of the primary current cannot be implemented on the dual active bridge (Figure 2.1) because in this topology the transformer is being actively driven from both the primary and the secondary sides [10]. Therefore, the voltage across the transformer does not change when Q1 is turned off since it is determined by the conduction status of Q3 and Q4. Therefore, only the leakage inductance (or external series inductance Ls) is available to charge and discharge the MOSFET parasitic capacitances. As a consequence, this converter does not lend itself to handle an output power in the order of 50 W and hence will not be studied any further. The interested reader may refer to [10] for a detailed description of this circuit.

The modification of the primary current described above carries a penalty which is an increase of the RMS value of the primary current, which in turn causes an increase of conduction losses. The impact of these additional conduction losses on the overall EPC efficiency depends on the topology. In the next paragraph, we will calculate for each of the

three topologies under consideration the amount of magnetizing current which must be added to the primary current in order to guarantee ZVT operation.

In addition to achieving ZVT, an important parameter to consider is the time it takes to do so, that is the amount of time it takes the combined primary load current and magnetizing current to completely discharge the MOSFET parasitic capacitances. This time interval represents a dead time, i.e. a time during which insufficient or no voltage is applied to the gate of the secondary synchronous rectifier MOSFETs. It is therefore mandatory to minimize this transition time and this can only be done by increasing the primary magnetizing current beyond the value strictly needed to perform ZVT. As explained further in the next paragraph, one of the constraints we will be imposing on the three competing topologies is to perform ZVT in less than 200 ns.

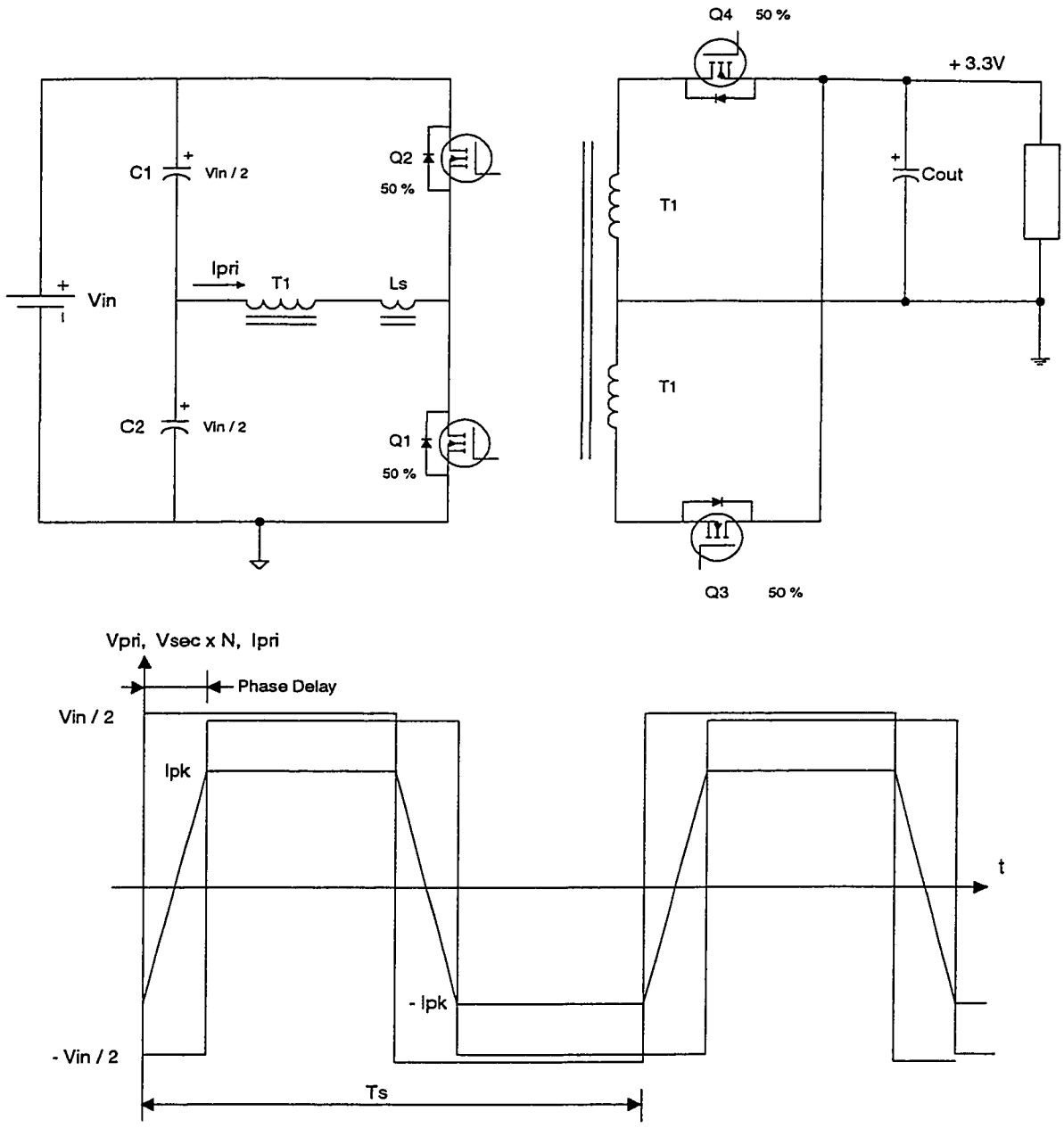


Figure 2.1 Dual active bridge converter

2.3 Comparison Criteria

For the three topologies being studied, if we increase the primary magnetizing current in order to guarantee ZVT in each of them, then the turn-on losses become negligible.

It will be shown in Chapter 3 that by properly designing the gate drive circuit, the turn-off losses can be made negligible too. Therefore, the final choice of the topology can only be made after a comparison of conduction losses for topologies No. 1, No. 2 and No. 3 is carried out.

This comparison of conduction losses for all three topologies will be made based on the following operating conditions and constraints:

Input voltage : 100 V

Output power : 50 W

For all three topologies, the secondary winding of the transformer is assumed to have the same resistance per section, in order to provide a fair basis of comparison. The resistance of the primary winding was taken as the secondary winding resistance multiplied by the square of the turns ratio.

All three topologies use two secondary synchronous rectifiers. (In the Flyback converter, they are connected in parallel). For the active clamp single ended forward converter and for the complementary half bridge converter, the secondary synchronous rectifiers are self driven, i.e. their gate to source voltage is derived from the power transformer secondary winding voltage waveform. For the Flyback converter, the secondary synchronous rectifiers are externally driven. For all three topologies, the synchronous rectifiers used are Logic Level MOSFETs FSYC053LD made by HARRIS which are presently under development. The Logic Level MOSFET was chosen because in a self-driven scheme, and due to the low value of the output voltage, insufficient voltage is

developed across the transformer secondary winding to drive a conventional MOSFET. The HARRIS MOSFET was chosen because it is radiation hardened, which is a requirement in most aerospace applications.

The primary MOSFETs used depend on the topology. In the Complementary Half Bridge, the maximum Drain to Source voltage of the primary switches never exceeds the input voltage; since the input voltage does not exceed 110 V, 200 V MOSFETs are used. In the ZVT Flyback converter, it will be shown that the Drain to Source voltage of the primary MOSFETs will not exceed 145 V; therefore, 200 V MOSFETs can also be used. In the active clamp forward converter, the Drain to Source voltage of the primary MOSFETs will be significantly higher than the input voltage; therefore, 400 V MOSFETs are used for this topology.

Although V_{in} equals 100 V, The power stages of all three topologies were designed to handle input voltage variations ranging from 90 V to 110 V.

For all three topologies, the combined primary load current and magnetizing current must have a value such as to guarantee a ZVT in less than 200 ns.

Having defined all the constraints and criteria, it is now necessary that we undertake a more detailed study of each topology in order to accurately calculate the amount of primary current needed to perform ZVT in less than 200 ns.

2.4 The active clamp single ended forward converter

The simplified schematic and the primary current waveform of the active clamp single ended forward converter are shown on Figure 2.2 below. The theory of operation is identical to that of a conventional PWM single ended forward converter with the following modifications, which are covered in detail in [1], [2], [14], [15] and [16]:

When Q1 turns off, the energy stored in the transformer magnetizing and leakage inductances charges the parasitic capacitances of Q1 and discharges the parasitic capacitance of Q2 until the Drain to Source voltage of Q1 is clamped by capacitor C1 through Q2's antiparallel diode. At this time, Q2 is turned ON for the remainder of the switching period whose duration is given by $(1-D) \times Ts$. Since the lower end of the transformer primary is now held at a voltage higher than the input voltage, the magnetizing current through the transformer decreases and eventually changes sign.

At the beginning of the next switching period, Q2 is turned OFF. Since the magnetizing current of the transformer is now negative, it starts charging Q2's parasitic capacitance and discharging Q1's parasitic capacitance until Q1's antiparallel diode conducts. At this time, Q1 is turned ON. It should be noted that under those conditons, both Q1 and Q2 experience a Zero Voltage turn-on; for this to occur however, the magnetizing inductance of the transformer must be lower than the one of a conventional forward converter in order to allow the transformer to store energy during the conduction periods of Q1 and Q2; as explained above, this is why the solid line of the current waveform in Figure 2.2 has a steeper slope than the dotted line which corresponds to the current waveform of a conventional converter.

Since the voltage across the switching transformer is either positive or negative but never zero (no dead time), both secondary synchronous rectifiers are always being driven on their gates in a complementary fashion, with the exception of the transition periods where

Q1 and Q2's parasitic capacitances are charged and discharged. Moreover, since the gate to source voltage of the synchronous rectifiers is synchronized with their drain to source voltage (the gate to source signal is derived from the transformer secondary winding), the synchronous rectifiers also turn on under zero voltage on their drain.

Before we attempt to calculate the minimum amount of primary current needed to achieve ZVT, it is necessary to perform a rough design of the converter in order to extract the important parameters such as the transformer turns ratio, nominal and worst case duty cycle.

The detailed calculations are performed in Appendix A; the complete characterization of the primary and secondary power MOSFETs used is performed in Appendix B; therefore, only the important steps will be outlined in this chapter.

The voltage across the clamping capacitor C1 is easily calculated by noting that the transformer is always being driven in one direction or the other and must therefore satisfy the volts - microseconds balance.

Therefore, $V_{C1} = \frac{D \cdot V_{in}}{1 - D}$

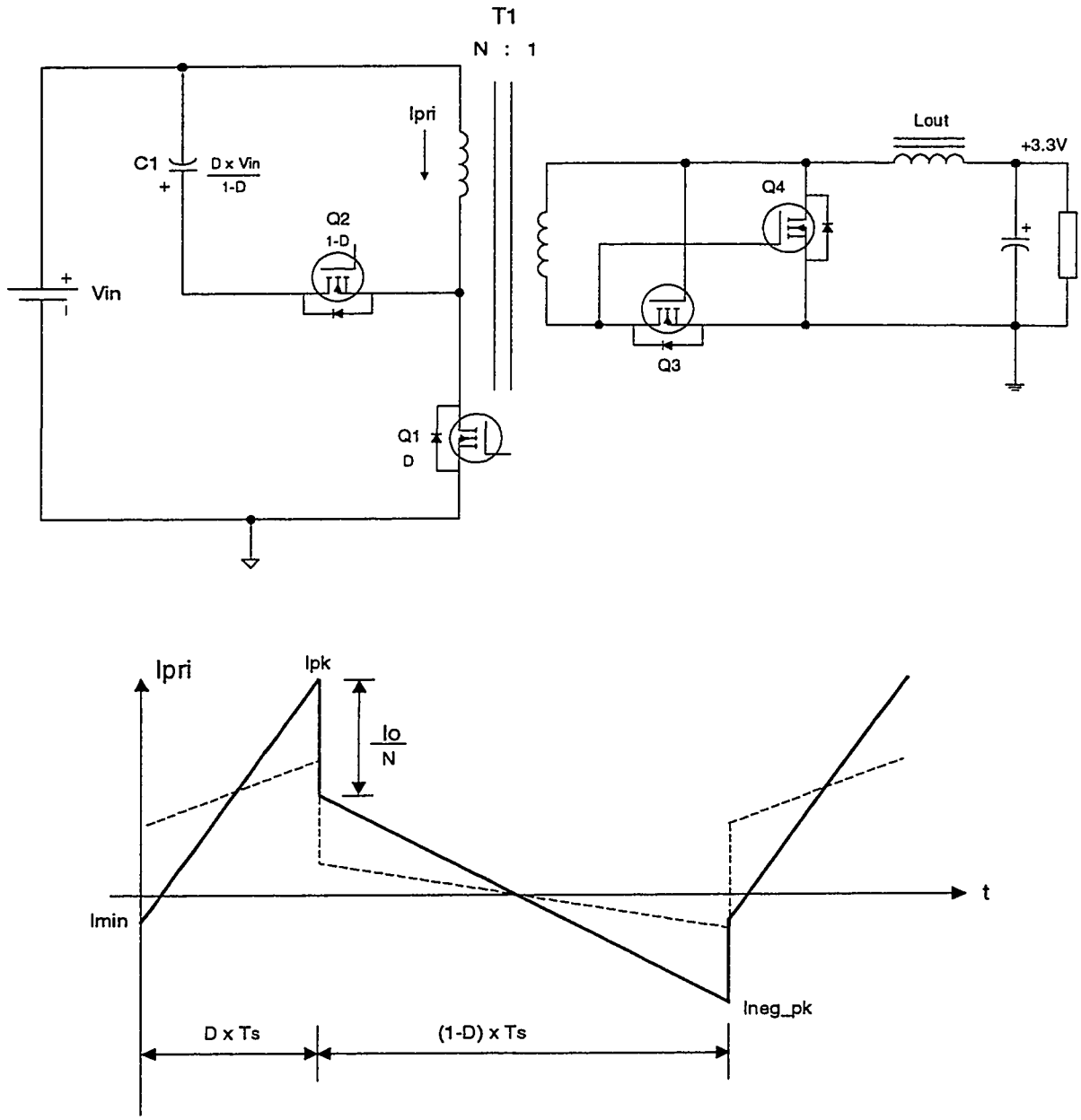


Figure 2.2 Forward converter with active clamp and self driven synchronous rectifier

The Drain to Source voltage of Q1 and Q2 is equal to

$$V_{DS} = V_{in} + V_{C1} = \frac{V_{in}}{1 - D} \tag{2.4.1}$$

We pose the constraint that the maximum V_{DS} across the primary switches never exceeds 300 V (consistent with the use of 400 V devices); let's find the condition where V_{DS} reaches its maximum value; from the above expression of V_{DS} given in (2.4.1), we have

$$V_{DS} = \frac{V_{in}}{1 - D} = \frac{N \cdot V_{out}}{D \cdot (1 - D)}$$

where N is the power transformer turns ratio.

The above expression only depends on the duty cycle (the numerator is constant); from the denominator expression, it can be seen that V_{DS} reaches a minimum when $D = 0.5$ and increases for values of D higher than 0.5. On the other hand, it is desirable to run the converter at duty cycles higher than 0.5 in order to reduce the output inductor ripple current and hence the output voltage ripple; if the converter always operates above 50 % cycle, then the above expression of V_{DS} reaches its maximum when D is maximum; this corresponds to V_{in} being minimum; we know that $Vin_{min} = 90$ V; therefore, we readily calculate the maximum duty cycle:

$$D_{max} := 1 - \frac{Vin_{min}}{300} \qquad D_{max} = 0.7$$

Let us now calculate the transformer turns ratio N.

Figure 2.3 below shows the Forward Converter secondary rectifier stage along with the waveforms of the voltage across the transformer secondary, the voltage at point A on the schematic and the secondary current.

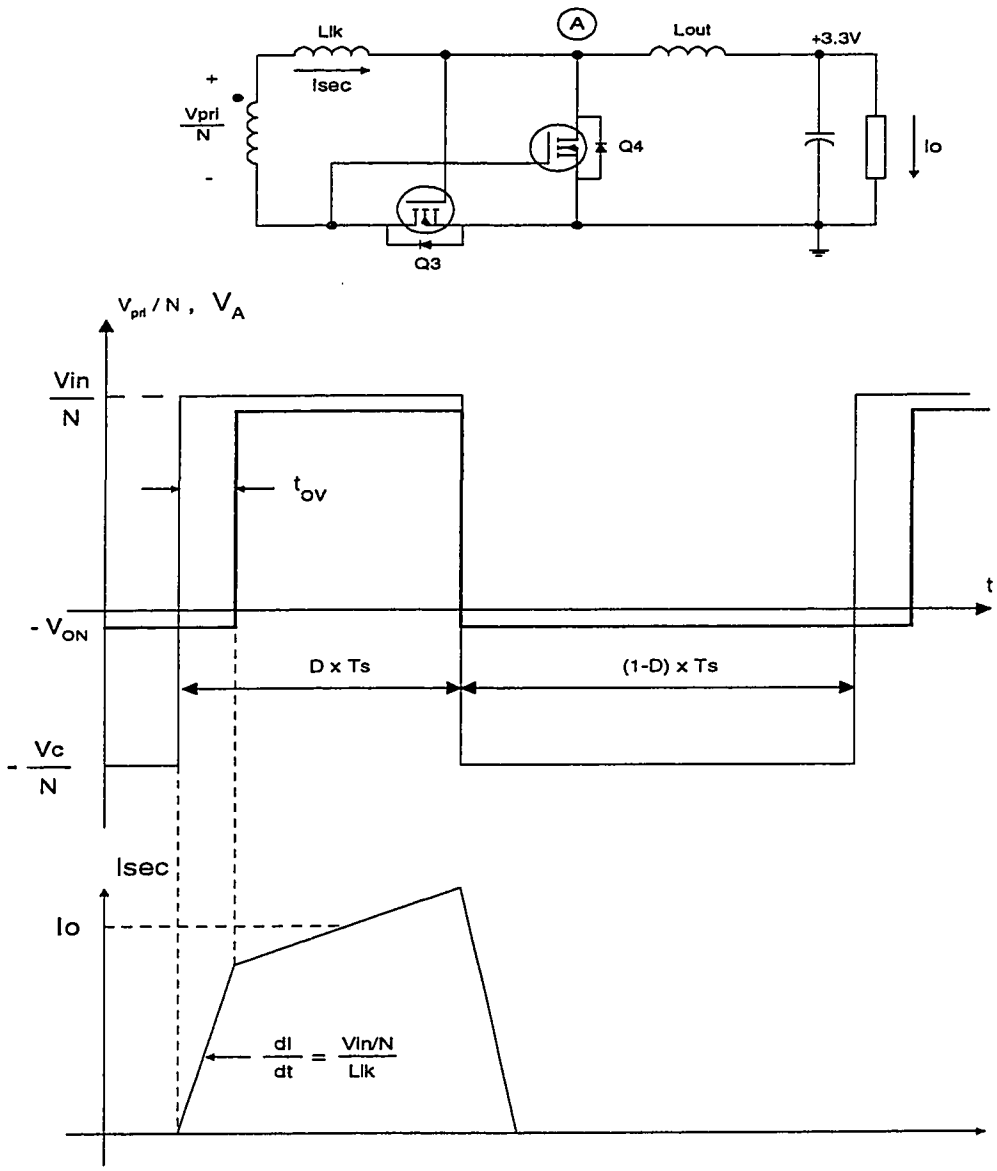


Figure 2.3 Forward Converter Secondary Rectifier Stage Showing Effect of Leakage Inductance

As can be seen from Figure 2.3 , when the secondary voltage becomes positive, the voltage at point A stays at zero for a period of time t_{ov} during which the output current is gradually transferred from Q4 to Q3; during this time, both Q3 and Q4 conduct through their antiparallel diodes because V_{GS} of both Q3 and Q4 are equal to zero. Neglecting the

ripple current through the output inductor and assuming the reverse recovery current of Q4's body-drain diode is negligible, the overlap time is given by

$$t_{ov} = \frac{L_{lk} \cdot I_o}{\left(\frac{V_{in}}{N}\right)} \tag{2.4.2}$$

where L_{lk} is the leakage inductance value as seen from the secondary.

On the other hand, the time overlap diminishes the converter effective duty cycle; if we call V_{on} the voltage drop across Q3 or Q4 when they conduct, the expression of the output voltage is given by

$$V_{out} = \frac{V_{in}}{N} \cdot \frac{D \cdot Ts - t_{ov}}{Ts} - V_{on} \tag{2.4.3}$$

where Ts is the switching period.

It should be noted that if t_{ov} is made equal to zero, the above expression reduces to the classical input to output relationship for a forward converter.

Introducing the expression of t_{ov} given by (2.4.2) in (2.4.3) yields:

$$V_{out} = \frac{V_{in}}{N} \cdot D - L_{lk} \cdot I_o \cdot Fs - V_{on} \tag{2.4.4}$$

where $Fs := \frac{1}{Ts}$ is the switching frequency.

From (2.4.4), it can be seen that the leakage inductance introduces an extra term proportional to the switching frequency and to the output current; this effect has been described in detail in [3].

Based on the above considerations, we can now calculate the minimum turns ratio needed to achieve output regulation at minimum input voltage and maximum load ($I_o = 15$ A):

Assuming that L_{lk} is equal to 33 nH (measured on a real breadboard with a low profile transformer), and with the value of V_{on} calculated in Appendix A, we obtain

$$N := \frac{D_{max} \cdot Vin_{min}}{V_{out} + V_{on} + L_{lk} \cdot I_o \cdot Fs} \qquad N = 17.331$$

We choose $N = 17$.

With the above value of N, the maximum and nominal values of V_{DS} on the primary MOSFETs corresponding respectively to $V_{in} = Vin_{min} = 90$ V and $V_{in} = Vin_{nom} = 100$ V are calculated in Appendix A:

$Vds_{max} = 283.8$

$Vds_{nom} = 259.4$

We must now calculate the maximum magnetizing inductance of the transformer which will guarantee ZVT in less than 200 ns. Referring to the current waveforms shown on Figure 2.2, it should be noted that the current value Ipk (at the end of Q1's conduction period) is higher than the current value Ineg_pk (at the end of Q2's conduction period); thus, the latter represents the worst case because less energy is stored in the transformer magnetizing inductance to achieve ZVT. Therefore, if we can guarantee that ZVT takes place in less than 200 ns when Q2 is being turned off, then automatically the condition will be met when Q1 is turned off. Therefore, we shall study ZVT on the converter at the turn-off of Q2 only.

In order to do so, it is important to recognize that the parasitic MOSFET capacitances which play an important role in the phenomenon are not constant but rather

are functions of the applied voltage, as explained in paragraph 2.2 above. As a result, the energy exchange phenomena which we will be analyzing are non linear in nature. As explained in [5], the voltage transition takes place in two phases:

Phase I: A resonant transition takes place between the equivalent primary capacitance, the transformer leakage inductance and the equivalent secondary capacitance. The equivalent primary capacitance is the sum of the primary MOSFETs parasitic capacitances and the transformer capacitance; the equivalent secondary capacitance is the sum of the secondary MOSFETs parasitic capacitances. This phase ends when the voltage across the secondary capacitance reaches zero. At this moment, MOSFET Q3 (see Figure 2.2) starts to conduct through its anti-parallel diode and the secondary current is being gradually transferred from Q4 to Q3. Figure 2.4 below is the equivalent schematic of the forward converter during Phase I. Also represented on Figure 2.4 are the voltages across the capacitances and the current through the leakage inductance at the beginning of the phase.

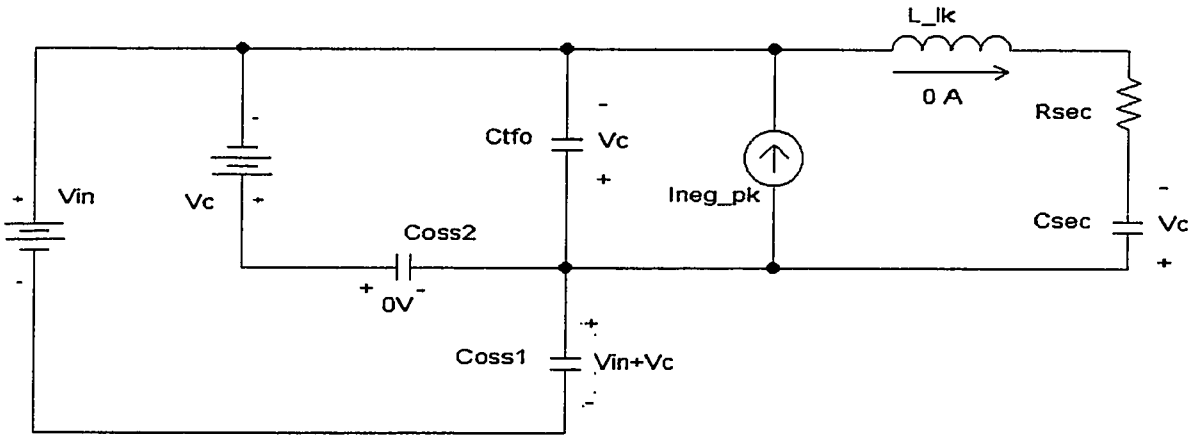


Figure 2.4 Forward Converter Equivalent Circuit During Phase I

Phase II: During this phase, the voltage across the equivalent secondary capacitance is clamped to zero because both secondary synchronous rectifiers are ON and the output

current is being transferred from one synchronous rectifier to the other; this phase consists in a resonance between the equivalent primary capacitance and the transformer leakage inductance. This phase ends when the current through the synchronous rectifier which is being turned off has reduced to zero; in practice however some negative current will flow through the synchronous rectifier being turned off due to the reverse recovery of its antiparallel diode; this means that the overall current excursion is higher than the output current. Figure 2.5 below is the equivalent schematic of the forward converter during Phase II, which also shows the voltages across the capacitances and the current through the leakage inductance at the beginning of the phase.

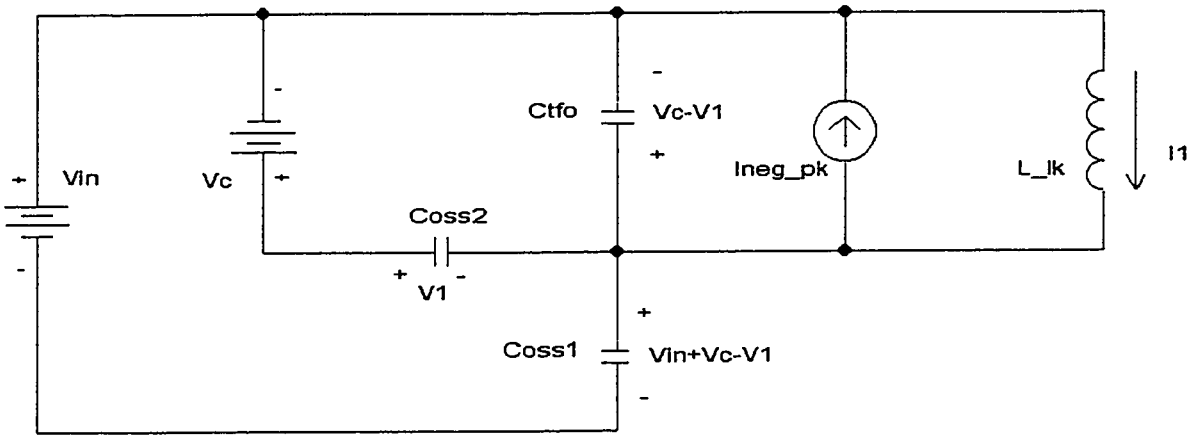


Figure 2.5 Forward Converter Equivalent Circuit During Phase II

Referring to Figure 2.4, voltage source V_c represents the clamping capacitor C1 of Figure 1.2. Since the transition will last less than 200 ns (this is one of the conditons we must meet), we can safely neglect the voltage variation across this capacitor during the transition, and therefore the clamping capacitor can be represented by voltage source V_c. Current source I_{neg_pk} represents the primary current at the end of Q2's conduction period: it is the sum of the load current and the magnetizing current stored in the transformer primary magnetizing inductance. Again, we make the assumption that this current remains constant

during the whole transition. *Coss*2 represents the output capacitance of primary MOSFET Q2 and is completely discharged at the beginning of Phase I, which corresponds to the instant Q2 is being turned off; *Coss*1 represents the output capacitance of Q1 and is charged at $V_{in} + V_c$ at the beginning of Phase I; C_{tfo} represents the transformer parasitic capacitance and is charged to V_c. C_{sec} is the overall capacitance of the secondary MOSFETs, reflected to the primary side of the transformer; at the beginning of Phase I, it is also charged to V_c. Rsec represents the gate resistance of the secondary MOSFETs, reflected to the primary side.

Although the MOSFET parasitic capacitances are non linear and can only be represented by an equation such as (2.2.1), the resonant transition of Phase I involves too many elements and its description by non linear capacitances would make the calculations too complex. Rather, a good approximation is obtained by averaging expression (2.2.1) over the voltage range covered by each of the identified capacitances during Phase I.

Referring to Figure 2.2, when Q2 is turned off, Q3 is OFF and Q4 is ON. Therefore, the secondary capacitance consists of Q4's input capacitance (constant), in parallel with Q3's output capacitance, whose value is averaged from zero to V_c / N. Referring to Appendix A, the averaged value of Q3's output capacitance is given by

$$Coss_{OFF} = \frac{1}{\left(\frac{V_c}{N}\right)} \cdot \int_0^{\frac{V_c}{N}} Coss_{sec}(V)\, dV \qquad \text{(A.4)}$$

The overall secondary capacitance as seen from the primary of the transformer is given by

$$C_{sec} = \frac{Ciss_{ON} + Coss_{OFF}}{N^2} \qquad \text{(A.5)}$$

where $Ciss_{ON}$ represents Q4's input capacitance, $Coss_{OFF}$ represents the average value of Q3's output capacitance and N is the transformer turns ratio.

From Figure 2.2 again, the primary capacitance consists of the parallel combination of Q1's output capacitance, Q2's output capacitance and the transformer's capacitance; while the latter is constant, Q1 and Q2's output capacitances must be averaged over their respective voltage ranges. The overall primary capacitance is given by

$$C_{pri} = \frac{1}{V_c \cdot M_{ov}} \cdot \left(\int_0^{V_c \cdot M_{ov}} Coss(V)\, dV + \int_{V_{in} + V_c - V_c \cdot M_{ov}}^{V_{in} + V_c} Coss(V)\, dV \right) + C_{tfo} \tag{A.6}$$

where M_{ov} is a correction factor which accounts for the fact that the primary voltage actually extends beyond V_c during Phase I.

The analytical expressions of the current through the leakage inductance, the voltage across the secondary capacitance and the voltage across the primary capacitance (the latter being defined as the voltage across C_{tfo} as shown on Figure 2.4) have been calculated in Appendix A and are given by

$$I_{L\_lk}\left(I_{neg\_pk}, t\right) = \frac{I_{neg\_pk} \cdot C_{sec}}{C_{pri} + C_{sec}} \cdot \left[1 - exp\left(-\frac{R_{sec}}{2 \cdot L_{lk}} \cdot t \right) \cdot \left(\frac{sin\left(\omega_1 \cdot t\right)}{\sqrt{4 \cdot Q^2 - 1}} + cos\left(\omega_1 \cdot t\right) \right) \right] \tag{A.8}$$

$$\begin{aligned} V_{Csec}\left(I_{neg\_pk}, t\right) = & -V_c - \frac{I_{neg\_pk} \cdot C_{pri} \cdot C_{sec}}{\left(C_{pri} + C_{sec}\right)^2} \cdot R_{sec} + \frac{I_{neg\_pk}}{C_{pri} + C_{sec}} \cdot t \ \ldots \\ & + exp\left(-\frac{R_{sec}}{2 \cdot L_{lk}} \cdot t \right) \cdot \left[\frac{sin\left(\omega_1 \cdot t\right)}{\sqrt{4 \cdot Q^2 - 1}} \cdot \frac{1}{\omega_o} \cdot \left(\frac{1}{Q} - 2 \cdot Q \right) + \frac{cos\left(\omega_1 \cdot t\right)}{\omega_o \cdot Q} \right] \cdot \frac{I_{neg\_pk}}{C_{pri} + C_{sec}} \end{aligned} \tag{A.9}$$

$$V_{Cpri}(I_{neg\_pk}, t) = -V_c + \frac{I_{neg\_pk}}{C_{pri} + C_{sec}} \cdot t \ldots$$
$$+ I_{neg\_pk}\left(\frac{C_{sec}}{C_{sec} + C_{pri}}\right)^2 \cdot R_{sec}\left(1 - exp\left(-\frac{R_{sec}}{2 \cdot L_{lk}} \cdot t\right) \cdot cos(\omega_1 \cdot t) + \frac{2 \cdot Q^2 - 1}{\sqrt{4 \cdot Q^2 - 1}} \cdot exp\left(-\frac{R_{sec}}{2 \cdot L_{lk}} \cdot t\right) \cdot sin(\omega_1 \cdot t)\right)$$

(A.10)

where ω_o, ω_1 and Q are defined in Appendix A. R_{sec} is the secondary MOSFET gate resistance reflected to the primary side and is also calculated in Appendix A. As can be seen from the above expressions, I_{Llk} , V_{Csec} and V_{Cpri} are functions of time and of I_{neg_pk}, the latter being the primary current at the moment Q2 is being turned off, as shown in Figure 2.4 and in Figure 2.5. As explained above, Phase I ends when the secondary capacitance is completely discharged, and from there on, the secondary voltage is clamped to zero because both Q3 and Q4 are conducting through their anti-parallel diodes.

Therefore, the time *t1* which corresponds to the end of Phase I is obtained by making Equation (A.9) above equal to zero:

$$V_{Csec}(I_{neg\_pk}, t) = 0$$

Solving the above equation for t yields the time *t1* we are looking for. We are now in a position to calculate the current through the leakage inductance and the voltage across the primary capacitance at the end of Phase I by making $t = t1$ in (A.8) and (A.10) above, we obtain:

V_{Cpri} at end of Phase I = $V_{Cpri}(I_{neg\_pk}, t1)$

$I_{L.lk}$ at end of Phase I = $I_{L.lk}(I_{neg\_pk}, t1)$ (Called *I1* on Figure 2.5)

The above values are the initial conditions for Phase II. To simplify the subsequent analysis, it is convenient to define *V1* as the voltage variation across the primary capacitance during Phase I. From Figure 2.4, the initial value of V_{Cpri} (across C_{tfo}) equals $-V_c$. From

Figure 2.5, the final value of V_{Cpri} (at the end of Phase I) equals $-V_c + V1$. Since the final value of V_{Cpri} was calculated above, we have

$$V1 - V_C = V_{Cpri}\left(I_{neg\_pk}, t1\right) \qquad \text{or} \qquad V1 = V_{Cpri}\left(I_{neg\_pk}, t1\right) + V_C$$

As can be seen from Figure 2.5, $V1$ also represents the voltage variation across $Coss1$ and $Coss2$ during Phase I.

Having calculated all the initial conditions, we are now ready to study Phase II. Referring to Figure 2.5, Phase II ends when one of the two following conditions occurs:

1. The voltage across $Coss1$ reduces to zero in which case the Zero Voltage Transition is over.

2. The current through the leakage inductance L_{lk} reaches I_{neg_pk}; in this case, the net current flowing from the primary capacitance reduces to zero, which means that the primary capacitance cannot be discharged any further; this occurs when the value of I_{neg_pk} is insufficient to ensure a complete ZVT.

For the subsequent analysis, it is convenient to call $V2$ the total voltage variation (Phase I + Phase II) across the primary capacitance. Having called $V1$ the voltage variation across the primary capacitance during Phase I, the voltage variation during Phase II simply equals $V2 - V1$.

At the end of Phase II, the voltages across the different components of the primary capacitance are the following:

Across $Coss1$	$V_{in} + V_c - V2$
Across $Coss2$	$V2$
Across C_{tfo}	$V2 - V_c$.

Since our goal is to achieve ZVT, we look for a complete discharge of $Coss1$, hence,

$V_{in} + V_c - V2 = 0$

We called $t1$ the duration of Phase I. Likewise, let's call $t2$ the duration of Phase II. One additional constraint we have imposed on the transition is that: $t1 + t2 < 200$ ns.

Since we deal with the discharge of non-linear capacitors, the best way to analyze Phase II is by writing the energy balance at the beginning and at the end of Phase II.

Let's define the following variables:

$E1$ = total energy stored in the reactive elements at the end of Phase I (At $t = t1$)

$E2$ = total energy stored in the reactive elements at the end of Phase II (At $t = t1 + t2$)

$I1$ = current through L_{lk} at the end of Phase I.

$I2$ = current through L_{lk} at the end of Phase II.

$\Delta I = I2 - I1$

$I_{Lpri} = I_{neg\_pk} - I1$: this is the net current available at the beginning of Phase II to discharge the primary capacitance.

$E_{Coss}(V)$ = energy stored in a MOSFET output capacitance when the voltage across this output capacitance is equal to V.

From inspection of Figure 2.5, we have

$$E1 = E_{Coss}(V1) + E_{Coss}\left(V_{in} + V_c - V1\right) + \frac{1}{2}\cdot C_{tfo}\cdot\left(V1 - V_c\right)^2 + \frac{1}{2}\cdot L_{lk}\cdot I1^2 \qquad (2.4.5)$$

$$E2 = E_{Coss}(V2) + E_{Coss}\left(V_{in} + V_c - V2\right) + \frac{1}{2}\cdot C_{tfo}\cdot\left(V2 - V_c\right)^2 + \frac{1}{2}\cdot L_{lk}\cdot I2^2 \qquad (2.4.6)$$

Subtracting (2.4.5) from (2.4.6) , we obtain

$$E2 - E1 = E_{Coss}(V2) - E_{Coss}(V1) + E_{Coss}\left(V_{in} + V_c - V2\right) - E_{Coss}\left(V_{in} + V_c - V1\right) \ldots$$
$$+\frac{1}{2}\cdot C_{tfo}\cdot\left[\left(V2 - V_c\right)^2 - \left(V1 - V_c\right)^2\right] + \frac{1}{2}\cdot L_{lk}\cdot\left(I2^2 - I1^2\right) \qquad (2.4.7)$$

Applying the same principle as the one which lead to equations (2.2.2) and (2.2.3), we obtain

$$E_{Coss}(V2) - E_{Coss}(V1) = \int_{V1}^{V2} Coss(V)\cdot V\, dV$$

Therefore, (2.4.7) can be rewritten as

$$E2 - E1 = \int_{V1}^{V2} Coss(V)\cdot V\, dV + \int_{V_{in} + V_c - V1}^{V_{in} + V_c - V2} Coss(V)\cdot V\, dV \ldots$$
$$+\frac{1}{2}\cdot C_{tfo}\cdot\left[\left(V2 - V_c\right)^2 - \left(V1 - V_c\right)^2\right] + \frac{1}{2}\cdot L_{lk}\cdot\left(I2^2 - I1^2\right) \qquad (2.4.8)$$

On the other hand, this energy difference in the storage elements can only have been supplied by the sources; the sources are: V_{in}, V_c and I_{neg_pk}.

1. Energy supplied by V_{in}: $V_{in} \times \int dQ$; from Figure 2.5, the total charge coming from or going to V_{in} is the result of the discharge of $Coss1$ and is actually returned to V_{in}; therefore,

$$E_{Vin} = V_{in}\cdot\int_{V_{in} + V_c - V1}^{V_{in} + V_c - V2} Coss(V)\, dV$$

The fact that $V_{in} + V_c - V2 < V_{in} + V_c - V1$ confirms that the energy supplied by V_{in} is negative and hence is returned to V_{in}.

2. Energy supplied by V_c: $V_c \times \int dQ$; from Figure 2.5, the total charge coming from or going to V_c is the result of the charge of $Coss1$; therefore,

$$E_{Vc} = V_c \cdot \int_{V1}^{V2} Coss(V)\, dV$$

3. Energy supplied by I_{neg_pk}: it is the product of the current I_{neg_pk} and the integral of the voltage across the current source; this voltage is identical to the one appearing across the leakage inductance L_{lk}. Therefore,

$$E_{Ineg\_pk} = I_{neg\_pk} \cdot \int_{0}^{t2} V_{L.lk}(t)\, dt = I_{neg\_pk} \cdot \int_{0}^{t2} L_{lk} \cdot \frac{d}{dt} I_{L.lk}(t)\, dt =$$

$$I_{neg\_pk} \cdot \int L_{lk}\, dI_{L.lk} = I_{neg\_pk} \cdot L_{lk} \cdot (I2 - I1)$$

As stated above, $E2 - E1 = EV_{in} + EV_c + E_{Ineg\_pk}$; therefore,

$$E2 - E1 = V_{in} \cdot \int_{V_{in} + V_c - V1}^{V_{in} + V_c - V2} Coss(V)\, dV + V_c \cdot \int_{V1}^{V2} Coss(V)\, dV + I_{neg\_pk} \cdot L_{lk} \cdot (I2 - I1) \qquad (2.4.9)$$

By comparing equations (2.4.8) and (2.4.9) and after introducing the variables ΔI and I_{Lpri} defined above, we obtain

$$\frac{1}{2} \cdot L_{lk} \cdot \Delta I^2 - L_{lk} \cdot I_{Lpri} \cdot \Delta I + \frac{1}{2} \cdot C_{tfo} \cdot \left[(V2 - V_c)^2 - (V1 - V_c)^2 \right] + \int_{V1}^{V2} Coss(V) \cdot V\, dV \ldots = 0$$

$$+ \int_{V_{in} + V_c - V1}^{V_{in} + V_c - V2} Coss(V) \cdot V\, dV - V_{in} \cdot \int_{V_{in} + V_c - V1}^{V_{in} + V_c - V2} Coss(V)\, dV - V_c \cdot \int_{V1}^{V2} Coss(V)\, dV$$

(2.4.10)

The above equation which describes the energy exchange during Phase II contains two unknowns: ΔI and $V2$. Equation (2.4.10) can be rewritten as

$$\frac{1}{2}\cdot L_{lk}\cdot \Delta I^2 - L_{lk}\cdot I_{Lpri}\cdot \Delta I + X(V2) = 0 \qquad (2.4.11)$$

where $X(V2)$ contains all the terms which are independent of ΔI but are dependent of $V2$.

As mentioned above, our goal is to achieve ZVT, that is: $V2 = V_{in} + V_c$, which corresponds to condition 1 described above. However, as explained earlier, if I_{neg_pk} is insufficient to completely discharge the primary capacitance, then condition 2 will occur.

Therefore, (2.4.11) can only be resolved in two steps.

Step 1 : Make $V2 = V_{in} + V_c$ in (2.4.11) and solve for ΔI:

$$\Delta I = I_{Lpri} - \sqrt{\left(I_{Lpri}\right)^2 - 2\cdot\frac{X\left(V_{in} + V_c\right)}{L_{lk}}} \qquad (2.4.12)$$

If $\left(I_{Lpri}\right)^2 - 2\cdot\frac{X\left(V_{in} + V_c\right)}{L_{lk}} > 0$, then ΔI given by (2.4.12) is real and the problem is solved (full ZVT has been achieved).

If $\left(I_{Lpri}\right)^2 - 2\cdot\frac{X\left(V_{in} + V_c\right)}{L_{lk}} < 0$, then there is no real ΔI which will make : $V2 = V_{in} + V_c$.

Condition 2 described above occurs (incomplete ZVT) and we need to go to Step 2.

Step 2 : Make $\Delta I = I_{Lpri}$ in (2.4.11) and solve for $V2$; this will necessarily yield a value of $V2$ less than $V_{in} + V_c$.

The above calculations are outlined in detail in Appendix A.

Having found ΔI and $V2$, we can now calculate $t2$, the duration of Phase II.

The primary capacitance C_{pri} consists of the parallel combination of $Coss1$, $Coss2$ and C_{tfo}.

Hence: $Cpri(V) = Coss(V) + Coss(V_{in} + V_c - V) + C_{tfo}$.

On the other hand, $I_{Cpri} = C_{pri}(V) \cdot \frac{dV}{dt}$ therefore,

$$dt = \frac{C_{pri}(V) \cdot dV}{I_{Cpri}(V)} \tag{2.4.13}$$

From Figure 2.5, $I_{Cpri}(V) = I_{neg\_pk} - I_{L.lk}(V)$

The only way whereby we can extract an expression for $I_{Llk}(V)$ is to write the energy balance between two voltages: $V1$ and V. The energy balance has already been written between $V1$ and $V2$ in (2.4.10); all we need to do is to rewrite (2.4.10) and replace $V2$ by V.

To simplify the calculations, let's introduce two working variables:

$I_{Lpri} = I_{neg\_pk} - I1$ (already defined earlier)

$\Delta I(V) = I_{L.lk}(V) - I1$

We obtain

$$\frac{1}{2} \cdot L_{lk} \cdot \Delta I(V)^2 - L_{lk} \cdot I_{Lpri} \cdot \Delta I(V) + X(V) = 0 \tag{2.4.14}$$

where $X(V)$ represents all the terms of (2.4.10) which are independent of ΔI and where $V2$ has been replaced by V.

Solving (2.4.14) for $\Delta I(V)$ yields

$$\Delta I(V) = I_{Lpri} - \sqrt{I_{Lpri}^2 - 2 \cdot \frac{X(V)}{L_{lk}}} \tag{2.4.15}$$

Therefore, $I_{Cpri}(V) = I_{neg\_pk} - I_{L.lk}(V)$ and, from the definition of the working variables:

$$I_{Cpri}(V) = I_{Lpri} - \Delta I(V)$$

And finally, from (2.4.15),

$$I_{Cpri}(V) = \sqrt{I_{Lpri}^2 - 2 \cdot \frac{X(V)}{L_{lk}}} \tag{2.4.16}$$

Taking the expression of the time increment dt defined in (2.4.13), replacing $I_{Cpri}(V)$ by its expression given in (2.4.16) above and integrating between $V1$ and $V2$ yields

$$t2 = \int_{V1}^{V2} \frac{Coss\left(V_{in} + V_c - V\right) + Coss(V) + C_{tfo}}{\sqrt{I_{Lpri}^2 - 2 \cdot \frac{X(V)}{L_{lk}}}} \, dV \tag{2.4.17}$$

$V1$, $V2$, $t1$ and $t2$ were calculated in Appendix A for a range of values of I_{neg_pk} starting at I_o/N: the results are shown on the two graphs below.

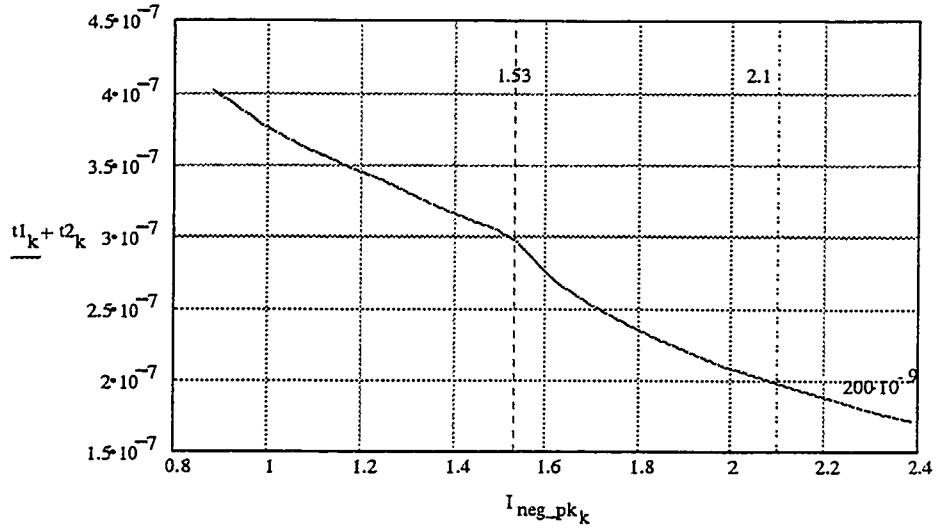


Figure 2.6 **Total transition time as a function of I_{neg_pk}**

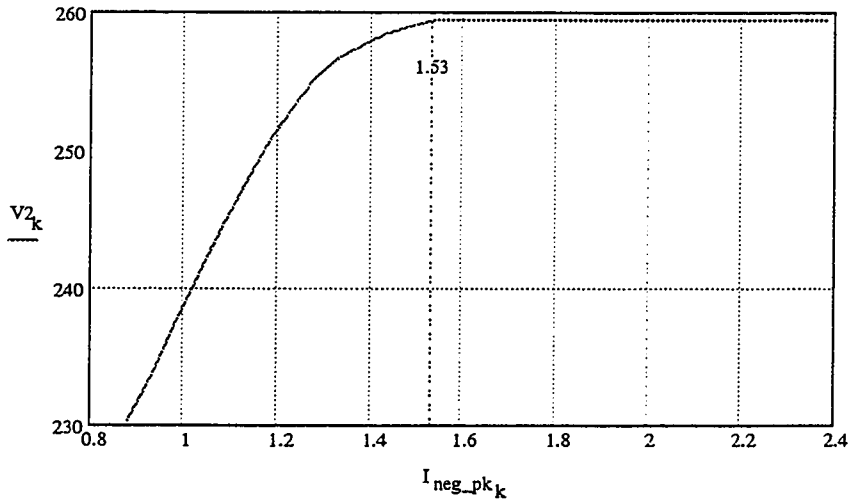


Figure 2.7 **Primary Voltage Excursion as a function of I_{neg_pk}**

As can be seen from Figure 2.7, the current I_{neg_pk} strictly required to perform ZVT equals 1.53 A. From the figure, this is the minimum current which will yield a value of $V2$ equal to $V_{in} + V_c$, i.e. 259 V. However, from Figure 2.6, this value of current would lead to a total transition time $t1 + t2$ equal to 300 ns. Since we imposed the constraint: $t1 + t2 < 200$ ns, we need a minimum I_{neg_pk} equal to 2.1 A.

We can easily calculate the primary inductance value needed to produce a value of I_{neg_pk} equal to 2.1 A:

$$L_{pri} := \frac{V_{in}}{2 \cdot I_{neg\_pk}} \cdot D \cdot Ts \qquad L_{pri} = 3.655 \cdot 10^{-5}$$

To confirm the above results, a PSPICE model of the forward converter was built, using the parameters calculated above and using the model for the MOSFETs developed in Appendix B which includes all the non-linear effects highlighted above. The circuit schematic is shown on Figure 2.8. The circuit was simulated at a switching frequency of 400 kHz, with a duty cycle of 0.618 as calculated in Appendix A and with an output current of 15 A.

The gate drive circuit has built-in delays which allow each primary MOSFET to turn on through its anti-parallel diode before applying voltage on its gate.

The primary inductance L_{pri} was set equal to 31 μH, slightly lower than the value of 36.55 μH calculated above; this reduction in inductance value was necessary because otherwise, the transition intervals (which are a significant portion of the whole period) would prevent the primary current to reach a value I_{neg_pk} equal to 2.1 A.

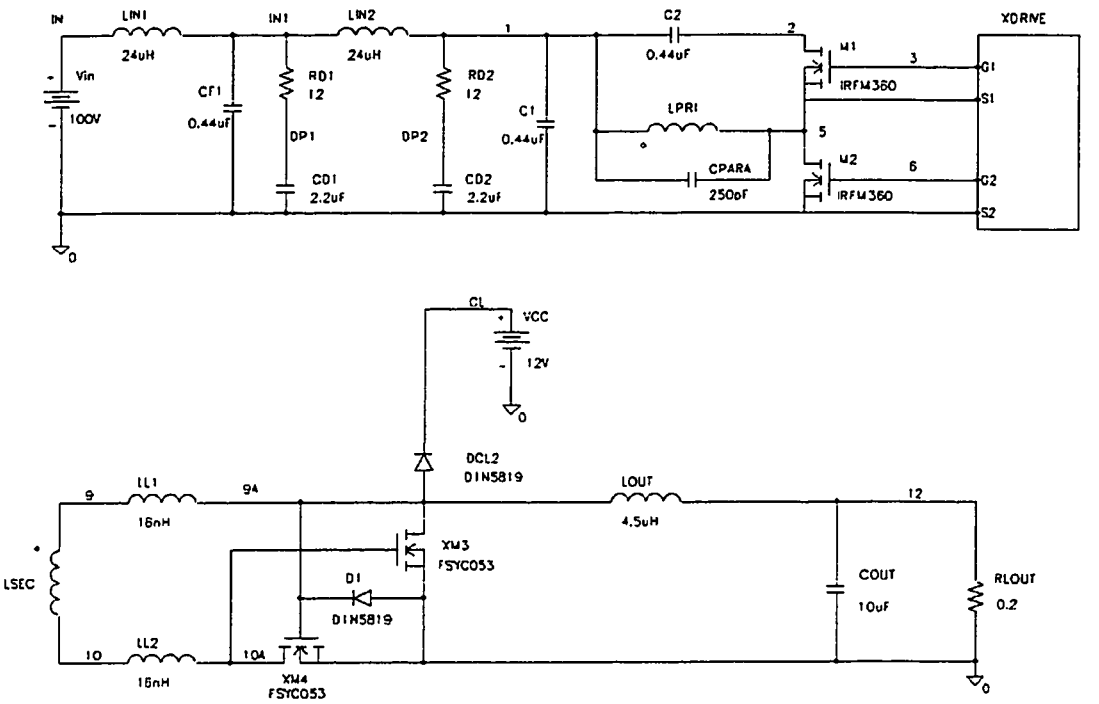


Figure 2.8 PSPICE Model of Forward Converter With Zero Voltage Switching

The results of the simulation are shown on Figure 2.9.

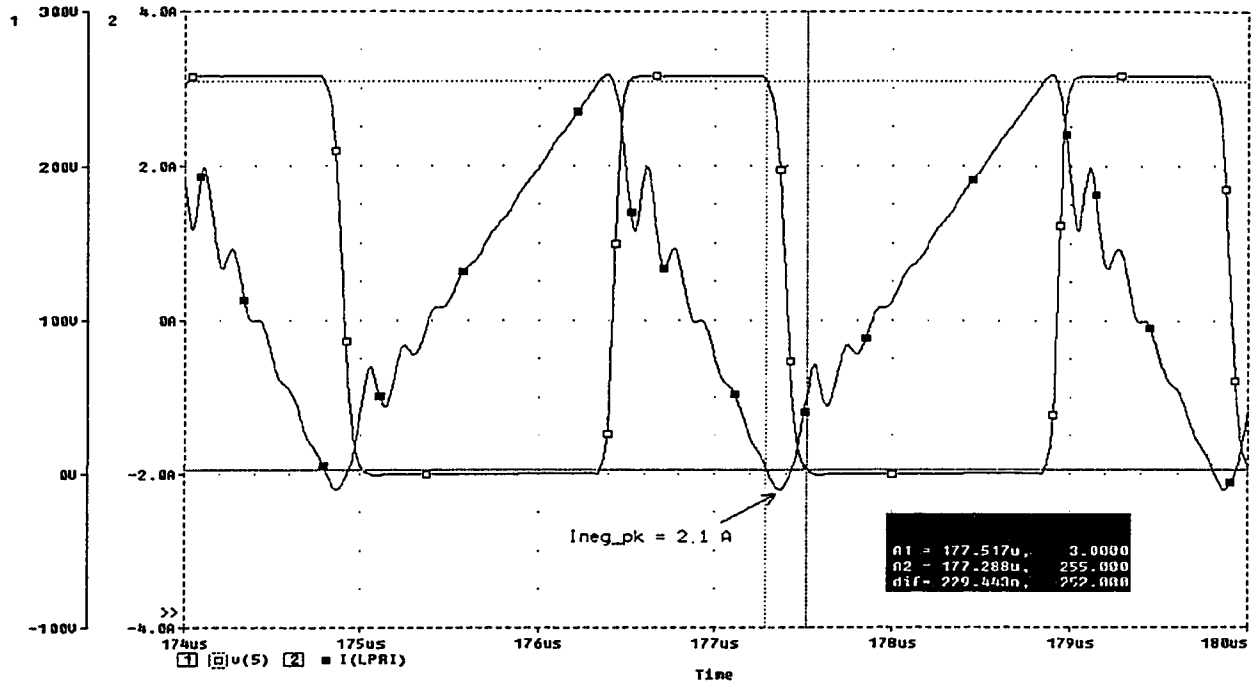


Figure 2.9 Simulation Results of Forward Converter with Zero Voltage Transition

Shown on Figure 2.9 are the waveforms of the drain voltage of M2 and the current through the transformer primary (see Figure 2.8).As can be seen from the simulation, the peak drain voltage of M2 reaches 259 V, which confirms the calculations of Appendix A. The output voltage (not shown on the graph equals 3.2 V, slightly lower than the desired 3.3 V. This is explained by the fact that the series voltage drops through the synchronous rectifiers were higher in the simulation than in the calculations, therefore yielding a lower output voltage for a given duty cycle.

The total transition time due to $I_{neg\_pk} = 2.1$ A is equal to 230 ns, slightly above the predicted 200 ns. This difference is easily explained by noticing that at the moment M1 is turned off, the primary current is not equal to 2.1 A but rather to 1.95 A; it increases to 2.1 A during the transition; this current increase is due to the transformer magnetizing inductance being too low to keep the magnetizing current constant during the transition.

This results in small differences with respect to the calculations carried out in Appendix A where we took the assumption that the magnetizing current would remain constant.

As can be seen from Figure 2.9, the duration of the positive voltage transition is significantly lower than for the negative transition: this is a direct consequence of the positive peak current being significantly higher (≈3 A) than I_{neg_pk}.

Since we have now calculated all the parameters, we are now in a position to calculate the RMS values of the transformer primary and secondary currents and therefore, the conduction losses in the ZVT forward converter. This calculation is detailed in Appendix A.

The overall conduction losses for the forward converter were found equal to 3.83 W.

2.5 The Complementary Half Bridge Converter

The simplified schematic and the primary current waveform of the Complementary half bridge converter are shown on Figure 2.10 below. The theory of operation is explained in detail in [3], [4] and [5].

As far as the Zero Voltage switching goes, the theory of operation of the Complementary Half Bridge converter is almost identical to the one of the forward converter, therefore, only the important steps of the previous paragraph will be repeated here.

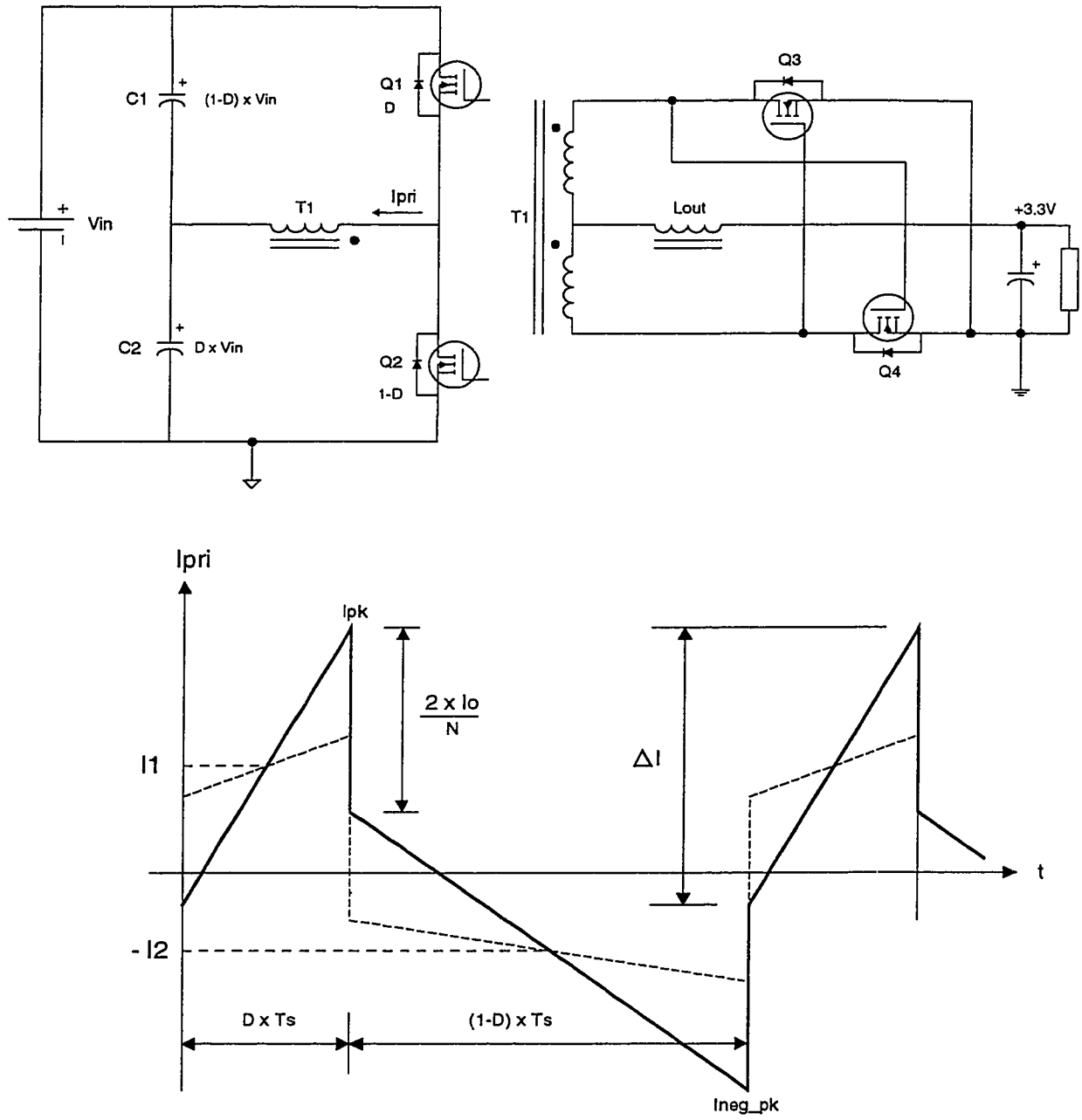


Figure 2.10 Complementary half bridge with self driven synchronous rectifiers

Referring to Figure 2.10, the voltage at the middle point of the capacitive divider consisting of C1 and C2 is easily calculated by noting that the transformer is always being driven in one direction or the other and must therefore satisfy the volts - microseconds balance. Therefore,

$$V_{C1} = D \cdot V_{in} \qquad \text{and, of course,} \qquad V_{C2} = (1 - D) \cdot V_{in}$$

If we neglect the transition times, the output voltage is easily calculated by expressing the volts - microseconds balance across the output inductor: the voltage at the front end of the output inductor is equal to $V_{in} \cdot (1 - D)/N$ during $D \cdot Ts$ and equal to $V_{in} \cdot D/N$ during the remainder of the period, i.e. $(1 - D) \cdot Ts$. Therefore, the output voltage is simply equal to the average value of the output filter front end voltage and is given by

$$V_{out} := \frac{2 \cdot D \cdot (1 - D) \cdot V_{in}}{N} \tag{2.5.1}$$

where N is the turns ratio of the primary to one half secondary.

However, as shown in [3], the transitions are not instantaneous: two overlap periods exist during which the current is being transferred from one synchronous rectifier to the other. During this overlap periods, the voltage at the front end of the output inductor equals zero, which will cause a reduction of the output voltage.

Figure 2.11 below shows the Complementary Half Bridge Converter secondary rectifier stage along with the waveforms of the voltage across the transformer secondary, the voltage at point A and the secondary current.

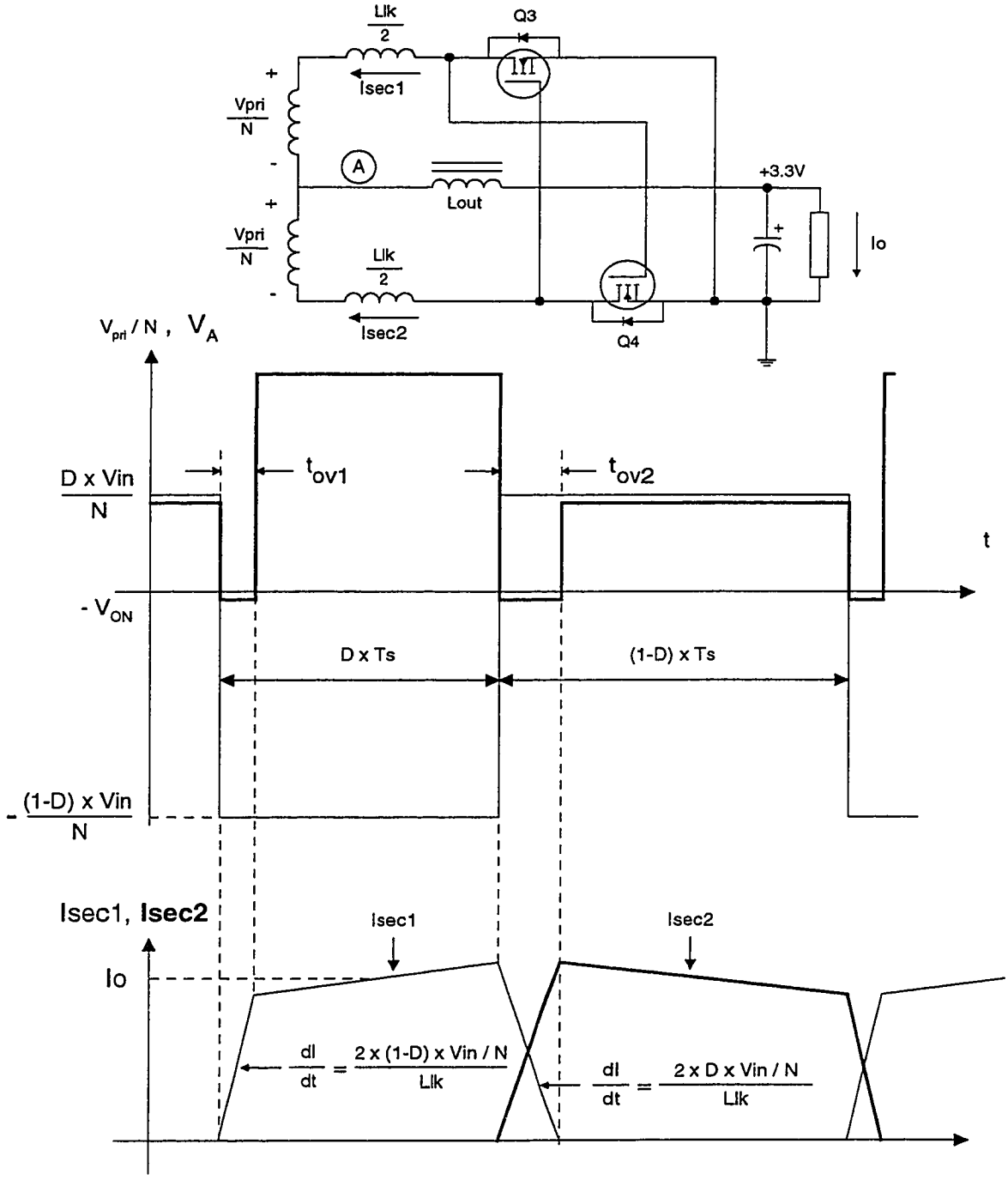


Figure 2.11 Complementary Half Bridge Converter Secondary Stage

As can be seen from Figure 2.11, when the secondary voltage changes polarity, the voltage at point A stays at zero for two periods of time t_{ov1} and t_{ov2} during which the output current is gradually transferred from Q4 to Q3 and vice-versa; during this time, both Q3 and Q4 conduct through their antiparallel diodes because V_{gs} of both Q3 and Q4 are equal to zero. Neglecting the ripple current through the output inductor and assuming the reverse recovery current of Q4's body-drain diode is negligible, the overlap times are given by

$$t_{ov1} = \frac{\frac{L_{lk} \cdot I_o}{2 \cdot (1 - D) \cdot V_{in}}}{N} \qquad (2.5.2) \qquad \text{and} \qquad t_{ov2} = \frac{\frac{L_{lk} \cdot I_o}{2 \cdot D \cdot V_{in}}}{N} \qquad (2.5.3)$$

The total overlap time, which is the sum of t_{ov1} and t_{ov2} is given by

$$t_{ov} = t_{ov1} + t_{ov2} = \frac{\frac{L_{lk} \cdot I_o}{2 \cdot D \cdot (1 - D) \cdot V_{in}}}{N} \qquad (2.5.4)$$

We have seen in paragraph 2.4 that any time overlap decreases the effective converter duty cycle which in turn causes a decrease in output voltage. If we call V_{on} the voltage drop across Q3 and Q4 when they conduct, the expression of the output voltage is given by

$$V_{out} = \frac{D \cdot V_{in}}{N} \cdot \frac{(1 - D) \cdot Ts - t_{ov2}}{Ts} + \frac{(1 - D) \cdot V_{in}}{N} \cdot \frac{D \cdot Ts - t_{ov1}}{Ts} - V_{on}$$

After replacing t_{ov1} and t_{ov2} by their expressions given by (2.5.2) and (2.5.3), we obtain

$$V_{out} = \frac{2 \cdot D \cdot (1 - D) \cdot V_{in}}{N} - \frac{L_{lk} \cdot I_o}{Ts} - V_{on}$$

$$\text{or :} \quad V_{out} = \frac{2 \cdot D \cdot (1 - D) \cdot V_{in}}{N} - L_{lk} \cdot I_o \cdot Fs - V_{on} \qquad (2.5.5)$$

where $Fs = \frac{1}{Ts}$ is the switching frequency.

Expression (2.5.5) is very similar to the one we had found in paragraph 2.4 in that the effect of the secondary leakage inductance is identical in both cases. It should be noted that making L_{lk} and V_{on} equal to zero in (2.5.5) leads back to (2.5.1).

If V_{in} and I_o are held constant, the right hand side of (2.5.5) reaches its maximum for $D = 0.5$. This means that the control region for this converter goes from $D = 0$ to $D = 0.5$ and thus the maximum allowed duty cycle is 50 %. The maximum voltage occurs when the input voltage is at its minimum, i.e. $V_{in} = Vin_{min} = 90$ V.

Therefore, from (2.5.5), we can readily calculate the transformer turns ratio:

$$D_{max} := 0.5 \qquad L_{lk} := 33 \cdot 10^{-9}$$

$$N := \frac{2 \cdot D_{max} \cdot (1 - D_{max}) \cdot Vin_{min}}{V_{out} + V_{on} + \frac{L_{lk} \cdot I_o}{Ts}} \qquad N = 12.38$$

We choose $N = 12$.

Using (2.5.5) again, the nominal duty cycle D for $V_{in} = 100$ V was calculated in Appendix A; the calculation yields $D = 0.321$.

We now proceed to calculate the maximum magnetizing inductance which will guarantee ZVT in less than 200 ns. Again, we will consider the worst case (slowest) commutation, which is the one corresponding to the smallest value of primary current, i.e. I_{neg_pk} on Figure 2.10.

As for the forward converter, the Complementary Half bridge commutation takes place in two phases; Figure 2.12 and Figure 2.13 show the equivalent schematics of the Complementary Half Bridge converter during Phase I and Phase II respectively. Also

represented on both figures are the voltages and the currents at the beginning of the corresponding phase.

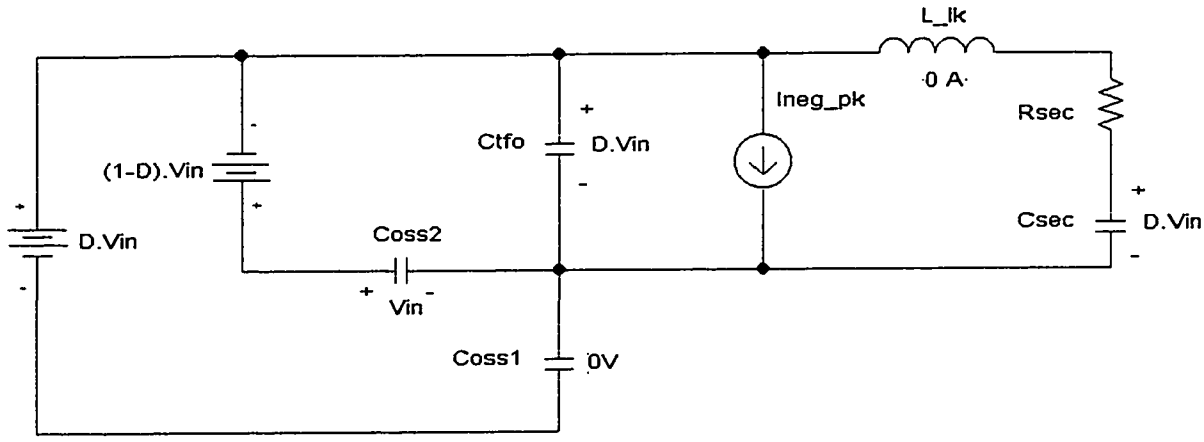


Figure 2.12 Complementary Half Bridge Converter Equivalent Circuit During Phase I

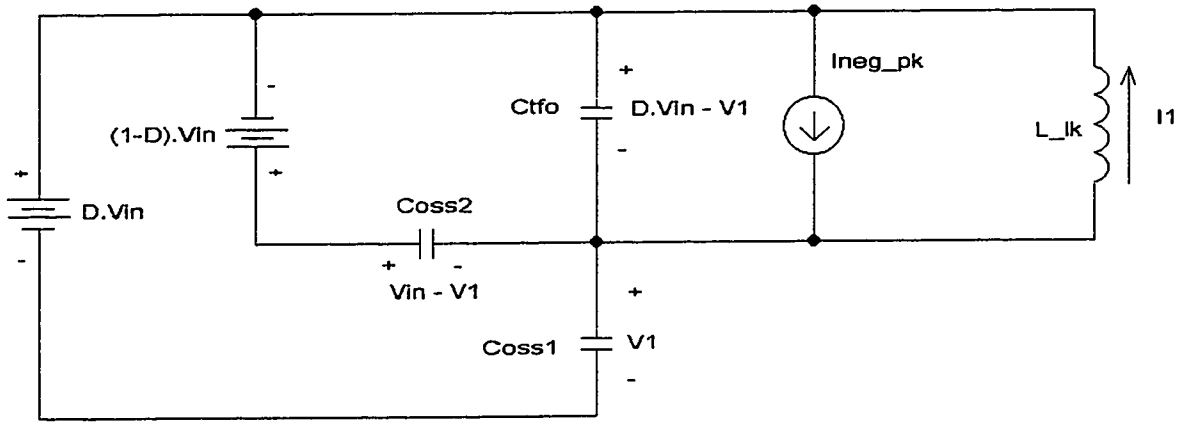


Figure 2.13 Complementary Half Bridge Converter Equivalent Circuit During Phase II.

Referring to Figure 2.12, voltage sources $D \cdot V_{in}$ and $(1-D) \cdot V_{in}$ represent the voltages across capacitors C2 and C1 of Figure 2.10 respectively. Since the transition will last less than 200 ns, we can safely neglect the voltage variation across these capacitors

during the transition and therefore these capacitors can be replaced by constant voltage sources. If we compare Figure 2.12 and Figure 2.13 with Figure 2.4 and Figure 2.5 respectively, we see that they can be made identical by performing the following substitutions:

1. Voltage source V_{in} of Figure 2.4 must be replaced by $D \cdot V_{in}$.
2. Voltage source V_c of Figure 2.4 must be replaced by $(1-D) \cdot V_{in}$.
3. Initial voltage V_c across the primary and secondary capacitance must be replaced by $D \cdot V_{in}$.

Therefore, the analysis which was carried out for the forward converter can be repeated for the complementary half bridge converter simply by making the above substitutions in the equations.

The detailed calculations are performed in Appendix A, where we defined the same working variables as for the forward converter. The MOSFET parameters used were those of 200 V MOSFETs as opposed to 400 V MOSFETs for the forward converter. The 200 V MOSFETs characterisation has been carried out in Appendix B.

V1, *V2*, *t1* and *t2* were calculated for a range of values of I_{neg_pk}; the results are shown on the two graphs below.

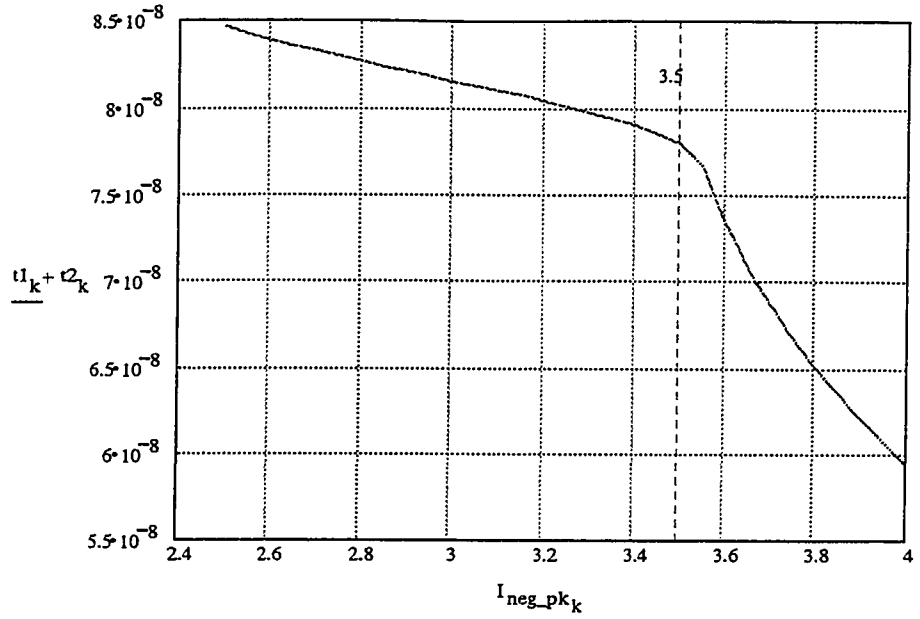


Figure 2.14 Total transition time as a function of I_{neg_pk}

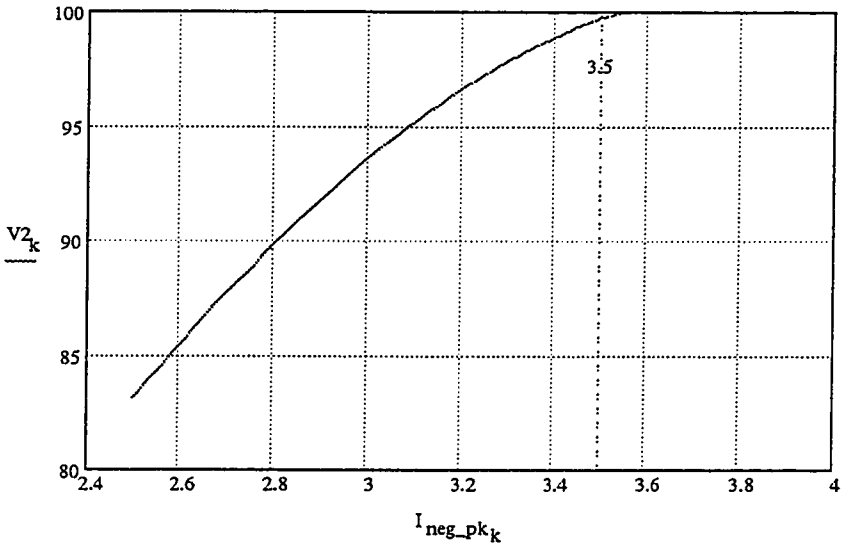


Figure 2.15 Primary Voltage Excursion as a function of I_{neg_pk}

As can be seen from Figure 2.15, the current I_{neg_pk} required to perform ZVT equals 3.5 A. From the figure, this is the minimum current which will yield a value of $V2$ equal to

V_{in}, i.e. 100 V. From Figure 2.14, this value of current will lead to a total transition time $t1 + t2$ equal to 78 ns.

As can be seen, the transition time for a full ZVT is much shorter for the complementary half bridge converter than for the forward converter. This difference can be explained by two factors.

1. The total voltage excursion equals 100 V as opposed to 259 V in the forward converter.
2. The MOSFETs used are 200 V size 5 devices (IRFM250) which have less parasitic capacitance than the 400 V size 6 devices (IRFM360) used in the forward converter.

We can now proceed to calculate the primary inductance value needed to produce a value of I_{neg_pk} equal to 3.5 A.

With reference to the waveforms shown on Figure 2.10, $I1$ and $I2$ represent the average values of the primary current during the conduction period of Q1 and Q2 respectively. $I1$ and $I2$ could also represent the actual values of the primary current if the transformer magnetizing inductance and the output inductance were infinite.

Since the transformer primary is connected to the common connection of capacitors C1 and C2, its average value over the whole period must be zero.

Therefore, $I1 \cdot D = I2 \cdot (1 - D)$.

On the other hand, when Q1 turns off and Q2 turns on, the primary current undergoes a variation equal to twice the load current divided by the turns ratio.

Therefore, $I1 + I2 = \frac{2 \cdot I_O}{N}$.

The above two equations enable us to calculate $I1$ and $I2$.

$$I1 = \frac{2 \cdot (1 - D) \cdot I_o}{N} \qquad \text{and} \qquad I2 = \frac{2 \cdot D \cdot I_o}{N}$$

Referring to Figure 2.10 again and calling ΔI the peak to peak value of the primary magnetizing current, we obtain

$$I_{pk} = I1 + \frac{\Delta I}{2} \qquad \text{or} \qquad I_{pk} = \frac{2 \cdot (1 - D) \cdot I_o}{N} + \frac{\Delta I}{2} \tag{2.5.6}$$

$$I_{neg\_pk} = I2 + \frac{\Delta I}{2} \qquad \text{or} \qquad I_{neg\_pk} = \frac{2 \cdot D \cdot I_o}{N} + \frac{\Delta I}{2} \tag{2.5.7}$$

Using the values of $D = 0.321$ and $I_{neg\_pk} = 3.5$ A which were calculated above , we can easily calculate ΔI from (2.5.7)

$$\Delta I = 2 \cdot I_{neg\_pk} - \frac{4 \cdot D \cdot I_o}{N} \qquad \text{or} \qquad \Delta I = 5.41$$

We can now calculate the transformer magnetizing inductance required to yield $\Delta I = 5.41$. Referring to Figure 2.10, when Q1 conducts, the voltage $(1 - D) \cdot V_{in}$ is applied to the transformer during $D \cdot Ts$ seconds.

$$\text{Therefore, } \Delta I = \frac{D \cdot (1 - D) \cdot Ts \cdot V_{in}}{L_{pri}} \qquad \text{or} \qquad L_{pri} = \frac{D \cdot (1 - D) \cdot Ts \cdot V_{in}}{\Delta I}$$

This yields a value of L_{pri} equal to 10 μH.

To confirm the above results, a PSPICE model of the complementary half bridge converter was built, using the parameters calculated above and using the model for the MOSFETs developed in Appendix B which includes all the non-linear effects highlighted above. The circuit schematic is shown on Figure 2.16 below. The circuit was simulated at a

switching frequency of 400 kHz, with a duty cycle of 0.321 as calculated in Appendix A and with an output current of 15 A.

The gate drive circuit has built-in delays which provide enough time for ZVT to occur: ideally, the built-in delays should be just sufficient for each primary MOSFET to turn on through its anti-parallel diode before voltage is applied on its gate.

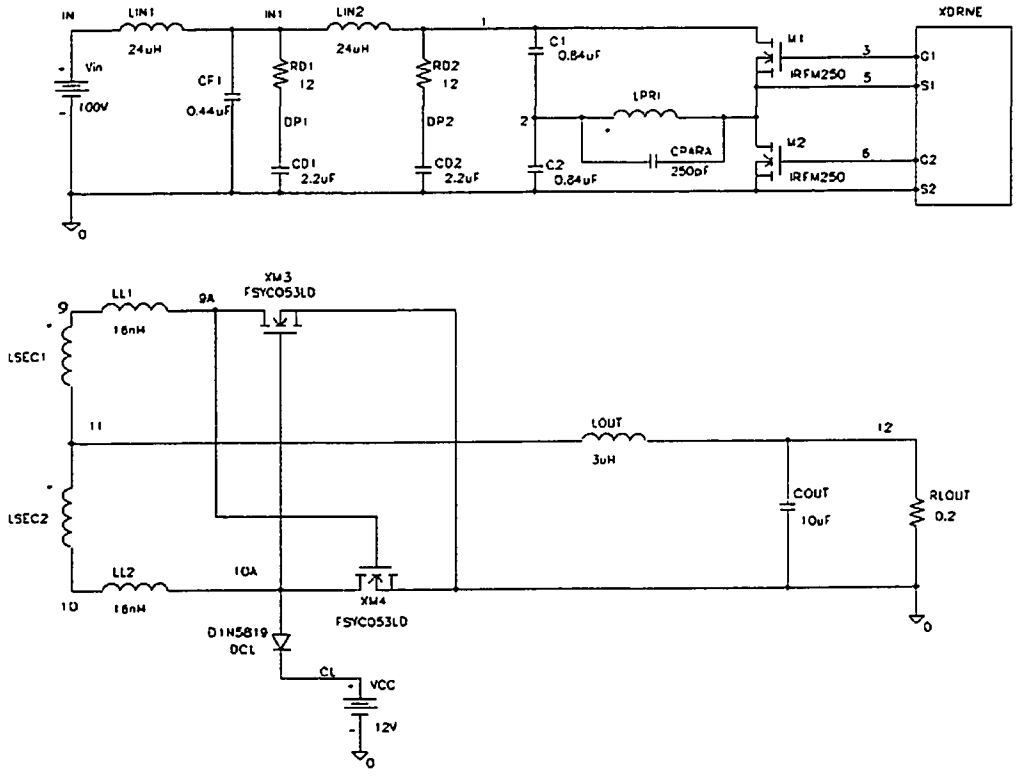


Figure 2.16 PSPICE Model of the Complementary Half Bridge Converter

The results of the simulation are shown on Figure 2.17 below.

Shown on Figure 2.17 are the waveforms of the drain voltage of M2 and the current through the transformer primary (see Figure 2.16 above). As can be seen from the simulation, a primary current I_{neg_pk} value of 3.5 A is just sufficient to bring the peak drain voltage of M2 up to 100 V, which confirms the above calculations.

It should be noted that the natural commutation causes the drain voltage of M2 to reach its peak value of 100 V exactly at the instant the primary current changes sign, as expected.

After the maximum voltage of 100 V is reached, the drain voltage of M2 rolls back down to about 70V until a sharp rising edge brings it back to 100 V. This simply indicates that the gate drive built-in delays were made too high and thus allow a resonant discharge of the primary parasitic capacitances to be initiated before the upper MOSFET M1 is actually turned ON; this excessive delay causes MOSFET M1 to experience a "hard" turn-on over a voltage range of about 30 V (second rising edge on Figure 2.17).

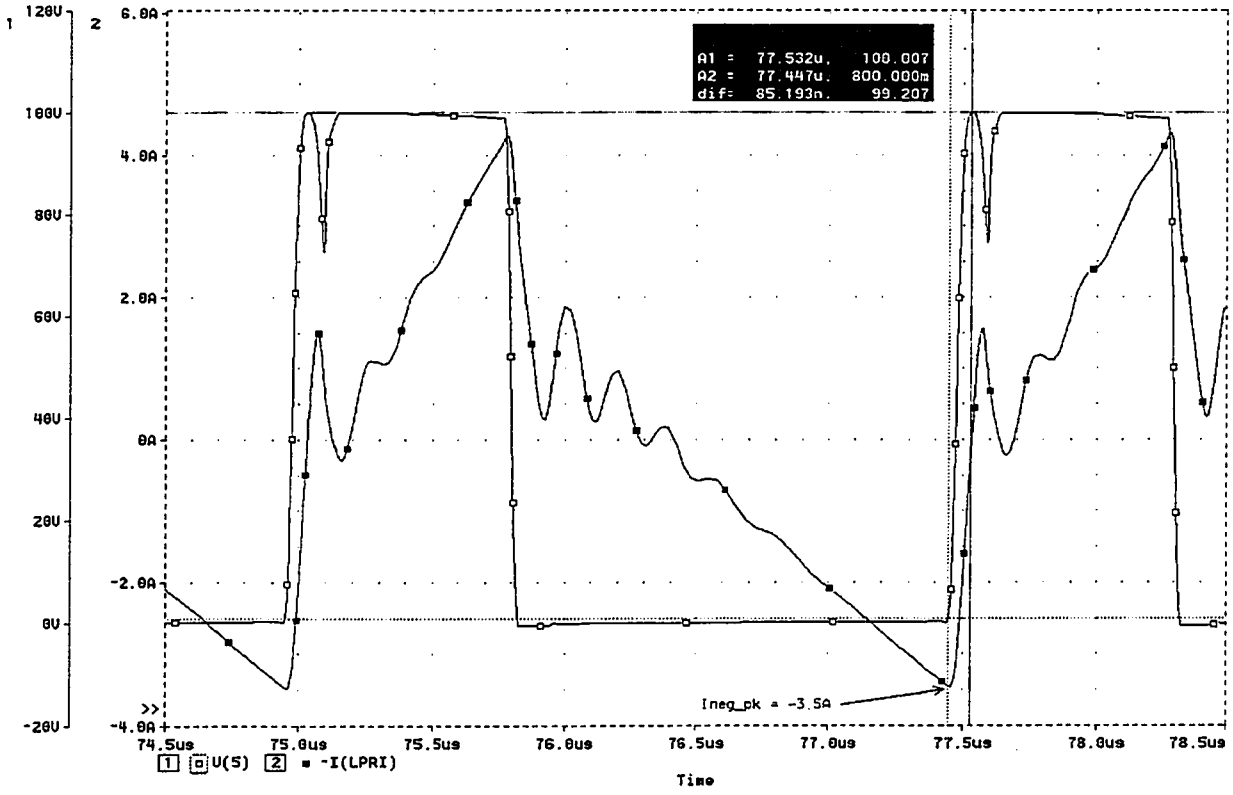


Figure 2.17 Simulation Results of Complementary HB Converter with ZVT

The duration of the voltage transition is 85 ns, slightly higher than the predicted 78 ns. The output voltage (not shown) equals 3.34 V for a duty cycle $D = 0.321$.

As can be seen from Figure 2.17, the duration of the negative ZVT is lower than for the positive ZVT: this is the direct consequence of the positive peak current I_{pk} being higher than I_{neg_pk}.

From Figure 2.17, the value of I_{pk} equals 4.3 A, very close to the value calculated in Appendix A.

Since we have now calculated all the parameters, we are now in a position to calculate the RMS values of the transformer primary and secondary currents and therefore, the conduction losses in the ZVT complementary half bridge converter. This calculation is detailed in Appendix A.

The overall conduction losses for the complementary half bridge converter were found equal to 4.1 W.

2.6 The ZVT Flyback Converter

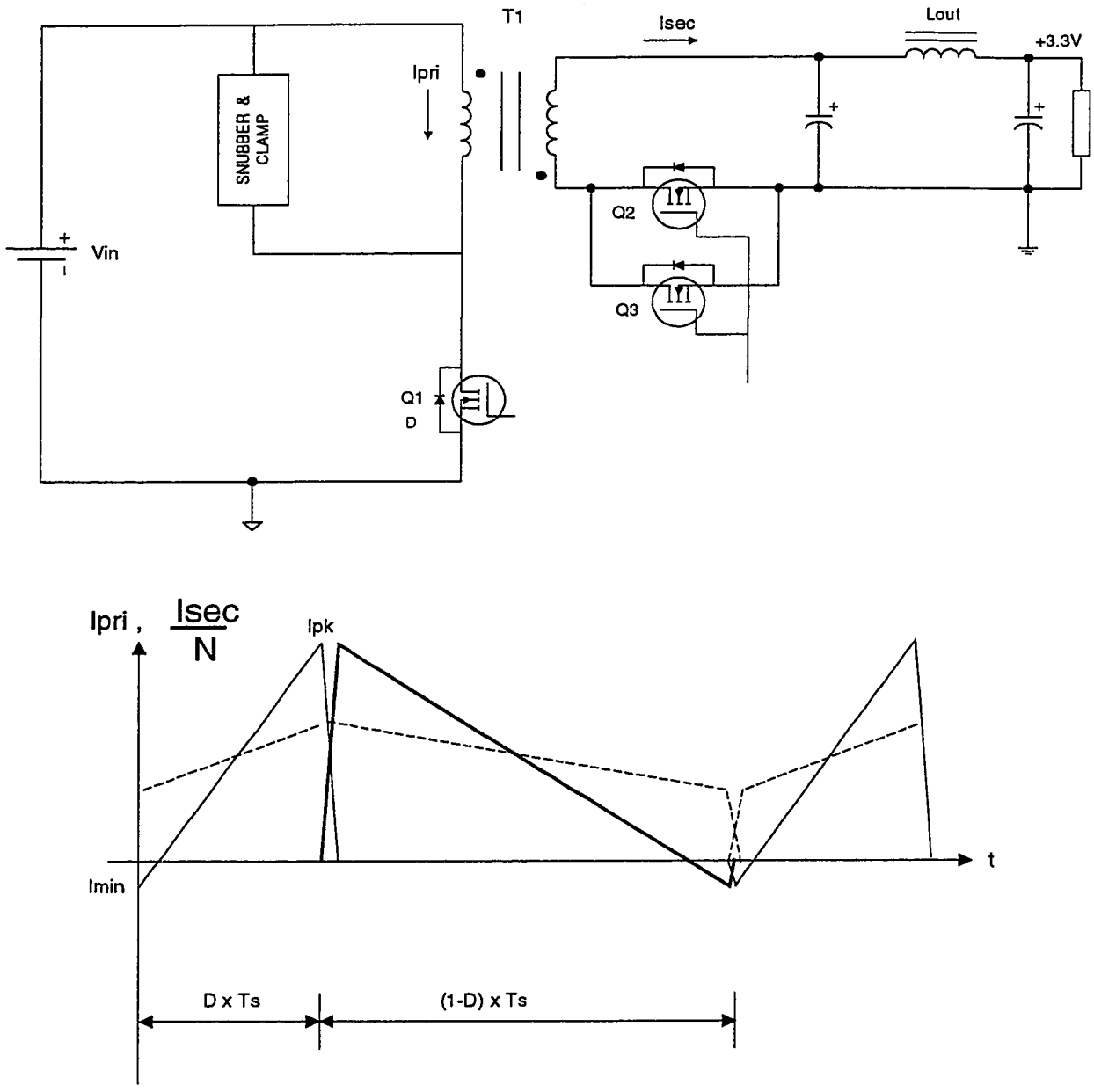


Figure 2.18 **Flyback converter with ZVT for both primary side and secondary side transistors**

Figure 2.18 below shows the simplified schematic of the ZVT Flyback Converter along with the waveforms of the primary and secondary currents. The dotted lines represent the primary and secondary current waveforms of a conventional Flyback converter.

As seen from the simplified diagrams, the slopes of the primary and secondary currents are much steeper for a ZVT Flyback than for a conventional Flyback.

The theory of operation is almost identical to that of a conventional Flyback converter with some modifications highlighted below.

It should be noted that if secondary synchronous rectifiers are used in a conventional Flyback converter, their turn-on occurs under zero voltage because when the primary MOSFET is turned off, the energy is being transferred to the secondary winding and hence to the output capacitor through the anti-parallel diodes of Q2 and Q3 (see Figure 2.18); therefore, Q2 and Q3 can be subsequently turned on their gates without incurring turn-on losses. However, in a conventional Flyback, the primary MOSFET Q1 experiences a "hard" turn-on.

As discussed earlier, the ZVT Flyback converter is characterised by a transformer magnetizing inductance much smaller than that of a conventional Flyback converter; as a result, the magnetizing current variation over one switching period is considerably larger. Referring to Figure 2.18, this large magnetizing current variation causes the secondary current (I_{sec} in Figure 2.18) to become negative. With respect to synchronous rectifier MOSFETs Q2 and Q3, this negative secondary current is a forward transistor current which can be interrupted simply by turning off Q2 and Q3.

Once Q2 and Q3 are turned off, the transformer magnetizing current charges the output capacitances of Q2 and Q3 and discharges the output capacitance of Q1 and the transformer winding capacitance. If enough magnetizing energy is stored in the transformer

inductance at the moment Q2 and Q3 are turned off, ZVT is achieved for the primary MOSFET Q1.

The purpose of this paragraph is to calculate the minimum value of the peak negative secondary current I_{neg_pk} in order to guarantee ZVT for the primary MOSFET Q1.

Before we attempt to do so, we must first calculate some key parameters of the converter such as the steady state duty cycle D and the transformer turns ratio.

We note that the average value of the secondary current must be equal to the output current I_o. Hence,

$$\frac{I_{pk} - I_{neg\_pk}}{2} \cdot (1 - D) = I_o \qquad (2.6.1)$$

The above expression suggests that we must look for a duty cycle as short as possible because the energy is transferred to the secondary during (1–D); hence, in order to minimize the RMS value of the secondary current, it is desirable to "spread" the secondary current over the longest possible period of time.

Choose $D = 0.25$

The balance of volts-microseconds across the transformer requires:

$$D \cdot V_{in} = (1 - D) \cdot N \cdot \left(V_{out} + V_{on}\right)$$

V_{on} represents the voltage drop across the secondary synchronous rectifiers and is taken equal to 0.2 V. V_{out} is equal to 3.3 V.

Therefore, $$N := \frac{D \cdot V_{in}}{(1 - D) \cdot \left(V_{out} + V_{on}\right)} \text{ or } \qquad N = 9.524$$

Take $N = 10$; we then need to recalculate the duty cycle according to the new value of N.

$$D := \frac{N \cdot (V_{out} + V_{on})}{N \cdot (V_{out} + V_{on}) + V_{in}} \qquad \text{or} \qquad D = 0.259$$

The maximum drain to source voltage of the primary MOSFET Q1 equals

$$VDS_{max} := Vin_{max} + N \cdot (V_{out} + V_{on}) \qquad VDS_{max} = 145 \cdot V$$

This value of VDS_{max} allows the use of an IRFM250 (200V) MOSFET for Q1.

The next step we need to carry out is the calculation of the minimum value of I_{neg_pk} which will guarantee ZVT for Q1 in less than 200 ns.

Figure 2.19 below is the equivalent schematic of the ZVT Flyback during the soft transition which immediately follows the turn-off of secondary MOSFETs Q2 and Q3.

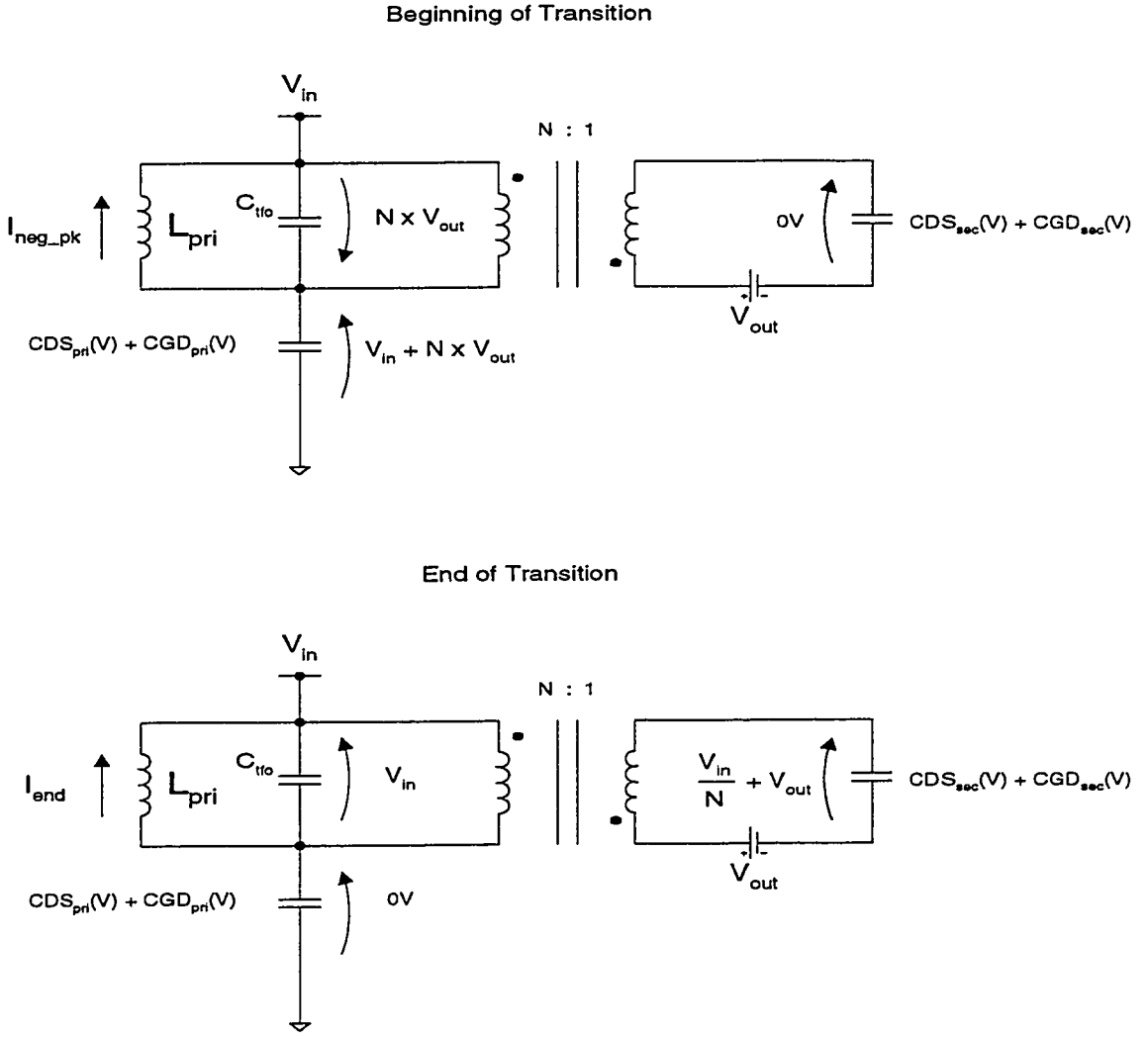


Figure 2.19 ZVT Flyback Equivalent schematic during the soft transition

Represented on Figure 2.19 are the voltages and currents at the beginning and at the end of the transition, assuming that the converter achieves full ZVT.

Capacitances $C_{pri}(V)$ and $C_{sec}(V)$ represent the non-linear output capacitances of the primary and secondary MOSFETs respectively. The expressions of $C_{pri}(V)$ and $C_{sec}(V)$ are given by

$$C_{pri}(V) = \frac{Cgdo_{pri}}{\left(A_{pri} + V\right)^{\gamma_{pri}}} + \frac{Cdso_{pri}}{\sqrt{1 + \frac{V}{0.8}}} \tag{2.6.2}$$

$$C_{sec}(V) = 2 \cdot \left[\frac{Cgdo_{sec}}{\left(A_{sec} + V\right)^{\gamma_{sec}}} + \frac{Cdso_{sec}}{\sqrt{1 + \frac{V}{0.8}}} \right] \tag{2.6.3}$$

Expressions (2.6.2) and (2.6.3) are very similar to (2.2.1). Each of them contains two terms which correspond to the drain to gate capacitance and the drain to source capacitance respectively. Parameters $Cgdo_{pri}$, $Cdso_{pri}$, A_{pri} and γ_{pri} are those of an IRFM250 MOSFET and are calculated in Appendix B. Parameters $Cgdo_{sec}$, $Cdso_{sec}$, A_{sec} and γ_{sec} are those of an FSYC053LD MOSFET and are also calculated in Appendix B. The multiplying factor of 2 in (2.6.3) accounts for the fact that we have two secondary MOSFETs in parallel.

We will analyse the soft transition the same way as we did for the ZVT Forward Converter and for the ZVT Complementary Half Bridge by writing the energy balance at the beginning and at the end of the soft transition.

Let's define the following variables:

$E1$ = total energy stored in the reactive elements at the beginning of the transition

$E2$ = total energy stored in the reactive elements at the end of the transition

L_{sec} = transformer magnetizing inductance as seen from the secondary winding ($= L_{pri} / N^2$)

I_{neg_pk} = current through the transformer at the beginning of the transition (reflected to the secondary of the transformer).

I_{end} = current through the transformer at the end of the transition (reflected to the secondary of the transformer).

$EC_{pri}(V)$ = Energy stored in the primary MOSFET output capacitance when the voltage across this capacitance is equal to V.

$EC_{sec}(V)$ = Energy stored in the secondary MOSFET output capacitance when the voltage across this capacitance is equal to V.

Δt = duration of the transition

From inspection of Figure 2.19 and after replacing L_{pri} by N^2 x L_{sec}, we have

$$E1 = \frac{1}{2}\cdot L_{sec}\cdot I_{neg\_pk}^{2} + EC_{pri}\left(V_{in} + N\cdot V_{out}\right) + \frac{1}{2}\cdot C_{tfo}\cdot\left(N\cdot V_{out}\right)^{2} \qquad (2.6.4)$$

$$E2 = \frac{1}{2}\cdot L_{sec}\cdot I_{end}^{2} + EC_{sec}\left(\frac{V_{in}}{N} + V_{out}\right) + \frac{1}{2}\cdot C_{tfo}\cdot\left(V_{in}\right)^{2} \qquad (2.6.5)$$

In the above expressions, $EC_{pri}\left(V_{in} + N\cdot V_{out}\right)$ and $EC_{sec}\left(\frac{V_{in}}{N} + V_{out}\right)$ are given by

$$EC_{pri}\left(V_{in} + N\cdot V_{out}\right) = \int_{0}^{V_{in} + N\cdot V_{out}} C_{pri}(V)\cdot V\, dV$$

$$EC_{sec}\left(\frac{V_{in}}{N} + V_{out}\right) = \int_{0}^{\frac{V_{in}}{N} + V_{out}} C_{sec}(V)\cdot V\, dV$$

where $C_{pri}(V)$ and $C_{sec}(V)$ are given by (2.6.2) and (2.6.3).

The energy difference $E2$ - $E1$ can only have been supplied by the sources represented by V_{in} and V_{out}.

1. Energy supplied by V_{in}: $V_{in} \times \int dQ$; from Figure 2.19, the total charge coming from or going to V_{in} is the result of the discharge of $C_{pri}(V)$ and is actually returned to V_{in}. Therefore,

$$E_{Vin} = -V_{in} \cdot \int_0^{V_{in} + N \cdot V_{out}} C_{pri}(V)\, dV$$

2. Energy supplied by V_{out}: $V_{out} \times \int dQ$; from Figure 2.19, the total charge coming from or going to V_{out} is the result of the charge of $C_{sec}(V)$. Therefore,

$$E_{Vout} = V_{out} \cdot \int_0^{\frac{V_{in}}{N} + V_{out}} C_{sec}(V)\, dV$$

As stated above, $E2 - E1 = E_{Vin} + E_{Vout}$; on the other hand, $E2 - E1$ can also be obtained by subtracting (2.6.4) from (2.6.5); by identifying the two expressions of $E2 - E1$ and after simplifications, we obtain

$$\frac{1}{2} \cdot L_{sec} \cdot \left(I_{end}^2 - I_{neg\_pk}^2 \right) = \Delta E \qquad (2.6.6)$$

where :

$$\Delta E = V_{out} \cdot \int_0^{V_{out} + \frac{V_{in}}{N}} C_{sec}(V)\, dV - V_{in} \cdot \int_0^{V_{in} + N \cdot V_{out}} C_{pri}(V)\, dV - \int_0^{V_{out} + \frac{V_{in}}{N}} C_{sec}(V) \cdot V\, dV \ldots$$
$$+ \int_0^{V_{in} + N \cdot V_{out}} C_{pri}(V) \cdot V\, dV - \frac{1}{2} \cdot C_{tfo} \cdot V_{in}^2 + \frac{1}{2} \cdot C_{tfo} \cdot \left(N \cdot V_{out} \right)^2$$

(2.6.7)

The right hand side of (2.6.6) represents the capacitive energy variation required to achieve a full ZVT. If we make $I_{end} = 0$, then (2.6.6) reduces to

$$\frac{1}{2}\cdot L_{sec}\cdot I_{neg\_pk}^{2} = \Delta E \qquad (2.6.8)$$

which corresponds to the situation where the magnetic energy stored in the transformer exactly equals the capacitive energy variation required to achieve ZVT. This of course corresponds to the minimum value of I_{neg_pk}.

There are three unknowns in (2.6.6): L_{sec} , I_{neg_pk} and I_{end}. Equation (2.6.1) provides a second equation but also introduces a fourth unknown I_{pk}.

A third equation can be written by expressing the magnetizing inductance L_{sec} as a function of the total secondary current variation.

We have : $$V_{out} + V_{on} = L_{sec}\cdot\frac{dI}{dt}$$

Therefore,

$$L_{sec} = \frac{(V_{out} + V_{on})\cdot(1 - D)\cdot Ts}{I_{pk} + I_{neg\_pk}} \qquad (2.6.9)$$

Another important parameter is the duration of the transition Δt.

We have imposed the constraint $\Delta t \leq 200$ ns. We therefore need an expression for Δt.

The total voltage variation reflected to the secondary side equals $\frac{V_{in}}{N} + V_{out}$.

At any intermediate voltage V such that

$$0 < V < \frac{V_{in}}{N} + V_{out}$$

the voltage across the secondary MOSFET capacitance C_{sec} is equal to V whereas the voltage across the primary MOSFET capacitance C_{pri} is equal to

$V_{in} + N \cdot V_{out} - N \cdot V$. Therefore, the total parasitic capacitance reflected to the secondary side equals

$$C_{sec}(V) + N^2 \cdot C_{pri}\left(V_{in} + N \cdot V_{out} - N \cdot V\right) + N^2 \cdot C_{tfo}$$

If we call $I(V)$ the current through the transformer inductance at voltage V, we have

$$I(V) = \left(C_{sec}(V) + N^2 \cdot C_{pri}\left(V_{in} + N \cdot V_{out} - N \cdot V\right) + N^2 \cdot C_{tfo}\right) \cdot \frac{dV}{dt}$$

Therefore,

$$dt = \frac{\left(C_{sec}(V) + N^2 \cdot C_{pri}\left(V_{in} + N \cdot V_{out} - N \cdot V\right) + N^2 \cdot C_{tfo}\right) \cdot dV}{I(V)} \qquad (2.6.10)$$

The total transition time is then obtained by integrating (2.6.10) from 0 to $\frac{V_{in}}{N} + V_{out}$

However, we need an analytical expression for $I(V)$. This expression can be obtained by re-writing the energy balance equations (2.6.6) and (2.6.7) between 0 and V, where

$$0 < V < \frac{V_{in}}{N} + V_{out}$$

We obtain

$$\frac{1}{2} \cdot L_{sec} \cdot \left(I(V)^2 - I_{neg\_pk}^2\right) = \Delta E(V)$$

Therefore,

$$I(V) = \sqrt{2 \cdot \frac{\Delta E(V)}{L_{sec}} + I_{neg\_pk}^2} \qquad (2.6.11)$$

where

$$\Delta E(V) = V_{out}\cdot\int_0^{V} C_{sec}(x)\,dx - V_{in}\cdot\int_{V_{in}+N\cdot V_{out}-N\cdot V}^{V_{in}+N\cdot V_{out}} C_{pri}(x)\,dx - \int_0^{V} C_{sec}(x)\cdot x\,dx \ldots$$
$$+\int_{V_{in}+N\cdot V_{out}-N\cdot V}^{V_{in}+N\cdot V_{out}} C_{pri}(x)\cdot x\,dx - \frac{1}{2}\cdot C_{tfo}\cdot\left(N\cdot V - N\cdot V_{out}\right)^2 + \frac{1}{2}\cdot C_{tfo}\cdot\left(N\cdot V_{out}\right)^2 \qquad (2.6.12)$$

And finally, after integrating (2.6.10),

$$t_{tr} = \int_0^{\frac{V_{in}}{N}+V_{out}} \frac{C_{sec}(V) + N^2\cdot C_{pri}\left(V_{in}+N\cdot V_{out}-N\cdot V\right) + N^2\cdot C_{tfo}}{\sqrt{2\cdot\frac{\Delta E(V)}{L_{sec}} + I_{neg\_pk}^{\,2}}}\,dV \qquad (2.6.13)$$

The system of equations consisting of (2.6.1). (2.6.6), (2.6.9) and (2.6.13) was iteratively solved in Appendix A for a switching frequency of 400 kHz (Ts = 2.5 µs). The results were the following:

I_{pk} = 52.4 A

I_{neg_pk} = 11.9 A

I_{end} = 1.7 A

L_{sec} = 101 nH

Δt = 197 ns.

To confirm the above results, a PSPICE model of the ZVT Flyback converter was built, using the parameters calculated above and using the MOSFET models developed in Appendix B. The circuit schematic is shown on Figure 2.20 below. The circuit was simulated at a switching frequency of 400 kHz, with a duty cycle of 0.259 as calculated

above and with an output current of 15 A. The primary and secondary gate drive signals had built-in delays to allow each MOSFET to turn on through its anti-parallel diode before applying voltage on its gate. In order to obtain a current I_{neg_pk} equal to 11 9 A, the transformer secondary inductance had to be reduced to 91 nH, down from the calculated value of 101 nH.

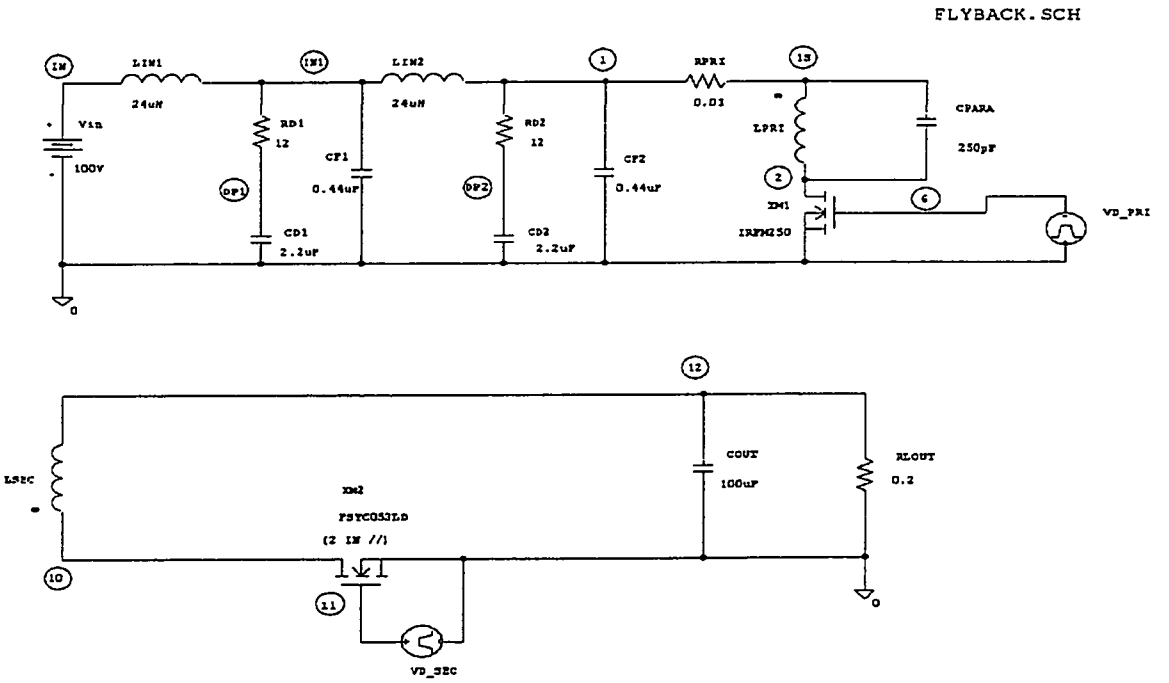


Figure 2.20 PSPICE Model of ZVT Flyback Converter

The results of the simulation are shown on Figure 2.21.

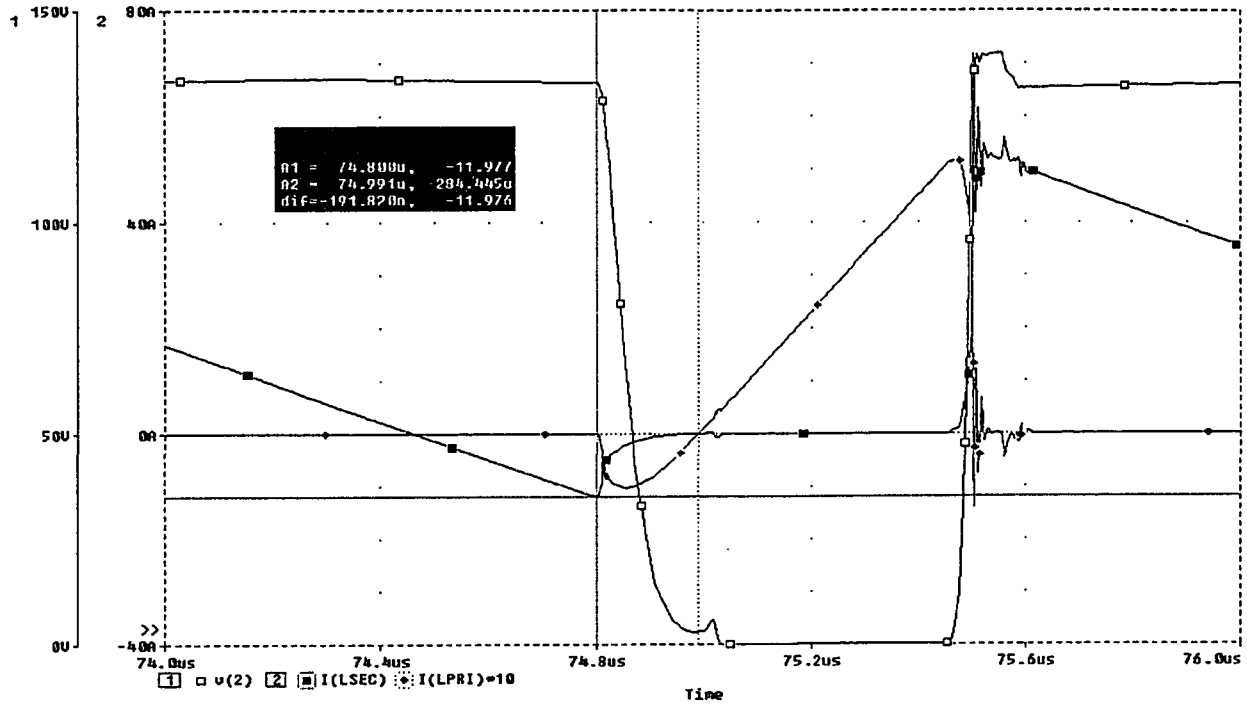


Figure 2.21 Simulation Results for the ZVT Flyback Converter

Shown on Figure 2.21 are the waveforms of the drain voltage of M1, the current through the transformer secondary and the current through the transformer primary, reflected to the secondary. (see Figure 2.20 above). As can be seen from the simulation, a secondary current I_{neg_pk} of 12 A causes the commutation to occur in 192 ns, very close to the above calculations. It can also be seen that the natural commutation is incomplete: there is a residual voltage of about 3 V, which is then cleared by the forced turn-on of Q1; this incomplete ZVT corresponds to $I_{end} = 0$, as opposed to the calculated value of 1.7 A. This is a direct consequence of having reduced the transformer magnetizing inductance from 101 to 91 nH (less energy stored in L_{sec}).

Since we have now calculated all the parameters, we are now in a position to calculate the RMS values of the transformer primary and secondary currents and therefore,

the conduction losses in the ZVT Flyback converter. This calculation is detailed in Appendix A.

The overall conduction losses for the ZVT Flyback converter were found equal to 5.3 W.

2.7 Comparison summary

The comparison carried out in the previous paragraphs yielded the results shown in Table 2.2 below.

Table 2.2 Efficiency comparison of three topologies

	ZVS Forward Converter	ZVS CHBC	ZVS Flyback Converter
Turns Ratio (N)	17	12	10
Duty Cycle (%)	61.8	32.1	25.9
I_{pk} Ref. to primary (A)	3	4.3	5.24
I_{neg_pk} Ref. to primary (A)	2.1	3.5	1.19
Transformer winding + interconnection losses (W)	1.12	1.445	2.431
Primary MOSFETs conduction losses (W)	0.663	0.606	0.313
Secondary MOSFETs conduction losses (W)	2.048	2.048	2.543
Total Conduction Losses (W)	3.83	4.1	5.3

The higher losses occurring in the Flyback converter are due to the fact that, unlike in the other two converters, the steep slope of the modified primary current is also seen on the secondary side. This causes the RMS secondary current to be quite high, which in turn

causes high conduction losses in the secondary winding as well as in the synchronous rectifiers.

The losses in the ZVT Forward converter are comparable to those occurring in the ZVT Complementary Half Bridge converter.

However, the half bridge carries the significant advantage of requiring 200 V MOSFETs on the primary side as opposed to 400 V MOSFETs required by the forward converter. So far, 400 V RadHard MOSFETs have been supplied by only one manufacturer and have not been available in any surface mount package.

Also, comparison of Figure 2.9 and Figure 2.17 shows that the transition times are much longer in the ZVT Forward converter than in the ZVT Complementary Half Bridge. This in turn puts a limit to the switching frequency.

For these reasons, the complementary half bridge topology is the chosen topology for developing a +3.3 V converter.

Chapter 3
Design of a ZVT Complementary Half Bridge Converter

3.1 Introduction

The comparative study carried out in Chapter 2 concluded that the ZVT Complementary Half Bridge (ZVT CHB) was the best topology in terms of efficiency for developing a 100 V to 3.3 V converter. We now want to design such a converter, based on the schematics shown on Figure 2.10 and Figure 2.16 and taking full advantage of the principles developed in the previous chapter.

We will choose a switching frequency of 400 kHz.

3.2 Power Circuit Description

The schematic of the proposed converter power section is shown on Figure 3.1 below.

The proposed schematic differs from the one shown on Figure 2.10 and Figure 2.16 in that it implements a current doubler on the secondary side; this current doubling technique is described in detail in [11] to [14] and offers the following significant advantages:

The transformer secondary has only one winding as opposed to two windings with a center tap in Figure 2.10, which greatly simplifies its construction.

Since each output inductor carries half of the output current, only half of the output current flows through the transformer secondary winding at any moment, which reduces the secondary copper losses by a factor of 4.

As will be shown further in this chapter, the disappearance of the center tap at the transformer secondary winding has the effect of reducing the transformer turns ratio by a factor of two; this means that for the same number of secondary turns, only half the number of primary turns are needed for the current doubler topology, which greatly simplifies the construction of the primary winding. It should be noted that, with the new turns ratio divided by two, the primary current remains unchanged with respect to the non current doubler topology because the secondary current is also divided by two; as a result, having only half the primary turns with the same primary current results in primary copper losses divided by two.

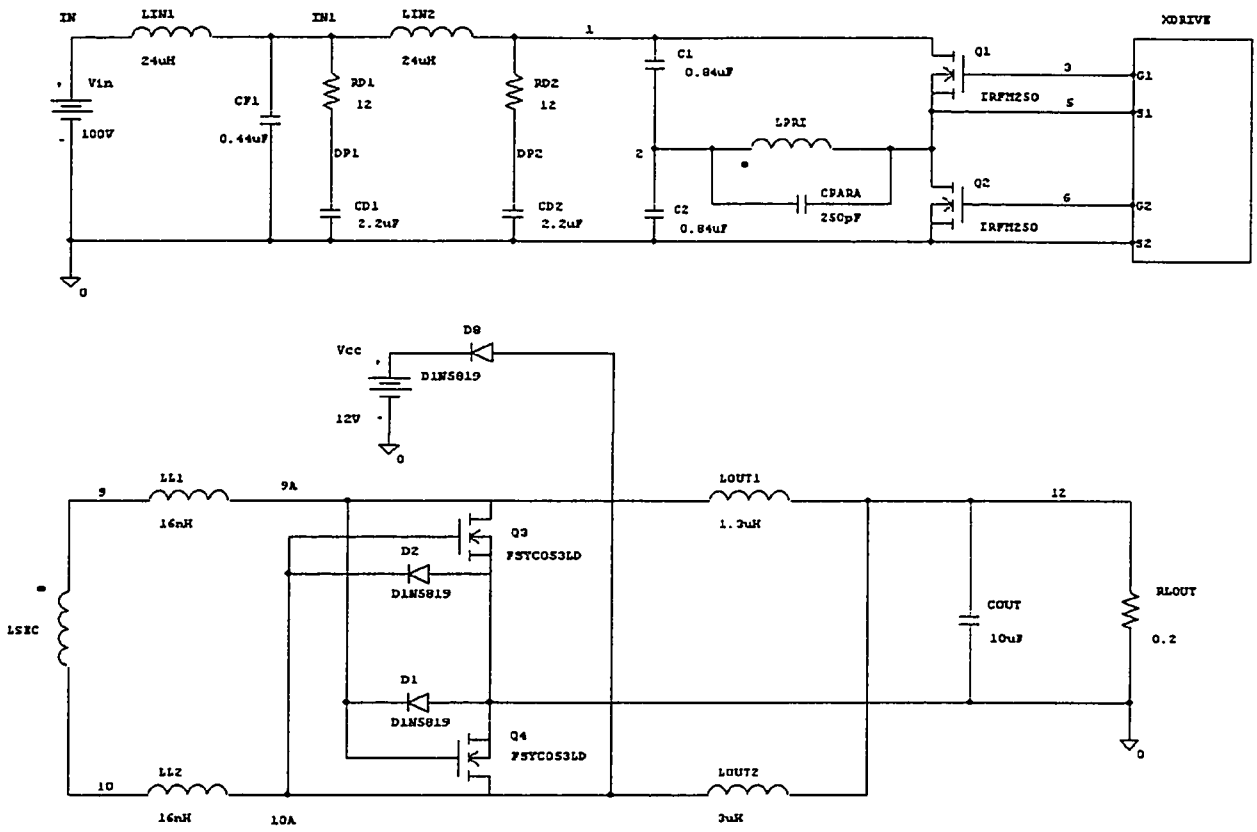
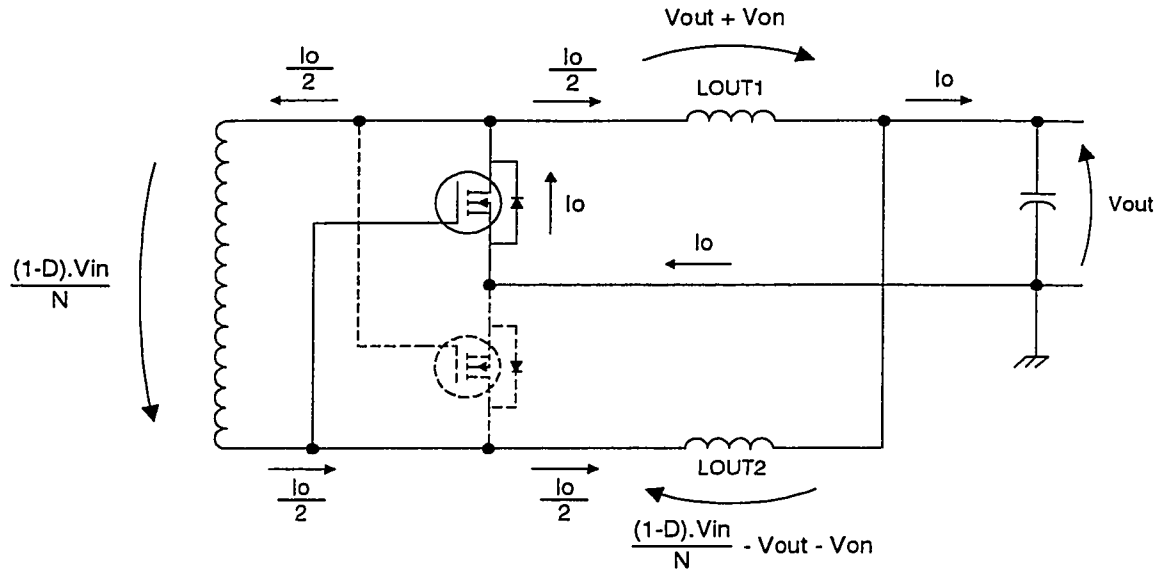


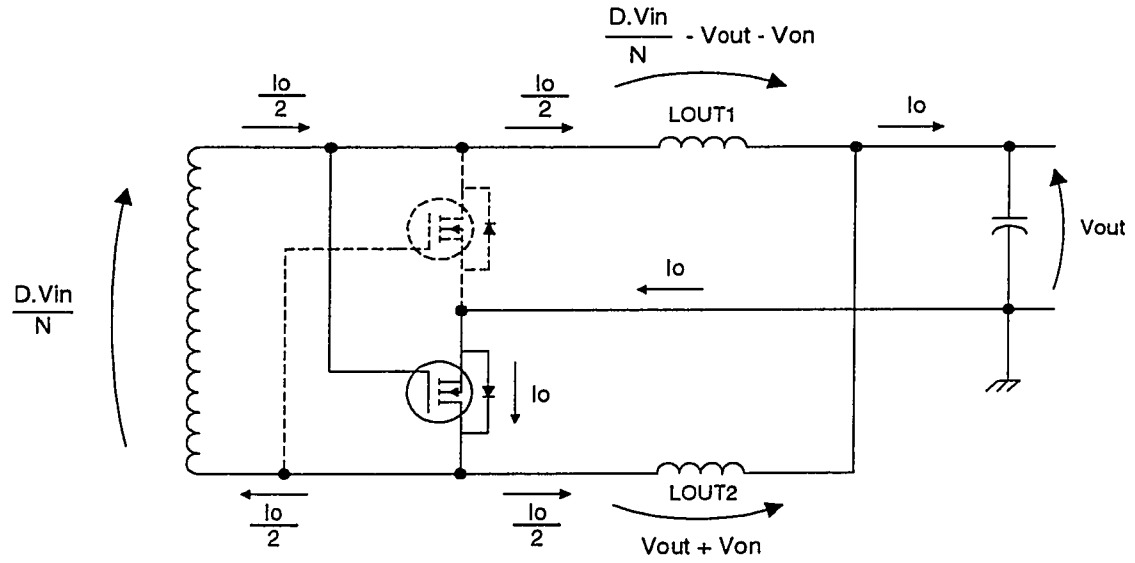
Figure 3.1 ZVT CHB Schematic (Power section)

Figure 3.2 shows the voltages and currents amplitudes at different points of the circuit during primary MOSFET Q1's conduction time $D \cdot Ts$ and during primary MOSFET Q2's conduction time $(1-D) \cdot Ts$. As can be seen from Figure 3.2, the secondary synchronous rectifiers are self driven, i.e. their gate to source voltage is directly derived from the power transformer secondary winding.

Figure 3.3 shows the ZVT CHB secondary rectifier stage along with the idealized waveforms of the voltage across the transformer secondary, the voltages at points A and B and the secondary current.



ZVT CHB OUTPUT STAGE DURING D x Ts



ZVT CHB OUTPUT STAGE DURING (1-D) x Ts

Figure 3.2 ZVT CHB Secondary Stage during *D* × *Ts* and during (1-*D*) × *Ts*

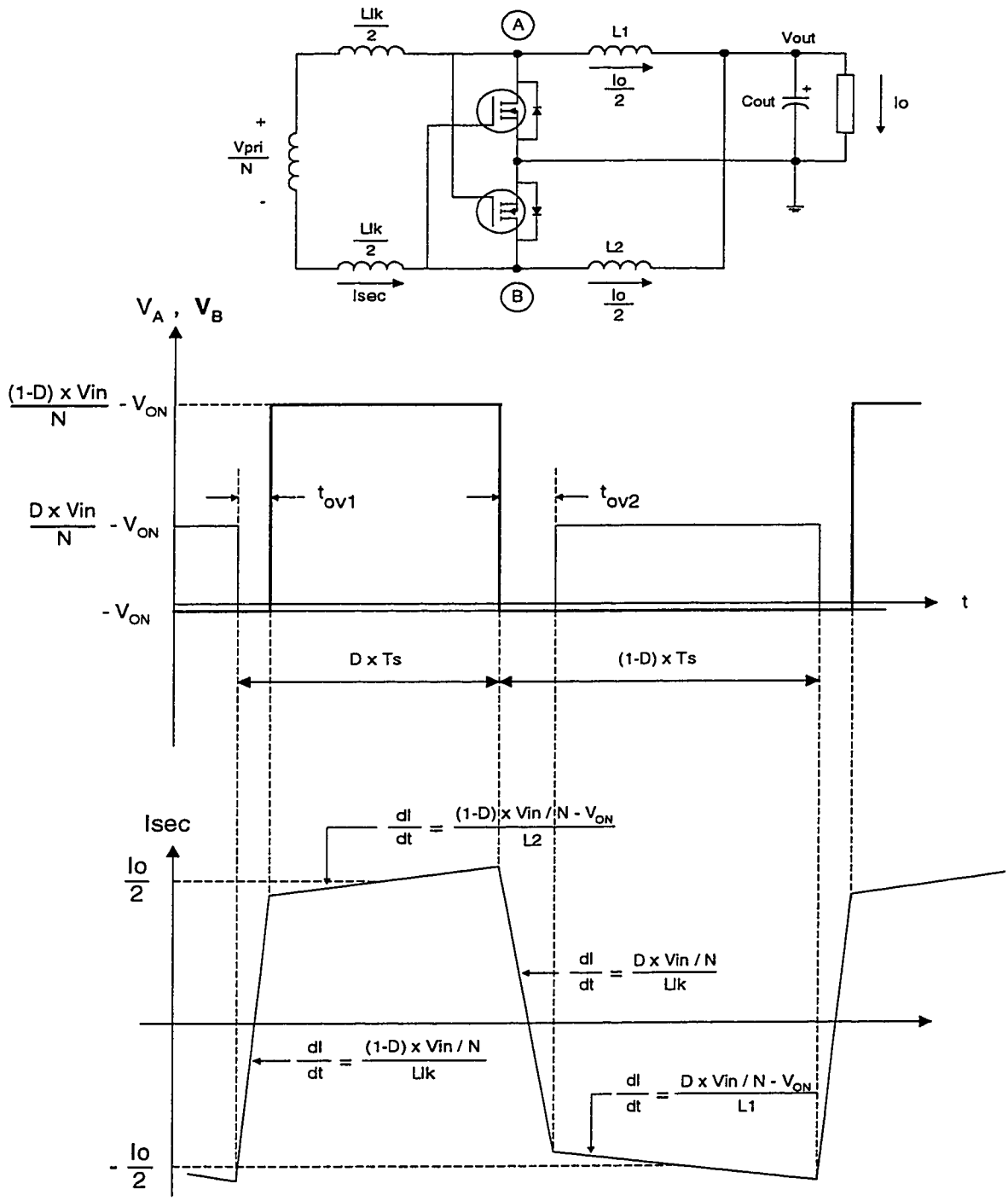


Figure 3.3 ZVT CHB Secondary Stage: Idealized Waveforms

With reference to Figure 3.3, the voltage waveforms at points A and at point B are filtered by output filters: $L1$, C_{out} and $L2$, C_{out} respectively. Therefore, the output voltage can easily be calculated since it is simply the average value of the voltage at point A or at point B.

Taking the average value of voltage at point B and calling V_{on} the voltage drop across each synchronous rectifier when it is conducting, we obtain

$$V_{out} = V_{B\_average} = \frac{1}{Ts} \cdot \left[\left[\frac{(1 - D) \cdot V_{in}}{N} - V_{on} \right] \cdot (D \cdot Ts - t_{ov1}) - V_{on} \cdot (Ts - D \cdot Ts + t_{ov1}) \right]$$

$$\text{or} \qquad V_{out} + V_{on} = \frac{1}{Ts} \cdot \frac{(1 - D) \cdot V_{in}}{N} \cdot (D \cdot Ts - t_{ov1})$$

In the above two expressions, t_{ov1} is one of the two overlap periods which had already been identified in paragraph 2.5.

Since during the commutations, the current through the transformer secondary undergoes a variation whose amplitude is equal to I_o, it is easily shown that

$$t_{ov1} = \frac{L_{lk} \cdot I_o}{\frac{(1 - D) \cdot V_{in}}{N}} \tag{3.1}$$

Therefore,

$$V_{out} = \frac{D \cdot (1 - D) \cdot V_{in}}{N} - L_{lk} \cdot I_o \cdot Fs - V_{on} \tag{3.2}$$

where $Fs = \frac{1}{Ts}$ is the switching frequency; the same result would have been found by calculating the average value of the voltage at point A.

If we compare expression (3.2) above with expression (2.5.5), we see that they are almost identical except for the factor of 2 in the numerator of (2.5.5). Therefore, if all other

parameters are kept the same, (2.5.5) and (3.2) will yield identical values of output voltage if the turns ratio N in (3.1) is made equal to one half the turns ratio in (2.5.5).

If the turns ratio is reduced by a factor of two, then expressions (3.1) and (2.5.2) also yield identical values of t_{ov1}. It is easily shown that this conclusion can be extended to all parameters calculated in paragraph 2.5.

Therefore all the analysis made in paragraph 2.5 remains valid provided we divide the turns ratio by two. The turns ratio N found in paragraph 2.5 was equal to 12; hence, from this point on, we will adopt a turns ratio N equal to 6.

3.3 Output Filter Design

The proposed modification of the standard ZVT CHB converter has the drawback of introducing a second output inductor *L2*. It offers however the potential of reducing the output ripple current into the output capacitor to zero for a specific value of the duty cycle.

Figure 3.4 shows the idealised waveforms of the current through *L1*, the current through *L2* and the output current before the output capacitor, which is the sum of I_{L1} and I_{L2}.

It can be seen from the figure that the output current ripple ΔI_o is equal to $\Delta I_{L1} - \Delta I_{L2}$.

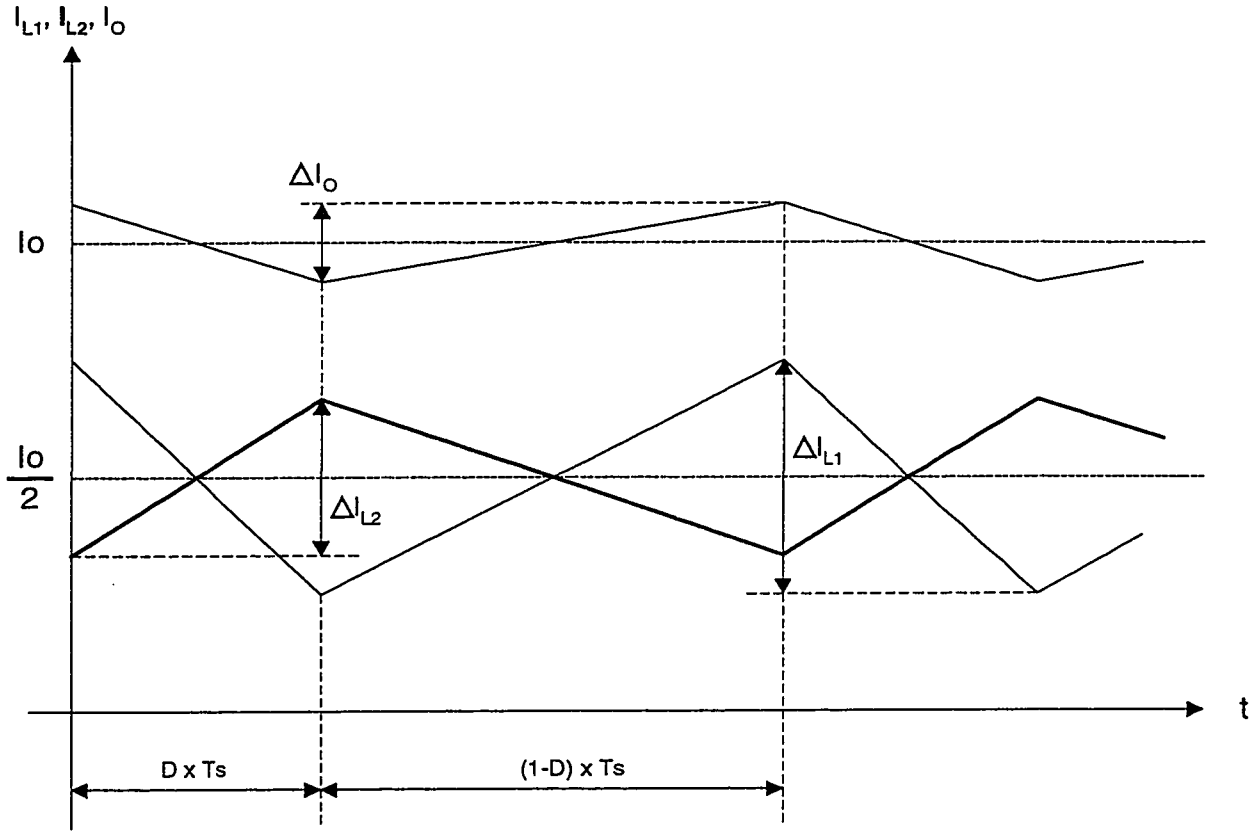


Figure 3.4 Idealized Current waveforms in ZVT CHB Output Inductors

Referring to Figure 3.2 which shows the voltages applied to L1 and L2 during $D \cdot Ts$ and $(1-D) \cdot Ts$, we can easily calculate ΔI_{L1} and ΔI_{L2}.

$$\Delta I_{L1} = \frac{V_{out} + V_{on}}{L1} \cdot D \cdot Ts$$

$$\Delta I_{L2} = \frac{V_{out} + V_{on}}{L2} \cdot (1 - D) \cdot Ts$$

For a specific value of the duty cycle D which corresponds to the nominal input voltage, we want to make $\Delta I_o = 0$.

Therefore, $\Delta I_{L1} - \Delta I_{L2} = 0$ or $\frac{V_{out} + V_{on}}{L1} \cdot D \cdot Ts - \frac{V_{out} + V_{on}}{L2} \cdot (1 - D) \cdot Ts = 0$

This yields

$$L2 = L1 \cdot \frac{1 - D}{D} \tag{3.3}$$

From paragraph 2.5, the value of D corresponding to the nominal input voltage of 100 V equals 0.321; therefore, from (3.3), $L2 = 2.115 \times L1$.

In order to calculate the actual values of $L1$ and $L2$, we must define a maximum value of the output ripple current ΔI_o; Let's choose: $\Delta Io_{max} = 1.5$. We must now determine the value of the duty cycle where the above ripple current will occur.

From above,

$$\Delta I_o = \Delta I_{L1} - \Delta I_{L2} = \frac{V_{out} + V_{on}}{L1} \cdot D \cdot Ts - \frac{V_{out} + V_{on}}{L2} \cdot (1 - D) \cdot Ts$$

If we replace $L2$ by $2.115 \times L1$ in the above, we obtain

$$\Delta I_o(D) = \frac{V_{out} + V_{on}}{L1} \cdot Ts \cdot \frac{3.115 \cdot D - 1}{2.115} \tag{3.4}$$

The above expression reduces to zero for $D = 0.321$ as expected. From paragraph 2.5 and Appendix A, the values of D corresponding to the minimum and maximum input voltages are

$D_{min} = 0.273$ for $V_{in} = 110$V and $D_{max} = 0.5$ for $V_{in} = 90$V.

From (3.4),

$$\Delta I_o(D_{min}) = -0.071 \cdot \frac{V_{out} + V_{on}}{L1} \cdot Ts \tag{3.5}$$

whereas

$$\Delta I_o(D_{max}) = 0.264 \cdot \frac{V_{out} + V_{on}}{L1} \cdot Ts \qquad (3.6)$$

From above, it is clear that the worst case corresponds to $D = D_{max} = 0.5$.

Having chosen $\Delta Io_{max} = 1.5$ and knowing all other parameters, we can calculate $L1$ from (3.6).

We obtain $L1 = 1.54$ µH.

$L2 = 2.115 \times L1 = 3.26$ µH

Output capacitor calculation We impose a maximum output peak to peak ripple of 15 mV at the switching frequency of 400 kHz.

The peak to peak ripple voltage is given by $\Delta V_{out} = \frac{\Delta I_o}{8 \cdot Fs \cdot C_{out}}$

where ΔI_o is the worst case value of 1.5 A

We need $\Delta V_{out} := 15$ mV therefore, $C_{out} = 31.25$ µF

3.4 Transformer Design

In order to respond to the market trend for ever lower profile DC to DC converters, we deliberately chose to design the transformer as a low profile customized geometry. The magnetic core is a custom E - I shape made of Philips 3F3 ferrite material. The core is designed in such a way as to accommodate a small Printed Circuit Board (PCB) which contains the transformer windings. As explained above, the transformer turns ratio for this topology is equal to 6. Since the output voltage we are to generate is very low (3.3 V), the

secondary winding may consist of only one turn and therefore, the primary winding will have 6 turns.

Figure 3.5 below shows the cross-section of the PCB which contains the transformer windings. As can be seen, the PCB consists of 10 layers, six of which contain the primary winding and the remaining four layers are connected in parallel to make up the secondary winding. The second part of Figure 3.5 shows two consecutive primary layers and one secondary layer. As can be seen from the layer build-up and from the detailed layer drawing, each primary section consists of 2 layers comprising three turns each and connected in series. There are three identical primary sections which are interleaved with the secondary layers and connected in parallel. This design minimises leakage inductance and AC copper losses.

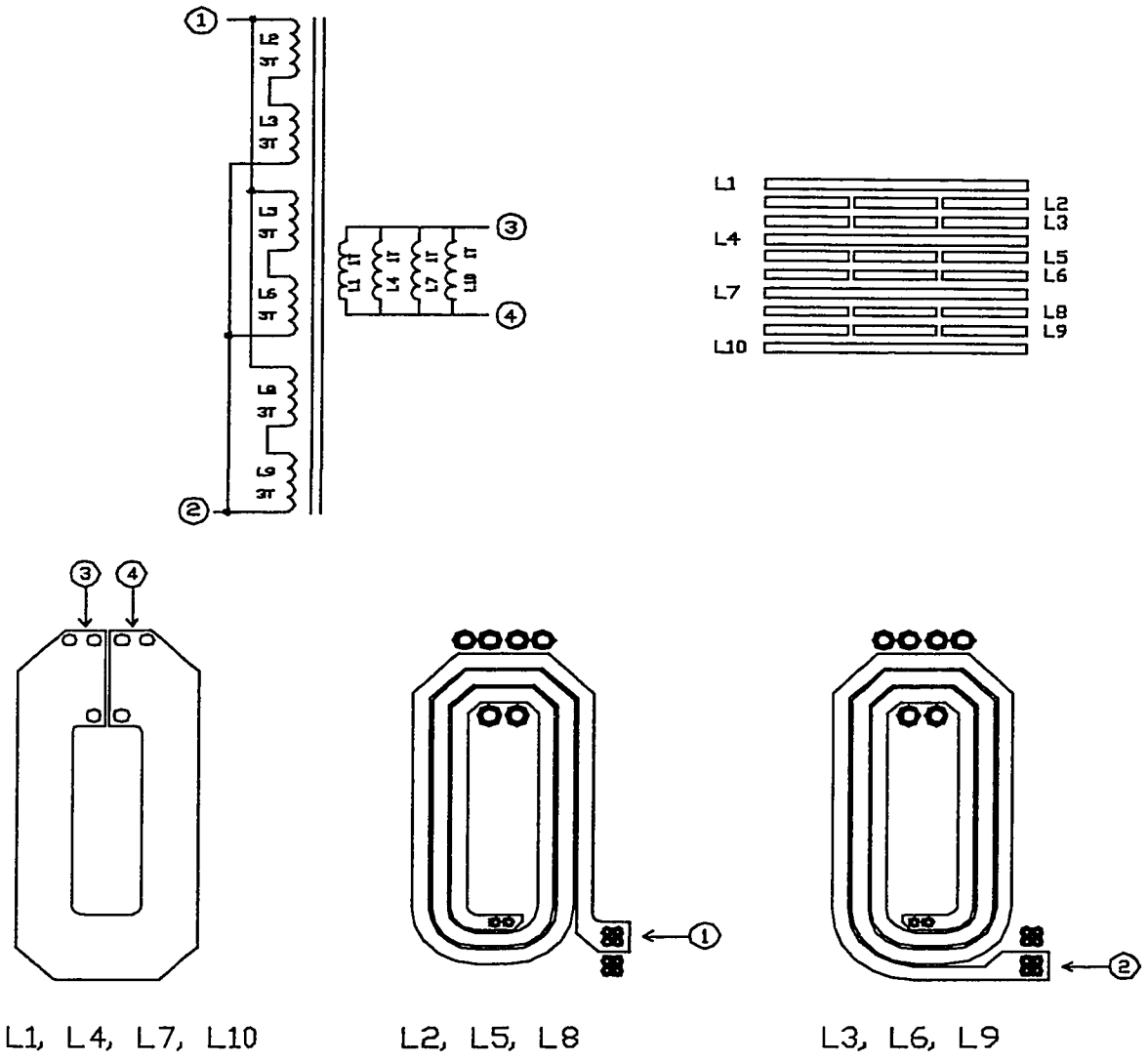


Figure 3.5 Main Power Transformer Design

There is a gap in the center leg of the magnetic core which yields a primary inductance value of 10 μH in accordance with the analysis carried out in paragraph 2.5.

The magnetic core has a cross-section A_c of 0.7 cm^2 , thus the AC flux density is calculated as follows:

$$B_{ac} := \frac{1}{2}\cdot\frac{D\cdot(1-D)\cdot V_{in}}{N\cdot A_c\cdot Fs} \quad \text{or} \quad B_{ac} = 0.065 \text{ Tesla}$$

This value of flux density yields a core loss of 0.377 W for a 3F3 material at 400 kHz

As has been identified in [4] and [5], the transformer used in this topology has a DC magnetizing current whose average value equals

$$I_{magn\_DC} := \frac{I_o}{2\cdot N}\cdot(1-2\cdot D)$$

This DC magnetizing current in turn creates a DC flux density in the magnetic core. The peak flux density in the core is the sum of the DC flux density and the AC flux density calculated above and must be kept below the saturation flux density of 0.3 Tesla for ferrites. B_{AC} was calculated above as 0.065 Tesla.

Let's calculate B_{DC}.

We have

$$N\cdot\Phi_{DC} = L_{pri}\cdot I_{magn\_DC} \quad \text{or} \quad B_{DC} = \frac{L_{pri}\cdot I_{magn\_DC}}{N\cdot A_c}$$

From the above expression of I_{magn_DC}, we finally obtain

$$B_{DC} = \frac{L_{pri}\cdot I_o\cdot(1-2\cdot D)}{2\cdot N^2\cdot A_c}$$

L_{pri} = 10 μH, N = 6, A_c = 0.7 cm^2 , I_o = 15 A and D = 0.321.

Therefore, B_{DC} = 0.011 Tesla.

Hence, $B_{max} = B_{DC} + B_{AC}$ = 0.076 Tesla which is well below 0.3 Tesla.

The winding losses in the transformer are the sum of the primary losses and the secondary losses.

The PCB transformer whose geometry has been described above has a primary DC resistance of 33 mΩ and a secondary DC resistance of 1 mΩ.

The windings losses are equal to

$$P_{wdg} := R_{pri} \cdot I_{pri\_RMS}^2 + R_{sec} \cdot I_{sec\_RMS}^2$$

where

$R_{pri} := 0.033$

$R_{sec} := 0.001$

$I_{pri\_RMS} := 1.946$ A (calculated in Appendix A)

$$I_{sec\_RMS} := \frac{I_o}{2}$$

We obtain $P_{wdg} = 0.181$ W

In reality, the winding losses will be substantially higher because the primary and secondary windings exhibit AC resistances significantly higher than the DC resistances due to proximity effect. The primary and secondary resistances were measured at different frequencies up to 1 MHz with the opposite winding open and shorted; the secondary resistance measurement was inconclusive because of the difficulty to measure a very low resistance value (1 mΩ); the primary resistance measurement yielded the following results at 400 kHz:

R_{pri} with secondary open: $Rpri\_open = 0.125\ \Omega$

R_{pri} with secondary shorted: $Rpri\_short = 0.090\ \Omega$

The reason why *Rpri_open* is higher than *Rpri_short* is believed to lie in the fact that when measuring the primary resistance with the secondary open, the primary current is not cancelled by any secondary current; as a result, the magnetic field outside the transformer windings is non zero; this may cause the existence of a magnetic field component perpendicular to the copper layers which compose the windings (see Figure 3.5); this in turn causes large eddy currents to circulate in the copper planes which creates higher losses.

By contrast, when the secondary winding is shorted, the , the magnetic field outside the transformer windings is equal to zero by virtue of Ampere's Law; this forces the magnetic field inside the windings to be parallel to the copper layers, which precludes the existence of any H-field component normal to the copper layers.

The primary resistance characterization exercise yielded two curves of resistance versus frequency. A curve fitting technique allowed us to obtain two empirical analytical expressions for the primary resistance *Rpri_open(f)* and *Rpri_short(f)* .

In the subsequent efficiency calculations, the two empirical curves of primary resistance obtained above will be used as follows:

The primary current is the sum of the load current I_{LOAD} which is reflected to the secondary winding and of the magnetizing current I_{MAGN} which flows into the primary winding only. It is therefore reasonable to assume that the magnetic field outside the transformer windings due to I_{LOAD} is zero, whereas the magnetic field outside the windings due to I_{MAGN} is non zero. On the other hand, both I_{LOAD} and I_{MAGN} have fundamental terms and harmonics; therefore, a first order approximation of transformer winding losses is given by

$$P_{wdg} = \sum_n R_{pri\_short}(n \cdot Fs) \cdot \frac{\left(I_{LOAD_n}\right)^2}{2} + \sum_n R_{pri\_open}(n \cdot Fs) \cdot \frac{\left(I_{MAGN_n}\right)^2}{2} \qquad (3.7)$$

where Fs is the switching frequency, I_{LOADn} and I_{MAGNn} are the Fourier series terms of the load current and magnetizing current respectively; the above sum is truncated at $n = 8$.

Using (3.7), we obtain $P_{wdg} = 0.475$ W at 400 kHz, well above the value of 0.181 W obtained using only DC resistances.

3.5 Gate Drive Circuit

As discussed earlier, the primary MOSFETs Q1 and Q2 are driven in a complementary fashion; however, in order to allow the soft transition to occur, a delay must be implemented between the turn-off of Q1 and the turn-on of the complementary transistor Q2. Likewise, an equal delay must be implemented between the turn-off of Q2 and the turn-on of Q1. If no delay was present between the turn-off of one MOSFET and the turn-on of the other MOSFET, then the latter would undergo a "hard" transition, which would defeat the whole purpose of ZVT.

The delays described above must obey two criteria:

1. Their accuracy must be sufficiently well controlled in order to ensure a reasonable degree of delay repeatability from one circuit to the next and also in order to avoid the possibility of delay drifting over temperature and life.

2. The generation of these delays must not result in gate drive signals having rising and falling edges less sharp than the original pulse width modulator output signal.

The above two criteria preclude the use of simple R - C delay circuits because they have poor accuracy and because they do not retain the sharp edges which are required to drive the MOSFET gates.

The retained delay generation scheme is shown on Figure 3.6. As can be seen, it consists of a classical Pulse Width Modulator IC which controls the duty cycle based on the control loop error signal, followed by a delay generator IC; it should be noted that the

selected delay generator IC produces output signals V_{Q1} and V_{Q2} which have low output impedance and therefore have adequate gate drive capability.

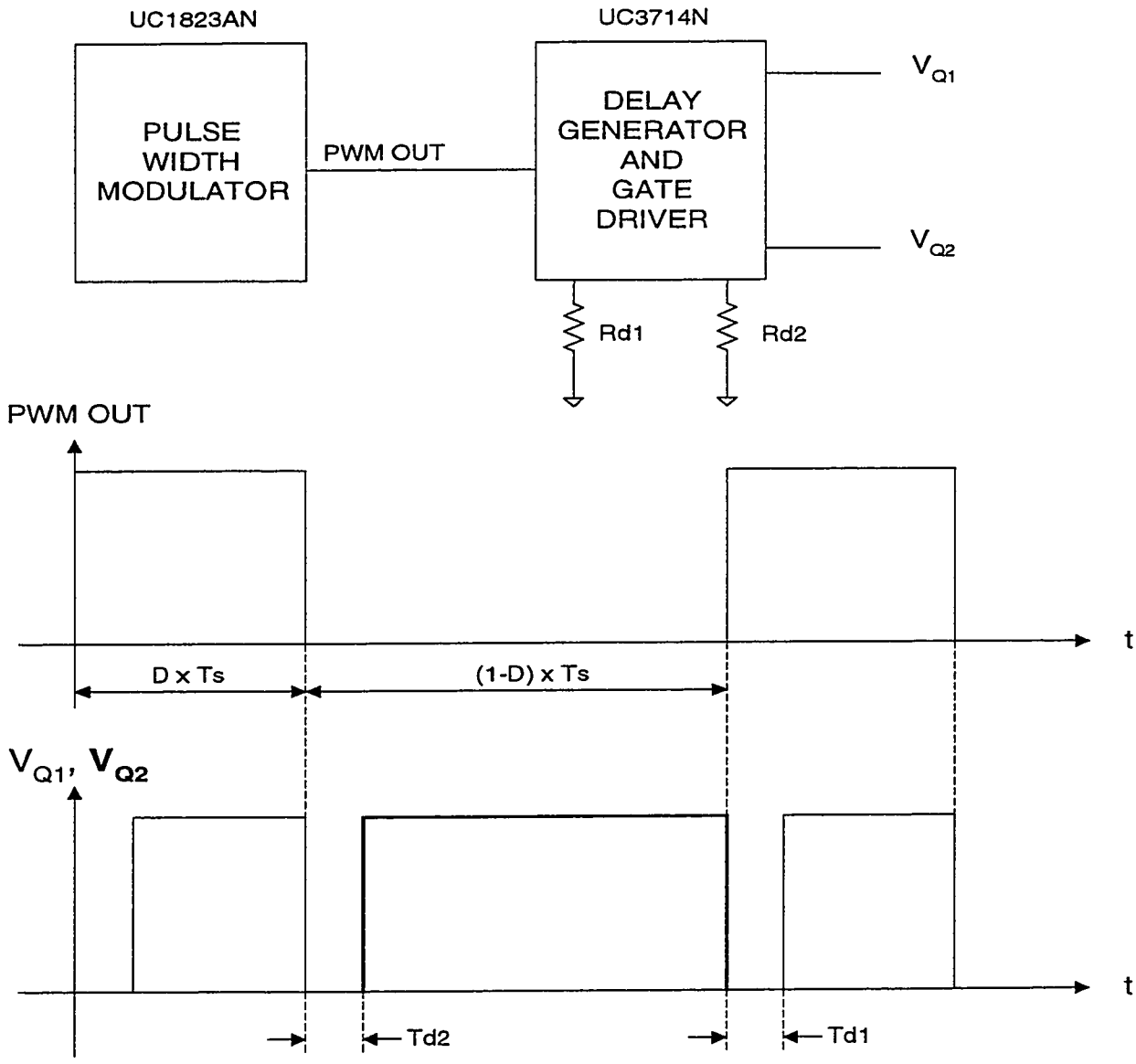


Figure 3.6 Gate Drive Signal Generation for Q1 and Q2

The timing of V_{Q1} and V_{Q2} with respect to the Pulse Width Modulator signal is shown on the bottom part of Figure 3.6. As can be seen, two delays T_{d1} and T_{d2} are generated

between the turn-off of one MOSFET and the turn-on of the other MOSFET. These two delays T_{d1} and T_{d2} are independently programmable through two external resistors R_{d1} and R_{d2}.

If appropriate delays are implemented between the gate drive signals and if the circuit is capable of achieving a full ZVT as per the criteria defined in Chapter 2, then each primary MOSFET is turned on under zero voltage, i.e. when its antiparallel diode is conducting. As a consequence, no stringent delays and gate drive capability requirements are imposed on the turn-on of the primary MOSFETs because no turn-on losses will occur as a result of a V_{gs} rise slower than normal.

By contrast, the turn-off action must be fast in order to minimise MOSFET turn-off losses.

The gate drive circuit for MOSFET Q2 (the bottom primary MOSFET on Figure 3.1) is shown on Figure 3.7.

As the ZVT CHB circuit uses two complementary MOSFETs, a circuit identical to the one shown is used to drive MOSFET Q1.

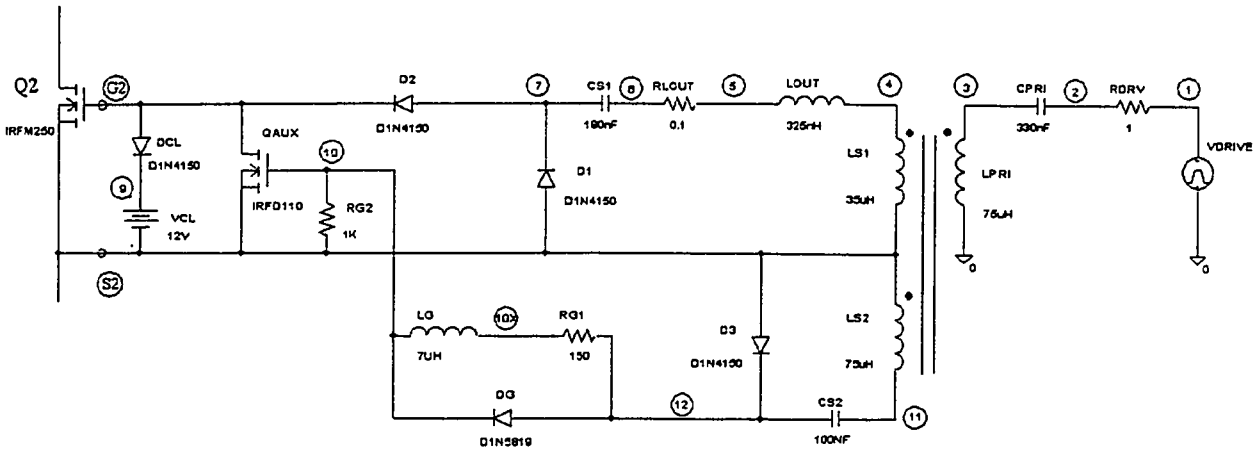


Figure 3.7 Primary MOSFET Gate Drive Circuit

As can be seen from Figure 3.7, the gate drive circuit is transformer coupled, consistent with the isolation requirement between the control circuit and the power MOSFETs. The gate drive transformer consists of primary winding L_{PRI} and secondary windings L_{S1} and L_{S2}. While secondary winding L_{S2} is tightly coupled to the primary winding, L_{S1} instead is loosely coupled to L_{PRI}. Therefore, L_{S1} exhibits a substantial leakage inductance represented by L_{OUT}. This leakage inductance in turn allows this circuit to charge the power MOSFET gate to source capacitance in a resonant fashion. It is shown [20, 21] that substantial power savings result from this gate drive technique.

On the other hand, the resonant gate drive results in a slower MOSFET turn-on than in a conventional gate drive scheme. In our application however, this slower than normal turn-on has no impact on circuit performance as per the above discussion. Therefore, this drive scheme is quite acceptable.

Referring to Figure 3.7, the power MOSFET is turned on when the driving signal V_{DRIVE} goes positive. A resonant half cycle takes place on the secondary side between L_{OUT} and MOSFET Q2's $Ciss_{ON}$. When the resonant half cycle is over, diode D2 becomes reverse

biased and prevents Q2's $Ciss_{ON}$ from being discharged. It should be noted that the resonant transition allows the voltage at node *G2* to rise to a higher value than the voltage across the transformer secondary winding L_{S1} (node 4). This in turn allows a turns ratio between L_{S1} and L_{PRI} less than one (in our case, this turns ratio has been set at 0.67); in turn, this results in a substantial reduction of gate drive power because the total charge delivered by the primary gate drive circuit equals Q2's total gate charge reflected to the primary side, i.e. multiplied by 0.67.

When the driving signal V_{DRIVE} goes back to zero, the voltage across the transformer changes polarity, which causes the voltage at node 11 to become positive. This causes MOSFET Q_{AUX} to turn on and consequently, to provide a quick discharge path for Q2's $Ciss_{ON}$.

Figure 3.8 shows the simulated waveforms of the Gate to Source and Drain to Source voltages of MOSFET Q2 of the schematic shown in Figure 3.1. Figure 3.9 shows the waveforms of the above voltages in the real circuit. It can be seen from both the simulation and the measurement that the V_{GS} waveform exhibits a smooth resonant rising edge and a sharp falling edge, in accordance with the above discussion.

Figure 3.10 shows the simulated V_{GS} of Q2 along with the voltage at the anode of D2 (Node 7 on Figure 3.7). Figure 2.1 shows the actual captured waveforms at the corresponding points in the breadboard. From these two figures, the resonant action described above is quite evident.

3.6 Converter Test Results and Waveforms

The prototype 3.3 V converter shown in Figure 3.1 was simulated using PSPICE and tested under power at P_{out} = 50 W, Fs = 400 kHz and with a transformer primary inductance of 10 μH.

In the simulation, the duty cycle was adjusted in order to obtain an output voltage of 3.3 V under full load (15 A). The PSPICE model makes full use of the MOSFET model with the non-linear gate to drain capacitance developed in Appendix B.

Figure 3.12 shows the simulated waveforms of the Drain to Source voltage of Q2, along with the transformer primary current. Figure 3.13 shows the same waveforms captured in the real circuit. The comparison of the two figures shows an excellent agreement between the simulation and the actual measurement. Both the simulation and the measurement yield a value of I_{neg_pk} equal to -3.5 A, in accordance with the results of paragraph 2.5; in addition, it can be seen that this value of I_{neg_pk} is just sufficient to cause a full zero voltage transition, in full agreement with the result predicted by Figure 2.15.

Figure 3.14 shows the captured waveforms of secondary synchronous rectifiers Q3 and Q4 gate to source voltages. The waveforms of Figure 3.14 correspond to the idealized waveforms at points A and B shown on Figure 3.3. Except for the oscillation which is superimposed onto the ideal flat levels in the real measurement, the correlation between Figure 3.14 and Figure 3.3 is very good. Moreover, Figure 3.14 clearly shows the overlap times t_{ov1} and t_{ov2} which have been discussed previously.

The durations of t_{ov1} and t_{ov2} measured on Figure 3.14 are the following:

$t_{ov1} = 60$ ns and $t_{ov2} = 120$ ns.

The theoretical durations, calculated using (2.5.2) and (2.5.3) with L_{lk} = 33 nH (measured on the real breadboard) and $D = 0.321$ would yield the following results:

$t_{ov1} = 44$ ns. and $t_{ov2} = 95$ ns

The measurements are shown to be in good agreement with the theoretical values.

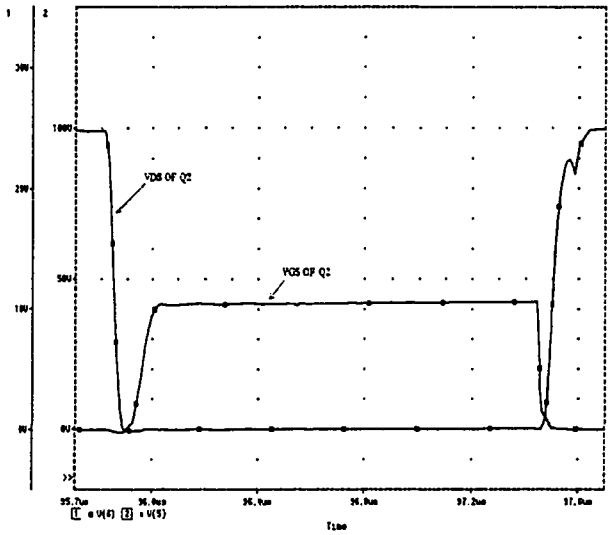


Figure 3.8 Simulated V_{GS} and V_{DS} of Q2

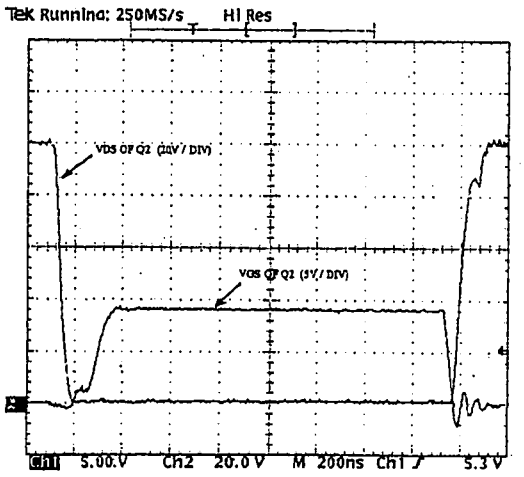


Figure 3.9 Measured V_{GS} and V_{DS} of Q2

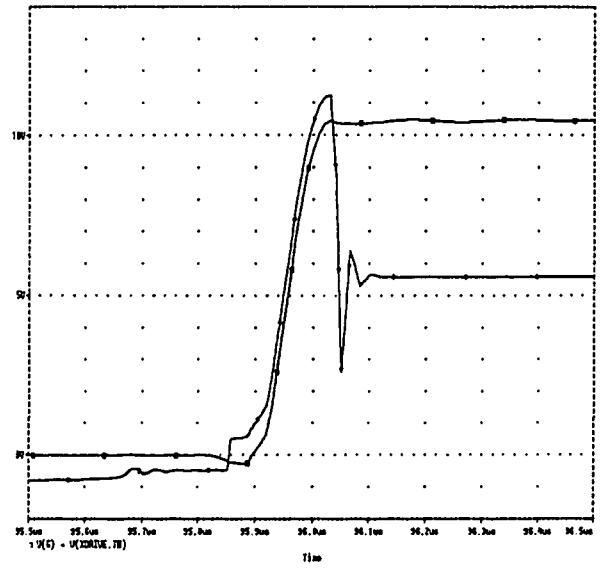


Figure 3.10 Simulated Q2 V_{GS} and V at anode of D2

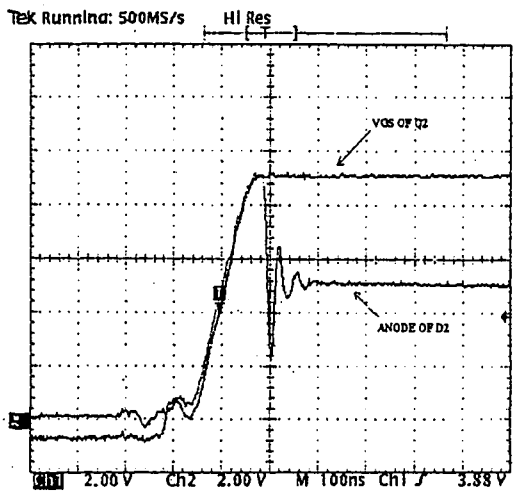


Figure 3.11 Measured Q2 V_{GS} and V at anode of D2

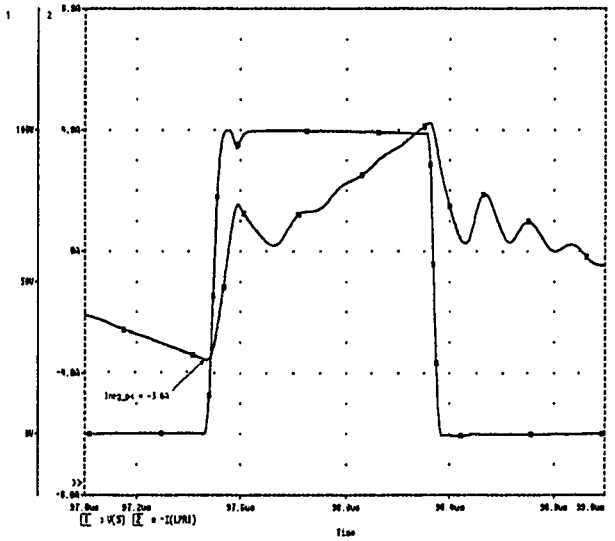


Figure 3.12 Simulated Q2 VDS and Primary Current

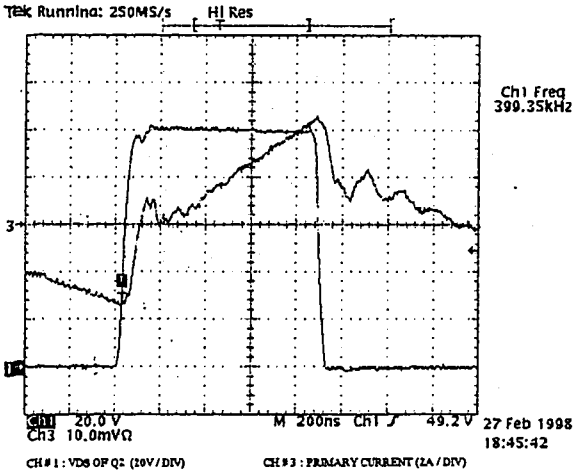


Figure 3.13 Measured Q2 VDS and Primary Current

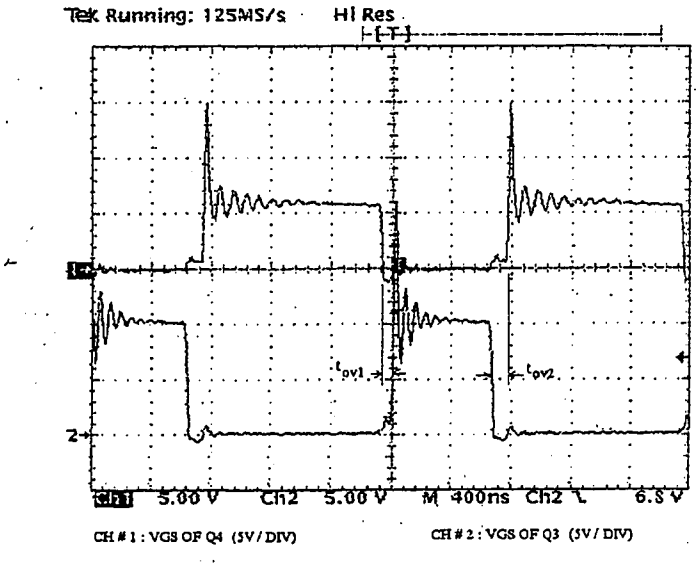


Figure 3.14 Measured V_{GS} of Q3 and Q4

3.7 Converter Efficiency

The prototype converter as shown on Figure 3.1 was tested at a switching frequency of 400 kHz, an input voltage of 100 V and an output current of 15A. The measured efficiency was 85.4%.

It was immediately recognized that the addition of a second MOSFET in parallel with Q4 could be beneficial to efficiency because Q4 conducts during $(1\text{-}D) \times Ts$, i.e. during most of the period. Therefore, the effective Rds_{ON} would be reduced by a factor of two during $(1\text{-}D) \times Ts$ and hence would greatly alleviate the conduction losses.

On the other hand, the additional MOSFET would introduce extra parasitic capacitance which not only would increase the switching losses but might also prevent full ZVT from occurring on the primary side. With the additional MOSFET, the measured efficiency was 86.5 %, which indicates that the savings in conduction losses exceeded the additional switching losses due to increased parasitic capacitance.

As a first step towards converter optimization, a mathematical model which calculates efficiency was developed based on the following degrees of freedom:

Switching frequency: Although the implementation of ZVT makes the converter relatively immune to switching losses, the converter will still experience significant efficiency variations for the following reasons:

The energy stored in the parasitic MOSFET capacitances on the secondary side can only be partially recovered. An important part of this capacitive energy is dissipated in the synchronous rectifier gate resistances.

During the overlap times t_{ov1} and t_{ov2}, the synchronous rectifiers conduct through their antiparallel diodes; as a result, these will experience reverse recovery losses which are proportional to the operating frequency.

As was outlined in paragraph 3.4, the higher the switching frequency, the higher the losses occurring in the transformer windings as a result of proximity effect.

Number of secondary synchronous rectifiers in parallel: Based on the above discussion, it is quite important to find out if the addition of synchronous rectifier MOSFETs in parallel with the existing ones will result in an efficiency increase for any switching frequency.

Power transformer primary magnetizing inductance: As explained in Chapter 2, the deliberate increase of primary magnetizing current was found mandatory in order to achieve ZVT. However, this added magnetizing current increases the primary current RMS value which in turn causes additional conduction losses in the primary MOSFETs and also in the transformer primary winding. Furthermore, this added magnetizing current is not compensated by equal Ampere-turns on the secondary side and therefore, as outlined in paragraph 3.4, the resulting proximity effect and winding losses are more severe than in the case of a perfectly compensated primary current. On the other hand, keeping the

magnetizing current low will alleviate the primary conduction losses low but may also introduce turn-on losses in the primary MOSFETs which need to be quantified.

The MathCad spreadsheet which calculates efficiency based on the above considerations is shown in Appendix C. The mathematical model calculates the efficiency based on the following calculated losses:

Conduction losses in primary MOSFETs: The spreadsheet calculates the RMS value of the primary current and uses this value to calculate primary MOSFET conduction losses.

Switching losses in primary MOSFETs: Based on the switching frequency and the transformer magnetizing inductance value, the spreadsheet determines whether a full zero voltage transition is achieved on the primary side. This determination is based on the non-linear model described in Chapter 2 and in Appendix A for the ZVT CHB. If a full ZVT is achieved, then no switching losses occur in the primary MOSFETs. If not, the spreadsheet calculates the residual voltage resulting from the incomplete ZVT and calculates the MOSFET turn-on losses using equation (2.2.3) where V_{in} / 2 is replaced by the residual voltage.

Gate losses in primary MOSFETs: As discussed in paragraph 3.5, the gate to source capacitances of the primary MOSFETs are charged in a resonant fashion; therefore, the gate turn-on losses are considered negligible. Therefore, the spreadsheet calculates the gate losses incurred upon primary MOSFET turn-off.

Losses in primary capacitor bridge: Based on the RMS value of the primary current calculated above and on the ESR value of the capacitors, the spreadsheet calculates the dissipation in the input capacitors C1 and C2 (see Figure 3.1).

Conduction losses in secondary synchronous rectifier MOSFETs: These consist of two distinct contributions:

1. The losses due to MOSFET conduction.

2. The losses due to antiparallel diode conduction: during overlap intervals t_{ov1} and t_{ov2}, the voltage applied between gate and source of both synchronous rectifiers is equal to zero; thus, both synchronous rectifiers conduct through their antiparallel diodes. Therefore, the spreadsheet calculates t_{ov1} and t_{ov2} using (2.5.2) and (2.5.3) and then calculates diode conduction losses during these intervals.

Switching losses in secondary synchronous rectifier MOSFETs: These consist of:

1. Gate losses during the turn-off of the synchronous rectifiers. These result from a soft capacitive discharge due to the soft ZVT transition on the primary side. This soft capacitive discharge is represented by the falling edges of the waveforms shown on Figure 3.14.

2. Gate losses during the turn-on of the synchronous rectifiers. These result from a hard capacitive charge due to a hard transition on the secondary side. This hard capacitive charge is represented by the rising edges of the waveforms shown on Figure 3.14.

3. Reverse recovery losses associated with the synchronous rectifier antiparallel diodes.

Losses in the main power transformer: These consist of core losses and winding losses. The winding losses themselves are the sum of two distinct contributions:

1. Winding losses due to load current (compensated on the secondary side by equal Ampere-turns)

2. Winding losses due to primary magnetizing current (not reflected on the secondary side).

As explained above, the proximity effect associated with each of the two components of the primary current is quite different. The spreadsheet calculates the fundamental term and the harmonics (up to the 8th) of both the load current and the magnetizing current and then calculates winding losses using equation (3.7).

Losses in input inductors: The spreadsheet calculates the input current and then calculates the winding losses through each of the two input inductors; core losses are considered negligible.

Losses in output inductors: these mainly consist of conduction losses. Again, core losses are considered negligible.

Losses in the control circuit: The power consumption of the control circuit (excluding primary MOSFET gate drive) has been measured and found equal to 0.54 W.

The efficiency of the converter breadboard has been measured and calculated for four different values of main transformer primary inductance and for four different values of switching frequency.

The four different transformer primary inductances were obtained by introducing different spacers in the magnetic core which allowed us to vary the air gap. The values of primary inductance tried were: L_{pri} = 24.5 μH, 14.5 μH, 10.5 μH and 8.7 μH.

The switching frequency was varied from 200 kHz to 500 kHz in 100 kHz increments.

Figure 3.15 shows the measured efficiencies (solid lines) versus calculated efficiencies (dotted lines) for all the above conditions under full load (I_o = 15 A), where Q4 consists in only one MOSFET.

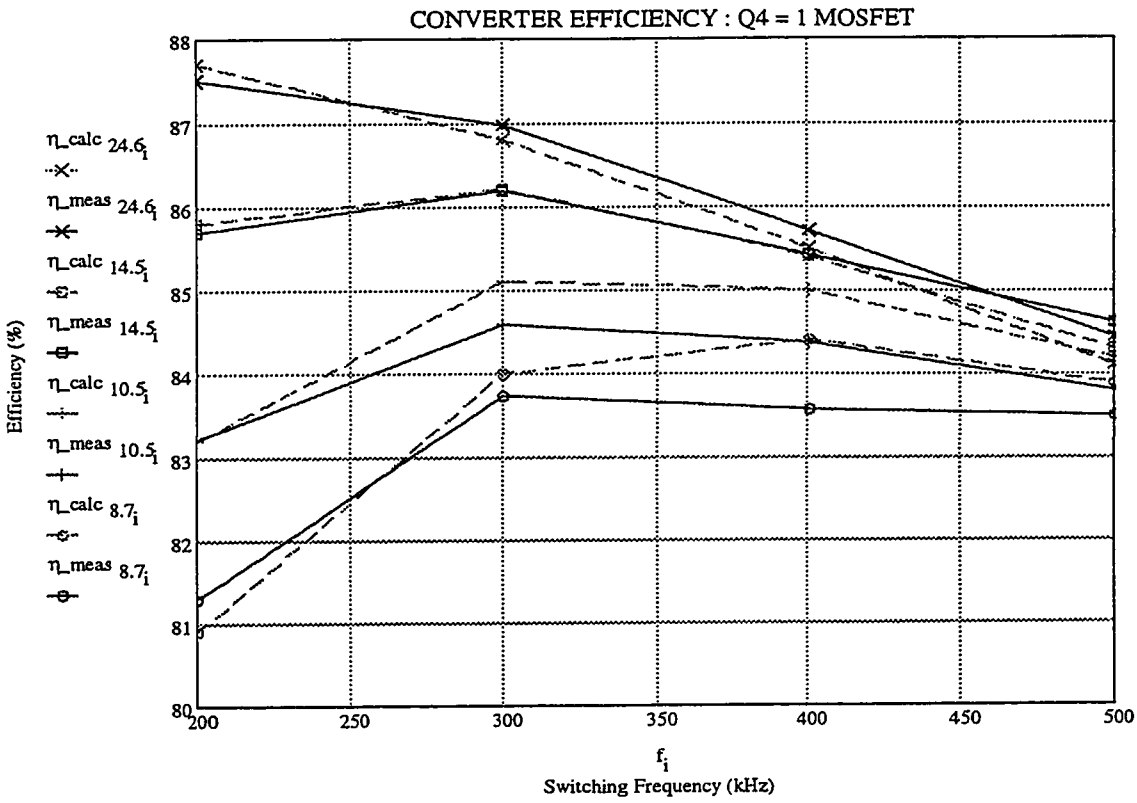


Figure 3.15 3.3 V Converter Calculated versus Measured Efficiencies when Q4 consists of only one MOSFET

Figure 3.16 shows the measured versus calculated efficiencies under the same conditions except that Q4 consists in two MOSFETs in parallel.

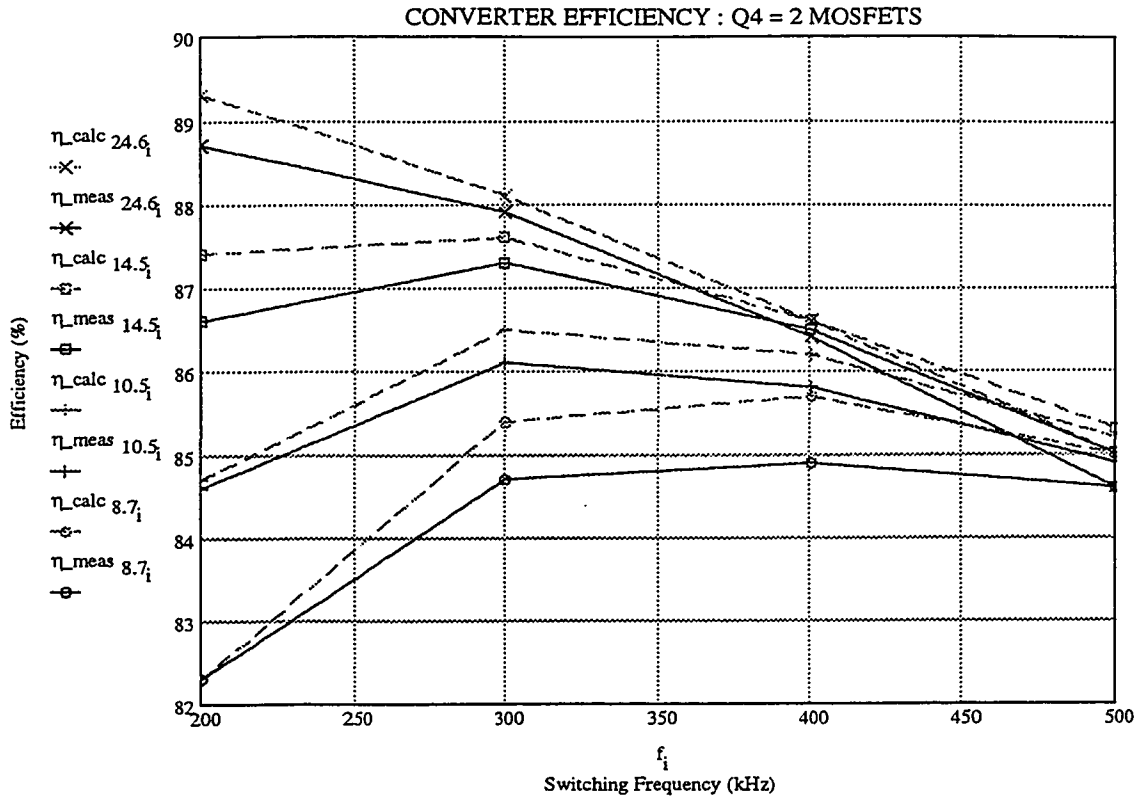


Figure 3.16 3.3 V Converter Calculated versus Measured Efficiencies when Q4 consists of two MOSFETs in parallel.

As can be seen from the above figures, the match between calculated and measured efficiencies is excellent, which validates the mathematical model.

The interpretation of the above results is best done by considering the efficiency variation over frequency for the two extreme values of primary inductance, i.e. 24.6 μH and 8.7 μH.

Referring to Figure 3.16, the top pair of curves corresponds to the calculated and measured efficiencies for a primary magnetizing inductance of 24.6 μH. The efficiency at low frequency is quite high because at that frequency, ZVT is achieved even though this value of inductance is much higher than the calculated value of 10 μH; therefore, no switching losses occur in the primary MOSFETs. All other switching losses are low due to

the low frequency of operation. The conduction losses in the primary transistors and the transformer winding losses are low because the RMS value of the primary current is low. This explains the high efficiency at low frequency.

As the frequency increases however, ZVT is no longer achieved for the primary MOSFETs because insufficient magnetizing current is built up in the primary to guarantee ZVT; as a result, turn-on losses occur in the primary MOSFETs and these losses increase rapidly with increasing frequency. This explains the relatively low efficiency at high frequency.

The bottom pair of curves corresponds to the calculated and measured efficiencies for a primary magnetizing inductance of 8.7 μH. It should be noted that this low value of magnetizing inductance always guarantees ZVT for all switching frequencies up to 500 kHz. The efficiency at low frequency is very low because the magnetizing current being built up on the primary side is very high, which causes the RMS value of the primary current to be quite high; this in turn creates high conduction losses in the primary MOSFETs as well as high transformer winding losses.

As the frequency increases, the transformer primary magnetizing current decreases, yet remains sufficient to guarantee ZVT. As a result, no increase in primary switching losses occurs. However, the primary conduction losses dramatically decrease as a result of the sharp decrease in primary current RMS value. The efficiency curve for this magnetizing inductance reaches a maximum beyond which the increase of the secondary switching losses as well as the increase of transformer winding losses due to proximity effect cause the efficiency to decrease again.

The comparison of Figure 3.15 Figure 3.16 reveals that the addition of a MOSFET in parallel with Q4 causes an increase in efficiency which goes from 1 % for a frequency of 200 kHz down to 0.3 % for a frequency of 500 kHz. This reduction in efficiency gain at

high frequencies indicates that the gain in conduction losses is partly offset by additional losses associated with parasitic capacitances charge and discharge which increase as the frequency increases.

3.8 Converter size optimization

Based on the mathematical model for efficiency described in the previous paragraph, an optimization effort was undertaken in order to determine the optimum switching frequency.

The goal of this exercise was to find the board area occupied by all the magnetics and filtering capacitors of the power circuit as a function of the switching frequency.

The height of all the magnetics was fixed to 1 cm.

The following constraints were imposed on the power circuit being studied for all switching frequencies:

- Power dissipated in the main transformer (core losses + winding losses) was forced equal to 0.5 W.
- The transformer primary magnetizing inductance value was calculated in order to just guarantee ZVT for all switching frequencies.
- The total power dissipated in the output inductors LOUT1 and LOUT2 (see Figure 3.1) was forced equal to 0.3 W.
- The total power dissipated in the input inductors LIN1 and LIN2 (see Figure 3.1) was forced equal to 0.3 W.

The double stage input filter components are calculated in order for the differential mode conducted emissions to exactly meet MIL-STD-461 CE03 specification for all switching frequencies; this specification allows a maximum input ripple current going from

74 dB above 1 μA (74 dBμA) at 15 kHz down to 45 dBμA at 500 kHz, following a log-linear decrease.

A second stage output filter, not represented on Figure 3.1 was added to the power circuit; the first and second stage output filter components are calculated in order to obtain an output voltage ripple of 10 mV peak to peak.

The power dissipated in the second stage output inductor was forced equal to 0.15 W.

The calculation details are shown in Appendix D.

The results of the optimization are shown on Figure 3.17 below.

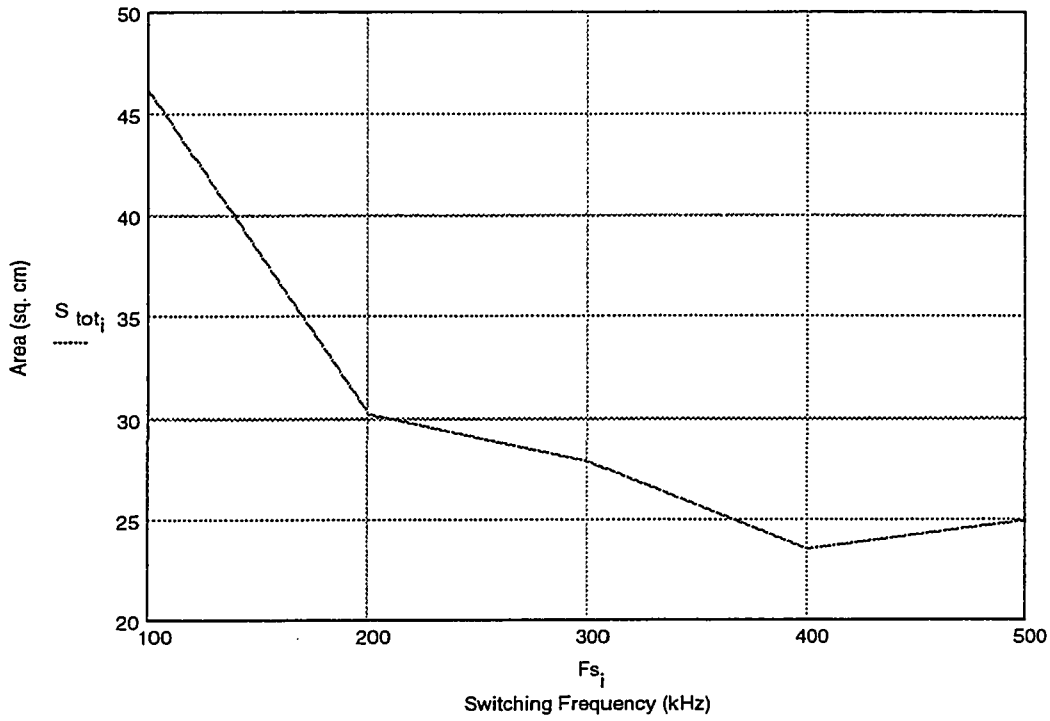


Figure 3.17 Total Area of Magnetics and capacitors versus Switching Frequency

As can be seen from Figure 3.17, the increase in switching frequency allows for a quick initial decrease in converter total area; the reasons for this decrease are the following:

At a given peak to peak input current ripple or output voltage ripple, the capacitance and inductance values in the input and output filters decrease as the frequency increases.

The magnetic core area of the main transformer which will yield a given peak flux density is inversely proportional to the switching frequency.

The total magnetics and capacitors area reaches a minimum of 24 cm^2 at a switching frequency of 400 kHz.

Beyond this frequency, the area increases again. This is easily explained considering that the winding losses in the main transformer and the core losses in all the magnetics (including the transformer) increase as the frequency increases. Eventually, a point is

reached where the magnetic core sizes and the winding cross-sections must increase in order to keep the total losses constant as imposed by the constraints described above.

3.9 Conclusions

This chapter was devoted to the design and prototyping of a 3.3 V, 50 W converter based on the circuit parameter values calculated in Chapter 2 in order to obtain ZVT on the primary side. The waveforms recorded on the breadboard are shown to be in excellent agreement with the predictions of Chapter 2. Moreover, the waveforms confirm the crucial role played by the leakage inductance during ZVT on the primary side.

A mathematical model which calculates efficiency for different switching frequencies and different primary magnetizing inductance values was developed. The measured efficiencies on the prototype are shown to be in excellent agreement with the calculated ones, using the model. At 400 kHz, typical efficiencies of 87% have been measured.

A mathematical model which calculates the size of the power magnetics and capacitors as a function of the switching frequency has been developed. Fixed constraints consistent with the efficiency and input/output ripple requirements are imposed to the model for any switching frequency. It is shown that the size of the converter sharply decreases from 100 kHz to 200 kHz and then slowly decreases until it reaches a minimum at 400 kHz. Based on this small size decrease beyond 200 kHz and also on the efficiency figures obtained before, it can be seen that there is little incentive to increase the switching frequency beyond 300 kHz.

Chapter 4
CHBC Dynamic Modelling

4.1 Introduction

Having designed and built the 3.3 V converter based on the CHB topology, it is now necessary to study the issues related to the converter regulation, both static and dynamic.

The static regulation of a converter describes its ability to maintain its DC output voltage within a given regulation band in the absence of perturbations, whereas the dynamic regulation describes its ability to respond to perturbations such as an abrupt change of the output current (step load change) or a sudden variation of the input voltage.

For this purpose, it is necessary to develop a model which accurately describes the dynamic characteristics of the converter. This model will then be used to design a proper compensation ; the purpose of this compensation is to correct the dynamic behaviour of the converter in such a manner that under all specified conditions of input voltage perturbations and output current changes, the deviations of the converter output voltage with respect to its nominal value remain within specifications.

In modelling the CHBC, we will adopt the following strategy:

1. Development of a basic averaged dynamic model
2. From the basic averaged model, develop a small signal model

3. Based on the small signal model, derive analytical expressions for the fundamental transfer functions, i.e. Control to Output and Input to Output

4. Based on the transfer functions obtained in step (3), design a suitable compensation loop such that the converter meets a defined set of requirements.

The results obtained at each of the above steps will be validated by tests before moving on to the next step.

For the purpose of the following analyses, we shall adopt the following notations:

- Quantities designated by small letters represent a variable's full value (steady state value + AC small signal variation).
- Quantities designated by capital letters refer to steady state values.
- Quantities designated by small letters topped with a " ˆ " represent small signal variations.

As an example of the above definition, the converter's duty cycle would be described by the following equation:

$$d = D + \hat{d}$$

4.2 The Basic Averaged Dynamic Model

The basic averaged model can be obtained either by the classical state space averaging technique [32] or by the switching cell averaging method [31], [34] where the averaging exercise is performed on the converter switching cell only. Both techniques lead to locally averaged state space variables (inductor currents and capacitor voltages); a locally averaged state space variable is obtained by computing the average value of a state space variable over one switching period. As demonstrated in [31] to [34], this fundamental step results in

the complete elimination from the modelization process of the ripple at the switching frequency.

Both methods rely on the fulfilment of a fundamental criterion: the dynamic variation of locally averaged state space variables must be small over any switching cycle. This implies that the poles and the zeroes of the converter considered as a dynamic system must occur at frequencies significantly lower than the switching frequency.

Each method has its own merits: the state space averaging method is a systematic approach which uses the well known formulation:

$$\dot{x} = A \cdot x + B \cdot u$$

where A, B and x are averaged over one switching period [32]. This method however is purely mathematical at this stage and does not offer an immediate circuit insight because the averaging process is performed on the entire circuit.

By contrast, the model obtained from the switching cell averaging technique is a circuit where the original switching cell (usually a combination of switching MOSFETs and switching diodes) has been replaced by the averaged switching cell, with all other circuit elements remaining unchanged. The circuit thus obtained readily lends itself to simulation. Moreover, since no small signal restriction was made thus far, this model is a large signal model which is well suited to simulate large load and line transients.

Due to these advantages, the switching cell averaging technique was chosen to develop the basic averaged model.

Figure 4.1 below shows the simplified schematic of the CHBC.

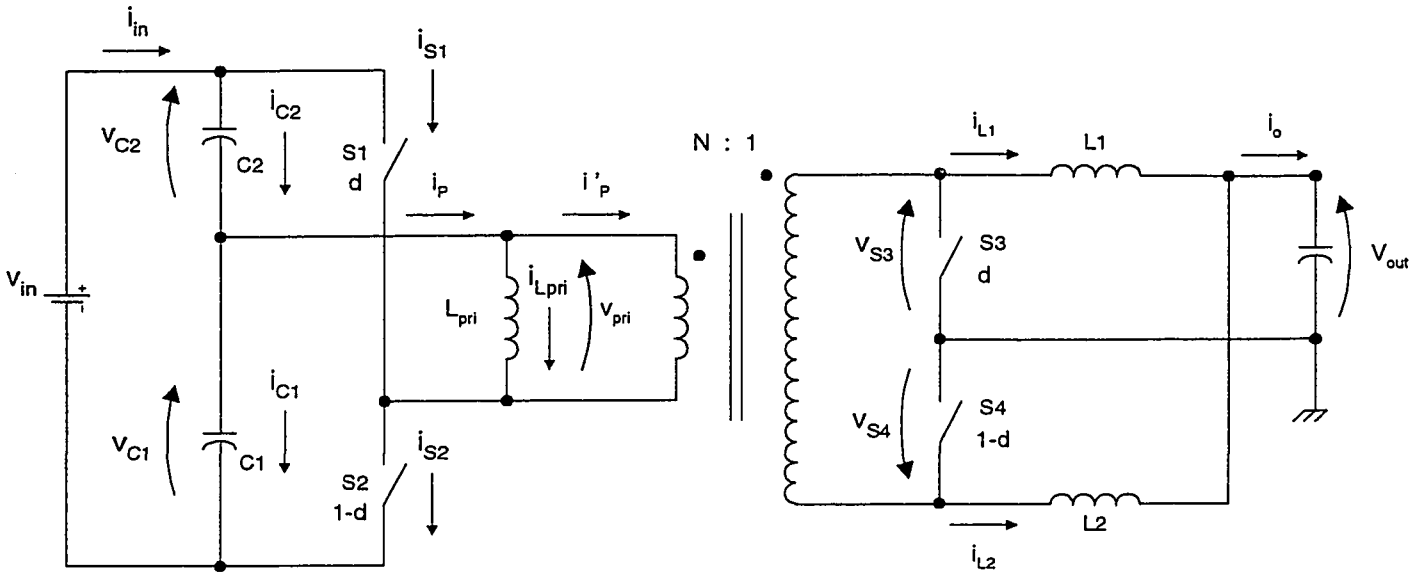


Figure 4.1 Simplified Schematic of CHBC

As can be seen from the figure, the switching cell consists of four switches S1 to S4, two of which are conducting during $d \times Ts$, the other two are conducting during $(1\text{-}d) \times Ts$. N is the transformer turns ratio which was calculated in Chapter 2. Its value is $N = 6$.

Application of the switching cell averaging principle to the above circuit results in the following equations:

Average voltage across S3

$$v_{S3} = \frac{v_{C1}}{N} \cdot (1-d) - L_{lk} \cdot \frac{i_o}{Ts} \qquad (4.2.1)$$

Average voltage across S4

$$v_{S4} = \frac{v_{C2}}{N} \cdot d - L_{lk} \cdot \frac{i_o}{Ts} \qquad (4.2.2)$$

Average current through S1

$$i_{S1} = -i_{Lpri} \cdot d + \frac{i_{L2}}{N} \cdot d \qquad (4.2.3)$$

Average current through S2

$$i_{S2} = i_{Lpri} \cdot (1-d) + \frac{i_{L1}}{N} \cdot (1-d) \qquad (4.2.4)$$

Average voltage across primary magnetizing inductance

$$v_{Lpri} = -v_{C2} \cdot d + v_{C1} \cdot (1-d) \qquad (4.2.5)$$

The above five equations are all that is strictly required to build the basic averaged circuit model. However, as will be detailed in the next paragraph, three more equations are required to develop the small signal model.

Average primary load current (excluding magnetizing current)

$$i'_P = \frac{i_{L1}}{N} \cdot (1-d) - \frac{i_{L2}}{N} \cdot d \qquad (4.2.6)$$

Average input current

$$i_{in} = i_{C2} + d \cdot (\frac{i_{L2}}{N} - i_{Lpri}) \qquad (4.2.7)$$

Average input current (alternate expression)

$$i_{in} = i_{C1} + (1-d) \cdot (\frac{i_{L1}}{N} + i_{Lpri}) \qquad (4.2.8)$$

Equations (4.2.1) and (4.2.2) contain the term: $L_{lk} \cdot i_o / Ts$. This terms is used to describe the overlap time during which the output current is transferred from one synchronous rectifier to the other. It was shown in Chapter 2 that this overlap time has the effect of reducing the effective duty cycle and hence, reduces the effective voltage applied to L1 and L2. The resulting voltage drop was calculated in Chapter 2 as $L_{lk} \cdot i_o / Ts$. Since this voltage drop is proportional to the output current, it can be modelled as a resistive drop. The value of this " overlap " resistor is simply equal to $R_{ovlp} = L_{lk} / Ts$.

Equations (4.2.1) to (4.2.5) enable us to build the basic averaged model which is shown in Figure 4.2 below. For more convenience, we introduce from this point on the inverse transformer turns ratio n, defined as $n = 1/N$.

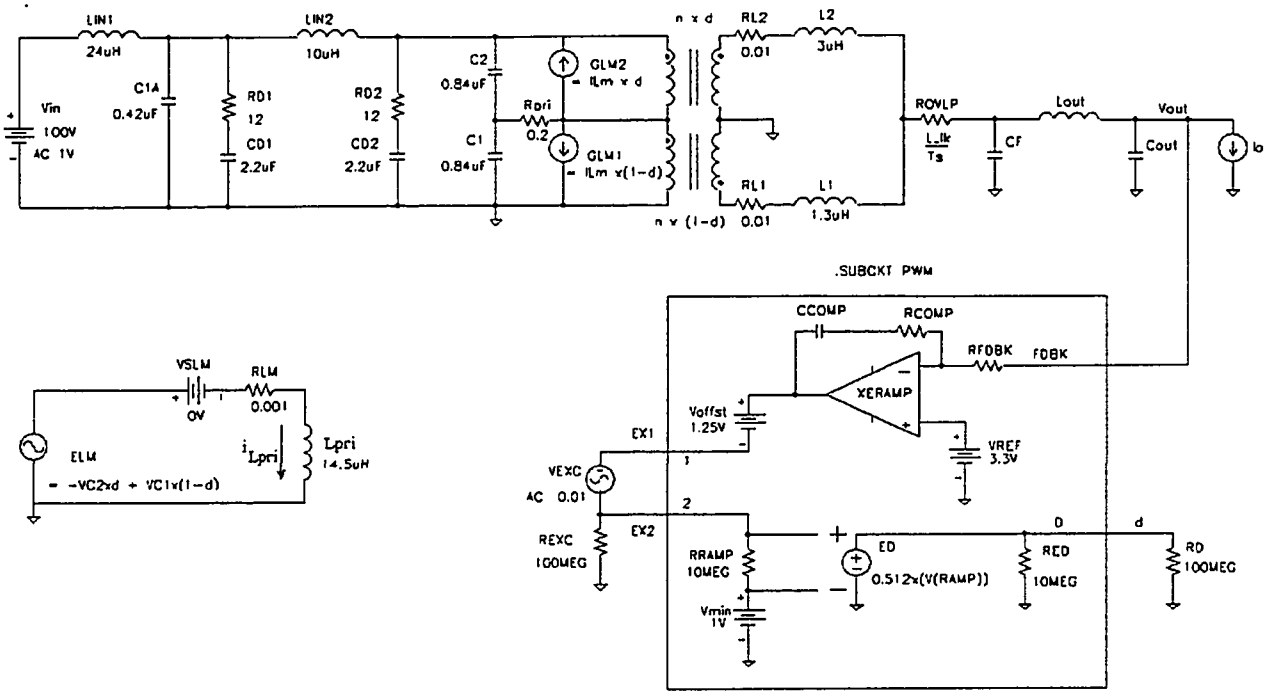


Figure 4.2 CHBC Basic Averaged Model

As can be seen from the above figure, switches S1 to S4 of Figure 4.1 have been replaced by two transformers whose turns ratios are given by $n \times d$ and $n \times (1\text{-}d)$ respectively.

The two current sources GLM1 and GLM2 represent the primary magnetizing current which is described by the first term of equations (4.2.4) and (4.2.3) respectively. From inspection of the circuit of Figure 4.2, we can see that the two transformers, along with the two current sources GLM1 and GLM2 satisfy the set of equations (4.2.1) to (4.2.4) and (4.2.6) to (4.2.8).

On the other hand, the circuit composed of voltage source ELM, current sense voltage source VSLM and primary inductance L_{pri} satisfies equation (4.2.5). The voltage defined by ELM is impressed across inductance L_{pri}. This voltage in turn creates a

magnetizing current i_{Lpri} which is then used to calculate the values of current sources GLM1 and GLM2.

In order to complete the model, all we need to do is to find a suitable representation for the duty cycle. This is accomplished by the subcircuit PWM.

In the real converter, the duty cycle definition results from the comparison between the error amplifier output (often called the control voltage v_c) and the timing ramp. The higher the control voltage, the higher the duty cycle. What we need to determine is the gain between v_c and d.

The UC1823A Pulse Width Modulator being used in the breadboard has a ramp amplitude equal to: $V_{ramp} = 1.8$ V.

The timing capacitor of 1 nF and the timing resistor of 3.8 kΩ, which were selected for 400 kHz operation yield an oscillator charge time equal to: $t_{ch} = 2.3$ μs. The discharge time equals 0.2 μs. The switching period Ts is the sum of the charge and discharge times and is equal to 2.5 μs.

The slope of the timing ramp is given by $\frac{\Delta v_c}{\Delta t} = \frac{V_{ramp}}{t_{ch}}$

But $\Delta t = Ts \cdot \Delta d$

Hence, $\frac{\Delta d}{\Delta v_c} = \frac{t_{ch}}{Ts \cdot V_{ramp}} = \frac{2.3\mu s}{2.5\mu s \cdot 1.8} = 0.512$

Referring to Figure 4.2, voltage source ED contained in the PWM subcircuit is equal to $v_c \times 0.512$ and therefore, its output voltage represents the duty cycle.

It can be seen that upon a large load or line transient, the duty cycle is dynamically calculated in accordance with the variations of the error amplifier output XERAMP. No small signal assumption is made in this model. It is therefore a large signal model.

However, since PSPICE always starts an AC simulation with a DC bias calculation and a subsequent linearization around the calculated bias point, this model can also perform small signal frequency analysis. Voltage source VEXC injects a small AC signal for the purpose of loop frequency response computation.

In PSPICE simulations, the loop frequency response is obtained by displaying the amplitude and phase of expression *V(EX2) / V(EX1)* .

In order to validate our model, two simulations were performed and then compared against test results. The first simulation computes the control to output frequency response (AC analysis). The second simulation simulates a step load change from 7.5A to 15A (Transient analysis). The simulation results, along with the actual test results are shown in Figure 4.3 to Figure 4.6.

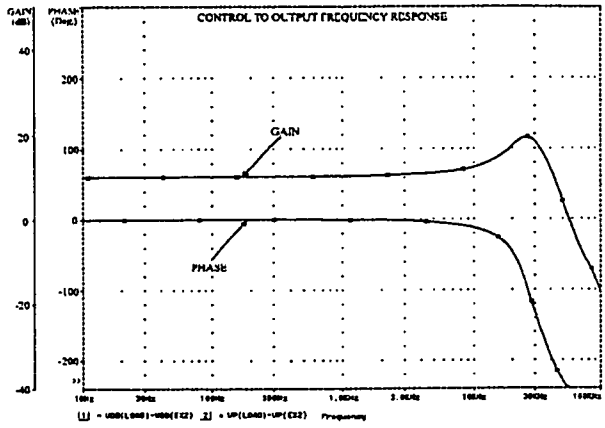


Figure 4.3 Simulated Control to Output Frequency Response

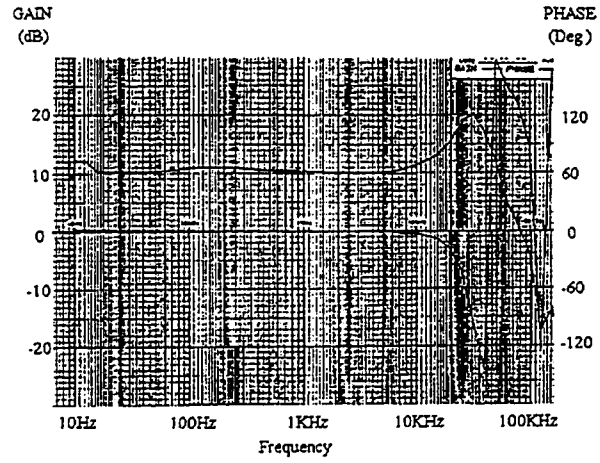


Figure 4.4 Measured Control to Output Frequency Response

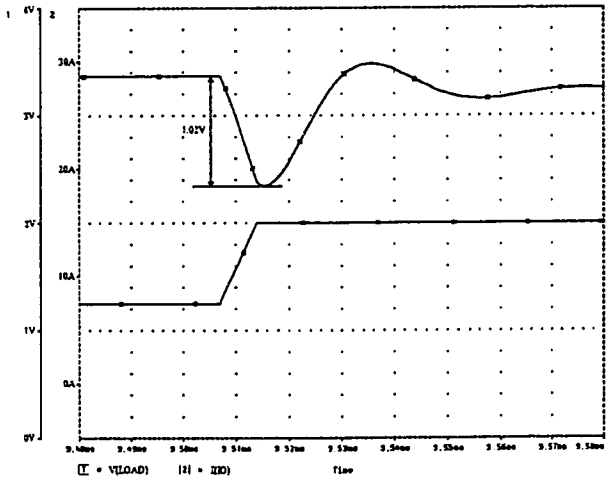


Figure 4.5 Simulated Response to a Step Load Change from 7.5A to 15A

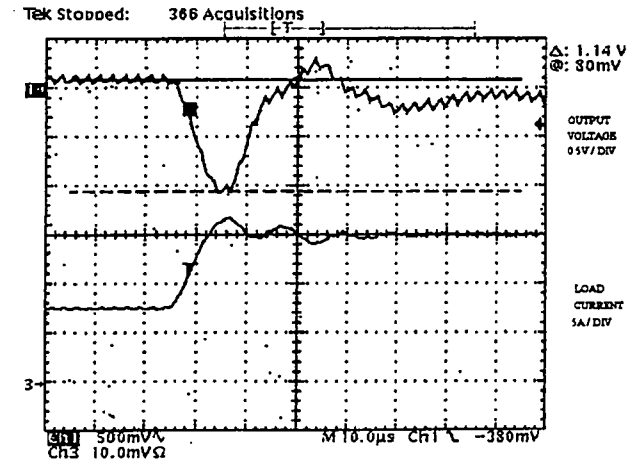


Figure 4.6 Measured Response to a Step Load Change from 7.5A to 15A

As can be seen from the above figures, excellent match exists between the simulations and the test results.

Having now validated our large signal model, we can proceed and develop the small signal model.

4.3 The Small Signal Model

The small signal model is derived from the large signal model by introducing perturbations in Equations (4.2.1) to (4.2.8) and subsequently linearizing these perturbed equations [31 to 34]. The linearization step consists in neglecting the products of perturbations, thus leaving terms containing DC quantities only or DC quantities multiplied by perturbations.

It should be pointed out that neglecting the products of perturbations can be done only if the small signal assumption is satisfied, i.e. $\hat{v} << V$.

The perturbation and linearization of (4.2.1) is carried out in the next lines.

$$V_{S3} + \hat{v}_{S3} = n \cdot (V_{C1} + \hat{v}_{C1}) \cdot (1 - D - \hat{d}) - \frac{L_{lk}}{Ts} \cdot (I_o + \hat{i}_o)$$

Neglecting the products of small signal perturbations yields the following hybrid equation:

$$V_{S3} + \hat{v}_{S3} = n \cdot V_{C1} \cdot (1 - D) - \frac{L_{lk}}{Ts} \cdot I_o + n \cdot \hat{v}_{C1} \cdot (1 - D) - n \cdot V_{C1} \cdot \hat{d} - \frac{L_{lk}}{Ts} \cdot \hat{i}_o$$

The above equation is called hybrid because it contains DC terms as well as terms containing perturbations. But if all perturbations are set to zero, the above hybrid equation reduces to the purely DC equation:

$$V_{S3} = n \cdot V_{C1} \cdot (1 - D) - \frac{L_{lk}}{Ts} \cdot I_o$$

Hence, after subtracting the DC equation from the hybrid equation and recognizing that $V_{C1} = D \cdot V_{in}$, we obtain the following linearized small signal equation:

$$\hat{v}_{S3} = n \cdot \hat{v}_{C1} \cdot (1 - D) - n \cdot D \cdot V_{in} \cdot \hat{d} - \frac{L_{lk}}{Ts} \cdot \hat{i}_o \qquad (4.3.1)$$

Applying the same procedure to equations (4.2.2) and (4.2.5) to (4.2.7) yields the following set of equations:

$$\hat{v}_{S4} = n \cdot \hat{v}_G \cdot D - n \cdot \hat{v}_{C1} \cdot D + n \cdot (1-D) \cdot V_{in} \cdot \hat{d} - \frac{L_{lk}}{Ts} \cdot \hat{i}_o \tag{4.3.2}$$

$$\hat{v}_{Lm} = \hat{v}_{C1} - \hat{v}_G \cdot D - V_{in} \cdot \hat{d} \tag{4.3.3}$$

$$\hat{i}'_P = n \cdot \hat{i}_{L1} \cdot (1-D) - n \cdot \hat{i}_{L2} \cdot D - n \cdot I_o \cdot \hat{d} \tag{4.3.4}$$

$$\hat{i}_{in} = \hat{i}_{C2} + n \cdot (1-D) \cdot I_o \cdot \hat{d} + D \cdot (n \cdot \hat{i}_{L2} - \hat{i}_{Lm}) \tag{4.3.5}$$

In the above equations, $\hat{v}_G$ represents the input voltage at the output of the input filter. At DC, we have of course $V_G = V_{in}$.

Equations (4.3.1) to (4.3.5) enable us to build the small signal model which is represented on Figure 4.7 below.

In Figure 4.7, the subcircuit PWM is the same as the one used in the large signal model of Figure 4.2 with the following modifications: the offset voltages V_{offst} and V_{min}, inherent to the actual pulse width modulator circuit and also the reference V_{ref} have been set to zero. This is consistent with the fact that in a small signal model the only relevant quantities are small signal variations and not DC quantities.

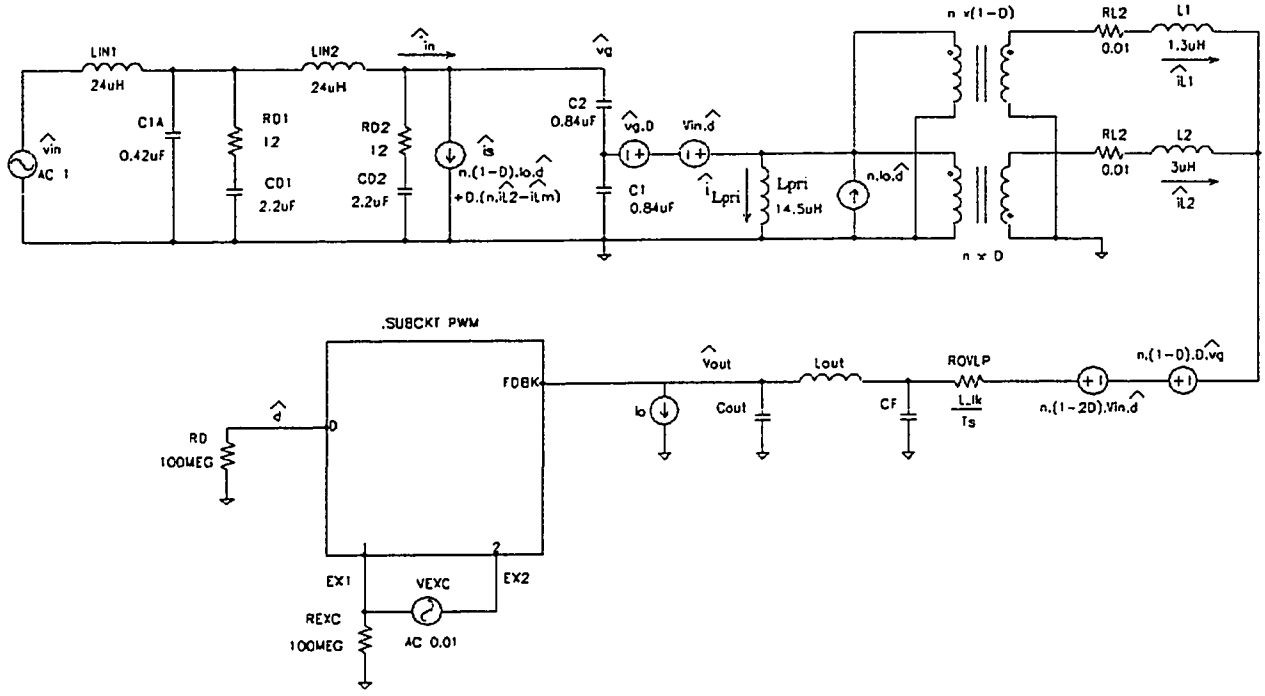


Figure 4.7 Small Signal Model of the CHBC

Comparison between Figure 4.2 and Figure 4.7 reveals that the small signal model differs from the basic averaged model (large signal model) in two respects:

The small signal model contains additional voltage and current sources whose values are proportional to the small signal perturbations. As an example, the current source $\hat{i}_s$ represents the sum of all the terms of (4.3.5) on the right hand side of $\hat{i}_{C2}$.

Several voltage and current sources as well as the DC transformer turns ratios depend on the steady state quantities I_o, V_{in} and D. This simply highlights the fact that any small signal model is only valid for one specific bias point; therefore, any significant departure from this bias point invalidates the results. As a corollary, any simulation using a small signal model requires that the bias point be defined prior to the simulation (for example through parameter statements in PSPICE).

In order to validate the small signal model just developed, two AC simulations were performed, one aimed at obtaining the control to output frequency response, the second one aimed at obtaining the line rejection. The results of the simulations were then compared to those obtained from the large signal model running under the same conditions. Both frequency responses were found identical (in amplitude and phase) to the ones obtained from the large signal model.

4.4 Derivation of the Main Transfer Functions

Having developed the small signal model, we wish to find an analytical expression for the main transfer functions; these are

$$\frac{\hat{v}_{out}}{\hat{d}} \text{ for } \hat{v}_G = 0 \qquad \text{and} \qquad \frac{\hat{v}_{out}}{\hat{v}_G} \text{ for } \hat{d} = 0$$

The first expression above represents the duty cycle to output voltage transfer function, which differs from the control to output transfer function by a factor of 0.512 as mentioned earlier. This transfer function is needed in order to close the feedback loop with appropriate gain and phase margins.

The second expression represents the input to output transfer function and is required in order to determine the ability of the converter to reject input ripple.

As mentioned earlier, $\hat{v}_G$ represents the input voltage small signal variation after the input filter; it is therefore different from $\hat{v}_{in}$ in that the converter stage has a loading effect on the input filter. It has been shown in [33] that if the incremental input impedance of the converter stage is made much larger than the input filter output impedance over the dynamic frequency range of interest, then the loading effect of the converter stage on the input filter is negligible and we can write $\hat{v}_G = \hat{v}_{in}$.

As explained in [33], one essential condition to meet in order for the above criterion to be satisfied is that the corner frequency of the input filter should never coincide with the corner frequency of the output filter. This would make the value of the input filter output impedance close to the value of the converter input impedance which in turn would defeat the above criterion.

Another fundamental criterion that any converter must satisfy is its stability in presence of an input filter. It is shown in [33] that from DC to a frequency which depends on the converter and on the control method, the incremental input impedance of a converter is negative and is equal to $\frac{-V_{in}}{I_{in}}$. If the output impedance of the unloaded input filter exceeds the absolute value of this negative impedance, then the converter becomes unstable. In our case, for a 50 W converter running at 87 % efficiency, V_{in} = 100 V and I_{in} = 0.574 A. This yields an incremental input impedance equal to –174 Ω.

We must therefore design the input filter such that its maximum unloaded input impedance is well below the absolute value of this negative impedance. If, in addition, the power stage is designed in such a way as to keep the resonant frequencies of the input filter and of the output filter well apart from one another, then the loading effect of the converter stage on the input filter can be considered negligible and therefore, $\hat{v}_G = \hat{v}_{in}$. The validity of this assumption will be verified later.

4.4.1 Input Filter Design

As can be seen from Figure 4.2 and Figure 4.7, we have deliberately chosen to make the input filter double stage, both stages consisting of *identical* elements (the series combination of the second stage capacitors C1 and C2 is equal to first stage capacitor C1A). This choice brings about the advantage of increased component commonality and hence, of fewer parts in inventory.

Figure 4.8 below shows the equivalent input filter with its two identical stages.

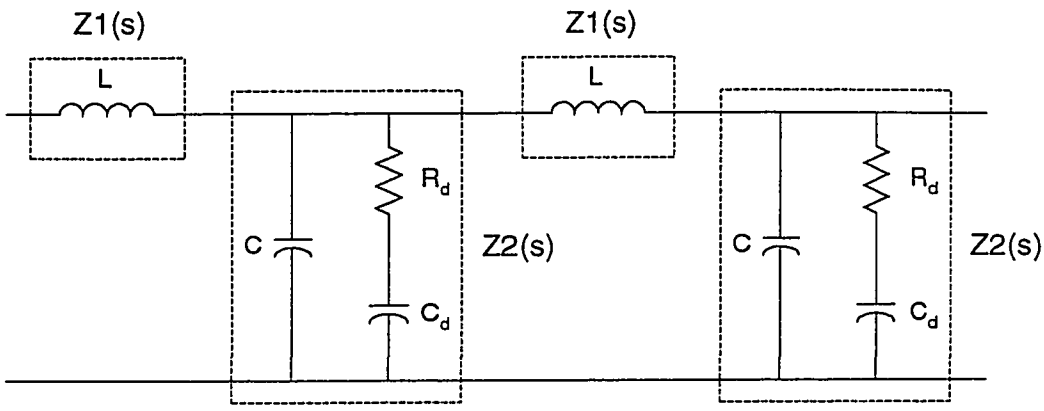


Figure 4.8 CHBC Double Stage Input Filter

Defining the series impedance of each stage as $Z1(s)$ and the parallel impedance as $Z2(s)$, it is easy to demonstrate that the filter frequency response $He(s)$ is given by

$$He(s) := \frac{1}{1 + 3\cdot\frac{Z1(s)}{Z2(s)} + \left(\frac{Z1(s)}{Z2(s)}\right)^2}$$

which can also be written as

$$He(s) := \frac{1}{\left(1 + 2.618\cdot\frac{Z1(s)}{Z2(s)}\right)\cdot\left(1 + 0.382\cdot\frac{Z1(s)}{Z2(s)}\right)} \qquad (4.4.1)$$

It can be shown that if $C_d >> C$, $He(s)$ can be approximated as

$$He(s) := \frac{1}{\left[1 + \frac{1}{Q_0}\cdot\frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right]\cdot\left[1 + \frac{1}{Q_1}\cdot\frac{s}{\omega_1} + \left(\frac{s}{\omega_1}\right)^2\right]} \qquad (4.4.2)$$

where

$$\omega_0 := \frac{1}{\sqrt{2.618 \cdot L \cdot C}} \qquad \omega_1 := \frac{1}{\sqrt{0.382 \cdot L \cdot C}}$$

$$Q_0 := \frac{R_d}{\sqrt{\frac{2.618 \cdot L}{C}}} \qquad Q_1 := 2.618 \cdot Q_0$$

For frequencies well above $\omega_1 / 2 \cdot \pi$, (4.4.2) reduces to

$$He(s) := \frac{1}{\left(\frac{s}{\omega_c}\right)^4} \tag{4.4.3}$$

where $\omega_c := \frac{1}{\sqrt{L \cdot C}}$

The attenuation provided by this double stage output filter is 80 dB/decade as expected. The equivalent corner frequency ω_c is exactly equal to $\sqrt{\omega_0 \cdot \omega_1}$.

The value of the filter capacitor C is determined by the maximum ripple current this capacitor can handle at the switching frequency; a suitable value of the capacitor is usually found by defining the maximum value of the ripple voltage across it. Since the analytical expression of the current through the capacitor at the switching frequency is known, it is then easy to calculate the capacitance value. From Appendix D, the maximum peak to peak ripple voltage across each capacitor of the half bridge was fixed to 1 V. This yielded a capacitor value of 0.96 μF. Since the capacitors of the half bridge are connected in series, the equivalent filter capacitance is equal to one half of the value found above, or C = 0.48 μF.

The value of the filtering inductor L is found by calculating the attenuation required at the switching frequency. In Appendix D, the fundamental value of the unfiltered input

current at the switching frequency (Fs = 400 kHz) was found equal to 1.038 A. From MIL-STD-461, CE03, the maximum current that can be injected into the input line at 400 kHz equals 188 μA.

Therefore, the filter must provide an attenuation at 400 kHz calculated as

$$\frac{1.038A}{188\mu A} = 5521$$

From (4.4.3) above, we have $\left(\frac{2\cdot\pi\cdot Fs}{\omega_c}\right)^4 = 5521.$

Hence, $\omega_c := 291.6\cdot 10^3$ rad/sec, and from the expression of ω_c given above, we obtain

L = 24.5 μH.

The values installed in the circuit are:

Filter inductor	:	L = 24 μH
First stage filter capacitor	:	C = 0.44 μF
Second stage filter capacitors (Half bridge capacitors)	:	C1, C2 = 0.84 μF

With the above component values, we obtain corner frequencies $\omega_0/(2\cdot\pi)$ and $\omega_1/(2\cdot\pi)$ equal to 31 kHz and 79.25 kHz respectively.

All that remains to be calculated are the values of the damping resistor R_d and the damping capacitor C_d.

From our previous discussion, the maximum unloaded output impedance of the input filter must be much smaller than 174 ohms for stability.

Referring to Figure 4.8, it is easy to show that the output impedance of the input filter when the input is shorted is given by

$$Zs(s) := 2 \cdot Z1(s) \cdot \frac{1 + 0.5 \cdot \frac{Z1(s)}{Z2(s)}}{\left(1 + 2.618 \cdot \frac{Z1(s)}{Z2(s)}\right) \cdot \left(1 + 0.382 \cdot \frac{Z1(s)}{Z2(s)}\right)}$$

In the above expression, the numerator and the second factor of the denominator are very similar; therefore, we can eliminate both terms. This will introduce a maximum error equal to 0.5 / 0.382 = 1.31 or 2.3 dB, which is pretty negligible.

The output impedance expression reduces to

$$Zs(s) := \frac{2 \cdot Z1(s)}{1 + 2.618 \cdot \frac{Z1(s)}{Z2(s)}} \tag{4.4.4}$$

Introducing again the assumption: $C_d >> C$, it can be shown that $Zs(s)$ can be approximated as

$$Zs(s) := \frac{2 \cdot L \cdot s}{1 + \frac{1}{Q_0} \cdot \frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2}. \tag{4.4.5}$$

The maximum value of the above impedance occurs at $\omega = \omega_0$ and is given by

$$Zs_{max} = 2 \cdot L \cdot \omega_0 \cdot Q_0 = 2 \cdot L \cdot \frac{1}{\sqrt{2.618 \cdot L \cdot C}} \cdot \frac{R_d}{\sqrt{\frac{2.618 \cdot L}{C}}} = \frac{2 \cdot R_d}{2.618}. \tag{4.4.6}$$

Choose $Zs_{max} := 10\ \Omega$; therefore, from (4.4.6), $R_d := Zs_{max} \cdot \frac{2.618}{2}$ or $R_d = 13.09$

The value actually installed in the circuit is: $R_d := 12\ \Omega$.

The damping capacitor C_d is calculated such that the damping branch $R_d - C_d$ becomes resistive at a frequency equal to one fifth of ω_0.

This yields $C_d = 2.14 \cdot 10^{-6}$.

The value actually installed in the circuit is $C_d = 2.2\ \mu F$.

Figure 4.9 and Figure 4.10 show the simulated input filter frequency response and output impedance respectively. As can be seen from Figure 4.9, the filter provides an attenuation of 72.2 dB at 400 kHz, or an attenuation factor of 4087. This is slightly below the target number of 5521 calculated above only because the components actually used in the filter are slightly below the calculated values. The filter's response decays at a rate of 80 dB per decade, as expected.

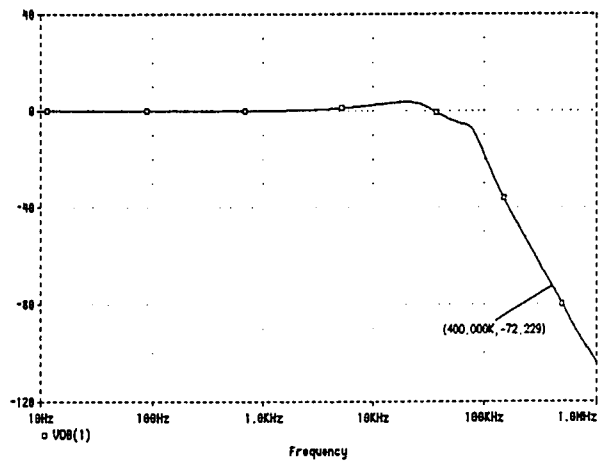


Figure 4.9 Input Filter Frequency Response

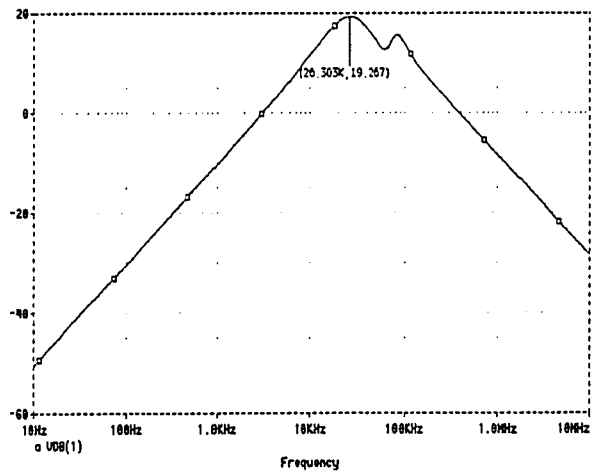


Figure 4.10 Input Filter Output Impedance

Referring to Figure 4.10, the maximum output impedance is equal to 20 dBΩ or 10 Ω, which confirms our earlier calculations. This maximum impedance occurs at

26.3 kHz, close to $\omega_0/(2\cdot\pi) = 31\,\text{kHz}$ calculated above, which confirms (4.4.5). The output impedance exhibits a second peak at 83.2 kHz, close to $\omega_1/(2\cdot\pi) = 79.25\,\text{kHz}$ calculated above. This second peak frequency does not appear in (4.4.5) because of the simplification introduced earlier. However, it can be seen that the error introduced is negligible, as predicted. The maximum input filter output impedance is much lower than 174 Ω which allows us to neglect the effect of the input filter in the subsequent calculations.

4.4.2 Main Transfer Functions

For more convenience, in all the subsequent developments, the input to output transfer function: $\frac{\hat{v}_{out}}{\hat{v}_G}$ for $\hat{d} = 0$ will be designated as $F(s)$ and the control to output transfer function: $\frac{\hat{v}_{out}}{\hat{d}}$ for $\hat{v}_G = 0$ will be designated as $G(s)$.

The main transfer functions can easily be derived from the small signal model developed earlier where, based on the above discussion, we have neglected the effects of the input filter.

For the input to output transfer function, we obtain

$$F(s) := n\cdot D\cdot(1 - D)\cdot\frac{1 + \frac{1}{Q_{z1}}\cdot\frac{s}{\omega_{z1}} + \frac{s^2}{\omega_{z1}^2}}{\left(\frac{s^2}{\omega_{p2}^2} + \frac{1}{Q_{p2}}\cdot\frac{s}{\omega_{p2}} + 1\right)\cdot\left(\frac{s^2}{\omega_{p3}^2} + \frac{1}{Q_{p3}}\cdot\frac{s}{\omega_{p3}} + 1\right)}\cdot He(s) \qquad (4.4.7)$$

where $He(s)$ is the transfer function of the input filter whose expression is given by (4.4.2),

$$\omega_{p2} := \frac{1}{\sqrt{\frac{L_{pri}\cdot(L1 + L2)\cdot(C1 + C2)}{n^2\cdot L_{pri} + L1 + L2}}}$$

$$Q_{p2} := (C1 + C2)\cdot R_{damp}\cdot\omega_{p2}$$

$$\omega_{p3} := \frac{1}{\sqrt{\left(\frac{L1\cdot L2}{L1 + L2} + L_{out}\right)\cdot C_o}}$$

$$Q_{p3} := \frac{1}{\frac{L_{lk}}{Ts}\cdot C_o\cdot\omega_{p3}}$$

$$\omega_{z1} := \frac{1}{\sqrt{\frac{D\cdot L1\cdot C1 + (1 - D)\cdot L2\cdot C2}{\left(n^2\cdot L_{pri} + L1 + L2\right)\cdot D\cdot(1 - D)}\cdot L_{pri}}}$$

$$Q_{z1} := 2\cdot R_{damp}\cdot\omega_{z1}\cdot\frac{C1\cdot C2}{C1 + C2}$$

C_o is the total output capacitance; referring to Figure 4.7, it is the sum of the first stage and second stage capacitors C_F and C_{out} respectively.

L_{out} is the second stage output inductor (usually much smaller than $L1$ and $L2$).

Equation (4.4.7) reveals that F(s) has four pairs of poles. The first two pairs are located at ω_0 and ω_1; these are the poles of the input filter transfer function $He(s)$. The third pair of poles is given by ω_{p2}. As can be seen from the expression of ω_{p2} and from Figure 4.1 , this pair of poles represents the resonance frequency of the L-C tank composed of the half bridge capacitors C1 and C2 and of the parallel combination of transformer

magnetizing inductance L_{pri} on one hand and output inductors L1 and L2 connected in series and reflected to the primary side on the other hand.

Q_{p2} represents the quality coefficient of the L-C tank; if no deliberate damping is provided ($R_{damp} = \infty$), its value is expected to be quite high.

The fourth and last pair of poles is given by ω_{p3} . Again, from the expression of ω_{p3} and from Figure 4.1, this pair of poles represents the resonance frequency of the output filter where the two output inductors L1 and L2 are effectively connected in parallel.

Q_{p3} represents the quality coefficient of the equivalent output filter; as shown by its expression, some damping is provided by the "overlap resistance" L_{lk}/Ts which is effectively connected in series with the equivalent output inductance: $L1 \cdot L2/(L1 + L2) + L_{out}$.

From (4.4.7), F(s) also has a pair of zeroes given by ω_{z1}.

Q_{z1} is the quality coefficient of the pair of zeroes; if no deliberate damping is provided ($R_{damp} = \infty$), its value is expected to be quite high.

The DC value of $F(s)$ equals $n \cdot D \cdot (1 - D)$ and is exactly the steady state input to output relationship, as expected.

For the control to output transfer function, we obtain

$$G(s) := n \cdot (1 - 2 \cdot D) \cdot V_{in} \cdot \frac{\dfrac{s^2}{\omega_{z2}^{\,2}} + \dfrac{1}{Q_{z2}} \cdot \dfrac{s}{\omega_{z2}} + 1}{\left(\dfrac{s^2}{\omega_{p2}^{\,2}} + \dfrac{1}{Q_{p2}} \cdot \dfrac{s}{\omega_{p2}} + 1\right) \cdot \left(\dfrac{s^2}{\omega_{p3}^{\,2}} + \dfrac{1}{Q_{p3}} \cdot \dfrac{s}{\omega_{p3}} + 1\right)} \qquad (4.4.8)$$

where ω_{p2}, ω_{p3}, Q_{p2} and Q_{p3} are defined above and

$$\omega_{z2} := \frac{1}{\sqrt{(C1 + C2)\cdot L_{pri}\cdot\frac{(1 - D)\cdot L1 - D\cdot L2}{\left(n^2\cdot L_{pri} + L1 + L2\right)\cdot(1 - 2\cdot D)}}}$$

$$Q_{z2} := \frac{1}{n\cdot\frac{I_o}{V_{in}}\cdot L_{pri}\cdot\frac{(1 - D)\cdot L2 - D\cdot L1}{\left(n^2\cdot L_{pri} + L1 + L2\right)\cdot(1 - 2\cdot D)}\cdot\omega_{z2}}$$

Referring to Chapter 3, the values of $L1$ and $L2$ were chosen in order to satisfy the relationship $(1-D)\cdot L1 = D\cdot L2$. It was shown that this would provide cancellation of the output current ripple. As a result, the pair of zeroes ω_{z2} occurs at a very high frequency and we can rewrite (4.4.8) as follows:

$$G(s) := \frac{n\cdot(1 - 2\cdot D)\cdot V_{in}}{\left(\frac{s^2}{\omega_{p2}^2} + \frac{1}{Q_{p2}}\cdot\frac{s}{\omega_{p2}} + 1\right)\cdot\left(\frac{s^2}{\omega_{p3}^2} + \frac{1}{Q_{p3}}\cdot\frac{s}{\omega_{p3}} + 1\right)} \qquad (4.4.9)$$

This differs from the results obtained in [4] where the presence of only one output inductor causes the pair of zeroes ω_{z2} to be located at a frequency close to ω_{p2}.

It should be noted that if we make L1 equal to L2, then the values of the poles and zeroes obtained from (4.4.7) and (4.4.8) are identical to those obtained in [4].

At DC, the above expression reduces to $n\cdot(1-2\cdot D)\cdot V_{in}$, quite consistent with the fact that the control loop gain of this topology at 50 % duty cycle reduces to zero.

With the original values of components, we obtain the following values for the corner frequencies:

$$f_{p2} = \frac{\omega_{p2}}{2\cdot\pi} = 33.7\,\text{kHz} \quad \text{and} \quad f_{p3} = \frac{\omega_{p3}}{2\cdot\pi} = 29.4\,\text{kHz}$$

This confirms the peaking in the control to output frequency response occuring at approximately 30 kHz as observed on Figure 4.3 and Figure 4.4. As can be seen on both figures, the phase of the control to output response decreases well below –180 °, which confirms the existence of a fourth order system.

It will be shown in the next paragraph that having corner frequencies f_{p2} and f_{p3} close one to another is not a good choice.

4.5 Compensation Loop Design

As highlighted at the beginning of this chapter, the converter compensation and hence, its loop gain is dictated by a specified set of performances for the converter.

This set of performances is defined as follows:

1. Load and Line regulation: ±1 %
2. Maximum undershoot (overshoot) resulting from a step load change from half load to full load: 5 % of nominal input voltage.
3. Maximum recovery time following a step load change from half load to full load: 200 µs
4. Maximum output ripple voltage resulting from input ripple: 10 mV pk

The first requirement is a steady state one and simply means that the compensation must provide a very high loop gain at low frequencies in order to preclude any permanent error.

The second and third requirements involve the converter output impedance. If the converter operates in open loop, the converter output impedance reduces to the impedance of the output filter as seen from its output [33]. Its expression is given by

$$Zo(s) := \frac{s \cdot L_{eff}}{1 + C_o \cdot L_{eff} s^2}, \tag{4.5.1}$$

where C_o represents the total output capacitance; referring to Figure 4.7, this total output capacitance is the sum of the first and second stage output capacitors C_F and C_{out} respectively.

L_{eff} represents the effective output inductance; it has been shown in the previous paragraph that this effective output inductance is given by $L_{eff} := \frac{L1 \cdot L2}{L1 + L2} + L_{out}$, which highlights the fact that the two output inductors $L1$ and $L2$ are effectively connected in parallel. It should be noted that the damping effect created by the "overlap resistance" has been neglected.

The application of an output current abrupt change of amplitude ΔI to the output filter will result in an output voltage oscillation whose amplitude is given by $\Delta V := \Delta I \cdot \sqrt{\frac{L_{eff}}{C_o}}$ and whose frequency is given by $\frac{\omega_{p3}}{2 \cdot \pi}$, where ωp3 has been defined above.

The specified step load change brings the output current from half load to full load.

Hence, we have: $\Delta I = 7.5$ A.

The current values of the output filter components are

$L1 = 1.3\mu H$, $L2 = 3\mu H$, $C_o = 31.2\mu F$ and $L_{out} = 0$.

Using the above values, we obtain ΔV equal to 1.28 V, and an oscillation half period equal to 16.7 μs; both these results are confirmed by the simulated and measured waveforms of Figure 4.5 and Figure 4.6 respectively.

From requirement # 2, the maximum allowed undershoot equals 5 % of the output voltage or 0.165 V. Our calculated and measured ΔV exceeds by much the maximum allowed value, which in turn requires a proper compensation.

From classical control theory, we know that the converter closed loop output impedance is given by

$$Zo_{cl}(s) := \frac{Zo(s)}{1 + T(s)} \tag{4.5.2}$$

where $T(s)$ represents the loop frequency response.

We target a closed loop phase margin of 90 °. Therefore, it is desirable to have a loop frequency response that, at least near the cross-over frequency (the frequency for which $|T(s)| = 1$), takes the form:

$$T(s) := \frac{A}{s} \tag{4.5.3}$$

In order to reduce our voltage undershoot ΔV from 1.28 V down to 0.165 V, the loop $T(s)$ must provide a gain at $s = \omega_{p3}$ approximately equal to $1.28/0.165 = 7.76$.

From the above expression of $T(s)$, this means that the 0 dB loop cross-over frequency must be equal to

$$f_c := \frac{\omega_{p3}}{2 \cdot \pi} \cdot 7.76 \qquad \text{or} \qquad f_c = 232 \text{ kHz}$$

The above situation is hopeless for two reasons:

1. The required cross-over frequency is too close to the switching frequency and is beyond the capabilities of any practical wide gain-bandwidth error amplifier.

2. The converter loop transfer function $T(s)$ is the product of the forward transfer function $G(s)$ whose expression is given in (4.4.9) and of the compensation transfer function $C(s)$. As shown in expression (4.4.9), $G(s)$ is a fourth order system whose poles f_{p2} and f_{p3} were calculated earlier and were shown to both lie around 30 kHz. This means that at f_c = 232 kHz, $G(s)$ has a phase lag of –360 °. In order for the overall loop transfer function $T(s)$ to provide a phase margin of 90 °, the compensation transfer function $C(s)$ would need to provide a phase boost of 270 ° at 232 kHz, which is also impossible.

The above situation was described in [4] where the solution proposed by the authors was to decrease f_{p2}; from the expression of ω_{p2} given above, this implies either making half bridge capacitors C1 and C2 much larger or making the transformer magnetizing inductance much larger, or both.

Half bridge capacitors C1 and C2 are located on the primary side; therefore, they are rated at 100 V minimum and thus, increasing their value would be detrimental to the overall converter size, mass and cost. Increasing the transformer magnetizing inductance is also impractical since it was shown in Chapters 2 and 3 that it played an important role in achieving ZVT. In addition, increasing the inductance also has the effect of increasing the DC flux density in the transformer as was demonstrated in paragraph 3.4. Thus, increasing the inductance might lead to transformer saturation.

The solution proposed here is rather to decrease f_{p3}, by substantially increasing the output capacitance. This solution was found realistic and economical for two reasons:

1. In typical digital applications requiring a 3.3 V converter delivering 50 W, the load capacitance can be as high as 300 µF. Since the converter must

accommodate a wide range of load capacitances, it is logical to increase its intrinsic output capacitance to 300 μF, in order to match the maximum load capacitance.

2. The output capacitors only have to support 3.3 V, and therefore, are low voltage capacitors. Therefore, increasing their value is economical, both from a cost and size point of view.

The output capacitance was increased to 612 μF (9 × 68 μF), which includes 300 μF of load capacitance. Only the second stage filter capacitance C_{out} was increased; the first stage filter capacitance C_F was left unchanged at 1.2 μF, in accordance with the recommendations of [35].

The second stage filter inductance L_{out} was made equal to 100 nH.

It was mentioned earlier that the pair of poles occurring at ω_{p2} were poorly damped.

It is therefore desirable to remedy to this situation, otherwise the peaking in $G(s)$ gain occurring at ω_{p2} could compromise stability.

The input filter second stage damping network was split as shown in Figure 4.11 and the mid point created was connected to the C1 , C2 capacitive divider mid point.

Assuming that the effective damping capacitance is much larger than C1 + C2, the effective damping resistance of the primary L - C tank is now equal to the two resistances $R_d / 2$ in parallel, hence,

$$R_{damp} := \frac{R_d}{4}$$

The value of R_d was calculated in paragraph 4.4.1; we had obtained: R_d = 12 Ω.

Hence, R_{damp} = 3 Ω.

From the expression of Q_{p2} defined above with $R_{damp} = 3\ \Omega$, we obtain

$Q_{p2} = 1.068$, which is quite acceptable.

As will be shown later, this reduction in peaking at $f = f_{p2}$ is also beneficial to the line rejection.

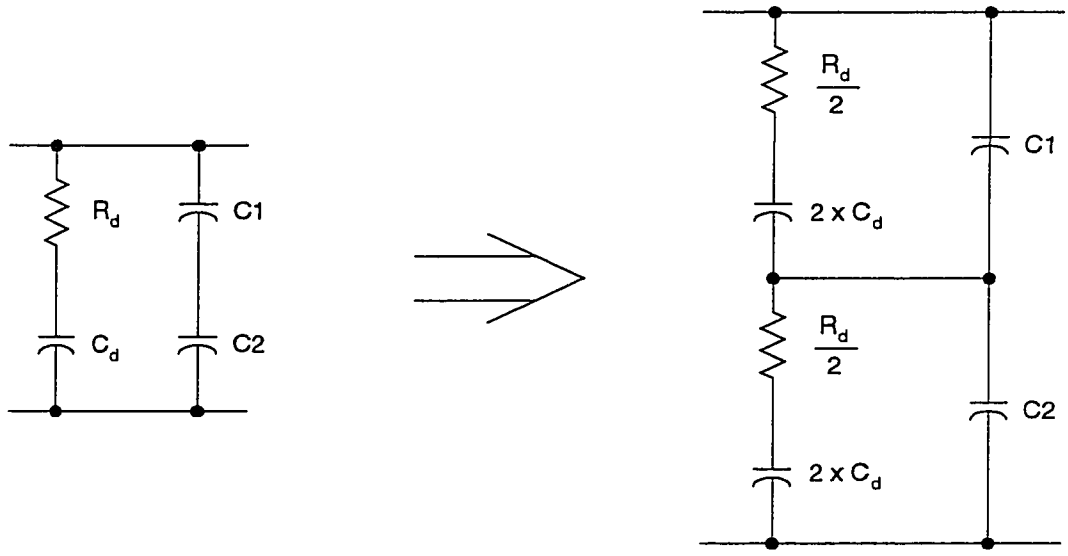


Figure 4.11 Modified Second Stage Input Filter

With the new value of C_{out}, the amplitude of the open loop output voltage undershoot under a step load change of 7.5 A becomes

$$\Delta V := \Delta I \cdot \sqrt{\frac{L_{eff}}{C_o}} \qquad \text{or} \qquad \Delta V = 0.304\ \text{V}$$

The oscillation frequency f_{p3} is now equal to

$$f_{p3} := \frac{1}{2 \cdot \pi \cdot \sqrt{L_{eff} C_o}} \qquad \text{or} \qquad f_{p3} = 6.4\ \text{kHz}$$

The output voltage undershoot still requires an attenuation whose value is equal to

$$0.304/0.165 = 1.842$$

The desired attenuation must occur at the oscillation frequency f_{p3} whose value is now much lower than before.

From the closed loop output impedance whose expression is given in (4.5.2), we can write the closed loop output voltage undershoot upon a step load change ΔI.

$$\Delta V_{cl} := \frac{\Delta V}{1 + T(s)} \tag{4.5.4}$$

Hence,

$$\left|\frac{\Delta V_{cl}}{\Delta V}\right| = \left|1 + T\left(j\omega_{p3}\right)\right| = 1.842 \tag{4.5.5}$$

$$\omega_{p3} := 2\cdot\pi\cdot f_{p3} \qquad \omega_{p3} = 4.024\cdot 10^4$$

Let's introduce the expression (4.5.3) of $T(s)$ into (4.5.5); we obtain

$$\left|1 + T\left(j\omega_{p3}\right)\right| = \left|1 + \frac{A}{j\omega_{p3}}\right| = \sqrt{1 + \left(\frac{A}{\omega_{p3}}\right)^2} = 1.842 \tag{4.5.6}$$

Solving the above equation for A yields $A = 62248$

From expression (4.5.3) of $T(s)$ again, and with the value of A calculated above, we can now calculate the the desired loop cross-over frequency:

$$f_c := \frac{A}{2\cdot\pi} \qquad f_c = 9907.8 \text{ Hz}$$

The loop frequency response $T(s)$ is the product of the control to output frequency response $G(s)$ and of the compensation $C(s)$.

At $f = f_c = 10$ kHz, the phase of $G(s)$ is approaching –180 degrees because $f_c > f_{p3}$; therefore, in order to obtain a phase margin of 90 degrees, $C(s)$ must provide a phase boost of 90 degrees at 10 kHz. This means that $C(s)$ must ideally have a slope of 20 dB / decade at $f = 10$ kHz.

The small signal model was simulated after the modifications described earlier were implemented. Figure 4.12 shows the resulting control to output frequency response, along with the desired compensation asymptotic plot.

As can be seen from the figure, $G(s)$ has a gain of 5.7 B at 10 kHz. Therefore, in order for the loop cross-over to occur at 10 kHz, the compensation $C(s)$ must have a gain of –5.7 dB at 10 kHz.

This is achieved by placing a pole of $C(s)$ at exactly 10 kHz and providing a plateau gain of -2.7 dB. The gain of $C(s)$ at 10 kHz is then 3 dB below the plateau gain or –5.7 dB.

The asymptotic diagram of $C(s)$ shows that it will provide a phase boost of 45 degrees at 10 kHz. Since the phase of $G(s)$ at the same frequency equals –133 degrees, the overall loop $T(s)$ will have a phase margin of 90 degrees at 10 kHz.

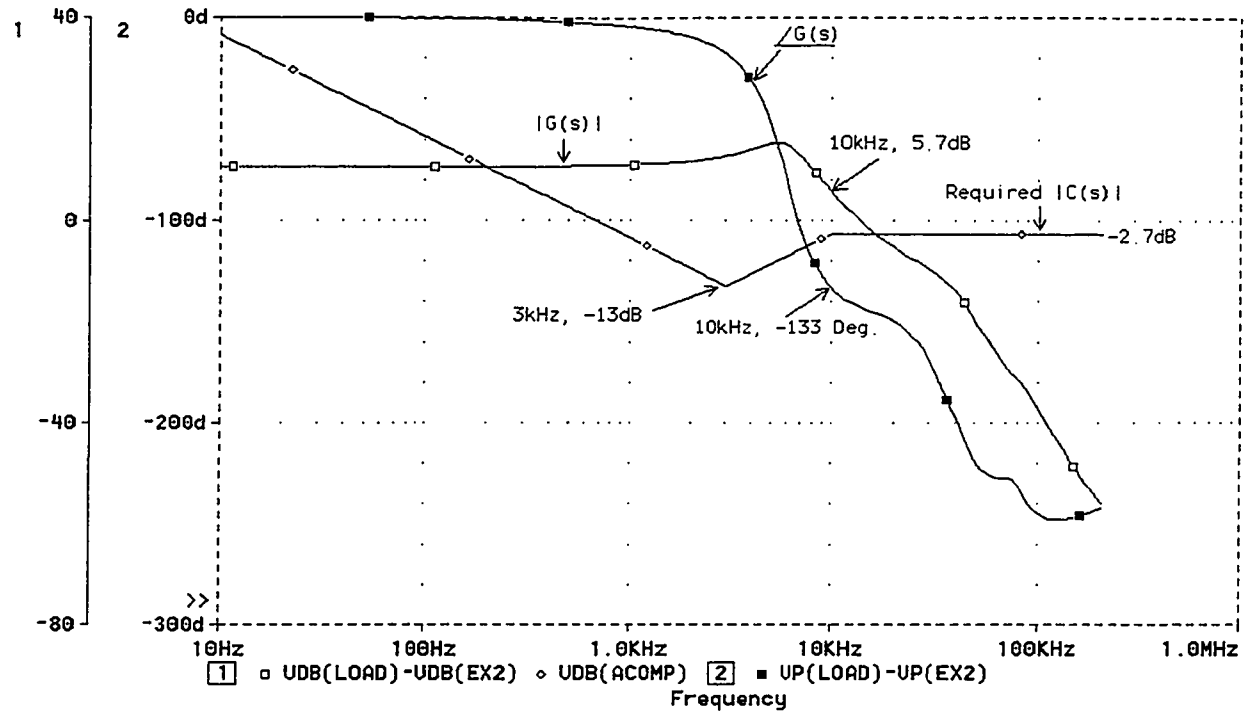


Figure 4.12 Control to Output Response with Required Compensation

The actual implementation of the compensation described above is shown in Figure 4.13.

The transfer function of the compensation is given by (the effect of capacitor C2 has been neglected)

$$C(s) = \frac{1}{s\cdot(R1 + R2)\cdot C3}\cdot\frac{(1 + s\cdot R1\cdot C1)\cdot(1 + s\cdot R3\cdot C3)}{1 + s\cdot C1\cdot\dfrac{R1\cdot R2}{R1 + R2}} \qquad (4.5.7)$$

At low frequencies, $C(s)$ is an integrator whose transfer function reduces to $\dfrac{1}{s\cdot(R1 + R2)\cdot C3}$.

At high frequencies, $C(s)$ reduces to $\frac{R3}{R2}$; from the values of R3 and R2 shown on Figure 4.13, the high frequency gain equals 0.75 or –2.5 dB, close to the target value of –2.7 dB.

It can be seen from (4.5.7) that $C(s)$ has a pair of zeroes at

$\frac{1}{2 \cdot \pi \cdot R1 \cdot C1} = \frac{1}{2 \cdot \pi \cdot R3 \cdot C3} = 3$ kHz, and a pole at $\frac{1}{2 \cdot \pi \cdot C1 \cdot \frac{R1 \cdot R2}{R1 + R2}} = 10$ kHz, as per our asymptotic diagram of Figure 4.12.

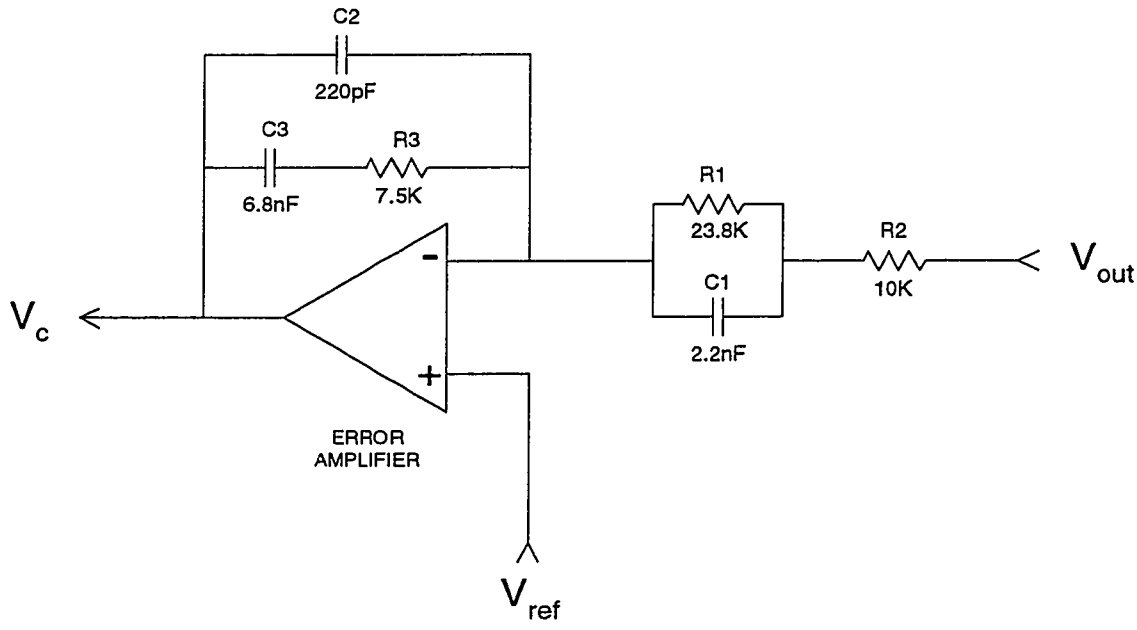


Figure 4.13 Compensation Schematic

It should be noted that the output of the error amplifier is the control voltage, which, when compared to the timing ramp, defines the duty cycle.

With the above compensation implemented, the loop frequency response was simulated using the small signal model and measured on the actual prototype. The results are shown on Figure 4.14.

As can be seen from the figure, the match between the simulation and the measurement is excellent.

The loop has a cross-over frequency of 10 kHz as expected, with a phase margin of approximately 50 degrees and a gain margin of 14 dB.

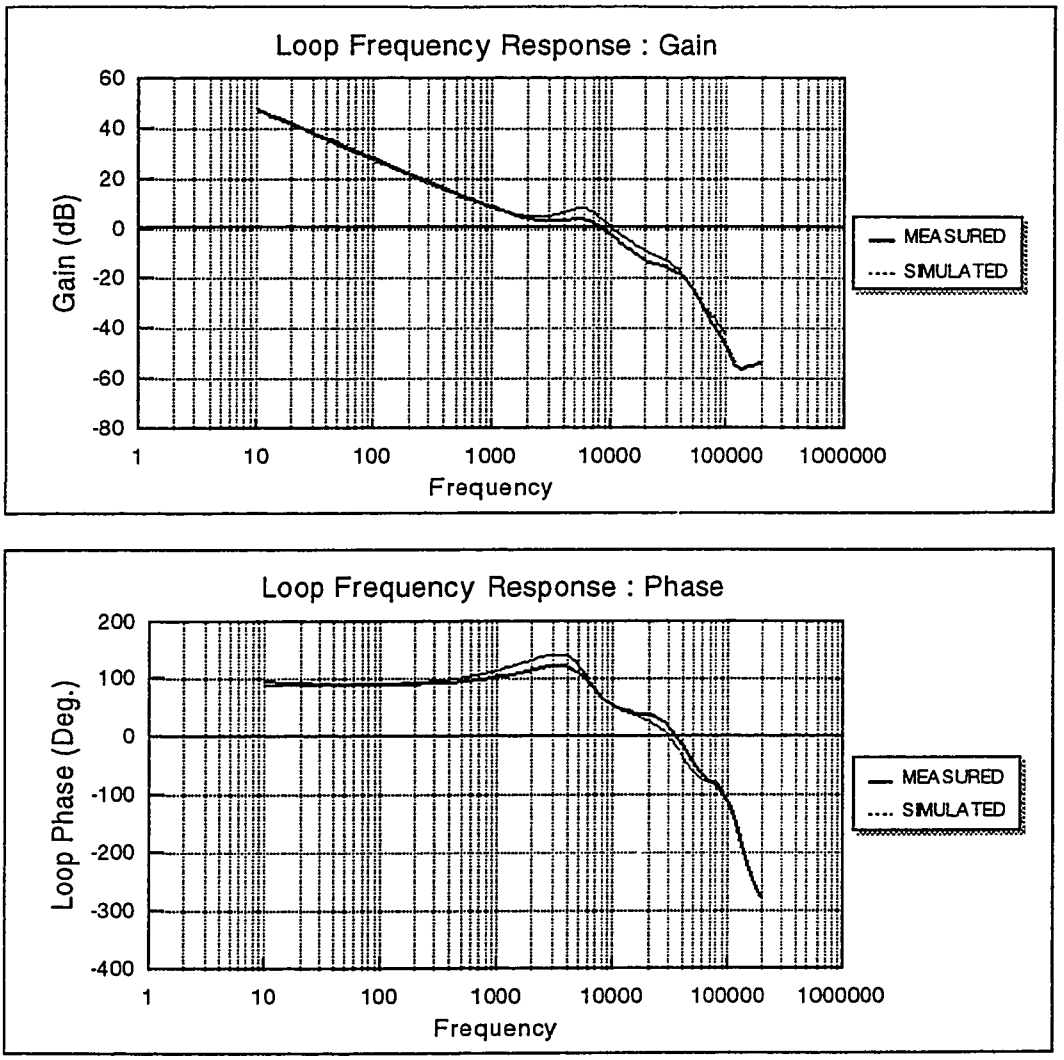


Figure 4.14 Simulated and Measured Loop Frequency Response

With the above compensation, the converter was submitted to a step load change from 7.5 A to 15 A.

The step load change was simulated using the large signal model and measured on the actual prototype. For the simulation, the large signal model was preferred over the small signal model because of the large amplitude of the transient involved.

The simulated and measured results are shown on Figure 4.15 and Figure 4.16 respectively.

Again, the match between the simulation and the measurement is excellent.

The amplitude of the output voltage transient was found equal to 0.2 V, slightly above our target value of 0.165 V.

This is due to the fact that our loop transfer function $T(s)$ was not exactly implemented as in (4.5.3); in particular, the phase margin is 50 degrees, rather than the targeted 90 degrees. This will cause the transient voltage amplitude to be slightly different from the value predicted by equations (4.5.5) and (4.5.6).

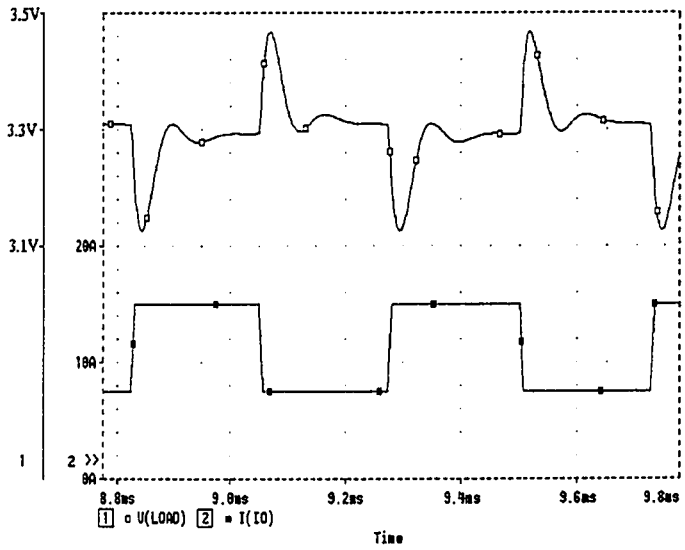


Figure 4.15 **Simulated Step Load Change Transient**

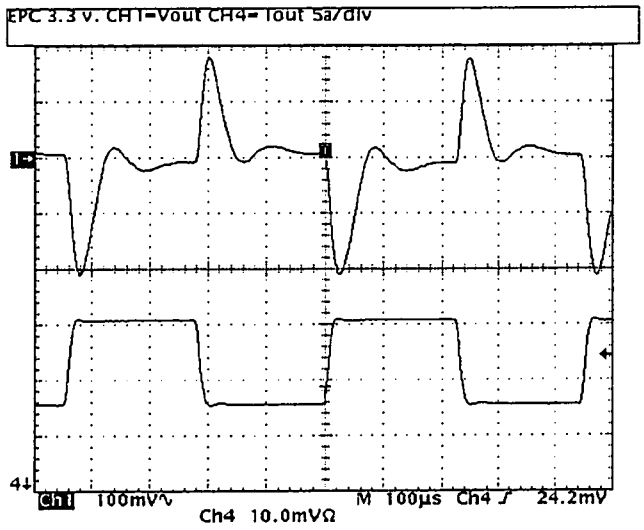


Figure 4.16 **Measured Step Load Change Transient**

Requirement # 4 of the converter performance specifies a maximum output voltage ripple caused by the input voltage ripple equal to 10 mV peak.

On a 100 V input bus, the maximum input voltage ripple is specified at 1 V peak.

This means that the converter must provide an input to output rejection of 100 (or 40 dB).

From classical control theory, we know that the closed loop input to output rejection is given by

$$F_{cl}(s) = \frac{F(s)}{1 + T(s)} \tag{4.5.8}$$

where $F(s)$ is the open loop input to output rejection defined in (4.4.7) and $T(s)$ is the loop gain.

The input to output rejection was simulated using the small signal model and measured on the prototype. The result is shown on Figure 4.17.

As can be seen from the figure, a slight difference (3 dB maximum) occurs between the simulation and the actual measurement in the frequency range from 2 kHz to 20 kHz. This is probably due to the differences between the output filter capacitors equivalent series resistances (ESRs) used in the simulation and the actual ones.

Those differences cause the damping coefficients associated with the capacitors to be different and therefore, the peaking occurring at the poles of $F_{cl}(s)$ are different.

The worst case measured rejection occurs at 10 kHz and is equal to –30 dB, which does not meet our specification of –40 dB.

It should be noted that the frequency at which the peaking in the input to output rejection occurs is precisely the loop cross-over frequency. This is an indication that $F_{cl}(s)$ exhibits a pair of poles at 10 kHz, corresponding to the zeroes of $1 + T(s)$ as suggested by its expression defined in (4.5.8).

This is consistent with the phase margin (at 10 kHz) of 50 degrees; a higher phase margin would have provided a lower peaking and therefore a better attenuation.

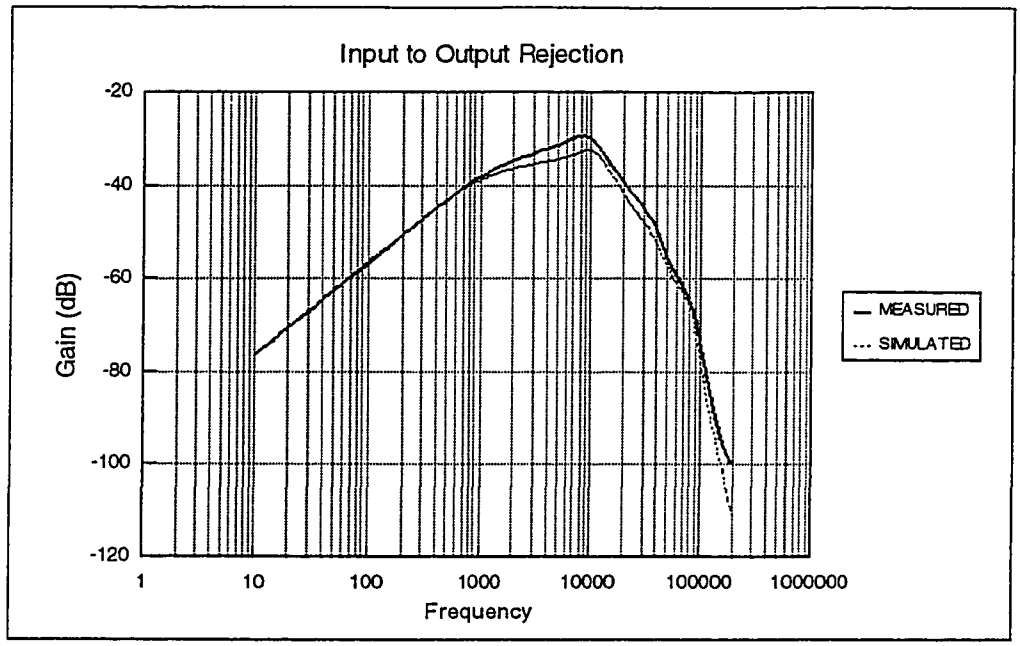


Figure 4.17 Simulated and Measured Input to Output Rejection

In order to improve the line rejection, feedforward compensation was implemented; this consists in superimposing a suitable fraction of the input voltage onto the PWM timing ramp. In theory, this should null the input to output transfer function as demonstrated below.

The small signal output voltage can be written as

$$\hat{v}_{out} = F(s) \cdot \hat{v}_{in} + G(s) \cdot \hat{d} \tag{4.5.9}$$

Where $F(s)$ and $G(s)$ are given by (4.4.7) and (4.4.9) respectively.

Without feedforward compensation, the small signal duty cycle $\hat{d}$ is equal to $0.512 \cdot \hat{v}_c$ as shown earlier, where $\hat{v}_c$ is the small signal error amplifier output.

Superimposing a fraction K of the input voltage onto the timing ramp results in the following relationship for the duty cycle:

$$\hat{d} = 0.512(\hat{v}_c - K \cdot \hat{v}_{in}) \tag{4.5.10}$$

The objective of feedforward consists in finding a value of K which reduces to zero the contribution of $\hat{v}_{in}$ in (4.5.9).

From (4.4.7) and (4.4.9), $F(s)$ and $G(s)$ have the same denominator.

If we rewrite (4.5.9) by considering only the DC gains of $F(s)$ and $G(s)$, we obtain

$$\hat{v}_{out} = n \cdot (1-2D) \cdot V_{in} \cdot 0.512(\hat{v}_c - K \cdot \hat{v}_{in}) + n \cdot D \cdot (1-D) \cdot \hat{v}_{in} \tag{4.5.11}$$

In the above equation, the $\hat{v}_{in}$ terms cancel out if we choose

$$K = \frac{D \cdot (1-D)}{0.512(1-2D) \cdot V_{in}} \tag{4.5.12}$$

This cancellation is valid at low frequencies. At higher frequencies, the different numerators of $F(s)$ and $G(s)$ will cause some $\hat{v}_{in}$ contribution to be present.

The above feedforward scheme was implemented with the injection factor K having the value calculated in (4.5.12). Figure 4.18 shows the resulting measured Input to Output rejection.

As can be seen from Figure 4.18, the worst case rejection is equal to 39 dB. This translates into an output voltage ripple of 11 mV peak ($\hat{v}_{in}$ = 1 V), which is acceptable.

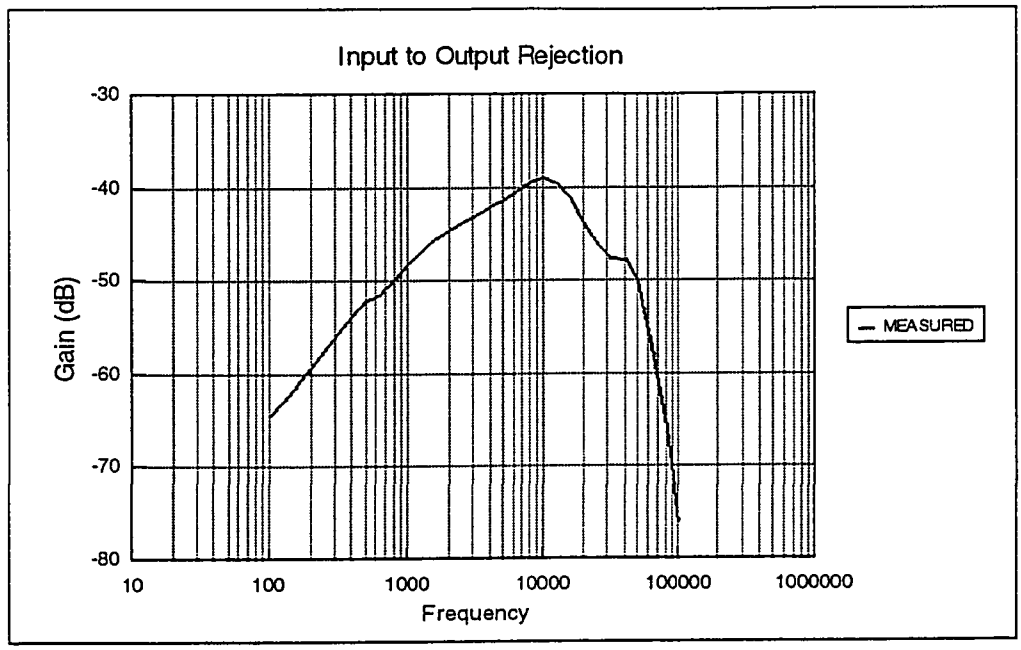


Figure 4.18 Measured Input to Output Rejection with Feedforward

4.6 Conclusions

Dynamic modelling of the CHBC was carried out in the following sequence :

1. Development of a state space averaged large signal model.
2. Development of a small signal model.
3. Based on the small signal model, obtain analytical expressions for both the control to output and input to output transfer functions.
4. Based on above transfer functions, develop a compensation circuit such that when the feedback loop is closed, the converter satisfies a given set of performance criteria when subjected to load transients (step load changes) and to input voltage ripple.

Each step of the above sequence was validated by test before going to the next step.

Excellent correlation was obtained between simulation and test. The expressions of control to output and input to output transfer functions confirm the existence of the double pair of complex poles as outlined in [4]: one pair of complex poles is due to the output filter, the second one is due to the input tank which consists of the half bridge capacitive divider and the transformer magnetizing inductance. The existence of this double pair of poles makes the compensation more difficult to achieve than in a conventional converter having only one pair of poles due to the output filter.

In order to meet the converter dynamic performance specifications while guaranteeing stability, it was found that the two pairs of poles had to be widely separated ; this could only be achieved by substantially increasing the output capacitance. In addition, the pair of poles due to the primary capacitive divider and the transformer magnetizing inductance had to be properly damped. This was easily achieved by splitting the input filter second stage damping network into two identical halves and connecting the resulting midpoint to the capacitive divider midpoint.

With the above modifications, a compensation network was designed which, under a step load condition from half load to full load (7.5A to 15A) and vice-versa, yielded a maximum output voltage undershoot (overshoot) equal to 5% of the nominal value (3.3V).

The compensation scheme however failed to yield a residual output ripple equal to or less than 10mV peak when an AC perturbation of 1V peak was superimposed onto the DC input voltage. A feedforward compensation scheme was added to the feedback loop which resulted in a worst case output voltage ripple of 11mV peak, which was found acceptable.

Chapter 5
Summary and Conclusions

5.1 Summary

The work performed in this thesis consisted in three main parts contained in Chapters 2, 3 and 4 respectively. Chapter 2 is devoted to a comparative study of several conversion topologies ; Chapter 3 describes the design and construction of a working prototype based on the CHBC topology. Finally, Chapter 4 covers the dynamic modelling of the converter.

1. Comparative Study of Several Topologies

Three power conversion topologies were studied and compared in terms of their conduction losses. These topologies are: the ZVS Forward Converter, the ZVS Complementary Half-Bridge Converter (CHBC), and the ZVS Flyback Converter. The objective of the comparison was to determine which topology would deliver an output power of 50 W at an output voltage of 3.3 V and an input voltage of 100 V with the highest efficiency.

All three topologies are derived from conventional PWM topologies and are modified to achieve a soft Zero Voltage Transition (ZVT). A precise mathematical model which includes MOSFET non-linear parasitic capacitances was developed in order to accurately predict the amount of primary magnetizing current required for ZVT to occur. This

mathematical model also performs an accurate calculation of the switching times. It was shown in Chapter 2 that due to the non-linear nature of the Drain to Gate and Drain to Source MOSFET capacitances, the peak voltages reached during a soft transition and the transition times could be determined only by calculating the energies at the beginning and at the end of the transition.

2. Design of a ZVT Complementary Half Bridge Converter

Chapter 3 describes the design and the prototyping of a CHBC delivering 50 W at 3.3 V, from a 100 V input. The breadboard design is based on the circuit parameter values calculated in Chapter 2 which will exactly yield ZVT on the primary side. The design uses a low profile power transformer which consists of a printed circuit board containing the windings, sandwiched between two ferrite core halves.

The design features a delay generator which introduces delays between the turn-off of one primary MOSFET and the turn-on of its complement. These delays are essential to the correct implementation of ZVT on the primary side.

In an effort to determine the converter optimal operating conditions, a mathematical model which calculates efficiency for different switching frequencies and different primary magnetizing inductance values was developed.

As a second phase of the optimization effort, a mathematical model which calculates the size of the power magnetics and capacitors as a function of the switching frequency has been developed. Fixed constraints in accordance with the efficiency and input/output ripple requirements are imposed to the model for any switching frequency.

3. CHBC Dynamic modelling

Dynamic modelling of the CHBC was carried out in the following sequence:

5. Development of a state space averaged large signal model.

6. Development of a small signal model obtained by performing a perturbation and linearization of the basic state space averaged (large signal model) equations.

7. Based on the small signal model developed in the previous step, obtain analytical expressions for both the control to output and input to output transfer functions.

8. Based on above transfer functions, develop a compensation circuit such that when the feedback loop is closed, the converter satisfies a given set of performance criteria when subjected to load transients (step load changes) and to input voltage ripple.

Each step of the above sequence was validated by test before going to the next step.

5.2 Conclusions

1. Comparative Study of Several Topologies

The accuracy of both the magnetizing current required for ZVT and of the switching times as predicted by the mathematical model was confirmed by the simulations and by the measurements on the real prototype.

It has been shown that under the same operating conditions the Forward Converter and the CHBC had comparable conduction losses whereas the Flyback Converter had significantly higher conduction losses.

The CHBC was preferred over the Forward Converter because the Drain-to-Source voltage of the primary MOSFETs is inherently clamped to the input voltage even under transient conditions. Since the maximum input voltage equals 110 V, 200 V MOSFETs can be used. These MOSFET have a low Rds_{on} and are supplied by several power MOSFETs manufacturers.

By contrast, the Forward Converter requires 400 V devices because the maximum V_{DS} across the primary MOSFETs was found equal to 260 V, and this value does not include transient conditions. At this moment, 400 V MOSFETs are only supplied by International Rectifier, and are not offered in surface mount packages. In addition, the higher V_{DS} than in a CHBC causes longer transition times which limit the frequency of operation.

2. Design of a ZVT Complementary Half Bridge Converter

The waveforms recorded on the breadboard are shown to be in excellent agreement with the predictions of Chapter 2. Moreover, the waveforms confirm the crucial role played by the leakage inductance during ZVT on the primary side.

The measured efficiencies are shown to be in excellent agreement with the calculated ones, using the mathematical model. Both the calculations and the experimental results show that the addition of one MOSFET in the secondary synchronous rectifier branch which conducts during $(1\text{-}D) \times Ts$ yields an efficiency increase of more than 1 % at 400 kHz. With two parallel MOSFETs in the *(1-D)* branch, typical efficiencies of 87% have been measured.

The mathematical model which calculates the size of the power stage as a function of the switching frequency with a fixed set of constraints reveals that the size of the converter decreases rapidly from 100 kHz to 200 kHz and then slowly decreases until it reaches a minimum at 400 kHz. Based on this small size decrease beyond 200 kHz and on the efficiency figures obtained before, it can be seen that there is little incentive to increase the switching frequency beyond 300 kHz.

3. CHBC Dynamic Modelling

Excellent correlation was obtained between simulation and test. The expressions of control to output and input to output transfer functions confirm the existence of the double pair of complex poles as outlined in [4]: one pair of complex poles is due to the output

filter, the second one is due to the input tank which consists of the half bridge capacitive divider and the transformer magnetizing inductance. The existence of this double pair of poles makes the compensation more difficult to achieve than in a conventional converter having only one pair of poles due to the output filter.

Current mode control would eliminate one pole of the output filter; however, the classical implementation of peak current mode control which is achieved by sensing the current in the transformer primary is impractical in this application because the primary magnetizing current creates a primary current slope much larger than that of the reflected secondary current.

5.3 Suggestions for Future Work

There are two areas which deserve further investigation.

1. **Reverse Recovery Characterization of the Synchronous Rectifier MOSFETs Antiparallel Diode**

It has been shown in Chapters 2 and 3 that the transformer leakage inductance plays a crucial role in the ZVT phenomena. The higher the leakage inductance, the less primary magnetizing current is required to perform a full ZVT; therefore, the primary conduction losses decrease. However, a higher leakage inductance also causes the overlap times in the secondary synchronous rectifiers to increase; this in turn causes higher secondary conduction losses because during the overlap times, only the antiparallel diodes of the synchronous rectifiers conduct, not the MOSFETs themselves. Another loss mechanism which strongly depends on the leakage inductance is the reverse recovery of the synchronous rectifier antiparallel diodes. The higher the leakage inductance, the lower the peak reverse recovery current; in theory, this would cause a decrease of the reverse recovery losses.

Based on the above considerations, we conclude that there exists an optimum value of the leakage inductance for which the sum of all the losses which depend on this leakage inductance is minimum. However, this optimum value cannot be determined unless a suitable model which describes the secondary MOSFETs antiparallel diodes reverse recovery charge and peak current as a function of the forward current and of the *dI/dt* becomes available. This model does not yet exist for the synchronous rectifier MOSFETs used in this project because these are still in a developmental phase. In this thesis, the value of peak reverse recovery current used for the purpose of losses calculations was taken equal to one half of the main forward current (determined empirically). It is strongly suggested that these MOSFETs be characterized for reverse recovery in order to build a more precise model, which would then lead to an optimum value of the leakage inductance.

2. High Frequency Proximity Effect in Transformer Windings

As explained in Chapters 2 and 3, the CHBC belongs to a family of ZVS topologies which require a significant amount of primary magnetizing current in order to guarantee ZVT on the primary side; this magnetizing current is not reflected on the secondary winding of the transformer and therefore, the magnetic field outside the transformer windings is non zero; this causes the existence of a magnetic field component perpendicular to the winding layers. As a result, the proximity effect in the windings cannot be computed using the classical theory formulation described for example in [30] because the fundamental assumption supporting this theory, i.e. the magnetic field must everywhere be parallel to the winding layers is invalidated. As explained in Chapter 3, the primary AC resistance of the PCB transformer used in the prototype was characterized for different frequencies under two conditions: secondary winding open and shorted. This exercise resulted in two characterization curves which were then used to calculate the high frequency losses due to magnetizing current and load current respectively. This empirical method is only valid for one geometry. The only method leading to an accurate prediction of the proximity effect for

all geometries is to perform a Finite Element Analysis using software packages such as Ansoft's Maxwell 3D Field Simulator [25]. This precise analysis would then yield frequency dependent correction curves for all geometries. The author strongly encourages future work in this area.

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Appendix A

A Comparative Study of Three Topologies in Terms of Conduction Losses

A COMPARISON OF CONDUCTION LOSSES BETWEEN THREE TOPOLOGIES :

- THE SOFT SWITCHING ACFCSR
- THE CONTINUOUS ZVT FLYBACK
- THE COMPLEMENTARY HB WITH HIGH MAGNETIZING CURRENT

$Rds_{360} := 0.2 \cdot 1.7$ $\quad Rds_{360} = 0.34$ $\quad Vout := 3.3$ $\quad Vin_{min} := 90$

$Rds_{053} := 0.007 \cdot 1.3$ $\quad Rds_{053} = 9.1 \cdot 10^{-3}$ $\quad Pout := 49.5$ $\quad Vin := 100$

$Rds_{250} := 0.1 \cdot 1.6$ $\quad Rds_{250} = 0.16$ $\quad Ts := 2.5 \cdot 10^{-6}$ $\quad Vin_{max} := 110$

$R\_sec := 0.004$ $\quad R\_pri(N) := (R\_sec - 0.003) \cdot N^2$

$I_o := \frac{Pout}{Vout}$ $\quad I_o = 15$ $\quad Von := I_o \cdot Rds_{053}$ $\quad Von = 0.137$

1) SOFT SWITCHING ACFCSR

Constraint : VDS_{max} = 300V ; this will occur when Vin = Vin_{min} = 90V.

$D_{max} := 1 - \frac{Vin_{min}}{300}$ $\quad D_{max} = 0.7$

We know that : $Vout + Von = D \cdot \frac{Vin}{N} - \frac{L\_lk \cdot I_o}{Ts}$ $\quad$ Take : $L\_lk := 33 \cdot 10^{-9}$

$N := \frac{D_{max} \cdot Vin_{min}}{Vout + Von + \frac{L\_lk \cdot I_o}{Ts}}$ $\quad N = 17.334$ $\quad N := 17$ $\quad \frac{I_o}{N} = 0.882$

$D_{max} := \frac{N \cdot \left(Vout + Von + \frac{L\_lk \cdot I_o}{Ts} \right)}{Vin_{min}}$ $\quad D_{max} = 0.687$

$D := \frac{N \cdot \left(Vout + Von + \frac{L\_lk \cdot I_o}{Ts} \right)}{Vin}$ $\quad D = 0.618$

$Vds_{max} := \frac{N \cdot \left(Vout + Von + \frac{L\_lk \cdot I_o}{Ts} \right)}{D_{max} \cdot (1 - D_{max})}$ $\quad Vds_{max} = 287.097$

$Vds_{nom} := \frac{N \cdot \left(Vout + Von + \frac{L\_lk \cdot I_o}{Ts} \right)}{D \cdot (1 - D)}$ $\quad Vds_{nom} = 261.688$ $\quad Vc := Vin \cdot \frac{D}{1 - D}$ $\quad Vc = 161.688$

Calculate I_{neg_pk} to guarantee ZVT

The current I_{neg_pk} must discharge the equivalent primary side capacitance from Vin+Vc to zero.
Therefore, we need to calculate the minimum current and primary inductance required to guarantee ZVS.
Zero voltage transition occurs in two steps :
1) Discharge of secondary parasitic capacitances from Vc/N to zero
2) Transfer of secondary current from one synchronous rectifier to the other ; At the end of this stage, either the voltage across the switching MOSFET equals zero in which case the voltage transition is over or the primary current reduces to zero in which case some residual charge is still present across the primary parasitic capacitance ;

IRHM7360 DATA

$Cds0 := 3.54 \cdot 10^{-9}$ $Cgd0 := 12 \cdot 10^{-9}$ $A := 2$ $Qgd := 120 \cdot 10^{-9}$ $C_{tfo} := 0.25 \cdot 10^{-9}$

$$Coss(V) := \frac{Cds0}{\sqrt{1 + \frac{V}{0.8}}} + \frac{Cgd0}{A + V} \qquad (A.1)$$

$$Cgd(V) := \frac{Cgd0}{A + V} \qquad (A.2)$$

FSYC053 DATA

$Ciss_{ON} := 13 \cdot 10^{-9}$

$$Coss_{sec}(V) := \frac{223.15 \cdot 10^{-9}}{(8.074 + V)^{1.599}} + \frac{14.2 \cdot 10^{-9}}{\sqrt{1 + \frac{V}{0.8}}} \qquad (A.3)$$

$$Coss_{OFF} := \frac{1}{\left(\frac{Vc}{N}\right)} \cdot \int_0^{\frac{Vc}{N}} Coss_{sec}(V)\, dV \qquad (A.4)$$

$Coss_{OFF} = 1.036 \cdot 10^{-8}$

The leakage inductance as seen from the primary side equals :

$L\_lk := 33 \cdot 10^{-9} \cdot N^2$ $L\_lk = 9.537 \cdot 10^{-6}$

We need to implement a capacitive divider such that the total voltage excursion on the gate of the MOSFET is 10V

$$C_{bias} := \frac{Ciss_{ON} \cdot 10}{\frac{Vin + Vc}{N} - 10} \qquad C_{sec} := \frac{\frac{C_{bias} \cdot Ciss_{ON}}{C_{bias} + Ciss_{ON}}}{N^2}$$

Calculate total secondary side capacitance and resistance : $R_{damp} := 0$ $M_{ov} := 1.25$

$$C_{sec} := \frac{Ciss_{ON} + Coss_{OFF}}{N^2} \qquad (A.5) \qquad C_{sec} = 8.085 \cdot 10^{-11}$$

$$R_{sec} := \frac{(0.25 + R_{damp}) \cdot Ciss_{ON}^{2} + 0.25 \cdot Coss_{OFF}^{2}}{(Ciss_{ON} + Coss_{OFF})^2} \cdot N^2 \qquad (A.6) \qquad R_{sec} = 36.585$$

$$C_{pri} := \frac{1}{Vc \cdot M_{ov}} \cdot \left(\int_{0}^{Vc \cdot M_{ov}} Coss(V)\, dV + \int_{Vin + Vc - Vc \cdot M_{ov}}^{Vin + Vc} Coss(V)\, dV \right) + C_{tfo} \qquad (A.7)$$

$$C_{pri} = 1.311 \cdot 10^{-9}$$

$$\omega_o := \frac{1}{\sqrt{\frac{L\_lk \cdot C_{pri} \cdot C_{sec}}{C_{pri} + C_{sec}}}} \qquad Q := \frac{1}{R_{sec}} \cdot \sqrt{\frac{L\_lk}{\frac{C_{pri} \cdot C_{sec}}{C_{pri} + C_{sec}}}} \qquad \omega_1 := \omega_o \cdot \sqrt{1 - \frac{1}{4 \cdot Q^2}}$$

$$I_{L\_lk}(I_{n\_pk}, t) := \frac{I_{n\_pk} \cdot C_{sec}}{C_{pri} + C_{sec}} \cdot \left[1 - \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \left(\frac{\sin(\omega_1 \cdot t)}{\sqrt{4 \cdot Q^2 - 1}} + \cos(\omega_1 \cdot t) \right) \right] \qquad (A.8)$$

$$V_{Csec}(I_{n\_pk}, t) := -Vc - \frac{I_{n\_pk} \cdot C_{pri} \cdot C_{sec}}{(C_{pri} + C_{sec})^2} \cdot R_{sec} + \frac{I_{n\_pk}}{C_{pri} + C_{sec}} \cdot t \ldots$$
$$+ \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \left[\frac{\sin(\omega_1 \cdot t)}{\sqrt{4 \cdot Q^2 - 1}} \cdot \frac{1}{\omega_o} \cdot \left(\frac{1}{Q} - 2 \cdot Q \right) + \frac{\cos(\omega_1 \cdot t)}{\omega_o \cdot Q} \right] \cdot \frac{I_{n\_pk}}{C_{pri} + C_{sec}} \qquad (A.9)$$

$$V_{Cpri}(I_{n\_pk}, t) := \frac{I_{n\_pk}}{C_{pri} + C_{sec}} \cdot t - Vc \ldots$$
$$+ I_{n\_pk} \cdot \left(\frac{C_{sec}}{C_{sec} + C_{pri}} \right)^2 \cdot R_{sec} \cdot \left(1 - \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \cos(\omega_1 \cdot t) + \frac{2 \cdot Q^2 - 1}{\sqrt{4 \cdot Q^2 - 1}} \cdot \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \sin(\omega_1 \cdot t) \right)$$

(A.10)

$t1 := 10^{-9}$

GIVEN

$V_{Csec}(I_{n\_pk}, t1) + R_{sec} \cdot I_{L\_lk}(I_{n\_pk}, t1) = 0$

$Answer(I_{n\_pk}) := Find(t1)$

$k := 0..30$ $\qquad I_{neg\_pk_k} := \frac{I_o}{N} + k \cdot 0.05$

$t1_k := Answer(I_{neg\_pk_k})$

$I_{Lm_k} := I_{neg\_pk_k} - I_{L\_lk}(I_{neg\_pk_k}, t1_k)$ $\qquad V1_k := V_{Cpri}(I_{neg\_pk_k}, t1_k) + Vc$ $\qquad V2_k := Vin + Vc$

We now calculate the current through L_lk at the end of the voltage transition, assuming that the transition takes place in 2 steps ; for this first calculation we assign to V2 a value equal to Vin + Vc. If the current value is less than Io/N, the assumption is validated. If not, we must redo the calculation by assigning a current value through L_lk equal to Io/N and calculating V2.

$$X_k := \int_{V1_k}^{V2_k} Coss(V)\cdot V\, dV + \int_{Vin+Vc-V1_k}^{Vin+Vc-V2_k} Coss(V)\cdot V\, dV - Vc\cdot\int_{V1_k}^{V2_k} Coss(V)\, dV \ldots$$
$$+\frac{1}{2}\cdot C_{tfo}\cdot\left[(V2_k - Vc)^2 - (V1_k - Vc)^2\right] - Vin\cdot\int_{Vin+Vc-V1_k}^{Vin+Vc-V2_k} Coss(V)\, dV$$

We now need to find the roots of the following polynomial : $\frac{1}{2}\cdot L\_lk\cdot(I_k)^2 - L\_lk\cdot I_{Lm_k}\cdot I_k + X_k = 0$

$$I_k := if\left[\left(I_{Lm_k}\right)^2 - 2\cdot\frac{X_k}{L\_lk} < 0, I_{Lm_k}, I_{Lm_k} - \sqrt{\left(I_{Lm_k}\right)^2 - 2\cdot\frac{X_k}{L\_lk}}\right]$$

$W := 10$

GIVEN

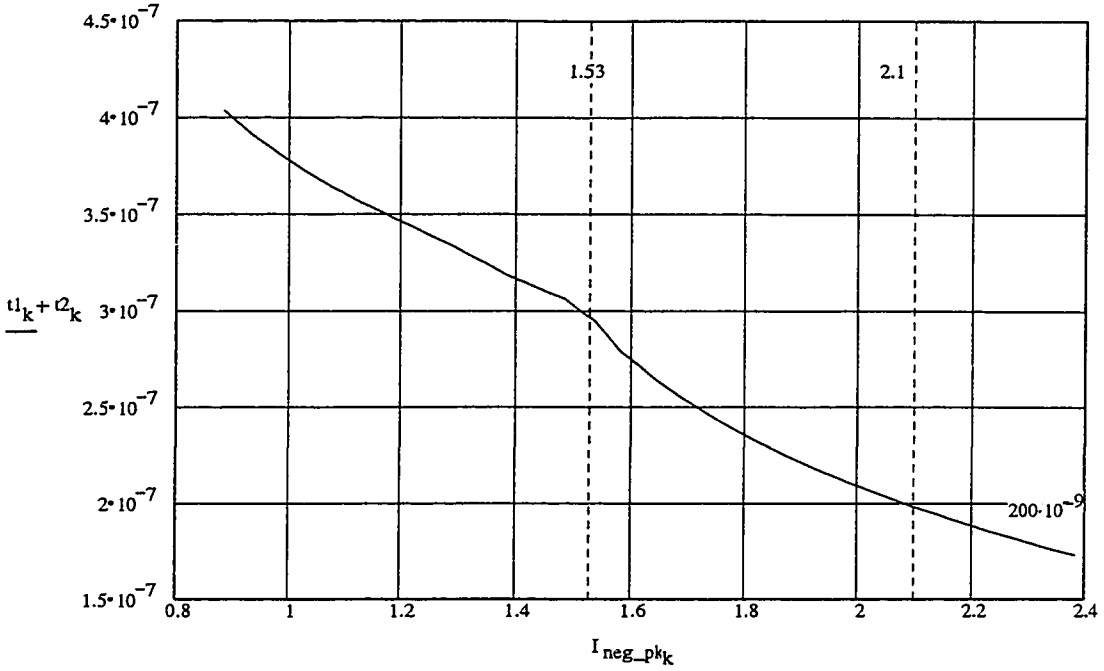
$$\frac{1}{2}\cdot L\_lk\cdot(x)^2 - L\_lk\cdot y\cdot x + \int_U^W Coss(V)\cdot V\, dV + \int_{Vin+Vc-U}^{Vin+Vc-W} Coss(V)\cdot V\, dV - Vc\cdot\int_U^W Coss(V)\, dV \ldots = 0$$
$$+\frac{1}{2}\cdot C_{tfo}\cdot\left[(W - Vc)^2 - (U - Vc)^2\right] - Vin\cdot\int_{Vin+Vc-U}^{Vin+Vc-W} Coss(V)\, dV$$

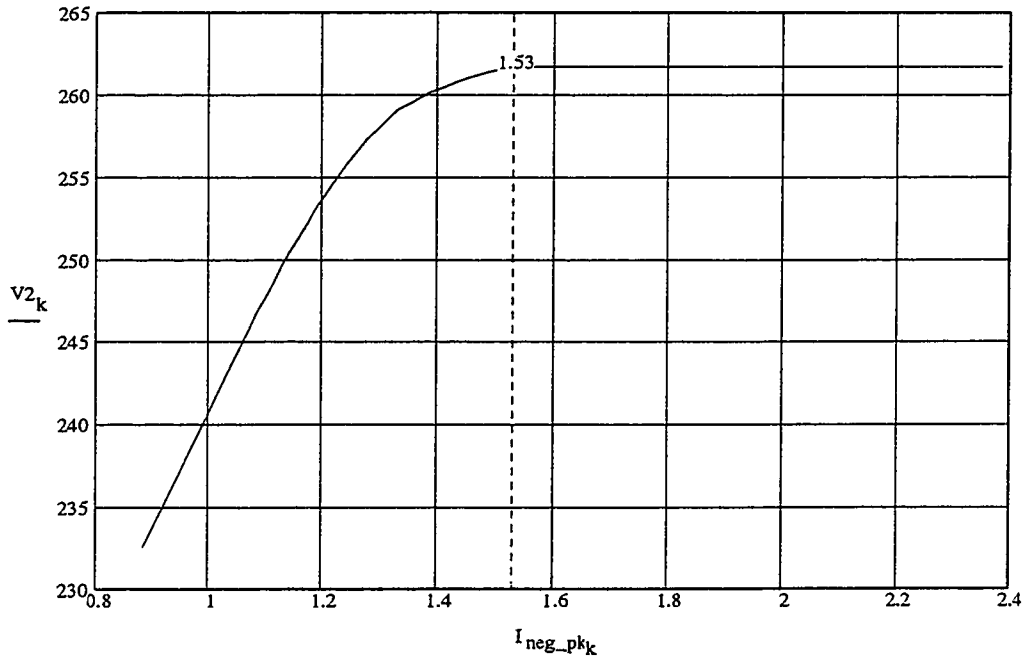
$Ans(U, W, x, y) := Find(W)$

$V2_k := Ans\left(V1_k, V2_k, I_k, I_{Lm_k}\right)$

$$F(U,V) := \int_U^V Coss(x)\cdot x\, dx + \int_{Vin+Vc-U}^{Vin+Vc-V} Coss(x)\cdot x\, dx - Vc\cdot\int_U^V Coss(x)\, dx - Vin\cdot\int_{Vin+Vc-U}^{Vin+Vc-V} Coss(x)\, dx \ldots$$
$$+\frac{1}{2}\cdot C_{tfo}\cdot\left[(V - Vc)^2 - (U - Vc)^2\right]$$

$$t2_k := \int_{V1_k}^{V2_k - 0.5} \frac{Coss(V) + Coss(Vin + Vc - V) + C_{tfo}}{\sqrt{\left(I_{Lm_k}\right)^2 - \frac{2\cdot F\left(V1_k, V\right)}{L\_lk}}}\, dV$$


4.5·10^-7
4·10^-7
3.5·10^-7
3·10^-7
2.5·10^-7
2·10^-7
1.5·10^-7
t1_k + t2_k
1.53
2.1
200·10^-9
0.8
1
1.2
1.4
1.6
1.8
2
2.2
2.4
I neg_pk_k


265
260
255
250
245
240
235
230
V2_k
1.53
0.8
1
1.2
1.4
1.6
1.8
2
2.2
2.4
I neg_pk_k

Choose Ineg_pk equal to the value required to make a full ZVT transition in 200 nanoseconds ; therefore :

$I_{neg\_pk} := 2.1$

a) Calculate the peak positive transformer current :

$I_{pk} := I_{neg\_pk} + \frac{I_o}{N}$ $\qquad I_{pk} = 2.982$

b) Calculate the RMS value of the primary current :

In the forward converter, the primary current is the superposition of a triangular wave whose peak to peak amplitude equals 2 x I_{neg_pk} and a rectangular wave whose amplitude equals $\frac{I_o}{N}$ during D x Ts seconds and zero for the rest of the period. Therefore,

$$I_{pri\_RMS} := \sqrt{\frac{I_o^2 \cdot D}{N^2} + \frac{1}{3} \cdot (I_{neg\_pk})^2} \qquad I_{pri\_RMS} = 1.397$$

c) Calculate the losses occurring on the primary side of the converter :

With the exception of the transition periods (which are considered negligible with respect to the switching period), the primary current always flows through the transformer primary winding and through one of the primary Mosfets. Therefore, the total primary resistance consists of the transformer primary winding resistance in series with one primary Mosfet RDS_{ON}

$P_{primary} := \left(R\_pri(N) + Rds_{360}\right) \cdot I_{pri\_RMS}^{2}$ $\quad P_{primary} = 1.227$ Watt

d) Calculate the losses in the transformer secondary winding :

The secondary current flows through the secondary winding only during D x Ts ; ttherefore :

$P_{sec} := R\_sec \cdot I_o^{2} \cdot D$ $\quad P_{sec} = 0.556$ Watt

e) Calculate the losses in the secondary synchronous rectifiers :

With the exception of the transition periods (which are considered negligible with respect to the switching period), the secondary current always flows through one of the secondary synchronous recitifier Mosfets. Therefore :

$P_{SR} := Rds_{053} \cdot I_o^{2}$ $\quad P_{SR} = 2.048$ Watt

f) Calculate total conduction losses :

$P_{tot} := P_{primary} + P_{sec} + P_{SR}$ $\quad P_{tot} = 3.831$ Watt

Calculate primary magnetizing inductance needed to achive the required value of Ineg_pk :

$L_{pri} := \frac{Vin}{2 \cdot I_{neg\_pk}} \cdot D \cdot Ts$ $\quad L_{pri} = 3.678 \cdot 10^{-5}$

2) SOFT SWITCHING COMPLEMENTARY HALF BRIDGE

Choice of D = 50% when Vin = Vin_{min} = 90V

$D_{max} := 0.5$ $L\_lk := 33 \cdot 10^{-9}$

$$N := \frac{2 \cdot D_{max} \cdot (1 - D_{max}) \cdot Vin_{min}}{Vout + Von + \frac{L\_lk \cdot I_o}{Ts}} \qquad N = 12.381 \qquad N := 12$$

Calculate D for Vin = 100V

$D := 0.1$

GIVEN

$$Vout + Von = \frac{2 \cdot D \cdot (1 - D) \cdot Vin}{N} - \frac{L\_lk \cdot I_o}{Ts}$$

$D := Find(D)$ $D = 0.321$

Calculate D_{min} for Vin = Vin_{max} = 120V

$D_{min} := 0.1$

GIVEN

$$Vout + Von = \frac{2 \cdot D_{min} \cdot (1 - D_{min}) \cdot Vin_{max}}{N} - \frac{L\_lk \cdot I_o}{Ts}$$

$D_{min} := Find(D_{min})$ $D_{min} = 0.273$

Calculate I_{min} to guarantee ZVT in 200 nanoseconds

The current I_{min} must discharge the equivalent primary side capacitance from Vin to zero in 200 nanoseconds. Therefore, we need to calculate the minimum current and primary inductance required to guarantee ZVS in 200 nanoseconds maximum.
Zero voltage transition occurs in either two or three steps :
1) Discharge of parasitic capacitances from Vin to (1-D) x Vin.
2) Transfer of Io/N from primary to secondary ; At the end of this stage, the voltage across the switching MOSFET either equals zero in which case the voltage transition is over ; or is still above zero, in which case a third discharge step is needed.
3) Discharge of parasitic capacitances from residual positive voltage to zero.

IRHM7250 DATA

$Cds0 := 3.311 \cdot 10^{-9}$ $Cgd0 := 9.186 \cdot 10^{-9}$ $A := 2.211$ $\gamma := 1.107$ $C_{tfo} := 250 \cdot 10^{-12}$

$$Coss(V) := \frac{Cds0}{\sqrt{1 + \frac{V}{0.8}}} + \frac{Cgd0}{(A + V)^{\gamma}} \qquad Cgd(V) := \frac{Cgd0}{(A + V)^{\gamma}}$$

The leakage inductance as seen from the primary side equals :

$$L\_lk := 33 \cdot 10^{-9} \cdot \left(\frac{N}{2}\right)^2 \qquad L\_lk = 1.188 \cdot 10^{-6}$$

We need to implement a capacitive divider such that the total voltage excursion on the gate of the MOSFET is 10V

$$C_{bias} := \frac{Ciss_{ON} \cdot 10}{2 \cdot \frac{Vin}{N} - 10} \qquad C_{sec} := \frac{\frac{C_{bias} \cdot Ciss_{ON}}{C_{bias} + Ciss_{ON}}}{\left(\frac{N}{2}\right)^2}$$

Calculate total secondary side capacitance $R_{damp} := 0$ $M_{ov} := 2$

$$Coss_{OFF} := \frac{1}{\frac{2 \cdot Vin \cdot D}{N}} \cdot \int_0^{\frac{2 \cdot Vin \cdot D}{N}} Coss_{sec}(V)\, dV \qquad Coss_{OFF} = 1.276 \cdot 10^{-8}$$

$$C_{sec} := \frac{Ciss_{ON} + Coss_{OFF}}{\left(\frac{N}{2}\right)^2} \qquad C_{sec} = 7.154 \cdot 10^{-10}$$

$$R_{sec} := \frac{(0.25 + R_{damp}) \cdot Ciss_{ON}^2 + 0.25 \cdot Coss_{OFF}^2}{(Ciss_{ON} + Coss_{OFF})^2} \cdot \left(\frac{N}{2}\right)^2 \qquad R_{sec} = 4.5$$

$$C_{pri} := \frac{1}{Vin \cdot D \cdot M_{ov}} \cdot \left(\int_0^{Vin \cdot D \cdot M_{ov}} Coss(V)\, dV + \int_{100 - Vin \cdot D \cdot M_{ov}}^{100} Coss(V)\, dV \right) + C_{tfo}$$

$C_{pri} = 1.747 \cdot 10^{-9}$

$$\omega_o := \frac{1}{\sqrt{\frac{L\_lk \cdot C_{pri} \cdot C_{sec}}{C_{pri} + C_{sec}}}} \qquad Q := \frac{1}{R_{sec}} \cdot \sqrt{\frac{L\_lk}{\frac{C_{pri} \cdot C_{sec}}{C_{pri} + C_{sec}}}} \qquad \omega_1 := \omega_o \cdot \sqrt{1 - \frac{1}{4 \cdot Q^2}}$$

$$I_{L\_lk}(I_{n\_pk}, t) := \frac{I_{n\_pk} \cdot C_{sec}}{C_{pri} + C_{sec}} \cdot \left[1 - \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \left(\frac{\sin(\omega_1 \cdot t)}{\sqrt{4 \cdot Q^2 - 1}} + \cos(\omega_1 \cdot t) \right) \right]$$

$$V_{Csec}(I_{n\_pk}, t) := -Vin \cdot D - \frac{I_{n\_pk} \cdot C_{pri} \cdot C_{sec}}{(C_{pri} + C_{sec})^2} \cdot R_{sec} + \frac{I_{n\_pk}}{C_{pri} + C_{sec}} \cdot t \ldots$$
$$+ \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \left[\frac{\sin(\omega_1 \cdot t)}{\sqrt{4 \cdot Q^2 - 1}} \cdot \frac{1}{\omega_o} \cdot \left(\frac{1}{Q} - 2 \cdot Q \right) + \frac{\cos(\omega_1 \cdot t)}{\omega_o \cdot Q} \right] \cdot \frac{I_{n\_pk}}{C_{pri} + C_{sec}}$$

$$V_{Cpri}(I_{n\_pk}, t) := \frac{I_{n\_pk} \cdot t}{C_{pri} + C_{sec}} - Vin \cdot D \ldots$$
$$+ I_{n\_pk} \cdot \left(\frac{C_{sec}}{C_{sec} + C_{pri}} \right)^2 \cdot R_{sec} \cdot \left(1 - \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \cos(\omega_1 \cdot t) + \frac{2 \cdot Q^2 - 1}{\sqrt{4 \cdot Q^2 - 1}} \cdot \exp\left(-\frac{R_{sec}}{2 \cdot L\_lk} \cdot t \right) \cdot \sin(\omega_1 \cdot t) \right)$$

$t1 := 10^{-9}$

GIVEN

$V_{Csec}(I_{n\_pk}, t1) + R_{sec} \cdot I_{L\_lk}(I_{n\_pk}, t1) = 0$

$Answer(I_{n\_pk}) := Find(t1)$

$k := 0..30 \qquad I_{neg\_pk_k} := 2 \cdot \frac{I_o}{N} + k \cdot 0.050$

$t1_k := Answer(I_{neg\_pk_k})$

$I_{Lm_k} := I_{neg\_pk_k} - I_{L\_lk}(I_{neg\_pk_k}, t1_k)$

$V1_k := V_{Cpri}(I_{neg\_pk_k}, t1_k) + Vin \cdot D \qquad V2_k := Vin$

We now calculate the current through L_lk at the end of the voltage transition, assuming that the transition takes place in 2 steps ; for this first calculation we assign to V2 a value equal to Vin. If the current value is less than 2 x Io/N, the assumption is validated. If not, we must redo the calculation by assigning a current value through L_lk equal to 2 x Io/N and calculating V2.

$$X_k := \int_{V1_k}^{V2_k} Coss(V)\cdot V\,dV + \int_{Vin - V1_k}^{Vin - V2_k} Coss(V)\cdot V\,dV - D\cdot Vin\cdot \int_{V1_k}^{V2_k} Coss(V)\,dV \ldots$$
$$+ \frac{1}{2}\cdot C_{tfo}\cdot\left[\left(V2_k - D\cdot Vin\right)^2 - \left(V1_k - D\cdot Vin\right)^2\right] - (1 - D)\cdot Vin\cdot \int_{Vin - V1_k}^{Vin - V2_k} Coss(V)\,dV$$

We now need to find the roots of the following polynomial : $\frac{1}{2}\cdot L\_lk\cdot\left(I_k\right)^2 - L\_lk\cdot I_{Lm_k}\cdot I_k + X_k = 0$

$$I_k := if\left[\left(I_{Lm_k}\right)^2 - 2\cdot\frac{X_k}{L\_lk} < 0, I_{Lm_k}, I_{Lm_k} - \sqrt{\left(I_{Lm_k}\right)^2 - 2\cdot\frac{X_k}{L\_lk}}\right]$$

$W := 10$

GIVEN

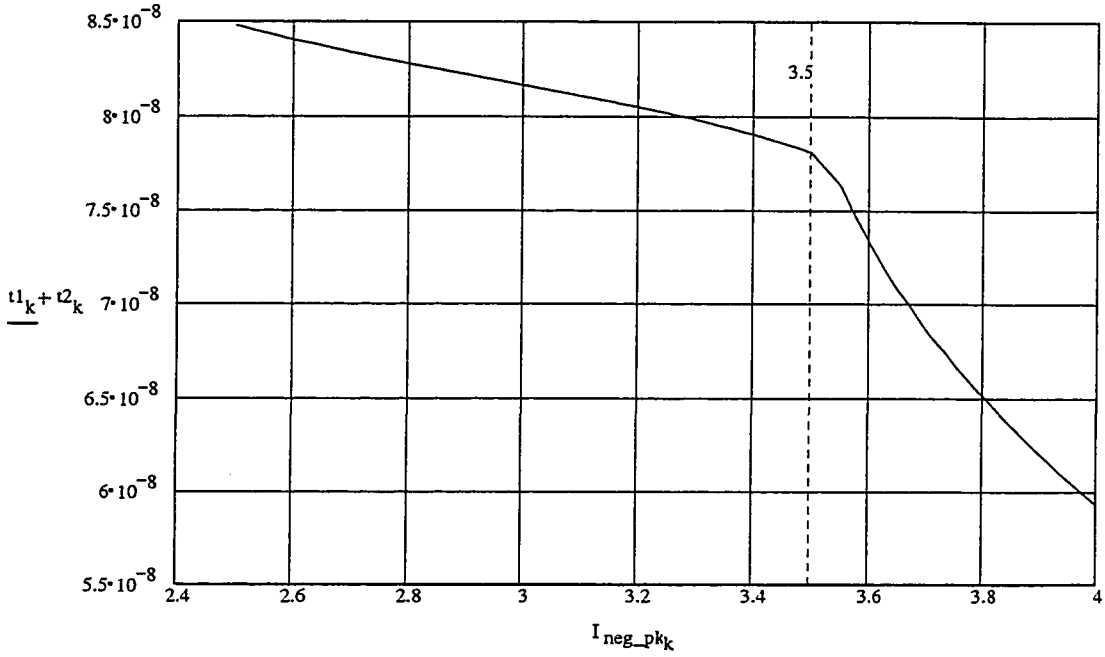
$$\frac{1}{2}\cdot L\_lk\cdot(x)^2 - L\_lk\cdot y\cdot x + \int_U^W Coss(V)\cdot V\,dV + \int_{Vin - U}^{Vin - W} Coss(V)\cdot V\,dV - D\cdot Vin\cdot \int_U^W Coss(V)\,dV \ldots = 0$$
$$+ \frac{1}{2}\cdot C_{tfo}\cdot\left[(W - D\cdot Vin)^2 - (U - D\cdot Vin)^2\right] - (1 - D)\cdot Vin\cdot \int_{Vin - U}^{Vin - W} Coss(V)\,dV$$

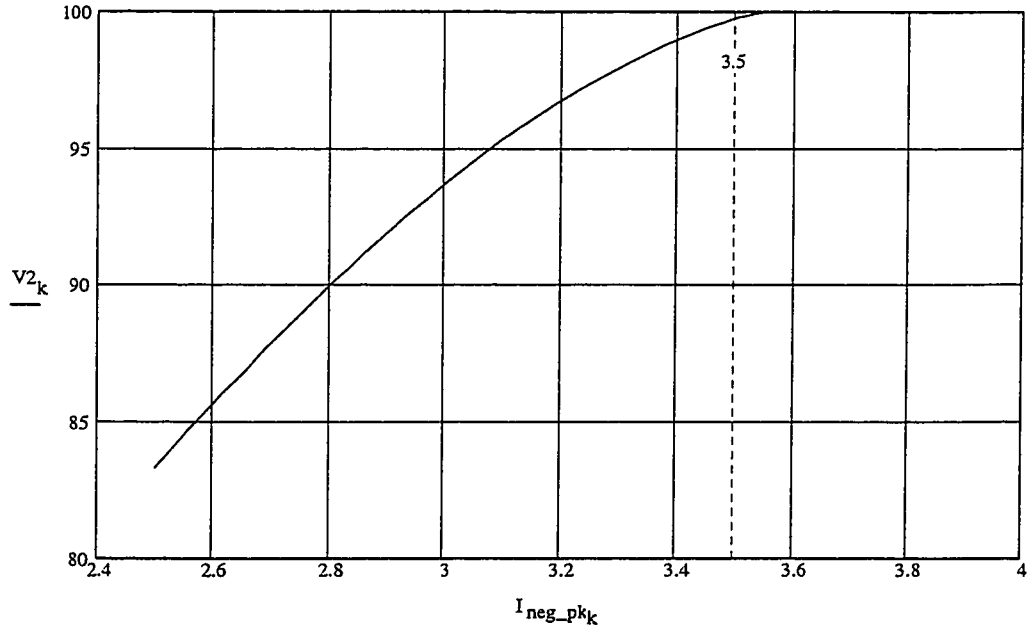
$Ans(U, W, x, y) := Find(W)$

$V2_k := Ans\left(V1_k, V2_k, I_k, I_{Lm_k}\right)$

$$F(U,V) := \int_U^V Coss(x)\cdot x\,dx + \int_{Vin - U}^{Vin - V} Coss(x)\cdot x\,dx - D\cdot Vin\cdot \int_U^V Coss(x)\,dx \ldots$$
$$+ \frac{1}{2}\cdot C_{tfo}\cdot\left[(V - D\cdot Vin)^2 - (U - D\cdot Vin)^2\right] - (1 - D)\cdot Vin\cdot \int_{Vin - U}^{Vin - V} Coss(x)\,dx$$

$$t2_k := \int_{V1_k}^{V2_k - 0.5} \frac{Coss(V) + Coss(Vin - V) + C_{tfo}}{\sqrt{\left(I_{Lm_k}\right)^2 - \frac{2\cdot F\left(V1_k, V\right)}{L\_lk}}}\,dV$$


8.5·10^-8
8·10^-8
7.5·10^-8
7·10^-8
6.5·10^-8
6·10^-8
5.5·10^-8
t1_k + t2_k
3.5
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
4
I neg_pk_k


100
95
90
85
80
V2_k
3.5
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
4
I neg_pk_k

Choose I_{neg_pk} equal to the minimum value required to perform full ZVT, i.e. : $I_{neg\_pk} := 3.5$

a) Calculate the peak to peak value of the transformer magnetizing current :

$$\Delta I := 2 \cdot I_{neg\_pk} - \frac{4 \cdot D \cdot I_o}{N} \qquad \Delta I = 5.393$$

b) Calculate the RMS value of the primary current :

In the complementary half bridge converter, the primary current is the superposition of a triangular wave whose peak to peak ampliturde equals ΔI and an asymmetric rectangular wave whose amplitude equals $\frac{2 \cdot D \cdot I_o}{N}$ during (1-D) x Ts seconds and equals $\frac{2 \cdot (1 - D) \cdot I_o}{N}$ during D x Ts seconds. Therefore,

$$I_{pri\_RMS} := \sqrt{\left(\frac{2 \cdot D \cdot I_o}{N}\right)^2 \cdot (1 - D) + \left[\frac{2 \cdot (1 - D) \cdot I_o}{N}\right]^2 \cdot D + \frac{1}{3} \cdot \left(\frac{\Delta I}{2}\right)^2}$$

After simplifications, we obtain :

$$I_{pri\_RMS} := \sqrt{\frac{\Delta I^2}{12} + \frac{4 \cdot D \cdot (1 - D) \cdot I_o^{\,2}}{N^2}} \qquad I_{pri\_RMS} = 1.946$$

c) Calculate the losses occurring on the primary side of the converter :

With the exception of the transition periods (which are considered negligible with respect to the switching period), the primary current always flows through the transformer primary winding and through one of the primary Mosfets. Therefore, the total primary resistance consists of the transformer primary winding resistance in series with one primary Mosfet RDS_{ON}

$P_{primary} := \left(R\_pri(N) + Rds_{250}\right) \cdot I_{pri\_RMS}^{2}$ $P_{primary} = 1.151$ Watt

d) Calculate the losses in the transformer secondary winding :

The secondary current always flows through one of the secondary windings ; ttherefore :

$P_{sec} := R\_sec \cdot I_{o}^{2}$ $P_{sec} = 0.9$ Watt

e) Calculate the losses in the secondary synchronous rectifiers :

With the exception of the transition periods (which are considered negligible with respect to the switching period), the secondary current always flows through one of the secondary synchronous recitifier Mosfets. Therefore :

$P_{SR} := Rds_{053} \cdot I_{o}^{2}$ $P_{SR} = 2.048$ Watt

f) Calculate total conduction losses :

$P_{tot} := P_{primary} + P_{sec} + P_{SR}$ $P_{tot} = 4.099$ Watts

Calculate primary magnetizing inductance

The analysis carried out above yielded : $\Delta I = 5.393$ $L_{pri} := \frac{D \cdot (1 - D) \cdot Ts \cdot Vin}{\Delta I}$ $L_{pri} = 1.011 \cdot 10^{-5}$

3) DUAL ACTIVE BRIDGE

From the file "DAB2.MCD", we know that the optimum operating point lies at 300 kHz with Lleak = 8.5uH and N = 11 ; From DAB2.MCD, we extract the following parameters :

$Ipk := 2.481$ $Ivalley := 0.631$ $\Phi_{max} := 0.563$ $N := 11$

$F_s := 300 \cdot 10^3$

$$Irms_{Q1} := \sqrt{\frac{1}{3} \cdot \left(\frac{Ipk^2 + Ivalley^2}{2} + Ipk \cdot Ivalley \cdot \frac{\pi - 2 \cdot \Phi_{max}}{2 \cdot \pi} \right)} \qquad Irms_{Q1} = 1.122$$

$P_{Q1} := Rds_{250} \cdot Irms_{Q1}^2$ $P_{Q1} = 0.202$

$P_{Q3} := Rds_{053} \cdot (Irms_{Q1} \cdot N)^2$ $P_{Q3} = 1.387$

$P_{sec} := R\_sec \cdot 2 \cdot (Irms_{Q1} \cdot N)^2$ $P_{sec} = 1.219$

$P_{pri} := R\_pri(N) \cdot 2 \cdot Irms_{Q1}^2$ $P_{pri} = 0.305$

Unlike the other topologies, this one also has a primary AC inductor whose winding resistance is given by :

$$RL_{pri} := 0.005 \cdot \frac{\left(\frac{Vin}{2}\right)^2}{\left(\frac{Pout}{0.9}\right)} \qquad RL_{pri} = 0.227$$

$P_{Lpri} := RL_{pri} \cdot 2 \cdot Irms_{Q1}^2$ $P_{Lpri} = 0.573$

$P_{tot} := 2 \cdot P_{Q1} + 2 \cdot P_{Q3} + P_{pri} + P_{sec} + P_{Lpri}$ $P_{tot} = 5.274$

4) SOFT SWITCHING FLYBACK

We look for a current I_{neg_pk} that will cause the parasitic capacitances to be completely discharged.

We know : $I_o = 15$

We must have : $\frac{I_{pk} - I_{neg\_pk}}{2} \cdot (1 - D) = I_o$

The above expression suggests that we must look for a duty cycle as short as possible because the energy is transferred to the secondary during (1-D) ; so we need to "spread" the secondary current during the longest possible period of time.

Choose : $D := 0.25$

The balance of volts-microseconds across the transformer primary requires :

$D \cdot Vin = (1 - D) \cdot N \cdot (Vout + Von)$ Take : $Von := 0.2$

Therefore: $N := \frac{D \cdot Vin}{(1 - D) \cdot (Vout + Von)}$ $N = 9.524$

Take : $N := 10$

Therefore : $D := \frac{N \cdot (Vout + Von)}{N \cdot (Vout + Von) + Vin}$ $D = 0.259$

To simplify the calculations, let's assign Vout the value of Vout + Von, i.e. : $Vout := 3.5$

Calculate the primary and secondary parasitic capacitances :

$Cdso_{sec} := 2 \cdot (14.2 \cdot 10^{-9})$ $Cgdo_{sec} := 2 \cdot (223.15 \cdot 10^{-9})$ $A_{sec} := 8.074$ $\gamma_{sec} := 1.599$

$Cdso_{pri} := 3.311 \cdot 10^{-9}$ $Cgdo_{pri} := 9.186 \cdot 10^{-9}$ $A_{pri} := 2.211$ $\gamma_{pri} := 1.107$

$$C_{sec}(V) := \frac{Cgdo_{sec}}{(A_{sec} + V)^{\gamma_{sec}}} + \frac{Cdso_{sec}}{\sqrt{1 + \frac{V}{0.8}}} \qquad C_{pri}(V) := \frac{Cgdo_{pri}}{(A_{pri} + V)^{\gamma_{pri}}} + \frac{Cdso_{pri}}{\sqrt{1 + \frac{V}{0.8}}} \qquad C_{tfo} := 250 \cdot 10^{-12}$$

$$\Delta E1 := Vout\cdot\int_0^{Vout+\frac{Vin}{N}} C_{sec}(V)\,dV - Vin\cdot\int_0^{Vin+N\cdot Vout} C_{pri}(V)\,dV - \int_0^{Vout+\frac{Vin}{N}} C_{sec}(V)\cdot V\,dV \ldots$$
$$+\int_0^{Vin+N\cdot Vout} C_{pri}(V)\cdot V\,dV - \frac{1}{2}\cdot C_{tfo}\cdot Vin^2 + \frac{1}{2}\cdot C_{tfo}\cdot(N\cdot Vout)^2$$

$$\Delta E1 = -6.991\cdot 10^{-6}$$

$$\Delta E(V) := Vout\cdot\int_0^{V} C_{sec}(x)\,dx - Vin\cdot\int_{Vin+N\cdot Vout-N\cdot V}^{Vin+N\cdot Vout} C_{pri}(x)\,dx - \int_0^{V} C_{sec}(x)\cdot x\,dx \ldots$$
$$+\int_{Vin+N\cdot Vout-N\cdot V}^{Vin+N\cdot Vout} C_{pri}(x)\cdot x\,dx - \frac{1}{2}\cdot C_{tfo}\cdot(N\cdot V - N\cdot Vout)^2 + \frac{1}{2}\cdot C_{tfo}\cdot(N\cdot Vout)^2$$

$$0 < V < \frac{Vin}{N} + Vout \qquad \Delta E\left(\frac{Vin}{N} + Vout\right) = -6.991\cdot 10^{-6}$$

Flyback equations

$$M := \left|\begin{array}{l} \text{for } t \in 0..7 \\ \quad I_{neg\_pk} \leftarrow 11.9 + t \\ \quad I_{pk} \leftarrow \frac{2\cdot I_o}{1-D} + I_{neg\_pk} \\ \quad L_m \leftarrow \frac{Vout\cdot(1-D)\cdot Ts}{I_{pk}+I_{neg\_pk}} \\ \quad t_{tr} \leftarrow \int_0^{\frac{Vin}{N}+Vout} \frac{C_{sec}(V)+N^2\cdot C_{pri}(Vin+N\cdot Vout-N\cdot V)+N^2\cdot C_{tfo}}{\sqrt{2\cdot\frac{\Delta E(V)}{L_m}+I_{neg\_pk}^2}}\,dV \\ \quad M^{\langle t\rangle} \leftarrow \begin{bmatrix} I_{pk} \\ I_{neg\_pk} \\ L_m \\ t_{tr} \end{bmatrix} \\ M \end{array}\right.$$

$$M = \begin{bmatrix} 52.4 & 53.4 & 54.4 & 55.4 & 56.4 & 57.4 & 58.4 & 59.4 \\ 11.9 & 12.9 & 13.9 & 14.9 & 15.9 & 16.9 & 17.9 & 18.9 \\ 1.008\cdot10^{-7} & 9.776\cdot10^{-8} & 9.49\cdot10^{-8} & 9.22\cdot10^{-8} & 8.965\cdot10^{-8} & 8.723\cdot10^{-8} & 8.495\cdot10^{-8} & 8.278\cdot10^{-8} \\ 1.972\cdot10^{-7} & 1.45\cdot10^{-7} & 1.275\cdot10^{-7} & 1.154\cdot10^{-7} & 1.06\cdot10^{-7} & 9.824\cdot10^{-8} & 9.17\cdot10^{-8} & 8.606\cdot10^{-8} \end{bmatrix}$$

$$\begin{bmatrix} I_{pk} \\ I_{neg\_pk} \\ L_m \\ t_{tr} \end{bmatrix} := M^{<0>} \qquad \begin{bmatrix} I_{pk} \\ I_{neg\_pk} \\ L_m \\ t_{tr} \end{bmatrix} = \begin{bmatrix} 52.4 \\ 11.9 \\ 1.008\cdot10^{-7} \\ 1.972\cdot10^{-7} \end{bmatrix}$$

$$I_{end} := \sqrt{2\cdot\frac{\Delta El}{L_m} + I_{neg\_pk}^{2}} \qquad I_{end} = 1.704$$

$$\int_0^{Vout + \frac{Vin}{N}} C_{sec}(V)\,dV = 2.416\cdot10^{-7} \qquad \int_0^{Vin + N\cdot Vout} C_{pri}(V)\,dV = 9.298\cdot10^{-8}$$

$$Irms_{sec} := \sqrt{I_{pk}^{3} + I_{neg\_pk}^{3}}\cdot\sqrt{\frac{1 - D}{3\cdot(I_{pk} + I_{neg\_pk})}} \qquad Irms_{sec} = 23.642$$

$$Irms_{pri} := \frac{Irms_{sec}}{N}\cdot\sqrt{\frac{D}{1 - D}} \qquad Irms_{pri} = 1.399$$

$$P_{SR} := \frac{Rds_{053}}{2}\cdot Irms_{sec}^{2} \qquad P_{SR} = 2.543$$

$$P_{Q1} := Rds_{250}\cdot Irms_{pri}^{2} \qquad P_{Q1} = 0.313$$

$$P_{pri} := R\_pri(N)\cdot Irms_{pri}^{2} \qquad P_{pri} = 0.196$$

$$P_{sec} := R\_sec\cdot Irms_{sec}^{2} \qquad P_{sec} = 2.236$$

$$P_{tot} := P_{Q1} + P_{SR} + P_{sec} + P_{pri} \qquad P_{tot} = 5.288$$

Appendix B

A Mathematical Model of the Gate to Drain Capacitance for Power MOSFETs

MOSFET MODELS

This appendix calculates the mathematical and PSPICE models of two power MOSFETs, the IRFP250 and the FSYC053LD. The models include non-linear gate to drain capacitances. The methodology used to develop these models is described in reference [23] of the main text.

IRFP250

From the typical transfer characteristic curve of the IRFP250 at 25 Deg.C, we have :

$K := 10$ $V_{TO} := 3$ $\Theta := 0.1$ $Cox := 34 \cdot 10^{-9}$ F/cm^2 $\mu_0 := 600$ cm^2/V x sec

GIVEN

$$\frac{K \cdot (4.25 - V_{TO})^2}{1 + \Theta \cdot (4.25 - V_{TO})} = 0.75 \qquad \frac{K \cdot (5 - V_{TO})^2}{1 + \Theta \cdot (5 - V_{TO})} = 6$$

$$\frac{K \cdot (4.75 - V_{TO})^2}{1 + \Theta \cdot (4.75 - V_{TO})} = 3.2 \qquad \frac{K \cdot (6 - V_{TO})^2}{1 + \Theta \cdot (6 - V_{TO})} = 22$$

$$\begin{pmatrix} K \\ V_{TO} \\ \Theta \end{pmatrix} := \text{Minerr}(K, V_{TO}, \Theta) \qquad \begin{pmatrix} K \\ V_{TO} \\ \Theta \end{pmatrix} = \begin{pmatrix} 4.531 \\ 3.891 \\ -0.04 \end{pmatrix}$$

We will take : $\Theta := 0$ $K \cdot (6 - V_{TO})^2 = 20.159$

We know that : $K = \frac{Kp}{2} \cdot \frac{W}{L}$

Where $Kp := Cox \cdot \mu_0$ = 34nF/cm^2 x 600 cm^2/V x sec ; therefore, $Kp = 2.04 \cdot 10^{-5}$ F/V x sec

$L := 2 \cdot 10^{-6}$ for all MOSFETs

Therefore, $W := \frac{2 \cdot K \cdot L}{Kp}$ $W = 0.888$ m

Calculate Rchannel, RS and RD

Vgs := 10 $R_{ch} := \frac{1}{Kp \cdot \frac{W}{L} \cdot (Vgs - V_{TO})}$ $R_{ch} = 0.018$

Take : $RS := 15 \cdot 10^{-3}$ Then, $RD := 85 \cdot 10^{-3} - RS - R_{ch}$ $RD = 0.052$

MATHCAD MODELS OF NON-LINEAR CAPACITANCES

ANALYTICAL REPRESENTATION OF DRAIN TO SOURCE NON-LINEAR JUNCTION CAPACITANCE

$Cds0=(Coss(1V) - Crss(1V))\cdot\sqrt{2}$

$Cds0 := (4.75 - 2.6)\cdot\sqrt{2}$ $\quad Cds0 = 3.041 \ nF$ $\quad Cds(V) := \frac{Cds0}{\sqrt{1 + V}}$

ANALYTICAL REPRESENTATION OF GATE TO DRAIN NON-LINEAR CAPACITANCE

$Cgd0 := 1 \ nCb$ $\quad A := 1.5$ $\quad \gamma := 0.5$

$V1 := 1$ $\quad V2 := 2$ $\quad V3 := 4$ $\quad V4 := 10$ $\quad V5 := 25$

GIVEN

$\frac{Cgd0}{A^{\gamma}} = 3.8$ $\quad \frac{Cgd0}{(A + V1)^{\gamma}} = 2.6$ $\quad \frac{Cgd0}{(A + V2)^{\gamma}} = 1.8$ $\quad \frac{Cgd0}{(A + V3)^{\gamma}} = 1.2$ $\quad \frac{Cgd0}{(A + V4)^{\gamma}} = 0.6$ $\quad \frac{Cgd0}{(A + V5)^{\gamma}} = 0.25$

$\begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} := Minerr(Cgd0, A, \gamma)$ $\quad \begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} = \begin{pmatrix} 9.186 \\ 2.211 \\ 1.107 \end{pmatrix}$

$Cgd(V) := \frac{Cgd0}{(A + V)^{\gamma}}$ $\quad Cgd(V4) = 0.575$ $\quad \int_{40}^{160} Cgd(V)\,dV = 7.706 \ nCb$

Calculate Miller Charge

$V_{DD} := 160$ $\quad V_{plateau} := 6.45$ $\quad Rds_{on} := 0.085$ $\quad Id := 30$

From the Gate Charge Curve :

$Ciss_{on} := \frac{120 - 60}{14 - 6.45}$ $\quad Ciss_{on} = 7.947 \ nF$ $\quad Ciss_{off} := \frac{17}{6.45}$ $\quad Ciss_{off} = 2.636 \ nF$

From the Data Sheet : $Ciss_{1V} := 5.35nF$ $\quad Crss_{1V} := 2.6 \ nF$ $\quad Ciss_{20V} := 2.85nF$ $\quad Crss_{20V} := 0.3 \ nF$

$$CGS := \frac{\left(Ciss_{20V} - Crss_{20V}\right) + \left(Ciss_{1V} - Crss_{1V}\right)}{2} \qquad CGS = 2.65 \text{ nF}$$

$$Crss_{on} := Ciss_{on} - CGS \qquad Crss_{on} = 5.297 \text{ nF}$$

$$QG_{Miller} := \int_0^{V_{DD} - V_{plateau}} Cgd(V)\, dV + \frac{Crss_{on} + Cgd(0)}{2} \cdot \left(V_{plateau} - Rds_{on} \cdot Id\right)$$

$QG_{Miller} = 46.588$ nanocoulombs

PSPICE REPRESENTATION OF GATE TO DRAIN NON-LINEAR CAPACITANCE

When $V_{GD} > 0$, C_{gd} is equal to $Ciss_{on}$ - CGS ; Therefore : $Crss_{on} = 5.297$

When $V_{GD} < 0$, C_{gd} is the series combination of $Crss_{on}$ and a variable capacitance. This series combination must be determined using the capacitance Cgd analytical expression found above.
Let's first deterine the voltages Vx at the junction between $Crss_{on}$ and the variable capacitance :

$Vx1 := 1$ $Vx2 := 1$ $Vx3 := 1$ $Vx4 := 1$ $Vx5 := 1$

GIVEN

$$Vx1 = V1 - \frac{\int_0^{V1} Cgd(V)\, dV}{Crss_{on}}$$

$Vx1 := Find(Vx1)$ $Vx1 = 0.417$

GIVEN

$$Vx2 = V2 - \frac{\int_0^{V2} Cgd(V)\, dV}{Crss_{on}}$$

$Vx2 := Find(Vx2)$ $Vx2 = 1.009$

GIVEN

$$Vx3 = V3 - \frac{\int_0^{V3} Cgd(V)\,dV}{Crss_{on}}$$

$Vx3 := Find(Vx3)$ $\quad Vx3 = 2.443$

GIVEN

$$Vx4 = V4 - \frac{\int_0^{V4} Cgd(V)\,dV}{Crss_{on}}$$

$Vx4 := Find(Vx4)$ $\quad Vx4 = 7.513$

GIVEN

$$Vx5 = V5 - \frac{\int_0^{V5} Cgd(V)\,dV}{Crss_{on}}$$

$Vx5 := Find(Vx5)$ $\quad Vx5 = 21.495$

Find the new values for Cgd0, A and γ. The total charge accumulated up to Vx_n must be identical to the one accumulated by the original Cgd model up to V_n.

GIVEN

$$\int_0^{Vx1} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V1} Cgd(V)\,dV$$

$$\int_0^{Vx2} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V2} Cgd(V)\,dV$$

$$\int_0^{Vx3} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V3} Cgd(V)\,dV$$

$$\int_0^{Vx4} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V4} Cgd(V)\,dV$$

$$\int_0^{Vx5} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V5} Cgd(V)\,dV$$

$$\begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} := \text{Minerr}(Cgd0, A, \gamma) \qquad \begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} = \begin{pmatrix} 3.662 \\ 0.27 \\ 0.855 \end{pmatrix}$$

Verify that the series combination of $\frac{Cgd0}{(|A| + V)^{\gamma}}$ and $Crss_{on}$ yields the values of Cgd defined above for 0, V1 to V5.

$$\frac{Crss_{on} \cdot \frac{Cgd0}{(|A|)^{\gamma}}}{Crss_{on} + \frac{Cgd0}{(|A|)^{\gamma}}} = 3.598 \qquad \frac{Crss_{on} \cdot \frac{Cgd0}{(|A| + Vx1)^{\gamma}}}{Crss_{on} + \frac{Cgd0}{(|A| + Vx1)^{\gamma}}} = 2.584 \qquad \frac{Crss_{on} \cdot \frac{Cgd0}{(|A| + Vx2)^{\gamma}}}{Crss_{on} + \frac{Cgd0}{(|A| + Vx2)^{\gamma}}} = 1.902$$

$$\frac{Crss_{on} \cdot \frac{Cgd0}{(|A| + Vx3)^{\gamma}}}{Crss_{on} + \frac{Cgd0}{(|A| + Vx3)^{\gamma}}} = 1.205 \qquad \frac{Crss_{on} \cdot \frac{Cgd0}{(|A| + Vx4)^{\gamma}}}{Crss_{on} + \frac{Cgd0}{(|A| + Vx4)^{\gamma}}} = 0.566 \qquad \frac{Crss_{on} \cdot \frac{Cgd0}{(|A| + Vx5)^{\gamma}}}{Crss_{on} + \frac{Cgd0}{(|A| + Vx5)^{\gamma}}} = 0.25$$

The match with the initial values is excellent

The PSPICE representation of a diode reverse capacitance is : $CJ(V) = \frac{CJ0}{\left(1 - \frac{Vd}{VJ}\right)^{M}}$

From above : $M := \gamma$ $\quad VJ := |A|$

$M = 0.855$ $\quad VJ = 0.27$

$CJ0 := \frac{Cgd0}{(|A|)^{\gamma}}$ $\quad CJ0 = 11.215$

$$\frac{Crss_{on} \cdot \frac{CJ0}{\left(1 + \frac{Vx4}{VJ}\right)^{M}}}{Crss_{on} + \frac{CJ0}{\left(1 + \frac{Vx4}{VJ}\right)^{M}}} = 0.566$$

PSPICE REPRESENTATION OF DRAIN TO SOURCE NON-LINEAR DIODE JUNCTION CAPACITANCE

$CBD := 2$ $PB := 0.8$ $V1 = 1$ $V3 = 4$

GIVEN

$$\frac{CBD}{\sqrt{1 + \frac{V1}{PB}}} = 4.75 - 2.6$$

$$\frac{CBD}{\sqrt{1 + \frac{V3}{PB}}} = 2.5 - 1.2$$

$$\begin{pmatrix} CBD \\ PB \end{pmatrix} := \text{Find}(CBD, PB) \qquad \begin{pmatrix} CBD \\ PB \end{pmatrix} = \begin{pmatrix} 3.311 \\ 0.729 \end{pmatrix}$$

$$Cds(V) := \frac{CBD}{\sqrt{1 + \frac{V}{PB}}}$$

PSPICE REPRESENTATION OF GATE TO SOURCE CAPACITANCE

$Cox := Cox \cdot 10^{4}$ $Cox = 3.4 \cdot 10^{-4}$ F/m^2

$$CGS0 := \frac{CGS \cdot 10^{-9} - Cox \cdot W \cdot L}{W} \qquad CGS0 = 2.303 \cdot 10^{-9} \quad F$$

Let's now disable Cox (in PSPICE, this means making Tox = 1 , i.e. very large)

$Cox := 0$

$$CGS0 := \frac{CGS \cdot 10^{-9} - Cox \cdot W \cdot L}{W} \qquad CGS0 = 2.983 \cdot 10^{-9} \quad F$$

TRANSIT TIME OF ANTI-PARALLEL DIODE

From Data Sheet, at I_F = 30A and dI/dt = 100A/μs : $Q_{rr} := 4600 \cdot 10^{-9}$

$I_F := 30$

$dI\_dt := 100 \cdot 10^6$

$t_f := \frac{I_F}{dI\_dt}$ $\quad t_f = 3 \cdot 10^{-7}$

$t_\theta := 10 \cdot 10^{-9}$

GIVEN

$Qrr = I_F \cdot t_\theta \cdot e^{-\sqrt{\frac{t_f}{t_\theta}}}$

$t_\theta := \text{Find}(t_\theta)$ $\quad t_\theta = 3.75 \cdot 10^{-7}$

FSYC053LD

From the typical transfer characteristic curve of the FSYC053LD at 25 Deg.C, we have :

The typical transfer characteristic of the FSYC053LD is unavailable at this time

$K := 10$ $V_{TO} := 1.5$ $\Theta := 0$ $Cox = 68 \cdot 10^{-9}$ F/cm^2 $\mu_0 := 600$ cm^2/V x sec

$$\frac{K \cdot (2.25 - V_{TO})^2}{1 + \Theta \cdot (2.25 - V_{TO})} = 0.2\Omega \qquad \frac{K \cdot (2.75 - V_{TO})^2}{1 + \Theta \cdot (2.75 - V_{TO})} = 7\Omega \qquad \frac{K \cdot (3 - V_{TO})^2}{1 + \Theta \cdot (3 - V_{TO})} = 20\Omega$$

$$\frac{K \cdot (3.5 - V_{TO})^2}{1 + \Theta \cdot (3.5 - V_{TO})} = 60\Omega \qquad \frac{K \cdot (4 - V_{TO})^2}{1 + \Theta \cdot (4 - V_{TO})} = 100\Omega$$

$$\begin{pmatrix} K \\ V_{TO} \end{pmatrix} := \text{Minerr}(K, V_{TO})\Omega \qquad \begin{pmatrix} K \\ V_{TO} \\ \Theta \end{pmatrix} = \begin{pmatrix} 10 \\ 1.5 \\ 0 \end{pmatrix}$$

Calculate Rchannel, RS and RD

Take : $RS := 2 \cdot 10^{-3}$ $RD := 1.5 \cdot 10^{-3}$

From measurements, RdsON at Vgs = 5V is equal to 7.4 mΩ , RdsON at Vgs = 10V is equal to 5.2 mΩ

$V_{TO} := 1.5$ $K = 10$

GIVEN

$$\frac{1}{2 \cdot K \cdot (5 - V_{TO})} + RS + RD = 7.4 \cdot 10^{-3} \qquad \frac{1}{2 \cdot K \cdot (10 - V_{TO})} + RS + RD = 5.2 \cdot 10^{-3}$$

$$\begin{pmatrix} K \\ V_{TO} \end{pmatrix} := \text{Find}(K, V_{TO}) \qquad \begin{pmatrix} K \\ V_{TO} \end{pmatrix} = \begin{pmatrix} 33.183 \\ 1.136 \end{pmatrix} \qquad R_{ch}(Vgs) := \frac{1}{2 \cdot K \cdot (Vgs - V_{TO})}$$

We know that : $K = \frac{Kp}{2} \cdot \frac{W}{L}$

Where $Kp := Cox \cdot \mu_0$ = 68nF/cm^2 x 600 cm^2/V x sec ; therefore, $Kp = 4.08 \cdot 10^{-5}$ F/V x sec

$L := 2 \cdot 10^{-6}$ for all MOSFETs

Therefore, $W := \frac{2 \cdot K \cdot L}{Kp}$ $W = 3.253$ m

MATHCAD MODELS OF NON-LINEAR CAPACITANCES

ANALYTICAL REPRESENTATION OF DRAIN TO SOURCE NON-LINEAR JUNCTION CAPACITANCE

$$Cds0=(Coss(25V) - Crss(25V))\cdot\sqrt{1+\frac{25}{0.8}}$$

$$Cds0 := (3.9 - 1.4)\cdot\sqrt{1+\frac{25}{0.8}} \qquad Cds0 = 14.197 \quad nF \qquad Cds(V) := \frac{Cds0}{\sqrt{1+\frac{V}{0.8}}} \qquad Cds(25) = 2.5$$

PRELIMINARY CALCULATION OF CGS

From Data Sheet, CGS=Ciss(25V) - Crss(25V)

CGS := 6.2 - 1.4 nF CGS = 4.8 nF

ANALYTICAL REPRESENTATION OF GATE TO DRAIN NON-LINEAR CAPACITANCE

Cgd0 := 1 nCb A := 1

V1 := 1 V2 := 5 V3 := 10 V4 := 25

GIVEN

$$\frac{Cgd0}{A^{\gamma}} = 12.47 - CGS \qquad \frac{Cgd0}{(A+V1)^{\gamma}} = 11.8 - CGS \qquad \frac{Cgd0}{(A+V2)^{\gamma}} = 8.21 - CGS \qquad \frac{Cgd0}{(A+V3)^{\gamma}} = 6.91 - CGS$$

$$\frac{Cgd0}{(A+V4)^{\gamma}} = 5.83 - CGS$$

$$\begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} := Minerr(Cgd0, A, \gamma) \qquad \begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} = \begin{pmatrix} 223.153 \\ 8.074 \\ 1.599 \end{pmatrix}$$

$$Cgd(V) := \frac{Cgd0}{(A+V)^{\gamma}} \qquad Cgd(0) = 7.907 \qquad \int_{15}^{24} Cgd(V)\,dV = 10.172 \ nCb$$

Calculate Miller Charge

$V_{DD} := 24$ $V_{plateau} := 3.6$ $Rds_{on} := RS + RD + R_{ch}(5)$ $Rds_{on} = 7.4\cdot10^{-3}$ Id := 71

From measurements performed on 2 devices :

$Ciss_{on} := 13.3 \quad nF$ $\qquad Crss_{on} := Ciss_{on} - CGS \qquad Crss_{on} = 8.5 \quad nF$

$V_{plateau} := 5$

$$QG_{Miller} := \int_0^{V_{DD} - V_{plateau}} Cgd(V)\,dV + \frac{Crss_{on} + Cgd(0)}{2} \cdot \left(V_{plateau} - Rds_{on} \cdot Id\right)$$

$QG_{Miller} = 91.652$

PSPICE REPRESENTATION OF GATE TO DRAIN NON-LINEAR CAPACITANCE

When $V_{GD} > 0$, C_{gd} is equal to $Ciss_{on}$ - CGS ; Therefore : $\quad Crss_{on} = 8.5$

When $V_{GD} < 0$, C_{gd} is the series combination of $Crss_{on}$ and a variable capacitance. This series combination must be determined using the capacitance Cgd analytical expression found above.
Let's first deternine the voltages Vx at the junction between $Crss_{on}$ and the variable capacitance :

$Vx1 := 1 \qquad Vx2 := 1 \qquad Vx3 := 1 \qquad Vx4 := 1$

GIVEN

$$Vx1 = V1 - \frac{\int_0^{V1} Cgd(V)\,dV}{Crss_{on}}$$

$Vx1 := Find(Vx1) \qquad Vx1 = 0.153$

GIVEN

$$Vx2 = V2 - \frac{\int_0^{V2} Cgd(V)\,dV}{Crss_{on}}$$

$Vx2 := Find(Vx2) \qquad Vx2 = 1.856$

GIVEN

$$Vx3 = V3 - \frac{\int_0^{V3} Cgd(V)\,dV}{Crss_{on}}$$

$Vx3 := Find(Vx3)$ $\quad Vx3 = 5.199$

GIVEN

$$Vx4 = V4 - \frac{\int_0^{V4} Cgd(V)\,dV}{Crss_{on}}$$

$Vx4 := Find(Vx4)$ $\quad Vx4 = 17.85$

Find the new values for Cgd0, A and γ. The total charge accumulated up to Vx_n must be identical to the one accumulated by the original Cgd model up to V_n.

GIVEN

$$\int_0^{Vx1} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V1} Cgd(V)\,dV \qquad \int_0^{Vx3} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V3} Cgd(V)\,dV$$

$$\int_0^{Vx2} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V2} Cgd(V)\,dV \qquad \int_0^{Vx4} \frac{Cgd0}{(|A| + V)^{\gamma}}\,dV = \int_0^{V4} Cgd(V)\,dV$$

$$\begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} := Minerr(Cgd0, A, \gamma) \qquad \begin{pmatrix} Cgd0 \\ A \\ \gamma \end{pmatrix} = \begin{pmatrix} 10.326 \\ 0.086 \\ 0.788 \end{pmatrix}$$

Verify that the series combination of $\frac{Cgd0}{(|A| + V)^{\gamma}}$ and $Crss_{on}$ yields the values of Cgd defined above for 0, V1 to V5.

$$\frac{Crss_{on}\cdot\frac{Cgd0}{(|A|)^{\gamma}}}{Crss_{on}+\frac{Cgd0}{(|A|)^{\gamma}}}=7.599 \qquad \frac{Crss_{on}\cdot\frac{Cgd0}{(|A|+Vx1)^{\gamma}}}{Crss_{on}+\frac{Cgd0}{(|A|+Vx1)^{\gamma}}}=6.714 \qquad \frac{Crss_{on}\cdot\frac{Cgd0}{(|A|+Vx2)^{\gamma}}}{Crss_{on}+\frac{Cgd0}{(|A|+Vx2)^{\gamma}}}=3.558$$

$$\frac{Crss_{on}\cdot\frac{Cgd0}{(|A|+Vx3)^{\gamma}}}{Crss_{on}+\frac{Cgd0}{(|A|+Vx3)^{\gamma}}}=2.094 \qquad \frac{Crss_{on}\cdot\frac{Cgd0}{(|A|+Vx4)^{\gamma}}}{Crss_{on}+\frac{Cgd0}{(|A|+Vx4)^{\gamma}}}=0.943$$

The match with the initial values is excellent

The PSPICE representation of a diode reverse capacitance is : $CJ(V)=\frac{CJ0}{\left(1-\frac{Vd}{VJ}\right)^{M}}$

From above : $M := \gamma$ $\quad M = 0.788$ $\qquad VJ := |A|$ $\quad VJ = 0.086$

$$CJ0 := \frac{Cgd0}{(|A|)^{\gamma}} \qquad CJ0 = 71.732$$

$$\frac{Crss_{on}\cdot\frac{CJ0}{\left(1+\frac{0}{VJ}\right)^{M}}}{Crss_{on}+\frac{CJ0}{\left(1+\frac{0}{VJ}\right)^{M}}}=7.599$$

PSPICE REPRESENTATION OF GATE TO SOURCE CAPACITANCE

$Cox := Cox\cdot 10^{4}$ $\qquad Cox = 6.8\cdot 10^{-4}$ F/m^2

$$CGS0 := \frac{CGS\cdot 10^{-9}\cdot W\cdot L - Cox\cdot W\cdot L}{W} \qquad CGS0 = 1.155\cdot 10^{-10} \text{ F}$$

Let's now disable Cox (in PSPICE, this means making Tox = 1 , i.e. very large)

$Cox := 0$

$$CGS0 := \frac{CGS\cdot 10^{-9}\cdot W\cdot L - Cox\cdot W\cdot L}{W} \qquad CGS0 = 1.475\cdot 10^{-9} \text{ F}$$

TRANSIT TIME OF ANTI-PARALLEL DIODE

From Data Sheet, at I_F = 71A and dI/dt = 100A/μs : $Q_{rr} := 450 \cdot 10^{-9}$

$I_F := 71$

$dI\_dt := 100 \cdot 10^{6}$

$t_f := \frac{I_F}{dI\_dt}$ $\quad t_f = 7.1 \cdot 10^{-7}$

$t_\theta := 10 \cdot 10^{-9}$

GIVEN

$Q_{rr} = I_F \cdot t_\theta \cdot e^{-\sqrt{\frac{t_f}{t_\theta}}}$

$t_\theta := \text{Find}(t_\theta)$ $\quad t_\theta = 9.607 \cdot 10^{-8}$

Appendix C

Efficiency Calculation of 3.3 V Complementary Half Bridge Converter

EFFICIENCY CALCULATION OF SOFT SWITCHING COMPLEMENTARY HALF BRIDGE

$Vin_{min} := 90$ $Vin := 100$ $Vin_{max} := 110$ $Vout := 3.3$

$Pout := \frac{49.5}{1}$ $Fs := 400 \cdot 10^{3}$ $L_{pri} := 14.5 \cdot 10^{-6}$

Multiplying factor for Cpri averaging voltage : $M_{ov} := 2$

Damping resistance in series with the gate of Mosfet driven during 1-D : $R_{damp} := 0$

Number of parallel Mosfets in the 1-D branch : $Np1 := 2$

Number of parallel Mosfets in the D branch : $Np2 := 1$

IRHM7250 DATA

$Rds_{pri} := 0.1 \cdot 1.6$ $Rds_{pri} = 0.16$

$Cds0 := 3.311 \cdot 10^{-9}$ $Cgd0 := 9.186 \cdot 10^{-9}$ $A := 2.211$ $\gamma := 1.107$ $C_{tfo} := 250 \cdot 10^{-12}$

$$Coss(V) := \frac{Cds0}{\sqrt{1 + \frac{V}{0.8}}} + \frac{Cgd0}{(A + V)^{\gamma}} \qquad Cgd(V) := \frac{Cgd0}{(A + V)^{\gamma}}$$

$Ciss\_pri_{ON} := 7.947 \cdot 10^{-9}$

$C_{GS} := 2.65 \cdot 10^{-9}$

FSYC053 DATA

$Rds_{sec\_L} := 0.0073 \cdot 1.3$ $Rds_{sec\_L} = 9.49 \cdot 10^{-3}$ $Rds_{sec} := 0.0052 \cdot 1.3$ $Rds_{sec} = 6.76 \cdot 10^{-3}$

$Ciss_{L\_ON} := 13 \cdot 10^{-9}$

$RG := 0.25$

$$Coss_{sec\_L}(V) := \frac{223.15 \cdot 10^{-9}}{(8.074 + V)^{1.599}} + \frac{14.2 \cdot 10^{-9}}{\sqrt{1 + \frac{V}{0.8}}} \qquad Cgd_{sec\_L}(V) := \frac{223.15 \cdot 10^{-9}}{(8.074 + V)^{1.599}}$$

$V_D := 0.75$

BASIC PARAMETERS

$I_o := \frac{Pout}{Vout}$ $I_o = 15$ $Von := I_o \cdot (Rds_{sec\_L} + 0.005)$ $Von = 0.217$ $Ts := \frac{1}{Fs}$ $Ts = 2.5 \cdot 10^{-6}$

Choice of D = 50% when Vin = Vin_{min} = 90V

$D_{max} := 0.5$ $L\_lk := 33 \cdot 10^{-9}$

$$N := \frac{2 \cdot D_{max} \cdot (1 - D_{max}) \cdot Vin_{min}}{Vout + Von + \frac{L\_lk \cdot I_o}{Ts}} \qquad N = 12.112$$

$N := 12$

Calculate D for Vin = 100V

$D := 0.1$

GIVEN

$$Vout + Von = \frac{2 \cdot D \cdot (1 - D) \cdot Vin}{N} - \frac{L\_lk \cdot I_o}{Ts}$$

$D := Find(D)$ $\quad D = 0.335$

Calculate D_{min} for Vin = Vin_{max} = 120V

$D_{min} := 0.1$

GIVEN

$$Vout + Von = \frac{2 \cdot D_{min} \cdot (1 - D_{min}) \cdot Vin_{max}}{N} - \frac{L\_lk \cdot I_o}{Ts}$$

$D_{min} := Find(D_{min})$ $\quad D_{min} = 0.282$

Since we want to implement a Complementary Half Bridge with current doubler, we take :

$N := \frac{N}{2}$ $\quad N = 6$

The leakage inductance as seen from the primary side equals :

$L\_lk := (33 - 3.75 \cdot (Np1 + Np2 - 2)) \cdot 10^{-9} \cdot N^2$ $\quad L\_lk = 1.053 \cdot 10^{-6}$

Calculate total secondary side capacitance

$$Coss_{OFF} := \frac{1}{\frac{Vin \cdot D}{N}} \cdot \int_0^{\frac{Vin \cdot D}{N}} Coss_{sec\_L}(V)\, dV \qquad Coss_{OFF} = 1.258 \cdot 10^{-8}$$

$$C_{sec} := \frac{Np1 \cdot Ciss_{L\_ON} + Np2 \cdot Coss_{OFF}}{N^2} \qquad C_{sec} = 1.072 \cdot 10^{-9}$$

$$R_{sec} := \frac{\left(\frac{RG}{Np1} + R_{damp}\right)\cdot\left(Np1\cdot Ciss_{L\_ON}\right)^2 + \frac{RG}{Np2}\cdot\left(Np2\cdot Coss_{OFF}\right)^2}{\left(Np1\cdot Ciss_{L\_ON} + Np2\cdot Coss_{OFF}\right)^2}\cdot N^2 \qquad R_{sec} = 3.001$$

$$C_{pri} := \frac{1}{Vin\cdot D\cdot M_{ov}}\cdot\left(\int_0^{Vin\cdot D\cdot M_{ov}} Coss(V)\,dV + \int_{Vin - Vin\cdot D\cdot M_{ov}}^{Vin} Coss(V)\,dV\right) + C_{tfo}$$

$$C_{pri} = 1.732\cdot 10^{-9}$$

$$\omega_o := \frac{1}{\sqrt{\frac{L\_lk\cdot C_{pri}\cdot C_{sec}}{C_{pri} + C_{sec}}}} \qquad Q := \frac{1}{R_{sec}}\cdot\sqrt{\frac{L\_lk}{\frac{C_{pri}\cdot C_{sec}}{C_{pri} + C_{sec}}}} \qquad \omega_1 := \omega_o\cdot\sqrt{1 - \frac{1}{4\cdot Q^2}}$$

$$I_{L\_lk}(I_{pk}, t) := \frac{I_{pk}\cdot C_{sec}}{C_{pri} + C_{sec}}\cdot\left[1 - \exp\left(-\frac{R_{sec}}{2\cdot L\_lk}\cdot t\right)\cdot\left(\frac{\sin(\omega_1\cdot t)}{\sqrt{4\cdot Q^2 - 1}} + \cos(\omega_1\cdot t)\right)\right]$$

$$V_{Csec}(I_{pk}, t) := -Vin\cdot D - \frac{I_{pk}}{\left(C_{pri} + C_{sec}\right)^2}\cdot C_{pri}\cdot C_{sec}\cdot R_{sec} + \frac{I_{pk}}{C_{pri} + C_{sec}}\cdot t \ldots$$
$$+ \exp\left(-\frac{R_{sec}}{2\cdot L\_lk}\cdot t\right)\cdot\left[\frac{\sin(\omega_1\cdot t)}{\sqrt{4\cdot Q^2 - 1}}\cdot\frac{1}{\omega_o}\cdot\left(\frac{1}{Q} - 2\cdot Q\right) + \frac{\cos(\omega_1\cdot t)}{\omega_o\cdot Q}\right]\cdot\frac{I_{pk}}{C_{pri} + C_{sec}}$$

$$V_{Cpri}(I_{pk}, t) := \frac{I_{pk}}{C_{pri} + C_{sec}}\cdot t + I_{pk}\cdot\left(\frac{C_{sec}}{C_{sec} + C_{pri}}\right)^2\cdot R_{sec}\cdot\left[1 - \exp\left(-\frac{R_{sec}}{2\cdot L\_lk}\cdot t\right)\cdot\cos(\omega_1\cdot t) \ldots \right.$$
$$\left. + \frac{2\cdot Q^2 - 1}{\sqrt{4\cdot Q^2 - 1}}\cdot\exp\left(-\frac{R_{sec}}{2\cdot L\_lk}\cdot t\right)\cdot\sin(\omega_1\cdot t)\right] - Vin\cdot D$$

We now need to calculate I_{neg_pk}

$$I_{neg\_pk} := \frac{Vin \cdot D \cdot (1 - D)}{2 \cdot Fs \cdot L_{pri}} + \frac{I_o \cdot D}{N} \qquad I_{neg\_pk} = 2.76$$

$$\Delta I := \frac{Vin \cdot D \cdot (1 - D)}{L_{pri} \cdot Fs} \qquad \Delta I = 3.843$$

$$Ipri_{rms} := \sqrt{\frac{\Delta I^2}{12} + \frac{D \cdot (1 - D) \cdot I_o^{\,2}}{N^2}} \qquad Ipri_{rms} = 1.62$$

$$Isec_{rms} := \frac{I_o}{2}$$

$$t1 := 10^{-9}$$

GIVEN

$$V_{Csec}(I_{pk}, t1) + R_{sec} \cdot I_{L\_lk}(I_{pk}, t1) = 0$$

$$Answer(I_{pk}) := Find(t1)$$

$$t1 := Answer(I_{neg\_pk}) \qquad t1 = 5.409 \cdot 10^{-8}$$

$$I_{Lpri} := I_{neg\_pk} - I_{L\_lk}(I_{neg\_pk}, t1) \qquad I_{Lpri} = 1.29$$

$$V1 := if(V_{Cpri}(I_{neg\_pk}, t1) + Vin \cdot D > Vin, Vin, V_{Cpri}(I_{neg\_pk}, t1) + Vin \cdot D) \qquad V1 = 68.19 \qquad V2 := Vin$$

We now calculate the current through L_lk at the end of the voltage transition, assuming that the transition takes place in 2 steps ; for this first calculation we assign to V2 a value equal to Vin. If the current value is less than 2 x Io/N, the assumption is validated. If not, we must redo the calculation by assigning a current value through L_lk equal to 2 x Io/N and calculating V2.

$$X := \int_{V1}^{V2} Coss(V) \cdot V \, dV + \int_{Vin - V1}^{Vin - V2} Coss(V) \cdot V \, dV - D \cdot Vin \cdot \int_{V1}^{V2} Coss(V) \, dV \ldots$$
$$+ \frac{1}{2} \cdot C_{tfo} \cdot \left[(V2 - D \cdot Vin)^2 - (V1 - D \cdot Vin)^2 \right] - (1 - D) \cdot Vin \cdot \int_{Vin - V1}^{Vin - V2} Coss(V) \, dV$$

We now need to find the roots of the following polynomial : $\frac{1}{2}\cdot L\_lk\cdot(I)^2 - L\_lk\cdot I_{Lpri}\cdot I + X = 0$

$$I := \text{if}\left[\left(I_{Lpri}\right)^2 - 2\cdot\frac{X}{L\_lk} < 0,\ I_{Lpri},\ I_{Lpri} - \sqrt{\left(I_{Lpri}\right)^2 - 2\cdot\frac{X}{L\_lk}}\right]$$

GIVEN

$$\frac{1}{2}\cdot L\_lk\cdot(x)^2 - L\_lk\cdot y\cdot x + \left[\begin{array}{l}\displaystyle\int_{V1}^{V2} Coss(V)\cdot V\,dV + \int_{Vin-V1}^{Vin-V2} Coss(V)\cdot V\,dV - D\cdot Vin\cdot\int_{V1}^{V2} Coss(V)\,dV \ldots \\ \displaystyle +\frac{1}{2}\cdot C_{tfo}\cdot\left[(V2 - D\cdot Vin)^2 - (V1 - D\cdot Vin)^2\right] - (1 - D)\cdot Vin\cdot\int_{Vin-V1}^{Vin-V2} Coss(V)\,dV\end{array}\right] = 0$$

$Ans(x,y) := Find(V2)$

$V2 := Ans\left(I, I_{Lpri}\right)$ $\qquad V2 = 82.146$

$$F(V) := \int_{V1}^{V} Coss(x)\cdot x\,dx + \int_{Vin-V1}^{Vin-V} Coss(x)\cdot x\,dx - D\cdot Vin\cdot\int_{V1}^{V} Coss(x)\,dx \ldots$$
$$+\frac{1}{2}\cdot C_{tfo}\cdot\left[(V - D\cdot Vin)^2 - (V1 - D\cdot Vin)^2\right] - (1 - D)\cdot Vin\cdot\int_{Vin-V1}^{Vin-V} Coss(x)\,dx$$

$$t2 := \int_{V1}^{V2-0.5} \frac{Coss(V) + Coss(Vin - V) + C_{tfo}}{\sqrt{\left(I_{Lpri}\right)^2 - \frac{2\cdot F(V)}{L\_lk}}}\,dV \qquad t2 = 2.487\cdot10^{-8}$$

$$t1 + t2 = 7.896\cdot10^{-8}$$

Due to additional delay in the turn-on of the upper transistor : $V2 := V2 - 8\square$

1) Conduction losses in primary transistors

$$P_{Qpri\_cond} := Rds_{pri} \cdot Ipri_{rms}^{2} \qquad P_{Qpri\_cond} = 0.42$$

2) Switching losses in primary transistors

$$P_{Qpri\_swit} := \left[\int_{0}^{Vin - V2} \left(Coss(V) + Coss(Vin - V) + C_{tfo} \right) \cdot V \, dV \right] \cdot Fs \qquad P_{Qpri\_swit} = 0.133$$

3) Gate losses in primary transistors

Due to the resonant nature of the gate charge, almost no dissipation occurs on transistor turn-on ; therefore, all the gate dissipation occurs during the turn-off ; we shall assume that the gate discharge process is powerful enough so as to completely discharge the gate capacitance from V_{Logic} to zero before the drain to source voltage starts to rise ; therefore :

$$P_{Qpri\_gate} := 2 \cdot Fs \cdot \left(0.66 \cdot Ciss\_pri_{ON} \cdot V_{Logic}^{2} + 0.66 \cdot V_{Logic} \cdot \int_{0}^{Vin - V2} Cgd(V) \, dV \right) \qquad P_{Qpri\_gate} = 0.709$$

4) Losses in primary capacitor bridge

$ESR := 0.1$ (For 1 capacitor)

$$P_{Cap} := ESR \cdot Ipri_{rms}^{2} \qquad P_{Cap} = 0.262$$

5) Conduction losses in secondary MOSFETs

The secondary MOSFETs conduct most of the switching period as transistors ; but, during the current transfer from one Sync Rect to the other (whose duration is deternined by the leakage inductance), only their body-drain diodes conduct. We must therefore determine the duration of the overlap.

$$L\_lk := (33 - 3.75 \cdot (Np1 + Np2 - 2)) \cdot 10^{-9} \qquad L\_lk = 2.925 \cdot 10^{-8}$$

It can be shown that :

$$t_{ov1} := \frac{N \cdot L\_lk \cdot I_o \cdot 1.5}{(1 - D) \cdot Vin} \qquad t_{ov1} = 5.942 \cdot 10^{-8} \qquad t_{ov2} := \frac{N \cdot L\_lk \cdot I_o \cdot 1.5}{D \cdot Vin} \qquad t_{ov2} = 1.177 \cdot 10^{-7}$$

t_{ov} is the sum of t_{ov1} and t_{ov2} and is equal to :

$$t_{ov} := \frac{N \cdot L\_lk \cdot I_o \cdot 1.5}{D \cdot (1 - D) \cdot Vin} \qquad t_{ov} = 1.771 \cdot 10^{-7}$$

Therefore :

$$P_{Qsec\_cond} := \frac{\left(D \cdot Ts - t_{ov1}\right) \cdot \frac{Rds_{sec}}{Np2} \cdot I_o^{\,2} + \left[(1 - D) \cdot Ts - t_{ov2}\right] \cdot \frac{Rds_{sec\_L} \cdot I_o^{\,2}}{Np1} + t_{ov} \cdot V_D \cdot I_o}{Ts} \qquad P_{Qsec\_cond} = 1.93$$

6) Switching losses in secondary MOSFETs

These consist of :
a) Gate losses during the turn-off of the Sync rectifiers
b) Gate losses during the turn-on of the Sync rectifiers
c) Reverse recovery losses

Gate losses during turn-on result from a soft transition ; let's estimate this transition

$t_{fall\_1} := tl$ at the end of the 1-D period ; $t_{fall\_2} := t_{fall\_1} \cdot 0.5$ at the end of the D period ;

$$Cgd_1 := \frac{Np2}{\frac{D \cdot Vin}{N}} \cdot \int_0^{\frac{Vin \cdot D}{N}} Cgd_{sec\_L}(V)\, dV \qquad Cgd_2 := \frac{Np1}{\frac{(1 - D) \cdot Vin}{N}} \cdot \int_0^{\frac{Vin \cdot (1 - D)}{N}} Cgd_{sec\_L}(V)\, dV$$

$$RC_1 := \left(R_{damp} + \frac{RG}{Np1}\right) \cdot \left(Np1 \cdot Ciss_{L\_ON}\right) \qquad RC_2 := \frac{RG}{Np2} \cdot Cgd_1$$

$$RC_3 := RG \cdot Ciss_{L\_ON} \qquad RC_4 := \left(R_{damp} + \frac{RG}{Np1}\right) \cdot Cgd_2$$

$$P_{Qsec\_1} := RC_1 \cdot \left(\frac{Vin \cdot D}{N \cdot t_{fall\_1}}\right)^2 \cdot \left[t_{fall\_1} - RC_1 \cdot \left(1 - e^{\frac{-t_{fall\_1}}{RC_1}}\right)\right] \cdot Np1 \cdot Ciss_{L\_ON} \cdot Fs$$

$$P_{Qsec\_2} := RC_2 \cdot \left(\frac{Vin \cdot D}{N \cdot t_{fall\_1}}\right)^2 \cdot \left[t_{fall\_1} - RC_2 \cdot \left(1 - e^{\frac{-t_{fall\_1}}{RC_2}}\right)\right] \cdot Cgd_1 \cdot Fs$$

$$P_{Qsec\_3} := RC_3 \cdot \left[\frac{Vin \cdot (1 - D)}{N \cdot t_{fall\_2}}\right]^2 \cdot \left[t_{fall\_2} - RC_3 \cdot \left(1 - e^{\frac{-t_{fall\_2}}{RC_3}}\right)\right] \cdot Np2 \cdot Ciss_{L\_ON} \cdot Fs$$

$$P_{Qsec\_4} := RC_4 \cdot \left[\frac{Vin \cdot (1 - D)}{N \cdot t_{fall\_2}}\right]^2 \cdot \left[t_{fall\_2} - RC_4 \cdot \left(1 - e^{\frac{-t_{fall\_2}}{RC_4}}\right)\right] \cdot Cgd_2 \cdot Fs$$

$$P_{Qsec\_off} := P_{Qsec\_1} + P_{Qsec\_2} + P_{Qsec\_3} + P_{Qsec\_4} \qquad P_{Qsec\_off} = 0.101$$

Gate losses during turn-on :

$$P_{Qsec\_on} := \left[\frac{1}{2}\cdot Np1\cdot Ciss_{L\_ON}\cdot\left(\frac{D\cdot Vin}{N}\right)^2 + \frac{1}{2}\cdot Np2\cdot Ciss_{L\_ON}\cdot\left[\frac{(1-D)\cdot Vin}{N}\right]^2 \ldots \right.$$
$$+ Np2\cdot\frac{D\cdot Vin}{N}\cdot\int_0^{\frac{Vin\cdot D}{N}} Coss_{sec\_L}(V)\,dV - Np2\cdot\int_0^{\frac{Vin\cdot D}{N}} Coss_{sec\_L}(V)\cdot V\,dV \ldots$$
$$\left. + Np1\cdot\frac{(1-D)\cdot Vin}{N}\cdot\int_0^{\frac{Vin\cdot(1-D)}{N}} Coss_{sec\_L}(V)\,dV - Np1\cdot\int_0^{\frac{Vin\cdot(1-D)}{N}} Coss_{sec\_L}(V)\cdot V\,dV \right]\cdot Fs$$

$P_{Qsec\_on} = 1.149$

Reverse recovery losses can be viewed as the dissipation of the excess energy stored in the leakage inductance ; we know that the total current transition typically equals 1.3 x I_o ; therefore,

$P_{Qsec\_RR} := L\_lk\cdot(0.5\cdot I_o)^2\cdot Fs$ $\quad$ $P_{Qsec\_RR} = 0.658$

7) Losses in main power transformer

Transformer data :

Copper trace width : $x := 5.08 \cdot 10^{-3}$

Number of secondary layers : $N_{sec} := 4$

PCB thickness : $t := 2.5 \cdot 10^{-3}$

Core center leg width : $l := 4 \cdot 10^{-3}$

Core length : $L := 17.5 \cdot 10^{-3}$

Core height : $h := 7.5 \cdot 10^{-3}$

3F3 material constants :

$$\begin{pmatrix} K \\ \alpha \\ \beta \end{pmatrix} := \text{if}\left[Fs \le 10^5, \begin{pmatrix} 1.0097 \cdot 10^{-2} \\ 1.8694 \\ 2.8536 \end{pmatrix}, \text{if}\left[Fs \le 2 \cdot 10^5, \begin{pmatrix} 8.4886 \cdot 10^{-3} \\ 1.8694 \\ 3.0875 \end{pmatrix}, \text{if}\left[Fs < 4 \cdot 10^5, \begin{pmatrix} 8.3427 \cdot 10^{-3} \\ 1.8694 \\ 2.8026 \end{pmatrix}, \text{if}\left[Fs \le 4 \cdot 10^5, \begin{pmatrix} 8.1994 \cdot 10^{-3} \\ 1.8694 \\ 2.544 \end{pmatrix}, \begin{pmatrix} 6.12 \cdot 1 \\ 2.3 \\ 2.4 \end{pmatrix}\right]\right]\right]$$

$$\begin{pmatrix} K \\ \alpha \\ \beta \end{pmatrix} = \begin{pmatrix} 8.1994 \cdot 10^{-3} \\ 1.8694 \\ 2.544 \end{pmatrix}$$

$$K1 := K \cdot \frac{10^{\beta}}{1000^{\alpha}} \cdot 1000 \qquad K1 = 7.073 \cdot 10^{-3}$$

Calculate core losses :

$$P_{core} := K1 \cdot \left[\frac{D \cdot (1 - D) \cdot Vin}{2 \cdot N}\right]^{\beta} \cdot Fs^{\alpha - \beta} \cdot l^{1 - \beta} \cdot L^{1 - \beta} \cdot (2 \cdot t + 2 \cdot x + 2 \cdot l + 0.007) \qquad P_{core} = 0.446$$

Calculate copper losses :

Calculation of copper losses in the transformer is very complex and necessitates the calculation of current harmonics. Practical measurements have shown that the primary winding AC resistance behaves differently whether the secondary is open or short. Therefore, two different AC resistance curves have been established : One for the open case and the other for the short case.
We will use the secondary open AC resistance for the magnetizing current (not transferred to the secondary) and the secondary short AC resistance for the load current.

Define high frequency AC resistance correction curves :
The correction curves corresponding respectively to the secondary open and the secondary shorted are :

$$k_o(f) := 1 + 7.216 \cdot 10^{-3} \cdot f^{0.462} \qquad k_s(f) := 1 + 0.077 \cdot f^{0.241}$$

a) Calculate fundamental and harmonics of primary load current

$$Ts := \frac{1}{Fs} \qquad Ts = 2.5 \cdot 10^{-6} \qquad n := 1 .. 8$$

$$a_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[-(1-D)\cdot\frac{I_o}{N}\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt + \frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left(D\cdot\frac{I_o}{N}\right)\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$b_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[-(1-D)\cdot\frac{I_o}{N}\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt + \frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left(D\cdot\frac{I_o}{N}\right)\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$IL_n := \sqrt{(a_n)^2 + (b_n)^2}$$

b) Calculate fundamental and harmonics of primary magnetizing current

$$a_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[\frac{(1-D)\cdot Vin}{L_{pri}}\cdot\left(\frac{D\cdot Ts}{2} - t\right)\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt \ldots$$
$$+\frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left[\frac{D\cdot Vin}{L_{pri}}\cdot\left(t - \frac{1+D}{2}\cdot Ts\right)\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$b_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[\frac{(1-D)\cdot Vin}{L_{pri}}\cdot\left(\frac{D\cdot Ts}{2} - t\right)\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt \ldots$$
$$+\frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left[\frac{D\cdot Vin}{L_{pri}}\cdot\left(t - \frac{1+D}{2}\cdot Ts\right)\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$Im_n := \sqrt{(a_n)^2 + (b_n)^2}$$

We know that the primary winding is made up of N layers in series whereas the secondary is made of Nsec layers in //.

$$R_{layer} = \frac{\rho}{z}\cdot\frac{2\cdot l + 2\cdot L + 4\cdot x + 0.01}{x}$$

Where z is the copper thickness corresponding to 2 ounces of copper, i.e. $71.12\cdot10^{-6}$ m.
ρ is the copper resistivity at 80 Deg. C

$$\rho := 1.72 \cdot 10^{-8} \cdot \frac{234.5 + 80}{254.5} \qquad \rho = 2.126 \cdot 10^{-8}$$

$$z := 2 \cdot 1.4 \cdot 10^{-3} \cdot 25.4 \cdot 10^{-3} \qquad z = 7.112 \cdot 10^{-5}$$

Let's now calculate the copper losses ; it should be noted that the correction factors calculated above include the secondary winding resistance ; the latter shall not be included in the calculation.

$$R_{pri\_DC} := \frac{\rho}{z} \cdot \frac{2 \cdot l + 2 \cdot L + 4 \cdot x + 0.01}{\frac{2}{N} \cdot \left[x - \left(\frac{N}{2} - 1 \right) \cdot 0.254 \cdot 10^{-3} \right]} \cdot \frac{N}{3} + 0.004 \qquad R_{pri\_DC} = 0.033$$

$$R_{sec\_DC} := \frac{\rho}{z} \cdot \frac{2 \cdot l + 2 \cdot L + 4 \cdot x + 0.01}{x} \cdot \frac{1}{4} \qquad R_{sec\_DC} = 1.078 \cdot 10^{-3}$$

$$P_{wdg} := R_{pri\_DC} \cdot \left[\sum_n k_o(n \cdot Fs) \cdot \frac{(Im_n)^2}{2} + \sum_n k_s(n \cdot Fs) \cdot \frac{(IL_n)^2}{2} \right] \qquad P_{wdg} = 0.28$$

8) Losses in output inductors

$R_{Lout} := 1 \cdot 10^{-3}$

$P_{Lout} := 2 \cdot R_{Lout} \cdot \left(\frac{I_o}{2}\right)^2$ $\quad P_{Lout} = 0.113$

9) Losses in intput inductors

Calculate I_{dc} : $\quad I_{dc} := D \cdot (1 - D) \cdot \frac{I_o}{N}$ $\quad I_{dc} = 0.557$

$R_{Lin} := 150 \cdot 10^{-3}$

$P_{Lin} := 2 \cdot R_{Lin} \cdot I_{dc}^2$ $\quad P_{Lin} = 0.093$

10) Losses in input filter second stage damping resistor

We need to calculate the RMS value of the DC ripple voltage ;

The expression of the current through capacitor C1 (in parallel with the MOSFET which is ON during DTs equals :

$I_{C1}(t) = -(1 - D) \cdot \frac{I_o}{N} + \frac{(1 - D) \cdot Vin}{L_{pri}} \cdot \left(\frac{D \cdot Ts}{2} - t\right) + I_{dc}$ $\quad$ For $0 < t < DTs$

$I_{C1}(t) = I_{dc}$ $\quad$ For $DTs < t < Ts$

Therefore : $\quad I_{C1}(t) := \text{if}\left[t < D \cdot Ts, -(1 - D) \cdot \frac{I_o}{N} + \frac{(1 - D) \cdot Vin}{L_{pri}} \cdot \left(\frac{D \cdot Ts}{2} - t\right) + I_{dc}, I_{dc}\right]$

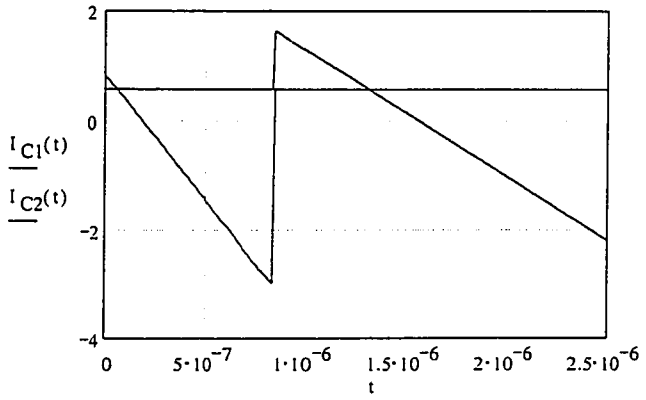
The expression of the current through capacitor C2 (in parallel with the MOSFET which is ON during (1-D) Ts equals :

$I_{C2}(t) = I_{dc}$ $\quad$ For $0 < t < DTs$

$I_{C2}(t) = -D \cdot \frac{I_o}{N} + \frac{D \cdot Vin}{L_{pri}} \cdot \left[\frac{(1 + D) \cdot Ts}{2} - t\right] + I_{dc}$ $\quad$ For $DTs < t < Ts$

Therefore : $\quad I_{C2}(t) := \text{if}\left[t < D \cdot Ts, I_{dc}, -D \cdot \frac{I_o}{N} + \frac{D \cdot Vin}{L_{pri}} \cdot \left[\frac{(1 + D) \cdot Ts}{2} - t\right] + I_{dc}\right]$

$t := 0, 10 \cdot 10^{-9} .. Ts$



Calculate the RMS ripple voltage across the series combination of C1 and C2:

$C1 := 0.82\cdot10^{-6}$ $C2 := 0.82\cdot10^{-6}$

$$V_{pri\_rms} := \sqrt{\frac{1}{Ts}\cdot\int_0^{Ts}\left(\frac{1}{C1}\cdot\int_0^t I_{C1}(x)\,dx + \frac{1}{C2}\cdot\int_0^t I_{C2}(x)\,dx\right)^2 dt} \qquad V_{pri\_rms} = 0.45$$

$R_{damp} := 12$

$$P_{Rdamp} := \frac{V_{pri\_rms}^2}{R_{damp}} \qquad P_{Rdamp} = 0.017$$

11) Losses due to interconnections

$R_{contact} := 10^{-3}\cdot(10 - 2\cdot Np1 - 2\cdot Np2)$ $R_{contact} = 4\cdot10^{-3}$

$P_{contact} := R_{contact}\cdot I_o^2$ $P_{contact} = 0.9$

12) Losses in the control circuit

The gate drive losses have already been estimated above (3) ; therefore, only the quiescent current will be taken into account.

$I_{Logic} \equiv 0.045$ $V_{Logic} \equiv 12$ $P_{Logic} := V_{Logic}\cdot I_{Logic}$ $P_{Logic} = 0.54$

TOTAL LOSSES :

$$Q_{tot} := P_{Qpri\_cond} + P_{Qpri\_swit} + P_{Qpri\_gate} + P_{Cap} + P_{Qsec\_cond} + P_{Qsec\_on} + P_{Qsec\_off} + P_{Qsec\_RR} \cdots + P_{core} + P_{wdg} + P_{Lout} + P_{Lin} + P_{Rdamp} + P_{contact} + P_{Logic}$$

$Q_{tot} = 7.752$ Watts

EFFICIENCY :

$$\eta := \frac{Pout}{Pout + Q_{tot}} \cdot 100 \qquad \eta = 86.46 \quad \%$$

Calculated and measured efficiencies at Io = 5A and 1 MOSFET in each branch :

$i := 1..4$ $\quad f_i := 200 + (i - 1)\cdot 100$

$\eta = 86.46$

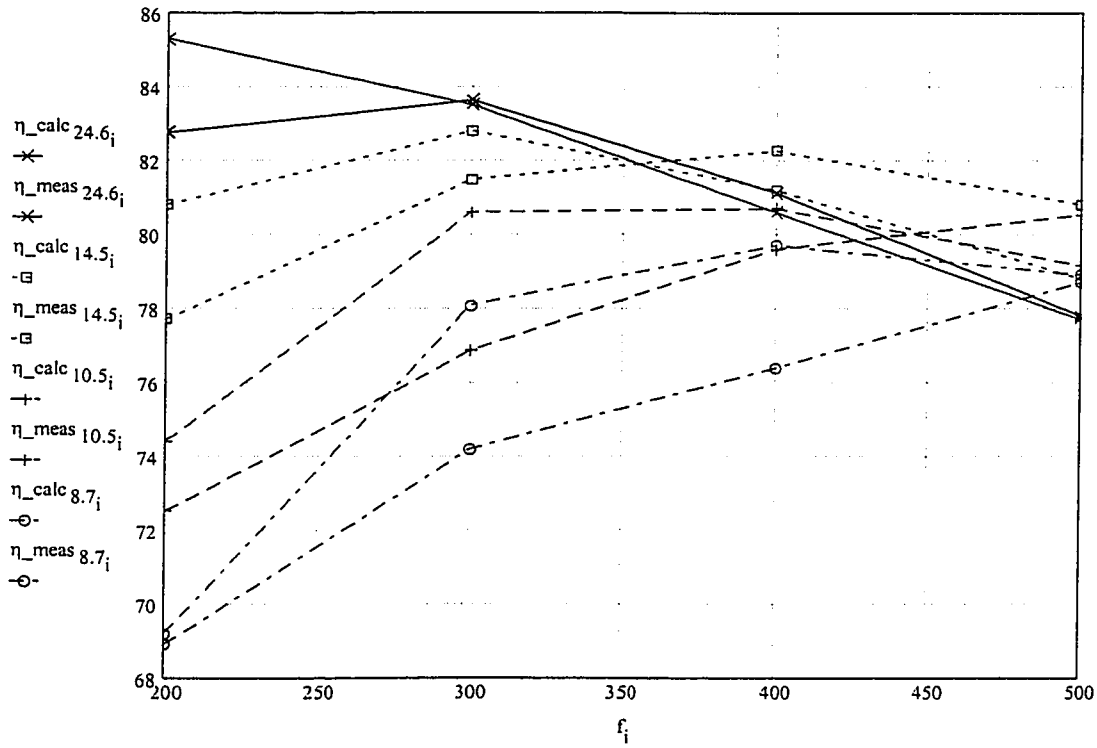
$$\eta_{calc} := \begin{bmatrix} 85.3 & 80.8 & 74.4 & 69.2 \\ 83.5 & 82.8 & 80.6 & 78.1 \\ 80.6 & 81.2 & 80.7 & 79.7 \\ 77.7 & 78.8 & 79.15 & 78.9 \end{bmatrix} \qquad \eta_{meas} := \begin{bmatrix} 82.75 & 77.7 & 72.5 & 68.9 \\ 83.63 & 81.49 & 76.86 & 74.2 \\ 81.13 & 82.26 & 79.6 & 76.39 \\ 77.8 & 80.81 & 80.53 & 78.7 \end{bmatrix}$$

$\eta\_calc_{24.6} := \eta_{calc}^{<1>}$ $\qquad \eta\_meas_{24.6} := \eta_{meas}^{<1>}$

$\eta\_calc_{14.5} := \eta_{calc}^{<2>}$ $\qquad \eta\_meas_{14.5} := \eta_{meas}^{<2>}$

$\eta\_calc_{10.5} := \eta_{calc}^{<3>}$ $\qquad \eta\_meas_{10.5} := \eta_{meas}^{<3>}$

$\eta\_calc_{8.7} := \eta_{calc}^{<4>}$ $\qquad \eta\_meas_{8.7} := \eta_{meas}^{<4>}$



Calculated and measured efficiencies at Io = 15A and 1 MOSFET in each branch :

$\eta = 86.46$

$$\eta_{calc} := \begin{bmatrix} 87.7 & 85.8 & 83.2 & 80.9 \\ 86.8 & 86.2 & 85.1 & 84 \\ 85.5 & 85.4 & 85 & 84.4 \\ 84.1 & 84.3 & 84.2 & 83.9 \end{bmatrix}$$

$$\eta_{meas} := \begin{bmatrix} 87.5 & 85.69 & 83.21 & 81.3 \\ 86.97 & 86.19 & 84.59 & 83.73 \\ 85.7 & 85.42 & 84.37 & 83.58 \\ 84.44 & 84.62 & 83.8 & 83.51 \end{bmatrix}$$

$\eta\_calc_{24.6} := \eta_{calc}^{<1>}$

$\eta\_calc_{14.5} := \eta_{calc}^{<2>}$

$\eta\_calc_{10.5} := \eta_{calc}^{<3>}$

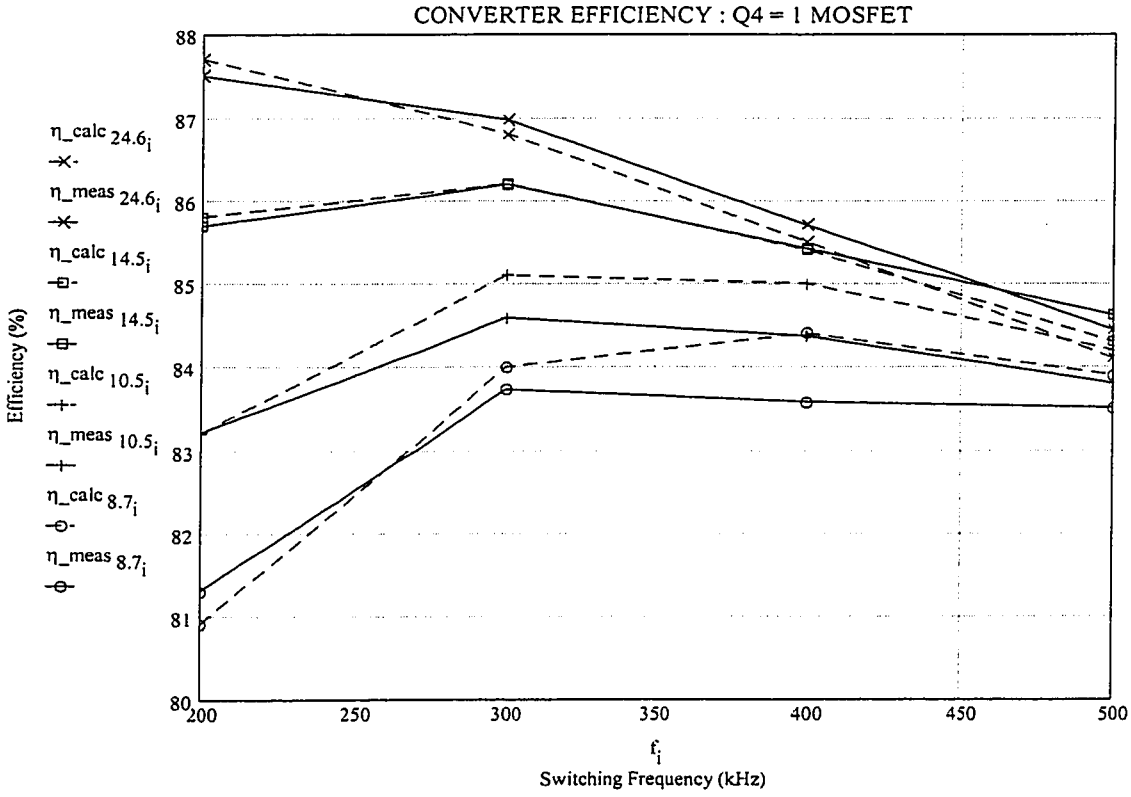
$\eta\_calc_{8.7} := \eta_{calc}^{<4>}$

$\eta\_meas_{24.6} := \eta_{meas}^{<1>}$

$\eta\_meas_{14.5} := \eta_{meas}^{<2>}$

$\eta\_meas_{10.5} := \eta_{meas}^{<3>}$

$\eta\_meas_{8.7} := \eta_{meas}^{<4>}$



Calculated and measured efficiencies at Io = 15A and 2 MOSFETs in the 1-D branch :

$\eta = 86.46$

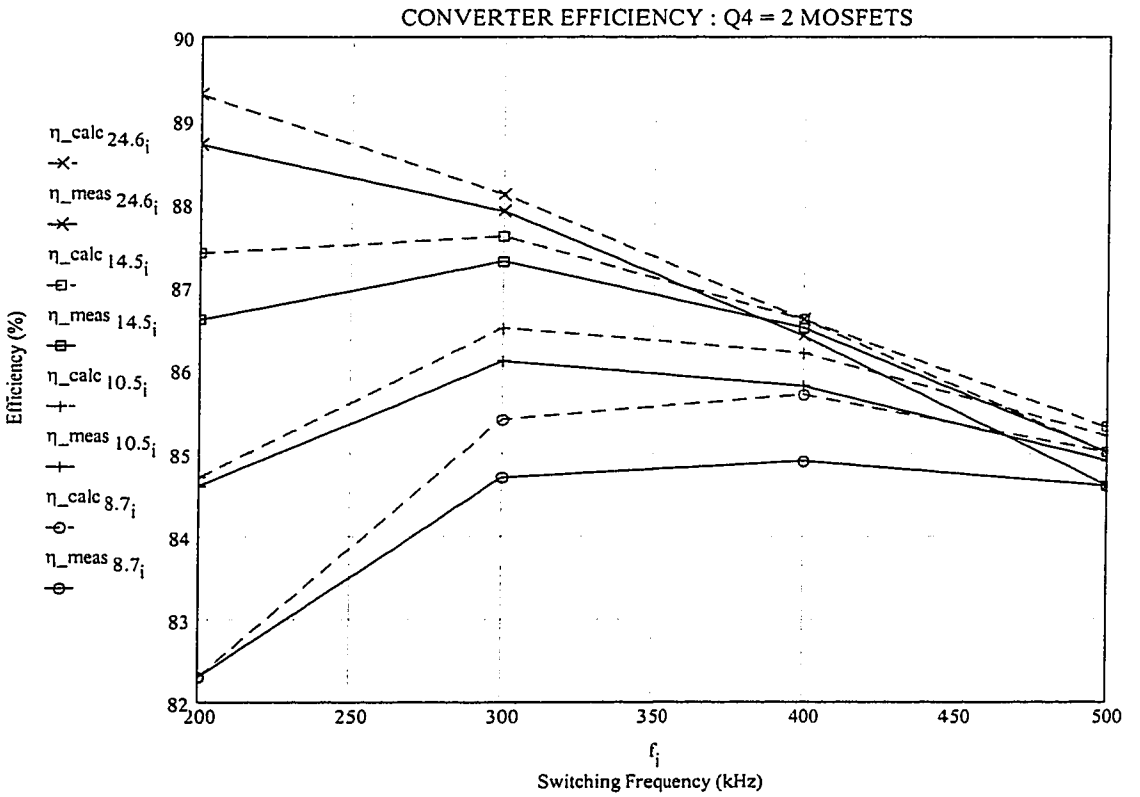
$$\eta_{calc} := \begin{bmatrix} 89.3 & 87.4 & 84.7 & 82.3 \\ 88.1 & 87.6 & 86.5 & 85.4 \\ 86.6 & 86.6 & 86.2 & 85.7 \\ 85 & 85.3 & 85.2 & 85 \end{bmatrix} \qquad \eta_{meas} := \begin{bmatrix} 88.7 & 86.6 & 84.6 & 82.3 \\ 87.9 & 87.3 & 86.1 & 84.7 \\ 86.4 & 86.5 & 85.8 & 84.9 \\ 84.6 & 85 & 84.9 & 84.6 \end{bmatrix}$$

$\eta\_calc_{24.6} := \eta_{calc}^{<1>}$ $\qquad \eta\_meas_{24.6} := \eta_{meas}^{<1>}$

$\eta\_calc_{14.5} := \eta_{calc}^{<2>}$ $\qquad \eta\_meas_{14.5} := \eta_{meas}^{<2>}$

$\eta\_calc_{10.5} := \eta_{calc}^{<3>}$ $\qquad \eta\_meas_{10.5} := \eta_{meas}^{<3>}$

$\eta\_calc_{8.7} := \eta_{calc}^{<4>}$ $\qquad \eta\_meas_{8.7} := \eta_{meas}^{<4>}$



Appendix D

Size optimization of 3.3 V Complementary Half Bridge Converter

DETERMINE EPC OPTIMUM FREQUENCY OF OPERATION

Statement of the problem : For a given switching frequency, find the minimum volume and the minimum area of magnetics which will lead to a given total magnetics power loss.

$Io := 15$ $Vin := 100$ $Fs := 400 \cdot 10^{3}$ $D := 0.1$ $N := 6$

$Vout := 3.3$ $Vin_{min} := 90$ $D_{min} := 0.1$

$Von := 0.2$ $Vin_{max} := 110$ $D_{max} := 0.1$ $L\_lk := 33 \cdot 10^{-9}$

Calculate Dmax, Dmin and D

GIVEN

$$Vout + Von = \frac{D_{max} \cdot (1 - D_{max}) \cdot Vin_{min}}{N} - L\_lk \cdot Io \cdot Fs$$

$D_{max} := \text{Find}(D_{max})$ $D_{max} = 0.441$

GIVEN

$$Vout + Von = \frac{D_{min} \cdot (1 - D_{min}) \cdot Vin_{max}}{N} - L\_lk \cdot Io \cdot Fs$$

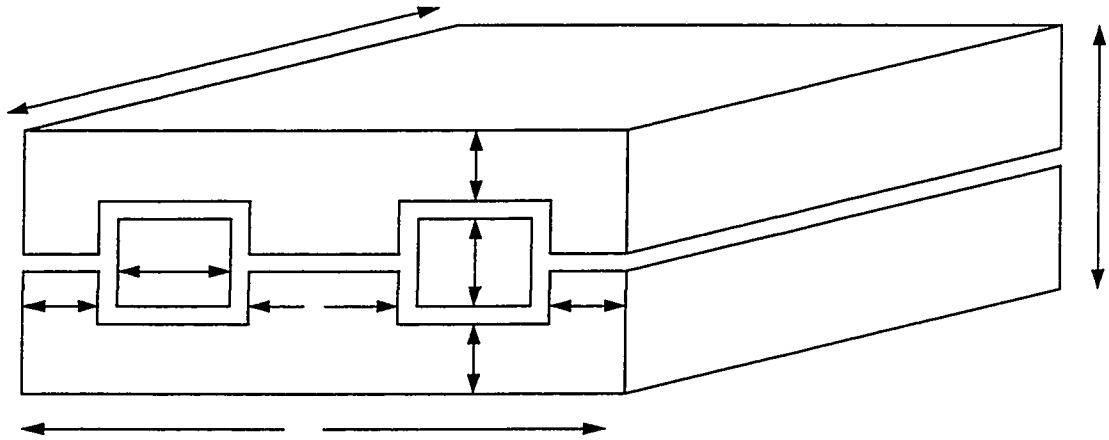
$D_{min} := \text{Find}(D_{min})$ $D_{min} = 0.28$

GIVEN

$$Vout + Von = \frac{D \cdot (1 - D) \cdot Vin}{N} - L\_lk \cdot Io \cdot Fs$$

$D := \text{Find}(D)$ $D = 0.332$

Let's now define the magnetic core parameters : Shape, dimensions and type of material



Magnetic cores material : Philips 3F3

$K := 97 \cdot 10^{-6}$ $\alpha := 2.569$ $\beta := 2.307$

$K1 := K \cdot \frac{10^{\beta}}{1000^{\alpha}} \cdot 1000$ $K1 = 3.862 \cdot 10^{-7}$

We will keep the height of all the magnetics constant and equal to 10 mm

$h := 0.01$

The PCB thickness is fixed and equal to 2.5 mm.

$t := 0.0025$

Therefore, the center leg width is equal to (allow a 1 mm clearance in window height) : $l := h - t - 0.001$

$l = 6.5 \cdot 10^{-3}$

A) Power transformer

In a previous spreadsheet, it has been determined that the value of primary peak current that will lead to ZVS at Io = 15A equals 2.8 Amps ; let's calculate the corresponding Lpri

$Ipk := 2.8$

Starting from : $\Delta I = 2 \cdot Imin + 2 \cdot \frac{Io}{N} \cdot (1 - D)$

$Ipk = Imin + \frac{Io}{N}$

$\Delta I = \frac{Vin \cdot D \cdot (1 - D)}{Lpri \cdot Fs}$

We obtain :

$Lpri := \frac{1}{Fs} \cdot \frac{Vin \cdot D \cdot (1 - D)}{2 \cdot Ipk - 2 \cdot \frac{Io}{N} \cdot D}$ $\quad Lpri = 1.408 \cdot 10^{-5}$

$\Delta I := \frac{Vin \cdot D \cdot (1 - D)}{Lpri \cdot Fs}$

$$Ipri_{rms} := \sqrt{\frac{\Delta I^2}{12} + \frac{D\cdot(1 - D)\cdot Io^2}{N^2}} \qquad Ipri_{rms} = 1.637$$

$$Isec_{rms} := \frac{Io}{2}$$

Calculation of copper losses in the transformer is very complex and necessitates the calculation of current harmonics. Practical measurements have shown that the primary winding AC resistance behaves differently whether the secondary is open or short. Therefore, two different AC resistance curves have been established : One for the open case and the other for the short case.
We will use the secondary open AC resistance for the magnetizing current (not transferred to the secondary) and the secondary short AC resistance for the load current.

a) Calculate fundamental and harmonics of primary load current

$$Ts := \frac{1}{Fs} \qquad Ts = 2.5\cdot 10^{-6} \qquad n := 1..8$$

$$a_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[-(1 - D)\cdot\frac{Io}{N}\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt + \frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left(D\cdot\frac{Io}{N}\right)\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$b_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[-(1 - D)\cdot\frac{Io}{N}\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt + \frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left(D\cdot\frac{Io}{N}\right)\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$IL_n := \sqrt{(a_n)^2 + (b_n)^2}$$

b) Calculate fundamental and harmonics of primary magnetizing current

$$a_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[\frac{(1-D)\cdot Vin}{Lpri}\cdot\left(\frac{D\cdot Ts}{2}-t\right)\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt \ldots + \frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left[\frac{D\cdot Vin}{Lpri}\cdot\left(t-\frac{1+D}{2}\cdot Ts\right)\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$b_n := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[\frac{(1-D)\cdot Vin}{Lpri}\cdot\left(\frac{D\cdot Ts}{2}-t\right)\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt \ldots + \frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left[\frac{D\cdot Vin}{Lpri}\cdot\left(t-\frac{1+D}{2}\cdot Ts\right)\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$Im_n := \sqrt{(a_n)^2+(b_n)^2}$$

The correction curves corresponding respectively to the secondary open and the secondary shorted are :

$$k_o(f) := 1 + 6.035\cdot10^{-3}\cdot f^{0.481} \qquad k_s(f) := 1 + 0.202\cdot f^{0.172}$$

Let the PCB trace width be x and the core length be L. We can now write the core width W(x).

$$W(x) := 2\cdot\left(x + 2.5\cdot10^{-3}\right) + 2\cdot l$$

(Allow a 2.5mm clearance in window width :
Need 0.030" between edge of trace and edge of PCB + 0.5 mm between edge of PCB and core window wall ; hence :
2x(0.030" x 25.4 + 0.5 mm) = 2.5mm)

$$Pcore(x,L) := K1\cdot\left[\frac{D\cdot(1-D)\cdot Vin}{2\cdot N}\right]^{\beta}\cdot Fs^{\alpha-\beta}\cdot l^{1-\beta}\cdot L^{1-\beta}\cdot(2\cdot t + 2\cdot x + 2\cdot l + 0.007)$$

We shall assume that the primary winding is made up of 6 layers in series whereas the secondary is made of 4 layers in //.

$$R_{layer} = \frac{\rho}{z} \cdot \frac{2 \cdot l + 2 \cdot L + 4 \cdot x + 0.01}{x}$$

Where z is the copper thickness corresponding to 2 ounces of copper, i.e. $71.12 \cdot 10^{-6}$ m.
ρ is the copper resistivity at 80 Deg. C

$$\rho := 1.72 \cdot 10^{-8} \cdot \frac{234.5 + 80}{254.5} \qquad \rho = 2.126 \cdot 10^{-8}$$

$$z := 2 \cdot 1.4 \cdot 10^{-3} \cdot 25.4 \cdot 10^{-3} \qquad z = 7.112 \cdot 10^{-5}$$

Let's now calculate the copper losses ; it should be noted that the correction factors calculated above include the secondary winding resistance ; the latter shall not be included in the calculation.

$$Pwdg(x, L) := \frac{\rho}{z} \cdot \frac{2 \cdot l + 2 \cdot L + 4 \cdot x + 0.01}{x} \cdot N \cdot \left[\sum_n k_o(n \cdot Fs) \cdot \frac{(Im_n)^2}{2} + \sum_n k_s(n \cdot Fs) \cdot \frac{(IL_n)^2}{2} \right]$$

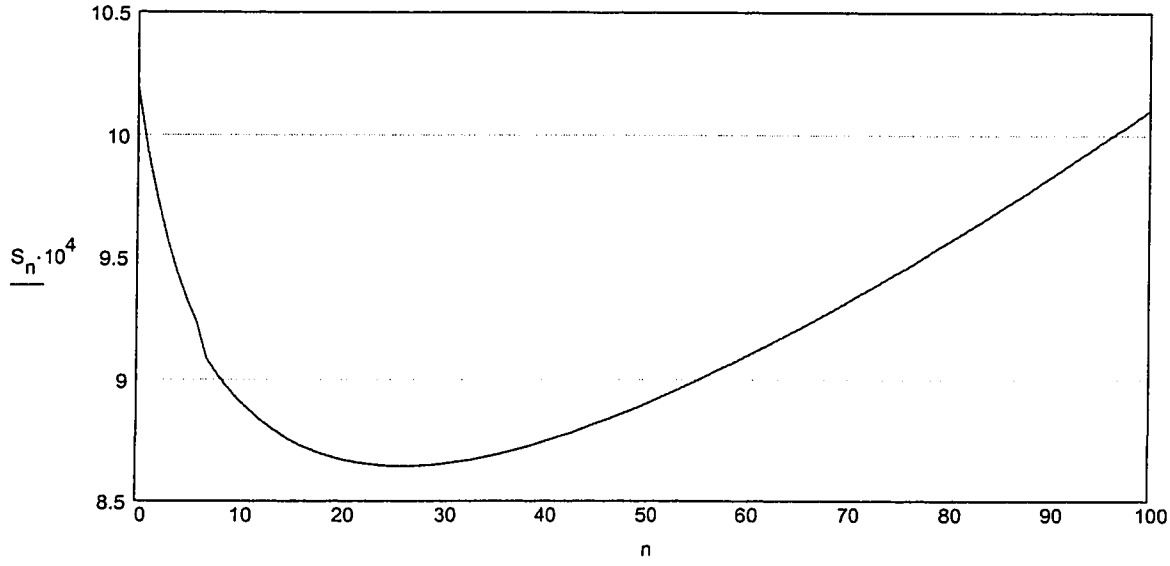
$n := 0 .. 100$

$L_n := 0.0155 + n \cdot 0.0001$

$x := 0.001$ Allow a power dissipation in the transformer = 0.5 W

$w_n := root\left(Pcore(x, L_n) + Pwdg(x, L_n) - 0.5, x\right)$

$S_n := \left(L_n + 2 \cdot w_n + 5 \cdot 10^{-3}\right) \cdot \left(2 \cdot l + 2 \cdot w_n + 5 \cdot 10^{-3}\right)$



$S_{tfo} := \min(S)$ $S_{tfo} = 8.643 \cdot 10^{-4}$ $V_{tfo} := S_{tfo} \cdot h$

$m_n := \text{if}(S_n > S_{tfo}, 0, n)$

$n := \max(m)$ $n = 26$

$S_n = 8.643 \cdot 10^{-4}$

$Pcore(w_n, L_n) = 0.217$ $w_n = 4.479 \cdot 10^{-3}$

$Pwdg(w_n, L_n) = 0.283$ $L_n = 0.018$

$$k2 := 2.2 \cdot \sqrt{\frac{Fs}{500 \cdot 10^3}}$$

$$R_{sec} := \frac{\rho}{z} \cdot \frac{2 \cdot l + 2 \cdot L_n + 4 \cdot w_n + 0.01}{w_n} \cdot \frac{k2}{4} \qquad R_{sec} = 2.531 \cdot 10^{-3}$$

B) Output inductors

Let $\Delta Io_{max} := 1A$. ΔIo is the sum of ΔI_{L1} and ΔI_{L2}. We design L1 and L2 such that their respective ripples exactly cancel out at $D_{nom} := D$. This means :

$$L2 = L1 \cdot \frac{1 - D_{nom}}{D_{nom}} \qquad f(D) := \frac{D_{nom} - D}{1 - D_{nom}}$$

ΔIo is given by : $$\Delta Io = \frac{Vout + Von}{L1} \cdot \frac{1}{Fs} \cdot f(D)$$

ΔIo is maximum at $D = D_{max}$

$$L1 := \left| \frac{Vout + Von}{\Delta Io_{max}} \cdot \frac{1}{Fs} \cdot f(D_{max}) \right| \qquad L1 = 1.426 \cdot 10^{-6}$$

$$L2 := L1 \cdot \frac{1 - D_{nom}}{D_{nom}} \qquad L2 = 2.865 \cdot 10^{-6}$$

Design L1 and L2 such that $I_{L1} = I_{L2} = Io/2$. In addition, choose Bdc = 0.25T @ I = 15A through L. We will also allow a total copper loss in the output inductors of 0.3W.

$P_{wdg} := 0.3$ $\qquad P_{wdg} = (R_{L1} + R_{L2}) \times (Io/2)^2$

In order to have : $I_{L1} = I_{L2} = Io/2$, the DC resistances of L1 and L2 must satisfy the relationship : $R_{L2} + D \times R_{sec} = R_{L1} + (1\text{-}D) \times R_{sec}$, or : $R_{L2} = R_{L1} + (1\text{-}2D) \times R_{sec}$ .Therefore :

$$R_{L1} := \frac{P_{wdg} - (1 - 2 \cdot D) \cdot R_{sec} \cdot \left(\frac{Io}{2}\right)^2}{2 \cdot \left(\frac{Io}{2}\right)^2} \qquad R_{L1} = 2.242 \cdot 10^{-3}$$

$$R_{L2} := R_{L1} + (1 - 2 \cdot D) \cdot R_{sec} \qquad R_{L2} = 3.091 \cdot 10^{-3}$$

Bdc := 0.25 (@ Io = 15)

Calculate optimum area for L1

Reset all S to a high number : $n := 0, 1 .. 100$ $S_n := 1000$

Let the number of turns vary from 1 to 4 $n := 1 .. 4$

$$L_n := \frac{L1 \cdot Io}{Bdc \cdot n \cdot l}$$

$$x_n := \frac{\frac{n^2}{10} \cdot \frac{\rho}{z} \cdot \left(2 \cdot L_n + 2 \cdot l + 0.01\right)}{R_{L1} - 4 \cdot \frac{n^2}{10} \cdot \frac{\rho}{z}}$$

The winding of L1 uses 10 layers, so each turn takes up 10/n layers.

x_n
$6.945 \cdot 10^{-4}$
$2.451 \cdot 10^{-3}$
$7.328 \cdot 10^{-3}$
0.043

L_n
0.013
$6.581 \cdot 10^{-3}$
$4.388 \cdot 10^{-3}$
$3.291 \cdot 10^{-3}$

Calculate core losses

$$Pcore_n := K1 \cdot \left[\frac{(Vout + Von) \cdot D}{2 \cdot n} \right]^{\beta} \cdot Fs^{\alpha - \beta} \cdot l^{1 - \beta} \cdot \left(L_n\right)^{1 - \beta} \cdot \left(2 \cdot t + 2 \cdot x_n + 2 \cdot l + 0.007\right)$$

$Pcore_n$

0.018
0.01
$8.895 \cdot 10^{-3}$
0.019

Calculate Area of L1

$$S_n := \left(L_n + 2 \cdot x_n + 0.005\right) \cdot \left(2 \cdot l + 2 \cdot x_n + 0.005\right)$$

S_n

$3.791 \cdot 10^{-4}$
$3.775 \cdot 10^{-4}$
$7.852 \cdot 10^{-4}$
$9.778 \cdot 10^{-3}$

Minimal area is given by $n := 2$; so, this becomes our optimum number of turns for L1.

$S_{L1} := \min(S)$

$S_{L1} = 3.775 \cdot 10^{-4}$ $\qquad$ $V_{L1} := S_{L1} \cdot h$

Calculate optimum area for L2

Let the number of turns vary from 1 to 4 $n := 1..4$

$$L_n := \frac{L2 \cdot Io}{Bdc \cdot n \cdot l}$$

$$x_n := \frac{\frac{n^2}{10} \cdot \frac{\rho}{z} \cdot \left(2 \cdot L_n + 2 \cdot l + 0.01\right)}{R_{L2} - 4 \cdot \frac{n^2}{10} \cdot \frac{\rho}{z}}$$

The winding of L2 uses 10 layers, so each turn takes up 10/n layers.

x_n
$7.633 \cdot 10^{-4}$
$2.262 \cdot 10^{-3}$
$5.423 \cdot 10^{-3}$
0.015

L_n
0.026
0.013
$8.816 \cdot 10^{-3}$
$6.612 \cdot 10^{-3}$

Calculate core losses

$$Pcore_n := K1 \cdot \left[\frac{(Vout + Von) \cdot (1 - D)}{2 \cdot n} \right]^{\beta} \cdot Fs^{\alpha - \beta} \cdot l^{1 - \beta} \cdot (L_n)^{1 - \beta} \cdot (2 \cdot t + 2 \cdot x_n + 2 \cdot l + 0.007)$$

$Pcore_n$

0.036
0.02
0.016
0.018

Calculate Area of L2

$$S_n := (L_n + 2 \cdot x_n + 0.005) \cdot (2 \cdot l + 2 \cdot x_n + 0.005)$$

S_n

$6.439 \cdot 10^{-4}$
$5.124 \cdot 10^{-4}$
$7.114 \cdot 10^{-4}$
$1.944 \cdot 10^{-3}$

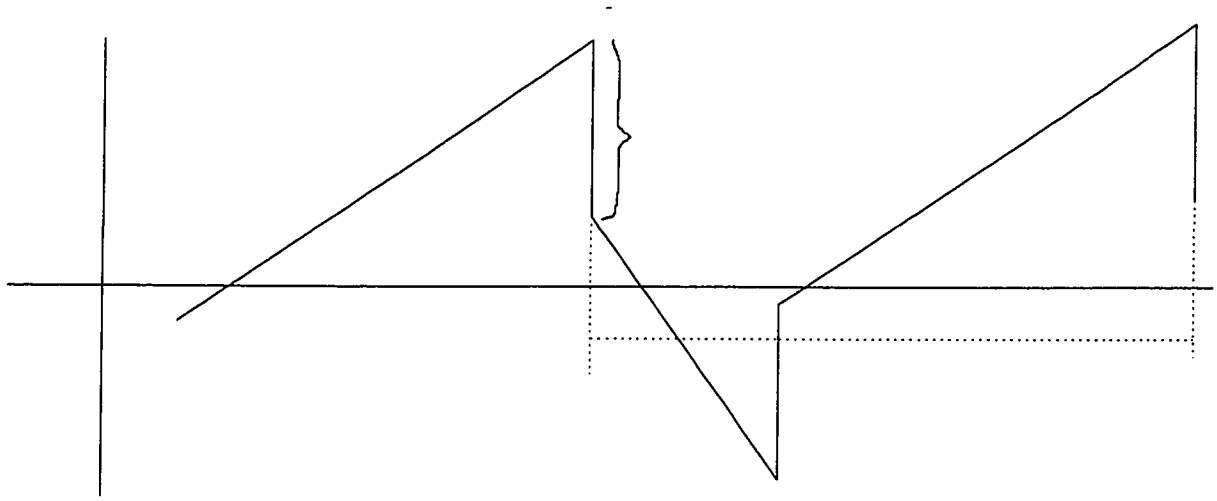
Minimal area is given by $n := 2$; so, this becomes our optimum number of turns for L2.

$S_{L2} := \min(S)$

$S_{L2} = 5.124 \cdot 10^{-4}$ $\qquad V_{L2} := S_{L2} \cdot h$

C) Input inductors

The criteria we will apply here are : constant copper losses and constant attenuation.
We need to find out the fundamental of the primary current waveform.



$$Ts := \frac{1}{Fs} \qquad Ts = 2.5\cdot 10^{-6} \qquad n := 1$$

$$a_1 := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[-(1-D)\cdot\frac{Io}{N}+\frac{(1-D)\cdot Vin}{Lpri}\cdot\left(\frac{D\cdot Ts}{2}-t\right)\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt \ldots$$
$$+\frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left[D\cdot\frac{Io}{N}+\frac{D\cdot Vin}{Lpri}\cdot\left(t-\frac{1+D}{2}\cdot Ts\right)\right]\cdot\cos\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$b_1 := \frac{2}{Ts}\cdot\int_0^{D\cdot Ts}\left[-(1-D)\cdot\frac{Io}{N}+\frac{(1-D)\cdot Vin}{Lpri}\cdot\left(\frac{D\cdot Ts}{2}-t\right)\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt \ldots$$
$$+\frac{2}{Ts}\cdot\int_{D\cdot Ts}^{Ts}\left[D\cdot\frac{Io}{N}+\frac{D\cdot Vin}{Lpri}\cdot\left(t-\frac{1+D}{2}\cdot Ts\right)\right]\cdot\sin\left(n\cdot\frac{2\cdot\pi}{Ts}\cdot t\right)dt$$

$$Fund := \frac{\sqrt{a_1^2 + b_1^2}}{2}$$ The division by 2 comes from the capacitive divider on the primary side

Fund = 1.038

The CE03 spec requires a maximum conducted emission of 45 dBuA at 500kHz. This converts into

$lin_{500} := 10^{\frac{45}{20}} \cdot 10^{-6}$; $lin_{500} = 1.778 \cdot 10^{-4}$; At 15 kHz, the maximum conducted emission equals 74dBuA,

which converts into : $lin_{15} := 10^{\frac{74}{20}} \cdot 10^{-6}$ or $lin_{15} = 5.012 \cdot 10^{-3}$ In between 15kHz and 500kHz, the maximum conducted emission is a linear interpolation beween lin500 and lin15 ; therefore, let's calculate the maximum concucted emission at the given frequency of operation :

$$lin_{Fs} := lin_{15} \cdot \frac{15000}{Fs}$$ $lin_{Fs} = 1.879 \cdot 10^{-4}$

Let's now calculate the required attenuation :

$$Att := \frac{Fund}{lin_{Fs}} \cdot 2$$ (The factor of 2 provides 6dB margin) $Att = 1.105 \cdot 10^4$

Calculate the corner frequency (double stage filter) :

$$f_c := \frac{Fs}{Att^{0.25}}$$ $f_c = 3.902 \cdot 10^4$

Calculate the DC current

$$Idc := D \cdot (1 - D) \cdot \frac{Io}{N}$$ Idc = 0.555

Calculate the half bridge capacitance value : it is the capacitance that yields a mid-point peak to peak voltage not exceeding 1V. Let's first determine the instant t1 where the current through C2 (bottom capacitor of half bridge) crosses the zero line.

$t1 := 1 \cdot 10^{-6}$

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$$Idc - \left[D \cdot \frac{Io}{N} + \frac{D \cdot Vin}{Lpri} \cdot \left(t1 - \frac{1 + D}{2} \cdot Ts \right) \right] = 0$$

$t1 := Find(t1)$

$t1 = 1.548 \cdot 10^{-6}$

$$C_{hb} := \left| \frac{1}{1} \cdot \left[\int_{t1}^{Ts} Idc - \left[D \cdot \frac{Io}{N} + \frac{D \cdot Vin}{Lpri} \cdot \left(t - \frac{1 + D}{2} \cdot Ts \right) \right] dt \right] \right|$$

$C_{hb} = 1.068 \cdot 10^{-6}$

Take : $C_{hb} := 0.96 \cdot 10^{-6}$ (3 layers of SM05, 200V) (1)

Calculate the RMS current through the capacitor ; the worst case is the top capacitor ;

$$Ic_{rms} := \sqrt{(1 - D) \cdot Idc^2 + \frac{1}{Ts} \cdot \int_0^{D \cdot Ts} \left[Idc - (1 - D) \cdot \frac{Io}{N} + \frac{(1 - D) \cdot Vin}{Lpri} \cdot \left(\frac{D \cdot Ts}{2} - t \right) \right]^2 dt}$$

$Ic_{rms} = 1.024$

This results in an ESR of 54 mΩ which yields a dissipation of 54 mW per capacitor.

The filter capacitance is actually one half of each half bridge capacitance :

$$C_f := \frac{C_{hb}}{2} \qquad C_f = 4.8 \cdot 10^{-7}$$

Calculate the area of overall filtering capacitors : Need 2 half-bridge capacitors for the second stage filter and 1 for the first stage filter.
All 3 capacitors are SM05.

$$S_{Cf} := 3 \cdot 0.25 \cdot 0.3 \cdot \left(25.4 \cdot 10^{-3}\right)^2 \qquad S_{Cf} = 1.452 \cdot 10^{-4} \qquad (2)$$

$$V_{Cf} := S_{Cf} \cdot 2 \cdot 0.12 \cdot 25.4 \cdot 10^{-3}$$

Calculate filter inductance :

$$L_f := \frac{1}{C_f} \cdot \left(\frac{1}{2 \cdot \pi \cdot f_c}\right)^2 \qquad L_f = 3.466 \cdot 10^{-5}$$

Calculate damping resistance value :

$$Rd := \sqrt{2.618 \cdot \frac{L_f}{C_f}} \qquad Rd = 13.75$$

Calculate damping capacitance value :

$$Cd := \frac{5 \cdot \sqrt{2.618 \cdot L_f \cdot C_f}}{Rd} \qquad Cd = 2.4 \cdot 10^{-6}$$

Calculate the area of damping capacitors : need 2 damping capacitors (one in each stage)
Both are SM04.

$$S_{Cd} := 2 \cdot 0.4 \cdot 0.44 \cdot \left(25.4 \cdot 10^{-3}\right)^2 \qquad S_{Cd} = 2.271 \cdot 10^{-4} \qquad (3)$$

$$V_{Cd} := S_{Cd} \cdot 2 \cdot 0.12 \cdot 25.4 \cdot 10^{-3}$$

In order to undertake the next step which is to determine the size of the input filter inductor, let's define the geometrical dimensions of the 16 most likely MPP cores which we will be using. All dimensions are in cm.

$i := 0..15$

$OD_0 := 0.432$	$ID_0 := 0.198$	$Ht_0 := 0.297$	$Ac_0 := 0.0211$
$OD_1 := 0.521$	$ID_1 := 0.193$	$Ht_1 := 0.330$	$Ac_1 := 0.0285$
$OD_2 := 0.699$	$ID_2 := 0.229$	$Ht_2 := 0.343$	$Ac_2 := 0.0470$
$OD_3 := 0.724$	$ID_3 := 0.229$	$Ht_3 := 0.318$	$Ac_3 := 0.0476$
$OD_4 := 0.732$	$ID_4 := 0.221$	$Ht_4 := 0.554$	$Ac_4 := 0.0920$
$OD_5 := 0.851$	$ID_5 := 0.343$	$Ht_5 := 0.381$	$Ac_5 := 0.0615$
$OD_6 := 0.762$	$ID_6 := 0.345$	$Ht_6 := 0.572$	$Ac_6 := 0.0725$
$OD_7 := 1.029$	$ID_7 := 0.427$	$Ht_7 := 0.381$	$Ac_7 := 0.0752$
$OD_8 := 1.029$	$ID_8 := 0.427$	$Ht_8 := 0.457$	$Ac_8 := 0.0945$
$OD_9 := 1.080$	$ID_9 := 0.457$	$Ht_9 := 0.457$	$Ac_9 := 0.1000$
$OD_{10} := 1.190$	$ID_{10} := 0.589$	$Ht_{10} := 0.472$	$Ac_{10} := 0.0906$
$OD_{11} := 1.346$	$ID_{11} := 0.699$	$Ht_{11} := 0.551$	$Ac_{11} := 0.1140$
$OD_{12} := 1.740$	$ID_{12} := 0.953$	$Ht_{12} := 0.711$	$Ac_{12} := 0.1920$
$OD_{13} := 1.803$	$ID_{13} := 0.902$	$Ht_{13} := 0.711$	$Ac_{13} := 0.2320$
$OD_{14} := 2.110$	$ID_{14} := 1.207$	$Ht_{14} := 0.711$	$Ac_{14} := 0.2260$
$OD_{15} := 2.360$	$ID_{15} := 1.339$	$Ht_{15} := 0.838$	$Ac_{15} := 0.3310$

Let's calculate wound outside diameter for all the above cores.

$$OD\_w_i := \sqrt{(OD_i)^2 + 0.75 \cdot (ID_i)^2}$$

Let's calculate MLT for all these cores.

$$MLT_i := 2 \cdot Ht_i + OD\_w_i - \frac{ID_i}{2}$$

Let's calculate Kg for all these cores

$Ku := 0.4$

$$Kg\_c_i := \frac{\pi \cdot \frac{(ID_i)^2}{4} \cdot (Ac_i)^2 \cdot Ku}{MLT_i}$$

Let's now calculate the size of the filtering inductors (Need two identical inductors, one in each stage. We target a total winding loss in the input inductors of 0.3W. This means that each inductor will dissipate 0.15W. Core losses are considered negligible.

Let's first calculate regulation :

$Pin := Vin \cdot Idc$

$Pwdg := 0.15$

$$\alpha := \frac{Pwdg}{Pin + Pwdg} \cdot 100 \qquad \alpha = 0.27$$

$\delta I := 0.05$ $\qquad Bdc := 0.2$

1) Calculate energy

$$E := L_f \cdot \frac{Idc^2}{2} \qquad E = 5.333 \cdot 10^{-6} \quad \text{Joules}$$

2) Calculate Ke and Kg coefficients

$$Ke := 0.145 \cdot Pin \cdot Bdc^2 \cdot 10^{-4} \qquad Ke = 3.217 \cdot 10^{-5}$$

$$Kg := \frac{E^2}{(Ke \cdot \alpha)} \qquad Kg = 3.278 \cdot 10^{-6}$$

3) From the above table of cores, select the core which has a value of Kg immediately higher than the Kg calculated above.

$b_i := if(Kg\_c_i - Kg < 0, 10^6, Kg\_c_i)$

$C := \sum b$

$n := \text{floor}\left(\frac{C}{10^6}\right)$ $\quad n = 0$ $\quad OD\_w_n = 0.465$ $\quad Kg\_c_n = 5.713 \cdot 10^{-6}$

4) Calculate area of filter inductors in square meters :

$S_{Lf} := 2 \cdot \pi \cdot \frac{(OD\_w_n)^2}{4} \cdot 10^{-4}$ $\quad S_{Lf} = 3.393 \cdot 10^{-5}$

$V_{Lf} := S_{Lf} \cdot Ht_n \cdot 10^{-2}$

D) Second stage output filter

Need a maximum output voltage ripple of 10mV pk-pk $Vo_{pk\_pk} := 0.010$

1) First criterion : peak to peak ripple voltage across first stage capacitor : 5% of Vout

$\Delta V_{pk\_pk} := 0.05 \cdot Vout$ $\Delta V_{pk\_pk} = 0.165$

First stage output capacitor : $C1 := \frac{\Delta Io_{max}}{8 \cdot Fs \cdot \Delta V_{pk\_pk}}$ $C1 = 1.894 \cdot 10^{-6}$

2) Second criterion : ΔVpk_pk appearing across the first stage output filter capacitor C1 must be attenuated to 10mV across the second stage filter capacitor.
Hence, the second stage filter corner frequency is given by :

$\omega_0 := 2 \cdot \pi \cdot Fs \cdot \sqrt{\frac{Vo_{pk\_pk}}{\Delta V_{pk\_pk}}}$ $\omega_0 = 6.187 \cdot 10^5$

$f_0 := \frac{\omega_0}{2 \cdot \pi}$ $f_0 = 9.847 \cdot 10^4$

First stage effective output inductance : $L_{eff} := \frac{L1 \cdot L2}{L1 + L2}$ $L_{eff} = 9.521 \cdot 10^{-7}$

Let : $Lout := \frac{L_{eff}}{5}$ $Lout = 1.904 \cdot 10^{-7}$

$Cout := \frac{1}{\omega_0^2 \cdot Lout}$ $Cout = 1.372 \cdot 10^{-5}$

Calculate damping resistance and damping capacitance required. The mode to be damped is the one defined by the corner frequency : $\omega_f := \frac{1}{\sqrt{(L_{eff} + Lout) \cdot (C1 + Cout)}}$

Let : $Q_{out} := 1$

Therefore : $Rd_{out} := Q_{out} \cdot \sqrt{\frac{L_{eff} + Lout}{C1 + Cout}}$ $Rd_{out} = 0.271$

The product Rd_{out} x Cd_{out} must be such that $\frac{1}{Rd_{out} \cdot Cd_{out}} = \frac{\omega_f}{3}$

Therefore : $Cd_{out} := \frac{3}{Q_{out}} \cdot (C1 + Cout)$ $Cd_{out} = 4.684 \cdot 10^{-5}$

Take : Cd_{out} = 47uF, 10V, CWR06, size H ; we therefore need 1 CWR06 capacitor
+ 1 SM05 capacitor (2 layers) in the first stage + 1 SM04 capacitor (4 layers) in the second stage.

$S_{Cout} := (0.285 \cdot 0.150 + 0.25 \cdot 0.3 + 0.4 \cdot 0.44) \cdot \left(25.4 \cdot 10^{-3}\right)^2$ $S_{Cout} = 1.895 \cdot 10^{-4}$

$V_{Cout} := (0.285 \cdot 0.150 \cdot 0.110 + 0.25 \cdot 0.3 \cdot 0.12 \cdot 2 + 0.4 \cdot 0.44 \cdot 0.12 \cdot 4) \cdot \left(25.4 \cdot 10^{-3}\right)^3$

$V_{Cout} = 1.756 \cdot 10^{-6}$ (5)

Let's now calculate the size of the second stage filter inductor. We target a total winding loss in Lout of 0.15W. Core losses are considered negligible.

Let's first calculate regulation :

$Pout := Vout \cdot Io$ $\quad Pout = 49.5$

$Pwdg := 0.15$

$\alpha := \frac{Pwdg}{Pout + Pwdg} \cdot 100$ $\quad \alpha = 0.302$

$\delta I := 0.05$ $\quad Bdc := 0.2$

1) Calculate energy

$E := Lout \cdot \frac{Io^2}{2}$ $\quad E = 2.142 \cdot 10^{-5}$ Joules

2) Calculate Ke and Kg coefficients

$Ke := 0.145 \cdot Pout \cdot Bdc^2 \cdot 10^{-4}$ $\quad Ke = 2.871 \cdot 10^{-5}$

$Kg := \frac{E^2}{(Ke \cdot \alpha)}$ $\quad Kg = 5.291 \cdot 10^{-5}$

3) From the above table of cores, select the core which has a value of Kg immediately higher than the Kg calculated above.

$b_i := if(Kg\_c_i - Kg < 0, 10^6, Kg\_c_i)$

$C := \sum b$

$n := floor\left(\frac{C}{10^6}\right)$ $\quad n = 4$ $\quad Kg\_c_n = 7.404 \cdot 10^{-5}$ $\quad OD\_w_n = 0.757$

4) Calculate area of second stage filter inductor in square meters :

$$S_{Lout} := \pi \cdot \frac{(OD\_w_n)^2}{4} \cdot 10^{-4} \qquad S_{Lout} = 4.496 \cdot 10^{-5}$$

$$V_{Lout} := S_{Lout} \cdot Ht_n \cdot 10^{-2}$$

Calculate total area occupied by the EPC magnetics + filter capacitors

$$S_{tot} := S_{tfo} + S_{L1} + S_{L2} + S_{Cf} + S_{Cd} + S_{Lf} + S_{Cout} + S_{Lout}$$

$S_{tot} = 2.395 \cdot 10^{-3}$ m^2

$S_{tot} := S_{tot} \cdot 10^4$ $S_{tot} = 23.948$ cm^2

Calculate total volume occupied by the EPC magnetics + filter capacitors

$$V_{tot} := V_{tfo} + V_{L1} + V_{L2} + V_{Cf} + V_{Cd} + V_{Lf} + V_{Cout} + V_{Lout}$$

$V_{tot} = 2.192 \cdot 10^{-5}$ m^3

$V_{tot} := V_{tot} \cdot 10^6$ $V_{tot} = 21.917$ cm^3

Fs = 100kHz

Equ. (1) p. 14 : $C_{hb} := 4.4 \cdot 10^{-6}$ (2 layers of SM03)

Equ. (2) p. 15 : $S_{Cf} := (2 \cdot 1 \cdot 0.5 + 0.4 \cdot 0.44) \cdot (25.4 \cdot 10^{-3})^2$

$S_{Cf} = 7.587 \cdot 10^{-4}$ (2 capacitors SM03 + 1 capacitor SM04)

Equ. (3) p. 15 : $Cd := 11 \cdot 10^{-6}$: Damping capacitors consist of 2 x 2 CLR79, 100V in series

$S_{Cd} := 4 \cdot 0.641 \cdot 0.312 \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cd} = 5.161 \cdot 10^{-4}$

The 4 CLR79 above are size T2

Equ. (4) p. 19 : $Cout := 181 \cdot 10^{-6}$

Take : Cout = 4 x 47uF, 6V, CWR06, size F ; we therefore need 8 CWR06 capacitors (2 capacitor banks) + a SM05 capacitor in the first stage for noise filtering.

$n := 8$

Equ. (5) p. 19 : $S_{Cout} := (n \cdot 0.265 \cdot 0.110 + 0.25 \cdot 0.3) \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cout} = 1.988 \cdot 10^{-4}$

This yields $S_{tot} = 46.1\ cm^2$

Fs = 200kHz

Equ. (1) p. 14 : $C_{hb} := 2.2 \cdot 10^{-6}$ (3 layers of SM04)

Equ. (2) p. 15 : $S_{Cf} := 3 \cdot 0.4 \cdot 0.44 \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cf} = 3.406 \cdot 10^{-4}$ (3 capacitors SM03)

Equ. (3) p. 15 : $Cd := 5.5 \cdot 10^{-6}$: Damping capacitors consist of 2 x 2 CLR79, 100V in series

$S_{Cd} := 4 \cdot 0.641 \cdot 0.312 \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cd} = 5.161 \cdot 10^{-4}$

The 4 CLR79 above are size T2

Equ. (4) p. 19 : $Cout := 9.048 \cdot 10^{-5}$

Take : Cout = 2 x 47uF, 6V, CWR06, size G ; we therefore need 4 CWR06 capacitors (2 capacitor banks) + a SM05 capacitor in the first stage for noise filtering.

$n := 4$

Equ. (5) p. 19 : $S_{Cout} := (n \cdot 0.265 \cdot 0.110 + 0.25 \cdot 0.3) \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cout} = 1.236 \cdot 10^{-4}$

This yields $S_{tot} = 30.2\ cm^2$

Fs = 300kHz

Equ. (1) p. 14 : $C_{hb} := 1.5 \cdot 10^{-6}$ (2 layers of SM04)

Equ. (2) p. 15 : $S_{Cf} := (2 \cdot 0.4 \cdot 0.44 + 0.25 \cdot 0.3) \cdot (25.4 \cdot 10^{-3})^2$

$S_{Cf} = 2.755 \cdot 10^{-4}$ (2 capacitors SM04 + 1 capacitor SM05)

Equ. (3) p. 15 : $Cd := 3.75 \cdot 10^{-6}$: Damping capacitors consist of 2 x 2 CLR79, 100V in series

$S_{Cd} := 4 \cdot 0.641 \cdot 0.312 \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cd} = 5.161 \cdot 10^{-4}$

The 4 CLR79 above are size T2

Equ. (4) p. 19 : $Cout := 6.032 \cdot 10^{-5}$

Take : Cout = 2 x 47uF, 6V, CWR06, size G ; we therefore need 4 CWR06 capacitors (2 capacitor banks) + a SM05 capacitor in the first stage for noise filtering.

$n := 4$

Equ. (5) p. 19 : $S_{Cout} := (n \cdot 0.265 \cdot 0.110 + 0.25 \cdot 0.3) \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cout} = 1.236 \cdot 10^{-4}$

This yields $S_{tot} = 27.8\ cm^2$

Fs = 400kHz

Equ. (1) p. 14 : $C_{hb} := 0.96 \cdot 10^{-6}$ (3 layers of SM05)

Equ. (2) p. 15 : $S_{Cf} := 3 \cdot 0.25 \cdot 0.3 \cdot (25.4 \cdot 10^{-3})^2$

$S_{Cf} = 1.452 \cdot 10^{-4}$ (2 capacitors SM04 + 1 capacitor SM05)

Equ. (3) p. 15 : $Cd := 2.4 \cdot 10^{-6}$: Damping capacitors consist of 2 x SM04, 200V

$S_{Cd} := 2 \cdot 0.4 \cdot 0.44 \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cd} = 2.271 \cdot 10^{-4}$

Equ. (4) p. 19 : $Cout := 4.524 \cdot 10^{-5}$

Take : Cout = 2 x 22uF, 6V, CWR06, size F ; we therefore need 4 CWR06 capacitors (2 capacitor banks) + a SM05 capacitor in the first stage for noise filtering.

$n := 4$

Equ. (5) p. 19 : $S_{Cout} := (n \cdot 0.22 \cdot 0.135 + 0.25 \cdot 0.3) \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cout} = 1.25 \cdot 10^{-4}$

This yields $S_{tot} = 23.5\ cm^2$

Fs = 500kHz

Equ. (1) p. 14 : $C_{hb} := 0.96 \cdot 10^{-6}$ (3 layers of SM05)

Equ. (2) p. 15 : $S_{Cf} := 3 \cdot 0.25 \cdot 0.3 \cdot (25.4 \cdot 10^{-3})^2$

$S_{Cf} = 1.452 \cdot 10^{-4}$ (2 capacitors SM04 + 1 capacitor SM05)

Equ. (3) p. 15 : $Cd := 2.4 \cdot 10^{-6}$: Damping capacitors consist of 2 x SM04, 200V

$S_{Cd} := 2 \cdot 0.4 \cdot 0.44 \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cd} = 2.271 \cdot 10^{-4}$

Equ. (4) p. 19 : $Cout := 3.619 \cdot 10^{-5}$

Take : Cout = 2 x 22uF, 6V, CWR06, size F ; we therefore need 4 CWR06 capacitors (2 capacitor banks) + a SM05 capacitor in the first stage for noise filtering.

$n := 4$

Equ. (5) p. 19 : $S_{Cout} := (n \cdot 0.22 \cdot 0.135 + 0.25 \cdot 0.3) \cdot (25.4 \cdot 10^{-3})^2$ $S_{Cout} = 1.25 \cdot 10^{-4}$

This yields $S_{tot} = 24.9\ cm^2$

$i := 0..4$ $\quad Fs_i := (i + 1)\cdot 100$ $\quad S_{tot} := \begin{bmatrix} 46.1 \\ 30.2 \\ 27.8 \\ 23.5 \\ 24.9 \end{bmatrix}$