Switching Converters with Paralleled MOSFETs

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ABSTRACT

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The requirements for increasing power density is spawning the use of techniques which are increasing the efficiency of the power supplies. The historic method of decreasing the size of the power supply was by increasing the switching frequency. This method was limited by switching losses which increased with switching frequency. Soft switching topologies have removed this barrier by minimizing these losses. These topologies however, have increased conduction losses because of higher currents which are required to flow through the switches in order to achieve lossless switching.

To further increase efficiency it has been proposed that switching MOSFETs be paralleled to decrease their effective on resistance R_{dson}. Although increased efficiency is achievable, there are limits and constraints which prevent continuously adding MOSFETs in parallel to further decrease conduction losses. These limitations will be presented and discussed. Furthermore, in order to understand the principles involved, a MOSFET model will be used in simulations to visualize the voltages and currents flowing through the MOSFET structure during switching in hard and soft switching topologies.

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LIST OF ACRONYMS

BJT	Bipolar Junction Transistor
D	Duty Cycle
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
HS	Hard Switching
HS-PWM	Hard Switching Pulse Width Modulation
KHz	Kilohertz
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOA	Safe Operating Area
SS	Soft Switching
SS-PWM	Soft Switching Pulse Width Modulation
PPM	Pulse Position Modulation
PSM-DTR	Phase-Shift Modulated Double Tuned Resonant
ZVS	Zero Voltage Switching
PWM	Pulse Width Modulation
PSPICE	PC version of SPICE (Simulation Program for Integrated Circuits and Electronics)
PROBE	PC Software used to plot PSPICE simulation results
SABER	Analog and mixed signal simulator from Analogy Inc.

LIST OF PRINCIPLE SYMBOLS

C_{dg}	MOSFET's drain-gate capacitance
C_{ds}	MOSFET's drain-source capacitance
C_{gs}	MOSFET's gate-source capacitance
g_{fs}	MOSFET's forward transconductance
I_{con}	BJT's on collector current
I_{don}	MOSFET's on drain current
I_{donmax}	MOSFET's maximum on drain current
I_{dss}	MOSFET's zero gate voltage drain current
R_d	MOSFET's drain contact resistance
R_g	MOSFET's gate contact resistance
R_s	MOSFET's source contact resistance
L_d	MOSFET's drain wiring inductance
L_g	MOSFET's gate wiring inductance
L_s	MOSFET's source wiring inductance
R_{dsoff}	MOSFET's drain-source off resistance
R_{dson}	MOSFET's drain-source on resistance
$t_{d(off)}$	MOSFET's turn off delay
$t_{d(on)}$	MOSFET's turn on delay
t_f	MOSFET's fall time
t_r	MOSFET's rise time
$V_{(br)dss}$	MOSFET's drain-source breakdown voltage
V_{gsth}	MOSFET's gate-source threshold voltage

CHAPTER 1

INTRODUCTION

1.1 Introduction

In recent years, the developments of soft switching techniques has allowed Pulse Width Modulation (PWM) converters to operate at higher frequencies and at higher efficiencies. This has allowed for higher power densities in modern converter design. It has also made conduction losses more dominant in the overall power losses of the switching element, which for high frequency applications is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). This has made designers attempt to further increase efficiency by paralleling MOSFETs to lower their effective R_{dson} as described in Chapter 2. This has led to some increase in efficiency but limitations exist which must be considered.

1.2 MOSFET Models

In order to comprehend what happens internally to the MOSFET, a MOSFET model will be explained in Chapter 2. Most papers presented on this topic concern themselves with modeling the MOSFET so accurate drive

wave forms can be obtained. This has resulted in complex models which require significant simulation time and at times present convergence problems. Also, mathematical models of the MOSFET are of little use in observing the internal currents causes by the switching action and the parasitic capacitances. The models used were obtained from Motorola and contain discrete elements which allowed the probing of currents flowing through the parasitic components with the PSPICE simulator. The parasitic components must be discrete so that simulation tools such as PSPICE can place current sensors in series with these devices and internal currents can be observed during switching.

1.3 Modulation Techniques

In switching power supply design there are two methods of controlling the output voltage. These are Pulse Position Modulation (PPM) where a fixed pulse width has its repetition rate varied to control the Duty Cycle (D), and PWM which uses a fixed frequency and a variable duty cycle. Of the two techniques PWM is the most commonly used technique because its fixed frequency optimizes the transformer inductor, and input filter design. As a result most controller IC's offered by semiconductor manufactures use PWM as the modulation technique.

PWM is further divided into Hard Switching (HS) and Soft Switching (SS). For the scope of this thesis HS-PWM is any technique which does not minimize the voltage across the MOSFET's drain-source capacitance

C_{ds} when it is turned on. As a result the MOSFET experiences high voltage and currents during switching and these generate switching losses. This is the original application of PWM and is most commonly used in the buck, the boost, the buck-boost, and the derived topologies [1]. A full bridge buck converter will be analyzed using the MOSFET model described in Chapter 2. This analysis will be presented in Chapter 3 and will consider HS-PWM circuits with single and multiple MOSFETs in parallel.

SS-PWM is any technique which minimizes the voltage across the MOSFET's drain-source capacitance C_{ds} before the drain current starts to flow through the MOSFET's drain-source conduction channel. This does not include the techniques which use snubbers to store energy derived during switching and dissipate it by using a resistor [2][3][4]. It also does not include techniques which store energy in inductors and capacitors and then removed by auxiliary circuits [5]. SS-PWM does include techniques which through the use of converter topologies and switching strategies minimizes switching losses. This includes techniques such as the Zero Voltage Switching (ZVS) PWM converter [6] and the Phase-Shifted Modulated Double Tuned Resonant (PSM-DTR) PWM converter [7]. The ZVS-PWM converter uses an auxiliary switch on the line side to discharge the drain-source capacitance C_{ds} of the MOSFETs before the are turned on. The PSM-DTR-PWM converter uses a resonant load to discharge the drain-source capacitance C_{ds} of the MOSFETs before they turn on. In both these cases C_{ds} is discharged before the MOSFET starts conducting in the forward direction. In these cases the MOSFET will have no voltage across it when it turns on and thus, no switching

loss at turn on. Conduction losses however are still present. The PSM-DTR-PWM converter will be analyzed using the MOSFET model described in Chapter 2. This analysis will be presented in Chapter 4 and will consider SS-PWM circuits with single and multiple MOSFETs in parallel.

1.4 Scope and Contribution

The scope and object of this thesis is to study the effects of switching on the MOSFETs parasitic components in both HS-PWM and SS-PWM schemes and observe the effects on switching losses when MOSFETs are paralleled in order to decrease conduction losses. The study is limited to converters switching with frequencies between 10 KHz and 200 KHz and with power levels up to 2000 watts. The contribution of this thesis is to use this understanding of the MOSFET's internal parasitics and to generate guidelines to evaluate the effectiveness of adding MOSFETs in parallel for different variables such as topologies, power devices, switching frequencies, cost, and loads.

1.5 Summary of Thesis

The contents of the thesis have been organized as follows:

Chapter 2 discusses the non-ideal MOSFET and considers the models presented in recent papers. The MOSFET model used in simulations and in explaining the effects of parasitics will be described Chapter 2 will

also discuss the requirements and considerations for paralleling MOSFETs. Using the model described in Chapter 2, the effects on the MOSFET's parasitics will be considered.

Chapter 3 will discuss the HS-PWM converter topology and the differences in losses when one MOSFET, and a parallel combination is used. Guidelines will be presented to determine the effectiveness of paralleling MOSFET's using this topology. Experimental measurements will be given to verify the theoretical and simulated analysis.

Chapter 4 will discuss the PSM-DTR-PWM converter topology and the differences in losses when one MOSFET, and a parallel combination is used. Guidelines will be presented to determine the effectiveness of paralleling MOSFET's using this topology. Experimental measurements will be given to verify the theoretical and simulated analysis.

Chapter 5 will summarize the results and effectiveness of paralleling MOSFETs in HS-PWM and SS-PWM topologies. A simplified algorithm will be presented which will help the designer to determine if paralleling is effective for different MOSFETs and applications

Chapter 6 will summarize the thesis and present a conclusion on the effectiveness of paralleling MOSFETs to decrease losses. Suggestions for further work will be presented in this section.

CHAPTER 2

MODELING and PARALLELING of MOSFETs

2.1 MOSFETs vs. BJTs

The MOSFET is a voltage controlled impedance which is widely used in power electronics as the switching element in converter topologies. Before power MOSFETs became commercially available, Bipolar Junction Transistors (BJT) were commonly used. MOSFETs however have become the switch of choice for power supply designers because they have the following advantages over BJTs [8]:

a) MOSFETs can switch faster than BJTs,
b) MOSFETs require less complicated drive circuitry,
c) MOSFETs have a low on voltage,
d) MOSFETs exhibit no secondary breakdown.

MOSFETs are faster because they are majority carrier devices. BJT are minority carriers which store base charge. As a result BJT's have a storage time parameter which prevents the device from being able to block a collector - emitter voltage. Until this charge is removed from the base, the BJT cannot be considered to have turned off. This places

a limit on the maximum switching frequency which can be used for BJT designed power supplies. Since MOSFETs can be switched at higher switching frequencies, power supplies designed with MOSFETs can use smaller transformers and inductors resulting in higher power densities.

MOSFETs require less complicated drive circuitry because the gate is insulated electrically from the drain-source channel Electrical connection of the gate-source region is not required because the MOSFET uses electric fields to control the conductivity of the drain-source channel. The MOSFETs drive circuitry requires power only when the device is turned on or off. It requires little power to stay on or off.

The voltage drop across the drain-source region of the MOSFET when it is turned on is dependent on the R_{dson} and the current I_{don} flowing through the device unlike the BJT device whose voltage drop is less dependent on its collector current I_{con} This makes MOSFETs desirable in low input voltage applications where voltage drops across the switching device limits the overall efficiency such as converters which use batteries as their voltage sources.

Unlike BJTs, secondary breakdown does not occur within the specified ratings of the MOSFET. The MOSFET's Safe Operating Area (SOA) is bounded by the peak current ratings, the drain-source breakdown voltages, and the devices power handling capabilities.

The MOSFET has the following disadvantages when compared to the BJT. These are [8]:

a) the gate is sensitive to Electro-Static Discharge (ESD),

b) dv/dt effects can turn the MOSFET on,

c) fabrication results in an inherent drain-source diode, D_{ds}.

Since the MOSFETs gate is insulted from the drain-source channel by a thin layer of silicon oxide (SO_2), the gate-source region can only support 20 V before the insulation is damaged. Before ESD protective measures were practiced, MOSFETs were damaged while handling during assembly because charged workers were discharging themselves through the gate-source region when they were handling the devices. Modern ESD preventative precautions have largely eliminated this problem.

MOSFETs can also be momentarily turned on when they are connected to an inductive load and driven off quickly. The inductor will generate a large voltage impulse when the current flowing through it is stopped by the MOSFET. This voltage impulse will generate capacitive currents in the MOSFETs gate-drain capacitance C_{gd} and will prevent the device from turning off. This will have the effect of increase the switching losses or destroying the device in the case of a full bridge configuration

The MOSFET also has an inherent drain-source anti-parallel body diode D_{ds} which will allow current to flow from the source to the drain even though the MOSFET is turned off. This can present problems in

topologies where blocking reverse current is required. Also, since this diode is a parasitic, it is typically slower in turning on and off as compared with the MOSFET itself. This presents problems in topologies such as the full bridge inverter where two MOSFETs are connected in series across the DC source. If current is flowing in the anti-parallel body diode of one MOSFET and the other is turned on, there will be a short across the DC rail because the MOSFET with the conducting diode will not be able to block the applied voltage until the charge is removed from its anti-parallel body drain diode.

2.2 MOSFETs as Switching Elements

The MOSFET, like the BJT can be used as a switch by operating it in its cutoff and saturation regions, or as an amplifier by operating it in its linear region. Since efficiency is a prime concern in switching converters, the MOSFET is not used in the linear region since this will force large currents to flow through the device when voltages are present across its drain and source. This will create high conduction losses. Linear regulators operate in this method and are used when low power and or low Electro-Magnetic Interference (EMI) is required.

Commercial power MOSFETs are optimized to operate in their saturation and cutoff regions. In the saturation region the MOSFET is on and the current flow through it will be dictated by the load impedance and the R_{dson} of the device. Very little drive power is

required to keep the MOSFET is this region since its gate-source input is a high impedance capacitance.

2.2.1 Controlling the MOSFET

MOSFETs unlike BJTs are voltage controlled impedances. This means that the MOSFET requires a voltage source to be applied to the gate instead of a current source as in the case of a BJT. Also, in order to use the MOSFET as a switching element it must be fully on or off. Unlike a BJT, where this requires the drive current to vary with load current, the MOSFET will turn on and off by simply insuring that the voltage at the gate is higher than the gate-source threshold voltage V_{gsth}, or lower than V_{gsth} respectively. Also, since the gate-source region of the MOSFET is electrically isolated from the drain-source region, only capacitive currents will flow from the drive. This requires that the MOSFET's drive circuitry be capable of supplying large currents for short periods of time in order for the device to switch quickly. The average current and power required is very small compared with an equivalent power BJT. In fact the MOSFET's drive power is dependent on its parasitic elements.

2.2.2 Parasitic Elements of the MOSFET

Like most semiconducting devices, the MOSFET has parasitic resistances and capacitances due to its construction, material,

junctions, and parasitic inductance due to its wiring from the silicon chip to the package. The parasitic resistances become dominant as current levels increase and the parasitic capacitances and inductances become dominant and cannot be neglected as switching frequencies increase. Power MOSFETs also have a parasitic diode across the drain-source region due to the physical construction of the silicon regions of the device. These parasitic elements affect the turn on and turn off characteristics of the MOSFET, the drive power and the switching losses. Figure 2-1 shows the MOSFET's parasitic elements which are considered when the device is used as a switching element.

The resistive parasitic elements are:

R_g	gate contact resistance
R_d	drain contact resistance
R_s	source contact resistance
R_{dson}	on drain-source resistance
R_{dsoff}	off drain-source resistance

The contact resistances R_g, R_d, and R_s are due the resistance between the silicon and the metal conductor in the contact area. R_{dson} is the resistance of the silicon in the drain-source conduction channel when the device is fully on. R_{dsoff} is the resistance between the drain and source when the MOSFET is off. This resistance can be estimated by obtaining the drain-source breakdown voltage $V_{(br)dss}$ and dividing it by

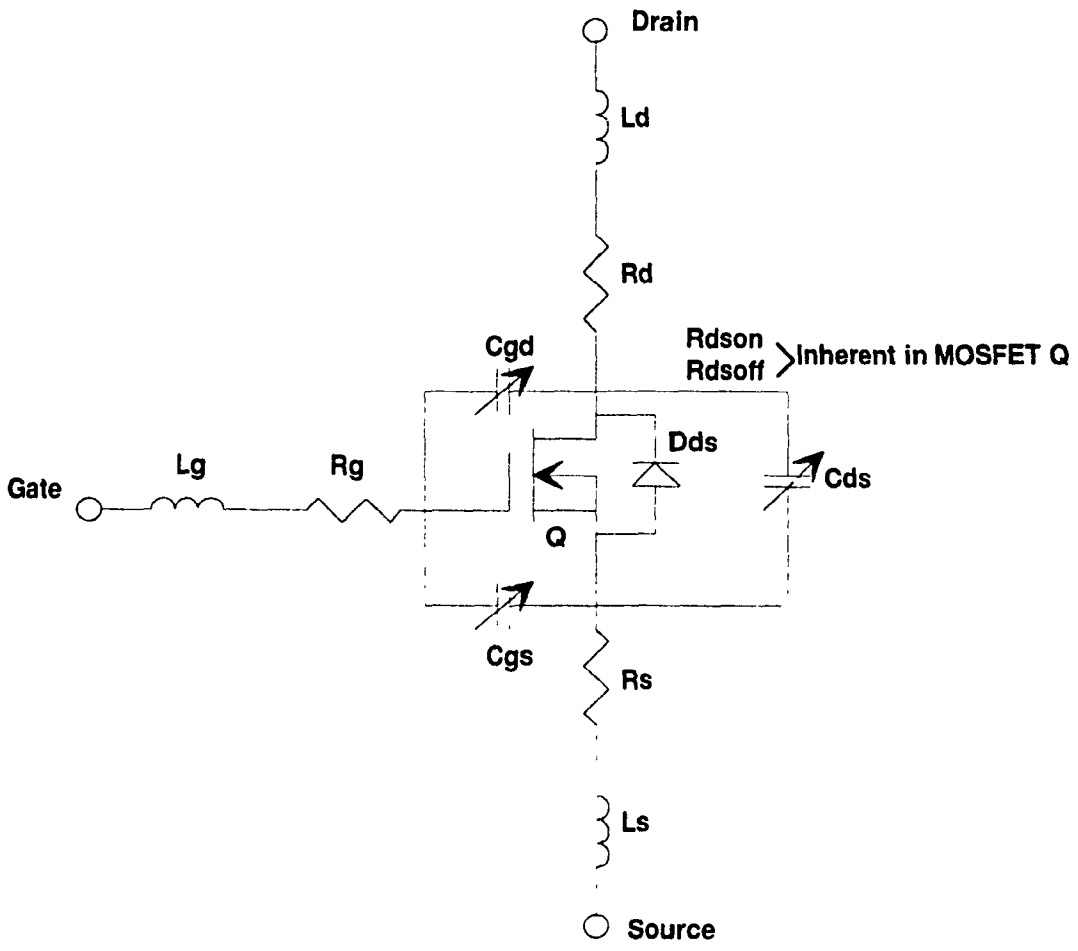


Figure 2.1 - Complete Model of the MOSFET

the zero gate voltage drain current I_{dss}. These parameters are given as worst case values in most data books [9].

The capacitive parasitic elements are:

C_{gs}	gate-source capacitance
C_{ds}	drain-source capacitance
C_{dg}	drain-gate capacitance

These parasitic capacitances are formed between the external device terminals and the silicon material and are dependent on the structure of the MOSFET [10]. As voltages are applied and varied on the gate, source and drain terminals of the MOSFET, charges will move through the silicon to the opposite charged terminal forming a capacitance. These capacitances will vary with the voltage applied across these terminals [11].

Data books provide typical maximum values of the short circuit input capacitance (common source) C_{iss}, the short circuit output capacitance (common source) C_{oss}, and the short circuit reverse transfer capacitance (common source) C_{rss}. These capacitances are related to the parasitic capacitances by the following equations [12]:

$$Ciss = Cgd + Cgs \qquad (2.1)$$

$$Coss = Cds + Cgd \qquad (2.2)$$

$$Crss = Cgd \qquad (2.3)$$

The parasitic capacitances value can be found from the fo lowing equations:

$$Cgs = Ciss - Crss \qquad (2.4)$$

$$Cds = Coss - Crss \qquad (2.5)$$

$$Cdg = Crss \qquad (2.6)$$

The inductive parasitic elements are:

L_g	gate wiring inductance
L_d	drain wiring inductance
L_s	source wiring inductance

These inductances are formed by the wire which is used to connect the semiconductor material to the device's case pins. L_d and L_s are dependent on the MOSFET's package case and are given as typical values in data books [9].

The MOSFETs parasitic anti-parallel body diode D_{ds} is formed between the drain and source of the device and is an inherent parasitic component formed by the fabrication of the MOSFET [13]. This diode will block the same voltage $V_{(br)dss}$ and conduct the same current as the MOSFET's maximum drain current $I_{don(max)}$ in the reverse direction, that is from source to drain, because of its excessive junction area [13]. The orientation of this parasitic diode prevents the MOSFET from blocking reverse voltages and prevents its use as a bilateral switch.

The parasitic diode also exhibits reverse recovery effects which prevent the MOSFET from blocking voltages until the charges are cleared from its junction.

Finally the MOSFET Q represents an ideal MOSFET which has infinite off resistance and zero on resistance. This MOSFET is modeled to have a

specific V_{gsth} for switching. It is also modeled to exhibit the MOSFET's linear region of operation.

2.3 Simulation MOSFET Models

There has been extensive work done on different MOSFET models used for simulation packages. Xu proposed that the parasitic capacitances C_{ds} and C_{gs} be modeled by the variable capacitance function of the PSPICE diode sub circuit model, and the gate-drain capacitance C_{gd} be modeled by a switched capacitance [14]. Switching the gate-drain capacitance simplifies the voltage variation of the capacitance and in some cases causes convergence problems. The model proposed by Haslem also has the switched gate-drain capacitance and does not include the anti-parallel body diode D_{ds} or the lead inductances [15]. Mathematical models such as those proposed by Ong [16] and Hancock [17] are not usable in studying power losses because the current and voltage cannot be probed directly across the parasitic capacitances, resistances and inductances. The model proposed by Yee is limited because it does not model the drain-source capacitance C_{ds} which can be a major source of losses as the switching frequency increases [18].

Software simulators such as PSPICE have their own MOSFET models which allow users to define the MOSFET's parameters. The PSPICE model of the MOSFET has 48 different parameter which need to be defined by the user [19]. The problem with some parameters is that detailed knowledge of the MOSFETs geometry and semiconductor material is required in order

to define them. Channel width and length, lateral diffusion, substrate doping density and forward bias capacitance co-efficient are required by the model, but are not given in the manufactures data books. These models are hard to obtain and do not allow access to the parasitic elements. Also, the waveforms obtained with the PSPICE MOSFET models do not give accurate waveforms during transitions.

The PSPICE software package has a program called PARTS which allows users to enter data sheet values which are converted by the program into parameters used by the MOSFET model [19]. Since data sheets provide partial information, these models are approximate. Manufactures suggest that typical, and worst case models be made and used in simulations. This is time consuming and again does not provide a model with accessible parasitic components.

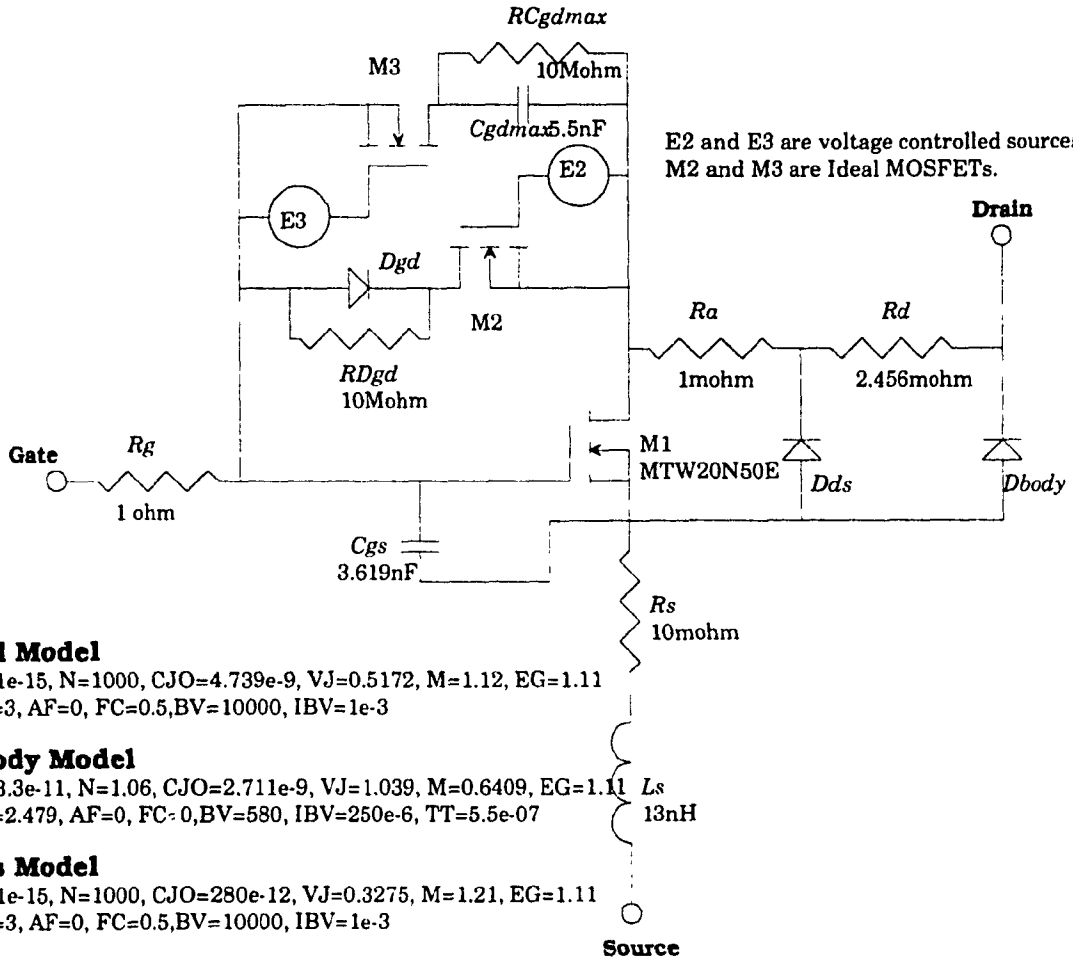
2.4 MOSFET Model Used in Simulations

In recent years semiconductor manufacturers such as Motorola and International Rectifiers have written articles and application notes describing MOSFET models that they have developed for the PSPICE and SABER simulation software packages. As in any model, a compromise is made between simplicity, accuracy and simulation time. Motorola's models are based on its application note AN1043 [20]. This model shown in Figure 2.2 simulates the variable drain-source capacitance C_{ds} by using the voltage controlled capacitance feature of the PSPICE diode models Dds. The variable drain-gate capacitance C_{dg} is modeled by a

PSPICE diode model Ddg and a capacitance *Cdgmax*, which is switched by ideal MOSFETs M2 and M3 and are controlled by monitoring the gate-drain voltage by voltage sources E2 and E3. The anti-parallel body diode is modeled by diode Dbody. Resistances *Rg*, *Rs* and *Rd* are the contact resistances which are formed when the leads are attached to the silicon die. Although the gate-source capacitance C_{gs} is fixed in the Motorola model accurate switching waveforms were obtained by Cordonnier [20]. Other simplifications of the Motorola model are that the gate and drain inductances were combined into a single source inductance *Ls*. The simulations were performed on a COMPAQ Deskpro XL 590 computer using version 5.4 of the PSPICE circuit simulator.

2.5 Paralleling of MOSFETs

MOSFETS are paralleled to obtain higher current handling capabilities, lower R_{dson}, higher efficiencies, and improved thermal performance [12]. Higher switch current capabilities allow a higher power level converter to be built at a lower cost as compared to building two separate converters and operating them in parallel at the unit level. It also avoids using complicated current sharing techniques which will prevent one converter from hogging the load current. A lower R_{dson} decreases the voltage drop across the MOSFET and lowers conduction losses. Thermal performance is improved by distributing the thermal flow over a larger surface area. This along with the lower conduction losses allows for smaller heatsinks to be used given the same MOSFET junction temperature. Paralleling MOSFETs is also less expensive than



Dgd Model
IS= 1e-15, N=1000, CJO=4.739e-9, VJ=0.5172, M=1.12, EG=1.11
XTI=3, AF=0, FC=0.5,BV=10000, IBV=1e-3

Dbody Model
IS= 3.3e-11, N=1.06, CJO=2.711e-9, VJ=1.039, M=0.6409, EG=1.11
XTI=2.479, AF=0, FC=0,BV=580, IBV=250e-6, TT=5.5e-07

Dds Model
IS= 1e-15, N=1000, CJO=280e-12, VJ=0.3275, M=1.21, EG=1.11
XTI=3, AF=0, FC=0.5,BV=10000, IBV=1e-3

M1 Model (MTW20N50E)
LEVEL=3, VTO=3.788, KP30.42, GAMMA=2.5, PHI=0.6, LAMBDA=1.178e-4, IS=1e-14, PB=0.8, MJ=0.5,MJSW=0.33
JS=1e-14, TOX=1e-07, NSUB=5e+17, NFS= 6.121e+11, TPG=1, UO=600, UCRIT=10000,VMAX=1e+06, NEFF=1, AF=1
FC=0.5, KAPPA=0.2

Figure 2.2 - Motorla Model of MOSFET MTW20N50E

using a single high current device because larger silicon die sizes cost more due to the lower yield rates [12].

Unlike BJTs, MOSFETs have a drain current with a negative temperature coefficient which prevents thermal runaway [19]. This characteristic makes paralleling MOSFETs much simpler than paralleling BJTs. From manufacturers data sheets it is documented that as junction temperature rises due to increasing drain current, the devices R_{dson} will increase since it has a positive temperature coefficient. This increase in R_{dson} will cause the current to decrease, or in the case of paralleled devices force more current to flow in the other device. This mechanism will effectively force the devices to share the load current.

2.6 Static and Dynamic Current Sharing in Paralleled MOSFETs

When MOSFETs are paralleled the areas of concern are the steady-state or static conditions, and the switching or dynamic conditions [21]. Static current sharing conditions are dominated by the MOSFETs R_{dson} and are relatively easy to predict [12]. In order to maximize reliability and increase the level of current sharing, paralleled MOSFETs should be thermally coupled by being mounted on the same heatsink and in close proximity to one another [12]. This ensures that the device's junction temperatures will be approximately the same and thus their R_{dson} will be approximately the same.

Dynamic current sharing is more complicated and involves more device parameters than static current sharing. Dynamic current sharing involves both the MOSFETs parasitic components and external circuit components and parasitics. MOSFET parasitics which affect dynamic current sharing are the gate-threshold voltage V_{gsth}, the forward transconductance g_{fs}, and the input capacitance C_{iss} [22]. Circuit components and parasitics which affect dynamic current sharing are the total gate impedance consisting of the gate resistance and gate trace inductance, and the parasitic drain inductance [22].

Dynamic current sharing can also be divided into two sub-sections which have different modes and different controlling parameters. The first sub-section is affected by the V_{gsth}, C_{iss}, and the parasitic gate impedance. These parameters will determine which ice will turn on first and cause a current imbalance. The second sub-section is affected by transconductance g_{fs}, and the drain parasitic inductance L_d. These parameters will determine how the MOSFETs will share current between the time they are turning on and the time they have reached static current sharing. To simplify the analysis, these two mechanisms will be lumped together for this thesis.

2.7 MOSFET Paralleling and Parasitics

When MOSFETs are paralleled, certain parameters and parasitics will affect static and dynamic current sharing. Reviewing Figure 2.1, the following observations can be made. R_{dson}, which affects static

current sharing will decrease and thus lower conduction losses. R_{dsoff} which affects the off leakage current will also decrease and will increase the leakage losses. As mentioned before, in power circuits, leakage losses are negligible when they are compared to the switching and conduction losses and can be ignored. C_{iss} will increase resulting in an increase in the required drive power. This increase in drive power will occur for both soft and hard PWM switching techniques. Drive power is also increased as switching frequencies are increased since the power required for driving the MOSFET is:

$$P = \frac{1}{2} \cdot (Cgs \cdot Vgs^2) \cdot f \qquad (3.1)$$

This equation also shows that a trade off will exist between switching frequency and paralleling MOSFETs. For example, at higher switching frequencies, the decrease in conduction losses due to paralleling MOSFETs may be less than the increase in drive power required to drive the extra MOSFETs.

Other parasitics which will be affected by paralleling MOSFETs will be the output capacitance C_{oss} and the transconductance capacitance C_{rss}. These parasitics will both increase when devices are paralleled and depending on whether hard or soft switching is used, may have an effect on efficiency as will be shown in subsequent chapters.

2.8 MOSFET Parameter and Parasitic Variations

In order to ensure perfect static and dynamic current sharing, all the relevant parameters should be made similar in value. Selection of component tolerances and careful symmetrical power and drive circuit layout will help minimize current imbalances caused by components and layout parasitic inductances and impedances The MOSFETs parasitics are more difficult to match. Table 2.8.1 below shows the variation of MOSFET parameters and parasitics expected during the production lifetime of a die. An expected value of 1.0 represents the typical value given in manufacturers data sheets.

Table 2.8.1 - MOSFET Parameter Variations [23].

Parameter	Expected Minimum	Expected Maximum	Variation Minimum	Variation Maximum
Turn On Delay (t_{don})	0.7	1 5	- 30%	+ 50%
Rise Time (t_r)	0.5	2.0	- 50%	+ 100%
Turn Off Delay (t_{doff})	0.5	2.0	- 50%	+ 100%
Fall Time (t_f)	0 5	2.0	- 50%	+ 100%
Gate Source Threshold Voltage (V_{gsth})	0.6	1.5	- 40%	+ 50%
Drain Source Resistance (R_{dson})	0.5	2.0	- 50%	+ 100%
Input Capacitance (C_{iss})	0.7	1 5	- 30%	+ 50%
Output Capacitance (C_{oss})	0.5	2.0	- 50%	+ 100%
Transconductance Capacitance (C_{rss})	0.6	1.6	- 40%	+ 60%

Table 2.8.1 also shows that the parameters which will determine the amount of current mismatch can vary by as much as 100% making accurate

prediction of losses and current mismatch difficult. From the numbers given in the data books, only best and worst case losses and current mismatch can be determined. It also shows that MOSFETs selected from different lots will most likely have different parameters and parasitics and thus current mismatch and higher than expected losses will result.

Since matching of all the parameters is impossible, PSPICE simulations were used to determine which parameters affected current imbalance the most. It was observed that R_{dson} most affected static current imbalance. C_{iss}, V_{gsth}, and g_{fs} affected dynamic current imbalance the most. These parameters vary greatly from production lots but also vary within the same production lots. Table 2.8.2 shows how these critical parameters and parasitics vary within the same production lot for the MTP8N20 MOSFET from Motorola.

Table 2.8.2 - MOSFET Parameter Variations Within Production Lots [24].

Wafer Lot	R_{dson}		g_{fs}		V_{gsth}		Sample Size
	Min.	Max.	Min.	Max.	Min.	Max.	
1	0.231	0.297	3.704	4.878	2.300	4.080	100
2	0.239	0.305	3.571	4.878	3.685	3.910	50

Normalized in terms of percentage Table 2.8.3 is obtained.

Table 2.8.3 - MOSFET Parameter Variations Within Production Lots (%)

Wafer Lot	R_{dson}		g_{fs}		V_{gsth}		Sample Size
	Min.	Max.	Min.	Max.	Min.	Max.	
1	-12.5%	+12.5%	-13.7%	+13.7%	-27.9%	+27.9%	100
2	-12.1%	+12.1%	-16.5%	+16.5%	-3.0%	+3.0%	50

Table 2.8.3 shows that even within the same production lots, selecting MOSFETs at random will result in parameter variations which will make static and dynamic current sharing difficult. In order to maximize current sharing between MOSFETs extra circuitry will be required or matching parameters of paralleled components will be necessary. This will depend on cost considerations, the intent of paralleling and of course whether hard or soft switching topologies are used. Another method to increase current sharing would be to insist manufactures specify key parameters such as R_{dson}, g_{fs}, C_{iss}, and V_{gsth}, with tighter tolerances, but this does not seem feasible unless the design engineer is willing to commit to large production orders and higher costs. This technique would not involve any changes in the manufacturing process but tighter screening during testing and selection of the devices [25].

2.9 Paralleling and MOSFET Parameter and Parasitic Variations

Considering the variation of parameters and parasitics, and assuming proper layout techniques were used to make the MOSFETs power and drive circuits symmetrical, there are other affects which will occur when MOSFETs are paralleled. The variation of R_{dson} will force more current through one device resulting in some static current imbalance. The variation of C_{iss} and V_{gsth} will result in one device turning on before the other and carrying the full current resulting in a dynamic current imbalance. This becomes more dominant as frequency increases and the time when only one device is on becomes larger in percentage terms. Also, the variation of the transconductance g_{fs}, will affect the dynamic current sharing as the devices turn on. All these variation will affect the current imbalance and result in higher than expected losses.

CHAPTER 3

HARD SWITCHING PWM AND PARALLELED MOSFETs

3.1 Introduction

Hard Switching PWM (HS-PWM) is the most popular modulation technique presently used in switching power supplies. As mentioned in Chapter 1, HS-PWM is a modulation technique used to control the output voltage which does not take the voltage across, and current through the switching element into account when the element is turned on and off. As a result, HS-PWM converters exhibit both conduction and switching losses. Since switching losses increase with increasing switching frequency, converters using this topology are limited to lower operating frequencies. In this chapter, a converter using HS-PWM will be described, and simulated in terms of losses with a single switch and with paralleled switches. Experimental results will also be obtained for the converter using single and multiple switches.

3.2 Hard Switching PWM Topology

Figure 3.2.1 shows a HS-PWM full bridge converter circuit which was simulated. MOSFETs Q1, Q2, Q3 and Q4 are used to generate a

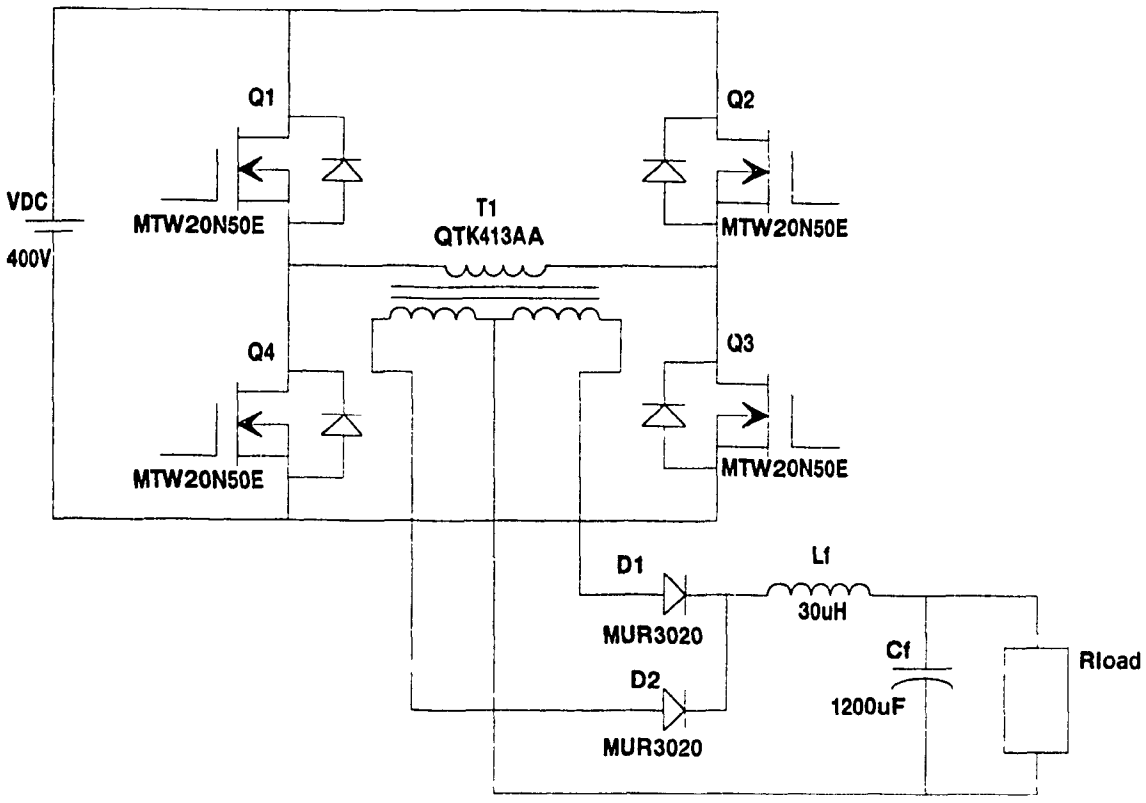


Figure 3.2.1 - HS-PWM Full Bridge Converter

high frequency bipolar waveform which will not saturate transformer T1. This transformer is used to provide impedance matching, and galvanic isolation between the power source and the load. This is desirable because optimization of the MOSFETs and filter components is obtained when the duty cycle is fully utilized. Diodes D1 and D2 are used to rectify the bipolar waveform from the secondary of the transformer. Inductor Lf and capacitor Cf form a low pass filter which allows the DC component to flow to the load and attenuates the high frequency components generated by the switching action of the converter. The filter decreases the ripple voltage at the load and also reduces EMI presented to the load.

The MOSFETs are switched so that Q1 and Q3, or Q2 and Q4 are on, or all the MOSFETs are off. By controlling the MOSFETs in this manner a bipolar waveform with a varying duty cycle can be generated at the primary of the transformer T1. The volt-second product of the positive cycle (Q1 and Q3 on) must equal the volt-second product of the negative cycle (Q2 and Q4 on) in order to prevent the transformer T1 from saturating. Voltage control is achieved by varying the duty cycle, that is the time the MOSFETs are on with respect to a fixed time period (fixed frequency). Higher duty cycles will produce higher output voltages across the capacitor Cf.

3.3 Single MOSFET HS-PWM Simulated and Experimental Results

As mentioned earlier, hard switching occurs when the MOSFETs are turned on and off irregardless of the voltage across or the current flowing through them. This is the most common switching technique used in switching power supplies. The PSPICE model of the MOSFET described in chapter 2 was used in simulations to observe the charging currents of the parasitic capacitances around the MOSFET.

3.3.1 HS-PWM Turn On Transition

Figure 3.3.1 shows the MOSFET in its steady state off condition. The voltage across C_{ds} is *(0.5 x VDD)*, which is half the DC bus voltage. The drive circuit applies a negative voltage across the gate-source,

resulting in the gate-drain voltage across capacitor C_{gd} being *(0.5xVDD + VGS)*

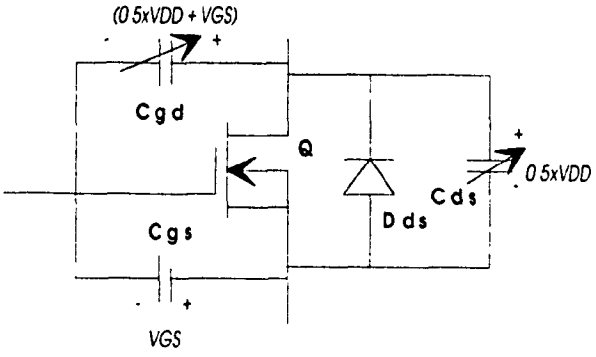


Figure 3.3.1 - HS-PWM Off Condition

To turn the MOSFET on, a positive gate-source voltage is applied as shown in Figure 3.3.2. Currents will flow from the drive circuit in order to charge capacitor C_{gs} to V_{gsth}, and capacitor C_{gd} to *(0.5xVDD - Vgsth)*. This current will flow from the drive source, through the gate resistance and will generate a power loss across this resistance.

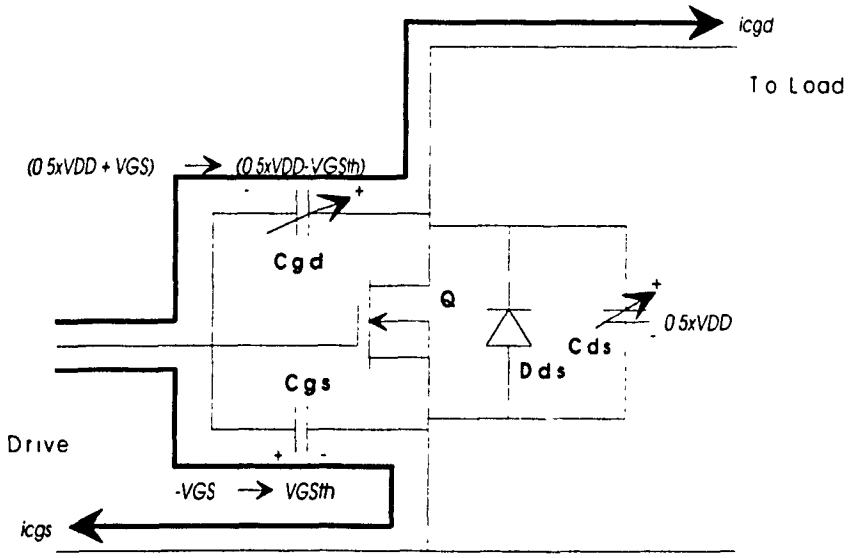


Figure 3.3.2 - HS-PWM Off Condition Vgs = Vgsth

Although the MOSFETs gate-source region is isolated by an oxide layer, a charging current will flow as the gate is charged and discharged when the MOSFET is turned on and off. A gate resistance is required to minimize oscillations during the switching of the MOSFET. The current path for the charging of capacitor C_{gd}, will flow through the load circuit before it returns to the drive supply.

When the capacitor C_{gs} is charged to V_{gsth}, the MOSFET will start to turn on as shown in Figure 3.3.3. This will short the capacitor C_{ds} across the MOSFET and result in the energy in capacitor C_{ds} being lost across the device Also, as the MOSFET turns on it will connect the capacitor C_{gd} across capacitor C_{gs} and will drain current away from the capacitor C_{gs} resulting in a slower turn on cycle for the time it takes to charge the capacitor C_{gd}. Also, the charge required to discharge the capacitor C_{gd} will result in a current flowing from the drive supply through the MOSFETs drain-source conduction channel. This current will also generate a power loss across the MOSFET. Switching losses also occur at this time as the voltage across the MOSFETs drain-source decreases to zero volts while the load current through the drain flows through the MOSFET. During this interval, the gate-drain capacitance C_{gd} and the drain-source capacitance C_{ds} are charged from $(0.5 \times VDD)$ to VDD. This charging current will also flow through MOSFET Q.

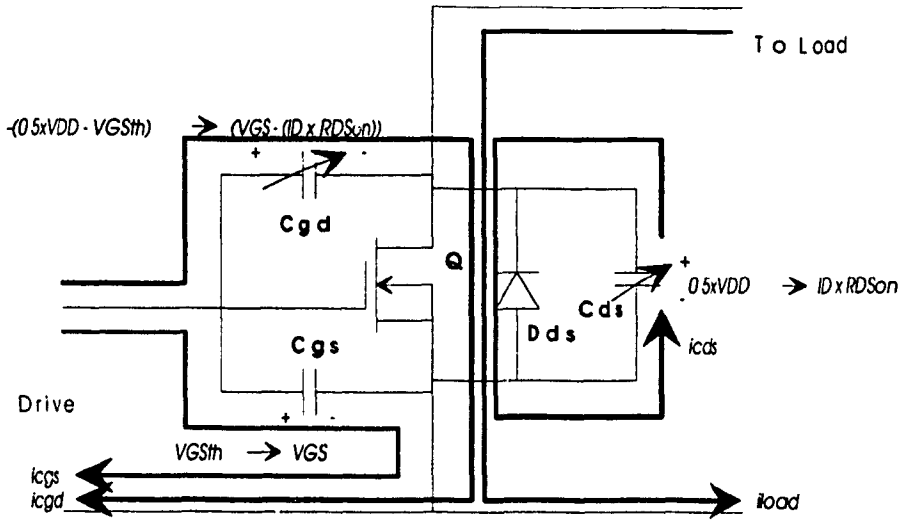


Figure 3.3.3 - HS-PWM Off Condition Vgs > Vgsth

Figure 3.3.4 shows the MOSFET when it is fully on. In this state the only losses across the MOSFET are the conduction losses caused by the drain current I_d and the R_{dson} of the device.

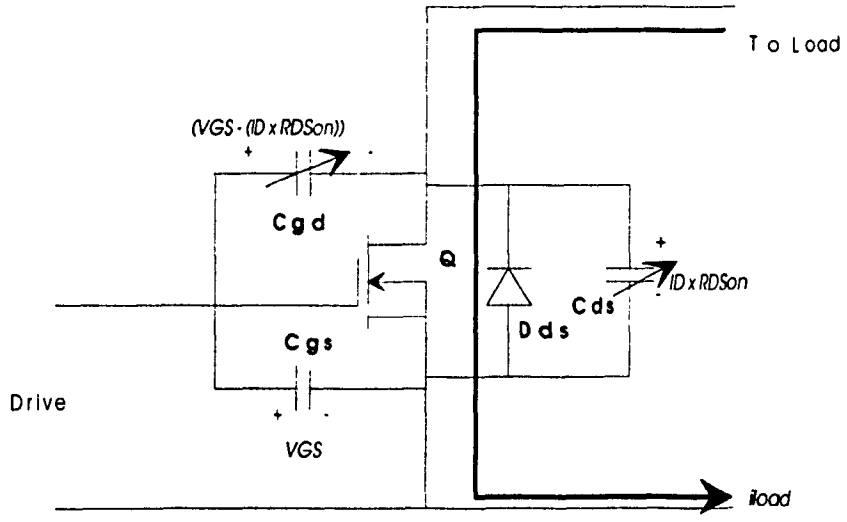


Figure 3.3.4 - HS-PWM On Condition

3.3.2 Losses During HS-PWM Turn On Transitions

When any charging current flows from the load or from the drive source through the gate resistance, losses will result. Thus losses will result when the gate-drain and gate-source capacitances C_{gd} and C_{gs}, are charged and discharged during the switching cycle. Also, as the MOSFET turns on the load current will start to flow through the drain-source conduction channel of the MOSFET before the impedance drops to R_{dson} and will generate a switching loss. During turn on, the drain-source capacitance C_{ds} will be discharged through the MOSFETs drain-source channel resulting in a loss of the energy stored. Once the MOSFET is fully on, the only losses will be conduction losses caused by the drain current I_d flowing through the drain-source channel which has a resistance of R_{dson}.

3.3.3 HS-PWM Turn Off Transition

The current flow during the MOSFETs turn off cycle is shown in Figures 3.3.5, 3.3.6, and 3.3.7. When the MOSFET is on, the parasitic capacitances C_{ds}, C_{gd}, and C_{gs} are charged to the levels shown in Figure 3.3.4. The turn off gate signal applied forces the gate-source capacitance C_{gs} to discharge to V_{gsth} and the gate-drain capacitance C_{gd} to discharge to *(Vgsth - (ID x RDSon))*. Again, the gate resistance will have these discharge currents flowing through it and will result in losses. The discharge current flow for the gate-source capacitance C_{gs} flows through the drive resistance to the drive source as is shown in

Figure 3.3.5. The discharge current path for the gate-drain capacitance C_{gd} is more complex and is dependent on the load. In general, this current will flow from the gate supply to the load and also through the source-drain channel of the MOSFET. The ratio will depend on the dynamic impedance of the MOSFET.

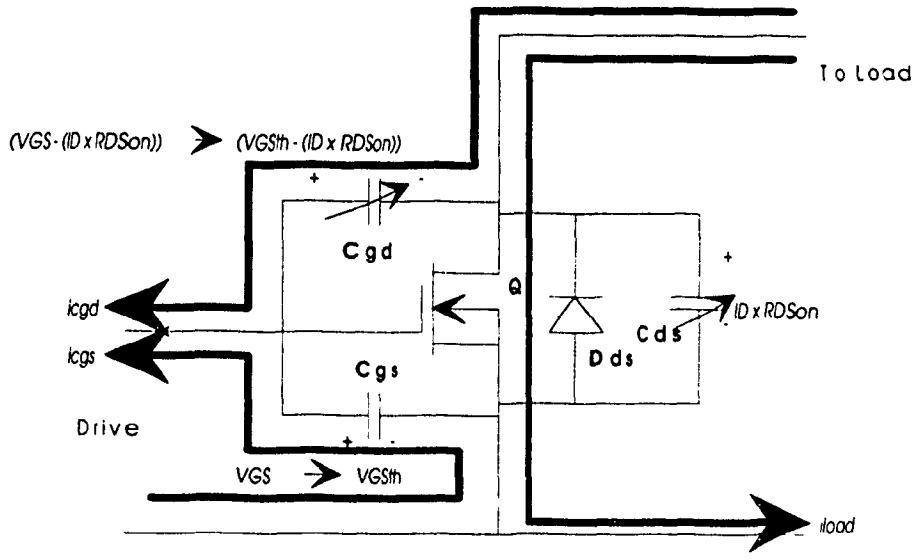


Figure 3.3.5 - HS-PWM On Condition Vgs > Vgsth

When the gate-source voltage reaches V_{gsth}, the MOSFET will start to turn off as shown in Figure 3.3.6. The drain current will flow through the drain-source channel of the MOSFET and when the drain-source voltage starts to rise towards the voltage *(0.5 x VDD)*, a charging current will flow from the load to the drain-source capacitance as its voltage also rises to *(0.5 x VDD)*. The gate-source voltage will continue to decrease from *Vgsth* to - *Vgs*, which will continue the flow of the gate-source current through capacitance C_{gs}. The voltage across the gate-drain capacitance C_{gd} will increase as the MOSFETs drain-source

voltage increases. This will make the gate-drain capacitance C_{gd} charge to *((0.5 x VDD) + VGS)*. The current to charge the gate-drain capacitance will again flow through the MOSFETs drain-source region, and also through the load circuit. As the MOSFET turns off, more of the gate-drain discharge current will flow through the load.

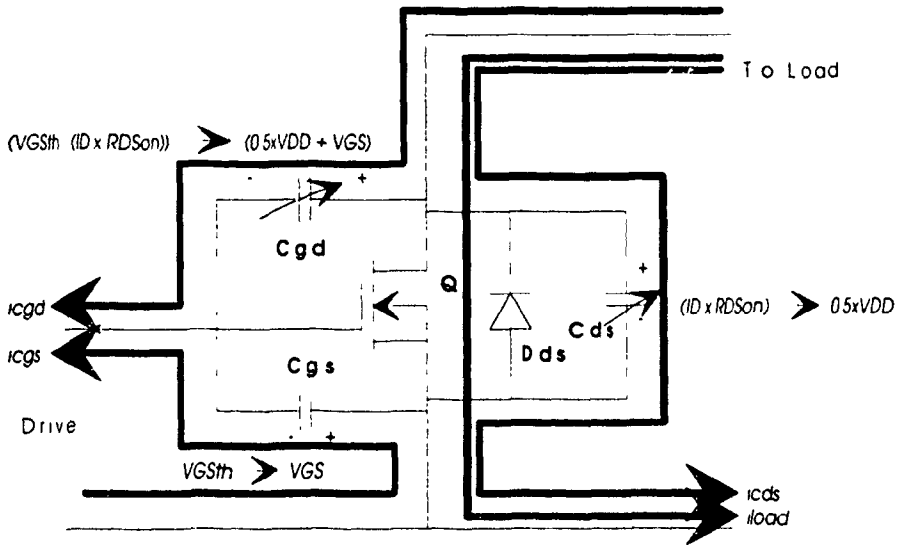


Figure 3.3.6 - HS-PWM On Condition Vgs < Vgsth

Figure 3.3.7 shows the steady-state off condition of the MOSFET. There are no currents flowing, other than the drain-source leakage current. The gate-source capacit ·ce C_{gs} is charged to - *VGS*, the drain-source capacitance C_{ds} is charged to *(0.5 x VDD)*, and the gate-drain capacitance C_{gd} is charged to - *(VGS + (0.5 x VDD))*.

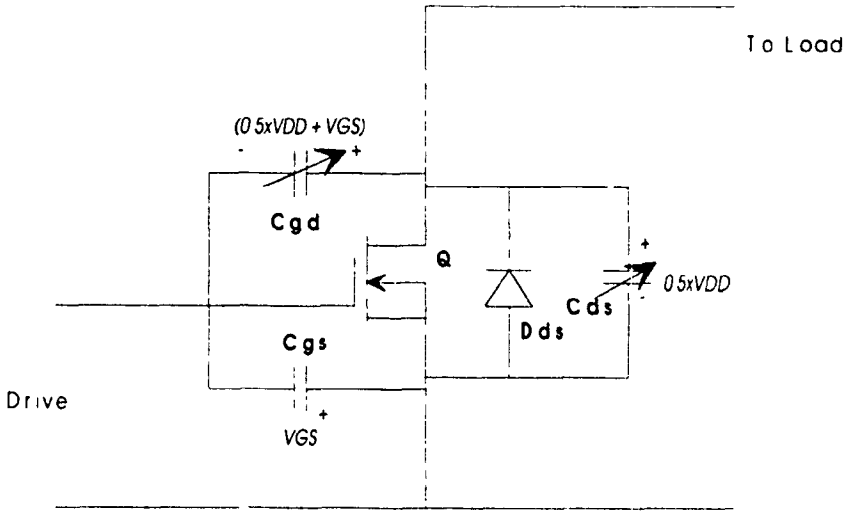


Figure 3.3.7 - HS-PWM Off Condition

3.3.4 Losses During HS-PWM Turn Off Transitions

As in the case when the MOSFET turned on, any charging current flowing through the gate-drain and gate-source capacitances C_{gd} and C_{gs}, will generate losses in the drive source resistor. Also, as the MOSFET turns off, the load current flowing through the MOSFET will generate a switching loss as the drain voltage rises to *(0.5 x VDD)*. The drain-source capacitance C_{ds} helps to divert some of the load current away from the conduction channel of the MOSFET at the cost of generating a turn on switching loss when it has to be discharged. Negligible leakage losses will be generated when the MOSFET is on because of the small off leakage current.

3.3.5 Single MOSFET HS-PWM Simulated Results

The MOSFET model described in Section 2 was used in the full bridge HS-PWM circuit shown in Figure 3.2.1 to obtain simulated results. The results presented in this section focus on the turn on and turn off conditions since charging and discharging of the parasitic components occurs during these intervals.

Figure 3.3.8 shows the parasitic capacitive currents which flow through MOSFET Q4 when MOSFET Q1 is turned on. At 140.5 uS, the drive signal of MOSFET Q1 is applied to turn it on. At 140.55 uS, MOSFET Q1 turns on allowing MOSFET Q4 drain-source capacitance C_{ds} to charge from *(0.5 x VDD)* to *VDD*. The gate-drain capacitance C_{gd} of MOSFET Q4 also charges from *((0.5 x VDD)-(-Vgs))* to *(VDD-(-Vgs))* Current also flows through the gate-source capacitance C_{gs} of MOSFET Q4 since it carries some of the current used to charge its gate-drain capacitance C_{gd}. At 140.7 uS the drain-source capacitance C_{ds} and the gate-drain capacitance C_{gd} of MOSFET Q4 will be charged Current will flow through the gate-source capacitance C_{gs} as the gate drive circuit of MOSFET Q4 tries to recharge this capacitance to - *Vgs*.

Figure 3.3.9 shows the parasitic capacitive currents which will flow through MOSFET Q4 when it is turned on. At 144.3 uS the gate-source signal is applied to MOSFET Q4. Current will first start to flow through the gate-source capacitance C_{gs} of MOSFET Q4 as it charges from - *VGS* to its threshold voltage + *Vgsth*. When the gate-source threshold voltage is reached at 144.4 uS, MOSFET Q4 will start to turn on.

Currents will start to flow through the gate-drain and drain-source capacitances, C_{gd} and C_{ds} respectively as they start to discharge. The gate-source capacitance C_{gs} stops charging when the MOSFET Q4 turns on because the drive current is diverted away from the gate-source capacitance C_{gs} to discharge the gate-drain capacitance C_{gd}. In fact, the negative current flowing through the gate-source capacitance C_{gs} at 144.4 uS shows that some charge is taken from it in order to charge the gate-drain capacitance C_{gd}. After MOSFET Q4 has turned on at 144.45 uS, no significant current will flow through the drain-source and drain-gate capacitances. Current will flow through the gate-source capacitance C_{gs} as it continues to charge to + *Vgs*.

Figure 3.3.10 shows how the load current is supplied from the MOSFETs Q1 and Q4 during the turn on of MOSFET Q1. At 140.5 uS, MOSFET Q1 is turned on when the gate-source voltage signal is applied. When MOSFET Q1 turns on at 140.55 uS there is a large drain current which flows internally to MOSFET Q1. This current is caused by the discharging of the drain-source and gate-drain capacitances, C_{ds} and C_{gd}, of MOSFET Q1, and the charging of the drain-source and gate-drain capacitances, C_{ds} and C_{gd}, of MOSFET Q4. In Figure 3.3.10 this charging and discharging current is denoted as *Ia*. After MOSFET Q1 parasitic capacitances have discharged and MOSFET Q4 parasitic capacitances have charged at 140.65 uS, MOSFET Q1 will carry the full load current *I(LSA)*.

When MOSFET Q4 is turned on at 144.3 uS it will also be required to discharge its drain-source and gate-drain capacitances, C_{ds} and C_{gd}, as well as charge the drain-source and gate-drain capacitances of MOSFET

Q1 as shown in Figure 3.3.11. This charging and discharging current is denoted as *Ia*. At 144.4 uS the drain-source and gate-drain capacitances of MOSFET Q4 will be discharged and the drain-source and gate-drain capacitances of MOSFET Q1 will be charged. At this time the full load current *I(LSA)* will be carried by MOSFET Q4.

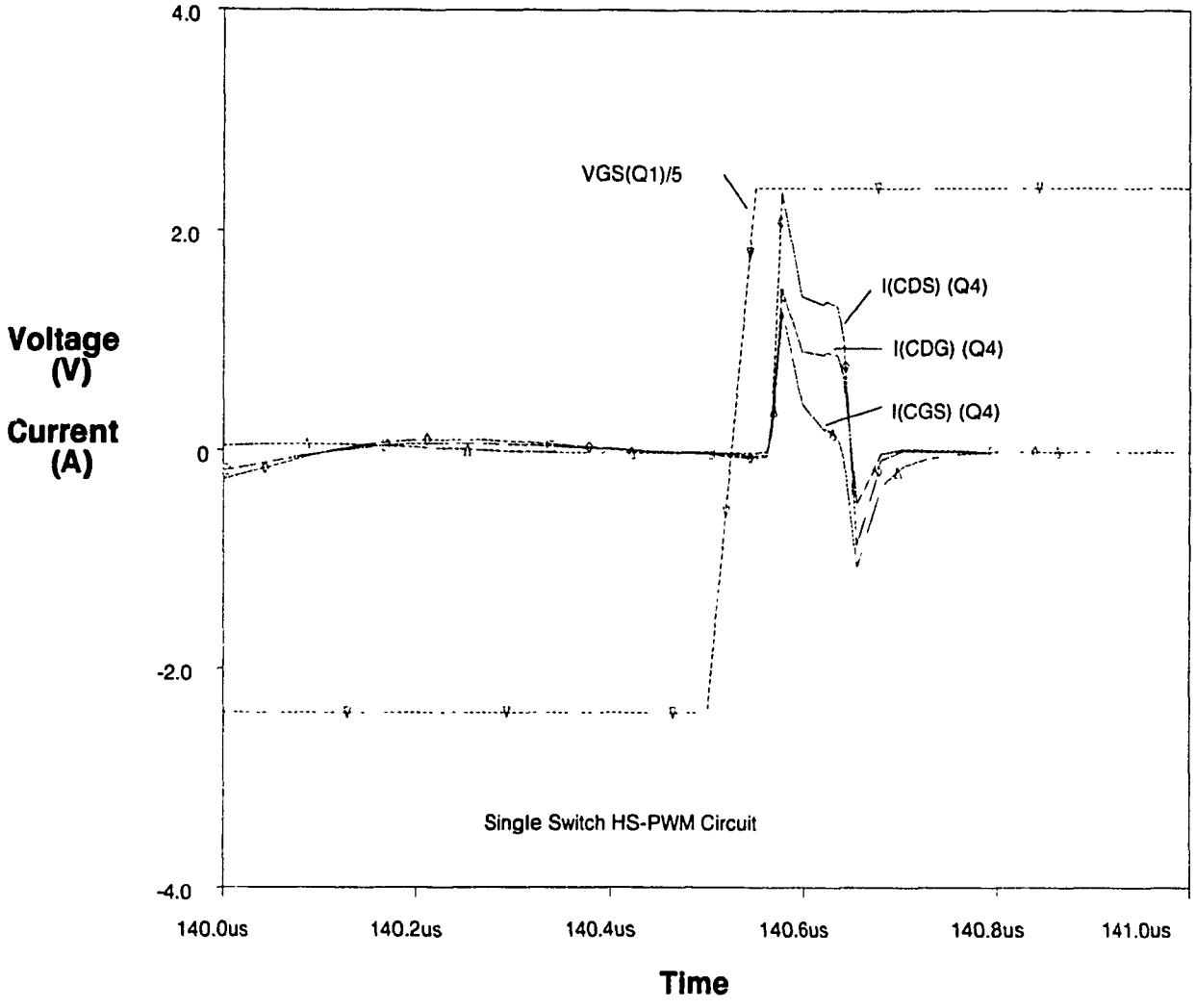


Figure 3.3.8 - HS-PWM MOSFET Q4 Turn Off, Q1 Turn On Parasitic Capacitive Currents

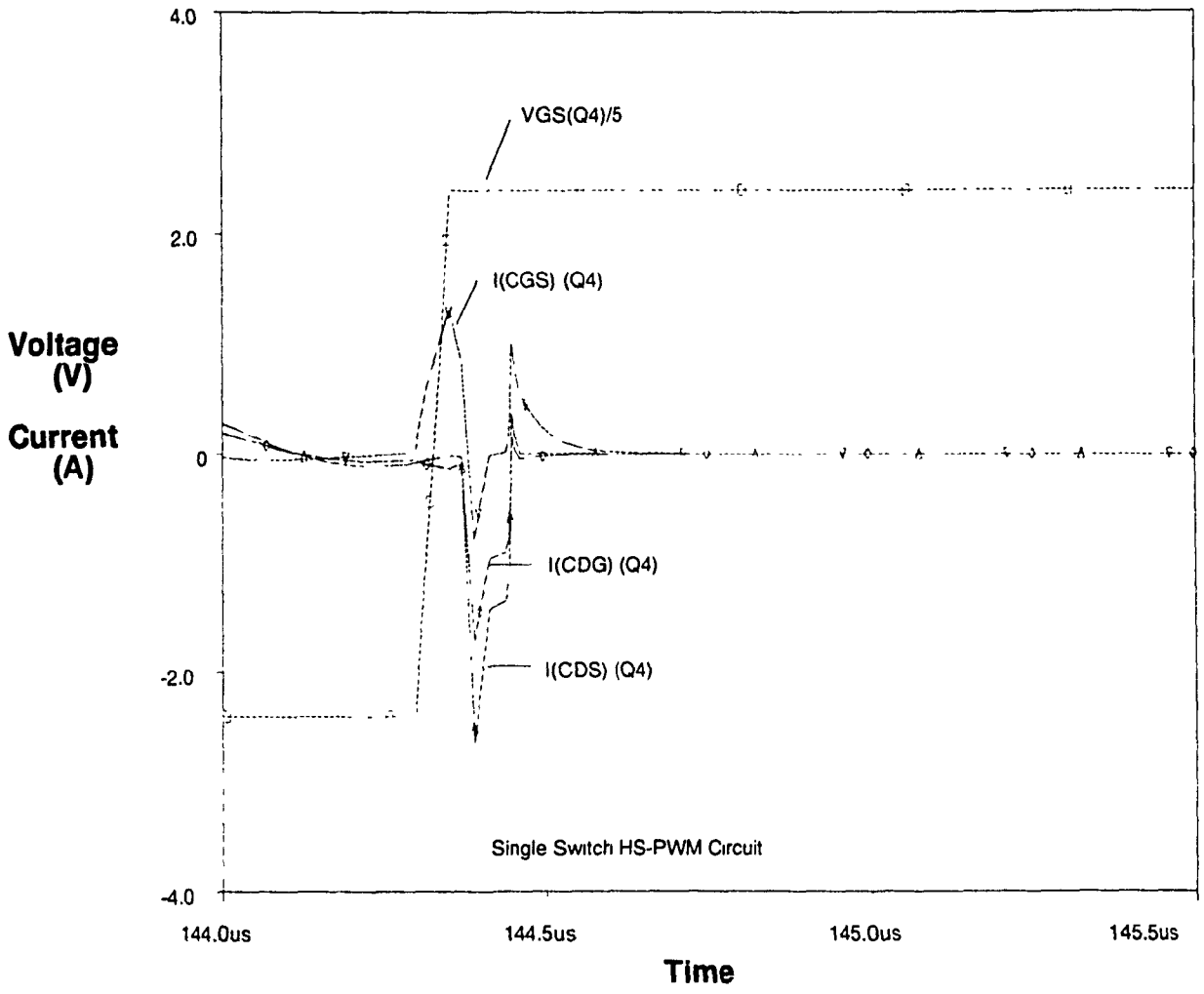


Figure 3.3.9 - HS-PWM MOSFET Q4 Turn On Parasitic Capacitive Currents

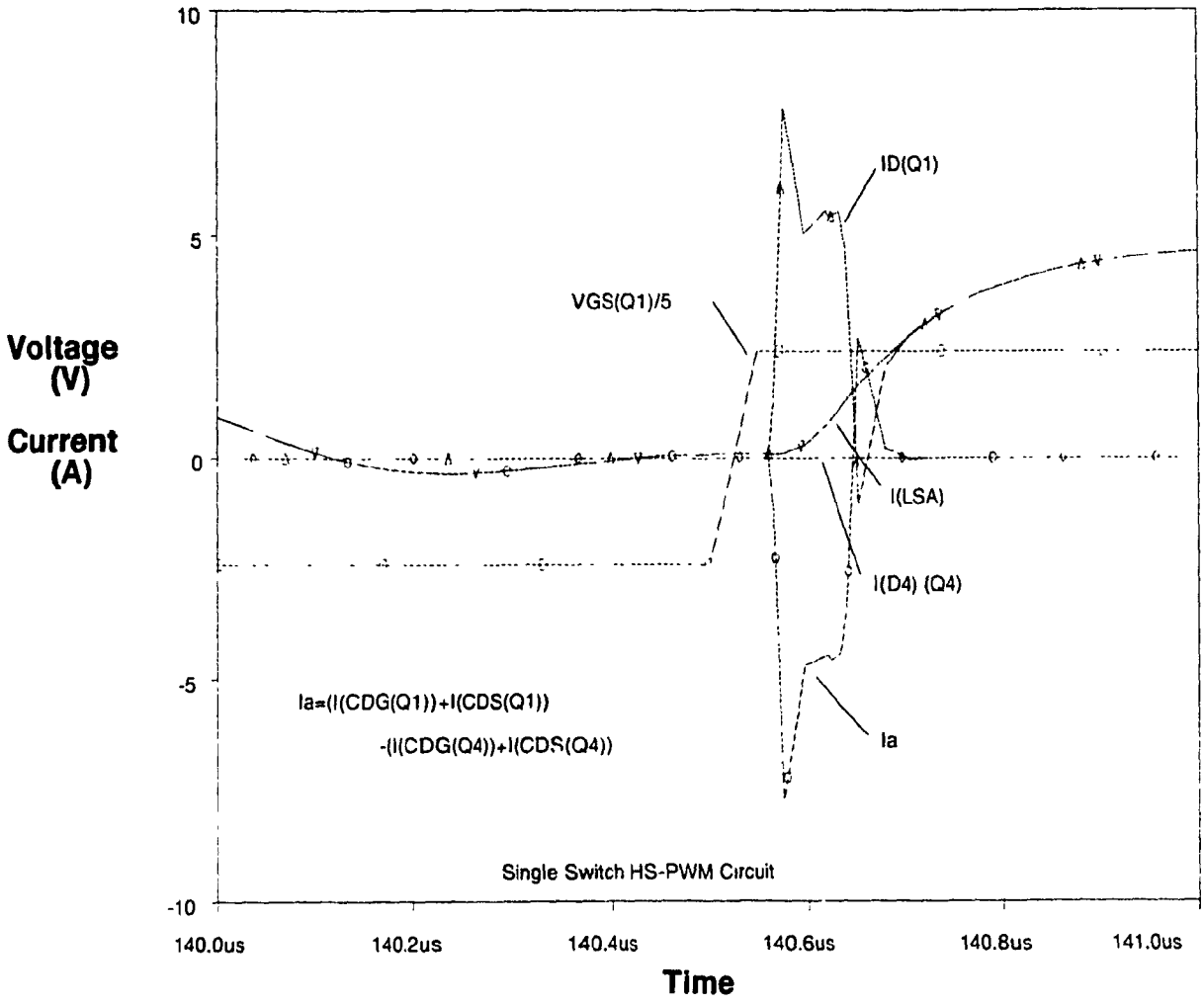


Figure 3.3.10 - HS-PWM MOSFET Q1 Turn On Capacitive, Drain and Body Diode Currents

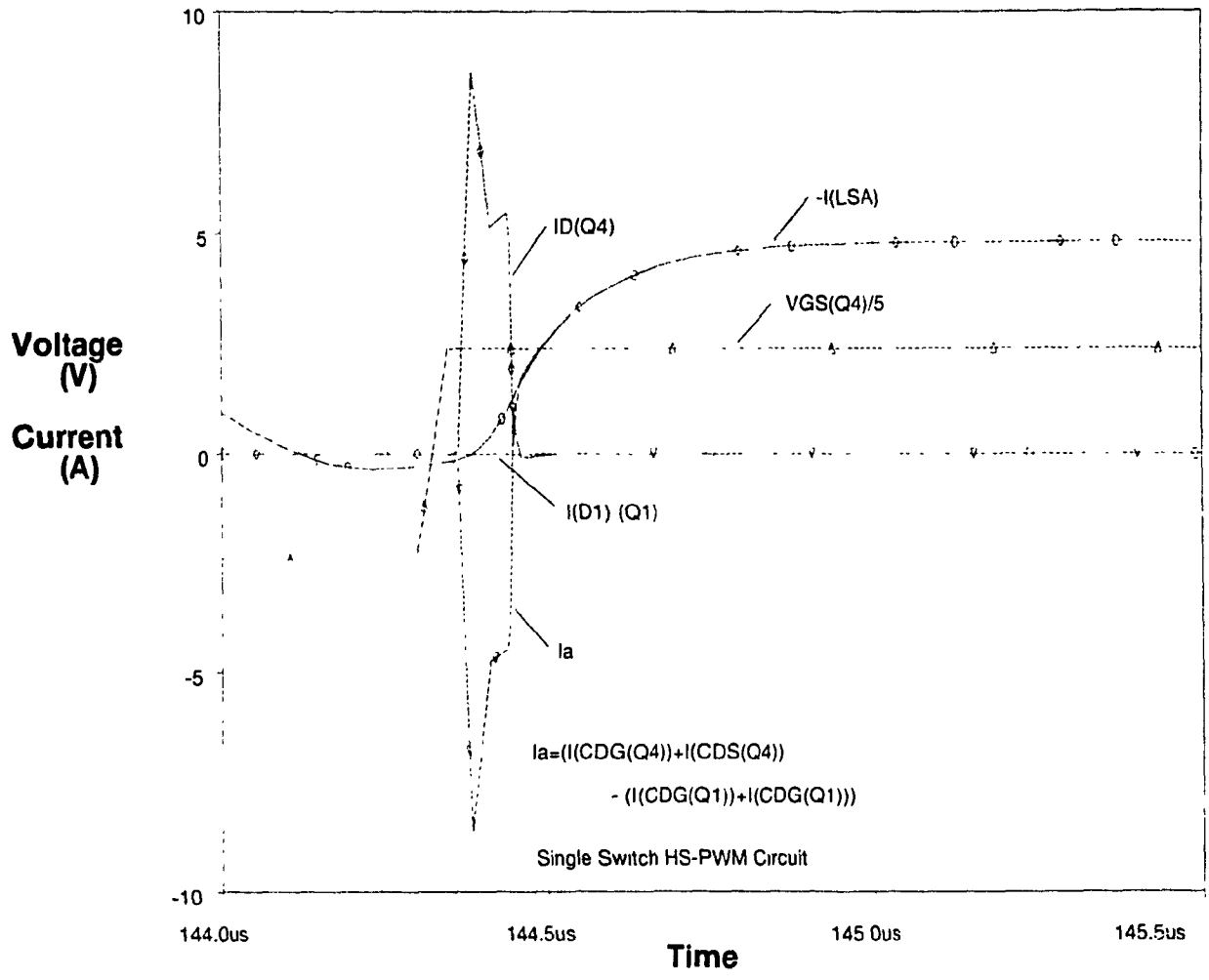


Figure 3.3.11 - HS-PWM MOSFET Q4 Turn On Capacitive, Drain and Body Diode Currents

3.3.6 Single MOSFET HS-PWM Experimental Results

Experimental results were obtained when the HS-PWM circuit was connected as shown in Figure 3.3.12. The experimental results obtained along with the simulated results are shown in Table 3.3.1. Simulated results were obtained by using the PSPICE program to simulate the circuit using the MOSFET model described in Chapter 2. The PROBE sub-program of PSPICE was used to graph the waveforms and mathematically generate loss plots which were then read from the graph by the cursor function.

The experimental results were obtained by comparing the output power of the converter to the input power supplied to it. The output power was obtained by multiplying the output current *Ao*, with the output voltage *Vo*. The output current was obtained by using a Keithley 179A TRMS ammeter which could read the current to 5 significant figures. The voltage was read by a Keithley 179A TRMS voltmeter which could read the voltage to 4 significant figures. The input power was obtained by multiplying the input current *Ai*, with the input voltage *Vi*. The same ammeter was used to read both the input and output currents. Also, the same voltmeter was used to read the input and output voltages.

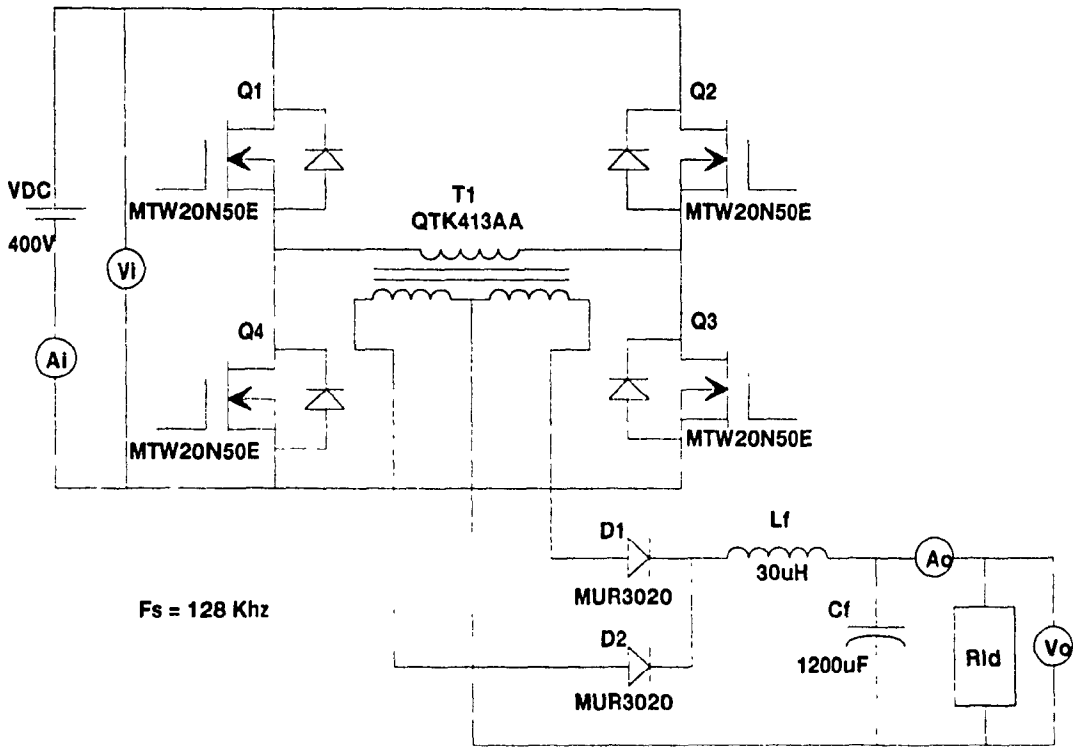


Figure 3.3.12 - HS-PWM Circuit Set-up for Efficiency Measurements

It was necessary to read the output DC voltage and current because the high frequency output waveform at the bridge could not be accurately measured by the laboratory equipment available. The losses of the transformer T1, diodes D1 and D2, resonant inductors LSa and LSb, and filter inductor Lf were estimated by subtracting the simulated single switch converter losses from the experimental losses obtained. The losses of T1, D1 and D2, and Lf were then assumed to remain constant as the switches were paralleled since the current and voltage applied to the bridge remained constant. Any difference in the losses were due to the effects of paralleling MOSFETs. Table 3.3.1 shows a comparison of the losses obtained.

Table 3.3.1 Comparison of Experimental, and Simulated Losses for Single HS-PWM MOSFETs

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
1	23.92 W	65.80 W	23.92 W

3.3.7 Summary of Losses for Single MOSFET HS-PWM Topology

When single MOSFETs are used, there will be conduction losses due to the resistance of the drain-source conduction channel and switching losses due to the charging and discharging of the devices parasitic capacitances. Switching losses will also result due to the topology which will cause the drain-source current to flow through the MOSFETs even though voltage is present across its drain-source.

3.4 Two Paralleled MOSFETs HS-PWM Simulated and Experimental Results

When MOSFETs are paralleled, the parasitic capacitances C_{gs}, C_{dg} and C_{ds} of both devices are effectively placed in parallel. If the multiple combination of MOSFETs is considered as a single switch, it will have twice the current handling capability and twice the parasitic

capacitances. If the multiple combination of MOSFETs is analyzed as two separate switches, it is unlikely that they will turn on and off at the same time unless they are matched as mentioned in Chapter 2. These differences in turn on and turn off times will generate different current flows from those generated by a single switch.

3.4.1 HS-PWM Turn On Transition

Figure 3.4.1 shows the two parallel MOSFETs in the off condition in a HS-PWM topology. The voltages across the parasitic capacitances C_{ds}, C_{gd}, and C_{gs} are the same in this case as in the single switch example.

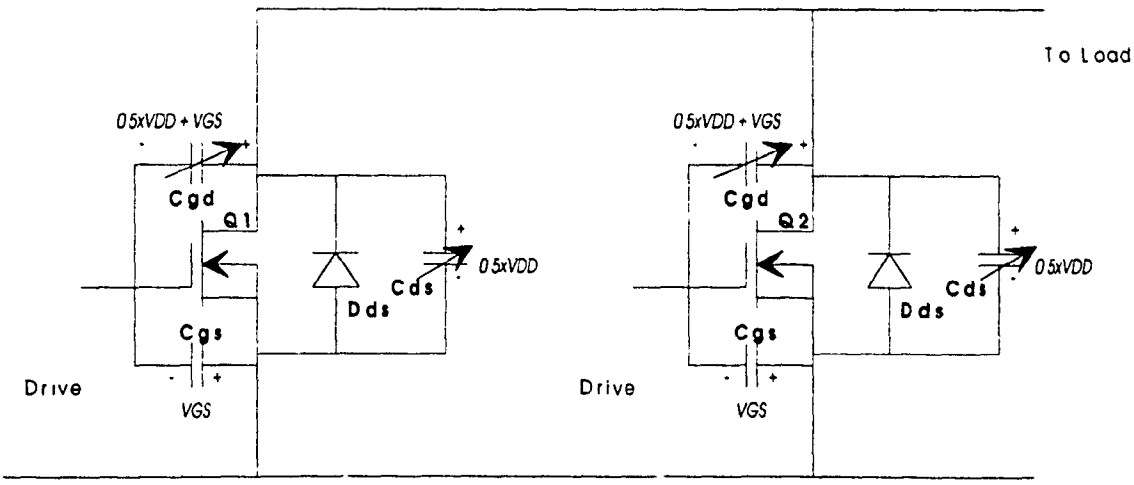


Figure 3.4.1 - HS-PWM Off Condition

When a gate signal is applied to turn the two MOSFETs on, the gate-source capacitances C_{gs} of both MOSFETS will start charging to V_{GSth} and both gate-drain capacitances C_{gd} will start charging to ((0.5

x VDD) - VGSth) as shown in Figure 3.4.2. This will cause a charging current to flow through the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} of both MOSFETS.

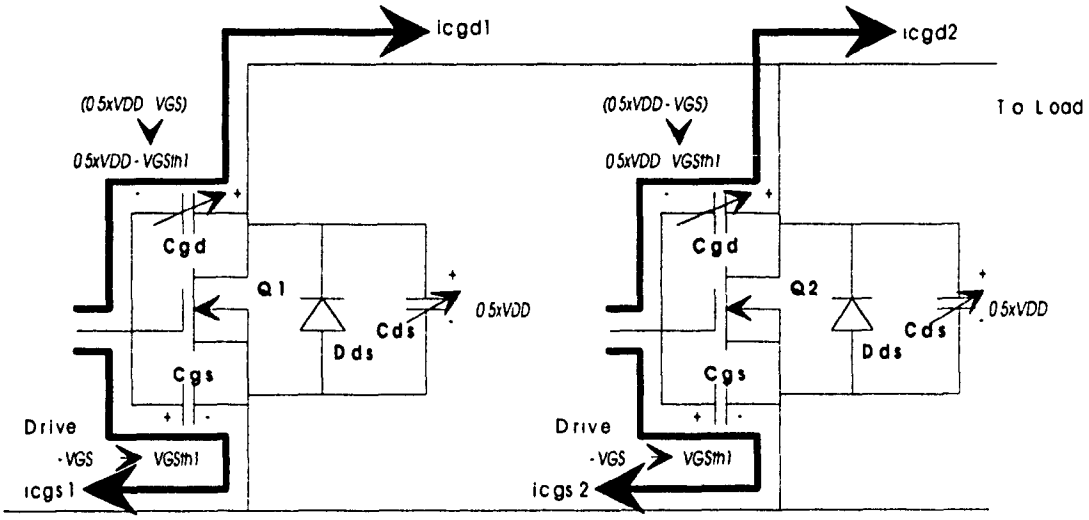


Figure 3.4.2 - HS-PWM Off Condition Vgs < Vgsth

Figure 3.4.3 shows the condition when one MOSFET reaches its gate-source threshold voltage first. In this example, MOSFET Q1 has a lower gate-source threshold voltage and thus turns on first. The parasitic capacitances of MOSFET Q1 will charge and discharge in the same manner as in the single switch case: drain-source capacitance C_{ds} will discharge through MOSFETs Q1 drain-source conduction channel, gate-drain capacitance C_{gd} will continue to charge but through MOSFET Q1 and not the load circuit, and the gate-source capacitance C_{gs} will charge to *VGS*. The parasitic capacitances C_{ds} and C_{gd} of MOSFET Q2 will charge and discharge through MOSFET Q1 and not MOSFET Q2. The load current however will only flow through the drain-source channel of MOSFET Q1.

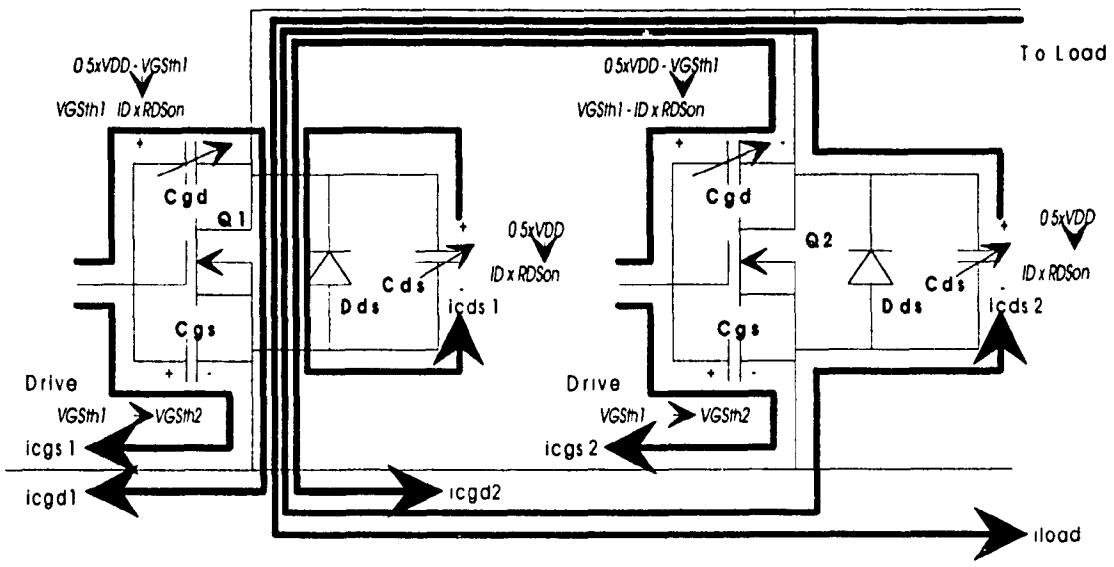


Figure 3.4.3 - HS-PWM Off Condition Vgs = Vgsth1 (Q1 Turns on First)

Both the MOSFETs gate-source voltage will continue to rise until the gate-source threshold voltage of MOSFET Q2 is reached as shown in Figure 3.4.4. During this interval, charging current will flow through both MOSFETs parasitic capacitances C_{gd} and C_{gs}.

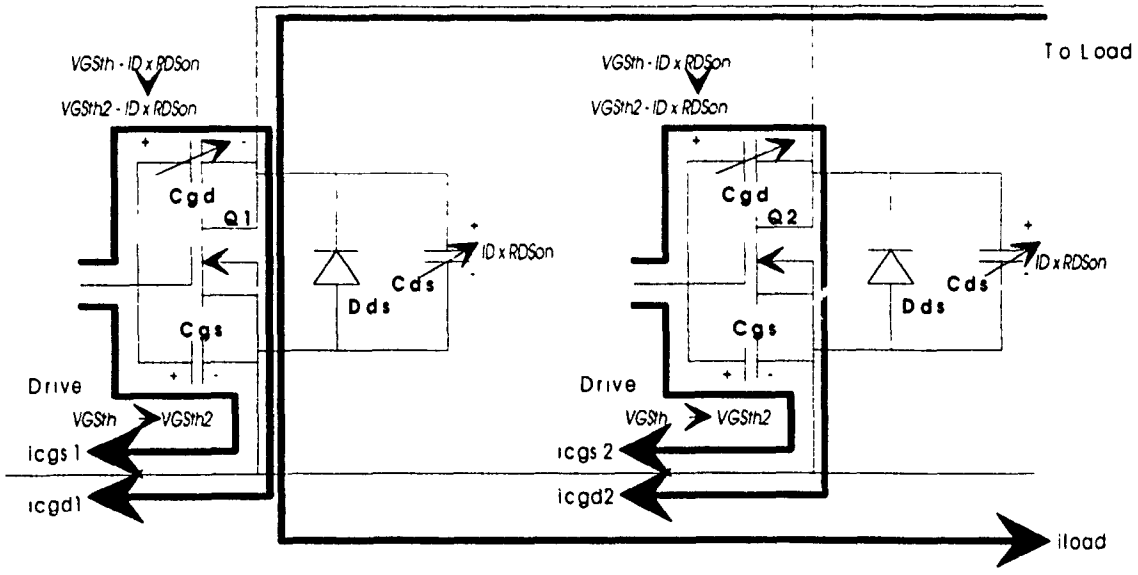


Figure 3.4.4 - HS-PWM Off Condition Vgs = Vgsth2 (Q2 Turns on)

When the gate-source voltage of MOSFET Q2 is equal to its threshold level, MOSFET Q2 will turn on as shown in Figure 3.4.5. At this instant, both MOSFETs will be conducting the load current. When MOSFET Q2 starts to conduct, its losses will be small because MOSFET Q1 discharged MOSFET Q2 drain-source capacitance C_{ds}. Also, the gate-drain and gate-source capacitances C_{gd} and C_{gs} of both MOSFETS will conduct current as the voltage across them changes.

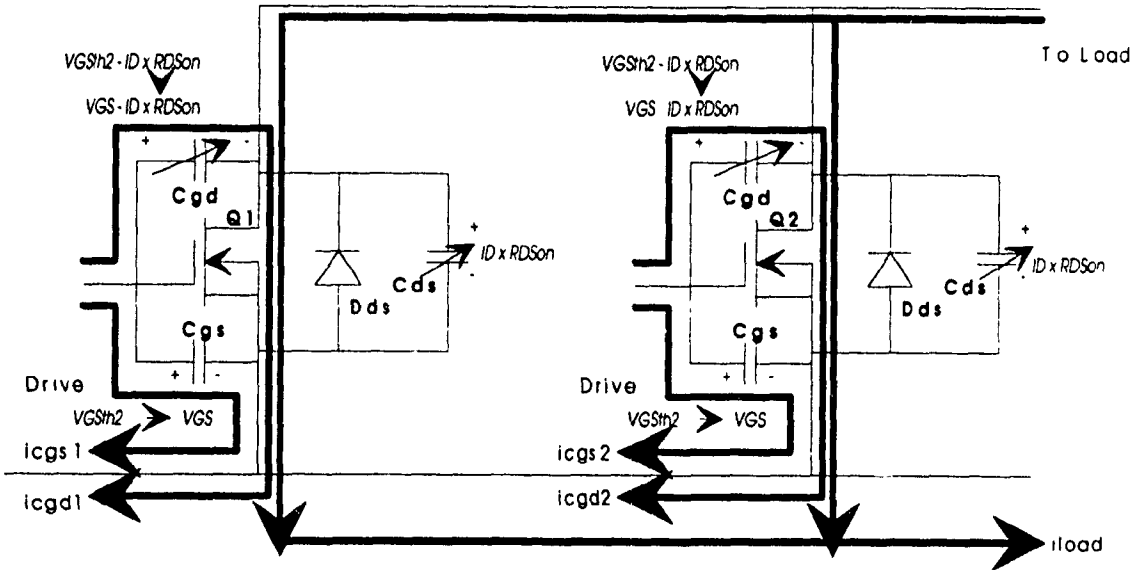


Figure 3.4.5 - HS-PWM On Condition Vgs > Vgsth2 (Q1 and Q2 On)

When the gate-source voltage reaches *VGS*, the charging currents will stop flowing through the parasitic capacitances C_{gs} and C_{gd} of both MOSFETs and the devices will be in their steady state on condition as shown in Figure 3.4.6. The load current will be shared between the MOSFETs and flow through their drain-source conduction channels. The

voltage across both gate-source capacitances C_{gs} will be *VGS*, the voltage across both gate-drain capacitances will be *(VGS - (ID x RDSon))* and the voltage across both drain-source capacitances C_{ds} will be *(ID x RDSon)*.

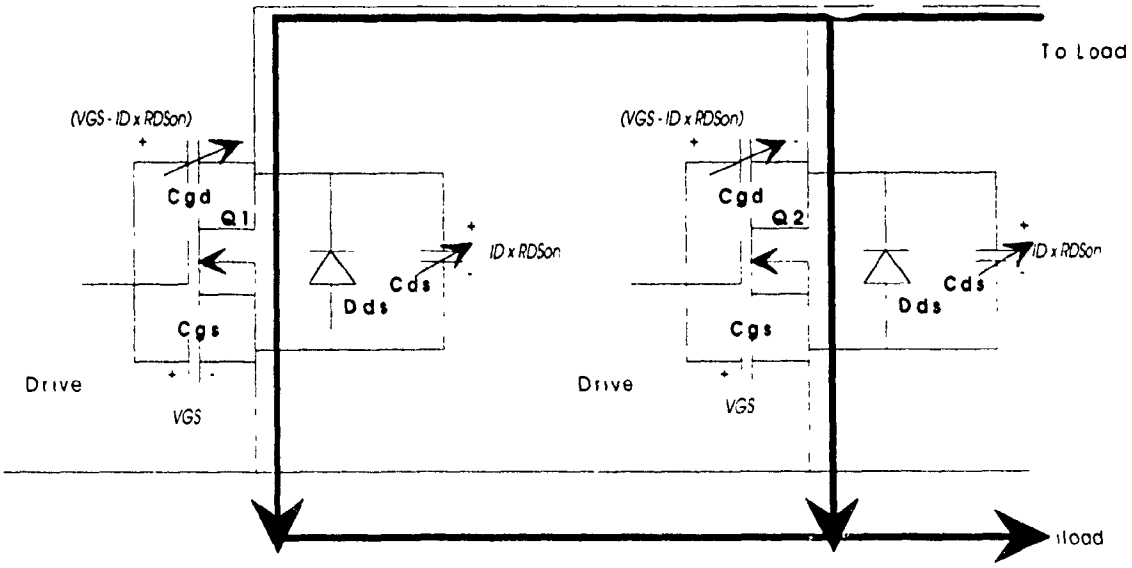


Figure 3.4.6 - HS-PWM On Condition

3.4.2 Losses During HS-PWM Turn On Transitions

As in the single MOSFET case, the currents flowing through the gate-source and gate-drain capacitances C_{gs} and C_{gd} will generate losses because they will also flow through the drive source resistance. Although one MOSFET will turn on with no losses, the MOSFET which turns on first will have to discharge the drain-source capacitances C_{ds} of both MOSFETs. This results in having more losses as compared to the single switch case, since there will be more drain-source capacitance

C_{ds} for paralleled MOSFETs. Also, more drive power will be required to charge and discharge the higher gate-source capacitances C_{gs} and the higher gate-drain capacitances C_{gd}. These charging losses are a function of frequency and increase as the switching frequency increases.

Conduction losses on the otherhand, will be less because of the lower effective R_{dson} which results when multiple MOSFETs are used. The greatest savings occur when both MOSFETs turn on at the same time. As mentioned above in Chapter 2, this is a highly unlikely condition. Practically, there will always be a delay between the turn on of both MOSFETs. During this period, the conduction losses will be similar as if only one MOSFET was used. Since this delay period is a function of the MOSFETs transconductance g_{fs}, gate-source threshold voltage V_{gsth}, and input capacitance C_{iss}, the delay will be constant to the particular MOSFET combination. The delay will also be independent of the switching frequency. Therefore, as the switching frequency is increased, the delay will become more significant with respect to the conduction period. This will diminish the savings in conduction losses. This shows that the efficiency gained by paralleling MOSFETS in HS-PWM topologies diminishes as switching frequency is increased.

Finally, assuming the same heatsink size is used, the MOSFETs will operate at lower case temperature resulting in lower R_{dson} values and lower conduction losses for a given current. This effect however is small and can be neglected in the analysis. Also, power designers tend to accept a higher heatsink temperature to decrease the size of the power supply.

3.4.3 HS-PWM Turn Off Transition

Figure 3.4.7, shows when the turn off gate signal is applied to the MOSFETs. Currents will flow from the load circuit to the gate drive circuit through the gate-drain capacitances C_{gd}, and circulate in the gate drive circuit through the gate-source capacitances C_{gs} as in the single switch case.

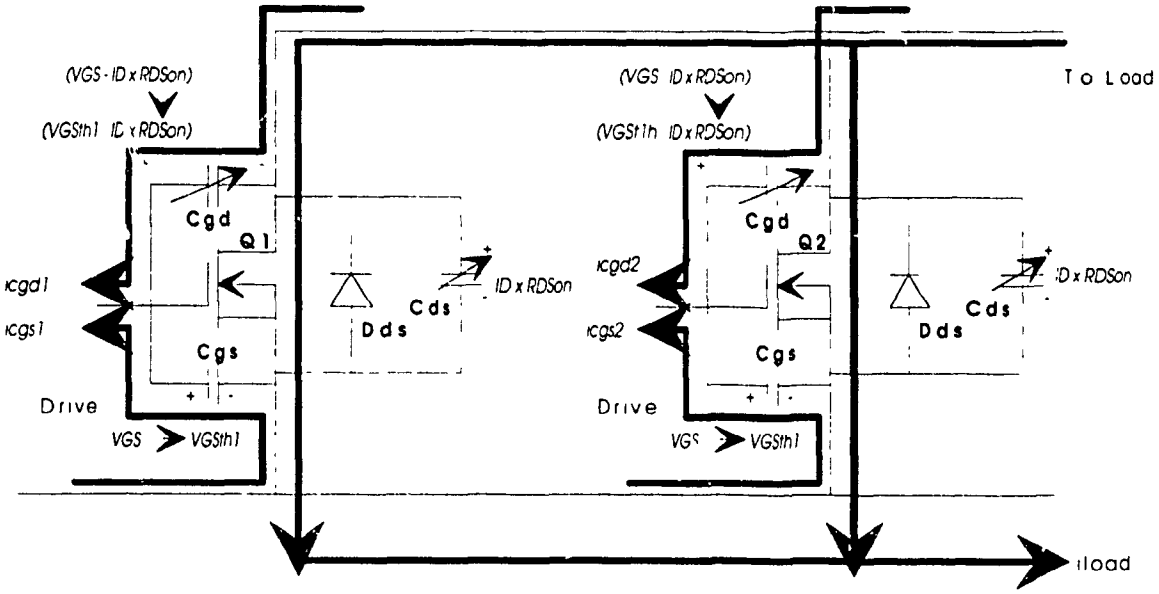


Figure 3.4.7 - HS-PWM On Condition Vgs > Vgsth

When the gate-source threshold voltage V_{gsth} is reached by MOSFET Q1, it will start to turn off as shown in Figure 3.4.8. MOSFET Q1 however will turn off with no losses because MOSFET Q2 is still conducting and will carry the full load current. The currents through the parasitic capacitances C_{dg} and C_{gs} will continue to flow during this period.

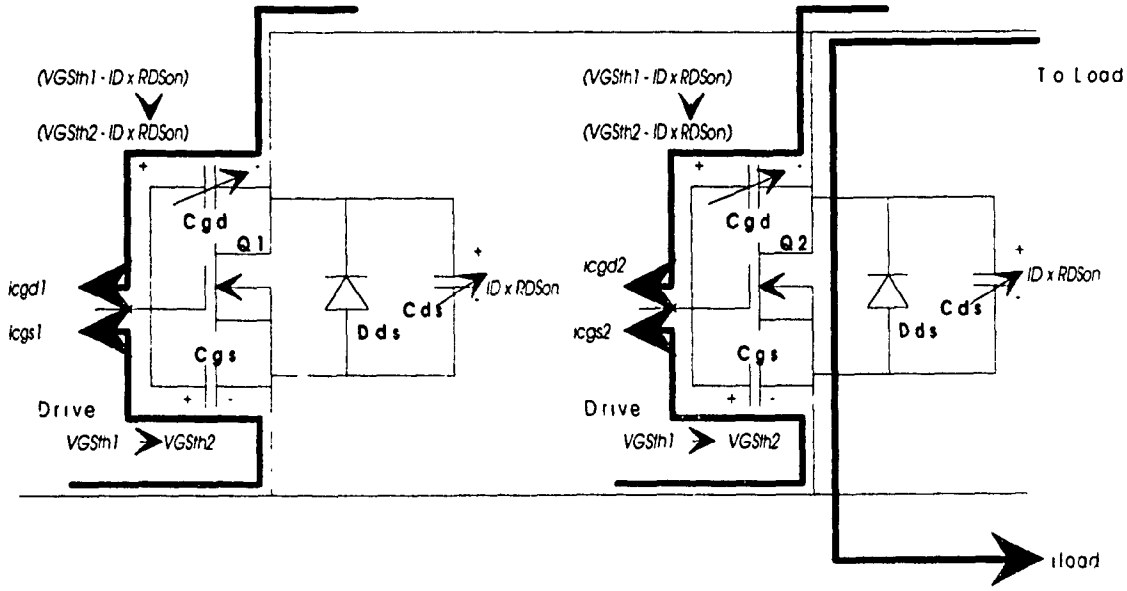


Figure 3.4.8 - HS-PWM On Condition Vgs < Vgsth1 (Q1 Turns off First)

When the gate source threshold voltage V_{gsth} of MOSFET Q2 is reached, it will start to turn off as shown in Figure 3.4.9. Current will flow through the drain-source channel of MOSFET Q2 and also through the drain-source capacitances C_{ds} of both MOSFETs as the drain-source voltage increases across MOSFET Q2. Again, currents will continue to flow through the gate-drain capacitances C_{gd} as the drain-source voltage increases. Currents will also flow through the gate-source capacitances C_{gs} as the gate drive circuit lowers the gate-source voltage *VGS*.

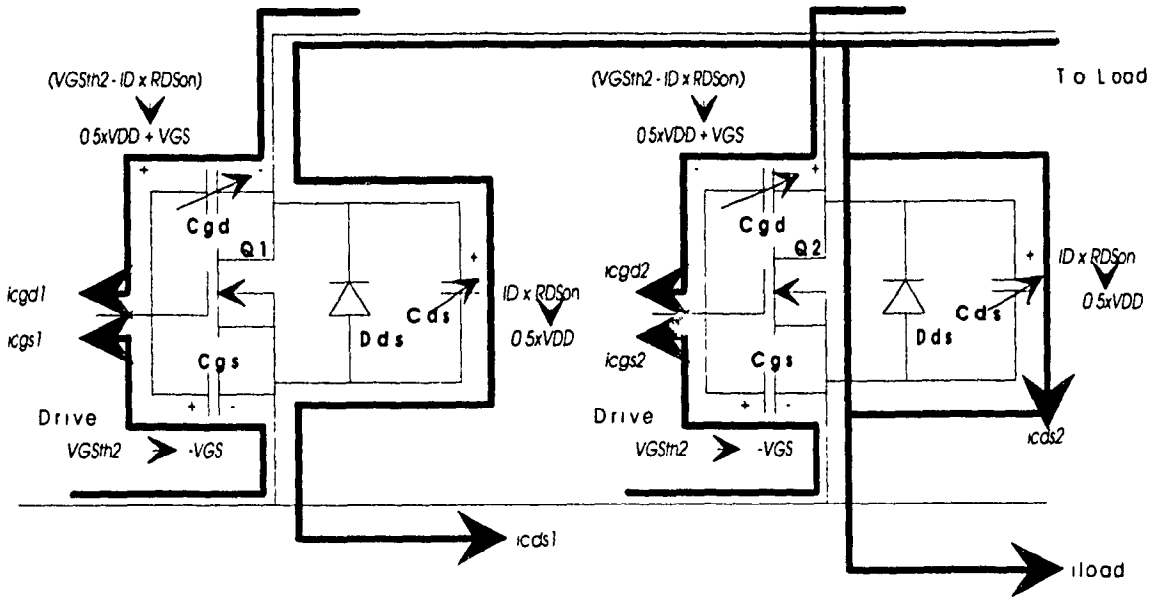


Figure 3.4.9 - HS-PWM On Condition Vgs < Vgsth2 (Q2 Turns off)

Figure 3.4.10 shows the off state of the MOSFETs. During this condition the only current flowing is the leakage drain-source current which is negligible and can be ignored. The drain-source capacitances C_{ds} are charged to *(0.5 x VDD)*, the gate-drain capacitances are charged to - *((0.5 x VDD) + VGS)*, and the gate-source capacitances are charged to - *VGS*.

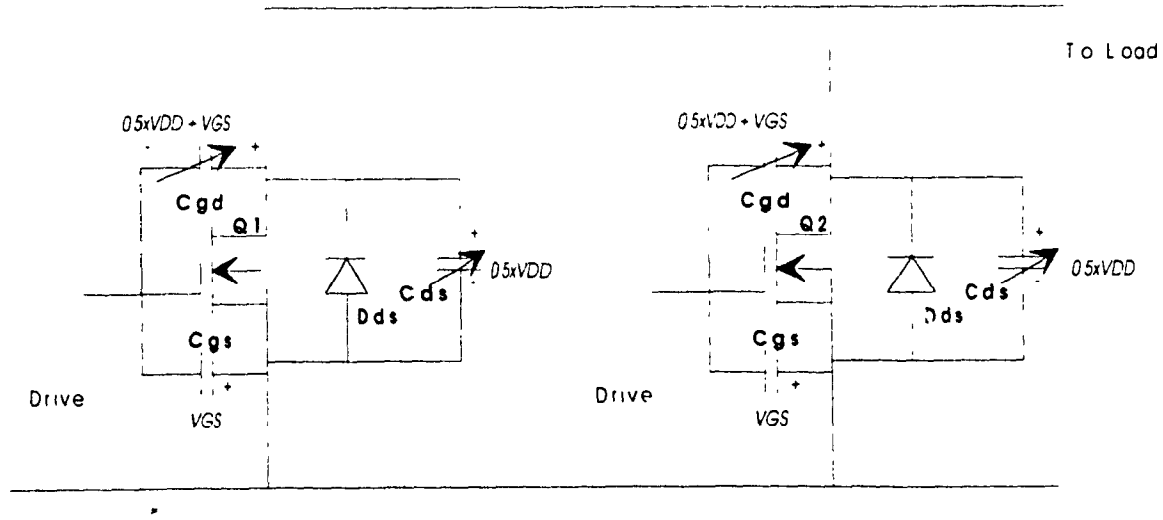


Figure 3.4.10 - HS-PWM Off Condition

3.4.4 Losses During HS-PWM Turn Off Transitions

As in the turn on transition, losses will occur when current is flowing through the gate-drain capacitances C_{gd} and the gate-source capacitances C_{gs}. More power will be required in the multiple switch case because of the increased parasitic capacitances C_{gs} and C_{gd}. Conduction losses will be lower as mentioned in section 3.4.2 when both MOSFETs are on. For the period when one MOSFET is on and the other is off, the conduction losses will be the same as in the single switch case.

3.4.5 Two Paralleled MOSFETs HS-PWM Simulated Results

The MOSFET model described in Chapter 2 was used in the full bridge HS-PWM circuit shown in Figure 3.2.1 to obtain simulated results. The MOSFET model was paralleled and switched on and off at the same time. The results presented in this section focus on the turn on and turn off conditions since charging and discharging of the parasitic components occurs during these intervals. This section will be presented in two parts. The first part will describe the ideal case where both MOSFETs in the paralleled combination will turn on and off at the same time. The second section will describe the case where the paralleled MOSFETs will turn on and off at different times due to different V_{gsth}, g_{fs}, C_{iss}, and drive impedances.

3.4.5.1 Two Paralleled MOSFETs HS-PWM Ideal Case

Figure 3.4.11 shows the case when two MOSFETs are connected in parallel and are turned on at the same time. It also shows the parasitic capacitive currents which flow through MOSFETs Q4a and Q4b when MOSFETs Q1a and Q1b are turned on. At 140.5 uS, the drive signals of MOSFETs Q1a and Q1b are applied to turn them on. At 140.55 uS, MOSFETs Q1a and Q1b turn on allowing MOSFETs Q4a and Q4b drain-source capacitances C_{ds} to charge from *(0.5 x VDD)* to *VDD*. The gate-drain capacitances C_{gd} of MOSFETs Q4a and Q4b also charge from *(0.5 x VDD-(- Vgs))* to *(VDD - (- Vgs))*. Current also flows through the gate-source capacitances C_{gs} of MOSFETs Q4a and Q4b since they carry some of the current required to charge the gate-drain capacitances C_{gd}. At 140.7 uS the drain-source capacitances C_{ds} and the gate-drain capacitances C_{gd} of MOSFETs Q4a and Q4b will be charged. Current will flow through the gate-source capacitances C_{gs} as the gate drive circuit of MOSFETs Q4a and Q4b tries to recharge these capacitance to - *Vgs*.

Figure 3.4.12 shows the parasitic capacitive currents which will flow through MOSFETs Q4a and Q4b when they are turned on. At 144.3 uS the gate-source signal is applied to MOSFETs Q4a and Q4b. Current will first start to flow through the gate-source capacitances C_{gs} of MOSFETs Q4a and Q4b as they charge from - *VGS* to the MOSFETs threshold voltage + *Vgsth*. When the gate-source threshold voltage is reached at 144.4 uS, MOSFETs Q4a and Q4b will start to turn on. Currents will start to flow through its gate-drain and drain-source capacitances, C_{gd} and C_{ds} respectively as they start to discharge. The gate-source capacitances

C_{gs} stops charging when MOSFETs Q4a and Q4b turn on because their drive current is diverted away from their gate-source capacitances C_{gs} to discharge their gate-drain capacitances C_{gd}. In fact, the negative current flowing through the gate-source capacitances C_{gs} of MOSFETs Q4a and Q4b at 144.4 uS shows that some charge is taken from them in order to charge the gate-drain capacitances C_{gd}. After MOSFETs Q4a and Q4b have turned on at 144.45 uS, no significant current will flow through their drain-source and drain-gate capacitances. Current will flow through the gate-source capacitances C_{gs} of MOSFETs Q4a and Q4b as they continues to charge to + *Vgs*.

Figure 3.4.13 shows how the load current is supplied from the paralleled combination of MOSFETs Q1a and Q1b and MOSFETs Q4a and Q4b during the turn on of MOSFETs Q1a and Q1b. At 140.5 uS, MOSFETs Q1a and Q1b are turned on when the gate-source voltage signal is applied. When MOSFETs Q1a and Q1b turn on at 140.55 uS there is a large drain current which flows internally to both MOSFETs Q1a and Q1b. This current is caused by the discharging of the drain-source and gate-drain capacitances, C_{ds} and C_{gd}, of MOSFETs Q1a and Q1b, and the charging of the drain-source and gate-drain capacitances, C_{ds} and C_{gd}, of MOSFETs Q4a and Q4b. In Figure 3.4.13 this charging and discharging current is denoted as *Ia*. After MOSFETs Q1a and Q1b parasitic capacitances have discharged and MOSFETs Q4a and Q4b parasitic capacitances have charged at 140.65 uS, MOSFETs Q1a and Q1b will share the load current *I(LSA)*.

When MOSFETs Q4a and Q4b are turned on at 144.3 uS they will also be required to dis harge their drain-source and gate-drain capacitances, C_{ds} and C_{gd}, as well as charge the drain-source and gate-drain capacitances of MOSFETs Q1a and Q1b as shown in Figure 3.4.14. This charging and discharging current is denoted as *Ia*. At 144.4 uS the drain-source and gate-drain capacitances of MOSFETs Q4a and Q4b will be discharged and the drain-source and gate-drain capacitances of MOSFETs Q1a and Q1b will be charged. At this time the load current *I(LSA)* will be shared by MOSFETs Q4a and Q4b.

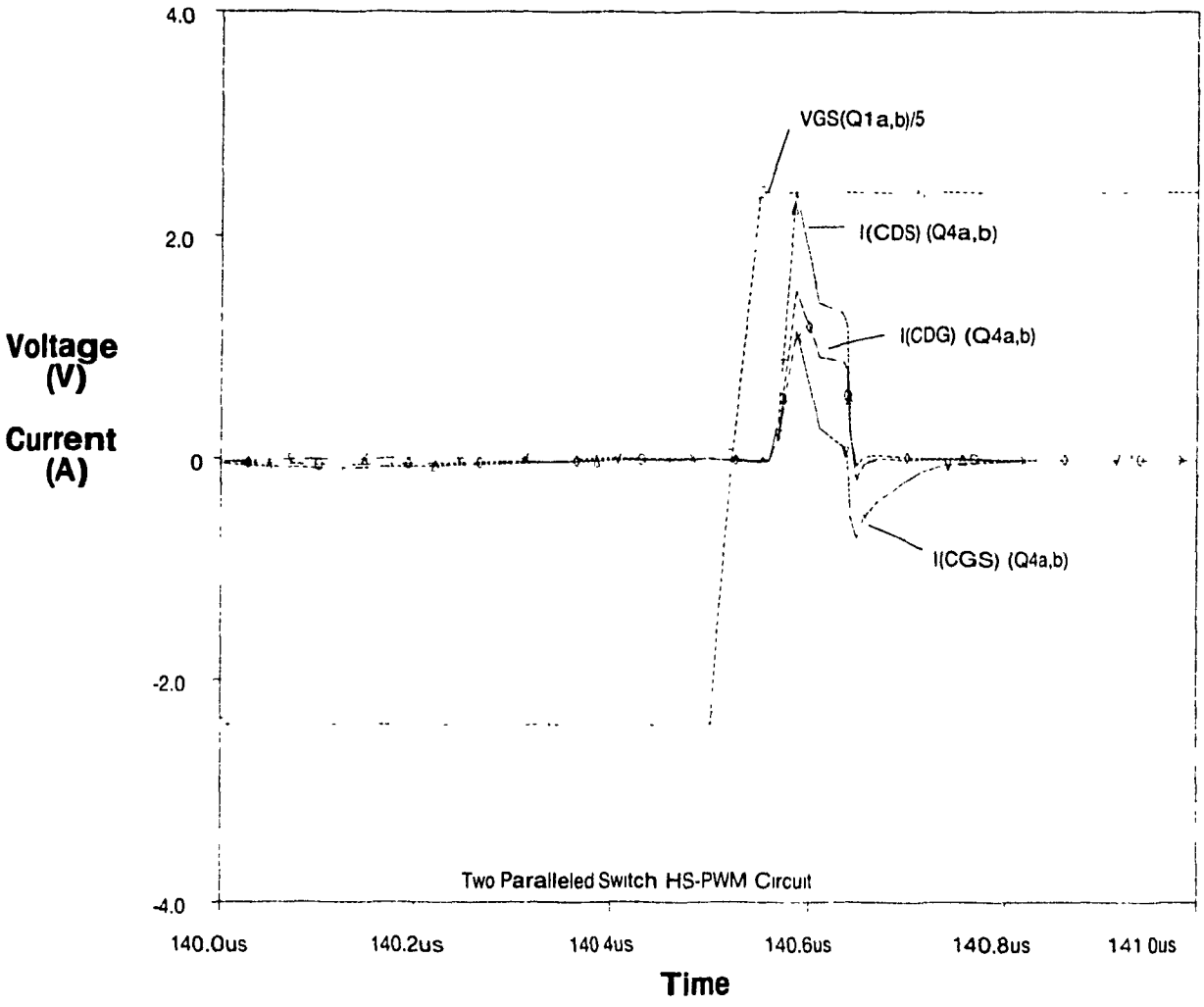


Figure 3.4.11 - HS-PWM MOSFETs Q4a, Q4b Turn Off, MOSFETs Q1a, Q1b Turn On (No Delay) Parasitic Capacitive Currents

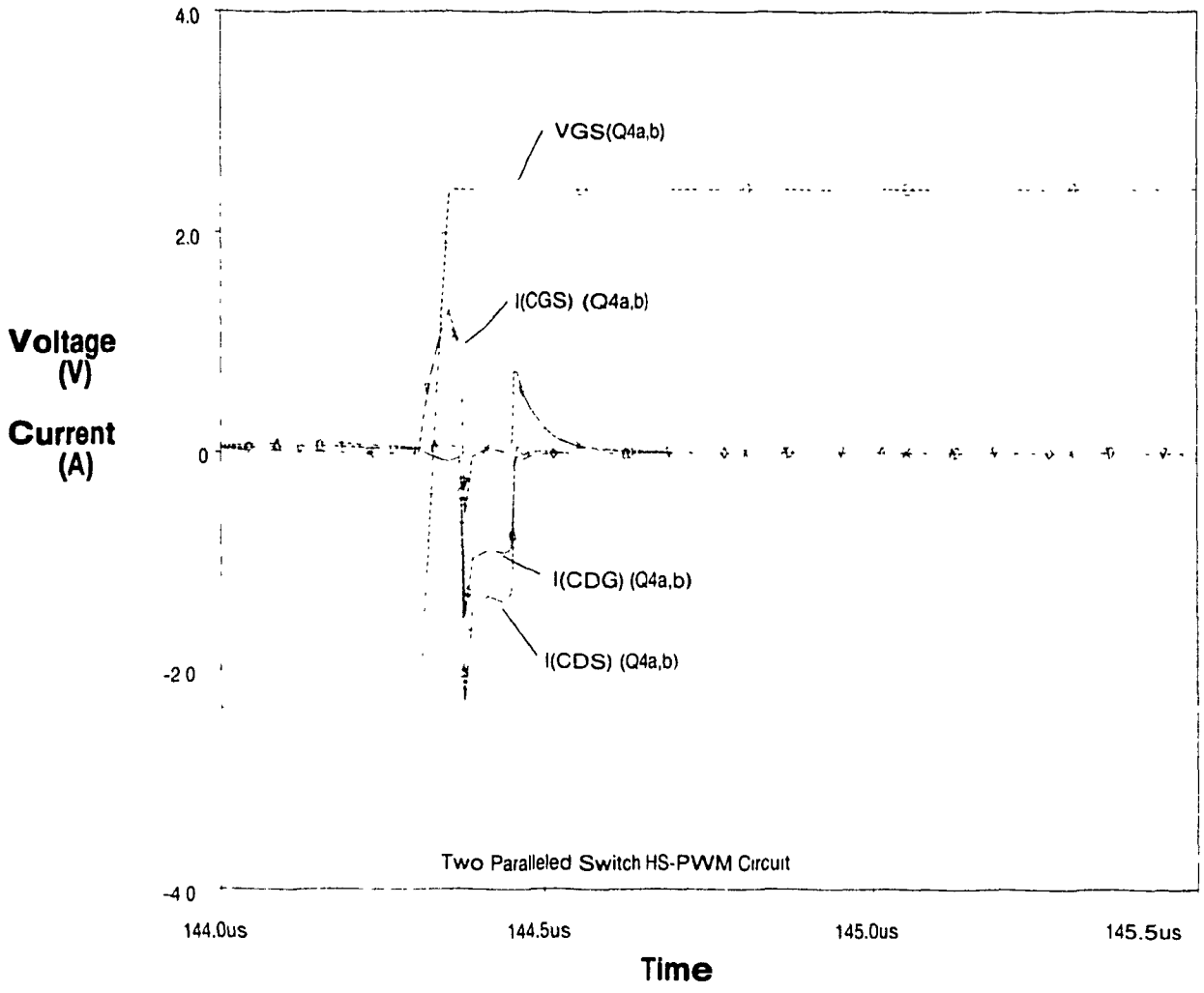


Figure 3.4.12 - HS-PWM MOSFETs Q4a, Q4b Turn On (No Delay) Parasitic Capacitive Currents

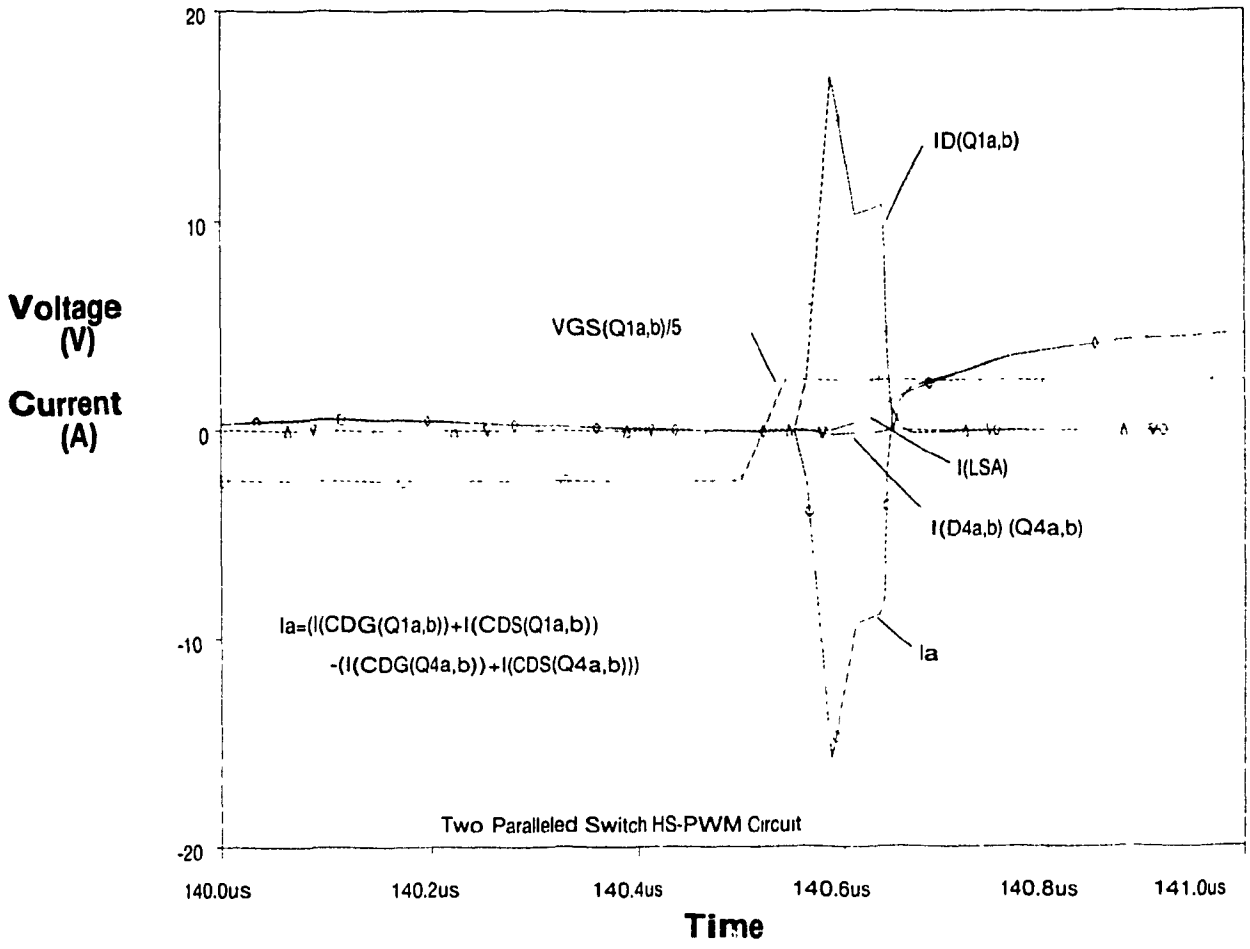


Figure 3.4.13 - HS-PWM MOSFETs Q4a, Q4b Turn Off, MOSFETs Q1a, Q1b Turn On (No Delay) Capacitive, Drain and Body Diode Currents

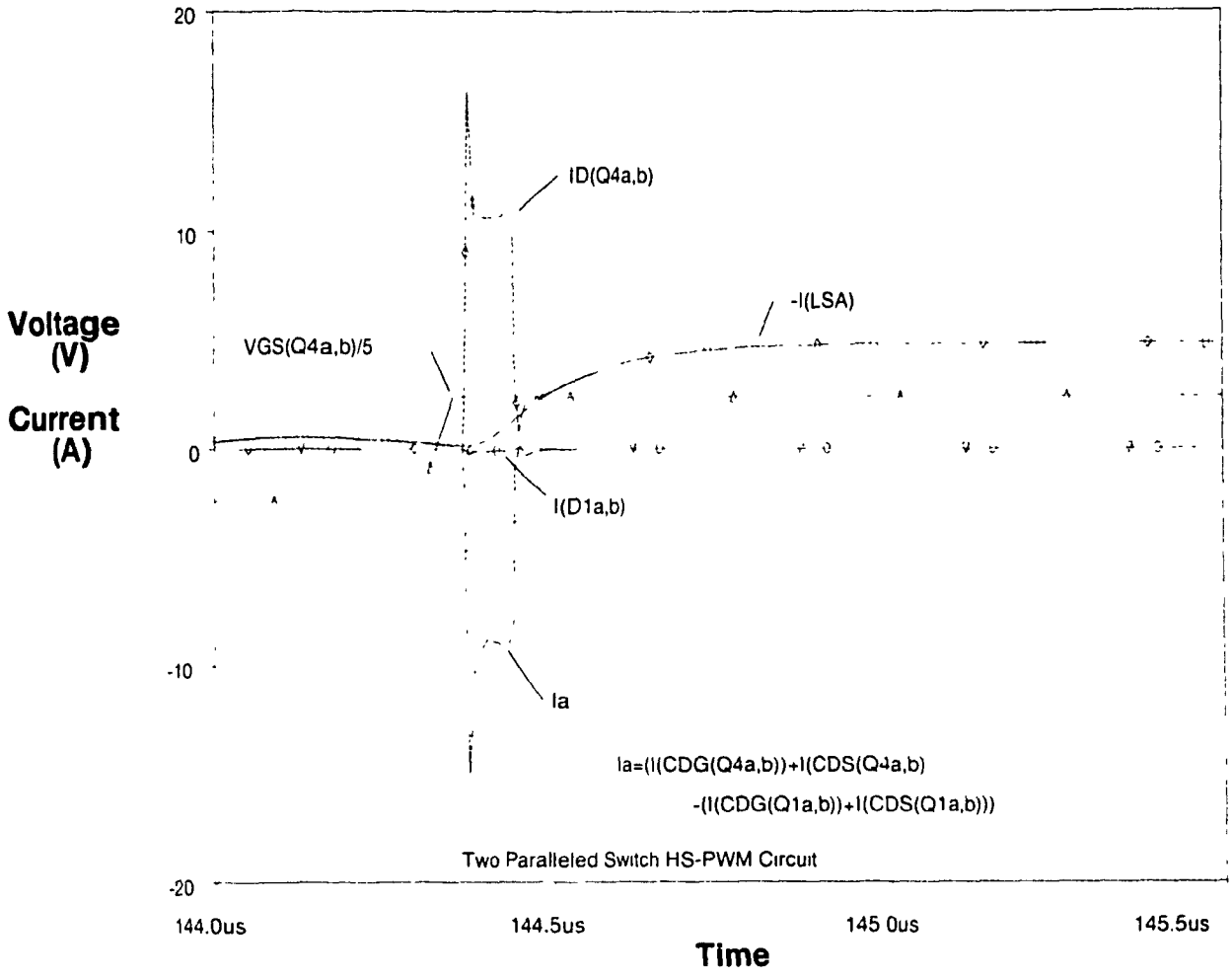


Figure 3.4.14 · HS-PWM MOSFETs Q4a, Q4b Turn On (No Delay) Capacitive, Drain and Body Diode Currents

3.4.5.2 Two Paralleled MOSFETs HS-PWM Non-Ideal Case

Figure 3.4.15 shows the condition when MOSFET Q1a turns on before MOSFET Q1b and MOSFET Q4a turns on before MOSFET Q4b. The capacitive parasitic currents through MOSFETs Q4a and Q4b will be the same as was the case when MOSFETs Q1a and Q1b turned on at the same time. This occurs because the charging currents for the drain-source and gate-drain capacitances, C_{ds} and C_{gd} will start to flow as soon as one MOSFET in the Q1 combination turns on.

Figure 3.4.16 shows the condition when MOSFET Q4a turns on before MOSFET Q4b. The capacitive parasitic currents flowing through MOSFETs Q4a and Q4b will be the same as was observed when both these MOSFETs turn on at the same time. The only difference observed between these two cases was the current flowing through the gate-source capacitance C_{gs} of MOSFET Q4b. At 144.6 uS, the current flows through the gate-source capacitance C_{gs} of MOSFET Q4b and is similar to the current which starts to flow through the gate-source capacitance C_{gs} of MOSFET Q4a. The only difference between these currents is that the gate-source parasitic capacitance current of MOSFET Q4b does not reverse direction when MOSFET Q4b is turned on at 144.5 uS because its gate-drain capacitance has already been discharged by MOSFET Q4a.

Figure 3.4.17 shows how current flows through MOSFETs Q1a and Q1b when they are turned on at 140.5 uS and 140.75 uS respectively. At 140.55 uS, MOSFET Q1a will turn on first and will carry current Ia. This current is the sum of the load current *I(LSA)*, the charging

parasitic capacitive current of MOSFETs Q4a and Q4b and the discharging parasitic capacitive current of MOSFETs Q1a and Q1b. Also, MOSFET Q1a will carry the full load current *I(LSA)* until MOSFET Q1b turns on at 140.85 uS. When both MOSFETs Q1a and Q1b are turned on, they will share the load current *I(LSA)*.

Figure 3.4.18 shows how current flows through MOSFETs Q4a and Q4b when they are turned on at 144.30 uS and 144.55 uS respectively. At 144.30 uS, MOSFET Q4a will turn on first and will carry current *Ia*. This current is the sum of the load current *I(LSA)*, the charging parasitic capacitive current of MOSFETs Q1a and Q1b and the discharging parasitic capacitive current of MOSFETs Q4a and Q4b. Also, MOSFET Q4a will carry the full load current *I(LSA)* until MOSFET Q4b turns on at 140.85 uS When both MOSFETs Q4a and Q4b are turned on, they will share the load current *I(LSA)*.

Figure 3.4.19 shows the turn on of MOSFETs Q1a and Q1b. In this case MOSFET Q1a turns on 250 nS before MOSFET Q1b. MOSFET Q1a will carry the charging and discharging currents of all the MOSFETs in the leg, that is MOSFETs Q1a, Q1b, Q4a and Q4b. MOSFET Q1a will carry the load current until MOSFET Q1b turns on at 140.85 uS.

Figure 3.4.20 shows the turn on of MOSFETs Q4a and Q4b. In this case MOSFET Q4a turns on 250 nS before MOSFET Q4b. MOSFET Q4a will carry the charging and discharging currents of all the MOSFETs in the leg, that is MOSFETs Q4a, Q4b, Q1a and Q1b. MOSFET Q4a will carry the load current until MOSFET Q4b turns on at 144.60 uS.

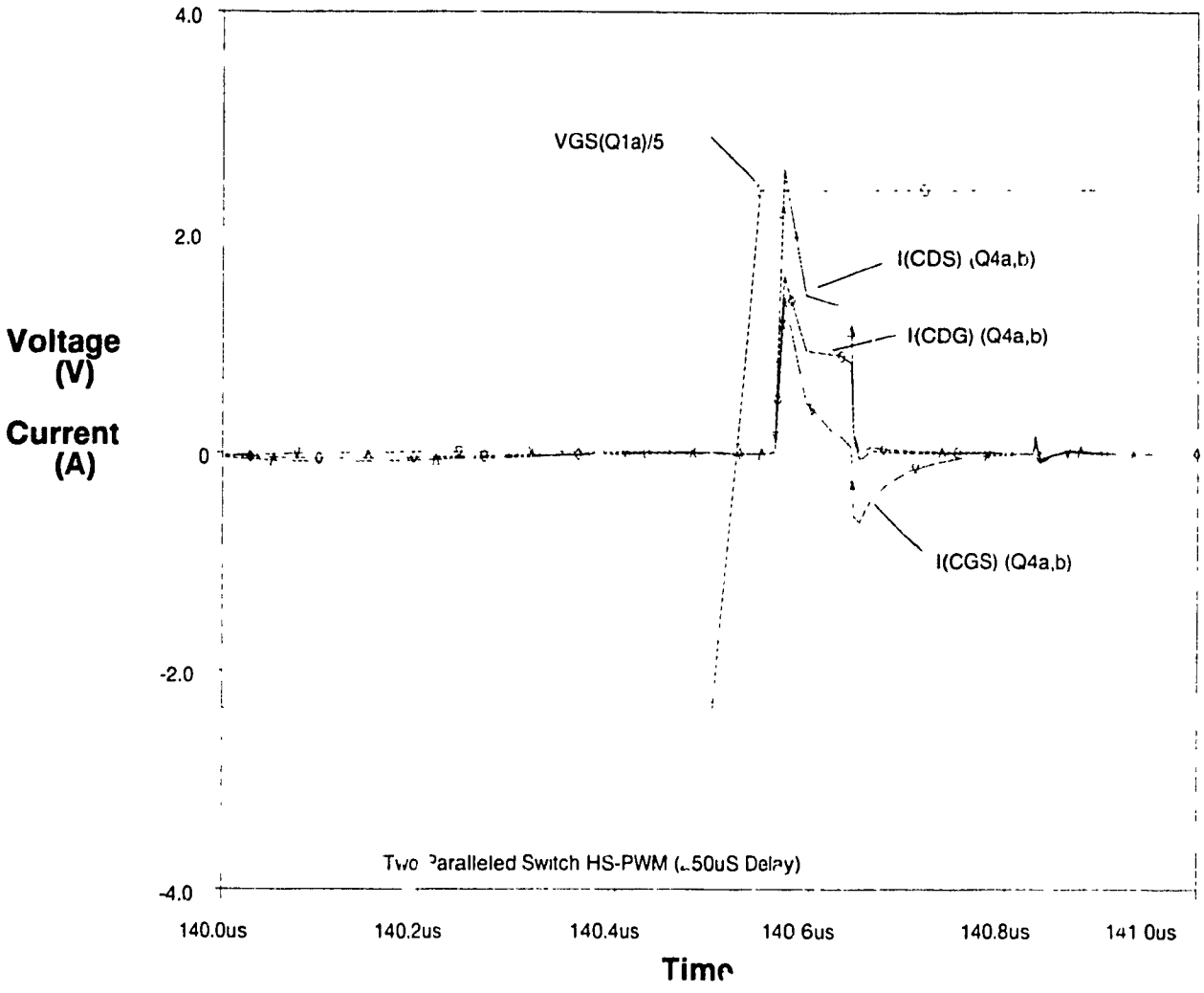


Figure 3.4.15 - HS-PWM MOSFETs Q4a, Q4b Turn Off, MOSFETs Q1a, Q1b Turn On (250 nS Delay) Parasitic Capacitive Currents

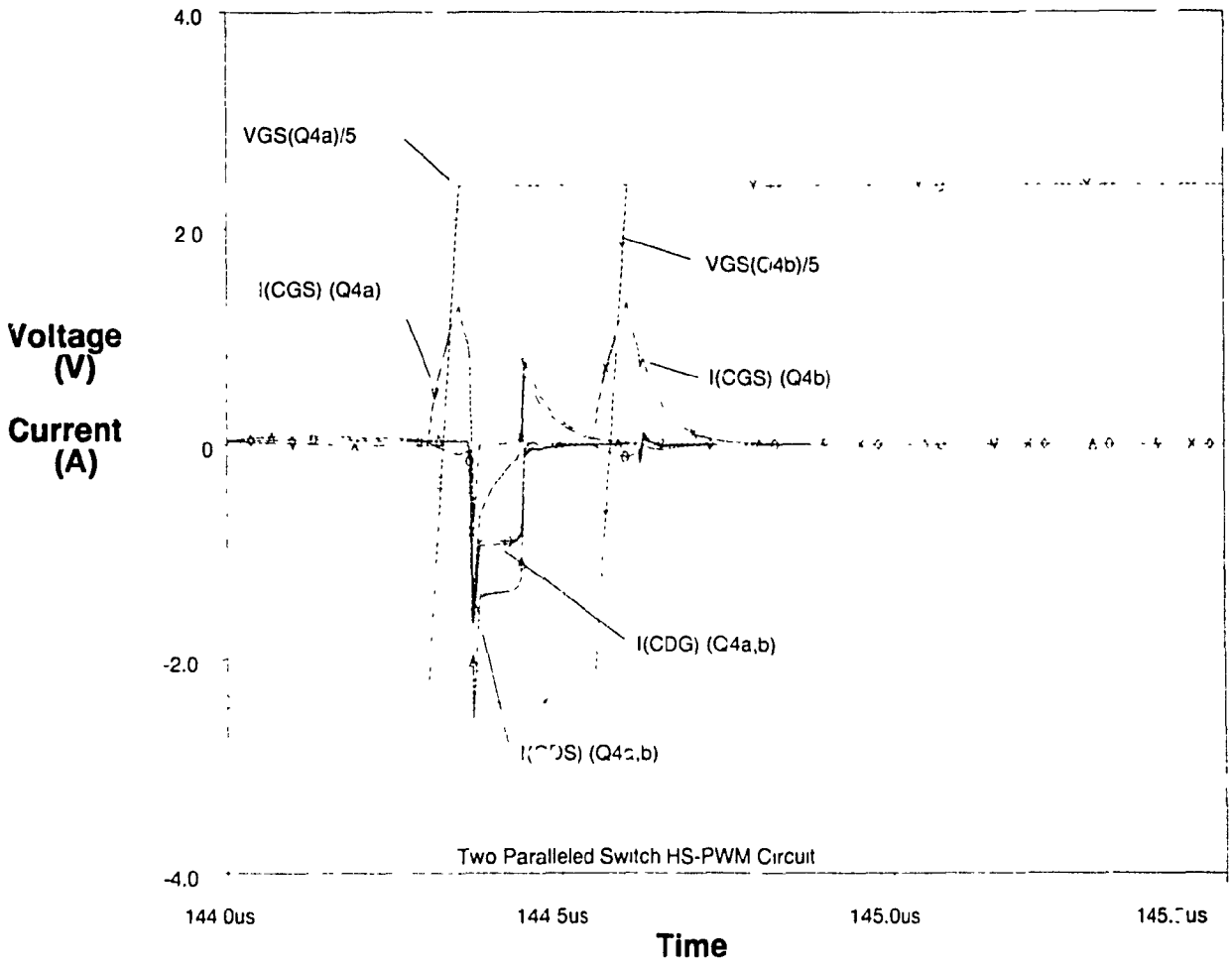


Figure 3.4.16 - HS-PWM MOSFETs Q4a, Q4b Turn On (250 nS Delay) Parasitic Capacitive Currents

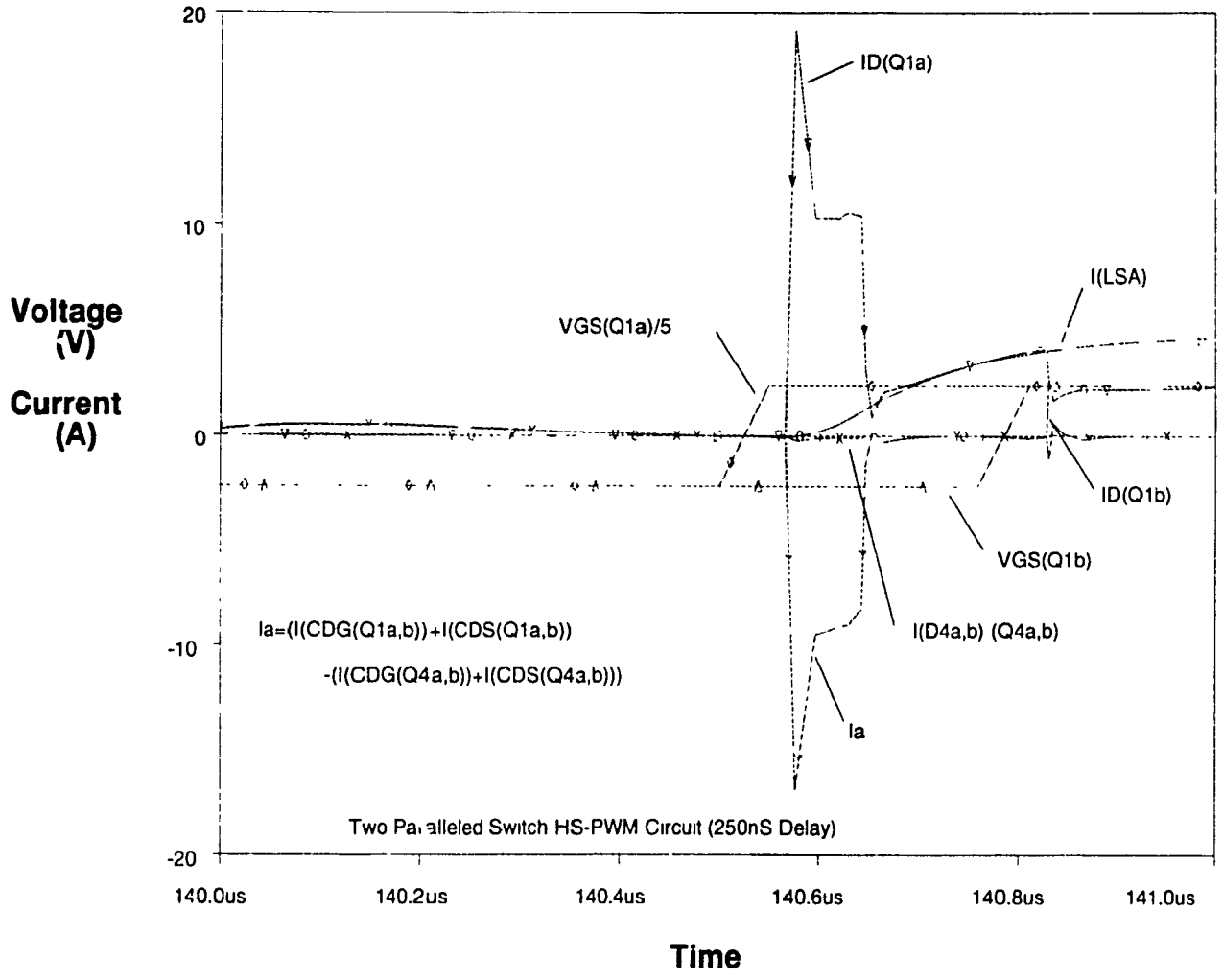


Figure 3.4.17 - HS-PWM MOSFETs Q4a, Q4b Turn Off, MOSFETs Q1a, Q1b Turn On (250 nS Delay) Capacitive, Drain and Body Diode Currents

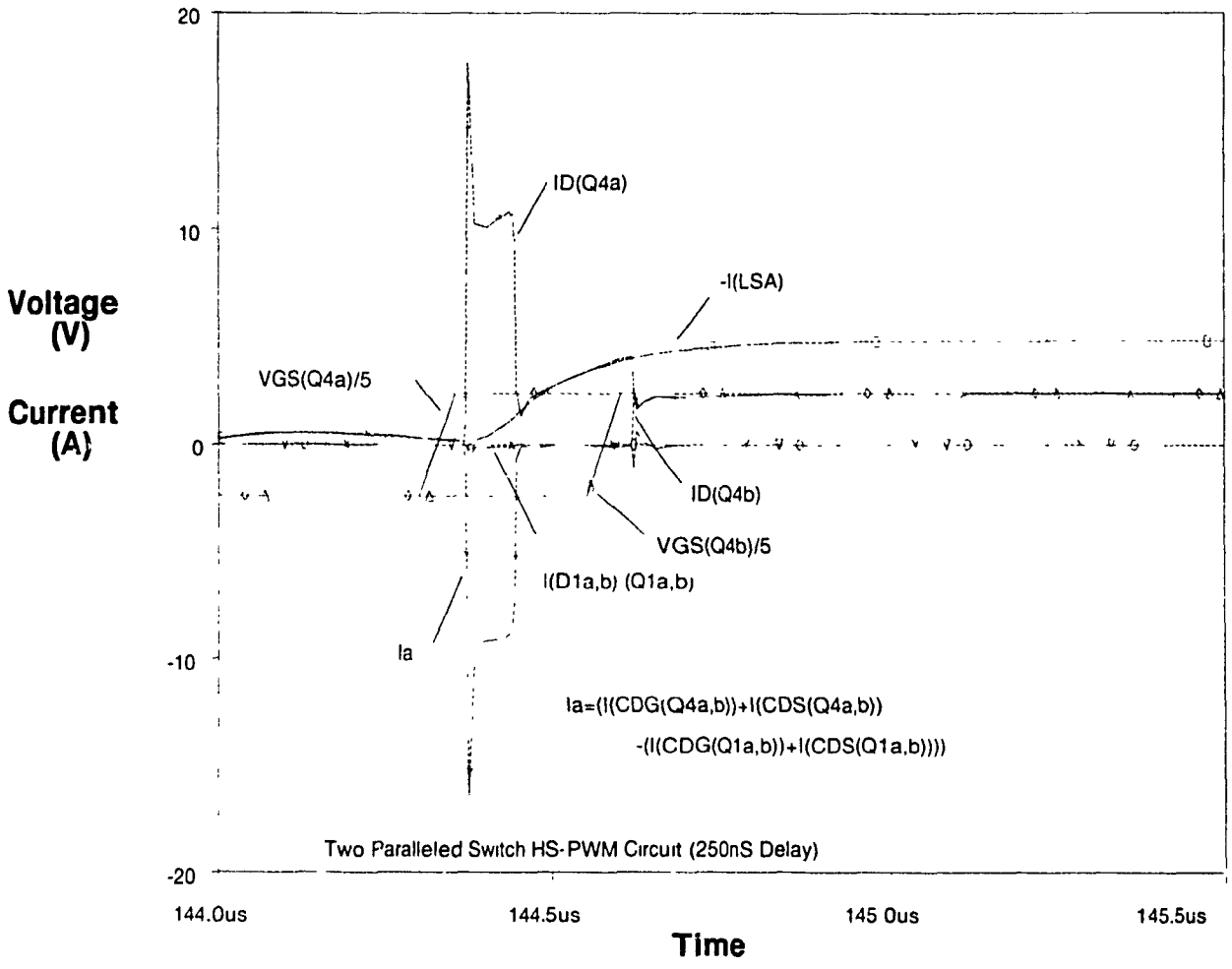


Figure 3.4.18 · HS-PWM MOSFETs Q4a, Q4b Turn On (250 nS Delay) Capacitive, Drain and Body Diode Currents

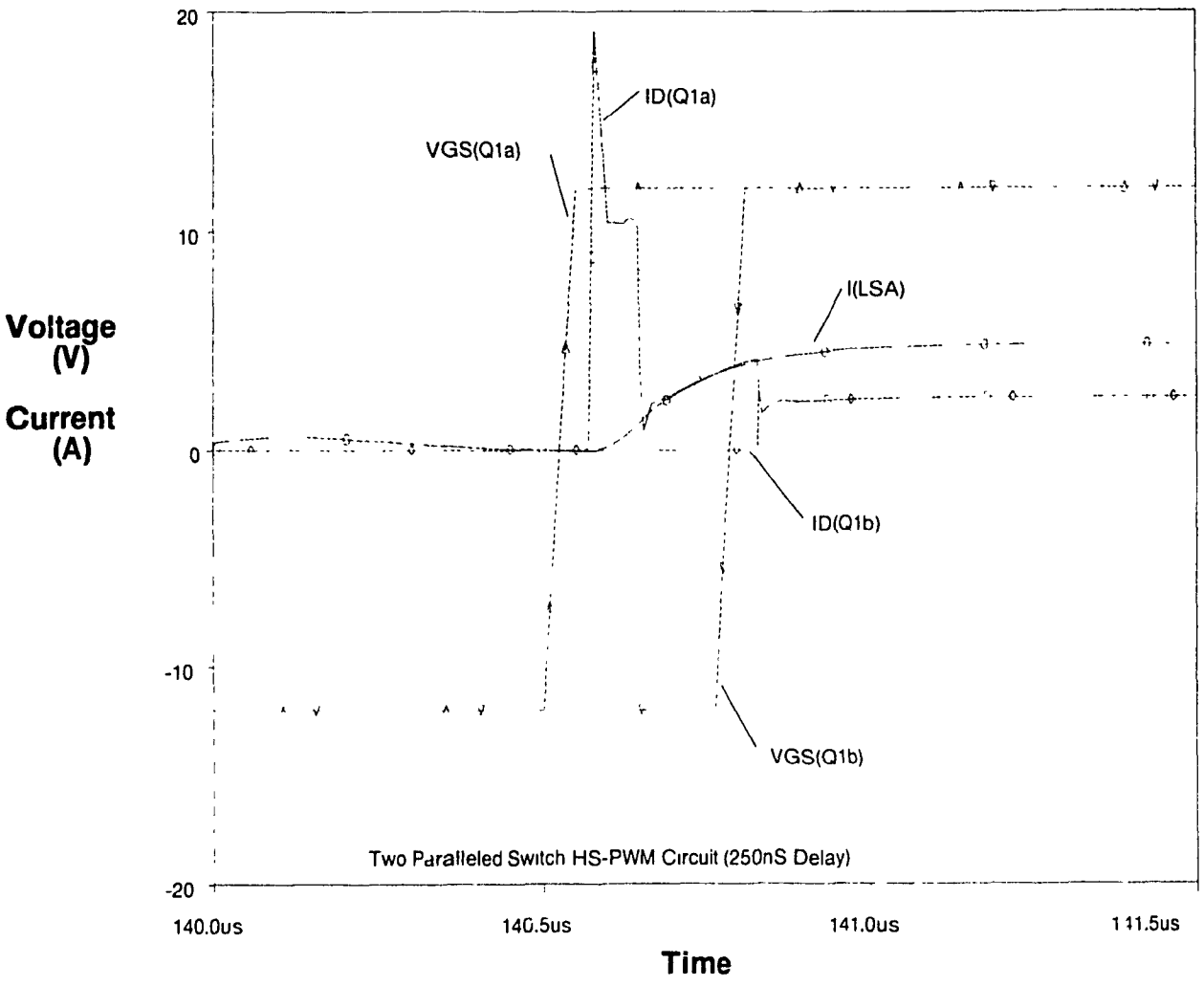


Figure 3.4.1) - HS-PWM MOSFETs Q1a, Q1b Turn On (250 nS Delay) Drain and Body Diode Currents

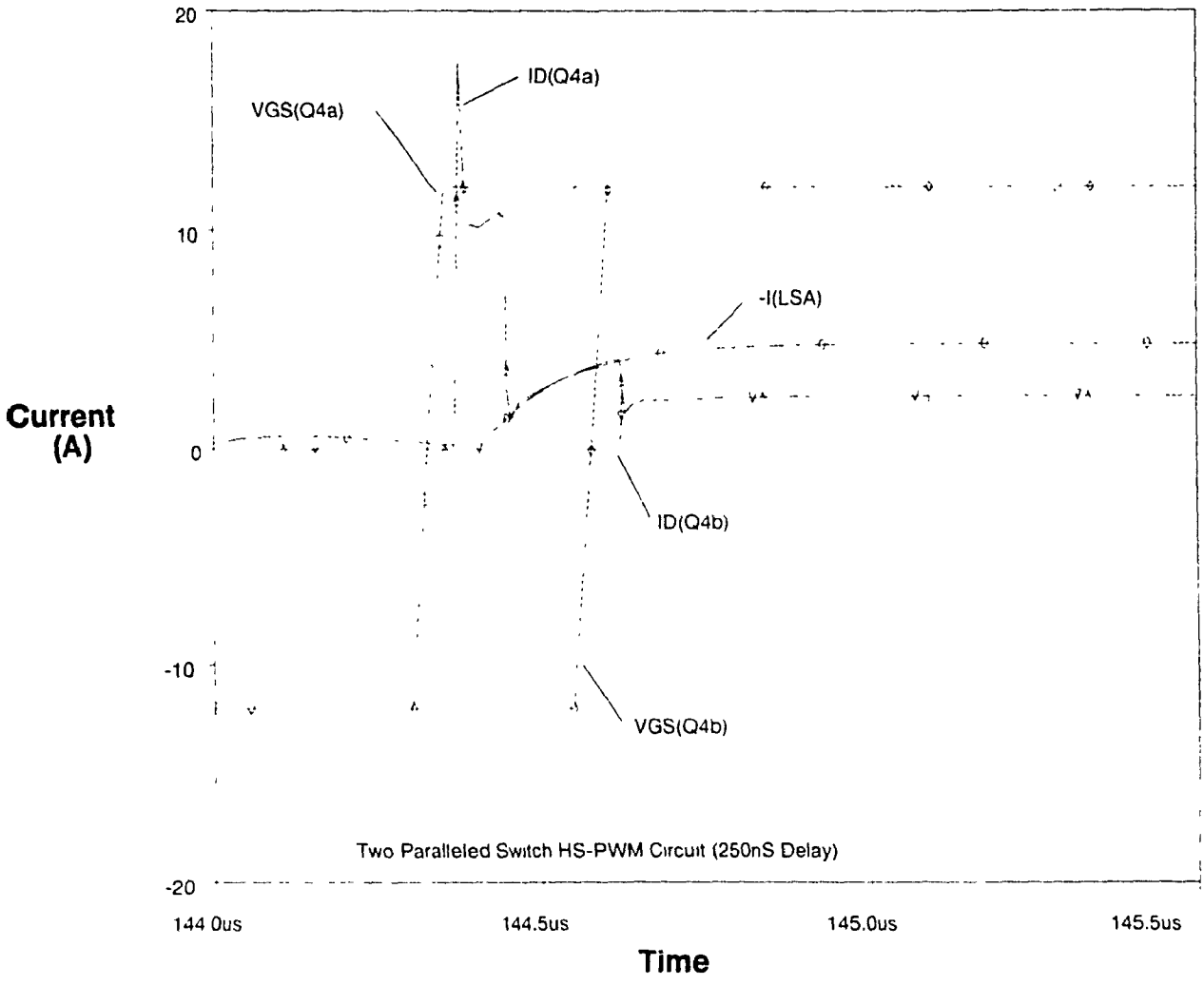


Figure 3.4.20 - HS-PWM MOSFETs Q4a, Q4b Turn On (250 nS Delay) Drain and Body Diode Currents

3.4.6 Two Paralleled MOSFETs HS-PWM Experimental Results

Experimental results were obtained when the HS-PWM circuit shown in Figure 3.2.1 was connected with two MOSFETs connected in parallel. The experimental results obtained along with the simulated results are shown in Table 3.4.1. Simulated results were obtained by using the PSPICE program to simulate the circuit using the MOSFET model described in Chapter 2. The PROBE sub-program of PSPICE was used to graph the waveforms and mathematically generate loss plots which were then read from the graph by the cursor function. The experimental results were obtained by measuring the input power to the bridge and subtracting the output power of the diode filter. The losses of the transformer, diodes, and filter inductor were estimated and subtracted from the final loss result as described in section 3.3.6. Table 3.4.1 shows a comparison of the experimental and simulated results.

Table 3.4.1 Comparison of Experimental, and Simulated Losses for Paralleled HS-PWM MOSFETs

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
1	23.92 W	65.80 W	23.92 W
2	38.40 W	79.64 W	37.52 W

A time delay was simulated to see the effects on the losses when two MOSFETs were used in parallel. This delay was implemented experimentally by varying the gate drive resistor of one MOSFET of the parallel combination while observing its gate source voltage. The results are given in Table 3.4.2 for delay times of 250 nS and 500 nS. and compared with the no (minimal) delay case mentioned above.

Table 3.4.2 Comparison of Experimental, and Simulated Losses for Paralleled HS-PWM MOSFETs with Switching Delays

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
0 nS	38.40 W	79.64 W	37.52 W
250 nS	39 55 W	80.45 W	38.72 W
500 nS	39.78 W	110.75 W	39.12 W

3.4.7 Summary of Losses for Two Paralleled MOSFETs HS-PWM Topology

From the results obtained is this section it is seen that paralleling MOSFETs will decrease the conduction losses because of the decrease of the effective R_{dson}. Switching losses however will increase because the parasitic capacitances C_{gs} and C_{gd} will also increase requiring more gate drive power to turn the devices on and off. The increase in the drain-source capacitances C_{ds} will require the MOSFET

which turns on first to dissipate more energy as it discharges this capacitance for both devices. The MOSFET which turns on last will also generate the same turn on losses due to the voltage and current as in the single MOSFET case. The MOSFET which turn off last will also experience the same turn off switching losses as a single switch. Also, as mentioned above, since it is unlikely that both MOSFETs will turn on and off at the same time, there will exist a period of time when only one MOSFET is conducting. During this period it will seem as if only one MOSFET is used and the conduction losses will be the same as in the single MOSFET case.

As switching frequencies are increased, the drive power to charge and discharge the parasitic capacitances will also increase. Also, the time period when only one MOSFET conducts will become more significant with respect to the on time of the MOSFET. This means that savings obtained by paralleling MOSFETs will decrease as switching frequency increases. In fact, the decrease in conduction losses may be offset by the increase in switching power required for a given frequency.

From the experimental result it is seen that as more MOSFETs are added in parallel, losses increase. The losses do not double when two MOSFETs are used in parallel because the conduction losses of the combination decreases and the switching losses caused by the overlap of drain-source voltage and current remains the same for the combination

When the MOSFETs within the paralleled combination were delayed the losses increased due to fact that one MOSFET had more conduction

losses. For the delay time of 500 nS, the losses were less than those obtained for a delay time of 250 nS and was due to some instability during switching.

3.5 Three Paralleled MOSFETs HS-PWM Simulated and Experimental Results

The case where three MOSFETs are paralleled for a single switching element was studied and found to be similar to the two paralleled MOSFET case. In order to prevent a repeat of section 3.4, only a summary of the differences observed between the two cases will be presented in this section.

When three MOSFETs were paralleled, the parasitic capacitances C_{ds}, C_{gd} and C_{gs} were effectively placed in parallel and resulted in a switching element which had three times the parasitic capacitances of the single MOSFET case. This resulted in more drive power required to switch the MOSFETs on and off. Also, when three MOSFETs are paralleled the effective R_{dson} will be one third that of the single MOSFET case.

As in the two paralleled MOSFET case, the MOSFET which turns on first will carry the full load current. This MOSFET will also be required to discharge the other MOSFETs drain-source capacitances C_{ds}, and gate-drain capacitances C_{gd}. The load current will be shared when the other MOSFETs turn on in the steady state condition. Also, the MOSFET which turns off last will conduct the full load current. Care

must be taken to ensure that the MOSFETs in the configuration can handle the full load current and drain-source capacitance discharge current for the brief time when only one device is conducting. The differences in conduction times of the MOSFETs will increase the effective R_{dson} to a value greater than one third the value observed in the single MOSFET case. In order to make the conduction times similar it is necessary to match the MOSFETs input capacitance C_{iss}, gate-source threshold voltage V_{gsth}, and transconductance g_{fs}.

3.5.1 Three Paralleled MOSFETs HS-PWM Simulated Results

The MOSFET model described in Chapter 2 was used in the full bridge HS-PWM circuit shown in Figure 3.2.1 to obtain simulated results. The MOSFET model was paralleled so that a switching element consisted of three MOSFETs. These MOSFETs where switched on and off at the same time. The results presented in this section focus on the turn on and turn off conditions since charging and discharging of the parasitic components occurs during these intervals.

Figure 3.5.1 shows the case when three MOSFETs are connected in parallel and are turned on at the same time. It also shows the parasitic capacitive currents which flow through MOSFETs Q4a, Q4b and Q4c when MOSFETs Q1a, Q1b, and Q1c are turned on. At 140.5 uS, the drive signals of MOSFETs Q1a, Q1b, and Q1c are applied to turn them on. At 140.55 uS, MOSFETs Q1a, Q1b, and Q1c turn on allowing MOSFETs Q4a, Q4b and Q4c drain-source capacitances C_{ds} to charge from *(0.5 * VDD)* to

VDD. The gate-drain capacitances C_{gd} of MOSFETs Q4a, Q4b, and Q4c also charge from *(0.5 x VDD-(-Vgs))* to *(VDD - (-Vgs))*. Current also flows through the gate-source capacitances C_{gs} of MOSFETs Q4a, Q4b, and Q4c since they carry some of the current used to charge their gate-drain capacitances C_{gd}. At 140.7 uS the drain-source capacitances C_{ds} and the gate-drain capacitances C_{gd} of MOSFETs Q4a, Q4b, and Q4c will be charged. Current will flow through the gate-source capacitances C_{gs} as the gate drive circuits of MOSFETs Q4a, Q4b and Q4c try to recharge these capacitances to - *Vgs*.

Figure 3.5.2 shows the case when three MOSFETs are connected in parallel and are turned on at the same time. It also shows the parasitic capacitive currents which will flow through MOSFETs Q4a, Q4b, and Q4c when they are turned on. At 144.3 uS the gate-source signal is applied to MOSFETs Q4a, Q4b and Q4c. Current will first start to flow through the gate-source capacitances C_{gs} of MOSFETs Q4a, Q4b and Q4c as they charge from - *VGS* to their threshold voltage + *Vgsth*. When the gate-source threshold voltage is reached at 144.4 uS, MOSFETs Q4a, Q4b and Q4c will start to turn on. Currents will start to flow through the gate-drain and drain-source capacitances, C_{gd} and C_{ds} respectively as they start to discharge. The gate-source capacitances C_{gs} stop charging when the MOSFETs Q4a, Q4b and Q4c turn on because the drive current is diverted away from their gate-source capacitances C_{gs} to discharge their gate-drain capacitances C_{gd}. In fact, the negative current flowing through the gate-source capacitances C_{gs} at 144.4 uS shows that some charge is taken from them in order to charge the gate-drain capacitances C_{gd}. After MOSFETs Q4a, Q4b and Q4c have turned on at 144.45 uS, no

significant current will flow through the drain-source and drain-gate capacitances. Current will flow through the gate-source capacitances C_{gs} as it continues to charge to + *Vgs*.

Figure 3.5.3 shows how the load current is supplied from MOSFETs Q1a, Q1b and Q1c and MOSFETs Q4a, Q4b and Q4c during the turn on of MOSFETs Q1a, Q1b, and Q1c. At 140.5 uS, MOSFETs Q1a, Q1b and Q1c is turned on when the gate-source voltage signal is applied. When MOSFETs Q1a, Q1b and Q1c turn on at 140.55 uS there is a large drain current which flows internally to MOSFETs Q1a, Q1b and Q1c. This current is caused by the discharging of the drain-source and gate-drain capacitances, C_{ds} and C_{gd} of MOSFETs Q1a, Q1b and Q1c, and the charging of the drain-source and gate-drain capacitances, C_{ds} and C_{gd}, of MOSFETs Q4a, Q4b, and Q4c. In Figure 3.5.3 this charging and discharging current is denoted as *Ia*. After MOSFETs Q1a, Q1b and Q1c parasitic capacitances have discharged and MOSFETs Q4a, Q4b and Q4c parasitic capacitances have charged at 140.65 uS, MOSFETs Q1a, Q1b and Q1c will carry the full load current *I(LSA)*.

When MOSFETs Q4a, Q4b and Q4c are turned on at 144.3 uS they will also be required to discharge their drain-source and gate-drain capacitances, C_{ds} and C_{gd}, as well as charge the drain-source and gate-drain capacitances of MOSFETs Q1a, Q1b and Q1c as shown in Figure 3.5.4. This charging and discharging current is denoted as *Ia*. At 144.4 uS the drain-source and gate-drain capacitances of MOSFETs Q4a, Q4b and Q4c will be discharged and the drain-source and gate-drain capacitances of

MOSFETs Q1a, Q1b and Q1c will be charged. At this time the full load current *I(LSA)* will be carried by MOSFETs Q4a, Q4b and Q4c.

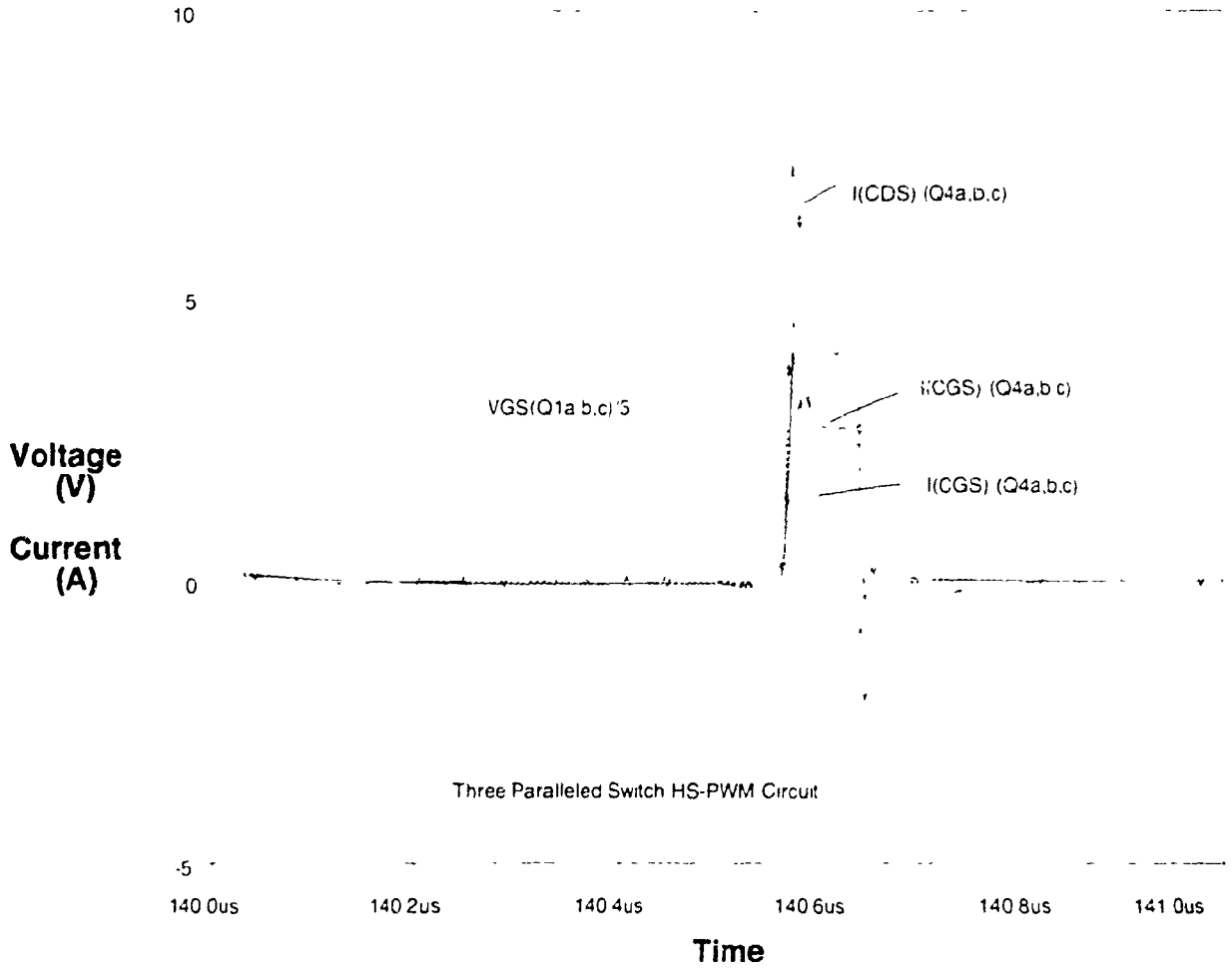


Figure 3.5.1 - HS-PWM MOSFETs Q4a, Q4b, Q4c Turn Off, MOSFETs Q1a, Q1b,Q1c Turn On Parasitic Capacitive Currents

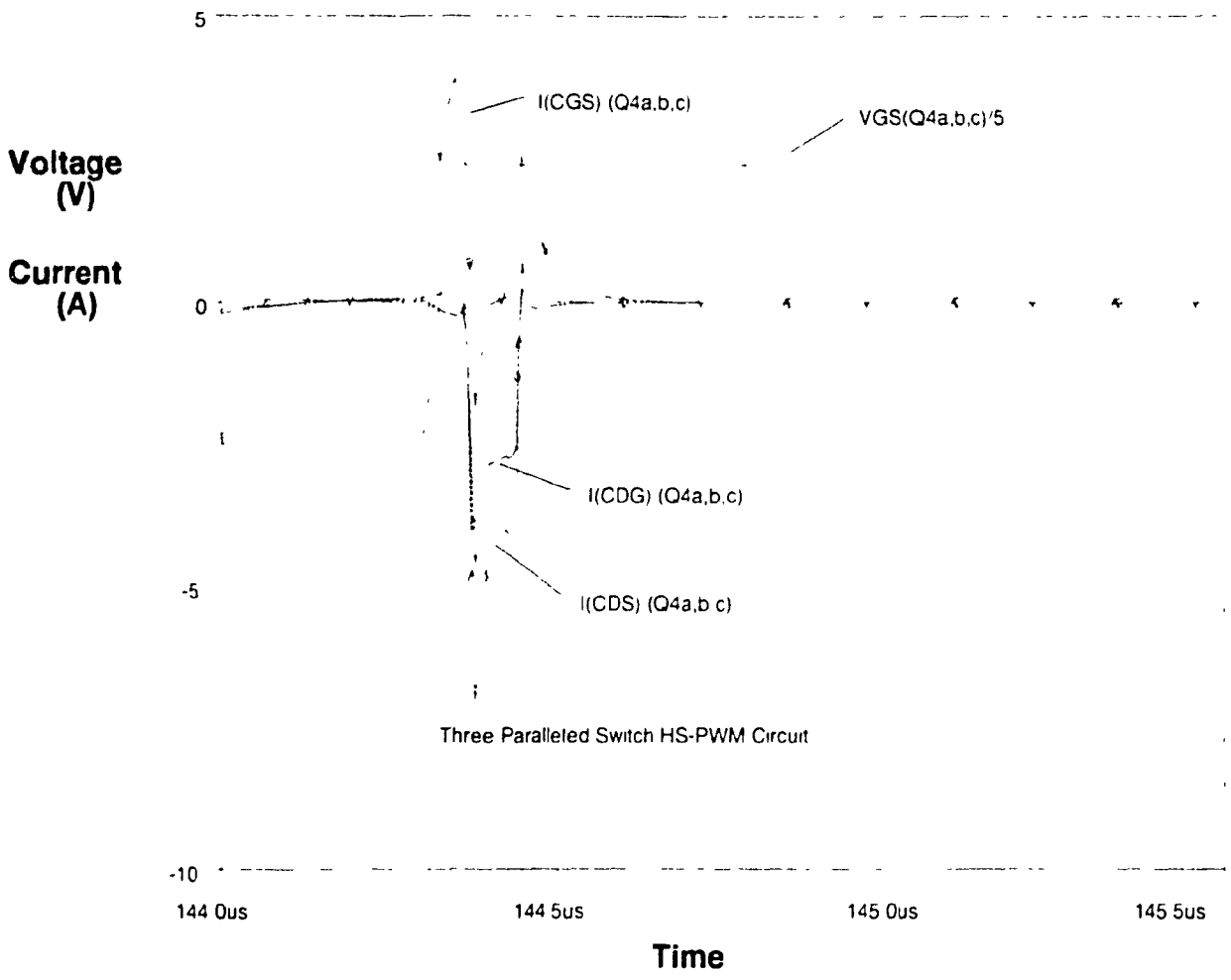


Figure 3.5.2 - HS-PWM MOSFETs Q4a, Q4b, Q4c Turn On Parasitic Capacitive Currents

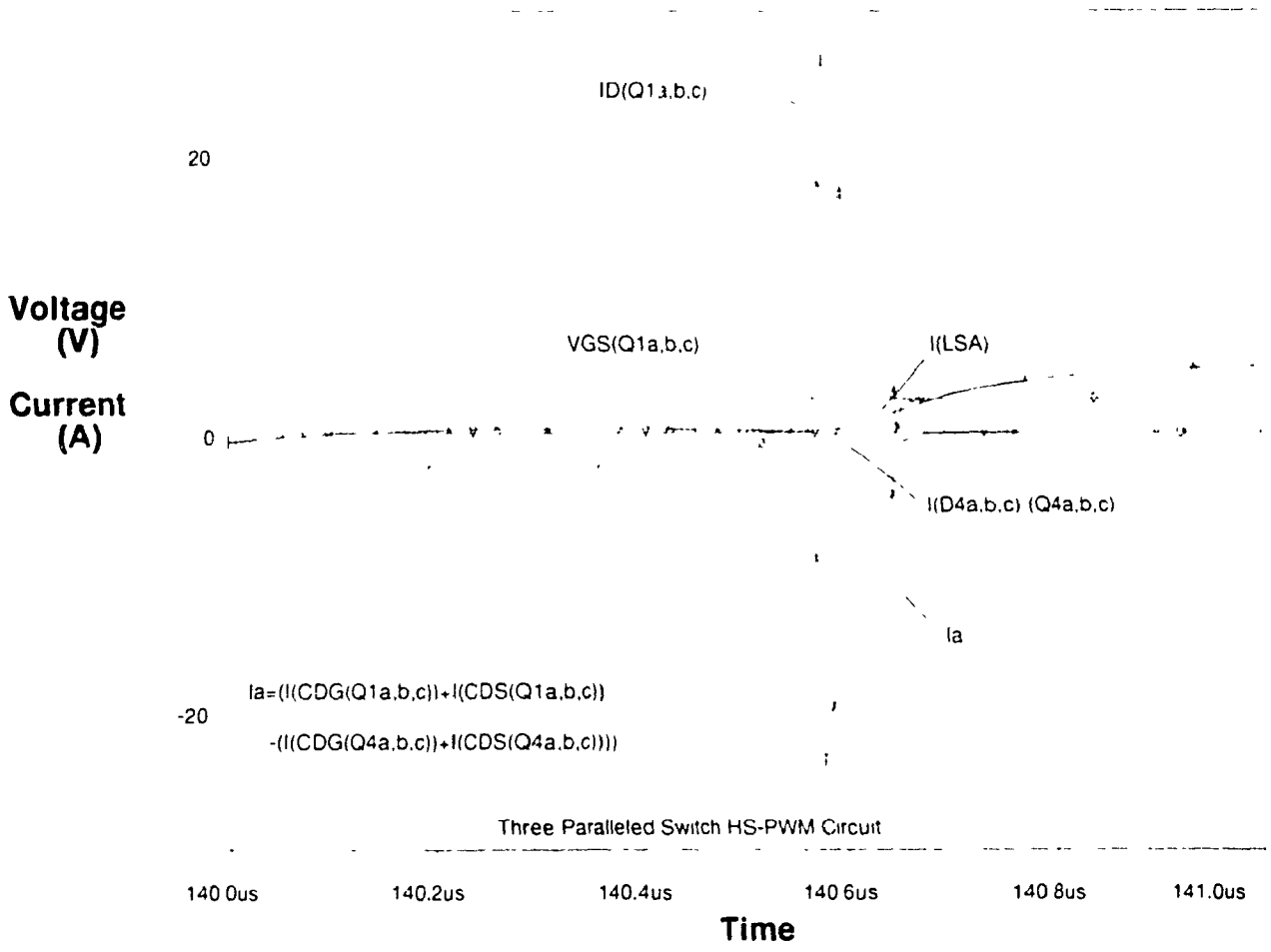


Figure 3.5.3 - HS-PWM MOSFETs Q1a, Q1b, Q1c Turn On Capacitive, Drain and Body Diode Currents

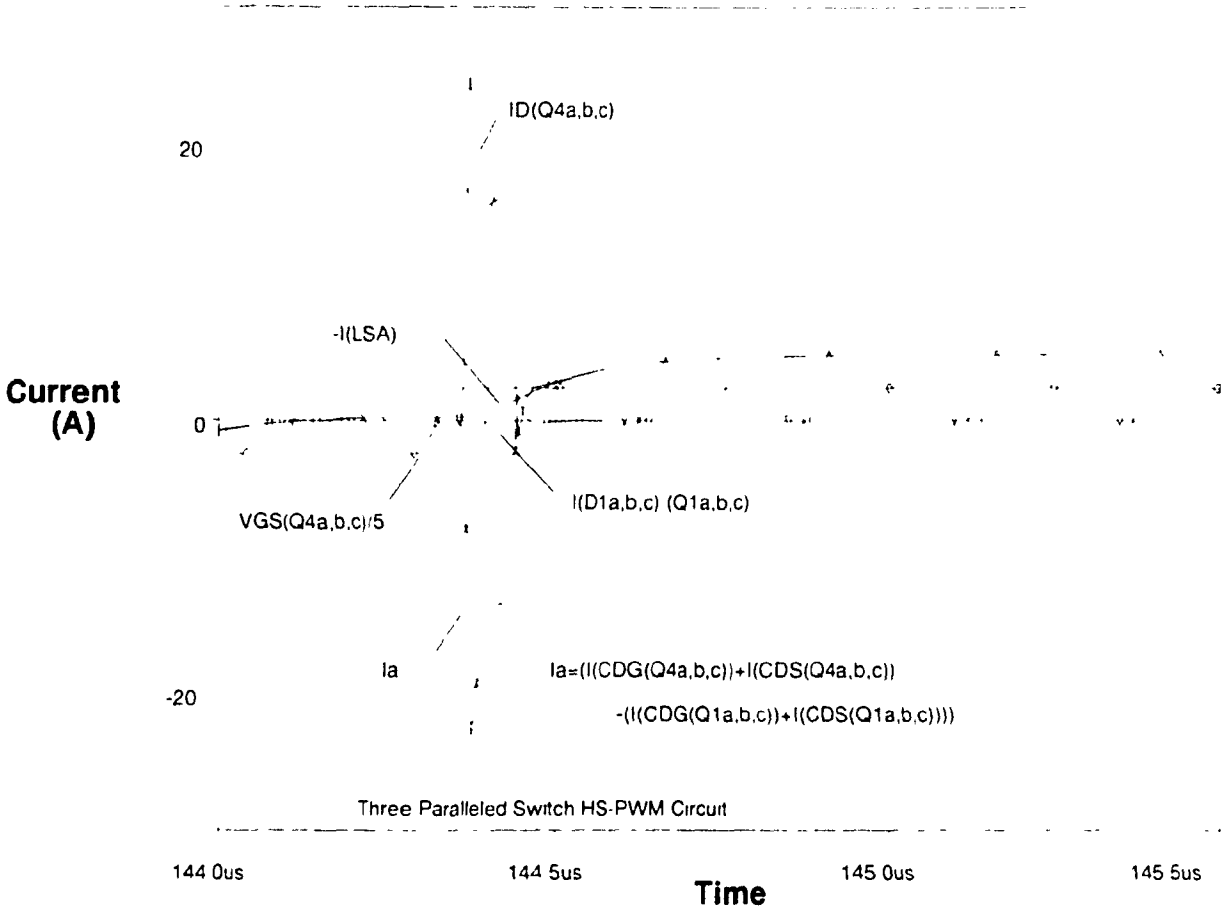


Figure 3.5.4 - HS-PWM MOSFETs Q4a, Qab, Q4c Turn On Capacitive, Drain and Body Diode Currents

3.5.2 Three Paralleled MOSFETs HS-PWM Experimental Results

Experimental results were obtained when the HS-PWM circuit shown in Figure 3.2 1 was connected with three MOSFETs connected in parallel The experimental results obtained along with the simulated results are shown in Table 3.5 1. Simulated results were obtained by using the PSPICE program to simulate the circuit using the MOSFET model described in Chapter 2. The PROBE sub-program of PSPICE was used to graph the waveforms and mathematically generate loss plots which were then read from the graph by the cursor function. The experimental results were obtained by measuring the input power to the bridge and subtracting the output power of the diode filter. The losses of the transformer, diodes, and filter inductor were estimated and subtracted from the final loss result as described in section 3.3.6 Table 3.5.1 shows a comparison of the experimental and simulated results.

Table 3.5.1 Comparison of Experimental, and Simulated Losses for Three Paralleled HS-PWM MOSFETs

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
1	23.92 W	65.80 W	23.92 W
2	38.40 W	79 64 W	37.52 W
3	42.72 W	83.01 W	41.13 W

The total MOSFET losss when they were connected in paralleled for both the simulated and experimental cases were plotted for comparison and shown in Figure 3.5 5

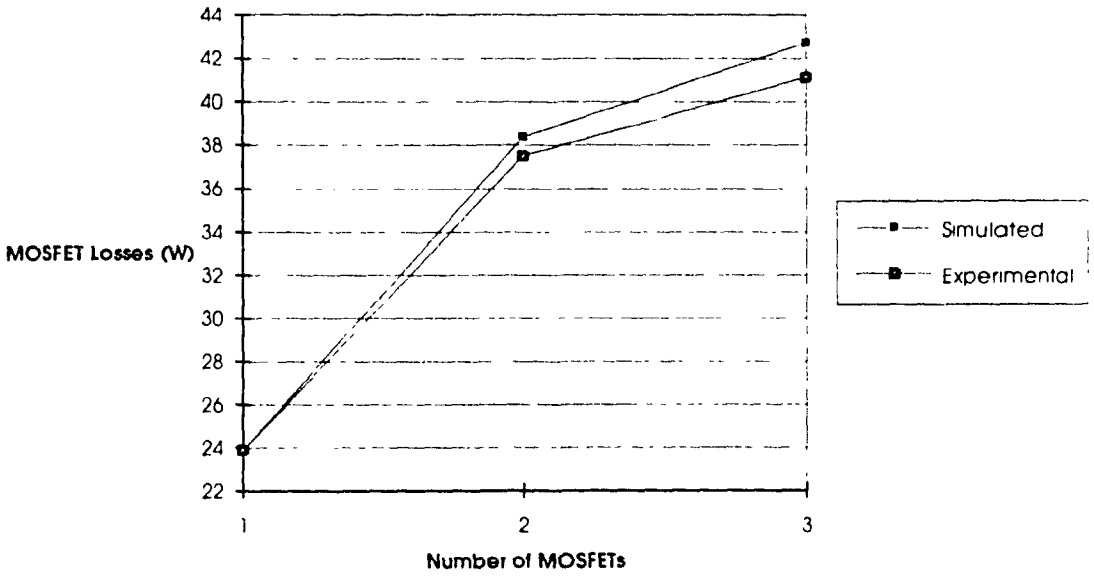


Figure 3.5.5: Plot of Simulated and Experimental Losses for Paralleled MOSFETs used in the HS-PWM Topology

3.5.3 Summary of Losses for Three Paralleled MOSFETs HS-PWM Topology

From the results obtained is this section it is seen that paralleling MOSFETs will decrease the conduction losses because of the decrease of the effective R_{dson}. Switching losses however will increase

because the parasitic capacitances C_{gs} and C_{gd} will also increase requiring more gate drive power to turn the devices on and off. The increase in the drain-source capacitances C_{ds} will require the MOSFET which turns on first to dissipate more energy as it discharges this capacitance for all three devices. The MOSFET which turns on last will also generate the same turn on losses due to the voltage and current as in the single MOSFET case. The MOSFET which turn off last will also experience the same turn off switching losses as a single switch. Also, as mentioned above, since it is unlikely that all three MOSFETs will turn on and off at the same time, there will exist a period of time when only one MOSFET is conducting. During this period it will seem as if only one MOSFET is used and the conduction losses will be the same as in the single MOSFET case.

As switching frequencies are increased, the drive power to charge and discharge the parasitic capacitances will also increase. Also, the time period when only one MOSFET conducts will become more significant with respect to the on time of the MOSFET. This means that the savings obtained by paralleling MOSFETs will decrease as the switching frequency increases. In fact, the decrease in conduction losses may be offset by the increase in switching power required for a given frequency.

From the experimental results it is seen that as more MOSFETs are added in parallel, losses increase. The losses do not triple when three MOSFETs are used in parallel because the conduction losses of the combination decreases and the switching losses caused by the overlap of drain-source voltage and current remains the same for the combination.

When three MOSFETs were used in the experimental circuit, the larger drain-source capacitances C_{ds} affected the operation of the circuit and thus these results should be neglected.

CHAPTER 4

SOFT SWITCHING PWM AND PARALLELED MOSFETs

4.1 Introduction

Soft Switching PWM (SS-PWM) is a popular new modulation technique being used in switching power supplies. As mentioned in Chapter 1, SS-PWM is a modulation technique used to control the output voltage of a power supply which tries to minimize the voltage across, and or the current through the switching elements when they are turned on and off. As a result, SS-PWM converters exhibit conduction losses but minimal switching losses. The decrease in switching losses allows SS-PWM converters to operate at higher frequencies compared to older HS-PWM converters and thus operate at higher power densities. In this chapter, a converter using SS-PWM will be described, and simulated in terms of losses with a single switch and with paralleled switches. Experimental results will also be obtained for the converter using single and multiple switches.

4.2 Soft Switching PWM Topology

Figure 4.2.1 shows a constant frequency, four element series tuned SS-PWM converter topology [26]. The topology consists of a full bridge inverter consisting of 4 MOSFETs and four external snubber capacitors C1, C2, C3 and C4 connected across the MOSFETs drain-source terminals It should be understood that these capacitors are in parallel with the internal drain-source capacitance C_{ds} of the MOSFETs In cases when the drain-source capacitance is large or when MOSFETs are paralleled, the effective capacitance across the MOSFET may be large enough to eliminate the need for the external snubber capacitors Also, the anti-parallel body drain diode D_{ds} of the MOSFET is used in this topology The MOSFET bridge, as in the HS-PWM topology, converts the input DC voltage into a high frequency bipolar waveform which allows the transformer T1 to operate without saturating

A resonant circuit consisting of Lsa, Lsb, Cs, Lp and Cp is used to form a series and parallel resonant circuit. The series resonant circuit consisting of Lsa Lsb and Cs is tuned to have a resonant frequency equal to the switching frequency of the converter so that it will present a minimum impedance to the load. The parallel resonant circuit consisting of Lp and Cp is off tuned so that it will it appears inductive to the MOSFET bridge [27]. This will cause an inductive or lagging current to flow through the MOSFETs and facilitate lossless switching.

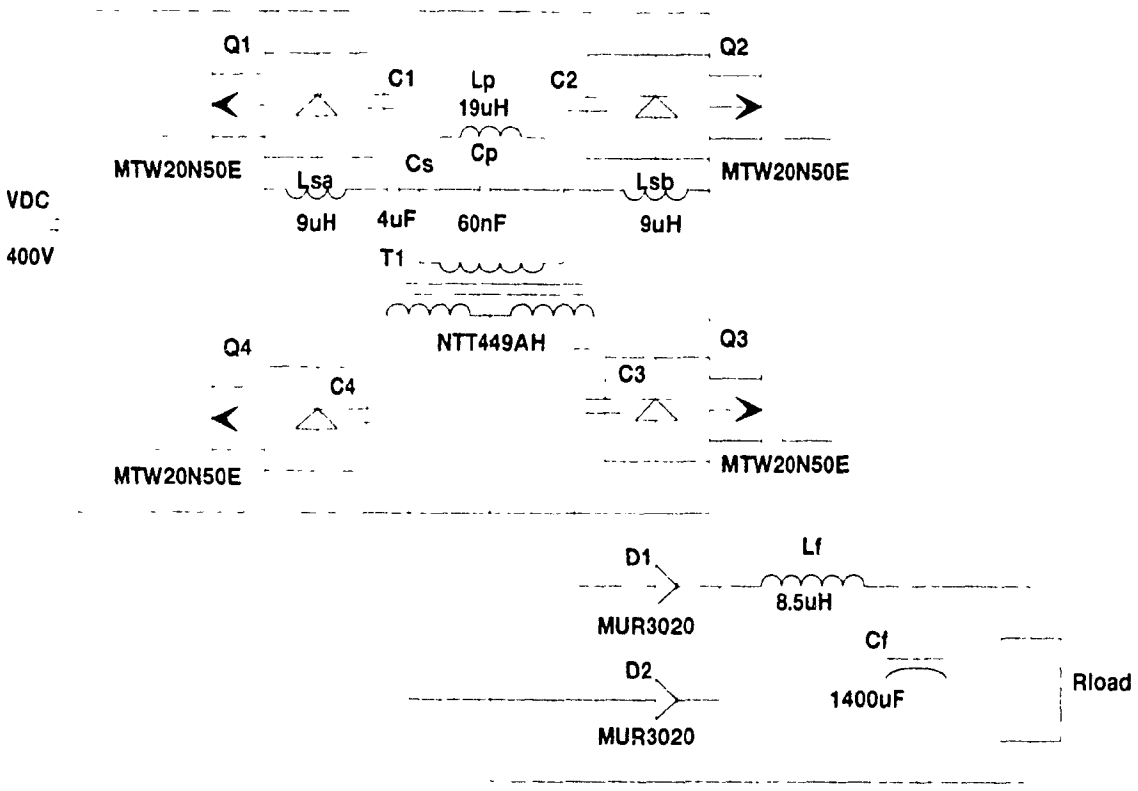


Figure 4.2.1 - SS-PWM Circuit (Phase-Shift Resonant)

The diode rectifiers D1 and D2 and the output filter are the same as in the HS-PWM circuit except that the diodes conduct for their full duty cycle of almost 50% in this topology. This minimizes the voltage stress across the diodes allowing lower forward voltage drop schottky diodes to be used resulting in lower conduction losses. It also allows the filter inductor to be minimized since the conducting diodes will present a voltage to the filter for almost 100% of the switching period.

4.2.1 Modes of Operation

There are eight distinct intervals of operation for the PSM-DTR-PWM converter. Since these intervals are half cycle symmetrical, the first

four cycles involving one pair of MOSFETs will be the same the last four cycles involving the remaining pair of MOSFETs. Thus in this section only the first four intervals will be described.

During the first interval MOSFET Q1 is on and the current is flowing through the resonant circuit and through the anti-parallel body diode of MOSFET Q2.

At the beginning of the second interval MOSFET Q1 is turned off External snubber capacitor C1 will start to charge to the supply voltage and the external snubber capacitor C4 will start to discharge to zero volts. When capacitor C4 reaches zero volts, the anti-parallel body diode of MOSFET Q4 will start to conduct the resonant load current. The resonant load current will flow through the resonant circuit, through the anti-parallel body diodes of MOSFET Q2 and MOSFET Q4 to the DC source

MOSFET Q4 is turned on to start the third interval. The resonant current will be completely or partially transferred from the anti-parallel body diode of MOSFET Q4 to its drain-source channel. Since MOSFET Q4 was turned on when its anti-parallel body diode was conducting, it will not have any turn on losses. During this interval the resonant current will reverse its direction and will flow from the DC source through the drain-source conduction channels of MOSFET Q2 and MOSFET Q4.

At the beginning of fourth interval MOSFET Q2 is turned off. The resonant current will flow through the external snubber capacitor C2 and charge it to the source voltage The resonant current will also flow through the external snubber capacitor C3 and discharge it to zero volts. Since the resonant current was diverted from MOSFET Q2s conduction channel to capacitor C2, the MOSFET will turn off with no losses. When capacitor C3 reaches zero volts the anti-parallel body diode of MOSFET Q3 will conduct the resonant current The current will flow through the drain-source conduction channel of MOSFET Q4 through the resonant circuit and through the anti-parallel body diode of MOSFET Q3 until MOSFET Q3 is turned on The half cycle will repeat itself with MOSFET Q1 and MOSFET Q3

4.3 Single MOSFET SS-PWM Simulated and Experimental Results

As mentioned earlier, soft switching occurs when the MOSFETs are turned on and off when the voltage across or current through them is at zero. PSM-DTM-PWM is a new switching technique used in switching power supplies and is preferred over the quasi-resonant techniques because it uses a fixed switching frequency. The PSPICE model of the MOSFET mentioned in Chapter 2 was used in simulations to observe the charging currents of the parasitic capacitances around the MOSFET. This section will present the analytical results first and summarize them when simulated results are presented in section 4.3.5. Experimental results

will be presented in section 4 3.6 and compared with the simulated results.

4.3.1 SS-PWM Turn On Transition

The charging and discharging of the MOSFETs parasitic capacitors is more complicated for resonant soft switching topologies than for hard switching topologies because the MOSFETs anti-parallel body diode D_{ds} is used to conduct load current during the off state of the MOSFET, and the load current reverses direction during the off state.

The MOSFET is shown in Figure 4.3.1 when it is in its steady-state off condition. Since the gate-source voltage is - *VGS*, all the load current will flow through the MOSFETs anti-parallel body diode D_{ds}, forcing the drain-source voltage to be equal to the forward voltage drop of the anti-parallel diode, - *Vdf*.

Figure 4.3.2 shows when the gate signal is applied to turn the MOSFET on. The gate-source capacitance C_{gs} will start charging to *VGSth*, and the gate-drain capacitance C_{gd} will start charging to *(VGSth - Vdf)*. The charging of the gate-drain capacitance C_{gd} will cause a current to flow from the drive circuit to the load, and the charging of the gate-

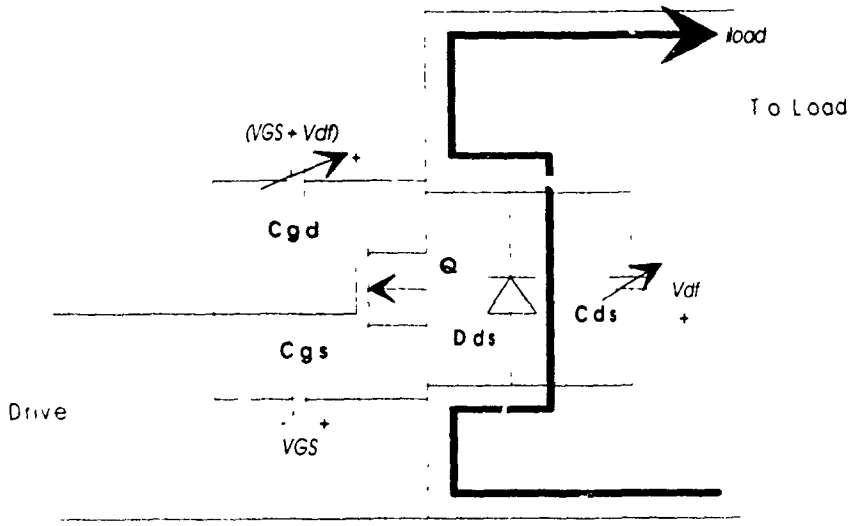


Figure 4.3.1 - SS-PWM Off Condition

source capacitance C_{gs} will cause a current to flow in the gate drive circuit. As in the HS-PWM topology, the drive circuitry includes a resistance to dampen the oscillations which may result when the MOSFET is switched on or off. The parasitic charging currents will flow through this drive resistor and will generate losses.

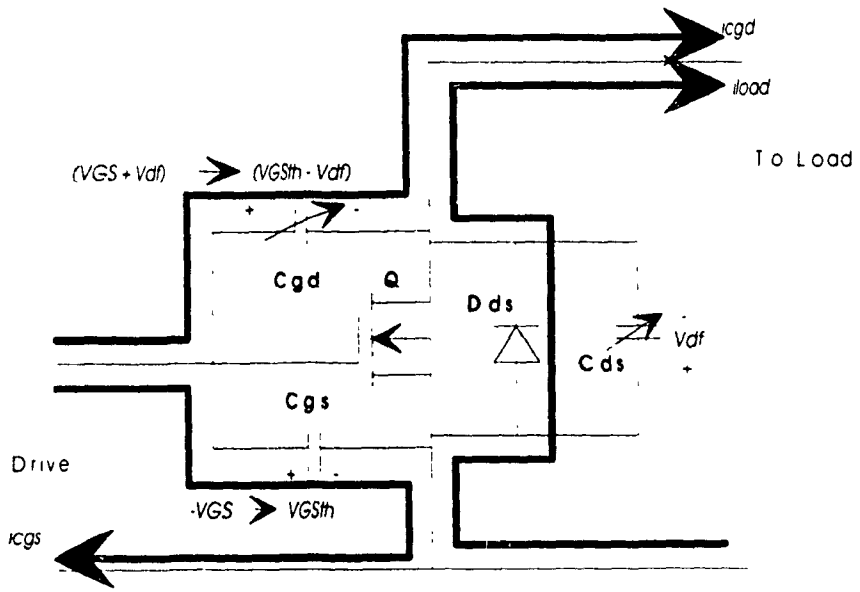


Figure 4.3.2 - SS-PWM Off Condition Vgs < Vgsth

When the gate-source voltage reaches *VGSth* as shown in Figure 4.3.3, the MOSFET will turn on and the load current will start to flow from the source to drain within the MOSFETs drain-source channel. The load current may also flow through the MOSFETs anti-parallel body diode D_{ds}. The division of the load current is determined by its level, the forward drop of the body diode D_{ds}, and the drain-source resistance R_{dson} of the MOSFET. The maximum current which will flow through the MOSFETs drain-source channel will be determined by the forward voltage drop of the body diode *Vdf*, and will be:

$$Id\max = \frac{Vdf}{Rdson} \qquad (4.1)$$

If the load current is greater than Idmax, it will flow through the anti-parallel body diode. The gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} will continue to charge as mentioned above.

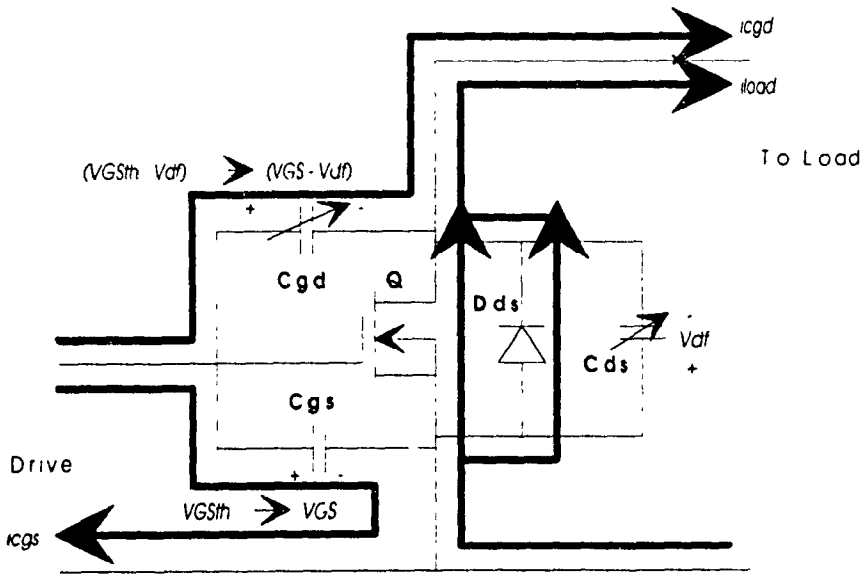


Figure 4.3.3 - SS-PWM Off Condition Vgs > Vgsth

Figure 4.3 4 shows the condition when the gate-source voltage has reached *VGS* and the MOSFETs drain-source voltage is less than the forward drop of the anti-parallel body diode D_{ds}. At this point, all the load current will flow through the MOSFETs drain-source channel. Since the load current is decreasing because of the resonant topology, the voltage drop across the MOSFET will be increasing from *-(ID x RDSon)* to 0V. There will be no charging current for the gate-source capacitance C_{gs} since it has reached its desired voltage. The gate-drain capacitance C_{gd} and the drain-source capacitance C_{ds} will have a charging current as the drain-source voltage decreases to 0V.

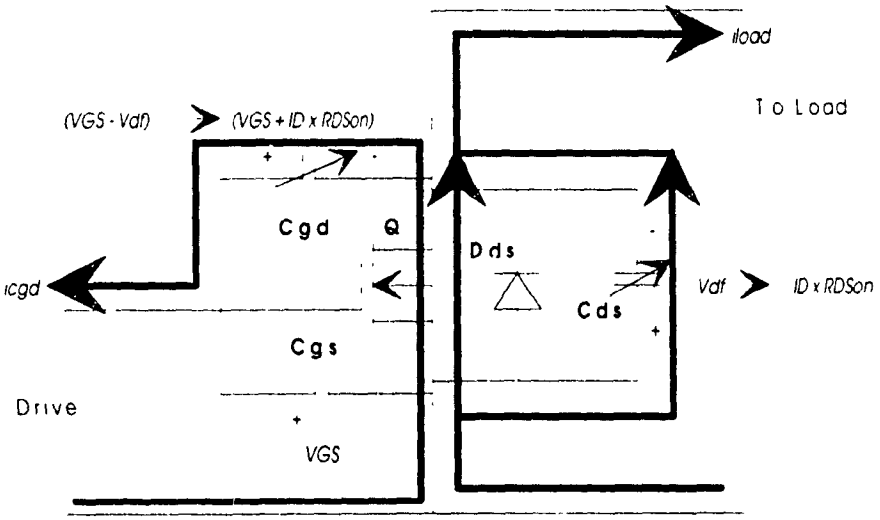


Figure 4.3.4 - SS-PWM On Condition (Iload Decreasing)

Figure 4.3.5 shows the instant when the reversing load current reaches 0A. At this point the drain-source capacitance C_{ds} is at 0V, and the gate drain-capacitance C_{gd} is at *VGS*.

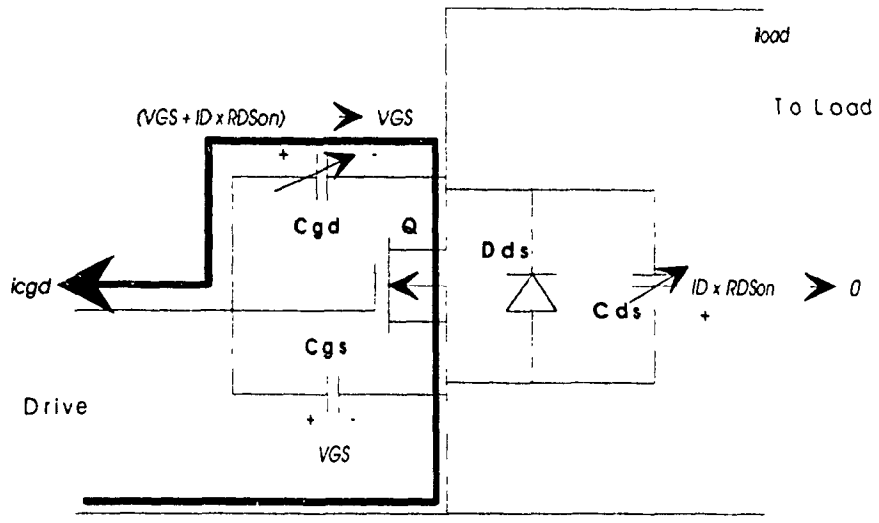


Figure 4.3.5 - SS-PWM On Condition (Iload Approaching 0 Amps)

As the current starts to increase in the opposite direction, the voltage drop across the MOSFET will be *(ID x RDSon)*. Figure 4.3.6 shows this condition which will cause a charging current to flow through the drain-source capacitance C_{ds}, and a charging current to flow through the gate-drain capacitance C_{gd}.

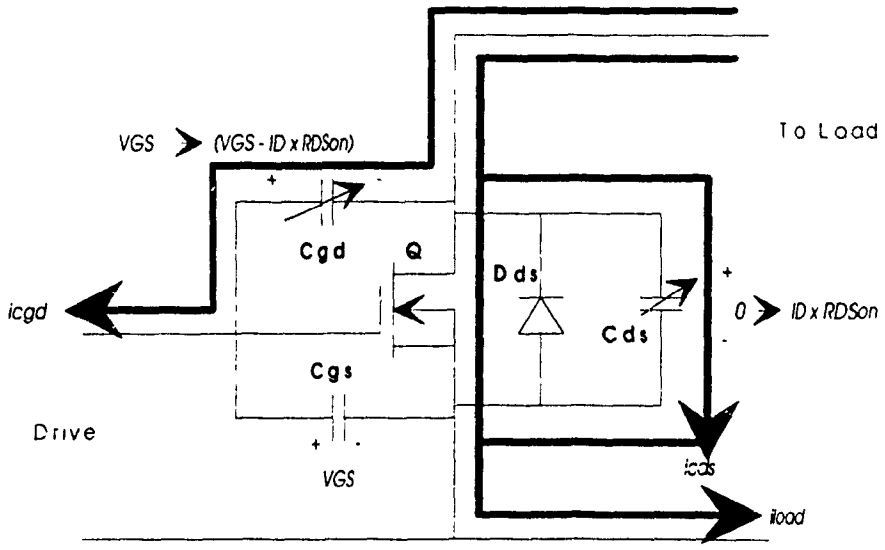


Figure 4.3.6 - SS-PWM On Condition (Iload Reversed)

Figure 4.3.7 shows the MOSFET in its steady state on condition. Since the load current is not constant, the drain-source voltage will change since it is equal to *(ID x RDSon)*. This will result in small charging and discharging currents flowing through both the drain-source capacitance C_{ds} and the gate-drain capacitance C_{gd} during the MOSFETs on condition.

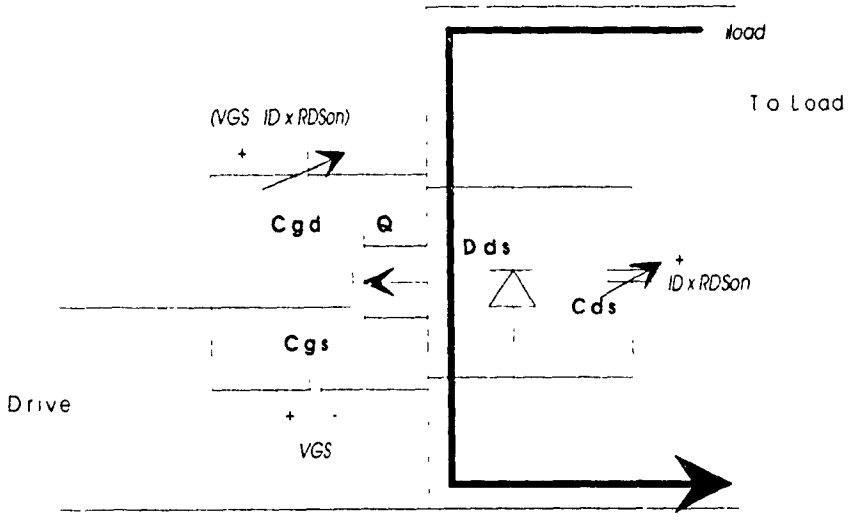


Figure 4.3.7 - SS-PWM On Condition

4.3.2 Losses During SS-PWM Turn On Transitions

Losses for SS-PWM topologies are less than those for HS-PWM topologies but are more difficult to calculate because of the larger number of conditions during switching. For example, conduction losses occur when the MOSFET conducts the load current from drain to source or from source to drain. Also, losses are generated in the anti-parallel

body diode when it is conducting the load current. Also, as in the case of HS-PWM, all the charging and discharging currents flowing through parasitic capacitances C_{dg} and C_{gs}, will generate a loss through the drive source resistance. Unlike HS-PWM, there are no turn on switching losses because the load current discharges the drain-source capacitance C_{ds} and is flowing through the MOSFETs anti-parallel body diode D_{ds}.

4.3.3 SS-PWM Turn Off Transition

The off transition of the MOSFET begins when a negative gate signal is applied as shown in Figure 4.3.8. The load current will flow through the MOSFET causing conduction losses, and discharge currents will flow through the gate-source capacitance C_{gs}, and through the gate-drain capacitance C_{dg}. These currents will generate losses through the drive source resistor.

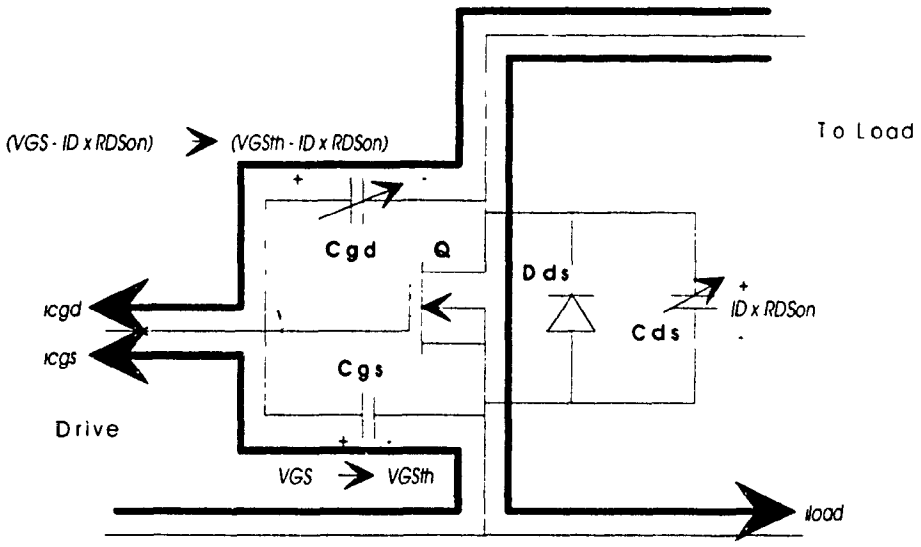


Figure 4.3.8 - SS-PWM On Condition Vgs > Vgsth

When the gate-source voltage reaches *VGSth*, the MOSFET will start to turn off and the drain-source voltage will rise to *VDD* as shown in Figure 4.3.9. This will force a charging current to flow through the drain-source capacitor C_{ds}. In the soft switching topology, an extra capacitor is added to divert the load current away from the MOSFET as it turns off but in the general case, some load current will flow through the MOSFETs drain-source channel as it turns off generating a power loss. As the drain-source voltage rises, the discharge current will continue to flow through the gate-drain capacitance C_{gd}. Also, the gate-source capacitance C_{gs} will continue the discharge to - *VGS*.

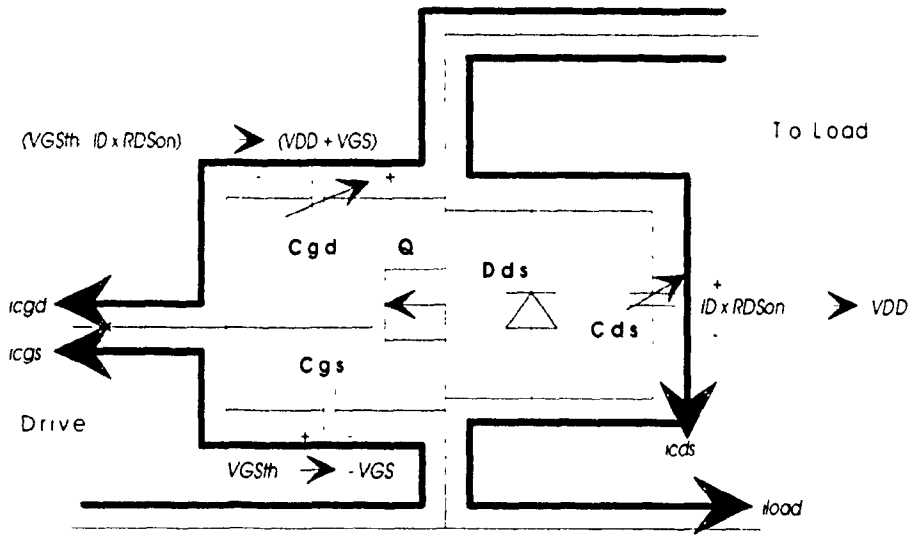


Figure 4.3.9 - SS-PWM On Condition Vgs < Vgsth

In the condition when the load current is low and there is adequate drain-source capacitance added to the circuit, the charging and discharging currents will flow as shown in Figure 4.3.10.

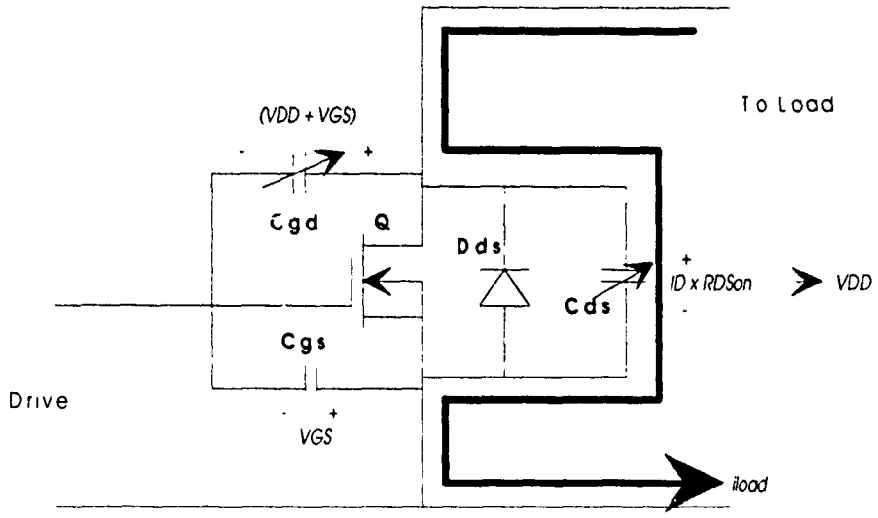


Figure 4.3.10 - SS-PWM Off Condition (Forward Current)

When the gate-source voltage reaches $-VGS$, the MOSFET will be off as shown in Figure 4.3.11. There will be no currents flowing through the parasitic capacitances C_{ds}, C_{gs}, and C_{gd} or the MOSFET. The MOSFET will remain in this condition as long as the load current flows from the load, through the upper MOSFETs drain-source capacitance.

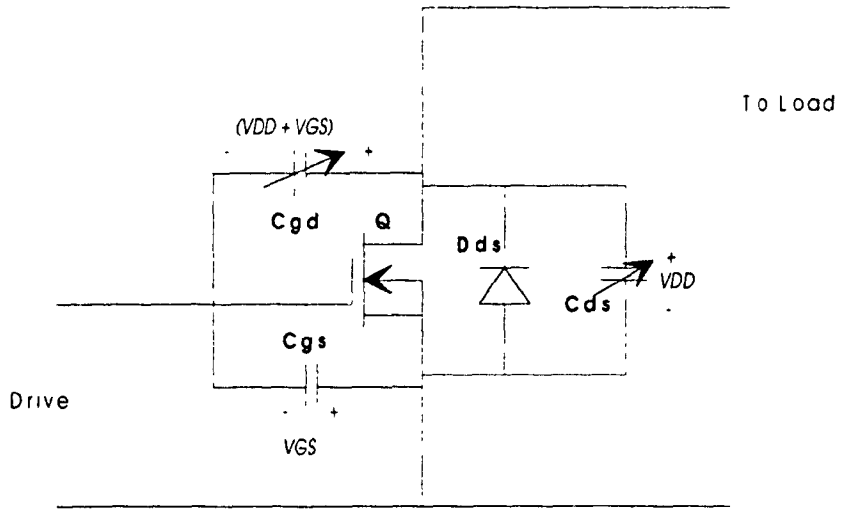


Figure 4.3.11 - SS-PWM Off Condition

Figure 4.3.12 shows the condition when the upper MOSFET turns on. At first, the load current will flow through the drain-source capacitance C_{ds} and discharge its voltage to - *Vdf*. While the drain-source voltage is dropping, a discharge current will also flow from the load through the gate-drain capacitance C_{gd}. This discharge current will flow through the gate-source capacitance C_{gs} and the drive circuit. When the drain-source voltage reaches - *Vdf*, the anti-parallel body diode D_{ds} will start conducting the load current.

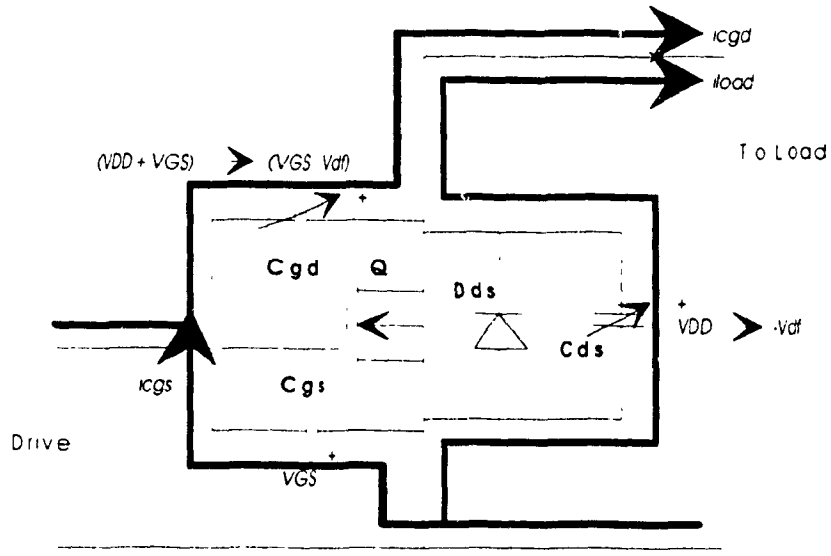


Figure 4.3.12 - SS-PWM Off Condition (Reverse Current)

The MOSFET will be ready to turn on when there will be no charging or discharging currents flowing and the load current will be flowing through the anti-parallel body diode. From Figure 4.3.13, the drain-source capacitance C_{ds} will be - *Vdf*, the gate-drain capacitance C_{gd} will be *(VGS - Vdf)*, and the gate-source capacitance C_{gs} will be - *VGS*.

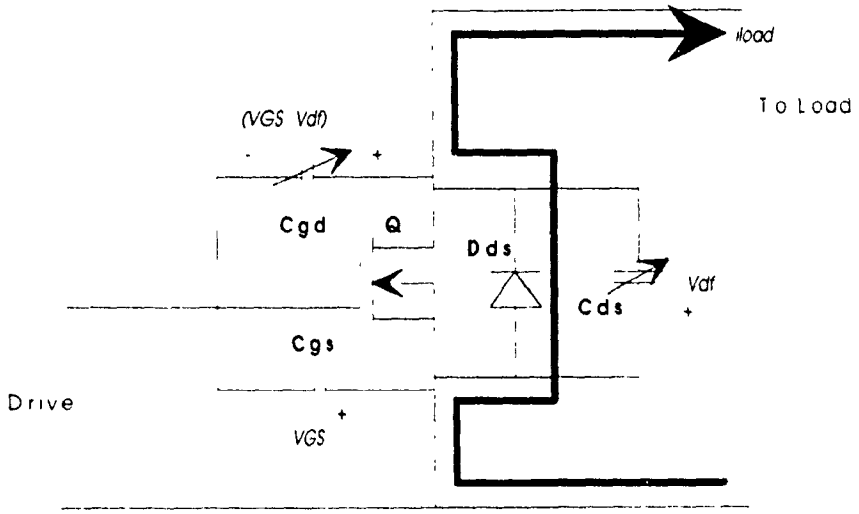


Figure 4.3.13 - SS-PWM Off Condition (Reverse Current)

4.3.4 Losses During SS-PWM Turn Off Transitions

During the turn off transition, the MOSFET will experience losses when it charges and discharges its parasitic capacitances C_{gd} and C_{gs}. Losses will occur when current is flowing through the MOSFETs drain-source channel and its anti-parallel body diode D_{ds}. A turn off loss can also result when the MOSFET attempts to turn off and the load current is diverted to the drain-source capacitance C_{ds}. If the load current is too large and the drain-source capacitance is too small, current will flow through the MOSFETs drain-source channel as it turns off resulting in a turn off loss.

4.3.5 Single MOSFET SS-PWM Simulated Results

The MOSFET model described in Chapter 2 was used in the full bridge resonant circuit shown in Figure 4.2.1 to obtain simulated results. The results presented in this section focus on the turn on and turn off conditions since charging and discharging of the parasitic components occurs during these intervals

Figure 4 3.14 shows the turn off condition of MOSFET Q4. When the MOSFETs drive signal begins to discharge to - 12V at 140.4 uS, a gate-source current will flow through the drive circuit as shown in Figure 4.3.8. The negative current in the plot indicates that this is a discharging current flowing through the gate-source capacitor C_{gs}.

The MOSFET turns off at 140.45 uS. Since the load current must be maintained through the resonant inductors LSa and LSb, it will flow through the MOSFETs drain-source, drain-gate and external snubber capacitances. Also, some of this current will flow through the gate-source capacitances C_{gs}. This interval corresponds to the currents shown in Figures 4.3.9 and 4.3.10.

Current will flow through the parasitic and external snubber capacitances of MOSFETs Q1 and Q4, until MOSFET Q1's drain-source capacitance C_{ds} has discharged to - *Vdf*. At this point, 140 6 uS, the anti-parallel diode D_{ds} of MOSFET Q1 will start to conduct and no significant current will flow through the parasitic capacitances.

Figure 4.3.15 shows the condition when MOSFET Q4 is turned on. At 144.30 uS the MOSFET Q1 will turn off by charging its gate-source capacitance C_{gs} to - *Vgs*. As described above, when MOSFET Q1 stops conducting through its drain-source channel, the drain-source, drain-gate, and external snubber capacitances of MOSFET Q1 will start to charge the drain-source, drain-gate, and snubber capacitances of MOSFET Q4 will start to discharge in order to maintain the load current through inductors Lsa and Lsb. This condition corresponds to Figure 4.3.12. When the drain-source capacitance C_{ds} discharges to - at 144.50 uS, current will flow through the anti-parallel diode D_{ds} of MOSFET Q4 as shown in Figure 4.3.13. No significant currents will flow through the parasitic capacitors when the anti-parallel body diode D_{ds} is conducting.

Figure 4.3.15 shows that MOSFET Q4 is turned on at 144.8 uS when its gate-source capacitance C_{gs} is charged to + *Vgs* as shown in Figure 4.3.2. This will cause a current to flow through the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} of MOSFET Q4.

Figure 4.3.16 shows when MOSFET Q4 is turned off at 140.4 uS, the current flowing through its drain-source conduction channel *(ID(Q4))* and the resonant inductor current *(I(LSA))* will be carried first by the parasitic and the external snubber capacitances of MOSFETs Q1 and Q4 during the interval between 140.45 uS and 140.60 uS. From 140.60 uS, the current to the load will flow through the anti-parallel body diode D_{ds} of MOSFET Q1 until it is turned on at 140.95 uS.

Figure 4.3.17 shows the condition before MOSFET Q4 is turned on. First, the load current will flow through the parasitic and the external snubber capacitors of MOSFETs Q1 and Q4 when MOSFET Q1 is turned off. Current will then flow through the anti-parallel body diode D_{ds} of MOSFET Q4 until it is turned on by the gate signal at 144.8 uS. At this point current will flow through both the anti-parallel body diode D_{ds} and the drain-source conduction channel of MOSFET Q4. The current flowing through the MOSFET Q4 will be from the source to the drain as shown in Figure 4.3.17. As the resonant current decreases, current will first decrease to zero in the anti-parallel body diode D_{ds}, and then decrease to zero in the drain-source conduction channel of the MOSFET before it reverses and flows from the drain to the source.

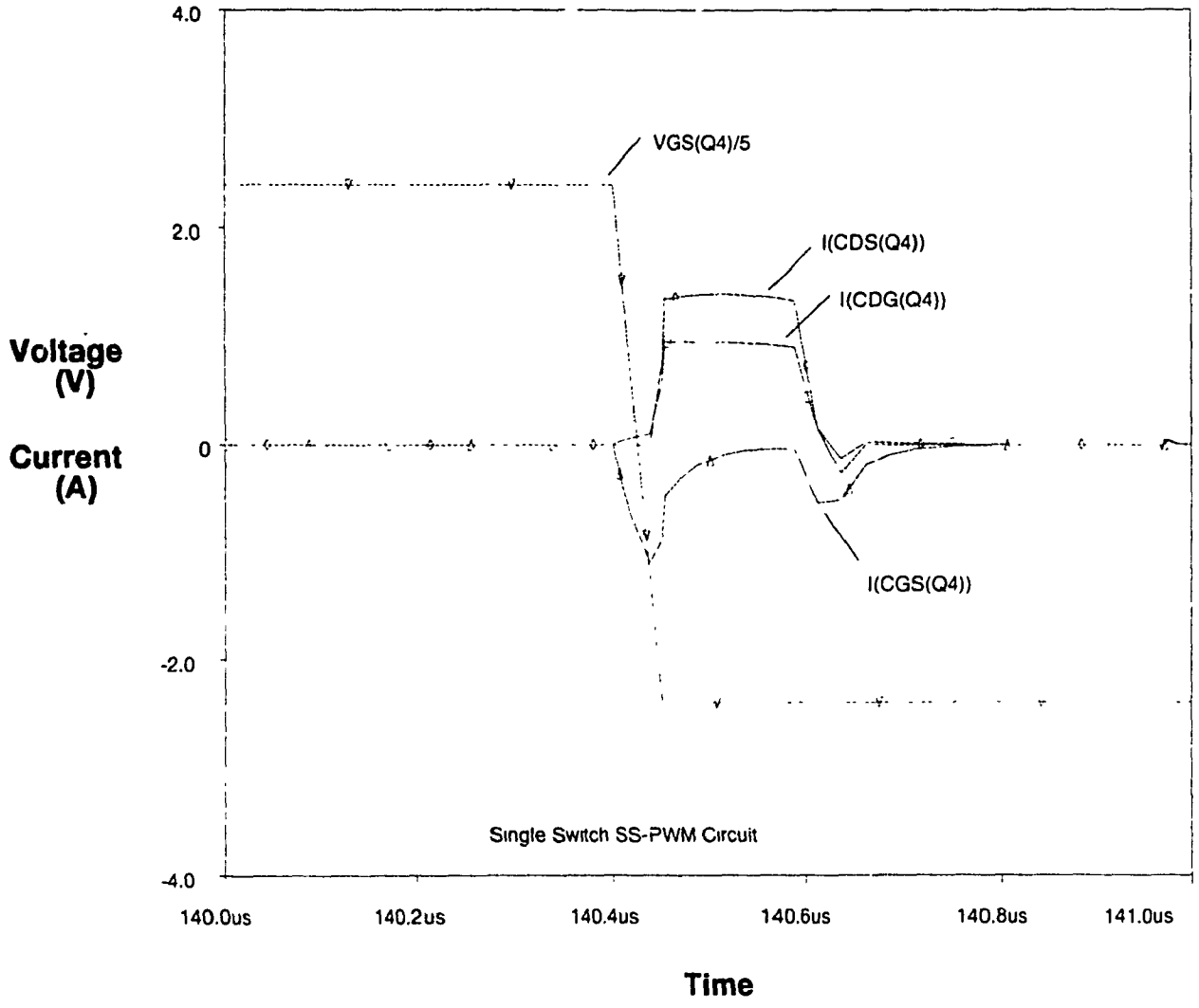


Figure 4.3.14 - SS-PWM MOSFET Q4 Turn Off Parasitic Capacitive Currents

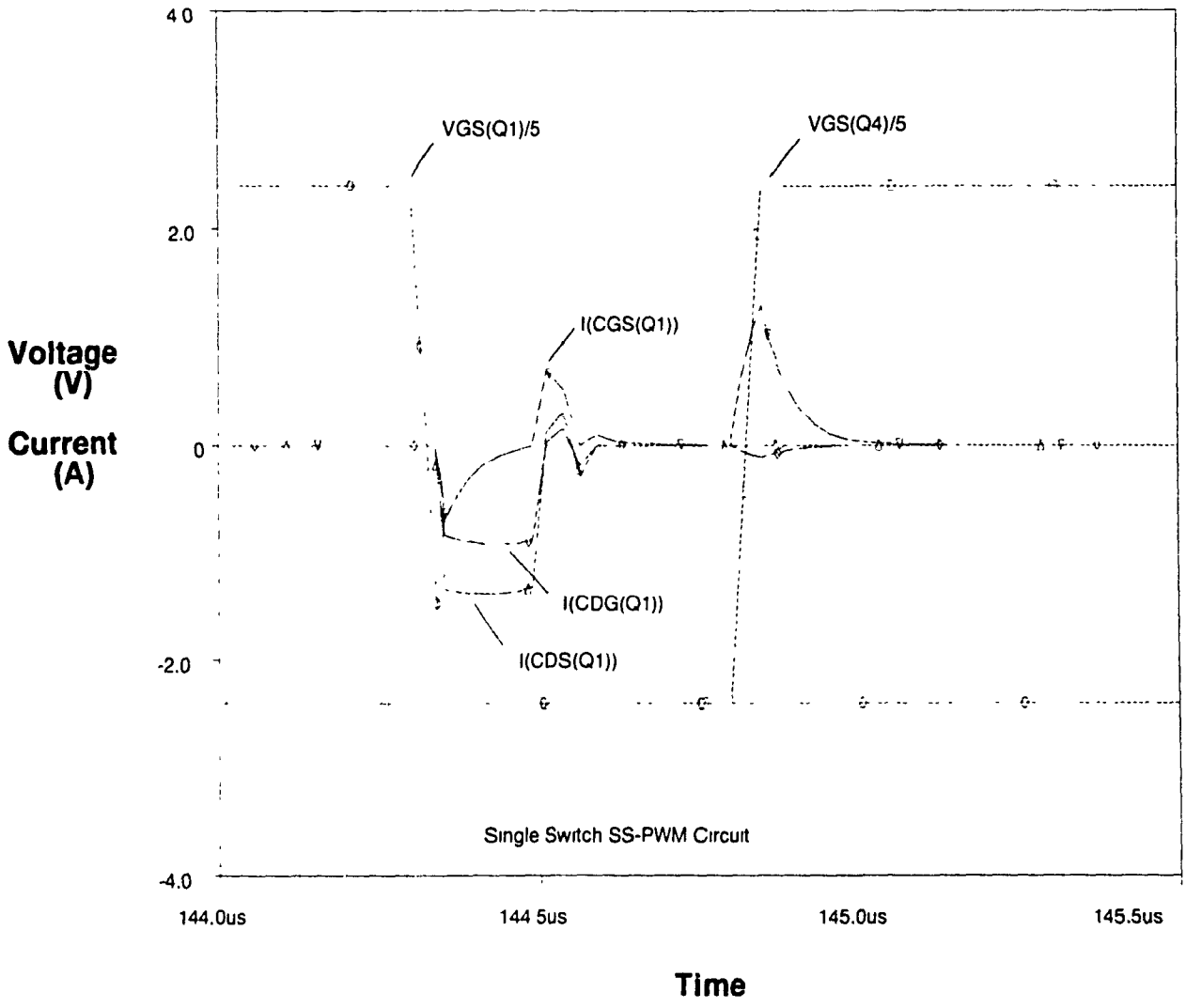


Figure 4.3.15 - SS-PWM MOSFET Q4 Turn On Parasitic Capacitive Currents

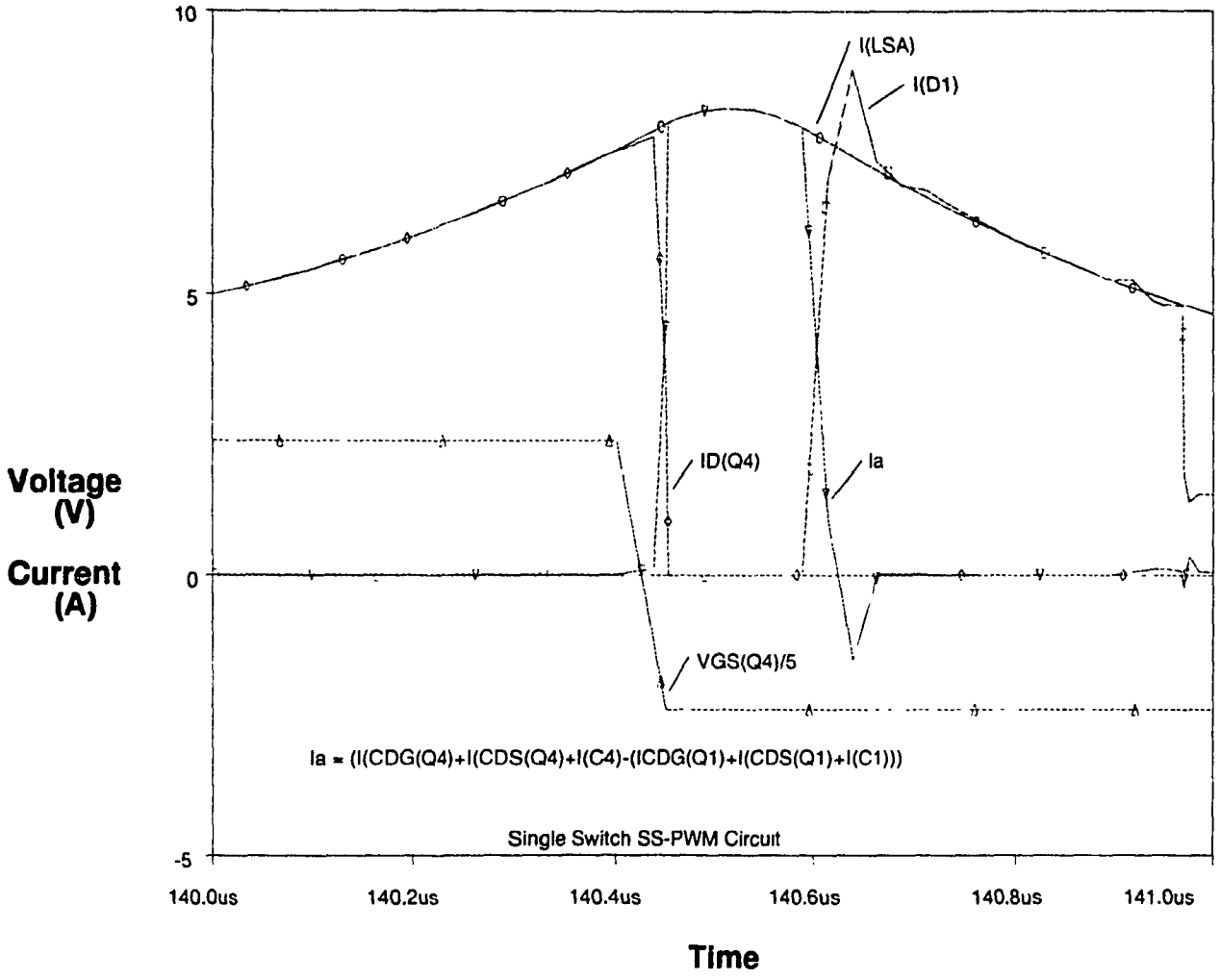


Figure 4.3.16 - SS-PWM MOSFET Q4 Turn Off Capacitive, Drain and Body Diode Currents

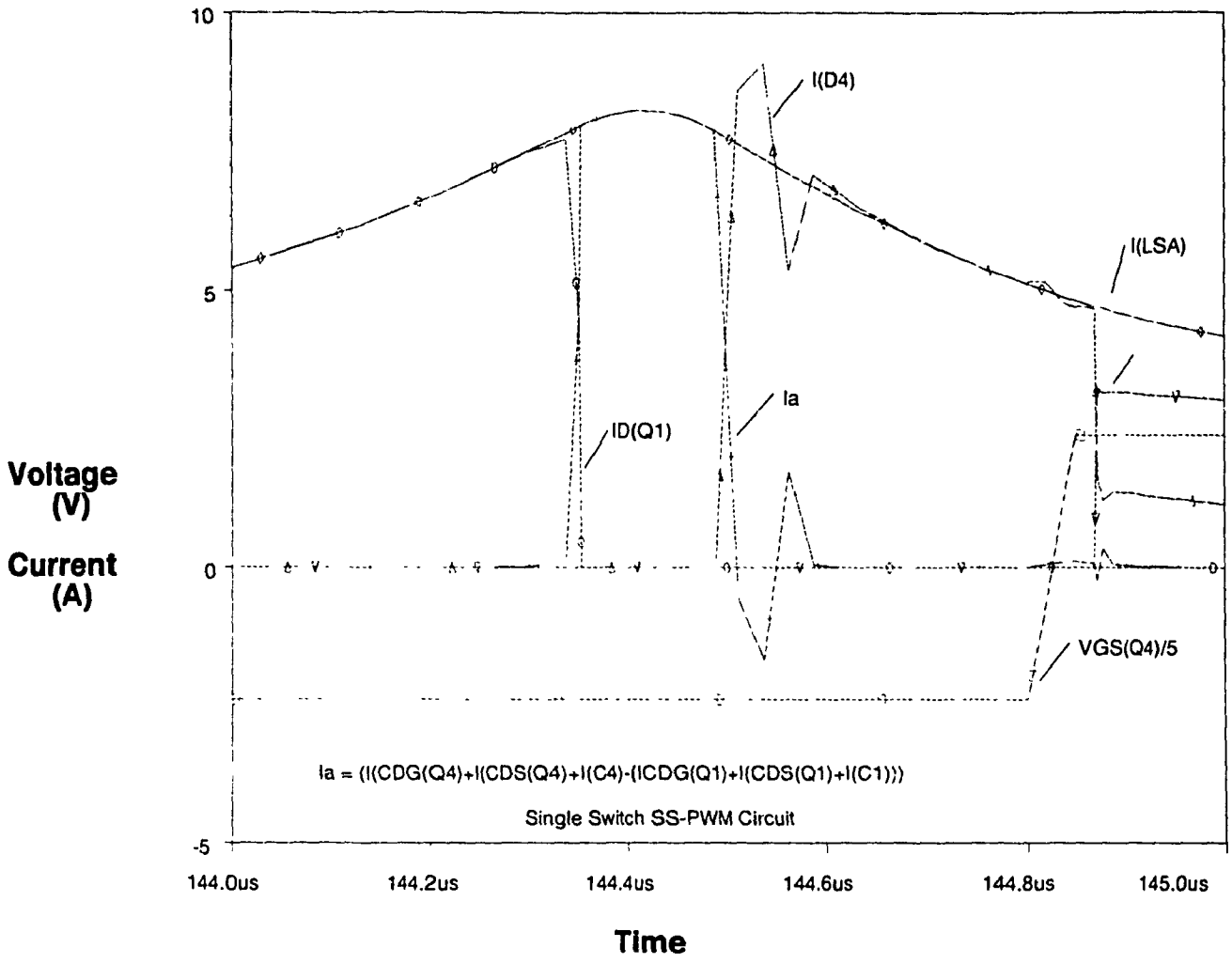


Figure 4.3.17 - SS-PWM MOSFET Q4 Turn On Capacitive, Drain and Body Diode Currents

4.3.6 Single MOSFET SS-PWM Experimental Results

Experimental results were obtained when the SS-PWM circuit was connected as shown in Figure 4.3.18. The experimental results obtained along with the simulated results are shown in Table 4.3.1. Simulated results were obtained by using the PSPICE program to simulate the circuit using the MOSFET model described in Chapter 2. The PROBE sub-program of PSPICE was used to graph the waveforms and mathematically generate loss plots which were then read from the graph by the cursor function.

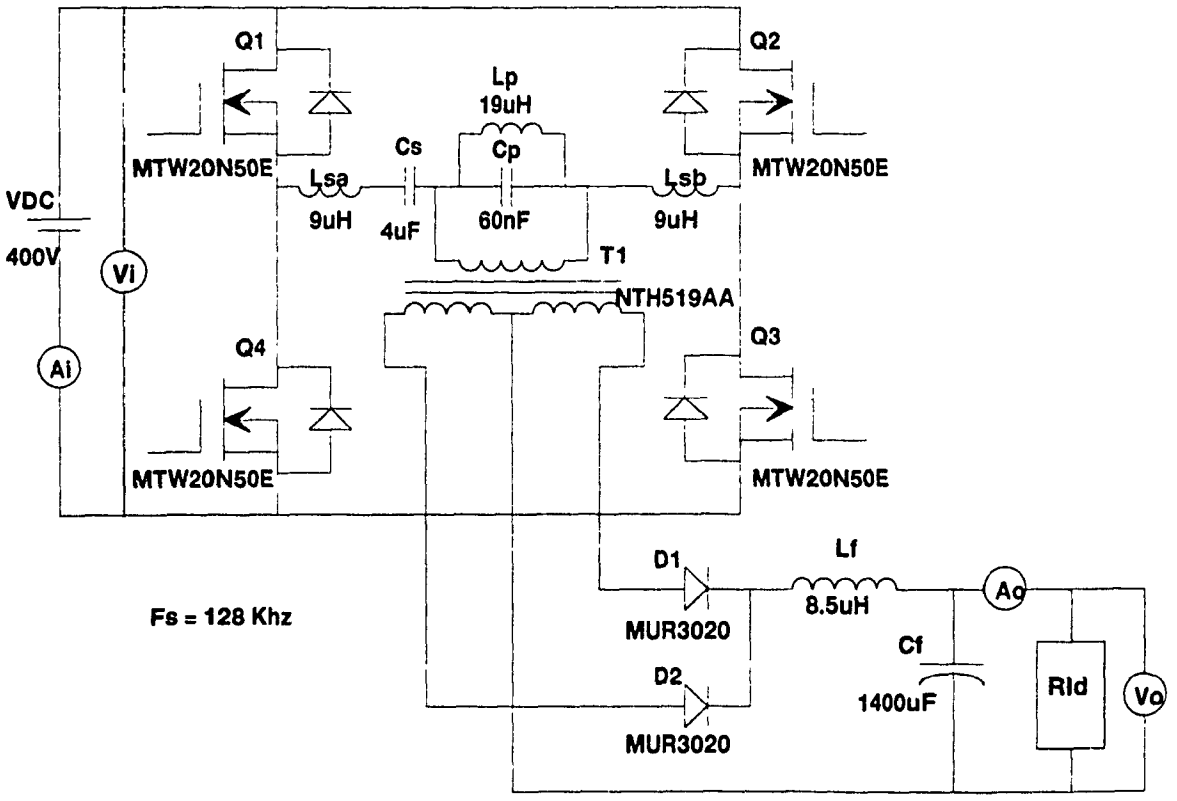


Figure 4.3.18 - SS-PWM Circuit Set-up for Efficiency Measurements

The experimental results were obtained by comparing the output power of the converter to the input power supplied to it. The output power was obtained by multiplying the output current *Ao*, with the output voltage *Vo*. The output current was obtained by using a Keithley 179A TRMS ammeter which could read the current to 5 significant figures. The voltage was read by a Keithley 179A TRMS voltmeter which could read the voltage to 4 significant figures. The input power was obtained by multiplying the input current *Ai*, with the input voltage *Vi*. The same ammeter was used to read both the input and output currents. Also, the same voltmeter was used to read the input and output voltages. It was necessary to read the output DC voltage and current because the high frequency output waveform at the bridge could not be accurately measured by the laboratory equipment available. The losses of the transformer T1, diodes D1 and D2, resonant inductors LSa and LSb, and filter inductor Lf were estimated by subtracting the simulated single switch converter losses from the experimental losses obtained. The losses of T1, D1 and D2, LSa and LSb, and Lf were then assumed to remain constant as switches were paralleled since the current and voltage applied to the bridge remained constant. Any difference in the losses were due to the effects of paralleling MOSFETs. Table 4.3.1 shows a comparison of the losses obtained.

Table 4.3.1 Comparison of Experimental, and Simulated Losses for Single SS-PWM MOSFETs

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
1	15.64 W	47.82 W	15.64 W

4.3.7 Summary of Losses for Single MOSFET SS-PWM Topology

When single MOSFETs are used, conduction losses will be present because of their R_{dson}. There will be no switching losses due to the discharging of the drain-source capacitance C_{ds} when the MOSFETs turns on because the anti-parallel body source diode D_{ds} is conducting at turn on clamping the drain-source voltage at $-V_{df}$. There will be switching losses due to the charging and discharging of the gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs}. At turn off there will be no turn off losses because the snubber capacitors will divert the current away from the MOSFET as it turns off.

4.4 Two Paralleled MOSFETs SS-PWM Simulated and Experimental Results

As in the HS-PWM case when MOSFETs are paralleled the parasitic capacitances C_{gs}, C_{dg} and C_{ds} of both devices are effectively placed in parallel. If the multiple combination of MOSFETs is considered as a single switch, it will have twice the current handling capability and higher parasitic capacitances as in the HS-PWM case. If the multiple combination of MOSFETs is analyzed as two separate switches, it is unlikely that they will turn on and off at the same time unless they are matched as mentioned in Chapter 2. These differences in turn on and turn off times will generate different current flows from those generated in the single switch SS-PWM case.

4.4.1 SS-PWM Turn On Transition

Figure 4.4.1 shows the two parallel MOSFETs in the off condition in the SS-PWM topology. The voltages across the parasitic capacitances C_{ds}, C_{gd}, and C_{gs} are the same in this case as in the single switch example. Important to note is that the load current is flowing through the anti-parallel body diode D_{ds} forcing the voltage across the drain source capacitances C_{ds} to be at the low voltage of - *Vdf*.

When a gate signal is applied to turn the two MOSFETS on, the gate-source capacitances C_{gs} of both MOSFETS will start charging to *VGS* and both gate-drain capacitances C_{gd} will start charging to *(VGS + Vdf)*

as shown in Figure 4.4.2. This will cause a charging current to flow through the gate-source capacitance C_{gs} and the gate-drain capacitance

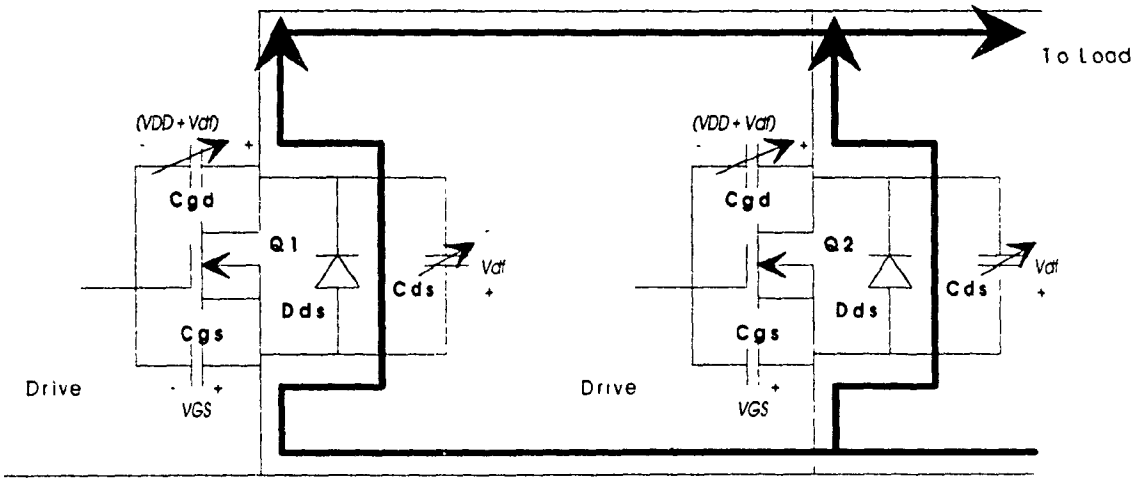


Figure 4.4.1 - SS-PWM Off Condition

C_{gd} of both MOSFETs. The load current will continue to flow through the anti-parallel body diode D_{ds} until the MOSFETs reach their gate-source threshold voltage V_{gsth}. Also, since the MOSFETs are off, the current flow through the gate-drain capacitances C_{gd} will flow from the drive source through the capacitance to the load.

Figure 4.4.3 shows the condition when one MOSFET reaches its gate-source threshold voltage first. In this example, MOSFET Q1 has a lower gate-source threshold voltage V_{gsth} and it will turn on first. The parasitic capacitances of MOSFET Q1 will charge and discharge in the same manner as in the single switch case. The drain-source capacitance

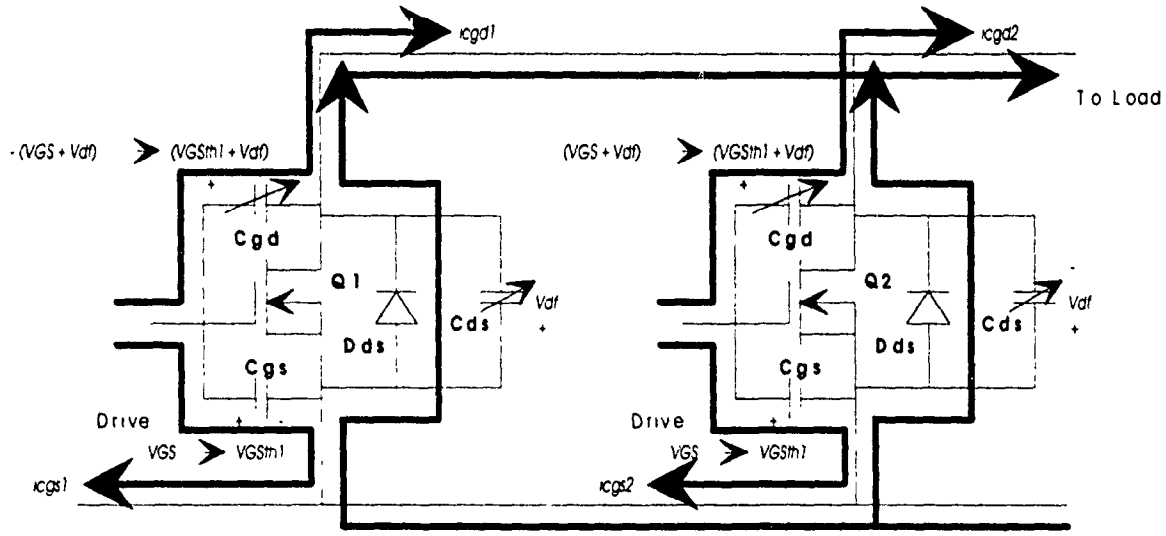


Figure 4.4.2 - SS-PWM Off Condition Vgs < Vgsth1

C_{ds} will remain at - *Vdf* since the MOSFET which is off will conduct through its anti-parallel body diode D_{ds}. The gate-drain capacitance C_{gd} will continue to charge through the load circuit since the load is a current source, and the gate-source capacitance C_{gs} will continue to charge to *VGS* through the drive circuit. The parasitic capacitances C_{gs} and C_{gd} of MOSFET Q2 will charge and discharge as in Figure 4.4.2. Load current will flow through the drain-source channel of MOSFET Q1. If the current is large enough to generate a voltage drop across the drain-source on resistance R_{dson} which is equal to the forward diode drop of the anti-parallel body diode D_{ds}, then current will also flow through the body diode for both MOSFETs.

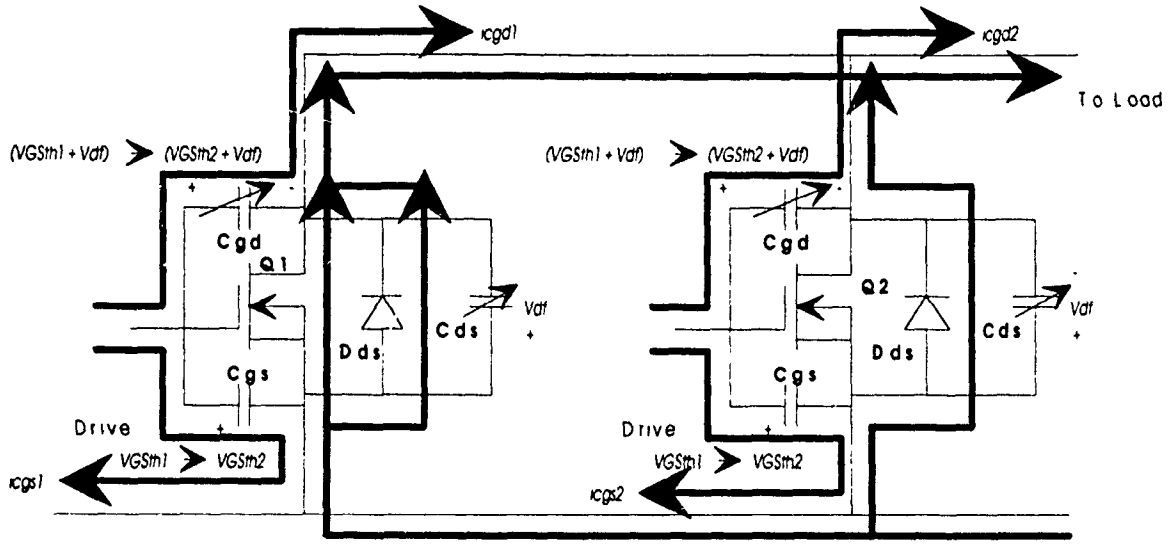


Figure 4.4.3 - SS-PWM Off Condition Vgs > Vgsth1 (Q1 Turns on First)

Both the MOSFETs gate-source voltage will continue to rise until the gate-source threshold voltage of MOSFET Q2 is reached as shown in Figure 4.4.4. During this interval, charging current will flow through both MOSFETs parasitic capacitances C_{gd} and C_{gs}. Load current will start to flow through the drain-source channel of MOSFET Q2. This will lower the currents through the drain-source channel and the anti-parallel body diodes D_{ds} of MOSFET Q1 and MOSFET Q2. If the voltage drop across the drain-source conduction channel of both MOSFETS is less than the forward drop of the anti-parallel body diodes, then all the load current will flow through their drain-source conduction channels. If the voltage drop across the conduction channel is greater than the forward drop of the anti-parallel body diodes *Vdf*, a current of *- Vf/(2 x Rdson)* will flow through the MOSFETs conduction channel and the rest of the load current will be shared by the MOSFETs anti-parallel body diodes D_{ds}.

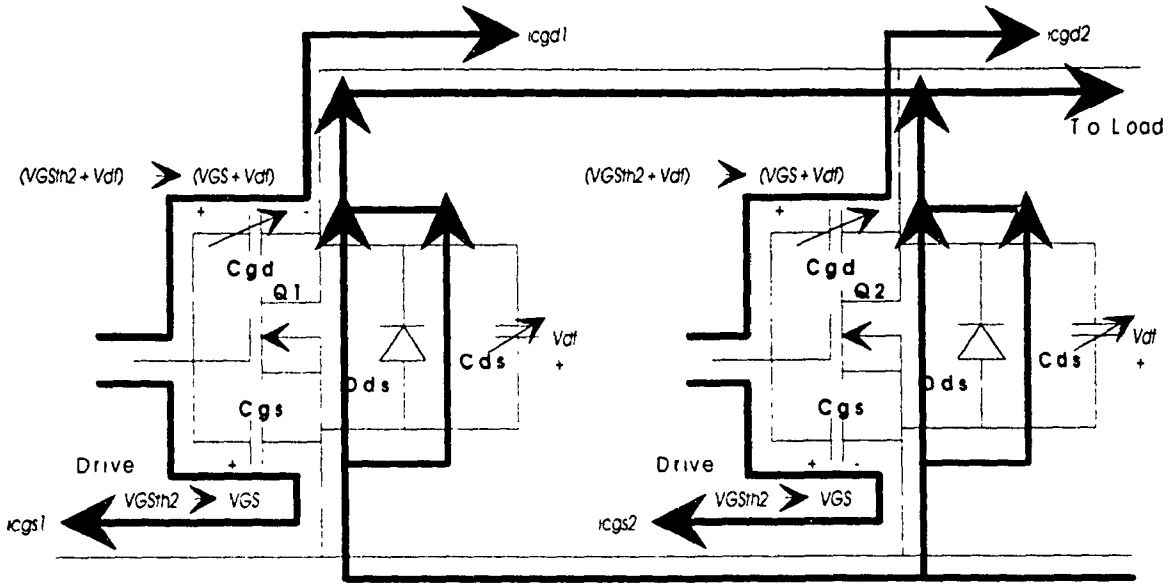


Figure 4.4.4 - SS-PWM On Condition Vgs > Vgsth2 (Q1 and Q2 on)

Figure 4.4.5 shows the condition when both MOSFETS are fully on and the load current is decreasing. If the load current was large enough for it to be flowing through both MOSFETS drain-source conduction channels and the anti-parallel body diodes D_{ds}, it will first stop flowing through the anti-parallel body diodes as the drain-source voltage drops and then gradually decrease through the MOSFETs drain-source conduction channels. While this occurs, the drain-source voltage will change from - *Vdf* to - *(ID x RDSon)* to 0 volts. This will cause a charging current to flow through the drain-source capacitance C_{ds}. The current through the gate-drain capacitance C_{gd} will reverse direction and flow through the MOSFET instead of the load.

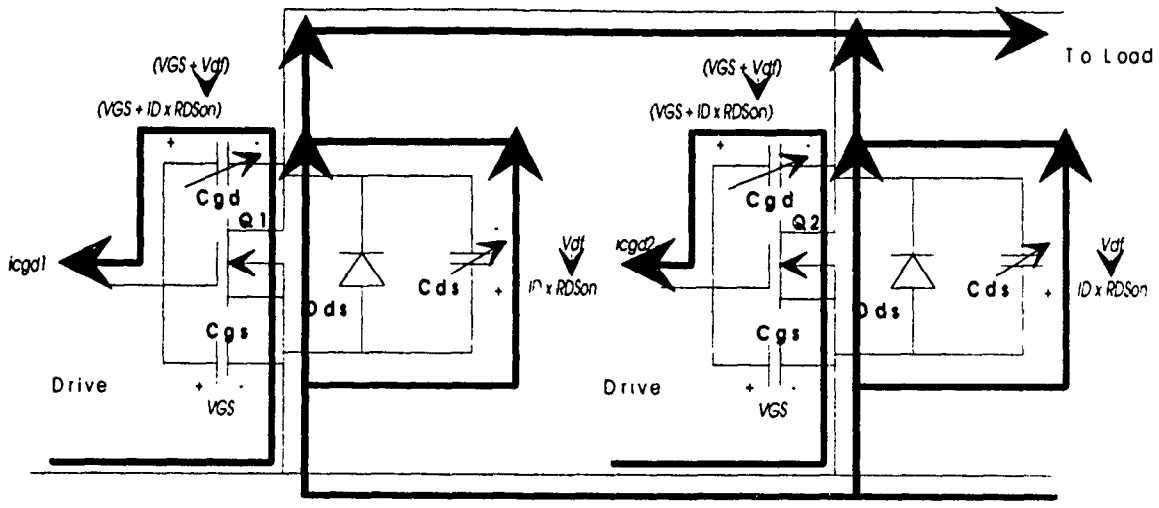


Figure 4.4.5 - SS-PWM On Condition (Reverse Current)

Figure 4.4.6 shows the condition when the reversing load current is 0 amps. There will be no charging current for the gate-source capacitances C_{gs} since they are charged to *VGS*. The charging current for the gate-drain capacitances C_{gd} will continue to flow through the MOSFETs conduction channel and not through the load.

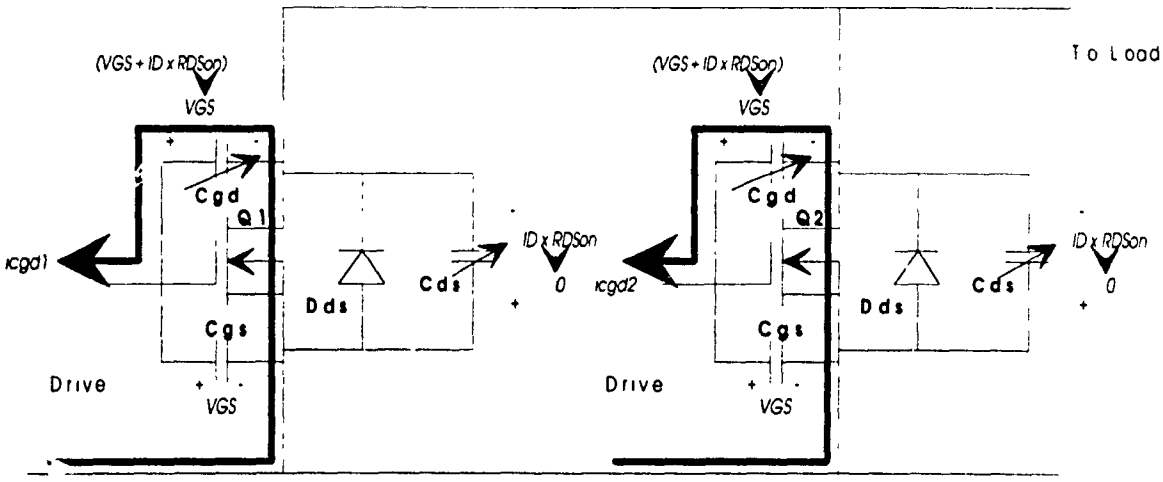


Figure 4.4.6 - SS-PWM On Condition (Iload Decreasing)

When the load current starts to increase in the forward direction as shown in Figure 4.4.7, load current will start to flow through the MOSFETs drain-source conduction channels. As the voltage drop across the drain-source of the MOSFETs increases with current, some load current will flow through the drain-source capacitances C_{ds}. Drive source current will also flow through the gate-drain capacitance C_{gd} as the voltage across it changes from *VGS* to *(VGS - (ID x RDSon))*.

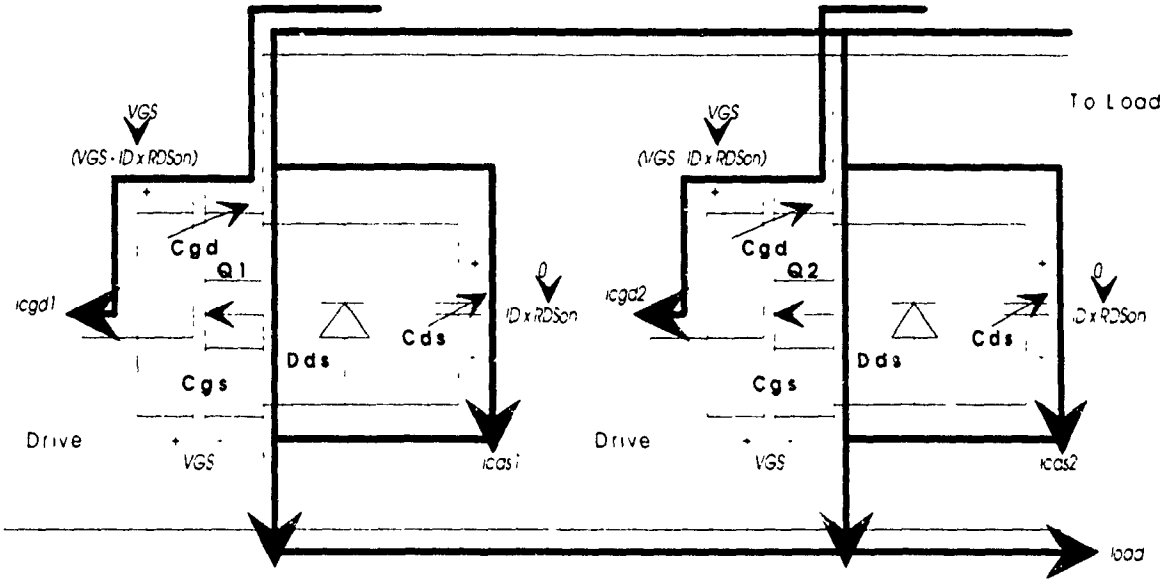


Figure 4.4.7 - SS-PWM On Condition (Forward Current)

Figure 4.4.8 shows the MOSFETs in their on condition with forward current flowing through them. There will be some charge current flowing through the drain-source and gate-drain capacitances C_{ds} and C_{gs} as the current through the drain-source conduction channel increases causes the drain-source voltage to increase.

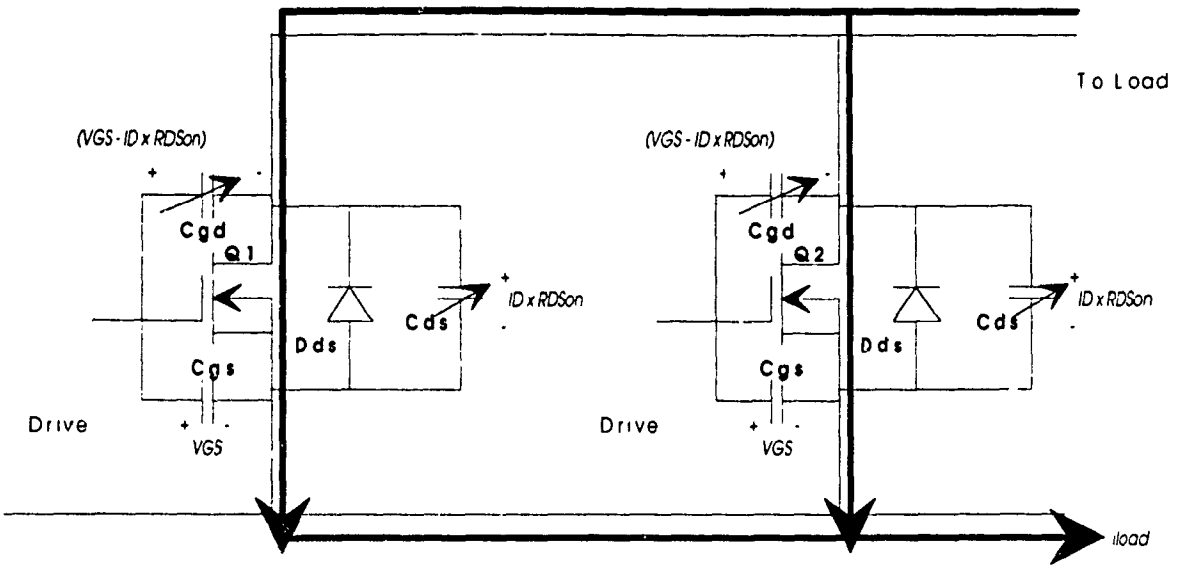


Figure 4.4.8 - SS-PWM On Condition

4.4.2 Losses During SS-PWM Turn On Transitions

As in the single MOSFET case, the currents flowing through the gate-source and gate-drain capacitances C_{gs} and C_{gd} will generate losses because they will also flow through the drive source resistance. Since the voltage across drain-source capacitance C_{ds} is almost 0 volts when the MOSFETs are turned on, there will be no turn on losses and the addition of more MOSFETs in parallel will not increase the switching losses as in the HS-PWM case where losses increased with the addition of more MOSFETs. The increase in the gate-drain capacitances C_{gd} and the gate-source capacitances C_{gs} will increase the drive power required to turn the MOSFETs on and off. Also, some load current will be diverted to charge and discharge the gate-drain capacitance C_{gd} through the drive source resistance resulting less power delivered to the load. This will also lower the overall efficiency.

Conduction losses on the other hand, will be less because of the lower effective R_{dson} which results when multiple MOSFETs are used. The greatest savings occur when both MOSFETs turn on at the same time. As in the HS-PWM case, this is a highly unlikely condition. Practically, there will always be a delay between the turn on of both MOSFETs. During this period, the conduction losses will be similar as if only one MOSFET was used. Since this delay period is a function of the MOSFETs transconduction g_{fs}, gate-source threshold voltage V_{gsth}, and input capacitance C_{iss}, the delay will be constant to the particular MOSFET combination. The delay will also be independent of the switching frequency. Therefore, as the switching frequency is increased as is the tendency in SS-PWM circuits since there are lower switching losses, the delay will become more significant with respect to the conduction period. This will diminish the savings in conduction losses. This creates a contradiction since SS-PWM has smaller switching losses which allows higher switching frequencies for single MOSFET switches. For the paralleled MOSFET switch however, the higher switching frequencies make the delay time for both MOSFETs to conduct more significant and thus minimizes the effects of paralleling. This compromise should be considered when the designer is considering the switching frequency and whether MOSFETs should be paralleled.

4.4.3 SS-PWM Turn Off Transition

Figure 4.4.9, shows when the turn off gate signal is applied to the MOSFETs. Currents will flow from the load circuit to the gate drive

circuit through the gate-drain capacitances C_{gd}, and circulate in the gate drive circuit through the gate source-capacitances C_{gs} as in the single switch case.

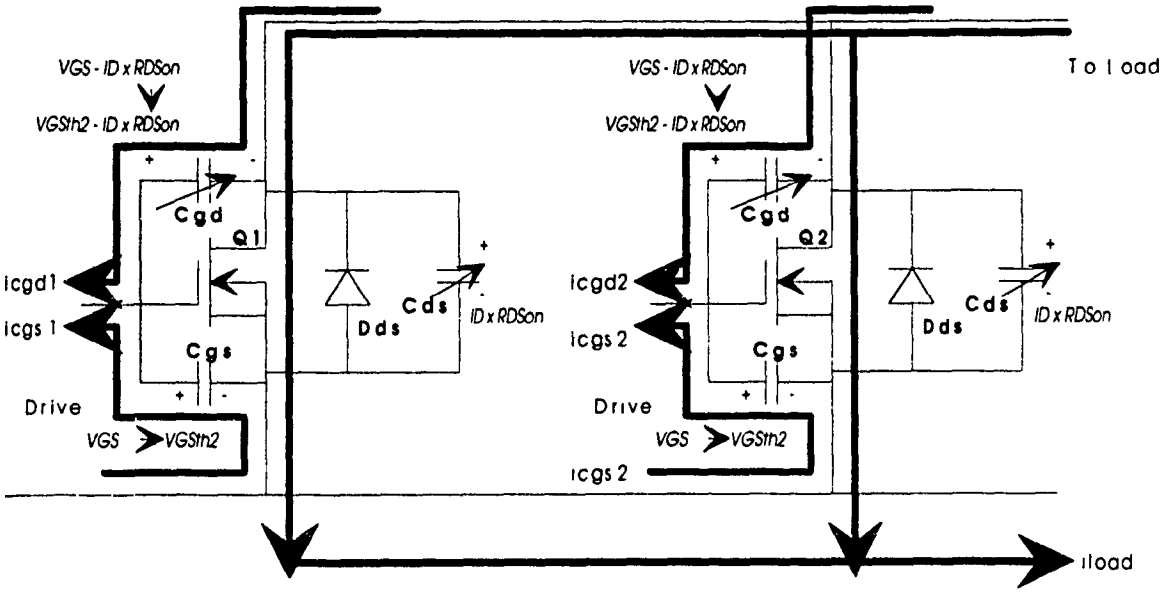


Figure 4.4.9 - SS-PWM On Condition Vgs > Vgsth1

When the gate-source threshold voltage V_{gsth} is reached by MOSFET Q1, it will start to turn off as shown in Figure 4.4.10. The load current will continue to flow through the MOSFET Q2 which is still on. The currents through the parasitic capacitances C_{dg} and C_{gs} will continue to flow during this period.

When the gate-source threshold voltage V_{gsth} of MOSFET Q2 is reached, it will start to turn off as shown in Figure 4.4.11. The load current will flow through the drain-source capacitances C_{ds} of both MOSFETs as the drain-source voltage increases across the MOSFETs. No

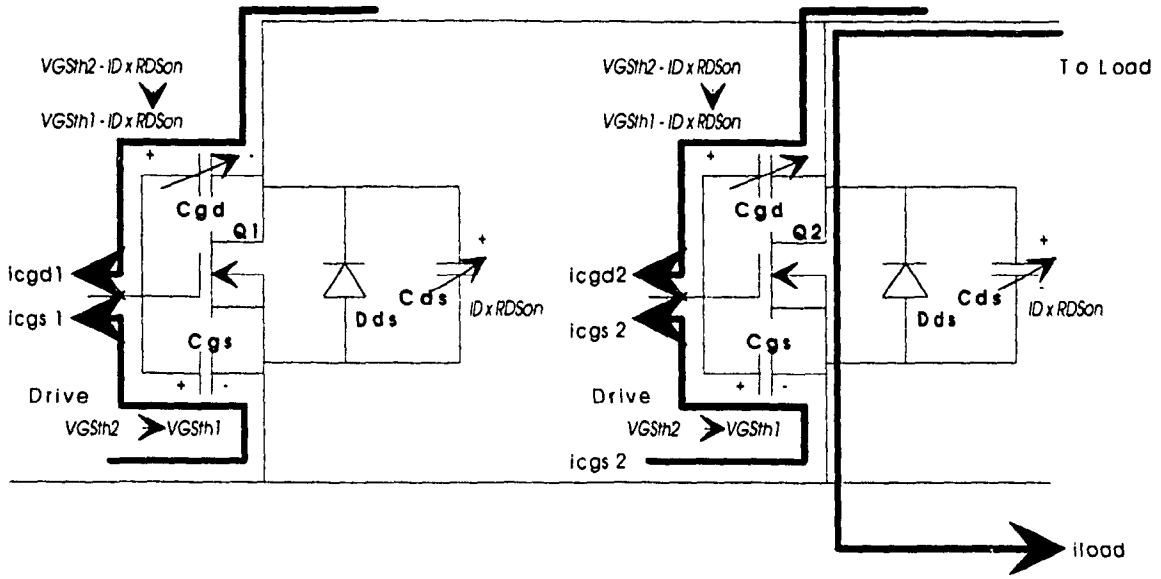


Figure 4.4.10 - SS-PWM On Condition Vgs > Vgsth2 (Q1 turns off first)

load current will flow through the drain-source channel of the MOSFETS as the drain-source capacitances are charging. External capacitances may be added across the MOSFETs to increase the time taken to charge the drain-source capacitances C_{ds} to *VDD*. This will allow the other switches in the leg to turn on with zero or little voltage across them. Again, currents will continue to flow through the gate-drain capacitances C_{gd} as the drain-source voltage increases. Currents will also flow through the gate-source capacitances C_{gs} as the gate drive circuit lowers the gate-source voltage *Vgs*.

Figure 4.4.12 shows the off state of both MOSFETs. During this condition the only current flowing is the leakage drain-source current which is negligible and can be ignored. The drain-source capacitances C_{ds} are charged to *VDD*, the gate-drain capacitances are charged to *-(VDD + VGS)*, and the gate-source capacitances C_{gs} are charged to *- VGS*.

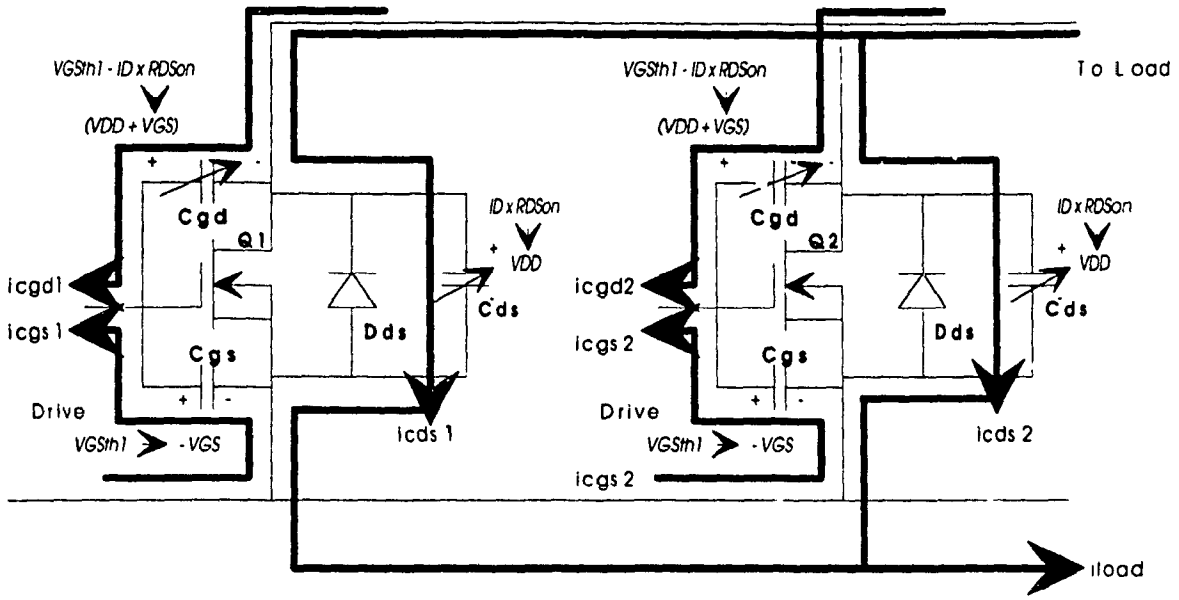


Figure 4.4.11 - SS-PWM Off Condition (Q1 and Q2 off)

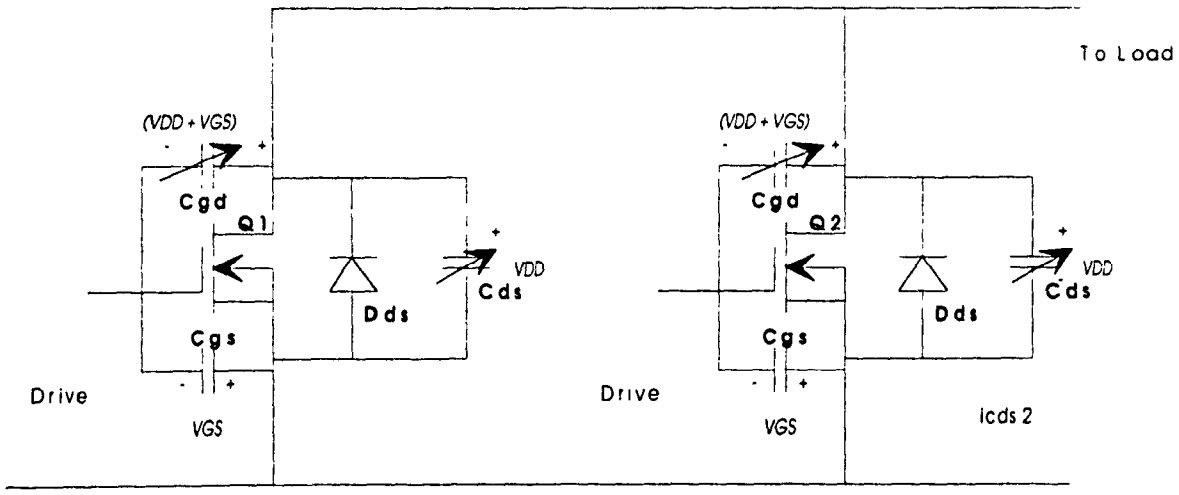


Figure 4.4.12 - SS-PWM Off Condition

When the upper MOSFET is turned off, the load current will first start to flow through the drain-source capacitances C_{ds} as shown in Figure 4.4.13. This will discharge them to - *Vdf*. While the voltage across the drain-source capacitances C_{ds} is decreasing, the gate-drain capacitances C_{gd} will be discharging through the drive circuit and the load until the voltage across them is - *(VGS + Vdf)*.

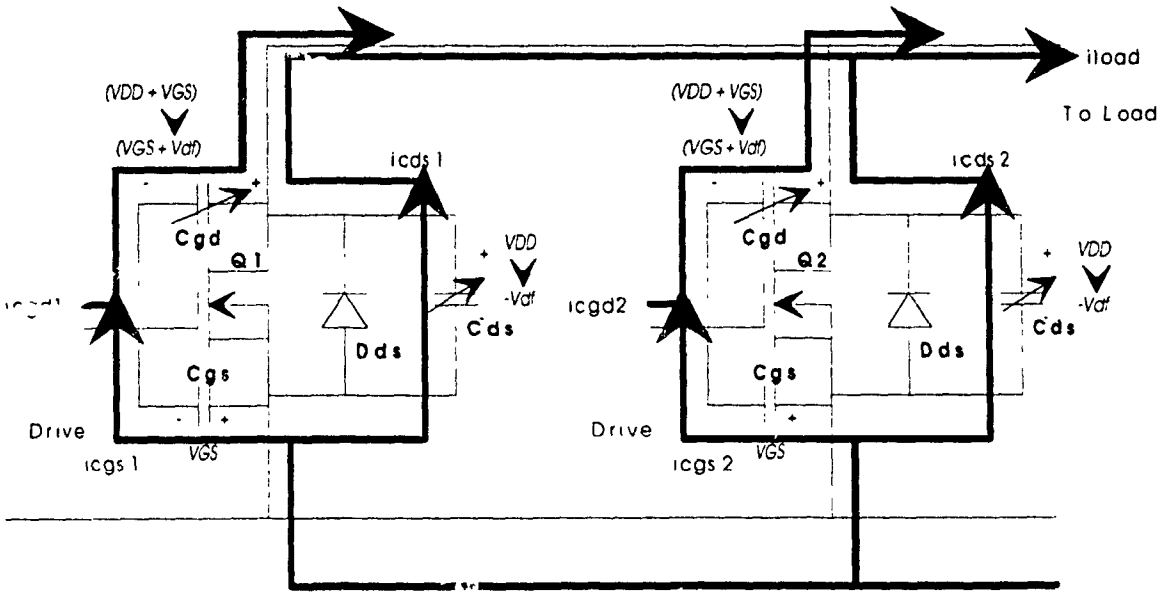


Figure 4.4.13 - SS-PWM Off Condition (Reverse Current)

When the voltage across the drain-source capacitance reaches - *Vdf*, the anti-parallel body diodes D_{ds} will start to conduct the load current as shown in Figure 4.4.14. These diodes will continue to conduct the load current until the MOSFETs turn on. When they turn on, some current will be diverted to the MOSFETs drain-source conduction channel.

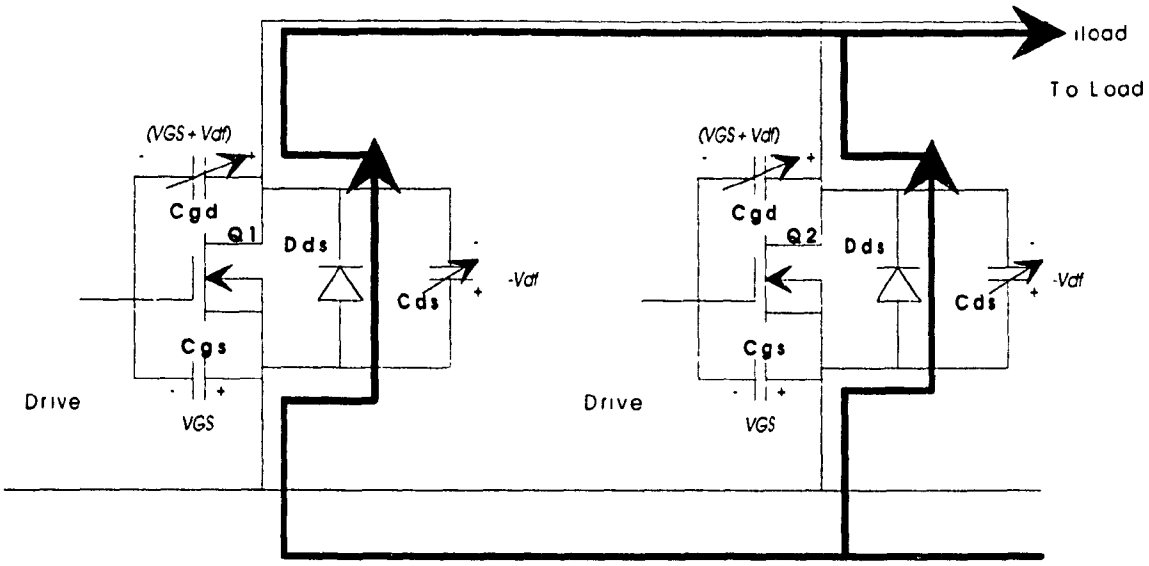


Figure 4.4.14 - SS-PWM Off Condition (Reverse Current)

4.4.4 Losses During SS-PWM Turn Off Transitions

As in the turn on transition, losses will occur when current is flowing through the gate-drain capacitances C_{gd} and the gate-source capacitances C_{gs}. More power will be required in the multiple switch case because of the increased parasitic capacitances C_{gs} and C_{gd}. Conduction losses will be lower as mentioned above when both MOSFETs are on. When one MOSFET is on and the other is off, the conduction losses will be the same as in the single switch case. As in the turn on transitions, the delay time which only one MOSFET is conducting will decrease the gains in efficiency as the switching frequency is increased.

4.4.5 Two Paralleled MOSFETs SS-PWM Simulated Results

The MOSFET model described in Chapter 2 was used in the full bridge resonant circuit shown in Figure 4.2.1 to obtain simulated results. The MOSFET model was paralleled and switched on and off at the same time. The results presented in this section focus on the turn on and turn off conditions since charging and discharging of the parasitic components occurs during these intervals. This section will be presented in twc parts. The first part will describe the ideal case where both MOSFETs in the paralleled combination will turn on and off at the same time. The second section will describe the case where the paralleled MOSFETs will turn on and off at different times due to differing V_{gsth}, g_{fs}, C_{iss}, and drive impedances.

4.4.5.1 Two Paralleled MOSFETs SS-PWM Ideal Case

Figure 4.4.15 shows the turn off condition of parallel combination of MOSFET Q4A and Q4B. When the MOSFETS drive signal begins to discharge to -12V at 140.4 uS a gate-source current will flow through the drive circuit as shown in Figure 4.4.9. The negative current in the plot indicates that these are discharging currents flowing away from the gate-source capacitance C_{gs}. Also, this current is the same magnitude as in the single MOSFET case shown above in Figure 4.3.14. As expected, this implies that the gate power required to drive two MOSFETs will be double that required to drive one MOSFET.

The parallel MOSFET combination turns off at 140.45 uS. Since the load current must be maintained through the resonant inductors LSa and LSb, it will flow through both MOSFETs drain-source, drain-gate, and external snubber capacitances. Also some current will flow through the gate-source capacitances C_{gs}. The drain-source and drain-gate capacitive currents are the same for both MOSFETs in the parallel combination because they have the same capacitive value in the simulation model. However, the total capacitive current flowing through the paralleled MOSFET combination is equivalent to the capacitive current flowing in the single MOSFET case since the resonant load current is the same for both cases. Also, the time the parasitic capacitors are conducting increases from 0.175 uS to 0.325 uS when the MOSFETs are paralleled since the load current is the same and the parasitic capacitance has increased. Current will flow through the parasitic and snubber capacitances of the paralleled combination of MOSFETs Q1 and Q4 until MOSFETs Q1A and Q1B have their drain-source capacitances C_{ds} discharged to - *Vdf*. At 140.75 uS, the anti-parallel body diode D_{ds} of MOSFETs Q1A and Q1B will start to conduct and no significant current will flow through the parasitic capacitances.

Figure 4.4.16 shows the condition when both MOSFETs Q4A and Q4B turn on. At time 144.30 uS the MOSFETs Q1A and Q1B will turn off when their gate-source capacitances C_{gs} are discharged to - *Vgs*. As described above, when the MOSFETs Q1A and Q1B stop conducting through their drain-source channel, the drain-source, drain-gate, and external snubber capacitances of MOSFETs Q1A and Q1B will start to charge, and the drain-source, drain-gate, and external snubber capacitances of

MOSFETs Q4A and Q4B will start to discharge in order to maintain the load current through the resonant load inductors LSa and LSb. When the drain-source capacitances C_{ds} of MOSFETs Q4A and Q4B discharge to - *Vdf* at 144.65 uS, current will flow through the anti-parallel body diodes D_{ds} of MOSFETs Q4A and Q4B. No significant current will flow through the parasitic capacitors when the anti-parallel body diodes D_{ds} are conducting.

Figure 4.4.16 shows that MOSFETs Q4A and Q4B are turned on at 144.8 uS when their gate-source capacitance C_{gs} is charged to + *Vgs*. This will cause currents to flow through the gate-source capacitances C_{gs} and the gate-drain capacitances C_{gd} of MOSFETs Q4A and Q4B.

Figure 4.4.17 shows when MOSFETs Q4A and Q4B are turned off at 140.4 uS, the current flowing through their drain-source conduction channel *(ID(Q4A) + ID(Q4B))*, and the resonant inductor current *(I(LSA))* will be carried first by the parasitic and the external snubber capacitances of MOSFETs Q1A, Q1B and MOSFETs Q4A, Q4B during the interval between 140.5 uS and 140.7 uS. As mentioned above, since the load current is the same as the single MOSFET case, and the parasitic capacitances have increased because of the paralleled combination, it will take more time for the load current to charge and discharge the MOSFETs parasitic capacitances. From 140.70 uS, the current to the load will flow through the anti-parallel body diodes D_{ds} of MOSFETs Q1A and Q1B until they are turned on at 140.95 uS. When MOSFET Q1A and Q1B turn on, all the load current will flow through their drain-source conduction channel. This occurs because the paralleled MOSFET combination will

have a voltage drop across the drain-source region which will not bias their anti-parallel body diodes D_{ds} on. This differs from the single MOSFET case where current was flowing through both the anti-parallel body diode D_{ds} and the MOSFETs drain-source conduction channel.

Figure 4.4.18 shows the condition before MOSFETs Q4A and Q4B turn on. First, the load current will flow through the parasitic and the external snubber capacitors of MOSFETs Q1A, Q1B and MOSFETs Q4A, Q4B when MOSFETs Q1A and Q1B are turned off at 144.3 uS. Current will then flow through the anti-parallel body diodes D_{ds} of MOSFETs Q4A and Q4B until these MOSFETs are turned on by their gate signal at 144.45 uS. At this point current will only flow through the drain-source conduction channels of MOSFETs Q4A and Q4B and not through their anti-parallel body diodes D_{ds}. This occurs because the paralleled MOSFETs effective R_{dson} is low enough so that the voltage generated by the load current will not bias their anti-parallel body diode D_{ds} on. Some current does flow through these diodes because of their reverse recovery interval. In Figure 4.4.18 this happens from 144.9 uS to 145.15 uS.

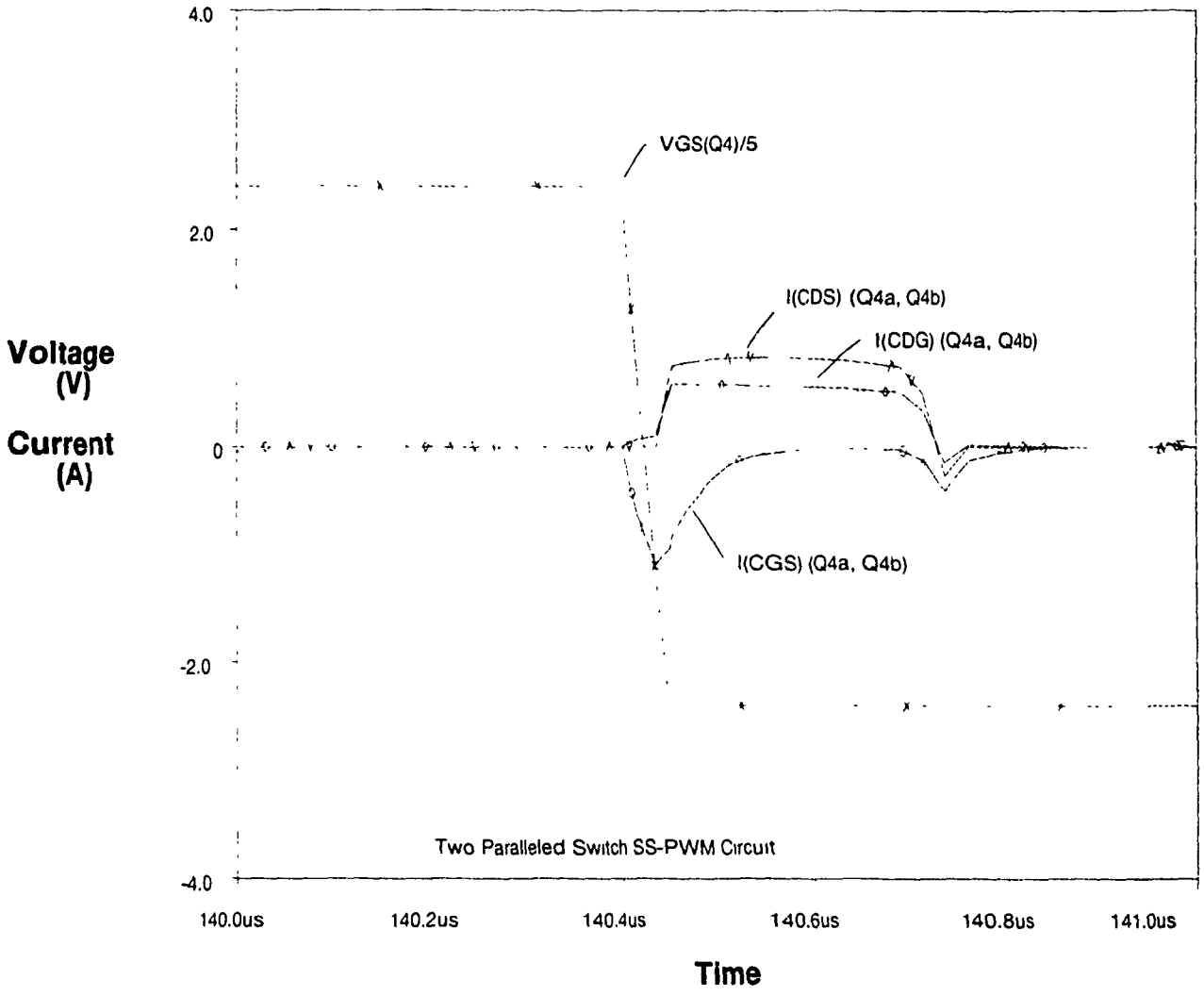


Figure 4.4.15 - SS-PWM MOSFETs Q4a, Q4b Turn Off (No Delay) Parasitic Capacitive Currents

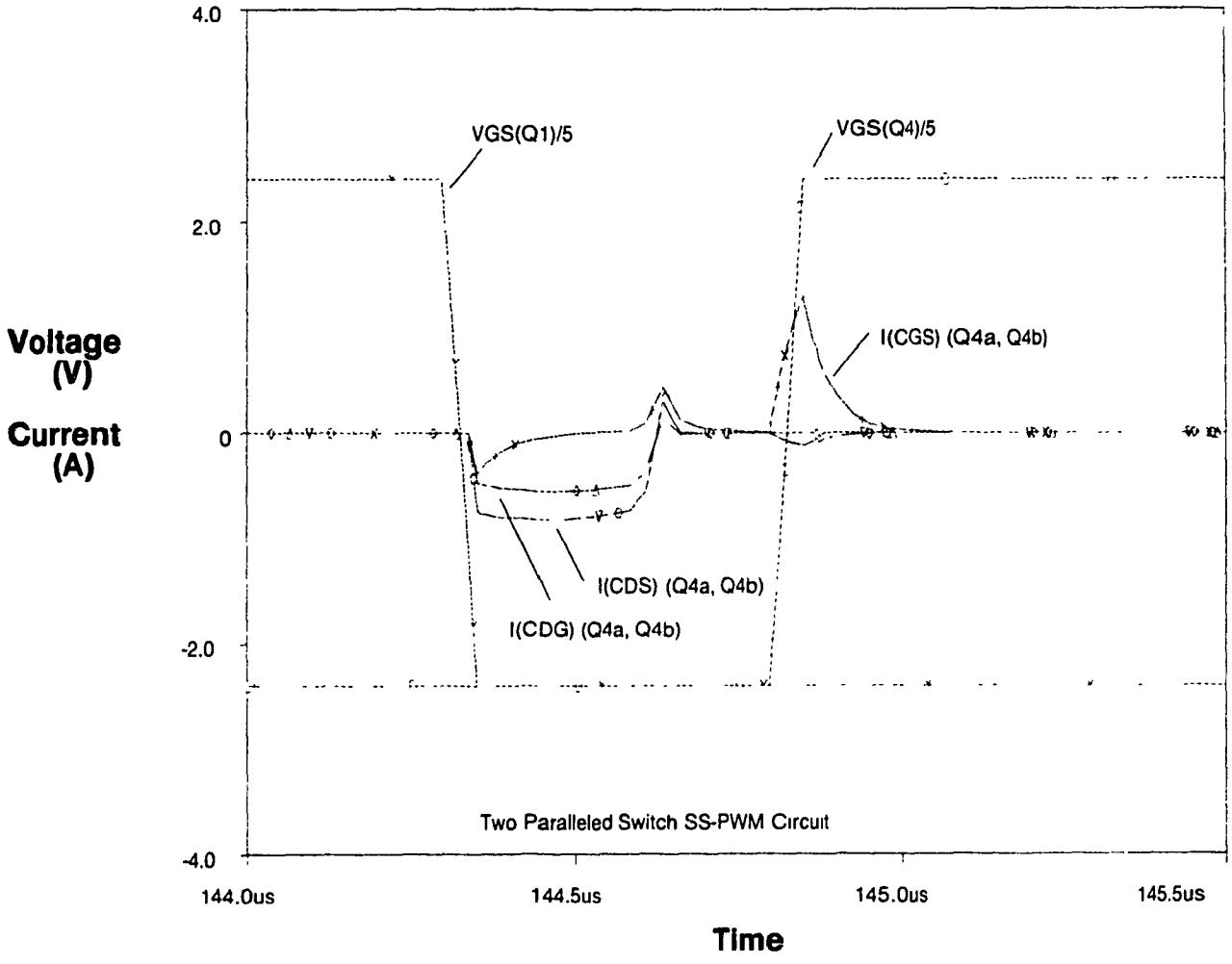


Figure 4.4.16 - SS-PWM MOSFETs Q4a, Q4b Turn On (No Delay) Parasitic Capacitive Currents

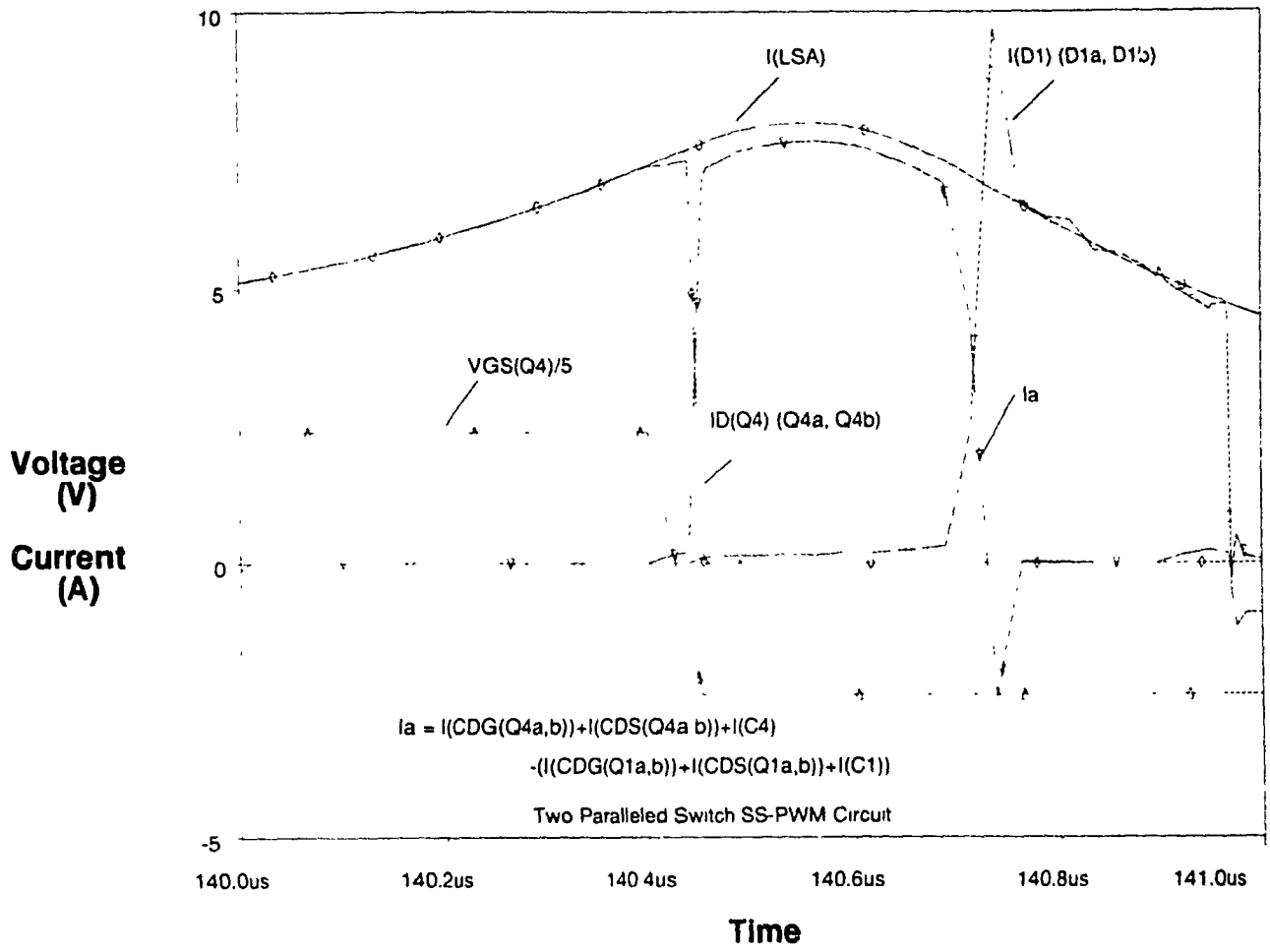


Figure 4.4.17 - SS-PWM MOSFETs Q4a, Q4b Turn Off (No Delay) Capacitive, Drain and Body Diode Currents

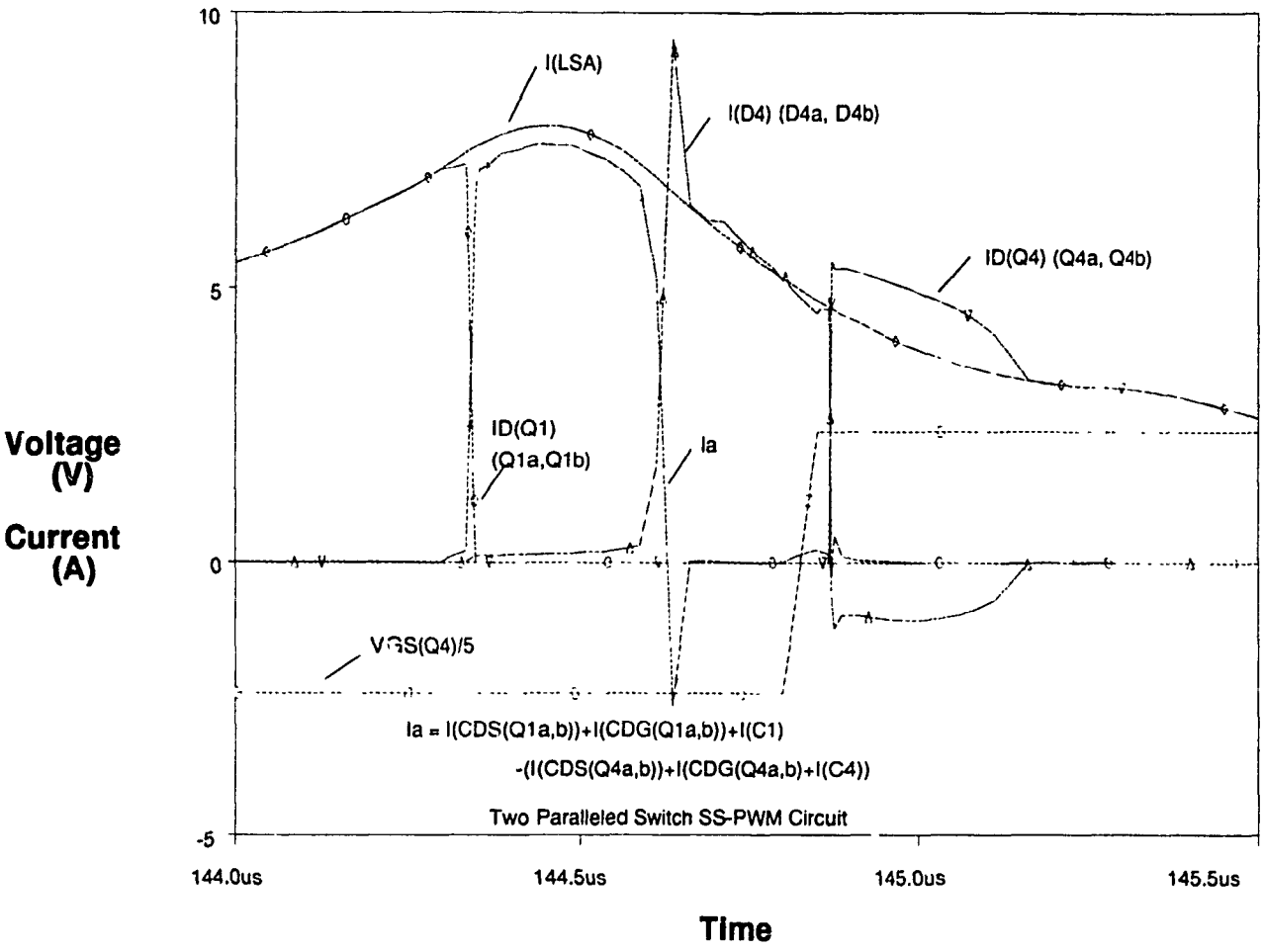


Figure 4.4.18 - SS-PWM MOSFETs Q4a, Q4b Turn On (No Delay) Capacitive, Drain and Body Diode Currents

4.4.5.2 Two Paralleled MOSFETs SS-PWM Non-Ideal Case

The MOSFET model described in Chapter 2 was used in the full bridge resonant circuit shown in Figure 4.2.1 to obtain simulated results. The MOSFET models were paralleled and one was turned on and off 0.250 uS before and after the other MOSFET to emulate the delay caused by the mismatching of g_{fs}, C_{iss}, and V_{gsth} of the MOSFETs in the parallel combination. This delay was implemented by changing the gate-source impedance of each MOSFET so that one MOSFET had less impedance while the other MOSFET had more impedance. This caused the MOSFET with the lower gate-source impedance to turn on and turn off before the other MOSFET. The results presented in this section focus on the turn on and turn off conditions since charging and discharging of the parasitic components occur during these intervals.

Figure 4.4.19 shows the turn off condition of MOSFETs Q4A and Q4B. When the MOSFETs drive signal begins to discharge to -12V at 140.4 uS, a gate-source current will flow through the drive circuit as shown in Figure 4.4.9. The negative current in the plot indicates that this is a discharging current for the gate-source capacitor C_{gs}. In this case MOSFET Q4A will turn off first since its gate-source impedance is smaller than the gate-source impedance of MOSFET Q4B. The parasitic and the external snubber capacitances will not carry any of the load current because the other MOSFET in the paralleled combination Q4B is still turned on and will carry this current. MOSFET Q4A will also keep the voltage across the paralleled combination clamped to the voltage drop

across its drain-source region. This condition is shown in Figure 4.4.10.

The MOSFET Q4A turns off at 140.48 uS. At this point, since both MOSFETs Q4A and Q4B in the paralleled combination are turned off, the load current which must be maintained through the resonant inductors LSa and LSb will flow through their drain-source, drain-gate and the external snubber capacitances. Also, some of this current will flow through the gate-source capacitances C_{gs}. This interval corresponds to the current flows shown in Figures 4.4.11.

Figure 4.4.20 shows the condition when MOSFETs Q4A and Q4B are turned on. At time 144.30 uS the MOSFETs Q1A and Q1B will turn off by charging their gate-source capacitance C_{gs} to - *Vgs*. As described above, when both MOSFETs Q1A and Q1B stop conducting through their drain-source channel, the drain-source and drain-gate capacitances of MOSFETs Q1A and Q1B will start to charge and the drain-source and drain-gate capacitances of MOSFETs Q4A and Q4B will start to discharge in order to maintain the load current through inductors LSa and LSb. This condition corresponds to Figure 4.4.13. When the drain-source capacitances C_{ds} discharge to - *Vdf* at 144.65 uS, current will flow through the anti-parallel body diodes D_{ds} of MOSFETs Q4A and Q4B as shown in Figure 4.4.14. Since these diodes are turned on by the voltage applied across them they will be unaffected by the delayed gate-source signal. No significant currents will flow through the parasitic capacitors when the anti-parallel body diode D_{ds} is conducting.

The MOSFET Q4A is turned on at 144.8 uS when its gate-source capacitance C_{gs} is charged to + *VGSth1* as shown in Figure 4.4.2. When the gate-source voltage is first applied to the paralleled MOSFET combination, a current flow through the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} of both MOSFETs Q4A and Q4B. This condition is shown in Figure 4.4.2. The gate-source capacitance C_{gs} current is different for MOSFETs Q4A and Q4B because of the different gate-source impedance which was used in the simulation.

Figure 4.4.21 shows when MOSFETs Q4A and Q4B are turned off at 140.4 uS, the current flowing through their drain-source conduction channel *(ID(Q4A) + ID(Q4B))* and the resonant inductor current *(I(LSA))* will be carried first by the parasitic and the external snubber capacitances of MOSFETs Q1A, Q1B and MOSFETs Q4A, Q4B during the interval between 140.45 uS and 140.75 uS. From 140.75 uS, the current to the load will flow through the anti-parallel body diodes D_{ds} of MOSFETs Q1A and Q1B until they are turned on at 140.95 uS. Also, at 140.48 uS there is a negative transition in the total MOSFET current *(ID(Q4A) + ID(Q4B))* when MOSFET Q4A turns off first and MOSFET Q4B is forced to carry the full current. This transition does not affect the load current *(I(LSA))*.

Figure 4.4.22 shows the condition before MOSFETs Q4A and Q4B are turned on. First, current will flow through the parasitic and the external snubber capacitors of MOSFETs Q1A, Q1B and MOSFETs Q4A, Q4B when MOSFETs Q1A, and Q1B are turned off at 144.3 uS. Current will the flow through the anti-parallel body diode D_{ds} of MOSFET Q4A and Q4B

until one MOSFET turns on. This condition is shown in Figure 4.4.14. MOSFET Q4A will turn on at 144.85 uS and current will flow through both the anti-parallel body diodes D_{ds} of MOSFETs Q4A and Q4B, and the drain-source conduction channel of MOSFET Q4A as shown in Figure 4.4.3. The current flowing through the MOSFET Q4A will be from the source to the drain as shown in Figure 4.4.3 since it is negative. When MOSFET Q4B finally turns on at 144.9 uS, it will lower the effective R_{dson} of the paralleled MOSFET combination and all the load current will flow through the MOSFETS drain-source conduction channel as shown in Figure 4.4.5. If the load current is large, then both the MOSFETs drain-source conduction channels and anti-parallel body diodes D_{ds} will conduct. As the resonant current decreases, current will first decrease to zero in the anti-parallel body diode D_{ds}, and then decrease to zero in the drain-source conduction channel of the MOSFET before it reverses and flows from the drain to the source.

Figure 4.4.23 shows how load current is transferred from MOSFETs Q4A to Q4B when they are turned off at 140.45 uS. The current is shared equally until this point where it decreases to zero for MOSFET Q4A and doubles for MOSFET Q4B. Figure 4.4.23 also shows how load current is transferred from MOSFET Q1A to Q1B they are turned on at 140.8 uS. This case is more complicated since current is also flowing through the MOSFETs anti-parallel body diodes D_{ds}. Load current is first carried equally by both anti-parallel body diodes. When MOSFET Q1A turns on at 140.9 uS, it will carry a portion of the load current while the anti-parallel diodes carry the rest. When MOSFET Q1B turns on at 141.0 uS,

the anti-parallel body diode will stop conducting and the load current will be carried equally by the MOSFETs in the parallel combination.

Figure 4.4.24 shows how MOSFETs Q1A and Q1B transfer current when they are turned off. This transition is the same as described in the paragraph above when MOSFETs Q4A and Q4B were turned off. Figure 4.4.24 also shows how MOSFETs Q4A and Q4B transfer current when they are turned on. This transition is the same as described in the paragraph above when MOSFETs Q1A and Q1B are turned on.

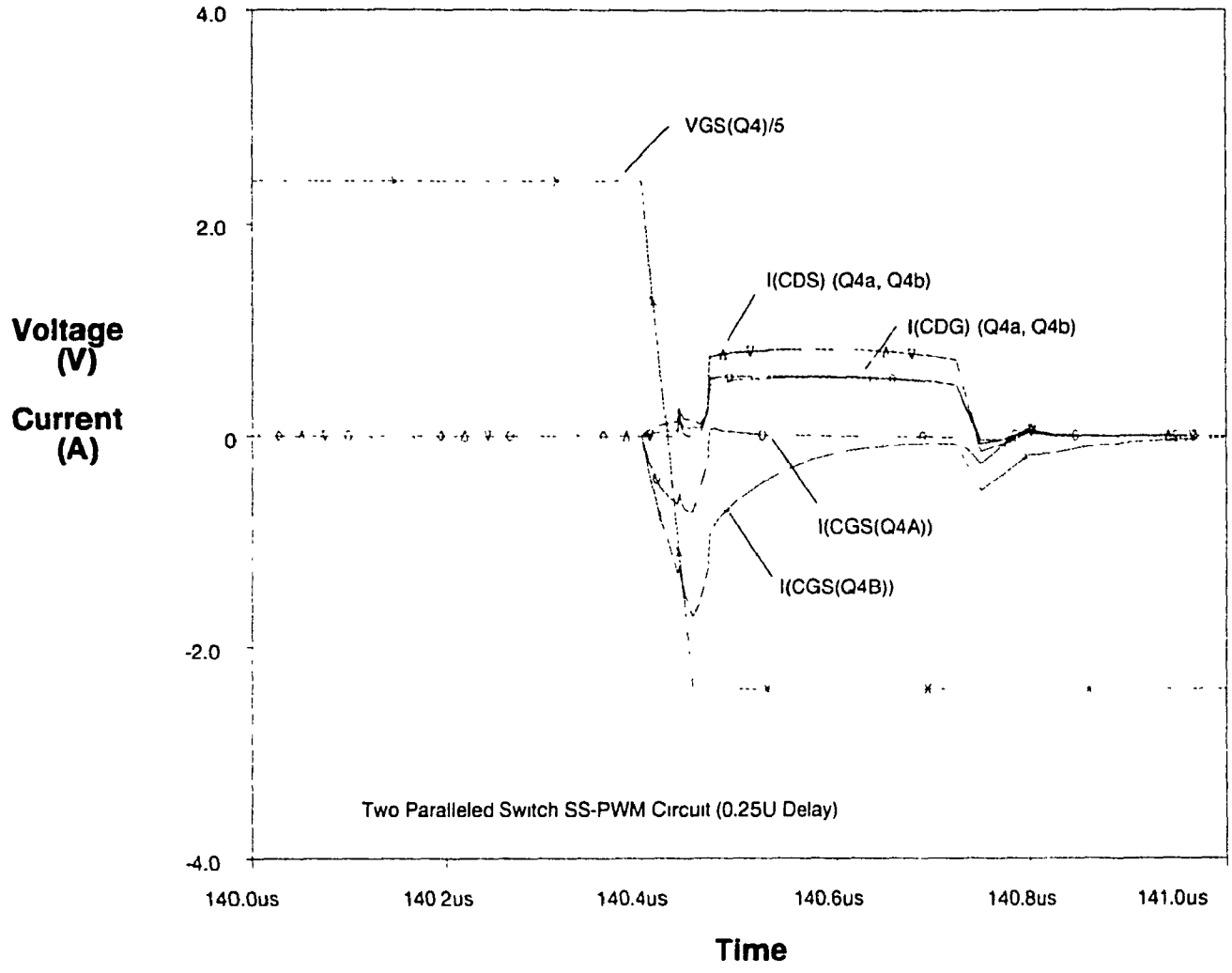


Figure 4.4.19 - SS-PWM MOSFETs Q4a, Q4b Turn Off (250 nS Delay) Parasitic Capacitive Currents

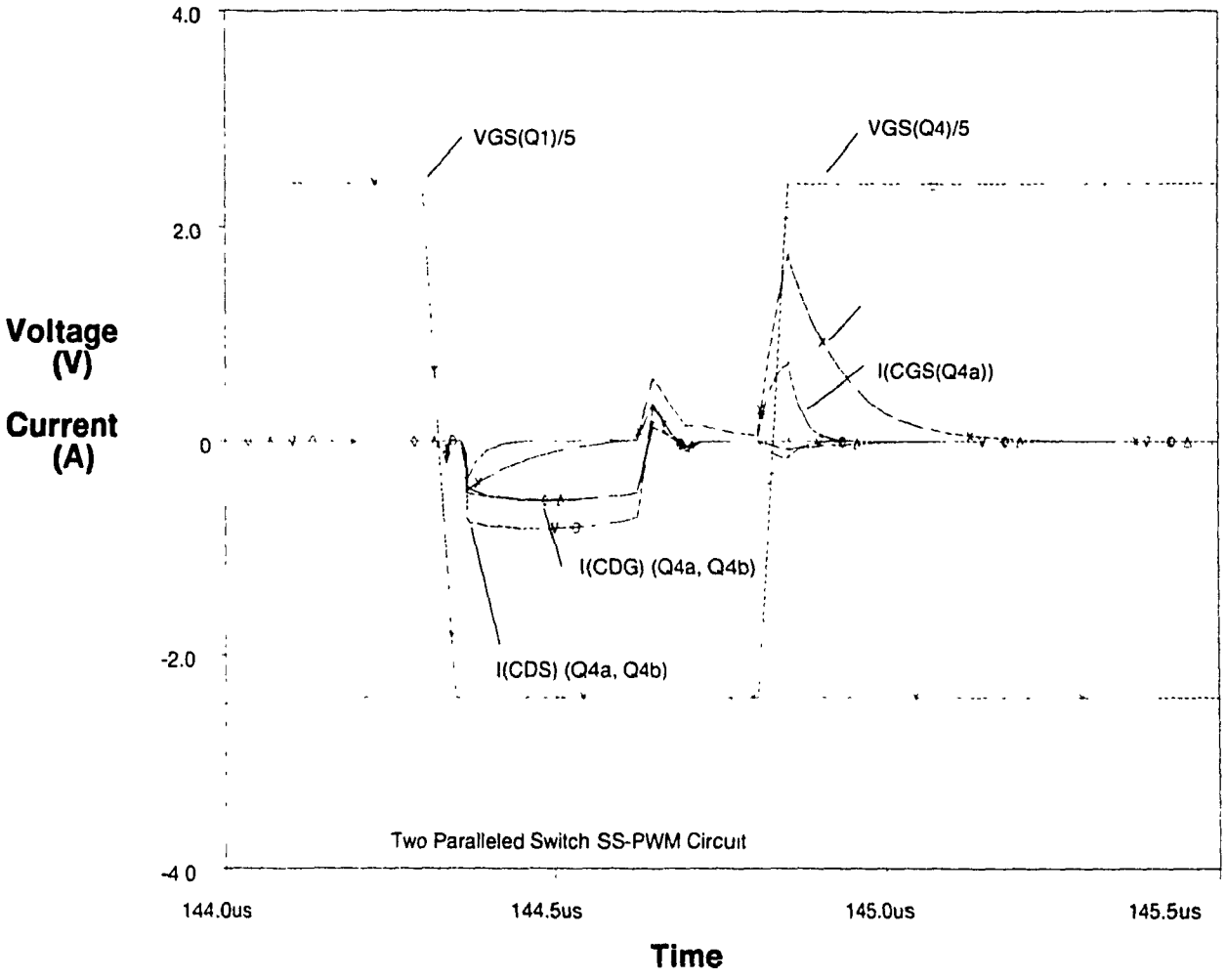


Figure 4.4.20 - SS-PWM MOSFETs Q4a, Q4b Turn On (250 nS Delay) Parasitic Capacitive Currents

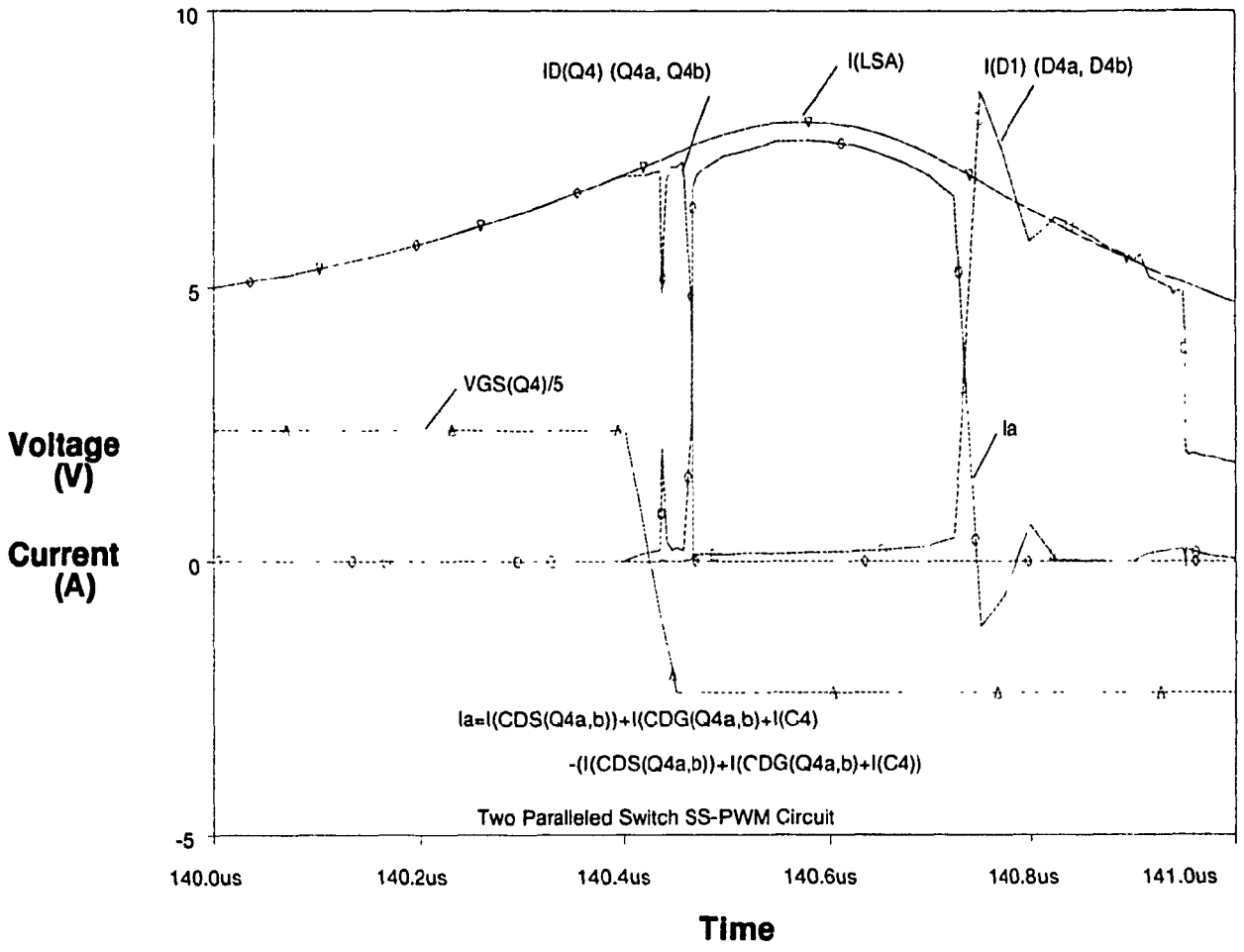


Figure 4.4.21 - SS-PWM MOSFETs Q4a, Q4b Turn Off (250 nS Delay) Capacitive, Drain and Body Diode Currents

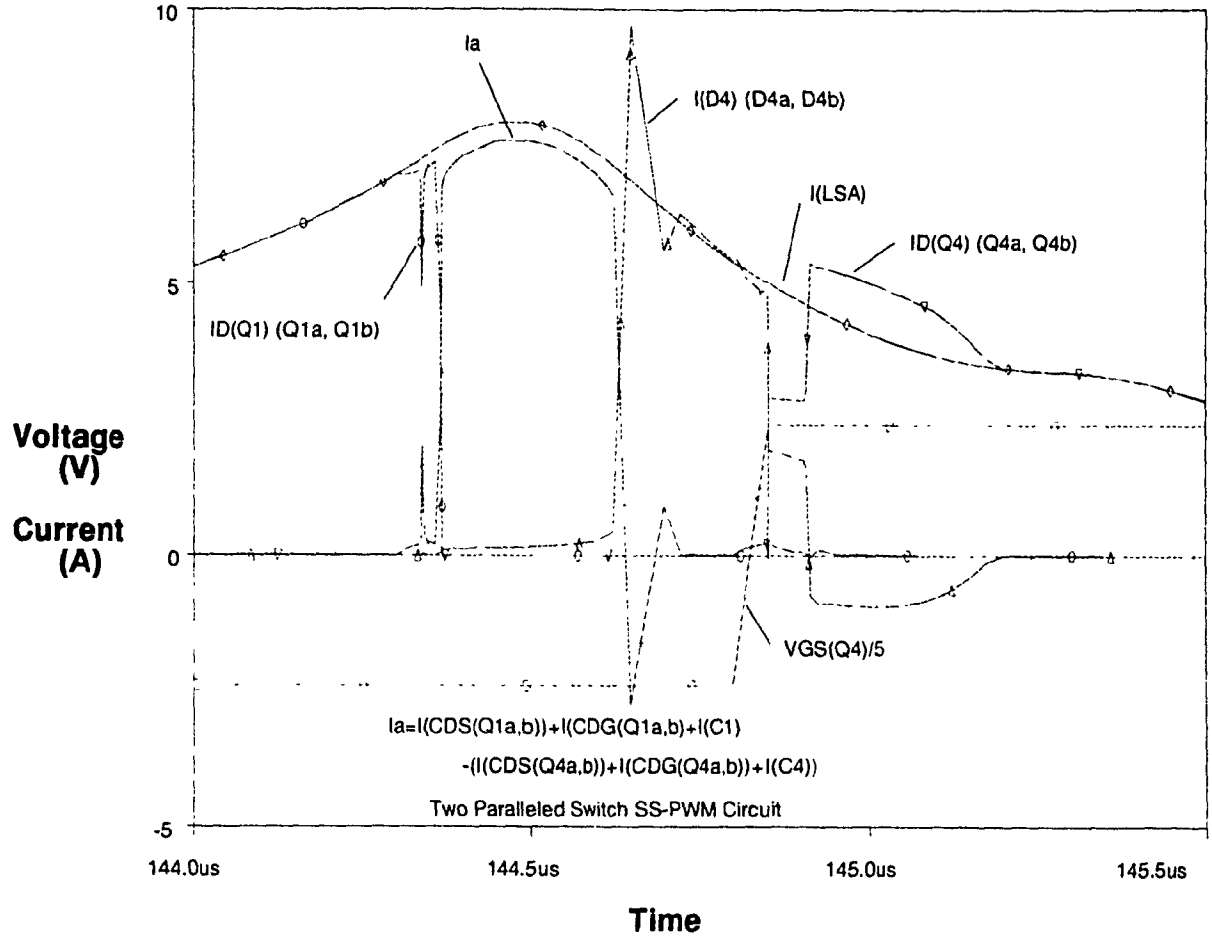


Figure 4.4.22 - SS-PWM MOSFETs Q4a, Q4b Turn On (250 nS Delay) Capacitive, Drain and Body Diode Currents

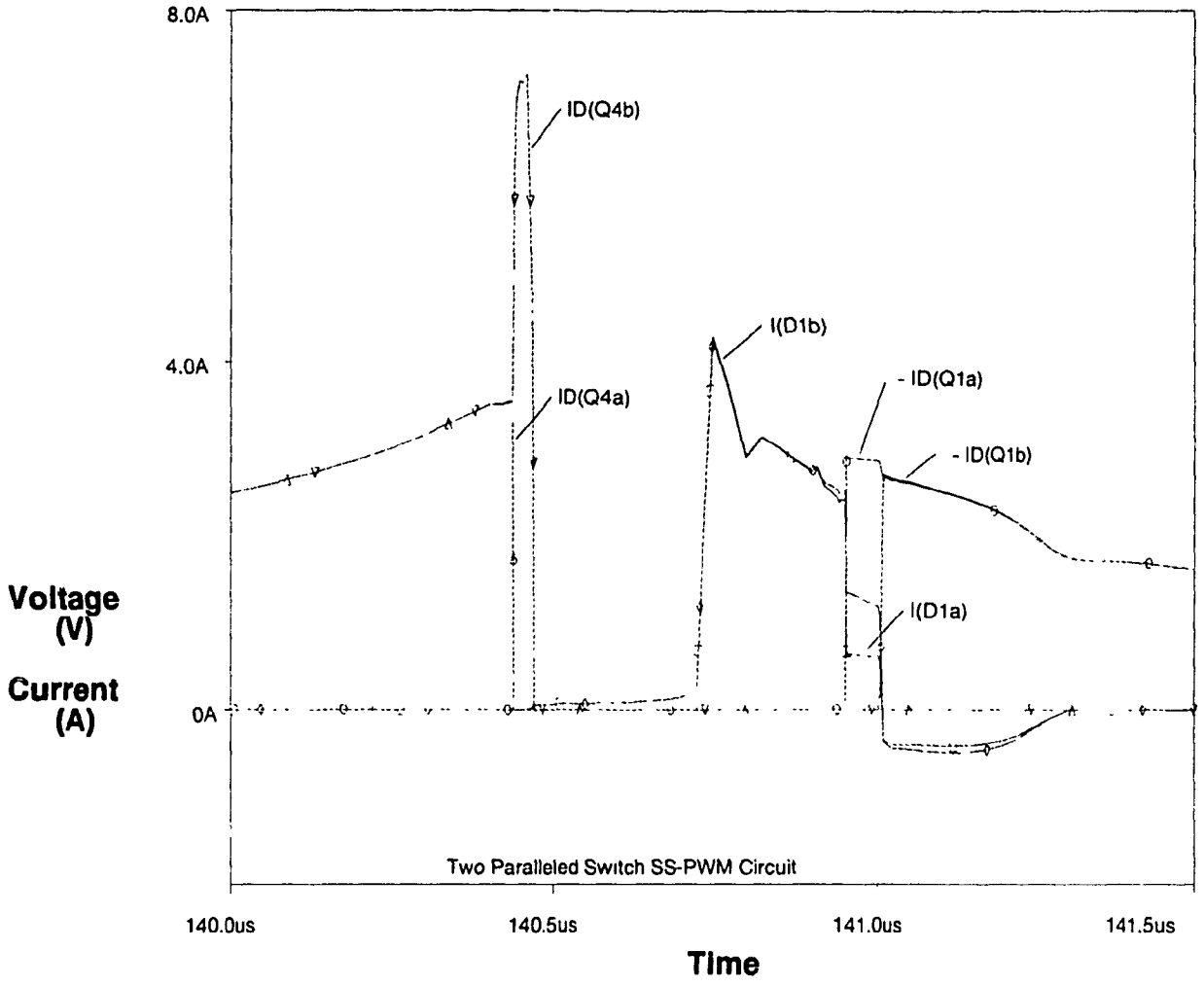


Figure 4.4.23 - SS-PWM MOSFETs Q4a, Q4b Turn Off (250 nS Delay) Drain and Body Diode Currents

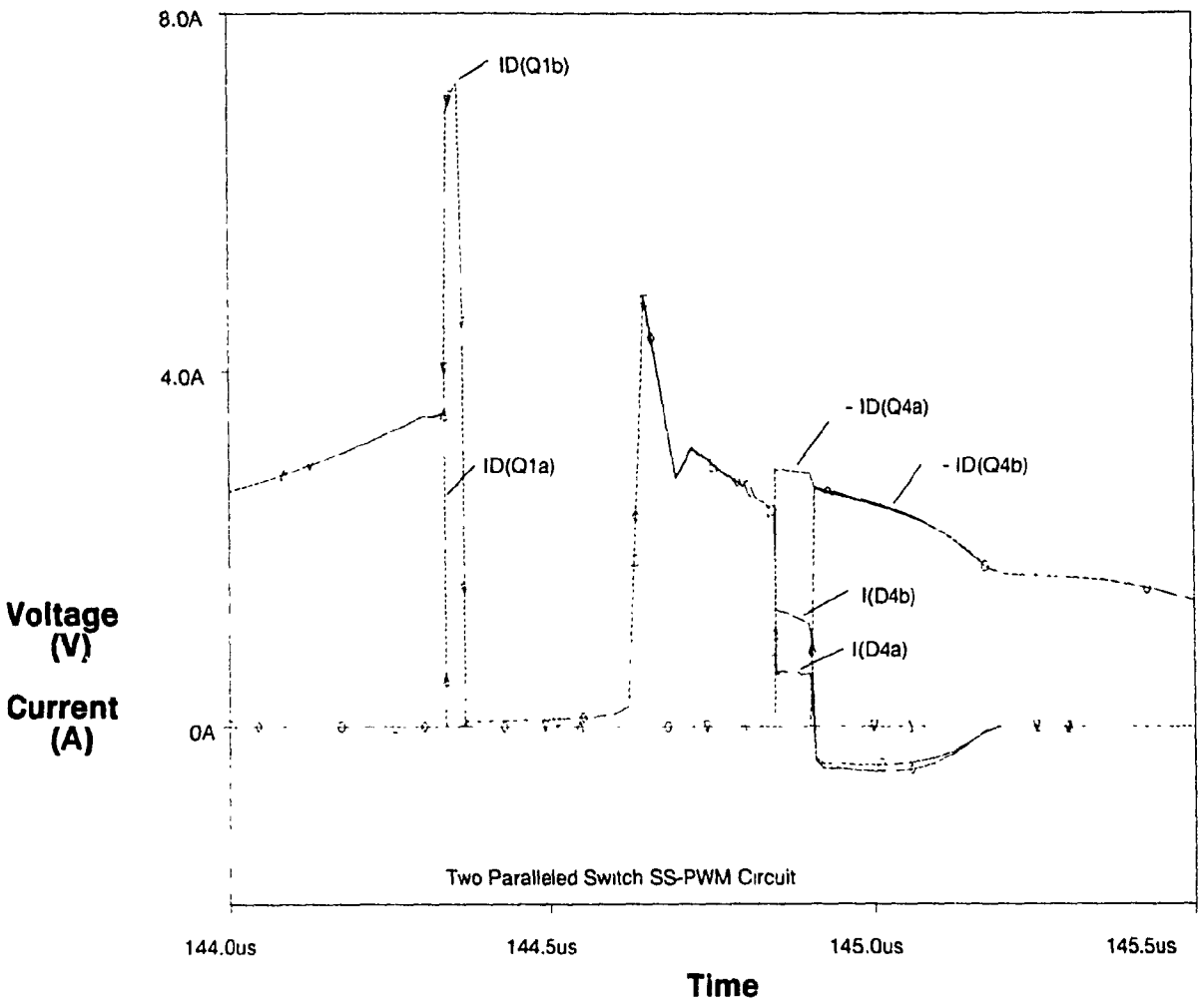


Figure 4.4.24 - SS-PWM MOSFET Q4a, Q4b Turn On (250 nS Delay) Drain and Body Diode Currents

4.4.6 Two Paralleled MOSFETs SS-PWM Experimental Results

Experimental results were obtained when the SS-PWM circuit shown in Figure 4.2.1 was connected with two MOSFETs connected in parallel. The experimental results obtained along with the simulated results are shown in Table 4.4.1. Simulated results were obtained by using the PSPICE program to simulate the circuit using the MOSFET model described in Chapter 2. The PROBE sub-program of PSPICE was used to graph the waveforms and mathematically generate loss plots which were then read from the graph by the cursor function. The experimental results were obtained by measuring the input power to the bridge and subtracting the output power of the diode filter. The losses of the transformer, diodes, and filter inductor were estimated and subtracted from the final loss result as described in section 4.3.6. Table 4.4.1 shows a comparison of the experimental and simulated results.

Table 4.4.1 Comparison of Experimental, and Simulated Losses for Paralleled SS-PWM MOSFETs

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
1	15.64 W	47.82 W	15,64 W
2	11.15 W	43.42 W	11.24 W

A time delay was simulated to see the effects on the losses when two MOSFETs were used in parallel. This delay was implemented experimentally by varying the gate drive resistors of both MOSFETs of the parallel combination while observing their gate-source voltage V_{gs}. The results are given in Table 4.4.2 for delay times of 250 nS and 500 nS. and compared with the no (minimal) delay case mentioned above.

Table 4.4.2 Comparison of Experimental, and Simulated Losses for Paralleled SS-PWM MOSFETs with Switching Delays

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
0 nS	11.15 W	43.42 W	11.24 W
250 nS	11.76 W	44.22 W	12.04 W
500 nS	12.02 W	45.42 W	13 24 W

4.4.7 Summary of Losses for Two Paralleled MOSFETs SS-PWM Topology

From the results obtained is this section it is seen that paralleling MOSFETs will decrease the conduction losses because of the decrease of the effective R_{dson}. Switching losses however will increase because the parasitic capacitances C_{gs} and C_{gd} will also increase requiring more gate drive power to turn the devices on and off. This is the same as in the case when MOSFETs in HS-PWM circuits are paralleled.

The increase in the drain-source capacitances will have no effect on losses because the load circuit will discharge them before the MOSFETs are turned on. Also, as mentioned above, since it is unlikely that both MOSFETs will turn on and off at the same time, there will exist a period of time when only one MOSFET is conducting. During this period it will seem as if only one MOSFET is used and the conduction losses will be the same as in the single MOSFET case.

As switching frequencies are increased, the drive power required to charge and discharge the parasitic capacitances will also increase. Also, the time period when only one MOSFET conducts will become more significant with respect to the on time of the MOSFET. This means that the savings obtained by paralleling MOSFETs will decrease as switching frequency increases. Since SS-PWM minimizes switching losses, higher switching frequencies are used. This makes the delay time more significant with respect to the on time of the MOSFETs. As the delay time becomes more significant the gains obtained in efficiency by paralleling MOSFETs are minimized.

From the experimental result it is seen that as more MOSFETs are added in parallel, the overall losses decrease. The losses are not halved when two MOSFETs are used in parallel because losses are incurred when the gate-drain capacitance C_{gd}, and the gate-source capacitance C_{gs} are charged and discharged during switching.

When the MOSFETs within the paralleled combination were delayed the losses increased due to the fact that one MOSFET had more conduction losses.

4.5 Three Paralleled MOSFETs SS-PWM Simulated and Experimental Results

The case where three MOSFETs are paralleled for a single switching element was studied and found to be similar to the two paralleled MOSFET case. In order to prevent a repeat of section 4.4, only a summary of the differences observed between the two cases will be presented in this section.

When three MOSFETs were paralleled, the parasitic capacitances C_{ds}, C_{gd} and C_{gs} were effectively placed in parallel and resulted in a switching element which had three times the parasitic capacitances of the single MOSFET case. This resulted in more drive power required to switch the MOSFETs on and off. Also, for a given load current, it will take longer for the MOSFETs drain-source and gate-drain capacitance, C_{ds} and C_{dg} respectively, to discharge. This will decrease the effective duty cycle of the converter and may cause switching losses if the external snubber capacitors are not decreased. Also, when three MOSFETs are paralleled the effective R_{dson} will be one third that of the single MOSFET case.

As in the two paralleled MOSFET case, the MOSFET which turn on first will carry the full load current. The load current will be shared when the other MOSFETs turn on in the steady state condition. Also, the MOSFET which turns off last will conduct the full load current. Care must be taken to ensure that the MOSFETs in the configuration can handle the full load current for the brief time when only one device is conducting. The differences in conduction times of the MOSFETs will increase the effective R_{dson} to a value greater than one third the value observed in the single MOSFET case. In order to make the conduction times similar it is necessary to match the MOSFETs input capacitance C_{iss}, gate-source threshold voltage V_{gsth}, and transconductance g_{fs}.

4.5.1 Three Paralleled MOSFETs SS-PWM Simulated Results

The MOSFET model described in Chapter 2 was used in the full bridge resonant circuit shown in Figure 4.2.1 to obtain simulated results. The MOSFET model was paralleled so that a switching element consisted of three MOSFETs. These MOSFETs where switched on and off at the same time. The results presented in this section focus on the turn on and turn off conditions since charging and discharging of the parasitic components occurs during these intervals.

Figure 4.5.1 shows the turn off condition of the parallel combination of MOSFET Q4A, Q4B and Q4C. When the MOSFETs drive signal begins to discharge to - 12V at 140.4 uS, a gate-source current will flow through the drive circuits. The negative current in the plot

indicates that these are discharging currents flowing away from the gate-source capacitance C_{gs}. Also, this current is the same magnitude as in the single MOSFET case shown above in Figure 4.3.14. As expected, this implies that the gate power required to drive three MOSFETs will be triple that required to drive one MOSFET.

The three parallel MOSFET combination turns on at 140.45 uS. Since the load current must be maintained through the resonant inductors LSa and LSb, it will flow through all the MOSFETs drain-source, drain-gate, and the external snubber capacitances. Also some current will flow through the gate-source capacitances C_{gs}. The drain-source and drain-gate capacitive currents are the same for all three MOSFETs in the parallel combination because they have the same gate-source capacitance C_{gs} and gate-source impedance value in the simulation model. However, the total capacitive current flowing through the paralleled MOSFET combination is equivalent to the capacitive current flowing in the single MOSFET case since the resonant load current is the same for both cases. Also, the time the parasitic capacitors are conducting increases from 0.175 uS to 0.450 uS when the MOSFETs are paralleled since the load current is the same and the parasitic capacitances have increased. Current will flow through the parasitic and the external snubber capacitances of the paralleled combination of MOSFETs Q1 and Q4 until MOSFETs Q1A, Q1B and Q1C have their drain-source capacitances C_{ds} discharged to - *Vdf*. At this point, 140.85 uS, the anti-parallel body diode D_{ds} of MOSFETs Q1A, Q1B and Q1C will start to conduct and no significant current will flow through the parasitic capacitances.

Figure 4.5.2 shows the condition when the paralleled MOSFETs Q4A, Q4B and Q4C turn on. At time 144.30 uS the MOSFETs Q1A, Q1B and Q1C will turn off when their gate-source capacitances C_{gs} are discharged to - *Vgs*. As described above, when the MOSFETs Q1A, Q1B and Q1C stop conducting through their drain-source channel, the drain-source, drain-gate, and the external snubber capacitances of MOSFETs Q1A, Q1B, and Q1C will start to charge, and the drain-source, drain-gate, and the external snubber capacitances of MOSFETs Q4A, Q4B and Q4C will start to discharge in order to maintain the load current through the resonant load inductors LSa and LSb. When the drain-source capacitances C_{ds} of MOSFETs Q4A, Q4B and Q4C discharge to - *Vdf* at 144.75 uS, current will flow through the anti-parallel body diodes D_{ds} of MOSFETs Q4A, Q4B and Q4C. No significant current will flow through the parasitic capacitors when the anti-parallel diodes D_{ds} are conducting. Figure 4.5.2 shows that MOSFETs Q4A, Q4B, and Q4C are turned on at 144.8 uS when their gate-source capacitance C_{gs} is charged to + *Vgs*. This will cause currents to flow through the gate-source capacitances C_{gs} and the gate-drain capacitances C_{gd} of MOSFETs Q4A, Q4B, and Q4C.

Figure 4.5.3 shows when MOSFETs Q4A, Q4B and Q4C are turned off at 140.4 uS, the current flowing through their drain-source conduction channel *(ID(Q4A) + ID(Q4B) + ID(Q4C))*, and the resonant inductor current *(I(LSA))* will be carried first by the parasitic and the external snubber capacitances of MOSFETs Q1A, Q1B, Q1C and MOSFETs Q4A, Q4B, Q4C during the interval between 140.5 uS and 140.85 uS. As mentioned above, since the load current is the same as the single MOSFET case, and since the parasitic capacitances have increased because of the paralleled

combination, it will take more time to charge and discharge the MOSFETs parasitic capacitances. From 140.85 uS, the current to the load will flow through the anti-parallel body diodes D_{ds} of MOSFETs Q1A, Q1B and Q1C until they are turned on at 140.95 uS. When MOSFET Q1A Q1B Q1C turn on, all the load current will flow through their drain-source conduction channel. This happens because the three paralleled MOSFET combination will have a voltage drop across the drain-source region which will not bias their anti-parallel body diodes D_{ds} on. This differs from the single MOSFET case where current was flowing through both the anti-parallel body diode D_{ds} and the MOSFETs drain-source conduction channel.

Figure 4.5.4 shows the condition before MOSFETs Q4A, Q4B and Q4C turn on. First, the load current will flow through the parasitic and the external snubber capacitors of MOSFETs Q1A, Q1B, Q1C and MOSFETs Q4A, Q4B, Q4C when MOSFETs Q1A, Q1B and Q1C are turned off at 144.3 uS. Current will then flow through the anti-parallel body diodes D_{ds} of MOSFETs Q4A, Q4B and Q4C until these MOSFETs are turned on by their gate signal at 144.85 uS. At this point current will only flow through the drain-source conduction channels of MOSFETs Q4A, Q4B and Q4C and not through their anti-parallel body diodes D_{ds}. This happens because the paralleled MOSFETs effective R_{dson} is low enough so that the voltage generated by the load current will not bias their anti-parallel body diode D_{ds} on. Some current does flow through these diodes because of their reverse recovery interval. In Figure 4.5.4 this happens from 144.85 uS to 145.00 uS.

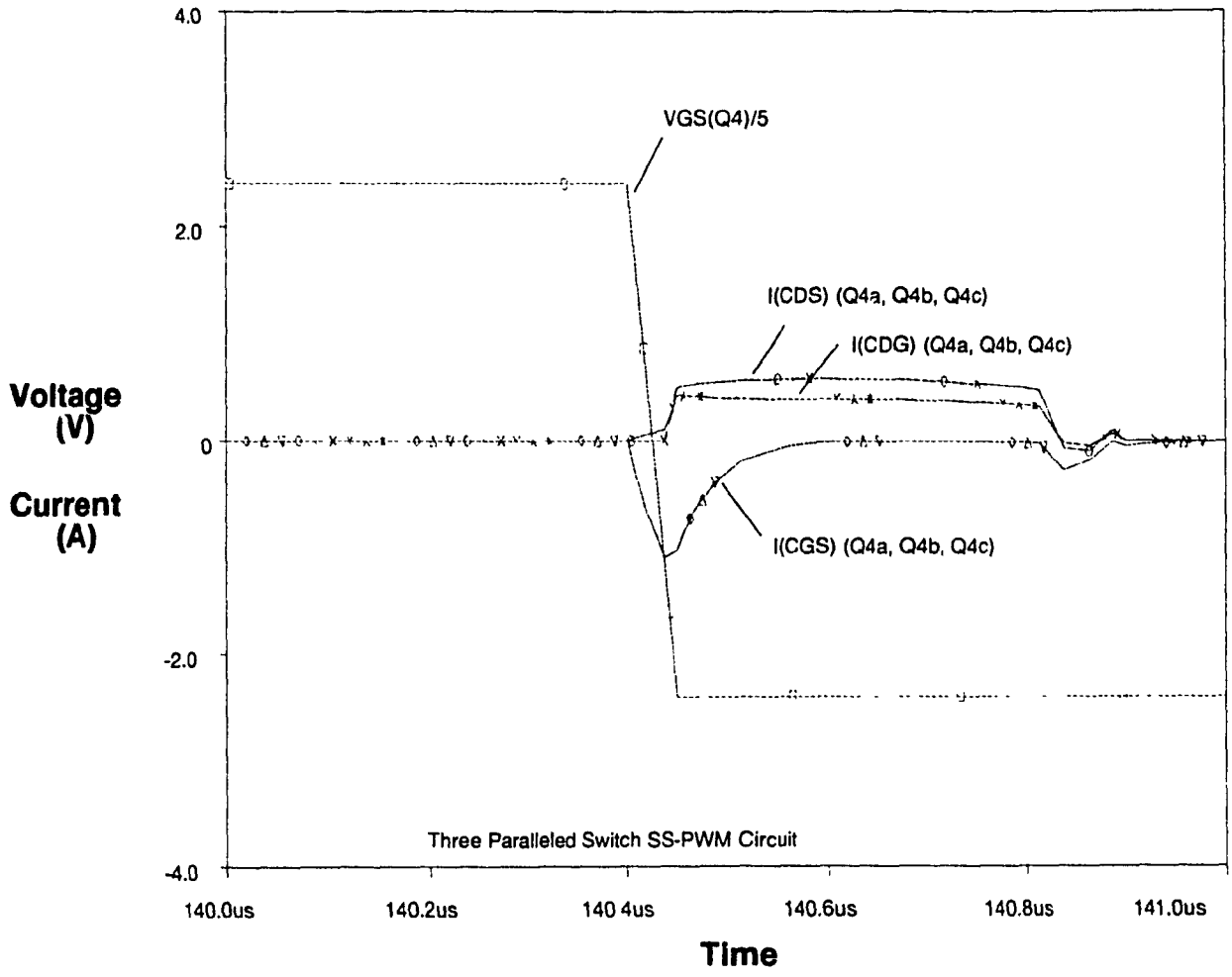


Figure 4.5.1 - SS-PWM MOSFETs Q4a, Q4b, Q4c Turn Off (No Delay) Parasitic Capacitive Currents

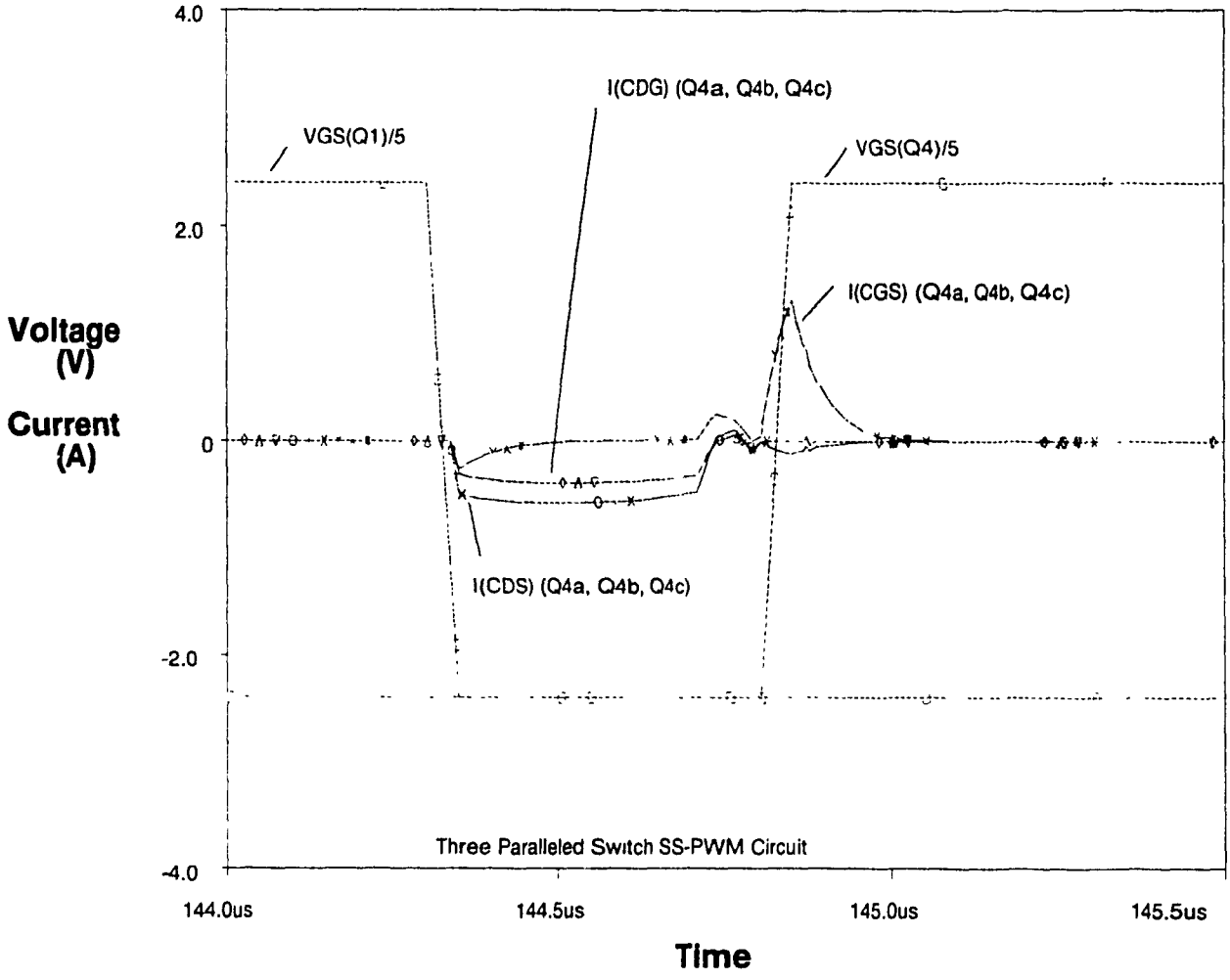


Figure 4.5.2 - SS-PWM MOSFETs Q4a, Q4b, Q4c Turn On (No Delay) Parasitic Capacitive Currents

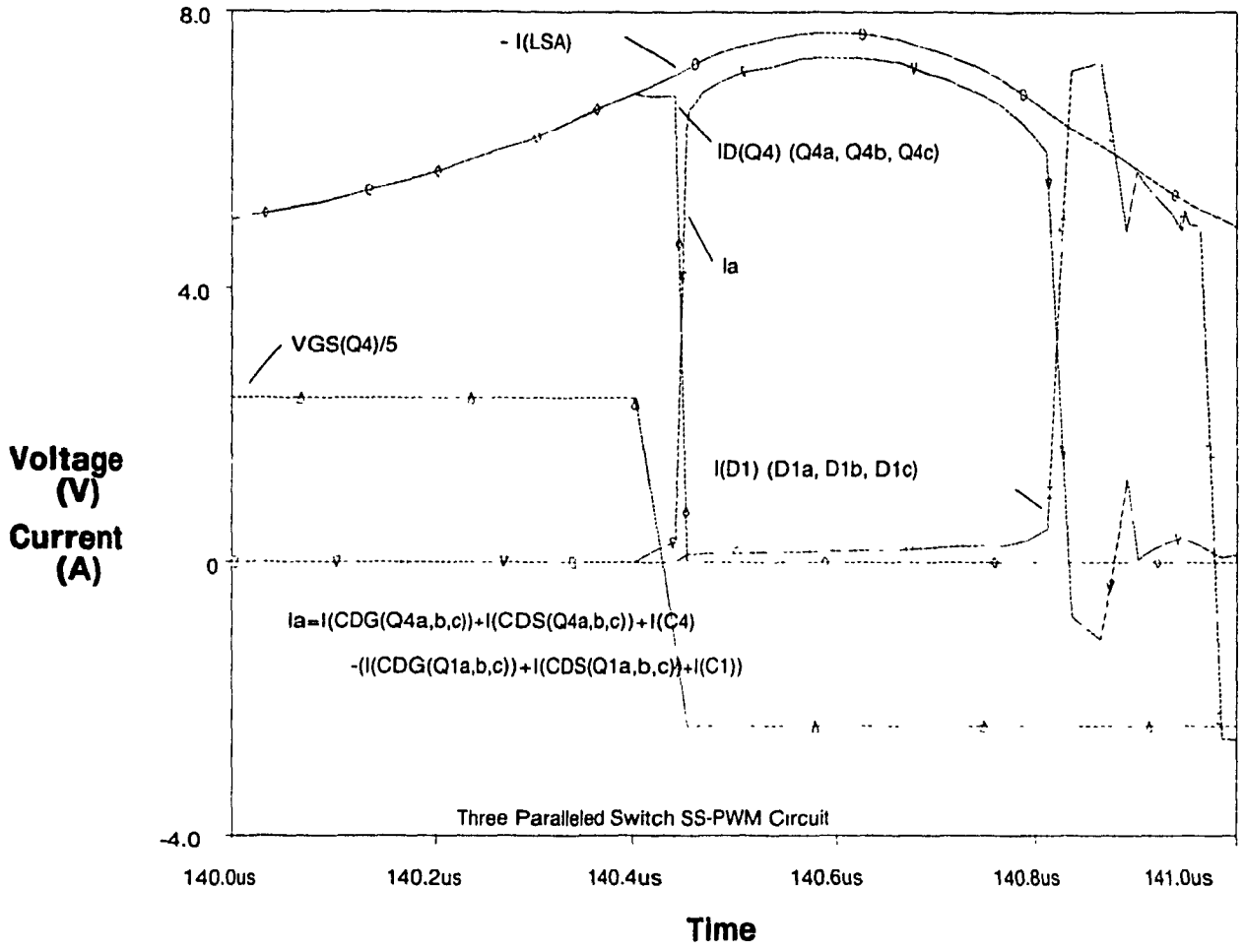


Figure 4.5.3 - SS-PWM MOSFETs Q4a, Q4b, Q4c Turn Off (No Delay) Capacitive, Drain and Body Diode Currents

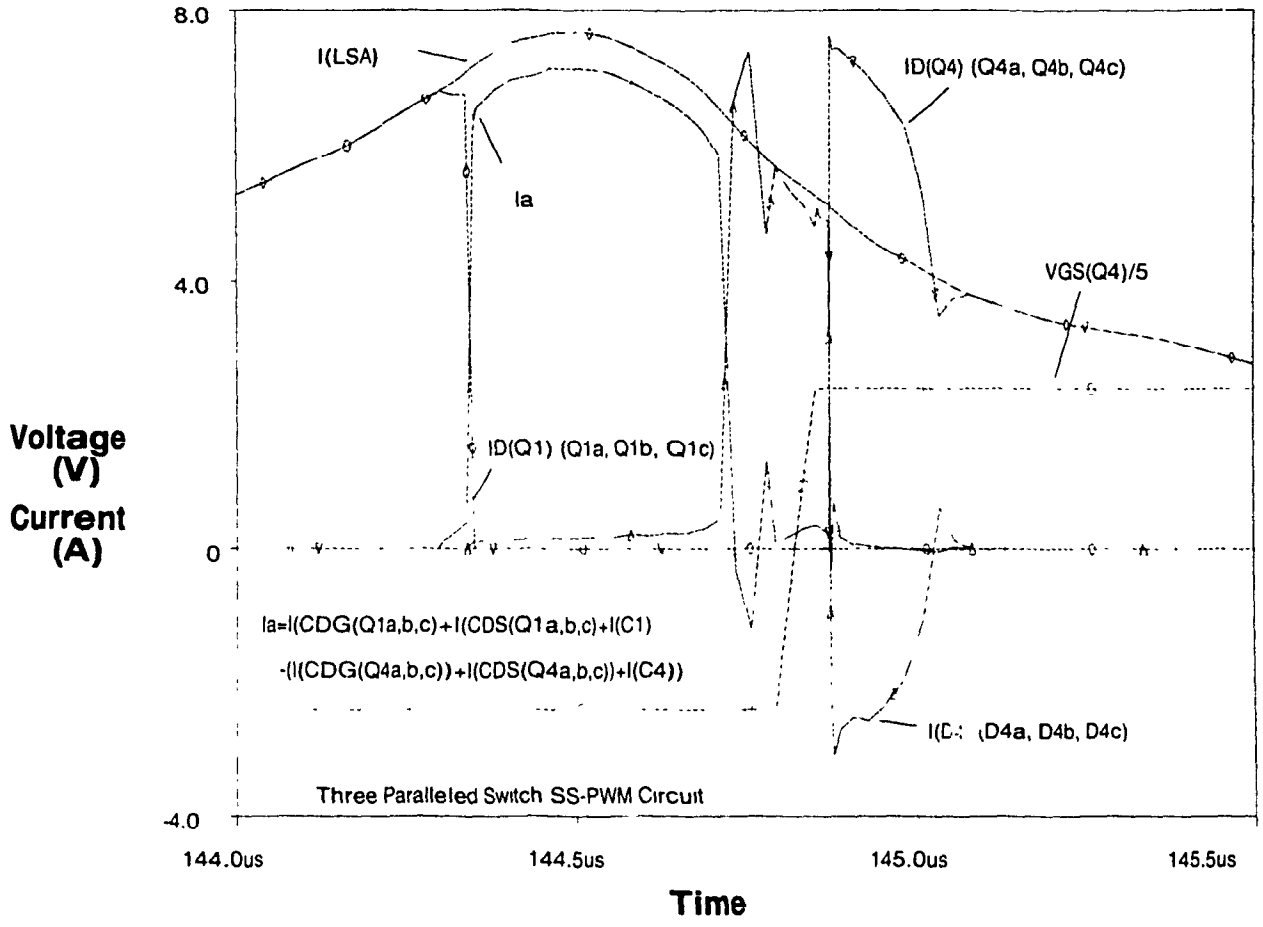


Figure 4.5.4 - SS-PWM MOSFETs Q4a, Q4b, Q4c Turn On (No Delay) Capacitive, Drain and Body Diode Currents

4.5.2 Three Paralleled MOSFETs SS-PWM Experimental Results

Experimental results were obtained when the SS-PWM circuit shown in Figure 4.2.1 was connected with three MOSFETs connected in parallel. The experimental results obtained along with the simulated results are shown in Table 4.5.1. Simulated results were obtained by using the PSPICE program to simulate the circuit using the MOSFET model described in Chapter 2. The PROBE sub-program of PSPICE was used to graph the waveforms and mathematically generate loss plots which were then read from the graph by the cursor function. The experimental results were obtained by measuring the input power to the bridge and subtracting the output power of the diode filter. The losses of the transformer, diodes, and filter inductor were estimated and subtracted from the final loss result as described in section 4.3.6. Table 4.5.1 shows a comparison of the experimental and simulated results.

Table 4.5.1 Comparison of Experimental, and Simulated Losses for Three Paralleled SS-PWM MOSFETs

Number of MOSFETs	Simulated Losses (MOSFETS)	Experimental Losses (Total)	Experimental Losses (MOSFETS)
1	15.64 W	47.82 W	15.64 W
2	11.15 W	43.42 W	11.24 W
3	10.47 W	41.82 W	9.64 W

The total MOSFET losss when they were connected in paralleled for both the simulated and experimental cases were plotted for comparison and shown in Figure 4.5.5.

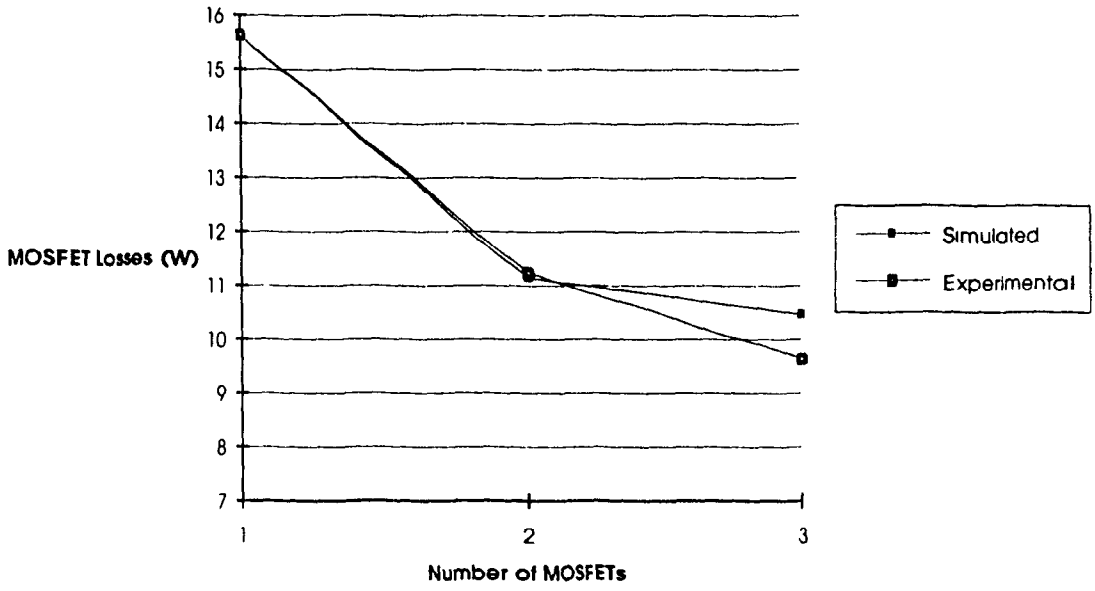


Figure 4.5.5: Plot of Simulated and Experimental Losses for Paralleled MOSFETs used in the SS-PWM Topology

4.5.3 Summary of Losses for Three Paralleled MOSFETs SS-PWM Topology

From the results obtained is this section it is seen that paralleling three MOSFETs will decrease the conduction losses because of the decrease of the effective R_{dson}. Switching losses however will increase because the parasitic capacitances C_{gs} and C_{gd} will also

increase requiring more gate drive power to turn the devices on and off. This is the same as in the case when MOSFETs in HS-PWM circuits are paralleled and when two MOSFETs are paralleled in SS-PWM circuits. The increase in the drain-source capacitances C_{ds} will have no effect on losses because the load circuit will discharge them before the MOSFETs are turned on. Also, as mentioned above, since it is unlikely that all the MOSFETs will turn on and off at the same time, there will exist a period of time when only one MOSFET is conducting. During this period it will seem as if only one MOSFET is used and the conduction losses will be the same as in the single MOSFET case.

As switching frequencies are increased, the drive power required to charge and discharge the parasitic capacitances will also increase. Also, the time period when only one MOSFET conducts will become more significant with respect to the on time of the MOSFET. This means that savings obtained by paralleling MOSFETs will decrease as switching frequency increases. Since SS-PWM minimizes switching losses, higher switching frequencies are used. This makes the delay time more significant with respect to the on time of the MOSFETs. As the delay time becomes more significant the gains obtained in efficiency by paralleling MOSFETs are minimized.

From the experimental results it is seen that as more MOSFETs are added in parallel, the overall losses decrease. The losses do not decrease to a third when three MOSFETs are used in parallel because losses are still incurred when the gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs} are charged and discharged during switching.

It was also observed that when three MOSFETs were paralleled the savings were minimal as compared to the case when two MOSFETs were paralleled.

CHAPTER 5

COMPARISON BETWEEN HARD AND SOFT SWITCHING CONVERTERS WITH PARALLELED MOSFETS

5.1 Introduction

In this section the advantages and disadvantages of paralleling MOSFETS are considered for the HS-PWM and SS-PWM topologies. A simplified procedure is also presented and explained which allows the designer to determine if paralleling MOSFETs in either topology will yield any savings in power dissipation.

5.2 Advantages and Limitations of Paralleling MOSFETs in the HS-PWM Topology

In Chapter 3, the HS-PWM topology was studied when a single and paralleled MOSFET were used as switching elements. It was observed analytically and experimentally that total losses increased when two MOSFETs were paralleled in the HS-PWM topology. Also when three paralleled MOSFETs were used as a switching element, the total losses also increased compared to the losses observed in the single MOSFET case. Although the effective R_{dson} of the paralleled combination

decreased, the energy lost in switching the MOSFETs on and off increased because of the increased parasitic capacitances. Since the HS-PWM topology does not discharge the drain-source and drain-gate capacitances before the MOSFET is switched on, these capacitances will be forced to discharge through the MOSFET when it turns on.

The variations of the MOSFETs input capacitance C_{iss}, the gate-source threshold voltage V_{gsth}, and transconductance g_{fs}, will cause the MOSFETs in the parallel combination to turn on and off at different times. This will prevent the effective R_{dson} from being *1/n* that observed in the single MOSFET case when *n* MOSFETs are paralleled. Also, the MOSFET which turns on first must carry the full load current and also discharge the drain-source capacitance C_{ds} of the other MOSFETs in the parallel combination. This must be considered when selecting the MOSFET.

The effectiveness of paralleling MOSFETs in the HS-PWM topology to decrease the losses is dependent on the load current, the switching frequency of the converter, the on drain-source resistance R_{dson}, and the parasitic capacitances C_{ds}, C_{gs}, and C_{gd}. By observing the switching waveforms obtained in Chapter 3, the power lost in the parasitic capacitances C_{ds}, C_{gs} and C_{gd}, can be approximated by the following equation:

$$P_{cap} = \frac{1}{2}(C_{gs} \cdot V_{gs}^2 + C_{ds} \cdot V_{ds}^2 + C_{gd} \cdot V_{gd}^2) \cdot f \qquad (5.1)$$

where

V_{gs} is the gate-source voltage

V_{ds} is the drain-source voltage

V_{gd} is the gate-drain voltage, and

f is the switching frequency.

The conduction losses, P_{cond}, can be approximated by the following equation:

$$P_{cond} = I_d^2 \cdot R_{ds(on)} \cdot t_{on} \cdot f \qquad (5.2)$$

where

I_d is the drain current, and

t_{on} is the on time of the MOSFET.

The off losses, P_{off}, are approximated by the following equation:

$$P_{off} = I_{dss} \cdot V_{dd} \cdot t_{off} \cdot f \qquad (5.3)$$

where

I_{dss} is the leakage current which flows when the MOSFET is turned off.

V_{dd} is the applied DC bus voltage, and

t_{off} is the time the MOSFET is turned off.

The transition losses, P_{trans}, also known as the switching losses are approximated by the following equation:

$$P_{trans} = \frac{1}{2} \cdot (I_d \cdot V_{ds}) \cdot (t_{ondly} + t_{offdly}) \cdot f \qquad (5.4)$$

where

V_{ds} is the drain source voltage at turn off,

t_{ondly} is the MOSFETs turn on delay time, and

t_{offdly} is the MOSFETs turn off delay time.

The total MOSFET losses, P_{tot}, is the sum of all these losses:

$$P_{tot} = P_{cap} + P_{cond} + P_{off} + P_{trans} \qquad (5.5)$$

From the equations above it is seen that if the switching frequency and load current are kept constant, then paralleling MOSFETs will increase the P_{cap} and P_{off} losses, and decrease the *Pcond* losses. The transition losses P_{trans} will remain the same for the paralleled combination. Intuitively it can be seen that if P_{cap} and P_{off} are a significant part off the losses, paralleling will have a minimal effect on decreasing the MOSFET losses. If the conduction losses P_{cond} form a significant part of the losses, then paralleling will have a larger effect on decreasing the switching losses. The ratio of conduction

losses P_{cond} to total losses P_{tot} can be used as a figure to determine the effect of paralleling. The closer this ratio is to 1, the greater the effect paralleling will have in decreasing losses.

The following simplified procedure should be used to determine if paralleling will have a significant effect on decreasing the MOSFET losses. It can also be used to determine which MOSFET will have the greatest impact when they are paralleled.

1) Determine the conduction losses P_{cond}, by using equation 5.2. This equation assumes that the MOSFETs will turn on at the same time. Although this is very unlikely, it does not matter in this comparison since exact values are not important.

2) Determine the parasitic capacitance losses P_{cap}, by using equation 5.1.

3) Determine the off losses P_{off}, by using equation 5.3.

4) Determine the transition losses P_{trans}, by using equation 5.4.

5) Calculate the total losses P_{tot}, by using equation 5.5.

6) Determine the ratio of conduction losses to total losses by using the following equation:

$$CL = \frac{P_{cond}}{P_{tot}} \qquad (5.6)$$

The closer this number is to one the greater the effect in decreasing the losses when the MOSFETs are paralleled.

At this point the designer may wish to consider using other MOSFETs which will have a larger portion of its total losses due to its R_{dson}. Of course it is desirable that the new MOSFET selected will achieve this by decreasing its overall losses. Steps 1 to 6 should be repeated until an acceptable solution considering cost, design, and component limitations is reached.

Once a MOSFET is selected the effects of paralleling can be assessed by using the following steps.

1) Use equation 5.7 below to determine the total losses $P_{tot(n)}$, for different paralleled MOSFET combinations. Although this equation is valid for any number of MOSFETs, it is recommended that for practical reasons, no more than two MOSFETs in parallel should be considered.

$$P_{tot(n)} = (\frac{1}{n})^2 \cdot P_{cond} + n \cdot (P_{off} + P_{car}) + \frac{P_{trans}}{n} \qquad (5.7)$$

where n is the number of MOSFETs in parallel.

2) The total MOSFET losses $P_{tot(n)}$ as a function of the number of MOSFETs n, could then be plotted to illustrate the effect on paralleling

on the losses as different MOSFETs are paralleled. An example illustrating this procedure is given in Appendix A.

For most modern switching power supplies using HS-PWM, paralleling MOSFETs will not decrease total losses even though individual MOSFET losses will decrease. Some improvement may result when the switching frequency is decreased since this will make the conduction losses more significant with respect to the total MOSFET losses. This is not desirable since the magnetics in the power supply will have to increase in size. Also, the transition losses are a significant portion of the losses and are not affected by the number of MOSFETs that are paralleled. Therefore, the MOSFETs parameters mentioned above should be considered before they are paralleled. From Appendix A, it is observed that paralleling some MOSFETs will increase overall losses while paralleling others will decrease the overall losses. The closer the *CL* coefficient is to 1, the more optimal results will be obtained when MOSFETs are paralleled. However, this may not yield a combination which will give the lowest total MOSFET losses. It is recommended that the analysis described above be done to determine which combination of MOSFETs will yield the best results. The other advantage obtained by paralleling MOSFETs is that the lower individual MOSFET losses will allow the MOSFETs junction to operate at a lower temperature. This allows the converter's heatsink to be smaller for a fixed ambient and junction temperature. Appendix C shows an analysis comparing heatsink size required for different parallel combinations of MOSFETs.

5.3 Advantages and Limitations of Paralleling MOSFETs in the SS-PWM Topology

In Chapter 4, the SS-PWM topology was studied when a single and paralleled MOSFETs were used as switching elements It was observed analytically and experimentally that total losses decreased but did not drop to half the value when two MOSFETs were paralleled in the SS-PWM topology Also when three paralleled MOSFETs were used as a switching element, the total losses decreased but were not less than a third of the losses observed in the single MOSFET case. Although the effective R_{dson} of the paralleled combination decreased, energy was lost in switching the MOSFETs on and off and this energy increased because of the increased gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}. The increase in the drain-source capacitance had no effect on the losses since it continued to be discharged by the load current. The increased drain-source capacitance did increase the time required to discharge it since the load current was the same as in the single MOSFET case. This decreased the available duty cycle available for regulation of the power supply.

As in the HS-PWM topology, the variations of the MOSFETs input capacitance C_{iss}, the gate-source threshold voltage V_{gsth}, and transconductance g_{fs}, will cause the MOSFETs in the parallel combination to turn on and off at different times. This will prevent the effective R_{dson} from being $1/n$ that observed in the single MOSFET case when n MOSFETs are paralleled. Also, the MOSFET which turns on first must carry the full load current and also discharge the drain-source

capacitance C_{ds} of the other MOSFETs in the parallel combination. This must be considered when selecting the MOSFET.

The effectiveness of paralleling MOSFETs in the SS-PWM topology to decrease the losses is dependent on the load current, the switching frequency of the converter, the on drain-source resistance R_{dson}, and the parasitic capacitances C_{gs}, and C_{gd}. By observing the switching waveforms obtained in Chapter 4, the power lost in the parasitic capacitances C_{gs} and C_{gd}, can be approximated by the following equation:

$$P_{cap} = \frac{1}{2}(C_{gs} \cdot V_{gs}^2 + C_{gd} \cdot V_{gd}^2) \cdot f \qquad (5.8)$$

where

V_{gs} is the gate-source voltage

V_{gd} is the gate-drain voltage, and

f is the switching frequency.

The conduction losses P_{cond}, consist of the two seperate losses which occur when the MOSFET is turned on. The first loss P_{ds}, is due to the current flowing through the drain source conduction channel. The second loss P_{diode} is due to the current flowing through the anti-parallel body diode D_{ds}. There are also two conditions of operation during the turn on period. If the drain current I_d is not large enough to forward bias the anti-parallel diode D_{ds}, then all of it will flow through the drain-source conduction channel of the MOSFET and the losses can be approximated by equation 5.10 If the drain current I_d is large

enough to forward bias the anti-parallel diode D_{ds} then current will flow through both the drain-source conduction channel of the MOSFET and it anti-parallel body diode D_{ds}. The losses in this case can be approximated by equation 5.11.

$$P_{cond} = P_{ds} + P_{diode} \tag{5.9}$$

$$P_{cond} = I_d^2 \cdot R_{dson} \cdot t_{on} \cdot f \tag{5.10}$$

if $I_d \leq \frac{V_{df}}{R_{dson}}$, or,

$$P_{cond} = (((\frac{V_{df}^2}{R_{dson}} + (I_d - \frac{V_{df}}{R_{dson}}) \cdot V_{df}) \cdot t_1 + (I_d^2 \cdot R_{dson} \cdot t_2)) \cdot f \tag{5.11}$$

if $I_d \geq \frac{V_{df}}{R_{dson}}$

where

I_d is the drain current flowing through the MOSFET,

V_{df} is the voltage drop across the anti-parallel MOSFET diode D_{ds},

t_1 is the time both the MOSFETs drain-source channel and diode D_{ds} are conducting,

t_2 is the time when only the diode D_{ds} is conducting,

t_{on} is the time the MOSFET is turned on, and

f is the switching frequency.

The off losses, P_{off}, consist of two separate losses. These losses are the leakage losses P_{leak}, which occur when the MOSFET is turned off and it is blocking a drain-source voltage, and the reverse conduction losses P_{dio}, which occur when the MOSFET is off and current is flowing through the anti-parallel body diode D_{ds}. These losses can be approximated by the following equation:

$$P_{off} = P_{leak} + P_{dio} \tag{5.12}$$

$$P_{off} = (I_{dss} \cdot V_{dd} \cdot t_{off} + I_d \cdot V_{df} \cdot t_3) \cdot f \tag{5.13}$$

where

I_{dss} is the leakage current which flows when the MOSFET is turned off and a drain-source voltage is applied,

V_{dd} is the applied DC bus voltage,

V_{df} is the anti-parallel diode D_{ds} voltage drop,

t_{off} is the time the MOSFET is turned off, and

t_3 is the time the anti-parallel diode D_{ds} conducts.

For the SS-PWM topology there are no transition losses because the MOSFETs voltage is zero when it turn on and its drain-source current is diverted to the snubber capacitors when it is turned off.

The total MOSFET losses, P_{tot}, is the sum of all these losses:

$$P_{tot} = P_{cap} + P_{cond} + P_{off} \tag{5.14}$$

From the equations above it is seen that if the switching frequency and load current are kept constant, then paralleling MOSFETs will increase the P_{cap} and P_{off} losses, and decrease the P_{cond} losses. This was similar in the HS-PWM case. However, the P_{cap} losses are less in the SS-PWM topology because the drain-source capacitance C_{ds} discharged by the resonant load current. Intuitively it can be seen that if P_{cap} and P_{off} are a significant part of the losses, paralleling will have a minimal effect on decreasing the MOSFET losses. If the conduction losses P_{cond} form a significant part off the losses, then paralleling will have a larger effect on decreasing the switching losses. The ratio of conduction losses P_{cond} to total losses P_{tot} can be used as a figure to determine the effect of paralleling. The closer this ratio is to 1, the greater the effect paralleling will have in decreasing the losses.

The following simplified procedure should be used to determine if paralleling will have a significant effect on decreasing the MOSFET losses. It can also be used to determine which MOSFET will have the greatest impact.

1) Determine the conduction losses P_{cond}, by using equation 5.10 or equation 5.11 depending on the value of I_d with respect to V_{df}, n, and R_{dson}. This equation assumes that the MOSFETs will turn on at the same time. Although this is very unlikely, it does not matter in this comparison since exact values are not important.

The times t_1 and t_2 can be obtained by simulation of the resonant circuit and the load.

2) Determine the parasitic capacitance losses P_{cap}, by using equation 5.8.

3) Determine the off losses P_{off}, by using equation 5.13. The time t_3 can be obtained by simulation of the resonant circuit and the load.

4) Calculate the total losses P_{tot}, by using equation 5.14.

5) Determine the ratio of conduction losses to total losses by using the following equation:

$$CL = \frac{P_{cond}}{P_{tot}} \qquad (5.15)$$

The closer this number is to one the greater the effect in decreasing the losses when the MOSFETs are paralleled.

At this point the designer may wish to consider using other MOSFETs which will have a larger portion of its total losses due to its R_{dson}. Of course it is desirable that the new MOSFET selected will achieve this by decreasing its overall losses. Steps 1 to 5 should be repeated until an acceptable solution considering cost, design, and component limitations is reached.

Once a MOSFET is selected the effects of paralleling can be assessed by using the following steps.

1) Use equation 5.16 or equation 5.17 depending on the value of I_d with respect to V_{df}, n, and R_{dson} to determine the total losses $P_{tot(n)}$, for different paralleled MOSFET combinations. Although this equation is valid for any number of MOSFETs, it is recommended that for practical reasons, no more than two MOSFETs in parallel should be considered in SS-PWM topologies.

$$P_{tot(n)} = n \cdot \left(\left(\frac{I_d}{n}\right)^2 \cdot R_{dson} \cdot t_{on} + I_{dss} \cdot V_{dd} \cdot t_{off} + I_d \cdot V_{df} \cdot t_1 + P_{cap}\right) \cdot f \qquad (5.16)$$

if $I_d \le \frac{V_{df}}{R_{dson}}$, or,

$$P_{tot(n)} = n \cdot \left(\left(\frac{V_{df}^2 \cdot n}{R_{dson}} + \left(\frac{I_d \cdot V_{df} \cdot n}{R_{dson}}\right)\right) \cdot V_{df} \cdot t_1 + \left(\frac{I_d}{n}\right)^2 \cdot R_{dson} \cdot t_2 + I_{dss} \cdot V_{dd} \cdot t_{off} + I_d \cdot V_{df} \cdot t_1 + P_{cap}\right) \cdot f \qquad (5.17)$$

if $I_d \ge \frac{V_{df}}{R_{dson}}$

2) The total MOSFET losses $P_{tot(n)}$ as a function of the number of MOSFETs n, could then be plotted to illustrate the effect on paralleling on the losses as different MOSFETs are paralleled. An example illustrating this procedure is given in Appendix B.

For most modern switching power supplies using SS-PWM, paralleling MOSFETs will decrease the total losses. These losses however will not

decrease to $1/n$ the losses observed for a single MOSFET because the leakage losses P_{leak} and the parasitic capacitance losses P_{cap} increase as MOSFETs are paralleled. Also, the overall off diode losses P_{dio} will stay the same as MOSFETs are paralleled. Some improvement may result when the switching frequency is decreased since this will make the conduction losses more significant with respect to the total MOSFET losses. This is not desirable since the magnetics in the power supply will have to increase in size. Therefore, MOSFETs should be paralleled if decreasing the losses is the main criteria when SS-PWM topologies are used. Of course the increased cost of MOSFETs must be considered and assessed. In some applications where space is limited, it may be the only solution a designer has to fit the converter in the given area. In cost sensitive applications, paralleling may not be desirable if the efficiency specifications are met.

CHAPTER 6

SUMMARY and CONCLUSIONS

6.1 Summary of the Thesis

MOSFETs are paralleled to obtain higher current handling capabilities, and to lower losses. A simplified MOSFET model was presented in Chapter 2 which considers the parasitic capacitances and inductances. This model was found to give reasonable results and not require long simulation times. Considerations in paralleling MOSFETs were also discussed in Chapter 2. Dynamic and static current sharing were discussed and the MOSFET parasitic variations were presented to show that these vary significantly from device to device.

Chapter 3 discussed the HS-PWM topology used in this thesis and the MOSFETs losses observed during operation. This section was divided into theoretical and simulated, and experimental sections. The theoretical and simulated section described the effects of switching on the MOSFETs parasitic capacitances using the model described in Chapter 2. The experimental section presented results that were obtained in the laboratory and compared with the losses obtained by simulation. This format was repeated for single MOSFETs, two MOSFETs connected in parallel, and three MOSFETs connected in parallel.

Chapter 4 discussed the SS-PWM topology used in this thesis and the MOSFET losses observed during operation. This section was divided into theoretical, simulated and experimental sections. The theoretical section presented the analytical results that were expected when the MOSFETs were operating in the SS-PWM topology. The simulated results show the PSPICE results which were obtained when the MOSFET model described in Chapter 2 was used in the SS-PWM topology. The experimental section presents results which were obtained in the laboratory and compared with the results obtained by simulation. This format was repeated for single MOSFETs, two MOSFETs connected in parallel, and three MOSFETs connected in parallel.

The results obtained in Chapter 3 and Chapter 4 were summarized in Chapter 5. The advantages and disadvantages of paralleling MOSFETs in HS-PWM and SS-PWM were also reviewed. In this section a simplified procedure was discussed which would help the designer to determine if paralleling MOSFETs would reduce losses in HS-PWM and SS-PWM topologies.

6.2 Conclusions

The effectiveness of paralleling MOSFETs is dependent on the MOSFETs, the topology and the operational parameters of the converter. Determining the exact power losses due to parasitic parameters was found to be difficult because these parameters are not tightly specified in the manufacturers data sheets. This is because these parameters vary

widely from device to device. Also, the layout parasitics such as lead inductances and capacitance will affect the loss results.

Paralleling MOSFETs for HS-PWM topologies lowered the individual MOSFET losses but not the overall switch losses. This occurred because the drain-source capacitance C_{ds}, the gate-drain capacitance C_{gd}, and the gate-source capacitance C_{gs}, increased when MOSFETs are paralleled. The individual MOSFET conduction losses due to the R_{dson} decreased and because the drain current I_d is less, overall switch conduction losses decreased as well. The individual MOSFET transition losses also decreased, but the overall switch transition losses remained the same. The effectiveness of paralleling MOSFETs in HS-PWM topologies depends on the ratio of conduction losses to the overall losses. This ratio can be approximated by the formulas described in Chapter 6 and should be used to determine the effectiveness of paralleling before the decision is made to parallel MOSFETs.

The variation of the MOSFETs parasitic parameters also reduce the effectiveness of paralleling MOSFETs by allowing one MOSFET to turn on before the other. As a result the MOSFETs should be chosen to have similar gate-source threshold voltage V_{gsth}, input capacitance C_{iss}, and transconductance g_{fs}.

Paralleling MOSFETs for SS-PWM topologies lowered the individual MOSFET losses and the overall switch losses. This occurred because the drain-source capacitance C_{ds} was discharged by the resonant load current before the MOSFETs were turned on and there were no transition losses.

The individual MOSFET conduction losses due to the R_{dson} decreased and because the drain current I_d is less, overall switch conduction losses decreased as well. The effectiveness of paralleling MOSFETs in SS-PWM topologies depends on the ratio of conduction losses to the overall losses. This ratio can be approximated by the formulas described in Chapter 5 and should be used to determine the effectiveness of paralleling before the decision is made to parallel MOSFETs. As in HS-PWM case the gate source threshold voltage V_{gsth}, the input capacitance C_{iss} and the transconductance g_{fs} should be similar for the MOSFETs being paralleled so that they will turn on and off at the same time.

Finally, when MOSFETs are paralleled the layout should be symmetrical with respect to the power circuit and the drive circuit. Similar drain-source circuit traces will ensure similar drain impedance which will improve dynamic current sharing. Similar drive circuit traces will ensure similar gate-source impedance, allowing the devices to turn on at the same time and optimizing the effect of paralleling.

6.3 Suggestions for Future Work

Future work on paralleling MOSFETs should concentrate on SS-PWM techniques since this topology gives the best results. The MOSFET model presented in Chapter 2 should also be improved by adding more parasitic components as computer speeds increase.

Work on a more realistic PSPICE simulation model should consider the printed circuit board layout parasitic inductances and capacitances Again, this becomes more feasible as computer speeds increase, decreasing the simulation times required for analysis.

Optimization of paralleled MOSFETs would result if the devices turn on and off at the same time. Work should be done to design a circuit which can monitor the turn on and turn off characteristics of the MOSFETs and control the driver for each individual device In order to minimize the drawbacks, this circuit should not significantly increase the switching time of the MOSFETs

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APPENDIX A

Mathcad Spreadsheets used to Determine the Effectiveness of Paralleling MOSFETs in the HS-PWM Topology

Appendix A1 - Program to Determine the Effectiveness of Paralleling IRF720 MOSFETs in the HS-PWM Topology

Appendix A2 - Program to Determine the Effectiveness of Paralleling IRF730 MOSFETs in the HS-PWM Topology

Appendix A3 - Program to Determine the Effectiveness of Paralleling IRF740 MOSFETs in the HS-PWM Topology

Appendix A1

Program to Estimate the Effectivness of Paralleling IRF720 MOSFETs in the HS-PWM Topology

Units:

m = 0.001	ohm = 1	Hz = 1
u = m·m	F = 1	W = 1
n = u·m	S = 1	
p = n·m	A = 1	
K = 1000	V = 1	

Parameters : MOSFET IRF720

Rdson = 1.8·ohm

Ciss = 600·p·F	tondly = 40·n·S	Idss = 1·m·A
Coss = 200·p·F	toffdly = 100·n·S	
Crss = 40·p·F		

Application Parameters:

Id = 3·A	Drain Current
d = 0.3	Duty Cycle
Vdd = 400·V	Applied Drain-Source Voltage
Vgs = 12·V	Applied Gate-Source Voltage
f = 128·K·Hz	Switching Frequency

Calculations:

Cgs = Ciss − Crss

Cgs = 560·p·F

Cds = Coss − Crss

Cds = 160·p·F

Cdg = Crss

Cdg = 40·p·F

Vgs = 2·Vgs

Vgs = 24·V

$Vdg = \frac{Vdd}{2} - Vgs$

Vdg = 224·V

$Vds = \frac{Vdd}{2}$

Vds = 200·V

$ton = \frac{1}{f}\cdot d$

ton = 2.344·u·S

$toff = \frac{1}{f}\cdot(1 - d)$

toff = 5.469·u·S

Step 1: Calculation of Conduction Losses

$Pcond = Id^2 \cdot Rdson \cdot ton \cdot f$ (5.2)

Pcond = 4.86·W

Step 2: Calculation of Parasitic Capacitance Losses

$$Pcap := \frac{1}{2}\cdot\left(Cgs\cdot Vgs^2 + Cds\cdot Vds^2 + Cdg\cdot Vdg^2\right)\cdot f \qquad (5.1)$$

$$Pcap = 0.559\cdot W$$

Step 3: Calculation of Off Losses

$$Poff := Idss\cdot Vdd\cdot toff\cdot f \qquad (5.3)$$

$$Poff = 0.28\cdot W$$

Step 4: Calculation of Transition Losses

$$Ptrans := \frac{Id\cdot Vds\cdot(tondly + toffdly)}{2}\cdot f \qquad (5.4)$$

$$Ptrans = 5.376\cdot W$$

Step 5: Total MOSFET Losses

$$Ptot_1 := Pcond + Pcap + Poff + Ptrans \qquad (5.5)$$

$$Ptot_1 = 11.075\cdot W$$

Step 6: Calculation of Effectivness Coefficient CL

$$CL := \frac{Pcond}{Ptot_1} \qquad (5.6)$$

$$CL = 0.439$$

Step 7: Calculation of Paralleled MOSFET Losses (Individual)

$$n := 2..3$$

$$Ptot_n := \left(\frac{1}{n}\right)^2\cdot Pcond + (Poff + Pcap) + \frac{Ptrans}{n} \qquad (5.7)$$

$Ptot_2 = 4.742\cdot W$ (2 MOSFETs)

$Ptot_3 = 3.171\cdot W$ (3 MOSFETs)

Step 8: Calculation of Paralleled MOSFET Losses (Total)

$n := 1..3$

$Ptott_n := Ptot_n \cdot n$

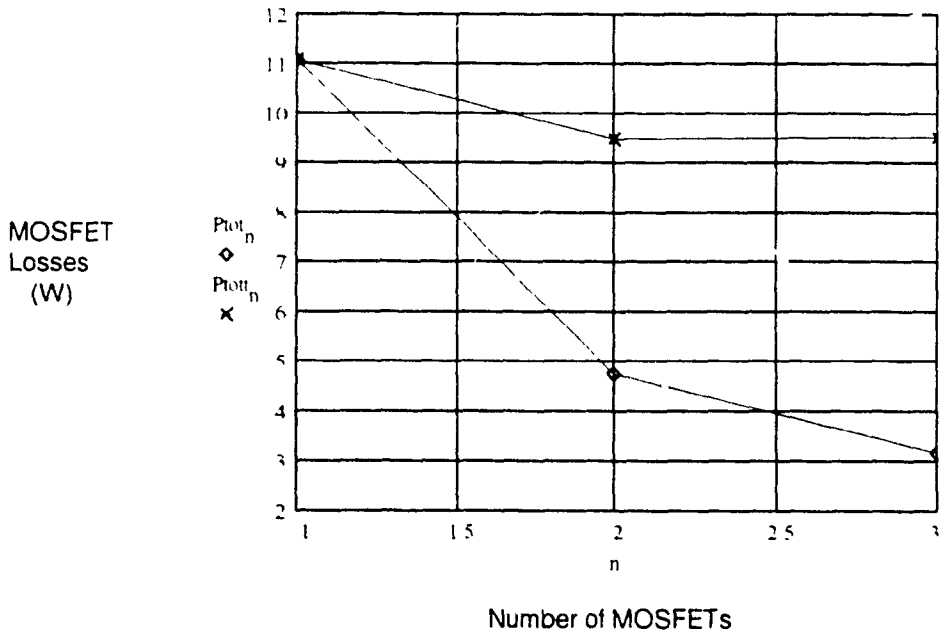
$Ptott_1 = 11.075 \cdot W$ (1 MOSFET)

$Ptott_2 = 9.483 \cdot W$ (2 MOSFETs)

$Ptott_3 = 9.512 \cdot W$ (3 MOSFETs)

Step 9: Plot of Paralleled MOSFET Losses (Individual and Total)

$n := 1..3$



Appendix A2

Program to Estimate the Effectivness of Paralleling IRF730 MOSFETs in the HS-PWM Topology

Units:

m = 0.001	ohm = 1	Hz = 1
u = m·m	F = 1	W = 1
n = u·m	S = 1	
p = n·m	A = 1	
K = 1000	V = 1	

Parameters : MOSFET IRF730

Rdson = 1.0·ohm

Ciss = 800·p·F	tondly = 30·n·S	Idss = 1·m·A
Coss = 300·p·F	toffdly = 55·n·S	
Crss = 80·p·F		

Application Parameters:

Id = 3·A	Drain Current
d = 0.3	Duty Cycle
Vdd = 400·V	Applied Drain-Source Voltage
Vgs = 12·V	Applied Gate-Source Voltage
f = 128·K·Hz	Switching Frequency

Calculations:

$Cgs = Ciss - Crss$ $\quad Cgs = 720 \cdot p \cdot F$

$Cds = Coss - Crss$ $\quad Cds = 220 \cdot p \cdot F$

$Cdg = Crss$ $\quad Cdg = 80 \cdot p \cdot F$

$Vgs = 2 \cdot Vgs$ $\quad Vgs = 24 \cdot V$

$Vdg = \frac{Vdd}{2} + Vgs$ $\quad Vdg = 224 \cdot V$

$Vds = \frac{Vdd}{2}$ $\quad Vds = 200 \cdot V$

$ton = \frac{1}{f} \cdot d$ $\quad ton = 2.344 \cdot u \cdot S$

$toff = \frac{1}{f} \cdot (1 - d)$ $\quad toff = 5.469 \cdot u \cdot S$

Step 1: Calculation of Conduction Losses

$Pcond = Id^2 \cdot Rdson \cdot ton \cdot f$ (5.2)

$Pcond = 2.7 \cdot W$

Step 2: Calculation of Parasitic Capacitance Losses

$$Pcap = \frac{1}{2}\cdot\left(Cgs\cdot Vgs^2 + Cds\cdot Vds^2 + Cdg\cdot Vdg^2\right)\cdot f \qquad (5.1)$$

$$Pcap = 0.847\cdot W$$

Step 3: Calculation of Off Losses

$$Poff = Idss\cdot Vdd\cdot toff\cdot f \qquad (5.3)$$

$$Poff = 0.28\cdot W$$

Step 4: Calculation of Transition Losses

$$Ptrans = \frac{Id\cdot Vds\cdot(tondly + toffdly)}{2}\cdot f \qquad (5.4)$$

$$Ptrans = 3.264\cdot W$$

Step 5: Total MOSFET Losses

$$Ptot_1 = Pcond + Pcap + Poff + Ptrans \qquad (5.5)$$

$$Ptot_1 = 7.091\cdot W$$

Step 6: Calculation of Effectivness Coefficient CL

$$CL = \frac{Pcond}{Ptot_1} \qquad (5.6)$$

$$CL = 0.381$$

Step 7: Calculation of Paralleled MOSFET Losses (Individual)

$$n = 2..3$$

$$Ptot_n = \left(\frac{1}{n}\right)^2\cdot Pcond + (Poff + Pcap) + \frac{Ptrans}{n} \qquad (5.7)$$

$$Ptot_2 = 3.434\cdot W \qquad \text{(2 MOSFETs)}$$

$$Ptot_3 = 2.515\cdot W \qquad \text{(3 MOSFETs)}$$

Step 8: Calculation of Paralleled MOSFET Losses (Total)

$n := 1..3$

$Ptott_n := Ptot_n \cdot n$

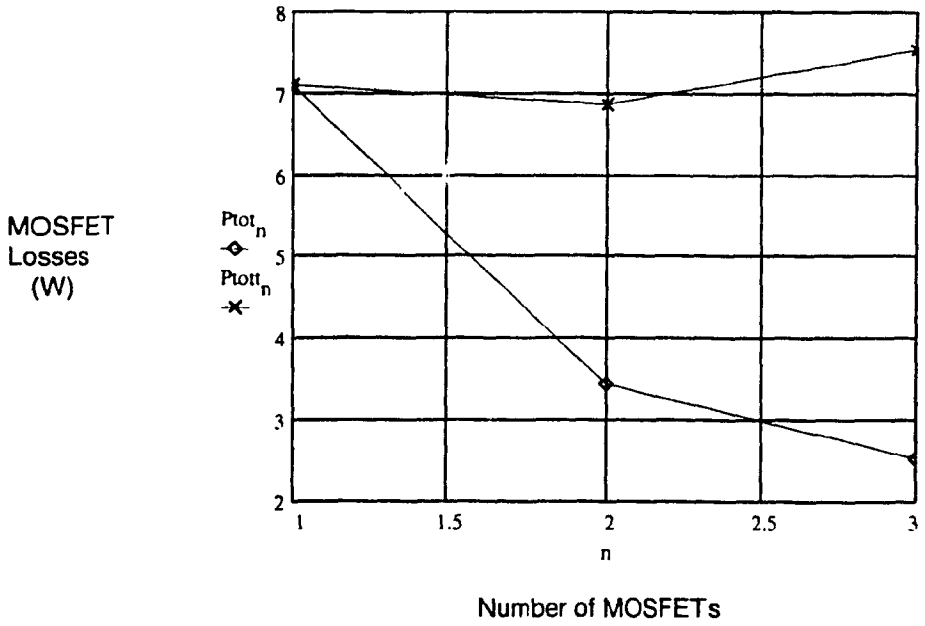
$Ptott_1 = 7.091 \cdot W$ (1 MOSFET)

$Ptott_2 = 6.867 \cdot W$ (2 MOSFETs)

$Ptott_3 = 7.544 \cdot W$ (3 MOSFETs)

Step 9: Plot of Paralleled MOSFET Losses (Individual and Total)

$n := 1..3$



Appendix A3

Program to Estimate the Effectivness of Paralleling IRF740 MOSFETs in the HS-PWM Topology

Units:

m = 0.001	ohm = 1	Hz = 1
u = m·m	F = 1	W = 1
n = u·m	S = 1	
p = n·m	A = 1	
K = 1000	V = 1	

Parameters : MOSFET IRF740

Rdson = 0.55·ohm

Ciss = 1600·p·F	tondly = 35·n·S	Idss = 1·m·A
Coss = 450·p·F	toffdly = 90·n·S	
Crss = 150·p·F		

Application Parameters:

Id = 3·A	Drain Current
d = 0.3	Duty Cycle
Vdd = 400·V	Applied Drain-Source Voltage
Vgs = 12·V	Applied Gate-Source Voltage
f = 128·K·Hz	Switching Frequency

Calculations:

Cgs = Ciss - Crss

Cgs = $1.45 \cdot 10^{3}$ ·p·F

Cds = Coss - Crss

Cds = 300·p·F

Cdg = Crss

Cdg = 150·p·F

Vgs = 2·Vgs

Vgs = 24·V

$$Vdg = \frac{Vdd}{2} + Vgs$$

Vdg = 224·V

$$Vds = \frac{Vdd}{2}$$

Vds = 200·V

$$ton = \frac{1}{f} \cdot d$$

ton = 2.344·u·S

$$toff = \frac{1}{f} \cdot (1 - d)$$

toff = 5.469·u·S

Step 1: Calculation of Conduction Losses

$Pcond = Id^2 \cdot Rdson \cdot ton \cdot f$ (5.2)

Pcond = 1.485·W

Step 2: Calculation of Parasitic Capacitance Losses

$$Pcap := \frac{1}{2}\cdot\left(Cgs\cdot Vgs^2 + Cds\cdot Vds^2 + Cdg\cdot Vdg^2\right)\cdot f \qquad (5.1)$$

$$Pcap = 1.303\cdot W$$

Step 3: Calculation of Off Losses

$$Poff := Idss\cdot Vdd\cdot toff\cdot f \qquad (5.3)$$

$$Poff = 0.28\cdot W$$

Step 4: Calculation of Transition Losses

$$Ptrans := \frac{Id\cdot Vds\cdot(tondly + toffdly)}{2}\cdot f \qquad (5.4)$$

$$Ptrans = 4.8\cdot W$$

Step 5: Total MOSFET Losses

$$Ptot_1 := Pcond + Pcap + Poff + Ptrans \qquad (5.5)$$

$$Ptot_1 = 7.868\cdot W$$

Step 6: Calculation of Effectivness Coefficient CL

$$CL := \frac{Pcond}{Ptot_1} \qquad (5.6)$$

$$CL = 0.189$$

Step 7: Calculation of Paralleled MOSFET Losses (Individual)

$$n := 2..3$$

$$Ptot_n := \left(\frac{1}{n}\right)^2\cdot Pcond + (Poff + Pcap) + \frac{Ptrans}{n} \qquad (5.7)$$

$$Ptot_2 = 4.354\cdot W \qquad \text{(2 MOSFETs)}$$

$$Ptot_3 = 3.348\cdot W \qquad \text{(3 MOSFETs)}$$

Step 8: Calculation of Paralleled MOSFET Losses (Total)

$n := 1..3$

$Ptott_n := Ptot_n \cdot n$

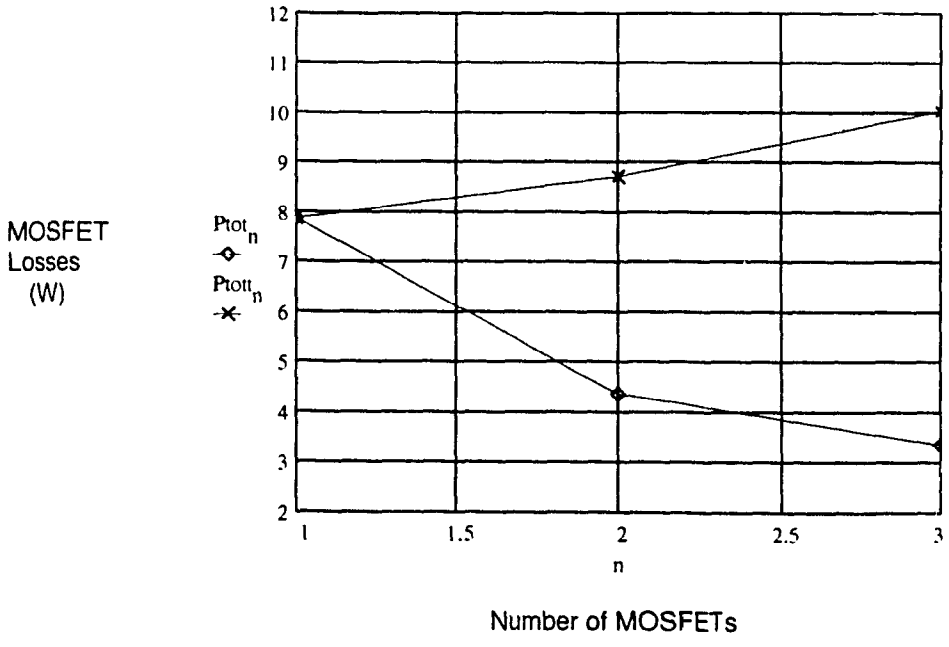
$Ptott_1 = 7.868 \cdot W$ (1 MOSFET)

$Ptott_2 = 8.709 \cdot W$ (2 MOSFETs)

$Ptott_3 = 10.044 \cdot W$ (3 MOSFETs)

Step 9: Plot of Paralleled MOSFET Losses (Individual and Total)

$n := 1..3$



APPENDIX B

Mathcad Spreadsheets used to Determine the Effectiveness of Paralleling MOSFETs in the SS-PWM Topology

Appendix B1 - Program to Determine the Effectiveness of Paralleling IRF720 MOSFETs in the SS-PWM Topology

Appendix B2 - Program to Determine the Effectiveness of Paralleling IRF730 MOSFETs in the SS-PWM Topology

Appendix B3 - Program to Determine the Effectiveness of Paralleling IRF740 MOSFETs in the SS-PWM Topology

Appendix B1

Program to Estimate the Effectivness of Paralleling IRF720 MOSFETs in theSS-PWM Topology

Units:

m = 0.001	ohm = 1	Hz = 1
u = m·m	F = 1	W = 1
n = u·m	S = 1	
p = n·m	A = 1	
K = 1000	V = 1	

Parameters : MOSFET IRF720

Rdson = 1.8·ohm

Ciss = 600·p·F	tondly = 40·n·S	Idss = 1·m·A
Coss = 200·p·F	toffdly = 100·n·S	Vdf = 1·V
Crss = 40·p·F		

Application Parameters:

Id = 5·A	Drain Current
Vdd = 400·V	Applied Drain-Source Voltage
Vgs = 12·V	Applied Gate-Source Voltage
f = 128·K·Hz	Switching Frequency
ton = 1.5·u·S	MOSFET Conduction Time
toff = 2.5·u·S	MOSFET Off Time
t3 = 0.2·u·S	MOSFET Diode Conduction Time

Calculations:

Cgs = Ciss - Crss	Cds = Coss - Crss	Cdg = Crss
Cgs = 560·p·F	Cds = 160·p·F	Cdg = 40·p·F
Vgs = 2·Vgs	Vdg = Vdd + Vgs	Vds = 0
Vgs = 24·V	Vdg = 424·V	

Step 1: Calculation of Conduction Losses

$$Pcond = Id^2 \cdot Rdson \cdot ton \cdot f \qquad (5.10)$$

Pcond = 8.64·W

Step 2: Calculation of Parasitic Capacitance Losses

$$Pcap := \frac{1}{2}\cdot\left(Cgs\cdot Vgs^2 + Cdg\cdot Vdg^2\right)\cdot f \qquad (5.8)$$

$$Pcap = 0.481\cdot W$$

Step 3: Calculation of Off Losses

$$Poff1 := Idss\cdot Vdd\cdot toff\cdot f \qquad Poff2 := Id\cdot Vdf\cdot t3\cdot f$$

$$Poff := Poff1 + Poff2$$

$$Poff = 0.256\cdot W$$

Step 4: Total MOSFET Losses

$$Ptot_1 := Pcond + Pcap + Poff \qquad (5.14)$$

$$Ptot_1 = 9.377\cdot W$$

Step 5: Calculation of Effectivness Coefficient CL

$$CL := \frac{Pcond}{Ptot_1} \qquad (5.15)$$

$$CL = 0.921$$

Step 6: Calculation of Paralleled MOSFET Losses (Individual)

$$n := 2..3$$

$$Ptot_n := \left(\frac{1}{n}\right)^2\cdot Pcond + \left(Poff1 + \frac{1}{n}\cdot Poff2 + Pcap\right) \qquad (5.16)$$

$$Ptot_2 = 2.833\cdot W \qquad \text{(2 MOSFETs)}$$

$$Ptot_3 = 1.612\cdot W \qquad \text{(3 MOSFETs)}$$

Step 7: Calculation of Paralleled MOSFET Losses (Total)

$$n := 1..3$$

$$Ptott_n := Ptot_n\cdot n$$

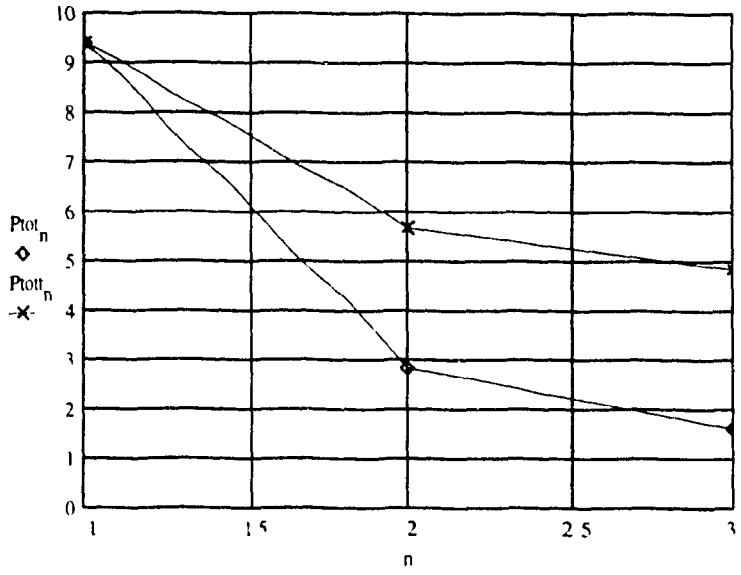
$$Ptott_1 = 9.377\cdot W \qquad \text{(1 MOSFET)}$$

$$Ptott_2 = 5.666\cdot W \qquad \text{(2 MOSFETs)}$$

$$Ptott_3 = 4.835\cdot W \qquad \text{(3 MOSFETs)}$$

Step 8: Plot of Paralleled MOSFET Losses (Individual and Total)

$n := 1 .. 3$



MOSFET Losses (W)

Number of MOSFETs

Appendix B2

Program to Estimate the Effectivness of Paralleling IRF730 MOSFETs in the SS-PWM Topology

Units:

m = 0.001	ohm = 1	Hz = 1
u = m·m	F = 1	W = 1
n = u·m	S = 1	
p = n·m	A = 1	
K = 1000	V = 1	

Parameters . MOSFET IRF730

Rdson = 1.0·ohm

Ciss = 800·p·F	tondly = 30·n·S	Idss = 1·m·A
Coss = 300·p·F	toffdly = 55·n·S	Vdf = 1·V
Crss = 80·p·F		

Application Parameters:

Id = 5·A	Drain Current
Vdd = 400·V	Applied Drain-Source Voltage
Vgs = 12·V	Applied Gate-Source Voltage
f = 128·K·Hz	Switching Frequency
ton = 1.5·u·S	MOSFET Conduction Time
toff = 2.5·u·S	MOSFET Off Time
t3 = 0.2·u·S	MOSFET Diode Conduction Time

Calculations:

Cgs = Ciss - Crss	Cds = Coss - Crss	Cdg = Crss
Cgs = 720·p·F	Cds = 220·p·F	Cdg = 80·p·F
Vgs = 2·Vgs	Vdg = Vdd - Vgs	Vds = 0
Vgs = 24·V	Vdg = 424·V	

Step 1: Calculation of Conduction Losses

$$Pcond = Id^2 \cdot Rdson \cdot ton \cdot f \qquad (5.10)$$

Pcond = 4.8·W

Step 2: Calculation of Parasitic Capacitance Losses

$$Pcap = \frac{1}{2}\cdot\left(Cgs\cdot Vgs^2 + Cdg\cdot Vdg^2\right)\cdot f \qquad (5.8)$$

$$Pcap = 0.947\cdot W$$

Step 3: Calculation of Off Losses

$$Poff1 = Idss\cdot Vdd\cdot toff\cdot f \qquad Poff2 = Id\cdot Vdf\cdot t3\cdot f$$

$$Poff = Poff1 + Poff2$$

$$Poff = 0.256\cdot W$$

Step 4: Total MOSFET Losses

$$Ptot_1 = Pcond + Pcap + Poff \qquad (5.14)$$

$$Ptot_1 = 6.003\cdot W$$

Step 5: Calculation of Effectivness Coefficient CL

$$CL = \frac{Pcond}{Ptot_1} \qquad (5.15)$$

$$CL = 0.8$$

Step 6: Calculation of Paralleled MOSFET Losses (Individual)

$$n = 2..3$$

$$Ptot_n = \left(\frac{1}{n}\right)^2\cdot Pcond + \left(Poff1 + \frac{1}{n}\cdot Poff2 + Pcap\right) \qquad (5.16)$$

$Ptot_2 = 2.339\cdot W$ (2 MOSFETs)

$Ptot_3 = 1.651\cdot W$ (3 MOSFETs)

Step 7: Calculation of Paralleled MOSFET Losses (Total)

$$n = 1..3$$

$$Ptott_n = Ptot_n\cdot n$$

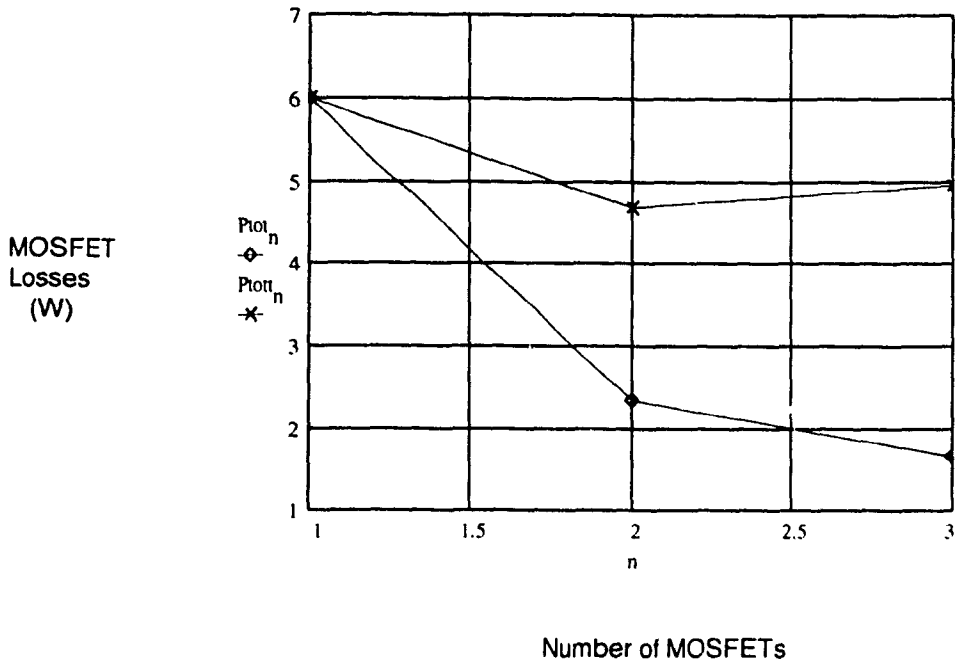
$Ptott_1 = 6.003\cdot W$ (1 MOSFET)

$Ptott_2 = 4.678\cdot W$ (2 MOSFETs)

$Ptott_3 = 4.953\cdot W$ (3 MOSFETs)

Step 8: Plot of Paralleled MOSFET Losses (Individual and Total)

$n := 1..3$



Appendix B3

Program to Estimate the Effectivness of Paralleling IRF740 MOSFETs in the SS-PWM Topology

Units:

m = 0.001	ohm = 1	Hz = 1
u = m·m	F = 1	W = 1
n = u·m	S = 1	
p = n·m	A = 1	
K = 1000	V = 1	

Parameters : MOSFET IRF740

Rdson = 0.55·ohm

Ciss = 1600·p·F	tondly = 35 n·S	Idss = 1·m A
Coss = 450·p·F	toffdly = 90·n·S	Vdf = 1 V
Crss = 150·p·F		

Application Parameters:

Id = 5·A	Drain Current
Vdd = 400·V	Applied Drain-Source Voltage
Vgs = 12·V	Applied Gate-Source Voltage
f = 128·K·Hz	Switching Frequency
ton = 1.5·u·S	MOSFET Conduction Time
toff = 2.5·u S	MOSFET Off Time
t3 = 0.2·u·S	MOSFET Diode Conduction Time

Calculations:

Cgs = Ciss − Crss	Cds = Coss − Crss	Cdg = Crss
Cgs = 1.45·10^3 ·p F	Cds = 300·p·F	Cdg = 150·p·F

Vgs = 2·Vgs	Vdg = Vdd − Vgs	Vds = 0
Vgs = 24·V	Vdg = 424·V	

Step 1: Calculation of Conduction Losses

$$Pcond = Id^2 \cdot Rdson \cdot ton \cdot f \qquad (5.10)$$

Pcond = 2.64·W

Step 2: Calculation of Parasitic Capacitance Losses

$$Pcap = \frac{1}{2}\cdot\left(Cgs\cdot Vgs^2 + Cdg\cdot Vdg^2\right)\cdot f \qquad (5.8)$$

$$Pcap = 1.779\cdot W$$

Step 3: Calculation of Off Losses

$$Poff1 = Idss\cdot Vdd\cdot toff\cdot f \qquad Poff2 = Id\cdot Vdf\cdot t3\cdot f$$

$$Poff = Poff1 + Poff2$$

$$Poff = 0.256\cdot W$$

Step 4: Total MOSFET Losses

$$Ptot_1 = Pcond + Pcap + Poff \qquad (5.14)$$

$$Ptot_1 = 4.675\cdot W$$

Step 5: Calculation of Effectivness Coefficient CL

$$CL = \frac{Pcond}{Ptot_1} \qquad (5.15)$$

$$CL = 0.565$$

Step 6: Calculation of Paralleled MOSFET Losses (Individual)

$$n = 2..3$$

$$Ptot_n = \left(\frac{1}{n}\right)^2\cdot Pcond + \left(Poff1 + \frac{1}{n}\cdot Poff2 + Pcap\right) \qquad (5.16)$$

$Ptot_2 = 2.631\cdot W$ (2 MOSFETs)

$Ptot_3 = 2.243\cdot W$ (3 MOSFETs)

Step 7: Calculation of Paralleled MOSFET Losses (Total)

$$n = 1..3$$

$$Ptott_n = Ptot_n\cdot n$$

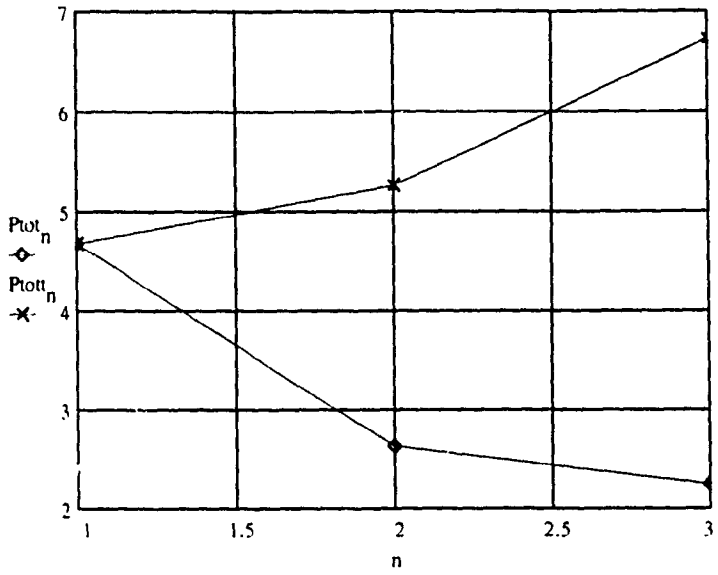
$Ptott_1 = 4.675\cdot W$ (1 MOSFET)

$Ptott_2 = 5.263\cdot W$ (2 MOSFETs)

$Ptott_3 = 6.73\cdot W$ (3 MOSFETs)

Step 8: Plot of Paralleled MOSFET Losses (Individual and Total)

$n := 1..3$



APPENDIX C

Mathcad Spreadsheet used to Determine the Thermal Resistance of the Heatsink when MOSFETs are Paralleled in the HS-PWM Topology

Calculation of Heatsink Thermal Resistance required for Paralleled MOSFETs in the HS-PWM Topology.

Units

$W = 1 \qquad C = 1$

IRF740 Device Losses

$Ptot_1 = 7.868 \cdot W$

$Ptot_2 = 4.354 \cdot W$

$Ptot_3 = 3.348 \cdot W$

Application Information:

$R\theta jc = 1 \cdot \frac{C}{W}$ $\qquad$ $Tjmax = 105 \cdot C$

$Tmaxamb = 65 \cdot C$

Calculation of Heatsink's Thermal Resistance

$n = 1 .. 3$

$$R\theta hs_n := \frac{Tjmax - Tmaxamb}{Ptot_n}$$

$$R\theta hs_1 = 5.084 \cdot \frac{C}{W}$$

$$R\theta hs_2 = 9.187 \cdot \frac{C}{W}$$

$$R\theta hs_3 = 11.947 \cdot \frac{C}{W}$$

When three IRF740 MOSFETs are used in parallel, the heatsink thermal resistance ROhs can be 11.947 C/W. This means that the heatsink can be smaller than in the case where only one IRF740 MOSFET is used.