Design of a 2-Dimensional Single-Chip Accelerometer

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ABSTRACT

Design of a 2-Dimensional Single-Chip Accelerometer

Haider J. Ahmed

A surface micromachined 2-D accelerometer is designed. Its implementation requires only the addition of three critical masking steps and one non-critical masking step to the commercially available Mitel 1.5 μm standard CMOS process. It has a ±100 g full range reading and better than 1% linearity within this range with a sensitivity of 0.5 mV/g. The signal detection circuitry is an on-chip switched capacitor charge transfer circuit operating on an internally generated 1 MHz four-phase non-overlapping clock. A dynamic electro-mechanical simulation was carried out for the lumped sensor/circuit model using HSPICE connected in an open-loop arrangement. The simulation takes into consideration the electrostatic forces, the damping force and the applied force due to acceleration. It also allows for simulating the sensor in a closed-loop arrangement.

Key Words: 2-D Accelerometer, Surface Micromachining and Electromechanical Simulation.

To my Parents

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LIST OF SYMBOLS

LIST OF ENGLISH SYMBOLS

Symbol	Description
A	Area.
a	Acceleration.
b	Damping coefficient.
C	Capacitance.
C_0	Sensor capacitance at zero acceleration.
c	Distance from the centroidal axis.
c_1, c_2	Constants of integration.
d_0	Initial distance.
E	Modulus of elasticity in tension and compression (Young's modulus).
F	Force.
F_a	Axial force.
F_e	Electrostatic force.
F_s	Shear force.
f_c	Clock frequency.
g	Earth gravitational acceleration.
H	Heat-transfer coefficient.
h	Height.
I	Moment of inertia.
k_s	Spring constant.
L	Length.
L_A	Anchor side length.
L_B	Buffer isle side length.
L_t	Tether length.
l	Length of tooth.
M	Bending moment.
m	Mass.
m_d	The ratio of the spacing between the plates of the same capacitor to the spacing between the plates of differential capacitors.
n	Number of teeth of the same type on each side.
R	Resistor.
R_f	Feedback resistor.
S	Device span.
t	Thickness.
V	Volume,Voltage.
V_L	Voltage of the left plate.
V_R	Voltage of the right plate.
V_{ref}	Reference voltage.
V_o	Output voltage.
V_0	Voltage of the middle plate.
V_δ	Voltage of the moving plate at position δ.
w	Width.
w_t	Width of tethers.

LIST OF GREEK SYMBOLS

Δ	Change of any designated function.
δ	Deflection.
ϵ_0	Permittivity of free space.
ϵ_r	Relative permittivity (dielectric constant).
P	Density of material.
ρ	Damping factor.
σ_a	Stress due to axial force.
σ_b	Stress due to bending.
σ_{sh}	Shear stress.
Φ	Phase shift.
τ	Time constant.
ω	Angular frequency.
ω_L	Force applied per unit length.
ω_0	Natural frequency.

CHAPTER 1: Introduction

1.1-General View

The idea of micromachined silicon sensors was born as a result of the search for low-priced, light-weight, small and low powered transducers to replace the costly, heavy, bulky and power consuming ones which are standard for use today. In some cases, additional advantages resulted as side effects from miniaturization to add up to their attractive features. The research in this field is still considered to be in its infant stage and it will take years from now to put microsensors in a lead position. As for now, a lot of the research work and funds are being directed to this field, and some experts predict that the market for microsensors for automotive use alone will exceed $3.5 billion by the turn of the century [1].

At the present time, traditional transducers are superior because they are more easily fabricated and much better understood. However, their size, weight and power consumption limit their use, for example, in space program where each extra kilogram increases the launching cost. In biomedical uses, a small sensor size facilitates the insertion of this sensors inside the human body. A lower price makes it more affordable.

In the light of the above discussion, the features listed in Table (1.1) reveal that the micromachined devices are really promising.

In order for the micromachined sensors and actuators to become practical and more widely usable, they must have the following features:

a-Low cost.
b-Small size and light weight.
c-Encapsulation in a single chip with on board electronics.
d-Performance to meet required conditions keeping acceptable sensitivity and linearity with minimum variations due to different operating temperatures.
e-High reliability and durability.

f-Low power consumption.

g-Possibility of fabrication in a standard IC fabrication process before making the final touches.

Although all of the points mentioned above are important, the last point is of special importance. This is because in building up a new technology, new specialized fabrication lines are needed, then the cost of production will increase. Appendix [K] describes some additional features of miniaturized sensors.

Features	Standard piezoelectric pressure transducer	Silicon micromachined capacitive pressure transducer
Diaphragm thickness (um)	100	1
Diaphragm material	Stainless steel or Inconel	Silicon or silicon compounds
Transducer dimensions (mm)	150 x dia 50	7 x 7 x 0.5
Transducer weight (gm)	≥ 750	<10
Power consumption (mW)	≥5000	≤15
Cost ($)	>50	≤10

Table (1.1): Comparison between a standard piezoelectric pressure transducer and a capacitive micromachined pressure transducer [2], [3]

1.2-Sensor Designing Steps

The process of designing a microsensor can be subdivided into the following four tasks:

a-Mechanical design of the sensing element.

b-Electronic design of the signal processing circuit.

c-Choice of the fabrication procedure.

d-Post-fabrication processes.

Each of the mentioned tasks requires thorough investigation and cautious selection of design, materials and implementation method. It takes a group of experts in mechanics, electronics, VLSI and chemical engineering to work as a team in order to produce a new type of microsensors. Each task by itself can impose rigorous restrictions on the others and for this reason, good collaboration among the group members is necessary. The details of these tasks are as follows:

a-Mechanical design of the sensing element: This field requires the study of static and dynamic behavior of the movable part under the encountered forces throughout the frequency range of operation. This is to determine the possible deflection/torsion as a function of the applied forces caused by the measured phenomena, maximum permissible deflection/torsion which sometimes determine the full range reading, the fracture stress that will determine the shock survival, the natural frequency of the system that will decide the bandwidth of the system, and the fatigue stress that might determine the durability of the system. Sensor development often needs a simultaneous optimization of both the electrical and mechanical characteristics of the employed materials. This usually imposes some compromises upon the performance of the sensor and is generally more difficult than optimizing each of them individually.

b-Electronic design of the signal conditioning circuit: This is highly dependent upon the method of sensing, whether capacitive or piezoresistive. In both cases special attention should be paid to the design since piezoresistive sensors suffer from the high temperature coefficient inherent in the piezoresistive materials [4]. Special compensation methods should be utilized to help it operate over a wider temperature range. On the other hand, capacitive sensors need more complicated signal conditioning circuits since the range here is usually less than *1pF* with changes due to the measured phenomena as small as 0.1fF. Such values often make even the parasitic capacitor look big. Stray capacitances should also be considered (at all frequencies), and this makes the hybrid sensor hard to implement. Despite the problems associated with integrating the mechanical device with the electronic circuit, the electromagnetic interference and the stray capacitances make the choice of on-chip signal conditioning circuit of special importance.

c-Choice of the fabrication process: Due to the lack of a standard method for fabricating these sensors, the choice of the fabrication procedure needs to be considered even before the mechanical design is approved. In other words, one can imagine and draw on paper many mechanical designs, but the one that will be chosen is the design which can be

realized by the use of an available fabrication method.

In practice, there are some sensors that have been implemented utilizing a standard CMOS process [5], but these have limited efficiency and most of them do not have moving structures.

d-Post fabrication processes: Post fabrication processes are chemical steps that are often added. The fabrication of micromachined sensors by itself is not a standard process and special processes must be involved in order to set the sensing element free by etching step or steps that follow fabrication and precede the packaging. The available etching processes should also be considered before the mechanical design is approved because certain modifications to the dimensions or materials might be imposed in view of the available etching processes.

1.3-Classification of Microsensors

Microsensors are divided into two basic groups according to the method adopted for sensor fabrication:

a-Bulk micromachined: Here the sensor is formed by etching (isotropically or anisotropically) the required shape into the silicon wafer itself and these sensors are usually anodically bonded to plates of metal coated Pyrex glass to achieve the sensor with full connections. Much higher sensor masses can be achieved out of the 0.5mm thick silicon wafers while double-sided processing is often needed. Double sided processing implies the need for double side polished wafers, special handling techniques and the use of double side aligners. Special bonding techniques might be needed here to bond the wafers to the packaging materials. Another restriction is imposed by thermal stresses. This involves using a glass that has a thermal expansion coefficient equal to that of the silicon so that the bonds will not be broken once the sensor cools down to ordinary temperatures. On the advantage side, anisotropic etching often allows the creation of shapes of very large aspect ratios; short and narrow groves are created with extremely large depth.

b-Surface micromachined: Here the sensor is formed by etching a certain layer of the deposited layers, and then setting it free by etching the layers underneath it. With regard to deposited layers, it should be noted that these are only few microns in

thickness compared to 500 microns of wafer thickness in the case of bulk micromachining. Consequently, surface micromachined sensors usually have the sensor part of much smaller mass and that often is very crucial in determining the operating range of the sensor. Structures of large height can not be achieved in a conventional CMOS or BiCMOS process, and special processes like (LIGA) might be needed. Single-sided processing is often enough. This means the need for simpler equipment and shorter processes. All etching on this level would be isotropic, and this limits the shapes that can be achieved using these methods. Wider choice of material is possible in the case of surface micromachining either as sensor material or as sacrificial layers. Often sandwiches of materials are created such as a layer of polysilicon sandwiched between two layers of SiO_2. LASER beams can be used to create shapes that are impossible to achieve using traditional technology like helical springs or creating vertical beams to support a surface that was already under-etched. LASER beams are also used to carve into a layer that is opaque to the LASER wavelength underneath a surface that is transparent to the same beam. Despite the fancy possibilities that it can create, this LASER growth is based on local heating on the surface ignited by the LASER beam. This means that a very small amount of growth is achieved in an area limited by the cross sectional area of the beam over time, and therefore, these processes are too slow to be considered commercially viable.

1.4-Accelerometers

The focus was put on accelerometers because they are useful devices that find different applications in robotics, aerospace technology, missile control, navigation and automotive fields. For automotive alone, different applications exist for the accelerometers such as air-bag deployment system, active suspension and control/navigation. Each field has its own requirements and operating conditions which might vary from µg to several thousands (g is the Earth's gravitational acceleration) at operating temperatures ranging from below -100°C to more than several hundred °C. The effective bandwidth of the signals to be measured might vary from a few Hz to a few thousand Hz hence, the specific application would determine the properties of the required accelerometer. For example the special requirements for an accelerometer to be employed in an air-bag control system in an automobile are given in Table (1.2). These requirements were set by the Society of Automotive Engineering (SAE).

Measurement range	±100 g
Noise	<1 g
Frequency range	$0 \leq f \leq 1$ kHz
Temperature range	-50°C to 125°C
Damping	Slightly under damped
Accuracy	Better than 5% over the temperature and voltage range
Linearity	Better than 1%
Shock survival	2000 g
Output	High level, buff-ered signal
Self test	yes
E.M.I.	Immune
Simple and easy to use	Yes
Reliability and Durability	Should be very high
Price	<10 $

Table (1.2): SAE requirements for an air-bag accelerometer [6].

1.4.1-Principle of Acceleration Measurement

The principle of an accelerometer is based on Newton's law:

$$F = m \times a \tag{1.1}$$

where m is the mass of a sensor, F is the force exerted on that system, and a is the acceleration with which this system will be moving.

If this force F is applied to a spring, then it will cause a displacement in the spring according to the following elastic model:

$$F = k_s \times \delta \qquad (1.2)$$

where δ is the measurable displacement of the spring, and k_s is the spring constant. Then the acceleration is given by:

$$a = k_s \times \frac{\delta}{m} \qquad (1.3)$$

The acceleration measurement is inversely proportional to the mass which is regarded to be universally constant (for velocities well below the velocity of light). The measured values of acceleration can be integrated to obtain the corresponding velocities, and then the displacements in the direction of the acceleration. This is much easier than the direct measurement of velocity and distance since they traditionally need a reference point to be measured with respect to. From the packaging point of view, accelerometers have the advantage that no physical contact is needed between the surroundings and the interior of the sensor. This gives the freedom of choosing the type of packaging. This tends to be a very serious matter for other types of sensors. Another good feature of the acceleration measurement is that it is easy to use the Earth's gravitational acceleration as a standard value for calibration. All it needs is to align the accelerometer exactly with the vertical direction

Basically a free moving structure is affected by the force induced by the applied acceleration. This effect appears mechanically as bending or torsion depending upon the way in which the microstructure is mounted (whether as beams or torsion bars). This structure is the sensor, while the role of the transducer is to translate the mechanical deformation into a signal that is electrically measurable. This is done either by piezoresistive or capacitive effects [6].

The standard bulky accelerometers are usually based on the piezoelectric effect. In these sensors, a ZnO crystal is connected to the moving part and a piezoelectric signal is generated that is proportional to the applied acceleration. Piezoelectric materials usually need high stresses in order to generate detectable signals (low sensitivity) and that is why these sensors are bulky and need a rather large central mass. The piezoelectric instruments also have a low damping factor which means prolonged oscillation after the end of the applied acceleration [6].

The piezoresistive accelerometers show a high temperature coefficient (around 1%/°C) [6]. This means increased error with the variation of temperature away from the calibration temperature. One way of compensating the temperature effect is to deposit another piezoresistor in an unstrained position, but being on the same chip, it will be affected by the temperature variations and the signal from the unstrained resistor is used for temperature compensation. Despite this compensation, the temperature coefficient remains high and sophisticated compensation techniques are needed to obtain a wider operating range of temperatures. The piezoresistive materials also suffer from hysteresis, drift and creep. This creep appears as dislocations in the structure of the material due to repeated exposures to stresses. As a result, the behavior of the piezoresistive material will change over time as if it was aging.

Because their temperature coefficient is one order of magnitude less and their sensitivity is higher than that of the piezoresistive ones, the capacitive accelerometers are more promising with respect to the required performance over high temperature ranges. The concept is that the measured phenomena (acceleration in this case) causes a change in the value of the capacitance formed between two plates, one of them being fixed, the other forming part of the moving structure. If more accuracy is needed, a differential capacitor may be formed among three plates. The central plate is part of the moving structure, while the other two are fixed. This differential capacitor technique has the advantage of reducing the effect of common capacitors within the circuit such as the parasitic capacitors of the electronic circuit and therefore increases the accuracy.

The problem associated with these capacitive microsensors is the sophisticated signal processing circuitry needed because of the very small values of the involved capacitances (in the range of *pF* or even less). The variations in the capacitance due to the acceleration will be typically in the range of 1-100*fF*. The smaller the capacitor, the more care should be taken, and more important it is to use monolithic accelerometers. In hybrid accelerometers, the wires connecting the sensor to the external electronic circuit give rise to an appreciable stray capacitance that should be considered at all frequencies. A hybrid model will be more susceptible to EMI.

Despite its inherent need for sophisticated circuitry, the high sensitivity and low temperature coefficient are attractive enough to direct most of the current research to capacitive

accelerometers. In fact, capacitive sensors show much smaller aging effect than the piezoresistive ones. This is related to the fact that they both have the same mechanical system, but the structure of the piezoresistors is affected by applied stresses over time that changes their performance and shows up as aging. On the other hand, nothing special usually happens to plates separated by air with frequent use.

Bulk micromachined accelerometers are more suitable for low values of acceleration due to their relatively high masses. Some are reported to operate in the µg range. On the other hand, surface micromachined accelerometers can reach the range of few thousands of g because of their low masses.

1.4.2-Previous Work in the Accelerometer Field

Different types of accelerometers have been reported to be fabricated and tested in laboratories. An example of each distinct type will be given depending upon the method of fabrication, the principle of sensing, and structure or method of detection.

In 1982, Petersen et al. [7] reported a surface micromachined capacitive accelerometer that has a range 10^{-2}-10 g. It is of a simple cantilever type and has a sensitivity of 2.2 mV/g and a 3 dB frequency of 2.2 KHz. The chip size is 24 mm^2. A very simple charge to voltage circuit is used as a detection circuit.

In 1983, Rudolf [8] reported a bulk micromachined capacitive accelerometer. The proof mass was supported by a couple of torsion bars situated on opposite sides. It has a 3 dB frequency of 200 Hz, and a chip size is 1.5x2.6 mm. No on-chip circuitry is implemented.

In 1987, Rudolf et al. [9] reported a bulk micromachined capacitive accelerometer that has 4 ranges of measurement 0-10^{-3}...0-1 g. The proof mass is supported by two torsion bars situated on opposite sides. It achieved a sensitivity of 10^3 V/g at the highest sensitivity range, and had a 3 dB frequency of 100 Hz at the same sensitivity. The chip size is 7.5x4.5 mm. A simple capacitive bridge is used as a detection circuit.

In 1988, Barth et al. [10] reported a bulk micromachined piezoresistive accelerometer that has a range of 0.5-100 g. The proof mass is supported by two identical cantilevers situated on the same side. It achieved a sensitivity of 10 mV/g and a 3 dB frequency of 500 Hz. The chip size is 3.4x3.4 mm. A compensated resistor bridge is used as the signal condi-

tioning circuit.

In 1989, Satchell et al. [11] reported a thermally-excited, bulk micromachined, piezoresistive accelerometer that has a range of 0-30 g. The proof mass is shaped like a double-ended tuning fork. It achieved a sensitivity of 13.2 Hz/g. The chip size is 7.5x5.8 mm. The detection of motion is achieved by two piezoresistive strain gauge.

In 1990, Suzuki et al. [12] reported a bulk micromachined capacitive accelerometer that has a range of 0-1 g. The proof mass is supported by a simple cantilever. It has a sensitivity of 1040 mV/g and a 3 dB frequency of 100 Hz. The chip size is 3x4.5 mm. A Pulse-Width Modulation (PWM) circuit in a closed-loop arrangement is used as the signal conditioning circuit.

In 1990, Yamada [13] reported a bulk micromachined piezoresistive accelerometer that has a 0-2000 g dynamic range. The proof mass is supported by 4 cantilevers one on each side. It has a sensitivity of 0.02 mV/g/V and a 3 dB frequency 500 Hz. The chip size is 5x3.5 mm. No on-chip circuitry is implemented.

In 1990, Rudolf et al. [14] reported a μg resolution bulk micromachined capacitive accelerometer that has a range of ±0.1 g. The proof mass is supported by two identical cantilevers situated on the same side. It achieved a sensitivity of 5 V/g and a 3 dB frequency of 100 Hz. The chip size is 8.3x5.9x1.9 mm. A self-adjusting capacitive bridge is used as the signal conditioning circuit.

In 1990, Seidel et al. [15] reported a bulk micromachined capacitive accelerometer that has a range of ±5 g. The proof mass is supported by highly symmetrical 8 cantilevers, 4 on each face, one on each corner. It has a 3 dB frequency of 3.3 KHz at reduced pressure. The chip size is 3.5x3.5 mm. A switched capacitor charge transfer circuit is used as the signal conditioning circuit.

In 1992, Nagata et al [16] reported a bulk micromachined capacitive accelerometer that has a range of 0-40 g. The proof mass is supported by 4 cantilevers, one on each side. It achieved a sensitivity of 90 mV/g and a 3 dB frequency of 500 Hz. The chip size is 4x1.3 mm. A capacitance PWM circuit in an open-loop arrangement is used for signal conditioning.

In 1992, Sherman et al. [17] reported a surface micromachined capacitive accelerometer that has a range of 0-50 g. The proof mass is supported by 4 cantilevers one on each side. It has a 3 dB frequency of 1 KHz. The chip size is 120x120 mil^2. A capacitor frequency modulation circuit in a closed-loop arrangement is used as the signal conditioning circuit.

In 1992, Roger et al. [18] reported a surface micromachined capacitive accelerometer that has a range of 0-2 g. The proof mass is supported by 4 U-shaped cantilevers, one at each corner. No data is available to define the sensitivity or the cut-off frequency. The chip size is 2.5x5 mm. A Σ-Δ modulation circuit is employed in a closed-loop arrangement for signal detection.

Many other micromachined accelerometers have been reported, but only one surface micromachined accelerometer is commercially available which is the ADLX50 that was introduced by Analog Devices Semiconductor. This indicates how difficult it is to build a commercially suitable micromachined accelerometer despite the huge research effort that has been put into the work. The ADLX50 was basically designed to comply with the requirements set by the SAE for the utilization in the deployment of an air bag in an automobile. No actual data are available concerning the yield of the sensor-production process nor its reproducibility which are important factors in any successful process.

1.5-Problem Statement

In some applications, such as robotics, navigation systems, automotive....etc., a 2-D measurement of acceleration is required. The common practice is to utilize 2 separate accelerometers normal to each other. A processor is then used to triangulate the resulting signals.

With integrated accelerometers, alignment is not an easy task and alignment of two accelerometers normal to each other is even more difficult. Also from the cost point of view, a single chip, 2-D accelerometer is cheaper than a 2-D accelerometer system based on a couple of 1-D accelerometers.

There is no single-chip 2-D micromachined accelerometer available in industry. Also the only industrially available surface micromachined accelerometer is 1-Dimensional and implemented in a BiCMOS process then:

The objective in this thesis is to design and implement a single-chip, 2-D accelerometer. The chip should be implemented in an available CMOS process. If the available processes were not suitable, then suggest minimum modifications to the selected process.

1.6-Contribution of the Thesis

1-A single chip 2-D surface micromachined accelerometer is designed.

2-The Mitel 1.5 μm CMOS process flow has been modified with minimum number of additional masks to achieve the task.

3-Simulation programs have been written for a-The electrical subsystem. b-The mechanical subsystem. c-The combined electromechanical system. All programs are written in HSPICE.

1.7-Thesis Outline

a-Chapter 2: This chapter gives complete static design specifying all the necessary dimensions. These dimensions are extracted based on an optimization procedure.

b-Chapter 3: This chapter describes the electrical design for the signal conditioning circuit supported by HSPICE simulation to verify the performance of the suggested circuit.

c-Chapter 4: This chapter gives the definition of the process steps required to achieve this sensor in addition to the necessary modifications needed to be applied to the process. The issues to be taken into consideration in the construction of the process sequence are also explained. Listing of the post fabrication steps needed to set the movable structure free is included.

d-Chapter 5: This chapter presents a method to integrate the mechanical and electrical systems into a single representation and simulation using HSPICE.

e-Chapter 6: This chapter presents the simulation results and the conclusions.

CHAPTER 2: Mechanical Design of Accelerometer

The mechanical design of an accelerometer consists of the following steps that should be carried out sequentially and often iteratively:

2.1-Static Behavior of the Sensor

The mechanical design of the proposed sensor, is based on the same basic structure as the ADLX50 but with modifications to make it work in two dimensions instead of only one. Figure (2.1) shows the basic mechanical structure of the sensor including the differential capacitor scheme.

The deflection in a cantilever due to a force acting at its free end is given by:

$$\delta = \frac{l_t^3}{3 \cdot E \cdot I} F_s \qquad (2.1)$$

where δ is the deflection due to shear force, l is the beam length, E is the Modulus of Elasticity, I is the Moment of Inertia and F_s is the applied shear force.

The moment of inertia, I in this case is given by:

$$I = \frac{t \cdot w_t^3}{12} \qquad (2.2)$$

where t is the beam thickness and w_t is the beam width.

Substituting Equation (2.2) into Equation (2.1) gives:

$$\delta = \frac{4}{E \cdot t} \cdot \left(\frac{l_t}{w_t}\right)^3 \cdot F_s \qquad (2.3)$$

On the other hand, the relative change in length, ε caused by the axial force is given by:

$$\frac{\Delta l_t}{l_t} = \frac{\sigma_a}{E} = \varepsilon \qquad (2.4)$$

where σ_a is the stress due to axial force and is given by:

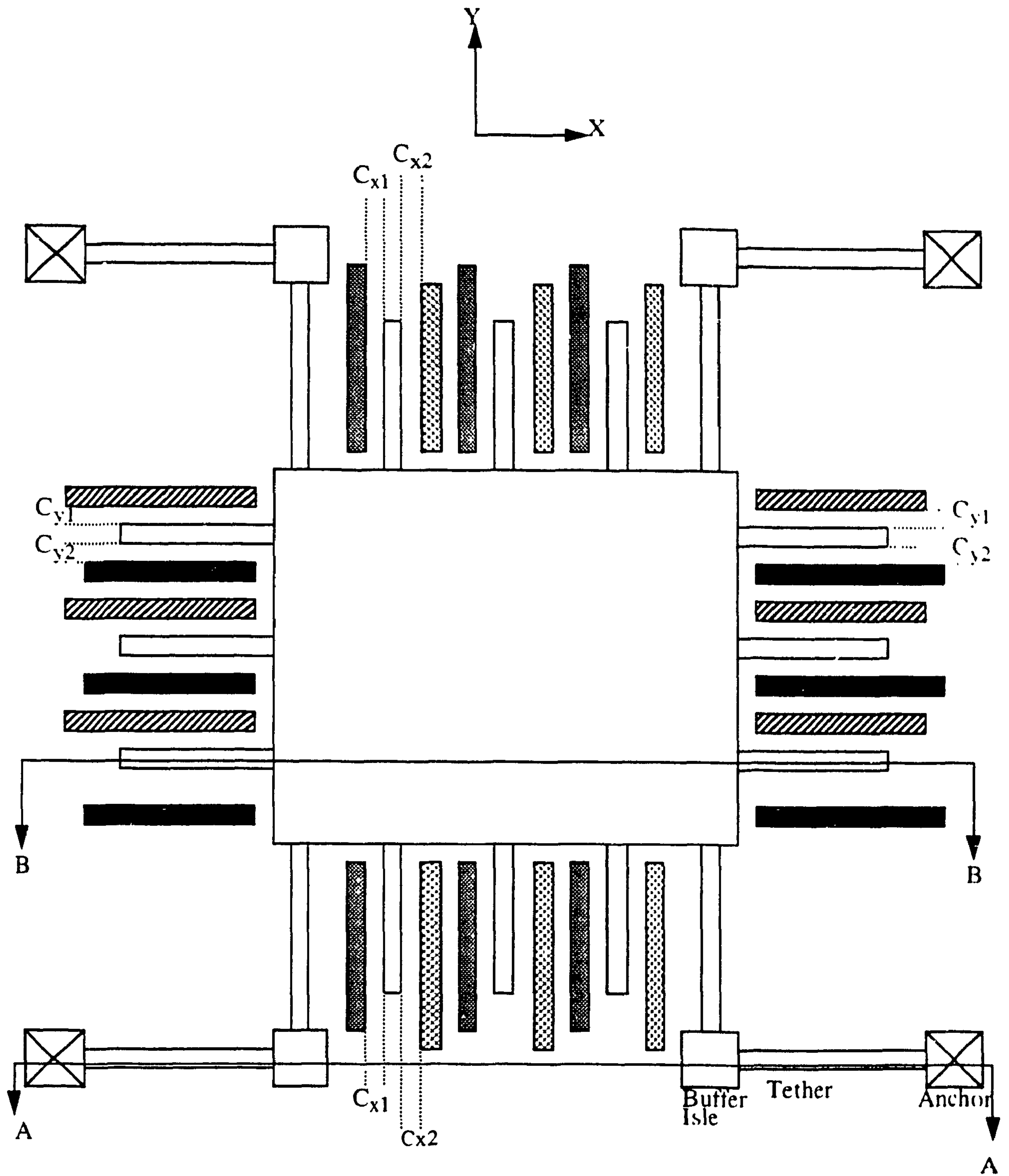

Figure (2.1): The basic mechanical structure of the sensor.

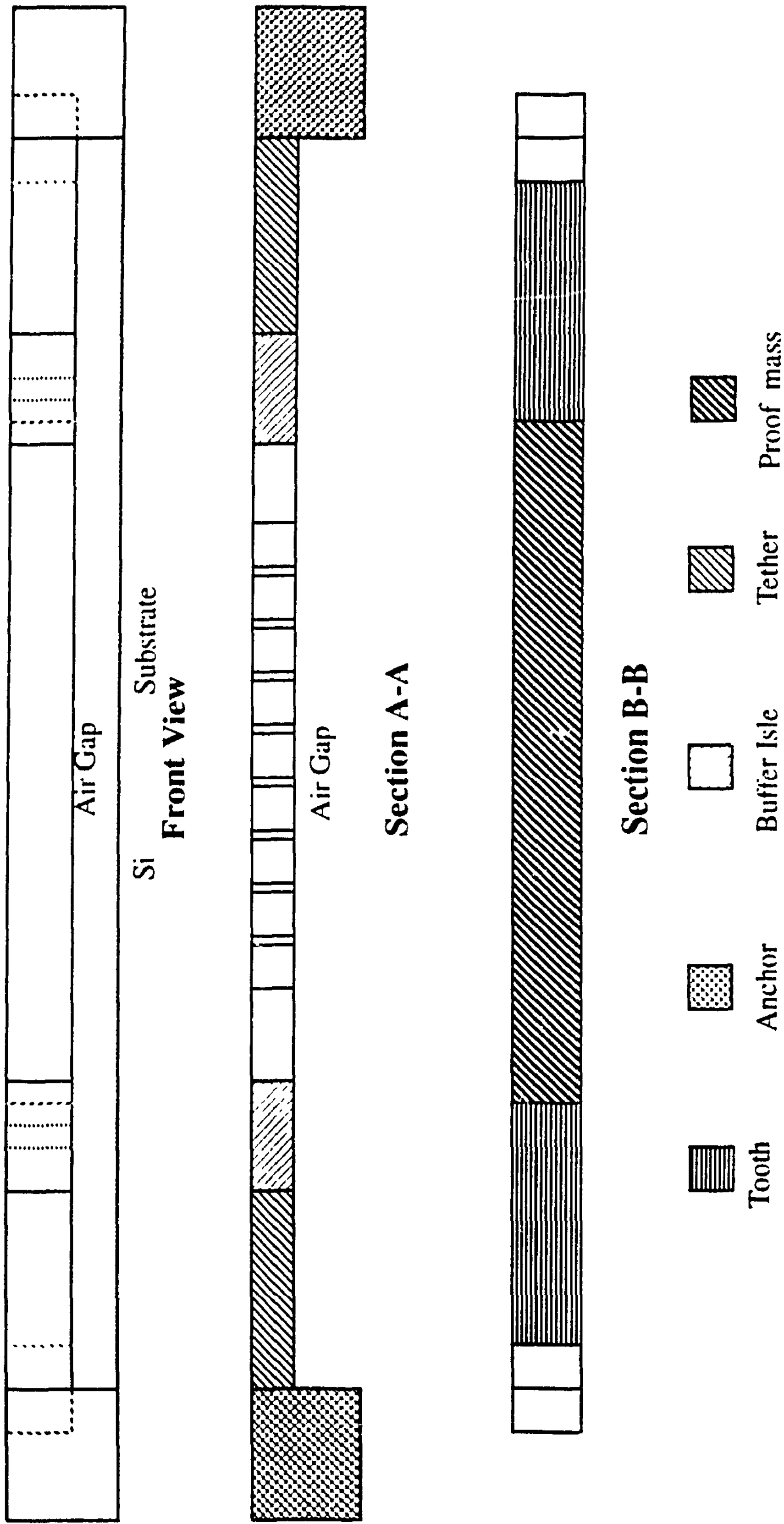

Figure (2.1): *Continued*

$$\sigma_a = \frac{F_a}{t \cdot w_t} \tag{2.5}$$

where F_a is the applied axial force as illustrated in Figure (2.2). This means that the compressive/tensile change in length is given by:

$$\Delta L = \frac{1}{E \cdot t} \cdot \frac{l_t}{w_t} \cdot F_a \tag{2.6}$$

Hence, the ratio of the bending to the compressive/tensile displacement is given by:

$$\frac{\delta}{\Delta l_t} = 4 \cdot \left(\frac{l_t}{w_t}\right)^2 \tag{2.7}$$

The structure is a mass of thick polysilicon. The choice of polysilicon as a material will be discussed later in Chapter 4. It is free to move in both X and Y directions simultaneously while each cantilever of the composite tether will be essentially affected by the shear force exerted on it while the influence on the orthogonal cantilever will be axial. Typical values for the aspect ratio (l_t/w_t) are more than 10. According to Equation (2.7), this will give a ratio of more than 400 between the deflection in the cantilever subjected to the shear force to the change in length in the cantilever subjected to the same force axially. This shows that the deflection will dominate the response of the mechanical system.

The four tethers are fixed mechanically (not electrically) to the substrate at the anchors. The clearance between the proof mass of the moving sensor and the substrate underneath it is an air gap.

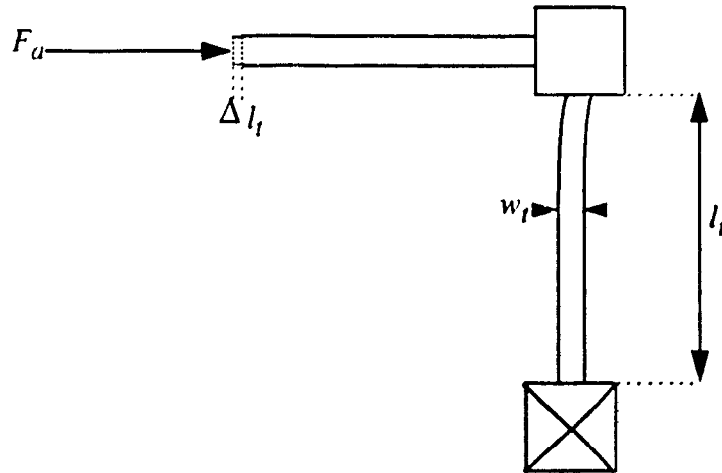

Figure (2.2): *A composite tether subjected to a force.*

From Equation (2.3), it is clear that it is possible to increase the mechanical sensitivity of the sensor by:

a-Increasing the mass of the sensor.
b-Increasing the length of the tethers.
c-Decreasing the width of the tethers.
d-Decreasing the thickness of tethers.

Increasing the mass of the sensor will increase the sensitivity in all directions including unwanted one(s). Besides, increasing the weight would decrease the natural frequency of the mechanical system according to Equation (2.8).

$$\omega_0 = \sqrt{\frac{k_s}{m}} \quad (2.8)$$

where k_s is the spring constant of the system and for a 4-cantilever system like this is defined by:

$$k_s = \frac{F_s}{\delta} = E \cdot t \cdot \left(\frac{w}{L}\right)^3 \quad (2.9)$$

Also, increasing the mass would increase the deflection of the proof mass due to its own weight and consequently decrease the gap between the proof mass and substrate to an extent that they might come into contact and friction might result.

Increasing the length of the tethers would decrease the spring constant, k_s and consequently reduce the natural frequency. Increasing the length would also increase the sensitivity in all directions including the unwanted one(s). In addition to these problems, there are practical limitations to the length of the tethers. These limitations are imposed by the mechanical properties of the polysilicon used to create these tethers. More details about these problems will be given in Section (2.3.2) and Appendix [C].

Decreasing the tether width will also decrease the spring constant mainly in the X and Y directions and therefore, the natural frequency will be reduced. This also increases, to a lesser extent, the sensitivity in the unwanted Z. There is a technical problem in decreasing the width due to the process tolerance. When the width is reduced close to the process minimum dimension, any contraction along the length of the beam would form a stress concentration point that might jeopardize the performance of the whole sensor.

In order to preserve the linearity of the capacitive sensors within 1% as specified in Table (2.1), the full scale reading change in capacitance should not exceed 10% of the value of the capacitance at zero acceleration (See Appendix [A]). Any capacitance-measuring circuit has limited sensitivity. As a result, it can not detect a change in capacitance unless it is above a certain threshold value. If high resolution is desired then intermediate values between zero and 10% change in capacitance should be measurable say 1% for example. In order for this 1% to be measurable by the existing measurement circuitry, it must be above the circuit threshold value. This implicitly imposes a minimum on the total capacitance of the sensor at zero acceleration (zero-acceleration capacitor).

There are three ways to increase the capacitance:

a-Increase the dielectric constant.
b-Decrease the spacing between plates.
c-Increase the surface area.

Increasing the dielectric constant could, hypothetically, be done by imposing liquids of high dielectric constants in between the plates. However, these liquids have very high viscosity that would forbid the small mass of the sensor from moving even under high acceleration. Gases in general have dielectric constant close to unity due to their low density. Adding layers of high dielectric materials is ruled out, because it is not practiced to add layers in the horizontal direction and even if this is done, it will increase the zero acceleration capacitance without affecting the absolute change in capacitance. The spacing between the plates has its minimum value determined by the fabrication process. By process of elimination, the only option left to play with is the surface area.

2.2-Dynamic Behavior of Sensor

The dynamic response of the sensor consists of basically the transients through which the sensor goes before reaching its equilibrium position. When a periodic acceleration (non DC) is acting on the device, the spring, mass system of the sensor can be treated as a forced oscillator [20]. This oscillator changes kinetic energy into potential energy and vice versa. Then the equation of motion would be in the form:

Decreasing the thickness of the tethers (assuming that the proof mass will sustain the high thickness) would decrease the natural frequency. What is more important is that it will increase the sensitivity in the unwanted Z direction to a higher proportionality than in the wanted X and Y and that is one of the reasons, the realization of reliable polysilicon sensors require thick polysilicon layers.

$$a(t) = \frac{d^2\delta}{dt^2} + 2\rho\frac{d\delta}{dt} + \omega_0^2\delta \qquad (2.10)$$

where δ is the displacement away from the center of equilibrium, $a(t)$ is the acceleration as a function of time, ω_0 is the natural frequency of the undamped system and ρ is the damping factor.

The amplitude $A(\omega)$ of the sensor displacement is a strong function of the applied frequency (of the acceleration signal) and is given by:

$$A(\omega) = \frac{a(\omega)}{\sqrt{(\omega_0^2-\omega^2)^2 + 4\rho^2\omega^2}} \qquad (2.11)$$

And there is a phase shift, Φ which is given by:

$$\Phi = \operatorname{atan}\left(\frac{2\rho}{\omega_0^2-\omega^2}\right) \qquad (2.12)$$

This gives zero phase shift for $\omega=0$ and 90^0 for $\omega=\omega_0$. $A(\omega)$ depends strongly on the input frequency showing a peak at $\omega=\omega_r$ which is not the first natural frequency of the undamped system and this effect is due to damping.

For a given natural frequency, it is possible to minimize the frequency dependance when the sensor works near its periodic limit, i. e. when the damping to natural frequency is near unity [20]. The amplitude versus frequency no longer shows a resonance peak but still decreases with frequency (critically damped response).

The analysis mentioned above is based on the assumption that the damping force is proportional to the relative velocity of the moving object with respect to the medium and it is mainly caused by the fluid drag force. In practice, this will be true only if the relaxation

time of the fluid is much shorter than the excitation time, but when these two times become comparable then certain modifications should be applied to the model.

Concerning damping, there are two requirements. In the unwanted directions, the structure should have as high damping as possible. In the wanted directions, the moving structure needs to have controlled damping to a certain natural frequency so that the critically damped behavior is achieved (and since it is very hard to achieve in practice then a slightly under-damped system is selected). This ensures high-fidelity acceleration transduction with minimum distortion caused by the frequency response of the sensor structure [21].

The common practice is to avoid strongly over-damped and strongly under-damped situations. The over-damped means the signal decreases strongly with frequency near the resonance frequency and in the case of step-like excitation, the signal only reaches its final value very slowly. The under-damped means large overshoot near the resonance frequency and prolonged oscillation after the end of excitation.

The idea of fluid damping is not new and it is widely employed in large machinery. In this case, what will be the source of damping? This accelerometer is a quadratic cantilever structure, where the mass is supported through polysilicon springs and moves like a piston. This piston tends to compress the fluid surrounding it depending upon the direction of movement. The fluid trapped between the moving piston and the substrate will resist the compression and tend to obtain pressure balance by travelling around the piston to the other side of the cavity [21]. This travel will take place in the narrow gap between the moving structure and the substrate in a viscous flow that will be strongly dependant upon the viscosity of the fluid. The damping effect of this fluid is usually referred to as "squeeze film damping" [22]. For small changes in displacement, this effect is linear, but for large changes (high amplitudes of acceleration) this linearity will be lost. In this special case, it is an important objective to increase this squeeze film damping so it will work to protect the sensor from being smashed into the substrate by a strong shock in that direction. In order to get consistent response in the wanted directions, the needed fluid should show very small changes in viscosity over the temperature range of operation. For this reason, oils and liquids in general are not suitable for use since they exhibit very wide viscosity change with temperature and gases would be the right choice. For simplicity and in order to avoid the need to have a leak-tight structure, air would be the most practical choice. Air has a relatively constant viscosity over temperature and pressure near the normal atmo-

has a relatively constant viscosity over temperature and pressure near the normal atmospheric ranges. The temperature dependance of viscosity of air is less than 0.2% which means only ±15% change from -30C^0 to +75C^0 [22].

Shape of the moving structure, the clearance between the moving structure and its surrounding and the pressure of air inside the cavity are all important factors that affect the damping and they can be used to control it especially the air pressure inside. Controlling the pressure means the sensor should be sealed at that certain pressure which is a costly and laborious process.

In some accelerometer designs, the designer resorts to change the shape of the moving part. U.E. Gerlach-Meyer [21] made a study on the effect of introducing slits inside the moving structure in order to shorten the flow path of air and consequently the relaxation time. Increasing number of slits proved to reduce the damping. On the other hand, this approach increases the complexity of fabrication procedure and also tends to degrade the mechanical properties of the sensor. In this case and since this design is a surface micromachined sensor, then for the sake of cutting down the etching time, some openings were introduced to reduce the time needed for the etchant to travel underneath the structure. These openings will invariably reduce the damping.

The other choice is to vary the air gap between the moving part and the substrate which gives good control over the damping in the dynamic mode. Decreasing the gap will increase the damping and vice-versa. This is an invitation to some undesired static problems where a steady high acceleration in the Z direction might very well bring the moving structure into friction with the residuals of the sacrificial layer where removing the sacrificial layer might not be fully developed or even worse come into contact with the substrate and hinder its movement in the X and Y directions.

The problem of damping of accelerometers was one of the first problems that had been studied in order to achieve the best solution. Roylance [23] discussed this problem in detail and investigated a number of options to achieve the correct damping. He deduced that an accelerometer with a quality factor of 10 will, when driven at resonance, deflect ten times more than it will when driven by the acceleration at lower frequencies. Under such conditions, the chance of breaking the device increases and the necessity of controlling the damping becomes more obvious.

Since the structure is only 2 μm thick, then drag force exerted on it when it moves in the X and Y directions are much lass than the drag forces in the Z direction. This means the chance of having the mechanical system underdamped in these directions. (Note that there is inherent electrical influence upon damping in X and Y directions and this effect will be discussed later in the electrical design).

2.3-Detailed Design

The process of the detailed design can be extensive without some constraints because of the vast number of alternatives that might lead to the goal. However, the process parameters and limitations often represent some inevitable constraints.

2.3.1-Design Optimization

The comb shape of the structure seems to be convenient to increase the surface area that forms the capacitors. Figure (2.3) shows the detailed section of one of the teeth and a sector of the moving structure.

The zero acceleration capacitor, C_0 is obtained by considering the capacitance between two parallel plates and is given by:

$$C_0 = \frac{\varepsilon \cdot A}{d_0} \Rightarrow A = \frac{C_0 \cdot d_0}{\varepsilon} \qquad (2.13)$$

Note that there always will be some fringing capacitances. However, in this case, it is hard to evaluate it since the surfaces of the plate are not even really parallel to each other (due to the nature of etching process) and any formula other than measuring the implemented capacitor will end up in some inaccuracy. For this reason, the ideal case was taken and the analysis was built on it.

The area, A is the sum of the surface areas of the teeth contributing to the capacitor under consideration as illustrated by Figure (2.3) is given by:

$$A = 2 \cdot n \cdot l \cdot t \Rightarrow n = \frac{A}{2 \cdot l \cdot t} \qquad (2.14)$$

where n is the number of teeth on each of the two sides contributing to the capacitor, l is the length of the tooth, and t is the height of the tooth (thickness of the polysilicon).

The total length of the sensor body excluding the added teeth at the two ends, L as illustrated by Figure (2.3) is given by the following:

$$L = n \cdot [3w + 2d_0 + m_d \cdot d_0] \qquad (2.15)$$

where w is the width of the tooth, d_0 is the spacing between teeth and m_d is the ratio of the spacing between the plates of the same capacitor to the spacing between the plates of differential capacitors.

Substitute for n from Equation (2.14) and for the area, A from Equation (2.13) into Equation (2.15) results into:

$$L = \frac{C_0 \cdot d_0}{2 \cdot \varepsilon \cdot l \cdot t}[3w + (m_d + 2) \cdot d_0] \qquad (2.16)$$

The total device span S is given by:

$$S = L + 2 \cdot l \qquad (2.17)$$

Now substitute for L from Equation (2.16) into Equation (2.17) results:

$$S = \frac{C_0 \cdot d_0}{2 \cdot \varepsilon \cdot l \cdot t}[3w + (m_d + 2) \cdot d_0] + 2 \cdot l \qquad (2.18)$$

Differentiating S with respect to l results:

$$\frac{dS}{dl} = \frac{\partial}{\partial l}\{\frac{C_0 \cdot d_0}{2 \cdot \varepsilon \cdot l \cdot t}[3w + (m_d + 2) \cdot d_0] + 2 \cdot l\} \qquad (2.19)$$

From Equation (2.19), define a lumped factor, K which is not function of l as follows:

$$K = \frac{C_0 \cdot d_0}{2 \cdot \varepsilon \cdot t}[3w + (m_d + 2) \cdot d_0] \qquad (2.20)$$

Substitute for K in Equation (2.19) and complete the differentiation. The first and second

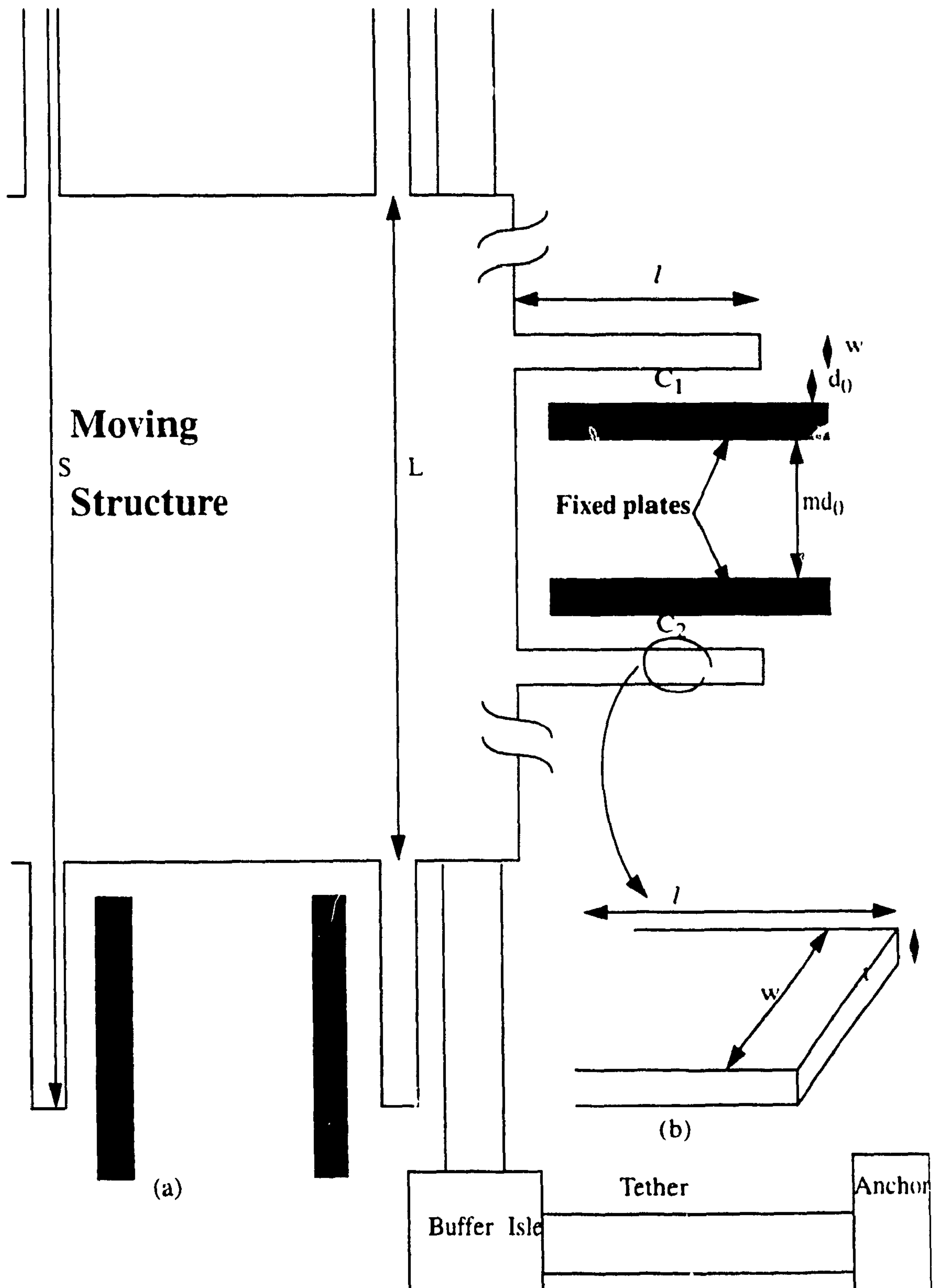

Figure (2.3): *(a) A sector of the moving structure.*
(b) A detailed tooth of the comb capacitor.

derivatives will be:

$$\frac{dS}{dl} = \frac{-K}{l^2} + 2 \Rightarrow \frac{d^2S}{dl^2} = \frac{2 \cdot K}{l^3} \qquad (2.21)$$

Note that the second derivative is always positive since all the components of K are positive and that means whatever value has the root of the first derivative, would be a global minimum of the function and it is given at:

$$\left.\frac{dS}{dl} = 0\right|_{l = \sqrt{\frac{K}{2}}} \qquad (2.22)$$

The tooth length, l is now defined in terms of K. With the objective to minimize the device span, S as possible, then K should be minimized.

2.3.2-Optimum Design Parameters

From Equation (2.20), to minimize K, the parameters affecting it should be investigated. The sensor capacitance at zero acceleration, C_0 seems to be a good point to start at and base the calculations on. Analysis, supported by HSPICE simulation revealed the value of 100 fF as a reasonable value for C_0. It is a compromise among the many conflicting factors discussed before. The value of C_0 will be discussed further from the electrical point of view in Section (3.2).

As far as the separation between capacitor plates, d_0 is concerned, it is clear that the more it is reduced, the more S is reduced. Since it is the separation between two poly lines, then it can be taken as the process minimum (1.5 µm). Since some of the teeth are parts of the moving structures then a safety factor should be considered in the prototype and some 30% of the process minimum should be added and d_0 is taken as 2 µm. If the process minimum (1.5 µm), proved in the implementation to be safe, then it would be advantageous to apply it. This will help increase the sensitivity and reduce the size of the device.

As was discussed before, the permittivity of the medium, $\in$ is a constant and almost equal to the permittivity of the space ($\in_0$=8.854x10^{-12} Farad/m).

As far as the thickness of the layer (the height of the teeth), t is concerned, it is clear both

from the discussion in Section (2.1) and Equation (2.20) that it is an asset to have thicker layers but for technical reasons related to the process of growing and patterning these layers, then a 2 μm limit seems to be a good compromise. Once the teeth length, l is estimated then the value of t=2 μm thickness should be checked against bending, in the Z direction, due to possible shocks.

Since w is the width of these teeth, then it is possible take it as the process minimum provided that it copes with the forces applied on these teeth. At the first glance, one would suggest that these teeth are only subjected to forces due to their own mass and applied acceleration while further investigation has shown that these teeth are also subjected to the electrostatic force present between the plates of a capacitor [19]. This finding requires taking into account the deflection in these teeth both due to the acceleration and electrostatic forces (Assuming that the built-in stresses were relieved by the annealing step). Due to the important influence of the process tolerances on the width of the teeth, local stress concentration points can be created and that might lead to the failure of one or more of these teeth. This might be enough to get the whole sensor stuck in place. For this reason a 30% safety factor had been taken and the width was set to be 2 μm.

The final parameter to look at is the multiplication factor, m_d. In order to reduce the interaction between the differential capacitors then m_d should be as large as possible. The capacitance arrangement is a differential capacitance and the circuit (this will be described later in Section 3.1) is built to suppress the common capacitors. Consequently, the distance can be taken to be the process minimum. For the same safety considerations, mentioned earlier, it will be taken as much as d_0 and therefore m_d will have the value of unity.

Substituting all these values in Equation (2.22) results in the value of $\boldsymbol{K=6.777\times10^{-8}m^2}$.
Substituting for this value in Equation (2.21) results in the value $\boldsymbol{l}$**=184 μm.**
Substituting for $\boldsymbol{l}$ in Equation (2.16) results in $\boldsymbol{L}$**=368 μm.**
Substituting for **L** in Equation (2.17) results in $\boldsymbol{S}$**=736 μm.**
Substituting for **L** in Equation (2.15) results in $\boldsymbol{n}$**=31.**

Now that there is a first estimate about the dimensions of the moving structure (does not include the tethers yet), the next step is to go back and check the compatibility of l, w and t with the forces exerted upon them.

a-Compatibility of results with forces in Z direction due to an applied acceleration in that direction. A shock of 2000 g will be used as a standard shock survival test as given in Table (1.2). At least, it should be made clear whether these teeth would be smashed by hitting the substrate or not. For this analysis, the model of a cantilever will be used as illustrated by Figure (2.4). At the free end, the maximum bending δ_{max} is given by:

$$\delta_{max} = \frac{\omega_L \cdot l^4}{8 \cdot E \cdot I} \qquad (2.23)$$

where ω_L is the force applied per unit length which is given by:

$$\omega_L = \rho \cdot a \cdot w \cdot t \qquad (2.24)$$

where ρ is the density of the material and a is the applied acceleration.

Taking the same value considered before for w and t and substituting for $E=1.6\times10^{11}$ Pas [24] and for a maximum shock of 2000 g, the maximum bending δ_{max} is given by: $\delta_{max}=0.1213\ \mu m < 1.5\ \mu m$. This 1.5 µm represents the thickness of the sacrificial layer and would be reflected on the final device as the spacing between the moving structure and the substrate. The thickness of the sacrificial layer will be discussed later in further details in Section(4.3.2).

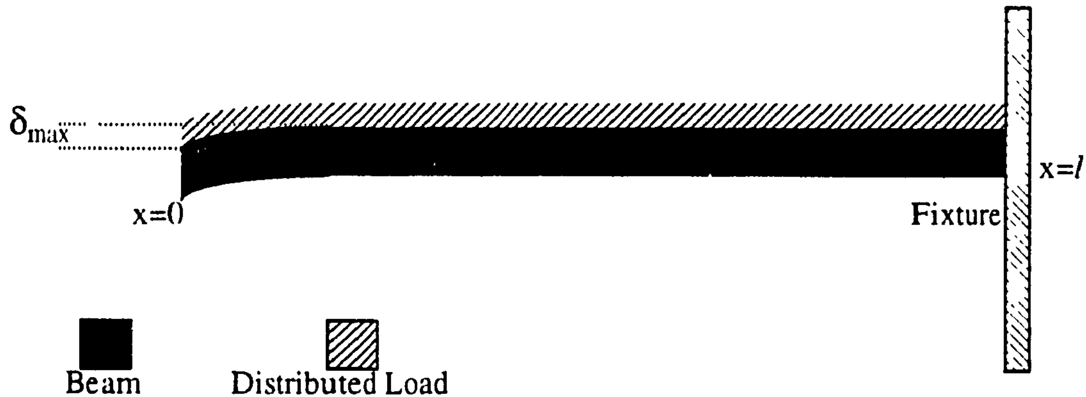

Figure (2.4): *A cantilever subjected to a uniform loading.*

While experiencing the 2000 g shock, there is also a chance that the stresses at the fixed end of the tooth (where maximum shear stress appears in a cantilever) would exceed the fracture stresses. There are two different components contributing to that maximum shear stress. The first would be the shear stress due to the shear force while the other is due to the bending. The stress due to bending will appear in two different directions depending

upon the direction of bending. If bending occurs downwards then the fibers on the top surface of the cantilever will suffer from tension while the fibers on the bottom surface of the cantilever will suffer from compression. This effect will appear in its peak on the outermost fiber [25]. Stress due to bending is given by:

$$\sigma_b = \frac{M}{I} \cdot c \qquad (2.25)$$

where σ_b is the stress due to bending, M is the bending moment at the section, c is the distance from the centroidal axis of the beam to the outermost fiber and I is the moment of inertia of the section with respect to its centoidal axis as defined by Equation (2.2).

The centroidal axis is the axis around which the first moment of the area is equal to zero. In other terms, if a section was supported on a sharp edge that runs across its centroidal axis, then this section would be balanced. For a uniform section like a square (which is the case for the teeth), this axis is the middle line between the upper and lower edge of the section.

The maximum shear stress, S_{max} is given by [25]:

$$S_{max} = \sqrt{\left(\frac{\sigma_b}{2}\right)^2 + \sigma_{sh}^2} \qquad (2.26)$$

where σ_{sh} is the shear stress.

For the teeth, the bending moment, in the Z direction, is due to their own weight only. Hence, this moment M is given by:

$$M = \rho \cdot a \cdot w \cdot t \cdot \frac{l^2}{2} \qquad (2.27)$$

The shear stress at the end of the cantilever is given by:

$$\sigma_{sh} = \rho \cdot a \cdot l \qquad (2.28)$$

Substituting for all the tooth parameters and for a=2000 g in Equations (2.28), (2.27) (2.25) and (2.26) respectively results in the following:

$\sigma_{sh} = 8.3 \times 10^3$ Pas.

M=3.056x10^{-12} N.m.

σ_b=2.3x10^{6} Pas.

S_{max}=1.154x10^{6} Pas.

Dividing the value of the maximum shear stress by the modulus of elasticity gives the value of maximum shear strain, $\in_{max}$=0.00073%. This value of the maximum shear strain is much less than the fracture strain reported for polysilicon as will be discussed later in Section(4.3.1).

This design then proved that, these teeth will not hit the substrate even under a shock of 2000 g nor will they exceed the maximum shear stress of polysilicon under the same shock conditions.

b-Compatibility of results with forces in X or Y direction due to applied accelerations. In the ideal case, these teeth are not supposed to deflect neither in X nor in Y direction. However, in the real case, they undergo some deflection due to their own mass subjected to the applied acceleration. It is required to ensure that the average deflection of these teeth should be much less than the deflection of the tethers or else the linearity of the system will be much worse than the design value. This is applicable within the defined range of acceleration. Outside that range, the readings are due to be ignored in any case. In fact, outside the linear region, more attention should be paid to the shock survival rather than the linearity.

For the sake of deflection measurement in X and Y directions, Equation (2.23) is still applicable and so are Equations (2.2) and (2.24). The only modification needed to be made is to make the values of t and w exchange places. Since they have the same value (only in this special case) then no real modification is to be done. The linear range of this accelerometer is expected to be ±100 g at which the tethers deflection would be ± 0.2 μm which is ± 10% of the clearance between the capacitor plates.

Applying the same values used in part (a), this time with a=100 g gives the value of the deflection at the free end of the tooth (maximum deflection across the tooth) to be δ=6.06 nm which is compared to 0.2 μm represents 3% of the corresponding displacement of the system. However, what is important is the average deflection of the tooth rather the maximum. It is already known that the deflection of the cantilever due to its own weight is pro-

weight is proportional to the fourth power of the length. According to Appendix [B], the average deflection is only 40% of the maximum deflection. This makes the average deflection only 1.2% of the system displacement. When the tooth is deflected to a certain direction then the counter tip of the counter plate of the capacitor subjected to the same acceleration would be deflected in the same direction. This will reduce the influence of their deflection upon the linearity even more.

c-Compatibility of results with forces in X or Y direction due to the electrostatic forces present from the voltages applied to the capacitor plates. These forces are nonlinear and vary with $1/d^2$. Their effect is strongly dependant upon the circuit performance. These forces also are proportional to the second power of the voltage difference between the fixed plates and the movable center plate. The voltage of the center plate itself changes with its position causing electrostatic voltages associated with its voltage and position (in open-loop arrangement) and with its voltage only (since the position is almost fixed in closed-loop arrangement). The maximum electrostatic forces exerted on each tooth (under normal operation) were found to be of the same order of magnitude of the mechanical forces caused by the mass of the tooth at full-scale acceleration 100 g. According to part (a), the stresses exerted on these teeth, in the Z direction under a shock of 2000 g were checked and still were found to be safe. Remember that the teeth have equal width and thickness. This gives them the same mechanical properties both in Z direction and the direction parallel to their width (whether X or Y depending on their orientation). This means that no danger to the teeth is expected from the electrostatic force. This matter will be discussed further in Chapter (5).

The next step is to look at the tethers' design which, to a great extent, determines the full reading range. Since the full range deflection was already limited to be 0.2 µm, then the tethers should designed in such a way that with the application of 100 g, to the proof mass (the total mass of the moving part) of the accelerometer, the force of 100 g times the mass exerted upon the tethers, should cause a deflection of 0.2 µm as full-scale deflection.

Equation (2.3) describes the behavior of a single cantilever subjected to a shear force acting at the free end. This is analogous to the proof mass hanging at the free end of a tether. In case, of 4 cantilevers having the same dimensions situated on exactly identical positions, as the case in this design, this means, the applied force is divided by 4.

With the specified dimensions of the sensor body, the mass is calculated to be around 7×10^{-10}Kg. The thickness of the tethers is fixed to 2 µm. The choice of the width of these tethers w_t is still open. The limitations of these parameters were already discussed. Accordingly, a low value for the width w should be chosen to increase the sensitivity. However, it should not be low enough to be close to the process minimum. In this sense, then 5 µm seems to be a reasonable value.

At this stage, all parameters of Equation (2.3) are known except the length of the tethers, l_t. As was mentioned earlier, l_t is extremely important in determining the mechanical sensitivity of the sensor. Substituting these values into Equation (2.3) gives a value of the tether length, **l_t= 226.7µm.**

The same tests applied to the teeth should be repeated for the tethers to verify their functionality under the expected forces in the Z direction. The major source of forces exerted on the tethers is the proof mass while for the teeth, it was only their own mass. The bending of the tethers under a shock is decelerated by the damping of the squeezed film of air to the proof mass.

Under the influence of acceleration, the combined tethers (both of the orthogonal tethers) experience deflection in the Z direction which adds up to be the deflection of the combined tether. Under a shock of 2000 g, the combined deflection would be around 50 µm and that is much bigger than the available space for travelling. The proof mass will reach the substrate under an acceleration which is close to 60 g only. However, under the effect of air damping, even the shock of 2000 g would look less violent.

Substituting for all the tether parameters and for a=2000 g in Equations (2.28), (2.27) (2.25) and (2.26) respectively results in the following:

$\sigma_{sh}=3.4 \times 10^5$ Pas.

$M=7.76 \times 10^{-10}$ N.m.

$\sigma_b=2.33 \times 10^9$ Pas.

$S_{max}=1.166 \times 10^9$ Pas.

Dividing the value of the maximum shear stress by the modulus of elasticity gives the value of maximum shear strain a value of the maximum shear stress, $\in_{max}=0.7\%$. This

value of the maximum shear strain is still less than the fracture strain reported for polysilicon as will be discussed later in Section (4.3.1). It is important to mention that this stress is only in the positive Z direction. It can travel more freely in this direction than the other since the proof mass will be resting on the substrate before the strain reaches 1/10 of this value in the negative Z direction.

The above analysis shows that the tethers design will stand up to the expected operating conditions.

As shown in Figure (2.1), a buffer area is placed between each pair of orthogonal tethers that are connected to each other. The role of these isles is to make sure that the orthogonal tethers work independently from each other. Their influence is caused by the high moment of inertia that they display. This reduces cross-axis sensitivity and helps reduce stress concentration at the joint of these tethers. A value of three times the tether width is selected. Consequently, a side length of 15 μm is chosen for these buffer isles.

For the anchors, a square area of 40 μm side is enough to hold the tethers in place while allowing the sensor to move.

Practically, there is a very important factor that will influence the behavior of the polysilicon structure and especially the tethers. It is the intrinsic stresses that is inherent in most of the deposited layers. Its value and direction varies with the type of the layer, the deposition conditions and post-deposition conditions including the annealing steps. A common case in a deposited layer of polysilicon is to be under compression with the values of the compressive stresses that reach values as high as 10^9 Pas [19]. In long cantilevers, these stresses are strong enough to force the cantilevers to buckle. The theory of buckling is explained in Appendix [C]. The way to reduce the buckling effects is to try one or more of the following:

a-Limit the length of the structures as explained in Appendix [C]. This imposes strict limitations upon the mechanical design that often makes it difficult to achieve high values of mechanical sensitivity.

b-Ease these stresses by heating the polysilicon structure to high temperatures for certain time (annealing). This depends, once again on the type of material and deposition

conditions. Despite the fact that annealing was proven to be very effective in reducing the stresses, yet the annealing process itself is not very predictable and needs to be studied on individual basis in order to be applied to any specific case. This will be discussed in further details in Section (4.1).

c-Deposit certain layer that has stresses in the opposite direction on top of the polysilicon layer. This will work on compensating the stresses in the polysilicon layer and that is proven to be an effective and feasible method. During a seminar conducted by Dr. Henry Baltes and a personal dialog, he indicated that the deposition of the silicon nitride (Si_3N_4), for example, which is a layer that is well known to be originally under tension, was proven to allow the increase of dimensions way beyond the limitations imposed by the original buckling. This option will also be discussed in further details in Section (4.1).

This almost wraps the detailed mechanical design. Note that special modifications would be carried-out according to the requirements enforced by the manufacturing process specifications or etching process and this will be discussed later in the corresponding design procedures. Table (2.1) lists the dimensions of the mechanical design.

Parameters	Symbol	Value
Thickness of the device	t	2 (μm)
Width of the tethers	w_t	5 (μm)
Length of the tethers	l_t	226.7 (μm)
Width of the tooth	w	2 (μm)
Length of the tooth	l	184 (μm)
Length of sensor body	L	368 (μm)
Number of teeth per capacitor per side	n	31
Spacing between parallel teeth of the same capacitor	d_0	2 (μm)
Multiplication factor for the distance between parallel teeth of different capacitors	m_d	1
Anchor side length	L_A	40 (μm)
Buffer isle side length	L_B	15 (μm)

Table (2.1): List of parameter values for the detailed design.

CHAPTER 3: Electrical Design

It was shown in Chapter (2) that it is viable to put the sensor in a free-moving structure. This sensor can serve as two pairs of differential variable capacitor where the difference in capacitance between each two capacitors within the pair is a linear function of acceleration within a certain range. Having accomplished the mechanical design of the sensor, the next step is to design a signal measurement circuit that is capable of detecting the difference in capacitances and transfer it into a signal that can be translated back, according to a predefined criteria, into acceleration.

The possible choices for the signal conditioning and amplification circuit were reviewed and are listed below:

a-Impedance bridges: These circuits suffer from relatively low sensitivity. This does not satisfy the requirements of this sensor despite their tremendous simplicity [26], [27]. They are often used with active circuits. This would increase their sensitivity and also increase their complexity.

b-Diode/MOS quadratic circuits: These circuits are a little more sophisticated than the impedance bridges and have a little higher sensitivity than the impedance bridges. However, their sensitivity is hardly enough to handle capacitance changes of few femto Farads which makes them more suitable for bulk-micromachined capacitive structures. They are highly affected by parasitics and for the diode circuit, the output voltage is limited to 0.2 V-0.3 V maximum. Beyond this value, serious distortion occurs because the diode then will not act as a switch [28], [29].

c-Capacitance Pulse-Width Modulation (PWM) circuits: These are more sensitive than the previous two categories and have the advantage of generating digital output without using an ADC but suffer from hysteresis and parasitic effects [12].

d-Capacitance Amplitude modulation circuits: These have high sensitivity but, less linearity and also are affected by parasitics [6].

e-Capacitor Frequency modulation circuits: These circuits have also high sensitivity. However, they are very sensitive to frequency drifts and also sensitive to parasitics [30].

f-Charge transfer circuits: These circuits can be easily implemented using switched capacitor techniques. They can achieve high sensitivity especially when special oversampling techniques are adopted. They have the great advantage of being capable of suppressing the parasitic effects and show very little sensitivity to frequency drifts [31].

According to the specifications of the circuits, the charge transfer circuit seems to be the most convenient for this application. That is due to the relatively high immunity to parasitics associated with its performance. Its sensitivity is reasonably high. The switched capacitor architecture is also quite suitable to be implemented in a CMOS circuit.

3.1-Circuit Arrangement

The circuit is shown in Figure (3.1) where C_{x1}, C_{x2} and C_{y1}, C_{y2} are the differential sensor capacitors in X and Y direction respectively. C_{p1}, C_{p2}, C_{p3}, C_{p4} and C_{p5} are the inevitably existing parasitic capacitances. There are 6 CMOS transmission gate switches for each direction S_1-S_6 for X and S_7-S_{12} for Y. They are controlled by a non-overlapping 4-Phase clock (Clk_1,Clk_2,Clk_3 and Clk_4) at a high frequency. During Clk_1, switches S_1, S_3 and S_5 are closed while the other nine are opened and C_{x1}, C_{x2}, Cp_1, Cp_2 and Cp_3 are charged. During Clk_2, S_2, S_4 and S_6 are closed while the other nine are opened. This time, C_{p1} and C_{p2} will be discharged to ground. C_{p3} will behave as a part of the already existing much bigger capacitor C_{inpx} then the current flowing through S_4 will be due to the difference in charge between C_{x1} and C_{x2}. This seems to be a suitable arrangement for a circuit that is almost immune to parasitics.

During the first two clocks (Clk_1 and Clk_2), the Y direction circuit and its reference voltages are completely isolated and will behave as though they are transparent to the moving plate and the electronic circuit of the X direction. An exception will be the combinations of (C_{y1} in series with Cp_4) and (C_{y2} in series with Cp_3) which will be small parasitics added to Cp_3. During the second two clocks (Clk_3 and Clk_4), the X direction circuit and reference voltages will become transparent and the Y direction circuit will take over. An

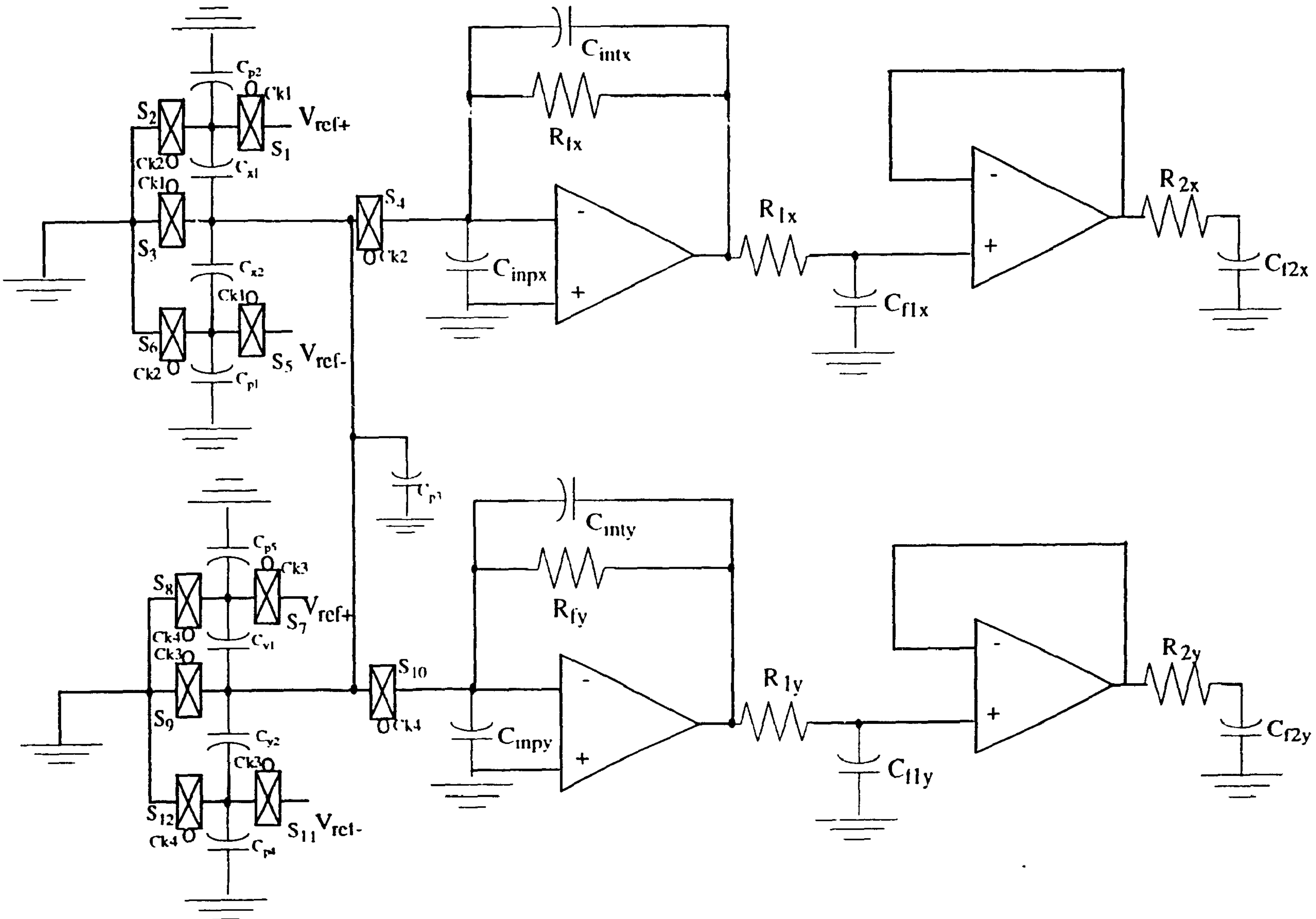

Figure (3.1): *Open-loop circuit arrangement for two dimensional acceleration measurement.*

exception will be the combinations of (C_{x1} in series with Cp_2) and (C_{x2} in series with Cp_1) which will be small parasitics added to Cp_3. During Clk_3, the switches S_7, S_9 and S_{11} are closed, while the other nine are opened. This time C_{y1}, C_{y2}, Cp_4, Cp_5 and Cp_3 are charged. During Clk_4, the switches S_8, S_{10} and S_{12} are closed while the other nine are opened. This time, C_{p4} and C_{p5} will be discharged to ground. C_{p3} will behave as a part of the already existing much bigger capacitor C_{inpy} then the current flowing through S_{10} will be due to the difference in charge between C_{y1} and C_{y2}. Figure (3.2) shows the clocking scheme of the 4–Φ clock.

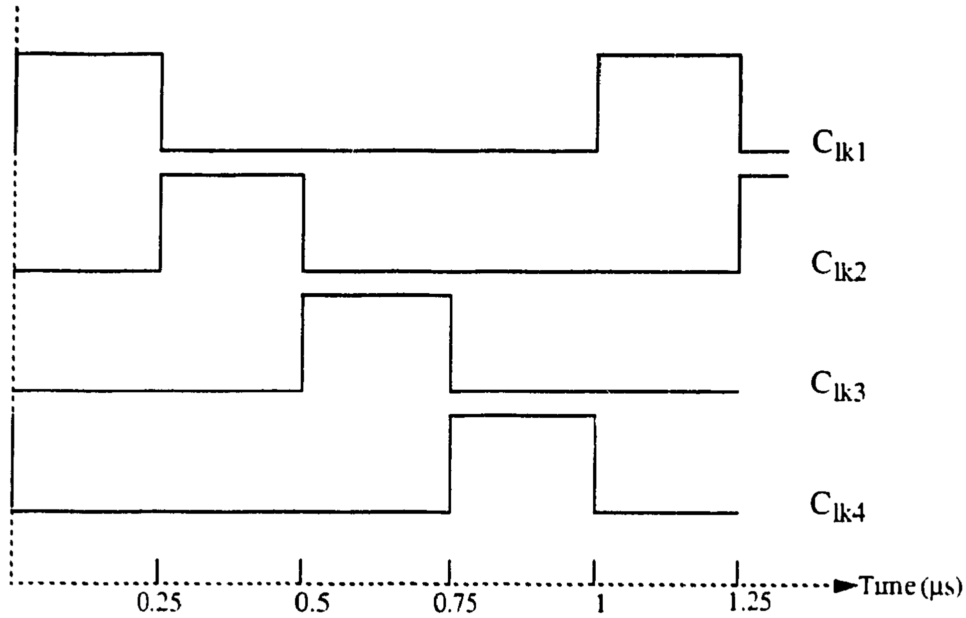

Figure (3.2): *The clocking scheme of the 4–Φ clock.*

The transfer function of the circuit in each direction separately will be of an RC circuit which can be written as:

$$\frac{V_o(s)}{V_{ref}(s)} = f_c \cdot R_f \cdot \left[C_1 \cdot \frac{1}{1+\tau_1 \cdot s} - C_2 \cdot \frac{1}{1+\tau_2 \cdot s}\right] \quad (3.1)$$

where Vref is the applied reference voltages, f_c is the clock frequency, R_f is the feedback resistor, $\tau_1 = C_1 . R_f$ is the time constant of charging/discharging the capacitor C_1 and $\tau_2 = C_2 . R_f$ is the time constant for charging/discharging the capacitor C_2.

The steady state value for a step input response would be given as:

$$V_o = V_{ref} \cdot f_c \quad R_f \cdot (C_1 - C_2) \quad (3.2)$$

Equation (3.2) indicates that the circuit of Figure (3.1) has a steady state output that is directly proportional to the differential capacitance. Note that the parasitics do not show in the equation and this gives this circuit its most important advantage over others.

According to the derivation given in Appendix [A], the value C_1-C_2 is directly proportional to the applied acceleration within the linear range of acceleration, and thus, this is a system whose output voltage is a linear function of the applied acceleration within a certain range of that acceleration:

$$V_o = V_{ref} \cdot f_c \cdot R_f \cdot \frac{K_c \cdot m}{k_s} \cdot a \quad (3.3)$$

It is clear from Equation (3.3) that increasing the input reference voltage (V_{ref}) would increase the sensitivity of the circuit. Unfortunately, the reference voltage, V_{ref} can not be increased indefinitely since V_{ref} is limited by the values of Vdd and Vss employed in the circuit. Now the values of Vdd and Vss are limited by the technology. In this technology, Mitel 1.5 µm, the absolute maximum permissible voltage difference is 7V [39]. This value was 24V for the device introduced by Analog Devices Inc. [19] To be on the safe side, Vdd=3.3 V and Vss=-3.3 V were chosen to base the calculations upon. If more than 6.6 V proved later to be safe, then it would advantageous to increase the absolute value of Vdd and Vss without any restrictions due to the design. Accordingly, V_{ref+} should be less than Vdd and V_{ref-} should be more than Vss or else some non-linearities would be forced to take place. To understand that recall that the clock has a maximum amplitude of 3.3 V. Increasing the voltage at the input port to a value close to 3.3 V would drive the transistors in the transmission gates to saturation and therefore loose the circuit linearity. It is necessary to find that value of the reference voltage at which the saturation takes place. For this reason, prolonged HSPICE simulations were performed, for a complete range of voltages, to make sure not to exceed this value in the circuit. The results of those simulations are explained in details in Chapter (6).

Running at a high clock frequency is a desired and valid option with a 1.5 µm CMOS

technology. The chosen clock frequency was inspired by the cutoff frequency of the utilized OPAMP. This cutoff frequency was slightly above 1MHz. In choosing the frequency, it is also important to regard the speed of the transmission gates. Since analog signals are used then sufficient time should be allowed for the signals to stabilize before the switch is opened again. In this respect, the period of the clock is defined by the time constant of the circuit being charged and discharged.

The feedback resistor of the integrator R_f is also very crucial in determining the circuit behavior since it will be defining the time constant of the charging or discharging paths. R_f should be a linear resistor to reduce the voltage dependency of the gain of the integrator otherwise linearity of the circuit will suffer. Therefore, R_f should not be created from diffusion or active load configuration. It should rather be laid out in polysilicon as will be discussed further in Section (3.2). In order to increase the sensitivity of the circuit, R_f should be made as big as possible, but this has its implications that will be discussed later in the circuit layout. On the other hand, R_f can not be increased indefinitely since a high value of this resistor would be causing some noise and even might drive the OPAMP into the saturation region due to the charge accumulation on the input side. For all these reasons above, a value of 1MΩ was found, based on HSPICE simulations, to be a good compromise between these conflicting factors. R_f can not be an external resistor or else, external noise will be added to the integrated signal.

From the mechanical point of view, the implications of increasing the sensor capacitance were discussed earlier. It is evident that the mechanical requirements would prefer the smallest possible capacitor (as small as possible of the sensor area), but what will be an acceptable limit for that capacitance?

The clock frequency was chosen to be 1MHz, divided into four phases and an over-estimated value of the rise time and fall time of 10 ns i.e. a clock active period of 0.23 μs/Φ. Now in order to make sure that an RC circuit would be allowed to be charged at least to 90% of the steady state value during a transient charge/discharge period, then a clock period of 2.3 times the time constant of that circuit is considered to be necessary. That gives an estimated value of 0.1 μs to be the time constant of the circuit. Having already chosen a resistor value of 1MΩ leads to an estimated value of C_1, C_2 of 100 fF. This value was close to the capacitance of the ADLX50 sensor [6]. Allowing for a total ±10 fF (10%) change as a full scale change in each of the capacitance, that would add up to be 20 fF of change in capacitance.

Having capacitors connected to the same circuits on both sides of the mechanical sensor in both X and Y directions would do a very good job in minimizing the cross axis sensitivity between these two directions. Figure (2.1) shows that whatever small effect will appear on the capacitance of one side, when the sensor moves to a certain direction on one axis, would be cancelled by the same effect but, in the other direction on the other side on the same axis. As a result, the total change in the differential capacitance due to the off-axis acceleration should be negligible.

The moving structure of the sensor will serve as the common plate of the capacitor which in electrical terms will have a voltage whose value depends upon the reference voltage and the position of the moving plate in the open loop arrangement In contrast to being electrically isolated from the substrate, this structure should be securely anchored in place to the substrate. The question is whether it should be allowed to touch the substrate or not and what the advantages and disadvantages are of each arrangement?

As a p-well process, Mitel 1.5 μm CMOS process uses n wafers as substrates which means that the substrate should be connected to the most positive voltage available (Vdd). This implies clearly that any direct connection between the anchors and the substrate would upset the biasing of the circuit. There are 2 options to electrically insulate the moving structure from the substrate while still leaning on it:

a-To let the anchors sit on an oxide layer instead of sitting directly on the silicon. This ensures the electrical insulation while providing mechanical support which is still under question, whether it is sufficient to support or not. This arrangement is electrically sound, yet should be further investigated mechanically.

b-To create a p-well and inside which, an n^+ diffusion is created. The anchor is placed directly on the silicon on top of the n^+ area. To ensure electrical insulation then the p-well is biased at the most negative voltage available (Vss) and therefore secures a reverse biased diode at all possible voltages applied to the moving structure. This arrangement is more sound mechanically since the polysilicon is directly seated on the substrate, yet from the electrical point of view, this added p-n junction is noisy and its noise increases with the temperature. This does not comply with the rule of reducing the noise as much as possible.

The first solution is more appealing. There will be some added layers that pile up on top of each other and help to secure the tethers in place and hence, can fix this arrangement mechanically. The addition of these layers will make the first choice more convenient than the second.

The circuit arrangement of Figure (3.1) shows that the first amplifier stage is an integrator which works to collect the pulses coming from the circuit over a time period and get a DC value out of it.

The input from the switched capacitors is connected to the inverting terminal of the opamp while the non-inverting terminal is connected to the ground in open loop arrangement. A calibrated output signal can be fed back to control the sensor position in the closed loop arrangement. This will be reflected on the inverting terminal because of the virtual short (due to the feedback resistor R_f) and consequently reflected on the middle plate of the capacitors. The gain of this fed back signal needs a very precise tuning (usually varies from chip to the other) that LASER trimming techniques are employed to tune it accurately. This technique is neither part of the standard Mitel 1.5 μm CMOS process nor it is available at Concordia. As a substitute, it is possible to either try adding a potentiometer of small value to a set of high precision resistors switched on externally so that the potentiometer will do the job of fine tuning. Considering the fact that external resistors are bulky and noisy then the choice is to send the chips to an outside laboratory for possible surgical operations on chips using LASER.

3.2-Circuit Layout

Equations (3.1), (3.2) deal with the sensor capacitances C_1, C_2 as single solid capacitors. The real situation is that each one of them consists of 62 small capacitors (will be referred to as the mini capacitors to distinguish them from the total capacitor) which increase and decrease, to a very good approximation, by the same values simultaneously. Having these mini capacitors connected to each other via a very low resistance path is crucial. To show that, imagine that one of the sensor capacitors, say C_{x1} in Figure (3.1) should be substituted by a network of mini capacitors connected via relatively big resistors as shown in Figure (3.3). The resulting circuit would have a different time constant for each of the mini capacitors depending upon its distance from the terminal connecting it to the rest of

the circuit. The furthest capacitors would have a relatively high time constants. This situation implies that one of the two choices described below may be chosen:

a-To use a slow clocking scheme in order to give time to all mini capacitors to charge and discharge. This, as was shown, would rapidly reduce the sensitivity of the circuit since the sensitivity is directly proportional to the clocking frequency.

b-To keep running at high frequency and accept to sacrifice those mini capacitors associated with high time constant. Consequently, the effective sensor capacitance would be smaller than the design value which reduces the sensitivity of the system. Moreover, silicon area is wasted, and also some of the useful frequency response of the mechanical system is wasted since increasing the mass and size generally causes the reduction of the natural frequency.

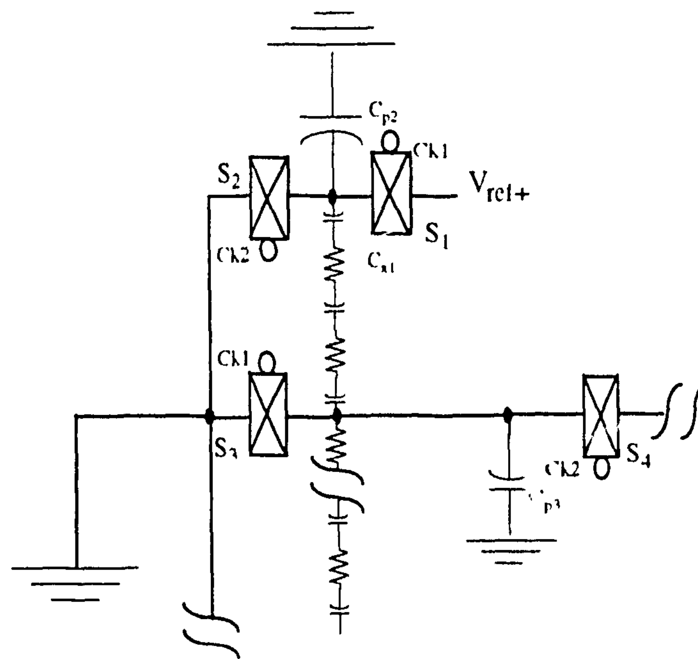

Figure (3.3): *The effect of the parasitic resistors on the circuit arrangement.*

The above choices are almost equally bad and accepting any of them would cause appreciable degradation to the circuit performance. Therefore, those mini capacitors should be connected to each other via small resistors.

Adding mini parasitic capacitors to those parasitic resistors will aggravate the situation

even more. The reason is that unlike the other parasitic capacitors, some of these mini parasitic capacitors would have larger time constant for discharge to the ground. The resulting effect is the addition of some parasitic capacitors that are not totally cancelled from the circuit performance. This also means having lower sensitivity.

To minimize the noise caused by the high resistivity of the substrate, several connections are made between the Vdd and the substrate through n^+ doping. The abundance of these substrate connections will help reduce the substrate currents and decrease the chance of charge accumulation within the substrate. It also eliminates any chance of latch up within the circuit.

As a rule in any high frequency design, and since this is a switched circuit, the supplies are driven to the circuit using wide metal lines. This ensures minimum flickering in the supply voltages. Having high capacity and low resistance, these metal lines will behave like voltage buses.

The ground line, being very important in the circuit performance was made even wider than both supplies.

Induction is a big source of noise in microelectronic circuits. Having two lines crossing would result into a parasitic capacitor. A high frequency signal would have a low impedance path to be transferred from a line to another that crosses it. In this case, no signal-carrying conductor should cross over another. All the crosses had, at least one out of the two crossing lines to be a DC-carrying line (Vdd, Vss, Gnd.) where the induced signal would die out in the large capacity of that metal line.

Another important issue in the layout of the circuit was the layout of the $1M\Omega$ resistors. The layer that has the highest resistivity out of the conducting layers in this process is the second polysilicon layer that is called "Capacitor Poly". However, making such a big resistor will grow up to occupy a very large area. To reduce the area reserved by this resistor, it is a common practice to make it of zig-zag shape. The long zig-zag shaped polysilicon layer would invite the external Electromagnetic Interference (EMI). However, the polysilicon layer has relatively large resistivity compared to metals. This implies that polysilicon is not a perfect antenna and the induced signals should die out without much of influence over the circuit. Such a structure is also accompanied by internal capacitance

between facing arms of the zig-zag. This will beha as a short circuit to the very high frequencies. However, those very high frequency signals, would be filtered by the operational amplifier due to its limited bandwidth imposed by the parasitic capacitances of the circuit. It is necessary to investigate whether a 1MHz signal (the clock fundamental frequency) would find these capacitances to be a low impedance path or not? This can be roughly checked by calculating the capacitance between two adjacent arms of the zig-zag which are defined to be 300 μm long and 0.35 μm thick and 1.5 μm apart. Having SiO_2 as the medium, this gives an approximate capacitance of 3 fF. For a signal of 1 MHz, each capacitor of these would show a reactance of 50 MΩ which is much higher than the resistor itself. Hence, these capacitances would not provide a short path for the fundamental frequency.

In order to conserve the accuracy of the measurement, then the signal coming out of the sensor should not remain as analog voltage signal. In the traditional sensors, it was a common practice to convert this voltage signal into a current signal where the resistance of the carrying wires would not affect the current signal. An even better approach is to convert this analog signal into a digital signal.

If a self test option was to be added to the sensor, then a suggested arrangement is to force preset voltages on the sensor capacitors C_{x1}, C_{x2}, C_{y1} and C_{y2}. These voltages should be placed on the plates of these capacitors other than the common (moving) plate. This can be done by bypassing the switches S_1 and S_{12} simultaneously and continue with the sensor operation as usual. The influence of these voltages will be to push the moving plate to the corresponding position by virtue of the electrostatic forces. The final effect should appear as repeatable output voltages which will indicate that the sensor is free to move and giving the right output.

Note that the operational amplifier used in this circuit is a standard cell from CMC library for Mitel 1.5 μm CMOS process.

CHAPTER 4: Process Flow

Following the mechanical and electrical design, there should be developed a well defined process sequence. This sequence described here is a combination of standard CMOS steps among which some modifications have been inserted and added.

4.1-Microelectronic Fabrication Processes

Before going into the details of the process sequence, a brief description of the regular steps found in a standard microelectronic fabrication process will be given. A standard microelectronic fabrication process has the objective of creating integrated circuits on silicon substrates. Special processes use GaAs, Ge or silicon on sapphire, but the emphasis here is only on silicon-based processes. This process usually consists of more than a hundred steps. These intermediate processes can be one of the following [32]:

a-Surface preparation (cleaning): These steps help to remove the residual effects of the previous step(s). For example, after dipping the wafers in an etchant, a special rinsing procedure is performed. This procedure might involve the use of one or more of the cleaning solutions where Deionized water (DI Water) is invariably used. These steps are usually short and performed at relatively low temperatures (usually below $100^{o}C$). For commercial processes, the preliminary cleaning steps are crucial which will make sure that no harmful contaminants will be introduced to their furnaces or reactors. For example, the presence of excessive Na^{+} ions in any wafer can spoil the characteristics of the MOS transistors. For this reason, companies usually do not accept that a wafer would be processed by some other party to be sent to them for further processing. Neglecting these safety precautions might end up contaminating a furnace or a reactor. Such a contamination might enforce that the whole batch would be discarded and that furnace would be excluded from the production line until thoroughly cleaned. In terms of commercial interest, this is considered to be a big loss.

b-Layer deposition or growth: This involves chemical reactions to grow silicon compounds like SiO_2 or Si_3N_4 by heating the silicon to high temperatures in oxygen or nitrogen environments. This growth usually consumes silicon from the wafer itself. The

deposition can be the deposition of silicon as in epitaxy layers whether doped or not. Polysilicon deposition is often done. It can also be silicon compounds like SiO_2 or Si_3N_4 and this time no silicon is consumed from the wafer and this deposition is most probably Low Pressure Chemical Vapor Deposition (LPCVD). It can be non-silicon materials like Metals which are basically Al alloys and deposited using sputtering or evaporation. SiO_2 can be added as liquid to planarize the surface then heated to turn into solid glass. These processes are usually carried out at elevated temperatures (sometimes higher than 1000^0C). However, after the metal patterning, no high temperature process is allowed (since the melting point of Al is around 670^0C) and deposition will be done at lower temperature such as the Plasma Enhanced Chemical Vapor Deposition (PECVD) of SiO_2 or Si_3N_4. In some laboratories, LASER is used to grow layers but this is not a standard commercial process.

c-Application of photoresist: This is usually spun on the surface then a pre-baking process is done to it. The spinning is done usually at room temperature while the pre-baking is done around 100^0C.

d-Application of mask: That is done by exposing the wafer to an Ultra-Violet source via a mask. This mask usually carries the shapes of the features to be patterned on the wafer. The number of masking steps is a good measure of the length of the process and its cost. It is not always the case that the number of the masking steps is equal to the number of masks since the same mask might be applied more than once in certain cases. This exposer is usually done at room temperature. A post-baking process usually follows the exposure and the temperature of that baking is usually higher than 100^0C.

e-Development of photoresist: This is done by dipping the wafers in a developer used specifically for that type of the photoresist. This development is done either at room temperature or slightly higher. This process is a time controlled process and both under development and over development are not recommended since the final shape in both cases would be different from the originally intended one. After development, the patterns will be carved on the photoresist. The application of photoresist, exposure and development are usually called "Photolithography".

f-Etching process: This is done by dipping the wafers in a suitable etchant. This etchant should selectively consume the material to be patterned without harming other

exposed materials especially the photoresist. These etching processes are usually performed at temperatures less than 120°C. Different techniques of dry etching are widely used in industry where no aqueous solution is involved. Dry etching usually needs special type of reactors to create the required environment and these reactors are considered more expensive than wet etching apparatus. LASER can be used in some laboratories to blow under some surfaces and consequently dig some shapes. This is a slow type of etching. yet without direct exposure.

g-Stripping off photoresist: This is done either using dry etching or wet etching and it aims to remove any trace of photoresist without implications on the other layers. These processes are done at medium temperatures in case of dry etching and low temperatures in case of wet etching.

h-Doping: This is usually done through ion-implantation. In ion-implantation. the exposed surface is bombarded with an exact dose of ions having a specified energy. The final depth of these ions is determined by their energy and the total thermal budget they would be exposed to. The apparatus needed for controlling ion implantation is usually expensive. Another way of doping is to add doping material during the deposition to form a part of the deposited material. The advantage of this method is that no extra step is needed for doping and uniform doping profiles can be achieved. More precise doping profiles can be achieved using the implantation. Diffusion is another way of doping that is used less often. It is a non costly. yet less accurate process.

i-A drive-in process: The ions are driven to a certain depth. This process aims to define the required junction depth. It is carried out by subjecting the wafers to high temperatures for prolonged time periods.

j-Surface passivation: This is done by adding some passive layers as the top layers of the wafer. This passivation can be adding SiO_2 and/or Si_3N_4 depends on the specific process. The reason of applying them is to protect the circuit against dirt. moisture and against further reactions that are possible within the environment of operation.

These are the steps that are usually applied to the silicon wafer. There are more steps that would yet be applied to the wafers after being sliced into dies. These processes are usually physical processes like metal bonding and packaging. The discussion will be about the

steps applied to the wafers before dicing only for a good reason. It is often regarded to be one of the best features of surface micromachined accelerometers, having no special requirements for the packaging process. This means, whatever is done in a standard process, can be practiced on accelerometers with no modifications. This was already explained in the properties of accelerometers.

4.2-Sensor Material

In order to define the process sequence required to realize the sensor, the sensor material should be selected. The materials available in a standard CMOS process including Mitel 1.5 µm, are SiO_2, Si_3N_4, polysilicon and aluminum. The material needed to create the sensor body should show the following properties:

a-It should have satisfactory mechanical properties like high yield stress, high fracture stress and a reasonable value for Young's modulus.

b-It should be possible to selectively etch it without affecting the other layers or else, the definition of the sensor structure would be an impossible job.

c-It should have very good electrical conductivity to be capable of serving as a capacitor plate.

Property (a) prefers polysilicon over others. The use of metal is dismissed since the metal alloys commonly used in these processes have weak mechanical properties. This is partially due to the nature of the alloy and also due to the fact that it is originally sputtered, then it is alloyed through heating up for a short period of time. This does not seem to give enough time to establish complete bonds of the metallic crystalline structure.

Property (b) does not favor SiO_2 as a choice since it is used too often in the process and every time a dioxide is etched, the sensor body should be protected in a special arrangement. This makes it a laborious and expensive procedure to achieve the structure with the required uniformity using SiO_2.

Property (c) dismisses both SiO_2 and Si_3N_4 because they both are perfect insulators in the process and since this design deals with lateral capacitors, then it is not possible to change

their conductivities by depositing some other conductive material on top of it. On the other hand, polysilicon, in this process, can be a good conductor as deposited. On the average, the fist polysilicon layer has a resistance of 20 Ω/sq.

By exclusion, there is no other choice other than the polysilicon to become the sensor material and in fact, polysilicon is the favorite even among larger selection of materials. The fact is that polysilicon is almost the favorite choice for everybody when it comes to the creation of moving structures. This is attributed to its good mechanical properties.

It is worth mentioning that pure polysilicon, in nature, is not a good conducting material and the choice of doping it by implantation is not recommended. This is true since implanted ions seem to severely degrade the mechanical properties of the polysilicon by the multiple collisions and associated dislocation of atoms. The result is focal highly stressed areas which will be the first to fail mechanically. The good thing is that Phosphorus is added to the gasses entering the reaction chamber for polysilicon deposition and that produces polysilicon that is uniformly impregnated with Phosphorus ions without the additional stress caused by implantation.

4.3-Fabrication Process

Design of the sensor as given in Chapter (2) shows the requirement of a structure of polysilicon having the dimensions given in Table (2.1) and sitting on top of a sacrificial material that would be etched in later step(s). There are several issues to be addressed in arranging the fabrication process.

4.3.1-The Problem of Thick-Poly Deposition

The need for a layer of thick polysilicon to form the sensor body was already explained in Chapter (2). There are two major problems associated with handling (deposition and patterning) of polysilicon:

a-The general problem of patterning thin layers deposited on top of patterned thick layers: This problem is caused by the application of the photoresist for patterning. The photoresist is spun over the surface of the wafer to form a planar surface. If a wafer happened to have surface topography of diverse heights, i.e. areas with thick poly next to areas without poly then a layer of very thick photoresist will be deposited where there is

no thick polysilicon as illustrated in Figure (4.1). First, this will create a problem in the exposure of the photoresist since deeper photoresist needs longer exposer than thin layers. Over-exposure of the thin layers might affect adjacent areas that were not supposed to be exposed and consequently cause deformation around the edges of the exposed areas. Second, when stripping off the photoresist, timed etching is usually performed. The thick layers of photoresist need longer etching and there will be a serious problem of photoresist residuals.

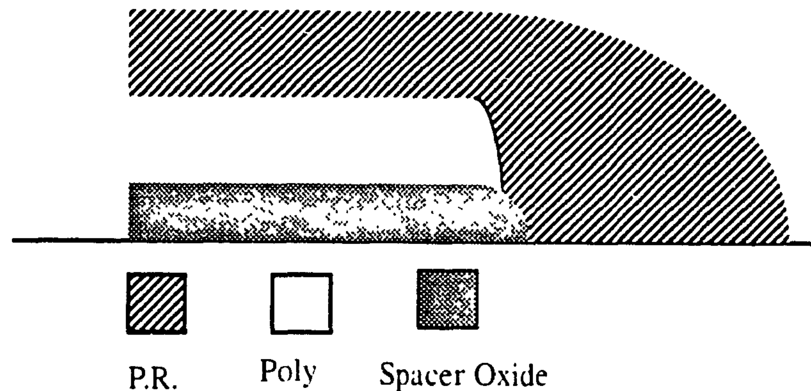

Figure (4.1): *The creation of thick photoresist due to the surface topography.*

b-The special problem of intrinsic compressive forces in thick polysilicon layers: The consequences of this problem were already discussed in Chapter (2). The question now is "What causes these compressive stresses in polysilicon films?" Even before that "how is polysilicon deposited commercially"?

Polysilicon can be deposited by the thermal decomposition of Silane SiH_4 in a low pressure chemical-vapor deposition process (LPCVD). Grain size control is achieved in principle by temperature selection. Thus deposition below 580^{0}C is reported to be amorphous whereas deposition above 580^{0}C leads to increasing grain size with temperature [33]. The transition temperature from amorphous to polycrystalline films appear to be a temperature range rather than a specific value and depends on Silane purity, substrate condition and processing conditions. It was determined that reaction temperatures of 591.5^{0}C gives adequate results and improves the deposition rate from 50A^0/min at 580^{0}C to 68A^0/min [34]. Films deposited at 591.5^{0}C are typically compressive with strain levels that often reach as high as -0.6%. Annealing in nitrogen or under vacuum converts the as-deposited built-in strain to tensile field with controllable strain fields from +0.5% to 0%. Typically, 2 μm thick poly films exhibit a strain of 0.25% after vacuum annealing at 835^{0}C for 1 hour [33].

H. Guckel et al. [33] had studied as-deposited thick polysilicon as far as the stresses are concerned. The result they came out with (from Transmission Electron Microscopy) was that the as-deposited thick polysilicon consists of two regions. The region near the substrate interface has recrystallized during growth while the layer covering it was amorphous. The recrystallized region contains grains from $100A^0$ to $4000A^0$ in size. The orientation of these grains is randomized.

H. Guckel et al. [33] also found that cantilever structures of the as deposited film exhibit beam deflections towards the substrate. Annealing in nitrogen at $1150^{o}C$ for 3hours reduces the strain field to very low levels. The results of the Microscopy indicated that the amorphous phase had been converted to the polycrystalline phase. There was no increase in the grain size. However, there was a slight increase in surface roughness as measured with a Surfscan instrument. The interpretation of the microscopy data led them to the conclusion that the strain field reversal during partial annealing, say at $835^{o}C$ for 1hour involves a conversion of the amorphous phase to the polycrystalline phase and is associated with a volume contraction which is responsible for the tensile field. This conversion does not involve the entire amorphous phase.

Tai and Muller [35] had studied the fracture of brittle materials including polysilicon. They concluded that fracture occurs when a crack can propagate in the material. Cracks can originate from defects in solids such as impurity inclusions and segregations, and grain boundaries. The probability that these defects will cause fracture depends heavily on their spatial extent, shape and orientation, which are statically distributed. They performed $1000^{o}C$ annealing for 1hour and ended up with the result that annealing caused to reduce the fracture strain of polysilicon. However, annealing reduced the variance with which the fracture strain can be determined. This also means that the annealing increased the repeatability of the strain patterns achieved from polysilicon structures.

The above discussion shows that annealing can be very useful since it even converted the strain field in polysilicon from compressive to tensile and increased the repeatability of the polysilicon properties. However, care should be taken in designing polysilicon structures that would be annealed since, according to Tai and Muller [35], the fracture load should be checked for annealed Poly rather unannealed.

From the above discussion, it is clear that the standard annealing processes are long periods of exposure to high temperature (high thermal budgets). In Section (4.1), the effect of high thermal budgets as a drive-in to the dopants was discussed. Now if annealing was performed before any doping process then its influence can be neglected but, what happens if this can not be arranged since the p/n-well implantation is one of the very early steps in any CMOS process? The answer to that is that the final well depth will be deeper and average doping (conductivity) of the well will be lower. Consequently, latch-up immunity that is usually influenced by careful control of the doping profile in the diffusion wells, will suffer from that conventional annealing. This will eventually cause junction depths deeper than the intended values despite the fact that modern MOS processes should have shallow Source/Drain diffusion to limit short-channel effects. The transistor threshold voltage control depends on maintaining a threshold-control implant close to the substrate/gate oxide interface. This added thermal budget would change the threshold voltages of the transistors and as a result, would change the anticipated behavior of the circuitry.

The conclusion from the discussion above is that in order to reserve the liberty of depositing and annealing the polysilicon at the chosen step, then major changes to the process should also be taken care of including changing all the doping levels in the circuit. This proves to be a costly and complicated procedure that is beyond the scope of this project. The other choice is to limit the choices within the following:

a-The deposition and annealing of the sensor poly should take place as early as possible in the process so that their influence will show up on less number of doping processes.

b-No conventional annealing methods that implies prolonged periods of heating at high temperatures (high thermal budgets) should be utilized. To minimize the effect of annealing on the on-chip circuitry, Putty and Chang [37] have investigated Rapid Thermal Annealing (RTA), with its associated low thermal budget as a strain-relief technique for polysilicon microstructure. They have found RTA for 3minutes at 1150^0C, to be almost as effective as conventional annealing for reducing the strain in as-deposited polysilicon. The low thermal budget for this process has a minimal effect on the on-chip circuitry, yet very effective for reducing the high compressive strain in the polysilicon film. This is very helpful in allowing free-standing microstructures to be incorporated with high-quality circuitry while reducing the processing time required for annealing the polysilicon.

In Mitel 1.5 μm process, deposited polysilicon is doped with Phosphorous. Lober et al [36] had noticed that the behavior of doped polysilicon is different from that of the undoped as far as annealing is concerned. Their observation was that all $POCl_3$-doped polysilicon beams deflected downwards, while all undoped beams deflected upwards. Their second observation was that undoped polysilicon responded to annealing for 3 hours at 1150^oC bringing their stresses to low levels (Note that they have not reported a reversal of strain field). However, doped polysilicon showed very little or no response to that annealing process. They attributed the similarity of the strain fields of the $POCl_3$-doped unannealed and annealed polysilicon to the fact that grain structure of $POCl_3$-doped films is a stable state of equilibrium after the doping cycle; the annealing cycle does not effectively alter this state [36].

The conclusion from the above discussion is that different deposition conditions and different compositions would possibly result in different strain behavior of the materials. Different post-deposition treatment might also result in different strain fields. The final conclusion is that all these experiments should be repeated on the very polysilicon that is going to be used in creating the structure. This would be the best way to make sure that the same quality of polysilicon can be repeatedly achieved.

Another way of overcoming the problem of intrinsic compressive stresses in as-deposited polysilicon, as was mentioned earlier, is to deposit a layer of opposite strain field on top of the polysilicon. This layer should be thick enough to invert, or at least very much reduce, the strain field of the polysilicon. nitride seems to be a very good candidate to accomplish this goal. However, nitride would increase the stiffness of, the already stiff, tethers of the sensor. This means that the tethers have to be redesigned according to the new composition and the length of the old tethers should be increased according to the new thickness of the tethers, yet this time with much less fear of increasing the length of the tethers. This will allow designing for much higher sensitivities.

4.3.2 The Choice of Sacrificial Layer

Surface micromachinig relies on high selectivity between the sacrificial spacer layer on one side and the layers used to form the microstructure and the etch stop on the other side. The underetching requirements will be discussed in details in Section(4.4). Thick polysilicon was already taken to be the sensor material, but what is the proper material to be cho-

sen to form the sacrificial layer?

Some form of silicon dioxide is commonly used as the sacrificial layer, because it is etched much more rapidly in HF than is polysilicon Phosphosilicate glass (PSG) is often used as the sacrificial layer, because it is etched more rapidly in HF than is undoped form of SiO2. It can also be conveniently deposited using Chemical Vapor Deposition (CVD), and is a very common material in conventional CMOS processes. However, when a single-layer PSG sacrificial layer is used, Putty and Chang [37] have noticed that the polysilicon microstructure was severely distorted after the strain-relief cycle. Similar effects were observed during furnace annealing at 1100^0C of polysilicon/PSG/Si_3N_4 sandwiches. This distortion was attributed to the fact that PSG flows at 1100^0C and therefore does not stick well to Si3N4; this allows the microstructure to assume a relaxed configuration before the high compressive stress has been relieved. They suggested a solution to this problem in the form of using composite sacrificial spacer of PSG on top of an undoped CVD SiO_2 layer. In this configuration, the PSG flows at the annealing temperature but adheres well to the underlying SiO_2 layer which does not flow. This will hold the polysilicon layer in place during the annealing procedure and consequently will produce a reasonably flat undistorted microstructure.

The composite sacrificial layer does not etch as quickly as the single-layer PSG spacer, yet it does etch much faster than a single layer CVD SiO_2. However, as easy as it sounds, a composite sacrificial layer, simply means additional masking steps. This means, as was stated earlier, prolonged more expensive fabrication process.

Guckel et al. [38] studied the deposition of polysilicon on different surfaces and concluded that polysilicon deposited on freshly grown silicon dioxide has superior qualities. They also found that quality polysilicon films on Si_3N_4 are more difficult to achieve and the texture and irregularities of the Si_3N_4 layer are being transferred to the polysilicon layer.

Thickness of the sacrificial layer is determined by several factors. The fluid damping, static deflection due to own weight and the underetching requirements. Fluid damping requires as small as possible of a gap between the moving structure and the substrate to reduce the sensitivity in the unwanted Z direction. Static deflection requires a spacing big enough to allow the sensor to move without hitting the substrate, in the mean time, small

enough to stop the sensor and protect the tethers from reaching the fracture stress limit in case of a shock. Basic calculations show that the tethers will have a combined deflection of almost 50 μm under a shock of 2000 g without reaching the fracture limit. However, their deflection due to gravitational acceleration is only 0.025 μm. The third factor, the underetching requirement needs as thick as possible of the sacrificial layer. The viscosity of the liquid will prohibit the etchant from travelling freely into narrow channels. If large channel is available then this will help getting fast, fully developed etching. As a result to the discussion above, a sacrificial layer thickness of 1.5 μm was chosen as a compromise between the conflicting factors.

4.3.3-Process Sequence

The sensor material and the type of the sacrificial layer have been already chosen. What comes next is to set the process flow that will result in the formation of these layers in the desired shape and sequence while keeping in mind the available etching process for the final etching to be BOE etching. The process will be discussed in details from the etching point of view in Section(4.4). The procedure was to move back and forth from Section(4.3) to Section(4.4) in an iterative manner making the necessary modifications and adjustment in both parts. In doing this, it is necessary to keep in mind that a commercially successful design would have minimum possible number of masking steps. Any standard fabrication process already has a solid sequence of steps for the sake of the creation of the circuitry. A good objective would be to perform as little as possible of modifications to the process, namely, the number of added masks. A big challenge was to make a very well defined distinction between the circuit area and the sensor area. The best way to achieve this is by creating a full wall of etch-stop material that prohibits the etchant from attacking the circuit area without the interruption of the electrical connections.

Looking at the process flow described by Theresa Core et al. [19], their strategy was built on forming a full container of Si_3N_4 that conceals the sensor area which seems to be a very convenient way while securing the electrical connection between the sensor area and circuit area through buried n^+ underpasses tens of microns long. These underpasses were implanted in the early stages using the highly doping Emitter mask which seems to be working for them. For us, this implantation represents two problems:

a-In a CMOS process, there is no access to a high doping dose equivalent to the Emitter doping and that means the presence of relatively high resistance in the signal path

A typical resitance of n^+ diffusion is 100 Ω/sq [39].

b-These underpasses would represent high diffusion capacitance as parasitic capacitors, added to them parasitic resistors. Consequently, the sensor capacitance would be better represented by small capacitors connected to each other via a network of parasitic resistors with parasitic capacitors connected from each node of the network to the substrate. This would affect the sensitivity of the circuit as was described in Chapter (3). For Analog Devices Inc., they could recover from that, perhaps relying on the high voltage range (24V) that their process allows [19]. In this case, the voltage range was already pushed to the limit and the presence of these parasitic resistors/capacitors would be a real drawback in the sensor design.

Based on the above discussion, an alternative for these underpasses was to be found. With that in mind, the inspiration was taken from the ADLX50 to use the Si_3N_4 as an important part of the etch stop barrier both from between the polysilicon lines and on the very top of the circuit area to encapsulate the circuit area, but what about the connection between the sensor and the circuit? Is there anything that can serve satisfactorily as a substitute for the underpasses and still can be created with not as much of side effects?

In the beginning, the idea in mind, was to have metal lines, connecting the polysilicon fixed plates inside the sensor area. Consequently, after the final etching, these metal lines will be flying in the air as microbridges after the dioxide that used to separate and support them had been etched away. The information sent by the company that runs the process did not favor this approach for two reasons:

a-The belief is that the mechanical properties of their metal will not allow it to stand in the air as microbridges especially in the case of shocks. The collapse of any of these microbridges would mean, in the least case, the loss of balance between the differential capacitors which means the introduction of a big nonlinearity in the readings. The worst case would be the failure of the whole sensor.

b-In this arrangement, metal lines are used to connect the sensor area to the corresponding metal at the circuit area. As a result, the artificial addition of the spacer LTO (1.5 μm thick) and Sensor Poly (2 μm thick) in the sensor area will cause a 3.5 μm difference in height between these metal lines. In order to bring these metal lines into contact, then

special arrangements are required. One of the proposed arrangements was to etch a pit of 3.5 μm depth in the substrate for the sensor area. If this was achieved then one can proceed with the rest of the steps with other problems yet to come. This was ruled out by the process engineers from the company since it was not conceivable for them to define a pit of that depth in the substrate unless an anisotropic etching would be performed on the wafers before the process really starts and they found that to be unacceptable.

Once the metal flying microbridges were ruled out then another practical solution was needed. A very promising suggestion was presented by Dr. L. M. Landsberger in an informal discussion on the subject. His opinion was to continue with the idea of encapsulating the circuit area using Si_3N_4. The modification was to let the polysilicon lines run inside the circuit area to make direct contacts to the circuitry without the help of flying metal lines or buried underrunners. The difference is to create an area where the sensor Poly comes into contact with the LPCVD Si_3N_4 once it reaches the borders of the concealed area and therefore penetrates that border as shown by Figure (4.2a). Since the etch rate of silicon and polysilicon in the final etchant (BOE) is fairly low, then this can be as good as the wall created by LPCVD/PECVD Si_3N_4 joint. Once the polysilicon lines are inside the circuit area, the connections among them and with the rest of the circuit will be the same as the circuit connections without resorting to any diffused underpasses or flying metal bridges.

After several stages of refinement, the process sequence required to implement the sensor was put into order. The starting point for building the process sequence was the original process flow of the unmodified process listed in Appendix [E]. From Figure (4.2a), it is clear that there is a need for thick SiO_2 layer. This layer should also be strong enough to serve as a support for fixed capacitor plates and the tethers once they cross to the circuit area. The field oxide seems to satisfy both requirements, besides growing another layer of the same qualities would require long period of heating at high temperature and it will not be advisable to add another high temperature step to the process. On the other hand, it is imperative to deposit and anneal the sensor poly before the threshold voltage implant or else, appreciable changes in the threshold voltages might take place and the implications of these changes were already described in Section(4.3.1). Based on that argument, the creation and patterning of the field oxide (step 10 in the Process Flow Overview given in Appendix [E]) was taken as the starting point of the modified process. The added steps will be numbered starting from 10a and upwards as follows:

10a-Pre-gate oxidation: This step is the same as the standard Pre-gate oxidation (Step 11) Its objective is to create a thin layer of oxide on the silicon surface then etch it totally to ensure that the silicon surface would be clean. It needs no mask.

10b-LPCVD nitride deposition: This step creates the LPCVD Si_3N_4 necessary to act as the etch stop for the final etching.

10c-Patterning of nitride: This step shapes the Si_3N_4 layer into the etch stop wall needed at the borders between the sensor area and the circuit area. It requires the first additional mask defined in the modified process. This mask does not need to be a very precise one since the features defined here are not critical in dimensions. However, this does not make it any less important than the others.

10d-Spacer SiO_2 deposition: This step creates the sacrificial SiO_2 layer that will define the platform over which the polysilicon would be sitting and therefore defines the spacing between the sensor poly and the substrate.

10e-Patterning of spacer SiO_2: This step shapes the sacrificial layer to create the preliminary mechanical support for sensor poly necessary to create the moving structure. It is necessary to overlap the sacrificial layer over the Si_3N_4 layer and that will make sure that the polysilicon will not come any close to the substrate without the presence on the Si_3N_4. This step requires the second additional mask.

10f-Sensor Poly Deposition: This step creates the polysilicon layer that will end up forming the sensor structure. This requires the growth of the thick, low resistance polysilicon. Effectively, this would end up to be the thickest layer deposited in this process sequence.

10g-Patterning of sensor poly: This step is the one that defines the sensor structure. This mask carries the finest structures and should be very precise in dimensions. The alignment of this mask is also crucial since the polysilicon structure should sit exactly on the SiO_2 base especially in the areas where the teeth cross from the sensor area to the circuit area. This step requires the third additional mask.

10h- Annealing of polysilicon structure: This step is very important in reducing the internal stresses of the polysilicon. As was discussed earlier, Rapid Thermal Annealing (RTA) would be applied to cause mild influence on the electronic circuitry.

The rest of the process should go smoothly according the original process flow. However, step 37 should be modified to the following sequence:

37a-Depositing of passivation SiO_2: This remains unchanged and the SiO_2 will be deposited all over the wafer to protect the circuit area.

37b-Patterning of passivation SiO_2: This step is very important for this particular case to ensure that the next passivation layer (passivation Si_3N_4) will come into contact with either polysilicon or silicon nitride as illustrated by Figure (4.2a). This step requires the fourth additional mask which is a coarse mask and its alignment is not that critical.

37c-Deposition of passivation Si_3N_4: This remains unchanged and PECVD Si_3N_4 will be deposited all over the wafer to protect the circuit area. When the Si_3N_4 comes into contact with either polysilicon or silicon nitride then this should form a lateral etch stop barrier to the final etching of the sacrificial SiO_2.

With the conclusion of this step, the modified process sequence, will come up to need a total of four masking steps, three having masks with critical alignment and one with coarse features and non critical alignment. The steps to follow are the standard packaging procedure with very little adaptation. The metal lids are better not be welded to the packages since the following step(s) needs the dice to be uncovered so that they would be exposed to the etchant. In fact, this is not so critical since the dicing and bonding are not so critical as processes. For this reason, it is often more convenient to do the final etching before the dicing. This becomes mandatory when a mask is needed in the final etching and that is the case for this design.

4.4-Post Fabrication Steps

As was stated earlier, this should be the last chemical step(s) of the device fabrication. It is meant to set the moving structure free without harming the electronic circuitry based on the selectivity of the etchant to the deposited materials.

Now it is already known that the moving structure is made of sensor poly under which, a sacrificial layer of dioxide is deposited. This sacrificial layer should be removed without even leaving a chance to the residuals to affect the sensor performance. This means that the actual etching time should be fairly longer than the theoretical one.

It is imperative here to get a relatively high etching selectivity. However, no matter how high this selectivity is, still it is finite. This means that certain situations will be source for worry. As an example, since the proof mass has a side length of 368 μm then the etching process should remove away all the sacrificial SiO_2 from underneath the 184 μm long polysilicon structure still maintaining the passivation layers on top of the circuit area in place or else the circuit will be damaged. The comparison of etching hundreds of microns of SiO_2 underneath the moving structure to the preservation of less than 1μm Si_3N_4 on top of the circuit area gives rise to this question "Can this selective etching be achieved depending on the SiO_2/Si_3N_4 selectivity?"

The other and equally important question is that will the Si_3N_4 used as lateral etch-stop between the sensor area and the circuit area hold for the prolonged etching time of the SiO_2 without giving the etchant a breakthrough to the circuit area?

The answers to these questions require thorough investigation and experimenting these different factors that control the etching time including the possible modifications required to facilitate this step. Before starting these experiments, it should be decided what type of etchant could be used to etch SiO_2 without having much influence over the polysilicon or the Si_3N_4 which should work as an etch-stop. The best choice of an etchant that eats away SiO_2 without having much of effect over silicon would be HF. Now is HF alone suitable to be used with Si_3N_4? The answer is absolutely not since Si_3N_4 dissolves in HF rather fast but with the addition of NH_4F as a buffer, things will be so much better for Si_3N_4 yet not much different for SiO_2. This mixture of HF and NH_4F is known as Buffered Oxide Etchant (BOE) and it comes with different ratios of NH_4F to HF starting from 4:1 and going upwards. The higher is the number, the lower is the portion of HF in the mixture. Figure (4.3) illustrates the effect of adding the Ammonium Fluoride upon the etch rate of LPCVD nitride.

The fact that the etch rate of SiO_2, Si_3N_4 or any other deposited material, in most of the

etchants change according to the deposition conditions like temperature and pressure as well as the concentrations of the etchant, was already explained.

It is very important to recall the fact that this sensor has planar dimensions in hundreds of microns, yet the vertical dimensions of only few microns. Should they be allowed to be subjected to the same etchant during the final etching?

Since the passivation used in this process is a stack of PECVD Si_3N_4 on top of SiO_2 and the thickness of each is less than 1μm then a lot of precautions should be taken in the etching process. Considering this scenario of relying upon Si_3N_4 to protect the dioxide underneath it in the circuit area (taking for the sake of argument that the etch ratio of LTO/ LPCVD Si_3N_4 is convenient). The etching will have to progress laterally for hundreds of microns which will take a long time and assuming (which is a valid assumption) that there is that very small spot where the passivation Si_3N_4 was very thin. What will happen is that the BOE will break through to the SiO_2 and further more to the circuit with a good chance of spoiling the whole circuit by dissolving the gate oxide of a key transistor in the circuit. In order to reduce the viability of that very dramatic scenario then two measures have been taken:

1-In order to drastically reduce the etching time, a uniformly dispersed openings were created inside the proof mass. They are 30 μm separated which makes the longest path to be etched 15 μm rather than 184 μm since the etchant will be attacking the dioxide from both sides. This results in an important saving in etching time despite the undeniable degradation those openings will impose upon the mechanical properties. In order to minimize the degradation in the mechanical properties, the, those openings should better be made of circular shape. The reason is that a circular shape has the least stress concentration factor of all, yet have the disadvantage of being harder to achieve as a mask since most of mask making processes for microelectronics go only according to the Manhattan geometry. In fact, it is only the micromachining trend to go otherwise. The creation of these openings is also associated with reducing the damping in the Z direction and can be a considerable loss of mass. In order to help the etchant infiltrate through these openings and allowing the gases, produced from the chemical reaction, to escape, then the size of the opening should not be very small and 5 μm squares seem to be reasonable.

2-Depending upon the quality of the passivation PECVD Si_3N_4, a photo resist might be

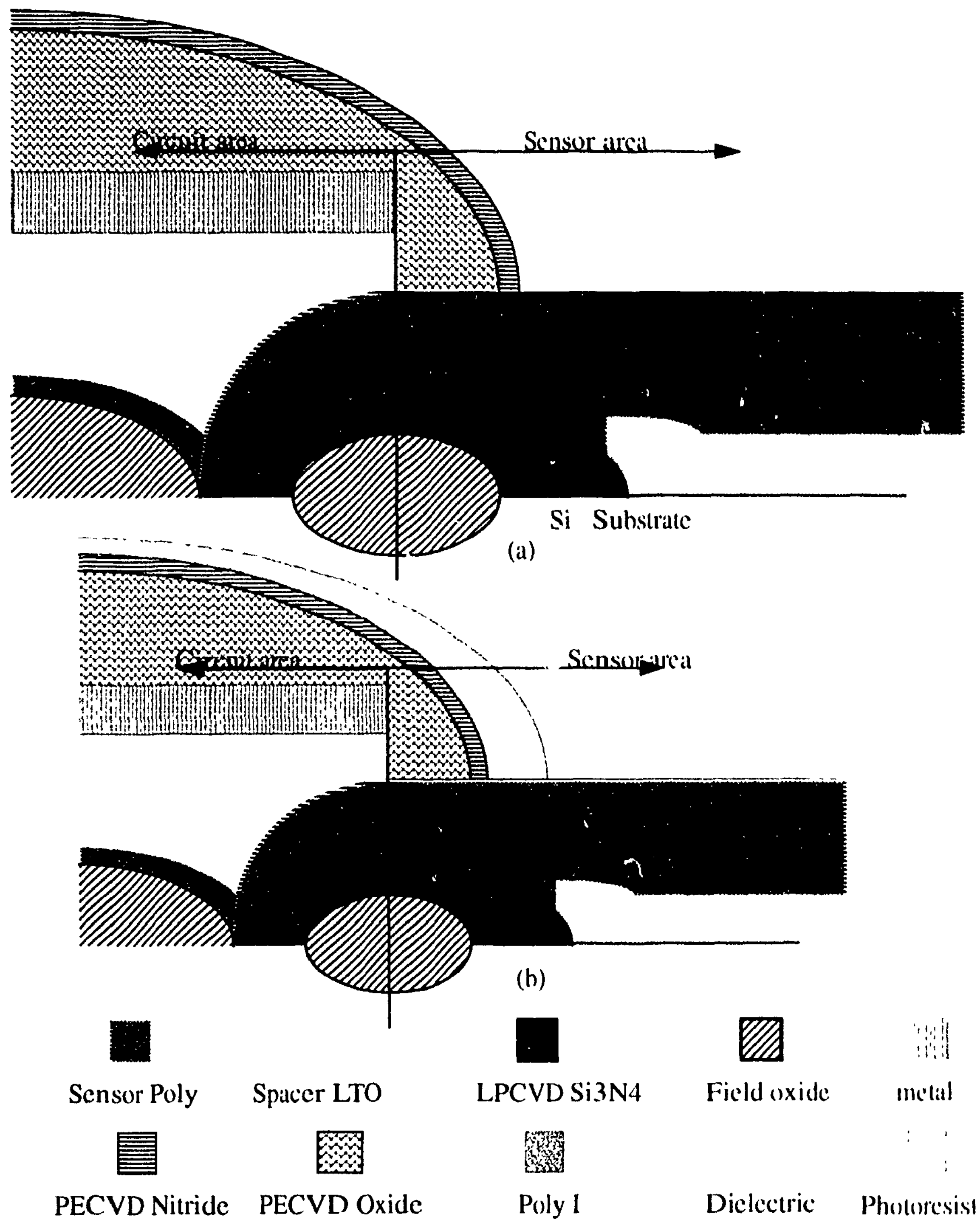

Figure (4.2): *(a) The suggested arrangement for the Circuit/Sensor area interface.*
(b) The application of photoresist for final etching.

deposited on top of the passivation layer during the final etching and that would almost ensure that the circuit will not be harmed. Note that a coarse mask will be needed to pattern the photoresist. However, the mask that was intended to pattern the passivation dioxide will no longer be needed. This restores the total number of additional masks to four.

4.4.1-Etch Time Estimation and Etch Rate Measurements

In order to estimate the final etching period length and whether the LPCVD Si_3N_4 would work as a lateral etch stop then a series of experiments were conducted with materials of the same type of those used in the process and grown under the same conditions. Figures (4.3 -4.5) show the average etching rates in different ratios of HF/NH_4F in the BOE. It should be noted here that the etch rates given in those graphs are not very accurate and the etch rate expected for a sample deposited under the same conditions would be somewhere around the values given in these graphs. To go even more on the safe side, then the etching selectivity of SiO_2/LPCVD Si_3N_4 in BOE experiment was conducted with thermal oxide rather than LTO. The results would ensure that the etching would be viable and on the safe side in the worst possible scenario. The only time when LTO will be used will be while trying to estimate the real etching time. Notice that the selectivity of Thermal SiO_2/ PECVD Si_3N_4 in BOE was less than 4. Since the thickness of the PECVD Si_3N_4 layer in the passivation is less than 5000A°, (see Appendix [E]), then it is not reasonable to rely on it to stand alone as a vertical etch stop that protects the circuit area during the final etching.

4.4.2-Utilization of Photoresist in the Final Etching

The procedure of using the photoresist should be further clarified. During the discussion of the process flow, emphasis was put on the need for the passivation PECVD Si_3N_4 to come into contact with the primary LPCVD Si_3N_4 and encapsulate the circuit area. The overlap between these two layers should be as much as the longest distance of LTO needed to be etched (15 µm). This will ensure that the circuit will not be attacked from the sides since this joint will be guaranteed to hold. The overlap of the photoresist on top of that will leave no chance that the circuit would be harmed neither from the sides nor from the top. Figure (4.2b) shows the arrangement mentioned above, in details. Notice that the mask needed to pattern the photoresist is a coarse mask with a big tolerance in its alignment. After the final etching then the photoresist should be stripped away and the wafers should be thoroughly rinsed to make sure that no flakes from the photoresist are trapped underneath the freed structure.

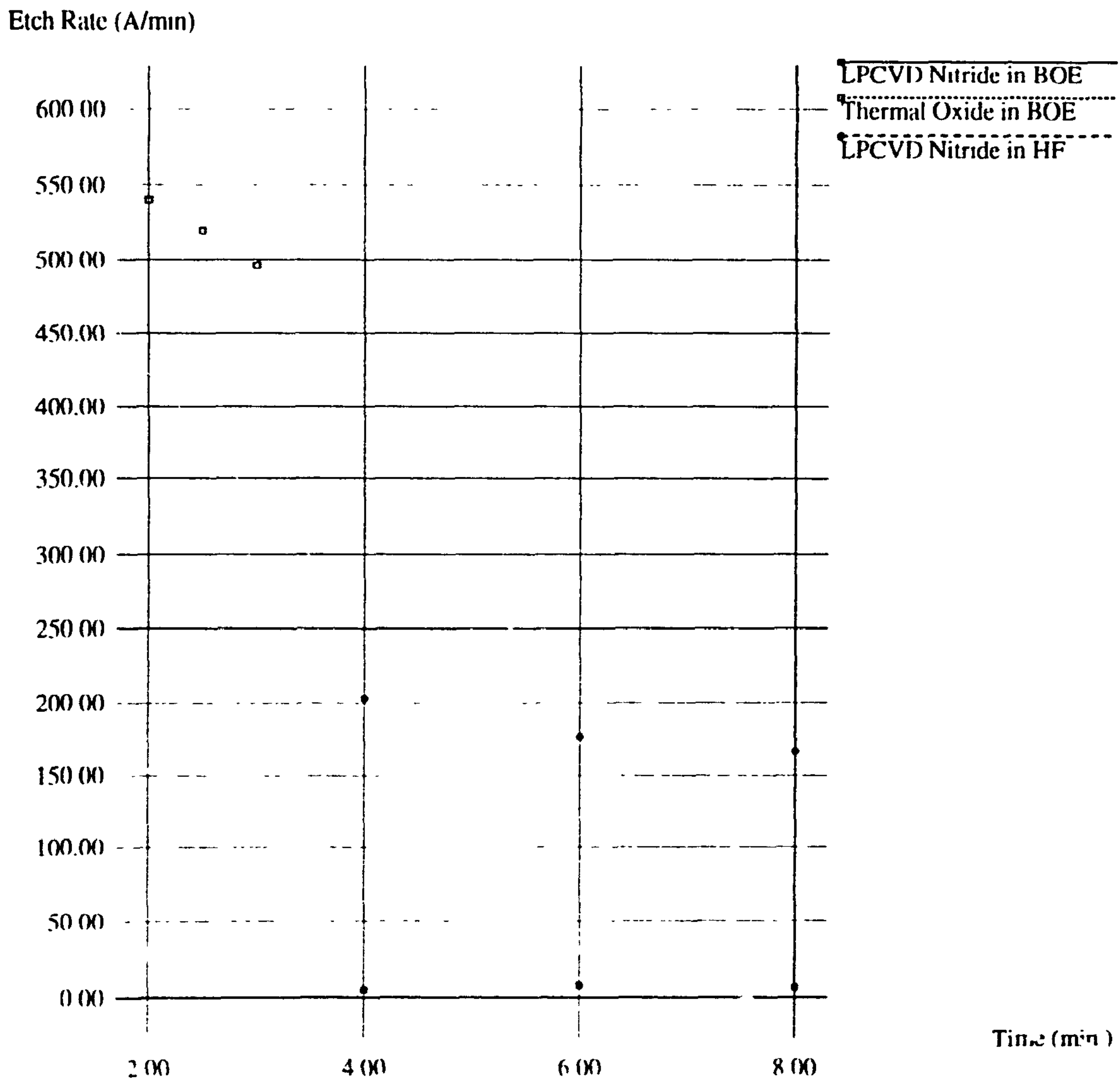

Figure (4.3): *Etch rate of LPCVD Nitride and Thermal Oxide in HF and BOE.*

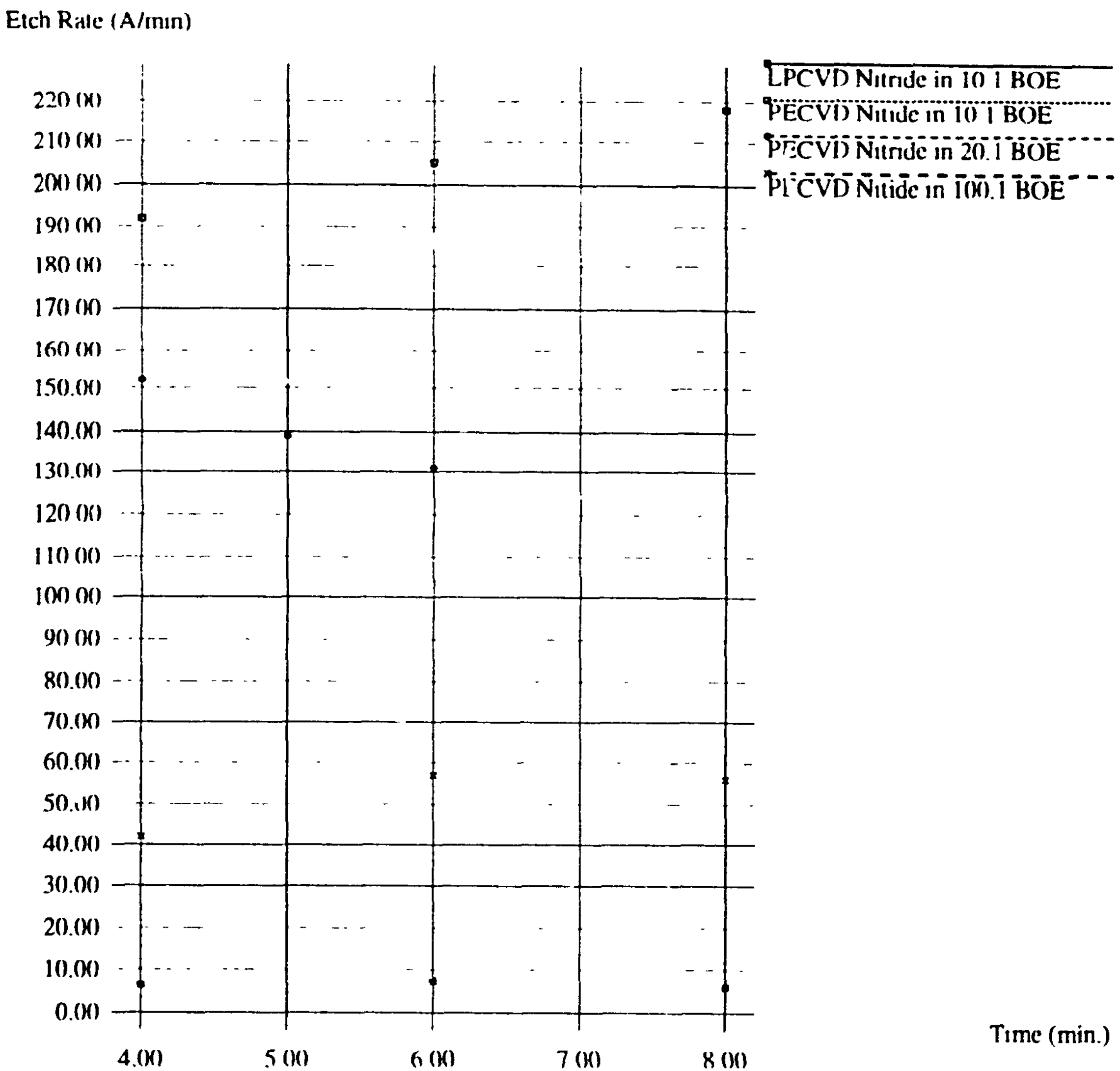

Figure (4.4): *Etch rate of PECVD Nitride in different BOE concentrations compared to Thermal Oxide in BOE.*

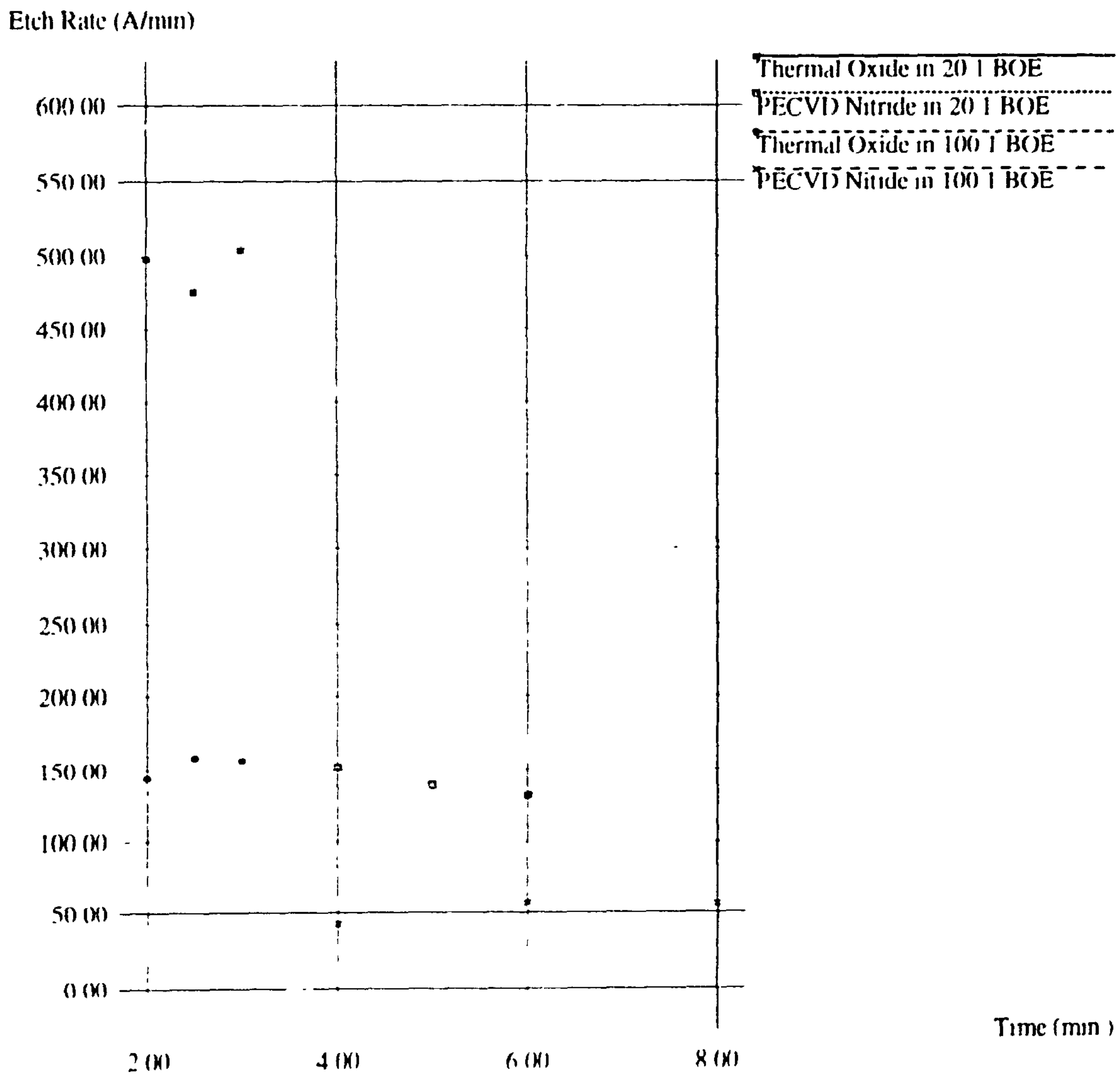

Figure (4.5): *Etch rate of PECVD Nitride and Thermal Oxide in different concentrations of BOE.*

4.4.3-Stiction

After the final etching then, in a way or another the wafers should be dried up. In doing this, the movable parts of the surface micromachined sensors were found to suffer from a very serious problem when a liquid is supposed to be removed from below those structures [19]. Under the influence of the surface tension of the liquid, those structures would be pulled down and often get stuck to the substrate (if the substrate was close enough) permanently even after the liquid had been totally removed. Releasing them back requires the application of mechanical forces strong enough to break these structures in most of the cases [19]. Special strategies were developed to deal with this problem some by changing the shape of the structures, others by changing the etchant and/or the drying process.

One way to reduce the chance of stiction is to pattern the LTO to have multiple circular shaped recesses [19]. This is done using a masking step followed by timed etching. Once the sensor poly is deposited on top of that LTO, those recesses will be reflected as dimples on the lower surface of the sensor poly. These dimples would play an important role in reducing the surface tension, yet this extra masking step needs a fine mask with critical alignment and that seems to unduly increase the device cost.

An alternative that looks more convenient than the dimples is to change the properties of the rinsing fluid (DI water) by dissolving another fluid, like Methanol, in it [33]. The solution that results, would be close to its triple point at room conditions. The fluid is then cooled down to freezing at normal pressure then the wafers are placed in a heated vacuum chamber where the frozen fluid is forced to sublimation without passing by the liquid phase and consequently no stiction problems should take place. Using pure DI water has the disadvantage of the need to be supercooled from room temperature to be safely lower than its triple point (0.0076^{o}C) [40]. This 20°C supercooling might cause extensive change in volume and therefore, extensive damage to the structure is expected

Appendix [F] explains the phase diagram in the vicinity of the triple point. It is clear from Figure (F1) that any change in temperature while keeping the chamber pressure below the pressure of the triple point will transfer the solid directly into the gaseous phase and vice versa. This effect is called "sublimation".

4.5-Summary of Conclusions for the Process Flow

Due to the diversity of issues discussed here, a summary of the conclusions is given here as follows:

1-Sensor material should be thick polysilicon. This polysilicon should be thermally treated for stress relieving. Rapid Thermal Annealing (RTA) might be a good way to anneal it. Due to some inconsistent results reported by different researchers, the annealing process, most compatible with the same type of sensor poly should be selected after examining different options.

2-Sacrificial layer should be of Low Temperature Oxide (LTO) of around 1.5 μm thickness.

3-The bulk of the added masking steps is after the field-oxide deposition.

4-LPCVD nitride can serve efficiently as a lateral etch stop against BOE. PECVD nitride can not serve as a vertical etch stop against BOE and photoresist should be used to cover it from top.

5-Sublimation should be used to avoid surface tension-related stiction

CHAPTER 5: Electromechanical Simulation

So far, both the behavior of the mechanical system and the behavior of the electrical circuit were dealt with as separate units. The model that was described so far, gives the impression that the mechanical forces, only, are driving the mechanical structure and the resultant position of the mechanical system will determine the electrical output. In reality, this is not true since the electrical circuit itself would exert a mechanical force upon the mechanical system as electrostatic forces in a feedback arrangement. The electrostatic force between two parallel capacitor plates is governed by the formula:

$$F_e = \frac{1}{2} \cdot \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d_0^2} \cdot (V - V_0)^2 \qquad (5.1)$$

where F_c is the electrostatic force, $\in_0$ is the permittivity of free space, $\in_r$ is the dielectric constant of the medium, A is the surface area of capacitor, d_0 is the distance between the plates and $(V-V_0)$ is the voltage difference between the plates.

If the plates happened to be fixed at constant voltages (no electrical feedback), then the resultant feedback would be positive since the closer the plates will come, the higher the electrostatic attraction will be and vice versa. In other words, the application of a specific value of acceleration usually causes a certain deflection to the pure mechanical system. This decrease of spacing between the plates will increase the electrostatic force which in turn, will decrease the clearance even more.

In this case, there are two capacitors consisting of three plates (as was described earlier). This would have made the positive feedback even stronger since one side will be strengthened when the plates come closer while the other side will be weakened. Both changes on either sides would be added to the acceleration force and thus, increasing the positive feedback.

In the circuit arrangement described in Chapter (3), the central plate would change its voltage with respect to the non-inverting terminal of the OPAMP (as mentioned earlier). Accordingly, what will happen when acceleration is applied is that the moving, central, plate will move towards a certain plate, depending upon the direction of acceleration. As

a result of decrease/increase in clearance. the value of the capacitor will increase/decrease respectively causing the voltage of the central plate to approach that of the closest plate. This in turn. will act against the resultant increase in electrostatic force caused by the decrease/increase in clearance and tend to reduce the positive feedback of the electrostatic force.

The electrostatic feedback will show its influence or might even dominate the system behavior where the mechanical spring of the system is not strong enough. This depends upon the range of the applied force, because the mechanical spring is almost independent of the change in clearance while the electrostatic spring changes with the clearance. If the mechanical spring is strong enough, then it would dominate the behavior when the changes of clearance are small (within the linear range of the sensor) while the electrostatic force will start to dominate the behavior whenever the moving plate is forced to go very close to any of the other fixed plates as in the case of strong shocks.

Refer to Figure (A1) for illustration. The electrostatic force is given by:

$$F_E = F_L - F_R = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{2 \cdot (d_0 - \delta)^2} \cdot (V_L - V_\delta)^2 - \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{2 \cdot (d_0 + \delta)^2} \cdot (V_R - V_\delta)^2 \quad (5.2)$$

where V_R is the voltage of the plate right to the moving plate, V_L is the voltage of the plate left to the moving plate and V_δ is the voltage of the moving plate at position δ.

5.1-Constructing the Differential Equation

Looking at the moving plate in Figure (A1) again, the forces acting on it can be summarized as follows:

a-Acceleration force: This force is the result of the externally applied acceleration. Its value is simply counted by multiplying the mass of the moving structure times the externally applied acceleration. The measurement of this acceleration is the soul goal of building this sensor and it is different from the acceleration with which the proof mass will be moving.

b-Damping force: This is the force that tries to hamper the movement of the structure due to the "Squeezed Film Damping" that was already mentioned in Section (2.2). It is

valid to take this force to be linear with the velocity of the moving structure with the damping coefficient (b) as the slope. This force works against the applied acceleration and thus takes a different sign from the applied acceleration. It is worth noting that this force is often confused with friction forces. The difference is that friction forces are tangential to the moving surface that depend on the nature of the two surfaces undergoing that friction (The roughness of the upper/lower surface of the sensor) and the viscosity of air. The drag force, on the other hand, is normal to the surface and depends on the relative speed of movement, the surface area normal to the force and the clearance between the moving structure and the surrounding walls. In that sense, they usually coexist but depending upon the speed of movement, the roughness of the surfaces and the normal surface area, it will be decided which one will be the dominant. As combined effect, they are called "The damping force".

c-Mechanical spring force: This force is due to the mechanical structure which shows a behavior that can be represented by a spring as was discussed earlier in Section (2.1). The spring force is a linear function of deflection with a slope (k_s). This force also works against the applied acceleration and takes a different sign from the applied acceleration. It should be noted that intrinsic stresses play an important role in deciding the value of the spring constant.

d-Electrostatic attraction to the left (F_L): This force was just discussed above. For convenience, consider the movement of the middle plate to the left to be associated with positive acceleration. That gives the electrostatic attraction to the left, F_L the same sign of the applied acceleration.

e-Electrostatic attraction to the right (F_R): According to the convention set above, this force acts against the applied acceleration and should take a different sign from the applied acceleration.

f-The resultant force: This is the net force acting on the moving structure. It will act to push the moving plate in an acceleration that is proportional to its own weight. Keeping the same convention, this force will take a different sign from the applied positive acceleration.

The force balance of the moving plate can be written as:

$$m \cdot \frac{d^2\delta}{dt^2} = m \cdot a + F_L - F_R - b \cdot \frac{d\delta}{dt} - k_s \cdot \delta \qquad (5.3)$$

where δ is the displacement of the moving plate that was established earlier in Section (1.4.1). Its second derivative with respect to time would be the acceleration with which the free structure would be moving. It is absolutely different from the acceleration that the sensor is measuring. It is only after the plate reaches steady state when the reading can be declared to be reliable.

Equation (5.3) is a linear ordinary differential equation of the second order. It can be easily simulated using analog computers. However, the same goal can be achieved by running the analog simulation using digital computers. In order to make that compatible with electronic simulation then HSPICE is used to run that simulation.

5.2-HSPICE Simulation of the Mechanical Element

The commercially available electronic simulation package (HSPICE) does not support analog simulation directly. However, it offers multi-dimensional controlled sources with polynomial nonlinearities. Therefore, analog computer elements like summers, multipliers, dividers and integrators can be constructed and used, together with HSPICE netlist, to solve this differential equation [41]. Appendix [G] shows the construction of the HSPICE compatible analog simulation elements. HSPICE supports transient simulation then all the variables, except time, are represented as voltages including the voltages applied to the plates. The applied acceleration is represented by a time dependant voltage source. For the time being, it is easier to ignore the electrical feedback resulting from the change in the values ot the capacitance due to the displacement of the middle plate. Also, fixed DC voltages were applied to the capacitor plates instead of the actual case of the switched voltage applied by the real circuit.

Figure (5.1) shows HSPICE simulation of the mechanical system alone. It is a direct implementation of Equation (5.3) In this simulation arrangement, the attempt was to reduce, as much as possible, the diversity of the numbers (the simultaneous presence of very large values alongside very small values) resulting from the simulation. This was done by arranging the sequence of operations e.g. dividing a small number by another small number before multiplying it by a third small number. This would help to avoid the

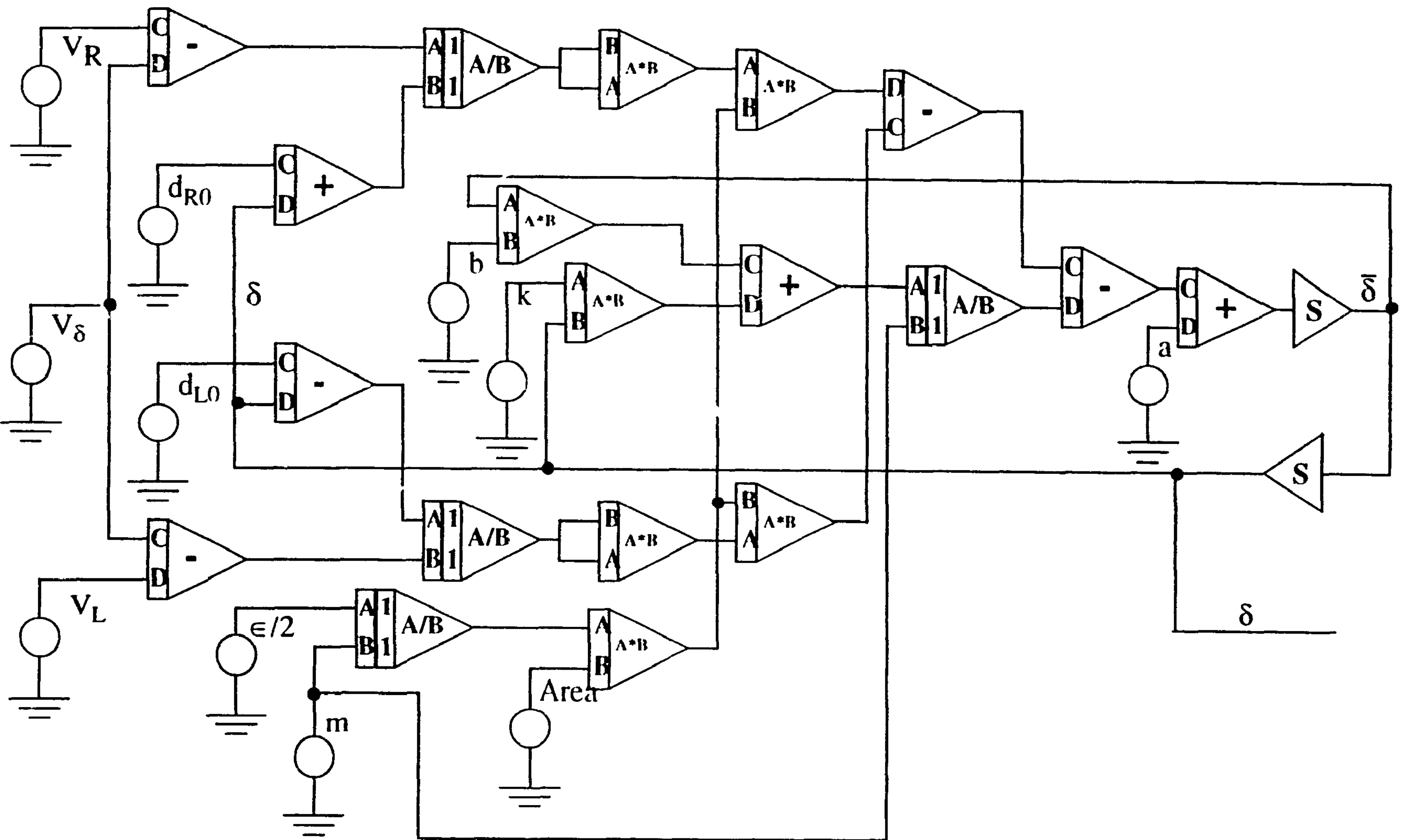

Figure (5.1): *Analog Simulation of the Mechanical System.*

generation of a very small number during the solution. This strategy helps both convergence and the reduction of the truncation errors.

In order to determine the values of the constants including the coefficients, the distances and the voltages (all applied as voltages), then refer to Chapters (2), (3) for those values. The value of the damping force coefficient (b) should be measured practically but since that can not be practically done until the device is fabricated, then an educated guess based on similar structures was taken. In the X or Y direction, this value of (b) should be around 1×10^{-4} N.m/s [18]. This value plays a very important role in the determination of the transient response, as was described earlier in Section (2.2) but, has nothing to do with the steady state values.

The output from this simulation (δ) represents the displacement of the middle plate and consequently, the values of the capacitances can be easily reconstructed from the new position of the middle plate.

In this numerical simulation there are numerical errors associated with this solution. In this case and in order to ensure the DC convergence, an inevitable increase in the relative error convergence limit of HSPICE (RELV) was to be made. Its final value was a little bit more than the default value of HSPICE which is set at 1×10^{-3}. However, as far as this simulation is concerned, the accuracy seems to be very good as will be demonstrated in Chapter (6).

Running this simulation program requires other adjustments in HSPICE options in order to ensure transient convergence. Appendix [H] contains a sample HSPICE code that shows the formulation of the simulation program and HSPICE options to be modified. Among these options that should be modified, the value of RMIN which sets the minimum value of the internal time step. In this case, its value was reduced to one tenth of the default value of HSPICE. This means increasing the transient simulation time to ten times in some cases.

5.3-Simulation of the Mechanical Element Combined with the Electrical Circuit

The previous section was about carrying out the simulation of the mechanical system

while ignoring the electrical feedback. Practically the electrical feedback plays an important role that can not be ignored. Even more, the electrical circuit was not included in the simulation yet. The objective is to lump the whole sensor (mechanical and electrical parts) in one model. This means the representation of the movement of the free structure by the change of the values of the sensor capacitors while applying the switched reference voltage to the capacitor plates. This requires the utilization of a voltage controlled capacitor and that is not supported by HSPICE. This problem was overcome by employing this active sub-circuit arrangement whose resultant behavior within the circuit is equivalent to that of a Voltage Controlled Capacitor as shown in Appendix [I]. It is clear that this arrangement gives the effect of capacitance multiplied by (V+1) rather than V. Hence, that extra Volt should be subtracted from the voltage before it is applied to the voltage controlled capacitor. Since the voltage applied to the voltage controlled capacitor stands for the spacing between the plates, then the value that substitute for C (see Appendix [I]), should be the area of the plates multiplied by the permittivity of the air.

In order not to run into stability problems, no direct connection is created between the simulation of the mechanical system and the simulation of the electrical circuit. Instead, voltage controlled voltage sources are used with unity gain. This implies that the voltage of the plate follows the voltage of that node in the circuit without enforcing a connection between them.

Now, both mechanical and electrical systems were incorporated together then the feedbacks is expected to appear. One of the problems that was expected to surface would be the case that the central plate would not be in the middle of the fixed plates even at zero acceleration. This would be due to some unbalance in the electrostatic forces even without an applied acceleration. It might also cause the loss of symmetry of the sensor characteristics between the negative and positive accelerations.

Figure (5.2) shows the arrangement for simulating the sensor in open loop arrangement. In this case, more increase to the value of the relative error (RELV) was made to ensure the DC convergence of the solution. This causes a little bit more of errors in the solution for the operating point. Once the correct link between the mechanical and electrical systems is established, then any other modifications to the circuit can be done almost freely. It is almost guaranteed to have the new simulation working provided that the tolerance is increased even more for the more sophisticated design, as in the case of closed loop arrangement. In order to obtain the steady state solutions for the electrical signals then a

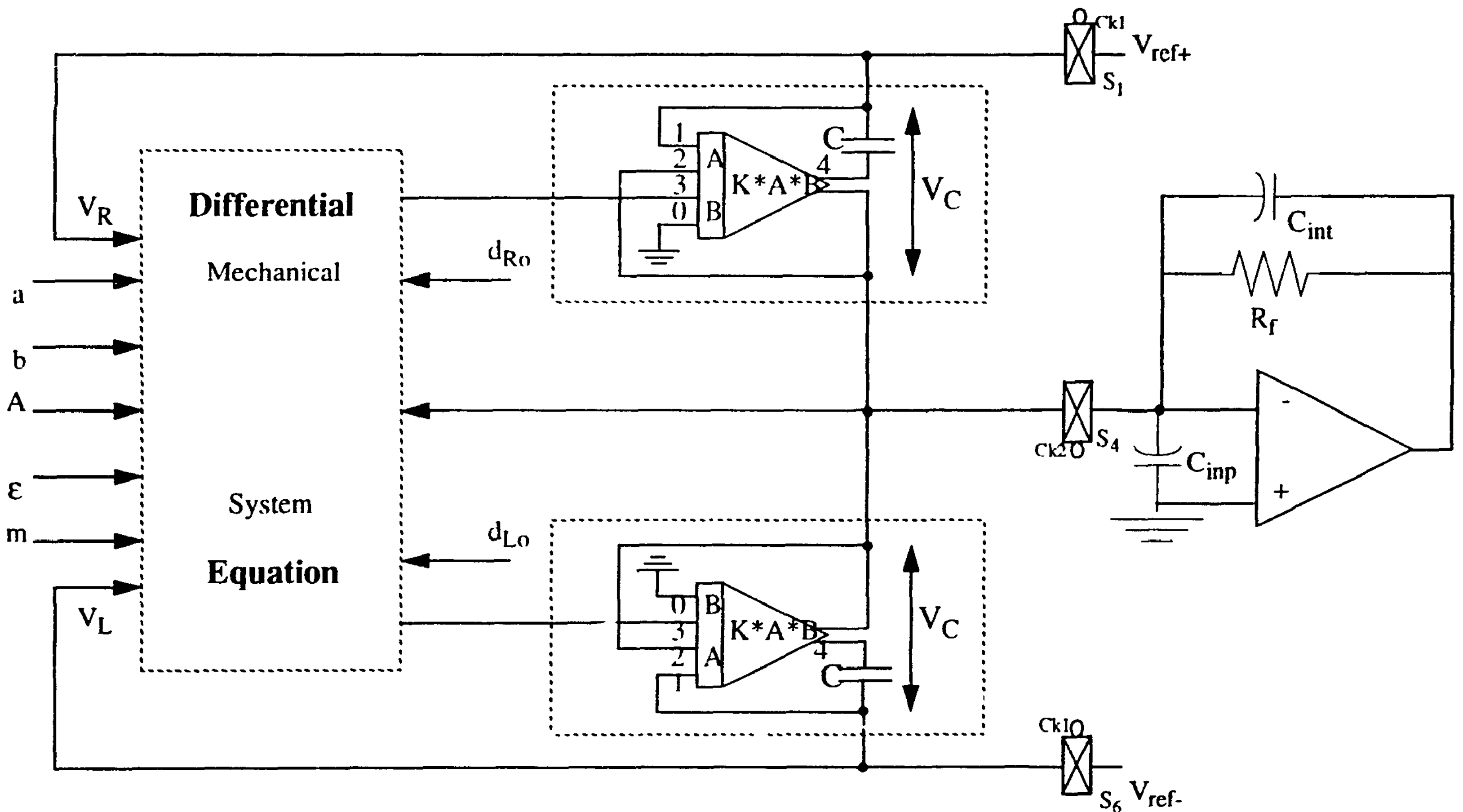

Figure (5.2): *Simulation of the lumped model in the open loop arrangement.*

transient simulation over a prolonged time period is a performed. Often, a single-run simulation needed more than 4 hours to complete.

CHAPTER 6: Results and Conclusions

HSPICE simulation runs were performed in three parts to validate the sensor operation. First the electronic circuit was tested alone to ensure its functionality. Then the mechanical element was simulated alone. Finally, the combined model was simulated to take into consideration the interaction between the electronic subsystem and the mechanical subsystem.

6.1-Simulation Results of Electrical Circuit

The simulation of the electrical circuit was run using HSPICE into two consecutive steps.

6.1.1-Simulation Results of the 1-Dimensional Circuit

In order to ensure the basic circuit functionality, HSPICE simulation for the 1-D circuit was performed. Also, a range of reference voltages was swept to help achieve the following:

a-Prove that the dynamic range of the circuit increases with the value of the reference voltage (V_{ref}) applied to the circuit as a verification to Equation (3.2).

b-Find the ultimate value of V_{ref} that achieves the highest possible dynamic range.

Figure (6.1) shows the change of circuit output voltage with the change of the sensor differential capacitor for values of $|V_{ref}|$=2.8, 2.9, 3.0, 3.05, 3.1 V respectively. It is clear that, over the desired range of change in differential capacitance (±20 fF), the results are fairly linear. Moreover, they show that the dynamic range increases with V_{ref}. This is consistent with Equation (3.2).

In order to check the resolution of the same results above, Figure (6.2) was drawn as a zoom on the central part of Figure (6.1) in the vicinity of the zero capacitance difference. It shows that some non-linearities have started to appear when V_{ref}=3.1V. For the value, V_{ref}=3.05V, it is better, yet less than acceptable and the highest acceptable characteristics

were associated with V_{ref}=3V. This proves that the prediction of the presence of an upper limit for V_{ref}, mentioned in Chapter (3), was justified. On the other hand, this also shows that the circuit performance is sensitive to the value of the reference voltages which makes it rather susceptible to temperature drifts over wide temperature of operating temperatures. That might require the use of reference voltage circuits in order to stabilize the circuit performance over the required temperature range (in case it was very wide or in case there was a rigorous limitation imposed over the temperature coefficient of the circuit output).

Figure (6.1) shows that the slope for each curve is different. Evidently, it increases with the value of the reference voltage. Figure (6.3), shows a plot of the dynamic ranges of the curves in Figure (6.1) versus the value of their corresponding reference voltages. Not surprisingly, the result was close-to-linear again. This is consistent with Equation (3.2).

Figure (3.1) shows that the circuit after the integrator is nothing but an RC LPF followed by a buffer stage then another RC LPF. Since the gain of the passive LPF is a function of the frequency only and it should not change with the amplitude of the signal and the buffer gives a uniform and very close to unity gain, then the circuit after the integrator has a combined gain which is constant with respect to the output signal.

The straight line of Figure (6.3) is the product of Equation (3.2) times the combined gain of the LPFs and the buffer (G_c). From the slope of Figure (6.3), the values of R_f, f_c and the span of differential capacitance, the value of the combined gain was found to be Gc=0.76. In other terms, the combined efficiency of the filters and buffer is 76% which is nable value. This supports the circuit behavior as was described by Equation (3.2).

Up to this point, the output voltage was considered to be the DC value of the steady state output. However, from the transient AC response, it was noticed that the output signal had a peak voltage that was repeatable and allows a sensitivity of 1.3 times the sensitivity obtained from the steady state value. This discovery was promising yet, capturing the peak value proved to be difficult. The problem is that the peak lasted only for less than a microsecond. With the limitations of the 1.5 μm process, it was difficult to construct a peak detector fast and accurate enough to capture the value and make use of it in the measurements. As a result of this difficulty, the steady state DC value of the output signal was taken as the signal to be measured.

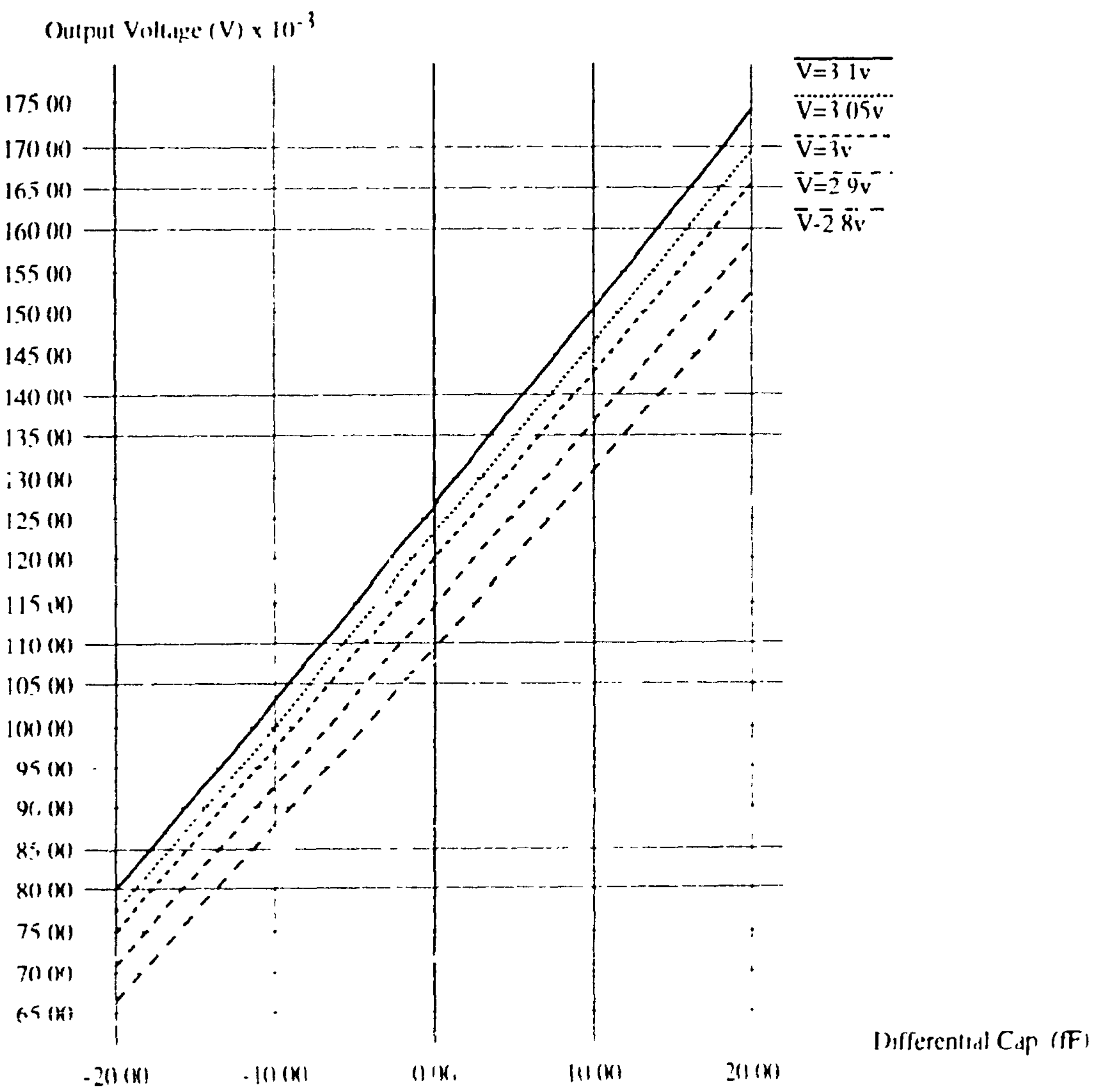

Figure (6.1): *Output Voltage vs Differential Cap for Different Reference Voltages.*

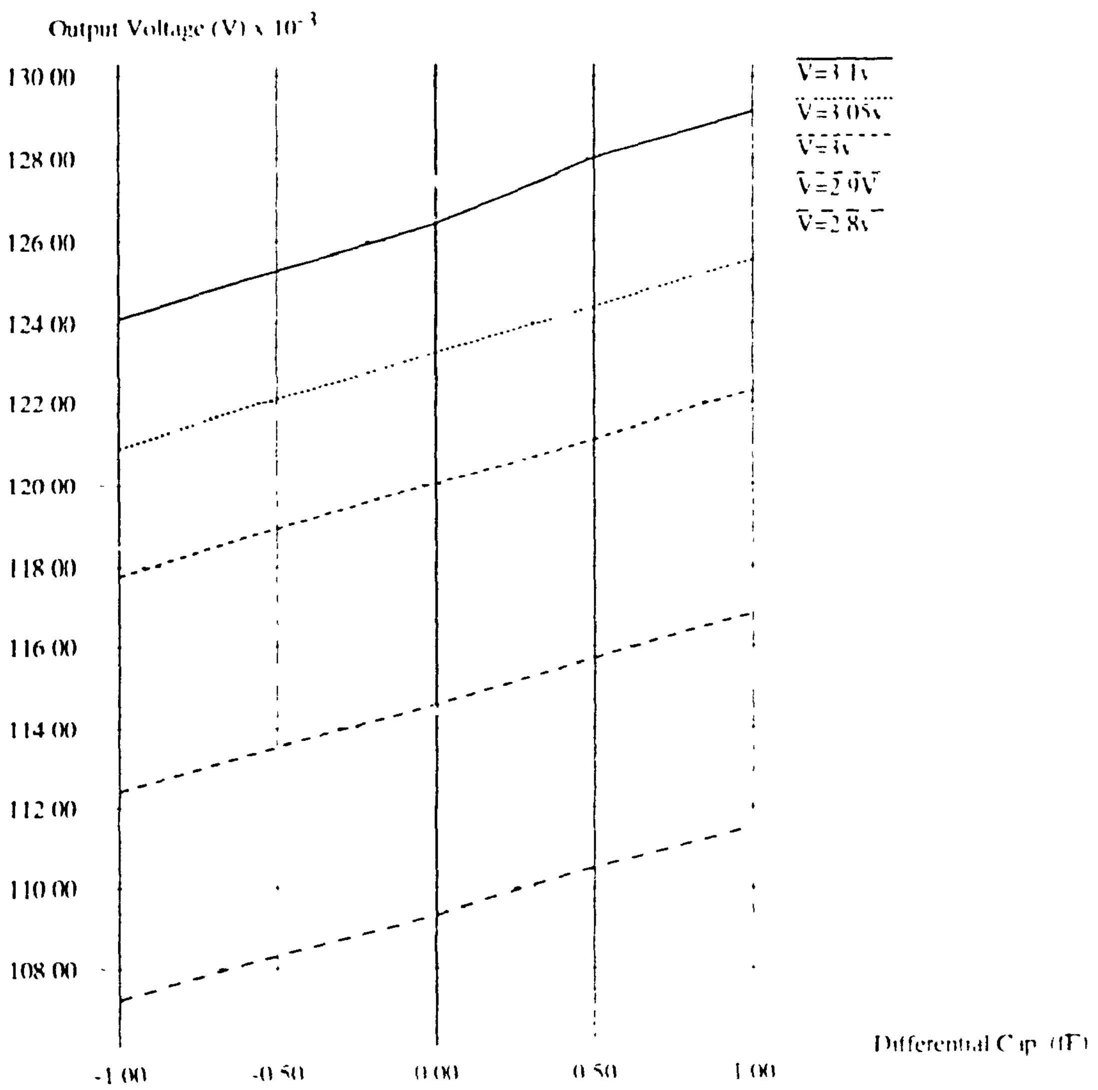

Figure (6.2): *Output Voltage vs Differential Cap for Different Reference Voltages Blown up around the Zero Differential Cap*

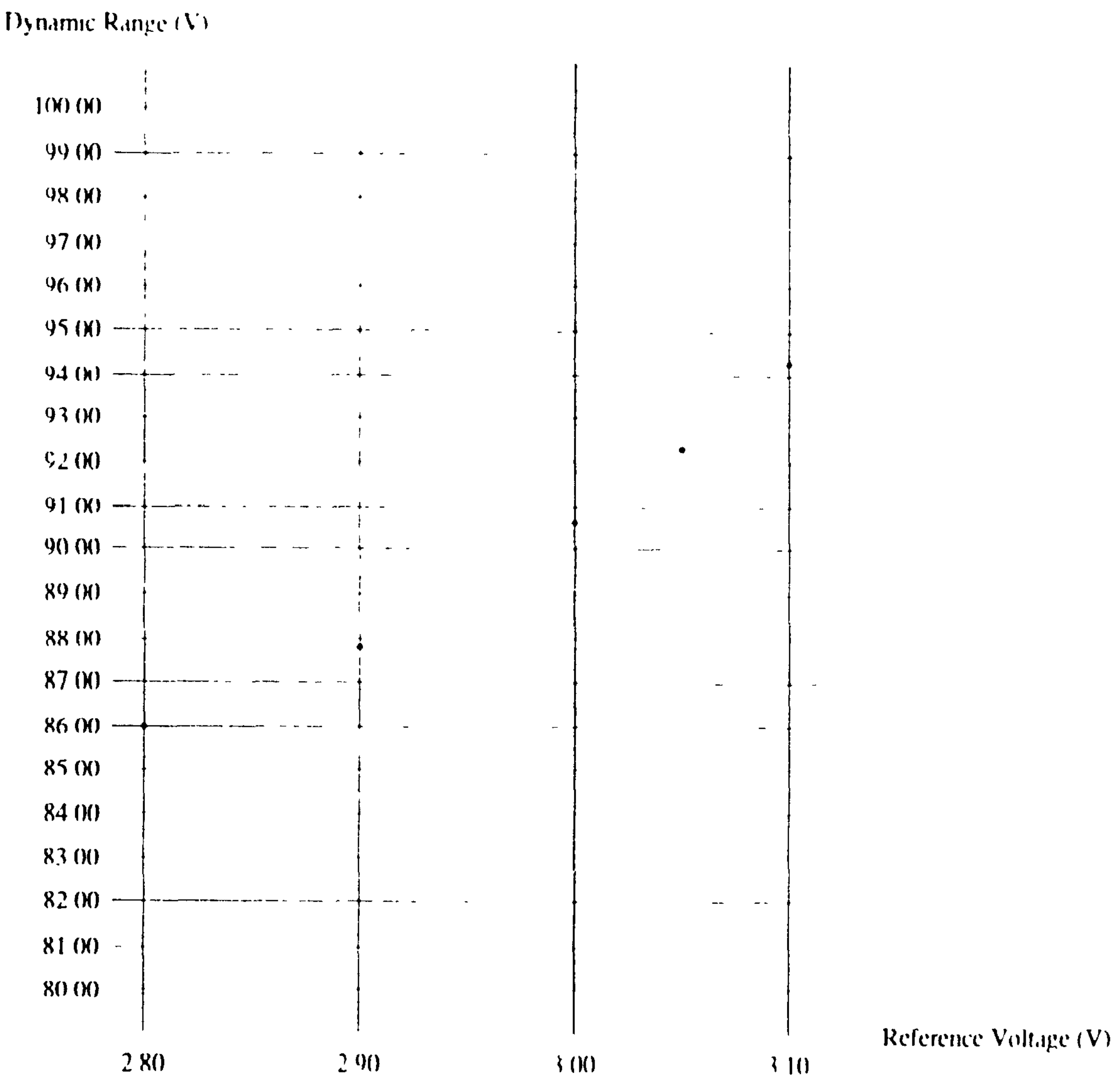

Figure (6.3): *Dynamic Range vs. Reference Voltage.*

6.1.2-Simulation Results of the 2-Dimensional Circuit

Having ensured the operation of the 1-D circuit and having obtained its optimum reference voltage. now the concept of sharing the same common plate (the moving plate of the sensor) by the capacitors in both X and Y directions is verified. A series of simulations was carried out to sweep the full range of the sensor capacitors. The HSPICE file for the circuit is listed in Appendix [D]. The reference voltage was fixed at $|V_{ref}| = 3V$. The results are shown in Figure (6.4) for the full range of change of capacitance (-10% to +10% of the zero-acceleration capacitor) as output voltages versus differential capacitance for both X and Y directions.

It is clear from Figure (6.4) that both circuits have the same gain (slope), yet there is a very little difference in the voltage of the zero differential capacitance crossing. Figure (6.5) is a detailed graph for the central part of Figure (6.4) which proves that the resolution of the circuit is acceptable.

6.2-Simulation Results of the Mechanical Element

It is evident that Equation (5.3) at steady state will be reduced to Equation (1.3) plus the influence of the electrostatic force. In order to verify the validity of the simulation of the mechanical element, and to verify that the model fulfills the basic accelerometer static behavior described by Equation (1.3), a set of simulations was performed by changing the following parameters:

a-The applied acceleration: The deflection of the mechanical system is proportional to the applied acceleration and as shown by Equation (1.3). Figure (6.6) illustrates the deflection of the system as a response to the influence of different input accelerations. Curves 1, 3, 5, 7 and 9 show different values for the input acceleration. These values cover the full range of the input acceleration changes. Curves 2, 4, 6, 8 and 10 show the corresponding deflections respectively. Figure (6.6) shows clearly that the deflection follows the magnitude and direction of the acceleration which indicates the proper behavior of the element within 200 nm (0.2 μm) as full-scale deflection.

b-The mass of the sensor: The deflection is proportional to the mass of the sensor as shown by Equation (1.3). Figure (6.7) illustrates the deflection as response to the input

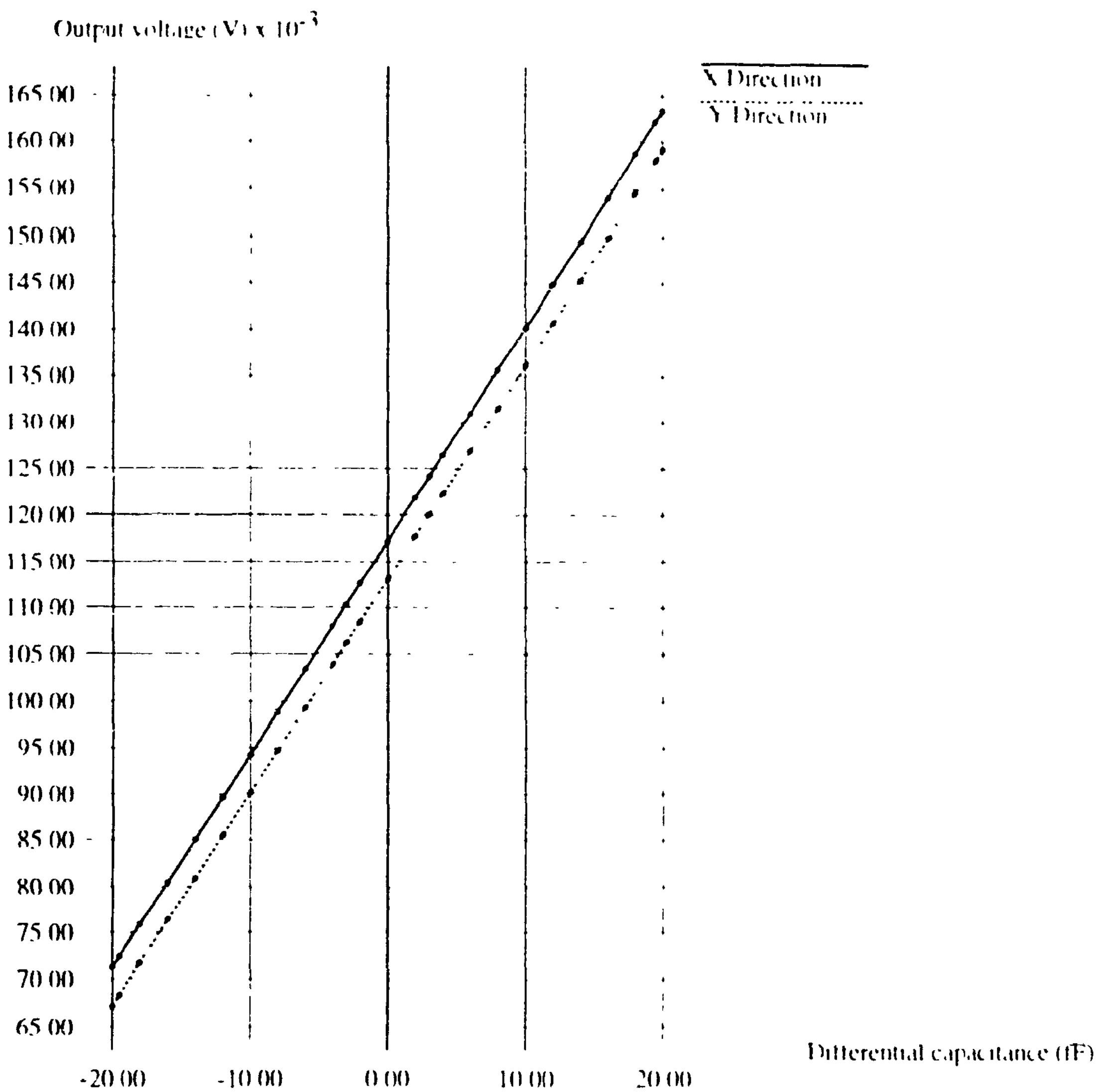

Figure (6.4): *Output Voltage vs. Differential Cap for the 2-D circuit*

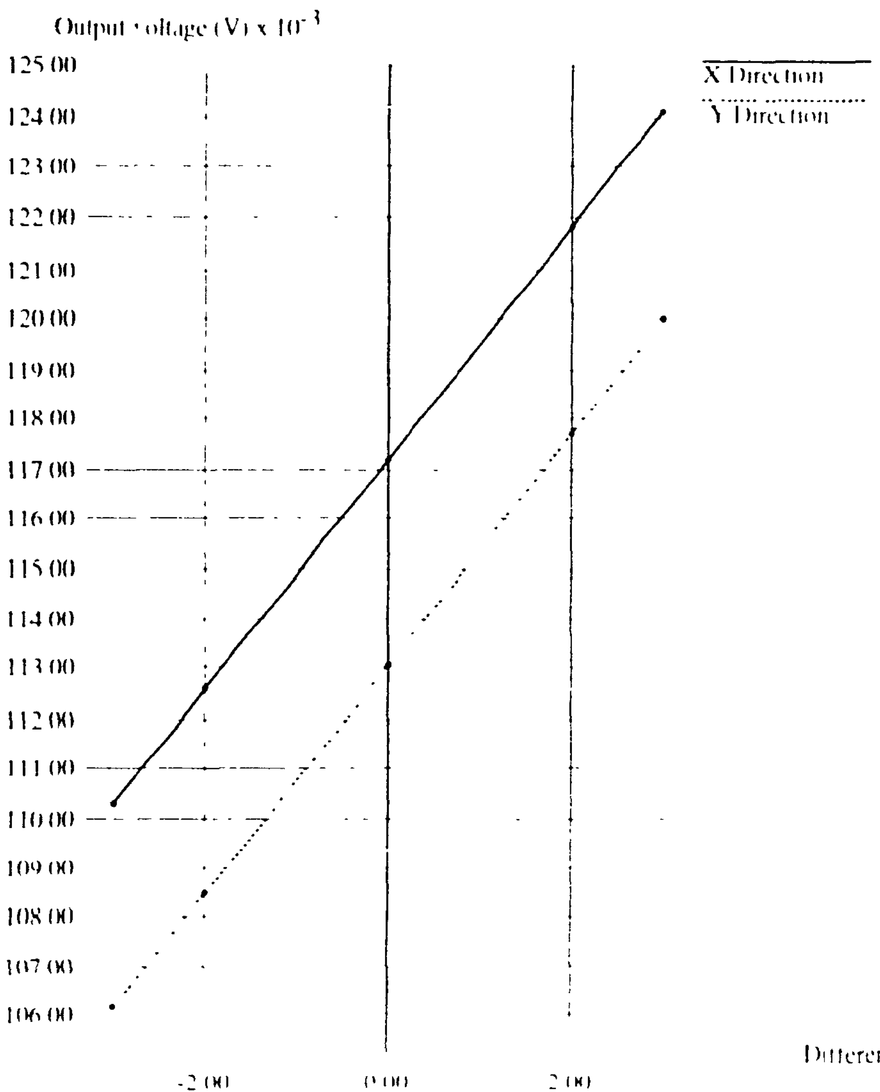

Figure (6.5): *Output Voltage vs. Differential Cap. Blown up around the Zero Differential Cap. for the 2-D Circuit*

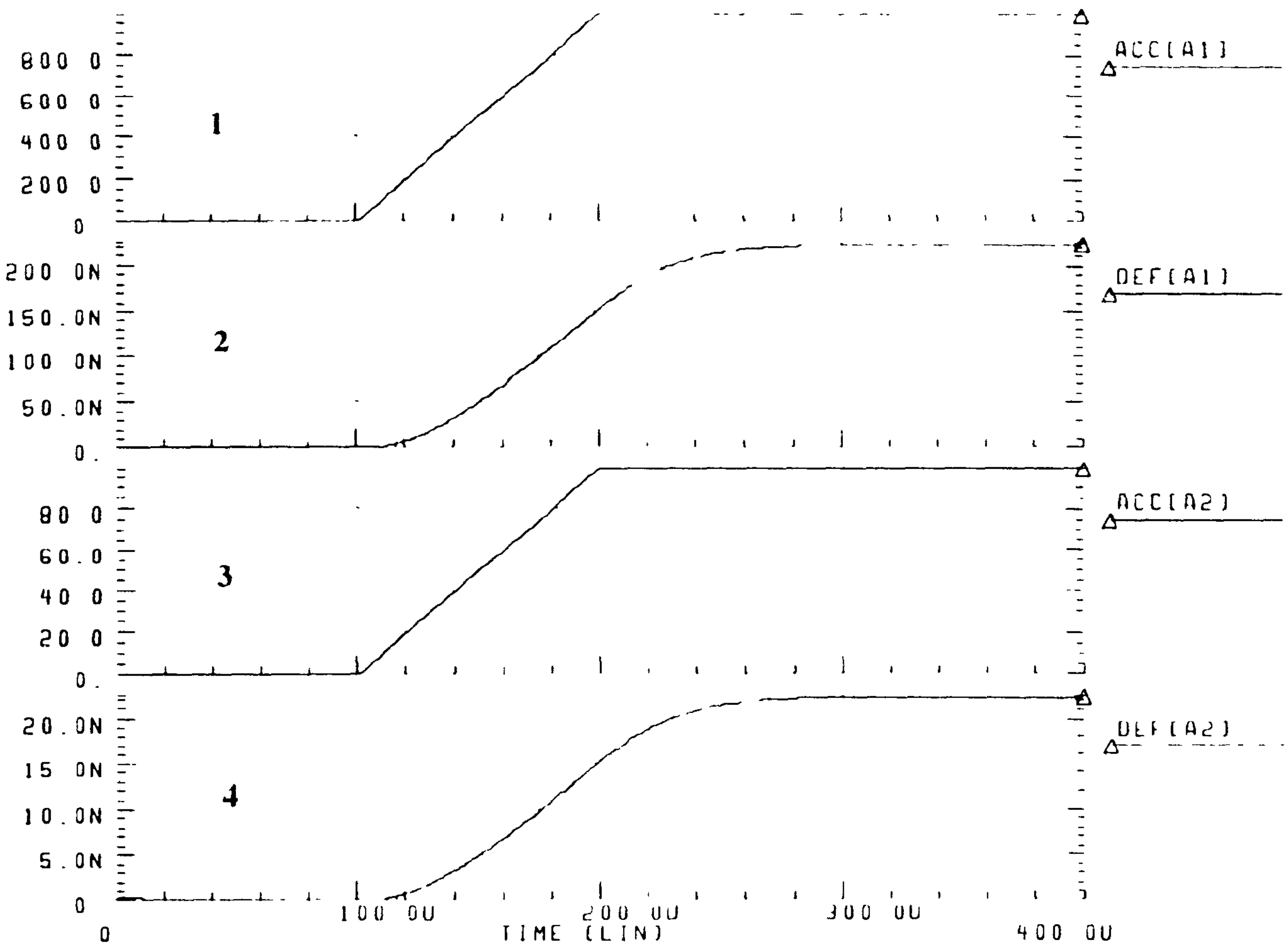

Figure (6.6): *Deflection (m) vs. Time (s) as a response to different values of applied Acceleration for the mechanical element alone*

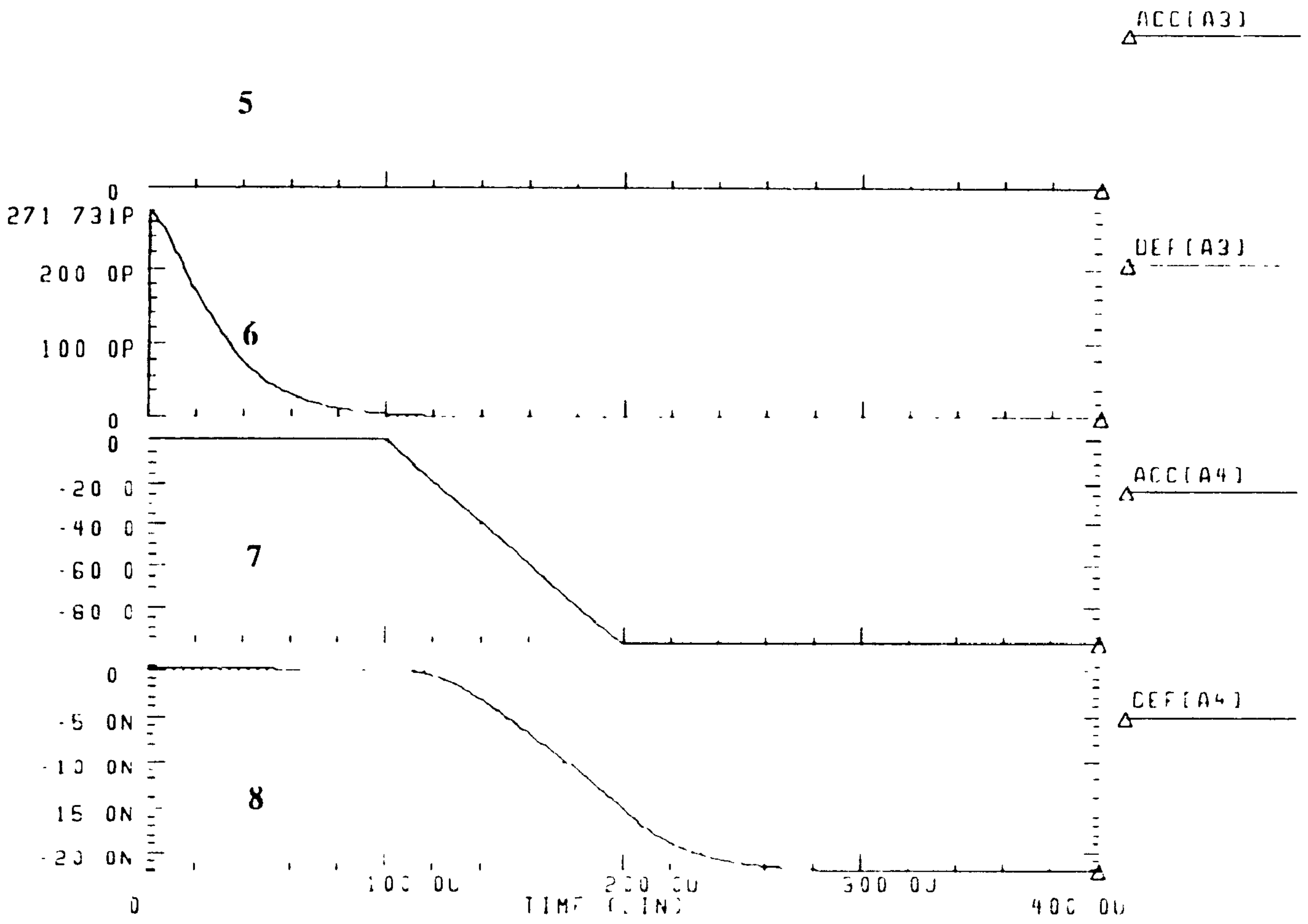

Figure (6.6) *(Continued)*

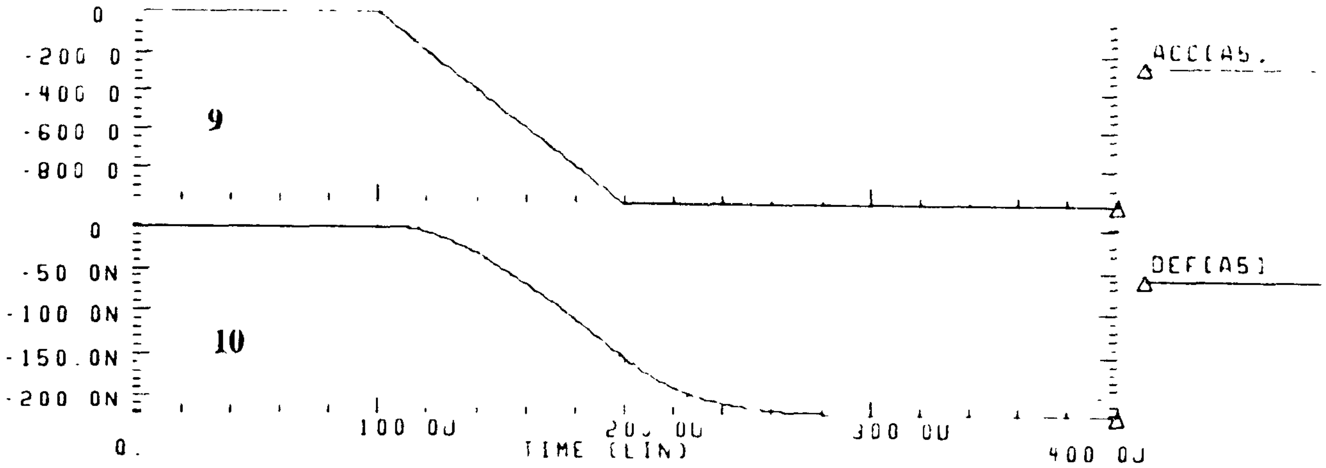

Figure (6.6): *(Continued)*

acceleration shown in curve 1 for different values of the proof mass curve 2 is the deflection when the mass is 7×10^{-10} Kg, curve 3 is the deflection when the mass is 1.4×10^{-9} Kg while curve 4 is the deflection when the mass is 3.5×10^{-10} Kg. Figure (6.7) shows that when the mass is doubled, then the deflection doubles while when the mass is reduced by the half, then the deflection follows. It is evident that the deflection is really proportional to the mass of the sensor.

c- The spring constant: The deflection is inversely proportional to the spring constant according to Equation (1.3). Figure (6.8) illustrates the deflection as a response to the input acceleration shown in curve 1 for different values of the spring constant. Curve 2 is the deflection when the spring constant is 3.4 N/m, curve 3 is the deflection when the spring constant is 6.8 N/m while curve 4 is the deflection when the spring constant is 1.7 N/m. Figure (6.8) shows that when the spring constant is doubled then the deflection is reduced to half while when the spring constant is reduced by half then the deflection is doubled. It is evident that the deflection is inversely proportional to the spring constant.

d- The reference voltage: The electrostatic force appeared as a term in Equation (5.3). This gives a positive feedback effect on the moving structure. In order to study the effect of the electrostatic force, the left and the central plates were kept at fixed voltages. Three simulations were carried out for three different voltages on the right plate. The corresponding deflections of the central plate as a response to the applied acceleration were monitored. Figure (6.9) illustrates the deflection as a response to the input acceleration of -98.1 N/m^2 (-10 g) shown in curve 1 for different values of the voltage applied to the right plate. Curve 2 is the deflection when the voltage applied to the right plate is 2.5 V and the voltage applied to the left plate was -2.5 V, curve 3 is the deflection when the voltage applied to the right plate is 2.3 V and the voltage applied to the left plate was -2.5 V, while curve 4 is the deflection when the voltage applied to the right plate is 2.0 V and the voltage applied to the left plate was -2.5 V. The positive feedback effect of the applied voltage is evident. It is clear that the zero-acceleration position of the middle plate was shifted towards the left plate with the decrease of the positive voltage applied to the right plate. Moreover, the value of the deflection as a response to the applied acceleration also increased with the change of voltage. The conclusion that can be drawn from it is that the electrostatic feedback of this system is rather strong compared to the mechanical resistance of the system that is represented by the spring constant. It can be seen from Figure

(6.9), that relatively small changes in the voltage make big differences in the steady state value. In case of the real sensor, this effect will be weaker since the absolute value of the effective voltages of the plates are even less than the values assumed here. This is due to the fact the duty cycle of the voltage is only 25% in this 4-Φ clock. Moreover, in real life, the voltage of the moving plate approaches that of the closest plate and consequently reduces the positive feedback. The most important conclusion from that is the fact that for such a sensor with such a strong electrostatic effect, the operation in a closed-loop arrangement will be very useful.

The steady state behavior given by the simulation was proven to be in consistence with the equations. Next, the dynamic behavior should be tested by changing the value of the damping coefficient and see the effect on the transient behavior of the system. Figure (6.10) illustrates the deflection as a response to the input acceleration shown in curve 1 for different values of the damping coefficient. Curve 2 is the deflection when the damping coefficient is 1E-4 N.m/s, curve 3 is the deflection when the damping coefficient is 2E-4 N.m/s while curve 4 is the deflection when the damping coefficient is 5E-5N.m/s. Figure (6.10) shows the delay of the transient behavior imposed by the increase of the drag force which, shows that the simulation results of the mechanical system are reasonable.

6.3-Simulation Results of the Electrical Circuit Combined with the Mechanical Element

A set of simulations of the electromechanical system in an open-loop arrangement was performed to ensure that the model describes both the electrical and the mechanical systems and their interaction with each other accurately.

Figure (6.11) illustrates the deflection of the central plate in response to different input accelerations. Curve 1, shows the input acceleration, A=98.1 m/s^2 whose associated deflection is shown in curve 2. Curve 3 shows the input acceleration, A=-98.1 m/s^2 whose associated deflection is shown in curve 4. The value of the of the reference voltages, V_{ref-} =-3.0 V and V_{ref+}=3.0 V. Figure (6.11) shows that the zero-acceleration position of the middle plate is initially influenced by the electrostatic forces and the moving plate ended up to be offset by almost 15 nm towards the negatively charged (right) plate. This is mainly due to the switching delay of the transmission gates which creates unbalanced

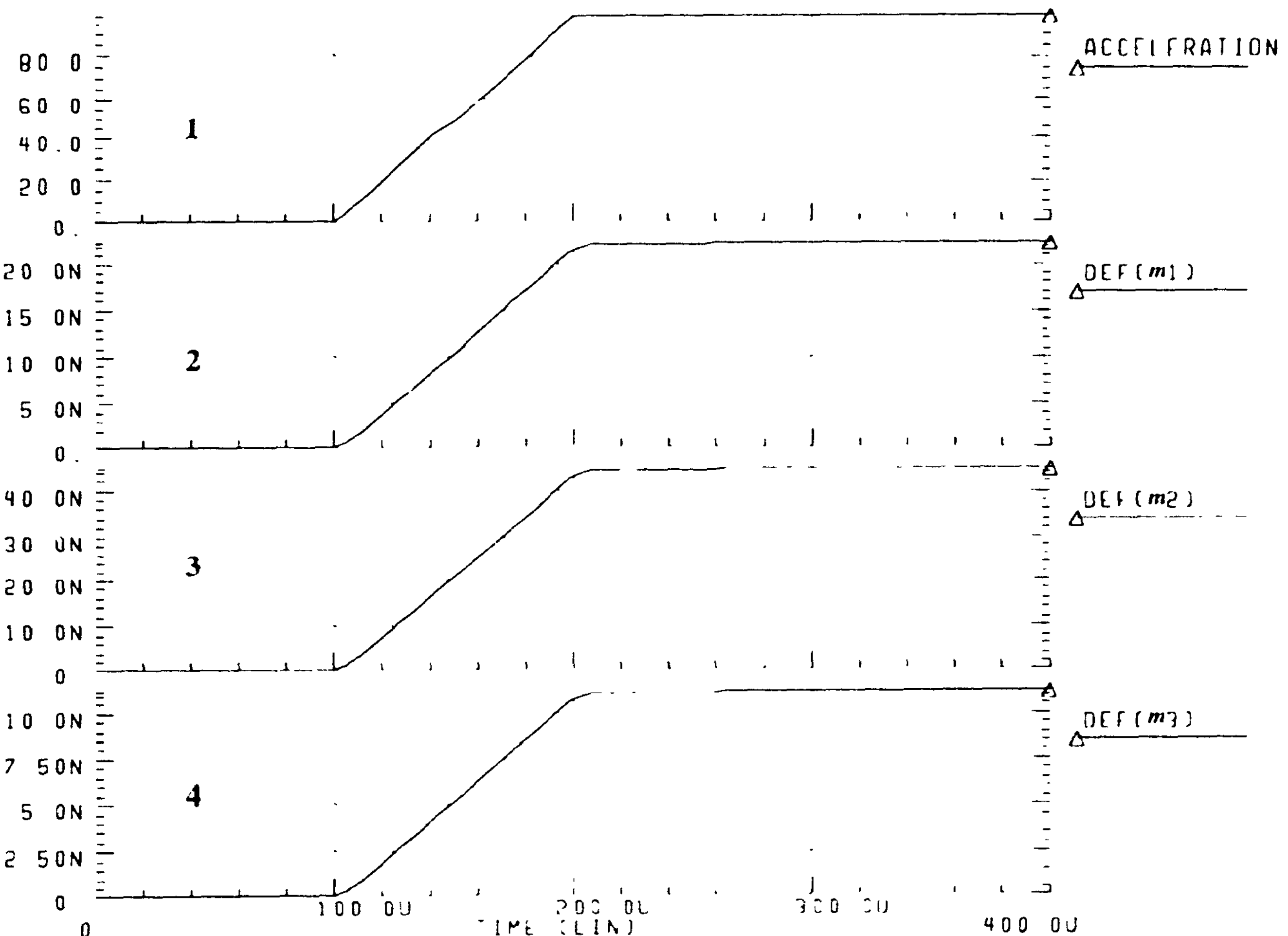

Figure (6.7): *Deflection (m) vs Time (s) as a response for Acceleration for different masses of sensor for the mechanical element alone*

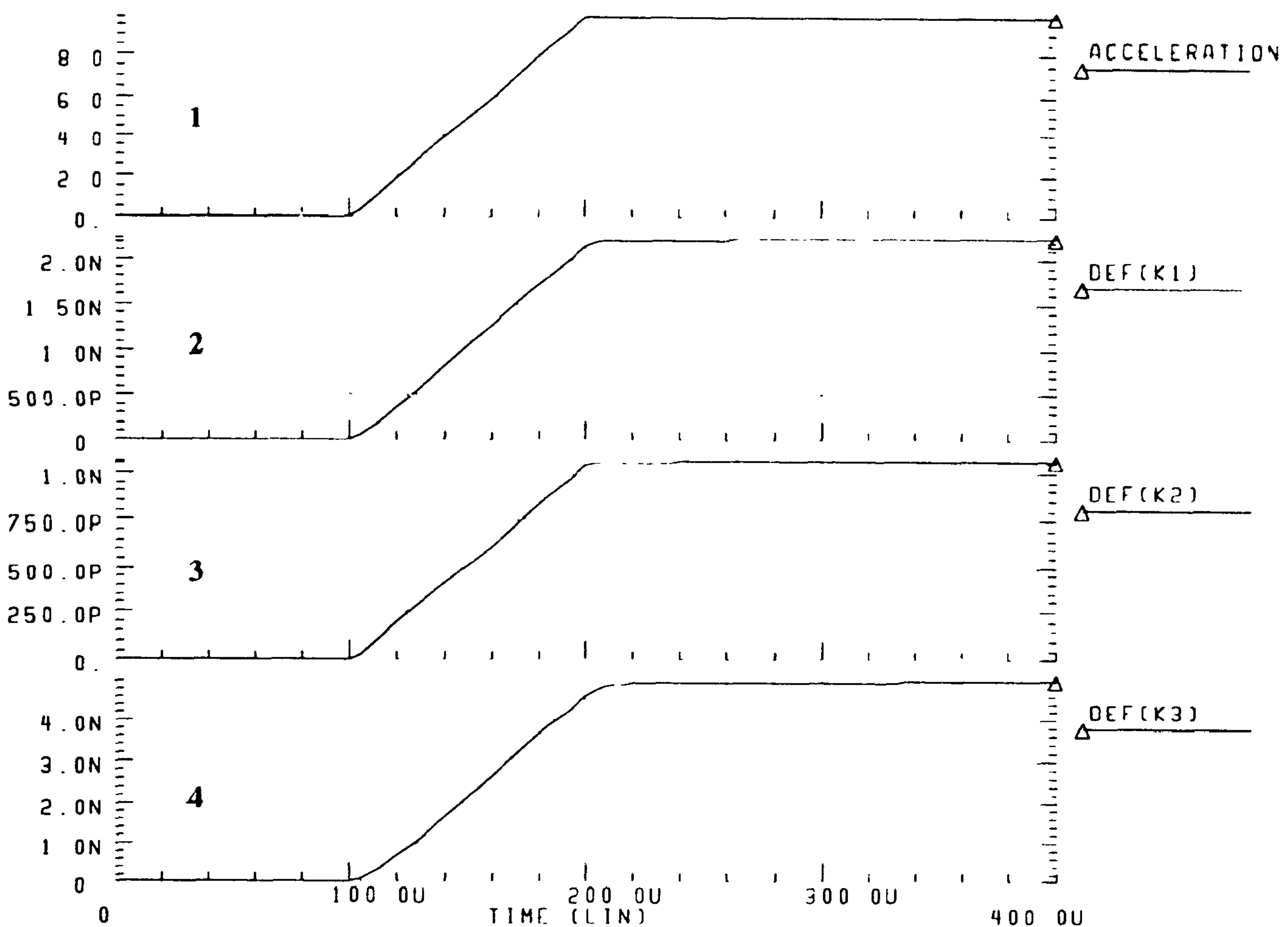

Figure (6.8): *Deflection (m) vs. Time (s) as a response for Acceleration for different Spring constants for the mechanical element alone.*

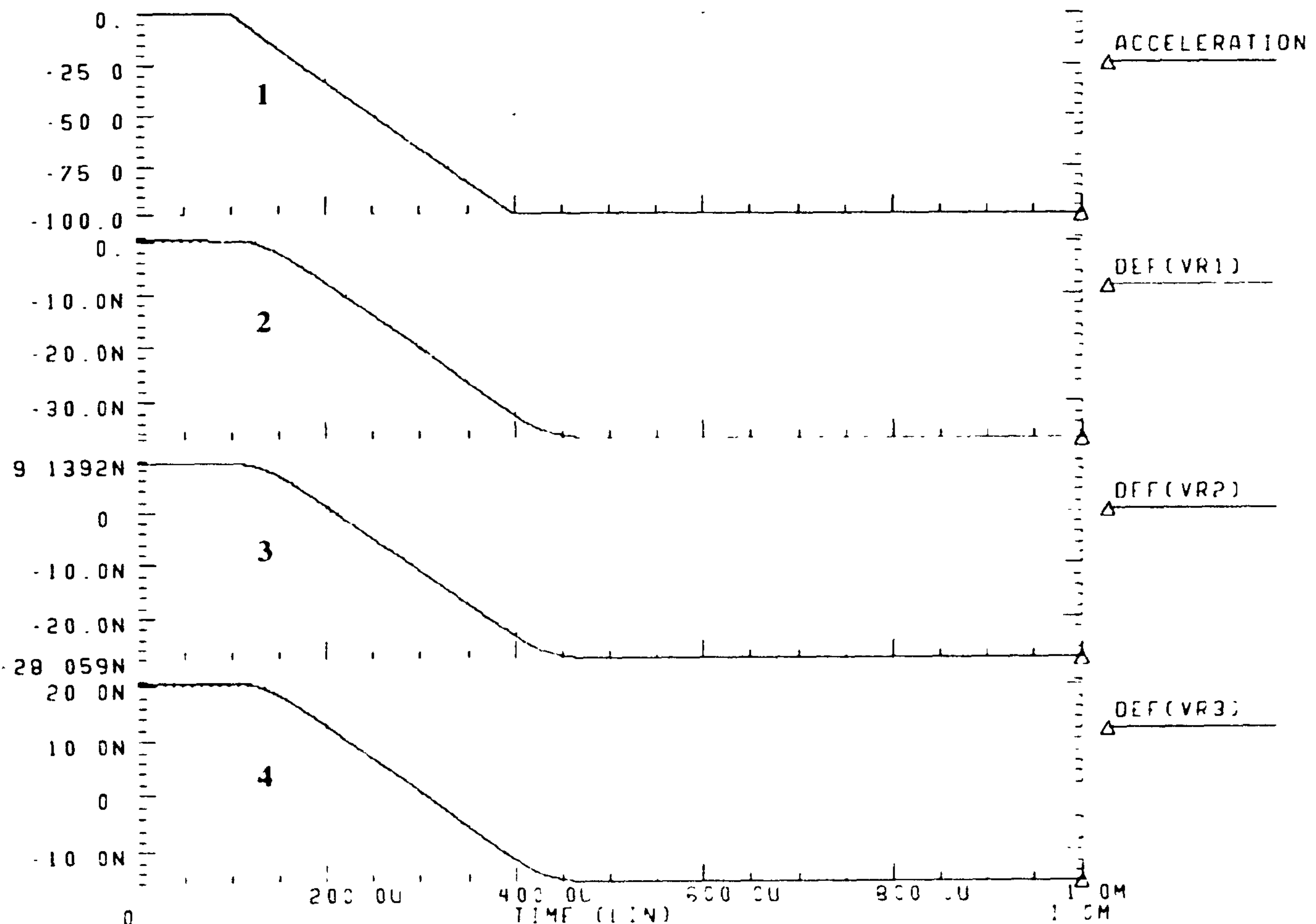

Figure (6.9). *Deflection (m) vs Time (s) as a response to an Acceleration for different reference voltages for the mechanical element alone*

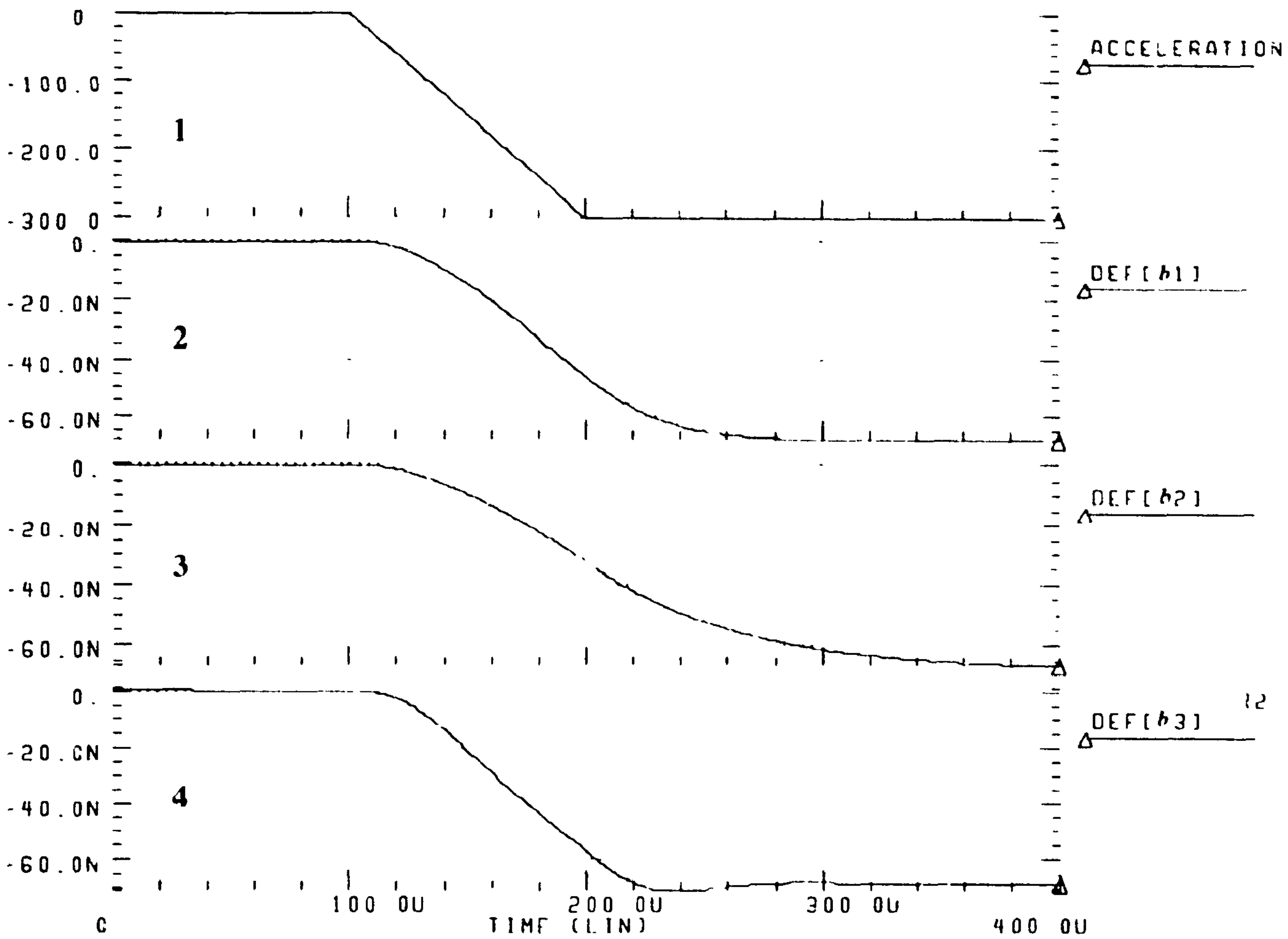

Figure (6.10): *Deflection (m) vs. Time (s) as a response to Acceleration for different Damping Coefficients for the mechanical element alone.*

voltages on the left and right plates. If negative and positive reference voltages of equal absolute values were applied, then due to the difference in the behavior of the switched transmission gates towards negative and positive voltages, the effective values of the voltages at the right and left plates would be different. Also, the moving plate does not have fixed zero voltage as was assumed in the simulation of the mechanical system since its voltage changes with its position according to the applied acceleration.

An important task was to find the values of the reference voltages to be applied to the sensor plates to ensure an electrostatic balance in the case of zero-acceleration. It should be noted that V_{ref+} and V_{ref-} are quite different from (Vdd and Vss).

To balance the central plate in the middle of the spacing between the right and left plates at zero-acceleration, the applied reference voltages should be adjusted. The adjustment was done by decreasing the negative reference voltage. The positive reference voltage was unchanged at 3.0 V. After a series of HSPICE simulations, the combination of V_{ref+}=3.0 V and V_{ref-}=-2.5 V was found to correct the offset.

Figure (6.12) illustrates the deflection of the central plate in response to different input accelerations. Curves 1, 3, 5, 7 and 9 show different values for the input acceleration. These values cover the full range of acceleration changes. Curves 2, 4, 6, 8 and 10 show the corresponding deflections respectively. Figure (6.12) shows clearly that the deflection follows the magnitude and direction of the acceleration which indicates the proper behavior of the element at steady state. The initial deflection offset of Figure (6.12) is not a real offset. It is due to HSPICE DC analysis. This offset is obtained only initially when the device is switched on and it will not affect the transient or steady state response of the accelerometer. This became very clear in curve 6 when the applied acceleration was zero and the steady state deflection was effectively zero. This sensor with adjusted reference voltages will be referred to hereinafter as the balanced sensor.

Figure (6.13) illustrates the deflection of the balanced sensor in response to the input acceleration shown in curve 1 for different values of the damping coefficient. Curve 2 is the deflection when the damping coefficient is 1E-4 N.m/s, curve 3 is the deflection when the damping coefficient is 1E-3 N.m/s while curve 4 is the deflection when the damping coefficient is 1E-5 N.m/s. curve 3 shows a typical over-damped behavior while curve 4

shows a typical under-damped behavior.

Achieving a balanced sensor is essential. Achieving it in the manner described above will reduce the sensitivity of the sensor. Figures (6.14), (6.15) show the effect of reducing the negative reference voltage over the linearity and the resolution of the sensor. These graphs reveal that the linearity is still the same and that the resolution is still acceptable. Figure (6.16) compares the output voltages between the case where the reference voltages were (3, -3 V) and the balanced case where the reference voltages are (3, -2.5 V). It is clear that the sensitivity had suffered. However, the balanced sensor has higher output voltages. Having a higher output voltage with the reduced $|V_{ref-}|$ is quite expected since less charges can be absorbed by the negative side.

The other option for balancing the system is to connect it in a closed-loop arrangement. This option, as was described earlier in Chapter (3) is not that easy to achieve. However, the same simulation method can be used to simulate the sensor in a closed-loop arrangement with minor modifications. It is worth noting here that the result that one might get for the gain of the fed back signal in the closed-loop arrangement is susceptible to big changes once the sensor is implemented. These changes would be imposed by the deviation from the design values of the mechanical spring, the average clearance between plates, the shape of the plates, the total surface area of the sensor and the behavior of the electronic circuitry.

Figure (6.17) shows the transient change of the output voltage of the sensor with the applied acceleration. Curve 1 is an input acceleration of 981 m/s^2 and curve 2 is the corresponding output voltage from the sensor. Curve 3 is an input acceleration of -981 m/s^2 and curve 4 is the corresponding output voltage. It shows that the output voltage is decreasing with the increase of the applied acceleration in the positive direction while it increases with the increase of the applied acceleration in the negative direction. This substantiates a valid link between the mechanical and electrical systems.

Figure (6.18) shows the steady state output voltages corresponding to 5 different input accelerations. The curve points to a linear relationship between the acceleration and the output voltage as was given earlier in Equation (3.3). It also establishes the sensor sensitivity at a value of 0.5 mV/g.

Figure (6.19) shows the mechanical response (deflection) and electrical response (output voltage) to a sinusoidal input acceleration of 1 KHz in frequency and 100 g in amplitude. The deflection is in phase and has a delay of 30 μs. The output voltage is anti-phase and has a delay of 50 μs.

The simulations shown in Figures (6.11-6.19) that were carried out for the electromechanical model prove that the model demonstrates the behavior expected from an accelerometer.

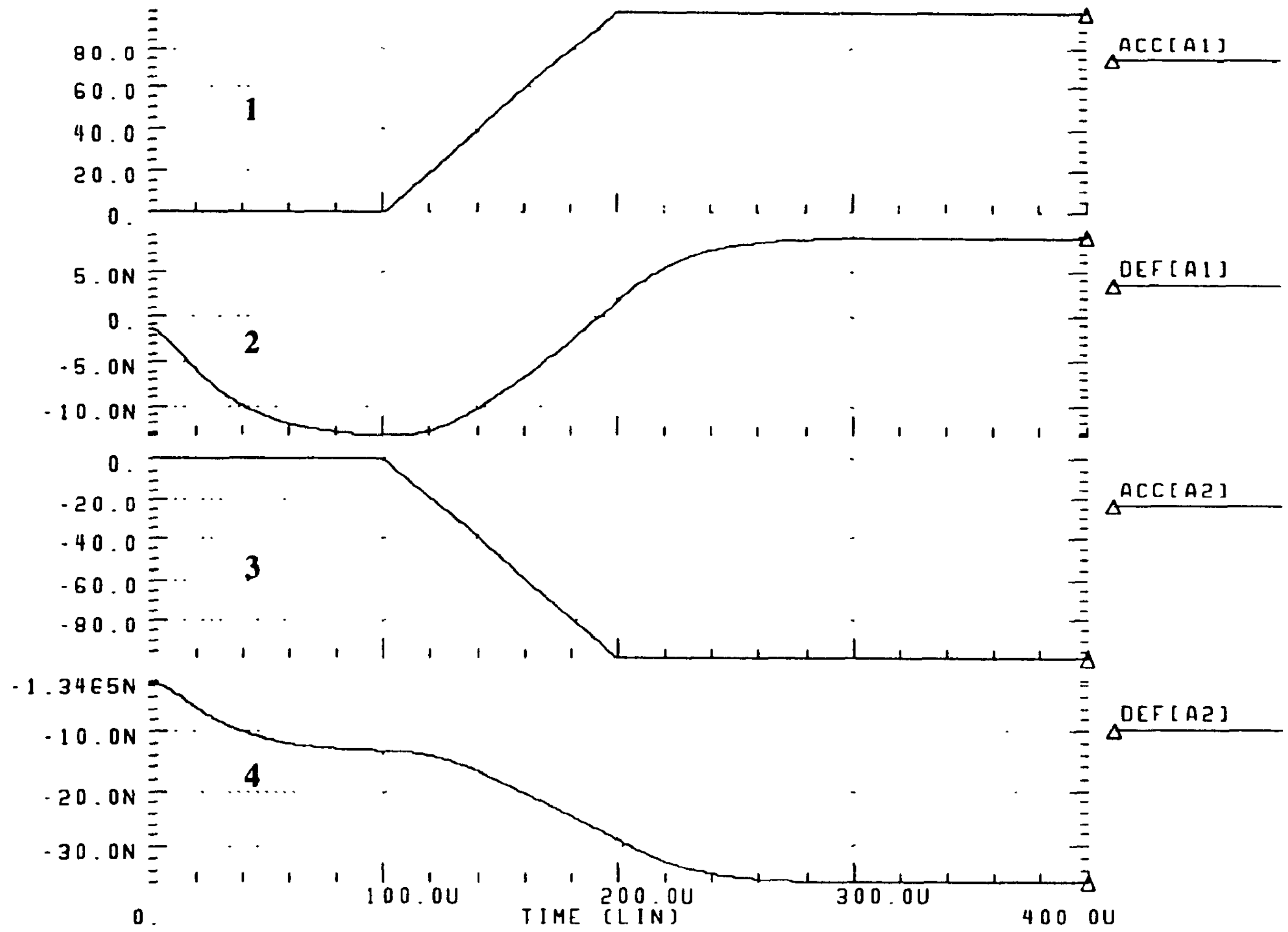

Figure (6.11): *Deflection (m) vs. Time (s) as a response to different values of applied Acceleration for the lumped electromechanical system before balancing.*

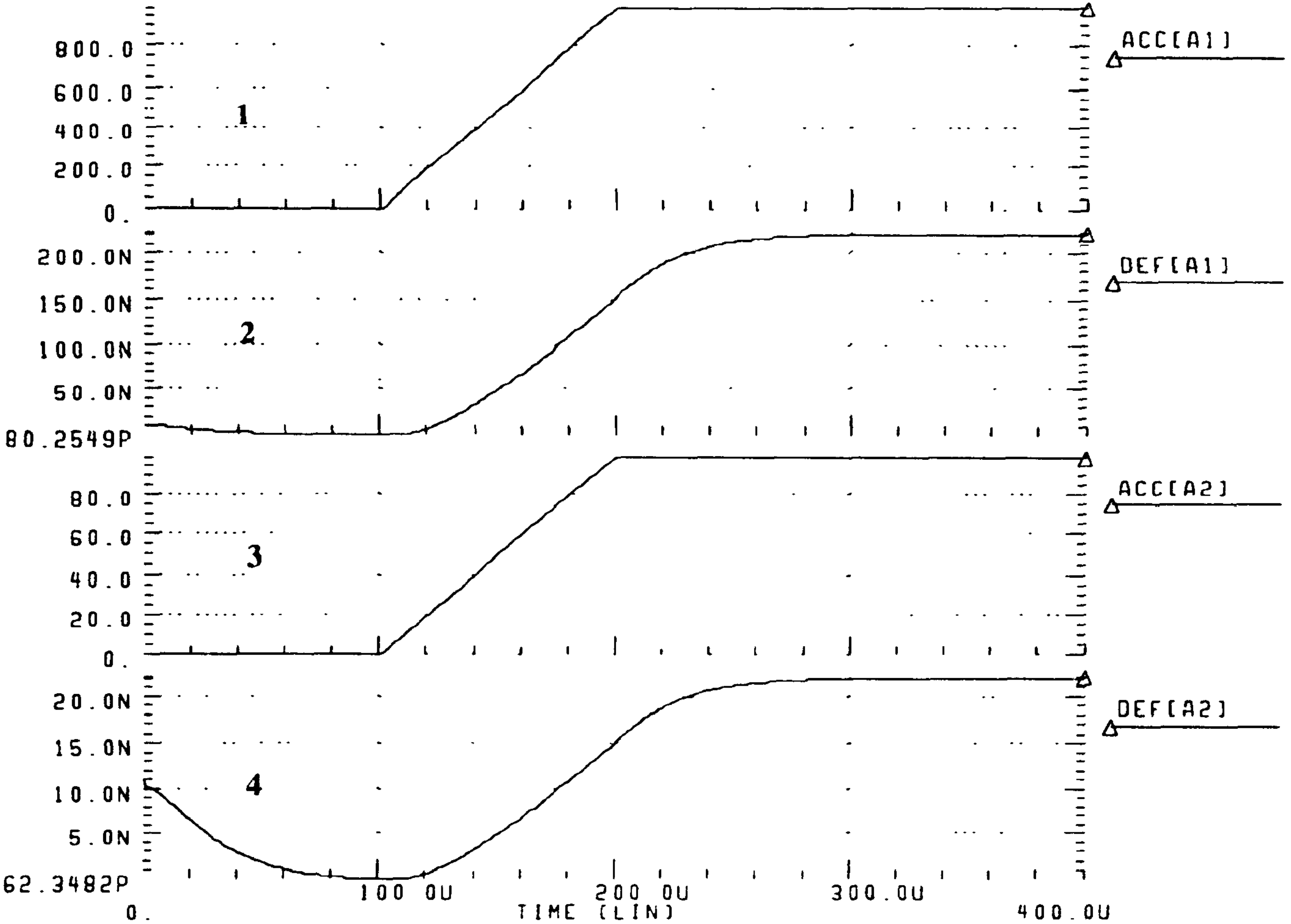

Figure (6.12): *Deflection (m) vs. Time (s) as a response to different values of applied Acceleration for the lumped electromechanical system after balancing.*

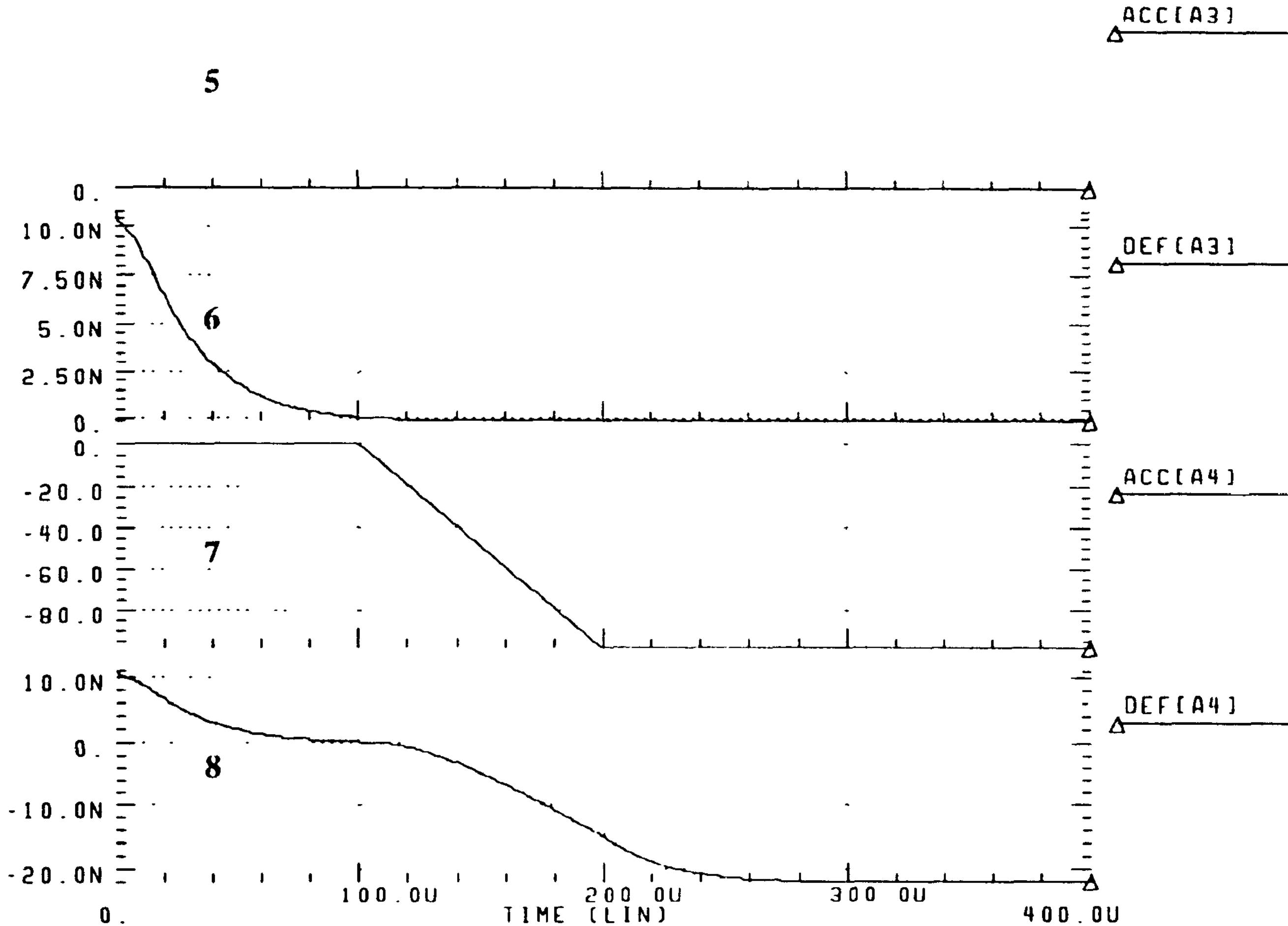

Figure (6.12): *(Continued)*

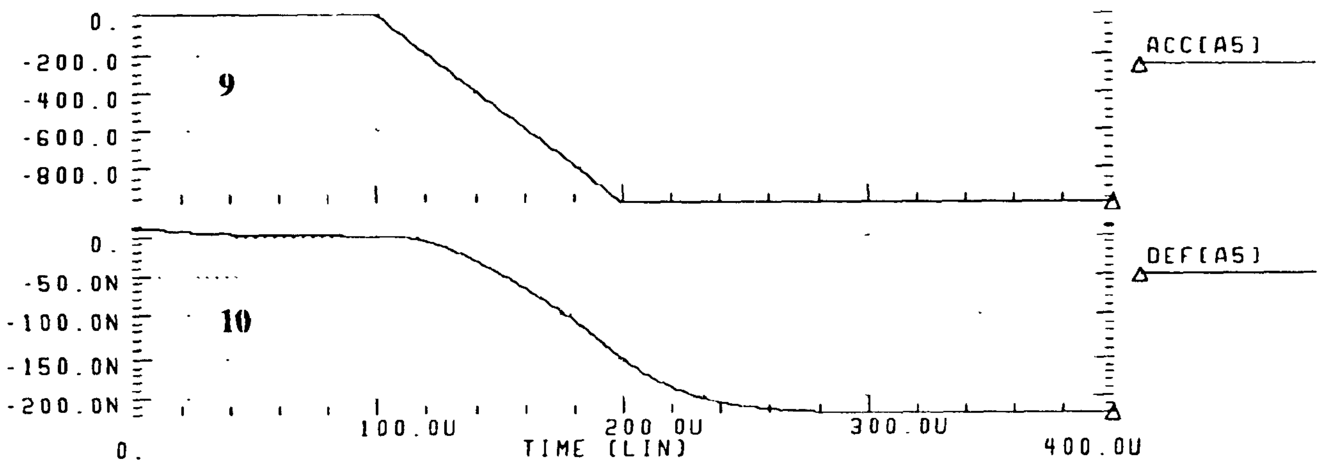

Figure (6.12): *(Continued)*

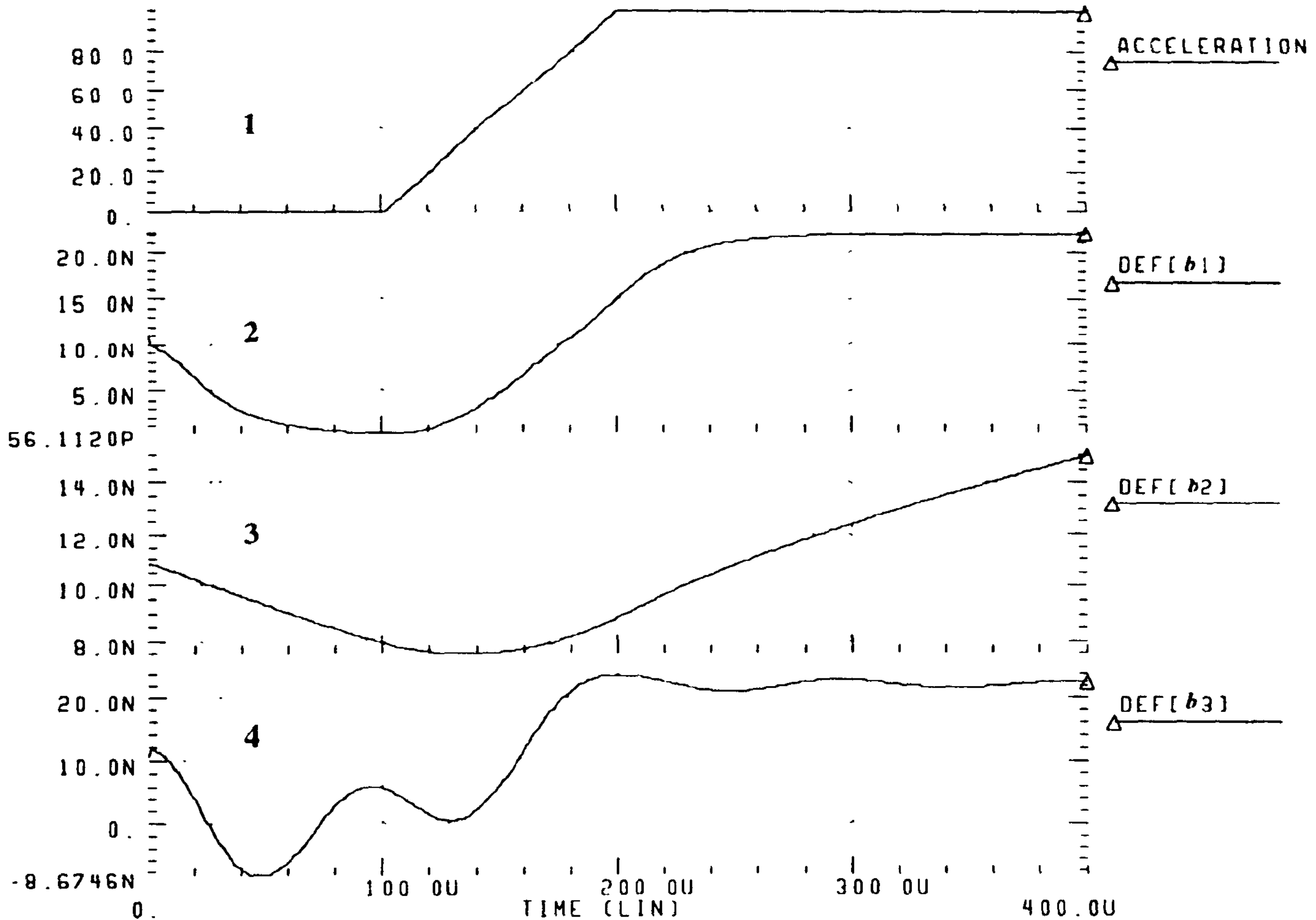

Figure (6.13): *Deflection (m) vs. Time (s) as a response to Acceleration for different Damping Coefficients for the lumped electromechanical system after balancing.*

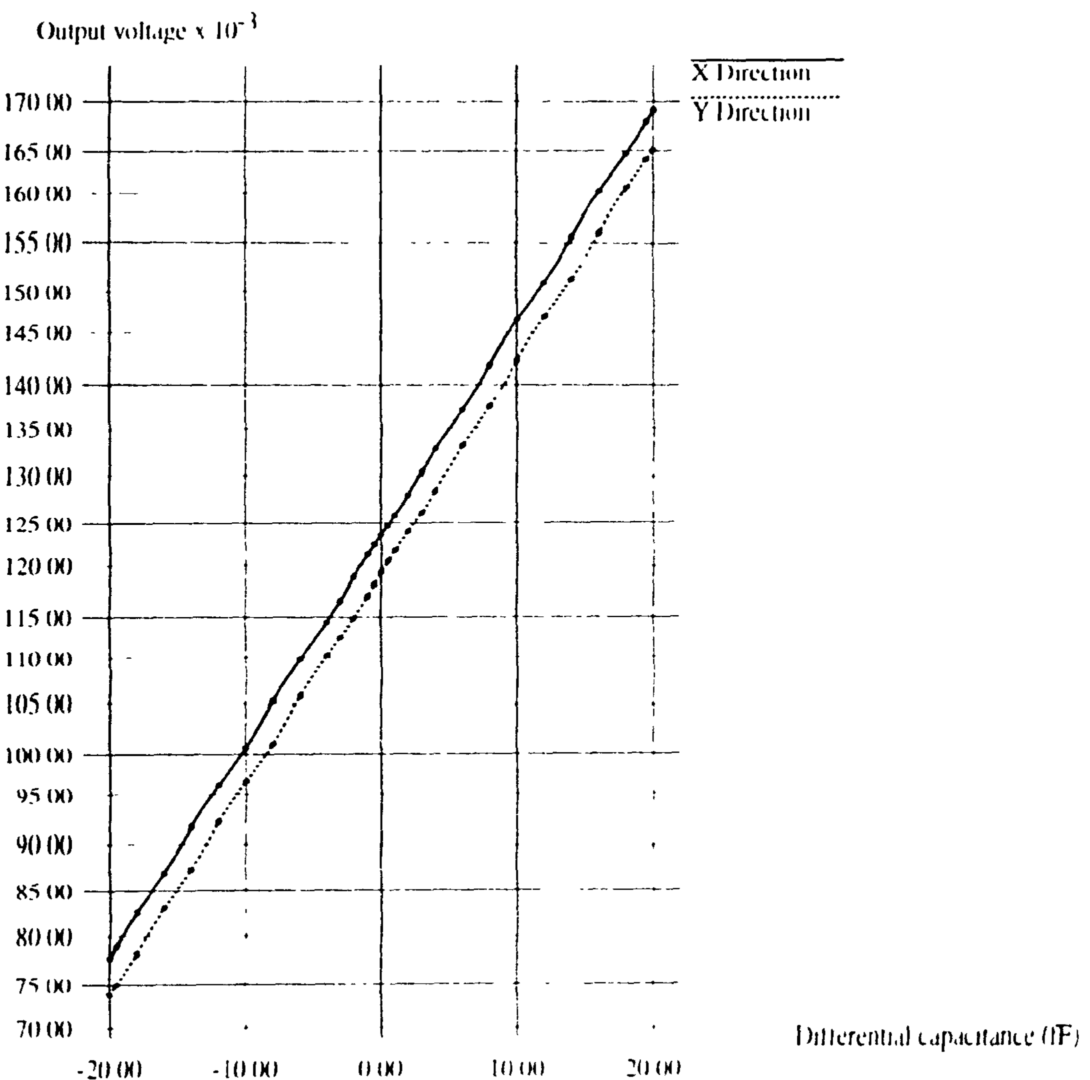

Figure (6.14): *Output Voltage vs. Differential Cap. for the 2-D circuit with*

$V_{ref+}=3$ V, $V_{ref-}=-2.5$ V.

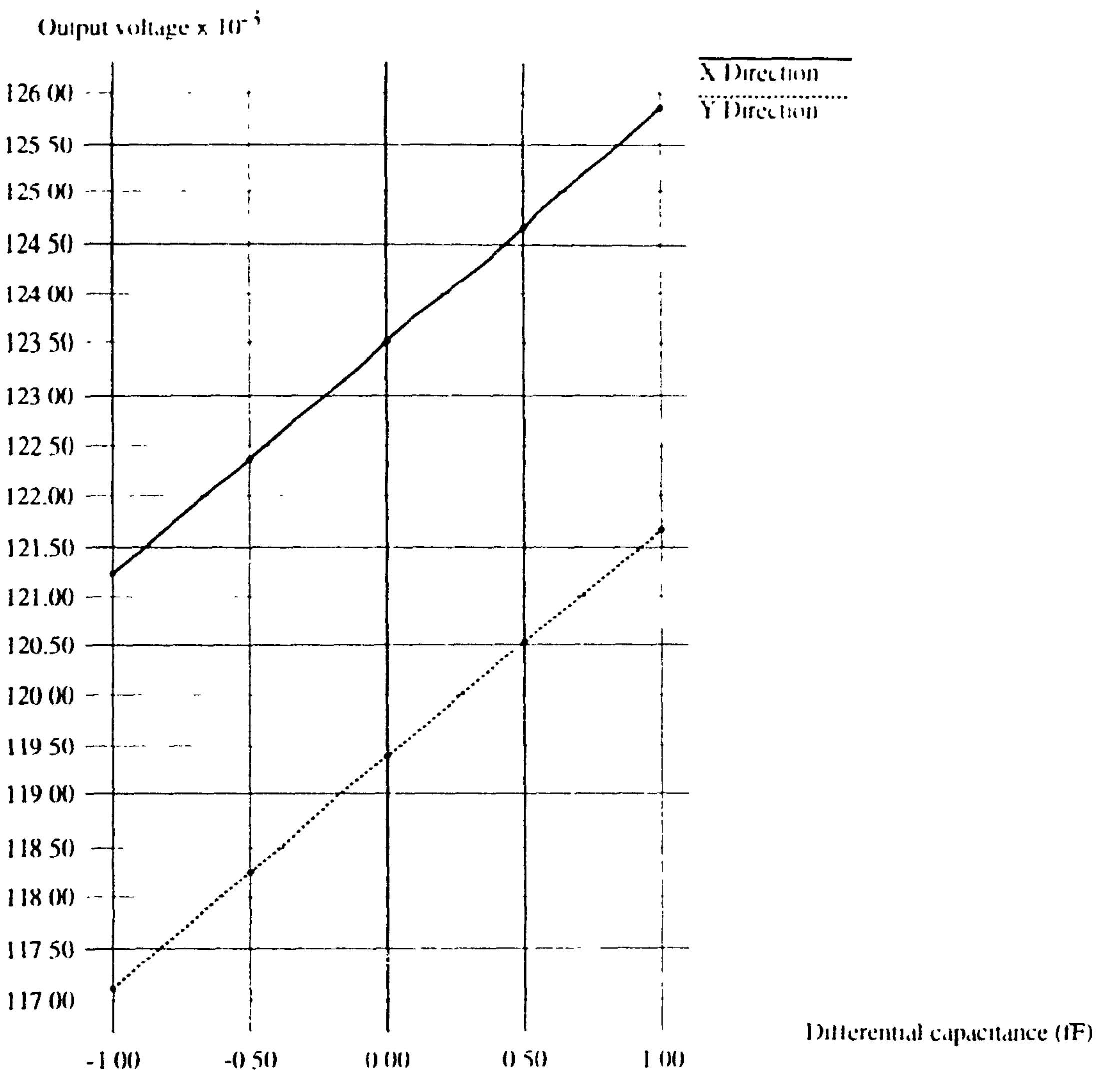

Figure (6.15): *Output Voltage vs. Differential Cap. Blown up around the Zero Differential Cap. for the 2-D Circuit* $V_{ref+}=3$ *V,* $V_{ref-}=-2.5$ *V.*

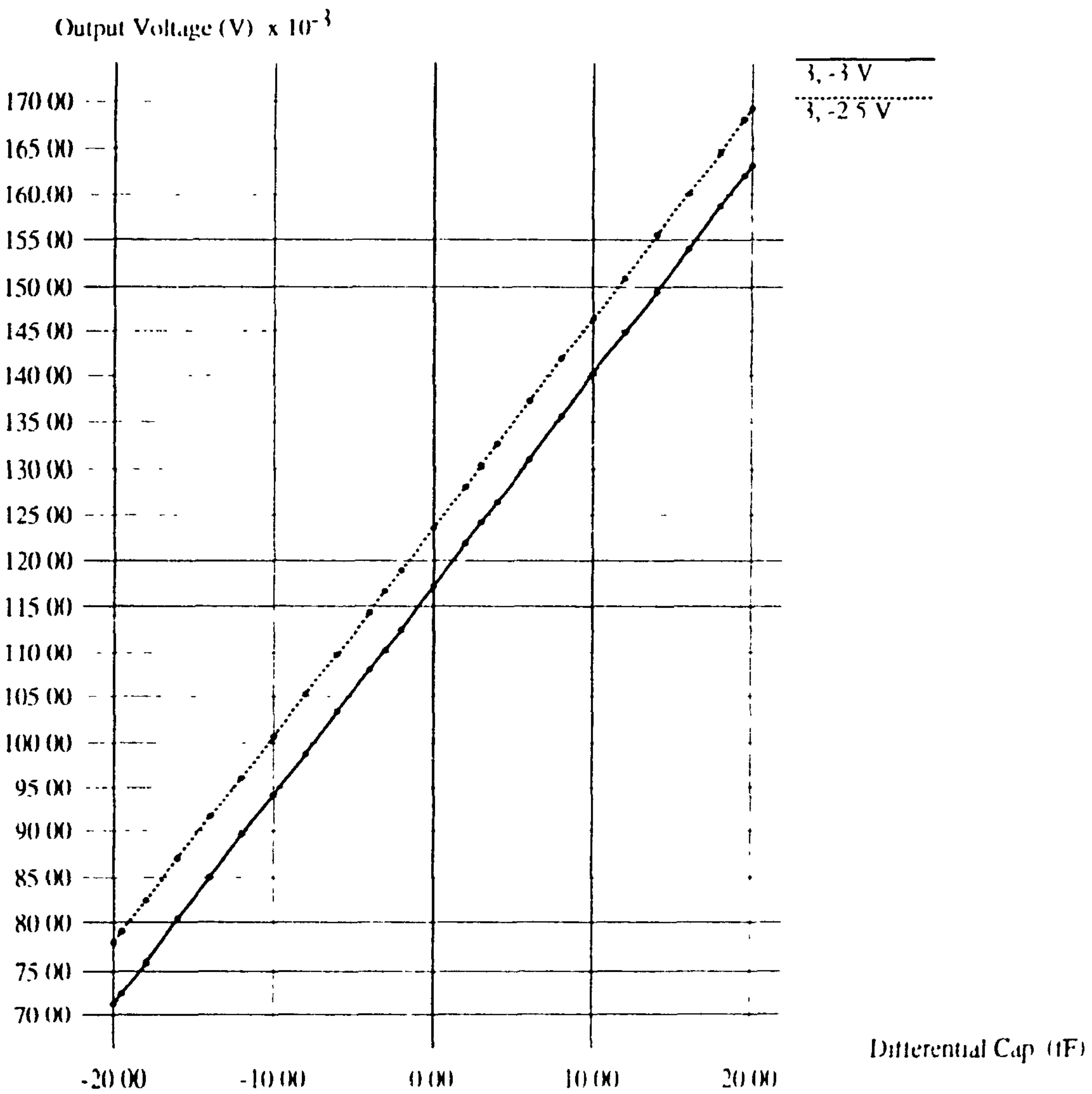

Figure (6.16): *Output Voltage vs. Differential Cap. for the 2-D circuit, a comparison between* $V_{ref+}=3$ *V,* $V_{ref-}=-3$ *V and* $V_{ref+}=3$ *V,* $V_{ref-}=-2.5$ *V arrangements.*

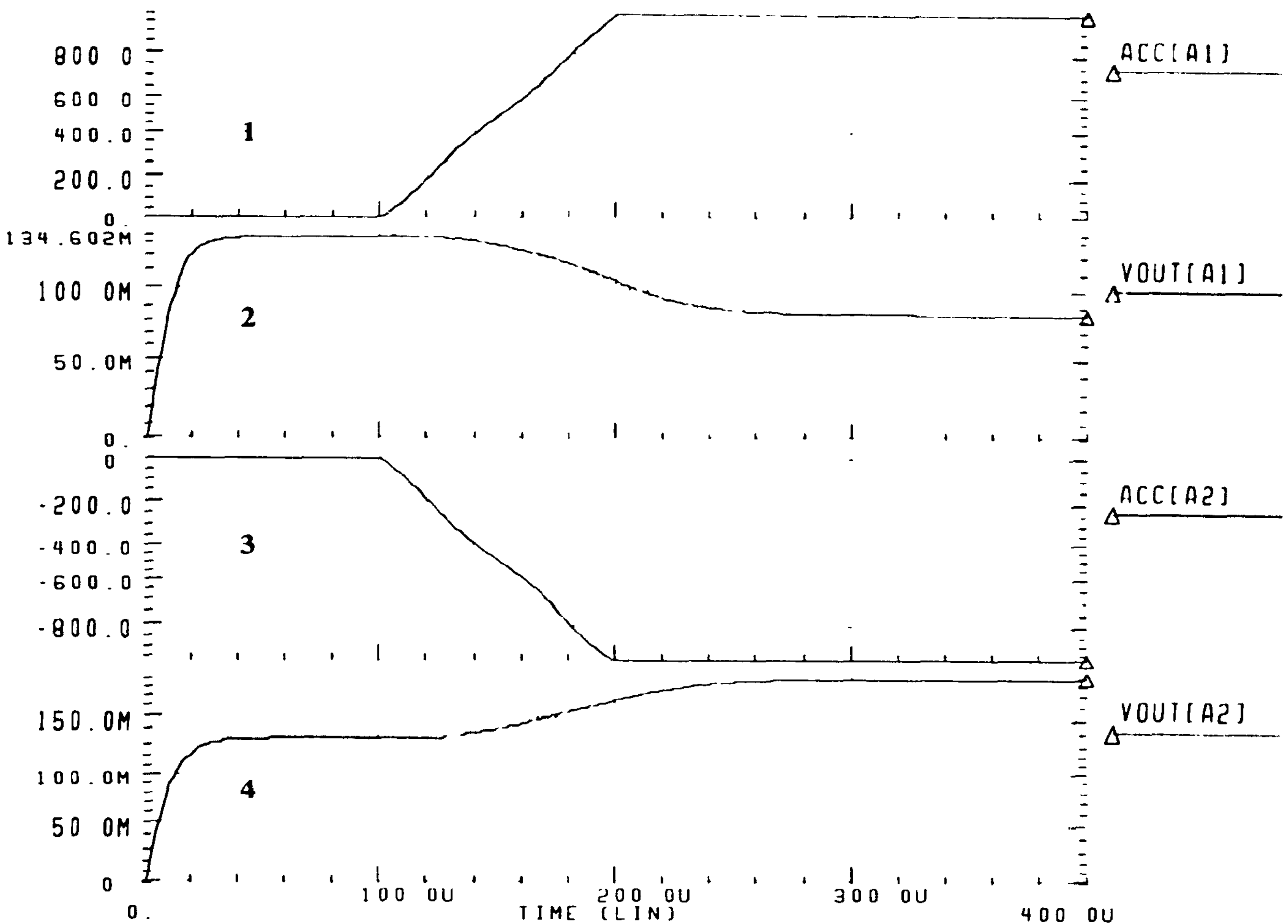

Figure (6.17): *Output Voltage (V) vs. Time (s) for different values of input Accelerations for the lumped electromechanical system after balancing.*

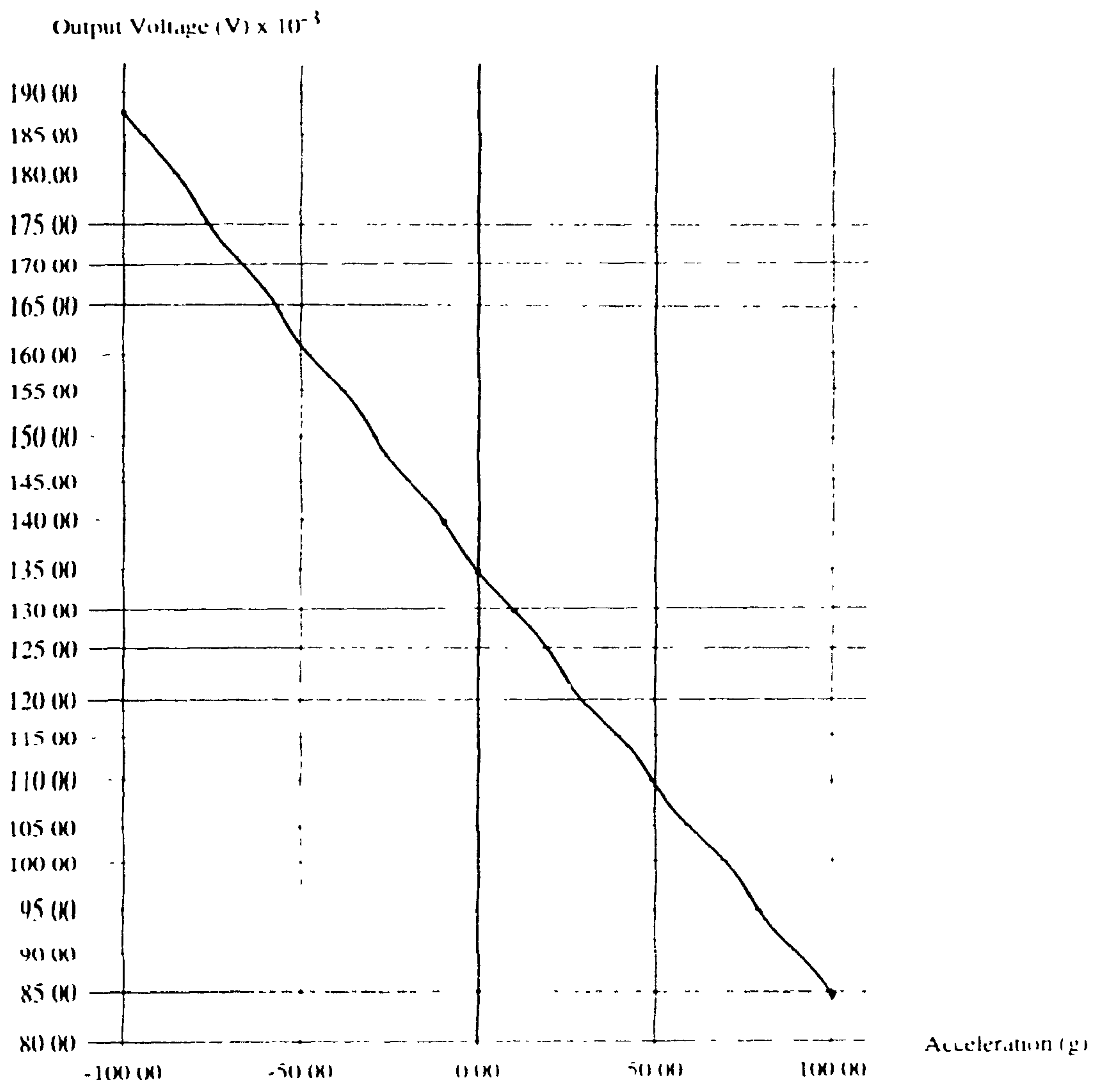

Figure (6.18): *Output Voltage vs. Acceleration for the balanced sensor*

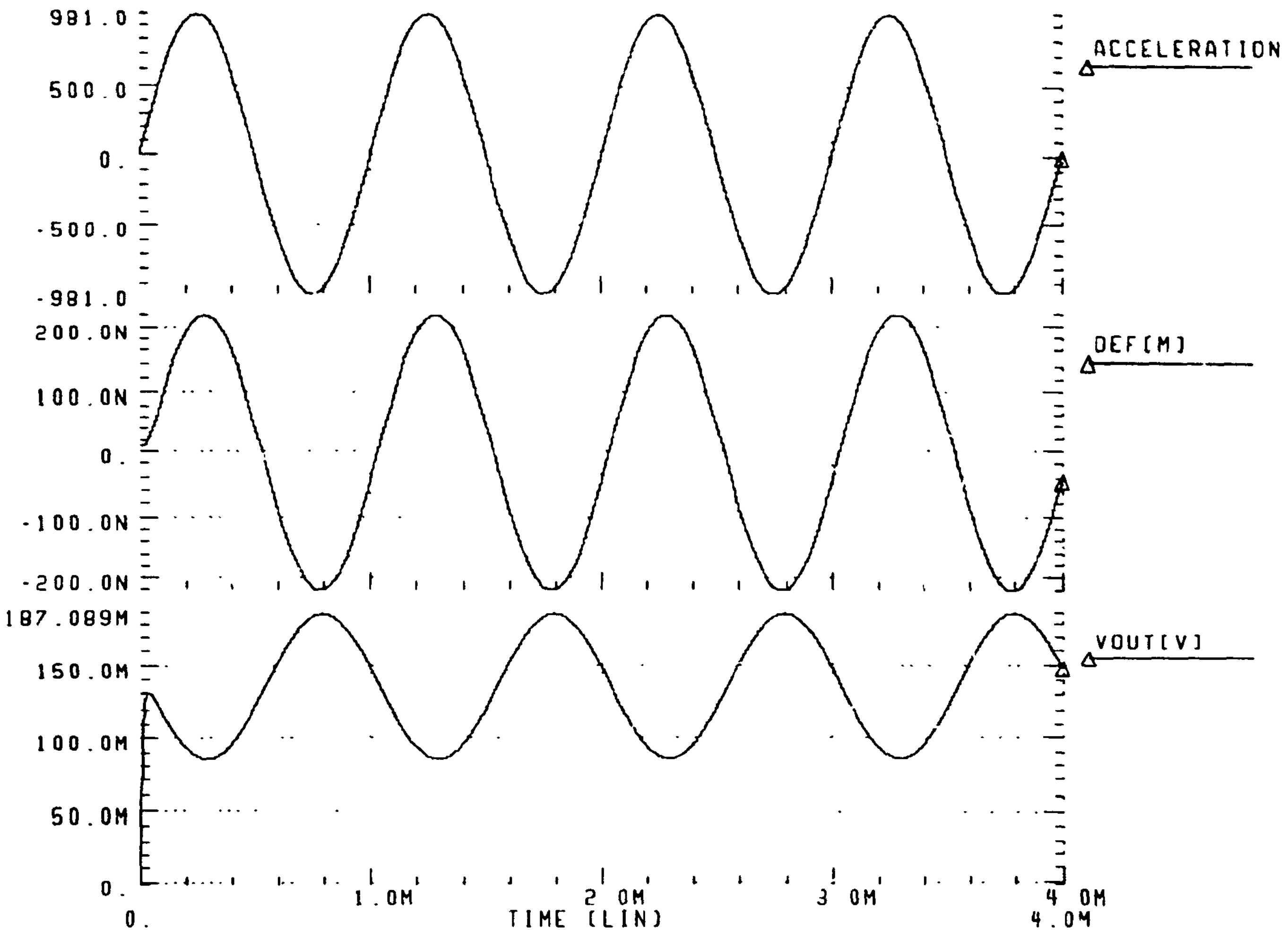

Figure (6.19): *Deflection (m) and Output Voltage(V) vs. Time (s) in response to a 1KHz sinusoidal Acceleration.*

6.4-Implementation

Since this project started, two runs were offered by Mitel Corporation through the Canadian Microelectronic Corporation (CMC). The first run was Mitel's first experience in Micromachining. The objective was testing the structure mechanically. This mechanical test was aimed at evaluating some process parameters such as the repeatability of the structures, the tolerances in the dimensions especially the fine ones like the clearances between the teeth. The mechanical structure was implemented using the first polysilicon layer. The design was part of the die named "CALES".

In order to make the structure accessible to post-fabrication etching, a contact cut and via openings were created on top of the polysilicon structure. Also a square opening in the passivation layer was created which included all the moving structure while leaving the roots of the fixed teeth to be covered by the passivation layers. This proved later to be a costly mistake.

By the end of July 1994, the dice were received from CMC. Using optical microscope, it could be seen that the totally exposed polysilicon was eaten away completely by the etching processes. However, the polysilicon that was covered by the passivation layers survived. Trying to analyze what went wrong, the process engineers from Mitel were contacted to discuss the matter. Their answer was that opening a via with no metal I underneath it was unprecedented in their process since a via is opened to create a connection between Metal I and Metal II. Opening the passivation layer with no Metal II underneath it also was not part of their standard process since the passivation layer is usually opened to expose a Metal II pad. Consequently, the etching processes that were supposed to consume the dioxide/nitride (in the via opening and the passivation opening) were not suited to avoid etching the polysilicon. Nevertheless, the implementation was not a total waste since we could monitor the repeatability in the creation of the teeth and the uniformity of the spacing between them which proved to be fairly good (in the areas covered by the passivation layers, at least).

Figure (6.20) shows the result of the first implementation. Note that we can see the shape of the polysilicon structure as a negative impression carved on the substrate underneath it in the totally open areas. This impression does not seem to be present in the areas covered

by the passivation layers. This leads to the fact that by the time of opening the passivation layers, the polysilicon structure was not totally gone nor had the silicon substrate underneath been carved.

The deadline for the second implementation was September 22 1994. In this implementation, the mistake committed in the first run was avoided. This time, no contact cut on top of the structure was created. The thick dielectrics deposited on top of the polysilicon before opening the via would work to protect the polysilicon throughout the etching steps that followed.

It is vital to have more flexibility in testing the functionality of both the mechanical structure and the electronic circuit. In order to facilitate this, the following options were furnished:

a-Two separate electronic circuits are included in the design. One for X direction and the other for Y direction. They have separate supplies and can be controlled by different clocks.

b-An on chip oscillator is included to create the clock that feeds the X direction circuit. Other inputs are supplied for an external clock to feed the Y direction circuit.

c-Two pairs of fixed capacitors are implemented on the chip so that they would help in testing the circuit functionality, in case the mechanical structure did not work. The selection is also multiplexer-controlled.

Up to this date, April, 1st., 1995 the chips for the second implementation are not delivered. Consequently, no comments can be made concerning the degree of progress that is made in this implementation.

Figure (6.21) shows the top view of the mask design that was sent to CMC for the second implementation as a part of the chip "CADP1". Note that the mechanical element and the 2-D detection circuitry occupy less than half a 3x3 mm die. Appendix [L] shows the pad assignment for this design within the chip "CADP1".

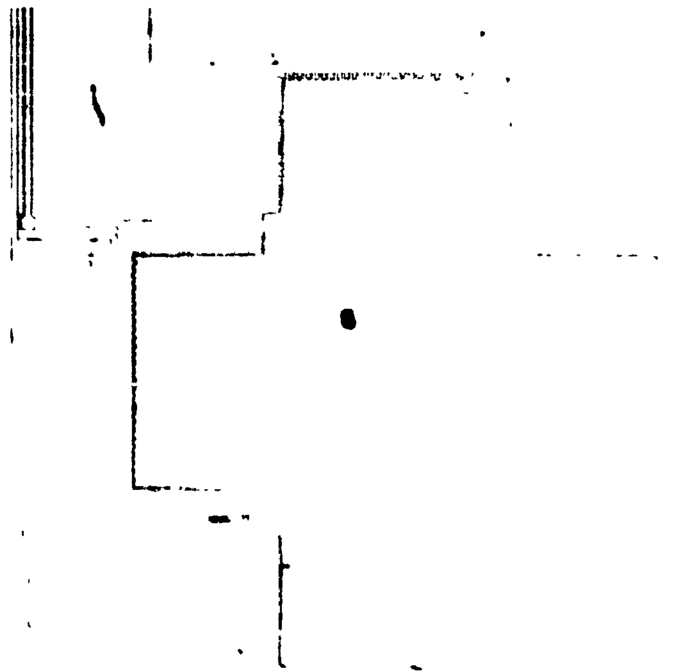

Figure (6.20): *Top view of the result of the first implementation.*

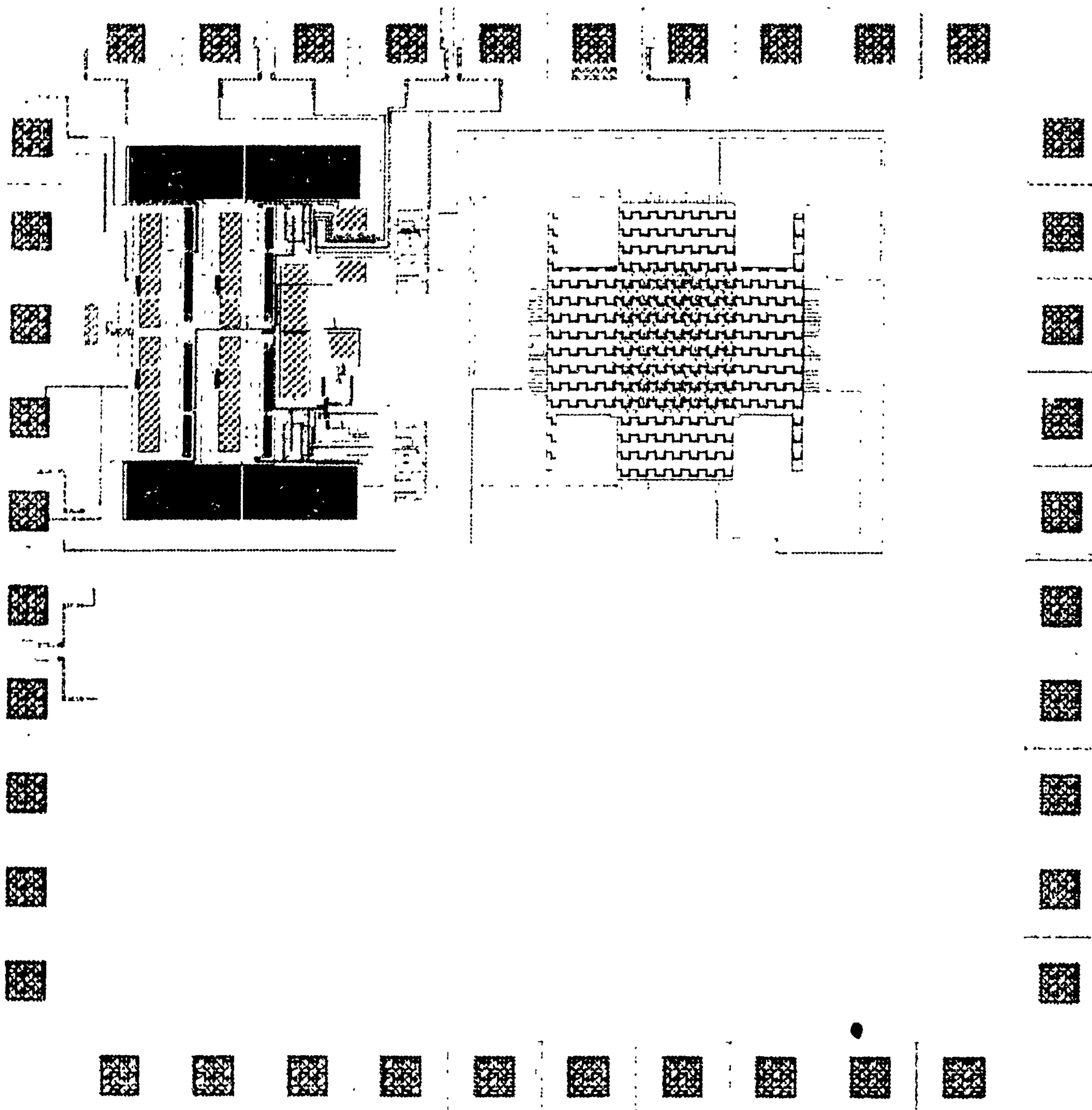

Figure (6.21): *Top view of the mask design sent to CMC for second implementation.*

6.5-Conclusions and Contribution of this Thesis

1-A 2-D accelerometer with on-chip circuitry is designed and implemented in a modified standard CMOS 1.5 micron process. This chip has not yet been received from CMC. We do not expect this implementation to work because the suggested modifications to the process were not adopted in this run. However, the two systems on board are furnished with enough I/O, multiplexers and test circuitry to test the sensor and the signal processing circuitry separately.

2-A new process flow based on modifying Mitel 1.5 micron CMOS process is developed and presented. Four additional masking steps are added to the commercially available Mitel 1.5 μm process to implement this sensor. One of these masks can be fabricated in the microelectronics laboratory at Concordia. With 2 micron polysilicon layer being one of the added masks, the mechanical structure of such an accelerometer can handle strong shocks as high as 2000 g without failure.

3-The 2-D signal conditioning circuit has been designed and thoroughly simulated. The concept of sharing one centre plate for both directions using multi-phase switching technique has been suggested and used. This technique has achieved considerable saving in area. Reasonably high sensitivities can be obtained from the sensor depending on the ADC to be used with the sensor. With an 8-Bit ADC, a resolution of 0.8 g is expected throughout the ±100 g range. Higher resolution can be achieved using an ADC with higher number of bits.

4-In order to simulate the integrated sensor as a unit, simulation modules based on HSPICE have been developed/used for the mechanical structure and the overall system. With this method, the interactions between the mechanical and electrical sub-systems are covered.

6.6-Suggestions and Future Work

Certain steps are considered to be useful complements to the design of this accelerometer in order to boost its performance. They can be listed as follows:

1-The transient behavior of the AC component of the output signal has a distinct peak that may be utilized for the capacitance measurement as was explained earlier in Section (6.1.1). A signal processing circuitry based on a fast and accurate peak detector can increase the sensitivity of the device by 30%.

2-An ADC may be implemented on chip to reduce the error in the output signal. The addition of the on-chip ADC will also push the sensor one more step ahead towards being a commercial sensor.

3-Special annealing should be applied to the polysilicon to help create the free-standing structure. The property of sublimation can be used to prevent the free structure from getting stuck by the surface tension forces.

4-A self test option should also be added to the sensor as was described earlier in Section (3.2).

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Appendix A

Relationship between Acceleration and the Differential Capacitance:

In a differential capacitance system, examine the arrangement shown in Figure(A1). The values of capacitances C_1 and C_2 are given by:

$$C_1 = \frac{\varepsilon \cdot A}{d_0 - \delta} \qquad C_2 = \frac{\varepsilon \cdot A}{d_0 + \delta} \tag{A1}$$

where $\varepsilon=\varepsilon_0.\varepsilon_r$ is the permittivity of the medium. A is the surface area of plates, d_0 is the zero-acceleration plate separation and δ is the deflection. The differential capacitance, ΔC will be given by:

$$\Delta C = C_1 - C_2 = \varepsilon \cdot A \cdot \frac{2 \cdot \delta}{d_0^2 - \delta^2} \tag{A2}$$

If $\delta^2 \leq 0.01 d_0^2$ i.e. $|\delta| \leq 0.1 d_0$, then Equation (A2) can be linearized while still keeping the linearization error within 1% and therefore ΔC becomes:

$$\Delta C = C_1 - C_2 = \frac{2 \cdot \varepsilon \cdot A}{d_0^2}\delta = K_c \cdot \delta \tag{A3}$$

And ΔC is a linear function of the deflection. Now according to Equation (1.3), the deflection itself is a linear function of acceleration. Substituting for the deflection into Equation (A3) gives:

$$C_1 - C_2 = \frac{K_c \cdot m}{k_s} \cdot a \tag{A4}$$

This special arrangement is of special importance since it gives the differential change in capacitance as a linear function of the applied acceleration.

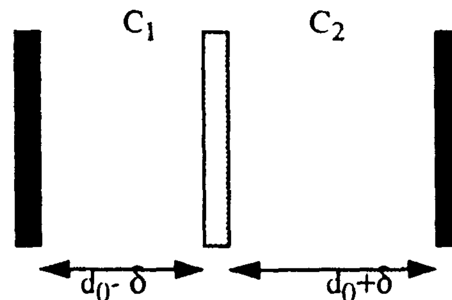


Figure (A1): *The Differential Capacitor plate arrangement.*

Appendix B

The Ratio of Maximum/Average Deflection in a Uniformly Loaded Cantilever Beam:

The equation of the deflection of a cantilever beam subjected to uniform loading as shown in Figure (2.4), is given by:

$$\delta = \frac{\omega}{E \cdot I}\left[\frac{l^3 \cdot x}{6} - \frac{l^4}{8} - \frac{x^4}{24}\right] \qquad (B1)$$

where δ is the deflection, ω is the load per unit length, E is the modulus of elasticity, I is the moment of inertia, x is the distance along the cantilever and l is the total length of the cantilever. At the tip of the cantilever, this equation will be reduced to Equation (2.23). On the other hand, the average deflection will be given by:

$$\delta_{avg} = \frac{\int_0^l \frac{\omega}{E \cdot I}\left[\frac{l^3 \cdot x}{6} - \frac{l^4}{8} - \frac{x^4}{24}\right] dx}{\int_0^l dx} \qquad (B2)$$

$$|\delta_{avg}| = \frac{\omega \cdot l^4}{20 \cdot E \cdot I} \Rightarrow \frac{\delta_{max}}{\delta_{avg}} = 2.5 \qquad (B3)$$

Appendix C

Theory of Buckling:

Buckling is the deformation that takes place in an element due to axial stresses applied to that element. These stresses can be both intrinsic or extrinsic.

Choose the positive direction of the **X** axis as the right and positive direction of **Y** as downwards as explained in Figure (C1). Applying the general formula for bending: to that structure gives:

$$E \cdot I \cdot \frac{d^2y}{dx^2} = -F_a \cdot y \qquad (C1)$$

where E is the modulus of elasticity, I is the moment of inertia, F_a is the applied axial force and y is the deflection in Y direction.

The negative sign comes from the fact that the slope changes from a positive value at $x=0$ to a negative value at $x=l$ which gives the second derivative a negative value. By expanding the equation and multiplying both sides with $2dy$ gives:

$$E \cdot I \cdot \left(2\frac{dy}{dx} \cdot d \cdot \frac{dy}{dx}\right) = -2F_a \cdot y \cdot dy \qquad (C2)$$

Then integration result in:

$$E \cdot I \cdot \left(\frac{dy}{dx}\right)^2 = -F_a \cdot y^2 + C_1 \qquad (C3)$$

Now at $y=\Delta$, the first derivative (the slope) is equal to zero which leads to $C_1=F_a.\Delta^2$ and the equation will be modified into

$$\frac{dy}{dx} = \sqrt{\frac{F_a}{E \cdot I}} \cdot \sqrt{\Delta^2-y^2} \qquad (C4)$$

Separating the variables gives:

$$\frac{dy}{\sqrt{\Delta^2 - y^2}} = \sqrt{\frac{F_a}{E \cdot I}} \cdot dx \qquad (C5)$$

Integrating with respect to x again gives:

$$\operatorname{asin}\left(\frac{y}{\Delta}\right) = \sqrt{\frac{F_a}{E \cdot I}} \cdot x + C_c \qquad (C6)$$

But at $x=0$, the value of $y=0$ which leads to the value $C_2=0$ and the equation becomes:

$$\frac{y}{\Delta} = \sin\left(\sqrt{\frac{F_a}{E \cdot I}} \cdot x\right) \qquad (C7)$$

The equation above defines the elastic curve of the column as a continuous sine wave whose amplitude equals the maximum deflection Δ. The importance of the equation lies not, however in defining the deflection curve but in permitting the determination of the critical load.

In determining this load, it is first necessary to note that the projected length of the deflected column is not exactly equal to its real length l. In fact, not until the load is reduced to a value that will just make the column straight will the projected length equal the actual length. The value of the load sustained by the column as it becomes straight is the *Euler Critical Load.*

To obtain the Euler Critical Load, the column curvature is reduced to the point where Δ is infinitesimally small and the column is just about straight. Under this condition, the LHS of the equation still remains zero, and the value of x is for all intents and purposes is equal to l and the equation would result in:

$$\frac{y}{\Delta} = 0|_{x=l} \Rightarrow \sqrt{\frac{F_a}{E \cdot I}} \cdot l = \pi \qquad (C8)$$

The angle whose sine is equal to zero must equal to π or some multiple of π, depending upon the number of half-sine that are included in the column length. It follows that the minimum or critical value of F_a for a column whose length equals one half a sine wave (i.e for a column with a bend on one side of the axis and hinged at each end) is found by:

$$F_{critical} = \frac{\pi^2 \cdot E \cdot I}{l^2} \qquad (C9)$$

The general formula for the buckling of a slender column would be:

$$F_{critical} = \frac{(n \cdot \pi)^2 \cdot E \cdot I}{l^2} \qquad (C10)$$

An important question would be "Why does the buckling take place anyway and since the force is axial then where did the bending moment come from?"

The question seems to be a very reasonable one since a pure axial force applied on a perfectly uniform column should cause no bending and rather only compression should take place. The answer to that question is that the bending is caused by two real-life imperfections:

1-In real life, there is no really 100% axial load and a shear component exists no matter how small it was.

2-There always be some degree of non uniformity in the section of the column where the centre of mass will move away from the original central axis and bending moment is generated.

It is very important to notice here that buckling does not occur under tensile forces and it is restricted to compressive forces.

Another very important conclusion can be drawn from the equations is that the longer the column, the lower the critical force needed to buckle it since it is inversely proportional to the second power of the length.

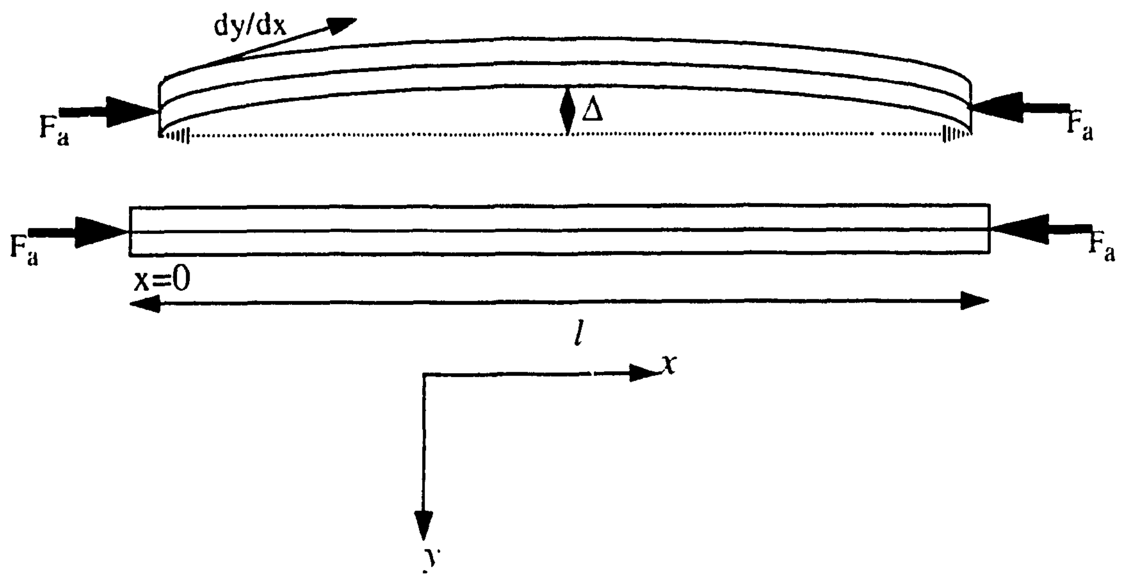


Figure (C1): *Buckling of a column subjected to axial load [42].*

Appendix D

HSPICE File for the 2-Dimensional Circuit:

```
*$$$$$$$$$$$$$$$$$$$$$$$$ X Direction Circuit$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

****************************Clocks************************************
va 1 0 pulse (0.000000000e+00 3.3000000000e+00 0.000000000e+00
+ 1.000000000e-08 1.000000000e-08 2.300000000e-07 1.000000000e-06)
vb 2 0 pulse (0.000000000e+00 3.3000000000e+00 2.500000000e-07
+ 1.000000000e-08 1.000000000e-08 2.300000000e 07 1.000000000e-06)
*************************Voltage Sources*****************************
vv41 10 0 -3.3
vv40 21 0 -3.3
vv39 17 0 -3.3
vv38 19 0 -3.3
vv37 13 0 -3.3
vv36 15 0 -3.3
vv33 20 0 3.3
vv32 14 0 3.3
vv31 12 0 3.3
vv30 18 0 3.3
vv29 16 0 3.3
vv28 9 0 3.3
****************************vr and -vr******************************
vv27 11 0 -3.0
vv26 8 0 3.0
***********************Transmission Gates**************************
mq25 8 2 5 9 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u ps=
+ 17.52u nrd=1 nrs=1
.model m1mmpmos pmos vto=-560m ld=153n tox=27n pb=800m nsub=3.6e+16
+ nfs=225g theta=35.9m level=3 vmax=217k mj=500m gamma=864m rsh=65 kp=
+ 17.7u is=10f cgso=251p af=1 eta=147m delta=1.53 fc=500m xj=409n
+ kappa=5.69 cgbo=256p cj=618u uo=138 phi=765m cgdo=251p
```

```
mq24 5 1 8 10 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
.model m2mmnmos nmos vto=828m ld=240n tox=27n pb=800m nsub=1.6e+16
+ nfs=868g theta=34.7m level=3 vmax=1.6meg mj=500m gamma=586m rsh=
+ 62.5 kp=68u is=10f cgso=269p af=1 eta=141m delta=1.06 fc=500m xj=
+ 297n kappa=10m cgbo=256p cj=419u uo=532 phi=725m cgdo=269p
mq22 24 1 3 18 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq21 3 2 24 19 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq19 11 2 4 12 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq18 4 1 11 13 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq16 3 2 0 16 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq15 0 1 3 17 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq13 5 1 0 20 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq12 0 2 5 21 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq10 4 1 0 14 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq9 0 2 4 15 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=1
+ nrs=1

*************************Sensor Capacitors***************************
cc5 3 4 100f tc=0 $ Cx1
cc3 5 3 100f tc=0 $ Cx2
****************************paracitics*********************************
ccp2 4 0 70ff   $Cp2
ccp1 5 0 70ff   $Cp1
```

```
ccp3 3 0 50ff    $ Cp3
****************************filters**********************************
RFL1 6 7 1e6 tc=0 0    $ Rf1x
CFL1 7 0 5p tc=0       $ Cf1x
RFL2 106 109 1e6 tc=0 0 $ Rf2x
CFL2 0 109 5p tc=0     $ Cf2x
*************************Integrator Circuit**************************
rr42 24 6 1e6 tc=0 0   $ Rfx
cc6 6 24 50f tc=0      $ Cintx
cc4 24 0 10p tc=0      $ Cinpx
xopamp1 0 24 6 opamp
****************************Buffer Circuit***************************
xopamp2 7 106 106 opamp
*********************************************************************

*$$$$$$$$$$$$$$$$$$$$$$$$$$ Y Direction Circuit$$$$$$$$$$$$$$$$$$$$$$$$$$

*******************************Clocks********************************
vd 2002 0 pulse (0.0000000000e+00 3.3000000000e+00 7.5000000000e-07
+ 1.0000000000e-08 1.0000000000e-08 2.3000000000e-07 1.0000000000e-06)
vc 2001 0 pulse (0.0000000000e+00 3.3000000000e+00 5.0000000000e-07
+ 1.0000000000e-08 1.0000000000e-08 2.3000000000e-07 1.0000000000e-06)
****************************Voltage Sources**************************
vvc41 2010 0 -3.3
vvc40 2021 0 -3.3
vvc39 2017 0 -3.3
vvc38 2019 0 -3.3
vvc37 2013 0 -3.3
vvc36 2015 0 -3.3
vvc33 2020 0 3.3
vvc32 20[illegible]4 0 3.3
vvc31 2012 0 3.3
vvc30 2018 0 3.3
```

```
vvc29 2016 0 3.3
vvc28 2009 0 3.3
******************************vr and -vr********************************
vvc27 2011 0 -3.0
vvc26 2008 0 3.0
*************************Transmission Gates***************************
mqc25 2008 2002 2005 2009 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mqc24 2005 2001 2008 2010 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mqc21 3 2002 2024 2019 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mqc19 2011 2002 2004 2012 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mqc18 2004 2001 2011 2013 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=1 nrs=1
mqc16 3 2002 0 2016 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mqc15 0 2001 3 2017 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mqc13 2005 2001 0 2020 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mqc12 0 2002 2005 2021 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mqc10 2004 2001 0 2014 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mqc9 0 2002 2004 2015 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=1
+ nrs=1
*************************Sensor Capacitors*****************************
ccc5 3 2004 100f tc=0   $ Cy1
```

```
ccc3 2005 3 100f tc=0   $ Cy2
*****************************paracitics**********************************
cccp1 2004 0 70ff       $ Cp5
cccp2 2005 0 70ff       $ Cp4
cccp3 3 0 50ff          $ Cp3
******************************filters*************************************
RFcL1 2006 2007 1e6 tc=0 0 $ R1y
CfcL1 2007 0 5p tc=0      $ Cf1y
RFcL2 2106 2109 1e6 tc=0 0 $ R2y
CfcL2 0 2109 5p tc=0      $ Cf2y
*************************Integrator*ircuit******************************
rrc42 2024 2006 1e6 tc=0 0 $ Rfy
ccc6 2006 2024 50f tc=0   $ Cinty
ccc4 2024 0 10p tc=0      $ Cinpy
xopamp3 0 2024 2006 opamp
***************************Buffer Circuit*******************************
xopamp4 2007 2106 2106 opamp

*$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

*******************************OPAMP*********************************
.subckt opamp 5 6 1

*This is the netlist file for a cmos opamp supplied to cmc by goal company
* and implemented on mitel process.
* net 0 = gnd!
* net 1 = vout
* net 2 =
* net 3 =
* net 4 =
* net 5 = vin+
* net 6 = vin-
* net 7 = vdd
```

```
* net 8 = vss
* net 9 =
* net 10=
* capacitor(0) = /+8

vdd 7 0 3
vss 8 0 -3.3
rc 9 1 9800
 c0 2 9 1.40251e-11
rin 7 10 140k
.model model2 pmos level=3 vto=-0.56 phi=0.765 gamma=0.864
+nsub=3.6e+16 bex=-1.5 kp=1.77e-05 nfs=1.6617e+09 uo=138
+vmax=217000 xj=4.09e-07 ld=1.53e-07 theta=0.0359 af=1
+cgbo=2.5e-13 cgdo=2.51e-10 cgso=2.51e-10 tox=2.7e-08
+wd=9.77e-08 capop=12 is=1e-14 cj=0.000618 mj=0.5 pb=0.8
+rsh=65.2 delta=1.53 kappa=5.69 eta=0.147
* pfet( 1 ) = /+7
m1 1 2 7 7 model2 w=0.0001604 l=4e-06 ad=8.9824e-10
+as=8.9824e-10 pd=0.000332 ps=0.000332
* pfet(2) = , '6
m2 2 4 7 7 model2 w=7.54e-05 l=6e-06 ad=4.3732e-10
+as=4.0716e-10 pd=0.0001624 ps=0.000 1616
* pfet(3) = /+5
m3 4 4 7 7 model2 w=7.54e-05 l=6e-06 ad=4.2224e-10
+as=4.2224e-10 pd=0.000162 ps=0.000162
.model model3 nmos level=3 vto=0.828 phi=0.725 gamma=0.586
+nsub=1.6e+16 bex=-1.5 kp=6.8e-05 nfs=8.68e+11 uo=532
+vmax=160000 xj=2.97e-07 ld=2.4e-07 theta=0.0345 af=1
+cgbo=2.56e-13 cgdo=2.69e-10 cgso=2.69e-10 tox=2.7e-08 wd=1e-10
+capop=12 is=1e-14 cj=0.000419 mj=0.5 pb=0.8 rsh=62.8 delta=1.06
+kappa=0.01 eta=0.141
* nfet(4) = /+4
m4 1 10 8 8 model3 w=7.54e-05 l=5e-06 ad=4.0716e-10
```

```
+as=4.3732e-10 pd=0.0001616 ps=0.0001624
* nfet(5) = /+3
m5 8 10 3 8 model3 w=3.04e-05 l=5e-06 ad=1.7632e-10
+as=1.6416e-10 pd=7.24e-05 ps=7.16e-05
* nfet(6) = /+2
m6 2 5 3 3 model3 w=0.0001504 l=2.4e-06 ad=8.4224e-10
+as=7.8208e-10 pd=0.000312 ps=0.0003112
* nfet(7) = /+1
m7 4 6 3 3 model3 w=0.0001504 l=2.4e-06 ad=8.1216e-10
+as=8.1216e-10 pd=0.0003116 ps=0.0003116
* nfet(8) = /+0
m8 8 10 10 8 model3 w=3.04e-05 l=5e-06 ad=2.128e-10
+as=1.7024e-10 pd=7.48e-05 ps=7.2e-05
.ends
*****************************************

.temp 27
.op
.tran 1e-07 5e-4 0
.options brief dcon=1
.END
```

Appendix E

Steps of the Standard Fabrication Process [39]:

Step	DESCRIPTION	CONDITION
1	Starting Material N-type bulk	2-4 Ωcm
2	Initial Oxidation (and nucleation)	3900±200 °A
3	P-well Mask and Implant	
4	P-well Diffusion	1975±200 °A
5	Sub Nitox	500±50 °A
6	Nitride Deposition	1825±125 °A
7	Active Area Mask and Etch	
8	P^- Field Mask and Implant	
9	N^- Field Implant Blanket	
10	Field Oxidation	9000±500 °A
11	Pre-gate Oxidation	1400±100 °A
12	Gate Oxidation	270±20 °A
13	V_t Blanket Implant	
14	V_{tp} Adjust and Punchthrough mask and Implant	
15	Polysilicon Gate Deposition	3225±300 °A 20.0Ω/sq
16	Poly Gate Mask and Etch	
17	N^- Mask and Implant	
18	Implant Oxide	200±20 °A
19	N^+ Mask and Implant	
20	P^+ Mask and Implant	
21	Poly Cap Deposition	2500±250 °A
22	Poly Cap Implantation	
23	Poly Cap Mask and Etch	

Step	DESCRIPTION	CONDITION
24	Dielectric Deposition SG/PSG/SOG	1300/5000/1800 °A
25	Flow	130±20 °A
26	RTP Activation	45±5 °A
27	Contact Mask and Etch	
28	Metallization I	8000±800 °A; 250 °A SiCr
29	Metal I Mask and Etch	
30	Inter-dielectric I	3000±300 °A
31	Spin-On-Glass	4200 °A
32	Inter-dielectric II	3000±300 °A
33	Vias Mask and Etch	
34	Metallization II	8000±800 °A
35	Metal II Mask and Etch	
36	Alloy	
37	Passivation oxide/nitride	7000/3000 °A
38	Pads Mask and Etch	

Appendix F

Triple-Point of a Material:

The triple point of a material is temperature and pressure at which the material will reach a state of equilibrium between the solid phase and the liquid phase in the absence of any other material [43]. That invariably implies that the gaseous phase is present too since any liquid would not stabilize until it reaches an equilibrium with its vapor. This means the presence of the three phases of matter simultaneously and for that reason, this point is called the "triple point"

The triple point for pure water is at 0.0076^{0}C and 4.6 torra* (612 Pascal) [40].

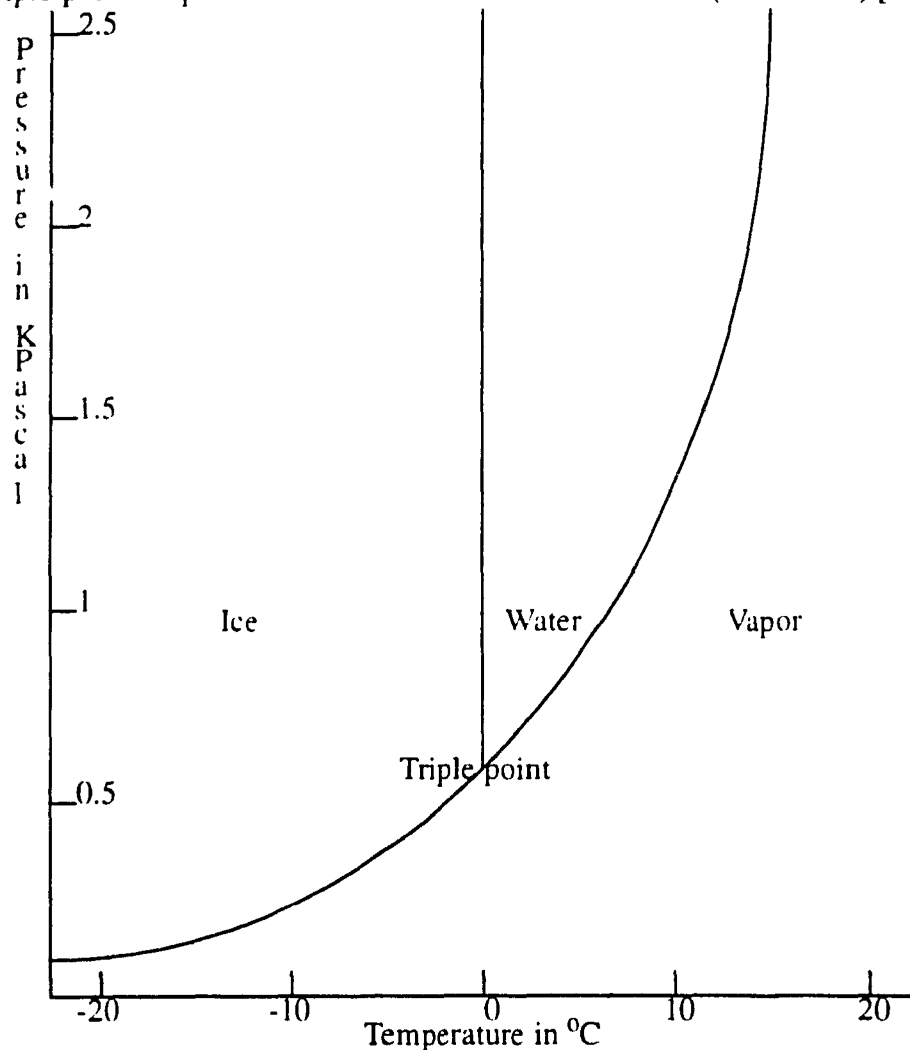


Figure (F1): *Phase diagram of water at low pressure.*

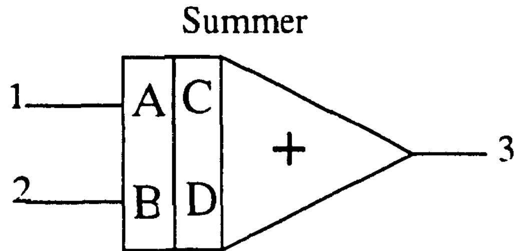
---

* torra=Absolute pressure equivalent to 1 mm of Mercury.

Appendix G

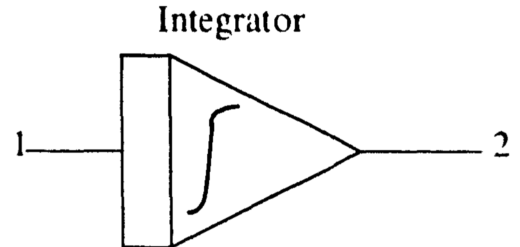
HSPICE Analog elements:

The analog elements that can be used in constructing the HSPICE modelling [41].



ES 3 0 POLY(2) 1 0 2 0 0 C D (HSPICE Notation).

Output=C*A+D*B (Mathematical Notation)



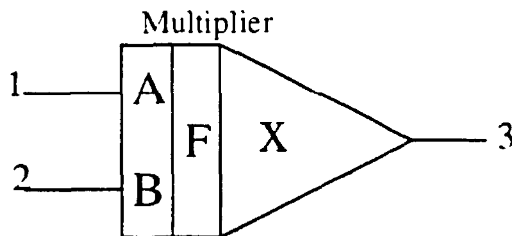
E1 3 0 0 4 1E9

C 4 4 1E-6

R 1 4 1E6 IC=0

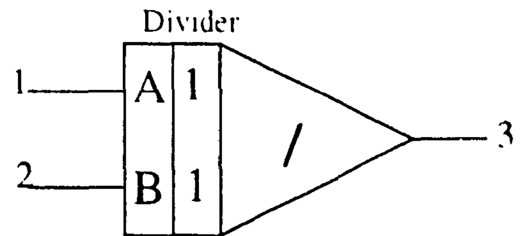
E2 2 0 0 3 1 (HSPICE Notation)

Output=A/S (S Domain Notation)



EM 3 0 POLY(2) 1 0 2 0 0 0 0 F (HSPICE Notation)

Output=F*A*B (Mathematical Notation).



G1D 0 4 1 0 1

G2D 4 0 POLY(2) 2 0 4 0 0 0 0 0 1

ED 3 0 4 0 1 (HSPICE Notation).

Output=A/B (Mathematical Notation)

Appendix H

A Sample Program for the Simulation of the Mechanical System:

```
****All variables are in SI units****

Vcon 30 0 DC 4.427e-12 $Permittivity of space divided by 2
Rcon 30 0 1G
Va 16 0 PWL(0 0 2e-2 0 4e-2 -300) $ applied acceleration
Ra 16 0 1G
vm 21 0 DC 7e-10 $ Mass of the sensor
Rm 21 0 1G
Vb 26 0 DC 1e1 $  Drag force coefficient
Rb 26 0 1G
Vk 27 0 DC 3.4 $ Spring constant
Rk 27 0 1G
Varea 25 0 DC 2.26e-8 $ Surface area for capacitor
Rarea 25 0 1G
xcons 30 21 31 divide
Econs 24 0 poly(2) 25 0 31 0 0 0 0 0 1
Vr 1 0 DC 2.5 $ Voltage of the plate to the RHS
Rr 1 0 1G
Vx 2 0 DC 0 $ Voltage of central plate
Rx 2 0 1G
Vl 3 0 DC -2.5 $ Voltage of the plate to the LHS
Rl 3 0 1G
Vxl 4 0  2e-6 $ Distance between central plate and plate to the left
Rxl 4 0 1G
Vxr 5 0  2e-6 $ Distance between central plate and plate to the right
Rxr 5 0 1G
Exr 6 0 poly(2) 1 0 2 0 0 1 -1
Rexr 6 0 1G
Exl 7 0 poly(2) 2 0 3 0 0 1 -1
```

```
Rexl 7 0 1G
Expr 9 0 poly(2) 5 0 19 0 0 1 1
Rexpr 9 0 1G
Exml 8 0 poly(2) 4 0 19 0 0 1 -1
Rexml 8 0 1G
xdr 6 9 10 divide
xdl 7 8 11 divide
Edrs 23 0 poly(1) 10 0 0 0 1
Redrs 23 0 1G
Edls 22 0 poly(1) 11 0 0 0 1
Redls 22 0 1G
Edrsc 13 0 poly(2) 23 0 24 0 0 0 0 0 1
Redrsc 13 0 1G
Edlsc 12 0 poly(2) 22 0 24 0 0 0 0 0 1
Redlsc 12 0 1G
Eflmfr 14 0 poly(2) 12 0 13 0 0 1 -1
Reflnfr 14 0 1G
Ecoefk 29 0 poly(2) 27 0 19 0 0 0 0 0 1
Recoefk 29 0 1G
Ecoefb 28 0 poly(2) 26 0 18 0 0 0 0 0 1
Recoefb 28 0 1G
Ecoefbk 32 0 poly(2) 28 0 29 0 0 1 1
xcoefbkm 32 21 15 divide
Elrkdm 20 0 poly(2) 14 0 15 0 0 1 -1
Relrkdm 20 0 1G
Elrkdma 17 0 poly(2) 20 0 16 0 0 1 1
Relrkdma 17 0 1G
xbar 17 18 integ   $ Xbar is the speed of the centre plate in m/s
x1 18 19 integ     $ X1 is the displacement of the centre plate in m

*****Capacitors measurement*********************************************
Eeps 100 0 poly(1) 30 0 0 2
```

```
Eepsarea 101 0 poly(2) 100 0 25 0 0 0 0 0 1
xc1 101 9 102 divide
xc2 101 8 103 divide

*****Integrator*********************************************************
.subckt integ 1 2
E1 3 0 4 0 1e9
R1 1 4 1MEG
C1 4 3 1uF IC=0
E2 2 0 0 3 1
.ends
*****Divider************************************************************
.subckt divide 1 2 3
Ediv 3 0 4 0 1
G1div 0 4 1 0 1
G2div 4 0 poly(2) 2 0 4 0 0 0 0 0 1
.ends
************************************************************************
.op
.tran 1e-6 2e-3
.options post converge=1 dcfor=1 itl1=2800 relv=3e-3   rmin=1e-11
.end
```

Appendix I

HSPICE Implementation of a Voltage Controlled Capacitor:

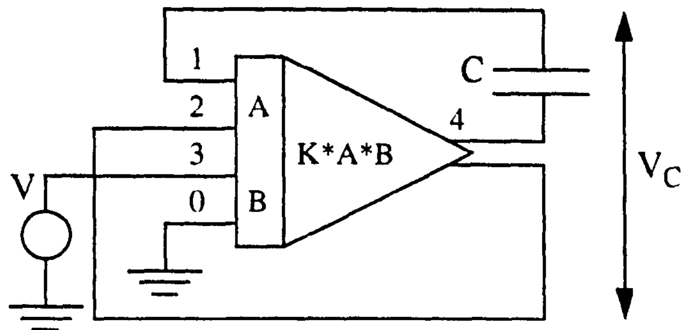


Figure (I1): *Voltage Controlled Capacitor arrangement.*

EVCC 4 2 POLY(2) 1 2 3 0 0 0 0 0 -1 (HSPICE Notation).

The effective capacitance of that circuit can be derived as follows:

$Vcap=V_1-V_4$

$Vout=-V_C*V=V_4-V_2$

$V_4=V_2-V_C*V$

$Vcap=V_1-V_2+V_C*V$

$V_C=V_1-V_2$

$Vcap=V_C+V_C*V$

$Vcap=(1+V)*V_C$

$C_{eff}=(1+V)*C$

This shows that the capacitor used will have an effect on the circuit as though it was (V+1) times its value.

Appendix J

A Sample program for the simulation of the mechanical element combined with the electronic circuit:

```
****All variables are in SI units****

*$$$$$$$$$$$$$$$$$$$$$$$$$$$$$Mechanical Element$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

Vcon 1030 0 DC 4.427e-12 $ Permittivity of space divided by 2.
Rcon 1030 0 1
Va 1016 0 PWL(0 0 20e-6 0 40e-6 196.2 50e-6 19) $ applied acceleration
Ra 1016 0 1
vm 1021 0 DC 7e-10 $ Mass of the sensor
Rm 1021 0 1
Vb 1026 0 DC 1e-3 $  Drag force coefficient
Rb 1026 0 1
Vk 1027 0 DC 3.4 $ Spring constant
Rk 1027 0 1
Varea 1025 0 DC 2.26e-8 $ Surface area for capacitor
Rarea 1025 0 1
xcons 1030 1021 1031 divide
Econs 1024 0 poly(2) 1025 0 1031 0 0 0 0 0 1
Er 1001 0 4 0 1 $ The RHS plate in the model follows that in the cct
Ex 1002 0 3 0 1 $ Centre plate in the model follows that in the cct
El 1003 0 5 0 1 $ The LHS plate in the model follows that in the cct
Vxl 1004 0 2e-6 $ Distance between central plate and LHS plate
Rxl 1004 0 1
Vxr 1005 0 2e-6 $ Distance between central plate and RHS plate
Rxr 1005 0 1
Exr 1006 0 poly(2) 1001 0 1002 0 0 1 -1
Rexr 1006 0 1
Exl 1007 0 poly(2) 1002 0 1003 0 0 1 -1
Rexl 1007 0 1
```

```
Expr 1009 0 poly(2) 1005 0 1019 0 0 1 1
Rexpr 1009 0 1
Exml 1008 0 poly(2) 1004 0 1019 0 0 1 -1
Rexml 1008 0 1
xdr 1006 1009 1010 divide
xdl 1007 1008 1011 divide
Edrs 1023 0 poly(1) 1010 0 0 0 1
Redrs 1023 0 1
Edls 1022 0 poly(1) 1011 0 0 0 1
Redls 1022 0 1
Edrsc 1013 0 poly(2) 1023 0 1024 0 0 0 0 0 1
Redrsc 1013 0 1
Edlsc 1012 0 poly(2) 1022 0 1024 0 0 0 0 0 1
Redlsc 1012 0 1
Eflmfr 1014 0 poly(2) 1012 0 1013 0 0 1 -1
Reflnfr 1014 0 1
Ecoefk 1029 0 poly(2) 1027 0 1019 0 0 0 0 0 1
Recoefk 1029 0 1
Ecoefb 1028 0 poly(2) 1026 0 1018 0 0 0 0 0 1
Recoefb 1028 0 1
Ecoefbk 1032 0 poly(2) 1028 0 1029 0 0 1 1
xcoefbkm 1032 1021 1015 divide
Elrkdm 1020 0 poly(2) 1014 0 1015 0 0 1 -1
Relrkdm 1020 0 1
Elrkdma 1017 0 poly(2) 1020 0 1016 0 0 1 1
Relrkdma 1017 0 1
xbar 1017 1018 integ  $ Xbar is the speed of the centre plate in m/s
x1 1018 1019 integ  $ X1 is the displacement of the centre plate in m
*****Capacitors measurement********************************************
xc1 1025 1009 1102 divide $ Area/(Xo+x1)
xc2 1025 1008 1103 divide $ Area/(Xo-x1)
Ec1 1140 0 poly(1) 1102 0 -1 1 $ subtract 1 from this value since a 1 will be automati
*cally added to it in subckt cap.
```

```
Ec2 1141 0 poly(1) 1103 0 -1 1 $ subtract 1 from this value since a 1
*will be automatically added to it in subckt cap.
xevcc1 1140 3 5 cap $ This is the RHS capacitor
xevcc2 1141 3 4 cap $ This is the LHS capacitor
*****Integrator************************************************************
.subckt integ 1 2
E1 3 0 0 4 1e9
R1 1 4 1MEG
C1 4 3 1uF IC=0
E2 2 0 0 3 1
.ends
*****Divider***************************************************************
.subckt divide 1 2 3
Ediv 3 0 4 0 1
G1div 0 4 1 0 1
G2div 4 0 poly(2) 2 0 4 0 0 0 0 0 0 1
.ends
*****SPICE voltage controlled Capacitor*******************************
.subckt cap 3 2 1
C1 1 4 8.854e-12
Evcc 4 2 poly(2) 1 2 3 0 0 0 0 0 -1
.ends
*****************************************************************************

*$$$$$$$$$$$$$$$$$$$$$$$$$$$$Electrical Circuits$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

*****************************Clocks*********************************
voscb 2 0 pulse (0.000000000e+00 3.3000000000e+00 2.500000000e-07
+ 1.000000000e-08 1.000000000e-08 2.300000000e-07 1.000000000e-06)
vosca 1 0 pulse (0.000000000e+00 3.3000000000e+00 0.000000000e+00
+ 1.000000000e-08 1.000000000e-08 2.300000000e-07 1.000000000e-06)
***************************Voltage Sources*****************************
vv41 10 0 -3.3
```

```
vv40 21 0 -3.3
vv39 17 0 -3.3
vv38 19 0 -3.3
vv37 13 0 -3.3
vv36 15 0 -3.3
vv33 20 0 3.3
vv32 14 0 3.3
vv31 12 0 3.3
vv30 18 0 3.3
vv29 16 0 3.3
vv28 9 0 3.3
******************************vr and -vr*******************************
vv27 11 0 -3
vv26 8 0 3
***************************Transmission Gates***************************
mq25 8 2 5 9 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u ps=
+ 17.52u nrd=1 nrs=1
.model m1mmpmos pmos vto=-560m ld=153n tox=27n pb=800m nsub=3.6e+16
+ nfs=225g theta=35.9m level=3 vmax=217k mj=500m gamma=864m rsh=65 kp=
+ 17.7u is=10f cgso=251p af=1 eta=147m delta=1.53 fc=500m xj=409n
+ kappa=5.69 cgbo=256p cj=618u uo=138 phi=765m cgdo=251p
mq24 5 1 8 10 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
.model m2mmnmos nmos vto=828m ld=240n tox=27n pb=800m nsub=1.6e+16
+ nfs=868g theta=34.7m level=3 vmax=1.6meg mj=500m gamma=586m rsh=
+ 62.5 kp=68u is=10f cgso=269p af=1 eta=141m delta=1.06 fc=500m xj=
+ 297n kappa=10m cgbo=256p cj=419u uo=532 phi=725m cgdo=269p
mq22 24 1 3 18 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq21 3 2 24 19 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4 5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq19 11 2 4 12 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
```

```
mq18 4 1 11 13 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq16 3 2 0 16 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq15 0 1 3 17 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq13 5 1 0 20 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq12 0 2 5 21 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=
+ 1 nrs=1
mq10 4 1 0 14 m1mmpmos l=1.5u w=5.76u ad=17.28p as=17.28p pd=17.52u
+ ps=17.52u nrd=1 nrs=1
mq9 0 2 4 15 m2mmnmos l=1.5u w=1.5u ad=4.5p as=4.5p pd=9u ps=9u nrd=1
+ nrs=1
****************************paracitics******************************
ccp2 4 0 70ff $ Cp2
ccp1 5 0 70ff $ Cp1
ccp3 3 0 50ff $ Cp3
******************************filters*******************************
RFL1 6 7 1e6 tc=0 0          $ R1
CFL1 7 0 5p tc=0             $ Cf1
RFL2 106 109 1e6 tc=0 0      $ R2
CFL2 0 109 5p tc=0           $ Cf2
****************************Integrator Circuit**************************
rr42 24 6 1e6 tc=0 0         $ Rf
cc6 24 6 50fF tc=0           $ Cint
cc4 24 0 10p tc=0            $ Cinp
xopamp1 0 24 6 opamp
******************************Buffer Circuit**************************
xopamp2 7 106 106 opamp
*********************************OPAMP******************************
.subckt opamp 5 6 1
```

```
*this is the netlist file for a cmos opamp supplied to cmc by goal
* company and implemented on mitel process.
* net 0 = gnd!
* net 1 = vout
* net 2 =
* net 3 =
* net 4 =
* net 5 = vin+
* net 6 = vin-
* net 7 = vdd
* net 8 = vss
* net 9 =
* net 10=

vdd 7 0 3.3
vss 8 0 -3.3
* capacitor(0) = /+8
c0 2 9 1.40251e-11
rc 9 1 98[illegible]
rin 7 10 140k

.model model2 pmos level=3 vto=-0.56 phi=0.765 gamma=0.864
+nsub=3.6e+16 bex=-1.5 kp=1.77e-05 nfs=1.6617e+09 uo=138
+vmax=217000 xj=4.09e-07 ld=1.53e-07 theta=0.0359 af=1
+cgbo=2.5e-13 cgdo=2.51e-10 cgso=2.51e-10 tox=2.7e-08
+wd=9.77e-08 capop=12 is=1e-14 cj=0.000618 mj=0.5 pb=0.8
+rsh=65.2 delta=1.53 kappa=5.69 eta=0.147
* pfet(1) = /+7
m1 1 2 7 7 model2 w=0.0001604 l=4e-06 ad=8.9824e-10
+as=8.9824e-10 pd=0.000332 ps=0.000332
* pfet(2) = /+[illegible]
m2 2 4 7 7 model2 w=7.54e-05 l=6e-06 ad=4.3732e-10
+as=4.0716e-10 pd=0.0001624 ps=0.0001616
```

```
* pfet(3) = /+5
m3 4 4 7 7 model2 w=7.54e-05 l=6e-06 ad=4.2224e-10
+as=4.2224e-10 pd=0.000162 ps=0.000162
.model model3 nmos level=3 vto=0.828 phi=0.725 gamma=0.586
+nsub=1.6e+16 bex=-1.5 kp=6.8e-05 nfs=8.68e+11 uo=532
+vmax=160000 xj=2.97e-07 ld=2.4e-07 theta=0.0345 af=1
+cgbo=2.56e-13 cgdo=2.69e-10 cgso=2.69e-10 tox=2.7e-08 wd=1e-10
+capop=12 is=1e-14 cj=0.000419 mj=0.5 pb=0.8 rsh=62.8 delta=1.06
+kappa=0.01 eta=0.141
* nfet(4) = /+4
m4 1 10 8 8 model3 w=7.54e-05 l=5e-06 ad=4 0716e-10
+as=4.3732e-10 pd=0.0001616 ps=0.0001624
* nfet(5) = /+3
m5 8 10 3 8 model3 w=3.04e-05 l=5e-06 ad=1.7632e-10
+as=1.6416e-10 pd=7.24e-05 ps=7.16e-05
* nfet(6) = /+2
m6 2 5 3 3 model3 w=0.0001504 l=2.4e-06 ad=8.4224e-10
+as=7.8208e-10 pd=0.000312 ps=0.0003112
* nfet(7) = /+1
m7 4 6 3 3 model3 w=0.0001504 l=2.4e-06 ad=8.1216e-10
+as=8.1216e-10 pd=0.0003116 ps=0.0003116
* nfet(8) = /+0
m8 8 10 10 8 model3 w=3.04e-05 l=5e-06 ad=2.128e-10
+as=1.7024e-10 pd=7.48e-05 ps=7.2e-05
.ends
*****************************************************
.temp 27
.options post interp  converge=1 dcfor=1 itl1=2800 relv=5e-3
+ rmin=1e-10 newtol=1 brief $ Note that RELV value solved the problem
*of convergence and allowed  the decrease of gmindc without decreasing
* rmin
.end
```

Appendix K

Additional attractive features of microsensors:

In addition to the targeted features, while working to reduce the size of the sensors, some additional improvements came as side effects from the miniaturization process and that worked to substantiate the cause.

When measuring with traditional sensors, the need is to measure the phenomena without affecting it. For example, measuring the temperature of a small volume of gas with a thermometer, requires the large mass of Mercury in the thermometer to be heated. This would certainly change the temperature of the gas. Also another example would be when measuring the acceleration of a small body, then the added mass of the bulky accelerometer will certainly change the acceleration of that body. This introduces high inaccuracies in the measurement.

Now if the mass of the measuring devices was reduced, by miniaturization, then this effect will be greatly reduced and in addition, some other features will be enhanced. For example, take the response time of a thermocouple having a time constant τ, given by:

$$\tau = \frac{m \times Cp}{H \times A} = \frac{Cp}{H} \times \frac{\rho \times V}{A} \qquad (I1)$$

where m is the mass of thermocouple, Cp is the specific heat of sensor material, H is the heat transfer coefficient, A is the surface area of thermocouple, V is the volume of the sensor and ρ is the density of sensor material.

Assuming that the miniaturization reduces all the dimensions by a factor of k. For the same materials (Cp, ρ and H constants) then the time constant will be proportional to the ratio of the volume to the area (which will be the height h assuming a uniform shape).

$$\frac{\tau 1}{\tau 2} = \frac{h1}{h2} = \frac{h1}{h1/k} = k \qquad (I2)$$

The response time was reduced by, k. In some processes, this might prove to be crucial. Not only the response time for thermometers is reduced. This also applies to any sensor that depends on the change in the inertia of the system would benefit from reducing that inertia.

An important industrial parameter is the shock survival. Each material has a value of the fracture stress σ_{frac} the stress after which the material will endure a fracture. One of the design requirements is to make sure that the sensor will survive up to the highest possible shock that it might encounter. This is achieved by making the highest possible impact stress less than the fracture stress (σ_{frac}) of the sensor material. The impact stress is given by:

$$\sigma(imp) = c_f \times \frac{m \times a}{A} = c_f \times a \times \rho \times \frac{V}{A} \qquad (I3)$$

where c_f is the shape factor, m is the mass of the body, a is the decceleration caused by the collision, A is the area subjected to collision, V is the volume of the body and ρ is the density of the material

Now using the same miniaturization factor k, and the same materials then c_f and ρ will be the same while the acceleration, a depends slightly on elasticity of the material, otherwise it is constant. The impact stress will be proportional to the ratio between the volume and surface area which will be the height h.

$$\frac{\sigma(imp)1}{\sigma(imp)2} = \frac{h1}{h2} = k \qquad (I4)$$

i.e. by miniaturization, results a sensor that can survive, k times the shock survival of the original one. That means higher durability.

Appendix L

Pad assignment for the second implementation:

The pad assignment for the second implementation as part of the chip "CADP1" is described here. The reference point is the lower right corner of the chip as it appears in Figure (6.21). Starting from the reference point and counting upwards, the pads will be assigned as follows:

1-The output pad for the Y direction. This pad is protected against over-voltage.
2-The output pad for the Y direction. This pad has no over-voltage protection.
3-Vss.
4-The output pad for the X direction. This pad is protected against over-voltage.
5-The output pad for the X direction. This pad has no over-voltage protection.
6-V_{ref+} for the X direction.
7-V_{ref-} for the X direction.

Now, going back to the reference point and this time start counting to the left, the pads will be assigned as follows:

1-Gnd.
2-V_{ref+} for the Y direction.
3-C_{lk1} for the Y direction.
4-V_{ref-} for the Y direction.
5-C_{lk2} for the Y direction.
6-Vdd.
7-The multiplexer input for the mechanical-structure/fixed-capacitors selection.