INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

Bell & Howell Information and Learning
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA

UMI®
800-521-0600

EMTP Simulation Of An Active Filter Operating With Weak AC Distribution System

Rachit Arora

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

for the Degree of Master of Applied Science at

Concordia University

Montreal, Canada

January 1999

Abstract

EMTP Simulation Of An Active Filter

Operating With A Weak AC Distribution System

Rachit Arora

An AC distribution system has a myriad of loads connected at the system bus. Many of the DC based loads cause disturbance on the ac bus due to high harmonic load currents. Traditionally passive filters are used for filtering these load harmonics. Recent technological advances have enabled the use of high frequency switching devices in the development of active filtering techniques.

In this thesis, an active filter topology was selected for the system, and a test system was modeled using EMTP. The objective of active filtering is to meet the harmonic and reactive load locally, and thus removing the harmonic content of source currents. The AF controller based on the on-line power computation scheme was modeled. Tracking control was demonstrated using two control methodologies - hysteresis band control and sliding mode control.

A performance comparison was made between the two control schemes, and the impact of various circuit and control parameters on the filtering performance was studied. To assess the transient performance achieved with the control schemes presented, results from EMTP based studies for this distribution system under various AC-DC fault conditions are analyzed.

Acknowledgment

I would like to thank my supervisor, Dr. V. K. Sood for his financial support during my Masters research work, and appreciate his valuable advice and patience with which he guided me during my deliberations.

The other aspect of my stay here has been made possible in the company of many friends who have been a constant support with their love, affection and presence.

Thanks *Meghana, Cthru, Mahesh, Subha, V. Pisini, Tanu & Vijay, Miki, Uju, Daksha, Jaya, Jasjit* and *Sraddha* for everything. I also thank all my colleagues at GM 905, for making the office a habitable place to stay late hours.

The assistance of Department secretaries and Computing Services is appreciated. I also owe my gratitude to Dr. B. N. Singh and Dr. A. Chandra of the ETS for assisting me in technical clarifications.

My parents and my sister, *Ruchi* were always a source of encouragement and moral support. I dedicate this work to them.

Dedicated to
my parents
and my sister
Ruchi

CONTENTS

List of Figures

List of Tables

Chapter 1

Introduction

Power Electronics technology has been increasingly used in many fields in recent years. The proliferation of non-linear loads on distribution systems has resulted in the deterioration of power quality in a substantial way. In a utility system, it is desirable to prevent harmonic current which result in EMI and resonance problems, and limit reactive power flow so as to reduce the losses in transmission and/or distribution lines. Further more a stable and harmonic-free bus voltage is required at the user end.

Traditionally, shunt passive filters comprised of tuned LC elements and capacitor banks were used to filter the harmonics and to compensate for reactive current due to non-linear loads. However, in practical applications these methods have many disadvantages.

In the last two decades, considerable progress has been made in the field of Active Filters (AFs). AFs are inverter circuits, comprising of active devices i.e. semiconductor switches that can be controlled so as to act as harmonic current or voltage generators. Different topologies and control techniques have been proposed for their implementation. AFs are superior to passive filters in terms of filtering characteristics and improve the system stability by removing resonance related problems.

This thesis deals primarily with an EMTP (Electro-magnetics Transient Program) based digital simulation of a shunt active filter compensating for harmonic and reactive power drawn by a three phase controlled rectifier. The system AC bus is fed from a weak AC source, hence the effect of source impedance on system behavior is studied here. The performance of the AF system is presented for steady state and transient analyses.

1.1 Effect of Harmonics

Harmonic terminal voltages may be produced partly by the power generator itself (source harmonics) and partly by non-sinusoidal load currents flowing through the internal impedance of the generator (load harmonics).

Harmonic voltages at the terminal end cause harmonic currents in the connected load. This leads to extra losses and heating in the load. Capacitors attached at the terminal end for power factor correction also suffer extra heating losses.

Overvoltages may arise due to resonance conditions between a shunt capacitor bank and the rest of the system at a harmonic frequency. Due to the distortion of the terminal bus voltage, unstable or inappropriate converter operation may result. Ripple control systems using the power distribution network for transmission of control signals may suffer interference problems. Harmonics also produce noise and interference in telephone circuits running adjacent to power networks.

Such problems lead to reduced system stability and safety margins, and may require derating of distribution equipment.

1.2 Passive AC Filters

Passive filters in power systems are usually used as shunt filters, the accepted practice being to connect a number of separate shunt branches across the terminals of the AC bus to reduce the harmonic distortion in the AC system. Each of these branches is tuned to one of the predominant harmonics, with a high pass branch added that exhibits low impedance for the remaining higher order harmonics.

Passive filters serve two purposes: (1) to reduce the harmonic voltages and currents in the AC power network to acceptable levels and (2) to provide all or part of the reactive power consumed by the converter, the remainder being supplied by shunt capacitor banks, by synchronous condensers, or by the AC power system.

The design of passive filters for a system is complicated by several factors:

- The source impedance, which is not accurately known and varies with the system configuration, strongly influences filtering characteristics of the shunt filter. The impedance of the tuned branches must be low with respect to the source impedance at the harmonic frequencies to provide the filtering required. If the source impedance is low, and the desired degree of attenuation is high, the size and cost of passive filters can become prohibitive.
- The shunt passive filter acts as a current sink to the harmonic voltages present in the AC source voltage. In the worst case, the shunt passive filter may come to series resonance with the source impedance. Even small ripple voltages at resonant frequencies present in the source voltage may produce excessive harmonic currents in the filter.
- At a specific frequency ($f_o = 1/\{2*pi*sqrt([L_{source} + L_{filter}]C_{filter})\}$), an anti-resonance or parallel resonance condition occurs between the source impedance and the shunt passive filter, which leads to harmonic amplification in the source and filter.
- The tuned branches are designed for a range of frequency variation allowed for by the AC source. The larger the variation of the supply frequency, larger would be the variation of predicted harmonic frequencies and more impractical the sizes of components used in each branch.
- The passive filter also does not handle uncharacteristic lower order harmonics (such as 2nd, 4th, etc.) which may be present in the load current due to unbalanced loads, faulty equipment etc.

With remarkable progress in the speed and capacity of semiconductor switching devices like GTO thyristors and IGBTs, active filters composed of voltage or current source inverters are being put to practical use, because they have the ability to overcome the above mentioned disadvantages inherent in passive filters. Moreover, active filters act as "harmonic eliminators" rather than "harmonic attenuators", thus improving filtering characteristics.

1.3 Problem Definition

A test system needs to be defined for distribution system studies. It consists of a DC load connected to a rectifier, that presents a non-linear load and an active filter (AF) that compensates for harmonics and reactive power drawn by the load. The AF should exhibit fast dynamic response and good efficiency. The AF control scheme should function irrespective of the source impedance, and be simple to implement. After compensation the non-linear load should present a fundamental frequency, unity power factor load to the AC source.

The AF should also be able to maintain the Total Harmonic Distortion (THD) of source current within 5%. The simulation model assumes ideal switches, but the switching frequency limit imposed by real switches is taken into consideration during the model design.

The strength of an AC system is measured in terms of Short Circuit Ratio (SCR) which is defined as

$$\text{SCR} = \frac{\text{Short Circuit Level at AC bus}}{\text{Rated Power}}$$

If SCR is less than 3, the AC system is considered weak.

Most of the published works consider a strong AC system feeding non-linear loads, thus not considering the distortion introduced in the terminal voltage. This escapes the practical situations faced by distribution systems, and hence does not give a realistic model. The model developed here would take a weak AC system into consideration and also give detailed analysis of the model under various AC-DC fault conditions.

1.4 Literature Survey

Harmonic levels in distribution systems have been well investigated by utility companies [1,2,3]. In [1], results of a research project involving the investigation of power system harmonic levels on selected distribution circuits on the American Electric Power

System (AEP) were presented. Field measurements were done to record harmonic levels in three classes of distribution circuits - residential, commercial and industrial. Analysis of data collected provided an insight into harmonic distortion in a real distribution system.

In [3], the authors emphasized a probabilistic approach for data collection and the importance of statistical distributions of harmonics in terms of maximum, mean and minimum levels.

The problems faced by passive filter systems influenced the development of active filters. Active filters have been studied, since their basic compensation principles were proposed in the 1970's, to compensate for reactive power, negative-sequence currents and harmonics in industrial power systems.

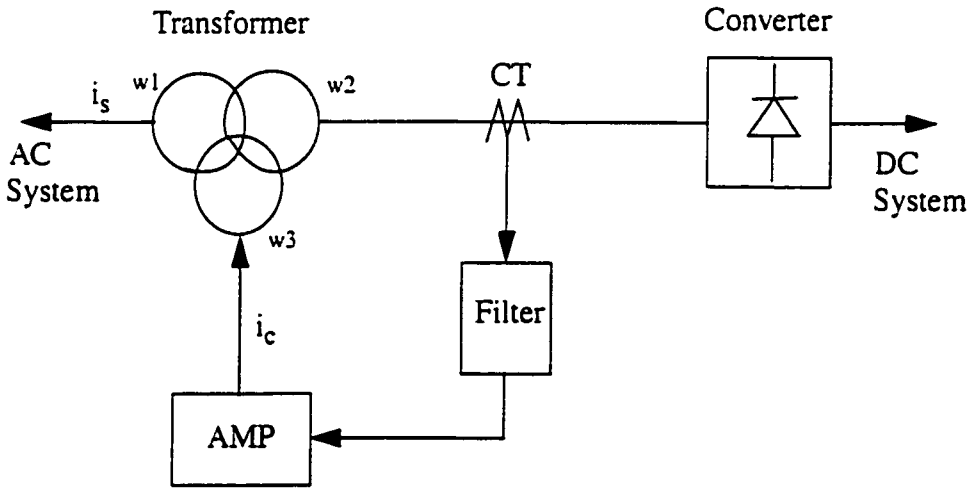


Fig 1.1 Harmonic elimination by magnetic compensation

The basic principle of a shunt active filter was originally presented by H. Sasaki and T. Machida in 1971 [4]. As shown in Fig 1.1, a shunt active filter is controlled in such a way so as to actively shape the source current, i_s, into a sinusoid by injecting the compensating current i_c. The authors proposed a new method of eliminating AC harmonic current based on the principle of magnetic flux compensation in a transformer core. A signal

detection circuit extracted the fundamental current component of the non-linear load current flowing in the secondary transformer winding and generated the harmonic current, which after appropriate turns-ratio amplification, is injected in the transformer tertiary winding. This produced harmonic flux cancellation in the transformer core, and resulted in only fundamental frequency current in the primary winding. This technique is considered as the archetype of shunt active filters. Since a linear amplifier was used to generate the compensating current, its realization is unreasonable due to low efficiency.

In 1976, L. Gyugyi and E. C. Strycula [5], presented a family of shunt and series active filters, and established the concept of active filters consisting of PWM inverters using power transistors. However, they could not be realized in real power systems because high-power high-speed switching devices were unavailable in the 1970's.

The work is considered a pioneering effort, as it laid fundamental principles in the theory of active filters. Later research evolves around the same fundamental concepts, but advancing towards newer control techniques for switching signals generation. With the remarkable development and advances in switching speed and capacity of power semiconductor devices in the 1980's, active filters consisting of PWM inverters have been put to practical applications in real power systems.

Earlier work on active filters discussed compensation characteristics only for steady state conditions. The calculation circuit for the compensating current references was simple, and only ideal compensation characteristics could be attained. However, in transient states such as those caused by fluctuating loads, the design of compensating current calculation circuit becomes difficult.

In 1984, H. Akagi *et al.* [6] introduced a new concept of instantaneous reactive power. It dealt with arbitrary 3 phase voltages and currents considering their distortion content. The instantaneous voltages and currents were represented as instantaneous space vectors on the a-b-c coordinate system, with the a,b,c vectors fixed on the same plane, apart from each other by 2 pi/3. These space vectors were then transformed along the

alpha-beta orthogonal coordinate system. The instantaneous real and reactive power defined along the alpha-beta coordinates have a DC and AC component. The AC component pertains to the reactive and harmonic current of the load. The instantaneous active and reactive power were computed on-line and the AC component was extracted with a suitable filter. The design of the extraction filter has a significant effect on the compensation characteristics of the active filter. With the choice of cut-off frequency, the AF can be made to compensate for only the harmonic current or the reactive current or both. However the theory was conceptually limited to three phase systems without zero-sequence currents.

A generalized instantaneous reactive power theory which is valid for sinusoidal or non-sinusoidal, balanced or unbalanced three phase power systems with or without zero-sequence currents was later proposed by F. Z. Peng and J. S. Lai [7]. Active filters controlled on the basis of instantaneous reactive power theory provided good compensation characteristics in steady state as well as transient states.

At the same time, the following problems of active filters were pointed out:

- It was difficult to realize high power PWM inverters with rapid current response and low loss for use as a main circuit of active filters.
- The initial cost was high as compared with that of passive filters, and active filters were inferior in efficiency to passive filters.
- Injected currents by shunt active filters may flow into shunt passive filters and capacitors connected to the power system.

Therefore attention was paid to combined or hybrid systems of active filters and shunt passive filters.

In [8], the authors presented a novel compensation scheme using a shunt active filter along with a conventional shunt passive filter. By sharing their roles so that the active filter absorbs lower order harmonic currents and the passive filter absorbs higher order

ones, the active filter can fulfil its function with relatively small capacity, which brings an economical system. A lead function was introduced in its controller which brought about an interesting characteristic that the active filter can act as a damping device in a parallel resonance circuit formed by the passive filter and the power supply system. This made it possible to realize an ideal harmonic filter with no amplification due to the parallel resonance over a whole range of harmonic orders. Experimentally the technique was verified on a cycloconverter load (2 sets of 2800 kW), being compensated with a 900 kVA active filter and a 6600 kVA passive filter.

In [11], the authors proposed a combined system of a shunt passive filter and a small rated series active filter. The combined system gave better filtering characteristics and lower initial and running costs. The technique was verified on a 20 kVA 3-ph, thyristor load, compensated by a shunt passive filter of 10 kVA and a series active filter of 0.45 kVA. The function of the series active filter is not to directly compensate for the harmonics of the rectifier, but to improve the filtering characteristics of the shunt passive filter and to solve the resonance related problems of a passive filter used alone.

It was shown that the series AF acts as a "damping resistance" which could eliminate the parallel resonance between the shunt passive filter and the source impedance, and also acts as a "blocking resistance" which could prevent the harmonic current produced by the source harmonic voltage from flowing into the shunt passive filter.

A novel hybrid filter topology was presented by M. Rastogi, N. Mohan and A. E. Edris in [12]. A passive filter in series with an inverter operating in current controller mode was connected in shunt at the system bus. It was shown that the proposed filter has a rating of only 9% as compared to the converter in an active filter acting alone and approximately half of that of a series hybrid filter.

In [13], P. T. Cheng, Subhashish Bhattacharya and D. M. Divan presented a hybrid parallel active filter (HPAF). The AF implements square-wave inverters in series with

tuned passive L-C filters, to provide supply-load harmonic isolation at dominant harmonic frequencies (5^{th} & 7^{th}) and meets IEEE 519 harmonic standards for high power application. It was shown that small rated AFs (1%-2%) of the load rating, provide a practically viable and cost effective solution for high power non-linear loads upto 100 MW.

In [14], P. G. Barbosa, J. A. Santisteban and E. H. Watanabe proposed a shunt series active power filter. The AF consisted of a shunt AF connected to the AC side and a series AF connected to the DC side of a rectifier unit. The shunt AF was controlled to eliminate current harmonics in ac line currents and the series AF was controlled to cancel the output voltage ripple of the rectifier.

For moderate power ratings, active filters function well independently with small power rated filters connected to eliminate switching voltages and currents. Different control techniques like PWM carrier based error sawtooth control [8,11,19,20,23], hysteresis based dead band control [6,10,16,21], magnetic flux compensation have been proposed and experimentally verified.

In [15], an AF for a 3-phase controlled rectifier system was presented. The active filter comprised of a 3-phase voltage source inverter (VSI) with a DC bus capacitor source, connected in shunt to the AC source. The converter used 2 control loops. The outer control loop regulated the voltage across the DC bus capacitor, and generated reference phase AF currents. The inner control loop used sliding mode control to shape the AF currents in accordance with the reference currents.

In this work, the following assumptions were made:

- An infinite (strong) AC system was assumed. Since source impedance was not considered, the problem of voltage distortion at the terminal end does not occur.
- The line currents supplied by the source are in phase with the source voltages.
- An isolation transformer served as the connection impedance between the AF and the AC system.

- The sliding mode control principle was used to check the state of the system at a constant decision frequency, and to generate appropriate gating signals for the AF switches.

The sliding mode control principle used is easy to implement, and sets an upper limit to the switching frequency. The authors gave a good analysis of the effect of decision frequency, DC bus voltage, and variation of load on the THD of source current, power factor and efficiency of the system. The AF was able to supply load harmonics and limit the source current THD to 12-13% at full load.

In [16], a different control scheme was used to estimate the reactive and harmonic content of the non-linear load. The system here too, comprised of a shunt connected 3-phase voltage source active filter.

But here also, the effect of source impedance was not considered. The non-linear load considered was a diode-rectifier feeding a capacitive load. The control scheme measured the active power requirements of the load on-line, and generated reference currents for the AF switches. The switching signals for the AF switches were generated by a hysteresis based controller. The scheme provided excellent performance in terms of limiting the THD of source current to less than 5% at full load, along with a good efficiency.

Although hysteresis controllers provide excellent current tracking, they inherently rely on having a variable switching frequency. However, a proper choice of the hysteresis band and the connection impedances limits the average switching frequency to within the switching constraints. The work also highlighted the fast response of the active filter to transient and load variations.

An interesting application of an active filter as a "load balancer" has been shown by V. B. Bhavaraju and P. N. Enjeti in [17]. An active filter based on a PWM-controlled static ac to dc converter topology with inductive load is designed to act as a continuous load balancer. The negative sequence component of load current is continuously measured

and an equal but opposite of this quantity is injected by the AF at the point of installation, thereby achieving the objective of continuous load balancing of unbalanced load.

1.5 Proposed Approach

The objective of this thesis is to develop test models and control schemes for an active filter system. Practical difficulties in distribution system studies are realized by considering a weak AC system. A line impedance (20% base impedance) connects the AC source to the system AC bus. An active filter along with a small high pass AC filter is connected at the AC bus to filter current harmonics generated by nonlinear loads connected at the bus. Hysteresis based current control and sliding-mode control techniques are applied to the active filter and the performance of the system is compared under different test conditions.

1.6 Thesis Outline

In Chapter 2, the concept of AFs is explained. The shunt active filter topology is selected, and its working principle is described. The distribution system test model considered is described. Each building block and its circuit configuration is discussed.

In Chapter 3, the control schemes implemented for active filter control are presented. The impact of circuit parameters, and controller elements on the AF performance is discussed.

In Chapter 4, simulation results for the system under steady and transient state are presented. The system model is tested under various AC-DC fault conditions, and its performance analyzed.

Finally, in Chapter 5, conclusions from this study, and recommendations for further work are provided.

Chapter 2

System Configuration

2.1 Introduction

This chapter introduces the concept of active filters. The basic active filtering methodologies are explained. The system model considered to verify this technique is described. The various sub-units of the model and their circuit configurations are explained. The selection of an active filtering technique, for a weak AC distribution system is discussed.

2.2 Active Filters [5]

Active filters are the modern approach to harmonics filtering. They act as ideal current or voltage sources connected in shunt or series with the AC supply to cancel harmonic terminal voltages or to supply harmonic currents produced by both the internal harmonic voltages of the supply and the nonlinear load.

The realization of these generators is accomplished by appropriately modulated switching circuits which operate in a self-sufficient manner from passive reactive storage elements (inductors, capacitors) without the need of a DC source. A number of control schemes like PWM, hysteresis-control, sliding-mode control etc. are used to generate switching signals for the controllable switching devices. The switching rate in these circuits is high enough to achieve good filtering characteristics in the low harmonic range, with distortion components shifted to higher frequencies where they may easily be

removed by passive filtering.

There are two basic filtering techniques - shunt and series filters [2]. The different topologies are shown in Fig. 2.1.

The system consists of a non-sinusoidal voltage source with a reactive internal impedance, (X_s= w.L_s), supplying a nonlinear load. The AC source V_s with fundamental component V_F and internally generated ripple component V_r, supplies a nonlinear load current I_L, with fundamental component I_F and harmonic component I_R.

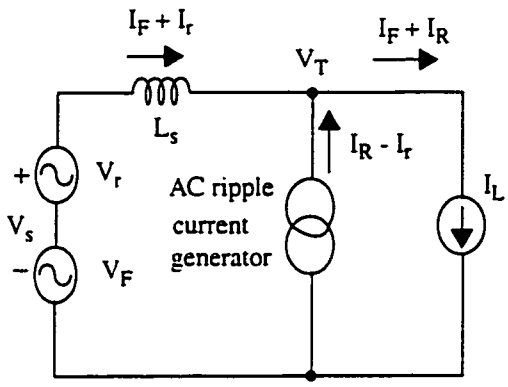
$$V_s = V_F + V_r$$

$$I_L = I_F + I_R$$

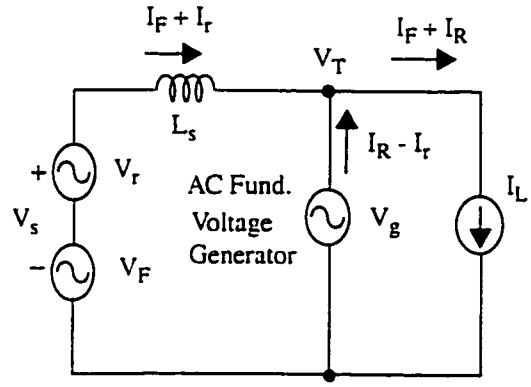
In this general case, the distortion of the terminal voltage V_T is caused by both the internally generated source harmonics V_r and the harmonic load current I_R flowing through the source's internal impedance. An ideal filter should remove all the harmonics from the terminal voltage without affecting the flow of the fundamental load current I_F from the AC source.

(i) Shunt ripple current generator

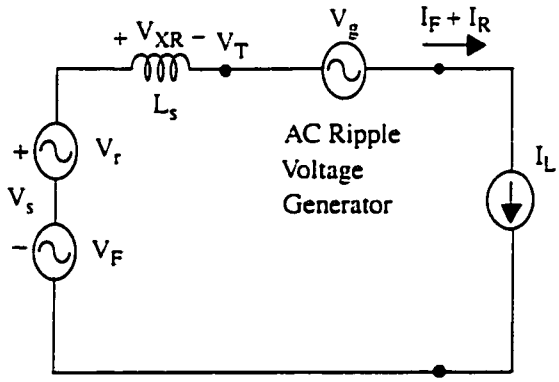
The shunt filters work on the concept of harmonic compensation. An ideal ripple current generator is connected in shunt at the terminal bus, as shown in Fig. 2.1(i). It supplies all the load harmonics (I_R) and absorbs all the source harmonic current (I_r). This ensures that no load harmonics flow through the source impedance and that no source harmonic current flows into the load. It therefore acts as a short circuit at all harmonic frequencies. Consequently, the terminal voltage $V_T = V_F - I_F.Z_s$, is a pure sinusoidal voltage of fundamental frequency.



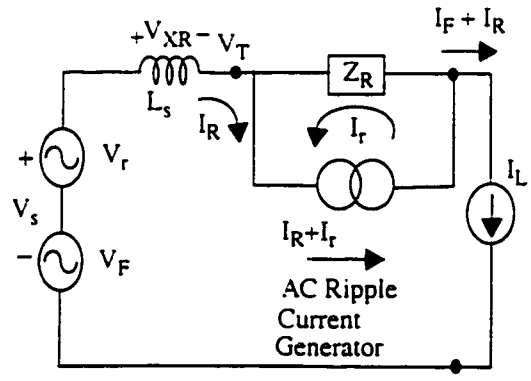
(i) Shunt ripple current generator



(ii) Shunt fundamental voltage generator



(iii) Series ripple voltage generator



(iv) Series impedance and ripple current generator

Fig. 2.1 Active Filter Topologies

(ii) Shunt fundamental voltage generator

An equivalent filtering technique is realized by an ideal voltage generator connected in shunt at the terminal bus (Fig. 2.1(ii)). It produces a voltage, V_g equal to the fundamental of the terminal bus voltage, $V_T = V_F - I_F Z_s$. As a result the load harmonics (I_R)

are restricted to flow through the shunt filter, and the ripple voltage (V_r) drops across the source impedance. The shunt filter thus absorbs the source harmonics (I_r) and supplies the load harmonics (I_R), thereby maintaining a sinusoidal voltage at the terminal bus.

(iii) Series ripple voltage generator

This technique uses the concept of voltage cancellation. As shown in Fig.2.1(iii), a ripple voltage generator is connected in series with the source impedance. The terminal voltage V_T is the sum of the fundamental voltage, V_F, the internal source ripple voltage, V_r, and the load ripple voltage, V_{XR} produced by the load current harmonics flowing through the source impedance X_s, i.e. $V_T = V_F + V_r + V_{XR}$ (the voltage drop of I_F is not considered as it doesn't contribute to the filtering problem). The terminal ripple voltage can be cancelled by connecting a perfect ripple voltage generator, $V_g = -(V_r+V_{XR})$ between the source and the load, producing a sinusoidal voltage at the terminal bus.

(iv) Series ripple current generator with series impedance

An equivalent technique is realized by using an AC ripple current generator as shown in Fig. 2.1(iv). Here the ripple voltage required is produced across the impedance Z_R, inserted between the AC source and the load, by an appropriate current generator having a ripple current component I_r such that $I_r Z_R = -(V_r+V_{XR})$. The current generator has another component, I_R, to ensure that the load ripple current bypasses the impedance Z_R. Z_R must exhibit negligible impedance for the fundamental load current I_F in order not to cause an appreciable fundamental voltage drop. Since the ripple voltage is cancelled, the terminal voltage, V_T becomes a fundamental harmonic voltage ($V_T = V_F - I_F Z_s$).

2.3 Active Filter Topology Selection

Theoretically perfect active filters can be realized by ideal current and voltage generators, connected in shunt or series configuration. In the practical realization of such generators, inverter circuits comprising of controllable switches are used. A DC current source in the form of a charged capacitor or inductor powers the inverter circuit. Appropriate modulation schemes are used to generate switching signals for the active filter to modulate required harmonic currents. The filtering characteristic can be improved indefinitely by increasing the switching frequency, but owing to switching rate limitation of semiconductor devices, a proper selection of AF parameters is essential. The switching inverters introduce high frequency distortion components, but these can be removed by passive filters.

Both the series and shunt topologies produce sinusoidal voltages at the terminal end by voltage cancellation or harmonic compensation, but it can be seen from Fig. 2.1 (iii&iv) that in series compensation the AC source carries the load harmonics, I_R, whereas in shunt compensation, Fig 2.1 (i&ii), the load harmonics are filtered locally at the terminal bus, leading to a source current consisting of only the fundamental load current, I_F and a small amount of source ripple current, I_r (if source voltage harmonics are considered).

For a distribution system model, the shunt filter topology is better suited as the load harmonics are not carried by the transmission lines connecting the AC source to the terminal bus, but are compensated locally by an active filter connected at the terminal bus.

Therefore, the shunt active filter topology has been selected in this work.

The shunt ripple current generator topology, as shown in Fig 2.1(i) was preferred over the shunt ripple voltage generator topology (Fig 2.1 (ii)), as an accurate value of source impedance (L_s) is required for the second case in the evaluation of terminal voltage V_T ($V_T = V_F - I_F Z_s$), and it would be of interest to have a control scheme that provides

compensation irrespective of source or line impedance.

The ripple current generator can be realized by a voltage source inverter (VSI) or a current source inverter (CSI). The voltage source inverter powered by a DC bus capacitor is preferred to an inductor powered current source inverter, because a VSI is higher in efficiency and lower in cost than a CSI.

2.4 System Model

The system model considered here to verify the active filter control technique is shown in Fig. 2.2. The system considered is 3 phase and a one-line diagram is shown in the figure. The base quantities for the system taken are:

1 p.u. voltage = 100 Volts

1 p.u. current = 1 Amp

The system has been modeled for 60 Hz line frequency.

It can be divided into the following sub-units:

1. AC side of the system
2. DC side of the system
3. Active Filter
4. Control Circuits

1) AC side of the system

The AC side of the system consists of the distribution system and an AC filter connected to the system terminal AC bus. The system bus is separated from the DC side of the system by an isolation transformer.

i) Distribution System: The distribution system is represented by its simplified Thevenin equivalent circuit. The AC source phase voltage taken is 1 p.u.. A weak AC system is assu-

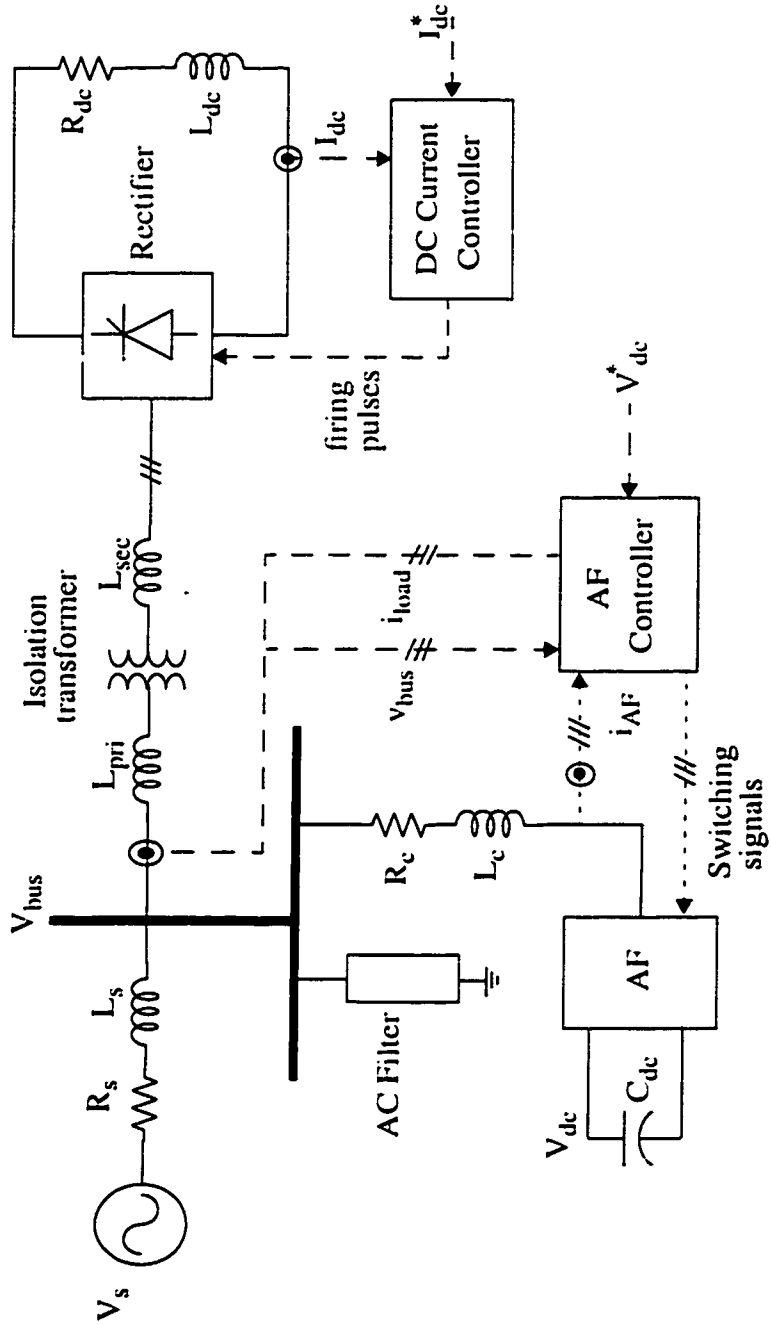


Fig. 2.2 System Model

med with a typical source impedance of 20% base impedance. The impedance is primarily inductive, and a small value of resistance is assumed using a typical quality factor of 50.

ii) AC filter: A high pass AC filter is connected at the system bus to filter out high switching frequency currents introduced by the active filter. The AC filter is of high pass type, and is tuned to the 12^{th} harmonic. The filter components calculation are shown in Appendix A. Fig 2.3 shows the filter circuit configuration.

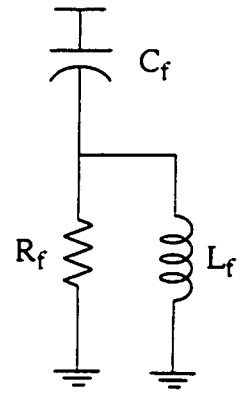


Fig. 2.3 High Pass Filter

iii) Isolation: The AC side of the system is isolated from the DC side by a 3 phase star-star isolation transformer. The transformer line impedance is taken as 20% of base impedance and is divided equally on the primary and secondary side. The impedance is taken as being primarily inductive, and a small value of resistance is assumed.

2) DC side of the system

The DC side of the system comprises of a converter unit and an inductive load.

i) Converter unit: This unit comprises of a 3 phase current controlled rectifier (Fig. 2.4). The rectifier performs conversion of AC bus voltage to DC voltage, which feeds an inductive load. A current controller maintains the output DC current close to its reference value.

The DC controller generates appropriate firing signals for each of the thyristors. The thyristor switches are protected from over-voltages by connecting R-C snubbers across them.

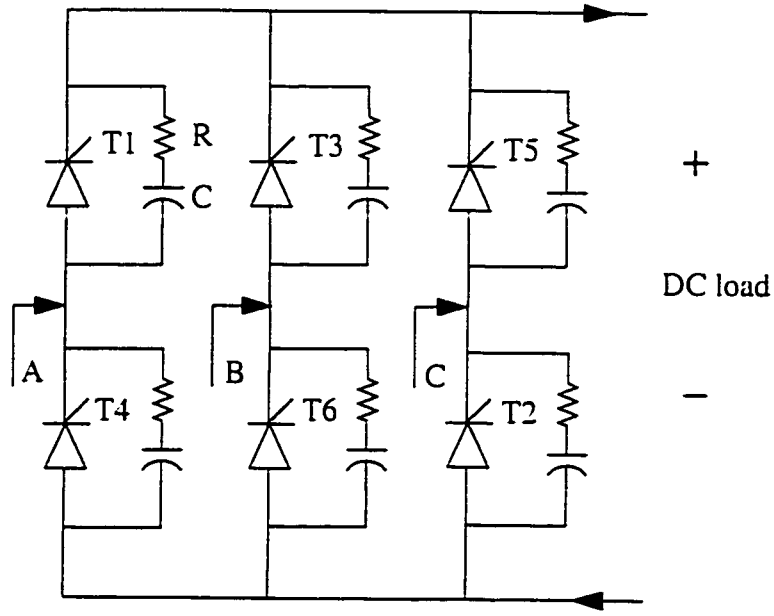


Fig. 2.4 Converter unit

ii) DC load: The DC load of the system comprises of a resistor load R_{dc}=120 ohms and a smoothing reactor L_{dc}=300 mH in series. The high inductance value smooths the ripple in the DC current and prevents it from becoming discontinuous at light loads.

3) Active Filter

The active filter unit comprises of an inverter and connection impedances. The active filter supplies the harmonics and reactive power, thus enabling the AC source to supply only the active power component of the nonlinear load.

i) Inverter unit: The AF consists of a 3 phase voltage source inverter (Fig. 2.5). The inverter switches are made bidirectional by connecting anti-parallel diodes across the

switches. Snubbers are connected across the switch-diode pair to protect the devices from dv/dt and di/dt stresses. The inverter is sourced by a DC bus capacitor, C_{dc}, the voltage of which is maintained at a fixed level to overcome the switching and conduction losses incurred by the AF providing harmonic compensation. The AC source replenishes the energy lost by the AF during compensation period.

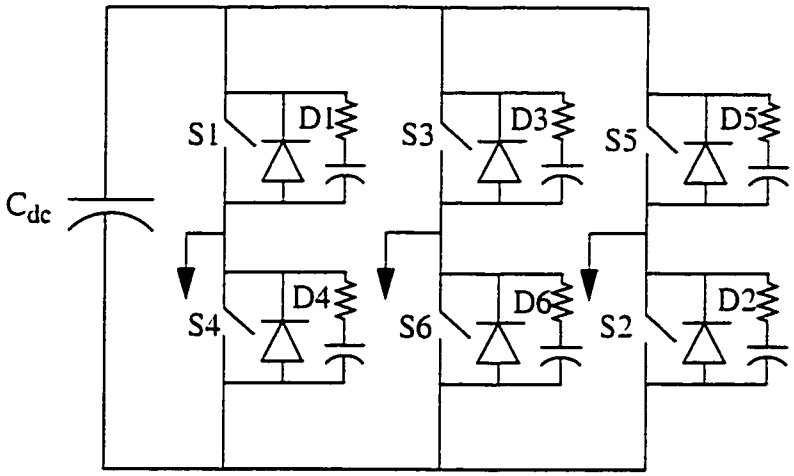


Fig. 2.5 Voltage Source Inverter unit

The choice of switching devices for the inverter depend on the power level of compensation provided by the AF. For medium power application, IGBTs, and for high power application GTOs are suitable. The choice of switching device sets an upper limit to the frequency of operation for the inverter circuit. A GTO inverter can operate to a limit of around 5 kHz, whereas an IGBT inverter may operate upto 80 kHz.

ii) Connection impedances: The active filter is connected to the system bus through series R-L impedances. The connection impedances serve 2 purposes:

1. They separate the high frequency switching AF end terminals from the system bus by

taking the switching voltage harmonics drop across them.

2. They serve an important role in wave shaping the AF line currents about their reference currents.

The component values for the connection impedances are decided upon by the switching frequency constraint imposed by the inverter switching devices. The design of connection impedances is discussed in Chapter 3.

4) Control Circuits

The system comprises of 2 control units.

i) Rectifier Control Unit

The Rectifier Control unit consists of a PI current controller that maintains the DC output current close to its reference value by generating appropriate triggering pulses for the rectifier thyristors.

ii) AF Control Unit

The AF controller consists of an on-line power controller and a tracking controller. The on-line power controller computes the reference currents for the active filter to generate so as to supply the reactive and harmonic current of the nonlinear load. The tracking controller compares the actual AF line currents with the reference currents and generates switching signals for the inverter switches to modulate the reference currents. Different tracking control techniques are available to do so. Hysteresis-band control and sliding-mode control were implemented in this work. The control philosophy for both the schemes is discussed in Chapter 3 and performance of the controllers under different test conditions is demonstrated in Chapter 4.

2.5 Summary

This chapter introduced the concept of active filters. The different techniques of active filtering were stated and the shunt ripple-current generator AF topology was selected for a weak AC distribution system. The test system considered to model a weak AC distribution system was described. Also the various sub-units of the test system and their configurations were elaborated.

Chapter 3

Control Circuits

3.1 Introduction

In this chapter, control circuits of a distribution system operating with a weak AC source are presented. The control circuit consists of a rectifier control unit and an AF control unit.

The rectifier control unit controls the output DC current by generating an appropriate firing angle. A gate firing unit generates firing pulses for each of the rectifier thyristors.

The AF control unit comprises of two controllers. The feed-forward controller implements the on-line power computation scheme to compute the active power drawn by the load. It calculates the reference currents for the AF to supply the reactive and harmonic current required by the nonlinear load.

The feedback controller tracks the AF currents close to the reference currents. Tracking control is demonstrated by two methodologies - hysteresis control and sliding-mode control. The controller design and parameter selection is discussed.

3.2 Rectifier Control Unit

The rectifier control unit maintains the output DC current close to the current order I_{ref}. It consists of a PI controller that generates an alpha order or firing angle shift, appropriate to load requirements. The alpha order is fed to a Gate Firing Unit that generates firing pulses for each of the rectifier thyristors. The block diagram of the rectifier control unit is

shown in Fig. 3.1.

The current order I_{ref} is a step function. It is fed to an integrator-limiter to get a ramp-step signal. This prevents the DC current to shoot up at start, and provides a smooth initialization for the rectifier system. It is then compared with the measured output current I_{dc} to give an error signal I_{err}. The error signal is fed to a PI block that generates the firing angle order, α (alpha). The Gate Firing Unit (GFU) block takes the alpha order and synchronous bus voltages to generate firing pulses for the rectifier thyristors. Phase locked loop (PLL) filters were used to extract synchronous sinusoidal voltage signal V_{sync}, from the system AC bus voltage which suffers from high harmonic distortion, inherent in weak AC systems.

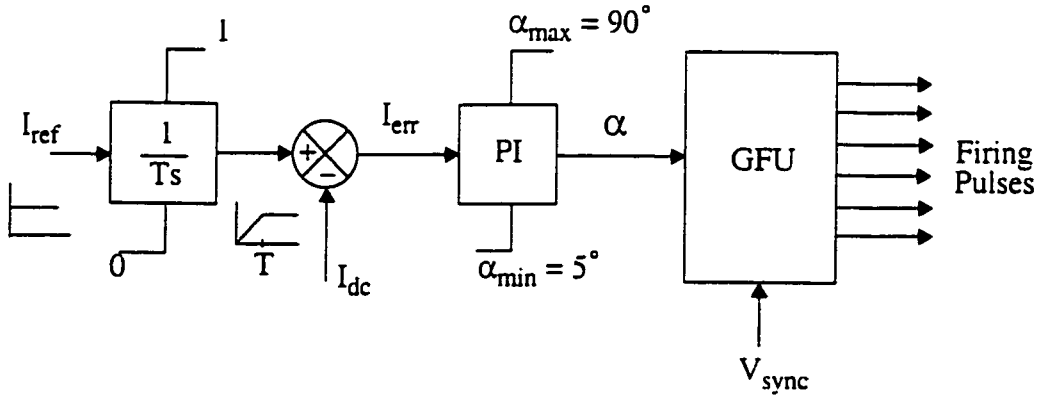


Fig. 3.1 Rectifier Control Unit

3.3 AF Control Unit

The system model including the active compensator is shown in Fig. 3.2.

The AF control unit controls the operation of the shunt active filter. It ensures that the AF, in steady state, provides all the harmonics and reactive current demand of the rec-

tifier load.

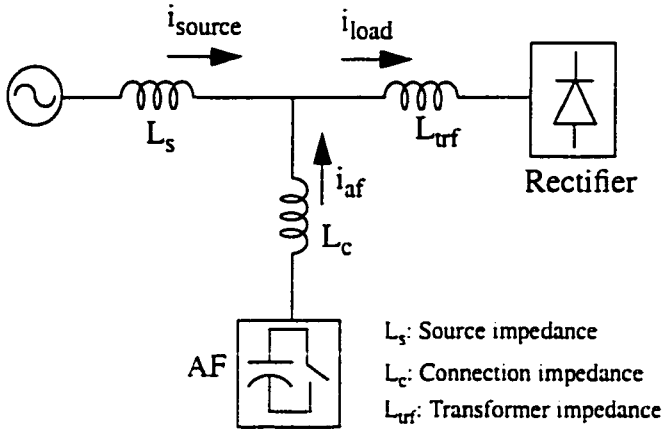


Fig 3.2 System model

The rectifier load current i_{load} can be expressed in fourier series as

$$i_{load} = \Sigma 4\frac{I_{dc}}{n\Pi}\sin\left(\frac{n\Pi}{2}\right)\sin\left(\frac{n\Pi}{3}\right)\sin(nw_0t)$$

$$n = 1,5,7...$$

where I_{dc} is the output DC current.

The fundamental harmonic of load current consists of an active and a reactive component. In steady state the AC source should supply only the active component of the load fundamental harmonic, and the reactive component and higher harmonics be supplied by the AF.

The AF control unit consists of a feed-forward and a feedback controller. The feed-forward controller implements the on-line power computation scheme. It measures AC bus voltages and line currents on-line and computes AF reference currents (i^*_f), which are fed to the feedback controller. The feedback controller (tracking control) ensures tracking of AF currents (i_f) about their reference values. The feedback loop is a faster control loop

and implements either hysteresis-based control or sliding-mode control. The block diagram of the AF control unit is shown in Fig. 3.3.

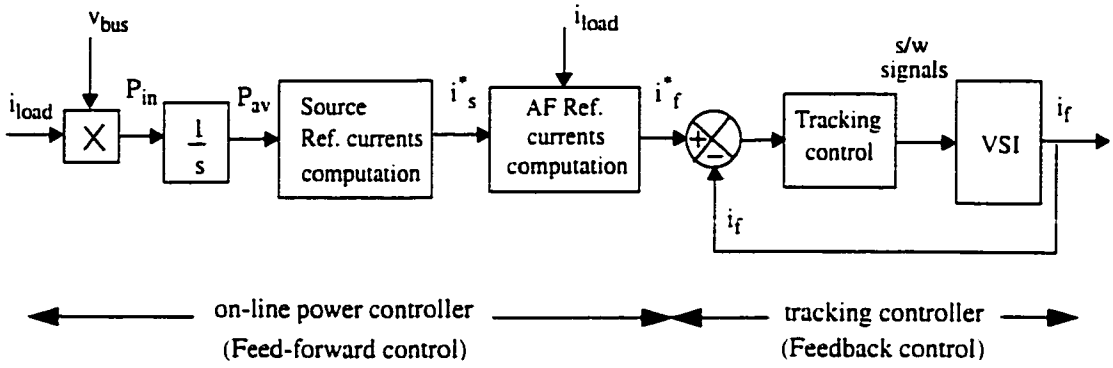


Fig. 3.3 AF control unit

3.3.1 On-line power computation scheme (Feed-forward Control)

The on-line power computation scheme is a feed-forward control that computes reference currents for the feedback controller by measuring AC line currents and bus voltages on-line. Fig 3.4 shows the schematic of the AF Control Unit: on-line power controller and tracking controller (segmented block).

The scheme computes on-line, the average power consumed by the load. The measured instantaneous bus phase voltages v_{busA}, v_{busB}, v_{busC} and line currents i_{La}, i_{Lb}, i_{Lc} are fed to a block that computes the instantaneous power p_{in} given by

$$p_{in} = v_{busA} * i_{La} + v_{busB} * i_{Lb} + v_{busC} * i_{Lc} \qquad (3.1)$$

Since it is a 3 phase, 6 pulse rectifier system, the instantaneous power is periodic at 6 times the line frequency. A clock cycle of 6 times the line frequency is taken to provide

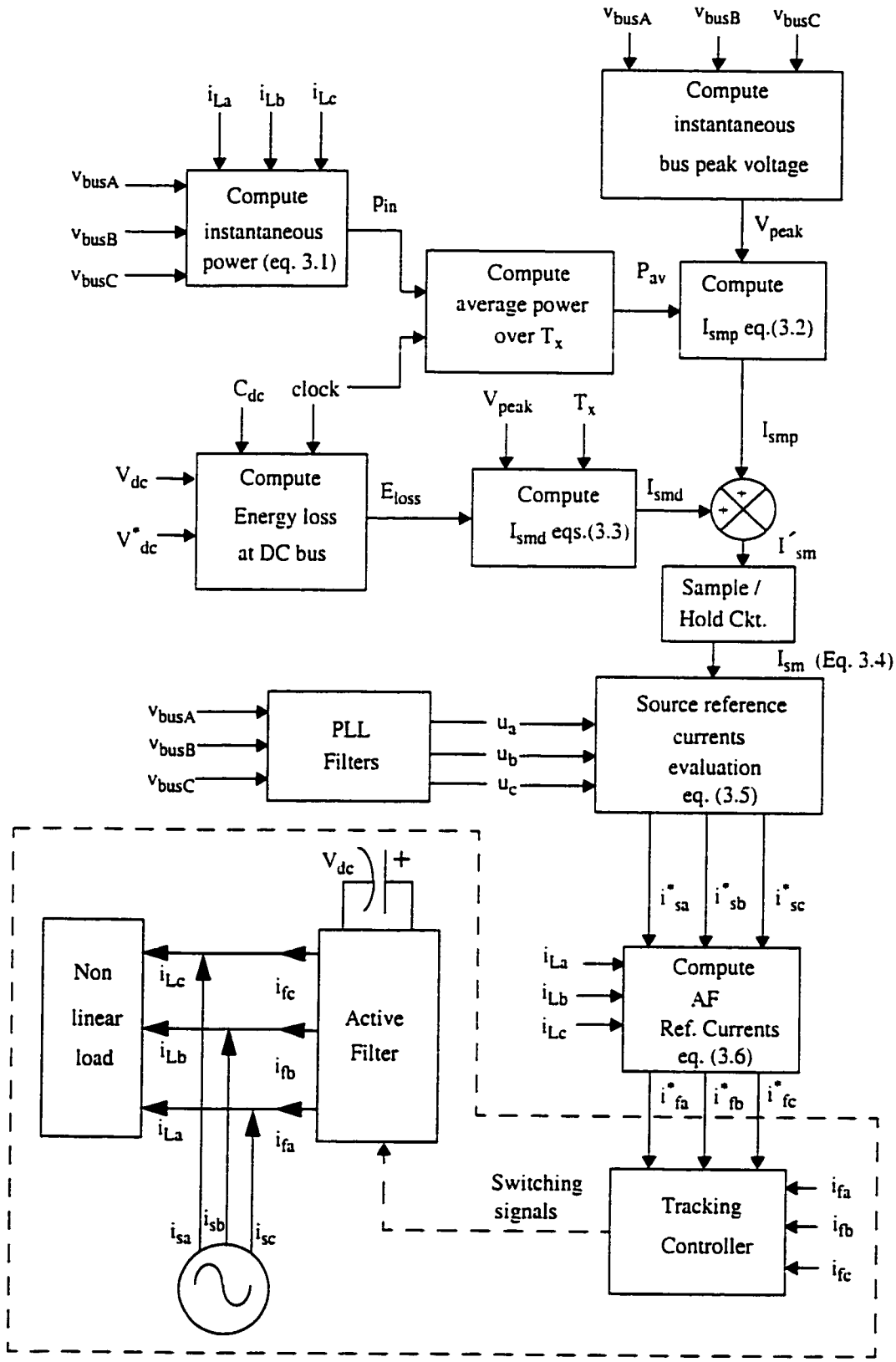


Fig 3.4 AF Control Unit Schematic

computational instants and timing reference for the scheme.

The instantaneous power is averaged over 1 clock period T_x. This average power P_{av} should be supplied by the AC source as a fundamental frequency current i_{smp} at unity power factor. Therefore the average power supplied can also be expressed as

$$P_{av} = 3/2 * V_{peak} * I_{smp} \tag{3.2}$$

where V_{peak} is the bus peak voltage and I_{smp} is the peak value of i_{smp}. The system measures the bus peak voltage, V_{peak}, at all instants as the bus voltage may fluctuate with load variations. Since the P_{av} has been computed over 1 clock cycle and the V_{peak} is measured on-line, the I_{smp} value can be calculated from eq. (3.2).

The AC source should also supply the losses occurring in the AF due to switching and conduction. A reference voltage V_{ref} is set for the DC bus, high enough to pump harmonics into the system bus (Appendix B1.3). The energy lost due to switching and conduction can be estimated by the voltage dropped across the DC bus capacitor, V_{dc}. The energy loss during one clock cycle is given by

$$E_{loss} = 1/2 * C_{dc} * (V_{ref}^2 - V_{dc}^2) \tag{3.3a}$$

This energy lost is replenished by the AC source which supplies an additional fundamental harmonic current i_{smd} at unity power factor to meet the AF losses. E_{loss} can also be expressed as

$$E_{loss} = 3/2 * V_{peak} * I_{smd} * T_x \tag{3.3b}$$

where I_{smd} is the peak value of i_{smd}.

Eqs. 3.3 a,b can be equated to yield I_{smd}.

The I_{smp}, I_{smd} values are sampled signals computed at each clock cycle.

The sampled peak value, I'_{sm} of total current supplied by the AC source is given by

$$I'_{sm} = I_{smp} + I_{smd} \tag{3.4}$$

The sampled peak value signal I'_{sm} is fed to a Sample/Hold circuit to generate a continuous peak value signal I_{sm}.

To generate sinusoidal waveforms for each of the source reference currents, unit amplitude sinusoidal template waveforms are required. It is further required that the source current should be at unity power factor, i.e. the nonlinear load should present a unity power factor sinusoidal load to the AC source. Phase locked loop (PLL) filters extract the fundamental harmonic component from the bus phase voltages to generate synchronous voltages (without any phase shift), which are further scaled to generate unit amplitude template waveforms u_a, u_b, u_c. The source reference currents i^*_{sa}, i^*_{sb}, i^*_{sc} are obtained by multiplying the template signals with the continuous peak source current I_{sm}.

$$\begin{aligned} i^*_{sa} &= I_{sm} * u_a \\ i^*_{sb} &= I_{sm} * u_b \\ i^*_{sc} &= I_{sm} * u_c \end{aligned} \tag{3.5}$$

The AF reference currents i^*_{fa}, i^*_{fb}, i^*_{fc} are generated by subtracting the source reference currents from the load line currents. (Note: The AF is considered as a harmonic source here).

$$\begin{aligned} i^*_{fa} &= i_{La} - i^*_{sa} \\ i^*_{fb} &= i_{Lb} - i^*_{sb} \\ i^*_{fc} &= i_{Lc} - i^*_{sc} \end{aligned} \tag{3.6}$$

As shown in the segmented block in Fig 3.4, the tracking controller compares the reference currents with the actual AF currents, and appropriate switching signals are generated for the inverter circuit to achieve close tracking of the reference values.

Validation of On-line Power Computation Scheme

Fig. 3.5 shows the simulation of the on-line power computation scheme. Plots (i)&(ii) show the three phase bus voltages and the AC load currents. A clock signal of 6 times the line frequency is chosen. Computation is performed at each clock pulse. The instantaneous power p_{in} oscillates at 6 times the line frequency. A high frequency ripple is observed along with characteristic 6^{th} harmonic of 6-pulse three-phase systems. This is due to distortion in the system bus voltage caused by high frequency switching currents injected by the active filter. The instantaneous power p_{in} is fed to a reset integrator that integrates it over one clock period to generate p_{out} and resets at the next clock pulse. The average power P_{av} is obtained by sampling the p_{out} signal at clock frequency. The peak source current components I_{smp} and I_{smd} are computed at the clock instants. The sampled peak source current (I_{smp}+I_{smd}) is fed to a sample-hold circuit to generate a continuous peak value, I_{sm}.

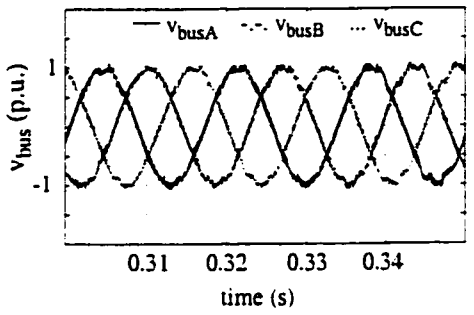
Synchronized voltage signals are obtained from the bus voltages by PLL filters and are further scaled to produce unit amplitude template voltages u_a, u_b, u_c. In the plot (ix), the signals u_a, u_b, u_c have been scaled by 50% to show that they lie in phase with the bus voltages and are free from distortion.

The unit template voltages are multiplied with the continuous peak source current I_{sm}, to generate sinusoidal source reference currents i^*_{sa}, i^*_{sb}, i^*_{sc} at unity power factor. The difference of source reference currents from load currents gives the active filter reference currents i^*_{fa}, i^*_{fb}, i^*_{fc}. It can be observed from plot (xii) that the active filter currents i_{fa}, i_{fb}, i_{fc} track the reference currents very closely.

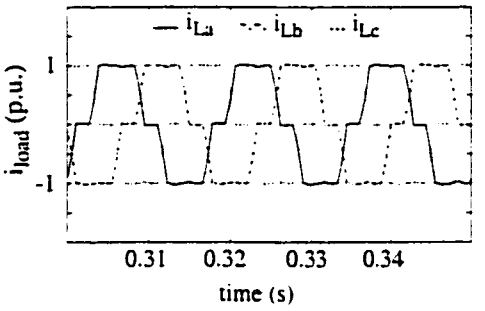
The source current, i_{sa} is sinusoidal at unity power factor with a high frequency

ripple superimposed due to switching errors. The high frequency ripple current is filtered by the AC high pass filter attached at the AC bus, and a harmonic free sinusoidal current flows in the source phase.

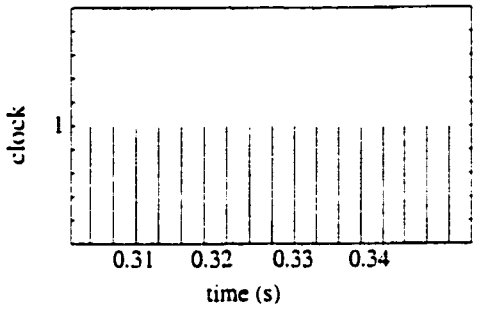
At steady state the DC bus voltage maintains itself at a constant level, consistent with the voltage difference necessary to replenish the losses incurred by the DC capacitor during switching and conduction. During transient conditions the DC bus voltage may exceed or go below the reference voltage, as per the energy transaction between the active filter and the load.



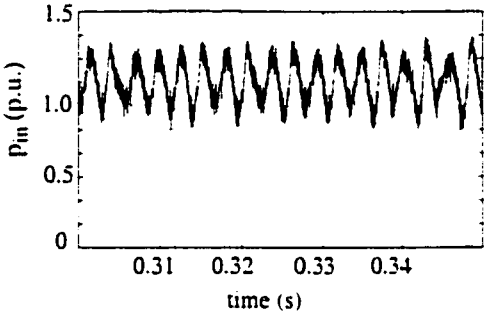
(i) AC Bus Voltages



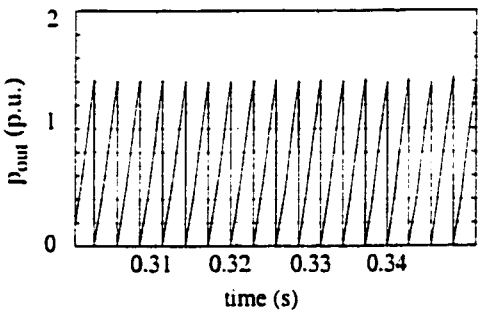
(ii) AC load currents



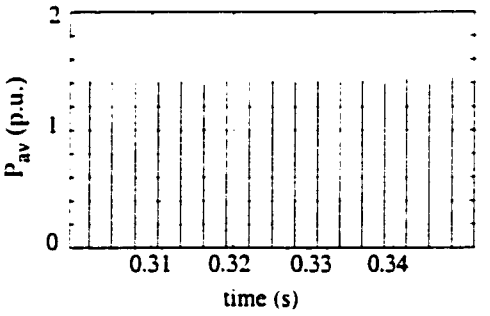
(iii) clock cycle



(iv) Instantaneous power

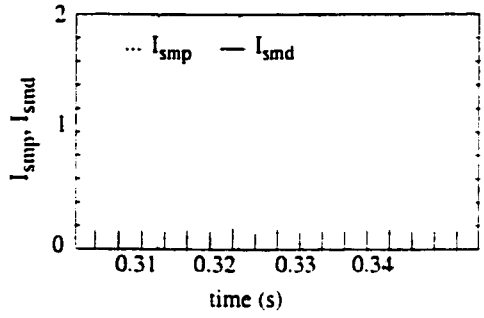


(v) Integrated power

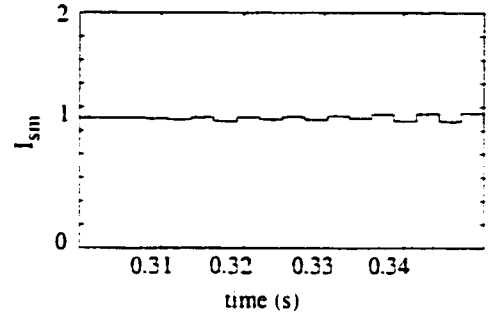


(vi) Average power

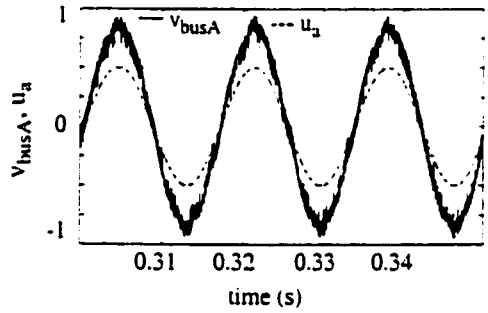
Fig 3.5 Simulation of On-line Power Computation Scheme



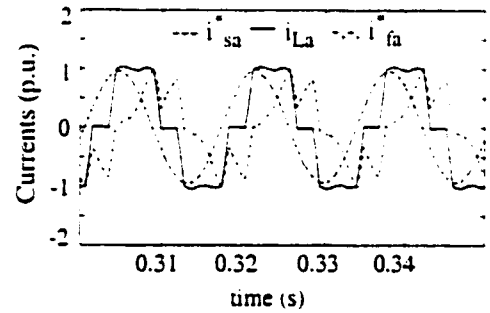
(vii) Peak source current components I_{smp}, I_{smd}



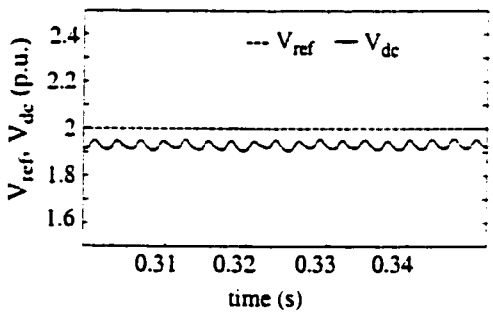
(viii) Peak source current



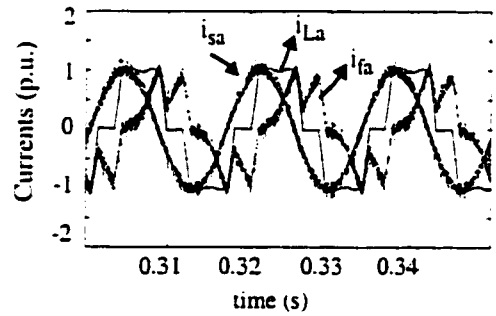
(ix) v_{busA}, u_a



(x) i^*_{sa}, i_{La}, i^*_{fa}



(xi) V_{ref}, V_{dc}



(xii) i_{sa}, i_{La}, i_{fa}

Fig 3.5 *contd.* Simulation of On-line Power Computation Scheme

3.3.2 Tracking Control (Feedback control)

The tracking control is a feedback control that compares the actual AF currents with the reference currents and generates switching signals for the AF to regulate them. The switching signal generation depends on the control law implemented. Two control laws have been tested.

(a) Hysteresis control

(b) Sliding-mode control

3.3.2.1 Hysteresis control

In this control technique, a tolerance or hysteresis band is drawn about the reference current, and the AF current is restricted within the band. The hysteresis bandwidth, hb, chosen corresponds to the ripple allowed in the AF current. Switching functions U_a, U_b, U_c are generated for each of the phases independently.

The switching function is a bipolar function (1 or -1) and changes state as the AF current reaches the upper or lower hysteresis band limits.

The switching logic for phase a is as follows:

(i) $i_{fa} < (i^*_{fa} - hb/2)$ $\quad (U_a = +1)$ (3.7a)

i.e. when the AF current reaches the lower band limit, the inverter supplies less current than required. The upper s/w goes ON and lower switch goes OFF, connecting the DC bus capacitor to the AC bus. The DC bus maintained at higher voltage is able to boost the phase current, thus causing it to rise. The switching function becomes unity ($U_a = +1$).

(ii) $i_{fa} > (i^*_{fa} + hb/2)$ $(U_a = -1)$ (3.7b)

i.e. when the AF current exceeds the upper band limit, the inverter supplies more current than required. The upper s/w goes OFF and lower s/w goes ON, removing the DC bus capacitor from the phase circuit. The switching function reverses sign ($U_a = -1$). As the DC source is removed from the phase, the current begins to fall.

Thus, the hysteresis controller is able to regulate the rise and fall of AF currents within tolerance limits about the reference currents, by appropriately switching the inverter legs.

The implementation of hysteresis control is shown as a block diagram in Fig. 3.6. A hysteresis band of width hb is drawn about the reference current i^*_{fa}. A detection circuit checks when the AF current exceeds band-limits. The setA signal goes high when the AF current becomes equal to or less than the lower band limit ($i^*_{fa} - hb/2$). The resetA signal goes high when the AF current exceeds the upper band limit ($i^*_{fa} + hb/2$). The setA and resetA signals are fed to a flip-flop circuit, that gives out the switching function U_a.

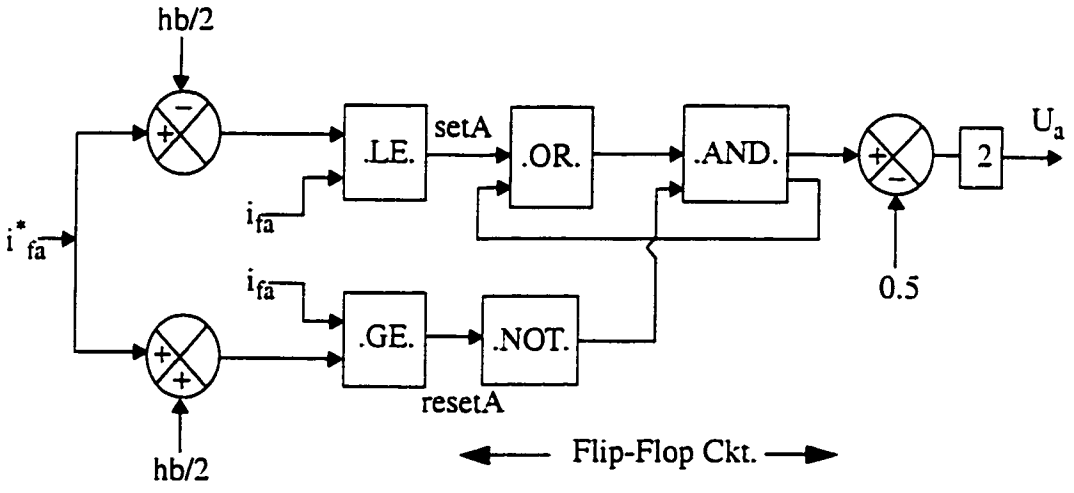


Fig 3.6 Hysteresis controller implementation

The switching functions U_b and U_c for phases b and c are determined similarly, using the corresponding reference and measured currents and the hysteresis band hb.

Fig. 3.7 shows the hysteresis control tracking of reference current i^*_{fa} within the hysteresis band.

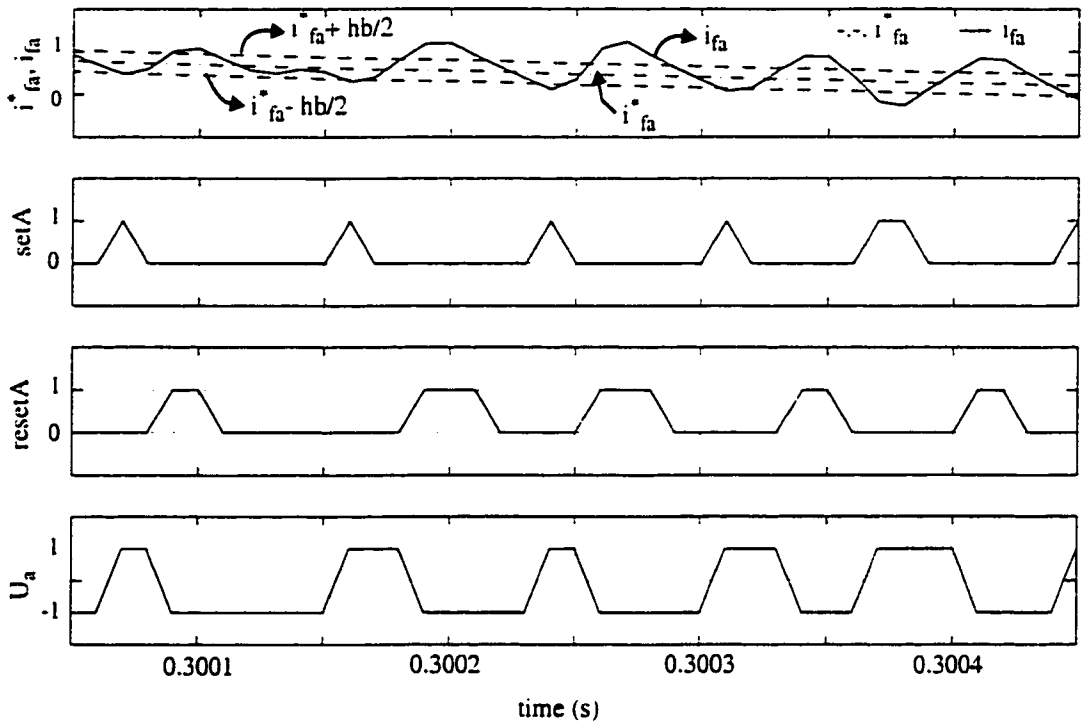


Fig 3.7 Simulation of Hysteresis Controller

The inverter switching frequency depends on the frequency at which the AF current hits the hysteresis band limits. This frequency is variable in nature as the variation of current within the hysteresis band is dependent on circuit parameters. The waveshaping of current within the band limits depends upon the hysteresis band width, the connection inductance and the DC bus voltage of the AF inverter. The circuit and control parameters have to be chosen such that the switching frequency doesn't exceed the limit imposed by semiconductor switches, but is high enough to provide good modulation of reference cur-

rents.

The maximum switching frequency attained by the inverter can be estimated by the relationship (Appendix B1.5):

$$f_{max} = \frac{V_{dc}}{(2L_c \cdot hb)} \qquad (3.8)$$

This relationship is derived for the maximum switching frequency, but since for the hysteresis control technique the switching frequency is variable, the above expression can be approximated for the average switching frequency. From the above relationship, it may be observed that the average switching frequency f_{av} depends on the following factors:

(i) Hysteresis bandwidth, hb

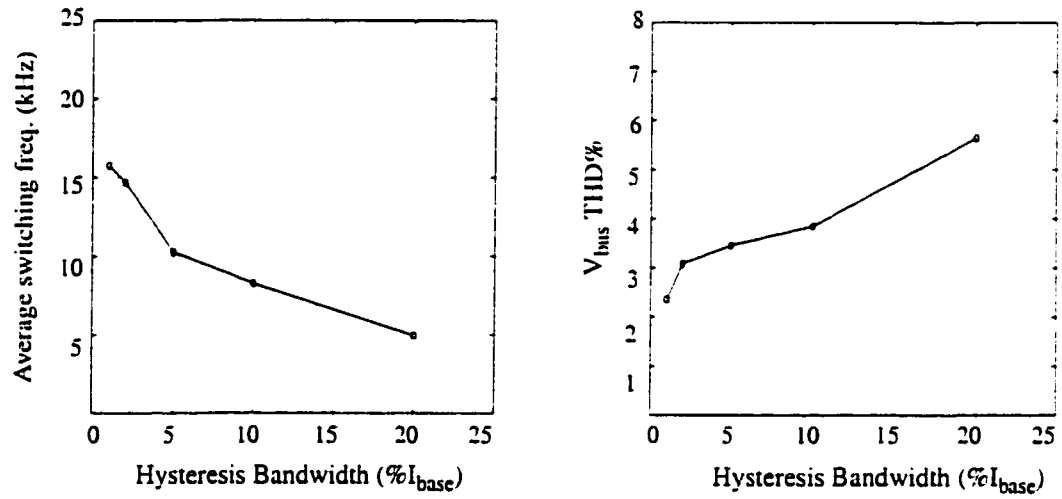
The hysteresis bandwidth corresponds to the ripple allowed in the AF current. Keeping other factors constant, an increase in the bandwidth causes the AF current to hit the tolerance limits less frequently, thus reducing the switching frequency. Whereas a decrease in the bandwidth causes the AF current to hit the tolerance limits more often thus increasing the inverter switching frequency. In terms of performance, a smaller hysteresis bandwidth causes the AF current to track the reference current more closely. The magnitude of switching error currents introduced at the system bus reduces, the switching frequency shifts to higher ranges thus improving the THD of system bus voltage.

Table 3.1 and Fig. 3.8 show the effect of variation of hysteresis bandwidth on the inverter switching frequency and the THD of bus voltage.

It can be observed that the average switching frequency decreases and the V_{bus} THD deteriorates with increasing bandwidth. Fig 3.9 shows simulation results for different values of hysteresis bandwidths chosen.

Table 3.1: Variation of Hysteresis Bandwidth, hb

Hysteresis Bandwidth hb (% I_{base})	Avg. Switching Frequency (kHz)	V_{bus} THD%
1%	15.75	2.36
2%	14.65	3.09
5%	10.25	3.46
10%	8.25	3.85
20%	4.95	5.65

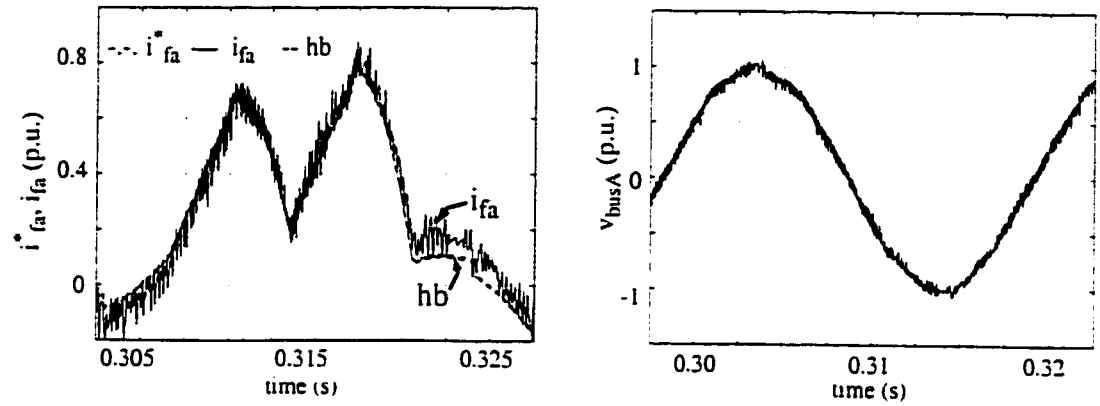


(i) f_{av} vs. hb

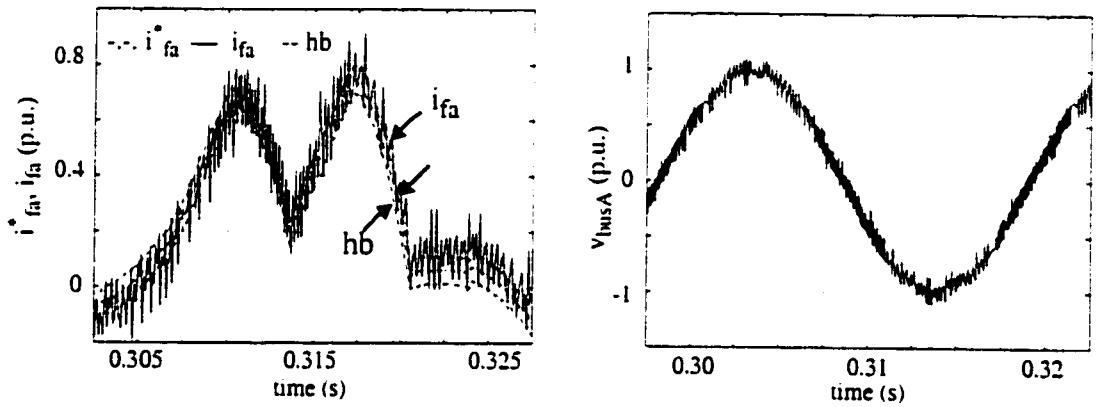
(ii) v_{bus} THD% vs. hb

Fig. 3.8 Variation of Hysteresis Bandwidth

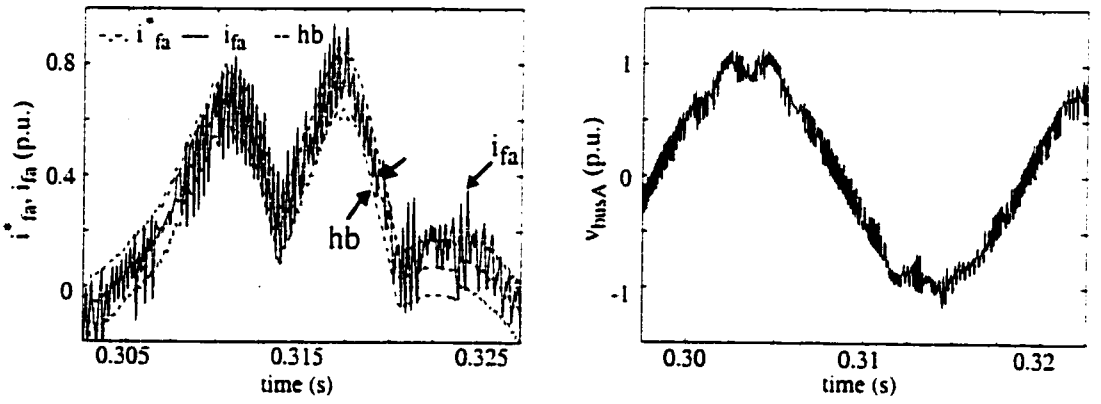
It is noted that the AF performance and switching frequency is very sensitive to the hysteresis bandwidth.



(i) hb = 1% I_{base}



(ii) hb = 10% I_{base}



(iii) hb = 20% I_{base}

Fig 3.9 Effect of variation of Hysteresis bandwidth, hb

(ii) Connection impedance inductance, L_c

The connection impedance plays an important role in shaping the AF current within the hysteresis band. A large value of inductance, decreases the rate of change of current within the tolerance band, thus reducing the switching frequency. Whereas a smaller value of L_c would allow more frequent changes in the AF current, thus increasing the switching frequency.

Table 3.2 and Fig 3.10 show the effect of variation of connection inductance on the switching frequency and the THD of bus voltage. It may be observed from Fig. 3.10 (i) that the switching frequency decreases with an increase in L_c. This can be naturally expected, since an increase in L_c reduces the rate of change of AF current within the hysteresis band.

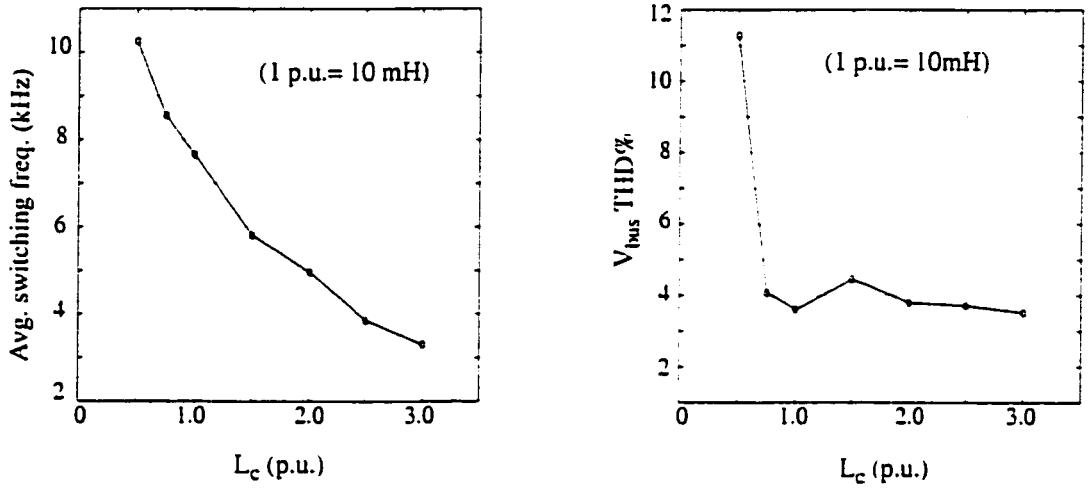
An increase in the inverter switching frequency does not necessarily indicate better performance in terms of THD. At a high switching frequency of 10.25 kHz, the THD is unexpectedly high. This is so because the L_c value is very low, and the low impedance is unable to contain the AF current within the hysteresis band, inspite of corrective action taken by the tracking controller. As a result the switching error currents, although shifted to high frequencies, have greater magnitude and produce larger distortion at the system bus.

Table 3.2: Variation of Connection inductance, L_c

Connection Inductance L_c (1p.u=10mH)	**Avg. Switching Freq.(kHz)**	**V_{bus} THD%**
0.5	10.25	10.28
0.75	8.55	3.07
1.0	7.65	2.6
1.5	5.80	3.45
2.0	4.95	2.79

Table 3.2: Variation of Connection inductance, L_c

Connection Inductance L_c (1p.u=10mH)	Avg. Switching Freq.(kHz)	V_{bus} THD%
2.5	3.85	2.71
3.0	3.30	2.52



(i) L_c vs. switching freq. f_{av}

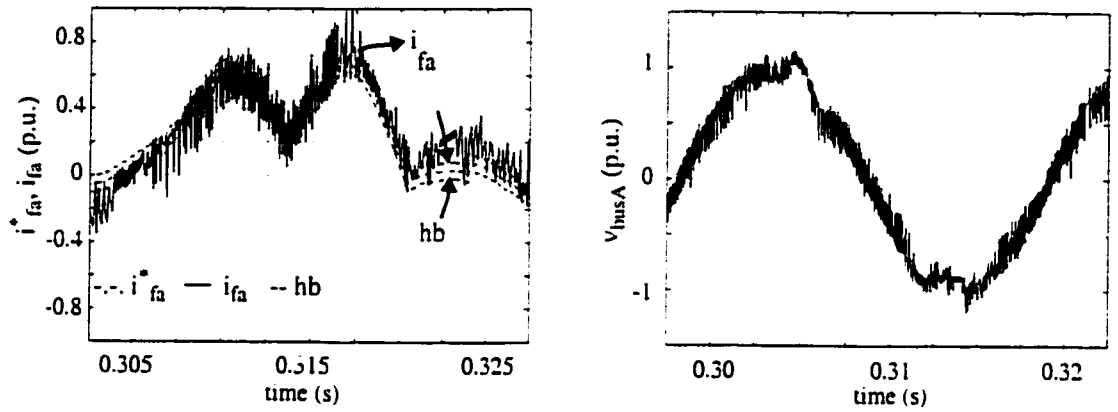
(ii) L_c vs. V_{bus} THD%

Fig. 3.10 Variation of L_c

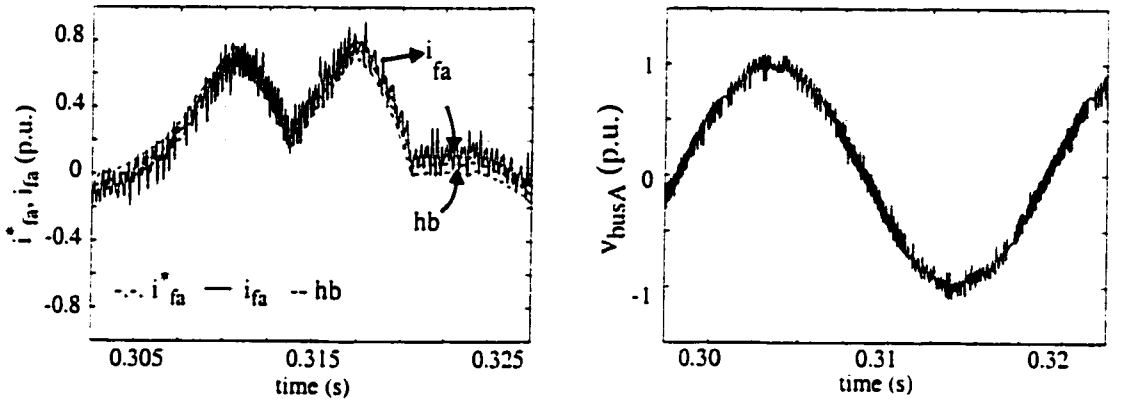
Fig 3.11 shows the modulation of AF current within hysteresis band for different values of L_c.

Ideally it may be expected that a higher switching frequency would shift the switching error components to higher frequencies improving the THD. But simulation results show that THD remains more or less constant. At a low value of L_c, the switching frequency is high, but the magnitude of switching error currents is higher. Therefore the THD in this case is contributed by higher frequency switching error currents of larger magnitude. At a higher value of L_c, the switching frequency is low. The THD is contrib-

uted by lower order switching error currents with smaller magnitude, keeping it almost constant for L_c values greater than 0.75 p.u.

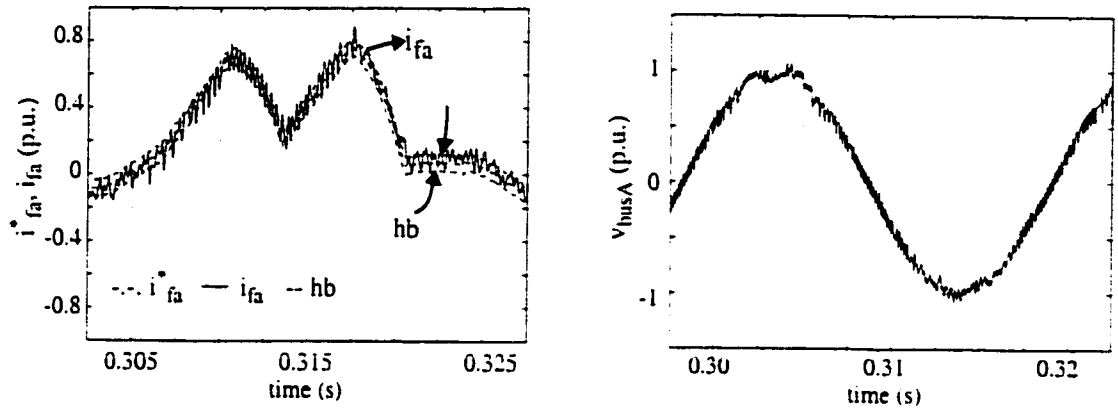


(i) $L_c = 0.5$ p.u.



(ii) $L_c = 1.0$ p.u.

Fig 3.11 Effect of variation of L_c



(iii) L_c = 2.0 p.u.

Fig 3.11 *contd.* Effect of variation of L_c

(iii) DC bus capacitor voltage V_{dc}

The DC bus voltage V_{dc}, must be maintained at a minimum level, so as to have sufficient power to modulate AF currents about their reference values. For independent phase control, the DC bus voltage must be minimum 2 times the system AC bus peak voltage (Appendix B1.3). A voltage level higher than the minimum level gives the DC capacitor higher energy to modulate the AF current, thus increasing the switching frequency. Table 3.3 and Fig 3.12 show the effect of variation of V_{dc} on the average switching frequency and the V_{bus} ripple voltage.

An increase in the DC bus voltage increases the rate of change of current, thus increasing the switching frequency (Fig. 3.12 i). The V_{bus} THD is not a correct measure for performance in this case. This is so because an increase in V_{dc} leads to an increase of I_{smd} component (Eqns. 3.3 a,b) of source current and a greater voltage drop across source

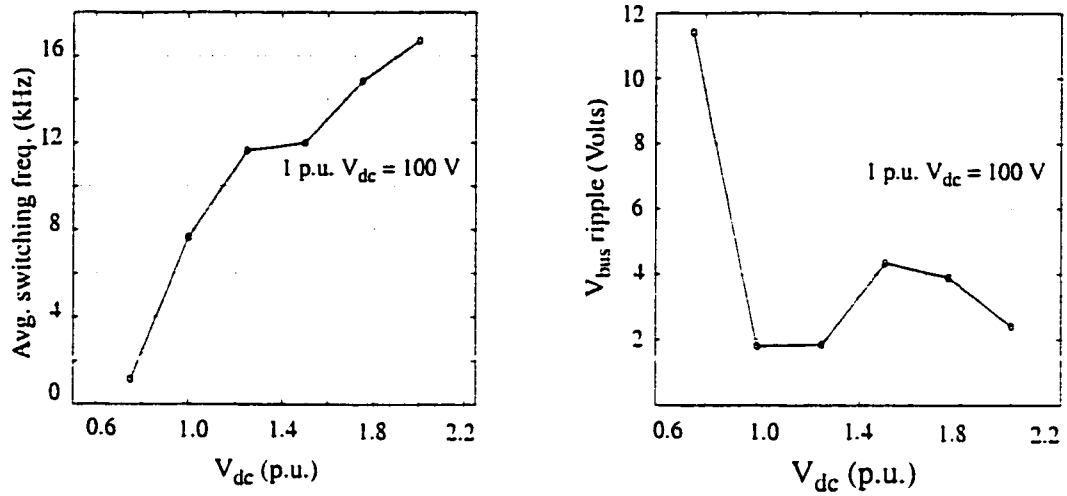
impedance. The bus fundamental voltage component gets reduced and although the ripple voltage reduces with the increase in V_{dc}, the THD shows an increase. The bus ripple voltage reflects the AF performance in this case. Fig 3.13 shows the modulation of AF current for different V_{dc} values.

It may be observed (Fig 3.13 i) that at a voltage level of 1.5 p.u. (lower than the minimum level of 2.0 p.u.), the AF reference current departs from its usual waveform, as the distortion at AC bus is high. The AF modulates its currents about their reference values only when the DC bus voltage exceeds the AC bus voltage. At other instants it falls out of tracking, leading to higher switching error currents and higher THD at system bus voltage.

The V_{bus} ripple voltage shows a general decline with an increase in V_{dc}, but for higher values of V_{dc} (beyond 1.4 p.u.), the DC bus has higher energy to modulate the AF current, and the high rate of di/dt causes the AF currents to exceed the hysteresis bandlimits. This leads to greater switching error currents and higher ripple in V_{bus}.

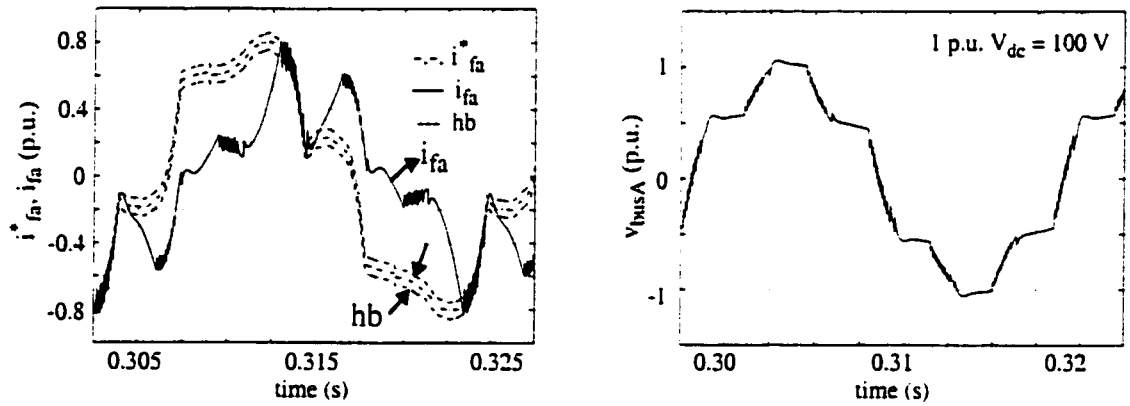
Table 3.3: Variation of DC bus voltage, V_{dc}

V_{dc} (p.u.) (1 p.u.=100 V)	Avg. Switching Freq. (kHz)	V_{bus} THD%	RMS V_{bus} ripple (Volts)	RMS V_{bus} fundamental (Volts)
1.5	1.15	16.6	11.41	68.74
2.0	7.65	2.61	1.81	69.82
2.5	11.65	2.67	1.85	69.02
3.0	12.0	6.40	4.34	67.85
3.5	14.85	5.91	3.89	65.88
4.0	16.7	3.83	2.41	62.86



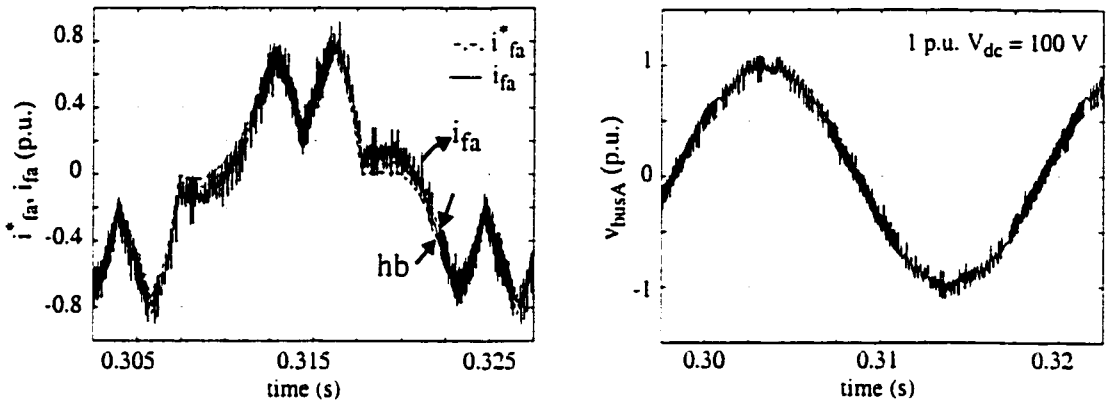
(i) f_{av} vs. V_{dc} (ii) v_{bus} ripple vs. V_{dc}

Fig 3.12 Variation of V_{dc}

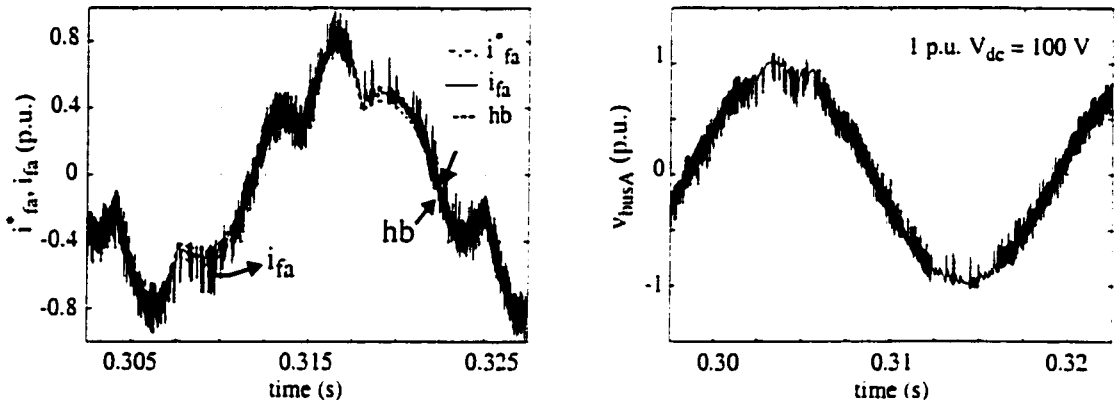


(i) V_{dc} = 1.5 p.u.

Fig 3.13 Effect of variation of V_{dc}



(ii) V_{dc} = 2.0 p.u.



(iii) V_{dc} = 3.0 p.u.

Fig 3.13 *contd.* Effect of variation of V_{dc}

AF Design (Calculations in Appendix):

Keeping with the restriction imposed by the semiconductor switches on inverter switching frequency, a judicious selection of parameters has to be made so as to limit the

switching frequency below the maximum limit and to have good performance in terms of low THD at the system bus voltage.

The active filter provides compensation for a 1 p.u. output DC current load. For this load requirement, IGBT switches would be adequate. The simulation model assumes an ideal switch, but considers the switching frequency restraint imposed by a real switch. For high power application, GTO switches would be chosen, and the AF design would be according to their switching frequency constraints.

(i) Hysteresis bandwidth, hb: To have a good replication of reference currents, the hysteresis bandwidth was chosen at 10% of I_{base} i.e. 0.1A. From simulation studies (Fig. 3.9 i&ii), a hysteresis bandwidth of 10% I_{base}, kept the switching frequency below 10 kHz, and the THD less than 4%.

(ii) DC bus capacitor voltage, V_{dc}: Since the system AC bus voltage is 100V(peak), the DC bus voltage was taken at 200V. A higher voltage value would further increase the switching frequency, and also increase switching losses. Thus the DC bus voltage reference was set at the minimum value.

(iii) Connection inductance, L_c: Substituting the V_{dc} and hb values in eq.(3.7) and taking the maximum switching frequency for the inverter at 80 kHz, the value of L_c obtained is 12.5 mH. As shown in Fig.3.10 (ii), the THD remains practically constant for a range of L_c, unless it is a very low value. Simulations for the circuit show that the L_c value at 10 mH provided good modulation conforming with the switching frequency restraint, and acceptable THD.

(iv) DC bus capacitor, C_{dc}: The DC bus capacitor should be large enough to store enough energy to supply the total power required by the load, for short duration failures at the system AC bus. The capacitor was selected at 200uF, so as to meet load requirements, during 1 cycle faults at AC bus. A higher value of C_{dc}, improves the DC bus voltage ripple, but

adds to the cost.

3.3.2.2 Sliding-Mode Control

This control technique is based on the concept of Variable Structure Systems (VSS) [7,15]. Variable structure systems consist of a set of continuous subsystems with proper switching logic. The control actions are discontinuous functions of system state and reference inputs. The switching inverter used as an active filter is a natural variable structure system because its topology changes from one continuous state to another with the switching action.

For a given circuit, a state vector, usually a set of voltages or currents to be controlled, is defined. The objective of the technique is to derive a control law for the switching function to maintain the system state on a desired trajectory or sliding surface.

A switched circuit topology imposes natural restraint on the switching function. For the inverter circuit, the switches may be in open or closed state. The switching function is thus bipolar and is expressed as

$U_x = +1$ (Upper switch of leg x closed, lower switch open)

$U_x = -1$ (Lower switch of leg x closed, upper switch open)

The continuous control concept is used to derive the equivalent switching function U_{eq} (Appendix B2).

The equivalent switching function for phase x is given by

$$U_{eqx} = \left(\dot{i}_{cx} + \frac{e_{xn}}{L_c}\right) \times \frac{2L_c}{V_{dc}} \qquad (3.9)$$

For the state to remain on the sliding surface, the circuit parameters L_c, V_{dc} must be chosen such that the equivalent control doesn't exceed the natural bounds of the system, i.e.

$$-1 \leq U_{eqx} \leq 1$$

The sliding mode control theory is used to derive the discontinuous control law for the switching function U_x.

The switching logic states that,

$$\text{(i) if } (i_{fx} < i^*_{fx}), \text{ then } U_x = +1 \qquad (3.10)$$

$$\text{(ii) if } (i_{fx} > i^*_{fx}), \text{ then } U_x = -1$$

To provide current tracking, a constant decision frequency control is used. At a regular time interval, the system state is checked and the switching logic applied.

The block diagram implementation of the sliding mode controller (for phase A) is shown in Fig. 3.14. The measured AF current and reference current are sampled at the decision frequency, CLK and compared by the detection circuit. The setA signal goes high if i_{fa} is less than the reference current i^*_{fa}. The resetA signal indicates the change in state of the switching function. It goes high if i_{fa} exceeds i^*_{fa}. The setA and resetA signals are fed to a flip-flop circuit that outputs the switching function U_a.

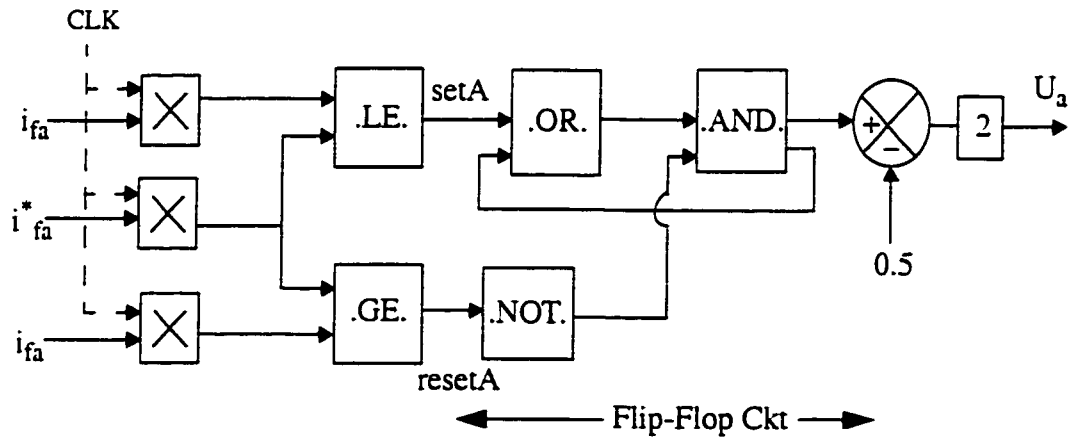


Fig 3.14 Sliding-Mode Controller implementation

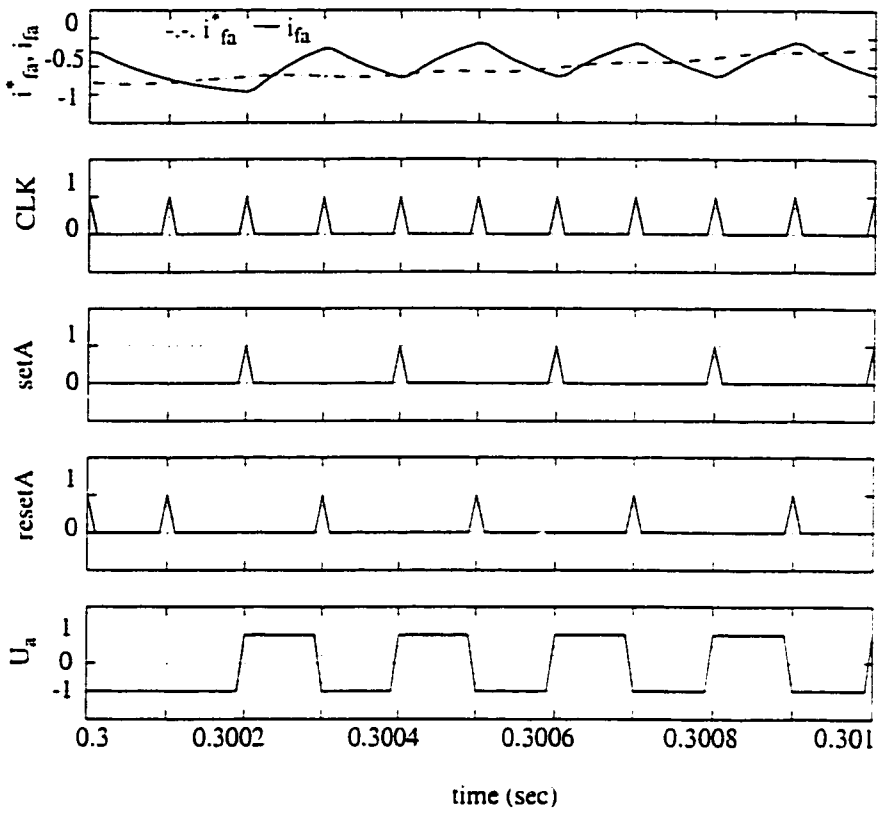


Fig 3.15 Simulation of Sliding-Mode controller

Fig. 3.15 shows the simulation of sliding mode controller. A decision clock signal of frequency 10 kHz is used. The AF line currents and the reference values are compared at the decision clock instants and the switching logic is applied to generate the switching function U_a.

The resulting switching frequency is less than or equal to one half of the decision frequency, and therefore the decision rate can be fixed on the basis of switching frequency limit of semiconductor switches. The switching frequency components of the AF current would be spread over a wider range of frequencies since the actual switching is not performed at a constant rate.

It is observed from the expression for U_{eq} (Eq. 3.9), that the equivalent switching

function is proportional to the ratio of inverter line inductance to bus voltage. Therefore as this ratio increases, the U_{eq} will increase in magnitude until some point where it will exceed the natural bounds of the circuit, and tracking error will begin to occur.

On the other hand, peak to peak ripple, Δi of the AF current during one switching period is inversely proportional to the same ratio L_c/V_{dc} (Eqn. 3.11 & Appendix B2.12). Therefore at a given decision frequency, a trade off has to be made to keep the switching function within the natural bounds of the circuit and to keep the ripple magnitude at an acceptable level.

$$\Delta i = i^*_{fx} + \int_0^T \frac{e_{xn}}{L_c} - u_x \times V_c / (2L_c) dt \qquad (3.11)$$

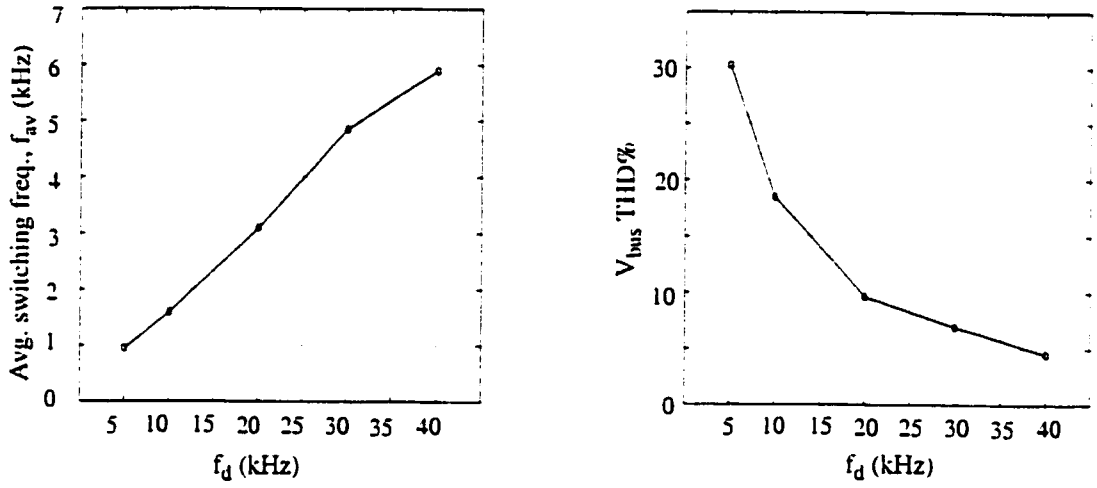
The performance of the AF is measured in terms of the THD of the source currents or bus voltages. The performance of the sliding mode controller depends on the choice of the decision frequency, the connection impedance and the DC bus voltage. The effect of each of these factors is discussed below:

(i) Decision frequency (f_d)

An increase in the decision frequency, reduces the distortion due to switching ripple, as the effective switching frequency increases, thereby reducing peak to peak ripple in the AF current. The limiting factor to the increase in decision frequency would be the allowable losses in the power circuit. The effect of varying decision frequency is studied by keeping the V_{dc} and L_c fixed. Table 3.4 and Fig. 3.16 show the effect of variation of the decision frequency on the switching frequency and the bus voltage THD.

Table 3.4: Variation of decision frequency f_d

Decision frequency, f_d (kHz)	Average Switching frequency f_{av} (kHz)	V_{bus} THD%
5	0.95	30.23
10	1.60	18.44
20	3.10	9.61
30	4.85	6.93
40	5.90	4.52

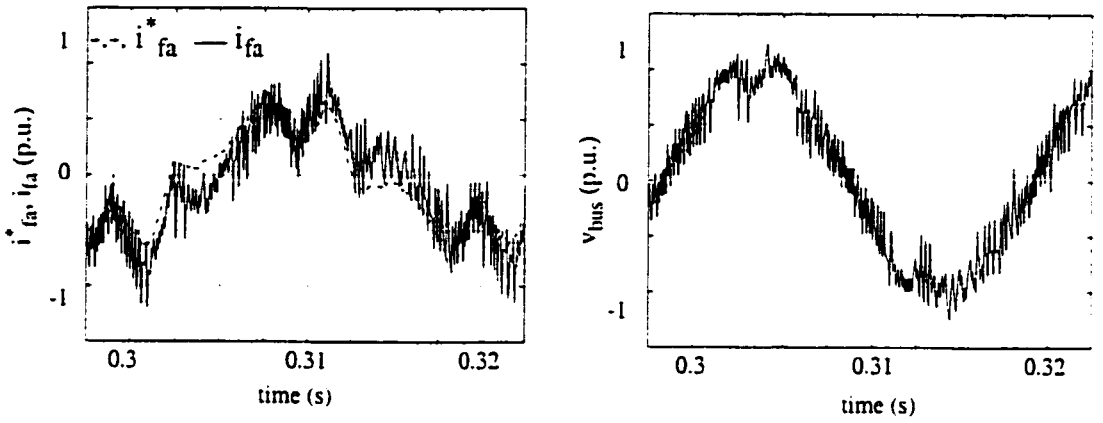


(i) f_{av} vs. f_d (ii) V_{bus} THD% vs. f_d

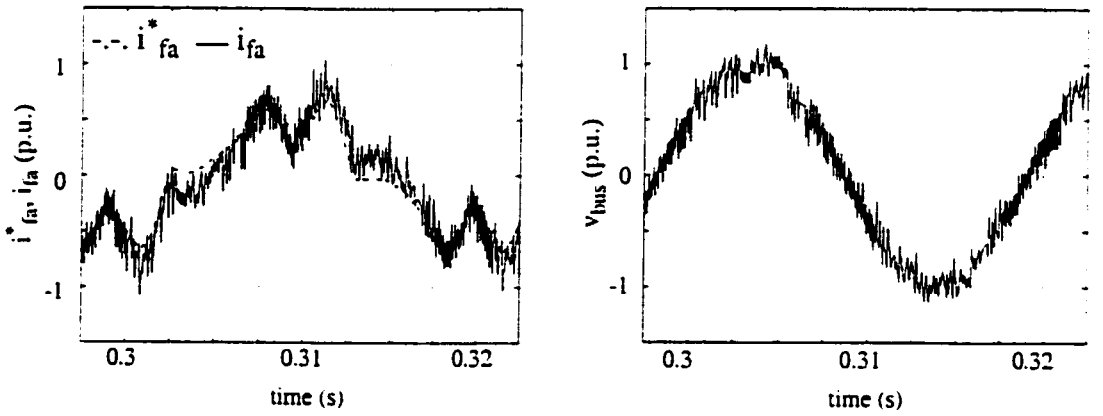
Fig 3.16 Variation of decision frequency

The inverter maximum frequency always remains at less than half of the decision frequency, and this criteria helps in making a choice of optimum decision frequency for the inverter switches selected. The V_{bus} THD improves with the increase in decision fre-

quency as the switching error currents shift to higher frequencies with lower magnitudes. Fig 3.17 shows simulation results in this context.

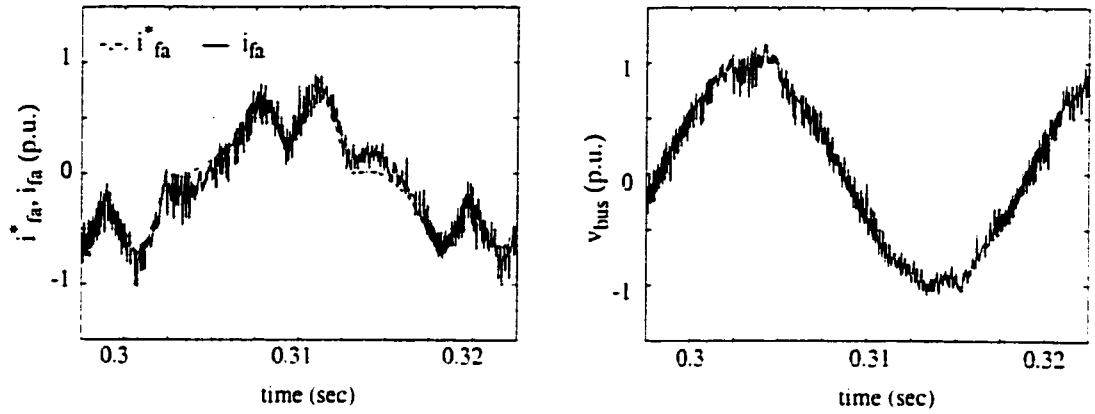


(i) $f_d = 20$ kHz



(ii) $f_d = 30$ kHz

Fig 3.17 Effect of variation of decision frequency



(iii) f_d = 40 kHz

Fig 3.17 *contd.* Effect of variation of decision frequency

(ii) Connection inductance L_c

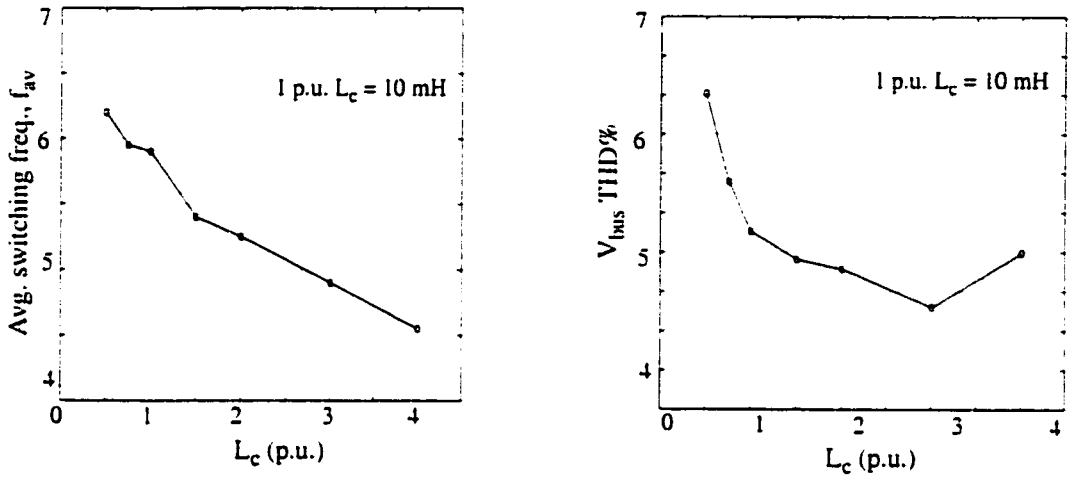
The choice of L_c does not affect the maximum switching frequency of the inverter, which is set by the decision frequency of the controller. The chosen value of L_c controls the rate of change of current between two decision instants. Since the decision interval is fixed, the wave-shaping of current and hence the switching error ripple of AF is influenced by L_c. An increase in the value of L_c, reduces the rate of change of current, lowering the switching frequency.

Table 3.5: Variation of Connection inductance L_c

L_c(p.u.)	f_{av} (kHz)	THD%
0.5	6.20	8.04
0.75	5.95	5.79
1.0	5.90	4.52
1.5	5.40	3.81
2.0	5.25	3.57

Table 3.5: Variation of Connection inductance L_c

L_c(p.u.)	f_{av} (kHz)	THD%
3.0	4.90	2.60
4.0	4.55	3.98

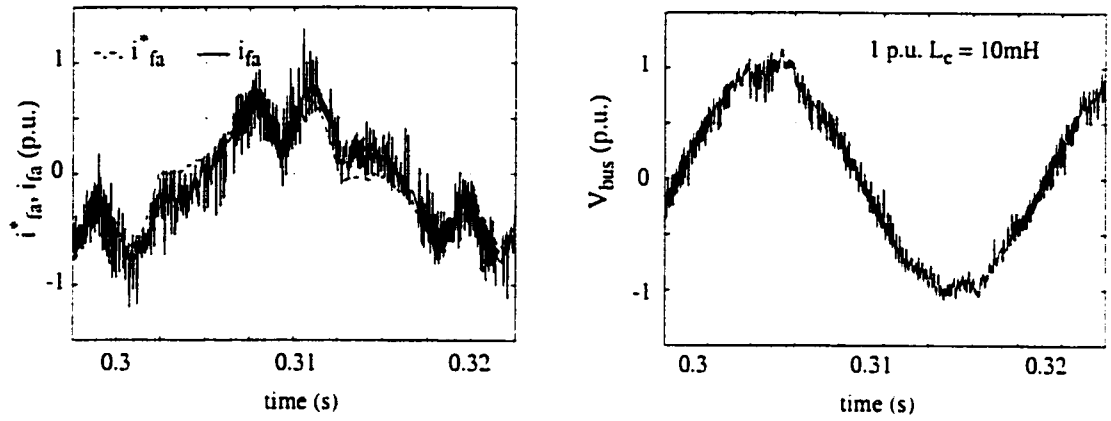


(i) f_{av} vs. L_c (ii) f_{av} vs. L_c

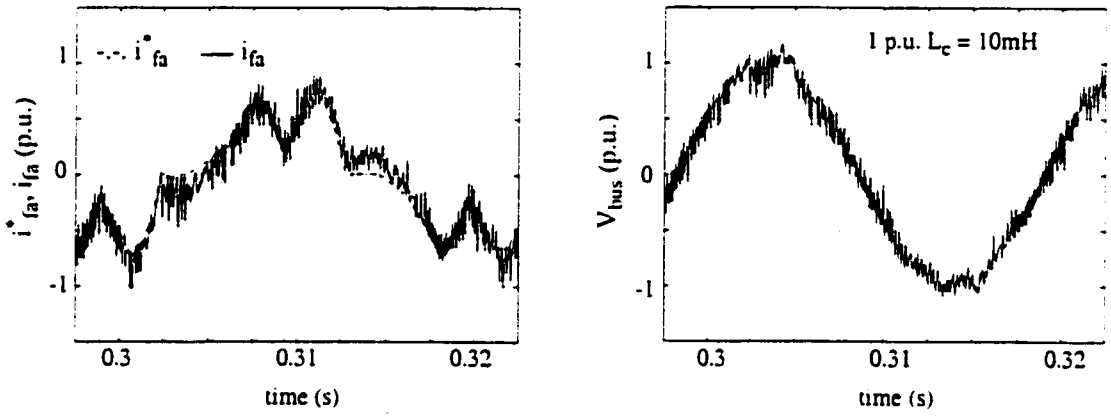
Fig 3.18 Variation with L_c

Table 3.5 and Fig. 3.18 show the effect of variation of L_c on the average switching frequency and the bus voltage THD.

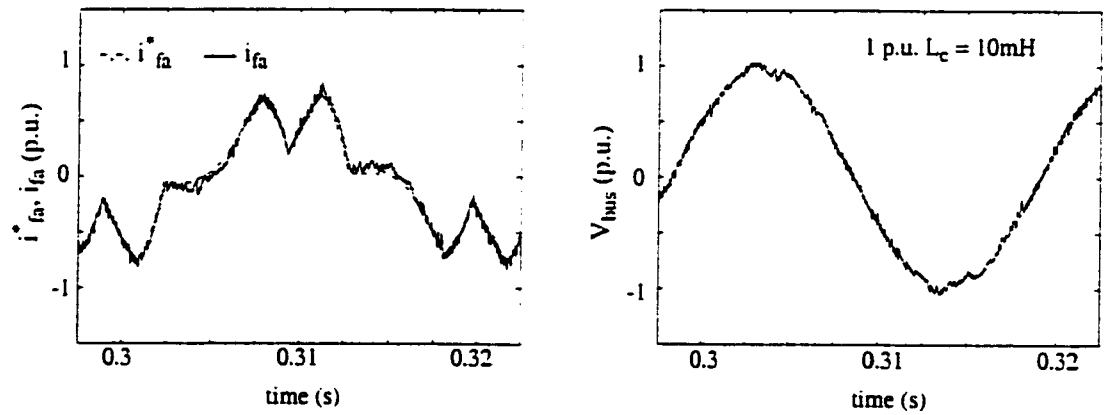
It may be observed from Fig 3.18(i) that the average switching frequency reduces steadily with an increase in L_c value. As the value of L_c increases the switching error ripple reduces and the V_{bus} THD improves. At higher values of L_c, the THD begins to deteriorate. This is so because a stage is reached when the L_c value causes the equivalent switching function, U_{eq} to exceed the natural limits of the circuit. Tracking error begins to occur, worsening the V_{bus} THD. Fig 3.19 shows simulation results for the different values of L_c.



(i) L_c = 0.5 p.u.



(ii) L_c = 1.0 p.u.



(iii) L_c = 3.0 p.u.

Fig 3.19 Effect of variation of L_c

(iii) DC bus voltage V_{dc}

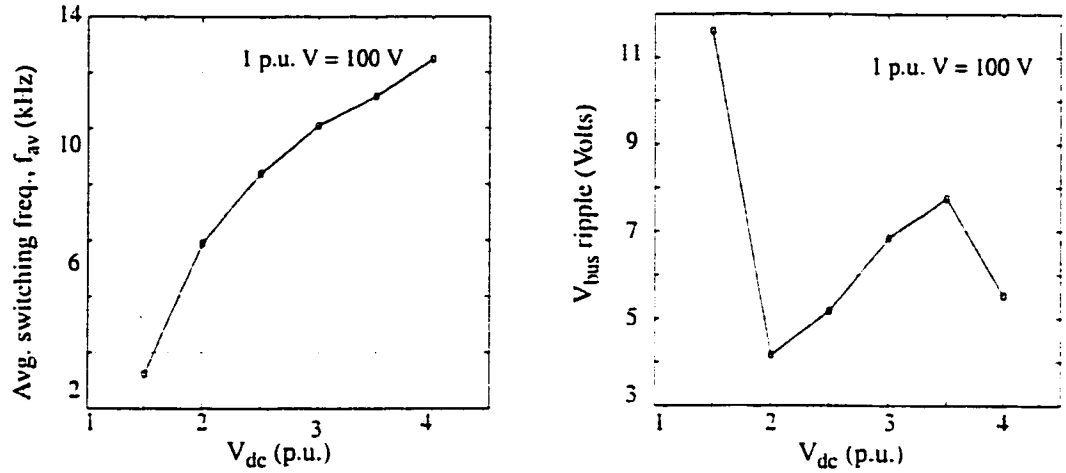
The rate of change of AF current is directly proportional to V_{dc}. A value of V_{dc} higher than the minimum required for good tracking, gives the DC bus capacitor greater energy to modulate the AF currents, between decision instants. An increase of V_{dc} causes the AF current to change more often between two decision instants leading to an increase in the switching ripple and switching frequency.

Table 3.6: Variation of DC bus voltage V_{dc}

V_{dc} (p.u.) (1 p.u.=100V)	f_{av} (kHz)	THD%	V_1 (Volts)	V_{rip} (Volts)
1.5	1.25	15.36	69.07	10.61
2.0	5.90	4.52	69.85	3.16
2.5	8.40	6.07	68.89	4.18
3.0	10.10	8.65	67.58	5.85
3.5	11.15	10.32	65.56	6.76
4.0	12.5	7.25	62.46	4.53

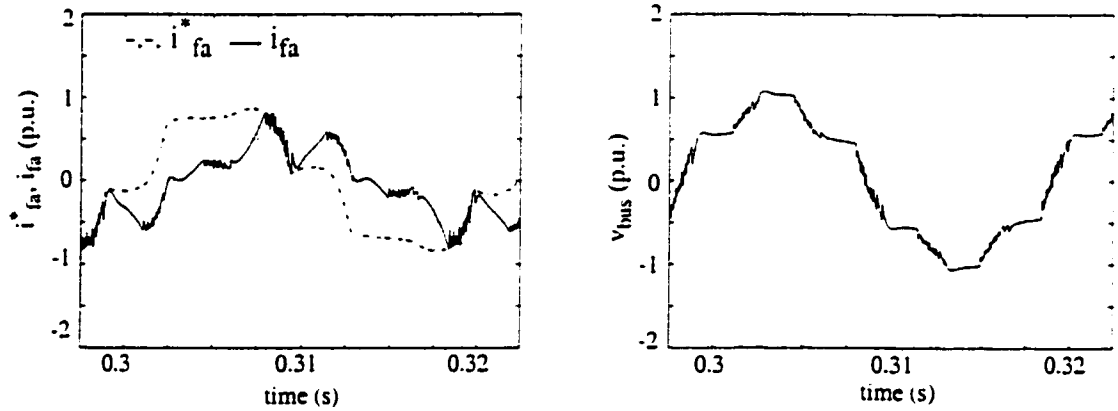
Table 3.6 shows the effect of variation of V_{dc} on different parameters. The bus voltage THD is not a correct measure in this case, as the fundamental voltage drops with an increase in V_{dc}. The bus ripple voltage V_{rip} is used as a measure.

Fig 3.20(i) shows a steady increase in switching frequency with the DC bus voltage. The THD is high for V_{dc} less than the minimum required V_{dc} as the AF is unable to track the reference currents properly. For higher values of V_{dc}, the switching error current magnitude and frequency increase causing greater distortion at the system bus. Fig 3.21 shows the simulation results for different values of V_{dc}. In Fig. (3.21 i), the AF reference current departs from its regular waveform as the dc bus voltage is insufficient for compensation and the distortion at ac bus is high.

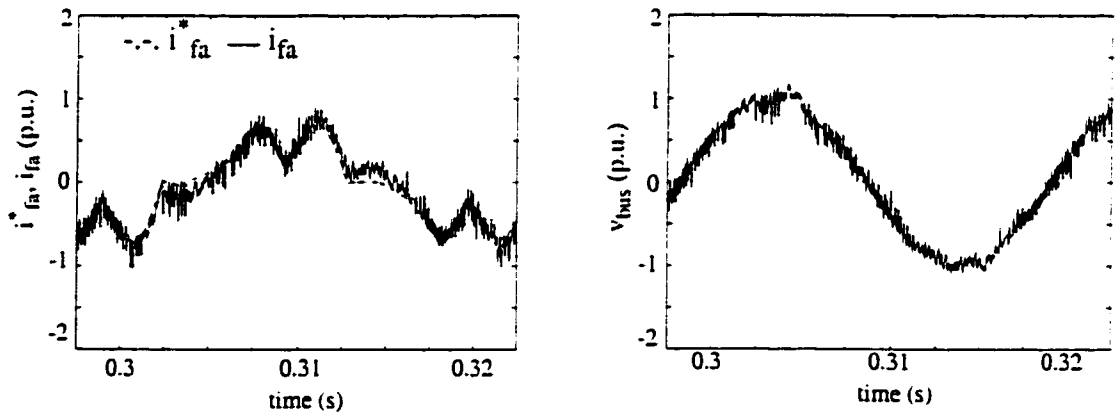


(i) f_{av} vs. V_{dc} (ii) V_{bus} ripple vs. V_{dc}

Fig 3.20 Variation of V_{dc}

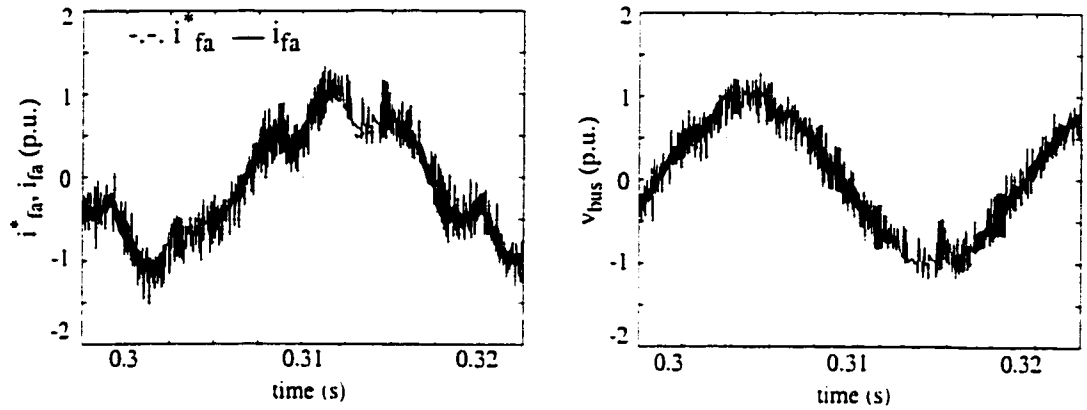


(i) V_{dc} = 1.5 p.u.



(ii) V_{dc} = 2.0 p.u.

Fig 3.21 Effect of V_{dc} variation



(iii) V_{dc} = 3.0 p.u.

Fig 3.21 *contd.* Effect of V_{dc} variation

AF Design

The AF design requires selection of the decision frequency, connection inductance L_c, the DC bus reference voltage and the DC bus capacitor, C_{dc}. To have comparable performance to the hysteresis controller, the decision frequency was chosen at 40 kHz. This also limited the maximum switching frequency to less than 20 kHz. An L_c value of 15 mH kept the THD at an acceptable level of less than 5%. The V_{dc} reference value was set at the minimum value, to keep the switching losses low, and a low THD at system bus. The C_{dc} value was taken as 200uF, high enough to meet load requirements temporarily for atleast 1 cycle, during fault at the AC bus.

3.4 Summary

In this chapter, the control aspect of the system model was covered.

The Rectifier Control Unit controls the output DC load current and the AF control Unit controls operation of the AF inverter. The feed-forward control scheme (on-line power computation) for AF reference currents computation was discussed.

Tracking control was demonstrated by hysteresis and sliding-mode control techniques. The effect of control parameters and circuit components on AF performance was discussed in detail. On the basis of that, control parameters for both the controllers were selected for optimal performance under switching frequency constraints.

Chapter 4

Transient Behavior of the Active Filter Model

4.1 Introduction

The transient performance of the active filter model operating with a weak AC system depends to a great extent on the control systems utilized. The details regarding the control system were presented in Chapter 3. To validate the operation of the rectifier control unit and the AF control unit under transient conditions, the system model was tested under various AC-DC fault conditions. The results of these tests are presented in this chapter.

4.2 System Tests

To validate the operation of the control scheme, the control units of the distribution system are optimized individually.

The controllers in operation for the distribution system are:

1) Rectifier Control Unit

2) Active Filter (AF) Control Unit

Initialization tests were performed for both the controllers to reach the steady state. Dynamic behavior of the overall system was checked, by performing the following tests:

i) Step change in rectifier current reference

ii) AC-DC system fault tests

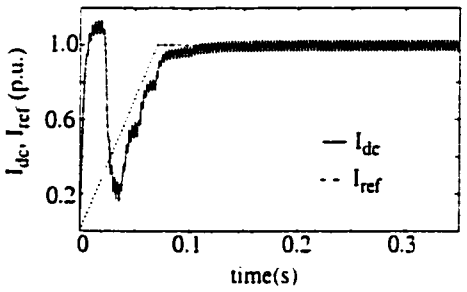
4.3 Initialization Tests

Prior to conducting any dynamic tests, the system model must achieve steady state operation. At first, the rectifier system is initialized by allowing the PI controller in rectifier control unit to regulate the DC load current to its reference value. After the DC current stabilizes, the active filter is switched on, and the AF controller controls the AF current according to compensation requirements. Steady state is reached when the whole system stabilizes.

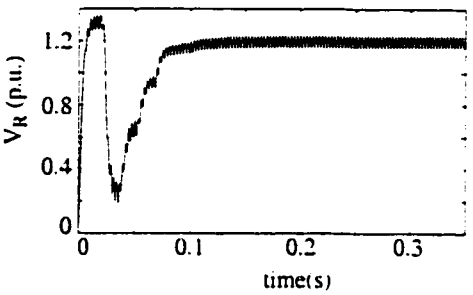
4.3.1 Initialization of Rectifier Control Unit

The rectifier control unit is initialized by disconnecting the AF compensator from the distribution system. Care should be taken to initialize the system and achieve the steady state operation point in a realistically short time. This depends on the selection of the PI controller parameters. The initializing current reference I_{ref} uses a ramp signal, so that the current rise in the DC load is gradual.

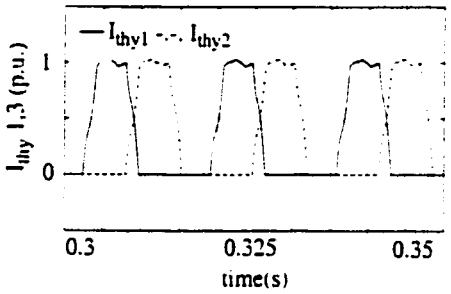
Fig 4.1 shows simulation plots for initialization of the rectifier unit. The firing signals are blocked for 0.02 sec, to initialize the inductor current. The rectifier thyristors act as diodes and the DC load current, I_{dc} rises to maximum. The firing angle, alpha increases to the upper limit to keep the DC load current in track with the blocked ramp reference signal, I_{ref}. It can be observed that the PI controller is able to track the reference current and achieve steady state in a fairly short time of 0.15 sec. Alpha attains a steady state value of 27 degrees. The AC bus voltage suffers from high distortion due to the weak AC source (source impedance-20% Z_{base}) and isolation transformer impedance (20% Z_{base}). The AC source current too has high distortion levels, as it supplies all the load harmonics, with no compensation from the active filter.



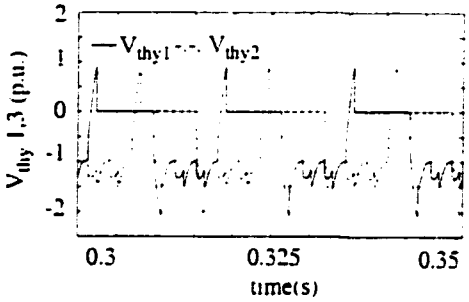
(i) DC load current



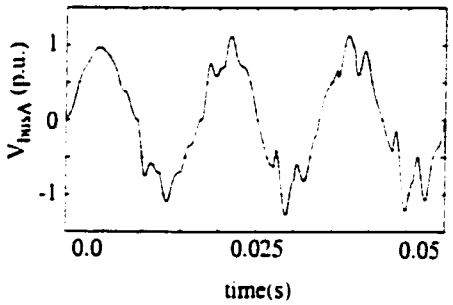
(ii) DC load voltage



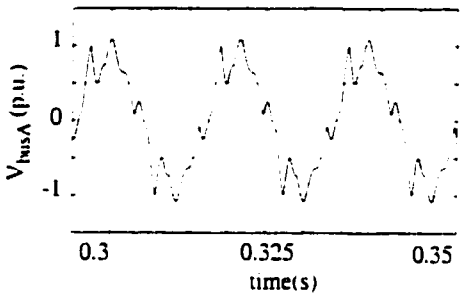
(iii) Current commutation



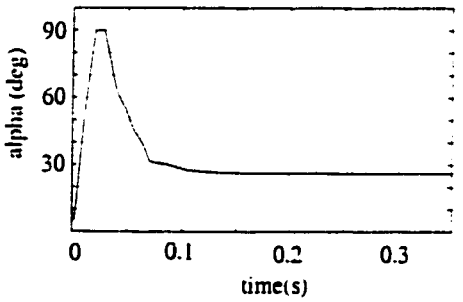
(iv) Thyristor voltage



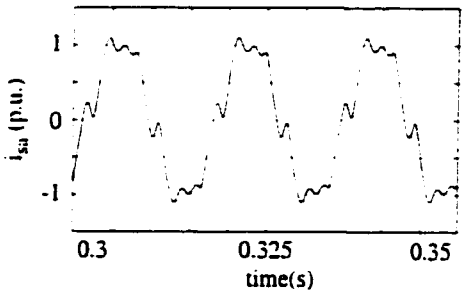
(v) AC bus voltage, at start



(vi) AC bus voltage, at steady state



(vii) Firing angle



(viii) Source current

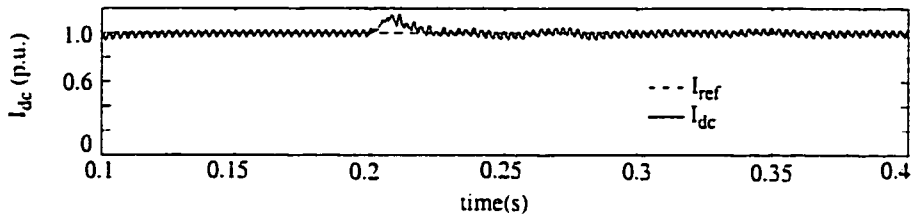
Fig 4.1 Initialization of Rectifier Unit

4.3.2 Initialization of AF Control Unit

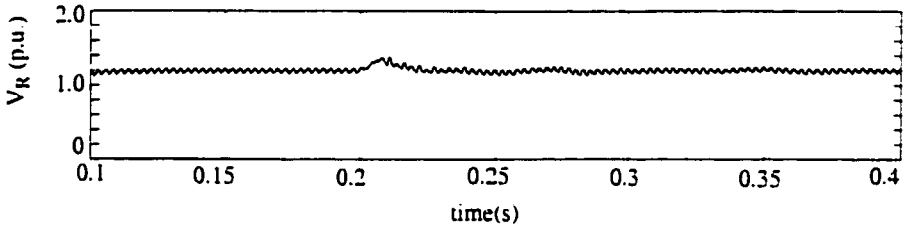
After the rectifier system has achieved steady state, the shunt active filter is switched on. The AF controller computes reference currents for the active filter from the start of simulations, but the active filter is switched on only after the DC load current has achieved steady state. The purpose is to observe the effect of switching in the active filter, on system operation and time taken by the AF to provide harmonic compensation. The AF compensation efficiency depends on the control law implemented. As mentioned in Chapter 3, the AF control has been demonstrated by two methodologies - hysteresis & sliding-mode control. A comparison of AF compensation efficiency is presented later, based on harmonic analyses of the system bus voltage and source current. Fig 4.2a shows the simulation plots for the case when a hysteresis based AF is switched into operation.

The DC load current, I_{dc} reaches its reference value at 0.15 sec, and the active filter is switched on at 0.2 sec. A small rise in DC current is observed. This is so because the AC bus voltage rises as the AF compensates for reactive power, leading to an increase in rectifier output voltage and DC load current. The PI controller takes care of the rise in DC load current by increasing the firing angle, alpha. The AF begins to track the reference currents within one cycle of operation. It can be observed that the system stabilizes within one cycle of switching in the active filter. There is a marked improvement in the AC source current which changes from a high harmonic content, square wave current to a fundamental harmonic, sinusoidal unity power factor current. As a result, the AC bus voltage distortion reduces tremendously, and the source power factor improves. The DC bus capacitor voltage, V_{dc} maintains a difference with the reference voltage, V_{ref} to absorb energy lost in switching and conduction. The DC bus voltage has a predominant sixth harmonic reflected from the three phase AC bus voltages, superimposed by high frequency ripple caused by the high frequency current supplied by the capacitor.

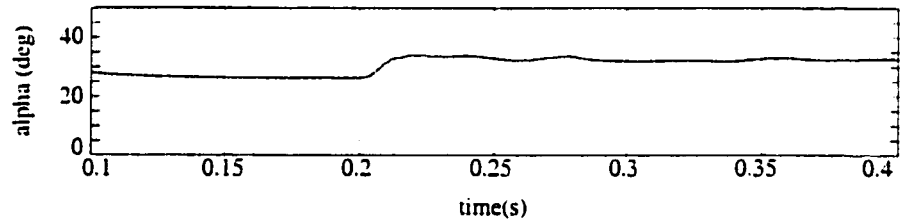
Fig. 4.2b shows compensation characteristics for sliding mode based AF in operation.



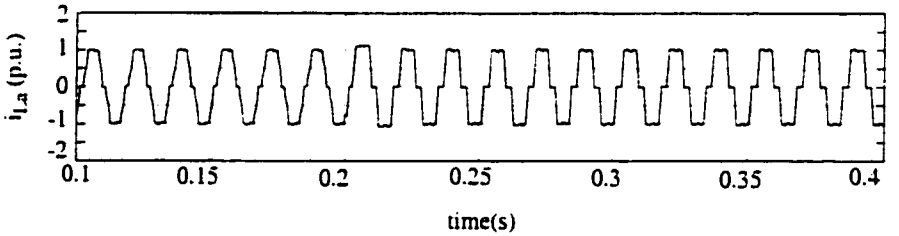
(i) DC load current



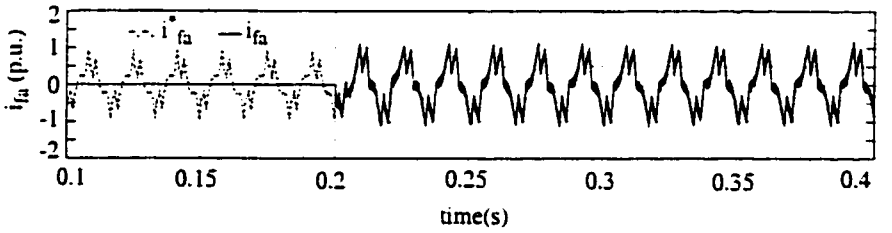
(ii) DC load voltage



(iii) Firing angle

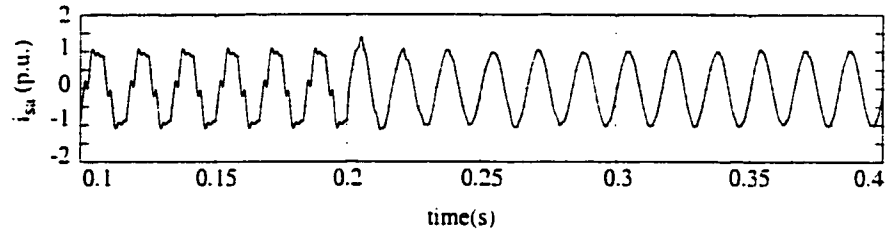


(iv) AC load current

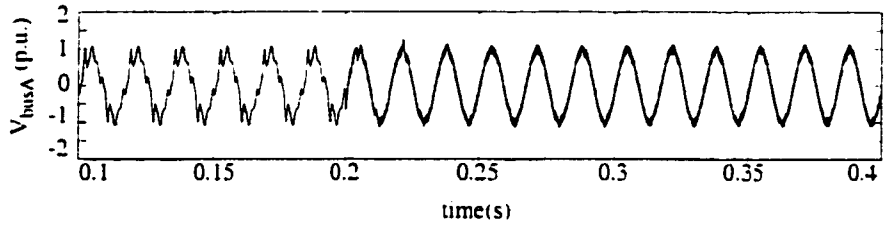


(v) Active Filter current

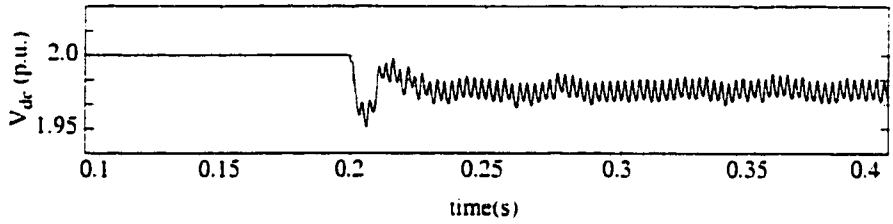
Fig 4.2a Active Filter Initialization - Hysteresis control



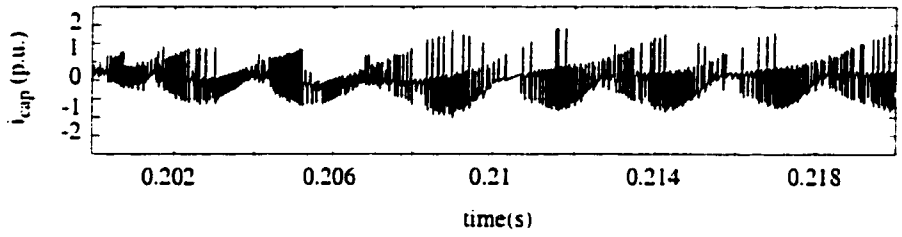
(vi) AC source current



(vii) AC bus voltage

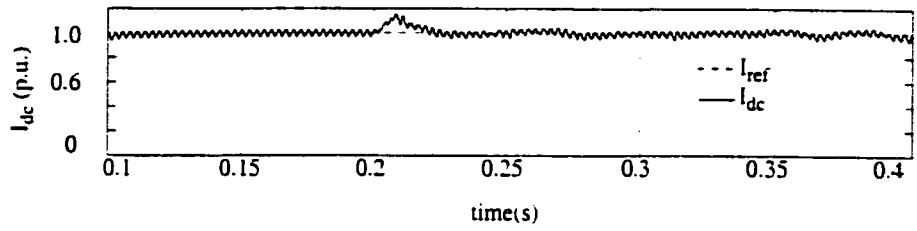


(viii) DC capacitor bus voltage

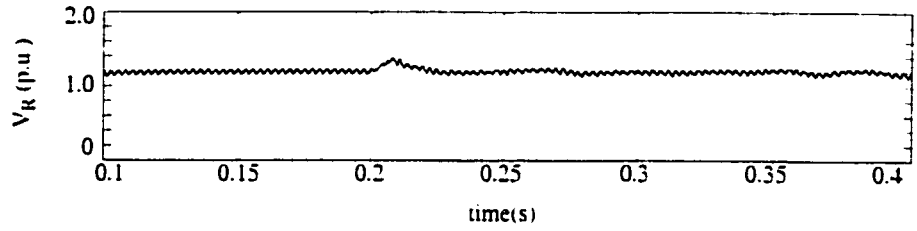


(ix) DC capacitor current

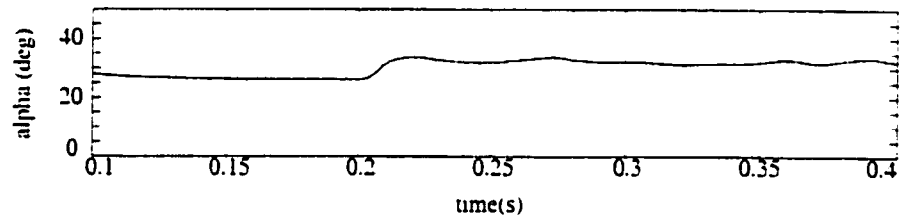
Fig 4.2a *contd.* Active Filter Initialization - Hysteresis control



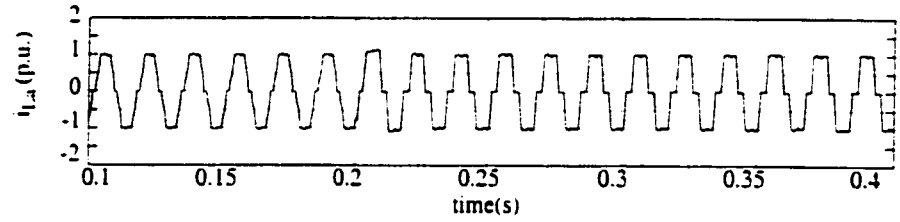
(i) DC load current



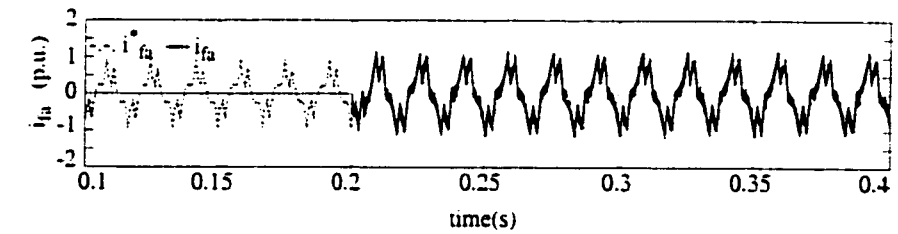
(ii) DC load voltage



(iii) Firing angle

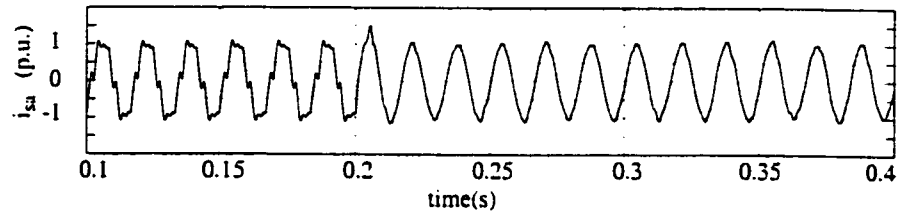


(iv) Load current

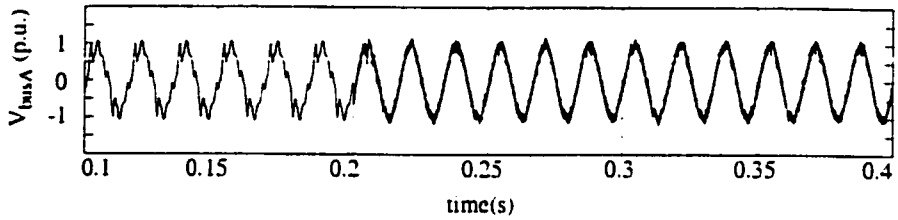


(v) Active Filter current

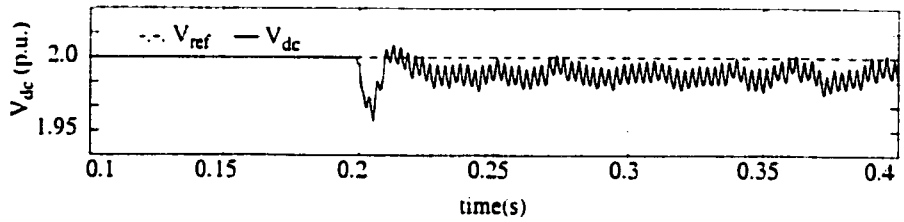
Fig 4.2b Active Filter Initialization - Sliding Mode Control



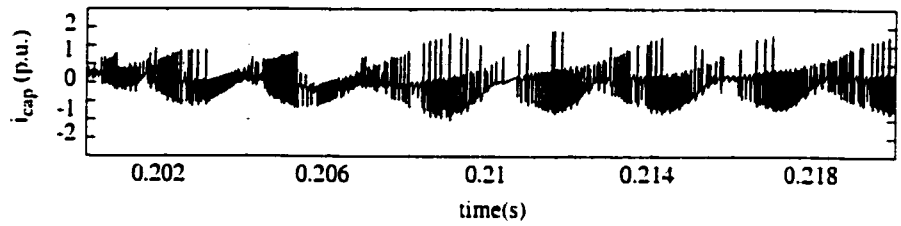
(vi) AC source current



(vii) AC bus voltage



(viii) DC capacitor bus voltage



(ix) DC capacitor current

Fig 4.2b *contd.* Active Filter Initialization - Sliding-mode Control

4.3.3 Comparison of Hysteresis and Sliding-mode control

Both controllers cause a variable switching frequency in the AF inverter. Therefore, a comparison of their compensation characteristics is made at an average switching frequency over a time period T, after steady state has been achieved.

The circuit parameters for AF - connection inductance L_c, DC bus capacitor C_{dc}, and the DC bus voltage V_{dc} were kept the same. The hysteresis bandwidth of hysteresis controller and decision frequency of sliding mode controller were adjusted to have similar average switching frequencies in the AF. The performance of the AF was measured by the improvement of THD of AC bus voltage.

For an average switching frequency of 6 kHz,

V_{bus} THD (Hysteresis Controller) = 2.6%

V_{bus} THD (Sliding Mode Controller) = 5.8%

The hysteresis controller provided better tracking of reference currents as the AF current was restricted within a tolerance band, limiting the tracking error.

The performance of sliding mode controller can be improved further by increasing the decision frequency.

4.3.4 Harmonic analysis

A harmonic analysis was done for the steady state initialization case, with and without the active filter compensation. The analysis has been done for a hysteresis-based AF, but similar analysis is also valid for the sliding mode based AF. The standard FFT algorithm in MATLAB has been used. Only the contribution of characteristic harmonics is shown, although non-characteristic harmonics are also present.

1) Steady state case before AF switched on

Table 4.1 shows the harmonic analyses for the steady state case, before the active filter is switched on. The AC source current, i_{source} has high harmonic content for the lower order harmonics. This is due to current amplification of load harmonics by the high pass AC filter connected in shunt at the system bus and tuned to the 12^{th} harmonic. The AC filter provides harmonic compensation only for harmonics greater than the tuned frequency. The system bus voltage suffers from high distortion due to high harmonic content of source current.

Table 4.1: Harmonic Analyses (without AF compensation)

Harmonic order #	i_{load} (p.u.)	i_{source} (p.u.)	$i_{acfilter}$ (p.u.)
1	0.759	0.738	0.042
5	0.078	0.122	0.044
7	0.023	0.076	0.057
11	0.027	0.023	0.045
13	0.023	0.013	0.032
17	0.008	0.003	0.009

THD of V_{bus} = 26.01%

2) Steady state case after AF switched on

Table 4.2 gives the harmonic analyses of steady state currents, after the active filter is switched on. The AF meets most of the harmonic requirements of the load locally, thus reducing tremendously the harmonic content of source current. The switching error currents generated are absorbed by the shunt AC filter connected at the AC bus. It may be

noted that the AF also supplies a fundamental harmonic current that corresponds to the reactive power compensation. Reactive power compensation increases AC bus voltage and harmonics compensation reduces distortion tremendously.

Table 4.2: Harmonic Analyses (with AF compensation)

Harmonic order #	i_{load} (p.u.)	i_{source} (p.u.)	i_{AF} (p.u.)	$i_{acfilter}$ (p.u.)
1	0.778	0.718	0.536	0.047
5	0.151	0.005	0.152	0.002
7	0.079	0.007	0.077	0.005
11	0.035	0.001	0.036	0.002
13	0.024	0.0007	0.023	0.002
17	0.005	0.0007	0.007	0.003

THD of V_{bus} = 2.90%

4.4 Dynamics Tests

After the system achieved steady state, the model was subjected to different dynamic tests to check system operation under transient conditions. The transient tests include a step change of DC current reference and AC-DC system fault conditions subjected on the model.

4.4.1 Step change of 20% in DC current reference, I_{ref}

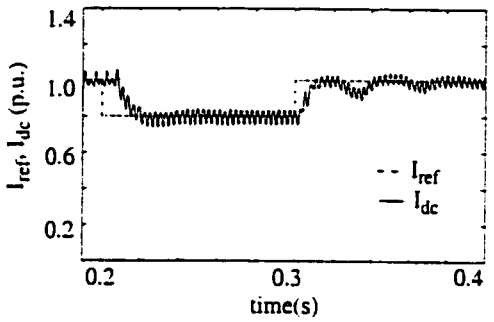
To test the performance of the PI controller in rectifier control unit, a step change of 20% was applied to its current reference, I_{ref}. The step change is applied at 0.2 s and lasts for 6- cycles (0.1 s).

The simulation results are shown in Fig 4.3 a,b for the hysteresis and sliding mode

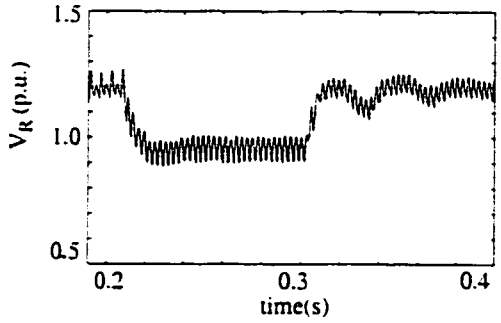
controllers respectively. The response is well controlled and stable. The firing angle signal, alpha rises instantly at 0.2 s to reduce the DC current and returns to steady state after the step change is over. During the transition period, there is a drop in active load. As a result, the source reference currents reduce.

Reactive power drawn remains practically the same as the increase in firing angle compensates for the drop in current magnitude. Therefore the AF reference currents show only a minor variation. The AF replicates its reference currents completely within allowed limits. It is interesting to observe that even during the transient change, the source current remains sinusoidal at unity power factor.

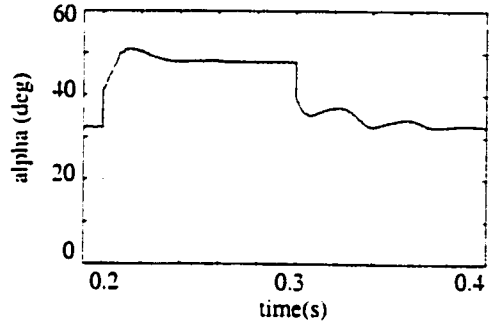
The AC bus voltage remains practically unaffected as the AF maintains compensation during the transient period. The DC bus voltage rises and falls below its steady state value at the transition instants, due to the 1 cycle computation delay when the AF absorbs or supplies extra active power to the load.



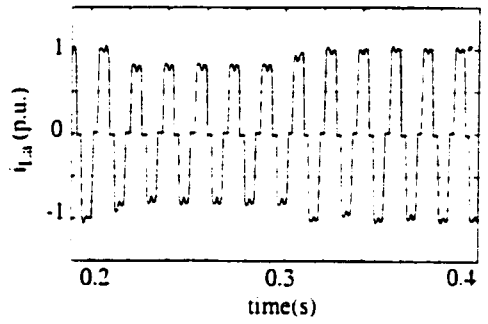
(i) DC load current



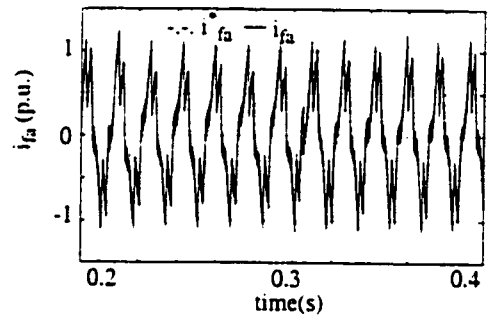
(ii) DC load voltage



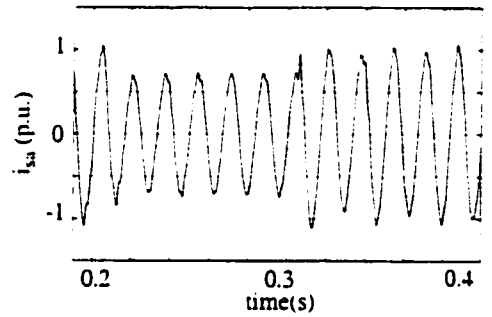
(iii) Firing angle



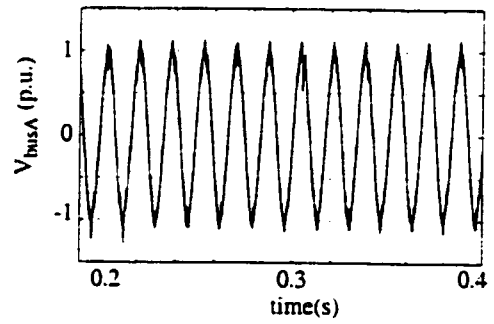
(iv) Load current



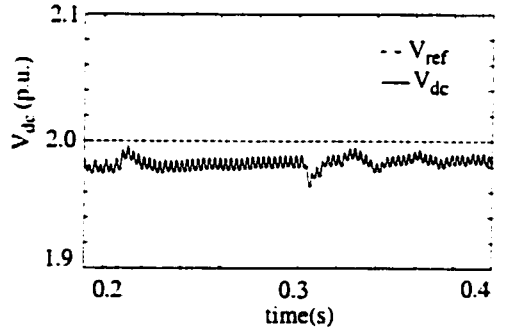
(v) Active filter current



(vi) Source current

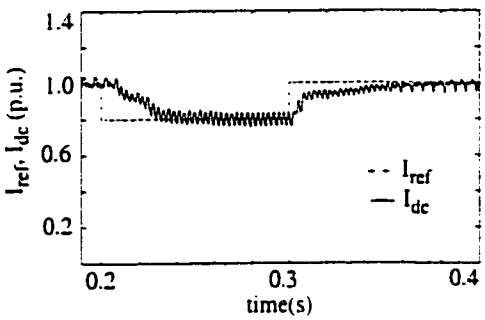


(vii) AC bus voltage

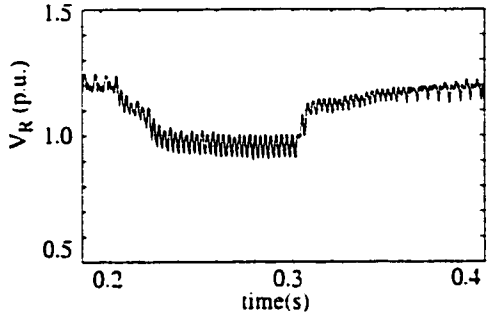


(viii) DC bus voltage

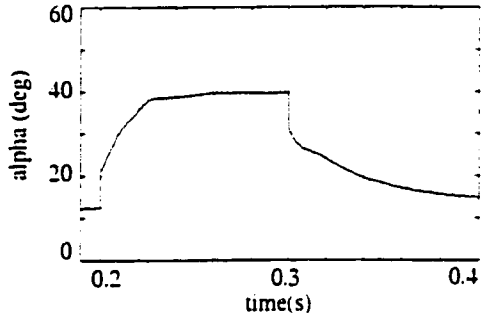
Fig 4.3a Hysteresis Controller - transient response



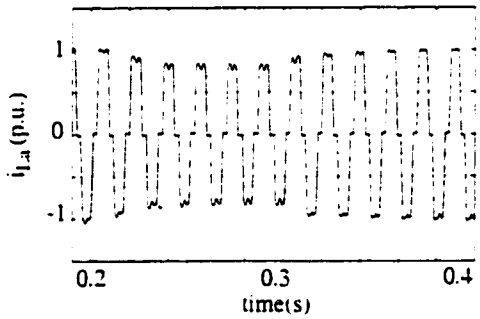
(i) DC load current



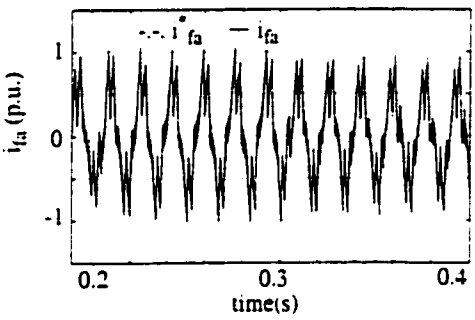
(ii) DC load voltage



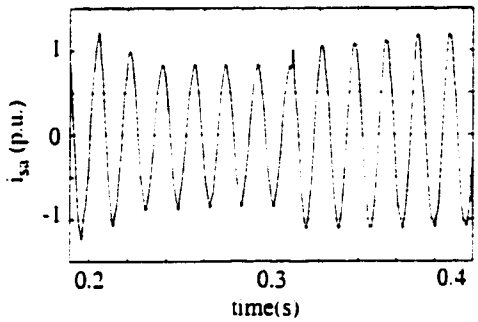
(iii) Firing angle



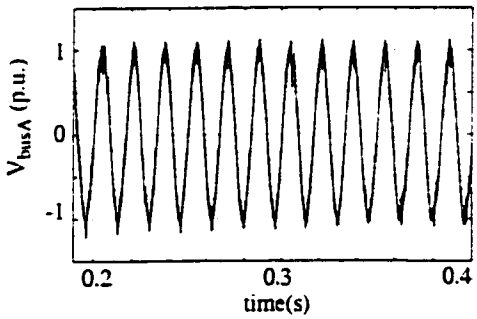
(iv) Load current



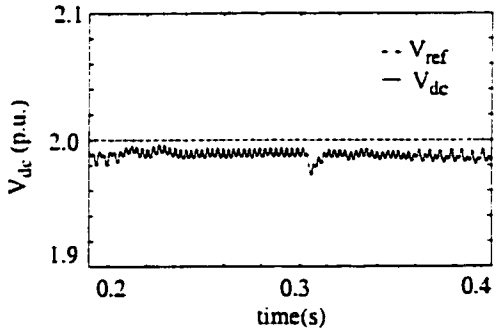
(v) Active filter current



(vi) Source current



(vii) AC bus voltage



(viii) DC bus voltage

Fig 4.3b Sliding Mode controller - transient response

4.4.2 Fault Tests

In the following sections, results from a number of fault tests are presented and discussed.

4.4.2.1 Single-Phase "Solid" Line to Ground 3-Cycle Fault at AC bus (Commutation failure test)

A commutation failure occurs when either the triggering signals are not generated or are wrongly positioned. This prevents commutation from one thyristor to another. It is simulated by creating a single phase 3-cycle fault at the AC bus. Fig.4.4a shows simulation results for the hysteresis control based active filter.

The single line to ground (SLG) fault was applied to phase A of AC bus at 0.2s and lasted for 3 cycles (0.05s). As bus voltage of phase A, V_{busA} goes to zero, the rectified DC voltage drops, reducing the DC load current I_{dc}.

The firing angle, alpha goes down to a minimum to increase the DC current. Due to the non-uniform DC current during the fault period, the AC load currents i_{La}, i_{Lb}, i_{Lc} become unbalanced. The on-line power controller computes average power consumed by the load and balances the active load on the three phases by generating balanced source reference currents. Since the AC load currents are unbalanced, the AF reference currents i^*_{fa}, i^*_{fb}, i^*_{fc} (Eqn. 3.6) are unbalanced and non-uniform (plot v).

The AF reference currents i_{fa}, i_{fb}, i_{fc} replicate their reference currents keeping the source currents i_{sa}, i_{sb}, i_{sc} balanced at all times. Thus the AF serves the dual purpose of balancing the unbalanced active power of load phases on source phases and meeting the reactive and harmonic requirements locally. The fault at the AC bus is fed only by the respective phase as the active filter is a floating device with no ground connection.

The generator phase current consists of a fault current component i_{fltA} and the balanced active load component i_{sa}. A decaying DC transient is present in the fault component i_{fltA} (plot ix).

Due to a single line to ground fault at the AC bus, positive, negative and zero sequence currents are introduced into the network unbalancing the AC bus voltages. Hence during the fault period, the source currents although balanced are not strictly at unity power factor.

A drop in the DC bus capacitor voltage V_{dc} is noted. The DC bus loses more active power due to the increased harmonic load during fault period, resulting in more conduction losses in the active filter.

Similar observations were made for the sliding-mode controller based active filter, as shown in Fig. 4.4b.

4.4.2.2 Single Phase Line to Ground 3-cycle fault at AC bus (with fault impedance)

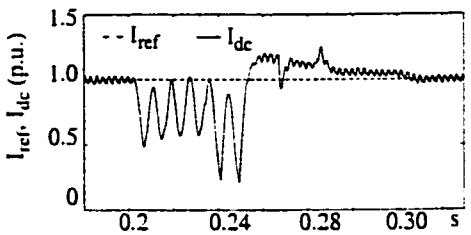
A single phase line to ground fault with fault impedance was applied to phase A of the AC bus at 0.2s for 3 cycles (0.05s).

The fault impedance, predominantly inductive, was selected such that the fault current magnitude was 50% of that for the SLG solid fault case. Figs. 4.5a,b show the fault results for the hysteresis and sliding-mode control based AFs.

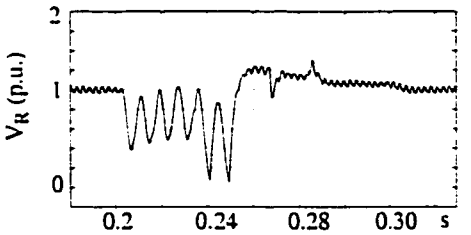
The bus voltage of phase A (plot viii) drops to 50% of its normal value (1 p.u.) reducing the DC load current and making it non-uniform. The firing angle, alpha drops to increase the DC current.

Although the AC load currents are unbalanced, the on-line power controller computes balanced source reference currents. Balanced three phase currents are drawn from the AC source, and the AF provides power exchange to meet individual requirements of the unbalanced rectifier load.

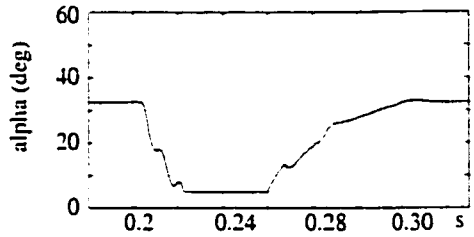
The AC bus voltages are unbalanced due to the presence of positive, negative and zero sequence currents. Hence the source currents are not at unity power factor during the fault period. The DC bus voltage drops due to increased conduction losses, but recovers rapidly to its steady state value after fault removal. A decaying DC transient was noted in the generator phase fault current i_{fltA} (plot ix).



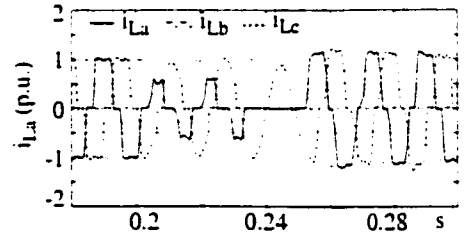
(i) DC load current



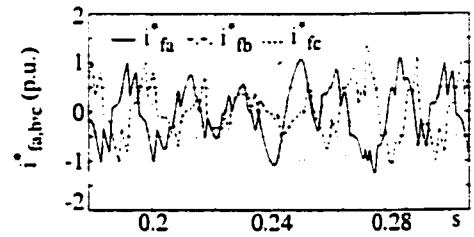
(ii) DC load voltage



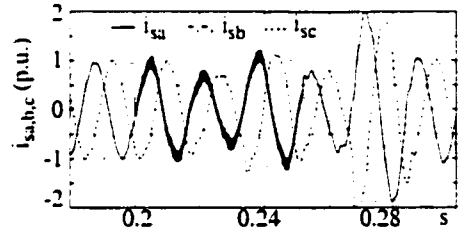
(iii) Firing angle



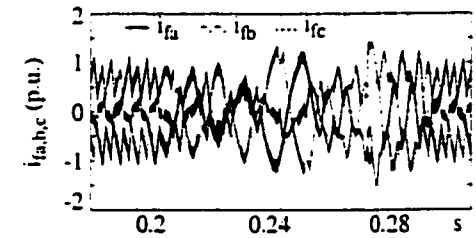
(iv) AC load current



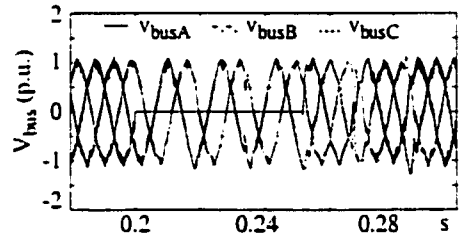
(v) AF reference currents



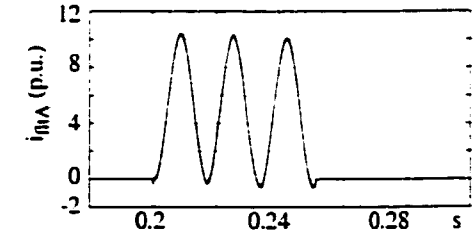
(vi) Source currents



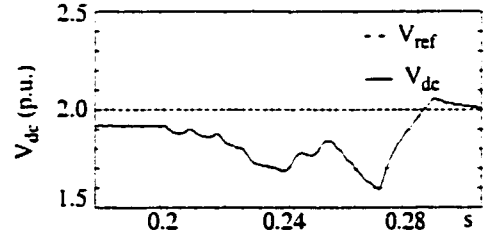
(vii) AF currents



(viii) AC bus voltages

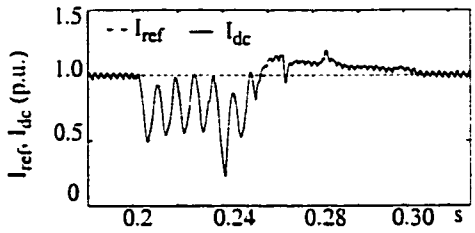


(ix) Fault current

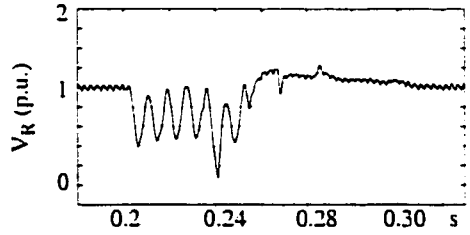


(x) DC bus voltage

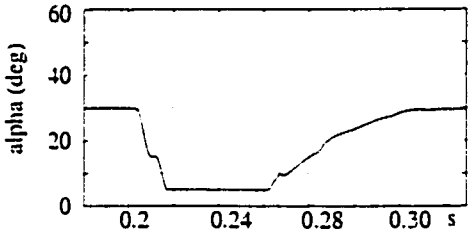
Fig 4.4a Hysteresis Controller - Single phase fault at AC bus



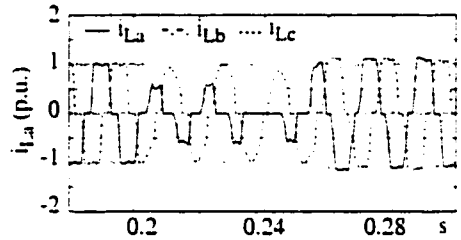
(i) DC load current



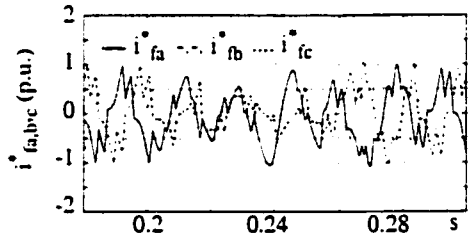
(ii) DC load voltage



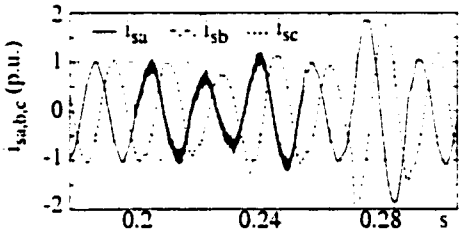
(iii) Firing angle



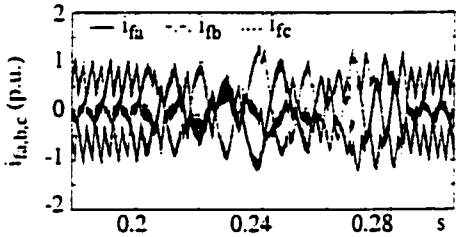
(iv) AC load current



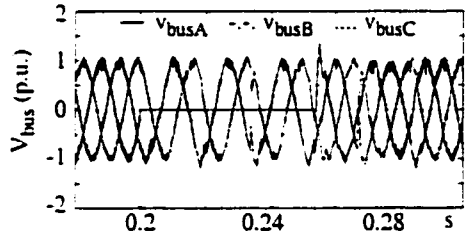
(v) AF reference currents



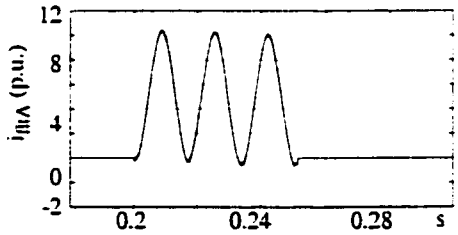
(vi) Source current



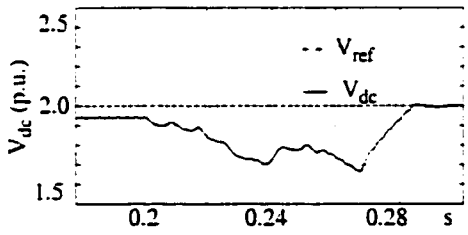
(vii) AF currents



(viii) AC bus voltages



(ix) Fault current



(x) DC bus voltage

Fig 4.4b Sliding-mode Controller - Single phase fault at AC bus

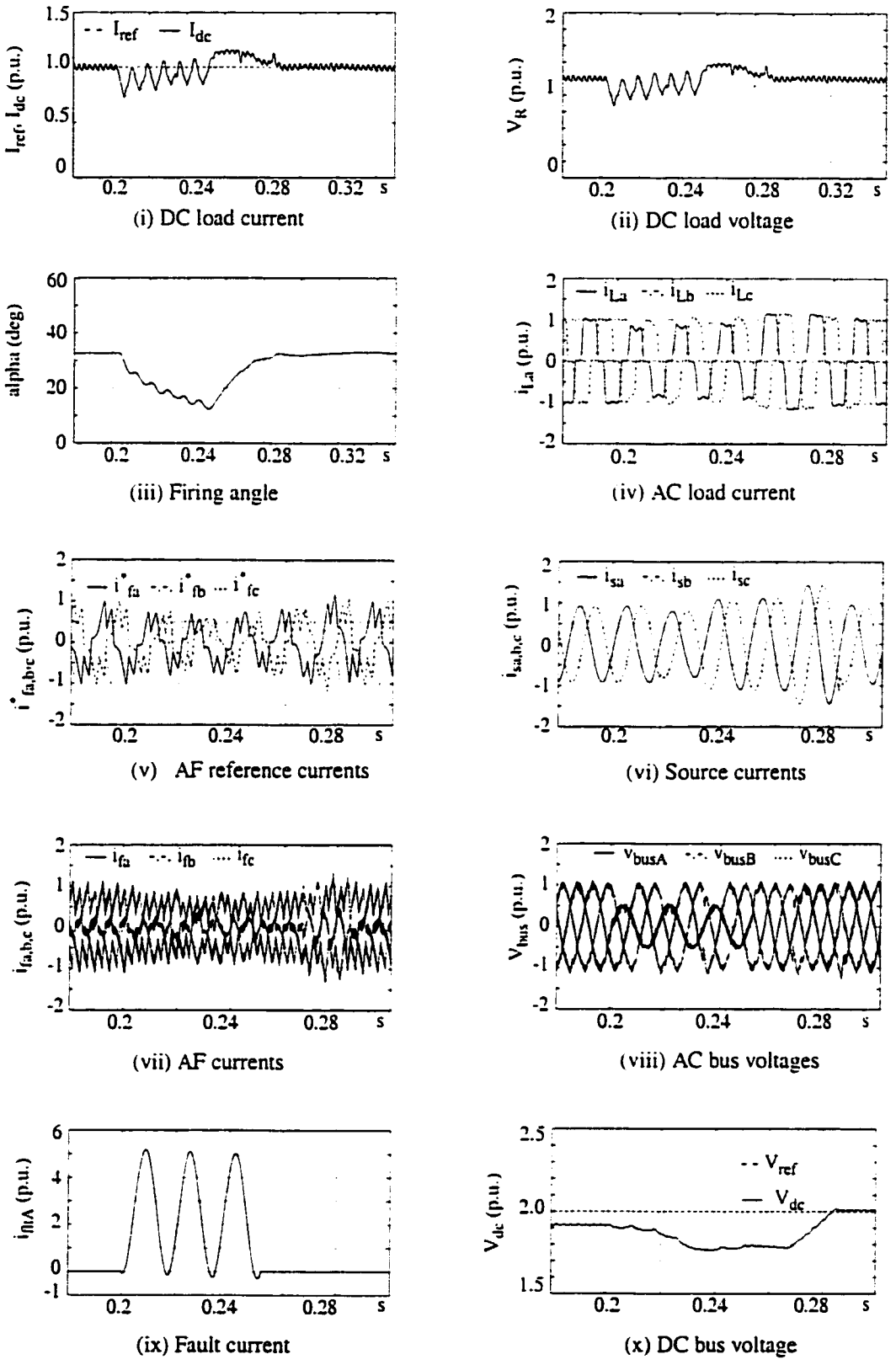


Fig 4.5a Hysteresis Controller - Single phase fault (50%) at AC bus

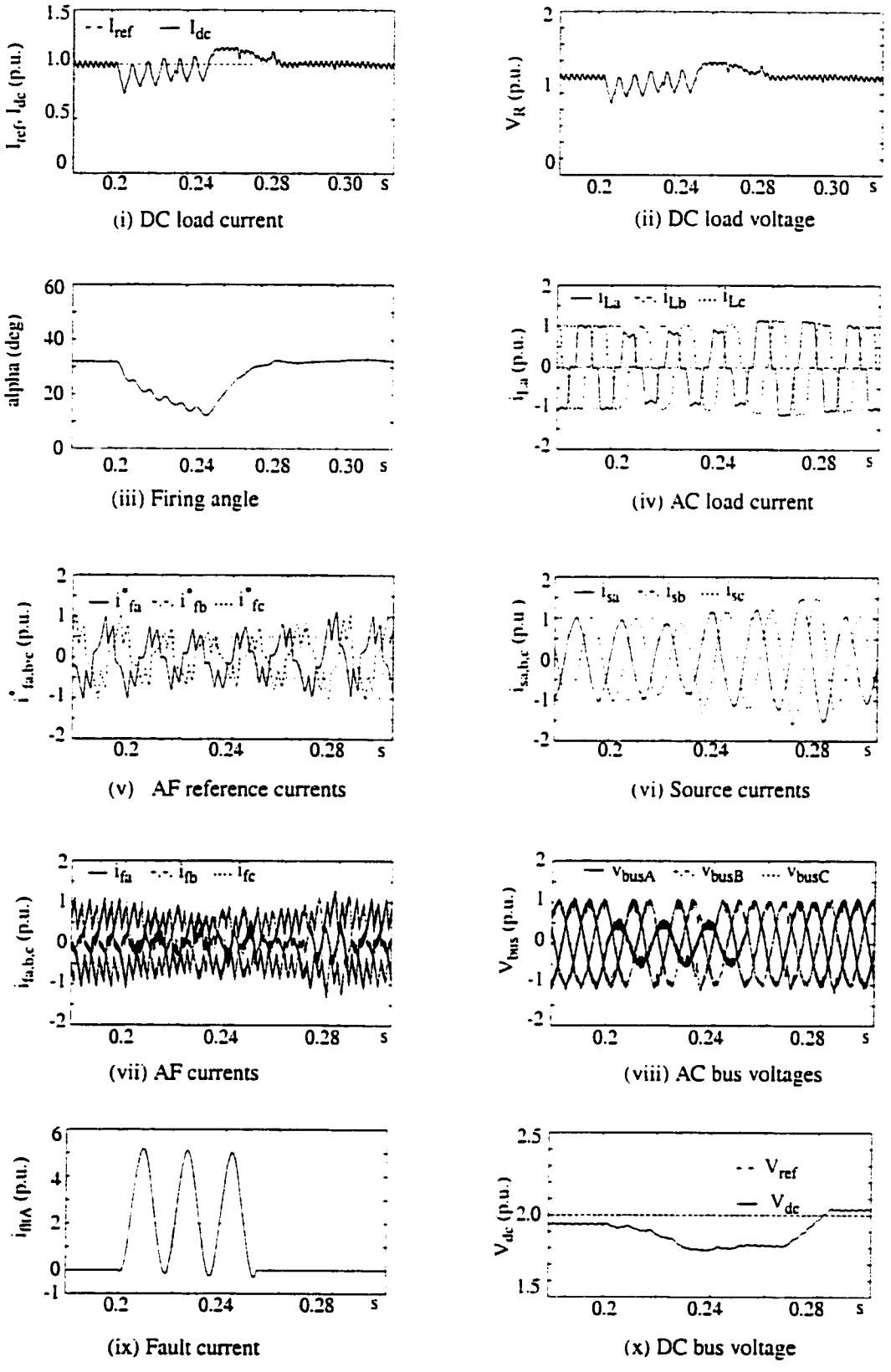


Fig 4.5b Sliding-mode Controller - Single phase fault (50%) at AC bus

4.4.2.3 Line to Line 3-Cycle Fault at AC bus (phases A,B)

A 3-cycle line to line (L-L) fault was applied at the phases A and B of the AC bus at 0.2s. The phase voltages become unbalanced due to introduction of positive and negative sequence currents in a weak AC network.

Figs 4.6a,b show simulation plots for the test case.

The rectified DC voltage drops causing the DC load currents to reduce and become non-uniform. Alpha drops down to a minimum to rapidly increase the DC current. Although the bus voltages are unbalanced, the PLL filters generate balanced 3-phase unit template voltages (u_a, u_b, u_c) and hence balanced source reference currents. The AF reference currents are highly irregular due to the distorted AC load currents, but the AF tracks its reference currents completely at all instants.

Thus inspite of highly distorted AC load currents, the rectifier load draws balanced three phase currents even during the fault period.

The generator phase current consists of a fault component i_{fltAB} and a balanced active load component i_{sa} drawn by the rectifier load. Plot (ix) shows the fault current component i_{fltAB} flowing in the source phases A and B of the generator. A decaying DC transient is also observed in the fault current.

The DC bus capacitor voltage V_{dc} drops during the fault due to increased harmonic and conduction losses, but recovers within 2 cycles after fault removal.

4.4.2.4 Three Phase "Solid" Line to Ground Fault at AC bus (Phases A,B,C)

A three phase solid line to ground fault was applied at the AC bus at 0.2s for 3 cycles (0.05s). Figs. 4.7 a,b show simulation results for the test case.

Phase voltages of the three phases of AC bus become zero. The DC rectified voltage and the DC load current I_{dc} become zero. Firing angle, alpha hits the minimum to increase DC current. As the AC load currents and bus voltages drop to zero, the active

power drawn by the load becomes zero. The only active load on the source is the charging of the DC bus capacitor for meeting the conduction and switching losses in the active filter.

Thus during the fault period, the AF acts as a balanced three phase load to the AC source, drawing active power to keep its DC bus charged.

The generator phase current consists of a fault component that circulates in the three phases and a balanced active load component drawn by the AF. Plot (ix) shows the fault currents i_{fltA}, i_{fltB}, i_{fltC} circulating in the three phases of the generator.

The DC bus voltage recovers within 2 cycles after removal of the fault.

4.4.2.5 DC 6-cycle Fault at Rectifier load end

A DC fault was applied at the rectifier load end by short-circuiting the load resistor for 6 cycles (0.1s), starting at 0.15s. Simulation results for the hysteresis and sliding-mode based AFs are shown in Figs. 4.8a,b.

The DC load current rises to 2.5 p.u. due to sudden loss of load. The DC load voltage drops to zero and the Voltage Dependent Current Limiter (VDCL) protection is activated, bringing down the DC current reference I_{ref} from 1 p.u. to 0.2 p.u. The VDCL protection prevents wide swings in DC load current and saturation in firing angle during fault periods. I_{ref} rises uniformly after removal of fault for smooth rise in DC load current.

At the onset of fault, the current reference drops to the minimum limit (0.2 p.u.) and the firing angle goes into inverter mode to bring down the overshoot to the new reference limit. Commutation failures due to high distortion in AC bus voltages (plot viii) prevent I_{dc} from tracking I_{ref} properly, and the DC current oscillates about the reference value. The AC load currents are unbalanced due to the discontinuous DC load (plot vi). The on-line power controller generates balanced yet non-sinusoidal source reference currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) as the unit template voltages are non-sinusoidal due to high distortion in AC bus voltages.

The AF stabilizes the bus voltages within 3-cycles of fault occurrence (plot viii). The DC bus capacitor voltage V_{dc}, drops slightly at the instant of fault onset, as the DC current overshoots and the AF meets the increased active power demand, by supplying some of its stored active energy momentarily.

At the end of the current overshoot, the DC capacitor gains excess active energy due to the 1-cycle computation delay inherent in the algorithm, stabilizing shortly to its steady state value. A drop in V_{dc} is again noted when I_{dc} increases to 1 p.u. after fault removal, and the AF temporarily supplies some active energy, stabilizing soon to its steady state value.

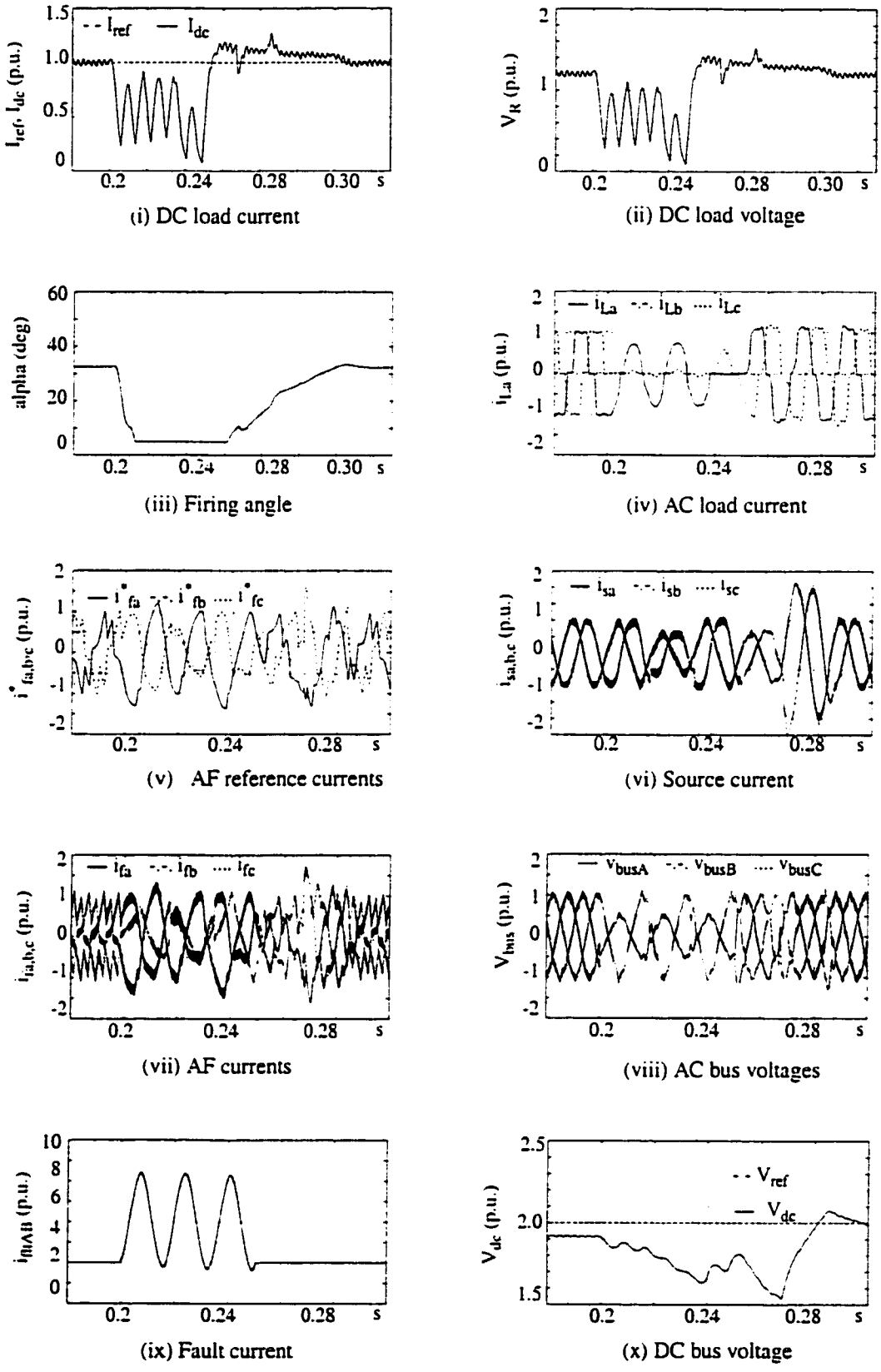


Fig 4.6a Hysteresis Controller - Line-Line fault at AC bus (ph. A-B)

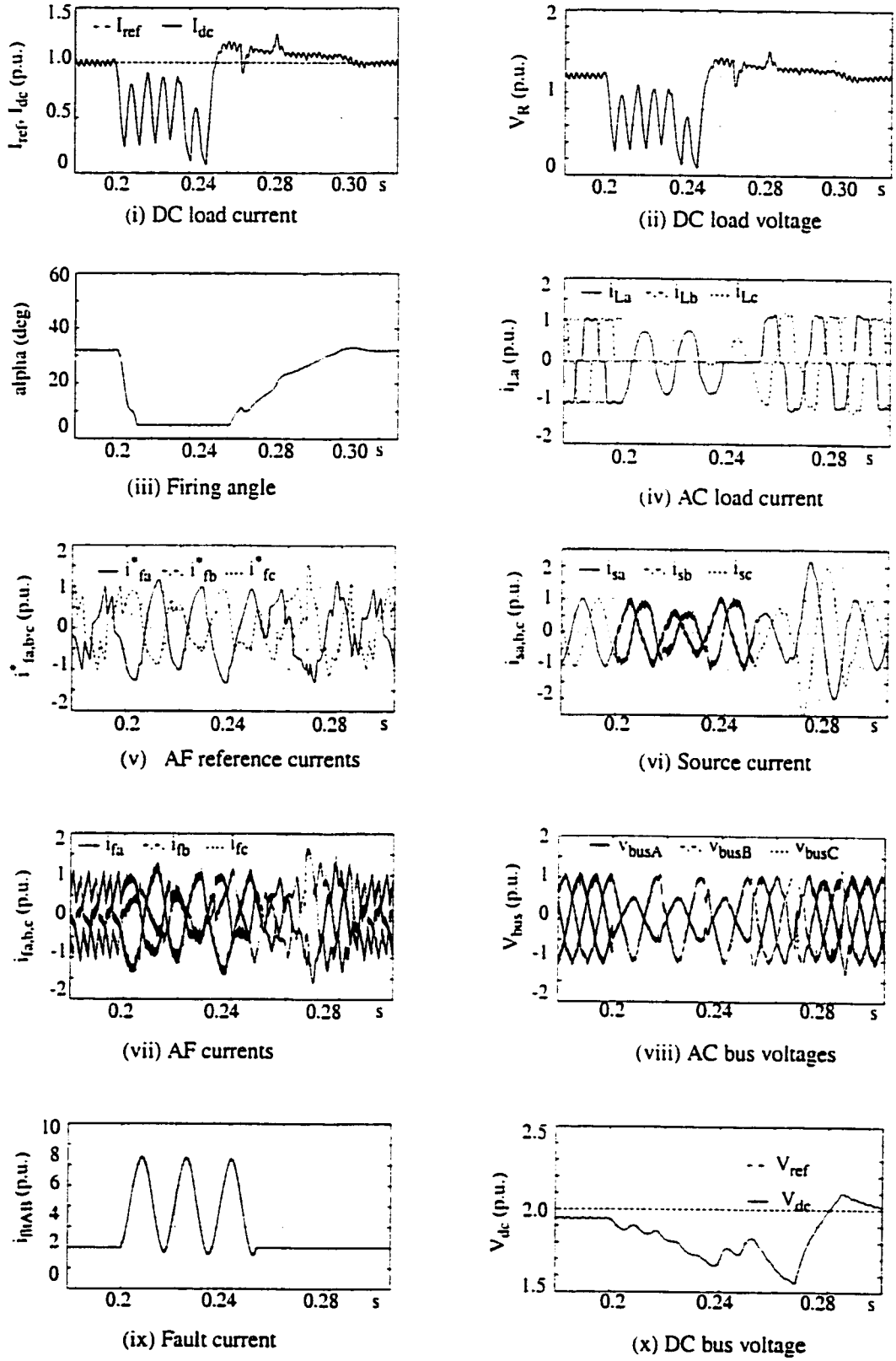


Fig 4.6b Sliding-mode Controller - Line-Line fault at AC bus (ph. A-B)

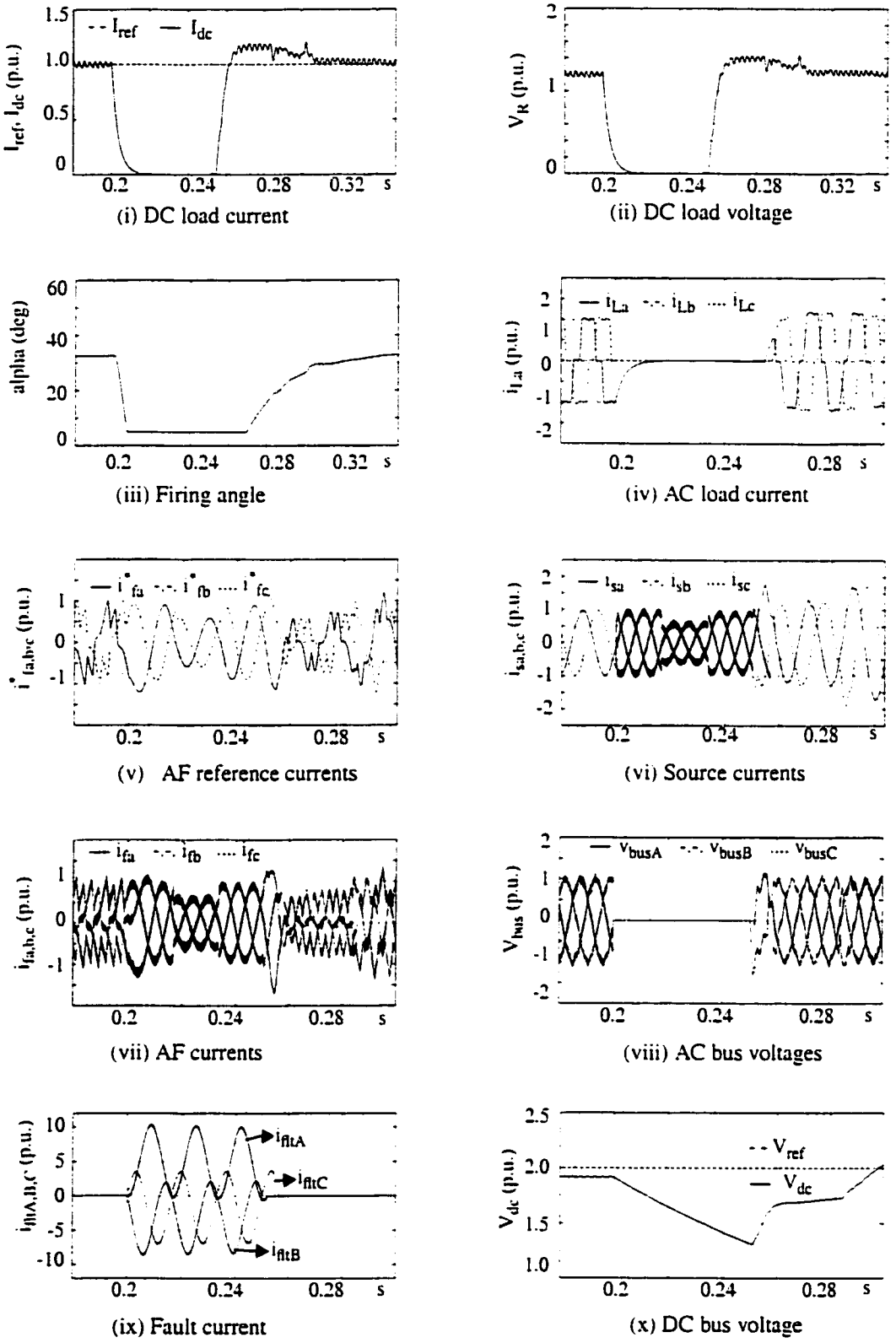


Fig 4.7a Hysteresis Controller - 3 phase L-G fault at AC bus

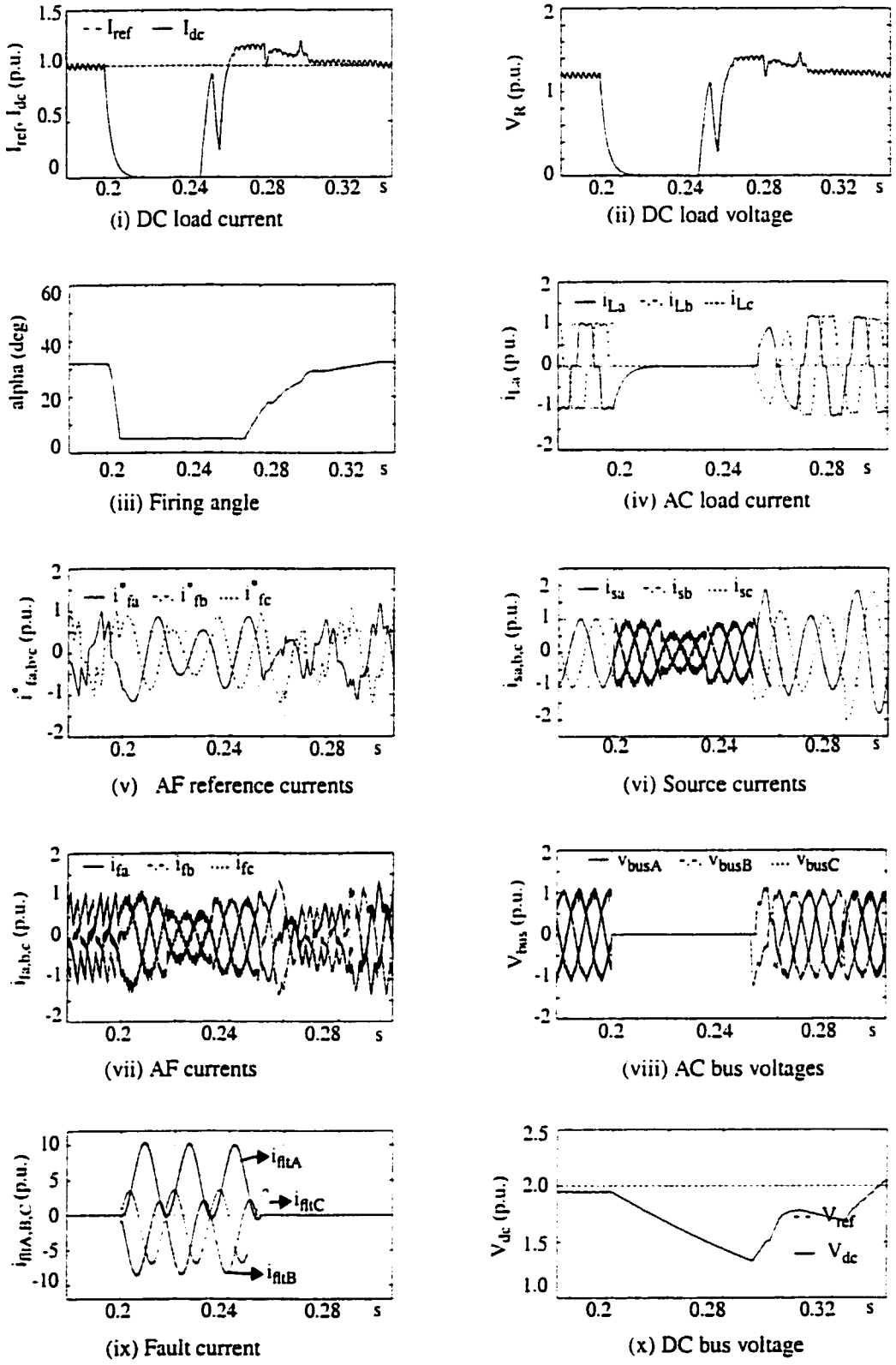
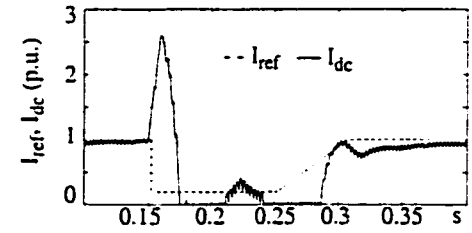
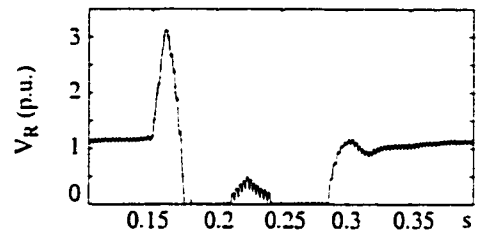


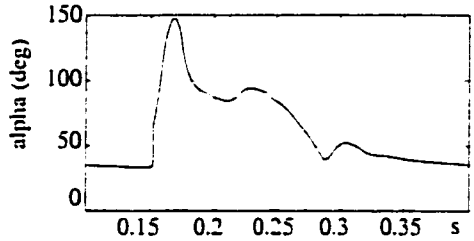
Fig 4.7b Sliding-mode Controller - 3 phase L-G fault at AC bus



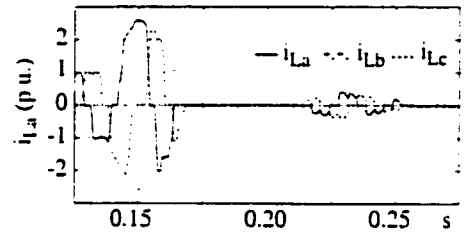
(i) DC load current



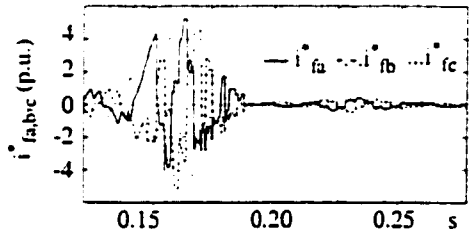
(ii) DC load voltage



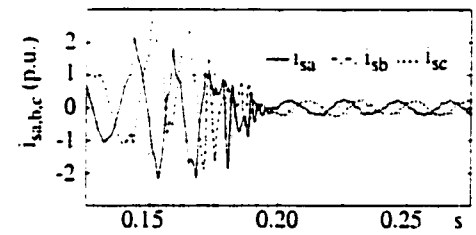
(iii) Firing angle



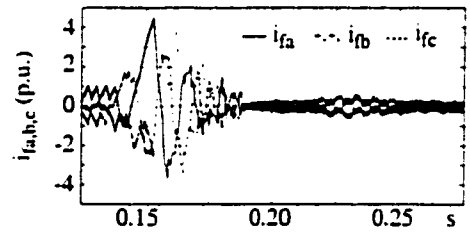
(iv) AC load currents



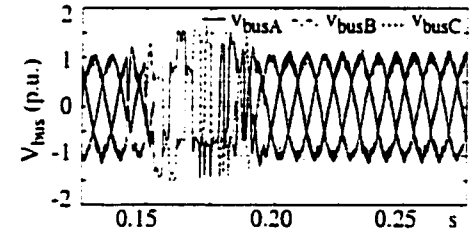
(v) AF reference currents



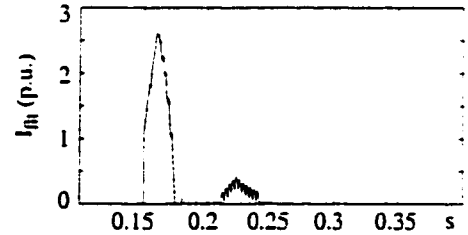
(vi) Source currents



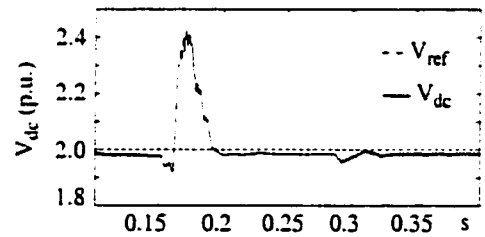
(vii) AF currents



(viii) AC bus voltages



(ix) DC Fault current



(x) DC bus voltage

Fig 4.8a Hysteresis Controller - Fault at DC load

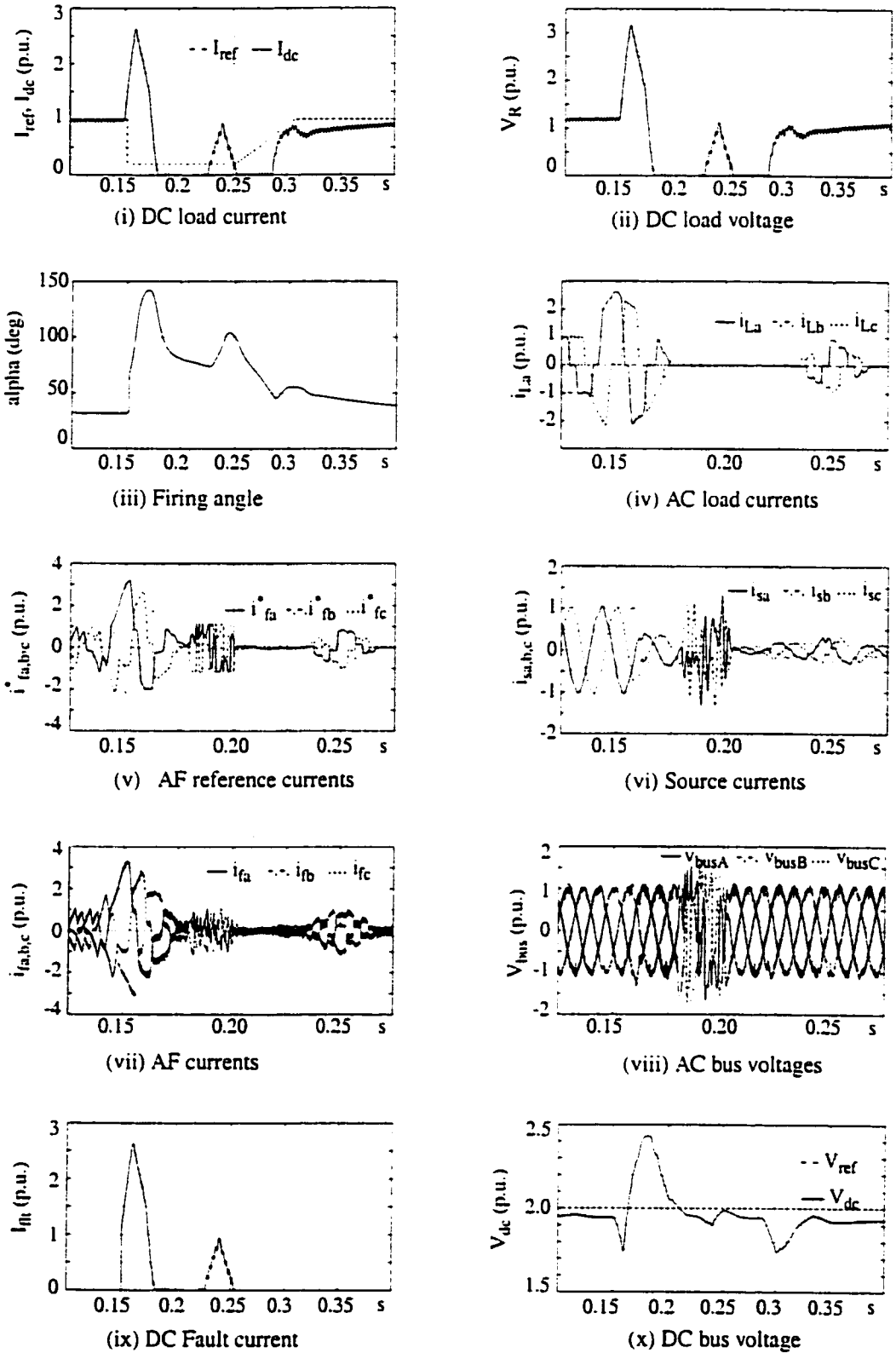


Fig 4.8b Sliding-mode Controller - Fault at DC load

4.5 Summary

In this chapter the system model was initialized and subjected to various dynamic tests. It was observed that the system initialized in a short time, and the active filter begins to provide compensation within a cycle of operation.

During transient tests, when the current reference for DC load was changed, the active filter maintained compensation during the transition period. The test results of both the controllers were similar, although the hysteresis controller provides better tracking of reference currents for comparable switching frequencies. The performance of the sliding mode controller could be improved further by increasing its decision frequency.

During AC-DC faults, the DC load current becomes non-uniform, unbalancing the AC line currents. The on-line power controller generates balanced source reference currents. The AF connected at the AC bus provides exchange of power, balancing the active load over the three source phases, and compensating for harmonics locally. Thus an unbalanced load appears as a balanced three phase load under all fault conditions. This helps in keeping the voltage distortion in the healthy phases under control. As an exception, in the DC fault case, the system bus voltage and source currents suffer from excessive distortion at the onset of fault due to highly irregular line currents. The bus voltage and source currents become balanced and sinusoidal within 2-cycles of fault occurrence.

Chapter 5

Conclusions

In this thesis, an active filter model was developed for reactive and harmonic power compensation in a distribution system operating with a weak AC source. The main contribution has been the development and implementation of an active filter controller model in the EMTP simulation program.

Most of the published work deals with strong AC systems. The simulation results validate the operation of an on-line power computation scheme and different tracking control techniques for a weak AC system.

The specific contributions are as follows:

1) Selection of an Active Filter topology suitable for a weak AC system compensation problem

Out of a possible four topologies, the shunt ripple current generator topology was chosen as all the load harmonics are supplied locally causing the distribution bus to supply only sinusoidal fundamental-frequency current. Furthermore the compensation current computation does not closely depend on distribution system parameter values, which may not be accurate or may change in time.

2) Implementation of an on-line power computation algorithm in EMTP

The on-line power computation controller measures the active power consumed by the load, and computes reference currents for the active filter to generate. The benefits of this scheme are its simplicity, accuracy and fast response. The computation clock cycle frequency was kept at six times the line frequency, so the

active filter responds to transient changes within 3 ms.

It is an accurate compensation scheme, as actual reactive and harmonic current requirements are computed digitally and the active filter compensates within marginal error.

3) Comparison of 2-Control Techniques

Two control techniques - hysteresis band control and sliding mode control - were implemented in the AF controller to track reference currents. A performance comparison was made of the two techniques in terms of harmonic content of source current and THD of AC bus voltage. The hysteresis controller provided better tracking of reference currents, but the sliding mode controller performance is comparable at a higher decision frequency.

Both the controllers have the disadvantage of producing a variable switching frequency in the AF inverter. In the sliding mode controller, a maximum limit for the inverter switching frequency can be defined (half of decision frequency). In the hysteresis controller, circuit and control parameters have to be adjusted, in accordance with the switching frequency constraints of the inverter.

For high power applications, where GTO switches are used and the switching frequency constraints are low (< 10 kHz), sliding mode tracking should be preferred as the maximum switching frequency is clearly defined.

For medium power applications, where IGBT switches are used, hysteresis control tracking may be preferred due to better tracking and higher switching frequency constraints (<80 kHz).

4) Behavior under AC-DC transient and fault conditions

The system model was subjected to different AC-DC transient and fault conditions. Its operation was well controlled and stable during transient conditions. In the event of a change in the DC current reference, the AF maintained compensation throughout the transition period; the source currents remained sinu-

soidal and at unity power factor. The AF response was excellent, as it stabilized within a cycle of transition instant.

During AC-DC system faults, load unbalancing occurred in the AC line currents. But the on-line power controller balanced the active load across the three phases, by generating balanced source reference currents. The active filter acts as a medium of exchange of active power between the three source phases. As a result, even during fault conditions, an unbalanced load appears as a balanced three phase load at the AC bus. The bus voltages become unbalanced due to positive, negative and zero sequence currents introduced in the network during faults, but the source currents remain balanced, although not completely at unity power factor.

Recommendations for future work

The following activities should be considered for further research in this area:

- The distribution system model chosen is a simplified one and a more complicated type could be used to analyze the impact of AF compensation and interactions with the system.
- In this work, the costing factor was not taken into account. Therefore, other active filtering techniques such as series compensation or hybrid systems i.e. combination of active and passive filters, may be applied and verified for greater compensation efficiency and lower costs.
- It is desirable, especially in the domain of high power applications that the switching frequency of the AF inverter be constrained within practical limits. Therefore more research is needed in applying tracking techniques such as Pulse Width Modulation (PWM), Sliding-mode control etc. which put an upper limit to the inverter switching frequency.
- And finally it is accepted that simulation results may not be accurate enough for a

thorough understanding of system behavior. It is therefore essential to verify the technique on an experimental setup for a more complete validation.

Inspite of the above shortcomings, this work would be helpful to educators and utility planners designing active filters for practical systems.

References

[1] T. C. Shuter, H. T. Vollkomer Jr. & T. L. Kirkpatrick, "Survey of Harmonic Levels on the American Electric Power Distribution System", IEEE Trans. on Power Delivery, Vol. 4, No. 4, Oct. 1989, pp. 2204-2213.

[2] IEEE Working Group on Power System Harmonics, "Power System Harmonics: An Overview", IEEE Trans. on Power Apparatus and Systems, Vol. 102, No. 8, Aug. 1983, pp. 2455-2460.

[3] A. E. Emanuel, J. A. Orr, D. Cyganski & E. M. Gulachenski, "A Survey of Harmonic Voltages and Currents at the Customer's Bus", IEEE Trans. on Power Delivery, Vol. 8, No. 1, Jan. 1993, pp. 411-421.

[4] H.Sasaki & T.Machida, "A New Method to eliminate AC harmonic Currents by Magnetic Compensation Considerations on basic design", IEEE Trans. on Power Apparatus and Systems, 1971, Vol. PAS-90, No.5, pp. 2009-2019.

[5] L.Gyugyi & E.C.Strycula, "Active AC Power Filters", IEEE-IAS Annual Meeting Record,1976, pp. 529-535.

[6] H. Akagi, Y. Kanazawa & A. Nabae, "Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components", IEEE Trans. on IAS, Vol. IA-20, No.9, May/June 1984, pp. 625-630.

[7] Fang Zheng Peng & Jih-Sheng Lai, "Generalized Instantaneous Reactive Power Theory for Three-Phase Power Systems", IEEE Trans. on Instrumentation and Measurement, Vol. 45, No.1, February 1996, pp. 293-297.

[8] Masatoshi Takeda, Kazuo Ikeda & Yoshiharu Tominaga, "Harmonic Current Compensation with Active Filter", IEEE-IAS, 1987, pp. 808-815.

[9] D. Sutanto, M. Bou-rabee, K. S. Tam & C. S. Chang, "Harmonic Filters for Industrial Power Systems", IEE International Conference on Advances in Power System Control, Operation and Management, November 1991, Hong Kong, pp. 594-598.

[10] G. Ledwich & P. Doulai, "Control Techniques of Active Power Filters", IEE International Conference on Advances in Power System Control, Operation and Management, November 1991, Hong Kong, pp. 582-587.

[11] Fang Zheng Peng, Hirofumi Akagi & Akira Nabae, " A New Approach to Harmonic Compensation in Power Systems - A Combined system of Shunt Passive and Series Active Filters", IEEE-IAS, Vol. 26, No. 6, November/ December 1990, pp. 983-990.

[12] M. Rastogi, N. Mohan & A. A. Edris, "Hybrid-Active Filtering of Harmonic Current in Power Systems", IEEE Trans. on Power Delivery, Vol. 10, No. 4, Oct. 1995, pp. 1994-2000.

[13] P. T. Cheng, S. Bhattacharya & D. M. Divan, "Control of Square-Wave Inverters in High Power Hybrid Active Filter Systems", IEEE Trans. on Industry Applications, Vol. 34, No. 3, May/June 1998, pp. 458-472.

[14] P. G. Barbosa, J. A. Santisteban & E. H. Watanabe, "Shunt Series Active Power Filter for Rectifiers AC and DC Sides", IEE Proc.- Electric Power Appl., Vol. 145, No. 6, Nov. 1998, pp. 577-584.

[15] Suttichai Saetieo, Rajesh Devaraj & David A. Torrey, "The Design and Implementation of a Three-Phase Active Power Filter Based on Sliding Mode Control", IEEE Trans. on Industrial Applications, Vol. 31, No. 5, September/ October 1995, pp. 993-1000.

[16] Bhim Singh, Kamal Al-Haddad & Ambrish Chandra, "A New Control Approach to 3-phase Active Filter for Harmonics and Reactive Power Compensation", IEEE Trans.on Power Systems, Vol. 13, No. 1, Feb. 1998, pp. 133-138.

[17] V. B. Bhavaraju & Prasad N. Enjeti, "Analysis and Design of an Active Power Filter for Balancing Unbalanced Loads", IEEE Trans. on Power Electronics, Vol. 8, No. 4, Oct. 1993, pp. 640-647.

[18] Toshihiko Tanaka & Hirofumi Akagi, "A New Method of Harmonic Power Detection Based on the Instantaneous Active Power in Three-Phase Circuits", IEEE Trans. on Power Delivery, Vol. 10, No.4, October 1995, pp.1737-1742.

[19] Phoivos D. Ziogas, "The Delta Modulation Technique in Static PWM Inverters", IEEE Trans. on Industry Applications, Vol. IA-17, No.2, March/April 1981, pp. 199-204.

[20] Luis T. Moran, Phoivos D. Ziogas & Geza Joos, "Analysis and Design of a Three-Phase Synchronous Solid-State Var Compensator", IEEE Trans. on Industry Applications, Vol. 25, No.4, July/August 1989.

[21] Atsuo Kawamura & Richard Hoft, "Instantaneous Feedback Controlled PWM Inverter with Adaptive Hysteresis", IEEE Trans. on Industry Applications, Vol IA-20, No.4, July/August 1984, pp. 769-775.

[22] Hirofumi Akagi, "Trends in Active Power Line Conditioners", Proceedings of IECON, San Diego, October 92, pp. 19-24.

[23] Fang Zheng Peng, Hirofumi Akagi & Akira Nabae, "A Novel Harmonic Power Filter", IEEE-PESC Record, April 1988, pp. 1151-1158.

[24] Hideaki Fujita & Hirofumi Akagi, "A Practical Approach to Harmonic Compensation in Power Systems - Series Connection of Passive and Active Filters ", IEEE Conference Record IAS, Seattle, October 1990, Vol. 2, pp. 1107-1112.

[25] P.F.Wojciak & David A.Torrey, "The design and implementation of active filter systems using variable structure system concepts", IEEE-IAS Annual Meeting Conf. Record, pp 850-857, 1992.

[26] Vijay Khatri, "EMTP simulation of an HVDC system operating with weak AC systems", April 1995, Concordia University.

[27] N.Mohan, T. M. Undeland, W. P. Robbins, "Power Electronics - Converters, applications, and design", second edition, John Wiley& Sons, Inc., 1996.

[28] W. D. Stevenson, Jr., "Elements of Power System Analysis", McGraw-Hill Book Company, Inc., 1982.

[29] E. W. Kimbark, "Direct Current Transmission", John Wiley & Sons, Inc., 1971.

[30] S. B. Dewan and A. Straughen, "Power Semiconductor Circuits", John Wiley & Sons, Inc., 1984.

[31] L. Gyugyi, T. R. Rietman, A. E. Edris, "The Unified Power Flow Controller: A New Approach to Power Transmission Control", IEEE Transactions on Power Delivery, Vol. 10, No.2, April 1995, pp. 1085-1097.

[32] L. Gyugyi, "Unified power-flow control concept for flexible AC transmission systems", IEE Proceedings-C, Vol. 139, No. 4, July 1992, pp. 323-331.

Appendix A

Harmonic Filter Calculations

A high pass AC filter is connected at the AC bus, to absorb the high frequency switching harmonics injected by the active filter into the source phases. The high pass filter is of small rated capacity (10% of output VA), as the major share of harmonics is compensated by the active filter.

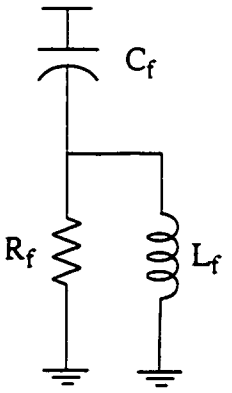


Fig A.1 2^{nd} order High Pass Filter

The filter is tuned to the 12^{th} harmonic, as the lower order harmonics are compensated by the shunt active filter.

At the tuned frequency, i.e. $w_n = n.\ w_f$, where w_f is the fundamental frequency (377 rad),

$$L_{12} \cdot C_{12} = \frac{1}{(w_n)^2} \qquad (A.1)$$

which gives

$$L_{12} \cdot C_{12} = 4.88 \times 10^{-8}$$

The AC filter provides small reactive power compensation, i.e. 10% of output load. For a 1 p.u. power load (1 p.u. power = 100 VA), each phase of the AC filter provides 10/3 VA's of reactive power.

$$V^2 \cdot w_f \cdot C_{12} = 10/3 \qquad \text{(A.2)}$$

where V is the AC bus fundamental rms voltage, and w_f is the fundamental angular frequency.

For a bus voltage of 70.7 V rms,

$$C_{12} = 1.768 \text{ uF} \qquad \text{(A.3)}$$

Substituting the value of C_{12} from (A.3) in (A.1) for L_{12} gives

$$L_{12} = 27.6 \text{ mH}$$

The quality factor, Q is kept low. (Q = 0.7)

$$Q = \frac{R}{n \cdot w_f \cdot L_{12}} \qquad \text{(A.4)}$$

Substituting values in (A.4) yields

$$R = 87.4 \text{ ohms}$$

Appendix B

Controller Calculations

1. Hysteresis Controller

The active filter model analysis can be simplified by considering an independent phase control. The inverter DC bus is powered with a DC split capacitor, the midpoint of which is connected to the system neutral.

The single phase diagram for the circuit is given by:

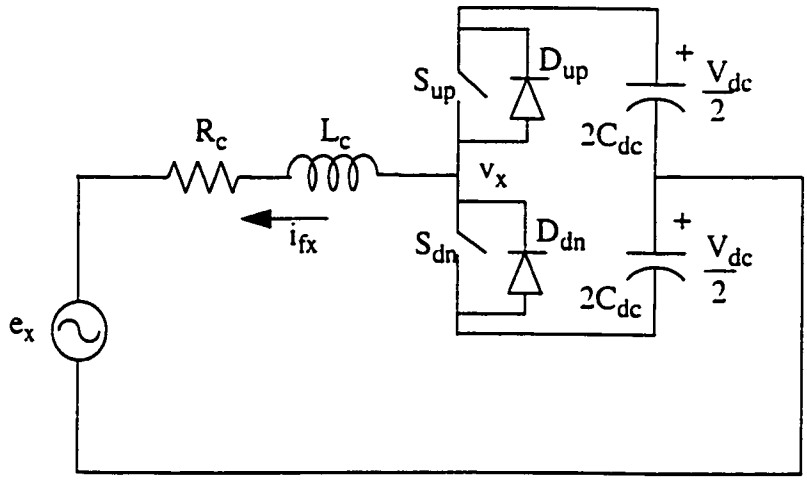


Fig B.1 Single phase equivalent circuit

where e_x is the AC bus phase voltage for phase x (x=a,b,c), v_x is the inverter phase voltage. R_c, L_c comprise the connection impedance. U_x is the switching function for phase x.

U_x = 1 when S_{up} goes ON and S_{dn} goes OFF.

U_x =-1 when S_{dn} goes ON and S_{up} goes OFF.

The circuit equation can be written as

$$v_x - e_x = i_{fx}R_c + L_c\frac{d}{dt}i_{fx} \qquad \text{(B1.1)}$$

where

$$v_x = U_x \times \frac{V_{dc}}{2} \qquad \text{(B1.2)}$$

To shape the signal i_{fx}, the DC bus voltage must be higher than the AC bus voltage i.e.

$$\frac{V_{dc}}{2} \geq e_x(\text{peak}) \qquad \text{(B1.3)}$$

Considering the waveshaping of i_{fx} within the tolerance band around the reference current i^*_{fx}.

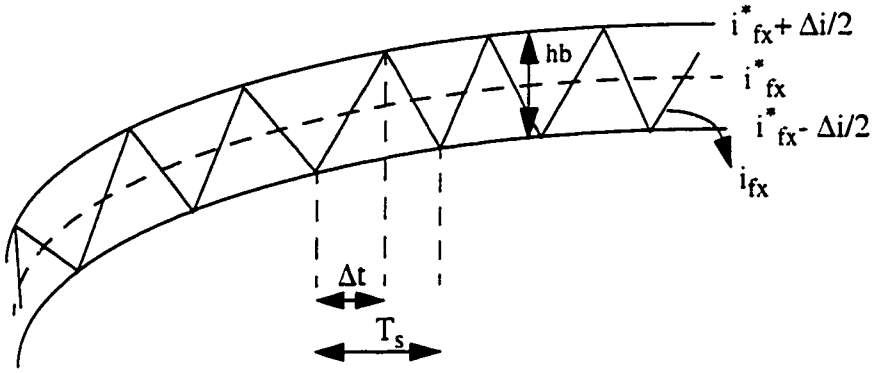


Fig. B.2 Wave-shaping of i_{fx} in hysteresis band

During one switching transition, the circuit equation is given by eq. (B1.1).

Since the connection resistance is small, (to keep conduction losses low, $R_c = 0.1$ ohms), it can be neglected, and the equation reduces to:

$$v_x - e_x = L_c\frac{d}{dt}i_{fx} \qquad \text{(B1.4)}$$

The switching frequency is maximum when the forcing function is highest, i.e. $v_x = V_{dc}/2$ and e_x

goes through zero. Considering these conditions and eq. (B1.2) in eq. (B1.4),

$$\frac{V_{dc}}{2} = L_c \frac{\Delta i_{fx}}{\Delta t} \qquad \text{(B1.5)}$$

where Δi_{fx} is the change in current allowed by the hysteresis limit hb. Since the switching frequency is variable, it would be highest when Δt is approximately equal to the switching time period T_s, i.e.

$$f_{max} = \frac{1}{\Delta t} = \frac{1}{T_S} = \frac{V_{dc}}{2(L_c \cdot \Delta i_{fx})} = \frac{V_{dc}}{2(L_c \cdot hb)} \qquad \text{(B1.6)}$$

Generally, the maximum switching frequency limit is imposed by the semiconductor switches selected for the inverter. For high power applications GTO's could switch upto 5 kHz, whereas IGBTs used for medium power applications switch safely upto 80 kHz.

The DC bus voltage V_{dc} must be greater than twice the AC bus peak voltage so as to modulate the AF phase current about its reference value. A higher value of V_{dc} increases the forcing function, thus increasing the inverter switching frequency. Also the voltage rating of switches goes up, thereby causing an increase in the switching losses. Therefore the DC bus voltage was selected at twice the AC bus peak voltage, i.e. $V_{dc} = 2V_x(peak)$.
Since $V_x(peak) = 100V$, $V_{dc} = 200V$.

The hysteresis bandwidth hb was chosen at 10% of I_{base}, so as to have a good tracking of reference currents.

Therefore,

$$hb = \Delta i_{fx} = 10\% \text{ of } I_{base}$$
$$= 10\% \text{ of } 1A = 0.1 \text{ A}$$

Considering the case for an IGBT inverter, having maximum switching frequency at 80 kHz, the connection inductance L_c can be computed from (B1.6) as

$$L_c = \frac{V_{dc}}{2(f_{max} \cdot hb)} \qquad \text{(B1.7)}$$

which gives an L_c value of 12.5mH.

Simulations show that an L_c value of 10 mH keeps the inverter average switching frequency to 8.25 kHz. Eq. (B1.6) gives an approximate starting estimate for the L_c value, the actual choice would be based on further simulation work.

2. Sliding Mode Controller

Considering the phase circuit diagram shown in Fig B.1., the controller has to modulate the AF current i_{fx} about its reference current i^*_{fx}. The system state is defined, to consist of the AF line currents i_{fx} (x=a,b,c). The desired state trajectory, or sliding surface is obtained from the on-line power computation scheme which computes the AF reference currents i^*_{fx}.

For the system state to be on the desired trajectory, the equation for the sliding surface is written as

$$s_x = i^*_{fx} - i_{fx} = 0 \qquad \text{(B2.1)}$$

To assure that the system state be maintained on the sliding surface, a natural control which satisfies

$$s_x \cdot \dot{s}_x \leq 0 \qquad \text{(B2.2)}$$

must exist.

With the concept of equivalent control, the above equation can be satisfied for all state values if

$$\dot{s}_x = 0 \tag{B2.3}$$

at all instants.

The circuit equation for the phase circuit states:

$$v_x = e_x + L_c \frac{d}{dt} i_{fx} + i_{fx} R_c \tag{B2.4}$$

where

$$v_x = U_x \cdot \frac{V_{dc}}{2} \tag{B2.5}$$

The switching function U_x for phase x is given by:

$U_x = 1$ when S_{up} goes ON and S_{dn} goes OFF.

$U_x = -1$ when S_{dn} goes ON and S_{up} goes OFF.

Solving for di_{fx}/dt from eq. (B2.4) and neglecting R_c

$$\frac{d}{dt} i_{fx} = \dot{i}_{fx} = \frac{-1}{L_c} \cdot \left(e_x - U_x \cdot \frac{V_{dc}}{2} \right) \tag{B2.6}$$

Substituting di_{fx}/dt in eq. (B2.1), we get

$$\dot{s}_x = i^*_{fx} + \frac{1}{L_c} \cdot \left(e_x - U_x \cdot \frac{V_{dc}}{2} \right) \qquad \text{(B2.7)}$$

From equivalent control, equating $\dot{s}_x = 0$, and solving for the equivalent switching function U_{eqx} gives

$$U_{eqx} = \left(i^*_{fx} + \frac{1}{L_c} \cdot e_x \right) \cdot \frac{2L_c}{V_{dc}} \qquad \text{(B2.8)}$$

For the state to remain on the desired trajectory, U_{eqx} should be within the natural bounds of the system, i.e. $-1 \leq U_{eqx} \leq 1$.

Eq. (B2.7) is linear with respect to U_x.

Therefore,

$$\text{If } (U_x < U_{eqx}) \quad \text{then} \quad (\dot{s} > 0) \qquad \text{(B2.9a)}$$

and

$$\text{If } (U_x > U_{eqx}) \quad \text{then} \quad (\dot{s} < 0) \qquad \text{(B2.9b)}$$

Since the switching function U_x can be either 1 or -1,

$$\text{If } (U_x = -1) \quad \text{then} \quad (U_x < U_{eqx}) \therefore (\dot{s} > 0) \qquad \text{(B2.10a)}$$

and

$$\text{If } (U_x = 1) \quad \text{then} \quad (U_x > U_{eqx}) \therefore (\dot{s} < 0) \qquad \text{(B2.10b)}$$

To satisfy Eq. (B2.2) at all instants,

i.e.

$$\text{If } (\dot{s} > 0) \text{ then } (s < 0) \text{ or } (U_X = -1)$$

and

$$\text{If } (\dot{s} < 0) \text{ then } (s > 0) \text{ or } (U_X = +1)$$

Therefore, the switching logic of the sliding mode controller can be stated as:

$$\begin{aligned} &\text{If } (s<0) \text{ then } (U_x = -1) \\ &\text{\& if } (s>0) \text{ then } (U_x = +1) \end{aligned} \qquad \text{(B2.11)}$$

The system uses constant frequency decision control in which the status of s is checked at regular time intervals and appropriate switching signals are generated.

The peak to peak ripple, Δi_{fx} of the AF current, during one switching period is given by

$$\Delta i_{fx} = i^*_{fx} - i_{fx} = i^*_{fx} + \int_0^T \frac{e_X}{L_C} - \left(U_X \cdot \frac{V_{dc}}{2L_C} \right) dt \qquad \text{(B2.12)}$$

where i_{fx} is substituted from eq. (B2.6).

Appendix C

List of Publications

Papers published on this research:

- Rachit Arora, V. K. Sood, *"Development of EMTP Based Model of an Active Filter for Distribution System Studies"*, Canadian Conference on Electrical and Computer Engineering, Waterloo, May 1998, pp. 77-80. (4 pages)

- V. K. Sood, Rachit Arora, *"Development of EMTP Based Model of an Active Filter for Distribution System Studies"*, IEE Int. Conf. on Power Electronics and Variable Speed Drives, Publication #456, PEVD'98, London, UK., September 98, pp. 181-186. (6 pages)