

**Application of Network Transposition in the
Design of OTA-C Filters and Oscillators**

Zhigang Tang

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ABSTRACT

Application of Network Transposition in the Design of OTA-C Filters and Oscillators

Zhigang Tang

Recent advances in analog integrated circuit and signal processing have shown that the current-mode approach is superior to the voltage-mode in terms of its wide bandwidth, high speed, low voltage and power. As a wide range of voltage-mode analogue circuits already exist, a straightforward method of converting these voltage-mode circuits to current-mode circuits would be very useful. The network transposition, introduced by Bhattacharyya and Swamy as early as in 1971, provides a perfect solution to this question of conversion from voltage-mode to current-mode circuits.

A vast body of literature already exists concerning voltage-mode OTA-C filter structures. At the same time, many current-mode OTA-C filter structures are being reported in the literature. These two apparently independent areas of research and development could be unified by the application of the principle of network transposition. For this reason, an intensive investigation on the OTA-C structures is conducted. The result of this investigation shows that transposition relationship could be used to advantage in deriving current-mode filter structures from the voltage-mode filter

structures and vice versa. The principle of transposition has been extended to oscillator circuits to derive new OTA-C oscillator structures from known ones. The concept of transposition has been extended to differential input dual-output (DIDO) structures, since such structures can increase the common-mode rejection ratio, eliminate the even-order harmonic distortion components and reduce the effects of power supply noise. The theoretical work presented in the thesis is verified by simulation results as well as by practical circuits using discrete resistors, capacitors and OTA devices. In addition, an oscillator is fabricated in a 0.18 μm CMOS process to further verify the validity of network transposition. The measurement result shows good agreement with the theoretical analysis.

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Nomenclature

VLSI: very large scale integration

DIDO: differential input dual-output

BJT: bipolar junction transistor

FET: field effect transistor

OA: operation amplifier

OTA: operational transconductance amplifier

OTA-C: operational transconductance amplifier and capacitor

MHz: Mega (10^6) hertz

GHz: Giga (10^9) hertz

V_{th} : threshold voltage of transistor

V_{od} : overdrive voltage of transistor

β : MOS transistor gain factor

K_p : process gain factor

VCVS: voltage control voltage Source

VCCS: voltage control current Source

CCVS: current control voltage Source

CCCS: current control current Source

L: inductor

C: capacitor

R: resistor

MOSFET: MOS field effect transistor

CMOS: complementary MOSFET

NMOS: n-channel MOSFET

PMOS: p-channel MOSFET

IAM: indefinite admittance matrix

ppm: parts per million (10^{-6})

V_{pp} : peak to peak voltage

C_{gd} : gate-drain capacitance of transistor

OTAN: n-type input circuit

OTAP: p-type input circuit

pf: pico (10^{-12}) farad

nF: nano (10^{-9}) farad

ns: nano (10^{-9}) second

μm : micro (10^{-6}) meter

DIP: dual in-line IC package

Ω : angular frequency of oscillation

THD : total harmonic distortion

IM : inter-modulation

IIP3 : input-referred 3rd order intercept point

Chapter 1 Introduction

1.1 Motivation

Active filters and oscillators are basic building blocks in many electronic systems such as telecommunication, consumer electronics and instrumentation system. The trend in modern integrated circuits is to incorporate as many system blocks as possible on a single chip, ultimately progressing towards a complete system on chip (SoC). Operational transconductance amplifier (OTA)-C filters are the most common continuous time analog filters used for monolithic integration on a chip. Compared to the conventional operation amplifier (OP-AMP)-based circuits, OTA-based circuits possess several major advantages.

1. OTAs may be used at much higher frequency ranges. Depending on the technology used, they can be made to function in the range from tens to hundreds of MHz.
2. OTA-based circuits and digital signal processing circuits can be fabricated on the same semiconductor chip. Thus, a hybrid signal processing system can be truly produced on one integrated system. This greatly reduces the cost and size, and at the same time increases the reliability of the hardware.
3. OTA-based circuits are electronically tunable.

Hence, in this thesis, we concentrate only on OTA-C filters and OTA-C oscillators.

On the other hand, the design of current-mode circuits is another topic of current interest. Driven by the demand for low power consumption in practical applications, as well as consequence of the improvements in the technology process, the oxide thickness and channel length have been decreasing. This has led and will continue to lead to the scaling down of the supply voltage. However, the threshold voltage V_{th} of transistors cannot be scaled down proportionally. Therefore, many conventional voltage mode analog circuits become nonfunctional in low voltage environment. There is thus a growing need for new, low voltage, low power analogue circuit techniques. One solution to finding alternative, preferably simpler, circuit realizations is to use current signals rather than voltage signals for signal processing. First, BJTs and FETs are essentially current output devices. For this reason, integrated current-mode systems are easier to be realized at the transistor level than the conventional voltage-mode ones. Moreover, in terms of signal operations, implementations in current-mode are simpler. For instance, addition / subtraction can be done by injecting / extracting current signals to / from circuit node; multiplication by a constant can be realized by properly setting the ratio of a current mirror. Usually, simpler realization results in a higher speed, and lower voltage and power. However, too often electronic engineers tend to think in voltage terms rather than current, and it is only now that the analogue designer is realizing the full benefits of the current-mode approach. As a wide range of voltage-mode analogue circuits already exist, a straightforward method of converting these voltage-mode circuits to

current-mode circuits would be very useful. The network transposition, proposed by Bhattacharyya and Swamy as early as in 1971, can provide a perfect solution to voltage/current mode transformations [1]. It is worthy to note that at the time of its introduction in 1971, the advantages of network transposition were not fully apparent, particularly since the monolithic OP-AMP was the only choice for analog IC designers and the other active devices, namely, VCCS, CCCS, CCVS were not commercially available yet. The fast developments of various analogue building blocks such as OTAs, current conveyors and transimpedance amplifiers in the recent years, coupled with a strong demand for current-mode signal processing, have lead us to reconsider this important circuit principle as a powerful tool in analogue circuit design.

1.2 Current mode OTA-C filter realization techniques in the past decade

Current-mode OTA-C filter design has received much attention in research in the past decade. This is confirmed by the wealth of literature on this area. Just as in the case of a voltage-mode filter, the biquad is also the building block for the high-order current-mode filters. In 1996, a method of systematically generating current-mode biquad structures was proposed by Sun et al [2]. In Fig.1.1, signal flow diagrams are used to illustrate the four general two integrator loop structures. Signal operations such as integration, multiplication and summation are implemented in current-mode to realize the

desired function for every loop. Note that the feedback loops in these structures can be open, i.e. $K_{ij} = 0$, or direct connection, i.e. $K_{ij} = 1$, or have any other gain. A variety of filter structures can be derived from these signal flow diagrams by changing the value of K_{ij} . Moreover, input / output current signals can be injected / taken at any circuit node. This will also result in different transfer functions. The derivations of the transfer functions involve complicated circuit node voltage/current calculations and will not be discussed here. A further investigation on these structures will be given in Chapter 3.

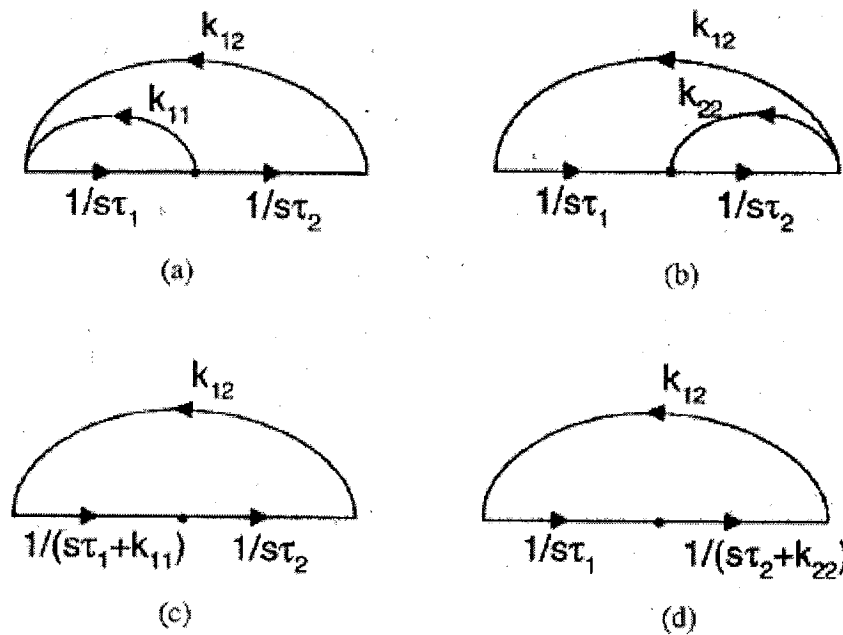


Fig. 1.1 Illustration of two integrator loop structures

Once biquad structures have been designed, a popular way of realizing a higher-order filter is to cascade the biquad structures, in view of the modularity of the structure and the simplicity of design and tuning. For a given transfer function, we first factorize it into lower-order functions and then realize these functions using the known

first and second-order filter structures. For lowpass and highpass filters, we can simply cascade lower-order lowpass and highpass sections, respectively. For the bandpass filters we can either use both lowpass and highpass sections, or only bandpass sections. Finally we cascade the designed sections and the cascaded circuit gives the desired transfer function. The cascade method however suffers from the disadvantage of having very high sensitivities to component tolerances.

It has been recognized that resistively terminated lossless LC ladders have very low sensitivity. Again, similar to the voltage mode filter, current mode OTA-C filter can thus be designed by simulating passive LC ladders to achieve low sensitivities[3-8]. This simulation technique can be broadly classified into two categories: component substitution and signal simulation. In the signal simulation method, the circuit equations that describe the topology of the passive ladder structure are first written. These original equations are of the mixed current and voltage type. For current-mode operation, we convert these mixed equations to the current-only equivalent and realize the corresponding current signal flow diagram using current mode OTA-C building blocks. Note that in both the component substitution method and signal simulation method, there are two types of components, which are resistors and inductors. They need to be substituted by OTAs and/or ground capacitors because of their poor accuracy and large size in IC implementation. As shown in Fig.1.2 (a) and (b), either the grounded or floating resistor can be realized by one OTA. While Fig.1.3(a) shows that simulating the grounded inductor needs two OTAs and one capacitor, Fig.1.3(b) indicates that the

floating one requires three OTAs and one capacitor.

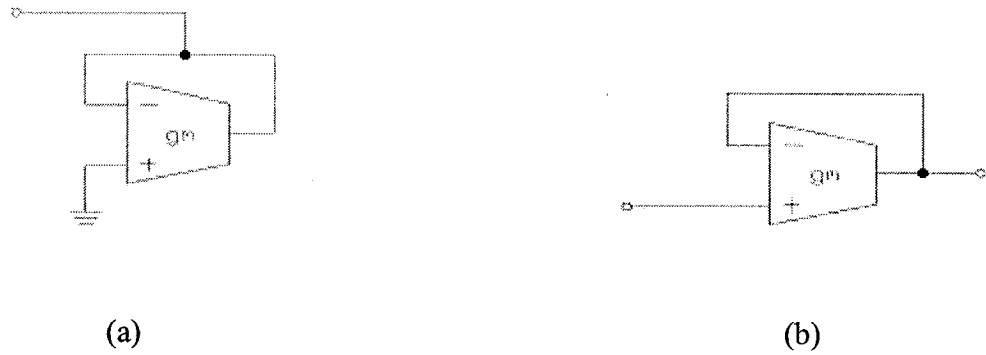


Fig. 1.2 OTA simulation of (a) grounded resistor and (b) floating resistor

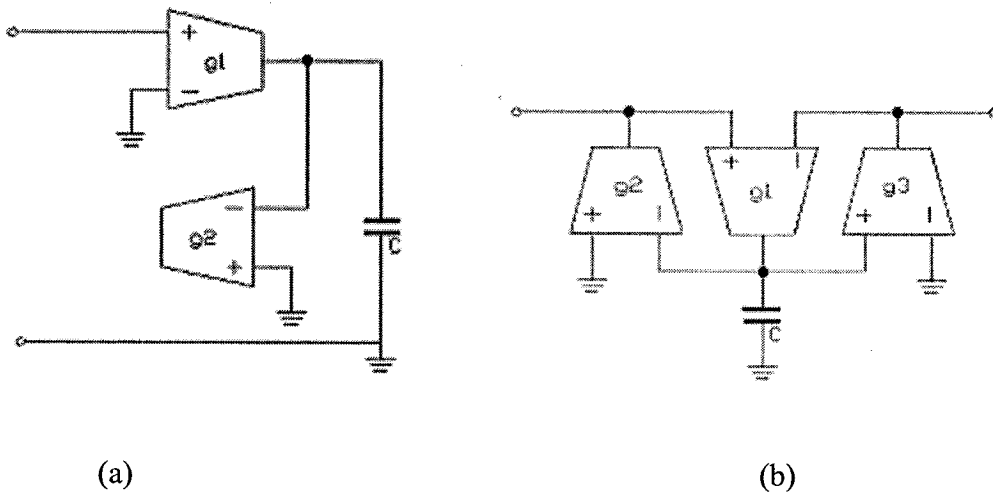


Fig. 1.3 OTA simulation of (a) grounded inductor and (b) floating inductor.

Obviously, ladder simulation OTA-C filters have to use more OTA devices than other filter structures do. Consequently, there is more OTA parasitic impedances. These parasitic impedances and noise have a negative impact on the performance of the filter. Hence, this structure may not be suitable for low power high frequency application.

A very popular higher-order current-mode filter structure is the multiple loop feedback

structure [9], which was proposed by Sun et al in 1997. This type of filter enjoys a simple structure and still displays low sensitivity to component tolerances, compared with the cascade case. However, a high order feedback coefficient matrix F is involved to reflect the filter structure. As shown in Fig.1.4, the matrix element $f_{ij}=I_{fi}/I_{oj} \neq 0$ if there exists feedback between I_{fi} and I_{oj} ; otherwise, $f_{ij}=0$. The non-zero current coefficient f_{ij} can be realized as $f_{ij}=g_{ij1}/g_{ij2}$, or simply as a direct connection if $f_{ij}=1$.

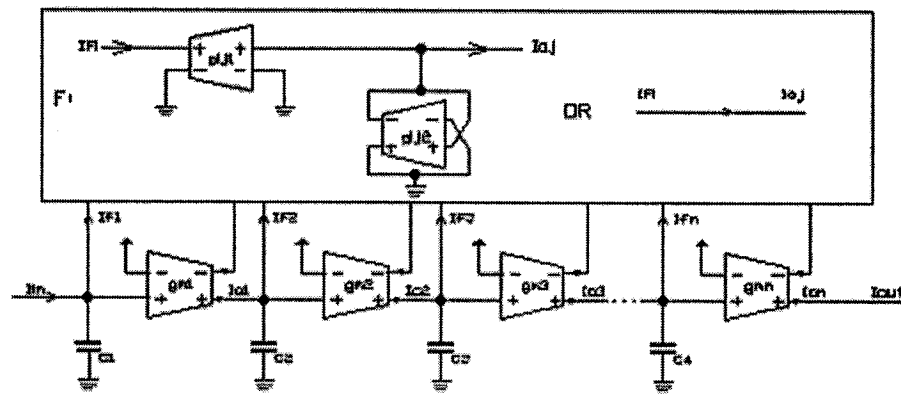


Fig. 1.4 Current-mode multiple loop feedback OTA-C model

According to the one-to-one correspondence between the feedback matrix F and the filter architecture for a given order, the generation of filter structures can be accomplished by finding all the combinations of the non-zero elements of F . If the output current of any integrator is fed back to some circuit node, then F has one and only one non-zero element in each column. Therefore, for the general n th-order case there are $n!$ possible combinations. Hence, when the order of the filters is higher than 4, solving these matrix equations becomes very difficult. Moreover, the non-canonical realizations of the

filters (i.e. $f_{ij} \neq 1$) also make the solutions mathematically more complicated.

Using the result in [1] on network transposition, it has been shown that a current-mode three-terminal filter could be very simply implemented from an associated voltage-mode filter [8,10,11]. However, the use of network transposition on networks containing four-terminal (i.e., differential input, dual-output) OTAs still remains unexplored. By the application of the principle of network transposition on existing voltage-mode three-terminal or four-terminal OTA-C filters, we can generate the corresponding current-mode OTA-C filters. These new structures have the same sensitivities as their voltage-mode counterparts with respect to the corresponding parameters. In fact, we will show that all the OTA-C current-mode filters proposed by earlier authors are nothing but the transposes of the well known voltage-mode OTA-C filters. The concept of transpose can also be used to advantage in deriving new OTA-C oscillator circuits from existing OTA-C oscillator circuits. These new structures have the same characteristic equations (have the same conditions for oscillation and frequencies of oscillation) as those of the corresponding OTA-C oscillators from which the new ones have been generated.

1.3 Scope of the thesis

The primary aims of this thesis are to investigate the feasibility of applying network transposition to design current-mode OTA-C filters from the well-known voltage-mode

OTA-C filters as well as to derive new OTA-C oscillators from known OTA-C oscillators, and then to implement and test some of the derived circuits. Besides, design techniques in low voltage environment need several important considerations. In order to address the above objectives, the thesis is concerned with the following tasks.

1. Presentation of the network transpose of a dual-input dual-output OTA.
2. Generation of new structures of current-mode OTA-C filters, and implementation using discrete components.
3. Generation of new structures of OTA-C oscillator, and implementation using discrete components as well as CMOS VLSI technology.
4. Verifications using computer-aided simulation tools and testing of a fabricated chip obtained through the Canadian Microelectronics Corporation (CMC).

1.4 Thesis Organization

Chapter 2 gives a review of the concept of network transposition and derives the transpose for a dual-input dual-output (DIDO) OTA. This derivation is very useful in the design of DIDO OTA-C circuit structures. A thorough investigation is conducted in Chapter 3 to show the close relationship that exists among the OTA-C voltage-mode and current-mode filter structures that have been proposed in the literature. Furthermore, new current-mode DIDO OTA-C filter structures are derived using network transposition. Chapter 4 presents the application of network transposition in deriving new OTA-C

oscillator structures from known oscillator structures. Chapter 5 describes the implementation of three-terminal OTA-C filters and oscillators using commercial chip LM13700 and discrete resistors and capacitors. Chapter 6 focuses on the IC realization of a current-mode four-terminal OTA-C bandpass filter and a four-terminal OTA-C oscillator. Especially, low-voltage IC design techniques are discussed in detail. Printed circuit board layout is also illustrated here. In Chapter 7 two common simulation tools such as Hspice and SpectreRF are introduced. The simulation results concerning both the filters and oscillators are given. Measurement results on the fabricated oscillator chip are also presented in this chapter. Chapter 8 contains concluding remarks and recommendations for future work.

Chapter 2 Fundamentals of Network Analysis and Network Transposition

2.1 Introduction

This chapter will start with a review of the concept of network transposition. Then, the transposes of three-terminal active elements including VCVS, VCCS, CCVS and CCCS are described in brief. Following this basic introduction, a practical application of network transposition will be given as an example. Finally, short circuit admittance matrix of a DIDO OTA is derived.

2.2 Basic Definitions and Related Expressions

A linear electrical network may be considered as an interconnection of linear elements which may be passive, active, reciprocal or nonreciprocal. A two-port network, as the name indicates, is a network that consists of two ports. For each port, the current entering one terminal shall be exactly equal to the current existing out of the other terminal, i.e. $I_1=I_2$, $I_3=I_4$ as shown in Fig.2.1.

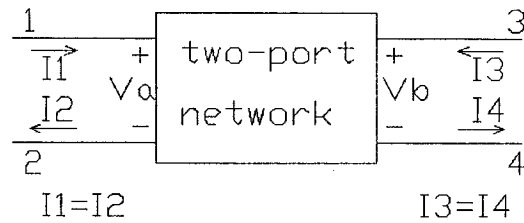


Fig. 2.1 Two-port network model

Two-port network can be treated as a black box with no independent current/voltage source(s) residing inside the black box. Also all initial conditions are assumed to be zero.

A two-port network can be completely specified by a set of four parameters. This set of four parameters could be any one of the sets of y -, z -, h -, or ABCD parameters. All these are network characterizations based on the voltages and currents appearing at the terminals of the two-port. Here we will adopt y - parameters for the convenience of discussing network transposition. In the general case of a circuit with $n+1$ nodes, the n independent equations, when the $n+1$ th node has been chosen as the reference node, with $V_{n+1}=0$, are as follows:

$$I_1 = y_{11}V_1 + y_{12}V_2 + \dots + y_{1n}V_n$$

$$I_2 = y_{21}V_1 + y_{22}V_2 + \dots + y_{2n}V_n$$

.....

$$I_n = y_{n1}V_1 + y_{n2}V_2 + \dots + y_{nn}V_n$$

This set of equations can be written in matrix form, which is

$$\begin{bmatrix} y_{11} & y_{12} & \cdots & y_{1n} \\ y_{21} & y_{22} & \cdots & y_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ y_{n1} & y_{n2} & \cdots & y_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \cdots \\ V_n \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \cdots \\ I_n \end{bmatrix}$$

or simply $[y] [V] = [I]$, where $[y]$ is an $n \times n$ matrix, and $[V],[I]$ are column matrices. We will see in the following that the y - parameters are very useful in the definition of network transposition.

2.3 Network Transposition Overview

Consider two linear networks such that their short circuit admittance matrices are the transposes of each other, then the two networks are said to be transposes of each other[1]. The operation of finding a transposed network for a given network is called transposition.

It is obvious that any reciprocal network such as passive RLC network is the transpose of itself. Hence, only the nonreciprocal networks are discussed here.

Assume a general linear network N with (1,0) as the input port and (2,0) as the output port, and having $(n-2)$ internal nodes as shown in Fig.2.2.

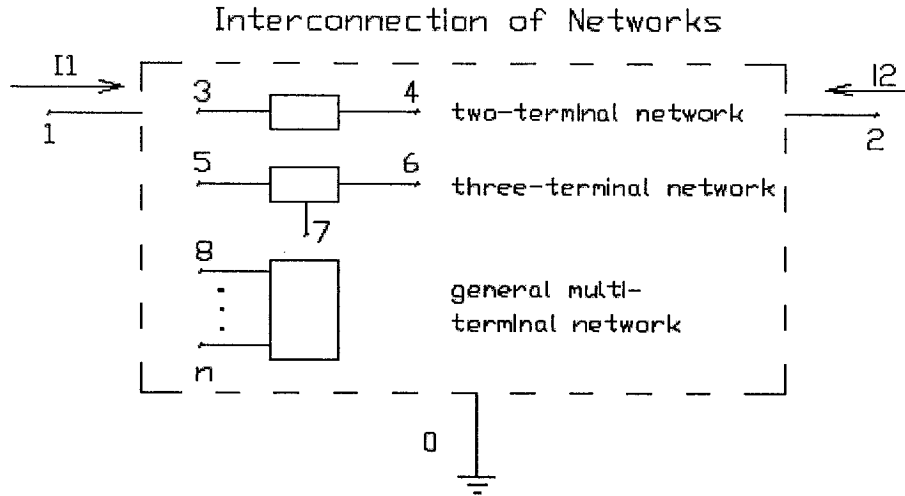


Fig. 2.2 A general linear network N

This network may consist of both active and passive elements, which may be reciprocal or nonreciprocal. The indefinite admittance matrix (IAM) of such an $(n+1)$ terminal network may be written in the form $[Y]_N = [Y]_R + [Y]_{NR}$, where $[Y]_R$, the reciprocal part, is usually due to the passive elements but may also contain contribution from active reciprocal elements such as tunnel diodes; $[Y]_{NR}$, the nonreciprocal part, usually arises from the active elements but may also be due to passive nonreciprocal elements such as ideal gyrators. However, many of the active nonreciprocal elements do not possess an IAM. In this case we can always obtain an IAM by modifying the given nonreciprocal elements. As an example, the modification is shown in Fig.2.3(a) for a 3-terminal non-reciprocal element that does not possess an IAM. This modification does not alter the properties of the original network N . It should be mentioned that these resistors may not be required at all the three terminals. If we now replace N_a in Fig.2.3(a)

with N_b in Fig.2.3(b) such that its IAM is the transpose of N_a , then the IAMs of networks in Figs.2.3(a) and (b) are transpose of each other. Also, the nonreciprocal elements NRA and NRB in Figs.2.3(a) and (b) are transposes of each other.

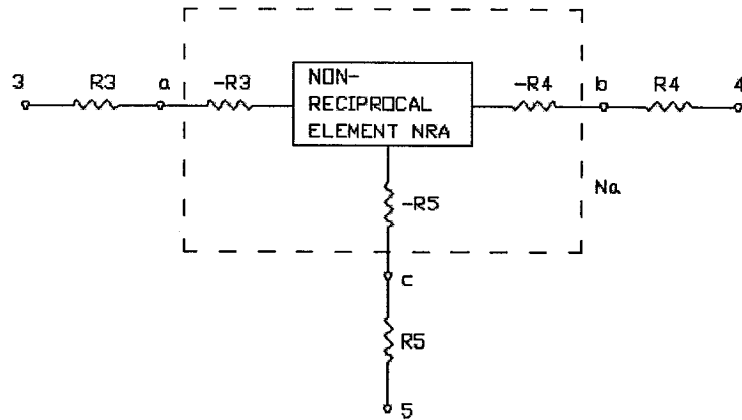


Fig. 2.3(a) The modified nonreciprocal element

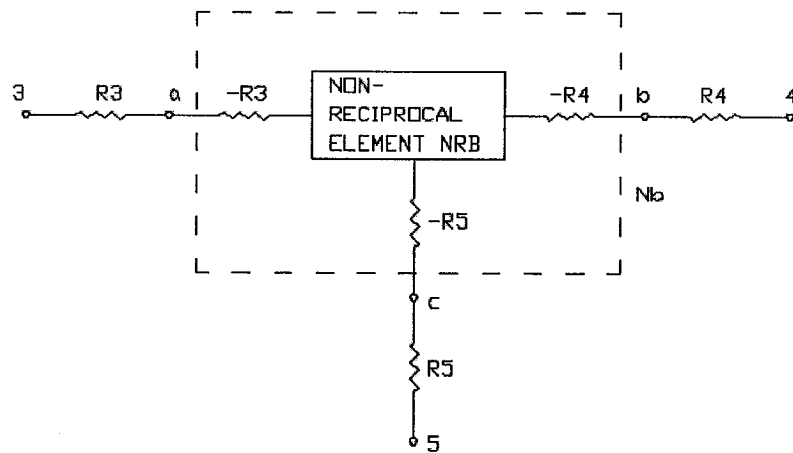


Fig.2.3(b) The transpose of the nonreciprocal network in Fig.2.3(a)

Similarly the other nonreciprocal elements in the network N are replaced by their transposes. By doing so, the original reciprocal part $[Y]_R$ of the given network N is

unchanged, while the nonreciprocal part $[Y]_{NR}$ is replaced by its transpose. Hence we get a new network N_t for which the IAM is the transpose of that of N . Let us now denote the definite admittance matrices of the networks N and N_t by $[Y]$ and $[Y]_{Nt}$, with 0 as the reference terminal. The admittance description for the definite poles is:

$$\begin{bmatrix} I_1 \\ I_2 \\ \dots \\ I_{n-1} \\ I_n \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & \dots & Y_{1(n-1)} & Y_{1n} \\ Y_{21} & Y_{22} & \dots & Y_{2(n-1)} & Y_{2n} \\ \dots & \dots & \dots & \dots & \dots \\ Y_{(n-1)1} & \dots & \dots & \dots & Y_{(n-1)n} \\ Y_{n1} & \dots & \dots & \dots & Y_{nn} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ \dots \\ V_{n-1} \\ V_n \end{bmatrix} \quad (2.1)$$

Note that only the nodes 1,2 are external nodes and the others are internal nodes, so $I_3=I_4=\dots=I_n=0$. Now partitioning the matrices as follows:

$$\begin{array}{c} \mathbf{I}' \\ \mathbf{I}_2' \end{array} \begin{bmatrix} I_1 \\ I_2 \\ \dots \\ I_{n-1} \\ I_n \end{bmatrix} = \begin{array}{cc} \mathbf{Y}_{11}' & \mathbf{Y}_{12}' \\ \mathbf{Y}_{21}' & \mathbf{Y}_{22}' \end{array} \begin{bmatrix} Y_{11} & Y_{12} & \dots & Y_{1(n-1)} & Y_{1n} \\ Y_{21} & Y_{22} & \dots & Y_{2(n-1)} & Y_{2n} \\ \dots & \dots & \dots & \dots & \dots \\ Y_{(n-1)1} & \dots & \dots & \dots & Y_{(n-1)n} \\ Y_{n1} & \dots & \dots & \dots & Y_{nn} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ \dots \\ V_{n-1} \\ V_n \end{bmatrix} \begin{array}{c} \mathbf{V}_1' \\ \mathbf{V}_2' \end{array}$$

The matrix equation 2.1 can be written as :

$$\begin{bmatrix} I_1' \\ I_2' \end{bmatrix} = \begin{bmatrix} Y_{11}' & Y_{12}' \\ Y_{21}' & Y_{22}' \end{bmatrix} \times \begin{bmatrix} V_1' \\ V_2' \end{bmatrix}, \text{ i.e. } I_1' = Y_{11}'V_1' + Y_{12}'V_2', \quad I_2' = Y_{21}'V_1' + Y_{22}'V_2'.$$

Since $I_2' = \begin{bmatrix} I_3 \\ \dots \\ I_n \end{bmatrix} = \begin{bmatrix} 0 \\ \dots \\ 0 \end{bmatrix}$, it can be shown that $I_1' = [Y_{11}' - Y_{12}'(Y_{22}')^{-1}Y_{21}'] \times V_1'$, where

I_1' and V_1' represent the port currents and voltages of the network N . Hence the short-circuit admittance matrix of the network N is $[y]_N = Y_{11}' - Y_{12}'(Y_{22}')^{-1}Y_{21}'$. On the

other hand, the definite admittance matrix of the network N_t is the transpose of that of N ,

$$\text{so } [Y]_{N_t} = [Y]_N^t, \quad \text{i.e. } \begin{bmatrix} Y_{11t}' & Y_{12t}' \\ Y_{21t}' & Y_{22t}' \end{bmatrix} = \begin{bmatrix} Y_{11}' & Y_{12}' \\ Y_{21}' & Y_{22}' \end{bmatrix}^t = \begin{bmatrix} (Y_{11}')^t & (Y_{21}')^t \\ (Y_{12}')^t & (Y_{22}')^t \end{bmatrix}, \quad \text{where}$$

$Y_{11t}', Y_{12t}', Y_{21t}', Y_{22t}'$ are the partition parts of the network N_t . Similar as the case of

network N , the short-circuit admittance matrix of N_t is

$$[y]_{N_t} = Y_{11t}' - Y_{12t}'(Y_{22t}')^{-1}Y_{21t}' = (Y_{11}')^t - (Y_{21}')^t\{(Y_{22}')^t\}^{-1}(Y_{12}')^t = [y]_N^t. \quad \text{Thus, the}$$

network N_t is the transpose of the network N . Hence, given a network N , its transpose N_t

can be obtained by simply replacing all the nonreciprocal elements in N by their

corresponding transposes, and keeping the reciprocal elements unchanged. This operation

has been called network transposition by Bhattacharyya and Swamy [1].

Based on the network N and its transpose N_t , we can make the following interesting observation:

- 1) The forward voltage transfer function and current transfer function of network N become the reverse current transfer function and voltage transfer function of N_t , and vice versa.
- 2) Driving point function of the two networks are the same.
- 3) The sensitivities of the corresponding network functions for the original and the transposed networks are the same with respect to the corresponding network parameters.

The above results have been extended to a network with n inputs and m outputs[1].

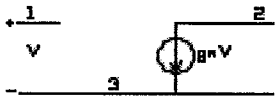
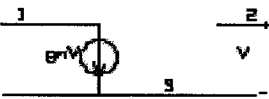
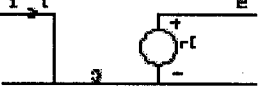
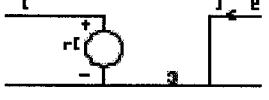
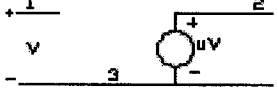
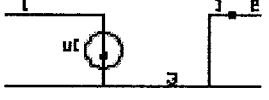
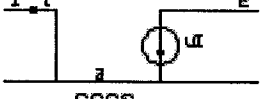

This extension enables us to derive fully differential filter structures in the chapter 3.

Since most passive elements are reciprocal, the transposition operation can be

done by merely replacing each of the active elements in the network by its transpose.

The transposes of important three-terminal active elements, namely, VCVS, VCCS, CCVS, CCCS have been derived and these are given in Table 2.1.

Table 2.1: Active Three-terminal Elements and Their Transposes [1]

ACTIVE ELEMENT	CORRESPONDING TRANSPOSE
 <p style="text-align: center;">VCCS</p>	 <p style="text-align: center;">VCCS</p>
 <p style="text-align: center;">CCVS</p>	 <p style="text-align: center;">CCVS</p>
 <p style="text-align: center;">VCVS</p>	 <p style="text-align: center;">CCCS</p>
 <p style="text-align: center;">CCCS</p>	 <p style="text-align: center;">VCVS</p>

2.4 Practical application of network transposition

At the time this very important concept of transposition was introduced in 1971[1], commercial devices to realize VCCS, CCCS and CCVS were not available yet. Hence, this important circuit principle was not applied in practice in analog current-mode IC design. Now that the OTA has become a very popular current-mode building block, let us see how the beauty and simplicity of network transposition can help us in deriving current-mode circuits. The symbol and the equivalent circuit of a three-terminal OTA are shown in Figs.2.4 (a) and (b) respectively.

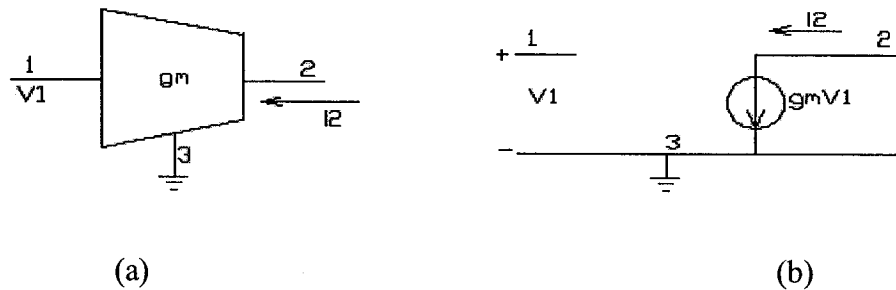


Fig. 2.4(a) The symbol of OTA and (b) its equivalent circuit

From the table 2.1, it is seen that the transpose of a three-terminal OTA is itself with its input and output terminals reversed, which leads to the transposed OTA in Fig.2.5.

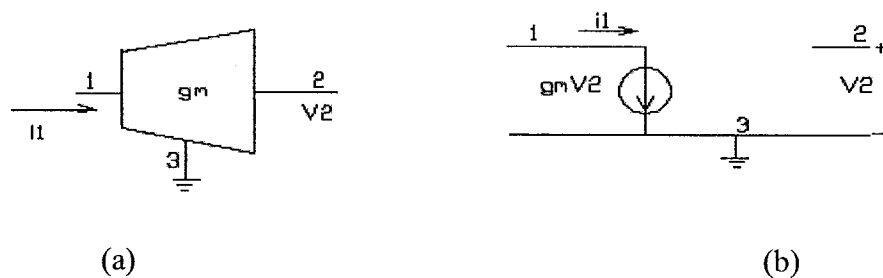


Fig. 2.5(a) The symbol of transposed OTA and (b) its equivalent circuit

As an example, consider the voltage-mode filter, filter A, shown in Fig.2.6 employing a resistor, two capacitors and a three-terminal OTA.

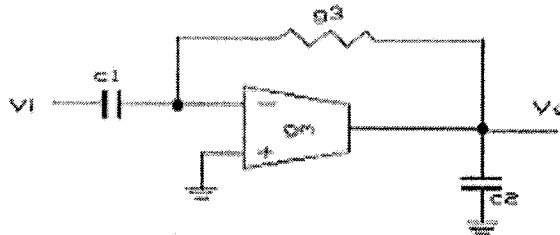


Fig. 2.6 Voltage-mode filter A

Following the procedure of transposition operation, first we keep the passive elements, i.e. resistor and capacitors unchanged and reverse the ports of the active element OTA. Then we interchange the input and output ports of this filter. The transposed network, a current-mode filter, shown in Fig.2.7 results.

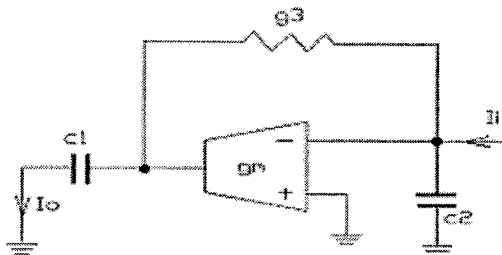


Fig. 2.7 Current-mode filter B, the transpose of the filter A

It can easily be verified that the voltage transfer function of filter A will be the same as the current transfer function of filter B, namely,

$$\frac{V_o}{V_i} = \frac{I_o}{I_i} = \frac{(g_3 - g_m)C_1s}{C_1C_2s^2 + g_3(C_1 + C_2)s + g_mg_3} .$$

Thus, if we need to design a current-mode filter with a given transfer function, what we can do is to simply find a voltage-mode filter structure having the same transfer function. That, most likely, will be much easier than designing a current-mode filter starting from scratch since a wide range of voltage-mode filter structures already exist. On the other hand, it has been known that the differential structures can increase the common-mode rejection ratio, eliminate the even-order harmonic distortion components and reduce the effects of power supply noise. Hence, these structures are most widely utilized in today's continuous-time integrated filter design. Consequently, a question naturally arises as to what the transpose a four-terminal OTA is. We now derive the transpose of a four-terminal OTA.

2.5 The transpose of four-terminal OTA

Since it was proved that the transpose of a three-terminal OTA is itself with its ports reversed, it is reasonable to expect that the same will hold to the case of four-terminal OTA. The following analysis is presented to confirm this expectation.

Figs.2.8 (a) and (b) presents the symbol and the equivalent circuit of an OTA with differential inputs and differential outputs.

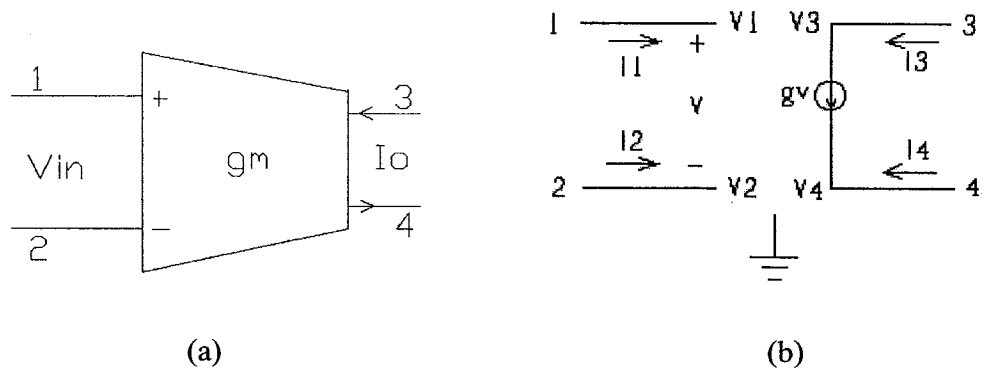


Fig. 2.8(a) The symbol of a DIDO OTA and (b)its equivalent circuit

Y is the short circuit admittance matrix of this OTA, and is described by:

$$I = Y V$$

Where
$$Y = \begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} \\ y_{21} & y_{22} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{33} & y_{34} \\ y_{41} & y_{42} & y_{43} & y_{44} \end{bmatrix}$$

$$I = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}$$

$$V = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$

It is known that for ideal OTA, the input current is zero, i.e. $I_1=I_2=0$, so we can obtain:

$$y_{11} = \frac{I_1}{V_1} = 0 \quad (\text{when } V_2=V_3=V_4=0)$$

$$y_{12} = \frac{I_1}{V_2} = 0 \quad (\text{when } V_1=V_3=V_4=0)$$

$$y_{13} = \frac{I_1}{V_3} = 0 \quad (\text{when } V_1=V_2=V_4=0)$$

$$y_{14} = \frac{I_1}{V_4} = 0 \quad (\text{when } V_1=V_2=V_3=0)$$

Similarly, from $I_2 = 0$ we can get: $y_{21}=y_{22}=y_{23}=y_{24}=0$

From $I_3 = -gV = -g(V_1 - V_2)$, we can obtain:

$$y_{31} = \frac{I_3}{V_1} = \frac{-gV_1}{V_1} = -g \quad (\text{when } V_2=V_3=V_4=0)$$

$$y_{32} = \frac{I_3}{V_2} = \frac{-g(0 - V_2)}{V_2} = g \quad (\text{when } V_1=V_3=V_4=0)$$

$$y_{33} = \frac{I_3}{V_3} = \frac{-g(0 - 0)}{V_3} = 0 \quad (\text{when } V_1=V_2=V_4=0)$$

$$y_{34} = \frac{I_3}{V_4} = \frac{-g(0 - 0)}{V_4} = 0 \quad (\text{when } V_1=V_2=V_3=0)$$

From $I_4 = gV = g(V_1 - V_2)$, we can obtain:

$$y_{41} = \frac{I_4}{V_1} = \frac{gV_1}{V_1} = g \quad (\text{when } V_2=V_3=V_4=0)$$

$$y_{42} = \frac{I_4}{V_2} = \frac{g(0 - V_2)}{V_2} = -g \quad (\text{when } V_1=V_3=V_4=0)$$

$$y_{43} = \frac{I_4}{V_3} = \frac{g(0 - 0)}{V_3} = 0 \quad (\text{when } V_1=V_2=V_4=0)$$

$$y_{44} = \frac{I_4}{V_4} = \frac{g(0 - 0)}{V_4} = 0 \quad (\text{when } V_1=V_2=V_3=0)$$

So the short circuit admittance matrix of this OTA becomes

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -g & g & 0 & 0 \\ g & -g & 0 & 0 \end{bmatrix}$$

Now we reverse the input and output ports of the DIDO OTA, the resulting DIDO OTA is shown in Fig.2.9.

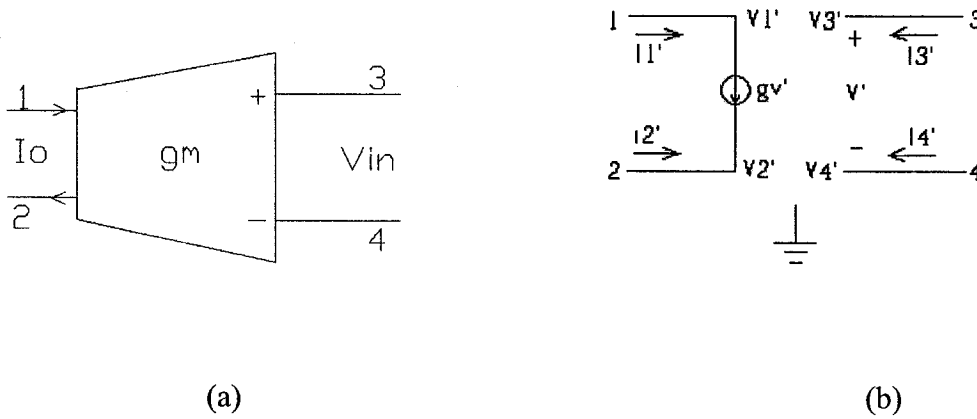


Fig. 2.9(a) The symbol of the transposed OTA and (b) its equivalent circuit

The admittance matrix for the resulting DIDO OTA is given by $I' = Y'V'$, where

$$Y' = \begin{bmatrix} y_{11}' & y_{12}' & y_{13}' & y_{14}' \\ y_{21}' & y_{22}' & y_{23}' & y_{24}' \\ y_{31}' & y_{32}' & y_{33}' & y_{34}' \\ y_{41}' & y_{42}' & y_{43}' & y_{44}' \end{bmatrix}$$

From $I_1' = -gV' = -g(V_3' - V_4')$, we can obtain:

$$y_{11}' = \frac{I_1'}{V_1'} = 0 \quad (\text{when } V_2' = V_3' = V_4' = 0)$$

$$y_{12}' = \frac{I_1'}{V_2'} = 0 \quad (\text{when } V_1' = V_3' = V_4' = 0)$$

$$y_{13}' = \frac{I_1'}{V_3'} = -g \quad (\text{when } V_1' = V_2' = V_4' = 0)$$

$$y_{14}' = \frac{I_1'}{V_4'} = g \quad (\text{when } V_1' = V_2' = V_3' = 0)$$

From $I_2' = gV' = g(V_3' - V_4')$, we can obtain:

$$y_{21}' = \frac{I_2'}{V_1'} = 0 \quad (\text{when } V_2' = V_3' = V_4' = 0)$$

$$y_{22}' = \frac{I_2'}{V_2'} = 0 \quad (\text{when } V_1' = V_3' = V_4' = 0)$$

$$y_{23}' = \frac{I_2'}{V_3'} = g \quad (\text{when } V_1' = V_2' = V_4' = 0)$$

$$y_{24}' = \frac{I_2'}{V_4'} = -g \quad (\text{when } V_1' = V_2' = V_3' = 0)$$

Note that for this reversed OTA, $I_3' = I_4' = 0$. So we can get:

$$y_{31}' = y_{32}' = y_{33}' = y_{34}' = 0 \quad \text{and} \quad y_{41}' = y_{42}' = y_{43}' = y_{44}' = 0$$

So the short circuit admittance matrix of the reversed OTA is:

$$Y' = \begin{bmatrix} 0 & 0 & -g & g \\ 0 & 0 & g & -g \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

Comparing with the short circuit admittance matrix of the original OTA, we see that the transpose of Y is Y' . Hence, the transpose of four-terminal OTA is itself with its input and output terminals reversed.

2.6 Summary

In this chapter, the concept of network transposition has been reviewed. The transposes of the active three-terminal elements including VCVS, VCCS, CCVS and CCCS have been presented. Furthermore, the transposition operation on a voltage-mode filter has been given as an example. Finally, the transpose of a DIDO OTA has been derived. With this, we are able to find transposes of DIDO-OTA-C filters and DIDO-OTA-C oscillators.

Chapter 3 OTA-C Filter Structures

3.1 Introduction

The commercialization of new analog building blocks such as OTA, CCII, and transimpedance amplifier coupled with the development in integrated circuit process technology has made current-mode signal processing more and more popular. Network transposition is a powerful tool for voltage/current mode conversion, and provides great convenience for the analysis and design of analog continuous-time filters. Since a vast body of voltage-mode OTA-C filter structures are already known, while many current-mode OTA-C filter structures are still being reported in the literature, one may wonder if these two apparently independent areas of research and development could be unified by the application of the principle of network transposition. For this reason, an intensive investigation on the OTA-C structures is conducted in this chapter.

Furthermore, the principle of network transposition is extended to cover the case of OTA-C filters using DIDO-OTAs. As illustrations, two new current-mode DIDO-OTA-C filters are derived from the corresponding voltage-mode OTA-C filters using transposition operation. As expected, their transfer functions are identical.

3.2 OTA-C voltage mode and current mode filter structures by network transposition

The design of OTA-C filters has traditionally been viewed as a voltage dominated form of signal processing. Over the last fifteen years, current-mode signal processing has emerged as an important class of analogue circuitry because of the simplicity associated with implementing basic operations such as signal summing and replication, and the potential to operate at higher signal bandwidths and lower voltage than the voltage-mode approach. Numerous current mode OTA-C filter configurations have been developed [2],[6]-[9],[12]. In [2],[9] Sun and Fidler proposed current-mode two integrator loop dual output OTA-C filter and current-mode multiple-loop feedback filters. In principle, a number of current mode filter structures can be generated by these systematic methods. However, complicated circuit node voltage/current calculations are needed for the derivation of the transfer function in the case of two integrator loop structures. For the multiple-loop feedback structure, high order feedback coefficient matrix F has to be manipulated to reflect the filter structure. Approaches are required to solve the coefficient matching nonlinear equations associated with the feedback matrix. Moreover, for the general n th-order case there are $n!$ possible structures. Searching and analyzing all these structures is an exhausting work. In contrast, by using network transposition, current-mode OTA-C filter structures can be obtained in a straightforward manner from

the well-known voltage-mode counterparts, without time-consuming mathematical analysis and synthesis. In fact, we will show that Sun and Fidler's current-mode multiple-loop feedback filters [9] are just the transposes of the corresponding voltage-mode multiple-loop feedback filters [13], also proposed by Sun and Fidler. Furthermore, the current-mode two integrator loop dual output OTA-C filters of Sun and Fidler [2] can be derived as the transposes of the voltage mode two integrator loop OTA-C filters proposed earlier by Sanchez-Sinencio et al. [14]

To establish the one to one transpose relationship among these structures, we consider an example. Consider the voltage-mode structure given in Fig.3.1[14]. Network transposition can be carried out by transposing the OTAs and reversing the input/output ports of the filter. First, we transpose the voltage-mode filter structure of Fig.3.1 and obtain the corresponding current-mode filter structure, as shown in Fig.3.2. If we now replace g_{m4}, g_{m6} in Fig.3.2 with resistors g_4, g_6 , and redraw this structure from the right to the left, we will obtain the structure shown in Fig.3.4. This structure is identical to the current-mode filter proposed by Sun and Fidler in [2].

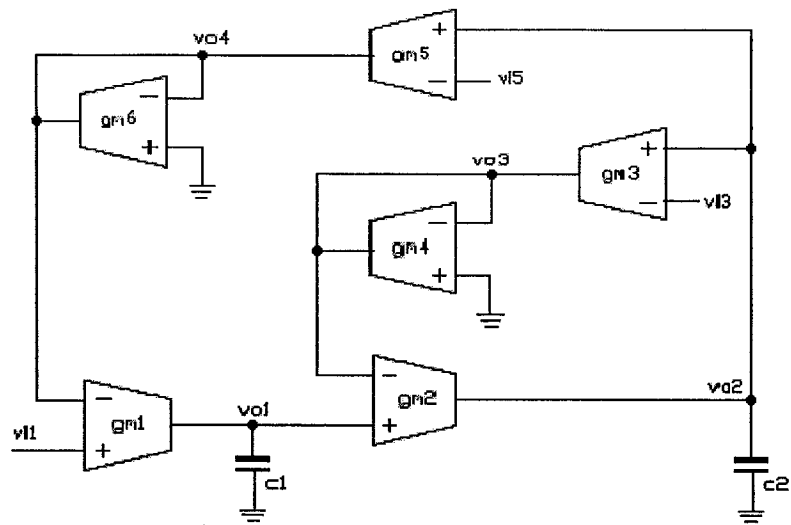


Fig. 3.1 Voltage-mode OTA-C filter

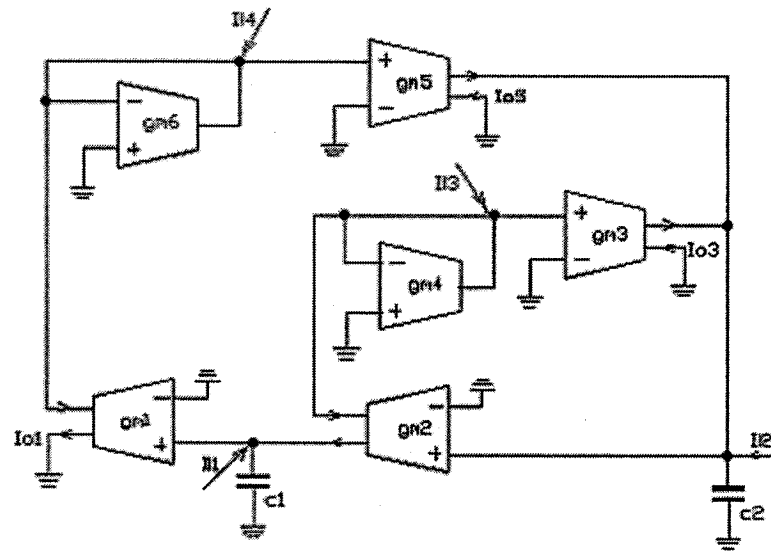


Fig. 3.2 Transpose of the structure of Fig.3.1

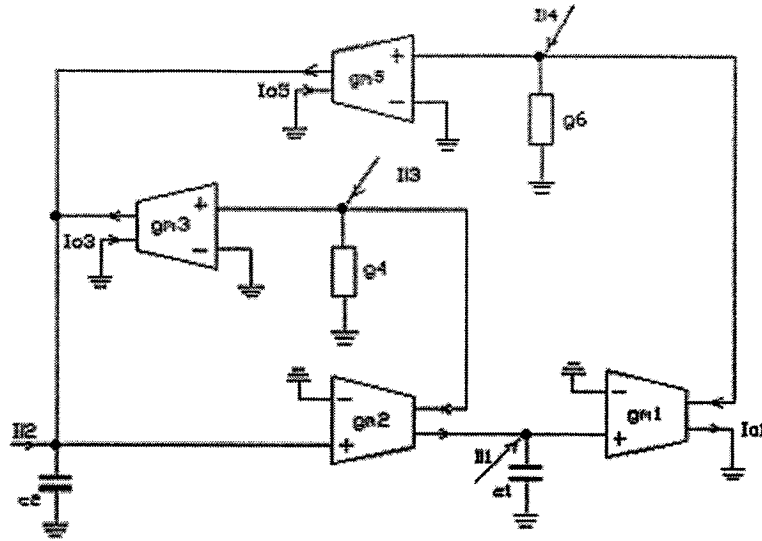


Fig. 3.3 Redrawing of the structure in Fig.3.2

Similarly, it can be shown that all the current-mode filter that have been proposed in the literature using OTAs [2,9,12] can be shown to be transpose of the corresponding voltage-mode filters using OTAs. These are listed in Table 3.1.

Table 3.1 Voltage-mode OTA-C filter structures and their transposition

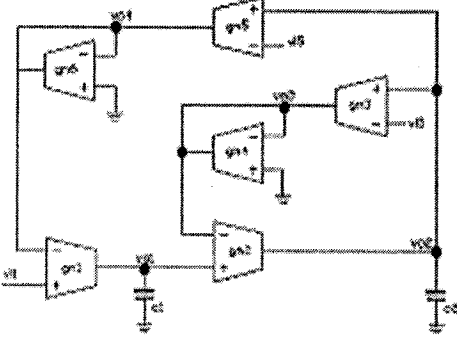
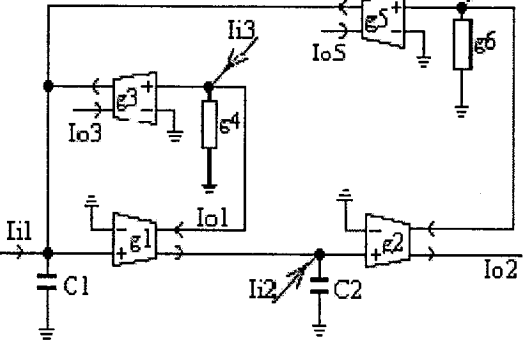
Voltage Mode OTA-C Filters	Current Mode OTA-C Filters
 <p style="text-align: center;">Proposed in [14]</p>	 <p style="text-align: center;">Proposed in [2]</p>

Table 3.1 Voltage-mode OTA-C filter structures and their transposition (continued)

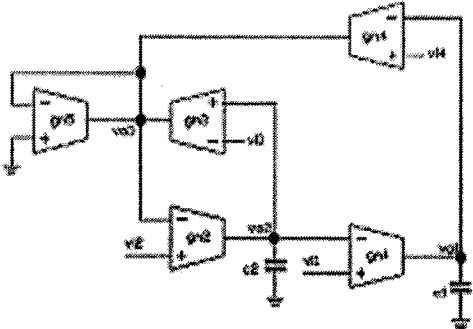
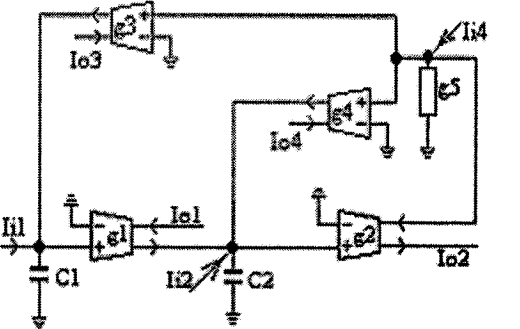
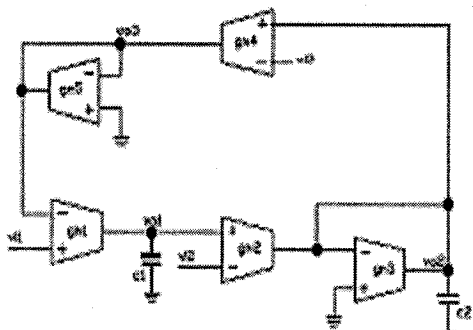
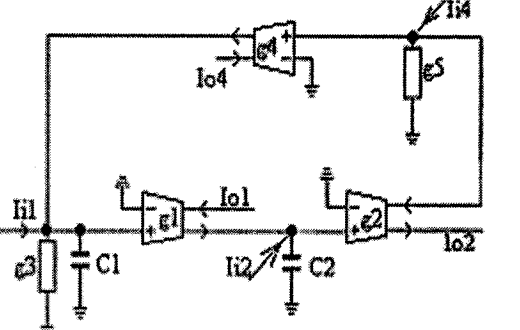
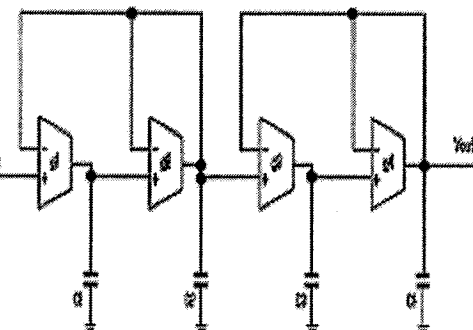
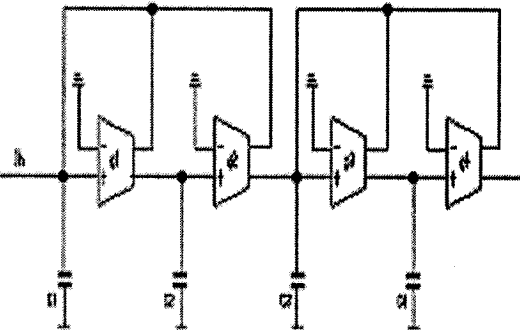
Voltage Mode OTA-C Filters	Current Mode OTA-C Filters
 <p style="text-align: center;">Proposed in [14]</p>	 <p style="text-align: center;">Proposed in [2]</p>
 <p style="text-align: center;">Proposed in [14]</p>	 <p style="text-align: center;">Proposed in [2]</p>
 <p style="text-align: center;">Proposed in [13]</p>	 <p style="text-align: center;">Proposed in [9]</p>

Table 3.1 Voltage-mode OTA-C filter structures and their transposition (continued)

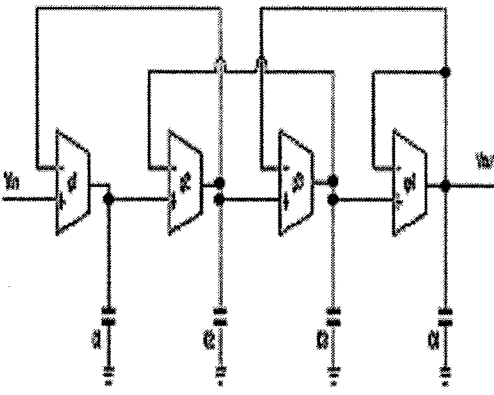
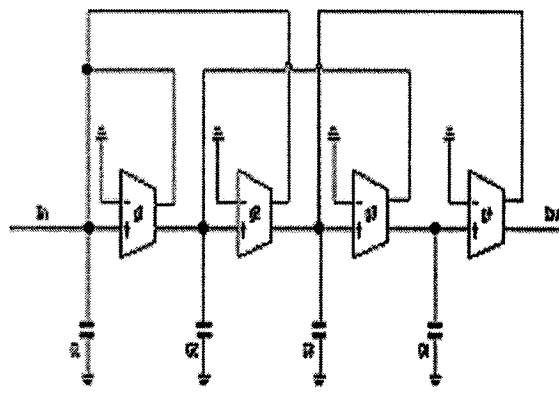
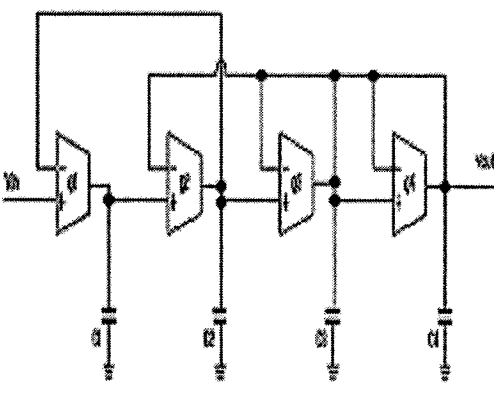
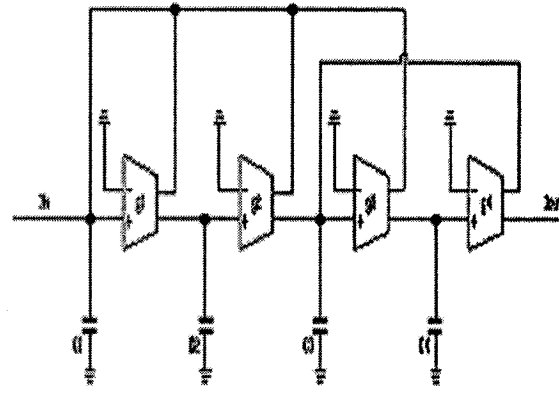
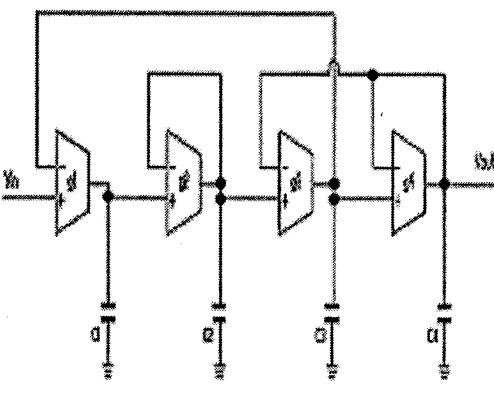
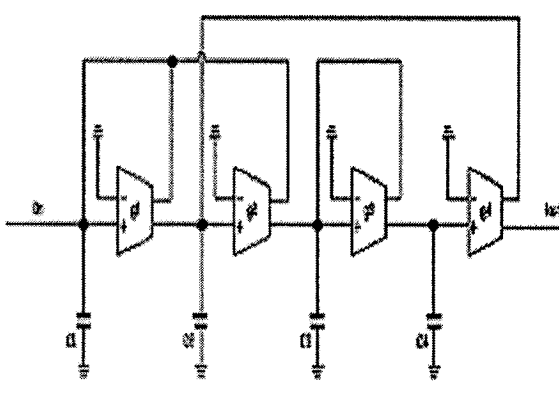
Voltage Mode OTA-C Filters	Current Mode OTA-C Filters
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 <p data-bbox="461 1271 678 1306">Proposed in [13]</p>	 <p data-bbox="1036 1271 1237 1306">Proposed in [9]</p>
 <p data-bbox="461 1773 678 1808">Proposed in [13]</p>	 <p data-bbox="1036 1773 1237 1808">Proposed in [9]</p>

Table 3.1 Voltage-mode OTA-C filter structures and their transposition (continued)

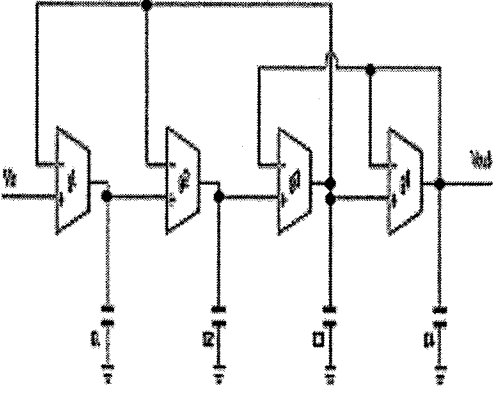
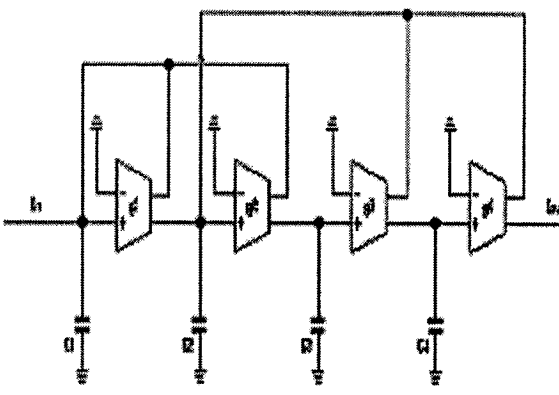
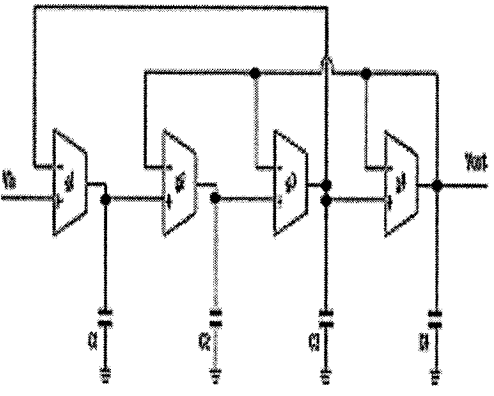
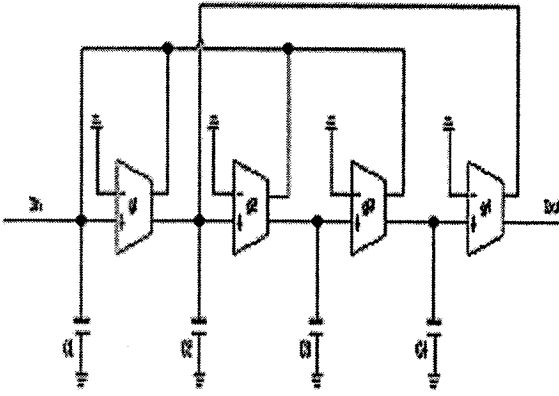
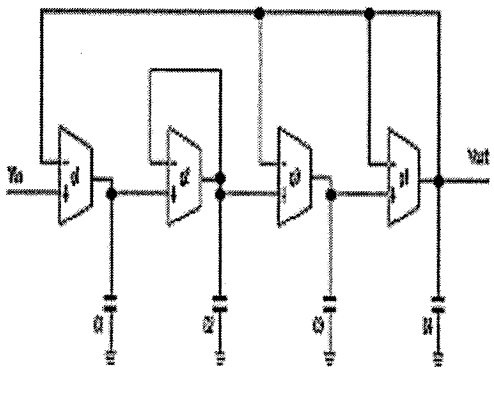
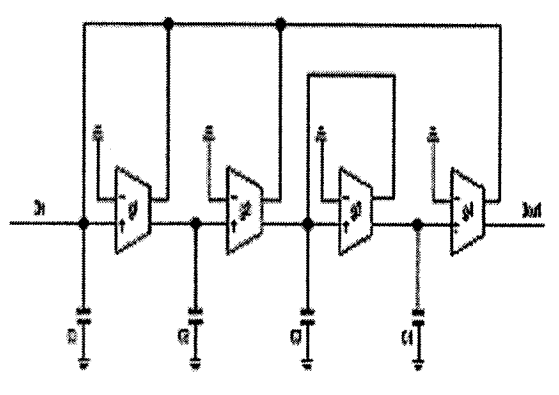
Voltage Mode OTA-C Filters	Current Mode OTA-C Filters
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 <p data-bbox="461 1275 678 1312">Proposed in [13]</p>	 <p data-bbox="1002 1275 1203 1312">Proposed in [9]</p>
 <p data-bbox="461 1777 678 1814">Proposed in [13]</p>	 <p data-bbox="1002 1777 1203 1814">Proposed in [9]</p>

Table 3.1 Voltage-mode OTA-C filter structures and their transposition (continued)

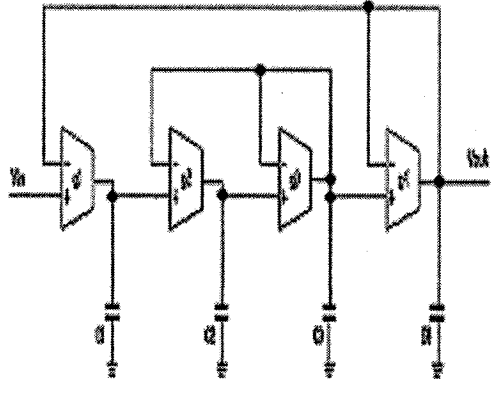
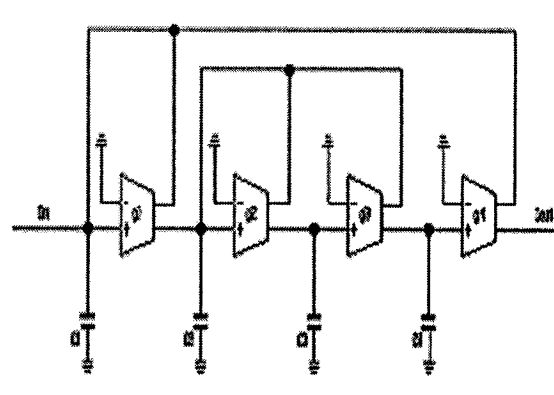
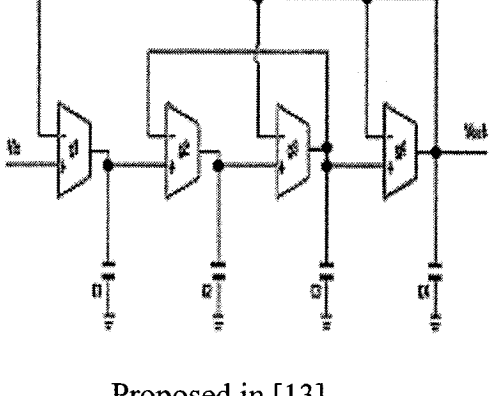
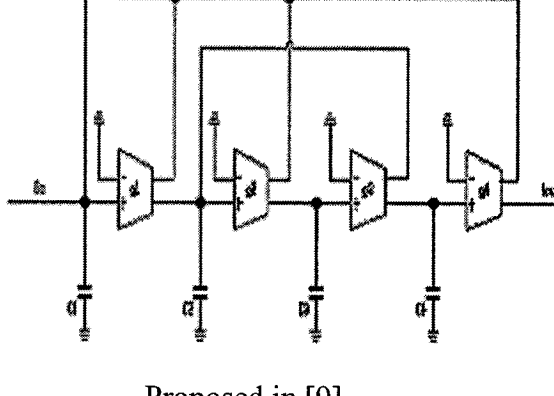
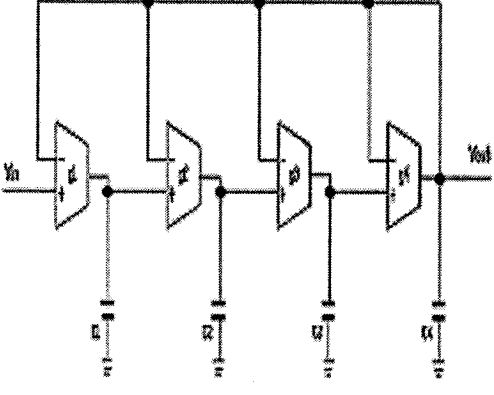
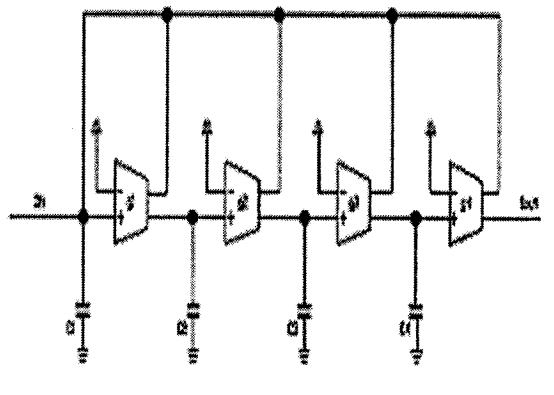
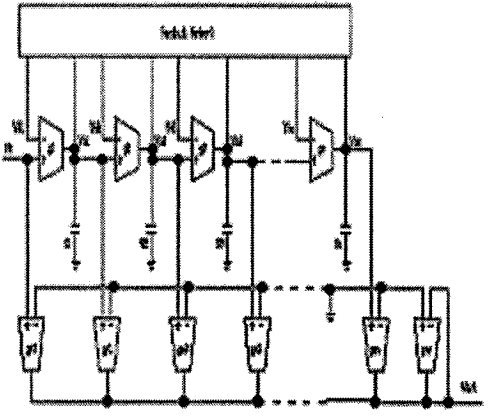
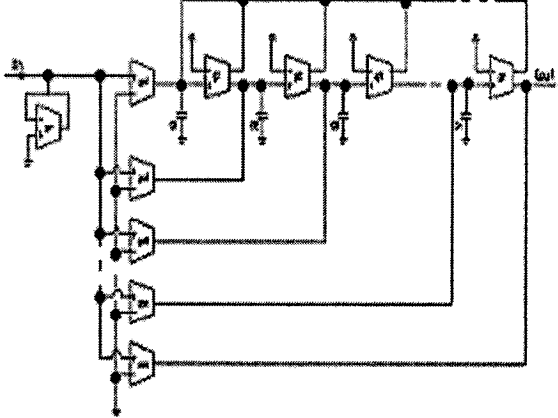
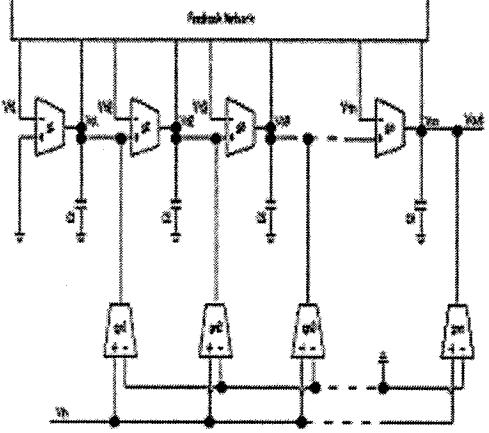
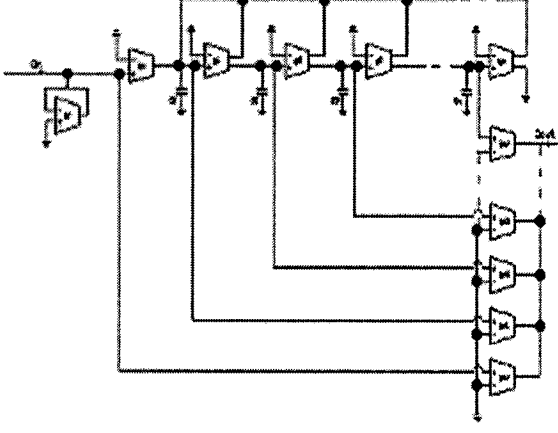
Voltage Mode OTA-C Filters	Current Mode OTA-C Filters
 <p data-bbox="459 770 678 810">Proposed in [13]</p>	 <p data-bbox="1036 770 1239 810">Proposed in [9]</p>
 <p data-bbox="459 1229 678 1268">Proposed in [13]</p>	 <p data-bbox="1019 1229 1222 1268">Proposed in [9]</p>
 <p data-bbox="459 1731 678 1771">Proposed in [13]</p>	 <p data-bbox="1019 1731 1222 1771">Proposed in [9]</p>

Table 3.1 Voltage-mode OTA-C filter structures and their transposition (continued)

Voltage Mode OTA-C Filters	Current Mode OTA-C Filters
 <p data-bbox="459 814 678 847">Proposed in [13]</p>	 <p data-bbox="1019 814 1230 847">Proposed in [12]</p>
 <p data-bbox="459 1354 678 1386">Proposed in [13]</p>	 <p data-bbox="1019 1354 1230 1386">Proposed in [12]</p>

3.3 Application of Network Transposition on fully differential OTA-C filter structure

We have already derived the transpose of a DIDO OTA in chapter 2. The transposition operation on a DIDO OTA-C filter consists of simply transposing each of the four-terminal OTAs in the filter in accordance with the principle discussed in Chapter 2. As an example, consider the DIDO-OTA-C voltage-mode filter shown in Fig.3.5 [15]. Its transpose may be directly obtained and is shown in Fig.3.6. This filter is a current-mode filter.

It can be easily verified that the voltage transfer function of the former (i.e., Fig. 3.5) is the same as the current transfer function of the latter (i.e., Fig.3.6). These are given by:

$$\frac{V_{lp}}{V_i} = \frac{I_o}{I_{in2}} = \frac{-gm_3gm_4}{C_1C_2s^2 + gm_3C_2s + gm_1gm_2}$$

$$\frac{V_{bp}}{V_i} = \frac{I_o}{I_{in1}} = \frac{-gm_4C_2s}{C_1C_2s^2 + gm_3C_2s + gm_1gm_2}$$

An additional example of a voltage mode OTA-C filter [16] and its transpose (i.e., a current-mode OTA-C filter) are shown in Fig. 3.7, and Fig.3.8 respectively.

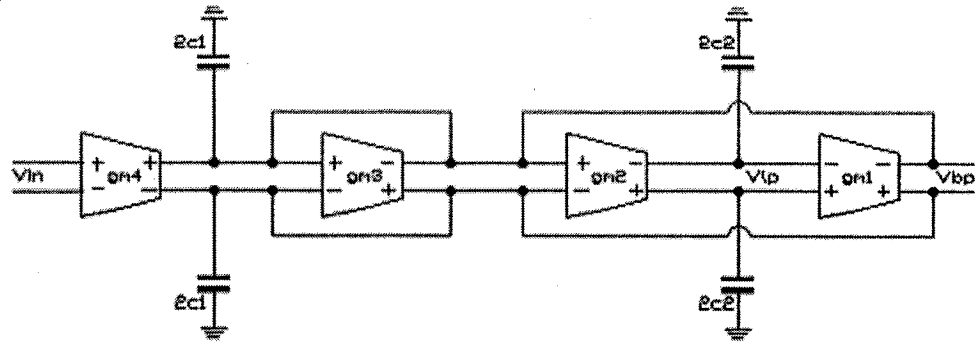


Fig. 3.4 OTA-C differential voltage-mode filter

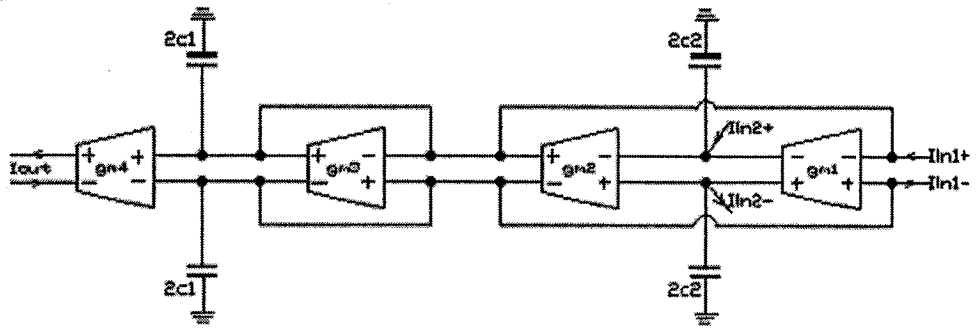


Fig. 3.5 Transposition of the filter in Fig.3.4

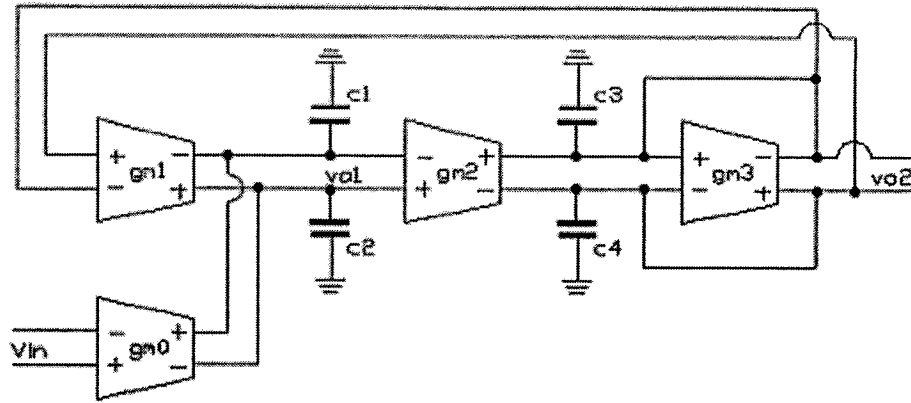


Fig. 3.6 OTA-C differential voltage-mode filter

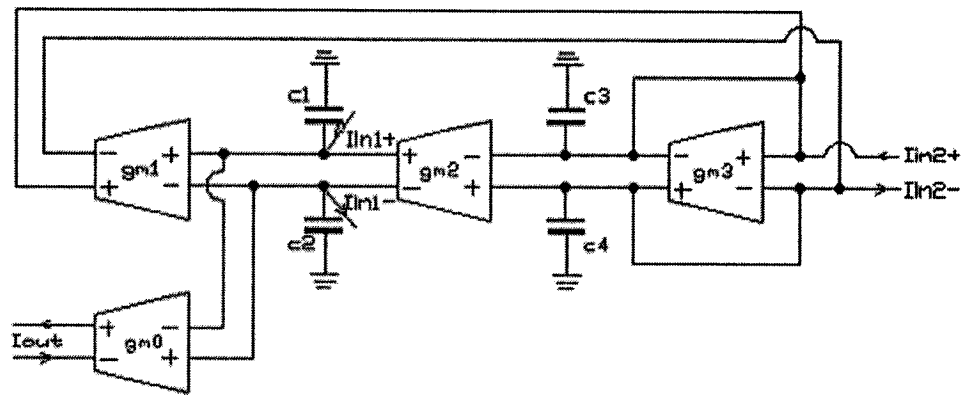


Fig. 3.7 Transposition of the filter in Fig.3.6

The corresponding transfer functions are given by:

$$\frac{V_{o1}}{V_i} = \frac{I_o}{I_{in1}} = \frac{-gm_0 C_2 s - gm_0 gm_3}{C_1 C_2 s^2 + gm_3 C_1 s + gm_1 gm_2} \quad \frac{V_{o2}}{V_i} = \frac{I_o}{I_{in2}} = \frac{gm_0 gm_2}{C_1 C_2 s^2 + gm_3 C_1 s + gm_1 gm_2};$$

3.4 Summary

In this chapter it has been shown that voltage-mode/current-mode OTA-C filter architectures can always be obtained from the corresponding current-mode/voltage-mode architectures using network transposition. Many such filter structures have been published in the literature as if they were independent structures. In this chapter we have considered examples of such structures. These examples establish the beauty, simplicity, feasibility and usefulness of network transposition. Furthermore, by transposing four-terminal OTA devices and interchanging the input and output ports of the circuits, new DIDO-OTA-C filter architectures have been derived from known voltage-mode architectures. In the following chapter, we will apply this method in the design of another class of important electronic circuits i.e., CMOS sine wave oscillators.

Chapter 4 OTA-C Oscillator Structures

4.1 Introduction

We saw in Chapter 3 that the concept of network transposition is very useful in the design of OTA-C current-mode filters from associated OTA-C voltage-mode filter architectures. However, this concept has not yet been utilized in the area of OTA-C based oscillator design. In this chapter, first a review of the OTA-C oscillators is given. Then, a linear model of an OTA-C oscillator is presented, followed by a discussion about the feasibility of applying network transposition in deriving new oscillator circuits from known OTA-C oscillator circuits. Finally, new DIDO-OTA-C oscillator architectures consisting of four-terminal OTAs and capacitors are derived from single output oscillator architectures using the principle of “mirroring”.

4.2 OTA-C Oscillators – A Brief Review

OTA-C oscillators have been attracting considerable attention in the recent years for various signal processing and signal generation applications in view of their being able to operate at a higher frequency range; suitability for IC implementation; and linear electronic tunability of oscillation frequency. In 1989, Senani et al proposed a linearly tunable Wien bridge oscillator [17]. This structure originates from the well-known active

RC Wien bridge oscillator. By replacing the OP-AMPs and resistors in the original circuit with OTAs, the OTA-C Wien bridge oscillator is obtained. This oscillator requires 4 OTAs and 2 capacitors. In contrast, Abuelmaatti presented two OTA-C oscillators using minimum components, which are 2 OTAs and 2 capacitors for each oscillator [18]. In 1990, Senani et al discussed a systematic method of generating more oscillator structures [19]. In this method, the oscillator is broken up into two parts: capacitors and an all-OTA network. The all-OTA network is represented by its y-matrix. The y-parameters are chosen to satisfy the oscillation condition, i.e. $b=0$ for the general characteristic equation: $s^2+bs+c = 0$. Various oscillator structures can be derived from different sets of y-parameters. In 1992, Linares-Barranco et al proposed new structures based on the quadrature model [20]. In this model, the oscillator is considered as two lossless integrator cascaded in a loop, which results in a characteristic equation with a pair of roots lying on the imaginary axis of the complex frequency plane. Furthermore, the proposed oscillator structures were implemented in $3\mu\text{m}$ CMOS technology. It was the first IC implementation of an OTA-C oscillator among all the papers cited above.

4.3 Linear Model of OTA-C Oscillator and its Transpose

Consider two second order 3-terminal active networks which are transposes of each other (Fig.4.1) Let their transfer functions be $\frac{V_o}{V_i} = \frac{I_o}{I_i} = a \times \frac{(s^2 + ds + e)}{(s^2 + bs + c)}$. The characteristic equation (CE) of N and N_T are the same, namely, $s^2+bs+c = 0$. (4.1)

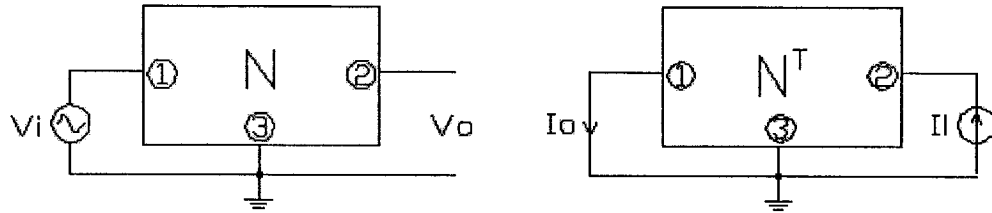


Fig. 4.1 Second order three-terminal active networks

For network N , if we set $V_i=0$ and replace the voltage source V_i by its zero internal impedance and leave the output terminals open, N assumes the basic structure of a sinusoidal oscillator (say, oscillator A) as shown in Fig.4.2. Similarly, for the network N_T if we set $I_i=0$ and replace the current source I_i by its internal admittance (i.e., open circuit) and connect the output terminal to ground, N_T assumes the basic structure of the transposed sine oscillator (say oscillator B) as shown in Fig.4.3.

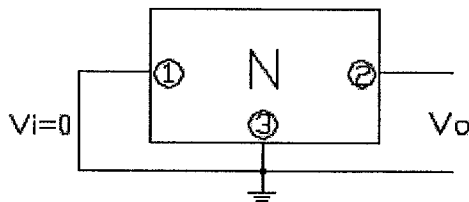


Fig. 4.2 Oscillator A

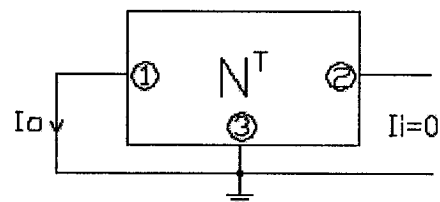


Fig. 4.3 Oscillator B

The characteristic equations in both cases are the same and given by eq.(4.1). Thus, we can derive the oscillator structure B from the original oscillator A by network transposition and vice versa. To ensure that oscillation exists, be stable and unique, the condition of oscillation $b=0$ should be satisfied and c that determines the frequency of oscillation must be greater than 0. The original oscillator A and the transposed one,

oscillator B, have the same characteristic equation as well as the same condition and frequency of oscillation. Also, the various sensitivities with respect to the corresponding parameters are identical. Thus, the two oscillators are expected to have similar performances.

4.4 Single-Output OTA-C Oscillator Architectures

Several OTA-C oscillator architectures employing single-output OTAs and capacitors have been proposed in the past. Based on these architectures, new OTA-C oscillator architectures can be obtained by the application of network transposition. For example, consider the OTA-C oscillator shown in Fig. 4.4 [14]. At first, we treat it as a

voltage-mode filter, whose voltage transfer function is given by
$$\frac{V_o}{V_i} = \frac{C_1 C_2 s^2}{C_1 C_2 s^2 - (gm_1 C_2 - gm_2 C_1)s + gm_1 gm_2}$$
. By applying network transposition, we can derive

the corresponding current-mode filter, as shown in Fig. 4.5 with its current transfer function given by
$$\frac{I_o}{I_i} = \frac{C_1 C_2 s^2}{C_1 C_2 s^2 - (gm_1 C_2 - gm_2 C_1)s + gm_1 gm_2}$$
. As expected, both the filters

have the same characteristic equations, namely, $C_1 C_2 s^2 - (gm_1 C_2 - gm_2 C_1)s + gm_1 gm_2 = 0$.

Now we set $V_i=0$ for the voltage-mode filter and $I_i=0$ for the current-mode filter. Then, both the networks function as oscillators as long as the condition of oscillation is satisfied:

$b=0$, that is, $gm_1 C_2 = gm_2 C_1$. Also the frequency of oscillation for either of the oscillators is given by $\sqrt{\frac{gm_1 gm_2}{C_1 C_2}}$. Both these oscillators in Fig.4.4, 4.5 have been proposed in [18]

and as seen above, the two oscillators are just transposes of each other.

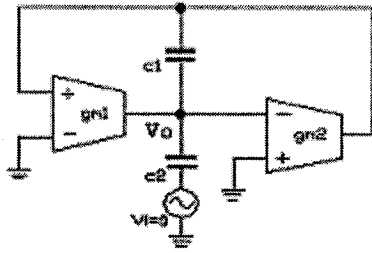


Fig. 4.4 Oscillator structure
proposed in [18]

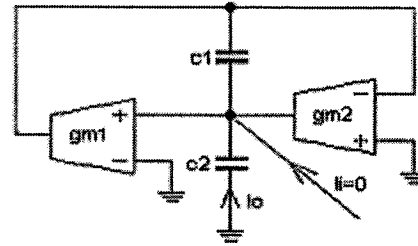


Fig. 4.5 Its transpose-same as the one
proposed in [18]

Other single-output OTA-C oscillator structures can be found in [17,19,20]. Their transposed counterparts can be easily obtained by means of network transposition, and are shown in Table 4.1. All the OTA-C oscillator structures thus derived using the principle of network transposition are new. The characteristic equations, as well as the conditions and frequencies of oscillation of these new oscillators, are the same as those of the original oscillators from which they have been derived. These are listed in Table 4.2.

Table 4.1 Associated OTA-C oscillator structures

OTA-C Oscillator Structures	Transposed Oscillator Structures
<p data-bbox="321 1753 659 1786">Fig.4.6 Proposed in [20]</p>	<p data-bbox="911 1753 1195 1786">Fig.4.7 New structure</p>

Table 4.1 Associated OTA-C oscillator structures (continued)

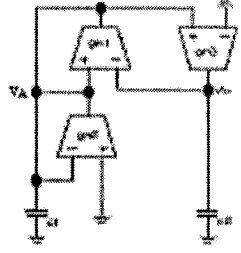
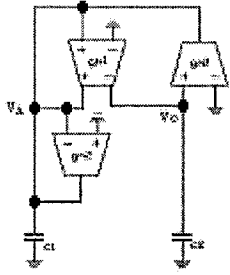
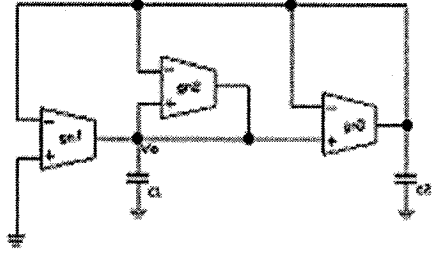
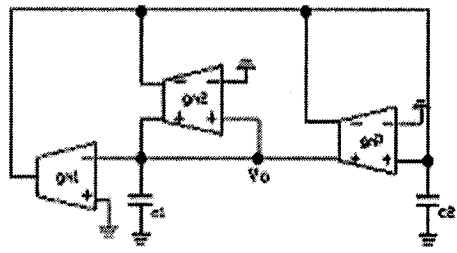
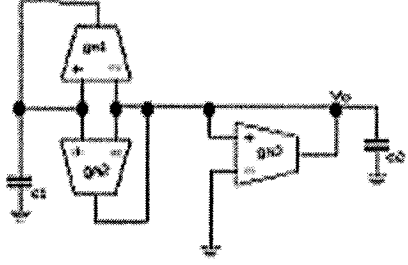
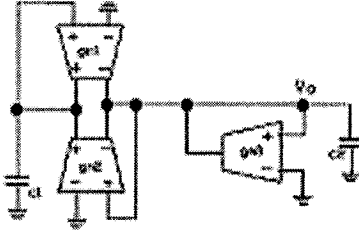
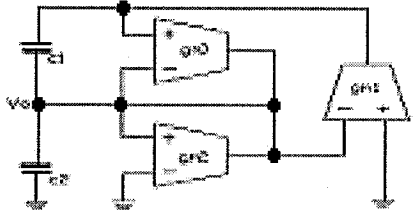
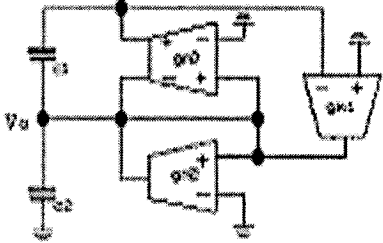
OTA-C Oscillator Structures	Transposed Oscillator Structures
 <p data-bbox="370 650 711 690">Fig.4.8 Proposed in [19]</p>	 <p data-bbox="912 650 1198 690">Fig.4.9 New structure</p>
 <p data-bbox="370 1022 711 1061">Fig.4.10 Proposed in [19]</p>	 <p data-bbox="912 1022 1214 1061">Fig.4.11 New structure</p>
 <p data-bbox="370 1397 711 1437">Fig.4.12 Proposed in [19]</p>	 <p data-bbox="912 1397 1237 1437">Fig.4.13 New structure</p>
 <p data-bbox="370 1812 711 1852">Fig.4.16 Proposed in [19]</p>	 <p data-bbox="912 1812 1214 1852">Fig.4.17 New structure</p>

Table 4.1 Associated OTA-C oscillator structures (continued)

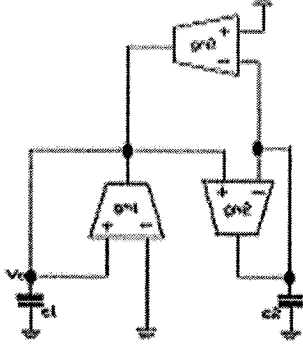
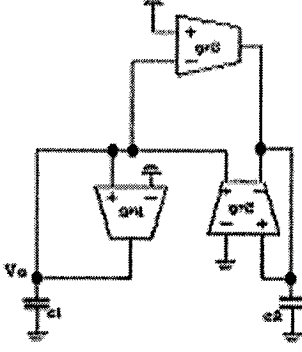
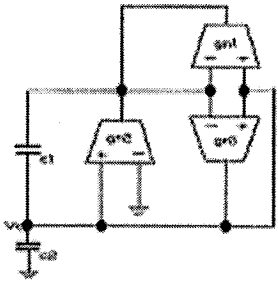
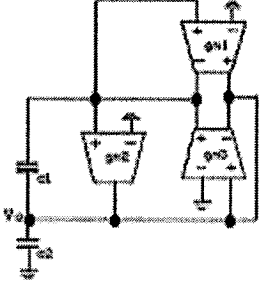
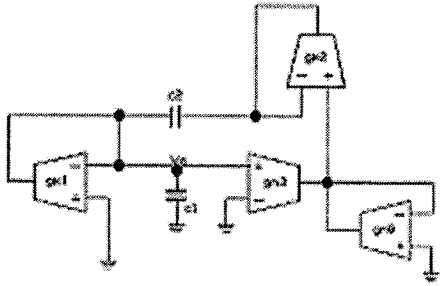
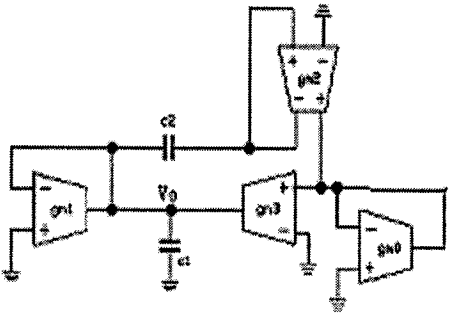
OTA-C Oscillator Structures	Transposed Oscillator Structures
 <p data-bbox="386 760 717 797">Fig.4.14 Proposed in [19]</p>	 <p data-bbox="961 760 1263 797">Fig.4.15 New structure</p>
 <p data-bbox="386 1174 717 1212">Fig.4.18 Proposed in [19]</p>	 <p data-bbox="945 1174 1247 1212">Fig.4.19 New structure</p>
 <p data-bbox="386 1633 717 1670">Fig.4.20 Proposed in [17]</p>	 <p data-bbox="928 1633 1230 1670">Fig.4.21 New structure</p>

Table 4.2. Characteristic equations, conditions and frequencies

of oscillation for various oscillators.

Oscillators of Figs.	Characteristic Equation	Oscillation Condition	frequency (Ω^2)
4.6,4.7	$s^2 - \frac{(g_{m3} - g_{m4})}{C_1}s + \frac{g_{m1}g_{m2}}{C_1C_2} = 0$	$g_{m3} - g_{m4} = 0$	$\frac{g_{m1}g_{m2}}{C_1C_2}$
4.8,4.9	$s^2 - \left(\frac{g_{m1}}{C_1} - \frac{g_{m2}}{C_1}\right)s + \frac{g_{m1}g_{m3}}{C_1C_2} = 0$	$\frac{g_{m1}}{C_1} - \frac{g_{m2}}{C_1} = 0$	$\frac{g_{m1}g_{m3}}{C_1C_2}$
4.10,4.11	$s^2 - \left(\frac{g_{m2}}{C_1} - \frac{g_{m3}}{C_2}\right)s + \frac{g_{m1}g_{m3}}{C_1C_2} = 0$	$\frac{g_{m2}}{C_1} - \frac{g_{m3}}{C_2} = 0$	$\frac{g_{m1}g_{m3}}{C_1C_2}$
4.12,4.13	$s^2 - \left(\frac{g_{m1}}{C_1} + \frac{g_{m3}}{C_2} - \frac{g_{m2}}{C_2}\right)s + \frac{g_{m1}g_{m3}}{C_1C_2} = 0$	$\frac{g_{m1}}{C_1} + \frac{g_{m3}}{C_2} - \frac{g_{m2}}{C_2} = 0$	$\frac{g_{m1}g_{m3}}{C_1C_2}$
4.14,4.15	$s^2 - \left(\frac{g_{m1}}{C_1} - \frac{g_{m2}}{C_2}\right)s + \frac{g_{m2}g_{m3} - g_{m1}g_{m2}}{C_1C_2} = 0$	$\frac{g_{m1}}{C_1} - \frac{g_{m2}}{C_2} = 0$	$\frac{g_{m2}g_{m3} - g_{m1}g_{m2}}{C_1C_2}$
4.16,4.17	$s^2 - \left(\frac{g_{m2}}{C_2} - \frac{g_{m1}}{C_2}\right)s + \frac{g_{m1}g_{m3}}{C_1C_2} = 0$	$\frac{g_{m2}}{C_2} - \frac{g_{m1}}{C_2} = 0$	$\frac{g_{m1}g_{m3}}{C_1C_2}$
4.18,4.19	$s^2 - \left(\frac{g_{m2}}{C_2} - \frac{g_{m1}}{C_1}\right)s + \frac{g_{m2}g_{m3}}{C_1C_2} = 0$	$\frac{g_{m2}}{C_2} - \frac{g_{m1}}{C_1} = 0$	$\frac{g_{m2}g_{m3}}{C_1C_2}$
4.20,4.21	$s^2 - \left(\frac{g_{m2} \times g_{m3}}{C_1g_{m0}} - \frac{g_{m2}}{C_2} - \frac{g_{m1}}{C_1} - \frac{g_{m2}}{C_1}\right)s + \frac{g_{m1}g_{m2}}{C_1C_2} = 0$	$\frac{g_{m2} \times g_{m3}}{C_1g_{m0}} - \frac{g_{m2}}{C_2} - \frac{g_{m1}}{C_1} - \frac{g_{m2}}{C_1} = 0$	$\frac{g_{m1}g_{m2}}{C_1C_2}$

4.5 Differential OTA-C Oscillator Architectures

Differential structures are widely used in OTA-C based designs because of improved common-mode rejection ratio, elimination of even-order harmonic distortion components and reduction of the effects of power supply noise. In mixed-signal or system on chip design, differential structures are especially important for reducing interference and noise from the digital circuits on the same chip. Differential configurations can be obtained from single-ended structures using the principle of mirroring. This method of conversion consists of three steps [21]:

- 1) Form a mirror image of the nominal single-ended structure about a plane through the ground node.
- 2) Change the sign of the gain of all mirrored active elements
- 3) Merge the resulting pair with inverting and non-inverting gains into a single balanced device.

By following these steps, the oscillator in Fig.4.7 is mirrored as shown in Fig.4.24, and the resulting differential architecture is shown in Fig.4.25. Similarly, using the oscillator of Fig.4.6, one can derive the differential oscillator architecture as shown in Fig.4.26. As expected, the oscillator networks of Fig.4.25 and 4.26 are themselves transposes of each other.

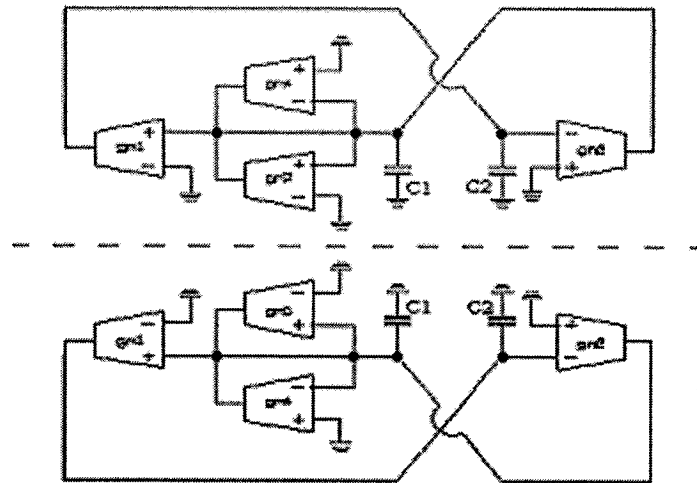


Fig. 4.22 Mirrored OTA-C oscillator

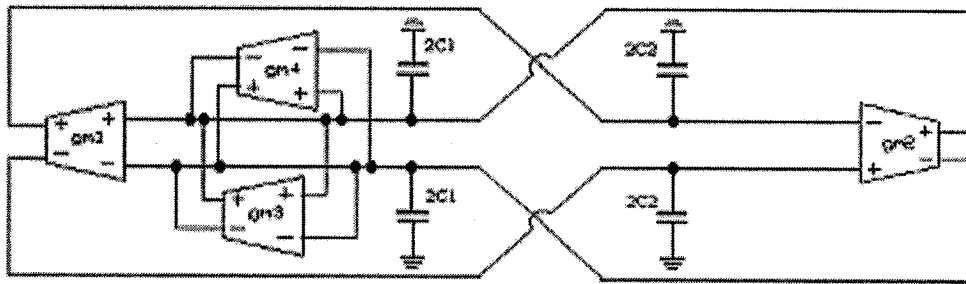


Fig. 4.23 Differential OTA-C oscillator

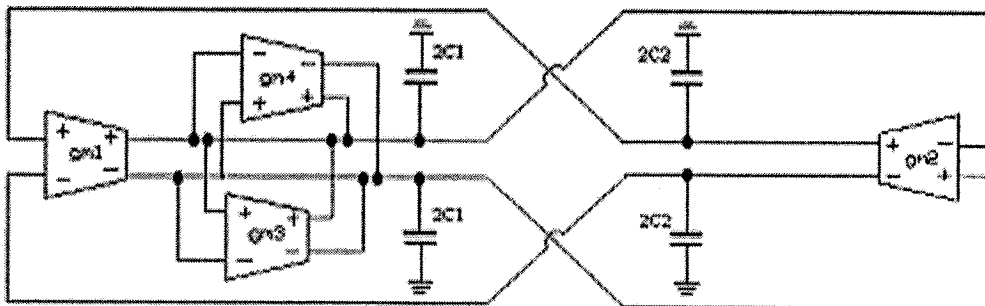


Fig. 4.24 OTA-C oscillator

This technique can be used for all the other single-ended OTA-C oscillator circuits to derive the corresponding differential structure oscillators employing OTAs and capacitors.

4.5 Summary

In this chapter network transposition principle has been extended to oscillator circuits, and used to derive several new OTA-C oscillator architectures from previously known oscillator structures. The characteristic equations, oscillation frequencies and the oscillation conditions for these oscillators are shown to be the same as those of the original oscillators. Finally, differential OTA-C oscillator architectures have been obtained by means of the “mirroring” technique.

Chapter 5 Experiments with Discrete Elements

5.1 Introduction

In the previous chapters we addressed various theoretical issues related to current mode filters and oscillators using OTAs. In this chapter we intend to provide validation of the theoretical work using commercially available OTA devices, discrete resistances and capacitors. First, some basic electrical characteristics of the discrete components are introduced. Then, the configurations and the experiment setup of the OTA-C oscillators are shown. Output oscillation waveforms are measured and compared with the theoretical predictions. Finally, a pair of OTA-C bandpass filters are built with discrete elements and the test results are given.

5.2 Electrical Characteristics of the discrete components

In this experiment, commercial OTA chip, the LM13700 from National Semiconductors and discrete R, C components available in the electronics laboratory are used to build the test circuit. The resistors have tolerance of $\pm 2\%$ and temperature characteristic of $\pm 100\text{ppm}/^{\circ}\text{C}$, which means 1°C change in temperature results in 0.1% resistance variation. The capacitors have tolerance of $\pm 10\%$. For the LM13700, its input offset voltage is 0.4mV, the slew rate is $50\text{V}/\mu\text{s}$, and the open loop bandwidth is 2MHz.

Because of its narrow bandwidth, the test frequency in the experiments is limited to the order of 100KHz. The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. Its connection diagram is shown in Fig.5.1. Note that the buffers are not used here because of its low output impedance.

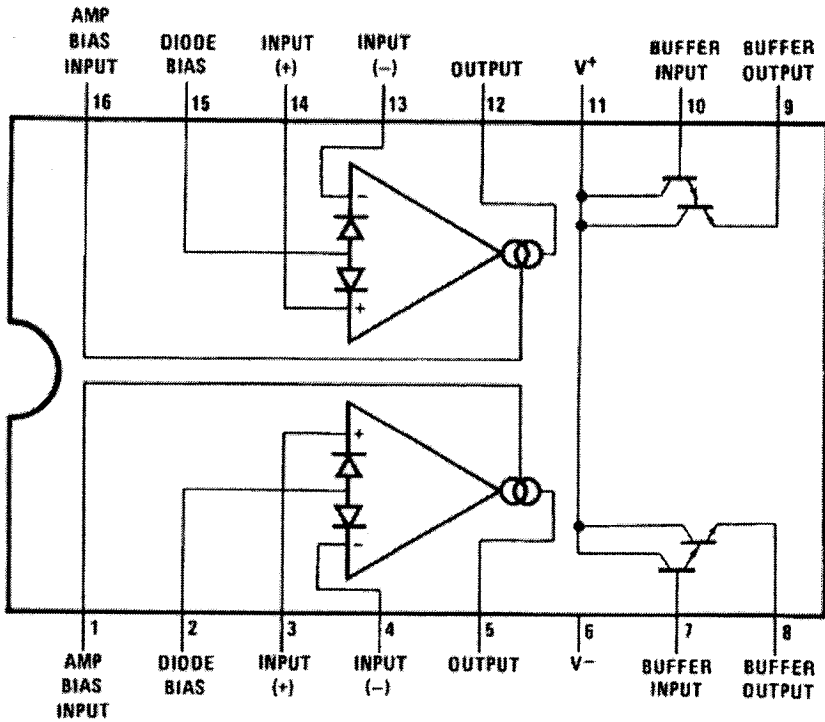


Fig. 5.1 The LM13700 connection diagram

5.3 Experiments on OTA-C oscillators

The oscillators structures presented in Fig.4.8, 4.9 and re-drawn in Fig.5.2 (a) and (b), are tested in the laboratory. Their characteristic equations are identical and given as:

$$s^2 - \left(\frac{g_{m1}}{C_1} - \frac{g_{m2}}{C_1}\right)s + \frac{g_{m1}g_{m3}}{C_1C_2} = 0.$$

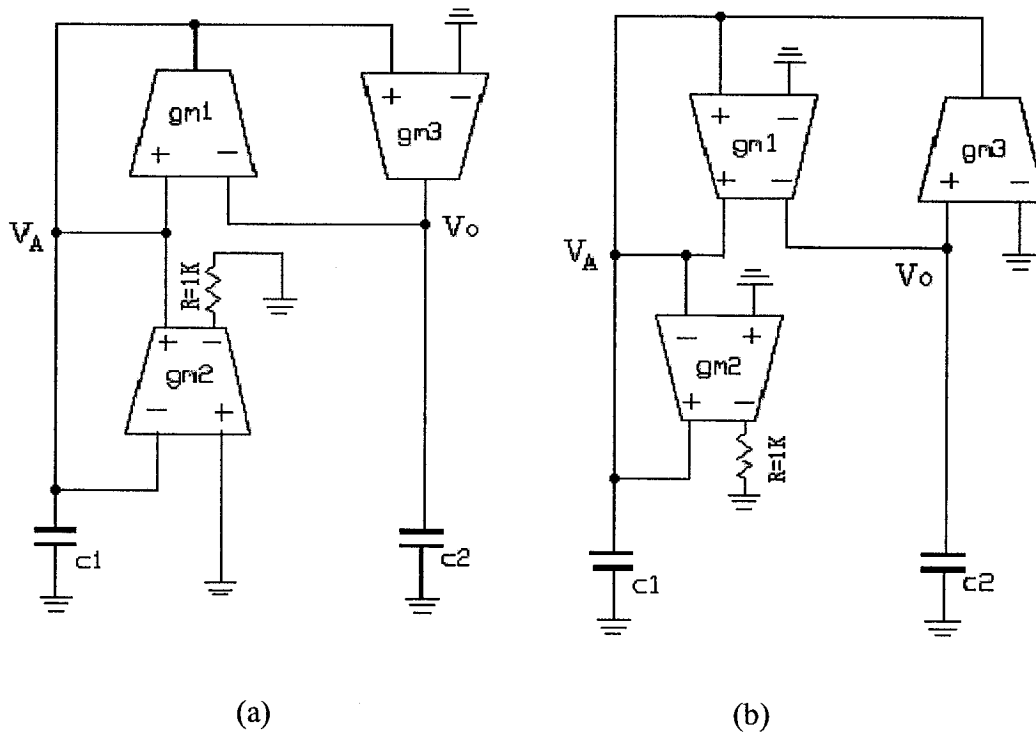


Fig. 5.2 OTA-C oscillator (a) and its transposition (b)

To overcome the narrow range of linearity of the OTA devices, a resistive divider is used to broaden the input linearity range and aid in starting up the oscillation. This is shown in Figure 5.3.

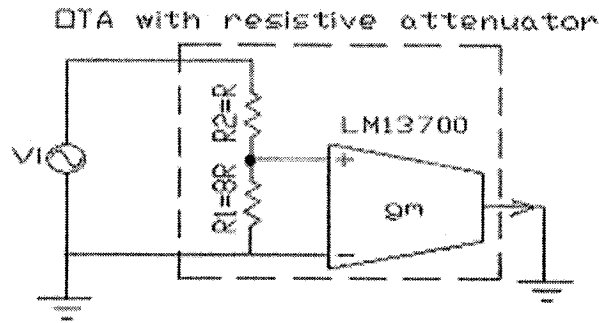


Fig. 5.3 OTA with resistive divider

With the attenuator in place, the transconductance is attenuated by 88.9% (ratio 8/9) while the linearity range is increased to 112.5% (ratio 9/8) because $I_o = 0.889V_i \times gm = V_i \times (0.889 \times gm)$. This decrease in transconductance value is found necessary in order to make sure $b < 0$ in the general characteristic equation $s^2 + bs + c = 0$ so that the roots of the equation is initially placed to the right of the imaginary axis. Thus, the oscillation builds up and then stabilizes at the correct amplitude when the roots move to the left and remain on the imaginary axis.

Fig.5.4 illustrates the variations of the transconductance values as the OTA input signal V_A grows.

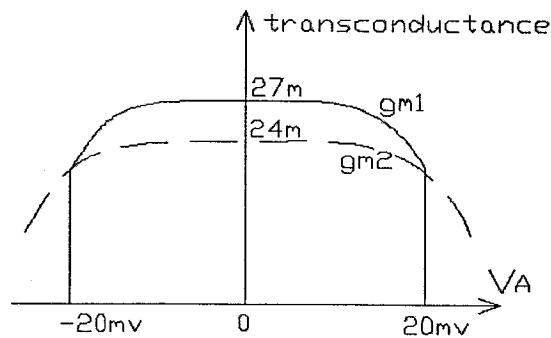


Fig. 5.4 Variation of transconductance

Initially, when $V_A=0$, $gm_1 > gm_2$, oscillation starts up. As V_A increases, the transconductance of gm_1 falls more quickly than that of gm_2 , which makes $gm_1 = gm_2$ at around $V_A = 40mV_{pp}$. Then the amplitude and frequency become stable at this point. Resistive loads of $1\text{ k}\Omega$ have been used to facilitate measurement of the output signals in the both oscillators. Fig.5.5 and Fig.5.6 present the wiring diagrams respectively. To implement the DIDO OTA, two LM13700 devices connected in parallel have to be used where the inputs are interchanged in one of the devices.

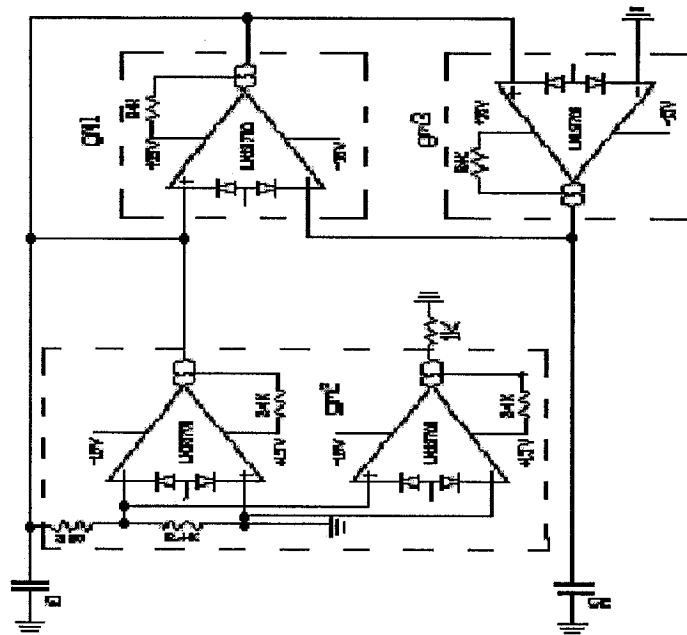


Fig. 5.5 wiring diagram of Fig.5.1

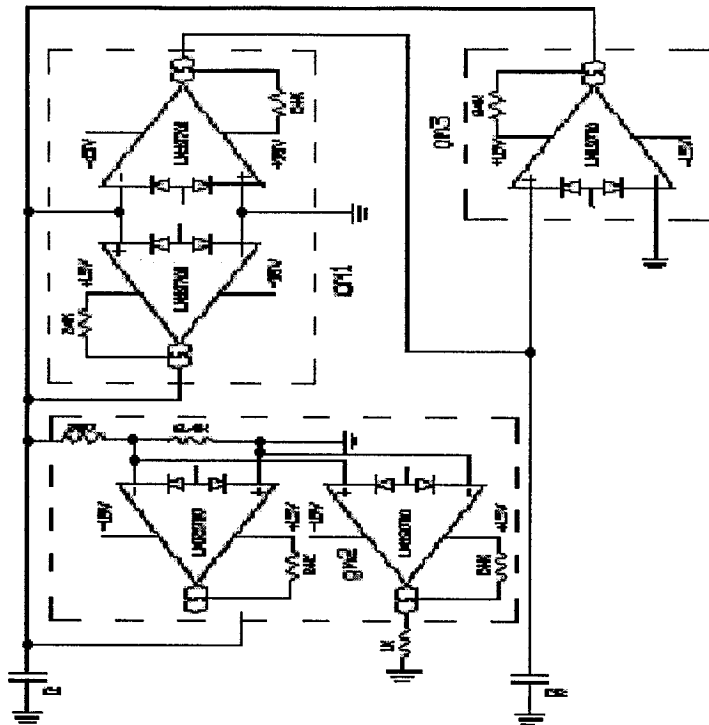


Fig. 5.6 wiring diagram of Fig.5.2

The experimental setup for the oscillator measurement is illustrated in Fig.5.7

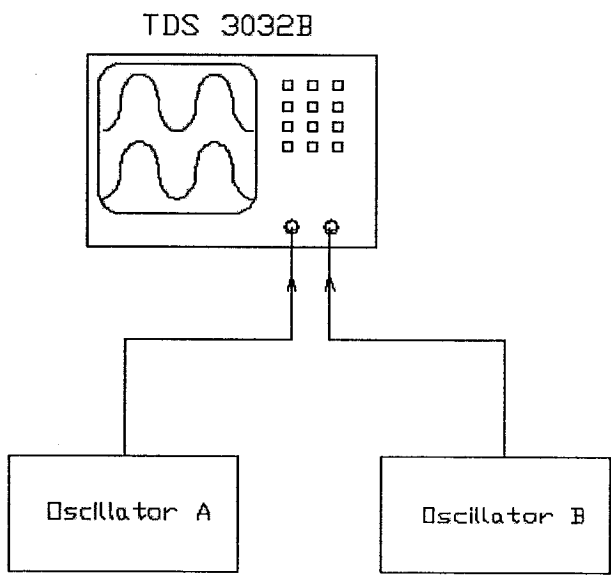


Fig. 5.7 The experimental setup for the oscillators measurement

The output signals of the oscillator A and B are directly sent to the channel 1 and channel 2 of the oscilloscope (TDS 3032B in Fig.5.7), respectively. The output signals observed from the digital oscilloscope is shown in Fig.5.8.

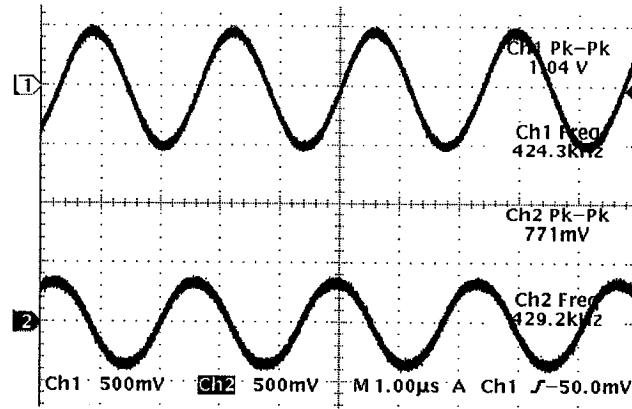


Fig. 5.8 Output signals of OTA-C oscillators in experiment

The voltage waveforms indicate that their frequencies are almost equal with a low distortion. For $g_{m1}=g_{m3}=g_m=27\text{mmho}$, $C_1=C_2=C=10\text{nF}$, the observed frequencies are 429.2 KHz and 424.3 KHz for the oscillators of Figs.5.5 and 5.6 respectively. In theory, $f = \frac{g_m}{2\pi C} \approx 430\text{KHz}$. The small difference may be due to the relative tolerance of the discrete components and/or slight mismatch among the LM 13700 devices.

5.4 Experiments on OTA-C filters

Discrete version of a voltage-mode filter is shown in Fig.5.9 and its transpose, the current-mode counterpart is provided in Fig.5.10. The building blocks are OTAs and capacitors. The transfer functions of these filters are identical and given as:

$$\frac{V_o}{V_{in}} = \frac{I_o}{I_{in}} = \frac{g_{m1}C_2s}{C_1C_2s^2 + g_{m3}C_2s + g_{m1}g_{m2}}$$

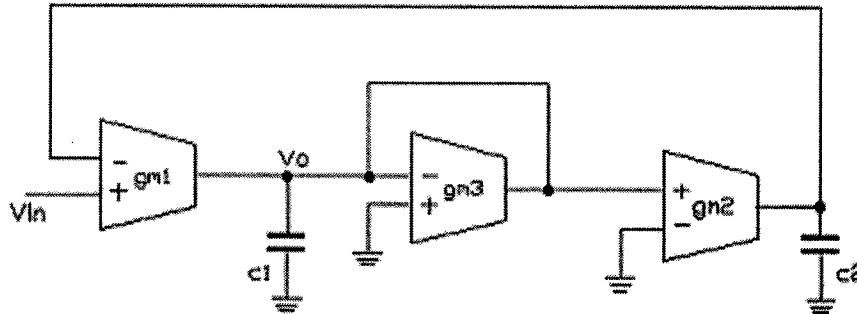


Fig. 5.9 Voltage-mode OTA-C band pass filter

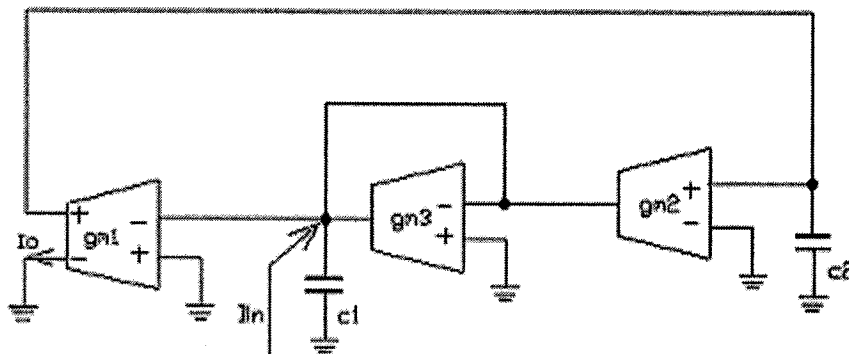


Fig. 5.10 Current-mode OTA-C band pass filter (transpose of the filter of Fig.5.9)

Fig.5.11 and Fig.5.12 respectively present their wiring diagrams. The experimental setup for the filter measurement is illustrated in Fig.5.13.

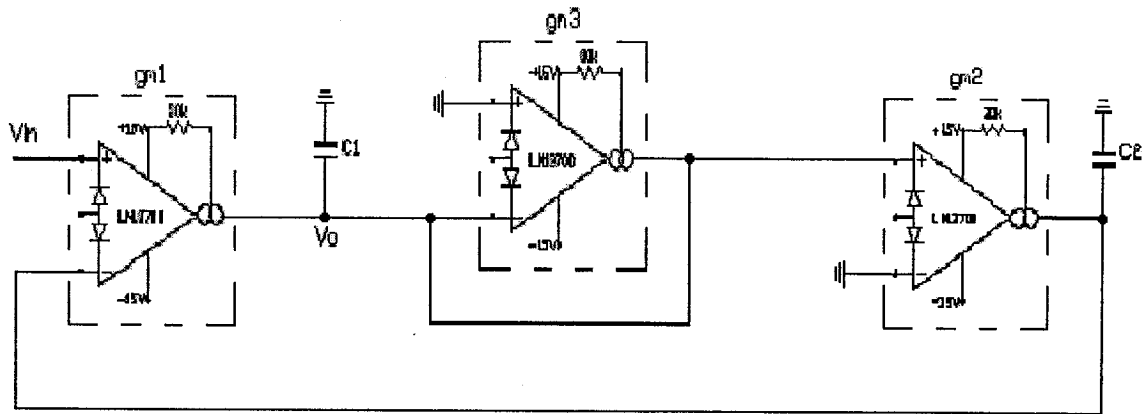


Fig. 5.11 wiring diagram of the voltage-mode filter

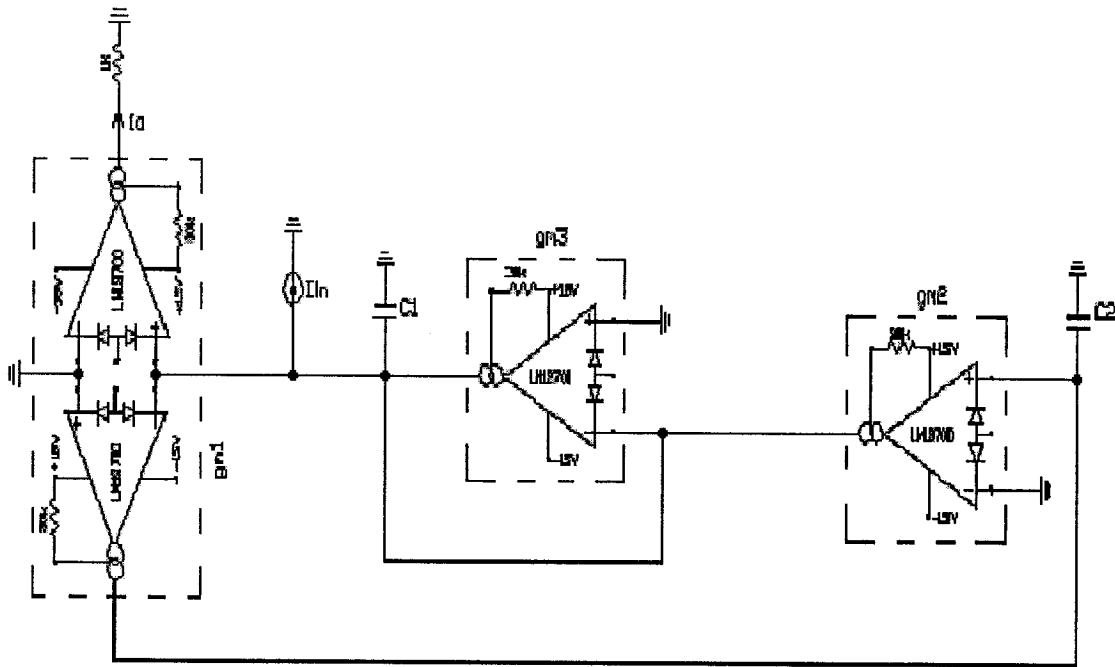


Fig. 5.12 wiring diagram of the current-mode filter

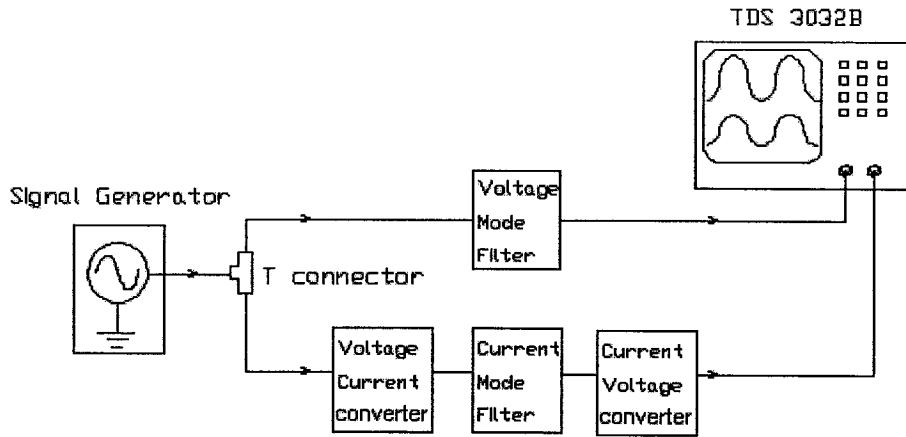


Fig. 5.13 The experimental setup for the filters measurement

The input signal comes from the sine signal generator. This signal is equally distributed by a T connector to the two filters. However, for the current-mode filter, the input voltage signal has to be transformed into current signal. Therefore, another OTA device need to be used as the voltage current converter and its transconductance is set to be 10mmho. Likewise, a 100ohm resistor is connected to the output of the filter to convert the current signal back into voltage signal. Note that the transconductance 10m mho multiplying the resistance 100ohm results in 1, which means the converters pose no effect on the gain of the current-mode filter. Finally, the voltage output signals of the two filters are sent to channels 1 and 2 of the Tektronix digital oscilloscope (TDS 3032B). Thus, these signals can be observed and compared conveniently. As shown in Fig.5.14, the magnitude responses of the voltage-mode and the current-mode filters are almost identical.

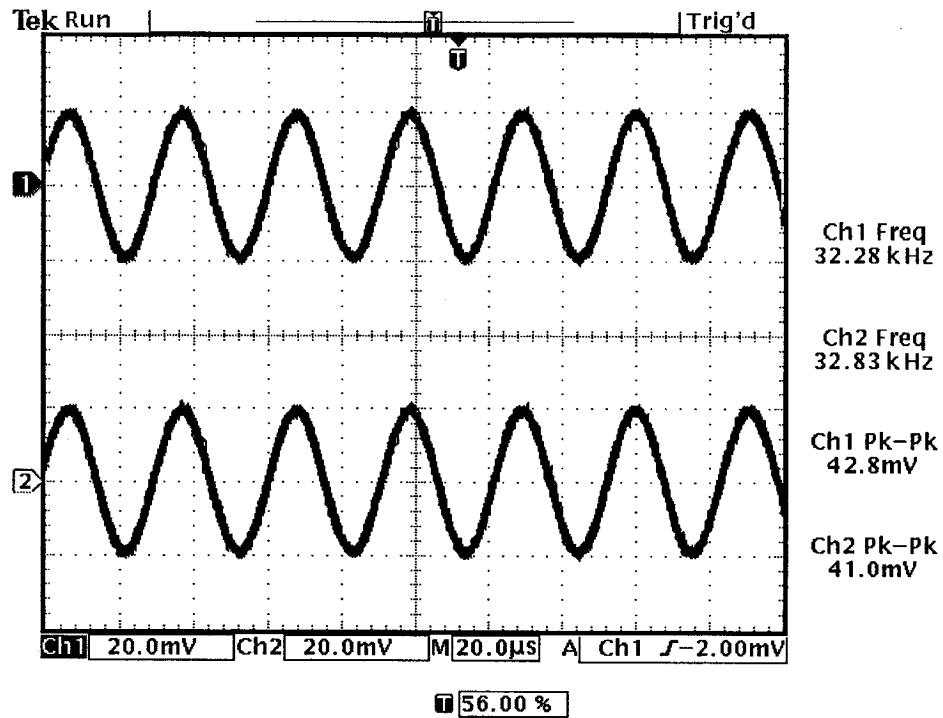


Fig. 5.14 The output signals of the voltage-mode and the current-mode filters

Furthermore, their magnitude responses in frequency domain are shown in Fig.5.15.

With $g_{m1}=g_{m2}=g_{m3}=21\text{mmho}$, $C_1=C_2=C=100\text{nF}$, the recorded center frequencies are around 31.8KHz and 32.4KHz for the voltage-mode and current-mode filters respectively.

In theory, $f = \frac{gm}{2\pi C} \approx 33\text{KHz}$. Hence, the experiment results are in good agreement with the theoretical calculations.

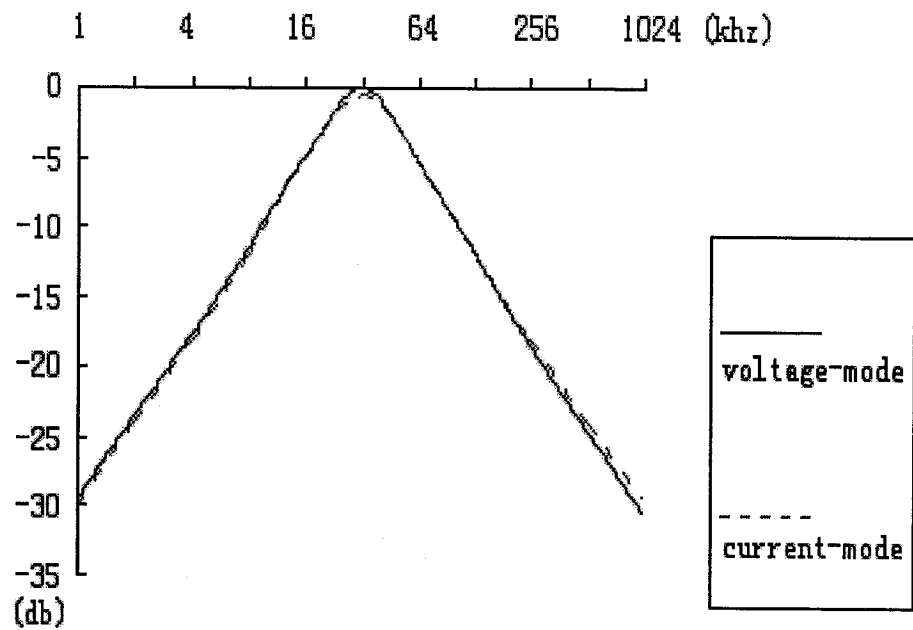


Fig. 5.15 Magnitude-frequency response of the band pass filters

5.5 Summary

To verify the theoretical results obtained through the principle of network transposition, an OTA-C oscillator, an OTA-C band pass filter and their transposed circuits have been built and tested. The LM13700 from National Semiconductors and discrete R, C components have been used to realize these circuits. For the oscillators, the observed frequencies are 429.2KHz and 424.3KHz respectively while the designed frequency is 430KHz. For the filters, the recorded center frequencies are around 31.8KHz and 32.4KHz accordingly while the theoretical value is 33KHz.

Chapter 6 Realization in CMOS Technology

6.1 Introduction

In the previous chapters we used discrete resistance, capacitance and integrated circuit OTA to verify the theoretical results obtained through the principle of network transposition as applied to filters and oscillators. The operating frequency was less than a MHz. Finite frequency response of active devices (i.e., OTA) makes it difficult to build systems at high frequencies. To obviate this difficulty we can take recourse to sub-micron transistors available in modern CMOS technology to build the active device, i.e., OTA, buffer, amplitude limiter, and then realize systems such as an oscillator or a filter. For this purpose, the DIDO-OTA-C filter and oscillator shown in Fig.3.7 and Fig.4.25 respectively have been designed in TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μ CMOS integrated circuit technology. The layout of the oscillator was sent to the Canadian Microelectronics Corporation (CMC) for fabrication.

First, we review the various popular OTA structures and then discuss their advantages and limitations. Then, an OTA structure suitable for low-voltage high-frequency application is chosen for implementation. The undesirable parasitic positive conductance of the OTA is compensated by the use of the negative conductance realized from CMOS transistors [22,23,24]. This technique is further used to start up the oscillations. Then, the design of the amplitude limiter and the input/output (I/O) buffers

are presented; the principle of feedback is used to decrease the impedance of I/O buffer to the standard 50Ω level. Finally, the printed circuit board, which provides the interface between the chip and the testing equipment, is designed; bypass technique is used to reduce the noise from the power supply.

6.2 Selection of the OTA

OTA is the core element in an OTA-C filter or OTA-C oscillator. In the literature, several OTA design techniques targeting at different applications have been described. For example, Raut successfully extended the flat band operation of the transconductor to very high frequencies by suitable sizing of the transistors and using a fully differential signal at the input to cancel the effect of the gate-drain overlap capacitances [22]. The configuration of this OTA is given in Fig.6.1. Assuming that M1-M5, M2-M6, M3-M7 and M4-M8 are matched pairs, it turns out that the differential ac signal output current equals to:
$$i_{out} = 2(g_1 - g_8)v_{in} - 2s(C_{gd1} - C_{gd8})v_{in},$$

where v_{in} is the input ac signal, i.e. $v_{in}=v_1-v_2$ and g_i and C_{gdi} are the transconductance and gate-drain capacitance of the transistor M_i respectively. If the geometric layout of the devices is arranged to make $C_{gd1}=C_{gd8}$, then the output current i_{out} can be expressed as $i_{out}=2(g_1-g_8)v_{in}$. A linear OTA is achieved at the cost of comparably small transconductance value because of the cancellation.

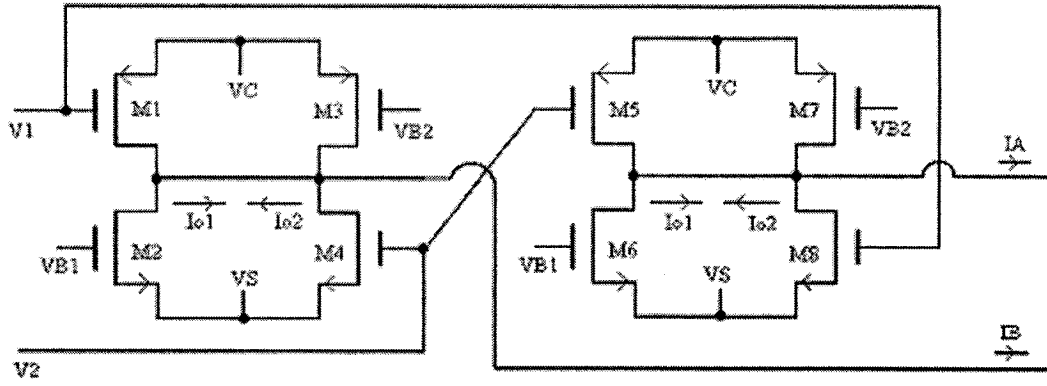


Fig. 6.1 Raut's wideband transconductor

M. F. Li et al. designed a wide input range OTA [25], in which a pair of complementary n-type input OTAN and p-type OTAP circuits are connected in parallel to implement the rail-to-rail differential input range. The principle of this implementation is shown in Fig.6.2. When $V_i > 0$, the OTAN output sinks current at the same time the OTAP output current is zero. When $V_i < 0$, the output current is sourced by the OTAP and OTAN output current is zero. i.e.

$$i_o = i_{ON} = g_{m_n} V_i \text{ when } V_i > \text{ or } = 0; \quad i_o = i_{OP} = g_{m_p} V_i \text{ when } V_i < \text{ or } = 0;$$

where g_{m_n} and g_{m_p} are the transconductances of the OTAN and OTAP respectively, and $V_i = V_{i+} - V_{i-}$ is the differential input signal. In order to ensure linearity over the entire range of the input, the transconductances of the OTAN and OTAP must be equal. This requires a complicated transconductance tuning circuit and leads to a very low -3db cutoff frequency, which is only 0.55 MHz according to the report.

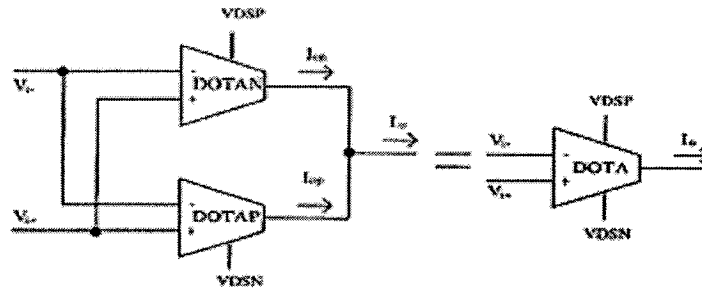


Fig. 6.2 Li's rail to rail OTA

Koziel and Szczepanski proposed an analytical design method of a highly linear OTA [26] shown in Fig.6.3. This OTA combines a cross-coupled quad cell and a source-coupled differential pair, as well as the current mirror technique in the output stage. As a result, improved linearity over the large tuning range is obtained. However, this circuit can hardly work with a power supply below 3.3V because of its five-stack transistor structure.

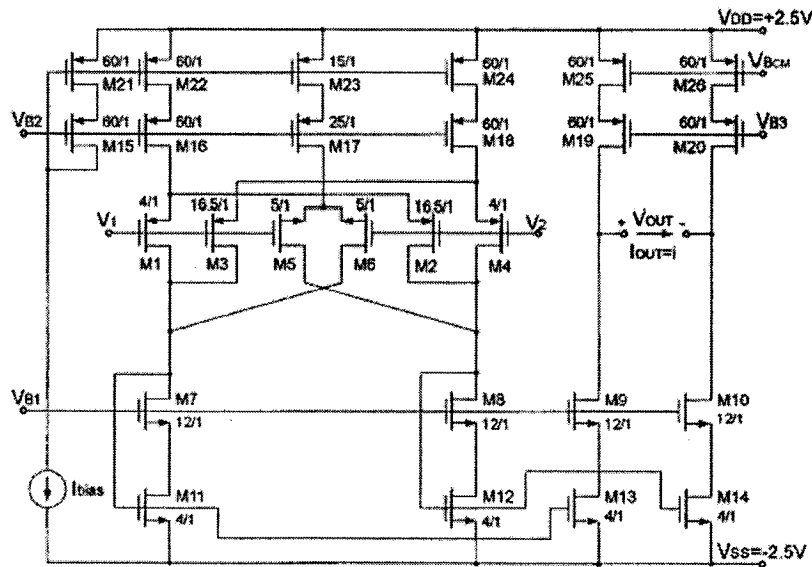


Fig. 6.3 Koziel's highly linear OTA

Recently, Mohieldin et al. proposed a fully balanced pseudo-differential OTA with common-mode feed forward and inherent common-mode feedback detector [27], which is shown in Fig.6.4.

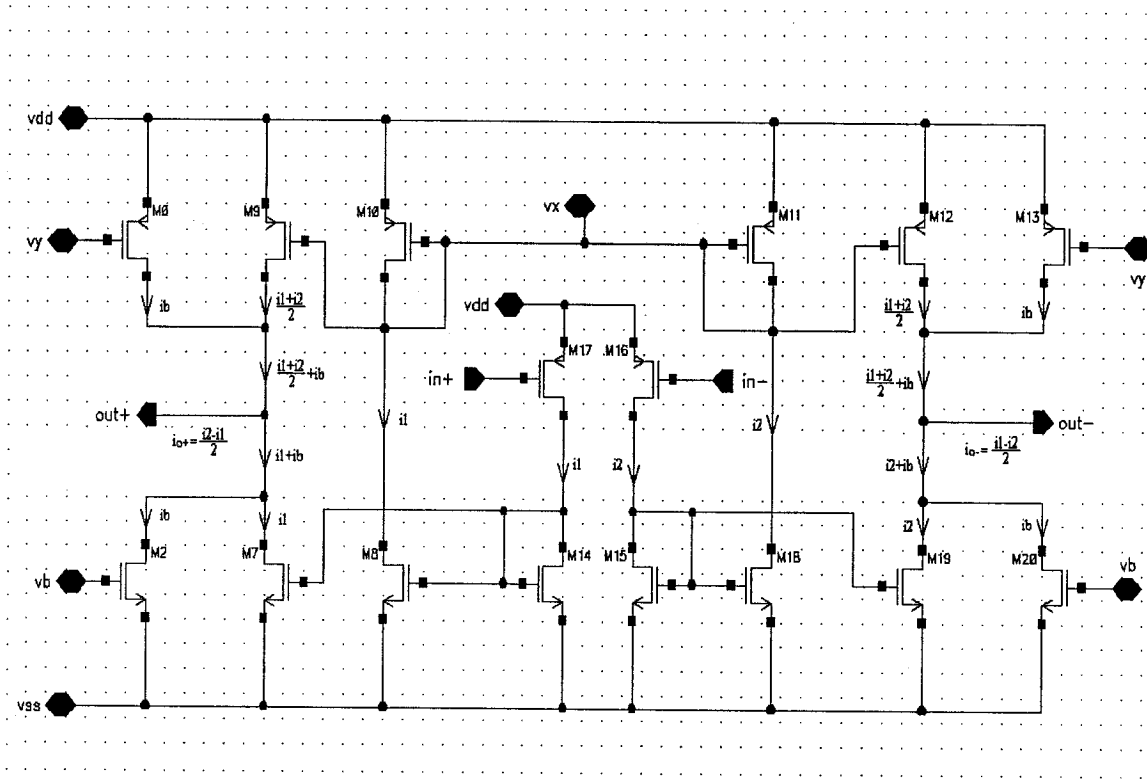


Fig. 6.4 Mohieldin's fully balanced pseudo-differential OTA

In this OTA circuit, the current $\frac{(i_1 + i_2)}{2}$ provides the information of the common-mode level of the inputs. This current is mirrored to the output and is subtracted at the OTA output node. Hence, a feed-forward cancellation of the common-mode input signal is performed, yielding (neglecting short channel effects):

$$i_{od} = i_{o+} - i_{o-} = i_2 - i_1 = \beta \times v_{ov} \times v_d = gm \times v_d,$$

where $\beta = Kp(W/L)_{17}$, $v_{od} = v_{sg17} - |v_{tp}|$ is the overdrive voltage of input transistor M17, $v_d = V_{in+} - V_{in-}$ is the input AC voltage signal and i_{od} is the output AC current signal.

The attractive features of this OTA are: (a) efficient (i.e., fewer transistors) technique for common mode feedback, (b) high rejection for common mode signals, (c) high bandwidth (about 1 GHz with 0.18 micron CMOS technology) for current-mode (i.e., output shorted for ac signals) operation and (d) low voltage operation (1.8V DC and below). Because our work is focused toward low-voltage high-frequency application, this OTA is chosen among the OTAs discussed above. However, no OTA is perfect. From the filter point of view, the major drawback of this OTA is its low output impedance. This makes the realization of the ideal OTA-C integrator very difficult. A lossless integrator in principle becomes a lossy integrator in practice. This seriously deteriorates the low frequency performance of the designed bandpass filter, which will be discussed in detail in the following sections.

6.3 Application of Negative Conductance in OTA-C Filter Case

A fully differential filter shown in Fig.3.8 and redrawn in Fig.6.5 has been designed in TSMC CMOS 0.18 μ m VLSI technological process.

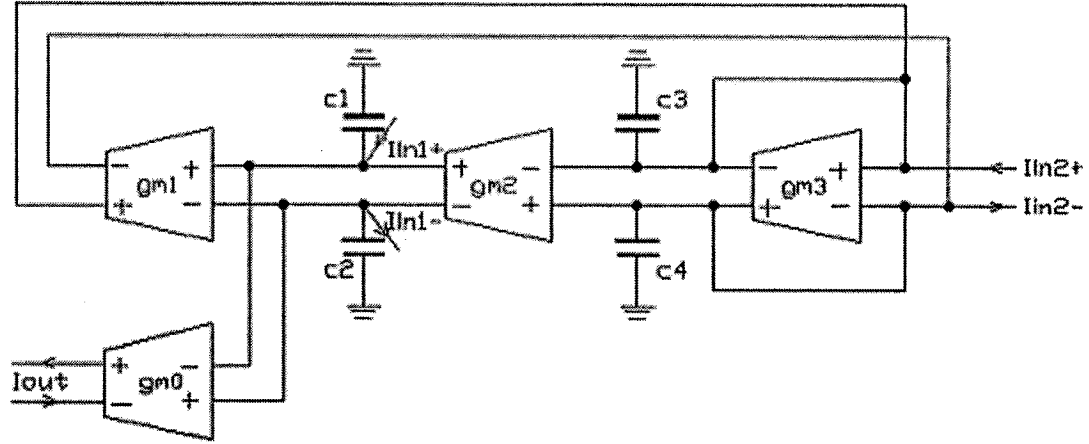


Fig. 6.5 Fully differential current-mode filter

The transfer function of the filter is

$$\frac{I_o}{I_{in1}} = \frac{-g_{m0}C_2s - g_{m0}g_{m3}}{C_1C_2s^2 + g_{m3}C_1s + g_{m1}g_{m2}}, \quad \frac{I_o}{I_{in2}} = \frac{g_{m0}g_{m2}}{C_1C_2s^2 + g_{m3}C_1s + g_{m1}g_{m2}}$$

By setting $I_{in1}=I_{in2}=I_{in}$, $g_{m1}=g_{m2}=g_{m3}=g_m$, $C_1=C_2$ and injecting the input current signals

$$I_{in1}, I_{in2} \text{ at the same time, a band-pass filter is realized as } \frac{I_o}{I_{in}} = \frac{-g_mCs}{C^2s^2 + g_mCs + g_m^2}$$

with center frequency $\Omega = \frac{g_m}{C}$.

However, as mentioned in the section 6.2, the OTA chosen for this project has a relatively low output resistance. When taking this parasitic impedance into account, the transfer function of the filter of Fig.6.1 becomes

$$\frac{I_o}{I_i} = \frac{Cg_ms + 2g_og_m}{C^2s^2 + (Cg_m + 3Cg_o)s + (2g_o^2 + 2g_og_m + g_m^2)}$$

where, the OTAs are assumed to have identical parasitic output conductance g_o .

Comparing it with the transfer function in the ideal case, which is

$$\frac{I_o}{I_{ii}} = \frac{Cg_m s}{C^2 s^2 + Cg_m s + g_m^2},$$

one can find that OTA parasitic resistance affect especially

the low frequency response of the OTA-C band pass filters. This is a common problem with a double-stack OTA structure. The simulated frequency response of this filter shown in Fig.6.6 gives this problem a clearer exposure. In the above, the following values were used: $g_m=0.94\text{m mho}$, $g_o=0.14\text{m mho}$, $C=0.65\text{pF}$.

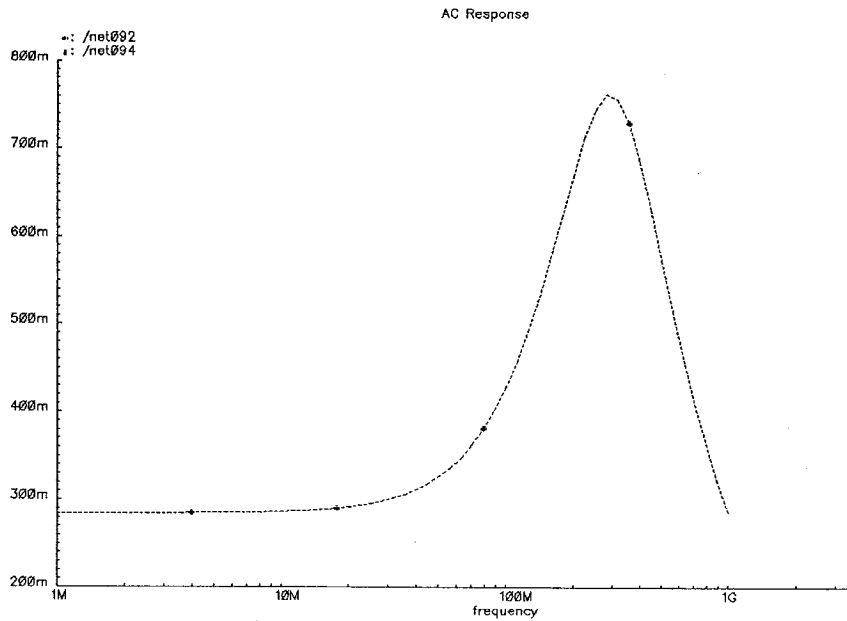


Fig. 6.6 Frequency response of the performance-degraded band pass filter

A common method of improving the output resistance of the OTA is to use a cascode structure at the output stage. But this method does not work well with a power supply as low as 1.8V. A technique that can enhance the output resistance without increasing the number of stacks in the OTA structure is to add a negative conductance [22,23,24] at each of the output terminals of each of the OTAs. As shown in Fig.6.7,

M37 and M38 introduce local positive feedback between the output terminals, leading to a negative conductance to cancel the parasitic conductance of the OTA.

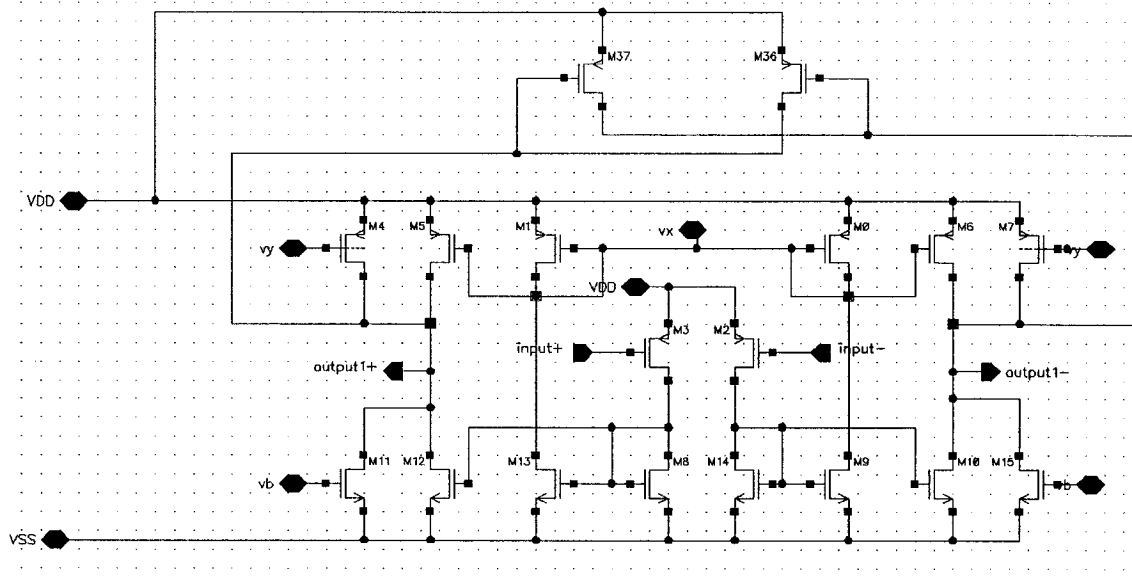


Fig. 6.7 Output impedance enhanced OTA

Fig.6.8 illustrates the small signal macro model of the OTA, including the parasitic output conductance g_p in parallel with a negative conductance g_n .

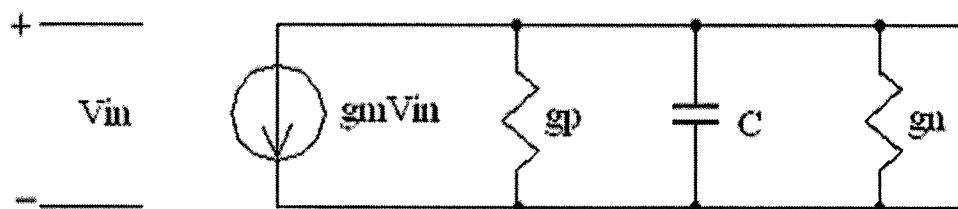


Fig. 6.8 OTA small signal macro model

The total output conductance of the OTA becomes $g_o = g_p - g_n$. In principle, if $g_p = g_n$ then

$g_o=0$ and the total output resistance $r_o = \frac{1}{g_o}$ becomes infinite. However, it is impossible

to set them exactly equal since they depend on the process and environment. Hence in practice, by optimizing the sizes of the transistors M37 and M38, we make g_n smaller than g_p by about 1μ mho to achieve an output impedance value as high as $1M\Omega$. The improvement in the performance of the filter is illustrated in Fig. 6.9. Here all the OTAs are designed to have $g_m=0.94m$ mho. The total capacitance for each capacitor is estimated as $C_t=C_1 + C_p$, where C_1 is the layout capacitor value which is set to $0.5pF$, and C_p is the parasitic capacitance which is estimated to be $0.15pF$. So C_t becomes $0.65pF$.

For the designed filter, the center frequency is estimated as $f_o = \frac{g_m}{2\pi C_t} = 230MHz$.

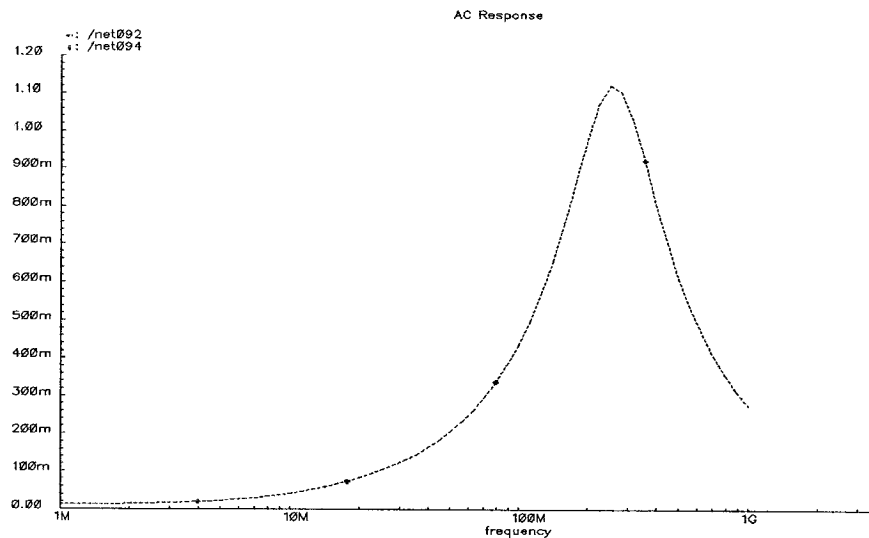


Fig. 6.9 The improved frequency responses of band pass filter

On the other hand, if we purposely make g_n larger than g_p so that g_o becomes negative, then we can take advantage of the negative output conductance of the OTAs in the design of oscillator circuits, which will be described in the following section.

6.4 Use of Negative Conductance in OTA-C Oscillators

The oscillator using DIDO OTAs shown in Fig.4.25 and redrawn in Fig.6.10 has been designed and implemented. The characteristic equation of the oscillator is:

$$s^2 - \frac{(gm_3 - gm_4)}{C_1} s + \frac{gm_1 gm_2}{C_1 C_2} = 0.$$

To start the oscillation, $gm_3 - gm_4 > 0$ has to be satisfied.

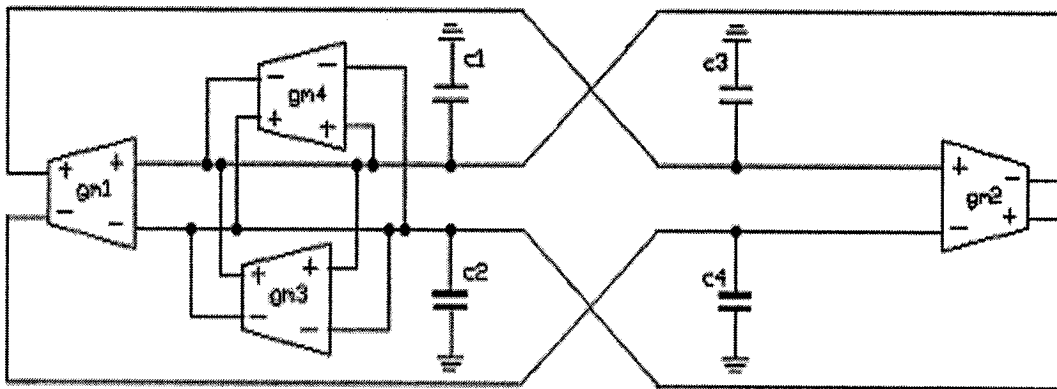


Fig. 6.10 An oscillator using DIDO OTAs

An ideal OTA-C oscillator consists of two lossless integrators (one inverting and one non-inverting) cascaded in a loop, which results in a characteristic equation with a pair of roots lying on the imaginary axis of the complex frequency plane. In practice, however, parasitic components may cause the roots to be inside the left half of the complex frequency plane, thereby preventing the oscillation to start. Any practical OTA-C oscillator must include some form of negative conductance to cancel these

parasitic conductance and ensure that the roots are initially located in the right half plane. In Fig.6.10, gm_3 and gm_4 provide this function. Besides, some amplitude stabilization mechanism must be added to pull the roots back towards the imaginary axis until a stable value for the amplitude is obtained. A practical implementation of OTA-C oscillator is shown in Fig.6.11. This includes a pair of limiters for stabilizing the amplitude.

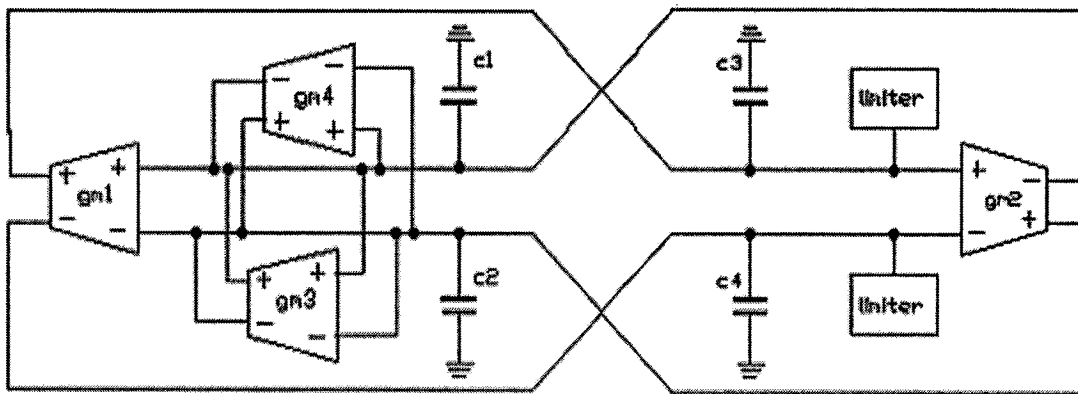


Fig. 6.11 OTA-C oscillator with amplitude limiter

In the above, the inverting integrator consists of gm_2 , C_1 and C_2 , whereas the non-inverting integrator consists of gm_1 , C_3 and C_4 . Negative conductance consisting of gm_3 and gm_4 is to start up the oscillation. Two limiters are connected to the outputs of gm_1 to stabilize the amplitude of oscillation. One question might arise why two OTAs instead of one are used to realize the negative conductance? This is because a large negative conductance will move the roots farther into the right-half plane, forcing the amplitude control mechanism to work harder and causing the distortion level to increase.

So it is necessary to keep negative conductance as small as possible as long as it can start up an oscillation. Generally, a small negative conductance leads to a design with long-channel transistors biased at low current level, which increases the size of circuit, degrades the frequency performance; while two OTAs canceling each other can easily do it by virtue of the relation $g_{total}=gm_4-gm_3$. Fortunately, the negative conductance technique introduced in section 6.4 can also work with this oscillator circuit. In other words, if gm_1 or gm_2 or both in Fig.6.11 displays appropriate negative output conductance characteristics, gm_3 and gm_4 may not be required. Fig.6.12 shows this version of the OTA-C oscillator.

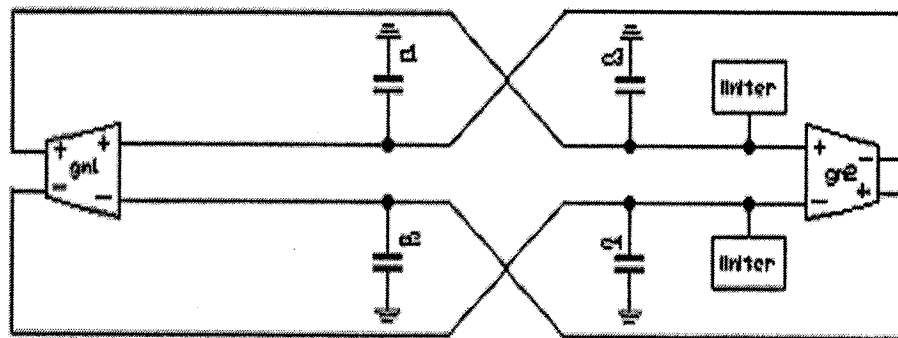


Fig. 6.12 Oscillator with negative-output-conductance OTA

6.5 Amplitude Limiter in the Oscillator

At the start-up, the oscillation amplitude will increase exponentially until limited by the non-linear transfer characteristic of the device. The amplitude-controlling mechanism is intended to limit the growth of the amplitude and regulate the output level so that the

amplitude stabilizes before the onset of the non-linearity. This provides better controllability [11].

An amplitude limiter is a nonlinear resistor exhibiting a voltage-current transfer characteristics as shown in Fig.6.13. A very simple CMOS implementation of this non-linear characteristics is given in Fig.6.14. Here, the bias voltage lim_+ and lim_- are the positive and negative setting values respectively, which can be symmetrically changed from 50 to 100 mV to control the oscillation amplitude. The node *ext* is the external node connecting to each output terminal of the oscillator.

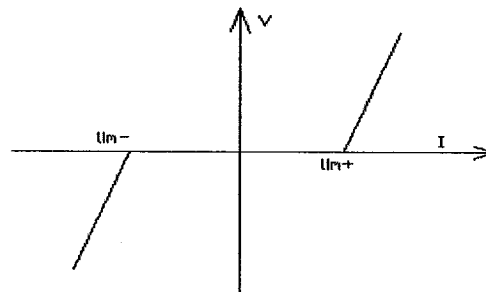


Fig. 6.13 Amplitude limiter driving point characteristics

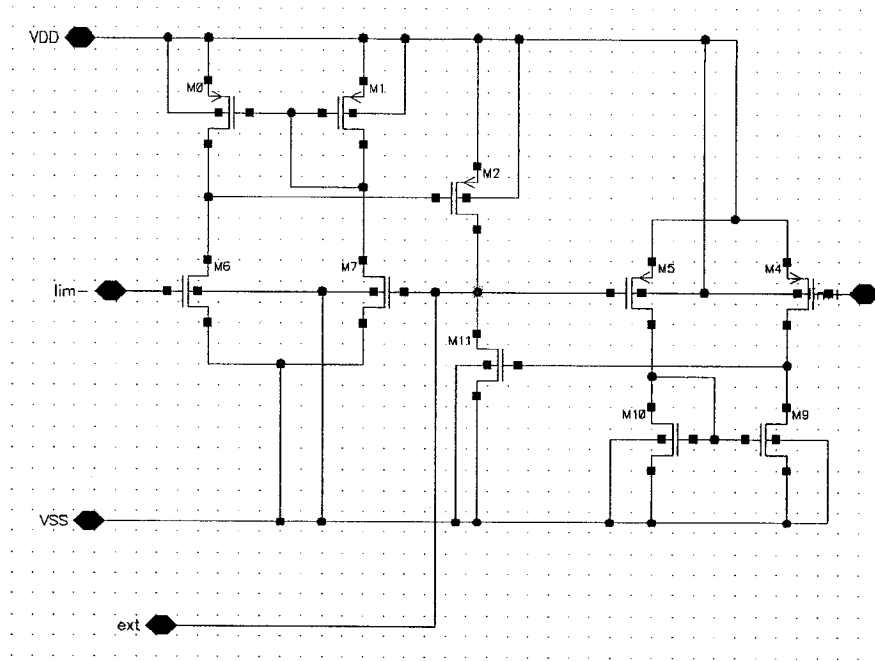


Fig. 6.14 CMOS implementation of the amplitude limiter

6.6 Input and Output Buffers

For high frequency circuits, proper matching of impedance, which is nominally 50 ohm, at both the input and the output ports is necessary to avoid reflection. On chip buffers also facilitate characterization of the system under test more accurately. Several input and output buffer architectures are available in the literature [28]-[33], but almost all of them are designed to work with a power supply voltage of 3.3v or higher. Under low power supply of 1.8v or 1v, when the threshold voltage V_T becomes close to one rail of power supply, stacked structures may not work properly. For our systems an input buffer and an output buffer exploiting feedback techniques as used in current conveyor implementation [28] have been designed. A test bench system diagram where these

buffers are employed is depicted in Fig.6.15.

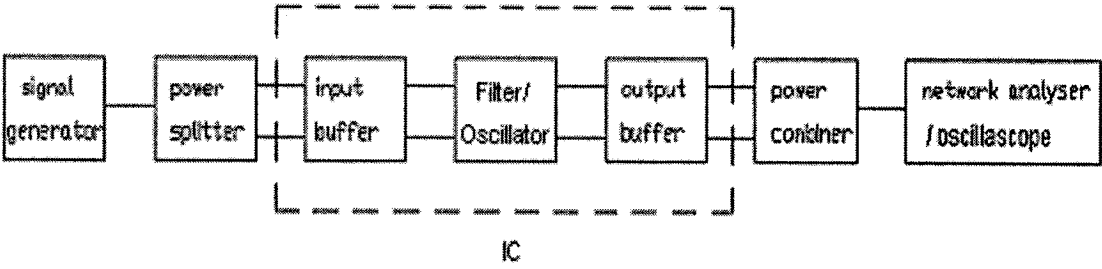


Fig. 6.15 Test bench structure

The buffer circuits are designed for operation over bandwidth up to about 1 GHz. The circuit schematics of input buffer and output buffer are given in Fig.6.16 and Fig.6.17 respectively.

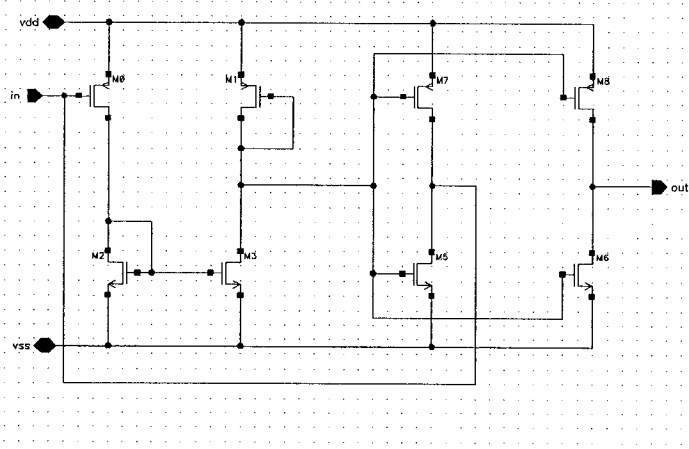


Fig. 6.16 CMOS input buffer

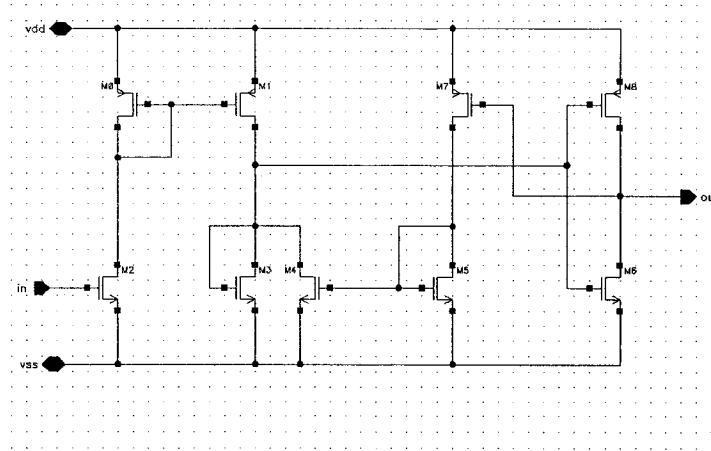


Fig. 6.17 CMOS output buffer

It can be seen that each buffer has a feedback path to reduce the impedance level at either the input or the output terminal as required. The simulated frequency responses of the input (output) impedance for the input (output) buffer are presented in Fig.6.18 and Fig.6.19 respectively. The responses are flat with a value of 50 ohm up to about 600 MHz. Each buffer consumes about 9mW of power.

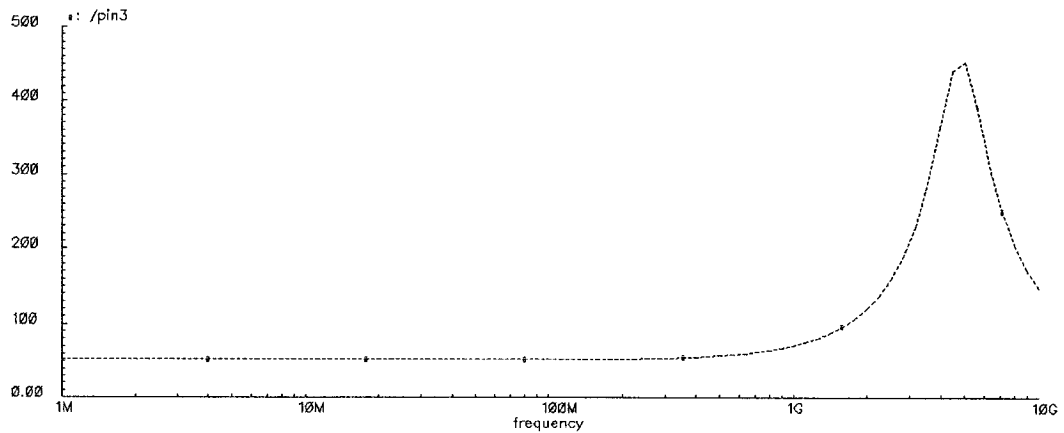


Fig. 6.18 Input buffer frequency response

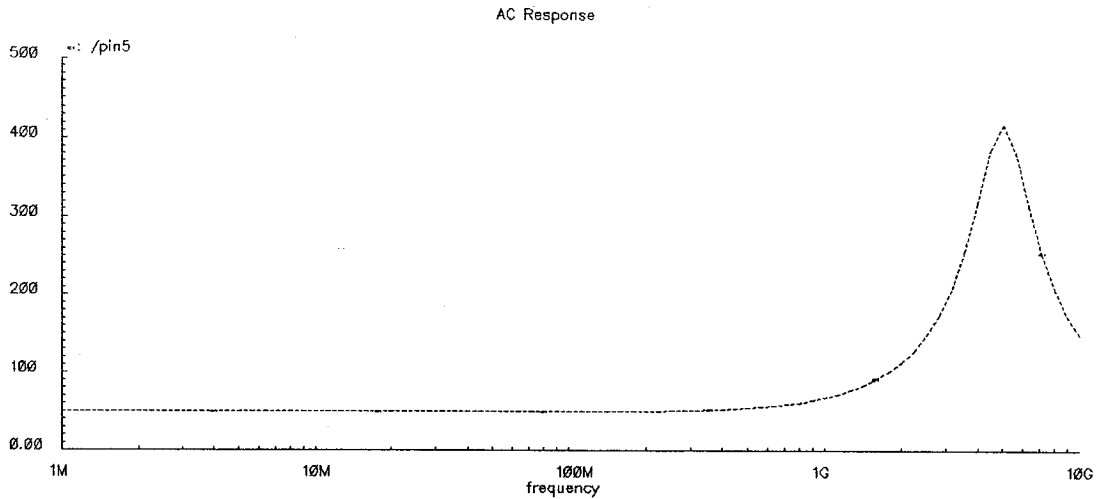


Fig. 6.19 Output buffer frequency response

6.7 Circuit layout

After various building blocks have been designed and laid out, the complete system is obtained by putting these building blocks together and interconnecting properly. In general, the layout should be symmetrical for the purpose of matching. The input and output pins are arranged to be far away from each other to decrease the signal interference. The input/output buffers are put close to the corresponding pins so that the signal routes are kept as short as possible. As a rule of thumb, the current density $1\text{mA}/\mu\text{m}$ should be used for calculating the metal width. Considering that the total power consumption of the chip is around 30mW with 1.8VDC supply voltage, $40\mu\text{m}$ width is chosen for the main power supply metal lines. The completed circuit layout is given in Fig.6.20. The whole die area is $1000 \times 1000 \mu\text{m}^2$ inclusive of the pad frame. The die is

bonded to a 40 pins of DIP (Dual In-line Package) as shown in Fig.6.21. All the OTAs in this die are designed to have identical transconductance, namely, $g_m=0.94\text{m mho}$. All the grounded capacitors are layout to possess the same capacitance, namely, 0.5pF . Taking the parasitic capacitance of the OTAs and interconnection routes into account, the total capacitance at each concerned node is $C_t=C_l+ C_p$, where C_t is the total capacitance, C_l is the layout capacitor value which is set to 0.5pF , and C_p is the parasitic capacitance which is estimated to be 0.15pF . So C_t becomes 0.65pF . For the designed oscillator, the oscillation frequency is also estimated as $f_o = \frac{g_m}{2\pi C_t} = 230\text{MHz}$.

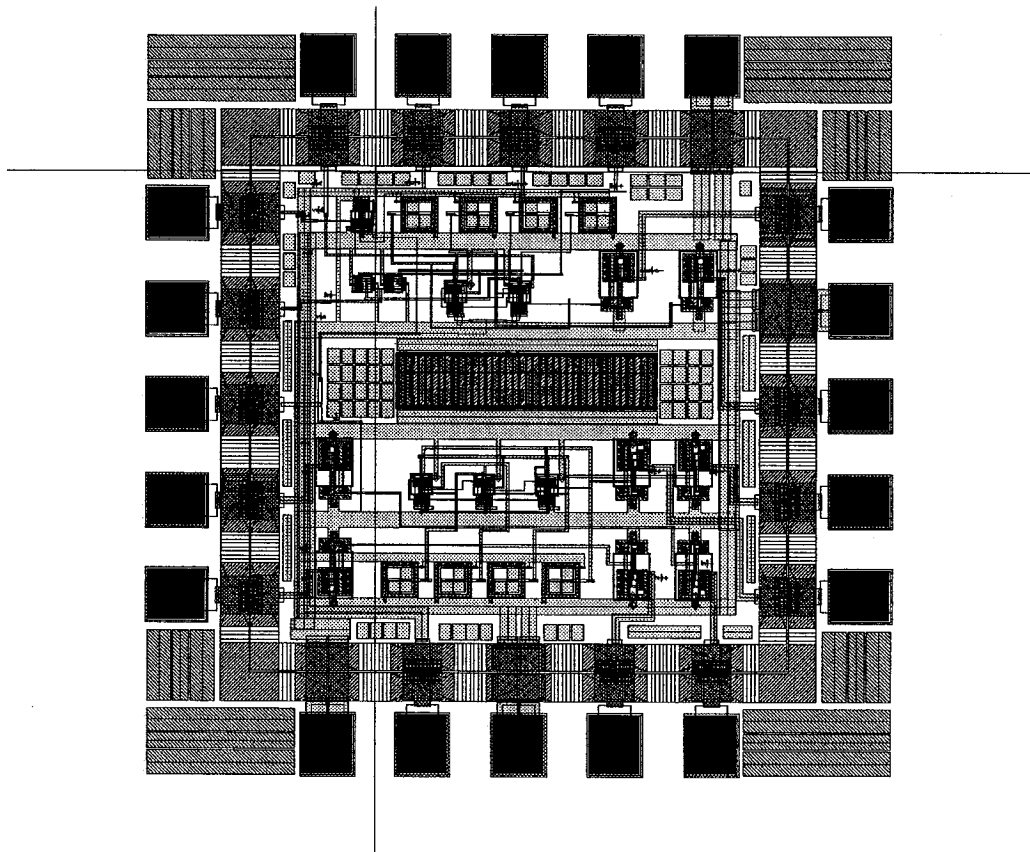


Fig. 6.20 Chip layout

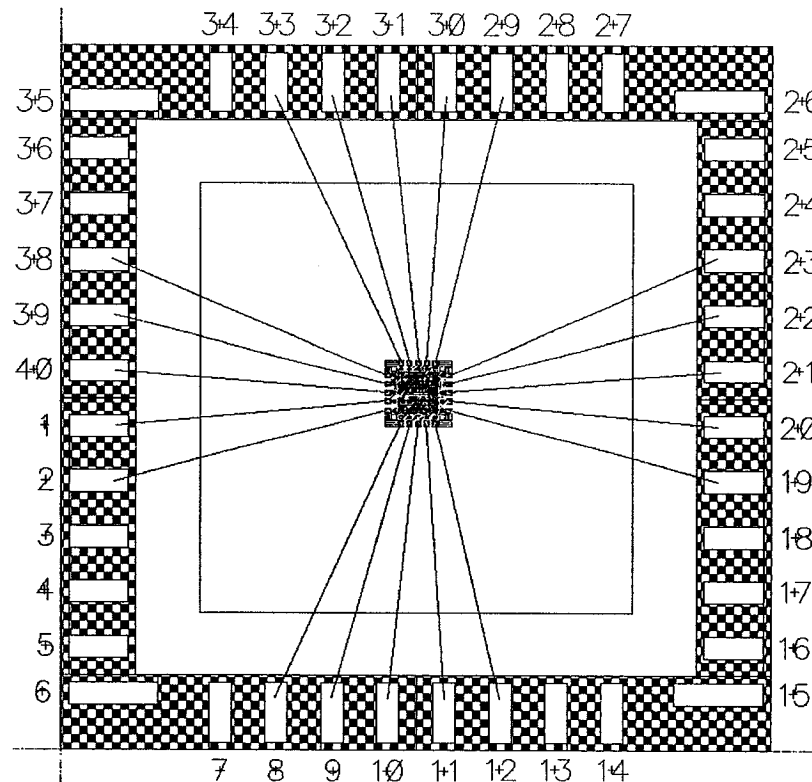


Fig. 6.21 Bonding Diagram

6.8 Printed Circuit Board Design

Printed circuit board provides a base for chip and an interface between chip and testing equipments. In the design of printed circuit board, proper bypassing is essential. Even if there are no digital circuits present in the system and no ground and supply bounces exist, proper bypassing of the supply lines provides for an effective filtering scheme against the high frequency components on the ground and DC power lines. An ideal bypassing mechanism would provide a zero impedance path for the DC power to the chip and an infinite impedance path for all other frequencies. The use of shunt

capacitors provides a low pass function which shunts the high frequency components to ground. However, the resistance of the bypass node is typically very low and the low-pass cutoff frequency is therefore very high, resulting in an inefficient bypassing scheme. Here, a series inductor is necessary to achieve a higher order low pass function. By providing a series inductor, the impedance seen by the capacitor is increased significantly, resulting in a much better bypassing scheme. Totally, two 1 nF inductors and two 100 μ F capacitors are placed on the printed circuit board to decouple power supply noise. In addition, eight BNC connectors surrounding the chip will be connected to the power splitter when testing; two 10k ohm resistors are used for DC measurement purpose. The final printed circuit board has dimensions 72mm x 82mm. The layout is given in Fig.6.22.

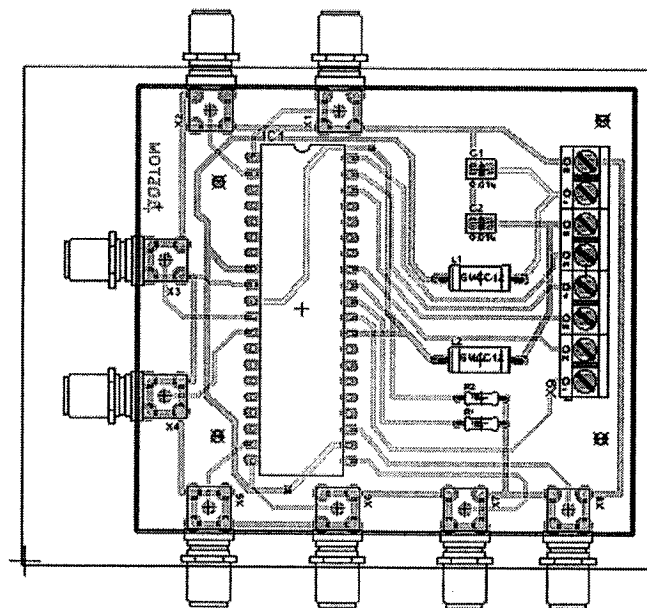


Fig. 6.22 Layout of printed circuit board

6.9 Summary

This chapter described IC design strategies for the DIDO-OTA-C filter and oscillator in CMOS 0.18 μm process. The degradation of the output impedance of the OTA for low voltage operation has been overcome by using the negative conductance canceling technique. This negative conductance not only improved the performance of the filter, but also replaced two OTAs in the original oscillator. The CMOS amplitude limiters have been used to stabilize the oscillation. New low impedance wideband on chip buffers have been designed for ease of system level measurements over a wide frequency range. Finally, the design of printed circuit board has been presented; bypass technique was employed to reduce the noise from the power supply.

Chapter 7 Simulation and Measurement Results

7.1 Introduction

It is important that the functioning of the circuit is re-checked after the circuit has been physically laid out, because the interconnecting tracks will add a capacitive loading to the signal lines which increases the delays, and may cause it to function out of specification. This chapter presents post-layout simulation results of the OTA-C filter and the OTA-C oscillator and measurement results of the oscillator chip fabricated with the assistance of Canadian Microelectronics Corporation (CMC). Original circuit configurations need to be modified so as to conform to the voltage-mode dominated simulators such as Hspice and SpectreRF. Some basic parameter definitions about linearity and phase noise will be given, followed by related simulation results. Then, the experimental setup for testing the fabricated chip will be described; the results will be presented and discussed.

7.2 Hspice vs. SpectreRF

SPICE is a powerful general purpose analog circuit simulator that is used to verify circuit designs and to predict the circuit behavior. It was originally developed at the Electronics Research Laboratory of the University of California, Berkeley (1975). As its

name implies: **S**imulation **P**rogram for **I**ntegrated **C**ircuits **E**mphasis, SPICE is of particular importance for integrated circuit simulation. HSpice is a version of SPICE that runs on workstations and larger computers.

SpectreRF is a SPICE-like simulator from Cadence. It has several extensions over ordinary SPICE, including Periodic Steady-State (PSS) analysis and Periodic Noise (Pnoise) analysis. Periodic Steady-State (PSS) analysis is a large-signal analysis that directly computes the periodic steady-state response of a circuit. With PSS, simulation times are independent of the time constants of the circuit, so PSS can quickly compute the steady-state response of circuits with long time constants, such as high-Q filters and oscillators. Swept Periodic Steady-State Analysis (SPSS) is a PSS option that is available only in the Analog Artist Simulation Environment. An SPSS analysis performs a sweep of multiple PSS analyses. One can sweep by frequency, by time, or by a design variable. The Periodic Noise (Pnoise) analysis is similar to conventional noise analysis except that it models frequency conversion effects. It can compute the phase noise of oscillators as well as the noise behavior of other similar circuits. SpectreRF provide additional functions in simulating high frequency analog and RF circuits. In this thesis work, Hspice is used for DC, AC and harmonic distortion analysis; SpectreRF is used for intermodulation distortion and phase noise analysis. In both the simulators, the MOS device models are typical model (TT model) for NMOS and PMOS in level 49. The temperature is set to 25 °C.

7.3 Schematic for the simulated circuits

In various integrated circuit simulators, analog circuit is conventionally assumed to be single-input, single-output and in voltage-mode, since this is the most common case. In this project, the filter is, however, in the current-mode, and has two pairs of differential inputs and one dual output. To make it suitable for the simulators, some elements need be added to convert the signals. As shown in Fig.7.1, four VCCS, $G_0 \sim G_3$, are used to change the single input voltage signal from V_2 to two pairs of differential current signals injecting into Pin1, Pin2, Pin3, Pin4. At the output terminals, two 1k ohm resistors are used as symmetrical loads; one VCVS, E_0 , is employed to convert the differential voltage signals on the resistors into single voltage output signal. Note that all the controlled sources in Fig.7.1 are assumed to be ideal, i.e., no impedance with VCCSs and no conductance with VCVS. So they impose no effect on the bandwidth performance of the tested circuit. In addition, V_0 and V_3 are positive and negative power supplies respectively connected to the Pins VDD and VSS; V_5 is a bias voltage source connected to Pins V_b . Pin GND represents ground.

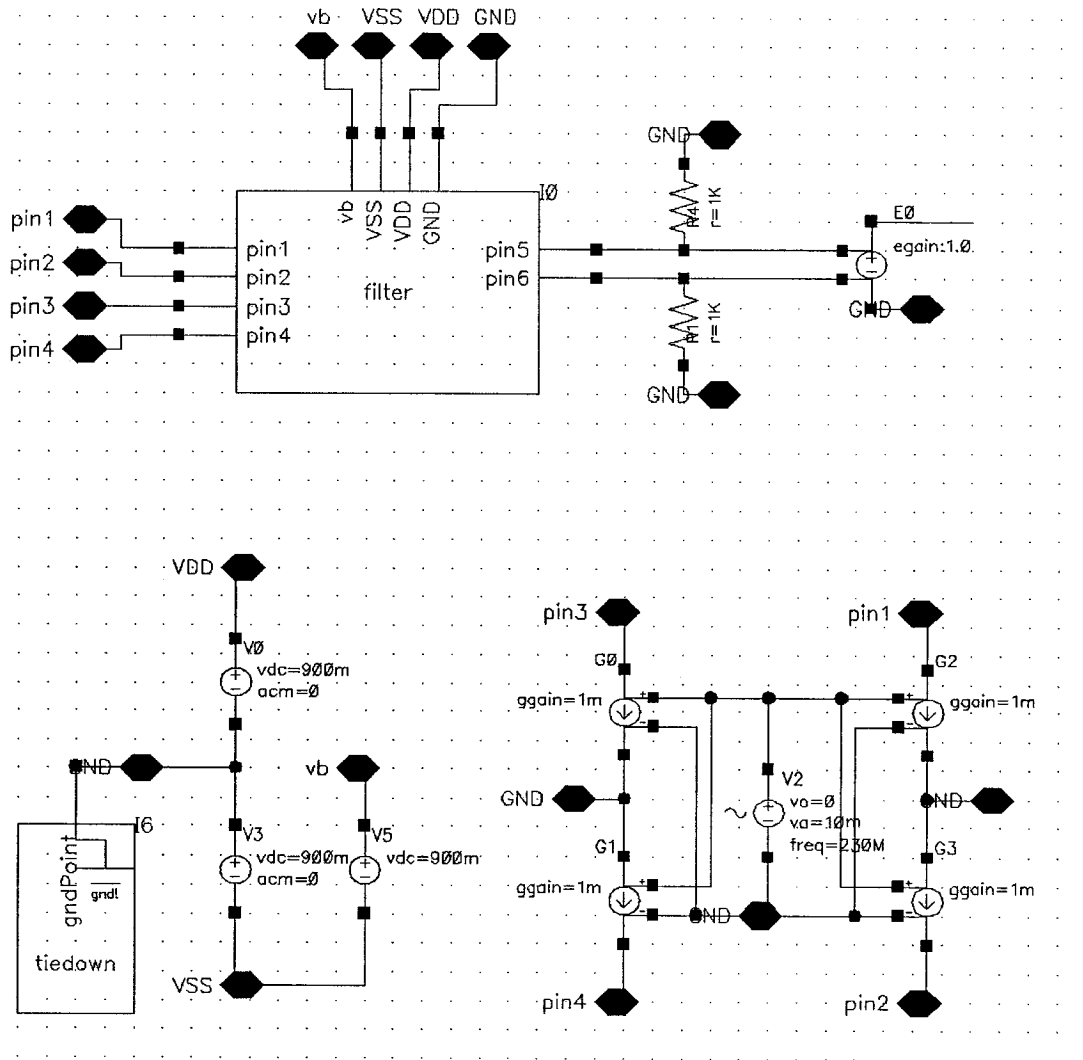


Fig. 7.1 Filter simulation configuration

Likewise, the test configuration of the oscillator is shown in Fig.7.2. V_7 and V_8 are positive and negative power supplies respectively connected to Pins VDD and VSS; V_6 is the bias voltage source connected to Pin V_b . V_1 and V_4 are the bias voltages for the amplitude control circuit and connected to Pins V_{b+} and V_{b-} . Two resistors are also used as symmetrical loads.

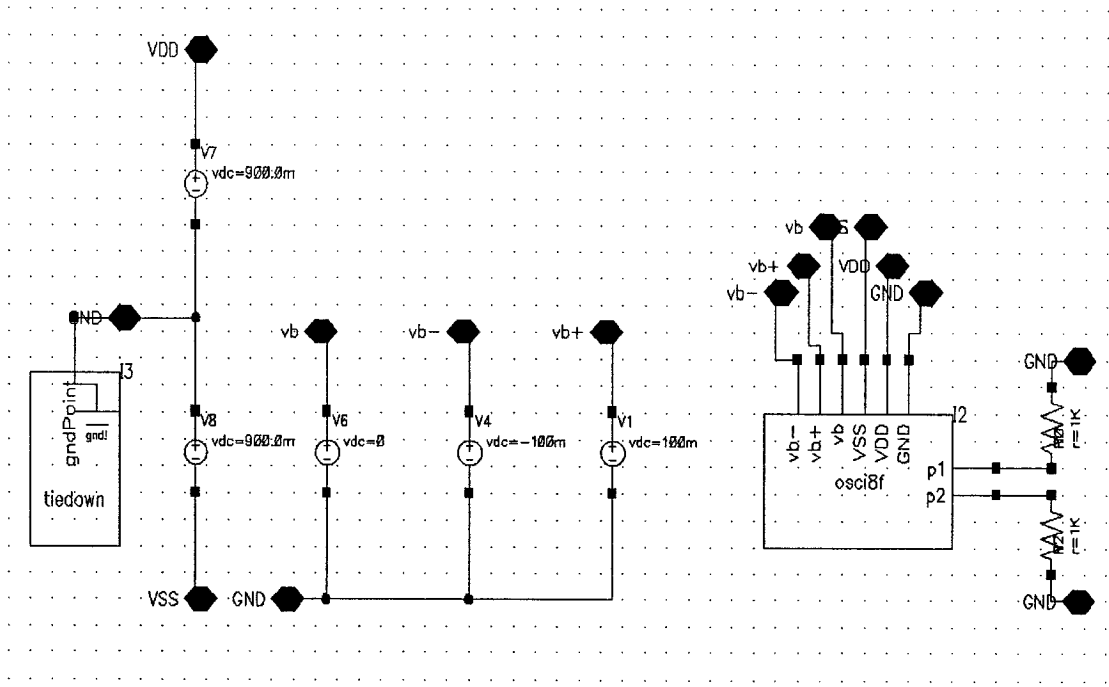


Fig. 7.2 Oscillator simulation configuration

7.4 Simulated Performance

7.4.1 DC, AC and Transient Characteristics of the Filter

DC operating point analysis is critical to the realization of any successful simulation because the operating point determines the bias points within a circuit, which directly affects the gain and linearity characteristics of the circuit. On the other hand, AC and transient analyses are respectively frequency and time dependent. In most cases, AC and transient analyses require three basic elements to function:

- 1) An input source to stimulate the circuit being evaluated.
- 2) A definition of a sweep range to bound the analysis.

3) A definition of the output voltage or current to be evaluated.

For a band-pass filter, the magnitude response is the most important characteristic, which can be simulated by selecting the AC analysis mode in Hspice simulation.

To evaluate the AC characteristics of the filter (see schematic in Fig.7.1) we first set V_2 as a sine signal source with 1V peak-to-peak magnitude, and then sweep its frequency from 10MHz to 1GHz. What appears at the output of E_0 is the magnitude frequency response of the filter as shown in Fig.7.3. The post-layout simulation result shows that the center frequency of the band pass filter is around 220 MHz, which is very close to the calculated value of 230MHz.

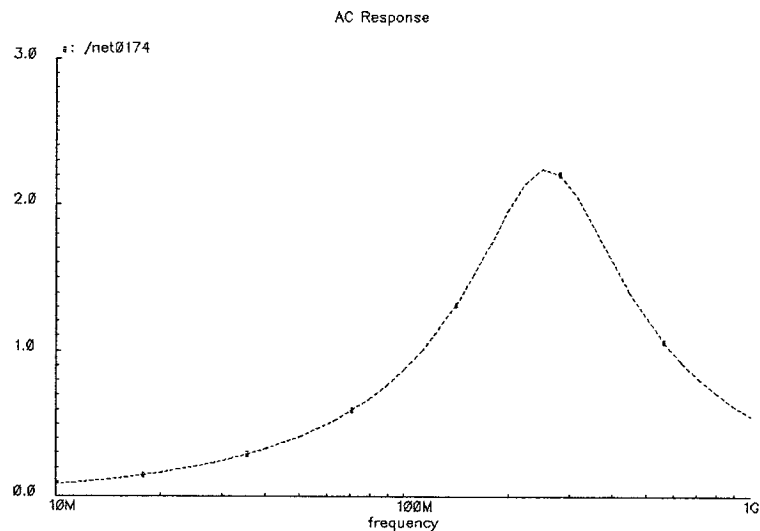
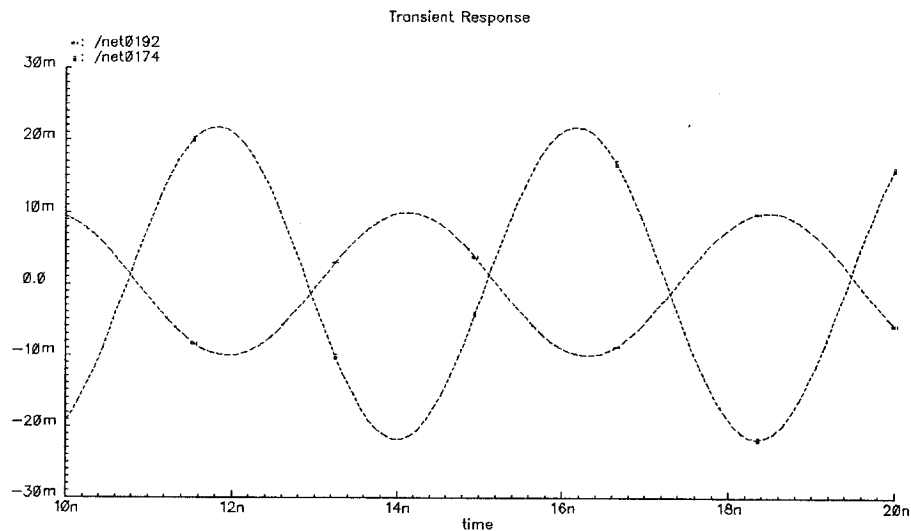


Fig. 7.3 Magnitude frequency response of the simulated filter

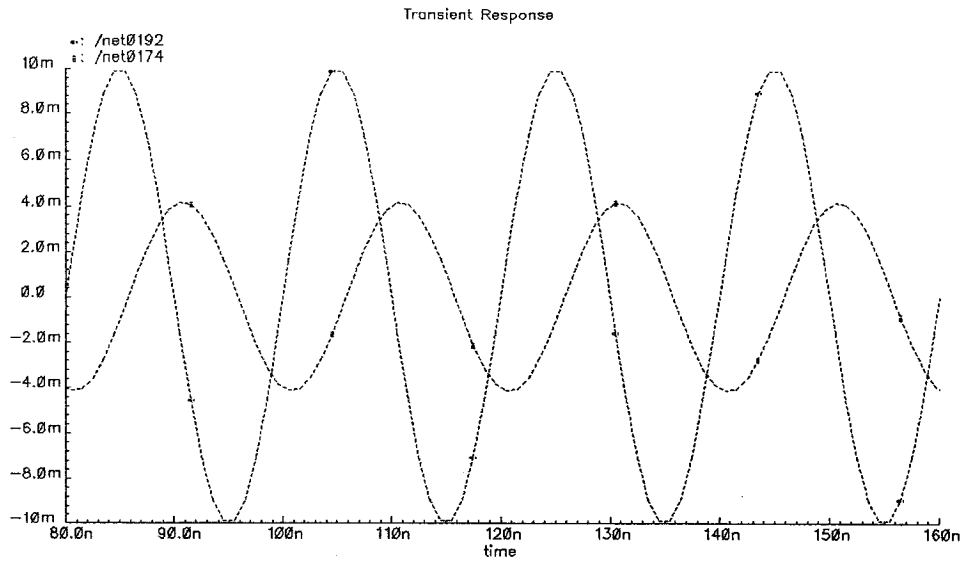
The test bench schematic for transient simulation is similar to that of AC simulation, the only change being the input signal. The input for transient simulation is a 10mV sinusoid signal with frequency of 220 MHz (in band), 50 MHz and 1000 MHz (out of the

band). Note that choosing the sweep time not starting from 0ns is to observe the filter response in the steady state. Graphical plots of the simulation results is given in Fig.7.4 (a), (b) and (c). In these figures, the net0192 curve represents the input signal that is 10mV; the net0174 curve represents the output signals that are 23mV, 4.2mV, and 5.2mV respectively. It can be seen from the curves that the transient characteristics of the output voltage are in line with the AC simulation results.

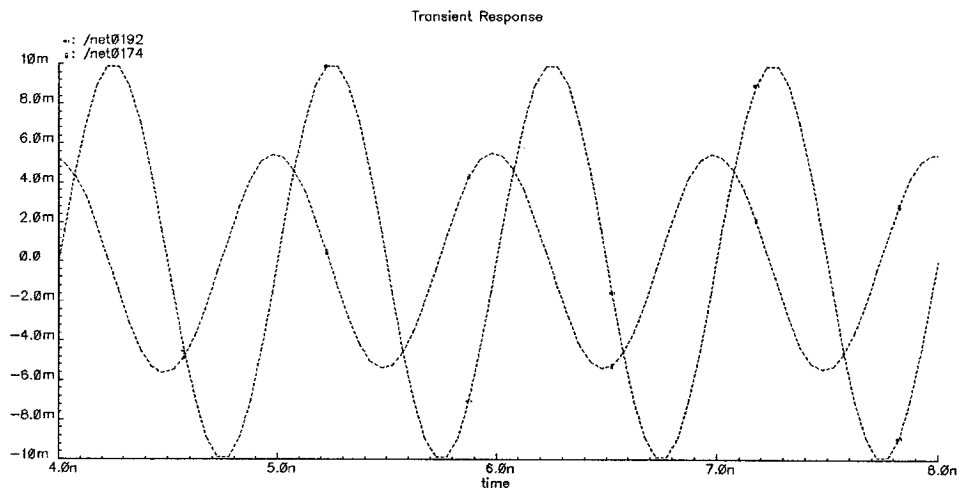
From the DC operating point analysis, the filter core consumes 4mW which is very economical compared with the input and output buffers, each of which consume 9mW of power.



(a)



(b)



(c)

Fig. 7.4 Simulated filter transient response with frequency

(a) 220MHz; (b) 50MHz; (c) 1000MHz.

7.4.2 Harmonic Distortion of the filter

For a real circuit, which is non-linear, the transfer function can always be broken down into a polynomial of the input signal. In voltage-mode case, the output can be modeled as:

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \dots \quad (7.1)$$

Let the input signal be $v_{in} = v \cos \omega t$ (7.2)

Substituting (7.2) into (7.1) yields

$$\begin{aligned} v_{out} &= (a_0 + \frac{1}{2} a_2 v^2) + (a_1 v + \frac{3}{4} a_3 v^3) \cos \omega t + \frac{1}{2} a_2 v^2 \cos 2\omega t + \frac{1}{4} a_3 v^3 \cos 3\omega t + \dots \\ &= b_0 + b_1 \cos \omega t + b_2 \cos 2\omega t + b_3 \cos 3\omega t + \dots \end{aligned} \quad (7.3)$$

where b_0 represents DC level, b_1 is the amplitude of the fundamental and b_i ($i=2,3,4,\dots$) is the amplitude of the i th harmonic.

The linearity of a filter is usually measured in terms of the total harmonic distortion (THD) which is the ratio of the sum of the power of all harmonics to the fundamental itself. So

$$THD = \frac{\sqrt{(b_2^2 + b_3^2 + b_4^2 + \dots)}}{b_1} \quad (7.4)$$

The total harmonic distortions (THD) performance of the filter can be obtained using HSPICE Fourier analysis. The Fourier analysis is to find the DC term and magnitudes and phases of the first nine harmonics of the Fourier Series expansions of the voltages. As a result, THD is given at the end of the netlist file. Note that a transient analysis must be done before SPICE can perform the Fourier series calculations, because it uses the results of the transient analysis in its calculations.

The simulation results show that the THD of the filter reaches 3.1% for a 100mV peak sine wave at 220 MHz frequency.

7.4.3 Intermodulation Distortion of the filter

Previously, harmonic distortion was introduced as the result of non-linearity due to a single sinusoidal input. When two or more sine waves are applied to the input of a two-port network, another non-linearity called inter-modulation (IM) also occurs. To see the effects of both harmonic distortion and inter-modulation, assume that an input signal contains two frequencies ω_1 and ω_2 with the same amplitude, which is

$$v_{in} = v(\cos \omega_1 t + \cos \omega_2 t) \quad (7.5)$$

Substituting (7.5) into (7.1), the linear term is obtained as:

$$a_1 v_{in} = a_1 v(\cos \omega_1 t + \cos \omega_2 t) \quad (7.6)$$

The second term is:

$$a_2 v_{in}^2 = a_2 v^2 (\cos \omega_1 t + \cos \omega_2 t)^2 \quad (7.7)$$

$$= a_2 v^2 \quad \text{zero-frequency constant term}$$

$$+ \frac{a_2 v^2}{2} (\cos 2\omega_1 t + \cos 2\omega_2 t) \quad \text{2nd harmonics}$$

$$+ a_2 v^2 [\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t] \quad \text{second order IM products.}$$

The third order term is:

$$a_3 v_{in}^3 = a_3 v^3 (\cos \omega_1 t + \cos \omega_2 t)^3 \quad (7.8)$$

$$\begin{aligned}
&= \frac{9}{4} a_3 v^3 (\cos \omega_1 t + \cos \omega_2 t) && \text{fundamental} \\
&+ \frac{1}{4} a_3 v^3 (\cos 3\omega_1 t + \cos 3\omega_2 t) && \text{3rd harmonic} \\
&+ \frac{3}{4} a_3 v^3 [\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t] \\
&&& \text{third order IM products}
\end{aligned}$$

Higher order terms can be written in the same fashion.

As shown in equations 7.7 and 7.8, harmonic distortion terms are produced as if each sine wave was applied separately. However, second order intermodulation terms are produced at the frequency of $(\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$; third order intermodulation terms are also produced at the frequency of $(2\omega_1 + \omega_2)$, $(2\omega_1 - \omega_2)$, $(2\omega_2 + \omega_1)$ and $(2\omega_2 - \omega_1)$. Fig.7.5 shows the frequency positions of the distortion terms.

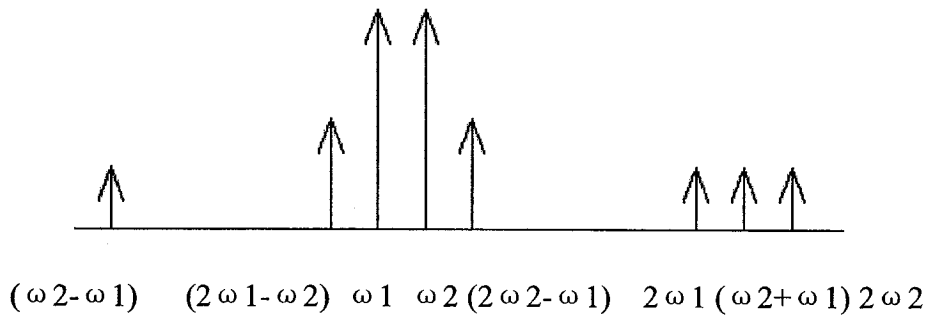


Fig. 7.5 the position of fundamental frequency and distortions.

It can be observed from the above figure, the third order inter-modulation terms $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ are usually of primary interest because they are large and difficult to filter from the desired fundamental signal. One common way to measure the third order inter-modulation distortion in a two-port network is to estimate the third order

intercept point. Since the third order non-linearity is proportional to the input signal cubed, while the fundamental is increasing only linearly with input signal, there will be a point at which the amplitudes of the fundamental and the third inter-modulation product meet. The input signal at this point is defined as the input-referred 3rd order intercept point (IIP3). SPSS analysis in SpectreRF is used to estimate the third order intercept point of the designed filter. Two tones of interference, namely 222 MHz and 224 MHz, of the same amplitude are injected and the 220 MHz inter-modulation product is observed. The IIP3 of the filter is -3.2dBm . The plot of the IIP3 point is shown in Fig. 7.6.

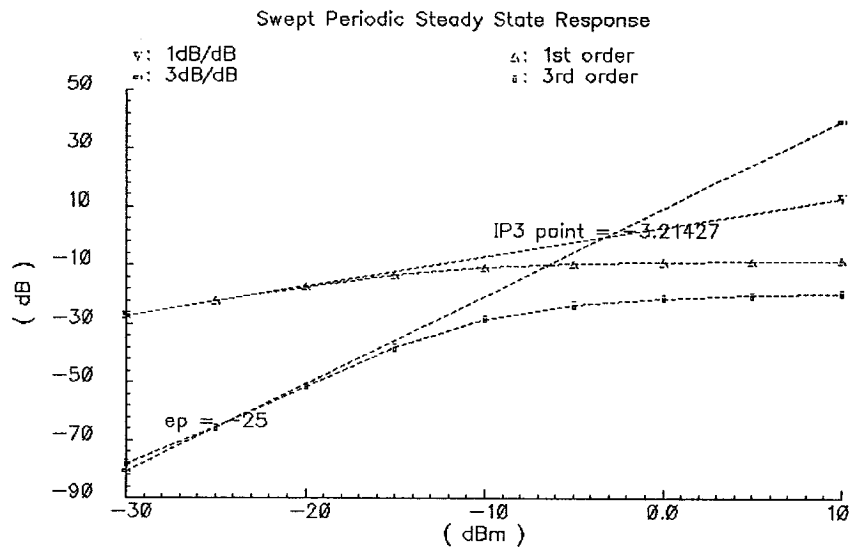


Fig. 7.6 The IIP3 point of the filter

7.4.4 Transient Characteristics of the oscillator

Transient analysis of the oscillator is similar to that of the filter. However, the oscillator requires no stimulus source, as the circuit is self-stimulating, and thus produce an output without an input. The test bench schematic has been shown in Figure 7.2 and the transient response is presented in Fig.7.7. The response looks stable and goes around 4.4 cycles in 20ns. So the frequency of oscillation is $f = \frac{1}{T} = \frac{4.4}{20 \times 10^{-9}} = 220\text{MHz}$.

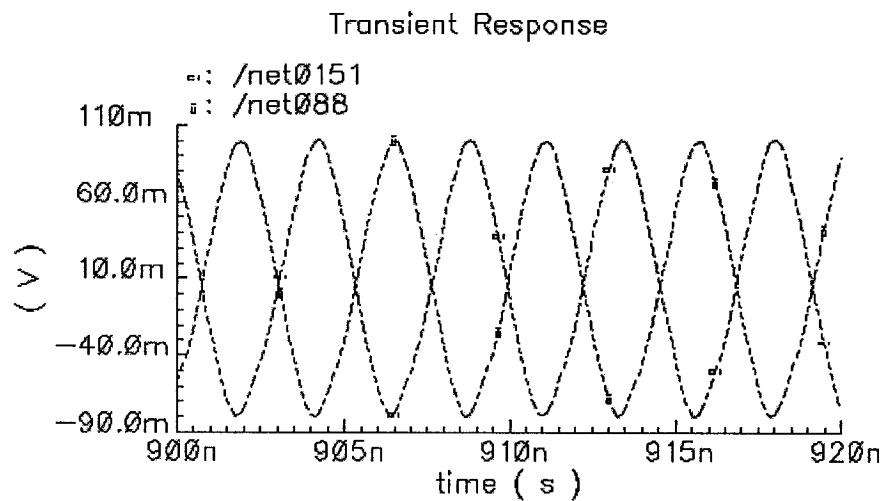


Fig. 7.7 Transient response of the simulated oscillator

7.4.5 Phase noise of the oscillator

A critical specification for any oscillator is its spectral purity, characterized by phase noise. Ideally, the spectrum of an oscillator is an impulse located at a single frequency. However, in any practical oscillator, the spectrum has power distributed around the desired oscillation frequency 220MHz, in addition to power located at harmonic

frequencies. This undesirable power distribution around the desired oscillation frequency is known as phase noise. Pnoise analysis in SpectreRF is used to estimate the phase noise of the oscillator. The result is shown in Fig. 7.8.

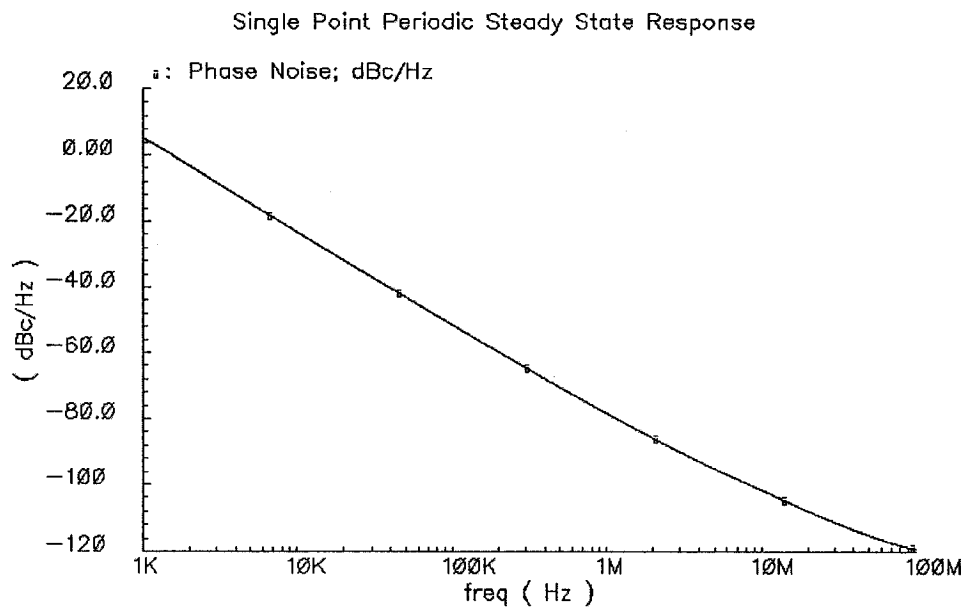


Fig. 7.8 The phase noise of the oscillator

7.5 Measurement results on the oscillator chip

The measurement setup for the fabricated oscillator chip is illustrated in Fig.7.9.

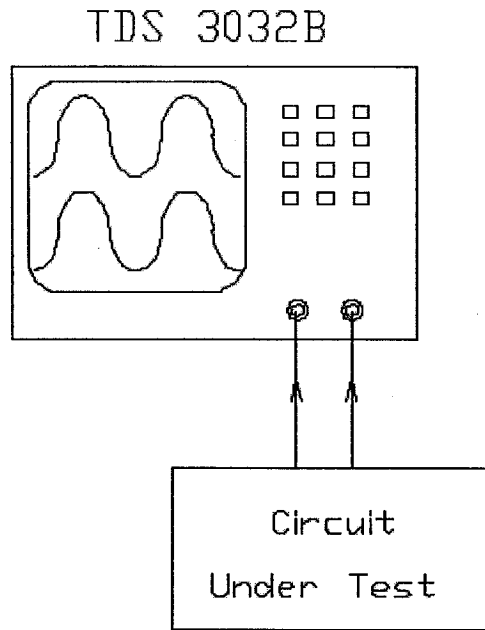


Fig. 7.9 Measurement setup for the oscillator

The differential output signals of the oscillator are directly sent to Channels 1 and 2 of the oscilloscope TDS 3032B for purpose of comparison. The outputs as they appear on the digital oscilloscope are shown in Fig.7.10.

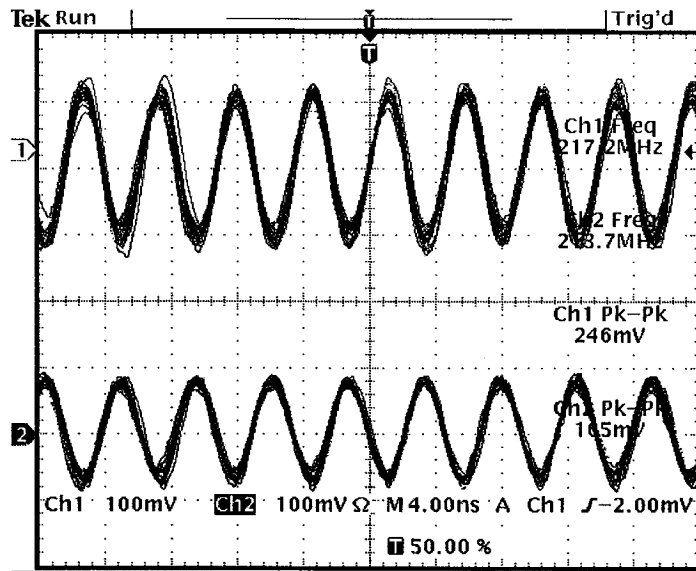


Fig. 7.10 Output signals of the oscillator

It is observed that the oscillation frequency is about 217MHz, which is very close to the design value of 230MHz.

7.6 Summary

This chapter presented some basic parameter definitions about linearity and phase noise. To obtain these parameter values, Hspice and SpecterRF are used in the post-layout simulation for the filter and the oscillator. The experimental setup for testing the fabricated oscillator chip has been provided. The measurement result has a good agreement with the theoretical predictions.

Chapter 8 Conclusions

The design of analog circuit has traditionally been viewed from the point of voltage. Over the last few years, current-mode circuits are becoming more and more popular. One of the primary motivations behind the increased importance of current-mode signal processing is the shrinking feature size of digital CMOS devices, which implies a degradation of their voltage-mode performance for analog circuits because it necessitates a reduction of supply voltages. This problem can be overcome by exclusively operating in the current domain. In addition, using current as the signal variable has significant advantages for the analog designer such as the enhancement in bandwidth and the reduction in circuit complexity. As a vast body of voltage-mode filter structures already exist, a straightforward method of converting these voltage-mode circuits to current-mode circuits would be very useful. With this viewpoint, network transposition, introduced by Bhattacharyya and Swamy as early as in 1971, is reconsidered as an important tool for this kind of mode conversion. As OTA-C filters and oscillators are important building blocks in telecommunication, consumer electronics and instrumentation system, applications of network transposition in the design of OTA-C filters and oscillators are studied. We now summarize the results of the work presented in this thesis and give suggestions for future work.

8.1 Summary

First, a review of current-mode filter realization techniques in the past decade has been given. As illustrated, these realization techniques are often quite complicated and demand a lot of time-consuming mathematic work. In contrast, by simply using the principle of network transposition, current-mode filter structures can be obtained from the associated voltage-mode counterparts. In chapter 3, an intensive investigation on OTA-C filters has shown that the various voltage-mode and current-mode structures proposed in the literatures are transposes of one another. This reflects the feasibility and usefulness of the network transposition. Due to the limitation of technology in 1970s, network transposition did not cover the DIDO structures for various analog building blocks. This is accomplished in chapter 2, and as a consequence, network transposition can be applied in the design of DIDO-OTA-C filters. New current-mode filter structures have been derived from the known voltage-mode structures using the principle of network transposition. Furthermore, network transposition is extended to the design of OTA-C oscillators. As discussed in chapter 4, an oscillator can be viewed as a linear network without an input signal. Transposing the OTA-C oscillator will not change its characteristic equation. Hence, the original as well as its transpose will have the same oscillation condition and oscillation frequency. Also, the various sensitivities with respect to the corresponding parameters will be identical. After this theoretical analysis, new single-output OTA-C oscillator structures have been derived from the known oscillator

structures. In addition, DIDO-OTA-C oscillator structures are also obtained from the corresponding single- output versions by means of the “mirroring” technique.

To verify the theoretical work presented above, several circuits have been implemented either on breadboard or on monolithic silicon. First, an oscillator, a filter and their transposed circuits have been built with discrete resistors, capacitors and OTA device LM13700 and tested in the laboratory. Chapter 5 describes the set up for testing such circuits. The test results are in good agreement with the design values. Chapter 6 focuses on the IC realization of a current-mode DIDO-OTA-C bandpass filter and a DIDO-OTA-C oscillator. Especially, low-voltage IC design techniques have been discussed in detail. For instance, negative conductance is used to cancel the parasitic conductance of OTA; negative feedback is used to reduce the impedance level of the I/O buffers. The post-layout simulation has shown satisfactory results. Finally, the fabricated oscillator chip has been tested. The oscillation frequency is 217MHz, which is very close to the design value of 230Mhz.

8.2 Future Work

In connection with the work presented in this thesis, two areas of further research may be proposed.

At the circuit level, fully differential filters based on multi-input and multi-output OTAs and grounded capacitors is worthy of investigation. Fully differential structure

means that both the input and output signals of the filter are differential. Usually, the OTAs inside the filter have to deal with not only differential input/output signals but also double feedback signals. So multiple-input terminals may be needed by the voltage-mode OTA-C filters. Similarly, a current-mode filter may need multiple-output terminals to send output and feedback signals. In general, using multi-input and multi-output OTA in filter design can lead to simpler structure. To apply network transposition in the design of this kind of circuit, the transpose operation of the multi-input and multi-output OTA need to be first studied.

At the building block level, tuning circuitry is needed to adjust the transconductance and negative conductance so that the overall filter/oscillator performances remain stable, when fabrication tolerances are encountered and the center frequency is to be changed according to the practical applications. Usually, fine tuning of OTA is achieved by changing the tail current of its differential pairs. However, this method is not feasible for the two-stack OTA structure because there is no tail current source in this OTA. Some papers have suggested adjusting the power supply voltage or changing the input common mode voltage to deal with the tuning of such a structure, but in most practical circumstances, OTAs share the power supply rails with other devices on the same board. Changing the power supply or the common mode level probably will affect the function of the other devices. Even if this change is allowable, it will pull the transistors away from the optimal DC working point, as in the case of conventional tuning based on adjusting the tail current source. As a result, some specifications of the OTA such as the

dynamic range and linearity will be degraded dramatically. Hence, the transconductance tuning of this kind of an OTA remains a challenge.

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