ON THE DESIGN AND SYNTHESIS OF DIFFERENTIAL CLOCK DISTRIBUTION NETWORK

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ABSTRACT

On The Design and Synthesis of Differential Clock Distribution Network

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This research work focuses mainly on the design and synthesis of Differential Clock Distribution Networks (DCDNs). The Clock Distribution Network (CDN) plays an important role in synchronous systems. The network is spread all over the chip to synchronize its sub-systems. The system performance is influenced by the performance of its clock network. As technology advances and the complexity increases, a drastic growth in the chip complexity in the near future is expected. Thus designing a reliable CDN is becoming a must, and therefore all the design efforts should be utilized to efficiently design clock distribution networks.

Of importance in chip design are low power and low noise concepts. Differential signaling scheme offers high noise immunity and since it is associated with signal amplitudes lower than the usual, it may contribute to reduce power consumption as well. Due to these potentials, the design and analysis of DCDN has been the focus of this research work.

First, a line equivalent delay model based on the decoupling method is proposed to be able to route DCDNs with minimum skew. This part refers to the routing and synthesis of DCDNS. Later, new configurations for differential buffers based on body-biased transistors are proposed, which show better performance for future low voltage applications.

Finally, a circuit and system design method that reduces the power consumption of DCDNs is proposed. This is accomplished in two steps: First circuit configurations that reduce the differential voltage swing giving less power consumption are introduced. Later, by reducing the supply voltage, a DCDN is designed which has the same power consumption as single-node CDNs, but has less skew variation in the presence of external noises such as power supply fluctuations.

ACKNOWLEDGMENT

It was not doable for me to accomplish my Master's without the significant support from my mentors, family, colleagues. First and foremost, I would like to thank and appreciate Professor A.J.Al-Khalili, my principle advisor. His understanding and endless support was the main key and the best motivation toward my progress and achievements. He supported me mentally and financially and supported me like his son. It is not easy to express my experience and feeling in a few words but I could reveal that he is one of the few angels beside my parents that I owe my current and future achievements.

Secondly, I would like to thank Professor Yvon Savaria, my co-supervisor, for his valuable guidance and advice on this project. His insights into microelectronics along with his parental and supporting attitude made a perfect advisor for me and I am honored to be supervised by this distinguished professor.

Thirdly, I would like to thank Dr. Haydar Saaied who made the best efforts to help me find my research path. He was deeply and fully involved with my guidance. It is because of his fundamental and solid advices that I was able to accomplish these contributions.

Finally, I wish to offer my sincere gratitude to my family, who supported me mentally, spiritually and financially. I owe them all my life and I wish I have been and I will be able to make them happy of myself.

DEDICATION

I dedicate this work to:

My Mother who is the source of love and is my best motivation,

My Father who sacrifices himself for his family,

My Sister and my nephews, for whom my being far is the hardest,

My grandmothers whose great memories are all remained for me and

The heroes who protected our borders at the price of losing their health, lives and families….

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1. Introduction

1.1 Clock Network Design and Challenges

Clock Distribution Networks (CDNs) play an important role in today's high performance synchronous systems. With technology scaling, the issue of designing high performance and robust clock distribution networks has become a significant issue in Deep Sub Micron (DSM) era. Clock network design depends on several design issues. Interconnect delay results in performance degradation. Parasitic elements such as parasitic capacitances threaten signal integrity and act as sink of power consumption. System complexity may be the cause of timing errors and system malfunctioning.

In Deep Submicron Very Large Scale integration circuits, the delay of interconnect dominates gate delay as shown in Figure 1-1 [1-3]. As technology scales down, the delay of interconnect increases. Table 1-1 demonstrates the effect of technology scaling on the delay of the interconnect [4]. The delay of Global interconnect increases by the factor of $S^2S^2_c$ in which S is the feature size scaling factor and S_c is the scaling factor for the die area whereas the delay of local interconnects relatively remains the same. The delay of global interconnects can be reduced significantly by introducing different techniques such as introduction of buffers, as it can be seen in the Figure 1-1.

The clock network design is associated with the aforementioned issues. The clock is distributed all over the chip with minimum possible skew or variation. The clock should operate at its maximum frequency in order to increase the performance of the system. Designing a high performance clock distribution network is affected by technology advances. With the introduction of Systems-on-a-Chip (SOC), which is the integration of various modules on a single die, due to the complexity increase of the design, noise has

become an important design factor which threatens the signal integrity and system performance. International Technology Roadmap for Semiconductors has predicted that the number of transistors on a single chip will exceed one billion, by the end of the decade (2010) [3]. Thus *noise immunity* due to complexity of the design, high density of the devices, power supply and similar issues have become major concerns. Moreover a clock network consumes a significant fraction of the total power of the chip during operation. Fractions as high as 20%-50% have been reported [5]. This is partly due to the high switching activity. *Minimizing the power consumed* by the clock network will significantly affect the power efficiency of the total system. Thus designing noise tolerant, yet energy efficient and high performance clock distribution network (CDN) is a design objective for future synchronous IC designs.

Table 1-1, Interconnect parameters scaling with technology advances. Last line denotes the quadratic increase in the delay of interconnect with technology scaling

Parameters	Scaling Factor
Cross sectional dimensions	1/S
Resistance per unit length	S^2
Capacitance per unit length	1
RC constant unit length	S^2
Local interconnection length	1/S
Local interconnection RC delay	1
Die size	S_C
Global interconnection length	S_C
Local interconnection resistance	$S^2 S_C$
Local interconnection RC delay	$S^2 S_C^2$

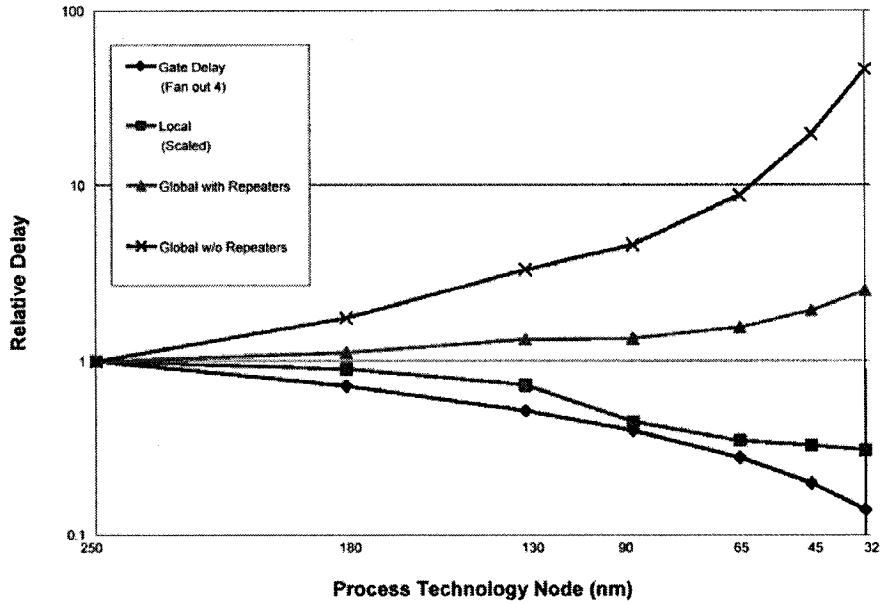

Figure 1-1, Global interconnect delay increases significantly with technology scaling [3].

Having discussed the various important issues of CDN design and the fact that designing high performance CDNs in Deep-Sub-Micron (DSM) era is a critical design objective, a design methodology is proposed to achieve these goals.

Differential signaling has shown great advantages in terms of noise tolerance over single mode signaling scheme [1, 6]. Differential signaling rejects common-mode noises and can be distributed with lower voltage swings which are widely referred to in the literature as Low Voltage Differential Signaling (LVDS) especially in off-chip applications. Switching noise in power supplies results in variations in the system performance. This issue directly affects the system functionality and may cause system errors. In differential signaling, the voltage difference of the two differential signal pair is the resulting signal, thus any common-mode noise applied to the differential signals is eliminated at the time of evaluation. This benefit comes at the price of doubling the routing area and circuit complexity, leading to higher power consumption of the differential signaling.

System *parametric variations* have become a concern with the presence of current complex systems and the need for high speed applications. Any variation in the system components could result in error in the functionality of the system. Timing variations is one kind of system variations which may affect the system performance. Variations can be static or dynamic. Static variations are often due to fabrication processes and they are usually referred to as *Process Induced Variations*. Any process induced variations results in heterogeneous devices which may function differently compared to each other. This will cause the different parts of the system to function in a different manner in terms of functionality, timing issues, noise immunity or other factors. Dynamic variations are also referred to as *Dynamic Noise*. This phenomenon is generally due to external perturbations affecting the system during its operation. Crosstalk and power supply variations are two recognized sources of dynamic perturbations.

1.2 Thesis Motivations

The objective of this research project is to design and develop reliable clock distribution networks with low timing variations for synchronous systems. Due to the expected benefits of differential signaling in terms of high noise immunity, the design and synthesis of Differential Clock Distribution Networks (DCDN) is analyzed and investigated in this research project.

1.3 Thesis Contributions

In this dissertation several new ideas/contributions have been proposed:

1. A line equivalent delay model is proposed for zero skew routing of the differential clock trees.

2. New configurations of differential buffers based on Dynamic Threshold transistors are proposed and it is shown that in sub 1-V supply voltages, they outperform the

conventional buffers with 25% delay reduction.

3. New differential buffers are proposed by which it is possible to further reduce differential voltage swings as compared to available methods. This leads to further energy savings in the DCDN.

4. Using simultaneous supply voltage scaling and the proposed circuit techniques (differential voltage swing scaling), a clock network has been designed that has the same power consumption as the conventional single-node CDNs but has higher tolerance against external perturbations (has higher robustness and less variations).

1.4 Organization of the Dissertation

In this dissertation, the application of differential signaling in clock distribution networks is investigated and the feasibility of its application in terms of signal integrity and power consumption of the clock networks is evaluated. The dissertation is organized as follows:

Chapter 2 describes the background of the work. Different aspects of interconnect parameters such as resistance, capacitance and inductance are studied. Later, the background of clock distribution networks and its figures of merit are reviewed, and finally, the methods of clock synthesis are presented.

In chapter 3 the concepts of differential signaling is introduced. Further its application to clock distribution is discussed and problems associated with differential clock distribution networks are presented.

In chapter 4 the delay model and the methodology for zero skew routing of differential clock network is presented. Later, the proposed differential buffers based on dynamic threshold transistors are given. In the last section of this chapter, the proposed circuit and system techniques for energy efficient differential clock distribution are presented.

Chapter 5 concludes the thesis with a summary of the contributions and recommendations for future work. Finally references and appendix contents to support our work are given at the end of the dissertation.

2. Background

In this chapter the background of the work is presented. The study begins with the introduction of interconnects and its components known as interconnect resistance, capacitance and inductance. Later the preliminaries of Clock Distribution Network and its figures of merit are discussed. Finally, same relevant methods for clock network synthesis are summarized.

2.1 Interconnect

Interconnect along with the circuit is one out of two main important components in VLSI systems. In the past, due to the simple features of the systems and low frequency of system operation, interconnects were considered and modeled as simple wires without any parasitics. With technology and design advances, interconnect could no longer be considered as simple wire model. Technology advances have resulted in scaling of the device sizes. Due to shrinking of spaces between devices and interconnects, in combination with the increase of the complexity of the design, parasitic effects have become non negligible issues in the design and modeling of VLSI systems.

Chronologically, technology advance has influenced interconnects in the following manner: after considering parasitic, interconnects were modeled as a lump capacitance. This was the well known plate capacitance model due to the structure of the wire. With the continuation in scaling, the wire cross sectional area decreased, while at the same time wire length increased due to increase of the die area, resulting in a non-negligible wire resistance. This resulted in the development of the RC delay model, first as a lumped RC circuit and later as distributed RC model to improve accuracy.

2.1.1 Interconnect components

Reviewing the various methods of interconnect modeling, the three main components of any interconnects are the interconnect resistance, capacitance and inductance.

- **Interconnect Resistance**

All wires have a finite conductance or resistance. This implies the ability of the wire to carry a charge flow or the ability to resist the charge flow. The resistance of the wire is proportional to its length L and inversely proportional to its cross sectional A. The resistance of a rectangular conductor can be expressed as:

$$R = \rho \frac{L}{A} = \frac{\rho L}{HW} \tag{2.1}$$

where the constant ρ is the resistively of the material in Ω-m. In very high frequencies, conductive materials face a phenomenon which is called the *skin effect*. With the existence of this phenomenon, the resistance becomes frequency dependent. High frequency currents tend to flow primarily on the surface of the conductor with the current density falling off exponentially with depth into the conductor. The *skin depth* δ is defined as the depth at which the current falls off to a value of e^{-1} of its nominal value and is given by [1]:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{2.2}$$

where f is the frequency of the signal and μ is the permeability of the surrounding dielectric (typically permeability of the free space or $4\pi * 10^{-7}$ H/m). Figure 2-1 illustrates the impact of skin effect at high frequencies.

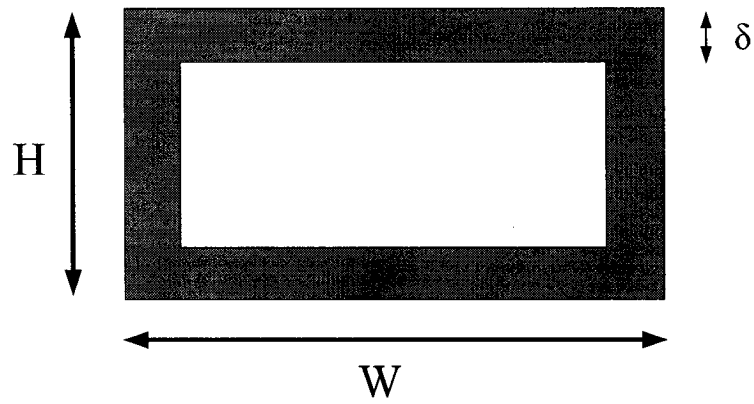

Figure 2-1, Skin effect phenomenon

Although the skin effect is of concern in high speed design especially in electromagnetic field engineering, in this work in order to simplify the design this effect is neglected in modeling of interconnects.

- **Interconnect Capacitance**

Modeling interconnect capacitance is no longer a simple task. Initially interconnect capacitance were modeled as a simple parallel plate capacitance, however the capacitance of such a wire is a function of its shape and surrounding environment as well as of its distances to the substrate and surrounding metal layers. The interconnection capacitance is mainly composed of three components:

a. Parallel plate capacitance (C_a)

b. Fringing capacitance (C_F)

c. Inter-wire coupling capacitance (C_C)

Modeling of a single wire capacitance should include the fringing components. Due to the mass integration of the systems and increase in the density in SOCs, this component

is no longer negligible. In recent designs, interconnection capacitance is modeled as in Figure 2-2:

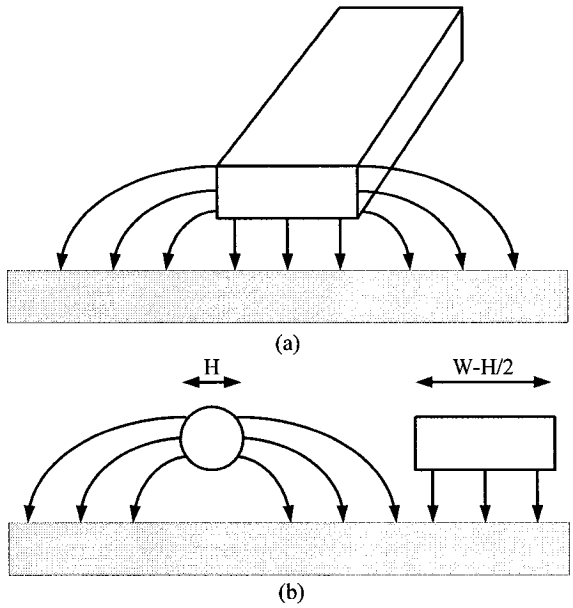

Figure 2-2, (a) Typical interconnection capacitances and (b) its modeling components

As shown, the interconnection capacitances have two main components: the parallel plate and the fringing capacitances. The following equation describes the capacitances numerically according to [1]:

$$C_{wire} = C_{plate} + C_{Fring} = \frac{(W - H/2)\varepsilon_{dielectric}}{t_{dielectric}} + \frac{2\pi\varepsilon_{dielectric}}{\log(t_{dielectric}/H)} \quad (2.3)$$

In Equation 2.3, W is the width and H is the diameter of the relative cylindrical conductor. With technology advances and device scaling, the fringing part becomes the dominant component. The fringing component which is usually referred to as sidewall capacitances is increasing compared to intrinsic parallel plate capacitances. One kind of sidewall capacitance is known as the coupling capacitances or inter-wire capacitances

of various conductors. Figure 2-3 shows that in DSM regime, in sub 100nm technologies, coupling capacitances becomes 80% of the total interconnection capacitances or in other words, it becomes four times greater than the intrinsic parallel plate capacitances [7].

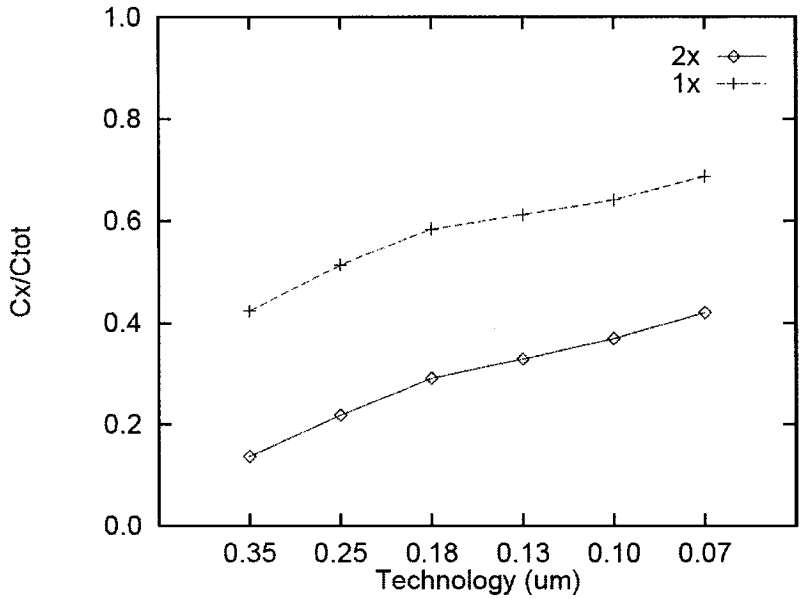

Figure 2-3, Coupling capacitance becomes the dominant component in advanced technologies (X represents the spacing between two adjacent wires)

- **Interconnect Inductance**

Interconnects also have inductance, representing inertia against changing current through the wire. Unlike resistance or capacitance, inductance has no first-order closed-form models. In the literature, the inductance is introduced as that of a loop, and a changing magnetic flux through that loop induces a voltage in it as:

$$\Delta V = L\frac{di}{dt} \tag{2.4}$$

Due to the growing importance of inductance especially with the introduction of low resistance material, recently researchers have been trying to find a closed form model

for interconnect inductance. Moreover researches which have focused on the interconnect inductance have shown that faster on-chip signal rise time, higher clock frequencies and use of copper wires for interconnects all have necessitated the use of RLC models in modeling interconnects. Ismail [8] showed the importance of considering inductance in DSM regime and demonstrated a wide range of errors neglecting inductance especially in the cases where there were small amount of resistance. They showed that on-chip inductance can be used to improve the performance of high-speed integrated circuits. Specifically, inductance improves the signal slew rate, virtually eliminates short-circuit power consumption and reduces the area of the active devices and repeaters inserted to optimize the performance of long interconnects.

2.1.2 Interconnect modeling

In previous section we introduced the electrical components of interconnects. These parasitic elements impact the electrical behavior of the circuit and influence its delay, power and reliability. To study these effects it is required to model these parameters to estimate the real behavior of interconnects/wires. The categories of these models vary from simple to complex models depending on the accuracy of the model. Here we have a brief overview on the various interconnect models.

- **The ideal Wire**

In schematics, wires are simple lines without any parasitic attached to them. This model does not have any impact on the system performance or behavior. This model is usually over-simplified and it does not show realistic behavior of the system unless the system frequency is low enough to neglect the loss of signal integrity.

- **The Lumped Model**

Interconnect parasitic elements are distributed along the interconnection lines. Yet, when only one single element is important or dominant along the line, this model can be

effective. The advantage of this model is that the effective parasitic is described by ordinary differential equations whereas for the case of more complex models, the equation becomes partial differential equation. As long as the resistance of the wires is small and the operation frequency is low, it is meaningful to lump the distributed capacitive elements of the line to a single *lumped capacitive model*. This simple, yet effective model is the *most common model* used in modeling interconnection in digital systems.

- **Lumped RC Model**

When the length of the interconnection is sufficient to have a considerable resistance, lumped capacitive model is no longer accurate. The most straight forward way to model the line is to lump the distributed resistance of the line into a single resistance attached to a lumped capacitance which is called *Lumped RC model*. This model is still simple and is pessimistic and inaccurate for long interconnections.

- **The Distributed rc Line**

In reality the parasitic elements of interconnects such as resistance, capacitance and inductance are spread throughout the wire. For accurate estimation of the behavior of the line it is needed to write the partial differential equations for the parasitic elements in order to have a precise model of the line. The disadvantage associated with distributed model is the complexity of the computation. Yet, these models show more accuracy compared to the lumped model of interconnects. Table 2-1 demonstrates the propagation delay for step responses relevant to each interconnect model in which R and C are the total resistance and capacitance of the interconnect network.

Table 2-1, Step response of Lumped and Distributed RC networks

Voltage Range	Lumped RC Network	Distributed rc Network
0 -> 50%	0.69 RC	0.38 RC
0 -> 63% (τ)	RC	0.5 RC
10%->90% (t_r)	2.2 RC	0.9 RC

- **Simulation Line Models**

For simulations, it will not be practical to utilize the distributed RC models as a line containing uncountable number of lumped RC sections. Sakurai in [2] showed the following configuration can model the distributed lines with maximum accuracy. These models are known as π or T models such as $\pi 3$ or T3. $\Pi 3$ shows more than 97% accuracy.

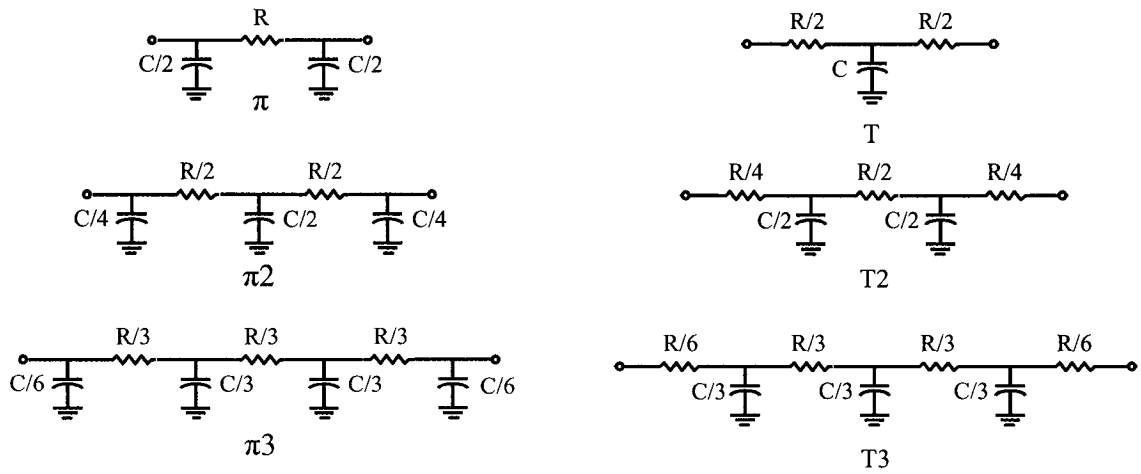

Figure 2-4, Simulation Models for Interconnect Based on distributed RC Model

2.1.3 Introducing Repeaters

Repeater insertion has been widely used to improve the propagation delay of interconnects. Many efforts have been invested to investigate the influence of applying buffers to interconnect for performance improvement. Bakoglu in [4] introduces the concept of optimal buffer insertion in interconnects to minimize the propagation delay of the line. [4] models interconnects as infinite number of lumped RC elements namely as Distributed RC model which has the following propagation delay formula:

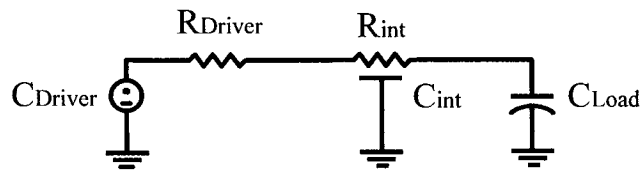

Figure 2-5, distributed model of interconnect considering driver and capacitive termination

$$T_{50\%} = 0.4R_{\text{int}}C_{\text{int}} + 0.7(R_{tr}C_{\text{int}} + R_{tr}C_L + R_{\text{int}}C_L) \tag{2.5}$$

In the above, $R_{\text{int}}, C_{\text{int}}, R_{tr}, C_L$ are interconnect resistance and capacitance & driver resistance and capacitance respectively. For the driver a first order approximation of R_{tr} is defined as [4]:

$$R_{tr} \approx \frac{L/W}{\mu C_{gox}(V_{dd} - V_T)} \tag{2.6}$$

Where $L, W, \mu, C_{gox}, V_T, V_{dd}$ are the device parameters known respectively as channel length and width, mobility, gate-oxide capacitance, threshold voltage and finally supply voltage. More accurate value can be obtained by:

$$R_{tr} = \int_{V1}^{V2} \frac{dV}{I} \tag{2.7}$$

where V1 and V2 are the end points of the region where transistor resistance is being averaged over, and I is the function of V. For example to calculate the pull down resistance of NMOS in $T_{50\%}$, $V_1=V_{dd}$ and $V_2=V_{dd}/2$.

In the case of buffer insertion, assume the optimum number of buffers to be inserted in interconnect to minimize interconnect delay $T_{50\%}$ is considered as k uniform repeaters as in Figure 2-6. These buffers are uniformly sized and are h times greater than a minimum size buffer. The buffer output impedance R_{tr} is R_0/h and the input capacitance of the buffer C_L is hC_0 where R_0 and C_0 are output impedance and input capacitance of minimum sized buffer.

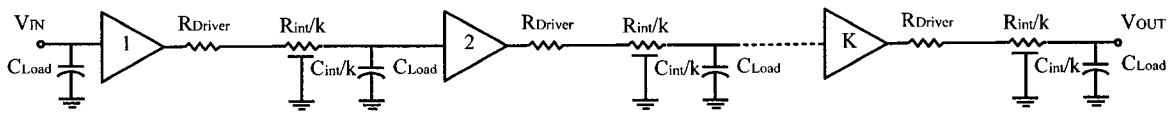

Figure 2-6, Interconnect with repeaters

The total propagation delay of the repeater system is the sum of the individual propagation delays of the k sections and is a function of h and k for a given interconnect line. Recall that each section of the line has interconnected parameters equal to $R_t/k, C_t/k, L_t/k$. The value of h and k that gives the minimum delay time $T_{50\%}$ can be obtained by simultaneously solving the following two differential equations which are needed to achieve total minimum delay $t_{pdtotal}$:

$$\frac{\partial t_{pdtotal}(h,k)}{\partial h} = 0 \qquad \frac{\partial t_{pdtotal}(h,k)}{\partial k} = 0$$

$$T_{50\%} = k\left[0.7R_{tr}\left(\frac{C_{\text{int}}}{k} + C_L\right) + \frac{R_{\text{int}}}{k}\left(\frac{0.4C_{\text{int}}}{k} + 0.7C_L\right)\right] \tag{2.8}$$

This will result in:

$$h_{opt}(RC) = \sqrt{\frac{R_0 C_t}{R_t C_0}} \tag{2.9}$$

$$k_{opt}(RC) = \sqrt{\frac{0.4R_t C_t}{0.7R_0 C_0}} \tag{2.10}$$

Equations 2.9 & 2.10 give the optimal number (k_{opt}) and optimal size (h_{opt}) of the uniform buffers to drive interconnect with minimum delay.

2.2 Clock Distribution Network

Almost all high performance VLSI systems today are synchronous. These systems use a signal to control the flow of data throughout the chip. This signal is called *clock*. This greatly facilitates the design process of the system because it provides a global framework that allows many different components to operate simultaneously while sharing data. The only price for using synchronous type of system is the additional overhead required to generate and distribute the clock signal in the design process.

Nearly all on-chip clock distributions contain a series of buffers and interconnects that power-up the clock signal from the clock source to the clock sinks. In the past, clock distributions consisted of only a single buffer stage driving wires to the clock loads [9]. This is still the case for clock distribution in smaller scale ASICs, but most contemporary complex systems use multiple buffer stages that each drives smaller portions of the clock load (hierarchical clock networks). This approach outperforms the former method; it improves the performance of the clock network as will be discussed later. A typical

clock distribution for a high-performance VLSI system is shown in Figure 2-7. The design is based on the reported clock distribution networks in [10-12].

The clock signal is generated with a PLL. The core clock signal is then amplified through the global buffer and distributed through a hierarchical network of the system and buffers. The system clock distribution is generally defined to span from the PLL to the clock "pins". The pin is the input to a buffer that locally amplifies and distributes the clock signal to clocked storage elements within a macro, the small blocks that make up a system. There can be any number of buffer levels between the PLL and the clock pin. For a typical high-performance VLSI system, there are at least two and up to four buffer levels. The last buffer level before the clock pin is generally called a sector buffer. This stage drives the interconnect leading to the macros and the local buffers at the pins. Although the structure of the clock distribution in Figure 2-7 is uniform, the non-uniform loading of the various macros requires careful tuning of the delays through the various paths. The design issues associated with the different levels of the clock distribution are described in the hierarchical clock network section.

2.2.1 Clock Network Hierarchy

A synchronous system even with a medium complexity has thousands of loads to be driven by the clock signal. In clock distribution networks, closely placed loads are grouped together and form a sub-block. These sub-blocks also follow the same process and form blocks. This trend gives the methodology to give a hierarchy to the clock distribution design resulting in three different levels/categories of clock distribution namely as *global, regional* and *local* clock networks as in Figure 2-7. Usually at each level of hierarchy there are buffers associated with the level to regenerate the clock signal. The reason of each level is to improve the distribution of the clock signal at that level. This fact facilitates the design process when complexity of the system increases. In what follows we review the aspects associated with each level.

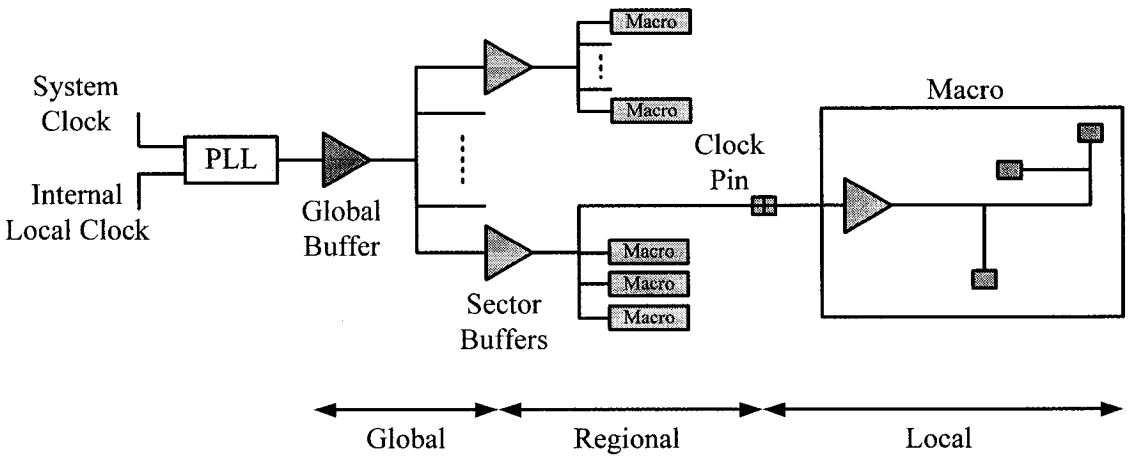

Figure 2-7, Typical hierarchical clock distribution network for a high performance synchronous VLSI system

- **Global**

The global clock distribution connects the global clock buffer to the inputs of the sector buffers. This level of the distribution is usually the *longest path* in clock network because it relays the clock signal from some central point on the die to the sector buffers located throughout the die. The issues in designing the global tree is mostly related to *signal integrity* issues which is meant to maintain a fast edge rate over long wires while not introducing a large amount of timing uncertainty. Skew and jitter accumulate as the clock signal propagates through the clock network and both tend to accumulate proportional to the latency of the path. **Because most of the latency occurs in the global clock distribution, this is also a primary source of skew and jitter [13].** On the other hand, the global network drives a small amount of the total capacitance in the clock network because it is at the upper portion of the fan-out of clock network. Therefore, relatively **little power is dissipated** at this level of the distribution compared to the other levels. **From a design point of view, achieving low timing uncertainty is more critical than reducing power dissipation at this level.**

- **Regional**

The regional clock level is defined to be the distribution of clock signals from the sector buffers to the clock pins. As clock frequency increases, the sector buffers which deal with regional level tend to be pushed lower into the clock hierarchy to reduce dispersion of the clock signal and achieve faster edge rates at the clock pins [14]. The regional clock network is sometimes categorized and considered as part of the global clock distribution, yet in order to show how different topologies are used at different levels, it may be separated into its own level. This level is the *middle ground* between global and local clock distribution; it does not span as much area as the global level and it does not drive as much load or consume nearly as much power as the local level. Although the regional level spans less area than the global level, it can still **contribute a significant amount of skew and jitter to the clock signal.**

- **Local**

The final level of a clock distribution network is the local level, which is the part of the clock network that follows the clock pin to the load of the system to be synchronized. This network drives the final loads of the clock distribution and hence **consumes the most power.** As a design rule, the power at the local level is about one order of magnitude larger than the power in the global and regional levels combined, with the only notable exceptions being clock networks that use a low-impedance grid at the regional level [13]. The layout of the local grid is generally included in the design of the macro block and is not related to the global and regional clock network parts. Due to the relatively limited span, it is sufficient to use automatic layout for this portion of the clock network. Because macros are irregular in nature, the layout is generally a nonsymmetrical tree which may be length-matched by introducing routing algorithms (such as DME) depending on the skew goals for the distribution.

2.2.2 Figures of Merit of a Clock Distribution Network

The figures of merit for a clock distribution are known as timing uncertainty and power consumption. Both of these performance metrics have a significant impact on the design, evaluation and verification of synchronous systems performance and reliability. In this section, the concept of timing uncertainty and its components are discussed and a model for power consumption is given and analyzed.

- **Timing Uncertainty**

As mentioned previously, the advantage of a synchronous system is to regulate the flow of data throughout the system. However, this synchronizing approach depends on the ability to accurately relay a clock signal to millions of individual clocked loads. Any timing error introduced by the clock distribution has the potential of causing a functional error leading to system malfunctioning. Therefore, the timing uncertainty of the clock signal must be estimated and taken into account in the first design stages. The two categories of timing uncertainties in a clock distribution are skew and jitter which are described below:

- **Skew**

Clock skew refers to the absolute time difference in clock signal arrival between two points in the clock network (Figure 2-7). An example of clock skew is shown in Figure 2-8 where the clock signal at n1 precedes the clock signal at n2 by t_{skew}. Clock skew is generally caused by mismatches in either device or interconnect within the clock distribution or by temperature or voltage variations around the die. Although skew generally refers to the timing difference between any two points on a die, a more important metric for current and future synchronous system is the components of clock skew [13].

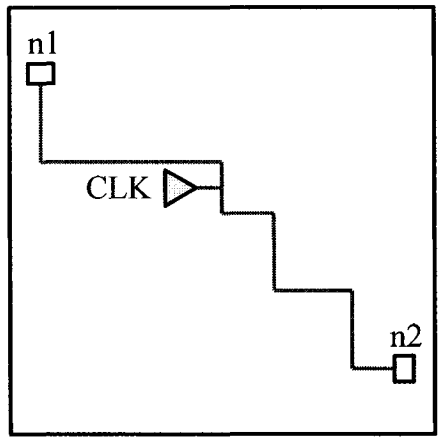

Figure 2-8, A portion of a clock tree including a clock source and two nodes

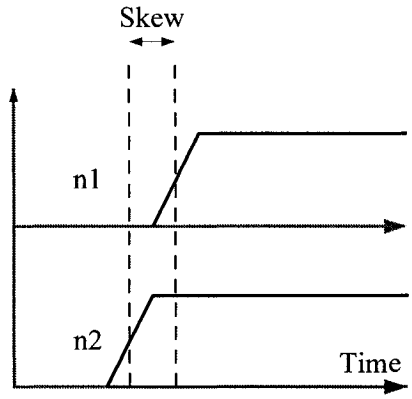

Figure 2-9, An example of skew between two nodes of clock tree

There are two components to the clock skew: the skew caused due to the static noise (such as imbalanced routing) that is *deterministic* and the one caused by the system device and environmental variations that is *random*. An ideal clock distribution would have zero skew, although in practice it is sometimes beneficial to intentionally skew the clock to speed-up specific paths in the design. Many works have been focused on the design of zero skew (low skew) deterministic clock network however there **is still lack of work to minimize the random (nondeterministic) aspect of the clock skew.**

- **Jitter**

Jitter is another source of dynamic timing uncertainties at a single clock load, as drawn in Figure 2-10. The key measure of jitter for a synchronous system is the period or cycle-to-cycle jitter, which is the difference between the nominal cycle time $T_{clk'}$, and the actual cycle time T_{clk}. In Figure 2-10, the first cycle, is the same as clock signal period and the second cycle, the clock period is longer by T_{jitter}. The total clock jitter is the sum of the jitter from the clock source and from the clock distribution. Power supply noise causes jitter in both the clock source and the distribution [15].

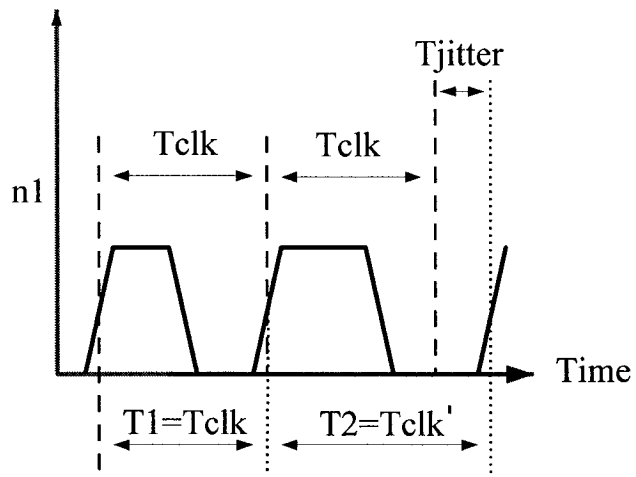

Figure 2-10, An example of jitter for a node of clock network

In the past, jitter was mainly due to the clock source which generally is an on-chip phase-locked loop (PLL) that multiplies up an off-chip clock reference to the core clock frequency. However, PLL jitter has scaled well with technology while the jitter in the clock distribution has not. As a result, the dominant source of clock jitter for today's high performing systems is the clock distribution [13].

- **Power**

The clock network should provide certain characteristics including a fast clock signal edges, low skew and variations associated with the clock signal. Clock network involves long interconnects which implies having lots of parasitic associated with the network. These contribute to the power consumption of the clock signal. Having the highest switching activity of the circuit in a chip is another fact of consuming a large amount of power of the system. This power consumption can be as high as 50% of the total power consumption of the chip according to [5]. The growing need for low power electronics has necessitated increasing effort to reduce the power of the clock network eventually.

The total power consumption of the clock network consists of three components:

- Static power dissipation
- Dynamic power dissipation
- Leakage power dissipation

The power consumption due to the leakage current is relatively a small component in the clock network. In the same way, keeping the proper rise/fall times minimizes the static power consumption. Thus the main portion of the power consumption is due to the dynamic power consumption. This is estimated as:

$$P = f \cdot C_L \cdot V_{DD} \cdot V_{swing} \tag{2.11}$$

where f, C_L, V_{DD} and V_{swing} are frequency of the clock network, total load capacitances, supply voltage and voltage swing of clock signal respectively. For the case of full swing (in which the clock signal swing reaches the supply level) the power consumption becomes:

$$P = f \cdot C_L \cdot V_{DD}^{\ 2} \tag{2.12}$$

As 2.11 and 2.12 imply some possible methods to reduce the power consumption are to:

a. Reduce total load capacitances (C_L)

b. Reduce voltage Supply (V_{DD}) which leads to the quadratic reduction of the power consumption. Note that for the case of reduced swing signaling clock signal swing should be scaled with the same factor for quadratic reduction of the power consumption.

c. Reduce clock signal swing (V_{swing}) which results in the linear power reduction of the clock network.

For the first approach there are some points of interest. First is that the intrinsic load capacitance relies in the process technology and there is no handy way to improve it. Yet, from the design aspects by breaking down interconnects by repeater insertion the total interconnect load is reduced. Worth mentioning is that in coupled lines the total load is greater than that of single node lines thus compensating design methods should be taken into consideration for power saving improvement. In this work because of the huge increase in interconnect load capacitances due to coupled lines we utilize both supply and swing voltage scaling for energy saving of the clock network.

2.2.3 Clock Routing

For the clock routing, several methodologies have been introduced in the literature. A comprehensive study has been given by Cong [16]. Since the clock tree routing is a broad area for discussion, investigating the detail of this issue requires its own dedications. Here we briefly review the ideas of clock tree routing. There are several ways to categorize clock network routing. Here briefly two general categories of clock tree

routing are introduced: symmetrical and asymmetrical routing.

In symmetrical clock tree routing the idea is to build up a symmetrical clock network to achieve zero skew. H-Tree is the most straight forward way/algorithm to route clock tree with minimum skew. In asymmetrical routing, there are several algorithms introduced which attempt to equalize the length from the clock source to the sinks in a top-down or bottom-up (or combination of both) fashions. Of the asymmetrical algorithm the concept of Tsay's algorithm is reviewed since the first part of our work is related to this algorithm. In the following the two most famous algorithms for symmetrical and asymmetrical clock tree routing: H-Tree and Tsay's are reviewed.

- **H-Tree**

Consider a set of clock loads. To have a symmetrical distribution of the clock tree such that the set of clock loads be divided into two symmetric sets recursively by vertical-horizontal lines consecutively until all sets become one only. In this case it is possible to connect all loads in an H fashion. This algorithm results in a clock network called H-Tree clock network. An example of an H-Tree clock network is given in the Figure 2-11:

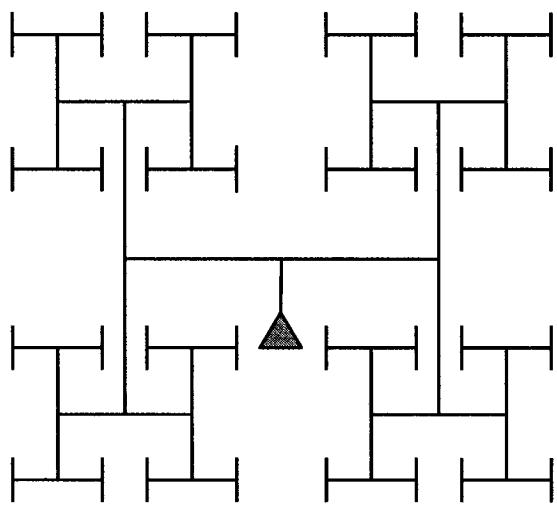

Figure 2-11, An example of a 6-level H-Tree clock network

The H-Tree increases the path length or widens the branches to equalize the path delay according to the loads attached to them.

- **Tsay's Algorithm**

Tsay proposed a method to produce zero skew clock trees based on Elmore delay model [17]. It requires an initial topology. Later the method equalizes the length of each edge of the tree in a fashion to achieve zero skew or in other words in a way that clock signal arrives on the same time at the loads according to the capacitances attached to each one. The median points (also called *Steiner* points) are selected iteratively in a bottom-up fashion. Referring to Figure 2-12, the methodology is as follows:

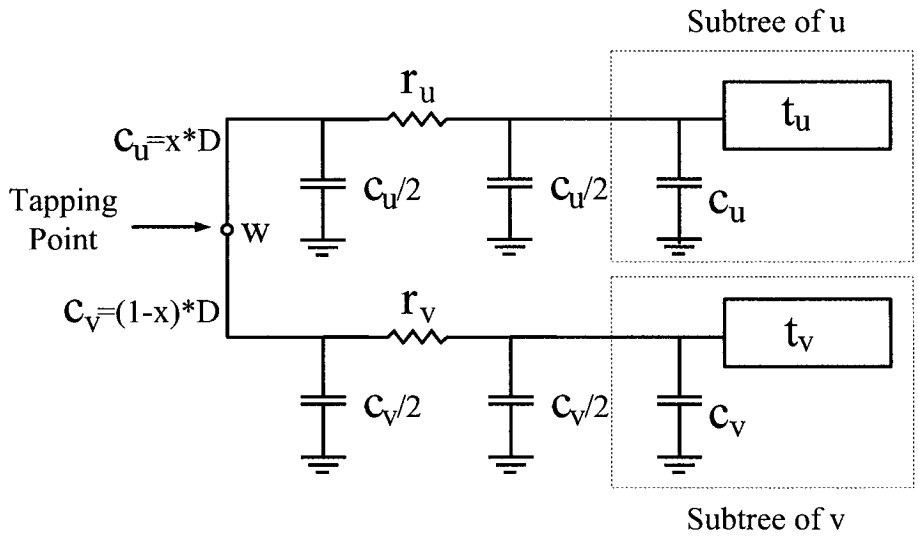

Figure 2-12, Determining edges lengths using Tsay's method for identical delay

Assuming during the method, Steiner point w is reached where u and v are the two children of the clock tree. This implies that w is the point from which all nodes belonging to sub-trees u and v have equal signal propagation delay. Let t_u and t_v be the clock signal delay from points u and v to their leaves respectively. In order to achieve zero skew, the following equation should be satisfied:

$$e_u r_0 (\frac{e_u c_0}{2} + C_u) + t_u = e_v r_0 (\frac{e_v c_0}{2} + C_v) + t_v \tag{2.13}$$

in which e_u and e_v are the edge lengths for u and v and also r_0 and c_0 are per unit length resistance and capacitance of the network wire. Also let D be the distance between u and v and x be a partitioning factor $0 \le x \le 1$. Then for u and v edges we have:

$$e_u = xD \quad , \quad e_v = (1-x)D \tag{2.14}$$

with these assumptions Equation 2.13 becomes as:

$$xDr_0 (\frac{xDc_0}{2} + C_u) + t_u = (1-x)Dr_0 (\frac{(1-x)Dc_0}{2} + C_v) + t_v \tag{2.15}$$

Solving Equation 2.15 with respect to x, results in:

$$x = \frac{(t_u - t_v) + r_0 D(\frac{Dc_0}{2} + C_v)}{r_0 D(c_0 D + C_u + C_v)} \tag{2.16}$$

If the resulting x from 2.16 satisfies the assumption of $0 \le x \le 1$, then the equalization is possible. In the case of contradicting the assumption of $x \le 0$ or $1 \le x$, then the wire length D cannot balance the propagation delay of the two sub-trees. This implies that one of the sub-trees has much greater delay than another one. For instance, the case of $x \le 0$ means $t_u >> t_v$, hence the node w must collapse on node u. this causes $e_u = 0$ and e_v according to 2.13 becomes:

$$x = \frac{\sqrt{(r_0 C_v)^2 + 2 r_0 c_0 (t_u - t_v)} - r_0 r_0 C_v}{r_0 c_0} \tag{2.17}$$

Similar approach happens for the other case when $1 \leq x$. Consequently, this will be considered as a wire elongation to equalize the delays of the two edges as given in the Figure 2-13:

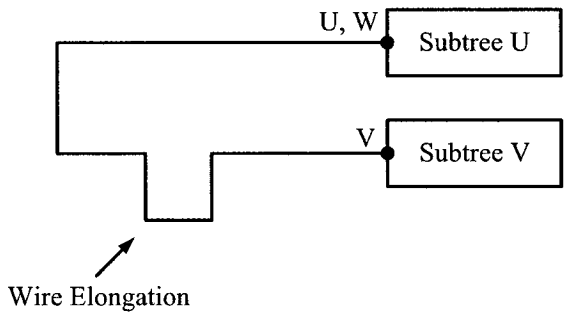

Figure 2-13, Wire Elongation for x<0, W collapse on U

2.3 Summary

In this chapter we discussed the preliminaries of the work. Two basic components of the work were introduced and discussed. We began the chapter by introducing interconnect and its parasitic elements. Later we introduced the concept of clock distribution and its figures of merit and the ways to synthesize it. In the next chapter we begin the investigation on differential signaling and the relative issues when this concept is applied to clock distribution.

3. Differential Clock Distribution

In this chapter the concepts of differential signaling scheme and coupled lines are given. The benefits and disadvantages of differential signaling are reviewed and the application of differential signaling into clock distribution network is further discussed. Due to certain advantages of differential signaling design, the motivation associated with Differential Clock Distribution Network (DCDN) design and its design challenges and problems are presented.

3.1 Differential Signaling

A binary/digital signal can be transmitted *differentially* over the medium by utilizing two conductors. One of which is used for transmitting the signal and the other is used for the complement of the signal. Figure 3-1 shows a differential voltage-mode signaling system. To transmit logic'1', the upper voltage source drives V_1 and the lower voltage source drives V_0. For logic '0' transmission, the voltages are reversed.

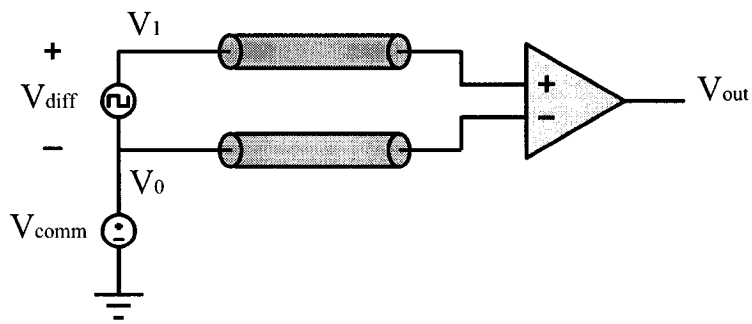

Figure 3-1, Voltage-Mode Differential Signaling

As is shown in the Figure 3-1, the following voltages are defined in a differential system:

a. V_1 is the signal on the first line with respect to common return path

b. V_0 is the signal on the second line with respect to common return path

c. V_{diff} is the differential signal which is the voltage difference of the two signal pair

d. V_{comm} is the common voltage signal which is in common between both of signal pair

Differential signal V_{diff} carries the information and at the receiver the information is extracted from this voltage difference. In addition to the differential voltage there is a common-mode signal. This signal is used to give an initial biasing to the differential signal pair. In ideal conditions, the common-mode signal is constant and it does not carry any information.

$$V_{diff} = V_1 - V_0 \tag{3.1}$$

$$V_{comm} = \frac{V_1 + V_0}{2} \tag{3.2}$$

Given the common-mode and differential signal, the single-ended voltages on each line with respect to the return path (virtual ground) can be extracted as:

$$V_1 = V_{comm} + \frac{1}{2} V_{diff} \tag{3.3}$$

$$V_0 = V_{comm} - \frac{1}{2} V_{diff} \tag{3.4}$$

Differential signaling requires more routing and wires and pins than its single-ended counterpart system. In return for this increase, differential signaling offers the following advantages over single-ended signaling:

a. A differential system, serves its own reference. The receiver at the far end of the system compares the two signal pair to detect the symbol of the information transmitted. Transmitters are less critical in terms of design issues since the receiver is comparing two pair of signals together rather than comparing to a fixed reference. This results in canceling any noises in common to the signals.

b. The voltage difference for the two signal pair between logic'1' and '0' is:

$$\Delta V = 2(V_1 - V_0) \tag{3.5}$$

which is twice as much as is defined for a single-ended signaling system. This shows that the noise margin of the differential system is twice as much as the single-ended signaling system. This doubling effect of signal swing improves the speed of the signaling system. It affects the transition times (rise/fall time) which is done in half of the transition time of single-ended signaling system.

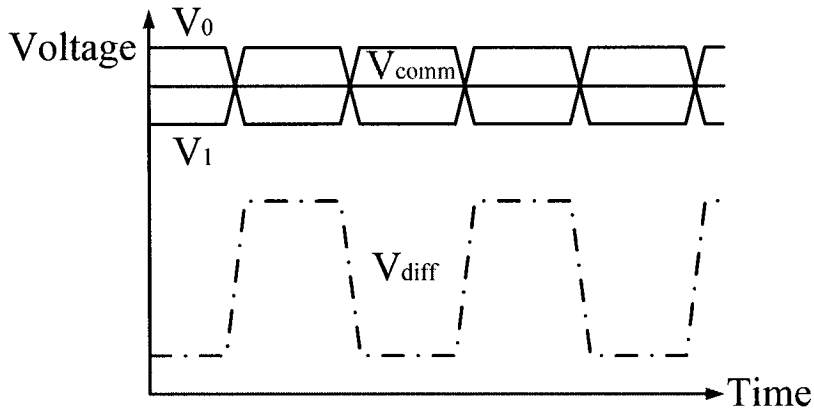

Figure 3-2, an example of signals mode in differential signaling system

After discussing the issues and different aspects of differential signaling, in the following part, the coupled interconnect and differential signal integrity issues are demonstrated.

3.1.1 Differential Signal Integrity

In order to utilize differential signaling, the coupled interconnects model is applied to the system. Coupled interconnects consist of two tightly coupled interconnect. This implies that this type of interconnect not only has the intrinsic signal integrity issues of interconnects which were discussed in the previous chapter but also they are involved with other signal integrity aspects. In Figure 3-3, a segment of a coupled interconnect is shown. As it is clear from Figure 3-3, not only the intrinsic signal elements exist in the coupled interconnects but also there are mutual parasitic elements involved.

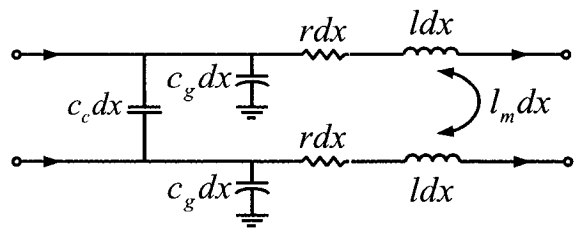

Figure 3-3, A segment of a coupled interconnect

These parasitic elements come into existence due to the adjacent line. These are mutual capacitance C_C and mutual inductance l_m in addition to the intrinsic parasitic elements r, C_g, l which indicate intrinsic resistance, capacitance and inductance of each line. The effective capacitance C_{eff} associated with each line, depending on the direction/mode of the signaling (in-phase or out-of-phase usually called *even* and *odd* mode respectively) can be calculated from the following equations [18]:

$$C_{eff\,(odd)} = 2\ C_c + C_g \tag{3.6}$$

$$C_{eff\,(even)} = C_g \tag{3.7}$$

And for effective inductance we have:

$$l_{eff\,(odd)} = l - l_m \tag{3.8}$$

$$l_{eff\,(even)} = l + l_m \tag{3.9}$$

As the above equations indicate for the case of differential signaling which is the same case as out-of-phase signaling, the effective capacitance is increased by the factor of 2 by coupling capacitances and effective inductance is decreased by the effect of mutual inductance. These facts are utilized later when the coupled lines are modeled for clock routing.

- **Switching Factor Analysis**

Kahng et al. in [19] showed that the effective capacitance obtained from Equation 3.6 depends on intrinsic signal slew rates and mutual signal degradation of the pair. The

lower signal slew rates cause this factor to increase to the upper bound 3. Thus a more precise model for the effective capacitance can be given as follows:

$$C_{eff} = \eta\, C_c + C_g \tag{3.10}$$

In which η has the value of {0, 2, 3} depending on the mode of signaling and slew rates of the coupled signals.

3.1.2 Differential Buffers

The configuration of differential buffers is based on current steering devices, in which the output logic can be set by steering the current in the circuit. These devices are also considered as Current Mode Logic (CML) circuits. CML circuits are known to outperform the conventional CMOS circuits in Giga Hertz (GHz) operation frequency. The basic differential buffer is given in the Figure 3-4:

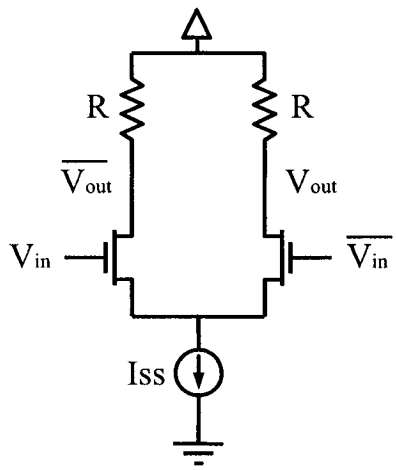

Figure 3-4, Basic Differential Buffer/Inverter

As it was mentioned before the functionality is based on current steering. The current source in differential buffer is the tail current I_{ss}. When the common mode voltage V_{comm} is applied to the differential buffer, due to the symmetry of the differential buffer, the

current is split equally between the two wings ($I_{ss}/2$). Augmenting one of the input voltages which implies the diminution of the other one (according to the principle of differential signaling and differential buffers configuration) will result in the tuning (while increasing) the current in one branch and decrease in the current of the other branch. Note that the total possible current to steer is I_{ss} and when one input voltage rises the other one decreases by the same amount. When the input differential voltage $\Delta V = V_{in} - \overline{V_{in}}$ has passed a specific threshold, in other words when one of the transistors derives all the possible current from one branch the other transistors goes off, hence the output voltage reaches V_{dd} whereas the first branch drops to $V_{dd} - RI_{SS}$. This ΔV can be approximated as [20]:

$$\Delta V = \sqrt{\frac{2I_{ss}}{\mu_n C_{ox}(W/L)}} \tag{3.11}$$

In which $\mu_n C_{ox}(W/L)$ is the trans-conductance of the input transistors. Equation 3.11 shows that the bigger the transistors the smaller the differential voltage threshold and hence the faster is the differential buffer. Due to the aforementioned, by finely tuning the I_{ss} and R it is possible to adjust the speed, swing and power consumption of the buffer.

Other design issues related to the differential buffers are the choice of differential loads. In the following the different kinds of differential loads are reviewed.

- **Differential load**

In literature different kinds of loads have been introduced [6]. The differential mode is characterized by its differential and common mode impedance r_Δ, r_C respectively:

$$r_{\Delta} = \frac{\partial \Delta V}{\partial \Delta I} \tag{3.12}$$

$$r_{C} = \frac{\partial \Delta V_{C}}{\partial \Delta I_{C}} \tag{3.13}$$

The differential impedance determines the change in the differential current I_{Δ} when the voltages on the two inputs of the terminal are varied in opposite directions. The common-mode impedance implies the average current changes when both input voltages are varied in the same direction. Three types of differential loads and their impedances are given in the Figure 3-5:

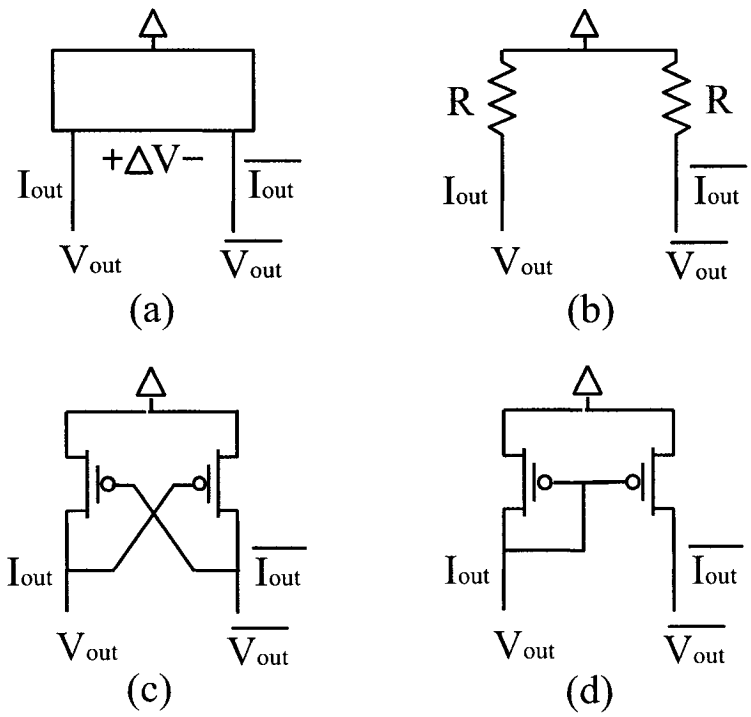

Figure 3-5, Available differential loads

Table 3-1, Differential and Common-mode impedance for various differential loads

Differential Load	r_C	r_Δ
Resistor (b)	R	R
Cross Coupled (c)	$1/g_m$	$-1/g_m$
Current Mirror (d)	$1/g_m$	$1/\lambda I$

After presenting the work background of clock distribution networks in the previous chapter and also taking the design aspects of differential system into considerations, we will begin the discussion on differential clock distribution by its overview, issues and finally by defining the problems associated with the design of such clock networks.

3.2 Differential Clock Distribution Network

3.2.1 Overview

As we discussed in the previous part, differential signaling offers higher immunity against external perturbations. Due to the complexity increase in contemporary systems which is due to the technologies advances and the need for any error free systems, the idea of integration of differential signaling and clock distribution is seemingly becoming a viable solution for future IC designs.

Historically the idea of DCDN was to be utilized for off-chip clock distribution and in the PCB level synchronization. This technique was utilized to reduce and suppress the Electro-Magnetic Interference (EMI) of the neighboring circuits and system waves. Recently due to the complexity increase and the fact that any timing uncertainty results in malfunctioning, there has been a couple of works on on-chip Differential Clock Distribution Network (DCDN).

The idea of utilizing On-Chip DCDN has not been widely used in the literature. Anderson et al. in [21] utilized DCDN in the global level in their hierarchical CDN for

Itanium Microprocessor. They reported that the use of DCDN has given the advantage of 10% less skew variation. Sekar in [22] reported that DCDN has 25%-42% less sensitivity to power supply noises and 6% less sensitivity to manufacturing variations when they utilized H-Tree DCDN.

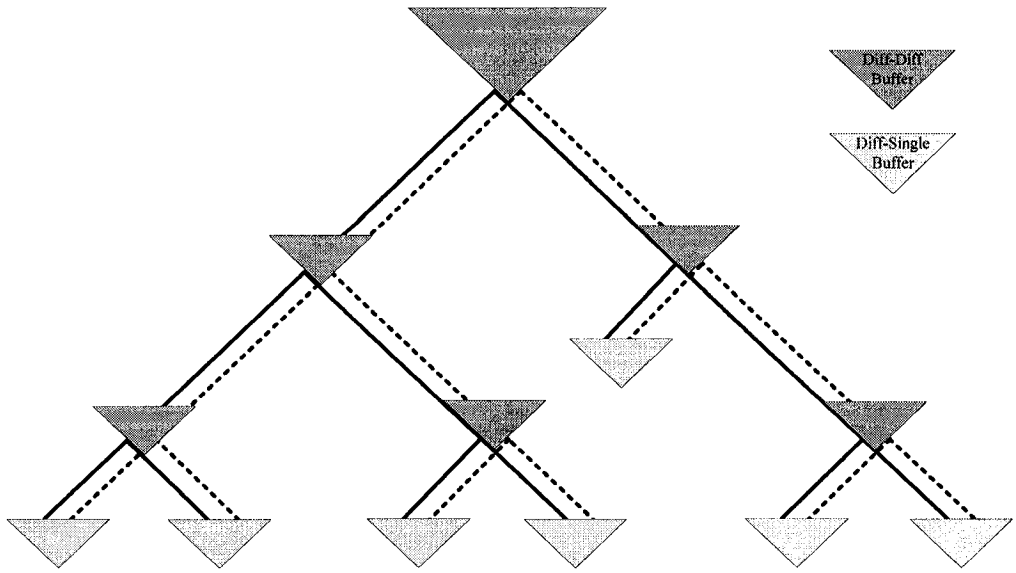

Figure 3-6, A general structure for Differential Clock Distribution Network

A schematic for DCDN is given in Figure 3-6. The DCDN is composed of a differential signal pair shown in two different patterns. The clock tree generally is a binary tree. The differential signal is dispersed along the clock network. Throughout the clock network at branching points the differential clock signals are regenerated by differential buffers to improve the signal integrity of the clock network. Finally at the last stage, they are all converted to single-ended signals for compatibility with the rest of the system functionality, which normally use single-ended signals. For the regenerative buffers a simple differential buffer introduced in the previous part can be utilized. The only design issue related to the buffer is the choice of differential loads. Based on the process technology, or design criteria, this item can be chosen from the design library. For final stage converters, usually the choice of current mirror load is the superior choice. As table 3-1 demonstrates, current-mirror loads have high differential output impedance which

results in fast change in the output that is used to drive the output of the clock network.

3.2.2 Motivations to design On-Chip DCDN

Differential clocking eliminates the induced crosstalk due to aggression of clock signals. Clock signal is spread all over the chip area. It also has full switching activity. Also device sizes tend to shrink as technology advances. These facts show that as technology advances the clock signal aggression can be quite harmful for all system components all over the chip area. Distribution of clock with differential signals eliminates this problem, to certain extend as both positive and negative signal values are applied and the noise would be cancelled.

Furthermore, as was given in [21], DCDN offers less skew variations in the presence of external noises, it has less sensitivity in presence of supply and process variations [22].

The aforementioned points are of the most important criteria/solutions for reliable system design. Due to technology advances and increase in system complexity, the design with low variation or no variation in ideal case has become the most concerning issue. Timing error results directly in system malfunctioning. Thus designing a reliable, noise tolerant, clock distribution may help significantly for a reliable system design. As introduced in the literature, DCDN has these potentials thus this design methodology can be a solution for future, robust system design.

After presenting the motivations and benefits of DCDN, design problems associated with these concepts are presented.

3.2.3 DCDN Design Problems

As given in the previous part, DCDN has advantages and benefits for future robust system design. However there are still some problems associated with the design of DCDN:

1. There is no general model/algorithm proposed for zero skew routing of DCDNs. The existing models/algorithms do not satisfy the concept of zero skew routing of DCDN. The existing ideas rely on the symmetric clock networks which intrinsically have no need for zero skew routing.

2. Differential signaling has higher parasitics associated with the coupled lines. Due to the doubling of lines, the total power consumption is increased. This problem should be solved to have a power efficient DCDN.

In the following chapters, these problems are addressed and some solutions are proposed.

4. Zero Skew Routing of DCDN

In the previous chapters the background of differential clocking and problems associated with clock network design method was given. In this chapter a new line delay model for zero skew routing of the differential clock trees is presented.

4.1 Preliminaries

In chapter two we became familiar with the concept of clock routing. Cong in [16] presents a comprehensive study on efficient clock routing. Tsay's method [17] is one of the methods introduced for zero skew routing of the clock trees. In order to route differential clock trees with zero skew characteristic, the existing methods are modified to satisfy design objectives. To achieve this aim here in this part, a line equivalent delay model is proposed. The model is applicable to Tsay's method [17] for zero skew routing of differential clock trees.

4.2 Modeling Differential Lines Utilizing Decoupling Technique

In order to efficiently model differential lines, several solutions have been proposed in literature. One method is to model each line and write the Kirchhoff laws for the return path as given in [18] and another method is to decouple the lines utilizing the intrinsic and coupling effects equations of each line as given in [18, 23]. In this design project the latter design methodology was utilized to model the effect of differential lines. In the following we review the process of modeling coupled interconnects using Kirchhoff's laws and later decoupling technique:

In odd-mode differential signaling, the current flow on the two differential lines as shown

in Figure 4-1 have the same magnitude but opposite direction. For proper modeling of coupled lines, the interconnect components should be modeled efficiently.

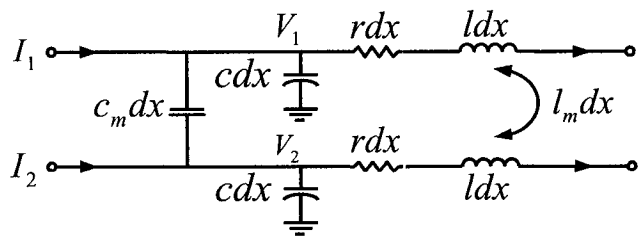

Figure 4-1, Coupled lines and its parasitic when driven differentially

Effective Inductance: To extract the effective inductance, the voltage induced by inductive coupling is calculated by Equation 4.1 as:

$$V = L\frac{di}{dt} \tag{4.1}$$

Subsequently, applying Kirchhoff's voltage law produces:

$$V_1 = L\frac{dI_1}{dt} + L_m\frac{dI_2}{dt} \tag{4.2}$$

$$V_2 = L\frac{dI_2}{dt} + L_m\frac{dI_1}{dt} \tag{4.3}$$

Since the signals for odd-mode differential switching are always opposite, there exists $I_1 = -I_2, V_1 = -V_2$; these yields:

$$V_1 = L\frac{dI_1}{dt} + L_m\frac{d(-I_1)}{dt} = (L - L_m)\frac{dI_1}{dt} \tag{4.4}$$

$$V_2 = L\frac{dI_2}{dt} + L_m\frac{d(-I_2)}{dt} = (L - L_m)\frac{dI_2}{dt} \tag{4.5}$$

There the effective inductance seen by each line in odd-mode is:

$$L_{effective\_differential} = (L - L_m) \tag{4.5}$$

Effective Capacitance: In a similar fashion the effect of mutual capacitance can be derived. Recalling that the current induced by capacitive coupling is calculated by Equation 4.6 as:

$$I = C\frac{dv}{dt} \tag{4.6}$$

Subsequently, applying Kirchhoff's current law at nodes V1 and V2 produces:

$$I_1 = C\frac{dV_1}{dt} + C_m\frac{d(V_1 - V_2)}{dt} \tag{4.7}$$

$$I_2 = C\frac{dV_2}{dt} + C_m\frac{d(V_2 - V_1)}{dt} \tag{4.8}$$

The Substitution of $I_1 = -I_2, V_1 = -V_2$ yields:

$$I_1 = C\frac{dV_1}{dt} + C_m\frac{d(V_1 - (-V_1))}{dt} = (C + 2C_m)\frac{dV_1}{dt} \tag{4.9}$$

$$I_2 = C\frac{dV_2}{dt} + C_m\frac{d(V_2 - (-V_2))}{dt} = (C + 2C_m)\frac{dV_2}{dt} \tag{4.10}$$

Therefore the equivalent effective capacitance seen by each line in odd-mode in differentially driven coupled lines is:

$$C_{effective\_differential} = (C + 2C_m) \tag{4.11}$$

After qualitatively (analytically) extracting the effective parasitic elements of the differential line, the quantification of inductive element is discussed. For the case of effective inductive coupling, differential signaling is known as a trend to resist inductive effects. The intrinsic inductance is reduced by the effect of mutual inductive effect. Quantifiably, [24] Reports a small quantity for effective inductance for multiple lines. For example for a twin differential line, consisting of two lines driven differentially, the effective inductance is given as 1nH for 2.0mm top metal layers driven in GHz ranges in 0.18u technology (in Precision less than 0.5nH/mm). Maheshwari in [25] reported a negligible amount of delay difference between the RC and RLC model of the line (less than 0.1ns delay difference for a 2cm Line). It shows this negligible difference due to the opposite direction of signals which degrades the total effect of inductance.

Due to the aforementioned, effective inductance in differential signaling is negligible. In this research project, the inductive effect of differential pair in our design and analysis is ignored.

4.3 Tapping Extraction in Differential Clock Trees

The approach used here to obtain zero skew using DCDN follows Tsay's method [17]. In this method zero skew is achieved by locating tapping points throughout the clock tree. Tapping points are the branching points at which sub-trees are chosen to maintain equal delay as in Figure 4-2.

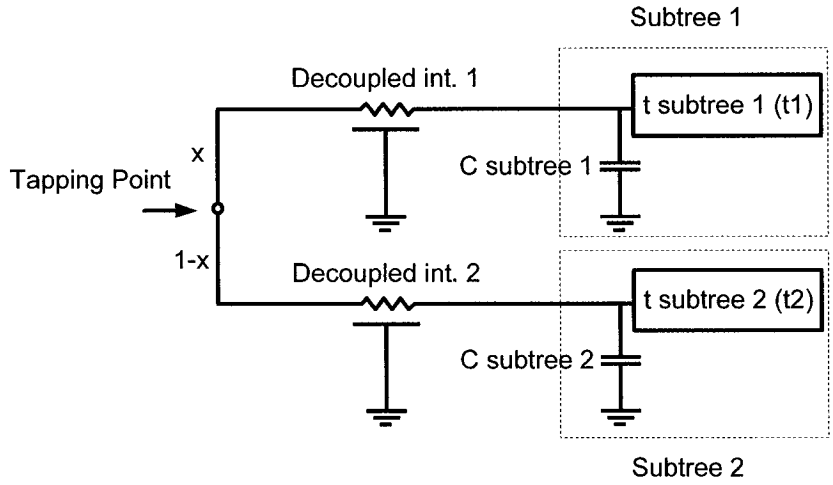

Figure 4-2, Tapping point extraction through merging decoupled sub-tree(s)

As was discussed in the previous section, the decoupling method is utilized to model differential signals. Also the effective inductive effect is neglected. Thus in this research project, decoupled RC Π model is used to model interconnects. The methodology of tapping extraction is as follows:

Figure 4-2 shows a schematic of a decoupled clock tree branch in which each line of the branch is a decoupled distributed RC model connected to its sub-tree child, for which the distributed line propagation delay is given by $t_{int}=0.37R_{int}C_{eff}$. Each sub-tree is modeled by a total capacitance $C_{subtree}$ and total propagation delay tsubtree as shown in Figure 4-2. Considering tapping location x, to satisfy the equality of the two branch delays, the following equation is realized:

$$t_{\text{int }1} + 0.74R_{\text{int }1}C_{subtree\ 1} + t_1 = t_{\text{int }2} + 0.74R_{\text{int }2}C_{subtree\ 2} + t_2 \qquad (4.12)$$

In the second part of the equality, since the interconnect resistance combined with sub-tree capacitance creates a Lumped loop, it has the lumped propagation delay of $0.74R_{int}C_{subtree}$ (as given in the lumped model of interconnects in chapter 2).

Assuming that:

$$R_{\text{int }1} = r_0 x\ell \quad , \quad C_{\text{int }1} = c_0 x\ell$$
$$R_{\text{int }2} = r_0(1-x)\ell \quad , \quad C_{\text{int }2} = c_0(1-x)\ell \tag{4.13}$$

in which r_0, c_0 are the resistance and capacitance per unit length of the wire, ℓ is total interconnection length between the two sub-trees and tapping location x. Solving equation (4.12) with respect to x results in:

$$x = \frac{1.35(t_2 - t_1) + r_0\ell(C_{2eff} + 0.5c_0\ell)}{r_0\ell(C_{1eff} + c_0\ell + C_{2eff})} \tag{4.14}$$

In case of ($x \leq 0$ or $x \geq 1$), elongation would be needed. The length of elongation to maintain zero skew is given by:

$$L' = \frac{-20r_0C_{2eff} + 2\sqrt{100r_0^2C_{2eff}^2 + 270r_0c_0(t_1 - t_2)}}{20r_0c_0} \tag{4.15}$$

The proposed decoupled line delay model using Tsay's method was applied to benchmarks r1...r5 (Tsay [17]). A CAD model given in appendix B, consisting of the DME algorithm [26] implemented using C++ for clock routing and PERL language for netlist manipulation was utilized for design and simulations. HSPICE simulation results for the proposed method are tabulated in Table 4-1. The delay and skew results presented throughout this thesis represent the average and absolute difference of clock signal phase delay at sink nodes respectively.

Two methodologies were used for routing differential lines: Single-Spaced (SS) and Double-Spaced (DS) routing. In Single-Spaced routing scheme, mutual coupling effects are stronger, therefore differential characteristics of the pair is more dominant. DS

offers smaller mutual coupling, consequently this reduces delay while degrading noise immunity. Figure 4-3 demonstrates the spacing between differential pair.

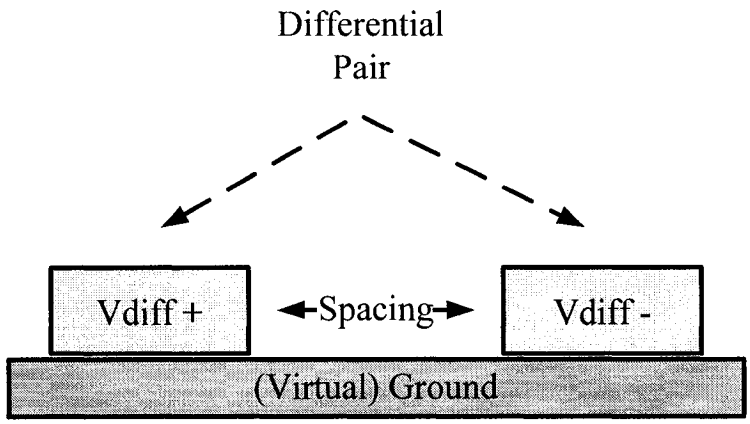

Figure 4-3, Spacing configuration in routing of differential pair

Table 4-1 demonstrates that, on average, clock trees generated with the proposed model show 97% skew reduction compared to those obtained using Elmore model. This improvement is achieved because coupling effects of differential lines are more accurately considered in the algorithm leading to tapping point selection. As technology advances the coupling effects increase and we are no longer able to neglect these effects in system modeling. In this case, neglecting the coupling effects, results in the misplacement of tapping points and reduces the effectiveness of the considered zero skew DCDNs. Simulation results also show smaller delay and skew for the DS scheme due to reduced coupling, however this design strategy as we will see degrades robustness in presence of external noise.

Table 4-1, Skew and delay of DCDN for benchmarks [17] based on proposed and Elmore delay model (V_{DD}=1.8V) based on the technology model given in appendix A.

Bench Mark	Elmore (SS)		Proposed Model (SS)		Proposed Model (SS)	
	Skew(ps)	Delay(ns)	Skew(ps)	Delay(ns)	Skew(ps)	Delay(ns)
r1	115	1.1	5.9	1.1	2.4	0.9
r2	199	3.8	15	3.7	8.8	3.3
r3	341	5.1	14	5.1	8.0	4.6
r4	759	17.5	36	17.1	20	14.5
r5	1825	34	51	34	39	28

4.4 Applying buffers

Buffer insertion is used as a method to improve the performance of interconnects and clock networks as mentioned in chapters 2 & 3. In this part, conventional differential buffers are utilized to investigate the effect of post processing of differential clock network by using differential buffers. In order to having a novelty in this design, the Dynamic Threshold (DT) [27] (sometimes referred to as Body-Biased) transistors were utilized. These transistors outperform the conventional transistors in low voltage applications which are suitable for advanced low voltage technologies. The use of DT transistors [27] helps improving the buffer performance. DT transistors switch faster since their threshold voltage decrease dynamically when the input is applied to their gate terminal. Recalling the body-effect threshold voltage equation:

$$V_T = V_{T0} + \gamma(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}) \tag{4.16}$$

In which $V_{T0}, |\phi_F|, \gamma$ are the zero-biased threshold voltage, bulk Fermi potential and body effect coefficient respectively. These parameters are technology constant.

The difference between conventional and DT-based differential buffers is the use of DT transistors which have superior performance when used in low supply voltages. The schematic of the buffers are given in Figure 4-4.

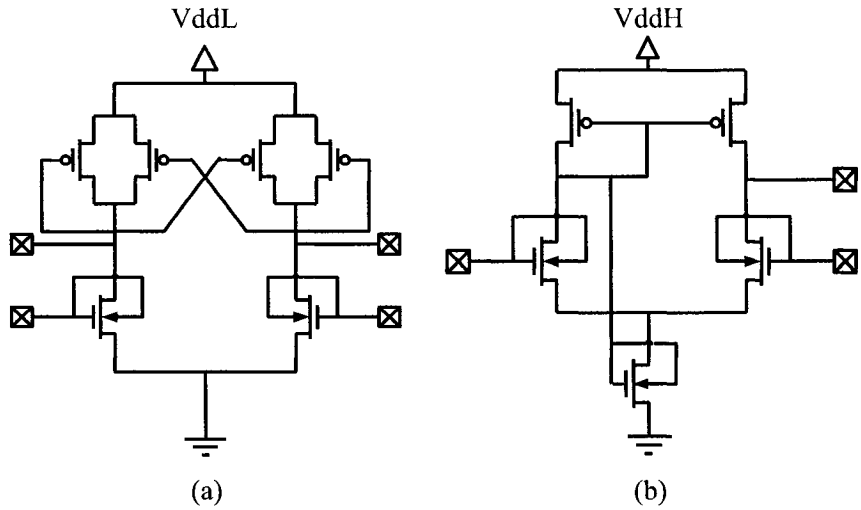

Figure 4-4, Proposed (a) Low Swing (b) Full Swing DT differential buffers

Figure 4-4(a) presents a Low-Swing: Low-Swing differential buffer. DT transistors help improving the speed of these buffers when low swing inputs are applied to the buffer. The use of cross-coupled differential load with high differential impedance helps to have a fast transition of the inputs to the outputs as mentioned in the previous chapter.

Figure 4-4(b) represents a Low Swing to Full Swing level converter buffer. This buffer is used at the sinks to restore clock signals to their single-node full amplitude. The current-source pull-ups help to have asymmetrical fast transformation of differential to single-ended. The structure is based on Chappell amplifier which offers good common-mode noise rejection [28].

Buffer insertion was performed to improve the performance of benchmark clock networks. The buffer insertion procedure is as follows: Low swing buffers were inserted at branching points and level converting buffers were inserted at sinks. Low swing buffers are sized to reduce propagation delay throughout the clock network. To

accomplish this, a base size for buffer according to its delay-power characteristic diagram was chosen to drive a unit length interconnect segment as given in Figure 4-5. Further, the buffers were uniformly sized according to the longest interconnect.

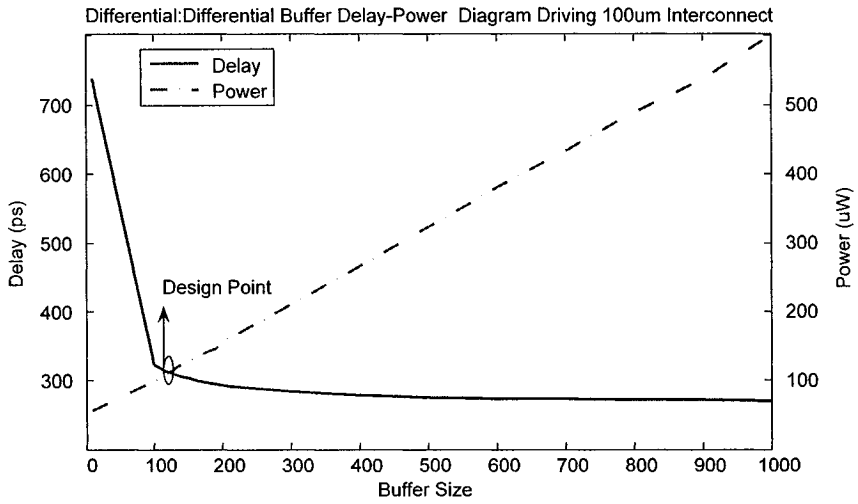

Figure 4-5, Characteristic diagram of a Differential-Differential buffer driving a 100um global interconnect

Full swing converters (Differential:Single-ended) were composed of minimum size transistors to reduce the power consumption and skew reduction; their sizes were scaled up relative to their load capacitance.

Table 4-2 shows the skew and delay difference for similarly sized, buffered DCDN based on conventional [6] and proposed buffers. It shows 25% delay and skews improvement on average compared to conventional buffers in low swing differential clocking scheme. Results show that the delays reduce significantly while skews are degraded as compared with un-buffered DCDNs. We believe that skews in buffered clock networks can be reduced significantly by enhancing the process of buffer insertion. For instance, differential buffers delay model should be considered when tapping points are selected in the zero skew DCDN design algorithm.

Table 4-2, Skew and Delay of Buffered Differential Clock Networks (Full Swing Vdd=1.8V, Low Swing Vdd=0.5V)

Benchmark		r1	r2	r3	r4	r5
Low Swing Conventional	**Skew (ps)**	695	844	808	1388	1566
	Delay (ns)	9.6	10	10	11.9	13.1
Low Swing Proposed	**Skew (ps)**	545	679	667	981	1135
	Delay (ns)	7.0	7.7	7.8	8.8	9.6
Full Swing Conventional	**Skew (ps)**	71	163	127	379	532
	Delay (ns)	1.1	1.3	1.3	1.6	1.9

4.5 Skew Sensitivity of the proposed design methods

In this part, two types of external aggressors which result in random skew are investigated: Power supply variations and crosstalk. Comparisons were made between similarly designed Single-node CDN, Single-Spaced (SS) DCDN and Double-Spaced (DS) DCDN. Benchmark r3 is used for simulations due to its average characteristic in terms of size and simulation time.

4.5.1 Power supply variations

For experiments of this part, the effect of power supply variations on two low swing DCDN and full swing DCDN were compared with the effect of power supply variations on low swing Single-node CDN and full swing Single-node CDN. For the low swing scheme, the power supplies were $V_{dd}H$=1.8V & $V_{dd}L$=0.5V, whereas for full swing scheme a single supply voltage ($V_{dd}H$=1.8V) was used. In those experiments, supply voltages were varied by ±10%.

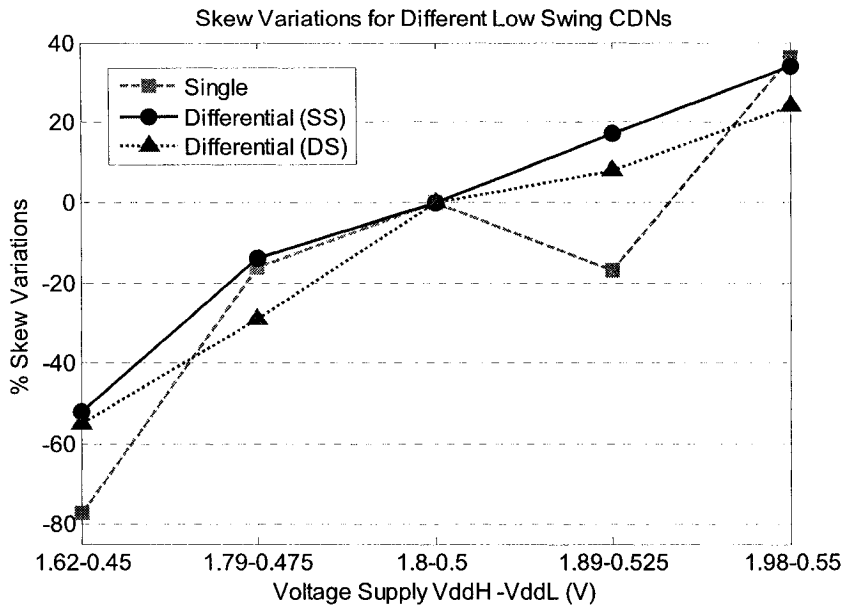

Figure 4-6, Skew variations due to supply variations in Low Swing Scheme

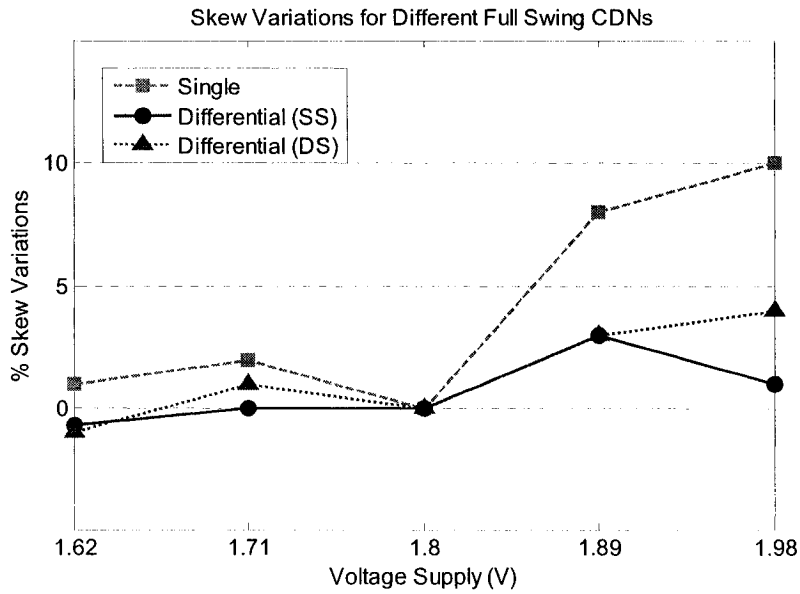

Figure 4-7, Skew variations due to supply variations in Full Swing Scheme

Simulation results show that for both clocking schemes, the proposed Single-Spaced (SS) DCDN is the most robust design method in the presence of power supply variations when compared to other CDNs. Skew variations increase when low-swing clocking is used.

Double-Spaced (DS) DCDN has less robustness to supply variations. DCDN is seen to have up to 25% less skew variations in low swing clocking scheme and up to 9% less skew variations in full swing clocking scheme than Single-node CDN in presence of power supply variations.

4.5.2 Crosstalk Coupling

Another source of perturbation that causes delay uncertainty in CDNs is crosstalk. For experiments, a full swing aggressor is applied to one of the two big-child of the clock tree. The same low swing and full swing clocking schemes were considered. Simulation results show that Single Spaced (SS) DCDN shows 6% less skew variations when combined with low swing clocking scheme and 9% when combined with full swing clocking scheme as compared to Single-node CDN subject to crosstalk.

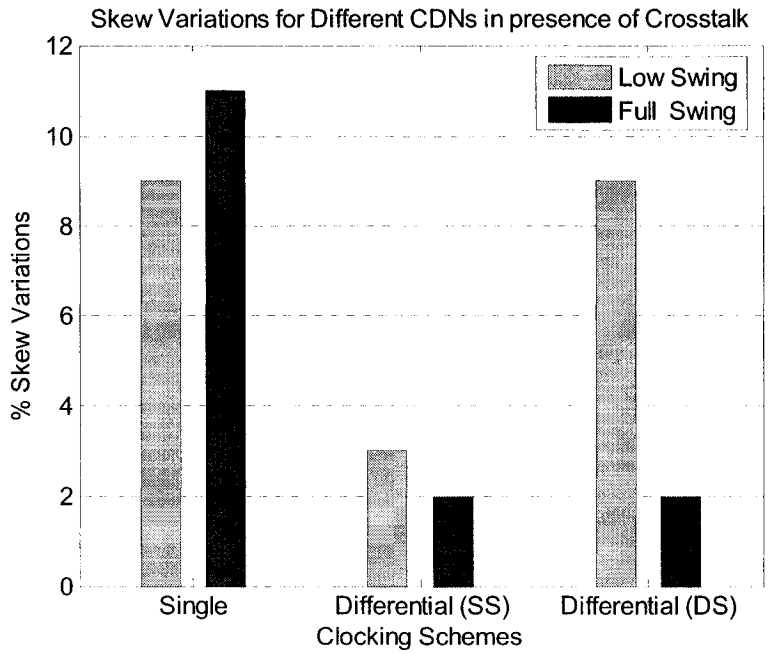

Figure 4-8, Skew variations due to crosstalk

4.6 Summary

In this section a delay model was developed and was applied to zero skew design method for differential clock distribution networks. The improved method shows 97% skew reduction compared with the same method based on Elmore model. To improve differential clock network performance, differential buffers based on dynamic threshold transistors were introduced and incorporated into zero skew clock networks. The incorporated buffers show 25% delay and skew improvement in low swing clocking scheme compared to conventional buffers. Moreover, the proposed low swing differential clock network shows 25% and 6% skew variations reduction in presence of power supply variations and crosstalk respectively, as compared to single-node clock distribution network.

5. Energy Efficient DCDN

In this chapter, we propose circuit techniques which improve the energy savings of the method of differential clock distribution. As mentioned previously, differential clocking is associated with higher routing and complexity issues which results in higher power consumption. The proposed circuit techniques help to overcome this issue. The energy saving is done in two steps: First, by proper modifications of differential buffers both in intermediate buffers and final stage buffers, we contribute to further reduction of the differential voltage swing of the clock signal which help to reduce the power consumption. Later, by reducing the supply voltage we additionally assist further energy saving of the clock network.

5.1 Differential Voltage Scaling

In this part, we investigate the effect of differential voltage scaling on the performance of the differential clock network. First, we introduce the circuit techniques and reduce the differential voltage for further energy saving of the clock tree. Later the effect of differential voltage reduction is investigated.

5.1.1 Proposed Differential Buffers

A. Final Stage Differential Level Converter

Recalling from Section 3.1, two voltage components are associated with differential signaling method: Common-mode and differential voltage. Common-mode also referred to as DC voltage biasing and is the voltage used for initial biasing of the differential buffer.

In order for differential receivers (differential to single-ended converters) to operate efficiently and have a full/proper output swing, the common-mode voltage or DC biasing of the differential buffer should be low enough to turn the input transistors off. In the literature, the method used in order to overcome this issue is to increase the voltage swing as much as possible to be able to decrease the common-mode voltage to the sufficient supply level (usually used differential voltage of 50% of V_{dd}) [21, 22]. This method results in a high power consumption of the clock network by two means: first, according to the basis of differential buffers (recalling from Chapter 3) the differential swing is derived from:

$$V_{diff\_low} = V_{dd} - RI_{ss} \tag{5.1}$$

The above equation implies that in order to increase the differential voltage swing, the only way is to increase the current tail which highly affects the power consumption of the clock network. Worth mentioning is the fact that, it is not possible to touch the loads since it directly affects the bandwidth of the clock network. Due to the aforementioned, in the previous works, to reach sufficient output swing the method used was to increase the differential voltage swing to reduce the common-mode voltage. Here, we propose a circuit technique to address this design problem.

The proposed differential receiver is given in Figure 5-1. The buffer configuration is based on Chappell amplifier [28] as introduced in previous section. Attached to the buffer are the level-shifting circuits. The buffer functionality is as follows:

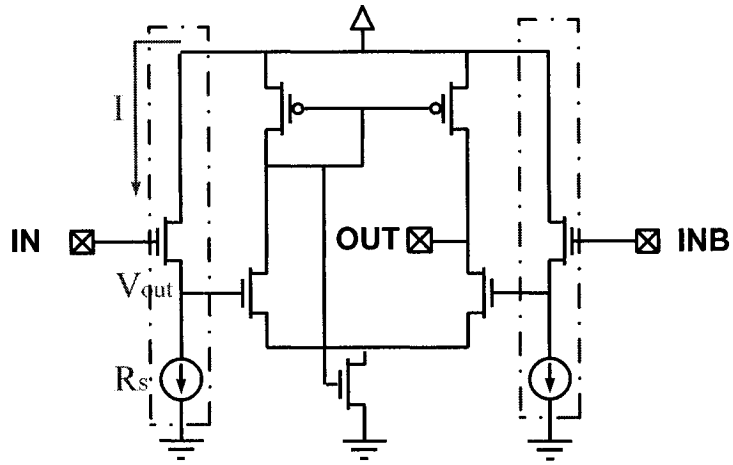

Figure 5-1, Differential Receiver with Level Shifter

The dashed parts of the receiver are the level shifters (also referred as source followers) [20]. When the input is applied to the gate terminals of the level shifter circuits, the output is dropped and follows its input. In other words, the voltage gain equals one (no voltage amplification), and the following relations are applicable [47]:

$$
\begin{aligned}
I &= \frac{\beta}{2}(V_{IN} - V_{OUT} - V_T)^2 \\
V_{OUT} &= I \cdot R_S \\
V_{OUT} &= (R_S \cdot \frac{\beta}{2})(V_{IN} - V_{OUT} - V_T)^2 \\
V_{OUT} + V_T + (\frac{V_{IN} - 2}{R_S \cdot \beta})^{0.5} &= V_{IN}
\end{aligned}
\tag{5.2}
$$

The last result shows that V_{OUT} can be derived by solving the final equation iteratively. However, by making the first order approximation that R_S is large enough (especially in current sources) to make the third term equal zero, we can conclude the following:

$$V_{OUT} \approx V_{IN} - V_T \tag{5.3}$$

This shows that the output of the source follower circuits copies the input of the gates with a shift of a transistor threshold which is a technology dependent factor (In CMOS 0.18um used in our simulation the collapse ratio or voltage drop is almost 0.5V). The transistor ratios for buffers sizing are the same as the ones given in [28]. However, the total size of the buffer is scaled to minimize the skew.

According to the aforementioned points, the above configuration of the differential receivers helps lower the common-mode (DC bias) of the internal input transistors of the receiver. Utilizing this design technique, it is possible to further reduce the differential voltage swing while maintaining a sufficient output swing at the final nodes.

B. Intermediate Differential Buffer

In order to perform differential voltage scaling in the proposed differential clock distribution network and to further evaluate the performance of the proposed clock networks while varying differential voltage, in the previous section, a new design for level converter was proposed. For the case of intermediate buffers, in order to be able to vary the differential voltage while maintaining the linearity of the buffer, the differential load should be reconfigured in a way to establish this design goal. In this part, a new configuration for differential load is proposed which enables us to have linearity in the buffer. Figure 5-2 shows the proposed buffer configuration.

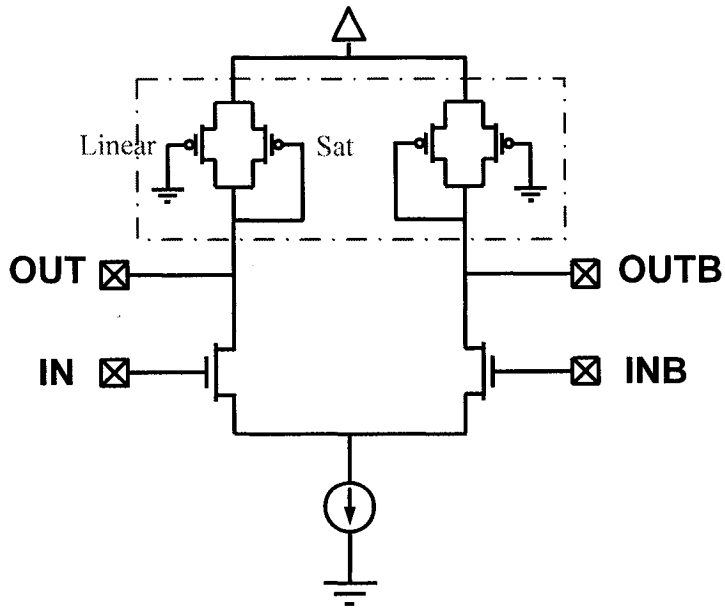

Figure 5-2, Differential Buffer with Composite Load

The dashed part demonstrates the proposed composite configuration of the differential load. Such composition enables the circuit to combine both the characteristics of the diode connected device and triode transistor together to have a linear operating load in various voltage range. Figure 5-3 shows the I-V characteristic of the proposed differential load.

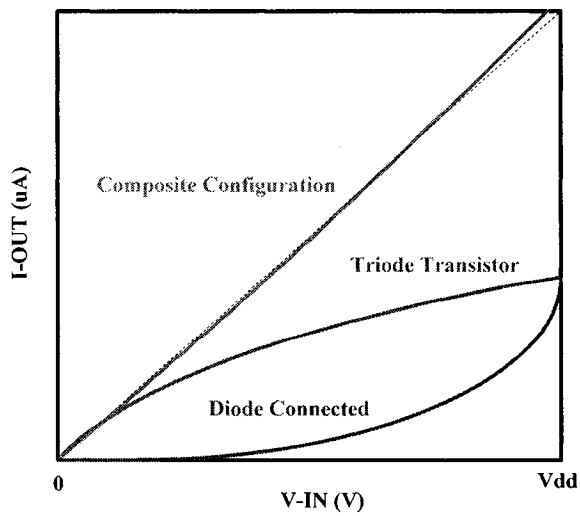

Figure 5-3, Composite configuration of differential load

As it can be understood from Figures 5-2 and 5-3, the diode connected transistor with quadratic I-V characteristic cancels the negative quadratic characteristic of grounded triode transistor. This combination provides the linearity in the operation of differential load. This linear operation could be achieved using simple resistor in the design. The purpose of utilizing transistors to build up differential load is the portability of the design.

The proposed differential load is a technology portable design and can be used in any available design process whereas the use of resistance is limited to current and future advanced technologies. This portable design method comes at the price of area and increase of parasitic elements. The transistor ratios for buffers sizing are 1 to 3 which refer to the ratio of pull up to pull down transistors ($L=2L_{min}$ to reduce the channel length modulation effect). The total size of the buffer is scaled to reach the objective frequency of operation.

5.1.2 Performance Evaluation of Differential Voltage Scaling

After proposing the circuit modifications to perform differential voltage-swing scaling, in this part the effect of this process on clock network performance is investigated. For comparison and performance evaluation of clock networks, a set of 400 MHz differential clock distribution networks were designed for different differential voltage swings for benchmark r3 due to its average size [17]. This was done by tuning the tail current source. The lower bound for differential voltage is achieved from $V_{dd} - RI_{SS}$ where these variables represent supply voltage, tail current and equivalent load resistance respectively. By finely tuning the tail current, it is possible to design the differential clock networks with the determined differential voltage swing. The load resistance determines the bandwidth (frequency) of the clock network hence the only variable with which we are able to tune the differential voltage swing is the tail current.

The performance evaluation of the clock networks is done by two means: first is to investigate the power consumption of the clock network and observe the effect of voltage scaling on power consumption and second is to investigate the variations against

external perturbations such as power supply variations and crosstalk. In the following we will investigate the effect of voltage scaling on these two criteria.

A. Effect of differential voltage scaling on power consumption

As previously mentioned, tail current was considered as a variable for tuning the differential voltage swing. The tail current affects both the short circuit and dynamic power dissipation. The short circuit power is consumed directly from the tail current in each differential buffer. In the case of dynamic power dissipation, recalling from Equation 2.11, by decreasing the tail current, the voltage swings of the coupled lines are reduced which contributes to the power reduction of the network. Figure 5-4 demonstrates the effect of differential voltage scaling on the power consumption of clock networks. It also shows the power consumption of the single-node clock distribution network.

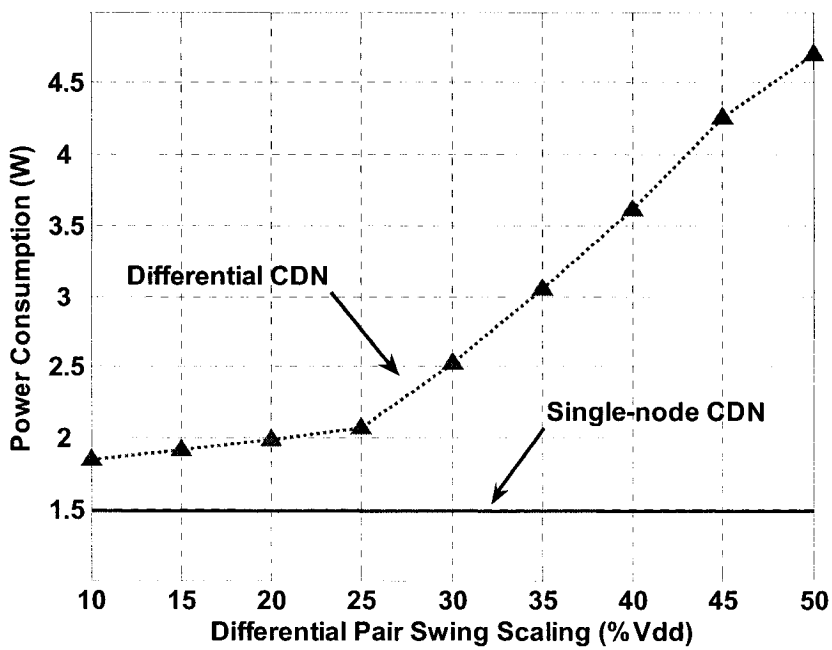

Figure 5-4, Power consumption for differential voltage scaled DCDNs vs. Single-node CDN (Benchmark r3)

As shown in Figure 5-4, the differential voltage scaling highly affects the power consumption of the differential clock network. As the differential swing increases beyond the 25% of supply voltage (450mV, V_{dd}=1.8V), the power consumption increases drastically. For the differential voltage swings below the 450mV, the power consumption is not much affected by the differential swing scaling. The lower bound of 10% of V_{dd} for the differential swing is due to the fact that for differential voltage swings smaller than 180mV and the common-mode voltage of 1.7V (Equation 3.2), no longer the common-mode voltage is low enough to turn the input transistor of converter off and have a sufficient output swing. Another consideration of the above figure is that even with low differential swing of 10% of V_{dd} (180mV), still the power consumption of differential clock network is almost 30% higher than that of single-node clock distribution network.

B. Effect of differential voltage scaling on clock network robustness

Another criteria for performance evaluation of clock network considered before was variations in skew. In section 4.1 we showed that differential clock networks have 25% less variations to power supply fluctuations. In this part, we will see how these variations change while scaling the differential voltage swing. Figure 5-5, demonstrates the effect of power supply variations on differential clock network skew while scaling the differential voltage swing.

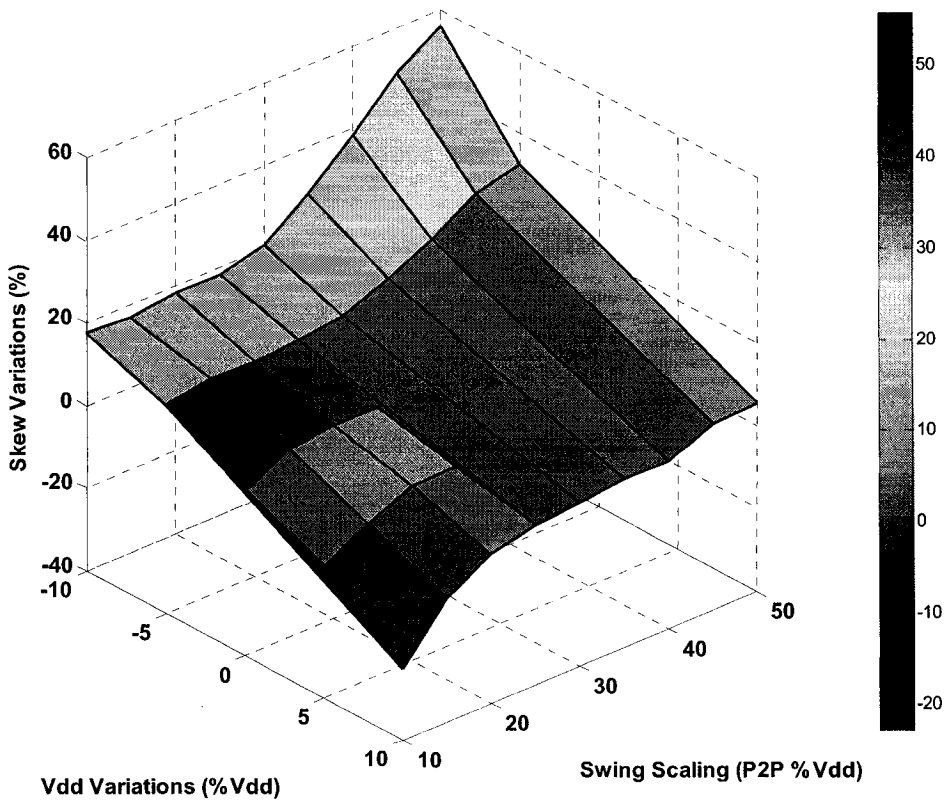

Figure 5-5, Simulation results showing skew variations with differential swing scaling of DCDN

In the above figure, x axis represents the total power supply variations (±10% of V_{dd}), y axis is the voltage swing scaling from 50% off V_{dd} down to 10% of V_{dd} (900V down to 180mV) and z axis demonstrates the skew variations for various differential voltage swings in the presence of power supply variations. For better understanding of the above figure, if we represent the max peak to peak skew variations (peak to peak of z axis) with respect to differential swings (y axis) we can draw Figure 5-6.

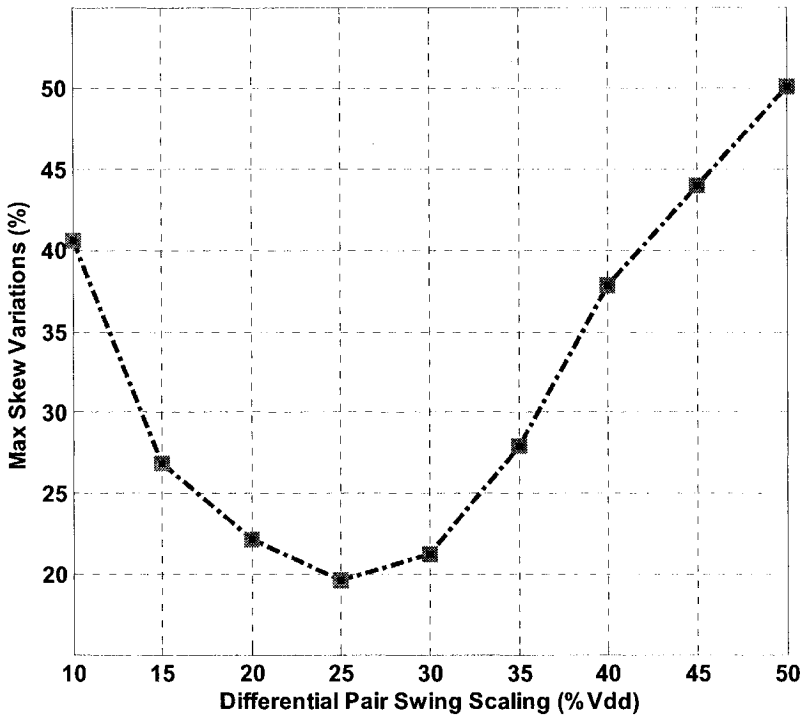

Figure 5-6, Peak to peak skew variations in differential voltage scaled DCDN

In Figure 5-6, it is shown that the minimum variation occur when the voltage swing equals 25% of V_{dd} (450mV). The reason in the increase of the two bounds of differential swing (180mV and 900mV) is that for the 180mV case when the supply voltage increases by +10%, the common-mode voltage increases enough not to make the output signal sufficiently fast. Similar case happens for the 900mV case with the decrease of -10% in power supply, two inputs drop sufficiently which disturbs the converters functionality.

The increase in the voltage swing along with the decrease in the supply voltage and vice versa gives a relative symmetry. Figure 5-6 can be redrawn as:

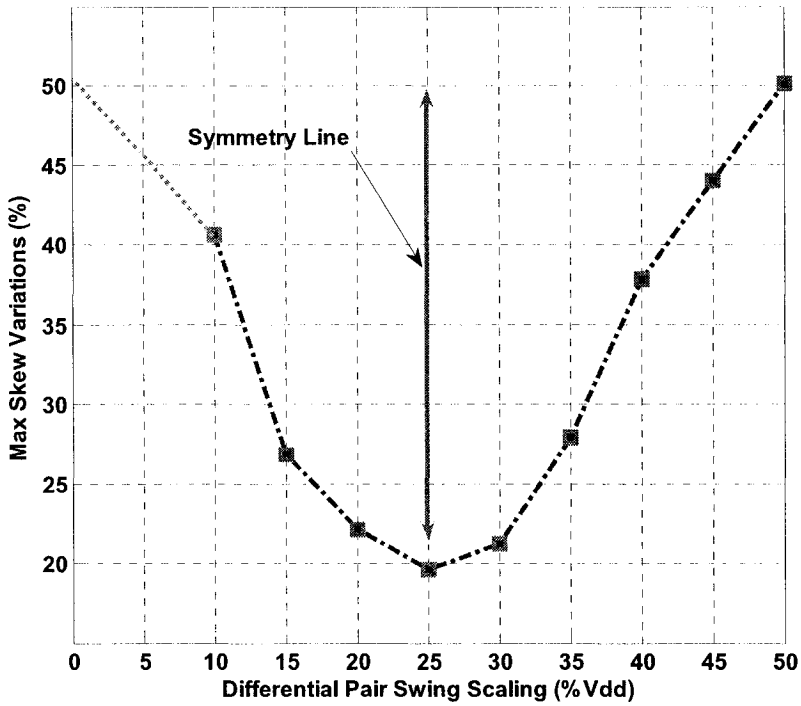

Figure 5-7, Symmetry of peak to peak variation due to supply fluctuations of swing scaled DCDN

Another experiment which was performed to determine the effect of voltage swing scaling on the robustness of the differential clock network is applying the external aggressor to one of the two big-child of the clock network.

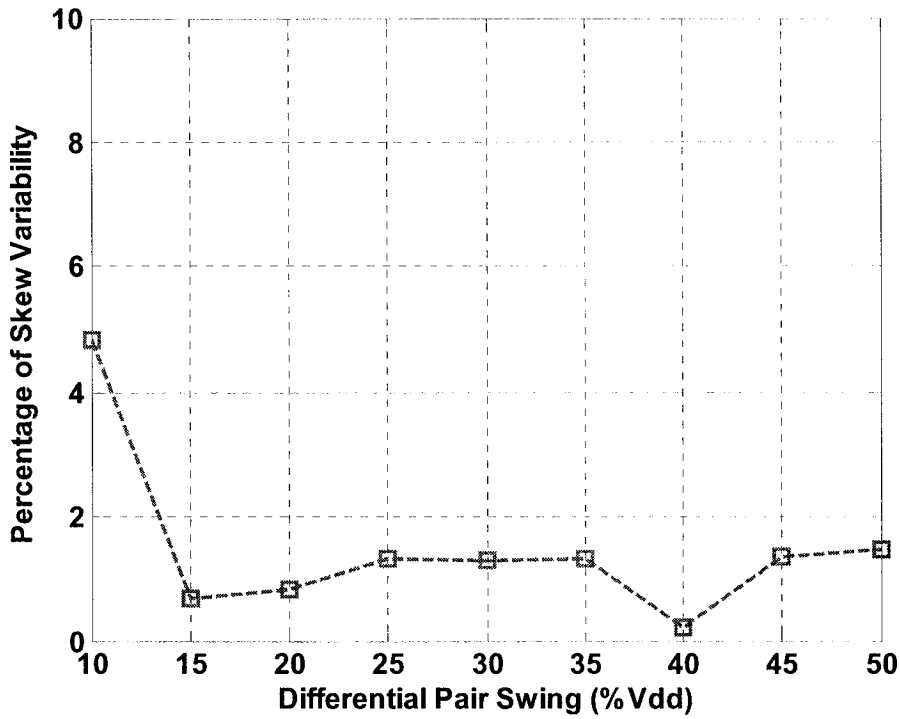

Figure 5-8, Simulation results showing variations in skew for swing scaled DCDN in presence of an external aggressor

Figure 5-8 shows, the robustness of the DCDN in the presence of external aggressors. It can be seen that scaling the differential swing is not as sensitive as it is to power supply perturbations. Simulation results show 1% variability on average for different swings except for small swing (180mV) due to the existence of crosstalk, the clock network performance is slightly influenced. This is due to change in the common-mode operation of differential buffers.

In this part, the effect of differential voltage scaling was investigated. In the next part we propose a system methodology to design an efficient clock distribution network.

5.2 Supply Voltage Scaling

In the previous section, the effect of differential swing scaling on the performance of the clock network was explored: First, we observed that the reduction of differential swing highly improves the power consumption. For differential swings smaller than 25% of V_{dd} the power consumption becomes less than half of the clock network with $50\%V_{dd}$ voltage swings. Second, as Figure 5-6 suggests, due to the fluctuations of common-mode voltage in clock network, the voltage swing of $25\%V_{dd}$ (450mV) shows the least variations against supply variations.

Taking the above considerations into account, we consider a design point for the differential swing of $20\%V_{dd}$ (450mV) and reduce the supply voltage to the point where we reach the same power consumption for the single-node and differential clock networks. HSPICE simulations demonstrate that for the supply voltage 1.4V and differential swing 450mV we obtain the same power consumption for the differential clock network. Yet, as it could be observed from Figure 5-9, the variation of clock skew is still less than that of single-node clock distribution network.

Another interesting point during supply scaling in DCDN observed is: simulation results show **negligible signal latency difference.** This can be justified according to Equation 3.11. As current tail is lowered to achieve lower differential swing; the necessary differential voltage needed for the differential buffer to switch is also decreased. This enables the differential buffer to operate/switch faster than in the case when greater supply voltage with greater differential swing is used.

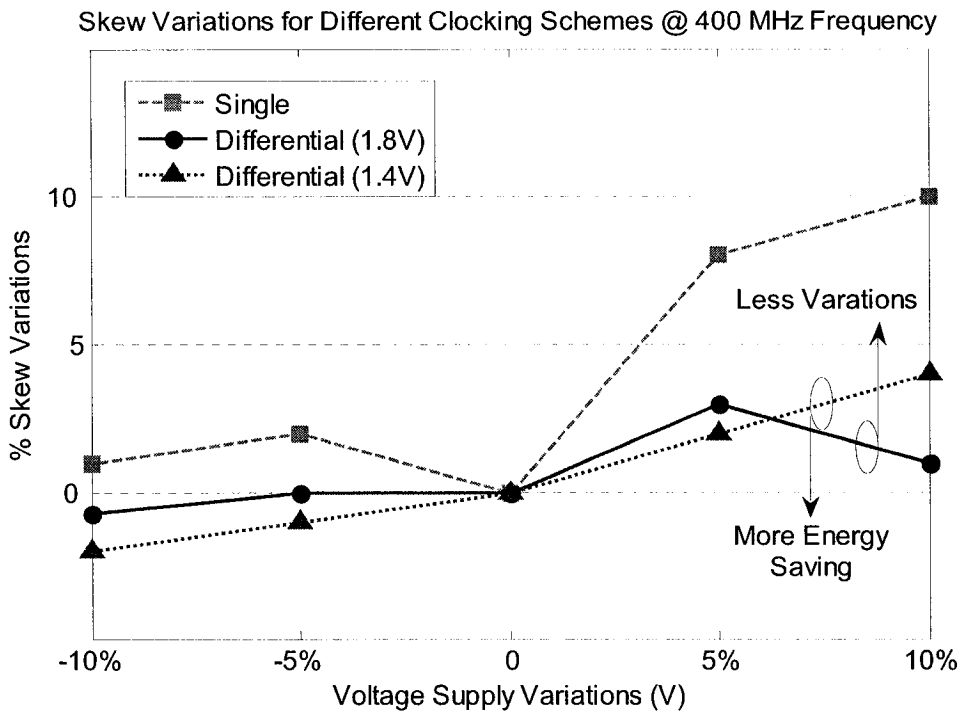

Figure 5-9, HSPICE simulation show less variations in DCDN compared to Single-node CDN for equal power consumption (V_{dd}: 1.4V)

5.3 Summary

In the first part of this chapter, we reached the conclusion that differential swing of $25\%V_{dd}$ has the performance as far as clock network criteria are concerned. Yet, the DCDN designed based on this method consumed almost 30% more power. In the second part, we kept the same differential voltage swing and reduced the supply voltage to the point that both the DCDN and Single-node CDN consume the same amount of power, while DCDN shows less variation in terms of skew.

6. Conclusions & Future Work

In this work, the design and analysis of on-chip Differential Clock Distribution Networks (DCDNs) was investigated. Initially two problems associated with the design of DCDN were looked at: First, there is no available model for zero skew routing of DCDNs. Second, DCDNs have higher power consumption than single-node CDNs. The following solutions were proposed to address the aforementioned design problems:

1. For Zero Skew routing, a line equivalent delay model is suggested by which it is possible to route DCDNs with minimum (Zero) skew. On average, 97% skew reduction was obtained utilizing this model compared to the classic Elmore model.

2. In order to overcome the high power consumption of DCDNs, initially a circuit configuration is proposed by which it is possible to reduce the differential voltage swings (down to 10% of V_{dd}) which reduces the power significantly (30% more than single-node CDN). Later, by scaling the supply voltage of the system from 1.8V to 1.4V, we reached a design point where the DCDN consumes the same power as its single-node CDN counterpart but has less variation (in terms of skew). This comes at the expense of delay and reduced voltage swing.

Beside the proposed solutions to the aforementioned design problems, new configurations for differential buffers based on Dynamic Threshold (DT) transistors are proposed as another contribution of this work. It is shown that in sub 1-V supply voltages, they outperform the conventional buffers with 25% delay reduction.

Conclusions regarding the utilization of DCDN in high-performance Systems-On-a-Chip can be summarized as: due to the drastic increase in system complexity, the use of Three Dimensional (3-D) ICs is becoming a promising design method to overcome the performance degradation in on-chip communications due to interconnect limitations. Doubling routing wires in interlayer interconnects will not be a reasonable design methodology, thus the use of differential clocking is not a rational design technique to be used entirely in CDN. Due to the advantage of DCDN, seemingly the best design method can be anticipated as utilizing DCDN in the global level of CDN to minimize clock uncertainty.

Recommendations for future work with respect to Differential Clock Distribution Network (DCDN) can be summarized as:

1. Modeling random skew, jitter and delay variations and the relations between them.

2. An accurate delay model of differential buffers for zero skew routing of buffered DCDN.

3. Investigation of low voltage differential swings instead of high voltage differential voltage swings ($[0, V_{swing}]$ instead of $[V_{dd}-V_{swing}, V_{swing}]$).

4. Differential buffer configuration based on dual threshold (or Multiple threshold MTCMOS) and its application to DCDN design.

5. Designing a clock distribution network for a high-performance 3-D IC in which DCDN is used entirely or just in global level.

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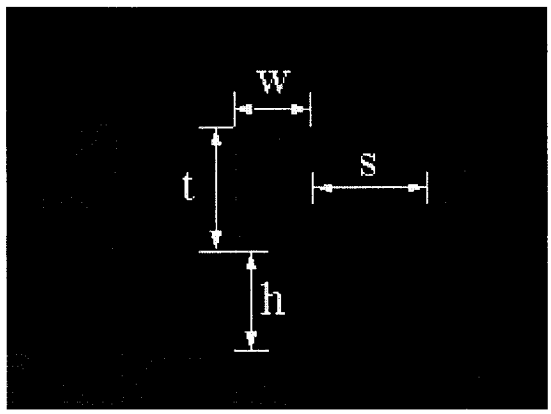
Appendix A

0.18um Interconnect Technology Parameters

In our design project, we used Berkeley Predictive Technology Model from [37] for our design and simulations. The structure for interconnect as given by the technology is given in the following figure:



Appendix A-1, Interconnect structure considered in the design project from [37]

The 0.18 Technology structure parameters are tabulated in table A-1. As it is also drawn in the above figure, Width (w) refers to the width of the interconnect wire, Space (s) refers to the spacing between the adjacent wires, Height (h) refers to the distance of the wire to the ground plane, Thickness (t) refers to the thickness of the wire and K_{ILD} is the insulation coefficient of the insulating material.

Table Appendix A- 1, 0.18um Technology structure parameters

Width (w)	Space (s)	Height (h)	Thickness (t)	K_{ILD}
0.80 um	0.80 um	0.65 um	1.25	3.5

Finally according to [37] and the aforementioned interconnect structure, the .18um interconnect parameters become the following:

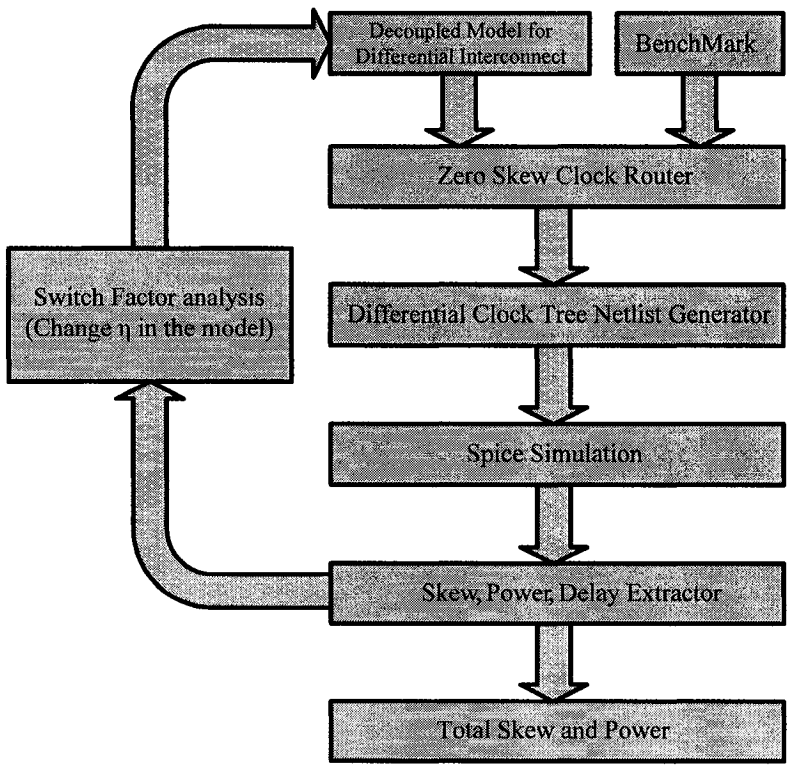
Table Appendix A- 2, 0.18um Technology parameters

Structure	R(Ω/um)	C_G(F/um)	C_C(F/um)
Single Spaced (SS)	0.022	0.08e-15	0.08e-15
Double Spaced (DS)	0.022	0.10e-15	0.04e-15

Appendix B

CAD System Model

The design project mainly relies on a CAD system. In other words a CAD system was developed to design and synthesis the differential clock distribution network. The proposed CAD system consists of various sections as given in Figure B-1.



Appendix B-1, CAD based system model for differential clock tree design

The CAD system functions as follows:

1) Initially the benchmark is chosen for which the differential clock network should be created. Then the decoupled interconnect model is used and is jointly applied to the package created in C++. Then the decoupled differential clock network, a single-node clock network based on effective capacitance is created.

2) Next the routed clock network is utilized by netlist generator implemented by PERL language. In this part the SPICE netlist for differential clock tree is created.

3) Subsequently, SPICE simulations are performed on the differential clock network netlist created in the previous step.

4) Later, the SPICE results such as delay of the sink nodes and power consumption are extracted by a CAD tool created in PERL as well. In the final step the total skew for the network is calculated by the CAD tool.

For the case of switch factor analysis, the coupling coefficient η in the decoupled model is changed and the whole process is repeated the same way and according to the skew results extracted in the last section, the effect of η on differential signal propagation is analyzed.