Comparison of Synchronization Techniques for Generation of Firing Pulses for a HVDC Converter

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ABSTRACT

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This study focuses on the special requirement of synchronization of firing pulses for a power converter operating with a weak AC system. The challenge for the synchronization technique is in providing a fast dynamic response while maintaining a high accuracy of equi-distant pulse generation during steady state operation and maintaining stability within a range of system frequency and phase deviations.

The phase locked loop (PLL) technique plays an important role in providing a reference signal synchronized with the AC system. With the development of new PLL techniques, it is possible to improve the dynamic response, robustness, harmonic rejection and stability of the converter system. These new techniques consist of an enhanced PLL and 3-phase PLL based on the DQZ method. A variety of these new synchronization techniques are investigated and compared with a conventional PLL in this thesis.

The test system used is a 12-pulse HVDC converter operating with a weak AC system that is modeled with the EMTP RV simulation program.

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I wish to give my special thanks to my wife for her continuous love and support, without it I would never be able to achieve my goals. I would also like to thank my parents for their everlasting love and constant encouragement.

This thesis is dedicated to my wife Mrs. Huichun Wang

and my daughter Nicole Leng.

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LIST OF ABBREVIATIONS

AC	Alternative Current
CPLL	Conventional Phase Locked Loop
DQPLL	DQ Phase Locked Loop
EPLL	Enhanced Phase Locked Loop
FACTS	Flexible AC Transmission System
GFU	Gate Firing Unit
HVDC	High Voltage Direct Current
IEEE	Institute of Electrical and Electronic Engineers
LF	Loop Filter
LPLL	Linear Phase Locked Loop
PD	Phase Detector
PI	Proportional and Integral
PLL	Phase Locked Loop
SCR	Short Circuit Ratio
SPLL	Software Phase Locked Loop
SNR	Signal-to-Noise Ratio
VCO	Voltage Controlled Oscillator
VFA	Variable Frequency Average

CHAPTER 1

INTRODUCTION

1.1 Introduction

High Voltage Direct Current (HVDC) Transmission was first applied in the under-sea cable interconnections of Gotland (1954) and Sardinia (1967) [1]. The first 25 years of HVDC transmission were implemented with HVDC converters using mercury arc valves till the mid-1970s. After that period HVDC transmission has been implemented with line-commutated converters using thyristor valves.

In Comparison with an AC transmission line, a HVDC line longer than the breakeven distance of about 300 km, results in a lower cost of the infra-structure (i.e. towers, conductors and insulators) and reducing power losses for a given power level. Due to its fast controllability, HVDC system has full control over transmitted power, and an ability to enhance transient and dynamic stability in associated AC networks.

A HVDC converter requires firing pulses for its valves. These firing pulses need to be synchronized to the AC system voltage for the proper functioning of the converter. Moreover these firing pulses are required to be equi-distant to avoid abnormal harmonics generation during steady state operation. For a strong AC system, synchronization

directly with the AC system voltages is easily achieved. However, for a weak AC system which is vulnerable to system disturbances and waveform pollution, special synchronization techniques are required to avoid harmonic instability in steady state operation. Synchronization techniques play an important role in firing pulses generation of a HVDC converter. Such techniques are employed to provide a synchronizing reference signal instead of the weak AC system.

Synchronization techniques, employing Phase locked Loop (PLL) techniques, have been used over the past decades for a wide range of applications in the fields of communications, control systems and power electronics. The basic PLL concept was originally published by de Bellescize in 1932 [2]. The techniques were mainly used for synchronous reception of radio signals. Widespread use of the PLLs began with TV receivers during the 1940s with integrated circuits (IC) in 1960s, large-scale integrators in 1970s, and with dramatic advances in IC technology in 1990s. After that some special applications on PLL technology were developed with the application of nonlinear and fuzzy control theory. PLL technology has enabled modern electronic systems to improve performance and is widely used with Flexible AC Transmission System (FACTS) and HVDC systems [3].

Firing pulses generation depends on the extraction of the phase and frequency of the AC system voltage waveform. The synchronous operation of the converter directly influences the quality, stability and reliability of the output of HVDC.

1.2 HVDC system overview

In Comparison with an AC transmission system, a HVDC transmission system has some obvious advantages:

(a) DC transmission system results in lower losses and costs than equivalent AC lines.

(b) DC transmission via cable is practical over long distances. Such a restriction exists with AC.

(c) A DC system constitutes an asynchronous interconnection and does not raise the fault level appreciably.

(d) The power flow in a DC link can be used to improve AC system stability of attached systems.

(e) DC stations can be justified for the interconnection of AC systems of different frequencies or different control philosophies.

However the HVDC systems also have their disadvantages:

(a) Converters generate harmonics, and therefore require expensive filters.

(b) Lack of low cost HVDC breakers hampers multi-terminal or network operation.

(c) The terminal costs and losses are higher

A typical HVDC system, including the control system, linking two AC systems is shown in Fig.1.1. Two subsystems are included in this system, these are: (a) power circuit system including AC power system and DC power system; (b) HVDC control system including local control system master control system and dispatch center.

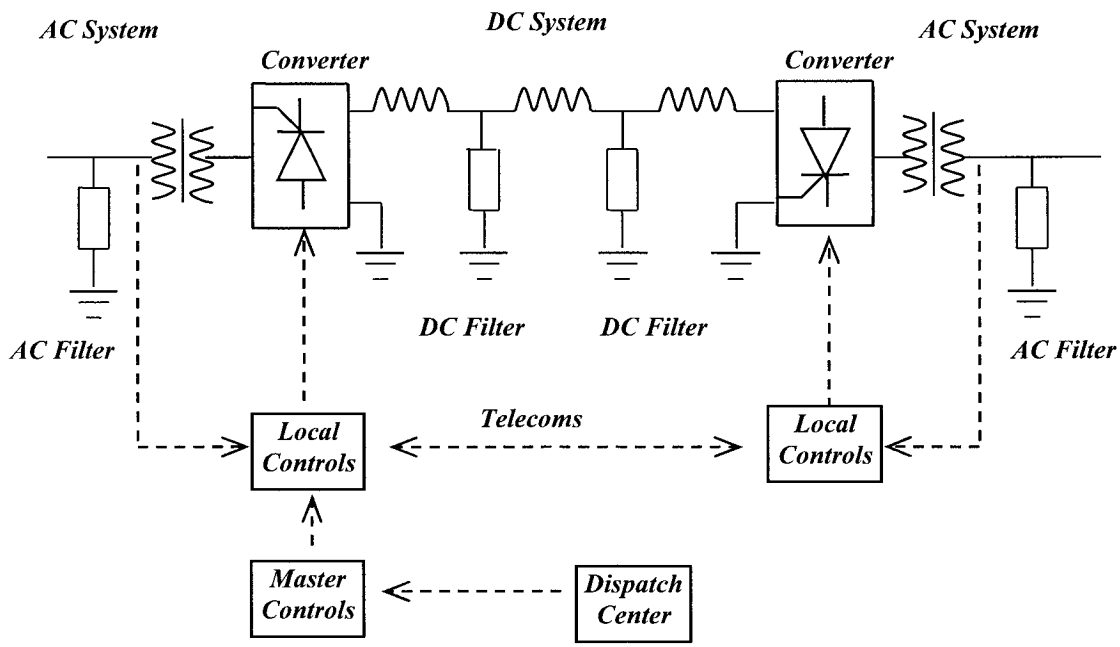

Figure 1.1 Typical HVDC systems

The AC portion of a power circuit system basically includes the AC filter and AC isolation transformer. The DC portion includes the converters and DC filter. The control subsystem will be responsible for generating firing pulses, control power flow between the terminals, protect the equipment against the current/voltage stresses caused by faults and stabilize the AC system against any operational mode of the DC link. A centralized

dispatch centre will send a power order to one of the terminals (local control unit) which will act as a Master controller and has the responsibility to coordinate the control functions of the DC link.

A local controller, shown in Figure 1.2, basically consists of 4 subunits: Measurement Unit, PLL Unit, Controller Unit and Gate Firing Unit (GFU). The Measurement Unit is one of two input units. The other one is the Controller Unit which receives the current order from the outside Master Controller and outputs a control signal which is the power control order. The measurement unit measures and transfers the power system voltage, current to a control signal which can be processed by the PLL. The PLL receives the information form both the Measurement and Control Units. The special application of PLL in a HVDC system is that the PLL will play a role to decouple the dependency on the AC main circuit of a weak system besides synchronizing the communication voltage. The output of a PLL is a modulated train of pulses which will finally serve the GFU and generate the firing pulses required by the valves of the converter.

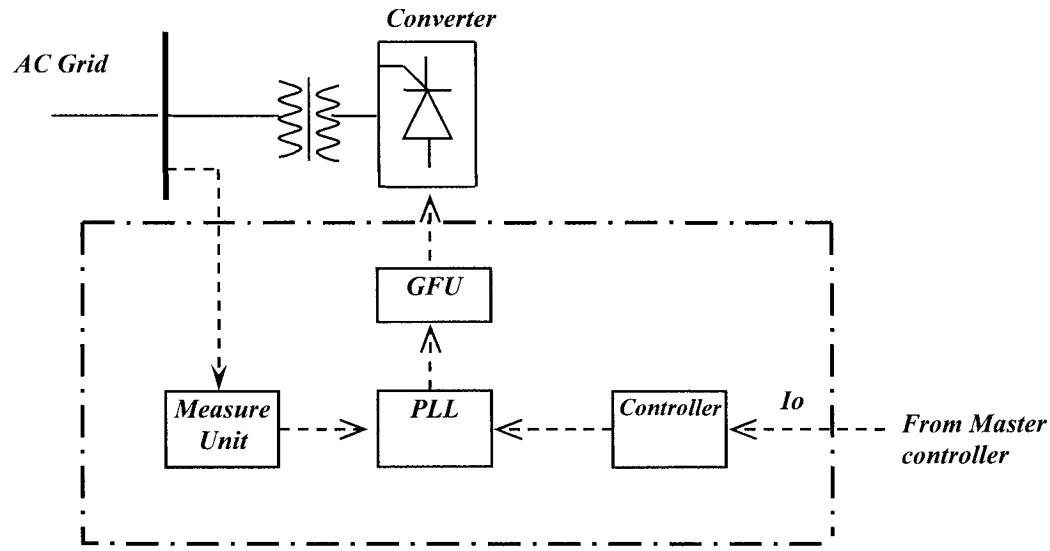

Figure 1.2 Local controls

1.3 Literature review

In this literature review, three aspects related to this thesis are presented, i.e.

(1) HVDC system

(2) Grid control unit

(3) PLL

HVDC system

Four books [1, 5, 6 and 7] supplied details about HVDC transmission systems from 1971 to 2004. The general topics discussed in these books covered the areas related to converter techniques, grid control techniques, operation and protection techniques, filters and harmonics.

Grid control unit

Two types of gate firing unit used in HVDC control systems are introduced [8]. The older obsolete method was called *Individual Phase Pulse Firing* Control. The modern method is called the *Equidistant Pulse Firing* Control.

In the Individual Phase Firing Control Unit, firing pulses of the valves are directly derived from the zero crossover points of the AC commutation voltage. The disadvantage of this unit is that it generates non-characteristic harmonics which can cause harmonic instability problems particularly when operating with weak AC systems.

The second method is the Equidistant Pulse Firing Control Unit. In this type of unit, pulses are decoupled from the AC commutation voltage and are instead related to a pure sinusoidal waveform generated by a synchronous Voltage Controlled Oscillator (VCO). The firing pulses generated by such a unit are equidistant during steady state operation. In the control circuit, a DC input signal (feedback error signal) to the VCO results in a frequency change of the VCO. And the pulses frequency is directly proportional to the DC control voltage. A ring counter is used to separate the pulse train into n sets of pulses for an n-pulse converter.

Three different operation modes are introduced in [3; 9]: (1) operation model on constant current with the converter operating either as a rectifier or as an inverter; (2) operation model on minimum firing angle as rectifier; (3) operation model on minimum

extinction angle as inverter. The rectifier normally operates on constant current control and the inverter on minimum extinction angle control, which gives the smallest consumption of reactive power in the inverter. The constant current control in the rectifier operation mode is exactly the same as current control in the inverter operation mode. The constant current control in the inverter operation mode only operates when the system is operated on a transition status. The operation characteristics of HVDC system are shown in Figure 1.3.

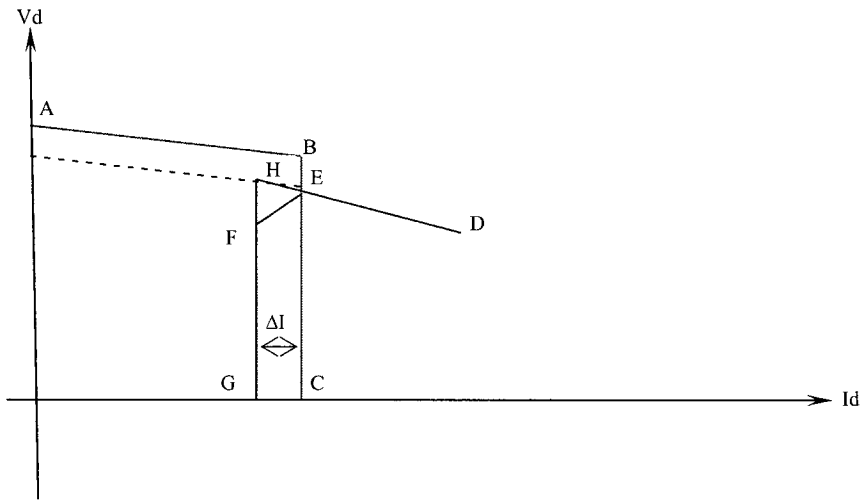

Figure.1.3 Operation characteristics for HVDC transmission

1) Rectifier-minimum delay angle control ------ AB
2) Rectifier-constant current control----- BC
3) Inverter-minimum extinction angle control ------- ED
4) Inverter-constant current control -------- FG
5) Stable operation point --------- E
6) Unstable operation point ------- H
7) Current order margin -------- ΔI

8) Inverter transfer control -------- EF (to avoid unstable operation point)

In a Constant Current Control model, a DC output current of the converter is maintained constant at the preset value, called I_{order}. A feedback control loop is designed to achieve this function. The feedback error is the amplified difference between the current reference signal (I_{order}) and the measured current. In steady state operation when the rectifier operates on the constant current mode, the inverter should operate on the minimum extinction angle operation mode. Then the HVDC system operates at a stable operation point.

In an Extinction Angle Control mode at the inverter, the system steady state operation holds a smallest gamma angle (extinction angle) at a predetermined value by the closed-loop control. In [3] a sampled-time gamma measurement with error correction feedback is used. The difference between two papers above is that [9] used a predicted gamma control rather than feedback gamma control. This means an advantage compared to a pure feedback extinction angle control system, where it is necessary to wait for a change in the extinction angle from the disturbance before any action is taken to restore the angle [9]. But this good prediction only is given at a low direct current and with sinusoidal commutation voltage (steady state and no distortion). Otherwise it needs to design a feedback error correction circuit. By using this feedback error correction, the prediction method loses its advantage. A Symmetrizer has been designed to keep following valves firing equidistantly when one valve has fired on minimum margin condition (extinction angle is adequate for valve deionization plus a margin to prevent

commutation failures for minor ac system transients). And it also prevents retarded but not advance firing. Compared with an individual phase control system, the equidistant firing system gives a lower direct voltage. Another disadvantage is that its half period measurement suffers some problems when 2nd order harmonics exist.

In the minimum firing angle operation mode at the rectifier, firing pulses must be prevented until the commutation voltage has reached a defined low value. This function is obtained by connecting an AND gate at the output of the level detector.

Phase-Locked Loop (PLL) Technology

PLL is an old technology dating from the 1930s. It has been used over the past decades for a wide range of applications in the fields of communications, instrumentation, control systems, multimedia apparatus and power electronics.

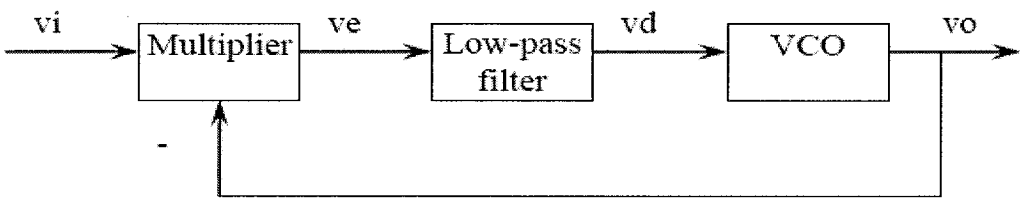

Figure.1.4 Block diagram of PLL

[2] is a tutorial paper where five special applications of PLL are presented. The first paper is a *tutorial paper* from Hsieh and Hung [10] that gives an overview of basic PLL concepts, operation, mathematical models and applications. The second paper, by

Kobayashi et al. [11; 12], presents recent developments in a *fast digital PLL*. The third paper, by Margaris and Mastorocostas [13], investigates the *synchronization* of a nonlinear analog PLL where nonlinear model for the VCO is proposed. The fourth paper, which is really in two parts, by Lai et al. [14; 15] incorporates *fuzzy* logic control in a phased-locked AC induction *motor speed drive*. The fifth paper by Takano [16] proposes an accurate and high-performance speed control system for motors.

In [8], the conventional PLL technology and three-phase DQ PLL is presented for use with applications on power electronics.

Conventional PLL: This type of PLL consists of a phase detector (modifier), low pass filter and a VCO. The low pass filter is designed to filter out a second harmonic AC component. The cut-off frequency is selected around 20 percent of the second harmonic AC component. i.e. 20% x 100 Hz = 20 Hz.

DQ PLL: DQ PLL operates on a three-phase basis, where the three-phase commutation voltages are transformed into DQ axis voltages. The other components are a PI controller and VCO. Comparing these two types of PLL, the Conventional PLL needs a low pass filter to remove the second harmonic AC component; the filter is a lagging phase element. The DQZ version, on the other hand, does not need this. Thus, the DQZ PLL can theoretically achieve a much faster dynamic response.

[10] is a tutorial paper about PLL. This paper introduces the basic PLL techniques including theory, phase detector, loop filter and VCO characteristics. Some important equations and interesting conclusions are obtained.

$$Vc = \frac{\omega_i - \omega_o}{K_v} \qquad (1.1)$$

$$\omega_{inst} = \omega_o + K_v V_c \qquad (1.2)$$

$$\phi_o = \theta_i - \cos^{-1}\left(\frac{\omega_i - \omega_o}{K_d K_v}\right) \qquad (1.3)$$

The equations (1.1) and (1.2) show that it is the DC signal v_c that changes the VCO frequency from its center value ω_0 towards the input signal ω_1. And equation (1.3) gives a relationship between input (phase, angular speed) and output (phase, angular speed). Meanwhile this equation gives the reason why the phase difference is 90^o when the loop is locked and ω_i-ω_o is much lower than K_dK_v . Lock-in range is an important parameter of the PLL. This paper gives some basic concepts about lock-in range:

- When the difference $|\omega_i - \omega_o|$ exceeds the loop gain K in a sinusoidal PD, phase lock can no longer exist.
- The higher order loop has the same lock-in range as the equivalent-gain first-order loop.
- The lock-in limit of a first-order loop is equal to the loop gain.
- A large value of K_d is usually required for achieving a good performance of the loop.

Papers [4, 17, 18,19 and 20] are a series of papers that investigate a new PLL technique named Enhanced Phase-Locked Loop System (EPLL). This technique gives a

new phase detection method which applies a total harmonics generator to produce an error signal proportional to the phase difference. The structure of the loop filter remains as simple as a gain which reduces the overall complexity of the system. Some advantages of the EPLL are as follows: (a) the output of EPLL is locked in both phase and amplitude, (b) the input and output phase angles are not only locked but also equal, (c) EPLL directly provides the estimated information of the amplitude and the phase of the fundamental component of the input signal in addition to the synchronization of the output, (d) EPLL structure is very robust with respect to whatever internal or outside structure since the loop gain is relatively independent on the input or the change of the small loop parameters. Based on this new technique, some new applications in the power field are developed such as power signal processing, nonlinear / active filter and peak detector technique.

[21] gives another idea to improve the PLL performance. In this paper, the information of input, frequency, phase, and amplitude are utilized as much as possible. The filter is taken out of the main control loop and replaced by new harmonics cancellation block to speed up the system transient response. In addition, a digital signal processing technique VFA (variable frequency average) is used to remove the AC harmonics. Due to the complete information utilization this structure of PLL has a fast response and a robust performance.

An application of the PLL technique in a HVDC converter was first introduced in papers [3; 9]. PLL technique gives a fresh method which can generate equal distant firing pulses and can remove the dependency on the AC waveform.

In the steady state constant current control operation model, the VCO center operation frequency is adjusted to 6 times AC power supply frequency (measured). Both feedback loop error and center operation frequency control the frequency of VCO. After the VCO, a ring counter is used to separate the pulse train. There are two ways to control the voltage oscillator; one is to change ramp wave slope while keeping the reset-voltage constant; another way is to change reset-voltage. In steady state, the firing pulses are equidistant (60 electrical degrees apart). If there is a frequency change, the system will settle down at the new firing angle with the same VCO frequency. Moreover, if there is a DC load change, the system will settle down at a new frequency (6f) with the same firing angle and DC current. This method can easily follow the AC system frequency over the normal range of variation with a fast response.

In a steady state operation of an extinction angle mode (gamma control), the response is fast due to the combination of short gamma measurement period (every 60 degrees), error correction feedback, and the lack of smoothing time constant lags either in the feedbacks or control system filters.

In conclusion, when comparing a PLL-based pulse firing generation of HVDC with other techniques, the PLL-based system is not directly related to the AC line voltage.

In steady state, its pulses are at an accurate spacing of 60 degrees, independent of preset adjustments even in the presence of considerable amounts of asymmetric distortion in the AC line voltage. It does not require a control filter with its associated disadvantages (delay stability and phase shift) and it is practically free from harmonic instability since the regularity of pulse spacing is not affected by even considerable AC line voltage distortion including a negative-sequence fundamental component. For the same reason, the impact of DC components and hence saturation effects in transformers are very small. Because of the freedom from harmonic instability and very low abnormal harmonic generation, this technique constitutes a substantial economy due to the high cost of power filters. For a converter with a relatively weak AC system, the PLL based system has a great advantage, both for steady state and transient conditions.

Finally, three topics have been reviewed as they impact on this thesis in this chapter i.e. HVDC system, grid control unit and PLL technique. The following chapters will focus on the detailed design, simulation and analysis of the above three topics.

CHAPTER 2

PROBLEM DEFINITION

In a HVDC system, a bad AC power quality (like distorted waveform or unstable frequency, phase and amplitude) usually result in operation fault in rectifier and inverter. The harmonic current injection into the utility grid caused by operation fault, unstable grid control or unreliable firing generation will make AC power quality worse. For inverter operation, the unreliable and inaccurate operation at minimum extinction angle control mode will result in commutation failure in the worst situation and increase operation cost (reactive power consumption). The improvement work can base on three important units of HVDC: (1) HVDC power circuit unit which includes converter, AC and DC transmission line, AC filter and reactive power compensation equipment; (2) grid control unit which includes rectifier and inverter operation and control; and (3) firing pulses generation unit which provides firing pulses signal to two terminals of HVDC system.

2.1 HVDC transmission system

A HVDC power circuit usually consists of an isolation transformer, converter bridges, AC and DC filters and reactive power compensation equipment. Some improvement of power circuit design can limit the effect of bad power quality, such as: (1) optimize the design of AC and DC power filter; (2) keep the electrical equipments/ power

circuit parameters balance; (3) limit the fault current and keep equipments protected; (4) reduce the reactive power consumption and keep reactive power balance; (5) provide a good arrangement of valves to cancel characteristic harmonics generation. The improvement of filter design, converter design, snubber design, and reactive power compensation equipment design can greatly increase the performance of the system.

2.2. Grid control unit

Grid control unit is to be used to maintain HVDC system at a stable operation state, restrain the harmonics generation, achieve a reliable operation switching and give a protection during system fault caused by switching operations or power line faults like short circuits. A good grid control unit in HVDC system can limit the effect caused by bad power quality to minimum. Then the design of grid control should aid in the follows:

(1) Harmonics stable in the steady state under bad AC power quality.

(2) Flexible control of power flow and frequency.

(3) Good quality of power

(4) System stability and reliability

(5) Operating the system under least power loss conditions, or having a power factor as high as possible.

(6) Good protection to electrical equipments for HVDC system.

2.3. PLL technology on firing pulse generation unit of HVDC system

A HVDC converter needs to synchronize the firing valves with the waveform of the attached AC system sinusoidal waveform to provide the conversion of AC – DC power or vice versa. Should the AC waveform be distorted due to a weak AC system suffering from harmonic pollution and other disturbances, then the converter cannot function in an orderly and stable manner. It is therefore, primordial that.

First, a decoupled and stable synchronizing voltage is utilized for generating the firing pulses for the converter. This synchronizing voltage must be in phase with the commutation voltage of the converter.

Second, the firing pulses must be equi-distant such that the generation of non-characteristic harmonics is minimized. The generation of non-characteristic harmonics caused by non-equi-distant firing pulses is harmful to equipment such as transformers etc. and must be minimized as AC and DC filters are not available to remove these harmonics. The characteristic harmonics (i.e. 5, 7, 11, 13 etc. on the AC side and 6, 12 etc on the DC side) usually have AC – DC filters to remove them.

Third, the firing pulses for the converter must be limited in steady state operation, within a range from alpha-min (around 6 degrees) to alpha-max (around 145 degrees). The alpha-min limit ensures that a minimum positive voltage exists across a valve before turn-on; this is a protective requirement for the valve to avoid firing any valve until its anode voltage is appreciably positive, to avoid the risk of any anode misfiring, and consequently giving over current in others. The alpha-max limit ensures that the inverter

mode of operation has sufficient margin angle (gamma plus overlap angle) to commutate the valve. Extinction angle (gamma) is adequate for valve deionization plus a margin to prevent commutation failures for minor ac system transients.

Fourth, a satisfactory response to transient disturbances must be obtained. Since the AC-DC systems are subjected to transient disturbances, the synchronizing voltage must be capable of locking to the commutation voltage in a safe and rapid manner.

The above requirements impose the usage of a PLL technology to generate the decoupled and stable synchronizing voltage to be utilized for generating the firing pulses for the converter.

In a HVDC system pulse firing of valves usually will inject normal and abnormal harmonics. Some lower harmonics are difficult to remove. A lower harmonics AC filter is expensive. So the design of pulse firing generation is to reduce the abnormal harmonics injection into main system. The PLL technology can be used to improve the design of pulse firing generation. The accuracy, synchronism and equi-distant pulse generation are the desired feature of the pulse firing unit. Usually a synchronous reference control signal (frequency and phase) is required in pulse firing unit. That process (called commutation voltage extraction) is the basis of everything. Thus the commutation voltage extraction from AC system even in the presence of considerable amounts of asymmetry distortion in the AC line voltage appears extra important. The PLL technology is utilized to extract

the fundamental component. Except for the requirements of accuracy and synchronism of a fast transient response, wider lock-in range and good stability are also required.

A conventional PLL has a simple structure comprising a voltage controlled oscillator (VCO), phase detector (PD) and loop filter (LF). Its sinusoidal phase detector operates as a multiplier. Generally this kind of PLL can work well under conditions that the input has a similar sinusoidal waveform. Its PD gain depends on the amplitude of input signals, and it is not a property of the circuit alone. That will result in a changeable lock-in range of PLL, and the structure will not be robust. Under certain conditions, the PLL loop is in lock but the phase is not equal. Since the presence of the loop filter the PLL has a phase/time lagging characteristic, it will slow the dynamic response of the system. Some methods have been investigated to improve the PLL's property such as utility of PI controller and nonlinear phase detector.

It is important that some trade-off is made between accuracy and faster dynamic response. The HVDC control system requires the PLL speed is as fast as possible, however, this must be under the precondition of satisfying the accuracy requirement. Otherwise it does not make sense.

This thesis will look at PLL technology to meet the four requirements stated above for generating the firing pulses for the converter.

CHAPTER 3

PHASE LOCKED LOOP

3.1. Introduction

The design, analysis and simulation of a HVDC converter system and its related controller need knowledge of mathematics, power electronics, digital signal processing and control theory. In this chapter, the PLL design, including the control loop design and filter design, are introduced by using time domain and frequency domain analysis techniques such as Bode plots, transfer functions, root locus and linearization.

Two softwares, EMTP RV and MATLAB, will be used as simulation and analysis tools for the study of the combined converter and control systems.

3.2. PLL design

A PLL is basically an oscillator whose frequency is locked onto some input frequency signal. This is done with a negative feedback control loop which is composed of an error generator, some loop filters and an oscillator controlled by the error signal. A PLL design basically is to develop and analyse such a control loop through the mathematical analysis and simulation.

In this thesis, old and new types of PLL will be explored. In order to generate valve firing signals for the HVDC converter that are synchronized to the AC commutation voltage, PLL technology will be utilized to produce a reference signal, which is in synchronism with the fundamental frequency component of the AC commutation voltage. This reference signal will be free from harmonics and distortion of any kind, even when it is functioning with a weak AC system.

Some desired properties of a PLL are a fast synchronizing ability, robustness to varying input magnitudes (within a certain tolerance band), robustness to varying input frequency (within a certain tolerance band) and zero steady state error.

3.2.1 Basic concept of PLL

A PLL is a circuit capable of synchronizing a clean output signal with a distorted input signal which may be varying (within certain limits) in amplitude, frequency and in phase [2]. The functional block diagram of a PLL is shown in Figure 3.1, which consists of a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO). The phase detector compares the phase between input and output signals, and develops a signal proportional to the phase difference. This signal is applied as a control voltage to the VCO to adjust the oscillator frequency. Through negative feedback, the PLL causes the input signal frequency to be equal to the output signal frequency, and the phase error is kept below some set value. Thus, both the phase and frequency of the oscillator output

signal are "locked" to the phase and the frequency of the input signal. In this thesis, the focus will be on the linear PLL design only.

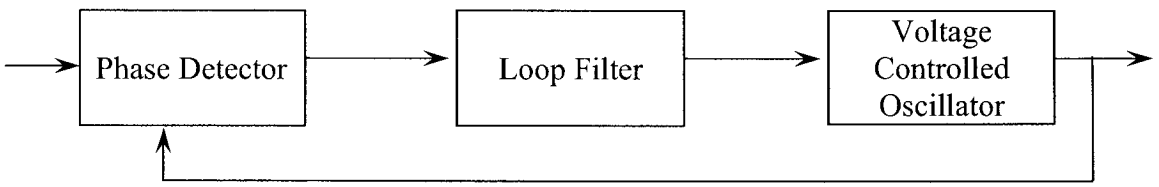

Figure 3.1 Block diagram of typical PLL

In the linear PLL, a four-quadrant multiplier is used as the phase detector. In most cases, the input signal is a sinusoidal wave, and the output of the phase detector consists of a DC component (proportional to the phase error θ) and AC components (having frequencies of $2\omega_1$ $4\omega_1$ ....). These higher frequencies are unwanted signals, and they will be filtered out by a low-pass filter. In the LPLL, the phase detector block represents a block having a gain K_d.

In a linear PLL design, the following topics are of concern:

(1) Order of the loop filter

Although a higher-order loop filter may offer better noise immunization, it is much more difficult to obtain a stable higher-order system than a lower-order one.

(2) Locked state / unlocked state of LPLL

A simplified linear model is best suited to explain the tracking performance of the PLL. This is the case if it is assumed that the PLL is considered initially locked (i.e. has small phase errors). If the PLL is initially unlocked, the linear model is no longer valid, because a large phase error in the output signal of the phase detector is not proportional to the phase error. But because the *sine* function cannot exceed unity, the maximum rate of change of the reference frequency that does not cause lock-out is $\Delta\omega_{\max} = \omega_n^2$ [23]. This result has two consequences (for the sine signal):

a) If the reference frequency is swept at a rate larger than ω_n^2 the system will unlock.

b) If the system is initially unlocked, it cannot become locked if the reference frequency is simultaneously swept at a rate lager than ω_n^2. The more practical design limit for $\Delta\omega_{\max}$ is considered to be

$$\Delta\omega_{\max} = \omega_n^2 / 2$$

Three conditions are necessary if a PLL system is to maintain phase tracking:

a) The angular frequency of the reference signal must be within the hold range (static limit of stability).

b) The maximum frequency step applied to the reference input of a PLL must be smaller than the pull-out range (dynamic limit of stability, the frequency offset step that causes the LPLL to unlock).

(3) Key parameters of LPLL

There are some key parameters that need specifying. These parameters are the basis of every LPLL design.

- The center frequency of the PLL – angular frequency of the VCO at error = 0.

- The natural frequency of the PLL – the natural frequency of the PLL system.
- The *hold range*-This is the frequency range in which an LPLL can statically maintain phase tracking.
- The *pull-out range* – This is the dynamic limit for stable operation of PLL. If tracking is lost within this range, a LPLLL normally will lock again, but this process can be slow if it is a pull-in process.
- The *pull-in range* – This is the range within which a LPLL will always become locked, but the process can be rather slow.
- The *lock-ran*ge – This is the frequency range within which a PLL locks within one single-beat note between reference frequency and out put frequency. Normally the operating –frequency range of a LPLL is restricted to the lock range.
- The noise bandwidth B_L.
- The pre-filter bandwidth – bandwidth of the pre-filter (or the input signal source) Bi.
- The signal-to-noise ratio of the loop. $(SNR)_L$.
- The rate of change of frequency offset – maximum allowable rate of change of (angular) reference frequency. $\Delta\omega$

(4) Noise of LPLL

a) Stable operation of the LPLL is possible if $(SNR)_L$ is approximately 4.

b) $(SNR)_L$ is calculated from

$$(SNR)_L = \frac{P_s}{P_n} \cdot \frac{B_i}{2B_L}$$

c) The noise bandwidth B_L is a function of ω_n and ζ.

d) The average time interval T_{av} between two unlocking events gets longer as $(SNR)_L$ increases.

e) The rate of change of the reference frequency $\Delta\omega$ must be lower than ω_n^2.

(5) LPLL design step

- Specify the center frequency.
- Specify the damping factor. (ζ for 2nd order system)
- Specify the lock range $\Delta\omega_L$ or the noise bandwidth B_L. $\Delta\omega_L$ and B_L cannot be specified independently.
- Specify the frequency range of the LPLL.
- Specify VCO parameters.
- Determining phase detector gain.
- Determining the nature frequency.
- Designing the loop filter.

Usually, a PLL is expected have some of the following properties:

- PLL should have a fast transient response. It can synchronize the input and response quickly while the input is in the transient state, which should include varying frequency, magnitude and signal phase.
- PLL should be stable in a broad frequency bandwidth. It means that the PLL should have a wide lock-in range for frequency and phase tracking.

- PLL should be harmonics stable. It means that PLL can work well under an input distortion, can attenuate the harmonics and the output should present an acceptable THD for a given template distorted input commutation voltage.
- PLL should be robust not only for frequency but also for varying magnitude of the input. PLL is insensitivity to frequency or magnitude changing. Any changing of input whatever frequency and magnitude should not lead to PLL failure to track the input.
- PLL should have a zero steady state error. An accurate output is important for pulse firing in the application of power electronics.

3.2.2 Conventional PLL (CPLL)

The block diagram of a conventional PLL (CPLL) is shown in Figure 3.2.

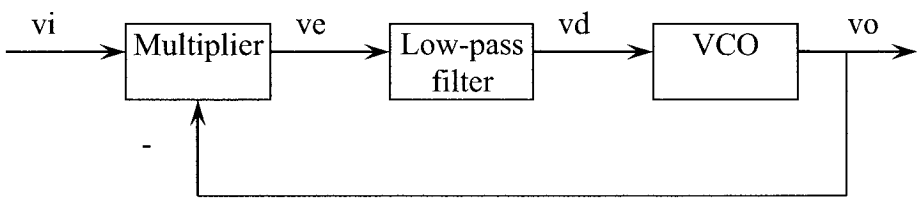

Figure 3.2 Block diagram of Conventional PLL

This type of PLL consists of a Phase Detector (PD), a low pass filter and a VCO. The PD is a linear gain during the phase angles ($-\pi/2 \sim \pi/2$). The PD gain depends also on the amplitude of the input signal and is not a property of the circuit alone. The loop filter in the conventional PLL is a low-pass filter, which is used to

remove any high-frequency and noise components from the PD and provides a DC controlled signal for the VCO. The output of the loop filter is proportional to phase error. A large DC gain and a small AC gain are desired in a loop filter deign. There are two types of low-pass filter possible: passive filter and active filter. A passive filter can only give a maximum gain of unity, but the active filter can provide a much bigger gain than the passive filter. The VCO is a frequency oscillator including an integrator, whose instantaneous angular frequency is a linear function of the controlled signal around the central operating frequency. Since the PD and VCO design are usually less flexible, the design of the loop filter is the principle factor in determining the bandwidth. There is usually a compromise in selecting the cut-off frequency ω_c of the low-pass filter. If ω_c is too high, it will introduce a high frequency noise. On the other hand, if ω_c is too low, the system response will be sluggish. In this paper, we select the parameters of the low-pass filter (with the help of simulations and frequency domain analysis method) to balance both requirements of the system bandwidth (response speed) and system steady state error (harmonics distortion effect).

The CPLL is a linear PLL which consists of a multiplier (phase detector PD), a low-pass filter (LF) and a voltage-controlled oscillator (VCO).

(1) Phase Detector

Although the input and output signals of a PLL are often not pure sinusoids, for the moment, we will assume that they are. The input, the (commutation) voltage $v_i(t)$ and the output voltage $v_o(t)$ are defined below:

$$v_i(t) = V_i \sin(\omega_i t + \theta_i) \qquad (3\text{-}1)$$

$$v_o(t) = V_o \cos(\omega_o t + \theta_o) \qquad (3\text{-}2)$$

Where ω_i is the angular frequencies of the input signal with dimension "radians per second"; θ_i is the initial phase angle of the input; ω_o is the angle frequency of the output; θ_o is the initial phase angle of the output.

If the system is initially unlocked, the output $v_e(t)$ of PD is given by

$$\begin{aligned} v_e(t) &= K_m v_i(t) v_o(t) \\ &= 0.5 K_m V_i V_o \sin[(\omega_i - \omega_o)t + \theta_i - \theta_o] + \\ &\quad 0.5 K_m V_i V_o \sin[(\omega_i + \omega_o)t + \theta_i + \theta_o] \end{aligned} \qquad (3\text{-}3)$$

Where K_m is the constant associated with the multiplier.

The second term of Eq.3-3 with frequency $(\omega_i + \omega_o)$ is eliminated by the low pass filter. The first term is considered to be the output of the loop filter. Assuming the VCO output v_o becomes synchronous with the input signal v_i after a period time for transient. The v_d then be expressed as

$$\begin{aligned} v_d(t) &= 0.5 K_m V_i V_o \sin[(\omega_i - \omega_o)t + \theta_i - \theta_o] \\ &= 0.5 K_m V_i V_o \sin(\theta_i - \theta_o) \\ &= 0.5 K_m V_i V_o \sin(\theta_e) \end{aligned} \qquad (3\text{-}4)$$

Where, θ_e is the phase difference. This sinusoidal characteristic is shown in Figure 3.3.

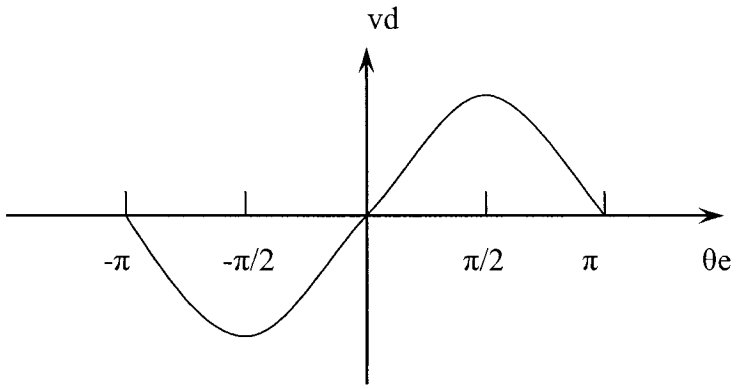

Figure 3.3 Sinusoidal Phase Detector Characteristic

For small values of θ_e, $\sin(\theta_e) \approx \theta_e$, (3-5)

$$v_d(t) \approx 0.5K_m V_i V_o \theta_e = K_d \theta_e \qquad (3\text{-}6)$$

K_d is the phase detector gain which depends on the amplitude of the input signals and *is not a property of the circuit alone*. The description of PD in the above equation is linear, although the linearity holds only for limited ranges. The linear model characteristic and signal diagram of PLL linear model are as follows:

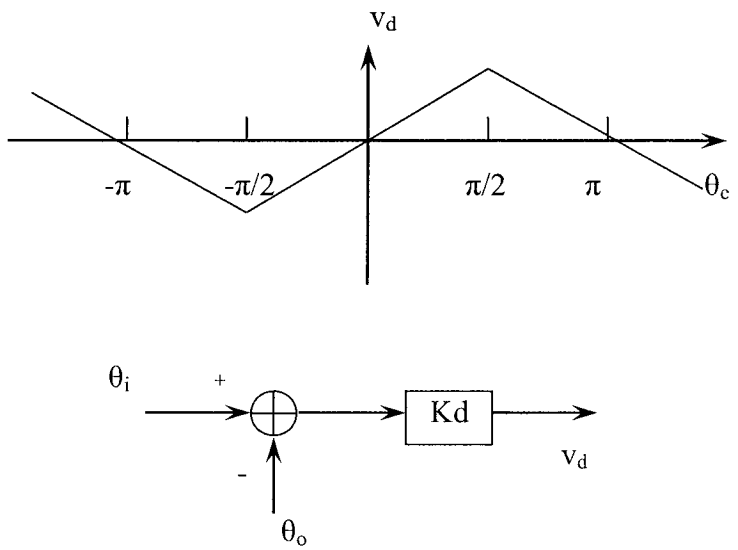

Figure 3.4 Sinusoidal Phase Detector characteristic under linearized model

A sinusoidal PD inherently has phase detection interval ($-\pi/2, \pi/2$).

(2) VCO

The VCO is a frequency oscillator including an integrator, whose instantaneous angular frequency is a linear function of the controlled signal, around the central operating frequency.

$$\omega_i - \omega_o = K_v v_d(t) = K_v K_d \sin(\theta_i - \theta_o) \quad (3\text{-}7)$$

$$\theta_o = \theta_i - \sin^{-1} \frac{\omega_i - \omega_o}{K_d K_v} \quad (3\text{-}8)$$

K_v is the VCO sensitivity. When $\omega_i - \omega_o = K_d K_v$, (3-8) gives $\theta_i - \theta_o = \pi/2$, indicating that the VCO signal is in phase quadrature with the input signal when the loop is locked. The product $K_d K_v$ is referred to as the loop gain. When the difference $|\omega_i - \omega_o|$ exceeds the loop gain K in a sinusoidal PD, lock can no longer exit.

(3) Loop filter

The loop filter in the conventional PLL is a low-pass filter, which is used to remove the high-frequency signal and noise components from the PD and provide a DC modulating signal for the VCO. The output of a loop filter is proportional to the phase error. A large DC gain and a small AC gain are desired in a loop filter design. There two types of low- pass filter: passive filter and active filter. A passive filter, although simpler, can only give a maximum gain of unity, but the active filter can provide a much bigger gain than the passive filter. Since the PD and VCO design are usually less flexible, the

designs of the loop filter are the principle factor in determining the bandwidth. There is usually a compromise in selecting the cut-off frequency ω_c of the low-pass filter. If ω_c is too high, it will introduce a high frequency noise. On the other hand, if ω_c is too low, the system response will be sluggish. The parameters of the low-pass filter can be selected with the help of simulations and frequency domain analysis method to balance the dual requirements of the phase margin (response speed) and system bandwidth (high frequency noise).

Usually there are three types of low-pass filter used in the PLLs.

a) **First order low-pass filter.**

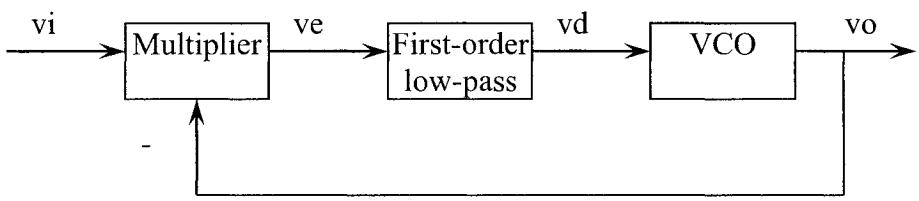

Figure 3.5 Conventional PLL with first-order low-pass filter

The transfer function of first order low-pass filter is:

$$F(s) = \frac{1}{1 + \tau s} \qquad (3\text{-}9)$$

A simulation study [3] show that a cut-off frequency around one fifth of the AC component $2\omega_1$ for a first-order low-pass filter gives satisfactory results. The transfer function of a first-order low-pass filter example is designed as follows:

$$F(s) = \frac{1}{1 + 0.00637s} \qquad \omega_c = 157 \text{ rad/s (25 Hz)} \qquad (3\text{-}10)$$

This system gives a constant steady state error of $\pi/2$.

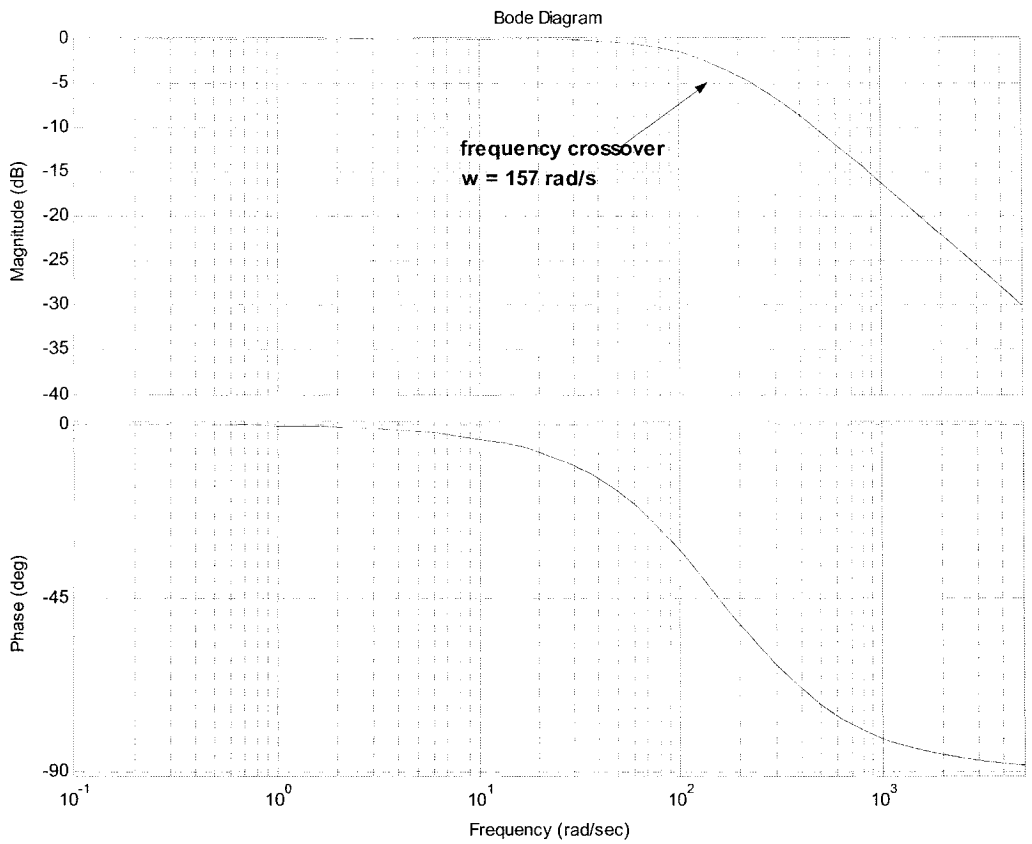

Figure. 3.6 First-order low-pass filter bode plot

b) **PI low-pass filter.**

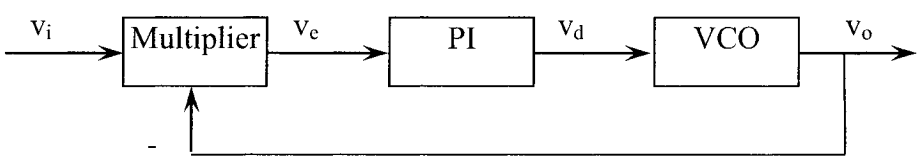

Figure 3.7 Conventional PLL with PI filter

In this thesis, a PI controller is used as loop filter to remove the constant steady error which usually accompanies a first order low pass filter. The PI controller is one type of an active filter. The transfer function of the PI filter is given by

$$F(s) = k_p + \frac{k_i}{s} \quad (3\text{-}11)$$

Clearly, the effects of the PI controller to the plant are: it adds a zero at s = - ki/kp to the forward-path transfer function, and adds a pole at s = 0 to the forward-path transfer function. This means that the system type is increased from type-I to type-II system i.e. the PI controller reduces the steady state error to zero. The introduction of a negative feedback loop herein keeps the PLL system in stable. The effects of PI are: (1) it improves damping and reduces maximum overshot; (2) it increases rise time; (3) it decreases bandwidth; (4) it improves gain margin and phase margin and (5) it attenuate high frequency noise. Based on the time-domain and frequency-domain analysis, the parameters of PI controller can be selected so that the system can obtain a good damping, bandwidth and phase margin. It should be noted that it is not possible to find suitable parameters of ki and kp so that all the three requirements are satisfied since the requirements of speed and stability always are contradictory. Some compromise has to be made. The characteristics of a PI filter are given below:

(1) For a given kp, the value of ki should not be too small, or the capacitor of the circuit implementation would be too large.

(2) The Phase Margin is around 45 ~ 60 degree.

(3) PLL system damping ratio is close to the best value i.e. $\xi = 0.707$.

(4) Bandwidth is selected to balance the speed requirement against the high frequency noise free requirement. The bandwidth of a conventional PLL depends on the gain of the PD, VCO and loop filter. In order to investigate the PI filter, we assume that the peak value of both input and output is unity, so that the gain of the PD and VCO is fixed.

For different input phase step, we can obtain the kp, ki and transfer function based on a method of simulation. When set damping ration equals 0.707, the system dynamic response speed become very slow so that the PLL system can not synchronize the input within 5 cycles. A trad-off has to made between response speed and steady state error and a gain is added to expand the bandwidth of PLL system.

A PI low-pass filter design example is shown as follows:

$$F(s)=\frac{20.3+90.1s}{s} \quad k_p=90.1;\ k_i=20.3 \quad (3\text{-}12)$$

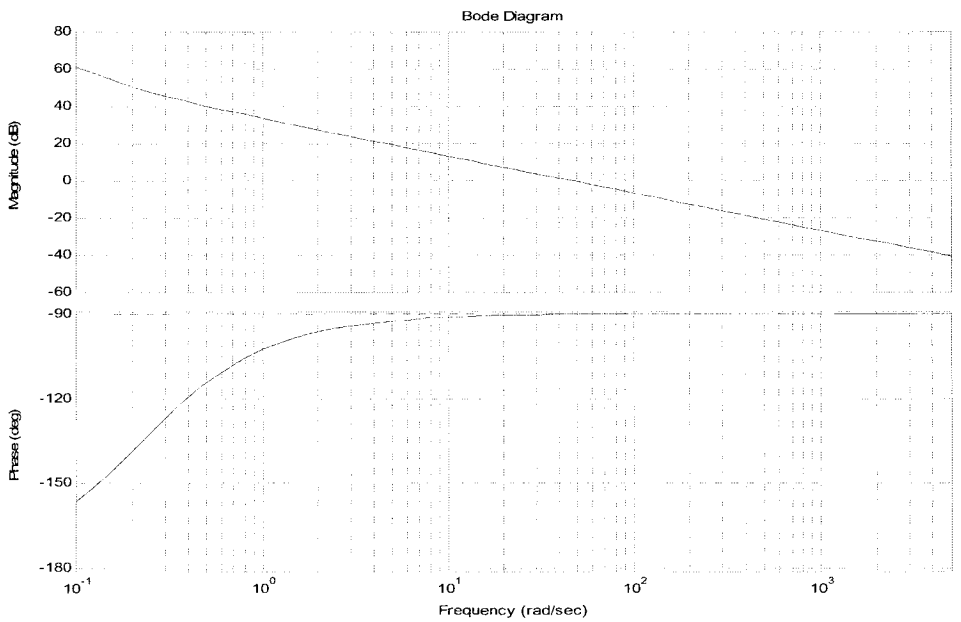

Figure. 3.8 PI low-pass filter Bode plot

c) **Higher order low-pass filter**

Higher order low-pass filters could be used instead of a simple one-pole filter, and it has the ability to roll off gain after the bandwidth at a sharper rate than lower-order filters. Because each pole introduces phase shift, it should be noted to maintain stability

in high order systems. It is easy to design a higher-order Butterworth low-pass filter by using of MATLAB. For a given order, the Butterworth filter, a kind of higher order low-pass filter, have the sharpest roll-off possible without introducing peaking in the Bode plot, and it is easy to design with the assistance of MATLAB.

A fourth-order Butterworth low-pass filter example is shown as follows:

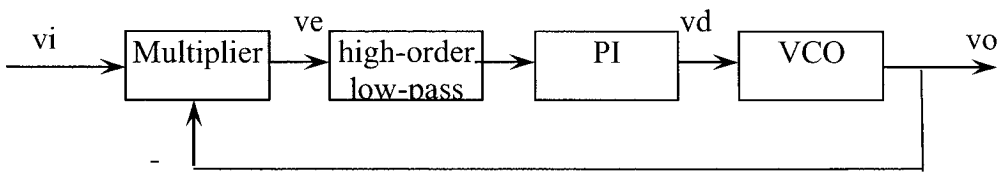

Figure 3.9 Conventional PLL with high-order low-pass filter

A fourth-order Butterworth low-pass filter example is shown as follows:

$$F(s) = \frac{6.088x10^8}{s^4 + 4.105x10^2 s^3 + 8.424x10^4 s^2 + 1.013x10^7 s + 6.088x10^8} \qquad (3\text{-}13)$$

ω_c = 157 rad/s (25 Hz) (3-14)

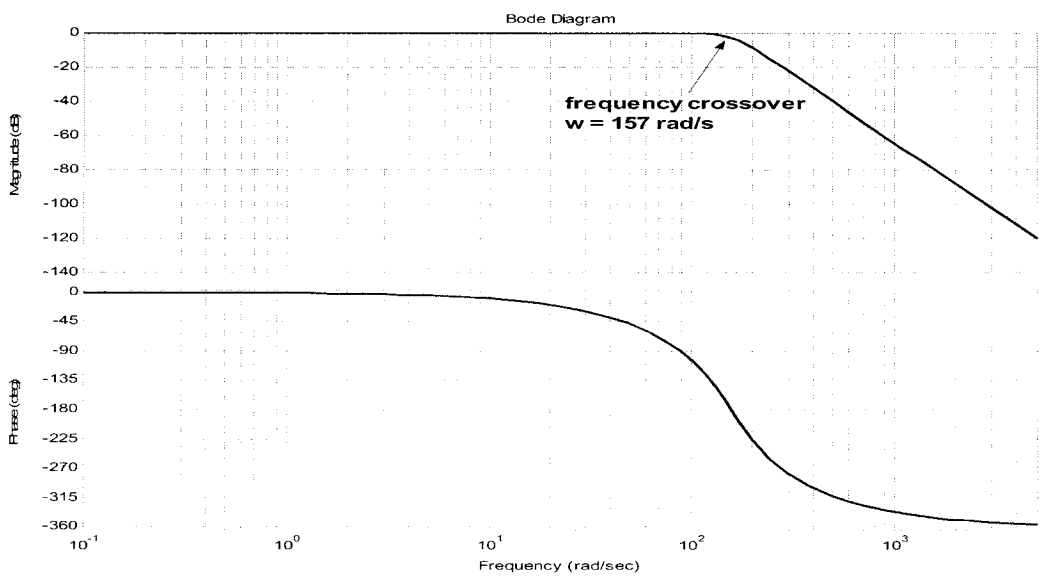

Fig. 3.10 Butterworth low-pass filter bode plot

(4) PLL Bandwidth

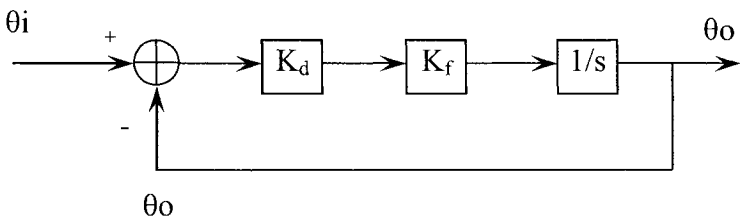

Figure 3.11 AC model of PLL

In discussing the bandwidth of a PLL, we form an AC model of the PLL by eliminating the DC parameters from the linear model. The forward gain of the loop is:

$$G(s) = K_d K_v K_f / s \quad (3\text{-}15)$$

K_d is phase detector gain, K_f is loop filter gain and K_v is VCO gain. The bandwidth is determined by the frequency for which $|G(j\omega)| = 0.707$ and gives an indication of the transient response properties in the time domain. A large bandwidth corresponds to a faster rise time since higher-frequency signals are more easily passed through the system. Conversely, if the bandwidth is small, only signals of relatively low frequencies are passed and the time response will be slow and sluggish. Bandwidth also indicates the noise-filtering characteristics and robustness of the system. From eq. (3-15) the bandwidth is:

$$\omega = K_d K_v K_f \quad (3\text{-}16)$$

Usually a wide enough bandwidth is desired so that it has the necessary speed to track the variations in input frequency. However, in the application for a HVDC system, the PLL

bandwidth is so small that the PLL is to extract the fundamental component rather than to track the input.

(5) Transfer function

Assuming the amplitude of the input and output signals is unity, thus the PD gain Kd is 0.5, Kv and Kf are 1. A trade-off is necessary to select the cutoff frequency and damping. The transfer function of conventional PLL is:

$$T(s) = \frac{0.5}{0.00637s^2 + s + 0.5} \qquad \text{(3-17) for one-order low-pass}$$

filter

The system has 2 poles at left real axis of poles plane, -0.5016 and -156.4843. Damping ratio $\xi = 1$.

$$T(s) = \frac{45.05s + 10.15}{s^2 + 45.05s + 10.15} \qquad \text{(3-18) for PI low-pass filter}$$

This system has one zero and two poles at left poles plane -44.86 and -0.2264, Damping ratio $\xi = 1$. A trade-off is made to select the bandwidth and damping ratio.

3.2.3 DQ Three-phase PLLs

The block diagram of DQ 3-phase PLL is shown in Figure 3.12:

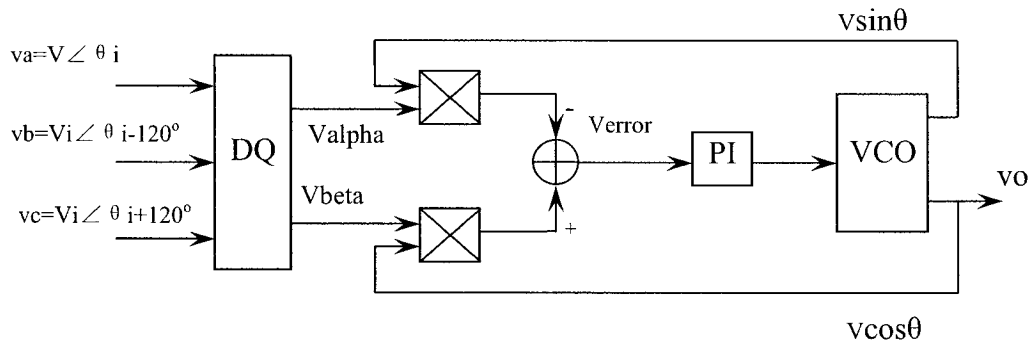

Figure 3.12: Block diagram of DQ 3-phase PLL

In this case, The DQ transform in a 3-phase PLL is used to transfer a three phase symmetrical AC phasor to DQ components (Figure 3.9). Through the transformation, a DC error signal proportional to fundamental phase error between input and output signals is generated. It will be fed through a PI controller to generate a modulating signal for the VCO. And the VCO can generate a sinusoidal signal. A low pass filter is used to remove all AC components.

Assuming the input three phase AC voltage signals are:

$$v_a = \hat{V}\cos(\omega t + \theta_i);$$
$$v_b = \hat{V}\cos(\omega t + \theta_i - 120°); \quad (3\text{-}19)$$
$$v_c = \hat{V}\cos(\omega t + \theta_i + 120°)$$

The 3-phase commutation voltages are transformed into DQO axis components, v_{alpha} and v_{bcta}, using the following equations:

$$V_{alpha} = \frac{2}{3}V_a - \frac{1}{3}V_b - \frac{1}{3}V_c \quad (3\text{-}20)$$

$$V_{beta} = \frac{1}{\sqrt{3}}(V_b - V_c) \quad (3\text{-}21)$$

$$V_{error} = -V_{alpha} V \sin\theta + V_{beta} V \cos\theta \qquad (3\text{-}22)$$

The small signal block diagram of DQ 3-phase PLL is shown in Figure 3.13.

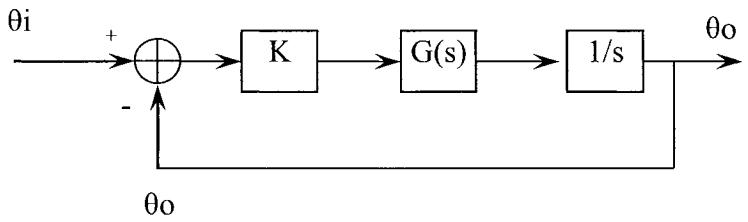

Figure 3.13: Small signal block diagram of DQ type PLL

This small signal structure is similar to the conventional PLL. The PI controller herein is used to remove the AC components which represent the harmonics in 3-phase AC system. The open loop transfer function of DQ PLL is as follows:

PI : $F(s) = \dfrac{20.3 + 90.1s}{s}$ $k_p = 90.1;\ k_i = 20.3$ (3-23).

System open loop transfer function: $G(s) = \dfrac{90.1s + 20.3}{s^2}$ (3-24)

And the close loop transfer function is: $T(s) = \dfrac{90.1s + 20.3}{s^2 + 90.1s + 20.3}$ (3-25)

Analyzing the poles and zeroes of the system, it is noted that there are two poles at the left real axis, -0.2259 and -89.8741 in the left half plane and the damping ratio $\xi = 1$. It should be pointed out that the unbalance of input commutation voltage would generate a phase shift between the input and output. The output of DQPLL is only an average phase of the 3-input phasor.

Based on the simulation tools EMTP RV and MATLAB, the Bode plot analysis is shown in Figure 3.14:

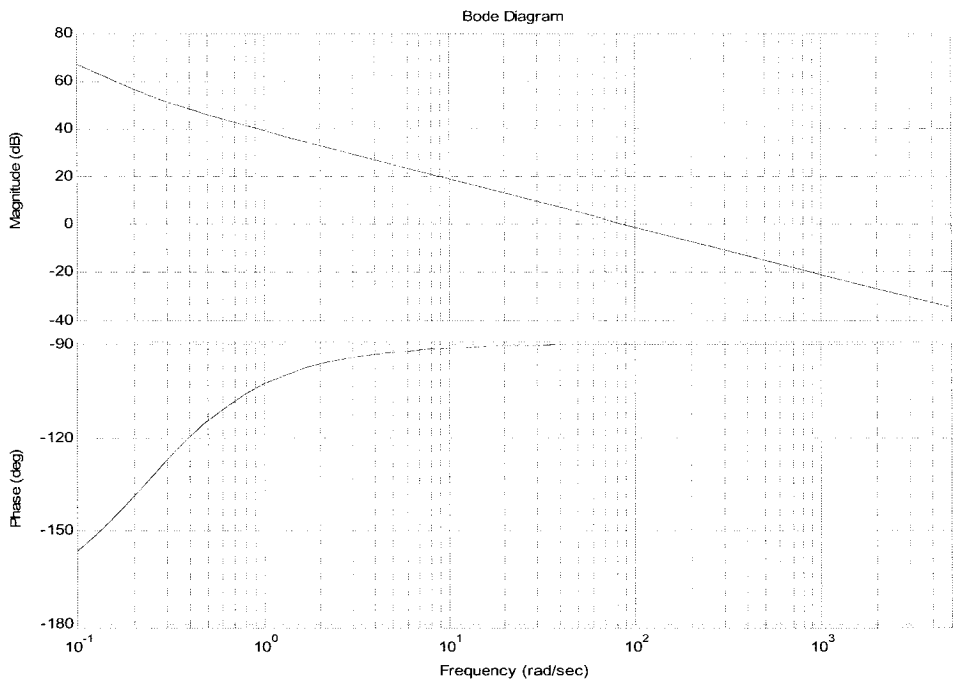

Figure 3.14: DQ PLL bode plot

3.2.4 Enhanced PLL (EPLL)

The main performance in the structure of the EPLL (Figure 3.15) is in the instruction of a novel phase detection scheme which can make a sensitive response to fundamental signal. Only fundamental signal exists in primary AC error (the sum between input and estimator) can generate a DC error signal. It will really improve the harmonic stability of EPLL system. EPLL have two negative feedback loops, main loop and estimator loop. The main loop of EPLL is normal including PD, LP and VCO

functions. The estimator loops include two branches, one is amplitude tracking branch, and the other one is phase tracking branch. Both phase information and the amplitude information of input are used not like other PLL which mostly only use the phase information.

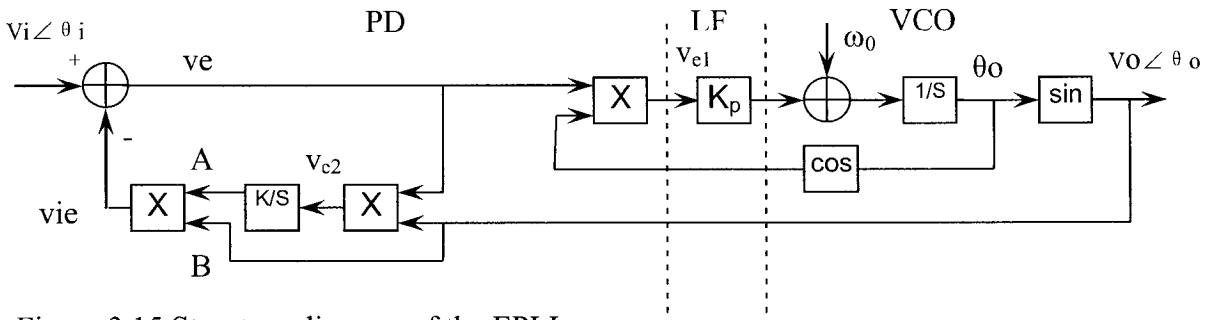

Figure 3.15 Structure diagram of the EPLL

The function diagram of the EPLL is shown in the Figures 3.16, 3.17.

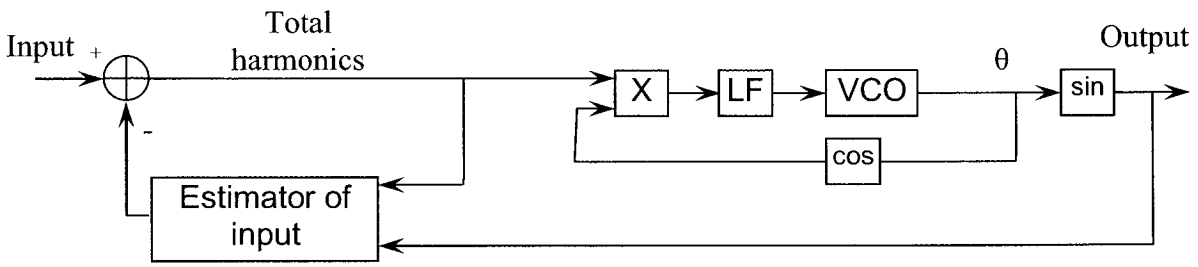

Figure 3.16 Simplified structure diagram of the EPLL

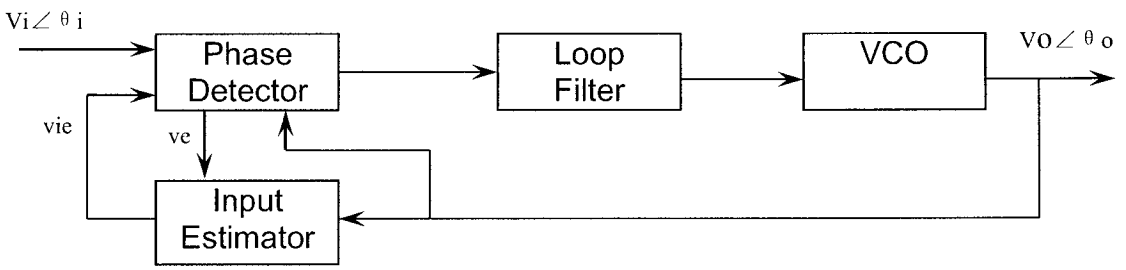

Figure 3.17: Function diagram of the EPLL

Analyzing the structure of EPLL, there exist two feedback loops in this PLL. One is the main loop including the functions of PD, VCO and LP. The other is the Estimator loop which is used to estimate a signal with the same phase and same amplitude of input fundamental component. Assuming the input is given by $v_i(t) = A\sin(\omega t+\theta_1)$

(3-26)

And the output of estimator is: $v_{ie}(t) = A\sin(\omega t+\theta_2)$ (3-27)

For the main loop:

$$ve(t) = A\sin(\omega t + \theta_1) - A\sin(\omega t + \theta_2) = 2A\cos(\frac{2\omega t + \theta_1 + \theta_2}{2})\sin(\frac{\theta_1 - \theta_2}{2}) \quad (3\text{-}28)$$

$$\begin{aligned} & v_{e1}(t) \\ & = 2A\cos(\frac{2\omega t + \theta_1 + \theta_2}{2})\sin(\frac{\theta_1 - \theta_2}{2})\cos(\omega t + \theta_2) \\ & = A(\cos(2\omega t + \frac{\theta_1 + 3\theta_2}{2}) + \cos(\frac{\theta_1 - \theta_2}{2}))\sin(\frac{\theta_1 - \theta_2}{2}) \\ & = A\cos(2\omega t + \frac{\theta_1 + 3\theta_2}{2})\sin(\frac{\theta_1 - \theta_2}{2}) + \frac{1}{2}\sin(\theta_1 - \theta_2) \\ & = A\cos(2\omega t + \frac{\theta_1 + 3\theta_2}{2})\sin(\frac{\theta_e}{2}) + \frac{1}{2}\sin(\theta_e) \end{aligned} \quad (3\text{-}29)$$

For small values of θ_e, $\sin(\theta_e) \approx \theta_e$, (26). Hence,

$$v_{e1} = k_1\theta_e + \frac{1}{2}\theta_e = k_2\theta_e \quad (3\text{-}30)$$

$$\begin{aligned} k_1 &= A\cos(2\omega t + \frac{\theta_1 + 3\theta_2}{2}) \\ k_2 &= \frac{1}{2}A\cos(2\omega t + \frac{\theta_1 + 3\theta_2}{2}) + \frac{1}{2} \end{aligned} \quad (3\text{-}31)$$

The phase detector of EPLL is a gain. Only the fundamental component within the signal v_e can result in a DC error. The AC error will be filtered out by the first order low pass filter.

For the Estimator loop:

$$
\begin{aligned}
& v_{e2}(t) \\
& = 2A\cos(\frac{2\omega t+\theta_1+\theta_2}{2})\sin(\frac{\theta_1-\theta_2}{2})\sin(\omega t+\theta_2) \\
& = A\sin(2\omega t+\frac{\theta_1+3\theta_2}{2})\sin(\frac{\theta_1-\theta_2}{2})-A\sin^2(\frac{\theta_1-\theta_2}{2}) \\
& = A\cos(2\omega t+\frac{\theta_1+3\theta_2}{2})\sin(\frac{\theta_e}{2})-A\sin^2(\frac{\theta_e}{2})
\end{aligned}
\qquad (3\text{-}32)
$$

In EPLL, a sinusoidal error generator (a multiplier) is used in both main loop and input estimator loop. This error generator can generate a DC error only when the input (ve) of error generator consists of fundamental component after a low-pass filter. The main loop of EPLL consists of a phase detector, a loop filter and a VCO. And the estimator loop is to estimate the input signal, which consists of two function units: the amplitude estimate unit and the phase estimate function. The amplitude estimator includes a sinusoidal error generator, a loop gain and an integrator. The output of error generator will include a DC component if an AC fundamental component passes through the error generator. After a low pass filter (integrator), the DC component will become a linear slope curve, and the AC component will be attenuation. Since the input phase is assumed to be equal to that of the output, the phase information is just picked up from VCO. This is the phase estimator unit. Finally a multiplier is used to combine these two information, phase and amplitude, and an estimated input signal is obtained. EPLL uses the phase information as well as the amplitude information of the input to track the fundamental of the input. This scheme can make dynamic response rapidly. Moreover the introduction of the new sinusoidal style PD improves the system harmonics stability.

3.2.5 New PLL technique

Basing on the fundamental PLL structure, some new technique, such as active filter, nonlinear phase detector, peak value estimator and positive sequence phase detector, are supposed to be capable to benefit the design and optimization of PLLs. There usually are unwanted AC second harmonic components in an error signal during the normal operation condition. A low-pass filter normally used in loop to filter out harmonics will result in low response speed. The proposal resolving method is active filter technique which can obtain a quicker response than common low pass filter and remove the drawback of passive filters which usually generate the phase lag. One proposal method is to generate a second harmonic signal which has the same frequency, phase and amplitude with that exists in error signal and to cancel it. To build a second harmonics signal, there are different methods. The Phase Shifter and Second Harmonic Generator are two of these options. There are something need to be noticed that the input frequency is not a constant value. Thus the phase and frequency circuit must have a frequency measurement unit. Except the frequency and phase unit, the amplitude unit is also required. The Peak Detector technique can be used in this area. The active filters can quickly filter out the AC component of error than the low pass filter. The active filter can benefit the PLL system, making system faster, but it also brings the damage of system harmonic stability.

CHAPTER 4

COMPARISON

The major difference among the CPLL, DQPLL and EPLL is due to a different PD structure and loop filter. The CPLL utilizes the multiplier as the PD; the DQPLL makes use of DQ transform and EPLL uses both differentiation and the multiplier as PD. Due to the presence of the AC harmonic components in the error signal under normal operating conditions, a low pass filter is required in all three PLL systems. However, the presence of a low pass filter also brings a drawback that it narrows the system bandwidth which directly influences the response speed.

In comparison with the three PLL's structure, they all maintain the same basic structure: PD, LF and VCO. In order to improve the system performance, some new technologies and mathematical methods are applied for PLL. The CPLL is a basic PLL, which usually has a constant steady state error when a normal low-pass filter is used. However, when an active loop filter, PI, replaces the low-pass filter, the system type is improved to type II and, the CPLL sustains a zero steady state error for a step input as a result. Both DQPLL and EPLL are type II systems, and they have zero steady state error when a step input is applied. DQPLL is a three-phase PLL, whose output depends on the information of three phases. It is sensitive to an unbalanced voltage due to the application of DQ transform. When commutation voltage suffers an unbalance, such as a single phase short circuit fault, the output accuracy of DQPLL will be influenced, and result in the loss of synchronization. However, some improved methods, such as the application of

positive components extraction, and averaging technology can be employed to remove this sensitivity. The DQ PLL presents a better attenuation characteristic of harmonics than other PLLs due to its three phase PD structure. The PD of EPLL is based on an input estimator which collects both phase and amplitude information from the input. The other PLLs use only the phase information. Due to the full information picked by the system, the EPLL can track the input faster and more accurately than other PLLs. Moreover, the estimator also improves the system parameter robustness and removes the input amplitude dependence which exists in CPLL and DQPLL. In the forward loop of the EPLL, there is no 1st order low-pass filter which is normally present in the DQPLL and CPLL. Instead, a gain is used as a loop filter. Also, there exist two feed back loops in the structure of EPLL as opposed to one in CPLL and DQPLL. Thus, the feedback can provide more negative feedback information of the output to the controller. Due to the absence of a low-pass filter and simple forward loop structure, the EPLL provides a faster dynamic response, but a bigger THD output than other PLLs. Thus a trad-off has to be made to balance both requirements of the PLL system.

A PLL comparison table is shown as follows:

Table 4.1. Comparison of PLLs

	CPLL	DQPLL	EPLL
Phase Detector	Multiplier	DQ transform	Differentiation& Multiplier
Loop Filter	Low-pass & PI	Low-pass & PI	Linear gain
VCO	Yes	Yes	Yes
Num of feedback loops	1	1	1
Tracking information	Phase	Phase	Phase & amplitude
Steady state error	Constant / zero	zero	zero
AC system unbalance sensitivity	No	Yes	No
Input amplitude sensitivity	Yes	No	No
Type of system	I / II	II	II

CHAPTER 5

PLL VALIDATION TESTS

5.1 Introduction

In this chapter, three typical tests: harmonics distortion test, magnitude step test, phase step response test and loss of synchronization test are performed to test the PLL performance. The program EMTP RV is used to build the test model, and Matlab is used to analyze the data. In each of the tests, the following signals are presented:

a) The pu input v_i (full line) and output v_o (dotted line) voltages from the PLL,

b) Theta signals: these represent the angular position of the input θ_i (presents by *thei*, full line) and output θ_o theo (presents by *theo*, dotted line) voltages shown above in (a), and

c) The angular difference between the signals shown in (b) above, i.e. $\Delta\theta$ (presents by *delta_theta*) $= \theta_i - \theta_o$.

5.2 Harmonic Distortion Test

This test first monitors the performance of the three PLLs with an injection of a 20% of fifth harmonic voltage and a 20% seventh harmonic voltage on the commutation voltage. These harmonics typically distort the commutation bus voltage when a rectifier is connected to a weak AC system in steady state. Moreover a futher test is designed to simulate commutation bus harmonics pollution of a THD of 5% and 10% for input to check and compare the THD value of output.

5.2a Harmonic Distortion Test for CPLL

Figure 5.1 shows that the output voltage of PLL contains virtually no harmonics and is rapidly synchronized to the fundamental component of the commutation voltage. Fig. 5.1 also shows that there exists a little 2nd harmonic component in the phase output since the loop filter does not completely filter out all 2nd harmonic which is created by PD.

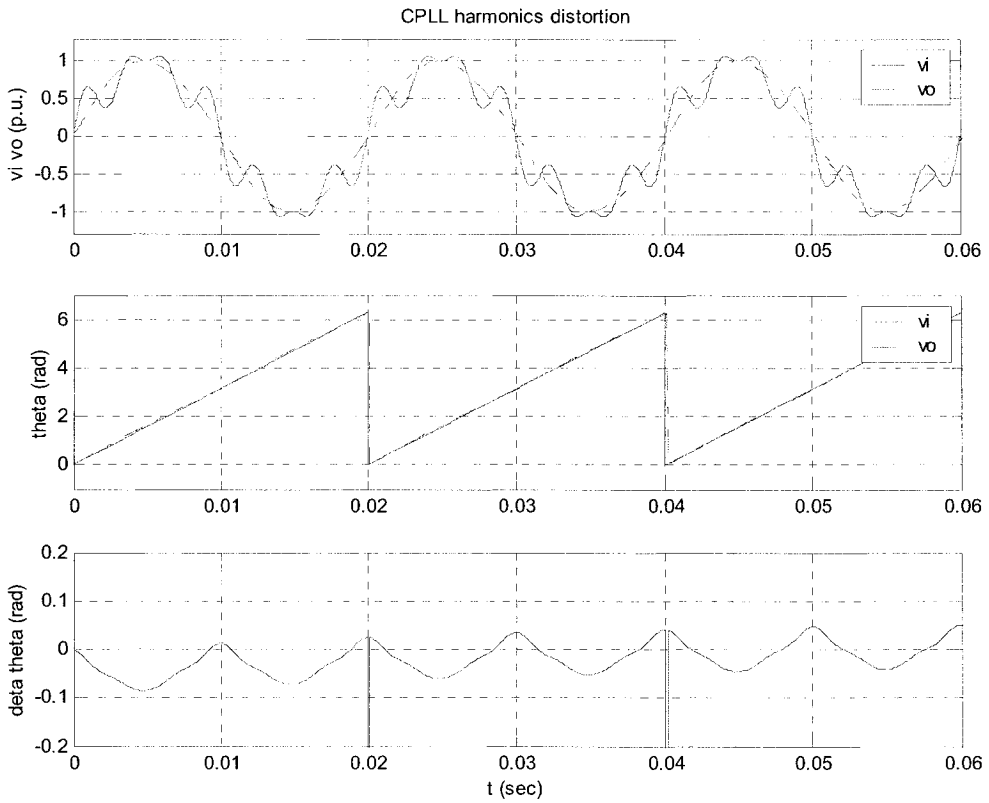

Figure 5.1: Harmonics distortion test for CPLL

Further harmonics pollution test for a given distorted input voltage (THD equals 5% and 10%) shows that the output THD is smaller than 0.107% for 5% THD harmonic injection and 0.2098% for 10% THD harmonic injection.

5.2b Harmonic Distortion Test for DQPLL

Figure 5.2 shows similar results obtained with the CPLL. However, the DQPLL displays a better anti-distortion character when the AC system commutation voltages are balanced.

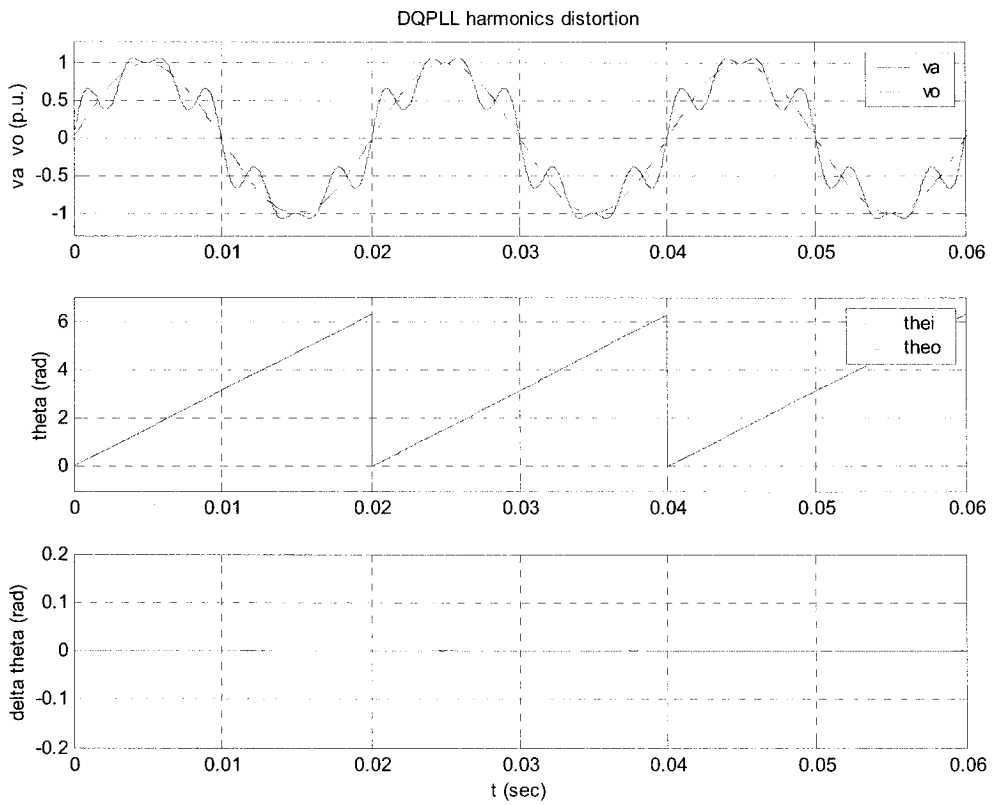

Figure 5.2: Harmonics distortion test for DQPLL

Further harmonics pollution test for a given distorted input voltage (THD equals 5% and 10%) shows that the output THD is smaller than 0.0042% for 5% and 10% THD harmonic injection. The value of THD is very small and shows good attenuation performance of harmonics.

5.2c Harmonic Distortion Test for EPLL Test

Similarly, Figure 5.3 shows the corresponding results with EPLL.

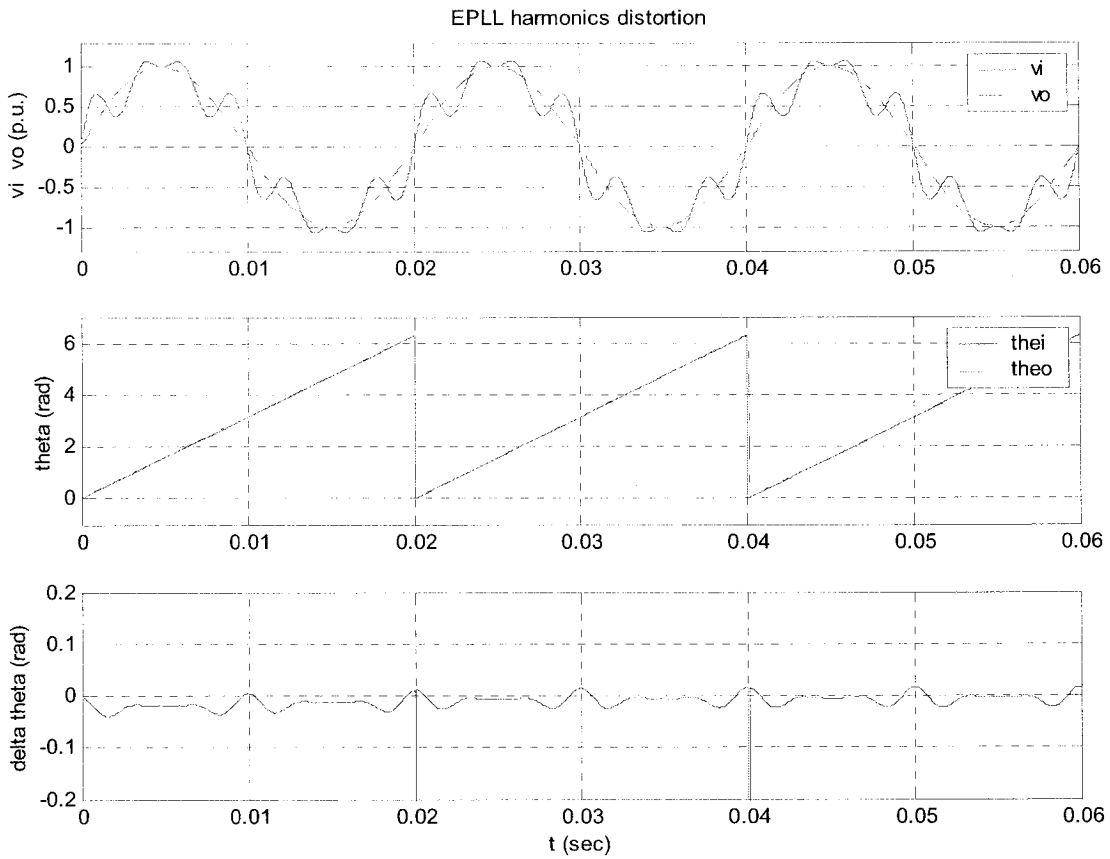

Figure 5.3: Harmonics distortion test for EPLL

Further harmonics pollution test for a given distorted input voltage (THD equals 5% and 10%) shows that the output THD is smaller than 0.21% for 5% THD harmonic injection and 0.42% for 10% THD harmonic injection.

5.3 Magnitude Step Response

This test monitors the performance of the three PLLs with a transient commutation voltage amplitude step change of a 200% rating.

5.3a CPLL Magnitude Step Response

The magnitude step response for the CPLL (Figure 5.4) shows that the $\Delta\theta$ waveform includes a big phase error (2^{nd} harmonic component) and the output voltage v_o and phase angle θ_o are not able to synchronize with the input commutation signal v_i and phase θ_i respectively when input commutation bus voltage has a magnitude step change of 200% rating. This test presents that the CPLL becomes sensitive when the input is more than 1 per unit since the phase gain is the function of amplitude of input.

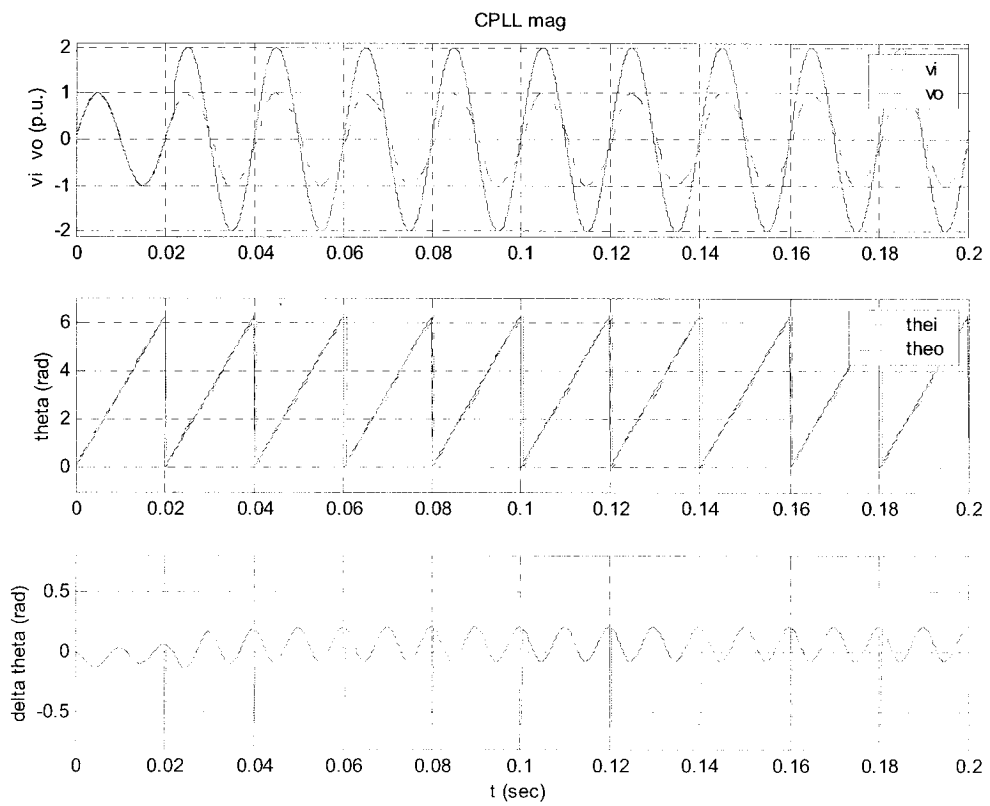

Figure 5.4: Magnitude step response test for CPLL

5.3b DQPLL Magnitude Step Response

The magnitude step response for the DQPLL (Figure 5.5) shows that the output voltage v_o and phase angle θ_o are able to synchronize with the input commutation signal v_i and phase θ_i respectively when input commutation bus voltage has a magnitude step change of 200% rating. This test presents that the DQPLL show a good performance when the input is 2 per unit. Further test shows that DQPLL will work well even when input amplitude is more than 10 per unit.

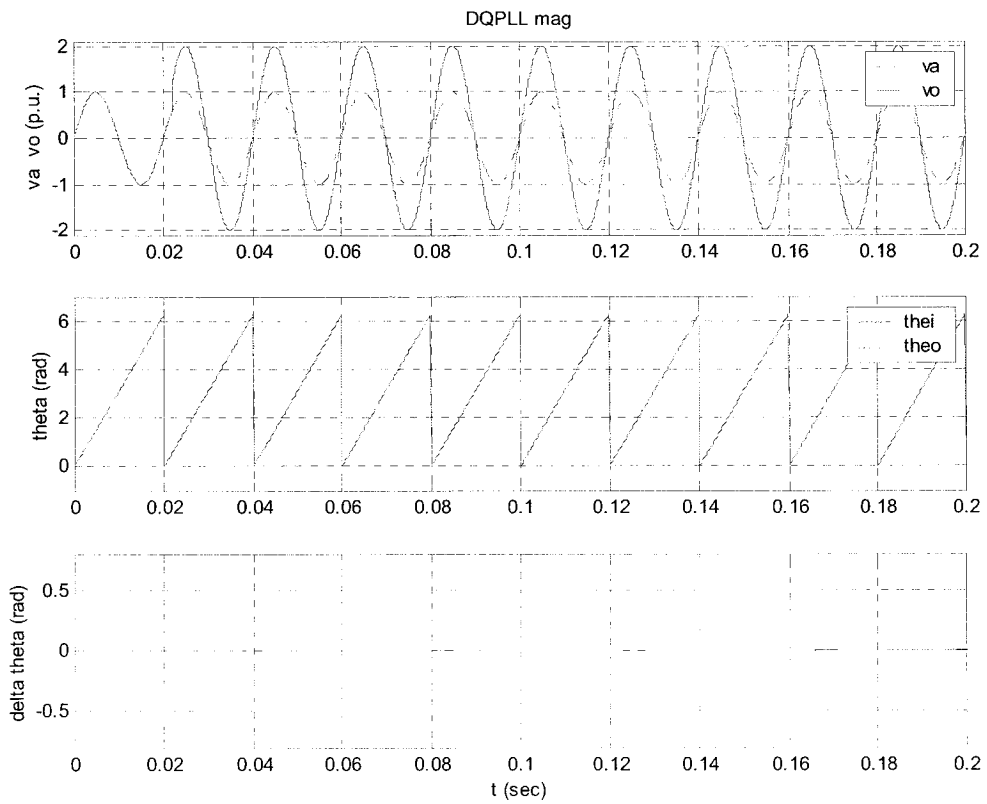

Figure 5.5: Magnitude step response test for DQPLL

5.3c EPLL Magnitude Step Response

The magnitude step response for the EPLL (Figure 5.6) shows that the output voltage v_o and phase angle θ_o are able to synchronize with the input commutation signal v_i and phase θ_i respectively when input commutation bus voltage has a magnitude step change of 200% rating. This test presents that the EPLL shows a good performance when the input is more than 1 per unit. Further test shows that EPLL will keep in the synchronization even when input amplitude increase to 10 per unit but need longer response set time.

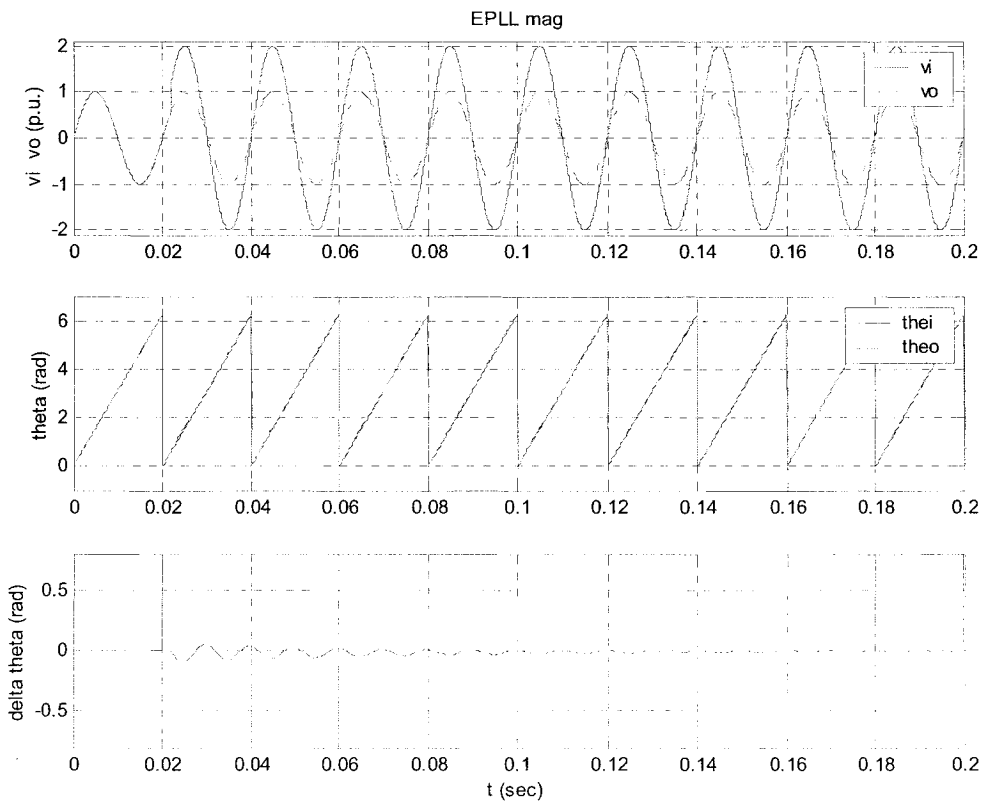

Figure 5.6: Magnitude step response test for EPLL

5.4 Phase Step Response

This test monitors the performance of the three PLLs under a phase jump, which can happen in the actual HVDC system when a single phase fault occurs on the AC system. During this test, a 60^{o} phase step jump of commutation voltage of phase of phase A is applied at time = 0.022 sec.

5.4a CPLL Phase Step Response

The phase step response for the CPLL (Figure 5.7) shows that the output voltage v_o and phase angle θ_o are able to synchronize with the input commutation signal v_i and phase θ_i respectively within 5 cycles (i.e. 100ms at 50 Hz). The $\Delta\theta$ waveform also confirms that the control loop is slightly under-damped.

Further evaluation shows that if the phase step is set at a smaller value, i.e. 5^{o} (result not shown here), the output v_o is able to synchronize with the input v_i within 1 cycle (20 ms at 50 Hz).

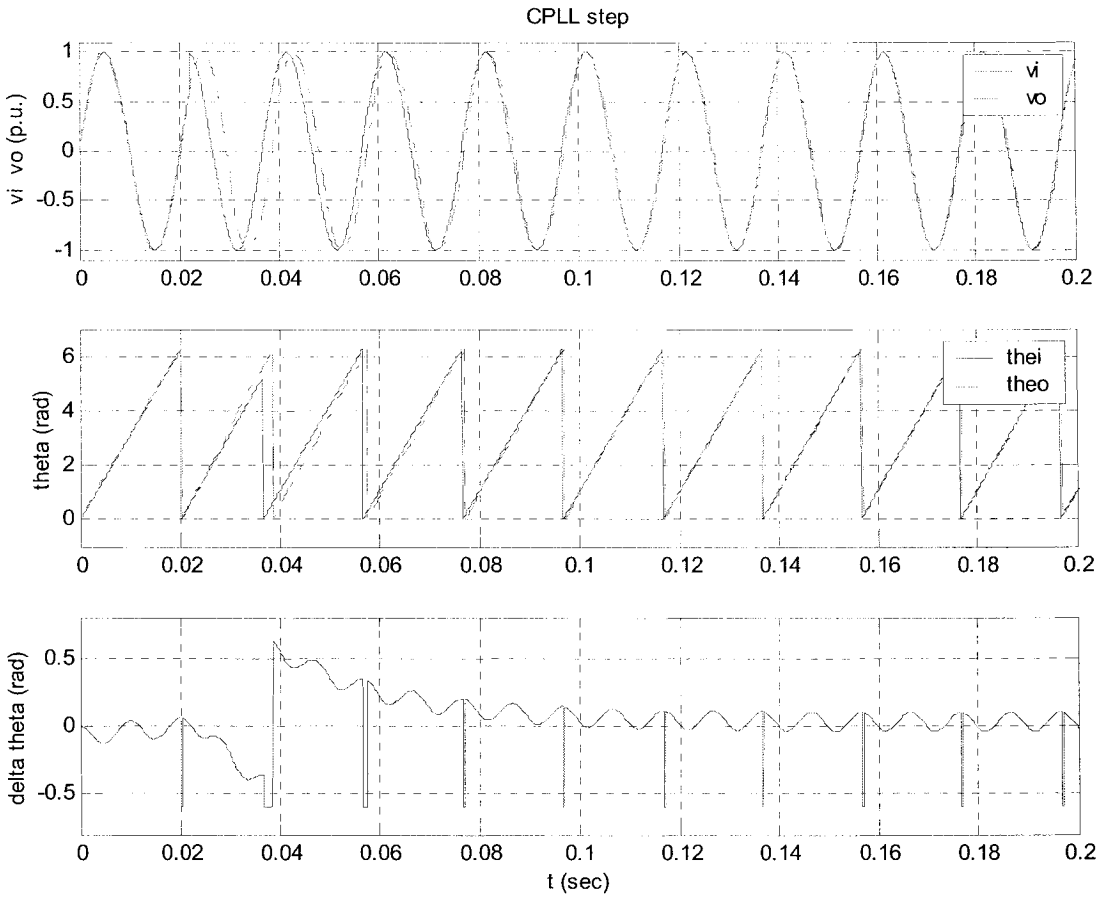

Figure 5.7: Phase step response test for CPLL

5.4b DQPLL Phase Step Response

The phase step response for the DQPLL (Figure 5.8) shows that the output voltage v_o and the phase angle θ_o are unable to synchronize with the input commutation signal v_i and phase angle θ_i respectively within 5 cycles (i.e. 100 ms at 50 Hz). There exists a phase angle error between the input and output due to characteristics of the DQ PLL; its output is an average value of all three phase inputs. When three inputs are unbalanced, for example, phase A has a phase jump, the output of DQ PLL is unable to synchronize with the commutation voltage. There always exists a fixed steady error in the

phase output and is a drawback of DQPLL. This test proves that the DQPLL is sensitive to phase angle unbalance in the three input waveforms.

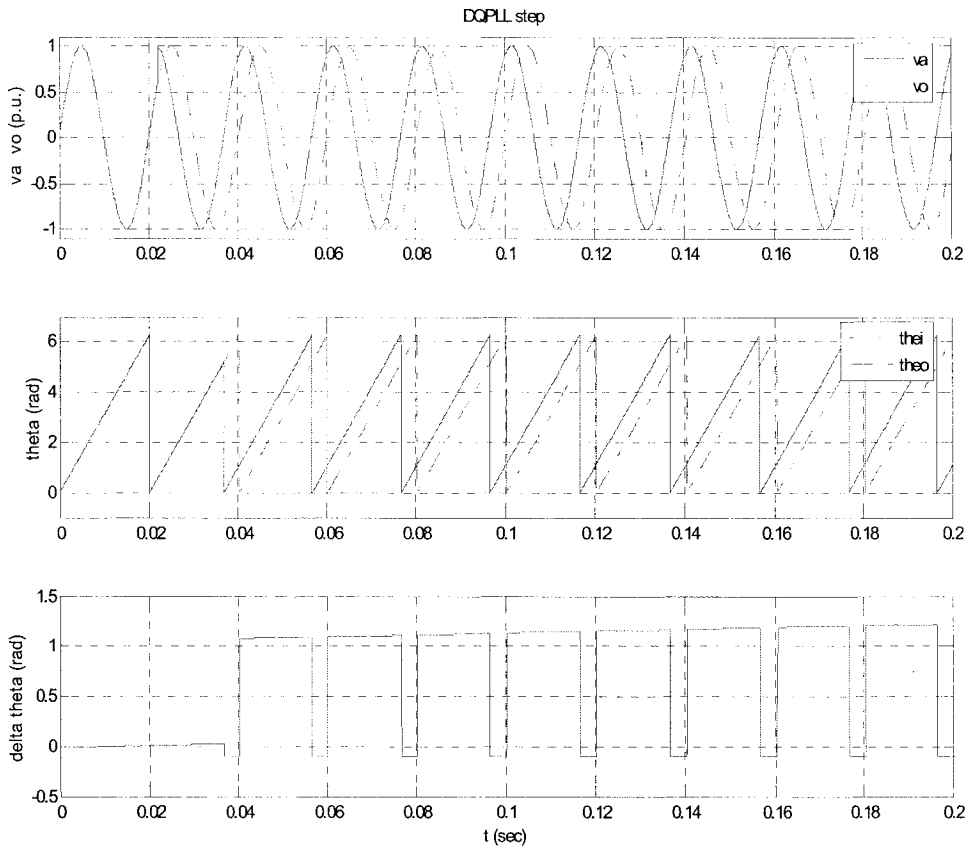

Figure 5.8: Phase step response test for DQPLL

5.4c EPLL Phase Step Response

Figure 5.9 shows the phase step response for the EPLL. The dynamics of the PLL shows that the output voltage v_o and the phase angle θ_o are able to synchronize with the input commutation signal v_i and phase angle θ_i, respectively within 3 cycles (i.e. 60 ms at 50 Hz). Also, if the phase step is set at smaller value of 5^o (results not shown), the output is able to synchronize with the input within 1 cycle (i.e. 20 ms at 50 Hz). The waveform

of $\Delta\theta$ also shows that the control loop is slightly under-damped and requires a settling time of about 4 cycles.

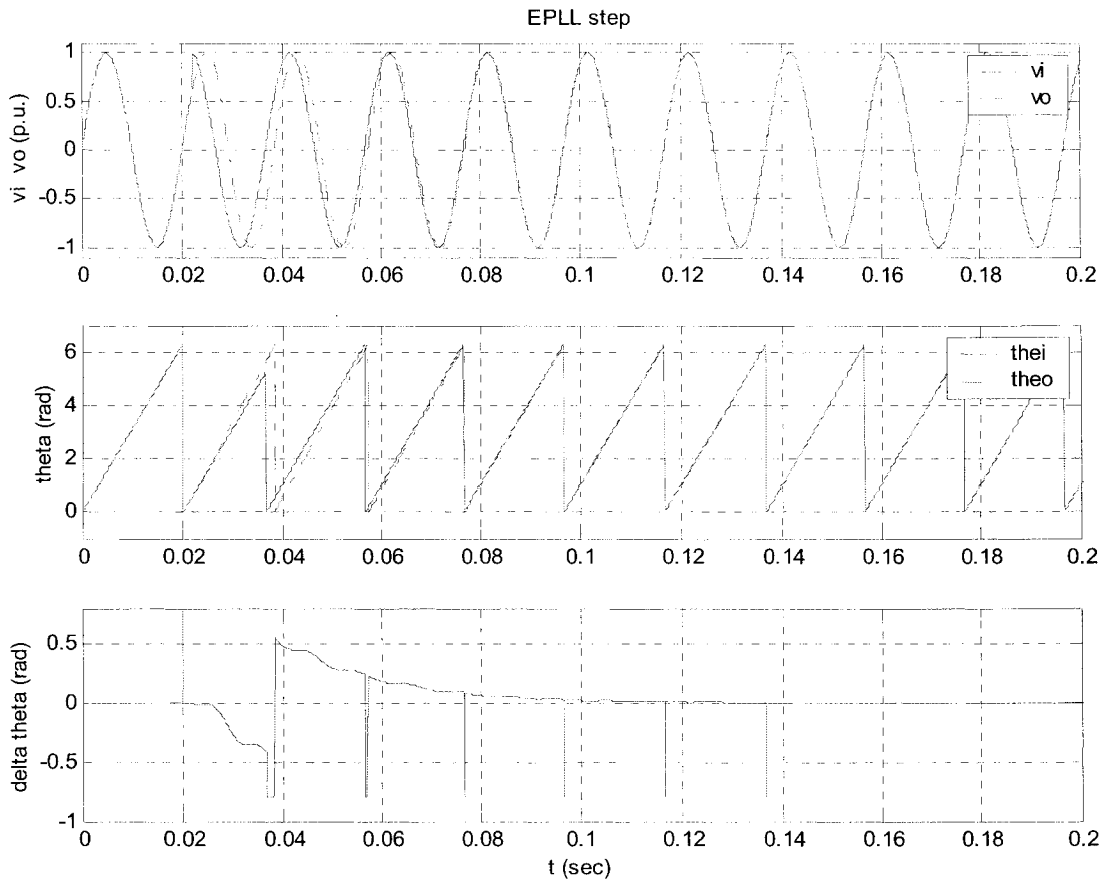

Figure 5.9: Phase step response test for EPLL

5.5 Loss of Synchronization

This test monitors the performance of the three PLLs under loss synchronization, which can happen in the actual HVDC system when the recloser opens after a temporary 3-phase fault occurs on the AC system. During this test, the commutation voltage v_i is unavailable at time = 0.022 sec. for 5 cycles. The VCO stage of the PLL is therefore in free running mode with a fixed center frequency of 50 Hz. Assume the actual frequency

(50.2 Hz before fault occurs) of the HVDC system is different than the center frequency of the PLLs at the moment of the free running.

5.5a Loss of Synchronization Test for CPLL

Figure 5.10 shows the internal signals from the CPLL during a temporary loss of the commutation voltage caused by a fault on the AC commutation bus. The output voltage is able to synchronize with the commutation voltage within 1 cycle (20 ms at 50 Hz). During the fault period, the output voltage is a free-running sinusoidal waveform with a fixed center frequency of 50 Hz.

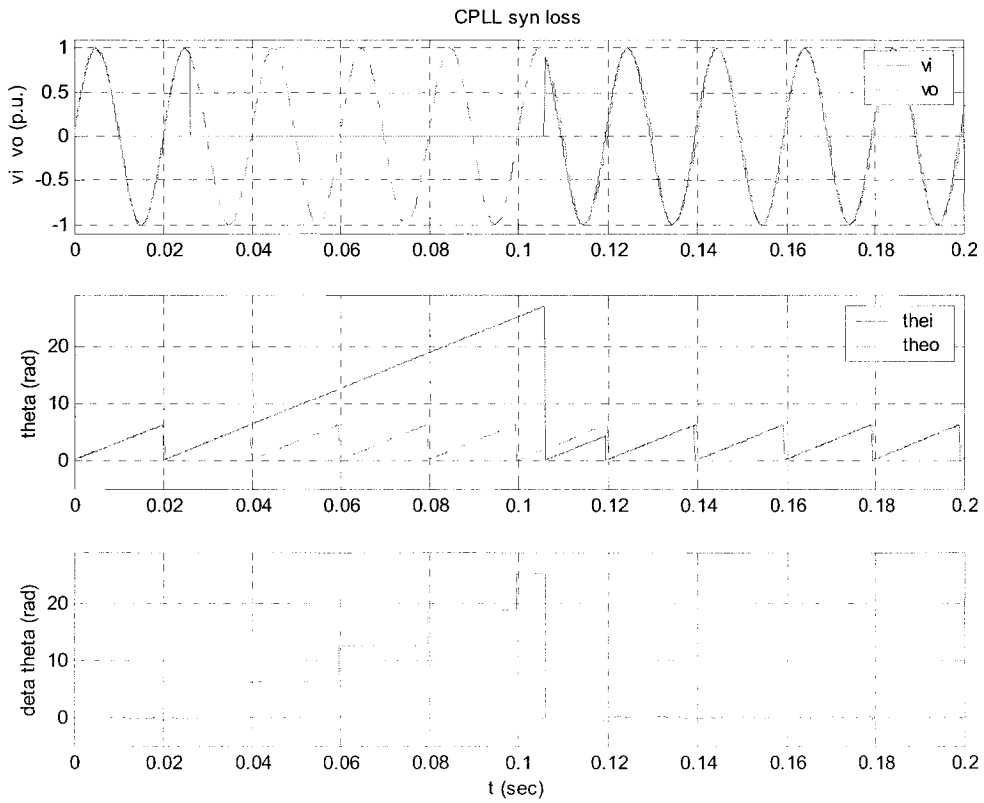

Figure 5.10: Loss of synchronization test for CPLL

5.5b Loss of Synchronization Test for DQPLL

Figure 5.11 shows the internal signals from the DQPLL during a temporary loss of the commutation voltage caused by a single phase fault on the AC commutation bus. The output voltage is able to synchronize with the commutation voltage within 1 cycle (20ms at 50 Hz).

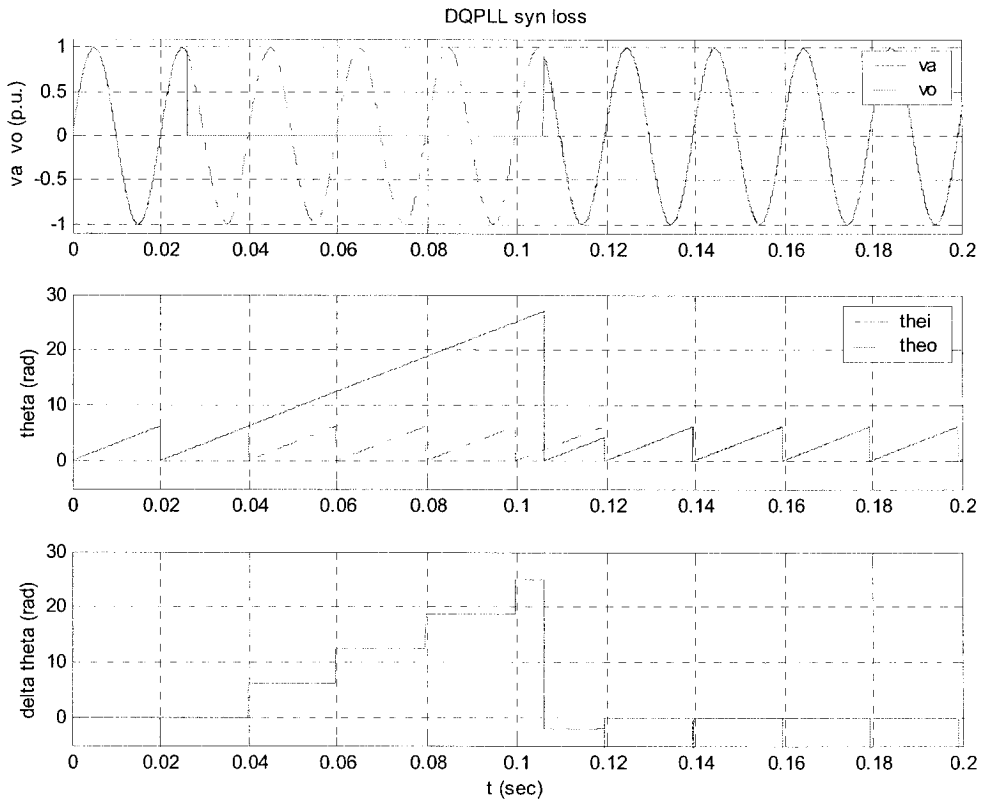

Figure 5.11: Loss of synchronization test for DQPLL

5.5c Loss of Synchronization Test for EPLL

Figure 5.12 shows the internal signals from the EPLL during a temporary loss of the commutation voltage caused by a fault on the AC commutation bus. The post-fault

synchronization dynamics of EPLL show that the output voltage is able to synchronize with the commutation voltage within 1 cycle (20ms at 50 Hz).

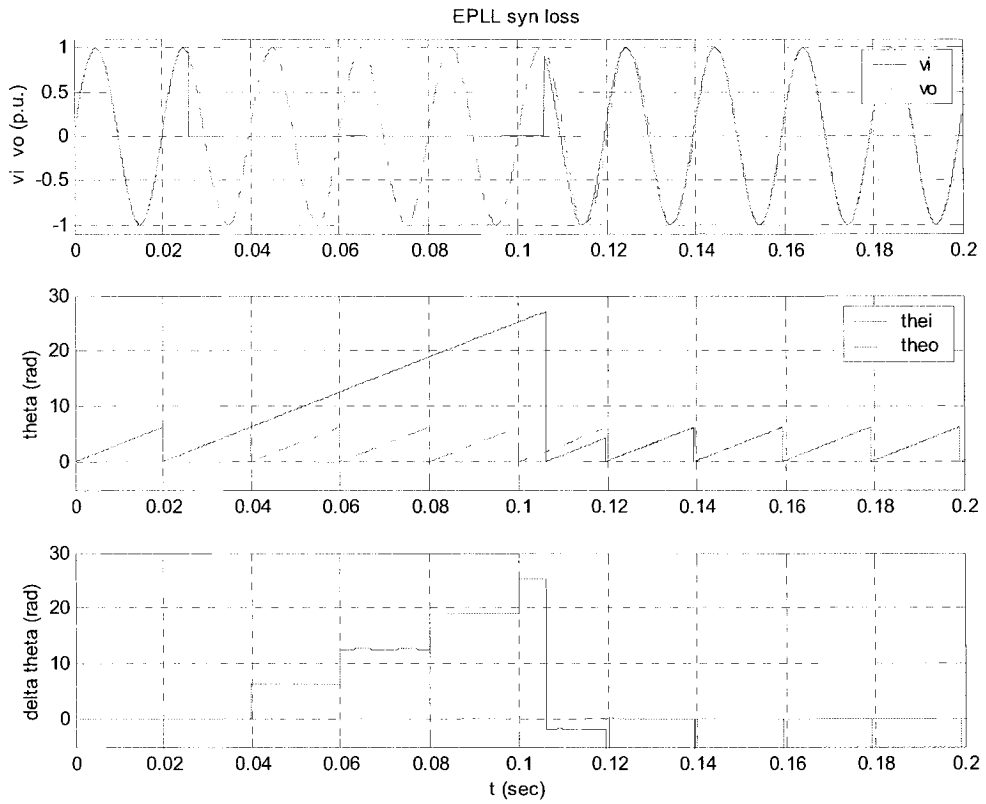

Figure 5.12: Loss of synchronization test for EPLL

5.6 Comparison of PLLs Tests

Figure 5.13-5.15 is a comparison by combining all three PLLs for one test. Figure 5.13 show the DQPLL performs a better anti-distortion characteristic than others.

Figure 5.14 shows the EPLL display a faster response and the DQPLL will lose the synchronization with commutation voltage for a 60 degree phase angle step input.

Figure 5.15 shows all three PLLs can display a good performance for loss of synchronization test.

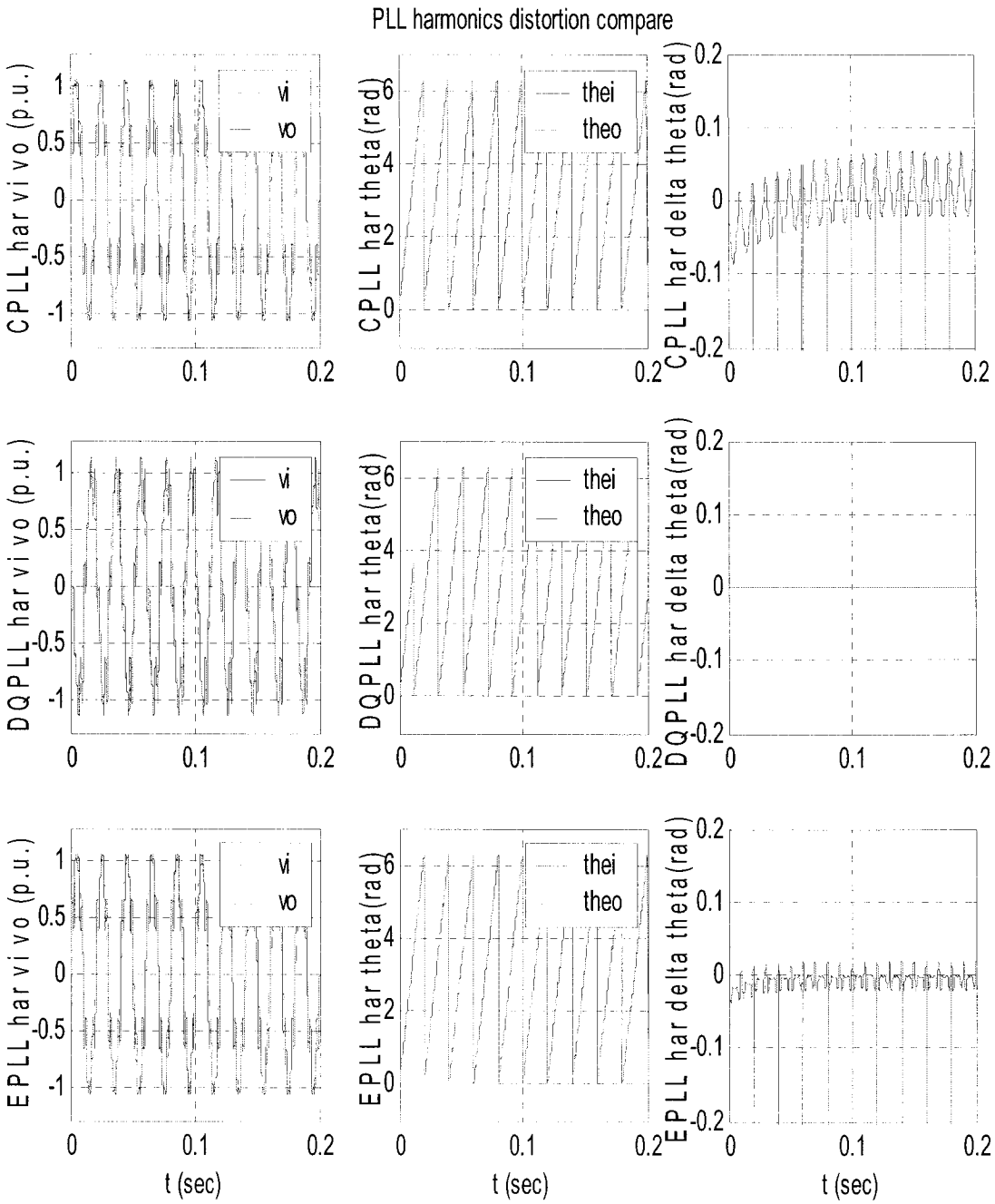

Figure 5.13: Harmonics distortion comparison for PLL

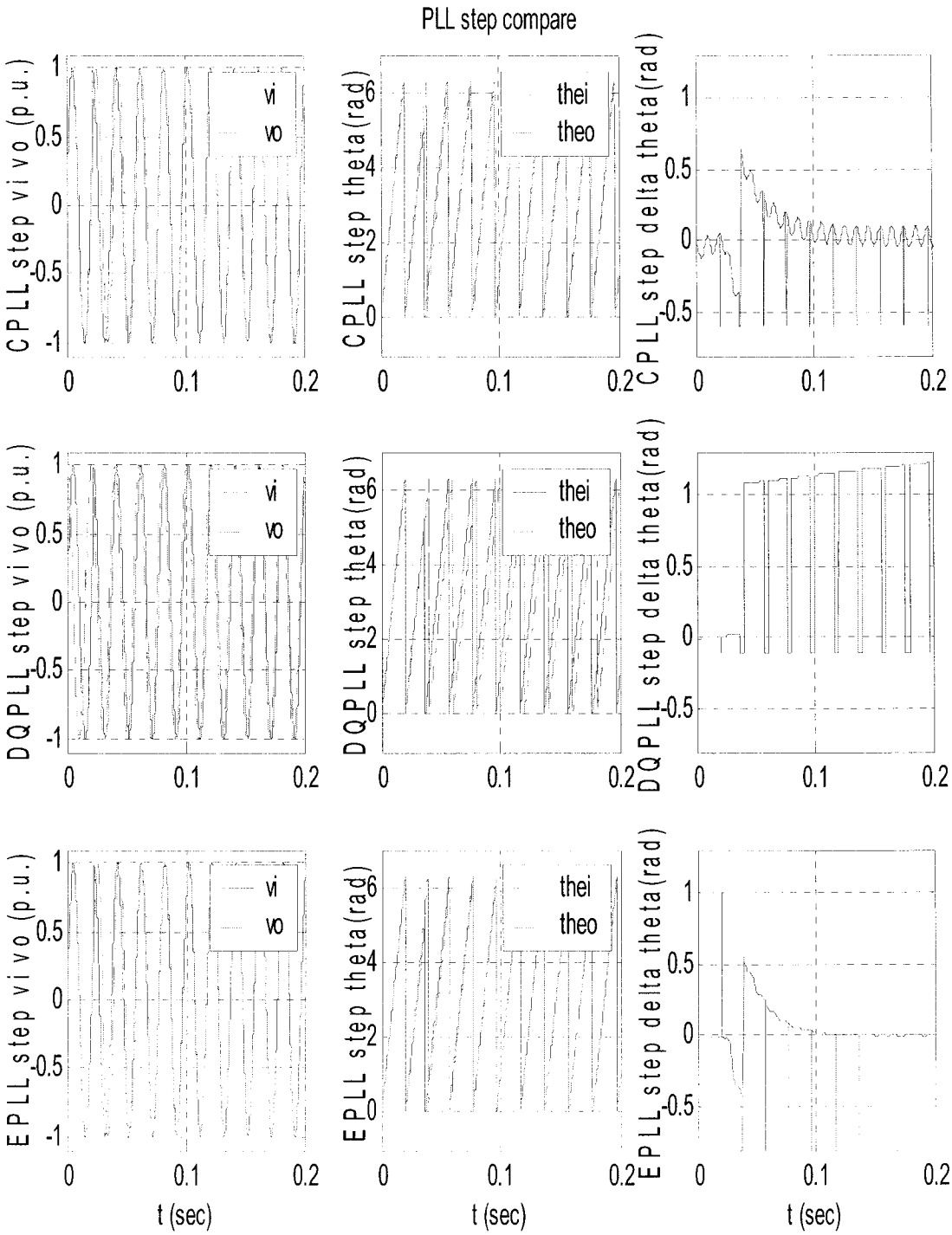

Figure 5.14: Step response comparison for PLLs

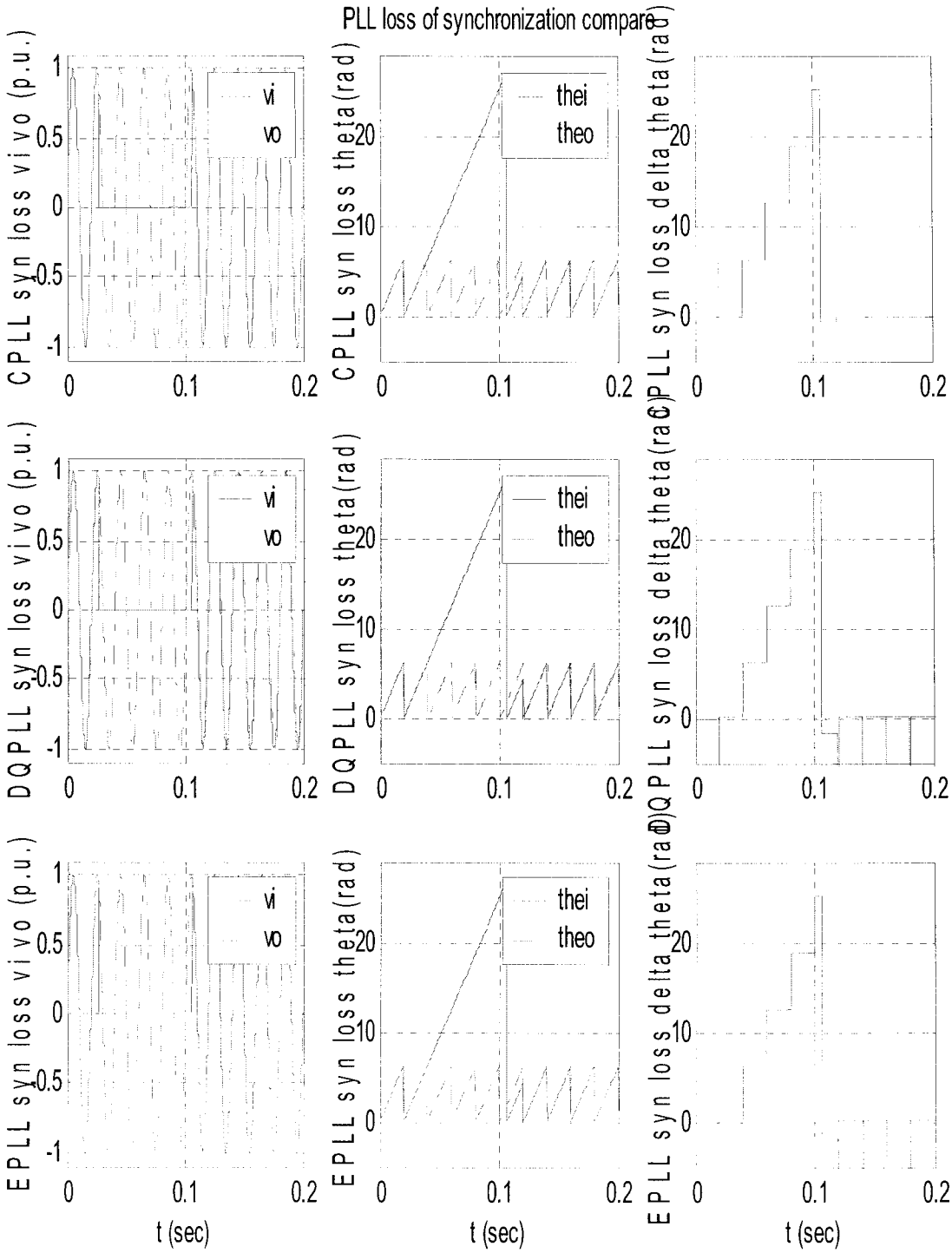

Figure 5.15: Loss of synchronization comparison for PLLs

CHAPTER 6

MODELING OF HVDC RECTIFIER SYSTEM

6.1 Introduction

An HVDC rectifier system operating at a weak AC commutation voltage bus (Figure 6.1) is modeled with EMTP RV simulation package. The HVDC model consists of a HVDC power circuit unit and a current control unit.

6.2 Power Unit of the HVDC Rectifier

The major power component of a HVDC system is the Converter. In this chapter two 3-phase converter bridges are connected in series to form a twelve-pulse converter unit. The converter is fed by converter transformers connected in star/star and star/delta arrangements to form a 12-pulse pair. The valves are protected using snubber circuits. The converter transformers are connected in parallel with the neutral ground on the AC side, the leakage impedance of the transformer is choose to limit short circuit currents through the valves. Due to generation of characteristic and non-characteristic harmonics by the converter, it is necessary to add 11th and 13th single tune AC filter and a high-pass AC filter to commutation bus on AC side and a 12^{th} harmonic DC filter on DC side. A large series rector is used on DC side of the converter to smooth the DC current and for the converter protection from the line surges.

Considering the theoretical analysis of a 12-pulse rectifier bridge, the following formulation is used.

Voltage on DC side: $U_d = 2(1.35U_L \cos\alpha - \frac{3}{\pi} X_r I_d)$ (6-1)

Current on DC side: $I_d = \frac{2(U_{d1} - U_{d2})}{R}$ (6-2)

$$I_d = \frac{2(U_{d1} - U_{d2})}{R}$$
$$R = 2(R_L + R_{SM}) \quad (6\text{-}3)$$
$$\Delta U = U_{d1} - U_{d2} = RI_d$$

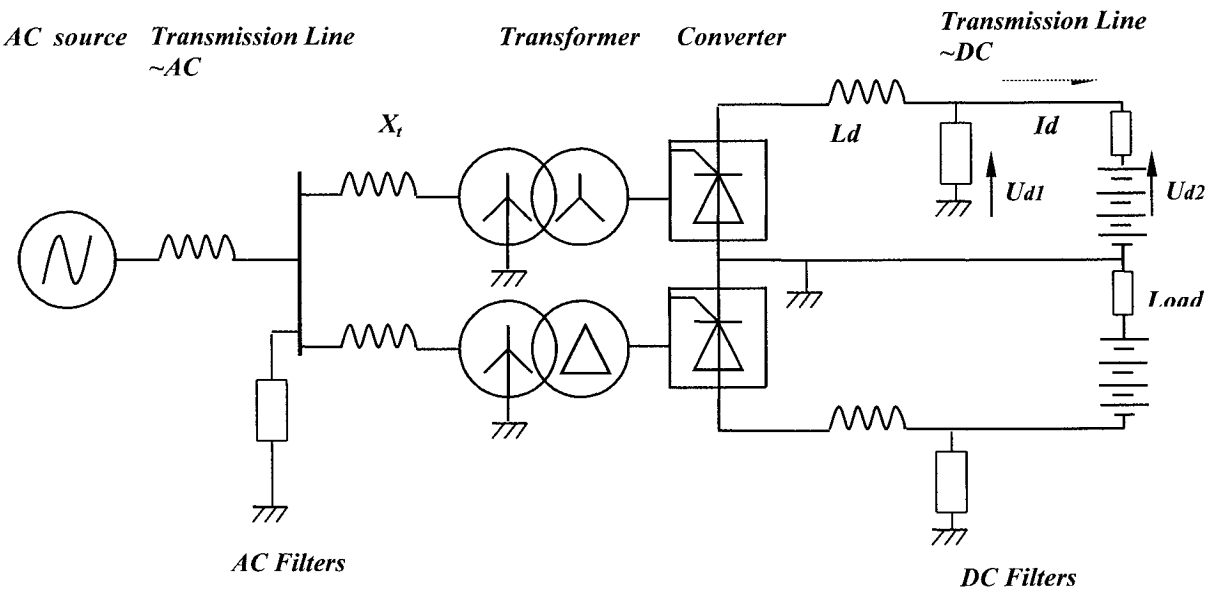

Figure 6.1: Power circuit diagram of a HVDC system

6.3 Control unit and firing pulse generation unit of the HVDC Rectifier

The control system (Figure 6.2) includes a current control loop and a firing pulses generator. The measured DC current, Id, is compared to a current order I_{ref}, and a current error signal is generated. This current error is fed to a PI controller and an alpha order signal is created. Before feeding to firing pulses generator, the alpha order will be modulated to a controlled signal, which will be kept unchangeable during one firing

pulses generating period by a function unit Alpha-Holder which is based on the using of Sample and Hold technology. The output of Alpha Holder is the average value of instantaneous alpha order value for the previous firing period (Figure 6.3). That means only one alpha order will be outputted for each firing period. Moreover this value will be held till the beginning of next firing period whatever transient state the system is in. A firing period measurement unit is required. By this control method, the dynamic speed of control system may be lowed, but it is capable to remove the non-characteristic harmonics in commutation bus during any transient state for a steady state operating. Finally the treated alpha order signal is fed to firing pulses generating unit. The PLL technology is used to extract the fundamental component from the weak AC commutation bus and generate clean 3-phase reference voltage for synchronization purposes. The zero crossover points of these wave forms are used to directly create 12 equi-distant firing pulses during steady-state operation (Figure 6.4, 6.5 and 6.6). And the Flip-Flop Technology is used to modulate the pulses width at 25μs. In this thesis, the function of Alpha Holder is finally disabled as it causes very slow dynamic response speed.

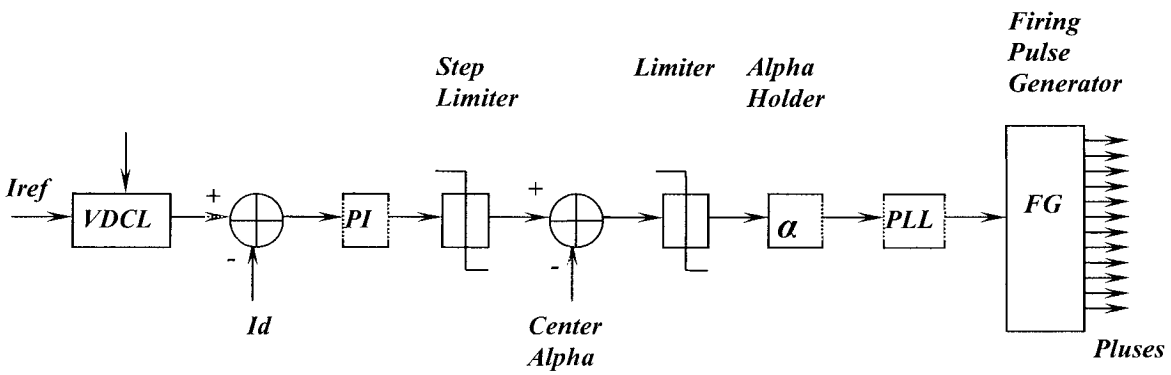

Figure 6.2: Block diagram of current control loop

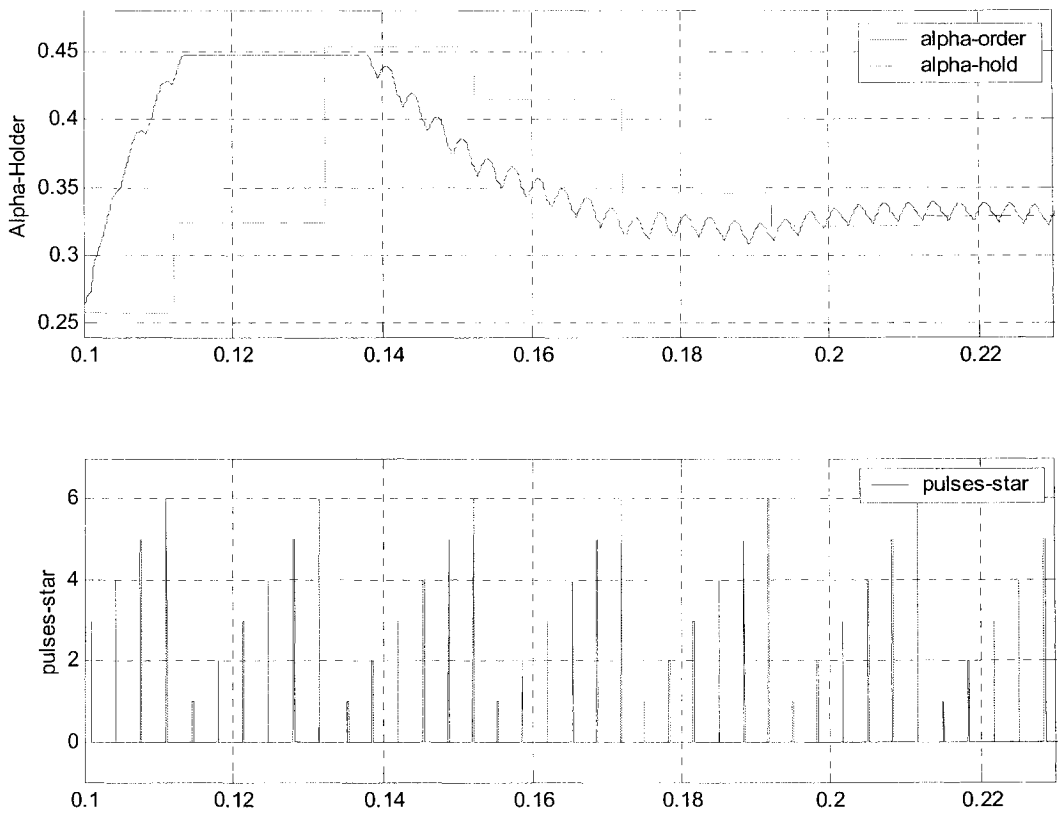

Figure 6.3: Output of Alpha Holder function

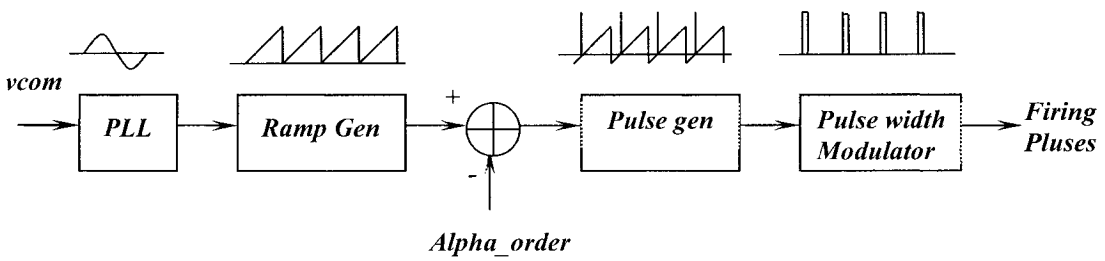

Figure 6.4: Block Diagram of Firing Pulse Generator

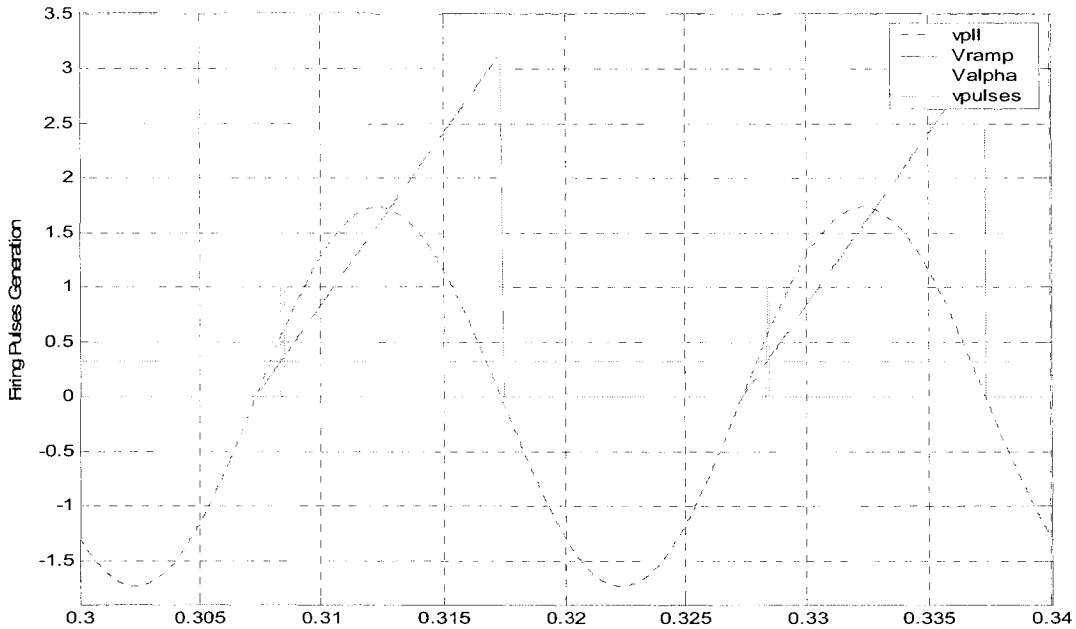

Figure 6.5: Generation of Firing Pulse

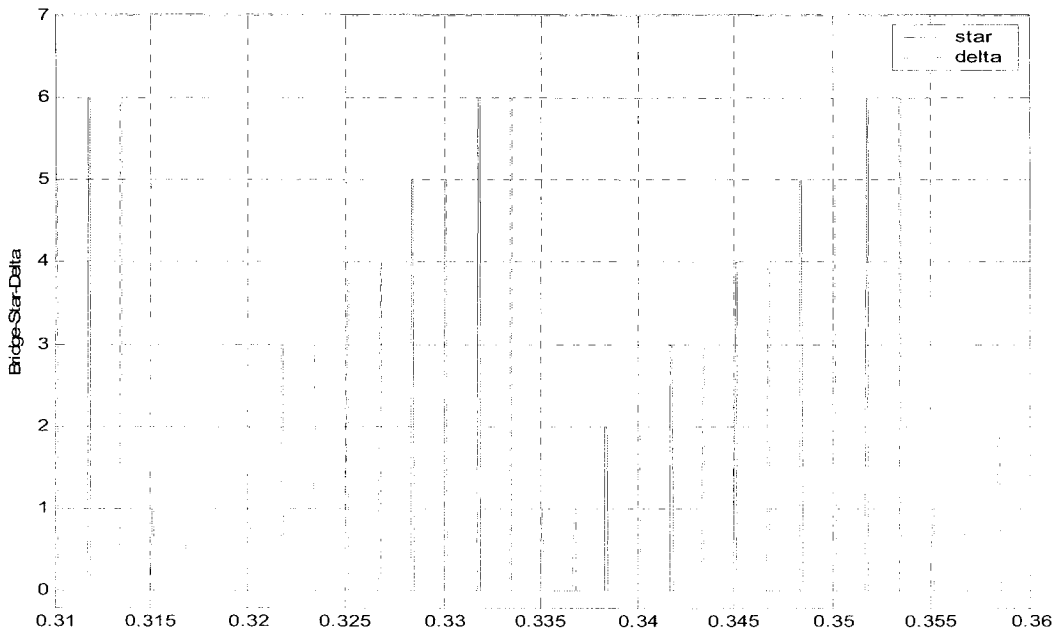

Figure 6.6: Bridge Firing Pulses

CHAPTER 7

SYSTEM PERFORMANCE TESTS

7.1 Introduction

In this section, cases of the HVDC system with the three PLLs are presented. These cases are very informative and show the performance of the system when the firing pulses are released to the converter valves at 0.1 sec. First the initialization results are shown in Figure 7.1 for the CPLL, Figure 7.2 for DQPLL and Figure 7.3 for EPLL. The signals presented for each are:

a) Three phase commutation voltages va, vb and vc,

b) DC current Id, and

c) Rectifier valve voltage showing the firing angle.

The results show that the system achieves full DC current transmission within 100ms (5 cycles at 50Hz) for CPLL, DQPLL and EPLL units.

Furthermore, four types of system performance tests are designed and modeled to analyze and compare three PLLs. The tests presented for each PLL are:

1) Steady-state operation with harmonics pollution in AC commutation bus.

2) Three phase voltage surge

3) Single phase fault

4) Three phase synchronization loss

7.2 System Initialization and Operation

7.2a System Initialization and Operation for CPLL

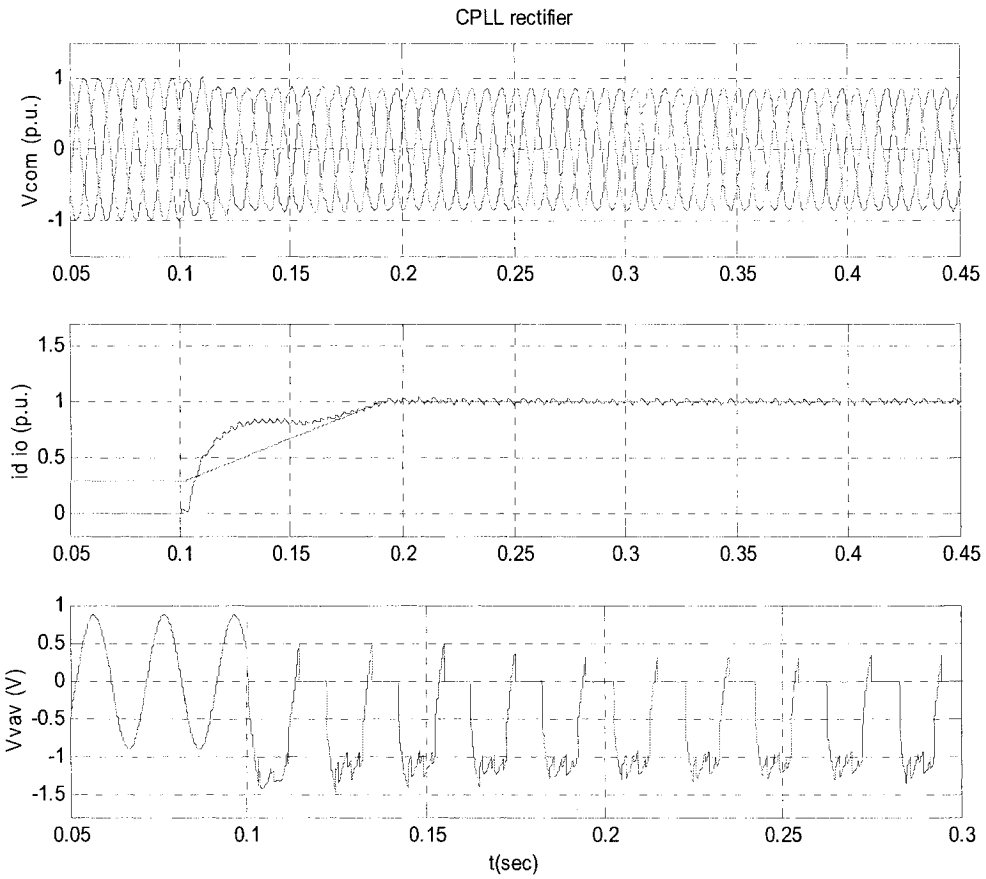

Figure 7.1: System initialization and operation for CPLL

Fig 7.1 shows that DC current can be built after 100ms initialization and the voltage signal in AC side and current signal in DC side only include the characteristic harmonics.

7.2b System Initialization and Operation for DQPLL

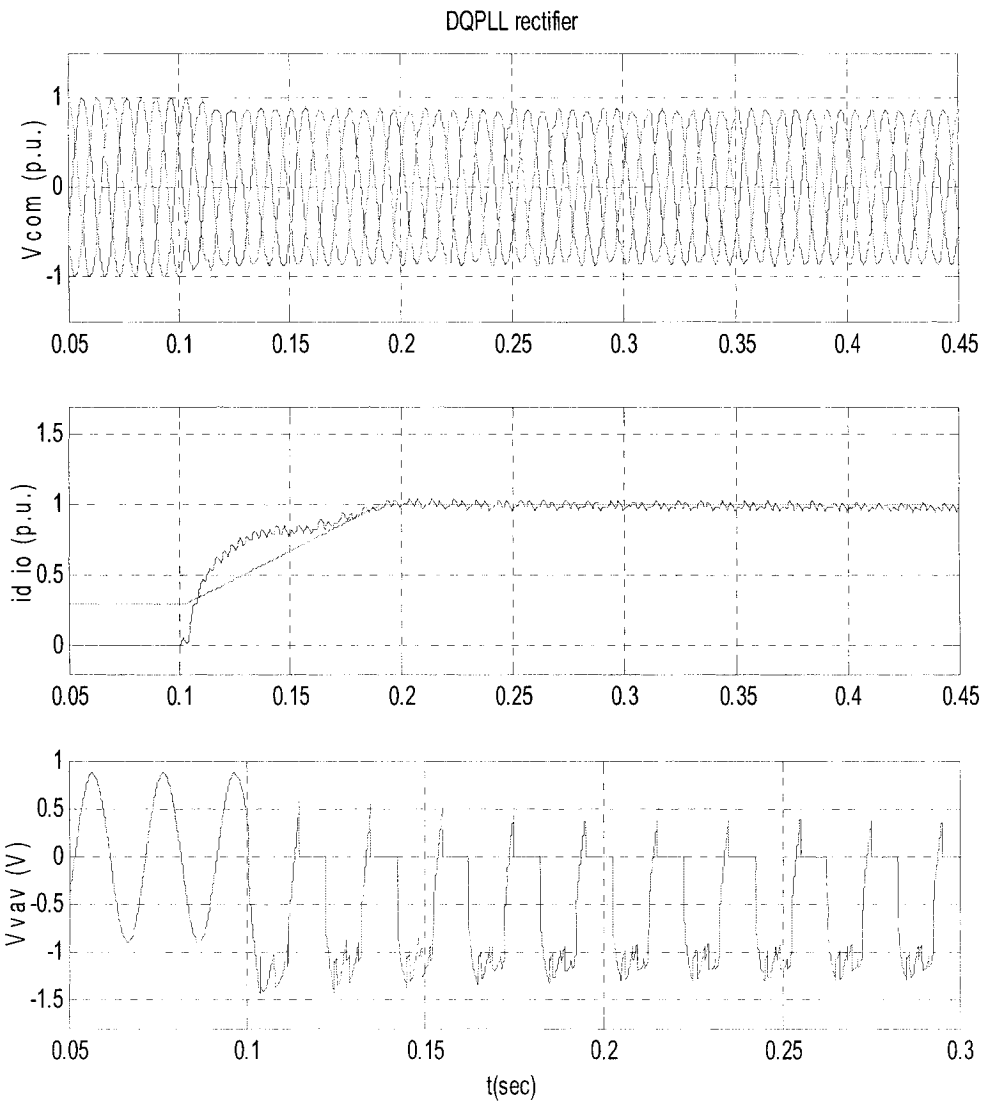

Figure 7.2: System initialization and operation for DQPLL

Fig 7.2 shows similar result, the DC system can be built and operated stably at steady state after initialization in weak system.

7.2c System Initialization and Operation for EPLL

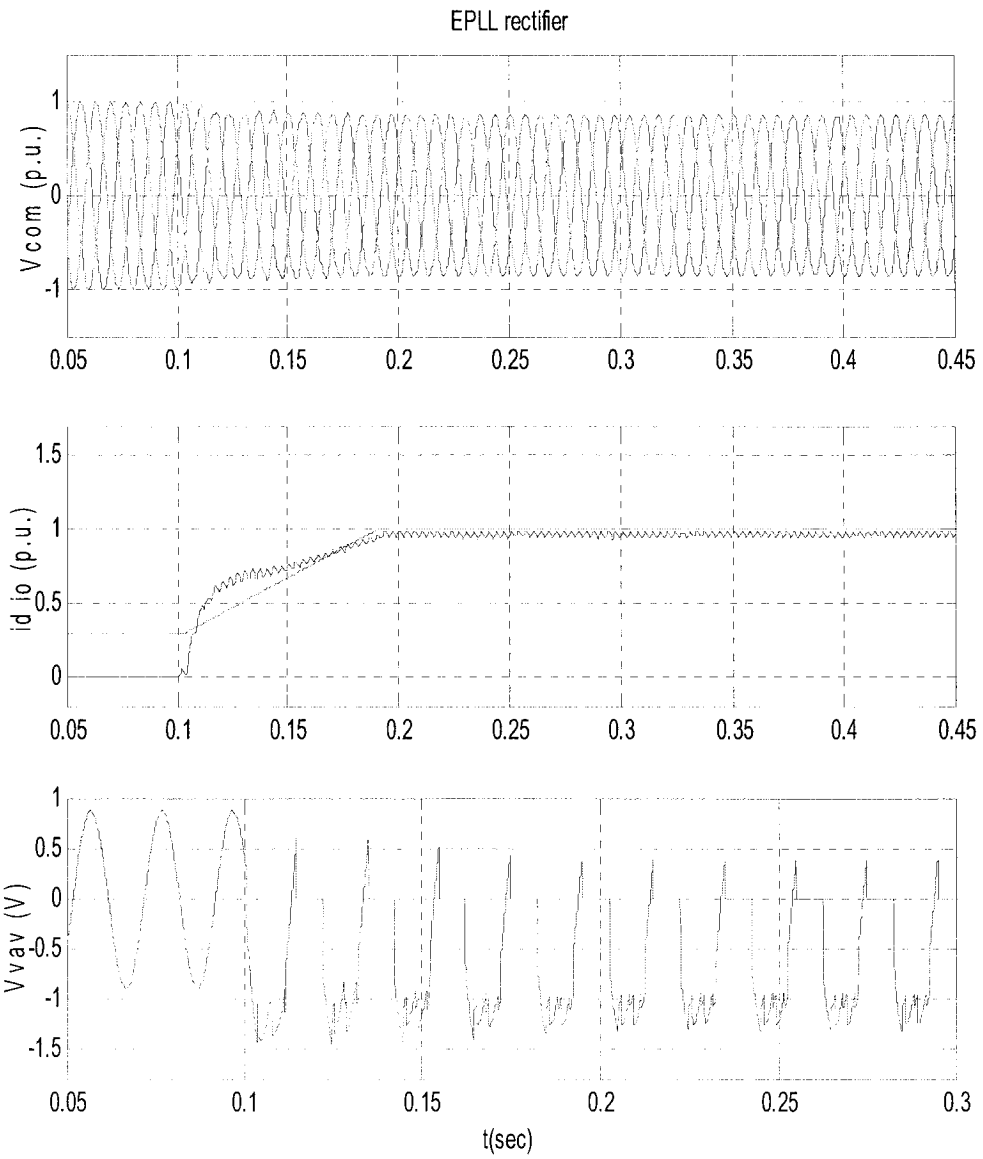

Figure 7.3: System initialization and operation for EPLL

Fig 7.3 shows similar result with CPLL and DQPLL rectifier in weak system.

7.2d Comparison for System Initialization and Operation

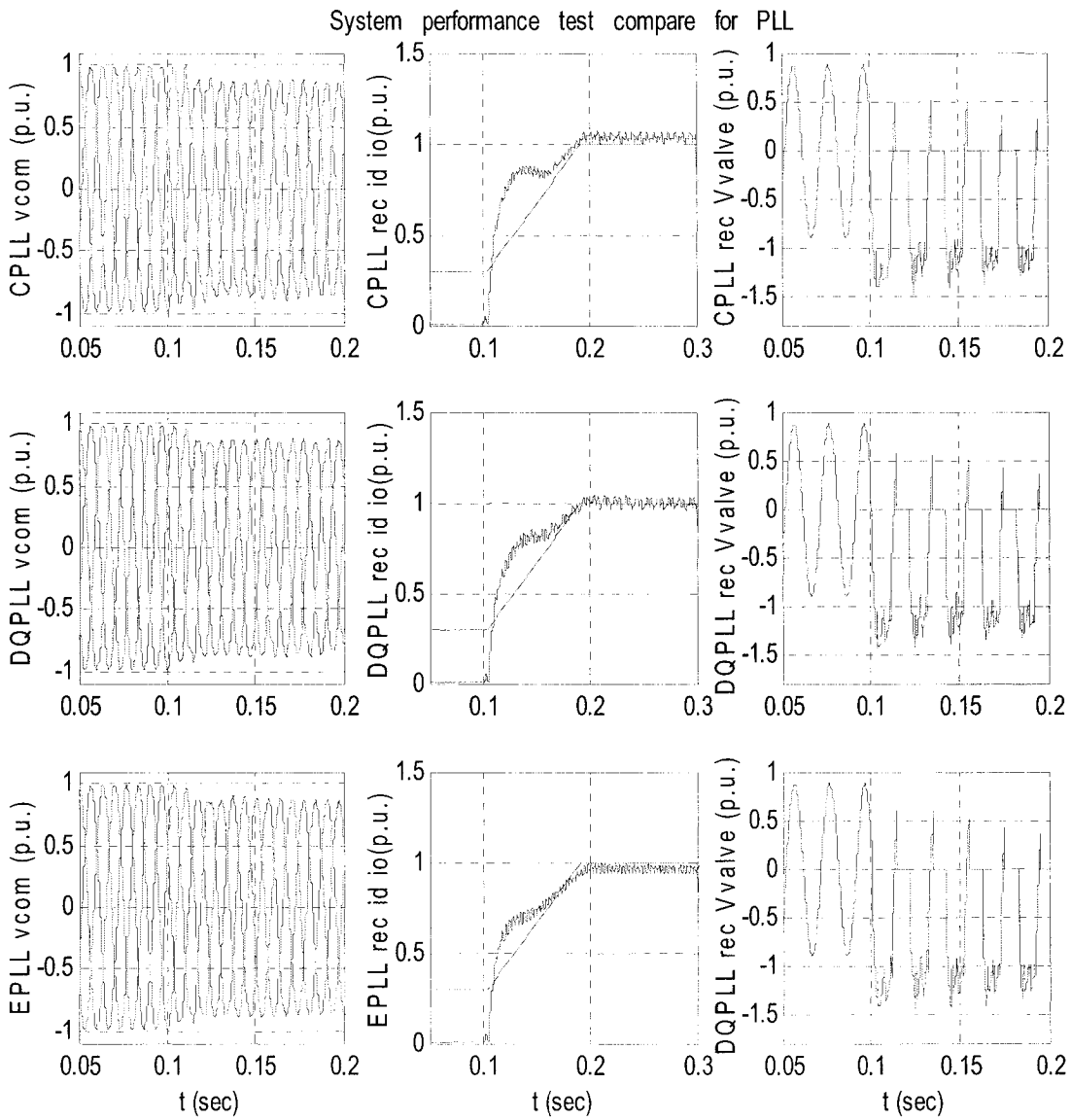

Figure 7.4: Comparison for system Initialization and Operation

In Fig.7.4, three diagrams are combined to one to compare the different PLLs. It shows that EPLL rectifier presents the fast response during initialization.

7.3 System Performance Tests

7.3.1 Steady Operation with Harmonics Pollution in AC Commutation Bus (Harmonics distortion)

In this test, the AC commutation bus is distorted by harmonics pollution (7% THD). Two types of rectifier system, with PLL and without PLL, for each rectifier are modeled. The results are shown in Figure 7.5 for the CPLL, Figure 7.6 for DQPLL and Figure 7.7 for EPLL.

7.3.1a Steady State Operation Test for CPLL Rectifier

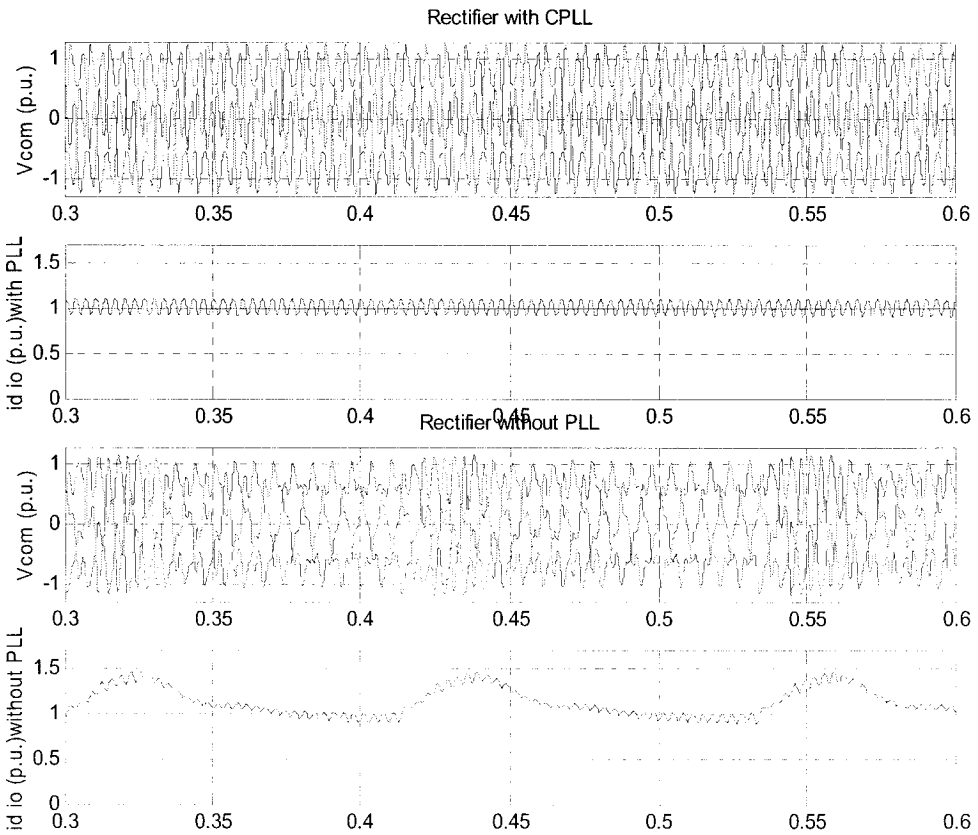

Figure 7.5: Steady state operation test for CPLL rectifier

Fig. 7.5 shows that the rectifier with CPLL works when the AC commutation bus (in a weak AC system) is distorted by heavy harmonics. However, the DC side current in rectifier without PLL will include abnormal harmonics and the signal is unstable. The harmonics injection occurs for both cases.

7.3.1b Steady State Operation Test for DQPLL Rectifier

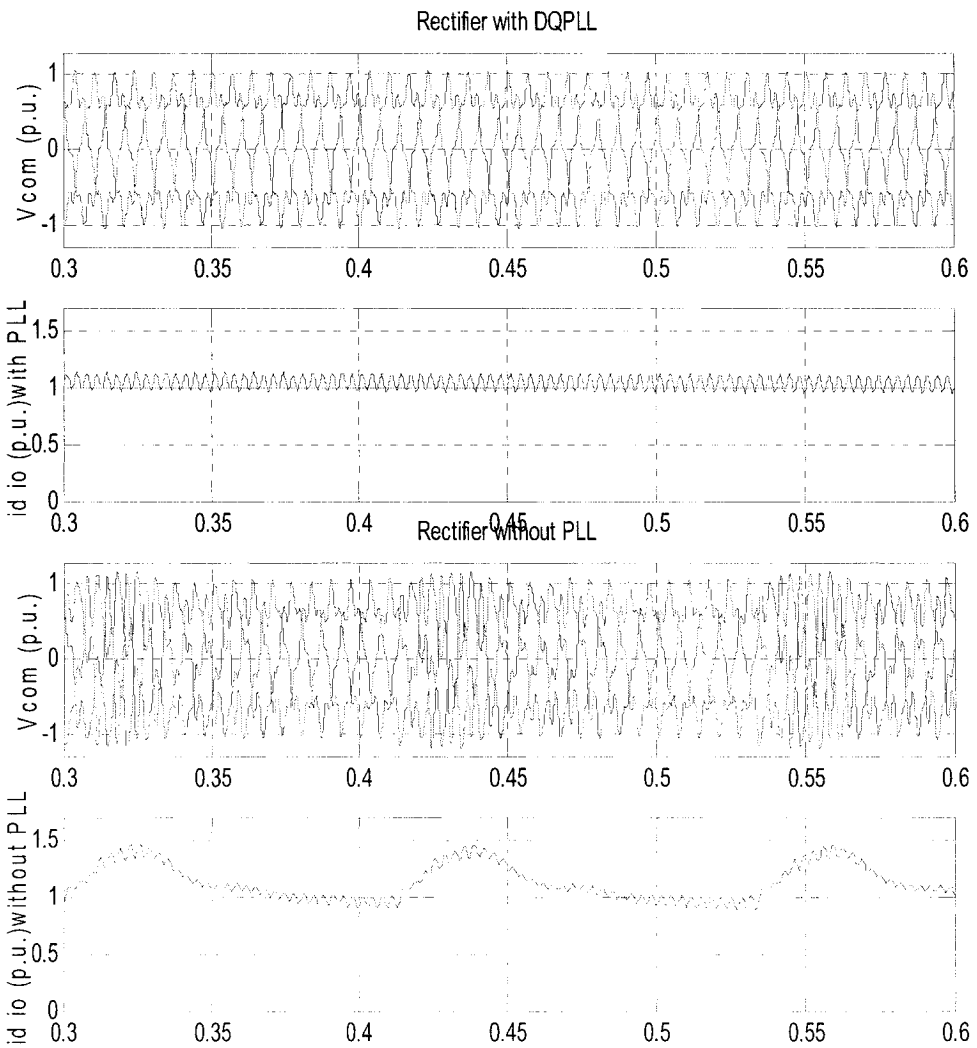

Figure 7.6: Steady state operation test for DQPLL rectifier

Fig. 7.6 shows the similar results that the rectifier with DQPLL works but injects harmonics in AC side when the AC commutation bus (in a weak AC system) is distorted by heavy harmonics. However, when disable PLL function, the rectifier will output abnormal harmonics and cause harmonic unstable in DC current.

7.3.1c Steady State Operation Test for EPLL Rectifier

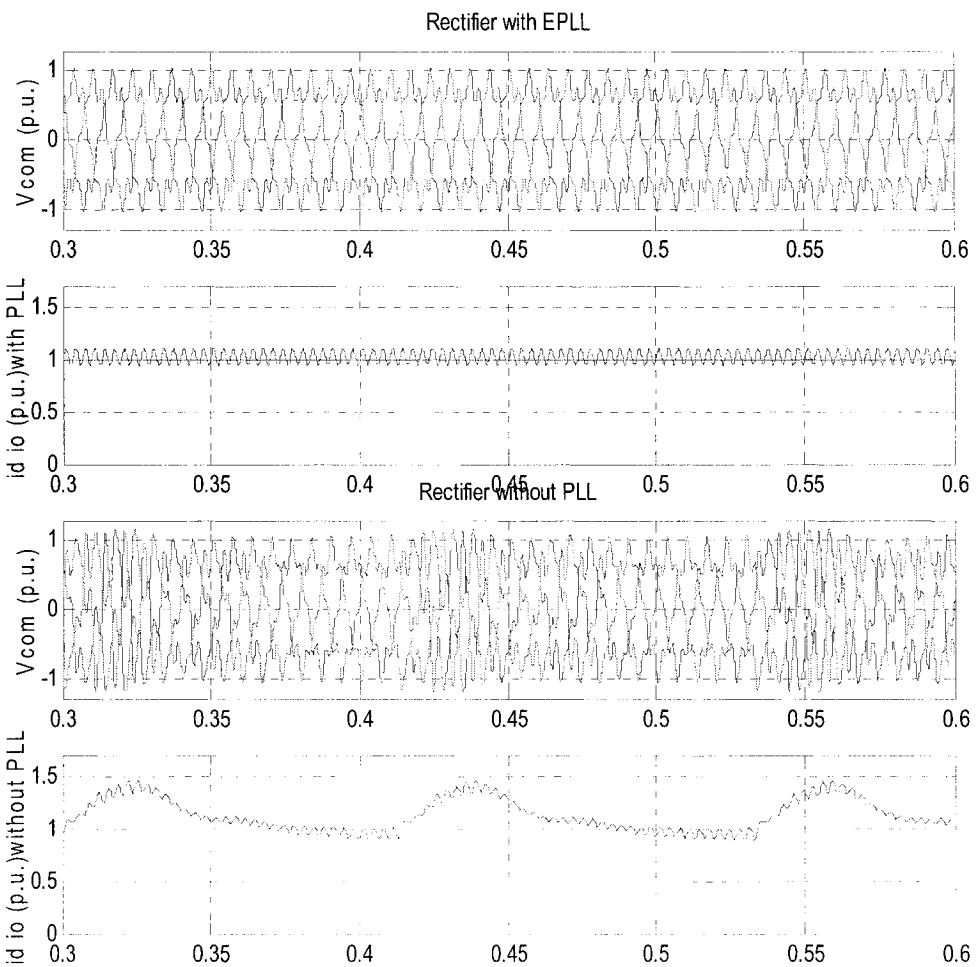

Figure 7.7: Steady state operation test for EPLL rectifier

Fig. 7.7 shows the similar results with DQPLL.

7.3.2 Three Phase Voltage Surge Test (Magnitude step)

In this test, three phase voltage surge tests are designed to simulate the commutation bus voltage magnitude change caused by three phase transient AC load reject. The commutation bus voltage change (+5%) is set at the time 0.3 sec. The results are shown in Figure 7.8 for the CPLL, Figure 7.9 for DQPLL and Figure 7.10 for EPLL.

7.3.2a Three Phase Voltage Surge for CPLL Rectifier

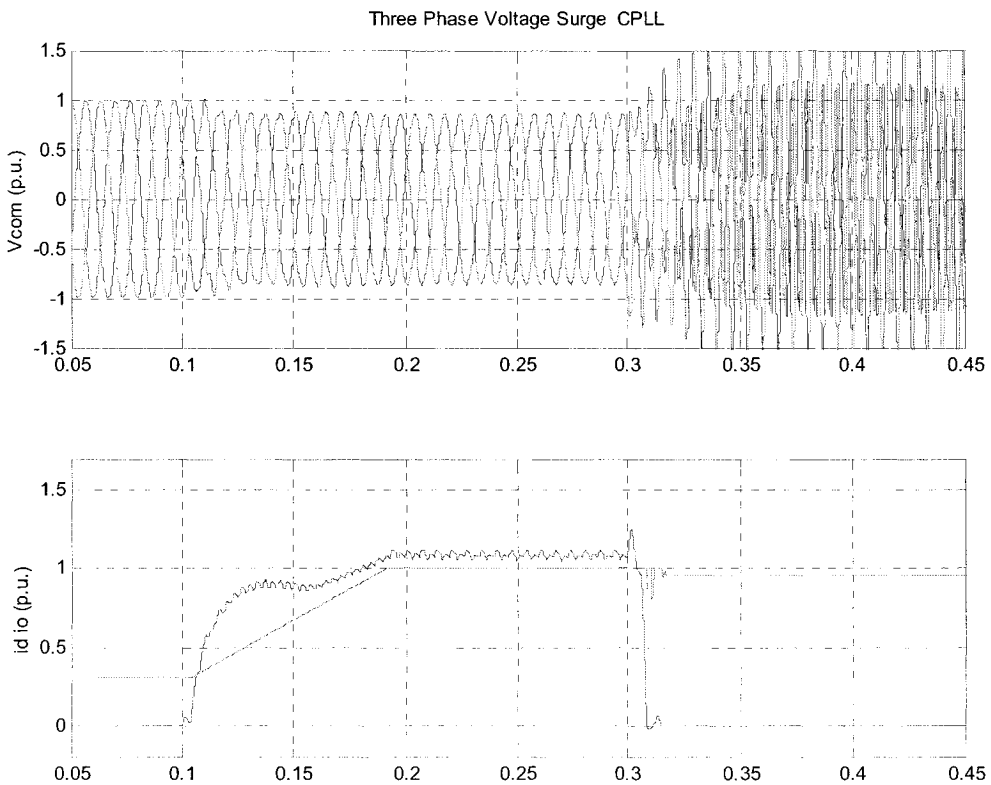

Figure 7.8: Three phase voltage surge for CPLL rectifier

Fig. 7.8 shows that the rectifier with CPLL fails to fire valves when the input commutation bus voltage has a magnitude jump. Meanwhile, the rectifier system injects harmonics to weak AC system.

7.3.2b Three phase Voltage Surge for DQPLL Rectifier

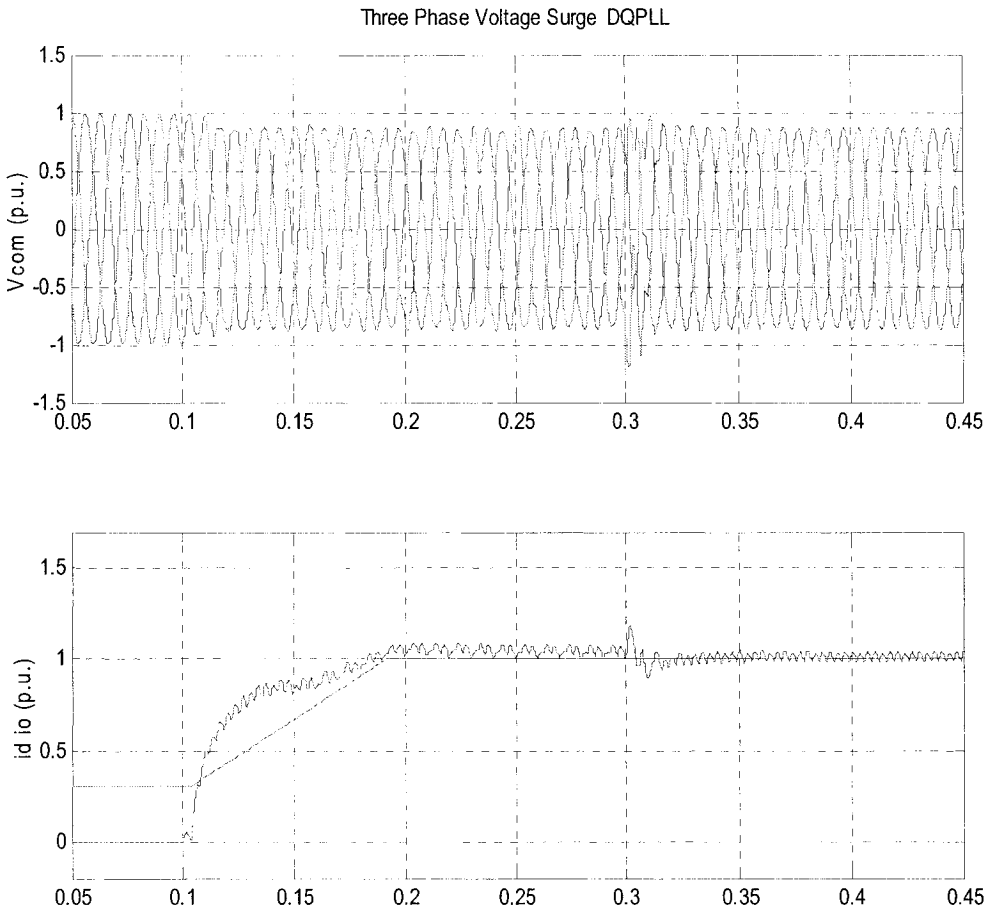

Figure 7.9: Three phase voltage surge for DQPLL rectifier

Fig. 7.9 shows that the rectifier with DQPLL is capable to operate stably at a new steady state when the input commutation bus voltage has a magnitude jump.

7.3.2c Three Phase Voltage Surge for EPLL

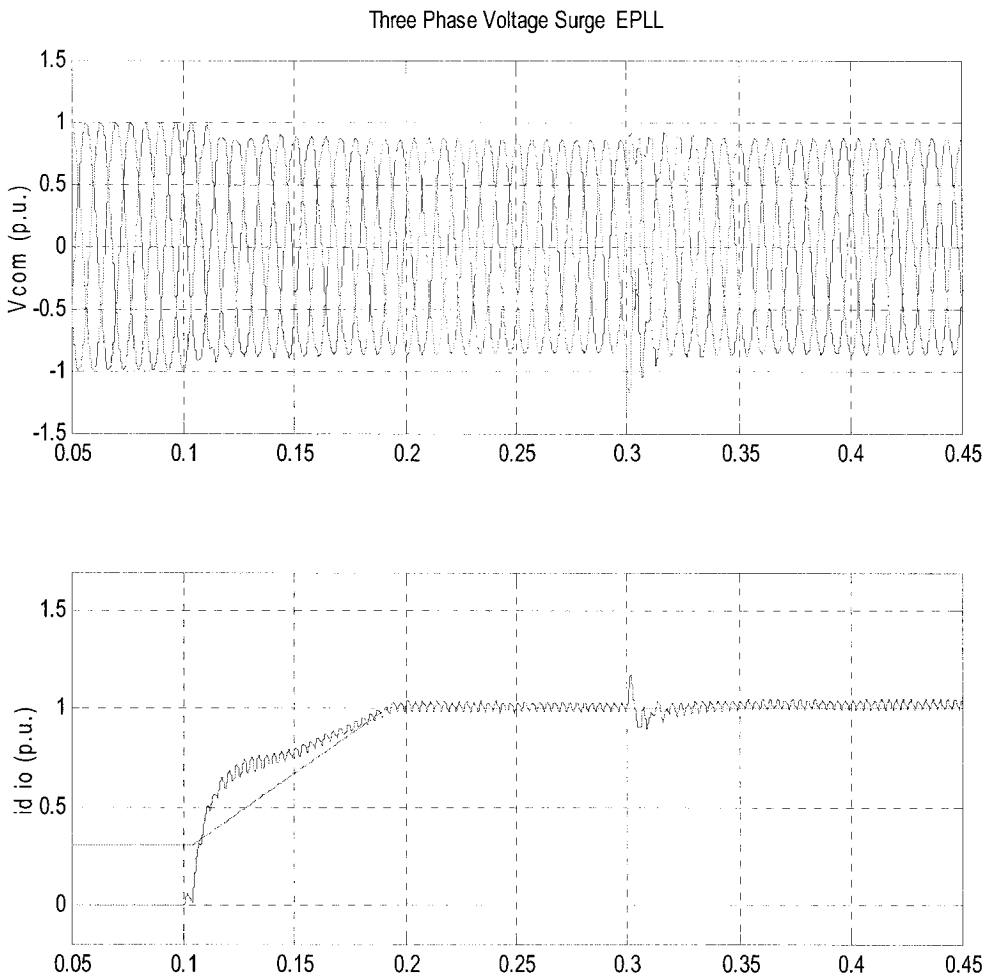

Figure 7.10: Three phase voltage surge for EPLL rectifier

Fig. 7.10 shows the similar result that the rectifier with EPLL is capable to operate stably at a new steady state when the input commutation bus voltage has a magnitude jump.

7.3.3 Single Phase Fault Test (Phase step)

In this test, a single phase non-metal short circuit fault is set at 0.3sec in AC commutation bus. The single phase fault will cause phase shift and voltage unbalance. The results are shown in Figure 7.11 for the CPLL, Figure 7.12 for DQPLL and Figure 7.13 for EPLL.

7.3.3a Single Phase Fault for CPLL rectifier

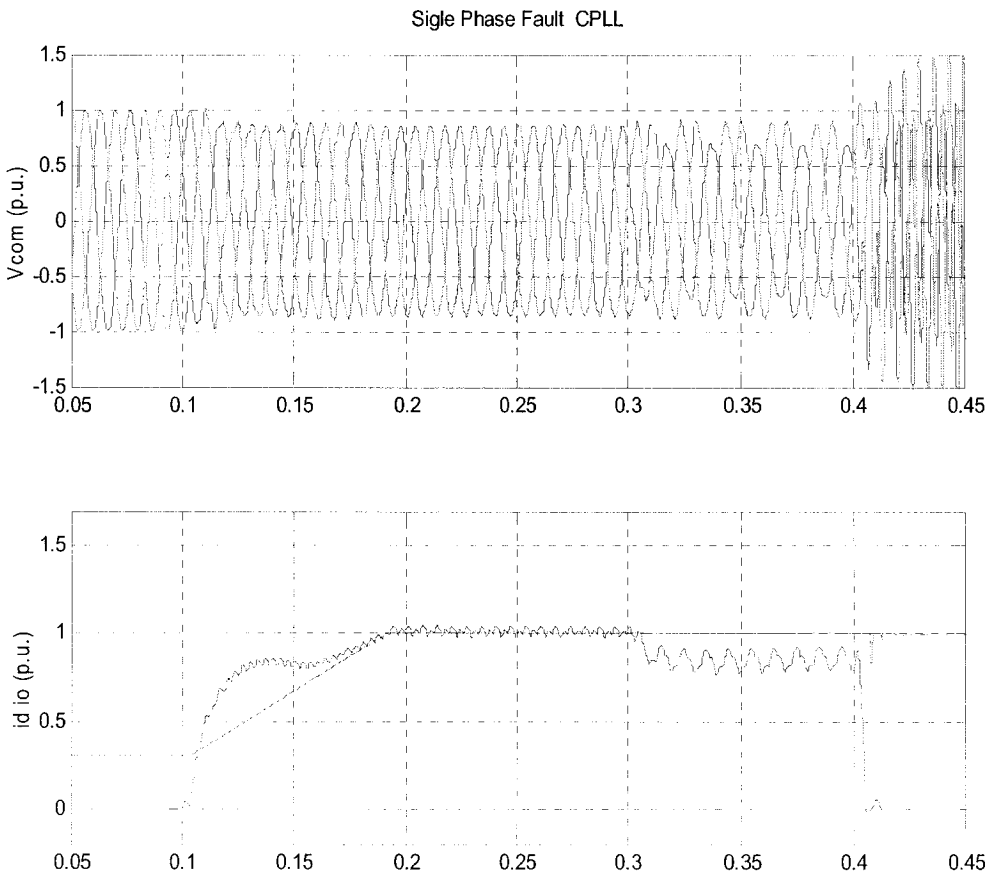

Figure 7.11: Single phase fault for CPLL rectifier

Fig 7.11 shows that a single phase fault results in a phase jump in fault phase and the CPLL rectifier can not recover from transient fault after 0.4sec. The rectifier system

fails to fire valves and DC current can not be built. However, if the impedance of short circuit point is big enough (>150mH), the system can work well. This is because that the phase jump amplitude depends on the impedance of circuit.

7.3.3b Single phase fault for DQPLL rectifier

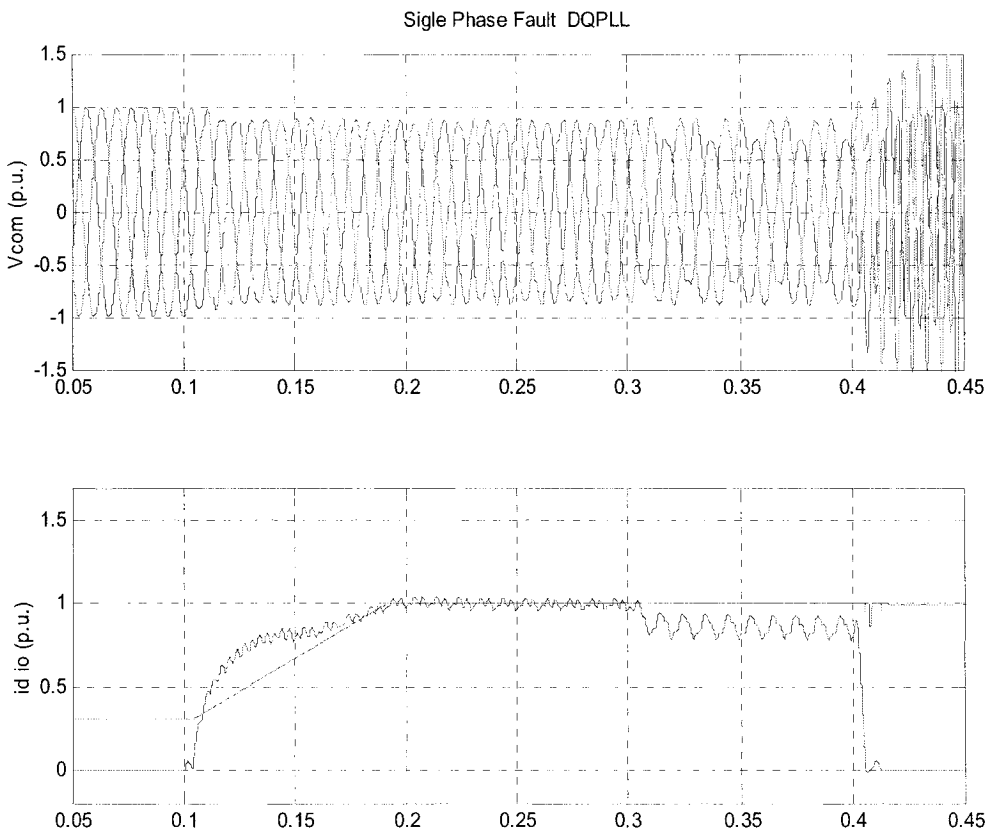

Figure 7.12: Single phase fault for DQPLL rectifier

Fig. 7.12 shows that the CPLL rectifier can not recover from a single phase transient fault after 0.4sec. The rectifier system fails to fire valves and DC current can not be built. Further test shows the similar result that the system can work well if the impedance of short circuit point is big enough.

7.3.3a Single Phase Fault for EPLL Rectifier

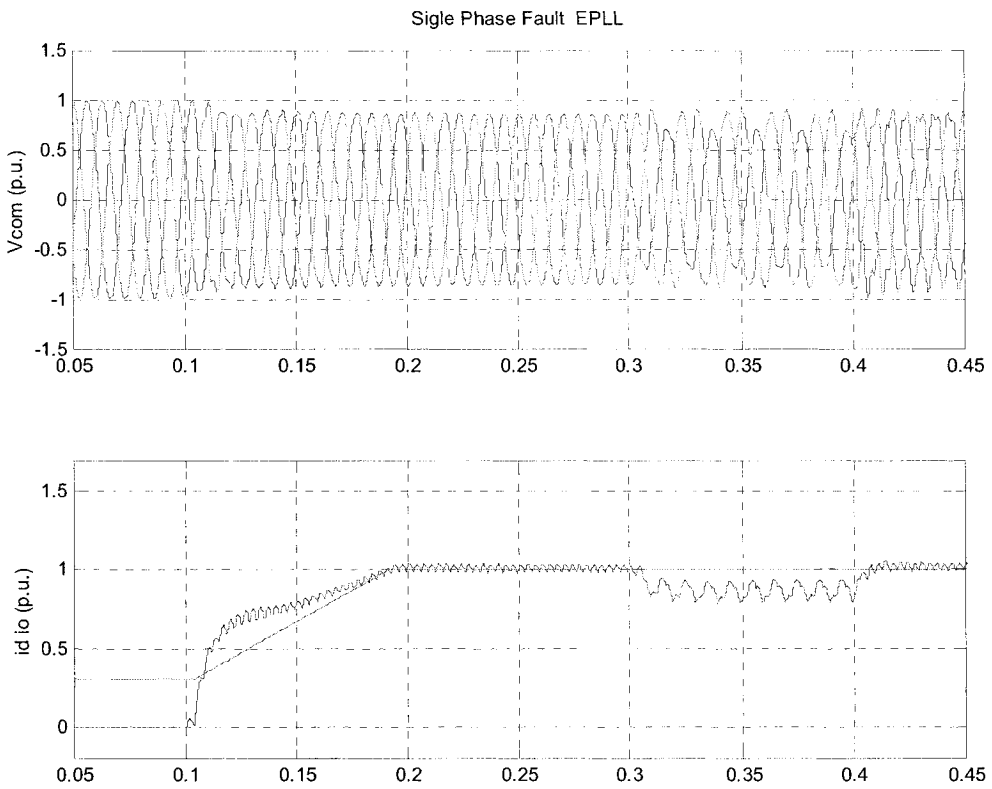

Figure 7.13: Single phase fault for EPLL rectifier

In Fig. 7.13, the rectifier with EPLL can recover and works well from a transient single phase fault. This shows that the EPLL has a good transient response.

7.3.4 Three Phase Fault Tests (Loss of synchronization)

In this test, a three phase metal short circuit fault, start at 0.3sec and end at 0.4sec, is set on AC commutation bus. This test can simulate the opening of the three phase recloser. During the loss of synchronization, the valves firing function will keep free running at center operation frequency (50Hz) which may be different with actual system

frequency (50.2Hz). The results are shown in Figure 7.14 for the CPLL, Figure 7.15 for DQPLL and Figure 7.16 for EPLL.

7.3.4a Three Phase Fault for CPLL Rectifier

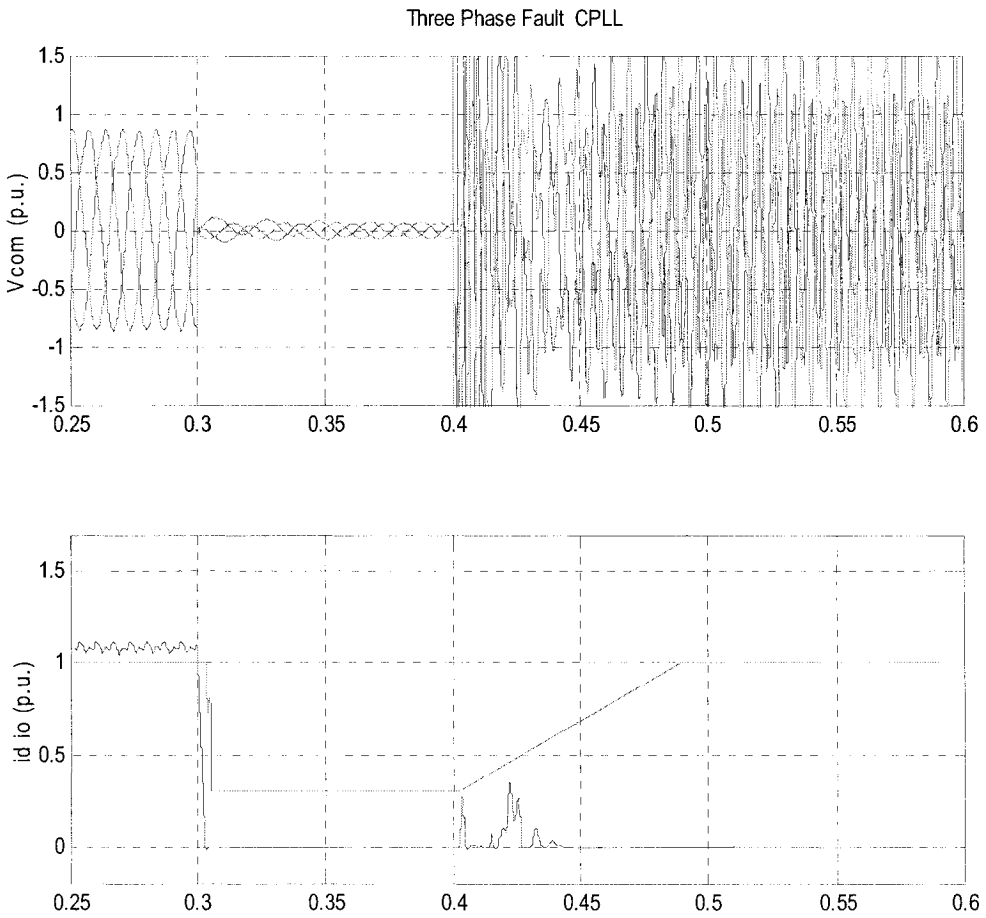

Figure 7.14: Three phase fault for CPLL rectifier

Fig. 7.14 shows that the CPLL rectifier can not recover from a three phase transient fault after 0.4sec. The rectifier system fails to fire valves and DC current can not be built.

7.3.4b Three phase fault for DQPLL rectifier

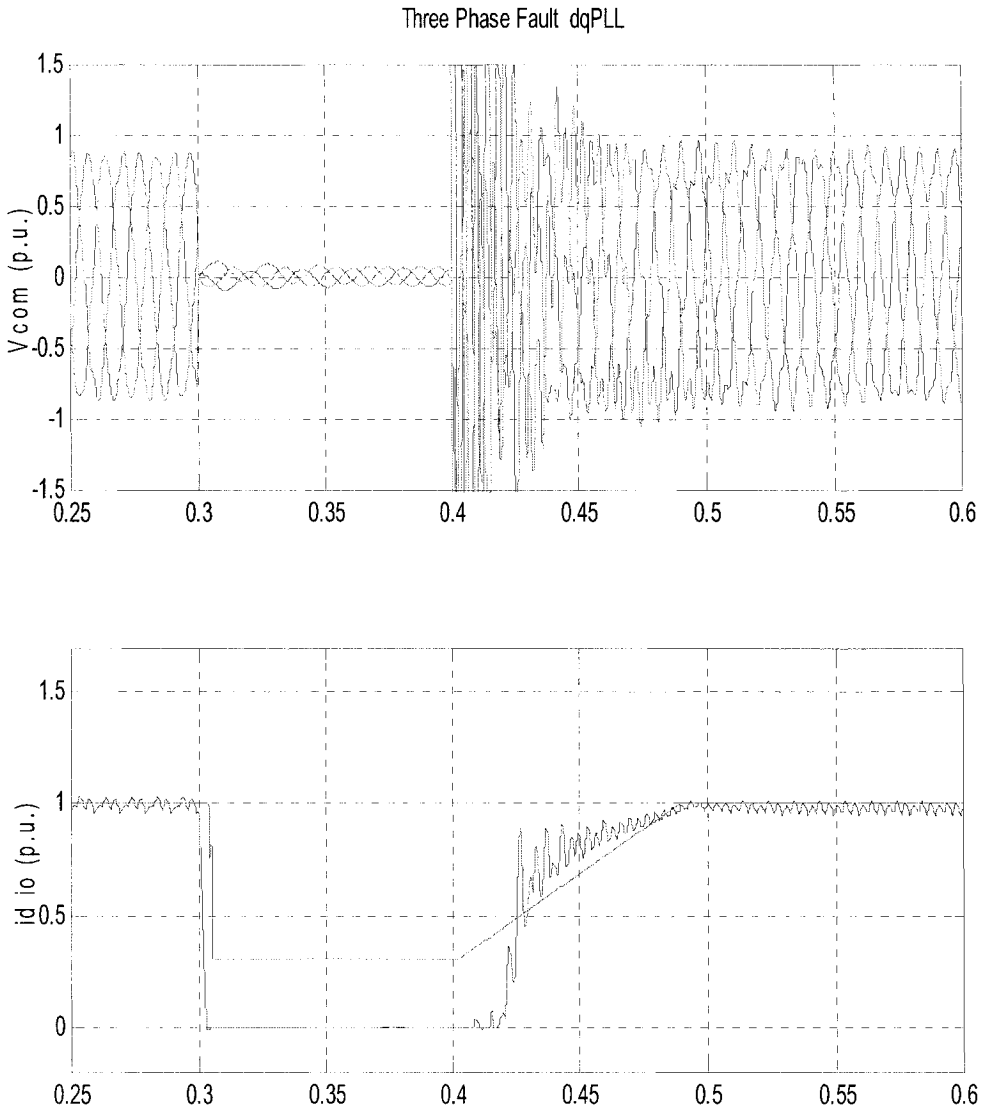

Figure 7.15: Three phase fault for DQPLL rectifier

In Fig. 7.15, the rectifier with DQPLL can recover and works well from a transient three phase fault within 100ms (5 cycles at 50Hz).

7.3.4c Three Phase Fault for EPLL Rectifier

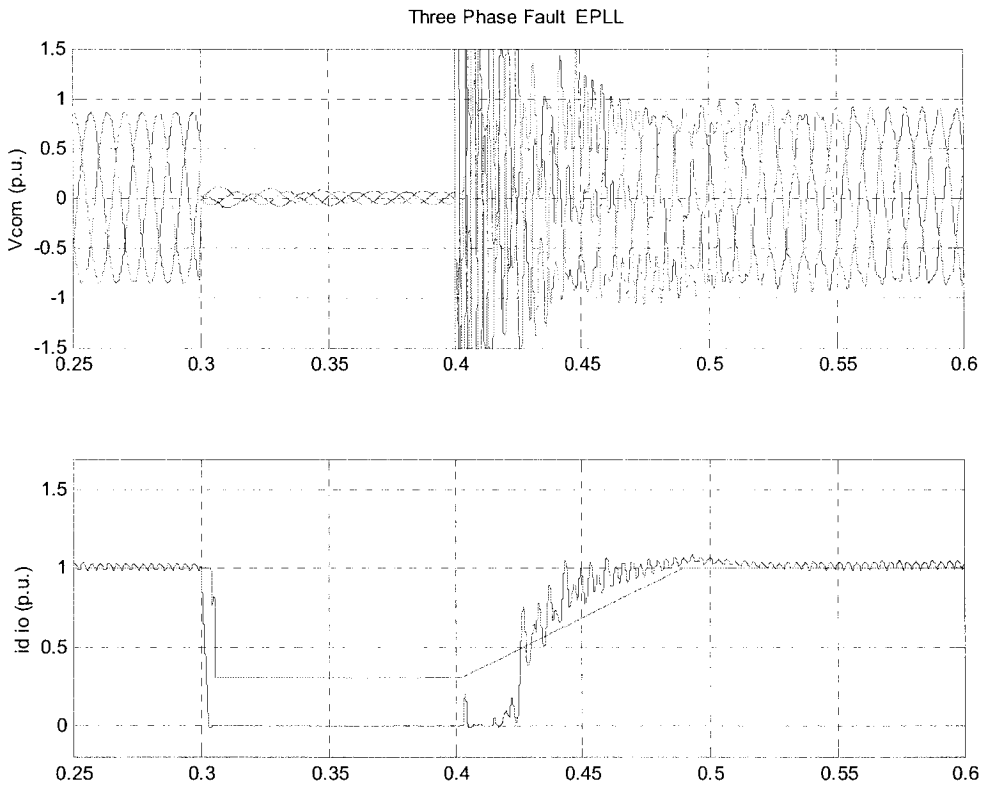

Figure 7.16: Three phase fault for EPLL rectifier

Fig. 7.16 shows the similar results with DQPLL rectifier that the rectifier with EPLL can recover and works well from a transient three phase fault within 100ms (5 cycles at 50Hz).

7.4 EPLL Rectifier System Performance with Current Step

In comparison of all performance tests, the EPLL rectifier can work well for both transient and steady state operation. Figure 7.17 shows the result that EPLL rectifier is capable of operating stably when a current step (20% magnitude drop, start at 0.3sec and

end at 0.4sec) is set. Vd represents DC side voltage and Vvav is the voltage crossing the valve.

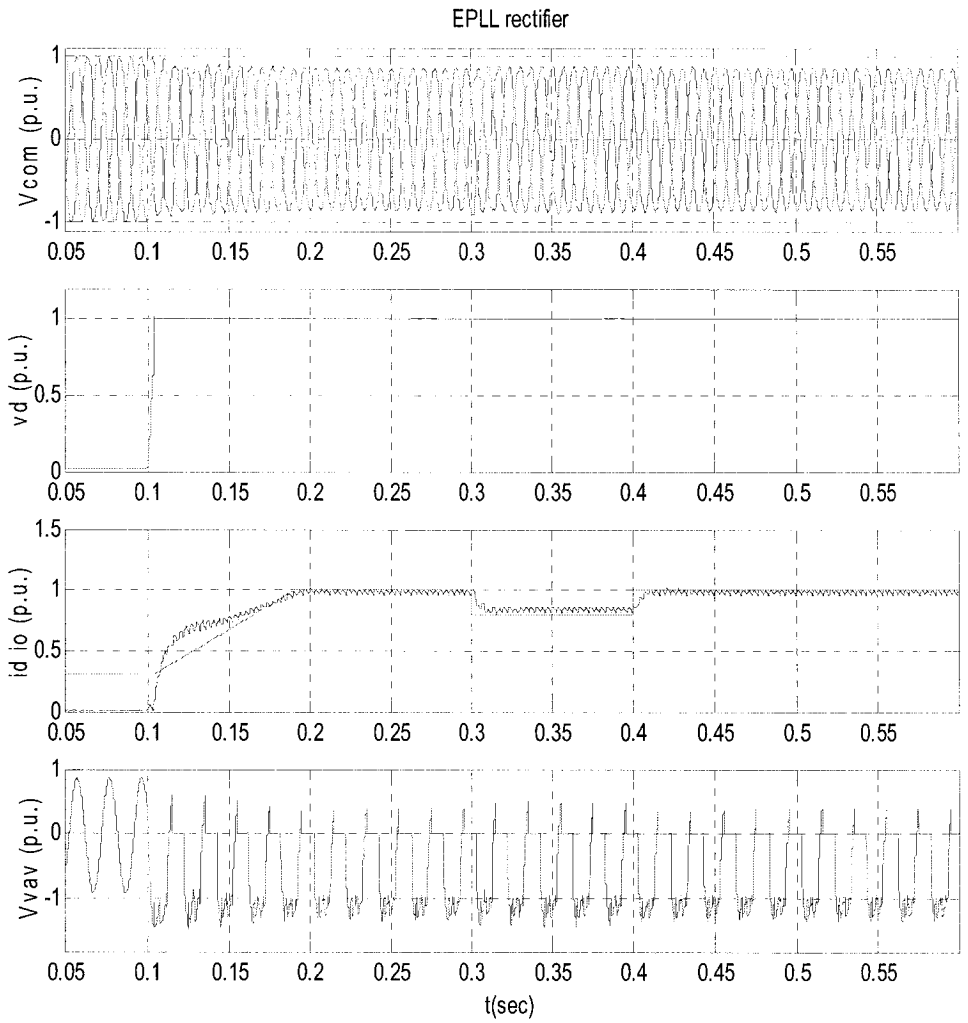

Figure 7.17: EPLL rectifier system performance with current step

Fig. 7.17 presents that the EPLL rectifiers can response well for a current order change. The system can transfer to a new steady state operation current within 1 cycle (at 50 Hz).

CHAPTER 8

CONCLUSIONS

This thesis provides performance results of three firing pulse generating units based on varying PLLs which can be used for HVDC converter systems operating with a weak AC system. A performance comparison between the three units showed that both DQPLL and EPLL are equally capable of operation in the weak AC system with high pollution/harmonics distortion in the commutation voltage but the CPLL shows a poor performance.

The performance difference in the HVDC system tests is caused by the reason of distinct structure application in the three PLLs. The CPLL with a basic structure is relatively easy to design and analyze but shows relatively poor speed of response. The DQPLL shows good tolerance characteristics to harmonics distortion due to the application of DQ PD, but it is very sensitive to commutation voltage unbalance for same reason. The EPLL provides a faster response and smaller steady error and is robust to phase and amplitude distortion of the input signal. Since EPLL is a single-phase PLL, there must be three PLLs required in a system when three phase reference voltage signals are required. This additional burden may make system slower and bring additional synchronization problems.

In analysis of the results of the system performance tests, the EPLL is the only one which is capable of operating stably in both steady state and transient cases under

same test configuration. DQPLL shows a poor performance in the single phase fault (single phase step and voltage unbalance) when non-metal single phase short circuit grounding impedance is not big enough. CPLL can not give a suitable support for rectifier system operation and it presents a bad performance for all the system tests. For the first performance test - steady state operation under harmonics pollution, it shows that PLLs can help rectifier survive under the heavy harmonics distortion on the AC commutation bus. The test results present the effect of harmonics for all rectifiers; they inject the characteristic harmonics to AC and DC bus. In the second test – three phase voltage surge, the results show that rectifiers are sensitive to voltage magnitude change even the DQPLL and EPLL give a good performance in the PLL test. In the third test – single phase fault, sensitivity to voltage unbalance of DQPLL is proved. The fourth test –Three phase fault shows that both DQPLL and EPLL can survive and recover from a transient three phase short circuit fault. In conclusion, EPLL is a suitable synchronization technique for HVDC rectifier with weak AC system, and DQPLL also is capable of operating at stable steady if an average technique is used to remove the sensitivity to voltage unbalance.

Future Work:

Based on the PLL structure and system characteristics, some new technologies, like active loop filter technology and optimal controllers could be developed to improve the system performance in the future.

The application of a combination of PLL synchronization technologies and current control could be thought of as an indirect firing pulse generation control scheme

as compared to the traditional method of HVDC system control. This characteristic could be used to help current control loop design as a function of the input AC commutation voltage. This would be important for operation with weak AC systems.

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Appendix A: Performance Test Model of HVDC System using EMTP RV

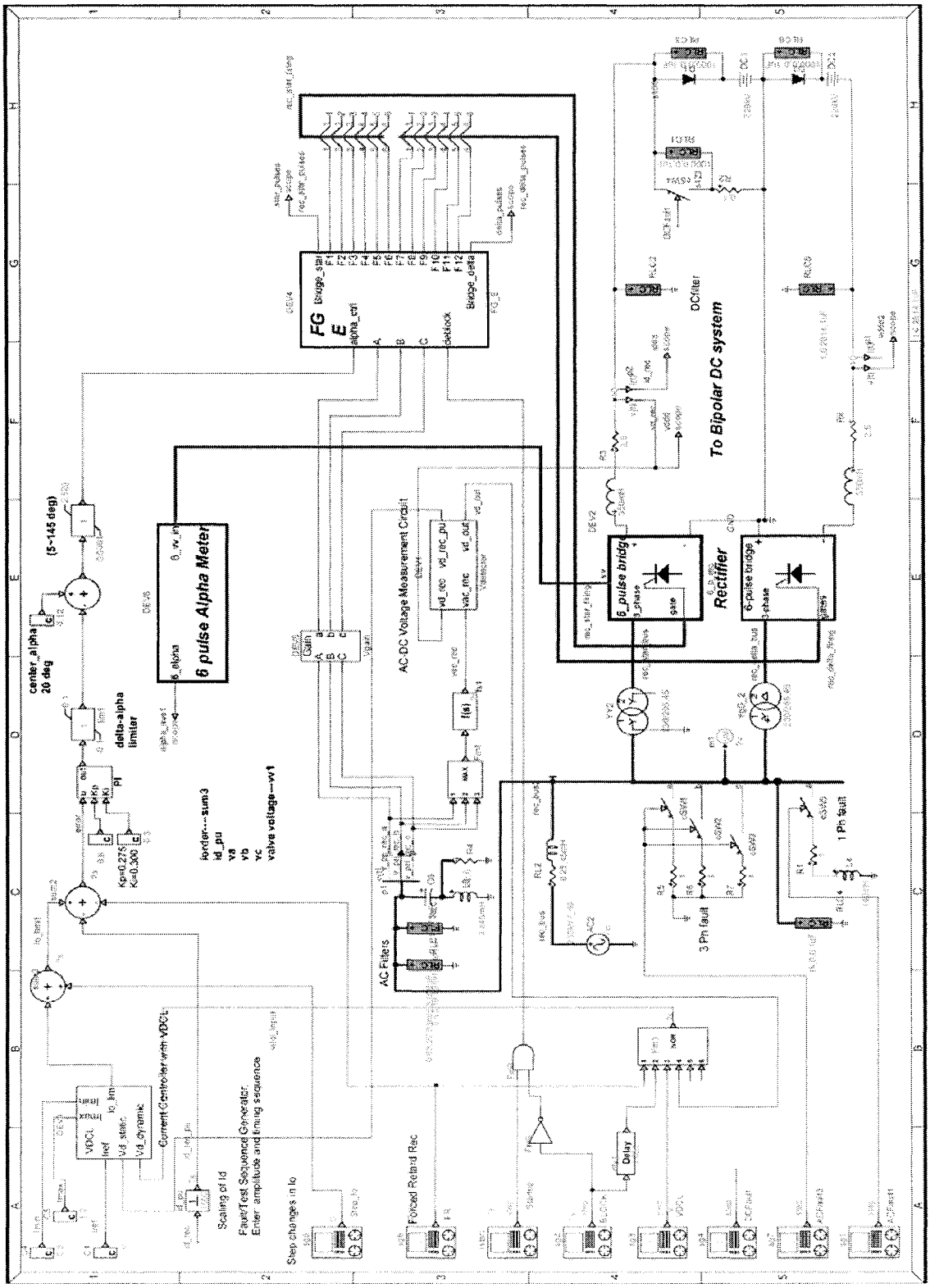


Figure A Performance test model of HVDC system using EMTP RV

Appendix B: Performance Test Model of EPLL using EMTP RV

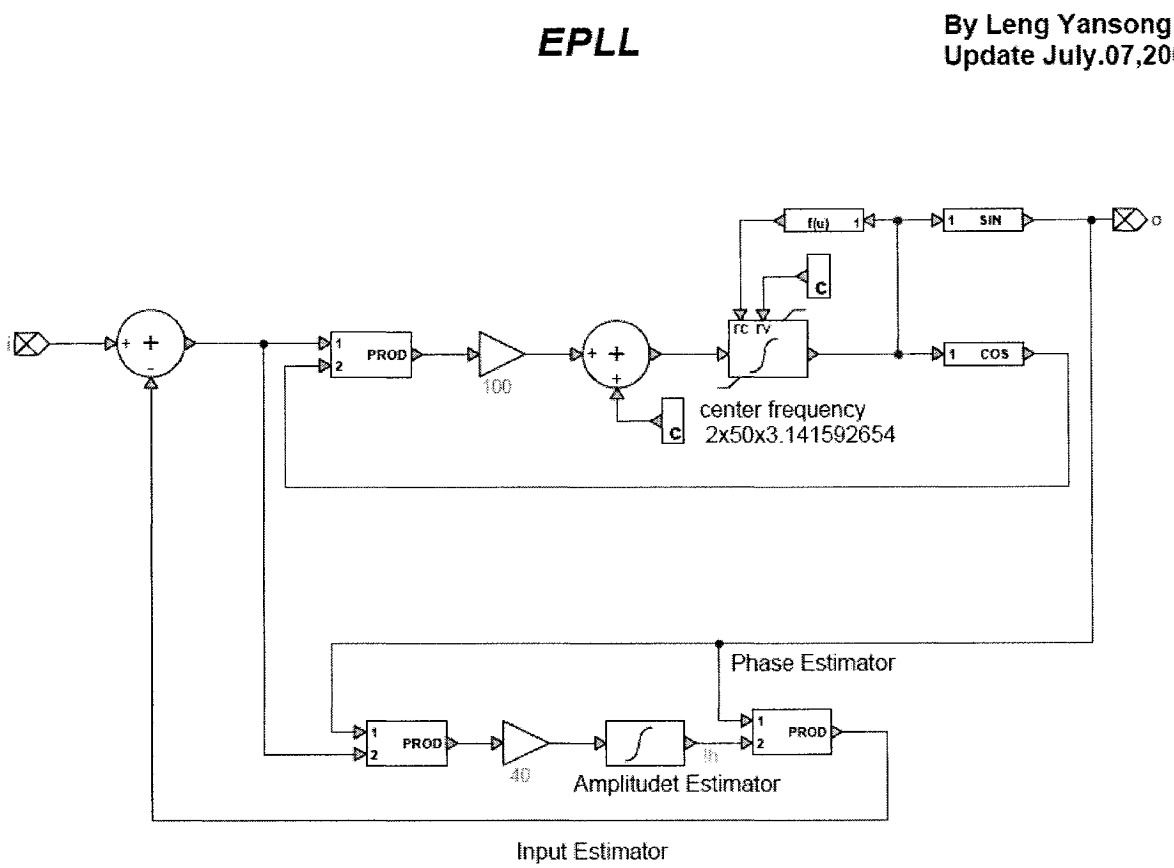


Figure B Performance test model of EPLL using EMTP RV

Appendix C: Performance Test Model of Ramp and Pulse Generator using EMTP RV

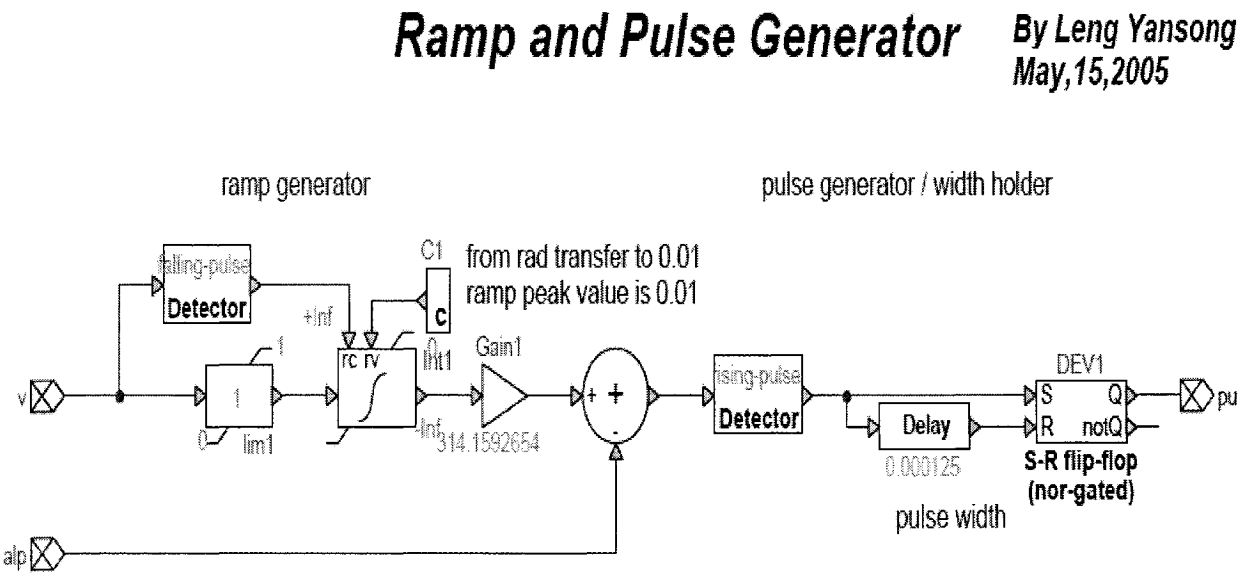
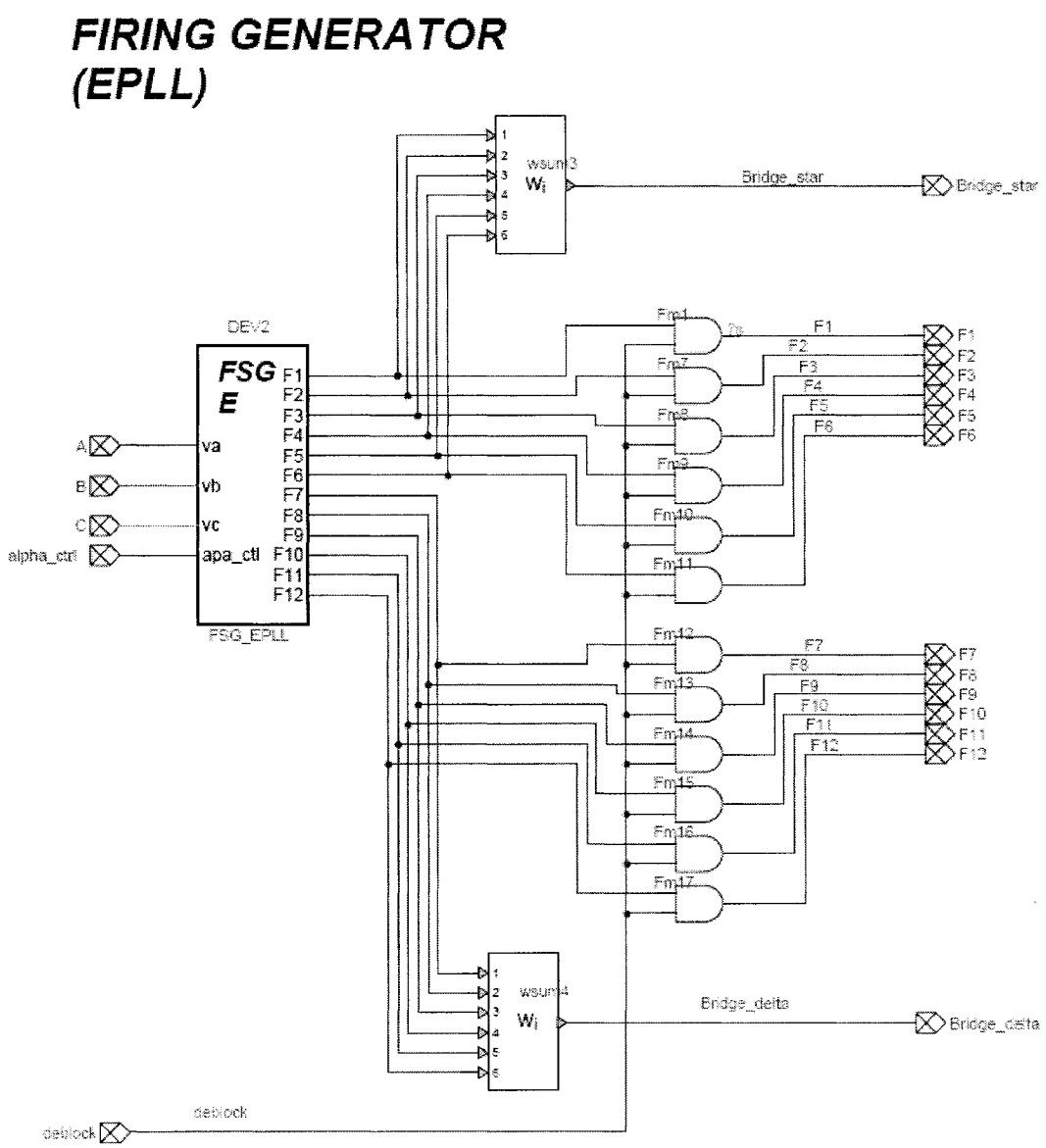


Figure C Performance test model of Ramp and Pulse Generator using EMTP RV

Appendix D: Function Model of Firing Pulse Generator I using EMTP RV



Firing Generator Block(2005 May 16)
Inputs are:
alpha_ctrl: alpha
Deblock: Can be used for protective purposes, and start up period

Outputs are:
12 Firing pulses
Bridge_star pulses on a weighted bases for ease of identification of pulses
Bridge_delta pulses on a weighted bases for ease of identification of pulses

Figure D Function Model of Firing Pulse Generator I using EMTP RV

Appendix E: Function Model of Firing Pulse Generator II using EMTP RV

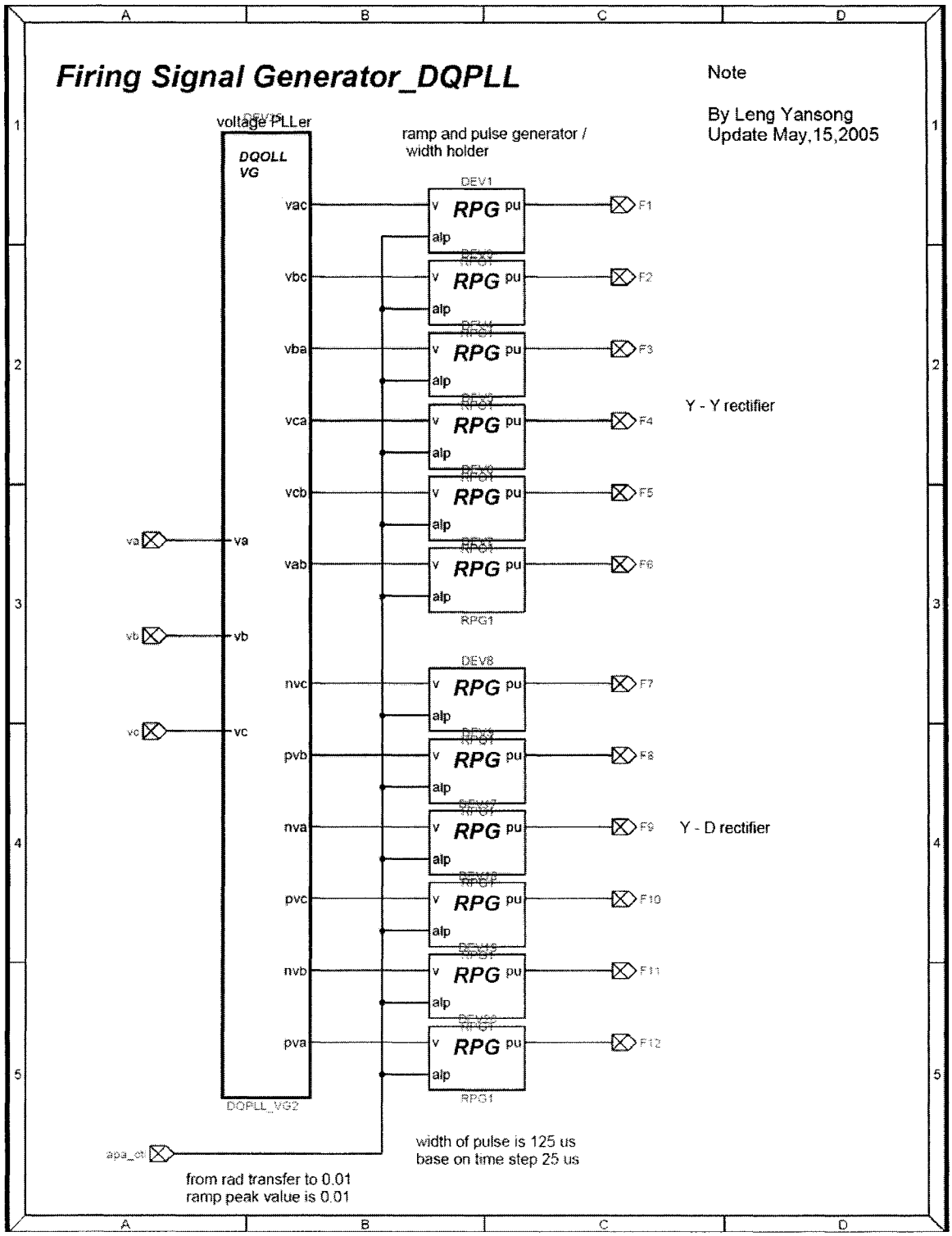


Figure E Function Model of Firing Pulse Generator II using EMTP RV

Appendix F: Function Model of Voltage Generator using EMTP RV

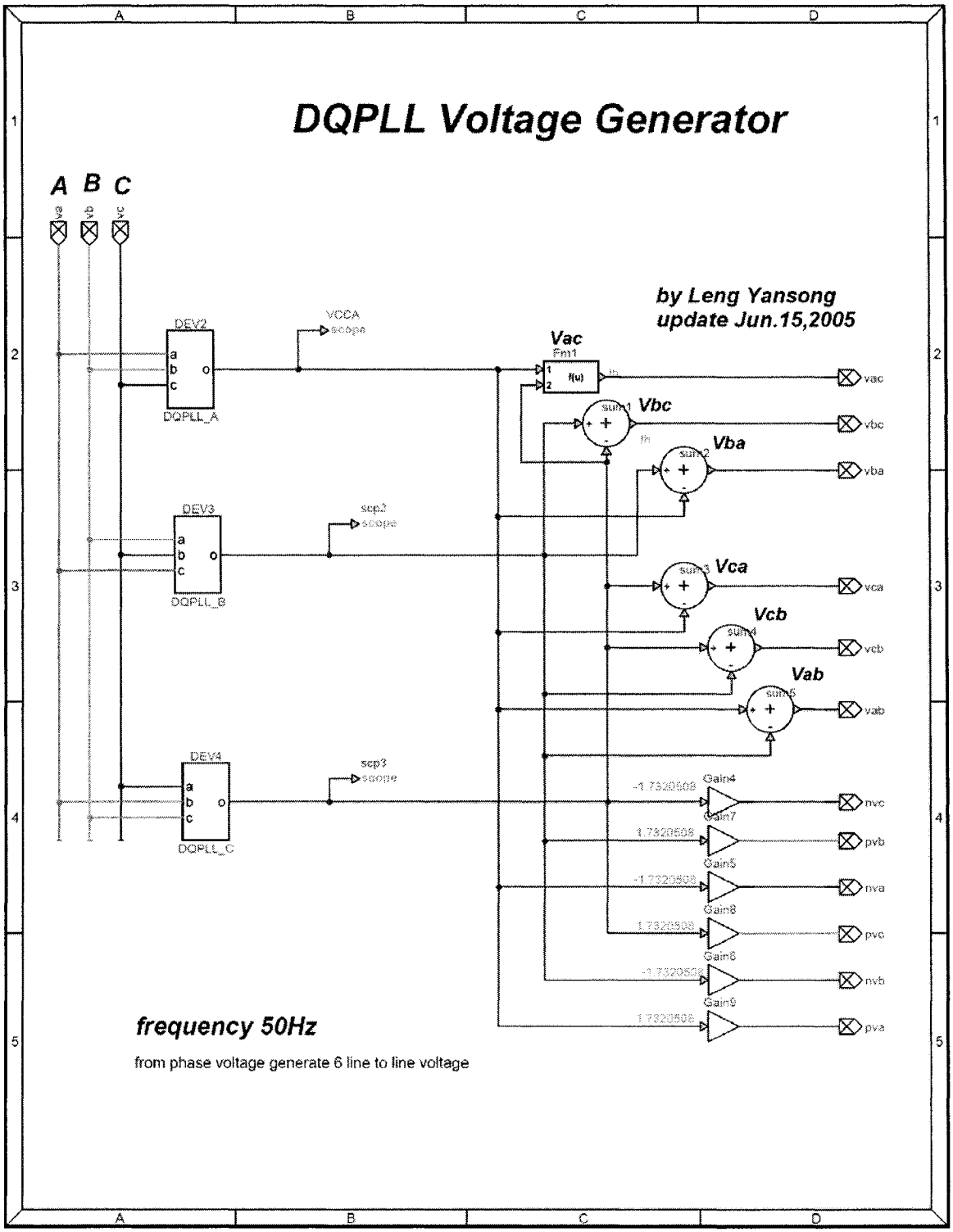


Figure F Function Model of Voltage Signal Generator using EMTP RV