Low Voltage CMOS LNA Design

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Abstract

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Two important factors are motivating recent CMOS Radio Frequency Integrated Circuits (RFIC) research: freeing new bandwidth for commercial use and the appealing characteristics of CMOS technologies. Traditionally implemented in bipolar and III – V compounded semiconductors, radio frequency receivers operating on frequencies up to 40 GHz are currently being researched and implemented in CMOS. Global Positioning System (GPS), Blue Tooth, Radio Frequency ID (RFID), wireless local area network (WLAN) and Automated Highway System (AHS), is a partial list of the newly growing market of RFIC commercial products and these products share the same design concepts: low prices, highly integrated systems and low power designs. With these concepts in mind, CMOS technology becomes a strong contender and the question of CMOS suitability has been answered. Low Power CMOS chips have been successfully fabricated in both, research centers and industry.

This dissertation explores the architectural and design techniques for CMOS Low Voltage Low Noise Amplifier design. The thesis studies different low voltage techniques and proposes a novel Low Voltage LNA design based on a cascade topology and a new way to control the amplifier gain and improve its linearity. Also, based on electromagnetic theory and simulation, simple techniques were proposed that increases the quality factor of on chip inductors. Detailed LNA design steps and optimization are

presented with special focus on CMOS transistor design, biasing and layout optimization for RFIC applications.

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Table of Contents

List of Figures.....x

List of Tables.....xii

Chapter 1 – Introduction.....1

1.1 - Recent trend in Radio Frequency Integrated Circuits (RFIC).....2

1.2 - State of the Art in MOSFET LNA.....3

1.3 - Motivation.....4

Chapter 2 – MOSFET LNA Noise and Linearity.....8

2.1 - Noise in MOSFET.....8

2.1.1 - Noise Types and Definitions.....9

2.1.2 - Noise in Long Channel MOSFET.....11

2.1.3 - Noise in short channel MOSFET.....12

2.2 - Linearity and Dynamic Range.....18

2.2.1 - Effects of Nonlinearity.....18

2.2.2 - Intermodulation Distortion.....21

2.3 - LNA Performance Metrics.....23

2.4 – Conclusion.....25

Chapter 3 - LNA Design and Optimization.....26

3.1 - Introduction.....26

3.2 - Input stage design and matching.....26

3.2.1 - Input stage topology.....26

3.2.2 - Power Versus Noise Matching.....28

3.2.3 - Non-Quasi Static Effect.....29

3.2.4 - Input Stage Matching.....30

3.2.5 - Effective Transconductance, PCC and PVC.....36

3.3 - LNA Design Optimization.....38

3.3.1 - Gain Boosting Techniques.....39

3.3.2 - Noise Figure Optimization within a Given Power Budget.....43

3.3.3 - Linearity Optimization.....46

3.3.4 - The design of the Cascode Device.....48

3.4 - Conclusion.....51

Chapter 4 – Low Voltage 5 GHz LNA Implementation.....52

4.1 - Introduction.....52

4.2 - Parasitic BJT in the MOS.....53

4.3 - LNA Chip Layout.....58

4.3.1 - RF I/O Pads Design.....58

4.3.2 - RF MOS Transistor Layout.....60

4.3.3 - Inductors Design and Layout.....62

4.4 - Post Layout Simulation results.....63

4.5 - Conclusion.....65

Chapter 5 – LNA Measurement Results.....66

5.1 – Introduction.....66

5.2 – Test Setup and Results.....66

5.3 – Conclusion.....70

References.....71

List of Figures

Figure 1.1 Schematic of the LNA in [7] including its off-chip matching.....5

Figure 1-2: Transformer feedback LNA (a) and High linearity LNA (b) circuits.....6

Figure 2-1 Thermal noise model of a resistor (a) voltage mode (b) current mode.....10

Figure 2-2: standard MOSFET noise model.....12

Figure 2-3: short channel small-signal equivalent circuit with noise generators.....18

Figure 2-4: Definition of the 1-dB compression.....20

Figure 2-5: Signal corruption due to two-tone intermodulation.....22

Figure 2-6: Third-order Intercept Point.....22

Figure3-1: Saw Filter termination: (a) perfect matched (b) Badly matched.....27

Figure 3-2: Common LNA input stages architectures. (a) Inductive degeneration.

(b) Local Shunt Feedback. (c) 1/gm termination.....28

Figure 3-3: RF Source and load system impedance.....29

Figure 3-4: First order small signal model including NQS effect.....31

Figure 3-5: inductive degenerated common source amplifier small-signal model.....32

Figure 3-6: MOS direct matching by inductive source degeneration.....37

Figure 3-7: indirect matching.....40

Figure 3-8: maximum achievable impute impedance at 5 GHz as a function of C_{gs}

and $C_{p,fixed}$ 42

Figure 3-9: Contour plots of constant noise figure (dB) relating the overdrive voltage

and P_D, for L_{eff}= 0.135um; w_o= 31.4 Grps, V_{DD}= 1 V, γ=1.4, δ=2.6, c=0.45, v_{sat}=0.9m/s 44

Figure 3-10: Contour plots of constant noise figure (dB) relating Q_M and g_{meff}, for w_o = 31.4 Grps, α =0.85, γ =1.4, δ =2.6, c=0.45.....45

Figure 3-11: contour plots of IIP3.....47

Figure 3-12: coscode transistor side effect troubleshooting.....50

Figure 4-1: MOS cross section showing the parasitic BJT.....53

Figure 4-2: The new NMOS-PNP transistor small signal model.....54

Figure 4-3: The proposed cascode LNA circuit and its parasitic.....55

Figure 4-4: Third-order signal harmonic cancellation.....58

Figure 4-5: Effects of RF pad shielding.....60

Figure 4-6: Transistor f_t Vs its unit gate length.....61

Figure 4-7: RF transistor layout.....62

Figure 4-8: LNA power gain and I/O signal reflection.....64

Figure 4-9: LNA linearity.....64

Figure 4-10: LNA gain tunability.....65

Figure 5-1: LNA test setup.....67

Figure 5-2: LNA schematic with Bias Tee circuit.....68

Figure 5-3: measured I/O signal reflection.....68

Figure 5-4: LNA measured power gain (S21).....69

List of tables

Table 1-1: Mixed Signal and RFCMOS Process Overview.....3

Table 1-2: Summary of selected recent LNA results.....6

Table 3-1: Summary of LNA's topology performance ($\alpha = 0.85, \delta = 4, c = j0.45$).....27

Table 4-1: Novel Cascode LNA performace versus Classic one.....65

Table 5-1: measured versus simulated LNA results.....67

Table 5-2: Comparison of this work versus other reported LNA.....67

Chapter 1 – Introduction

Historically, radio frequency design was thought to be incompatible with large scale integration and IC technology. The design of Radio Frequency circuits relies on bulky RLC circuits, and most of the radio frequency designs were discrete, implemented in III – V compound semiconductors or in bipolar technologies. Early GaAS and bipolar LNA's offer a good gain and low noise figure, but are expensive and cannot be integrated easily. As the new technology evolved toward integration and low cost, microelectronics engineers successfully researched the feasibility of the new CMOS technologies in RF circuit designs. Smaller CMOS devices translated into higher power gain and low noise figure and new RF CMOS processes were introduced to meet the stringent requirements of high frequency circuits. The latest CMOS RFIC technologies proved to be a strong contender not only in terms of cost and integration, but also in terms of high performance. Technologies such as the IBM 0.13 μm CMOS RF process is widely used in industry today for reliable and high performance RFIC circuits.

New CMOS RFIC imposes many uncertainties and challenges owing to the poor modeling of both the device and on chip passive components. Motivated by the upcoming surge in portable RFIC demand, this work is intended to explore the performance of a CMOS LNA fabricated in a standard TSMC 0.18 μm process as well as on-chip passive components. The rest of this chapter will elaborate more on topics such as recent trends in CMOS technologies and the motivation of this work as well as the state of the art in CMOS LNA design.

1.1 - Recent trend in radio frequency integrated circuits (RFIC)

Wireless communication at gigahertz frequencies has become a huge market, which keeps growing. MOSFET technology is an attractive solution due to its low cost, high level of integration and its recent high performance achievements. Peak CMOS unity-current-gain frequency (f_t) are now in excess of 115 GHz (CMOS 0.13 μm) [1], and the trend appears to be doubling of the f_t every three years. The device speed is supplemented by recently developed passive elements, such as fractal capacitors [2] and the shielded spiral inductor [3]. The lossy substrate is made much less relevant without requiring special processing steps and Silicon-on-Insulator (SOI) CMOS will replace conductive SiCMOS substrate. The minimum Device noise figure (NF_{min}) is typically under 0.7 dB at 5 GHz (0.13 μm CMOS) [4], and a better understanding of broadband MOSFET noise has shown how to minimize the overall amplifier noise figure, within a specified power budget. With the continuous downsizing of CMOS technology, unity-current-gain frequency (f_t) and maximum oscillation frequency (f_{max}) of active devices for 0.18-micron processes have exceeded 70 GHz for f_t and 150 GHz for f_{max} [5]. This is especially appealing since CMOS is a strong contender for implementing transceivers. The above brief about recent 0.18 and 0.13 μm CMOS technological performance, motivated many companies and researchers and as a result, more highly performing CMOS RF subsystems were fabricated and reported in the last couple of years [7]-[26]. Finally, one table illustrating the improved performance of the latest CMOS technologies is included below. The table is reproduced by the courtesy of Chartered Semiconductor Manufacturing®, one of the world's top three silicon foundries. Some discrepancy may appear in f_{max}, f_t, and NF_{min} performance compared to the aforementioned reported ones.

Table 1-1: Mixed Signal and RFCMOS Process Overview

	0.60μM	*0.35μM*	*0.25μM*	*0.18μM*	*0.13μM*
Supply Voltage (V)	*5.0*	*3.3*	*2.5/3.3*	*1.8/3.3*	*1.2/2.5, 3.3*
Gate Oxide Thickness (Å), Gate Stack	*125, WSi_X*	*65, $TiSi_2$*	*43/65, $TiSi_2$*	*30/63, $CoSi_2$*	*20/45, 65, $CoSi_2$*
Metal, Dielectric	*3 Al Layer, SiO_2*	*4 Al Layer, SiO_2*	*5 Al Layer, SiO_2*	*6 Al Layer, SiO_2*	*8 Cu Layer, F-TEOS/low-k*
Core x' tor V_{t_n}, V_{t_p} (V)	*0.80, -0.85*	*0.60, -0.75*	*0.57, -0.57*	*0.48, -0.48*	*0.34, -0.36*
Core Low-V_t x' tor V_{t_n}, V_{t_p} (V)	*No*	*Available upon request*	*0.33, -0.25*	*0.24, -0.30*	*0.24, -0.27*
Core Native-V_t NMOS V_t (V)	*No*	*Available upon request*	*Available upon request*	*0.04*	*0.118 (1.2V)*
NMOS f_t (GHz)	*No*	*27(V_{ds} = 3.0V)*	*39(V_{ds} = 2.5V)*	*60(V_{ds} = 1.8V)*	*80(V_{ds} = 1.2V)*
NMOS f_{max} (GHz)	*No*	*35(V_{ds} = 3.0V)*	*44(V_{ds} = 2.5V)*	*65(V_{ds} = 1.8V)*	*>100(V_{ds} = 1.2V)*
PMOS f_t (GHz)	*No*	*15(V_{ds} = 3.0V)*	*20(V_{ds} = 2.5V)*	*23(V_{ds} = 1.8V)*	*40(V_{ds} = 1.2V)*
PMOS f_{max} (GHz)	*No*	*20(V_{ds} = 3.0V)*	*23(V_{ds} = 2.5V)*	*38(V_{ds} = 1.8V)*	*60(V_{ds} = 1.2V)*
Core NMOS NF_{min} @ 2.45 GHz (dB)	*No*	*1.9(V_{ds} = 2V, V_{gs} = 1V)*	*1.6(V_{ds} = 2.5V, V_{gs} = 1V)*	*1.4(V_{ds} = 1.8V, V_{gs} = 0.8V)*	*=<1.4(V_{ds} = 1.2V, V_{gs} = 0.6V)*
Deep N-well	*No*		*Yes*		
Varactors	*No*	*MOS/PN*			

This is due to testing under different bias and geometry conditions. Note that copper is replacing aluminum for 0.13 μm technology, because it provides better conductivity.

1.2 - State of the art in MOSFET LNA

Recently, Radio Frequency designers are taking advantage of technology advances of the MOSFET device by trying to design monolithic high performance Low Noise Amplifiers. Many authors have investigated different CMOS LNA techniques in the 0.8-7.0 GHz frequency range. A few of these major contributions will be reviewed in this section.

The first successful CMOS LNA with detailed analysis is presented in [7]. A unilateral design based on a cascode topology is shown in Figure 1-1, proved later to be the most successful topology for CMOS LNA design. This pioneer work detailed all the design

guidelines of cascode CMOS LNA and proved that the cascode topology offers the lowest noise figure due to its source inductive degeneration, and highest linearity due to its common gate transistor. Based on the same topology, an excellent LNA was reported in [9] with less than 9mW of power consumption and 0.8db of noise figure at 1.2 GHz. The contribution of the later design was its very low noise figure with a small power budget. Until today, this design is considered the best in its class.

Another LNA design is a bilateral one and based on a single transistor design as shown in Figure 1-2.a. The transformer-feedback LNA [10] uses a negative feedback transformer to neutralize the RF coupling between the input and output or, expressed differently, to cancel the effect of miller capacitance (C_{gd}). This design achieved an extremely low noise figure of 0.9 db (at 5.75 GHz) with very low power dissipation. Again this low noise figure is the best reported to date at 5.75 GHZ. Although this topology is a good choice for low voltage LNAs, it is not a good candidate in terms of IIP3 performance, particularly when compared to cascode topology. The last design reviewed in this work provides a technique that improves the linearity of cascode LNAs. In [17], the IIP3 was increased up to 16 dBm instead of 3 dBm. The idea originated from the observation of the drain current's third harmonic waveform, which has even-odd symmetries between the boundary of saturation and triode regions. To cancel the effect of this harmonic, two NMOS transistors were stacked on top of each other and biased in triode and saturation while exiting their gates differentially. The schematic of this LNA is shown in figure1-2.b. Finally, the performance of the selected LNAs is summarized in table.2 below. It covers reported LNAs of different CMOS technologies and frequencies. These LNAs are classified throughout the table based on their optimization goal.

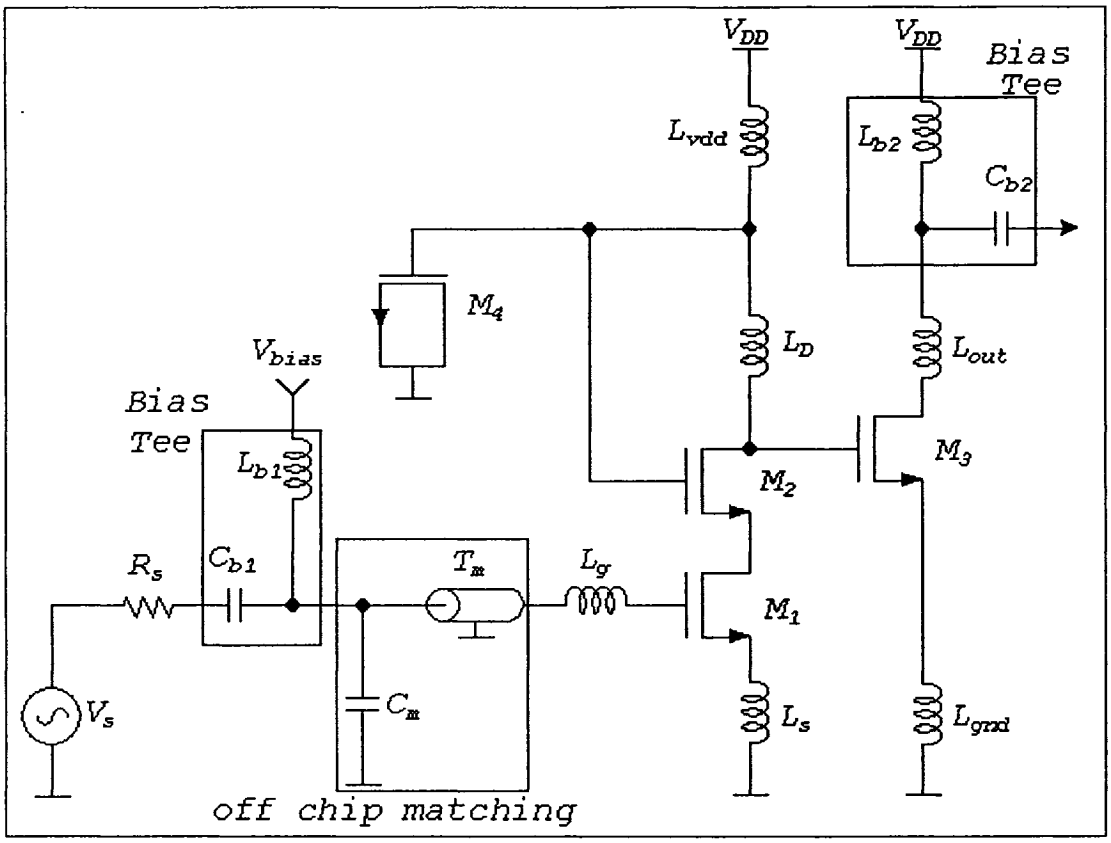

Figure 1-1: Schematic of the LNA in [7] including its off-chip matching.

1.3 – Motivation for and organization of the thesis

Complete integration of analog front-end and complex digital CMOS DSP processors onto the same silicon chip is the ultimate goal of research on MOSFET RFICs. Single MOSFET transceivers were reported for various wireless applications such as: GPS [7]-[28], PCS [29], GSM [30]-[31], DCS [31], CDMA [32], WLAN [33] and Blue Tooth [34]-[35].

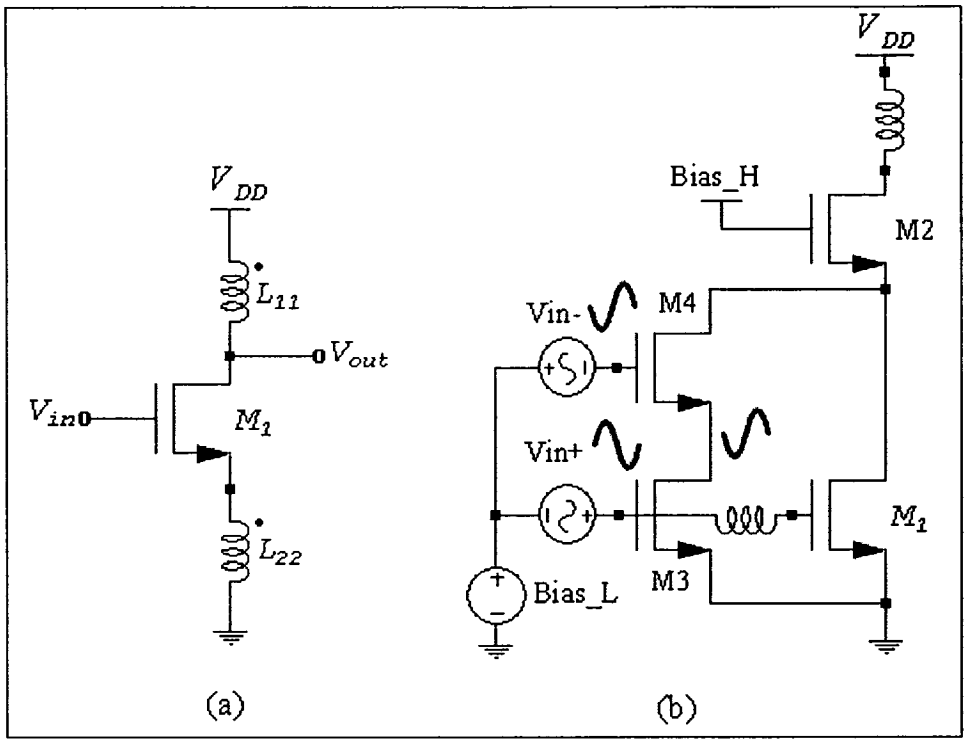

Figure 1-2: Transformer feedback LNA (a) and High linearity LNA (b) circuits.

Table 1-2: Summary of selected recent LNA results

REF	OPTIMIZATION	NF (DB)	GAIN (DB)	IIP3 (DBM)	V_{DD} / POWER (V / mW)	F_0 (GHZ)	TECH. (μm)	YEAR
[8]	NF	1.4/2.1*	17	na	/9	5.2	0.25	2001
[9]		0.8	20	-11	9	1.23	0.25	2002
[12]		0.9	8.8	7.1	7.5	0.8	0.24	2002
[14]		1.8	8.9	8.4	6.9	7	0.25	2002
[16]		0.85/1.2	13	-1.5	17.6/5	0.92	0.35	2001
[25]		2.5	16	na	16	5	0.25	2000
[17]	IIP3	3.1	15.6	13.9	na	2.4	0.25	2003
[17]		3	14.9	16.1	na	2.2	0.25	2003
[18]		2.8	5	18	45	0.9	0.35	2001
[11]	Low Voltage	0.9	14.2	0.9	1/16	5.75	0.18	2003
[7]		3.5	22	-9.3	1.5/15	1.5	0.6	1997
[21]		2.5	13.2	na	1/22.2	5.8	0.18	2002
[22]		3.2	7.2	6.7	1.3/20	5.8	0.35	2002
[35]		4.8	18	-7	1/32	2.4	0.35	2001
[29]		1.8	15	0	1/25	1.9	0.5	2001

*Reported noise after the addition of ESD protection.

New research focuses on designing high performance MOSFET transceivers to meet the increasing demand on bandwidth, low power, and higher frequencies of operation. Portable low power MOS transceivers are in high demand and this trend has motivated the evolution of low voltage RFIC. The design of a low voltage LNA, an important receiver building block, is a challenging task. Many Low power LNA structures suffer from noise or linearity performance degradation and some topologies are only conditionally stable. A low voltage LNA design that delivers good gain is highly desirable but also difficult to achieve. This work is intended to research and implement low voltage LNA circuits. Noise and linearity in CMOS LNA will be researched in details through this work.

Another design issue that affects the performance of RFIC systems and especially the LNA is the design of on-chip passive components such as inductors and capacitors. Optimizing and accurately selecting the quality factor of on-chip inductors will reduce the noise figure (NF) of the LNA and help in optimizing its power gain. On-chip inductor design is examined experimentally in this work; round planar inductor using double metal layers (both metal six and metal five) were implemented.

The nature and source of noise as well as the effect of the device nonlinearity will be covered in Chapter two. LNA design equations and optimization will be covered in chapter three. Chapter four present a novel low voltage LNA design based on built in parasitic BJT. Also, the Layout of passive and active component as well as high speed RFIC layout techniques will be covered in chapter four. Finally, the implementation and experimental measurement will be covered in chapter five.

Chapter 2 – MOSFET LNA Noise and Linearity

This chapter will cover basic LNA parameters such as noise and noise figure as well as linearity and distortion in LNA. In order to complete the discussion about these two important topics, this chapter will also cover the noise and linearity in cascade systems (i.e. receivers). Finally, some important LNA performance metrics will be presented.

The discussion about noise will cover both short and long channel CMOS devices in details. Starting with the definition of all types of noise and their origins, a complete derivation of noise equations in short channel devices will be provided. The discussion about the device linearity will be expanded to cover the harmful effects of nonlinearity in CMOS devices and the way it affects the receivers' performance. Problems such as gain compression, desensitization, blocking and intermodulation distortion will be covered in details.

2.1 –Noise in MOSFET

In his pioneer work on noise in solid state devices, Van der Zeil [36] defines two noise sources that are present at the solid state device terminals. The drain current noise, originated from the conductance of the channel and the induced gate noise current, originated from charge fluctuations in the channel. This section will define the origins and nature of these two sources, as well as, the noisy models of both long and short channel MOSFET devices.

2.1.1 – Noise types and definitions

Thermal noise: Thermal or Johnson noise is a consequence of Brownian motion in a given conductor [37], where thermally agitated charge carriers constitute a randomly varying current that give rise to random voltage. Due to its thermal origin, the available thermal noise power is given by:

$$P_{NA} = kT\Delta f \tag{2.1}$$

where $k = 1.38 \times 10^{-23}\ j/k$ is the Boltzman's constant, T is the absolute temperature in Kelvin and Δf is the noise bandwidth in Hertz. Thermal noise is approximated as white noise because it has constant energy per Hertz. By definition, available noise power is the maximum noise power that a given noise source can deliver to a matched load. As seen in figure 2-1, a noise source can be a voltage or current source (using ohm's law) and according to the above definition of P_{NA} we can write:

$$P_{NA} = kT\Delta f = \frac{\overline{e_n^2}}{4R} \tag{2.2}$$

and

$$\overline{e_n^2} = 4kTR\Delta f \tag{2.3}$$

By similar reasoning, the rms noise current delivered to R is equal to:

$$\overline{i_n^2} = \frac{4kT\Delta f}{R} = 4kTG\Delta f \tag{2.4}$$

It is clear from the equations of thermal noise that, reducing the noise bandwidth using properly matched sharp filters as well as lowering the conductor temperature, is the only means to reduce thermal noise of a given conductor.

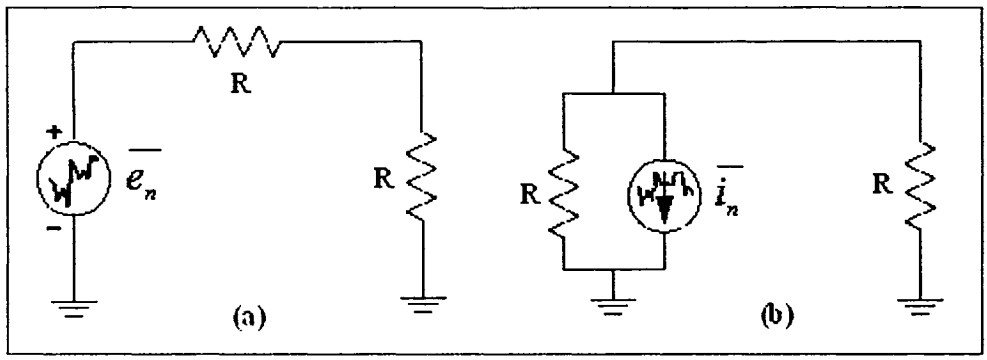

Figure 2-1: Thermal noise model of a resistor (a) voltage mode (b) current mode

Shot noise: Shot or Schotty noise is due to the granular nature of electronic charge [37]. When a direct current flows through a potential barrier such as a PN junction in a transistor, the flow of current happens in a discrete manner and discontinuous pulses of current occur every time an electron hops the PN energy barrier. Since the occurrence of electron hopping is random, shot noise is considered as white one. Shot noise current is expressed as:

$$\overline{i_{sn}^2} = 2qI_D\Delta f \tag{2.5}$$

where $\overline{i_{sn}^2}$ is the rms noise current, q is the electronic charge (about $1.6\times10^{-19}C$), I_D is the average DC current in Amperes. One can suppress this source of noise by reducing the noise source bandwidth and the DC current flowing through the PN junction. In a MOSFET transistor, for every V_{DD} supply there exists an optimum bias current where increasing the DC bias current above it will result in extra shot noise.

Flicker Noise: Impurities and defects in crystal lattices result into trapping of random charge carriers and hence Flicker or *1/f* noise. The trapping times are distributed in a way that leads to *1/f* noise in MOSFET. Larger gate capacitance smoothes the fluctuations in channel charge and helps suppressing *1/f* noise, which is not the case for deep devices where C_{gs} is relatively small. The mean square, *1/f*, noise current is given by:

$$\overline{i_{fn}^2} \approx \frac{K}{f} w_T^2 A \Delta f \tag{2.6}$$

where K is a device-specific constant and is roughly $50 \times 10^{-28} c^2/m^2$ for NMOS [37] and A is the area of the gate. The *1/f* noise exhibition is technology dependant, and of less importance in a narrow band LNA where the bandwidth is about few hundreds of MHz around the center frequency. This noise is more important, and should be carefully considered, when designing mixers and VCOs.

2.1.2 - Noise in long channel MOSFET

MOSFET transistors are essentially voltage-controlled resistors and the dominant noise source in MOS devices is channel thermal noise. Modeled as a shunt current source, as seen in figure 2.2, the channel thermal noise is considered as white noise and its power spectral density is given by[37]:

$$\overline{i_d^2} = 4kT\gamma g_{do} \tag{2.7}$$

where g_{do} is the zero-bias drain conductance of the device, and γ is a bias dependent factor (about 1.3 at saturation for long channels devices). γ may be as high as 2-3 in short channels devices and this is attributed to hot electrons in the channel [36] [38].

An additional source of noise in MOSFET devices is the one generated by the distributed polysilicon gate resistance [37]. The contribution of this source can be reduced to

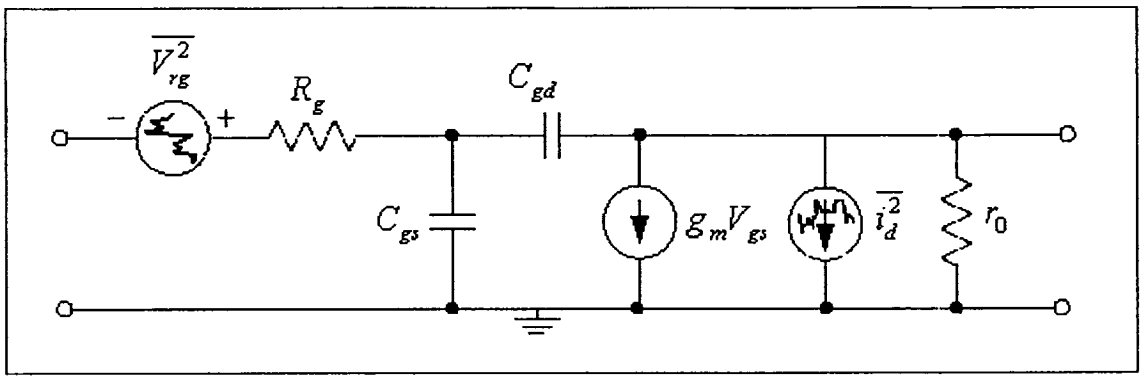

Figure 2-2: standard MOSFET noise model

insignificant level by contacting both ends of the fingered gates. The final gate resistance is given by:

$$R_g = \frac{R_S W}{12 n^2 L} \tag{2.8}$$

where R_S is the sheet resistance of the polysilicon, W is the total gate width of the device, L is the gate length, and n is the number of gate fingers.

The back gate epitaxial resistance is a third source of thermal noise, which can result in apparent increase of γ in equation (2.7). The final drain noise is given by:

$$\overline{i_d^2} = 4kT\{\gamma g_{do} + g_{mb}^2 R_{epi}\}\Delta f = 4kT\gamma_{eff} g_{do}\Delta f \tag{2.9}$$

where

$$\gamma_{eff} \approx \gamma + \frac{g_{mb}^2 R_{epi}}{g_{do}} \tag{2.10}$$

The design of substrate contacts plays an important role in suppression this type of noise.

2.1.3 - Noise in short channel MOSFET

Modified expression for S_{ID} and γ: Based on Van der Ziel noise theory [36], an extended noise version is needed in order to take into account the high field effects in short channel

devices and develop the expressions of optimum noise matching. The power spectral density of the drain noise is given by [37]:

$$S_{I_D} = 4kT\gamma g_{do} \tag{2.11}$$

where γ is a bias-dependent parameter used to account for excess in drain current noise (around 2 for short channel devices) and g_{do} is the zero bias drain given by:

$$g_{do} = g_m = \mu C_{ox} \frac{W}{L} V_{overdrive} \tag{2.12}$$

where $V_{overdrive} = (V_{gs} - V_{th})$.

In short channel devices, the carriers are under the effect of high electric field (including vertical electric field). This will increase the drain current noise. In [36], the power spectral density of the drain current noise is given by:

$$S_{I_D} = \frac{4kT}{L^2 I_D} \int_0^{V_d} \frac{T_e}{T_0} g^2(V) d(V) \tag{2.13}$$

Where $g(V)$ is one element of the distributed channel conductance (V is its corresponding voltage), T_e is the electron temperature and T_0 is the lattice temperature. Equating (2.11) and (2.13) we get the expression of γ as:

$$\gamma = \frac{1}{L^2 g_{do} I_D} \int_0^{V_d} \frac{T_e}{T_0} g^2(V) d(V) \tag{2.14}$$

On the other hand we know from [40] that electron velocity in short channel is given by:

$$v(y) = \frac{\mu_{eff} E(x)}{1 + \frac{E(x)}{E_{crit}}} \tag{2.15}$$

The above equation gives the following expression for I_D:

$$I_D = \mu_{eff} C_{ox} W\left(V_{gs} - V_t - V\right)\frac{E(x)}{1+\frac{E(x)}{E_{crit}}} = \left[\mu_{eff} C_{ox} W\left(V_{overdrive} - V\right) - \frac{I_D}{E_{sat}}\right]\frac{dV}{dx} \quad (2.16)$$

where E_{sat} is the velocity saturation field strength. I_D is also given in terms of channel conductance by:

$$I_D = g(V)E(x) = g(V)\frac{dV}{dx} \quad (2.17)$$

Equating (2.16) and (2.17) we get $g(V)$ as:

$$g(V) = \mu_{eff} C_{ox} W(V_{overdrive} - V) - \frac{I_D}{E_{sat}} \quad (2.18)$$

In order to evaluate (2.14) an expression for $\frac{T_e}{T_0}$ is needed. A simplified expression of the one given in [39] is equal to:

$$\frac{T_e}{T_0} = \left[1+\frac{E(x)}{E_{sat}}\right]^2 = \left[1+\frac{I_D}{g(V)E_{sat}}\right]^2 \quad (2.19)$$

Now (2.14) could be rewritten using (2.18) and (2.17) as follows:

$$\frac{T_e}{T_0} \times g^2(V) = \left[g(V) + \frac{I_D}{E_{sat}}\right]^2 = \left[\mu_{eff} C_{ox} W(V_{overdrive} - V)\right]^2$$

and γ is given by:

$$\gamma = \frac{1}{g_{do} L^2 I_D}\int_0^{V_D} \mu_{eff} C_{ox} W^2 (V_{overdrive} - V)^2 dV$$
$$= \frac{\mu_{eff}^2 C_{ox} W^2 V_D}{g_{do} L^2 I_D}\left[V_{overdrive}^2 - V_{overdrive} V_D + \frac{V_D^2}{3}\right] \quad (2.20)$$

Next, in order to develop the final expression of γ we need to find the expression of I_D and V_D. In strong inversion, [40] evaluate I_D and V_D as follow:

$$I_D = I_{Dsat} = \frac{1}{2}\mu_{eff} C_{ox} W E_{sat} \frac{V_{overdrive}}{V_{overdrive} + E_{sat} L} \tag{2.21}$$

$$V_D = V_{Dsat} = \frac{V_{overdrive} E_{sat} L}{V_{overdrive} + E_{sat} L} \tag{2.22}$$

Substituting (2.12), (2.21) and (2.22) into (2.20) results into the following γ expression:

$$\gamma = \frac{1}{[V_{overdrive} + E_{sat} L]^2} \left[\frac{2}{3} (E_{sat} L)^2 + 2 V_{overdrive} E_{sat} L + 2 V_{overdrive}^2 \right] \tag{2.23}$$

Assuming that $V_{overdrive} >> E_{sat} L$ for short channel devices γ becomes roughly equal to 2 or higher.

Induced gate noise and new expression for δ: High frequency and short channel are two conditions that boost the induced gate noise greatly. Recently, Knoblinger [39] reported measured results of gate noise for 0.18 μm NMOS transistor showing substantial increase in gate noise compared the long channel one (30 times more). Induced gate noise is mainly due to the distributed nature of the gate over the noisy channel as well as the gate admittance, which is given by:

$$Y_g = jwC_{gs} + g_g \tag{2.24}$$

where C_{gs} and g_g are given by:

$$C_{gs} = \frac{2}{3} WLC_{ox} \tag{2.25}$$

and

$$g_g = \frac{W^2 C_{gs}^2}{5 g_{do}} \tag{2.26}$$

The power spectral density of the gate noise associated with g_g is given by:

$$S_{I_G} = \frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \tag{2.27}$$

$\delta \approx \frac{4}{3}$ for long channel devices. For short channel devices S_{I_G} is given by [40]:

$$S_{I_G} = \frac{4kTw^2 C_{ox}^2 W^2}{I_D^2} \int_0^{V_D} \frac{T_e}{T_0} g^2(V)(V - V_a)^2 dV \tag{2.28}$$

where

$$V_a = V_{Dsat} + \frac{V_{Dsat}^2}{2E_{sat}L} - \frac{(V_{overdrive})\frac{V_{Dsat}}{2} - \frac{V_{Dsat}^2}{6}}{V_{overdrive} - \frac{V_{Dsat}}{2}}\left(1 + \frac{V_{Dsat}}{E_{sat}L}\right) \tag{2.29}$$

equating (2.25) - (2.28) result in the following expression for δ:

$$\delta = \frac{45 g_{do}}{4L^2 I_D^3} \int_0^{V_D} \frac{T_e}{T_0} g^2(V)(V_a - V)^2 dV \tag{2.30}$$

Substituting (2.19) into (2.30) we get:

$$\delta = \frac{1}{(V_{overdrive} + E_{sat}L)^4} \left[\begin{array}{l} \frac{4}{3}(E_{sat}L)^4 + \frac{17}{2}(E_{sat}L)^3 V_{overdrive} + \\ 23(E_{sat}L)^2 V_{overdrive}^2 + \frac{45}{2} E_{sat} L V_{overdrive}^3 + \frac{15}{2} V_{overdrive}^4 \end{array} \right] \tag{2.31}$$

Assuming that $V_{overdrive} >> E_{sat}L$ thus $\delta \approx \frac{15}{2}$ while the opposite is true for long channel devices and $\delta \approx \frac{4}{3}$.

Drain and gate noise correlation: The induced gate current noise is partially correlated with drain current noise. This correlation originates mainly from the distributed geometry of the gate over the noisy channel of the MOSFET device plus the effect of fringing electric field and given by:

$$|c| = \frac{\overline{i_d i_g^*}}{\sqrt{\overline{i_g^* i_g} \times \overline{i_d i_d^*}}} = \frac{\overline{i_d i_g^*}}{\sqrt{\overline{i_g^2} \times \overline{i_d^2}}} \tag{2.32}$$

where $\overline{i_d^2}$ is given by (2.7) and:

$$\overline{i_g^2} = \overline{i_g i_g^2} = 4kT\delta g_g \Delta f \tag{2.33}$$

$$\overline{i_g i_d^*} = 4kT\varepsilon jwC_{gs}\Delta f \tag{2.34}$$

(2.32) becomes

$$c = j\sqrt{\frac{5}{\gamma\delta}\varepsilon} \tag{2.35}$$

where ε is given by:

$$\varepsilon = \frac{(E_{sat}L)^2}{(V_{overdrive} + E_{sat}L)^3}\left[\frac{1}{6}E_{sat}L + \frac{1}{2}V_{overdrive}\right] \tag{2.36}$$

For short channel MOSFET $c = j0.55$ [44] and about $j0.395$ for long channel one. Finally, the revised small-signal equivalent circuit shown in figure 2-3 will replace the initial model illustrated in figure 2-2 when doing noise analysis.

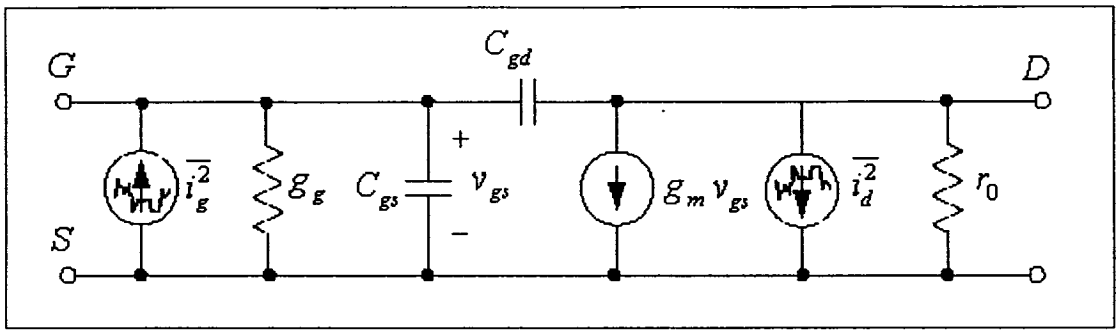

Figure 2-3: short channel small-signal equivalent circuit with noise generators

2.2 - Linearity and dynamic range

Linearity is the second important consideration in LNA design and while noise sets the sensitivity in a receiver (MDS), the maximum signal level is set by the linearity of the system. Also, it determines the Dynamic Range (DR) of the receiver since the DR is the ratio between the maximum and minimum detectable signal levels.

2.2.1 - Effects of nonlinearity

The non-linearity of a circuit is mainly due to the non-linear characteristics of the transistor. When the power of the input signal increases beyond the small-signal assumption (where we assume that harmonics are negligible) then non-linear effect becomes noticeable. Harmonics, gain compression, desensitization, cross-modulation and intermodulation are the effects of device nonlinearity.

Harmonics: Consider the transfer function of a practical nonlinear system [37]:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots\ldots \qquad (2.37)$$

where α_1, α_2 *and* α_3 are the gain second- and third-order distortion coefficients. By applying the sinusoid signal $x(t) = A\cos wt$ at the input of the nonlinear system we get:

$$y(t) = \alpha_1 A\cos wt + \alpha_2 A^2\cos^2 wt + \alpha_3 A^3\cos^3 wt + ...$$

$$y(t) = \alpha_1 A\cos wt + \frac{\alpha_2 A^2}{2}(1+\cos 2wt) + \frac{\alpha_3 A^3}{4}(3\cos wt + \cos 3wt) + ...$$

$$y(t) = \underbrace{\frac{\alpha_2 A^2}{2}}_{DC} + \underbrace{\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)}_{fundamental}\cos wt + \underbrace{\frac{\alpha_2 A^2}{2}}_{2^{nd}\ Harmonic}\cos 2wt + \underbrace{\frac{\alpha_3 A^3}{4}}_{3^{rd}\ Harmonic}\cos 3wt... \qquad (2.38)$$

Equation (2.38) shows that the response has a DC component, which is very harmful to direct conversion receivers. Equation (2.38) also shows that the response has even and odd harmonics. Note here that the mismatches in fully differential LNA structures corrupt the symmetry, yielding finite even-order harmonics.

Gain Compression: Gain compression (saturation) occurs when the input signal amplitude increases beyond the linear range of the device. In Equation (2.38) if $\alpha_3 < 0$ then the gain $\underbrace{\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)}_{fundamental}$ becomes a decreasing function of A. The 1-dB compression point occurs when the difference between the nonlinear gain and its ideal linear version becomes 1 dB as seen in figure 2-4. One can calculate the 1-dB point as follow:

$$20\log_{10}|\alpha_1| - 20\log_{10}\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{1-dB}^2\right| = 1dB \qquad (2.39)$$

Solving for Equation (2.39):

$$A_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \qquad (2.40)$$

In a practical receiver the 1-dB point occurs around –15 to –25 dBm.

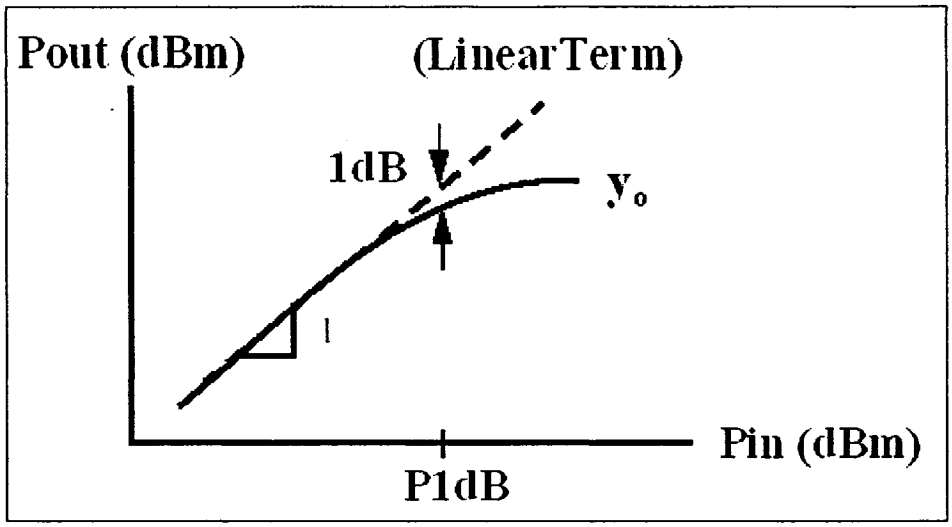

Figure 2-4: Definition of the 1-dB compression

***Desensitization and Blocking*:** In a circuit with compressive characteristics (i.e. $\alpha_3 < 0$ in equation (2.38)), a large interferer tends to reduce the gain or "block" a desired weak signal. Known also as "desensitization," this phenomena can be appreciated by assuming a two-tone signal, $x(t) = A_1 \cos w_1 t + A_2 \cos w_2 t$, as input for the system given by equation (2.37). The output is given by:

$$y(t) = \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2 \right) \cos w_1 t + \ldots \tag{2.41}$$

When $A_1 << A_2$ equation (2.41) becomes:

$$y(t) = \left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2 \right) A_1 \cos w_1 t + \ldots \tag{2.42}$$

The gain of the desired signal is $\left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2 \right)$, which is a decreasing function of A_2 when $\alpha_3 < 0$. When A_2 is large enough, the gain will drop to zero, and the signal will be blocked.

2.2.2 - *Intermodulation distortion:*

Intermodulation distortion occurs when two signals of different frequencies $w_1$and w2 are applied to a nonlinear system, resulting in corruption of the nearby desired signal, as seen in figure 2-5. In the case of third-order intermodulation distortion, the output signal consists of frequency components at $2w_1 - w_2$ and $2w_2 - w_1$. For the transfer function in equation (2.37), if the input signal is $x(t) = A_1 \cos wt + A_2 \cos w_2 t$ then:

$$y(t) = \alpha_1(A_1 \cos w_1 t + A_2 \cos w_2 t) + \alpha_2(A_1 \cos w_1 t + A_2 \cos w_2 t)^2 + \alpha_3(A_1 \cos w_1 t + A_2 \cos w_2 t)^3$$

$$= \ldots + \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2w_1 + w_2)t + \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2w_1 - w_2)t$$

$$+ \frac{3\alpha_3 A_2^2 A_1}{4}\cos(2w_2 + w_1)t + \frac{3\alpha_3 A_2^2 A_1}{4}\cos(2w_2 - w_1)t$$

$$+ \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos w_1 t + \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2\right)\cos w_2 t + \ldots + \ldots$$

Let $A_1 = A_2$ then $y(t)$ becomes:

$$y(t) = \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right)A\cos w_1 t + \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right)A\cos w_3 t$$

$$+ \frac{3}{4}\alpha_3 A^3 \cos(2w_1 + w_2)t + \frac{3}{4}\alpha_3 A^3 \cos(2w_2 - w_1)t + \ldots$$

If $\alpha_1 >> \frac{9}{4}\alpha_3 A^2$ then the input level (IIP3) for which the output components (OIP3) at w_1 and w_2 have the same amplitude as those at $(2w_1 + w_2) and (2w_2 - w_1)$ is given by:

$$|\alpha_1| A_{IIP3} = \frac{3}{4} A_{IIP3}^3 \qquad (2.43)$$

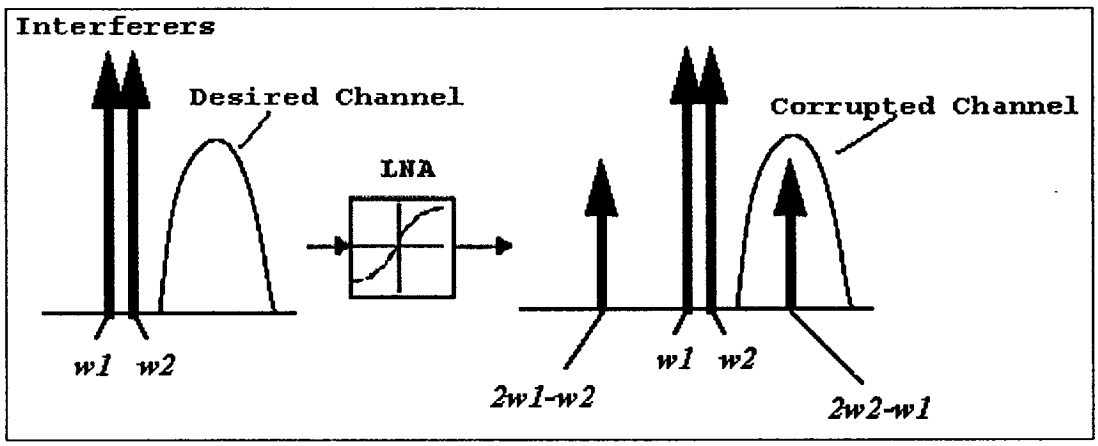

Figure 2-5: Signal corruption due to two-tone intermodulation

Thus, the IIP3 is equal to:

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.44}$$

and the OIP3 is equal to:

$$OIP3 = \alpha_1 A_{IP3} \tag{2.45}$$

Finally, figure 2-6 below is a geometric interpretation of the above using a log-log scale.

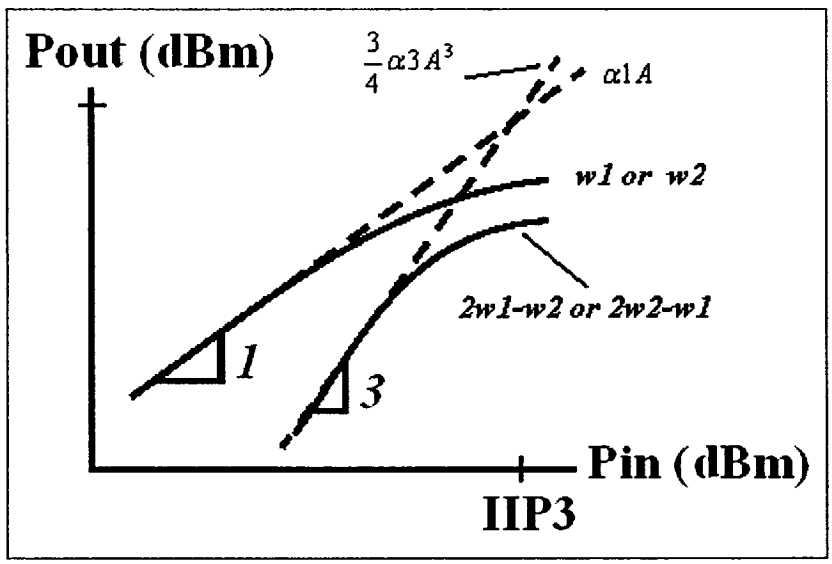

Figure 2-6: Third-order Intercept Point

2.3 - LNA performance metrics

Noise Figure: The noise performance of an LNA may be characterized by a couple of different metrics, such as, noise factor and noise figure. Noise figure is the most common metric used to measure how much the LNA degrades the signal to noise ratio (SNR) of the received signal. Noise Figure is defined as:

$$NF = 10\log_{10} F \tag{2.46}$$

Where F is the noise factor and given by:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \tag{2.47}$$

S_{in} and N_{in} are the signal and noise power at the LNA input, respectively, while S_{out} and N_{out} are the signal and noise power at the LNA output, respectively, and equal to:

$$S_{out} = G_p S_{in} \tag{2.48}$$

$$N_{out} = G_p N_{in} + N_a \tag{2.49}$$

where N_a is the available noise power of the subsequent stage. Substituting (2.48) and (2.49) into (2.47) we get:

$$F = 1 + \frac{N_a}{G_p N_{in}} \tag{2.50}$$

Another definition of noise factor is:

$$F \equiv \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} \tag{2.51}$$

or alternatively one may write:

$$F \equiv 1 + \frac{output\ noise\ due\ to\ injected\ noise}{output\ noise\ due\ to\ input\ source} \tag{2.52}$$

A common term used to evaluate the noise of an LNA is the noise figure and is given by:

$$NF = 10\log_{10} F = SNR_{in}(dB) - SNR_{out}(dB) \tag{2.53}$$

LNA Noise Measure: Another important and significant LNA performance metric is the LNA noise measure. Specifying noise figure of an LNA is meaningless without also specifying its gain since, a noiseless transmission line may have a zero dB noise, but without amplification. A metric less commonly used to characterize the noise performance of an LNA is noise measure. Noise measure accounts for both the noise and gain of the LNA and is given by [41]:

$$M \equiv \frac{F-1}{1-1/G} \tag{2.54}$$

where F and G are the LNA noise factor and power gain, respectively. LNA noise measure is an excellent metric, summarizing the performance of two important LNA performances.

Cascade NF and IIP3: For a cascade of matched stages, the overall noise figure can be obtained in terms of the NF and gain of each stage using Friis equation [42] as follow:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{P1}} + \ldots + \frac{NF_m - 1}{A_{P1} \cdots A_{P(m-1)}} \tag{2.55}$$

where NF_i is the noise factor of the i^{th} stage with respect to the source impedance driving that stage and A_{pi} is the power gain of the i^{th} stage.

In a similar fashion, we can evaluate the linearity of a cascade system. Assuming that all distortion products add in power fashion, we arrive at the following expression for IIP3:

$$\frac{1}{IIP3} \approx \frac{1}{IIP3_1} + \frac{G_{a1}}{IIP3_2} + \frac{G_{a1}G_{a2}}{IIP3_3} + \cdots \tag{2.56}$$

where $IIP3_i$ is the input-referred third-order intercept point of the i^{th} stage expressed in terms of available source power, and G_{ai} is the available power gain of the i^{th} stage. Finally, using equations (2.55) and (2.56), one can design a receiver that maximizes IIP3 and minimizes NF.

2.4 – Conclusion

The origins and natures of Noise and nonlinearity have been covered in details in this chapter. The next chapters will elaborate more on techniques that minimize the occurrence of these two characteristics in MOSFET transistors. Designs that reduce the thermal noise in a MOSFET channel and that cancels the signal's third harmonics will be discussed.

Chapter 3 - LNA Design and Optimization

3.1 Introduction

In the last chapter we have discussed various device and system level parameters that are of concern towards implementation of a low noise amplifier (LNA) using a sub-micron MOS technology. In this chapter we shall work with several of those parameters and indicate how these parameters could be optimized to achieve low noise figure and highly linear LNA. In addition to the aforementioned parameters, Other LNA topics such as input matching design and power gain optimization will be covered in this chapter. Towards this, section two of this chapter will presents the input stage design and input matching while section three will cover advanced design optimization topics such as gain, noise figure and linearity and conclude with the design of the common gate transistor amplifier.

3.2 - Input stage design and matching

3.2.1 - Input stage topology

A good input match is critical especially when a sharp SAW filter precedes the LNA, because such a filter is very sensitive to the quality of their terminating impedances as seen in figure 3-1. With this goal in mind, providing controlled input impedance (i.e. choosing the input stage) is an important stage of LNA design. Three input-stage topologies are considered in figure 3-2. All the topologies have been used in previously

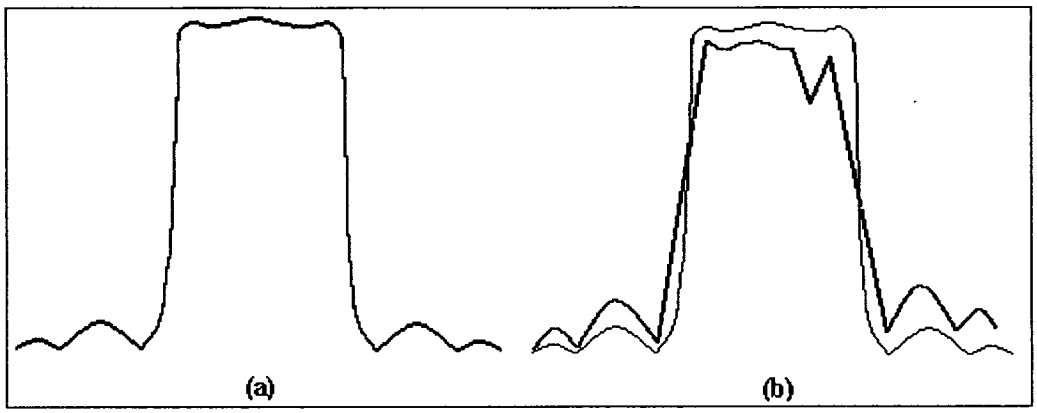

Figure3-1: Saw Filter termination: (a) perfect matched (b) Badly matched

reported LNA designs, each for a specific application. The first topology is shown in figure 3-2(a); it uses inductive source (or emitter) degeneration (L-Deg.) to generate a real term in the input impedance. This is the most used technique for narrow band LNAs and proves to provide the best noise performance and good stability. The second approach, Local Shunt Feedback, is shown in figure 3-2(b). Although usually used for broadband application, a narrowband input match may be achieved by adding a shunt inductor at the input of the LNA, in order to resonate with the gate capacitance of the transistor. One drawback for this design is the usage of passive resistors that consume more power and generate noise. The last approach, 1/gm termination shown in figure 3-2(c), uses the

Table 3-1: Summary of LNA's topology performance ($\alpha = 0.85, \delta = 4, c = j0.45$)

TOPOLOGY/METRICS	$F_{50\Omega}$	Z_{in}	A_V
CS with L-Deg.	≥ 1	$\frac{g_m L_S}{C_{gs}}$	$-j\frac{R_L}{wL_s}$
Common gate	$\geq 1 + \frac{\gamma}{\alpha}$ ≥ 3.4	$\frac{1}{g_g + g_m}$	$g_m R_L$
LSF	≥ 1	$\frac{R_f + R_l}{1 + g_m}$	$-g_m(R_F \Vert R_L)$

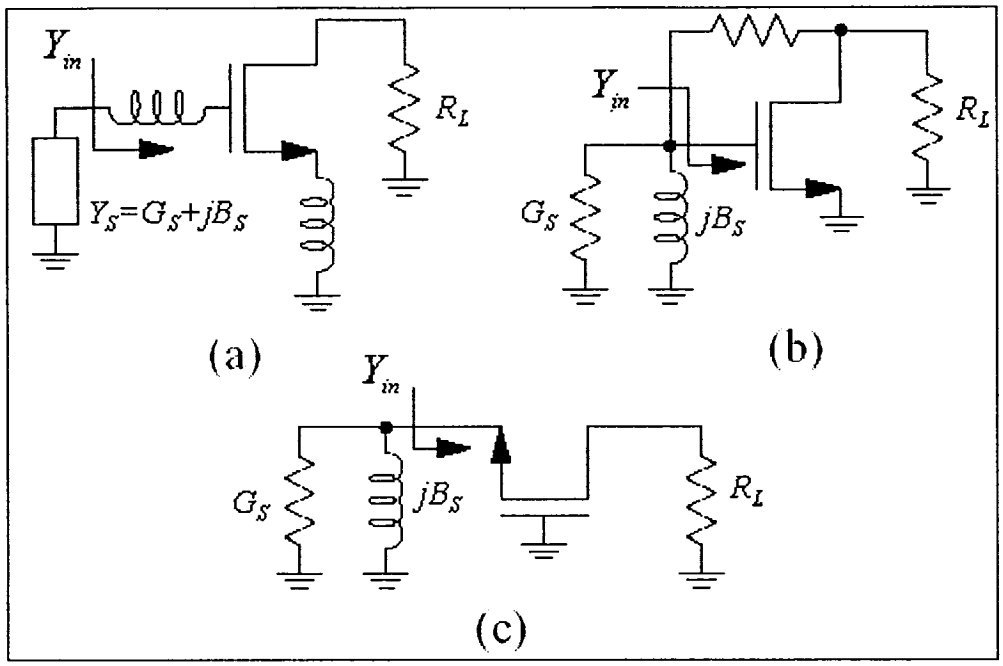

Figure 3-2: Common LNA input stages architectures. (a) Inductive degeneration. (b) Local Shunt Feedback. (c) 1/gm termination

source of a common-gate as the input termination. This topology has a poor $NF_{\min}$. In this work L-deg will be used for its superior performance and suitability for narrow band LNA. Below in table 3-1, a performance comparison of the three topologies is provided. The derivation of common source with inductive degeneration will be provided in section 3.2.4. The remaining derivations could be found using similar approach.

3.2.2 - Power versus noise matching

RF designers often refer to a source and load as being "power matched." By "power matched," they actually mean that for a given source impedance, the load impedance is such that the maximum available power is transferred to the load from the source. Another similar definition is "impedance matching". An impedance match happens when

the reflection coefficient (S_{11} or S_{22}) is equal to zero. There is a subtle difference between impedance matching and power matching. To clarify this ambiguity considers the diagram in figure 3-3 below. The condition for noise matching occurs when the load impedance is equal to the source impedance ($Z_L = Z_S$). However, the condition for power matching occurs when the load impedance is the complex conjugate of the source impedance $Z_L = Z_S^*$ (power gain matching). When the impedances are real, the conditions for power matching and impedance matching become identical. This is not the case in our work and that is why it is impossible to match for both noise and power at the same time.

3.2.3 - Non-quasi static effect

Often ignored, NQS effect is one of the important considerations that need to be taken into account when designing a high frequency CMOS LNA. This is especially true when input matching is implemented using bonding wires (i.e. high Q inductors). This section, will introduce this phenomenon by revealing its physical origins and discussing its importance.

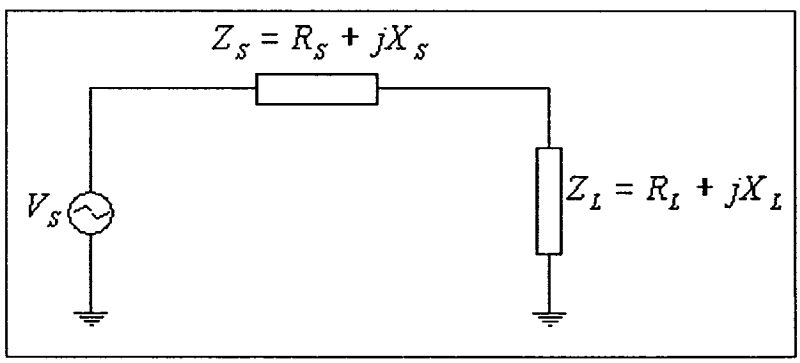

Figure 3-3: RF Source and load system impedance

MOS transistors operating at low frequencies ($w_o << w_T$) can be modeled only by the capacitance from gate to source (C_{gs}), since the inversion layer channel charge builds up fast enough relative to the frequency of the applied signal. However, at high frequencies this assumption is not valid due to the finite channel conductance that limits the speed of the build-up of the inversion layer. As a result, the channel needs time to achieve equilibrium with the source and drain voltages. This high frequency phenomenon is called the non-quasi static effect (NQS). Figure 3-4 present a simplified small-signal non-quasi static equivalent circuit model proposed in [42]. The value of the non-quasi static gate resistance in saturation can be determined, and is given by:

$$r_{g,NQS} = \frac{1}{\kappa g_m} = \frac{1}{6 g_m} \tag{3.1}$$

The above equation was derived using long channel transistor model, without considering short-channel effects. This resistance will affect the LNA performance and should be modeled as a resistance in series with the gate source capacitance, especially if the simulator doesn't support the NQS effect such as BSIM 3V3 (used by Spectre™). When a designer uses the package bonding wire for indirect input matching (i.e. high Q inductor), the series resistance due to NQS effect is dominant and influences the quality

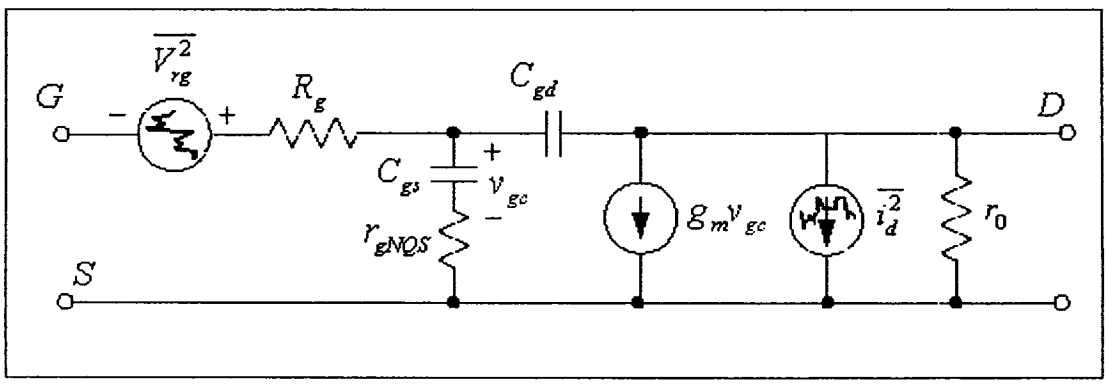

Figure 3-4: First order small signal model including NQS effect.

factor of the LNA and its bandwidth. As a result, the designer may fail to meet the design specifications due to this resistance.

3.2.4 - Input stage matching

Matching for minimum noise figure is a key design goal when designing LNA. In this section a complete derivation of matching formulae will be presented, as well as, an expression for optimum C_{gs} (the gate to source capacitance) that leads to optimum noise factor (F). A simplified small-signal model of the common source with inductive degeneration input stage is given in figure 3-5. The quantity g_g in figure 3-5 includes the NQS parasitic resistor, as well as, the serial parasitic resistance of the gate inductor. For the following analysis we will ignore g_g in order to simplify the mathematics and since the following condition is met:

$$w << \frac{5w_T}{\alpha} \tag{3.2}$$

where $\alpha \approx 0.8$ for 0.18μm process technology and f_T is about 70 GHz[5]. For the circuit in figure 3-5 the input impedance is given by:

$$Z_{in} = jw(L_g + L_s) + \frac{1}{jwC_{gs}} + \frac{g_m L_s}{jwC_{gs}} = w_T L_S - j\frac{1 - w^2 C_{gs}(L_g + L_s)}{wC_{gs}} \tag{3.3}$$

Where $w_T = 2 \times \pi \times f_T \approx \frac{g_m}{C_{gs}}$. A 50 ohm impedance match is achieved when $Z_{in} = 50$ in (3.3) this will result in the following two equations:

$$w_T L_s = R_S = 50 \tag{3.4}$$

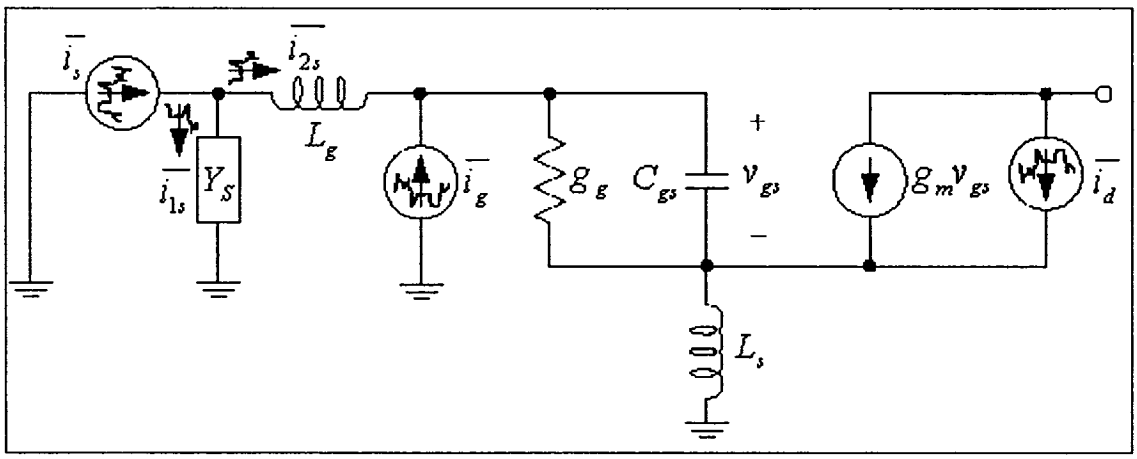

Figure 3-5: inductive degenerated common source amplifier small-signal model

$$L_g + L_s = \frac{1}{w^2 C_{gs}} \tag{3.5}$$

***Matching for Noise*:** Now using the definition given in (2.52) and knowing that a noise signal is random variable, the noise factor is given by:

$$F = 1 + \frac{VAR\left[\overline{i_{og}} + \overline{i_{od}}\right]}{\overline{i_{os}^2}} \tag{3.6}$$

Where the sum of two random variables has a variance:

$$VAR[A+B] = VAR[A] + VAR[B] + E[AB^*] + E[A^*B] \tag{3.7}$$

Where A^**and* B^* is the complex conjugate of A and B, the noise factor becomes:

$$F = 1 + \frac{\overline{i_{og}^2} + \overline{i_{og}^2} + \overline{i_{og}^* i_{od}} + \overline{i_{og} i_{od}^*}}{\overline{i_{os}^2}} \tag{3.8}$$

Using the superposition theorem, we will develop an expression for the noise factor in terms of drain, source, and induced gate noises. The noise developed at the drain of the input device due to source current noise $\overline{i_s}$ could be found as follows:

$$\frac{\overline{i_{1s}}}{\overline{i_{2s}}} = \frac{\overline{i_s - i_{2s}}}{\overline{i_{2s}}} = \frac{Y_{eq1}}{Y_{eq2}} = \frac{\left[G_s + jB_s\right]\left[1 - w^2 C_{gs}(L_g + L_s)\right]}{jwC_{gs}} \tag{3.9}$$

where $Y_{eq1} = Y_S = G_S + jB_S$ and $[Y_{eq2}]^{-1} = jwL_s + \frac{1}{jwC_{gs}}$

Equation (3.9) can be rewritten as a function of $\overline{i_s}$ as follows:

$$\overline{i_{2s}} = \frac{\overline{i_s} jwC_{gs}}{G_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + j\left\{B_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + wC_{gs}\right\}} \tag{3.10}$$

Thus, the output noise $\overline{i_{os}}$ due to source noise $\overline{i_s}$ is equal to:

$$\overline{i_{os}} = g_m v_{gs} = \frac{\overline{i_s} g_m}{G_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + j\left\{B_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + wC_{gs}\right\}} \tag{3.11}$$

For simplicity, we assumed here that conductance due to g_g is negligible compared to other conductance elements. In a similar manner, the output noise due to induced gate noise $\overline{i_{og}}$, drain current noise $\overline{i_{od}}$ and source current noise $\overline{i_{os}}$ are determined as:

$$\overline{i_{og}} = \frac{g_m \overline{i_g}\left[1 + jwL_g G_s - B_s wL_g\right]}{G_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + j\left\{B_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + wC_{gs}\right\}} \tag{3.12}$$

$$\overline{i_{od}} = \overline{i_d} \tag{3.13}$$

$$\overline{i_s^2} = 4kTG_S\Delta f \tag{3.14}$$

On the other hand, $\overline{i_{og} i_{od}^*}$ is given by:

$$\overline{i_{og} i_{od}^*} = \frac{g_m \overline{i_g i_d^*}\left[1 + jwL_g G_s - B_s wL_g\right]}{G_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + j\left\{B_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + wC_{gs}\right\}} \tag{3.15}$$

and

$$\overline{i_{og}^* i_{od}} = \frac{g_m \overline{i_g^* i_d}\left[1 + jwL_g G_s - B_s wL_g\right]}{G_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] - j\left\{B_s\left[1 - w^2 C_{gs}(L_g + L_s)\right] + wC_{gs}\right\}} \tag{3.16}$$

From (2.32) we have:

$$\overline{i_g i_d^*} = \left(\overline{i_g^* i_d}\right)^* = j|c|\sqrt{\overline{i_g^* i_g} \times \overline{i_d i_d^*}} = c\sqrt{i_g^2 i_d^2} \tag{3.17}$$

Using (3.8)-(3.17), (2.7) and (2.9), the resulting noise factor is given by:

$$\begin{aligned} F = 1 + & \underbrace{\frac{\alpha\delta w^2 C_{gs}}{5 g_m G_S}\left[\left(1 - wB_S L_g\right)^2 + w^2 G_S^2 L_g^2\right]}_{F1} \\ & + \underbrace{\frac{\gamma}{\alpha g_m G_S}\left\{\begin{array}{l}\left[B_S\left[1 - w^2 C_{gs}(L_g + L_s)\right] + wC_{gs}\right]^2 \\ + G_S^2\left[1 - w^2 C_{gs}(L_g - L_s)\right]^2\end{array}\right\}}_{F2} \\ & + \underbrace{2|c|\sqrt{\frac{\gamma\delta}{5}}\frac{wC_{gs}}{g_m G_s}\left\{\begin{array}{l}\left(1 - wB_S L_g\right)\left[wC_{gs} + B_s\left[1 - w^2 C_{gs}(L_g + L_s)\right]\right] \\ - wL_g G_S^2\left[1 - w^2 C_{gs}(L_g + L_s)\right]\end{array}\right\}}_{F3} \end{aligned} \tag{3.18}$$

Here it is assumed that the SAW filter preceding the LNA is matched with a 50 ohms or a pure real impedance and hence, B_S is set equal to zero. Taking this assumption into consideration and after substituting (3.5) into (3.18), the later equation can be rewritten as follows:

$$F = 1 + \underbrace{\frac{\alpha\delta w^2 C_{gs}^2}{5 g_m G_S}\left(1 + \frac{G_S^2}{w^2 C_{gs}^2}\right)}_{F1} + \underbrace{\frac{\gamma w^2 C_{gs}^2}{\alpha g_m G_S}}_{F2} + \underbrace{2|c|\sqrt{\frac{\gamma\delta}{5}}\frac{w^2 C_{gs}^2}{g_m G_s}}_{F3} \tag{3.19}$$

Optimum C_{gs} **:** Now it is easy to determine the optimum gate to source capacitance that optimizes the noise factor of the LNA. Substituting g_m by its equivalent expression given by:

$$g_m = \sqrt{2 I_D C_{ox} \mu_{eff} \frac{W}{L}} \tag{3.20}$$

and knowing that W is given by:

$$W = \frac{3C_{gs}}{2LC_{gs}} \tag{3.21}$$

The final expression of g_m will become:

$$g_m = \frac{\sqrt{3I_D\mu_{eff}C_{gs}}}{L} \tag{3.22}$$

After the substitution of (3.22) into (3.19) we get:

$$F = 1 + \underbrace{\frac{\alpha\delta w^2 C_{gs}^2 L}{5\sqrt{3I_D\mu_{eff}C_{gs}}G_S}\left(1+\frac{G_S^2}{w^2C_{gs}^2}\right)}_{F1} + \underbrace{\frac{\gamma w^2 C_{gs}^2 L}{\alpha\sqrt{3I_D\mu_{eff}C_{gs}}G_S}}_{F2} + \underbrace{2|c|\sqrt{\frac{\gamma\delta}{5}}\frac{w^2C_{gs}^2L}{\sqrt{3I_D\mu_{eff}C_{gs}}G_s}}_{F3} \tag{3.23}$$

In (3.23) the only variable is C_{gs}. The value of C_{gs} that optimizes F is the result of the following equation:

$$\frac{\partial F}{\partial C_{gs}} = 0 \tag{3.24}$$

Using (3.24), the optimum value of C_{gs} is given as:

$$C_{gsopt} = \frac{G_S}{w}\sqrt{\frac{\delta}{15\left(\frac{\delta}{5}+\frac{\gamma}{\alpha^2}+2|c|\sqrt{\frac{\delta\gamma}{5}}\right)}} \tag{3.25}$$

After finding the optimum value of C_{gs} we can determine the gate and source inductor value given in (3.4) and (3.5) and finalize the input matching network.

Finally, note that the value of C_{gs} depends and is controlled by the geometry of the device layout or in other words, the number of fingers of the interdigitated device and its width, as given in (3.21). When targeting optimum C_{gs} the designer must consider also the length and sheet resistance of the MOSFET polysilicon gate. The length of the

MOSFET gate affects the effective transconductance and this topic will be covered in chapter four. The designer should redesign the matching network based on a fixed power budget and variable transconductance, in order to keep the gate resistance low.

3.2.5 - Effective transconductance, PCC and PVC.

Before starting the next section about LNA performance optimization, three important LNA parameters need to be defined namely: $g_{m.eff}$, PCC, and PVC.

Effective transconductance: The amplification of an RF MOS device depends on its effective transconductance as seen in figure 3-6 and it is defined as:

$$\left|g_{m.eff}\right| = \frac{i_{out}}{v_s} = \frac{g_m}{w_o C_{gs}\left(R_S + w_T L_s\right)} \approx \frac{w_T}{2w_o R_S} \tag{3.26}$$

In the above equation we assumed a power matched device thus we used (3.4) to simplify (3.26). As shown in (3.26), $g_{m.eff}$ does not depend on device transconductance but on the device cut-off frequency w_T, the operating frequency w_o and the source resistance R_S. Thus, (3.26) could be rewritten in terms of device transconductance as following:

$$\left|g_{m.eff}\right| = Q_M g_m = \frac{v_{gs}}{v_s} g_m = \frac{g_m}{2w_o R_S C_{gs}} \tag{3.27}$$

where Q_M (or Q_{in}) is the quality factor of the input matching network.

PCC: PCC, or power to current conversion, is the second term which needs to be defined. It indicates how much input power is being converted into current at the output and is given by:

$$PCC = \frac{i_{out}^2}{P_{av}} \tag{3.28}$$

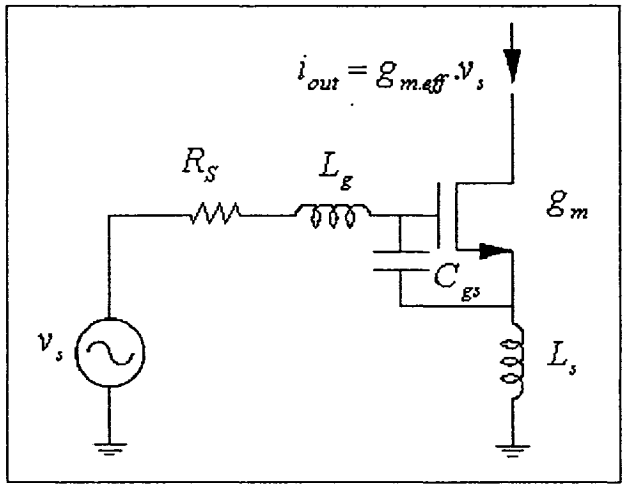

Figure 3-6: MOS direct matching by inductive source degeneration

where i_{out} is the output current device and P_{av} is the available source power. PCC and $g_{m.eff}$ are closely related since v_s is given by:

$$v_s = 2\sqrt{P_{av} R_S} \tag{3.29}$$

Thus, PCC becomes:

$$PCC = 4 g_{m.eff}^2 R_S = \left(\frac{w_T}{w_o}\right)^2 \frac{1}{R_S} \tag{3.30}$$

PVC: When the LNA is driving an off-chip image filter, then the output power is the relevant quantity. Yet, when it is used to drive a capacitive load such as a MOS mixer, then the output voltage becomes the relevant quantity. Hence, we need a measure that quantifies how efficiently the signal power at the receiver's antenna is being converted into output voltage. The needed measure is known as PVC, or power to voltage conversion, and is given by:

$$PVC = \frac{v_{out}^2}{Pav} = PCC \times R_L^2 = \left(\frac{w_T}{w_o}\right)^2 \frac{R_L^2}{R_S} \tag{3.31}$$

where R_L is the resistive load seen by the common source NMOS amplifier and is mainly due to resonance tank's parallel resistance.

3.3 - LNA design optimization

The design and optimization of a CMOS LNA starts with a set of specifications like DC power budget and power gain, noise figure, linearity and bandwidth. The LNA is a do-it-all amplifier and in order to meet all the design specification, the designer should follow an orderly approach.

First of all the power gain specification is normally set to minimum acceptable value and the designer should aim to meet this value or even try to exceed it, because high power gain helps in suppressing the overall noise in the receiver as suggested by equation (2.55).

The second consideration is noise figure. This specification is not independent. Limitations of power budget and bandwidth often make the achievement of this specification very challenging. Designers use contour plots to solve for noise figure with a given power budget and without violating the narrow bandwidth condition of the LNA. The overdrive voltage is one degree of freedom when designing for power and the quality factor of the input matching stage is another degree of freedom when designing for specific bandwidth.

The third and final consideration is the linearity of the LNA. Like power gain, specification for linearity is set to a minimum and the designer should meet or exceed this minimum. Although the LNA linearity does not dictate the overall linearity of the receiver, yet it is very important to design a linear amplifier. DC offset in equation (2.38) is one of the most difficult problems in direct conversion receivers and it is caused by MOSFET nonlinearity. The above discussion assumes a design that is bounded by a specific power budget that cannot be exceeded. Specification like noise figure and

linearity can be easily optimized at the cost of high power dissipation, yet this solution cannot be tolerated when designing for portable low power RFICs.

3.3.1 - Gain boosting techniques

The matching technique used in section 3.3, known as direct matching, is not the optimum one for power matching since the gain is fundamentally limited by the value of the source impedance as seen in equation (3.27). In [9] a more effective indirect matching scheme was presented as seen in figure 3-7. Using the RF pad (C_P) and wire bond inductor, the new method transforms the source impedance R_S into a lower $R_{S.Local}$ resistance. Using the power conservation theorem, the new effective transconductance becomes:

$$g_{m.eff} = \frac{w_T}{j2w_o R_S}\sqrt{\frac{R_S}{R_{S.Local}}} = \frac{w_T}{2jw_o\sqrt{R_S R_{S.Local}}} \tag{3.32}$$

The quality factor of the input matching network, Q_M and PCC becomes:

$$Q_M = \frac{1}{2w_o C_{gs}\sqrt{R_S R_{S.Local}}} \tag{3.33}$$

$$PCC = \left(\frac{w_T}{w_o}\right)^2 \frac{1}{R_{S.Local}} \tag{3.34}$$

Equations (3.32) and (3.34) clearly show that lowering $R_{S.Local}$ with respect to R_S will results in considerable increase in PCC and effective transconductance. Lowering $R_{S.Local}$ is limited by design specifications ($S11 \geq 10dB$) and the fact that the real part of

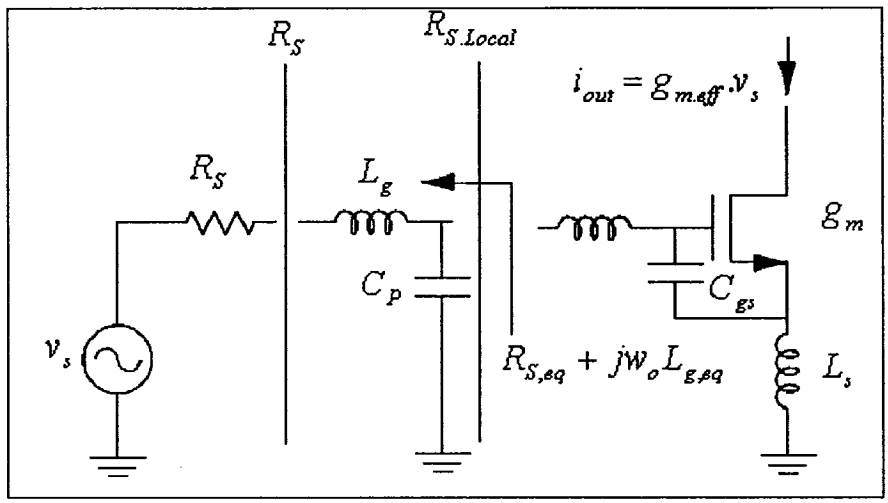

Figure 3-7: indirect matching

Z_{in} cannot be lower than $r_{gNQS} + w_T L_s$. The maximum achievable PCC becomes:

$$PCC = \left(\frac{w_T}{w_o}\right)^2 \frac{1}{r_{gNQS} + w_T L_s} \tag{3.35}$$

The above discussion suggests that L_s should be set to its lowest value. Also, r_{gNQS} should be set to its lowest value by increasing g_m of the device, or by increasing the number of fingers. The easiest way to achieve the indirect matching is by exposing r_{gNQS} through resonating C_{gs} against the gate inductor and then transforming R_S down to r_{gNQS}. Using the indirect matching method, L_g in (3.5) will be replaced by $L_{g.eq}$ shown in figure 3-6, where $L_{g.eq}$ and $R_{S.eq}$ are respectively given by:

$$L_{g.eq} = \frac{L_g - C_P\left(w_o^2 L_g^2 - R_S^2\right)}{w_o^2 C_P^2 R_S^2 + \left(1 - w_o^2 C_P^2 L_g\right)^2} \tag{3.36}$$

$$R_{S.eq} = \frac{R_S^2}{w_o^2 C_P^2 R_S^2 + \left(1 - w_o^2 C_P^2 L_g\right)^2} \tag{3.37}$$

Using (3.1) and (3.5), the minimum achievable $R_{S.eq}$ is given by:

$$R_{S.eq} = \underbrace{\frac{1}{\kappa g_m}}_{r_{gNQS}} + \underbrace{w_T\left(\frac{w_T}{w_o^2 g_m} - L_{g.eq}\right)}_{L_s} \tag{3.38}$$

When $\left(\frac{w_o}{w_T}\right)^2 << 1$ equation (3.38) can be rewritten as:

$$R_{S.eq} \cong \frac{2R_S\left(1+\frac{C_P w_T}{g_m}\right)^2}{\psi + \sqrt{\psi^2 - (\psi-1)^2\left(\frac{w_T}{w_o}\right)^2}} \tag{3.39}$$

where ψ is given by:

$$\psi = 1 + \frac{2C_P R_S w_o^2}{w_T}\left(1+\frac{C_P w_T}{g_m}\right) \tag{3.40}$$

The terms under the square root in (3.39) must be positive, this will translate into following:

$$R_S \le \frac{1}{2w_o C_P\left(1+\frac{C_P}{C_{gs}}\right)} \tag{3.41}$$

Meeting the condition in (3.41) becomes hard when either C_P or w_o becomes high (figure 3-8). Various techniques used to keep the value of C_P low will be discussed in the next chapter. Note that the effective value of C_P is higher than its fixed one and given by:

$$C_P = C_{P.fixed} + 0.3 \times C_{gs} \tag{3.42}$$

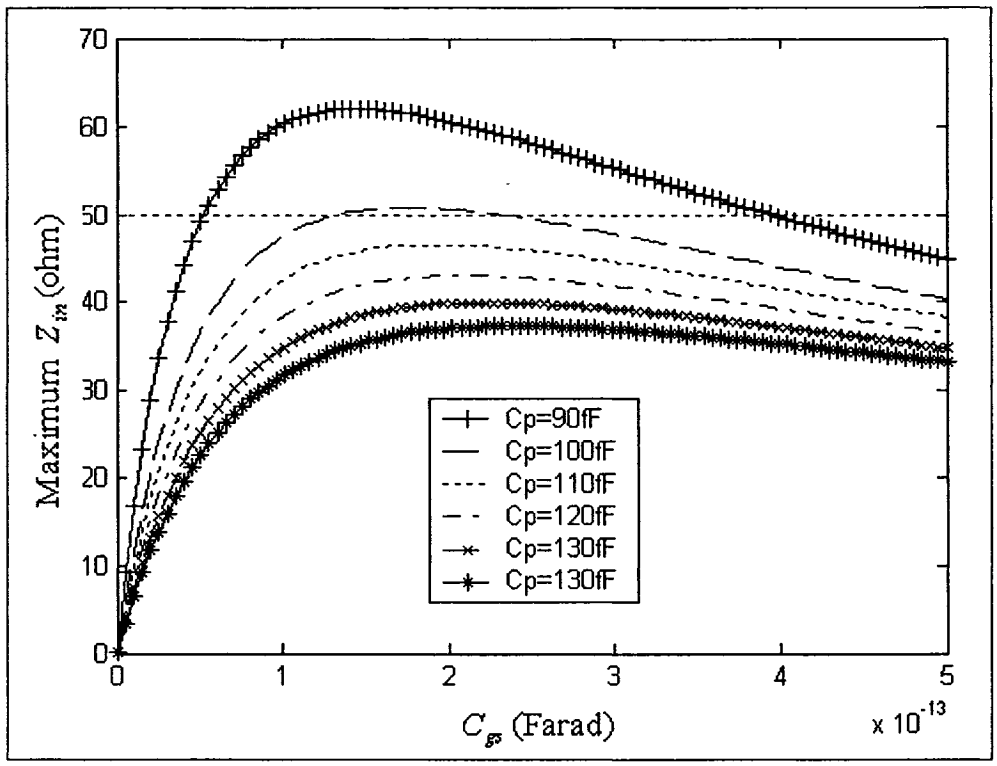

Figure 3-8: maximum achievable impute impedance at 5 GHz as a function of C_{gs} and $C_{p,fixed}$

It may also include the capacitance due to ESD protection.

When acheiving $R_{S.eq} < 50\Omega$ becomes difficult, then boosting the LNA gains (PCC, PVC and S21) without changing the cascode architecture could be achieved in two ways. First by increasing the value of R_L for PVC (i.e. using load inductor with higher quality factor) without violating the LNA specification, since a high Q inductor will affect the whole quality factor of the LNA (Q_{LNA}) hence its bandwidth$\left(Q_{LNA} = {}^{w_o}/_{Bandwidth}\right)$.

The second solution that increases both PCC and PVC is increasing w_T of the amplifying device through biasing (at the cost of higher DC power consumption). In this work, w_T was increased by using the parasitic BJT built in the substrate of the MOSFET device, without increasing $v_{overdrive}$ or the bias current, as will be shown in next chapter.

3.3.2 - Noise figure optimization within a given power budget

A practical and effective way to optimize the LNA noise figure is by using contour plots of precise NF equations in terms of DC power, input matching network quality factor and effective transconductance. In [7], the expression of noise factor was derived and found to be equal to:

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma\chi}{\alpha Q_M}\left(\frac{w_o}{w_T}\right) \tag{3.43}$$

where

$$\chi = 1 + 2|c|Q_M\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + Q_M^2\right) \tag{3.44}$$

and R_l , R_g are the resistive losses of the inductors and MOS amplifier polysilicon gate.

It was also found that the DC power dissipation and gate bias voltage could be related to the noise figure using the following equation:

$$NF = 10\times\log_{10}(F) = 10\times\log_{10}\left(1 + \frac{\gamma w_o L_{eff}}{3v_{sat}}\frac{\frac{P_D}{P_o}P_1(\rho) - P_2(\rho) + \frac{P_o}{P_D}P_3(\rho)}{\rho^3\left(1+\frac{\rho}{2}\right)^2(1+\rho)}\right) \tag{3.45}$$

with

$$P_o = \frac{3}{2}\frac{V_{DD}v_{sat}E_{sat}}{w_o R_S}$$

$$P_1(\rho) = (1+\rho)^6 + \frac{\delta}{5\delta}(1+\rho)^2\left(1+\frac{\rho}{2}\right)^2 \quad and \quad \rho = \frac{V_{overdrive}}{L_{eff}E_{sat}}$$

$$P_2(\rho) = 2|c|\sqrt{\frac{\delta}{5\delta}}(1+\rho)^3\left(1+\frac{\rho}{2}\right)\rho^2$$

$$P_3(\rho) = \frac{\delta}{5\gamma}\left(1+\frac{\rho}{2}\right)\rho^4$$

$$P_D = V_{DD} I_D = V_{DD} W_{eff} C_{ox} v_{sat} \frac{V_{overdrive}^2}{V_{overdrive} + L_{eff} E_{sat}}$$

After substituting the 0.18 μm technology parameters $(V_{DD}, v_{sat}, \delta, \gamma, \alpha, c)$ in (3.45) Matlab™ was used to create the first contour plot that relate the noise figure (NF) to dissipated DC power (P_D) and $V_{overdrive}$.

The resulting contour plots seen in figure 3-9 mimics the simulated results using Cadence™. Note that for a given dissipated DC power (or bias current), there exists a window of about 20 mV of DC overdrive voltage that minimizes the power consumption. In Equation (3.45) we assumed a fixed DC power dissipation, and then optimize $V_{overdrive}$.

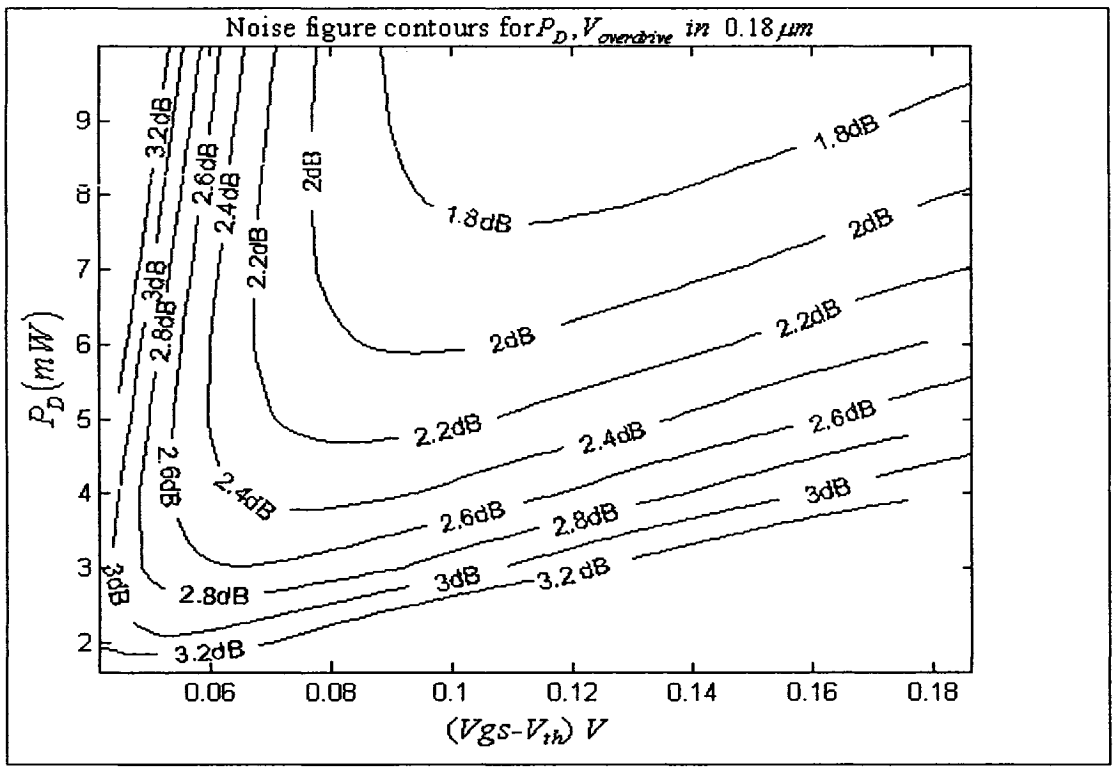

Figure 3-9: Contour plots of constant noise figure (dB) relating the overdrive voltage and P_D, for L_{eff}= 0.135um; w_o= 31.4 Grps, V_{DD}= 1 V, γ=1.4, δ=2.6, c=0.45, v_{sat}=0.9m/s, E_{sat}=6x10^4 V/m, α =0.85.

Another important approach is to assume a fixed effective transconductance for the amplifier and find the optimum Q_M that optimizes NF. The effective transconductance $g_{m.eff}$ is related to w_T by the equation (3.26), using this relation and substituting w_T in (3.43) we get:

$$F = 1 + \frac{\gamma}{\alpha} \frac{1 + 2|c|Q_M \sqrt{\frac{\delta\alpha^2}{5\delta}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_M)}{2\alpha Q_M R_S g_{m.eff}} \tag{3.46}$$

The contour plots of equation (3.46) are seen in figure 3-10 below, Q_M that optimize NF is equal to 2.7. Using equation (3.27) one can find the optimum value of C_{gs} (hence, the amplifier optimum width) based on this design approach. Note that the value of Q_M that optimizes NF, is not the same one that optimizes PCC and PVC. This is another proof of the impossibility of simultaneous noise and power matching of narrow band LNA.

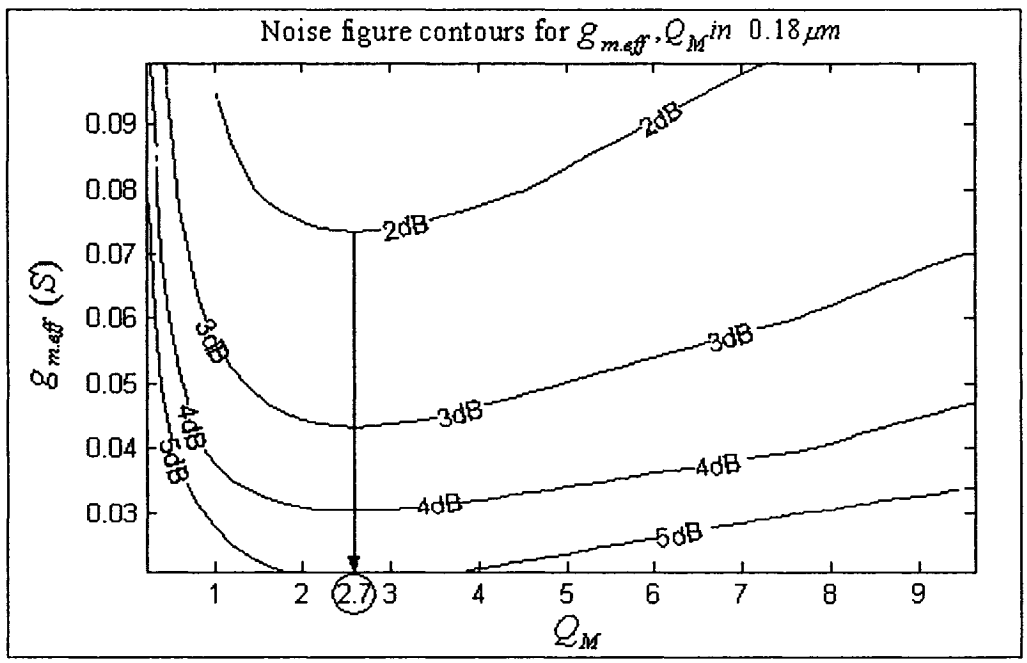

Figure 3-10: Contour plots of constant noise figure (dB) relating Q_M and $g_{m.eff}$, for w_o = 31.4 Grps, α = 0.85, γ = 1.4, δ = 2.6, c=0.45.

$Q_{M\_opt\_g_m}$ could be found also by solving the partial differential equation of (3.46) with respect to Q_M as:

$$Q_{M\_opt\_g_m} = \sqrt{1+\frac{5\delta}{\delta\alpha^2}} \tag{3.47}$$

In a similar way it was found in [7] that Q_{M_opt} for a fixed power budget is given by:

$$Q_{M\_opt\_PD} \cong |c|\sqrt{\frac{5\delta}{\delta}}\left[1+\sqrt{\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] = 4.15 \tag{3.48}$$

Note that $Q_{M\_opt\_PD} > Q_{M\_opt\_g_m}$ and therefore using $Q_{M\_opt\_PD}$ will help in compromising between good NF and optimum power matching.

Finally, the discussion about NF optimization in this section is based on the assumption that the RF layout of the chip is already optimized in a way that minimizes all sorts of exotic noise sources such as, bulk current noise, parasitic gate resistance, etc, as well as, a proper sizing of the cascode transistor (common gate) that minimizes NF. All these topics will be covered in later sections.

3.3.3 - Linearity optimization

Based on earlier work done in [44], a set of equations relating IIP3 with drain current and overdrive voltage were developed in [9] and [45] and are given by:

$$IIP3 = 10\log\left(\frac{4}{3}\frac{V_{overdrive}(1+\theta V_{overdrive})^2}{\theta}\right) + 20\log\left(w_o C_{gs}(R_{eq}+R_{in})\sqrt{\frac{50}{R_{eq}}}\right) - 10 \tag{3.49}$$

and

$$I_D = \frac{KW_{eff}}{L_{eff}} V_{overdrive}^2 \frac{1}{(1-\lambda V_{DS})(1+\theta V_{overdrive})} \tag{3.50}$$

where θ is a technology dependent constant that shows the mobility degradation and is approximately equal to 4.5 V^{-1} for 0.18 μm technology. Contour plots of IIP3 (i.e. equation 3.49) are shown in figure 3-11 above. These plots are only valid for MOS devices biased in saturation and clearly show that IIP3 is proportional to the drain current and the overdrive voltage. It is clear that it is difficult to get a good linearity at drain current below 2 mA. Note also that for a good noise figure performance, the overdrive voltage should be kept as low as possible (about 0.13 volts in the design presented by this work) and hence, a higher drain current is needed for good linearity.

For a device biased in triode, the linearity specs can in principle be obtained at a near zero current when the overdrive voltage is extremely low. For these conditions, the IIP3

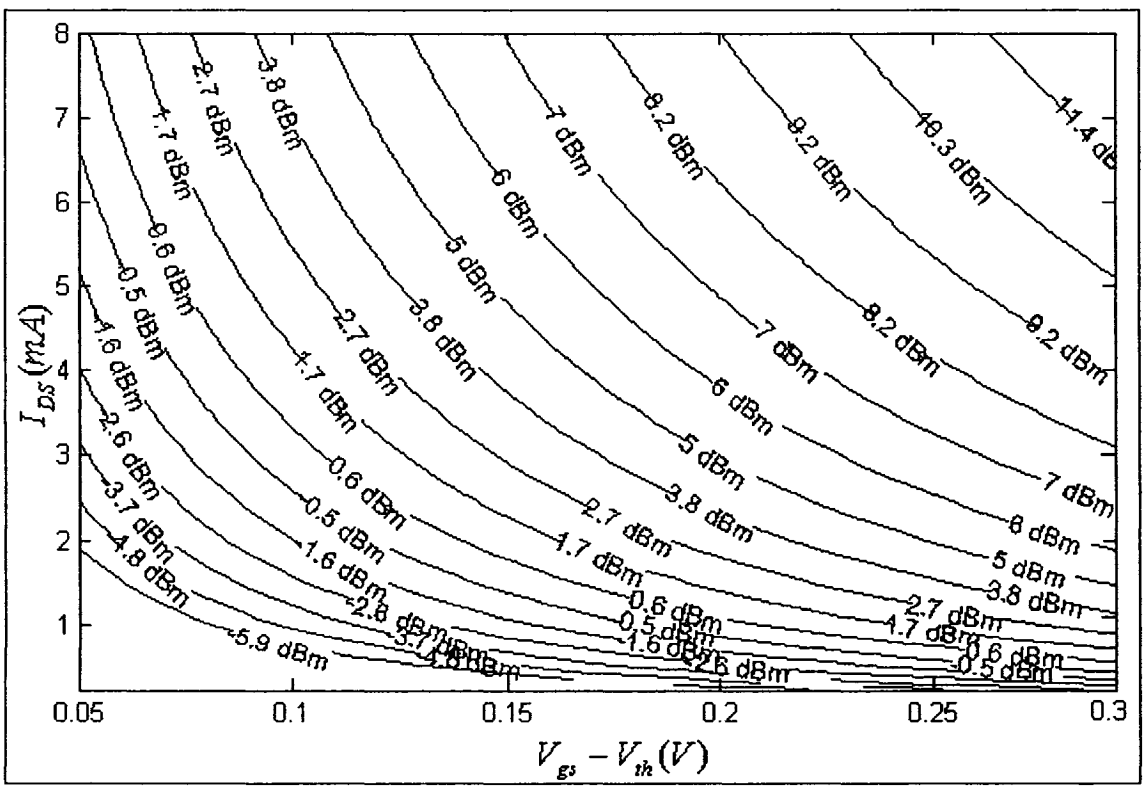

Figure 3-11: contour plots of IIP3.

is given by:

$$IIP3 \cong -12 + 20\log\left(w_o C_{gs}\sqrt{50R_S}\right) \tag{3.51}$$

It is clear from (3.51) that IIP3 becomes a function of the transistor width (or C_{gs}). Short channel NMOS devices exhibit an acceptable transconductance when biased in near saturation region (triode), yet a large C_{gs} is associated with low input quality factor and thus a low PCC. To overcome this obstacle, the design presented in the next chapter will employ the built in parasitic BJT transistor to boost the effective transconductance thus, enabling a combination of very low overdrive voltage and drain current, while maintaining a good power gain. Finally, if the target IIP3 cannot be met within the allowable power budget the designer must use circuits that cancel the effect of the signal third harmonics. An example of such circuits is presented in figure 1-2 (b). Another proven solution could be a BJT transistor in parallel with the MOSFET one, more about this architecture will be covered in chapter four.

3.3.4 - The design of the cascode device

Optimizing the design of the cascode device will help reducing the LNA overall noise, as well as, improving the power gain of the LNA. An ideal cascode device design should maximize its pole w_c and improve the shielding of the device, or reduce the Miller effect M. Improving w_c suggests minimizing the size of the transistor which increases M. Although looks difficult to reach a solution that optimize both factors simultaneously, a good compromise is always possible.

The expression of the cascode pole is given by [8]:

$$w_c = \frac{g_{m.c}}{\alpha\left(\left(\alpha_{db} + \alpha_{gd}\right)C_{gs} + \left(1 + \alpha_{sb}\right)C_{gs.c}\right)} \tag{3.52}$$

where $g_{m.c}$ and $C_{gs.c}$ are the cascode device poles and gate to source capacitances, respectively, and α_{xy} is technology dependent ratio given by:

$$\alpha_{xy} = \frac{C_{xy}}{C_{gs}} \tag{3.53}$$

It is clear from (3.52) that w_c is proportional to $g_{m.c}$, which is also proportional to the square root of *W/L*, or the square root of $C_{gs.c}$. For a given amplifier device w_c can be maximized when:

$$w_{c\_opt} = \frac{w_T}{2\alpha\sqrt{1 + \alpha_{sb}}\sqrt{\alpha_{db} + \alpha gd}} \tag{3.54}$$

which is equivalent to:

$$C_{gs.c\_opt} = \frac{\alpha_{db} + \alpha_{gd}}{1 + \alpha_{sb}} C_{gs} \tag{3.55}$$

and

$$M_{opt} = \alpha\sqrt{\frac{1 + \alpha_{sb}}{\alpha_{db} + \alpha_{gd}}} \tag{3.56}$$

Equation (3.54) suggests that $C_{gs.c\_opt} \approx 0.5C_{gs}$ for short channel devices and this will increase M and deteriorate overall LNA NF although, it improves w_c and reduces the contribution of the cascode device noise. A smaller cascode device will decrease PCC and increases M, on the other hand, decreasing M will require a larger cascode device ($C_{gs.c\_opt} \approx 2C_{gs}$) and this will increase the output capacitance given by:

$$C_L = C_{L.fixed} + \frac{\alpha^2}{M^2}(\alpha_{gd} + \alpha_{db})C_{gs} \tag{3.57}$$

and consequently, it will lower the achievable output resistance given by:

$$R_P = \frac{Q_{Ld}}{w_o C_L} \tag{3.58}$$

Non-ideal Effects in the Cascode Stage: To conclude the discussion about cascode transistor design, one important precaution should be highlighted when connecting the gate of the cascode device to external bias. The bond-wire used in the connection will act as an inductor and enter in a series resonance with $C_{gd.c}$ of the cascode device at a multiple of w_o and this will pull the power gain down to zero dB. The series resonance can be removed by shunting the transistor gate to ground using a large decoupling

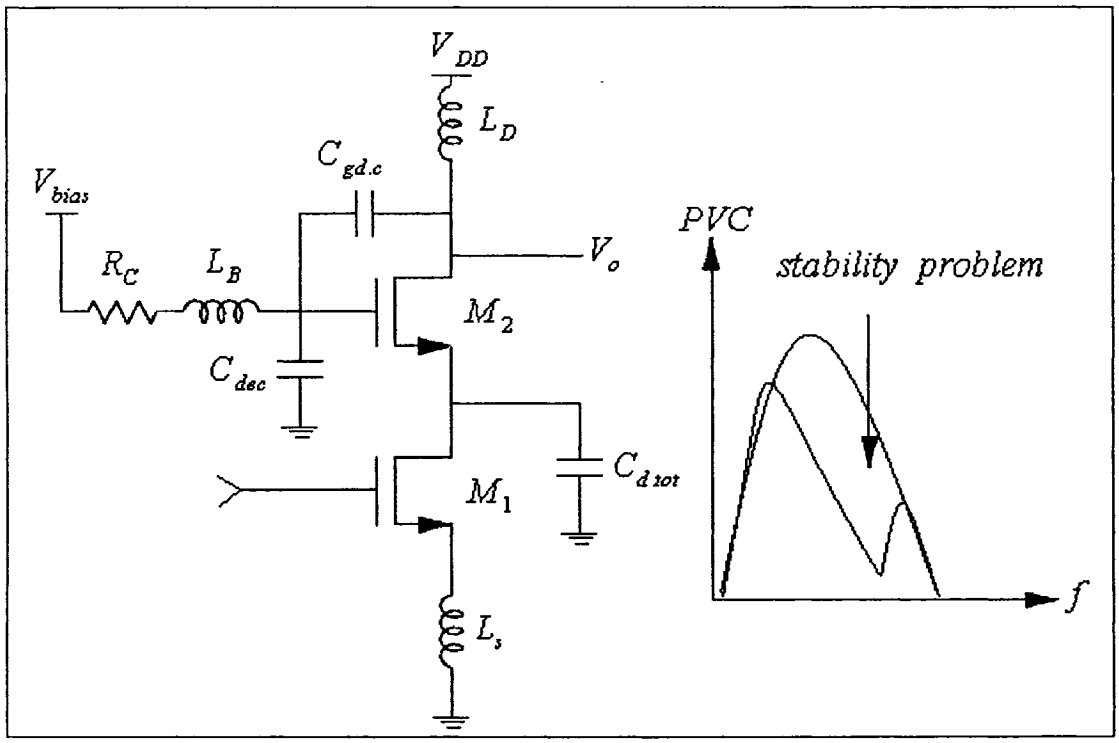

Figure 3-12: coscode transistor side effect troubleshooting

capacitor. Also, the cascode device will suffer from instability problem due to the capacitive degeneration seen by its source. Adding a resistor in series with the cascode device, as shown in figure 3-12, will kill the negative resistance due to this capacitive degeneration and help stabilizing the transistor.

3.4 – Conclusion

The design and optimization guidelines of a CMOS LNA have been presented in this chapter. Using contour plots, this chapter provides a way that enables the designer to meet the design specification within a specific power budget. Indirect matching was also presented, it helps achieve better power gain especial when the LNA is intended to be packaged. The next chapter will present a novel CMOS LNA based on the theory and discussion presented in chapters two and three.

Chapter 4 – Low Voltage 5 GHz LNA Implementation

4.1 - Introduction

The equations derived in chapter 3 show the difficulty of designing a very low voltage cascode LNA with a good performance. Operating the cascode LNA from a V_{DD} of 0.85 volts will result in a poor effective transconductance performance, which is required to have good power gain and low noise figure. The only solution to overcome this obstacle is by adopting a technique to boost the poor $g_{m.eff}$ of the input NMOS amplifier. This chapter will present a novel design that uses the built-in parasitic BJT transistor to boost $g_{m.eff}$ of the LNA and help achieving the rest of the LNA specification. The implementation of both the schematic and RF layout of the LNA chip will be covered in detail.

4.2 - Parasitic BJT in the MOS

Consider the cross section of the NMOS device built inside the P-well enclosed into an N-well as seen in figure 4-1 below. The parasitic BJT seen in this figure is considered by analog and digital designers as a problematic device and they avoid turning it on (cause latch up). For them, this BJT will bypass the CMOS circuit and result into circuit failure. As a matter of fact, this design exploits the existing parasitic BJT device in a way that enables the RF designer to build a very low voltage cascode LNA that delivers very good

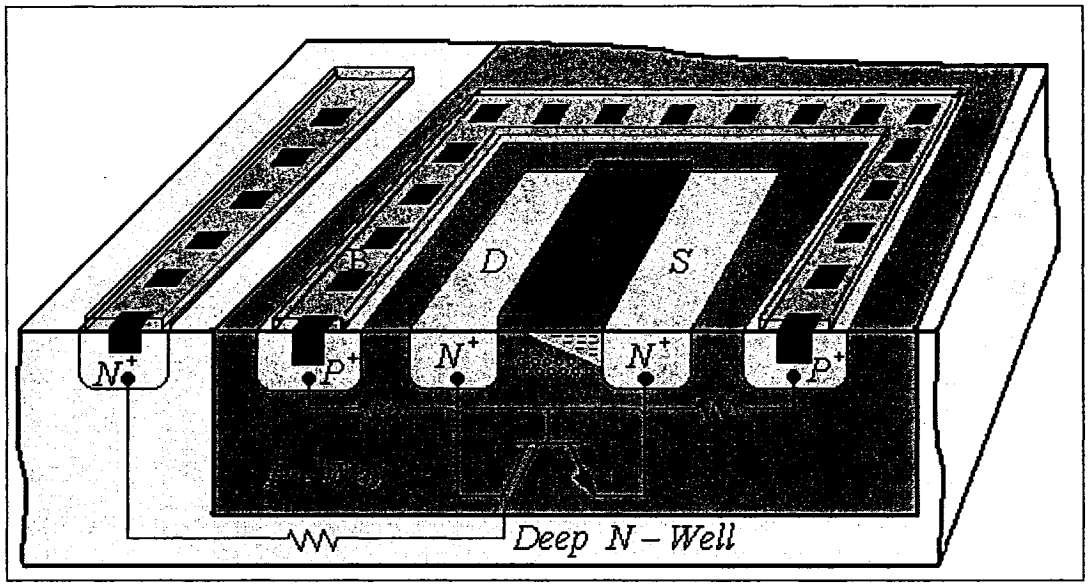

Figure 4-1: MOS cross section showing the parasitic BJT

power gain, while maintaining a good noise and linearity performance.

One can turn on this BJT transistor by applying a voltage higher than 0.7 volts to the bulk of the P-well (control voltage), which is at the same time the base of the BJT. This will reduces the threshold voltage of the NMOS device given by:

$$V_{th} = V_{to} + \gamma\left(\sqrt{|2\Phi - V_{BS}|} - \sqrt{|2\Phi|}\right) \tag{4.1}$$

The direct result of lowering the threshold is an increase in the cutoff frequency f_t of the NMOS. This increase helps enhancing the performance of the device (NF and PCC), specially when operating in low voltage mode. The MOS operated in this fashion can be considered as a composite of PNP and NMOS transistors. It will be referred to as a NMOS-PNP device.

The new small signal model of the **NMOS-PNP** device is shown in figure 4-2, Note that $C_{bs} = C_{\pi}$ where C_{bs} and C_{π} are the bulk to source and base to emitter junction capacitors respectively.

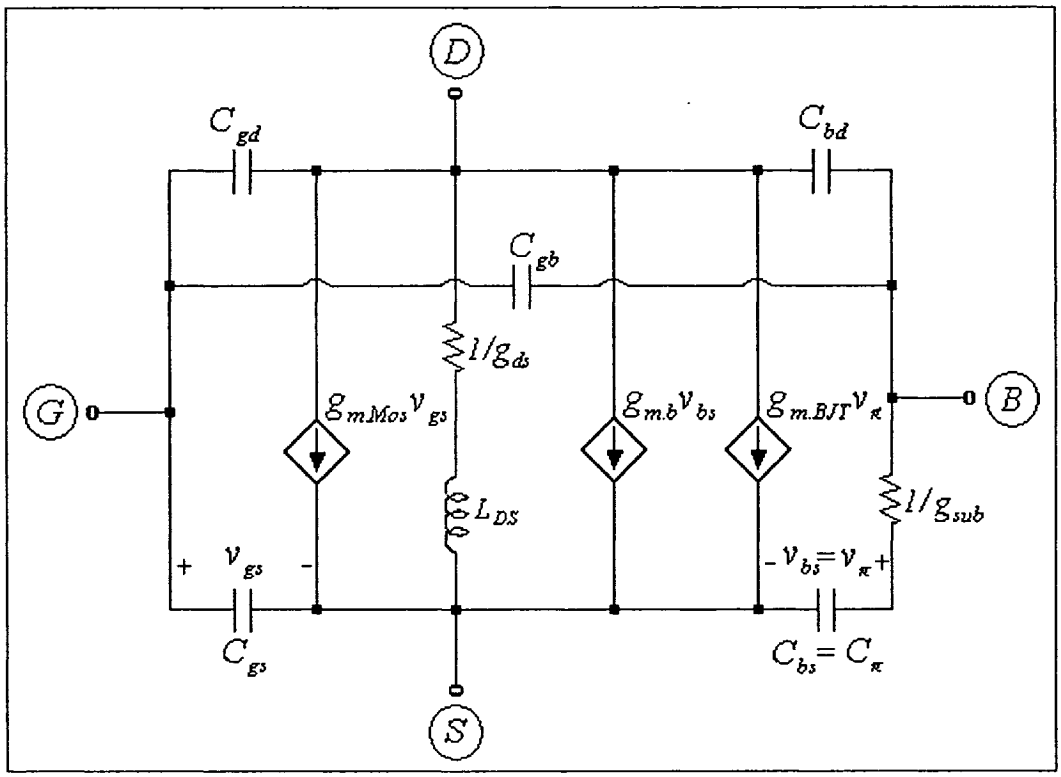

Figure 4-2: The new NMOS-PNP transistor small signal model

The **NMOS-PNP** device will replace the conventional NMOS one, in building the proposed novel low voltage LNA, as seen in figure 4-3 below. The new value of $g_{m.eff}$ already given by (3.26) becomes:

$$\left|g_{m.eff}\right| = \frac{i_{out}}{v_s} \cong \frac{g_{m.MOS}v_{gs} + g_{m.BJT}v_{bs}}{2i_{in}R_S} = \frac{g_{m.MOS}\dfrac{i_{in}}{sC_{gs}} + g_{m.BJT}\dfrac{i_{BB}}{sC_{BS}}}{2R_S i_{in}} \tag{4.2}$$

where i_{BB} is the BJT base current and is given by:

$$i_{BB} = \kappa g_{m.MOS}v_{gs} = \kappa\frac{g_{m.MOS}i_{in}}{sC_{gs}} = w_{T.MOS}\frac{g_{sub}}{(g_{sub}+g_{ds})}\frac{i_{in}}{s} \tag{4.3}$$

The factor κ represents the ratio of NMOS drain current that flows through the BJT base. This factor is highly dependent on the layout geometry of the device and the distance between the bulk contact and the device, or in other words, how wide is the base of the

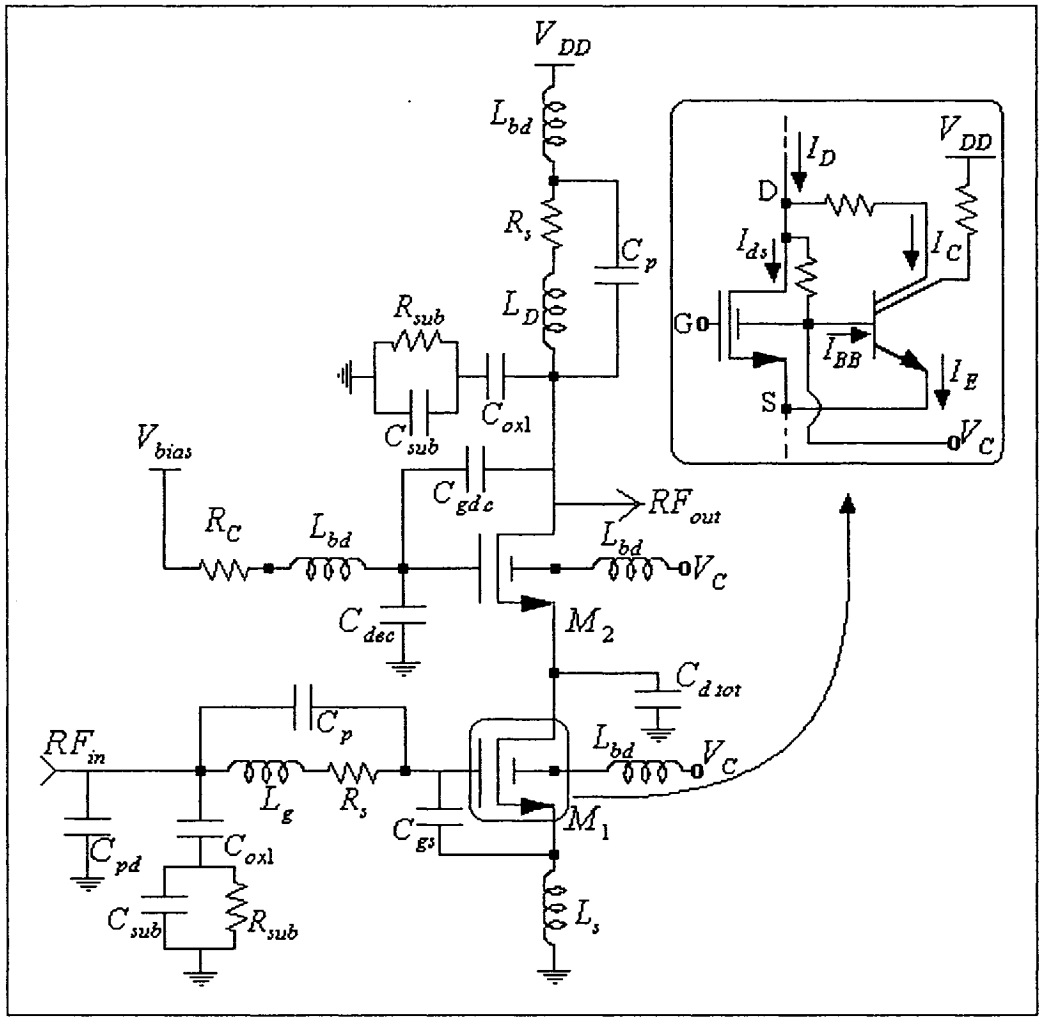

Figure 4-3: The proposed cascode LNA circuit and its parasitic

parasitic BJT. Also, $g_{m.MOS}$ and $w_{T.MOS}$, represent the transconductance and cutoff frequency of the NMOS device, respectively. Similarly, $g_{m.BJT}$ and $w_{T.BJT}$, represent the trans-conductance and cutoff frequency of the parasitic BJT. Equation (4.2) becomes:

$$\left|g_{meff}\right| = \frac{w_{T.MOS}}{2w_o R_s} + \frac{\kappa w_{T.MOS} w_{T.BJT}}{2w_o^2 R_s} = \overbrace{\frac{w_{T.MOS}}{2w_o R_s}}^{g_{m1}}\left(1 + \overbrace{\frac{\kappa w_{T.BJT}}{w_o}}^{g_{m2}}\right) \tag{4.4}$$

In (4.2) it was assumed that the SAW filter is power matched and hence, $v_s = 2R_s i_{in}$. The cut-off frequency of the BJT is given by [46]:

$$w_{T.BJT} \cong \frac{g_{m.BJT}}{C_{\pi}} \tag{4.5}$$

Equation (4.4) clearly shows that the initial MOS effective transconductance (g_{m1}) was boosted by a factor equal to $g_{m1}xg_{m2}$ and this factor is highly dependent on device layout. Dividing the NMOS into islands and surrounding these islands with bulk contacts, will greatly improve the effective transconductance of the parasitic BJT, since it reduces the width of its average base. Yet, it was found that by doing this, the linearity of the resulted device dropped slightly.

The matching conditions already given by (3.3)-(3.5) becomes:

$$v_{in} = sL_g i_{in} + \frac{i_{in}}{sC_{gs}} + sL_s i_{in} + sL_s\left(i_{in} + g_{m.MOS}v_{gs} + g_{m.BJT}v_{BS}\right) \tag{4.6}$$

$$v_{in} = sL_g i_{in} + \frac{i_{in}}{sC_{gs}} + sL_s i_{in} + sL_s\left(i_{in} + g_{m.MOS}\frac{i_{in}}{sC_{gs}} + g_{m.BJT}\frac{g_{m.MOS}i_{in}}{s^2 C_{BS}C_{gs}}\right) \tag{4.7}$$

$$Z_{in} = j\left[w\left(L_g + L_s\right) - \frac{C_{BS} + L_s g_{m.MOS}g_{m.BJT}}{wC_{gs}C_{BS}}\right] + w_{T.MOS}L_s \tag{4.8}$$

The matching condition holds for:

$$L_s = \frac{50}{w_{T.MOS}} \tag{4.9}$$

The above equations shows that the new **NMOS-PNP** device not only increase the conventional NMOS effective transconductancen and its power gain, but also offers interesting features such as gain tunability and good linearity.

Gain tunabilty: Gain tunability is an important design feature in modern LNAs. At high input power levels, reducing the gain will enhance the linearity of the LNA and relax the dynamic range and linearity of the other blocks in the receiver. This feature should come

at no cost in terms of noise figure or linearity. Gain control is another advantage offered by the novel design and could be appreciated through inspection of equations (4.4-9). The input network match slightly depends on the transconductance of the parasitic BJT and this will enable the designer to control the power gain of the LNA without degrading the noise figure and linearity of the LNA. When the bulk voltage (BJT base terminal) drops below 0.7V, the BJT will turn off, resulting in drop of $g_{m.eff}$ and forcing the gain down. The noise figure and linearity of the LNA remain almost constant since v_{gs} remains constant. The gain drops gradually until V_C=0.7V and remains almost constant after that (see simulation results below). Finally, the center frequency of the LNA and its bandwidth will be slightly affected by changing the bulk voltage, since the matching condition given by (3.8) partially depends on $g_{m\cdot BJT}$, this change is usually tolerated.

LNA linearity: Using the BJT transistor in parallel with NMOS one will greatly improve the overall linearity of the BJT-MOS device. With appropriate bias, the BJT and NMOS have almost the same third harmonic current signal but with opposite sign. When added together the resulted third harmonic current signal is almost zero. The technique is illustrated in figure (4-4) below, the target third harmonic component (g_3) cancelled.

4.3 – LNA chip layout

High speed analog layout techniques encompass each and every corner of the silicon mask layout including, I/O pads, chip interconnect, RF transistor design, matching techniques, bulk grounding, active devices isolation, passive components design and optimization. That is why RFIC designer consider the layout task as fifty percent of the chip design task.

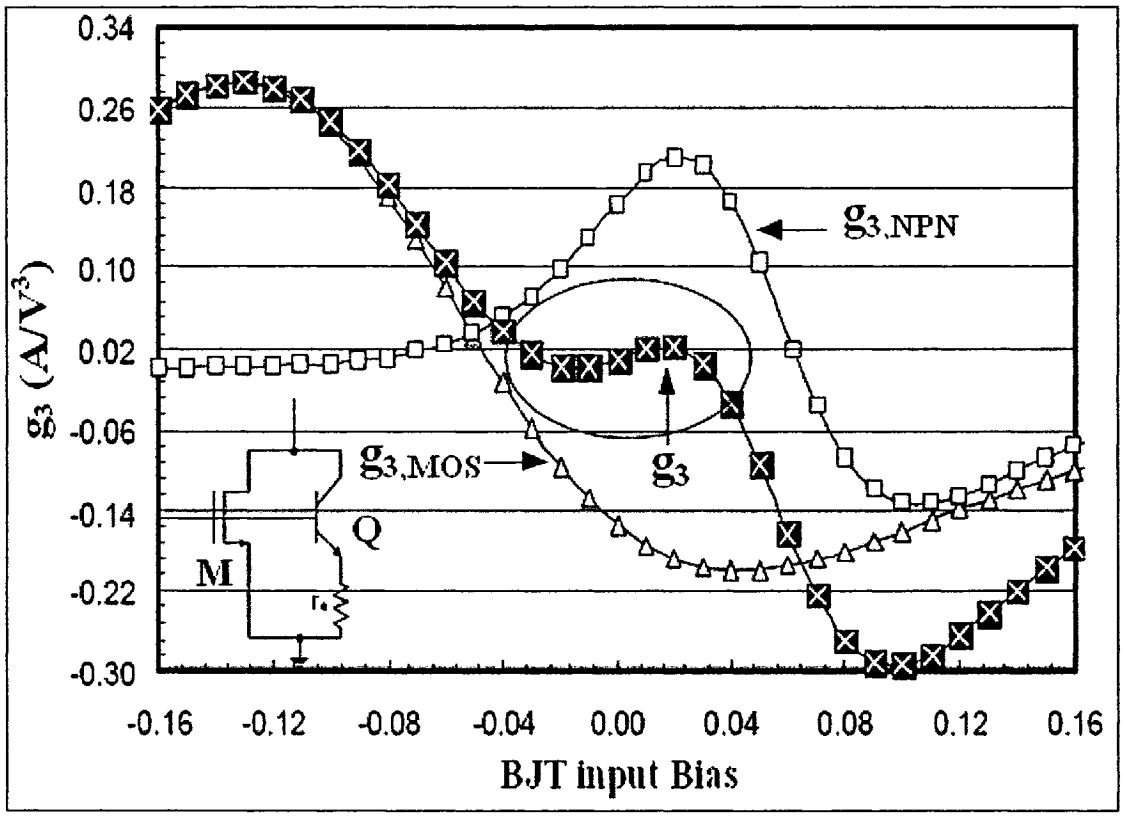

Figure 4-4: Third-order signal harmonic cancellation

4.3.1 - RF I/O pads design

The design of I/O RF pads plays an important role for matching, RF signal leakage and noise performance. A proper modeling of I/O RF pads is also important. First of all, only the top metal is used to build the I/O pads (i.e. metal six for 0.18 μm process technology) in order to reduce the capacitive coupling with the silicon substrate. Reducing the capacitive coupling with the silicon substrate is also achieved by reducing the area of the pads (using a nearly round Manhattan shape). Using nearly round RF I/O pads reduce the area or the coupling capacitance by a factor of up to 35%. This is essential for designers

using the RF input pad for matching purposes at high frequencies, where achieving a fifty ohm input impedance is limited by the parasitic capacitance of the RF input pad. This fact was illustrated in figure 3-7 of the previous chapter where a 100 fF is needed for indirect matching the 50 ohm source at 5 GHz. This pad could be achieved using a nearly round, metal six, pad with diameter of about 70 microns in 0.18 μm process technology, while it is almost difficult to build such a practical, bondable, low capacitance pad using a square shape pad. A small RF I/O pad will also reduce RF signal leakage and this will improve the port-to-port isolation by reducing the signal coupling and improve the power gain and noise performance of the LNA [14]. To improve the power gain and noise performance of the LNA, the I/O pads must be shielded from substrate capacitive coupling by using metal one grounded shield. To figure out how shielding will do all that let us take a look at the RF I/O pads before and after shielding as seen in figure 4-5 below. When the RF pad is not shielded (figure 5-4.a), the signal is coupled with noisy R_{sub} through C_{pad} and this will deteriorate the noise performance of the amplifier. A metal one shield will eliminate both R_{sub} and C_{sub} and as result will eliminate the noise generated when pad was coupled with R_{sub}. It also improves port-to-port isolation specially when the RF input and output pads are not far enough.

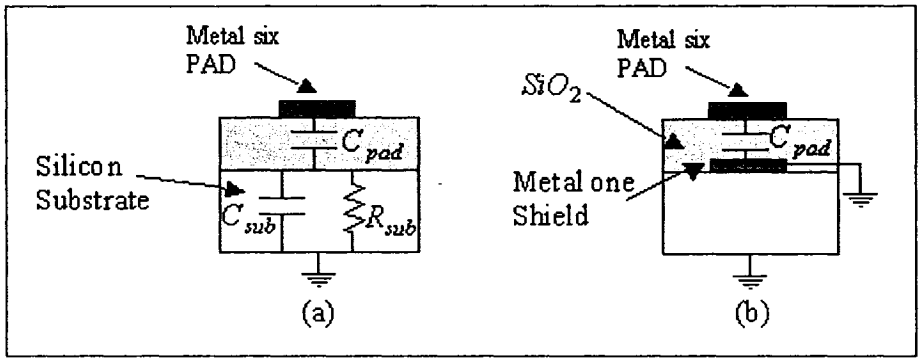

Figure 4-5: Effects of RF pad shielding

4.3.2 - RF MOS transistor layout

The design of the RF transistors start with sizing the NMOS, in order to reduce the area of the inductor L_g large interdigitated RF transistor is used (W = 200 microns). This large transistor need a careful layout, first of all the length of the unit finger width has to be chosen based on optimizing f_t and reducing the sheet resistance of the polysilicon gate (optimizing the noise figure). To reduce the sheet resistance of the polysilicon gate the width of the unite finger should be very short, yet a very short unit gate will degrade f_t. Figure (4-6) below shows that to optimize both the noise figure and f_t the unit finger width of the RF should be around three microns. In TSMC documents provided by CMC, the width of the unit gate finger is chosen to be 2.5 microns and we choose the same width in this work. Isolation of the RF transistor is another issue, the NMOS device has to be isolated from the surrounding noisy silicon substrate by using large straps of a well grounded guard rings (better to use both N and P-type guard rings around the RF transistors). Enclosing the NMOS device into a P-well built inside the N-well, will also provides a good isolation. To reduce the substrate resistance, the interdigitated NMOS device has to be divided into several islands and each one surrounded with a very close ring of AC grounded substrate contacts as shown in figure (4-7). In order to reduce the

sheet resistance of the fingered gate, the later has to be shorted from both ends as shown in figure (4-7). Finally, the interconnects of the NMOS devices, as well as all chip interconnects, have to be wide enough (10-15 microns) with no sharp angles, to avoid serial parasitic resistances and signal reflection along the path of the AC signal. At high frequencies it is helpful to map the substrate and the AC interconnect into an electromagnetic simulator and extract the interconnect parasitic, as well as, to visualize the areas of current crowding and try to fix it.

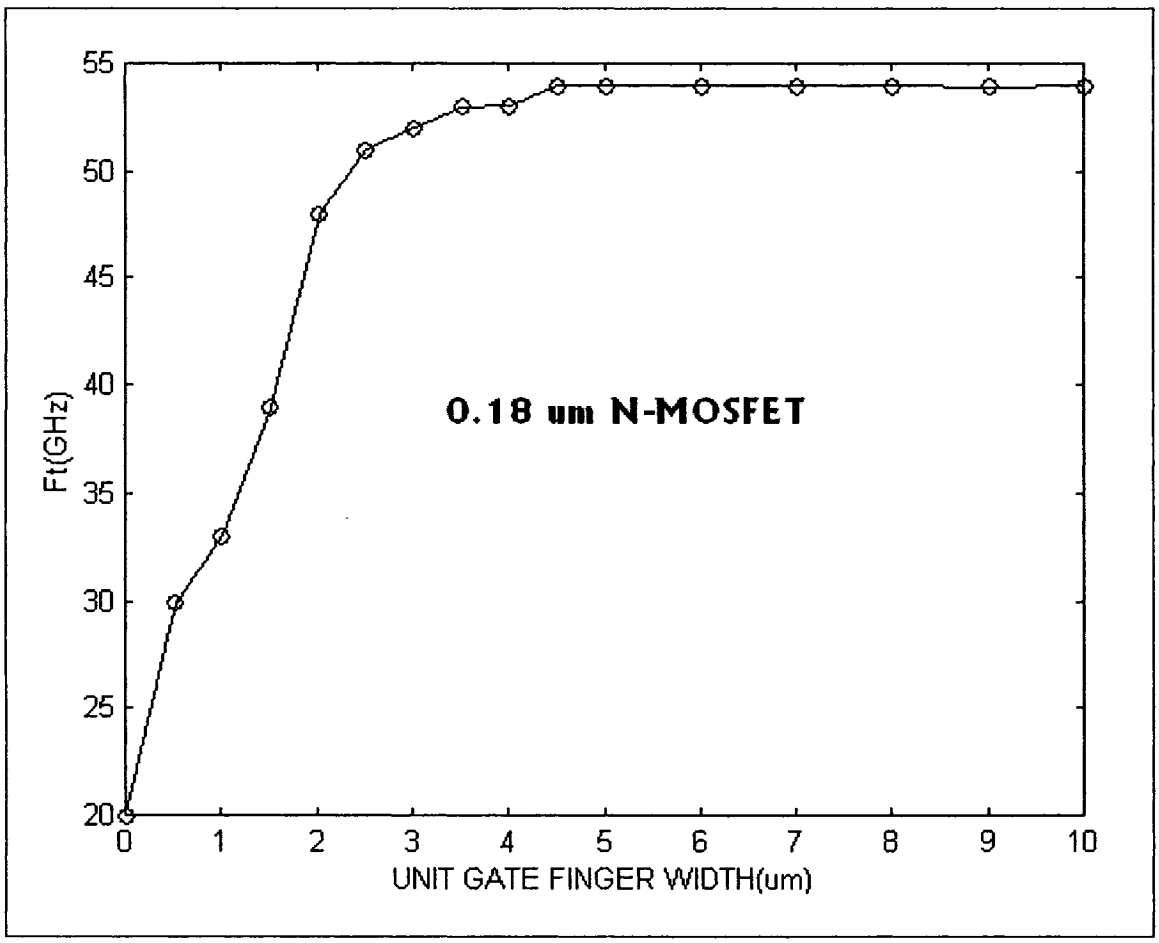

Figure 4-6: Transistor f_t Vs its unit gate length

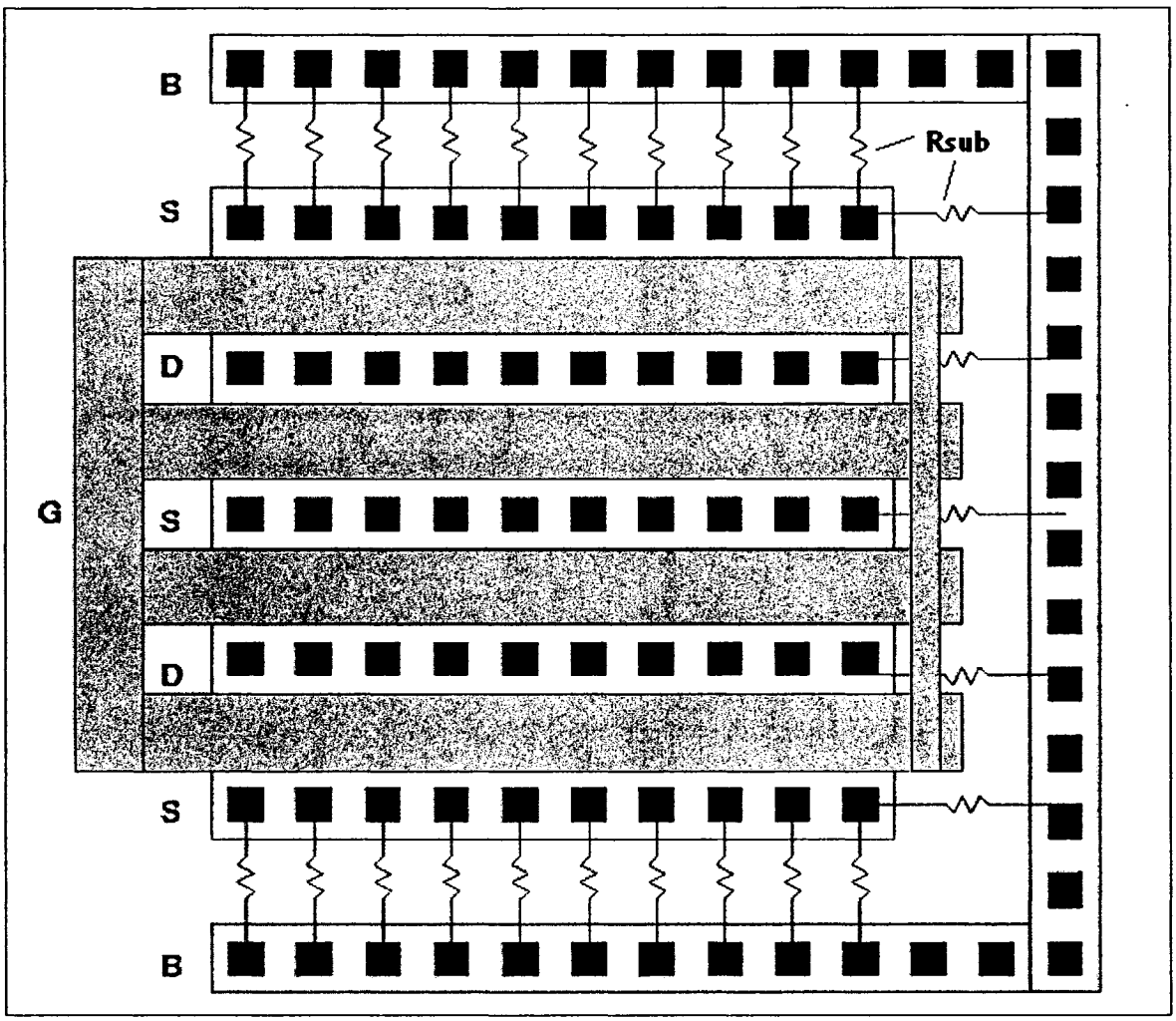

Figure 4-7: RF transistor layout

4.3.3 – Inductors design and layout

An important parameter to consider when designing on-chip inductors is quality factor given as:

$$Q = 2\pi \frac{E_{store}}{E_{diss}} \approx \frac{X_{in}}{R_{in}} = \frac{2\pi fL}{R} \qquad (4.10)$$

Where E_{store} and E_{diss} are respectively the energy stored and dissipated in inductor and R is the inductor's sheet resistance. To improve the quality factor of the inductor one has to increase the energy stored by adopting the appropriate geometry and reducing the sheet resistance. Round planar inductors gives the best quality factors, to optimize E_{store} the

radius of the inductor should be carefully simulated using Electro-magnetic simulator such as HP-ADS™. The spacing between two inductors segments should be considered carefully too. To reduce the sheet resistance for inductors built in 0.18 μm technology, the thick top layer (metal six) should be used. Increasing the inductor's width helps also reducing the sheet resistance but it lowers its resonant frequency. At 5 GHz frequency, the optimum width is around 18 microns. To increase the inductor's isolation, one may build the inductors on top of a deep Nwell.

Finally, at 5 GHz, the inductors should be placed at least 45 microns away from each other and from the chip edges so they don't magnetically couple with each other through the substrate.

4.4 – Post layout simulation results

The post-layout simulation results of the LNA shown in figure (4-3) is presented below. At 5 GHz, the LNA delivered 16 dB of power gain (S21) with Input (S11) and output (S22) signal reflection of -19dB and -15db respectively. These results are shown in figure 4-8 below. Operated from a V_{DD} = 0.85 volts and drawing 4 mA DC current, the LNA performed an excellent linearity of IIP3 = 4 dBm as shown in figure 4-9 and 7 dB of gain tuneability as shown figure 4-10.

Finally, the novel circuit was compared to a classic cascode LNA topology and simulated under the same DC power and layout conditions and using the same 0.18 μm standard technology; it was clear that the novel circuit outperforms the classic cascode topology in terms of gain, linearity and noise figure (see table 4-1 below). The gain tenability feature provided with the new BJT-CMOS transistor does not exist in the classical cascode LNA.

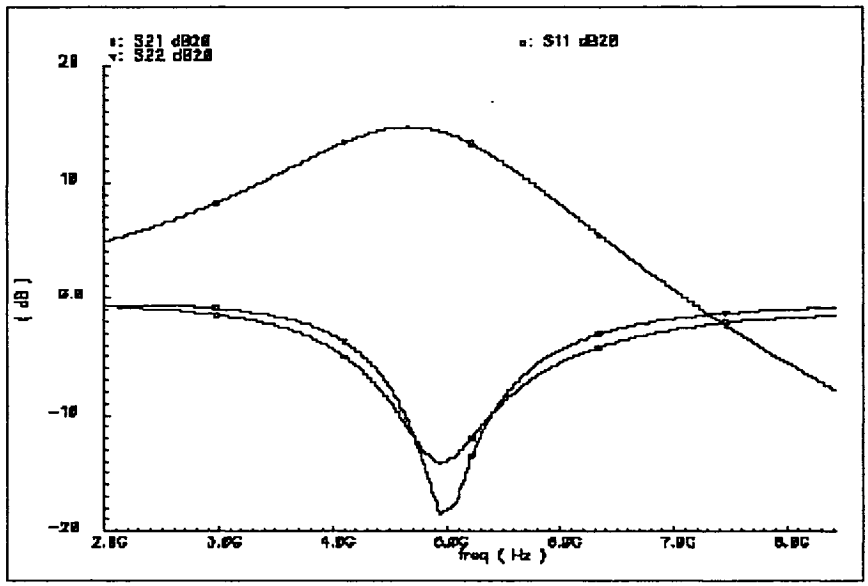

Figure 4-8: LNA power gain and I/O signal reflection.

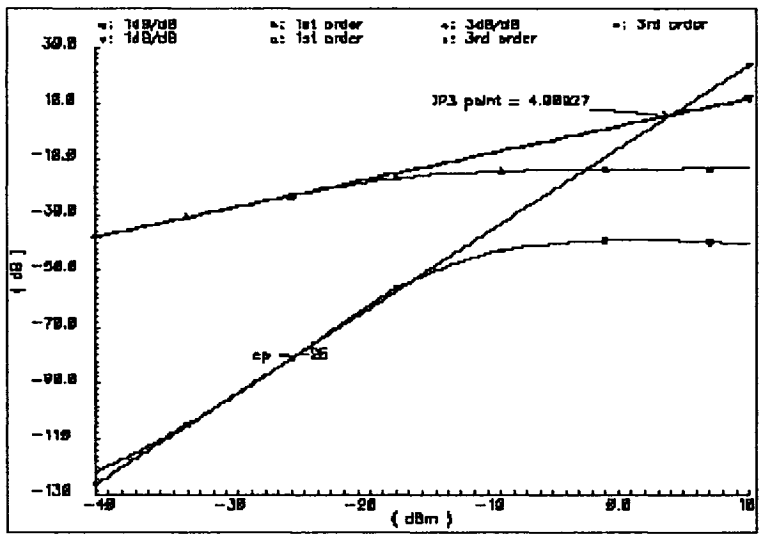

Figure 4-9: LNA linearity.

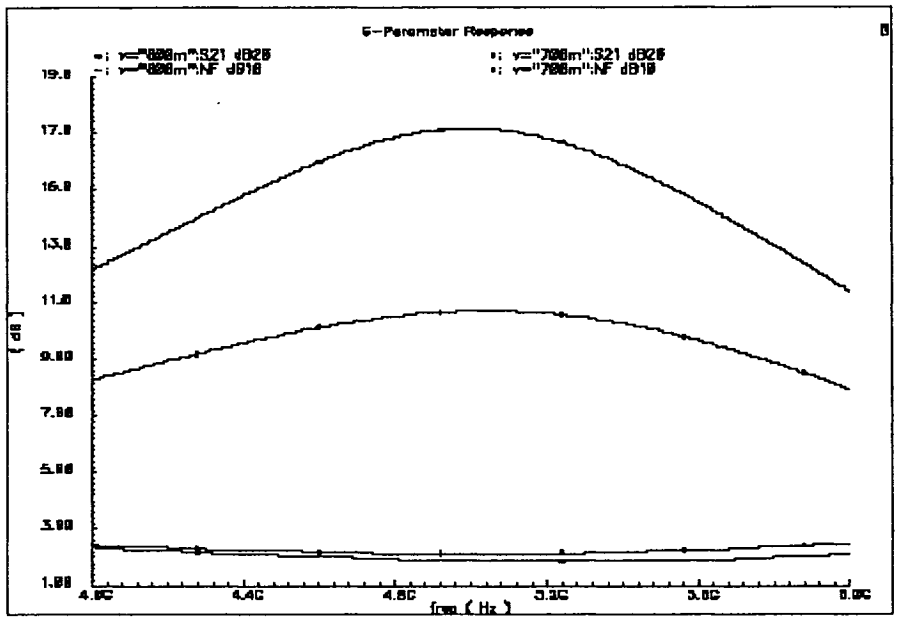

Figure 4-10: LNA gain tunability.

Table 4-1: Novel Cascode LNA performace versus Classic one

	Gain (dB)	IIP3 (dBm)	S11 (dB)	NF(dB)	Tunability
Novel LNA	16	4	-19	1.8	7 (dB)
Classic Cascode	9	-8	-15	2.1	0

4.5 – Conclusion

The design, implementation and Post Layout Simulation results of a low voltage novel LNA design were presented in this chapter. Radio frequency integrated circuit Layout techniques has been presented in this chapter. The final chapter of the thesis will present the measured results of the fabricated cascode LNA shown in figure 3-12 (with VDD = 1.5 volts) as part of this work.

Chapter 5 – LNA Measurement Results

Introduction

This chapter presents the experimental results of a 5 GHz cascade LNA. Test fixtures, techniques and equipment used will be presented in section one of this chapter. Section two will cite the contribution of this work. Section three provides the conclusion.

5.1 – Test setup and results

The LNA loose die was glued (using conductive clue) and bonded to a Roger 4000 series RF board material that operate up to frequencies of 10 GHz. The test fixture is shown in figure 4-1 below. The RF board was designed to enable both direct wafer probing as well as applying the RF signal through SMA connector. The RF signal were applied (and probed) directly to the die's input RF pad by using two GGB Industries Inc. microwaves Pico probes and indirectly through SMAs. The 8720ES Agilent vector network analyzer (VNA) was used to perform the measurement.

Standard calibration procedures were performed (Short – Open – Load – Through) resulted in a small attenuation of -0.85 dB over the VNA cables. The resulting measurement is listed versus the expected simulated values in table 4-1 as well as versus other reported LNA results in table 5-2. A 9.3 dB difference in power gain occurs mainly due to output mismatch (S22). The output matching network of the LNA was corrupted

by the addition of the extra series capacitance of the VNA's built in Bias Tee as shown in figure 4-2 below.

Table 5-1: measured versus simulated LNA results

	S21	S11	S22	IIP3	NF	VDD
Measured @ 5 GHz	5.3	-10.7	-3.6	-4	1.8	1.5
Simulated @ 5GHz	14.8	-21	-11.5	-3	1.4	1.5
difference	-9.5	-10.3	-8.1	-1	-0.4	-

Table 5-2: Comparison of this work versus other reported LNA

REF	OPTIMIZATION	NF (DB)	GAIN (DB)	IIP3 (DBM)	V_{DD} / POWER (V / mW)	F_0 (GHZ)	TECH. (μm)	YEAR
[8]	NF	1.4/2.1*	17	na	/9	5.2	0.25	2001
[9]		0.8	20	-11	9	1.23	0.25	2002
[12]		0.9	8.8	7.1	7.5	0.8	0.24	2002
[14]		1.8	8.9	8.4	6.9	7	0.25	2002
[16]		0.85/1.2	13	-1.5	17.6/5	0.92	0.35	2001
[25]		2.5	16	na	16	5	0.25	2000
[17]	IIP3	3.1	15.6	13.9	na	2.4	0.25	2003
[17]		3	14.9	16.1	na	2.2	0.25	2003
[18]		2.8	5	18	45	0.9	0.35	2001
[11]	Low Voltage	0.9	14.2	0.9	1/16	5.75	0.18	2003
[7]		3.5	22	-9.3	1.5/15	1.5	0.6	1997
[21]		2.5	13.2	na	1/22.2	5.8	0.18	2002
[22]		3.2	7.2	6.7	1.3/20	5.8	0.35	2002
[35]		4.8	18	-7	1/32	2.4	0.35	2001
This work		1.8	5.3	-4	1.5/11	5	0.18	2004

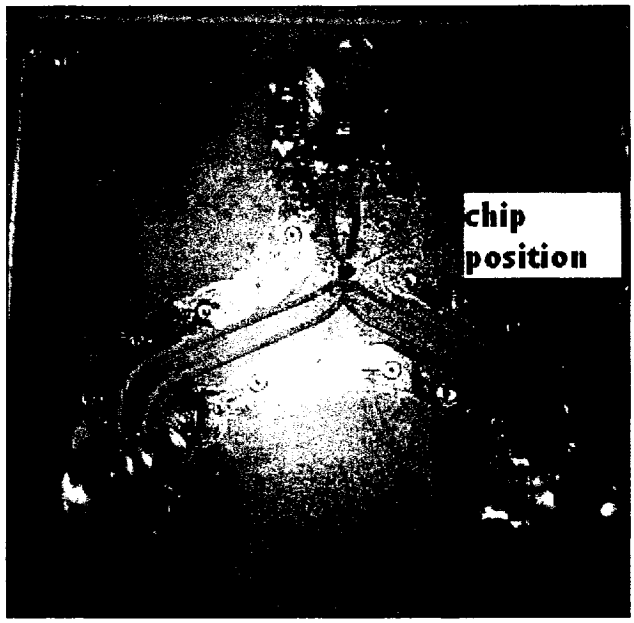

Figure 5-1: LNA test setup.

The measured input/output signal reflection shows a significant shift from the 5 GHz target center frequency at both input and output. The shift at the input reflection (S11) could be tolerated since S11 < -10 dB which is not the case for the signal reflection at the output. In order to partially resonate-out the Bias Tee extra capacitance and reduce the signal reflection at the output, an off chip inductor is added in series with the Bias Capacitor. This inductor could be implemented by either a bonding wire or by using a matching stub. Finally, the measured Input/Output reflection is shown in figure 5-3, the power Gain (S21) in figure 5-4 and the chip layout in figure 5-5.

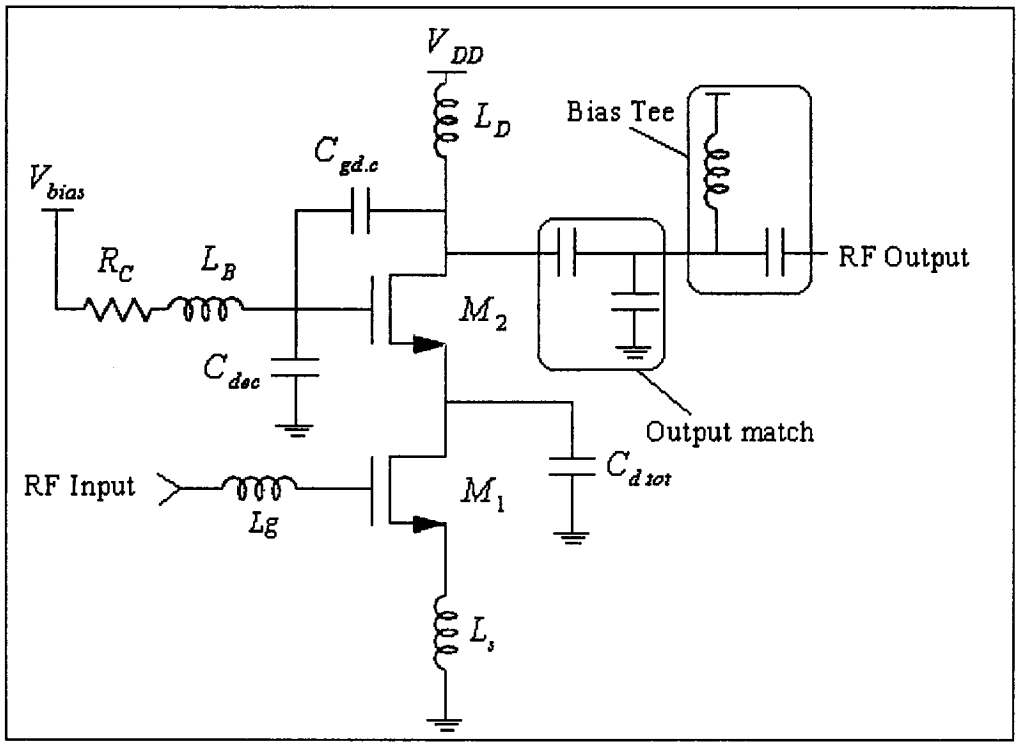

Figure 5-2: LNA schematic with Bias Tee circuit.

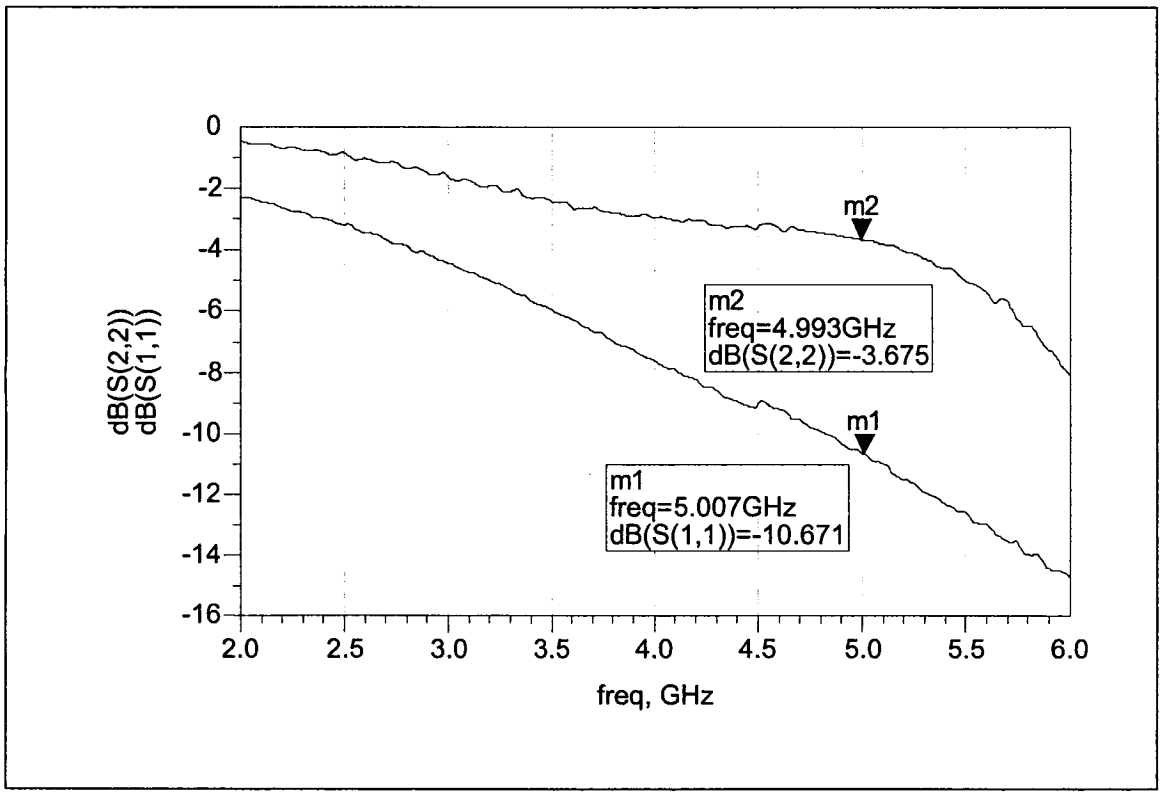

Figure 5-3: measured I/O signal reflection.

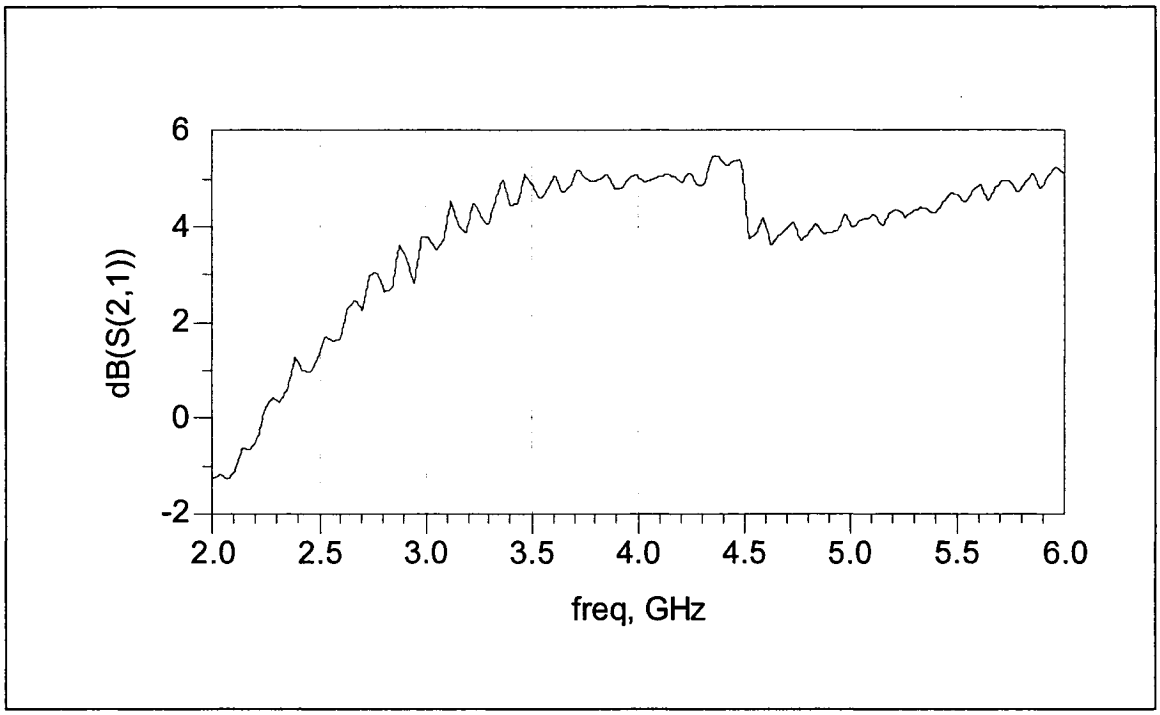

Figure 5-4: LNA measured power gain (S21)

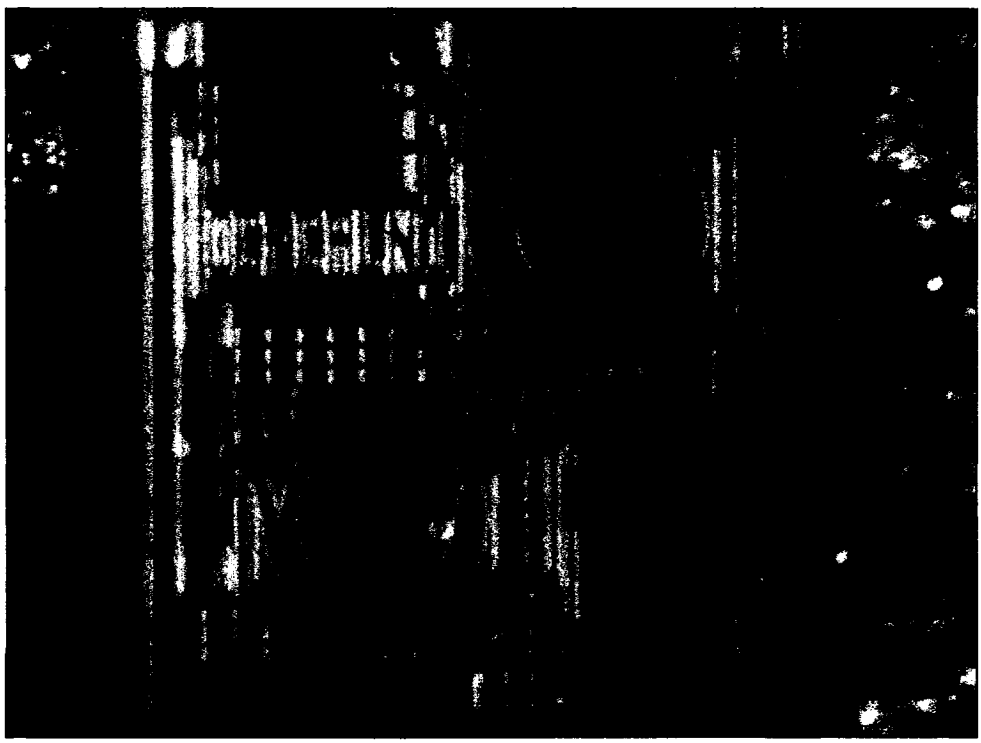

Figure 5-5: LNA die picture

5.2 – Thesis contributions

The following is a summary of the thesis contribution:

I. providing a state of the art of low voltage CMOS LNA designs, study their features and proposing a new low voltage LNA design. The novel design has three important features:

1- A new power gain boosting technique using the NMOS device parasitic BJT and boosting the LNA gain up to 60 percent.

2- Variable LNA gain control through varying the transconductance of the BJT transistor.

3- Improving the linearity of a low voltage LNA through cancellation of the third harmonic component of the current signal.

The proposed LNA design was published in the IEEE-NewCAS 2004:

G. Nohra, R. Raut, M. Sawan. "A 0.85 V TUNABLE GAIN 5 GHz CASCODE LOW NOISE AMPLIFIER" IEEE-NewCAS, Montreal, Canada, pp.353-356, 2004.

II. A CMOS LNA chip fabricated in 0.18 μm technology. The fabricated LNA didn't provide the expected simulated power gain due to the added Bias Tee capacitor in series with the output matching, yet this LNA should perform good gain once integrated in a true receiver where there is no such a series capacitance.

III. CMOS LNA design methodology (for 0.18 μm technology) based on graphical contour plots and developed equations for CMOS 0.18 μm technology parameters.

5.3 – Conclusion and future work

The measurement setup and results of the fabricate CMOS LNA have been presented in this chapter. The high measured output reflection caused by the series capacitor of the Bias Tee force a drop in the power gain. Finally, a list of the thesis contribution was presented in section two of this thesis.

The standard 0.18 μm CMOS technology was proven to be suitable for RFIC application. More research needs to be done in order to improve the performance of CMOS RFIC circuits especially LNA; LNA Linearity and noise figure are two key performances that could be improved.

Integrating the LNA into a CMOS receiver is another challenging and exiting project. New RFIC receiver architecture should be proposed with enhanced functionality and this project must involve novel LNA circuits. Also, packaging the RFIC receiver is another complicated task were modeling and extracting the bond wires and package parasitic is very important and could be used for indirect input/output matching.

Finally, wide band LNA is widely used in the industry today. CMOS wideband LNA could be the topic of a future work which involves new matching techniques as well as techniques to improve its noise performance.

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