Piecewise Nonlinear Approach to the Implementation of Nonlinear Current Transfer Functions

Chunyan Wang

Abstract — **A piecewise nonlinear approach to the nonlinear circuit design has been proposed in this paper. It is to approximate a target nonlinear transfer function by a particular combination of selected nonlinear pieces. The pieces can be produced by one or more analog blocks involving nonlinear devices. This approach can be applied to design nonlinear circuits to implement various current transfer functions. By controlling the operation modes of the transistor pair in a simple current mirror, one can modulate the current transfer function in a radical or fine-tuning manner. It is thus possible for the same current mirror to generate very different nonlinear pieces in different sections of its input range. In order that the control is done automatically by the input current, or in other words, the operation of the transistors is made to be input-current-dependent in a controlled manner, a series structure of two transistors has been proposed to be incorporated in the current mirror. The dependency can be made different by placing the structure in different places of the current mirror and/or by making the two transistors complementary or not, which makes the variations of the nonlinear function. Several current mirrors have been designed. Each of them consists of a very small number of transistors and performs a defined nonlinear current transfer function. The circuits have been simulated with HSPICE to validate the functions. The successful results have been obtained and are presented in the paper.**

Index Terms — **analog integrated circuits, current transfer functions, nonlinear circuit design, piecewise nonlinear approximation.**

Manuscript received on August 29, 2011, revised in April and July 2012.

The author is with the Center for Signal Processing and Communications, Department of Electrical and Computer Engineering, Concordia University, 1455 de Maisonneuve Blvd. West, Montréal, QC, H3G 1M8 Canada (e-mail: chunyan@ece.concordia.ca).

1. INTRODUCTION

Nonlinear circuits are widely applied in signal processing and communication systems, particularly for adaptive gain control, sensor conditioning, and bio-inspired computing. It is generally perceived that analog VLSI signal processing is most effective when the precision is not crucially required [9]. Implementing nonlinear functions in analog-mixed signal circuits will thus be promising and appealing, if the circuits can be made simple and easy to implement and if the drawback of poor accuracy is not critical in circuit operation or the errors can be corrected.

Research on nonlinear circuits has three fundamental topic areas, namely nonlinear circuit analysis, nonlinear circuit synthesis and nonlinear device modeling [2]. Talking about the design of nonlinear circuits, one would think of nonlinear circuit synthesis. More particularly, many synthesis methods are based on a piecewise linear approximation that has been studied and applied for decades [1][6][7]. The devices employed in the synthesis have been evolving over the period, but the principle remains valid and useful. Nevertheless, two facts in the technology evolution should be noted and can be explored. The first fact is that the devices used in integrated circuits are all nonlinear, not the mixture of linear and linearized ones. The second fact is that the research in the area of nonlinear device modeling and circuit simulation has been progressed enormously [8], facilitating the designs of both linear and nonlinear circuits. Hence, we propose a "piecewise nonlinear" approach to the nonlinear circuit design. It is to approximate a target nonlinear transfer function by a combination of nonlinear pieces. If these pieces can be generated easily with a small number of devices and then be merged smoothly, the piecewise nonlinear approach will make the nonlinear circuit design and implementation very cost-effective to achieve a good performance.

The work presented in this paper aims at designing circuits having nonlinear current transfer characteristics. This kind of circuits can be conveniently applied in adaptive biasing units, optical sensor systems, and current-mode circuits. The paper is organized as follows. In Section 2, the proposed piecewise nonlinear approach is presented. It describes the principle on which the design approach is based, the basic structures to be used for the modulation of nonlinear current transfer functions, and the possibility of using a single basic analog building block to produce multiple nonlinear pieces to form a well defined function. In Section 3, a good number of design examples are presented to demonstrate how the approach can be applied with variations to implement different nonlinear functions. The description of each of the design examples is immediately followed by the results of the simulation validating the function. The summary of the proposed approach and its applications in the nonlinear circuit design is found in Section 4.

2. PIECEWISE NONLINEAR APPROACH AND THE BASIC STRUCTURES FOR NONLINEAR CURRENT TRANSFER FUNCTIONS

The objective of the work presented in this paper is to develop analog circuits for nonlinear current transfer functions. The circuits should be as simple as possible, i.e., having a minimized number of basic units, with a view to minimizing the power dissipation and to facilitating their integration in electronic systems. To this end, as mentioned in Section 1, the proposed piecewise nonlinear approach is to approximate a target nonlinear transfer function by a combination of nonlinear pieces, instead of linear ones or linearized ones. A nonlinear piece can be produced by an analog building block involving nonlinear devices. In this aspect, one can have the following observations.

- A piece of nonlinear function can be approximated by a segment of another nonlinear function or by a number of segments of linear functions. In general, the approximation by the nonlinear segment produced by a single block is expected to result in a much simpler circuit implementation than that by the multiple linear segments.
- The characteristic of a nonlinear device does not have the same nonlinearity over its entire input range. For instance, the characteristic of a MOS transistor can be logarithmic or nearly-square-root, depending on the level of its voltage or current. In other words, the characteristic of such a device can be used to approximate, at one current level, a piece of logarithmic function, and also a square-root one when the current level is raised. Hence, it is possible to use one single block to generate two or even more pieces in different sections of its voltage or current range.

With the proposed piecewise nonlinear approach, one can minimize the number of the basic blocks to be employed by making good use of the device nonlinearity. In view of the targeted nonlinear current transfer functions, a current mirror can be considered as the basic building block producing nonlinear pieces.

A conventional current mirror performs a current scaling under its linear operation condition. Based on the principle of the piecewise linear approximation, one can use a combination of linear current mirrors to generate an arbitrary piecewise transfer function in order to synthesize nonlinear functions [13]. If current mirrors are used beyond the limit of the linear operation, they will be considered as nonlinear current mirrors and their current scaling factor will be input-current dependent. Incorporating a resistor in a linear current mirror can make a nonlinear current transfer to implement a gain control [5]. Nonlinear current mirrors can also be made resistor-free [3] [4]. Besides the prior knowledge about nonlinear current mirrors, there is a need to develop an effective method of modulating and segmenting nonlinear characteristics of current mirrors and those of the devices involved. In this work, the MOS current mirrors are used for the study of the nonlinearity of current mirrors.

The block diagram of a MOS current mirror is shown in Fig. 1. Each of the common-gate transistors, namely N_1 and N_2, can be made to operate in either saturation or triode mode, if they are under the condition of strong inversion. The current mirror can have four different states, as shown in Table 1, according to the operation modes of the two transistors. If both N_1 and N_2 operate in the saturation mode, the circuit will perform a linear scaling or linear transfer. In all the three other states, the scaling factor i_{OUT}/i_{IN}, or the derivative di_{OUT}/di_{IN}, is input-dependent, and each has a different dependency. Therefore, this current mirror is able to produce at least four very different pieces of current transfer characteristic in four different current ranges, respectively. It can be the case that two or more of these pieces are useful to form a nonlinear function. One can thus use a single current mirror to implement this function.

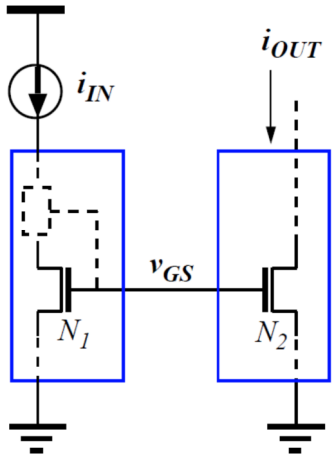

Fig. 1. Block diagram of a current mirror involving a NMOS transistor pair. The dashed lines are used to symbolically indicate connections that can be wires and/or devices [10].

Table 1 [10]

State	N_1	N_2	Function
1	saturation	saturation	linear scaling
2	triode	saturation	amplification
3	saturation	triode	compression
4	triode	triode	to be determined

It should be noted that, to perform a defined nonlinear function, when the level of the input i_{IN} is changing from one section to another in its range, the current mirror should be able to switch itself from one state to another according to the arrangement of the pieces of the function. To make it happen, the transistors should be able to switch themselves from one operation mode to

another in a “designed” manner. It is essential that they should be connected in such a way that the change of the operation mode is permitted. Fig. 2 illustrates three different configurations. The drain-gate short-circuit of the NMOS shown in Fig. 2(a) forces the transistor to operate only in the saturation mode. Contrarily, a series structure illustrated in Fig. 2(b) or 2(c) makes it possible for each of the two transistors to operate either in the saturation or triode mode, depending on their drain voltages with respect to their gate and base voltages. These structures can thus be useful in the design of nonlinear current mirrors.

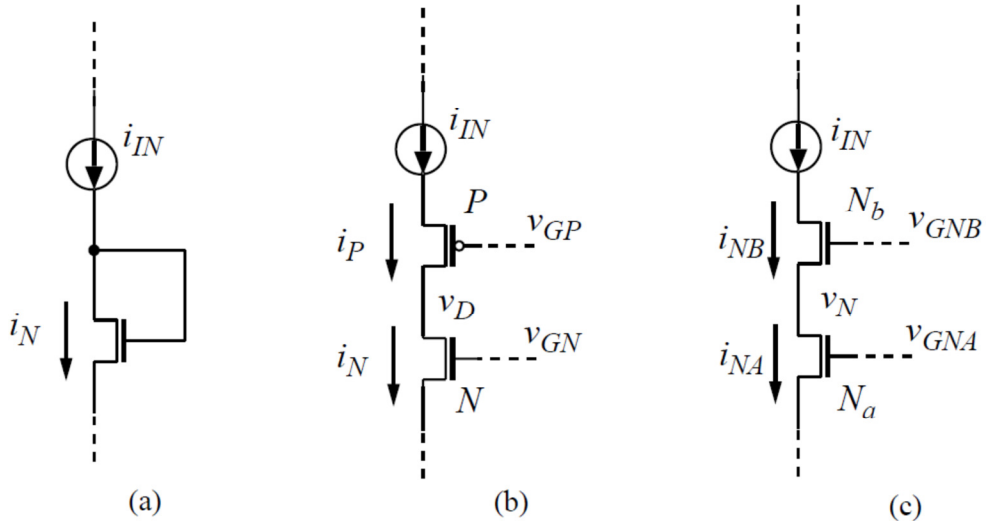

Fig. 2. MOSFET configurations. (a) Gate-drain short-circuit securing the saturation operation mode. (b) PMOS/NMOS series structure. (c) NMOS/NMOS series structure. Each of the transistors connected in series can operate in the saturation mode or other modes, depending on the level of i_{IN} and device parameters.

It is known that, if the current of a MOS transistor is fixed, the drain-source voltage can determine the operation mode of the device. As shown in Fig. 3, the operating points Q_1 and Q_2 are given by the same current i_{IN}, but the drain-source voltages, namely v_{DS1} and v_{DS2}, make one in the saturation region and the other in the triode one. In the structure shown in Fig. 2(b), the operation modes of N and P can be set up by adjusting the common-drain voltage v_D. From a static operation point of view, v_D is determined by the gate-source voltages of the two transistors and their characteristics of transconductance. From a dynamic operation point of view, during a transient period following an excitation of i_{IN}, the difference between i_N and i_P determines the direction in which v_D will change. As the gate-source voltages and geometrical parameters of the transistors are the elements determining the transconductances and the currents, one can adjust them to make v_D rise or fall during the transient period so that the transistor will be in the right operation mode and the current mirror in the right state.

To be more specific, let us look at the following two cases to see how the state of the structure shown in Fig. 2(b) can be determined by the transistor gate sizing or voltages, and how the operation modes of the transistors can be determined at a given

input current level. Assume that the initial state of this structure is as such: The input current i_{IN} is at a given level, the gate-source voltages of the two transistors and the voltage v_D are set up for both to operate in the saturation mode when the current equilibrium at v_D node is reached.

- Case 1: Modifying *W/L* ratio of *N* to be larger, while the gate-source voltages and the *W/L* ratio of *P* are kept the same, will lead to a decrease in v_D, due to a temporal increase of the NMOS current during the transient period, and the state of the circuit will be changed to "*P* in the saturation mode and *N* in the triode mode" when the new current equilibrium is reached with i_{IN} of the same level. Then, as long as i_{IN} is equal or lower than that given level, the transistors will be automatically driven to this state.
- Case 2: Increasing the gate-source voltage of *N*, while the gate-source voltage of *P* and the two *W/L* ratios are kept the same, will make the structure enter the same new state as that described in Case 1.

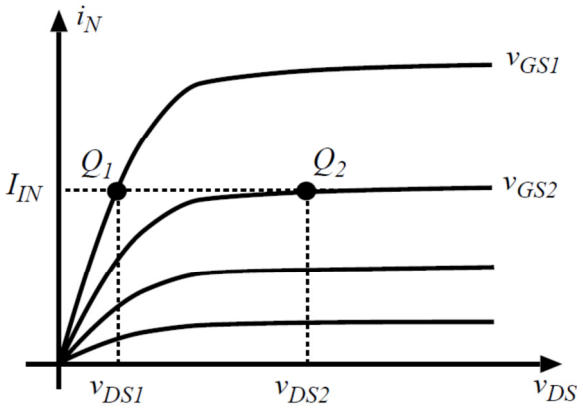

Fig. 3. Characteristics of a NMOS transistor. When a current i_{IN} is injected to the transistor, the transistor can be set up to operate at Q_1 or Q_2, visibly depending on its drain-source voltage v_{DS}. The derivative di_N/dv_{DS} at Q_1 is much greater than that at Q_2.

It should be noted that a change of the state in the structure of two MOS transistors connected in series results in a change of the nonlinearity of the characteristic of the nonlinear circuit in which the transistors are incorporated. Hence, an input current level that makes such a change is at the joint point of two adjacent nonlinear pieces of the target nonlinear function.

Between the two determining elements mentioned above, i.e., the gate-source voltage and the geometrical parameters of the transistors, the gate-source voltage may be more explorable as it can be made variable after the circuit fabrication, providing the users with a possibility of modifying the circuit function. Moreover, the voltage can be adjusted by applying another signal at the node, which makes it possible to modulate the nonlinear function in an adaptive manner. This gives the potential of implementing a sophisticated function in a simple circuit.

Fig. 2(c) shows another series structure where the transistors are not complementary. The node v_N is the drain of N_a and the source of N_b. Like v_D in Fig. 2(b), the voltage v_N is determined by the gate-source voltages of N_a and N_b, and/or the transistor aspect ratios of *W/L*, but in a completely different manner. This series structure can also be used in the design of nonlinear current mirrors, and will make the circuit characteristics have some other features than those provided by the structure 2(b).

In the following section, design examples of nonlinear current mirrors are presented. Each example involves one or more series structures shown in Fig. 2 and is of single-current-mirror circuit, i.e., only one current mirror being used to generate the needed pieces for a target nonlinear function. The description of the each design is followed by the presentation of the simulation results of the circuit.

3. DESIGN EXAMPLES

In this section, a couple of current mirror circuits are presented to demonstrate that the proposed piecewise nonlinear approach can be applied to implement nonlinear current transfer functions. It is also to illustrate that a single current mirror can be used to implement a nonlinear current transfer function by incorporating a series structure shown in Fig. 2(b) and/or 2(c). Moreover, by changing the connection of the series structure, one can alter the transfer function to suit another application. The simulation results of the circuits, by HSPICE unless otherwise specified, are also presented. As the currents in the design examples vary in a relatively wide range, they are displayed in a logarithmic scale. The transistor models used in the simulation are of a 0.18 μm CMOS technology and the supply voltage is 1.8 V.

3.1 Current amplification/attenuation circuit

It is often desirable, in analog signal processing circuits, that the ratio i_{OUT}/i_{IN} is high for a current amplification when i_{IN} is weak, and gets lowered, when i_{IN} becomes stronger, for an attenuation so that the circuit is not saturated. Such a function is particularly useful when adaptive characteristics of signal transfer are needed. The circuit for this function can be based on the structure shown in Fig. 1 [10], if the NMOS pair N_1 and N_2 are made to operate as follows.

- In case that i_{IN} is high, both N_1 and N_2 are in the saturation mode. If $(W/L)_{N2} < (W/L)_{N1}$, i_{OUT} will be an attenuated version of i_{IN}. The two transistors behave like a conventional current mirror for a linear down-scaling with the ratio $i_{OUT}/i_{IN} < 1$.
- In case of a low i_{IN}, N_1 operates in the triode mode. If N_2 is in the saturation mode, $i_{OUT} > i_{IN}$. The pair N_1 and N_2 perform a current amplification [11]. Please note that the amplification gain is defined as i_{OUT}/i_{IN}. It is not about small signals i_{in} and i_{out}.

For the design of the current mirror for the current amplification/attenuation, one can see that the transistor N_1 needs to change the operation mode according to the input, whereas N_2 is in the saturation mode regardless the input level. Fig. 4 illustrates a NMOS current mirror designed for this purpose and its PMOS version. In the mirror shown in Fig. 4(a), the series structure consisting of *P and* N_1 is placed in the left side of the circuit and the drain voltage v_D is adjustable by means of i_{IN}. The gate-source voltage of N_1 is equal to the source-gate voltage of *P*, noted as $v_{GSN} = v_{SGP} = v_G$, and the sum of the source-drain voltage of *P* and the drain-source voltage of N_1 is equal to v_G. The input current i_{IN} sets up v_G and v_D, and determines the operation mode of each transistor. If (v_G - v_D) is small, N_1 will be in the saturation mode and the circuit will behave like a conventional linear current mirror.

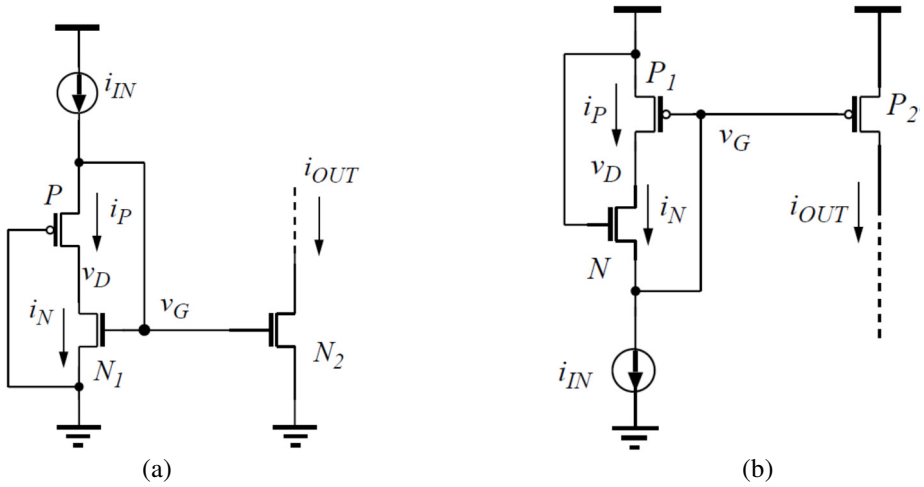

Fig. 4. Nonlinear current mirrors used for current amplification/attenuation [10]. (a) NMOS version. (b) PMOS version.

Assume that, in the circuit shown in Fig. 4(a), v_D is initially at a mid-point, i.e., around $v_G/2$, while $i_N = i_P$. To respond to an excitation of i_{IN}, v_G is being set up, updating i_N and i_P. The instantaneous current difference (i_P - i_N) determines how v_D will change. If (i_P - i_N) > 0, v_D will be raised and then stabilized at a higher voltage level, otherwise at a lower voltage level. Thus, we need to examine the conditions to make $i_P > i_N$ when i_{IN} is in the upper side of its range, and those to make $i_N > i_P$ when i_{IN} is in the lower side.

If i_{IN} is high, the transistors in the circuit shown in Fig. 4(a) will be in strong inversion. As $v_{GSN} = v_{SGP} = v_G$ and $|V_{tp}|$, the threshold of *P*, is greater than V_{tn} of N_1, the condition to make $i_P > i_N$ is $(\beta_p = \mu_p C'_{ox} \frac{W_p}{L_p}) >> (\beta_n = \mu_n C'_{ox} \frac{W_n}{L_n})$, if both devices are initially in the saturation mode, with C'_{ox} being the oxide capacitance per unit area and μ_n (or μ_p) the surface mobility in NMOS (or PMOS). This will lead to a state of $v_D > (v_G - V_{tn})$ when the steady state of $i_P = i_N = i_{IN}$ is reached after the transient period.

In case of a weak i_{IN}, the transistors are in weak inversion and have exponential characteristics. The following equations are used to calculate the currents i_N and i_P [8].

$$i_N = I_{Sn} e^{\frac{v_G - V_{Mn}}{n\varphi_t}} (1 - e^{-\frac{v_D}{\varphi_t}}) \quad (1)$$

$$i_P = I_{Sp} e^{\frac{v_G - |V_{Mp}|}{n\varphi_t}} (1 - e^{\frac{v_D - v_G}{\varphi_t}}) \quad (2)$$

where $I_{Sn} = \frac{1}{2}\frac{W_n}{L_n}\mu_n \varphi_t^2 \frac{\sqrt{2q\varepsilon_t N_A}}{\sqrt{2\varphi_{Fn}+V_{SBn}}}$, $I_{Sp} = \frac{1}{2}\frac{W_p}{L_p}\mu_p \varphi_t^2 \frac{\sqrt{2q\varepsilon_t N_D}}{\sqrt{2\varphi_{Fp}+V_{BSp}}}$, $V_{Mn} = V_{FB} + 2\varphi_{Fn} + \gamma_n\sqrt{2\varphi_{Fn} + V_{SBn}}$, $V_{Mp} = V_{FB} + 2\varphi_{Fp} + \gamma_p\sqrt{2\varphi_{Fp} + V_{BSp}}$, and $n = 1 + \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}}$. Also V_{Mn} is the upper limit of the weak inversion in terms of v_{GS} of a NMOS, V_{Mp} is that in terms of v_{SG} of a PMOS, φ_t is the thermal voltage, φ_F is the Fermi level, V_{FB} is the flat band voltage, γ is the body effect coefficient, and ε_t is permittivity of silicon.

Assume that v_D in Fig. 4(a) is initially at such a level that both $e^{-\frac{v_D}{\varphi_t}}$ and $e^{\frac{v_D - v_G}{\varphi_t}}$ are much smaller than unity, and we have $i_N \approx I_{Sn} e^{\frac{v_G - V_{Mn}}{n\varphi_t}}$ and $i_P \approx I_{Sp} e^{\frac{v_G - |V_{Mp}|}{n\varphi_t}}$. In this case, to secure $i_N > i_P$, one should have $I_{Sn} e^{\frac{v_G - V_{Mn}}{n\varphi_t}} > I_{Sp} e^{\frac{v_G - |V_{Mp}|}{n\varphi_t}}$, i.e., $\frac{I_{Sp}}{I_{Sn}} < e^{\frac{|V_{Mp}| - V_{Mn}}{n\varphi_t}}$. If this condition is satisfied, v_D will be reduced, easily to be $v_D < \phi_t$, and consequently v_G will be increased to compensate for the instantaneous decrease of i_N due to the lowered v_D. The voltages v_G and v_D are stabilized when $i_N = i_P = i_{IN}$. The same v_G is applied to N_2. If the drain-source voltage of N_2 is much greater than ϕ_t, we will have $i_{OUT} >> i_{IN}$, which makes a current amplification.

Summarizing the analysis presented above, to make the nonlinear current mirror illustrated in Fig. 4(a) operate as a current amplifier/attenuator, the transistors N_1 and P should satisfy the conditions

$$\beta_p >> \beta_n \text{ and } \frac{I_{Sp}}{I_{Sn}} < e^{\frac{|V_{Mp}| - V_{Mn}}{n\varphi_t}}.$$

The former is to make $v_D > (v_G - V_{tn})$, when the devices are in strong inversion, in order to have $i_{OUT}/i_{IN} < 1$ while $(W/L)_{N2} < (W/L)_{N1}$, and the latter is to lower v_D, in case of weak inversion, for $i_{OUT}/i_{IN} > 1$. It is obvious that in the curve of the current transfer characteristic i_{OUT} versus i_{IN}, there must be a particular point where $i_{OUT}/i_{IN} = 1$.

The design process can be quite simple. If the parameters of the fabrication process are given, one can choose the W/L ratios of N_1 and P to satisfy the conditions $\beta_p >> \beta_n$. It should be mentioned that I_{Sp}, I_{Sn}, V_{Mp} and V_{Mn} depend on the source-voltages of the

transistors and v_G, the source-voltage of P, is i_{IN}-dependent. If all the parameters of the transistors are fixed to make $\beta_p >> \beta_n$, one can find a particular value of i_{IN} that makes $\frac{I_{Sp}}{I_{Sn}} \leq e^{\frac{|V_{Mp}|-V_{Mn}}{n\varphi_t}}$, which sets the upper boundary of i_{IN} for N_1 to be in the triode mode, i.e., for the circuit to perform the current amplification. If i_{IN} is low enough within the boundary, the condition for the amplification will be satisfied. Otherwise the circuit will automatically be set in the state of the linear current down-scaling as $\beta_p >> \beta_n$ and $(W/L)_{N2} < (W/L)_{N1}$.

It is obvious that the particular value of i_{IN} for the upper boundary corresponds to the chosen W/L ratios of N_1 and P. In other words, one can size N_1 and P to have a desired value of the i_{IN} boundary and to satisfy the conditions $\beta_p/\beta_n >> 1$. It should, however, be noted that, in the circuit shown in Fig. 4 (a), as $\mu_n/\mu_p >> 1$ and $(|V_{Mp}| - V_{Mn}) >> n\phi_t$, the W/L ratio of P may need to be much larger than that of N_1 to make the i_{IN} boundary at an appropriate level.

Fig. 4 (b) illustrates the complementary version of the nonlinear current mirror shown in Fig. 4(a). In this circuit, the transistors P_1 and N should satisfy the conditions

$$\beta_p << \beta_n \text{ and } \frac{I_{Sn}}{I_{Sp}} < e^{\frac{V_{Mn}-|V_{Mp}|}{n\varphi_t}}$$

for the current amplification/attenuation. As $\mu_n/\mu_p >> 1$, $\beta_n/\beta_p >> 1$ can be easily made without a significant size difference of the devices P_1 and N. Please also note that in this version, it is the transistor N that has the body effect, and the numeric value of $(V_{Mn} - |V_{Mp}|)$ is, in general, smaller than that of $(|V_{Mp}| - V_{Mn})$ in the circuit shown in Fig. 4(a). Thus, the conditions can be satisfied in a wide range of the input current, without need of an excessive difference in W/L ratio between the NMOS and PMOS transistors.

It should be noted that the gate voltage of P in Fig. 4(a) and that of N in Fig. 4(b) are connected to V_{SS} and V_{DD}, respectively. They can, however, be set up at other voltage levels, or adjusted by another signal, to modulate the characteristics of the circuits.

The circuit shown in Fig. 4(b) has been simulated to validate the function. The DC characteristics of the circuit, when the transistor size ratios are specified in Table 2, are shown in Fig. 5. The input current range in this simulation is from 1 nA to 10 μA. It is observed that, in the lower part of the current range when the transistors are in the weak inversion region, v_D, the drain voltage of the transistor P_1 is very close to its source voltage at 1.8 V, making a current amplification. In the upper part of the current range, v_D is close to v_G, making P_1 operate in the saturation mode and the circuit a conventional current mirror performing a linear down-scaling as $(W/L)_{P2} < (W/L)_{P1}$. These characteristics demonstrate that the circuit shown in Fig. 4(b)

performs a current amplification when the input current is at the lower side of the range, and an attenuation if the input is in the upper side.

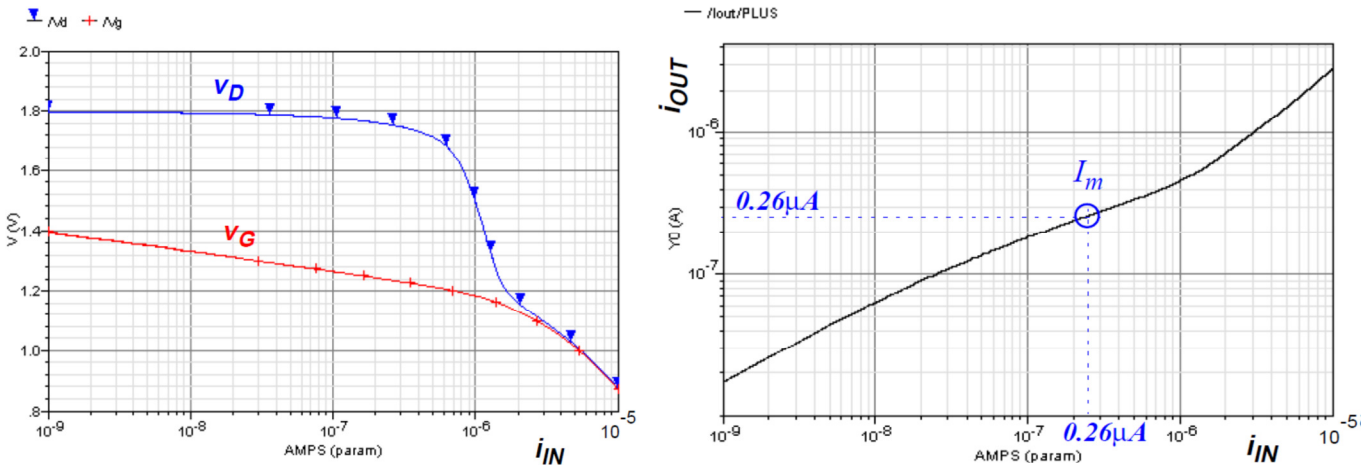

Fig. 5. DC characteristics of the circuit shown in Fig. 4(b). For this simulation, the transistors are sized with the *W/L* ratios shown in Table 2. The curves v_G versus i_{IN} and v_D versus i_{IN} are shown in the first graph. The other graph shows the current transfer characteristic i_{OUT} versus i_{IN}. If $i_{IN} < I_m = 0.26$ μA, $i_{OUT}/i_{IN} > 1$, otherwise $i_{OUT}/i_{IN} < 1$. The current magnitude is displayed in a logarithmic scale.

Table 2 Transistor *W/L* ratios in Fig. 4(b)

P_1	P_2	N
W_{min}/L_{min}	$W_{min}/ 2.8L_{min}$	$23W_{min}/L_{min}$
W_{min}: minimum width; L_{min}: minimum length		

The nonlinear current mirror illustrated in Fig. 4(b) can be used for a special signal transfer. The circuit illustrated in Fig. 6 is a current-to-voltage converter, in which the PMOS version of the current mirror, consisting of the three transistors placed within the red dashed frame, is incorporated. The input current i_{IN} varies over a dynamic range of more than five decades. The conversion is based on a low-pass current filtering performed by the 5 transistors, namely N_1, N_2, N_3, P_3, and P_4, and the time constant of this filtering structure is determined by the transconductance of P_3 and the capacitance at the the common-gate of P_3 and P_4 [12]. The dynamic range of the 5-transistor converter is, however, not much more than three decades, without a large capacitor at the common-gate. To solve the problem of this "mismatch" of dymanic ranges, i_{IN} is applied to the current mirror having the current transfer characteristic illustrated in Fig. 5. This current transfer is to make the input current amplified if it is in the lower section of the input range and attenuated if it is in the upper section so that the dynamic range of the current will be reduced, without losing its signal variations, to match that of the current filter. The transistor N_{BP} is normally off. However, if i_{IN}

is strong enough to make its gate-source voltage (V_{DD} - v_G) to reach a predefined level, N_{BP} will be conducting to reduce the current i_N so that v_G will not be too low for the current mirror to operate normally.

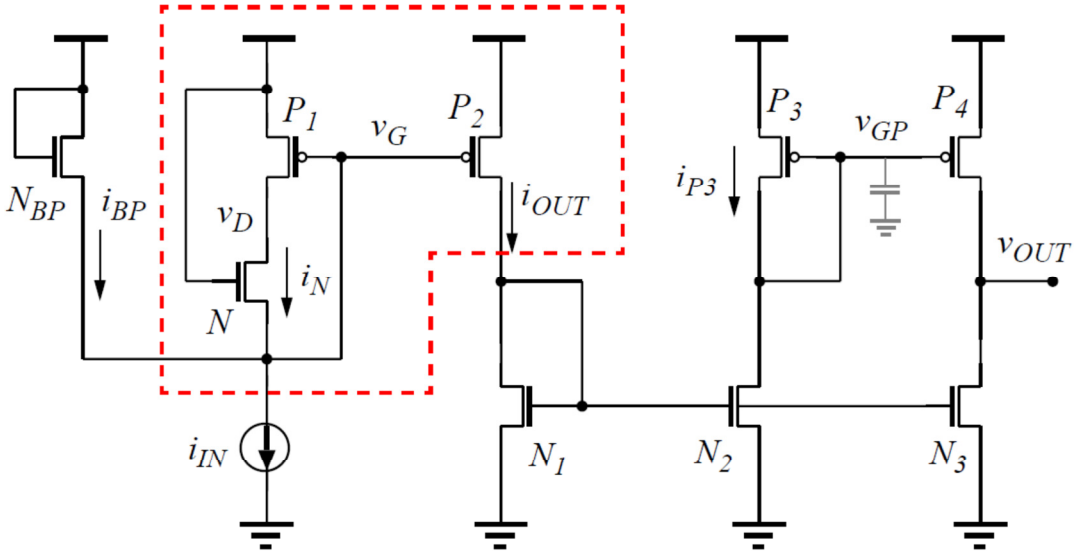

Fig. 6. Wide dynamic range current-to-voltage converter. The nonlinear current mirror, placed within the dashed-line frame, is employed to amplifier i_{IN} if it is of nano-Amperes and attenuate it if it is of micro-Amperes or upper. The current-to-voltage conversion is done by the five transistors in the right side [12].

The waveforms presented in Fig. 7 illustrate how the circuit shown in Fig. 6 functions when a varying input current is applied, with the transistor size ratios specified in Table 3. The voltage v_D is high when i_{IN} is in the lower side of its range, implying that P_1 operates in the triode mode for the current amplification, and it is low when i_{IN} is in the upper side of the range. It is observed that, by means of the current transfer provided by the nonlinear current mirror, the dynamic range of i_{OUT} is much smaller than that of i_{IN} while the current variations are however transmitted, enabling the low-pass filter to convert i_{OUT} to v_{OUT} easily. Without this nonlinear current transfer, the low-pass current filter would need a large capacitor given by a source-drain-shorted MOS gate sized 20 µm x 20 µm placed at the common-gate of P_3 and P_4 to do the same conversion [12].

Table 3 Transistor *W/L* ratios in Fig. 6

P_1	P_2	N	N_{BP}	
W_{min}/L_{min}	$W_{min}/2.8L_{min}$	$23W_{min}/L_{min}$	$20W_{min}/L_{min}$	W_{min}: minimum width L_{min}: minimum length
N_1	N_2	N_3	P_3, P_4	
$W_{min}/2.3L_{min}$	$W_{min}/11L_{min}$	$W_{min}/11L_{min}$	$W_{min}/11L_{min}$	

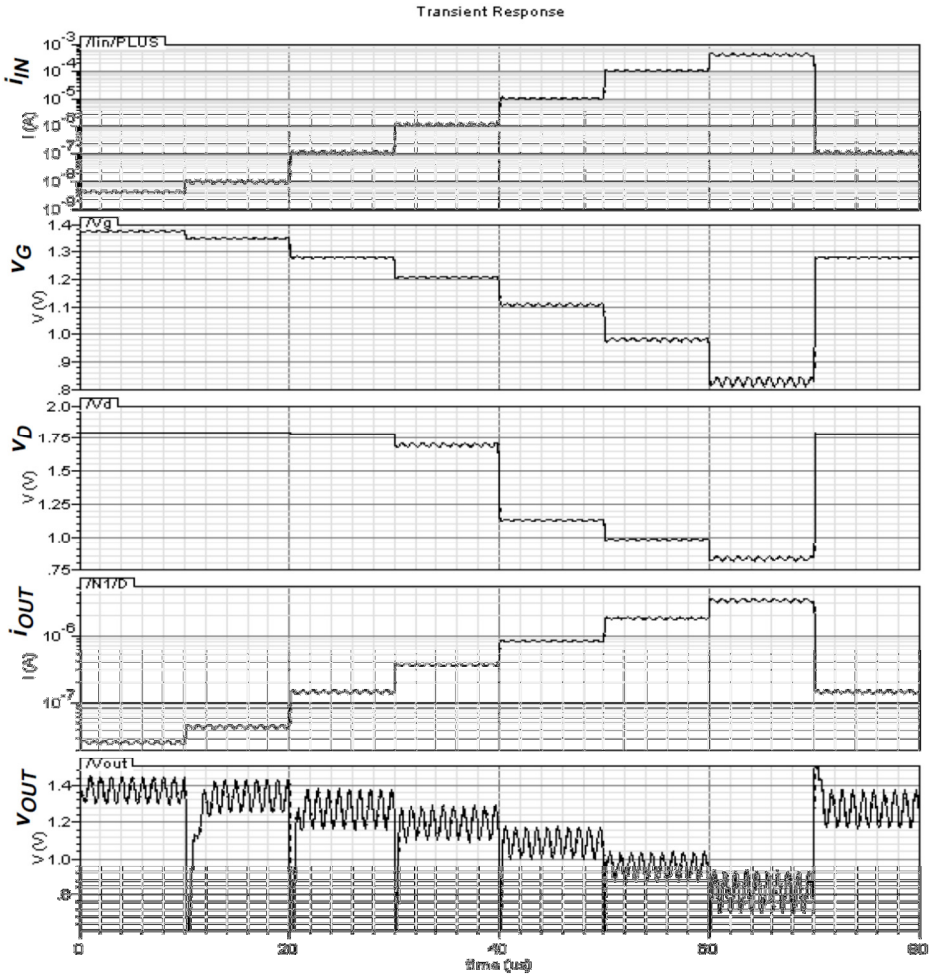

Fig. 7. Simulation waveforms of the circuit illustrated in Fig. 6, when the transistors are sized as those shown in Table 3. The input current i_{IN} varies from 4 nA to 0.4 mA, the magnitude of the signal variation is 10% of the DC level and the frequency is 1 MHz. The currents are displayed in a logarithmic scale.

3.2 Current scaling and clamping

In the nonlinear current mirror shown in Fig. 8, the transistors N_1 and P_1 operate in the saturation region, but the operation mode of N_2 and that of P_R depend on the input current i_{IN}. Let V_P to be fixed at a low voltage level. There will be the two cases.

- If i_{IN} is weak, v_G will be low. Assuming that both N_2 and P_R are initially in the saturation mode, the low v_G and low V_P will cause a transient current difference $(i_P - i_N) > 0$, raising v_D and making N_2 operate in the saturation mode and P_R in the triode mode when the steady state is reached. In this case, the circuit performs a "linear" scaling, i.e., i_N being "linearly" proportional to i_{IN} and determining i_P and i_{OUT}. It should be mentioned that i_P has an upper limit I_{Pmax}, determined by $(V_{DD} - V_P)$, the sum of the source-gate voltage of P_1 and that of P_R, if their *W/L* ratios are given. When both P_1 and that of P_R are in the saturation mode, $i_P = I_{Pmax}$.

- If i_{IN} is high enough to make i_P reach the level of I_{Pmax}, any further increase of i_{IN} will lead to the triode operation of N_2 while i_N is at its upper limit imposed by i_P, i.e., $i_N = i_P = i_{Pmax}$.

Therefore, the current mirror performs a "linear" scaling in the lower part of the input range and a current clamping in the upper part. The clamping level is determined by the voltage V_P and the W/L ratios of the transistors. It should be noted that a higher V_P results in a smaller source-gate voltages of P_R or P_1, thus lowering the upper limit of i_P and i_N. i.e., a lower clamping level.

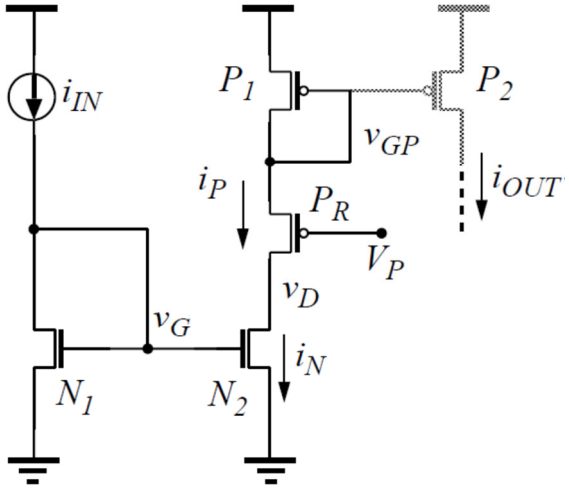

Fig. 8. Nonlinear current mirror performing current scaling and clamping. The branch of series NMOS-PMOS, also shown in Fig. 2(b), is placed in the right side of the NMOS mirror. The PMOS pair, P_1 and P_2, makes a linear current mirror for the current output.

The circuit shown in Fig. 8 has been simulated. The result is illustrated in Fig. 9. One can observe that v_D changes from high to low when i_{IN} increases, indicating the transistor N_2 switches its mode of operation from the saturation to the triode to respond to the change of i_{IN}. The characteristic of i_{OUT} versus i_{IN} confirms the function of current clamping.

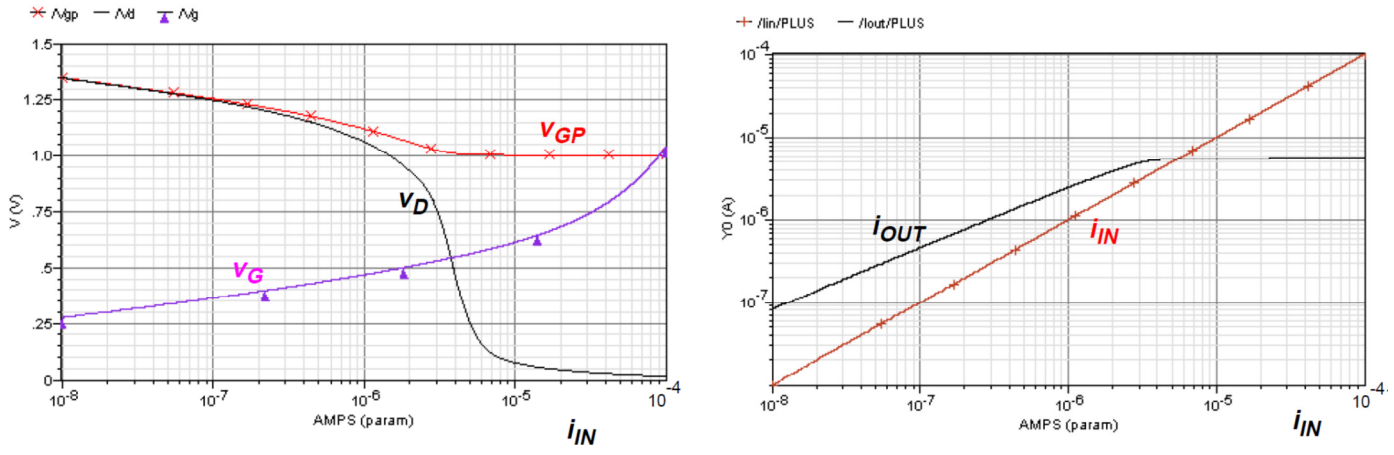

Fig. 9. DC characteristics of the circuit shown in Fig. 8 when $V_P = 0$ V. All the transistors, but N_2 having $W_2/L_2 = 2W_{min}/L_{min}$, are minimum-sized. In case of $i_{IN} < 4$ μA (approximately), v_D is high enough to make N_2 operate in the saturation mode and i_{OUT} increases with i_{IN}. If $i_{IN} > 4$ μA, i_{OUT} remains at a level about 6 μA and v_D is low to drive N_2 in the triode region.

The DC characteristics illustrated in Fig. 9 also show that in the lower end of the input current range, the ratio of i_{OUT}/i_{IN} is very much deviated from the scaling factor of 2 specified by the *W/L* ratios of the two NMOS transistors. This reflects a very pronounced mismatch effect in a weak current operation. If i_{IN} gets higher, i_{OUT}/i_{IN} decreases because of the decrease of v_D, as the effect of the channel length modulation is strong due to the short gate length of N_2. This decrease in i_{OUT}/i_{IN} is also due to the reduced mismatch effect in the higher current level. Moreover, while i_{IN} is increasing, the circuit moves from the state of current "scaling" to that of "clamping" gradually, which adds another reason for i_{OUT}/i_{IN} to decline when i_{IN} is approaching the level that changes the state for the current clamping.

The circuit shown in Fig. 8 can have different applications. For example, it can be used for a conditional current signal transfer. The input current signal will be transferred to the output if it varies at a DC current level in the lower section of the range, otherwise the current variation will be eliminated. The circuit can also be used to generate a variable biasing current for a voltage amplifier to extend its operation range and/or to make the gain variable.

3.3 Current mirror having a transfer function of double-side derivatives

The derivative di_{OUT}/di_{IN} of a nonlinear current mirror is input-dependent. In the current amplifer-attenuator shown in Fig. 4(a) or (b), it changes from $di_{OUT}/di_{IN} > 1$ to $di_{OUT}/di_{IN} < 1$ when the input current increases. Fig. 10 shows another nonlinear current mirror that gives $di_{OUT}/di_{IN} > 0$ or $di_{OUT}/di_{IN} < 0$, depending on its input current. The structure of this circuit is different from that shown in Fig. 8 by the short-circuit between the gate of the PMOS P_R and the NMOS common-gate v_G. This connection makes the "algebraic" sum of the gate-source voltages of the transistors, namely N_1 (or N_2), P_1 and P_R, equal to a fixed value V_{DD}, expressed as

$$V_{DD} = v_{GS\_N1} + v_{SG\_P1} + v_{SG\_PR}$$

where $v_{GS\_N1} = v_G$, $v_{SG\_P1} = V_{DD} - v_{GP}$, and $v_{SG\_PR} = v_{GP} - v_G$. It should be noted that v_G increases with i_{IN}, reducing $(v_{SG\_P1} + v_{SG\_PR})$, and the consequence of this voltage reduction can be one of the following two scenarios, depending on the input current level and the state of N_2 and P_R, while N_1 and P_1 are hard-wired to operate in the saturation mode.

- If i_{IN} is in the upper side of the input range, i.e., a relatively large v_G and small $(v_{SG\_P1} + v_{SG\_PR})$, i_{OUT} will decrease if i_{IN} increases, i.e., $di_{OUT}/di_{IN} < 0$. If P_R is in the saturation mode, an increase in v_G will make the source-gate voltage of each of the two PMOS transistors decrease and thus the current i_P will decrease. In this case, i_P determines i_N and N_2 is driven in the triode region.

- If i_{IN} is in the lower side of the input range, if i_{IN} increases, i_{OUT} will also increase, because v_{SG_P1} increases with v_G, and $di_{OUT}/di_{IN} > 0$. As both v_{GS_N1} and v_{SG_P1} are small, the source-gate voltage of P_R, $v_{SG\_PR} = V_{DD} - (v_{GS\_N1} + v_{SG\_P1})$, can be large enough to drive P_R in the triode mode, resulting in a small source-drain voltage ($v_{GP} - v_D$), which makes v_D large enough for N_2 to operate in the saturation mode. Hence, N_1 and N_2 operate like a conventional current mirror, and i_N sets up v_{SG_P1}.

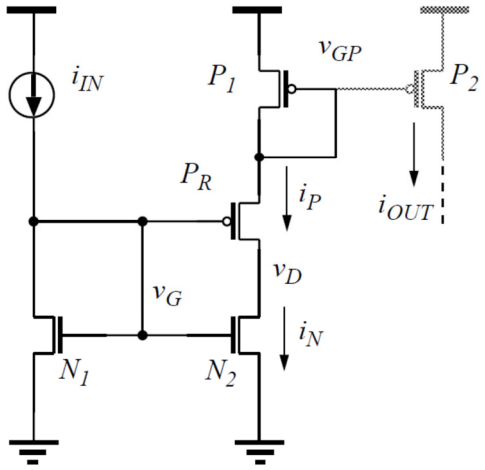

Fig. 10. Nonlinear current mirror, of which the current transfer function has a positive or negative derivative di_{OUT}/di_{IN}, depending on the level of i_{IN}.

If i_{IN} increases from the lower end of its range, the operating point of P_R will move from the triode region towards the saturation region while i_{OUT} is increasing. When P_R is driven to change its operation mode to the saturation, i_{OUT} reaches its maximun level I_{PK}. In other words, at the point where $di_{OUT}/di_{IN} = 0$, all the four transistors are in the saturation region. This state is "unstable". It does not last in practice and an excitation of a tiny increase (or decrease) of i_{IN} will drive N_2 (or P_R) to the triode region, as i_N tends to increase (decrease) while i_P tends to decrease (increase), leading to a decrease (increase) of v_D. Let $I_{IN\text{-}P}$ denote the level of the input current that makes $i_{OUT} = I_{PK}$. The value of $I_{IN\text{-}P}$ can be calculated based on $i_P = i_N$ and $i_P = i_{P1}$, i_{P1} denoting the current in P_1, under the condition that all the transistors are in the saturation mode. If N_1 and N_2 are identical, and P_1 and P_R are also so, the relationship between $I_{IN\text{-}P}$ and the other parameters of the circuit can be expressed as follows, and the derivation of the expression is found in Appendix.

$$I_{IN-P} \approx \frac{\beta_n}{2}\left(\frac{V_{DD}-2|V_{tp}|+2\alpha V_{tn}}{1+2\alpha} - V_{tn}\right)^2, with\ \alpha = \sqrt{\frac{\beta_n}{\beta_P}} \qquad (3)$$

One can see that $I_{IN\text{-}P}$ is related to the supply voltage V_{DD}, and the transistor size ratios, if the technological parameters are given. A larger V_{DD} results in a larger $v_{SG\_PR} = V_{DD} - (v_{GS\_N1} + v_{SG\_P1})$, giving more room for P_R to operate in the triode region, and thus moving $I_{IN\text{-}P}$ upwards. Also, $I_{IN\text{-}P}$ is propotional to the W/L of N_1, as the larger the ratio is, the smaller v_{GS_N1} and the larger v_{SG_PR} for a given i_{IN}, and the higher $I_{IN\text{-}P}$. Moreover, the W/L ratios of P_1 and P_R have also some effect on $I_{IN\text{-}P}$. If the other

parameters are fixed, making the gates of P_1 and P_R wider will result in a higher i_P and consequently a higher v_D when the current equilibrium at the common-drain of N_2 and P_R is reached, which may make N_2 to operate in the saturation region and P_R in the triode region and raise $I_{IN\text{-}P}$.

It should be noted that at $i_{IN} = I_{IN\text{-}P}$, $di_{OUT}/di_{IN} = 0$, i.e., zero signal gain. Also, as $I_{IN\text{-}P}$ is related to the supply voltage V_{DD} and the characteristics of the transistors, it is very sensitive to a modification of V_{DD} and to the process variation. In other words, $I_{IN\text{-}P}$ will be shifted left-or-rightwards if the voltage or a transistor parameter gets changed. Moreover, as mentioned above, the state of P_R and N_2 simultaneously being in the saturation mode is unstable, and V_{DD} should be large enough to satistfy the condition that $V_{DD} = v_{GS\_N1} + v_{SG\_P1} + v_{SG\_PR}$ when P_R or N_2 is in the triode mode. If V_{DD} is reduced, one may increase the W/L ratios of the transistors so that for the same current the gate-source voltages will be reduced to satisfy the condition. One can also use the complementary version of the circuit so that there will be one PMOS and two NMOS transistors in series, instead of one NMOS and two PMOS ones, in the right side of the current mirror, to reduce the “algebraic" sum of the three gate-source voltages.

The circuit shown in Fig. 10 has been simulated. Fig. 11 illustrates the characteristics of the circuit that confirm the circuit function of the double current derivatives in different parts of the input range, as described in the preceding paragraphs.

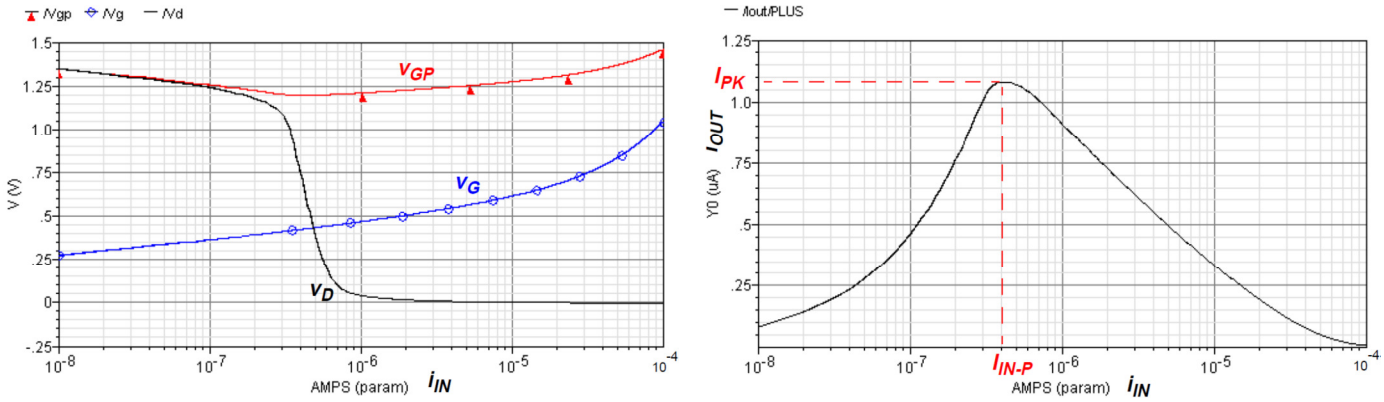

Fig. 11. DC characteristics of the circuit illustrated in Fig. 10. All the transistors, but N_2 having $W_2/L_2 = 2W_{min}/L_{min}$, are minimum-sized. If v_D is high, driving N_2 in the saturation mode, the current derivative $di_{OUT}/di_{IN} > 0$ as i_{OUT} follows i_{IN}, and if v_D is low, $di_{OUT}/di_{IN} < 0$. At the point $i_{IN} = I_{IN\text{-}P}$, $i_P = I_{Pmax} = i_{PK}$, $di_{OUT}/di_{IN} = 0$.

The current transfer characteristic of the double-side derivatives can be used in signal processing or communications to transmit current variations in a special manner. For example, two current signals differentiate themselves by their distinguished DC levels, which can be a case of currents generated by different sensors, and they are merged to be transmitted by a single channel, while one of them needs a phase shift of 180 degrees and the other does not. The simulation result illustrated in Fig. 12 shows that the circuit shown in Fig. 10 can be used to implement such a function. It performs a current signal transfer without

inversion if i_{IN} is below $I_{IN\text{-}P}$, otherwise with an inversion. In such an application, the input signal should be biased well below or above $I_{IN\text{-}P}$, to avoid the point of $di_{OUT}/di_{IN} = 0$.

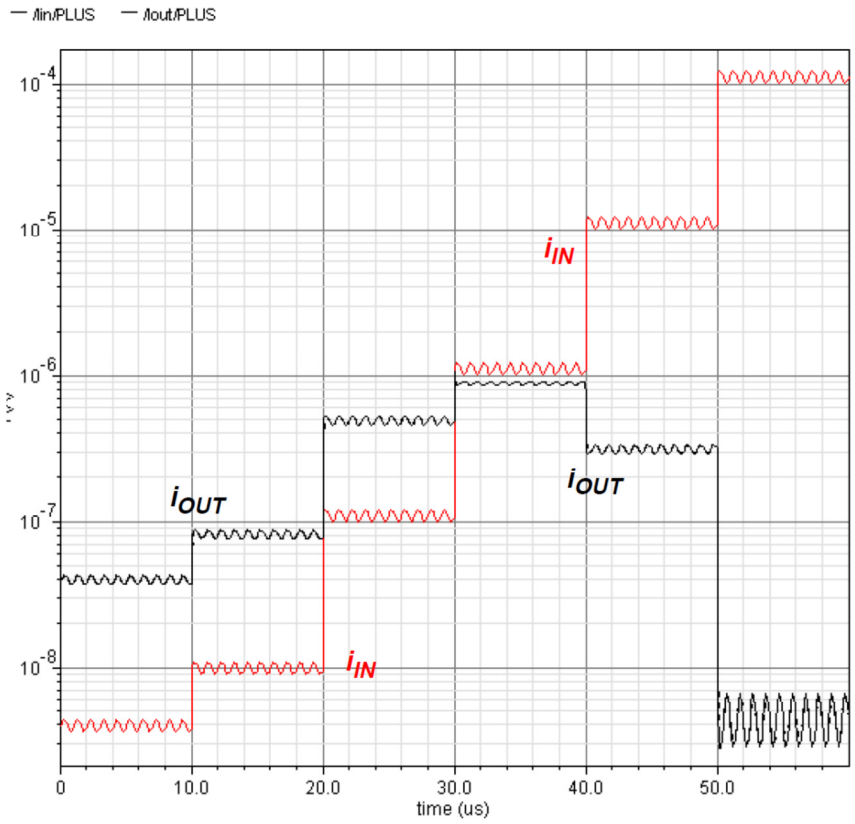

Fig. 12. Simulation waveforms of the circuit illustrated in Fig. 10. The waveform of i_{IN} is printed in red (or gray if printed in white/black) and i_{OUT} in black. The variation of i_{OUT} is in the opposite direction compared to that of i_{IN} when the DC level of i_{IN} is high.

3.4 Modulations of the current transfer characteristics

In the designs presented in the preceding sub-sections, one of the two common-gate transistors is replaced by the series structure of two transistors shown in Fig. 2(b) in order to modulate the drain voltage of one of the common-gate transistors. Fig. 13 illustrates another current mirror in which each of the common-gate NMOS transistors, namely N_1 and N_2, has a PMOS transistor connected to its drain node to make both drain voltages modulatable. The gate of P_R in Fig. 13 is short-circuited to v_G, like that in the circuit shown in Fig. 10, making the source-gate voltage of P_R decrease while i_{IN} is increasing. The gate terminal of P is reserved for the connection to a fixed or varying voltage to control the drain voltage of N_1, which is different from the circuit illustrated in Fig. 10.

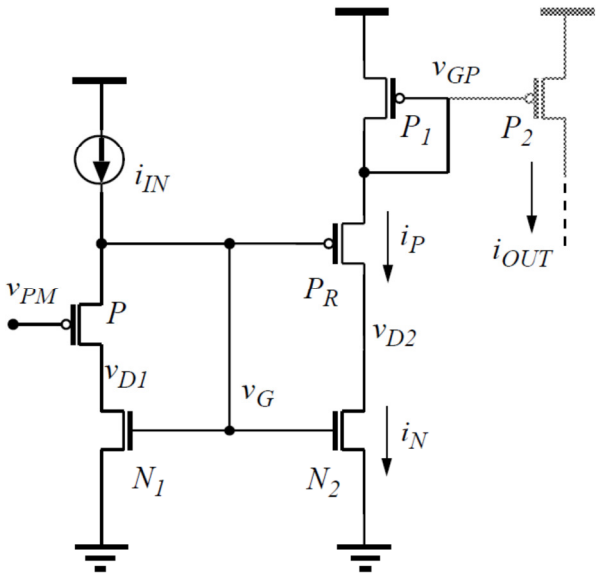

Fig. 13. Nonlinear current mirror. The PMOS P and P_R are used to adjust the voltages v_{D1} and v_{D2}, respectively.

As mentioned previously, the characteristics of a current mirror are related to the operation modes of its transistors, and the drain voltage of each transistor is the key to determine the operation mode. In the circuit shown in Fig. 13, the drain voltage v_{D1}, or v_{D2} is determined by the difference between the two transistor currents meeting at the node during the transient period after an excitation of the input. The device *W/L* ratios, and the gate voltages of the transistors are used to control the currents. Hence the characteristics of the current mirror can be made adjustable by means of changing the *W/L* ratios or by means of tuning the gate voltage of P.

The circuit illustrated in Fig. 13 has been simulated with two different settings of the transistor *W/L* ratios specified in Table 4, while v_{PM} = 0 V. When all the transistors are equally sized, its characteristics obtained are illustrated in Fig. 14. Due to the difference between μ_n and μ_p, and the body effect in the transistor P, the current driving capacity of N_1 is much stronger than that of P, making v_{D1} very low over the entire input current range, as shown in Fig. 14, and N_1 to operate in the triode mode. In this case, for a given input current, v_G needs to be higher than that in case of N_1 operating in the saturation mode. This higher v_G enhances i_N, reduces source-gate voltage of P_R, weakening i_P, and consequently results in a very low v_{D2}. Hence, N_2 is made to operate in the triode mode and P_R in the saturation mode, which makes the state in which an increase of i_{IN} causes a decrease of the current in P_R, i.e., $di_{OUT}/di_{IN} < 0$. The circuit has a similar current transfer characteristic as that in the upper section of the input current range shown in Fig. 11. Because the current driving capacity of N_1 is made stronger than that of P, N_1 can not be in the saturation mode and it is thus impossible for the circuit to be a “linear” current mirror, regardless the input level.

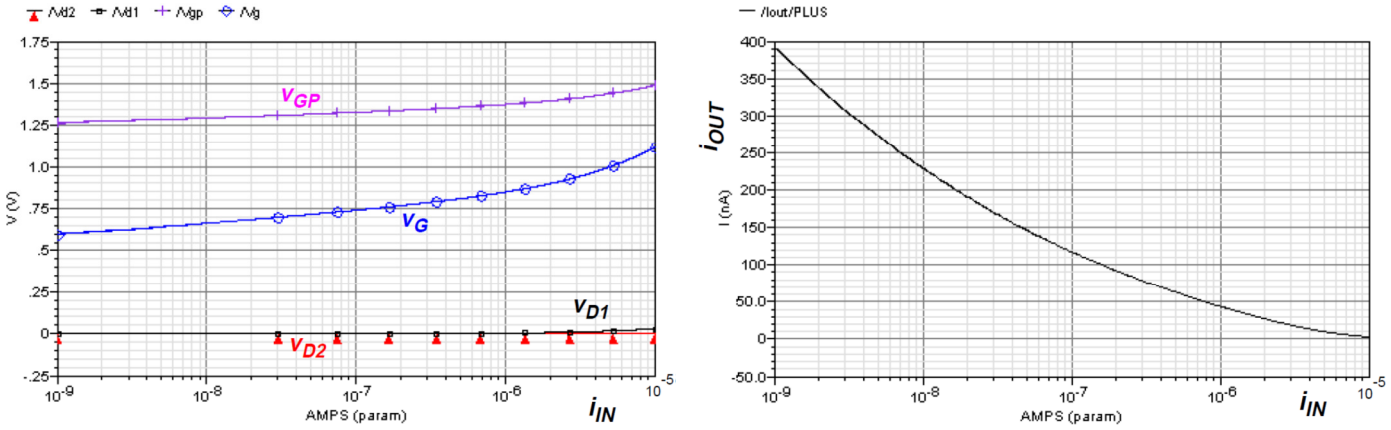

Fig. 14. DC characteristics of the circuit shown in Fig. 13 when all the transistors are equally minimum-sized (see the left column of Table 4) and v_{PM} = 0 V. Both v_{D1} and v_{D2} are very low, indicating N_1 and N_2 operating in the triode mode.

Table 4 *W/L* ratios to obtain the results shown in

	Fig. 14	Figs. 15, 16 and 18
P	W_{min}/L_{min}	$10W_{min}/L_{min}$
$\boldsymbol{N_1}$	W_{min}/L_{min}	$W_{min}/3L_{min}$
$\boldsymbol{N_2}$	W_{min}/L_{min}	$W_{min}/10L_{min}$
$\boldsymbol{P_R}$	W_{min}/L_{min}	$10W_{min}/L_{min}$
$\boldsymbol{P_1}$	W_{min}/L_{min}	$10W_{min}/L_{min}$
$\boldsymbol{P_2}$	W_{min}/L_{min}	$10W_{min}/L_{min}$
W_{min}: minimum width; L_{min}: minimum length		

If the transistors in Fig. 13 are sized as those shown in the right column of Table 4, the circuit characteristics obtained by the simulation are illustrated in Fig. 15. The transistors *P, P*$_R$ and *P*$_1$ are made much wider than those in the previous case to improve the current driving capacity of the PMOS devices. Also, for a given current, their source-gate voltages are reduced, leading to a lower v_G and higher v_{GP}, i.e., a larger source-gate voltage of P_R to enhance i_P. In the lower part of the current range, the voltage v_{D2} is high, as shown in Fig. 15, resulting from the much enhanced i_P against the relatively weakened i_N. Consequently N_2 operates in the saturation mode and i_N increases with i_{IN}. If the input current rises to the upper part of its range, the raised v_G and

lowered v_{GP} weakens the current driving capacity of P_R, despite its enhanced W/L ratio, and results in a low v_{D2}, driving P_R in the saturation mode and N_2 in the triode mode. Thus, i_P and i_{OUT} will decrease if i_{IN} increases, as shown in Fig. 15.

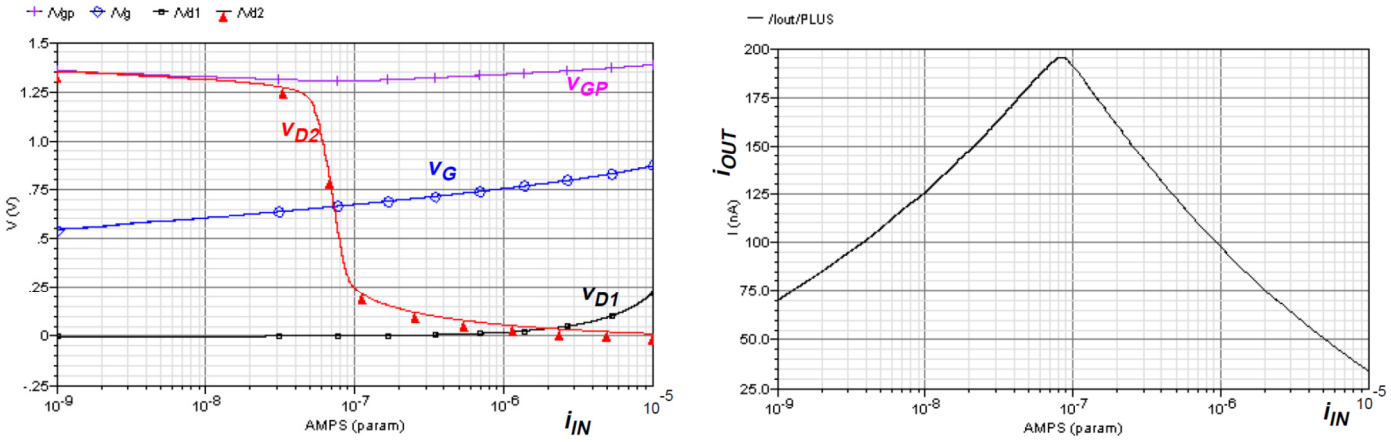

Fig. 15. DC characteristics of the circuit shown in Fig. 13 when the W/L ratios of the PMOS transistors are much larger than those of the NMOS ones, specified in the right column of Table 4, and $v_{PM} = 0$ V.

Also, as the current in a MOS transistor is sensitive to the gate voltage, adjusting v_{PM} in the circuit shown in Fig. 13 can result in a change of the current and then the drain voltage in order to modulate the current transfer characteristics. Fig. 16 illustrates the characteristics obtained with three levels of v_{PM} when the transistors are sized as specified in the right column of Table 4. In case of $v_{PM} = 0$ V, the characteristics are identical to those illustrated in Fig. 15 as the circuit is simulated under the exactly same conditions. If v_{PM} is fixed at a higher level, v_G will have to be higher for the transistor P to accommodate the same current, enhancing i_N and reducing (v_{GP} - v_G), the source-gate voltage of P_R, i.e., weakening i_P. Thus, by raising v_{PM}, the state of triode-N_2 and saturation-P_R will be set up at a lower level of i_{IN}, which makes the current transfer characteristic shift leftward, as shown in Fig. 16. The voltage v_{PM} can thus be used for an easy modification of the circuit characteristics. If this voltage is time-varying, the circuit function will also be made to vary with it, which may provide the designers with a simple way of implementing sophisticated functions.

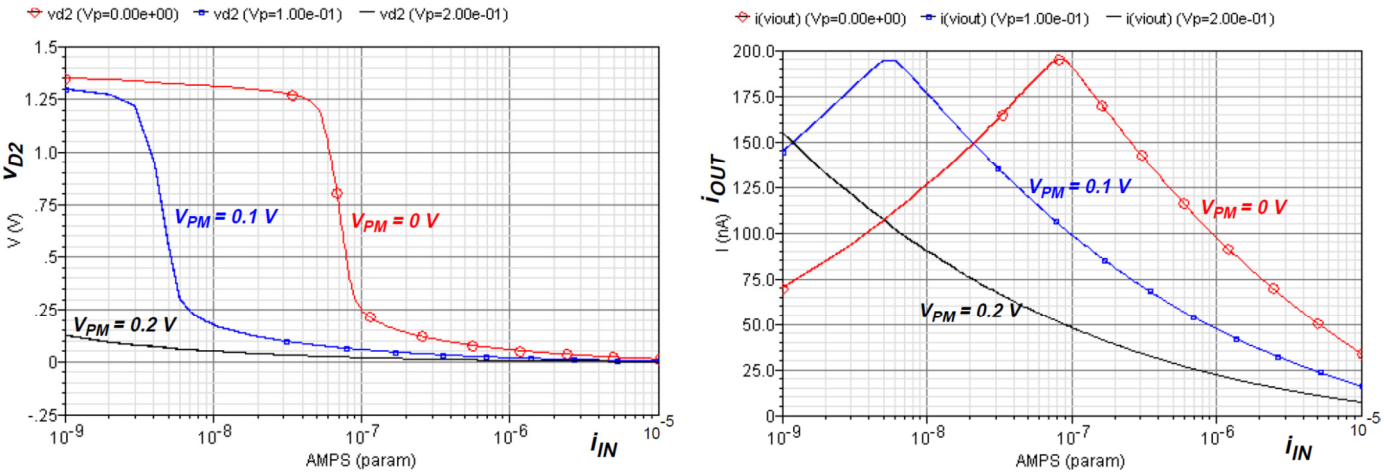

Fig. 16. DC characteristics of the circuit shown in Fig. 13. The *W/L* ratios of the transistors are specified in the right column of Table 4. The voltage v_{PM} is set at 0 V, 0.1 V and 0.2 V.

The current transfer characteristics of the nonlinear current mirrors presented in this paper are implemented by means of controlling the drain voltages of the common-gate transistor pair. In the examples presented above, this control is done by using the series PMOS-NMOS structure. It should be noted that varieties of structures can also be explored to have different ways of control in order to implement different functions.

Fig. 17 illustrates another current mirror. The sole difference between this circuit and that shown in Fig. 13 is that the transistor used to control the drain voltage v_{D1} is a NMOS, namely *N*, instead of a PMOS. The source voltage of this transistor is v_{D1}, not v_G in the previous cases. Hence, v_{D1} decreases with the increase of i_{IN}, and N_1 will likely to be in the triode mode if v_{NM} is at a relatively low level. In the lower part of the current range, if v_G is low enough to make N_2 operate in the saturation mode and P_R in the triode mode, i_N will be an "amplified" version of i_{IN} in case that N_1 and N_2 have the same *W/L* ratio. The derivative dv_G/di_{IN} can be made strong as a deeper-triode N_1 requires a much higher v_G to accommodate i_{IN}. If v_G gets too high, P_1 and P_R will be cut off, i_P, i_N and i_{OUT} will be zero. Therefore, as shown in Fig. 18, the current transfer characteristic of the circuit exhibits a point of $di_{OUT}/di_{IN} = 0$, and a much stronger derivative di_{OUT}/di_{IN} around point, compared to those found in Figs. 15 and 16. If the transistor sizes are given, the position of $di_{OUT}/di_{IN} = 0$ is determined by the gate voltage v_{NM}. The lower v_{NM} is, the lower v_{D1} and higher v_G will be, which makes the characteristic curve shift leftward, as shown in Fig. 18.

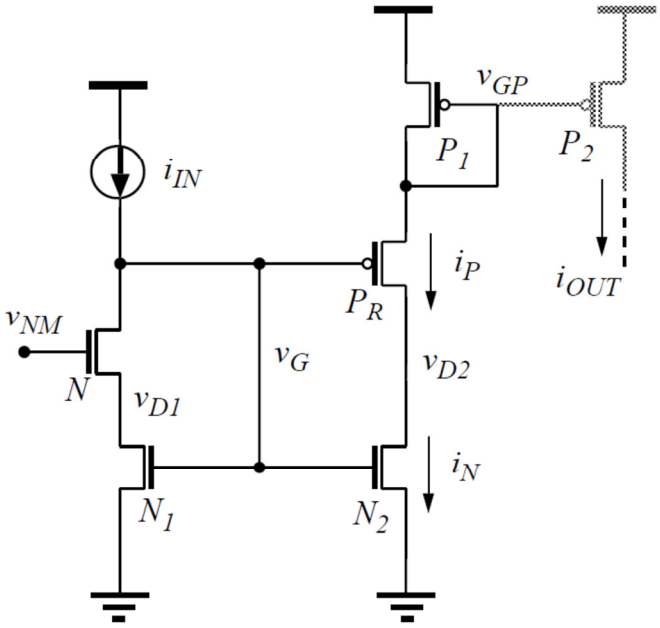

Fig. 17. Nonlinear current mirror producing strong current derivatives. The series structure of two NMOS is used in the left side of the mirror.

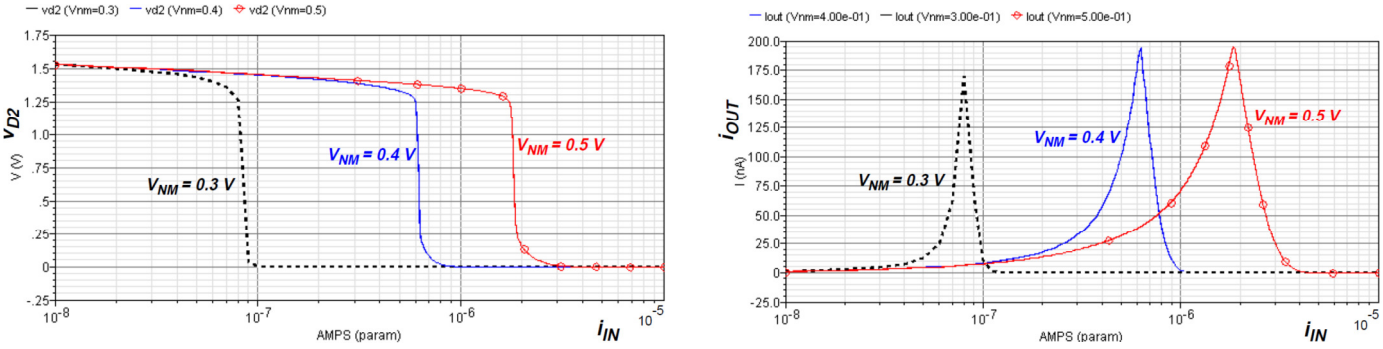

Fig. 18. DC characteristics of the circuit shown in Fig. 17. All transistors are sized as specified in the right column of Table 4, with the PMOS *P* replaced by the NMOS *N* of the same size. The voltage v_{NM} is set at 0.3 V, 0.4 V and 0.5 V.

3.5 Comments on the design examples

The design examples presented in the preceding sub-sections demonstrate how nonlinear current transfer functions can be implemented in nonlinear current mirrors by using the proposed piecewise nonlinear approach. One can have the following comments.

- In each of these examples, a sole nonlinear current mirror, with or without an additional transistor for the current output, is made to have a particularly nonlinear current transfer characteristic. The nonlinear curve is a combination of nonlinear pieces

generated by the same current mirror, instead of different circuit blocks.

- As the pieces of the curve are produced by the same transistors in different segments of the input range, there is no discontinuity from one piece to another in the nonlinear curve.
- The design examples have showed the implementation of a limited number of nonlinear functions. Based on these, one can generate more functions by combining some of them. One can also add current sources to generate other nonlinear functions. For example, combining the circuit shown in Fig. 10 with a current source producing I_{DC} can generate a V-shaped transfer characteristic, if the combination makes $I_{DC} - i_{OUT}$.
- The nonlinear functions are implemented based on the nonlinear characteristics of the transistors. They are, therefore, very sensitive to the process variations. Any change of device parameters can lead to a deviation of the current transfer characteristics. As an example, Fig. 19 shows the result of a Monte Carlo simulation of the circuit shown in Fig. 17. The dispersion of the characteristics is evident. If $I_{IN\text{-}P}$ denotes the level of i_{IN} that makes the peak of the output current, $I_{IN\text{-}P}$ can be any value between 0.84 μA and 1.6 μA. Thus, without any compensation, it is impossible to get a uniformed performance if such a current mirror is implemented in different locations of a circuit space, and it can not be used in a place where the characteristics need to be matched or the operation precision is critical. It should, however, be noted that, in case of the circuit shown in Fig. 17, as the gate voltage v_{NM} is used to shift $I_{IN\text{-}P}$, as illustrated in Fig. 18, the dispersion of $I_{IN\text{-}P}$ can be reduced by applying a signal generated by the difference between the desired value of $I_{IN\text{-}P}$ and actual one, based on which a compensation technique is currently being developed.

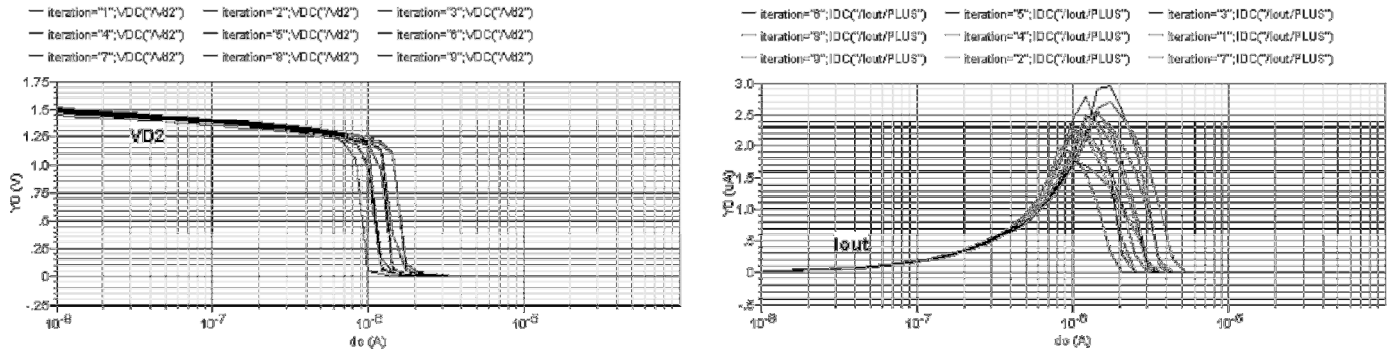

Fig. 19. Characteristics of v_{D2} versus i_{IN} and i_{OUT} versus i_{IN} of the circuit shown in Fig. 17, obtained by Monte Carlo simulation by Spectre with the device models of a 0.18 μm CMOS technology. All the transistors in the circuit are sized 0.4μm/1.5μm.

In summary, the main advantage of the nonlinear current mirror circuits designed with the proposed piecewise nonlinear approach is the simplicity that can lead to a small circuit space and thus small capacitances to achieve a high speed, with a given level of the operating currents, and low power dissipation. The quantitative performance assessment will be done in a later stage

of the design. The most notable drawback is the operation accuracy, like other analog circuits operating based on the device characteristics. Hence the development of the compensation techniques to be used to correct effectively some of the errors are in progress.

4. CONCLUSION

In this paper, a piecewise nonlinear approach to the design of nonlinear circuits has been proposed. Using this approach, the nonlinear function is implemented by means of merging nonlinear pieces of circuit characteristics given by analog blocks. The pieces are produced based on the nonlinear characteristics of the devices employed, namely MOS transistors at the present time. As the characteristic of one analog block can exhibit different nonlinearity in different sections of its input range, it is possible to use one single block to produce the multiple nonlinear pieces of a target function.

The application of this approach has so far been focused on the implementation of nonlinear current transfer functions in current mirrors. The current transfer characteristic of a current mirror has a strong dependency on the input current when at least one of the transistors employed operates out of the saturation mode. A method for controlling the operation modes of the transistors has been proposed. It is to use a series structure of two transistors and to make the drain voltage of one of them current-dependent in a desired manner by means of adjusting the current driving capacities of the two transistors. By incorporating such a structure into a current mirror, the current transfer characteristic can be changed to approximate the target nonlinear function.

Several nonlinear circuits have been designed. Each of them is based on a single current mirror, and consists of a very small number of transistors. It has been demonstrated that various nonlinear functions can be implemented in circuits of single-current-mirror. Each of the designed circuits has been simulated with the device models of a CMOS 0.18 μm technology. Although the results obtained are more “qualitative”, it has been confirmed that the proposed approach can be effectively used to design nonlinear circuits of very simple structure, which is very promising for a great facility of integration and for low-power applications.

ACKNOWLEDGMENTS

This work was supported in part by the Natural Sciences and Engineering Research Council (NSERC) of Canada and in part by the Regroupement Stratégique en Microélectronique du Québec (ReSMiQ).

REFERENCES

[1] Amin, H, Curtis, K.M., Hayes-Gill, B.R. : Piecewise linear approximation applied to nonlinear function of a neural network, IEE Proceedings - Circuits, Devices and Systems, vol. 144, no. 6, pp. 313 – 317, 1997.

[2] Chua, L. O.: Nonlinear circuits, IEEE Transactions on Circuits and Systems, vol. 31 , no. 1, pp. 69-87, 1984.

[3] Galan, J.A., Lopez-Martin, A.J., Carvajal, R.G., Ramirez-Angulo, J., Rubia-Marcos, C.: Super class-AB OTAs with adaptive biasing and dynamic output current scaling, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 54 , no. 3, pp. 449 - 457, 2007.

[4] Kronmueller, F. Zehnich, P.: Operational transconductance amplifier with a non-linear current mirror for improved slew rate, US Patent 6414552/d, July 2002.

[5] Mallory, R.E.: Nonlinear current mirror for loop-gain control, US Patent 6181142, Jan. 2001.

[6] Parodi, M., Storace, M., Julian, P.: Synthesis of multiport resistors with piecewise-linear characteristics: a mixed-signal architecture, International Journal of Circuit Theory and Applications, vol. 33, no. 4, pp. 307-319, July/August 2005.

[7] T. Poggi, A. Sciutto, and M. Storace, "Piecewise linear implementation of nonlinear dynamical systems: from theory to practice," Electronics Letters, vol. 45, no. 19, pp. 966 – 967, 2009.

[8] Tsividis, Y., McAdrew, C.: Operation and modeling of the MOS transistor, 3rd Ed., Oxford University Press, 2010.

[9] Vittoz, E.A.: Analog VLSI signal processing: Why, where, and how? Analog Integrated Circuits Signal Processing, vol. 6, pp. 27–44, July 1994.

[10] Wang, C.: Nonlinear Current Mirrors for Analog and Mixed Signal Processing, in Proc. IEEE Mid-West Symposium on Circuits and Systems, Aug. 2011.

[11] Wang, C.: A simple scheme of current amplification for sensor applications, in Proc. IEEE International Conference on Electronic Devices and Solide State Circuits, Dec. 2005, Hong Kong, pp. 647 - 650.

[12] Wang, C.: Wide-dynamic-range and high-sensitivity current-to-voltage converters, the Journal of Circuits, Systems, and Signal Processing, vol 29, no. 6, pp. 1223-1236, 2010.

[13] Wilamowski, B.M., Ferre-Pikal, E.S., Kaynak, O.: Low power, current mode CMOS circuits for synthesis of arbitrary nonlinear functions, 9th NASA Symposium on VLSI Design, 2000, pp. 7.3.1 - 7.3.8.

APPENDIX

The current transfer characteristic of i_{OUT} versus i_{IN} of the circuit shown in Fig. 10 features a positive di_{OUT}/di_{IN} in the lower part of the input range and a negative di_{OUT}/di_{IN} in the upper part. At the point $i_{IN} = I_{IN\text{-}P,}$ $di_{OUT}/di_{IN} = 0$ and i_{OUT} reaches its maximun value I_{PK}. The value of $I_{IN\text{-}P}$ can be estimated based on $i_P = i_N$ and $i_P = i_{P1}$, i_{P1} denoting the current in P_1, under the condition that all the transistors are in the saturation mode. To simplify the derivation, let us assume that N_1 and N_2 are identical, and P_1 and P_R are also so, i.e., $\beta_{N1} = \beta_{N2} = \beta_n = \mu_n C'_{ox} \frac{W_n}{L_n}$ and $\beta_{P1} = \beta_{PR} = \beta_p = \mu_p C'_{ox} \frac{W_p}{L_p}$. Also we assume that 1+ λv_{DS} is close to unity and the threshould voltage of P_1 is equal to that of P_R, i.e., $V_{t\_P1} \cong V_{t\_PR} = V_{tp}$.

If $I_{IN\text{-}P}$ is expected to be of micro-Amperes, $i_P = i_{P1}$ and P_R is in the saturation mode, we will have

$$\beta_P(v_{GP} - v_G - |V_{tp}|)^2 \approx \beta_p(V_{DD} - v_{GP} - |V_{tp}|)^2$$

$v_{GP} - v_G \approx V_{DD} - v_{GP}$, or $2v_{GP} \approx V_{DD} + v_G$

As $i_P = i_N$ and P_R and N_2 are in the saturation mode, we have

$$\beta_P(v_{GP} - v_G - |V_{tp}|)^2 \approx \beta_n(v_G - V_{tn})^2$$

$$v_{GP} - v_G - |V_{tp}| \approx \sqrt{\frac{\beta_n}{\beta_P}}(v_G - V_{tn})$$

Let $\alpha = \sqrt{\frac{\beta_n}{\beta_P}}$ and we have $2v_{GP} \approx V_{DD} + v_G$, then

V_{DD} - v_G - 2 $|V_{tp}| \approx$ $2\alpha v_G$ - $2\alpha V_{tn}$, $v_G \approx \frac{V_{DD} - 2|V_{tp}| + 2\alpha V_{tn}}{1+2\alpha}$, and $I_{IN\text{-}P}$ is given as

$$I_{IN-P} \approx \frac{\beta_n}{2}\left(\frac{V_{DD} - 2|V_{tp}| + 2\alpha V_{tn}}{1 + 2\alpha} - V_{tn}\right)^2$$

It should be noted that the simplest models for the saturation mode of MOS transistors have been used in the above derivation in order to formulate the relationship between $I_{IN\text{-}P}$ and other parameters such as V_{DD}, β_n and β_p. Thus, the result can only be used as a guideline in the design to determine approximately the level $I_{IN\text{-}P}$, not for a quantitative calculation of the value of $I_{IN\text{-}P}$, even though the transistors are in strong inversion.