COMPARISON OF TWO-LEVEL AND THREE-LEVEL NEUTRAL-POINT CLAMPED INVERTERS IN AUTOMOTIVE APPLICATIONS

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ABSTRACT

Comparison of Two-Level and Three-Level Neutral-Point Clamped Inverters in Automotive Applications

Lekha Sejpal

With the increasing popularity of multi-level inverters, the room for improvement of the performance of voltage source inverters has continuously been tested for various applications. The present project highlights the comparison of the conventional two-level inverter and the three-level Neutral-Point Clamped inverters for the application in automotive industry. The two inverters are compared for different conditions for losses, efficiency and the permissible temperature limit of operation for the non-ideal inverters that have been chosen for the application. The allowable limits of the switching frequencies for both the inverters have been discussed. The project highlights the DC-link balancing control which is the most commonly faced problem in case of a three-level Neutral-Point Clamped Inverter, with no additional circuit. Modifications of the modulation techniques for the realization of the DC-link balancing control have been proposed. Comparison of the total harmonic distortion of the line-to-line voltages at the outputs of the two and three-level inverters has been presented for both modulation techniques. The project also deals with the control of the Permanent Magnet Synchronous Motor drive using Field-Oriented Control Technique. From the detailed comparison, three-level Neutral-Point Clamped inverter has stood out as a better candidate when compared to the conventional, two-level inverter.

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Wish you were with me today, Dad!

Dedicated to Mom & Dad…

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CHAPTER 1: INTRODUCTION TO THESIS

1.1 INTRODUCTION

The present thesis project deals with the performance comparison of two and three-level inverters for the application in Permanent Magnet Synchronous Motor drive. The thesis has been divided into 5 chapters and a brief description of each chapter has been presented in what follows.

1.2 THESIS COMPONENTS

CHAPTER 1

Chapter 1 presents the most common multilevel inverters and gives a brief introduction about them. The introduction to the most basic and common topologies is intended to highlight their respective advantages and disadvantages, and also compare the performance of the topologies when compared to the conventional two-level inverter. The three-level topology to be used for the present thesis project has been selected based on the literature survey of the research papers of a few researchers who have compared (in laboratory) the basic multilevel inverter topologies with the conventional, two-level topology.

CHAPTER 2

Chapter 2 presents the modeling of the Permanent Magnet Synchronous Motor (PMSM) and this model is used to towards the PMSM drive and the associated torque equations with the chosen model will be used for the simulation purposes. The control of the PMSM for torque and speed employing the closed-loop control technique of Field-

Oriented Control (FOC) will be presented. The closed-loop control will be realized by deriving the transfer functions of the plant and the associated PI controller gains.

CHAPTER 3

Chapter 3 gives a brief description about the losses occurring in the power electronic components. The loss equations are derived from using the basic approach for both two and three-level inverters and they will be used to compare the losses occurring in the two inverters. The limitation of the temperature limits for the given cooling capability of the heat-sink will be highlighted and also the dependence of the losses and the junction temperature of the devices on the switching frequency of operation will be presented. Chapter 3 also deals with a challenge posed by the inverter topology chosen, the three-level Neutral Point Clamped Inverter. This topology is known to present unbalance across the DC-link voltage capacitors and this unbalance needs to be minimized. As one of the constraints of the present project, no additional system can be added for this control and therefore balancing should be accomplished by a control loop. Therefore, a PI controller will be developed for controlling the DC-link voltage.

CHAPTER 4

Chapter 4 highlights the need for the modification of the conventional modulation scheme for the three-level inverter in order to incorporate the balancing controller developed in Chapter 3. The Carrier-Based Space Vector Modulation approach will be used for the two-level inverter and a small modification will be proposed to incorporate the modulation scheme in the three-level inverter for which balanced voltages across the DC-link capacitors is the main criterion. The control of the DC-link capacitor voltages for

open loop operation with an RL-load will be presented. The control will also be tested for the closed-loop condition when applied in a PMSM drive. The comparison of the two inverters based on the total harmonic distortion of voltage will be presented.

CHAPTER 5

Chapter 5 presents the popular Space Vector Modulation technique for two and three-level inverters. The need for modifying the switching times in response to the control of the DC-link capacitors for the three-level inverter will be presented. Also, the three-level inverter-fed PMSM drive will be tested for closed-loop operation and its ability to control the neutral-point voltage. Comparison of voltage total harmonic distortion for two and three-level inverters based on Space Vector Modulation technique will be presented.

NOTE

The present thesis would consider the Insulated Gate Bipolar Transistor (IGBT) based inverters. The inverters that have shown in various parts of this thesis have been represented with the transistor-based switches as shown in Figure 1.1; however, they essentially represent the actual IGBT switch as shown in Figure 1.2.

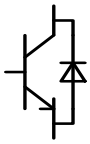


Figure 1.1: Transistor-based Switch Representing IGBT Switch

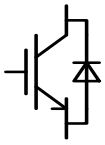


Figure 1.2: Actual IGBT Switch

1.3 INTRODUCTION TO MULTILEVEL INVERTERS

An attempt is made to present the most common multilevel (three-level) inverters and briefly describe their advantages and disadvantages based on a literature survey. The literature survey was intended to compare the inverters based on their performance aspects and the challenges and restrictions they could impose for application in the given area.

The fundamental purpose of considering multilevel inverters instead of the popular two-level inverters is due to the high value of DC-link voltage that needs to be employed in future developments. With increase in DC-link voltage, it is aimed that the performance of the inverter in use does not degrade and hence, multilevel inverter options have been considered.

The increase in power-handling capabilities of the power electronic switches has made the use of Voltage Source Inverter (VSI) feasible for high-power applications. For high voltage and high power systems, instead of using switches with high voltage ratings, it is beneficial to connect the switches having low-voltage ratings in series [1]. This would allow the latter to be switched faster than the switches having higher voltage ratings, thus resulting in switching harmonics of higher frequencies which can be filtered out easily. Due to the dynamic voltage sharing problem when the switches are connected in series, multilevel power converters have come into existence and they are being used due to several advantages that they offer over the conventional two-level converters. However, in principle, with increased DC-link voltage, there are different ways in which the semiconductor devices can be connected which can be done by:

- series connection of devices, however, dynamic voltage sharing among the devices is a big challenge
- using switching devices with higher voltage rating but it involves high $\frac{dV}{dt}$ stress and renders slower switching due to high voltage level
- adopting the multilevel solution which is more preferable due to the limited voltage ratings for the semiconductor devices

Multilevel converters can be operated at high voltages without the need for series connection of the switching devices. There are different ways in which the devices can be connected so that the dynamic voltage sharing problem posed by the series connection of the devices is no more confronted. The capability of the inverter to operate at high power level with lower harmonic distortion and lower voltage stress across the switches makes it a strong candidate for drives applications.

The features that make a multilevel converter an attractive candidate are [2]:

- Staircase waveform quality

  Multilevel inverters can generate output voltage with low distortion and reduced $\frac{dV}{dt}$ stresses, resembling a near sinusoidal waveform with increase in the number of levels.
- Switching frequency

  These inverters can be operated at both fundamental and high switching frequency pulse width modulation (PWM). Lower switching frequency would yield lower switching losses and thus improving the efficiency.

- Common-mode voltage

  In an inverter-driven A.C. machine, there exists a common-mode voltage as the VSI does not constitute an ideal balanced source. The parasitic capacitances in an A.C. motor become much relevant when this motor is driven by a PWM VSI. High $\frac{dV}{dt}$ of the common mode voltage applied across the stator and the ground of the motor (in a 3-φ, 4 wire system) causes pulsed currents (the common-mode currents) to flow through these capacitances thus producing the common-mode voltage. In multilevel inverter-fed motor drive, due to smaller $\frac{dV}{dt}$ when compared to the two-level inverter-fed drive, there is smaller common-mode voltage at the motor bearing terminals.

There are a number of multilevel converters introduced since the year 1975 but the three basic and most well-known topologies are the Cascaded H-Bridge Multilevel Converter (CHB), Neutral Point-Clamped Multilevel Converter (NPC) and the Flying Capacitor Multilevel Converter (FCC). These three basic topologies have been widely accepted for industrial applications [3].

In order to control the switches of the multilevel inverters, a number of new and modified modulation techniques have been developed [4]. These schemes include the Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), Selective Harmonic Elimination (SHE), etc. However, in literature, a number of other modified control schemes based on these basic schemes have also been proposed [5].

1.4 BASIC MULTILEVEL INVERTER TOPOLOGIES

A power electronic circuit that could operate in either inverter or rectifier mode is called a converter. Since the present project concentrates only on the inverter mode of operation of the converter, henceforth, only the term ‘inverter’ will be used.

In the case of a multilevel inverter, the DC-link constitutes more than one capacitor bank as opposed to that in a conventional, two-level inverter which consists of only one capacitor bank. The multiple DC sources formed with the series capacitors are aggregated with the commutation of the power semiconductor switches thus giving a high voltage at the output, and at the same time, each semiconductor switch has to withstand only the reduced level of voltage that appears across each capacitor. The connected DC voltage source determines the rating of the power semiconductor switches. It is difficult to connect a single power semiconductor switch directly to high voltage DC-link, as very high voltage rating of the switch has to be chosen by giving allowance to the voltage overshoot due to the stray inductances present in the semiconductor switch and the module (read as a phase leg of the inverter).

The number of levels in a multilevel inverter, in effect, can be defined as the number of levels of phase voltage with respect to the negative terminal of the inverter [6]. Therefore, in case of a two-level inverter, the output voltage with two values (levels) is generated with respect to the negative terminal of the capacitor. A brief introduction about the three basic multilevel (especially, the three-level) inverter topologies has been presented here and depending on the literature survey, the best candidate will be chosen and its detailed comparison will be made with the two-level inverter for the application in PMSM drive.

If 'm' denotes the number of steps (or, levels) of phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between the two phases of the load (or the line voltage at the load side) is denoted by 'k' which is given by

$$k = 2m + 1 \tag{1.1}$$

The number of levels in the phase voltage of a three-phase Y-connected load is denoted by 'l' which is given by

$$l = 2k - 1 \tag{1.2}$$

The above relations show that the number of steps of voltage seen by the load is increased in multilevel inverter when compared to the two-level inverter, thus providing a smoother output voltage (nearly sinusoidal) with reduced harmonic distortion.

In general, the advantages of utilizing multilevel inverters over the shortcomings of a conventional two-level inverter can be summarized as follows [7]:

- The output current of a multilevel inverter has lower distortion when compared to a two-level inverter.
- The multilevel inverter makes better utilization of the DC-bus voltage when compared to the two-level inverter.
- The smaller common-mode voltage of multilevel inverter reduces the stress in the bearings of a motor that is connected to a multilevel motor drive.
- Due to higher number of output voltage levels, the $\frac{dV}{dt}$ stress gets reduced which in-turn reduces the electromagnetic compatibility (EMC) issues.

- Multilevel inverters can be operated at fundamental as well as low or high switching frequency PWM; high switching frequency renders higher switching losses thus reducing the efficiency of the inverter.

There are a few disadvantages of multilevel inverters which can be summarized as follows:

- As the number of the required output level increases, the number of the power semiconductor switches required per phase also increases.
- Though the voltage rating of the switches required is lower than that of a two-level inverter, each switch demands a related gate drive circuit and this in turn makes the overall system more complex and expensive.

Since 1975, plentiful research has been dedicated to multilevel inverter topologies and their modulation schemes. The most promising topologies have been the cascaded H-Bridge inverter with separate DC sources, Neutral Point-Clamped (or Diode-Clamped) inverter and the Flying Capacitors (or Capacitor-Clamped) inverter.

The Cascaded H-Bridge multilevel inverter was first introduced in 1975. The idea was to connect the separate DC-sourced full-bridge cells in series so as to synthesize a staircase AC output voltage waveform. Later in 1980s, the Diode-Clamped multilevel inverter was introduced with diodes blocking the sources. It got its alternate name as Neutral-Point Clamped inverter because the mid-voltage level in three-level inverter was defined as the "neutral" point. The Capacitor-Clamped multilevel inverter was introduced in the 1990s. They possess a similar structure as that of the Diode-Clamped multilevel inverter; only that the clamping diodes are replaced by clamping capacitors. The duty of the clamping

device is to clamp the voltage level of the switch to that of the DC-link capacitors. Hence, each level in the output staircase waveform represents the voltage of each DC-link capacitor. Therefore, the aggregate of the capacitor voltages gives the output levels (or steps) in the staircase AC waveform. For applications involving high voltage and high power, it is favorable to utilize Diode-Clamped or Capacitor-Clamped multilevel inverters to replace the full-bridge cell in a Cascaded inverter so as to reduce the number of separate DC sources. Moreover, in applications with limitations in space allowance, and those demanding reduced weight, it is favorable to choose the Diode-Clamped multilevel inverter as the system would be bulky if capacitors are used for clamping purposes.

1.5 CASCADED H-BRIDGE MULTILEVEL INVERTER

In a Cascaded H-Bridge inverter, separate H-bridges are connected in series in each phase depending on the number of levels that are desired at the output. The three-phase structure of a Cascaded H-bridge inverter is shown in Figure 1.3. Separate DC sources are connected to each single-phase full-bridge inverter. The AC output of each level is then connected in series such that the overall output voltage waveform of the multilevel inverter is the sum of the individual inverter output [8].

From the knowledge of single-phase full-bridge inverters, each inverter level with V_{dc} as the DC voltage for each full-bridge can generate three different voltage outputs; $+V_{dc}$, 0 and $-V_{dc}$ and in case of the inverter represented in Figure 1.3, all the levels from $-2V_{dc}$ to $+2V_{dc}$ are present constituting 5 levels for the phase. This is made possible by connecting the DC sources (or capacitors) sequentially to the AC (output) side via the four power switches present in each cell.

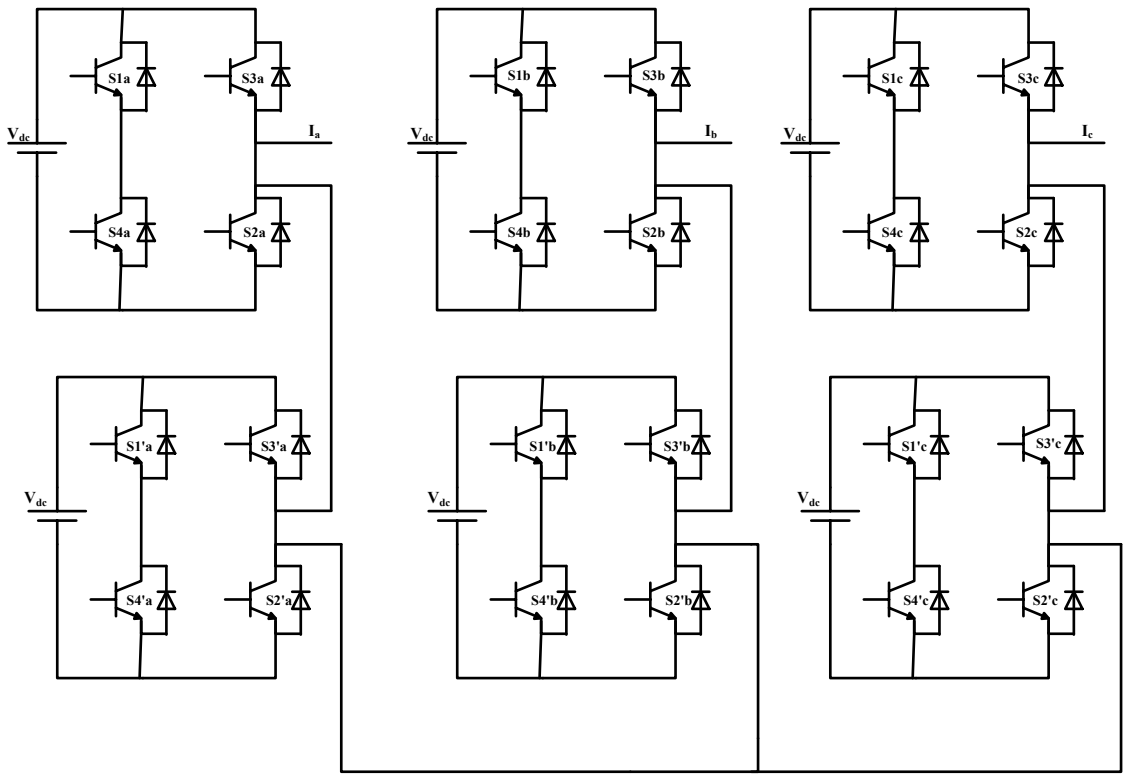


Figure 1.3: Three-phase Cascaded H-Bridge Multilevel Inverter

For an m-level cascaded inverter, the number of DC voltage sources '*s*' is related to the number of levels as

$$m = 2s + 1 \tag{1.3}$$

Cascaded inverters have been proposed for use as the main traction drive in electric vehicles where the inverter could serve as a rectifier/charger for the batteries of the vehicle when it is connected to an AC supply. For a vehicle that uses regenerative braking, this inverter can act as a rectifier.

1.5.1 ADVANTAGES

- The possible output voltage level is more than twice the number of DC sources.

- Modularity of the series H-bridges make the layout and packaging simple.

1.5.2 DISADVANTAGES

- The main restriction of a cascaded H-bridge inverter is that separate DC sources are required for each of the H-bridges thus limiting its application.
- Separation of batteries or using ultra-capacitors makes the inverter very bulky with higher levels.
- The problem of charge equalization for the separate bridges is an important issue to be taken care of.

1.6 NEUTRAL POINT-CLAMPED MULTILEVEL INVERTER

Since its proposal in 1981, this inverter has found its use in a number of industrial applications. The three-phase structure of a three-level Neutral Point-Clamped inverter is shown in Figure 1.4 [9]. The three phases of the inverter share a common DC bus. The three-level Neutral Point-Clamped inverter consists of two series-connected capacitors, C_1 and C_2. The DC-link capacitors divide the DC bus voltage into three levels; namely $+\frac{V_{dc}}{2}$, 0 and $-\frac{V_{dc}}{2}$. These voltage levels appear at the output of each phase of the inverter by appropriate switching of the power semiconductor devices. The middle point of the two capacitors is denoted as 'n' which is the neutral point. There are two complementary switch pairs (S_1, S_1') and (S_2, S_2') and two clamping diodes (D_1, D_1') per phase present in this inverter. The outer two switches are the main switching devices (S_1, S_2') that operate for pulse width modulation while the inner two switches are the auxiliary switching devices (S_2, S_1') that clamp the output terminal potential to the neutral point potential along with the help of the two clamping diodes.

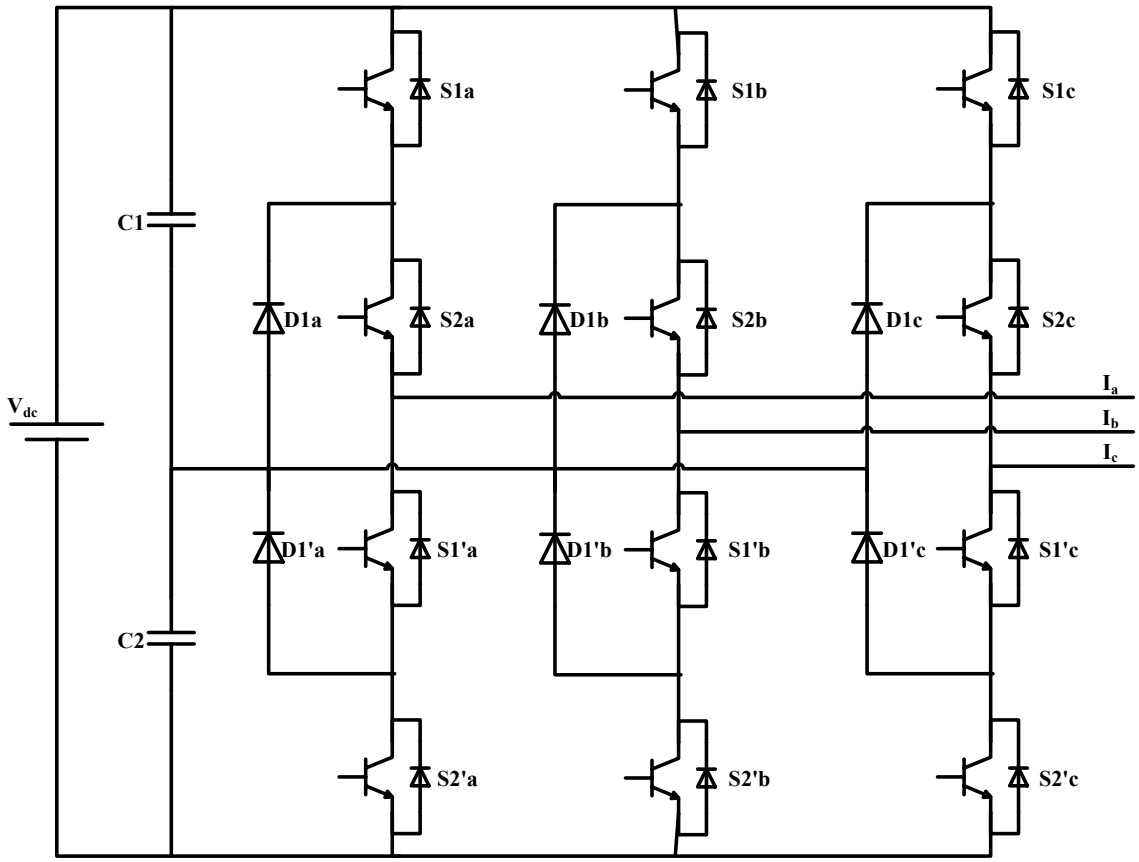


Figure 1.4: Three-phase, Three-level Neutral Point-Clamped Inverter

When both the upper switches S_1 and S_2 turn on, the voltage across 'a' (the first phase) and '0' (the negative inverter terminal), also called the pole voltage, is V_{dc}. The lower clamping diode, D_1' balances out the voltage sharing between the two lower switches, S_1' and S_2'. While the switch S_1' blocks the voltage across C_1, the switch S_2' blocks the voltage across C_2. The voltage between 'a' and '0' is the DC voltage whereas the voltage between 'a' and 'n' is the AC voltage. It is because the voltage appearing with respect to the negative inverter terminal ('0') is the voltage across each capacitor and the voltage appearing with respect to the neutral point of the inverter ('n') is the aggregate of the capacitor voltages; giving an AC waveform.

In order to obtain three levels across 'a' and 'n', there are three switch combinations as follows:

- Turn on upper switches, S_1 and S_2, in order to obtain $V_{an} = +\frac{V_{dc}}{2}$.
- Turn on middle switches, S_2 and S_1', in order to obtain $V_{an} = 0$.
- Turn on lower switches, S_1' and S_2', in order to obtain $V_{an} = -\frac{V_{dc}}{2}$.

Each power device is required to block a voltage level of $\left(\frac{V_{dc}}{m-1}\right)$ and if we assume that each blocking diode also has the same voltage rating as the active device, the number of diodes required for each phase will be $\{(m-1)\times(m-2)\}$. There is a quadratic dependency for the number of diodes with the number of levels of the multilevel inverter.

1.6.1 ADVANTAGES

- The three phases share a common DC-bus minimizing the capacitance requirements.
- The DC-link capacitors can be pre-charged, as a group.
- High efficiency for fundamental frequency switching.

1.6.2 DISADVANTAGES

- Increased number of clamping diodes.
- Neutral point control for balanced voltages across the DC-link capacitors should be achieved for all conditions of operation.

1.7 FLYING CAPACITOR MULTILEVEL INVERTER

The Flying Capacitor multilevel inverter came into existence in 1992. The three phases of the three-level Flying Capacitor inverter is shown in Figure 1.5. The three phases of the inverter share a common DC bus. Similar to the three-level Diode-Clamped multilevel inverter, the Capacitor-Clamped multilevel inverter has two series-connected capacitors, C_1 and C_2, dividing the DC bus voltage into three levels; namely $+\frac{V_{dc}}{2}$, 0 and $-\frac{V_{dc}}{2}$. These voltage levels appear at the output of each phase of the inverter by appropriate switching of the power semiconductor devices. In place of the "clamping diodes" present in the Diode-Clamped multilevel inverter, the Capacitor-Clamped multilevel inverter consists of "clamping capacitors". Each clamping capacitor clamps the device voltage to one DC-link capacitor voltage level [10].

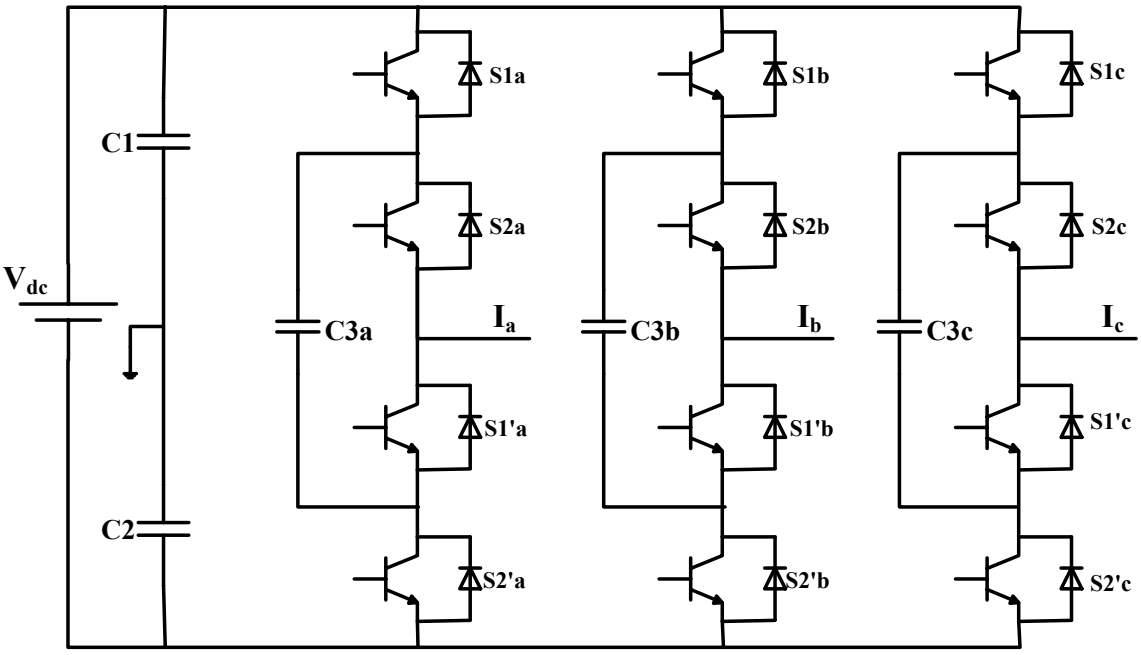


Figure 1.5: Three-phase Capacitor-Clamped Multilevel Inverter

In order to obtain three levels across 'a' and 'n', there are three switch combinations as follows:

- Turn on upper switches, S_1 and S_2, in order to obtain $V_{an} = +\frac{V_{dc}}{2}$.
- Turn on switches, (S_1, S_1') or (S_2, S_2'), in order to obtain $V_{an} = 0$.
- Turn on lower switches, S_1' and S_2', in order to obtain $V_{an} = -\frac{V_{dc}}{2}$.

During the zero output voltage, the clamping capacitor C_3 is charged when the switch pair (S_1, S_1') is turned on; and C_3 is discharged when the switch pair (S_2, S_2') is turned on.

1.7.1 ADVANTAGES

- Availability of switching redundancy for capacitor voltage balance.
- Increased number of capacitors allows the inverter to ride through short duration outages.

1.7.2 DISADVANTAGES

- Increased number of capacitors makes the system very bulky with increased losses.
- Capacitor voltage levels have to be maintained at all times; the capacitors require a separate pre-charge circuit.
- Cost increases manifold due to the increased number of capacitors in the Capacitor-Clamped topology when compared to the clamping diodes in the Diode-Clamped topology.

1.8 LITERATURE REVIEW BASED ON DETAILED ANALYSES

In [11], the authors compare the losses associated with two and three-level voltage source inverters, using Sinusoidal Pulse Width Modulation technique. The semiconductor losses and the DC-link capacitor losses were evaluated. The three-level inverters were found to have lower semiconductor losses but higher DC-link capacitor losses due to increased number of DC-link capacitors, but the lower DC-link capacitor losses of the two-level inverter cannot compensate for the increased switching losses of high voltage switches of the order of thousands of volts. However, it was concluded that the three-level Neutral Point-Clamped Inverter proved to be an efficient and promising solution. The author does not make a mention about the compensation of all the parameters, especially the gate resistance. Difference in values of the gate resistance impacts the values of the switching energies and hence it is an important factor to take into account.

In the present thesis, the loss calculations take into account the variations in all the parameters and hence the calculation is detailed.

In [12], the authors compared the cost and the power losses in the two and three-level converters. Though the cost for a two level inverter was found to be a little cheaper than a three-level Neutral Point-Clamped topology, the power losses encountered in the former topologies were much higher than the latter topology. As the Neutral Point-Clamped topology uses only one DC-bus, this topology was the one of choice among the other available multilevel topologies and also the losses are lower when compared to others. In this paper, though the author took care of the scaling factors for compensation however, the author did neglect the losses in the free-wheeling diodes considering them to be a

small fraction of the total losses. These losses change with changes in the values of the modulation indices and the power factor, so they cannot be neglected.

In the present thesis, all the losses, irrespective of small or large, occurring in all the devices have been considered.

In [13], the authors present a comparison of two-level and three-level inverters using the Space Vector Pulse Width Modulation (SVPWM) scheme for an Induction Motor Drive. The Total Harmonic Distortion (THD) analysis and the Fast Fourier Transform in the line voltage and line current for both the inverters were compared. It was concluded that the three-level inverter has higher DC-link voltage utilization and also the THD in the line voltage and line current is lesser than that in a two-level inverter for the same switching frequency of operation. The author does not address the prominent DC-link balancing issue encountered in the three-level Neutral Point Clamped Inverter.

In the present thesis, this issue is resolved by modifying the modulation strategy and by introducing a controller.

The present thesis therefore takes into account all the factors that affect the performance parameters, addressing the challenges that are faced and verifies the effectiveness of the proposed solution under various conditions.

1.9 CONCLUSION

In conclusion, as it can be seen from the results of detailed comparisons made by the various researchers all around the world, the Neutral Point-Clamped Inverter Topology stands out as the best inverter of choice for the applications in Drives providing better THD spectrum and lower losses than the conventional two-level inverter. Therefore, the

present project will be focused on the performance comparison of the conventional two-level and the Neutral Point-Clamped three-level inverter topologies.

The present thesis highlights the procedure to be followed for determining the performance parameters for the two-level and three-level inverters. The values calculated and obtained in the present work are application specific and may vary if any other component (other than mentioned) is used. In case of higher level inverters, the basic approach is similar, but not exactly the same. Certain modifications have to be done where need be.

CHAPTER 2: PERMANENT MAGNET SYNCHRONOUS MOTOR AND FIELD ORIENTED CONTROL

2.1 INTRODUCTION

The present chapter deals with the modeling of Permanent Magnet Synchronous Motor (PMSM) in the 'dq' rotating reference frame and applying this model for deriving the torque equation of the machine. The per-phase equivalent circuits with and without field-weakening are presented along with the relevant equations. Closed-loop control of Permanent Magnet Synchronous Motor with Field-Oriented Control technique is presented and the same approach has been used for the present project for the closed-loop control of the drive. The method to determine the PI controller gains for torque and speed control is presented and the same approach has been used in the further developments of this project.

2.1.1 MODELING OF PMSM IN ROTOR REFERENCE FRAME

The modeling of PMSM machine has been presented henceforth in the rotor reference frame. In a PMSM, the rotor is a permanent magnet without any windings and hence there are no equations associated with the rotor [14]. The 3-φ stationary 'abc' frame can be transformed into 2-φ synchronously rotating 'dq' frame, with the help of abc → dq transformations. The corresponding equations for abc → dq transformations can be found in Appendix. In the 'dq' frame, stator has two windings: d-axis winding and q-axis winding; and the d-axis winding is aligned with the magnetic pole axis. Consider the PMSM machine running at the speed of 'ω_r', in anti-clockwise direction, as shown in Figure 2.1.

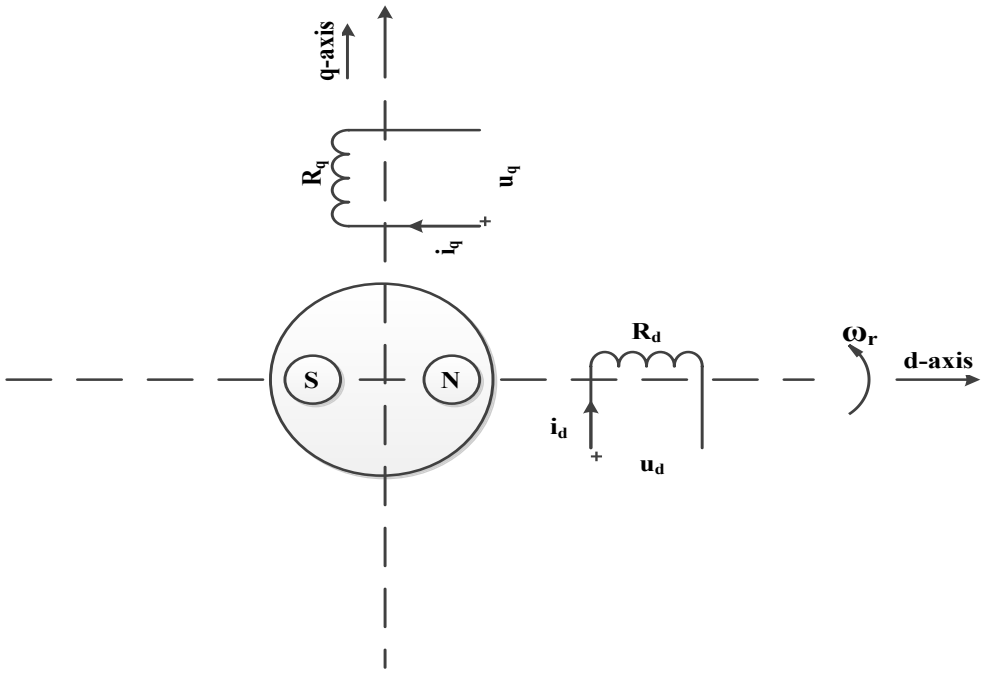


Figure 2.1: Model of PMSM in 'dq' or Rotor Reference Frame

From Figure 2.1, the voltage induced in the d-axis winding is given by:

$$u_d = R_d\, i_d + \frac{d\lambda_d}{dt} - \omega_r \lambda_q \tag{2.1}$$

where, 'R_d' and 'i_d' are the d-axis stator resistance and current

and the voltage induced in the q-axis winding is given by:

$$u_q = R_q\, i_q + \frac{d\lambda_q}{dt} + \omega_r \lambda_d \tag{2.2}$$

where, 'R_q' and 'i_q' are the q-axis stator resistance and current

The terms '$\omega_r\, \lambda_q$' and '$\omega_r\, \lambda_d$' represent the rotationally induced EMF in the stator due to the rotation of the 'dq' reference frame at the speed 'ω_r'.

where,

$$\lambda_d = L_d\, i_d + \lambda_m \tag{2.3}$$

λ_d = *flux-linkage in the d-axis stator (Wb)*

λ_m is the permanent magnet rotor flux as the d-axis is aligned along the rotor NS-magnetic axis

and,

$$\lambda_q = L_q\, i_q \tag{2.4}$$

λ_q = *flux-linkage in the q-axis stator (Wb)*

λ_m is absent in this case as there are no magnets along the q-axis

In the present study, a round rotor PMSM is considered and in this case the d-axis and q-axis inductance values are equal.

$$L_d = L_q \tag{2.5}$$

2.1.2 TORQUE EQUATION OF PERMANENT MAGNET SYNCHRONOUS MOTOR

The torque equation for PMSM [10] is given by:

$$T_e = \frac{3}{2}\frac{p}{2}\left(\lambda_d\, i_q - \lambda_q\, i_d\right) \tag{2.6}$$

Substituting for 'λ_d' and 'λ_q' in the torque equation of PMSM,

$$T_e = \frac{3}{2}\frac{p}{2}\left\{\left(L_d\, i_d + \lambda_m\right)i_q - \left(L_q\, i_q\right)i_d\right\} \tag{2.7}$$

$$T_e = \frac{3}{2}\frac{p}{2}\left\{\left(L_d - L_q\right)i_d\, i_q + \lambda_m\, i_q\right\} \tag{2.8}$$

It can be seen that the torque developed in a PMSM consists of two components given by:

Reluctance torque = $\frac{3}{2}\frac{p}{2}\left(L_d - L_q\right)i_d\, i_q$

Field torque = $\frac{3}{2}\frac{p}{2}\lambda_m\, i_q$

Since, for the round-rotor PMSM under consideration, the d and q-axes inductances values are equal, i.e., $L_d = L_q$, the reluctance torque component caused by the difference between the d-axis and q-axis inductances, gets vanished.

$$T_e = \frac{3}{2}\frac{p}{2}\lambda_m\, i_q \tag{2.9}$$

Hence the electromagnetic torque present in a round rotor permanent magnet synchronous machine is nothing but the field torque which is present due to the permanent magnet flux linkage, λ_m.

For a chosen permanent magnet synchronous machine, the number of poles (p) is constant and also the permanent magnet rotor flux-linkage (λ_m). Hence, the electromagnetic torque equation for the round-rotor PMSM can be re-written as

$$T_e = K_t\, i_q \tag{2.10}$$

where, K_t = Torque constant

$$K_t = \frac{3}{2}\frac{p}{2}\lambda_m \tag{2.11}$$

Therefore, the q-axis component of stator current is also called the torque-producing component of current.

It is known that the electro-magnetic torque of the motor should balance the torque as a result of the applied load, the viscous friction (*B*) and the moment of inertia (*J*) of the motor. Therefore, electro-magnetic torque can be expressed as:

$$T_e = T_l + B\omega_m + J\frac{d\omega_m}{dt} \tag{2.12}$$

where, $\omega_r = \frac{p}{2}\omega_m$

ω_m = mechanical speed of the rotor

ω_r = electrical speed of the rotor

The above equations can be used as the basis for modeling the transient and steady-state response of the PMSM under consideration.

When this motor is started from stalled (rest) condition and also when acceleration is required, high torque needs to be applied due to its high inertia. In order that the rotor of the machine rotates at the desired speed, appropriate acceleration is desirable. The high torque in turn will demand high in-rush current.

Once the speed starts building up from the initial condition, the initial high torque that was required can slowly be reduced once the motor has accumulated a good speed. Apart from this, by virtue of increasing speed, the back Electro-Motive Force (EMF) of the Permanent Magnet Synchronous Motor (PMSM) also starts increasing. Then, a point reaches where for a given strength of the magnetic field, or the rotor magnetic flux, a base speed is reached where the input (or the external) voltage cannot push anymore current into the electric motor against the developed back EMF of the machine. It is because the sum of the back EMF and the voltage drop across the stator impedance of the machine gets equal to the input voltage thus barring the flow of current from the output of the inverter towards the machine.

2.1.3 PER-PHASE EQUIVALENT CIRCUIT OF PERMANENT MAGNET SYNCHRONOUS MOTOR

The single-phase equivalent circuit of a permanent magnet synchronous machine [15] can be demonstrated as in Figure 2.2. The per-phase resistance (R) and per-phase inductive reactance (X_L) are shown and the Back EMF is given as E.

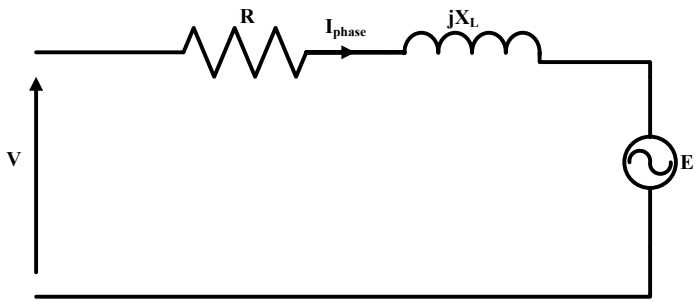


Figure 2.2: Per-phase Equivalent Circuit of a Permanent Magnet Synchronous Machine

The stator current (I) is composed of two components: the torque-producing component (I_q) and the flux-producing component (I_f) in the direction of the permanent magnet flux

of the rotor (λ). The angle between the stator phase current and the flux vector is the torque angle (δ). The power factor angle (Φ) is the angle between the terminal voltage (V) and the stator phase current.

2.1.4 PHASOR DIAGRAM OF PMSM WITHOUT FIELD-WEAKENING

The phasor diagram of the permanent magnet synchronous machine [16] can be realized as shown in Figure 2.3.

Since the voltage drop across the impedance is a function of the current, it might not be possible to further increase the current or the torque due to the limited voltage output of the inverter. In order to avoid such a situation, it is important to weaken the back EMF with increasing speed. In case of a PMSM, it is done by introducing flux-weakening wherein the rotor magnetic field is weakened in order to lower the back EMF voltage that is induced in the stator winding.

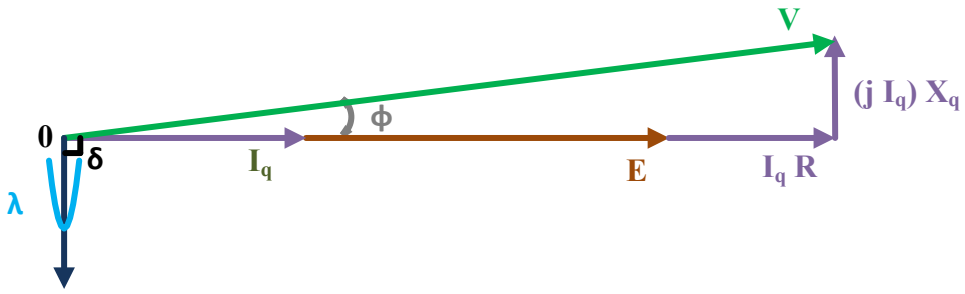


Figure 2.3: Phasor Diagram of Single-Phase of PMSM before Introducing Field-Weakening

Field weakening requires an opposing magnetic field to be applied to the permanent magnets. The fundamental approach behind flux-weakening control is to introduce and increase the magnitude of "opposing" current and employ the concept of armature

reaction (as in DC motors) so as to reduce the air-gap flux thereby reducing the effective permanent magnet flux. This approach affects the torque-component of current (and in turn, the torque) for the same value of stator current.

2.1.5 PHASOR DIAGRAM OF PMSM WITH FIELD-WEAKENING

In order to weaken this permanent magnet flux which is constant, current I_d which produces a flux, in the direction opposing the permanent magnet flux, is injected and this component of current is termed as the flux-weakening component of current (I_d). The voltage drop across the inductive reactance (jI_dX_d) opposes the direction of back EMF thus reducing its effect; as shown in the phasor diagram of Figure 2.4.

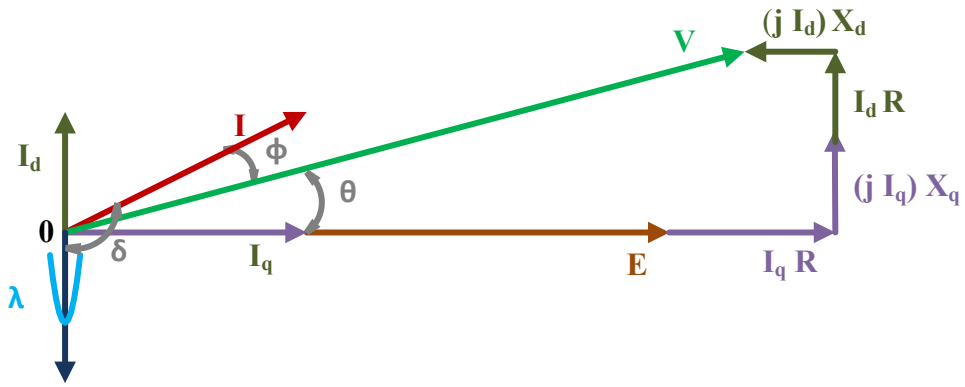


Figure 2.4: Phasor Diagram of Single-Phase of PMSM after Introducing Field-Weakening

Using the Pythagorean Theorem for the phasor diagram in Figure 2.4,

$$V^2 = \left(E + I_q R - I_d X_d\right)^2 + \left(I_d R + I_q X_q\right)^2 \tag{2.13}$$

$$V = \sqrt{\left(E + I_q R - I_d X_d\right)^2 + \left(I_d R + I_q X_q\right)^2} \tag{2.14}$$

When there is no field-weakening employed, $I_d = 0$ is substituted for Equation (2.14); and the corresponding phasor diagram is as demonstrated in Figure 2.3.

The load power factor is given by '*cos* φ' and the power factor angle 'φ' can be evaluated

$$\varphi = \delta - \theta \tag{2.15}$$

where,

θ = *the rotor angle*

When there is no field-weakening,

$$\delta = \frac{\pi}{2} \tag{2.16}$$

When field-weakening is applied,

$$\delta > \frac{\pi}{2} \tag{2.17}$$

$$\delta = \tan^{-1}\left(\frac{I_q}{I_d}\right) \tag{2.18}$$

$$\theta = \tan^{-1}\left\{\frac{\left(I_d R + I_q X_q\right)}{\left(E + I_q R - I_d X_d\right)}\right\} \tag{2.19}$$

For the same amount of output current, when a certain amount of flux-weakening component of current is injected, the torque-producing component of current decreases and thus reduces the torque requirement, as shown in Figure 2.5.

The inverter that drives the motor has limitations with respect to the voltage rating such that the stator voltage supplied to the motor from the inverter is limited by virtue of the DC-link voltage, thus limiting the speed (N) at which the motor can run; and the current rating such that the absolute value of stator current is required to be maintained below the maximum limit dictated by the maximum current rating of the inverter.

The torque-producing component of current (I_q) can be set up to the maximum limit in the normal operating range and the flux-producing component (I_d) can be set to zero to achieve maximum efficiency of PMSM. However, there is a limit on the absolute current value due to which the torque-producing current component is limited, in the field-weakening range. The limit for the torque-producing current component is given as in Equation (2.20).

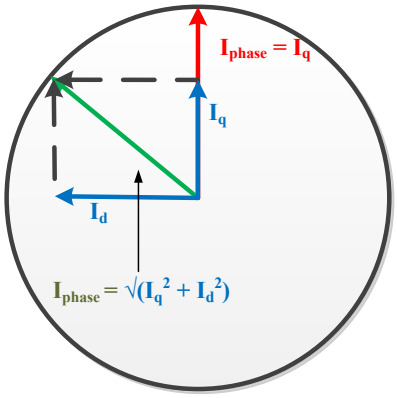


Figure 2.5: Torque and Flux-Producing Components of the Stator Phase Current

$$I_q < \sqrt{\left(I_{phase}^2 - I_d^2\right)} \tag{2.20}$$

This function can be incorporated by introducing a field-weakening controller which springs into action whenever the stator voltage approaches to exceed the maximum

voltage limit of the inverter. This controller introduces a negative value of the flux-producing component so that the above inequality is satisfied.

Flux-weakening helps weaken the constant permanent magnet rotor flux and thus allows the motor to run at an extended speed range. Up to the base speed, the motor is run at rated flux-linkage (λ) value of the rotor where V/f control is followed (as per the nomenclature, '*V*' denotes the induced EMF in the stator and '*f*' denotes the stator frequency); as speed is related to frequency as shown in equation:

$$N = \frac{120\ f}{p} \tag{2.21}$$

Alternatively, the fundamental frequency of the output voltage and current of the inverter, going into the machine can be given by:

$$f = \frac{p\ N}{120} \tag{2.22}$$

N = Speed of the machine (RPM)

f = Stator electrical frequency (Hz)

p = Number of poles

Flux-weakening can be related to the increase of speed and can be summarized as follows. Beyond the base speed, the back EMF also increases as it is a function of speed. Since the inverter is a voltage source inverter with constant DC input voltage, the inverter cannot supply enough voltage to spin the machine in motoring mode beyond the base speed, overcoming the back EMF. Hence, it is required to weaken the field flux for the

machine to be able to run in motoring mode beyond the base speed. By doing so, the back EMF is weakened for higher speed values thus resulting in the reduced V/f ratio (as the back EMF decreases and frequency increases; in-turn, speed increases). As a consequence of change in frequency, there is a proportional reduction in the torque allowing the motor to operate in constant power region. In case of constant power operation, with increasing speed, the torque has to be reduced as given as follows.

$$P = T\omega_m \tag{2.23}$$

$$E = K_e \lambda_m \omega_m \tag{2.24}$$

K_e = Back-EMF constant of the motor (V-sec/rad)

$$\omega_m = \frac{2\pi N}{60} \tag{2.25}$$

ω_m = Speed of the machine (rad/s)

Once the PMSM parameters such as the per-phase values of stator resistance (R_s) and inductance (L_s) are known, one can determine the per-phase value of the inductive reactance of the machine using the fundamental frequency value.

$$X_s = 2\pi f L_s \tag{2.26}$$

From the maximum power rating and the maximum back EMF of the machine, one can determine the maximum current rating of the machine given by:

$$P_{\max} = 3 E_{LL,\max} I_{\max} \tag{2.27}$$

From the above equation, one can obtain the maximum current value, I_{max}. Now, depending on the value of speed, one can determine the value of current for that particular speed condition. If this calculated value of phase current is greater than the maximum value of current, I_{max}, the current value is limited to I_{max}, otherwise, the obtained value of phase current is used for calculation.

For the present study, a PMSM which is used in the automotive industry with the following ratings has been considered:

Peak / Continuous Power: 100 kW / 37 kW

Peak / Continuous Torque: 180 Nm / 61 Nm

The values of the PMSM under consideration are as shown in Table 2.1.

Parameter	**Value**
R	30 mΩ
L	200 μH
p	8
λ_m	0.1 Wb
J	0.04 kgm^2
B	0.00035 Nm-s

Table 2.1: Parameters of the Permanent Magnet Synchronous Motor

For the PMSM chosen, there are two regions of operation, the transient region (at starting and during accelerations) and the permanent or continuous region (under steady-state of operation). Also, the PMSM operates in the following two speed ranges:

- Normal Range of Operation in which the speed of the motor is below its base speed. This range of operation signifies the Constant Torque condition.

- Extended Range of Operation, i.e. the Field-Weakening Range of Operation, in which the motor is required to be run beyond its base speed. This range of operation signifies the Constant Power condition.

This can be depicted as shown in Figure 2.6 and Figure 2.7, where the Transient Region and the Continuous Regions of Operation have been demonstrated respectively.

The required line-to-line voltage to run the PMSM is supplied by the inverter which switches the available DC-link voltage and provides the desired line-to-line voltage. However, in order to obtain the required value of the line-to-line voltage, it is required to switch the inverter at a modulation index which determines the amount of the peak value of output, fundamental line-to-line voltage. The modulation index is considered as the ratio of the peak line-to-line output voltage to the DC-link voltage. It can be calculated over the entire speed range for all the values of speed and torque.

Now, in order to have a controlled operation of the machine with varying speed and torque, it is required to have a closed-loop control implemented that controls the changes due to the abrupt variations or disturbances occurring in the machine.

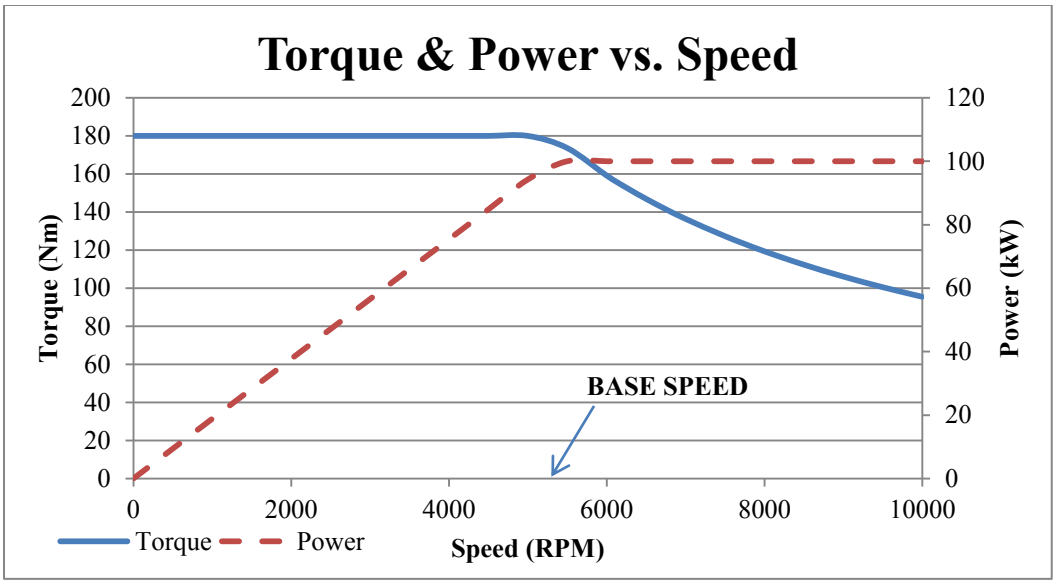


Figure 2.6: Torque & Power as a Function of Speed in the Transient Region of Operation

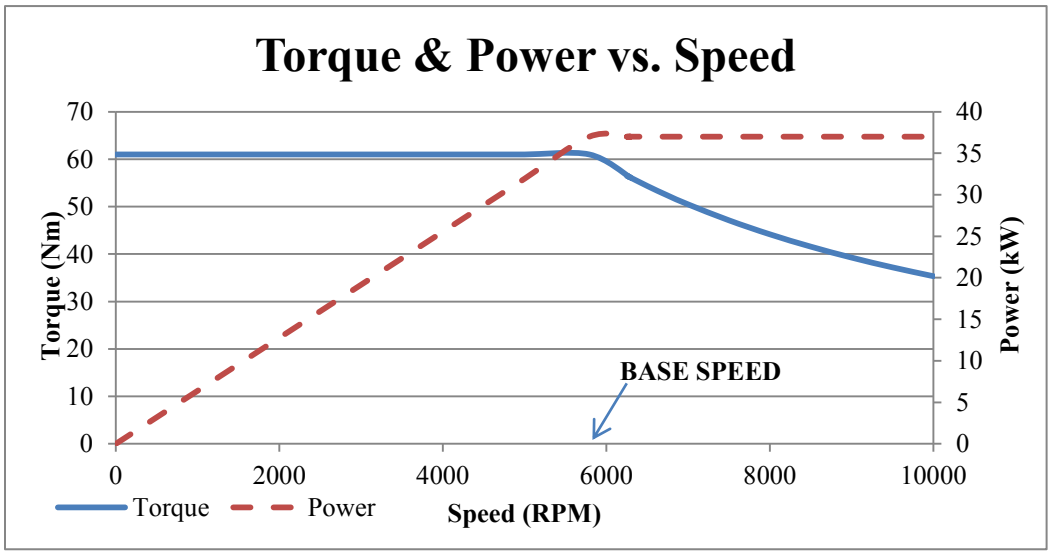


Figure 2.7: Torque & Power as a Function of Speed in the Continuous Region of Operation

2.2 CLOSED-LOOP, FIELD-ORIENTED CONTROL OF PMSM

In order to control a three-phase AC machine as a separately-excited DC machine, it is advantageous to employ Vector Control (control of magnitude and phase of the quantity

under study) which simplifies the control of the machine [17]. Vector control demands the understanding of the actual model of the machine so as to improve both the transient and steady-state performance. There are two basic and popular schemes of Vector Control, the Field-Oriented Control (FOC) and the Direct Torque Control (DTC). Though DTC presents better torque control, it presents variable switching frequency behavior which is not desirable as it presents higher switching losses [18]. Hence, FOC which presents lower switching losses with constant switching frequency of operation has been chosen to be the preferred control method in this project.

In case of the PMSM under consideration, the phase currents at the output of the inverter are sensed and are converted from the stationary 'abc' frame to the synchronously rotating 'dq' frame. The position sensor senses the angle which the 'dq' reference frame makes with respect to the 'abc' reference frame. This angle can be converted to speed using the position to speed calculator and in turn, this measured speed, which is important for cruise control, can be compared with the reference speed which one desires to obtain. The output of the speed controller gives the reference value of the current that controls the torque thereby controlling the torque component of current and also the torque. A third controller which controls the d-axis component of current governs the control of the flux, in the field-weakening region of operation for the PMSM. The output of the flux controller and the torque controller, after decoupling, represent the reference values of the 'd' and 'q' voltages. Decoupling is performed by the employed Field-Oriented Control technique. It is required to have an independent control of 'd' and 'q' axes voltages. These voltages are then transformed back into the stationary 'abc' frame in order to obtain the gating signals for the inverter under consideration.

In a vehicle, it is important to have control over torque. As an example, the accelerator pressure that is applied by the driver acts as the torque demand and the speed feedback loop is indirectly performed by the driver where he compares the speed he wants (the reference speed) with the speed that is indicated by the speedometer (the actual speed). According to the need, if the speed error is negative (when the actual speed is greater than the desired speed), the driver releases the accelerator up to the point the desired speed is achieved; and vice versa when the speed error is positive. It is easy to control the torque rapidly as the current can be changed rapidly.

The closed-loop control employing Field-Oriented Control method is depicted in Figure 2.8. The control emphasizes on speed control and torque control with the help of a speed controller, torque controller and a flux controller. Essentially, the control emphasizes on the control of ‘d’ and ‘q’ axes current and the speed. In order to design the PI controllers and to obtain the values of the proportional and integral gains, the entire system needs to be represented in terms of transfer functions.

The gains of the PI controllers for the ‘d’ and ‘q’ axes currents are the same, so one needs to calculate the gain for only one of them. When it comes to the PI speed controller, it consists of an inner current loop that controls the ‘q’ axis torque component of current, as seen from the control block diagram in Figure 2.8. The inner current control loop is desirable as it enhances the dynamic behavior of the drive and the current can be limited to a value below a given maximum value under the transient phase of operation.

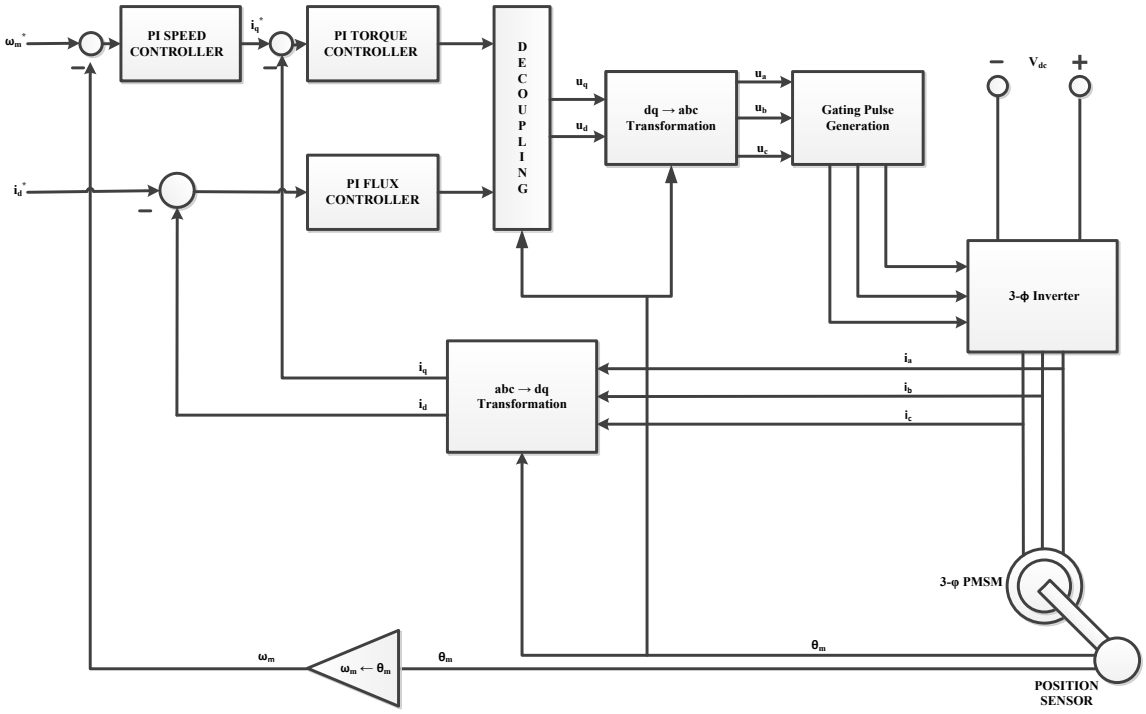


Figure 2.8: Field-Oriented Control of PMSM

In general, the entire system can be represented as in closed-loop block diagram as in Figure 2.9. The quantity that needs to be controlled is measured from the output of the motor or the plant in question. It is compared with the required, reference quantity. The error is treated through a PI controller. Now, the regulated value is sent to the inverter which in turn powers the motor.

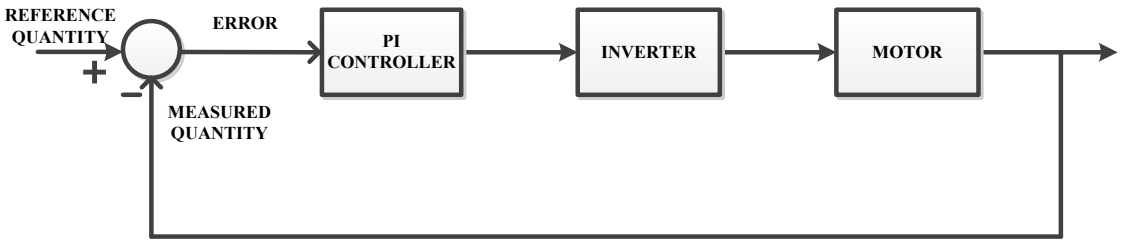


Figure 2.9: Simplified, Closed-loop Block Diagram of the System

Considering the loop that consists of the speed controller and the torque controller, or the 'q' axis current controller, one can see that there are two controllers in cascade connection. One needs to first evaluate the parameters of the inner current controller and then the inner current loop can be represented in terms of a simple transfer function when determining the parameters of the outer speed controller [19].

2.2.1 TRANSFER FUNCTION FOR CURRENT / TORQUE CONTROL

The components in the closed-loop consist of the PI current controller, the inverter and the motor as can be seen in Figure 2.10.

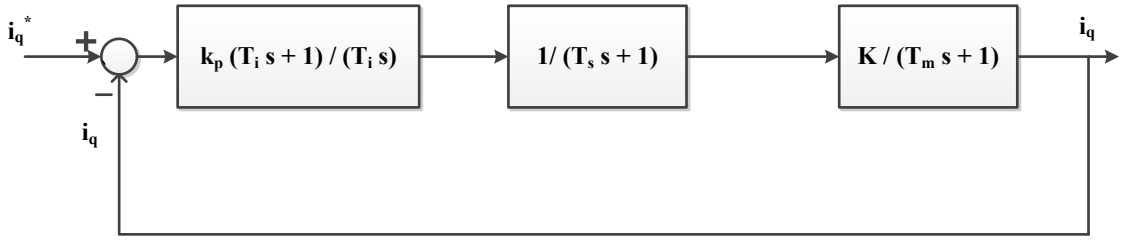


Figure 2.10: Closed-loop for Current Control

The PI controller transfer function is given as:

$$T_{f,PI}(s) = k_p + \frac{k_i}{s} \tag{2.28}$$

$$T_{f,PI}(s) = k_p \frac{(T_i\, s + 1)}{T_i\, s} \tag{2.29}$$

where k_p and k_i are the proportional and integral gains and T_i is the integral time constant of the controller.

$$T_i = \frac{k_p}{k_i} \tag{2.30}$$

The inverter is modeled as a first-order sampling delay when it is represented in terms of a transfer function.

$$T_{f,inv}(s) = \frac{1}{s T_s + 1} \tag{2.31}$$

where, T_s = sampling period = 2 μs

The output of the inverter is the voltage quantity and this voltage when applied to the motor impedance yields the current. The transfer function of the motor can be obtained from the voltage equations of the motor in the 'dq' domain and then taking the Laplace Transforms of the equations. Hence, the transfer function of the motor can be given as

$$T_{f,motor}(s) = \frac{I(s)}{V(s)} \tag{2.32}$$

$$T_{f,motor}(s) = \frac{1}{s L + R} \tag{2.33}$$

$$T_{f,motor}(s) = \frac{K}{s T_m + 1} \tag{2.34}$$

where, $K = \frac{1}{R}$ *; and,* $T_m = \frac{L}{R}$

The loop transfer function is given as:

$$LTF_{CURRENT}(s) = T_{f,PI}(s) T_{f,inv}(s) T_{f,motor}(s) \tag{2.35}$$

$$LTF_{CURRENT}(s) = \left\{ k_p \frac{s T_i + 1}{s T_i} \right\} \left\{ \frac{1}{s T_s + 1} \right\} \left\{ \frac{K}{s T_m + 1} \right\} \tag{2.36}$$

The closed-loop transfer function is required in order to make the steady-state error zero, for the system under consideration. With the pole at the origin for a PI controller, the steady-state error can be made zero if one compensates the zero of the controller with the pole of the motor transfer function with a big time constant. Big time constants render the system slow and hence in order to make the transient dynamics faster, the big time constant can be compensated with the controller zero. This can be achieved by making:

$$T_i = T_m \tag{2.37}$$

This gives the time constant of the PI controller, T_i.

Hence, the resulting loop-transfer function is given by:

$$LTF_{CURRENT}(s) = k_p\, K \frac{1}{s\, T_i} \frac{1}{s\, T_s + 1} \tag{2.38}$$

$$LTF_{CURRENT}(s) = \frac{k_p\, K}{T_i\, T_s\, s^2 + T_i\, s} \tag{2.39}$$

The final closed-loop transfer function with unity feedback can now be obtained as:

$$CLTF_{CURRENT}(s) = \frac{k_p\, K}{T_i\, T_s\, s^2 + T_i\, s + k_p\, K} \tag{2.40}$$

Using the conditions for the design of an optimum controller for a general second-order controlled system,

$$G_{CL}(s) = \frac{a_0}{a_2\, s^2 + a_1\, s + a_0} \tag{2.41}$$

In order to obtain unity value of amplitude response in the low frequency range, the condition to be fulfilled is:

$$a_1^2 = 2\,a_0\,a_2 \tag{2.42}$$

Therefore, one can obtain

$$T_i^2 = 2\,\left(k_p K\right)\left(T_i\,T_s\right) \tag{2.43}$$

$$T_i = 2\,k_p\,K\,T_s \tag{2.44}$$

$$k_p = \frac{T_i}{2\,K\,T_s} \tag{2.45}$$

In this way, one can evaluate the proportional gain (k_p) of the PI current controller.

Similarly, the integral gain (k_i) can be evaluated as:

$$k_i = \frac{k_p}{T_i} \tag{2.46}$$

Finally, the step response of the inner current-controlled, closed-loop transfer function can be obtained as shown in Figure 2.11.

2.2.2 TRANSFER FUNCTION FOR FLUX / SPEED CONTROL

In order to design the outer speed control loop, it is required to represent the inner current control loop in terms of a transfer function. Hence, the inner current loop is approximated by a first order transfer function whose time constant can be obtained as the inverse of the gain of the current loop transfer function. The closed-loop diagram for speed control can be seen in Figure 2.12.

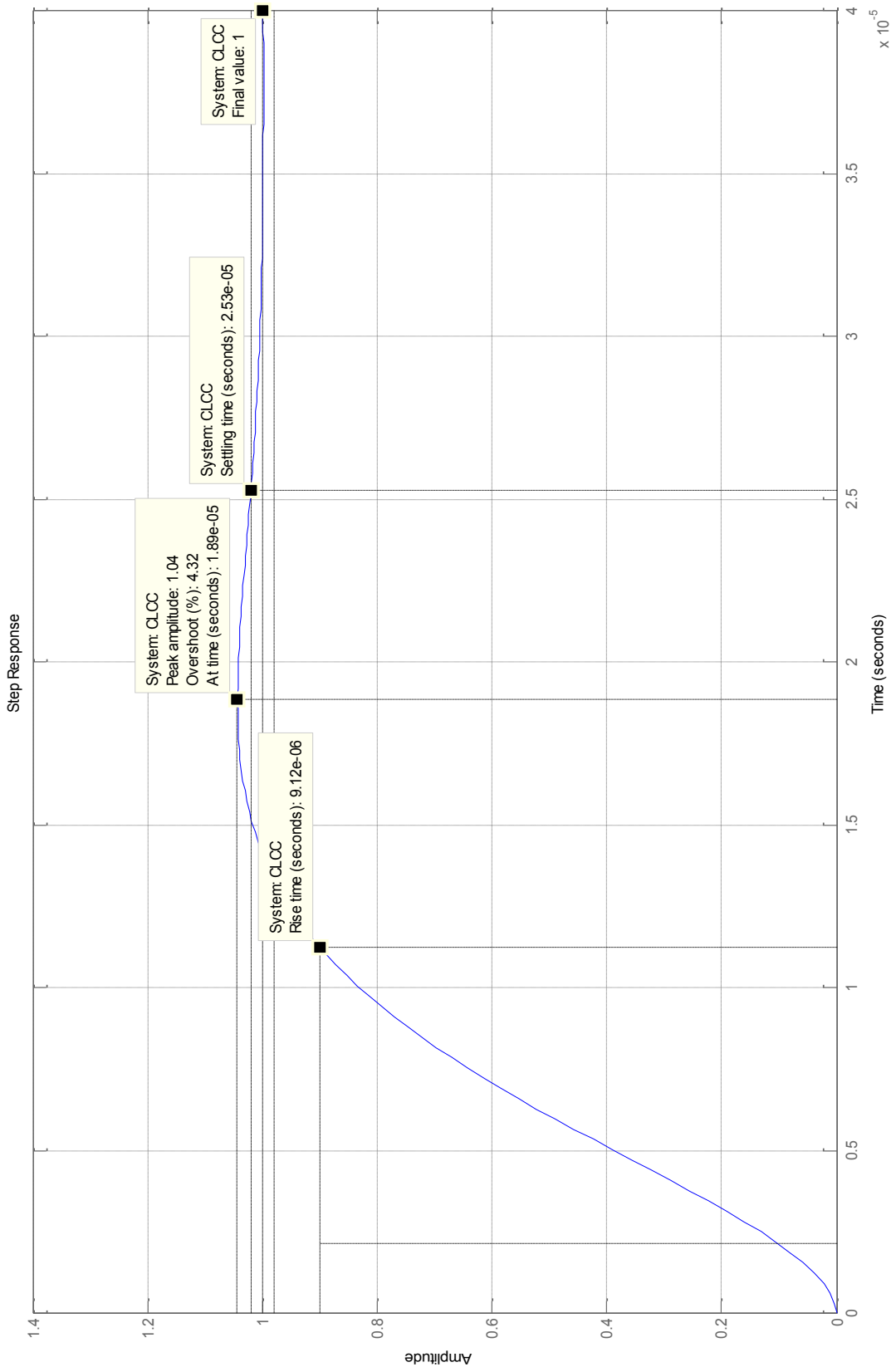


Figure 2.11: Step Response of Current for Closed-loop Operation

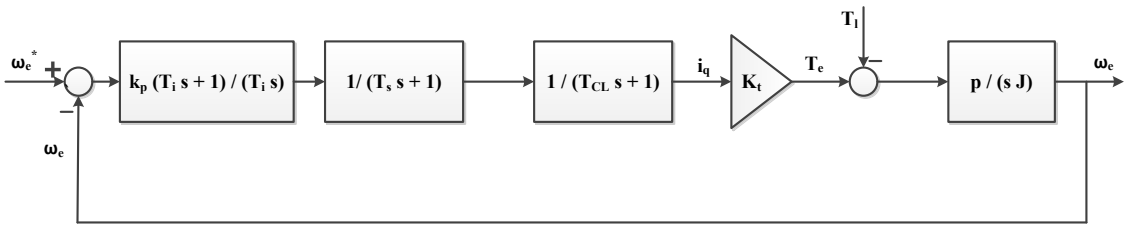


Figure 2.12: Closed-loop for Speed Control

The gain of the current loop transfer function for the present case is given by

$$G_{CURRENT} = \frac{k_p K}{T_i} \tag{2.47}$$

Since the time constant, T_{CL}, is given as the inverse of the current controller gain, $G_{CURRENT}$,

$$T_{CL} = \frac{1}{G_{CURRENT}} \tag{2.48}$$

$$T_{CL} = \frac{T_i}{k_p K} \tag{2.49}$$

Therefore, the first order transfer function approximating the current-controlled loop can be given as [19]

$$T_{f,CCL}(s) = \frac{1}{s T_{CL} + 1} \tag{2.50}$$

The motor transfer function for speed control can be obtained from the electromagnetic torque equation given by:

$$T_e = J\frac{d\omega_m}{dt} + B\omega_m + T_l \tag{2.51}$$

Taking the Laplace Transform of the above equation:

$$T_e(s) = s\,J\omega_m(s) + B\omega_m(s) + T_l(s) \tag{2.52}$$

where,

The torque developed due to viscous friction can be neglected as the coefficient of friction is very small. Hence, the torque equation can be re-written as:

$$T_e(s) = s\,J\,\omega_m(s) + T_l(s) \tag{2.53}$$

$$T_e(s) - T_l(s) = s\,J\,\omega_m(s) \tag{2.54}$$

$$\frac{\omega_m(s)}{T_e(s) - T_l(s)} = \frac{1}{s\,J} \tag{2.55}$$

Converting the mechanical speed to electrical speed,

$$\omega_r = \frac{p}{2}\omega_m \tag{2.56}$$

Hence, the equation in terms of electrical speed can be given as:

$$\frac{\omega_r(s)}{T_e(s) - T_l(s)} = \frac{p}{s\,J} \tag{2.57}$$

$$T_{f,motor}(s) = \frac{p}{s\,J} \tag{2.58}$$

Also, it is known that the electro-magnetic torque of the motor can be expressed as:

$$T_e = K_t\, i_q \tag{2.59}$$

where,

$$K_t = \frac{3}{2}\frac{p}{2}\lambda_m \tag{2.60}$$

The components in the closed-loop consist of the PI current controller, the inverter, the current-controlled loop and the motor. The loop transfer function is given as:

$$LTF_{SPEED}(s) = T_{f,PI}(s)T_{f,inv}(s)T_{f,CCL}(s)T_{f,motor}(s) \tag{2.61}$$

$$LTF_{SPEED}(s) = \left\{k_p \frac{s\,T_i + 1}{s\,T_i}\right\}\left\{\frac{1}{s\,T_s + 1}\right\}\left\{\frac{1}{s\,T_{CL} + 1}\right\}\left\{\frac{p}{s\,J}\right\} \tag{2.62}$$

The two time constants can be added together to get a simpler system:

$$T_{eq} = T_s + T_{CL} \tag{2.63}$$

$$LTF_{SPEED}(s) = \left\{k_p \frac{s\,T_i + 1}{s\,T_i}\right\}\left\{\frac{1}{s\,T_{eq} + 1}\right\}\left\{\frac{p}{s\,J}\right\} \tag{2.64}$$

$$LTF_{SPEED}(s) = \frac{k_p\, p\, T_i\, s + k_p\, p}{T_i\, T_{eq}\, J\, s^3 + T_i\, J\, s^2} \tag{2.65}$$

The closed-loop transfer function for speed with unity feedback can be obtained as follows:

$$CLTF_{SPEED}(s) = \frac{k_p\, p\, T_i\, s + k_p\, p}{T_i\, T_{eq}\, J\, s^3 + T_i\, J\, s^2 + k_p\, p\, T_i\, s + k_p\, p} \tag{2.66}$$

The speed step response can be obtained as shown in the Figure 2.13. From Figure 2.11 and Figure 2.13, it can be observed that the inner current loop is much faster than the outer speed loop and also presents a smaller overshoot.

The same approach has been used for determining the PI controller parameters for the FOC of the PMSM while testing the Closed-loop control of the drive in Chapter 4 and Chapter 5.

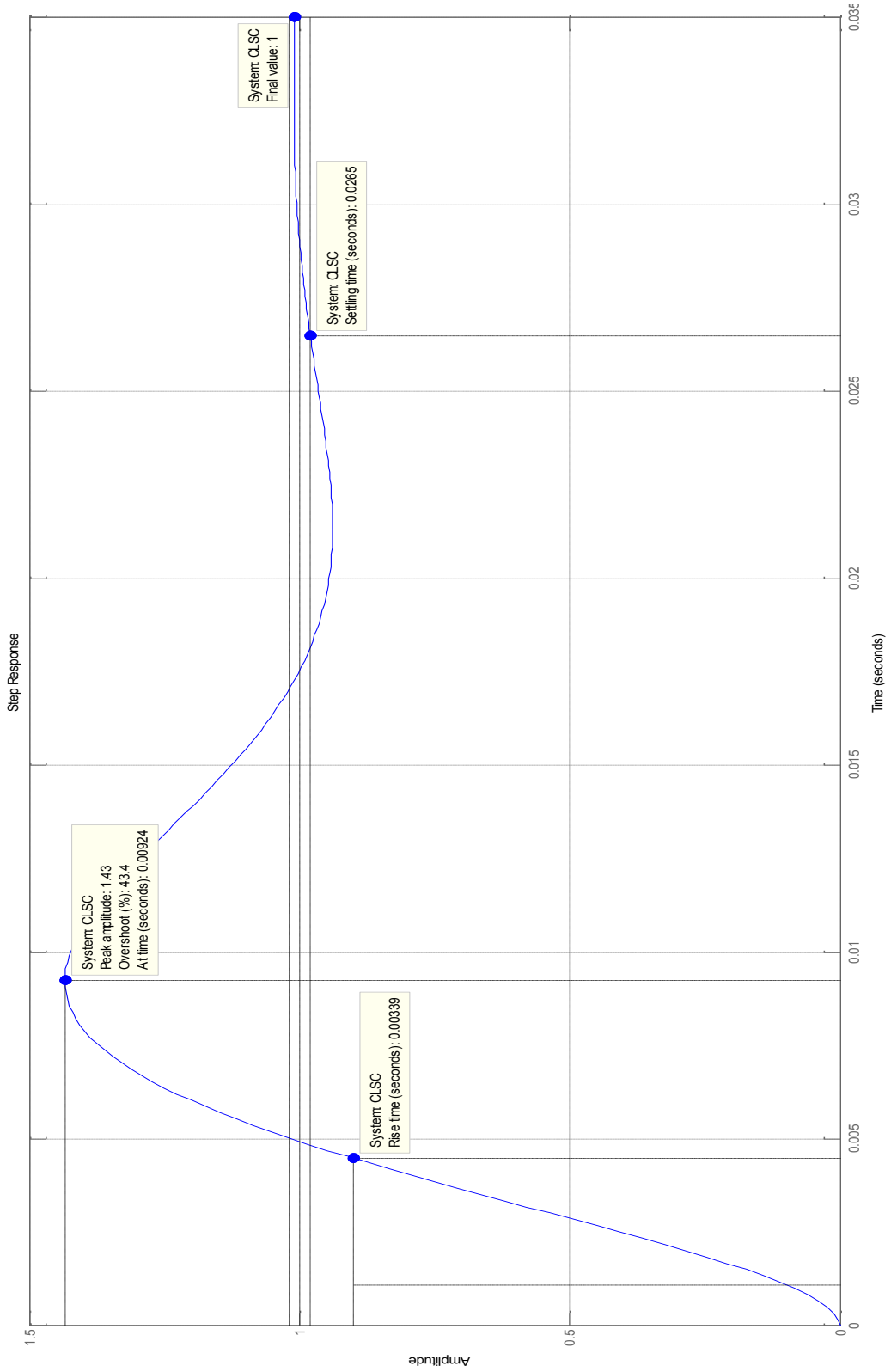


Figure 2.13: Step Response of Speed for Closed-loop Operation

CHAPTER 3: COMPARISON OF TWO AND THREE-LEVEL INVERTERS IN TERMS OF LOSSES AND EFFICIENCY

3.1 INTRODUCTION

The present chapter deals with the introduction of two-level and three-level, neutral-point clamped voltage source inverters. The importance of appropriate selection of the switches for a given DC-link voltage and a given motor to be driven has been underlined. The factors affecting the losses have been classified and the loss equations have been formulated. The losses have been calculated for a range of fundamental output frequency using the Microsoft Excel VBA Spreadsheet Tool for the chosen IGBT switch modules. The losses are calculated to determine the temperature as measure of safety for the module in terms of the acceptable temperature limits. The two- and three-level inverters have been compared in terms of losses and efficiency by switching them at an acceptable, pre-determined frequency of switching. The switching frequency is limited by the cooling capability of the coolant in use and this has a limitation on the switching frequency value. The later part of this chapter deals with the issue of DC link voltage balance in the three-level inverter. The factors influencing the neutral-point voltage shift in a three-level, neutral-point clamped inverter have been identified, listed and derived. The steps that could be taken to maintain neutral-point balance have been demonstrated and their pros and cons with respect to the requirements of the present project have been discussed.

3.2 VOLTAGE SOURCE INVERTER

The 3-φ Voltage Source Inverter (VSI) has to switch the input DC-link voltage and provide the sinusoidal fundamental component of voltage and current to the 3-φ motor, at

the output of the inverter. The magnitude and frequency of the sinusoidal output voltage of the inverter controls the speed of the machine that is driven. In the present study, conventional two-level inverter and three-level Neutral Point-Clamped inverter will be considered.

3.2.1 TWO-LEVEL INVERTER

The conventional two-level inverter with a 3-φ PMSM is depicted as shown in Figure 3.1.

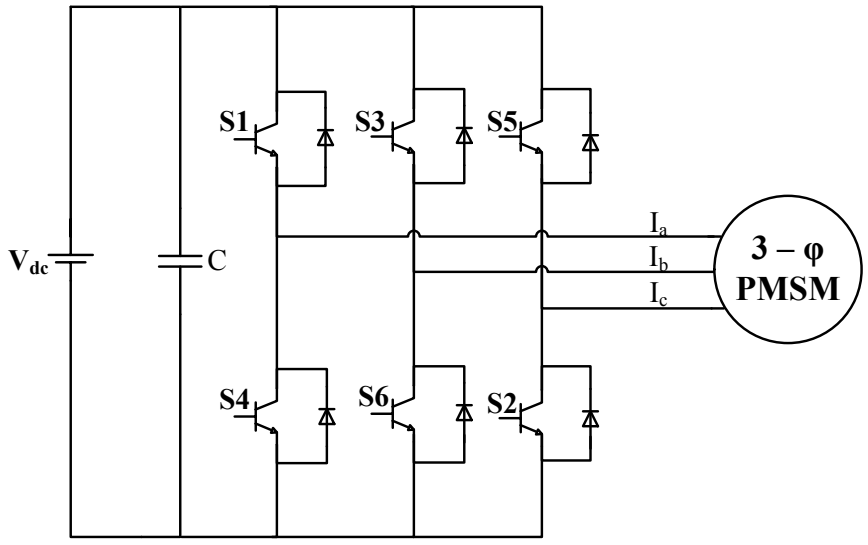


Figure 3.1: Conventional, Two-level Inverter

There are two switches per-phase in a conventional, two-level inverter; and the DC-link capacitor acts as a filter.

3.2.2 THREE-LEVEL INVERTER

The three-level Neutral Point-Clamped inverter with a 3-φ PMSM is depicted as shown in Figure 3.2. There are four switching devices, in this case IGBT's, per phase in a three-level Neutral Point-Clamped inverter and the blocking voltage per switch required in case

of a three-level inverter is halved when compared to a two-level inverter. Henceforth, in this thesis, a three-level inverter would represent a three-level Neutral Point-Clamped inverter. Each phase has a pair of clamping diodes by virtue of which the DC-bus voltage can be increased beyond the voltage rating of each switch.

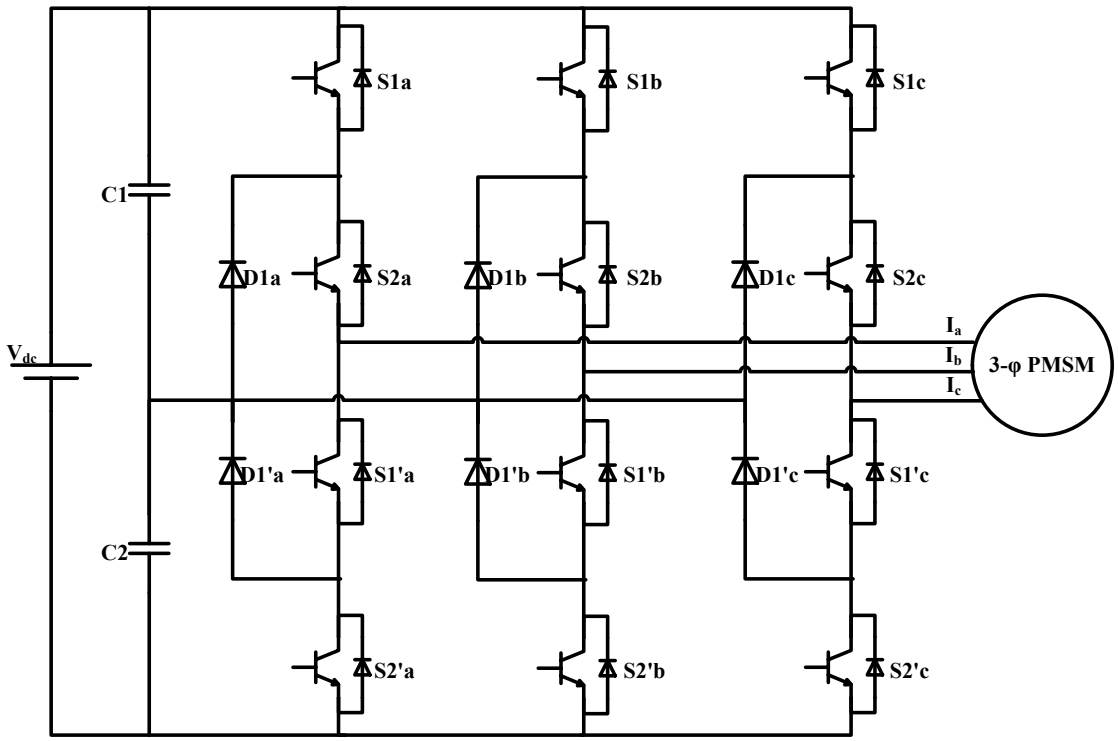


Figure 3.2: Three-level Neutral Point-Clamped Inverter

3.3 IMPORTANCE OF JUNCTION TEMPERATURE LIMIT

The inverter consists of semiconductor switching devices that are responsible for switching the DC-bus voltage and for the commutation of the current. In a practical scenario, unlike in a general simulation environment where one considers and assumes a lot of ideal conditions, the semiconductor devices do get heated up and there is a need to control the internal temperature of the power electronic component that is in use. It is

because excessive internal temperatures may prove detrimental to all the power electronic components, and the inverter as a whole, and eventually for the entire system that is connected to this inverter, therefore it is in the favour of the entire system that the junction temperatures of the semiconductor devices not be exceeded in any phase of operating condition. If the intrinsic temperature (the internal temperature of the semiconductor device at which the intrinsic carrier density in the most lightly doped region of the semiconductor device equals the majority carrier doping density in that region) is exceeded, the rectifying characteristics of the junction are lost because the intrinsic carrier density greatly exceeds the doping density and the depletion region that gives rise to the potential barrier is shorted out by the intrinsic carriers [20].

With increase in current, the power dissipation in the power electronic component increases and also the junction temperature of the device increases. Therefore, when designing and estimating the losses, it is always preferable to take into account the worst-case condition and hence estimate the losses. Beyond the acceptable temperature of operation, the device may fail and eventually crash the entire system that is associated with it.

When it comes to the industrial application of a device, not only the electrical properties but also the mechanical and thermal properties of the devices have to be taken into account so as not to exceed the acceptable operating conditions.

A power electronic device (or more simply, a switch) is mounted on a multiple layer structure in order to provide cooling throughout its operation lifetime. The layers of the structure are maintained at different temperatures by virtue of which there is net flow of

energy from the layer that has a higher temperature towards the one with a lower temperature . The temperature difference created between two successive layers for a unit power loss (that is, the unit flow of energy per unit time) is defined as the thermal resistance, R_{th}, between the layers under consideration.

$$R_{th} = \frac{\Delta T}{P_{loss}} \tag{3.1}$$

Different layers having different cross-sectional areas (A) and thicknesses (d) with differing thermal conductivities (λ) will have different values of thermal resistances between them.

$$R_{th} = \frac{d}{\lambda A} \tag{3.2}$$

As can be seen in Figure 3.3, each module (or one leg) of the 3-φ inverter is enclosed in a separate case and all the three cases are mounted on a common heat-sink. Considering the cooling method adopted (liquid cooling in this case), the tubes for circulation of cooling liquid are present at the side of the heat-sink base. The heat-sink has a greater area in order to allow faster dissipation of heat.

Allowed number of switching of a power electronic device is limited by power dissipation. The number of switching in a period is nothing but the frequency of switching or, more commonly, the switching frequency of the power electronic device. Since all the devices contained in one phase leg are fabricated and packaged in one container, the container is commonly described as a module.

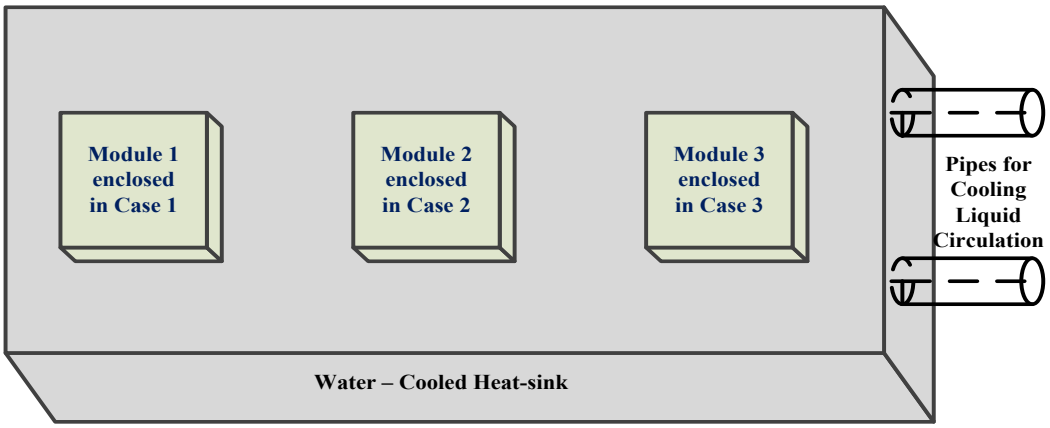


Figure 3.3: Multiple Layer Structure for a Liquid-Cooled Power Electronic Converter System

3.3.1 THERMAL EQUIVALENT CIRCUITS FOR TWO AND THREE-LEVEL INVERTERS

The temperature rise occurring in a device is a result of the losses (to be dealt with, in the subsequent sections) occurring in the device and the junction temperature of the device is cumulative of the all the losses and resulting temperature rise across the thermal resistances that are present in the path of the junction to the cooling medium.

$$T_j = T_{liquid} + P_{loss} \sum R_{th} \tag{3.3}$$

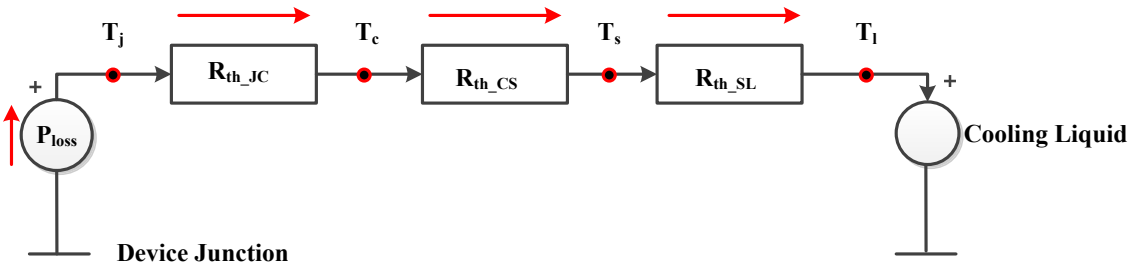


Figure 3.4: Electrical Equivalent of the Thermal Circuit of a Liquid-Cooled Semiconductor Device

The more detailed equivalent circuit emphasizing only one case, or one module, shown in Figure 3.3 has been drawn in Figure 3.5, for a two-level inverter, and in Figure 3.6, for a three-level inverter, respectively. Their electrical equivalents of the thermal circuits have been elaborated showing the respective thermal resistances. However, three such cases will be mounted on the common heat-sink during analysis and application, in case of each 3-φ inverter structure.

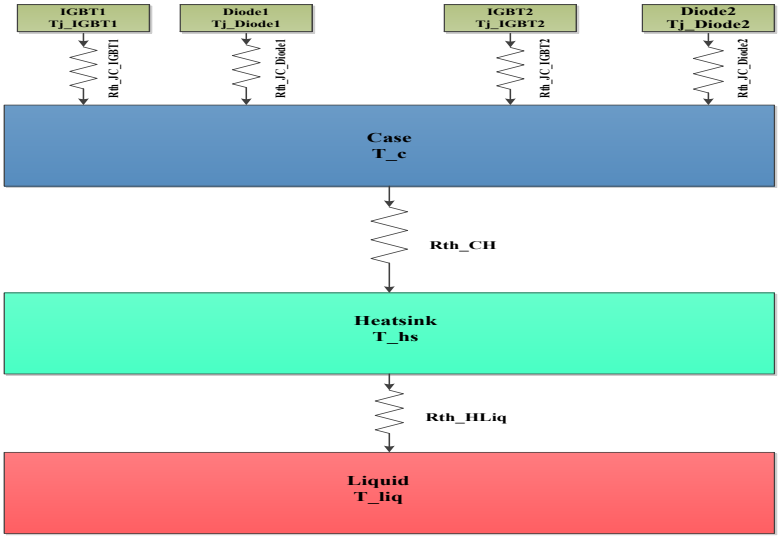


Figure 3.5: Thermal Equivalent Circuit for One Module of Two-Level Inverter

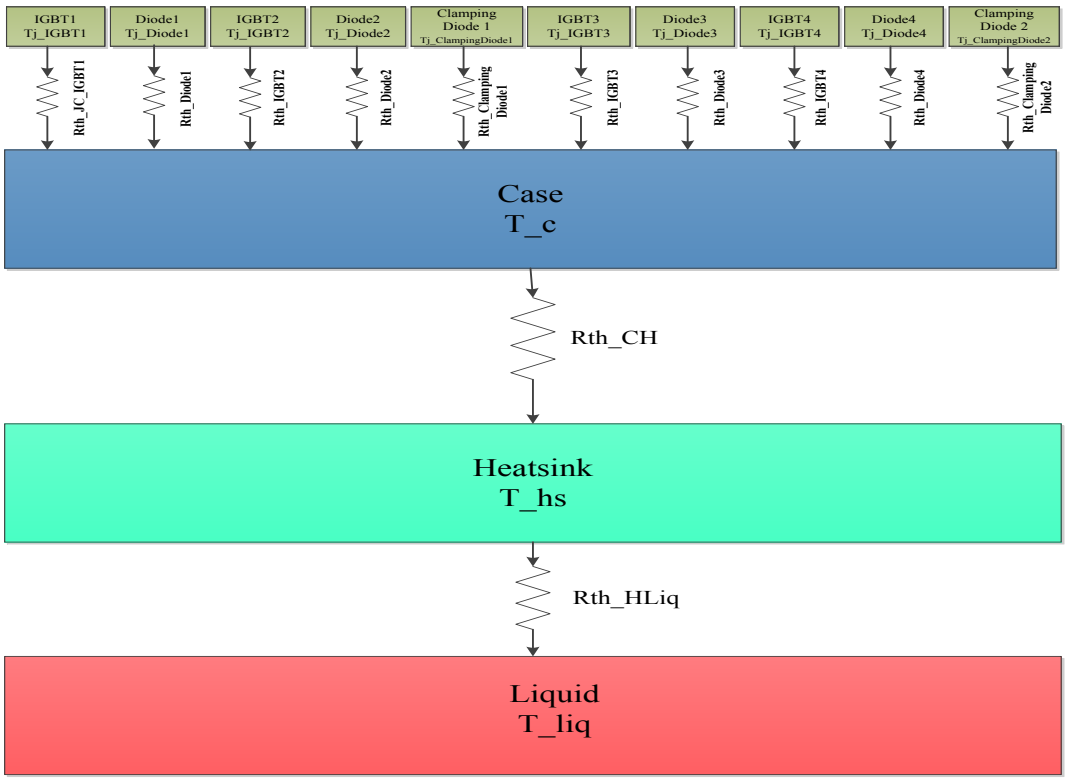


Figure 3.6: Thermal Equivalent Circuit for One Module of Three-level NPC Inverter

From Figure 3.5 and Figure 3.6, it can be seen that the junction temperature of each device can be computed as:

$$T_{jx} = T_{liquid} + \left(P_{tot,1\_case} R_{th\_HLiq}\right) + \left(P_{tot,1\_case} R_{th\_CH}\right) + \left(P_{tot,x} R_{th\_JC}\right) \qquad (3.4)$$

where,

T_{jx} = *Junction temperature of the device under consideration*

T_{liquid} = *Cooling liquid temperature*

R_{th_HLiq} = *Thermal resistance between the heat-sink and the cooling liquid*

R_{th_CH} = *Thermal resistance between the case and heat-sink*

R_{th_JC} = *Thermal resistance between the junction of the device and the case*

$P_{tot,1\_case}$ = *Total losses from all the devices in one case/module*

$P_{tot,x}$ = *Switching and conduction losses occurring in the device considered*

By keeping the above mentioned points in view, it is of utmost importance that the junction temperature of all the devices under operation during any phase of operation be maintained within the allowable limits, decided by the cooling capability of the cooling liquid in use. In terms of comparison of two- and three-level inverters, in order to have a fair comparison, it is necessary to consider the heat-sinks that have similar dimensions.

3.4 FACTORS GOVERNING LOSSES IN IGBT AND DIODE

In Power Electronics, both IGBT's and Diodes are operated as switches and they are subjected to various static and dynamic states in cycles [21]. Power and energy dissipation take place in these states thus heating the associated device. Since it has to be ensured that the junction temperature of the device is not exceeded beyond the maximum value, the losses that cause the increase in temperature have to be limited for each device. In order to limit the losses, the factors that are associated with the losses, which we will see in a short while, have to be properly taken care of.

The total losses occurring inside a power electronic switch can be categorized into three types, namely: static losses, dynamic losses and driving losses. Moreover, the static losses can be further classified as on-state losses and forward blocking losses, whereas, the dynamic (or switching) losses can be classified as turn-on and turn-off losses. The major share of the losses account for the on-state losses and the turn-on and turn-off losses; the losses comprising blocking (with negligibly small leakage current during the

off-state) and driving losses account for a negligible share and can be ignored. This is depicted in Figure 3.7.

Once the losses are classified, the factors that affect the losses which cannot be neglected have to be understood. Therefore for any power electronic switch comprising this inverter, be it IGBT or be it the diode, Figure 3.8 helps summarize the factors that influence the concerning losses.

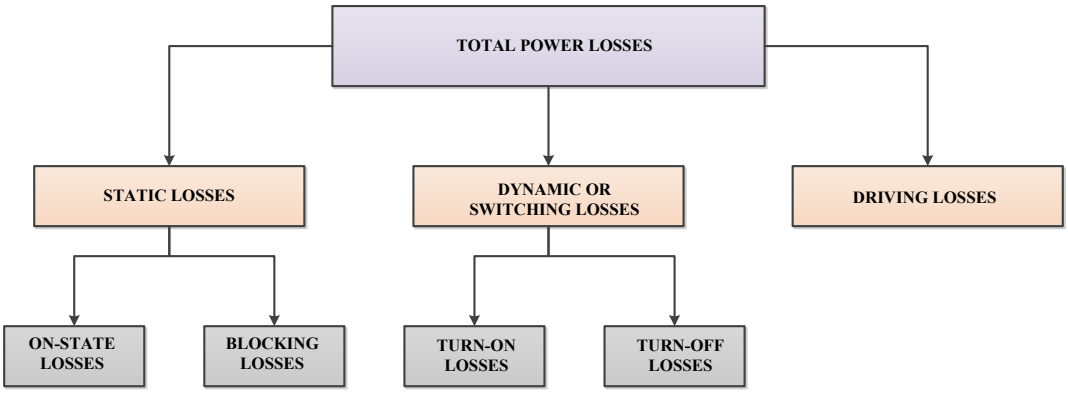


Figure 3.7: Losses Associated with a Power Electronic Switch

The technical information, or rather the information describing the behavior of the device that is provided with regard to the IGBT and the diode has to be considered from the datasheet of the IGBT module chosen.

For any switching device, the total losses are expressed as the sum of conduction (P_{cond}) and switching (P_{sw}) losses.

$$P_{loss} = P_{cond} + P_{sw} \tag{3.5}$$

The losses that occur when the power device is in the on-state and conducting the current are known as conduction losses. Since power loss is a product of voltage across the device and the current flowing through it, the conduction power loss of the IGBT or the Diode in their on-states is computed by multiplying the on-state voltage drop across the device with the load current flowing through device.

The saturation voltage which is a function of the current flowing through the device can be approximated as a linear function given by:

$$v_x = V_{x0} + i_x R_x \tag{3.6}$$

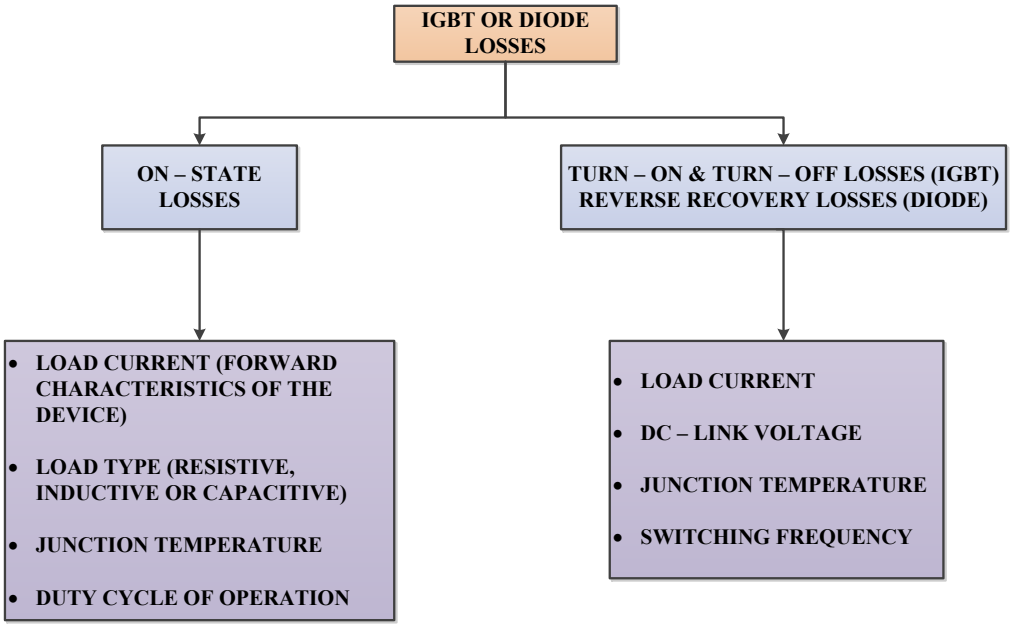


Figure 3.8: Summary of Factors Influencing the Losses

where,

v_x = *on-state voltage-drop of the device*

V_{x0} = *threshold voltage of the device*

i_x = *current through the device*

R_x = *device resistance*

Therefore, conduction loss of the device can be computed as:

$$P_{cond} = v_x \, i_x \tag{3.7}$$

The losses that take place during the turn-on and turn-off switching transitions of the device are termed as the switching losses. The switching losses play a significant role in high-frequency PWM and these losses contribute to a large extent for the temperature rise in the device. The switching energy is not a linear function of the device current, but it can be approximated as a second-order polynomial function given by:

$$E_{on/off,x} = a\, i_x^2 + b\, i_x + c \tag{3.8}$$

Referring to an IGBT datasheet, it can be noticed that the switching (turn-on and turn-off) energy is a function of gate resistance. It is because the gate current is dependent on the gate resistance value and once the IGBT undergoes switching, depending on the value of gate current, or the gate resistance; the switching energy value is affected. Therefore, after choosing a suitable IGBT module, it is necessary to determine the turn-on and turn-off switching energies for the gate resistance values employed at turn-on and turn-off respectively.

In order to obtain the forward threshold voltage and the on-state resistance of the device, the device characteristics given in the datasheet can be replicated by plotting the forward characteristics versus the device current graph. The switching energies versus the gate

resistance graphs can also be plotted and the curve-fit equations can obtained in order to obtain the switching energy values corresponding to the gate resistance values used. Alternatively, one can also plot the switching energies versus the device current graph and obtain the curve-fitting equations. Then the appropriate value of the switching energy for a certain value of device current can be obtained using the curve-fit equation and a scaling factor given by the quotient of the employed gate resistor value and the datasheet gate resistor value (Gate Resistance Value employed / Gate Resistance Value employed in datasheet) has to be multiplied so as to obtain the correct value of the switching energies. In case of the forward characteristics, only the linear region or the active region of the device is considered and the saturation region is neglected as the device is not supposed to go into saturation. Also, the switching energies versus the gate resistance graphs, the characteristics are assumed to be linear. However, in case of the switching energies versus the device current, the characteristics are assumed to have a non-linear variation.

3.5 DETERMINATION OF MODULATION INDICES FOR TWO AND THREE-LEVEL INVERTER WITH SPWM

In order to determine which IGBT or diode is active during the operation, an RL-load is considered for which the load current lags the load voltage by the power factor with a power factor angle of ‘φ’ radians; under steady-state conditions. In Figure 3.9, it can be seen that for an inductive load, the current lags the voltage. We can divide the fundamental cycle of operation into four regions; namely, 1, 2, 3 and 4.

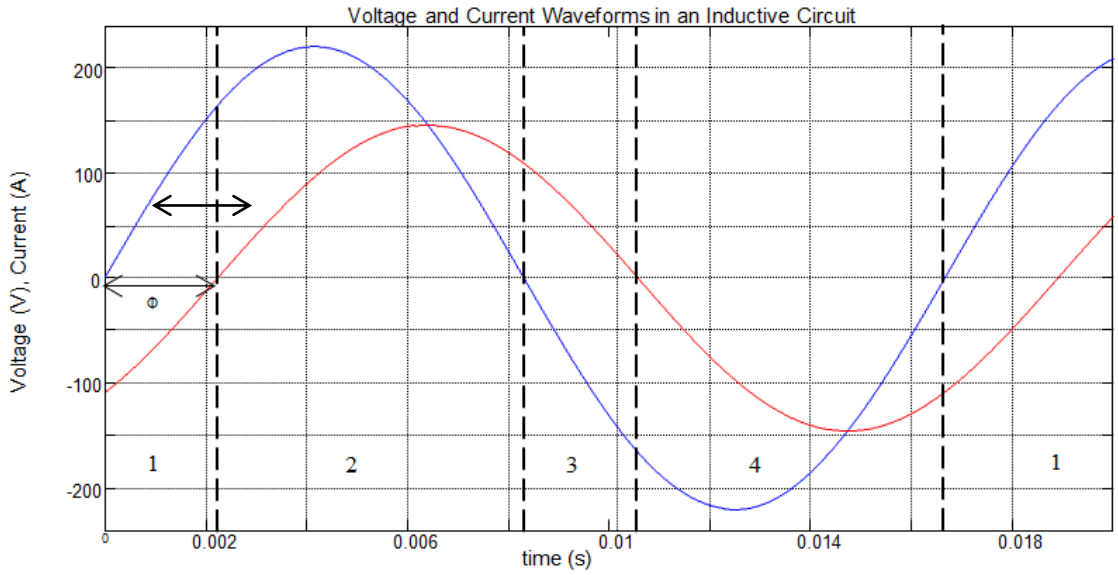
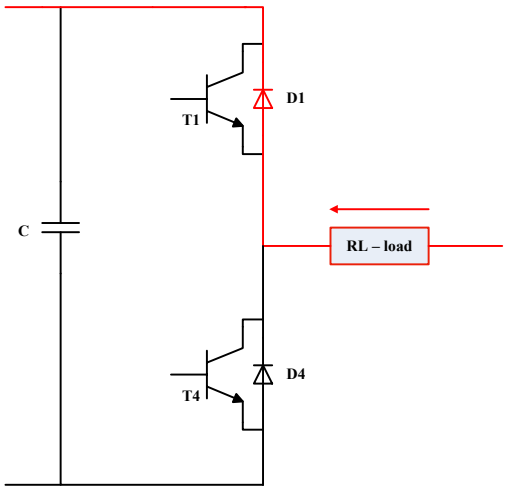


Figure 3.9: Steady-State, Load Voltage and Load Current Waveforms for an Arbitrary RL-load

For all the four regions of operation, the devices that are active are demonstrated graphically in the following figures from Figure 3.10 through Figure 3.13 for a two-level inverter.



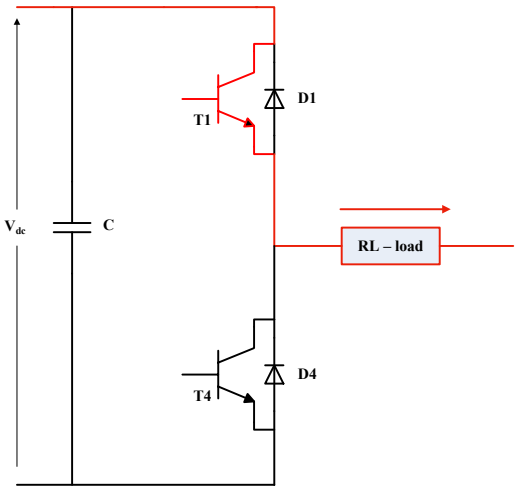


Figure 3.10: Region 1- V > 0 & I < 0 ; Figure 3.11: Region 2 - V > 0 & I > 0

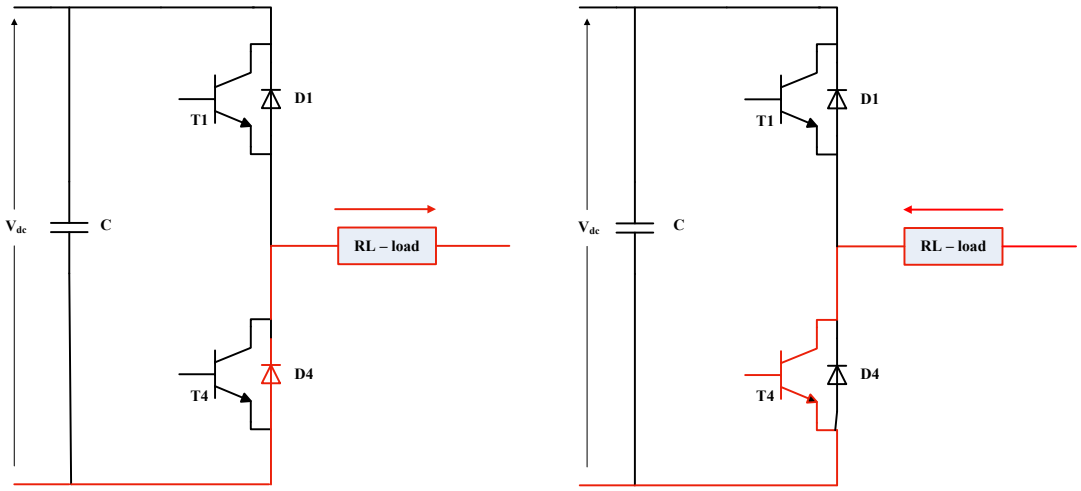


Figure 3.12: Region 3 - V < 0 & I > 0 ; Figure 3.13: Region 4 - V < 0 & I < 0

Similarly, for all the four regions of operation, the devices that are active in a three-level inverter are demonstrated graphically in the figures from Figure 3.14 through Figure 3.17.

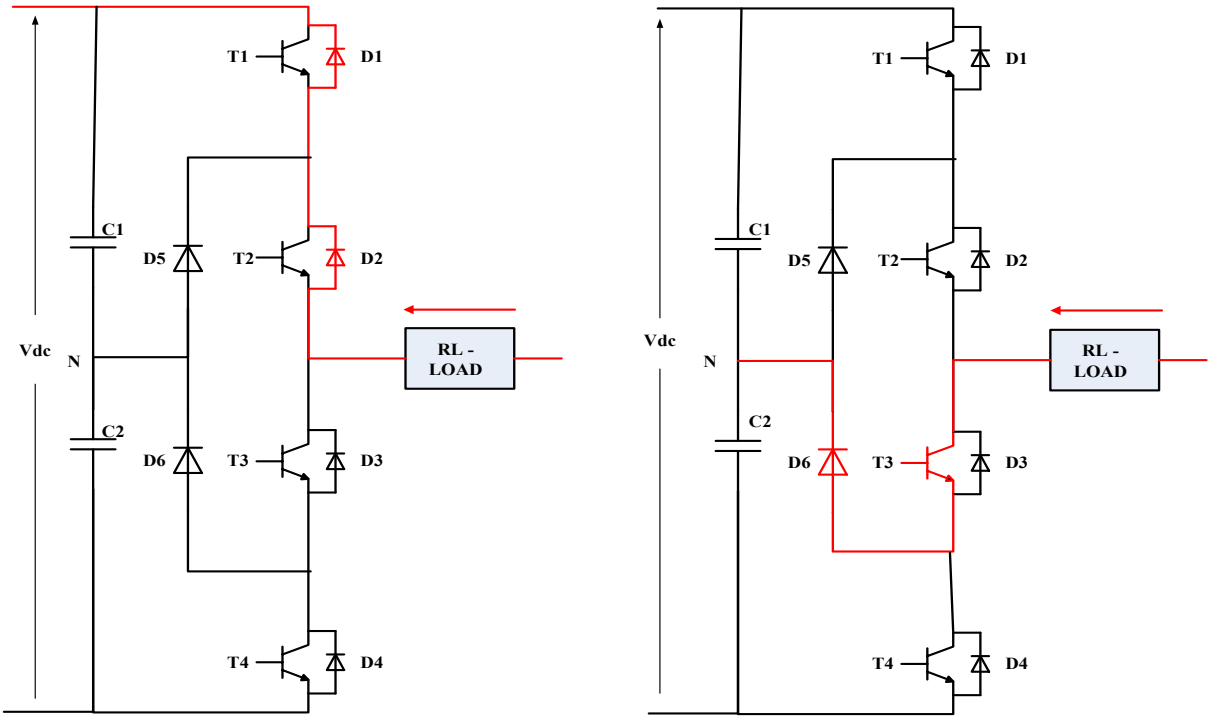


Figure 3.14: Region 1 - V > 0 & I < 0

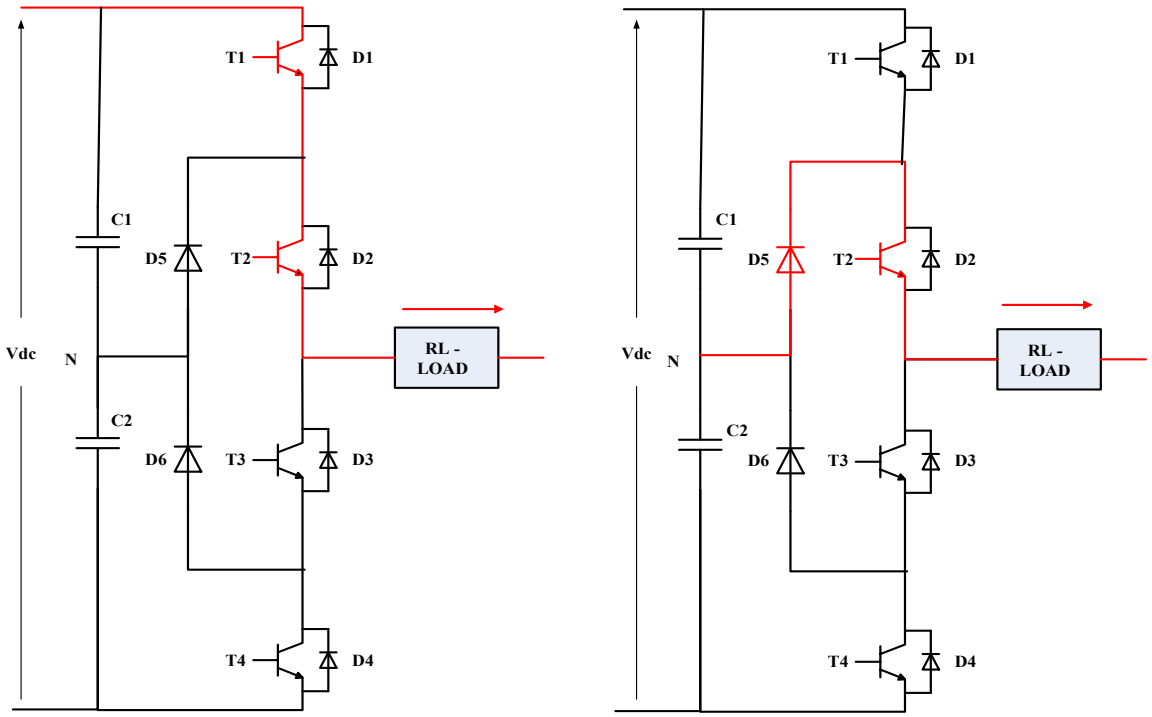


Figure 3.15: Region 2 - V > 0 & I > 0

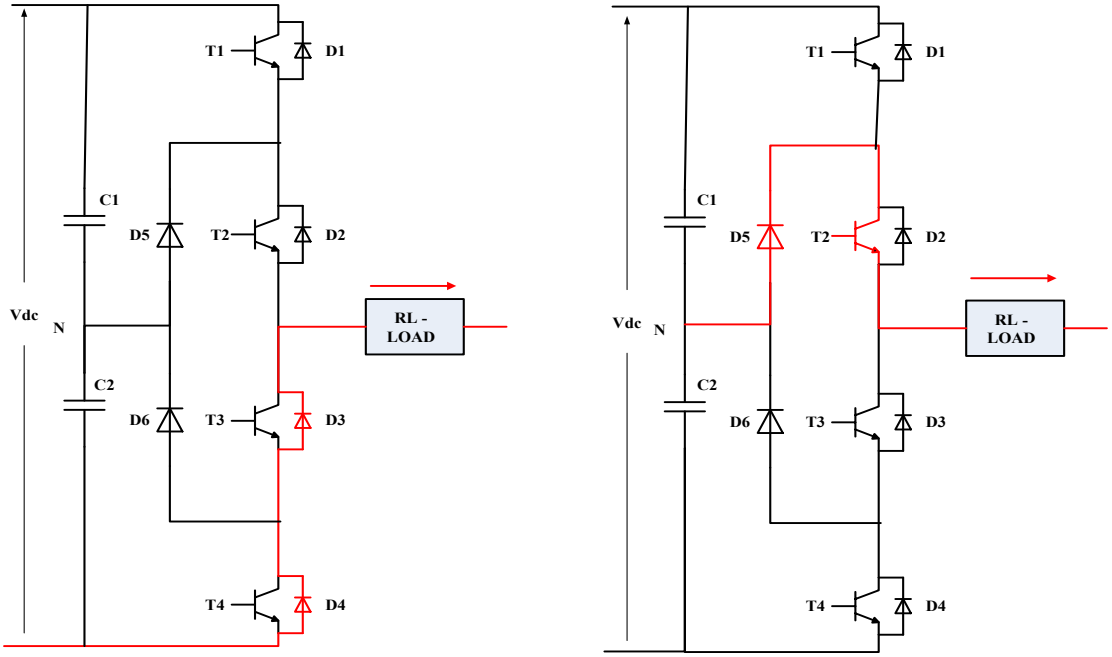


Figure 3.16: Region 3 - V < 0 & I > 0

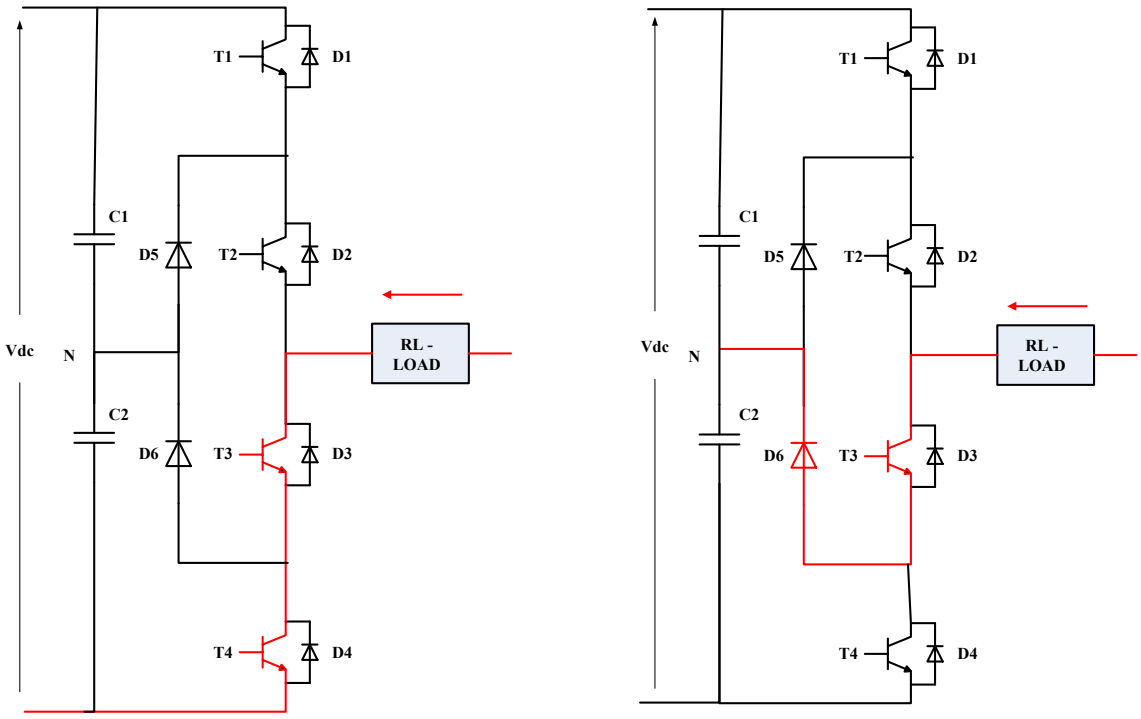


Figure 3.17: Region 4 - V < 0 & I < 0

In order to determine the losses, since the upper and lower IGBT/Diode pairs in a phase leg function in the same fashion, one needs to consider only one pair in case of a two-level inverter. However, in case of a three-level inverter, the upper two pairs of IGBT/Diode need to be considered and one clamping diode needs to be considered to model the losses. In doing so for one group for the phase, one needs to consider only the positive value of voltage at the output. The loss equations can be derived by considering that [22]:

i. Sinusoidal Pulse Width Modulation method for device switching is employed.

   It is because conventional pulse width modulation switches at the maximum number of possible commutation points in time, thereby yielding maximum switching losses.

ii. Modulating function is a sinusoidal with respect to time, given by '$m\sin(\omega t)$'.

iii. The load is inductive and the output current which is sinusoidal, under steady-state condition, lags the output phase voltage by an angle 'φ'.

$$i(\omega t) = I_{pk}\sin(\omega t + \varphi) \tag{3.9}$$

It is known that the 'sine' wave lies between the minimum and the maximum limits of $[-1, 1]$. The modulation index which is a function of 'sine' can be represented as:

$$-1 \leq m\sin(\omega t) \leq 1 \tag{3.10}$$

Since the modulation index cannot be negative, it is required to modify the above function so that it lies between the limits [0, 1].

Adding '1' throughout the inequality

$$0 \leq \{1 + m\sin(\omega t)\} \leq 2 \tag{3.11}$$

Dividing by '2' throughout the inequality

$$0 \leq \left\{\frac{1}{2} + \frac{m}{2}\sin(\omega t)\right\} \leq 1 \tag{3.12}$$

$$0 \leq \tau(t) \leq 1 \tag{3.13}$$

where,

$$\tau(t) = \frac{1}{2} + \frac{m}{2}\sin(\omega t)$$

Hence, $\tau(t) \in [0, 1]$, is the required modulation index function for a two-level inverter.

Since the IGBT and diode operate complementarily during the output fundamental cycle, if the modulation index for IGBT is τ (t), the modulation index for diode is given as {1 – τ (t)}. This is summarized in Table 3.1.

Device	**Period**	**Modulation Index Function τ (t)**
T1	[0, π]	$\frac{1}{2}+\frac{m}{2}\sin(\omega t)$
D1	[π, 2π]	$\frac{1}{2}-\frac{m}{2}\sin(\omega t)$

Table 3.1: Modulation Index Functions of IGBT and Diode in Two-level Inverter

In case of a three-level inverter, the functions of modulation index for all the devices under consideration as follows:

T1: conducts during the period between [φ, π] and $\tau(t)=m\sin(\omega t)$.

The same current is conducted by D1 for the period between [0, φ] and $\tau(t)=m\sin(\omega t)$.

Whenever T1 is conducting, T2 is also under conduction for the same period and therefore for the period when T1 conducts, i.e., [φ, π], modulation function for T2 = 1. However, during the time when T1 stops conducting, T2 will still be under conduction for the time when current is transferred from T1 to D5 during the period [π, π + φ], as the modulation function goes negative being a 'sine' function, factor '1' is added so as to obtain a positive number; the modulation function for T2 for the period [π, π + φ] is given by $\tau(t)=1+m\sin(\omega t)$.

The diode D2 complements T2 for the period between [0, φ] and $\tau(t)=m\sin(\omega t)$.

The clamping diode D5 conducts between [φ, π] complementing T1, and hence its modulation index function is given by $\tau(t) = 1 - m\sin(\omega t)$; since 'sine' function is positive in this region. For the period between [π, π + φ], as the 'sine' function becomes negative, the modulation index function is given as $\tau(t) = 1 + m\sin(\omega t)$.

The modulation index functions for the three-level inverter can be summarized as shown in Table 3.2.

Now, once the modulation index functions for each device for both the inverters have been identified, one can go ahead with the determination of losses occurring in each device.

Device	**Period**	**Modulation Index Function τ (t)**
T1	[φ, π]	$m\sin(\omega t)$
D1	[0, φ]	$m\sin(\omega t)$
T2	[φ, π]	1
T2	[π, π+φ]	$1 + m\sin(\omega t)$
D2	[0, φ]	$m\sin(\omega t)$
D5	[φ, π]	$1 - m\sin(\omega t)$
D5	[π, π+φ]	$1 + m\sin(\omega t)$

Table 3.2: Modulation Index Functions of IGBT and Diode in Two-level Inverter

3.6 DERIVING LOSS EQUATIONS FOR TWO AND THREE-LEVEL INVERTERS

Conduction loss is given by the product of the current through the device and the voltage across the device when the device is conducting and the time for which the device conducts is governed by the modulation function [23]. The loss equations can be derived:

$$P_{cond} = \frac{1}{T}\int_{0}^{T/2} v(t)\, i(t)\, \tau(t)\, d(\omega t) \tag{3.14}$$

In case of switching loss, as mentioned earlier, the switching energy curve versus the current is plotted again to obtain the curve-fitting second-degree polynomial equation in terms of current flowing through the device. It is of utmost importance to compensate for any non-consistency when one makes use of the graphs given in the datasheet. Datasheet graphs are plotted for certain conditions of temperature, current, DC-link voltage and the gate resistance. If the any of the datasheet values and the ones that are employed do not match, it is important to compensate for such variations. As an example, let's say the switching energy plots in the datasheet are plotted for the same values of current, voltage and temperature that one would wish to determine for; however, the gate resistor value varies from the datasheet assumed value; under such a condition, it is important to determine the actual switching energy for the required value of the gate resistor as follows:

$$\frac{E_{employed}}{E_{datasheet}} = \frac{R_{employed}}{R_{datasheet}} \tag{3.15}$$

$$E_{employed} = \frac{R_{employed}}{R_{datasheet}} E_{datasheet} \tag{3.16}$$

Hence, E_{on}, E_{off} and E_{rec} vs. i_x are plotted and their respective curve-fitting second-degree polynomial equations in terms of $\{(a\,i^2 + b\,i + c)$; where 'a' and 'b' are the coefficients of the second-degree term and the first-degree term respectively; and 'c' is the constant$\}$ are obtained. Since the current in turn is a function of 'ωt', one can obtain the expression for switching power loss in terms of current.

$$P_{sw} = f_{sw} \frac{1}{T} \int_0^{T/2} (E_{on} + E_{off}) d(\omega t) \tag{3.17}$$

$$P_{sw} = f_{sw} \frac{1}{T} \int_0^{T/2} E_{rec}\, d(\omega t) \tag{3.18}$$

To evaluate the average conduction losses for the two-level and three-level inverters, the equations listed in Table 3.3 and Table 3.4, respectively, can be used.

Once the average commutation losses and average switching losses of all the devices that make up the inverter under consideration are determined, the total losses for each device can be calculated. With the help of the calculated losses of a device, the junction temperature of the device can then be determined.

Device	Conduction Losses
T1, T2	$\left(\frac{1}{2}\right)\left\{\left(\frac{V_{CE0}\, I_{pk}}{\pi}\right)+\left(\frac{r_{CE}\, I_{pk}^2}{4}\right)\right\}+(m\cos\varphi)\left\{\left(\frac{V_{CE0}\, I_{pk}}{8}\right)+\left(\frac{r_{CE}\, I_{pk}^2}{3\pi}\right)\right\}$
D1, D2	$\left(\frac{1}{2}\right)\left\{\left(\frac{V_{F0}\, I_{pk}}{\pi}\right)+\left(\frac{r_{F}\, I_{pk}^2}{4}\right)\right\}-(m\cos\varphi)\left\{\left(\frac{V_{F0}\, I_{pk}}{8}\right)+\left(\frac{r_{F}\, I_{pk}^2}{3\pi}\right)\right\}$

Table 3.3: Average Conduction Losses of IGBT's and Diodes in Two-level Inverter

Device	Conduction Losses
T1, T4	$\left[\left(\frac{mV_{CE0}\, I_{pk}}{4\pi}\right)\{(\pi-\varphi)\cos\varphi+\sin\varphi\}\right]+\left[\left(\frac{m r_{CE}\, I_{pk}^2}{6\pi}\right)(1+\cos\varphi)^2\right]$
D1, D4	$\left[\left(\frac{mV_{F0}\, I_{pk}}{4\pi}\right)\{(-\varphi)\cos\varphi+\sin\varphi\}\right]+\left[\left(\frac{m r_{F}\, I_{pk}^2}{6\pi}\right)(1-\cos\varphi)^2\right]$
T2, T3	$\left[\left(\frac{V_{CE0}\, I_{pk}}{\pi}\right)+\left\{\left(\frac{mV_{CE0}\, I_{pk}}{4\pi}\right)(\varphi\cos\varphi-\sin\varphi)\right\}\right]+\left[\left(\frac{r_{CE}\, I_{pk}^2}{4}\right)-\left\{\left(\frac{m r_{CE}\, I_{pk}^2}{6\pi}\right)(1-\cos\varphi)^2\right\}\right]$
D2, D3	$\left[\left(\frac{mV_{F0}\, I_{pk}}{4\pi}\right)(-\varphi\cos\varphi+\sin\varphi)\right]+\left[\left(\frac{m r_{F}\, I_{pk}^2}{6\pi}\right)(1-\cos\varphi)^2\right]$
D5, D6	$\left[\left(\frac{V_{F0}\, I_{pk}}{\pi}\right)+\left\{\left(\frac{mV_{F0}\, I_{pk}}{4\pi}\right)\{(2\varphi-\pi)\cos\varphi-2\sin\varphi\}\right\}\right]+\left[\left(\frac{r_{F}\, I_{pk}^2}{4}\right)-\left\{\left(\frac{m r_{F}\, I_{pk}^2}{3\pi}\right)(1+\cos^2\varphi)\right\}\right]$

Table 3.4: Average Conduction Losses of IGBT's and Diodes in Three-level Inverter

The junction temperature of all the devices in the inverter is calculated in this way and depending on the maximum allowable temperature limit that a device can reach, which depends on the capability of the cooling liquid, the maximum switching frequency of the device can be determined. Switching frequency affects switching losses of the device

under consideration. During the presence of high current, if the IGBT's are switched at high switching frequency, there will be a rapid shoot-through in the current thus leading to very high junction temperatures. Therefore, during the starting phase of the motor and also during high accelerations, it is required to lower the switching frequency value so that the maximum junction temperature limits are not exceeded. After the determination of the losses and the junction temperature, the total losses occurring in all the three phases of the inverter can be determined.

P_{total_loss} = *Total losses in the three phases of inverter (W)*

Also, if the output voltage, current and the load power factor are known, one can calculate the power output at the output of the inverter.

P_{output} = *Total power output at the output of the inverter (W)*

Therefore, the inverter input power can be determined and is given by:

P_{input} = *Power input for the inverter (W)*

$$P_{input} = P_{output} + P_{total\_loss} \tag{3.19}$$

3.7 EFFICIENCY COMPARISON OF TWO AND THREE-LEVEL INVERTERS

Therefore, the efficiency of the inverter can be determined as:

$$\eta = \frac{Power\ Output}{Power\ Input} \tag{3.20}$$

$$\eta = \frac{P_{output}}{P_{output} + P_{total\_loss}} \tag{3.21}$$

In the present study, two IGBT inverters from Infineon are considered. As pointed out earlier, in order to have a fair comparison of the cooling efficiency of the heat-sink in use, it is required to compare two inverters that are similar in size. Therefore, when choosing the IGBT modules for the two- and three-level inverters, consideration of sizes is an important factor to be addressed.

The coolant under consideration is 40/60 water-glycol mix and has a maximum coolant temperature of 55 ºC. It can cool devices that have a maximum junction temperature of up to 135 ºC. For the present study, Infineon inverters, three modules of "FF300R12ME4" for two-level inverter were chosen and in case of the three-level inverter, three modules of "F3L300R07PE4*"* were chosen. The datasheets of both the modules of two- and three-level inverters are attached in Appendix. The choice was made depending on the considered DC-link voltage of 600 V and the peak current capability of 280 A. When choosing an inverter module for its blocking voltage capability, it is important to give the provision for dynamic voltage variations that are caused due to the stray inductances that are present within an inverter module. Every module from different manufacturers will have different values of blocking voltage, maximum current capabilities, switching energies, stray inductances, etc., and depending on the optimum value and also on the cost, a particular module can be chosen. However, the rule of thumb in the industry is to give a voltage safety margin of twice the DC-link voltage for each switch in case of the two-level inverter and at least the DC-link voltage value for each switch in case of the three-level inverter; the current safety margin is considered to be at least 1.2 times the maximum current expected to flow through the switch. Cost definitively plays an important role when a component is bought. All the calculations

pertaining to losses, junction temperature and efficiency were performed using the spreadsheet tool of Microsoft Excel.

The PMSM under consideration operates in two regions: the transient region (at starting and during accelerations) and the permanent or continuous region (under steady-state operation). Naturally, the losses under transient region will be higher due to high demand of torque and consequently high amount of current. Therefore, it is principally important that the devices do not violate the junction temperature limits especially in this transient region of operation.

For the purposes of demonstration, two cases have been chosen for the comparison of the losses as a function of the switching frequency; one below the base speed of the PMSM and the other above the base speed.

For the two chosen modules, the total losses for one inverter leg were evaluated for the range of switching frequencies and the graph is depicted as shown in Figure 3.18 for the machine torque of 180 Nm and the speed of 3500 RPM (which is below the base speed value of the machine).

It can be observed from Figure 3.18 that the losses in three-level inverter are more significant at lower frequencies of switching. However, beyond 4 kHz, the losses in two-level inverter increase at a sharper rate for the system under consideration.

The comparison of losses in one leg of the inverter for the machine torque of 127 Nm and the speed of 7500 RPM (which is above the base speed value of the machine) have also been demonstrated graphically as shown in Figure 3.19.

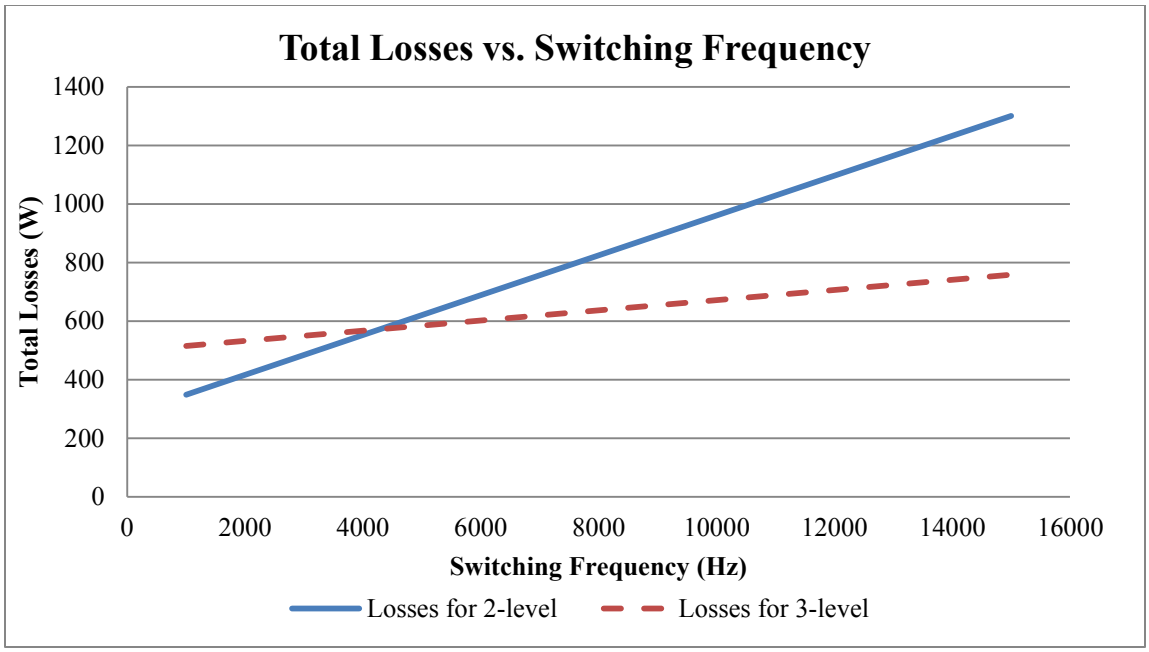


Figure 3.18: Total Losses as a Function of Switching Frequency for Two- and Three-level Inverters for a Torque of 180 Nm and a Speed of 3500 RPM

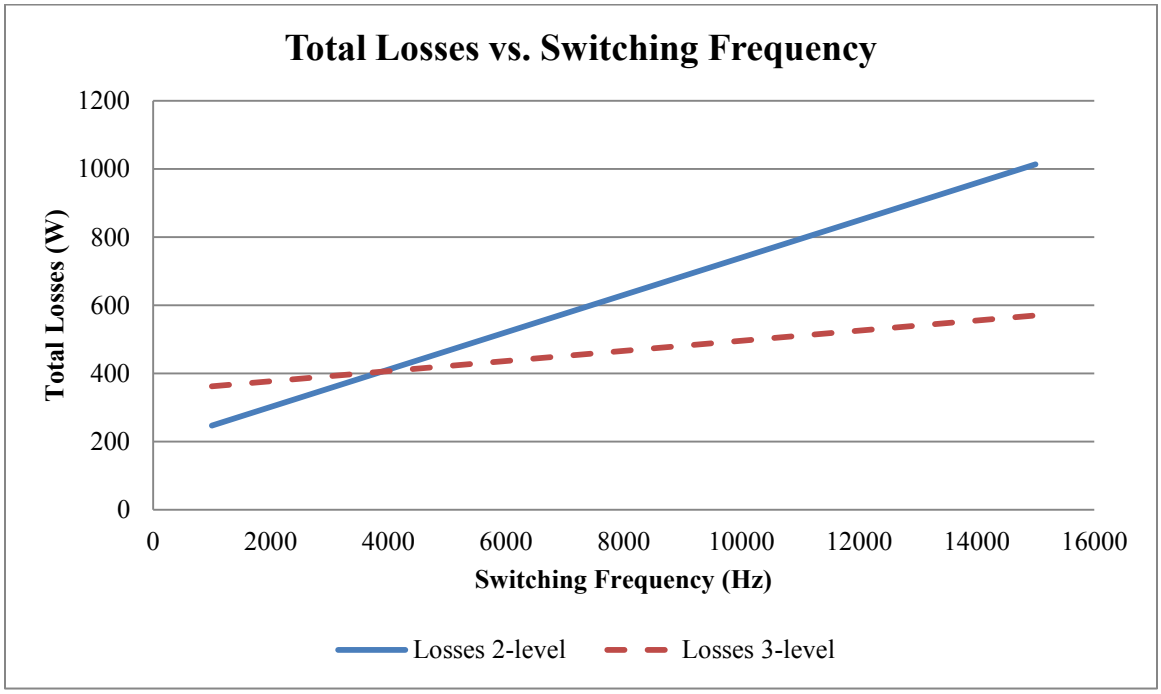


Figure 3.19: Total Losses as a Function of Switching Frequency for Two- and Three-level Inverters for a Torque of 127 Nm and a Speed of 7500 RPM

From Figure 3.19, it can again be observed that the losses in three-level inverter dominate for switching frequencies lower than 4 kHz, however, beyond that, the losses in two-level inverter have a sharp increment in slope when compared to that in three-level inverters.

Figure 3.20 depicts the temperature rise in each switch in one leg of the two- and three-level inverters. Keeping in view the capability of the coolant which can handle up to a rise in temperature of 135 ºC, any switching frequency resulting in a temperature rise beyond 135 ºC for any individual component needs to be ignored. For the torque of 180 Nm and for the speed of 3500 RPM for the PMSM machine, the junction temperature for all the switches have been evaluated and plotted for a range of switching frequency, as shown in Figure 3.20.

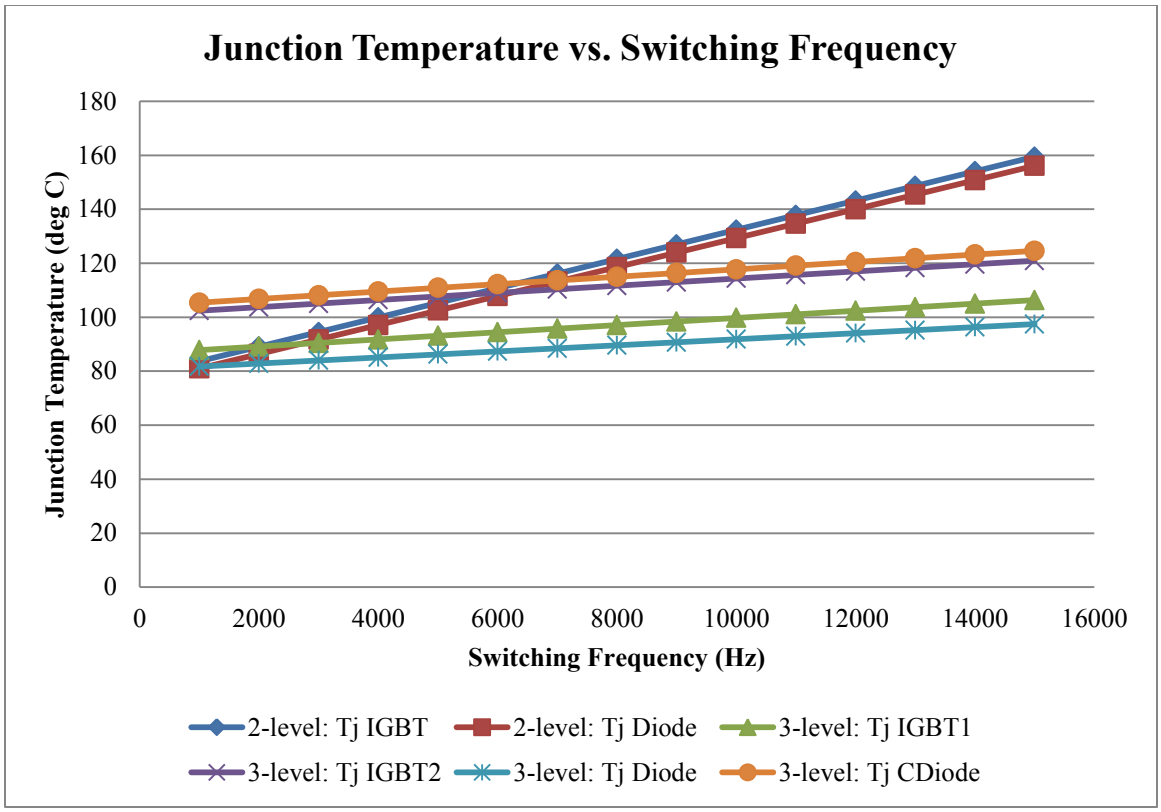


Figure 3.20: Junction Temperature for all the Devices in Two- and Three-level Inverters for a Torque of 180 Nm and a Speed of 3500 RPM

It can be observed that the junction temperature of the IGBT in the case of the two-level inverter exceeds beyond the acceptable limit with the values of switching frequency beyond 10 kHz.

Similarly, the evaluation of junction temperature of the devices for the torque of 127 Nm and the speed of 7500 RPM for the PMSM have been presented graphically, in Figure 3.21, for the switching frequency ranging from 1 kHz to 15 kHz.

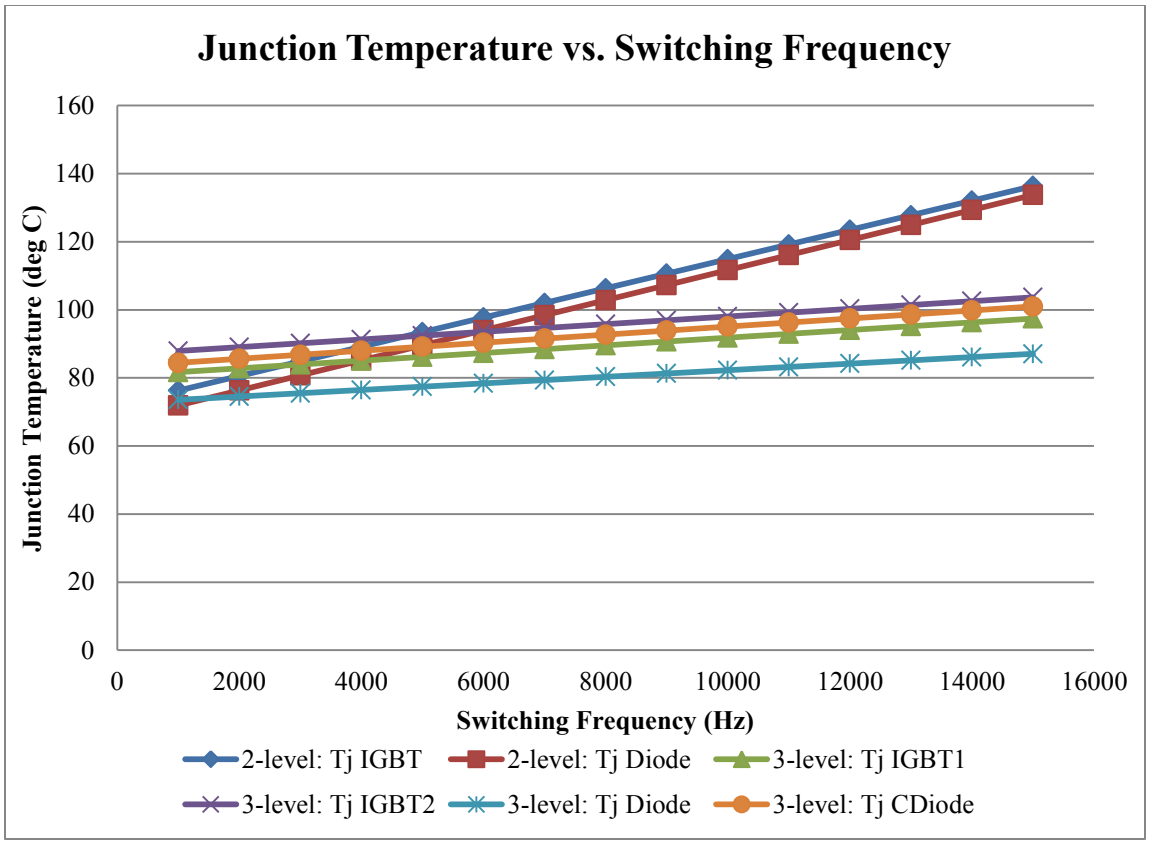


Figure 3.21: Junction Temperature for all the Devices in Two- and Three-level Inverters for a Torque of 127 Nm and a Speed of 7500 RPM

As can be seen from Figure 3.21, the acceptable junction temperature limit in the case of the IGBT in the two-level inverter exceeds only after increasing the switching frequency beyond 15 kHz, whereas, in case of the three-level inverter, the junction temperature of the devices remain well-under the acceptable limit.

Once the maximum acceptable limit of switching frequency for two and three-level inverters have been determined, Microsoft Excel Spreadsheet Tool (or any other convenient tool for the user) can be used to vary the switching frequencies of both the inverters starting from a value above 4 kHz (as this is the value at which the efficiency of the three-level inverter starts getting higher than that of the two-level inverter for the

chosen inverter modules). Once the switching frequency limits for the transient region of operation have been determined, the efficiencies of the two inverters can be compared. In case of the continuous region of operation, the peak current value decreases due to decreased torque demand. Therefore, for the same cooling capability, the junction temperatures of the devices in the chosen two and three-level inverters remain much lower than the acceptable limit even when they are switched at 20 kHz. The maximum junction temperatures reached for the devices in two and three-level inverters in the continuous region of operation are 110 ºC and 85 ºC, respectively. Figure 3.22 and Figure 3.23 compare the efficiencies of the two and three-level inverters for transient and continuous regions of operation, respectively.

In Figure 3.22, the efficiencies of the two-level inverter are determined by switching the devices at 6 kHz up to the base speed of the motor and at 8 kHz beyond the base speed of the motor; in case of the three-level inverter, the devices are switched at 5 kHz for region up to the base speed and at 10 kHz for the region above the base speed. It can be observed that comparable or even better efficiency can be obtained using a three-level inverter when compared with the two-level inverter, even though the former is switched at a reduced switching frequency.

In Figure 3.23, the efficiencies of the two-level and three-level inverter are compared by switching the devices in both of them at 20 kHz for the continuous region of operation of the motor, without violating the junction temperature limits. It can be observed that the three-level inverter presents much better efficiency throughout the entire range.

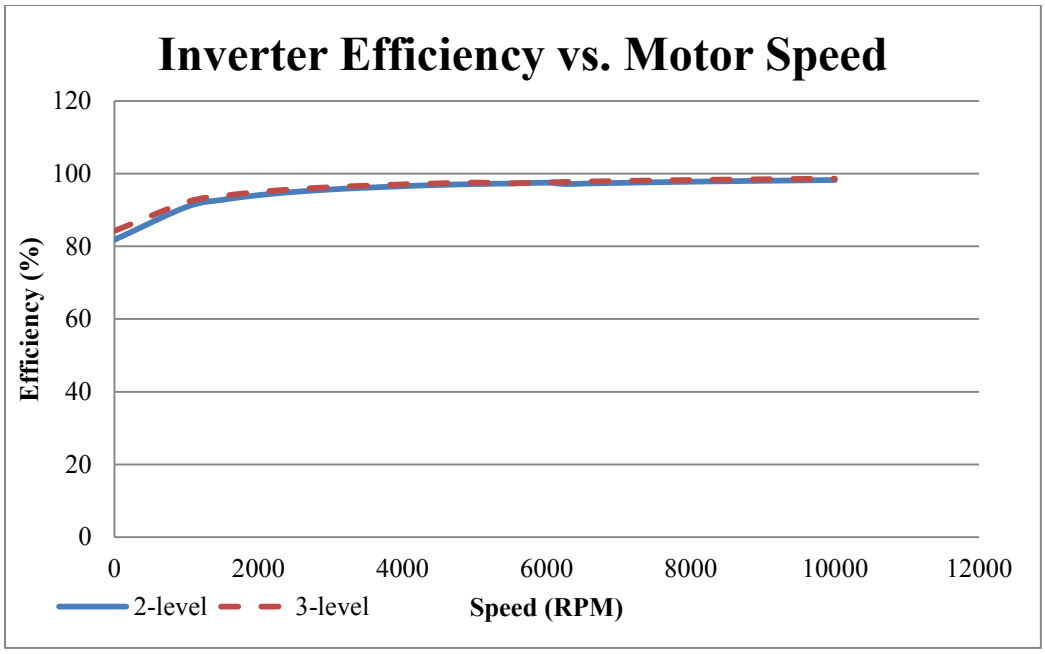


Figure 3.22: Efficiencies of Two and Three-level Inverters for Transient Region of Operation of the Motor

In the continuous region, comparable efficiency can be obtained for the two and three-level inverters when the former is switched at 14 kHz and the latter is switched at 20 kHz, for the entire range of speed. This can be observed in Figure 3.24.

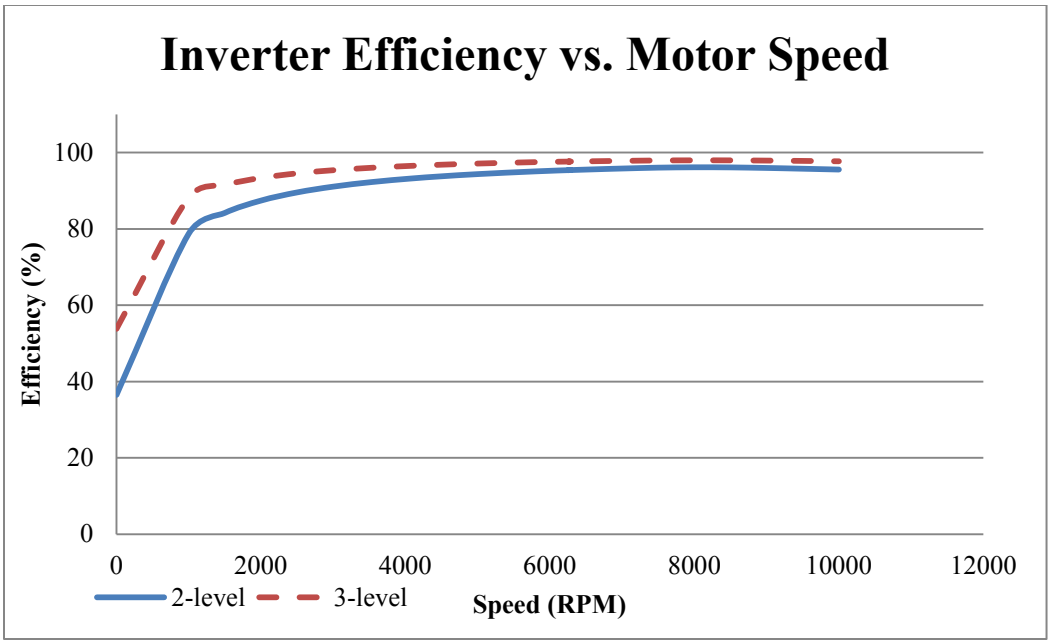


Figure 3.23: Efficiencies of Two and Three-level Inverters for Continuous Region of Operation of the Motor at 20 kHz Switching Frequency

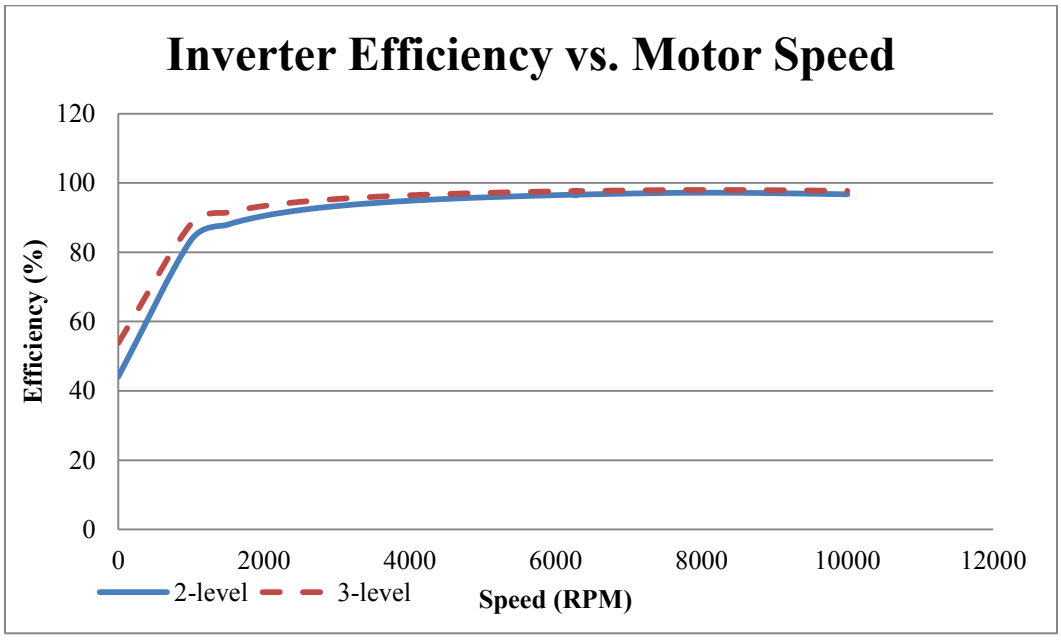


Figure 3.24: Efficiencies of Two and Three-level Inverters for Continuous Region of Operation of the Motor

From the above comparisons, it can be concluded that the three-level inverter presents better efficiency for both the transient and continuous regions of operation encountered in an automotive even when the switches in the three-level inverter are switched at a lower frequency that those in case of a two-level inverter.

3.8 PREVALENT DC-LINK VOLTAGE BALANCING ISSUE IN THREE-LEVEL INVERTER

The switching of the devices in an inverter is the reason for the presence of high-frequency pulsating currents in the DC bus of a battery-powered motor drive [24]. The aim of modulating (i.e., switching at appropriate intervals) the device is to obtain, in every switching period, an average value of the voltage which is equivalent to the average value of the reference signal. In order to vary the speed of the machine, the switches of the inverter need to be modulated. Therefore, modulation of the inverter switches leads to speed and torque changes which are accompanied by the change in current whose control has already been addressed in the earlier sections of this chapter (Chapter 4 would concentrate on the modulation of the switches of the two- and three-level inverters). However, before starting on with the modulation strategy, it is primarily important to address the DC-link capacitor unbalance issue which is widely-faced in the case of the three-level inverter under consideration. The neutral point potential is subject to fluctuation due to the irregular charging and discharging of the upper and lower DC-link capacitors. This is the reason why the neutral point voltage fails to keep at the half of the DC-link voltage, thus leading to excessively high voltage being applied across the switching devices and thus damaging them [25]. In order to cut down the cost of extra circuitry which would have otherwise been required if conventional modulation strategy

was employed, it is important that the modulation strategy chosen takes care of the inherent unbalance and provides balanced average DC-link capacitor voltages. Though the modified modulation strategy "might" present some side-effects, in terms of increased switching frequency (resulting in more losses and thus increasing the junction temperature of the devices), down-graded THD spectrum, or might result in any other un-expected reduction in quality or performance; as long as the level of deterioration is well within the allowable or tolerable limits, the modulation strategy is worth a modification keeping in view the otherwise unavoidable unbalance. While working towards neutral-point balancing, it is required in this project that there is no additional circuit adding to the cost of the system. Hence, it is required to modify the switching in such a way that there is no extra circuit required for balancing.

3.9 DETERMINATION OF THE FACTORS INFLUENCING THE NEUTRAL-POINT CURRENT

Before starting off with the modulation strategy apart from the conventional one (which is SPWM), it is required to ascertain the reasons behind the neutral-point shift and what all factors contribute to it and the resulting unbalance. The two DC-link capacitors are connected at the neutral-point in case of the three-level inverter. Unlike the two-level inverter, the devices in the three-level inverter have unequal loss distributions as seen previously. Therefore, it is required to turn-on and turn-off the devices in such a way such that the two capacitors are charged and discharged in a balanced manner. The unbalance would otherwise lead to non-zero neutral-point potential which needs to be avoided. Apart from the unbalanced distribution of losses, the causes of neutral-point voltage deviation include, but are not limited to:

- Unbalanced DC capacitors due to manufacturing tolerances leading to irregular unpredictable charging and discharging in each capacitor
- Inconsistency in switching device characteristics, i.e., non-ideal device components
- Unbalanced three-phase operation in case of faults or system disturbances due to transient conditions at the load
- Imperfection in the symmetry of the switching patterns due to device dead times

There may be serious consequences if the "average" neutral-point potential is not equal to zero since the semiconductor devices may have to handle high over-voltages thus leading to mal-functioning of the switches and eventually, failure of the inverter and thus the entire drive. Also, unbalanced capacitor voltages might lead to neutral-point voltage oscillations to mitigate which large capacitors might be required.

One can visualize the DC-link voltage unbalance problem when the switches are modulated using the regular Sinusoidal Pulse Width Modulation strategy and without any balancing control in place. This can be visualized in Figure 3.25 for an RL-load with the parameters mentioned in Table 2.1. The fundamental frequency is considered to be 250 Hz and the switching frequency is 2 kHz. The modulation index is 0.53 and the power factor of the load being 0.94.

From Figure 3.25, it can be observed that the DC-link capacitor voltages deviate from the average value and this problem needs to be rectified.

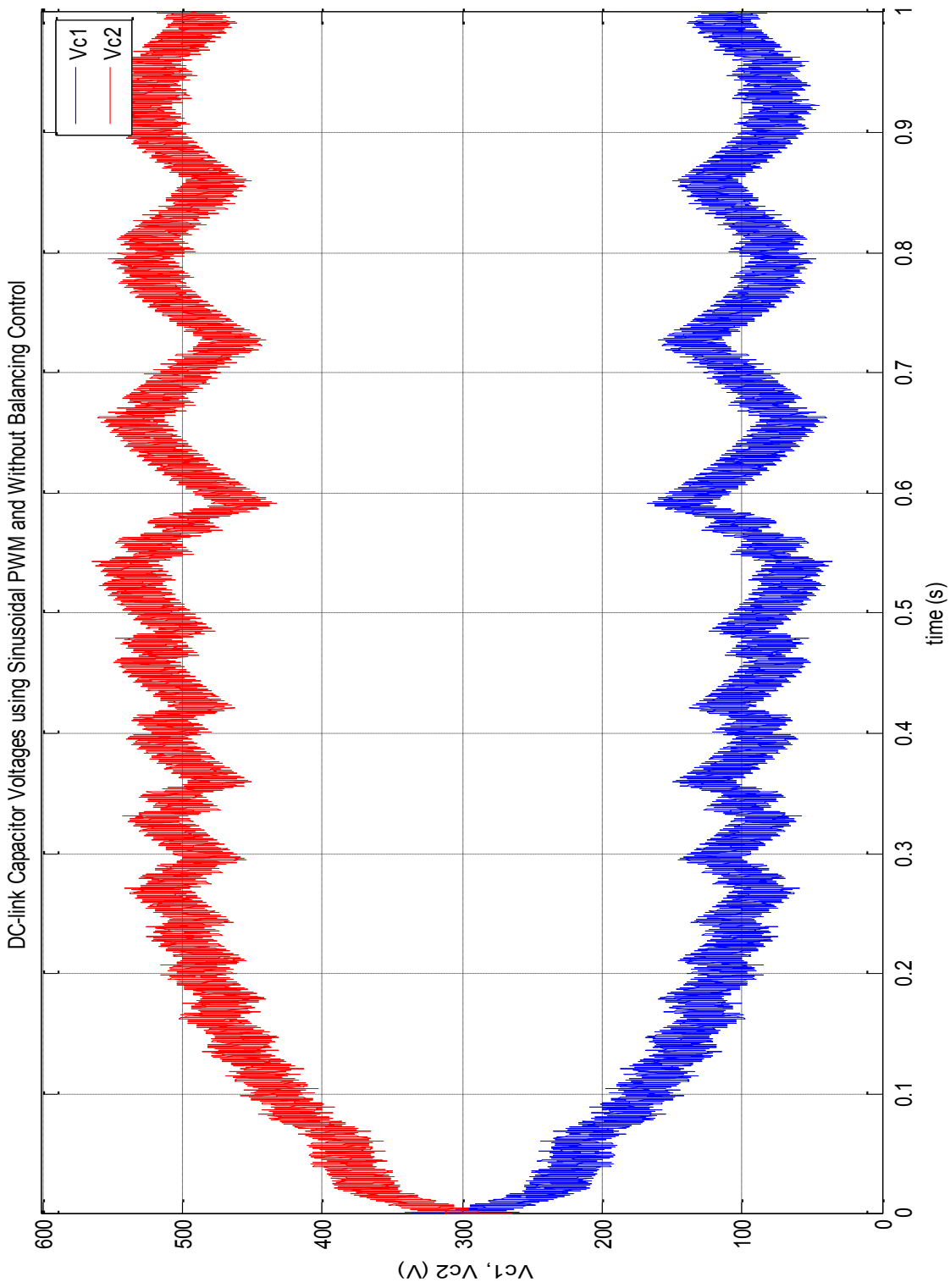


Figure 3.25: DC-link Capacitor Voltages using Sinusoidal Pulse Width Modulation without Balancing Control

The neutral-point voltage balancing problem essentially is a neutral-point current problem, which is going to be proved in a short while from now. The purpose is now to have zero average neutral-point current which otherwise, if present, leads to the unbalance and hence causes the deviation in the average neutral-point voltage from zero.

There are a few methods that can be adopted to avoid the neutral-point voltage deviation problem and they are listed as follows:

- Using two separate voltage sources supplying the two capacitors; but this approach would increase the cost
- Separate neutral point voltage balancing circuit that can be employed with extra converters, increasing the size of the system and also leading to increased system cost
- Adopting control algorithm which could be cost effective, but could be complex
- Improving the modulation method by modifying the switching pattern of the switching devices so that the average neutral point current is zero at all times

3.10 DERIVING THE NEUTRAL-POINT CURRENT EQUATION

In order to model the neutral-point balancing problem, it is beneficial to measure and make use of the actual difference in voltage between the two capacitors to model a regulator that would snap the neutral-point voltage to the zero level; throughout the cycle of operation. To do so, one can consider the single-phase circuit of the three-level Neutral-Point Clamped Inverter [26] as shown in Figure 3.25.

Considering the current passing through the upper DC-link capacitor C_1 to be 'i_{C1}' and through the lower DC-link capacitor C_2 to be 'i_{C2}', one can evaluate the neutral point current 'i_o' using Kirchoff's Current Law (KCL) at the node N, as shown in Figure 3.25.

The voltage developed across C_1 and C_2 due to the current flowing through them is V_{C1} and V_{C2}, respectively.

$$i_{C1} = C_1 \frac{dV_{C1}}{dt} \tag{3.22}$$

$$i_{C2} = C_2 \frac{dV_{C2}}{dt} \tag{3.23}$$

$$i_o = i_{C1} - i_{C2} \tag{3.24}$$

Assuming that $C_1 = C_2 = C$, i_o can be given as:

$$i_o = C \frac{d(V_{C1} - V_{C2})}{dt} \tag{3.25}$$

Considering 'v_o' to be the voltage at the neutral point, as shown in Figure 3.24, one can write:

$$V_{C1} = +\left(\frac{V_{dc}}{2}\right) - v_o \tag{3.26}$$

$$V_{C2} = v_o - \left(-\frac{V_{dc}}{2}\right) \tag{3.27}$$

$$V_{C2} = v_o + \left(\frac{V_{dc}}{2}\right) \tag{3.28}$$

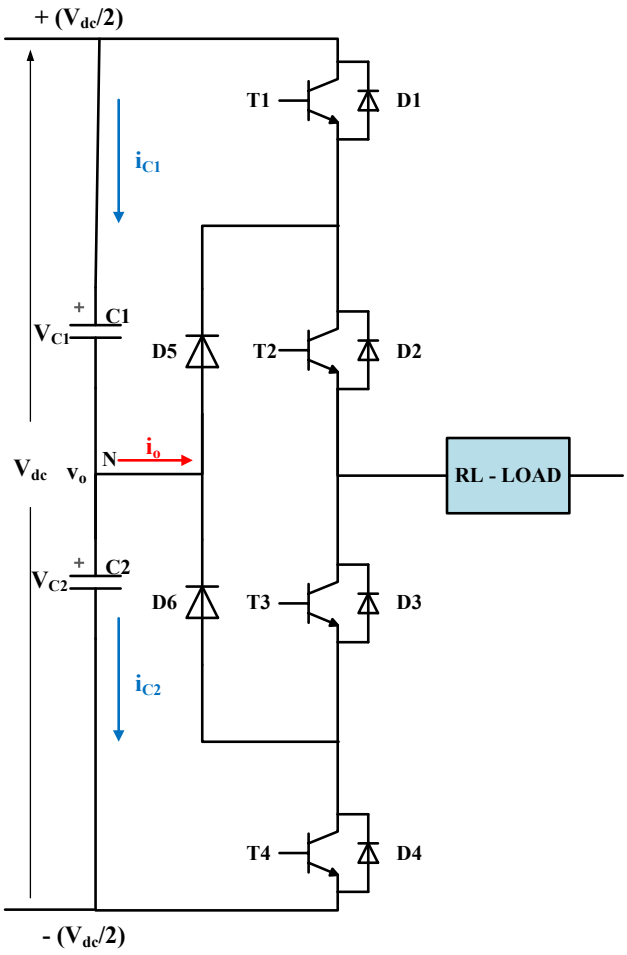


Figure 3.26: Three-level Neutral-Point Clamped Inverter with the DC-link Capacitors

Hence,

$$i_o = C\frac{d}{dt}\left(\frac{V_{dc}}{2} - v_o - v_o - \frac{V_{dc}}{2}\right) \tag{3.29}$$

$$i_o = C\frac{d(-2v_o)}{dt} \tag{3.30}$$

$$i_o = -2C\frac{dv_o}{dt} \tag{3.31}$$

$$dv_o = -\frac{1}{2C} i_o \, dt \tag{3.32}$$

Integrating on both sides,

$$\int_0^t v_o \, dt = -\frac{1}{2C} \int_0^t i_o \, dt \tag{3.33}$$

Dividing on both the sides by the switching time period, T,

$$\frac{1}{T} \int_0^t v_o \, dt = -\frac{1}{2C} \left\{ \frac{1}{T} \int_0^t i_o \, dt \right\} \tag{3.34}$$

Therefore, the average neutral-point voltage is a function of average neutral-point current. The average value of any quantity, voltage or current, can be obtained as the product of its instantaneous value and the duty cycle of operation. In case of the neutral-point current, since it is contributed by all the three phases; A, B and C, its average value can be obtained as:

$$I_o(t) = \sum_{x=a}^{c} d_x(\omega t) i_x(\omega t) \tag{3.35}$$

$d_x(\omega t)$ = duty cycle of phase 'x'

x = 'a' or 'b' or 'c'

From Chapter 3, we know that the duty cycle and the output current are the sinusoidal functions of time. Assuming the fundamental output voltage is a sinusoidal function of time, then the fundamental output current is also a sinusoidal function of time but phase-shifted from the voltage by the load power factor angle, φ.

$$v_a(\omega t) = V_m \sin(\omega t)$$

$$v_b(\omega t) = V_m \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{3.36}$$

$$v_c(\omega t) = V_m \sin\left(\omega t + \frac{2\pi}{3}\right)$$

The output phase currents are phase shifted to the voltage, as mentioned before, by the load power factor angle, φ.

$$i_a(\omega t) = I_m \sin(\omega t + \varphi)$$

$$i_b(\omega t) = I_m \sin\left(\omega t + \varphi - \frac{2\pi}{3}\right) \tag{3.37}$$

$$i_c(\omega t) = I_m \sin\left(\omega t + \varphi + \frac{2\pi}{3}\right)$$

Also, the duty cycles can be expressed as sinusoidal functions of time. However, though the duty cycle is a sinusoidal function of time, it cannot be a negative value. Therefore, only the absolute value is considered.

$$m_a(\omega t) = abs(m \sin(\omega t))$$

$$m_b(\omega t) = abs\left(m \sin\left(\omega t - \frac{2\pi}{3}\right)\right) \tag{3.38}$$

$$m_c(\omega t) = abs\left(m \sin\left(\omega t + \frac{2\pi}{3}\right)\right)$$

The average neutral-point current can now be determined as:

$$I_o = m_a(\omega t)\, i_a(\omega t) + m_b(\omega t)\, i_b(\omega t) + m_c(\omega t)\, i_c(\omega t) \tag{3.39}$$

With conventional modulation scheme, the average neutral-point current over a switching period can be evaluated as follows:

$$I_o = \frac{1}{T}\int_0^T \{m_a(\omega t)\, i_a(\omega t) + m_b(\omega t)\, i_b(\omega t) + m_c(\omega t)\, i_c(\omega t)\}\, d(\omega t) \tag{3.40}$$

By substituting the functions representing the duty cycles and the currents for each phase, one can determine the average neutral-point current to be given by:

$$I_o = \frac{3}{2}\,|m|\, I_m \cos\varphi \tag{3.41}$$

It can be observed that for the conventional modulation scheme, the average neutral-point current is not zero and therefore leads to an unbalance in the neutral-point voltage. The general trend in carrier-based PWM methods is to add an offset (zero-sequence signal) to the modulation waves of all the three phases, so that the line-to-line voltage remains the same. However, this addition of an offset does change the effective current path through the capacitor. This modulation strategy is alternately addressed as Carrier-based Space Vector Modulation (CB-SVM) Strategy.

The other very popular modulation strategy of the recent times is the Space Vector Pulse Width Modulation (SVPWM) strategy. In this strategy, the switching states of all the three legs of the inverter are utilized appropriately (according to the requirement which in this case is the balancing of the DC-link capacitor voltages) to provide the required

output voltage. As it is the combination of the switching states and the extent for which a switching state is active in a switching period which provides the output voltage, for the current requirement, one needs to change the switching sequence or the on-time of the switching state vector, or both.

Both these strategies will be dealt with in detail in the upcoming chapters. The above mentioned modulation strategies (CB-SVM and SVPWM) provide an increment in the maximum output voltage by 15%.

CHAPTER 4: CARRIER-BASED SPACE VECTOR PULSE WIDTH MODULATION

4.1 INTRODUCTION

The present chapter deals with Space Vector Modulation employed using the Carrier-based approach as in Sinusoidal Pulse Width Modulation. Carrier-based Space Vector Modulation strategies for the application in the two-level inverter and in the three-level inverter with neutral-point balancing (without any additional circuit) have been presented. The DC-link equivalent circuit has been derived and neutral-point balancing has been carried out by employing a PI controller which minimizes the neutral-point voltage deviation from the set point.

4.1.1 CARRIER-BASED SPACE VECTOR MODULATION

In the conventional Sinusoidal Pulse Width Modulation (SPWM) strategy, the amplitude modulation index controls the fundamental frequency component of the output voltage. However, in this case, the maximum value of the fundamental component of the line-to-line output voltage is only 61.2% of the DC-link voltage, at the maximum modulation index in the linear range of 1. This presents a poor utilization of the voltage available at the DC-link. In order to make better utilization of the DC-link voltage, one needs to go beyond the linear range of the modulation index, which is the over-modulation range, thus boosting the fundamental frequency component of the output voltage to 74.4% for square-wave operation [27]. However, in the over-modulation range, the amplitude modulation index has a non-linear relationship with the fundamental line-to-line output voltage as opposed to the linear range where the two quantities share a linear relationship. Though the output voltage can be increased by employing over-modulation, it also

introduces low-order harmonic components which are difficult to filter by the load inductance. To fulfill a similar objective of boosting the fundamental component of output voltage, another approach can be followed which does not introduce any lower order harmonics. This approach is the Carrier-based Space Vector Modulation, which in simple terms means the realization of Space Vector Modulation using the conventional Carrier-based approach. The approach for using Carrier-based Space Vector Modulation (CB-SVM) for two- and three-level inverters will be discussed in the upcoming sections.

4.1.2 MODULATION OF TWO-LEVEL INVERTER USING CB-SVM

In this strategy, as the name suggests, SVM-like signal is obtained from the carrier-based technique as that of a conventional SPWM. Implementing CB-SVM is similar to implementing the SPWM, with the only difference being that the reference waveforms are modified every switching period to obtain 15% more utilization of the DC-link or in other words, increasing the linear range of the modulation index. Similar to the implementation of SPWM where a fundamental frequency modulating wave is compared with high frequency triangular wave (since in case of a triangular wave, all the even order harmonics are zero and the odd order harmonics diminish with increase in order, as the reciprocal square of the order), in the present case also, the modified reference wave is compared with high frequency carrier waveform. In case of a two-level inverter, as there are only two switches per phase of the inverter, only one triangular carrier is required so that the two switches could be turned-on and -off complementarily.

From the equations (3.36, 3.37 & 3.38) in Chapter 3, it is known that the fundamental output voltage, the output current and the duty cycle are the sinusoidal functions of time. Assuming that the three phases are balanced and the instantaneous values of the three

phase voltages sum to zero $\{ v_a(t)+v_b(t)+v_c(t)=0 \}$, the peak value of the fundamental output phase voltage using SPWM is linearly related to half the DC-link voltage $\left(\frac{V_{dc}}{2}\right)$ and the proportionality factor is the amplitude modulation index which decides the maximum amount of output voltage for a given DC-link voltage. As an example, the relation is demonstrated for phase A as follows:

$$\hat{v}_a = m_a \frac{V_d}{2} \tag{4.1}$$

The modification factor must be added to each reference signal to obtain SVM-like waveform.

$$\begin{aligned} v_{a,m} &= v_a - v_k \\ v_{b,m} &= v_b - v_k \\ v_{c,m} &= v_c - v_k \end{aligned} \tag{4.2}$$

v_i, $v_{i,m}$ & v_k represent the reference signal, the modified reference signal and the modification factor respectively; where, $i = a, b, c$.

The modification factor to be employed so that the output line-to-line voltage is not modified is given by [28]:

$$v_k = \frac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2} \tag{4.3}$$

An example of the modified reference signal for Phase A can be shown in Figure 4.1.

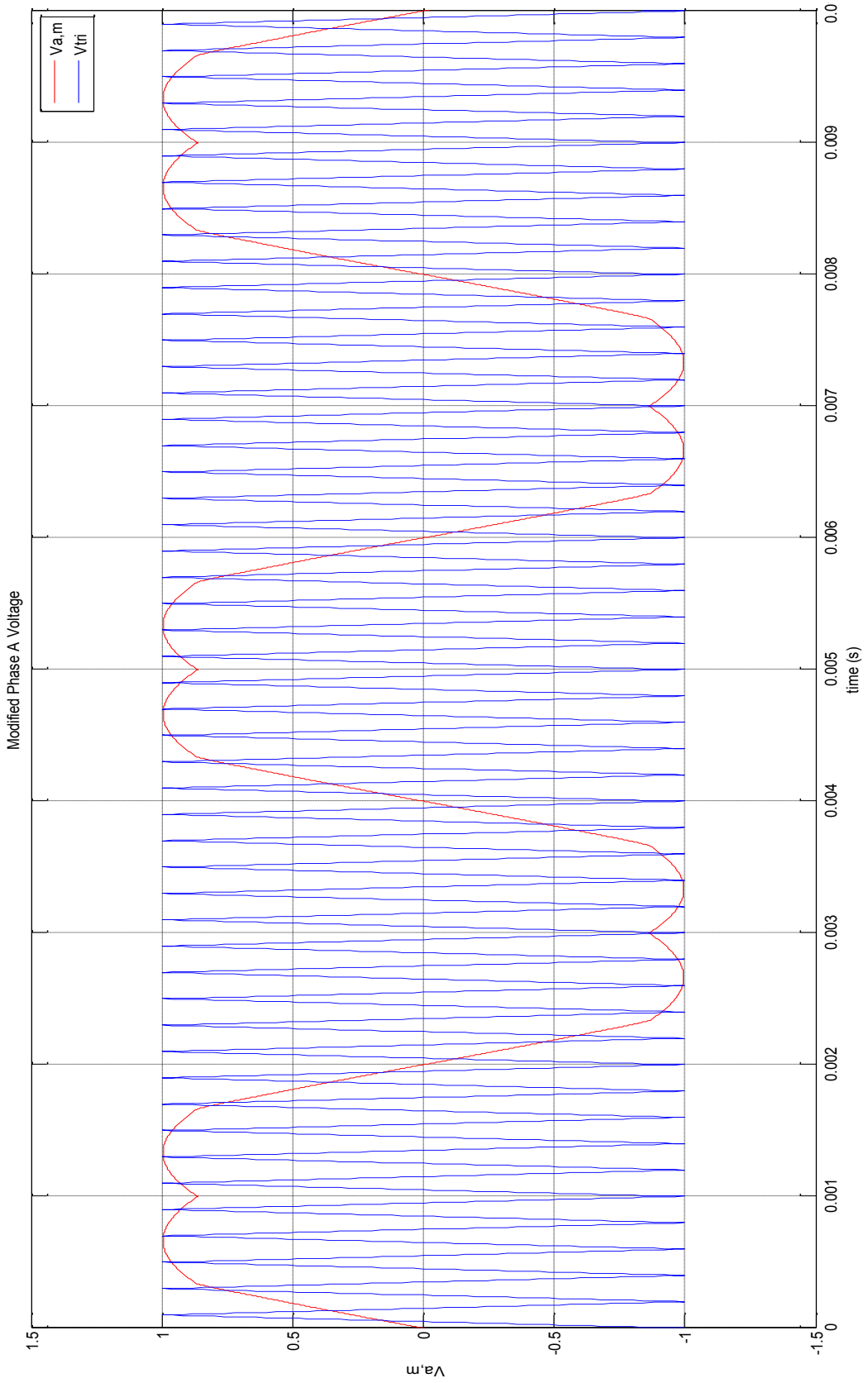


Figure 4.1: Modified Phase 'A' Reference Signal for Two-level Inverter

This modulation strategy is alternatively known as “Min-Max Modulation” strategy.

When considering CB-SVM, it is assumed that load is inductive so that the load current remains constant in a switching period, the DC-link voltage and the phase output voltage also remain constant during the considered switching period; as shown in Figure 4.2.

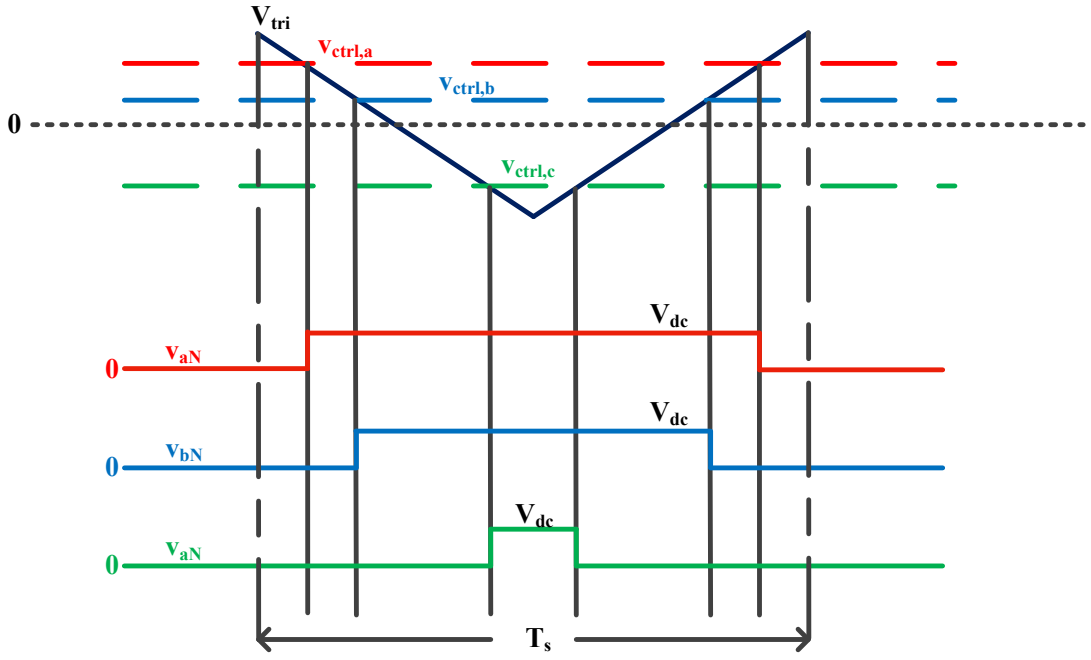


Figure 4.2: Gating Signal Generation in a Switching Period for One Leg of a Two-level Inverter

4.1.3 MODULATION OF THREE-LEVEL INVERTER USING CB-SVM

In case of a three-level inverter, as there are four switches per phase of the inverter, two triangular carriers are therefore required so that the four switches could be turned-on and –off complementarily.

It is now required to know as to how to place the two triangular carriers so that the harmonic content is not high. However, from literature, it is known that the Phase

Disposition (PD) PWM method is the most preferable due to lower Total Harmonic Distortion (THD) in the output waveform [29].

From the brief introduction in Chapter 3, it is known that in case of the three-level inverter, with the conventional sinusoidal pulse width scheme, the average neutral-point current is given as Equation (3.41),

$$I_o = \frac{3}{2} |m| \, I_m \cos\varphi$$

There are three reference signals in case of conventional SPWM and in every switching period; one of the three signals has the maximum value, one has the minimum value and the remaining signal has the middle voltage value. In case of a three-level inverter, the signal having positive maximum value switches its corresponding phase from the neutral-point to the positive of the DC-link in the first half of the considered switching period, and vice-versa for the other half; whereas the signal having minimum value switches its corresponding phase from the negative rail of the DC-link to neutral-point for the first half of the switching period, and vice versa for the other half of the switching period. This can be seen in Figure 4.3.

However, the signal having the middle value may either be positive or negative and correspondingly it will switch its phase like that of the signal having maximum value or the minimum value, respectively. Therefore, if one can decompose the signal having middle value so that middle phase which is connected to the neutral-point can have equivalent charge and discharge time for the DC-link capacitors for every switching

period, one can control the average neutral-point voltage and eventually the neutral-point current.

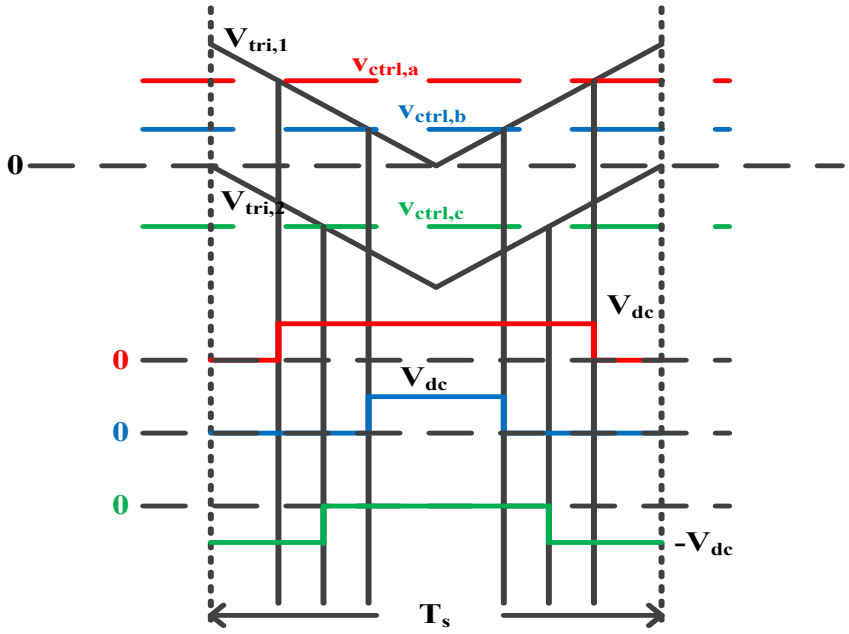


Figure 4.3: Gating Signal Generation in a Switching Period for One-leg of a Three-level Inverter

To be able to achieve this condition, an offset needs to be added to the modulating signal having middle value in every switching period throughout the entire cycle. In order to do this, it is assumed that the load is highly inductive and the switching devices are ideal so that one can assume that the DC-link voltage, the reference voltages and the output current are not varying in a switching period. This can be visualized as shown in Figure 4.4.

A common mode offset requires to be added to all the three reference signals. In case of a two-level inverter, for the phase having the middle voltage value, the common mode offset is split and added to the two halves in such a way that the two halves of the middle-

valued voltage reference signal is placed at an equal distance on the either side of the '0' axis.

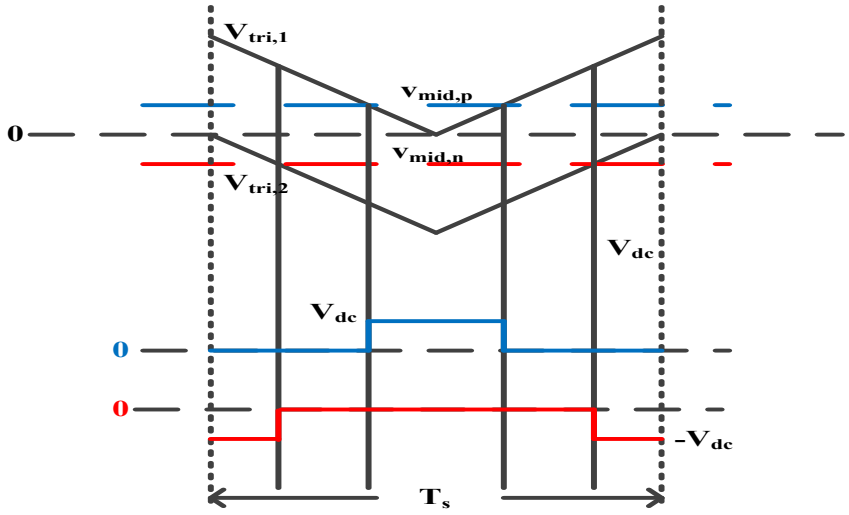


Figure 4.4: Decomposition of a Reference Signal in a Switching Period

It is required to modify all the three phases but not just the phase with the middle value. This is because at all times, the condition $(v_a + v_b + v_c = 0)$, or alternatively, $(v_{\max} + v_{mid} + v_{\min} = 0)$ must satisfy and hold good. Therefore, the factor '$\frac{1}{2}$' is employed in order to decompose the reference signals for each phase [30].

$$v_{ip} = \frac{1}{2}\left[v_i - \min(v_a, v_b, v_c)\right]$$

$$v_{in} = \frac{1}{2}\left[v_i - \max(v_a, v_b, v_c)\right] \tag{4.4}$$

where, i = a, b, c

The idea is to obtain an SVM pattern from the conventional SPWM waveform, and this strategy is alternatively called "Carrier-based SVM", so that maximum range for

modulation is achieved and thereby, DC-link utilization is increased. Therefore, the reference signals in each phase are now decomposed into positive and negative reference signals.

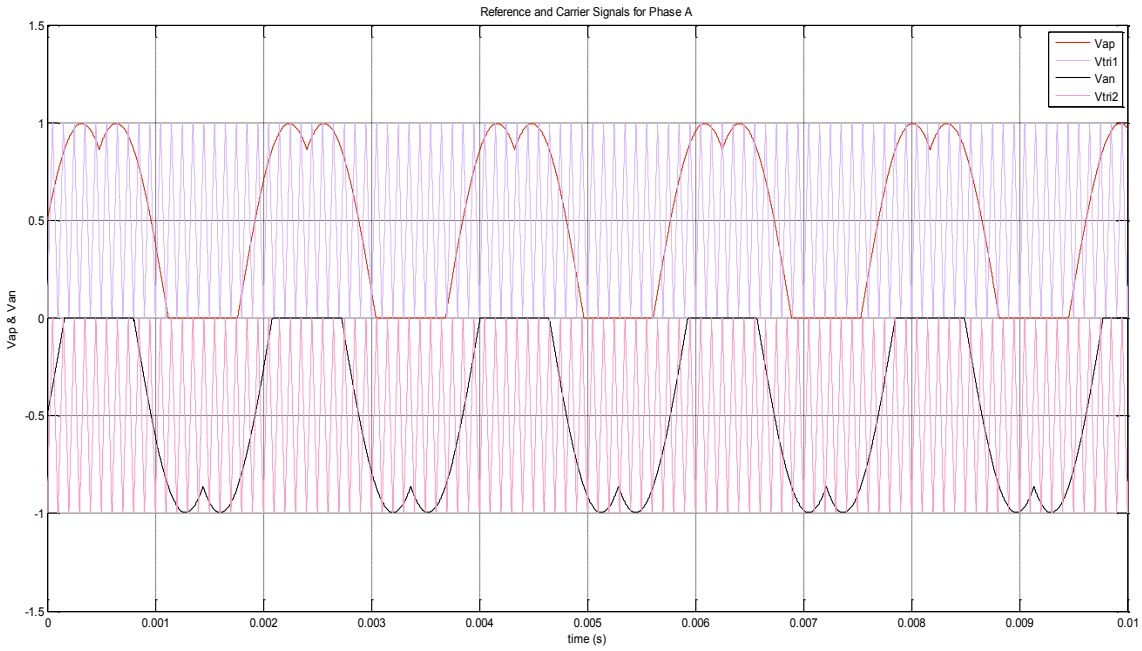


Figure 4.5: Positive and Negative Reference Signal for Phase 'A' of Three-level Inverter

In case of a three-level inverter, the decomposed signal having the middle voltage value which is connected to the "crucial" neutral-point of the DC-link may or may not be placed at an equal distance on the either side of the '0' axis. The position will now be governed by the amount of charge or discharge each component is now required to bring about for the two DC-link capacitors, in every switching period.

In order to obtain the three switching states (-1 0 1) for the three-level inverter, two switches could be turned-on at a time to obtain each switching states. Referring to Figure 3.2 from Chapter 3, switching state '1' can be obtained by turning on the switch pair S1

(T1/D1) and S2 (T2/D2), similarly, switching state ‘0’ can be obtained by turning on the switch pair S2 (T2/D2) and S3 (T3/D3), and finally, switching state ‘-1’ can be obtained by turning on the switch pair S3 (T3/D3) and S4 (T4/D4). The different ways to “turn-on” the switches in order to obtain the three switching states have been demonstrated as follows [31]:

Switch 1

- The positive reference signal is greater than the positive carrier
- The negative reference signal is greater than the negative carrier

Switch 2

- The positive reference signal is greater than the positive carrier
- The negative reference signal is greater than the negative carrier

  Or,

- The positive reference signal is lower than the positive carrier
- The negative reference signal is greater than the negative carrier

  Or,

- The positive reference signal is greater than the positive carrier
- The negative reference signal is lower than the negative carrier

Switch 3

- The positive reference signal is greater than the positive carrier
- The negative reference signal is lower than the negative carrier

Or,

- The positive reference signal is lower than the positive carrier
- The negative reference signal is greater than the negative carrier

Or,

- The positive reference signal is lower than the positive carrier
- The negative reference signal is lower than the negative carrier

Switch 4

- The positive reference signal is lower than the positive carrier
- The negative reference signal is lower than the negative carrier

The switches are turned-off if the conditions are not met.

Equation (3.39) in Chapter 3 for the average current (I_o) can be re-written as follows:

$$I_o = m_a(\omega t)\, i_a(\omega t) + m_b(\omega t)\, i_b(\omega t) + m_c(\omega t)\, i_c(\omega t)$$

$$I_o = (m_{ap} + m_{an})\, i_a + (m_{bp} + m_{bn})\, i_b + (m_{cp} + m_{cn})\, i_c \tag{4.5}$$

The above function results in zero average neutral-point current for every switching period, when a factor of '$\frac{1}{2}$' was employed for modification of the reference signals. However, the assumption that was made earlier regarding the ideality in switching device and high inductive load may or may not satisfy in a practical scenario. As a result of non-ideal conditions, especially in a three-level inverter, the neutral-point voltage deviates from zero and hence, one needs to use a factor that gets modified according to the variations or deviations from the expected outcome, thus accounting for any irregularities

that may be present. Therefore, instead of directly multiplying the modified signals with a factor '$\frac{1}{2}$' which does equal division, it is advisable to opt for a factor, say '*k*', and it's unity complement to serve the purpose. The factor '*k*' unlike the former ideal case, is a varying factor which should change its value depending on the deviation of the neutral-point voltage. Therefore, the compensating factor, *k*, can be obtained from a PI controller that is intended to control the difference between the DC-link capacitor voltages thus trying to maintain the voltage error as zero [32].

Mathematically, the modified reference signals can be obtained by introducing the control variable '*k*' which is applied in such a way that the output line-to-line voltages are not modified. The positive half of the reference signals are multiplied by the control factor '*k*' and the negative half of the reference signals are multiplied by the unity complement of the control factor 'k', i.e., '$1-k$'.

$$v_{ip,m} = k\left[v_i - \min\left(v_a, v_b, v_c\right)\right] \tag{4.6}$$

$$v_{in,m} = \left(1-k\right)\left[v_i - \max\left(v_a, v_b, v_c\right)\right]$$

where, i = a, b, c

5.2 PLANT MODEL OF THE DC-LINK IN THREE-LEVEL INVERTER

Now, for neutral-point current control using the traditional PI controller, the DC-link has to be modeled as a plant.

Also, the duty cycle is a ratio of maximum output voltage to the DC-link voltage, it can be noticed that the average value of the neutral-point current is a function of the output voltage. Hence,

$$I_o = \left(\frac{\hat{V}_a}{V_{dc}} I_a + \frac{\hat{V}_b}{V_{dc}} I_b + \frac{\hat{V}_c}{V_{dc}} I_c \right) \tag{4.7}$$

$$I_o = \frac{1}{V_{dc}} \left(\hat{V}_a I_a + \hat{V}_b I_b + \hat{V}_c I_c \right) \tag{4.8}$$

$$I_o = \left(\frac{\sqrt{2}}{V_{dc}} \right) \left(V_a I_a + V_b I_b + V_c I_c \right) \tag{4.9}$$

Since, the reference voltage signal has been decomposed into positive and negative components and each component can be represented in terms of the factor '*k*', the average output current can now be related to the factor '*k*' and the average output power (P_{avg}) as shown in Equation (4.9).

$$I_o = \left(\frac{1 - 2k}{V_{dc}} \right) P_{avg} \tag{4.10}$$

where, *k = control variable*

V_{dc} *= DC-link voltage (V)*

P_{avg} *= average, inverter output power (W)*

Hence, from Equation (3.25),

$$i_o = C\frac{d}{dt}\left(V_{C1} - V_{C2}\right)$$

Considering the average for one switching period,

$$\left\langle i_o \right\rangle_T = C\frac{d}{dt}\left\langle \Delta V_{dc} \right\rangle_T \tag{4.11}$$

Hence, comparing Equation (4.10) and Equation (4.11),

$$C\frac{d}{dt}\left\langle \Delta V_{dc} \right\rangle_T = \left(\frac{1-2k}{V_{dc}}\right) P_{avg} \tag{4.12}$$

Under steady state, the difference in voltage between the two capacitors is zero and therefore, $\Delta V_{dc} = 0$. When this happens, the right-hand side product also has to be equated to zero.

$$\left(1-2k\right)\left(\frac{P_{avg}}{V_{dc}}\right) = 0 \tag{4.13}$$

However, the quotient $\frac{P_{avg}}{V_{dc}}$ cannot be equal to zero under steady-state condition. Therefore,

$$1-2k = 0$$

$$k = \frac{1}{2} \tag{4.14}$$

Therefore, for the system to be in steady-state and to have voltages on both the DC-link capacitors equal, the control variable '*k*' should be maintained at 0.5. The linearized small signal model thus obtained is given by:

$$C\frac{d}{dt}\left(\tilde{v}_{dc}\right) = -\frac{2P_{avg}}{V_{dc}}\tilde{k} \tag{4.15}$$

Taking the Laplace Transform of the above equation for the change in the difference in capacitor voltage as a response to the control variable is given by:

$$\frac{\Delta\tilde{v}_{dc}(s)}{\tilde{k}(s)} = -\frac{2P_{avg}}{V_{dc}Cs} \tag{4.16}$$

5.3 CLOSED-LOOP FOR THE CONTROL OF NEUTRAL-POINT VOLTAGE DEVIATION

The linearized model of the DC-link can be obtained by introducing small signal perturbations around a DC operating point. The linearized small signal model can be obtained as follows:

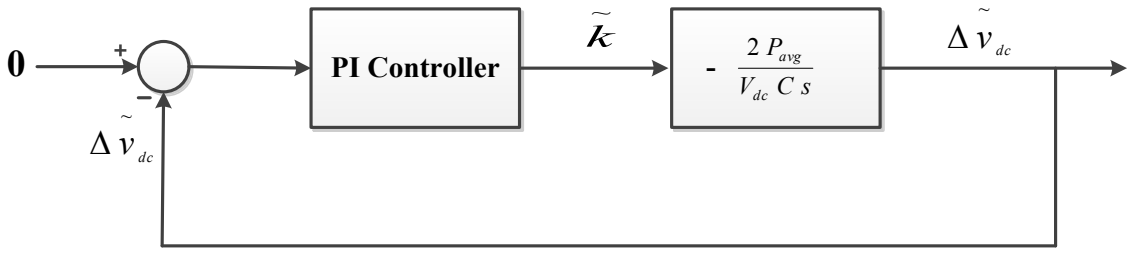


Figure 4.6: Closed-loop for the Neutral-Point Voltage Control

The transfer function of the PI controller is given as:

$$T_{f,PI}(s) = k_p + \frac{k_i}{s} \tag{4.17}$$

$$T_{f,PI}(s) = k_p \frac{T_i s + 1}{T_i s} \tag{4.18}$$

The transfer function of the plant can be given as:

$$T_{f,NPC}(s) = \frac{\Delta \tilde{v}_{dc}(s)}{\tilde{k}(s)} \tag{4.19}$$

$$T_{f,NPC}(s) = -\frac{2 P_{avg}}{V_{dc} C s} \tag{4.20}$$

The loop transfer function of the plant and the controller can be given as:

$$LTF_{NPC}(s) = T_{f,PI}(s) T_{f,NPC}(s) \tag{4.21}$$

$$LTF_{NPC}(s) = -k_p \left(\frac{T_i s + 1}{T_i s} \right) \left(\frac{2 P_{avg}}{V_{dc} C s} \right) \tag{4.22}$$

In order to determine the PI controller gains, the bode plot approach has been followed as shown in Figure 4.7. The step response of the system has been evaluated to determine the effectiveness of the controller during the dynamic step changes. This can be seen in Figure 4.8.

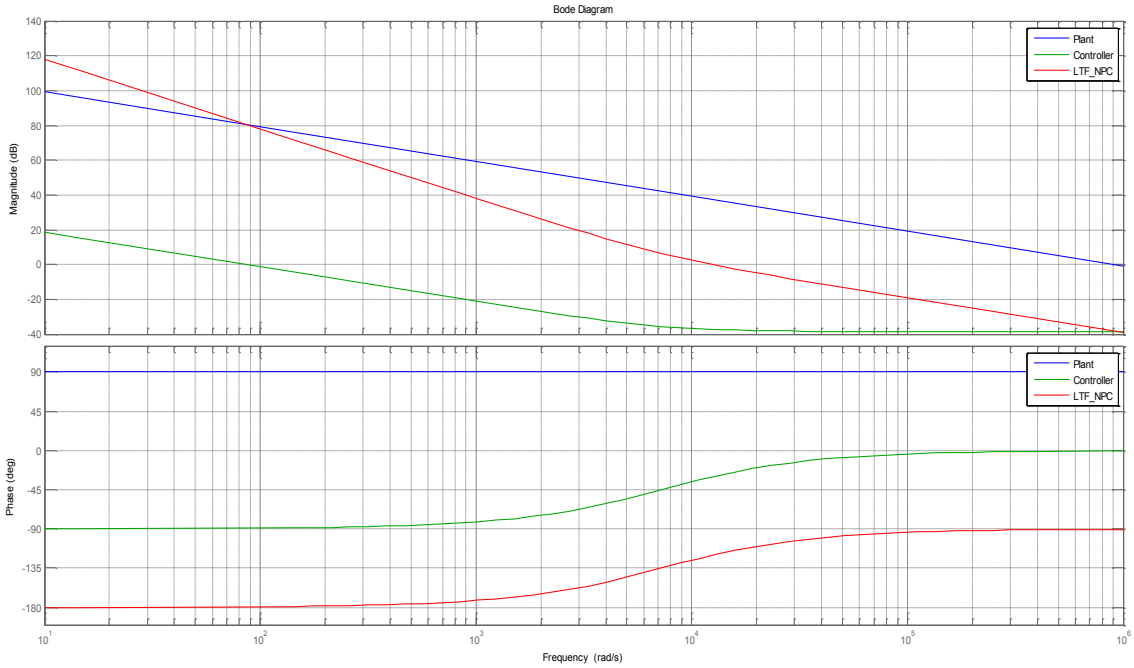


Figure 4.7: Bode Plot of the Loop Transfer Functions of the Plant and Controller

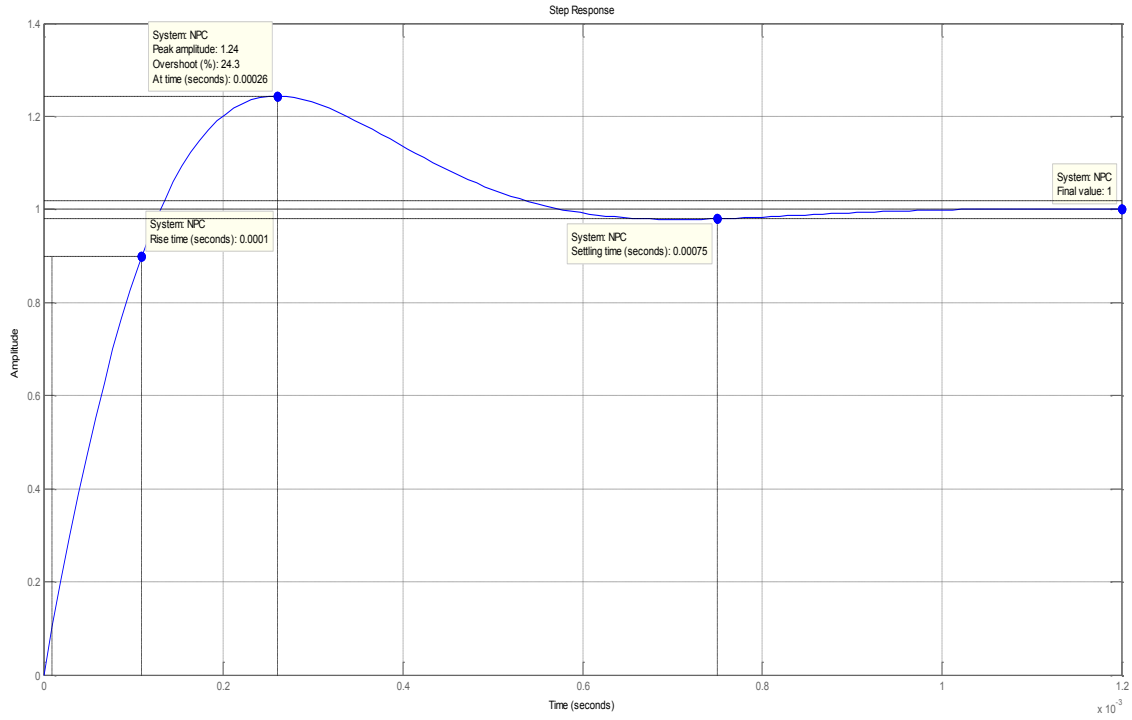


Figure 4.8: Step Response of the Closed Loop Transfer Function for Neutral-Point Control

4.4 SIMULATION BASED TESTS OF THE BALANCING CONTROLLER FOR VARIOUS OPERATING CONDITIONS

A few tests conditions have been simulated to determine the response of the voltage balancing efforts demonstrated by the controller thus developed. The first test highlights the response and the effectiveness of the voltage balancing control with changes in modulation index, the fundamental output frequency and the variation in RL-load connected to the output of the three-level inverter which is supplied by a DC-link of 600 V. The results of the test has been shown in Figure 4.9 where (a) describes the step increase in the modulation index value at specific intervals starting from a low value to a high value, (b) describes the changes in the output fundamental frequency: the changes include increase, decrease and also the ramp increase, from a low value up to a high value. Figure 4.9 (c) describes the voltages across the DC-link capacitors for the capacitors of 700 μF each, and Figure 4.9 (d) shows that the percentage error between the two capacitor voltages is well limited to $\pm 2\%$.

Similarly, the voltage balancing in case of regenerative operation mode is tested. In this case, both the capacitors (700 μF each) consist of large discharge resistors, 10 kΩ across the upper DC-link capacitor and 15 kΩ across the lower DC-link capacitor respectively. The three-phase inverter is connected to an A.C. grid with the same fundamental frequency of operation. From Figure 4.10, it can be observed that due to the presence of large, unbalanced discharge resistors across the DC-link capacitors, at the starting the voltage difference across the capacitors goes up to a maximum of 18%, however, the initial transients die down and the steady-state balance condition is reached in 0.05 s.

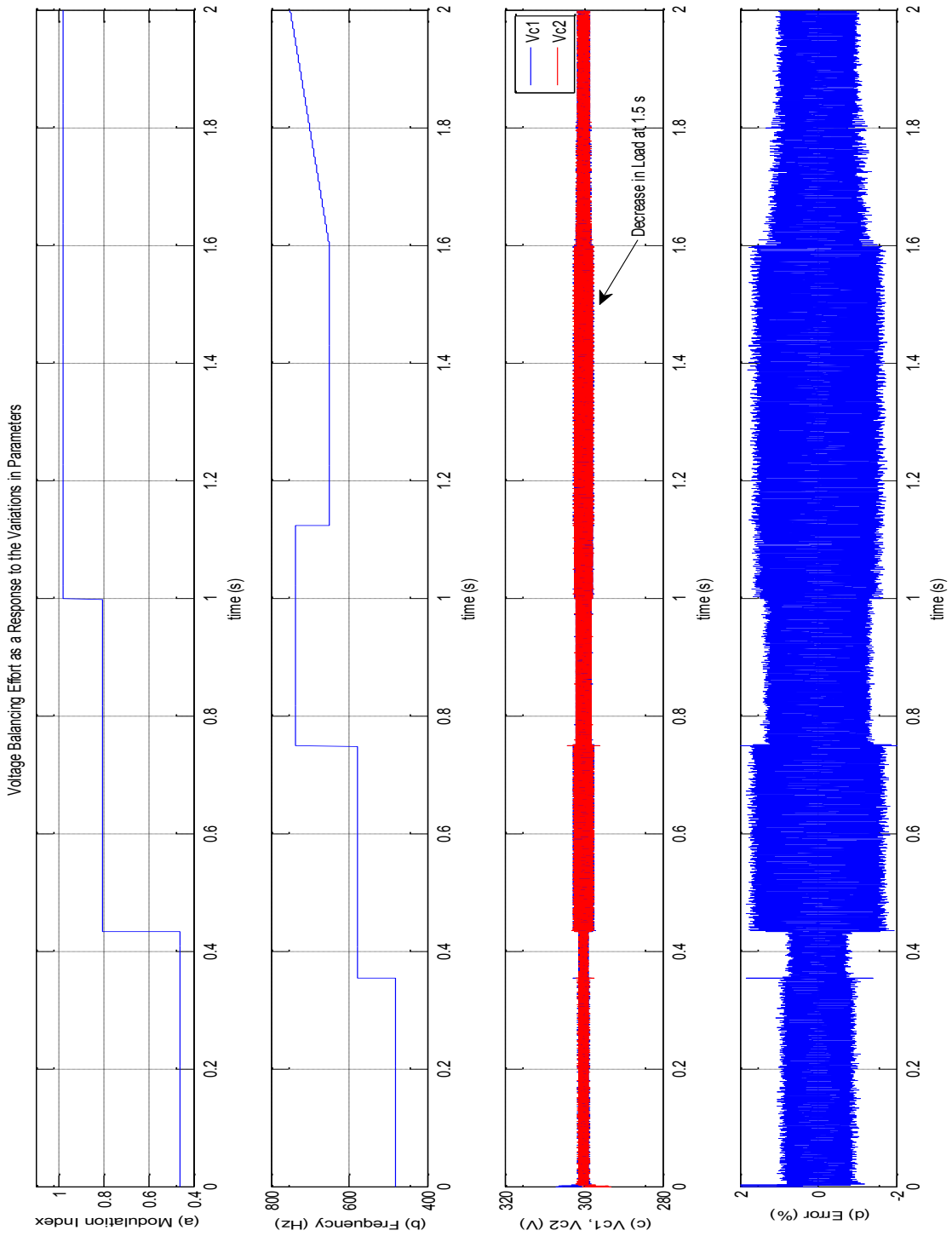


Figure 4.9: Balancing Effort of the Capacitors as a Response to the Variation in (a) Modulation Index, (b) Fundamental Output Frequency, (c) Voltages across the DC-link Capacitors, and (d) Percentage Error between the two DC-link Capacitor Voltages

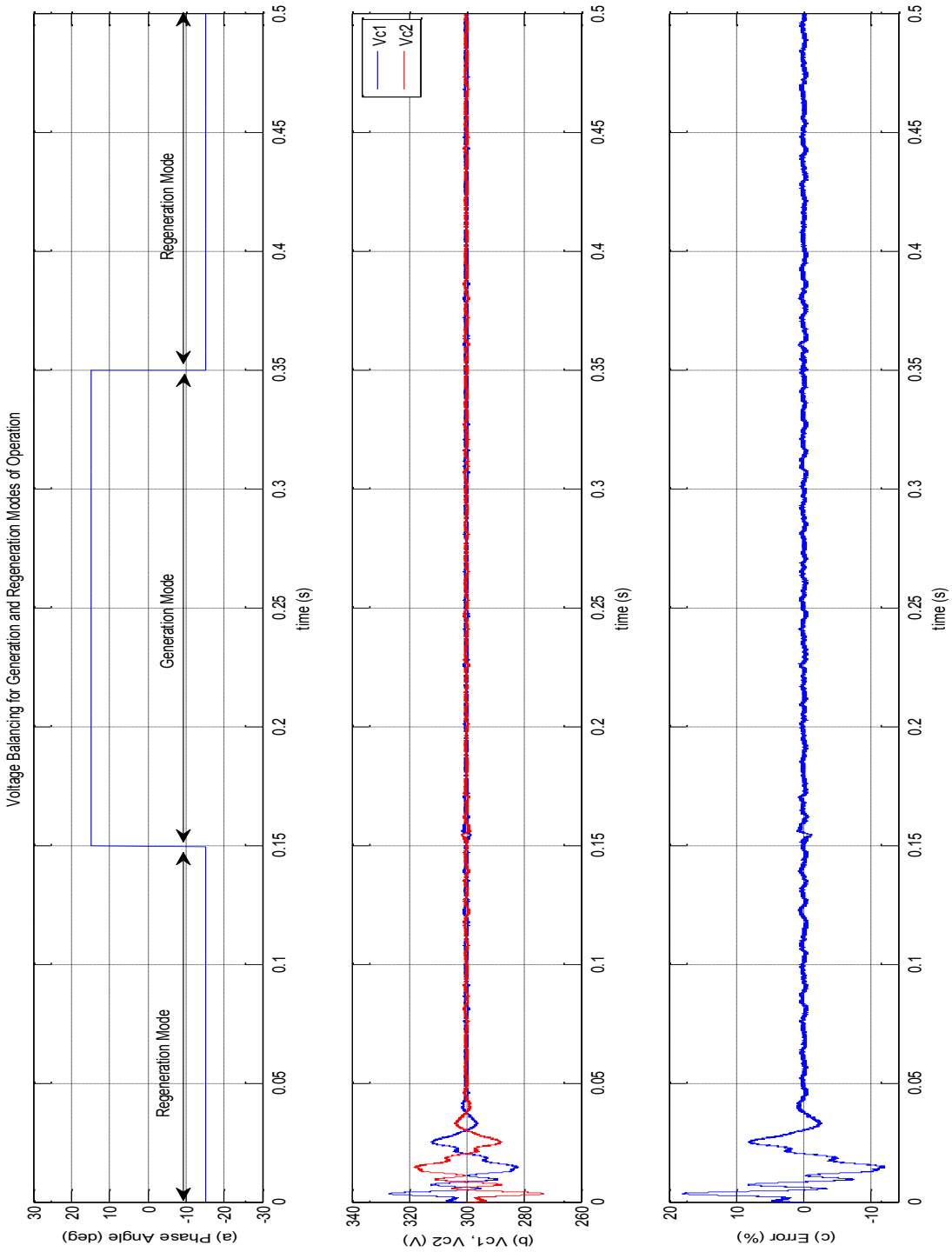


Figure 4.10: Voltage Balancing Effort for (a) Generation and Regeneration Modes of Operation, (b) Voltages across the DC-link Capacitors, and (c) Percentage Error Between the two DC-link Capacitor Voltages

4.5 CLOSED-LOOP ANALYSIS FOR THE NEUTRAL-POINT VOLTAGE BALANCING CONTROLLER WITH PMSM DRIVE

The voltage balancing capability has been tested with the PMSM drive introduced in Chapter 2 utilizing the Field-Oriented Control technique discussed. The drive has been tested for changes in torque and speed and the associated waveforms have been presented in Figure 4.11 for the transient region of operation of the drive.

Similarly, the drive has again been tested for changes in torque and speed and the associated waveforms have been presented in Figure 4.12, for the transient region of operation of the drive.

Hence, the effectiveness of the DC-link voltage balancing has been demonstrated for different operating conditions.

The carrier-based modulation strategies for the two and three-level inverters have been presented and they can be summarized in the form of a flow chart as shown in the following section.

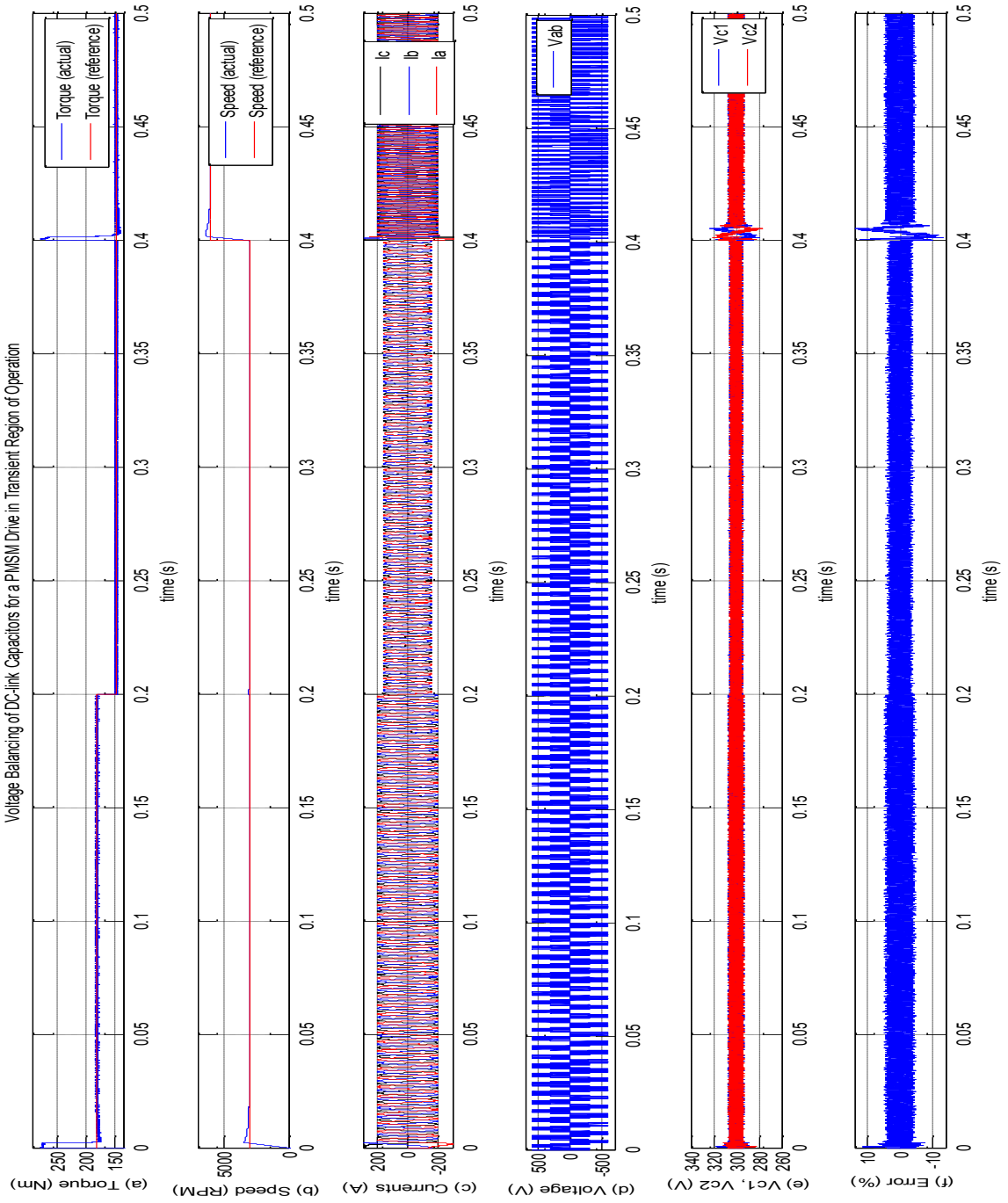


Figure 4.11: (a) Actual and Reference Torque, (b) Actual and Reference Speed, (c) Three Phase Inverter Output Current, (d) Line-to-line Output Voltage of the Inverter, (e) Voltages across the DC-link Capacitors, & (f) Percentage Error between the DC-link Capacitors

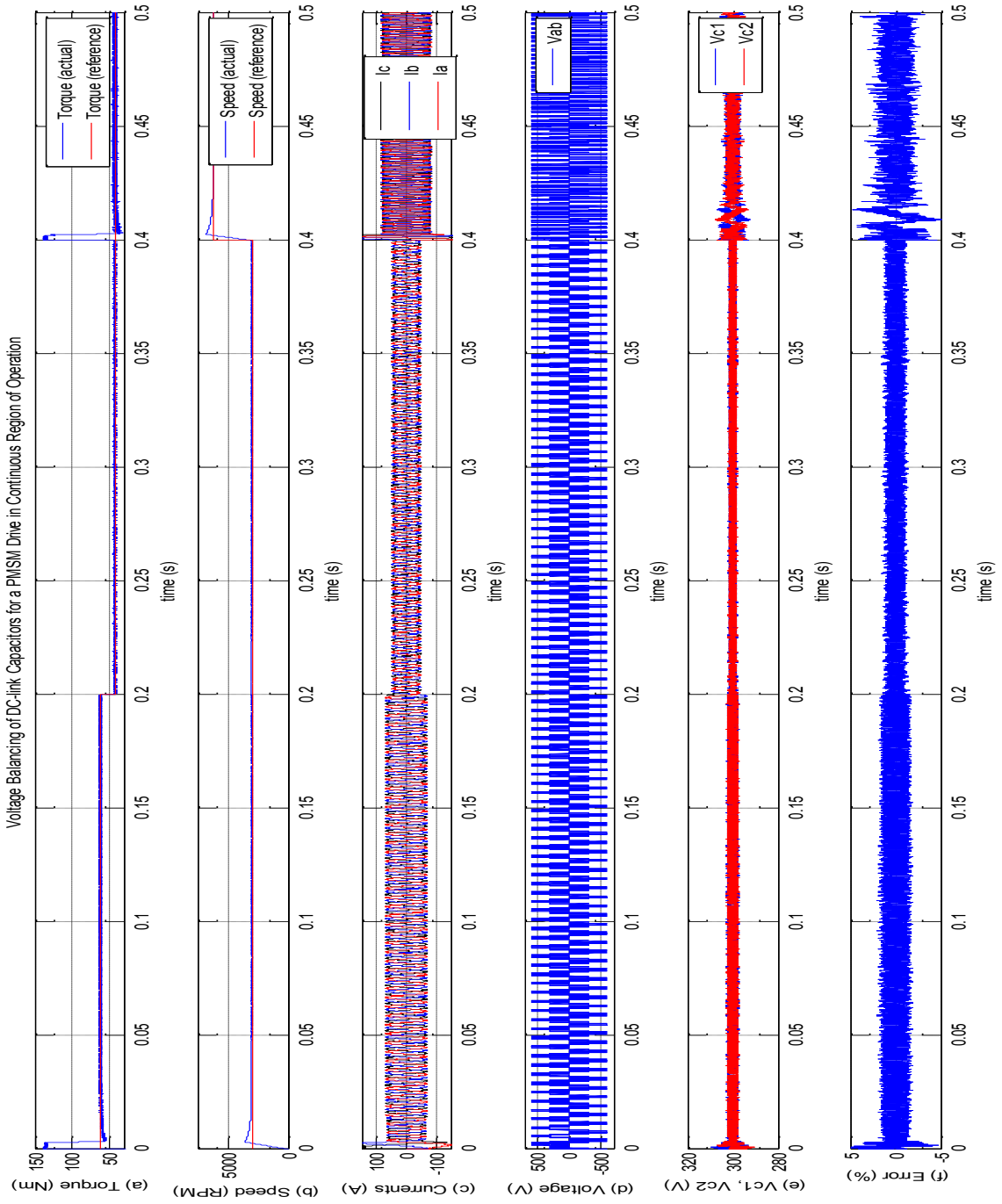


Figure 4.12: (a) Actual and Reference Torque, (b) Actual and Reference Speed, (c) Three Phase Inverter Output Current, (d) Line-to-line Output Voltage of the Inverter, (e) Voltages across the DC-link Capacitors, & (f) Percentage Error between the DC-link Capacitors

4.6 FLOW CHART FOR CARRIER-BASED SPACE VECTOR MODULATION OF TWO AND THREE-LEVEL INVERTERS

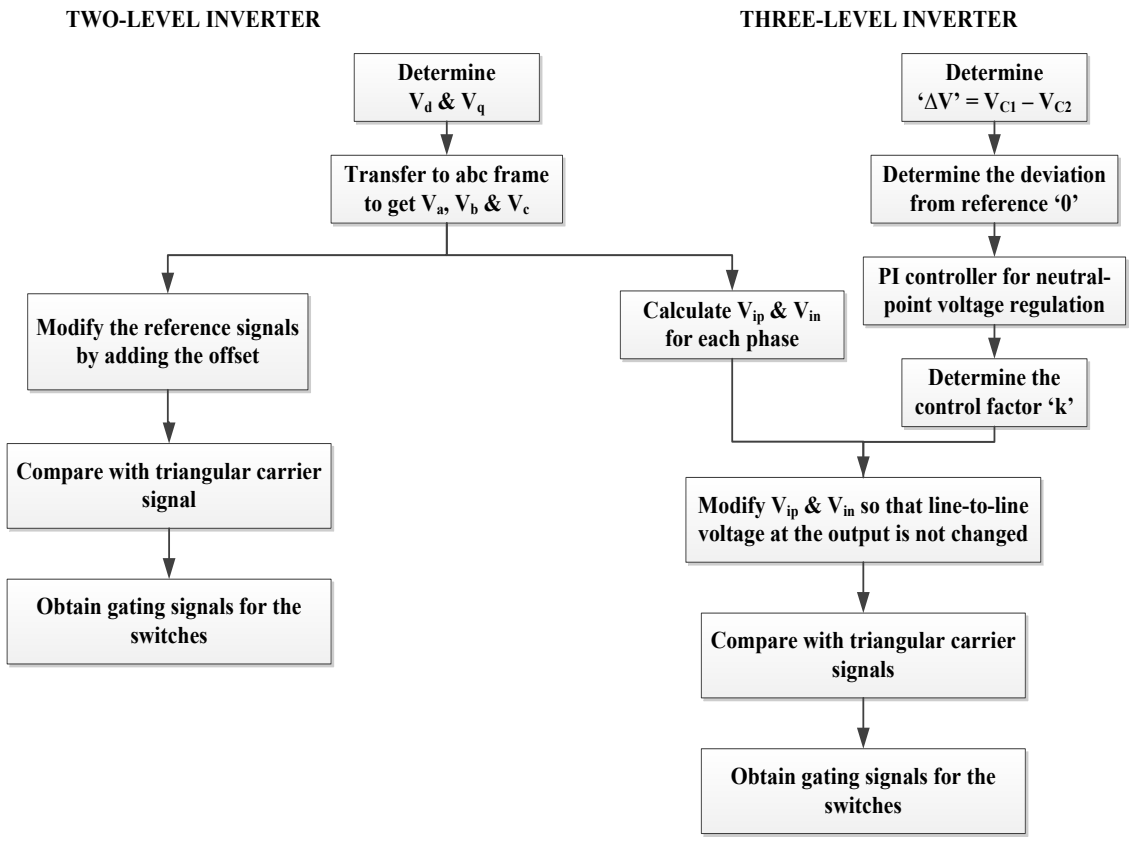


Figure 4.13: Flow Chart for CB-SVM of Two and Three-level Inverters

4.7 THD COMPARISON FOR TWO AND THREE-LEVEL INVERTERS

In the present project, the main concern is to have a reduced total harmonic distortion (THD) of operation (switching frequency is not an issue as long as the junction temperatures of the devices are well within the limits, as discussed in Chapter 3). Therefore, the total harmonic distortion of the line-to-line voltage for the two and three-level inverters using the Carrier-based Space Vector Modulation technique have been presented.

The Fast Fourier Transform of the Line-to-line output voltage of the inverters for DC-link voltage (V_{dc}) = 600 V, modulation index (m) = 0.43, fundamental output voltage frequency (f) = 250 Hz, switching frequency (f_{sw}) = 6 kHz, and for the same machine have been presented in Figure 4.14 for the two-level inverter and in Figure 4.15 for the three-level inverter.

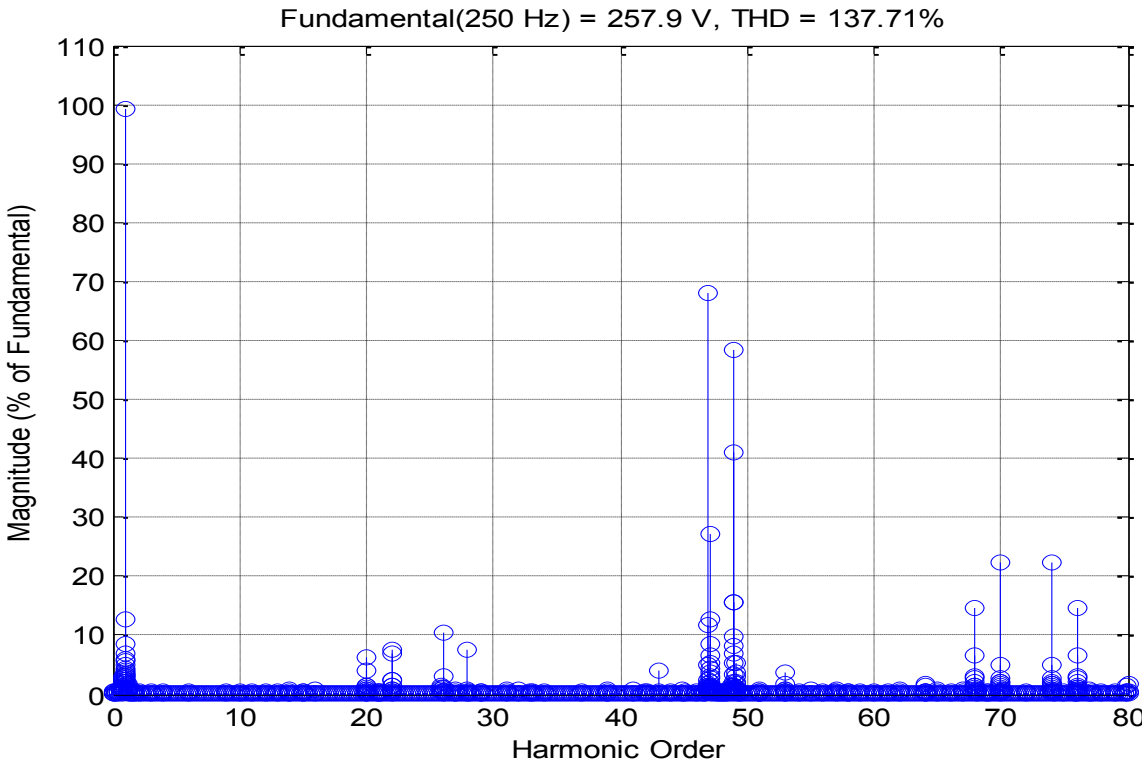


Figure 4.14: Line Voltage THD for Two-level Inverter with CB-SVM

It can be seen from Figure 4.14 and Figure 4.15 that in case of CB-SVM, the harmonics are eliminated and only the side-band harmonics are present, due to the addition of the min-max signals to the reference signals. The min-max signal is in effect a zero sequence signal which is composed by odd triple harmonics and the harmonics are eliminated in the line-to-line voltage as expected. However, it can been seen that the THD in case of

two-level inverter is almost double when compared to the case in three-level inverter. Alternately, if reduction of switching frequency is the criterion, THD value for three-level inverter equivalent to that in two-level inverter can be obtained for a much lower switching frequency of operation in case of the three-level inverter.

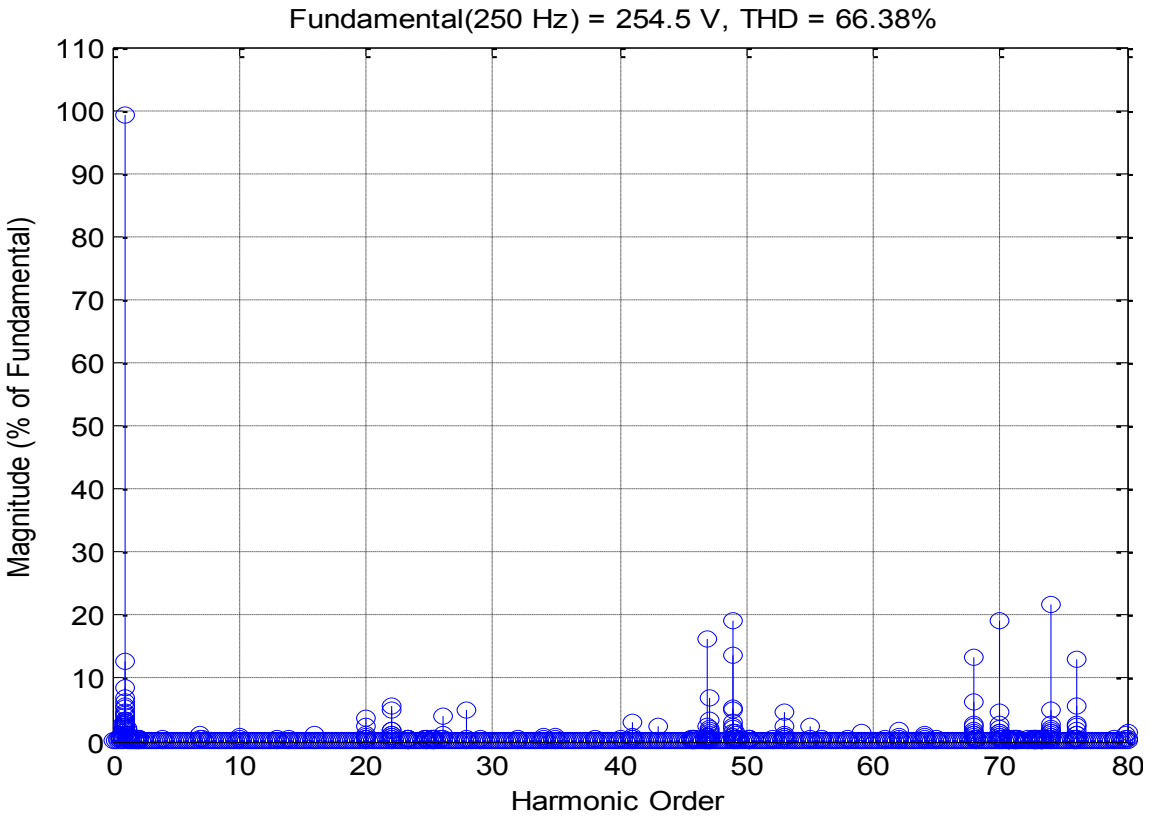


Figure 4.15: Line Voltage THD for Three-level Inverter with CB-SVM

In order to further reduce the THD, another modulation method will be investigated in the chapter that follows.

In order to compare the switching frequencies, the THD of current is considered to be the base value. For example, considering the operating conditions: power = 26 kW, torque = 61 Nm, current = 67.9 A, modulation index = 0.53 and power factor = 0.94. For these

values, the THD of current for two-level inverter at 26.5 kHz switching frequency (ensuring that the junction temperature limits of the switching devices are not violated), the THD of current at the output of the inverter is found to be 2.27%. In order to obtain the equivalent current THD using a three-level inverter, a switching frequency of only 8.5 kHz is sufficient. Hence, there is a reduction in the switching frequency of operation of about 68%.

The current THD spectrum for above conditions can be observed in Figure 4.16 for a two-level inverter and in Figure 4.17 in case of the three-level NPC inverter.

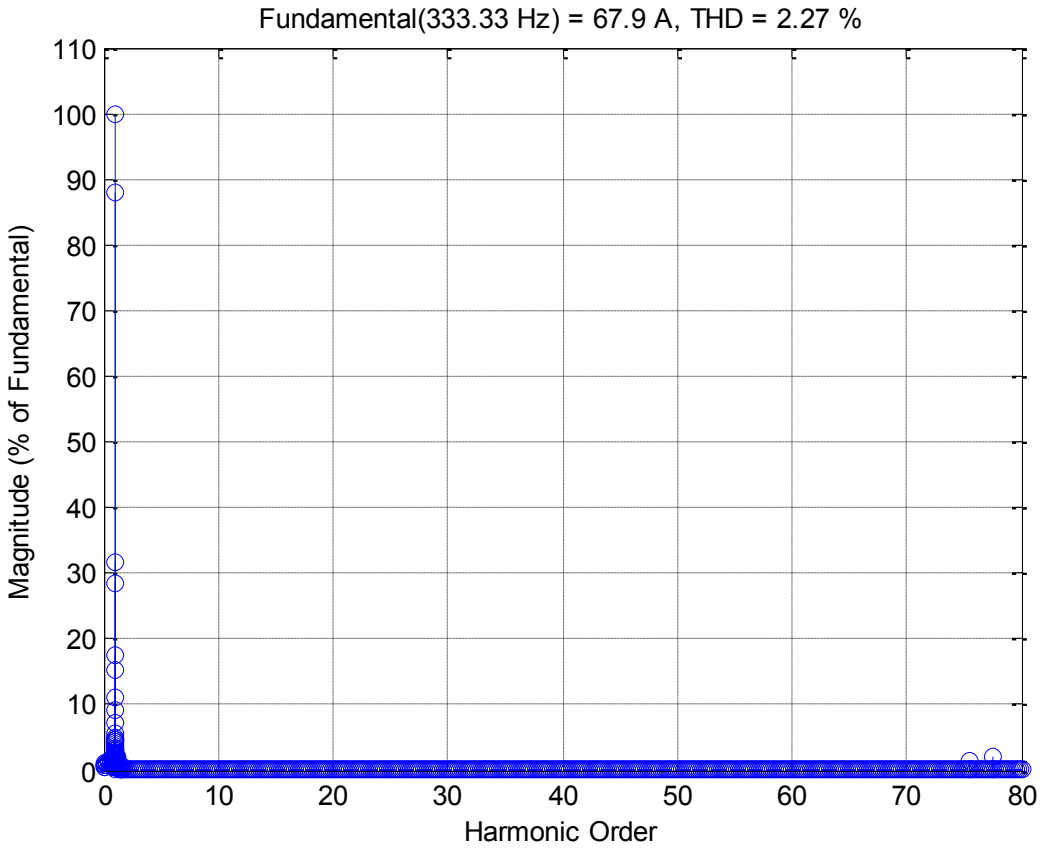


Figure 4.16: Output Current THD for Two-level Inverter at Switching Frequency of 26.5 kHz

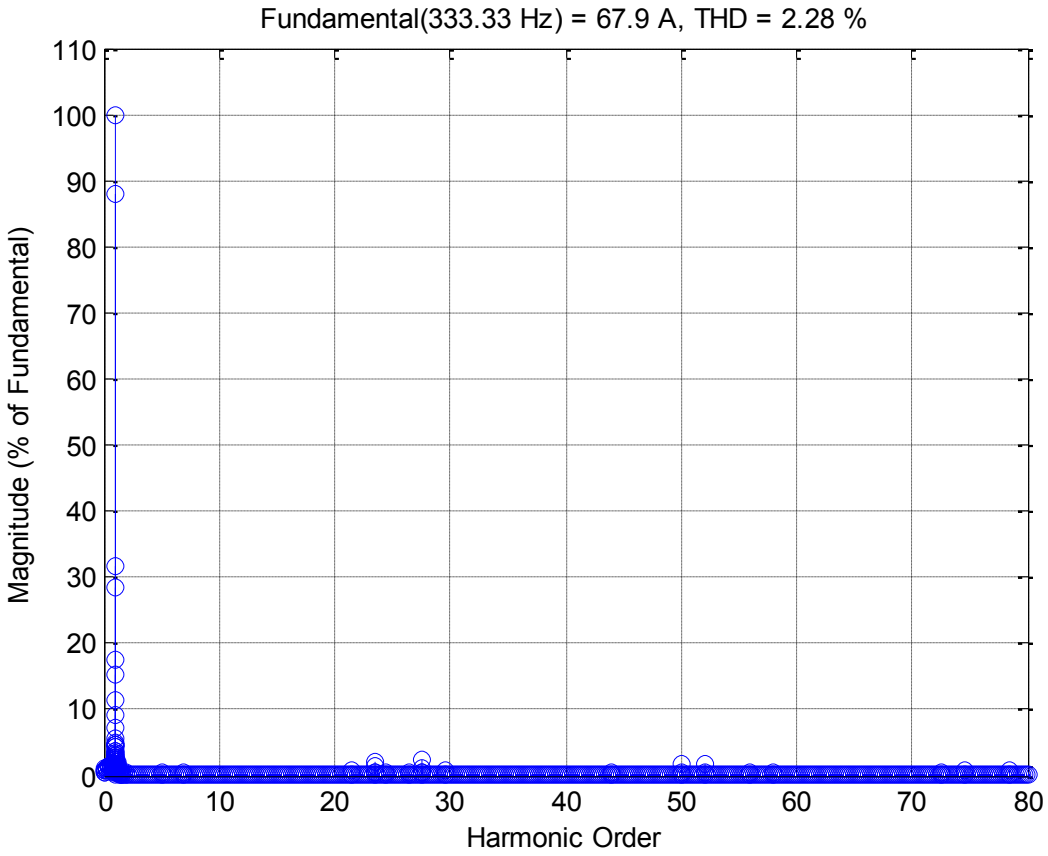


Figure 4.17: Output Current THD for Three-level NPC Inverter at the Switching Frequency of 8.5 kHz using CB-SVM

At these switching frequencies for each inverter, other performance parameters like losses and efficiencies of both the inverters can be evaluated and thus compared. From Figure 4.18, the individual losses occurring in a two-level inverter have been shown and total losses in this inverter is found to be 2381.16 W, for the same conditions of operation mentioned above. Similarly, the loss distribution in case of the three-level inverter can be found in Figure 4.19 and the total loss amounts to be 579.60 W. Therefore, there is a reduction in losses when a three-level NPC inverter is used (for the same THD of output current). The efficiencies thus evaluated in case of two-level and three-level inverters are

found to be 91.22% and 97.71%, respectively, thus providing an increase in three-level inverter efficiency of about 7%.

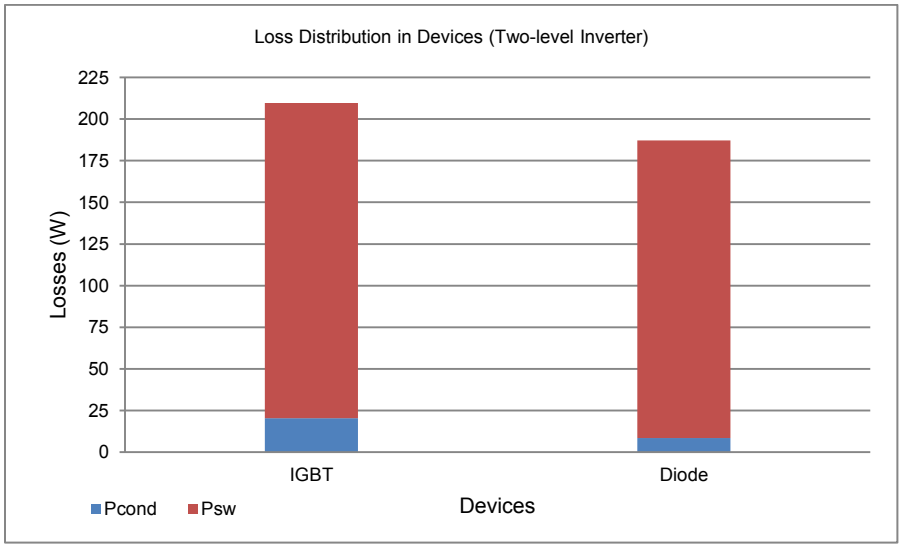


Figure 4.18: Loss Distribution in Two-level Inverter

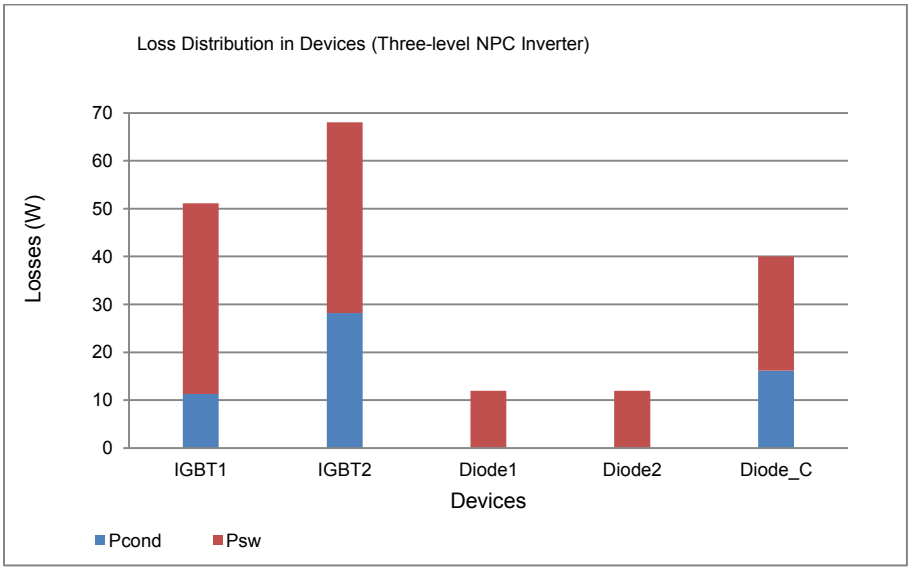


Figure 4.19: Loss Distribution in Three-level Inverter

CHAPTER 5: SPACE VECTOR PULSE WIDTH MODULATION

5.1 INTRODUCTION

The present chapter demonstrates the Space Vector Pulse Width Modulation methods for two- and three-level inverters. In case of the three-level inverter, the issue of neutral-point balancing by modifying the modulation scheme while using the voltage unbalance information has been addressed.

5.2 SPACE VECTOR PULSE WIDTH MODULATION

The reason for considering Space Vector Modulation strategy is due to the presence of lower order harmonics in the modulation method considered in Chapter 4. The lower order harmonics are non-desirable as they are difficult to filter out by the machine inductances.

Space Vector Pulse Width Modulation (SVPWM) has become a widely-preferred method for the modulation of the switches in the converters due to its easy applicability and the ease with which various criteria could be addressed just by the modification of the switching patterns. Also, it offers a high linear range of modulation and low load current ripple. The idea behind Space Vector Modulation will briefly be introduced for both two and three-level inverters and the need for modification of the switching time for the control of neutral-point voltage balance will be addressed in case of the three-level inverter.

5.2.1 SPACE VECTOR PULSE WIDTH MODULATION FOR TWO-LEVEL INVERTER

In case of a two-level inverter where only two switches are present in an inverter phase leg, each switch can have two states: 1 or 0, pertaining to whether it is on or off. As the two switches in each inverter pole conduct in a complementary manner, it is sufficient to demonstrate only for one switch and hence the upper switch in each leg will be considered. Since the present study concentrates only on a 3-φ inverter, there will be a total of 8 (i.e., 2^3) switching states. Of these 8; 6 are termed the "active" states and the remaining 2 are called the "zero" states. The "active" states represent the case where either two of the high-side switches and one of the low-side switches conduct, or vice-versa. The "zero" states represent the case when all three upper or lower switches in the poles are simultaneously turned-on, thus giving zero output voltage of the inverter.

The switching states of the inverter have been represented by using a 3-bit switching word where the most-significant bit (MSB, the 1^{st} bit) represents leg A of the inverter, the 2^{nd} bit stands for the leg B of the inverter and the least-significant bit (LSB, the 3^{rd} bit) represents the leg C of the inverter. When a particular bit is '1', the high-side switch of that leg is on and '0' for a particular bit indicates that the low-side switch of that particular leg is on. Therefore, switching word (101) would represent the conduction of high-side switches of legs A and C and the low-side switch of leg B.

When three-phase balanced sinusoidal voltages are applied to the windings of a three-phase AC machine, six discrete time instants can be observed during each time period of the phase voltages. These time instants are realized when one of the phase voltages have maximum positive or negative instantaneous magnitude; as shown in Figure 5.1.

Referring to Figure 5.1 and considering one time period of phase A voltage, V_a, there are six instants (two each for all the three phases) when one of the three phases has maximum positive or negative instantaneous magnitude. At these instants, the resultant of the three space-voltages can be denoted by V_1 through V_6.

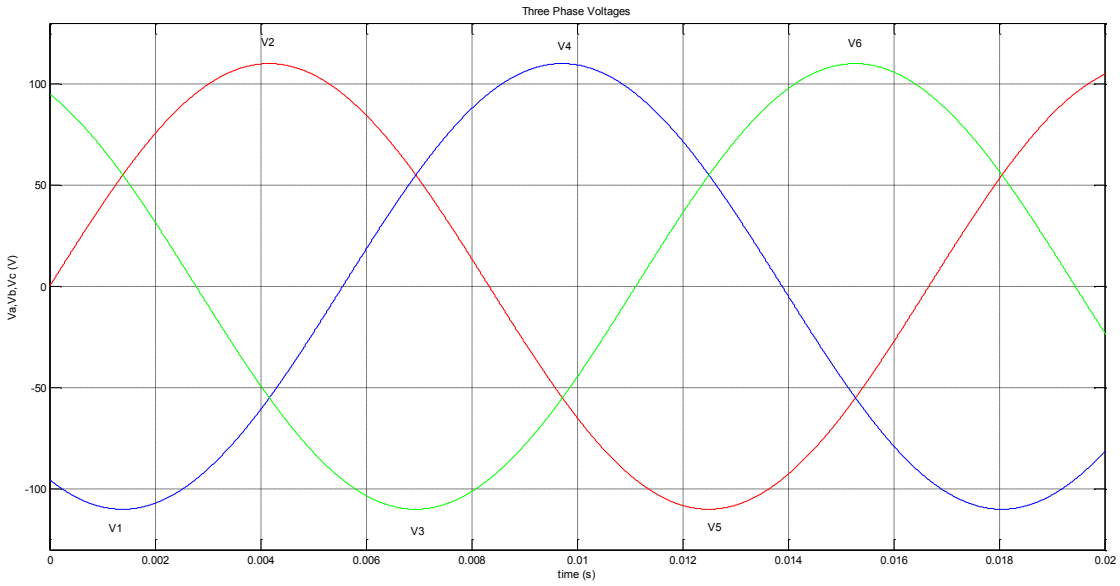


Figure 5.1: Three-Phase Balanced Voltage Supply

Referring to Figure 5.1 and considering one time period of phase A voltage, V_a, there are six instants (two each for all the three phases) when one of the three phases has maximum positive or negative instantaneous magnitude. At these instants, the resultant of the three space-voltages can be denoted by V_1 through V_6.

The continuously varying sinusoidal waveforms shown in Figure 5.1, result in a space voltage vector of fixed magnitude that is rotating at fixed (or synchronous) speed in the space. However, a practical inverter cannot produce perfectly ideal sinusoidal three-phase voltages as the inverter outputs are obtained from rectangular pole voltages and they

contain harmonic voltages apart from the desired fundamental. This being said, the instantaneous magnitudes of the inverter outputs and the sinusoidal voltages can be made to match at the six discrete instants of the output cycle, as mentioned earlier. Since an inverter cannot produce ideal sinusoidal three-phase voltages, the resultant space vector also cannot move smoothly in space with constant magnitude and constant angular speed. It is because when an inverter switches from one active state to another, the resultant voltage space vector changes its direction quite abruptly. This abrupt change in direction is in multiples of 60 electrical degrees. The basic idea of SVPWM is to compensate the required volt-seconds using discrete switching states and their respective on-times, i.e., the output voltage space vector is expressed as a weighted-average combination of two adjacent active space vectors and one of the two zero space vectors.

In order to have a near-sinusoidal voltage waveform, a standard SVPWM technique aims to get rid of the low frequency harmonic components from the output voltage by using two active vectors that are adjacent to the reference voltage vector and an adjacent zero vector, during each switching period.

The aforementioned discrete switching states can be represented in terms of a hexagon containing six sectors, the vertices of which denote the six active switching states and the center represents the two zero states [330]

]; as shown in Figure 5.2.

While the active state voltage vectors ($V_1 - V_6$) have a magnitude of V_{dc} pointing along the fixed directions, the null state voltage vectors (V_7 and V_8) have zero magnitude placed at the origin of the voltage space plane.

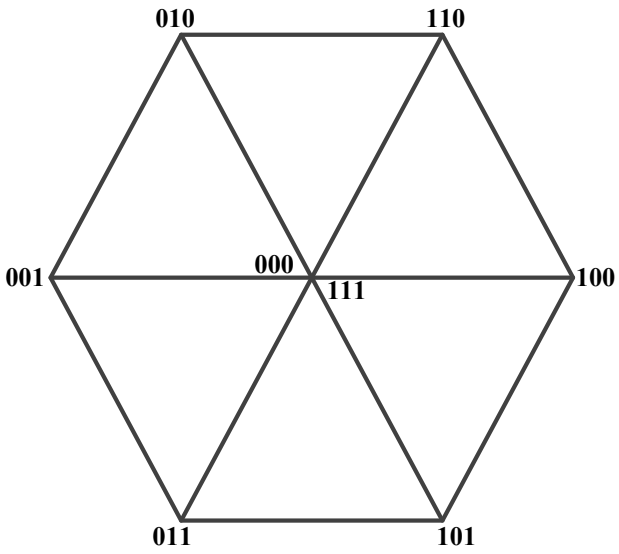


Figure 5.2: Output Voltage Space Vectors of a Three-Phase Two-level Inverter

While determining the switching time of the voltage vectors, each reference vector present in any sector can be represented on the αβ-plane as shown in Figure 5.3.

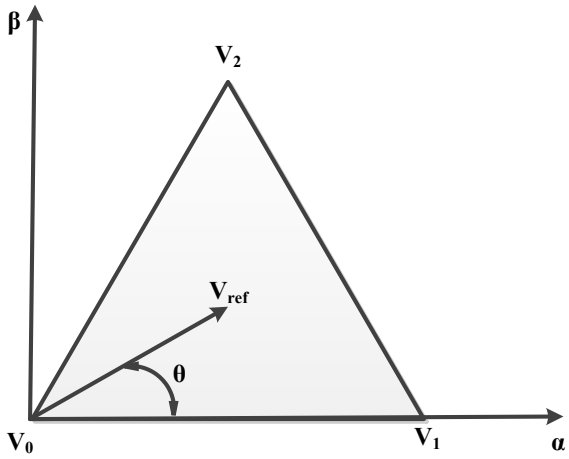


Figure 5.3: Sector 1 of a Two-Level Inverter

As mentioned earlier, the dwell time for each state in the inverter leg can be evaluated from the equations that follow:

$$T_1 V_1 + T_2 V_2 + T_0 V_0 = T_s V_{ref} \tag{5.1}$$

$$T_1 + T_2 + T_0 = T_s \tag{5.2}$$

$$V_{ref} = \left| V_{ref} \right| e^{j\theta} \tag{5.3}$$

The three equations mentioned above have to be solved in order to calculate the dwell times of the switching state vectors. Depending on the sector and the triangle, the magnitudes of vectors V_1, V_2 and V_0 have to be used as appropriately as seen in Table 5.1.

Sector	Switching Vectors	Switching Times
1	$V_0 = 0$ $V_1 = \frac{2}{3} V_{dc}$ $V_2 = \frac{2}{3} V_{dc} e^{j60^\circ}$	$T_0 = T_s - T_1 - T_2$ $T_1 = T_s \left[\left(\frac{\sqrt{3}}{2} \right) m_a \right] \left\{ \cos\theta - \sin\left(\frac{\theta}{\sqrt{3}} \right) \right\}$ $T_2 = T_s \left(m_a \sin\theta \right)$

Table 5.1: Switching Times for Two-Level Inverter

5.2.2 SPACE VECTOR PULSE WIDTH MODULATION FOR THREE-LEVEL INVERTER

In case of three-level inverter modulation, one can easily extend the concept of two-level SVPWM for the three-level inverter. It follows the same approach but the only difference is the increased number of total switching state vectors as each leg now has the three states (-1, 0, 1) to represent. Hence, there will be a total of 27 (i.e., 3^3) switching states possible for the three-phase, three-level inverter. Similarly, 27 switching vectors are further subdivided into zero, small, medium and large space vectors making them 19 different states (6 states for 6 large vectors, 6 states for 6 medium vectors, 6 states for 6

redundant pairs of small vectors and 1 state for 3 redundant zero vectors) [34]. The hexagon pertaining to the three-level inverter and representing all the possible 27 switching states has been depicted in Figure 5.4.

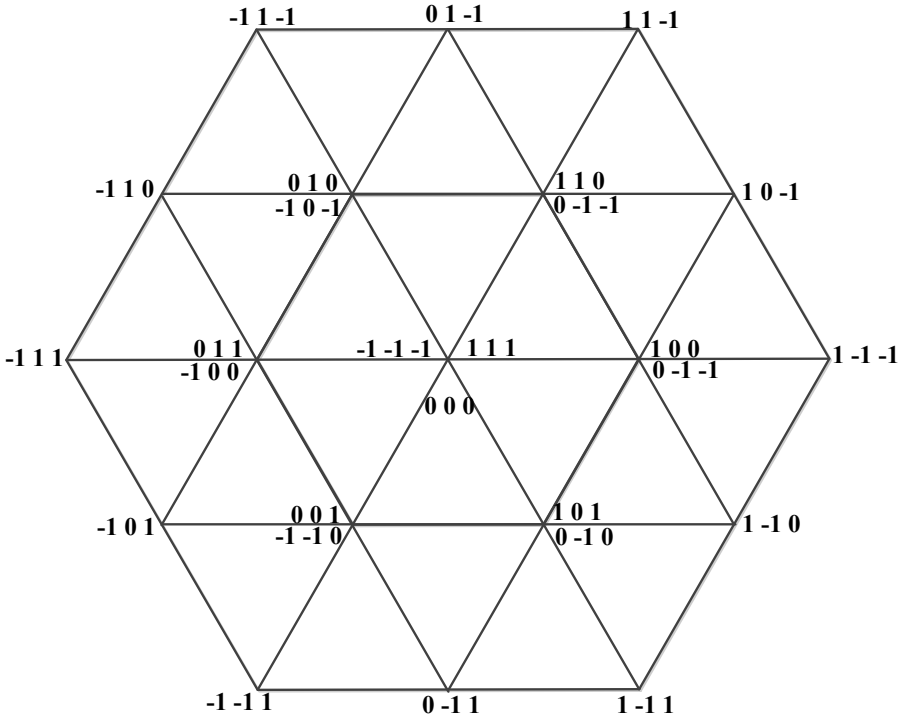


Figure 5.4: Output Voltage Space Vectors of a Three-Phase Three-level Inverter

The zero vectors (magnitude '0') are present at the center of the hexagon while the small vectors (magnitude '$\frac{1}{3}$') are the ones that are present in pairs at the vertices of the inner hexagon. The medium vectors (magnitude '$\frac{1}{\sqrt{3}}$') are the ones that lie in between the mid-points of the two consecutive vertices of the outer hexagon and the large vectors (magnitude '$\frac{2}{3}$') are those that are present at the vertices of the outer hexagon. All the

magnitudes mentioned have been normalized by the DC-link voltage magnitude. The reference vector rotates as mentioned in case of the SVPWM for two-level inverter. However, in case of the three-level SVPWM, the sectors are subdivided into four smaller triangles contained in each of them, making a total of 24 sub-triangles for the hexagon.

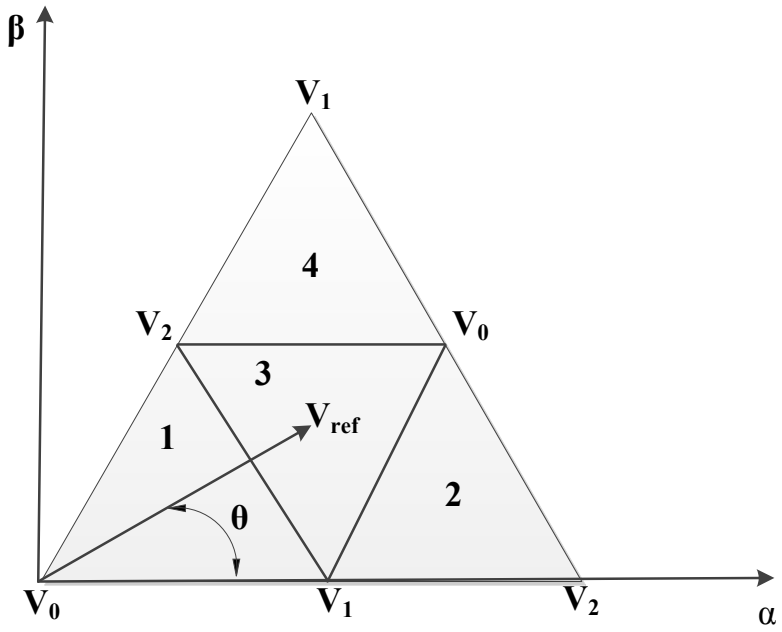


Figure 5.5: Sector 1 of a Three-Level Inverter

Similar to the case of the two-level inverter, the dwell time for each state in the three-level inverter can be evaluated using the equation set. After solving the equations for each position of the reference vector, one can obtain the switching times as enlisted in Table 5.2. Depending on the requirement, the sequence in which the switching states are selected would vary. Generally, in case of a two-level inverter, designers prefer to choose the switching sequence for minimum switching losses or minimum harmonic distortion, but in case of the three-level inverter, balancing the DC-link capacitor voltages is the principal criterion.

Triangle Number	Switching Vectors	Switching Times
1	$V_0 = 0$ $V_1 = \frac{1}{3}V_{dc}$ $V_2 = \frac{1}{3}V_{dc}e^{j60°}$	$T_0 = T_s\left[1-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$ $T_1 = T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$ $T_2 = T_s\left[2m_a\sin\theta\right]$
2	$V_0 = \frac{1}{\sqrt{3}}V_{dc}e^{j30°}$ $V_1 = \frac{1}{3}V_{dc}$ $V_2 = \frac{2}{3}V_{dc}$	$T_0 = T_s\left[2m_a\sin\theta\right]$ $T_1 = T_s\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$ $T_2 = T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$
3	$V_0 = \frac{1}{\sqrt{3}}V_{dc}e^{j30°}$ $V_1 = \frac{1}{3}V_{dc}$ $V_2 = \frac{1}{3}V_{dc}e^{j60°}$	$T_0 = T_s\left[2m_a\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$ $T_1 = T_s\left[1-2m_a\sin\theta\right]$ $T_2 = T_s\left[1-2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$
4	$V_0 = \frac{1}{\sqrt{3}}V_{dc}e^{j30°}$ $V_1 = \frac{2}{3}V_{dc}e^{j60°}$ $V_2 = \frac{1}{3}V_{dc}e^{j60°}$	$T_0 = T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$ $T_1 = T_s\left[2m_a\sin\theta-1\right]$ $T_2 = T_s\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$

Table 5.2: Switching Times of a Three-Level Inverter

where, $m_a = \sqrt{3}\frac{V_{ref}}{V_{dc}}$

5.3 NEUTRAL-POINT VOLTAGE BALANCING WITH SVPWM FOR THREE-LEVEL INVERTER

The three-level inverter operated in an open-loop mode with regular SVPWM does not cater to the inherent requirement of neutral-point voltage balancing issue. Though the zero vectors and the large vectors do not contribute to the neutral-point variation, the small vectors that are present in pairs and the medium vectors affect the neutral-point voltage potential.

The positive small vector (switching state vector consists of 1 and 0) increases the neutral-point voltage potential while the negative small vector (switching state vector consists of -1 and 0) reduces the neutral-point voltage potential; during the motoring operation of the machine and vice-versa occurs during the regenerative operation of the machine. In case of the medium vector (switching state vector consists of -1, 0 and 1), the effect it would present on the neutral-point potential cannot be predicted without knowing the circuit condition.

All the small triangles that can be seen in Figure 5.5 contain at least one pair of small vectors. Therefore, if one can regulate the on and off times of these pairs in a switching period, so that the dwell time for small vector is redistributed between the positive small vector and the negative small vector of the pair [35]. In this way, the increase in neutral-point potential caused by positive small vector can be regulated back by using the negative small vector thus reducing the previous increase.

From Figure 5.5, it can be seen that V_1 and V_2 (only those which are present at the vertices of triangle 1) represent the pairs of small vectors whose dwell times are given by

T_1 and T_2, as shown in Table 5.2. Therefore, dwell time T_1 can now be sub-divided equally into T_{1P} and T_{1N}, and the dwell time T_2 can also be sub-divided equally into T_{2P} and T_{2N}. The subscripts 'P' and 'N' denote that the corresponding dwell times relate to the respective positive and negative small vectors.

As an example,

$$T_1 = T_{1P} + T_{1N} \tag{5.4}$$

where, $T_{1P} = k\, T_1\, T_s$

$T_{1N} = (1-k)\, T_1\, T_s$

T_s = switching period

The factor '*k*' is the control variable seen in Chapter 4. The value of '*k*' gets modified accordingly by employing a PI controller which responds to the variations of the neutral-point voltage from the desired set point. Hence, the on-times of the positive and negative small vectors are modified for a given switching period and hence the voltages across the DC-link capacitors could be balanced [36].

The effectiveness of the balancing capability of the neutral-point balancing controller for various operating conditions has been validated via simulations, as was done in Chapter 4 using the CB-SVM technique. However, only the closed-loop tests for the PMSM closed-loop drive will be presented in what follows.

5.4 CLOSED-LOOP TEST FOR NEUTRAL-POINT VOLTAGE BALANCING WITH PMSM DRIVE

The voltage balancing capability in the present case has also been tested for a closed-loop PMSM drive using the Field-Oriented Control technique presented in Chapter 2. Figure 5.6 and Figure 5.7 highlight the waveforms for different conditions of speed and torque in transient operation and continuous operation of the drive respectively.

It can be observed that the voltages across the DC-link capacitors have balanced well for various operating conditions.

The Space Vector Pulse Width Modulation strategy for two and three-level inverters can be summarized in the form of a flow chart as shown in the following section.

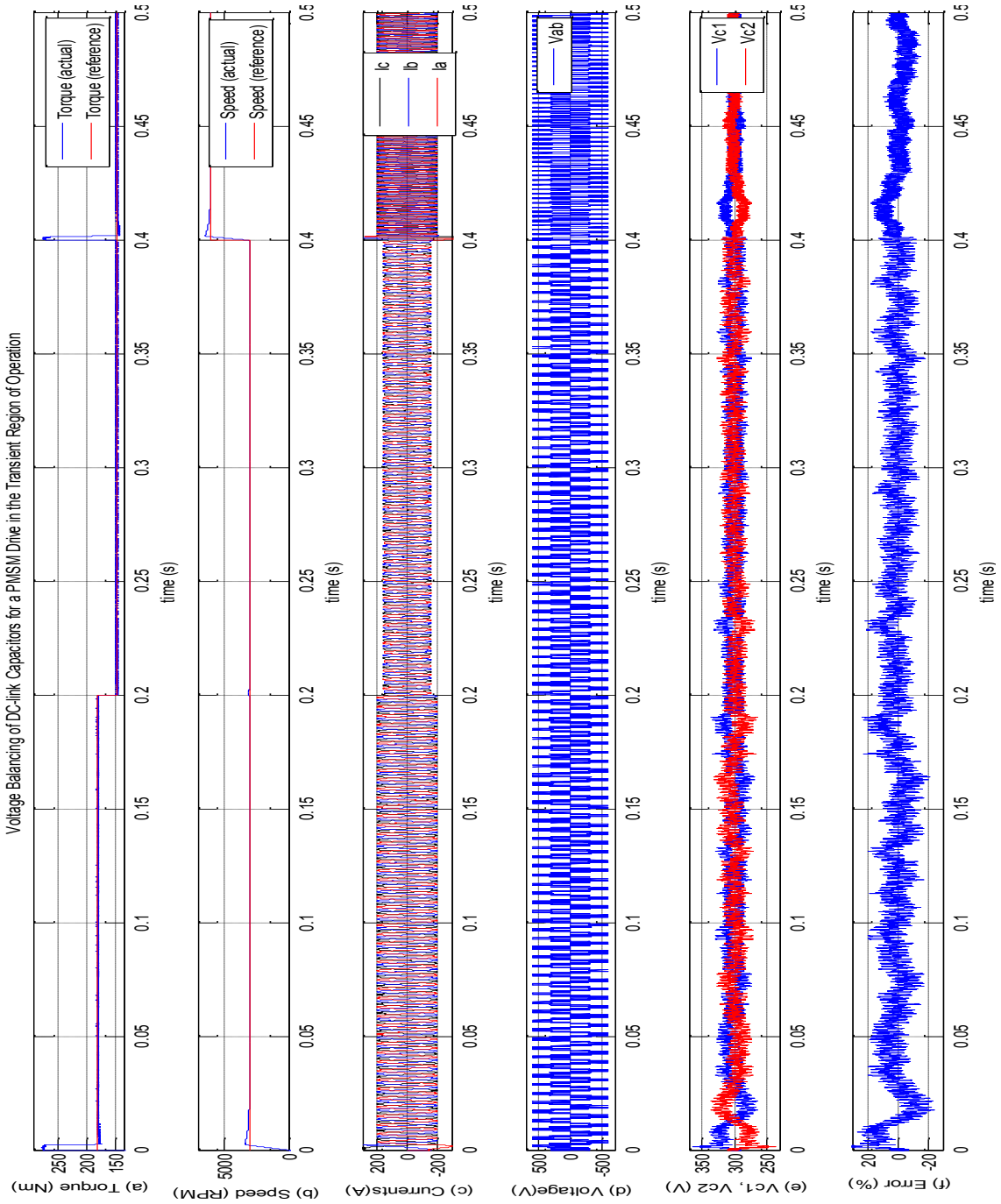


Figure 5.6: (a) Actual and Reference Torque, (b) Actual and Reference Speed, (c) Three Phase Inverter Output Current, (d) Line-to-line Output Voltage of the Inverter, (e) Voltages across the DC-link Capacitors, & (f) Percentage Error between the DC-link Capacitors

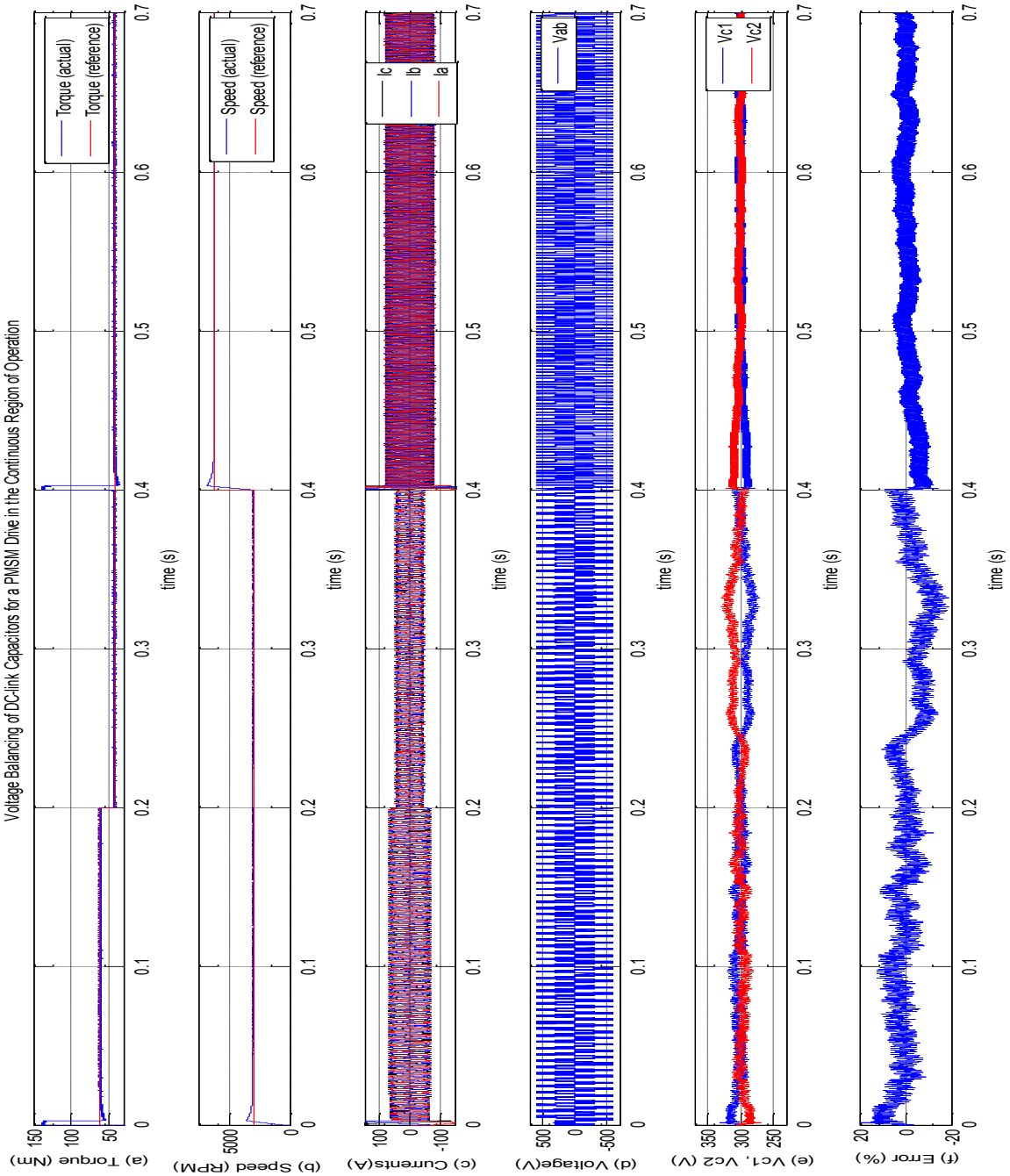


Figure 5.7: (a) Actual and Reference Torque, (b) Actual and Reference Speed, (c) Three Phase Inverter Output Current, (d) Line-to-line Output Voltage of the Inverter, (e) Voltages across the DC-link Capacitors, & (f) Percentage Error between the DC-link Capacitors

5.5 FLOW CHART FOR SPACE VECTOR PULSE WIDTH MODULATION OF TWO AND THREE-LEVEL INVERTERS

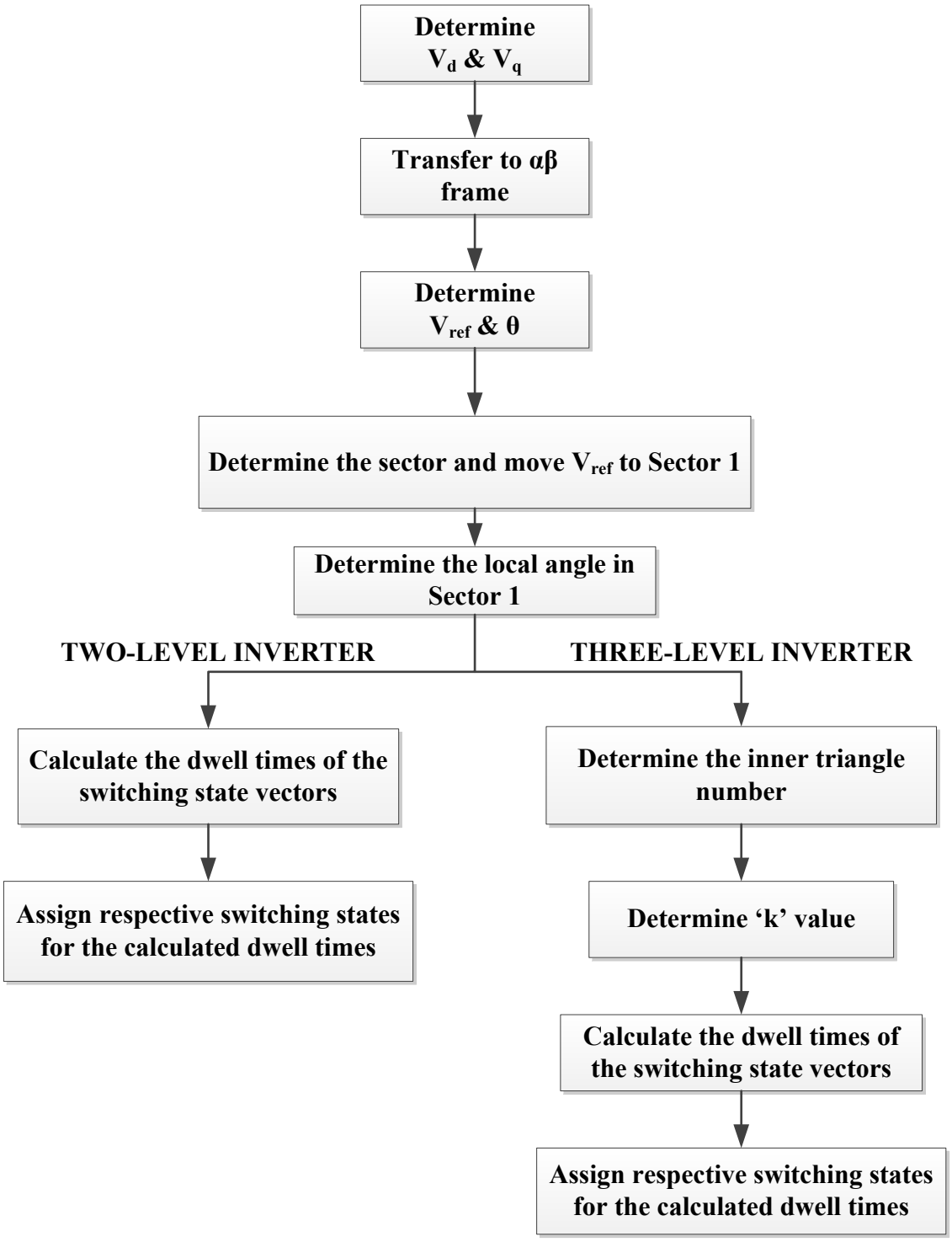


Figure 5.8: Flow Chart for SVPWM of Two and Three-level Inverters

5.6 THD COMPARISON FOR TWO AND THREE-LEVEL INVERTERS

In order to have further reduced total harmonic distortion of line-to-line voltage especially in the case of a three-level inverter, Space Vector Modulation method has been employed with neutral-point voltage balancing in the present chapter. The total harmonic distortion of the line-to-line voltage for the two and three-level inverters using the Space Vector Modulation technique have been presented.

The Fast Fourier Transform of the Line-to-line output voltage of the inverters for DC-link voltage (V_{dc}) = 600 V, modulation index (m) = 0.43, fundamental output voltage frequency (f) = 250 Hz, switching frequency (f_{sw}) = 6 kHz, and for the same machine have been presented in Figure 5.9 for the two-level inverter and in Figure 5.10 for the three-level inverter.

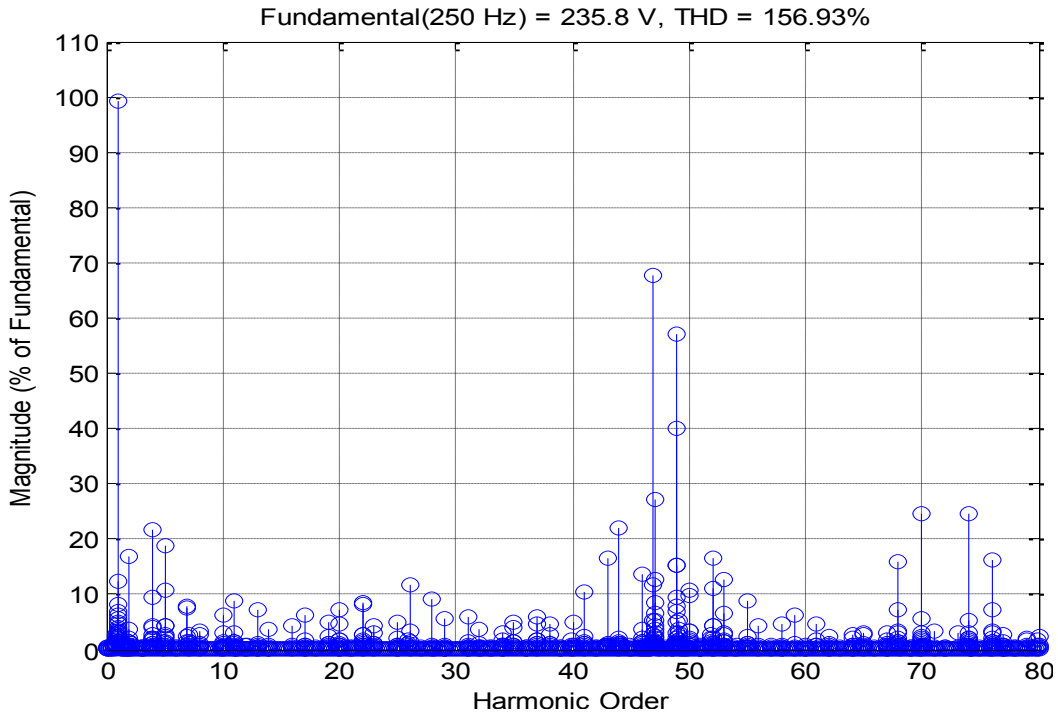


Figure 5.9: Line Voltage THD for Two-level Inverter with SVM

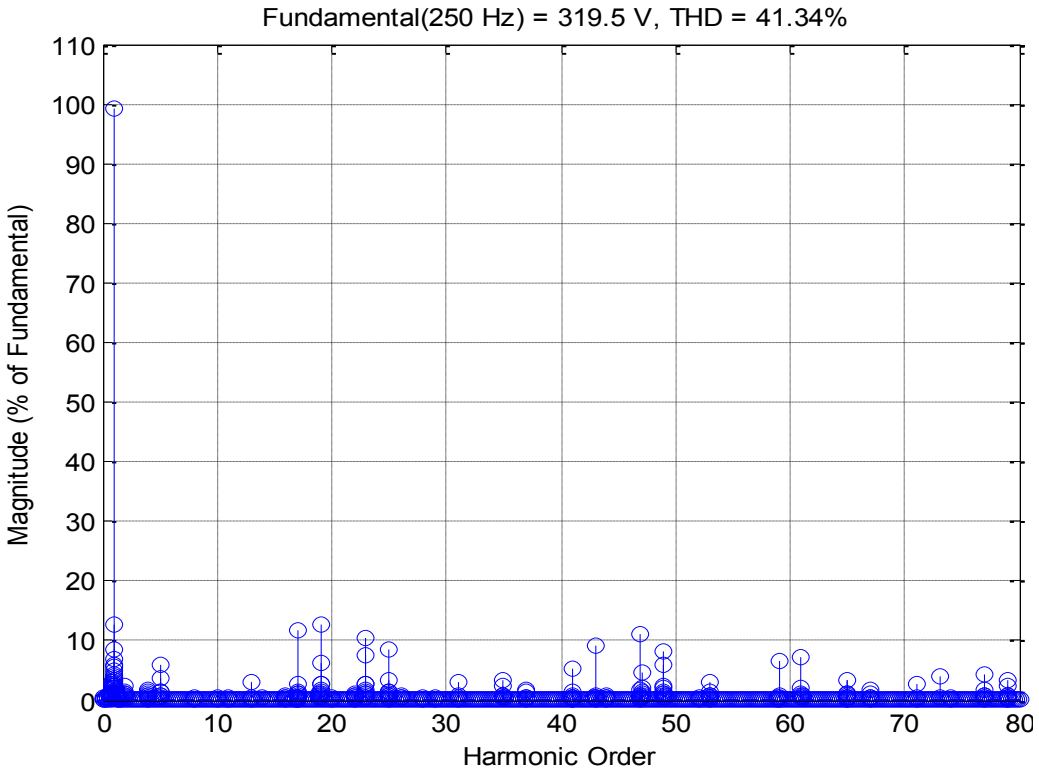


Figure 5.10: Line Voltage THD for Three-level Inverter with SVM

It can be seen from Figure 5.10 that in case of SVM, the THD is much lower for the same values of DC-link voltage, modulation index, fundamental frequency and switching frequency.

Though the control of DC-link voltage is more significant with lower error between the DC-link capacitor voltages, the total harmonic distortion of the line-to-line voltage is much lower by 37.7%. Also, the harmonics present in case of SVM three-level inverter have very less magnitude.

Therefore, Space Vector Modulation strategy with balanced DC-link approach for three-level NPC inverter proves to be a better approach.

In the previous chapter, it was seen that there was a reduction in the switching frequency value for the same value of current THD. Since the modulation scheme presented in this chapter aims at reduction in the THD, one can compare the current THD obtained in the previous chapter for a three-level inverter (switched using CB-SVM) with that of the current THD obtained in the present chapter for a three-level inverter (switched using SVM) at the "same" switching frequency. It can be seen that, when SVM strategy is employed for switching the inverter switches, the current THD obtained for the same conditions of operation and at the same switching frequency of 8.5 kHz is 0.97%.

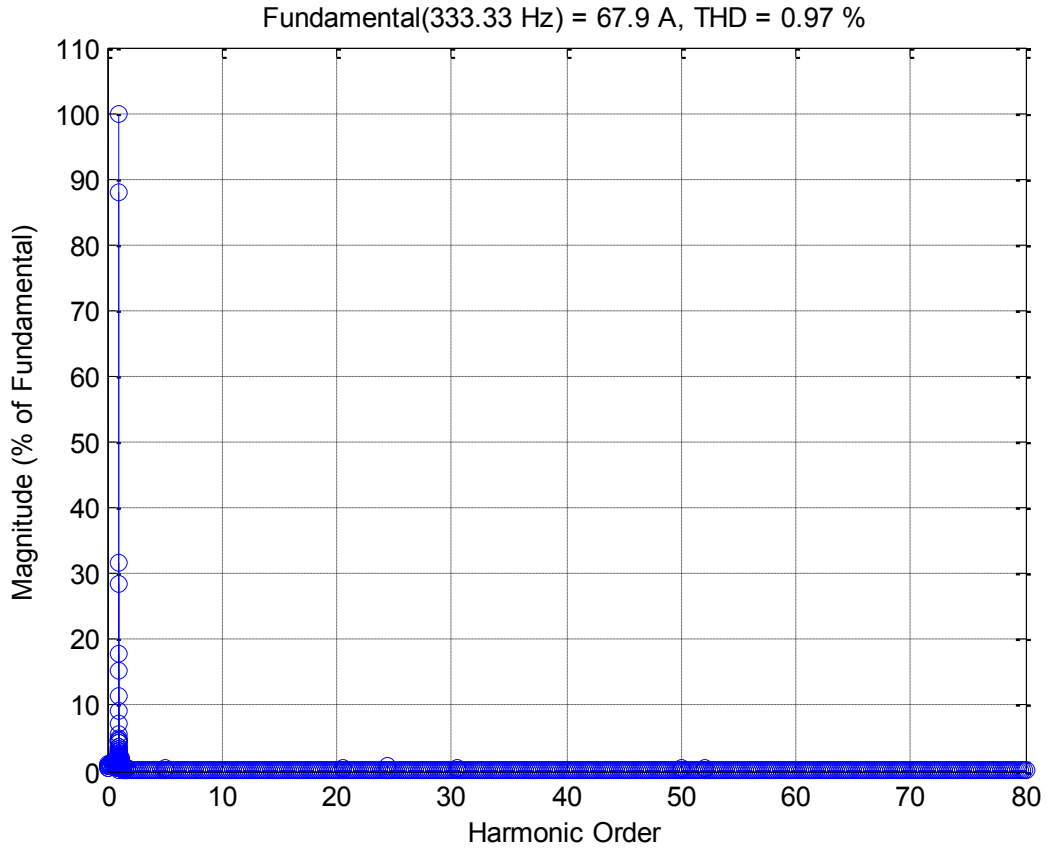


Figure 5.11: Output Current THD for Three-level Inverter at the Switching Frequency of 8.5 kHz using SVM

Therefore, one can observe a reduction in the total harmonic distortion of about 57% when SVM is used as the modulation scheme.

However, these are the procedures and guidelines that one can follow to make a performance comparison based on different criteria.

CONCLUSION

With efficiency becoming increasingly important in Power Electronics, it is the goal of every industry to take up initiatives for reduced energy consumption and improve the performance. Chapter 2 proposes the design of PI controllers for the control of speed and torque for a closed-loop PMSM drive with Field-Oriented Control approach. From the comparison of the two and three-level NPC inverters in Chapter 3, with respect to losses, efficiency, junction temperature and switching frequency for an entire range of speed and torque of an electric vehicle PMSM drive; three-level NPC inverter stands out as a better candidate.

The comparisons have been made by taking into account non-ideality of the switches for both the inverters. The practical limitations in terms of the junction temperature and the heat-sink capabilities have been taken into account and the procedure to determine the limits of the switching frequency has also been presented. The present thesis thus presents a performance comparison of the two and three-level NPC inverters and the approach presented has been strengthened with detailed calculations, graphical results and discussions.

The prevalent issue of DC-link voltage balancing for a three-level NPC inverter has been addressed in later part of Chapter 3. The equivalent circuit of the DC-link for the three-level NPC inverter has been derived from fundamentals and a method for DC-link capacitor voltage control using a simple PI controller has been proposed and presented. The effectiveness of the proposed controller for the balancing of the voltages across the capacitors for various conditions has been tested.

In order to avoid any additional circuit for the balancing purposes, the modification of the carrier-based modulation strategy has been proposed in Chapter 4. The DC-link balancing controller has been incorporated to test the control for various conditions. The THD of line-to-line voltage has been compared for two and three-level inverters and room for improvement of THD is sought, especially for the three-level NPC inverter. The switching frequency can be reduced by 68% when using a three-level inverter instead of a two-level inverter, for the same conditions of operation. The popular space vector modulation strategy incorporated with the balancing controller for the DC-link capacitor has been proposed in Chapter 5. The line-to-line THD of the three-level NPC inverter with SVM is proved to be 37% better than that with the Carrier-based approach of SVM. The current THD with this modulation method was found to be 57% lesser than the CB-SVM scheme. The effectiveness of the voltage balancing control for the three-level NPC inverter when employed in a PMSM drive has been presented and detailed results for various operating conditions have been presented; thus validating the effectiveness of control.

The present thesis, therefore, offers a detailed approach with designs, calculations and validations using MATLAB / SIMULINK and Microsoft Excel VBA platforms.

It can therefore be concluded that the three-level NPC inverter is a better candidate with varied advantages for the chosen application in the automotive industry employing PMSM drives.

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APPENDIX

'abc' to 'dq' TRANSFORMATION

For the purposes of simple analyses, the three-phase PMSM is considered in two-phase rotating frame which is rotating along with the rotor of the machine.

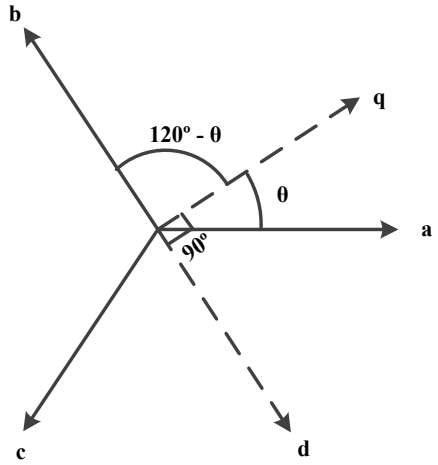


Figure.1: abc – dq Transformation

'abc → dq' transformation for any quantity 'x' can be carried out as follows:

$$x_q = \frac{2}{3}\left(x_a \cos\theta + x_b \cos\left(\theta - \frac{2\pi}{3}\right) + x_c \cos\left(\theta + \frac{2\pi}{3}\right)\right) \quad (1)$$

$$x_d = \frac{2}{3}\left(x_a \sin\theta + x_b \sin\left(\theta - \frac{2\pi}{3}\right) + x_c \sin\left(\theta + \frac{2\pi}{3}\right)\right) \quad (2)$$

Alternatively, dq → abc transformation can be carried out as follows:

$$x_a = x_d \sin\theta + x_q \cos\theta \quad (3)$$

$$x_b = x_d \sin\left(\theta - \frac{2\pi}{3}\right) + x_q \cos\left(\theta - \frac{2\pi}{3}\right) \quad (4)$$

$$x_c = x_d \sin\left(\theta + \frac{2\pi}{3}\right) + x_q \cos\left(\theta + \frac{2\pi}{3}\right) \quad (5)$$

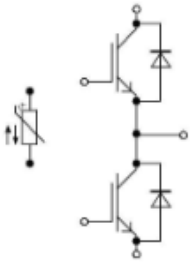
DATASHEET OF TWO-LEVEL INVERTER: FF300R12ME4

Technische Information / technical information

IGBT-Module
IGBT-modules

FF300R12ME4

EconoDUAL™3 Modul mit Trench/Feldstopp IGBT4 und Emitter Controlled HE Diode und NTC
EconoDUAL™3 module with Trench/Fieldstop IGBT4 and Emitter Controlled HE diode and NTC



V_{CES} = 1200V
$I_{C\ nom}$ = 300A / I_{CRM} = 600A

Typische Anwendungen
- Motorantriebe
- Servoumrichter
- USV-Systeme
- Windgeneratoren

Typical Applications
- Motor Drives
- Servo Drives
- UPS Systems
- Wind Turbines

Elektrische Eigenschaften
- Niedriges V_{CEsat}
- $T_{vj\ op}$ = 150°C

Electrical Features
- Low V_{CEsat}
- $T_{vj\ op}$ = 150°C

Mechanische Eigenschaften
- Standardgehäuse

Mechanical Features
- Standard Housing

Module Label Code

Barcode Code 128

DMX - Code

Content of the Code	Digit
Module Serial Number	1 - 5
Module Material Number	6 - 11
Production Order Number	12 - 19
Datecode (Production Year)	20 - 21
Datecode (Production Week)	22 - 23

prepared by: CU	date of publication: 2011-03-01	material no: 30804
approved by: MK	revision: 3.1	UL approved (E83335)

IGBT-Wechselrichter / IGBT-inverter

Höchstzulässige Werte / maximum rated values

Kollektor-Emitter-Sperrspannung collector-emitter voltage	T_{vj} = 25°C	V_{CES}	1200	V
Kollektor-Dauergleichstrom DC-collector current	T_C = 100°C, T_{vj} = 175°C T_C = 25°C, T_{vj} = 175°C	$I_{C\,nom}$ I_C	300 450	A A
Periodischer Kollektor Spitzenstrom repetitive peak collector current	t_P = 1 ms	I_{CRM}	600	A
Gesamt-Verlustleistung total power dissipation	T_C = 25°C, T_{vj} = 175°C	P_{tot}	1600	W
Gate-Emitter-Spitzenspannung gate-emitter peak voltage		V_{GES}	+/-20	V

Charakteristische Werte / characteristic values

			min.	typ.	max.	
Kollektor-Emitter Sättigungsspannung collector-emitter saturation voltage	I_C = 300 A, V_{GE} = 15 V I_C = 300 A, V_{GE} = 15 V I_C = 300 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$V_{CE\,sat}$	1,75 2,00 2,05	2,10	V V V
Gate-Schwellenspannung gate threshold voltage	I_C = 11,5 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	5,2	5,8	6,4	V
Gateladung gate charge	V_{GE} = -15 V ... +15 V		Q_G		2,25		µC
Interner Gatewiderstand internal gate resistor	T_{vj} = 25°C		R_{Gint}		2,5		Ω
Eingangskapazität input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		18,5		nF
Rückwirkungskapazität reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		1,05		nF
Kollektor-Emitter Reststrom collector-emitter cut-off current	V_{CE} = 1200 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			3,0	mA
Gate-Emitter Reststrom gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit (ind. Last) turn-on delay time (inductive load)	I_C = 300 A, V_{CE} = 600 V V_{GE} = ±15 V R_{Gon} = 1,3 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,on}$		0,17 0,18 0,19		µs µs µs
Anstiegszeit (induktive Last) rise time (inductive load)	I_C = 300 A, V_{CE} = 600 V V_{GE} = ±15 V R_{Gon} = 1,3 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r		0,05 0,05 0,05		µs µs µs
Abschaltverzögerungszeit (ind. Last) turn-off delay time (inductive load)	I_C = 300 A, V_{CE} = 600 V V_{GE} = ±15 V R_{Goff} = 1,3 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,off}$		0,45 0,56 0,60		µs µs µs
Fallzeit (induktive Last) fall time (inductive load)	I_C = 300 A, V_{CE} = 600 V V_{GE} = ±15 V R_{Goff} = 1,3 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_f		0,07 0,11 0,12		µs µs µs
Einschaltverlustenergie pro Puls turn-on energy loss per pulse	I_C = 300 A, V_{CE} = 600 V, L_S = 80 nH V_{GE} = ±15 V, di/dt = 6050 A/µs (T_{vj}=150°C) R_{Gon} = 1,3 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}		9,90 17,0 19,5		mJ mJ mJ
Abschaltverlustenergie pro Puls turn-off energy loss per pulse	I_C = 300 A, V_{CE} = 600 V, L_S = 80 nH V_{GE} = ±15 V, du/dt = 3100 V/µs (T_{vj}=150°C) R_{Goff} = 1,3 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}		25,0 37,5 42,0		mJ mJ mJ
Kurzschlussverhalten SC data	V_{GE} ≤ 15 V, V_{CC} = 800 V V_{CEmax} = V_{CES} -L_{sCE} ·di/dt	t_P ≤ 10 µs, T_{vj} = 150°C	I_{SC}		1200		A
Innerer Wärmewiderstand thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}			0,094	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,03		K/W

prepared by: CU	date of publication: 2011-03-01
approved by: MK	revision: 3.1

Diode-Wechselrichter / diode-inverter

Höchstzulässige Werte / maximum rated values

Periodische Spitzensperrspannung repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	1200		V
Dauergleichstrom DC forward current		I_F	300		A
Periodischer Spitzenstrom repetitive peak forward current	t_P = 1 ms	I_{FRM}	600		A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C V_R = 0 V, t_P = 10 ms, T_{vj} = 150°C	I²t	19000 15500		A²s A²s

Charakteristische Werte / characteristic values

				min.	typ.	max.	
Durchlassspannung forward voltage	I_F = 300 A, V_{GE} = 0 V I_F = 300 A, V_{GE} = 0 V I_F = 300 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	V_F		1,65 1,65 1,65	2,10	V V V
Rückstromspitze peak reverse recovery current	I_F = 300 A, - di_F/dt = 6050 A/µs (T_{vj}=150°C) V_R = 600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	I_{RM}		335 390 410		A A A
Sperrverzögerungsladung recovered charge	I_F = 300 A, - di_F/dt = 6050 A/µs (T_{vj}=150°C) V_R = 600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	Q_r		30,5 58,0 67,0		µC µC µC
Abschaltenergie pro Puls reverse recovery energy	I_F = 300 A, - di_F/dt = 6050 A/µs (T_{vj}=150°C) V_R = 600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}		19,0 29,5 34,5		mJ mJ mJ
Innerer Wärmewiderstand thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			0,15	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,046		K/W

NTC-Widerstand / NTC-thermistor

Charakteristische Werte / characteristic values

			min.	typ.	max.	
Nennwiderstand rated resistance	T_C = 25°C	R_{25}		5,00		kΩ
Abweichung von R_{100} deviation of R_{100}	T_C = 100°C, R_{100} = 493 Ω	$\Delta R/R$	-5		5	%
Verlustleistung power dissipation	T_C = 25°C	P_{25}			20,0	mW
B-Wert B-value	$R_2 = R_{25} \exp[B_{25/50}(1/T_2 - 1/(298,15\ K))]$	$B_{25/50}$		3375		K
B-Wert B-value	$R_2 = R_{25} \exp[B_{25/80}(1/T_2 - 1/(298,15\ K))]$	$B_{25/80}$		3411		K
B-Wert B-value	$R_2 = R_{25} \exp[B_{25/100}(1/T_2 - 1/(298,15\ K))]$	$B_{25/100}$		3433		K

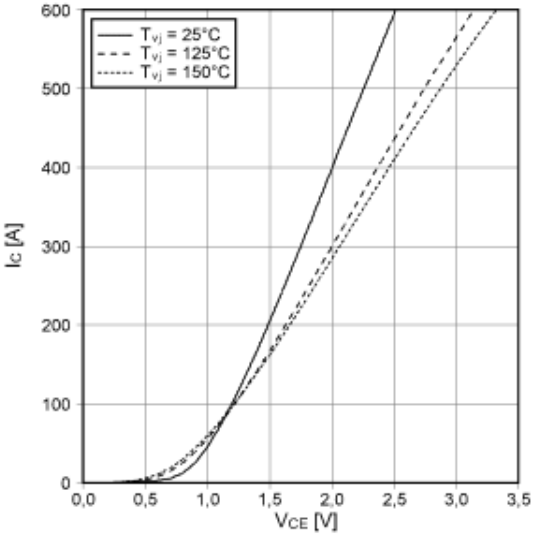
Angaben gemäß gültiger Application Note.
Specification according to the valid application note.

prepared by: CU	date of publication: 2011-03-01
approved by: MK	revision: 3.1

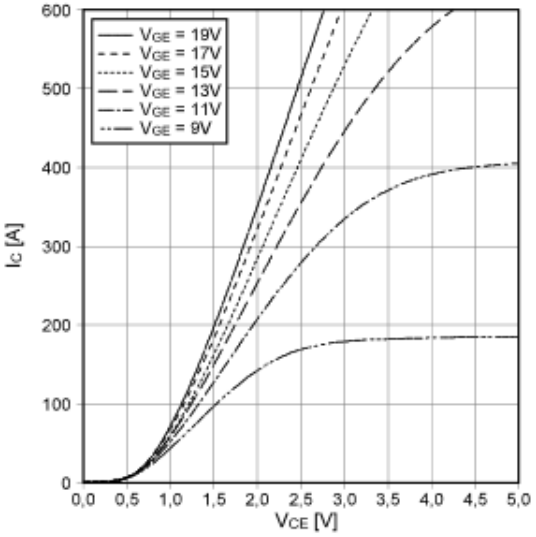
Modul / module

Isolations-Prüfspannung insulation test voltage	RMS, f = 50 Hz, t = 1 min	V_{ISOL}		2,5		kV
Material Modulgrundplatte material of module baseplate				Cu		
Material für innere Isolation material for internal insulation				Al_2O_3		
Kriechstrecke creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			14,5 13,0		mm
Luftstrecke clearance distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			12,5 10,0		mm
Vergleichszahl der Kriechwegbildung comparative tracking index		CTI		> 200		
			min.	typ.	max.	
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Modul / per module λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,009		K/W
Modulinduktivität stray inductance module		L_{sCE}		20		nH
Modulleitungswiderstand, Anschlüsse - Chip module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		1,20		mΩ
Höchstzulässige Sperrschichttemperatur maximum junction temperature	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	$T_{vj\ max}$			175	°C
Temperatur im Schaltbetrieb temperature under switching conditions	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	$T_{vj\ op}$	-40		150	°C
Lagertemperatur storage temperature		T_{stg}	-40		125	°C
Anzugsdrehmoment f. mech. Befestigung mounting torque	Schraube M5 - Montage gem. gültiger Applikation Note screw M5 - mounting according to valid application note	M	3,00	-	6,00	Nm
Anzugsdrehmoment f. elektr. Anschlüsse terminal connection torque	Schraube M6 - Montage gem. gültiger Applikation Note screw M6 - mounting according to valid application note	M	3,0	-	6,0	Nm
Gewicht weight		G		345		g

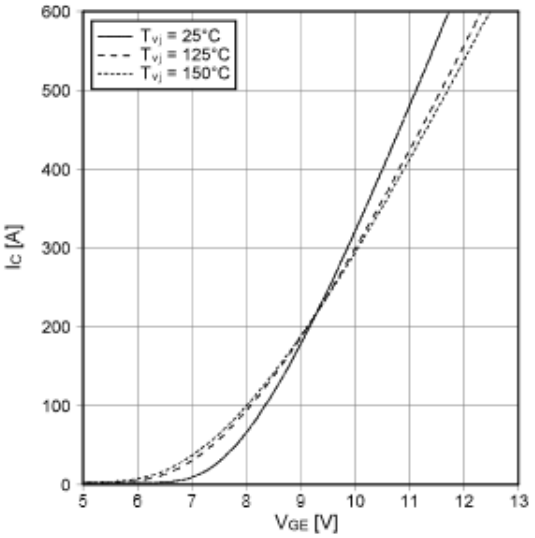
Ausgangskennlinie IGBT-Wechselr. (typisch)
output characteristic IGBT-inverter (typical)
$I_C = f(V_{CE})$
$V_{GE} = 15$ V



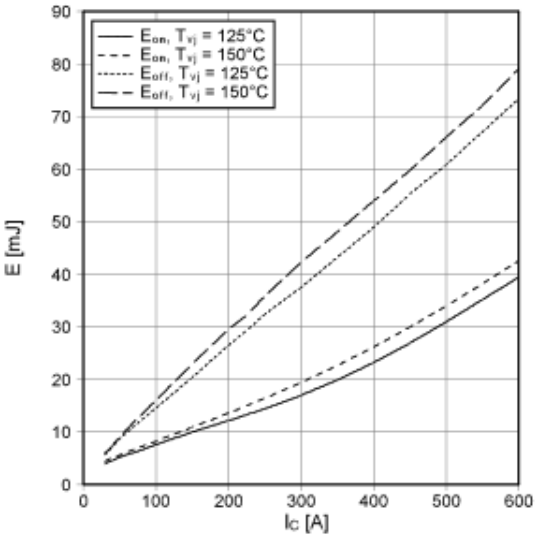
Ausgangskennlinienfeld IGBT-Wechselr. (typisch)
output characteristic IGBT-inverter (typical)
$I_C = f(V_{CE})$
$T_{vj} = 150°C$



Übertragungscharakteristik IGBT-Wechselr. (typisch)
transfer characteristic IGBT-inverter (typical)
$I_C = f(V_{GE})$
$V_{CE} = 20$ V



Schaltverluste IGBT-Wechselr. (typisch)
switching losses IGBT-inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
$V_{GE} = \pm 15$ V, $R_{Gon} = 1.3\ \Omega$, $R_{Goff} = 1.3\ \Omega$, $V_{CE} = 600$ V



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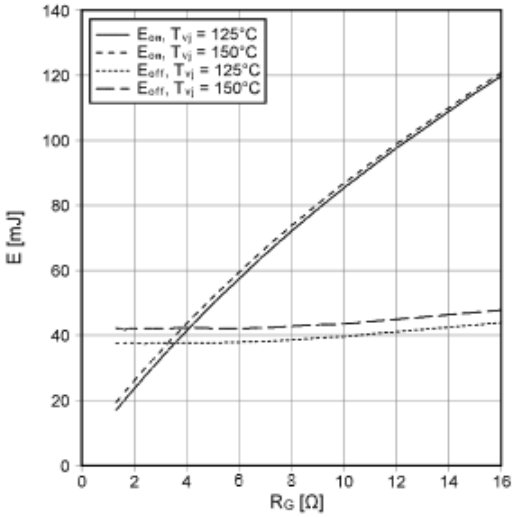
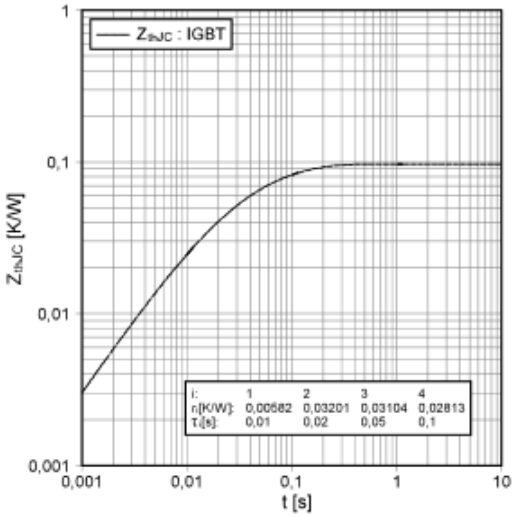
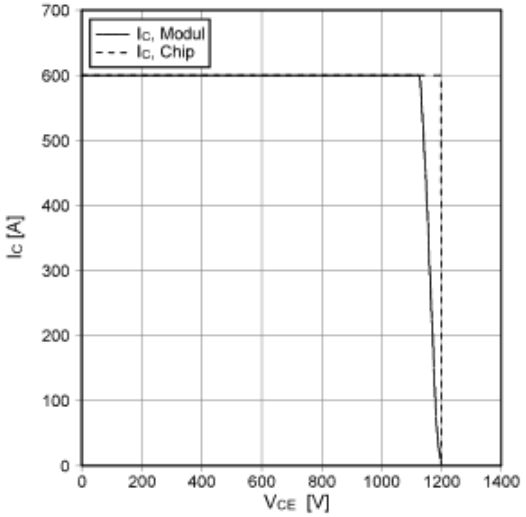
Schaltverluste IGBT-Wechselr. (typisch)
switching losses IGBT-Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
V_{GE} = ±15 V, I_C = 300 A, V_{CE} = 600 V



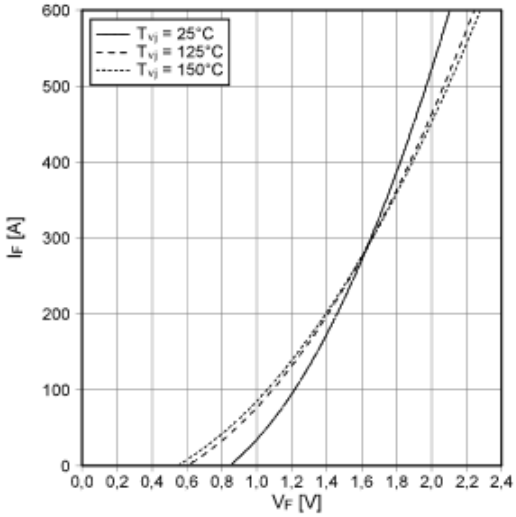
Transienter Wärmewiderstand IGBT-Wechselr.
transient thermal impedance IGBT-inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT-Wr. (RBSOA)
reverse bias safe operating area IGBT-inv. (RBSOA)
$I_C = f(V_{CE})$
V_{GE} = ±15 V, R_{Goff} = 1.3 Ω, T_{vj} = 150°C



Durchlasskennlinie der Diode-Wechselr. (typisch)
forward characteristic of diode-inverter (typical)
$I_F = f(V_F)$



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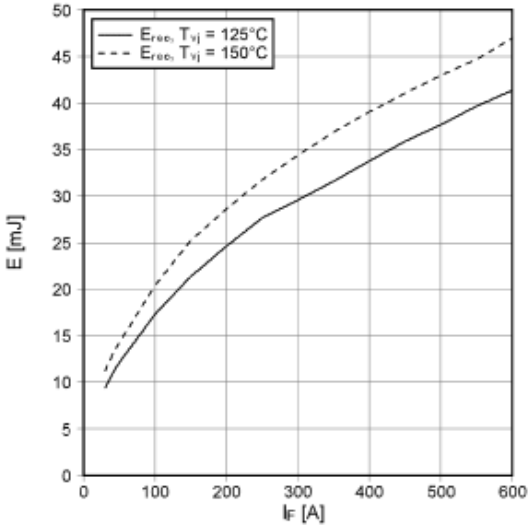
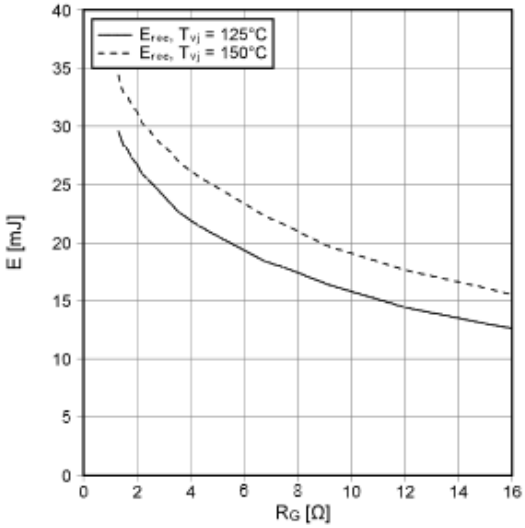
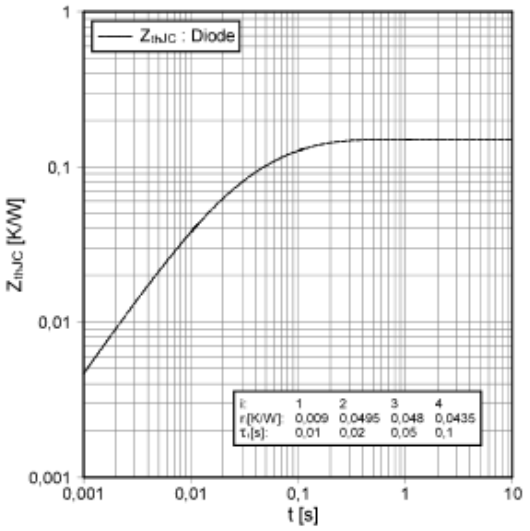
Schaltverluste Diode-Wechselr. (typisch)
switching losses diode-inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 1.3\ \Omega$, $V_{CE} = 600$ V



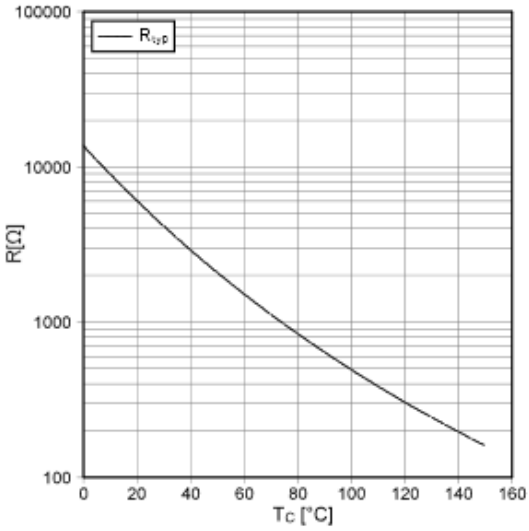
Schaltverluste Diode-Wechselr. (typisch)
switching losses diode-inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 300$ A, $V_{CE} = 600$ V



Transienter Wärmewiderstand Diode-Wechselr.
transient thermal impedance diode-inverter
$Z_{thJC} = f(t)$

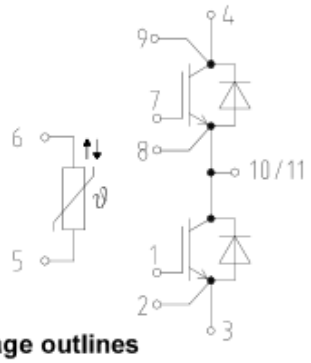


NTC-Temperaturkennlinie (typisch)
NTC-temperature characteristic (typical)
$R = f(T)$

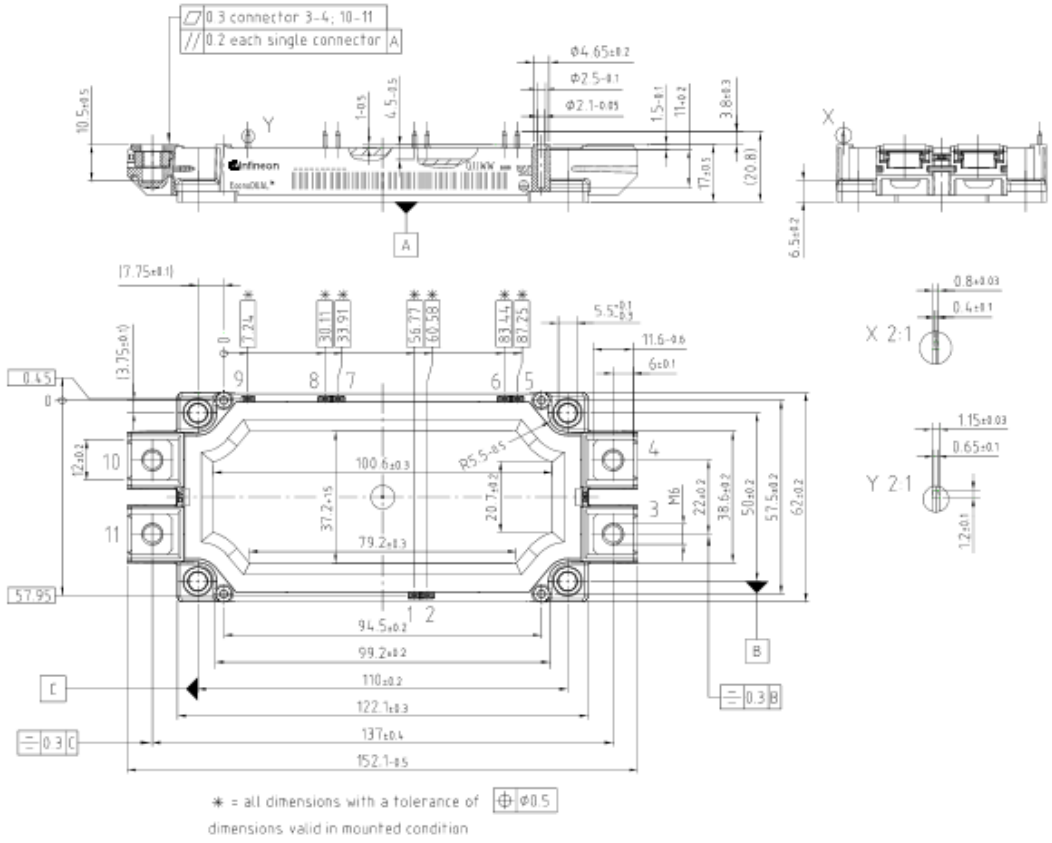


prepared by: CU	date of publication: 2011-03-01
approved by: MK	revision: 3.1

Schaltplan / circuit diagram



Gehäuseabmessungen / package outlines



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approved by: MK	revision: 3.1

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- to perform joint Risk and Quality Assessments;
- the conclusion of Quality Agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery depended on the realization of any such measures.

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approved by: MK	revision: 3.1

DATASHEET OF THREE-LEVEL INVERTER: F3L300R07PE4

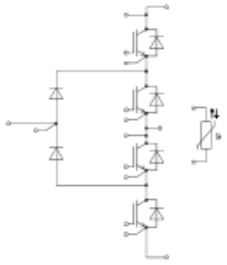
Technische Information / technical information

IGBT-Module
IGBT-modules

F3L300R07PE4

EconoPACK™4 Modul mit Trench/Feldstopp IGBT4 und Emitter Controlled 4 Diode und NTC
EconoPACK™4 module with Trench/Fieldstop IGBT4 and Emitter Controlled 4 diode and NTC

Vorläufige Daten / preliminary data



V_{CES} = 650V
$I_{C\ nom}$ = 300A / I_{CRM} = 600A

Typische Anwendungen
- 3-Level-Applikationen

Typical Applications
- 3-Level-Applications

Elektrische Eigenschaften
- Erhöhte Sperrspannungsfestigkeit auf 650V
- Erweiterte Sperrschichttemperatur $T_{vj\ op}$
- Trench IGBT 4
- $T_{vj\ op}$ = 150°C
- V_{CEsat} mit positivem Temperaturkoeffizienten

Electrical Features
- Increased blocking voltage capability to 650V
- Extended Operation Temperature $T_{vj\ op}$
- Trench IGBT 4
- $T_{vj\ op}$ = 150°C
- V_{CEsat} with positive Temperature Coefficient

Mechanische Eigenschaften
- 4 kV AC 1min Isolationsfestigkeit
- Hohe mechanische Robustheit
- Integrierter NTC Temperatur Sensor
- Isolierte Bodenplatte
- Standardgehäuse

Mechanical Features
- 4 kV AC 1min Insulation
- High mechanical robustness
- Integrated NTC temperature sensor
- Isolated Base Plate
- Standard Housing

Module Label Code

Barcode Code 128

DMX - Code

Content of the Code	Digit
Module Serial Number	1 - 5
Module Material Number	6 - 11
Production Order Number	12 - 19
Datecode (Production Year)	20 - 21
Datecode (Production Week)	22 - 23

prepared by: AS	date of publication: 2011-03-02	material no: 34036
approved by: MK	revision: 2.1	UL approved (E83335)

Vorläufige Daten
preliminary data

IGBT-Wechselrichter / IGBT-inverter

Höchstzulässige Werte / maximum rated values

Kollektor-Emitter-Sperrspannung collector-emitter voltage	T_{vj} = 25°C	V_{CES}		650	V
Kollektor-Dauergleichstrom DC-collector current	T_C = 70°C, T_{vj} = 175°C	$I_{C\ nom}$		300	A
Periodischer Kollektor Spitzenstrom repetitive peak collector current	t_P = 1 ms	I_{CRM}		600	A
Gesamt-Verlustleistung total power dissipation	T_C = 25°C, T_{vj} = 175°C	P_{tot}		940	W
Gate-Emitter-Spitzenspannung gate-emitter peak voltage		V_{GES}		+/-20	V

Charakteristische Werte / characteristic values

			min.	typ.	max.	
Kollektor-Emitter Sättigungsspannung collector-emitter saturation voltage	I_C = 300 A, V_{GE} = 15 V I_C = 300 A, V_{GE} = 15 V I_C = 300 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$V_{CE\ sat}$		1,55 1,70 1,75	1,95	V V V
Gate-Schwellenspannung gate threshold voltage	I_C = 4,80 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	5,0	5,8	6,5	V
Gateladung gate charge	V_{GE} = -15 V ... +15 V		Q_G		3,00		µC
Interner Gatewiderstand internal gate resistor	T_{vj} = 25°C		R_{Gint}		1,0		Ω
Eingangskapazität input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		18,5		nF
Rückwirkungskapazität reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		0,57		nF
Kollektor-Emitter Reststrom collector-emitter cut-off current	V_{CE} = 650 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			1,0	mA
Gate-Emitter Reststrom gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit (ind. Last) turn-on delay time (inductive load)	I_C = 300 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Gon} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\ on}$		0,11 0,12 0,13		µs µs µs
Anstiegszeit (induktive Last) rise time (inductive load)	I_C = 300 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Gon} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r		0,05 0,06 0,06		µs µs µs
Abschaltverzögerungszeit (ind. Last) turn-off delay time (inductive load)	I_C = 300 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Goff} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\ off}$		0,49 0,52 0,53		µs µs µs
Fallzeit (induktive Last) fall time (inductive load)	I_C = 300 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Goff} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_f		0,05 0,07 0,07		µs µs µs
Einschaltverlustenergie pro Puls turn-on energy loss per pulse	I_C = 300 A, V_{CE} = 300 V, L_S = 30 nH V_{GE} = ±15 V, di/dt = 3400 A/µs (T_{vj}=150°C) R_{Gon} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}		1,50 2,00 2,50		mJ mJ mJ
Abschaltverlustenergie pro Puls turn-off energy loss per pulse	I_C = 300 A, V_{CE} = 300 V, L_S = 30 nH V_{GE} = ±15 V, du/dt = 3300 V/µs (T_{vj}=150°C) R_{Goff} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}		14,0 17,5 18,5		mJ mJ mJ
Kurzschlussverhalten SC data	V_{GE} ≤ 15 V, V_{CC} = 360 V V_{CEmax} = V_{CES} -L_{sCE} ·di/dt	t_P ≤ 10 µs, T_{vj} = 25°C t_P ≤ 10 µs, T_{vj} = 150°C	I_{SC}		1500 1200		A A
Innerer Wärmewiderstand thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}			0,16	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,063		K/W

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approved by: MK	revision: 2.1

Vorläufige Daten
preliminary data

Diode-Wechselrichter / diode-inverter

Höchstzulässige Werte / maximum rated values

Periodische Spitzensperrspannung repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	650		V
Dauergleichstrom DC forward current		I_F	300		A
Periodischer Spitzenstrom repetitive peak forward current	t_P = 1 ms	I_{FRM}	600		A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C V_R = 0 V, t_P = 10 ms, T_{vj} = 150°C	I²t	6000 5600		A²s A²s

Charakteristische Werte / characteristic values

				min.	typ.	max.	
Durchlassspannung forward voltage	I_F = 300 A, V_{GE} = 0 V I_F = 300 A, V_{GE} = 0 V I_F = 300 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	V_F		1,55 1,50 1,45	1,95	V V V
Rückstromspitze peak reverse recovery current	I_F = 300 A, - di_F/dt = 3400 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	I_{RM}		145 195 210		A A A
Sperrverzögerungsladung recovered charge	I_F = 300 A, - di_F/dt = 3400 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	Q_r		11,0 21,0 24,0		µC µC µC
Abschaltenergie pro Puls reverse recovery energy	I_F = 300 A, - di_F/dt = 3400 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}		3,50 6,10 7,00		mJ mJ mJ
Innerer Wärmewiderstand thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			0,32	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,125		K/W

Diode-3-Level / Diode-3-level

Höchstzulässige Werte / maximum rated values

Periodische Spitzensperrspannung repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	650		V
Dauergleichstrom DC forward current		I_F	300		A
Periodischer Spitzenstrom repetitive peak forw. current	t_P = 1 ms	I_{FRM}	600		A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C V_R = 0 V, t_P = 10 ms, T_{vj} = 150°C	I²t	6000 5600		A²s A²s

Charakteristische Werte / characteristic values

				min.	typ.	max.	
Durchlassspannung forward voltage	I_F = 300 A, V_{GE} = 0 V I_F = 300 A, V_{GE} = 0 V I_F = 300 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	V_F		1,55 1,50 1,45	1,95	V V V
Rückstromspitze peak reverse recovery current	I_F = 300 A, - di_F/dt = 3400 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	I_{RM}		145 195 210		A A A
Sperrverzögerungsladung recovered charge	I_F = 300 A, - di_F/dt = 3400 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	Q_r		11,0 21,0 24,0		µC µC µC
Abschaltenergie pro Puls reverse recovery energy	I_F = 300 A, - di_F/dt = 3400 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}		3,50 6,10 7,00		mJ mJ mJ
Innerer Wärmewiderstand thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			0,32	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,125		K/W

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Vorläufige Daten
preliminary data

NTC-Widerstand / NTC-thermistor

Charakteristische Werte / characteristic values

			min.	typ.	max.	
Nennwiderstand rated resistance	T_C = 25°C	R_{25}		5,00		kΩ
Abweichung von R_{100} deviation of R_{100}	T_C = 100°C, R_{100} = 493 Ω	$\Delta R/R$	-5		5	%
Verlustleistung power dissipation	T_C = 25°C	P_{25}			20,0	mW
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/50}(1/T_2 - 1/(298,15\ K))]$	$B_{25/50}$		3375		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/80}(1/T_2 - 1/(298,15\ K))]$	$B_{25/80}$		3411		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/100}(1/T_2 - 1/(298,15\ K))]$	$B_{25/100}$		3433		K

Angaben gemäß gültiger Application Note.
Specification according to the valid application note.

Modul / module

Isolations-Prüfspannung insulation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		4,0		kV
Material Modulgrundplatte material of module baseplate				Cu		
Material für innere Isolation material for internal insulation				Al_2O_3		
Kriechstrecke creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			25,0 12,5		mm
Luftstrecke clearance distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			11,0 7,0		mm
Vergleichszahl der Kriechwegbildung comparative tracking index		CTI		> 200		
			min.	typ.	max.	
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Modul / per module λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,009		K/W
Modulinduktivität stray inductance module		L_{sCE}		45		nH
Höchstzulässige Sperrschichttemperatur maximum junction temperature	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	$T_{vj\ max}$			175	°C
Temperatur im Schaltbetrieb temperature under switching conditions	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	$T_{vj\ op}$	-40		150	°C
Lagertemperatur storage temperature		T_{stg}	-40		125	°C
Anzugsdrehmoment f. mech. Befestigung mounting torque	Schraube M5 - Montage gem. gültiger Applikation Note screw M5 - mounting according to valid application note	M	3,00	-	6,00	Nm
Anzugsdrehmoment f. elektr. Anschlüsse terminal connection torque	Schraube M6 - Montage gem. gültiger Applikation Note screw M6 - mounting according to valid application note	M	3,0	-	6,0	Nm
Gewicht weight		G		400		g

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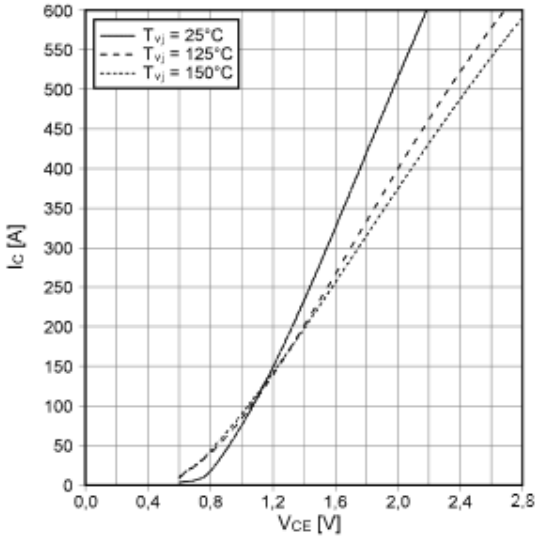
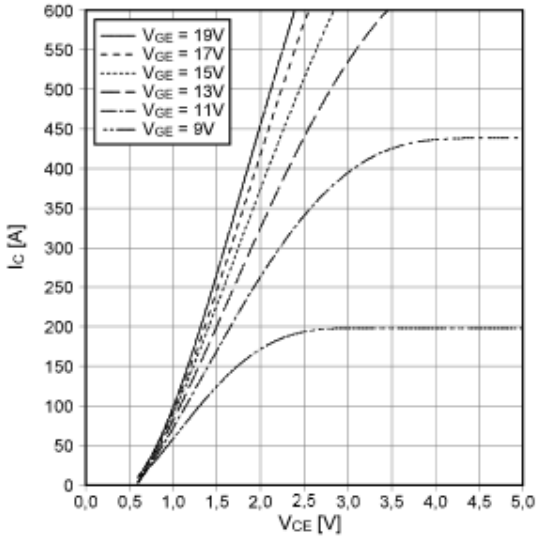
Vorläufige Daten
preliminary data

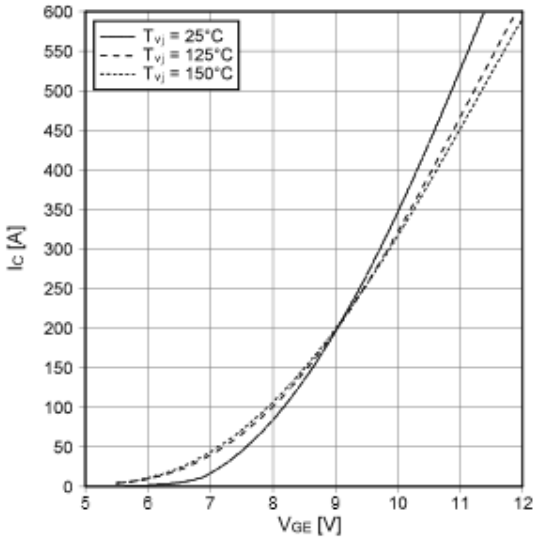
Ausgangskennlinie IGBT-Wechselr. (typisch)
output characteristic IGBT-inverter (typical)
$I_C = f(V_{CE})$
V_{GE} = 15 V



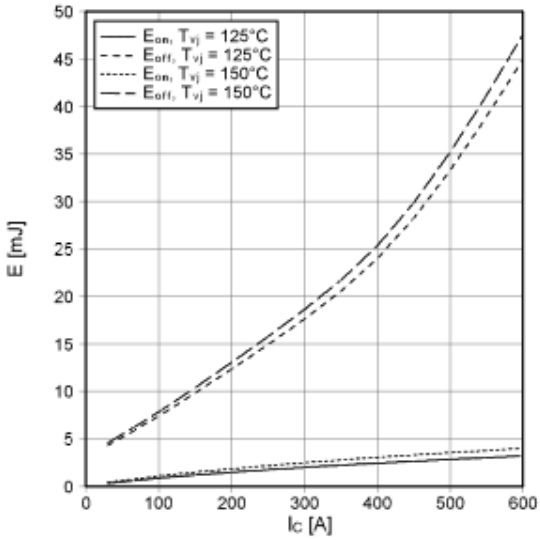
Ausgangskennlinienfeld IGBT-Wechselr. (typisch)
output characteristic IGBT-inverter (typical)
$I_C = f(V_{CE})$
T_{vj} = 150°C



Übertragungscharakteristik IGBT-Wechselr. (typisch)
transfer characteristic IGBT-inverter (typical)
$I_C = f(V_{GE})$
V_{CE} = 20 V



Schaltverluste IGBT-Wechselr. (typisch)
switching losses IGBT-inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
V_{GE} = ±15 V, R_{Gon} = 2 Ω, R_{Goff} = 2 Ω, V_{CE} = 300 V



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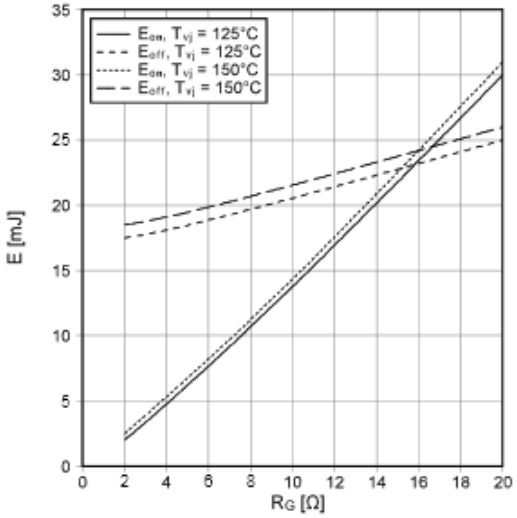
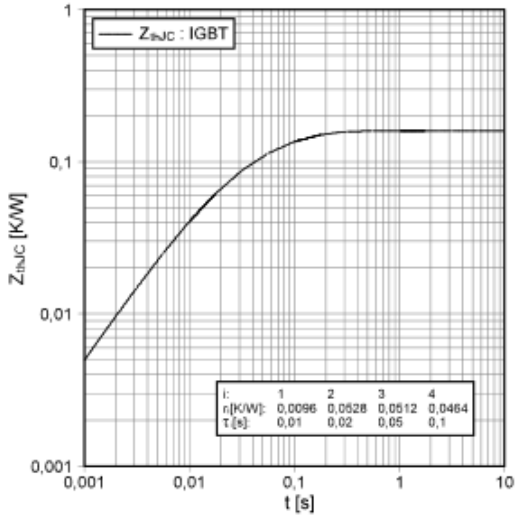
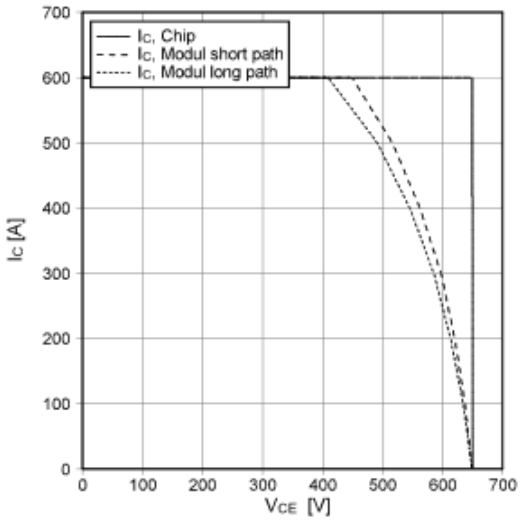
Schaltverluste IGBT-Wechselr. (typisch)
switching losses IGBT-Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
$V_{GE} = \pm 15$ V, $I_C = 300$ A, $V_{CE} = 300$ V



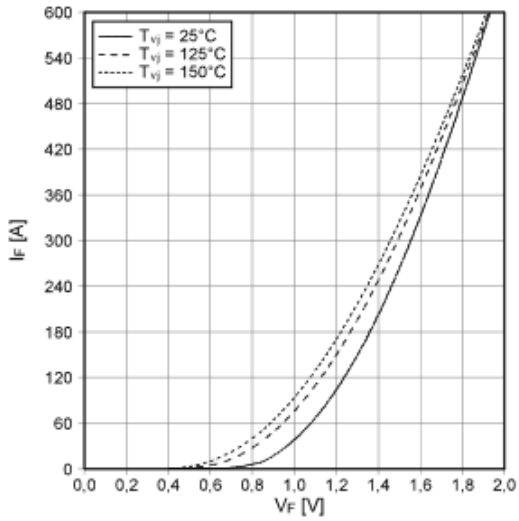
Transienter Wärmewiderstand IGBT-Wechselr.
transient thermal impedance IGBT-inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT-Wr. (RBSOA)
reverse bias safe operating area IGBT-inv. (RBSOA)
$I_C = f(V_{CE})$
$V_{GE} = \pm 15$ V, $R_{Goff} = 2\ \Omega$, $T_{vj} = 150°C$



Durchlasskennlinie der Diode-Wechselr. (typisch)
forward characteristic of diode-inverter (typical)
$I_F = f(V_F)$



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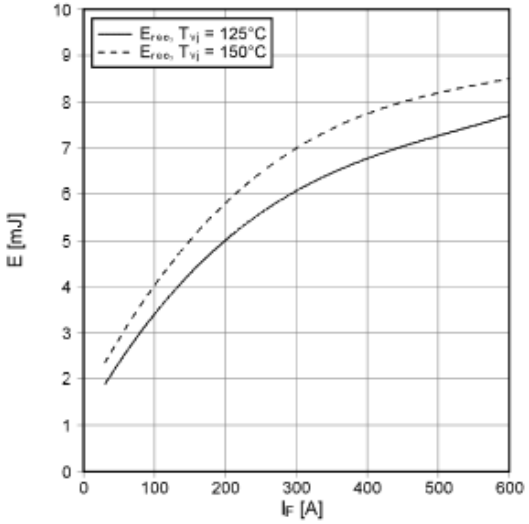
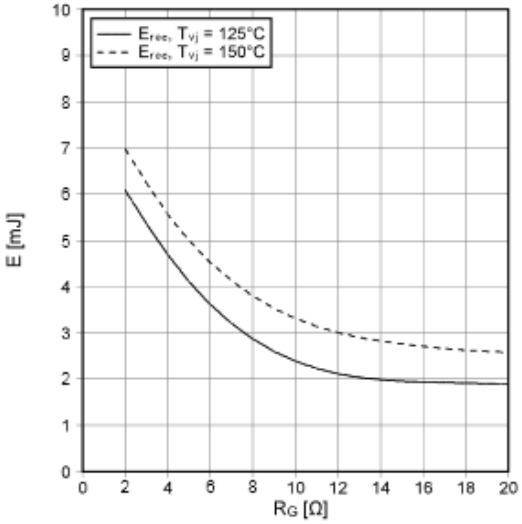
Vorläufige Daten
preliminary data

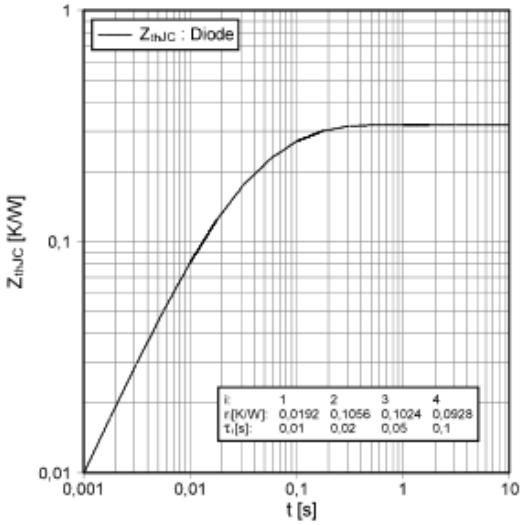
Schaltverluste Diode-Wechselr. (typisch)
switching losses diode-inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 2\ \Omega$, $V_{CE} = 300\ V$



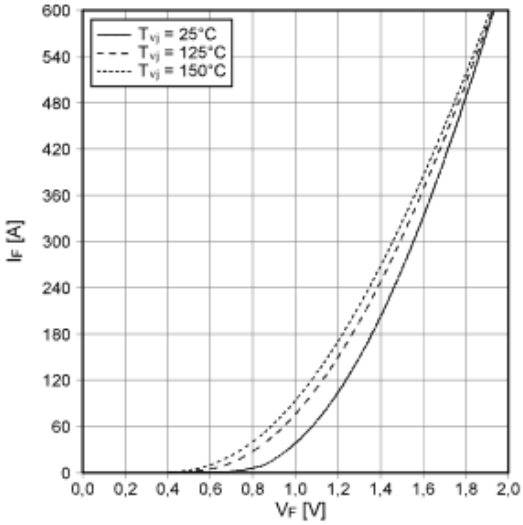
Schaltverluste Diode-Wechselr. (typisch)
switching losses diode-inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 300\ A$, $V_{CE} = 300\ V$



Transienter Wärmewiderstand Diode-Wechselr.
transient thermal impedance diode-inverter
$Z_{thJC} = f(t)$



Durchlasskennlinie der Diode-3-Level
forward characteristic of Diode-3-level
$I_F = f(V_F)$



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Vorläufige Daten
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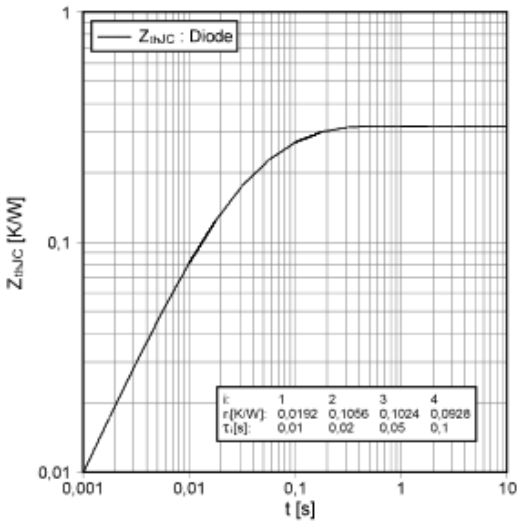
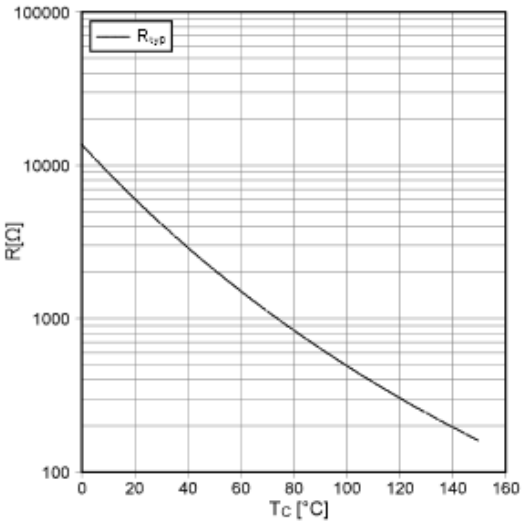
Transienter Wärmewiderstand Diode-3-Level
transient thermal impedance Diode-3-level
$Z_{thJC} = f(t)$



NTC-Temperaturkennlinie (typisch)
NTC-temperature characteristic (typical)
R = f (T)



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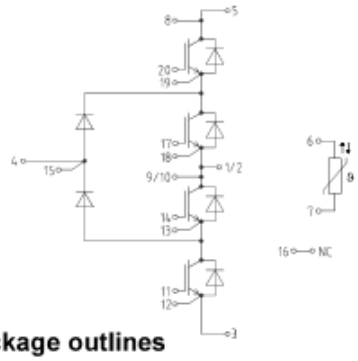
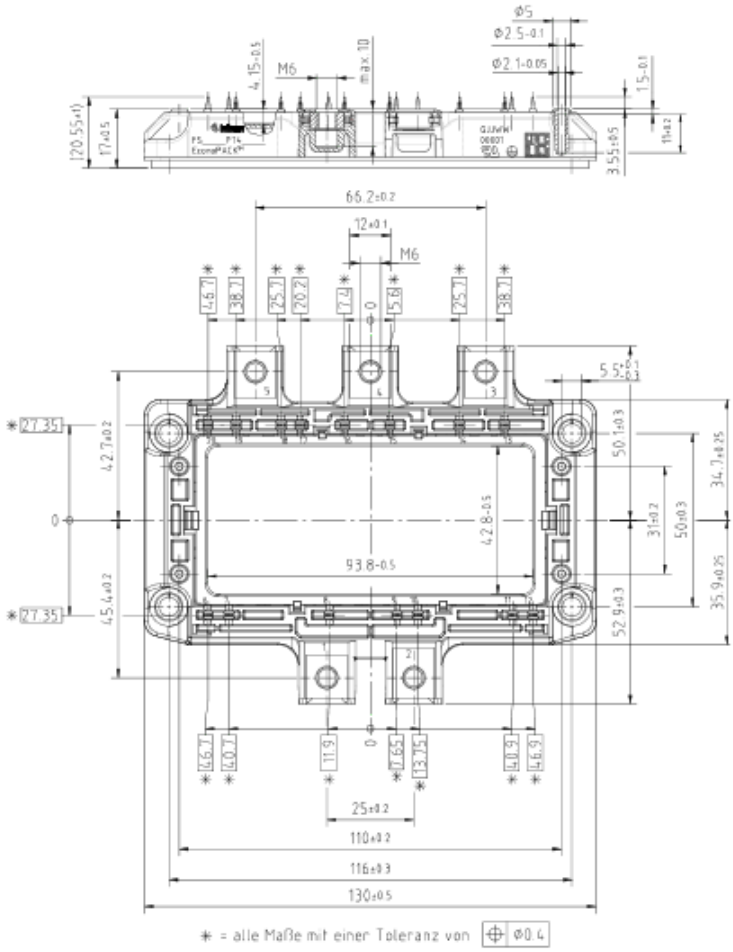
preliminary data

Schaltplan / circuit diagram



Gehäuseabmessungen / package outlines



* = alle Maße mit einer Toleranz von ⌖ Ø0.4

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