CMOS NEGATIVE RESISTANCE CIRCUITS

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Abstract

CMOS Negative Resistance Circuits

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Active resistors in VLSI technology have grown in stature as they enable the design of large resistive loads without using excessively bulky resistors, or a high voltage supply. Active resistors designed in CMOS technology have the property of being voltage controlled, which permits the design of negative resistance circuits. A negative resistance circuit has the property in which the current is a decreasing function of the input voltage, and has an I-V curve with a negative slope. They have the potential of being a key building block for larger electronic systems in VLSI technology, with applications in various fundamental circuits such as amplifiers and oscillators.

A detailed characterization of negative resistance circuits is presented in this thesis. Important large and small signal characteristics, including noise, linearity and power consumption are investigated. A strategy for designing wide bandwidth active resistors is proposed with supporting analysis. Key stability issues that have not previously been reported are brought forward and the stability of larger circuits that accommodate a negative resistor are investigated. To conclude the thesis, design applications in which negative resistors have been used to improve the performance of larger electronic systems are demonstrated. These include the design of a low phase noise current mode oscillator and a high bandwidth inverting feedback amplifier.

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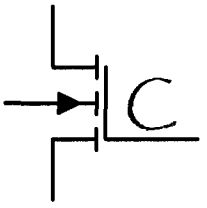
List of Symbols and Abbreviations

AC	Alternating Current
BJT	Bipolar Junction Transistor
C	Capacitor
CC	Current Conveyor
C_{gb}	Gate-Bulk Capacitance of MOS Transistor
C_{gd}	Gate-Drain Capacitance of MOS Transistor
C_{gs}	Gate-Source Capacitance of MOS Transistor
CMOS	Complimentary Metal-Oxide Semiconductor
C_{ox}	Channel Capacitance per Unit Area
dB	Decibels
DC	Direct Current
F	Farads – unit of measurement for capacitance
g_{ds}	Drain-Source Admittance of Transistor
g_m	Transconductance
H	Henry – unit of measurement for inductance
Hz	Hertz – unit of measurement for frequency
IC	Integrated Circuit
K	Kilo – 10^3
L	Length
LPF	Low Pass Filter

m	Milli - 10^{-3}
M	Mega - 10^{6}
μ	Micro - 10^{-6}
Ω	Ohms – unit of measurement for resistance
MOS	Metal-Oxide Transistor
NCN	Negative Conductance Network
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
R	Resistor
r_{ds}	Drain-Source resistance of Transistor
T	Temperature in Kelvin
VCCS	Voltage Controlled Current Source
VCT	Voltage-to-Current Transducer
Vdd	Positive Power Supply
VLSI	Very Large Scale Integration
Vss	Negative Power Supply
V_t	Threshold Voltage of Transistor
WBTC	Wide Band Transconductor



Chapter One

Introduction

1.1 Active Resistors in IC Technology

The use of active resistors for VLSI and IC design has become increasingly popular in recent years. Active resistors are resistors that are formed with active devices such as MOS or BJT transistors. The simplest design of an active resistor is by interconnection of the input and output terminals of a transistor, which converts the transconductance of the device to a driving point conductance. This can be achieved in a MOS transistor by connecting the drain and gate terminals together. Using this technique, resistors of values ranging from a few kilo ohms to tens of kilo ohms can be achieved. Higher resistance values can be obtained by simply using the output resistance of the active device, such as r_{ds} of a MOS transistor. These forms of resistances are especially suited in design of simple single stage amplifiers and simple current mirrors as seen in Figure 1.1.

In Figure 1.1(a) the p-channel current mirror (M2 and M3) serves as an active load for the n-channel common source amplifier. The resistance seen by the common-

source amplifier will be approximately equal to r_{ds2}. Similarly, for the cascode current mirror of Figure 1.1(b), M2 serves as the active load for the current mirror formed by M0 and M3. The use of such active devices allows the design of large resistive loads without the presence of excessively bulky resistors or a high voltage power supply. As a result, for a given power supply a larger voltage gain can be achieved when utilizing an active load than would be possible if a discrete resistor were used.

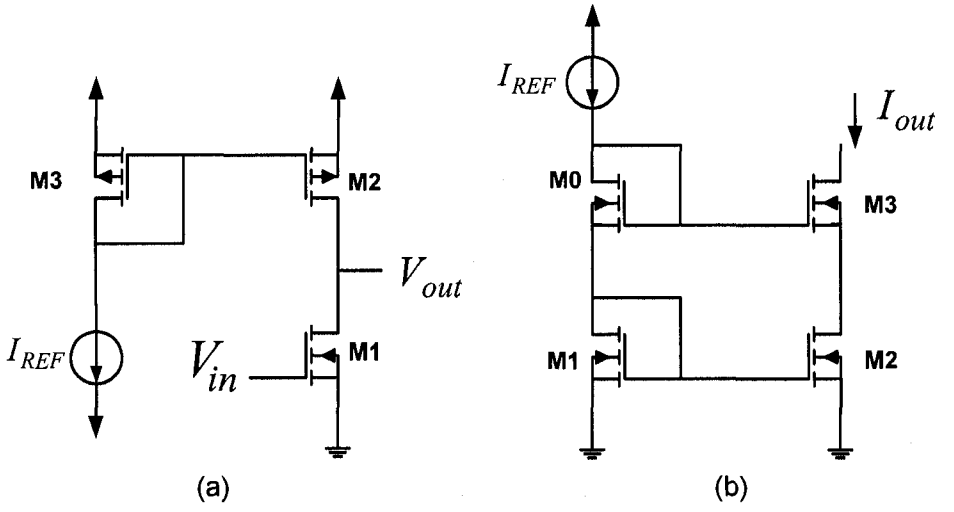


Figure 1.1 - (a) Common source amplifier (b) Cascode current mirror

Active resistors designed in CMOS technology have been widely used for VLSI technology. The conversion of a transconductance amplifier to a driving point impedance is a common configuration that is utilized. The use of CMOS circuits enables the design of active resistors with variable resistance values that are voltage controlled. Voltage controlled resistors have become extensively popular for VLSI technology, and are preferred over resistors made with silicon wafers or diffused resistors. Silicon and

diffused resistors are fixed in value and are much larger in size, which is undesirable for VLSI applications. A single MOS transistor is the simplest form of a voltage controlled resistor, where the resistance between the drain and source of the device is controlled by the gate to source voltage. CMOS technology allows the design of more complex circuits in which multiple voltages determine the output of the system.

1.2 Negative Resistance in VLSI Technology

The DC power supplies of the circuit that control the value of the resistance also influences the polarity, which permits the design of negative resistance circuits. A negative resistance circuit has the property in which the current is a decreasing function of the input voltage over a certain range of voltages, implying an I-V curve with a negative slope. They have the potential of being a key building block for larger electronic systems in VLSI technology. The tunnel and Gunn diodes were the first ever negative resistance devices (introduced in the late 1950s), after which numerous alternate and improved circuits have been reported [1]-[7]. Extensive research in this field is a result of applications in numerous electronic systems that are essential components in VLSI technology [6]-[10].

The most common application of negative resistors is the correction of non-ideal behavior of an electronic system caused by parasitic impedances introduced in the final design. The presence of these parasitic resistances degrades important performance characteristics such as DC gain and bandwidth. Negative resistors are used to overcome these limitations and improve the specifications of the system. Examples of this

application, where a negative resistor has been used to improve a particular characteristic of a larger electronic system are presented below.

1.2.1 Application in OTAs

An OTA (operational transconductance amplifier) is a device that produces an output signal current for an input signal voltage, and is an essential device in VLSI design involving analogue signal processing, in particular for design of current mode filters. A vital performance factor in the design of these devices is the DC gain, which is limited by the parasitic resistances at the output terminal. It is critical to compensate for these parasitic resistances in order to achieve high performance filtering when the device is used for the design of active filters. A negative resistance load has been used to design a linear fully balanced voltage-tunable CMOS OTA with large DC gain and bandwidth [6]. The block diagram of the design is shown in Figure 1.2. Not only is the negative resistance load used to compensate for the parasitic output resistance of the non-ideal OTA, but it also compensates for the parasitic resistance of the non-ideal input source.

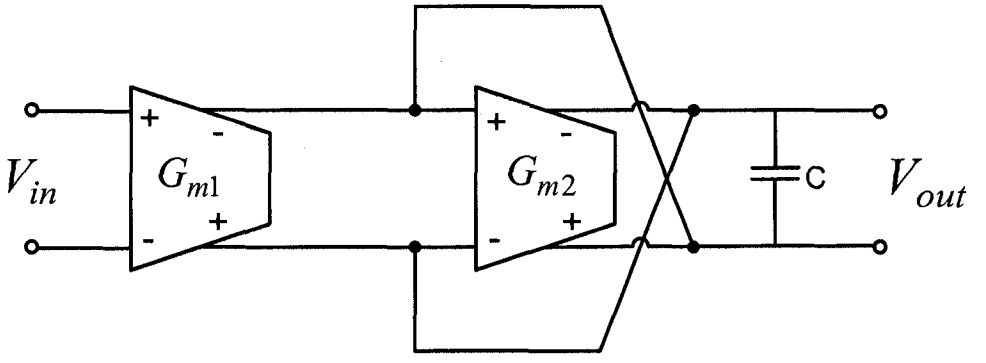


Figure 1.2 – OTA-C integrator with negative conductance output stage

The negative resistance load is implemented using an OTA by introducing local positive feedback between the output terminals, which is shown in Figure 1.2 as the G_{M2} stage. This technique enhances the gain of the OTA-C integrator without the addition of any internal nodes that would generate parasitic poles; hence the frequency performance is not significantly sacrificed. The entire network is simulated in SPICE using the 2 micron process technology. Simulation results show that for a 5 volt power supply the DC gain of the OTA-C integrator is kept well above 55 dB depending on the values of the control voltages used. The OTA was tested in the design of a third order elliptical filter, producing a bandwidth of up to 50 MHz.

1.2.2 Application in Operational Amplifiers

Operational amplifiers represent a highly influential building block for VLSI systems, and are commonly used for the design of active voltage-mode filters. The parasitic resistances introduced in the final design affect the DC gain and bandwidth of the amplifier. A negative conductance, which is connected at the output stage to compensate for the finite output resistance, has been used to design a very high DC gain operational amplifier [8].

Several other techniques for DC gain enhancement of OTA's and op amps have been suggested, however the use of a negative conductance output stage produces the best results without major bandwidth compensation. A commonly used alternative is the folded-cascode structure [11]. Though this approach does not sacrifice any bandwidth, it does however limit the drain-source resistance which decreases as a result of the large

bias current and short channel length transistors. To overcome this effect, a triple cascode output stage was suggested [12], however this approach limited the output swing of the device. The use of a negative conductance output stage will produce a high DC gain without degrading the frequency performance, such as the unity-gain frequency.

1.2.3 Application in CMOS Oscillators

Transconductance amplifiers and operational amplifiers are often used for the design of CMOS oscillators in VLSI technology. The parasitic resistances of these devices affect key performance parameters of the oscillator such as the quality factor and the phase noise. A negative resistor has been used to design an ideal coupled CMOS neural oscillator [9]. The oscillator, shown in Figure 1.3, was designed in AMI 0.5 micron technology using two operational transconductance amplifiers and two capacitors.

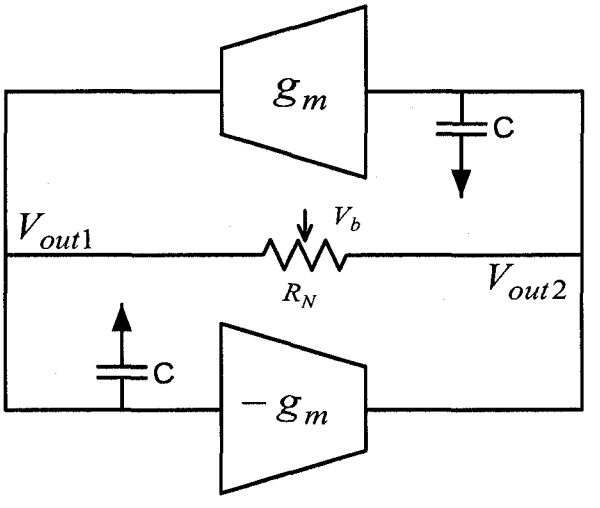


Figure 1.3 – CMOS neural oscillator designed with negative resistor

The non-zero output conductance of the OTAs result in the output waveform of the oscillator converging to a fixed point. A negative resistor is placed between the two output terminals to overcome the parasitic output resistance of the OTAs, thereby achieve a sustained limit cycle oscillation. The configuration utilizes a non-linear CMOS negative resistance as a current supply to compensate for the charge consumed through the output conductance.

1.2.4 Application in Voltage Reference Networks

Voltage reference networks are essential analog building blocks for VLSI and IC technology, and are often used for circuit biasing. A voltage reference network supplies a fixed DC voltage of known magnitude that is temperature independent. Often it is required to source more current than is available from the reference network. One possible solution is to cancel the load by making it appear as a large resistance. Once this is achieved, the remaining part of the load is compromised of any capacitance that may be in parallel with the resistive load. A negative resistor has been used to achieve the load cancellation in the design of a high output drive voltage reference network [10].

Placing a negative resistor of equal magnitude in parallel with the resistive load makes the effective load resistance infinite, with the load now appearing entirely capacitive. In using this design, which is presented in Figure 1.4, there is negligible output error as opposed to other possible approaches such as using a unity gain buffer amplifier. Tests performed on an ultra-stable reference driving 15 mA of current showed that adding the negative resistance enabled the reference to drive 50 mA of current or

more [10]. Load cancellation also minimizes drift current due to self heating caused when the output current is large and the difference between the output and reference voltage is large.

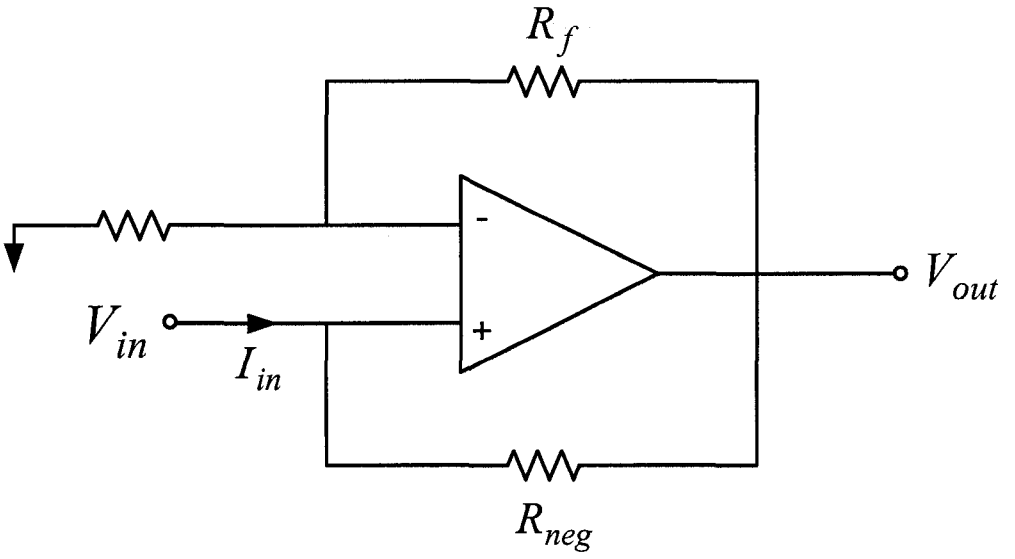


Figure 1.4 - Voltage reference network designed with negative resistor

In the above discussion we have demonstrated the importance of negative resistance circuits in VLSI technology. The negative resistance is used to correct non-idealities of important building blocks such as op amps and OTAs. These non-idealities degrade the characteristics of larger electronic systems that are designed with these building blocks. In the following section some of the negative resistance circuits that have been reported to date are presented.

1.3 Some Negative Resistance Circuits in CMOS Technology

Some of the negative resistance circuits that have been reported in recent years are presented in this section. Advantages of the particular negative resistance over other proposed circuits are discussed where possible. The schematic, expression of the equivalent resistance, and the simulation results of the negative resistance networks are presented, along with a brief description of the application in which they were used.

1.3.1 CMOS Bilateral Floating Resistor [1]

The schematic of a CMOS bilateral floating voltage controlled resistance circuit having both positive and negative values is shown in Figure 1.5.

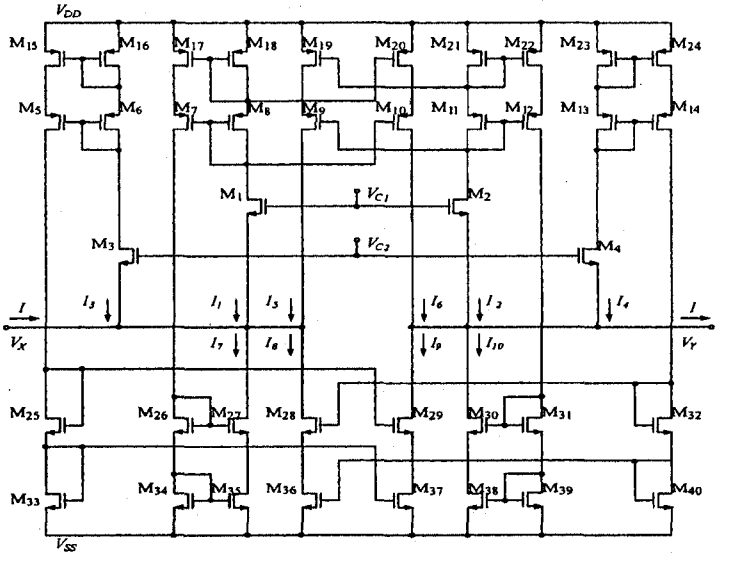


Figure 1.5 – Bilateral floating resistance circuit

The expression for the large signal resistance is given as [1]

$$R = \frac{V_X - V_Y}{I} = \frac{-1}{\beta(V_{C1} - V_{C2})} \quad \ldots(1.1)$$

It is seen from (1.1) that the resistance is made negative by setting the control voltage V_{C1} greater than V_{C2}. It is also observed that the equivalent resistance is independent of the threshold voltage of the transistors; therefore R could be realized precisely so long as the device matching is perfect. The resistance will however be sensitive to temperature and process variations.

The circuit was simulated using HSPICE (level 28) for a 5 volt power rail, with the results presented in Figure 1.6. The I-V curves of Figure 1.6(a) portray an equivalent negative resistance ranging from -1.21 $M\Omega$ to $-\infty$ could be realized. Figure 1.6(b) presents the frequency response of the circuit showing a gain of -6 dB and a bandwidth of 100 KHz. The voltage gain at the output of a simple circuit consisting of a series connection of two resistors, with one being the negative resistor, is used as a test bench to measure the frequency characteristics [1].

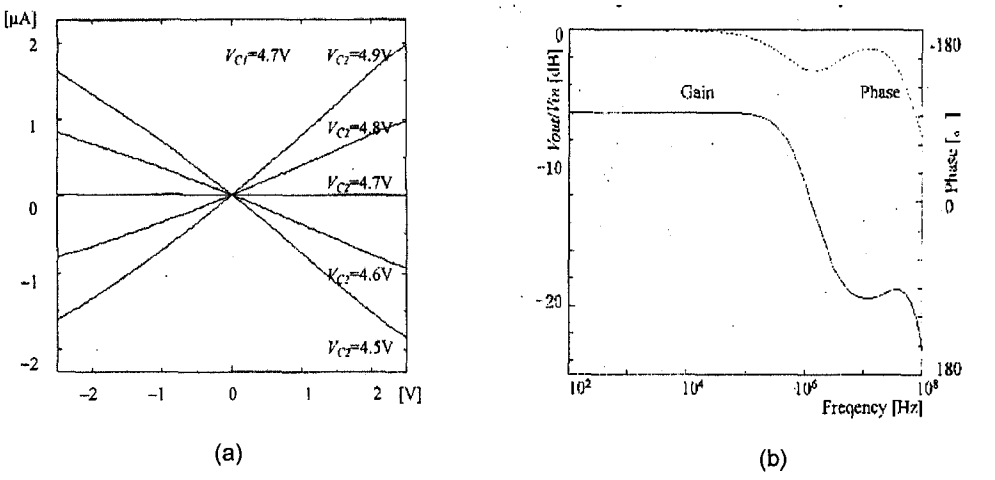


Figure 1.6 – Simulation results of bilateral floating resistance circuit (a) DC simulation (b) Frequency simulation

The proposed circuit was tested using a simple inverting feedback amplifier [1]. A negative resistance of value -1.6 MΩ was employed as the input resistor and a positive resistance of value 0.8 MΩ was used for the feedback resistor. Both resistors were designed with the proposed circuit of Figure 1.5. Simulation results for an input sine wave of frequency 80 KHz concluded that both resistor designs functioned as expected.

1.3.2 Voltage Controlled Negative Resistance Load [6]

A negative resistance load designed with a differential pair of MOS transistors is shown in Figure 1.7. The negative resistance is created by introducing local positive feedback between the two output terminals.

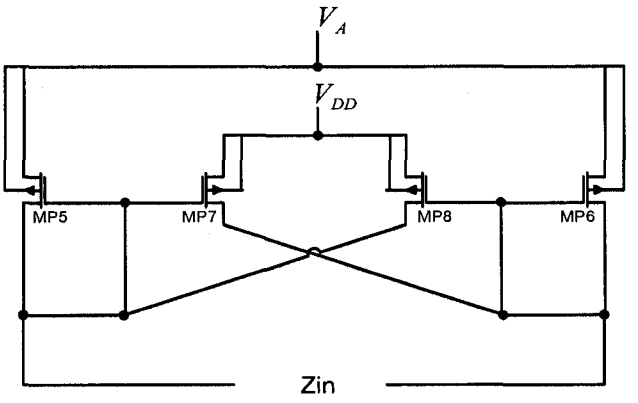


Figure 1.7 - Negative resistance load

The large signal expression for the resistance is given as [6]

$$R_N = \frac{-1}{2K_P(V_{DD} - V_A)} \qquad \ldots(1.2)$$

This result is valid as long as the transistors operate in their saturation region; hence there is a limit on the output of the network, which is given by [6]

$$V_{out} \leq \sqrt{\frac{I_0}{K_P} - \frac{3}{4}(V_{DD} - V_A)^2} - \frac{V_{DD} - V_A}{2} \qquad \ldots(1.3)$$

where $I = 2I_0$ is the bias current provided to the active resistor.

The simulation results in the form of I-V curves are presented in Figure 1.8. The simulation was performed using SPICE level 2 with transistors having a W and L of 12 μm and 2 μm respectively, and a power supply of $V_{DD} = 5$ volts. The control voltage V_A was varied from 4 volts to 4.75 volts, producing a negative resistance ranging from -122

KΩ to -12 KΩ. This particular negative resistance circuit was used in the design of a linear fully balanced OTA that was described in Section 1.2. The negative resistance was used to cancel the parasitic output impedance of the OTA and enhance the DC gain of an OTA-C integrator. An integrator with a DC voltage gain well over 55 dB was designed.

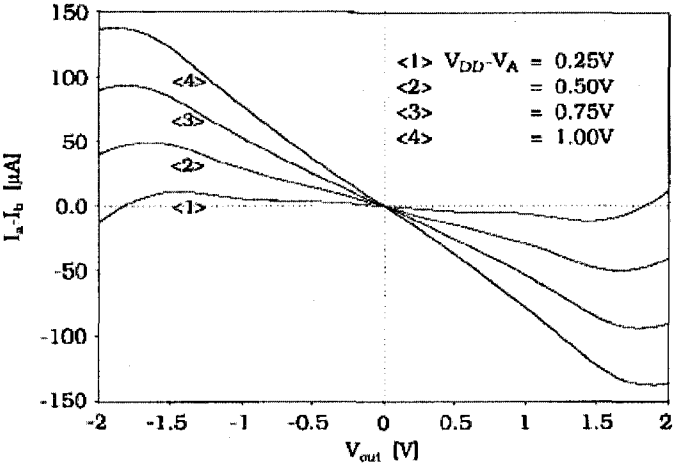


Figure 1.8 - Simulation result of negative resistance load

The negative resistance circuit produces nonlinear negative resistance loads for common mode signals. An alternate circuit that achieves improved linearity is shown in Figure 1.9 [6].

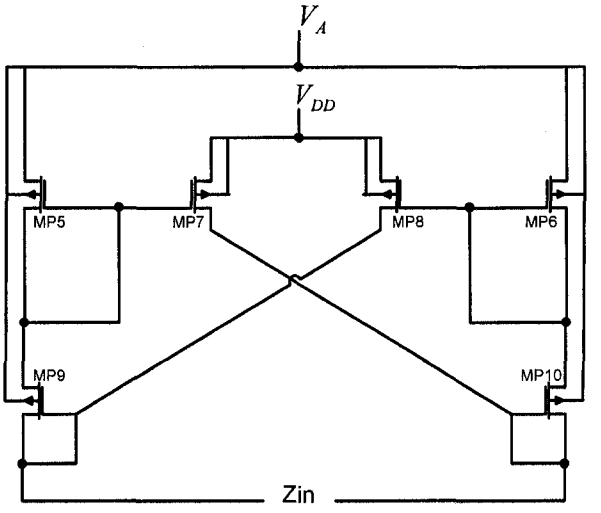


Figure 1.9 -Modified negative resistance load

The expression for the large signal resistance is given as

$$R_N = -\frac{1}{K_P(V_{DD} - V_A)} \qquad \ldots(1.4)$$

and the range of the output voltage is limited by

$$V_{out} \leq \sqrt{\frac{4I_0}{K_P} - 3(V_{DD} - V_A)^2} - (V_{DD} - V_A) \qquad \ldots(1.5)$$

A comparison between (1.3) and (1.5) shows that this modified negative resistance circuit has double the linear output signal range. This is also seen from the simulation results shown in Figure 1.10, where it is observed that the curves have

linearity over a broader voltage range. Identical simulation parameters, control voltages, and power supply values were used for the simulation.

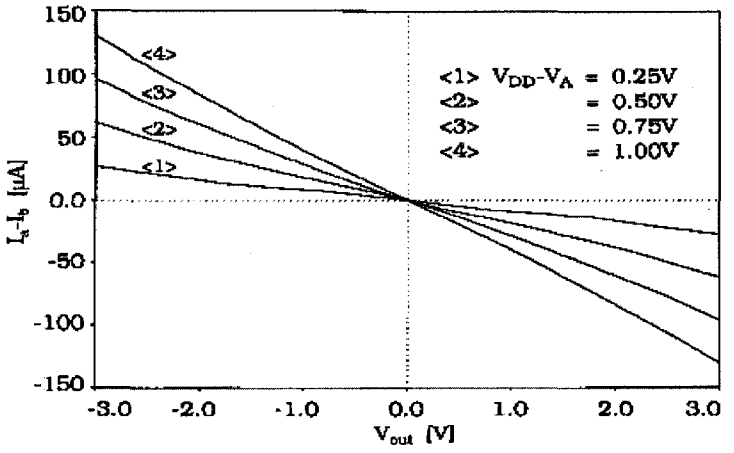


Figure 1.10 – Simulation result of modified negative resistance load

1.3.3 Voltage Controlled Floating Negative Resistor [2]

The floating resistor presented in Figure 1.11 has been designed using a new technique in negative resistance circuit design, which is based on the bisection of the input voltage. This technique allows the design of a fully floating voltage controlled resistor with wide input range, negative slope I-V curves passing through the origin, and very high linearity. The negative resistance is formed using a voltage controlled current source and a JFET operating in the non-saturation region.

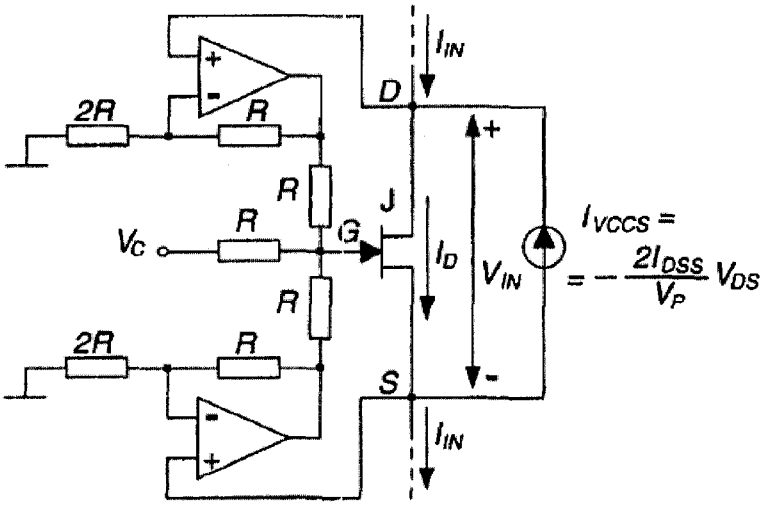


Figure 1.11 - Floating negative resistor

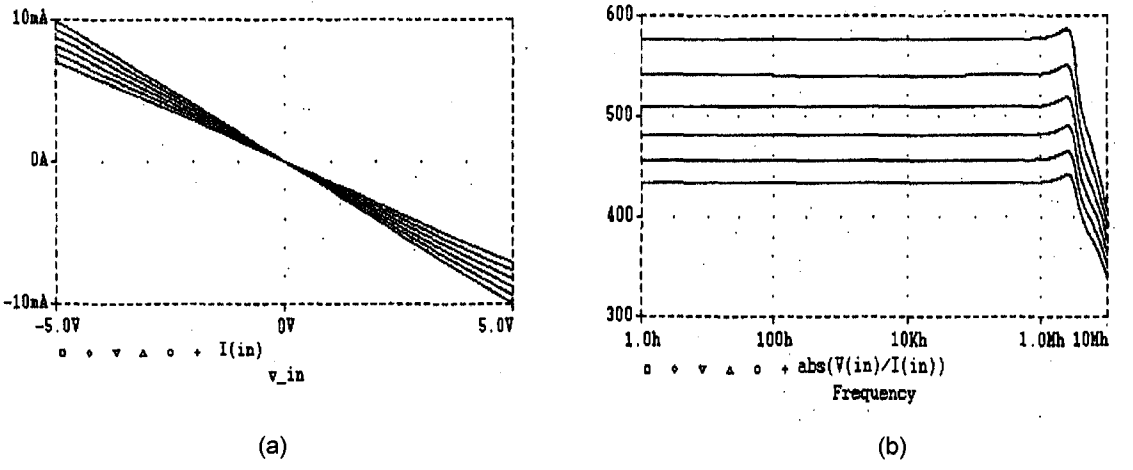
The equivalent resistance between the drain and source of the JFET is determined as [2]

$$R_{EQ} = \frac{V_{DS}}{I_{in}} = \frac{3V_P^2}{2I_{DSS}V_C} \qquad \ldots(1.9)$$

where V_P is the pinch off voltage and I_{DSS} is the saturation current of the JFET. It is indicated from (1.9) that if the control voltage V_C is negative, we have a negative resistor with equivalent resistance that is inversely proportional to this voltage. The VCCS with current $I_{VCCS} = -2I_{DSS}V_{DS}/V_P$ for this circuit was designed using a class AB bipolar implementation of the first generation current conveyor and a resistor $R_{VCCS} = -3V_P/4I_{DSS}$. For integrated circuit design, it is useful to determine the saturation current and pinch off voltage of the JFET, and then realize R_{VCCS} discretely. These two components can then be

added separately to the integrated circuit. This is done as the value of the saturation current and the pinch off voltage of the JFET are fairly unpredictable.

PSPICE simulations were performed to analyze the operation of the proposed circuit. A J2N5364 model JFET was used, along with an LF365 model operational amplifier with a 10 volt power supply and Resistor R_{VCCS} of value 371 Ω. Figure 1.12(a) shows the I-V curves resulting from the DC sweep of the input voltage from -5 volts to 5 volts, and the control voltage from -7.5 volts to -10 volts. The simulation result shows that an equivalent resistance ranging from -577 Ω to -432 Ω is obtained. The frequency response for an input voltage of 5 volts is shown in Figure 1.12(b). The control voltage was again ranged from -7.5 volts to -10 volts. A bandwidth between 1 MHz and 10 MHz is measured.



(a) (b)

Figure 1.12 – Simulation results of floating negative resistor (a) DC simulation (b) Frequency simulation

There could be several possible applications for this proposed negative resistance circuit, such as design of amplifiers and oscillators. The circuit could be ideal for AC applications as biasing techniques would not be needed because the negative resistance has parameters that can be adjusted to the required circuit specification, and has an I-V curve that passes through the origin. Another possible application is in the use of resistance measurements.

1.3.4 Voltage-to-Current Transducer Negative Conductance [7]

A voltage-to-current transducer (VCT) is a device that produces an output current for a given input voltage, and falls under the category of transconductance devices. The VCT is designed using CMOS transistors operating in their respective saturation regions, with the output current being proportional to two differential input voltage signals. The schematic of a differential in single ended output (DISO) VCT is shown in Figure 1.13. The VCT could be used for the design of both a grounded and a floating conductance. The polarity and the values of the resistance that can be realized are dependent on the control voltages V_{c1} and V_{c2}. Further analysis of the VCT as a conductance will be discussed in the coming chapters.

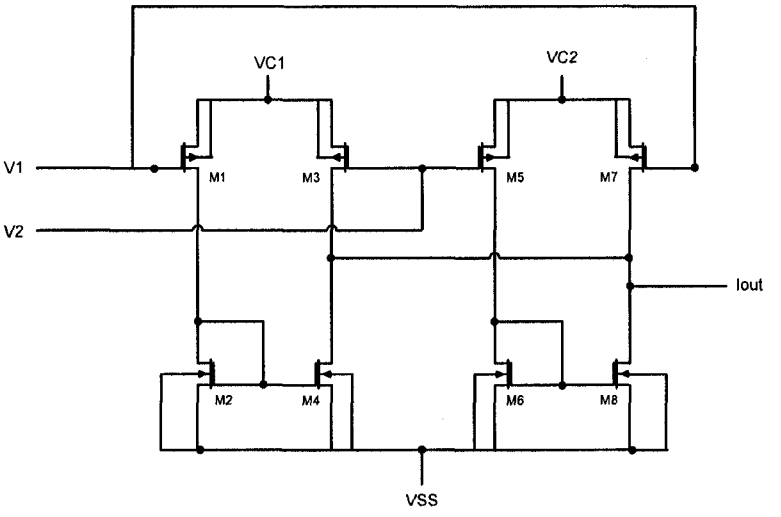


Figure 1.13 – DISO VCT network

1.4 Summary

In this chapter we discussed the advantages of using active resistors in VLSI technology over other excessively large resistors. The active resistors that are designed in CMOS technology have the property of being voltage controlled, and permit the design of negative resistance circuits. We brought forward the increasing popularity of negative resistors in VLSI technology, and expressed how these circuits have the potential of being a key building block for the design of larger electronic systems. This was justified by presenting applications in which negative resistance circuits have been applied, with design of OTAs and op amps being mentioned. Finally, we presented some of the negative resistance circuits that have been reported to date. A summary of the results reported are presented in Table 1.1.

Table 1.1 – Characteristics of reported negative resistance circuits

	Reference [1]	Reference [2]	Reference [6]
Power supply (Volts)	5	10	5
Resistance range	-1.2 MΩ to –inf.	-432 Ω to -577 Ω	-12 KΩ to -121 KΩ
Bandwidth (Hz)	100K	1M to 10M	-

1.5 Motivation for Thesis and Contributions

In all of my research, I came to learn that no work on detailed characterization of negative resistance circuits in CMOS technology has appeared in the current literature. Important characteristics such as noise and power consumption that could be beneficial to other designers and researchers have not been reported. Neither has there been any mention on the stability of the negative resistance circuits.

This thesis presents a detailed study on various negative resistance circuits designed in CMOS technology. Important large signal characteristics are investigated which include resistance range, linearity, noise and power consumption. The data presented will give designers a clear picture on the advantages and disadvantages of each resistor, and help in picking a particular circuit for a specific application. A study of the small signal characteristics reveal important bandwidth and stability concerns that have not previously been addressed. Finally, alternate applications of negative resistors, which include the design of a low phase noise oscillator and high bandwidth amplifier, are presented.

A total of six negative resistors will be investigated in detail for their characteristics, which are

i. VCT designed grounded negative resistor [7]

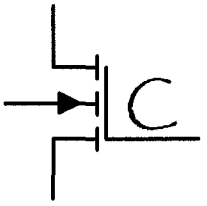
ii. Grounded negative resistance load [6]

iii. Current Conveyor designed grounded negative resistor [13]

iv. Floating negative resistance load [6]

v. Current mirror designed floating negative resistor [8]

vi. Floating negative conductance network [14]



Chapter Two

Large Signal Characteristics

The large signal characteristics of the negative resistance circuits are investigated in this chapter. The expression for the equivalent resistance of each circuit is presented, from which the required condition for the resistance to be negative is identified. The range of resistance values that can be obtained for a design in 0.5 micron CMOS process is investigated, with this data also being used to estimate the linearity with respect to the control voltage. The power consumption and noise of each negative resistance circuit is also examined. Each negative resistor is designed in 0.5 micron CMOS technology with transistors having W and L of 2.5 μm and 1 μm respectively, and a power supply rail of 1.5 volts.

2.1 VCT Grounded Negative Resistor [7]

The schematic of the voltage to current transducer was presented in Chapter 1. The large signal short circuit output current of the differential in single ended out (DISO) VCT of Figure 1.13 is given by [7]

$$i_{out} = \mu_p C_{oxp}\left(\frac{W_p}{L_p}\right)(V_{c1} - V_{c2})(V_1 - V_2) \quad \ldots(2.1)$$

The square law model of the transistors was used to derive (2.1), with the channel modulation factor being ignored. The transconductance characteristic of the DISO VCT allows the design of a grounded driving point conductance, which could be made negative using the control voltages. A possible configuration for the design of a grounded conductance is shown in Figure 2.1, which is achieved by grounding one of the inputs, and shorting the other with the output terminal.

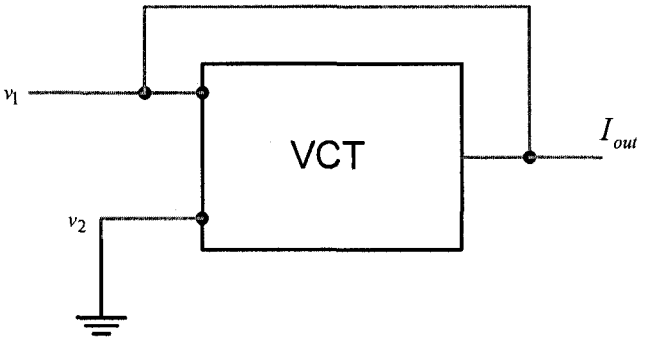


Figure 2.1 – VCT grounded conductance setup

The configuration of Figure 2.1 results in grounded resistance given by [7]

$$R = \frac{-1}{K_p\left(\frac{W_p}{L_p}\right)(V_{c1} - V_{c2})} \quad \ldots(2.2)$$

It is established from (2.2) that this configuration produces a negative resistance as long as the control voltage V_{C1} is larger than V_{C2}. It is also seen that the resistance is independent of the threshold voltage and can be realized precisely if the device matching is perfect.

The NMOS transistor pairs M2-M4 and M6-M8 in Figure 1.14 form current mirrors and serve as active loads for the transconductor. For simplicity, these two current mirrors could be replaced with a single current mirror load. This reduces the number of transistors in the circuit, which fractionally reduces the amount of noise in the system for the transistor sizes chosen in this design. The grounded negative resistor, shown in Figure 2.1, is designed using this modified version of the VCT. It has been verified that using the single current mirror load as opposed to two current mirrors does not change the value of the resistance for a given pair of control voltages, and (2.2) remains valid.

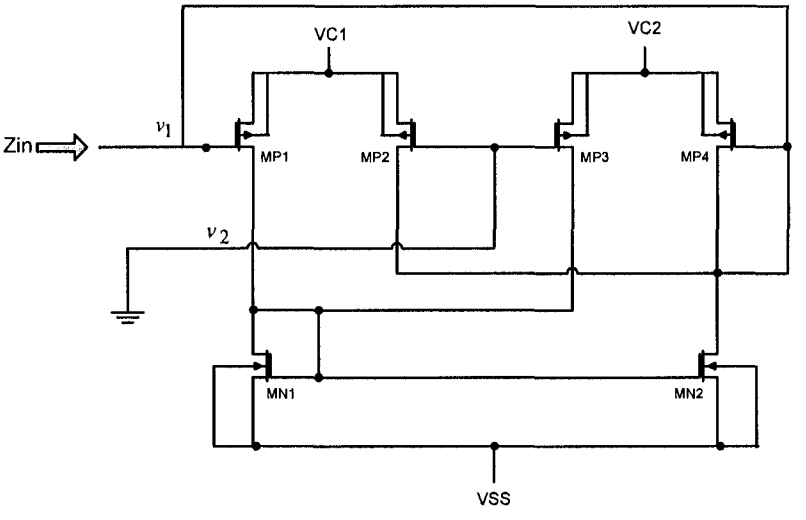


Figure 2.2 – VCT grounded negative resistor with single current mirror load

Figure 2.3 shows the range of negative resistance values that are obtained for a design in 0.5 micron CMOS process. V_{C1} is set constant at 1.5 volts, while V_{C2} is varied for different values less than 1.5 volts until any particular transistor is no longer in the saturation region of operation. This curve is data fitted to obtain an approximate relationship for the resistance value as a function of V_{C2}. The result of this, presented in Table 2.1, is used to estimate the linearity of the grounded negative resistor with respect to the control voltage V_{C2} .

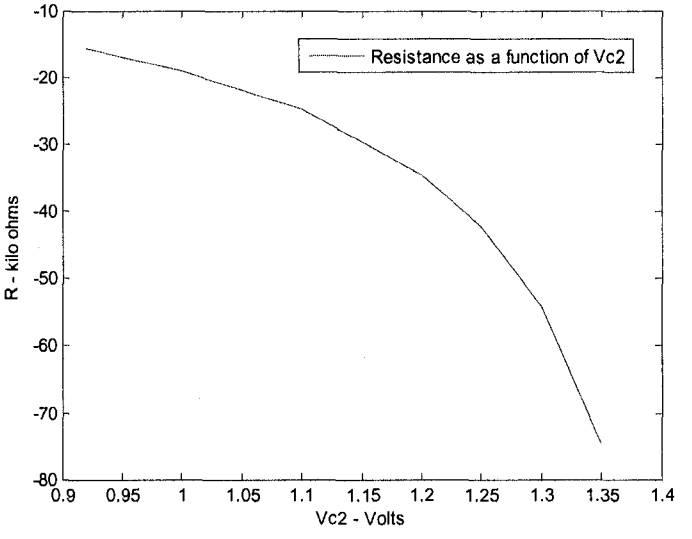


Figure 2.3 – Range of resistance for VCT grounded negative resistor

The I-V curve for a resistance of -20 KΩ is shown in Figure 2.4(a). This curve, along with the gradient of the I-V curve shown in Figure 2.4(b) determines the linearity of the circuit with respect to an input voltage. A highly linear circuit will follow the ohm's law relationship (given as V = IR), and have an I-V curve with a slope of $\frac{1}{R}$. The

gradient of the I-V curve, i.e. $\frac{\partial I}{\partial V}$, will be constant and have a slope of 0. The value of the gradient on the I-V plane corresponds to the admittance of the circuit.

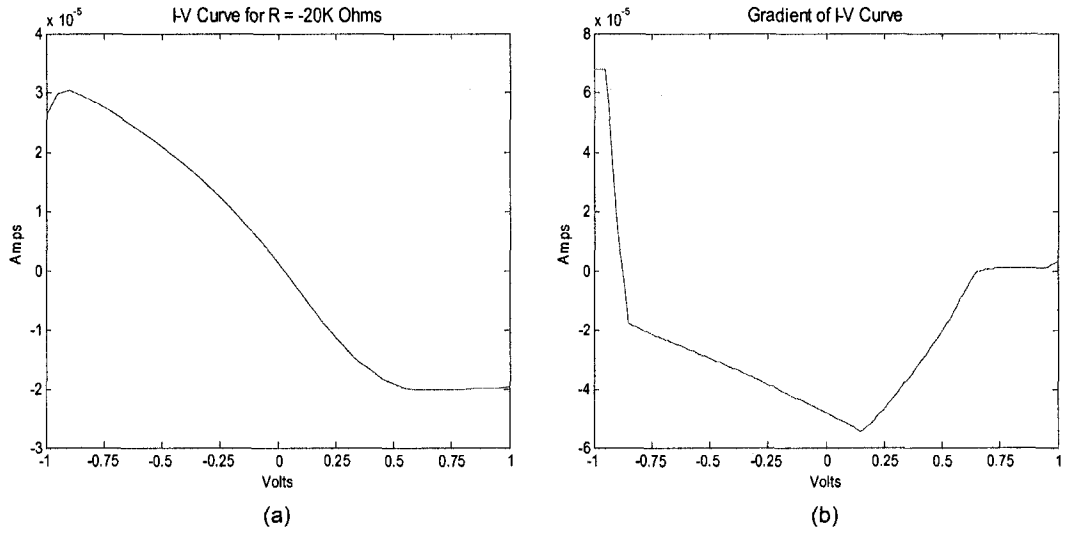


Figure 2.4 – (a) I-V curve of negative resistor (b) Gradient of I-V curve

The noise of the grounded negative resistor has been measured and compared to the thermal noise of a discrete resistance of equal value. The thermal noise of a resistor is given by

$$V_n^2 = 4kTR \quad \ldots(2.3)$$

In (2.3) k is the Boltzmann's constant ($1.38 \times 10^{-23}\ JK^{-1}$), T is the temperature in Kelvin, and R is the value of the resistance for which the noise is being calculated. The test bench shown in Figure 2.5 was used to measure the noise of the system.

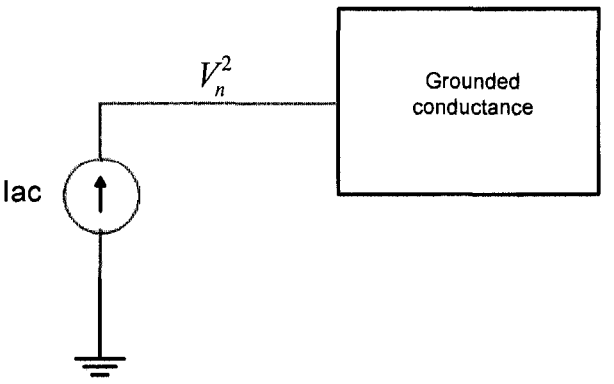


Figure 2.5 – Test bench for noise measurement

Finally, the total power consumed by the circuit for designing a particular resistance value was measured. The total power consumed is the sum of the power dissipated by each of the DC voltage sources in the circuit. The results of all of these investigations are presented in Table 2.1.

Table 2.1 – Characteristics of VCT grounded negative resistor

Range of Resistance	-15 KΩ to -75 KΩ (for 0.9 < Vc2 < 1.35)
Linearity	$R(K\Omega) \approx -3e3x^4 + 1.4e4x^3 - 2.2e4x^2 + 1.5e4x - 4e3$ (As a function of x = Vc2, with Vc1 = 1.5V)
Noise: R = -20 KΩ *4kTR*	1.93e-15 sq. V/Hz 3.31e-16 sq. V/Hz
Power Consumption	1.37e-4 Watts (for R = -20 KΩ)

2.2 Grounded Negative Resistance Load [6]

The schematic of a voltage controlled grounded negative resistance load is shown in Figure 2.6. The resistor is configured with a transconductance amplifier that is designed using two cross coupled differential pairs having identical MOS devices. The transistor pair MN1 and MN2 forms a current mirror and serves as an active load to the transconductor. The voltages V_c and V_r are used to control the values of the resistance that can be obtained. This form of an active resistance provides easy tuning without generating any additional internal nodes, which causes less attenuation in the bandwidth.

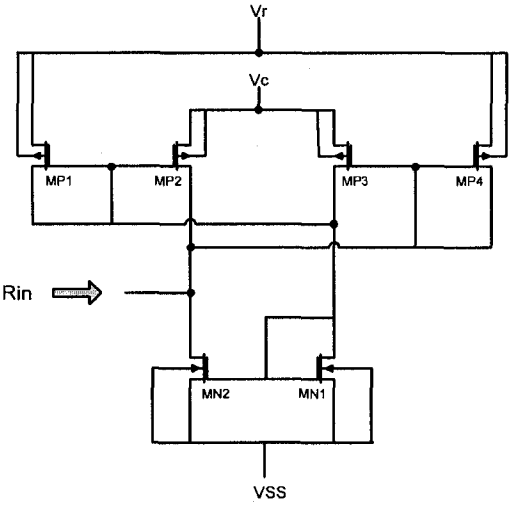


Figure 2.6 –Grounded negative resistance load

The expression for the large signal output current of the transconductor is by [6]

$$I = K_p\left(\frac{W_p}{L_p}\right)(V_r - V_c)V_{in} \qquad \ldots(2.4)$$

Shorting the input and output terminals results in an equivalent resistance given as

$$R = \frac{1}{K_p\left(\frac{W_p}{L_p}\right)(V_r - V_c)} \qquad \ldots(2.5)$$

It is expressed from (2.5) that the resistance is made negative as long as control voltage V_c is greater than V_r. It is also seen that the resistance is independent of the threshold voltage. Figure 2.7 shows the variance of negative resistance as a function of V_r, with V_c held constant at 1.5 volts.

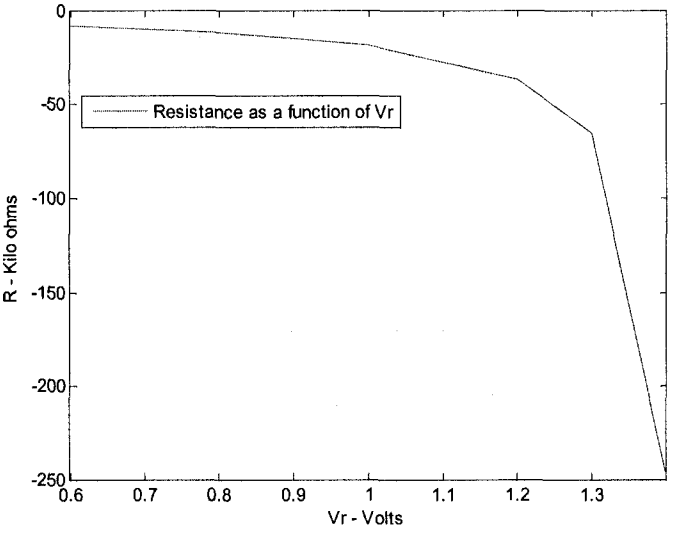


Figure 2.7 – Range of resistance for grounded negative resistance load

The I-V curve for a resistance of -20 KΩ is shown in Figure 2.8(a) with the gradient of the I-V curve shown in Figure 2.8(b). The results for the characteristics of this negative resistor are presented in Table 2.2. It is recognized that this grounded resistor

has a similar physical structure to that of the VCT grounded resistor and has comparable large signal characteristics.

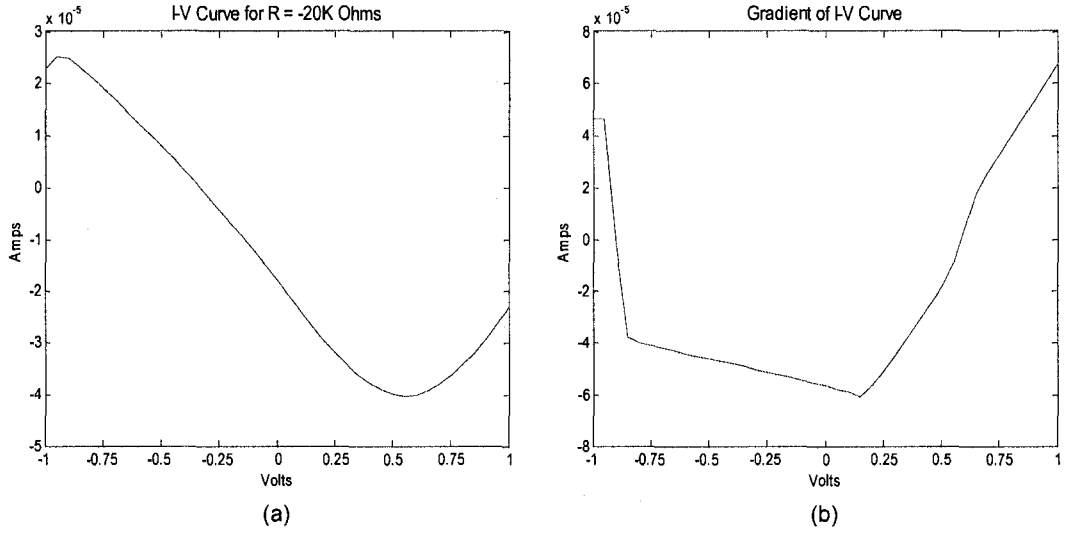


Figure 2.8 – (a) I-V curve of negative resistor (b) Gradient of I-V curve

Table 2.2 – Characteristics of grounded negative resistance load

Range of Resistance	-8 KΩ to -250 KΩ (for $0.6 < Vr < 1.4$)
Linearity	$R(K\Omega) \approx -2.3e3x^5 + 1e4x^4 - 1.7e4x^3 + 1.5e4x^2 - 6.41.5e3x + 1.1e3$ (As a function of x = Vr, with Vc = 1.5V)
Noise: R = -20 KΩ *4kTR*	3.6e-15 sq. V/Hz 3.3e-16 sq. V/Hz
Power Consumption	3.73e-4 Watts (for R = -20 KΩ)

2.3 Current Conveyor Grounded Negative Resistor [13]

A current conveyor is an active four (or five) terminal device which functions like a current controlled current source (CCCS). The device operates by producing an output current signal for a specific input current. Analogous to an op-amp, a current conveyor can be used for various signal processing applications such as current mode active filters. The first ever current conveyor (CCI) was a three port device whose black box representation can be described by Figure 2.9. Similar to an op amp, the two input terminals X and Y operate at the same small signal potential. Therefore, an input small signal current applied to terminal X will result in an equal amount of signal current flowing into terminal Y.

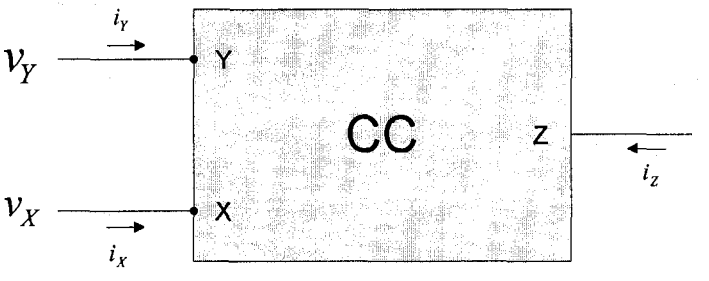


Figure 2.9 – Block diagram of a 3-terminal current conveyor

Terminal Z of the device (the output terminal) has the characteristics of a current source, with high output impedance and output current equal in value to the small signal current applied at the input terminal. The properties of the input terminals show that the device exhibits a virtual short circuit characteristic at port X and a dual open-circuit input

characteristic at port Y. The input-output characteristics of the CCI can be described in mathematical terms by

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad \ldots(2.6)$$

In (2.6) the + sign implies that the current at both terminal Z and X flow into the conveyor, and is denoted by CCI+. The – sign implies opposite polarity between the two terminals, and is denoted by CCI-. Soon after, a more versatile current conveyor in which no current flows into the Y terminal was introduced [13]. This second version is called the CCII, and is mathematically described by

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad \ldots(2.7)$$

The CCII- described by (2.7) is similar to a simple current buffer, with an input current flowing into terminal X flowing out of the output terminal Z. An ideal transistor is the simplest form of a CCII-, with the gate of the transistor replicating terminal Y of a CCII-, the source replicating terminal X, and the drain replicating terminal Z. A CCII- with better performance is designed using a pair of CMOS transistors in the feedback loop of an op-amp, and two stages of a CMOS current mirror to transfer the input current to the output terminal, as shown in Figure 2.10.

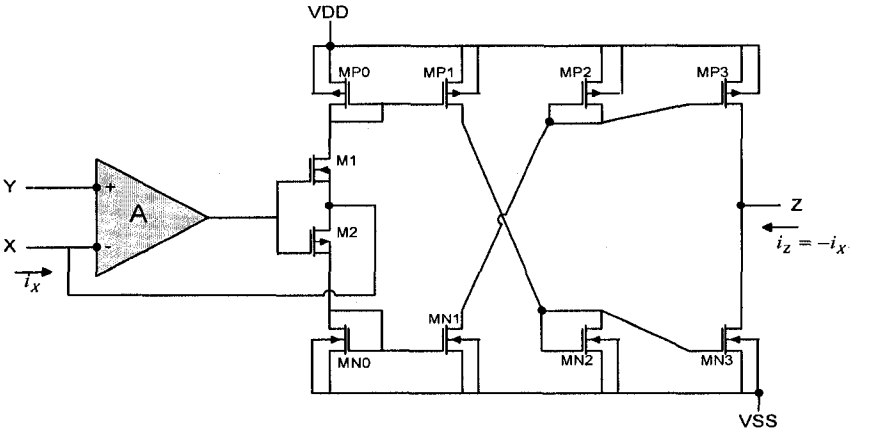


Figure 2.10 – Negative current conveyor, CCII-

The CCII- of Figure 2.10 has been used to design the grounded negative resistor of Figure 2.11. The input is applied directly to the gates of transistors MP1 and MN1, with the output terminal being shorted together with the input. This configuration resembles a transconductor, where an input voltage at the gates of MP1 and MN1 generates a current through the drains of the respective transistors. These currents are then transferred to the output terminal via the current mirrors.

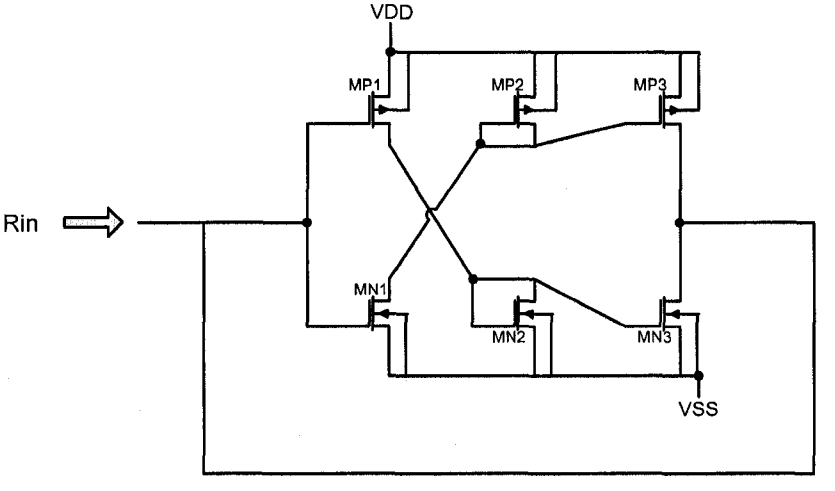


Figure 2.11 – CC grounded negative resistor

The short circuit output current of the transconductor in Figure 2.11 has been determined as

$$I_{out} = K\left(V_{ss} - V_{DD} + V_{tn} + |V_{tp}|\right)\left(V_{ss} + V_{DD} - 2V_{in} + V_{tn} - |V_{tp}|\right) \qquad \ldots(2.8)$$

For this design the transistors are sized such that $K = K_p\left(\frac{W}{L}\right)_P = K_n\left(\frac{W}{L}\right)_n$. The equivalent resistance is then given by

$$R = \frac{1}{2K\left(V_{ss} - V_{DD} + V_{tn} + |V_{tp}|\right)} \qquad \ldots(2.9)$$

It is seen from (2.9) that the resistance is negative as long as V_{DD} is greater than V_{ss}. It is also noticed that the resistance is dependant on the supply voltages; therefore the PSRR of this circuit is likely to be of concern. Figure 2.12 shows the variance of the resistance as a function of V_{DD}, with V_{ss} held constant at -1.5 volts. The I-V curve for a resistance of -20 KΩ is presented in Figure 2.13. All of the characteristics of this resistor are presented in Table 3.3. It is recognized that the power consumption of this design is considerably smaller than the previous two grounded resistors. This is a result of fewer DC voltage supplies employed in the design. This feature also reduced the amount of noise in the system.

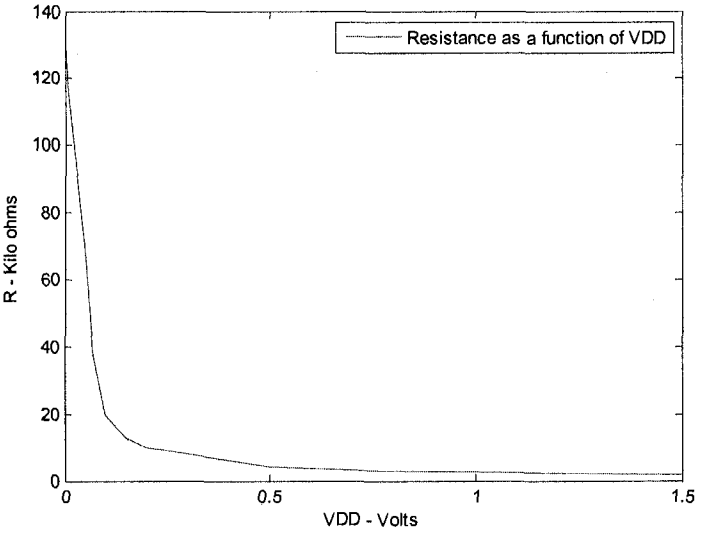


Figure 2.12 – Range of resistance for CC grounded negative resistor

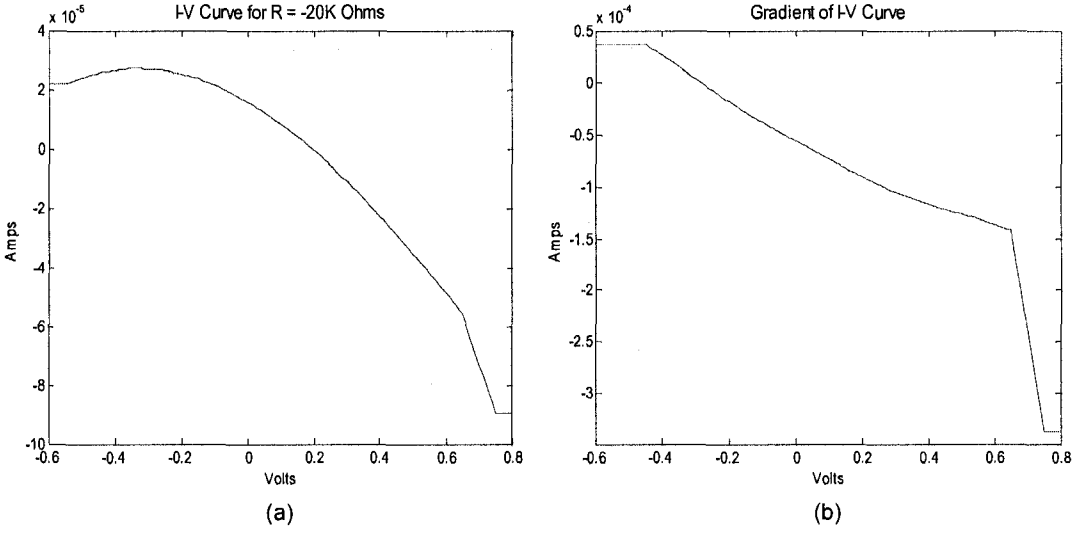


Figure 2.13 – (a) I-V curve of negative resistor (b) Gradient of I-V curve

Table 2.3 – Characteristics of CC grounded negative resistor

Range of Resistance	-2 KΩ to -131 KΩ (for 0 < Vdd < 1.5)
Linearity	$R(K\Omega) \approx -1e3x^5 + 5e3x^4 - 7e3x^3 + 5e3x^2 - 1e3x + 125$ (As a function of x = VDD)
Noise: R = -20 KΩ *4kTR*	6.56e-16 sq. V/Hz 3.3e-16 sq. V/Hz
Power Consumption	6e-6 Watts (for R = -20 KΩ)

2.4 Floating Negative Resistance Load [6]

Figure 2.14 shows a floating negative resistance load designed with a differential pair transconductance amplifier. The transconductor is identical to the one used in the design of the grounded negative resistance load of Section 2.2, and is actively loaded with a pair of transistors (MN1 and MN6) operating in their respective saturation regions.

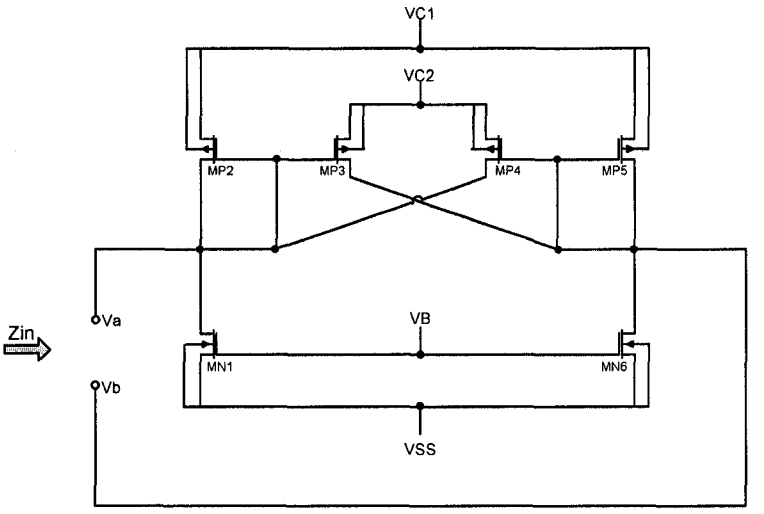


Figure 2.14 – Floating negative resistance load

The equivalent resistance of the floating resistor can be determined as

$$R = \frac{-1}{K_p\left(\frac{W_p}{L_p}\right)(V_{c2} - V_{c1})} \qquad \ldots(2.10)$$

It is seen from (2.10) that the resistance is negative as long as control voltage V_{C1} is less than V_{C2}. Figure 2.15 shows the variance of the resistance as a function of V_{C1}, with V_{C2} held constant at 1.5 volts. The I-V curve for a resistance of -50 KΩ is presented in Figure 2.16, and the results of the investigated characteristics presented in Table 2.4.

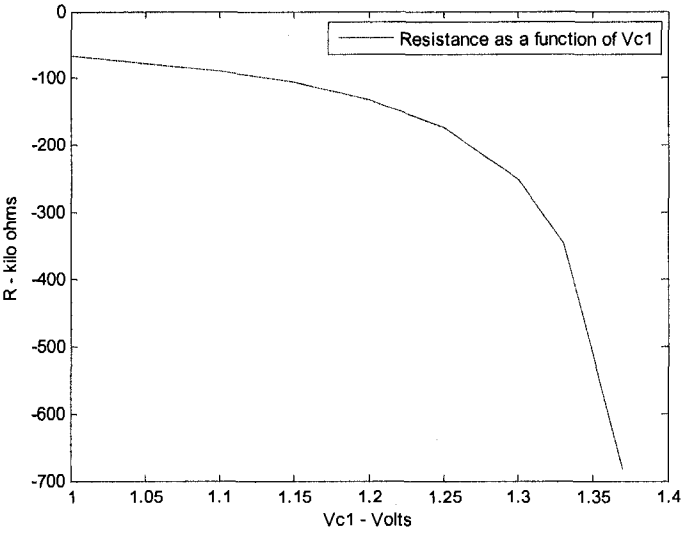


Figure 2.15 – Range of resistance for floating negative resistance load

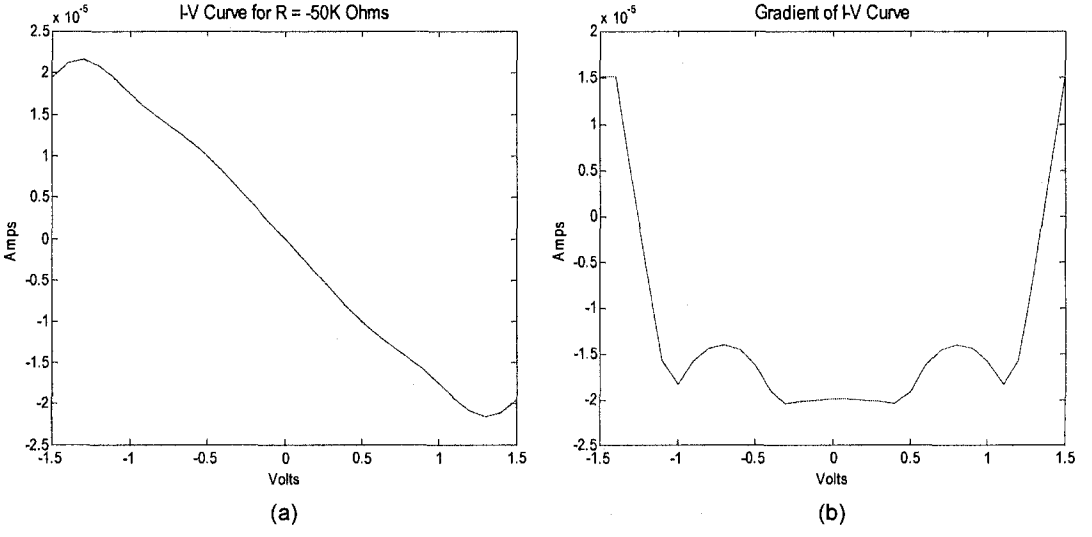


Figure 2.16 – (a) I-V curve of negative resistor (b) Gradient of I-V curve

Table 2.4 – Characteristics of floating negative resistance load

Range of Resistance	-50 KΩ to -700 KΩ (for 0.8 < Vc1 < 1.4)
Linearity	$R(K\Omega) \approx -1e7x^6 + 7e7x^5 - 2e8x^4 + 3e8x^3 - 3e8x^2 + 1e8x - 2.6e7$ (As a function of x = Vc1, with Vc2 = 1.5 V)
Noise: R = -50 KΩ *4kTR*	3.24e-15 sq. V/Hz 8.28e-16 sq. V/Hz
Power Consumption	6.7e-4 Watts (for R = -50 KΩ)

2.5 Current Mirror Floating Negative Resistor [8]

Figure 2.17 shows a floating negative resistor that is designed using two cross coupled current mirrors MN2 – MN5. Transistor pair MP1 and MP6 serves as an active load to the negative resistor. This form of negative resistance has been used in the design of op-amps and OTAs, where the resistor is connected at the output stage to cancel the output conductance of the device. This approach enables the designer to obtain an active device with extremely high DC gain.

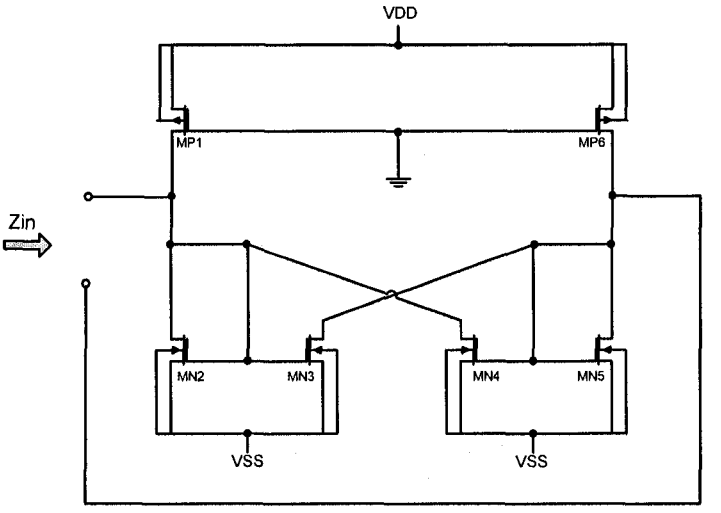


Figure 2.17 – Cross coupled current mirror floating negative resistor

The circuit of Figure 2.17 has been modified in order to design a negative resistance circuit with improved voltage control characteristics. This design, shown in Figure 2.18, is identical to the floating negative resistance load of Section 2.4, except that the transconductor is formed with NMOS transistors. The design employs fewer DC power supplies and will have less power consumption than the circuit of Figure 2.17. Transistors MP1 and MP6 operate in the triode region and serve as active loads to the transconductor.

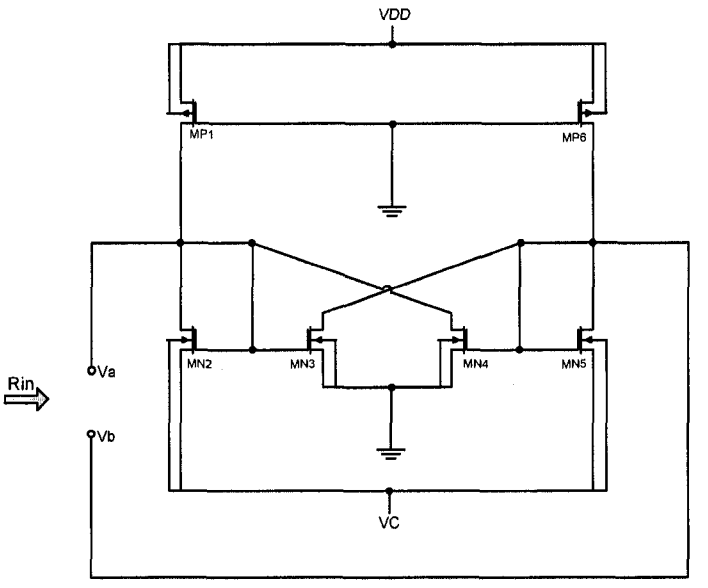


Figure 2.18 – Modified current mirror floating negative resistor

The expression for the equivalent resistance of Figure 2.18 is given by

$$R = \frac{-1}{K_n\left(\frac{W_n}{L_n}\right)V_c} \qquad \ldots(2.11)$$

The variance of the resistance as a function of Vc is shown in Figure 2.19, with Vdd held constant at 1.5 volts. The results of this, along with all the other characteristics of this floating negative resistor are presented in Table 2.5. The I-V curve for a resistance of -20 KΩ is presented in Figure 2.20.

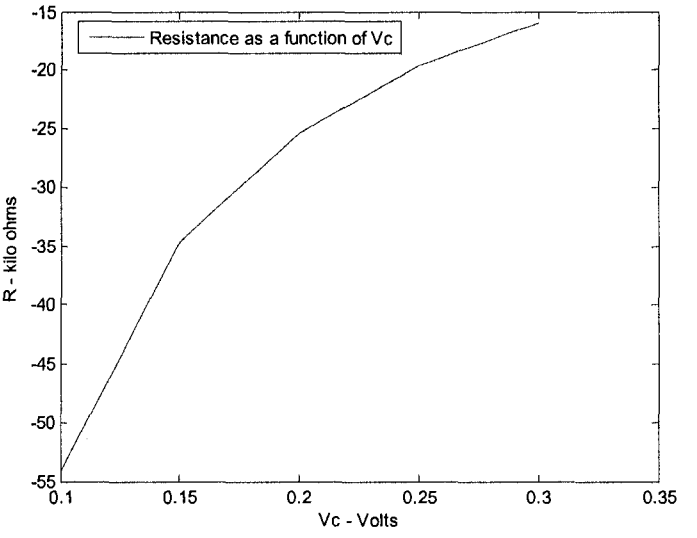


Figure 2.19 – Range of resistance for current mirror floating negative resistor

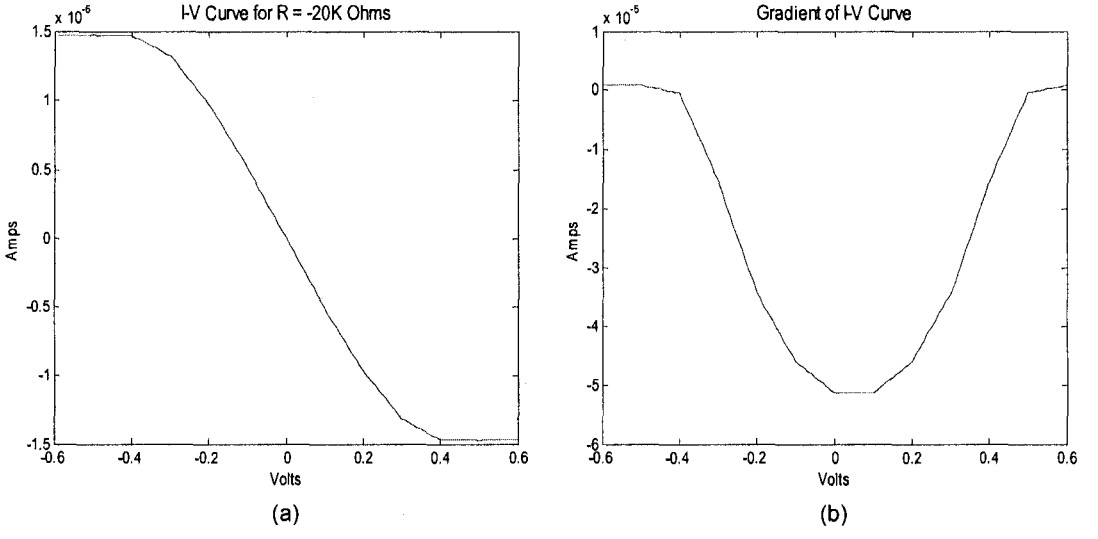


Figure 2.20 – (a) I-V curve of negative resistor (b) Gradient of I-V curve

Table 2.5 – Characteristics of current mirror floating negative resistor

Range of Resistance	-15 KΩ to -55 KΩ (for 0.1 < Vc < 0.3)
Linearity	$R(K\Omega) \approx -3e4x^4 + 3e4x^3 - 1e4x^2 + 2e3x - 170$ (As a function of x = Vc)
Noise: R = -20 KΩ *4kTR*	3.45e-16 sq. V/Hz 3.31e-16 sq. V/Hz
Power Consumption	6.58e-5 Watts (for R = -20 KΩ)

2.6 Floating Negative Conductance Network [14]

Figure 2.21 shows the schematic of a CMOS wideband transconductor (WBTC). The WBTC is designed such that the gate-drain overlap capacitance effects are negligible, which increases the flat band operation of the transconductor to extremely high frequencies. This is achieved by sizing the transistor dimensions accordingly, and by using a fully differential signal at the input.

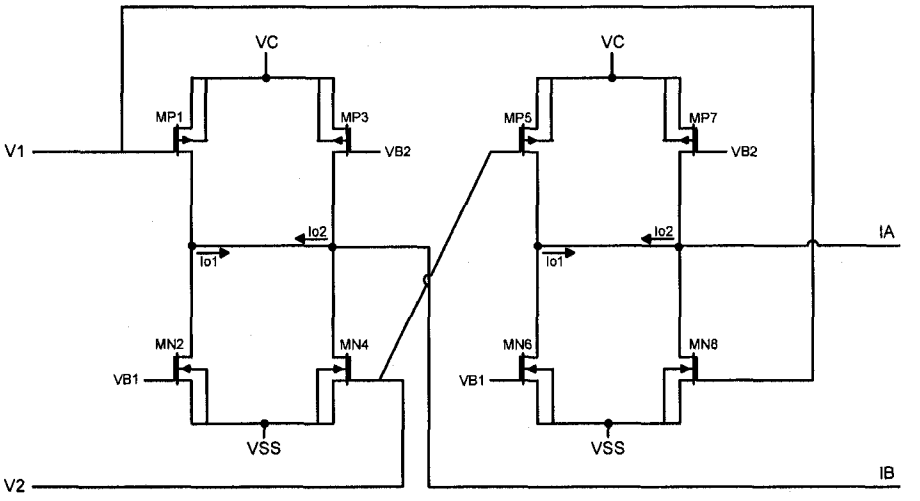


Figure 2.21 – Wideband transconductor network

The large signal differential short circuit output current of the WBTC for a differential input ($V_1 = V, V_2 = -V$) is given by [14]

$$I_{out} = -4V\left(\beta_1\left(V_c - |V_{tp}|\right) + \beta_4\left(V_s - V_{tn}\right)\right) \qquad \ldots(2.12)$$

In order to cancel the gate-drain capacitance effects, the transconductor is designed with transistor dimensions and DC bias voltages such that the residual currents $i_{01} = i_{02} \approx 0$ when there is no signal applied at the input, i.e. $V_1 = V_2 = 0$. Once this is achieved, applying a fully differential signal at the input ($V_1 = v, V_2 = -v$) makes the parasitic capacitances C_{gdM1} and C_{gdM4} equal, which cancels the feed forward signals at the output nodes. For a 0.5 micron process, the transconductor is designed with the transistor dimensions and bias voltages shown in Table 2.6. This design gives a WBTC with $i_{01} = 20.15\ nA$, $i_{02} = 14\ nA$, $C_{gdMP1} = 1.34e-15\ F$ and $C_{gdMN4} = 1.36e-15F$.

Table 2.6 – WBTC design parameters

Transistors	W (um)	L (um)
MP1, MP5	5	1.5
MP3, MP7	5.48	1.5
MN2, MN6	5.48	1.5
MN4, MN8	3.91	1.5
Vc1 = Vc2 = -Vss = 1.5 volts Vb1 = -0.58 volts, Vb2 = -0.84 volts		

The WBTC has been used to design the floating negative conductance network (NCN) shown in Figure 2.22 [14].

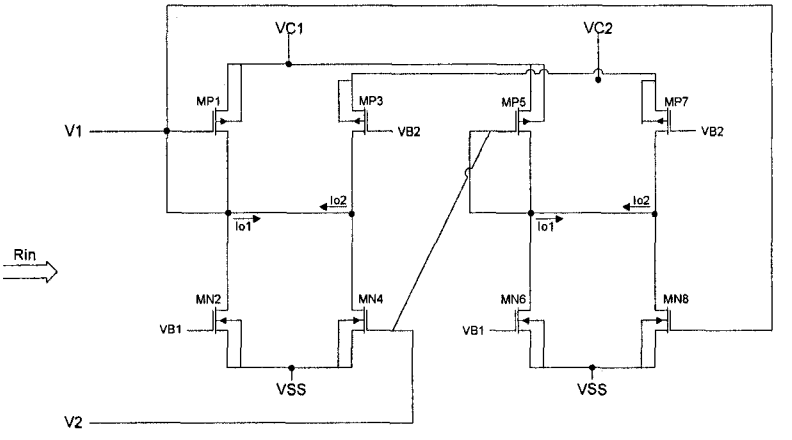


Figure 2.22 – Floating negative conductance network (NCN)

The equivalent resistance of the circuit has been determined as

$$R = \frac{-1}{4\left(\beta_1\left(V_{c1} - \left|V_{tp}\right|\right) + \beta_2\left(V_s - V_{tn}\right)\right)} \quad \ldots(2.13)$$

Figure 2.23 shows the variance of the resistance as a function of V_{c1}, with the I-V curve for a resistance of -10 KΩ presented in Figure 2.24. The large signal characteristics of this negative resistor are displayed in Table 2.7. It is noticed that this negative resistance has the best linearity with respect to the control voltage of all the circuits that have been investigated.

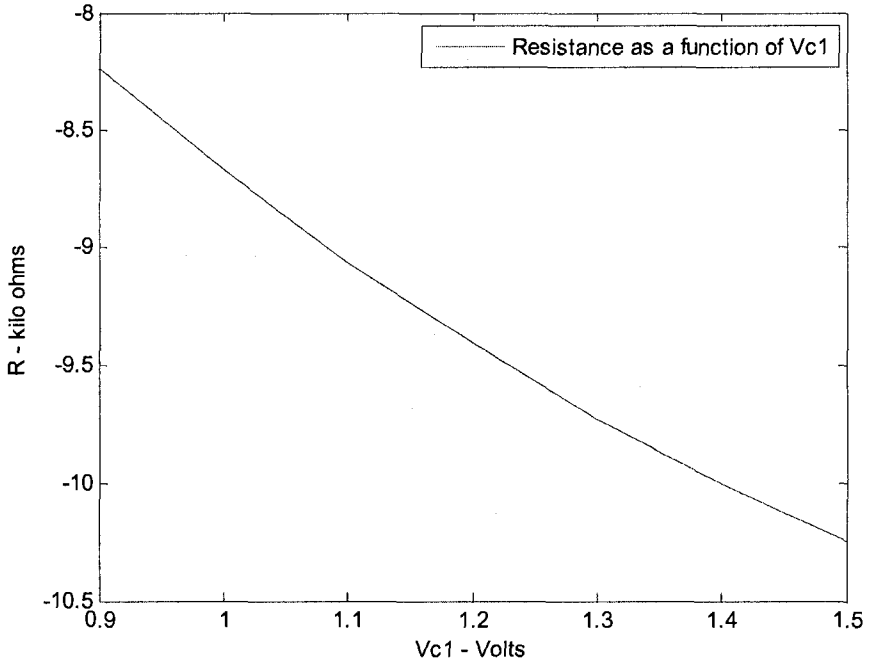


Figure 2.23 – Range of resistance for floating NCN

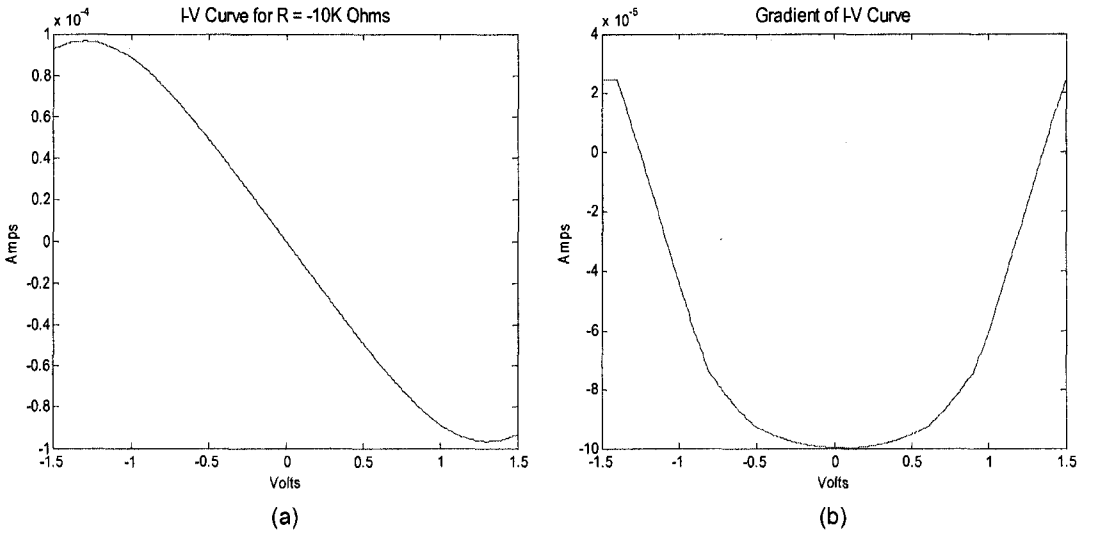


Figure 2.24 – (a) I-V curve of negative resistor (b) Gradient of I-V curve

Table 2.7 – Characteristics of floating NCN

Range of Resistance	-8 KΩ to -11 KΩ (for 0.9 < Vc1 < 1.4)
Linearity	$R(K\Omega) \approx 1.86\,x^2 + 7.8\,x - 2.72$ (As a function of x = Vc1)
Noise: R = -10 KΩ *4kTR*	2.5e-16 sq. V/Hz 1.7e-16 sq. V/Hz
Power Consumption	9.6e-4 Watts (for R = -10 KΩ)

2.7 Summary

The results of large signal characteristics for six negative resistance circuits were investigated in this chapter. The data presented could be useful in selecting a particular negative resistor for a specific design in which certain characteristics are desirable, such as low noise amplifiers. Table 2.8 summarizes a comparison between each of the grounded and floating negative resistors, where a ranking of 1 implies the best performance. Not all of the characteristics of the floating negative resistors have been ranked as identical resistance values cannot be achieved for the power supply and dimensions of the transistors used. The linearity in Table 2.8 is with respect to the control voltage.

Table 2.8 – Comparison of large signal characteristics

Grounded Negative Resistors:			
	VCT based [7]	Transconductor based [6]	Current conveyor based [13]
Range	-15 KΩ to -75 KΩ	-8 KΩ to -250 KΩ	-2 KΩ to -131 KΩ
Linearity	1	2	2
Noise	2	3	1
Power	2	3	1
Floating Negative Resistors:			
	Current mirror based [8]	Transconductor based [6]	NCN [14]
Range	-15 KΩ to -55 KΩ	-50 KΩ to -700 MΩ	-8 KΩ to -11 KΩ
Linearity	2	3	1
Noise (sq. V/Hz)	3.45e-16, R = -20 KΩ	3.24e-15, R = -50 KΩ	2.5e-16, R = -10 KΩ
Power (Watts)	6.58e-5, R = -20 KΩ	6.7e-4, R = -50 KΩ	9.6e-4, R = -10 KΩ

Figure 2.25 shows the gradient of the I-V curves for each of the grounded negative resistors plotted on the same axes. From the figure we see that the VCT resistor of Section 2.1 and the grounded negative resistance load of Section 2.2 have similar linearity characteristics. We also notice that the CC grounded negative resistor of Section 2.3 has poor linearity at the input in comparison with the other two circuits. The results of the floating negative resistors show that the circuits have very high linearity over a specific range of voltages.

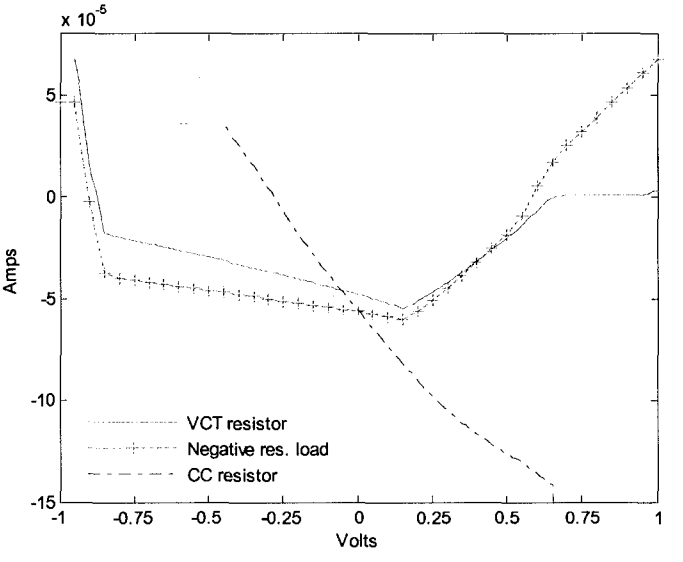
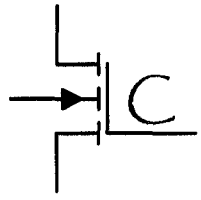


Figure 2.25 – Linearity comparison of grounded negative resistance circuits



Chapter Three

Small Signal Characteristics

The small signal characteristics of the negative resistance circuits are studied in this chapter. The AC equivalent model, which includes the transistors' parasitic capacitors, is used to derive the nodal admittance matrix and evaluate the frequency response expression. The distribution of the poles and zeros are analyzed, which are used to estimate the bandwidth of the resistors. In this chapter we also discuss some considerations regarding the prospect of designing wide bandwidth negative resistors. Finally, the stability of the negative resistance circuits will be addressed.

3.1 VCT Grounded Negative Resistor

The AC equivalent model for the grounded VCT resistor of Figure 2.2 is shown in Figure 3.1. This model includes the transistors' parasitic capacitances which influence the characteristics of the resistance at higher frequencies.

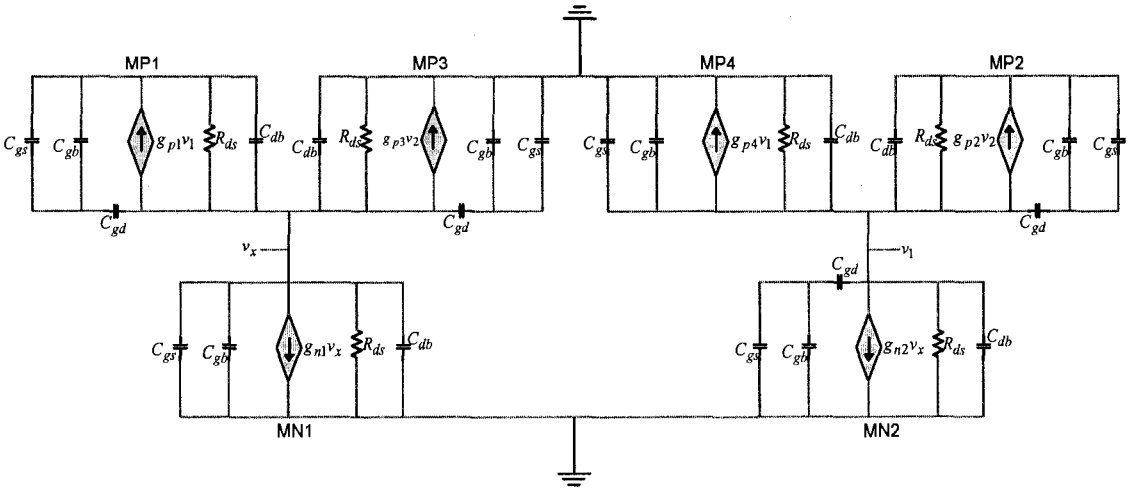


Figure 3.1 –AC equivalent model of VCT grounded resistor

The nodal admittance matrix of the AC model can be derived as

$$\begin{bmatrix} sB_1 + G_1 & sB_{1x} \\ sB_{x1} & sB_x + G_x \end{bmatrix} \begin{bmatrix} v_1 \\ v_x \end{bmatrix} = \begin{bmatrix} i_1 - g_{p4}v_1 - g_{n2}v_x \\ -g_{p1}v_1 - g_{n1}v_x \end{bmatrix} \qquad \ldots(3.1)$$

The details describing the admittance matrix elements are presented in Table 3.1. The expression for the resistance is evaluated as

$$R = \frac{v_1}{i_1} = \frac{sB_x + G_x + g_{n1}}{s^2(B_1B_x - B_{1x}B_{x1}) + s\begin{pmatrix} B_1(G_x + g_{n1}) + B_x(G_1 + g_{p4}) \\ -B_{1x}g_{p1} - B_{x1}g_{n2} \end{pmatrix} + \begin{pmatrix} (G_1 + g_{p4})(G_x + g_{n1}) \\ -g_{p1}g_{n2} \end{pmatrix}} \qquad \ldots(3.2)$$

Table 3.1 – Details describing admittance matrix elements

$B_1 = C_{dbn\,2} + C_{gdn\,2} + C_{dbp\,2} + C_{gdp\,2} + C_{dbp\,4} + C_{gbp\,4} + C_{gsp\,4} + C_{gdp\,1} + C_{gbp\,1} + C_{gsp\,1}$
$B_x = C_{gsn\,1} + C_{gbn\,1} + C_{dbn\,1} + C_{dbp\,1} + C_{gdp\,1} + C_{dbp\,3} + C_{gdp\,3} + C_{gsn\,2} + C_{gbn\,2} + C_{gdn\,2}$
$B_{1x} = B_{x1} = -C_{gdp\,1} - C_{gdn\,2}$; $G_1 = g_{dp\,4} + g_{dp\,2} + g_{dn\,2}$; $G_x = g_{dp\,1} + g_{dp\,3} + g_{dn\,1}$

For simplicity (3.2) is written in the form

$$R = \frac{s n_1 + n_0}{s^2 d_2 + s d_1 + d_0} \qquad \ldots(3.3)$$

The value of the resistance at low frequency and the phase characteristics of the resistor can be identified from (3.2) and (3.3). The resistance value at low frequencies is given as

$$R_{DC} = \frac{n_0}{d_0} = \frac{G_x + g_{n1}}{(G_1 + g_{p4})(G_x + g_{n1}) - g_{p1} g_{n2}} \qquad \ldots(3.4)$$

and the phase (in radians) of the resistor is given by (using $s = j\omega$)

$$\theta = \tan^{-1}\left(\frac{\omega n_1}{n_0}\right) - \tan^{-1}\left(\frac{\omega d_1}{d_0 - \omega^2 d_2}\right) \qquad \ldots(3.5)$$

Figure 3.2 presents the simulation result relating the magnitude and phase of the negative resistor as a function of frequency. The simulation result is for a design in 0.5 micron CMOS process.

The bandwidth of the resistor is dependent on the distribution of the poles and zeros, which can be located by determining the roots of the denominator and numerator of (3.2). The poles and zeros of the negative resistance whose magnitude and phase characteristics are shown in Figure 3.2 are presented in Table 3.2. It is noticed from the results that one of the poles is at a much lower frequency than the others. This pole has

the most influence on the frequency response of the resistor, and is labeled as the dominant pole. The value of the dominant pole often defines the bandwidth of a system. To be more precise, the bandwidth of a system having a dominant pole can be approximated by [15]

$$BW \approx \frac{1}{\sqrt{\left(\frac{1}{p_1^2}+\frac{1}{p_2^2}+..\frac{1}{p_n^2}\right)-2\left(\frac{1}{z_1^2}+\frac{1}{z_2^2}+..\frac{1}{z_n^2}\right)}} \qquad ...(3.6)$$

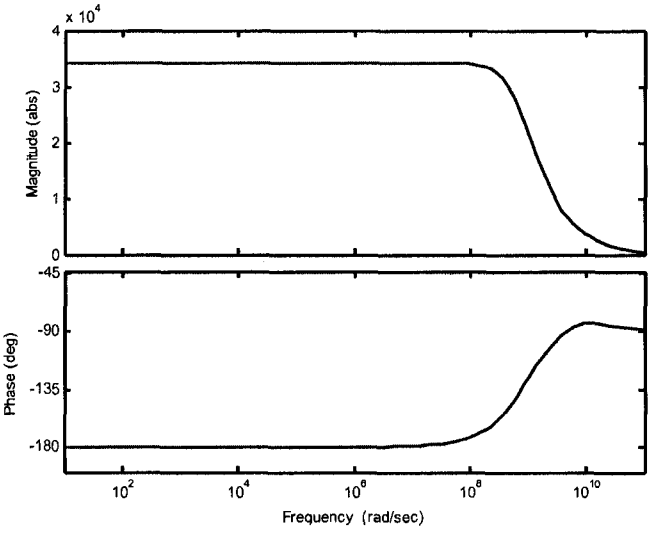


Figure 3.2 – Frequency simulation of VCT grounded negative resistor

The product of the resistance magnitude and the bandwidth is used as a figure of merit for comparing the various negative resistors (analogous to the gain bandwidth product of an amplifier). The value of the dominant pole, which dictates the bandwidth of the resistor, can be predicted from (3.2) and (3.3) as

$$P_{Dom} = \frac{d_0}{d_1} = \frac{(G_1 + g_{p4})(G_x + g_{n1}) - g_{p1} g_{n2}}{B_1 (G_x + g_{n1}) + B_x (G_1 + g_{p4}) - B_{1x} g_{p1} - B_{x1} g_{n2}} \quad \ldots(3.7)$$

An expression for the figure of merit, which we defined as the product of the resistance magnitude and the bandwidth, is then given by

$$FOM = \frac{d_0}{d_1} \times \frac{n_0}{d_0} = \frac{G_x + g_{n1}}{B_1 (G_x + g_{n1}) + B_x (G_1 + g_{p4}) - B_{1x} g_{p1} - B_{x1} g_{n2}} \quad \ldots(3.8)$$

The figure of merit can be increased by minimizing the denominator of (3.8). The denominator is a function of the transistors' parasitic capacitors; hence the optimization process would involve techniques of minimizing these capacitances, such as appropriate sizing of the transistors. This process was not attempted as part of this thesis and has been left for future consideration. The results of the small signal characteristics are presented in Table 3.2, which includes the computation of the dominant pole using (3.7) and the FOM using (3.8). It is seen from the results that the dominant pole prediction gives an adequate estimate of the bandwidth.

Table 3.2 – AC characteristics of VCT grounded negative resistor

<table>
<tr><th>Resistance (KΩ)</th><th>Poles (rad / sec)</th><th>Zeros (rad / sec)</th><th colspan="2">BW (rad / sec)</th></tr>
<tr><td rowspan="2">-34.4</td><td>-8.95e9

8.15e8</td><td rowspan="2">-6.05e9</td><td>Measured</td><td>8.3e8</td></tr>
<tr><td>P_{DOM}</td><td>8.97e8</td></tr>
<tr><td colspan="5">FOM: 3e13</td></tr>
</table>

3.2 Grounded Negative Resistance Load

The frequency response expression has been evaluated as

$$R = \frac{sB_2 + G_2 + g_{p1} + g_{n1}}{s^2(B_1B_2 - B_{12}B_{21}) + s\begin{pmatrix} B_1(g_{p1} + g_{n1} + G_2) + B_2(G_1 + g_{p4}) \\ -B_{21}(g_{p2} + g_{n2}) - B_{12}g_{p3} \end{pmatrix} + \begin{pmatrix} (G_1 + g_{p4})(g_{p1} + g_{n1} + G_2) \\ -g_{p3}(g_{p2} + g_{n2}) \end{pmatrix}} \quad \ldots(3.9)$$

The AC equivalent model and nodal admittance matrix that were used to derive (3.9) can be found in the appendix. The value of the resistance at low frequency and the phase characteristics of the resistor can be determined as described by (3.4) and (3.5) respectively. Figure 3.3 presents the simulation result relating the magnitude and phase of the negative resistor as a function of frequency.

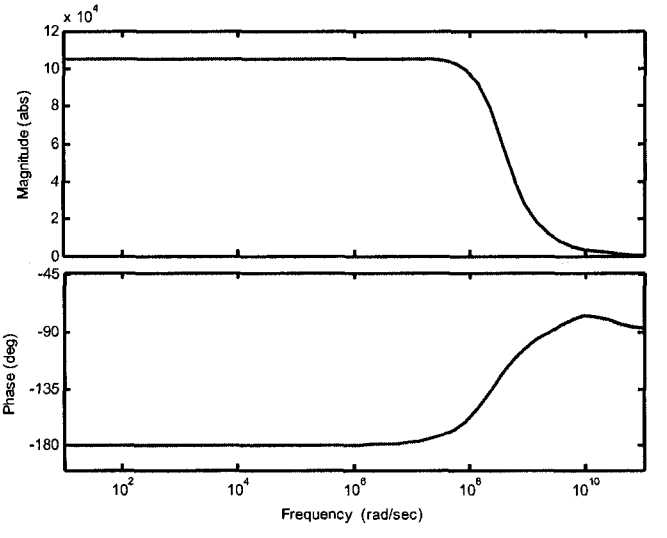


Figure 3.3 – Frequency simulation of grounded negative resistance load

The distribution of the poles and zeros, which have been located from (3.9), are presented in Table 3.3. The presence of a dominant pole is detected; therefore (3.6) can be used to estimate the bandwidth of the resistor. Using the dominant pole prediction described by (3.7), the expression for the figure of merit of this negative resistor is given by

$$FOM = \frac{G_2 + g_{p1} + g_{n1}}{B_1(G_2 + g_{p1} + g_{n1}) + B_2(G_1 + g_{p4}) - B_{21}(g_{p2} + g_{n2}) - B_{12}g_{p3}} \qquad \ldots(3.10)$$

The results of the small signal characteristics are presented in Table 3.3. This grounded negative resistor has a proportionate FOM value to the VCT grounded resistor. The similarity arises from the similar physical structure between the two active resistors, and was also evident for the large signal characteristics.

Table 3.3 – AC characteristics of grounded negative resistance load

Resistance (KΩ)	Poles (rad / sec)	Zeros (rad / sec)	BW (rad / sec)	
-105.16	-1.27e10 248e6	-7.82e9	Measured	2.71e8
			P_{DOM}	2.5e8
FOM: 2.7e13				

3.3 Current Conveyor Grounded Negative Resistor

The simplified expression for the frequency response of the grounded negative resistor circuit is given by

$$R = \frac{s^2 n_2 + s n_1 + n_0}{s^3 d_3 + s^2 d_2 + s d_1 + d_0} \qquad \ldots(3.11)$$

The details regarding the coefficients of the numerator and denominator in (3.11) can be found in the appendix. The value of the resistance at low frequency is determined as shown in the preceding sections. The phase characteristics of this negative resistor is given by

$$\theta = \tan^{-1}\left(\frac{\omega n_1}{n_0 - \omega^2 n_2}\right) - \tan^{-1}\left(\frac{\omega d_1 - \omega^3 d_3}{d_0 - \omega^2 d_2}\right) \qquad \ldots(3.12)$$

Figure 3.4 presents the simulation result relating the magnitude and phase of the negative resistor as a function of frequency.

The distribution of the poles and zeros for the resistor are presented in Table 3.4. This design lacks the presence of a dominant pole; hence (3.6) cannot be utilized for estimating the bandwidth. The dominant pole prediction that was employed in the preceding sections cannot be applied either; therefore an expression for the figure of merit has not been evaluated. The figure of merit has been calculated using the measured bandwidth.

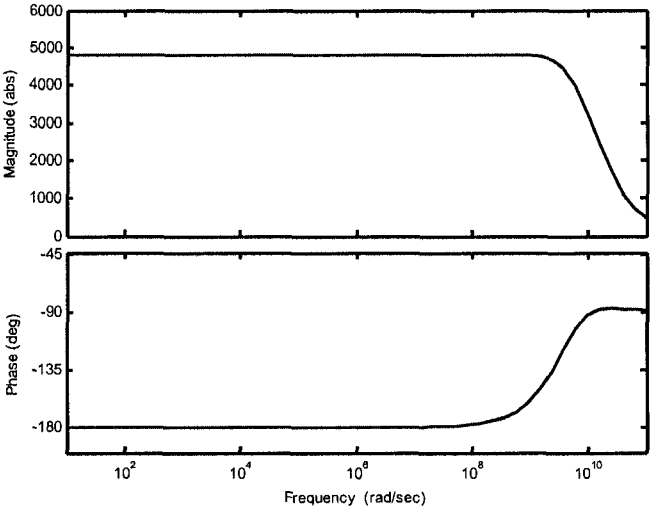


Figure 3.4 – Frequency simulation of CC grounded negative resistor

Table 3.4 – AC characteristics of CC grounded negative resistor

Resistance (KΩ)	Poles (rad / sec)	Zeros (rad / sec)	BW (rad / sec)
-4.81	-1.14e10 -0.51e10 0.41e10	-6.94e9 -3.67e9	8.92e9 (measured)
FOM: 4.29e13			

3.4 Floating Negative Resistance Load

The frequency response expression of the floating negative resistance load is given by

$$R = \frac{s(B_2 + B_{12} + B_1 + B_{21}) + G_2 + G_1 + g_{p5} + g_{p4} + g_{p2} + g_{p3}}{s^2(B_1B_2 - B_{12}B_{21}) + s\begin{pmatrix} B_1(G_2 + g_{p5}) - B_{21}g_{p4} \\ + B_2(G_1 + g_{p2}) - B_{12}g_{p3} \end{pmatrix} + \begin{pmatrix} (G_1 + g_{p2})(G_2 + g_{p5}) \\ - g_{p3}g_{p4} \end{pmatrix}} \quad \ldots(3.13)$$

Figure 3.5 presents the magnitude and phase of the negative resistor as a function of frequency.

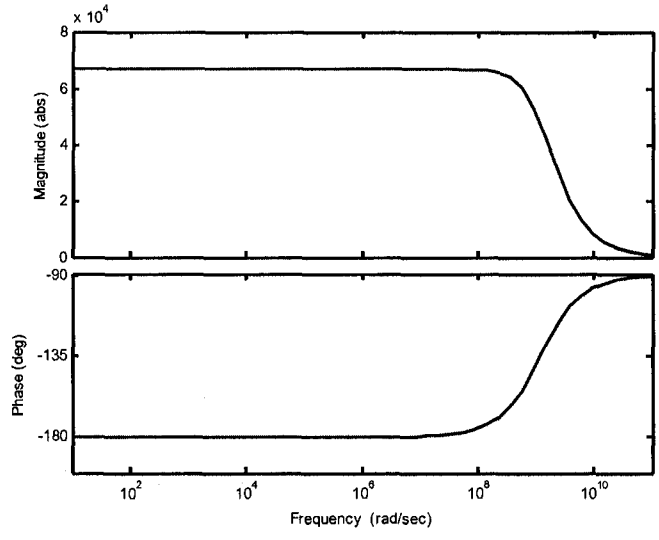


Figure 3.5 – Frequency simulation of floating negative resistance load

The distribution of the poles and zeros for the floating resistor are presented in Table 3.5. An interesting observation made is the appearance of a pole and a zero with equal value; hence there is a case of pole-zero cancellation. As a result, the bandwidth of the resistor is solely dependent on the single pole (which is the smaller of the two poles). The figure of merit of the floating resistor is calculated using the value of this pole, with the results presented in Table 3.5.

Table 3.5 – AC characteristics of floating negative resistance load

Resistance (KΩ)	Poles (rad / sec)	Zeros (rad / sec)	BW (rad / sec)
-66.86	-9.17e9 1.19e9	-9.17e9	1.19e9 (measured)
FOM: 8e13			

3.5 Current Mirror Floating Negative Resistor

The frequency response expression is given by

$$R = \frac{s(B_2 + B_{12} + B_1 + B_{21}) + G_2 + G_1 + g_{n5} + g_{n4} + g_{n2} + g_{n3}}{s^2(B_1B_2 - B_{12}B_{21}) + s\begin{pmatrix} B_1(G_2 + g_{n5}) - B_{21}g_{n4} \\ + B_2(G_1 + g_{n2}) - B_{12}g_{n3} \end{pmatrix} + \begin{pmatrix} (G_1 + g_{n2})(G_2 + g_{n5}) \\ - g_{n3}g_{n4} \end{pmatrix}} \quad \ldots(3.14)$$

The simulation result of the floating resistor is presented in Figure 3.6, with the distribution of the poles and zeros presented in Table 3.6.

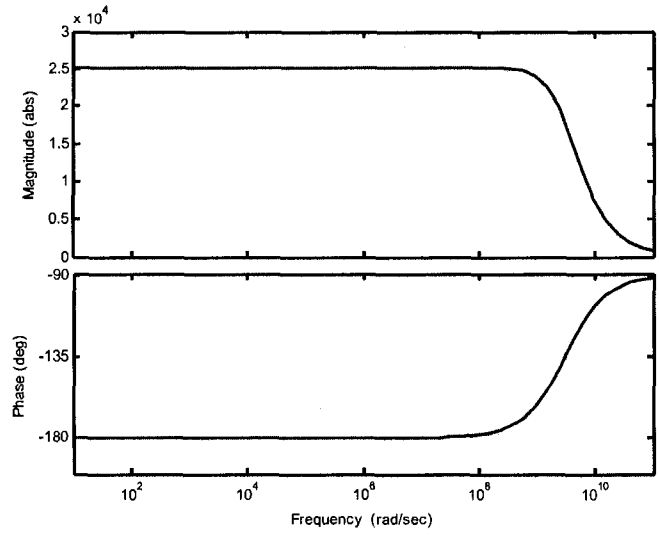


Figure 3.6 – Frequency simulation of current mirror floating negative resistor

As in the case of the floating negative resistance load of section 2.5, there is a case of pole-zero cancellation, and the bandwidth is dependent on the single pole, which is used for the computation of the figure of merit.

Table 3.6 – AC characteristics of current mirror floating negative resistor

Resistance (KΩ)	Poles (rad / sec)	Zeros (rad / sec)	BW (rad / sec)
-25.19	-7.69e9 3e9	-7.69e9	3e9 (measured)
FOM: 7.56e13			

3.6 Floating Negative Conductance Network

The frequency response expression is given by

$$R = \frac{s(B_2 + B_{12} + B_1 + B_{21}) + G_2 + G_1 + g_{p1} + g_{n4} + g_{n8} + g_{p5}}{s^2(B_1B_2 - B_{12}B_{21}) + s\begin{pmatrix} B_1(G_2 + g_{p5}) - B_{21}g_{n4} \\ + B_2(G_1 + g_{p1}) - B_{12}g_{n8} \end{pmatrix} + \begin{pmatrix} (G_1 + g_{p1})(G_2 + g_{p5}) \\ - g_{n4}g_{n8} \end{pmatrix}} \quad \ldots(3.15)$$

The simulation result and the distribution of the poles and zeros are presented in Figure 3.7 and Table 3.7 respectively.

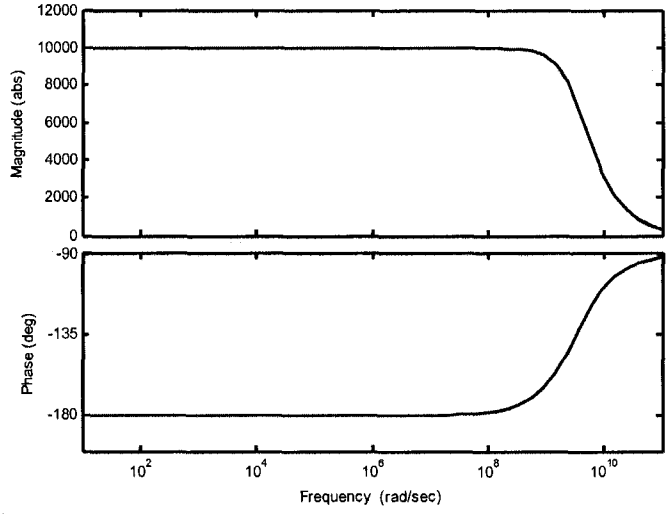


Figure 3.7 – Frequency simulation of floating NCN

Table 3.7 – AC characteristics floating NCN

Resistance (KΩ)	Poles (rad / sec)	Zeros (rad / sec)	BW (rad / sec)
-10	-6.39e9 3.31e9	-6.39e9	3.31e9 (measured)
Figure of Merit: 3.31e13			

3.7 Bandwidth Investigation

Active resistors in CMOS technology are often designed by converting a transconductance device to a driving point impedance. All of the negative resistance circuits that were studied have been designed using this technique. In this section my endeavor is to examine the effect on the bandwidth when such a transconductance device is transformed to an active resistor. We will first analyze a simple case; thereafter try to relate the result to the negative resistance circuits that are reported in this thesis.

3.7.1 CMOS Inverter

The transistor level schematic of a CMOS inverter is presented in Figure 3.8(a). The inverter is formed with a pair of complimentary transistors, and could be employed as a transconductance amplifier with the input voltage applied at the gates of the transistors and the output current measured at the drains. The inverter is analyzed for its bandwidth by locating the poles and zeros, after which it will be transformed to an active

resistor as shown in Figure 3.8(b). The effect on the values of the poles and zeros caused by this transformation will be observed.

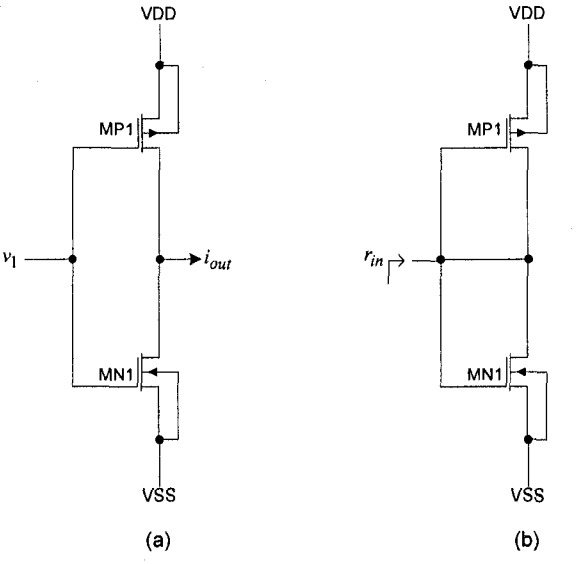


Figure 3.8 – CMOS inverter (a) Transconductor (b) Resistor

The small signal transconductance of the inverter shown in Figure 3.8(a) has been evaluated as

$$g_m = \frac{i_o}{v_1} = sB_{01} + g_{p1} + g_{n1} \qquad \ldots(3.16)$$

The AC equivalent model and the nodal admittance matrix describing the details of (3.16) can be found in the appendix. The transconductor has a single zero which determines the bandwidth of the system, with the simulation results for a design in 0.5 micron CMOS process presented in Table 3.8.

Shorting the input and output terminals together, in order to form the active resistor, prompts the addition of the elements in the corresponding rows and columns of the admittance matrix. This results in the expression for the resistance given as

$$r_{in} = \frac{v_1}{i_1} = \frac{1}{s(B_1 + B_o + B_{1o} + B_{o1}) + G_1 + G_o + g_{n1} + g_{p1}} \qquad \ldots(3.17)$$

The system now has a single pole and no zeros, with the simulation results summarized in Table 3.8.

Table 3.8 – Pole-zero analysis of CMOS inverter

	Expression	Zeros (rad/s)	Poles (rad/s)	Bandwidth (rad/s)
Transconductor	$-s1.6e-15+2.1e-4$	1.34e11	-	1.34e11
Resistor	$\frac{1}{s3e-14+2.4e-4}$	-	-7.3e9	7.3e9

The results of Table 3.8 show that there is a significant decrease in the bandwidth of the resistor when compared to that of the transconductor. Addition of the matrix elements causes the real and imaginary parts of the complex expression to become larger, translating to smaller pole and zero values; hence a lower bandwidth.

3.7.2 Voltage-to-Current Transducer [7]

The differential in single ended out voltage to current transducer was introduced in Chapter 1. For this experiment a slightly modified version which has a single current mirror load as opposed to two current mirrors is used, with the schematic presented in Figure 3.9. This VCT configuration was used for the design of the grounded negative resistor of Section 2.1.

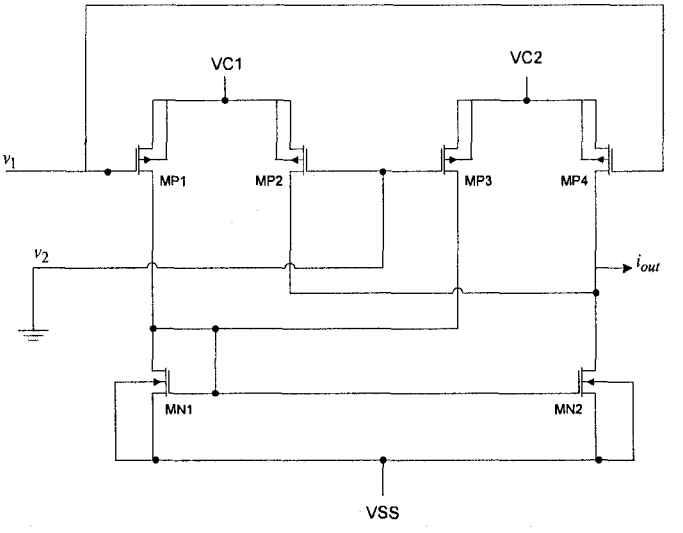


Figure 3.9 – DISO VCT with single current mirror load

The expression for the small signal transconductance of the VCT and the pole-zero distribution is presented in Table 3.9. The AC equivalent model and nodal admittance matrix used to evaluate this expression can be found in the appendix. When the input and output terminals are shorted together, each of the elements in the corresponding row and column of the admittance matrix are added together, and the complex expression will have larger real and imaginary parts. This leads to the poles and

zeros located at lower frequencies, resulting in a system with a smaller bandwidth. This reduction in the bandwidth is validated from the simulation results of Figure 3.10, where it is seen that the bandwidth of the resistor is a lot smaller. A summary of these results are presented in Table 3.9.

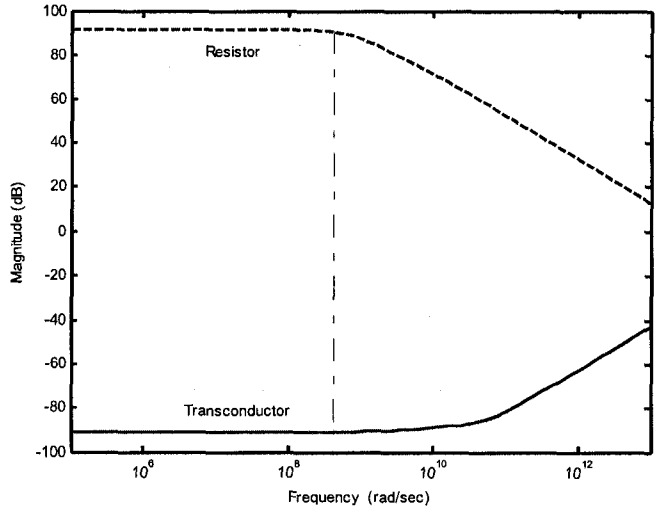


Figure 3.10 – Bandwidth of VCT: transconductor vs. resistor

In the above discussion we have come to recognize that we encounter a decrease in the bandwidth of a system when a transconductor is transformed to an active resistor. We can conclude that the decrease in bandwidth is a direct result of the parasitic capacitances at the input and output terminals adding up. The pole of the negative resistor will be located at the pole frequency of the transconductor loaded with an identical transconductance element. Therefore, for the design of a large bandwidth active resistor, it is recommended to use a high bandwidth transconductance amplifier.

Table 3.9 – Pole-zero analysis of VCT

	Expression	Zeros (rad/s)	Poles (rad/s)	Bandwidth (rad/s)
Transconductor	$\frac{-s^2\,1.8e-29+s\,1e-18-4.5e-9}{s\,2.4e-14\ +\ 1.5e-4}$	5.2e10 4.8e9	-6.4e9	2.28e10
Resistor	$\frac{s\,2.4e-14\ +\ 1.5e-4}{s^2\,5.7e-28\ +\ s\,4.8e-18\ -\ 4e-9}$	-6.4e9	7.8e8 -9.1e9	7.76e8

3.8 Stability

The stability of the negative resistance circuits in examined in this section. The location of the poles on the s-plane is used as the primary factor in predicting the stability. All the negative resistance circuits that have been investigated have an expression for the resistance as a function of frequency of the form

$$R=\frac{a_n s^n + a_{n-1}s^{n-1} .... + a_1 s + a_0}{d_n s^n + d_{n-1}s^{n-1} .... + d_1 s - d_0} \qquad ...(3.18)$$

According to the Hurwitz criteria, for a system to be stable it is mandatory that the denominator be a Hurwitz polynomial. A polynomial is said to be Hurwitzian if all the coefficients are positive, which translate to roots with real negative parts. The roots of the denominator represent the poles of the system; hence for stability it is required that the

real parts of the poles are negative and lie of the left hand side of the s-plane. This condition is described graphically in Figure 3.11.

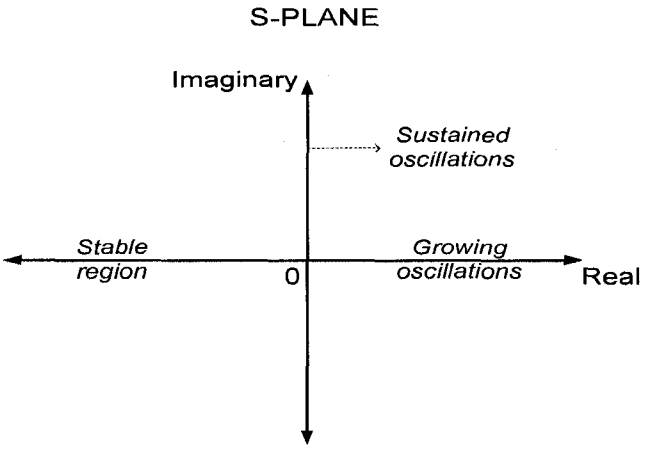


Figure 3.11 – S-plane describing pole location and stability

The negative coefficient in the denominator of (3.18) implies that one or more of the poles will have a positive real part, and lie on the right hand side of the s-plane. The negative coefficient is unwanted as it introduces potential instability; however it is what constrains the resistance to be negative at DC. Potential instability in the system can also be predicted from the positive slope phase response [16], which is evident from the simulations results of the resistors. The amount of lead angle can be related to the damping ratio of the negative resistance element and the attendant percent overshoot in response to a step signal input. The overshoot will provide an indication to the potential instability that a larger system may encounter when using the negative resistance as a sub-system. This knowledge can be used either (i) to ascertain stability of a system, or (ii) to achieve an oscillatory system.

The stability of an electronic circuit that accommodates a negative resistance of the form described by (3.18) is explored. A single pole negative resistor and a series RC circuit are used to perform this analysis. The negative resistor that is used is given by

$$R_N = \frac{R_{DC}\, p}{s - p} \qquad \ldots(3.19)$$

where p is the positive unstable pole, and R_{DC} is the magnitude of the resistance at low frequencies.

3.8.1 Parallel Connection

The circuit of Figure 3.12 is used to investigate a parallel connection of the negative resistor. The RC circuit represents a simple first order low pass filter.

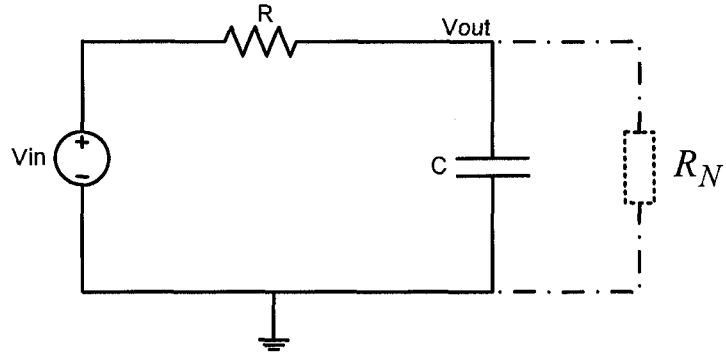


Figure 3.12 – RC Low pass filter with parallel negative resistor connection

The transfer function of the low pass filter (without the negative resistor) is given as

$$TF_1 = \frac{1}{s\,RC + 1} \qquad \ldots(3.20)$$

Equation (3.20) represents a stable system having a single pole with a negative real part. The negative resistor of (3.19) is added in parallel to the capacitive load as shown in Figure 3.20. The transfer function of the circuit is now given as

$$TF_2 = \frac{p\,R_{DC}}{s\,R\,C\,p\,R_{DC} + s\,R + p\,R_{DC} - p\,R} \qquad \ldots(3.21)$$

It is identified that the denominator (3.21) is a Hurwitz polynomial as long as the magnitude of R_{DC} is larger than resistor R of the RC circuit. As long as this condition is ascertained the system will remain stable. Table 3.10 summarizes the component values chosen for the design of a stable system. Figure 3.13 presents the simulation result with a step signal applied at the input. It is seen that the system has decaying oscillations, and eventually settles to a steady state, which indicates a stable system.

Table 3.10 – Design of LPF with parallel negative resistor connection

R (KΩ)	C (F)	R_N	TF
2	1f	$\frac{2.32e13}{s - 2.32e9}$	$\frac{2.32e13}{s^2\,46.4 + s\,2000 + 1.86e13}$

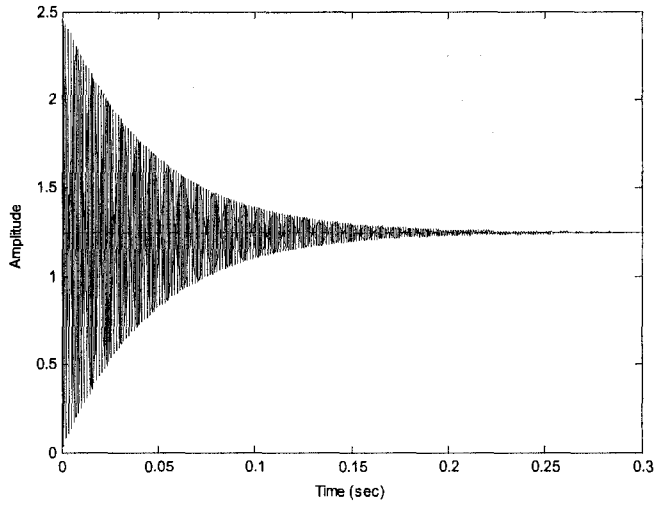


Figure 3.13 – Time domain simulation of LPF

The experiment was repeated for the high pass filter of Figure 3.14, with the negative resistor now being connected in parallel with the resistive load. The same component values of Table 3.10 are used.

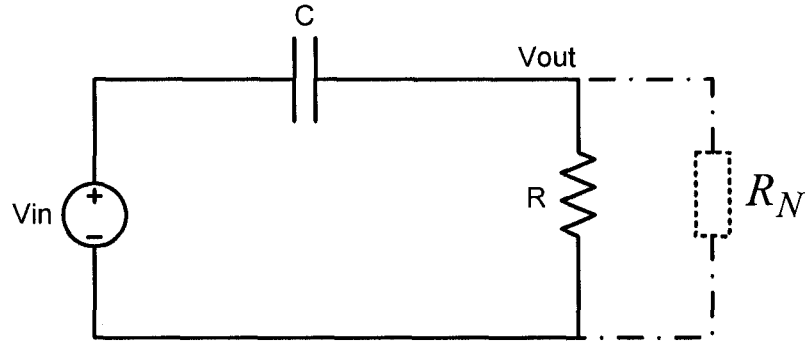


Figure 3.14 – RC high pass filter with parallel negative resistor connection

The transfer function of the high pass filter (with the negative resistor) is determined as

$$TF_3 = \frac{s\,C\,R\,p\,R_{DC}}{s\,R\,C\,p\,R_{DC} + s\,R + p\,R_{DC} - p\,R} \qquad \ldots(3.22)$$

The result of (3.22) reveals that the system will be Hurwitz stable as long as the magnitude of R_{DC} is larger than resistor R of the RC circuit. This result is identical to the one obtained for the low pass filter, where the negative resistor was connected in parallel to a capacitive load.

3.8.2 Series Connection

The RC circuit of Figure 3.15 is used for this analysis. The circuit represents a first order high pass filter.

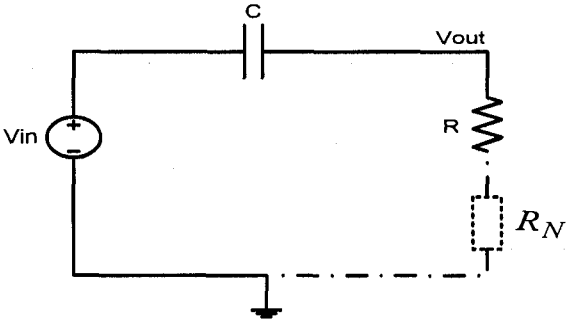


Figure 3.15 – RC high pass filter with series negative resistor connection

The transfer function of the high pass filter (without the negative resistor) is given by

$$TF_4 = \frac{s\,RC}{s\,RC + 1} \qquad \ldots(3.23)$$

Equation (3.23) represents a stable system having a pole-zero pair. Adding the negative resistor in series with the load as shown in Figure 3.15 gives a transfer function of

$$TF_5 = \frac{s^2 RC + s(C R_{DC}\, p - C R\, p)}{s^2 RC + s(1 + C R_{DC}\, p - C R\, p) - p} \qquad \ldots(3.24)$$

It is recognized from (3.24) that the denominator is not a Hurwitz polynomial, and the system will have at least one pole with a positive real part. The numerator is not Hurwitzian either, and there will also be a zero with a real positive part. It has been established that this pole and zero are located at frequencies that are very close together and cancel each other out. The results presented in Table 3.11 verify this realization.

Table 3.11 – Design of HPF with series negative resistor connection

R (KΩ)	C (Farads)	R_N	TF	Zeros (rad/s)	Poles (rad/s)
20	1n	$\frac{2.32e13}{s - 2.32e9}$	$\frac{s^2 2e-5 - s2.32e4}{s^2 2e-5 - s2.32e4 - 2.32e9}$	0 1.16e9	-1e5 1.16005e9

The results of the analysis in this section show that when a negative resistor is connected in parallel to a more complex system, it is possible to design the network to be Hurwitz stable by appropriate choice of components. For a series connection of the negative resistor, the presence of an unstable pole cannot be eliminated, and the circuit is likely to be unstable.

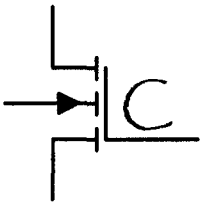
3.9 Summary

This chapter presented the small signal characteristics of the negative resistance circuits. The high frequency AC equivalent model was used to derive the frequency response expression for the resistors. The figure of merit, which was defined as the product of the bandwidth and the magnitude of the resistor, was calculated for each of negative resistors. For cases in which a dominant pole existed, an expression for the figure of merit was evaluated. The results of these are summarized in Table 3.12.

The effect on the bandwidth when a transconductance amplifier is used for the design of active resistors was explored in this chapter. It was concluded that a reduction in the bandwidth of the active resistor is encountered due to the parasitic capacitances at the input and output terminals of the transconductor adding up, causing the poles and zeros to be located at lower frequencies. To conclude the chapter, the locations of the poles on the s-plane were examined in order to analyze the stability of the negative resistance circuits.

Table 3.12 – Summary of small signal characteristics

Grounded Negative Resistors:			
	VCT [7]	Negative resistance load [6]	Current conveyor [13]
Resistance value	-34.4 KΩ	-105.16 KΩ	-4.81 KΩ
Bandwidth (rad/s)	8.3e9	2.71e8	8.92e9
FOM	3e13	2.7e13	4.29e13
Floating Negative Resistors:			
	Current mirror [8]	Negative resistance load [6]	NCN [14]
Resistance value	-25.19 KΩ	-66.86 KΩ	-10 KΩ
Bandwidth (rad/s)	3e9	1.18e9	3.31e9
FOM	7.56e13	8e13	3.31e13



Chapter Four

Applications

Numerous applications of negative resistance circuits in VLSI technology were discussed in chapter 1, with design of oscillators and voltage reference networks being mentioned. These applications demonstrated the significance of negative resistors in VLSI technology. In this chapter we illustrate some alternate applications, and design the system using some of the negative resistance circuits that have been investigated as part of this thesis.

4.1 Current Mode LC Oscillator

Current mode signal processing has become increasingly popular in the last decade. An oscillator with a current as the output is likely to be an important component in analog electronics. Figure 4.1 presents a current mode oscillator design in which an LC tank is driven by a transconductor [17]. For this design the VCT is used as the transconductance device.

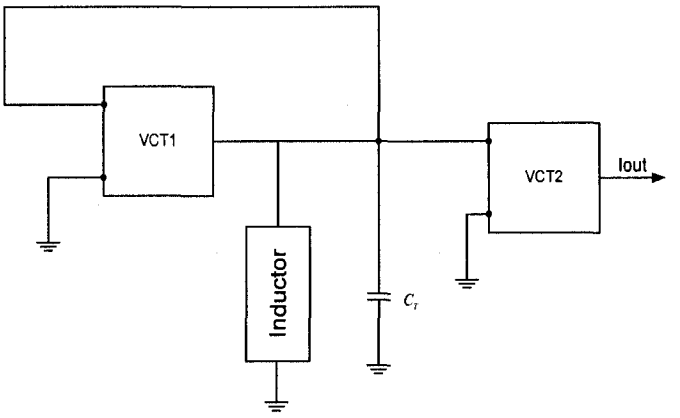


Figure 4.1 – Current mode oscillator design

The quality factor of an oscillator is a comparison between the frequency at which a system oscillates to the rate at which is dissipated its energy. The objective is to minimize the energy dissipated, therefore have a high quality factor oscillator design. For this particular design the quality factor of the oscillator is highly dependent on the quality factor of the LC tank circuit. The inductor that forms the LC tank generally has some parasitic resistance associated with it, which degrades the quality factor of the tank. Adding a negative resistor in parallel with the LC tank can cancel the effect of the parasitic resistance of the inductor, and enhance the characteristics of the system in which the tank is employed.

The inductor in Figure 4.1 is actively designed using a VCT configured gyrator loaded with a capacitor as shown in Figure 4.2. The effective impedance seen at the input terminal is given by [17]

$$Z_{in} = \frac{A + D + y_L}{(A + D + y_L)(A + \hat{y}_{11}) - (C + \hat{y}_{31})(B + \hat{y}_{13})} \qquad \ldots(4.1)$$

The details regarding coefficients of (4.1) can be found in the appendix. At low frequencies the impedance can be approximated as an ideal inductance of value [7]

$$Z_{in} \approx \frac{sC_L}{gm_1 gm_2} \qquad \ldots(4.2)$$

where g_m is the small signal transconductance of the respective VCT. Detailed analysis of (4.1) reveals that at low frequency Z_{in} represents an inductance of value given by (4.2) in series with a parasitic resistance which is a function of frequency. A design with 0.5 micron CMOS process produced an inductor of value 365 μH coupled with a series parasitic resistance of 1.092 KΩ. This resistance is constant for frequencies less than 50 KHz, after which it starts to increase.

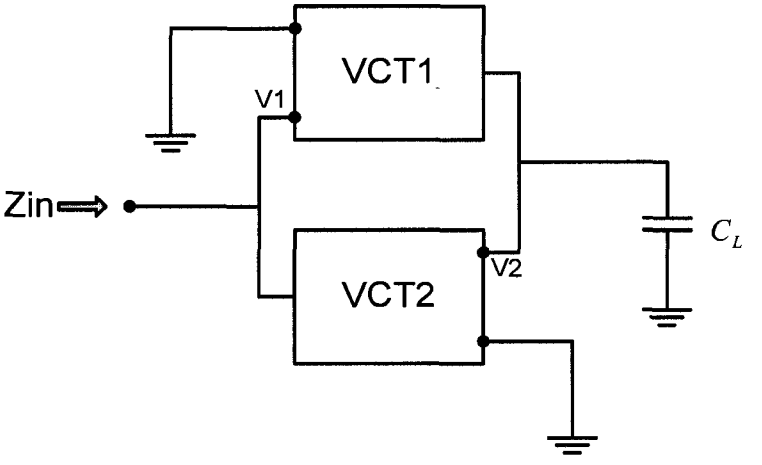


Figure 4.2 – Active inductor design

The quality factor of the LC tank is the ratio of resonant frequency to the bandwidth of resonance, described graphically in Figure 4.3. Adding a negative resistance in parallel with LC tank influences these two parameters such that

$$\omega_{01} = \sqrt{\frac{1}{LC}} \rightarrow \omega_{02} = \sqrt{\frac{N+R}{LCN}} \qquad \ldots(4.3)$$

and

$$BW1 = \frac{R}{L} \rightarrow BW2 = \frac{R}{L} - \frac{1}{CN} \qquad \ldots(4.4)$$

where R represents the parasitic resistor and N represents the magnitude of the negative resistor. Inspection of (4.3) and (4.4) reveals that if the magnitude of the negative resistor N is a lot larger than that of the parasitic resistor R, there is no significant effect on the resonant frequency, will however reduce the bandwidth of the tank; leading to an increase in the quality factor.

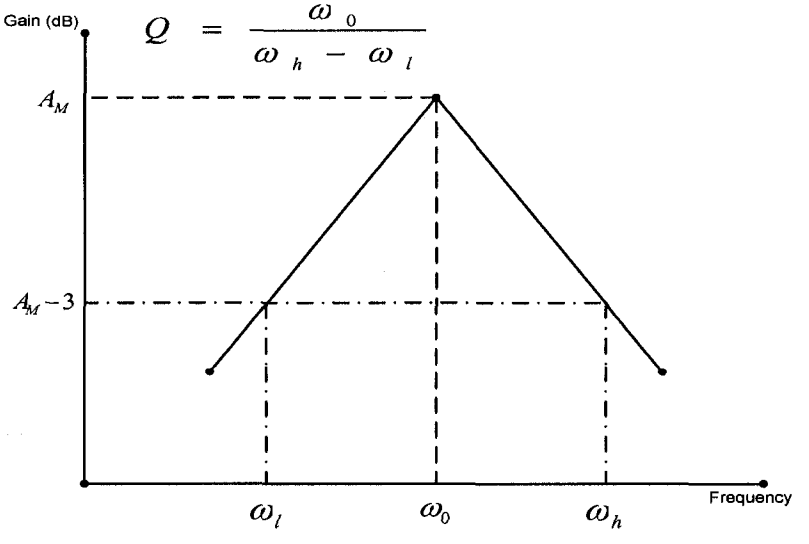


Figure 4.3 – Graphical interpretation of quality factor of an LC circuit

Using the above analysis, we propose to add a negative resistor of magnitude approximately 100 times larger than that of the parasitic resistor in parallel with the LC tank. Table 4.1 presents the simulation results of an LC tank formed using the active inductor, a 3.3 pF capacitor and an active negative resistance of value -105 KΩ. The grounded negative resistance load presented in Section 2.2 was used for this design.

Table 4.1 – Simulation results of LC tank resonator

	Resonant Frequency (Hz)	Bandwidth (Hz)	Quality Factor
Without negative R	4.4M	650K	7
With negative R = -105KΩ	4.4M	152K	29

The phase noise of an oscillator is described as the short term random frequency fluctuations of the output signal. An ideal oscillator would generate a pure sine wave, which in the frequency domain is depicted by a single line at the frequency of oscillation, i.e. all the signal's power is at a single frequency. The increasing demand for high resolution wireless communication has stressed the importance on design of low phase noise oscillators. The quality factor of the resonator, in this case being the LC tank circuit, is one of the significant sources that generate phase noise in the output of an oscillator. This application demonstrates how a negative resistance circuit has been used to improve the quality factor of a resonator; hence permit the design of a low phase noise current mode oscillator.

The stability of the LC tank circuit which accommodates the unstable negative resistor is analyzed. The expression of the resistance in pole-zero form is given as

$$R_N = \frac{R_{DC}\, p_1 p_2 (s + z_1)}{z_1 (s + p_1)(s - p_2)} \qquad \ldots(4.5)$$

where p_2 represents the unstable pole. The expression for the impedance of the LCR circuit given by

$$Z_{LCR} = \frac{Z_{DC}\ (s + z_2)}{z_2 (s^2 x_2 + s x_1 + x_0)} \qquad \ldots(4.6)$$

When the two impedances are combined in parallel the final expression is given as

$$Z = \frac{R_{DC}\, Z_{DC}\, (s+z_2)(s+z_1)}{R_{DC}\, p_1 p_2 z_2 (s+z_1)(s^2 x_2 + s x_1 + x_0) + Z_{DC}\, z_1 (s+z_2)(s+p_1)(s-p_2)} \qquad \ldots(4.7)$$

Simplifying (4.7) reveals that the denominator will be Hurwitzian as long as R_{DC} is greater than Z_{DC}. As long as this condition is guaranteed, the inclusion of a negative resistance will not introduce instability into the design of the LC tank circuit. Only the quality factor of the circuit will be changed in the desired direction to improve the selectivity. The final expression describing the LC tank circuit designed with the above mentioned component values and negative resistor is given by

$$Z = \frac{s^2 1.4e-17 + 1.1e-7 + 0.33}{s^3 4.8e-29 + s^2 3.8e-19 + 1.1e-13 + 3e-4} \qquad \ldots(4.8)$$

It is seen that the denominator of (4.7) is a Hurwitz polynomial representing a stable system.

4.2 Sine Wave Oscillator Using Low Pass Filter Structure

An electronic filter is a circuit that performs signal processing functions, specifically intended to remove unwanted signal components and enhance wanted ones. There are various known strategies of designing electronic filters, one of the most common being an active RC circuit. The term active implies the use of an active component such as a voltage amplifier. Figure 4.4 presents the schematic of an active RC single amplifier biquad low pass filter [18]. Because there is multiple feedback, this topology is known as a multiple feedback low pass filter. The term biquad suggests a filter with a second order transfer function.

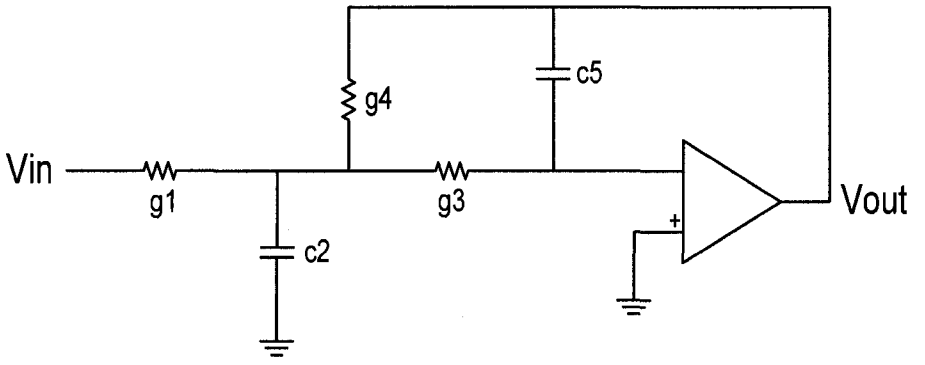


Figure 4.4 – Active RC low pass filter network

The transfer function of the low pass filter is given as

$$\frac{Vout}{Vin} = \frac{-g_1 g_3}{s^2 C_2 C_5 + sC_5(g_1 + g_3 + g_4) + g_3 g_4} \qquad \ldots(4.9)$$

The poles of the filter have a real and an imaginary part and will be of the form $\partial \pm j\sigma$. In order to ensure a stable frequency selective filter it is mandatory that the real parts of the poles be negative; hence lie on the left hand side of the s-plane. Upon examining the transfer function given in (4.9), we propose that a negative resistor could be used to shift the real part of the poles to a region that will make the system unstable. This will result in the system oscillating, and could be employed as a sine wave oscillator.

If the co-efficient of 's' in the denominator of (4.9) is made zero, the poles of the system become purely imaginary; i.e. have zero real part and lie on the imaginary axis of the s-plane. This can be achieved by solving the following equality

$$C_5(g_1 + g_3 + g_4) = 0 \qquad \ldots(4.10)$$

This condition introduces instability and the system will encounter sustained oscillations. If the real parts of the poles are located on right hand side of the s-plane, the system will incur growing oscillations until a steady state is reached.

The network component values for a low pass filter design having a pole frequency of 1000 Hz, a quality factor of 0.707 and unity gain are presented in Table 4.2. This design gives a network transfer function of

$$\frac{Vout}{Vin} = \frac{-2.5e-9}{s^2\,6.34e-17 + s5.63e-13 + 2.5e-9} \qquad \ldots(4.11)$$

Figure 4.5a shows the time domain response of the filter with a sine wave input of unity amplitude.

Table 4.2 – Active RC LFP design

R1 (KΩ)	C2 (F)	R3 (KΩ)	R4 (KΩ)	C5 (F)
20	16.9n	20	20	3.75n
Gain = 1, Q = 0.707, $\omega_0 = 1000\ Hz$				

It is seen from (4.10) that one way of making the 's' coefficient of the denominator zero is by making R1 = -10 KΩ. Adjusting R1 as opposed to R3 or R4 ensures that there is no alteration in the pole frequency of the filter. This adjustment results in a network transfer function of

$$\frac{Vout}{Vin} = \frac{-5e-9}{s^2\,6.4e-17+2.5e-9} \qquad \ldots(4.12)$$

Figure 4.5b presents the simulation result of the system described by (4.12) for a sine wave input of unity amplitude. It is evident that the system is unstable and oscillates.

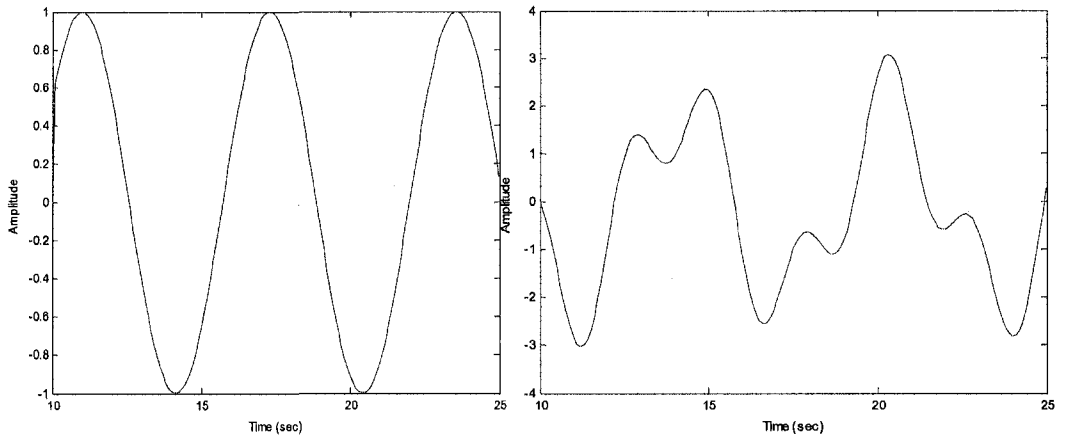


Figure 4.5 – Time domain simulation of active RC LPF for a) R = 20K and b) R = -10K Ohms

The oscillator is designed in a 0.5 micron CMOS process with an amplifier whose characteristics are described in Table 4.3. The negative resistor R1 was designed using the grounded negative resistance load presented in Section 2.2. The output of the oscillator with zero input is presented in Figure 4.6. The frequency of oscillation was measured at 1000 Hz, which is the pole frequency of the original low pass filter. The amplitude of oscillation was measured at 2.42 μV.

Table 4.3 – Op Amp characteristics

Parameter	Value	unit
Gain (open loop)	101	dB
Bandwidth (3db freq)	226	Hz
Phase margin	113	degrees
Unity Bandwidth	29	MHz
Output resistance	149	Ω
Input resistance	5E11	Ω

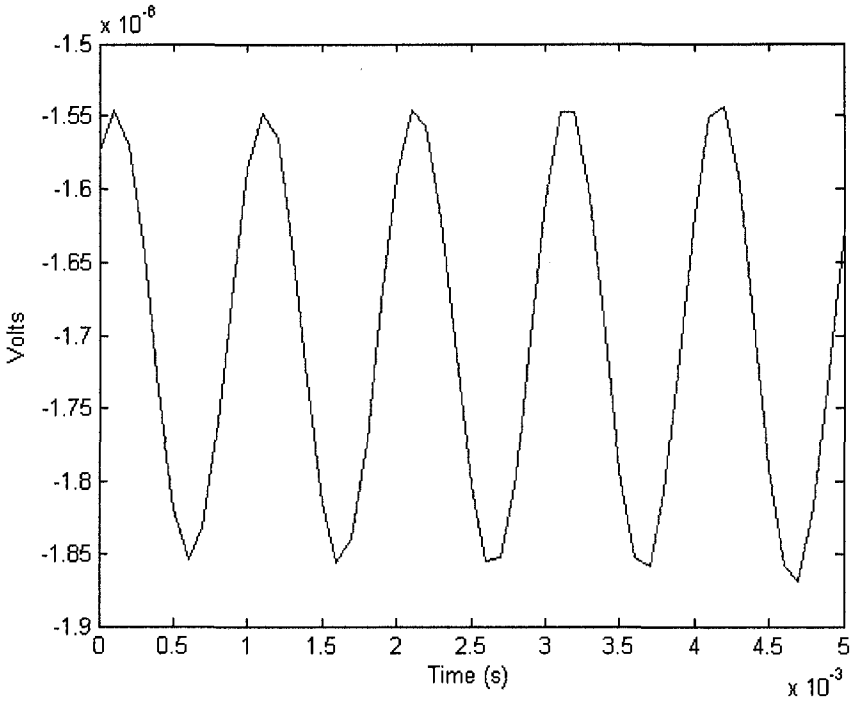


Figure 4.6 – Output of oscillator designed with LPF

The value resistor R1 is modified such that the poles of the system enter the right hand side of the s-plane. Making R1 = -9 KΩ gives a network transfer function of

$$\frac{Vout}{Vin} = \frac{-5.6e-9}{s^2 1e-14 + s(-2.8e-14) + 2.5e-9} \qquad \ldots(4.13)$$

Simulation results showed that for zero input the system produces growing oscillations at the output, and eventually settles to produce a uniform sine wave of amplitude 1.5 volts.

4.3 Inverting Feedback Amplifier [19]

Applying feedback to amplifiers has become a very common technique for stabilizing and improving the amplifiers operating characteristics. A universal structure used is the inverting feedback amplifier shown in Figure 4.7. The amplifier that is used generally has non ideal characteristics, most notably finite input and output impedance. As mentioned in earlier chapters, this affects the characteristics of the system in which the amplifier is employed. In this section we intend to illustrate how a negative resistance circuit could be used to extend the bandwidth of the inverting amplifier.

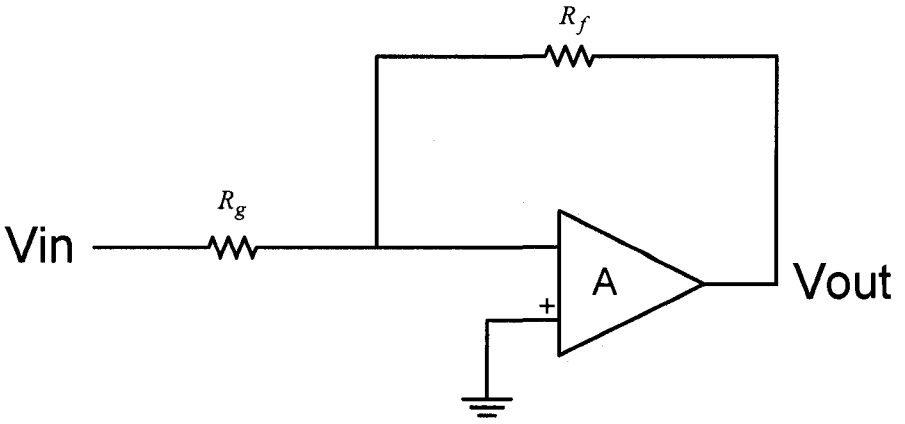


Figure 4.7 – Inverting feedback amplifier

The closed loop transfer function of the inverting amplifier of Figure 4.7 is given as [19]

$$\frac{V_o}{V_i} = -\frac{R_f}{R_g}\frac{A_0\omega_0}{s\,R_f(Y_f + Y_g + Y_i) + A_0\omega_0 + R_f(Y_f + Y_g + Y_i)\omega_0} \quad \ldots(4.14)$$

The one-pole model of an op-amp was used to derive (4.14). The one-pole model is given as

$$A(j\omega) = \frac{A_0\ \omega_0}{s + \omega_0} \qquad \ldots(4.15)$$

The amplifier whose characteristics were presented in Table 4.3 was used for this design, with the open loop gain $A_0 = 116$ KV/V, $Z_i = \frac{1}{Y_i} = 5e11\ \Omega$ and $\omega_0 = 226$ Hz. The output impedance of the op-amp was ignored. Equation (4.14) represents the transfer function of a single pole system, with the value of this pole determining the bandwidth. Adding a grounded negative resistor at the inverting input terminal of the negative feedback amplifier will reduce the effect of the op-amp input impedance and increase the bandwidth. This effect can be seen analytically from (4.14). Adding a negative resistor at the input terminal, such that $Y_i = Y_i - Y_N$, results in the denominator having smaller coefficients. This leads to the pole having a larger magnitude, therefore an increase in the bandwidth. This theory was proved in Section 3.7 where the effect on the bandwidth when a transconductor is transformed to an active resistor was examined.

Figure 4.8 presents the simulation result of the feedback amplifier (for $R_f = 10$ KΩ and $R_g = 1$ KΩ) with and without a negative resistor. The current conveyor designed grounded negative resistor (presented in Section 2.3) of value -1.3 KΩ was used for this design.

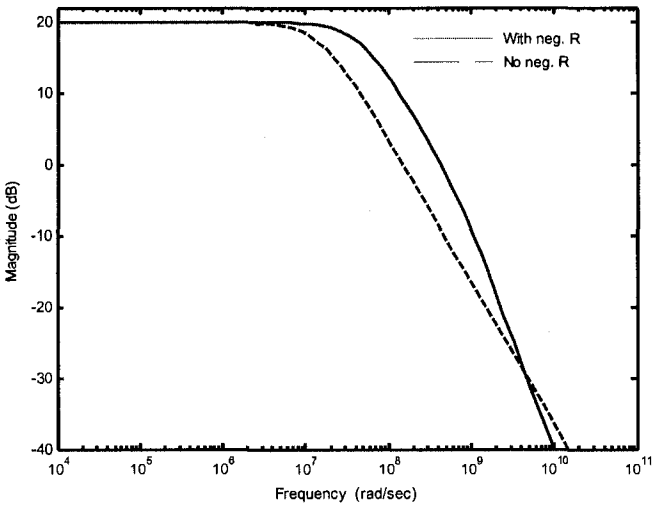


Figure 4.8 – Simulation results of inverting feedback amplifier

The simulation result of Figure 4.8 exhibits how the use of a negative resistance could minimize the effects of the finite input impedance of an op-amp, and hence extend the bandwidth of an inverting feedback amplifier. An increase in the bandwidth of the system from 2M Hz to 8M Hz has been achieved in the above.

The stability of the inverting feedback amplifier design is investigated. The current conveyor designed grounded negative resistor was used for this design, which is a three pole system given as an admittance by

$$Y_N = \frac{z_1 z_2 (s + p_1)(s + p_2)(s - p_3)}{R_{DC}\, p_1 p_2 p_3 (s + z_1)(s + z_2)} \quad \ldots(4.16)$$

Adding the admittance of (4.16) to $Y = Y_i + Y_f + Y_g$ (as required for the transfer function of (4.14)) results in an impedance of

$$Z = \frac{R_{DC}\ p_1 p_2 p_3\ (s + z_1)(s + z_2)}{YR_{DC}\ p_1 p_2 p_3\ (s + z_1)(s + z_2) + z_1 z_2\ (s + p_1)(s + p_2)(s - p_3)} \quad \ldots(4.17)$$

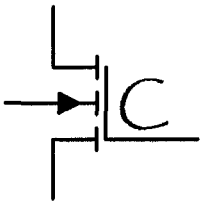
Expanding (4.17) reveals that the active impedance will be Hurwitz stable if $R_{DC} > R_i \| R_f \| R_g$. As long as this inequality is satisfied the inclusion of the negative resistor will not introduce instability into the inverting amplifier design. The final transfer function of the inverting amplifier designed with the above mentioned component values and negative resistor is given by

$$\frac{V_o}{V_i} = \frac{s^4 4.9e-44 + s^3 1e-33 + s^2 7.9e-24 + s 2.6e-14 + 3.2e-5}{s^6 2.7e-62 + s^5 9.3e-52 + s^4 1e-41 + s^3 5.3e-32 + s^2 1.1e-22 + s 7.5e-14 + 3.2e-6} \quad \ldots(4.18)$$

It is seen that the denominator of (4.18) is a Hurwitz polynomial and represents a stable system.

4.4 Summary

In this chapter we have successfully demonstrated three applications in which negative resistance circuits have been applied. Design, analysis and simulation results have been presented justifying further the importance of negative resistance circuits in VLSI technology. The stability of the system that accommodated the negative resistor was analyzed, and the required condition for stability was determined.



Chapter Five

Conclusions

A detailed characterization of CMOS negative resistance circuits has been presented in this thesis. Large signal characteristics that were investigated included resistance range, linearity, noise and power consumption. A comparison between each of the resistors was presented, enabling designers to pick a particular resistor for an application where a specific characteristic holds more importance over another.

A study of the small signal characteristics included a detailed investigation into the bandwidth of the negative resistance circuits. All of the resistors that were studied in this thesis were designed using a transconductance amplifier, which is a popular approach used in VLSI technology. It was determined that this design method has a negative effect on the bandwidth of the active resistor, which is a result of the parasitic capacitors at the input and output terminals of the transconductance device adding up.

Important stability issues regarding negative resistance circuits were revealed, where the presence of a positive unstable pole was detected. Analysis on how to overcome the instability when the negative resistor is employed in larger electronic systems was presented. To conclude the thesis, design examples where negative resistance circuits were used to improve the performance of larger electronic systems

were presented. The Q-factor enhancement of an LC tank circuit used for the design of a current mode oscillator and bandwidth extension of an inverting feedback amplifier were discussed and analyzed.

5.1 Future work

- The negative resistances could be fabricated and tested for its characteristics in the lab.
- The noise of the negative resistors could be examined further in an attempt to design a low noise system.
- The figure of merit expression, in the presence of a dominant pole, could be optimized
- The stability of more complex connections of the negative resistors could be examined
- Alternate structures for the design of negative resistance circuits could be investigated

5.2 Publications

The work and results of this thesis have contributed to the following publications:

R. Raut, Vishal Patel, "A Study on CMOS Negative Resistance Circuit", (Accepted), IEEE Canada, 21st Canadian Conference on Electrical and Computer Engineering, Niagara Falls, Ontario, May 2008

Appendix

A Grounded Negative Resistance Load

The AC equivalent model and nodal admittance matrix used to evaluate the frequency response expression of (3.9) are presented below.

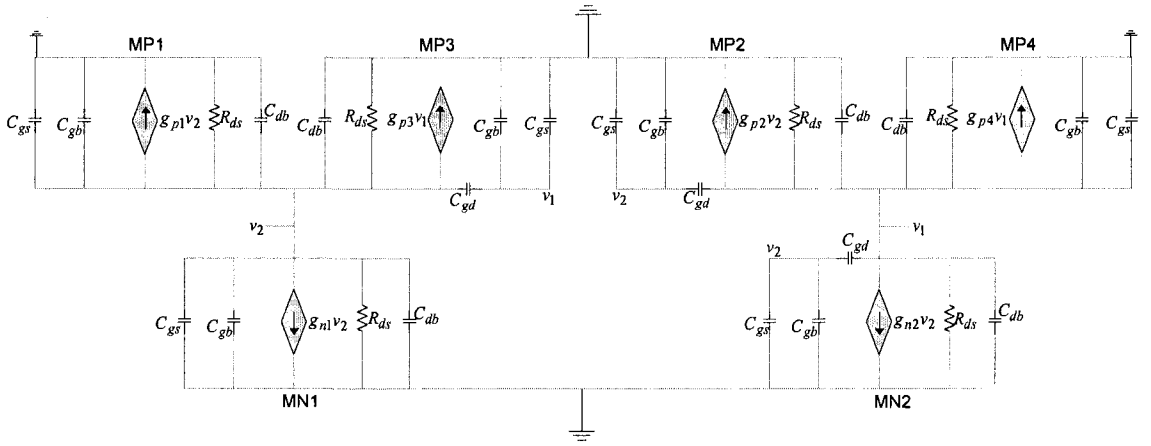


Figure A.1 – AC equivalent model of grounded negative resistance load

$$\begin{bmatrix} sB_1 + G_1 & sB_{12} \\ sB_{21} & sB_2 + G_2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} i_1 - g_{p4}v_1 - g_{n2}v_2 \\ -g_{p3}v_1 - g_{p1}v_2 - g_{n1}v_2 \end{bmatrix} \quad \ldots(A.1)$$

The details regarding the elements of (A.1) are given in Table A.1.

Table A.1 – Details describing the admittance matrix elements of (A.1)

$$B_1 = C_{gsp\,4} + C_{gbp\,4} + C_{dbp\,4} + C_{gdp\,2} + C_{dbp\,2} + C_{dbn\,2} + C_{gdn\,2} + C_{gsp\,3} + C_{gdp\,3} + C_{gbp\,3}$$

$$B_2 = C_{dbp\,1} + C_{gsp\,1} + C_{gbp\,1} + C_{gsn\,1} + C_{gbn\,1} + C_{dbn\,1} + C_{gdp\,3} + C_{dbp\,3} + C_{gsp\,2} + C_{gbp\,2} + C_{gdp\,2} + C_{gsn\,2} + C_{gbn\,2} + C_{gdn\,2}$$

$$B_{12} = B_{21} = -C_{gdp\,3} - C_{gdp\,2} - C_{gdn\,2};\ G_1 = g_{dp\,2} + g_{dp\,4} + g_{dn\,2};\ G_2 = g_{dp\,1} + g_{dp\,3} + g_{dn\,1}$$

B Current Conveyor Grounded Negative Resistor

The AC equivalent model and nodal admittance matrix used to derive the frequency response expression of (3.11) are presented below.

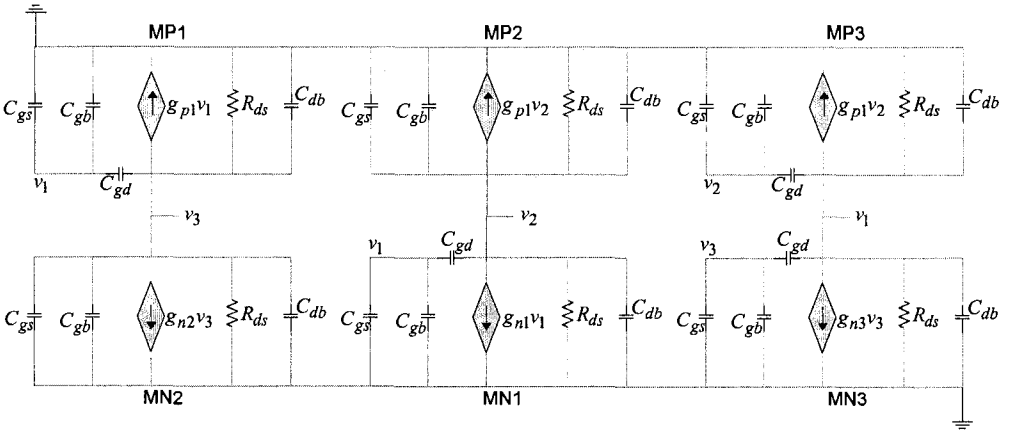


Figure B.1 – AC equivalent model of CC grounded negative resistor

$$\begin{bmatrix} sB_1 + G_1 & sB_{12} & sB_{13} \\ sB_{21} & sB_2 + G_2 & 0 \\ sB_{31} & 0 & sB_3 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} i_1 - g_{p3}v_2 - g_{n3}v_3 \\ -g_{n1}v_1 - g_{p2}v_2 \\ -g_{p1}v_1 - g_{n2}v_3 \end{bmatrix} \quad \ldots(B.1)$$

The details regarding (3.11) and (B.1) are given in Table B.1.

Table B.1 – Details describing the elements of (3.11) and (B.1)

$$n_2 = B_2 B_3;\ n_1 = B_2(G_3 + g_{n2}) + B_3(G_2 + g_{p2});\ n_0 = (G_2 + g_{p2})(G_3 + g_{n2})$$

$$d_3 = B_1 B_2 B_3 - B_{12} B_{21} B_3 - B_{13} B_{31} B_2;\ d_2 = B_1 B_2 (G_3 + g_{n2}) + B_1 B_3 (G_2 + g_{p2}) + G_1 B_2 B_3 - B_{21} B_{12} (G_3 + g_{n2}) - B_{21} g_{p3} B_3 - g_{n1} B_{12} B_3 - B_{31} B_{13} (G_2 + g_{p2}) - B_{31} g_{n3} B_2 - g_{p1} B_{13} B_2;$$

$$d_1 = B_1(G_2 + g_{p2})(G_3 + g_{n2}) + G_1 B_2 (G_3 + g_{n2}) + G_1 B_3 (G_2 + g_{p2}) - B_{21} g_{p3} (G_3 + g_{n2}) - g_{n1} B_{12} (G_3 + g_{n2}) - g_{n1} g_{p3} B_3 - B_{31} g_{n3} (G_2 + g_{p2}) - g_{p1} B_{13} (G_2 + g_{p2}) - g_{p1} g_{n3} B_2;$$

$$d_0 = G_1(G_2 + g_{p2})(G_3 + g_{n2}) - g_{n1} g_{p3} (G_3 + g_{n2}) - g_{p1} g_{n3} (G_2 + g_{p2})$$

$$B_1 = C_{gsp\,1} + C_{gbp\,1} + C_{gdp\,1} + C_{gsn\,1} + C_{gbn\,1} + C_{gdn\,1} + C_{gdp\,3} + C_{dbp\,3} + C_{gdn\,3} + C_{dbn\,3}$$

$$B_2 = C_{gsp\,2} + C_{gbp\,2} + C_{dbp\,2} + C_{gdn\,1} + C_{dbn\,1} + C_{gsp\,3} + C_{gbp\,3} + C_{dgp\,3}$$

$$B_3 = C_{gdp\,1} + C_{dbp\,1} + C_{dbn\,2} + C_{gbn\,2} + C_{gsn\,2} + C_{gsn\,3} + C_{gbn\,3} + C_{gdn\,3}$$

$$B_{12} = B_{21} = -C_{gdn\,1} - C_{gdp\,3};\ B_{13} = B_{31} - C_{gdp\,1} - C_{gdn\,3}$$

$$G_1 = g_{dp\,3} + g_{dn\,3};\ G_2 = g_{dp\,2} + g_{dn\,1};\ G_3 = g_{dp\,1} + g_{dn\,2}$$

C Floating Negative Resistance Load

The AC equivalent model and nodal admittance matrix used to derive (3.13) are presented below.

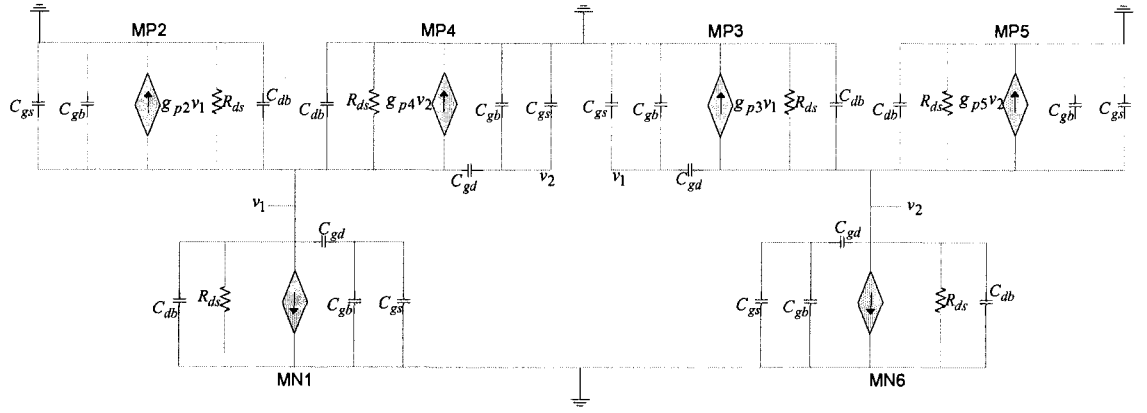


Figure C.1 – AC equivalent model of floating negative resistance load

$$\begin{bmatrix} sB_1 + G_1 & sB_{12} \\ sB_{21} & sB_2 + G_2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} i_1 - g_{p2}v_1 - g_{p4}v_2 \\ i_2 - g_{p3}v_1 - g_{p5}v_2 \end{bmatrix} \quad \ldots(C.1)$$

The details describing the elements of (C.1) are presented in Table C.1.

Table C.1 – Details describing the admittance matrix elements (C.1)

$B_1 = C_{gdn\,1} + C_{dbn\,1} + C_{dbp\,2} + C_{gbp\,2} + C_{gsp\,2} + C_{dbp\,4} + C_{gdp\,4} + C_{gdp\,3} + C_{gbp\,3} + C_{gsp\,3}$
$B_2 = C_{gdn\,6} + C_{dbn\,6} + C_{gsp\,5} + C_{gbp\,5} + C_{dbp\,5} + C_{gdp\,3} + C_{dbp\,3} + C_{gdp\,4} + C_{gbp\,4} + C_{gsp\,4}$
$B_{12} = B_{21} = -C_{gdp\,4} - C_{gdp\,3}$; $G_1 = g_{dp\,2} + g_{dp\,4} + g_{dn\,1}$; $G_2 = g_{dn\,6} + g_{dp\,3} + g_{dp\,5}$

D Current Mirror Floating Negative Resistor

The AC equivalent model and nodal admittance matrix used to derive (3.14) are presented below. For this design transistors MP1 and MP6 operate in the triode region.

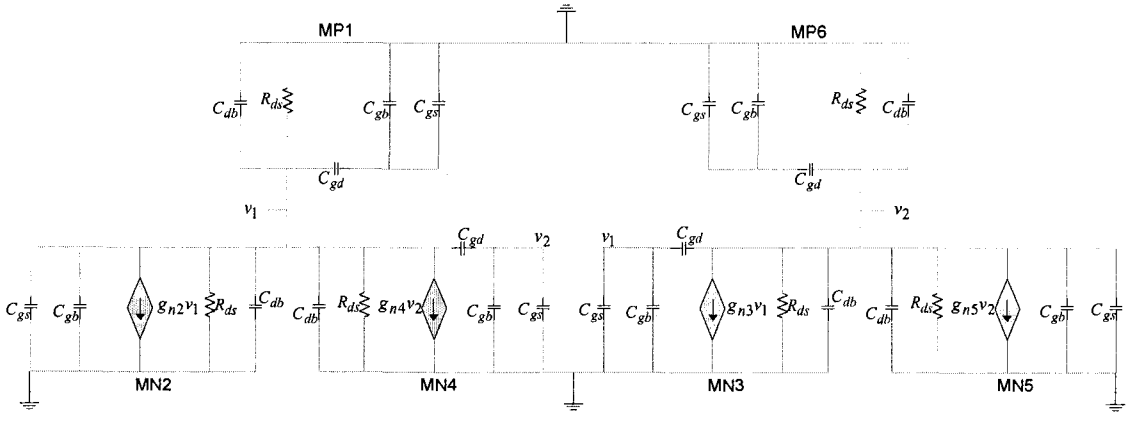


Figure D.1 –AC equivalent model of current mirror floating negative resistor

$$\begin{bmatrix} sB_1 + G_1 & sB_{12} \\ sB_{21} & sB_2 + G_2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} i_1 - g_{n2}v_1 - g_{n4}v_2 \\ i_2 - g_{n3}v_1 - g_{n5}v_2 \end{bmatrix} \quad \ldots(D.1)$$

The details describing the elements of (D.1) are given in Table D.1.

Table D.1 – Details describing the admittance matrix elements of (D.1)

$B_1 = C_{gdp\,1} + C_{dbp\,1} + C_{dbn\,2} + C_{gbn\,2} + C_{gsn\,2} + C_{gdn\,4} + C_{dbn\,4} + C_{gdn\,3} + C_{gbn\,3} + C_{gsn\,3}$
$B_2 = C_{gdp\,6} + C_{dbp\,6} + C_{gsn\,5} + C_{gbn\,5} + C_{dbn\,5} + C_{dbn\,3} + C_{gdn\,3} + C_{gdn\,4} + C_{gbn\,4} + C_{gsn\,4}$
$B_{12} = B_{21} = -C_{gdn\,4} - C_{gdn\,3}$; $G_1 = g_{dn\,2} + g_{dn\,4} + C_{dp\,1}$; $G_2 = g_{dp\,6} + g_{dn\,3} + g_{dn\,5}$

E Floating Negative Conductance Network

The AC equivalent model and nodal admittance matrix used to derive (3.15) are presented below.

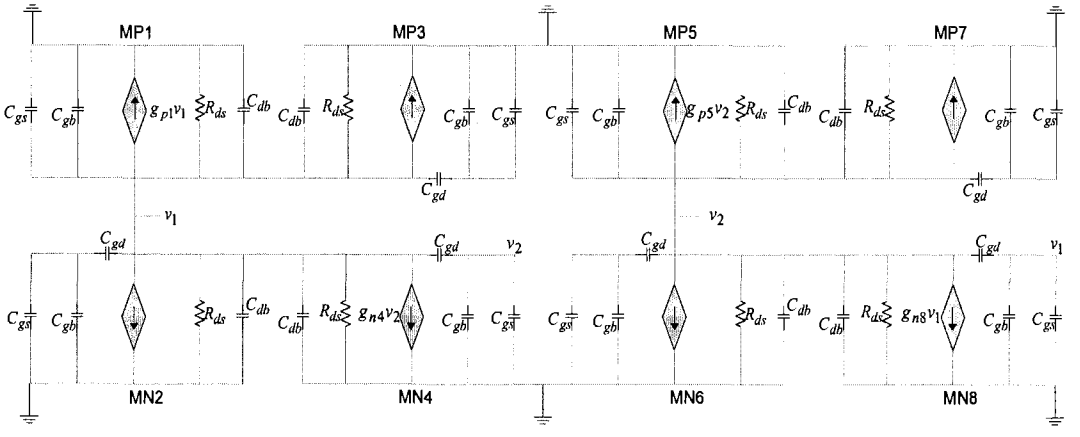


Figure E.1 –AC equivalent model of floating NCN

$$\begin{bmatrix} sB_1 + G_1 & sB_{12} \\ sB_{21} & sB_{22} + G_2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} i_1 - g_{p1}v_1 - g_{n4}v_2 \\ i_2 - g_{n8}v_1 - g_{p5}v_2 \end{bmatrix} \quad \ldots(E.1)$$

The details describing the elements of (E.1) are given in Table E.1.

Table E.1 – Details describing the admittance matrix elements of (E.1)

$$B_1 = C_{gsp1} + C_{gbp1} + C_{dbp1} + C_{dbp3} + C_{gdp3} + C_{gdn2} + C_{dbn2} + C_{dbn4} + C_{gdn4}$$
$$B_2 = C_{gsp5} + C_{gbp5} + C_{dbp5} + C_{gdn6} + C_{dbn6} + C_{gdn8} + C_{dbn8} + C_{gdp7} + C_{dbp7}$$
$$B_{12} = B_{21} = -C_{gdn4} - C_{gdn8};\ G_1 = g_{dp1} + g_{dp3} + g_{dn2} + g_{gn4};\ G_2 = g_{dp5} + g_{dp7} + g_{dn6} + g_{dn8}$$

F CMOS Inverter

The AC equivalent model and nodal admittance matrix used to derive (3.16) and (3.17) are presented below.

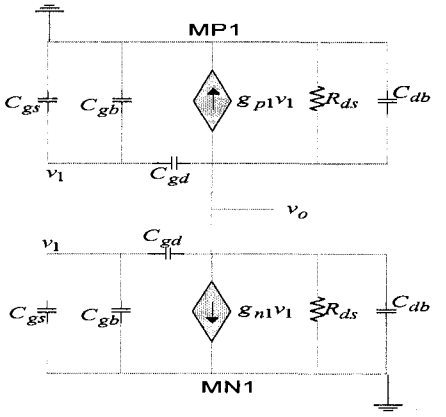


Figure F.1- AC equivalent model of CMOS inverter

$$\begin{bmatrix} sB_1+G_1 & sB_{1o} \\ sB_{o1} & sB_o+G_o \end{bmatrix} \begin{bmatrix} v_1 \\ v_o \end{bmatrix} = \begin{bmatrix} i_1 \\ i_o - g_{p1}v_1 - g_{n1}v_1 \end{bmatrix} \quad \ldots(F.1)$$

The details describing the elements of (F.1) are presented in Table F.1.

Table F.1 – Details describing the admittance matrix elements of (F.1)

$B_1 = C_{gsp1} + C_{gbp1} + C_{gdp1} + C_{gsn1} + C_{gbn1} + C_{gdn1}$; $B_o = C_{gdp1} + C_{dbp1} + C_{gdn1} + C_{dbn1}$ $B_{1o} = B_{o1} = -C_{gdp1} - C_{gdn1}$; $G_1 = 0$; $G_o = g_{dp1} + g_{dn1}$

G VCT with Single Current Mirror Load

The AC equivalent model of the VCT presented in Figure 3.9 is given below.

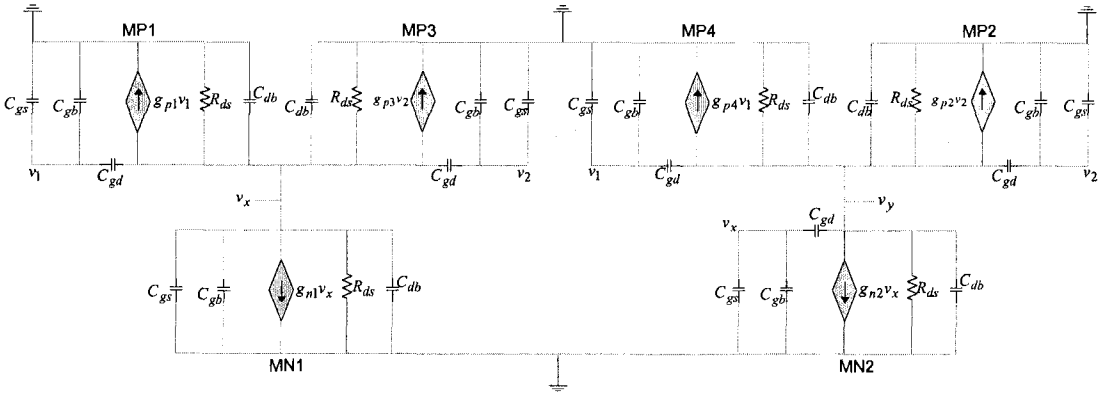


Figure G.1 – AC equivalent model of VCT

The nodal admittance matrix is derived as

$$\begin{bmatrix} sB_1 + G_1 & sB_{1x} & sB_{1y} \\ sB_{x1} & sB_x + G_x & sB_{xy} \\ sB_{y1} & sB_{yx} & sB_y + G_y \end{bmatrix} \begin{bmatrix} v_1 \\ v_x \\ v_y \end{bmatrix} = \begin{bmatrix} i_1 \\ i_x - g_{p1}v_1 - g_{n1}v_x \\ i_y - g_{p4}v_1 - g_{n2}v_x \end{bmatrix} \quad \ldots(G.1)$$

Suppressing node v_x results in a 2x2 matrix given by

$$\begin{bmatrix} sB_1 + G_1 - \dfrac{s^2B_{1x}B_{x1} + sB_{1x}g_{p1}}{sBx + G_x + g_{n1}} & sB_{1y} - \dfrac{s^2B_{1x}B_{xy}}{sB_x + G_x + g_{n1}} \\ sB_{y1} + g_{p4} - \dfrac{(sB_{yx} + g_{n2})(sB_{x1} + g_{p1})}{sB_x + G_x + g_{n1}} & sB_y + G_y - \dfrac{s^2B_{xy}B_{yx} + sB_{xy}g_{n2}}{sB_x + G_x + g_{n1}} \end{bmatrix} \begin{bmatrix} v_1 \\ v_y \end{bmatrix} = \begin{bmatrix} i_1 \\ i_y \end{bmatrix} \quad \ldots(G.2)$$

The details regarding the matrix elements are given in Table G.1. The transconductance of the VCT is determined as element Y_{21} in (G.2). Shorting the input and output terminals together results in the elements of the admittance matrix being added, producing an active resistance given by

$$R = \frac{1}{Y_{11} + Y_{12} + Y_{21} + Y_{22}} \quad \ldots(G.3)$$

Table G.1 – Details describing the admittance matrix elements of (G.1) and (G.2)

$$B_1 = C_{gsp1} + C_{gbp1} + C_{gdp1} + C_{gsp4} + C_{gbp4} + C_{gdp4};\ B_y = C_{gdn2} + C_{dbn2} + C_{gdp2} + C_{dbp2} + C_{gdp4} + C_{dbp4}$$

$$B_x = C_{gsn1} + C_{gbn1} + C_{dbn1} + C_{dbp1} + C_{gdp1} + C_{dbp3} + C_{gdp3} + C_{gsn2} + C_{gbn2} + C_{gdn2};\ B_{1x} = B_{x1} = -C_{gdp1}$$

$$B_{1y} = B_{y1} = -C_{gdp4};\ B_{xy} = B_{yx} = -C_{gdn2};\ G_x = g_{dn1} + g_{dp1} + g_{dp3};\ G_y = g_{dn2} + g_{dp4} + g_{dp2};\ G_1 = 0$$

$$d_2 = B_1B_x - B_{1x}B_{x1} + B_{1y}B_x - B_{1x}B_{xy} + B_{y1}B_x - B_{yx}B_{x1} + B_yB_x - B_{xy}B_{yx};\ d_1 = G_1B_x + g_{n1}B_1 + B_1G_x$$

$$- B_{1x}g_{p1} + B_{1y}g_{n1} + B_{1y}G_x + g_{p4}B_x + B_{y1}g_{n1} + B_{y1}G_x - g_{n2}B_{x1} - B_{yx}g_{p1} + G_yB_x + B_yg_{n1} + B_yG_x + g_{n2}Bxy$$

$$d_0 = G_1g_{n1} + G_1G_x + g_{p4}g_{n1} + g_{p4}G_x - g_{n2}g_{p1} + G_yg_{n1} + G_yG_x$$

H CMOS Voltage-to-Current Transducer

The nodal admittance matrix of the CMOS VCT shown in Figure 1.13 (with a double current mirror load) is derived as [7]

$$\begin{bmatrix} \hat{y}_{11} & \hat{y}_{13} & \hat{y}_{14} \\ \hat{y}_{31} & A & B \\ \hat{y}_{41} & C & D \end{bmatrix} \begin{bmatrix} v_1 \\ v_y \\ v_2 \end{bmatrix} = \begin{bmatrix} i_1 \\ i_y \\ i_2 \end{bmatrix} \qquad \ldots(H.1)$$

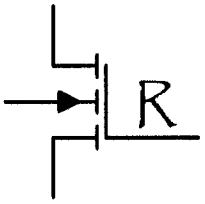
This VCT was used for the design of the active inductor described by (4.1). The details regarding the elements of (H.1) are given in Table H.1.

Table H.1

$$Y_{11}=sC_1;\ Y_{12}=-sC_{gd1};\ Y_{13}=-sC_{gd7};\ Y_{14}=Y_{15}=0;\ Y_{21}=g_{p1}-sC_{gd1};\ Y_{22}=G_1+g_{n1}+sC_2;$$
$$Y_{23}=-sC_{gd4};\ Y_{24}=Y_{25}=0;\ Y_{31}=g_{p4}-sC_{gd7};\ Y_{32}=g_{n2}-sC_{gd4};\ Y_{33}=G_2+sC_3;\ Y_{34}=g_{p2}-sC_{gd3};$$
$$Y_{35}=g_{n4}-sC_{gd8};\ Y_{41}=Y_{42}=0;\ Y_{43}=-sC_{gd3};\ Y_{44}=sC_4;\ Y_{45}=-sC_{gd5};\ Y_{51}=Y_{52}=0;\ Y_{53}=-sC_{gd8};$$
$$Y_{54}=g_{p3}-sC_{gd5};\ Y_{55}=g_{n3}+G_3+sC_5$$

$$C_1=C_{gs1}+C_{gb1}+C_{gd1}+C_{gs7}+C_{gb7}+C_{gd7};\ C_2=C_{db1}+C_{db2}+C_{gs2}+C_{gb2}+C_{gb4}+C_{gs4}+C_{gd1}+C_{gd3};$$
$$C_3=C_{db3}+C_{db4}+C_{db7}+C_{db8}+C_{gd8}+C_{gd7}+C_{gd4}+C_{gd3};\ C_4=C_{gs3}+C_{gd3}+C_{gb3}+C_{gs5}+C_{gb5}+C_{gd5};$$
$$C_5=C_{db5}+C_{gs6}+C_{db6}+C_{gs8}+C_{gb8}+C_{gb6}+C_{gd5}+C_{gd8};\ G_1=g_{ds1}+g_{ds2};\ G_2=g_{ds3}+g_{ds4}+g_{ds7}+g_{ds8};$$
$$G_3=g_{ds6}+g_{ds6};$$

$$\hat{y}_{11}=Y_{11}-Y_{12}Y_{21}/Y_{22};\ \hat{y}_{13}=Y_{13}-Y_{12}Y_{23}/Y_{22};\ \hat{y}_{14}=Y_{14}-Y_{12}Y_{24}/Y_{22};\ \hat{y}_{31}=Y_{31}-Y_{32}Y_{21}/Y_{22};\ \hat{y}_{41}=Y_{41}-Y_{42}Y_{21}/Y_{22};$$
$$A=Y_{33}-Y_{35}Y_{53}/Y_{55}-Y_{32}Y_{23}/Y_{22};\ B=Y_{34}-Y_{35}Y_{54}/Y_{55}-Y_{32}Y_{24}/Y_{22};$$
$$C=Y_{43}-Y_{45}Y_{53}/Y_{55}-Y_{42}Y_{23}/Y_{22};\ D=Y_{44}-Y_{45}Y_{54}/Y_{55}-Y_{42}Y_{24}/Y_{22};$$



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